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Par

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Conception et réalisation de transistors de puissance à base du GaN jusqu'en bande W

Design and fabrication of GaN-based field effect power transistors up to W-band

Soutenance le 16 décembre 2021 devant la Commission d'examen :

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Abstract

In the last decades, remarkable progresses have been achieved with GaN high electron mobility transistors (HEMTs) for use in high-frequency power amplification and switching applications. Currently, the most matured GaN HEMTs are based on AlGaN/GaN heterostructures. More recently, Al-rich ultrathin sub-10 nm (In)(Ga)AlN/GaN heterostructures have also received much attention for millimeter-wave applications. This is because in contrast to AlGaN/GaN, they can provide more than two times higher 2 Dimensional-Electron-Gas (2DEG) sheet carrier density while offering a high aspect ratio (gate length / gate to channel distance) down to sub-100 nm gate lengths. As a result, Al-rich ultrathin barrier GaN HEMTs are able to operate at much higher speed without the use of gate recess, thus potentially enabling high device reliability. In this frame, a number of research groups have demonstrated a unique combination of higher power and wider bandwidth using advanced GaN transistors all the way to 100 GHz as compared to other technologies (GaAs or Silicon). However, most of the applications require very high efficiency power amplifiers with high linearity and proven reliability under harsh conditions. Current state-of-the-art GaN HEMTs are limited to about 50% power-added-efficiency (PAE) in the Ka band and much lower at higher frequency. Moreover, very few reports are available on the device reliability for sub-150 nm gate lengths. On the other hand, one of the major limitations of modern RF devices is the thermal dissipation. The dissipated power improves by 80% when the PAE increases from 50% to 80%.

The aim of this work is to provide leading edge technologies in this field through the development and the improvement of sub-150 nm GaN transistors for high frequency applications. In particular, we have performed an extensive buffer engineering while carefully optimizing an ultrathin sub-5nm AlN barrier layer in order to maximize the power gain, improve the electron confinement under high electric and simultaneously reduce the trapping effects. Furthermore, the development of a power bench at 94 GHz enabled the demonstration of a record W-band output power density with the fabricated devices. This is believed to constitute a decisive asset in securing high performances and reliable GaN devices for next-generation millimeter-wave amplifiers related to future 5G telecommunications, space or military applications.

Key words: GaN, Heterostructure, Ultra-thin barrier layers, HEMT, Q-band, W-band, Millimeter-wave, High frequency, Load-pull

Résumé

Au cours des dernières décennies, des progrès remarquables ont été réalisés sur les transistors à haute mobilité électronique à base de GaN (HEMTs GaN) destinés aux applications d'amplification et de commutation de puissance à haute fréquence. Actuellement, les HEMTs GaN les plus matures sont basés sur des hétérostructures AlGaN/GaN. Plus récemment, les hétérostructures à barrières ultrafines (<10 nm) (In)(Ga)AlN/GaN riches en Al ont également présentées beaucoup d'intérêt pour les applications en gamme d'ondes millimétriques. En effet, contrairement aux structures AlGaN/GaN, les barrières ultrafines riches en Al peuvent fournir une densité d'électrons (2DEG) deux fois plus élevée tout en offrant un rapport d'aspect important (longueur de grille / distance grille-canal) y compris avec des grilles très courtes inferieures à 100 nm. Par conséquent, les HEMTs GaN à barrière ultrafine riche en Al permettent de fonctionner à une fréquence plus élevée de manière robuste. Dans ce contexte, plusieurs groupes de recherche ont démontré une combinaison unique de puissance plus élevée et une bande passante plus large jusqu'à 100 GHz par l'utilisation de transistors GaN par rapport aux autres technologies (GaAs ou silicium). Cependant, la plupart des applications nécessitent des amplificateurs de puissance à très haut rendement associé à une fiabilité éprouvée et une linéarité accrue. L'état de l'art des HEMTs GaN est limité aujourd'hui à environ 50% de rendement PAE (Power Added Efficiency) et peu de travaux reportés sur la fiabilité des composants GaN utilisant des grilles courtes inferieures à 150 nm. Néanmoins, l'une des limitations majeures des composants RF modernes est la dissipation thermique. En effet, la puissance dissipée s'améliore de 80% lorsque le rendement PAE passe de 50% à 80%.

L'objectif de ce travail est de fournir une technologie de pointe dans ce domaine avec le développement et l'optimisation de transistors GaN à grille sub-150 nm pour les applications en gamme d'ondes millimétriques. En particulier, nous avons effectué une optimisation des couches tampons (buffer) tout en optimisant une barrière AlN ultrafine inférieure à 5 nm afin d'augmenter le gain de puissance, d'améliorer le confinement des électrons sous fort champ électrique et de simultanément réduire les effets de pièges. De plus, le développement d'un banc de mesures de puissance à 94 GHz a permis de démontrer une densité de puissance à l'état de l'art en bande W avec les composants fabriqués. Ces travaux constituent une base de travail prometteuse pour garantir des performances élevées (notamment le rendement PAE) et fiables des HEMTs GaN pour l'amplification de puissance en gamme d'ondes millimétriques liée aux futures applications de télécommunication 5G, spatiales ou militaires.

Mots clé : GaN, Hétérostructure, Barrières ultrafines, HEMT, bande Q, bande W, ondes millimétriques, Haute fréquence, Load-pull

Summary

Introduction

1) Context of study

The last century has seen a remarkable evolution in the fields of science and technology related to many applications such as defense, military, space applications and wireless communications through the development and improvement of micro and nano-electronic devices. Most of the burden of microelectronics industry has been shouldered by the silicon (Si) material system. This is mainly due to the low cost and availability of Si worldwide. Nevertheless, progress in output power, gain and operating frequency are continually being achieved afterward.

Recent literature has demonstrated that Si-based devices, such as complementary metal oxide semiconductor (CMOS), Si-on-insulator (SOI) can achieve relatively high power at high frequencies. Consequently, they can be applied to high-power applications requiring a few watts below Ka-band. However, at higher frequencies, Si-based devices are limited to deliver the necessary output power due to the material constrains of Si. As a result, the industry has been looking for alternate materials in order to go beyond the limits of Si particularly III-V wide band-gap semiconductors such as Gallium Arsenide (GaAs) [1][2][3], Indium Phosphide (InP) [4][5][6] and Gallium Nitride (GaN) [7] which present a way forward towards achieving the desired performances. Indeed, the recent trend in RF and microwave applications is toward circuits that are reliable with low power consumption and low cost. Devices based on III-V materials like GaAs MESFETs, InP Heterojunction Bipolar Transistors (HBTs), GaAs High Electron Mobility Transistors (HEMTs) have been the preferred choice for Monolithic Microwave Integrated Circuits (MMICs).

Despite the excellent achievements, InP- and GaAs-based power amplifiers operating at higher frequency are also limited in saturated power levels because of the low breakdown voltage and related drain bias operation. Moreover, the increasing applications in RF domain required circuits that are highly miniaturized integrated delivering high power at high frequency range. GaN has emerged as strong and promising material to replace the existing technologies and to cater to the needs of these applications. The superior properties and mechanical robustness together with the capability to operate at high temperature as compared to Si, GaAs and InP materials are additional benefits of GaN. GaN MMICs revolutionize the field of millimeter-wave solid-state power amplifiers (SSPAs) and enable new applications that were previously not practical because of the limited output power of SSPAs and large size of traveling wave tube amplifiers (TWTAs). This strongly motivates operators and industries to turn their attention towards new frequency bands and especially millimeter-wave bands that cover frequency between 30 GHz and 300 GHz.

2) Interest of millimeter-wave band

As device technology improves, emerging application systems are moving forward to higher frequencies. A diagram of the entire electromagnetic spectrum is shown in **Figure.1**. In the past decade, an impressive development has extended the capability of detection based on magnetic, acoustic, ultrasound, microwave, millimeter-wave, Terahertz, infrared and X-ray sensors.

Historically, the lowest frequency bands have been used by the early radio systems for simple voice communication with sufficient bandwidth. As technology enhanced and wireless communication increased in size as well as complexity, system designers require more bandwidth at higher frequencies. The first exploration of the microwave spectrum, however, was done in the development of radar for military applications, where higher frequency allows high antenna resolution.

As engineers pushed higher in frequency for RF applications, interest in millimeter-wave band increases. Millimeter-wave radiation occupies a region of the electromagnetic spectrum between microwaves and terahertz. Thanks to its reduced wavelength from 30 GHz (10 mm wavelength) to 300 GHz (1 mm wavelength), millimeter-wave radiation has better transmission properties through most dielectrics, good penetration ability and high resolution. It is able to pass through obscurants such as fog, cloud and smoke. In addition, mm-W radiation is non-ionizing.

Although THz provides high resolution, it does not allow a large scene illumination due to the high atmospheric absorption and its medium penetration. Infrared technique is not the appropriate alternative and does not meet the requirements because of its low penetration. On the other hand, X-ray imager limits the human body illumination due to its safety concerns (ionizing radiation) and low range of detection and imaging. Therefore, the choice of mm-wave system is the most suitable solution to meet the requirement thanks to its properties and wide available bandwidth which enable smaller components with improved performances.

The transmission characteristics of millimeter-wave radiation are highly affected by the Earth's atmosphere. **Figure.1.2** shows the attenuation of electromagnetic radiation in the atmosphere as a function of frequency at a given temperature, pressure, and humidity. The attenuation in the atmosphere from millimeter-wave to THz region is marked by several resonant peaks of high attenuation and windows of lower attenuation between the peaks. These peaks render the atmosphere nearly opaque to most of the sub-mm and far-infrared wavelengths. It can be noticed that wavelengths in the windows are the ones typically used for transmission in this region.

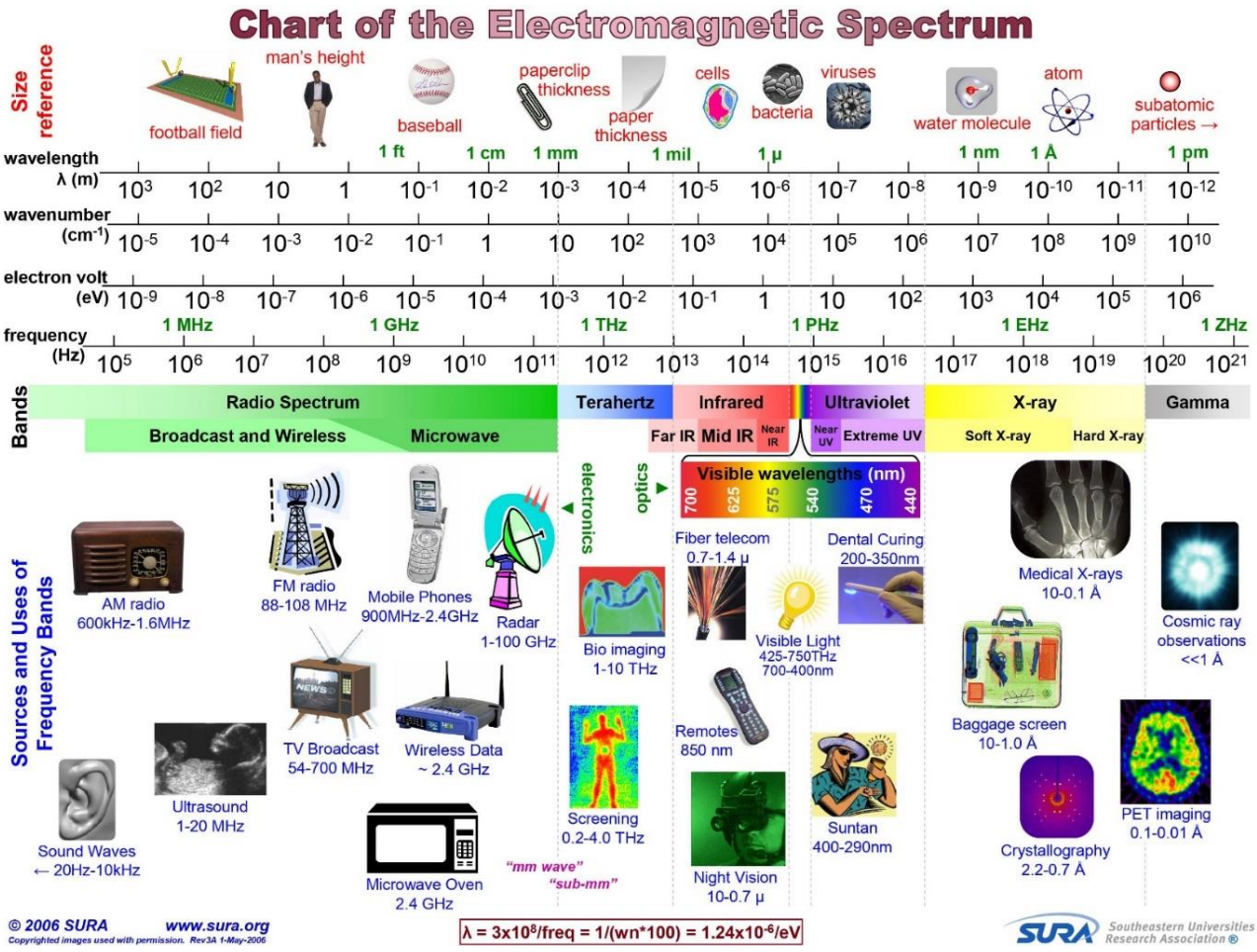


Figure.1.1 The electromagnetic spectrum as measured in wavelength (m), wavenumber (cm^{-1}), energy (eV), and frequency (Hz). www.sura.org

Continuing even higher in frequency, the absorption characteristics become dominated by molecular vibration and electron transition energy levels. Therefore, the attenuation increases with frequency starting in the microwave region until far-infrared region, then falls eventually through the infrared until reaching a minimum in the visible region. While the millimeter-wave region provides low attenuation and broad propagation windows the attenuation within the sub- millimeter-wave and THz regions rises to 100 dB/km and more. Millimeter-wave systems can be operated under humid, moistly, and rainy conditions. Also dust and fog can be propagated easily. It has the capability to operate during day and nighttime and under bad weather conditions. Moreover, it can "see through" some wall material such as drywall or dry plywood, but not through structural materials or metal sheets.

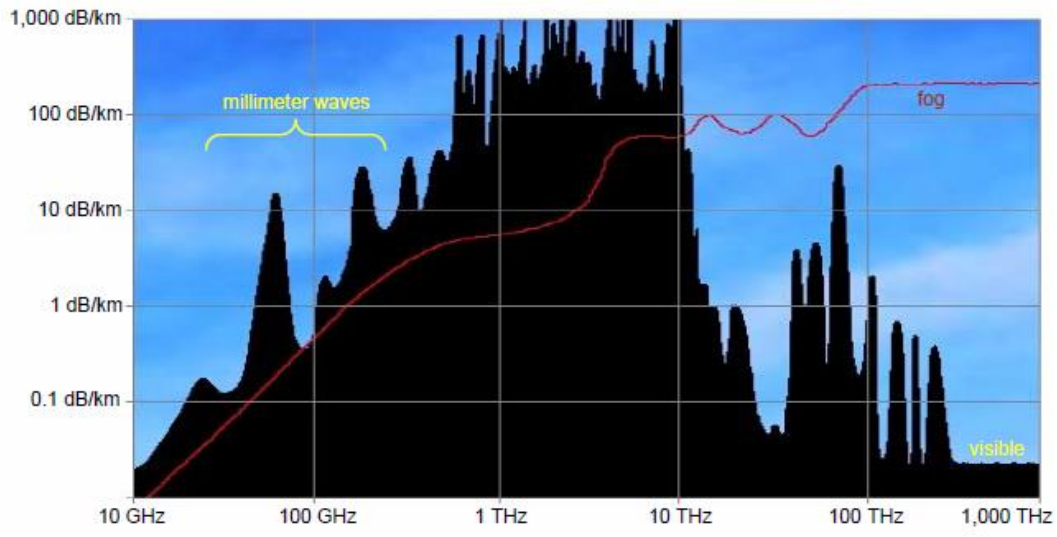


Figure.1.2. Absorption features in Earth's atmosphere

3) Thesis organization

This thesis work is part of several projects (FUI VeGaN, ANR COMPACT, EU EDA EUGaNiC and DGA-CNRS GREAT) at IEMN with the aim of developing a new GaN technology on SiC substrates for Ka and W-band frequency. The process is described in **Figure.1.3**. Between the epitaxial structure growth and the targeted applications, there are several steps, which are part of this thesis work.

This approach begins with device fabrication at IEMN using various epitaxial structures grown by different suppliers (Soitec, Veeco, SweGaN). Investigated research in this work for GaN technology development has several objectives: first, the development of a robust technology with high millimeter-wave performances while maintaining high operating voltages (V_{DS} > 20V). Second, a technology that will push the limits in terms of power density, current density and especially high power-added-efficiency. Third, a technology with a reduced impact of thermal and trapping effects.

Subsequently, in order to evaluate the heterostructure and the transistor performances, advanced characterizations are necessary. Several types of characterizations are carried out: static, small signal, pulsed and large signal at IEMN (details will be given in the next chapter) and structural characterizations.

Electric characterization is followed by a modelling step with the aim of implementing physical phenomena within a component using electrical diagram based on transistors and elementary components (capacitance, inductance, resistance…).

Once the electrical model reproduces the component behavior, the next step is to design the circuits. These devices typically perform functions such as microwave mixing, power amplification, low-noise

amplification, and high-frequency switching. As part of this research, the design focused on power amplifiers. Precise specifications have been set for the design of these amplifiers in order to ensure required needs of industrial for emerging applications (Thales, BluWan, etc).

This work covers the following steps: GaN-based active device fabrication and electrical / structural characterizations in millimeter-wave frequency (Figure 3 in red). The aim is to support the development of a complete European supply chain from III-V semiconductor material to a demonstrator. This is believed to constitute a decisive asset in securing a reliable European source of GaN for next-generation millimeter-wave amplifiers related to future 5G telecommunications, space or military applications.

The thesis begins with **chapter 1**, which introduces GaN technology and its role for millimeter-wave applications and describes the main industrial and academic players. The overview includes GaN material properties, GaN-based heterostructures and intrinsic characteristics of III-nitrides semiconductors. Then, GaN HEMT structure and related technologies are described showing the advantages and limitations for high frequency applications. Finally, the device design, fabrication, and optimization of millimeter-wave GaN-based HEMT as well as state-of-the art GaN devices are presented.

Chapter 2 summarizes the device fabrication steps and optimizations of GaN-based HEMT technology for high frequency. An overview of the test benches used in the frame of this thesis are described (static, small signal and DC pulsed, large signal up to 40GHz). The development of a power measurement set-up for carrying-out active Load-pull measurements in continuous (CW) and pulsed mode up to 94GHz is reported.

Chapter 3 presents the structural and electrical characterization of GaN technology on silicon carbide substrates. In this chapter, several batches of HEMT structures are studied in order to analyze various parameters affecting the device performances and reliability. In particular, the impact of both the undoped GaN channel thickness, the carbon concentration within the buffer, and the AlN barrier thickness has been extensively studied by means of DC, pulsed, RF, power measurements up to 94 GHz, and structural analysis.

Chapter 4 gives an overview of other approaches for high frequency GaN HEMTs based on InAlGaN/GaN and thin-HEMT AlGaN/GaN technology. Structural and preliminary electrical characterizations are realized on the InAlGaN/GaN structure.

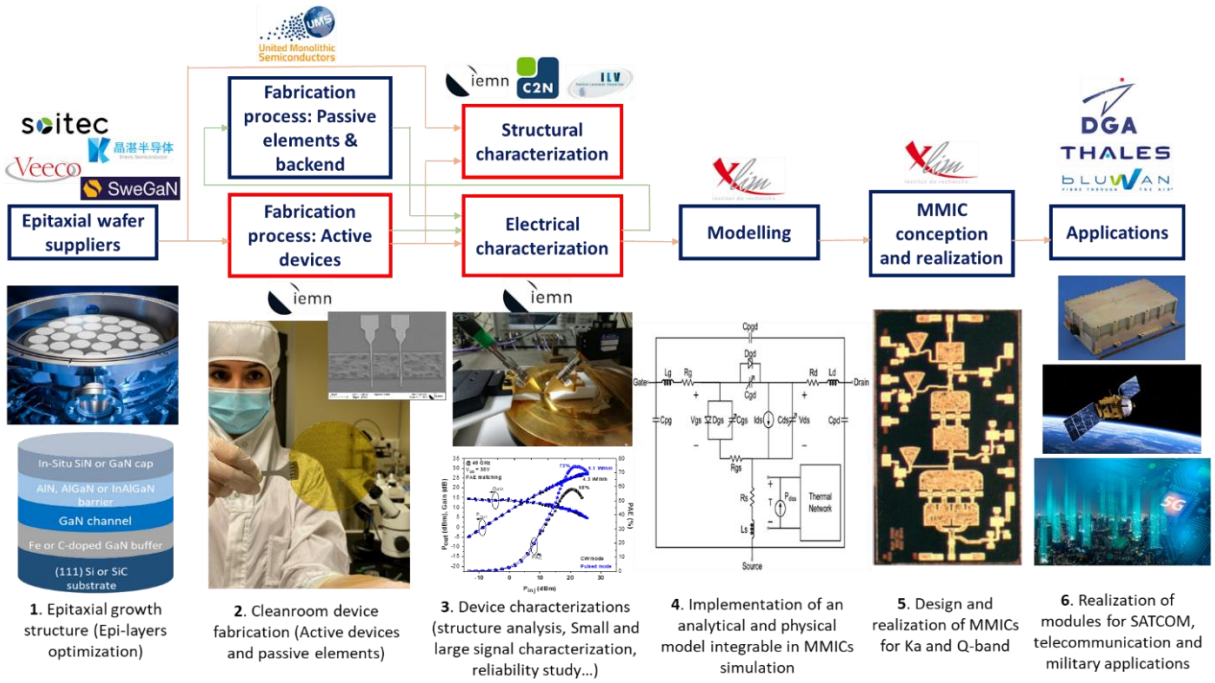


Figure.1.3. Simplified process of the GaN technology system realization

Chapter 1: GaN HEMTs – Technology and Overview

I. Introduction to GaN Technology

I.1 Targeted applications for GaN millimeter-wave

Recent improvement in GaN-based devices have allowed a demonstration of a variety of next generation millimeter-wave circuits. With its wide bandgap, high saturated electron velocity and higher breakdown voltage, GaN technology is a very promising candidate for realizing circuits with high power, high efficiency and wide operational bandwidth. GaN has also a high thermal conductivity, which combined with its wide bandgap makes them suitable for high temperature applications. These advantages are attractive for many applications such as defense and military, space applications and next-generation millimeter-wave amplifiers related to future 5G cellular telecommunications. Some of these applications are illustrated in **Figure.1.4.a**.

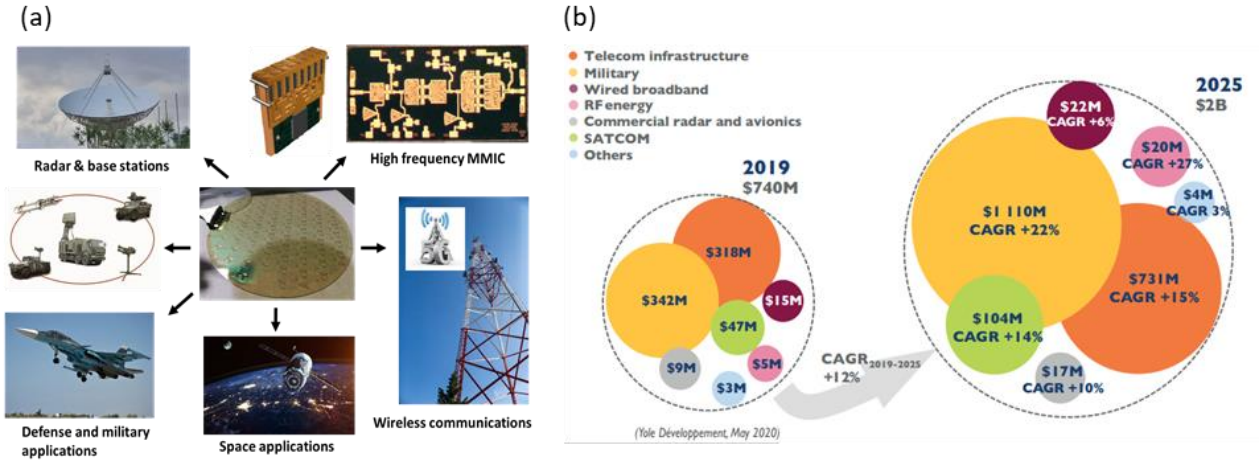


Figure.1.4. Illustration of some applications for GaN HEMTs (a), 2019-2025 packaged GaN RF device market forecast (b)

These applications have received a boost from the implementation of GaN technology in the past few years. The total GaN RF market will increases from $740M to more than $2B by 2025 in order to meet the needs of millimeter-wave spectrum (**Figure.1.4.b**) [8].

In telecom infrastructure, the wireless communication frontier is shifting from the current fourth generation (4G) to the forthcoming fifth generation (5G) while paving the way for millimeter-wave technology. GaN-based devices will overcome several challenges in order to meet ever-greater system level requirements especially in terms of efficiency, power levels and modulation bandwidth. The increase in bandwidth will favor increasing GaN deployment in the coming years.

For military applications, TWT-based systems have been replaced by GaN technology in order to improve the national security. While the demand is increasing for efficiency under harsh-conditions, GaN is a potential solution to satisfy the RF millimeter-wave transmitter/receiver module requirements for defense especially radar communication. The total GaN RF military market may surpass $1.1B in 2025.

For aerospace applications, some of the requirements for a device in a spacecraft are small size, and high/low temperature operation. Moreover, GaN-based devices deliver lower losses and have the capability to operate at high temperature. In addition, GaN material are inherently radiation-hard, which means that such devices are less sensitive to the radiation damaging effects. It can be noticed that no major European RF GaN devices industrial player has revealed any roadmap for radiation hard devices in millimeter-wave range dedicated to space up to now. The total GaN space application market will increase to more than $104M by 2025.

Such growth is explained by the fact that GaN will play a major role to satisfy such practical requirements of high-power amplification, broadband amplifiers and emerging 5G wireless communication network.

I.1.1. High power amplification

Recent and ongoing progress in semiconductor device fabrication and processing technology has pushed the limits of MMICs for millimeter-wave frequency. The first MMIC was reported in 1976 [9] and progress in output power, gain and operating frequency are continually being achieved afterwards. Indeed, MMIC components operating in millimeter-wave frequencies will be used to improve the sensitivity and performance of radiometers, receivers for communication systems and transceivers for radar instruments. Advanced GaN MMICs have demonstrated high power and recognized as a revolutionary technology, surpassing any other technologies such as GaAs and InP-based devices by a factor of 5 to 10 [7]. PAs-based on millimeter-wave GaN HEMT technology have been demonstrated up to W-band. **Figure.1.5** shows the main semiconductor technologies and their limits in terms of output power and operating frequency. State-of-the-art power level amplifiers have been reported with about 10 W and 3 W at Ka-band [10]–[12] and W-band [7][13]–[21] under continuous wave (CW) conditions, respectively. As expected, the output power decreases at higher frequencies due to the device scaling. Indeed, the gate length and the lateral device dimensions (gate-drain distance) are key parameters for high frequency operation. Furthermore, in order to reach high output power density, a high drain voltage is mandatory, which is typically inversely proportional to the device downscaling. On the other hand, spatial power combining enabled 5.2 W output power W-band GaN MMIC [22]. GaN is well known for its high output impedance and low output capacitance and high power MMIC performances.

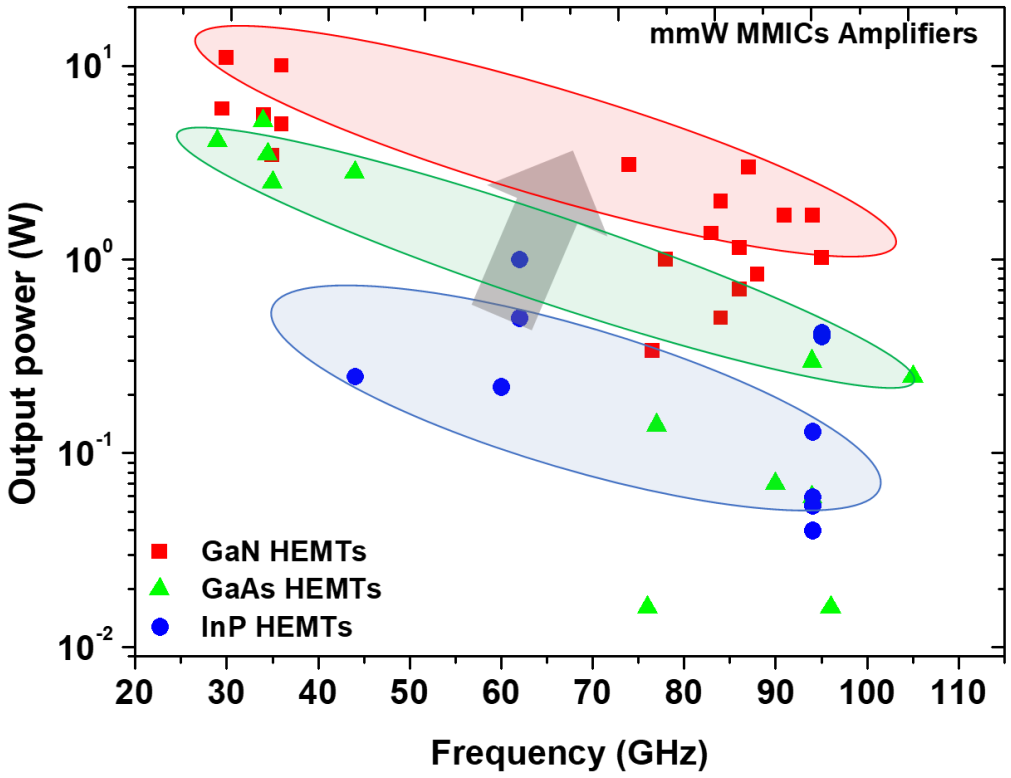


Figure.1.5. Output power of MMIC amplifiers under CW operation based on various semiconductor transistor technologies [23].

A summary of different MMICs designed in millimeter-wave frequency is shown in **Figure.1.6.** 3-stages Ka-band MMIC design based on AlGaN/GaN HEMTs fabricated on SiC is shown in **Figure.1.6.a** [12]. The measured results under CW operation for the balanced 3-stages demonstrate 9.5-11 W output power and 26-30% associated Power Added Efficiency (PAE) between 28-31 GHz. **Figure.1.6.b** illustrates Ka-band AlGaN/GaN HEMTs MMIC amplifier [24]. The designed amplifier is two-stage single-ended amplifier. The achieved output power under CW operation is 20 W and the PAE is 19% at 26.5 GHz. In the frequency range of (26 – 28) GHz the output power is greater than 15 W with an associated PAE of 13%. **Figure.1.6.c** shows a fabricated W-band GaN PA MMICs, which consist of two-stage cascade units with two transistors each and identical gate lengths in order to provide high gain and low loss matching circuit [14]. At 86 GHz, the maximum output power density was 3.6 W/mm with a PAE of 12.3% at V_{DS} = 20V under CW condition. **Figure.1.6.d** depicts a D-band PA MMICs using AlGaN/GaN HEMTs [25]. The MMIC consists of four actively matched cascode stages. Large signal measurements show a maximum output power density of 1.4 W/mm at 120 GHz at V_{DS} = 15V with associated PAE of 11.5%.

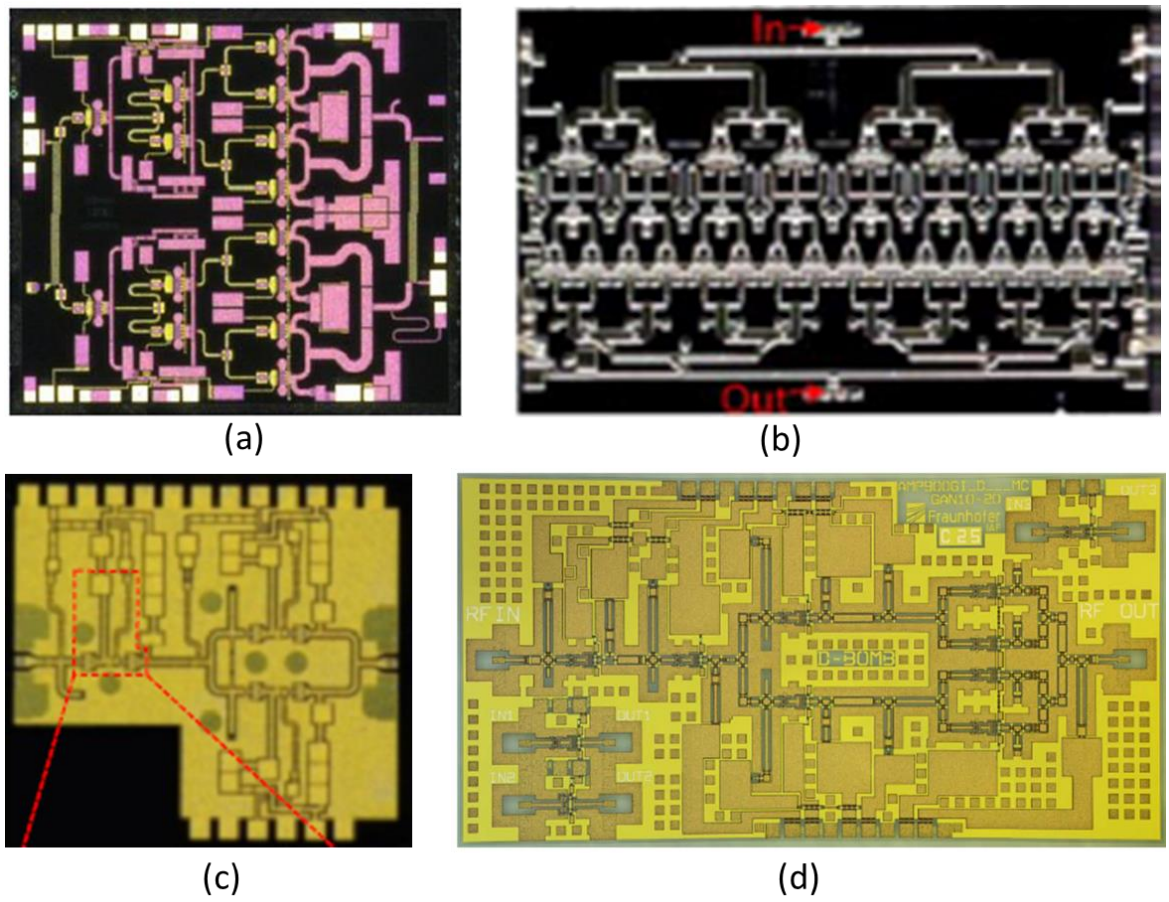


Figure.1.6. Examples of millimeter-wave MMICs at different frequencies: Ka-band (a)(b), W-band (c) and D-band (d).

I.1.2. Broadband amplifiers

Broadband power amplifiers have been considered as key components used in many applications such as instrumentation or communication systems that require the integration of several services with reduced number of components and size as well as operating in wide bandwidth. To date, systems covering a wide frequency range require multiple narrowband power amplifiers. Theses amplifiers are connected by means of switches or triplexers. In either case, the additional circuity causes losses and therefore such a system is not advantageous. A single broadband power amplifier covering multiple bands is necessary to replace multiple amplifiers in order to reduce costs and system complexity. Recently wideband power amplifier MMICs based on GaN have been largely used for high performance millimeter-wave components that are employed in emerged applications such as military and wireless communication. For 5G, GaN MMIC PAs are expected to be widely deployed in cellular base stations in order to reduce size and improve system integration. Therefore, it is essential for MMIC implementation to develop low-loss and compact

circuits in order to improve efficiency, output power, linearity, gain and bandwidth, which are key parameters to evaluate the power amplifiers performances.

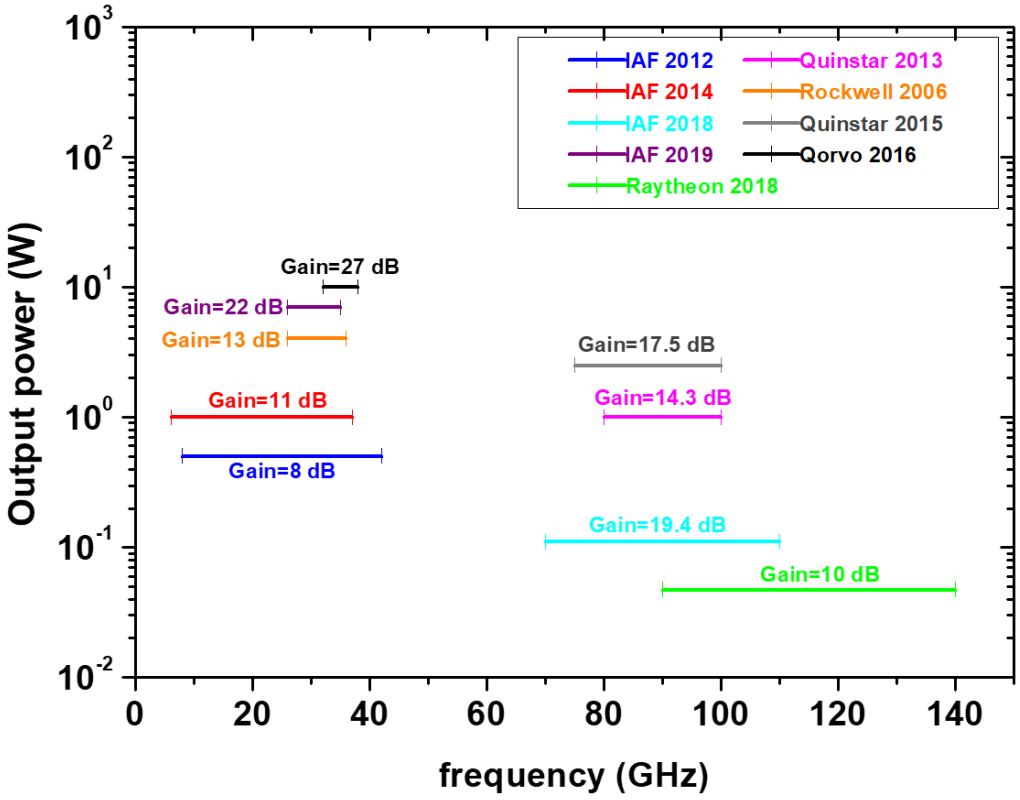


Figure.1.7. Output power of Broadband MMIC amplifiers [23].

The state-of-the-art broadband high-power millimeter-wave GaN MMIC is summarized in **Figure.1.7.** These results indicate the great potential of GaN-based PAs to increase solid-state power levels while maintaining wide bandwidth. Broadband GaN MMICs have been reported up to 140 GHz with output power ranging from 10 W over 32 – 38 GHz [11] to 47 mW over 90 – 140 GHz [26]. While these MMICs have produced attractive power levels, the highest output power is associated to a much narrower bandwidth as expected. However, by using on-chip traveling-wave power combiner circuit techniques, several watts output power using GaN MMICs have been reported by Quinstar with a bandwidth approaching the entire W-band [27]. Another reported technology enabling wide bandwidth amplifiers with high gain is the non-uniform distributed power amplifiers (NDPA). In this case, the amplifier uses dual-gate HEMTs in the driver stage of an NDPA, which boost the gain of the overall amplifier at wide bandwidth. IAF reported NDPA MMICs covering a frequency range from 6 – 37 GHz and from 8 – 42 GHz with an output power of 1 W and 500 mW with corresponding power gain above 11 dB and 8 dB, respectively [28][29].

I.1.3. Fifth generation wireless communication

To date, the wireless network evolution was principally driven by a need for higher data rate and the increasing number of connections for mobile communication, which offer exciting user experience in our every-day lives. Currently, the wireless communication frontier is shifting from the current fourth generation (4G) to the forthcoming fifth generation (5G). Major international communication companies and manufacturers are all competing to demonstrate 5G capabilities and features, while simultaneously paving the way for millimeter-wave technology that makes 5G fundamentally different from previous generations of mobile telecommunications. The broadband radio access and wireless networks cover several aspects of 5G, not only for the telecommunication industry but also for a wide range of sectors, including robotics, automotive, factory automation, healthcare, and education. Although the expected features and use cases for 5G are extensive and diverse, the start of 5G deployment will likely address only a few of the highlighted use cases through three scenarios: ultra-reliable low latency communications (uRLLC), enhanced mobile broadband (eMBB) and massive machine type communications (mMTC) as illustrated in **Figure.1.8**. Under the 5G umbrella, these scenarios have quite different system-level performance requirements such as latency, mobility, number of users and data rate while targeting to surpass any performances of previous mobile telecommunication generation.

The future 5G network for eMBB targets 20 Gb/s peak data rate, which represents ten times improvement compared with 4G LTE network. New waveform, along with Massive Input Massive Output (MIMO), beamforming and millimeter-wave technologies are considered as key features for 5G in order to reach dramatic network performance in terms of high efficiency, and high-power PA performance over a large frequency range, leading to low-cost, large bandwidth, and small size base-station system [30]. GaN will surpass conventional semiconductor materials for 5G network applications, requiring higher frequencies, tight integration, and minimal implementation cost while operating under harsh environments. Moreover, the device technology selection as well as the circuit configuration are critical in order to meet the complex requirements of PAs for 5G applications. As the development of GaN technology increases, advanced PA architectures have evolved in order to meet ever-greater system level requirements especially in term of efficiency, power levels and modulation bandwidth. Furthermore, silicon still dominates the sub-6 GHz band, but at higher frequencies, GaN is highly attractive. On the other hand, the critical allocation of spectrum will dictate the design and implementation of transceiver hardware. Therefore, the choice of millimeter-wave frequencies is required in order to extend the current 4G frequency band and to push the available spectrum limits for high data rates in the microwave range.

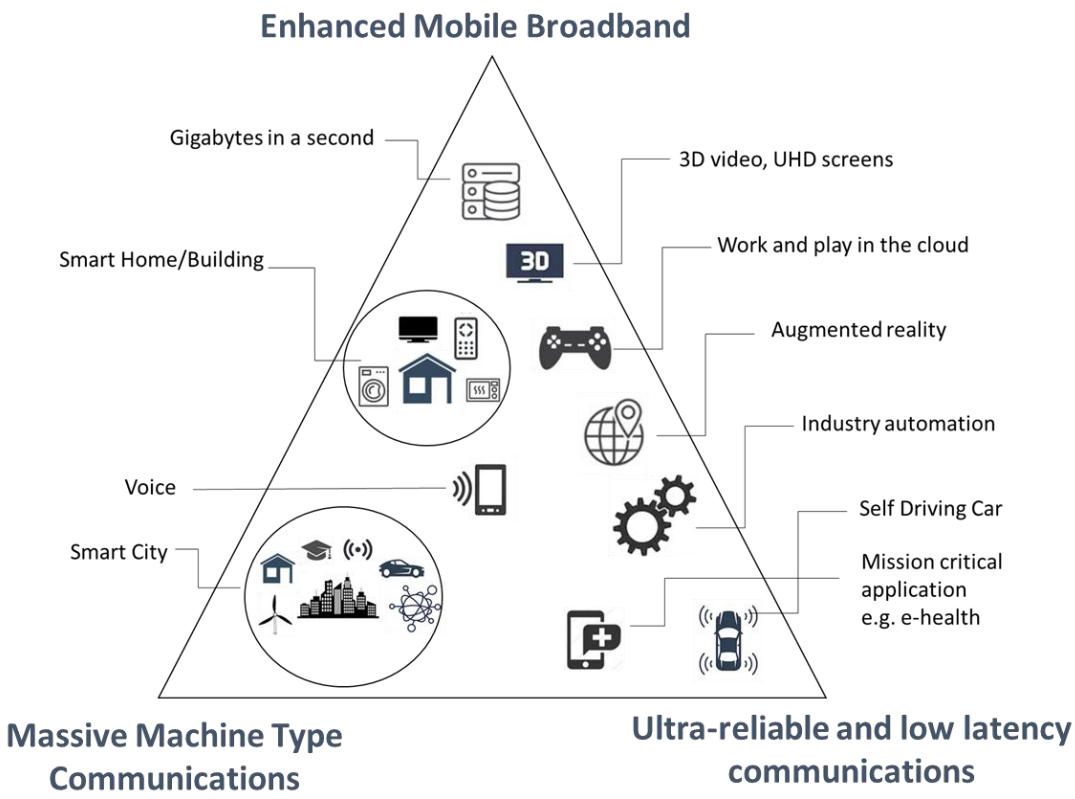


Figure.1.8. Some usage scenarios proposed by International Mobile Telecommunications (IMT)-2020 [31].

Recently, various GaN PAs have been reported in this frame. In order to increase data rate while operating at higher frequencies, modulated signals with large bandwidth and a more complex scheme are used. Moreover, with the increasing needs of efficiency under multiband, multimode operation, several approaches such as Doherty amplifiers, Envelope tracking amplifiers and a digital transmitter based on GaN have been demonstrated [32]–[34]. While millimeter-wave 5G is being developed, it will be first implemented on sub-6 GHz 5G systems using the same MIMO beamforming techniques but at lower and more technologically accessible frequencies [35]. 5G communication network is designed not only for spectrum bands below 6 GHz but also for high bands above 24 GHz. A number of sub-6 GHz 5G MIMO systems have been demonstrated at 3.3, 4.2 and 2.14 GHz [35][36]. In the millimeter-wave, several GaN PAs have been proposed. **Table.1.1** summarizes some performance results of PAs at different frequencies especially in Ka-band for 5G applications. Despite the proposed approaches, there are a large room for improvement of PA performances in order to satisfy such practical requirements of 5G wireless communication network, such as millimeter-wave, high linearity, high output power, large bandwidth and

compact size. GaN-based devices are among the most suitable for power amplifiers and will certainly play a major role as broadband technology for 5G wireless communication.

Table.1.1. Performance comparison of different PAs for 5G applications [24], [32], [35], [37]–[40].

Reference	Type	Size	F (GHz)	P_{out} (dBm)	PAE (%)	PAR (dBm)	Gain (dB)
[32]	PA	2.9 mm × 1.7 mm²	26.5 – 29.5	36.9 to 38	17.9 to 23	NA	NA
[35]	Doherty PA	1.8 mm × 1.7 mm	28	36	51	NA	30
[37]	Switching mode PA	NA	28 – 39	24.3	59	NA	8.2
[24]	PA	3.8 mm × 6.2 mm²	26 – 28	43.3 to 41.6	19.8 to 13.2	NA	NA
[38]	HPA	3.4 mm × 3.3 mm	26.5 – 29	39	25	NA	21.1 to 24
[39]	Doherty	3.4 mm × 2 mm²	23	36.9	27	29.4	15.4
[40]	Doherty PA	2.7 mm × 1.6 mm²	27.5 – 29.5	35.6	25.5	NA	NA

The 5G network system has been defined as the key for IoE application. Research efforts invested in millimeter-wave wireless communications and the success of 5G tests have enabled the commercialization and deployment of 5G wireless networks since 2020. The increasing number of new applications such as wireless backhaul, VR/AR and space travel makes it questionable whether they can satisfy emerging services and newer applications that have not been conceived yet. This creates a motivation towards sixth generation (6G) networks. Future 6G wireless communication will be implemented in 2030 [41] with devices operating up to the THz range. The key figure of merits for the evaluation of 6G wireless networks include a peak data rate of 1 Tb/s, which is 100 times that of 5G, a latency of 10 – 100 μs, an energy efficiency of 10 – 100 times better than 5G. The level of 6G maturity reachable in ten years by sub-THz can make this technology a powerful enabler.

II. GaN material system and properties

II.1. Crystal structure

The III-Nitride semiconductors group (AlN, GaN, and InN) can be found in three following common structures: rock-salt, wurtzite (hexagonal), and zinc-blend (cubic) crystal structures. The rock-salt structure is not relevant to electronic devices so far. The zinc-blend structure is the thermodynamically metastable polytype of GaN. It is used for device applications such as smaller bandgap and higher carrier

mobility due to the higher electron drift mobility and lower effective mass compared to wurtzite structure. At room temperature and atmospheric pressure, the wurtzite hexagonal structure is the thermodynamically stable crystal phase of nitride semiconductors. This structure is therefore the most commonly used for GaN-based HEMTs growth. The chemical bonds of III-nitride such as GaN are predominantly covalent, which means that each atom is tetrahedrally bonded to four atoms of the other type (see **Figure.1.9**). In addition, because of the large difference in electronegativity of Ga and N atoms, there is an ionic contribution of the bond which determines the stability of the structural phase. The GaN wurtzite structure has no inversion symmetry in the [0001] direction (c-axis). As a result, depending on whether the material is grown with Ga or N on top, it is possible to distinguish two different orientations of GaN crystals commonly known as Ga-face and the N-face, which correspond to the [0001], and $[000\bar{1}]$ crystalline faces as shown in **Figure.1.9**.

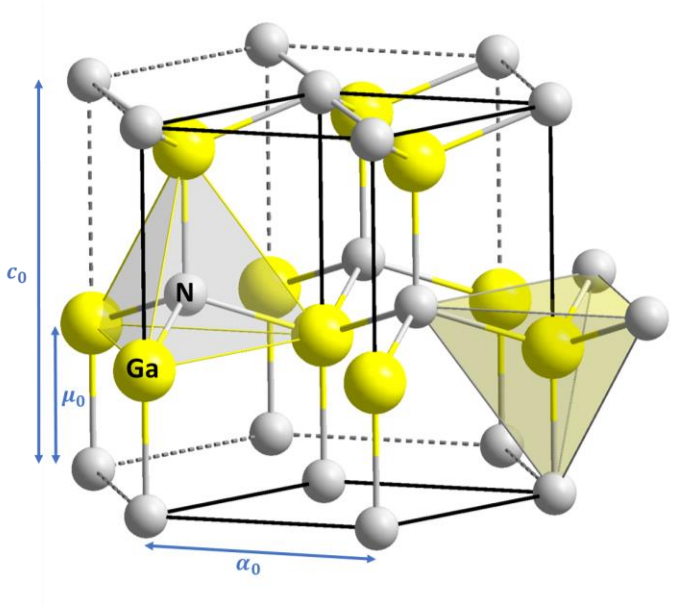


Figure.1.9. Hexagonal wurtzite crystal GaN

These two faces have different chemical properties: N-face crystal is chemically active which allows wet-chemical material etching. Therefore, they suffer from a rough surface morphology. Ga-face crystal is more chemically inert and presents much smoother surface morphology. In addition, Ga-face incorporates easier acceptors, while the N-face incorporates easier donors. Therefore, Ga-face is preferred for device operation thanks to its high electron transport properties.

The wurtzite crystal lattice parameters can be defined by the edge length of the basal hexagon a_0 (3.189Å), the height of the hexagonal lattice cell c_0 (5.185Å) and the internal parameter μ_0 defined as the length of the bond parallel to the c-axis, in units of c_0 as shown in **Figure.1.9**. The Ga and N atoms are arranged in two interpenetrating hexagonal closey packed lattice with a shift of 3/8 c_0. The subscript '0'

indicates that these values are those of the equilibrium lattice. **Table.1.2** shows an overview of these lattice parameters of wurtzite III-nitrides. Knowing that the ideal ratio lattice constant is $c_0/a_0 = 1.633$, GaN is the closest to the ideal wurtzite structure followed by InN and AlN. The increasing of the non-ideality crystal structure (μ_0 increases, c_0/a_0 ratio decreases) allows an increase of the spontaneous polarization which will be discussed in the next section [42] [43].

Table.1.2. Lattice constants of GaN, InN and AlN

Parameters	GaN	InN	AlN
α_0 (Å)	3.189	3.54	3.112
c_0 (Å)	5.185	5.705	4.982
c_0/α_0	1.627 [42] 1.634 [43]	1.612 [42] 1.627 [43]	1.601 [42] 1.619 [43]
μ_0	0.376 [43]	0.377 [43]	0.380 [43]

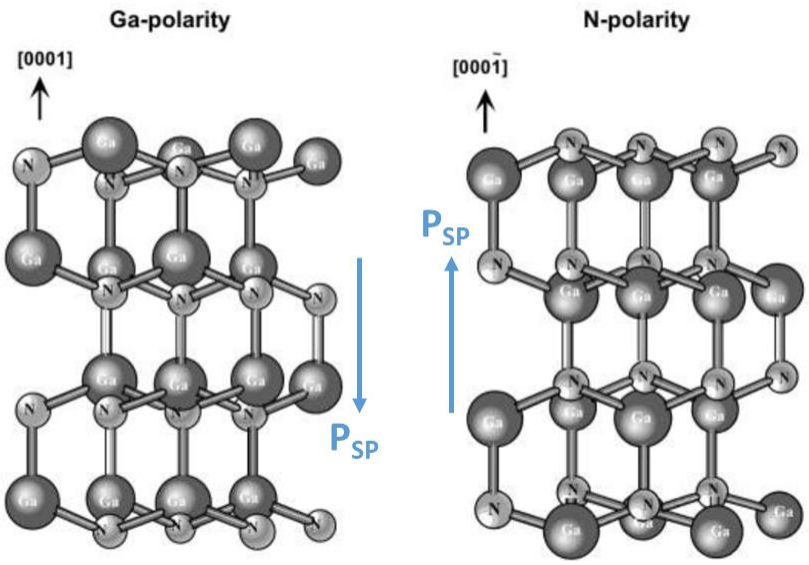


Figure.1.10. Hexagonal wurtzite crystal GaN: Ga-face polarity and N-face polarity

II.2. Polarization effect

Polarization effect in III-nitrides is a crucial material property. The total polarization is the sum of spontaneous polarization P_{SP} and piezoelectric polarization P_{PE}. The spontaneous polarization is induced because of the polar nature of III-N bonds and the low inversion symmetry of the crystal, which is due to

the large difference in electronegativity of Ga and N atoms. Indeed, Ga and N atoms exhibits anionic and cationic characteristics, respectively, thus resulting in negative spontaneous polarization along c-axis given by $P_{SP} = P_{SP}.\hat{z}$. "Spontaneous" means that the polarization is present at thermodynamic equilibrium in the absence of constraints and "negative" because the vector P_{SP} is pointing opposite to the c-axis as illustrated in **Figure.1.10**. As a result, P_{SP} increases with decreasing the c_0/a_0 ratio. For example, AlN crystal with a c_0/a_0 of 1.619 presents a higher P_{SP} (-0.081 C/m²) with respect to a GaN crystal (-0.029 C/m²) which have a c_0/a_0 ratio of 1.634 [43].

Moreover, an additional contribution to the polarization called piezoelectric P_{PE} is induced when external stress changes the ideality of the structure and the c_0/a_0 ratio. The P_{PE} is due to the mechanical deformation and the condition for a structure to exhibit P_{PE} is to lack a center of symmetry. A standard AlGaN/GaN heterostructure is grown along the c-axis direction. Furthermore, due to the different energy gaps between AlGaN film and GaN, the band diagram shows an energy discontinuity. In addition, the constant of AlGaN has to match the lattice constant of GaN ($a_0^{GaN} > a_0^{AlGaN}$), which induces a strong stress on the grown AlGaN layer. This stress causes strain in both basal plane and growth direction in order to compensate the in-plane lattice mismatch. Within the strained AlGaN/GaN heterostructure, the P_{PE} is induced along the c-axis (growth direction) or in the basal plane. The relevant relationship is [42]:

$$P_{PE} = e_{33}\,\epsilon_Z + e_{31}\left(\epsilon_x + \epsilon_y\right) \quad (1)$$

Where $\epsilon_z = \frac{(c - c_0)}{c_0}$ is the strain along the c-axis, $\epsilon_x = \epsilon_y = (a - a_0)/a_0$ are the in-plane strain assumed to be isotropic, e_{33}, e_{31} are the piezoelectric coefficients, and a and c are the lattice constants of the strained layer. The relation between the lattice constants in the hexagonal structure is given by [42]:

$$\frac{c - c_0}{c_0} = -2\,\frac{C_{13}}{C_{33}}\,\frac{a - a_0}{a_0} \quad (2)$$

Where C_{13} and C_{33} are elastic constants. Combining the equations (1) and (2) the P_{PE} along the c-axis can be also expected as [42]:

$$P_{PE} = 2\,\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\,\frac{C_{13}}{C_{33}}\right) \quad (3)$$

The piezoelectric polarization is negative for tensile strain and positive for compressive strain. Furthermore, the orientation of the piezoelectric and the spontaneous polarization is parallel in the case of tensile strain (AlGaN/GaN heterostructure), and antiparallel in the case of compressively strained AlGaN barrier (GaN/AlGaN heterostructure). For Ga-polar AlGaN/GaN heterostructure under tensile strain, the

piezoelectric and spontaneous polarization point in the same direction toward the GaN substrate as shown in **Figure.1.10**.

The polarization induced charge density in space is given by:

$$\sigma_p = -\nabla P \quad (4)$$

The polarization gradient at the interface of an AlGaN/GaN heterostructure determines a polarization induced charge density defined by:

$$|\sigma(x)| = |[P_{SP}(AlGaN) + P_{PE}(AlGaN) - P_{SP}(GaN)]| \quad (5)$$

For Ga-face AlGaN/GaN structure, the polarization induced sheet charge is found to be positive $(+\sigma)$. Therefore, free electrons tend to compensate the charges induced by polarization generating "Two Dimensional Electron Gas" (2DEG). The 2DEG is accumulated in the triangular quantum well at the lower AlGaN/GaN interface below the fermi level E_F as shown in **Figure.1.11**.

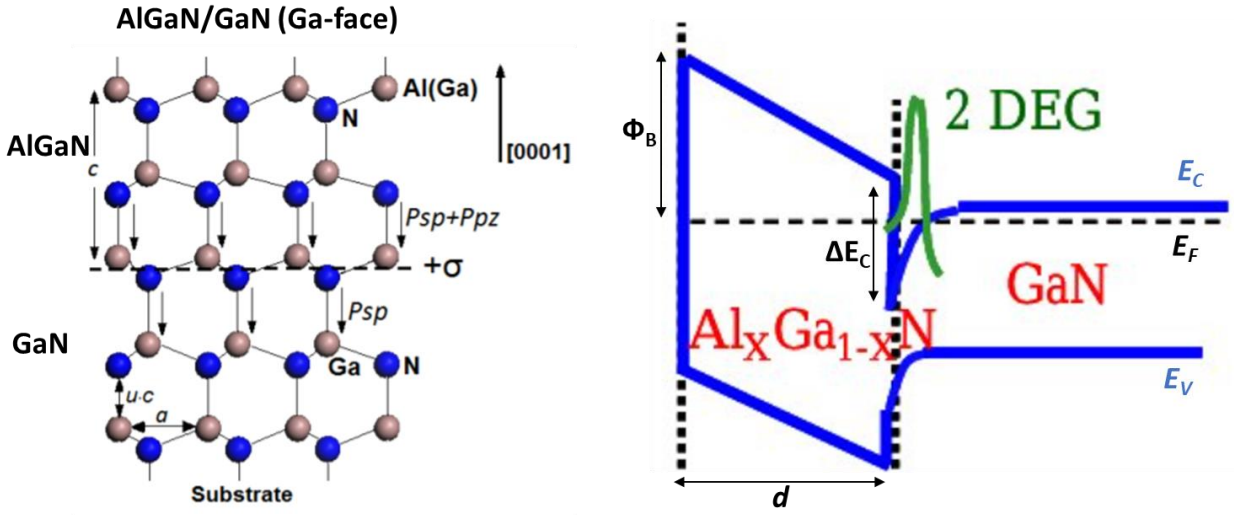


Figure.1.11. (a) Schematic of AlGaN/GaN heterostructure showing the spontaneous and piezoelectric polarization vector and (b) schematic band diagram of an AlGaN/GaN heterostructure [46].

In the case of N-face polarity, the spontaneous and piezoelectric polarizations have opposite directions to Ga-face polarity (point away from the substrate), which results in a negative polarization induced sheet charge density $(-\sigma)$. The negative sheet charge density causes an accumulation of holes at the interface, which assists to the formation of a "Two Dimensional Hole Gas" (2DEHG) upper GaN/AlGaN interface.

In a real AlGaN/GaN device, Schottky metal contact is formed by the gate electrode and the channel at the AlGaN interface. Therefore, the sheet carrier density of the 2DEG is modulated via external gate voltage bias. The maximum sheet electron concentration $n_s(x)$ can be expected as [42]:

$$n_s(x) = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{de^2}\right)[e\emptyset_b(x) + E_F(x) - \Delta E_C(x)] \quad (6)$$

Where, d is the thickness of the barrier layer, $\epsilon(x)$ is the relative dielectric constant of AlGaN, $e\emptyset_b(x)$ is the effective Schottky barrier of the gate contact, $E_F(x)$ is the fermi level with respect to the GaN conduction-band-edge energy, and $\Delta E_C(x)$ is the conduction band offset at the AlGaN/GaN interface.

The sheet carrier density of the 2DEG for a conventional AlGaN/GaN heterostructure is usually around 1×10^{13} cm^{-2} with an electron mobility around 2000 cm²/V.s [44][45]. It is found from Eq (6) that the sheet carrier concentration is dominated by the total polarization induced sheet charge, which can be controlled by the alloy composition and the thickness of the barrier layer. Several barrier layers especially ultrathin Al-rich material have been studied for millimeter-wave device applications. This part will be explained in more detail in the next sections.

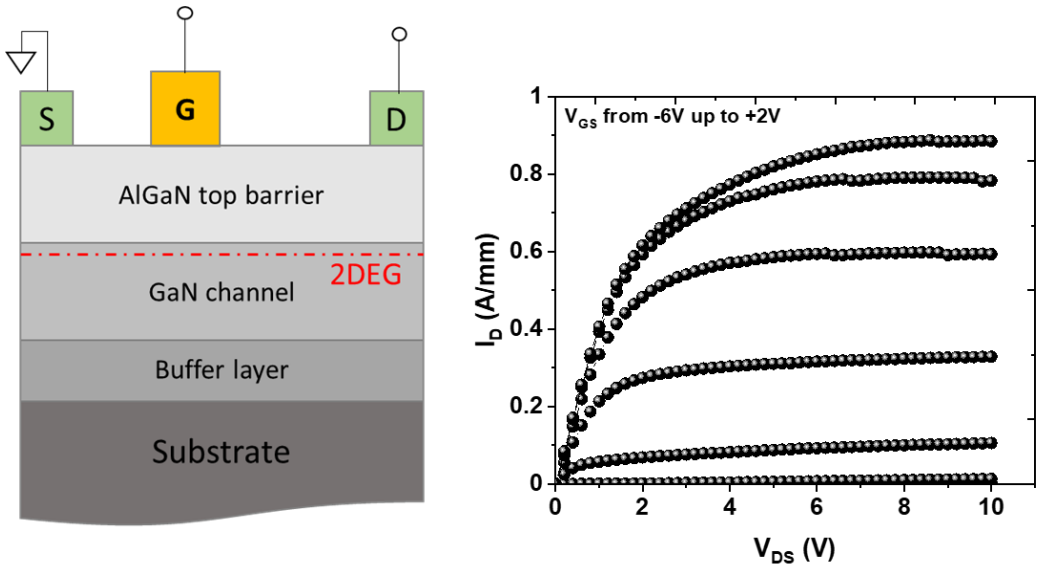


Figure.1.12. (a) Device schematic cross section of an AlGaN/GaN HEMT and (b) $I_D(V_{DS})$ output characteristics of a HEMT

Figure.1.12.a shows a schematic cross section of the AlGaN/GaN HEMT including ohmic contacts (source and drain), and a Schottky contact (gate electrode). The 2DEG is naturally present at the AlGaN/GaN interface. Therefore, the current flowing in the 2DEG channel, between source and drain contacts, is modulated by the voltage applied at the gate. **Figure.1.12.b** illustrates an example of typical

output characteristics I_{DS} (V_{DS}) showing the maximum output current, which is modulated by the bias applied to the gate. HEMT design technology and characteristics will be discussed widely in this work.

II.3. Material properties and comparison with other materials

Table.1.3 summarizes the material properties of widely used millimeter-wave semiconductors, demonstrating the benefit of GaN-based material system for high frequency and high-power applications. GaN technology is recognized as a key strategic enabling technology that has the potential to improve RF output power for millimeter-wave applications. Thanks to its excellent properties, a wider energy gap of 3.4 eV that exceed 3 times those of InP, GaAs and Si enables higher breakdown voltage and higher operating voltage. Another attractive characteristic of GaN is the high-saturated electronic velocity of 2.5×10^7 cm/s. The electron velocity is related to the current density; that is why at high voltage, GaN is able to produce high current. Therefore, the wide energy gap and the high electron velocity enable for ideal power devices since power is a function of voltage and current. Moreover, GaN-based heterostructures deliver a high electron mobility of $1\text{-}2\times10^3$ cm²/Vs, which allows low on-resistances. Therefore, at high frequencies, high PAE can be achieved. Also, GaN thermal conductivity (in the range of 1.3 - 2.1 W/cm.K) is much higher than GaAs and InP.

Table.1.3. Material properties of commonly used semiconductors

	Si	InP	GaAs	SiC	GaN	Diamond
E_{gap} (eV)	1.1	1.34	1.43	3.3	3.4	5.5
Electron mobility (cm²/V.s)	1350	12000	8500	900	2000	1900
Saturation velocity (10^7cm²/s)	1	3.3	1	2	1.5-2.5	1.9
Critical electric field (MV/cm)	0.3	0.5	0.4	3	3.3	10
Thermal conductivity (W/cm.K)	1.3	0.7	0.5	4.9	2	6-20

Figure.1.13 shows a diagram comparison between material properties of semiconductors, which highlights the superiority of GaN over its counterparts. The thermal conductivity is a key factor directly related to the power dissipation from the device. For ultra-short components operating at millimeter-wave frequencies, GaN-based heterostructures on SiC substrate are preferred in order to benefit from both properties of GaN and thermal conductivity of SiC so that heat generated by self-heating can be properly spread, allowing devices to operate at high-power densities and high frequency. In addition, GaN-based material benefit from the advantage of high temperature operation and it is inherently radiation hard. They can be used in extreme conditions where Si-based devices cannot be used [47][48]. These characteristics are very promising for space applications such as telecommunications, earth observation and science missions. Nevertheless, it is necessary to validate the reliability of GaN-transistors by studying in-depth and performing robustness tests under space operational conditions [49]. More details on GaN HEMT device reliability and available products will be discussed in this manuscript.

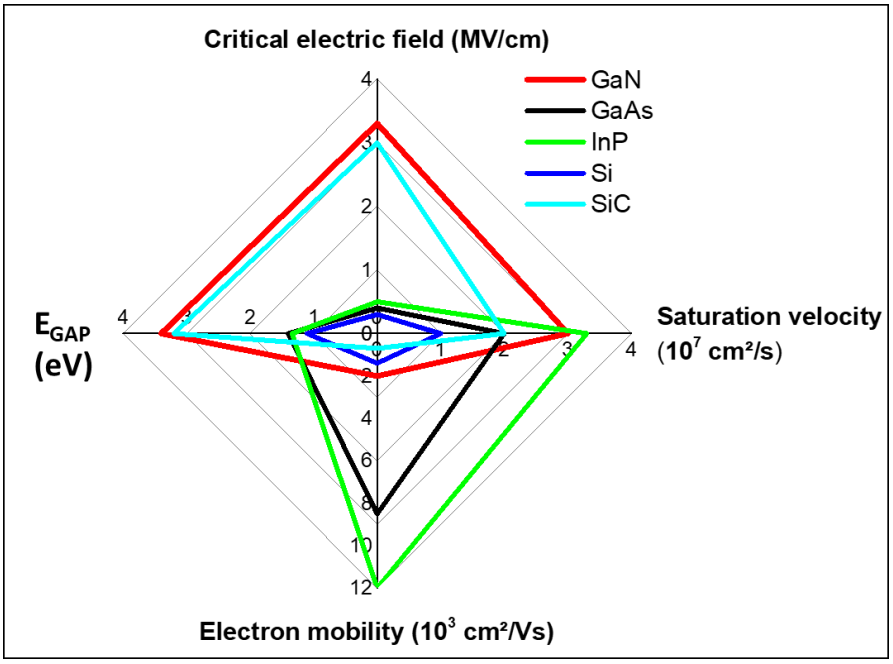


Figure.1.13. Material properties comparison of semiconductors [23]

Different figures of merits are used in order to evaluate the device performances based on different materials. They are expressed as a function of the intrinsic characteristic of the material to be analyzed. Among the indicator factors provided in the literature, we can distinguish:

Johnson's figure of merit (JFoM), widely used for RF devices, indicates the ability of the semiconductor material to operate at both high frequency and high power:

$$JFoM = \frac{V_{sat}E_C}{2\pi} \qquad (7)$$

Where E_C is the critical electric field and V_{sat} is the electron saturation velocity.

It can be noticed that JFoM can be expressed as a function of the breakdown voltage (V_{BK}) and cut-off frequency (F_T) in order to evaluate the RF performances. It is given by [50][51]:

$$JFoM = V_{BK} \times F_T \qquad (8)$$

Baliga's figure of merit (BFoM) provides an assessment in terms of voltage withstand capability and the resistive losses of the device, considering that it is given as a function of the dielectric constant of the material, the carrier mobility and critical electric field of the semiconductor:

$$BFoM = \epsilon\mu E_C^3 \qquad (9)$$

Table.1.4 summarizes the main figure of merits of different WBG semiconductors normalized with respect to Si. Diamond shows the best figure of merits with values exceeding every other semiconductor. However, in addition to the extreme high cost and small wafer size, the growth of GaN on diamond is still challenging due to the large lattice mismatch and thermal expansion mismatch [52][53].

GaN and SiC show similar figure of merits, which presents greater advantages over conventional semiconductors. Many of the present RF devices research are focused on GaN/SiC heterostructure and have already demonstrated superior performances compared to other technologies [54][55].

Table.1.4. Main figures of merits for WBG semiconductors compared with Si [56]

	Si	GaAs	4H-SiC	GaN	Diamond
JFoM	1	1.8	215.1	215.1	81000
BFoM	1	14.8	223.1	186.7	25106

GaN is well suited not only for high RF performances, but also lead to smaller and cheaper chip size. The GaN MMICs reported so far have more than 5 times higher power density with smaller size than GaAs MMICs. As illustrated in **Figure.1.14**, GaN MMICs enables the reduction by 82% as compared to GaAs pHEMT MMICs while providing more than 4 times power density. As a result, GaN MMICs can deliver higher efficiency due to the reduced on-chip combining losses both at the MMIC and module levels.

That is why, GaN MMICs will revolutionize the field of mmW SSPAs and enable new applications, that were previously not practical due to limited power of SSPAs or large size and high cost of TWTAs.

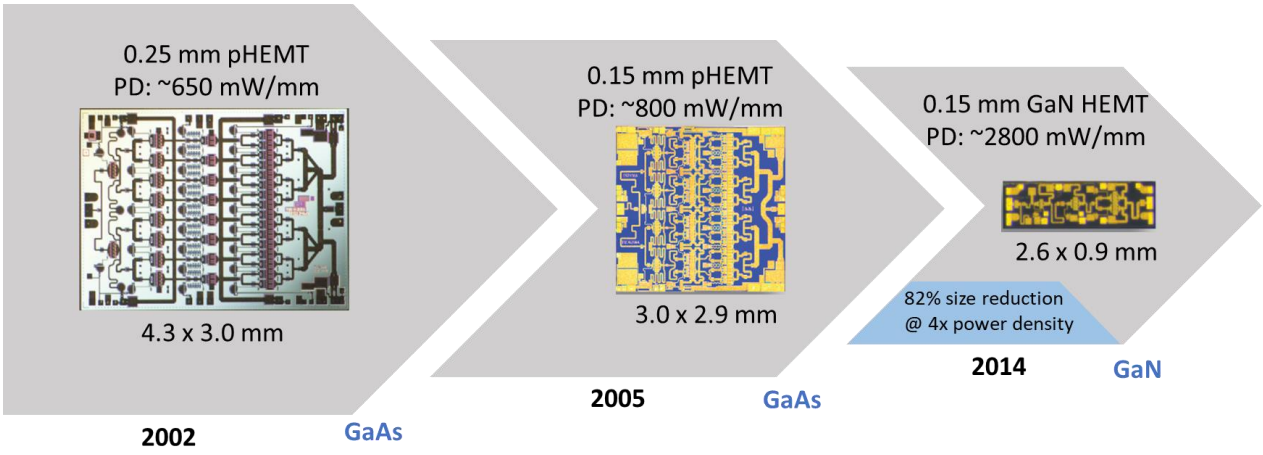


Figure.1.14. MMICs comparison with different technologies [23]

III. GaN-based device limitations

Despite the superior properties of GaN-based devices, they are still plagued by two important phenomena, especially when reducing the device dimensions: the trapping effects and the self-heating, which can directly cause current collapse and kink effect, thus reducing the device performances [57][58]. Trapping effects that occur at different location of the devices are mostly related to the crystalline imperfection induced during growth and defect-induced by device processing as shown in **Figure.1.15.a**. Surface [59][60] or buffer trapping [61] is generally electric field dependent. Several techniques are used to assess the trapping effects such as deep level transient spectroscopy measurements [62][63], temperature dependent threshold voltage analysis [64] or pulsed measurements [62][65]. As shown in **Figure.1.15.b**, pulsed I-V characteristics performed with quiescent drain voltages up to 25V at V_{GS} = +2V of AlN/GaN HEMT devices can show rather strong trapping effects as seen from the gate and drain lag due to the presence of surface and buffer traps.

The trapping/de-trapping mechanisms induce electrical parasitic effects such as current collapse and kink effect are shown in **Figure.1.16.a**. Several investigations have demonstrated that current collapse effects are related to the presence of traps and hot electron injection into the buffer layer under high electric field [58]. It was also shown that the current collapse is attributed to trapping under the gate and in the gate-drain access region using photo-transient measurements [66]. Another electrical parasitic effect due to the trapping mechanism is the kink effect that increases the drain current, resulting in a shift of pinch-off voltage towards more negative voltages. Several explanations have been suggested [67]: the impact ionization and

subsequent hole accumulation causing the change of surface or channel/substrate interface, field-dependent trapping/de-trapping in deep levels [68] and a combined effect of impact ionization and deep levels which induce a modification of surface states, buffer or channel/substrate interface deep levels by the generated holes [69]. Other studies have reported that kink effects in GaN HEMTs are related to both impact ionization coupled with the presence of slow traps in the epitaxial layers under the gate, possibly into the GaN buffer [70][71].

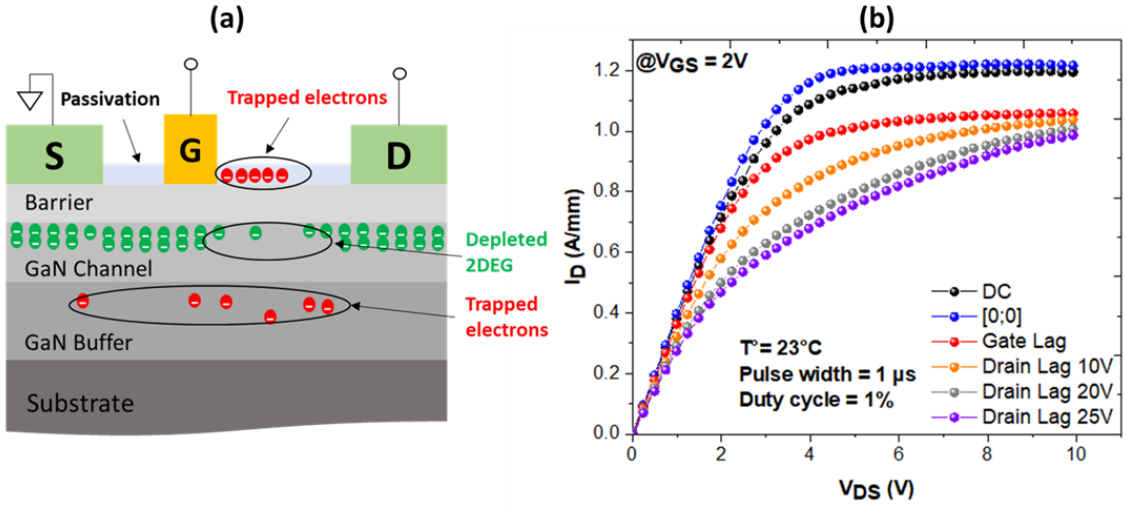


Figure.1.15. Schematic cross section of a GaN HEMT, indicating electron trapping location (a), Pulsed I-V characteristics with various quiescent bias points: Cold point: V_{DS} = 0V, V_{GS}= 0V, gate lag: V_{DS} = 0V, V_{GS}= -6V, and drain lag: V_{DS} = [10V-25V], V_{GS}= -6V (b) [23].

Figure.1.16.b [72] shows a comparison between large signal CW and pulsed mode at 40 GHz of the PAE as a function of V_{DS} of an AlN/GaN HEMT. The gap in terms of performances between CW and pulsed mode confirms the presence of traps within these devices. That is why, the optimization of material quality, and related process technology is necessary in order to minimize the trapping effect phenomena. Many efforts have been carried out to minimize the parasitic effects due to electron trapping such as:

- The use of silicon nitride passivation (Si_3N_4) to improve the gate lag [57][62][73],
- The optimization of epitaxial growth conditions in order to suppress deep level traps into the buffer layers [74],
- The use of gate field plates technology to spread the electric field in the vicinity of the gate [75] or the use of an in-situ SiN passivation reducing drastically the surface states are key parameters to improve RF performances.

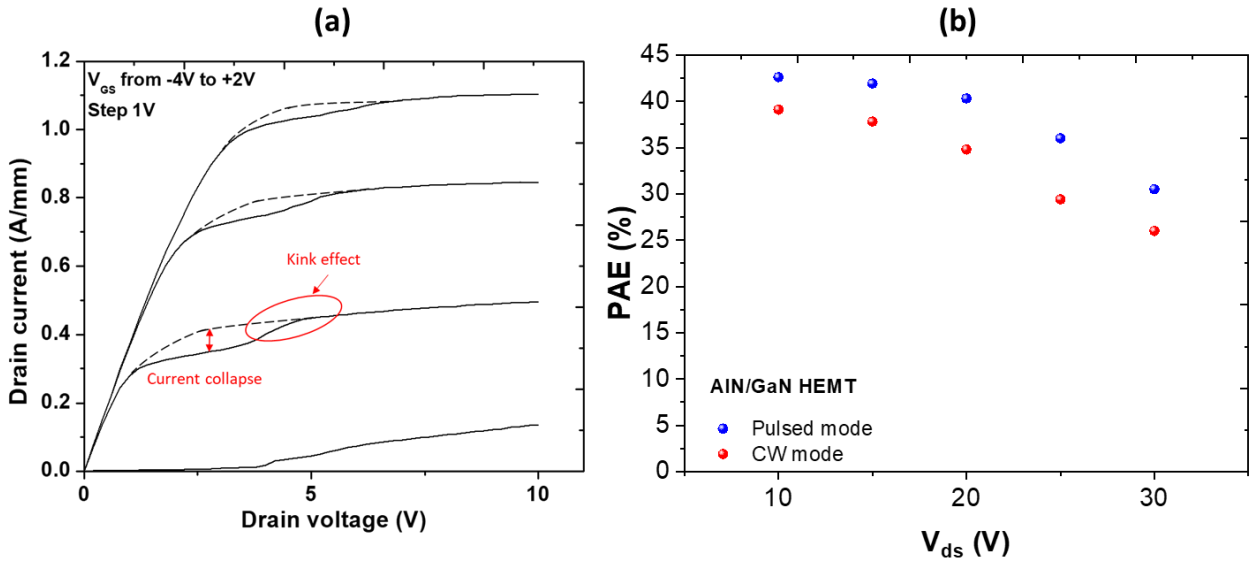


Figure.1.16. I-V characteristics showing the current collapse and kink effects due to electron trapping (a) and CW/pulsed PAE as a function of V_{DS} at 40 GHz of AlN/GaN HEMT (b).

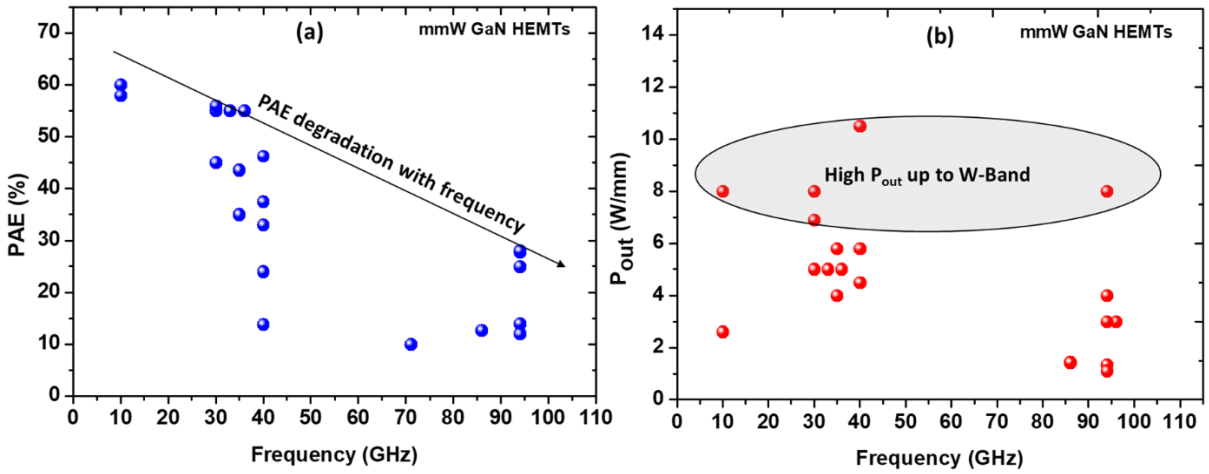


Figure.1.17. PAE (a) and associated P_{OUT} (b) of GaN HEMTs as a function of the frequency operation [23].

High frequency operation requires aggressive device scaling to increase the gain and the frequency performances of GaN HEMTs. **Figure.1.17** shows a benchmark of PAE and P_{OUT} of GaN HEMTs as a function of frequency. A remarkable PAE and P_{OUT} have been reported at Q-band. However, at higher frequency, the efficiency of GaN HEMTs is still limited mainly due to an insufficient gain. At W-band, the highest PAE reported to date is 33 % [76]. As shown in **Figure.1.17.a** the PAE decreases with frequency while P_{OUT} remains above 8 W/mm (**Figure.1.17.b**). The major current challenge for millimeter-wave GaN based devices is to maintain high PAE at high frequencies together with strong robustness. Thus, the

robustness and subsequent reliability remain under investigation as both scaled material and devices need to demonstrate high stability, reproducibility and uniformity.

IV. GaN high electron mobility transistors

IV.1. Historical development and incremental improvements

The history of solid-state electronic devices was marked by the introduction of the high electron mobility transistor (HEMT). The HEMT was first invented by Takashi Mimura at Fujitsu labs in 1980 using AlGaAs/GaAs device [77]. Moreover, a number of new structures HEMT-based on III-V material semiconductors have been developed by other researchers at Bell Labs in 1978 [78].

Later, GaN material demonstrated more advantages over other III-V semiconductors. The first demonstration of a 2DEG in AlGaN/GaN HEMT dates back to 1992 by Kahn [79]. This was followed by the first DC and RF measurements of an AlGaN/GaN HEMT by the same group in 1993 and 1994 [80][81]. In 1996 the first large signal RF power data at 2 GHz of an AlGaN/GaN HEMT reported an output power density of 1.1 W/mm by Wu et al [82]. The output power density increased over years up to 40 W/mm at 8 GHz [83] due to improved epitaxial growth and more advanced processing techniques.

However, the increasing demand for high frequency applications requires the development of new structures design in order to enhance the efficiency and the reliability. As discussed earlier, several research has demonstrated outstanding GaN HEMT performances in the millimeter-wave range [84][76][55][85]. Currently, reaching high PAE at high frequency of operation is the main challenge and not demonstrated so far due to the lack of power gain, enhanced trapping effects and reduced electron confinement when downscaling the device size or the self-heating.

Based on WBG material, GaN HEMTs are getting a significant focus of research activities in the recent years and are one of the most promising devices for high frequency applications. One of the approaches is the use of an ultrathin Al-rich barrier layer based heterostructure, which is promising for millimeter-wave range, because of the possibility to highly scale the epitaxial structure, while still benefiting from high polarization. Several investigations have been demonstrated that a thin InAlN and AlN barrier layers are very attractive for high frequency millimeter-wave devices. In 2006, Medjdoub *et al* at IEMN were first to demonstrate the capability of an InAlN/GaN heterostructure to deliver higher power density at high frequency and to be more stable than AlGaN/GaN structure [86][87]. Some years later, the same group has reported the high potential of the ultrathin AlN/GaN structure for high power millimeter-wave applications [88][89][90].

IV.2. Figure of merits of GaN-based HEMTs

In this thesis, the main focus of the research is to develop a high performances GaN HEMT device for future high frequency power applications. In order to better understand the purpose of this thesis, it is useful to review the most important aspects of GaN HEMTs operating in the millimeter-wave range. The targeted performances required for high frequency devices include the combination of high power/high efficiency and device reliability.

IV.2.1. High performances: PAE/output power density

In this frame, GaN HEMT devices should be capable of delivering high large signal gain, high efficiencies and high output power density at the targeted frequency range. Equations for assessing the RF device performances at a particular frequency are given by:

$$PAE = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}} = \frac{P_{RFOUT}}{P_{DC}} \times \left(1 - \frac{1}{G_p}\right) \qquad (10)$$

$$\eta = \frac{P_{RFOUT}}{P_{DC}} \qquad (11)$$

$$P_{OUT} = \frac{\left(V_{DSQ} - V_{knee}\right) \times I_{DSS}}{4} \qquad (12)$$

In equation (10), PAE is the power added efficiency, P_{RFOUT} is the output power density, P_{DC} is the dissipated DC power density and G_p the power gain at the frequency of interest. The PAE is the best factor in order to access the device heat management. The way in which a transistor is operated determines the polarization class. As shown in **Figure.1.18**, there are many different types of polarization class (A, AB, B…) but the main one used in this work is deep class AB. In class AB, the quiescent drain current is set to the optimum value corresponding to a trade-off between the linearity and efficiency. Furthermore, in order to achieve the highest possible PAE, a high-power gain and high drain efficiency are necessary.

η is the drain efficiency in equation (11) which is used when the power gain G_p is high enough to neglect the input power compared to the output power. To achieve the highest drain efficiency, the ratio between breakdown voltage and knee voltage should be high.

In equation (12), V_{DSQ} is quiescent drain-source voltage bias, V_{knee} is knee voltage of the transistor's I-V curve, and I_{DSS} is the saturated current density. High breakdown voltage allows high quiescent drain-source voltage operation and thus increasing the output power density.

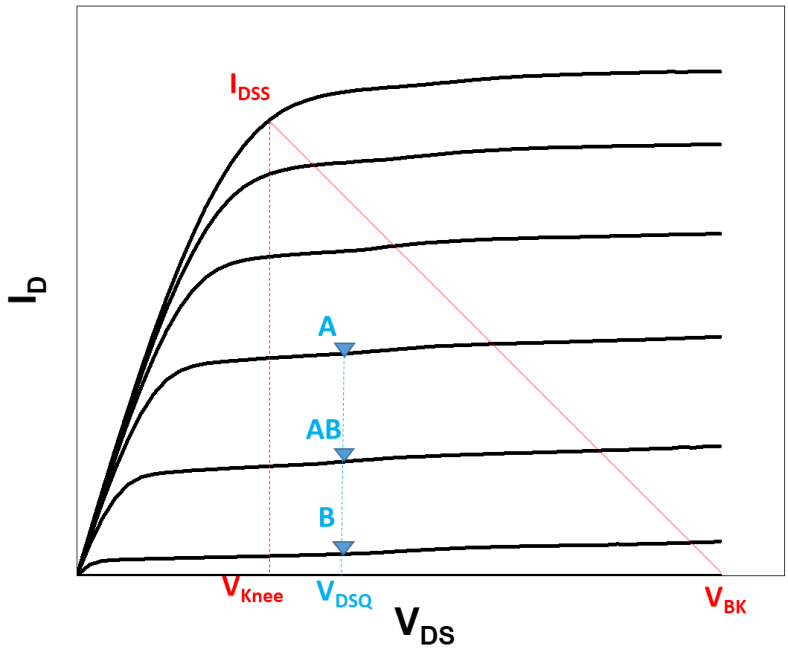


Figure.1.18. I-V curve of GaN HEMT showing three different polarization types

The main limiting factor of the PAE and the output power density is the combination of the DC to RF dispersion and the thermal effects. The dispersion (so-called current collapse) is due to the traps and leads to a drop of P_{OUT}, the PAE as well as the drain efficiency. Moreover, self-heating within the HEMT appears at high drain voltage and have a significant impact on the PAE mainly by reducing the electron mobility.

A successful control of the dispersion while simultaneously achieving reasonable large signal gain at high frequency is an important accomplishment of this work.

IV.2.2. GaN HEMTs Reliability

The reliability is crucial before marketing can be foreseen. It is defined as the ability of a component to perform a required function or mission successfully without failure or degradation over a given duration. This is particularly true for a system where any maintenance is impossible during operation such as satellite and military systems. The reliability of the final product is crucial and depends on device design and fabrication process.

A number of groups have demonstrated a unique combination of higher power and wider bandwidth available with GaN devices as compared to other technologies all the way to 100 GHz. However, for short GaN devices with gate lengths below 150 nm, the main limitation is the device reliability due to a significant

electric field peak and subsequent high junction temperature under high drain bias. That is why, very few millimeter-wave GaN device reliability reports can be found in the literature both for short and long-term assessment.

- ***Short-term reliability:***

Short-term reliability gives the possibility to assess the device degradation or failure and provide short time substantial feedback for material quality and adjustment before starting long-term reliability tests for the final application of the devices. It consists generally of on-wafer DC and RF large signal robustness assessment at room and/or high temperature for few hours by increasing the base-plate temperature. The DC robustness assessment is generally evaluated by means of off-state, semi-on state and on-state step stress tests where the drain voltage is increased up to hard device breakdown while monitoring the gate and drain current for several hours. Similarly, short-term on-wafer RF step stress consists of monitoring the device during several hours under large signal conditions at various temperature. However, short-term reliability does not provide any information on the degradation kinetics, activation energy, and mean time to failure. Therefore, long-term reliability is required in order to validate the device reliability. In this thesis, we performed both DC and RF short-term robustness on AlN/GaN HEMTs structures. The results can be found in chapter 3.

- ***Long-term reliability***

Long-term reliability is the last step before technology qualification. Some specific semiconductor failure such as kinetics degradation of activation energies cannot be provided by short-term reliability assessment. Long-term reliability of semiconductor devices is described by the known “bathtub” curve, which is divided into three regions as shown in **Figure.1.19**. The region 1 is the early infant mortality period which defines the time where devices show failure signs especially during short-time reliability tests or burn-in step. In region 2, the devices enter into a stable stage “random failure period” with a constant failure rate. For reliable devices, this period should be as long as possible with extremely small constant failure. Finally, the last region is the period where the failure rate will increase sharply due to the “wear-out” and the device comes to the end of its lifetime.

In order to evaluate the device reliability, data should be analyzed by lifetime distribution of GaN HEMTs during the stress and gives an insight into characteristics of failure times. Several accelerate lifetime reliability tests under high temperature are used to describe the expected mean time to failure (MTTF) such as:

- High temperature reverse bias (HTRB) which consists of monitoring the gate current while a high negative gate bias close to the breakdown voltage is applied at high temperature allows to estimate the gate reliability under harsh conditions.
- High temperature operating life test (HTOL) which defines the safe operating area at high temperature in DC and RF conditions by biasing the devices. This test permits to study the thermal and electrical stress effects and assess the wear-out mechanism. In addition, the devices with high early failure and infant mortality rate can be assessed by a short duration HTOL test known as burn-in.

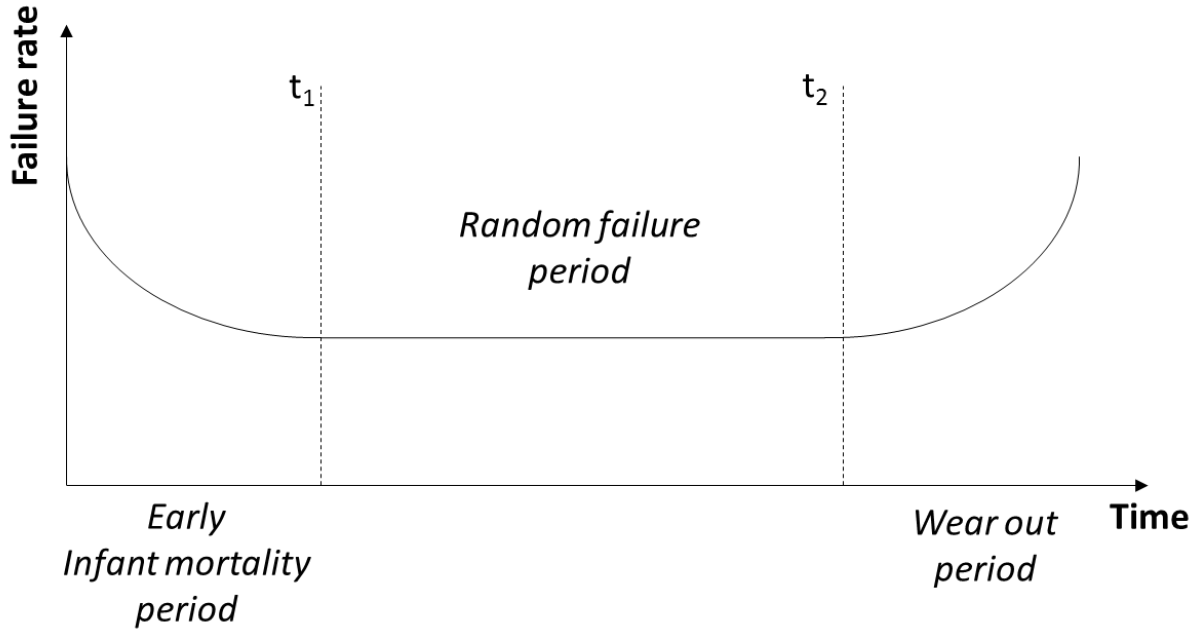


Figure.1.19. Typical bathtub behavior for long-term reliability.

Although, impressive results were reported for GaN HEMT devices in millimeter-wave range, the reliability demonstration is still limited by a number of mechanisms degradation especially the thermal dissipation, which leads to reduced MTTF. It is worth noting that no GaN high power amplifiers operating up to the W-band have been reported with high PAE > 30%, high linearity and high reliability simultaneously. This is essentially due to the poor aspect ratio of the standard AlGaN/GaN HEMT when using short gate lengths (< 150 nm), preventing high RF power gain and resulting in high device leakage current, high trapping effects and a reduced breakdown voltage. Therefore, it would be of high interest to pave the way to other structure designs such as AlN/GaN HEMT in order to satisfy the combination of high power and high reliability.

IV.3. GaN HEMT epitaxial structures

IV.3.1. Epitaxial structure and growth techniques

Figure.1.20 shows a cross section of GaN-based epitaxial structure which consists of multiple epilayers grown onto each other. The heterostructure based on III-nitride materials is composed of an in-situ SiN or GaN cap layer, a wide bandgap barrier layer (AlN, InAlN, InAlGaN or AlGaN), a GaN channel and GaN-based buffer layers grown on top of a substrate.

The growth techniques of GaN-based heterostructures have an impact on the HEMT device performances. The growth of good quality and uniformity of epitaxial layers highly depends on the growth parameters such as temperature, pressure and gas flow rate [91][92]. The most popular and commonly used growth techniques are Molecular Beam Epitaxy (MBE) and Metal Organic Chemical Vapor Deposition (MOCVD).

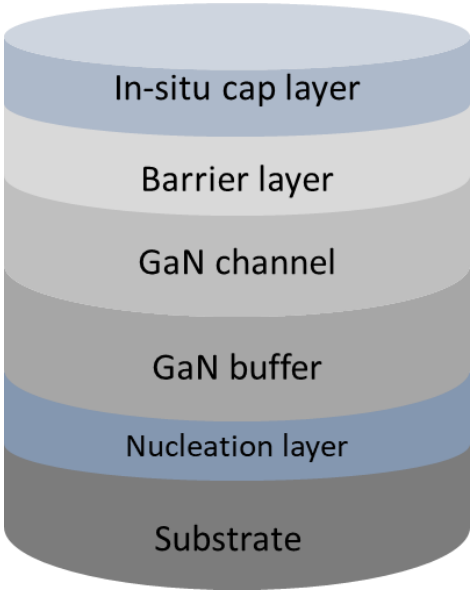


Figure.1.20. Cross section of GaN-based epitaxial structure

MBE is a growth technique based on reactions between thermal-energy molecular, atomic or ionized beams of the constituent elements on a heated substrate [93]. This method allows a precise definition of interfaces and low dislocation concentration and strain. The main benefits of this technique consist in a slow growth rate and a low growth temperature in the range between 600°C and 900°C. These advantages make it easy to control the layer thickness grown and the doping concentration, which enable high material quality with better transport properties and low RF losses [94][93][95]. However, the slow deposition rate of MBE system makes it a more expensive technique as compared to MOCVD technique.

MOCVD technique involves a dynamic flow in which gaseous reactants pass over a heated substrate on which the epitaxial growth of semiconductors takes place [96]. This technique is the most commonly used due to its low cost compared to MBE growth system. Typical growth rate is about few micrometers per hour, which is twice faster than MBE growth. In addition, MOCVD growth is performed at much higher temperature (>1000°C) compared to MBE growth [91]. MOCVD is therefore the main method used in GaN industry it combines low cost and high-quality material [92]. Since all the materials in this work have been grown by MOCVD method, this will be the main growth technique considered in this thesis. The main material supplier and collaborator is SOITEC (Ex-EpiGaN). For further structure studies and comparison, materials have also been supplied by SweGaN, Veeco, and Enkris using MOCVD system.

IV.3.2. Configuration and specific material systems of RF HEMT structures

Although the optimization of the epitaxial growth technique and conditions are necessary in order to achieve high RF performances, the epi-structure optimization is crucial as it has a huge impact on device performances and robustness. In this section, the purpose of each layer from the epi-structure shown previously in **Figure.1.20** will be explained and alternative material selections for millimeter-wave RF devices will be outlined. Currently more "exotic" epi-structure are frequently reported which will be discussed extensively later in this work.

IV.3.2.1. Substrate choice

The substrate is the base of growing process which determines crystal orientation, polarity, polytype, elastic constrain and concentration of GaN dislocations. Therefore, it is mandatory to choose a substrate that should ensures the highest quality of epitaxial layers. The choice of substrate depends on the available size, cost, thermal conductivity, coefficient of thermal expansion (CTE), lattice mismatch and targeted applications. Since bulk GaN substrates are still unavailable on large wafer diameter, GaN HEMTs are typically grown on SiC, Si and Sapphire. Although, most recently GaN on diamond is being carefully investigated for improved performance metrics due to its high thermal conductivity but still limited to use due to the small size and high cost [97][98]. **Figure.1.21** shows a comparison of the above-mentioned figure of merits between different substrates on which GaN can be grown.

It can be noticed that there are several techniques used to improve quality of growing crystal such as the insertion of an AlN nucleation layer, which is essential in order to accommodate the lattice mismatch between GaN and the substrate [99][100].

Sapphire is semi-insulating in nature and withstand high growth temperatures. However, several causes limit the use of Sapphire as an attractive substrate for power applications. Indeed, the low thermal conductivity coefficient of Sapphire leads to a rather poor thermal dissipation. A CTE and lattice constant showing a significant mismatch with GaN, which results in high concentration of dislocations and cracking of thick films thus decreasing the mobility of charge carrier [101][102].

Silicon is a relatively economical substrate option due to its low cost. It presents many advantages over Sapphire such as compatible processing with advanced CMOS, an acceptable thermal conductivity and availability of large wafer diameter. That is why several industries have chosen Si widely as a reference substrate [103][104]. Nevertheless, it also suffers from a large lattice mismatch with GaN as reflected by dislocations due to substantial elastic strains. For millimeter-wave RF devices, thermal dissipation effects remain a major factor in limiting the device performance and related reliability. A low thermal conductivity of Si leads to a higher thermal resistance, which has a large impact on RF device performances especially under high power dissipation conditions [105].

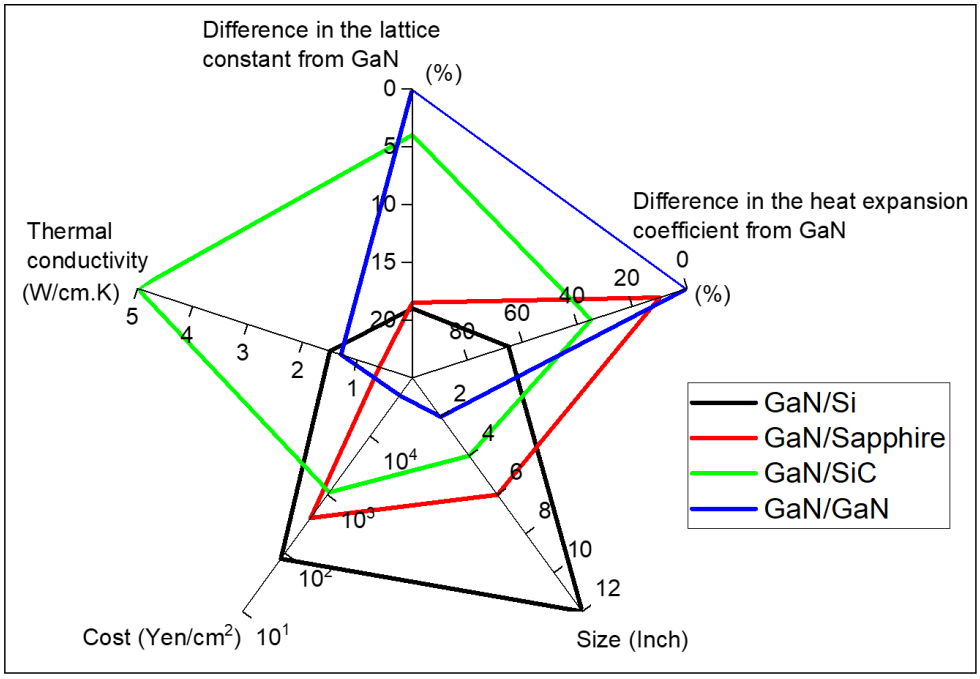


Figure.1.21. Comparison between different substrate used to grown GaN

Recent reported data confirm that SiC is the most attractive substrate for GaN millimeter-wave power devices. Because of its excellent physical properties especially low lattice mismatch with GaN and high thermal conductivity enabling superior power operations that are not reachable by any other materials [76][84][55]. Therefore, SiC is the most appropriate material for high power devices where thermal

conductivity is a critical parameter. However, the main limitation of SiC substrates lies in its high cost and availability of the large size wafers. **Figure.1.22** shows TEM image of GaN grown on SiC showing a rather low dislocation density. Within the framework of this work, most of the epitaxial structures studied are based on 4-inch SiC substrate.

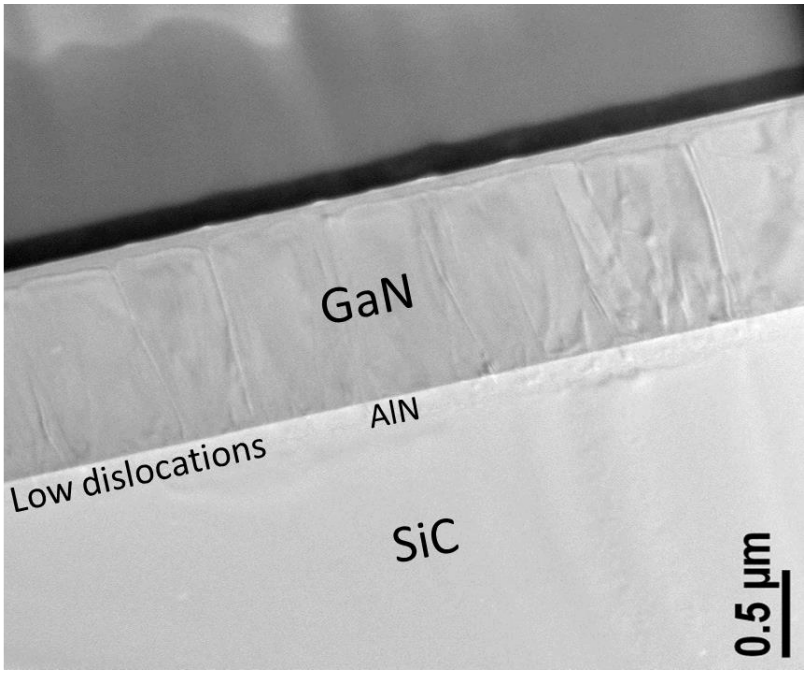


Figure.1.22. TEM image of a GaN layer grown on SiC

IV.3.2.2. Buffer design: C-doped GaN vs Fe-doped GaN vs AlGaN back-barrier

The buffer layer design can have a large impact on the device performances. The GaN buffer needs to be grown to a thickness of more than 1 µm in order to decrease the dislocations reaching the channel layer while allowing a smooth surface for the barrier layer. The buffer layer is also used to confine the electrons into the 2DEG under high electric field limiting the short channel effects. Latest literature has demonstrated that for devices with poor electron confinement, the robustness is expected to decrease and high operating frequencies cannot be achieved. Therefore, high quality of the buffer layer can be obtained by using a back barrier or incorporating acceptor type dopants such as carbon (C) or iron (Fe) in order to increase the resistivity. However, all of these alternatives are associated with increased deep traps into the buffer region. Minimizing trapping effects while maintaining good confinement is thus the main challenge to ensure high device performances. **Figure**.**1.23** presents two structures with different buffer layer: AlGaN back barrier and C-doped buffer layer showing the role of each buffer.

Unintentionally doped GaN is usually n-type due to the incorporation of impurities during growth. Therefore, compensation doping is required in order to increase the resistivity in the GaN buffer enabling good electron confinement and low buffer leakage current. However, compensating dopants introduce high defect density reflected by trapping effects and reduces the crystal quality thus decreasing the electron mobility. That is why low doping atoms in the vicinity of the 2DEG is required in order to increase the electron density (N_s) and the electron mobility (μ) in the 2DEG. The two most commonly used acceptors are Fe and C.

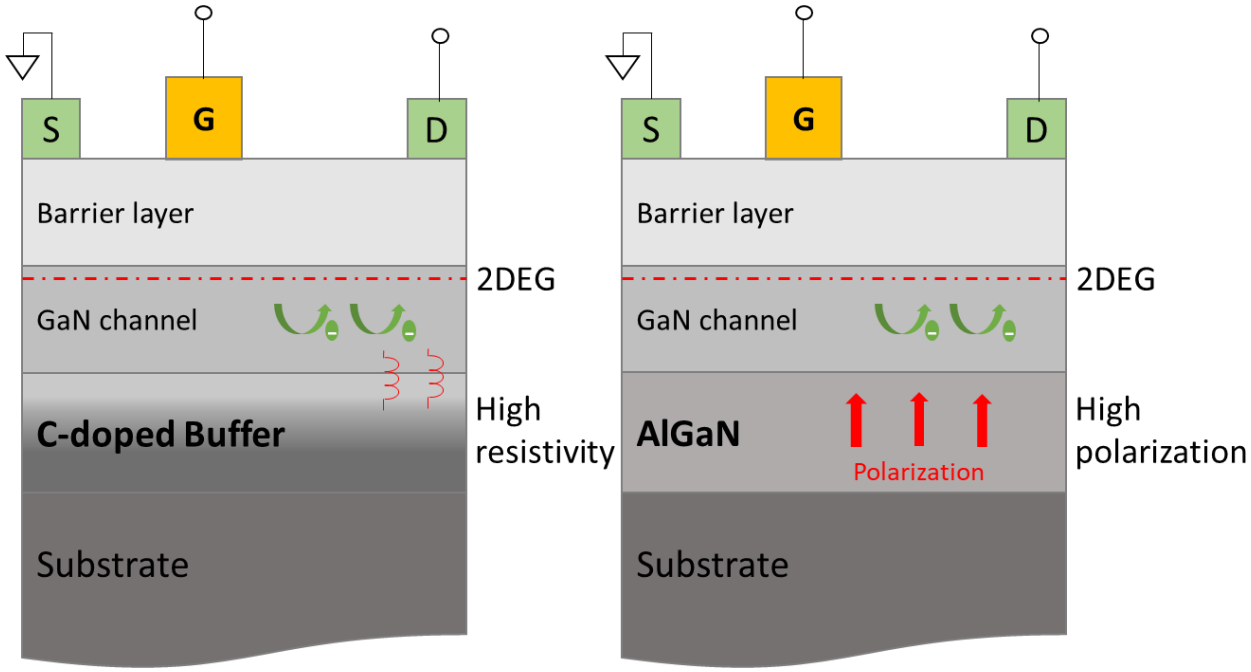


Figure.1.23. Cross section of a GaN HEMT structure with two type of buffers: C-doped GaN buffer (left) and AlGaN back barrier (right)

- ***Fe-doped GaN buffer***

Fe-doped buffers are used for GaN HEMTs due to its high resistivity and high breakdown voltage, which allows high associated output power density compared to unintentionally doped buffers [106][107]. However, the main disadvantage of using Fe-doping is the growth related memory effects where Fe dopant in the GaN epilayers tended to segregate to the surface making sharp transitions from high to low Fe-concentrations difficult to achieve [108][109]. The traps generated by Fe dopants are located below the GaN conduction band at E_C = 0.6 eV and has been identified as responsible of drain current collapse and related on-resistance increase [110].

- ***C-doped GaN buffer***

Highly C-doped GaN buffer offers a higher resistivity and much sharper profile as compared to Fe-doped GaN. For short devices delivering high performances at high drain bias, C-doped buffers are required in order to enhance the breakdown voltage and the device robustness [84][111]. However, high C-doped buffer increases the dislocation density and leads to an extensive dispersion when C-dopants are incorporated in the vicinity of the channel but nevertheless provides an excellent isolation and power performances [112][113]. Under high C-concentration, GaN has been shown to become p-type and hence, isolated from the channel by a pn-junction. Therefore, electrons can be trapped in the p-type region under high drain bias forming a back-biased pn-junction resulting in strong current collapse [114][115]. A solution to avoid the pn-junction formation is to tailor the doping profile with high precision. One of the advantages of C-doping is that it does not suffer from the same memory effects as for Fe-doping. That is why sharp profile from high to low C-concentration are readily achievable allowing a stepped C-profile with low C-concentration in vicinity of the 2DEG and a high concentration ($\sim 10^{19}$ cm^{-3}) deep in the buffer. This gives a good trade-off between short channel effect, dispersion and leakage. In this work C-doped buffer structures grown by EpiGaN have been investigated for millimeter-wave applications. Different C-doped buffer design and configuration have been studied and will be discussed widely in the next chapters.

- ***AlGaN back-barrier***

A possible alternative to compensated GaN buffers is the use of AlGaN back-barrier, which is a high energy barrier that prevents the space charge region from extending down into the heterostructure as shown previously in **Figure.1.23**. The AlGaN back-barrier double heterojunction devices (DHFET) demonstrate high electron confinement making it attractive for high frequency operation. However, the presence of an AlGaN back-barrier has a negative impact on thermal dissipation. Indeed, the thermal conductivity of (Al)GaN decreases while increasing the Al content. This impacts the gate leakage current and thus degrades the device performances. Moreover, AlGaN back-barrier transistors suffer also from trapping effects, since AlGaN alloy is intrinsically more difficult to grow with high crystal quality. Therefore, the design of the buffer layers should be carefully selected to perform not only high performances but also high robustness with GaN devices in the millimeter-wave range.

A comparative study has demonstrated that AlGaN back-barrier results in poor device robustness under high electric field due to the self-heating enhancement. Unlike C-doped based structures that delivers higher performances together with much better device robustness. In **Figure.1.24** is represented a comparison of RF performances at 40 GHz between two structures using two types of buffers: AlGaN back barrier and Carbon doped GaN buffers. Due to the poor thermal dissipation of the AlGaN buffer, we can

clearly observe a poor robustness of AlGaN back barrier devices as seen through the huge gate leakage current monitoring subsequent to load-pull measurements. This leads to a significant gap in term of PAE between both structures.

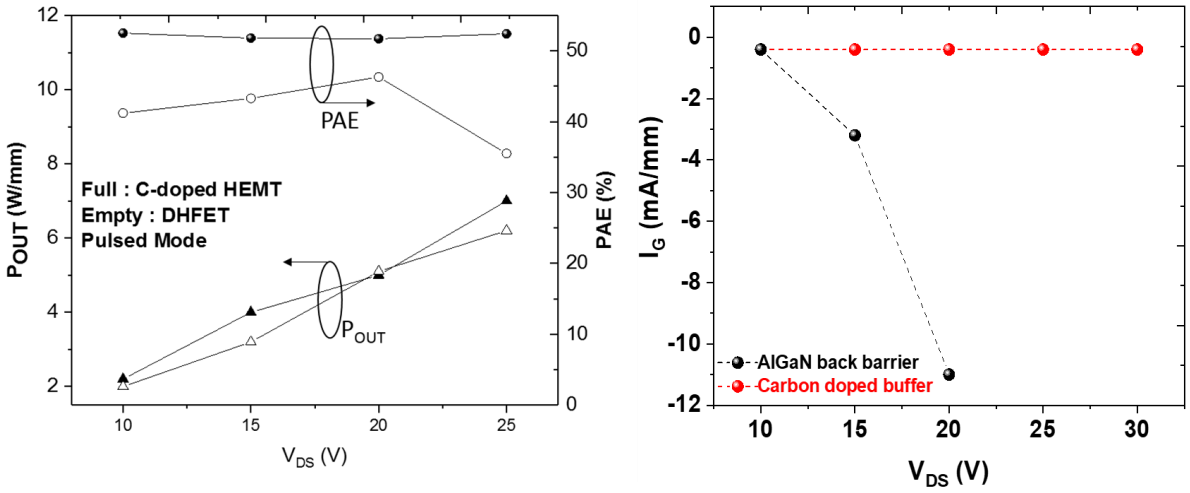


Figure.1.24. Comparison between DHFET and C-doped GaN HEMT in term of PAE and gate leakage after load-pull measurements at 40 GHz in Pulsed mode [84][116].

IV.3.2.3. Channel thickness

The GaN channel is generally undoped in order to allow high electron transport quality. The choice of GaN channel thickness is critical because it is directly related to the device robustness. A thick GaN channel leads to high electron density and low trapping effects by pushing away from the 2DEG eventual traps from the buffer layer. However, for device scaling using short gate lengths, a thinner GaN channel is required in order to reduce short channel effects such as DIBL, which can affect the device robustness and performances. Therefore, the choice the GaN channel is based on the trade-off between electron confinement and trapping effects.

IV.3.2.4. Barrier material options: AlN, InAlGaN, AlGaN

The choice of the barrier layer material depends on the thickness and Al-content which are key parameters impacting the mechanical strain and piezoelectric polarization. Various materials based on III-Nitride semiconductors including ternary and quaternary alloys are used as a barrier layer. A high 2DEG density is induced at the interface of the barrier layer and the GaN channel through spontaneous and piezoelectric polarization effects without the need for intentional doping. **Figure.1.25** shows the electrical properties of GaN HEMT structures based on different barrier layers grown on SiC substrate. The high sheet charge density of 1.2×10^{13} cm^{-2} can be obtained with an AlGaN barrier layer and up to 2×10^{13} cm^{-2}

for an AlN barrier layer. However, the 2DEG electron mobility decreases with the increase of 2DEG density from 2200 $cm^2/V.s$ for AlGaN barrier to about 1000 $cm^2/V.s$ for AlN barrier layer.

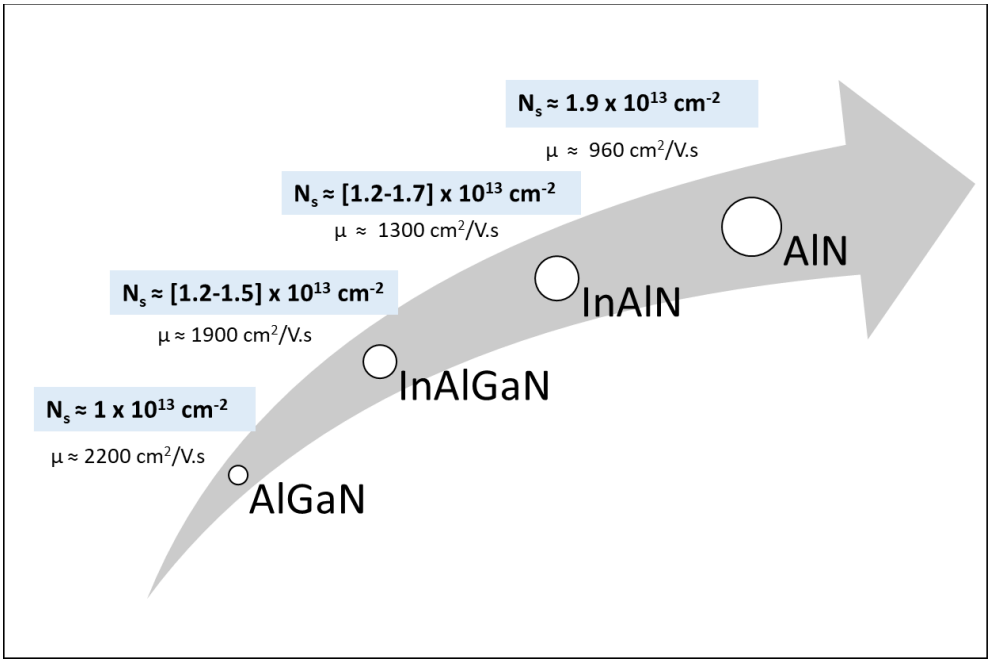


Figure.1.25. 2DEG electrical properties for AlGaN, InAlGaN, InAlN and AlN barrier layers

- ***AlGaN/GaN structures for microwave range and their limits in millimeter-wave range***

AlGaN/GaN based HEMTs is the most mature technology, which has demonstrated outstanding power performances in the microwave range. State of the art power level have been reported with about 40 W/mm, 30 W/mm and 10.5 W/mm at 4 GHz, 8 GHz and 40 GHz, respectively [83][75][117]. The output power density decreases as expected with frequency of operation due to the reduced breakdown voltage resulting from the device downscaling. High Al-content in AlGaN barrier layer leads to an increase of the spontaneous and piezoelectric polarizations and therefore increases the 2DEG density provided that a sufficiently high barrier thickness is maintained. However, a pseudomorphic growth of AlGaN on GaN is difficult to achieve with high Al-content due to the different physical properties. Indeed, the AlGaN/GaN heterostructure shows rather high dislocations due to the tensile strain when using thicker barrier layer close to the critical thickness [42]. Therefore, it is necessary to reduce the AlGaN barrier thickness in order to decrease the dislocation density. A compromise must be found between the barrier thickness and the Al-content. The Al-composition of a standard AlGaN barrier layer is between 20% and 30% while the barrier thickness varies between 20 and 30 nm. High Al-content and large barrier thickness in AlGaN/GaN

structures induces higher dislocation density. In this thesis, we demonstrated that high Al-content in the AlGaN barrier leads to a strong leakage current. On the other hand, low Al-content with thinner barrier thickness decreases the 2DEG density. Many studies on AlGaN/GaN HEMTs have reported a sheet carrier density between 5×10^{12} and 1×10^{13} with a 2DEG electron mobility up to 2000 cm²/V.s. These values are highly dependent on AlGaN barrier layer configuration.

Hall-effect measurements showing the 2DEG density and mobility as a function of the barrier thickness of AlGaN/GaN structures appear in **Figure.1.26**. By increasing the barrier thickness from 10 nm to 40 nm, the 2DEG density increases from 6×10^{12} cm^{-2} to 1.5×10^{13} cm^{-2}, which is also accompanied by a significant reduction in the electron mobility.

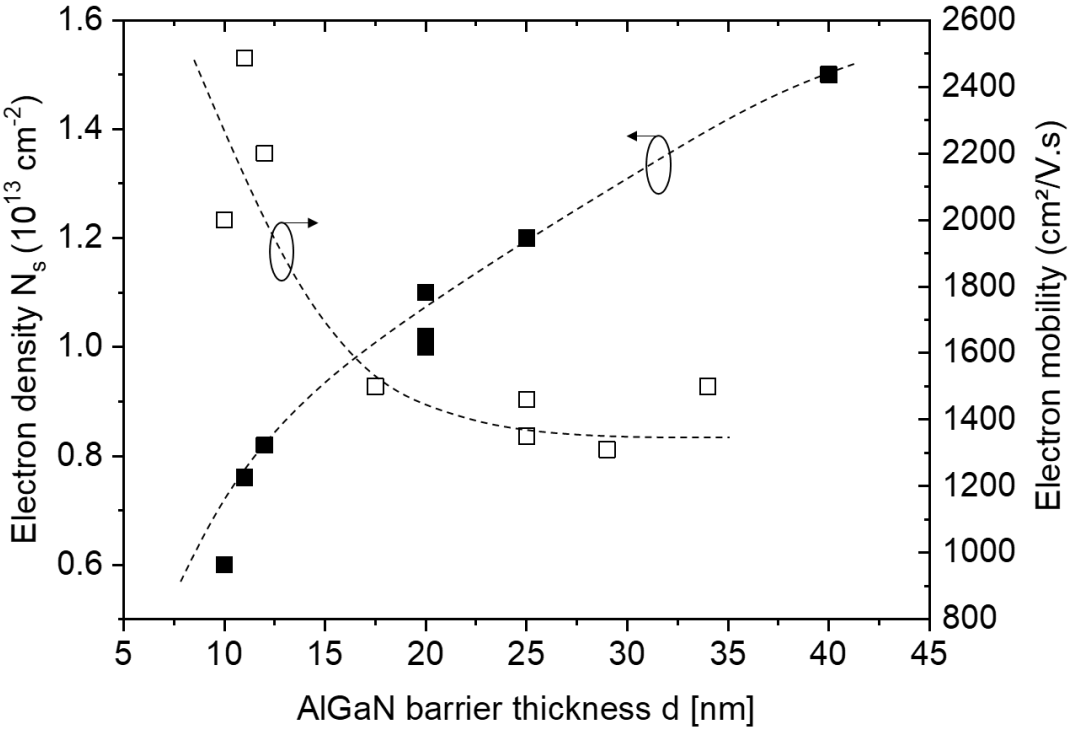


Figure.1.26. 2DEG density and associated electron mobility as a function of AlGaN barrier thickness.

Recent progress in HEMT technology paves the way to extending to higher frequencies as system designers need more bandwidth for many emerging applications. To date, it is difficult to improve the performances of AlGaN/GaN HEMTs as the scaling of this barrier is approaching the theoretical limits. Since device scaling for high frequency operations requires a reduced gate length, the barrier thickness scaling is necessary in order to maintain a high aspect ratio L_g/a to avoid short channel effects. Therefore, further improvements in structure epi-design especially the barrier layer choice are necessary to meet the millimeter-wave requirements.

- ***InAlN, InAlGaN/GaN structures with high 2DEG density***

A ternary and quaternary (InAlN and InAlGaN) barriers layers are attractively replaced a commonly AlGaN barrier layer to improve performances of GaN-based HEMTs [86][118]. InAlN and InAlGaN offer two main advantages over AlGaN/GaN structure. First, they can be grown lattice matched to GaN when the concentration of In is 17% [119]. The converse piezoelectric effect can be expected less critical due to the absence of lattice strain which decreases dislocation density thus allowing enhanced device performances and reliability. Second, the spontaneous polarization at InAlN, InAlGaN/GaN interfaces induces a significantly higher 2DEG density up to more than 2×10^{13} cm^{-2} for InAlN/GaN structure combined with high electron mobility up to 2200 $cm^2/V.s$ and low sheet resistance (R_{sh}) varying between 180 and 300 **Ω/□** [120][121]. As expected, this combination reduces the access resistances while avoiding to reduce too much the gate-to source distance leading to excellent device performances. Moreover, for device scaling using shorter gate lengths, sub-10 nm InAlN and InAlGaN barrier layers can be used while maintaining high carrier density N_S. This allows high aspect ratio L_G/a (gate length/gate-to-channel distance) and high frequency performances and makes such devices design attractive for millimeter-wave applications. **Figure.1.27.c** shows the electron transport properties of 2DEG in a sub-10 nm InAlGaN/AlN/GaN HEMT. A high 2DEG mobility of 1800 $cm^2/V.s$ at room temperature and 7340 $cm^2/V.s$ at 4 K were obtained combined with high carrier sheet density of 1.9×10^{13} cm^{-2}. The very high electron mobility in this structure over 4-400K range is attributed to the high crystal quality and reduced interface roughness as shown in **Figure.1.27.b** [121].

The optimized heterostructures with gate length scaling and efficient process technique demonstrated improved DC and RF performances. InAlN-based GaN HEMT technology using 30 nm gate length reported a maximum drain current I_{dmax} of 1.9 A/mm and an extrinsic g_m of 653 mS/mm combined with high F_t/F_{max} of 400/33 GHz [122]. Moreover, InAlGaN/GaN HEMTs achieved an F_t/F_{max} of 317/49 GHz with a peak g_m of 680 mS/mm using a 26 nm gate length [120]. Researchers reported that InAlGaN/GaN structures are a promising candidate for RF devices delivering low gate leakage current I_g and physical degradation of the gate-edge region while enhancing the breakdown voltage. At 96 GHz, a high output power density of 3 W/mm at V_{DS}= 20V has been reported using 80 nm gate length InAlGaN/GaN HEMT technology [123].

Although the InAlN and InAlGaN/GaN-based HEMT devices are promising candidates for millimeter-wave applications, they are still not mature and require more investigations in terms of degradation mechanisms and parasitic effects having a huge impact on the device reliability.

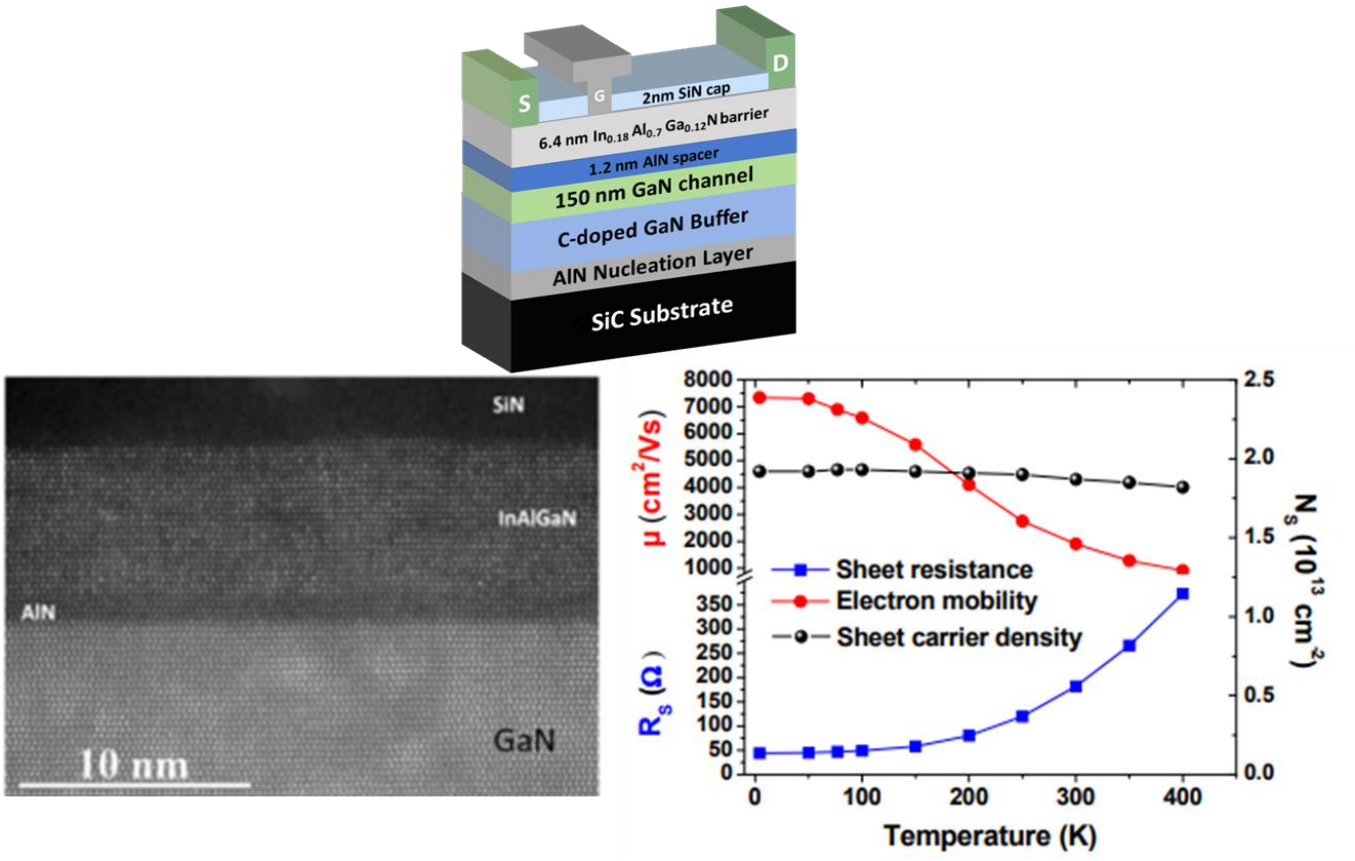


Figure.1.27. a) cross section of InAlGaN/AlN/GaN HEMT b) TEM image of InAlGaN/AlN/GaN grown on SiC substrate c) sheet resistance, hall mobility and sheet carrier density of the InAlGaN/AlN/GaN heterostructure as a function of temperature [121]

- ***Ultrathin AlN/GaN based HEMTs for millimeter-wave applications***

Ultrathin AlN/GaN material system has become an alternative candidate for high power millimeter-wave applications because of the possibility to highly scale the barrier layer thus benefiting from a high polarization. The 2DEG density can reach more than 2×10^{13} cm^{-2} with ultrathin AlN/GaN structure (sub-5 nm) combined with an electron mobility of around 1000 $cm^2/V.s$. In addition, ultrathin AlN/GaN structure enables mitigating the short channel effects with highly scaled devices due to the favorable aspect ratio L_G/a. These superior properties make this material system a potential solution to satisfy GaN HEMTs requirements for millimeter-wave applications. However, high quality AlN/GaN growth is difficult to achieve especially when using thicker AlN barrier due to large lattice mismatch between AlN and GaN. Indeed, the strain increases considerably with the AlN barrier thickness increasing the defect density into the barrier layer thus reducing the device robustness. Improvement in AlN/GaN structure resulted in high performances in millimeter-wave range. Nevertheless, pure AlN barrier layer leads to higher contact

resistance than InAlGaN barrier layer. Several approaches have been developed such as regrown ohmic contact by MBE technique in order to reduce the parasitic access resistance and then enhance the device performances [124][125]. Another issue from the AlN/GaN structure is the surface sensitivity if the epilayers is not protected during the process. Surface passivation is therefore required in order to prevent the trapping effects and passivate the surface charges thus reducing DC and RF dispersion [126][127]. **Table.1.5** summarize DC and RF AlN/GaN based devices performances which have been reported in the millimeter-wave range at the start of this PhD work. Despite the excellent achievements with this structure, the device reliability under harsh conditions still needs to be demonstrated.

One of the aims of this thesis is to develop a robust AlN/GaN HEMTs technology with high RF performances operating in the millimeter-wave up to 94 GHz.

Table.1.5. State of the art DC and RF AlN/GaN-based HEMTs performances [18], [20], [84], [92], [128]–[132][133].

Organization	Growth Method	Substrate	L_g (nm)	Operation Range	Electron Density (cm^{-2})	Mobility ($cm^2/V.s$)	R_C (ohm.mm)	Peak g_m (mS/mm)	F_t	F_{max}	PAE	P_{out} (W/mm)
HRL [129]	MBE	SiC	40	NA	$1.3x10^{13}$	1200	NA	723	220 GHz @2V	400 GHz @6V	NA	NA
HRL [20]	MBE	SiC	4O	PA 83 GHz	NA	NA	NA	NA	200 GHz	400 GHz	27%	1.37
HRL [130]	MBE	SiC	20	NA	$1.2x10^{13}$	1200	NA	1360	454 GHz	444 GHz	NA	NA
HRL [131]	MBE	SiC	20	32 GHz	$1.2x10^{13}$	1200	NA	NA	310 GHz	582 GHz	59%	0.44 @V_{DS}=3V
IAF [18]	MOCVD	SiC	70	PA 71 GHz	NA	NA	0.25	470	110	300	9.9%	0.95 @V_{DS}=10V
IAF [132]	MOCVD	SiC	50	PA 190 GHz	NA	NA	NA	NA	140	330	1.2%	0.279
IAF [92]	MOCVD	SiC	100	NA	$1.1x10^{13}$	1480	0.3	600	89	208	NA	NA
IEMN [128]	MOCVD	SiC	150	40 GHz	$2x10^{13}$	950	0.4	400	75	200	33%	2.3 W/mm @V_{DS}=15V
IEMN [133]	MOCVD	SiC	120	40 GHz	$1.8x10^{13}$	NA	NA	400	55	235	46.3	4.5 W/mm @V_{DS} = 20V
IEMN [84]	MOCVD	SiC	120	40 GHz	$1.8x10^{13}$	1100	0.3	500	60	242	52%	7 W/mm @V_{DS}=25V

V. GaN device scaling technologies

For millimetre-wave applications, GaN HEMT device scaling is required to improve the high frequency performances. These optimizations are needed not only for the epitaxial structure but also for some processing steps such as ohmic contacts, and gate module. Since the critical device dimensions tends to nanometer scale, the electron transit time is reduced by using shorter gate lengths. Therefore, the thicknesses of HEMT epitaxial layers should be reduced especially the barrier thickness. However, a high

aspect ratio L_G/a above 15 [134] should be maintained to prevent short channel effects while improving the F_t/F_{max} ratio that are defined by the following equations:

$$F_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})}, F_{max} = \frac{F_t}{2(R_g+R_{ds})^{1/2}}$$

Where g_m, C_{gs}, C_{gd} and R_{ds} are transconductance, gate-to-source capacitance, gate-to-drain capacitance, gate resistance and drain-to-source distance, respectively.

Reduction of intrinsic and extrinsic parasitic elements such as R_g and C_{gd} in GaN HEMTs has significantly improved device performances. Following many efforts from the research community, the best F_t and F_{max} reported to date are 450 and 600 GHz for W-band applications as shown in **Figure.1.28**. These performances have been achieved through innovative device technologies such as T-shaped gate [131], n^+ GaN ohmic contact regrown [135], self-aligned gate process [136], vertically scaled epitaxy [131].

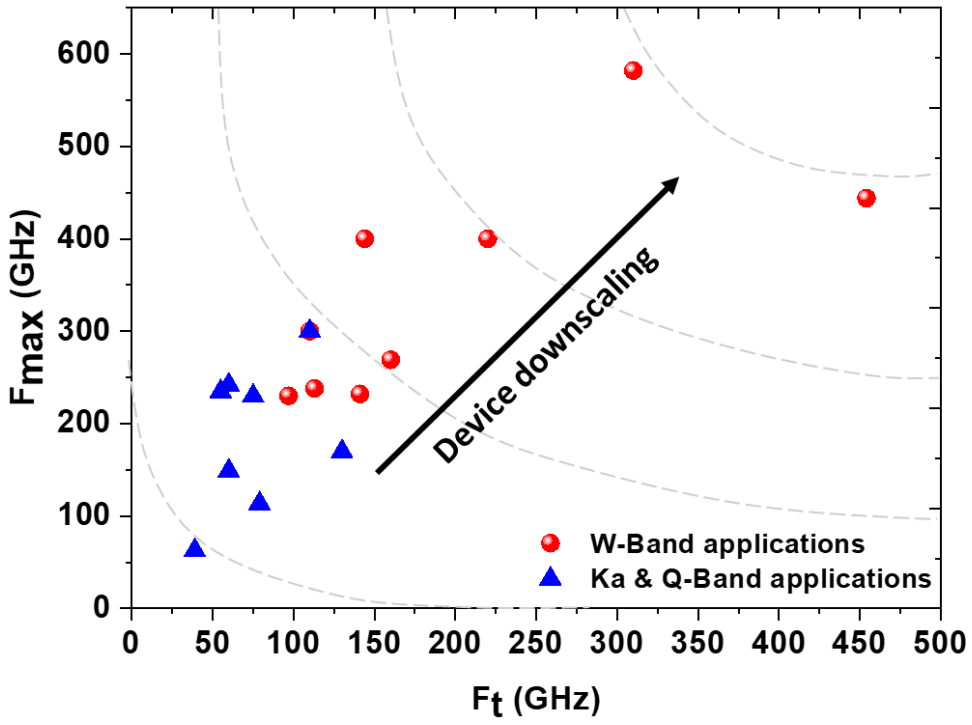


Figure.1.28. Comparison of cutoff frequencies (f_t) and maximum oscillation frequencies (f_{max}) among Ka up to W-band frequency

A short source-to-drain distance reducing the on-resistance has successfully increased F_t/F_{max} and maximum drain current. However, the breakdown voltage is directly affected due to the high electric field confined in such a small area. **Figure.1.29** shows the three terminal breakdown voltage as a function of L_G

for different L_{GD}. The plot demonstrates that L_{GD} have a large impact on the breakdown voltage. Therefore, an asymmetric gate structure with short L_{GS} and moderate L_{GD} was developed in order to maintain simultaneously high F_t/F_{max} and high breakdown voltage.

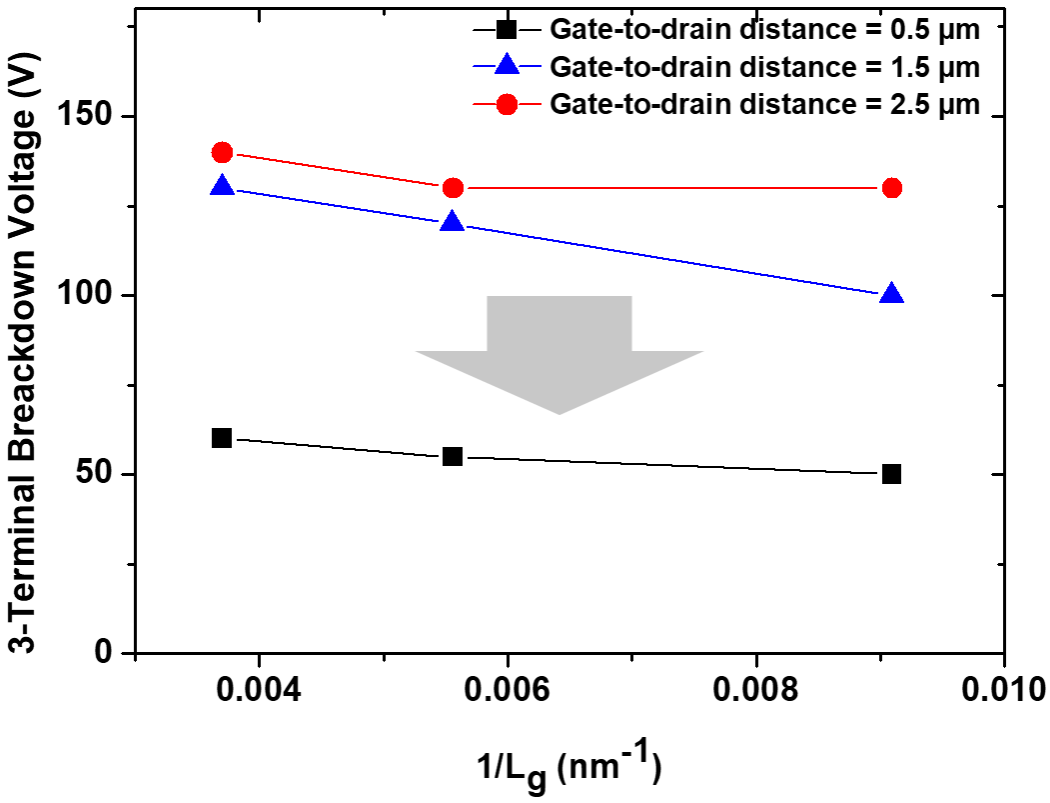


Figure.1.29. 3-Terminal breakdown voltage of GaN HEMTs as a function of gate length and gate-to-drain distance.

V.1. T-shaped gate and lateral scaling

The optimization of the gate module is the most important parameter to achieve high RF performances. T-shaped gate structures are widely used in order to reduce parasitic capacitances and gate resistance when reducing the gate length [45]. The frequency performances are currently mainly limited by short channel effects and parasitic elements which become of paramount importance with shorter devices. **Figure.1.30.a** shows a cross section of GaN HEMT structure illustrating the parasitic elements and the benefit of the T-gate design on device performances using short gate length [23]. A gate foot height (H_{gf}) above 100 nm is required to improve F_{max}. Otherwise, the guiding principle in improving F_t is reducing the gate length while maintaining a high aspect ratio L_G/a combined with high carrier density n_s. A significant increase of F_t has been demonstrated with reducing gate length down to 20 nm as shown in **Figure.1.30.b**.

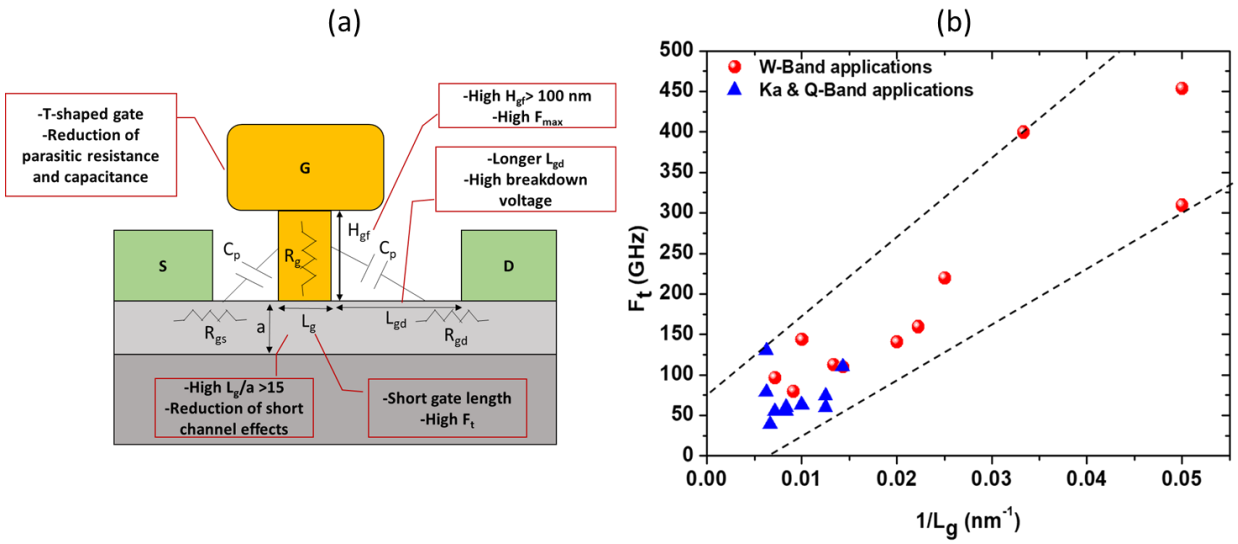


Figure.1.30. Cross section of T-gate GaN HEMT (a) and scaling of cutoff frequency (F_t) of GaN HEMTs as a function of gate length (L_G) (b)

V.2. Advanced ohmic contacts

In order to achieve high RF performances with aggressive device scaling, it is mandatory to reduce the contact resistances as it generally dominates the parasitic resistance. However, it is difficult to achieve low contact resistance through (Al, Ga, In)N Al-rich barrier layers due to their wide bandgap. In addition, higher Al content and thicker barrier layer lead to higher contact resistances which indicates a correlation between the barrier layer composition and the contact resistances.

Design optimization of the metal stack is critical to form high quality ohmic contacts. Various metal schemes have been investigated over time in order to improve contact resistivity, surface morphology and sharp edge acuity. A standard Ti/Al/Ni/Au metal stack has been widely established as ohmic contacts for HEMT devices due to the simple and low-cost method, which are formed by annealing this complex metal stacks at an optimum temperature. However, the Ti/Al-based metal stack requires high annealing temperature typically above 800°C resulting in severe lateral ohmic metal diffusion as well as rough metal surface. Typical contact resistances are about 0.25 to 0.5 Ω.mm leading to high parasitic resistances proportional to the device scaling. Several approaches have been studied in order to successfully reduce the contact resistance:

- The use of other metal stacks such as Mo and Ta-based ohmic contacts since it required an anneal temperature lower than 600°C resulted in an excellent surface morphology [137]–[139].

- Pre-metallization surface treatment using plasma in order to prevent and minimize the oxidation of the Al-rich barrier layer [137].
- Recessed ohmic contacts enable lower annealing temperature and thus better contact definition. It has been demonstrated that the optimum contact ohmic is obtained when the metal stack is closer to the 2DEG channel without degrading the GaN layer [140][141].
- Regrown n+-GaN ohmic contacts by MBE technique has been shown to be a viable technology to reduce parasitic access resistances [131][136]. The ohmic contact regrowth approach allows direct contact between n+-GaN and 2DEG layers leading to low interface resistance. This approach is used for aggressive design where the gate-to-source distance needs to be reduced leading to excellent device performances.

Among these approaches, regrown n+-GaN ohmic contacts is the most promising technology to reduce parasitic access resistance. Several studies have been reported excellent ohmic contacts with Rc as low as 0.1 Ω.mm. However, regrowth ohmic contacts method is not only more complex but also increase the cost significantly, which may make it less suitable for large-scale foundry process. As expected, the combination of high electron mobility and high carrier sheet density are key parameters to reduce parasitic resistances along to the device size scaling. This makes the electron mobility an important feature for millimeter-wave applications

VI. GaN-HEMTs: existing technologies in millimeter-wave range

The conventional GaN HEMT are generally developed with a Ga-polar crystal orientation where the 2DEG is formed at the barrier layer/channel interface while the polarization is inverted in N-polar heterostructures as shown in **Figure.1.31**. As a result, the N-polar HEMT structure presents several advantages such as an improved electron confinement owing to the strong back barrier, low ohmic contact resistivity and improved scalability when using shorter gate length, as the aspect ratio L_G/a is independent of the backbarrier layer thickness. On the other hand, as mentioned previously Ga-polar HEMTs can use ultrathin Al-rich barrier in order to increase the 2DEG density while maintaining high aspect ratio L_G/a.

Researchers from different laboratory have demonstrated state of-the-art devices performances in millimeter-wave range using both Ga and N-polar heterostructures.

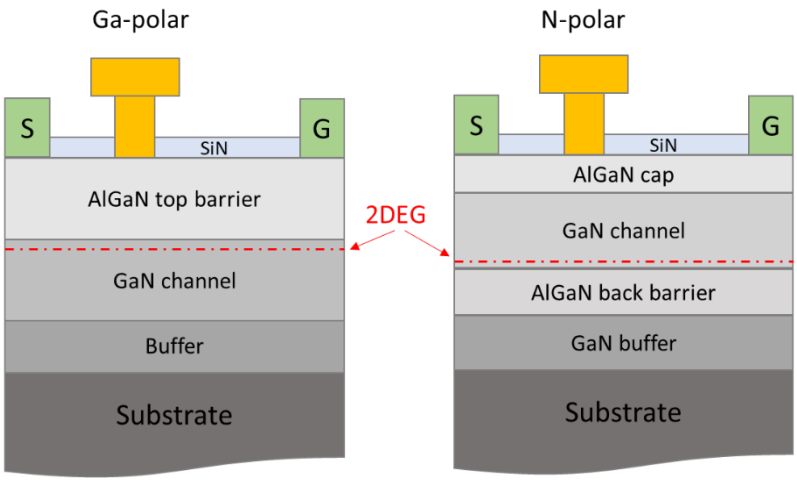


Figure.1.31. Device schematic cross section of Ga-polar and N-polar HEMTs

VI.1. Ga-polar technology

Hughes Research Laboratories (HRL) has recently demonstrated important results in this frame. High RF performances reflected by an F_t/F_{max} of 454/444 GHz using a fourth generation asymmetric self-aligned T-gate GaN HEMTs [130]. For these devices, the gate length was 20 nm and ohmic contact regrowth technique is used allowing direct contact of n^+-GaN to the 2DEG enabling extremely low interface resistance of 0.026 Ω.mm. An ultrathin sub-5 nm AlN barrier is used to both deliver high electron density n_S and maintain a high aspect ratio L_G/a. The asymmetric self-aligned gate with L_{GS} = 30 nm and L_{GD} = 80 nm allows high speed transistors with a breakdown voltage of 17V. With the same device using a gate length of 40 nm, a record power amplifier achieved high large signal performances at W-band. Output power was 1.37 W/mm associated to a PAE of 27% at 83 GHz [20]. Recently, high speed graded channel (GC) AlGaN/GaN demonstrated a large potential to operate at high frequency. **Figure.1.32** shows a 60 nm T-gate GC AlGaN/GaN HEMTs with the associated RF performances. The GC for this structure within an AlGaN layer with Al-composition graded from 0% to 10% leads to improve the output power density compared to the standard AlGaN/GaN HEMT. 30 GHz large signal measurements showed an outstanding PAE of 75% with an output power of 2.1 W/mm [55].

Figure.1.33 shows the cross section of Fujitsu's 80 nm gate length InAlGaN/GaN HEMT technology. InAlGaN barrier is well known for its high 2DEG density combined to a high electron mobility. it was used to avoid the formation of surface pits thus reducing the gate leakage current as compared to the ternary InAlN, which is required to improve the breakdown voltage and device reliability [123]. A double SiN passivation layer has been used to eliminate the current collapse. The offset overhanging gate was adopted to decrease the electric field without degrading high frequency performances. Load-pull

measurements at 96 GHz show high output power of 3 W/mm at V_{DS} = 20V under pulsed mode operation (**Figure.1.33**). Besides, an improved 80 nm gate length InAlGaN/GaN HEMT demonstrated high power operation in the wide-frequency range from S to W-band, using regrown n+ GaN contact layer, an InGaN back barrier to reduce the off-state drain leakage current and an AlN spacer to improve the electron mobility. Moreover, a diamond heat spreader was introduced in order to decrease the thermal resistance and further improve the output power density. The maximum pulsed output power density of this InAlGaN/GaN MMIC amplifier was 4.5 W/mm at 94 GHz [142].

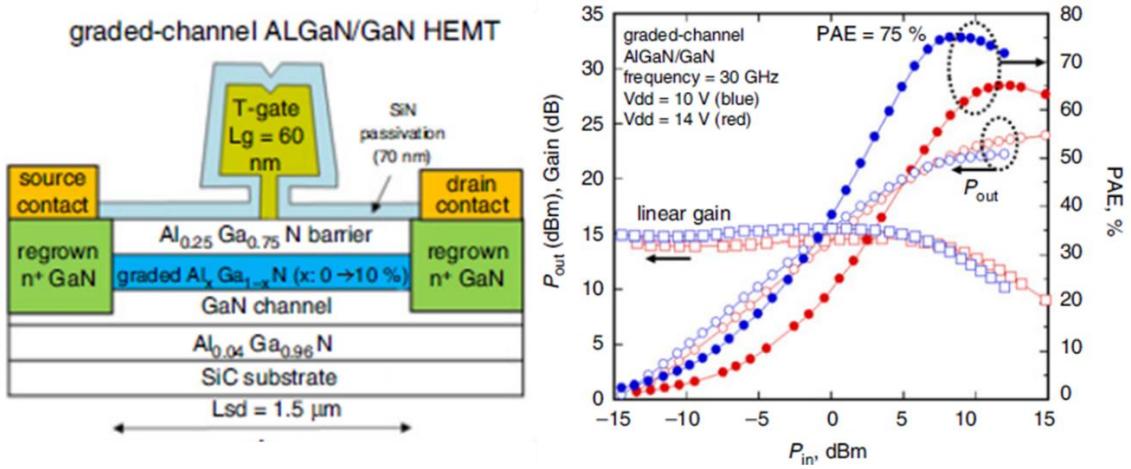


Figure.1.32. Schematic cross section of the HRL GC AlGaN/GaN HEMT (left) and associated RF power performances at 30 GHz (right)

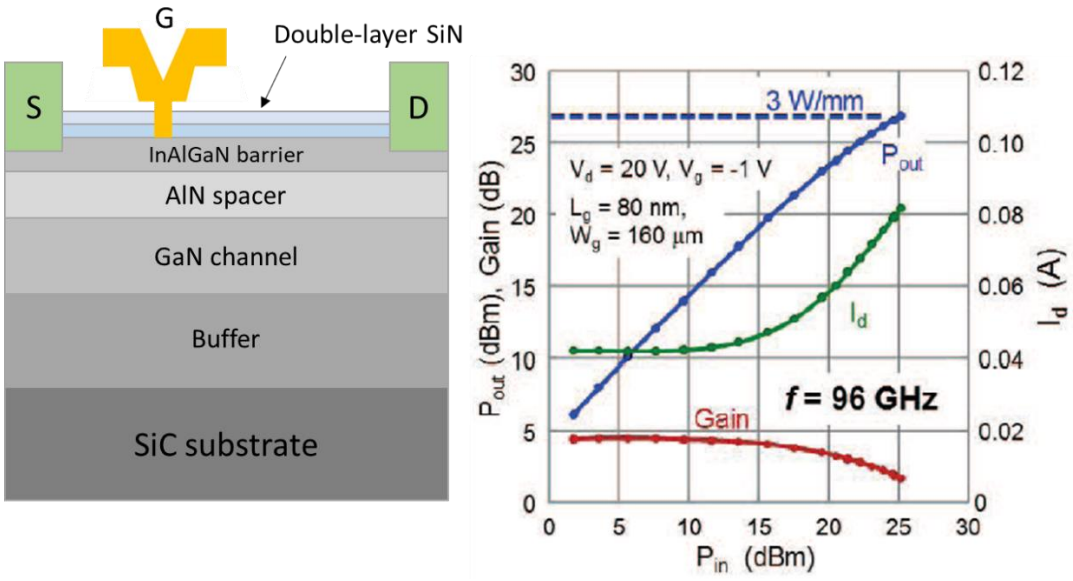


Figure.1.33. Schematic cross section of the Fujitsu InAlGaN/GaN HEMT (left) and associated RF power performances at 96 GHz (right)

Figure.1.34 shows a cross section of 120 nm AlN/GaN HEMT from IEMN laboratory as well as the associated RF power performances. The structure is based on 4 nm AlN barrier delivering high electron density n_s of 1.8×10^{13} cm^{-2}. C-doped GaN buffer is used to enhance device performances together with excellent electron confinement compared to AlGaN back-barrier. Pulsed large signal measurements at 40 GHz show high-saturated output power density of 7 W/mm associated with a PAE of 52% at V_{DS} = 25V [84]. The use of higher bias operation (V_{DS} > 20V) while using a short gate length confirms that the thermal resistance induced by the buffer layer is reduced. This technology is promising for achieving high device reliability.

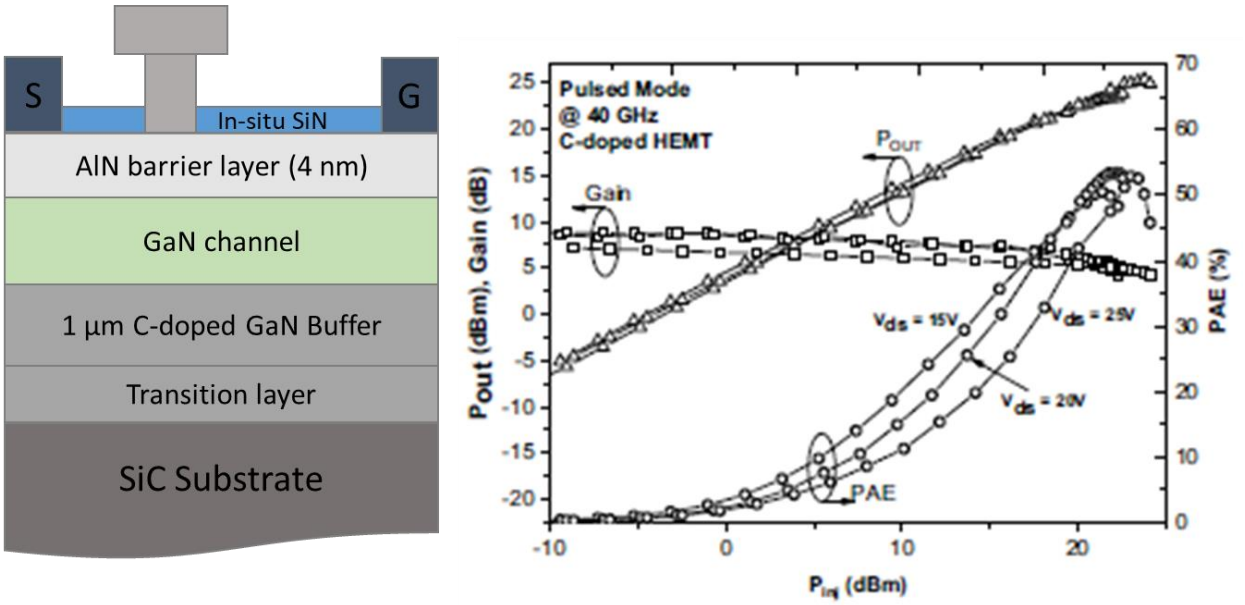


Figure.1.34. Schematic cross section of IEMN AlN/GaN HEMT (left) and associated RF power performances at 40 GHz (right)

VI.2. N-polar technology

Development of N-polar GaN devices and recent results reported by University of California, Santa Barbara (UCSB) shows large potential for improvements in the millimeter-wave power applications. N-polar deep recess MIS-HEMT with a gate length of 48 nm obtained by using atomic layer deposition (ALD) ruthenium resulted in a high-power gain of 8.1 dB at 94 GHz. The deep recess structure is used to control DC and RF dispersion. CW load-pull measurements at 94 GHz show a record output power of 6.2 W/mm associated with a PAE of 33.8% at V_{DS} = 18V (**Figure.1.35**) [76]. It can be noticed that the device robustness under harsh conditions still needs to be demonstrated with this configuration system.

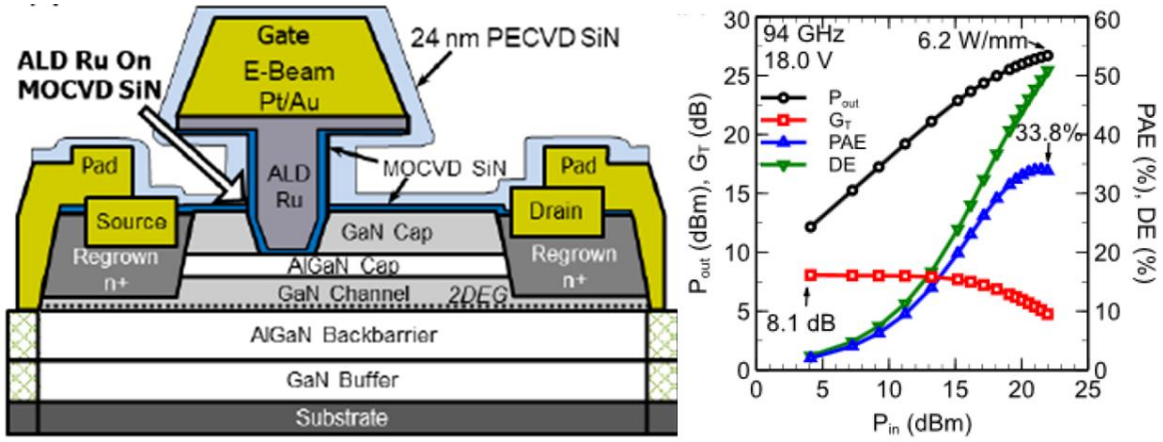


Figure.1.35. Schematic cross section of UCSB N-polar MIS-HEMT (left) and associated RF power performances at 94 GHz (right)

Figure.1.36 shows a summary of reported Ga-polar vs N-polar W-band RF performances. These results show a superior combination of PAE and output power density with N-polar devices at high frequency. However, the optimum technology choice is not based only on pure performances but also on the device reliability / robustness under harsh conditions as well as the ability to produce the technology in an industrial environment. This will determine in a near future which GaN-based structure will be best suited for millimeter-wave applications.

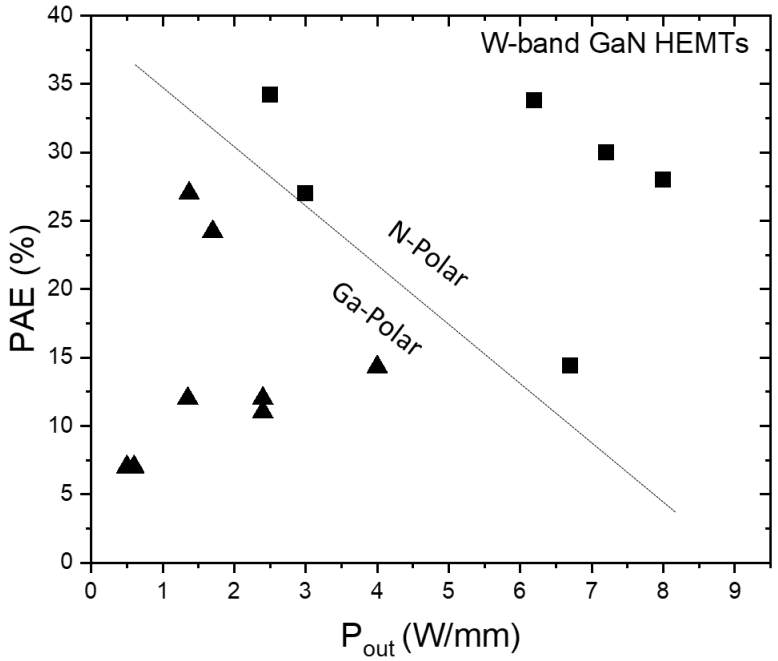


Figure.1.36. PAE versus associated P_{OUT} of N-polar (square) and Ga-polar (triangle) devices in W-band.

VII. Review of state-of-the art GaN transistors

Figure.1.37 shows a benchmark of a PAE as a function of P_{OUT} for GaN HEMTs in millimeter-wave range up to W-band. T. Palacios et al. reported a record P_{OUT} of 10.5 W/mm at 40 GHz using AlGaN/GaN HEMT technology with L_G = 160 nm, with a PAE of 33% that was limited by a small signal gain of 6 dB [117]. Recently, J.S. Moon et al. reported a graded-channel AlGaN/GaN HEMTs with an output power density of 2.1 W/mm associated with a PAE of 75% in CW mode at 30GHz [55]. Also, at 40 GHz F. Medjdoub et al. demonstrated in pulsed mode ultrathin AlN/GaN HEMTs with a PAE of 52% and an associated P_{OUT} of 7 W/mm at V_{DS} = 25V [84]. Therefore, RF performances of GaN HEMTs were improved compared to other technologies. Advanced research continues to extend GaN devices to high frequency up to W-band and beyond. High RF performances have been achieved through innovative device scaling technologies. Many efforts have been made in order to satisfy W-band requirements such as a short gate length (deep sub-100 nm), high F_t/F_{max} and low contact resistances. In 2006, Micovic et al. reported a first W-band GaN transistors with a high PAE of 14% associated to a P_{OUT} of 2.1 W/mm [143].

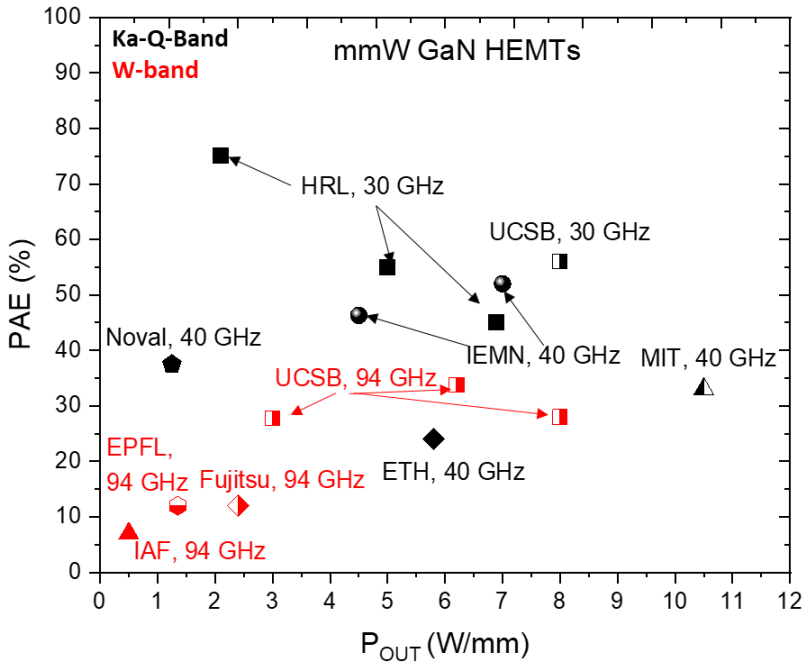


Figure.1.37. Benchmark of PAE as a function of P_{OUT} for mmW GaN HEMTs.

K. Mikiyama et al. demonstrated 3 W/mm P_{OUT} at V_{DS} = 20V under pulsed mode using 80 nm InAlGaN/GaN HEMTs at 96 GHz [123]. Although, these Ga-polar GaN HEMT structures have shown high performances at high frequency range, researchers from UCSB have developed N-polar GaN HEMTs providing a P_{OUT} of 6.2 W/mm associated with a PAE of 33.8% at 94 GHz [76]. However, these

performances need to be balanced with the device reliability under harsh condition that has to be definitely considered and assessed in order to pave the way of the next generation of millimeter-wave applications.

VIII. Conclusion

Nowadays, GaN-based HEMTs are becoming a key technology for millimeter-wave applications. Because of outstanding material properties, recent advances in GaN device designs provided a sharp increase in performances including high power, high efficiency, reliability, and compact size. These capabilities are ideally suited for numerous millimeter-wave power applications such as wireless networks and PAs MMIC for Q-band frequency and beyond. Therefore, GaN will play a important role in advanced RF and millimeter-wave applications including for instance 5G and satellite communications or military oriented applications in harsh environment. Thermal management, especially when using small component sizes, together with full control of surface and bulk traps will be the main challenge to ensure the required device reliability.

In this context, the main focus of this work is to develop GaN HEMT devices capable of delivering a combination of high power/high efficiency associated with a proven device reliability operating in the millimeter-wave range.

Chapter 2: Device fabrication and characterization methods for GaN HEMTs

I. Introduction:

As mentioned in chapter 1, high performances and robustness of GaN HEMT-based technology operating in the millimeter-wave range are of great importance. Recent progress in GaN HEMT devices have allowed the demonstration of high RF performances up to Q-band. However, at higher frequency, the efficiency and the reliability of GaN HEMTs are still limited mainly due to the lack of power gain, the enhanced trapping effects and reduced electron confinement when downscaling the device size or self-heating. Therefore, GaN HEMTs have evolved with the optimization of the epi-structure design and related process technology, which are essential to overcome the issues related to the dispersion and trapping effect phenomena thus allowing high performances of both transistors and MMIC. To address these challenges, several aspects were considered in this work with the aim of achieving both high RF performances and reliability. **Figure.2.1** shows the challenges to be addressed from the epitaxial growth structure to the device processing.

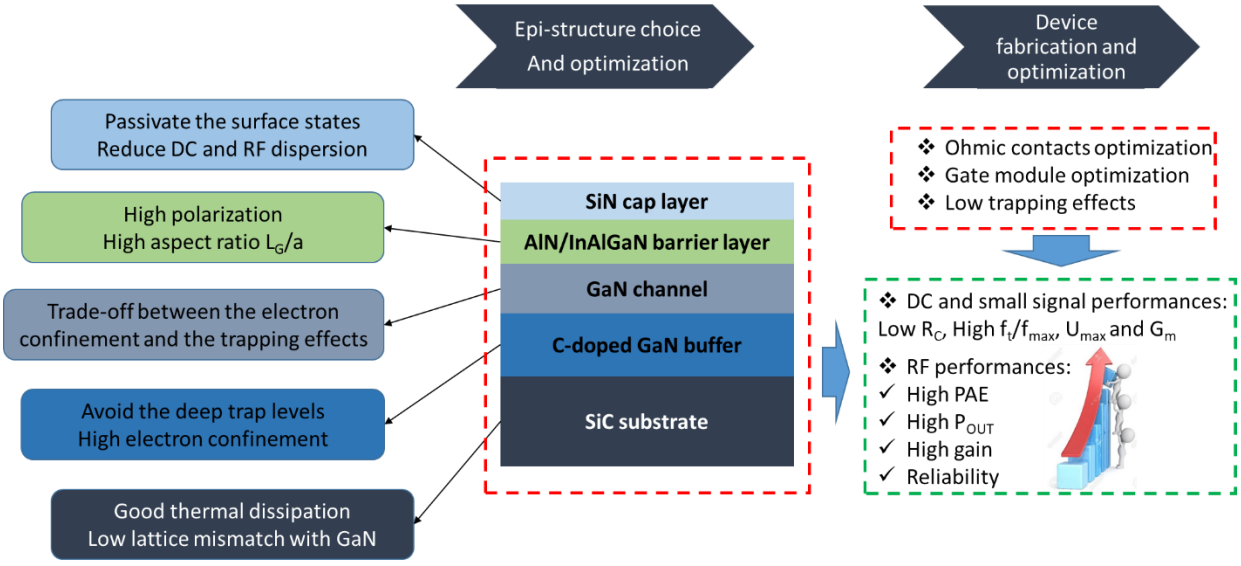


Figure.2.1. Schematic process from the epitaxial structure to the device fabrication showing the challenges to be overcome to achieve high performances.

This chapter describes the fabrication process of GaN HEMTs operating at high frequency as well as the device characterization tools which are used with a measurements protocol established in this framework. It can be noticed that GaN HEMT devices were processed and characterized at IEMN. In the first part, we will detail the processing development, the mask sets used for the fabrication of the components as well as the characterization techniques to validate the intermediate steps of the fabrication.

A shared process between UMS and IEMN will then be presented. Finally, we will describe the bench and the methods used for small and large signal characterizations.

II. Fabrication techniques

The fabrication process of HEMTs was carried out at the clean room of IEMN laboratory. Although the epitaxial structure used are different, the fabrication process remains relatively similar for each of them. The different steps of this process are shown in **Figure.2.2** and are detailed below. In particular, we will highlight the optimization performed for some processing steps especially the fabrication of the ohmic contacts and the gate module, which are critical for transistors operating at high frequency. The HEMTs studied in the framework of this thesis have a standard topology with two gate fingers, two source contacts and drain contact as shown in **Figure.2.2 (f)**. As a part of a project in collaboration with UMS foundry, transistors with multiple fingers have been studied. The fabrication of a complete HEMT device may involve five different processing steps as follow:

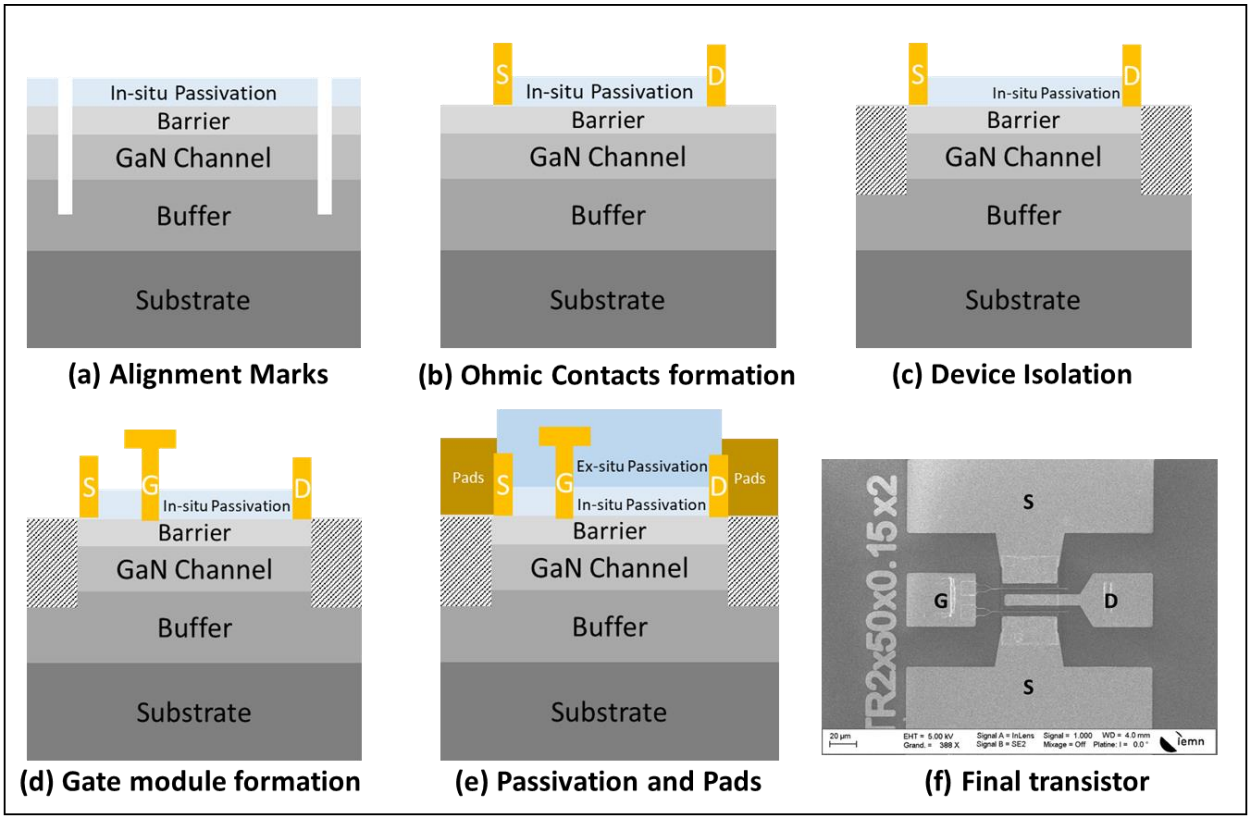


Figure.2.2. Process flow schematic of a GaN transistor fabrication (a-e), and SEM image of the final transistor (f).

(a) Alignment marks: The mark patterns are used to align the different fabrication steps since any device requires more than one pattern or level step of fabrication. The pattern for different lithography steps that belong to a single device must be aligned to one another in order to make functional devices. The first pattern transferred to a wafer usually includes a set of alignment marks, which are used as a reference when aligning the subsequent patterns. In this work alignment marks are realized by Inductively Coupled Plasma (ICP) deep etching. Using Cl_2/A_r plasma, alignment marks are etched to a depth of 500 nm as shown in **Figure.2.3**. The etched marks are used instead of metallized marks in order to avoid a poor surface roughness of the metal after the ohmic contact annealing step.

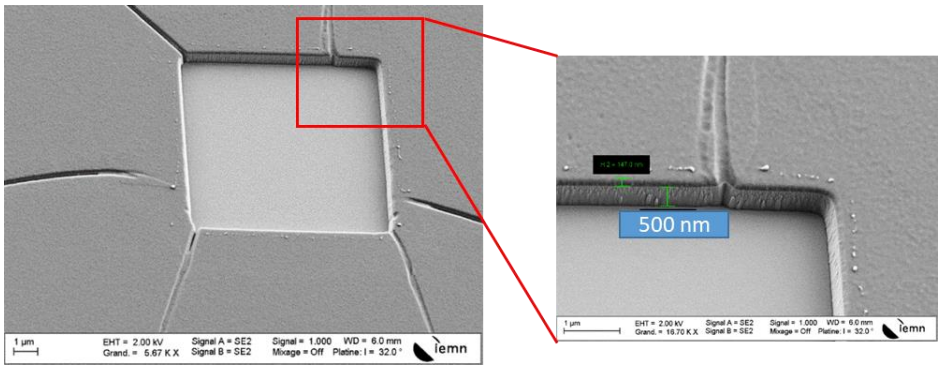


Figure.2.3. Tilted SEM image alignment mark.

(b) Ohmic contacts formation: An ohmic contact is a metal/ semiconductor contact, which is formed on top of the barrier layer having a linear current-voltage characteristic. A low resistance and thermally stable ohmic contacts are required for high frequency GaN HEMTs. This ensures a high maximum drain current density, a reduced on-resistance and a high extrinsic transconductance enabling high cutoff frequency (f_t) and high maximum oscillation frequency (f_{max}). The ohmic contacts are formed with a "Lift-Off" process technique, which is commonly used for III-V components. After the patterns have been defined by e-beam lithography, MOCVD SiN cap layer is etched using Reactive Ion Etching (RIE) SF_6 plasma. Then a Ti/Al/Ni/Au stack is deposited by metallic evaporation and the excess metal above the resist is removed by Lift-Off. Finally, high temperature annealing is carried out in order to reduce the contact resistance. The optimization of the ohmic contacts will be detailed more in the following sections.

(c) Device isolation: The purpose in this step is to isolate electrically the active operating area of the components, which is defined by an optical lithography since a low resolution is required. This can be carried out in two different methods: by physico-chemical deep etching by ICP (mesa technology) or by ion implantation using argon, nitrogen, helium or oxygen. Within the framework

of this thesis, ion implantation using nitrogen atom was used. The energies and implantation doses were optimized in order to break the crystalline structure of the implanted material and to make the semiconductor amorphous thus preventing any parasitic conduction.

(d) Gate module formation: The gate module is a critical step for high frequency transistors. The necessity of reducing the gate length leads to an increase of the transistor performances, in particular the cut-off frequency (f_t) and the maximum oscillation frequency (f_{max}). The T-gate footprint is defined using e-beam lithography followed by anisotropic SiN cap layer etching. Then a Ni/Au metal stack is deposited on top of the barrier layer to form a Schottky contact. T-shaped gates are finally obtained by lift-off. Since achieving sub-100 nm gate length is required in this work, the optimization of the gate process technology especially the SiN cap etching is also necessary.

(e) Pads thickening: The pads formed in this step permit to connect the gate and makes source/drain easily accessible for device characterization. An optical lithography is used to define the pads. Then, a thick SiN passivation deposited after the gate module step is etched with RIE SF_6 plasma. A Ti/Au metallization is then deposited by evaporation, followed by a lift-off step. An SEM image of a final transistor is shown in **Figure.2.2.f**.

II.1. Description of the mask layouts used

The fabrication of transistors was organized in two stages: First, the evaluation of the epitaxial structures is required to determine if it could be useful for high frequency short ebeam device fabrication (which is expensive and time consuming). At this stage, we can extract a number of parameters such as the 2DEG properties of the heterostructure (n_s, µ…) and DC characteristics (I_{dmax}, V_{th}, g_m…) through a similar but faster process including typically large gate length (about 3 µm). This study is carried out by using an optical layout design called "GaN Test" (see **Figure.2.4**) which consists of optical photolithography steps only. This method enables to detect issues related to the epitaxial structures that could severely affect the device operation such as excessive gate leakage or poor electron mobility for instance.

Furthermore, if the evaluation of the epitaxial structures has shown satisfactory results, then we use these structures for the fabrication of high frequency transistors with a more advanced processing using electron-beam lithography. **Figure.2.5** shows the complete transistor layout design "GaN FAST" widely used in this work. This layout consists of three e-beam lithography steps (Alignment marks, ohmic contacts and gate module) and two optical photolithography steps (isolation and pads). The advantage of using e-beam lithography is the high resolution of patterns, allowing to achieve sub-100 nm short gate lengths for high frequency operation. However, the drawbacks of using this technique are the high cost and time consuming processing.

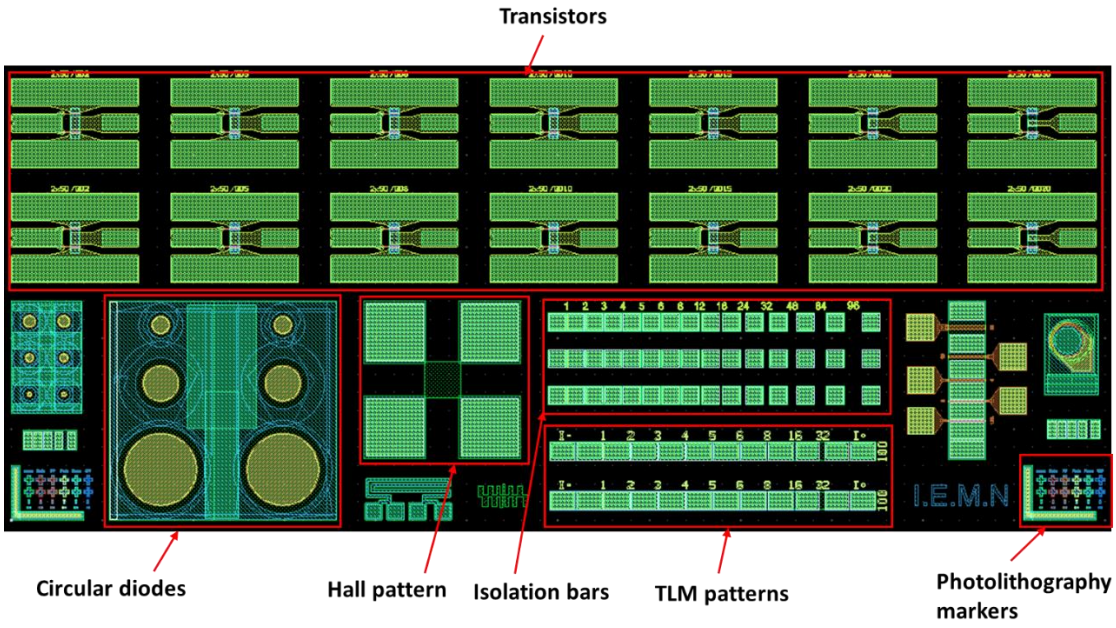


Figure.2.4. Layout design of "GaN Test" used for the fabrication of optical GaN HEMTs.

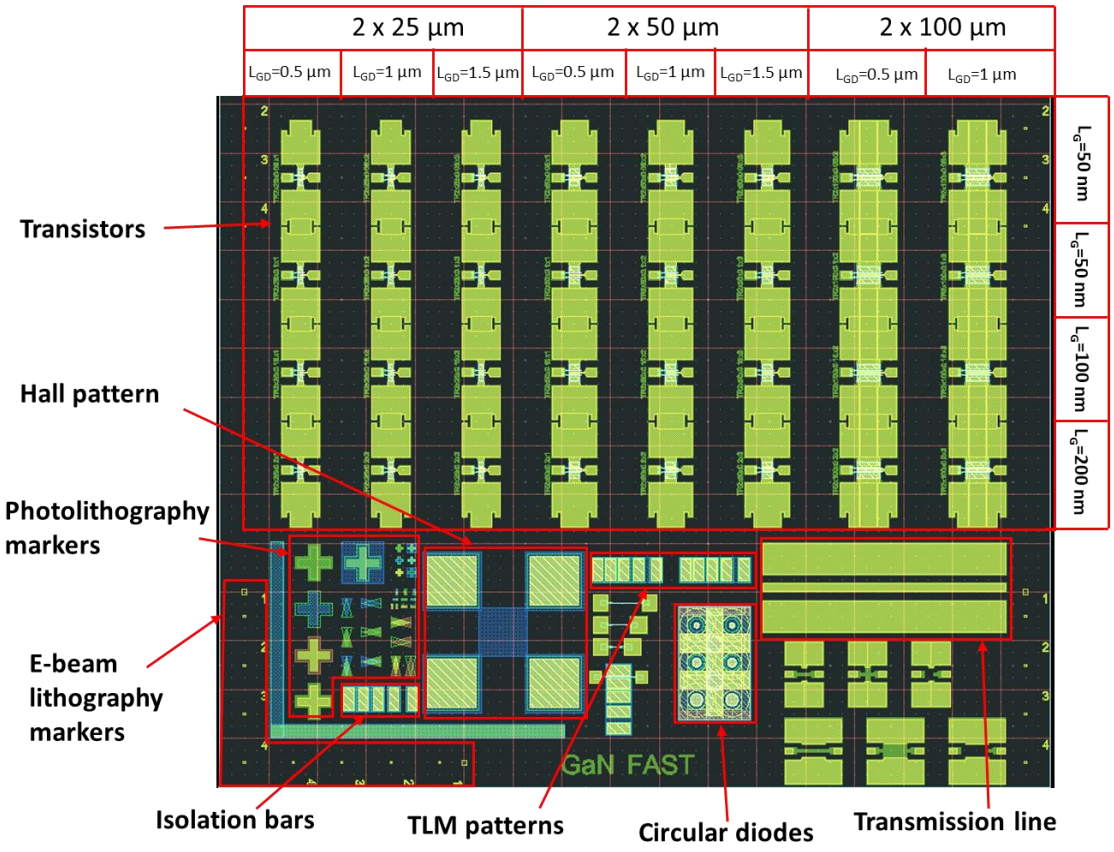


Figure.2.5. Layout design of "GaN FAST" used for the fabrication of e-beam GaN HEMTs.

"GaN test" and "GaN FAST" layout designs are rather similar and consist of a set of process control monitor patterns (PCM), alignment marks as well as transistors with various designs. We will focus on GaN FAST layout design since it is the most used in this work.

In the lower part of the layouts design, we can find a set of PCM, which allows to extract the electrical parameters of the epitaxial structure as well as to control the processing steps. TLM patterns are used to measure the maximum current density as well as the contact resistance by using Transmission Line Measurements (TLM). The Hall pattern is used to extract the 2DEG density, electron mobility as well as the sheet resistance of the heterostructures. Circular diodes allow to evaluate the Schottky or Metal Insolating Semiconductor (MIS) gate contacts while measuring the leakage current of reverse-biased diodes. The isolation step can be controlled and validated by measuring the leakage current between two isolated contact bars. Finally, transmission lines are used in order to assess the RF losses of the epitaxial structure.

In the upper part, we have 8 transistors columns available with 3 different gate width (W_G) of 2×25 µm, 2×50 µm, and 2×100 µm as shown in **Figure.2.5**. On each column, there are 4 transistors with 2 gate fingers and gate length varying from 50 nm to 200 nm. The variation of the gate to drain distance (L_{GD}) is 0.5 µm, 1 µm, and 1.5 µm while the gate-to-source distance remains constant (L_{GS} = 0.5 µm). **Figure.2.6** is a top view of a transistor showing the different distances between the gate and the S/D contacts.

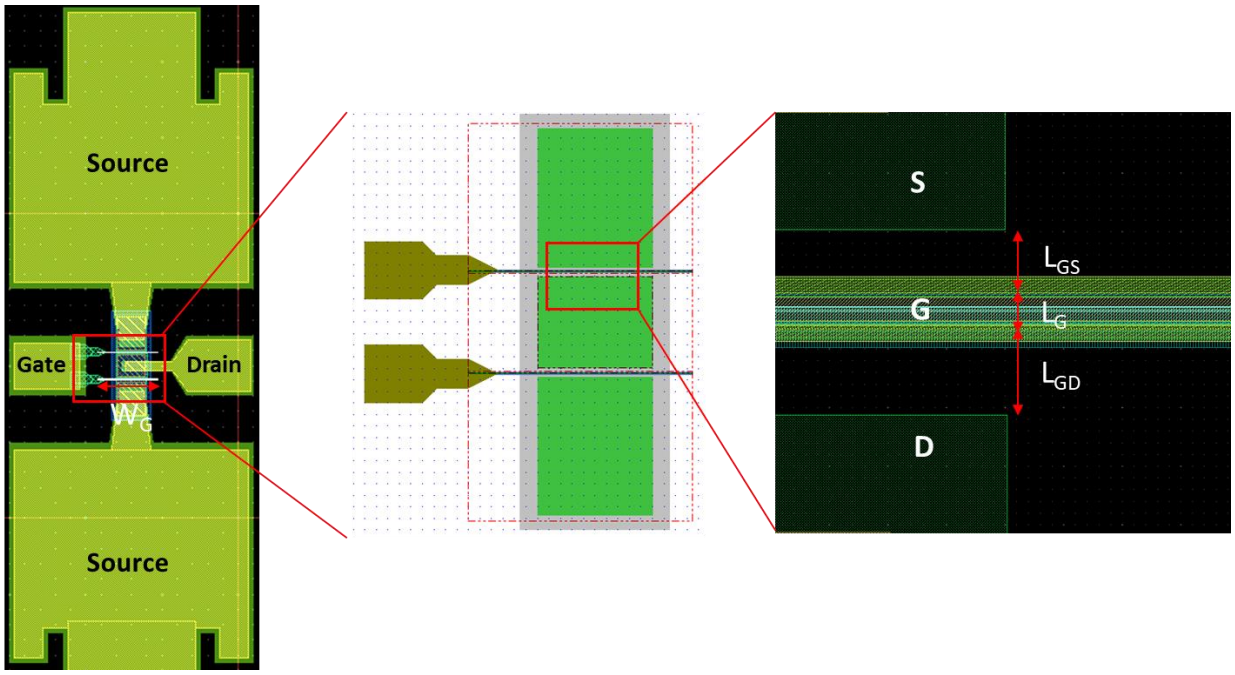


Figure.2.6. Top view of a transistor with 2 gate fingers

II.2. Optimization of device processing technology

Optimum performances of GaN-based HEMT devices requires the optimization of processing technology, in particular the metal / semiconductor contacts (ohmic contacts and gates) which lead to the improvement of the device performances operating at high frequency.

The metal-to-semiconductor contact can be either Schottky or ohmic. Schottky contact is naturally formed at the metal-semiconductor interface, which is used in GaN HEMTs as gate contacts. Although the barrier height at the metal / semiconductor interface is highly depend on metal work function, a high Schottky barrier is required in GaN HEMTs. Therefore, Ni/Au or Pt/Au are the popular Schottky contacts used for these types of transistors.

Schottky contact in GaN material system can turn into ohmic contact if the contact is annealed at high temperature due to the metal alloy inter-diffusion inside the barrier layer. In this case, metals having low Schottky barrier height in the range of 0.4-0.5 eV such as Al and Ti are required in order to form a high quality ohmic contact. Commonly used metal schemes for ohmic contact formation in the literature are Ti/Al/Ni/Au [144], Ti/Al/Mo/Au [145], and Ti/Al/Ti/Au [146].

This part describes the optimization of ohmic contacts and gate formation mandatory to achieve high GaN HEMT performances in the millimeter-wave range.

II.2.1. Ohmic contacts realization

A reliable ohmic contact process with low contact resistance (R_c) is crucial for high frequency performances of scaled devices. Power and RF performances are enhanced with low contact resistances. Furthermore, aggressive design with short gate-to-drain distance, the morphology and edge acuity of the contacts are of great importance in order to prevent short circuits with the gate metal.

II.2.1.1. Contact resistance optimization

A reduced contact resistance in GaN HEMT devices means that the 2DEG may be electrically contacted without adding additional resistance to the current. However, using a wide bandgap barrier layers separating the 2DEG from ohmic contacts lead to increased contact resistances, resulting from different parameters as illustrated schematically in **Figure.2.7**. A first contribution is related to the metal/Barrier layer interface ($R_{C.Metal/Barrier}$) and does not depends on the heterostructure properties. The two other components are correlated to the barrier thickness ($R_{C.Barrier}$) and to the 2DEG properties ($R_{C.2DEG}$).

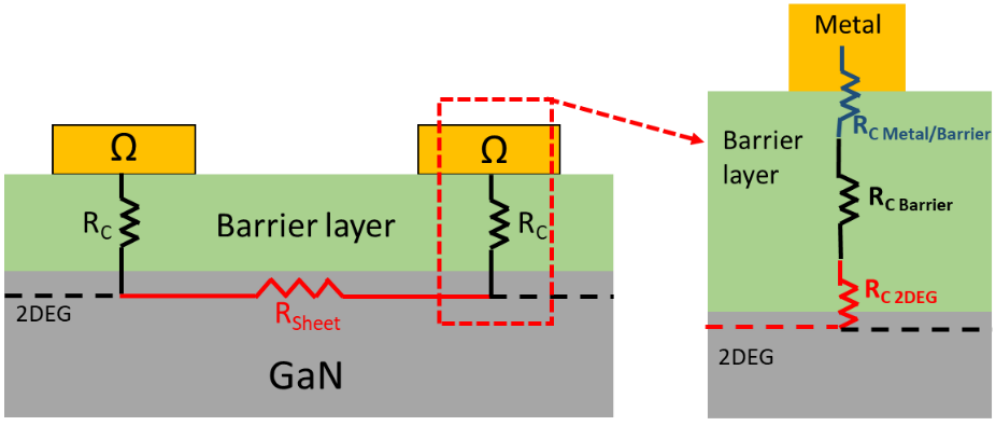


Figure.2.7. Schematic of a GaN HEMT structure showing the different contributions to the metal/barrier contact resistance R_C.

An optimum contact resistance is obtained through several techniques used for the fabrication of ohmic contacts on different barrier layer. The most popular technique is the use of a Ti/Al/Ni/Au metal stack followed by rapid thermal annealing (RTA) forming specific alloys that creates the ohmic contacts. The Titanium (Ti) is the first deposited metal acting as an adhesion layer, but also is at the origin of the formation of TiN alloy after annealing at the interface between the metal and the semiconductor. The diffusion of TiN into the barrier layer leads to the formation of nitrogen vacancies that act as donors and increase the net carriers concentration [140][147]. The aluminum (Al) allows to form a Ti-Al alloy at the interface with the titanium which minimizes the reactivity between titanium and GaN. The nickel (Ni) is referred as a barrier layer, which limits the inter-diffusion of Ti/Al and Au while improving the thermal stability of the contact [147]. Finally, gold (Au) is deposited in order to both benefit from its excellent electrical conductivity and to avoid any oxidation of the metal stack. This technique was optimized in the past at the laboratory and has demonstrated low contact resistances.

In the case of our epitaxial structures, the SiN cap layer is locally etched up to the barrier layer by SF_6 RIE plasma before the metallization. A Ti/Al/Ni/Au (12/200/40/100 nm) metal stack (**Figure.2.8**) is subsequently deposited by evaporation. During these different technological steps, it is essential to avoid the surface oxidation of the structure, which leads to the degradation of the contact resistance. Different techniques are used during the fabrication process to reduce the oxidation phenomena. First, metallization following the SiN etching needs to be performed as quick as possible in order to limit the formation of a native oxide on the barrier layer. A chemical deoxidation step in a weakly concentrated HF-based solution (BOE 7:1) is used before the sample introduction in the metallization room. Finally, when the sample is into the vacuum metallization chamber, an in-situ Ion Beam Etching (IBE) is carried out using Argon (A_r)

plasma. This step is a soft in-situ physical etching, which allows a surface treatment and ensure deoxidation of the barrier surface prior to the metal evaporation.

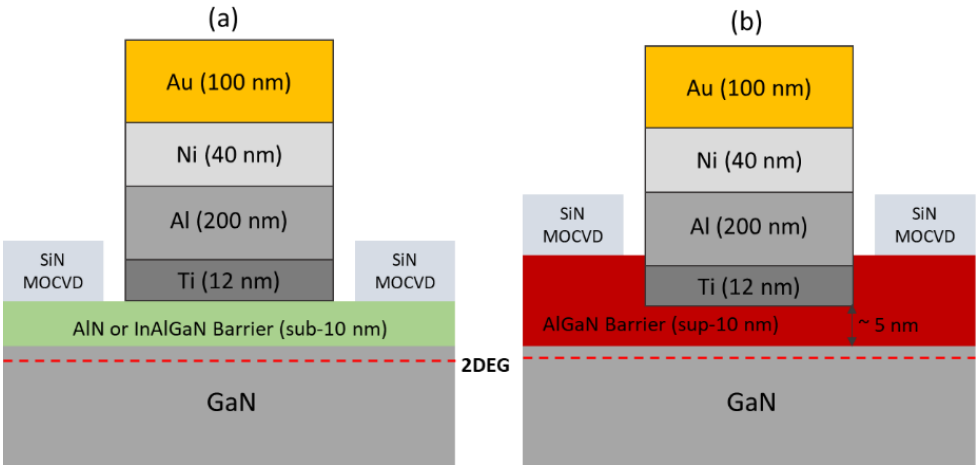


Figure.2.8. Non-recessed Ti/Al/Ni/Au ohmic contacts on AlN or InAlGaN/GaN (a) and partially recessed Ti/Al/Ni/Au ohmic contacts on AlGaN/GaN structures.

Different barrier layer-based structures have been studied in the framework of this thesis. For the sub-10 nm AlN or InAlGaN/GaN structures, the ohmic contacts are formed directly on the barrier layer as shown in **Figure.2.8.a**. After the metallization and lift-off, a subsequent annealing at high temperature of 850°C for AlN/GaN and 825°C for InAlGaN/GaN structures are performed in N_2 atmosphere. On the other hand, a specific ohmic contacts processing has been employed for the structures based on AlGaN barrier layer. In order to reduce the ohmic contact resistance, partially recessed ohmic contacts has been used prior to the metallization using Cl_2A_r ICP plasma. This etching step is necessary in order to bring the metal stack closer to the nearest conduction channel 2DEG without degrading the GaN layer as shown in **Figure.2.8.b**. An optimum contact resistance is obtained when around 75% of the barrier is etched followed by an annealing at 850°C.

II.2.1.2. Contact morphology optimization

Ti/Al/Ni/Au metal stack allows a reduced contact resistance. However, high temperature annealing of this metal stack causes significant lateral diffusion of metal alloys towards the SiN interface (**Figure.2.9.a**), which limits the scaling of source drain separation. This phenomenon appears on the epitaxial structure based on in-situ SiN cap layer. In fact, during annealing the lateral expansion of the metal opposes the SiN etched leading to the diffusion of the metal, which contributes to degrade the transistor performances by creating additional parasitic capacitances and short circuits between the source and the gate as shown in **Figure.2.9.b**.

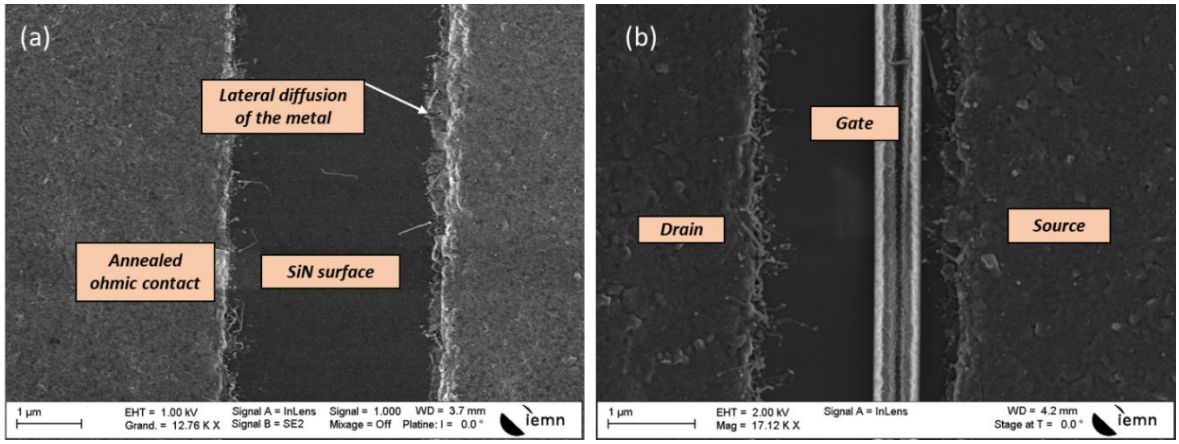


Figure.2.9. SEM image of a top view ohmic contact after annealing at 850°C showing a lateral diffusion of the metal (a) and a top view of the same ohmic contact after the gate formation very close to the source where the metal diffusion can generate a short circuit.

In order to better control the ohmic contacts morphology and to avoid the lateral diffusion of the metal towards the SiN interface, a SiN layer over-etching with a low power SF_6 RIE is carried out. This over-etching (**Figure.2.10.a**) allows to put away the SiN sidewalls by more than 100 nm from the deposited metal stack as shown in **Figure.2.10.b** and thus avoiding the metal diffusion due to the thermal expansion subsequent to the RTA. It can be noticed that the over-etching has no impact on the etching depth since the SF_6 plasma etching is highly selective with the conditions used. Therefore, through this method, we are able to achieve a significant reduction in lateral diffusion of metal, sharp edge acuity and smooth surface morphology after high temperature annealing process. **Figure.2.11.a** shows a SEM image of a top view ohmic contact after annealing at 850°C showing no metal diffusion owing to the SiN over-etching. **Figure.2.11.b** is a SEM image of ohmic contacts and the gate showing the benefits of the SiN over-etching.

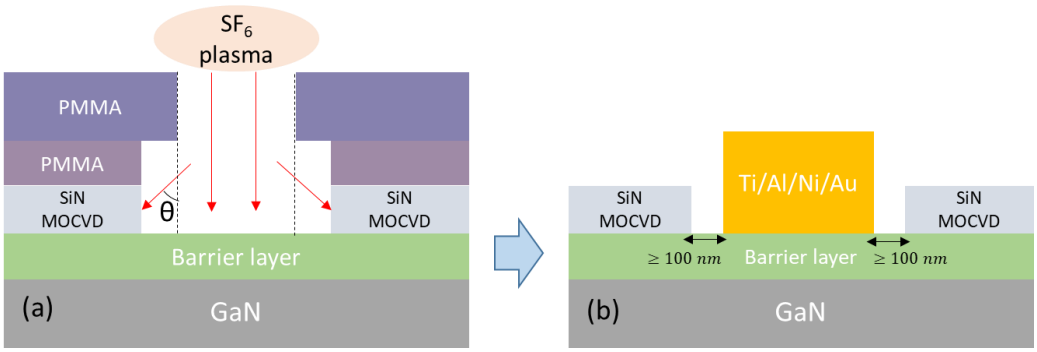


Figure.2.10. Process flow of ohmic contacts: (a) SiN etching step with SF_6 plasma and (b) Ti/Al/Ni/Au metallization step.

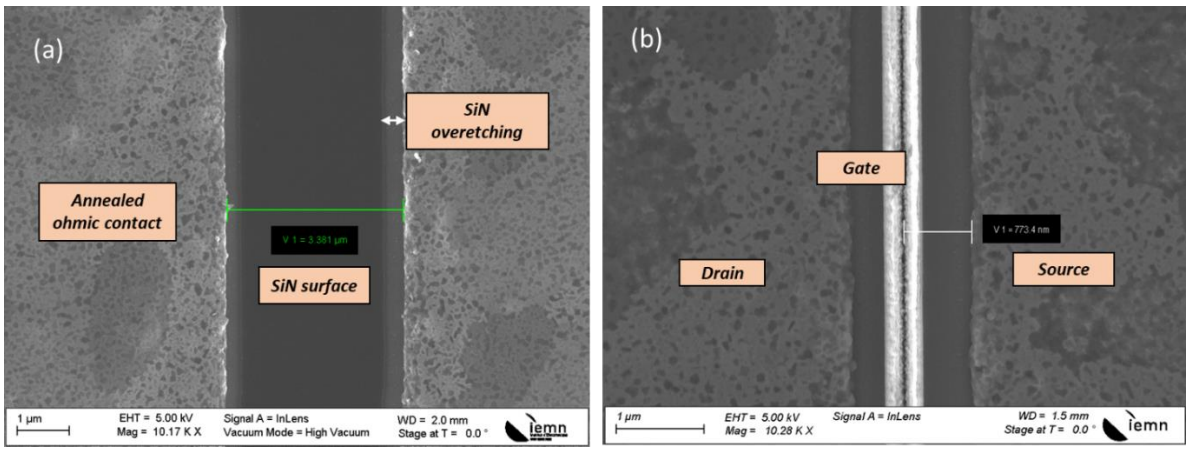


Figure.2.11. SEM image of a top view ohmic contact after annealing at 850°C showing no metal diffusion due to the SiN over-etching (a) and a top view of the same ohmic contact after the gate formation.

II.2.1.3. Transmission Line Model

The quality of ohmic contacts can be evaluated using the Transmission Line Method (TLM) test patterns as shown in **Figure.2.12.a**. It consists of rectangular metal contact with increasing spacing between them (d_0=2µm, d_1=5µm d_2=10µm, d_3=20µm). *W* is the contact width, and *L* is the contact length.

The total resistances are measured between two adjacent contacts. The current flows through the semiconductor from one contact to another. The total resistance R_T of a metal semiconductor contact is the sum of the resistances corresponding to each distance given by:

$$R_T = 2\frac{R_C}{W} + \frac{R_{Sheet}}{W}d$$

Where R_C is the contact resistance and R_{Sheet} is the sheet resistance of the semiconductor.

Ohmic contact resistance and semiconductor sheet resistance can be extracted through the linear fit plot of the measured total resistance as a function of the contact spacing *d* as shown in **Figure.2.12.b**. Sheet resistance R_{Sheet} is obtained from the slope of the linear fit while the contact resistance R_C is extracted from the intersect of the linear fit and y-axis. The current transfer length L_T obtained from the intersect of the linear fit and the x-axis, is the average distance that electrons (or holes) travel in the semiconductor beneath the contact before it flows up into the contact.

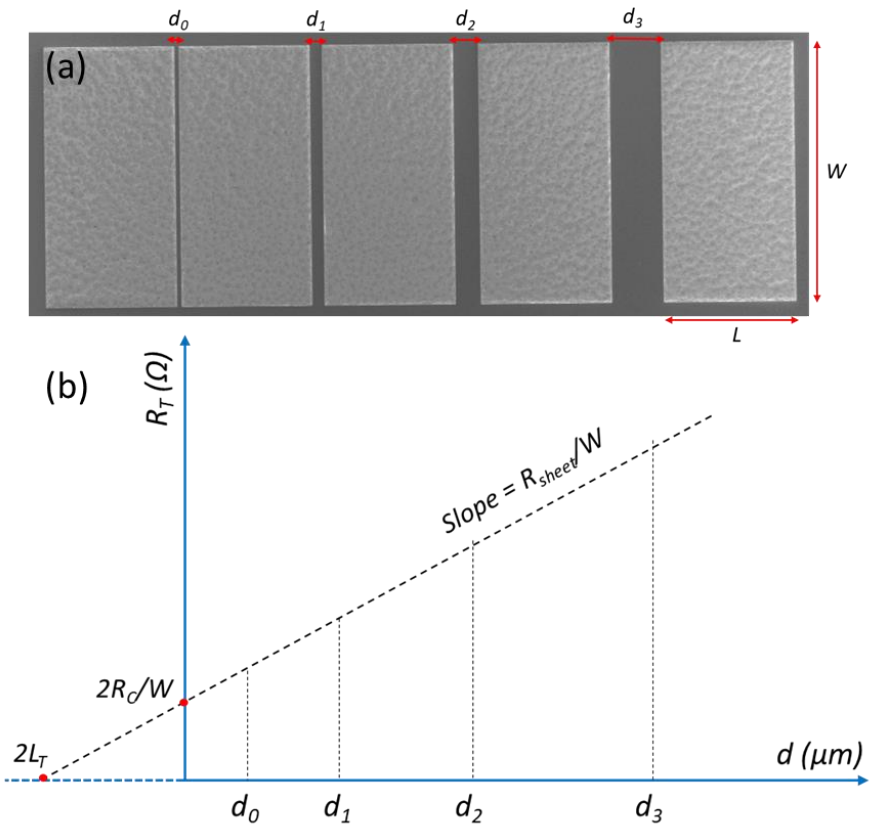


Figure.2.12. Transmission Line Method test pattern (a) and a plot of total resistance as a function of contact spacing *d*.

After metallization and lift-off, ohmic contacts are annealed at high temperature in order to significantly reduce the contact resistance. The influence of the temperature annealing, which is strongly dependent on the active layer of the heterostructures has been studied in order to optimize the contact resistance. This study was carried out on AlN, InAlGaN and AlGaN barrier layers. The average total resistance measured by TLM method was plotted as a function of different annealing temperature as shown in **Figure.2.13.a**. The lowest contact resistance for the 3 types of barrier layer were obtained with annealing at 850°C for AlN and AlGaN barrier layer and 825°C for InAlGaN barrier layer. The optimized contact resistance R_C of structures with InAlGaN barrier is 0.25 Ω.mm, which is lower than that of structure with AlN barrier (0.35 Ω.mm) and AlGaN barrier (0.3 Ω.mm).

The current density measured between two contacts separated by 2 µm for the three structures is shown in **Figure.2.13.b**. The high current density measured for AlN and InAlGaN barrier structures reflects the high electron density in the channel for these structures.

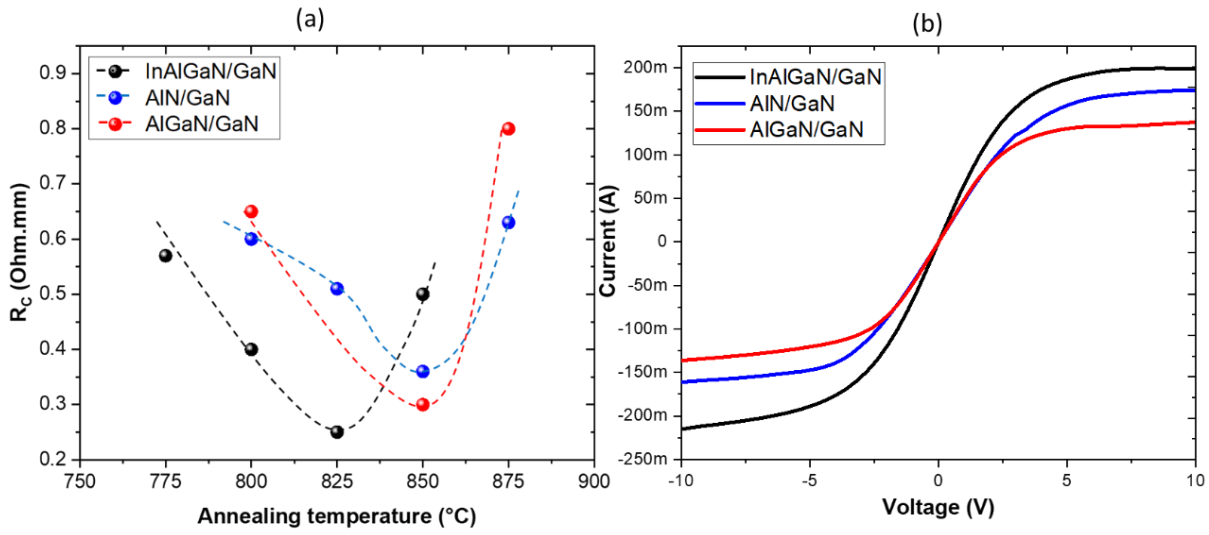


Figure.2.13. Specific contact resistance R_C evolution with the annealing temperature (a) and I-V measurements comparison of the different structures InAlGaN, AlN and AlGaN/GaN (b).

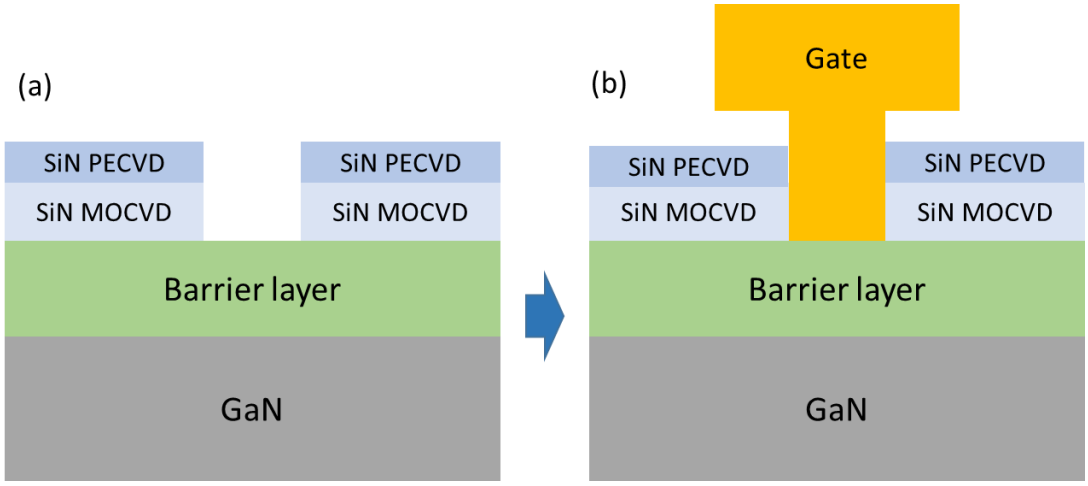


Figure.2.14. Gate formation of GaN HEMTs: SiN passivation etching (a) and gate metallization (b)

II.2.2. Gate Schottky optimization

The formation of Schottky contact for high frequency operation is a critical step for the fabrication of GaN HEMT. The main requirements that it should meet in this work is the dimension down to sub-100 nm T-gate length while maintaining a high aspect ratio L_G/a, low leakage current, low gate resistance and parasitic capacitances, high breakdown voltage and good thermal stability. Moreover, a high quality gate/barrier interface is of great importance since it affects the gate leakage as well as induces gate lag effects. In order to study the influence of the gate configuration and geometry on the device performances,

transistors with different gate development, gate length and gate-to-drain distance (as illustrated earlier) were fabricated and studied. The fabrication process of the gate module is composed of two steps as shown in **Figure.2.14**. The first one consists of an e-beam lithography using PMMA-type three-layer resist followed by SiN MOCVD layer etching to define the gate foot (**Figure.2.14.a**). The second step involves the gate metallization using nickel/gold (Ni/Au) metal stack (**Figure.2.14.b**). It can be noticed that for the structures with a GaN cap passivation, the gate is deposited directly on GaN after the photolithography.

II.2.2.1. Schottky Gate Etching

Achieving sub-100 nm gate length requires the optimization of the technological process especially the SiN etching step, which is critical since it defines the gate foot. More specifically, the chosen etching technique must be optimized in order to avoid the impurities on the gate/barrier interface while maintaining short gate lengths. In order to meet these requirements, we have developed an ICP-RIE physical/chemical etching process using highly selective SF_6 plasma. This technique enables anisotropic SiN layer etching profile, which allows a short gate length to be maintained while reducing the fluorine ion implantation during the etching.

ICP etching is extremely sensitive to external conditions such as the cleanliness of the chamber or the type of support used during the etching. Before the SiN etching, the ICP chamber must be cleaned and preconditioned in order to maintain a stable etch-rate.

In order to avoid the over-etching of the resist mask and SiN MOCVD layer, we used a low RIE power etching in order to reduce the physical etching aspect thus favoring a chemical etching, which is less damaging. Moreover, an etching cycle process is carried out allowing a uniform and controlled etching thus limiting the degradation of the surface state. However, the increased number of cycles for the structures with thicker SiN MOCVD cap (10 nm) leads to an over-etching of the SiN and the resist. **Figure.2.15.a** shows the SEM top view of the opening pattern after the development of the tri-layer resists, which shows 50 nm. After 10 cycles etching step, the etched SiN MOCVD dimension becomes 80 nm, which is larger than the opening of the resist pattern while the SiN PECVD opening is about 120 nm as shown in **Figure.2.15.b** due to the higher etching rate than that of SiN MOCVD.

In addition to the over-etching of the SiN, a fluorine implantation has been observed at the gate/barrier layer interface with HRTEM analysis when using long SF_6 etching. In fact, fluorine implantation leads to the degradation of the device performances especially the gate lag effects as shown in this work [148]. This part will be discussed in the next chapter.

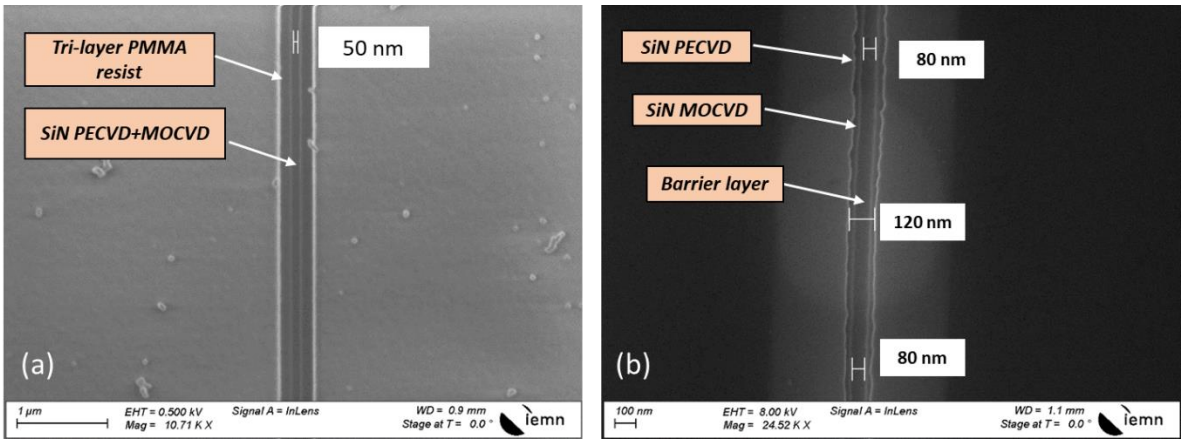


Figure.2.15. SEM image top view of the tri-layer resist pattern opening (a) and top view of SiN MOCVD and PECVD etching.

In order to avoid issues related to the SF_6 etching, we opted for an in-situ etching with the same chamber of the gate metallization using Argon (A_r) plasma, which allows:

- A reduced over-etching and thus shorter gate lengths
- More vertical SiN etching sidewalls
- High quality gate/barrier layer interface
- A reduced barrier surface damage and oxidation minimizing the gate and drain lag effects

II.2.2.2. Surface treatment and gate metallization

The Schottky contact in this work is formed using Ni/Au (20/400 nm) metal stack. Nickel metal is used because of its good adhesive properties and it ensures a reasonable Schottky barrier height while gold deposited on top improves the electrical contact. Moreover, Ni/Au metal stack allows a good Schottky contact stability, which is crucial for devices performances and reliability. A surface treatment before metallization using soft in-situ IBE A_r plasma etching is necessary (for the samples with SiN etched with SF_6 ICP plasma) in order to ensure a deoxidation of the barrier surface before Ni/Au evaporation.

T-shaped gates are used in order to reduce both the gate resistance and parasitic capacitances especially when using shorter gate length. A self-aligned gate technology consisting in reducing the gate-source distance is used in order to increase the breakdown voltage. This technological process combined with high quality ohmic contacts leads to increased F_t/F_{max} and maximum drain current thus improving the device performances. Different gate lengths varying between 80 to 500 nm have been implemented in order to study the impact on the device performances. **Figure.2.16** shows a SEM tilted image of an 80 nm Ni/Au T-gate (a) and the corresponding FIB cross section (b).

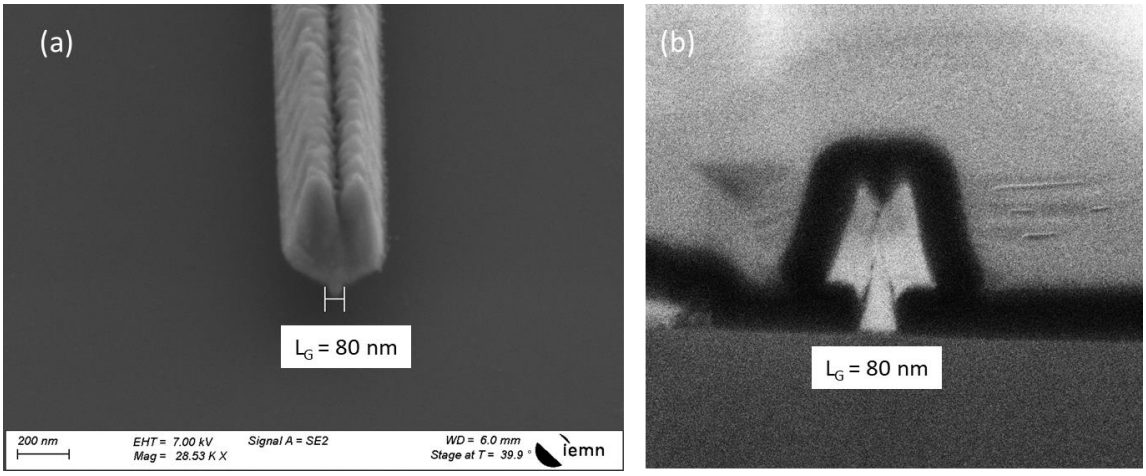


Figure.2.16. SEM tilted image of Ni/Au T-gate (a) and corresponding FIB cross section image (b)

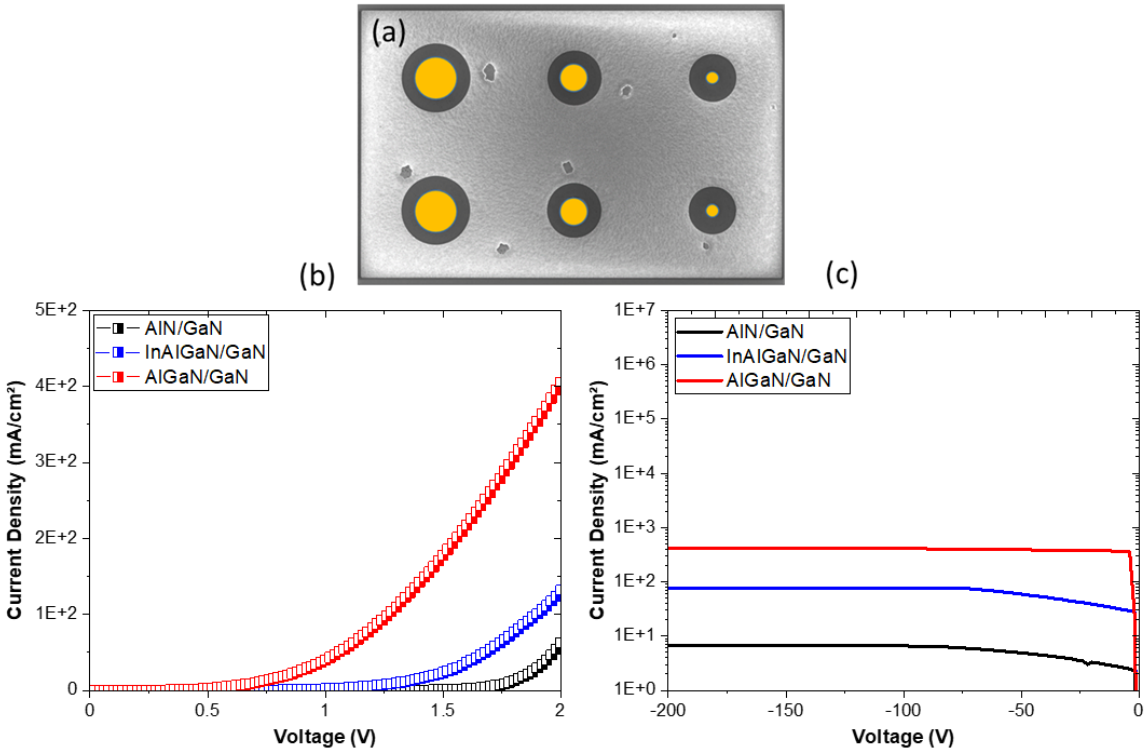


Figure.2.17. SEM image of circular diodes (a), electrical characteristics of diode-forward (b) and reverse diode (c)

After the gate formation, electrical characterizations of circular diodes are carried out in order to validate this technological step. These measurements are used to evaluate the Schottky contacts and to detect any problems that could be caused by the fabrication process. **Figure.2.17** shows 30-µm diameter diode characteristics for three structures with different barrier layer. When a positive voltage is applied to

the diode (diode-forward characteristics), the metal/semiconductor Schottky barrier is reduced, which results in an exponential increase of the current from a threshold voltage corresponding to the barrier height as shown in **Figure.2.17.b**. The threshold voltage of AlN/GaN structure (1.6V) is higher than that of InAlGaN/GaN (1V) and AlGaN/GaN (0.5V) structures due to the higher Schottky barrier height with AlN barrier layer. Electrical characteristics of the reverse diode are performed in order to detect any residues or contamination at the metal/semiconductor interface, which is reflected by the degradation of the reverse leakage current. **Figure.2.17.c** shows the leakage current of the reverse diode for the epitaxy structures.

II.3. Preindustrial device fabrication with UMS foundry within the frame of a shared process

United Monolithic Semiconductor (UMS) is a French-German company specialized in the design and fabrication of devices operating in the microwave and millimeter-wave range for wireless communication, satellite and military applications. UMS company is producing both GaAs-based and GaN-based devices.

Several GaN-based technologies developed at UMS (GH50, GH25 and GH15) have been qualified and validated for European space and defense. However, the demand is increasing for efficiency, reliability and higher frequency operation. Therefore, the optimization and the development of next generations of GaN-based industrial components is essential in order to enhance the performances and the reliability of the on-going GH10 technology from UMS. The project ALIEN is a follow-up activity of the UMS-IEMN collaboration for which a shared process of advanced heterostructures has been developed targeting transistors beyond GH10 technology. In this frame, we developed AlN/GaN RF devices on 4-inch SiC substrates. A common mask-set has been established in the first phase of the collaboration. This mask-set includes PCM devices from IEMN for internal benchmark and comparison with previous works as well as multi-finger devices using UMS designs as shown in **Figure.2.18**.

Three batches of two 4-inch wafers based on AlN/GaN have been processed. The processing for each wafer is performed as described in **Figure.2.19.** The final processed wafer is shown in **Figure.2.20**. Some solutions and various optimizations that we proposed could thus be tested in an industrial environment based on the epilayers grown by the company SOITEC. PCM measurements after IEMN front-end processing and before passives and back-end processing at UMS have been performed at IEMN. Moreover, measurements on multi-fingers devices after back-end processing at UMS have been further carried out at IEMN.

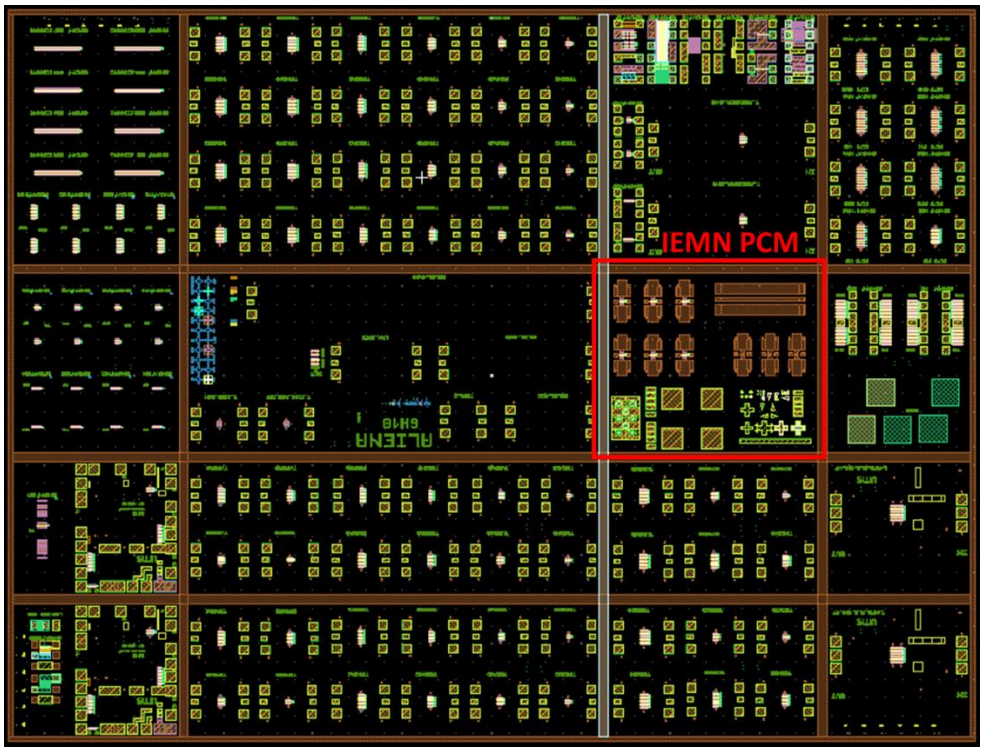


Figure.2.18. Mask set of shared UMS-IEMN process including PCM devices from IEMN (in red) and various multi-finger devices from UMS (others)

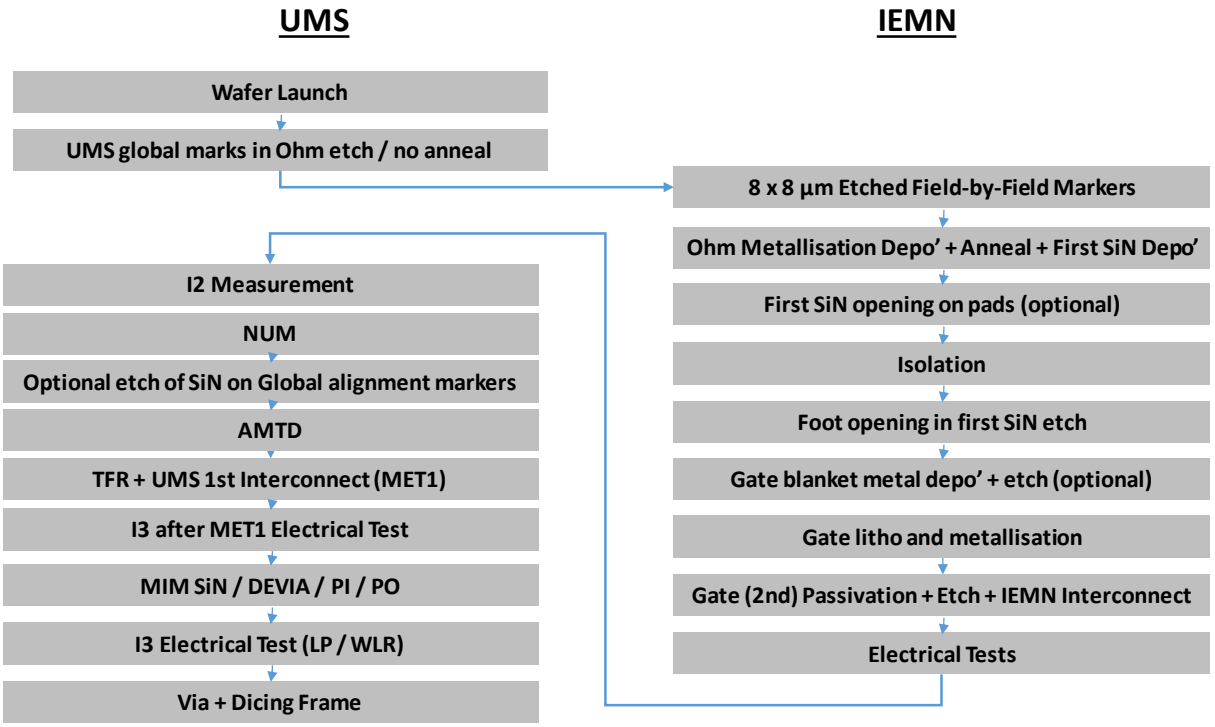


Figure.2.19. IEMN-UMS shared process flow

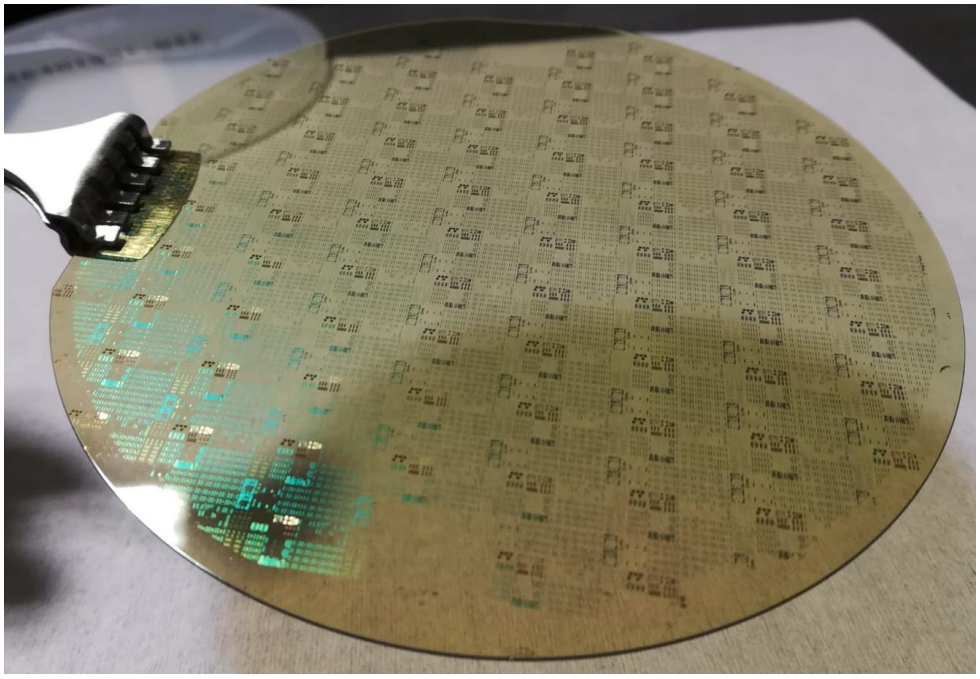


Figure.2.20. Photo of a processed wafer at IEMN

III. Device characterization methods

In order to evaluate and optimize the HEMT device performances, characterization campaigns have been carried out with a measurement protocol in order to extract the main figure of merits. These measurements have been performed by using several benches and tools available at IEMN. The transistor characterization procedure starts from the DC characterization to large signal characterization as shown in **Figure.2.21**.

Figure.2.21. Transistor characterization procedure

III.1. DC characteristics

The first step of the electrical characterization of the final transistors is the DC measurements. In this part, we describe the DC and small signal characterization methods used for the fabricated GaN HEMTs in this work. All the measurements have been carried out at IEMN characterization platform (CHOP) with

the aim of evaluating the performances of transistors and identifying undesirable effects, which can be at the origin of electrical anomalies such as short channel effects, robustness as well as trapping effects.

III.1.1. Static I-V characteristics

DC measurements are carried out with a "Keysight E5263A" Source Monitoring Unit, controlled by Keysight ICCAP software. I-V electrical measurements of a transistor are the drain current expressed as a function of the gate or drain voltages as shown in **Figure.2.22**. From these characteristics, different parameters can be extracted such as:

- $I_{D\ max}$, the maximum on-state drain current that the transistor can deliver
- $I_{D\ leak}$, the off-state drain leakage current of the transistor
- $I_{GS\ leak}$, the gate leakage of the transistor
- V_{TH}, the HEMT threshold voltage which can be extracted from the transfer characteristics $I_D(V_{GS})$
- $G_{m\ max}$, the maximum extrinsic transconductance, which is obtained from $I_D(V_{GS})$ characteristics at constant drain voltage. It is expressed by the following form:

$$G_m = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right)_{V_{DS}=Cste}$$

- DIBL (Drain Induced Barrier Lowering), which is a short channel effect referring to a negative shift of the threshold voltage V_{TH} at higher drain voltage.

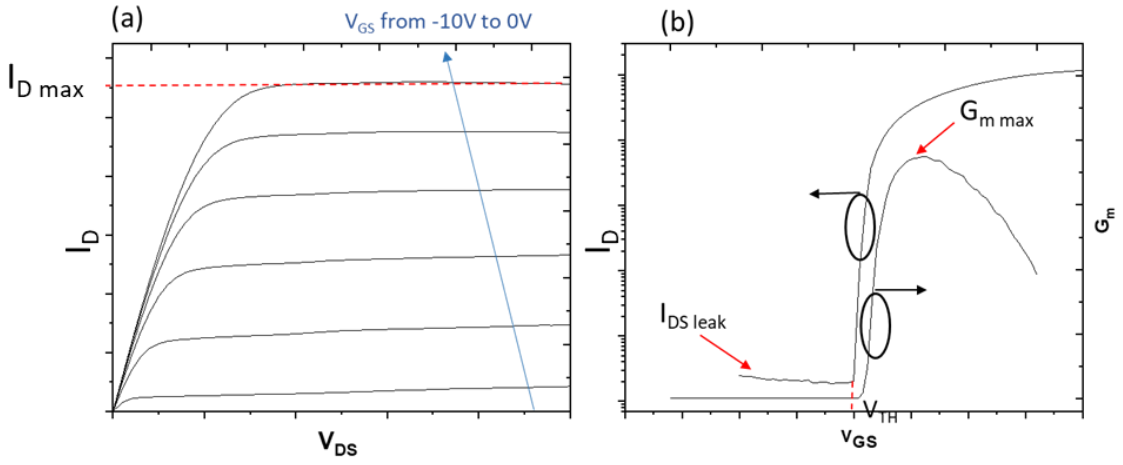


Figure.2.22. Typical $I_D(V_{DS})$ (a) and I_D-$G_m(V_{GS})$ characteristics of a GaN HEMT

The $I_D(V_{DS})$ characteristics of the HEMT (**Figure.2.22.a**) shows two operating regions: the linear region where the drain current is proportional to the drain voltage and the saturation region for which the drain current is independent of the drain voltage. The maximum drain current I_D max is extracted on the I_D-

V_{DS} plot at V_{GS} = 0V (or up to +2V for wider bandgap barrier such as AlN) and V_{DS} in saturation regime (V_{DS} = 10V in our case). Moreover, these characteristics provide indications on electron trapping through possible kink effects observed on the I_D-V_{DS} characteristic.

Figure.2.22.b shows typical I_D (V_{GS}) characteristics where we can determine the ON and OFF state drain current. The figure of merit of transistors correspond to a high I_{ON} / I_{OFF} ratio with low leakage current as needed for high power performances. The threshold voltage is extracted graphically with the tangent extrapolation method and allows us to evaluate the Schottky contact as well as the gate length scaling. Finally, plotting the G_m as a function of the gate voltage (V_{GS}) for a constant V_{DS} reveals three operating area:

- $V_{GS} < V_{TH}$ where the channel is depleted and the transistor is considered as turn-off.
- $V_{GS} > V_{TH}$, the carrier density in the channel increases with the drain current as a function of the gate voltage up to an optimum operating V_{GS} for which the transconductance is maximum.
- Beyond the gate voltage corresponding to $G_{m\,max}$, the transconductance decreases at open channel due to the thermal effect and the increase of parasitic elements with high drain voltage.

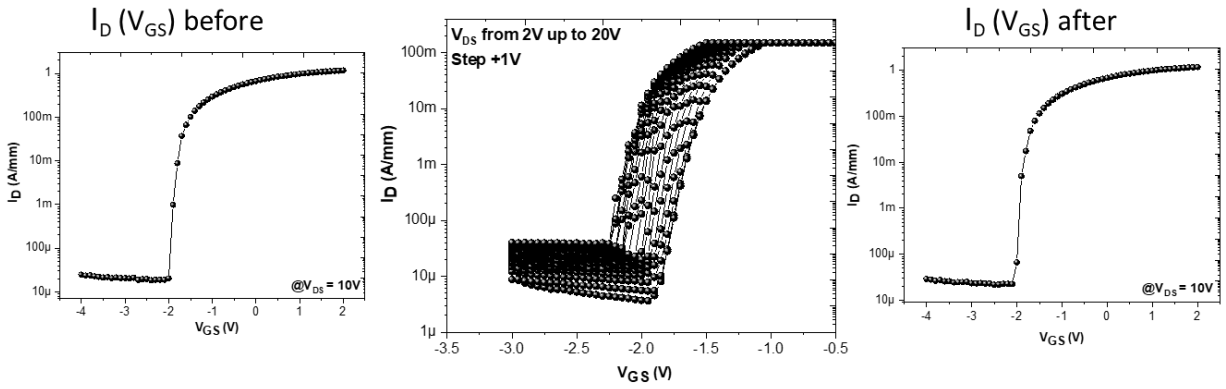


Figure.2.23. An example of semi-on robustness test with a compliance fixed at 150 mA/mm and swept from V_{DS} = 2V to 20V.

The DIBL is extracted from a so-called "semi-on robustness test", which consists in limiting the drain current at 150 mA/mm during several I_D (V_{GS}) sweeps from V_{DS} = 2V up to V_{DS} = 20V. I_D (V_{GS}) at V_{DS} = 10V are performed before and after the semi-on robustness test in order to evaluate the off-state current degradation (see **Figure.2.23**). This is a very efficient and quick test to highlight the material and processing quality as well as to define the safe operating area. The DIBL value allows us to evaluate the electron

confinement for the structure. A higher DIBL can affect the device robustness. It is expressed by the following form:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{DS}}$$

III.1.2. Pulsed I-V characteristics

Pulsed I-V measurements are carried out using different quiescent bias points in order to identify and quantify the trapping effects, which may affect the transistor performances. The gate and the drain are pulsed from quiescent bias points (V_{GQ}, V_{DQ}) corresponding to a fixed trapping in the off-state duration time (t_{off}) and then the drain current is measured in the on-state duration time (t_{on}) of the pulse as shown in **Figure.2.24**. The pulse width of the on-state duration time is chosen as small as possible (1µs) while the off-state duration time is much longer (99 µs) to prevent the self-heating effect and thus mostly investigating the trapping effect phenomena. The ratio between the pulse width and the period is known as duty cycle, which corresponds to 1%.

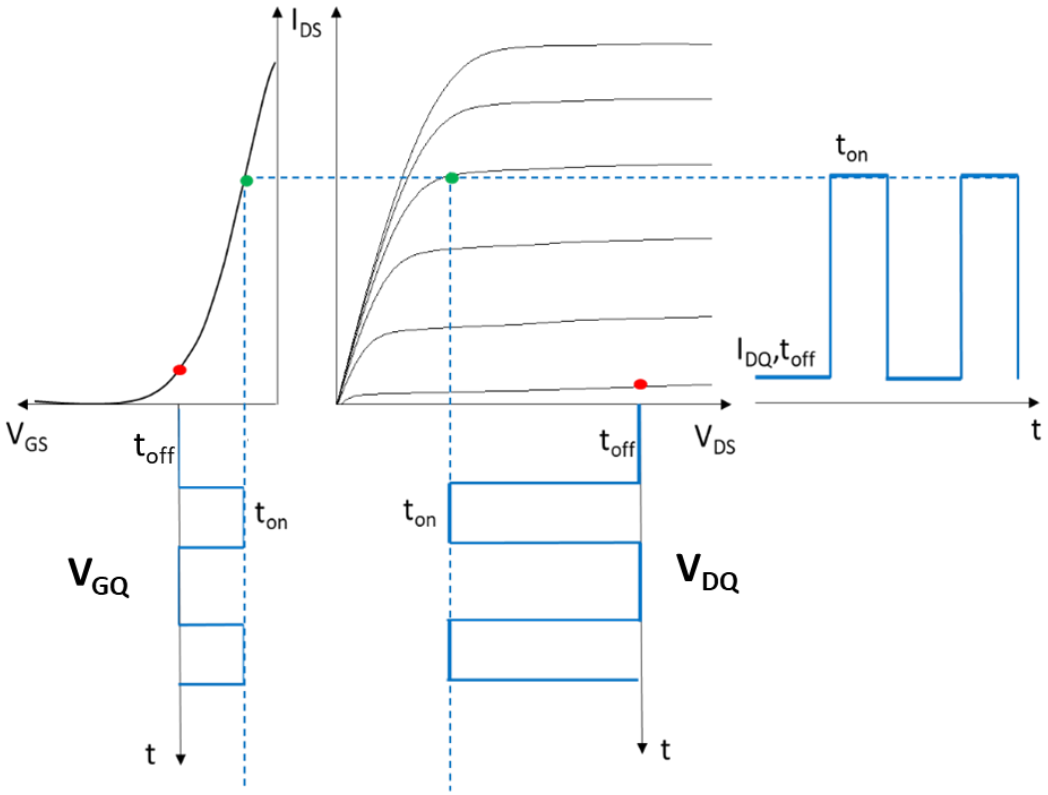


Figure.2.24. Principle of I-V pulsed measurements

Figure.2.25 shows an example of pulsed I_D (V_{DS}) characteristics and pulsed G_m. A specific trapping pulsed I-V protocol based on I-V characteristics has been settled for different bias points in order to identify the trapping effects:

- Cold point: (V_{GQ}, V_{DQ}) = (0V, 0V) which corresponds to a measurement where the self-heating effect is excluded, and the electron trapping is negligible
- Gate-lag: (V_{GQ}, V_{DQ}) = (-6V, 0V) which may favor the electron trapping under the gate region
- Drain-lag: (V_{GQ}, V_{DQ}) = (-6V, [10-25] V) which may favor the electron trapping under the gate-to-drain region

Pulsed transconductance measurements are also extracted from $I_D(V_{GS})$ characteristics in order to determine whether the electron trapping originates more from the buffer or from the surface of the transistor. Using gate and drain lag measurements, the buffer traps are highlighted by a positive threshold voltage shift while the surface traps are typically highlighted by the reduction of the maximum transconductance peak [149] as shown in **Figure.2.25.b**.

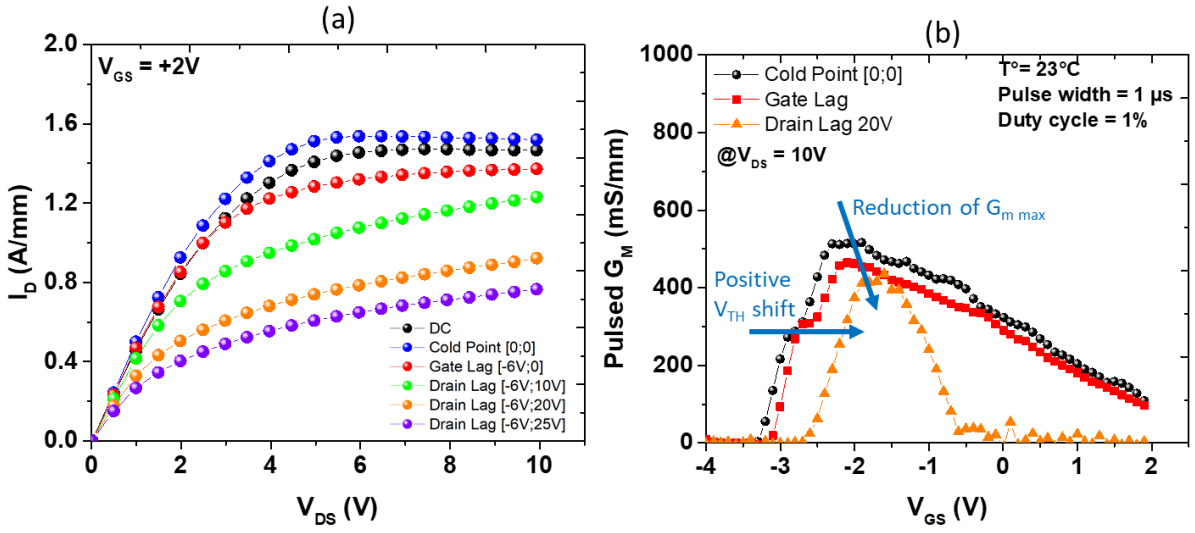


Figure.2.25. An example of pulsed I-V characteristics: (a) pulsed I_D (V_{DS}) and (b) pulsed G_m

III.2. Small signal characteristics

The extraction of a small signal equivalent circuit of fabricated GaN HEMTs were performed with an Agilent PNA-67GHz (E8361A) network analyzer from 250 MHz to 67 GHz in order to assess the device performances at high frequency. However, accuracy of device measurements depends mainly on the system calibration of the bench, which is necessary to remove systematic errors through a series of measurements.

The equivalent small signal model or linear model of HEMT is shown in **Figure.2.26**. It is composed of two types of parameter:

- The extrinsic parameters: which corresponds to the parasitic elements resulting from the access lines and metallization. It includes the pad capacitances C_{PG}, C_{PD} and C_{PGD}, the pad inductances L_G, L_D and L_S, and the gate and access resistances R_G, R_D, and R_S.
- The intrinsic parameters: include gate-to-source, gate-to-drain, and drain-to-source capacitances (C_{GS}, C_{GD}, and C_{DS}), and drain-to-source resistance R_{DS}, which are bias dependent.

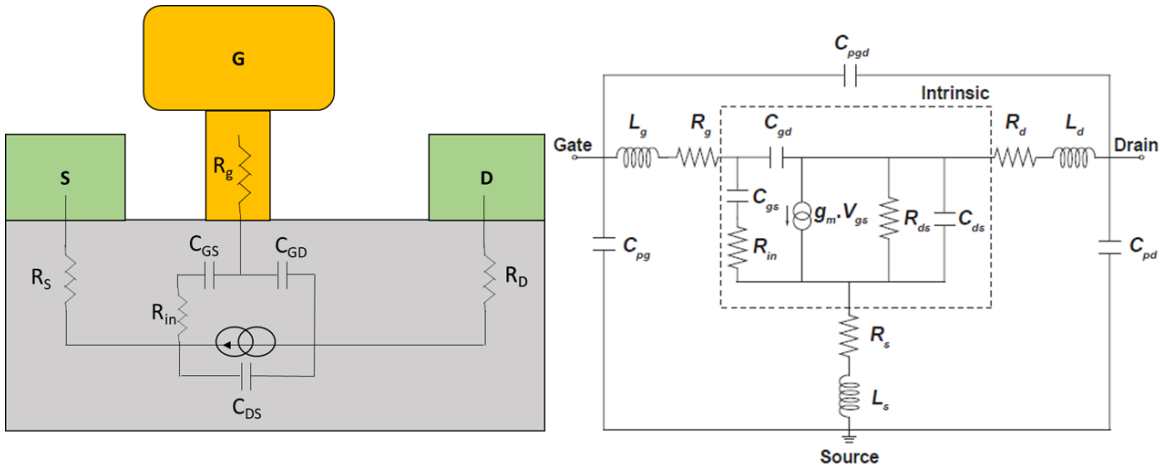


Figure.2.26. Small signal equivalent circuit model of GaN HEMTs

GaN HEMT high frequency performances are usually evaluated using two small signal figures of merit: the current gain cutoff frequency F_t and the maximum oscillation frequency F_{max}. The optimum gate polarization V_{GS} corresponds to the maximum transconductance $G_{m\ max}$ while the drain voltage V_{DS} is increased from 10V up to 25V to evaluate the maximum oscillation frequency F_{max} of the transistor.

In order to extract f_t and f_{max}, the current gain H_{21} and the unilateral power gain U are calculated using the following equations:

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$$

$$U = \frac{1}{2}\frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{k\frac{S_{21}}{S_{12}}-Re\left(\frac{S_{21}}{S_{12}}\right)}$$

The transition frequency is the cutoff frequency F_t of the current gain. It is defined at the frequency where the current gain $|H_{21}|$ is equal to 0 dB. It is expressed as a function of the transconductance and the intrinsic characteristics of the equivalent circuit model:

$$F_t = \frac{G_m}{2\pi(C_{GS} + C_{GD})}$$

F_{max} is an important figure of merit to assess the potentialities for high frequency transistor operation. It is defined as the frequency where the unilateral power gain U becomes 0 dB. f_{max} is expressed as a function of the cutoff frequency, intrinsic and extrinsic characteristics of the circuit model:

$$F_{max} = \frac{F_t}{2\left(R_g + R_{ds}\right)^{1/2}}$$

The cutoff frequency F_t and the maximum oscillation frequency F_{max} are extracted by extrapolation using a slope of -20 dB/decade method. The cutoff frequency F_t is the intercept of the -20dB/decade tangent with the unity (0 dB) of current gain H_{21} while the maximum oscillation frequency is the intercept of the -20dB/decade tangent with the unity of power gain U as shown in **Figure.2.27**.

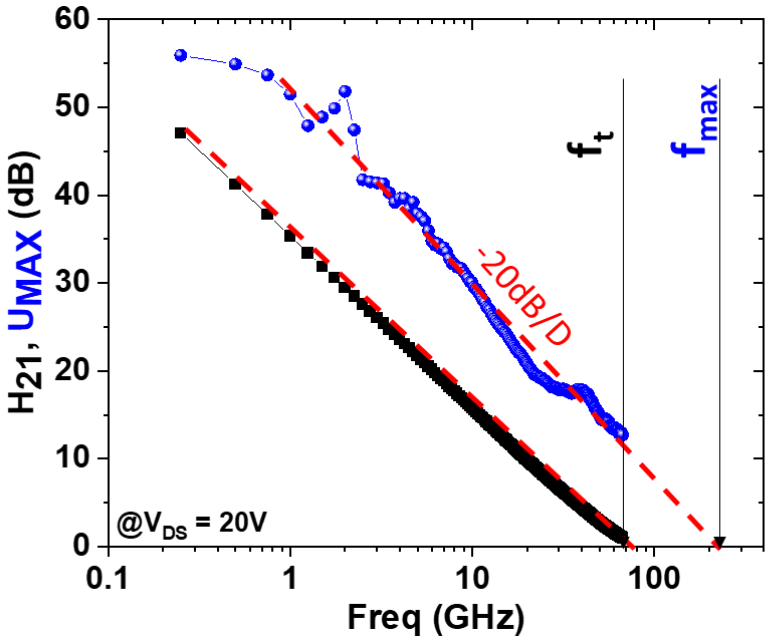


Figure.2.27. An example of U and H_{21} curves used for the extraction of f_t and f_{max}

III.3. Large signal characteristics

GaN technology has been recognized as a potential solution to satisfy RF applications where the combination of output power density and PAE is a key figure of merit to assess the device performances. Besides the technology challenges, a proper non-linear characterization of the transistors is a crucial step to extract the full potential of this emerging wide-band gap technology. Actually, the non-linear power device characterization is not easy to establish because of the losses, signal stability and measurement time. An active load-pull measurement bench has been developed in order to perform "Load-Pull" measurements up to 40 GHz in both CW and pulsed mode in the framework of a PhD thesis from our research group in 2016 [150]. In order to assess the device performances at higher frequency up to W-band, we developed an active load-pull large signal characterization bench at 94 GHz. **Figure.2.28** shows an example of large signal characteristics measured at 40 GHz.

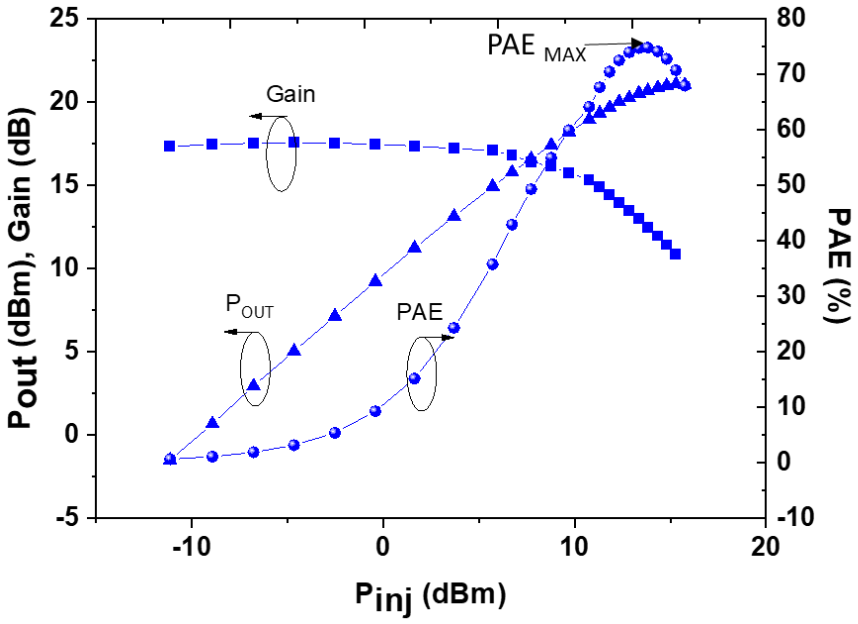


Figure.2.28. Large signal characteristics showing the PAE, the Output power density and the power gain at 40 GHz

In order to evaluate the RF transistor performances at a particular frequency, there are three main figures of merit:

- **The output power density P_{OUT}**: which is the power density delivered by a transistor usually expressed in W/mm to compare the performance of a transistor regardless of its size. The transistor power density is evaluated through the saturated power P_{SAT} (the maximum power delivered by the transistor) and various compression points, which allows quantifying the linear behavior of the transistor.

- **The power gain G_P**: the transistor performances are characterized by the gain, which defines the capability to amplify an RF signal. A high gain contributes to high power density and PAE. It is given by the following form:

$$G_P = P_{RFOUT} - P_{RFIN}$$

- **The power added efficiency (PAE)**: PAE represents the ratio between the power gain and the dissipated power P_{DC}. A high PAE reduces the self-heating of the component and limits the energy consumption required by specific applications. It is given by:

$$PAE = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}}$$

III.3.1. Large signal characterization at 40 GHz

The NVNA setup uses a Nonlinear Vectorial Network Analyzer (Keysight N5245A-NVNA), allowing power measurements up to 40 GHz in both CW and pulsed mode. **Figure.2.29** shows the power bench that has been optimized and the associated synoptic. The NVNA setup contains the following elements:

- Non-linear Vector Network Analyzer Keysight N5245A-NVNA
- 40 GHz Power Signal Generator (Agilent E8257D)
- Two 6-18 GHz amplifiers delivering 10W (CTT)
- Two 40-44 GHz amplifiers delivering 2W and 5W (Bonn Elektronik)
- A 40 GHz amplifier delivering up to 12W (TTi)
- A "Source Monitoring Unit" (SMU) delivering the DC power to the device under test (DUT) in CW mode (Agilent E5263A)
- Two pulse generators provide the DC power to the DUT in pulsed mode (HP-8110A & HP-8114A)
- Oscilloscope with voltage and current probes measures the voltage and current applied to the DUT in pulsed mode (Tektronix DPO7104)

Load-pull measurements are defined by the implementation of load impedances at the output of the transistor in order to determine the optimum load ($\neq 50\ \Omega$) and thus reaching the optimum power or PAE matching. This adaptation is also necessary in order to avoid instability or oscillation issues, which lead to the transistor degradation. The measurement consists initially in biasing the transistor in the desired operating class. Power is then injected at the transistor input in order to reach the saturation. At the same time, the load impedance is applied at the transistor output allowing power or PAE matching. During the load-pull measurements, the gate leakage current is monitored to ensure the integrity of the transistor.

Three solutions exist for load-pull measurements: passive, active, and hybrid load-pull. The choice of the large signal characterization method in this work was focused on the active load-pull. An active load-pull has the advantage to reach high value for the module Γ_L that are required especially when using small transistor size that generally generates high reflection coefficient.

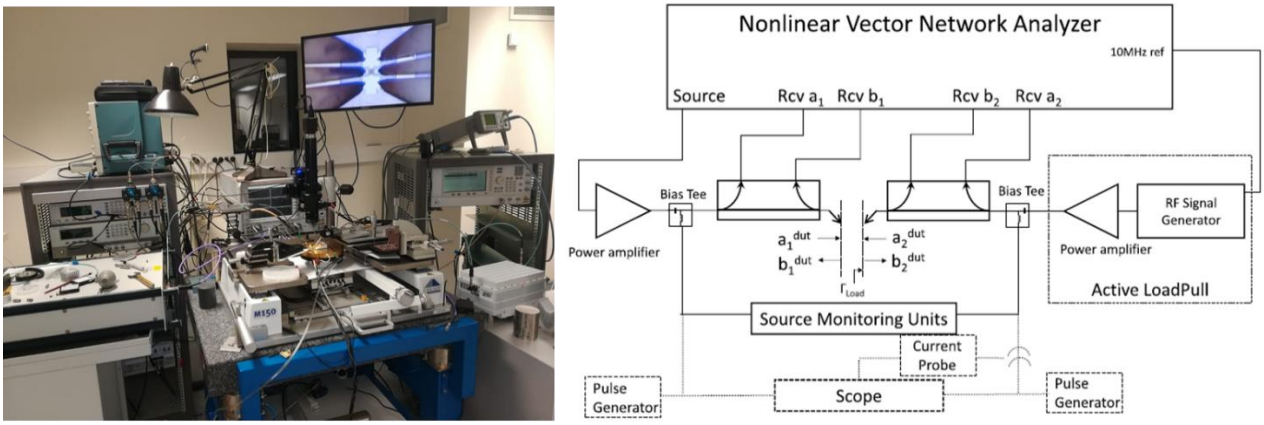


Figure.2.29. Image of the load-pull bench at 40 GHz and its optimized synoptic [150]

Load-pull measurements are performed using two excitations mode: Continuous Wave (CW) and pulsed mode. CW mode is the common way to perform nonlinear characterizations for most of the applications and it consists in a polarization of the transistor continuously throughout the measurements. On the other hand, in pulsed mode, the polarization bias is pulsed with a pulse width of 1 µs and a duty cycle of 1%. This type of unique measurement at such high frequency allows the investigation of trapping effects in operational conditions while highlighting the full potential of the devices by eliminating the trapping and thermal effects.

The load-pull measurements are carried out using several V_{DS} in CW and pulsed mode at a fixed drain current. The gate current I_G is monitored during the load-pull sweep as a function of the drain voltage V_{DS}. The degradation of the gate current (I_G > 100 µA/mm) reflects the device failure at the applied drain voltage.

The comparison between the CW and pulsed mode allows the evaluation of the trapping and thermal effects. However, it is mandatory to keep the same measurements conditions for both operation modes. One of the figure of merits of our transistors is to reach high efficiency; that is why, a deep class AB has been chosen to favor the PAE. The polarization point and the optimum load (Γ_{load}) presented at the transistor output are also chosen to achieve the maximum PAE. It can be noticed that, the optimal load is

not necessarily the same for both CW and pulsed mode. Indeed, the S parameters of a transistor in CW and pulsed mode may differ depending on the impact of trapping and thermal effects.

The transistors may present an instability area at 40 GHz on the smith chart, which can be determined using S-parameters and Keysight-ADS tool (Advanced Design System). This step is necessary before load-pull measurement in order to avoid any oscillation or degradation of the transistor.

III.3.2. Short term reliability at 40 GHz

Short-term on wafer RF step stress at 40 GHz are carried out using various drain voltage and temperature in order to assess the short-term device reliability in operational conditions. The transistors are monitored during 24 hours by steps of 8 hours under large signal conditions at 40 GHz and at peak PAE. Before each stress test sequence (8h, 16h and 24h), the gate voltage is adjusted in order to maintain the drain current at 100 mA/mm, which corresponds to the initial drain current before the auto-polarization. DC characteristics are then performed after each stress test to monitor the drain leakage current. The reliability test is carried out in two steps: the transistor is first monitored for 24 hours using different drain bias at room temperature. Afterwards, the robustness of the transistor is verified at higher temperatures by increasing the base-plate temperature (T_{bp}) up to 140°C.

III.3.3 Test bench development for large signal characterization at 94 GHz

III.3.3.1. Passive load-pull characterization

In the framework of this thesis, measurements at 94 GHz in CW condition were carried out using an existing passive load-pull bench at IEMN. The results showed a state-of-the art power density with an AlN/GaN technology that will be discussed in chapter 3. **Figure.2.30** shows a synoptic of the passive load-pull at 94 GHz, which contains the following elements:

- Vectorial Network Analyzer (Rohde&Schwarz ZVA24)
- A 6X frequency multiplier (Spacek, 12.5-18.3GHz to 75-100GHz)
- A manual continuously variable attenuator (75-110GHz / WR10 waveguide)
- Power amplifier (Farran, 88-96GHz, +30dBm output power)
- A dual directional coupler (Sage Millimeter, 75-110GHz / WR10 waveguide, 20dB coupling)
- A specific millimeter-wave converter designed by RPG-Radiometer Physics GmbH for IEMN
- A “Source Monitoring Unit” (SMU) delivering the DC power to the device under test (DUT) in CW mode
- An impedance tuner (Maury MT979A01, 75-110GHz / WR10 waveguide)

- A power-meter (Agilent W8486A , 75-110GHz / WR10)

The input signal from the VNA is sent at 15.6667GHz to a frequency multiplier (x6) and amplified at 94 GHz. The manual continuously variable attenuator is used to adjust the input power.

The incident (a_1) and reflected (b_1) waves are measured through the dual-directional coupler at the input of the DUT. Coupled signals are sent to a specific millimeter-wave converter developed by RPG-Radiometer Physics GmbH for IEMN. This converter is similar to a standard converter used for S-parameter measurements without signal generation except the fact that we just use the frequency down-conversion capability.

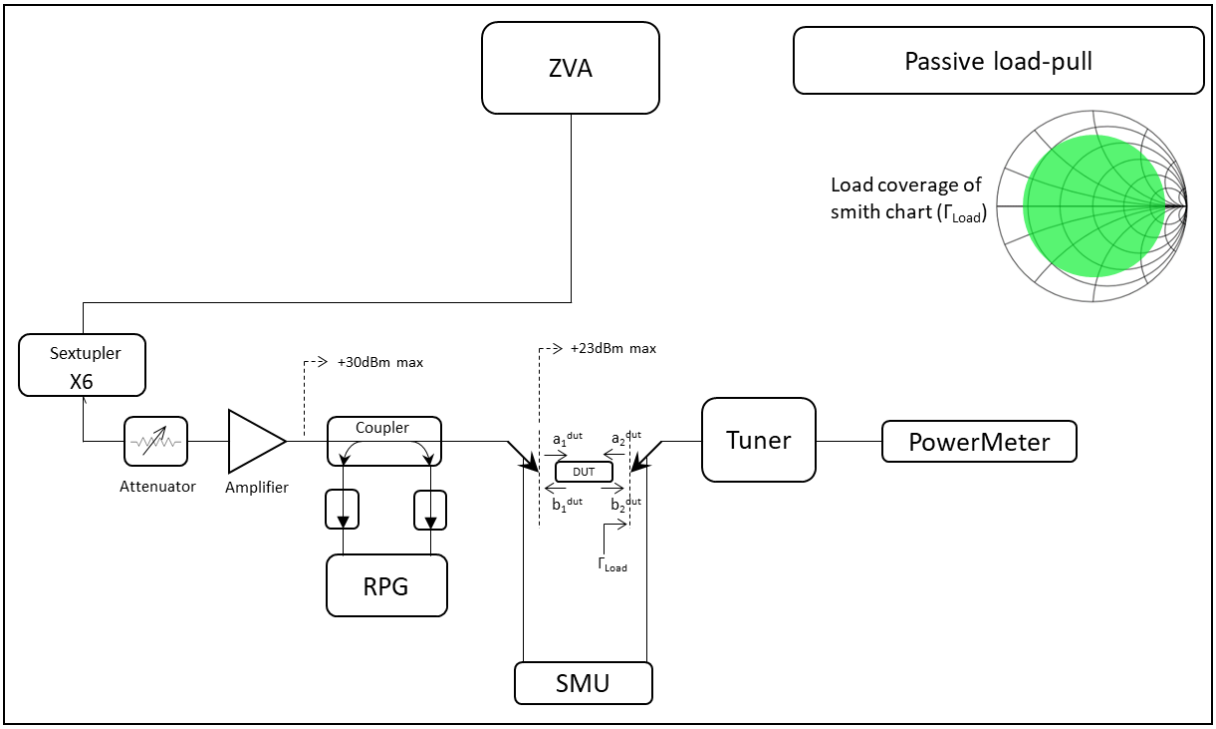


Figure.2.30. synoptic of the passive load-pull bench at 94 GHz

Passive load-pull requires an impedance tuner to control the load impedance at the DUT's output. The tuner is connected to the output of the DUT by a waveguide coplanar GSG probe. The part of the signal b_2 transmitted through the tuner is measured with the power-meter. The previously measured S-parameters of the tuner allow calculating $b_{2\,DUT}$ and then $a_{2\,DUT}$.

The main advantages of this technique are the stability and fastness. Tuners are able to produce reflection coefficient near to 1 with a phase control from 0 to 360° corresponding to the full Smith chart. However, the main limitation of this technique is the losses due to the additional elements inserted between

the tuner and the DUT's output. These losses lead to the reduction of the maximum achievable reflection coefficient at the DUT's level, which results in a lower Γ_{load} maximum magnitude of 0.7 compared to the maximum reachable Γ_{load} (see the smith chart in **Figure.2.30**). The few reports of W-band measurement systems using passive tuners also suffer from this limitation presenting maximum achievable Γ_{load} of 0.5 and 0.7 magnitude [151]–[154]. In addition to the losses, passive tuner characteristics may exhibit a variation due to the external conditions (such as the variation of the ambient temperature), which affects the tuner parameters leading to measurement errors. As a result, a regular tuner calibration is mandatory.

The challenge in this work was to optimize the passive load-pull bench to allow measurements using active load-pull technique in CW and pulsed mode. This represents a scientific added value for the characterization of GaN HEMTs in W-band, which is not demonstrated so far in the literature.

III.3.3.2. Active load-pull characterization

The active load-pull have been developed at IEMN by Etienne OKADA engineer at characterization platform. The System uses also a Vectorial Network Analyzer (Rohde&Schwarz ZVA24) with 2 specific millimeter-wave converters designed by RPG-Radiometer Physics GmbH for IEMN, allowing vectorial measurements at 94 GHz at the input and output. **Figure.2.31** shows the active load-pull bench that has been optimized and the associated synoptic. The active load-pull setup contains the following elements:

- Vectorial Network Analyzer (Rohde&Schwarz ZVA24)
- A 6x frequency multiplier (Spacek, 12.5-18.3GHz to 75-100GHz)
- Power amplifier (MC2 Technologies, 90-100GHz, +20dBm output power) AMP1
- 3dB coupler to split the signal for both input and output (for Load-Pull)
- A "Source Monitoring Unit" (SMU) delivering the DC power to the device under test (DUT) in CW mode

Input setup:

- Programmable continuously variable attenuator (MiWave, 75-110GHz / WR10 waveguide, 0-70dB) ATT1
- Power amplifier (Farran, 88-96GHz, +30dBm output power) AMP2
- Dual-directional Coupler (Sage Millimeter, 75-110GHz / WR10 waveguide, 20dB coupling)
- Specific millimeter-wave converter designed by RPG-Radiometer Physics GmbH for IEMN

Output setup:

- Programmable continuously variable attenuator (MiWave, 75-110GHz, 0-70dB) ATT2
- Programmable Phase shifter, which has been developed based on the previously used impedance tuner and a waveguide circulator.
- Power amplifier (Quinstar Technology, +37dBm output power at 94 GHz, specifically developed for IEMN) AMP3
- Circulator and 50Ω load integrated in the amplifier.
- Dual-directional Coupler (Sage Millimeter, 75-110GHz / WR10 waveguide, 20dB coupling)
- Specific millimeter-wave converter designed by RPG-Radiometer Physics GmbH for IEMN

Active load-pull configuration does not require a tuner, but an output signal controlled in magnitude and phase injected to the DUT's output to generate Γ_{load}. This method has a number of advantages that overcome the limitation of passive tuner. Load reflection coefficients Γ_{load} superior to 0.95 in magnitude can be reached at 94 GHz while providing a nearly full coverage of the smith chart (see **Figure.2.31**).

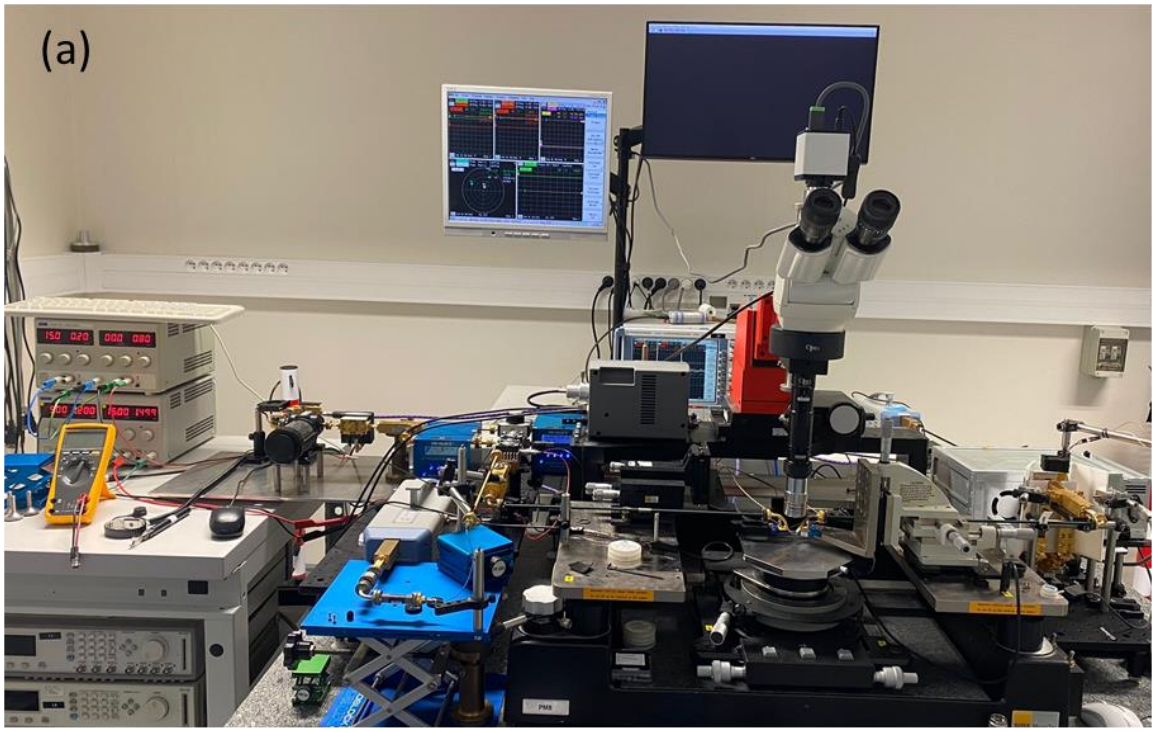


Figure.2.31. Image of the 94 GHz active load-pull power bench

Figure.2.32 shows the synoptic of the 94 GHz active load-pull. The input (a_1 and b_1) and output (a_2 and b_2) waves are measured through two dual-directional couplers at the input and the output of the DUT. Coupled ways are connected to specific millimeter-wave converters. The input signal from the VNA is sent at 15.6667GHz to a frequency multiplier (x6) and amplified at 94 GHz with AMP1. The signal is then

divided in two signals (signal 1 and 2). The input signal 1 is amplified with AMP2 in order to reach enough power to saturate the transistor. The programmable attenuator (ATT1) is used to adjust the input power.

The main optimization of this bench is the output setup implementation, which is used to create a signal (a_2) delivered to the DUT's output to produce the desired reflection coefficient (Γ_{load} = a2/b2). The magnitude and phase of this signal must be controlled in real-time via a programmable attenuator (ATT2) and a programmable phase shifter (PS). This load-pull technique requires a software to adjust the parameters of the signal in real-time because a2 must follow b2 to maintain a constant $\Gamma_{load.}$.

It can be noticed that for the 40 GHz active load-pull, the output signal delivered to the DUT's output is generated by a RF signal generator which is not used in the case of the 94 GHz active load-pull in order to avoid the phase divergence at higher frequencies between the RF signal generator and the input source.

This technique of active load-pull presents several advantages such as operating at high frequencies, W-band in this case but easily frequency scalable. The achievable reflection coefficient is only limited by the maximum power level delivered by AMP3. The use of a high-power amplifier can overcome this limitation. However, it can be pointed out that most of the elements of the bench are expensive.

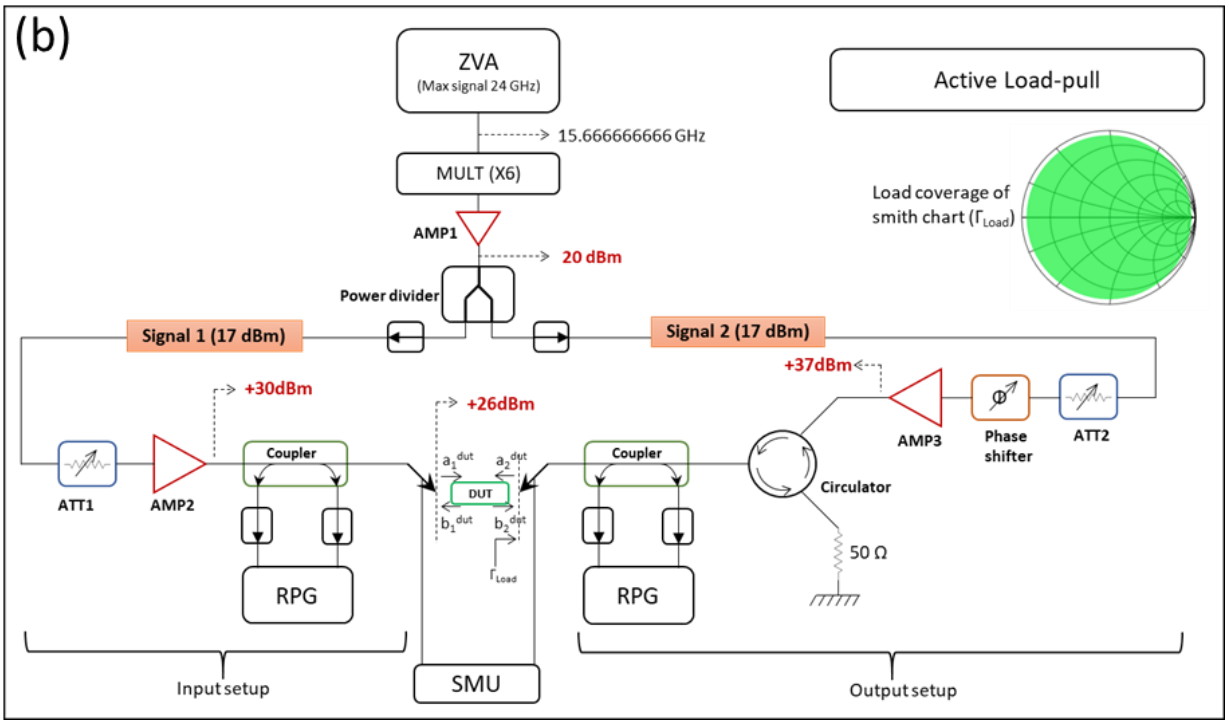


Figure.2.32. Synoptic of the 94 GHz active load-pull power bench

III.3.3.3. Nonlinear measurement method

i. Calibration

Prior to the power measurement, a mandatory ZVA calibration is performed in two steps: the power calibration and the on-wafer vector calibration. To measure the absolute power, an amplitude calibration needs to be performed using a waveguide power-meter, which cannot be connected directly to the coplanar probe. Thus, the power calibration has been performed just behind the dual-directional coupler. To perform an on-wafer power calibration, the losses from the calibration point and the probe level needs to be taken into account by determining the S-Parameters of this part of the setup including the coplanar probe and a waveguide section.

1) S-Parameter determination of the section to de-embedding for power calibration:

To determine the S parameters of the guide/coplanar section separating the connection point of the power-meter (x in **Figure.2.33**) and the DUT, we use a function of *FormFactor's WinCal* software called "Second tier". We start by performing a full-1port calibration on the ZVA in the power-meter connection plan from the waveguide structure. After reconnecting the guide/coplanar section, we carry out the measurements of the Open, Short and Load standards of an ISS (Impedance Standard Substrate from FormFactor) with the *WinCal* software corrected by the waveguide calibration previously performed. From these measurements, *WinCal* is able to provide with the S parameters of the block separating the calibration and measurement points in the form of an S2p file. This file will be used on the ZVA for power calibration.

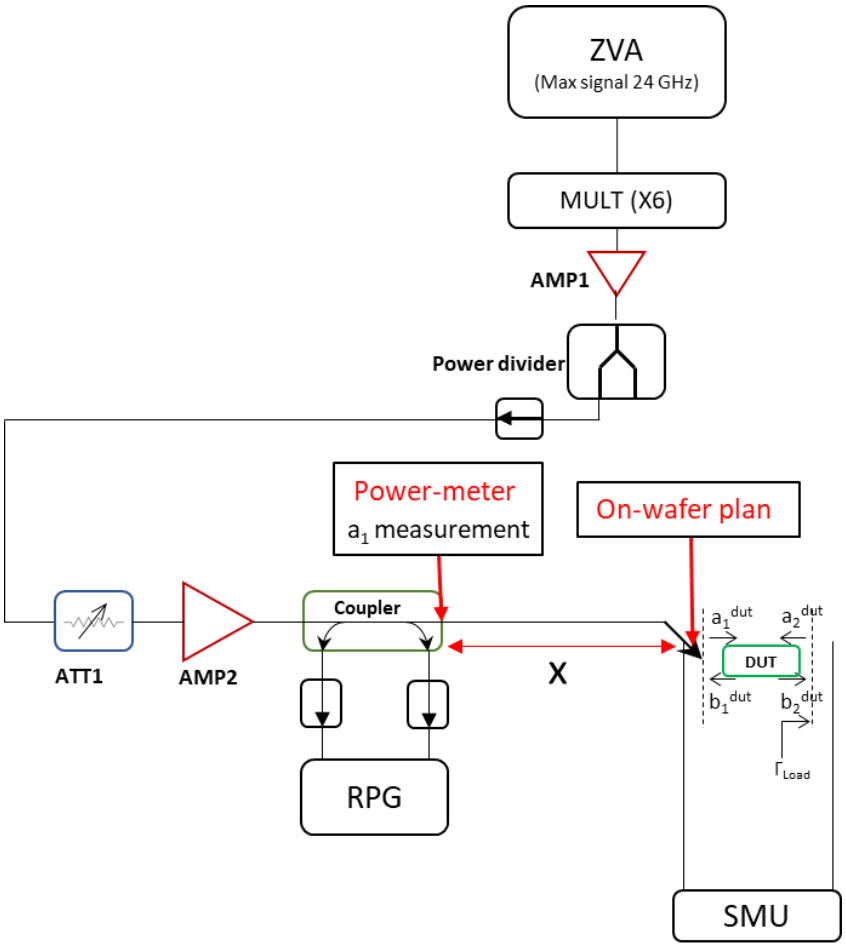


Figure.2.33. ZVA bench setup for power calibration

1) Power calibration:

To perform the power calibration, a waveguide power-meter connected to the output of the dual-directional coupler is used as shown in **Figure.2.33**. The ZVA enables to take into account additional losses if the power-meter is not directly connected to the desired calibration plan. We use this function to include the S-parameters of the section determined in the previous step. Thus, we can perform the power calibration in the "on-wafer" plan with a waveguide power-meter. The procedure is performed on the ZVA. A signal is generated with the input setup, acquired by the ZVA via the RPG millimeter-wave converter as well as the acquisition of the real power measured by the power-meter. The difference gives the scalar error of the measurement. This error, reduced by the losses characterized in the previous step, makes possible to obtain a calibrated measurement of the magnitude of the on-wafer a1 wave.

2) On-wafer vector calibration:

To be able to measure the four waves (a_1, b_1, a_2 and b_2) calibrated in amplitude and phase, we must first perform a full-2ports "on-wafer" S_{ij} calibration. We use the "LRRM" (Line Reflect Reflect Match) procedure and FormFactor ISS via WinCal software as shown in **Figure.2.34**. This procedure is considered at IEMN as the most accurate for "on-wafer" measurements at such frequency. The ZVA has a function called "Enhanced wave correction" that allows to correct the magnitude and phase measurement of the four waves using a 2-port vector calibration and an absolute calibration on one of the waves. As a result, we are able to carry out the calibrated measurements in amplitude and phase of the waves (a_1, b_1, a_2 and $b_{2)}$ at the wafer level.

ii. Continuous wave mode measurement

DC supply is provided by the SMUs through bias-T integrated in the coplanar probes. The RF excitation, which is also constantly injected, is supplied by the ZVA and frequency multiplier through the amplifier to ensure the saturation of the transistors. A 94 GHz signal is injected at the DUT input and its power level is increased step-by-step up to the DUT's saturation. At each point the active load-pull system is automatically tuned, owing to a programmable attenuator and phase shifter in order to keep constant the impedance presented to the DUT. Once saturation is reached, we analyze the device performance and start a new power sweep with a new impedance to find a potential better one for the DUT. This procedure is reiterated until the optimum impedance is found.

First measurement has been carried out on this bench using high performances HBT technology, which shows the expected performances from these devices. Measurements of our transistors at 94 GHz have been planned on this active load-pull bench.

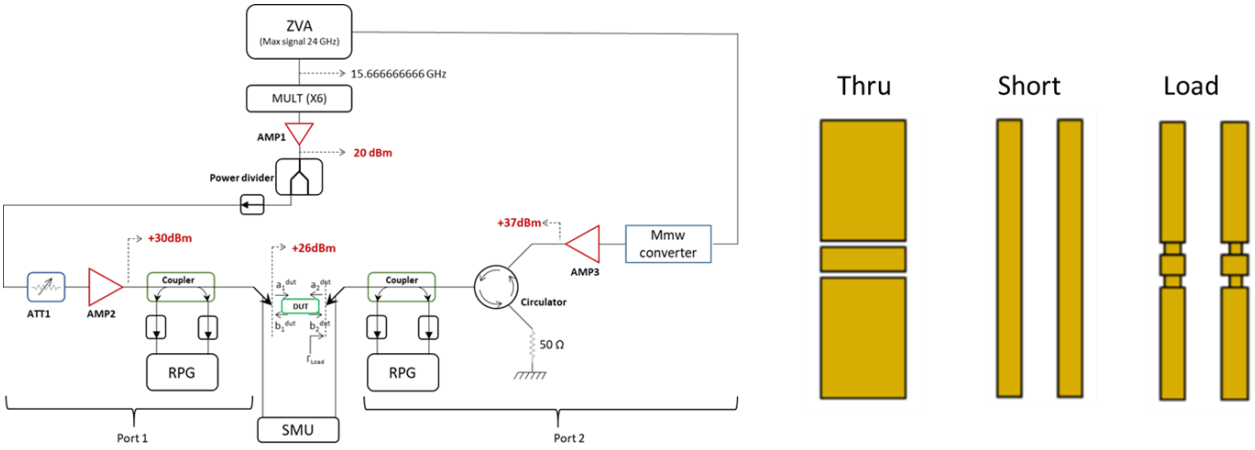


Figure.2.34. ZVA bench setup for vector calibration

IV. Conclusion

The demonstration of high performances GaN technology operating at high frequency requires not only the optimization of the epitaxial structures but also the device processing and characterizations. In this chapter, we described the fabrication process of GaN HEMTs operating at high frequency as well as the device characterization tools, which are used with a measurement protocol established in this framework at IEMN.

We first described the mask sets used and the device processing development. In order to enhance the device performances, the optimizations of the fabrication process is necessary, in particular the ohmic contacts and the gate module. Indeed, a reliable ohmic contact process with low contact resistances (R_c) is crucial for high frequency performances of scaled devices. On the other hand, the gate module for high frequency operation is a critical step. We developed a process allowing sub-100 nm gate lengths while maintaining a low leakage current, a low gate resistance and parasitic capacitances. Afterwards, preindustrial device fabrication with UMS foundry within the frame of a shared process has been presented.

Finally, we described the bench and methods used for small and large signal characterizations. The characterization campaigns carried out at IEMN with a measurement protocol are detailed including DC, pulsed, small and large signal characterizations. Two load-pull benches at different frequencies (active LP @40 GHz and passive LP @94 GHz) are used for the characterization of transistors. Finally, an active load-pull bench development for large signal characterization at 94 GHz is discussed.

In the next chapters, we will describe the electrical and structural characterization results of the different devices fabricated in this framework.

Chapter 3: Towards ultrathin Al-rich barrier layers for millimeter-wave devices: Electrical and structural characterization of AlN/GaN HEMTs

I. Introduction

Several studies have been carried out in this work with the aim of optimizing GaN-based devices in terms of performances, reliability as well as operating frequency up to W-band. In this chapter, we present the electrical and structural characterizations of the fabricated transistors in the frame of different studies. The measurement campaigns using various characterization tools (described in chapter 2) were performed on the final transistor at IEMN. Additional device reliability measurements have been carried out at the University of PADOVA. The structural characterizations are realized on both epitaxial structures and transistors by our partners from C2N and ILV laboratories. A shared processing of advanced heterostructures with UMS foundry has been performed targeting high performances in the millimeter-wave range. **Figure.3.1** shows the structure of the studies performed in this work indicating the different steps of the transistor's realization and characterization.

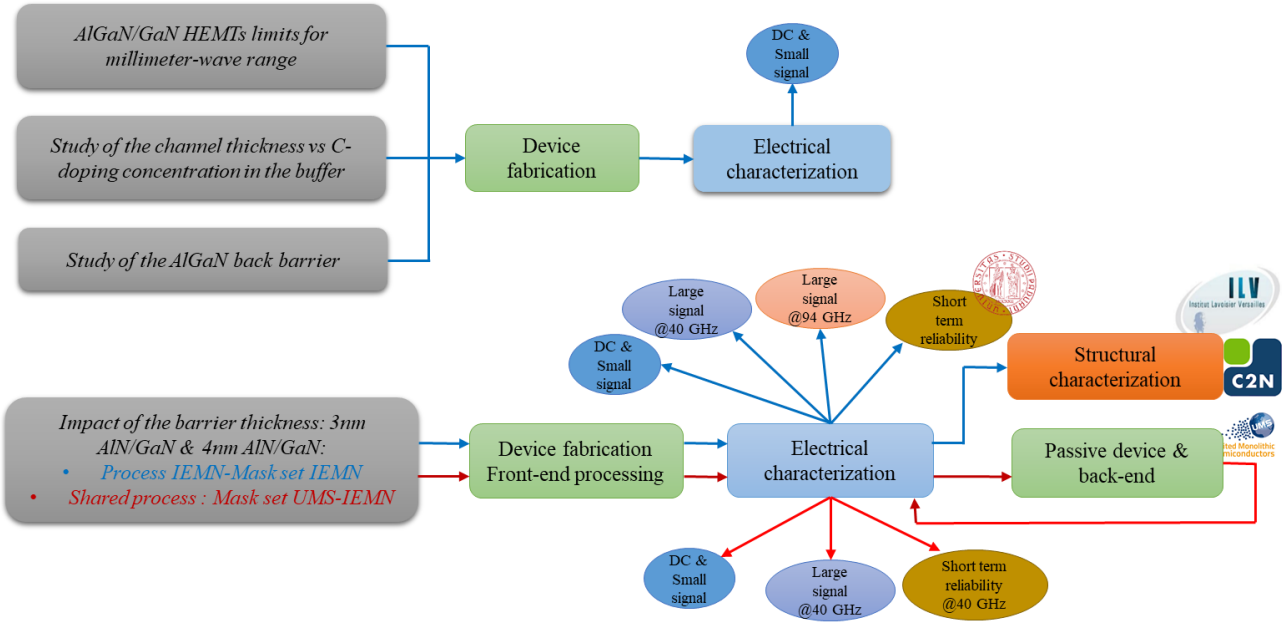


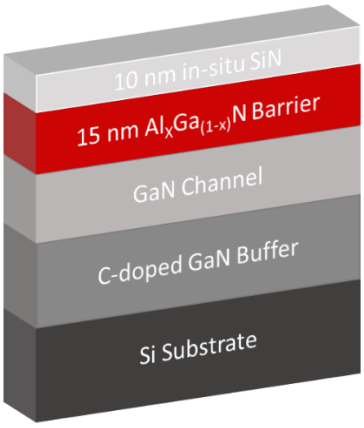
Figure.3.1. Structure of the different studies

II. AlGaN/GaN HEMTs limits in the millimeter-wave range

AlGaN/GaN based HEMTs is the most mature technology, which demonstrated outstanding power performances in the microwave range. However, at high frequency, it is difficult to improve the performances of AlGaN/GaN HEMTs as they are severely limited by short channel effects. The device scaling for high frequency requires short gate lengths along with the barrier thickness reduction while maintaining a high polarization. This is actually difficult to achieve with AlGaN barrier layers. The

following study was performed in order to understand and highlight the limitations of AlGaN barrier layer in the frame of transistor's scaling.

The structure shown in **Figure.3.2** was defined in order to evaluate the impact of the Al-content into the barrier layer on DC performances. The heterostructure was grown by MOCVD on Si substrate by SOITEC. It consists in a C-doped GaN buffer,UID GaN channel, followed by 15 nm AlGaN barrier layer with Al-concentration varying from 10% to 40%. Finally, the structure was capped with a 10 nm in-situ SiN cap layer. The electrical properties extracted by Hall Effect measurements are shown in **Figure.3.2** as a function of the Al-content. The 2DEG density increases as expected from 1.5 x 10^{12} cm^{-2} with low Al-content (10%) AlGaN barrier to about 1.5×10^{13} cm^{-2} for high Al-content (40%) AlGaN barrier. Moreover, despite a decrease of the sheet resistance, the electron mobility degrades with the increase of Al-content indicating a material crystal quality degradation.



Electrical properties / Al-content	n_s (cm^{-2})	μ (cm^2.V/s)	R_{sheet} (Ω/sq)
10%	1.5 x 10^{12}	1200	3230
20%	6.4 x 10^{12}	2000	470
30%	1.1 x 10^{13}	1750	320
40%	1.5 x 10^{13}	1200	320

Figure.3.2. Schematic cross section of an AlGaN/GaN structure grown on Si substrate and associated 2DEG electrical properties for different Al-content

II.1. Device fabrication

This study has been carried out using the optical mask-set "GaN TEST" in order to simplify the fabrication process and evaluate the epitaxial structures through DC characterizations. The source-drain ohmic contacts were formed by etching the in-situ SiN layer with SF_6 ICP and partially etching the AlGaN barrier layer with Cl_2A_r ICP prior to the metallization. A Ti/Al/Ni/Au metal stack annealed at 775°C has been used to obtain a contact resistance of 0.4 Ω.mm. Then, Ti/Au gates of 3 µm length were defined by optical lithography. The SiN underneath the gate was fully removed by SF_6 plasma using ICP etching. Finally, 200 nm PECVD SiN layer was deposited as final passivation. **Figure.3.3** shows the SEM image of gates with different gate-to-drain distances.

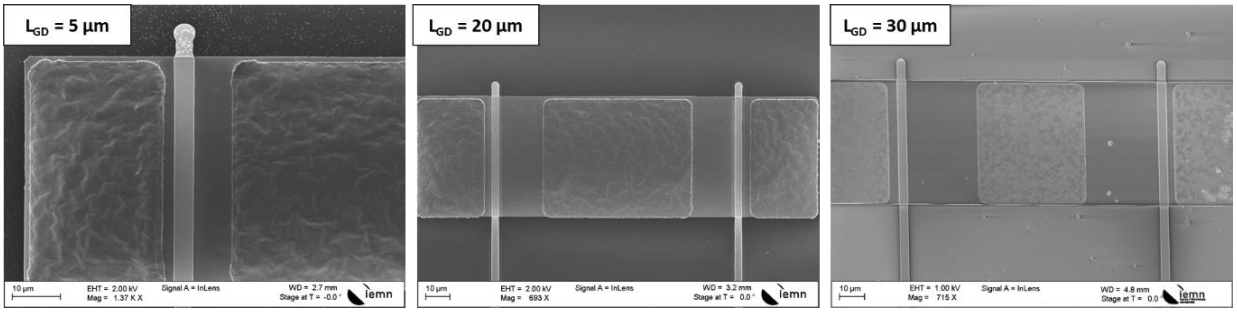


Figure.3.3. SEM image of the gates with different gate-to-drain distances (5, 20 and 30 µm)

II.2. DC and small signal characterization

Transfer characteristics of 2×50 µm transistors with L_G = 3 µm and L_{GD} = 5 µm on the structures with Al-content varying from 10% to 40% are shown in **Figure.3.4**. The maximum drain current increases as expected with the Al-content from 0.08 A/mm to 0.9 A/mm as a higher Al-content into the AlGaN barrier leads to an increase of the 2DEG density (as seen from Hall measurements) and thus higher current density. However, while increasing the Al-content we observed an expected shift of the pinch voltage but also an increase in the off-state leakage current up to10 mA/mm with 40% Al-content as shown in **Figure.3.5**. This can be explained by the higher dislocation density due to the lattice mismatch between the GaN and the AlGaN barrier with high Al-content.

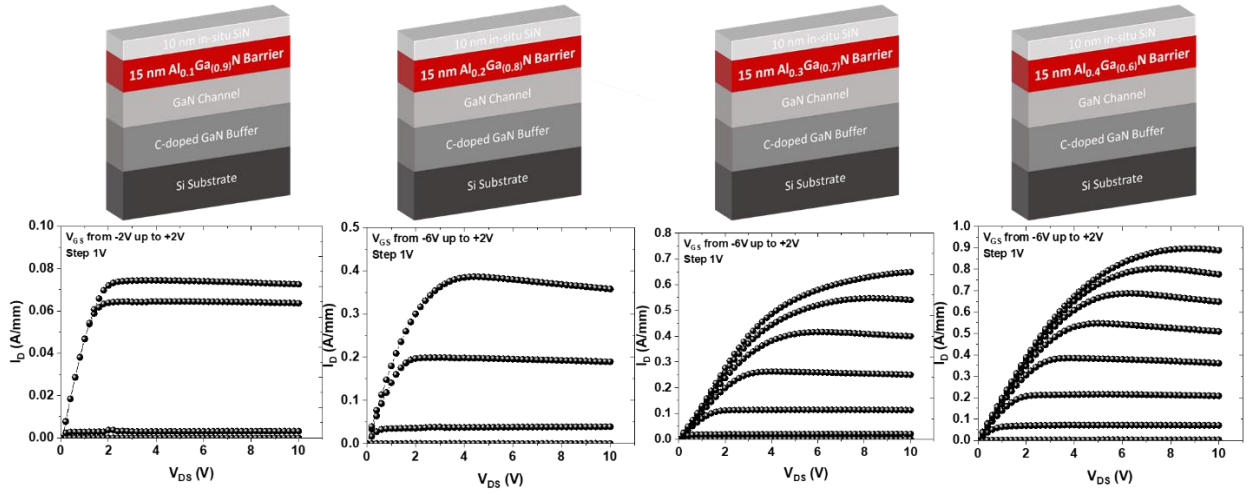


Figure.3.4. Transfer characteristics of 2×50 µm with L_G = 3 µm and L_{GD} = 5 µm of the structures with Al-content varying from 10% to 40%

Three-terminal breakdown voltage has been carried out on a 2×50 µm transistors with different gate-to-drain distances from L_{GD} = 10 µm to L_{GD} = 30 µm on each sample. As expected, the breakdown voltage scales well as a function of L_{GD} for each structure (see **Figure.3.6**). We observed also that the drain

leakage current increases with the Al-content into the AlGaN barrier layer up to 1mA/mm with 40% Al-content. The enhanced gate leakage current has been properly correlated to the dislocations by C-AFM measurements from Fraunhofer institute (IISB). They demonstrated the large impact of dislocations into the AlGaN barrier on the gate leakage current, especially if such dislocations are located near the drain side of the gate edge [155].

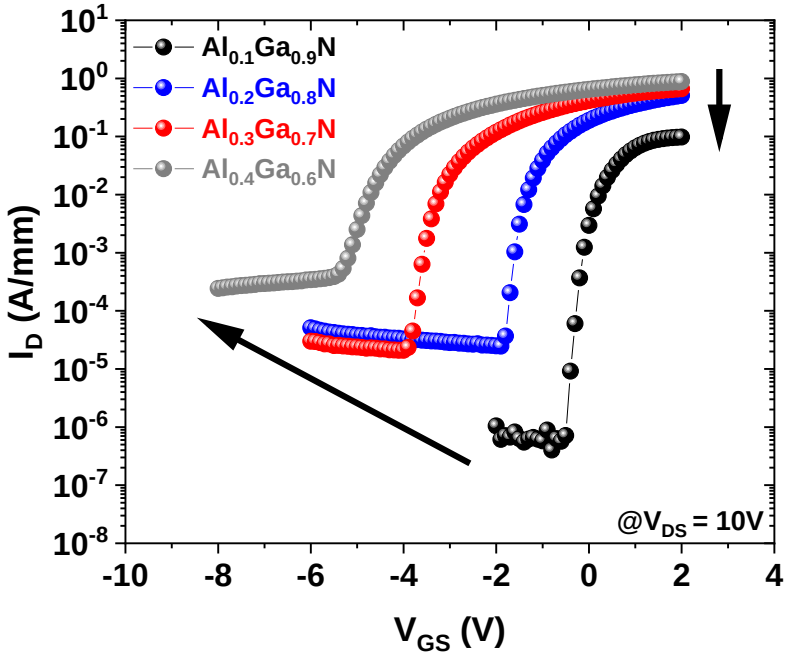


Figure.3.5. Output characteristics of 2×50 µm transistor with L_{GD} = 5 µm of the AlGaN/GaN structure with different Al-content

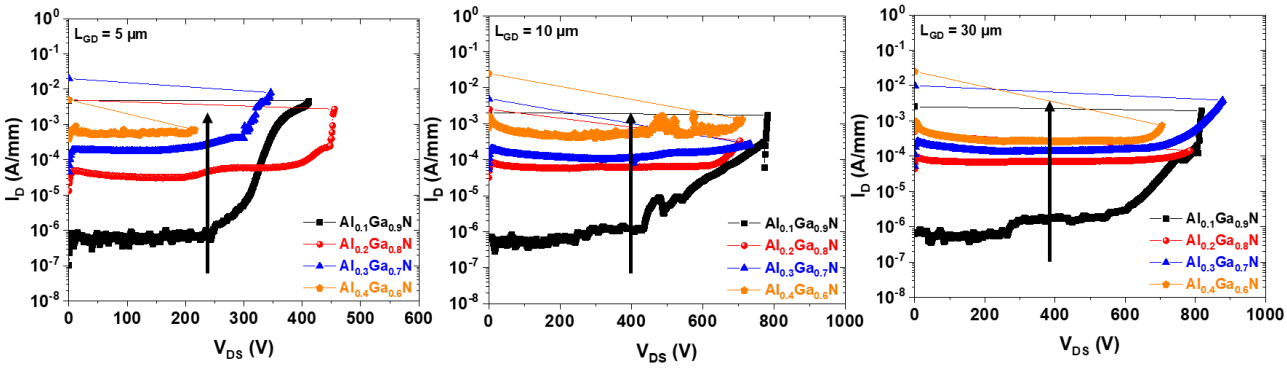


Figure.3.6. Three-terminal breakdown voltage of 2×50 µm with different L_{GD} of 5, 10 and 30 µm of the AlGaN/GaN structures with various Al-content

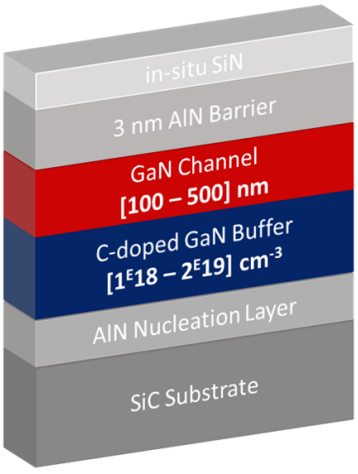
That is why; the Al-content of standard AlGaN barrier layers is kept between 20% and 30% associated with a sufficiently thick barrier layer needed to generate enough electrons. This prevents the downscaling of AlGaN barriers that cannot meet the requirements of millimeter-wave devices. On the other hand, ultrathin AlN or InAlGaN barriers are preferable materials for millimeter-wave range in order to avoid gate recess, which is known to degrade the device reliability [156]. The thickness and alloy composition are key parameters to mechanical strain and piezoelectric polarization, defining also the 2DEG density.

III. Ultrathin AlN/GaN technology

III.1. Impact of the channel thickness and C-doping concentration in the buffer

The epitaxial structures shown in **Figure.3.7.a** have been provided by SOITEC and consist in an AlN nucleation layer to accommodate the lattice mismatch between the buffer and the substrate. The variation of C-doping GaN buffer from 2×10^{19} down to 1×10^{18} cm^{-3} followed by a channel thickness varying from 100 to 500 nm are used for this study in order to evaluate the impact on deep trapping effects within the buffer as well as the short channel effects. A 3 nm AlN ultrathin barrier layer is used to benefit from both a high polarization and a high aspect ratio L_G/a. Finally, the structures were capped by 6 nm in-situ SiN layer to passivate the surface states.

(a)



(b)

C-doping buffer concentration \ Channel thickness	100 nm GaN	150 nm GaN	250 nm GaN	500 nm GaN
2^E19 cm^{-3}	**STRUCTURE A** N_s= 2x10^{13} cm^{-2} μ= 900 cm^2/V.s R_{sheet}= 340 Ω/sq	**STRUCTURE B** N_s= 2x10^{13} cm^{-2} μ= 895 cm^2/V.s R_{sheet}= 330 Ω/sq	**STRUCTURE C** N_s= 2.1x10^{13} cm^{-2} μ= 910 cm^2/V.s R_{sheet}= 320 Ω/sq	**STRUCTURE D** N_s= 2.1x10^{13} cm^{-2} μ= 905 cm^2/V.s R_{sheet}= 310 Ω/sq
9^E18 cm^{-3}		**STRUCTURE E** N_s= 2.1x10^{13} cm^{-2} μ= 950 cm^2/V.s R_{sheet}= 300 Ω/sq		
5^E18 cm^{-3}	**STRUCTURE F** N_s= 2x10^{13} cm^{-2} μ= 870 cm^2/V.s R_{sheet}= 330 Ω/sq		**STRUCTURE G** N_s= 2.1x10^{13} cm^{-2} μ= 950 cm^2/V.s R_{sheet}= 310 Ω/sq	**STRUCTURE H** N_s= 2x10^{13} cm^{-2} μ= 1000 cm^2/V.s R_{sheet}= 300 Ω/sq
1^E18 cm^{-3}	**STRUCTURE I** N_s= 2x10^{13} cm^{-2} μ= 830 cm^2/V.s R_{sheet}= 350 Ω/sq			

Figure.3.7. Schematic cross section of the epitaxial structure with C-doping concentration in the buffer varying from $2x10^{19}$ down to $1x10^{18}$ cm^{-3} and the channel thickness varying from 100 to 500 nm and the associated 2DEG properties measured by Hall Effect.

These HEMT epitaxial structures served as a starting point for the optimization of the device design targeting higher frequency of operation. The purpose is to optimize the C-doped concentration into the GaN buffer together with the GaN channel thickness with respect to the trade-off between deep level traps and proper electron confinement under high electric field. **Figure.3.7.b** shows the studied structures resulting in a matrix of C-doping concentration and channel thickness variations. The electrical properties of the heterostructures were characterized using Hall measurements at room temperature. Similar 2DEG concentration $n_s \sim 2\times10^{13}$ cm^{-2} associated with a mobility around $\mu \sim 950$ cm^2/V.s and a sheet resistance $R_{Sheet} \sim 325$ Ω/□ have been measured on the different structures. These values confirm the uniformity and reproducibility of the epitaxial structures, despite the sub-5 nm AlN barrier layer. Such a high quality is due to a large extent to the SiN cap layer, which enables to prevent the stress relaxation of the hetero-interface AlN/GaN during the growth.

III.1.1. Device fabrication

The fabrication process has been carried out using the e-beam mask-set "GaN Fast". Similar process has been applied on all structures for proper comparison. A Ti/Al/Ni/Au metal stack annealed at 850°C has been used to form source-drain ohmic contacts directly on top of the AlN barrier by etching the in-situ SiN layer. The contact resistance extracted by TLM method is about 0.4 Ω.mm for most of the structures. However, some of them have a contact resistance of about 0.8 Ω.mm due to the non-optimized Argon etching before metallization. Ti/Au T-gates were defined by e-beam lithography. The SiN underneath the gate was fully removed using an SF_6 plasma etching through the e-beam lithography. **Figure.3.8** shows various gate lengths varying from 500 nm to 100 nm enabling to evaluate the impact of the gate length (e.g. electric field) on the electron confinement. Finally, 200 nm PECVD SiN layer was deposited as final passivation.

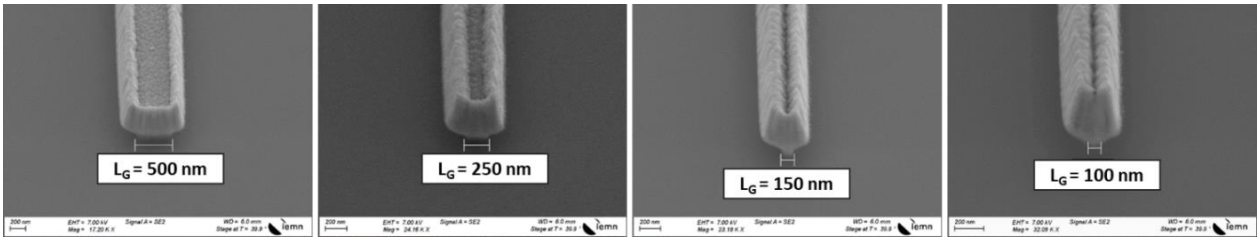


Figure.3.8. SEM image of different gate lengths

III.1.2. Impact of the undoped channel thickness variation

The first evaluation was performed by varying the channel thickness from 100 to 500 nm while maintaining the carbon concentration of the buffer at 2×10^{19} cm^{-3} as shown in **Figure.3.9**.

Channel thickness / C-doping buffer concentration	100 nm GaN	150 nm GaN	250 nm GaN	500 nm GaN
2^E19 cm^{-3}	**STRUCTURE A** N_s= 2x10^{13} cm^{-2} µ= 900 cm^2/V.s R_{sheet}= 340 Ω/sq	**STRUCTURE B** N_s= 2x10^{13} cm^{-2} µ= 895 cm^2/V.s R_{sheet}= 330 Ω/sq	**STRUCTURE C** N_s= 2.1x10^{13} cm^{-2} µ= 910 cm^2/V.s R_{sheet}= 320 Ω/sq	**STRUCTURE D** N_s= 2.1x10^{13} cm^{-2} µ= 905 cm^2/V.s R_{sheet}= 310 Ω/sq

Figure.3.9. Channel variation from 100 to 500 nm associated to a carbon concentration of 2×10^{19} cm^{-3}

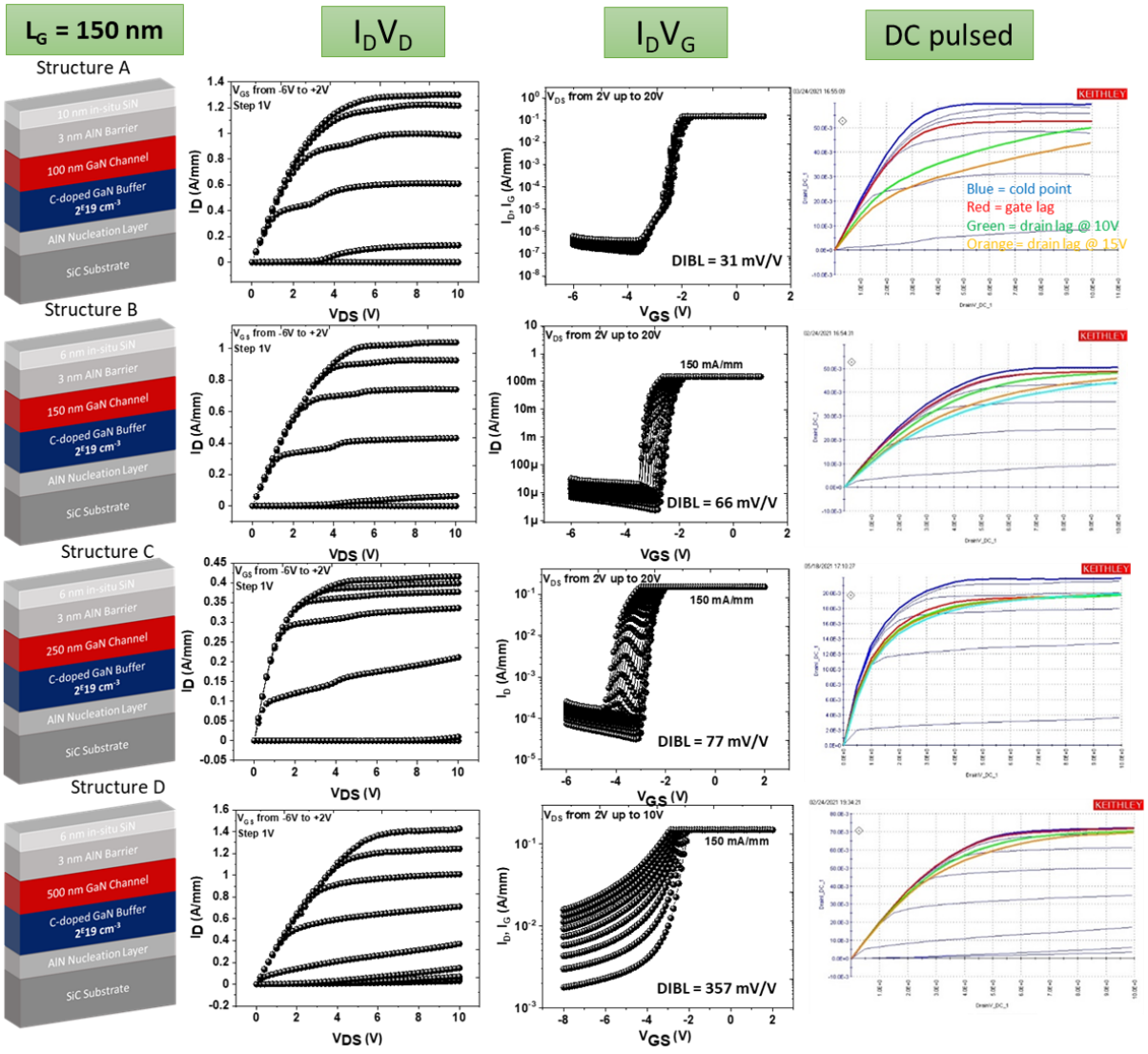


Figure.3.10. Transfer characteristics I_D (V_{DS}), semi-on robustness tests and DC pulsed characteristics of the structures with a channel thickness variation

1) DC and small signal characterization

Transfer characteristics, semi-on robustness tests and DC pulsed measurements of the different structures used for the channel thickness variation study (Structure A, B, C and D) are shown in **Figure.3.10**. 2×50 µm transistors with gate-to-drain distance L_{GD} of 1.5 µm and a gate length L_G of 150 nm show a maximum drain current $I_{D\,max}$ of 1.3, 1 and 1.4 A/mm for the structure A, B and D while the structure D shows 0.4 A/mm due to the non-optimized and poor ohmic contacts. Nevertheless, the transfer characteristics reveal that the increase of the channel thickness leads to reduced kink effects (which is directly related to the trapping effects). Indeed, trapping effects are reduced with the increase of the channel thickness as shown on the DC pulsed characteristics. However, a severe degradation of the electron confinement is observed on the semi-on robustness tests through the DIBL parameter, which strongly increases from 31 mV/V for the structure A to 357 mV/V for the structure D. Also, we observed a systematic degradation of the off-state leakage current at higher drain voltage, impacting the transistor robustness. Therefore, these analyses confirm the clear trade-off between trapping effects and the electron confinement under high electric field. It can be noticed that other gate lengths were measured in order to evaluate the impact on the electron confinement with the associated channel thickness. The whole results are summarized in the next section (**Figure.3.11**).

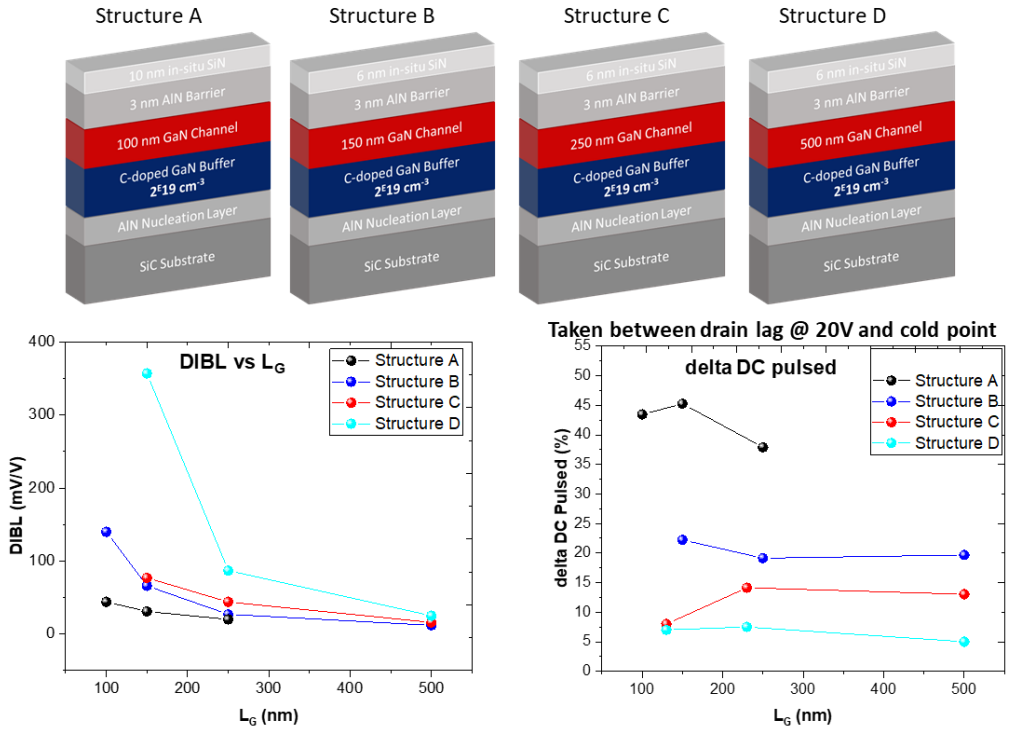


Figure.3.11. DIBL (left) and delta DC pulsed taken between drain lag at V_{DS}=20V and cold point (right) as a function of different gate length of the structures for the channel thickness variation

2) Results comparison:

Figure.3.11 shows the DIBL and delta DC pulsed taken between the drain lag at V_{DS} = 20V and the cold point as a function of the gate length for each structure. The trapping effects are significantly reduced when using thicker channel thickness but inversely a degradation of the electron confinement is observed which is highlighted by the increasing of the DIBL parameter. We also observed that the use of shorter gate lengths leads to a strong degradation of the electron confinement especially with thicker channel. Therefore, from this investigation, it can be concluded that an undoped channel thickness between 100 and 150 nm should be used with sub-150 nm gate lengths.

III.1.3. Impact of the Carbon-doped variation in the buffer

This evaluation deals with the variation of the Carbon-doped concentration into the buffer from 2×10^{19} cm^{-3} to 1×10^{18} cm^{-3} while maintaining a channel thickness of 100 nm for optimum electron confinement as shown in **Figure.3.12**.

C-doping buffer concentration / Channel thickness	2^E19 cm^{-3}	5^E18 cm^{-3}	1^E18 cm^{-3}
100 nm GaN	**STRUCTURE A** N_s= 2x10^{13} cm^{-2} µ= 900 cm^2/V.s R_{sheet}= 340 Ω/sq	**STRUCTURE F** N_s= 2x10^{13} cm^{-2} µ= 870 cm^2/V.s R_{sheet}= 330 Ω/sq	**STRUCTURE I** N_s= 2x10^{13} cm^{-2} µ= 830 cm^2/V.s R_{sheet}= 350 Ω/sq

Figure.3.12. Carbon-doped variation from 2×10^{19} cm^{-3} to 1×10^{18} cm^{-3} with an undoped GaN channel thickness of 100 nm

1) DC and small signal characterization

A comparison between the transfer characteristics, semi-on robustness tests and DC pulsed characteristics of the structures A, F and I is shown in **Figure.3.13**. 2×50 µm transistors with gate-to-drain distance L_{GD} of 1.5 µm and a gate length L_G of 100 nm show a maximum drain current $I_{D\,max}$ of 1.2 A/mm, for the structure A and 1.4 A/mm for the structure F and J. We have significantly reduced the concentration of carbon in the buffer from 2×10^{19} cm^{-3} for the structure A to 1×10^{18} cm^{-3} for the structure I. We observed that the decrease in carbon concentration reduces the kink effect on I_D (V_{DS}) characteristics, which indicates reduced trapping effects for the transistors as confirmed from the DC pulsed characteristics. These analyzes demonstrate that one of the main origins of trapping effects is the high carbon concentration into the buffer.

In contrast, we observed a degradation of the electron confinement associated with a huge increase in the drain leakage current as a function of the drain bias.

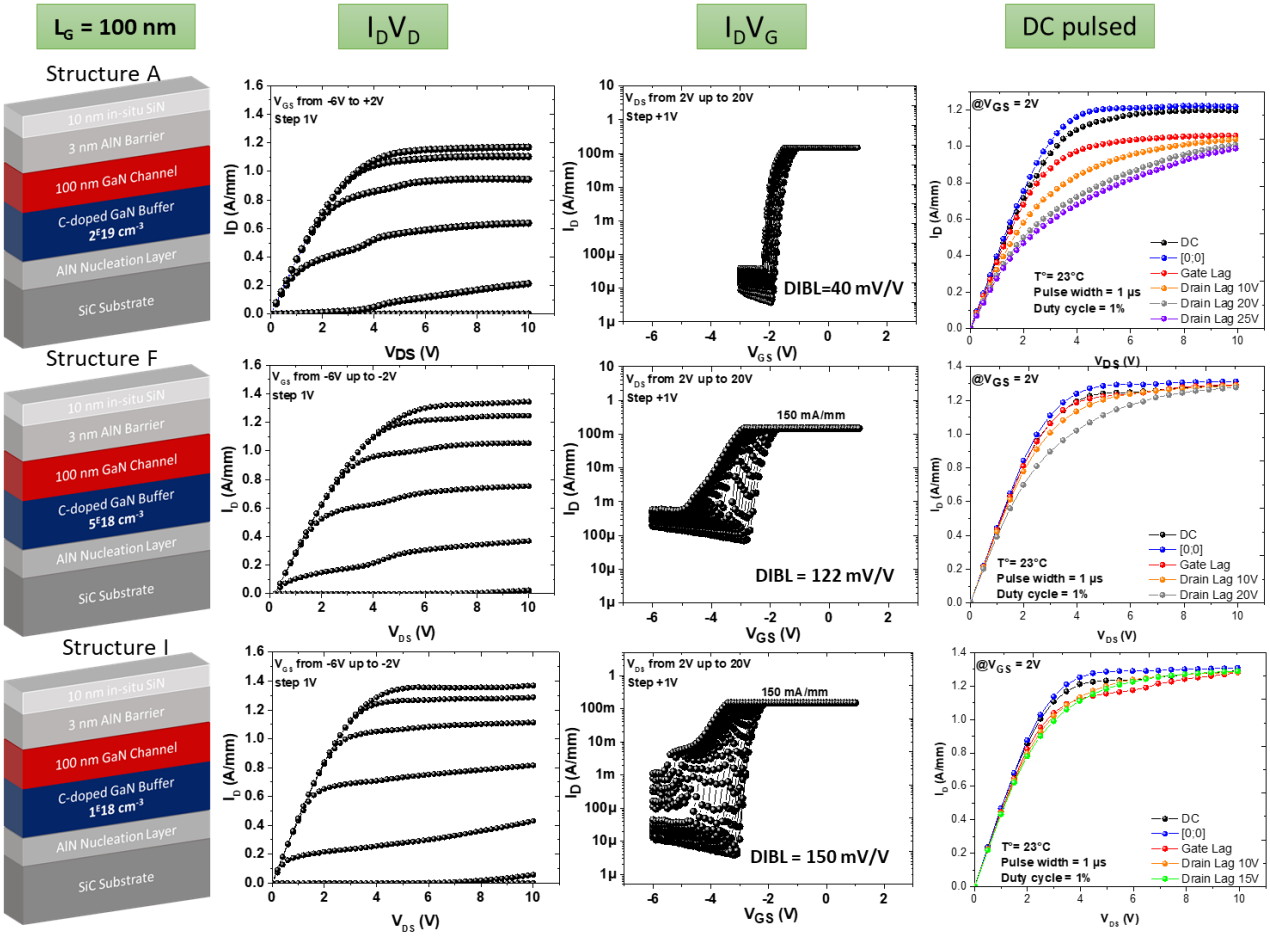


Figure.3.13. Transfer characteristics I_D (V_{DS}), semi-on robustness tests and DC pulsed characteristics of the structures with a C-doping buffer variation

CW Load-pull measurements at 40 GHz fully confirm the observations described on the I-V characteristics as shown in **Figure.3.14**. Indeed, the structure F with the intermediate carbon concentration of 5×10^{18} cm^{-3} shows enhanced RF performances at V_{DS} = 10V (both for optimum power and PAE matching). However, despite the attractive power performances, we observed a degradation of the transistor beyond V_{DS} = 10V due to the poor electron confinement in this case. On the other hand, the structure A shows lower RF performances compared to the structure F but no degradation of the transistors appeared for this structure up to V_{DS} = 30V. It can be pointed out that the structure I is not robust enough to perform any load-pull measurements.

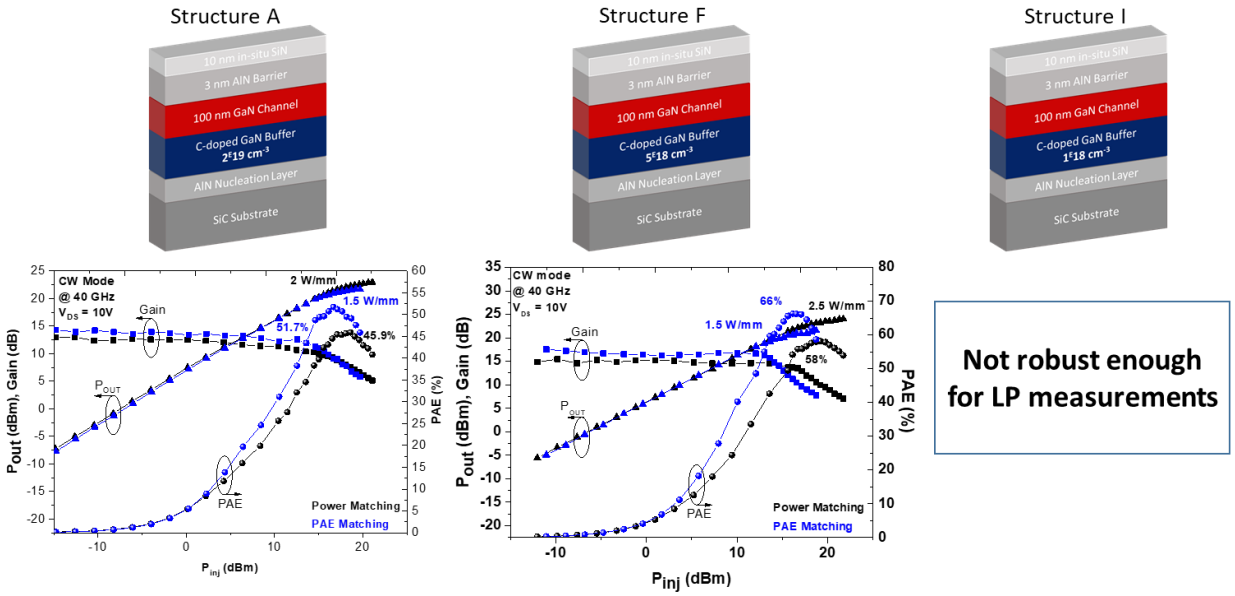


Figure.3.14. Load-pull measurements at 40 GHz and V_{DS} = 10V of the structures with a C-doping buffer variation

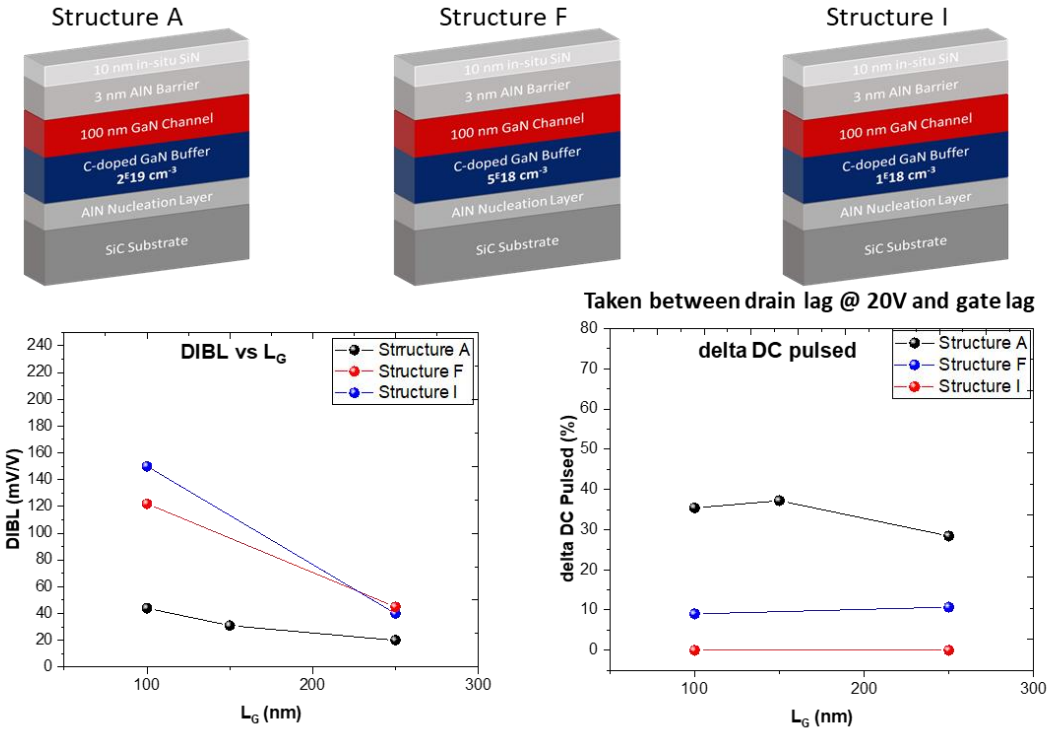


Figure.3.15. DIBL (left) and delta DC pulsed taken between drain lag at V_{DS}=20V and gate lag (right) as a function of different gate lengths for each structure.

1) Results comparison:

Figure.3.15 shows the DIBL and delta DC pulsed taken between the drain lag at V_{DS} = 20V and the gate lag as a function of different gate lengths for each structure. The trapping effects are significantly reduced when using lower carbon concentration but inversely a degradation of the electron confinement is observed through increased DIBL, especially for shorter gate length. Therefore, the carbon concentration in the buffer is a critical parameter that must be carefully optimized since it affects not only the device performances, but also the trapping effects as well as the robustness at high drain bias.

III.1.4. Study of structures with intermediate carbon doping and different channel thickness

We studied other structures in order to further confirm the observed trends previously described. The structure E consists in a carbon-doped buffer of 9×10^{18} cm^{-3} and an undoped GaN channel thickness of 150 nm while the structures J and H consist in a carbon-doped buffer of 5×10^{18} cm^{-3} and a channel thickness of 250 nm and 500 nm, respectively as shown in **Figure.3.16**.

C-doping buffer concentration \ Channel thickness	150 nm GaN	250 nm GaN	500 nm GaN
9^E18 cm^{-3}	STRUCTURE E N_s= 2.1x10^{13} cm^{-2} μ= 950 cm^2/V.s R_{sheet}= 300 Ω/sq		
5^E18 cm^{-3}		STRUCTURE G N_s= 2.1x10^{13} cm^{-2} μ= 950 cm^2/V.s R_{sheet}= 310 Ω/sq	STRUCTURE H N_s= 2x10^{13} cm^{-2} μ= 1000 cm^2/V.s R_{sheet}= 300 Ω/sq

Figure.3.16. Structures with intermediate carbon concentration of 9×10^{18} cm^{-3} and 5×10^{18} cm^{-3} and channel thickness varying from 150 to 500 nm.

1) DC and small signal characterization

Figure.3.17 shows the DIBL and delta DC pulsed taken between the drain lag at V_{DS} = 20V and the cold point as a function of the gate length. We observed rather low trapping effects for the structure H due to the low Carbon concentration in the buffer of 5×10^{18} cm^{-3} and a high channel thickness of 500 nm. However, the electron confinement and the leakage current are affected especially for the shorter gate length. The structure G with channel thickness of 250 nm and Carbon concentration of 5×10^{18} cm^{-3} shows low DIBL compared to the structure H with a channel thickness of 500 nm but it also suffers from the leakage current at high drain bias due to the low carbon concentration. Finally, the structure E with a channel thickness of 150 nm and Carbon concentration of 9×10^{18} cm^{-3} is comparable to the structure G in terms of DIBL and trapping effects but is more robust under high drain bias due to the higher carbon concentration.

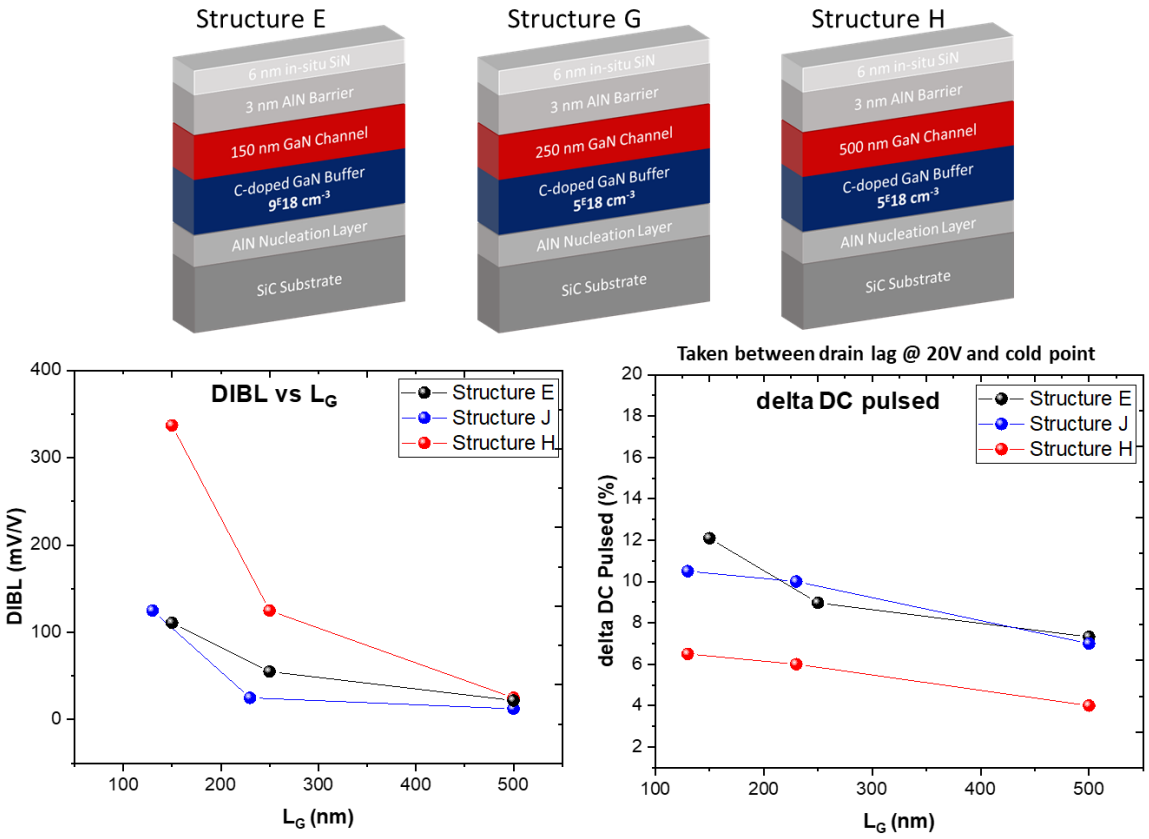


Figure.3.17. DIBL (left) and delta DC pulsed taken between drain lag at V_{DS}=20V and cold point (right) as a function of the gate length for the structures E, G and H.

2) Results discussion and comparison

In this study, the channel thickness and carbon concentration in the buffer are varied and systematically evaluated with DC characteristics. It is found that a thin GaN channel, typically below 150 nm exhibits good electron confinement, but significantly affects the trapping effects. Inversely, a thicker channel leads to reduced trapping effects but strongly degrades the electron confinement when using shorter gate length. On the other hand, high carbon concentration in the buffer leads an increased buffer resistivity and therefore enables not only high electron confinement, but also low leakage current under high electric field. Nevertheless, with high carbon concentration, transistors exhibit strong trapping effects, which are attributed to the higher point defects and nitrogen vacancies enhanced when using higher carbon concentration. Therefore, the channel thickness and the carbon concentration must be traded-off in order to avoid the parasitic effects such as punch-through and high DIBL and trapping thus enhancing the device performances and robustness (**Fig. 3.18**).

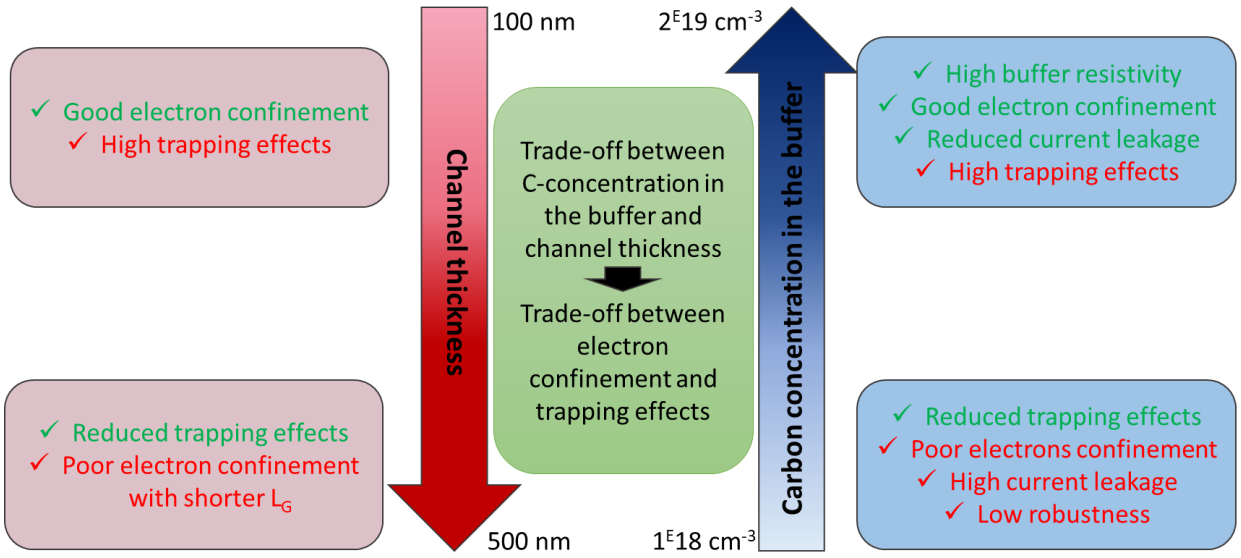


Figure.3.18. Schematic summary of the carbon concentration and the channel thickness impact on short GaN transistors

III.2. Study of the AlGaN back barrier

In the previous study, we observed that a carbon concentration limited to 5×10^{18} cm^{-3} in the buffer allows significantly reduced trapping effects but results in transistors with high leakage current under high drain bias directly affecting the device robustness. An effective solution is the introduction of an AlGaN back barrier (BB) underneath the GaN channel layer, which provides an electrostatic barrier preventing the punch-through effect and thus the drain leakage current. Combined with a low carbon-doping, this should enable maintaining low trapping effects.

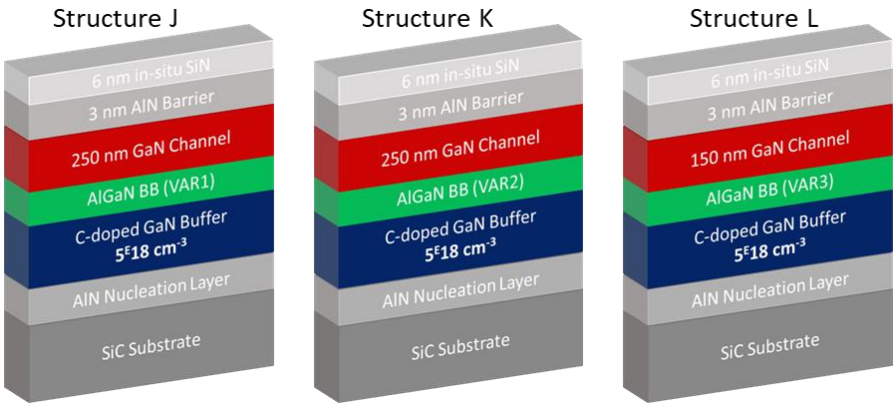


Figure.3.19. Cross section of the structures with carbon concentration of 5×10^{18} cm^{-3} and an AlGaN BB with VAR1, VAR2 and VAR3 for the structures J, K and L respectively

Figure.3.19 shows a cross section of the structures J, K, and L which consist in a 5×10^{18} cm^{-3} C-doped GaN buffer, a 200 nm AlGaN BB with low Al-content (4%) in order to improve the thermal dissipation. The AlGaN BB (VAR1 and VAR2 that can be disclosed) of the structures J and K is partly C-doped in the first 100 nm while the AlGaN BB (VAR3) of the structure L is undoped. The channel thickness is about 250 nm for the structure J and K and 150 nm for the structure L. Then a 3 nm AlN barrier layer and 6 nm in-situ SiN cap layer complete the growth. For these structures, Hall measurements show similar 2DEG density and mobility around 2.4×10^{13} cm^{-2} and 900 $cm^2/V.s$ respectively. The sheet resistance extracted by the same method is about 285 Ω/□.

1) Device fabrication

The same process described previously was applied except for the gate module etching. For these structures, we used an in-situ Argon etching plasma inside the metallization chamber. This etching method allows a shorter gate length but more important enables to suppress the Fluor implantation observed with HRTEM characterization. Indeed, it is known that the Fluor accumulation at the gate/barrier layer interface induces trapping effects [148]. **Figure.3.20** shows the various gate lengths varying from 500 nm to 80 nm fabricated on these structures using the same mask set in order to evaluate the impact of the electric field on the electron confinement.

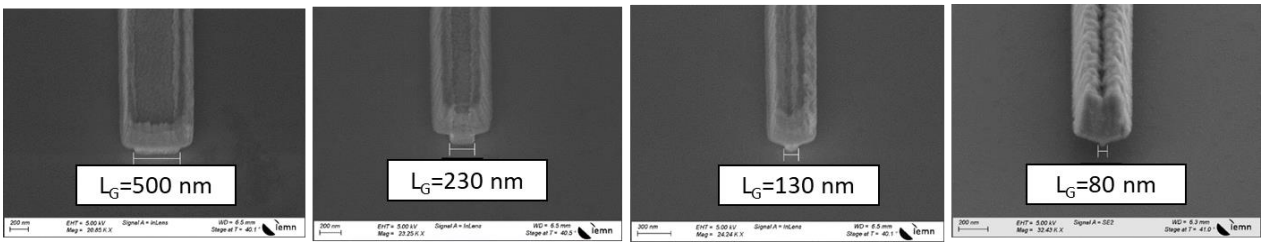


Figure.3.20. SEM image of different gate length

2) DC and small signal characterization

Transfer characteristics, semi-on robustness tests and DC pulsed measurements of the structures J, K, and L are shown in **Figure.3.21**. 2 × 50 µm transistors with gate-to-drain distance L_{GD} of 1.5 µm and a gate length L_G of 130 nm show a maximum drain current $I_{D\,max}$ between 0.8 and 1 A/mm due to the non-optimized ohmic contacts. We observed a reduced kink effect on I_D (V_{DS}) characteristics. Indeed, the trapping effects are reduced as shown on DC pulsed characteristics due to the use of both a low carbon concentration and the Fluor-free gate module processing. Moreover, we observed a low leakage current on the semi-on robustness tests for the three structures as expected. However, the electron confinement is slightly increased

with the shorter gate lengths. It can be pointed out that other gate lengths were measured in order to evaluate the impact on the electron confinement. This is depicted in the summary graphs (**Figure.3.22**).

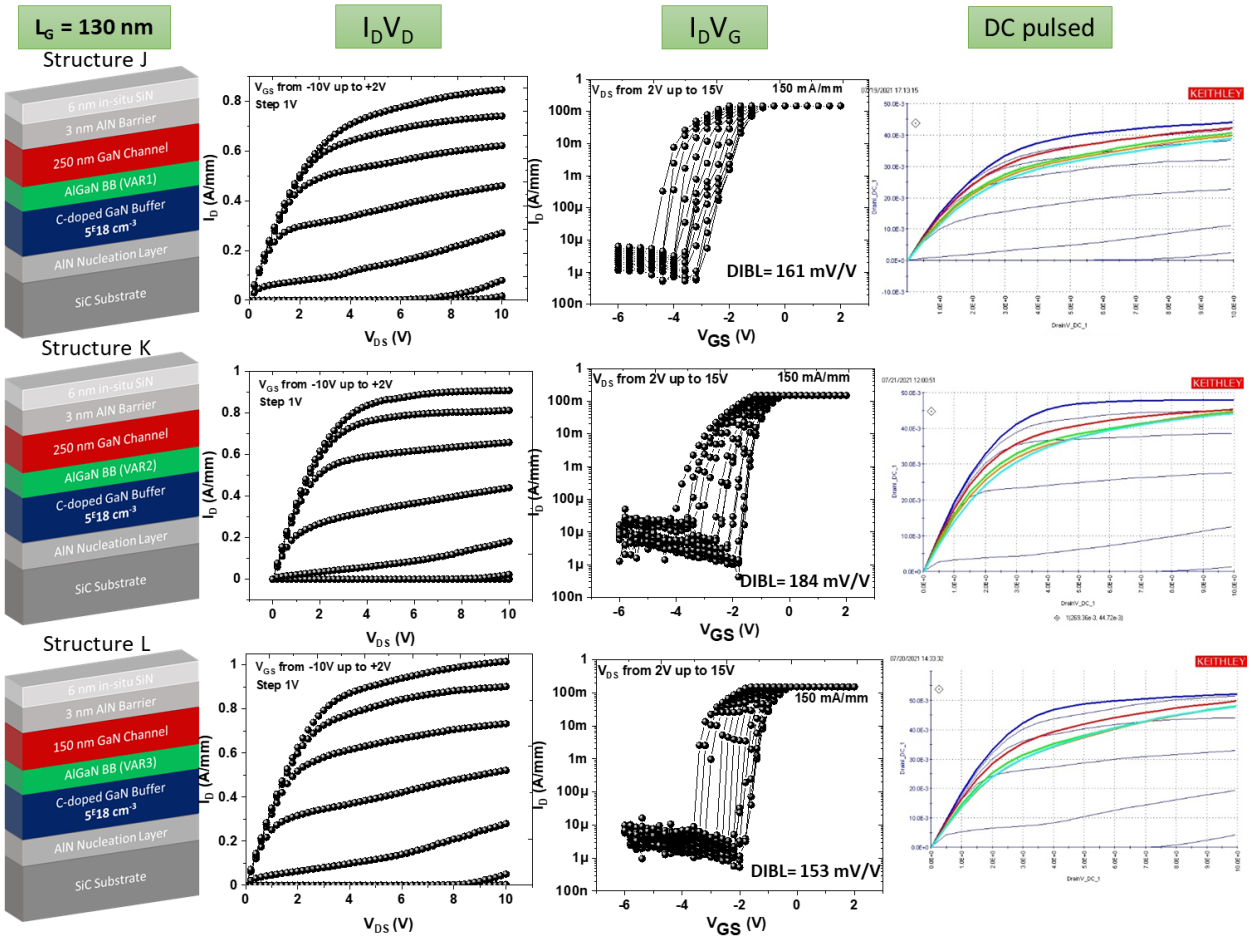


Figure.3.21. Transfer characteristics I_D (V_{DS}), semi-on robustness test and DC pulsed characteristics of the structures with an AlGaN BB

3) Results discussion and comparison

Figure.3.22 shows the DIBL and delta DC pulsed taken between the drain lag at V_{DS} = 15V and the gate lag as a function of the gate length for the structures J, K, and L. The trapping effects are significantly reduced due to not only the low carbon concentration of 5×10^{18} cm^{-3}, but also the gate etching processing without Fluor implantation. The degradation of the electron confinement is observed with short gate lengths (sub-150 nm), which is due to the low Al-content in the AlGaN BB. These structures show a quite similar characteristics which can be explained by the fact that the dopant variation in the AlGaN BB has no impact

on the DC characteristics. Therefore, similar structures with higher Al-content in the AlGaN BB (e.g. 10%) will enhance the electron confinement with short gate lengths while avoiding trapping effects as low C-doping is maintained. It can be pointed out that this batch is under way and will be processed and characterized.

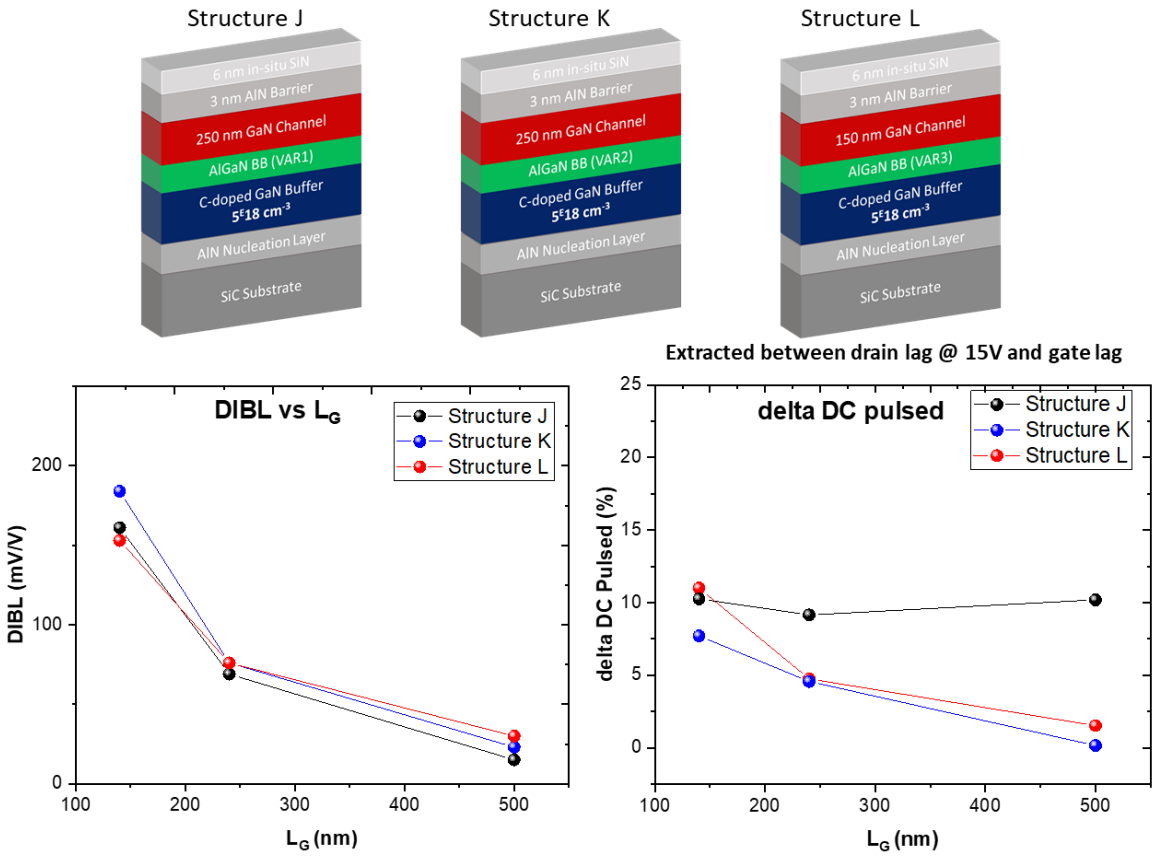


Figure.3.22. DIBL (left) and delta DC pulsed taken between drain lag at V_{DS}=15V and gate lag (right) as a function of the gate length for the structures J, K and L.

III.3. Impact of the barrier thickness 3 nm and 4 nm AlN/GaN

Figure.3.23 shows a schematic cross section of two epitaxial structures grown by MOCVD on 4-inch SiC substrate by SOITEC. After optimizing the C-doped buffer and the channel thickness, two different AlN barrier thicknesses 3 nm and 4 nm have been used in order to study the impact on RF device performances. For the 3 nm AlN/GaN structure, the growth time is basically reduced by 25% compared to the 4 nm AlN/GaN structure. Hall Effect measurements shows the same sheet resistance of ~ 340 Ω/□ and electron mobility of ~ 900 cm^2/V.s. As expected the structure B with a thicker barrier shows a higher electron density of 2×10^{13} cm^{-2} whereas the structure A shows an electron density of 1.8×10^{13} cm^{-2}.

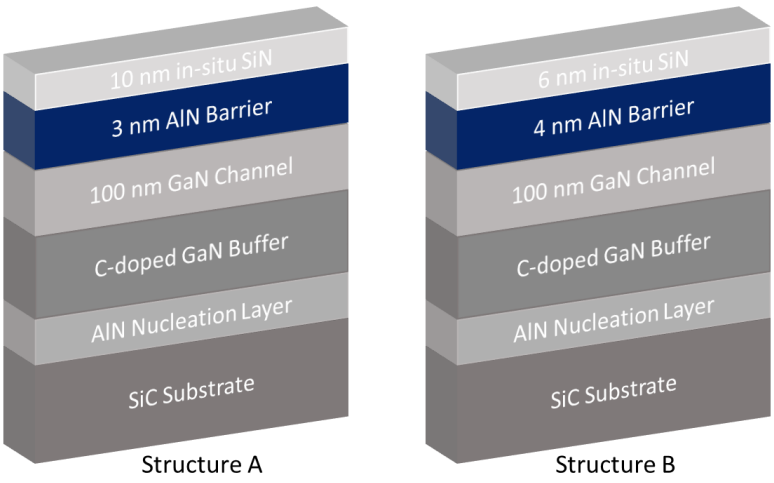


Figure.3.23. Schematic cross section of the 3 nm and 4 nm AlN/GaN epitaxial structures.

III.3.1. Shared process UMS-IEMN

The corresponding devices have fabricated within the project ALIEN within which a UMS-IEMN shared processing of advanced heterostructures targeting high device performances beyond GH10 technology has been established. Three batches of 2 wafers have been processed and characterized at IEMN. The first batch contains two wafers based on 4 nm AlN barrier layer (Structure B) and the two other batches contain four wafers based on 3 nm AlN barrier layer (Structure A).

III.3.1.1. 4 nm AlN/GaN structures

Two similar wafers grown on 4-inch SiC substrates have been used (see **Figure.3.24**). The HEMT structures consist in a 1 µm carbon doped buffer followed by a 100 nm GaN channel and a thin AlN barrier of 4 nm capped with a 10 nm in-situ SiN to prevent oxidation and ensure high surface quality despite the highly strained heterostructure. It can be noticed that the characterizations results will be shown only for one wafer since both shows comparable results.

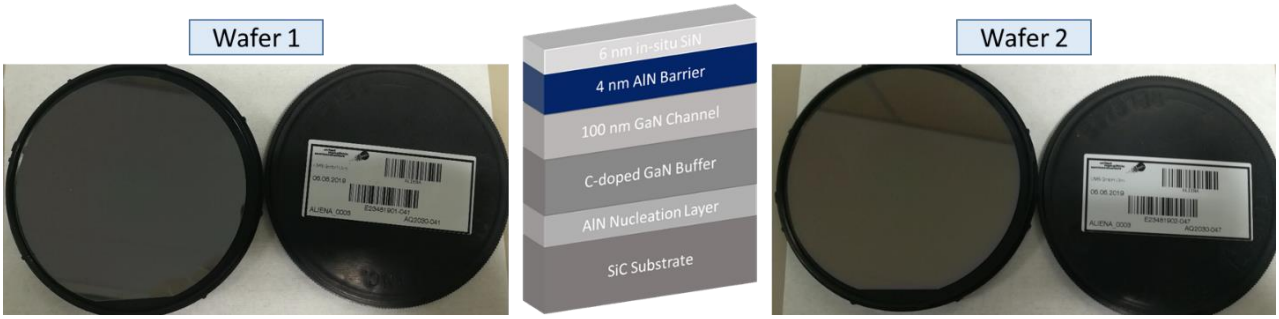


Figure.3.24. Schematic cross section and photos of the 4 nm AlN/GaN heterostructures

1) Device fabrication

The fabrication process of this study has been carried out using a shared process UMS-IEMN mask-set. Similar process has been applied on the wafers, which showed a comparable electrical characterization. A Ti/Al/Ni/Au metal stack annealed at 875°C has been used to form source-drain ohmic contacts directly on top of the AlN barrier by etching the in-situ SiN layer. The contact resistance extracted by TLM method is about 0.4 Ω.mm. Ti/Au T-gates were defined by e-beam lithography. The SiN underneath the gate was fully removed using SF_6 plasma etching through the e-beam lithography. Finally, 200 nm PECVD SiN layer was deposited as final passivation. **Figure.3.25** shows SEM gates image of both IEMN and UMS PCM. From SEM measurements, estimated gate lengths are about 105 nm and 150 nm. Two gate-to-drain distances (L_{GD} = 0.5 µm and L_{GD} = 1.5 µm) have been used on IEMN PCM devices and L_{GD} = 1.5 µm for UMS devices.

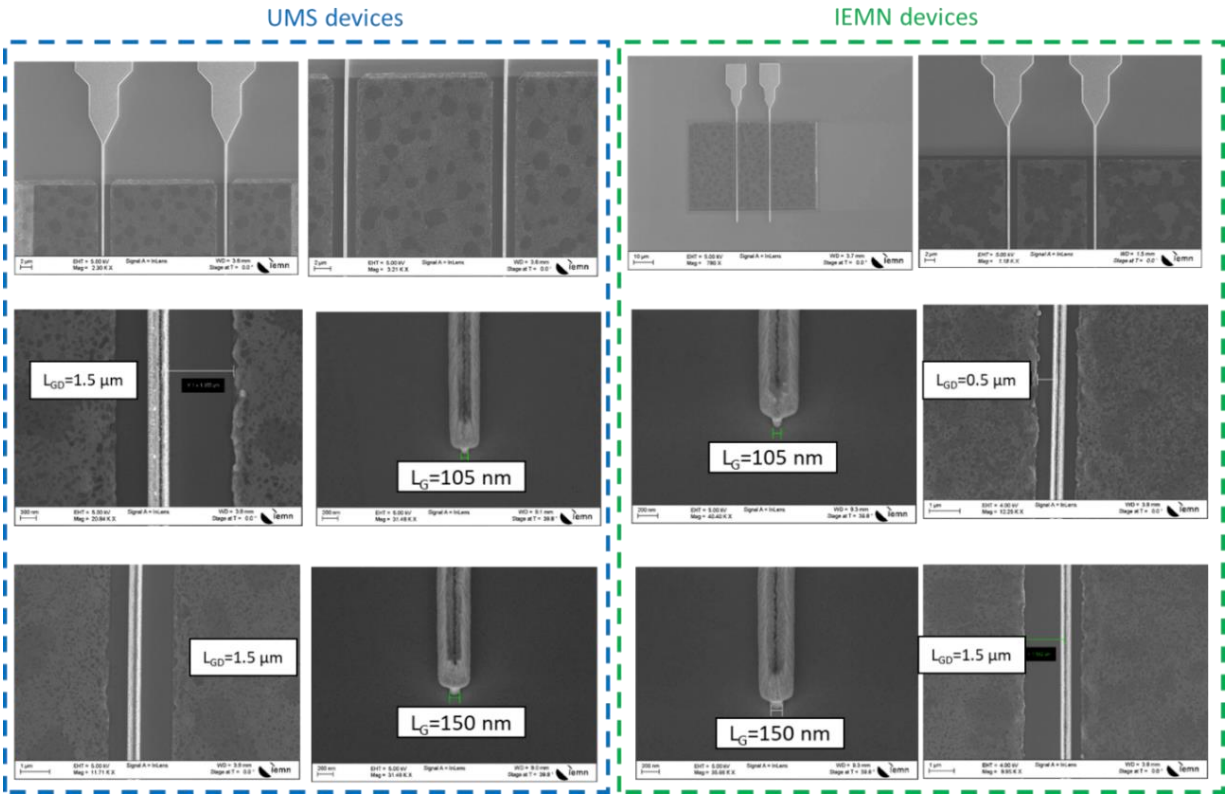


Figure.3.25. SEM transistor images of IEMN and UMS devices showing the different gate lengths and gate-to-drain distances.

2) DC and small signal characterization

Transconductance, transfer and output characteristics are shown in **Figure.3.26** on a 2×50 µm transistor with L_{GD} = 1.5 µm. All characteristics have been measured after a burn-in step, which consists of biasing

the transistor at high drain voltage for several seconds until the stabilization of the maximum drain current I_{Dmax}. A pinch-off voltage about V_{th} = -3V has been observed with a leakage current below 10 µA/mm. An I_{Dmax} of 1.4 A/mm (@ V_{GS} = +2V) and an extrinsic G_m = 400 mS/mm for L_g = 105 nm have been measured with a relatively good uniformity.

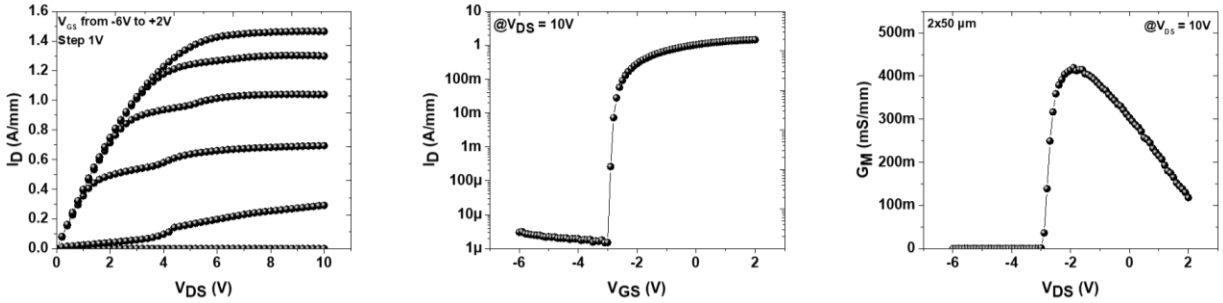


Figure.3.26. Transconductance, transfer and output characteristics of a 2 × 50 µm transistors with L_{GD} = 1.5 µm and L_G = 105 nm of the 4 nm AlN/GaN structure

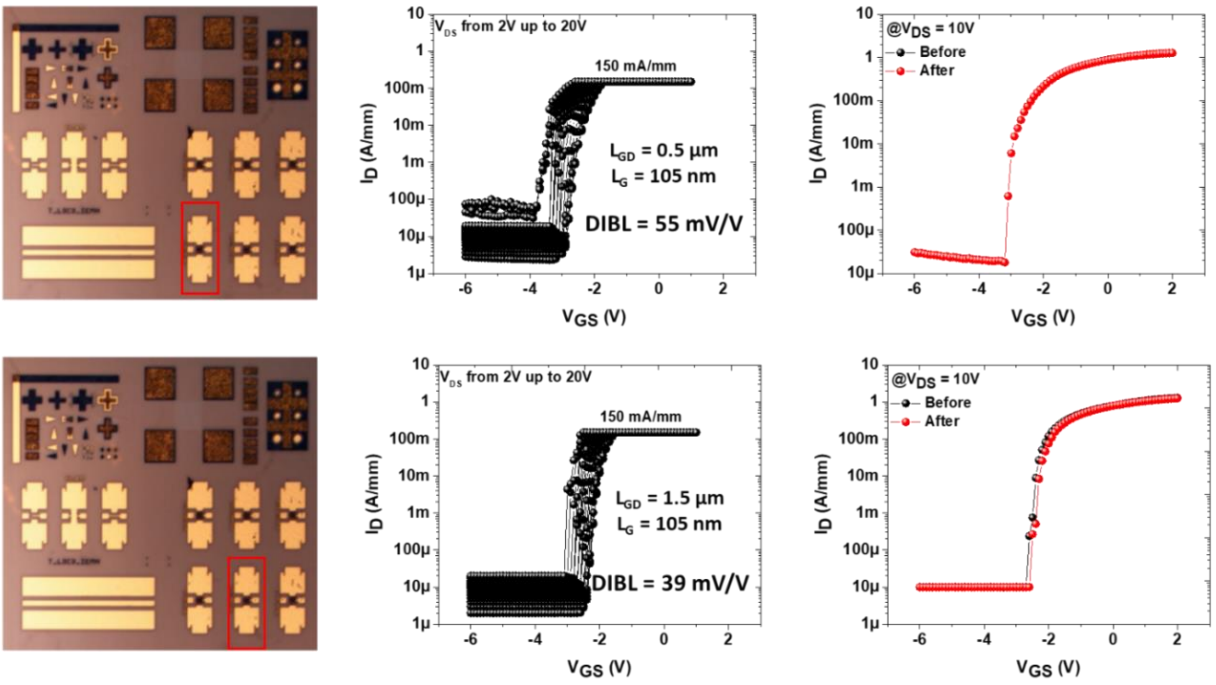


Figure.3.27. Semi-on robustness test of 2 × 50 µm transistors with L_{GD} of 0.5 µm and 1.5 µm and L_G = 105 nm of the 4 nm AlN/GaN structure.

In order to assess the electron confinement, Semi-on robustness tests have been carried out. Several I_D (V_{GS}) sweeps up to V_{DS} = 20V with a drain current I_D limitation at 150 mA/mm were carried out on two transistor designs. DIBL of 55 and 39 mV/V have been extracted for L_{GD} = 0.5 µm and 1.5 µm respectively.

For the short L_{GD} = 0.5 µm, an off-state current degradation for V_{DS} > 15V is observed as shown in **Figure.3.27**.

Small signal characteristics have been measured on several devices across the wafer (see **Figure.3.28**). An F_t/F_{max} around 75/190 GHz is observed for a 2×50 µm, L_{GD} = 0.5 µm at V_{DS} = 20V with a good uniformity. It is important to note that a systematic degradation of the transistors after the small signal measurements is observed reflected by an off-state degradation at $V_{DS} \geq$ 15V. This already indicates a lack of robustness of these devices beyond V_{DS} = 15 V.

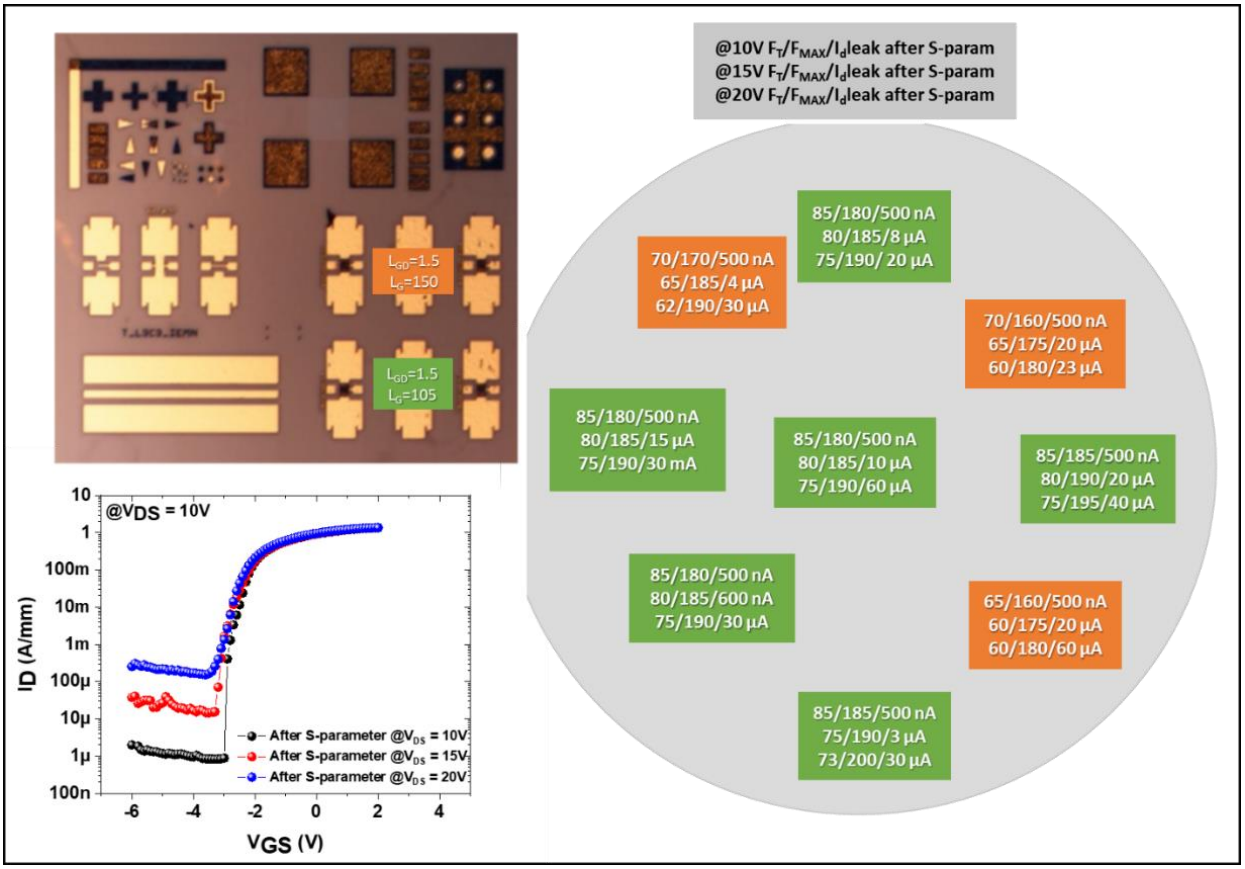


Figure.3.28. Small signal device characteristics measured across the wafer on 2 × 50 µm transistors with L_{GD} = 1.5 µm and two gate lengths of L_G = 105 and 150 nm of the 4 nm AlN/GaN structure

3) Large signal characterization @40 GHz

Large signal measurements have been performed on a Network Analyzer (PNA)-X (N5245A-NVNA) enabling on-wafer load-pull characterizations at 40 GHz in continuous-wave (CW) and pulsed mode. **Figure.3.29** shows 40 GHz CW power performances of a 2 × 50 µm with a gate-drain distance L_{GD} = 1.5 µm and a gate length L_G =105 nm at V_{DS} = 10V and 20V for the 4 nm AlN/GaN structure. A PAE of 50%

is observed at V_{DS} = 10V with a saturated power density P_{OUT} = 1.5 W/mm. At V_{DS} = 20V, the PAE decreases down to 45% with a POUT of 2.9 W/mm. The decrease of performances at higher drain voltage is attributed to the degradation of the device during the measurements.

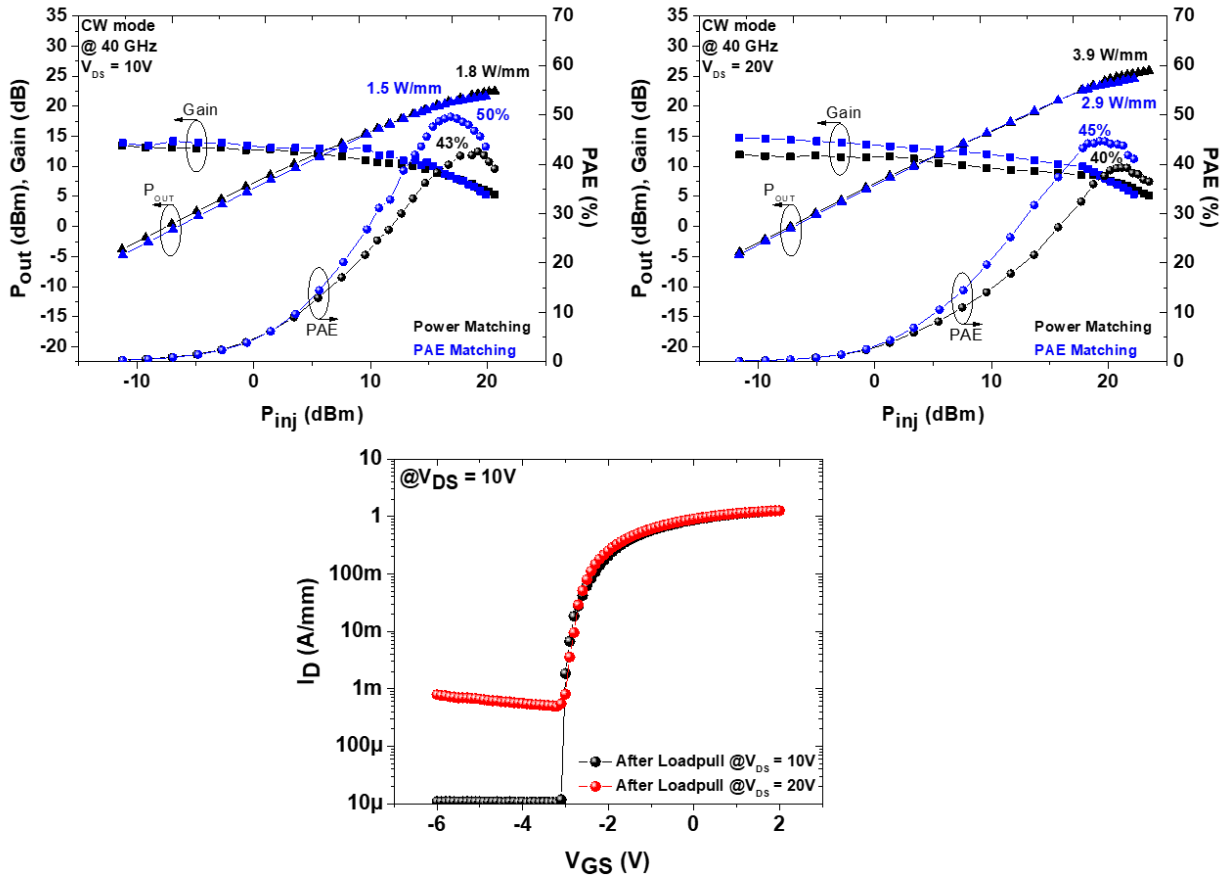


Figure.3.29. CW large signal performances at 40 GHz for a 2×50 µm transistor with L_G = 105 nm at V_{DS} = 10V and 20V of the 4 nm AlN/GaN HEMT structure and transfer characteristics after load-pull sweep up to V_{DS} = 20V.

Figure.3.30 shows the pulsed power performances for L_{GD} = 1.5 µm and various V_{DS} up to 20V. In this case, the PAE remains around 61% up to V_{DS} = 20V with a saturated P_{OUT} of 3.2 W/mm (PAE matching). CW and pulsed large signal manual mapping across the wafer have been carried out at 40 GHz with V_{DS} = 20V and PAE matching as shown in **Figure.3.31**. The mapping shows a PAE around 50% and 60% for all devices measured in CW and pulsed mode, respectively.

Despite good large signal performances, a strong impact of trapping effects can be observed through the PAE drop between CW and Pulsed mode (see **Figure.3.32**). It is important to note that even in pulsed mode degradation of device is observed under high V_{DS}.

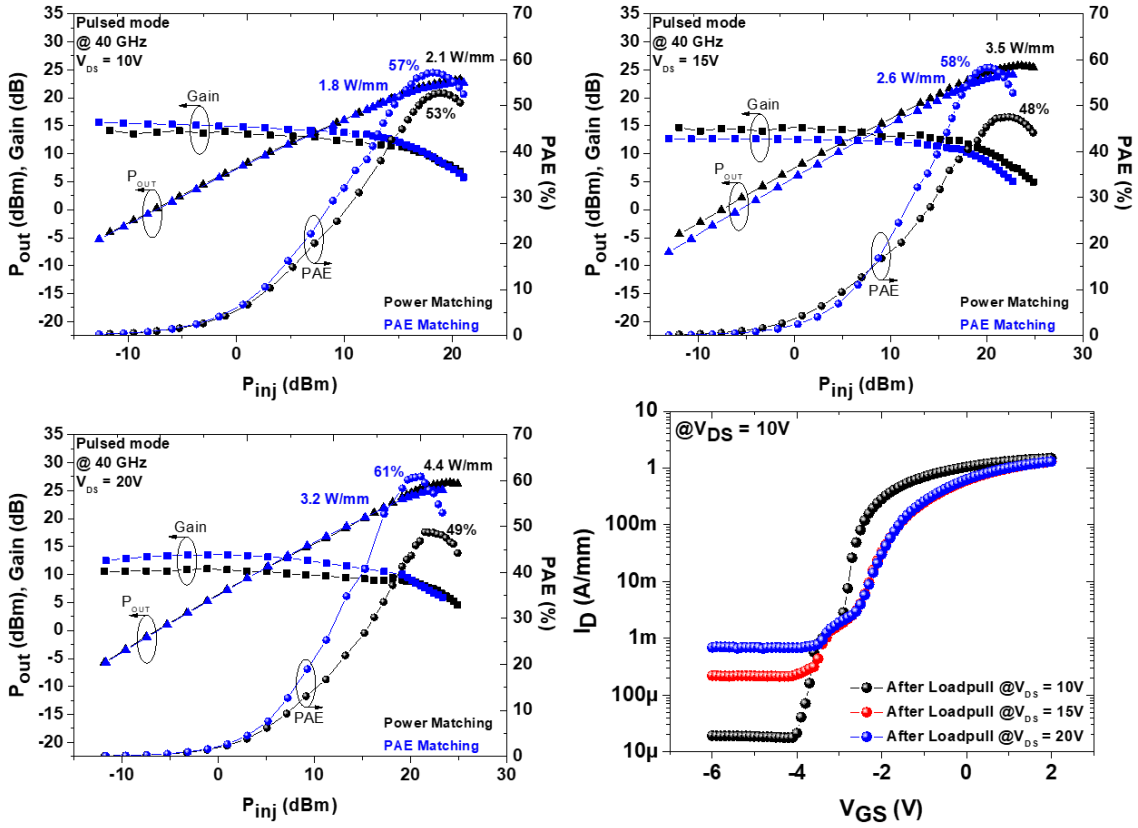


Figure.3.30. CW large signal performances at 40 GHz for a 2×50 µm transistor with L_G = 105 nm at V_{DS} = 10V and 20V of the 4 nm AlN/GaN HEMT structure and transfer characteristics after the load-pull sweeps up to V_{DS} = 20V.

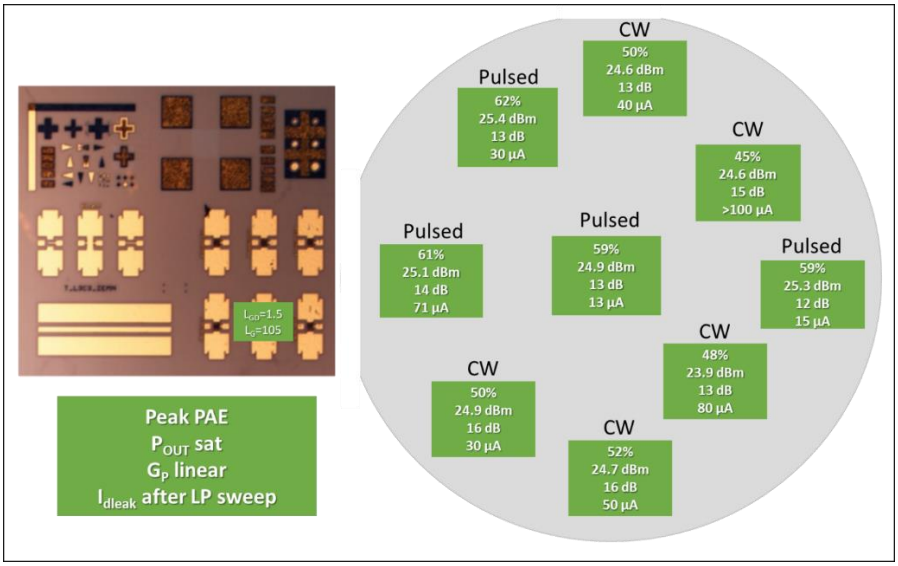


Figure.3.31. CW and pulsed large signal manual mapping at 40 GHz of 2×50 µm with L_G = 105 nm and L_{GD} = 1.5 µm at V_{DS} = 10V of the 4 nm AlN/GaN HEMT structure

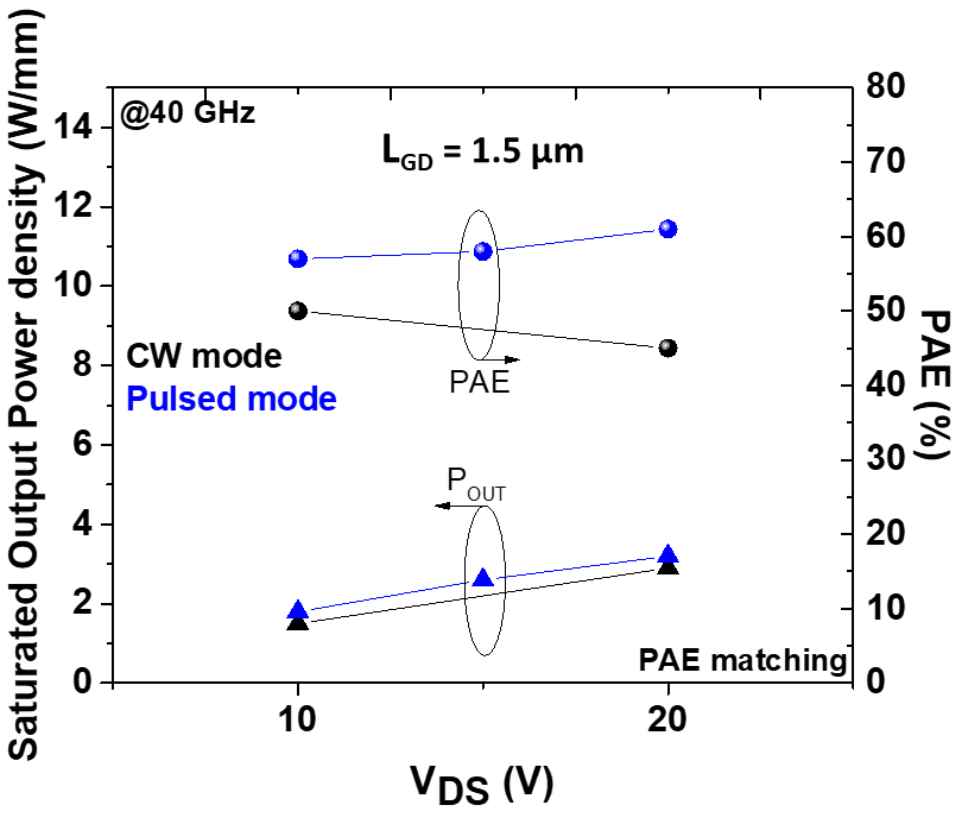


Figure.3.32. PAE and output power density (P_{OUT}) vs V_{DS} in pulsed and CW mode of the 4 nm AlN/GaN HEMT structure.

4) Short term reliability @40 GHz

Short-term on wafer RF step stress at 40 GHz has been carried out using various drain voltages. 2 × 50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm for the 4 nm AlN/GaN structure have been monitored at room temperature during 24 hours by steps of 8 hours under large signal conditions and at peak PAE as shown in **Figure.3.33**. At V_{DS} = 12V a systematic strong degradation of performances over time with a significant increase of leakage current is observed. Indeed, we can see clearly a drop of the output power density and the PAE from 45% to 30% after 24 hours stress while the P_{OUT} strongly reduces from 1.4 W/mm down to 0.8 W/mm. Several attempts have been carried for V_{DS} beyond 12V with a systematic instantaneous severe degradation of performances. The drain leakage current after each RF step stress is shown. After 24 hours at 12V (in red), we can clearly see a degradation of the leakage current while at V_{DS} > 12V we observed a strong degradation of the transistor after only few minutes of test. These results confirm the poor robustness observed already during large signal characterizations for V_{DS} beyond 12V.

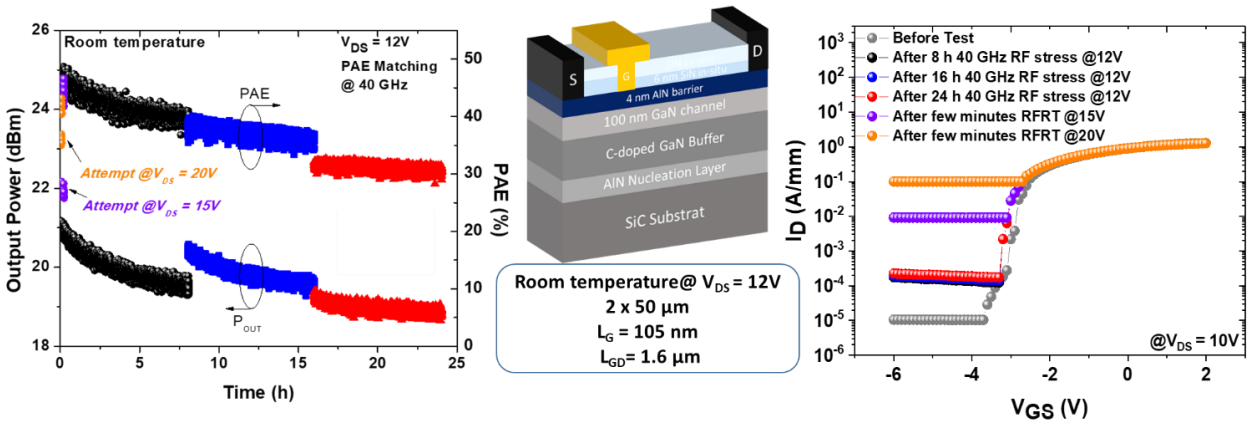


Figure.3.33. PAE and output power monitoring for 24 hours at room temperature on 2 × 50 µm transistor with L_G = 105 nm and L_{GD} = 1.5 µm at V_{DS} = 12V, 15V and 20V (PAE matching), and transfer characteristics before and after 8, 16 and 24 hours of 40 GHz RF stress of the 4 nm AlN/GaN HEMT structure.

5) DC short term reliability performed at the University of Padova

In order to further assess the robustness of the 4 nm AlN/GaN structure, parametric degradation and breakdown effect during V_{DS} step stress tests at off-state and semi-on state has been performed at the University of Padova [157].

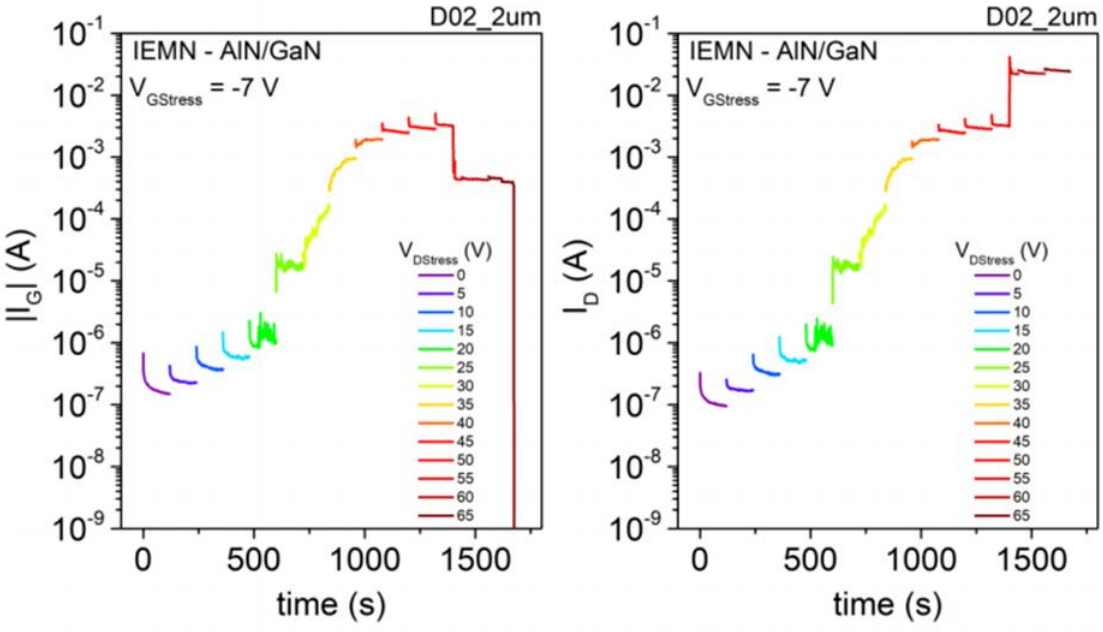


Figure.3.34. off-state drain step stress on a 2×50 µm transistor with L_G = 105 nm, L_{GD} = 1.5 µm of the 4 nm AlN/GaN HEMT structure

The first measurement shown in **Figure.3.34** consists in monitoring the gate and the drain current in off-state stress (pinch voltage: V_{GS} = -7V) during 24 hours for several V_{DS} at room temperature on a 2×50 µm transistor with L_G = 150 nm and L_{GD} = 1.5 µm. We observed a degradation of the gate current from V_{DS} = 20V after 10 hours. At V_{DS} = 25V a significant increase in gate and drain leakage is observed. Beyond V_{DS} = 25V, a strong increase in leakage current leading to the destruction of the transistor at V_{DS} = 65V after 24 hours.

The second measurement consists in monitoring the gate and the drain current in semi-on state (V_{GS} = -1.5V) during 24 hours for several drain voltages up to V_{DS} = 100V on a 2×50 µm with L_G = 105 nm and L_{GD} = 1.5 µm. The gate current remains below 10 µA/mm up to V_{DS} = 25V after 10 hours as shown in **Figure.3.35**. At the same time, the drain current shows an increase of 57% from the initial value. For a stress voltage of 30V a significant increase in gate current is observed associated to a decrease in drain current. Beyond V_{DS} = 30V, an increase of the gate current up to 70 mA/mm at V_{DS} = 100V.

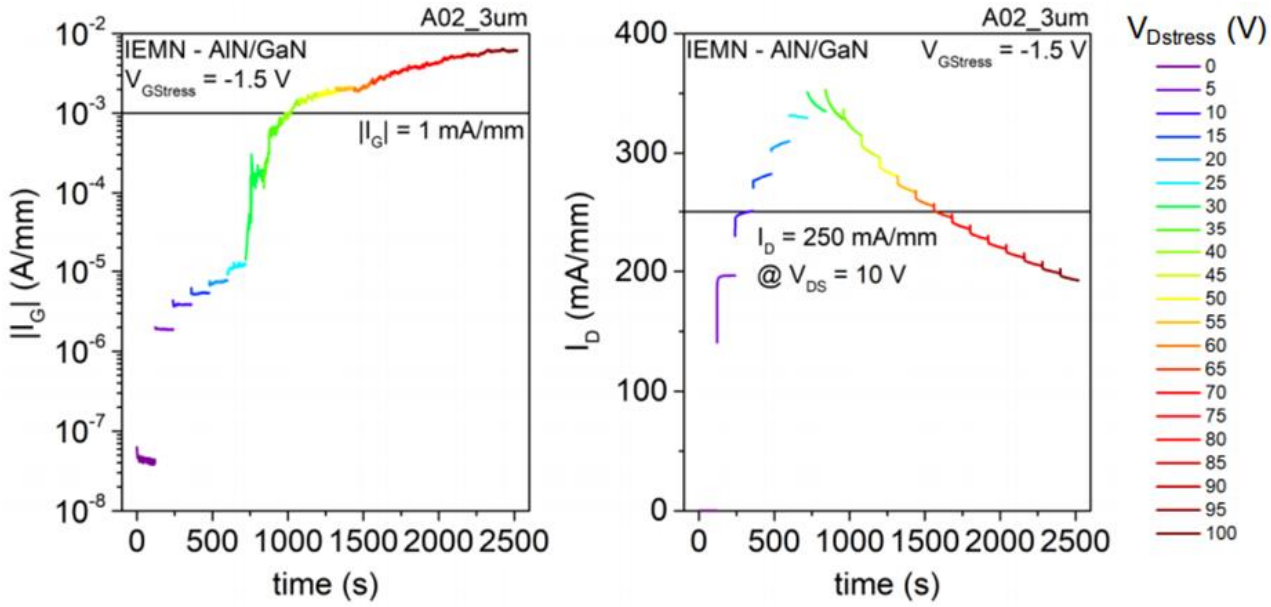


Figure.3.35. Semi-on-state drain step stress on 2×50 µm transistor with L_G = 105 nm, L_{GD} = 1.5 µm of the 4 nm AlN/GaN HEMT structure

Overall, the DC short-term stress fully confirms the instable nature under high electric field of the 4 nm AlN/GaN HEMT as observed in the RF stress tests.

III.3.1.2. 3 nm AlN/GaN structures

For the second and third batch, four similar wafers grown on 4-inch SiC substrate have been used (see **Figure.3.36**). The HEMT structure consist in a 1 µm carbon doped buffer followed by a 100 nm GaN channel and a 3 nm thin AlN barrier capped with a 10 nm in-situ SiN. It can be pointed out that a total of 4 wafers based on 3 nm AlN/GaN have been processed but again the characterizations results will be shown for only one wafer as they deliver similar results.

Figure.3.36. Schematic cross section and photos of the 3 nm AlN/GaN heterostructures

1) Device fabrication

The fabrication process is similar to that of the first batch except the ohmic contacts, which have been annealed at 850°C. The contact resistance extracted by TLM method is about 0.5 Ω.mm on this structure. **Figure.3.37** shows some SEM gate images of both IEMN PCM and UMS devices. From SEM measurements for both gate designs, similar gate lengths than batch 1 have been measured. Two gate-to-drain distances (L_{GD} = 0.5 µm and L_{GD} = 1.5 µm) have been used for IEMN devices and L_{GD} = 1.5 µm for UMS devices for fair comparison. Multi-finger devices have been characterized on this structure after back-end processing at UMS.

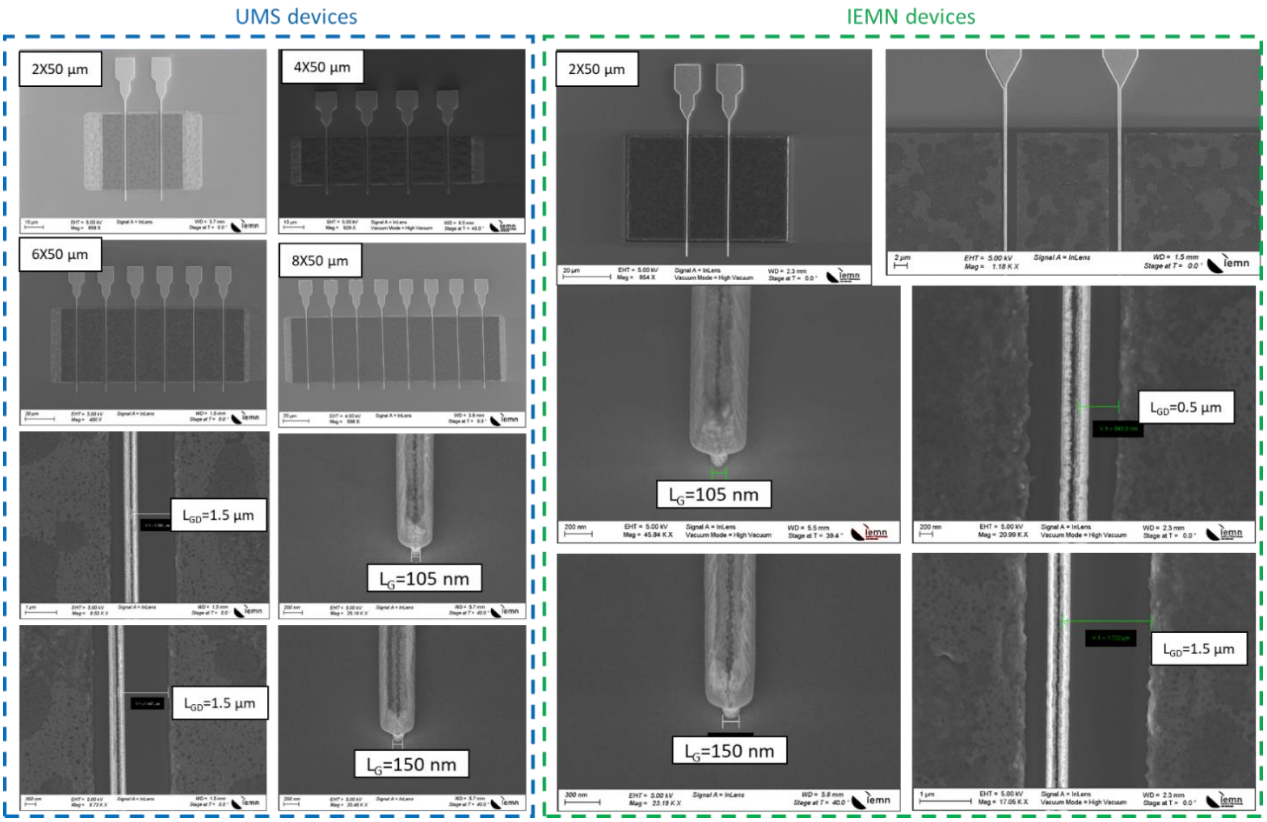


Figure.3.37. SEM transistor images of IEMN (two-finger transistors) and UMS devices (multi-finger transistors) showing the different gate lengths and gate-to-drain distances.

2) DC and small signal characteristics

Transconductance, transfer and output characteristics are shown in **Figure.3.38** on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 0.5 µm. All characteristics have been measured after a burn-in step. A pinch-off voltage V_{th} of about -2.9V has been observed with a leakage current below 100 µA/mm. An $I_{D\,max}$ of 1.1 A/mm (@ V_{GS} = +2V) and Gm = 450 mS/mm for L_G= 105 nm have been measured.

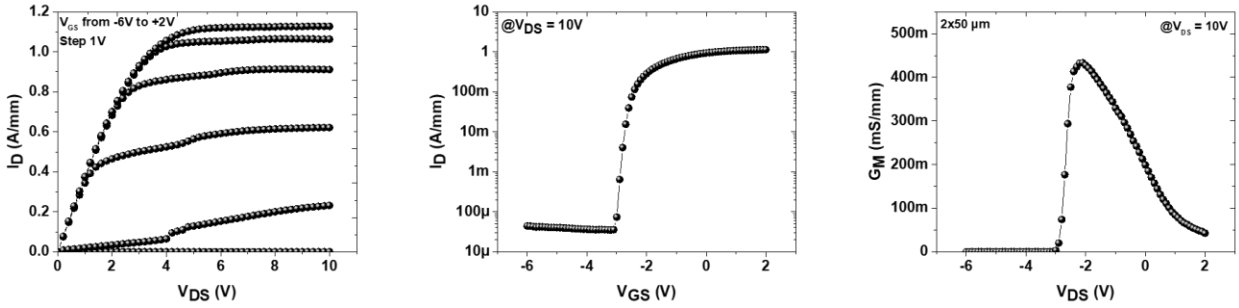


Figure.3.38. Transconductance, transfer and output characteristics of a 2×50 µm transistors with L_{GD} = 0.5 µm and L_G = 105 nm of the 3 nm AlN/GaN structure

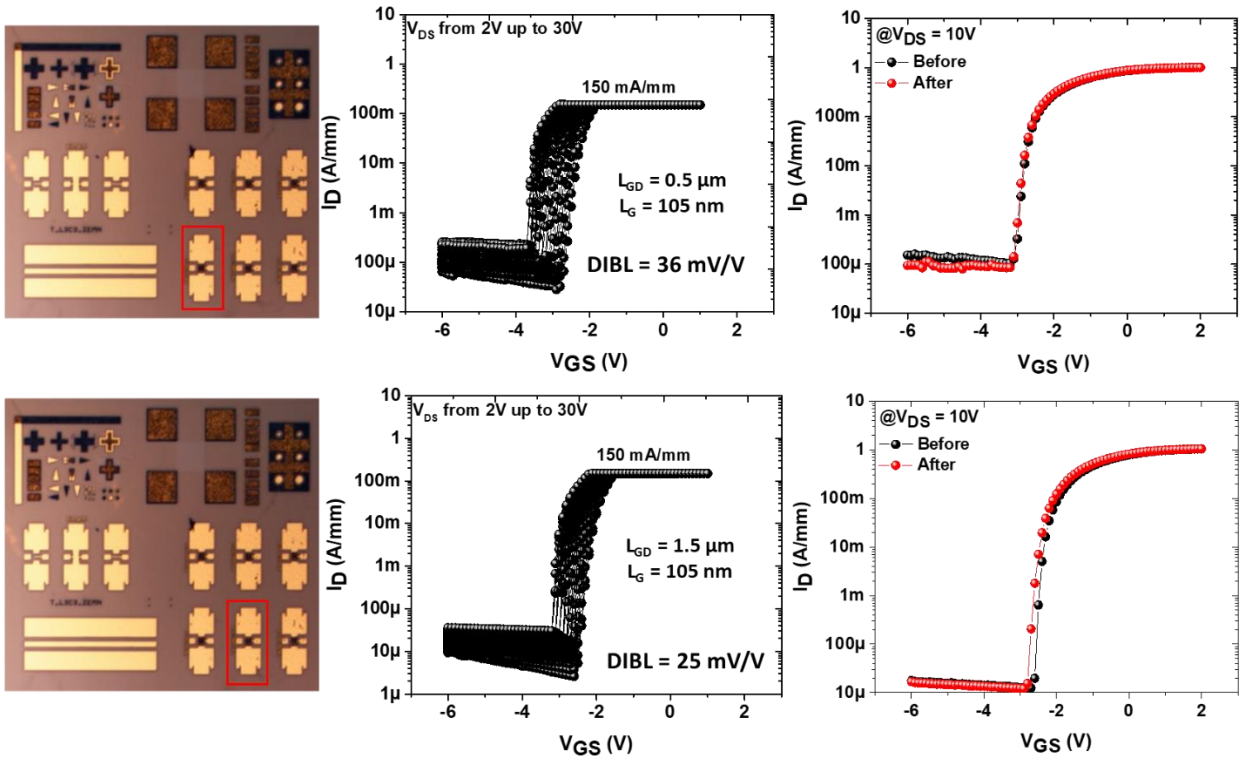


Figure.3.39. Semi-on robustness tests of 2×50 µm transistors with L_G = 105 and L_{GD} of 0.5 µm and 1.5 µm of the 3 nm AlN/GaN structure.

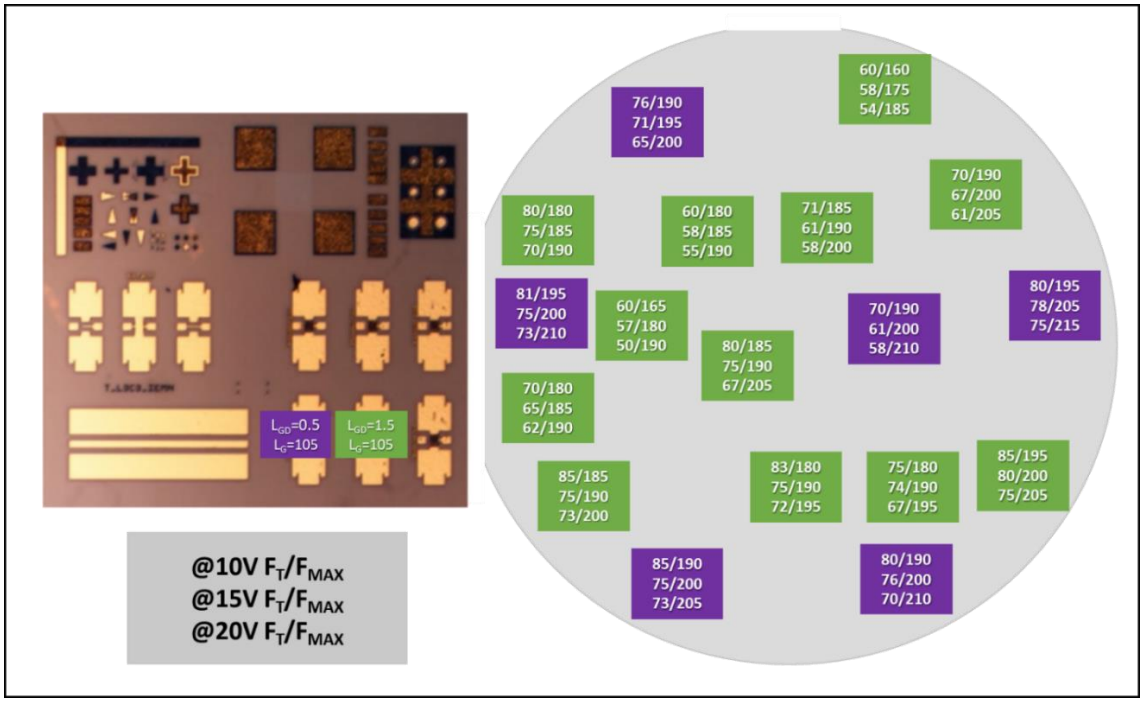


Figure.3.40. Manuel mapping of small signal characteristics measured across the wafer on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 0.5 µm of the 3 nm AlN/GaN structure

The electron confinement has been assessed in the same way using the semi-on robustness routine. Several I_D (V_{GS}) sweeps corresponding to different V_{DS} up to 20V with a drain current I_{DS} limitation at 150 mA/mm were carried out on several transistors. A DIBL of 36 and 25 mV/V has been extracted for a L_{GD} = 0.5 µm and 1.5 µm, respectively as shown in **Figure.3.39**.

Small signal characteristics have been measured on several devices across the wafer. An f_t /f_{max} around 75/210 GHz are observed for 2×50 µm transistors with L_G = 105 nm and L_{GD} = 0.5 µm at V_{DS} = 20V (see **Figure.3.40**). It is important to note that no degradation of the device after small signal measurements is observed up to V_{DS} = 20V unlike the 4 nm AlN/GaN structure from batch1.

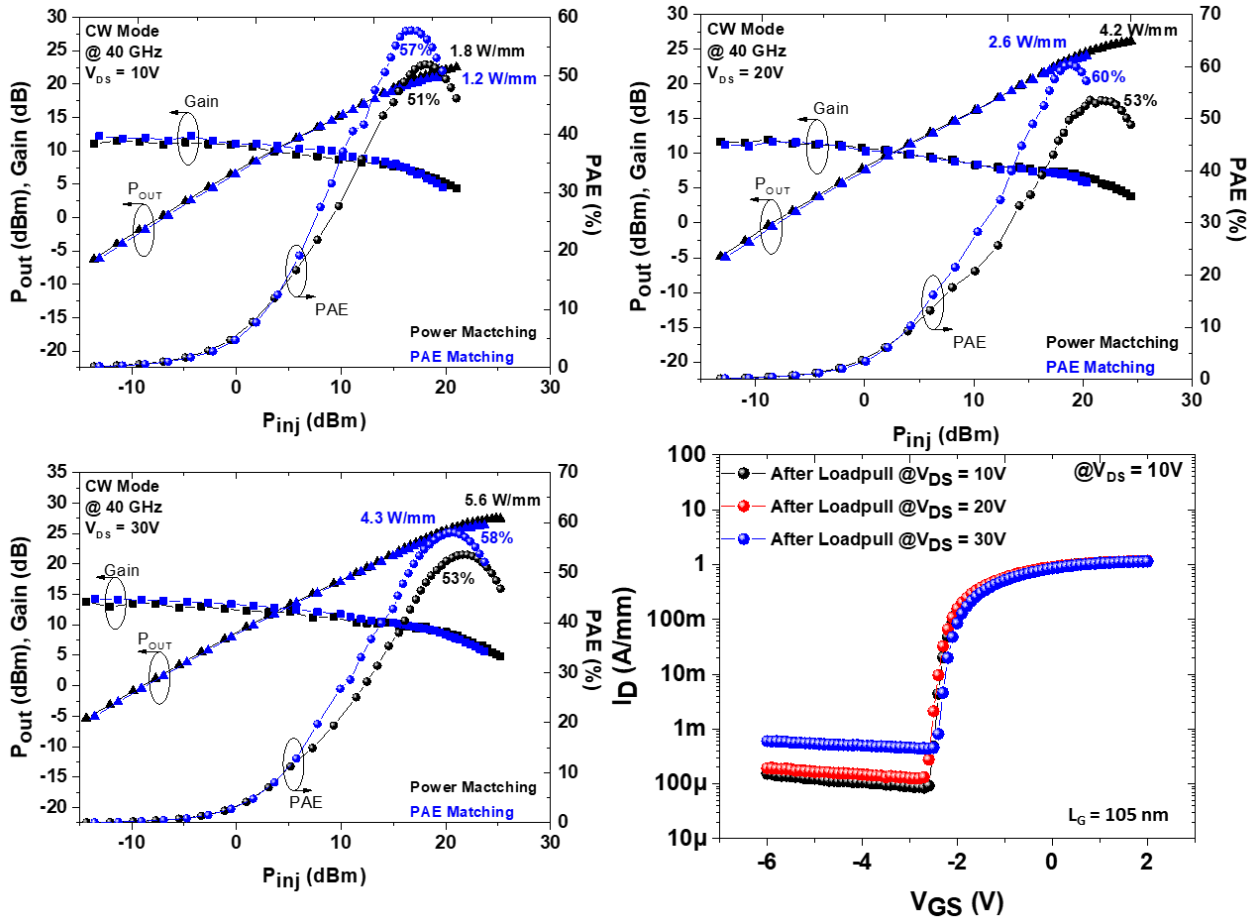


Figure.3.41. CW large signal performances at 40 GHz for 2×50 µm transistor with L_G = 105 nm and **L_{GD} = 0.5 µm** at V_{DS} = 10, 20, and 30V of the 3 nm AlN/GaN HEMT structure and transfer characteristics after load-pull sweeps up to V_{DS} = 30V.

3) Large signal characterization @40 GHz

Figure.3.41 shows 40 GHz CW power performances of a 2×50 µm transistor with L_G = 105 nm and L_{GD} = 0.5 µm from V_{DS} = 10V up to V_{DS} = 30V for the 3 nm AlN/GaN HEMT structure. A high PAE well-above 55% is observed up to V_{DS} = 30V with a saturated power density of 4.3 W/mm. With power matching, a PAE of 53% with a P_{OUT} of 5.6 W/mm are obtained. At V_{DS} = 20V, a PAE of 60% associated with a P_{OUT} of 2.6 W/mm is achieved. From the transfer characteristics after load-pull sweep, we observed no degradation of the transistors up to V_{DS} = 20V but at V_{DS} = 30V we notice an increase of the off-state current leakage.

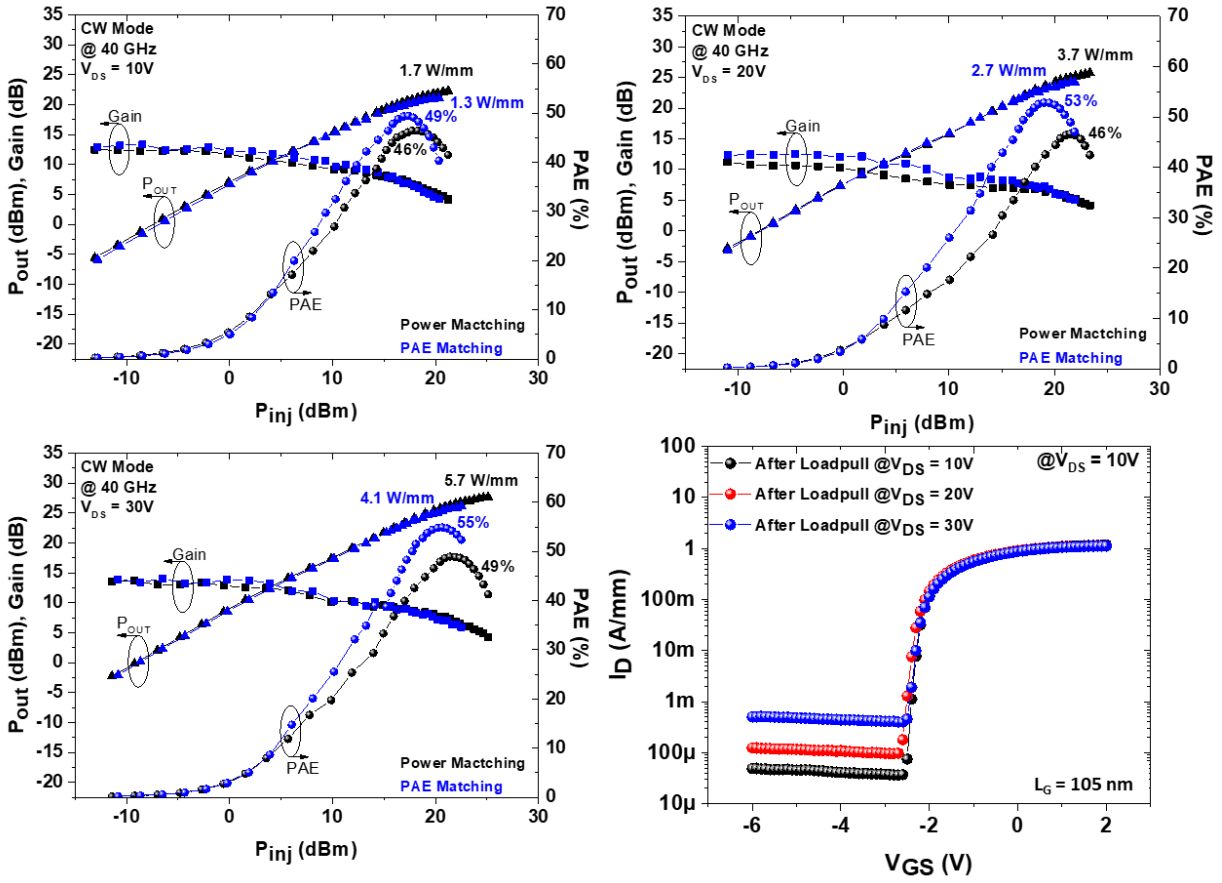


Figure.3.42. CW large signal performances at 40 GHz for 2×50 µm transistor with L_G = 105 nm and **L_{GD} = 1.5 µm** at V_{DS} = 10, 20, and 30V of the 3 nm AlN/GaN HEMT structure and transfer characteristics after load-pull sweeps up to V_{DS} = 30V.

Figure.3.42 shows 40 GHz CW power performances of a 2×50 µm with L_G = 105 nm and **L_{GD} = 1.5 µm** from V_{DS} = 10V up to V_{DS} = 30V for the 3 nm AlN/GaN HEMT structure. A PAE above 55% is observed up to V_{DS} = 30V with a saturated power density of 4.1 W/mm. At V_{DS} = 20V, a PAE of 53% with

a P_{OUT} of 2.7 W/mm are reached. With power matching, a PAE of 46% with a P_{OUT} of 3.7 W/mm are obtained. From the transfer characteristics after load-pull sweep, we observed no degradation of the transistor up to V_{DS} = 20V but at V_{DS} = 30V we observed an increase of the off-state current leakage. The various design fully confirms the attractive power results achieved at this frequency.

Figure.3.43 shows 40 GHz pulsed power performances of a 2×50 µm with L_G = 105 nm and **L_{GD} = 0.5 µm** from V_{DS} = 10V up to V_{DS} = 30V for the 3 nm AlN/GaN HEMT structure. A PAE above 70% is observed up to V_{DS} = 30V with a saturated power density of 5.1 W/mm. With power matching, a PAE of 65% associated to a P_{OUT} of 6.3 W/mm can be obtained. At V_{DS} = 20V, a record PAE of 72% associated with a P_{OUT} of 3.5 W/mm is reached. It can be noticed that up to V_{DS} = 20V, the devices show no degradation after the whole load-pull sweeps, but at V_{DS} = 30V, we observed an increase of the off-state current.

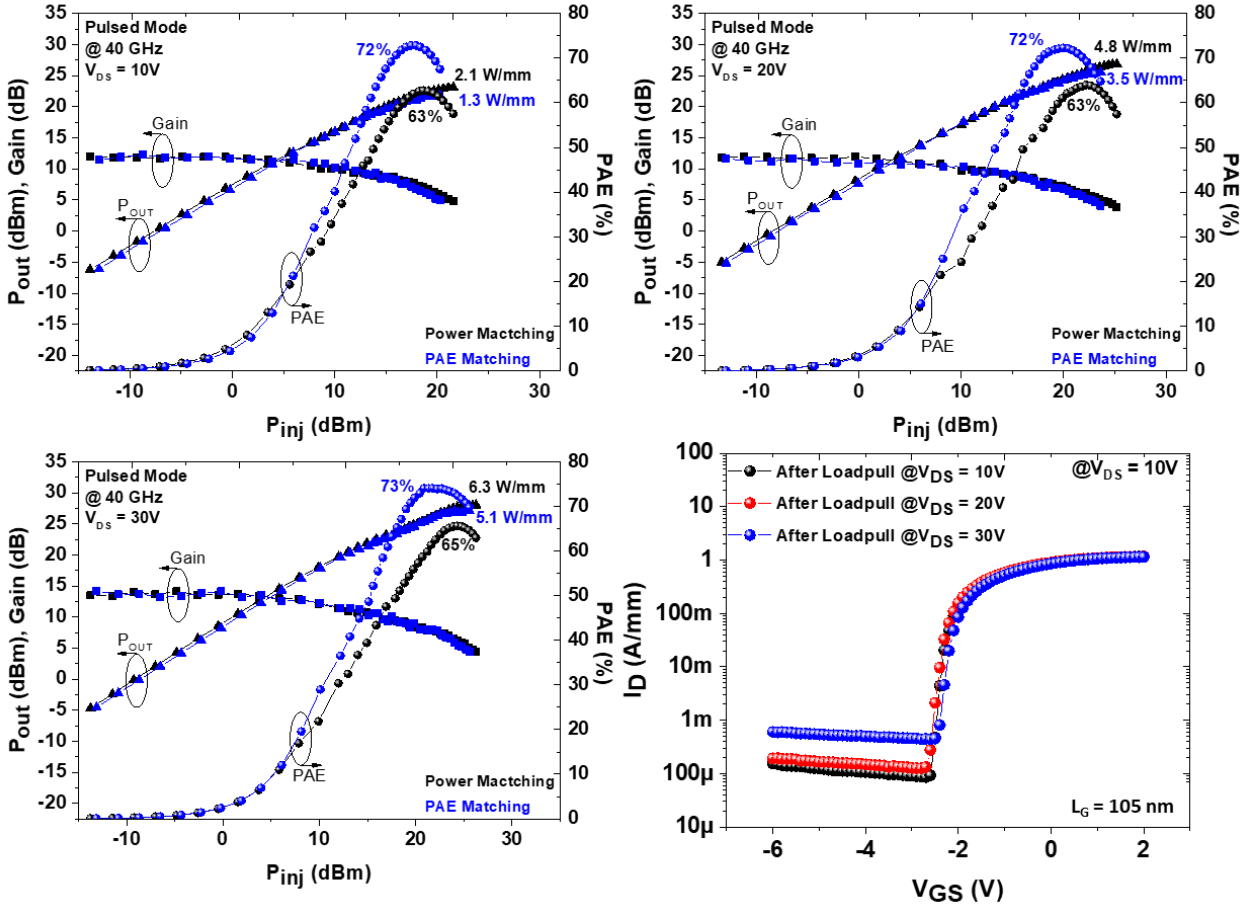


Figure.3.43. Pulsed large signal performances at 40 GHz for 2×50 µm transistors with L_G = 105 nm and **L_{GD} = 0.5 µm** at V_{DS} = 10, 20, and 30V of the 3 nm AlN/GaN HEMT structure and transfer characteristics after load-pull sweeps up to V_{DS} = 30V.

Figure.3.44 shows 40 GHz pulsed power performances of a 2×50 µm with L_G = 105 nm and **L_{GD} = 1.5 µm** from V_{DS} = 10V up to V_{DS} = 30V for the 3 nm AlN/GaN HEMT structure. A PAE above 70% is observed up to V_{DS} = 30V with a saturated power density of 5.2 W/mm with no degradation after several load-pull sweeps, confirming the outstanding achieved performances.

Figure.3.45 shows the large signal manual mapping across the 4-inch 3 nm AlN/GaN wafer. Several tenths of devices with similar design (2×50 µm, L_G = 105 nm, L_{GD} = 0.5 µm) have been measured across the wafer at 40 GHz with V_{DS} = 20 V under pulsed operation. We clearly observe an excellent yield and uniformity illustrated by a stable PAE/P_{OUT} combination (mean PAE ~ 70%, mean Pout ~ 25 dBm).

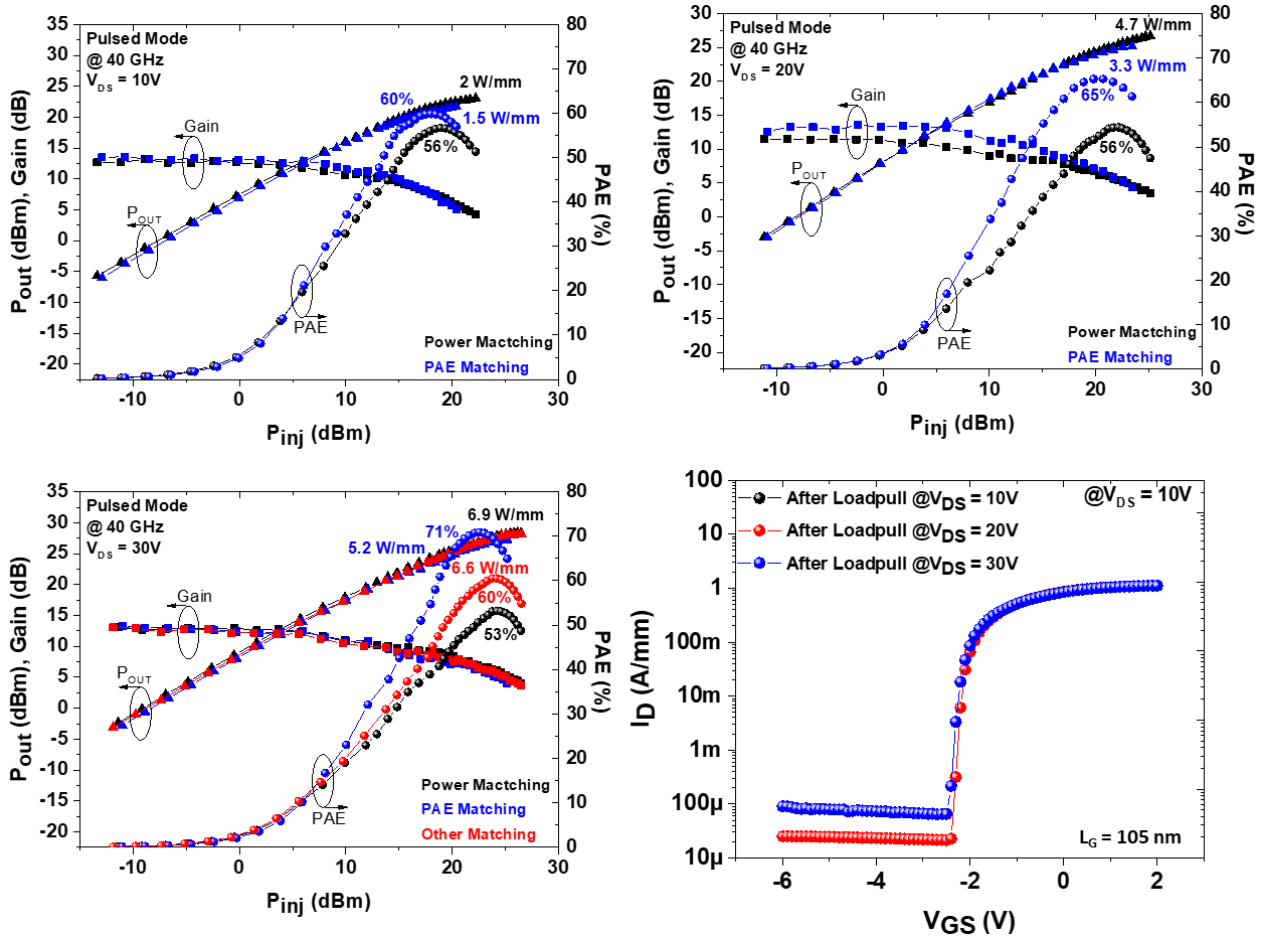


Figure.3.44. Pulsed large signal performances at 40 GHz for 2×50 µm transistor with L_G = 105 nm and **L_{GD} = 1.5 µm** at V_{DS} = 10, 20, and 30V of the 3 nm AlN/GaN HEMT structure and transfer characteristics after load-pull sweeps up to V_{DS} = 30V.

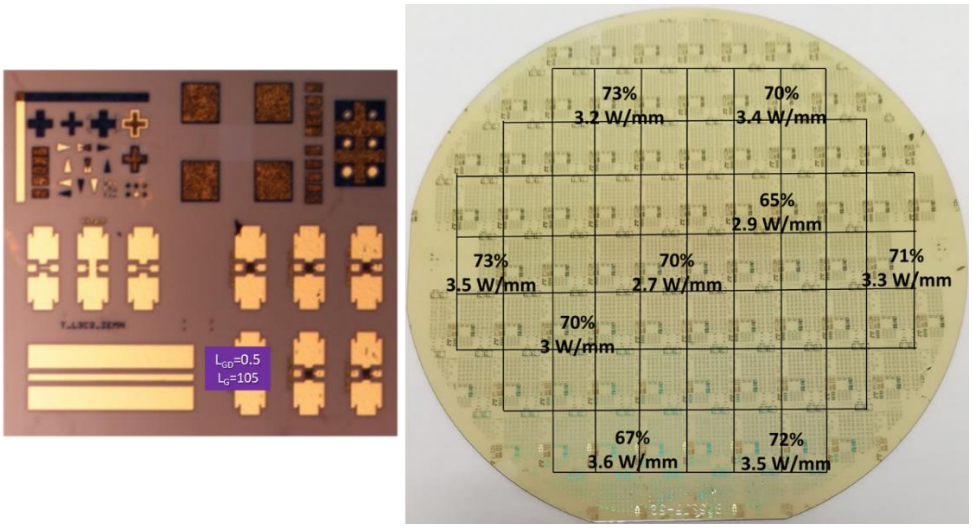


Figure.3.45. Pulsed large signal manual mapping at 40 GHz of 2×50 µm transistor with L_G = 105 nm and L_{GD} = 0.5 µm at V_{DS} = 20V of the 3 nm AlN/GaN HEMT structure

Despite the remarkable large signal performances, a strong impact of trapping effects appears through the gap between CW and pulsed load-pull measurements on these devices.

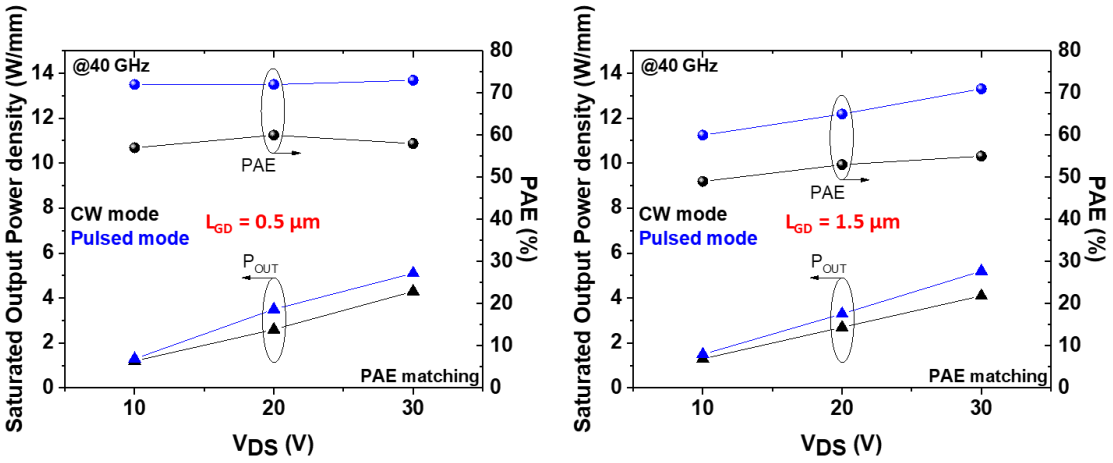


Figure.3.46. PAE and output power density (P_{OUT}) vs V_{DS} from pulsed and CW load-pull measurements of the 3 nm AlN/GaN HEMT structure.

4) Short term reliability at 40 GHz

Short-term on wafer RF step stress at 40 GHz has been carried out using various drain voltage and different temperature up to 140°C. 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm for the 3 nm AlN/GaN structure have been monitored at room temperature during 24 hours by steps of 8 hours under large signal conditions and at peak PAE as shown in **Figure.3.47**. Unlike the 4 nm AlN/GaN structure, the

3 nm AlN/GaN structure shows a stable output power density and PAE around 50% over 24 hours up to a drain voltage of V_{DS} = 20V with no degradation observed on the leakage current.

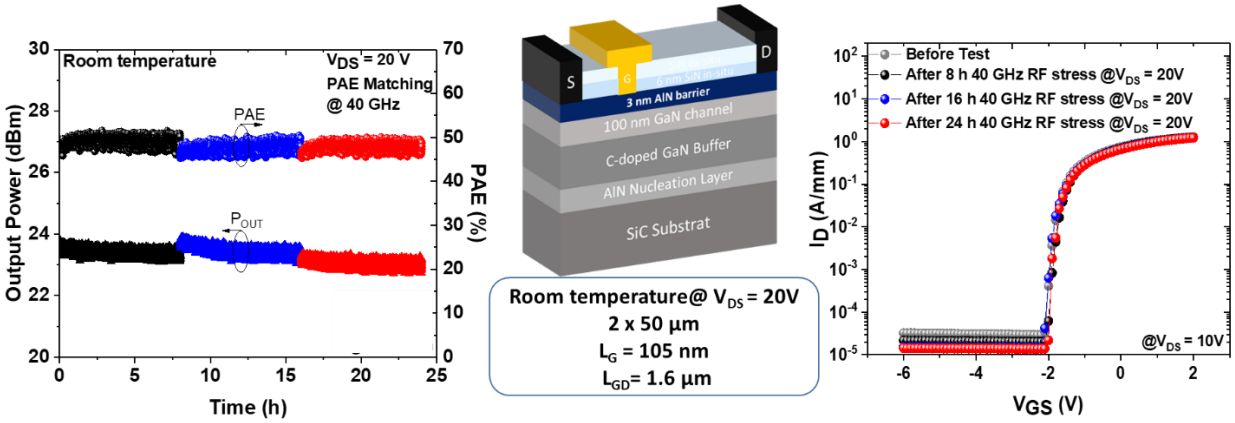


Figure.3.47. PAE and output power monitoring for 24 hours at room temperature on 2×50 µm transistor with L_G = 105 nm and L_{GD} = 1.5 µm at V_{DS} = 20V, (PAE matching), and transfer characteristics before and after 8, 16 and 24 hours of 40 GHz RF stress of the 3 nm AlN/GaN HEMT structure.

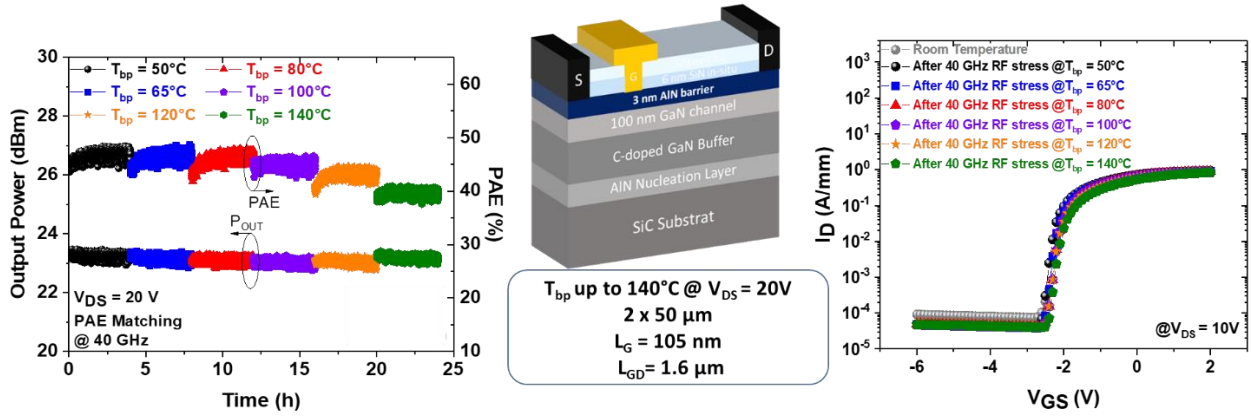


Figure.3.48. PAE and output power monitoring for 24 hours at several temperatures up to 140°C on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm at V_{DS} = 20V, (PAE matching), and transfer characteristics before and after 4 hours after each temperature for the 3 nm AlN/GaN HEMT structure.

In order to further assess the robustness of this structure, we also performed short-term on wafer RF stress at high temperature. Thus, the base-plate temperature (T_{bp}) has been increased up to 140°C by steps of 4 hours while using identical RF stress conditions at 40 GHz in order to observe the temperature impact on the RF performances. It worth noticing that the estimated junction temperature in this case is well-above 250°C as assessed on similar structure based on Raman measurements [65]. **Figure.3.48** shows a slight decrease of the PAE as a function of temperature from 47% at T_{bp} = 50°C down to 40% at T_{bp} = 140°C. This reduction is due to the thermal impact on the electron mobility as expected from any

semiconductors, which affects the gain, and thus the PAE. On the other hand, the output power density remains stable owing to the gate voltage adjustment at each T_{bp} in order to maintain the drain current at 100 mA/mm. From I_D (V_{DS}) characteristics we observed that no degradation occurs on the drain leakage current after all stress tests up to T_{bp} = 140°C. It can be noticed that the PAE is fully stable during the 4 hours stress at each temperature.

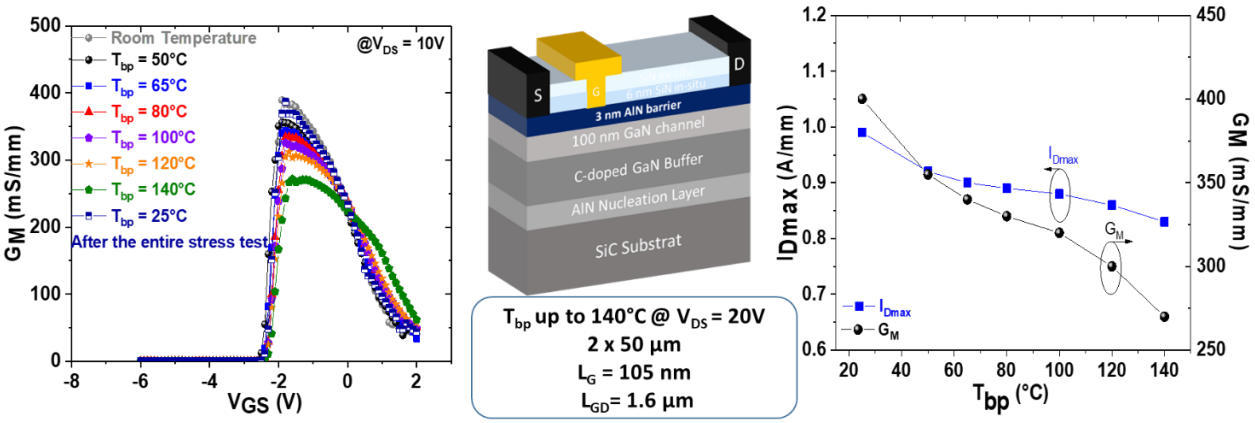


Figure.3.49. Evolution of the transconductance G_m and the $I_{D\,max}$ as a function of temperature after 40 GHz RF stress on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm of the 3 nm AlN/GaN HEMT structure

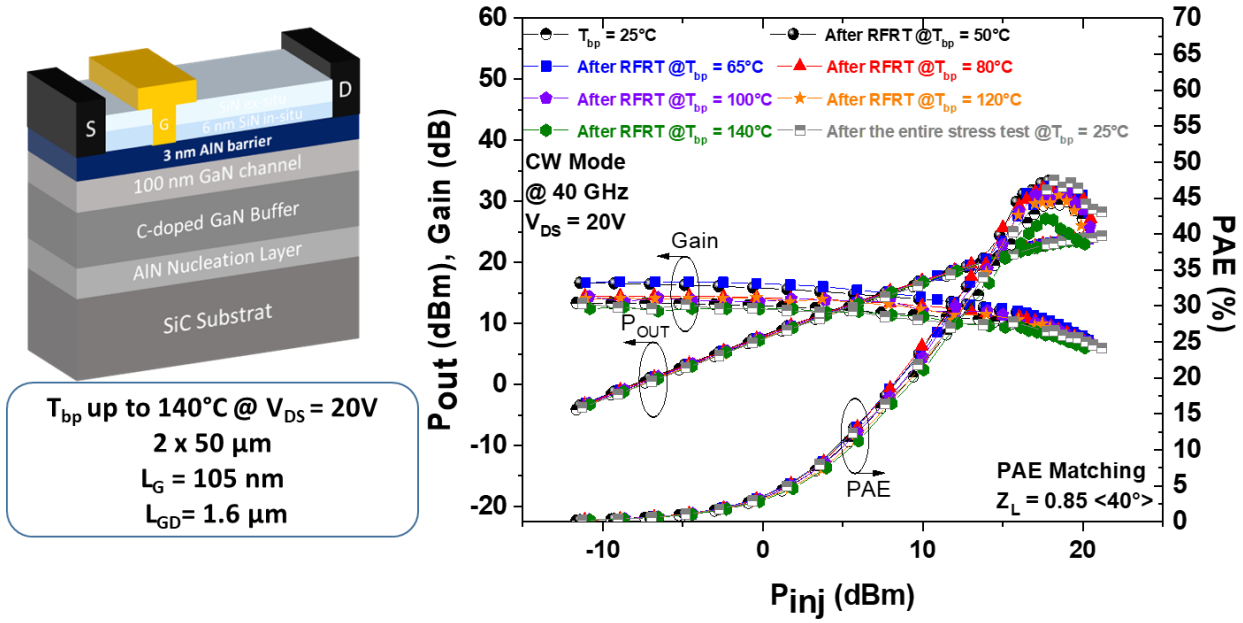


Figure.3.50. CW large signal performances at 40 GHz after each temperature up to 140°C on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm of the 3 nm AlN/GaN HEMT structure

Figure.3.49 shows the evolution of the transconductance and the open channel drain current as a function of temperature after each RF stress. As expected, the transconductance and the drain current decrease with temperature due to the drop of the electron mobility. It can be pointed out that after the entire test of 24 hours at several temperatures, the initial PAE value is recovered as shown in **Figure.3.50**.

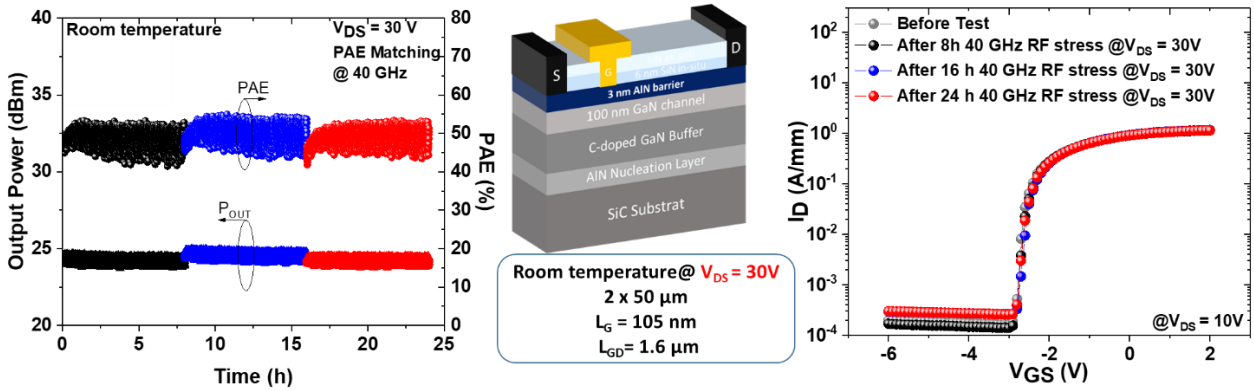


Figure.3.51. PAE and output power monitoring for 24 hours at room temperature on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm at **V_{DS} = 30V**, (PAE matching), and transfer characteristics before and after 8, 16 and 24 hours of 40 GHz RF stress of the 3 nm AlN/GaN HEMT structure.

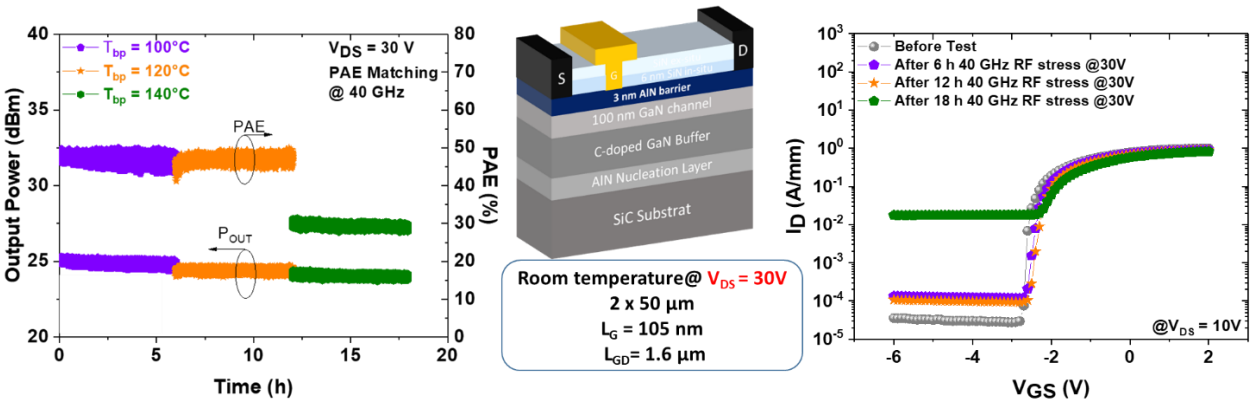


Figure.3.52. PAE and output power monitoring for 24 hours at several temperatures up to 140°C on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm at **V_{DS} = 30V**, (PAE matching), and transfer characteristics before and after 4 hours after each temperature for the 3 nm AlN/GaN HEMT structure.

40 GHz RF stress has also been performed at higher drain voltage (V_{DS} = 30V) for the 3 nm AlN/GaN HEMT structure. A PAE of 50% with a P_{OUT} around 3 W/mm combination remains stable with no increase of gate and drain leakage currents at room temperature as shown in **Figure.3.51**. It is interesting to note that even at high drain voltage of V_{DS} = 30V, the 3 nm AlN/GaN HEMT structure allows excellent

large signal performances with no degradation of the device over time. This reflects the high quality of both growth and device processing.

The same test has been performed at higher temperature up to 140° base plate. At 120°C for 6 hours, the devices still show almost no degradation, which can be seen in the transfer characteristics shown in **Figure.3.52** and a stable combination of PAE / P_{OUT} of 50% / 3 W/mm, respectively. However, at 140°C the transistor immediately degrades reflected by a huge increase of the off-state drain current > 10 mA/mm leading to a strong drop of the PAE from 50% down to 30%. It can be noticed that the degradation has no impact on the output power density, which remains stable around 3 W/mm at 140°C during the 4 hours. This shows that the self-heating is not dominant despite the high junction temperature.

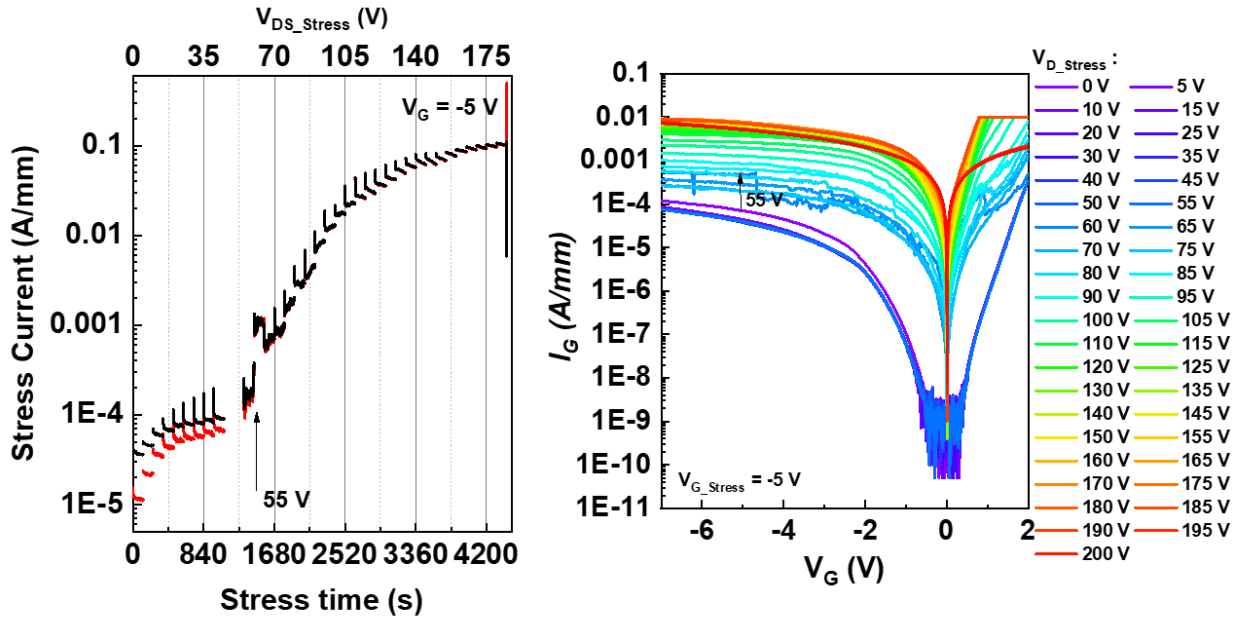


Figure.3.53. off-state drain step stress on 2×50 µm transistor with L_G = 110 nm, L_{GD} = 1.5 µm of the 3 nm AlN/GaN HEMT structure

1) DC short term reliability performed at the University of Padova

In order to further assess the robustness of the 3 nm AlN/GaN structure, parametric degradation and breakdown effect during V_{DS} step stress tests at off-state and semi-on state has been performed at the University of Padova.

The robustness tests have been carried out on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm from the 3 nm AlN/GaN structure. The first tests correspond to a step stress in off-state (pinch voltage: V_{GS} = -5V). Gate and drain current are monitored at several drain voltages up to V_{DS} = 200V (each V_{DS} stress

is maintained for 2 min). We observed a degradation starting at a drain voltage of V_{DS} = 55V even though the leakage currents remain well below 1 mA/mm (see **Figure.3.53**). It can also be noted that the transistor can withstand a drain voltage of 200V without degradation.

The second test corresponds to a step stress in semi-on state (at V_{GS} = -1V corresponding to a 0.4 A/mm). The on-state and the leakage currents are monitored at several stress voltages V_{DS}. The observed decrease of the on-state current corresponding to a shift in the pinch voltage is due to the trapping effects and self-heating. Similarly, to the off-state stress, we observed a significant degradation of the gate leakage current beyond V_{DS} = 55V (see **Figure.3.54**). It can be noticed that further stress tests have been performed in on-state (V_{GS} = 0V) on this structure which are explained in details in [158].

In conclusion, the 3 nm AlN/GaN structure shows superior robustness in off-state and semi-on state compared to the 4 nm AlN/GaN structure. Therefore, the DC reliability assessment is thus in agreement with RF short-term reliability performed on these structures.

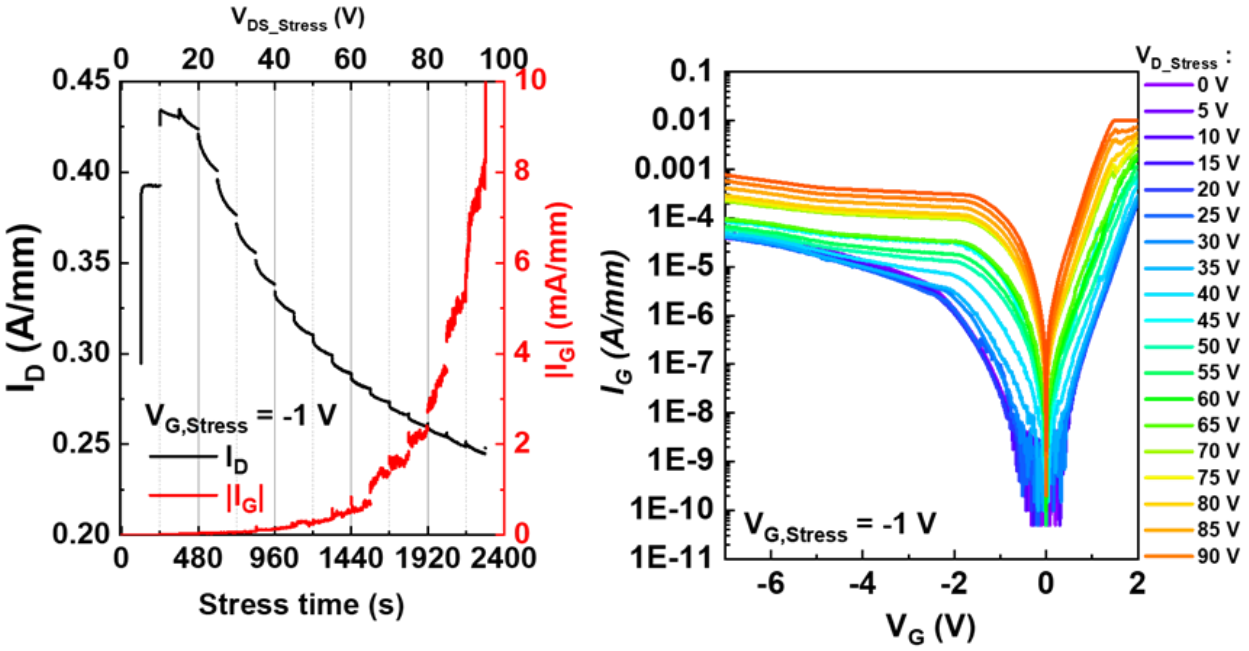


Figure.3.54. Semi-on-state drain step stress on 2×50 µm transistor with L_G = 105 nm, L_{GD} = 1.5 µm of the 3 nm AlN/GaN HEMT structure

III.3.1.3. Comparison between 3 nm and 4 nm AlN/GaN structures

We performed a comparison between two AlN/GaN HEMT structures on 4-inch SiC substrate using a 3 nm and 4 nm AlN barrier thickness. The power performances of both structures demonstrated the benefit

of ultrathin AlN barrier layer. However, despite the attractive RF performances of the 4 nm AlN/GaN HEMT structure, we observed a strong degradation after large signal measurements at room temperature at V_{DS} = 12V and an instantaneous degradation for higher V_{DS}. On the other hand, the 3 nm AlN/GaN HEMT structure delivered unprecedented power performances at 40 GHz while showing a promising device robustness. Indeed, short-term reliability shows no degradation up to V_{DS} = 30V during 24 hours at room temperature. At high temperature up to 140°C the 3 nm AlN/GaN structure remains fully stable at V_{DS} = 20V. At V_{DS} = 30V, the transistor shows degradation at 140°C associated with an off-state drain current degradation and a PAE drop from 50% down to 30%. **Figure.3.55** presents a summary and comparison of the RF performances of the 3 nm and 4 nm AlN/GaN HEMTs.

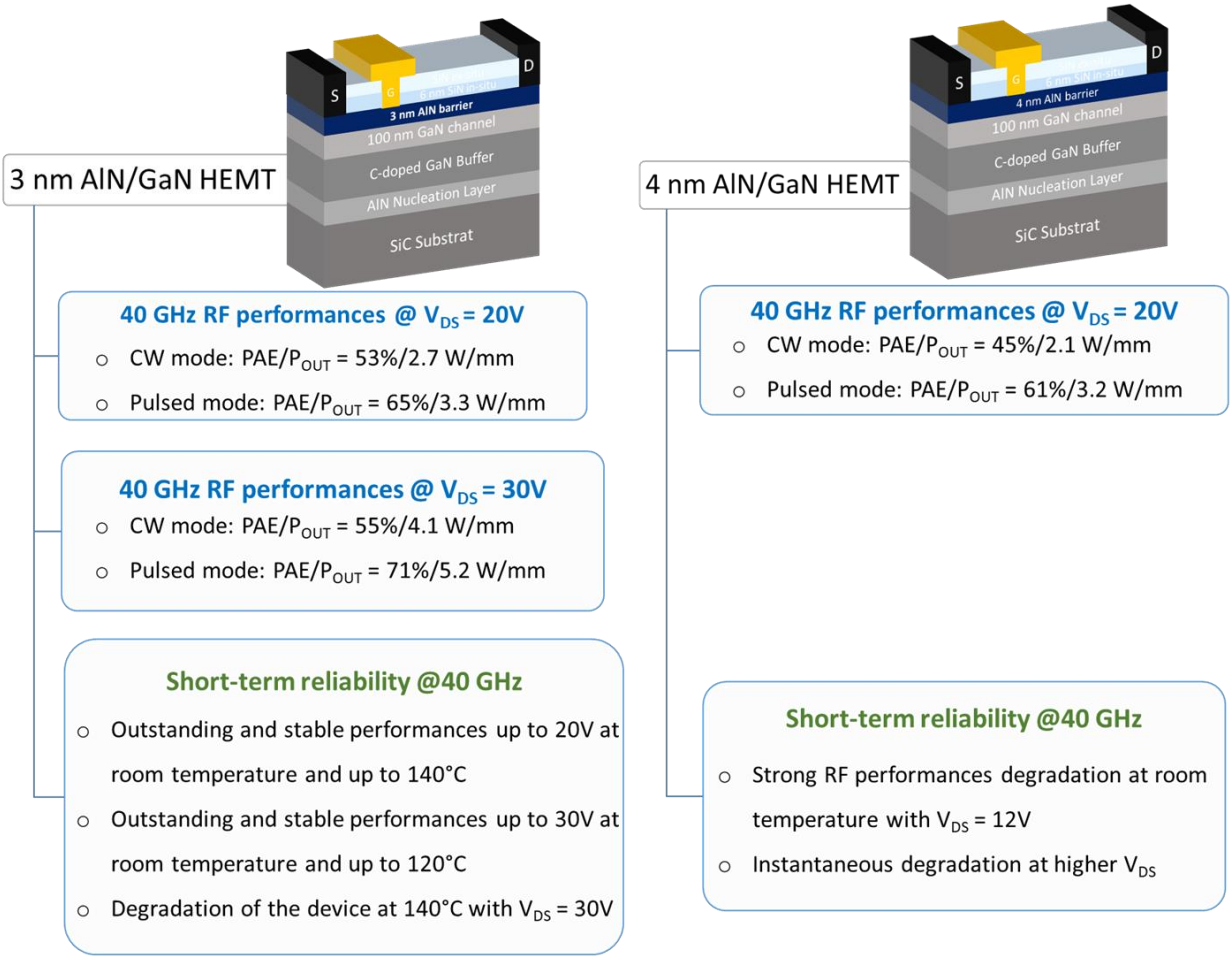


Figure.3.55. Schematic summary and comparison between the RF performances of the 3 nm and 4 nm AlN/GaN HEMT structures

The comparison between the 3 nm and 4 nm AlN/GaN structures shows superior robustness and RF performances in both CW and pulsed mode (see **Figure.3.56**) for the thinner barrier layer attributed mainly

to the high structural quality of the 3 nm AlN barrier resulting in an increased safe operating area under harsh conditions. In order to further understand the different electrical behavior between the 2 structures, HRTEM has been performed which will be discussed in the next section.

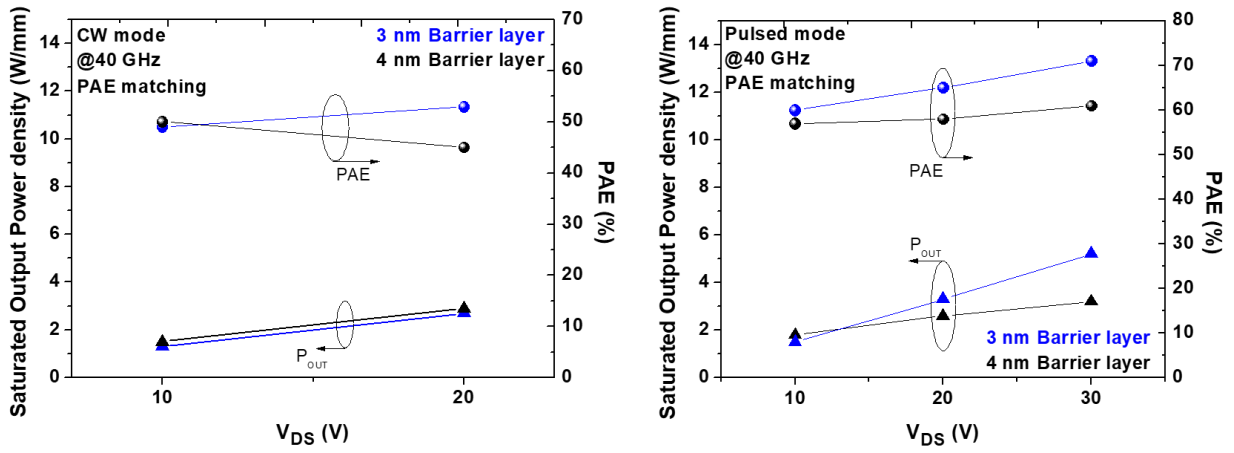


Figure.3.56. PAE and output power density (P_{OUT}) vs V_{DS} in CW and pulsed mode of the 3 nm and 4 nm AlN/GaN HEMT structures

III.3.1.4. Structural characterization of 3 nm and 4 nm AlN/GaN structures

In order to better understand such a different electrical behavior between the 3 nm and 4 nm AlN/GaN HEMT structure, we performed High Resolution Transmission Electron Microscopy (HRTEM) structural characterization on both epitaxial structures. Moreover, we also performed HRTEM on the fabricated 3 nm AlN/GaN transistors in order to assess the gate/barrier layer interface. The thin lamella preparation for the TEM study was carried out at IEMN using Focused Ion Beam (FIB) method. The samples were then sent to C2N laboratory in order to perform TEM analysis.

1) Al-distribution in the epitaxial structures

- **4 nm AlN/GaN structure**

The 4 nm AlN/GaN structure were investigated by Scanning Transmission Electron Microscopy (STEM). **Figure.3.57** shows high-angular annular dark field (HAADF) and Energy Dispersive X-ray (EDX) mapping images of the 4 nm AlN/GaN structure. With this method, we can identify different epitaxial layers highlighted by various contrasts from the HAADF image. The elemental composition of the material structure consists in Ga, Al, and Si atoms, which are homogeneously dispersed as shown in the EDX mapping images. We also observed an oxide on the surface due to the oxidation of the SiN cap layer. It can be noticed that the carbon observed in the material is deposited during the thin lamella preparation

by FIB. The EDX images reveal an unexpected Al-distribution. Indeed, the structure exhibits a blurred interface showing an AlGaN transition region between the GaN and AlN layers. Therefore, the total thickness of the barrier layer in this case is close to 10 nm (much more than the nominal 4 nm, taking into account this transition layer).

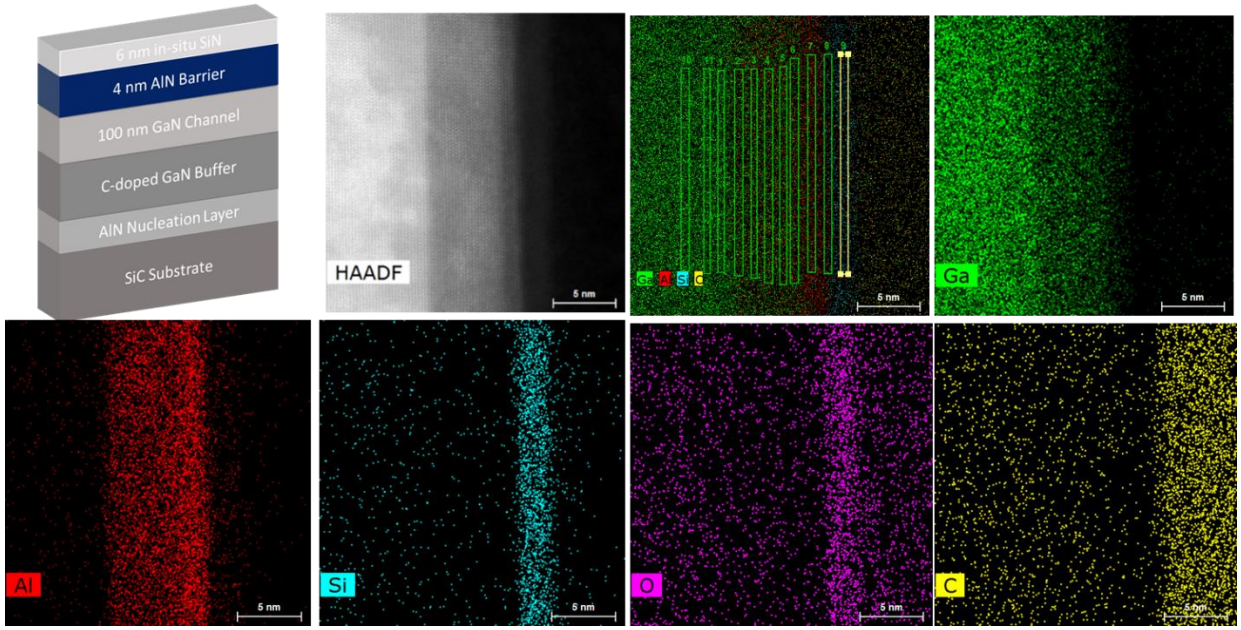


Figure.3.57. Energy Dispersive X-ray (EDX) mapping of the 4 nm AlN/GaN structure

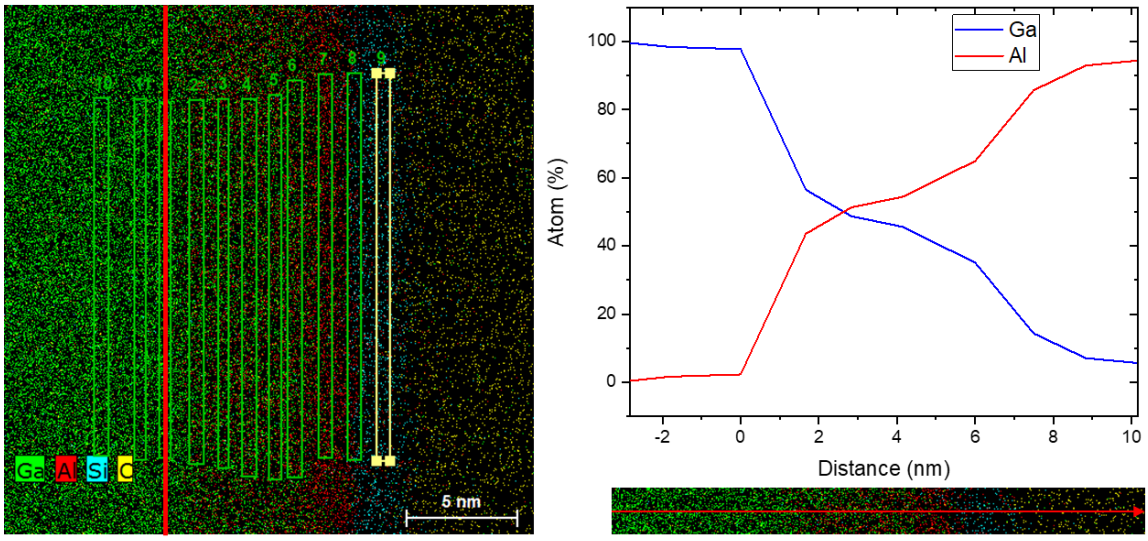


Figure.3.58. Al and Ga-distribution within the 4 nm AlN/GaN structure

The corresponding EDX-profile are shown in **Figure.3.58** with the y-axis showing the total atomic percentage of the Al and Ga compound. We can distinct three regions from this plot: the region of the GaN

channel with 100% Ga atoms, then the transition region with 54% Ga (on average), and finally, a quasi-pure AlN barrier with ~ 90% Al and a low Ga atom of ~ 5%. In fact, the 4 nm AlN/GaN structure exhibits a "slow" transition from Ga to Al, most probably due to the MOCVD tool configuration.

- **3 nm AlN/GaN structure**

Figure.3.59 shows HAADF and EDX mapping images of the 3 nm AlN/GaN structure. The different epitaxial layers were identified in the same way by various contrasts from the HAADF image. The elemental composition of the material structure shows Ga, Al, and Si, which are homogeneously dispersed as shown in the EDX mapping images. Similar to the 4 nm AlN/GaN structure, the oxide observed on the surface is due to the oxidation of the SiN cap layer while the carbon shown in the material is deposited during the thin lamella preparation by FIB. In contrast to the 4 nm AlN/GaN structure, we observed from the EDX images that the 3 nm AlN/GaN exhibits a much sharper interface between the GaN and AlN layers.

The corresponding EDX-profile are shown in **Figure.3.60** with the y-axis showing the total atomic percentage of the Al and Ga compound. The 3 nm AlN/GaN structure exhibits a "faster" transition from Ga to Al. The maximum Al atoms after the transition between Ga and Al for this structure is about 85% with 15 to 20% Ga atoms.

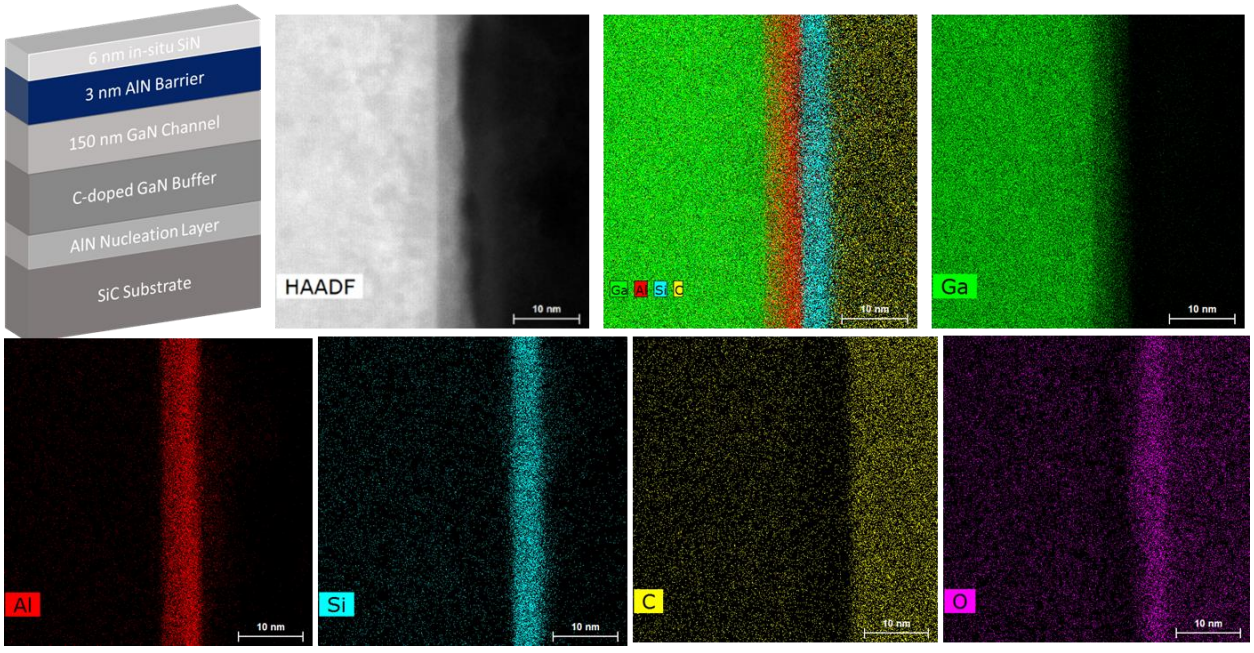


Figure.3.59. Energy Dispersive X-ray (EDX) mapping of the 3 nm AlN/GaN structure

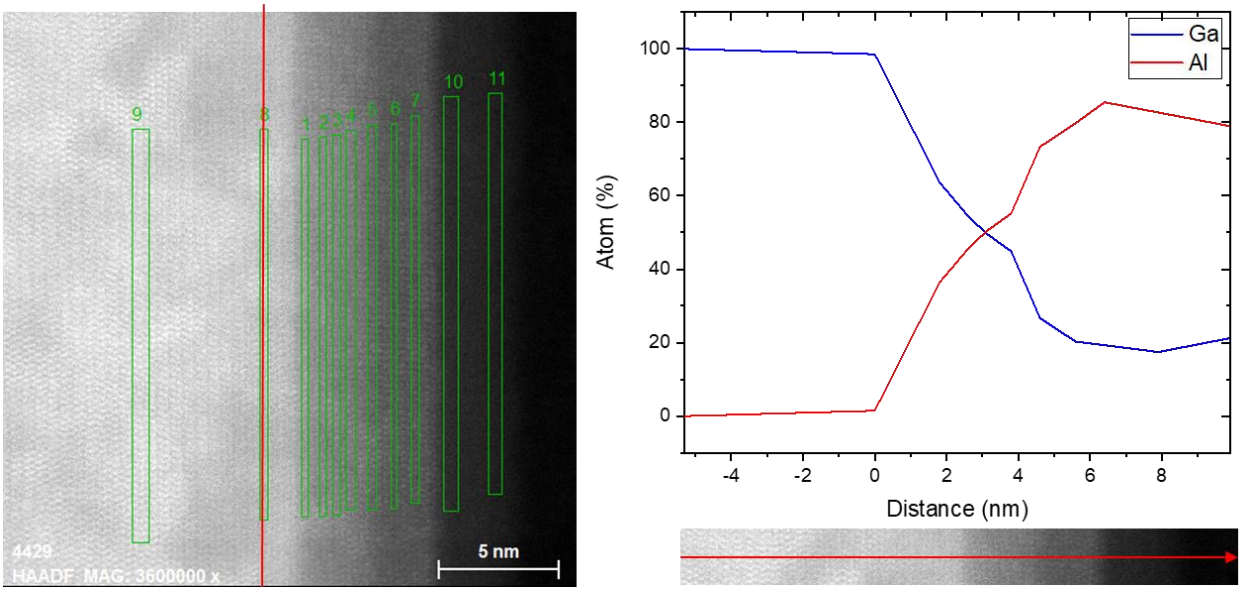


Figure.3.60. Al and Ga-distribution in the 3 nm AlN/GaN structure

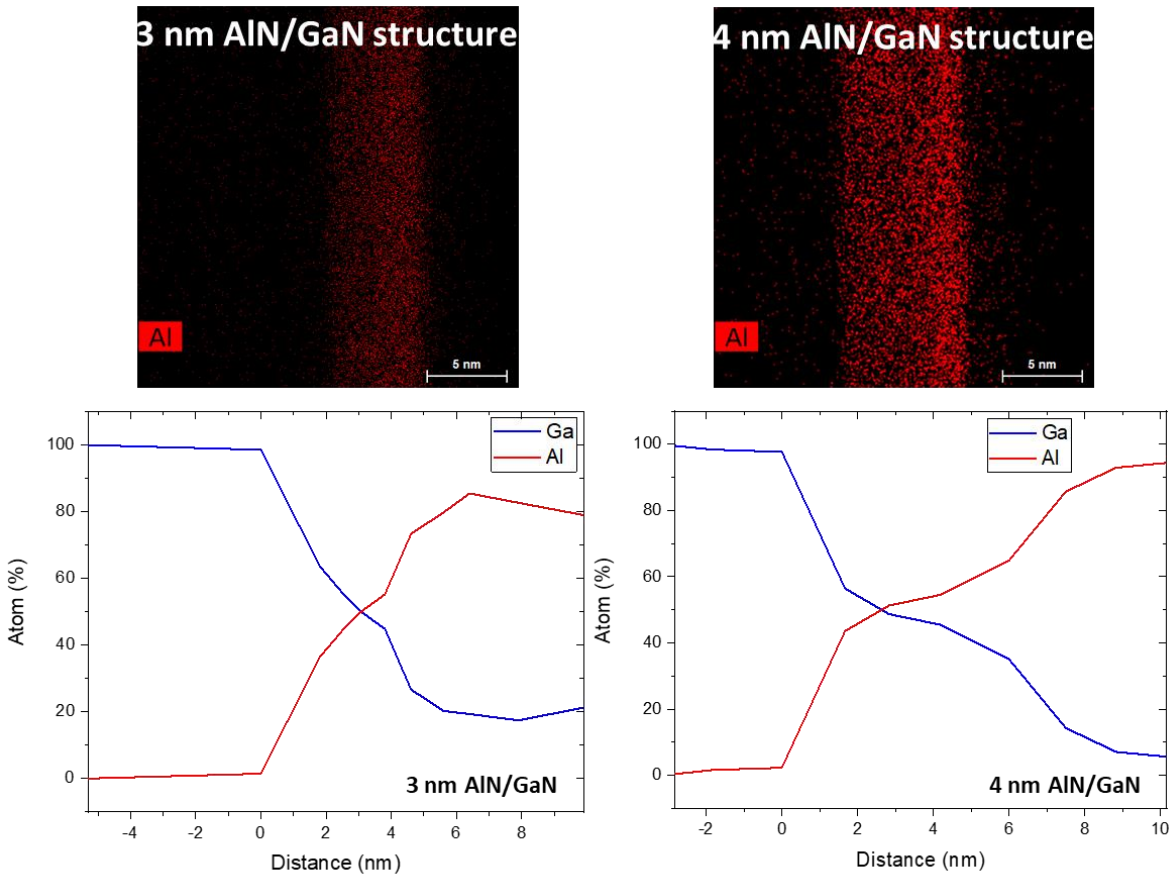


Figure.3.61. Comparison between the Al and Ga-distribution between the 3 nm and 4 nm AlN/GaN structures

1) Results comparison

The comparison between HRTEM analyses between the 3 nm and 4 nm AlN/GaN structures (see **Figure.3.61**) unveils a significantly different Al-distribution for each structure. There is a much sharper interface for the 3 nm AlN/GaN structure, whereas the Al-distribution observed for the 4 nm AlN/GaN exhibits an exponential profile with a slow transition from the Ga to Al due to the memory effects during the MOCVD growth at high temperature. This results in a large Al-rich AlGaN transition layer in this case. However, Al-rich AlGaN alloys are known to be rather instable, especially when grown by MOCVD thus explaining the performance degradation of devices.

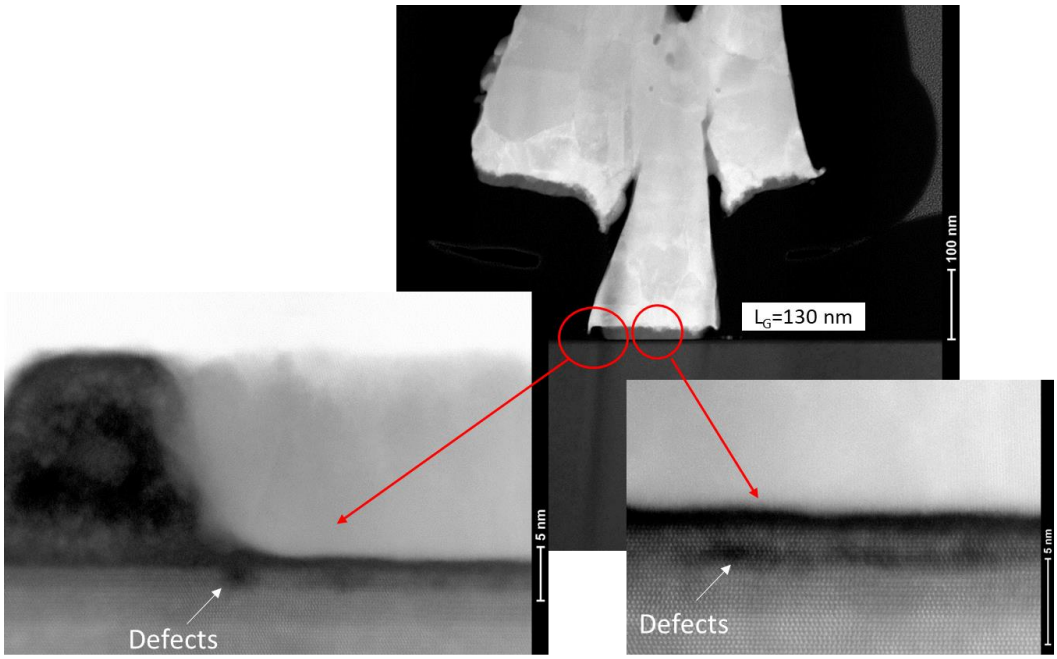


Figure.3.62. HRTEM images of the gate showing the defects at the gate/barrier layer interface

1) TEM analysis on the 3 nm AlN/GaN HEMT

In order to analyze the gate/barrier layer interface, which can be at the origin of surface trapping effects (gate lag), we performed HRTEM on the 3 nm AlN/GaN transistors. A gate length of L_G = 130 nm as shown in **Figure.3.62** has been analyzed. It can be noticed that the gate processing on these devices was performed using SF_6 plasma ICP etching prior to Ni/Au metal stack deposition. We can clearly see at the gate/barrier layer interface a high dislocation density identified by a strong contrast, which is due to the defects introduced during the ICP gate etching.

Figure.3.63 shows HAADF and EDX mapping images of the gate/barrier layer interface. The elemental composition shows Ni, Au, Si, and the unexpected F atoms, which are dispersed at the interface as shown in the EDX mapping images. The thin film of Si-atoms observed at the gate/barrier layer interface confirms that the SiN underneath the gate is not fully etched. On the other hand, the undesirable F-atoms are due to the Fluorine plasma ion implantation during the SF_6 plasma etching, which results in a degradation mechanism. It has been indeed demonstrated that the fluorine implantation in the gate region induces a channel local depletion under the gate thus leading to a shift of the threshold voltage [159].

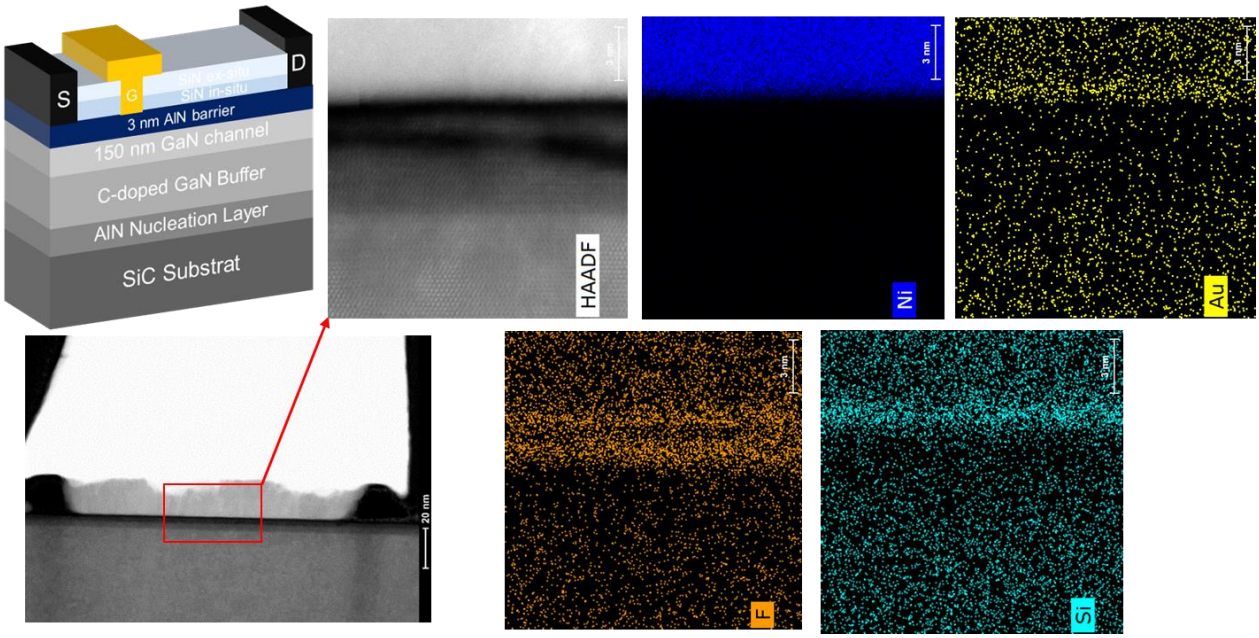


Figure.3.63. Energy Dispersive X-ray (EDX) mapping of the 3 nm AlN/GaN HEMT

III.3.1.5. 3 nm AlN/GaN wafer characterization after UMS back-end processing

After full IEMN process and characterization, the wafer was sent to UMS in order to process larger devices as shown in **Figure.3.64**. After receiving the epi-wafer back at IEMN, the first step was to evaluate the passives and back-end processing impact on PCM performances.

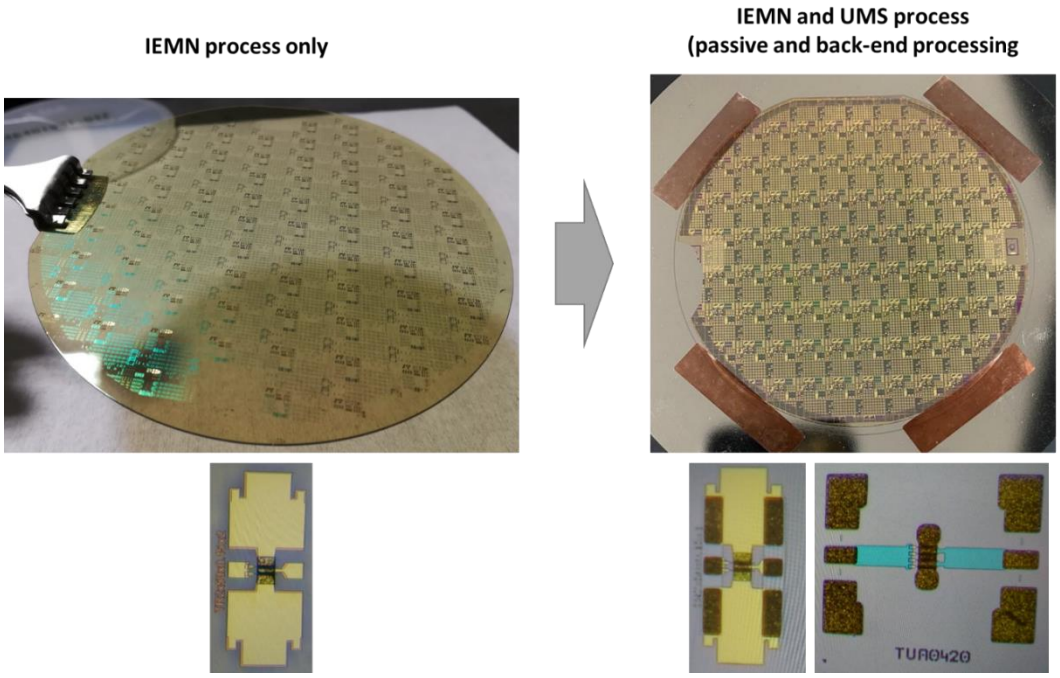


Figure.3.64. Photos of the 3 nm AlN/GaN epi-wafer before and after UMS passives and back-end processing

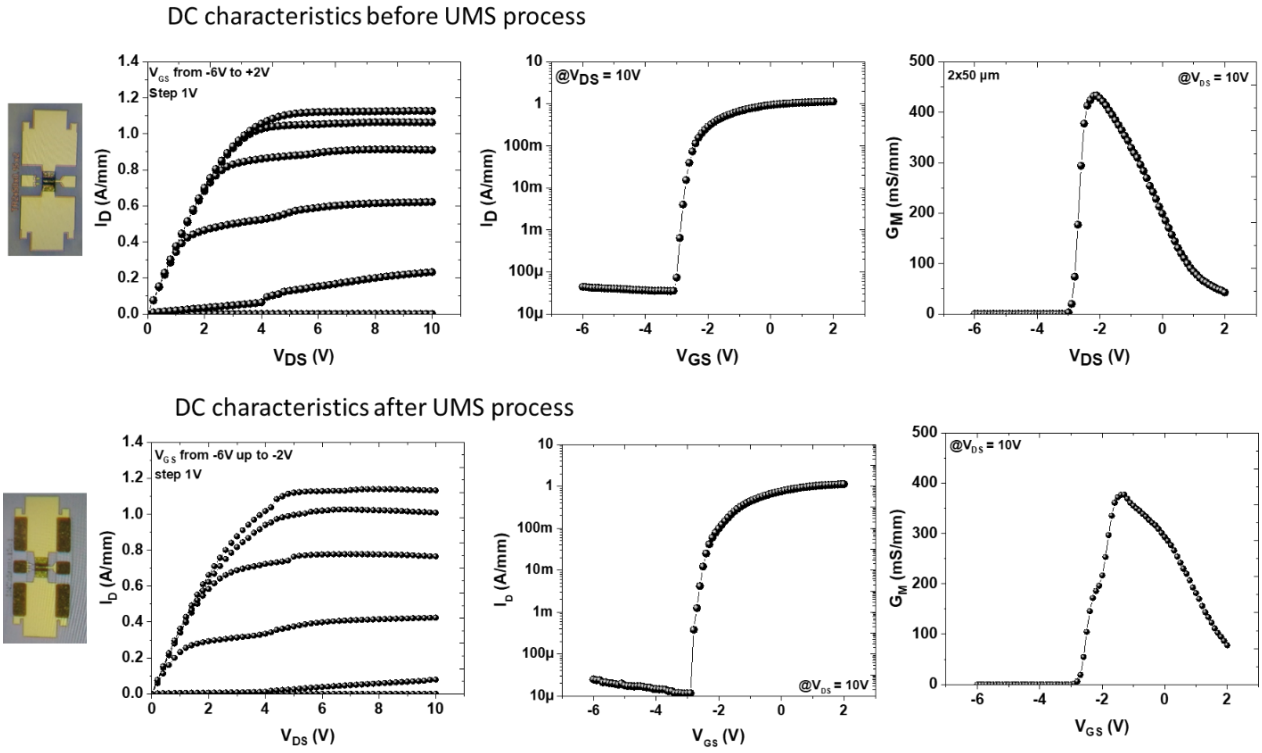


Figure.3.65. DC characteristics of IEMN PCMs before and after UMS process on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 0.5 µm for the 3 nm AlN/GaN HEMT structure

1) DC and small signal characterization

Transconductance, transfer and output characteristics are shown in **Figure.3.65** before and after UMS process on 2×50 µm transistor with L_G = 105 nm and L_{GD} = 0.5 µm. All characteristics have been measured after a burn-in step. A pinch-off voltage of about V_{th} = -2.9V has been observed with a gate leakage current below 100 µA/mm. An $I_{D\ max}$ of 1.1 A/mm (@ V_{GS} = +2V) and a Gm around 450 mS/mm have been measured. After UMS processing DC performances remains quite similar. In order to confirm the low impact of UMS processing on DC characteristics a manual mapping has been performed which confirms that the DC performances remain the same across the 4-inch wafer.

	2x50 µm	Before UMS processing			After UMS processing		
	V_{DS}	10V	15V	20V	10V	15V	20V
GD0.6	F_t (GHz)	81	75	73	55	52	50
	F_{max} (GHz)	195	200	210	140	150	155
	U_{max} (dB)	13.6	13.9	14.5	10.8	11.3	11.4

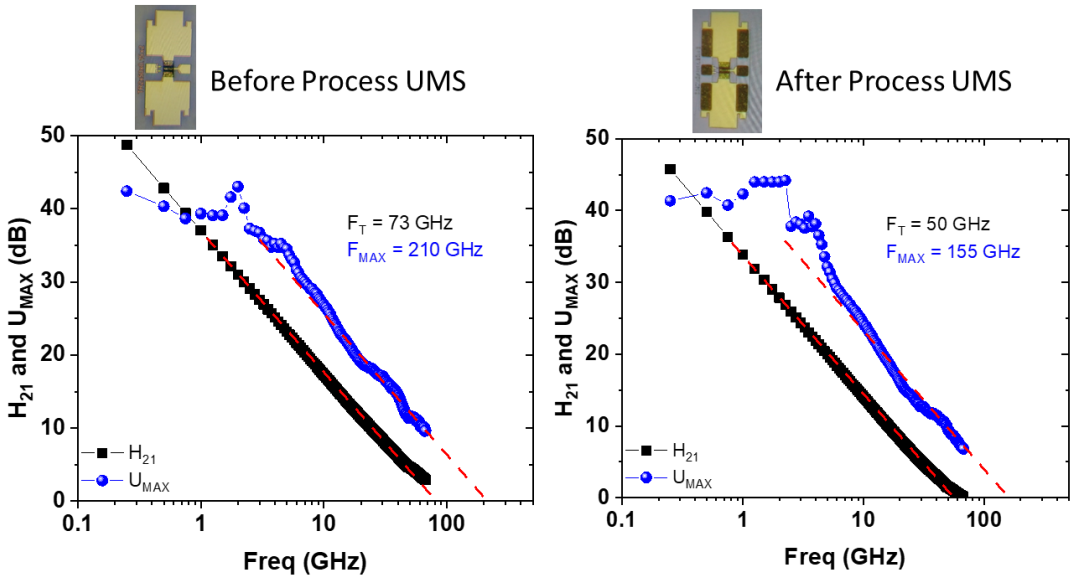


Figure.3.66. Small signal characteristics of IEMN PCMs before and after UMS process on 2×50 µm transistors with L_G = 105 nm and L_{GD} = 0.5 µm for the 3 nm AlN/GaN structure

Small signal characteristics have been measured on several devices across the wafer. A f_t/f_{max} around 50/150 GHz are observed for a 2×50 µm transistor with L_G = 105 nm and L_{GD} = 0.6 µm at V_{DS} = 20V compared to 75/210 GHz before UMS processing as shown **Figure.3.66**. We observed clearly this time a drop of small signal performances with a gap of 3 dB between the small signal Gain at 40 GHz

before and after UMS processing. This drop can be explained by the parasitic capacitance as well as the decrease of the extrinsic Gm resulting from the extra passivation needed for the back-end processing.

We also performed small signal measurements of multi-finger transistors from the same wafer. A constant f_t/f_{max} around 50/130 GHz for the various designs has been measured with L_G = 105 nm and L_{GD} = 1.5 µm at V_{DS} = 20V as shown in **Figure.3.67**. Gains are similar to IEMN PCM after UMS processing suffering also from parasitic capacitances. A change in the nature of the extra passivation helped to solve this issue (not shown in the manuscript) and enabled a decrease of only 0.5 dB after full processing.

		2x50 µm			4x50 µm		
	V_{DS}	10V	15V	20V	10V	15V	20V
L_{GD} = 1.5	F_t (GHz)	50	47	45	60	58	53
	F_{max} (GHz)	130	135	135	125	130	130
	U_{max} (dB)	10.6	10.9	11	9.9	10.1	10.2
		6x30 µm			6x50 µm		
	V_{DS}	10V	15V	20V	10V	15V	20V
L_{GD} = 1.5	F_t (GHz)	60	52	47	65	60	55
	F_{max} (GHz)	130	135	135	120	125	125
	U_{max} (dB)	10.7	10.8	11	9.6	10	10

Figure.3.67. Small signal characteristics of UMS PCMs on 2×50, 4×50, 6×30 and 6×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm for the 3 nm AlN/GaN structure

2) Large signal characterization

i. 2×50 µm IEMN PCMs after back-end processing

The comparison between both PAE and P_{OUT} performances between IEMN PCMs before and after UMS processing is presented in **Figure.3.68**. The significant drop of the PAE after UMS processing reflects the parasitic capacitances added after back-end processing and SiN extra-passivation. This gap in term of the PAE confirms the small signal decrease observed on the transistors after UMS process.

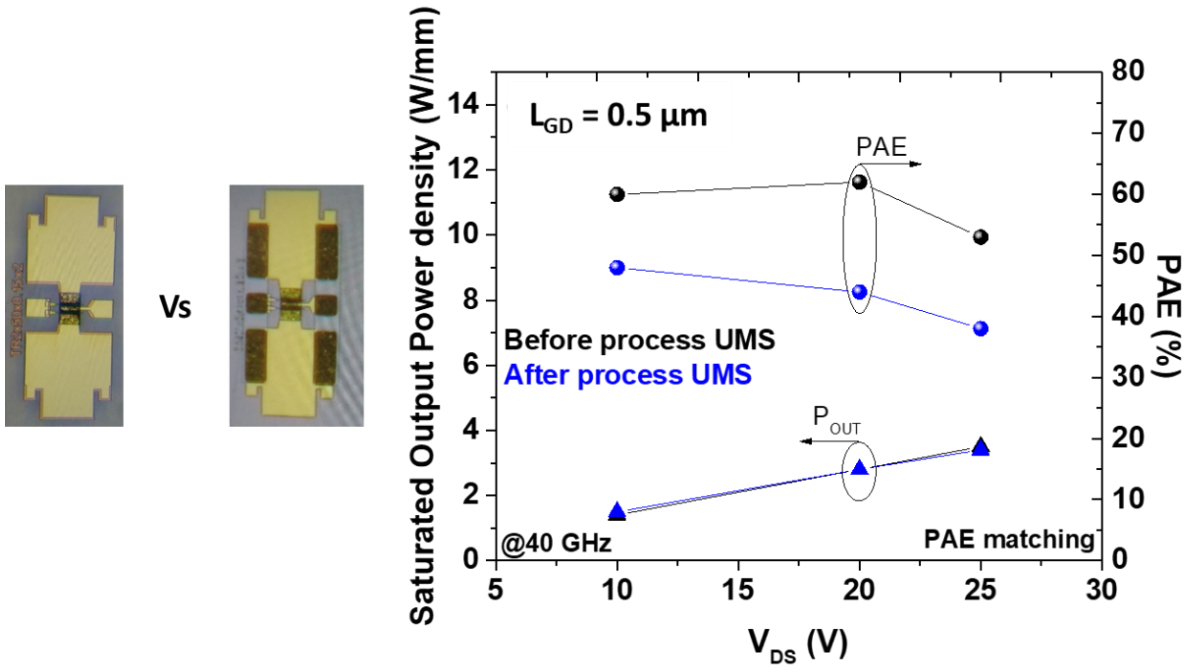


Figure.3.68. PAE and output power density (P_{OUT}) as a function of V_{DS} in **CW mode** of 2×50 µm IEMN PCMs with L_G = 105 nm and L_{GD} = 0.5 µm before and after UMS processing

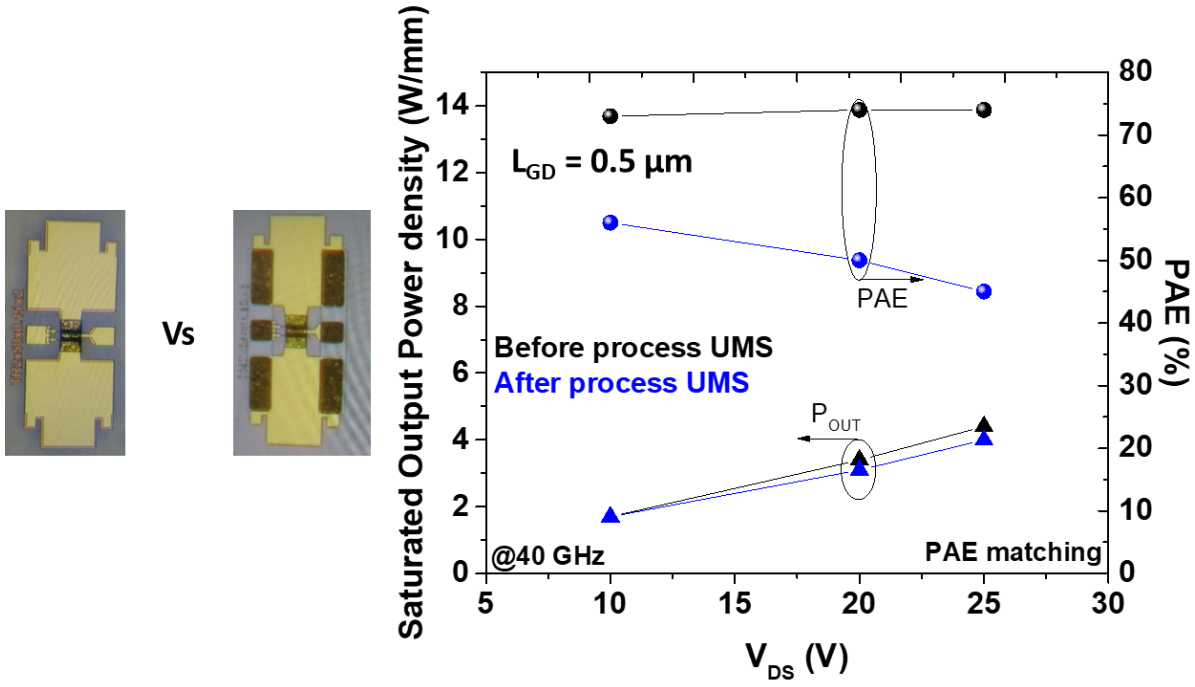


Figure.3.69. PAE and output power density (P_{OUT}) as a function of V_{DS} in **pulsed mode** of 2×50 µm IEMN PCMs with L_G = 105 nm and L_{GD} = 0.5 µm before and after UMS processing

Similarly, to the CW performances, the comparison between both PAE and P_{OUT} performances in pulsed mode between IEMN PCMs before and after UMS processing is presented in **Figure.3.69**. The significant drop of the PAE after UMS processing reflects the parasitic capacitances added after back-end processing. This gap in term of the PAE confirms the small signal decreases observed on the transistors after UMS process.

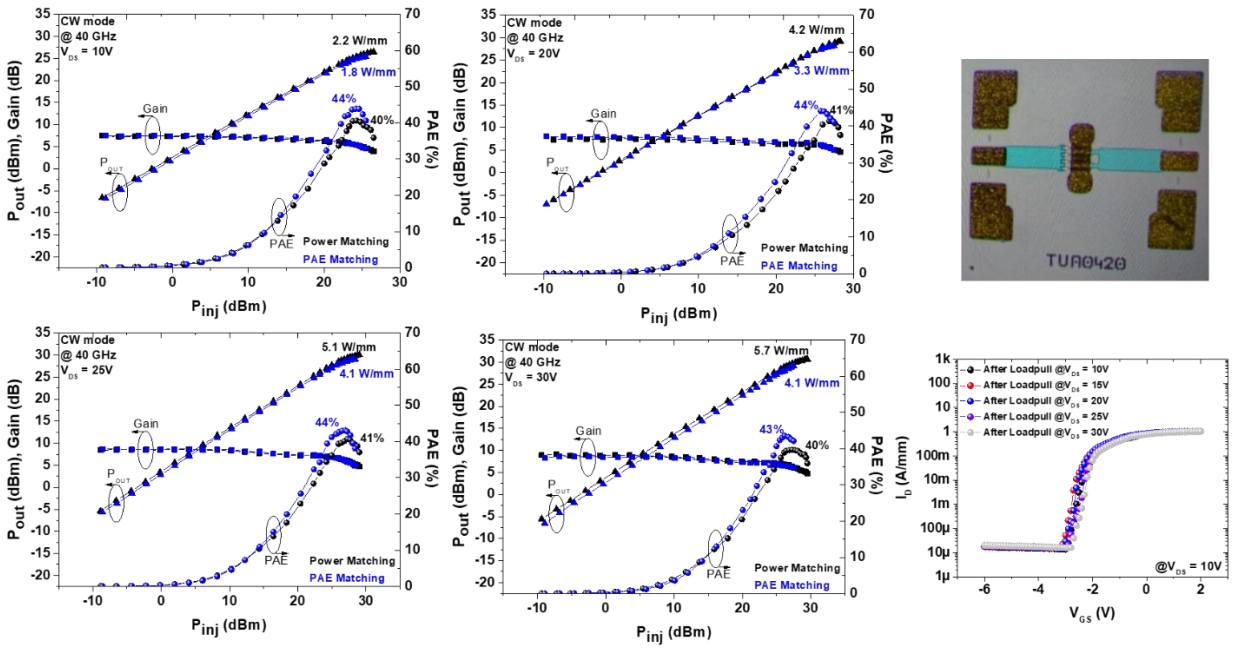


Figure.3.70. CW large signal performances at 40 GHz for 4×50 µm transistor UMS PCM after back-end processing with L_G = 105 nm and **L_{GD} = 1.5 µm** at V_{DS} = 10, 20, 25 and 30V of the 3 nm AlN/GaN HEMT structure and transfer characteristics after load-pull sweep up to V_{DS} = 30V

ii. 4×50 µm UMS PCMs after back-end processing

Figure.3.70 and **71** show 40 GHz CW and pulsed power performances of a 4×50 µm UMS PCMs after back-end processing with L_G = 105 nm and **L_{GD} = 1.5 µm** from V_{DS} = 10V up to V_{DS} = 30V for the 3 nm AlN/GaN HEMT structure.

- In CW: a stable PAE above 40% is observed up to V_{DS} = 30V with a saturated power density of 4.1 W/mm at 25V and 30V. With power matching, a PAE above 40% with a P_{OUT} of 5.7 W/mm are obtained. From the transfer characteristic after load-pull sweep, we observed no degradation of the transistor up to V_{DS} = 30V.

- In pulsed mode: a stable PAE above 50% is observed up to V_{DS} = 25V with a saturated power density of 4 W/mm at 25V. With power matching, a PAE of 45% with a P_{OUT} of 6.2 W/mm are obtained. It can be noticed that no degradation of the device observed after load-pull sweep up to V_{DS} = 30V.

The comparison between large signal CW and pulsed mode of 4×50 µm transistors with L_G = 105 nm and L_{GD} = 1.5 µm after back-end processing is presented in **Figure.3.72**. A stable and high PAE could be obtained in both CW and pulsed mode up to V_{DS} = 25V. Despite the gain loss subsequent to the passives and back-end fabrication leaving a large room for improvement, it can be pointed out that this preindustrial run shows that full MMICs can be produced out of this technology with outstanding PAE above 50% at 40 GHz under high power density.

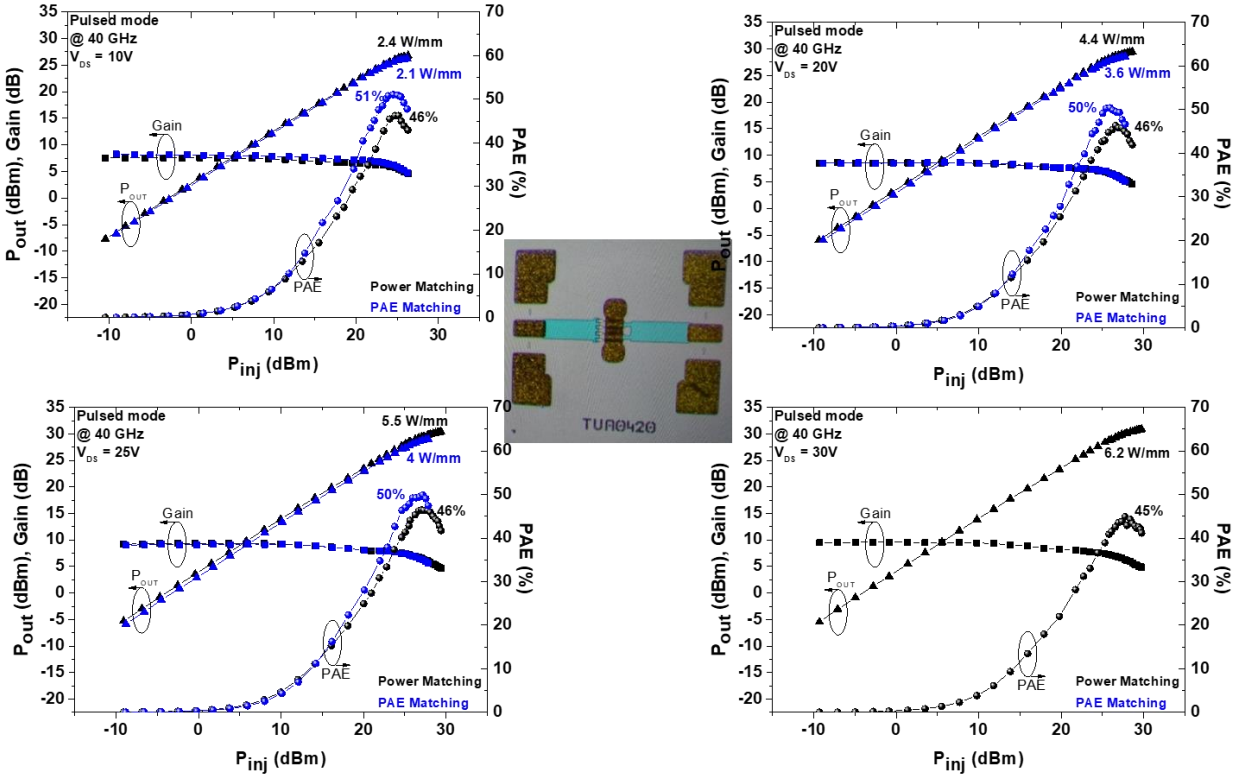


Figure.3.71. Pulsed large signal performances at 40 GHz for 4×50 µm transistor UMS PCM after back-end processing with L_G = 105 nm and **L_{GD} = 1.5 µm** at V_{DS} = 10, 20, 25 and 30V of the 3 nm AlN/GaN HEMT structure.

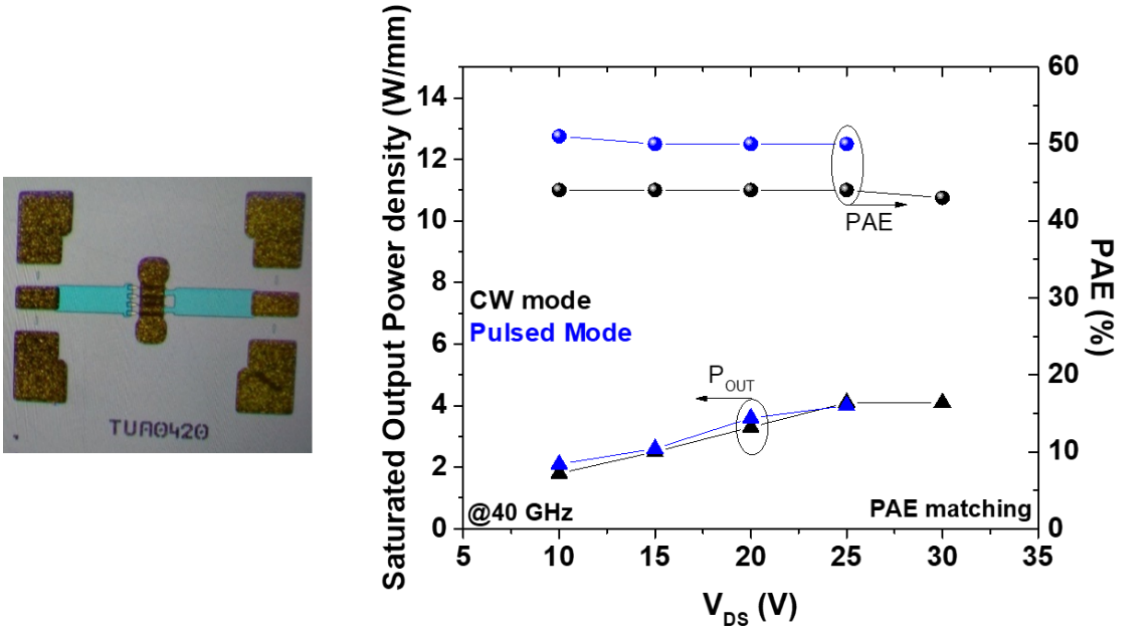


Figure.3.72. PAE and output power density (P_{OUT}) as a function of V_{DS} in CW and pulsed mode of 4×50 µm UMS PCMs with L_G = 105 nm and L_{GD} = 1.5 µm after back-end processing for the 3 nm AlN/GaN structure

III.3.2. Large signal characterization @94 GHz for the 3 nm AlN/GaN structure

Considering to the state-of-the-art large signal performances obtained at 40 GHz on the 3 nm AlN/GaN structure together with a promising reliability, we performed preliminary CW large signal characterizations at 94 GHz. 2×25 µm transistors with L_G = 105 nm and L_G = 0.5 µm have been measured with passive load-pull in CW mode. It can be specified that the passive load-pull power bench has been used for these measurements because the active load-pull upgraded bench was still not available at that time. A record P_{OUT} = 4W/mm has been achieved with a PAE of 14.3% at V_{DS} = 20V as shown in **Figure.3.73**. At V_{DS} = 15V, a PAE above 15% associated with a P_{OUT} = 3W/mm is obtained.

Therefore, we proved that with a gate length around 100 nm, this structure is able to show high performances in W-band. This can be enhanced to a large extent, especially the PAE by the optimization of the device processing, and the use of the optimized active load-pull bench. These optimizations consist in:

- The use of sub-100 nm gate length
- Optimized access resistances

- improvement of the electron mobility resulting in a higher transconductance
- Reduced trapping effects
- Optimized load-pull bench for better device matching: active load-pull, high power amplification, CW & pulsed mode that was not yet available at the time of this characterization campaign

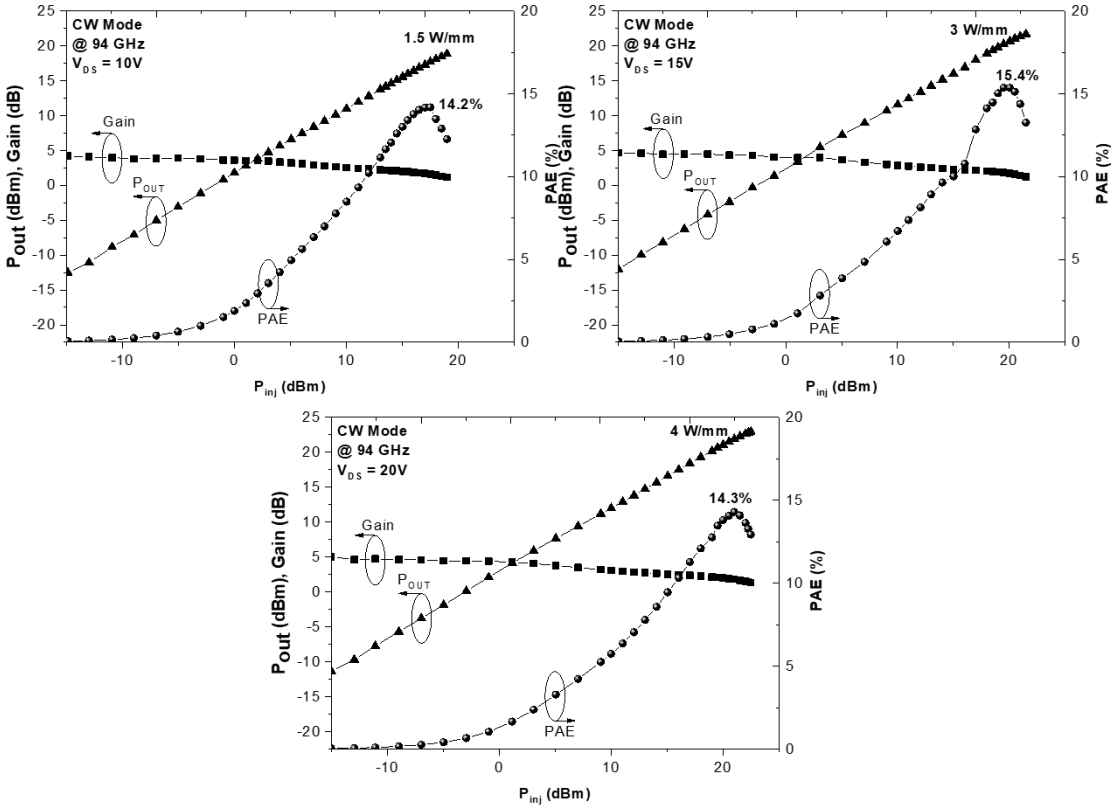


Figure.3.73. CW large signal performances at 94 GHz for 2 × 25 µm transistor L_G = 105 nm and **L_{GD} = 0.5 µm** at V_{DS} = 10, 15, and 20V of the 3 nm AlN/GaN HEMT structure

IV. State-of-the art AlN/GaN HEMT technology

Several process technologies have been performed in this work at IEMN with the aim of achieving a combination of high-power density and high PAE associated with high device robustness. In this section, we present the benchmark evolution of the AlN/GaN technology performed within the framework of this thesis.

The improvements in power density and PAE compared with past works in our Lab (see **Figure.3.74.a**) can be attributed to the optimization of epitaxial structure as well as the device processing enhancing the

power gain and device robustness. In turn, the use of ultrathin barrier layer 3 nm AlN/GaN (enabling sharper GAN to AlN transition) instead of a thicker AlN barrier allowed to benefit not only from the high performance but also the high robustness under high electric field. The improvement of our AlN/GaN technology featured a peak PAE evolution at 40 GHz from 18% (CW) in 2012 up to 60% (CW) and > 70% (pulsed) in 2020 as shown in **Figure.3.74.b**.

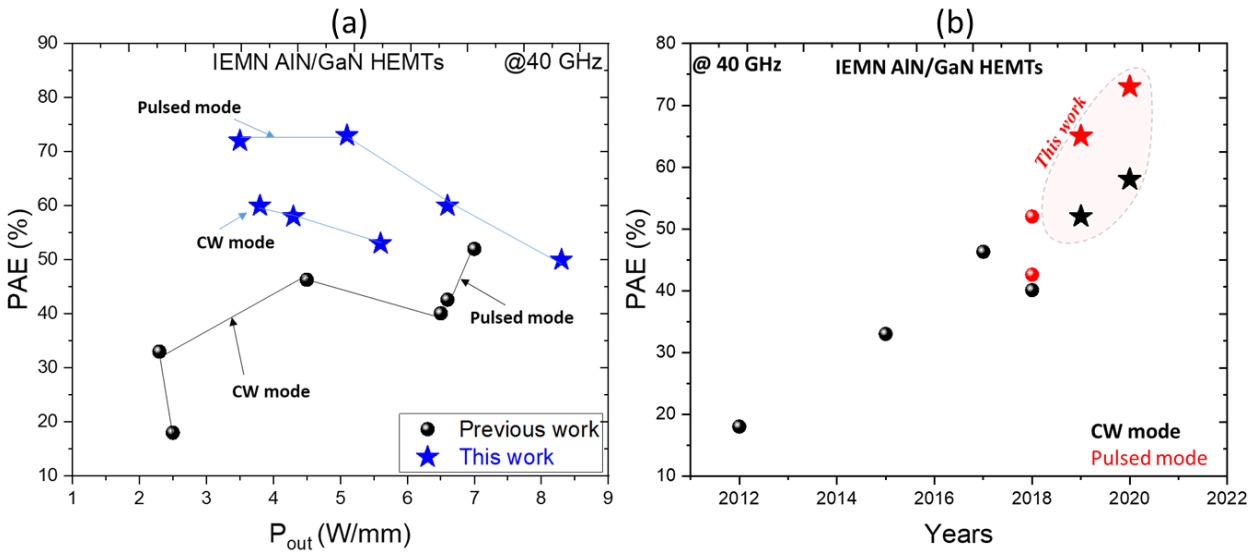


Figure.3.74. Comparison with peak reported PAE and power density at 40 GHz of IEMN AlN/GaN technology (a) and evolution of the reported peak PAE at 40 GHz from 2012 to 2021

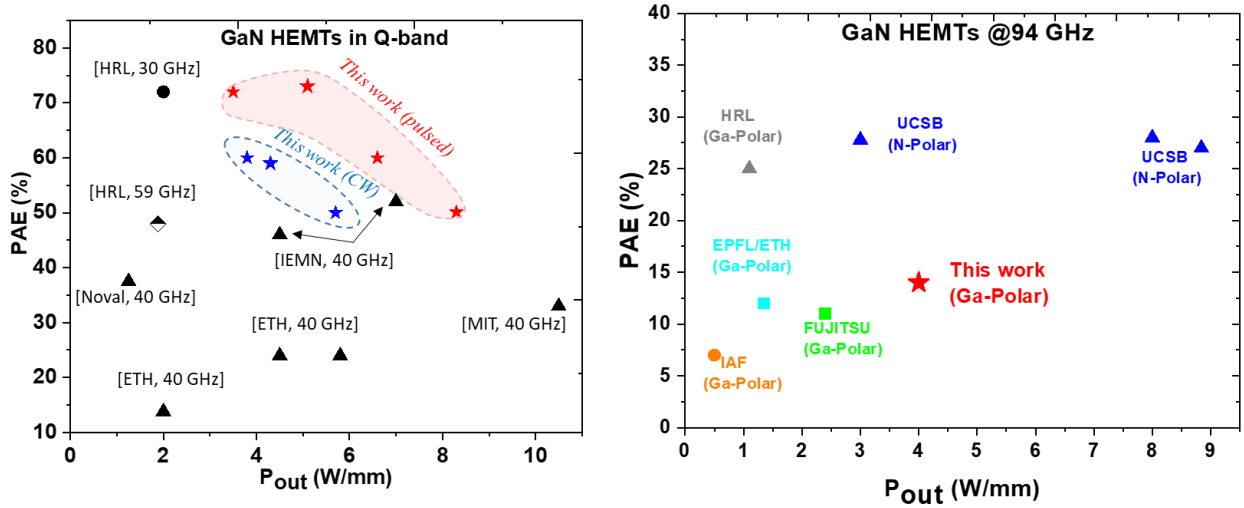


Figure.3.75. Benchmark of GaN HEMTs from the literature at Ka-Q-band (a) and W-band (b).

Figure.3.75 shows a benchmark representing the PAE as a function of the output power density from Ka to Q-band. Both CW and pulsed RF performances of our AlN/GaN devices at 40 GHz aree favorably comparable to the state-of-the art with a combination PAE/P_{OUT} (73%/5.2 W/mm) in pulsed mode. In W-band, a record output power density of 4 W/mm at V_{DS} = 20V exceeding any reported Ga-polar transistors in this frequency range. It can be noticed that no reliability reports are available for the N-polar based GaN transistors delivering performances that outperform so far other technologies.

V. Conclusion

In this chapter, we first showed the limits of AlGaN/GaN technology, which is not suitable for high frequency operation due to the difficult scaling of the AlGaN barrier layer while maintaining high polarization and/or avoiding gate leakage current with high Al-content. Numerous studies have been performed with the aim of developing a technology capable of providing high PAE, high output power density and superior device robustness at high frequency operation. In order to meet these requirements, the investigated solutions in this work consist in the optimization of both ultrathin Al-rich barrier layer epitaxial structure and associated device processing.

Variations of carbon concentration and channel thickness have been experimentally analyzed to understand the impact on the electrical performance. It was found that the channel thickness and the carbon concentration into the buffer are part of a clear trade-off in terms of trapping effects and parasitic effects such as punch-through and related DIBL. High carbon doping concentration with low undoped GaN channel thickness results in memory effects but excellent DIBL under high electric field and inversely. Therefore, an AlGaN BB introduced between a low C-doped GaN buffer and the channel has been studied. A degradation of the electron confinement is observed with short gate lengths due to the too low Al-content (4%) in the AlGaN BB as the back polarization needs to be increased. Therefore, SOITEC produced similar structures with a higher Al-content in the AlGaN BB that are under investigations.

A shared process between UMS and IEMN of advanced heterostructures have been established and implemented. Two different AlN barrier thickness of 3 nm and 4 nm have been used in order to study the impact on RF device performances. A superior robustness has been demonstrated with the 3 nm AlN/GaN HEMT as compared to the 4 nm AlN/GaN HEMT through short-term RF and DC reliability performed at IEMN and University of Padova. HRTEM structural characterization in collaboration with C2N Laboratory revealed a much sharper AlN/GaN interface in the case of the thinner barrier. The larger Al-rich AlGaN

transition due to memory effects during the MOCVD growth for the 4 nm barrier heterostructure explains the poor device robustness.

IEMN PCMs before back-end processing have demonstrated a state-of the art PAE and output power density associated with a promising short-term reliability up to high temperature. Large signal characterization at 94 GHz on the 3 nm AlN/GaN has demonstrated state-of-the art P_{OUT} of 4W/mm which exceed any Ga-polar technology. Improvements in both power density and efficiency in W-band are expected with the optimization of the device processing and characterization such as reduced trapping effects and smaller device design as well as the optimization of the active load-pull bench.

Other structures were studied in order to enhance device performances. For example, the quaternary InAlGaN/GaN structure that provides higher 2DEG electron mobility as compared to AlN/GaN structure or an innovative structure without buffer layer in order to reduce the thermal dissipation have been also studied. These structures will be discussed in the chapter 4.

Chapter 4: Other technological approaches for high frequency millimeter-wave GaN HEMTs

I. Introduction

In order to further enhance the device RF performances, especially at W-band and above, we studied an InAlGaN/GaN structure and an ultrathin AlGaN/GaN buffer-free HEMT. Therefore, we replaced the AlN barrier with InAlGaN barrier layer to benefit from a higher electron mobility, which is key for high frequency applications. Indeed, the high electron mobility enables both decreasing the electron transient time in the channel and favors the ohmic contact formation through the barrier layer, thus increasing the device RF performances. Furthermore, an innovative structure without buffer layer is studied in order to reduce the thermal dissipation during the device operation.

In this chapter, we present the electrical and structural characterizations of the fabricated transistors on InAlGaN/GaN and thin-HEMT AlGaN/GaN technology. The measurements campaign using various types of characterization (as described in chapter 2) were performed at IEMN. Structural characterizations are realized on both epitaxial structures and transistors on the InAlGaN/GaN structure with the support of our partners from C2N and ILV laboratories. **Figure.4.1** shows the studied structures showing the different steps of the transistor's fabrication and characterization.

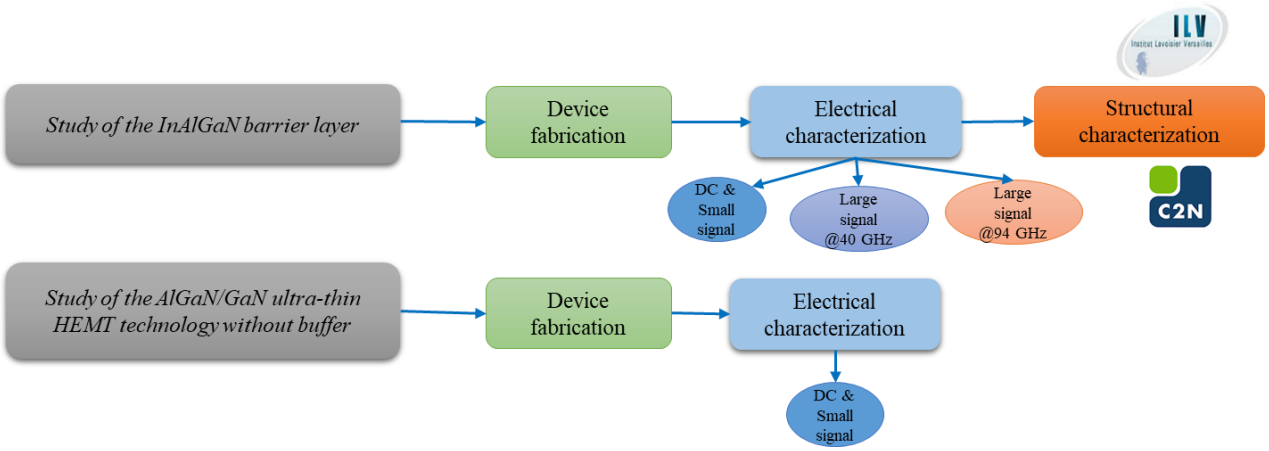


Figure.4.1. Structure of the different studies

II. InAlGaN barrier layer

The structures shown in **Figure.4.2** have been grown on SiC substrates by SOITEC. They consist of an AlN nucleation layer, 2×10^{19} cm^{-3} C-doped GaN buffer, followed by a 100 nm GaN channel, 6 nm InAlGaN barrier layer, and 2.5 nm SiN cap layer for the structure A. structure B is identical except for the 7 nm InAlGaN barrier with 6 nm SiN cap layer. A thicker SiN cap layer is used for the structure B in order to minimize the surface trapping. These structures generate high electron mobility of 1800 $cm^2/V.s$ and 1700

$cm^2/V.s$ associated with high 2DEG density of 1.5×10^{13} cm^{-2} and 1.9×10^{13} cm^{-2} for structure A and B, respectively. Low sheet resistances of 230 Ω/□ for structure A and 180 Ω/□ for structure B have been extracted, which can lead to reduced access resistances.

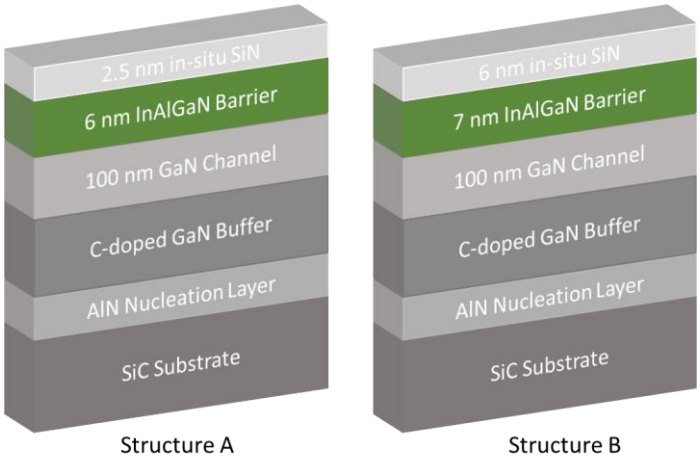


Figure.4.2. Schematic cross section of the 2.5 nm SiN/6 nm InAlGaN/GaN (left) and 6 nm SiN/7 nm InAlGaN/GaN structures (right).

II.1. 2.5 nm SiN/6 nm InAlGaN/GaN (structure A)

1) Device fabrication

The fabrication process on InAlGaN/GaN structures has been carried out using the e-beam mask-set "GaN Fast". A Ti/Al/Ni/Au metal stack annealed at 825°C has been used to form source-drain ohmic contacts directly on top of the InAlGaN barrier by etching the in-situ SiN layer. Very low contact resistances of 0.25 Ω.mm extracted by TLM method. Ni/Au T-gates were defined by e-beam lithography. The SiN underneath the gate was fully removed using SF_6 plasma etching through the e-beam lithography. Finally, 200 nm PECVD SiN layer was deposited as final passivation. **Figure.4.3** shows the various gate lengths fabricated on these structures in order to evaluate the impact on DC characteristics.

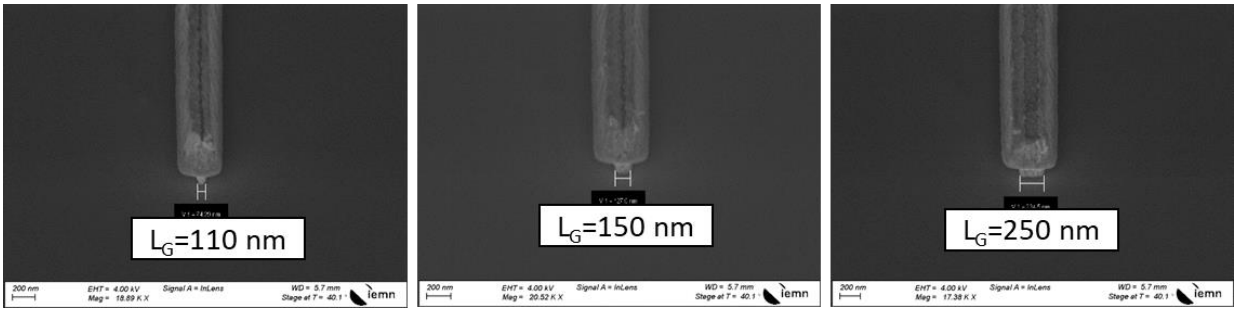


Figure.4.3. SEM images of different tilted T-gates

2) DC and small signal characterization

Figure.4.4 shows the transfer, output characteristics and transconductance of a 2×50 µm transistor with L_G = 110 nm and L_{GD} = 0.5 µm. All characteristics have been measured after a burn-in step. This structure delivers a maximum drain current density of 1.5 A/mm (at V_{GS} = +2V) with a leakage current below 10 µA/mm. a pinch-off voltage about V_{th} = -2V is observed. A high extrinsic transconductance close to 600 mS/mm is obtained at V_{DS} = 10V reflecting the superior electron mobility as compared to AlN/GaN heterostructure. The consequences are visible in the cut-off frequencies with an f_t/fmax of more than 65/305 GHz at V_{DS} = 20V and the corresponding power gain as high as 18 dB at 40 GHz.

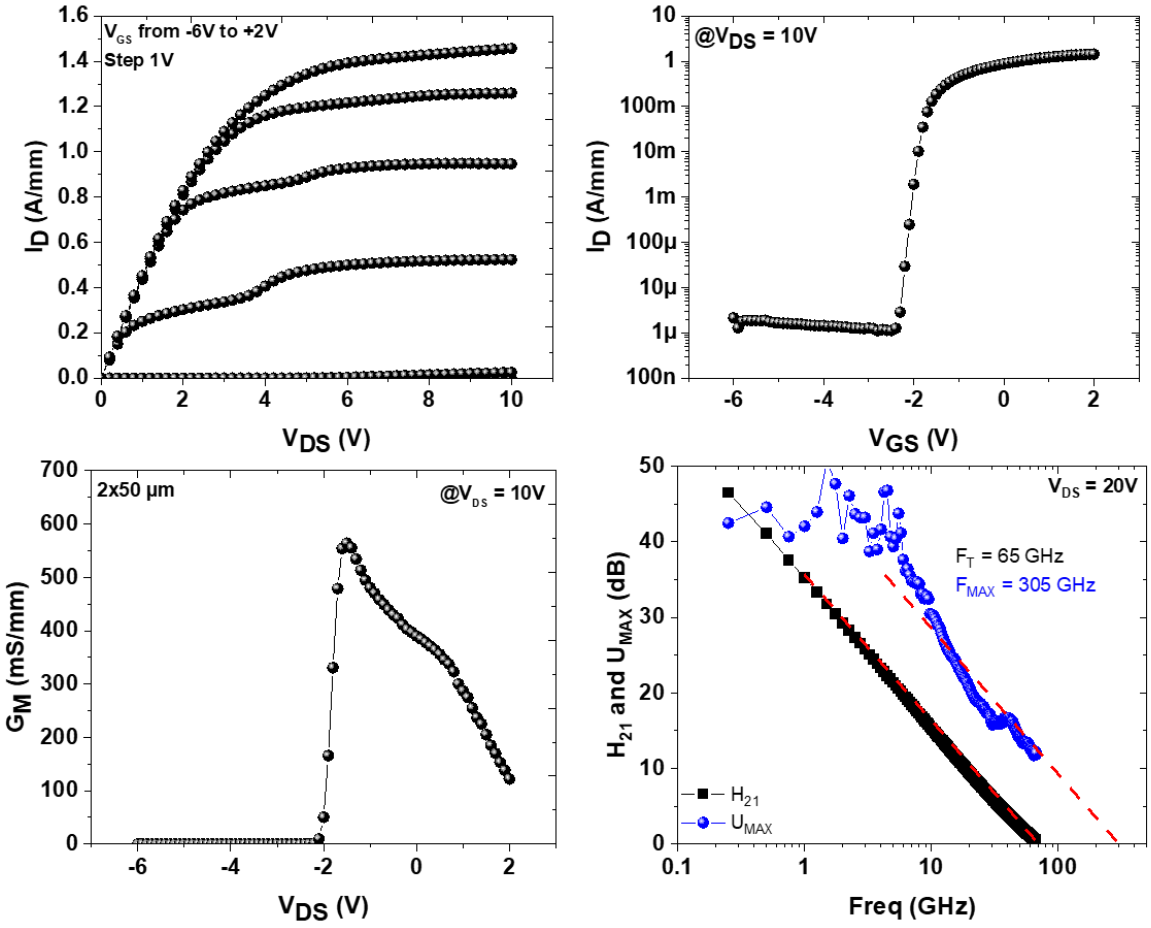


Figure.4.4. Transfer, output characteristics, transconductance and S-parameters of a 2×50 µm transistors with L_{GD} = 0.5 µm and L_G = 110 nm of structure A

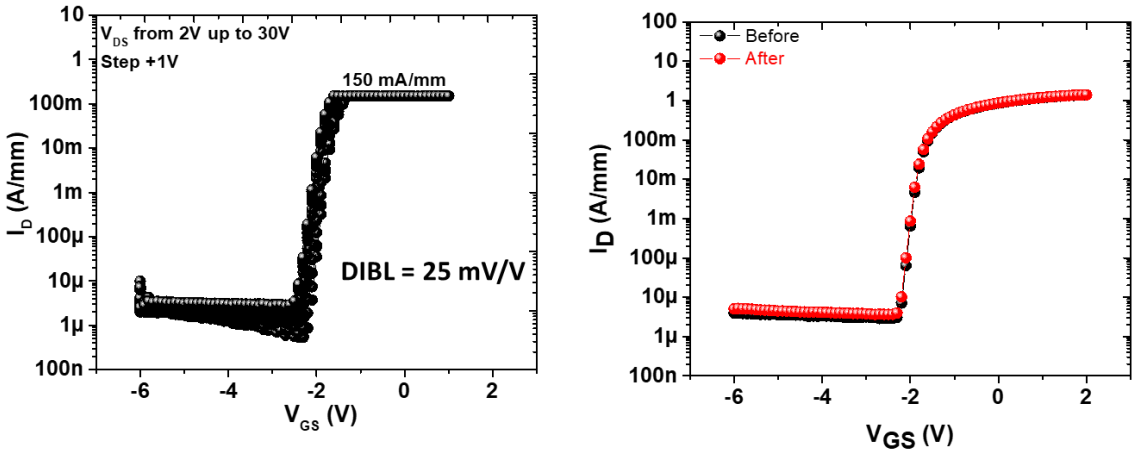


Figure.4.5. Semi-on robustness test of 2×50 µm transistors with L_G = 110 nm and L_{GD} = 0.5 µm of structure A

In order to assess the electron confinement, semi-on robustness tests have been carried out. Several I_D (V_{GS}) sweeps up to V_{DS} = 30V with a drain current I_D limitation at 150 mA/mm were carried out on 2×50 µm transistor with L_G = 110 nm and L_{GD} = 0.5 µm. Despite the short gate length, we observed no degradation of the leakage current up to V_{DS} = 30V with an excellent electron confinement owing to the high carbon concentration GaN buffer (as seen in the previous chapter). A DIBL as low as 25 mV/V has been measured for these transistors as shown in **Figure.4.5**.

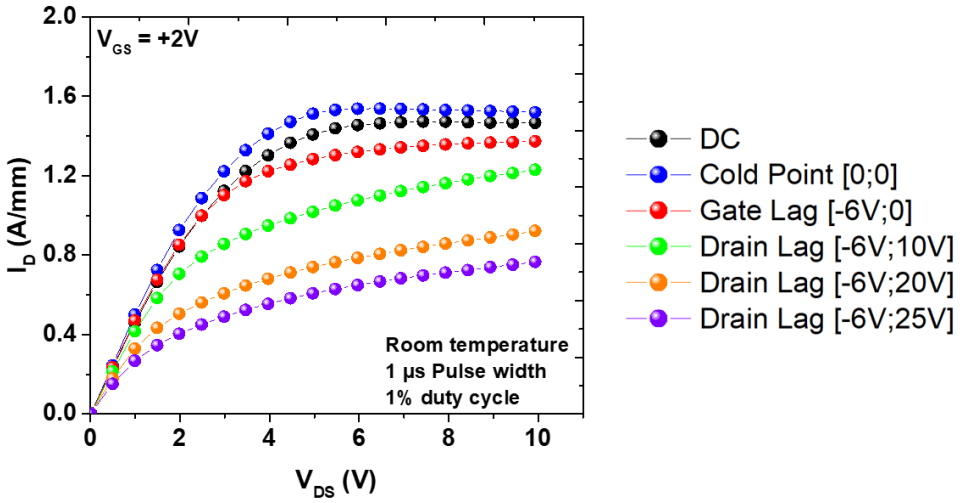


Figure.4.6. Pulsed I-V characteristics of 2×50 µm transistors with L_G = 110 nm and L_{GD} = 0.5 µm of structure A

Figure.4.6 shows the pulsed I-V characteristics using different quiescent bias points on 2×50 µm transistors with L_G = 110 nm and L_{GD} = 0.5 µm. We observed from the gate and the drain lag severe trapping

effects, which are attributed to the high carbon doping and surface states when using such an ultrathin SiN cap layer.

3) Large signal characterization @40 GHz

Figure.4.7 shows 40 GHz CW power performances of a 2×50 µm with L_G = 110 nm and **L_{GD} = 0.5 µm** from V_{DS} = 10V up to V_{DS} = 20V for the 2.5 nm SiN/6 nm InAlGaN/GaN HEMT structure. It can be noticed that the load-pull measurements have been carried out after a burn-in step, which consists of biasing the transistor at high drain voltage for several seconds until the stabilization of the maximum drain current I_{Dmax}. A PAE of 60% is observed at V_{DS} = 10V with a saturated power density of 1.7 W/mm. At V_{DS} = 20V, a PAE of 55% with a P_{OUT} of 3.5 W/mm are reached. With power matching, a PAE above 50% with a P_{OUT} of 4.8 W/mm are obtained. From the transfer characteristics after load-pull sweep, we observed no degradation of the transistor up to V_{DS} = 20V but at V_{DS} > 20V we observed a gate leakage current increase, which is attributed to the short gate-drain distance.

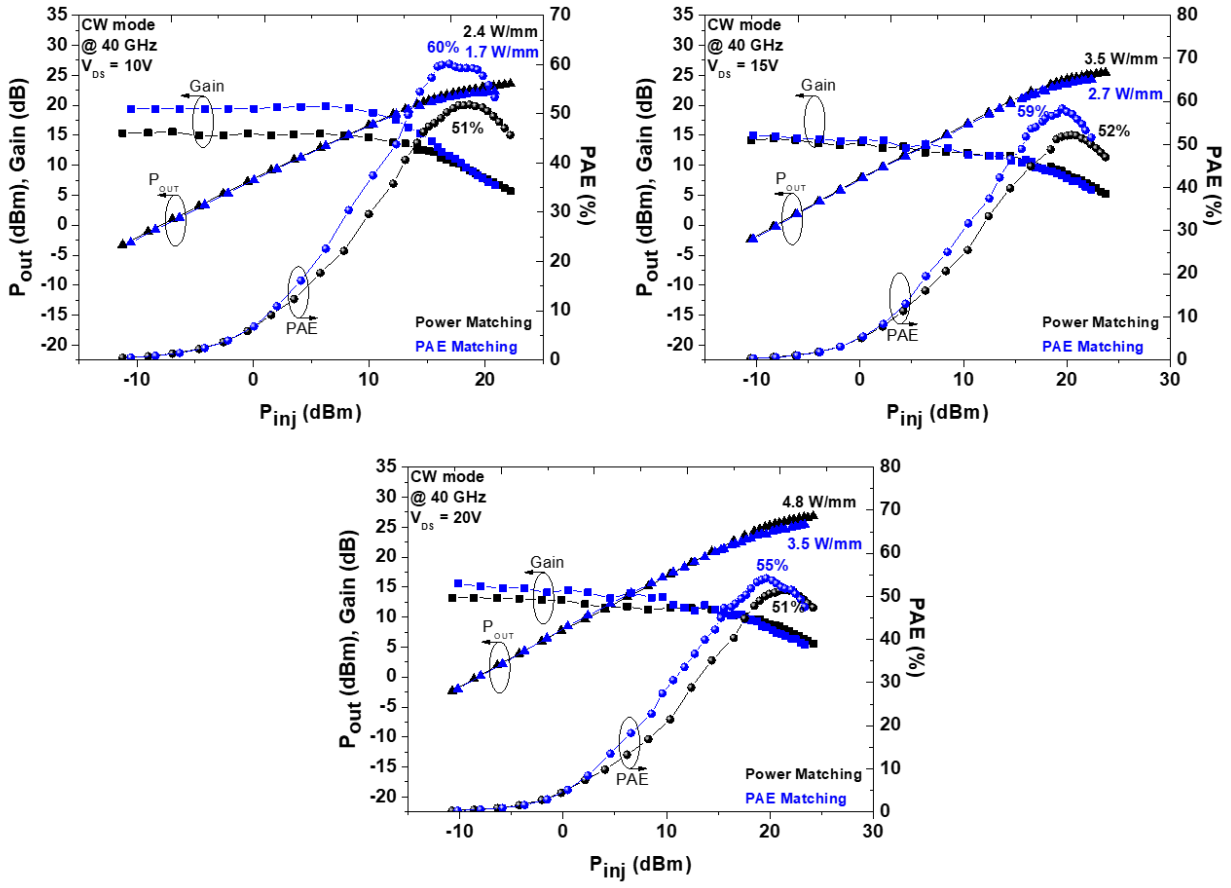


Figure.4.7. CW large signal performances at 40 GHz for 2×50 µm transistors with L_G = 110 nm and **L_{GD} = 0.5 µm** at V_{DS} = 10, 15, and 20V of structure A

Figure.4.8 shows 40 GHz pulsed power performances of a 2×50 µm with L_G = 110 nm and **L_{GD} = 0.5 µm** from V_{DS} = 10V up to V_{DS} = 20V for the 2.5 nm SiN/6 nm InAlGaN/GaN HEMT structure. A PAE of 74% is observed at V_{DS} = 10V with a saturated power density of 2.1 W/mm. At V_{DS} = 20V, PAE of about 70% with a P_{OUT} of 4.1 W/mm are reached. With power matching, a PAE of 65% with a P_{OUT} of 5.3 W/mm are obtained. Similar to the CW mode, we observed no degradation of the transistor up to V_{DS} = 20V unlike at V_{DS} > 20V limited by the transistor design.

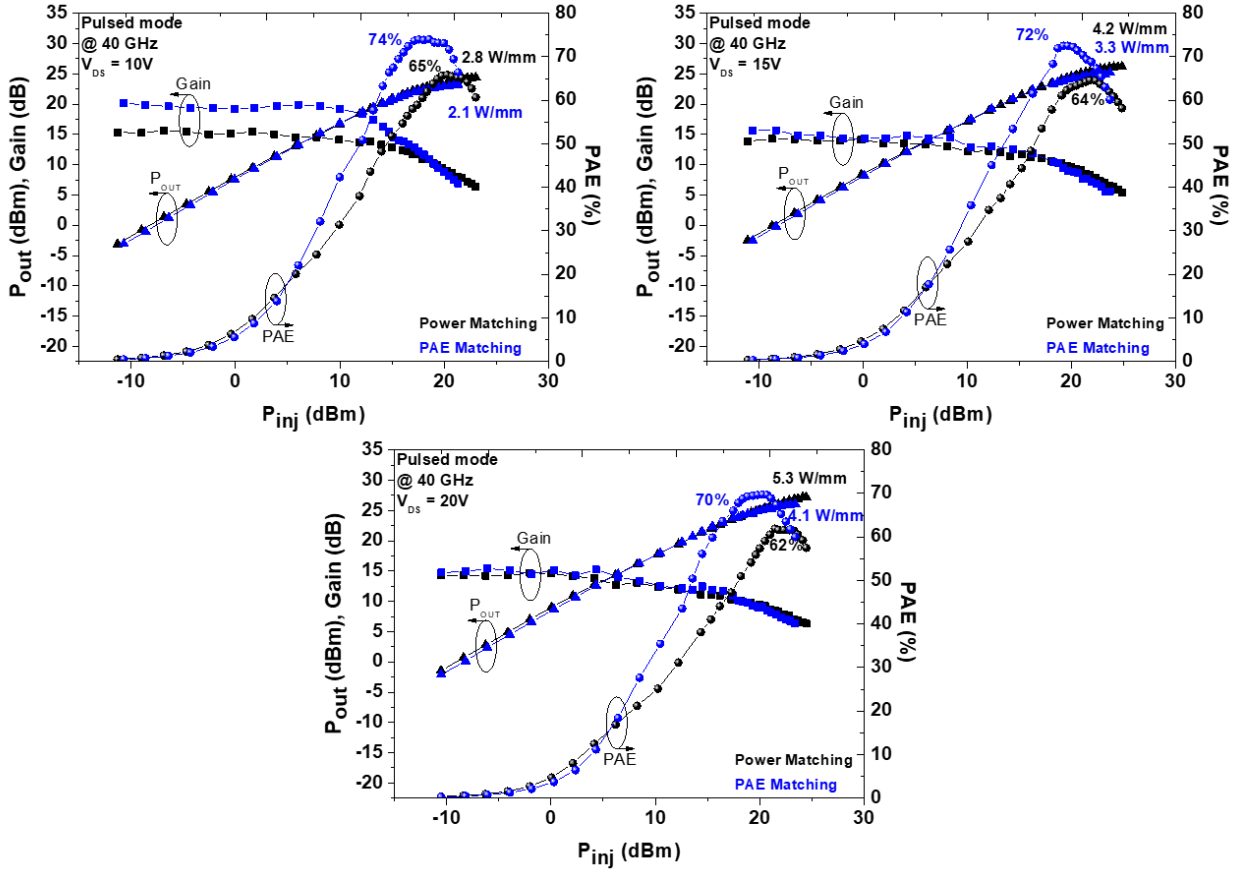


Figure.4.8. Pulsed large signal performances at 40 GHz for 2×50 µm transistor with L_G = 110 nm and **L_{GD} = 0.5 µm** at V_{DS} = 10, 15, and 20V of the 2.5 SiN/6 nm InAlGaN/GaN HEMT structure

4) Results discussion and comparison

The quaternary InAlGaN/GaN structure allows to benefit from higher power gain and current density as compared to AlN/GaN structure. A high power gain is crucial to achieve high power performances at high frequency up to W-band. Despite severe trapping effects observed on this structure resulting in a large gap between CW and pulsed measurements (as shown in **Figure.4.9**), preliminary achieved performances at 40 GHz are promising and already at the state-of-the-art level. On the other hand, there is a large room

for improvement as the fabrication process on this structure and the surface passivation needs to be extensively optimized.

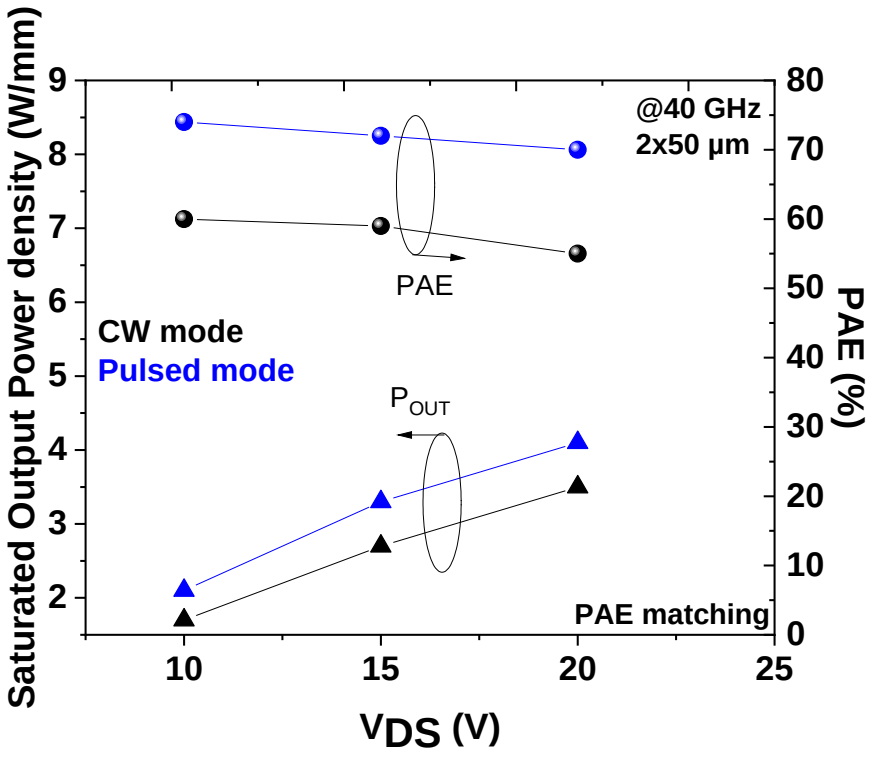


Figure.4.9. PAE and output power density (P_{OUT}) as a function of V_{DS} in CW and pulsed mode of 2×50 µm with L_G = 110 nm and L_{GD} = 0.5 µm of structure A

5) Structural characterization

The structural characterizations have been carried out on the same 2.5 SiN/6nm InAlGaN/GaN structure described above but with a different fabrication process. For these devices, we did not used physical etching for the gate module. The SiN underneath the gate was removed by chemical etching before the gate lithography step. This process allowed a very short gate length of L_G = 50 nm by the avoiding enlargement of the e-beam lithography occurring with plasma etching as shown in **Figure.4.10**. Small signal characterizations show a high f_t/f_{max} of 70/300 GHz and a high-power gain U_{max} of 19 dB at V_{DS} = 25V. However, DC pulsed characterization reveals again severe trapping effects as shown in **Figure.4.11.a**. **Figure.4.11.b** depicts pulsed transconductance measurements showing a reduction of the maximum transconductance peak, which confirms that the electron trapping originate from the surface. These trapping effects phenomena are mainly attributed to the non-passivated surface before the gate processing.

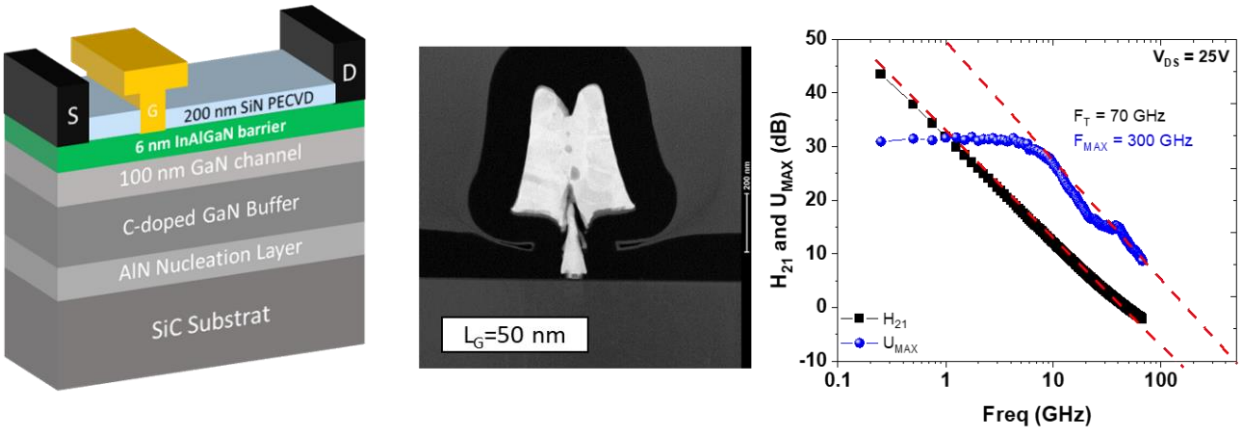


Figure.4.10. Schematic cross section of the 6 nm InAlGaN/GaN HEMT, cross section TEM view of a 50 nm gate length, and the corresponding S-parameters at V_{DS} = 25V

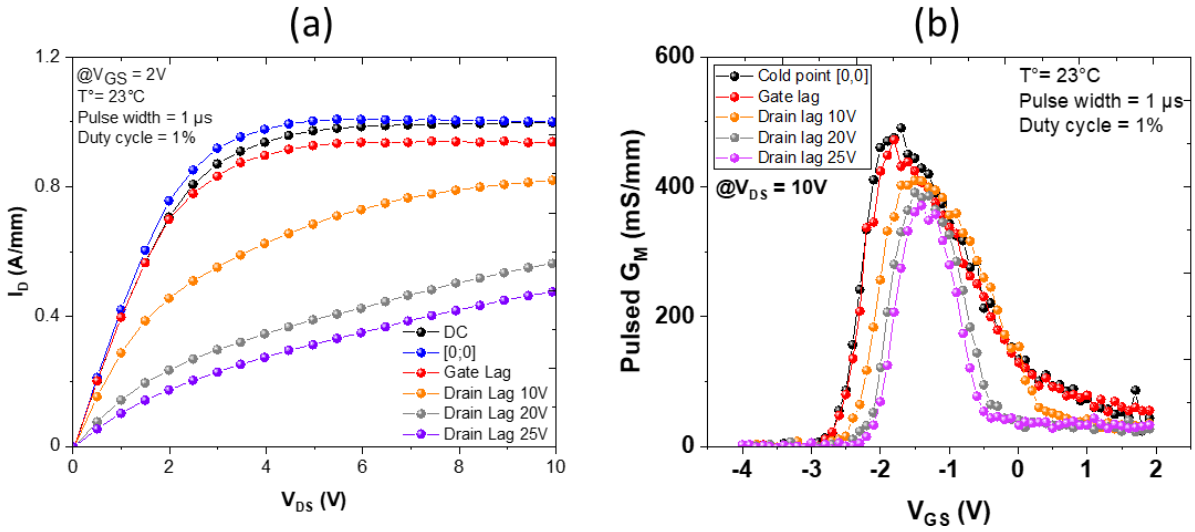


Figure.4.11. pulsed I_D (V_{DS}) characteristics and pulsed transconductance of a 2×25 µm transistor with L_G = 50 nm and L_{GD} = 0.5 µm of structure A

- **HRTEM analysis of structure A**

In order to identifying the elemental composition of the InAlGaN/GaN structure, we performed STEM analyses. **Figure.4.12** shows EDX mapping images of the structure A. The Ga, Al, In and Si are homogeneously dispersed as shown in the EDX mapping images. We observed also an oxide on the surface due to the oxidation of the SiN cap layer. As mentioned previously, the carbon observed in the material is deposited during the thin lamella preparation with the FIB. We observed from the EDX images that this structure exhibits a sharp interface between the quaternary materials and the GaN channel. The results

indicate a very well defined and uniform InAlGaN barrier layer resulting in successful atoms dispersion and high-quality materials.

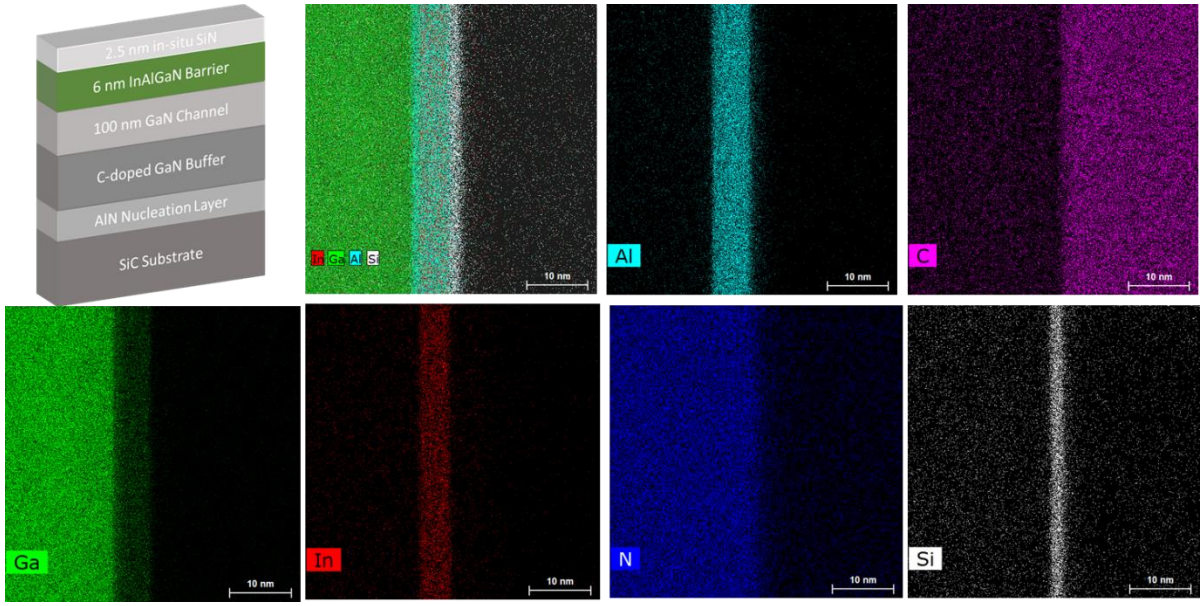


Figure.4.12. Energy Dispersive X-ray (EDX) mapping of structure A

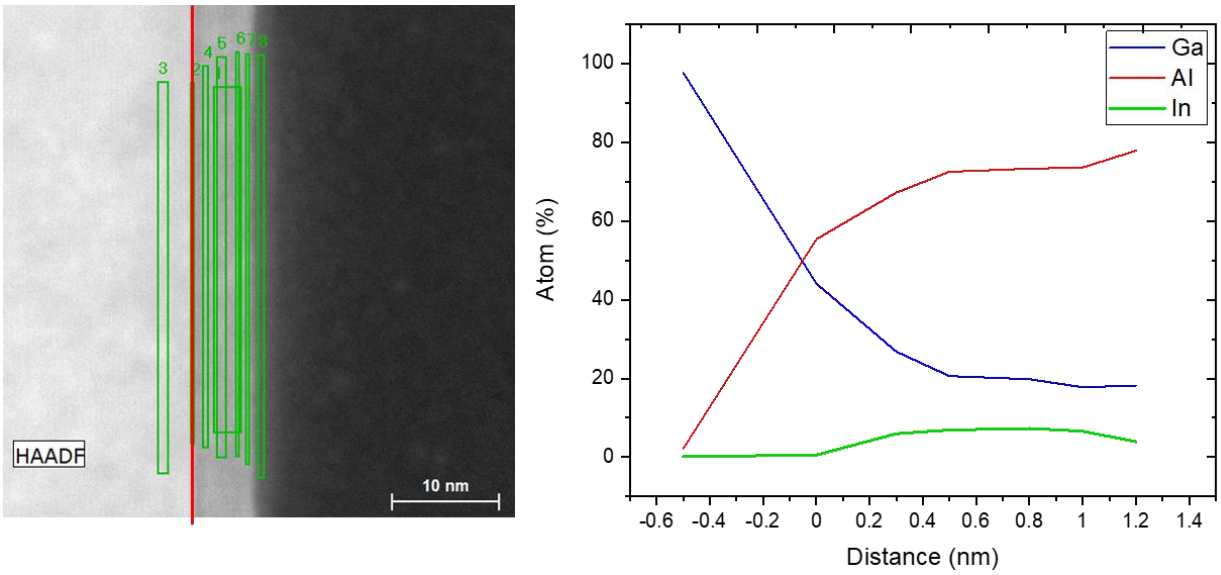


Figure.4.13. In-Al-Ga distribution in structure A

The corresponding HAADF image and EDX-profile are shown in **Figure.4.13** with the y-axis showing the total atomic percentage of the Al, In and Ga compound. In this case, we observed a short transition region between the GaN and quaternary layers. Al atoms of 70% are identified into the barrier with a Ga content of 20% and In content of less than 10%. This is in agreement with the requirements to allow a high

quality InAlGaN/GaN crystalline structure and explains to a large extent the superior electron mobility in the 2DEG.

- **HRTEM analyses on the InAlGaN/GaN HEMTs**

In order to analyze the gate/barrier layer interface, we performed HRTEM analyses on the 6 nm InAlGaN/GaN transistor. A gate length of L_G = 50 nm as shown in **Figure.4.14** has been measured. It can be reminded that the gate processing of these devices was performed without using SF_6 plasma ICP etching prior to the Ni/Au metal stack is deposited. We can clearly see at the gate/barrier layer interface a lower defect density as compared to the 3 nm AlN/GaN transistor, which is attributed to the absence of the SF_6 ICP gate etching.

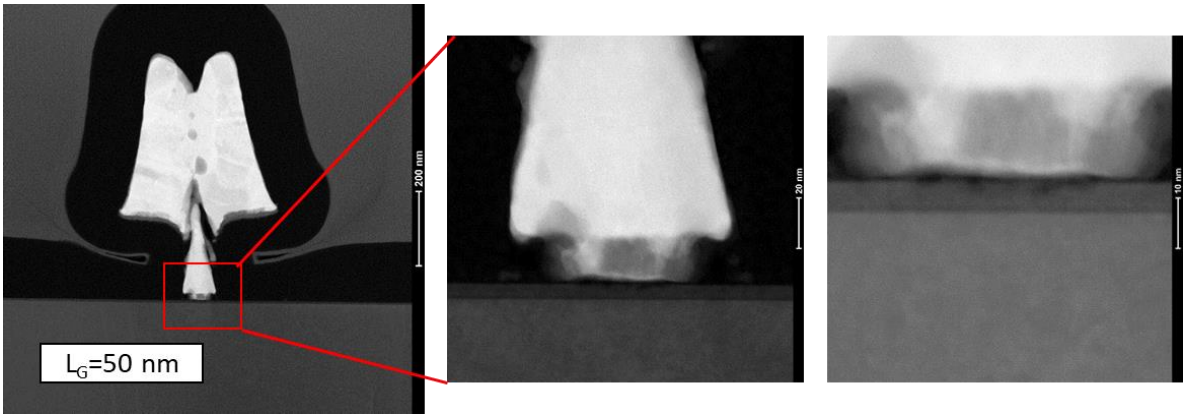


Figure.4.14. Cross section of the HRTEM of the 50 nm gate obtained with 6 nm InAlGaN/GaN structure

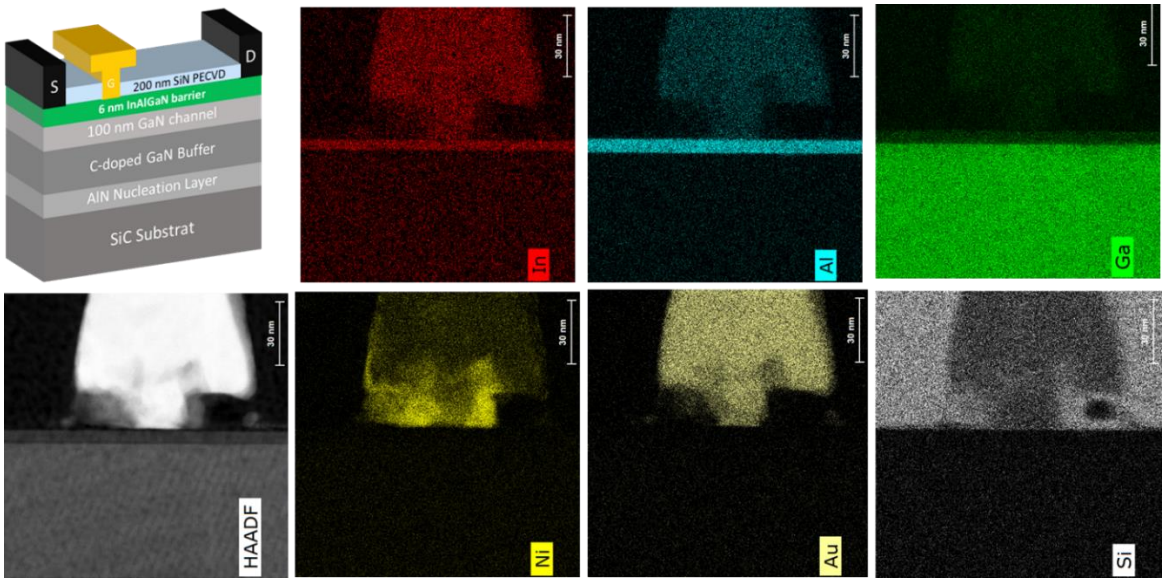


Figure.4.15. Energy Dispersive X-ray (EDX) mapping with 30 nm scale of structure A

Figure.4.15 and **16** show HAADF and EDX mapping images with two different scales (30 nm and 3 nm) of the gate/barrier layer interface. The elemental composition shows Ni, Au, metal stack and Si atoms corresponding to the final SiN PECVD passivation as it shown in the EDX mapping images. As expected, we observed an absence of Fluorine at the gate/barrier layer interface, which certainly helps reducing the gate lag effect. Further investigations on Fluor-free gate etching need to be performed to properly evaluate the potential benefit for the transistor performance and reliability.

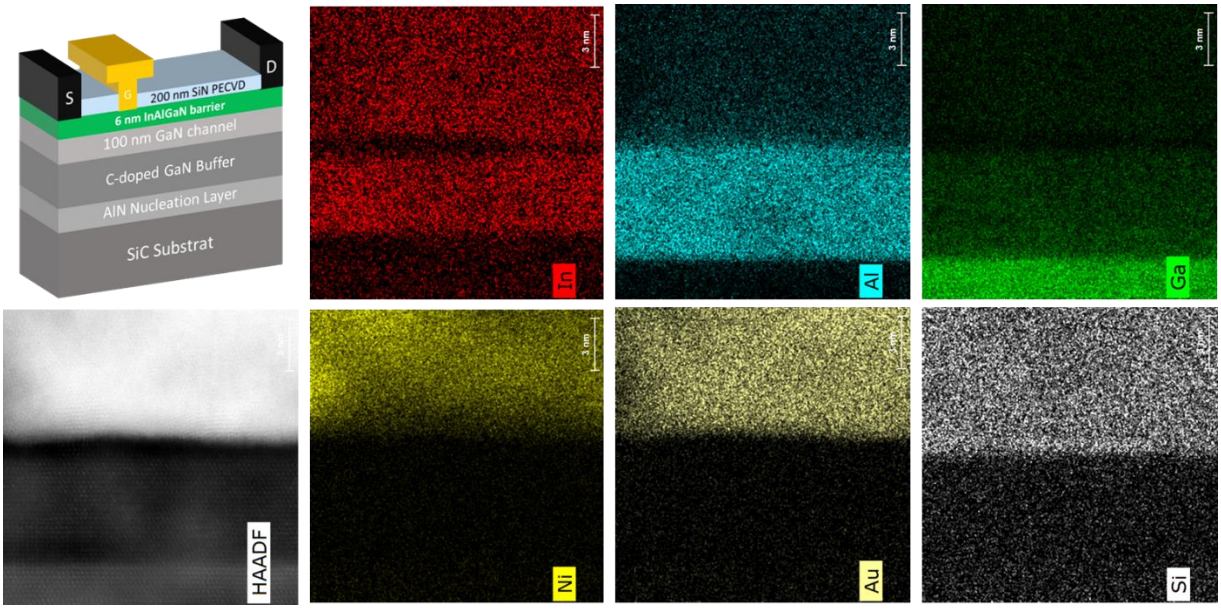


Figure.4.16. Energy Dispersive X-ray (EDX) mapping with 3 nm scale of structure A

II.2. 6 nm SiN/7 nm InAlGaN/GaN (structure B)

1) Device fabrication

The fabrication process of the structure B is similar to the structure A. slightly higher contact resistances of 0.4 Ω.mm were extracted by TLM method due to the non-optimized Argon etching prior to the metallization. The SiN underneath the gate was fully removed using in-situ Argon etching plasma in-situ within the metallization chamber. This etching method allows shorter gate lengths and to suppress the Fluor implantation observed in HRTEM characterization, which degrades the interface gate/barrier layer and induces negative ions implantation directly affecting the 2DEG. Finally, 200 nm PECVD SiN layer was deposited as final passivation. **Figure.4.17** shows the different gates fabricated this structure.

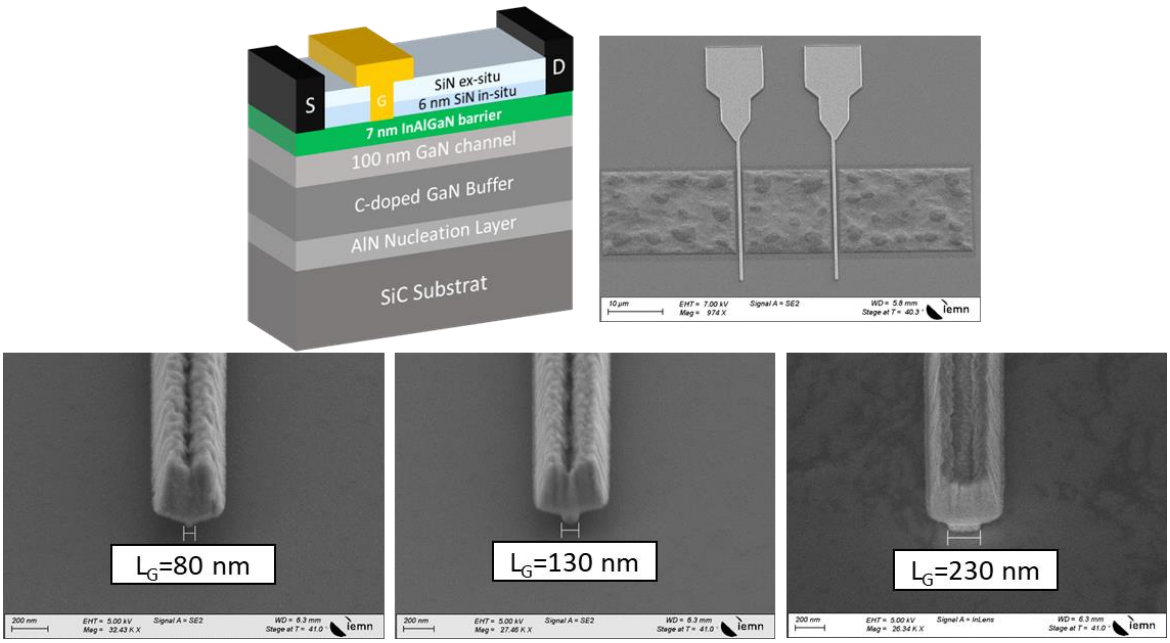


Figure.4.17. Schematic cross section of the HEMT structure and SEM image of different tilted gates

2) DC and small signal characterization

DC measurements have been performed on the fabricated transistors. **Figure.4.18** shows the output characteristics and semi-on robustness test of a 2×25 µm transistor with L_G = 130 nm and L_{GD} = 0.5 µm. The transistors deliver a lower maximum drain current of 1.1 A/mm due to the non-optimized ohmic contacts. Semi-on robustness tests have been carried out. Several I_D (V_{GS}) sweeps corresponding to different V_{DS} up to 30V with a drain current I_D limitation at 150 mA/mm were carried out. We observed no degradation of the leakage current up to V_{DS} = 30V with an excellent electron confinement.

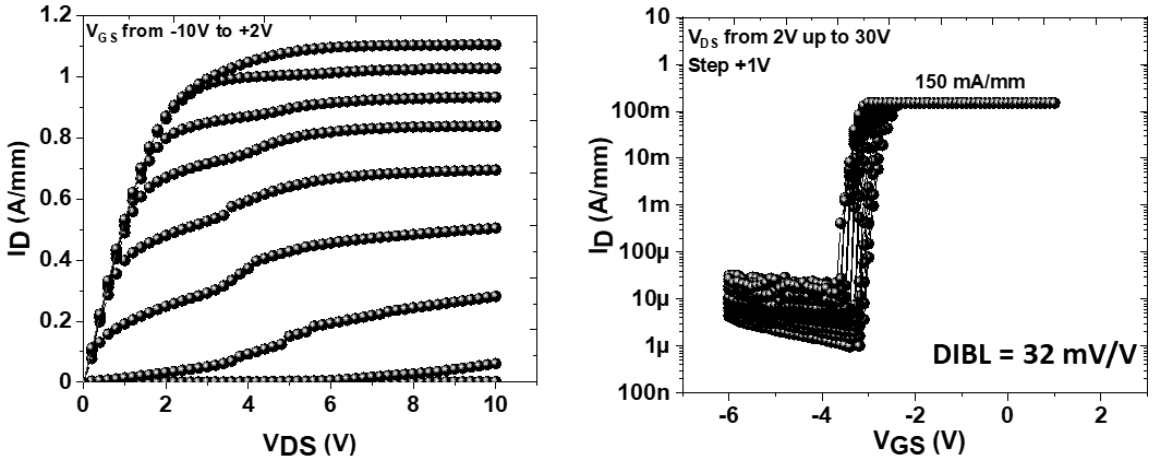


Figure.4.18. Output characteristics and semi-on robustness test of 2×25 µm transistors with L_G = 130 nm and L_{GD} of 0.5 µm of the 6 nm SiN/7 nm InAlGaN/GaN structure.

Figure.4.19 shows pulsed I-V characteristics using different quiescent bias points on 2×25 µm transistors with L_G = 130 and L_{GD} of 0.5 µm. We observed from the gate and drain lag rather low trapping effects compared to the structure A owing to the optimized gate etching process as well as the thicker SiN cap of 6 nm used for this structure. Indeed, the gate etching method used allows to suppress the Fluor implantation observed in HRTEM characterization, which degrades the device performances. Therefore, the quaternary structure with low trapping effects combined with high current density and high-power gain is promising for high frequency operation up to W-band.

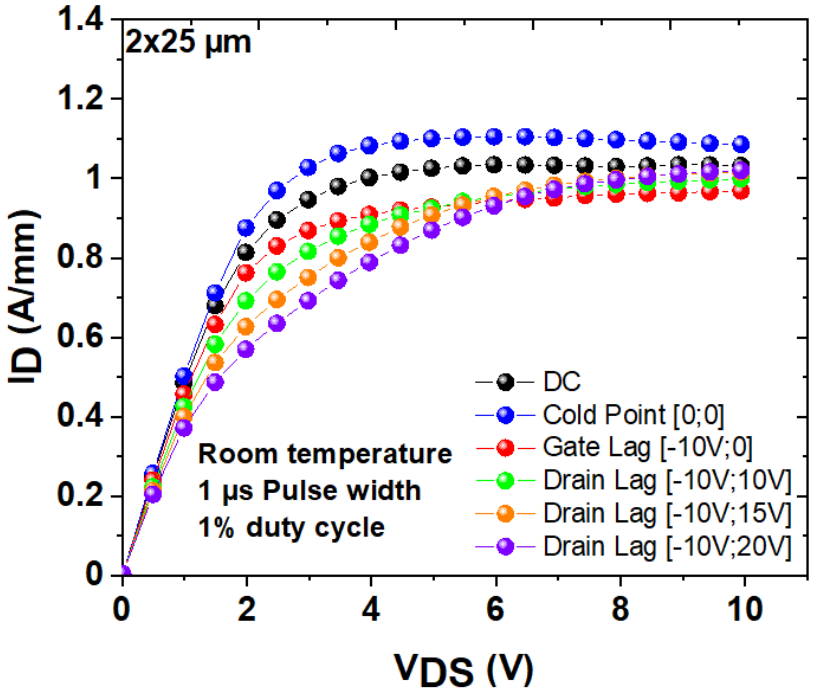


Figure.4.19. Pulsed I-V characteristics of 2×25 µm transistors with L_G = 130 nm and L_{GD} of 0.5 µm of structure B

II.3. State-of-the art InAlGaN/GaN HEMT technology

The InAlGaN/GaN technology is promising for high frequency operation owing to its excellent 2DEG properties. We demonstrated high RF performances at 40 GHz using this technology. **Figure.4.20** shows a benchmark representing the PAE as a function of the output power density for Ka to Q-band. Both CW and pulsed RF performances of our InAlGaN/GaN devices are reported. Despite severe trapping effects observed on this technology, a superior combination PAE/P_{OUT} in pulsed mode is demonstrated confirming the significant interest of this approach considering the large room for improvement within this technology.

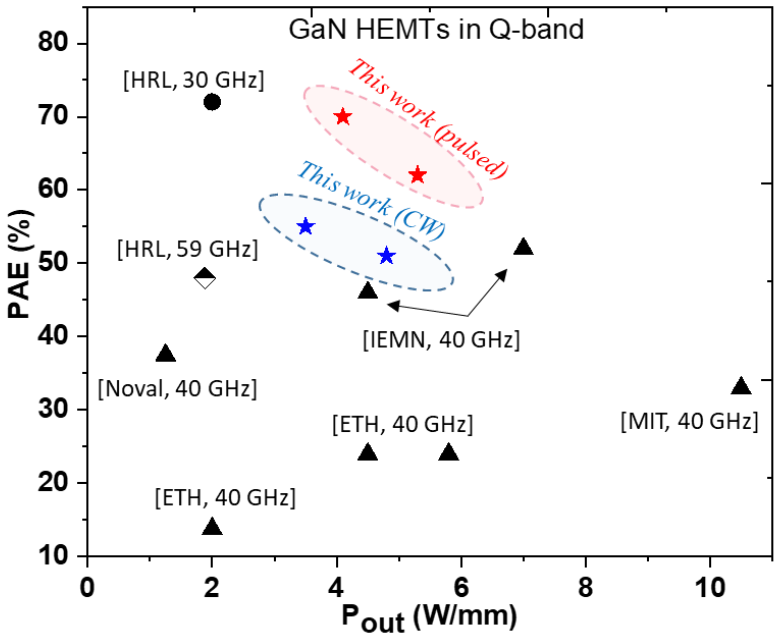


Figure.4.20. Benchmark of IEMN InAlGaN/GaN technology and reported GaN HEMTs in the literature at Ka-Q-band.

III. AlGaN/GaN buffer-free ultrathin HEMT technology

The structure shown in **Figure.4.21** without buffer layer has been grown by MOCVD on SiC substrate by the company SweGaN. This structure called QuanFine is grown in a Hot-Wall MOCVD equipment allowing the achievement of outstanding AlN nucleation layer quality and potentially enabling the direct growth of a GaN channel without using any transition layers.

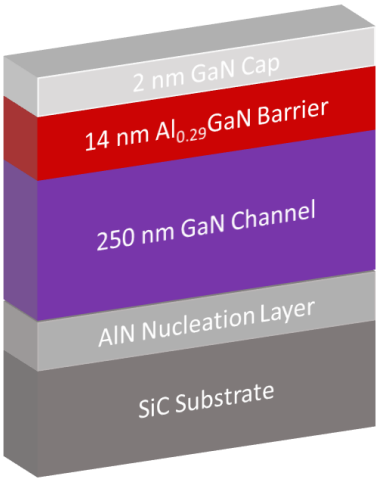


Figure.4.21. Schematic cross section of thin AlGaN/GaN hetrostructure without buffer layer.

The elimination of the buffer layer would definitely enhance the thermal dissipation, which is critical when using short gate lengths generating high electric field. In this case, the total thickness of the structure is less than 400 nm (compared to several µm for standard HEMTs). Hall Effect measurements shows excellent 2DEG properties with a sheet charge density of 1×10^{13} cm^{-2}, an electron mobility as high as 2200 $cm^2/V.s$ and sheet resistance of 320 Ω/□. This demonstrates the rather low defect density and high quality interfaces despite the absence of the buffer layers.

1) Device fabrication

The fabrication process has been carried out using the mask-set "GaN Fast". Partially recessed ohmic contacts has been used prior to the metallization using Cl_2A_r ICP plasma. Then a Ti/Al/Ni/Au metal stack annealed at 775°C has been applied to form source-drain ohmic contacts leading to a contact resistance of 0.45 Ω.mm extracted by TLM method. T-gates were defined by e-beam lithography, then Ni/Au was deposited directly on top of the AlGaN barrier layer. Finally, 200 nm PECVD SiN layer was deposited as final passivation. **Figure.4.22** shows various gate lengths fabricated on this structure.

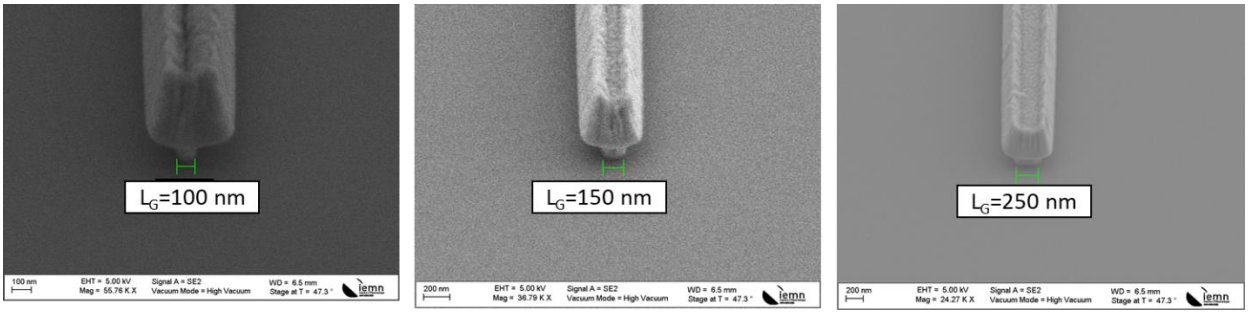


Figure.4.22. SEM images of various tilted gates

2) DC and small signal characterization

Figure.4.23 shows I-V (a) and pulsed I-V (b) characteristics of a 2 x 50 µm transistor with L_G = 100 nm and L_{GD} = 1.5 µm. The maximum drain current is about 0.85 A/mm (at V_{GS} = +2V). We observed from pulsed I-V characteristics (the gate and the drain lag) rather low trapping effects, which reflect the quality of the heterostructure despite the non-optimized surface passivation. **Figure.4.24** shows the output characteristics before and after SiN PECVD surface passivation. We observed a leakage current below 100 µA/mm and a pinch-off voltage about V_{th} = -3V. However, after surface passivation, the transistors exhibit a strong degradation of the off-state leakage current.

Therefore, no large signal characterization was possible on this structure due to the poor robustness. The reason is most probably due to the interface between the final passivation SiN PECVD and the GaN

cap layer that must be optimized. Several investigations are on-going on this structure in order to improve the passivation and thus increasing the robustness of these ultrathin buffer-free structure.

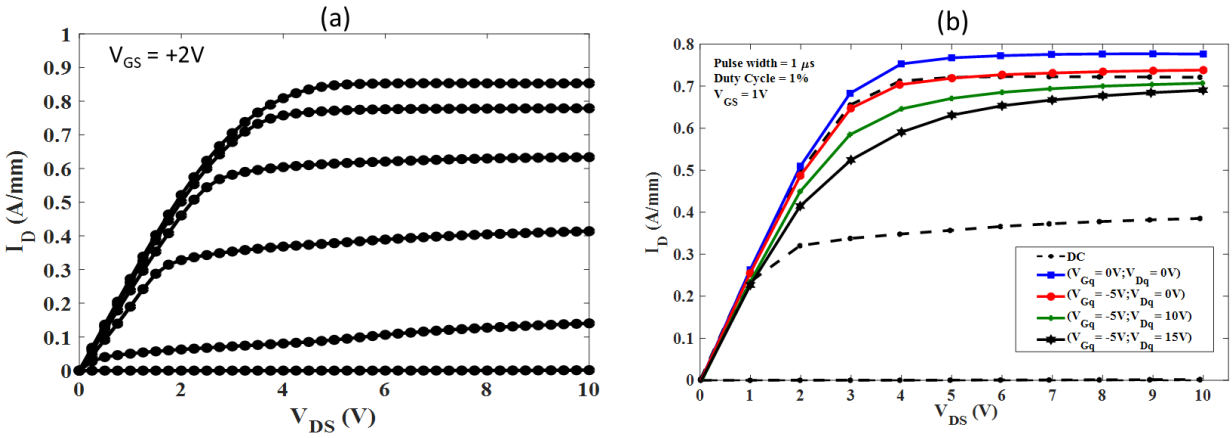


Figure.4.23. I-V (a) and pulsed I-V (b) characteristics of a 2×50 µm transistor with L_G = 100 nm and L_{GD} = 1.5 µm of the 14 nm AlGaN/GaN buffer-free structure.

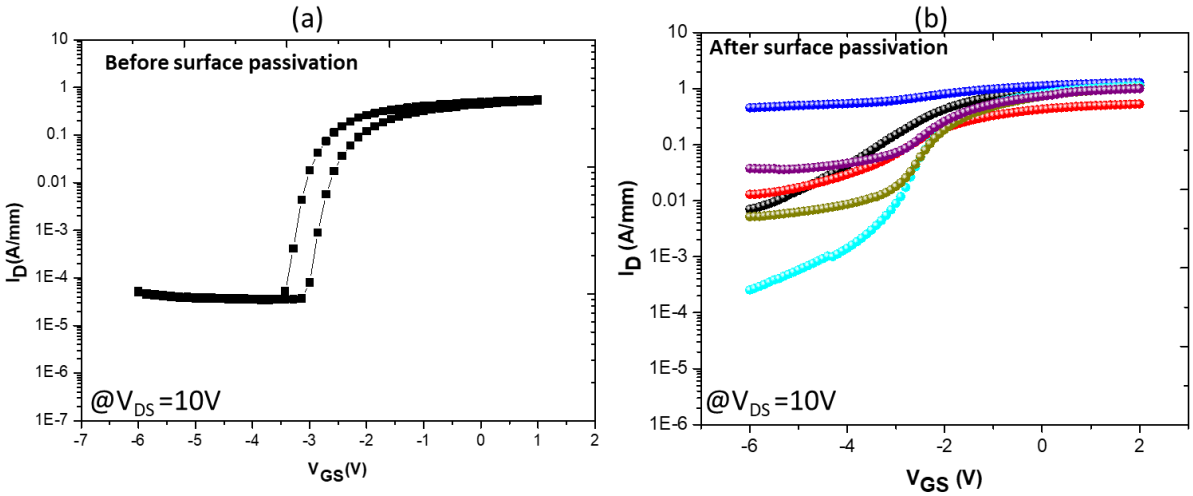


Figure.4.24. Output characteristics before (a) and after (b) SiN PECVD surface passivation of several 2×50 µm transistors with L_G = 100 and L_{GD} of 1.5 µm of the 14 nm AlGaN/GaN buffer-free structure.

IV. Conclusion

In this chapter, another InAlGaN barrier layer has been studied with the aim of developing a technology capable of providing high PAE, high output power density and superior device robustness at even higher frequency. This structure delivers indeed a much higher electron mobility than AlN/GaN and thus a higher power gain and current density. We demonstrated high power performances at 40 GHz despite the strong

trapping effects that need to be reduced. The same structure with thicker SiN cap and optimized process was performed and shows a promising reduction of trapping effects.

HRTEM structural characterization have been performed on InAlGaN/GaN to accurately determine the barrier composition of this structure. The results indicate a well-defined and uniform InAlGaN barrier layer indicating a high material quality.

Finally, a thin buffer-free HEMT technology has been studied. This structure from the company SweGaN based on 14 nm AlGaN barrier layer and a high AlN nucleation layer quality has been implemented in order to enhance the thermal dissipation. DC characteristics shows rather low trapping effects. However, no large signal characterization was possible due to the high leakage current after full passivation.

Conclusion

The interest for millimeter-wave frequency is continuously increasing due to the reduced wavelength and wide frequency bands enabling smaller components with enhanced performances. However, several challenges need to be overcome in order to use the mmW spectrum successfully. The targeted performances required for high frequency devices include a combination of high power/high efficiency, proven device reliability, compact size and low cost. GaN-based transistors are one of the most promising candidates in this frame.

In this work, the chapter 1 focused on the unique physical properties of III-nitride compound semiconductors, especially GaN material. The comparison between the material properties of commonly used semiconductors demonstrates the superiority of GaN over its counterparts; one of the challenges of GaN-based devices being the trapping effects and self-heating. GaN HEMT structures have been described showing the different configuration and specific material systems used for RF applications. The optimization of the epitaxial structure is crucial as it has a huge impact on device performances and robustness, especially under high electric field. An alternative material selection for millimeter-wave RF devices was outlined. The optimizations of GaN HEMTs for high frequency applications are needed not only for the epitaxial structure but also for the device fabrication. Some key processing steps for device scaling technology were described. Afterwards, a state-of the art of existing technologies in millimeter-wave range was reported.

The main objective of this research study was to push the limits of GaN HEMT power performances for future high frequency power applications. The targeted performances focused on high power-added-efficiency under high output power density together with the device reliability investigation, which were not demonstrated simultaneously so far in the literature.

In chapter 2, a description of the fabrication process development of GaN HEMTs and the key technological steps to achieve high performances at high frequency was discussed. Another part of this chapter presents the electrical characterization methods and tools used in this framework. The characterization campaigns spans from DC to large signal characterizations. Static and pulsed I-V characterization methods were reported. Afterwards, large signal characterization method using an active load-pull approach at 40 GHz was discussed. For device measurements at higher frequency, we used a passive load-pull at 94 GHz, which was described. Finally, the implementation of a new bench using active load-pull method was also discussed.

In chapter 3 and 4, the electrical and structural characterizations of different structures carried out at IEMN with the support of our partners (Padova, C2N) were presented. We first demonstrated the scaling issues of standard AlGaN/GaN heterostructure for millimeter-wave applications and the interest to moving towards to ultrathin Al-rich barrier layers. We studied the impact on the device performances using different buffer design and channel thickness. A matrix based on an extensive experimental variation of these 2 parameters showed a clear trade-off between the trapping and short channel effects. Two HEMT structures based on 3 nm and 4 nm AlN/GaN HEMTs were performed showing superior performances for the 3 nm AlN/GaN structure with a record PAE above 70% with an associated P_{OUT} of 5 W/mm. Interestingly, RF short-term reliability demonstrated a strong robustness up to V_{DS} = 20V at 140°C unlike the 4 nm AlN/GaN structure. This has been confirmed by the University of Padova, which has demonstrated a superior robustness for the 3 nm AlN/GaN as compared to the 4 nm AlN/GaN structure. The results were in agreement with RF short-term reliability. The electrical characterization difference between the two structures was correlated to the Al-distribution within the structures, which showed a thicker AlGaN transition layer for the 4 nm AlN/GaN structure compared to the 3 nm AlN/GaN structure. This analysis was carried out with HRTEM at C2N laboratory. A shared processing of 3 nm AlN/GaN technology with UMS foundry was reported showing high performances at 40 GHz and high robustness on multi-fingers, application representative transistors. Finally, large signal characterization at 94 GHz using passive load-pull bench on the 3 nm AlN/GaN was performed showing a state-of-the art P_{OUT} of 4W/mm exceed any Ga-polar technology. Further efforts are needed to improve the W-band PAE. Some preliminary studies have been performed on a quaternary sub-10 nm InAlGaN barrier delivering high electron mobility and a buffer-free structure enabled by a high quality AlN nucleation layer grown by hot wall MOCVD.

Outlooks and future work

- **InAlGaN/GaN and AlN/GaN structures with low trapping effects:**

As discussed in chapter 3 and 4, the AlN/GaN and InAlGaN/GaN structures (see **Figure.1**) have shown high RF performances. However, the devices still show rather strong trapping effects especially for InAlGaN/GaN structure as seen from the gate/drain lag and the performance gap between CW and pulsed mode, especially for the PAE. We identified by HRTEM that a part of traps is attributed to the fabrication process and the gate etching using SF_6 plasma. At the end of this thesis, we developed a new gate etching process based on an in-situ A_r etching.

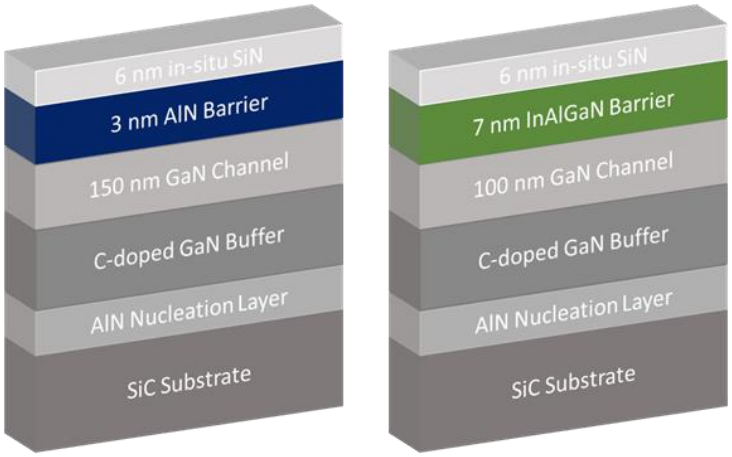


Figure.1. Schematic cross section of the AlN/GaN and InAlGaN/GaN structures

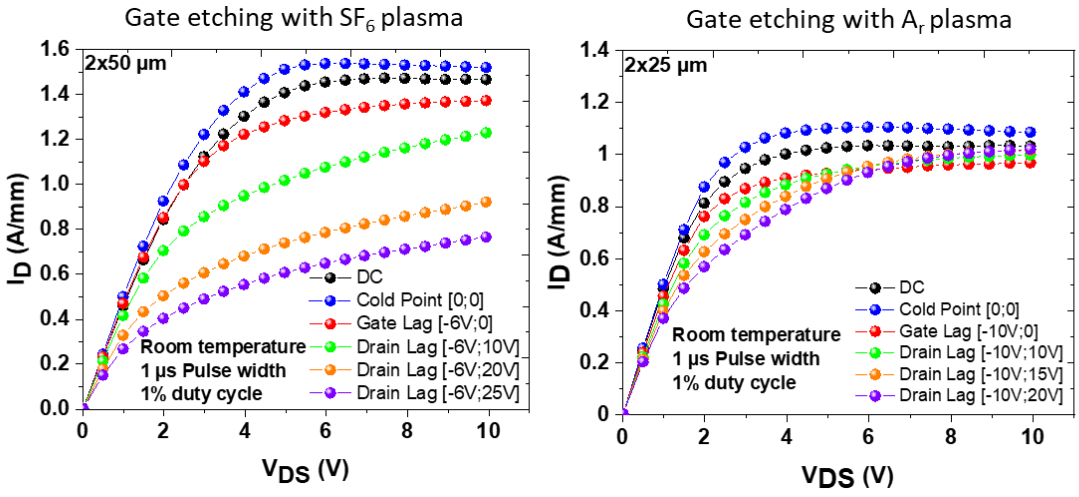


Figure.2. Pulsed I-V characteristics of InAlGaN/GaN structure using two different gate etching process

This process has been applied on the InAlGaN/GaN structure showing low trapping effects with preliminary DC characterization (see **Figure.2**). On top of trapping reduction, shorter sub-100 nm gate lengths can be achieved using this process by avoiding the lateral etching occurring during the fluorine-based plasma. Therefore, the realization of components with the new gate etching process will be carried out in order to observe a potential improvement up to 94 GHz.

❖ Combining AlGaN back barrier with higher Al-content and C-doping:

The concept consists in inserting an AlGaN back barrier between a low C-doped buffer and the undoped GaN channel. The aim is to provide an electrostatic barrier combined with a highly resistive buffer to limit the leakage current while benefiting from low trapping effects as low C-doped buffer away from the 2DEG is used. Preliminary results obtained in this thesis showed the feasibility of this approach. However, the electron confinement was not optimum with the short gate lengths due to the too low Al-content in the AlGaN back barrier. Therefore, a higher Al-content in the AlGaN back barrier using the same configuration should be used (See **Figure.3**). We expect from these structures that has been grown a good electron confinement together with low trapping effects as a Fluorine-free gate etching process will be applied.

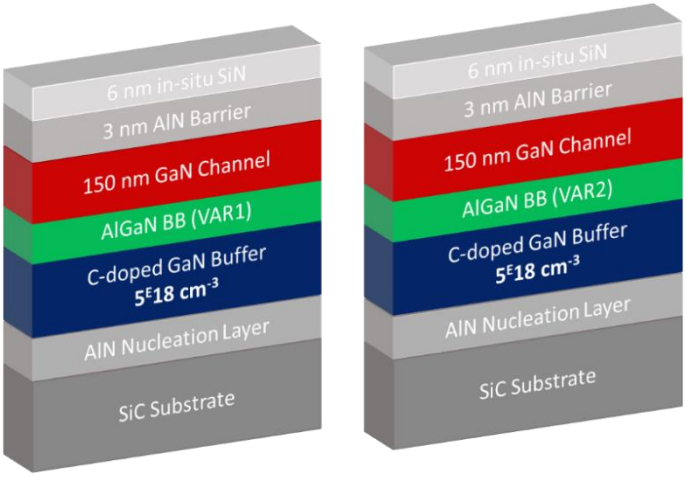


Figure.3. Schematic cross section of the 3 nm AlN/GaN structures with an AlGaN back barrier combined with a C-doped buffer

❖ GaN structure on hybrid substrate

Highly resistive SiC substrates are well suited for GaN-based stack growth for RF components due to their low lattice parameter difference and thermal expansion coefficient. However, they are currently very expensive and not widely available in Europe. SOITEC has recently started an innovative development in collaboration with "Applied Materials" with the aim of producing a new generation of hybrid SiC substrates

based on their smart-cut know-how. As shown in **Figure.4**, SOITEC solution consists in a thin highly resistive SiC transfer using a thermally and electrically conductive bonding on a low-cost substrate, resulting in a less expensive solution. The RF losses as well as the quality of epitaxial structure should be identical to that of standard SiC substrates. Several low cost receiving substrate are possible for the transfer of the monocrystalline and highly resistive SiC layer:

- Polycrystalline 'low cost" SiC substrate
- Polycrystalline AlN substrate
- Highly resistive silicon substrate

This study will be part of the PhD thesis from François Grandpierron in our research group.

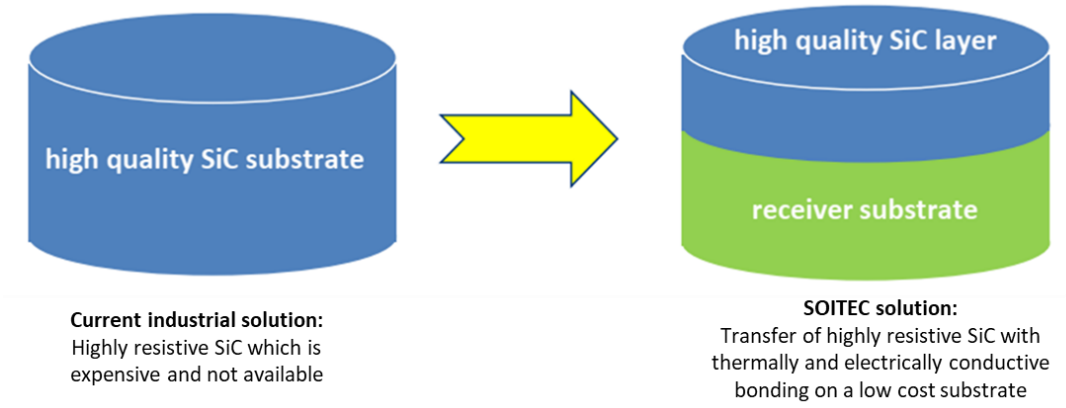


Figure.4. Transfer of highly resistive SiC using a thermally and electrically conductive bonding on a low cost substrate

❖ **Power bench development for pulsed large signal characterization at 94 GHz**

In order to assess the device performances in W-band, an active load-pull large signal characterization bench at 94 GHz will be further optimized. **Figure.5** shows the synoptic of 94 GHz pulsed load-pull. The primary aim of the pulsed mode is to investigate both the trapping effects and self-heating of the transistors in operational conditions. External pulse generators that provide the pulsed bias excitation will be added to the active load-pull setup. Specific probes associated with an oscilloscope will be used to measure the current and voltage of the transistors. Figure shows the synoptic of the active CW and pulsed load-pull bench.

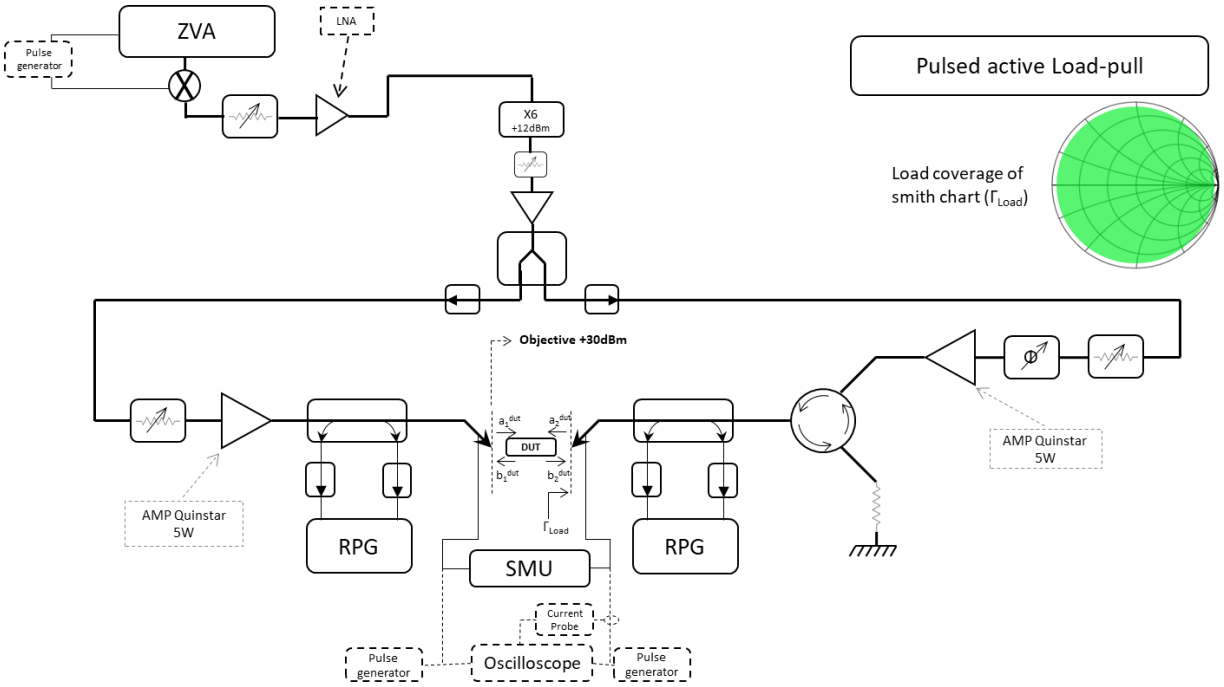


Figure.5. High power active load-pull setup in CW and pulsed configuration

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Publications related to this PhD thesis

❖ Journals

1) High Performance and Highly Robust AlN / GaN HEMTs for Millimeter-Wave Operation

K. Harrouche, R. Kabouche, E. Okada, and F. Medjdoub. IEEE J. Electron Devices Soc., vol. 7, pp. 11451150, 2019

2) High Efficiency AlN/GaN HEMTs for Q-Band Applications with an Improved Thermal Dissipation

R. Kabouche, Romain Pecheux, **Kathia Harrouche**, Etienne Okada, and Farid Medjdoub. Int. J. High Speed Electron. Syst., vol. 28, no. 12, pp. 111, 2019

❖ National and international conferences

1) Scaling of AlN/GaN HEMT for millimeter-wave power applications

K. Harrouche, R Kabouche, M. Zegaoui, F. Medjdoub. 43rd Workshop on Compound Semiconductor Devices and Integrated Circuits, WOCSDICE 2019, Jun 2019, Cabourg, France

2) Short-term reliability of high performance Q-band AlN/GaN HEMTs

R. Kabouche, **K. Harrouche**, E. Okada, F Medjdoub. IEEE International Reliability Physics Symposium (IRPS 2020), Apr 2020, Dallas, TX, United States. pp.1-6, ⟨10.1109/IRPS45951.2020.9129322⟩

3) High Power AlN/GaN HEMTs with record power-added-efficiency >70% at 40 GHz

K. Harrouche, R. Kabouche, E. Okada, and F. Medjdoub. 2020 IEEE/MTT-S International Microwave Symposium (IMS)

4) Short Term Reliability and Robustness of ultra-thin barrier, 110 nm-gate AlN/GaN HEMTs

Zhan Gao, Matteo Meneghini, **Kathia Harrouche**, Riad Kabouche, Francesca Chiocchetta, Etienne Okada, Fabiana Rampazzo, Carlo de Santi, Farid Medjdoub, Gaudenzio Meneghesso, Enrico Zanoni. 2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)

5) Above 70% PAE in Q-band with AlN/GaN HEMTs structures

K. Harrouche, R. Kabouche, E. Okada, and F. Medjdoub. WOCSDICE2021, Jun 2021, Bristol, United Kingdom. ⟨hal-03279173⟩ → **Best paper award given at WOCSDICE/EXMATEC 14 – 17 June 2021, Bristol (UK)**

❖ Book chapter

1) GaN-Based HEMTs for Millimeter-wave Applications

Kathia Harrouche and Farid Medjdoub. book: Nitride Semiconductor Technology: Power Electronics and Optoelectronic Devices, 03 August 2020

❖ Press release

1) Making more efficient, more reliable millimetre-wave HEMTs

K. Harrouche, R. Kabouche, and F. Medjdoub. magazine: Compound Semiconductor, volume 27 Issue 2

2) Communiqué de presse à l'université de Lille. Vers des transistors de puissance à haut rendement en gamme d'ondes millimétriques. 2021

3) Preindustrial GaN devices developed at the nanofabrication center of IEMN

K Harrouche, W Rili, E Carneiro, J Mehta, I Abid, F Medjdoub. Transducers 2021, Jun 2021, online France

Overview of samples used in this work

Structure Description	Gate length (nm)	Device design (µm)	$I_{DS\,max}$ (A/mm)	DIBL (mV/V)	Transconductance G_m (mS/mm)	f_t/f_{max} (GHz) U_{max} (dB)	Frequency (GHz)	P_{OUT} (W/mm) @V_{DS}= 20V	PAE (%) @V_{DS}= 20V	Robustness After LP	Short term reliability @40 GHz	Remarks	Processed samples
15nm AlGaN/GaN HEMT	• *Study of the AlGaN/GaN HEMTs and their limits for millimeter-wave range*											Drain leakage increases with high Al-content	4 samples
3nm AlN/GaN HEMT GaN channel variation vs Buffer variation	• *Study of the channel thickness vs C-doping concentration in the buffer* • *Study of the AlGaN Back Barrier*											Trade-off between the channel thickness and the C-doping buffer concentration	12 samples
10nm SiN/4nm AlN/GaN HEMT	105	2 x 50	1.4	55	400	75/200 14 @V_{DS}= 20V	40	2.9 (CW) 3.2 (pulsed)	45 (CW) 61 (pulsed)	Degradation at V_{DS}= 20V	Degradation at V_{DS} = 12V @Room temperature	- High trapping effects - Poor robustness	> 5 samples
10nm SiN/3nm AlN/GaN HEMT	105	2 x 50	1.1	36	450	75/210 15 @V_{DS}= 20V	40	2.6 (CW) 3.5 (pulsed)	60 (CW) 72 (pulsed)	No degradation up to V_{DS}= 30V	No degradation up to V_{DS} = 20V @140°C	- High robustness - Trapping effects to be optimized - Structure to be carried out with active LP @94GHz	> 10 samples
							94	4 (CW)	14 (CW)	No degradation up to V_{DS}= 20V	NA		
10nm SiN/3nm AlN/GaN HEMT	105	2 x 50 UMS PCMs	1.1	NA	450	50/135 11 @V_{DS}= 20V	40	3.2 (CW) 3.5 (pulsed)	51 (CW) 57 (pulsed)	No degradation up to V_{DS}= 20V	NA	- High trapping effects - SiN extra-passiv to be replaced with SiO_2	2 - 4" wafers
10nm SiN/3nm AlN/GaN HEMT	105	4 x 50 UMS PCMs	1.1	NA	450	50/130 10.2 @V_{DS}= 20V	40	3.3 (CW) 3.6 (pulsed)	44 (CW) 50 (pulsed)	No degradation up to V_{DS}= 20V	NA	- High trapping effects - SiN extra-passiv to be replaced with SiO_2	4 – 4" wafers
2.5nm SiN/6nm InAlGaN/GaN	100	2 x 50	1.5	14	580	75/300 18 @V_{DS}= 20V	40	3.5 (CW) 4.1 (pulsed)	55 (CW) 70 (pulsed)	Degradation at V_{DS}= 20V	NA	- Sever trapping effects	> 5 samples
6nm SiN/7nm InAlGaN/GaN	130	2 x 50	1.1	29	NA	NA	NA	NA	NA	NA	NA	- Low trapping effects - Further optimizations and characterizations will be carried out	4 samples
2nmGaN/14nm AlGaN/GaN (Thin HEMT)	100	2 x 50	0.85	NA	NA	NA	NA	NA	NA	NA	NA	- Low trapping effects - Poor robustness - Epitaxial structure to be optimized	4 samples