Université de Lille

Ecole Doctorale Sciences de l'Ingénierie et des Systèmes

THESE

pour l'obtention du grade de

Docteur de l'Université de Lille

Specialité: Electronique, Microélectronique, Nanoélectronique et Micro-ondes

par

Edoardo BREZZA

soutenue le 16 décembre 2022 à Grenoble

Development and Evaluation of a New Si/SiGe Heterojunction Bipolar Transistor Architecture for a High-Performance and Low Cost 55 nm BiCMOS technology.

Membres du Jury:

Pr. Florence PODEVIN - TIMA UGA	Présidente du Jury
Pr. Fabien PASCAL - IES Université de Montpellier	Rapporteur
Pr. Dimitri LEDERER - UCLouvain	Rapporteur
Dr. Virginie NODJIADJIM - III-V Lab	Examinatrice
Pr. Thomas ZIMMER - IMS Bordeaux	Examinateur
Dr. Pascal CHEVALIER - STMicroelectronics	Examinateur
Dr. Alexis GAUTHIER - STMicroelectronics	Examinateur
Pr. Christophe GAQUIERE - IEMN	Directeur de Thèse
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Les cent-cinquante pages de ce manuscrit ne suffiraient pas à décrire les trois années (et demi) folles et denses pour lesquelles le travail de cette thèse est raison et cadre.

Laissez-moi pour autant utiliser ce petit espace pour rendre honneur à qui fait désormais partie de ma collection de papillons. Ces papillons très chers à moi car trouvés dans mon jardin, ceux qui m'ont permis de fleurir encore et encore dans chaque saison, ceux qui m'ont fait savourer ces timides et fugaces éclaircis de beauté.

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A vous, tous : merci pour les roses, merci pour les épines.

Considerate la vostra semenza:
Fatti non foste a viver come bruti
Ma per seguir virtute e canoscenza

Considérez la race dont vous êtes,
Créés non pas pour vivre comme brutes,
Mais pour suivre vertu et connaissance.

Consider the seed that gave you birth:
You were not made to live as brutes,
But to follow virtue and knowledge.

Dante Alighieri, *La Divina Commedia*
Inferno, Canto XXVI, vv.118-120

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Glossary

BiCMOS A technology integrating both Bipolar and CMOS transistors in addition to passives devices on the same wafer.

BiCMOS055 (B55) A 55 nm BiCMOS technology developed by STMicroelectronics, basis of the present study.

BiCMOS055X (B55X) A 55 nm BiCMOS technology developed by STMicroelectronics, context in which this study has been conducted.

Bipolar Junction Transistor (BJT) A type of junction transistor which has been dominant in older analogic and digital technologies.

Buried OXide (BOX) The oxide layer buried into a SOI substrate.

Chemical Mechanical Polishing (CMP) A process used for planarizing and polishing a wafer. It uses mechanical abrasion along with chemical etching, resulting in a very good surface uniformity.

Chemical Vapour Deposition (CVD) A deposition technique based on the decomposition of a precursor gas on a solid surface and the consequent deposition of the desired material. Many materials can be deposited by this technique.

Complementary Metal Oxide Semiconductor (CMOS) A logic family based on n- and p-type MOSFET devices, dominant in nowadays digital circuits.

Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) A particular Heterojunciton Bipolar Transistor architecure, also used in STMicroelectronics' BiCMOS055 technology.

End Of Range (EOR) defects Defects generated outside the range amorphized by ion implantation.

Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) SiGe Heterojunction Bipolar transistor (HBT) architecture, the name stands for stands for Epitaxial eXtrinsic Base isolated from the Collector

Extrinsic collector/base Collector/base portion not directly playing in the transistor effect. These parts are important because they still play a role as parasitics, potentially having a big impact on performance.

Figure Of Merit (FOM) A numerical quantity based on one or more characteristics of a system or device that represents a measure of efficiency or effectiveness. (Merriam Webster)

Front End Of Line (FEOL) Part of the fabrication of an integrated circuit consisting in the realization of devices on silicon. It includes all fabrication processes up to the contact.

Go To EXBIC architecture The EXBIC architecture as defined after solving the problems affecting the preliminary EXBIC architecture. Chacteristic features are single SSTI and 1-step extrinsic base epitaxy.

Heterojunction Bipolar transistor (HBT) An improved version of the BJT based on heterojunctions.

Integrated Device Manufacturer (IDM) A company responsible for all the aspects of the production of an integrated circuit, from design to fabrication.

Intrinsic collector/base Collector/base portion playing a direct role in the transistor effect. It is generally used to refer to the portion close to the p-n junctions and delimited by the emitter window width.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) A modern field-effect transistor, dominant in the nowadays digital circuits for its superior performance in this field.

Non-Product Wafer (NPW) Wafer not integrating any device structure, i.e. with a plain surface

Preliminary EXBIC architecture The EXBIC architecture as it was at the beginning of this work. Chacteristic features are ring SSTI and 2-step extrinsic base epitaxy.

Safe Operating Area (SOA) Biasing limits beyond which the device could face permanent alteration of its characteristics or destruction.

Selectively Implanted Collector (SIC) A collector implantation circumscribed below the emitter window and used to adjust the base-collector junction in Hig-Speed HBTs.

Shallow Trench Isolation (STI) Vertical trench with a depth on the order of the hundreds od nanometers, used for electrical isolation between zones.

Silicon On Insulator (SOI) Particular type of silicon substrate featuring an oxide layer buried below the surface.

Smith Chart The Smith chart is a convenient way to represent parameters useful for describing the RF behavior of a device on a complex plane, e.g. impedances, reflection coefficients and scattering parameters.

Super Shallow Trench Isolation (SSTI) Vertical trench with a depth below 150 nm.

Technology Computer-Aided Design (TCAD) Design of semiconductor devices with the help of computer simulations.

Tetraethoxysilane (TEOS) Chemical compound with the formula $Si(OC_2H_5)_4$ used as a precursor in silicon oxide Chemical Vapour Deposition (CVD).

Time Of Flight - Secondary Ion Mass Spectroscopy (TOF-SIMS) Destructive analysis of the atom distribution present in a bulk. Energetic high-mass ions are sent to the surface, detaching the bulk atoms; mass spectroscopy allows to identify the detached atoms.

Transient Enhanced Diffusion (TED) Particularly important for Boron and Phosphorus, consists in an enhanced diffusivity when Silicon self-interstitials are present, generally after ion implantation.

Chapter I

Introduction

The tools needed for understanding the present work are here introduced.

This chapter introduces all the concepts needed for understanding this work and its scope. A glimpse to the context that led to the development of BiCMOS technologies opens the discussion.
The principal figures of merit are reviewed.
The state of the art is then examined by discussing the most recent solutions presented by the actors of current BiCMOS developments.
Finally, a focus on Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) architecture used for BiCMOS055 technology by STMicroelectronics will pave the way for the introduction of Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) Heterojunction Bipolar transistor (HBT)s, which makes the object of this study.

1 Context

After its invention in 1948 by John Bardeen, William Shockley and Walter Brattain, the Bipolar Transistor has become a milestone in human history.

Figure I.1 | Bardeen, Brattain and Shockley, discoverers of the transistor effect. (Picture by AT&T. Public domain.)

Celebrated with a Nobel prize to its inventors in 1956, it rapidly substituted the thermionic valves thanks to its reduced dimensions and cost in addition to better performances. The invention of dedicated logic families, the amelioration of the production processes and the development of reliable integrated circuits paved the way to modern electronics. In the meanwhile, the advancements in MOSFET technologies made the development of CMOS logic possible, replacing bipolar-based logics thanks to its high noise immunity and low static power.

Nowadays, most electronic circuits are based on CMOS technologies. The virtues that led to the domination of this technology, however, could not face all the strengths of the Bipolar Junction Transistor (BJT), which kept its superiority in high-frequency applications. Indeed, bipolar transistors outperform MOSFETs by a couple of technology nodes when compared on RF capabilities due to the intrinsic limitations of such devices. The necessity

of combining the CMOS logic capabilities with the *RF* BJT strengths in the same integrated circuit led to the development of BiCMOS technologies.

In order to keep increasing performances whilst being compatible with CMOS-process, the structure of the original bipolar device has been radically changed:

- Bandgap engineering became a new possibility thanks to the development of SiGe alloys fabrication processes. The Heterojunction Bipolar Transistor (HBT) is an improved type of bipolar transistors that uses a graded SiGe profile in the base to overcome its intrinsic gain-bandwidth limitations.

- The original simple planar layout has evolved to more complex and efficient vertical structures. Advancements in production techniques led to structure shrinkage and increase of complexity in order to ensure higher performances and integration density. While old fabrication processes required very simple integrations based on diffusion doping, modern equipments allow to combine ion implantation and in-situ epitaxy doping to obtain very complex and tiny structures.

- The production flow of a full-bipolar integrated circuit has been adapted to the constraints of a modern CMOS-based platform, leading to particular integration choices. The big difference between the fabrication processes of the two kind of devices is a big constraint during development.

Such innovations allowed to increase maximum frequencies from 500 MHz to above 300 GHz in more than 50 years. Device size shrinked from hundreds of μm down to the nanometric scale.

BiCMOS technologies are used nowadays in multiple *RF* applications where higher performance with respect to pure CMOS technologies has to be combined with smaller cost-per-chip with respect to III-V technologies. Bipolar transistors outperform MOSFET in terms of power amplification, low-frequency noise and reliability. Devices based on III-V semiconductors are capable of reaching much higher performances than HBT but are hindered by wafer size and yield, making them a costly solution not suitable for high-volume production. For all the fields needing high *RF* performance, mixed-signal capabilities, reduced dimensions, relatively low cost and mass

production, BiCMOS is the technology of choice. Typical commercial applications are optical fiber datacom or wireless networks [66]. Figure I.2 sketches the many systems in which BiCMOS technologies can be found.

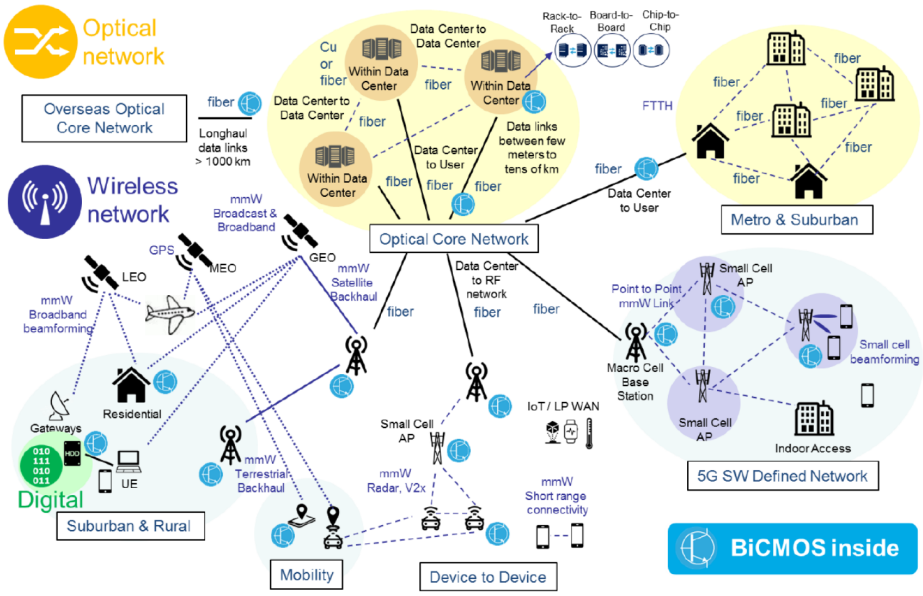

Figure I.2 | Typical applications of BiCMOS technologies in final devices.[9]

2 Figures Of Merit

Figures of merit must be defined to evaluate the performance of a device and set a common ground for discussion. The most important parameters for both *DC* and AC operations will be presented here. HBT theory has been widely treated in literature [1, 10] and will not be repeated here. Since this work is a study on an npn transistor, the following definitions and conventions will be related to this device. More details about some figures of merit will be given in the following chapters when the relative device component will be treated.

2.1 Voltage references and operating zones

Figure I.3 depicts the naming convention for the electric terminals as well as for currents and bias voltages. Biasing of the two pn junctions regulates carriers flow through the device (Figure I.4) and four regions of operation can be defined:

Cut-off Each junction is reversely biased and carriers cannot flow through the device.

Saturation Each junction is forward biased. Net current flow will be directed towards the higher potential terminal.

Forward active Emitter-base junction is forward biased and base-collector junction is reversely biased. Output emitter current is obtained from the sum of input base and collector currents.

Reverse active Base-collector junction is forward biased and emitter-base junction is reversely biased. Output collector current is obtained from the sum of input base and emitter currents.

2.2 Currents and gain

Simplified formulas for collector and base current can be obtained with the approximation of abrupt and constant doping profiles and assuming ideal behavior of the device:

$$I_C = \frac{qAD_{nb}n_{i,B}^2}{W_B N_{ab}} exp\frac{qV_{BE}}{k_B T} \tag{I.1a}$$

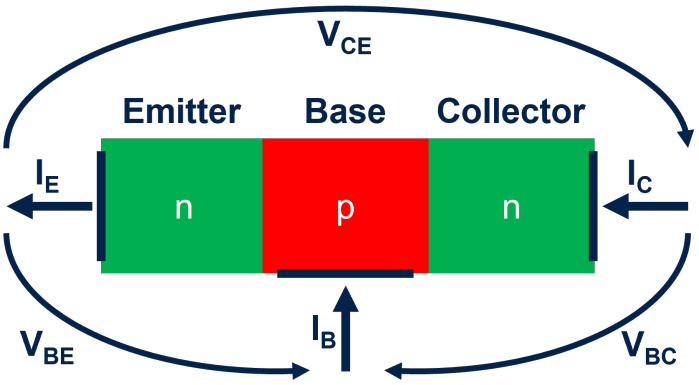

Figure I.3 | Schematic of an npn transistor with conventional currents and voltages in forward active region.

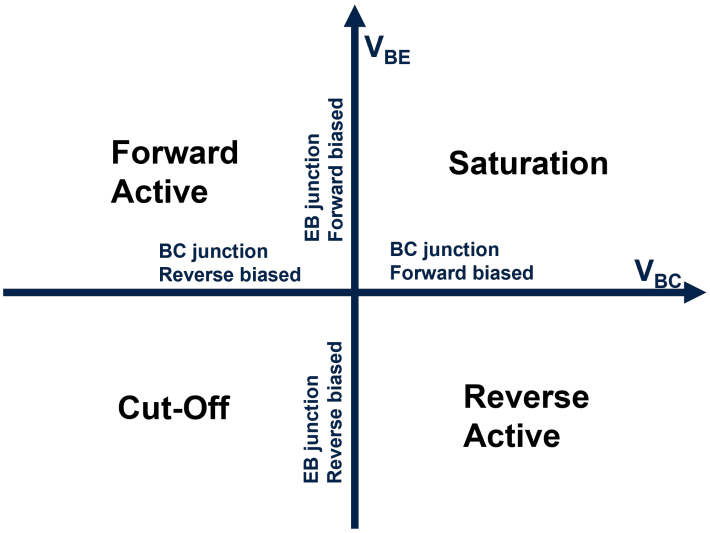

Figure I.4 | Regions of operation of a bipolar transistor based on junctions biasing.

$$I_B = \frac{qAD_{pe}n_{i,E}^2}{W_E N_{de}} exp \frac{qV_{BE}}{k_B T} \tag{I.1b}$$

Where q is the electron charge; A the junction area; D the diffusivity of electrons (n) or holes (p) in base (b) or emitter (e); n_i, B the intrinsic carrier density in the base and n_i, E in the emitter; W the width of base (B) or emitter (E); N the density of donors (d) or acceptors (a) in emitter (e) or base (b); V_{BE} the base-emitter voltage; k_B the Boltzmann constant; T the temperature.

The emitter current is related to the other two through a simple equation:

$$I_E = I_B + I_C \tag{I.2}$$

Current gain can be defined in different ways:

$$\alpha = \frac{I_C}{I_E} \tag{I.3a}$$

$$\beta = \frac{I_C}{I_B} \tag{I.3b}$$

Where α is the common base current gain and β is the common emitter current gain. Real devices can exhibit current leakages at low injection due to various phenomena inducing carrier generation and recombination. Two figures of merit are introduced to monitor them: collector current ideality factor η_{I_C} and base current ideality factor η_{I_B}. Ideality factors describe the gap between measured current values and those theoretically obtained if currents had a perfectly exponential dependence on junction voltages. An ideality factor of 1 means the device behaves perfectly, while bigger values indicate some non-idealities. Figure I.5 represents the effect of low-injection non-idealities on base current I_B.

Quasi-saturation is an effect related to collector resistance. When currents grows enough, the voltage drop across the collector resistance becomes large enough to counter the applied base-collector voltage. Consequently, the junction depletion region decreases in size as current increases, widening the neutral base and generating a negative feedback. If the current increases too much, it is also possible that the effective bias on the junction reverses, driving the device into saturation. Figure I.5 shows the impact of quasi-saturation on collector current.

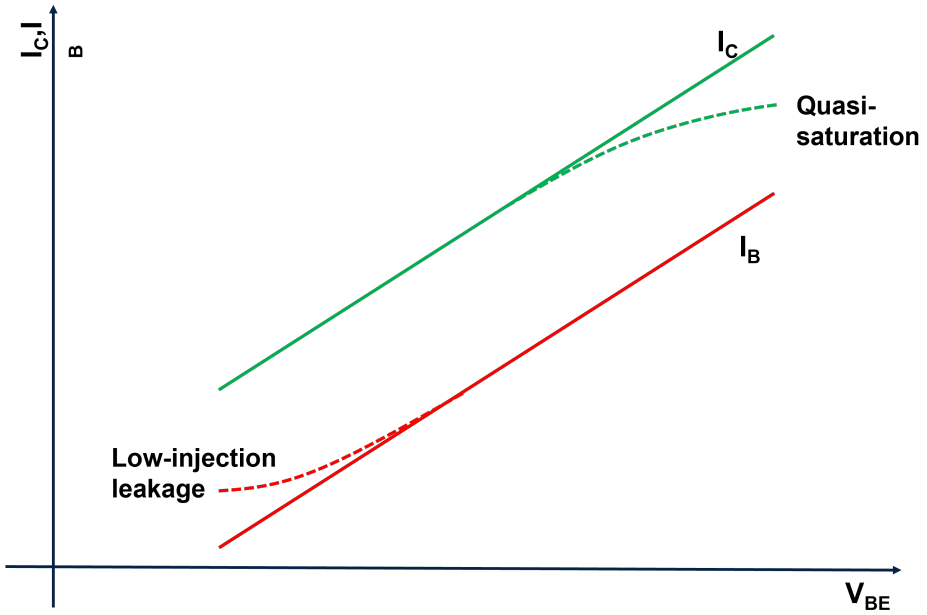

Figure I.5 | Impact of some current non-idealities on Gummel plot.

Kirk effect is another phenomenon occurring at high injection. When collector current is high enough, electrons transiting through the device have a non-negligible density when compared with the fixed charges (N_A in the base, N_D in the collector). At increasing currents, electrons will start to contribute significantly to junction electrostatics, shifting the depletion regions by acting on electric field. This effect, also known as electric-field screening, is particularly important for the base-collector junction, where the depletion region is progressively pushed out of the base, modifying its effective width. To an extreme point, the base will not be depleted anymore and the transistor will not work as expected.

2.3 Early voltages

Junction bias can have an appreciable impact on depletion regions, indirectly modulating neutral base width. Even if a fixed base width is considered in the current Equation (I.1a), it actually changes depending on the applied V_{BE} and V_{BC} voltages. This phenomenon, known as Early effect, can cause an important variation in the device characteristic in the forward active region, implying some difficulties in circuit design. Two figures of merit evaluate the

impact of this effect on device behavior: forward Early voltage V_{AF} and reverse Early voltage V_{AR}, related to base-collector and emitter-base junctions respectively. High values of Early voltages relate to a base less influenced by biasing and to a more stable collector current as a consequence.

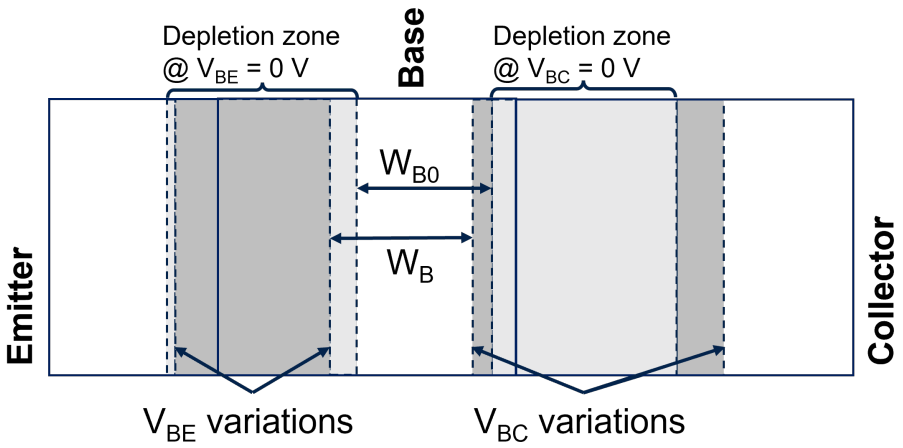

Figure I.6 | Schematic representing the impact of junction biasing on depletion zones. W_{B0} is the neutral base width of an unbiased device; W_B is the neutral base width of a biased device.

2.4 Breakdown voltages

When accelerated to high speeds, an electron acquires enough kinetic energy to ionize an atom by impact. When this occurs within the depletion region of a junction, the electron extracted by ionization can be accelerated by the electric field and ionize another atom. This effect can snowball inducing a cascade of ionizations and creating a massive current typical of the so-called avalanche breakdown. Ionization by impact and the rapid rise in temperature due to the massive current flux can induce permanent alterations of the device. Safe Operating Area (SOA) can be defined from breakdown voltages.

The critical voltage for a reverse-biased pn junction can be expressed as:

$$BV = \frac{\epsilon_0 \epsilon_r E_{crit}^2}{2qN} \tag{I.4}$$

Where ϵ_0 is the vacuum permittivity; ϵ_r is the relative permittivity; E_{crit} is the critical electric field for attaining impact ionization; N is the dopant concentration. The technological parameter regulating breakdown voltages is constituted by the doping level, posing a constraint on device design.

Three main breakdown voltages can be defined for a BJT (or HBT):

BV_{CB0} Breakdown voltage measured between base and collector with floating emitter. This value generally depends from base doping.

BV_{EB0} Breakdown voltage measured between emitter and base with floating collector. Notice that this value is obtained by reverse biasing the junction, i.e. outside the limits of forward active region. This value generally depends from emitter doping.

BV_{CE0} Breakdown voltage measured between collector and emitter with floating base. Biasing the device in such way reverse biases the base-collector junction, reproducing the same effect observed for BV_{CB0}. The two figures of merit are related by the equation:

$$BV_{CE0} = \frac{BV_{CB0}}{\sqrt[\gamma]{\beta}} \tag{I.5}$$

Where γ is defined by the breakdown severeness and β is the common emitter current gain. Typical values of γ are between 3 and 6.

2.5 Transit frequency

A way of representing high-frequency behavior of an amplifying device is to define its gain-bandwidth product. The transit frequency f_T of a transistor is defined as the frequency at which the current gain drops to 1. Such definition is valid for a small-signal current gain h_{fe} obtained in a common emitter configuration and with a short-circuit load. This is equivalent to having a value $h_{21} = 0$ dB in the S-matrix representation of the device.

Since the device reaches way higher frequencies than the ones handled by usual measurement equipments, the value of f_T is extrapolated from measurements performed at lower frequencies on the -20 dB/dec current-gain slope. Once the extrapolation frequency f_{extr} set, the transit frequency can be obtained:

$$f_T = h_{fe,extr}\, f_{extr} \tag{I.6}$$

where $h_{fe,extr}$ is the small-signal common-emitter gain at the extrapolation frequency f_{extr}.

Transit frequencies reported in this work are normally referring to an extrapolation frequency f_{extr} of 20 GHz. Tolerance on measured values can go up to 5 % on a well-performed setup.

High-frequency behavior of the bipolar transistor is determined by minority carriers stored in the different parts of the transistor. The capability to remove such carriers determines the speed at which the device can switch and therefore its maximum operating frequency. For an ideal device, the transit time τ_F defines such limit. In a real device, parasitics come to play and limit the speed at which excess carriers can be evacuated.

A simple yet fairly complete formula describing the transit frequency is:

$$f_T = \frac{1}{2\pi(\tau_F + (R_E + R_C)C_{BC} + \frac{k_B T}{qI_C}(C_{BE} + C_{BC}))} \tag{I.7}$$

Where τ_F is the electron transit time through the device; R_E is the emitter resistance; R_C the collector resistance; C_{BC} the base-collector capacitance; C_{BE} the base-emitter capacitance; I_C the collector current; k_B the Boltzmann constant; T the temperature; q the electron charge.

Equation (I.7) displays a dependence from the collector current I_C which minimizes the contribution of some capacitances at high injection. f_T drops when collector current increases too much because of some limiting phenomena such as quasi-saturation or the Kirk effect.

A common Figure Of Merit (FOM) is $f_{T,max}$ defined as the maximum value of f_T attainable for a device. In the following, f_T will be often used to mean $f_{T,max}$ for the sake of simplicity. In case of possible confusion, the correct notation will be used.

2.6 Maximum oscillation frequency

Considering power behavior of the transistor, it is also possible to define the maximum oscillation frequency f_{MAX} as the frequency at which the power (Mason) gain U drops to 1.

Analogously to what seen for the transit frequency, f_{MAX} is extrapolated from power gain measurements at lower frequencies of the -20 dB/dec power gain slope. Once the extrapolation frequency f_{extr} set, the transit frequency can be obtained as:

$$f_{MAX} = \sqrt{U} f_{extr} \tag{I.8}$$

where U is the Mason gain at extraction frequency f_{extr}.

Maximum oscillation frequencies reported in this work are normally referring to an extrapolation frequency f_{extr} of 20 GHz. Tolerance on measured values can go up to 5 % on a well-performed setup.

A simplified formula for defining such frequency as a function of device parameters is:

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{I.9}$$

Where f_T is the transit frequency; R_B the base resistance; C_{BC} the base-collector capacitance.

A common FOM is $f_{MAX,max}$ defined as the maximum value of f_{MAX} attainable for a device. In the following, f_{MAX} will be often used to mean $f_{MAX,max}$ for the sake of simplicity. In case of possible confusion, the correct notation will be used.

2.7 Capacitances and resistances

As seen in Equation (I.7) and Equation (I.9), parasitics play an important role in limiting the transistor's operation at high frequency. An important part of this work is about minimizing the parasitics to get the maximum out of the device.

Three main resistances can be defined:

R_C Collector resistance. It is often reported in Ω/sq.

R_B Base resistance. Normally splitted in two components: extrinsic base sheet resistance R_{sBX} and pinched intrinsic base sheet resistance R_{sPBI}, reported in Ω/sq.

R_E Emitter resistance. Normally reported in Ω or $\Omega/\mu m^2$

Base and collector resistances are obtained by model extrapolation based on measurements performed on various device geometries, while emitter resistance is obtained by the transconductance method [37]. See Appendix 4 for more details on the extraction techniques of R_C and R_B.

Among the capacitances we can list:

C_{BC} Base-collector capacitance. Normally reported in fF.

C_{BE} Base-emitter capacitance. Normally reported in fF.

Capacitances are extracted from S parameters measured on standard $0.2 \times 5\mu m$ transistors. Reported capacitances are always referring to 0 V junction bias.

2.8 Power behavior at high frequency

Load-pull measurements can be used to define the power behavior of the device at high frequency.

Chosen an extraction frequency f_{extr}, a cartography on the Smith chart allows to find the optimal load Z.

The power added efficiency PAE is used to express the power effectiveness of the transistor. In practice, it relates the RF increase of signal power with the power consumed for device operation. It is defined as:

$$PAE = \frac{P_{OUT}^{RF} - P_{ABS}^{RF}}{P_{TOTAL}^{DC}} \tag{I.10}$$

where P_{OUT}^{RF} is the output RF power, P_{ABS}^{RF} is the absorbed RF power and P_{TOTAL}^{DC} is the total DC absorbed power required for biasing the device.
PAE is normally expressed in percentage.

The output power at maximum efficiency $P_{OUT}@PAE_{MAX}$ measures the output power available at maximum efficiency. $P_{OUT} - 1dB$ is the output power at 1dB compression, setting a soft limit for maximum output power.

The power gain G_p measured in dB is expressed as:

$$G_p = 10 \cdot log(\frac{P_{OUT}}{P_{ABS}}) \tag{I.11}$$

3 State of the art

Many needs require many solutions and each producer of BiCMOS technologies offers its combination both of active and passive components. It is impossible to define which platform is the best since it really depends on customer needs. Specific device performance can be compared from a technical point of view. This section details how each actor is trying to offer the most performing HBT solution for RF applications.

Since HBTs are used in BiCMOS circuits for their RF characteristics, f_T and f_{MAX} are quite good parameters for evaluating their performance. Figure I.7 depicts the state of the art obtained from scientific publications of the principal players in the recent years.

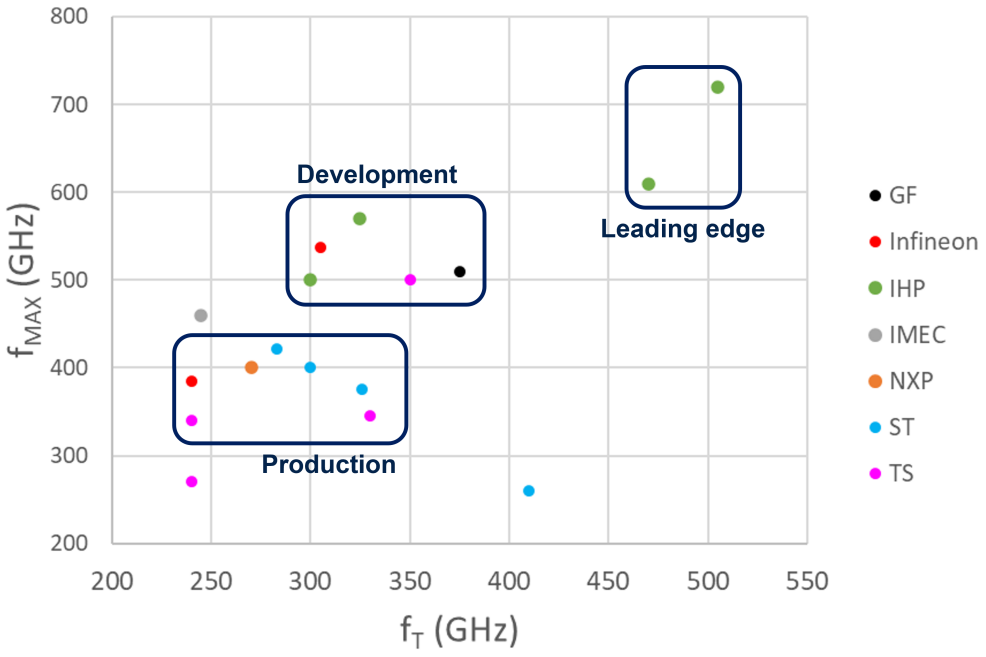

Figure I.7 | Published values of f_T/f_{MAX} achieved in the recent years by HBT producers.

Some distinction has to be made on the state of maturity of each result. "Production" solutions are those related to a complete BiCMOS platform and currently sold on the market. This means that a whole set of other

active and passive devices are also available for integration on the same die. Transistors appertaining to the "industrial development" category are not necessarily within all the constraints needed for series production but are being developed to be part of it. The present work is meant to establish a new state of the art in this category. "Leading edge" devices are the finest in terms of performance thanks to advanced device design and show the actual known limits for HBT performance.

In the following, the most recent solutions known from each HBT producer will be presented.

3.1 Global Foundries

In 2021, Global Foundries presented a BiCMOS platform based on a 45 nm PD-SOI CMOS node[46]. The HBT realized in this framework could reach an f_T of 375 GHz and an f_{MAX} of 510 GHz.

Not many informations are given on the HBT architecture. The collector is realized by opening the SOI BOX to expose the underlying silicon and followed by a typical sequence for realizing a buried doped layer. The rest of the device is obtained with a typical sequence of steps including intrinsic and extrinsic base epitaxy, emitter deposition and patterning with spacer formation. Lateral and vertical scaling allow to suppress parasitic components and optimize the doping profile.

Figure I.8 depicts a schematic cross-section of both HBTs and MOSFETs.

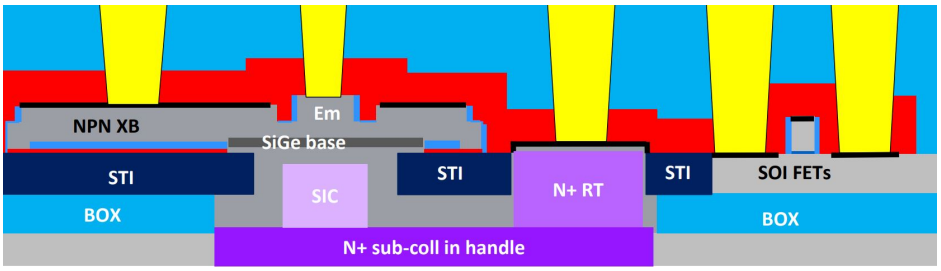

Figure I.8 | Schematic cross section of the BiCMOS platform presented by Pekarik et al. [46].

3.2 Infineon

The german Integrated Device Manufacturer (IDM) Infineon presented in 2018 its most updated version of the Elevated Base Link - Selective Epitaxial

growth (EBL-SEG) architecture exhibiting f_T/f_{MAX} = 305/537 GHz on a 130 nm CMOS platform[40].

This architecture has been conceived by IHP[21] and then transferred to Infineon's production line[39] for industrialization. Figure I.9 shows a TEM cross-section of the device. EBL-SEG devices rely on a dedicated lateral extrinsic base epitaxy to address the reduction of base resistance R_B and maximize f_{MAX}. In practice, the whole intrinsic collector-base-emitter stack is realized before a selective epitaxy is used to laterally contact the base. This sequence allows to heavily dope the extrinsic base without fearing excessive diffusion towards the intrinsic device.

An integration on a smaller 90 nm CMOS platform has been evaluated and should shortly take the place of the current 130 nm one.

Figure I.9 | TEM cross section of the Elevated Extrinsic Base - Selective Epitaxial growth (EBL-SEG) HBT presented by Manger et al. [40].

3.3 IHP

The Elevated Extrinsic Base - Non Selective Epitaxial Growth (EEB - NSEG) architecture has been firstly demonstrated by IHP in 2010[53] for the integration on a 130 nm CMOS platform. After some improvements[51], an updated version of the device achieved in 2019 a record performance of f_T/f_{MAX} = 470/610 GHz[52]. This device currently exhibits the maximum reported HBT frequencies on a BiCMOS platform.

A TEM cross-section of the HBT is shown in Figure I.10. This device is based on a non-selective epitaxy covering the whole surface and realizing the intrinsic base the seed layer for the extrinsic base at the same time.

An additional selective epitaxy is used to increase the doping level in the extrinsic base in order to address the base resistance R_B.

The same research institute presented in 2016 an improved version of this architecture conceived without the constraints of being co-integrated with CMOS devices[31]. The result is an astounding f_T/f_{MAX} of 505 Ghz and 720 GHz respectively, setting a new peak in HBT performance. Even though this solution is not currently suitable for BiCMOS integration, it raises the known limits for HBTs.

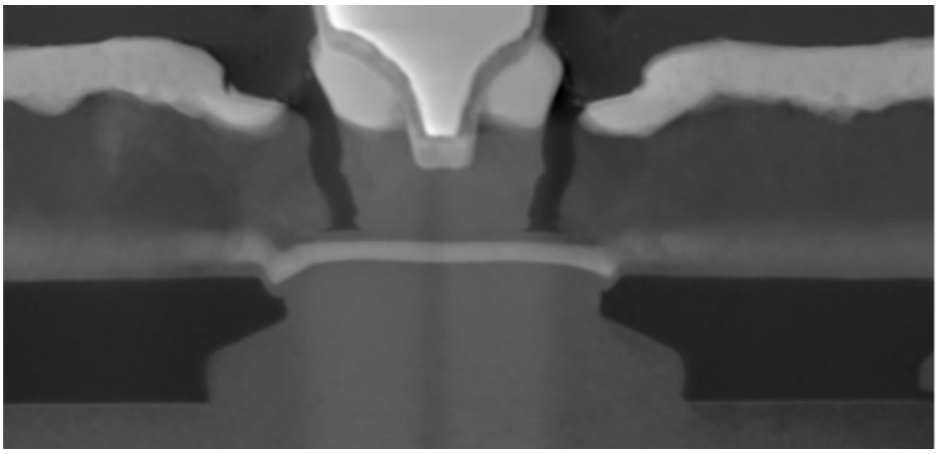

Figure I.10 | TEM cross section of the Elevated Extrinsic Base - Non Selective Epitaxial Growth (EEB - NSEG) HBT presented by Rücker et al. [52]

3.4 NXP

NXP makes use of the Double Polysilicon Self-Aligned-Selective Epitaxial Growth (DPSA-SEG) architecture for integrating its transistors on a 90 nm CMOS platform. The results presented in 2016 showed an integration achieving f_T and f_{MAX} of 270 GHz and 400 GHz respectively [61].

In order to have a high control over the vertical doping profile, this integration minimizes the thermal budget applied to the bipolar transistor by producing it at the end of the production flow, i.e. after the MOSFETS. The collector is doped by the means of a Sub-Isolation Buried Layer (SIBL) to reduce production cost by avoiding the costly epitaxy normally used in DPSA-SEG architectures. Figure I.11 highlights how the device has undergone an aggressive vertical scaling to bring the base contacts closer to the intrinsic base and minimize the R_B resistance.

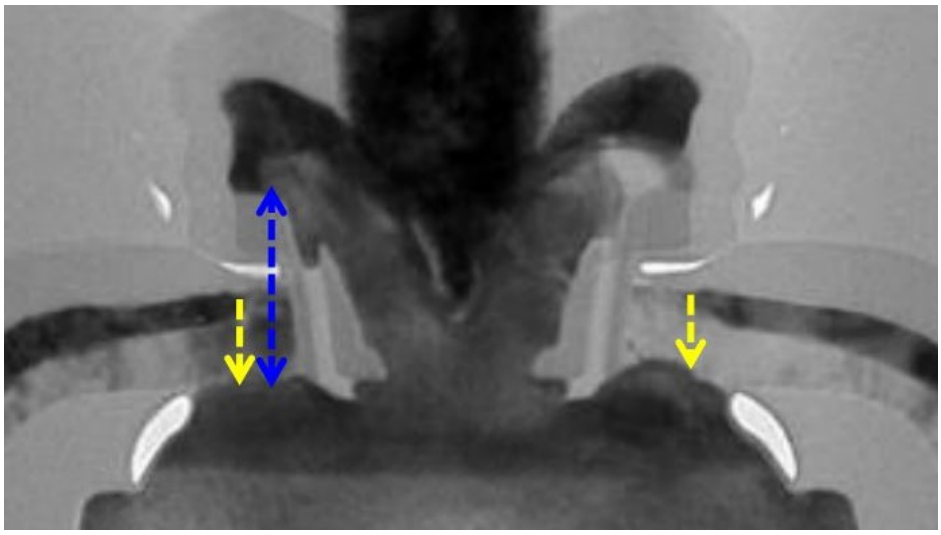

Figure I.11 | TEM cross section of the Double Polysilicon Self-Aligned-Selective Epitaxial Growth (DPSA-SEG) presented by Trivedi et al. [61].

3.5 STMicroelectronics

STMicroelectronics implements its own version of Double Polysilicon Self-Aligned-Selective Epitaxial Growth (DPSA-SEG) transistor. Firstly demonstrated for a 130 nm node on a 200 mm production line with f_T/f_{MAX} = 240/270 GHz by Avenier et al. [3], the architecture has been successively transferred on a 55 nm CMOS node, achieving f_T/f_{MAX} = 320/370 GHz in 2014[7].

In the years, many studies have worked on improving the performances obtained with this architecture. chevalier2009conventional worked on the maximization of f_{MAX}, attaining values above 400 GHz. The optimization of thermal budget has shown f_T values up to 340 GHz [26]. Following studies carried out by Gauthier et al. [22] could further improve f_T up to 450 GHz, at detriment of f_{MAX}.

Compared to NXP's solution, this device uses a standard buried layer for the collector. Three f_T/BV_{CEo} tradeoffs are offered on this platform to ensure maximum flexibility for circuit design.

More details on this integration are given in Section 4.1

3.6 Tower Semiconductor

Tower Semiconductor presented the Selective Emitter - Non Selective Epitaxial Growth (SE-NSEG) architecture in 2021 for a 180 nm CMOS platform[47]. Such device is capable of reaching values of f_T and f_{MAX} of 350 GHz and 500 GHz respectively. A TEM cross-section of the HBT is shown in Figure I.12.

This architecture has been used for a long time by Tower Semiconductor[49] because of its simplicity compared to competitor's solutions. The sacrifical emitter allows good alignment of the intrinsic components of the device without needing a complicated stack. The enhanced architecture presented by Phillips et al. [47] benefits from a reduced thermal budget to achieve high control over dopant diffusion in the base. Authors reported that an important simulation study has been performed to obtain a fine doping profile capable of delivering such important performance with a simple device design and - probably - reduced production cost.

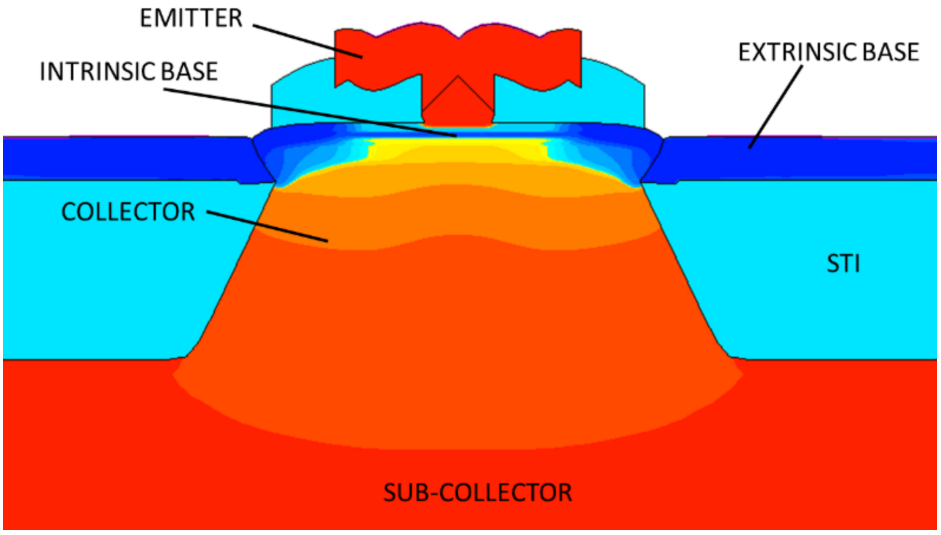

Figure I.12 | Schematic cross section of the Selective Emitter - Non Selective Epitaxial Growth (SE-NSEG) HBT architecture presented by Phillips et al. [47]

4 From DPSA-SEG to EXBIC architecture: starting point

The state of the art presented in Section 3 proves that the race for improving HBT performance is not over and each actor among the BiCMOS producers is striving to offer the best solution.

In the last years STMicroelectronics has started developing a proprietary architecture called Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC)[63] to overcome the intrinsic limitations of the Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) design used in the BiCMOS055 platform. A deeper analysis on the two architectures will explain the reasons of this study.

4.1 Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) architecture

The Self Aligned structure has been first demonstrated by Ning et al. [43] for a standard BJT with interesting possibilities to reduce the number of masks and increase precision in processes. The implementation of a complete DPSA-SEG structure for HBT has been reported by Sato et al. [55] for an HBT architecture and has been demonstrated for a 300 mm BiCMOS platform in Chevalier et al. [7], constituting the BiCMOS055 (B55) technology (Figure I.14). f_T/f_{MAX} amount to 320/370 GHz for this specific integration.

The name of the architecture explains its main features.

Structure self-alignment reduces the number of masks and cancels alignment tolerance, lowering cost and enforcing process precision. As a side effect, design rules can result in more efficient circuits, which increases the overall performance.

Double polysilicon means that emitter and extrinsic base are grown by Chemical Vapour Deposition (CVD), adding multiple degrees of freedom both in terms of device topology and doping strategies. Moreover, polysilicon is capable of recrystallizing when baked in contact with monocrystalline silicon, reducing parasitic resistances. When dealing with the intrinsic-extrinsic base contact, the link is obtained simultaneously during intrinsic base growth and does not require specific processes.

The selective epitaxial growth refers to the capability of performing a deposition on a specific material, particularly important for the base epitaxy:

spurious growth on undesired points is eliminated, removing the need for additional patterning steps.

Referring to Figure I.13, the process flow of a DPSA-SEG with a buried layer collector integrated in STMicroelectronics' B55 platform (Figure I.14 left) can be sketched as follows:

1. A buried layer is doped by ion implantation in the substrate before growing an intrinsic silicon layer by epitaxy.

2. DTIs are created to reduce collector-substrate capacitance C_{CS} and isolate devices while STIs are used to reduce base-collector capacitance C_{BC}.

3. An additional implantation is performed to obtain a Selectively Implanted Collector (SIC). Sinker implatations allow to reduce the resistance between collector contact and buried layer.

4. Different layers are deposited forming a stack; among them there is the extrinsic base polysilicon.

5. The stack is patterned, forming the emitter window. Spacers are formed to protect the cavity walls. An additional isotropic etching step generates an undercut below the polysilicon layer.

6. In the same window, the intrinsic base is grown by selective epitaxy. Contact with the extrinsic base is achieved during growth. Epitaxy allows a graded SiGe profile, with Carbon and Boron as dopants.

7. Spacers are formed inside the cavity and emitter is deposited by CVD.

8. Final patterning of the device.

Presented by Geynet [27] for a 200 mm platform and studied from Canderle [6] for a 300 mm production line, the possibility of creating a low-cost version of the DPSA-SEG structure thanks to a fully implanted collector has been presented by Gauthier et al. [22] (Figure I.14 right) with record performances for a BiCMOS platform.

The reduced thermal budget ensures limited dopant diffusion. Arsenic ion implantation has been replaced by carbon plus phosphourus co-implantation to suppress defects[22].

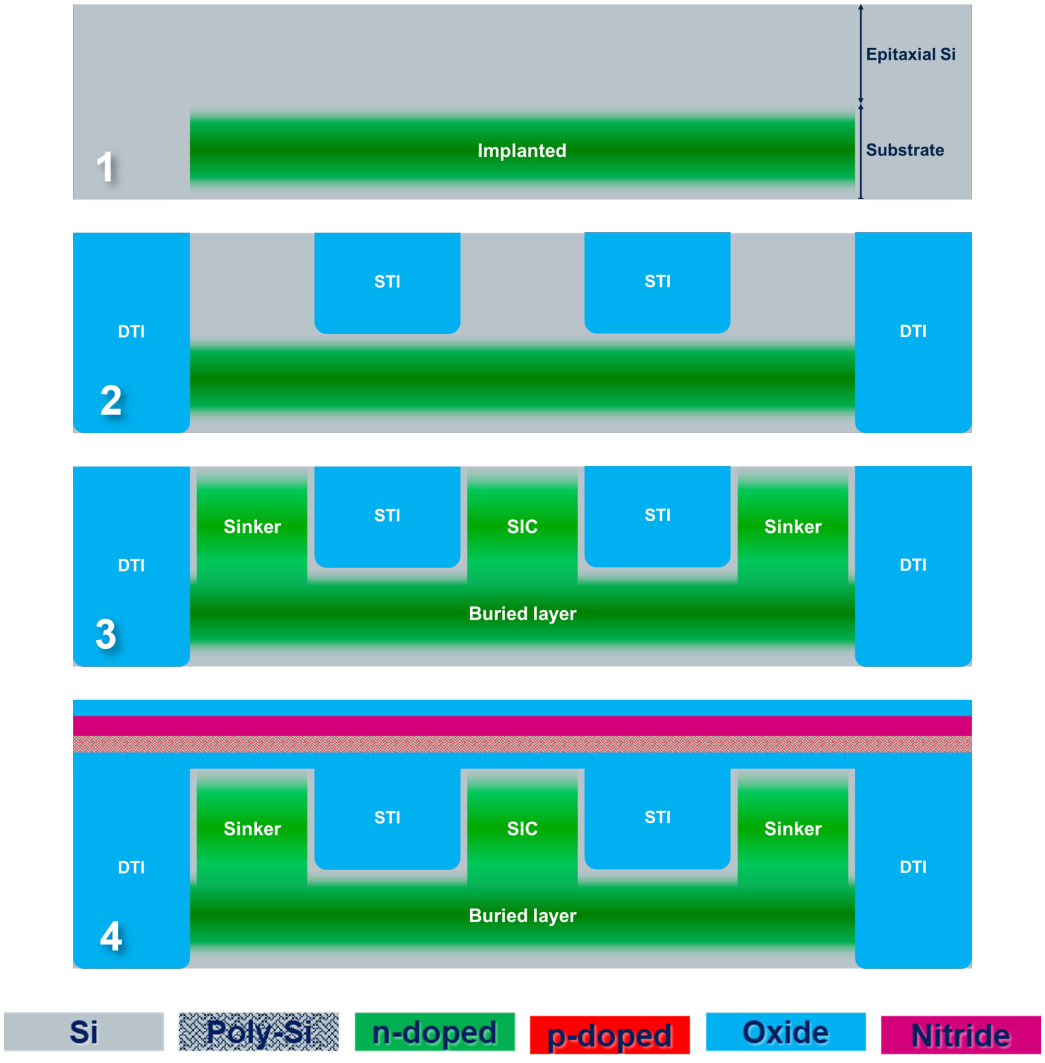

Figure I.13 | Schematic process flow of a B55 DPSA-SEG. Part 1
Picture not to scale.

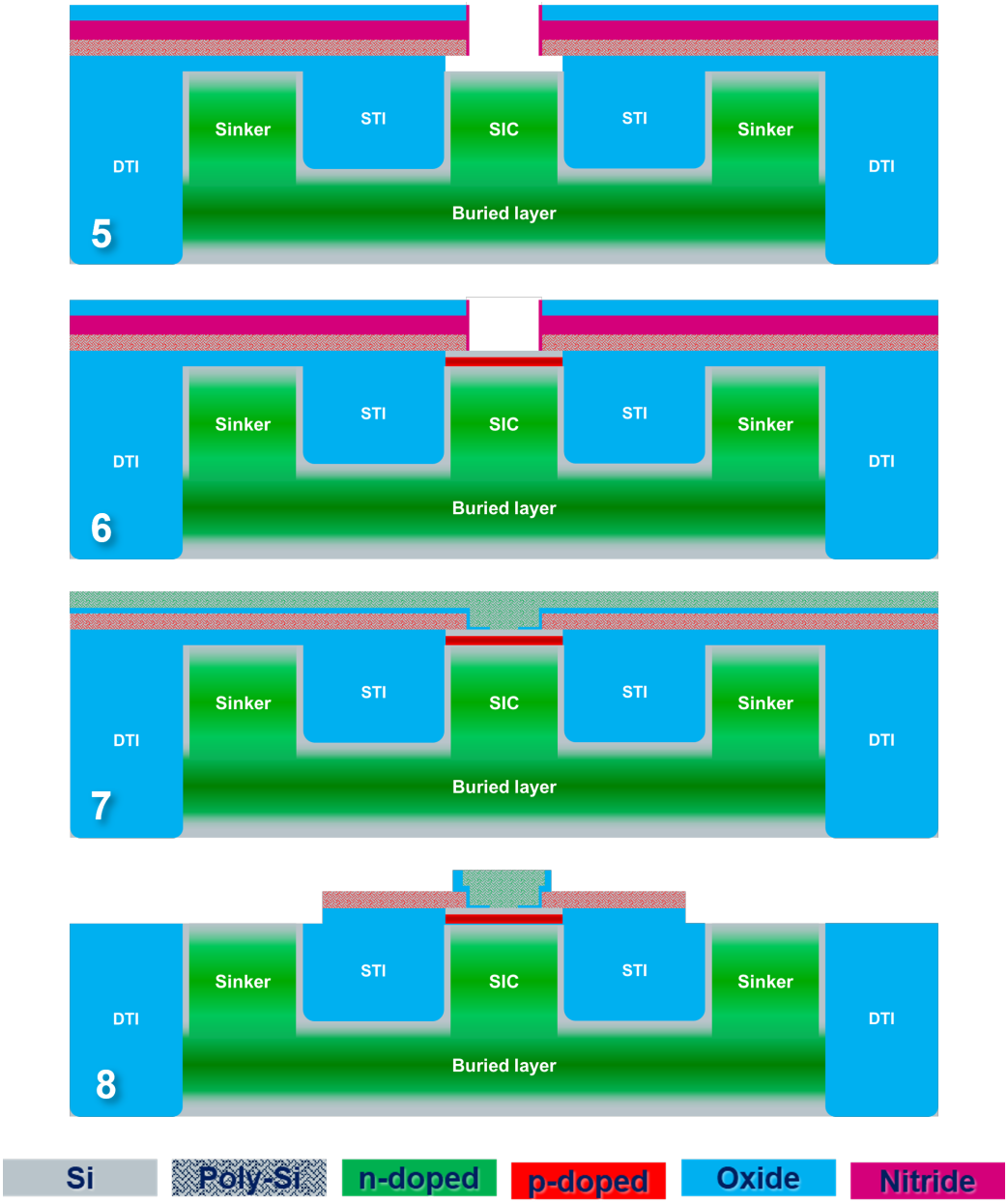

Figure I.13 | Schematic process flow of a B55 DPSA-SEG. Part 2
Picture not to scale.

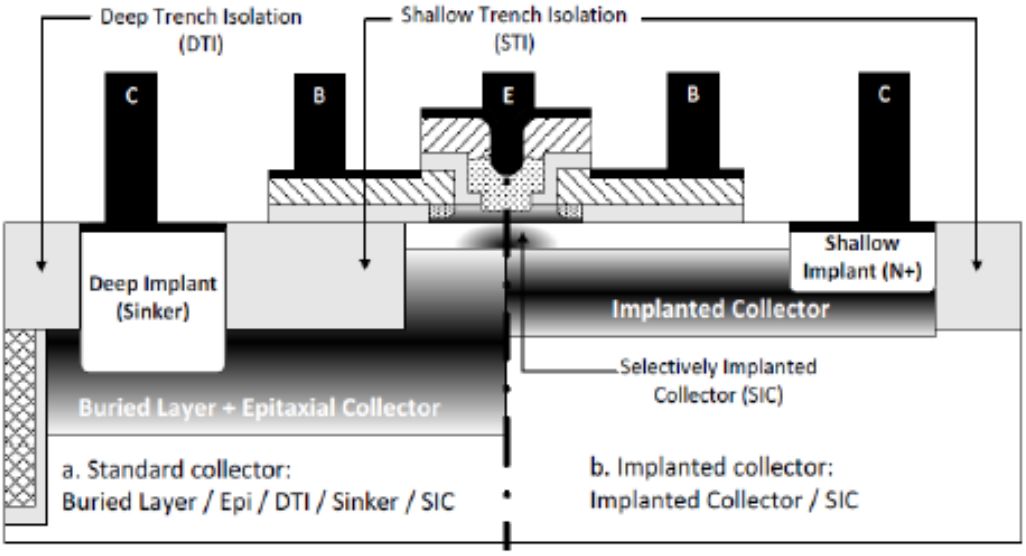

Figure I.14 | Comparison between DPSA-SEG HBTs featuring buried layer (left) or fully implanted (right) collector. Pictures from [8].

The introduction of a fully-implanted collector avoids the expensive buried layer, eliminates the need for DTIs and reduces overall device thickness. The redesigned collector doping targets collector resistance R_C to achieve 450 GHz f_T. On the other hand, the elimination of STIs causes increased base-collector capacitance C_{BC} at detriment of f_{MAX}. This final improvement of the DPSA-SEG architecture well displays that its limits have been attained. It is difficult to further increase f_T without degrading f_{MAX} and a new approach is needed. Equation (I.9) clearly shows that f_T increases f_{MAX}, but base resistance R_B and base-collector capacitance C_{BC} contribute to the equation as well and they can not be neglected.

Even though different solutions can be found for mitigating base-collector capacitance C_{BC} in absence of STIs, the big limitation of the DPSA-SEG architecture is represented by the extrinsic component of the base resistance. Since the link between extrinsic and intrinsic base is formed when the latter is grown by epitaxy, the only way to reduce extrinsic base resistance R_{Bx} is to tune the dopants in the extrinsic base. However, limitations in the production tools used for the extrinsic base deposition heavily hinder the capability of further improving this feature and represent a major showstopper for this architecture.

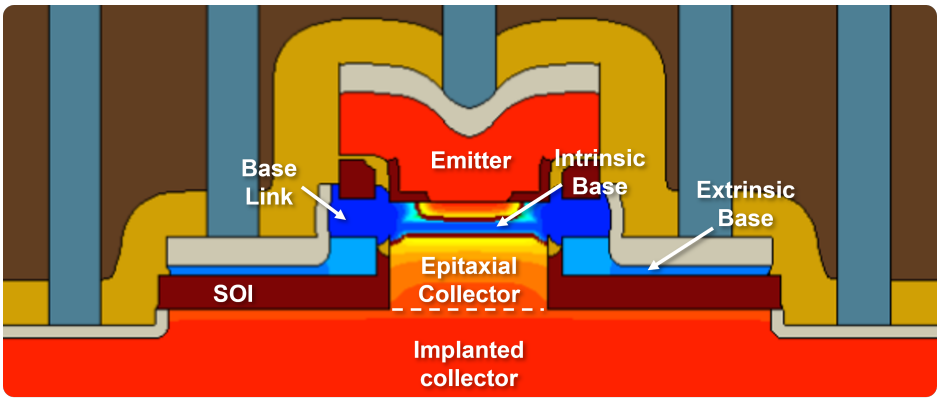

Figure I.15 | EXBIC structure from Technology Computer-Aided Design (TCAD) simulation. Original integration issued from Vu [63].

4.2 Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) architecture

Firstly presented by Vu [63], the EXBIC architecture (Figure I.15) results from the need to overcome the main DPSA-SEG limitations. Trying to improve f_T and f_{MAX} without compromise, the main focus is on the need to reduce the interdependence between base and collector parasitics. Thanks to the ability to reduce extrinsic base resistance without a consistent degradation of base-collector capacitance and the higher versatility in doping profile design thanks to in-situ-doped epitaxies, TCAD simulations forecasted f_T/f_{MAX} values of 470/870 GHz with a BV_{CEo} of 1.65 V. This architecture is also meant to be integrated on an SOI substrate, exploiting the buried oxide layer for isolating extrinsic base and collector.

Observing the schematic in Figure I.15, one may notice that the collector structure has been redesigned with respect to DPSA-SEG. A selective in-situ-doped epitaxy substitutes the purpose of a SIC implantation and exploits the better control over dopants distribution to enhance junction design. The possibility to dope in-situ allows to tune base-collector junction properties independently from the extrinsic collector thanks to a 2-step sharp dopant profile without defects creation. This solution is meant to relax the compromise between f_T and BV_{CEo} while allowing to minimize collector resistance. This solution allows to use a fully-implanted collector design, eliminating the need for buried layer epitaxy and STI isolation structures for addressing the base-collector capacitance. This approach also allows to easily integrate

devices with different $f_T \times BV_{CEo}$ compromises on the same die thanks to versatility and relatively low cost of ion implantation. Thanks to the shallower collector, DTI is not necessary to isolate devices one from another and a much simpler and cheaper STI can be used at its place. DTI can still be integrated for applications where the collector-substrate capacitance must be minimized. The elimination of the buried layer collector drastically reduces fabrication time and cost. The intrinsic-extrinsic base contact has also changed and uses a selective epitaxy to form a lateral link at the end of the process flow. This feature is meant to give more control over link formation and to reduce interfaces contributing to base resistance R_B. Moreover, the 2 epitaxies used to form link and contact zone are meant to offer maximum doping versatility. The advantages of EXBIC architecture, compared to DPSA-SEG's flaws, make it the chosen architecture for the future STMicroelectronics' BiCMOS055X (B55X) technology.

Once the architecture designed, process trials have been performed to asses its feasibility. The preliminary studies presented by Gauthier [23] led to a redesign of the initial architecture. This specific integration will be hereafter referred to as preliminary EXBIC architecture. Matters relating to fabrication processes and electric performance improvement have been considered.

Referring to Figure I.16, the Front End Of Line (FEOL) process flow of a BiCMOS die integrating both CMOS and preliminary EXBIC architecture HBT can be sketched as follows:

1. Isolation structures are realized. SSTI separates extrinsic base and collector, while STI is used to separate devices one from another. DTI can be optionally produced for lower collector-substrate capacitance.
2. CMOS wells are obtained by implantation doping.
3. Gate oxides and polysilicon are deposited.
4. The zone dedicated to HBT is opened through polysilicon.
5. Collector is doped by ion implantation.
6. The stack is deposited and the emitter window is patterned.
7. Collector and base are grown by selective epitaxy in the emitter window. In-situ doping allows to dope the grown layers. Air gaps are formed in the polysilicon stack layer.

8. Internal emitter spacers are realized.

9. Emitter is deposited with an in-situ-doped non-selective process. Patterning and oxide encapsulation follows.

10. In the remaining stack, an opening is obtained by removing the sacrificial nitride layer in the stack. A selective epitaxy leads to base link formation.

11. The oxide protecting the polysilicon seed layer is removed. The contact zone of the extrinsic base is grown by selective epitaxy and successively patterned.

12. The remaining processes related to MOSFET devices are performed.

Figure I.17 depicts the preliminary EXBIC architecture device issued from this process flow and used as a starting point for this work.

Comparing Figure I.15 and Figure I.17, we can immediately notice the appearance of Super Shallow Trench Isolation (SSTI) between base and collector where the buried oxide was present before. This means that the new architecture is no longer designed for SOI substrates, limiting the co-integration with advanced CMOS technologies but making the integration simpler. Still requiring an isolation structure for reducing the extrinsic component of base-collector capacitance in a fully-implanted approach, SSTIs are introduced. Notice that, in case an adaptation to SOI substrates was needed, the new integration would still be relatively easy to adjust.

Spacer walls surrounding the epitaxial collector disappeared. Mastery of selective epitaxy processes allows to create air gaps in the polysilicon seed layer present in the stack and separate the intrinsic collector from the extrinsic base. Oxide spacers can be avoided in this way without needing additional processing steps.

Not visible in the picture, the collector epitaxy is not doped in-situ and simple ion implantations in the substrate are used to dope the collector. This solution allows to avoid some issues arisen during the development of the epitaxy process on industrial tools. SIC can still be used at its place as done on the DPSA-SEG architecture but with the advantageous properties of carbon plus phosphorus co-implantations. Specific tuning of the base-collector junction is required. More details on the collector will be given in Chapter II Section 1.

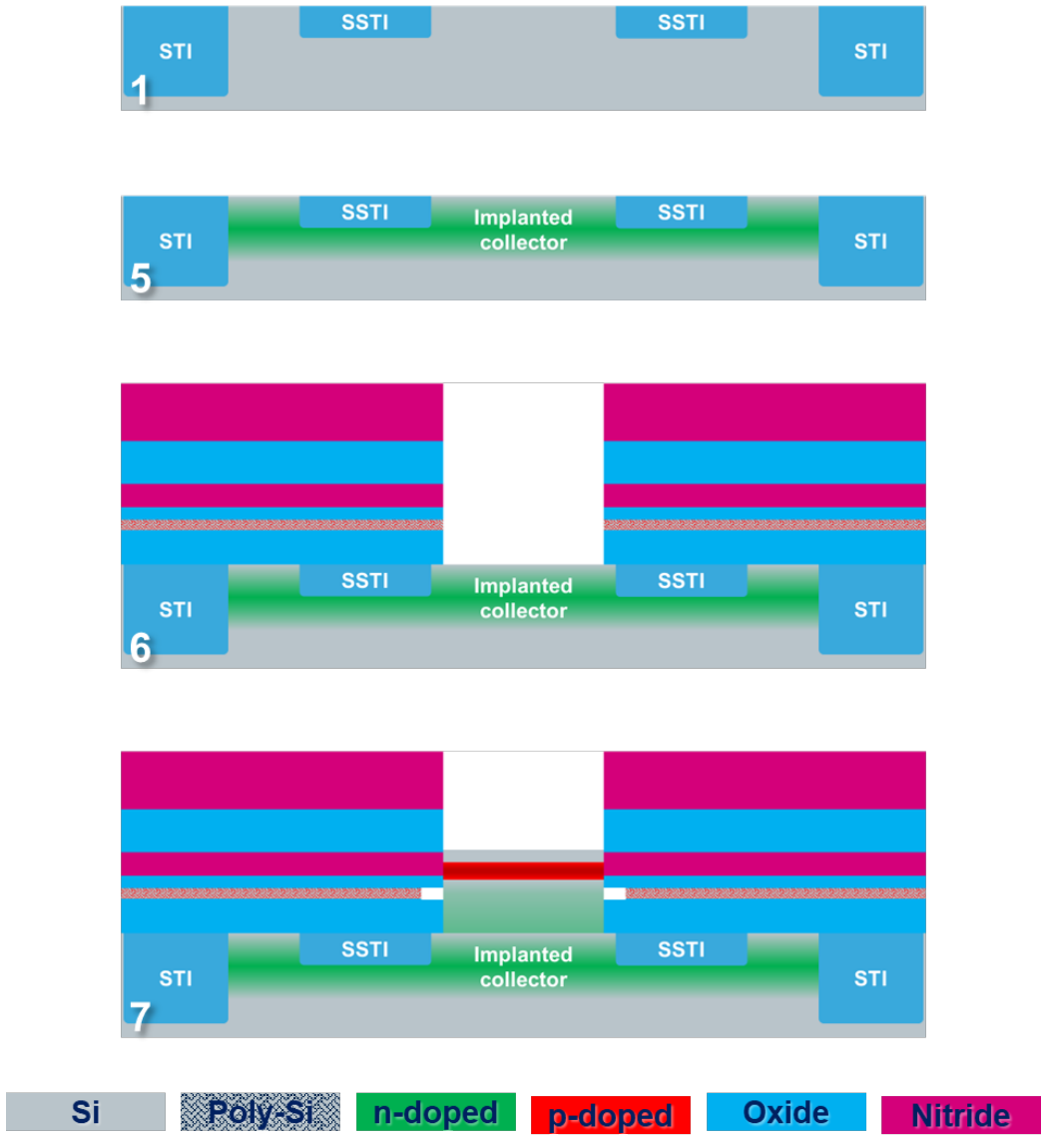

Figure I.16 | Schematic process flow of a Preliminary EXBIC. Part 1 Picture not to scale.

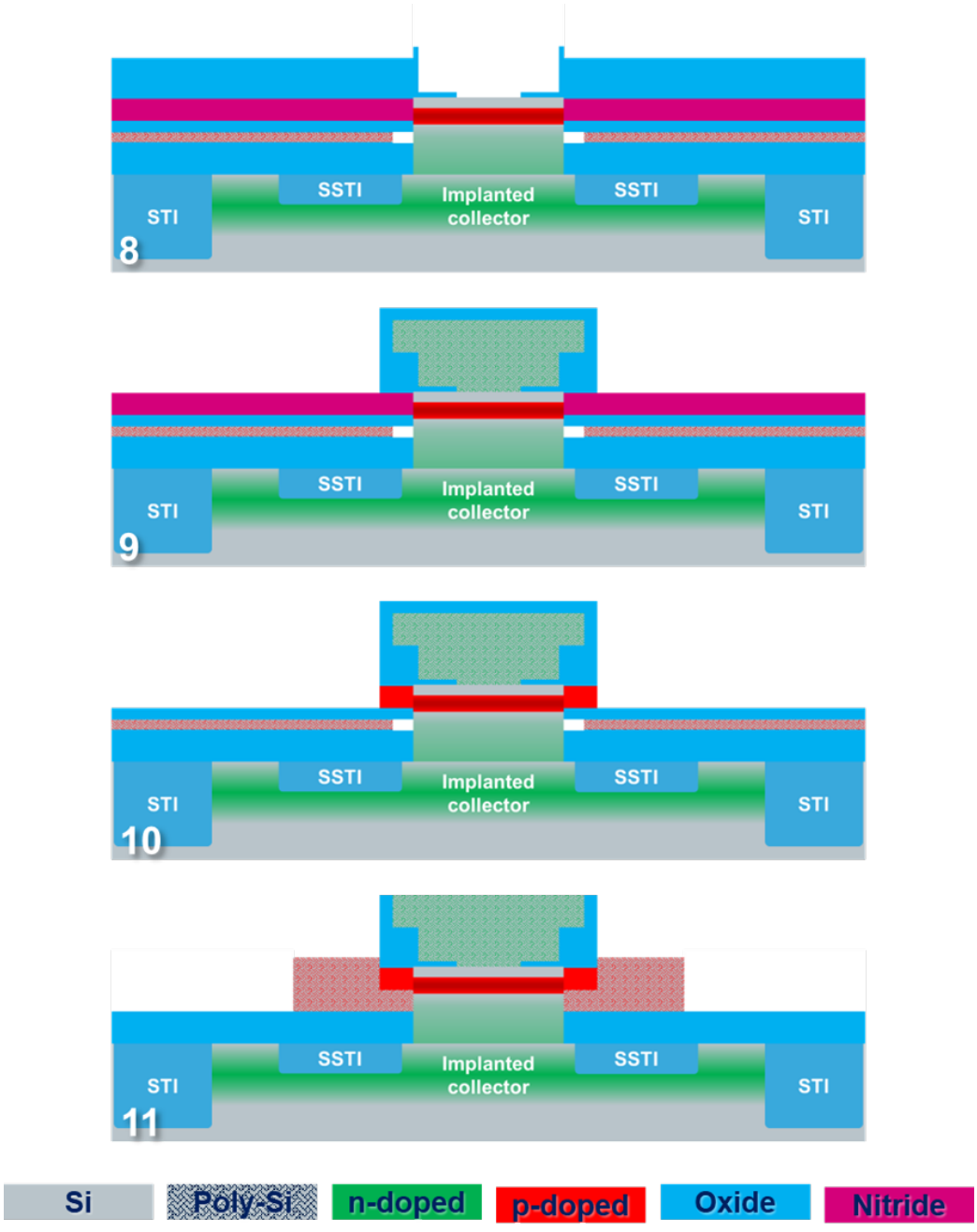

Figure I.16 | Schematic process flow of a Preliminary EXBIC. Part 2
Picture not to scale.

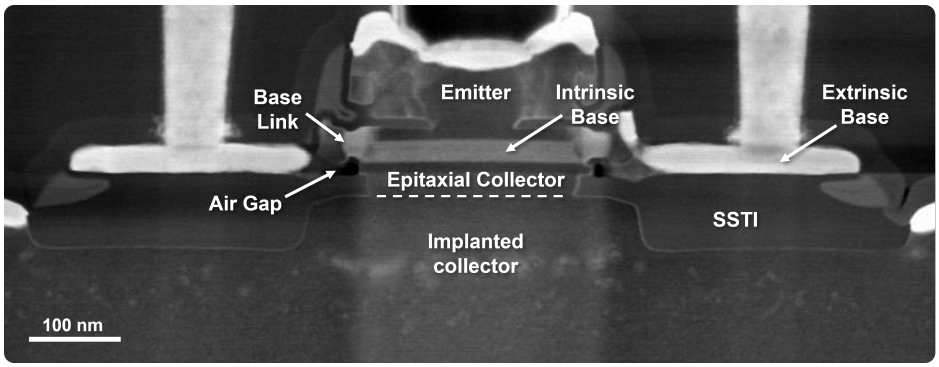

Figure I.17 | TEM cross-section of an HBT realized with the preliminary EXBIC architecture.

The alignment of intrinsic and extrinsic base has been modified for better link formation and base resistance R_B suppression. More details on this aspect will be given in Chapter II Section 2.

Finally notice that the updated version of the EXBIC architecture is no longer meant to exploit the BOX of an SOI subtrate. Focusing on achieving higher performance, a bulk substrate has been considered to allow more relaxed constraints for collector integration.

To better understand the innovations introduced with the new architecture, Figure I.18 compares TEM cross-sections of B55 DPSA-SEG and POR EXBIC transistors.

The difference between the two devices is immediately visible thanks to the base-collector isolation structures (STI vs SSTI). The buried-layer collector integration of the DPSA-SEG represents in fact a big part of the cost of this device, particularly due to the need of a thick epitaxy for the formation of a deep (> 300 nm) buried layer. The EXBIC transistor relies on the other hand on a way simpler fully-implanted collector, reducing both production cost and complexity. Collector defects are clearly visible in the EXBIC HBT while the DPSA-SEG one benefits from its mature development. Main purpose of the new architecture, the extrinsic base has been totally redesigned. While the extrinsic base was fabricated before the intrinsic one, requiring a vertical contact, a lateral link is used in the new integration. The main reason for this redesign is the need for more flexibility in the choice of process parameters in the scope of minimizing the extrinsic base resistance. The emitter spacers are also different, requiring to adapt to the specificities of each inte-

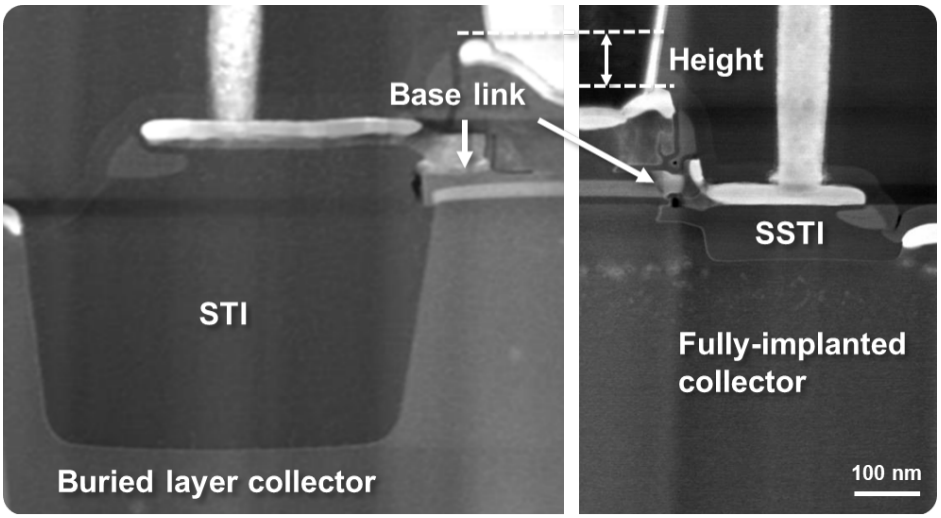

Figure I.18 | Comparison between TEM cross-sections of B55 DPSA-SEG and POR EXBIC transistors.

gration. Moreover, while the DPSA-SEG relies on a polysilicon-oxide stack, the EXBIC uses a nitride-oxide piling for spacers formation.

The new transistor is also drastically smaller, bringing collector and base contacts close to the intrinsic part of the device. This is advantageous for many aspects. Considering similar resistivities, a smaller device will imply smaller parasitic resistances. Vertical scaling is also important for the co-integration with MOSFETs on the same wafer, particularly for contacts formation.

The capabilities of an EXBIC HBT to overcome its DPSA-SEG counterpart have not been proven on silicon yet. Projections on its performance at maturity target an f_T/f_{MAX} couple of 400/600 GHz with a profile capable of withstand 1.35 V of maximum BV_{CEo}. In the scope of BiCMOS055X technology, an f_T/f_{MAX} couple of 400/500 GHz with $BV_{CEo} = 1.35$ V will be considered adequate.

5 Objectives of this work

The main objective of this work is to produce a Heterojunction Bipolar transistor (HBT) with the Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) architecture, reaching state-of-the-art performance of $f_T/f_{MAX} =$ 400/600 GHz with $BV_{CEo} = 1.35$ V.

Constraints of an industrial production line such as cost and reliability must be considered. Further enhancements are investigated to define future evolutions of HBT technologies.

In the scope of industrial production, values of $f_T/f_{MAX} = 360/420$ GHz are considered enough to validate the technology before attaining desired performance. Table I.1 compares B55X targeted figures of merit with the values deemed sufficient for the validation of this technology.

Table I.1 | Comparison of target values defined for main figures of merit.

NPN CBEBC $0.2 \times 5\ \mu m^2$		B55X targets	Validation target
Frequencies	f_T	400	> 360
	f_{MAX}	500	> 420
Current gain	$V_{BE} = 0.7\ V$	2250	> 650
V_A	F (V)	100	> 50
	R (V)	1,4	$> 1,2$
BV	CBo (V)	4,5	$> 4,1$
	CEo (V)	1,44	$> 1,3$
R	E normalized ($\Omega/\mu m^2$)	1,5	$< 1,8$
	B_{TOT} (Ω)	18	< 26
	sBI ($k\Omega/sq$)	4	< 6
	Bx ($\Omega \cdot \mu m$)	40	< 70
	sBL (Ω/sq)	50	< 60
C	BC normalized (fF/μm^2)	7,6	$< 8,5$
	BC normalized (fF/μm^2)	20	< 23

The development process and the objectives of each step presented in this work are schematized in Figure I.19:

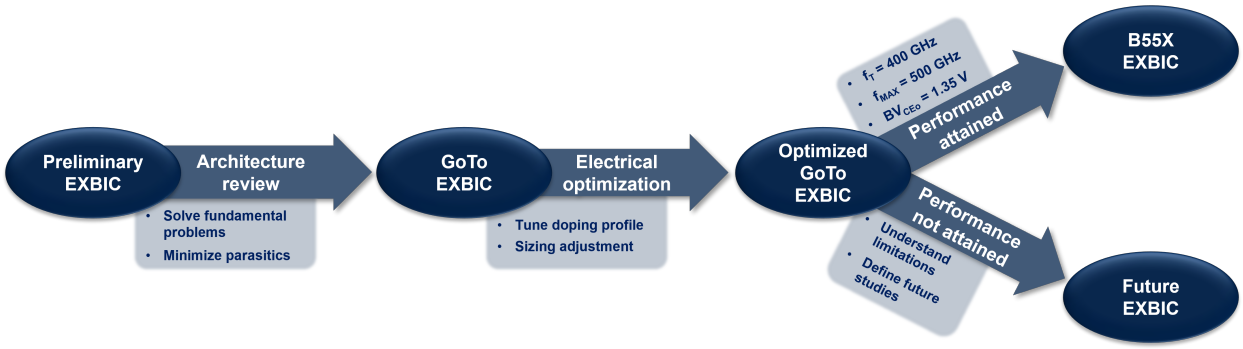

Figure I.19 | Development process and objectives of this work.

Chapter II is dedicated to the preliminary EXBIC architecture review, focused on improving weak points hindering performance and reliability. Where possible, the architecture is simplified to reduce production costs. A natural increase in performance is expected from the reduction of parasitics. The chapter is organized as follows:

Section 1 Investigates defect formation mechanisms induced by carbon plus phosphorus ion implantation and evaluates the contribution of SSTIs.

Reviews the SSTI integration as conceived in the preliminary EXBIC architecture to overcome some of its limitations.

Section 2 Details the problems linked to the extrinsic base integration and proposes an improved version.

Section 3 Investigates different alternatives in the cleaning process of the emitter-base junction.

Section 4 Sums up the innovations proposed in the chapter and defines the resulting Go To EXBIC architecture.

Section 5 Presents results of 94 GHz load-pull measurements in order to understand the high-frequancy power behavior of the EXBIC HBT architecture.

Chapter III details the electrical optimization process of the Go To EXBIC architecture to obtain best performances. Figures of merit are improved through doping profile optimization and sizing adjustment. The chapter is organized as follows:

Section 1 Investigates the reduction of collector resistance in presence of SSTI.

Treats base-collector junction tuning through carbon plus phosphorus ion implantation in the substrate.

Observes the impact of epitaxial collector thickness variability on device performance.

Section 2 Treats the optimization of the new extrinsic base integration by modifying its size and doping

Section 3 Investigates a modification in the boron doping profile more suited for the new device architecture.

Reviews a part of the germanium profile in the effort of improving its impact on transit time in the base.

Section 4 Is dedicated to tuning the emitter-base junction through resizing of the effective emitter window.

Section 6 Sums up all the results obtained in the optimization process of the Go To EXBIC architecture.

Chapter IV concludes by commenting the results presented in this work, establishing if they are sufficient for the needs of the future BiCMOS055X technology or if further studies are required for improving the EXBIC HBT architecture.

Chapter II

Architecture review

This chapter presents how the problems affecting the preliminary EXBIC architecture have been solved in order to reach a solid integration.

The process flow presented in Section 4.2 is analyzed in search of weaknesses to solve. The initial state of play and any further modification are evaluated through electrical Figure Of Merit (FOM).

Three modules are treated:

- *Collector*
- *Extrinsic base*
- *Emitter*

The results of all these modifications define the Go To EXBIC architecture.

The development of a new Heterojunction Bipolar transistor (HBT) architecture integration is not a straightforward operation. Leaps in transistor design are commonly due to the introduction of a new integration concept, most of times supported by advancements in fabrication processes. The Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) architecture makes wide use of advanced techniques such as selective epitaxies and co-implantations which are meant to optimize performance while reducing architecture complexity. Even though Technology Computer-Aided Design (TCAD) simulations can nowadays be very precise on the outcome of a particular device design, a good amount of work on manufacturing is still required to guarantee the expected performance.

Table II.1 compares some figures of merit measured on a DPSA-SEG HBT produced within the BiCMOS055 (B55) technology with those of one among the first functional EXBIC HBTs produced and the expected ones for the BiCMOS055X (B55X) technology. Notice that even if Vu et al. [64] set the target f_{MAX} to 600 GHz, the B55X technology aims to a value of 500 GHz.

Table II.1 | Some FOMs comparing a B55 DPSA-SEG, the EXBIC of Figure II.1 and the target values for the Go To EXBIC architecture integration. $0.2 \times 5\ \mu m^2$ reference devices.

	B55 DPSA-SEG	First EXBIC	B55X EXBIC target
η_{I_C}	1.03	1.17	<1.03
η_{I_B}	1.4	1.95	<1.3
BV_{CEo} (V)	1.5	1.81	1.35
f_T (GHz)	320	240	400
f_{MAX} (GHz)	370	170	500

Collector and base ideality factors η_{I_C} η_{I_B} way over the reference values indicate consistent current leakages. This situation is unsurprisingly bad seen the difficulties observed on the integration in Figure II.1.

Transit frequency f_T is below what seen on the B55 DPSA-SEG architecture and way below what expected for the EXBIC one. Elevated BV_{CEo} indicates that the junction is not pushed at its best, meaning that an optimization of the vertical doping profile is still possible. Imagining an identical $f_T \times BV_{CEo}$ product, the preliminary EXBIC architecture is already capable of reaching the 320 GHz f_T with a 1.35 V BV_{CEo}. Better design of the doping

profile could clearly go beyond this. Even considering the limited f_T, f_{MAX} is dramatically low, indicating particular issues both on base resistance R_B and base-collector capacitance C_{BC}.

Figure II.1 depicts the first functional EXBIC HBT featuring f_T/f_{MAX} = 240/150 GHz with 1.81 V BV_{CEo}, highlighting some flaws which will be detailed in the following part of this work. Thanks to specific studies on device fabrication previously performed, the transistor structure is good and no major defects are visible.

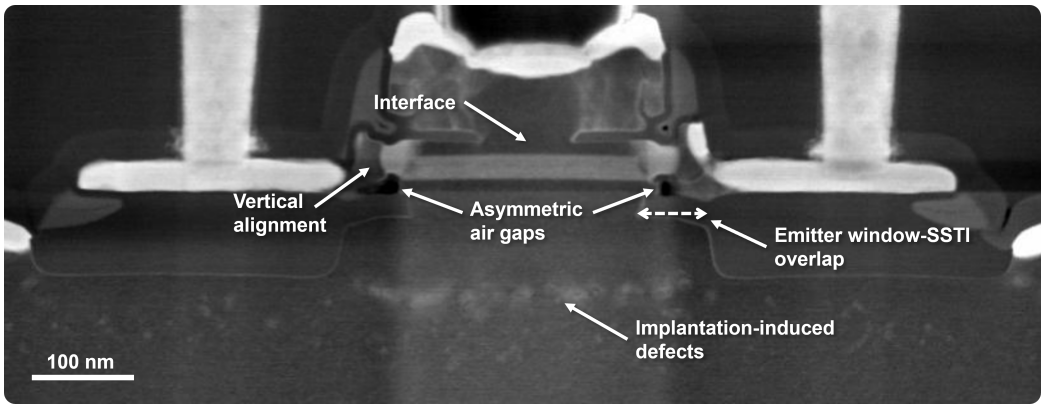

Figure II.1 | TEM cross-section of the first functional EXBIC HBT. Integration flaws are pointed out.

The collector is populated by many defects scattered in the ion-implanted zone and particularly dense between the two SSTI branches, suggesting an influence from these structures. The introduction of carbon plus phosphorus co-implantations has proven to be beneficial on DPSA-SEG devices with fully-implanted collector [22] but a specific extensive study is required for EXBIC HBTs. Regarding the newly-introduced isolation structures, overlap variability with the emitter window requires to be taken into account when designing the photolithographic masks. A zone without SSTI is therefore present between collector and base, limiting the benefits of C_{BC} reduction.

One of the main features of the EXBIC architecture is to reduce the base-collector capacitance C_{BC} by addressing its extrinsic component. The extrinsic base integration detailed in Section 4 is complex and very sensitive to process variations. Air gaps obtained in the seed polysilicon layer are not uniform in size and there is a huge variability from one device to the other. In some cases the gap is not even present and a spurious contact with the

base is obtained, leading to junction control issues. This also means that the base-collector capacitance C_{BC} reduction expected with this feature is not assured. The two epitaxies required for this integration of the extrinsic base allow high design versatility but need particular care. The device in Figure II.1, for example, has a bad connection between base link and contact zone of the extrinsic base, likely inducing high base resistance R_B. This integration is therefore deemed of being not robust enough. Reducing the number of steps and integration complexity would imply lower variability and production cost.

Last but not least, an interface is clearly visible between emitter and base. The cleaning process preceding the emitter epitaxy is possibly not well adapted to the integration and some undesired impurities are included in the crystalline lattice. The presence of undesired impurities within the emitter-base junction can lead to dopants segregation and additional parasitic effects. The emitter-base junction is essential for the transistor effect and requires careful attention to ensure good performance.

The EXBIC HBT presented in this section served as demonstrator of feasibility and functionality, allowing to set the initial development axes. Investigation has consequently been directed on three main parts of the device: emitter, extrinsic base and collector.

Figure II.2 sketches the architecture review process, detailing objectives for each module to improve. A steep increase in performance is expected thanks to the elimination of principal architecture weaknesses and the solution of process difficulties.

Chapter II is organized as follows:

Section 1 Treats how to eliminate defects induced by ion implantation and stress related to isolation structures.

Explores an alternative SSTI integration.

Section 2 Is dedicated to the design of a simpler and more reliable extrinsic base integration.

Section 3 Addresses the studies for eliminating undesired impurities included in the emitter-base junction.

Section 4 Sums up all the new features introduced during optimization and leading to the Go To EXBIC architecture. Integration advancements are

presented chronologically to show the actual impact of these innovations.

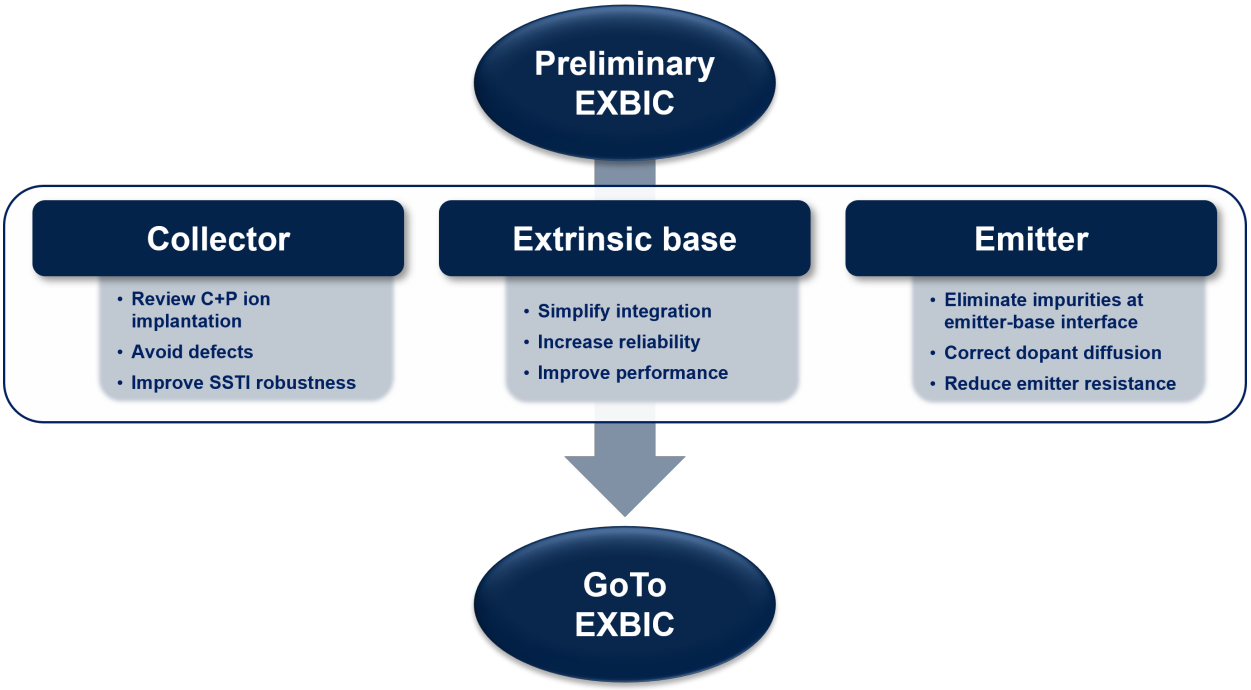

Figure II.2 | Modules impacted by the architecture review process and relative scopes.

1 Collector module

The collector module represents one of the main advancements for the EXBIC HBT architecture. Its principal needs are to remain as simple as possible while offering low parasitics and a sufficient degree of freedom to tune the base-collector junction.

The advantages observed on the Fully-Implanted-Collector DPSA-SEG integration [22] still required a way to manage the $R_C - C_{BC}$ compromise to deliver an adequate f_{MAX} while keeping f_T to good levels. Base-collector capacitance C_{BC} can be ideally separated in two components, i.e. junction (or intrinsic) capacitance and parasitic (or extrinsic) capacitance. While the first one depends on many factors such as junction sizing and doping profile, the second one is mainly related to device design. The concept of an isolation structure was already present in the standard DPSA-SEG architecture, where Shallow Trench Isolation (STI) served to separate extrinsic base and collector with a thick oxide layer. A standard 300 nm STI is however not compatible with a fully-implanted integration, since ion implantation tools are hardly capable of adequately doping at such depths with a consistent dose. The idea of a Super Shallow Trench Isolation (SSTI) was already presented by Canderle [6] and has been re-evaluated for the EXBIC architecture. This structure simply consists in an isolation trench realized by a shallow etching below 100 nm adapted to the implantation tools capabilities and therefore compatible with a fully-implanted integration.

Preliminary studies investigated the integration of an SSTI in order to define the correct sequence of processes [5, 23]. An isolation trench depth between 25 nm and 100 nm has been studied, generating a compromise between base-collector capacitance and collector resistance. Considering both benefits of reduced capacitance and requirements for ensuring a good resistance, results converged on a 50-nm-deep isolation structure realized at the beginning of the process flow right after STI. Carbon and phosphorus are successively implanted through the SSTI in order to dope the collector. For confidentiality reasons, the exact energies and doses will not be disclosed. The reference phosphorus energy e_P is chosen to place the projected range $R_{p,P}$ around 100 nm below the substrate surface. The carbon reference energy e_C allows to place the peak slightly deeper in order to obtain a Transient Enhanced Diffusion (TED)-suppression effect and limit defects[16, 17]. The carbon dose d_C, in the order of $10^{15} cm^{-2}$, is enough to induce substrate amorphization. This condition is fundamental and its reasons will be detailed in the following. Phosphorous dose d_P can vary from being a fraction to a multiple of d_C.

Figure II.3 highlights the main collector weak points of the preliminary EXBIC architecture.

Many defects are present in spite of the carbon plus phosphorus co-implantation. Even though the underlying principles of this doping technique are known, a study for this specific integration is still needed. Defects can not only degrade collector resistance but also lead to important current leakage if included in the base-collector depletion region.

The SSTI can be successfully integrated to introduce a thicker layer of oxide between extrinsic base and collector. Due to physical limitations of the photolithographic process, both SSTI and emitter window must be sized accounting for possible overlay mismatch. This solution requires in practice that the SSTI in not present all along the extrinsic base, leaving a zone close to the emitter window where base and collector are separated only by a thin layer of oxide. As a consequence, the extrinsic base-collector capacitance C_{BC} is still considerable and dependent from the doping levels outside the junction.

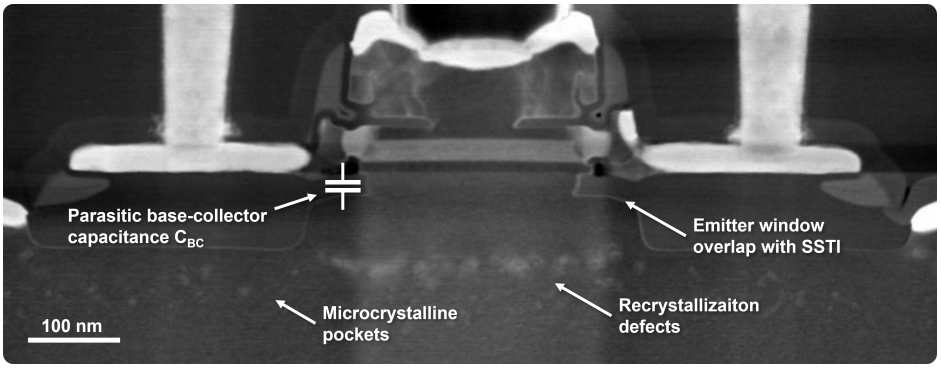

Figure II.3 | TEM cross-section showing the weak points of the collector in the preliminary EXBIC architecture.

This section focuses on the development of a better collector integration for the Go To EXBIC architecture.

Section 1.1 details a study for avoiding defects in the collector due to ion implantation and SSTI-induced stress.

Section 1.2 details the considerations leading to an improved version of the SSTI.

1.1 Ion implantation defects suppression

Suppression of defects in the collector is crucial to ensure a reliable integration prior to any collector resistance R_C reduction. Indeed, defects are known to degrade electron mobility[20] impacting overall collector resistance and transit frequency f_T as a consequence[1]. Even though carbon plus phosphorus co-implantations have been introduced for defects suppression, some kind of defects such as zipline dislocations cannot be avoided with the presence of carbon due to their generation mechanism[34, 16]. It is also important to ensure that no defect is located in the depletion zone of the base-collector junction since it could cause current leakage and device malfunctioning[41, 8].

The addition of a SSTI introduces more complexity to the defect generation mechanisms. Trench isolations are known to introduce stress in the substrate [19, 59], possibly inducing defects [59, 45] or guiding defects to combine into extended defects [30, 12]. The presence of stress within the amorphized zone can act on the recrystallization kinetic during Solid Phase Epitaxial Regrowth (SPER)[54].

A study for defining optimal implantation conditions is important to ensure device functionality before dealing with the resistance itself. For this reason, a variation on the implanted phosphorus dose d_P spanning from $d_C/3$ to $2d_C$ has been performed to observe how defect formation can be modulated.

A first TCAD study served to understand the constraint induced by isolation structures in the substrate. Results will be used to interpret observations made on real devices.

On silicon, three cases have been distinguished depending on implantation-induced amorphous layer positioning with respect to the surface (Fig.II.6. The layer can be fully buried in the bulk, touching the surface or surfacical. As a consequence, the surface can be crystalline, partially amorphized or fully amorphous.

1.1.a TCAD simulation of stress distribution in the substrate

The stress distribution in the substrate due to SSTIs cand be studied by the means of TCAD simulations.

Figure II.4 depicts Synopsis®Sentaurus Monte Carlo simulations of sub-

strate pressure calculated as

$$P = -\frac{1}{3}\sum_{i}^{a}\sigma_{ii} \tag{II.1}$$

where σ_{ii} is the stress in each direction.

Shrink factor during SSTI densification is set to 10 % and the trench aspect ratio is close to 6. The resulting stress pattern before implantation is complex. It is important to consider that densification occurs with a thick oxide layer covering the whole wafer, introducing compressive or extensive strain depending on the point in the substrate. Figure II.5 helps understanding the acting forces by depicting strain along x and y axes. Since SSTIs shrink in the two dimensions, the resulting constraint will be a combination of vertical and horizontal forces. It is also important to consider that a thick oxide layer is present during densification and is removed only after. This explains the presence of two opposite horizontal components between the isolation structures, leading to a V-shaped front when calculating total pressure. Stress impact on recrystallization speed [30, 54] is expected to induce a non-uniform crystallization front during SPER.

Examined at the end of the production flow, the residual pressure is radically modified. Amorphization induced by ion implantation and thermal treatments allow to release or rearrange the constraint. Considering the different pattern with respect to before implantation, it is possible that the stress field could induce defects migration.

1.1.b Silicon testing

Silicon is doped by high-dose carbon and phosphorus ion implantations capable of amorphizing the substrate. A phosphorus projected range $R_{p,P}$ two times the SSTI depth is considered optimal for minimizing collector resistance. Carbon projected range $R_{p,C}$ is arranged accordingly to obtain a defect pumping effect limiting Transient Enhanced Diffusion (TED)[17]. $R_{p,C}$ is 25 % bigger than $R_{p,P}$. A carbon dose on the order of 1e15 at/cm^2 is implanted to induce silicon amorphization with an energy correspondent to the reference projected range $R_{p,C}$. Variations on phosphorus dose with all the other process parameters constant allow to modulate the extension of the amorphous zone while keeping $R_{p,P}$ constant, modulating surface amorphization as a consequence. Tested phosphorus doses are 1/3, 1/2, 1 or 2 times the carbon dose. In the following they will be referred to as: P = C/3, P = C/2, P = C and P = 2C.

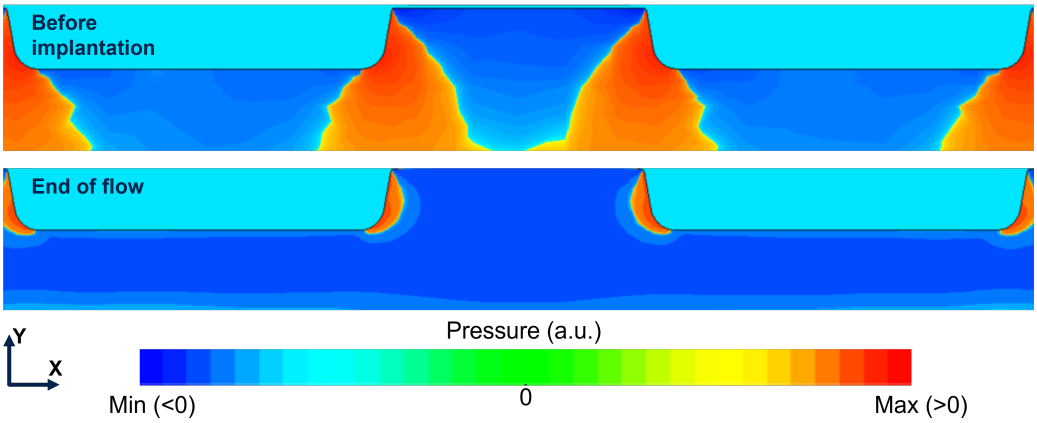

Figure II.4 | TCAD simulation of a device depicting silicon constraint between SSTIs before implantation and at the end of the production flow. Normalized values.

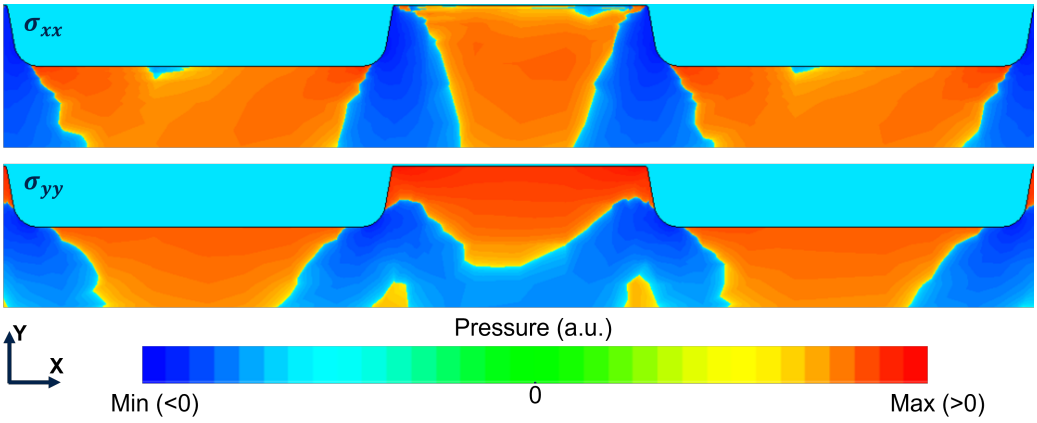

Figure II.5 | TCAD simulation of a device depicting components of silicon constraint between SSTIs before implantation. Normalized values.

Ion implantations have been performed on blanket wafers featuring an 8 nm oxide film to evaluate substrate amorphization through Transmission Electron Microscopy (TEM).

Tested implantation conditions have been reproduced for doping the collector of Heterojunction Bipolar Transistors (HBT) realized with the Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) architecture[64] and featuring a $0.2{\times}5\ \mu m^2$ emitter window. Super Shallow Trench Isolations (SSTI) are obtained by plasma etching, High Aspect Ratio Process (HARP) trench filling, oxide thermal densification and Chemical Mechanical Polishing (CMP) planarization. Oxide shrink ratio during densification is approximately 10 %. Carbon plus phosphorus ion implantations are then performed on the patterned substrate. Solid Phase Epitaxial Regrowth (SPER) occurs during the following high-temperature dielectrics depositions and epitaxies required for transistor fabrication. A 2 h 680 °C thermal treatment is held capable of attaining total substrate recrystallization, with the following steps allowing carbon to interact with defects[17].

Defects in the final device are visually evaluated through TEM cross-sections.

Time Of Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) is used to trace carbon profiles in dedicated 1 mm^2 structures on the same wafers.

On a blanket wafer, three cases have been distinguished depending on resulting surface amorphization. Figure II.6 reports TEM cross-sections of as-implanted wafers. For a phosphorus dose P = C/3, the amorphous layer is buried within the substrate and a continuous crystalline layer is present at the surface (fig. II.6a). P = C/2 leads to a shallower amorphous layer, with the amorphous-to-cristalline (a-c) transition layer placed at the wafer surface (fig. II.6b). Crystalline grains suspended in amorphous silicon are visible close to the surface. The substrate surface is completely amorphous when implanting with a P = C and P = 2C (fig. II.6c).

Four cases are distinguished when reproducing the same implantation processes on patterned wafers. Figure II.7 displays TEM cross-sections of device collectors implanted with the same conditions. Cuts are obtained after the complete production flow. In the case of a phosphorus dose P = C/3 generating a buried amorphous layer, zipline defects form after recrystallization (fig. II.7a). No defects are visible below the isolation structures but a discontinuous upwards-bent zipline with a minimum in the center of the device is present between the SSTIs. Phosphorus dose P = C/2 result in

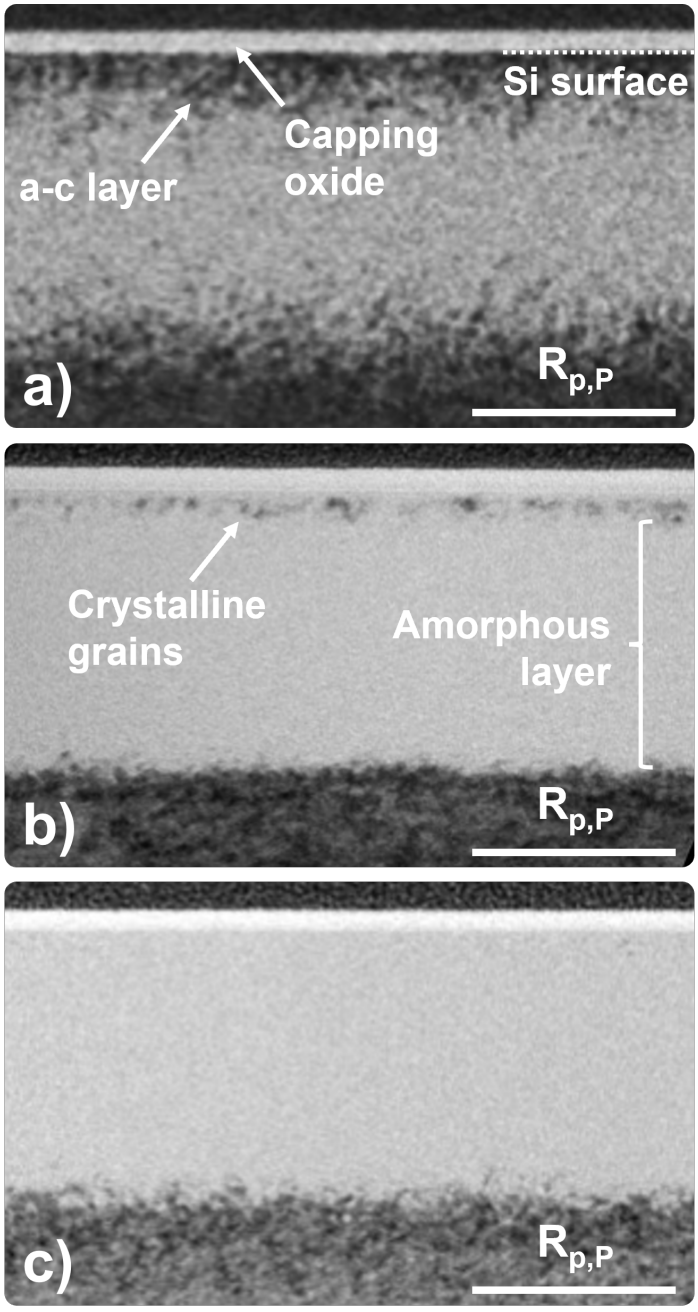

Figure II.6 | TEM cross-section of Non-Product (NP) wafers after implantation with phosphorus doses of a) P = C/3 b) P = C/2 c) P = C.

various defects in the central zone of the transistor (fig. II.7b). Defects are essentially misoriented crystals included in the substrate lattice. Figure II.8 reports a longitudinal TEM cross-section of a device implanted with P = C/2 featuring a particularly high defect density. In this case a zipline is visible as well as a hairpin dislocation extending from the zipline all the way up to the upper part of the transistor. A phosphorus dose P = C leads to a defect-free collector at the end of the production flow (fig. II.7c). Some clusters are visible in the collector of a device implanted with P = 2C (fig. II.7d). Defects are placed between the isolation structures and reach different depths down to $R_{p,P}$.

TOF-SIMS profiles of carbon density in the substrate after the whole production flow is reported in figure II.9. Wafers implanted with a phosphorus dose P = C/3 show a clear segregation effect around $R_{p,P}/2$. The carbon profile of a wafer implanted with P = C/2 has multiple bumps. A minor peak is placed close to the surface ($< R_{p,P}/3$) while the concentration is reduced after $R_{p,P}$. A smooth profile is obtained with P = C. With respect to other profiles, a a phosphorus dose P = 2C leads to a lower carbon distribution close to the surface but higher concentration towards the deeper part of the substrate.

An amorphous layer buried in the substrate has been obtained with a phosphorus dose P = C/3. Since SSTIs are thicker than the monocrystalline residual layer, the silicon below the isolation structures is totally amorphous and a single upwards recrystallization front occurs with no consequent defect. Between the isolation structures, a zipline is formed in accordance with literature[16] but has a complex shape. The upwards-bent defect line can be explained observing the pressure chart before implantation (fig. II.4a): SSTI densification induces a compressive stress field impacting the recrystallization speed of the upwards SPER front, leading to a shallower zipline on the edges. The reduced substrate stress after implantation (fig. II.4b) results insufficient for generating any additional defect. TOF-SIMS profiles (fig. II.9) confirm a massive presence of defects linked to carbon segregation in accordance with literature. Notice that the structure used for obtaining such profiles is too wide for detecting the contribution of the shallower defects which will be limited to its edges.

The amorphous-to-cristalline (a-c) transition layer is at the substrate surface when implanting with a a phosphorus dose P = C/2, meaning that the surface is not totally amorphous. Transversal TEM cross-section of a complete device (fig. II.7b) highlights some misoriented grains included in the

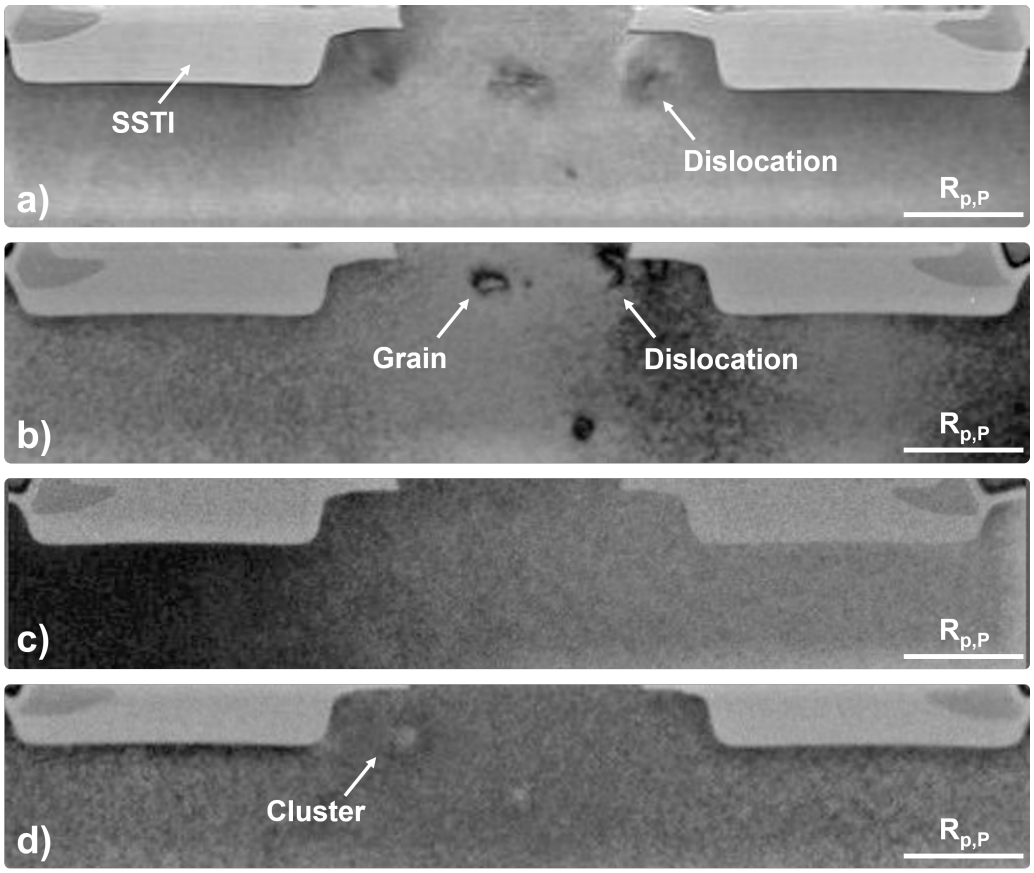

Figure II.7 | TEM cross-section of patterned wafers implanted with phosphorus doses of a) P = C/3 b) P = C/2 c) P = C d) P = 2C. Cuts performed at the end of the production flow.

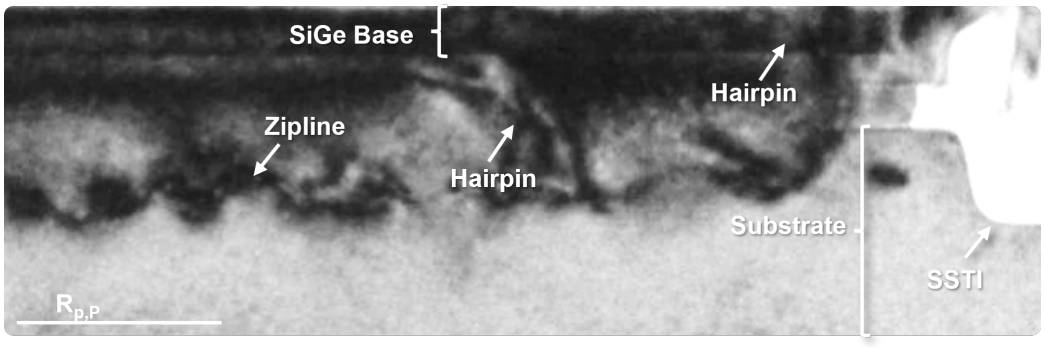

Figure II.8 | Longitudinal TEM cross-section of a complete device implanted with a phosphorus dose P = C/2.

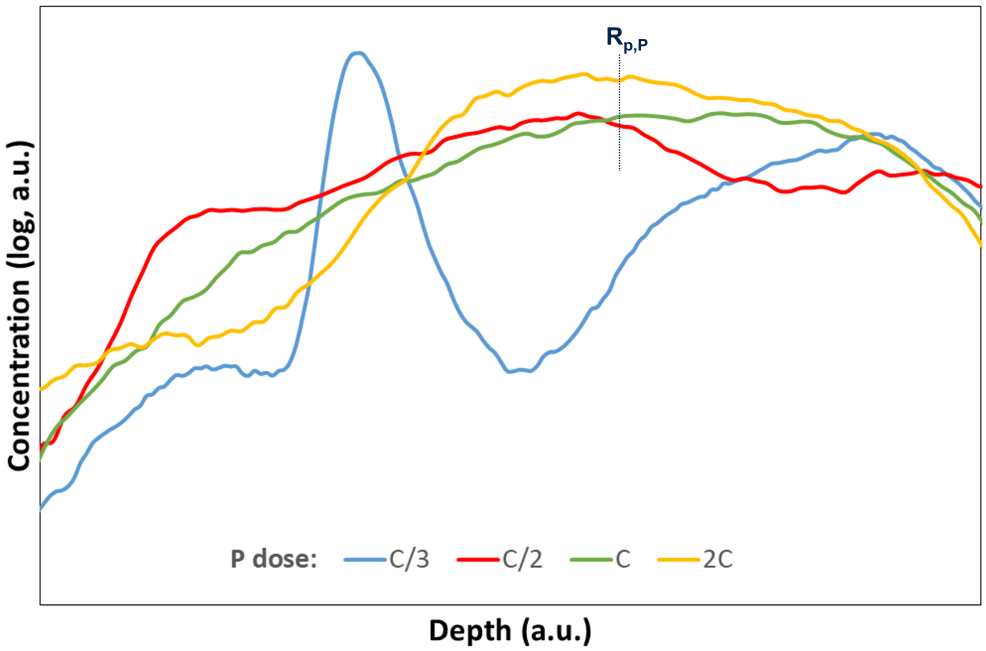

Figure II.9 | TOF-SIMS profiles of carbon measured on patterned wafers.

crystal lattice. For the observed device, the grains were small enough to be included in the upwards recrystallization front before they could merge. The longitudinal TEM cross-section (fig. II.8) shows on the other hand both a zipline and hairpin dislocations. In this case the suspended crystalline grains have grown enough to merge, generating an additional downwards recrystallization front. Hairpin dislocations are formed at the merging point of misoriented grains. The difference between figure II.7b and figure II.8 in term of defects highlights that this degree of surface amorphization can have quite different results depending on how crystalline clusters arrange during recrystallization. Carbon profile (fig. II.9) indicates the presence of some defects close to the surface. The bumps observed in the rest of the profile are attributed to deep defects observed in the TEM cross-section.

The total surface amorphization obtained when implanting with a phosphorus dose P = C and above gives different results when applied to a complete device. TEM cross-sections show a defect-free device with P = C (fig. II.7c). A smooth TOF-SIMS carbon profile (fig. II.9) confirms that there are no defects segregating carbon. Defect-free devices with a phosphorus dose below the carbon one could be obtained by adding a third ion implantation at

$R_p < R_{p,P}$ capable of amorphizing the residual crystalline silicon at substrate surface and induce a single upwards recrystallization front. Effectiveness of this solution has not been investigated and has to be proved.

A collector doped with a phosphorus dose P = 2C shows some small clusters between the isolation trenches (fig. II.7d). Such defects are different from dislocations observed at lower ratios. Carbon concentration is low near the surface and rises at a depth close to $R_{p,P}/2$ (fig. II.9), indicating that the defect-generating mechanism is different from the one of previous cases. The high phosphorus dose induces a big amount of silicon self-interstitials, possibly higher than the carbon dose. Carbon diffusion is therefore oriented towards the zone with higher self-interstitial concentration around $R_{p,P}$[48]. In zones where the carbon dose is insufficient to trap all self-interstitials, clusters will form and evolve during the multiple thermal treatments required for device fabrication[44]. Comparing clusters position with the simulated substrate pressure at the end of production flow (fig. II.4b), it appears that any strain in the collector could drive self-interstitial clusters positioning. A deeper analysis is required to understand if cluster positioning evolves with the thermal treatments required for fabrication. Defect evolution with device lifetime should also be investigated to assess whether these defects can further evolve with consequences on reliability. Phosphorus doses above two times the carbon dose, implying higher self-interstitials, could lead to increased cluster concentration and require further investigation if needed for device integration. Observations validate that phosphorus doses inducing total surface amorphization are not affected by recrystallization-induced dislocations as seen at lower doses. It is concluded that the pressure induced by SSTI densification is not at the origin of dislocation formation in the substrate but it only acts as a recrystallization speed modulator during SPER.

1.1.c Device functionality

Device functionality has been assessed through electrical testing at three different bias voltages. Measurements are performed directly on wafer through a Semiconductor Parameter Analyzer (SPM). A Back-End Of Line (BEOL) consisting of 8 metal layers allows to directly bias the single device under test. For each implantation condition, measurements have been performed on 9 evenly-spaced devices per wafer on at least 2 different wafers, i.e. at least 18 devices per process split. Low, medium and high injection levels correspond to a base-emitter voltage V_{BE} of 0.5 V, 0.7 V and 0.9 V respectively with constant base-collector voltage V_{BC} of 0 V. Collector current ideality

factor (η_{I_C}) is obtained by comparing theoretical and measured current values at low and medium injection levels[1]. An $\eta_{I_C} = 1$ corresponds to an ideal device and higher values indicate presence of non-idealities. Measurements have been performed on at least two wafers per tested condition.

Average values and relative standard deviation of collector currents I_C at different injection levels (V_{BE} = 0.5 V, 0.7 V, 0.9 V; V_{BC} = 0 V) and calculated ideality factors η_{I_C} measured on 0.2×5 μm^2 devices are reported in table II.2.

Table II.2 | Average values and relative standard deviation of low, medium and high injection collector currents I_C and correspondent ideality factor η_{I_C} for different phosphorus doses. 0.2×5 μm^2 reference devices.

		Phosphorus dose P			
		C/3	C/2	C	2C
Average	Low injection I_C (nA)	167	114	13	13
	Medium injection I_C (μA)	77	225	27	27
	High injection I_C (mA)	11	12	12	12
	η_{I_C}	1,29	3,83	1,02	1,03
σ%	Low injection I_C (%)	120	122	13	14
	Medium injection I_C (%)	102	117	13	14
	High injection I_C (%)	3	52	4	5
	η_{I_C} (%)	22	60	<1	<1

Measurements performed on devices implanted with phosphorus dose P = C/3 demonstrate current leakages, particularly at low injection. Even if the ideality factor η_{I_C} is not as bad as for other splits, the obtained value is not acceptable for the target technology specifications. Moreover, high standard deviation indicates bad control over the phenomena inducing such degradation.

Implanting with a phosphorus dose P = C/2, the impact on device functionality is important. High current leakages both at low and medium injection are detected, with a consequent huge ideality factor η_{I_C}. High standard deviation is observed on all values. Even if less dense, defects are enough to induce massive current leakages at all injection levels. The presence of hairpin dislocations extending to the superior parts of the device certainly have a critical impact on leakages as already observed in literature[41, 8]. The

elevated relative standard deviation well represents the variability observed in TEM cross-sections: some single devices are in fact fully functional while others are not working at all. Comparing with the results obtained on the P = C/3 devices, it results that collector current non-idealities are dependent on defects depth rather than on their concentration. P = C/2 reduces the peak carbon concentration by more than one order of magnitude when compared with P = C/3 and behalves its depth. η_{I_C} is much more degraded for the devices implanted with P = C/2.

The almost ideal collector currents obtained with a phosphorus dose P = C well relate with the absence of defects and carbon segregation close to surface. This solution appears to be the best condition among the ones tested in this study.

Collector current measurements performed on wafers implanted with a phosphorus dose P = 2C indicate no particular difference with P = C devices, meaning that observed defects are not electrically active.

1.2 Super Shallow Trench Isolation (SSTI) design

In the EXBIC HBT, SSTI replaces Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG)'s STI between base and collector by simply reducing the trench depth. STI is however still present around the transistor to isolate it from its neighbors. Even though the EXBIC architecture is well adapted to SSTI, some optimizations are still possible.

1.2.a Ring-shaped SSTI

Specifically to EXBIC HBTs, a SSTI featuring a ring-shaped trench is a very shallow (<100 nm) isolation structure where the trench encircles the central zone of the device below the emitter window opening in the stack. Even though photolithographic alignment ensures the minimum mismatch between emitter window and SSTI, sizing has to account for process variations: for this reason, the distance between the two branches of the SSTI is bigger than the emitter window width. This procedure requires maximum care to avoid an opening on the oxide of the isolation structures, which could perturb the selective epitaxies of collector and lead to a missing device. Figure II.10 shows both the difference in size and the overlap mismatch between SSTI gap and emitter window. In the small zone where the stack does not overlap the SSTI, only a thin oxide layer will be separating the extrinsic base from the intrinsic

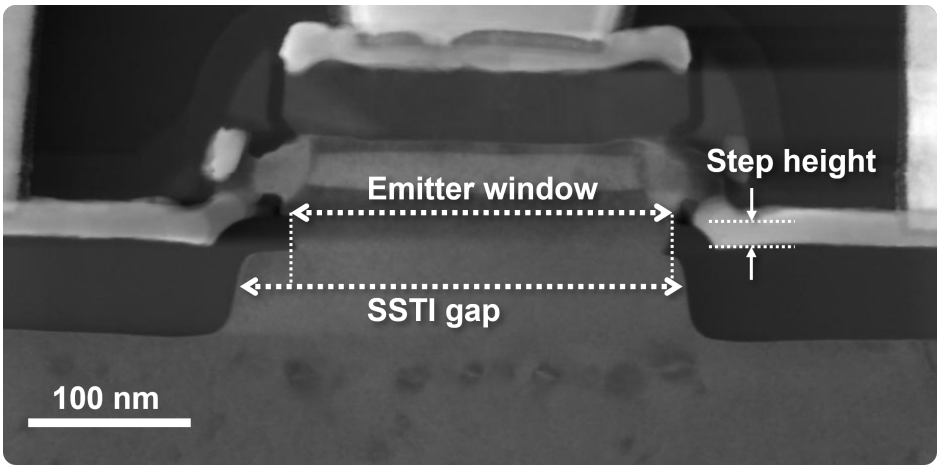

Figure II.10 | TEM cross-section detailing the alignment issues related to a ring-shaped SSTI.

collector. Such zone is responsible for a considerable perimetric contribution to the base-collector capacitance C_{BC}. Due to the small thickness of this oxide, capacitance will also depend on collector and extrinsic base doping [32]. Base-collector capacitance C_{BC} is therefore not completely independent from extrinsic base and collector doping. We can conclude that, even if a ring-shaped SSTI reduces base-collector capacitance C_{BC}, it is not totally capable of decorrelating extrinsic components of base and collector.

Another tiny yet important matter in SSTI sizing is represented by the step height between the top of the SSTI and the actual substrate surface (cf. Figure II.10). The Chemical Mechanical Polishing (CMP) used to planarize the isolation structures after oxide filling can be responsible of a light overpolishing of the SSTI oxide, resulting in a surface misalignment with the surrounding silicon. The EXBIC architecture is very sensitive to this matter because the intrinsic base needs to be perfectly aligned with the stack in order to be correctly contacted by the base link on the sides. Step height variations could therefore degrade base resistance R_B or even avoid formation of the lateral contact. It is also important to consider that epitaxies are susceptible to process variability that could eventually combine with the step height increasing vertical misalignment. Intra- and inter-wafer variability of CMP and epitaxy combined could lead to an extreme variation in device characteristics.

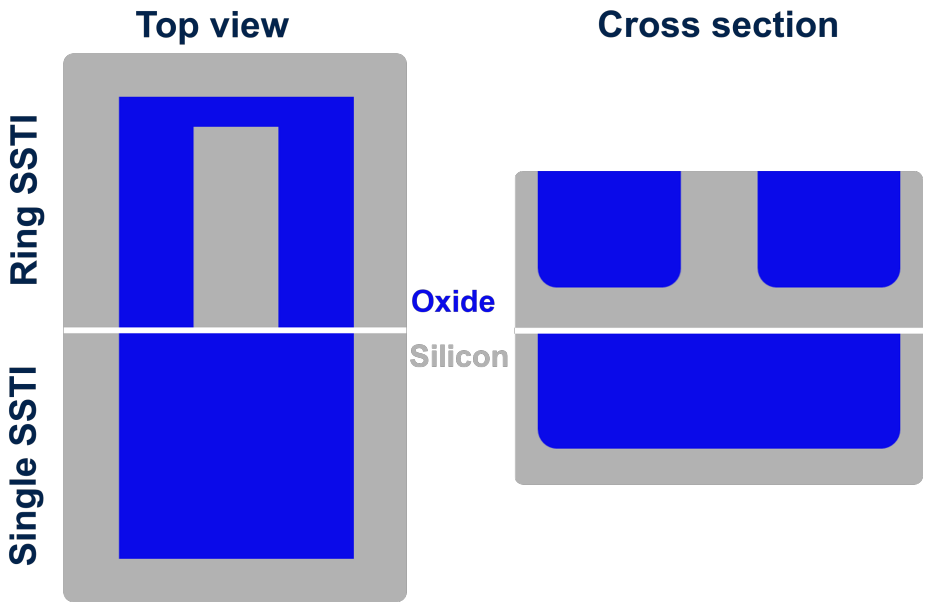

Figure II.11 | Top view and cross-section schematics comparing the ring and single SSTI integrations after trench filling and planarization.

1.2.b Single-trench SSTI

In order to overcome the limitations of a ring-shaped SSTI, a more robust design has been tailored to the needs of an EXBIC HBT. An SSTI featuring a single trench, hereinafter called single SSTI, is a way of overcoming said problems [25]. The trench outline is identical to the ring-shaped one but has no gap below the emitter window opening. Figure II.11 shows the difference between the two integrations.

In this way, the emitter window will be opened on the central part of the SSTI and an additional etching step will be required to eliminate the trench oxide and reach the underlying silicon. Such feature eliminates the requirement for fine overlapping because the window and the gap between the trenches are self-aligned and in fact part of the same cavity. Collector epitaxy needs to be thicker in order to compensate the lower starting point and correctly align the base with the stack, in practice replacing the etched trench oxide. Regarding the step height problem, the stack will be perfectly laid on the SSTI no matter the amount of overpolishing. Variability of collector epitaxy thickness still remains a critical point for good vertical alignment. Figure II.12 shows a TEM cross section of an EXBIC HBT featuring a single

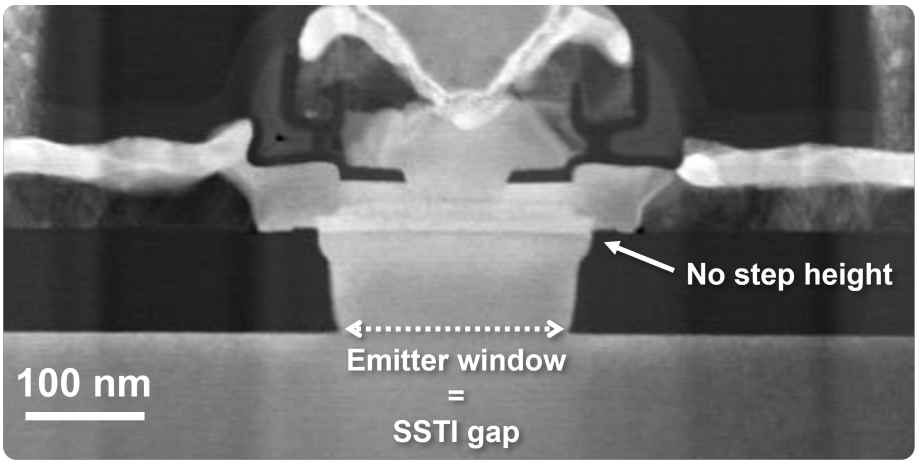

Figure II.12 | TEM cross-section detailing the improvements obtained with a single-shaped SSTI.

SSTI. The main improvements with the ring design are pointed out. Notice that devices shown in Figure II.10 and Figure II.12 present different integrations of the extrinsic base which will be discussed in Section 2.

An important consideration has to be made on collector doping.

Ring-shaped SSTIs allow to use an additional shallow collector implantation between the trenches to generate a so-called Selectively Implanted Collector (SIC). In this way, the base-collector junction can be tuned independently to collector resistance R_C. The implantation is performed right after the standard carbon plus phosphorus doping but requires a specific mask to target the selected zone. Since the implantation is done before substrate recrystallization, defects can be avoided following the principles described in Section 1.1.

Single-trench SSTI is not compatible with this technique because there is no silicon between two trenches at the moment of collector implantation. An ion implantation limited to the zone beneath the emitter window is however still possible but the profile doping would be different. A similar outcome could be obtained by implanting the epitaxial collector using the emitter window as a hard mask. An amorphizing ion implantation is vital in this case because any defect would be easily included in the depletion region of the base-collector junction and induce current leakage. An adequate doping concentration would be in the order of $1e17cm^{-2}$ and a shallow phosphorus

implantation alone is hardly amorphizing at the correspondent doses with a projected range below 100 nm. The addition of a carbon doping alike to what done in the main collector would reproduce the results seen in Section 1.1 and avoid defects while perfectly controlling TED. Such solution has not been explored due to the cost that it would imply on top of its complexity. Dopant contamination of the stack has also been imagined as a possible reliability matter.

1.2.c Electrical characterization of the two SSTI integrations

Even though it is really hard to directly compare two integrations of SSTI with the same collector implantation, Table II.3 reports the significant figures of merit measured on two devices with a ring- and single-shaped SSTI. They feature the same collector carbon plus phosphorus co-implantation resulting in a sheet resistance of 65 Ω/sq. The device integrated with a ring SSTI has an optimized doping profile thanks to the addition of a SIC implantation. The device featuring a single SSTI is the first one integrated with this isolation structure and misses any possible optimization.

Table II.3 | Figures of merit of two devices integrating respectively a ring-shaped SSTI and a single-trench SSTI. $0.2 \times 5\ \mu m^2$ reference devices.

		Ring SSTI	Single SSTI
η	I_B	1.26	1.30
	I_C	1.03	1.03
Early voltage	V_{AF} (V)	74	113
Breakdown voltage	BV_{CBo} (V)	4.6	5.2
Capacitance	C_{BC} (fF)	7.7	5.3
Base resistance	R_B	103	66
Frequency	f_T (GHz)	413	300
	f_{MAX} (GHz)	351	360

Base and collector current ideality factors η_{I_B} and η_{I_C} indicate that devices operate correctly with both SSTI integrations.

The higher forward Early voltage V_{AF} of the single SSTI device is a clear reflection of the mild doping profile of the collector, which is confirmed by the higher base-collector breakdown voltage BV_{CBo}.

In the single SSTI integration, the base-collector capacitance C_{BC} reduces by 30 %. If the new SSTI integration contributes to reducing the extrinsic

capacitance, the sub-optimal junction tuning certainly plays a concurrent role, degrading transit time. Indeed, in spite of reduced C_{BC}, f_T is more than 100 GHz lower than the ring SSTI counterpart surely due to a degraded transit time.

The decrease of base resistance is attributed to a better lateral link between intrinsic and extrinsic base thanks to the elimination of the step height problem.

In spite of the huge f_T difference, almost identical values of f_{MAX} are obtained with the two integrations due to improved parasitics. Recalling the dependence between f_T and f_{MAX} (cf. Equation (I.9)), one may notice how parasitics have an impressively lower impact. f_{MAX}/f_T ratio passes from 0.85 of the ring SSTI to 1.2 to the single SSTI. Even though an optimized collector doping profile will lead to an increase in C_{BC}, the single SSTI integration has a clear potential for further maximizing f_{MAX}.

The study for optimizing the performance of the single SSTI collector integration is discussed in Section 1 of Chapter III.

2 Extrinsic base module

Meant to overcome limitations of the DPSA-SEG integrations, the key advantage of the extrinsic base in the EXBIC architecture is to address base resistance R_B minimization independently from base-collector capacitance C_{BC} in order to increase f_{MAX}. Base resistance can be separated in two main components, namely intrinsic and extrinsic. In a first approximation, the intrinsic base resistance depends from the base epitaxy performed in the emitter window right after collector epitaxy. The extrinsic component is therefore dependent from the remaining part of the structure.

Figure II.13 shows a detail of the TEM cross-section presented in the introduction of this chapter, highlighting some flaws of the extrinsic base integration in the preliminary EXBIC architecture. Air gaps have different sizes on the two sides of the device. The base link has not grown adequately and the contact with the rest of the extrinsic base is badly shaped.

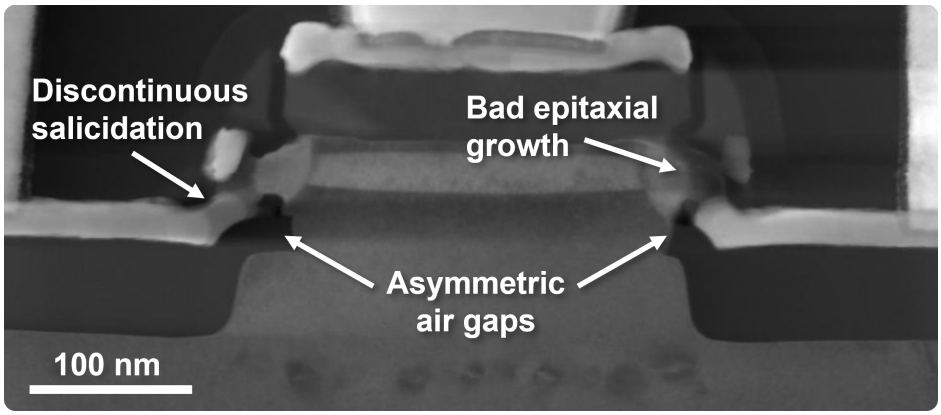

Figure II.13 | TEM cross-section showing the flaws of the 2-step extrinsic base integration.

The first part of this section focuses on reviewing the extrinsic base integration discussed at the beginning of this chapter, detailing all the limitations encountered during development.

The second part of this section presents an improved integration of the extrinsic base aiming to simplify the production process and gain control over some features inducing electrical non-idealities.

2.1 2-step extrinsic base integration

The 2-step extrinsic base integration makes use of two different selective epitaxies to connect the intrinsic base first and form the contact zone of the extrinsic base after.

The process flow is schematized in Figure II.14 and can be described as follows:

1 At the end of collector epitaxy in the emitter window, air gaps are present in the polysilicon seed layer.

2 Later in the flow, the emitter polysilicon is patterned and protected by an oxide encapsulation. The sacrificial nitride deposited with the stack is exposed.

3 A selective etching removes the sacrificial nitride opening the cavities around the intrinsic base.

4 The so-called base link is laterally grown by selective epitaxy and in-situ doped with boron and eventually germanium.

5 The underlying oxide layer is etched exposing the polysilicon seed layer. The base link partially masks the underlying oxide layer, leaving a small stub keeping the air gap closed.

6 A second in-situ-doped selective epitaxy grows the contact zone of the extrinsic base.

This solution, initially conceived to exploit the features of SOI substrates [64], allows high versatility. For the contact zone it is important to tune doping and thickness in order to minimize the extrinsic base resistance R_{sBx}. The base link must ensure minimum parasitic resistance between intrinsic base and contact zone while avoiding boron penetration in the intrinsic device, impacting the doping profile. Thanks to the fact that the link grows horizontally starting from the intrinsic base, a complex doping profile can be applied to achieve maximum control.

2.1.a Air gaps

Even though air gaps are intended to simplify the original EXBIC architecture of Vu [63], they are quite challenging from a robustness perspective.

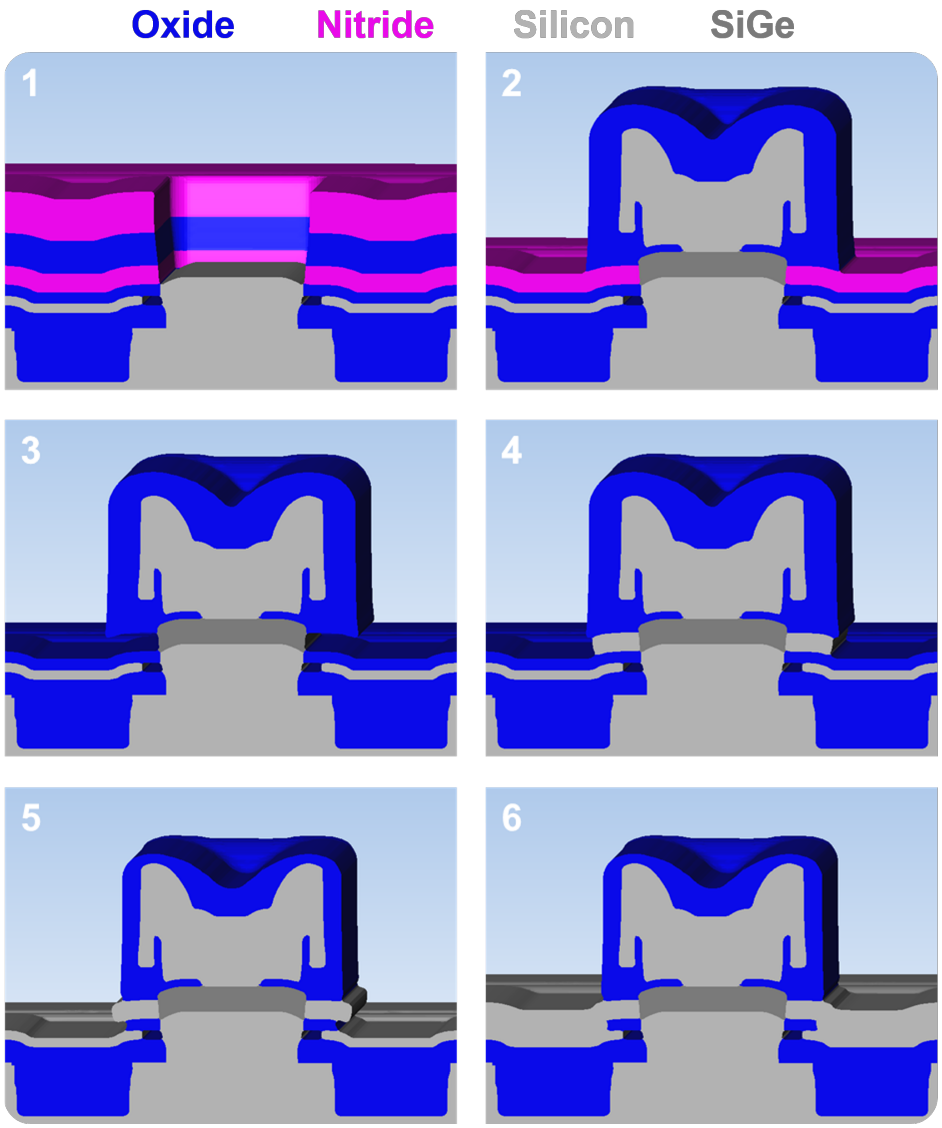

Figure II.14 | Process flow of the 2-step extrinsic base integration simulated with Coventor SEMulator 3D.

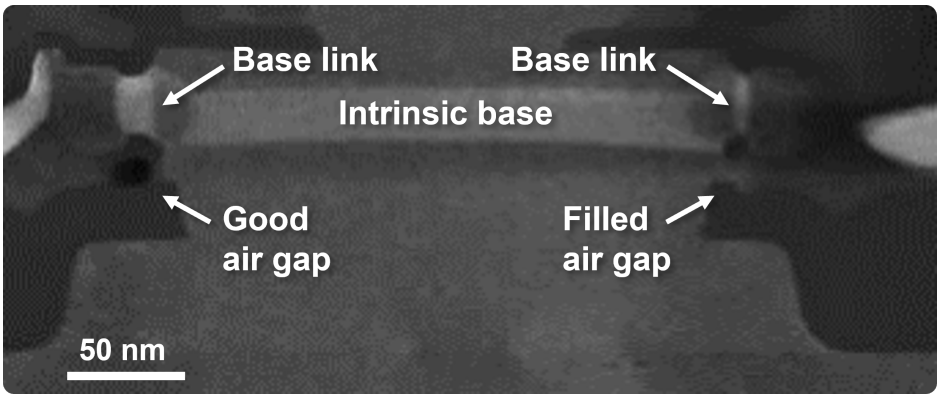

Figure II.15 | TEM cross section of an HBT presenting both a well-formed air gap and a parasitic base-collector junction.

Figure II.15 shows a typical asymmetry issue with air gaps observed on TEM cross-sections.

Oxide spacers were initially present in the architecture for separating the intrinsic collector from the extrinsic base on its sides. Air gaps are meant to avoid oxide spacers by separating collector and extrinsic base with air pockets. The collector selective epitaxy process exploits different growth and etching rates on the various materials to achieve net polysilicon etch at the end of the growth step. The polysilicon layer in which air gaps are formed is thin enough to be mostly composed of grains of the same size of its thickness. For geometrical reasons, a good air gap in this integration should have an aspect ratio around 2, which means that on average two grains will be etched during its formation. Since crystalline orientation can not be controlled, the etching process used to open the air gaps will proceed on a random crystalline plane. Due to etching anisotropy [15], the etching rate will depend on grain crystalline orientation and air gap size may vary significantly. If the air gap is too large, the intermediate oxide will not be wide enough to protect it and the top part of the collector may be exposed during Step 6. In this case, the epitaxy used for growing the contact zone of the extrinsic base will grow both on the base link and the collector. This situation must be avoided because a parasitic junction would form and the base-collector capacitance C_{BC} would not be independent from the extrinsic base doping anymore. In addition to this, sub-optimal overlay between the emitter window and the patterned emitter could lead to air gap exposure during Step 5. In Figure II.16 the air gaps grew so much to become visible through the oxide covering the

polysilicon layer.

It is difficult to evaluate the exact impact of such parasitic junctions on the electric FOM but there is no doubt on the advantages of an integration not relying on air gaps for base-collector isolation.

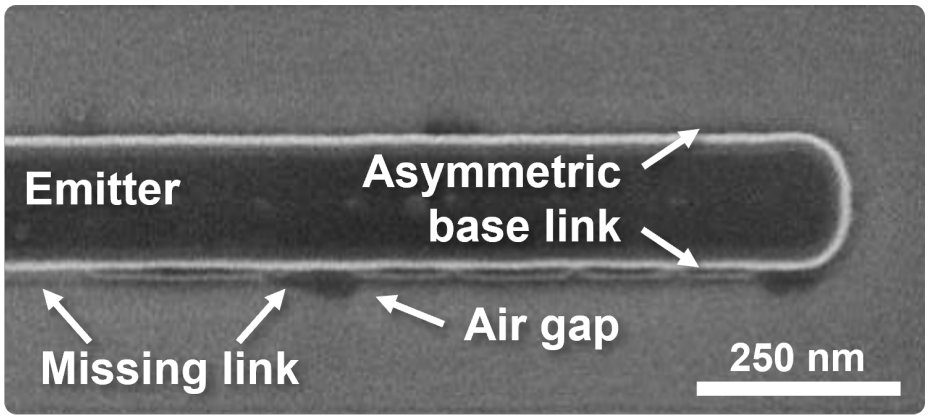

Figure II.16 | SEM top-view picture of an HBT after base link selective epitaxy. Typical defects are highlighted.

2.1.b Base link

Base link is a critical element of the 2-step extrinsic base integration.

The preliminary EXBIC architecture requires the base link to reach the extremity of the emitter encapsulation in order to protect the underlying air gap from being exposed during Step 5 and ensure a correct connection with the contact zone of the extrinsic base in Step 6. Figure II.16 shows a SEM top-view picture of an HBT after base link selective epitaxy (Step 4) where some typical problems can be observed. The base link emerges from below the emitter only one side and is not uniform. In some points the link is hidden below the emitter encapsulation ot totally missing.

The selective epitaxy needed for growing the base link is very sensitive and many effects can combine.

The asymmetrical growth is linked once again to the overlay mismatch between the emitter window and the patterned emitter. This shift modifies the cavity sizing where base link is formed. Since growth occurs in a thin and wide lateral cavity, any sizing modification can impact growth kinetics. This effect can be observed in Figure II.15 where the base link is doped with

germanium (light grey). The link on the left is much wider than the one on the right. Overlay mismatch not only impacts air gap formation but also complicates the correct growth of the base link, which is thinner on the right side. One possible solution would be to oversize the growth time to be sure that the base links entirely fills the cavity. Tilted SEM views of a device realized in such way (Figure II.17) show that the base link grows isotropically when not confined in a cavity. This situation can be particularly problematic during contact salicidation because a short circuit with the emitter can be formed. It follows that base link epitaxy must be conceived considering the varying growth rate as a function of the cavity width and at the same time account for its variability. It is in practice very difficult to obtain repeatable results.

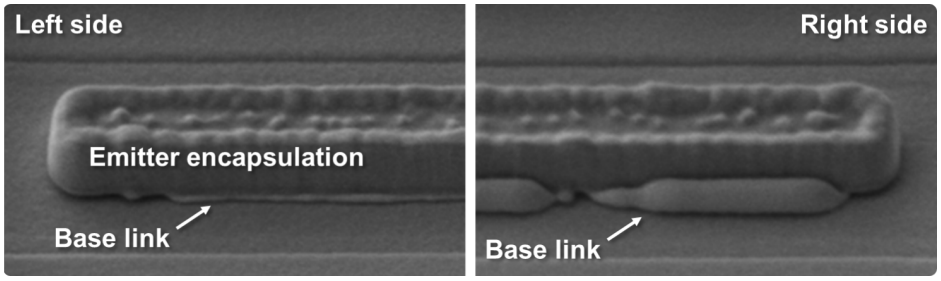

Figure II.17 | Tilted SEM views of the base link on the two sides of an HBT.

Base link discontinuity is due to bad cleaning. Selective epitaxies make advantage of disparate coalescence and growth rates of silicon on different materials [29] and the presence of oxygen on the seed layer can totally block the process.

Specific experiments testing both ex-situ and in-situ cleaning processes have been conducted to find a way of obtaining the best seed layer possible while taking into account the specificities of a lateral cavity with an important aspect ratio.

Process details will not be disclosed here for confidentiality reasons.

Figure II.18 shows the results obtained with perfect overlay and an optimized cleaning process. Notice that strict design rules can be enforced for reducing the overlay variability but its impact can not be avoided completely due to the intrinsic limits of photolithographic alignment.

Another complexity of the base link integration is its monitoring in terms

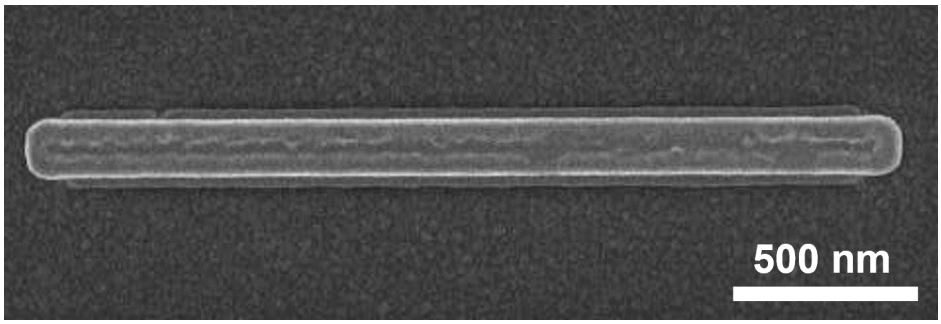

Figure II.18 | SEM top-view picture of an HBT presenting a uniform base link on the two sides. Growth time is oversized to make the link clearly visible.

of doping.

Since the epitaxy is performed in a tiny lateral cavity, traditional techniques such as Time Of Flight - Secondary Ion Mass Spectroscopy (TOF-SIMS) can not be used for its characterization. Even though more advanced techniques could be employed, they are generally not available in the industrial environment. A qualitative idea can be obtained performing a full-sheet epitaxy on a sample wafer and analyzing its composition by SIMS. The impact of cavity size on growth kinetics is however unknown, meaning that the exact chemical composition of the base link is hard to know. Figure II.15 is a clear example of this problem: between the germanium (light grey) of the intrinsic base and the one of the base link there is a darker intermediate zone where germanium is missing and boron distribution is also probably impacted. The specific process used on this wafer was not supposed to introduce such intermediate layer and it will be difficult to understand what happened without the analysis of its chemical composition. It follows that any change in process parameters could lead to an unexpected variation in doping which can only be evaluated indirectly through the analysis of electrical FOMs. Engineering of the process becomes extremely long and complicated in this way.

2.2 1-step extrinsic base integration

The 1-step extrinsic base integration makes use of a single selective epitaxy to connect the intrinsic base and form the contact zone of extrinsic base at the same time.

The process flow is schematized in Figure II.19 and can be described as follows:

1 At the end of collector epitaxy in the emitter window, air gaps are formed in the polysilicon seed layer. Notice that the oxide layer between sacrificial nitride and seed layer has not been produced during stack deposition.

2 Later in the flow, the emitter polysilicon is patterned and protected by an oxide encapsulation. The sacrificial nitride deposited with the stack is exposed.

3 A selective etching removes the sacrificial nitride opening the cavities around the intrinsic base and exposing the polysilicon seed layer.

4 An in-situ-doped selective epitaxy grows the whole extrinsic base. Two growths occur at the same time: silicon grows crystalline in contact with the intrinsic base and polycrystalline over the seed layer. The two fronts grow up until merging. Process conditions influence the growth speed on the two materials and can set the position of the mono-poly interface.

This integration makes an economy of one step during stack deposition and two steps in the fabrication of the extrinsic base. This simplification comes at the cost of lower versatility in the doping profile. While the 2-step integration allows to adopt two different dopings in base link and contact zone, a compromise has to be found in the 1-step integration to minimize R_{sBx} without flooding the intrinsic base with undesired boron.

The first device realized with this integration is depicted in Figure II.20, where the principal differences with the 2-step integration are highlighted.

2.2.a Air gaps

The 1-step extrinsic base integration does not make use of air gaps for isolating the extrinsic base from the collector.

Air gaps are in this case needed to avoid any spurious polysilicon growth during base epitaxy that could cause a polycrystalline-monocrystalline interface in the emitter window. In this case, the presence of grain boundaries, i.e. defects, withing the intrinsic part of the device would lead to device malfunctioning. In Step 1 air gaps are formed similarly to how they were made in the 2-step extrinsic base integration but with less constraints on

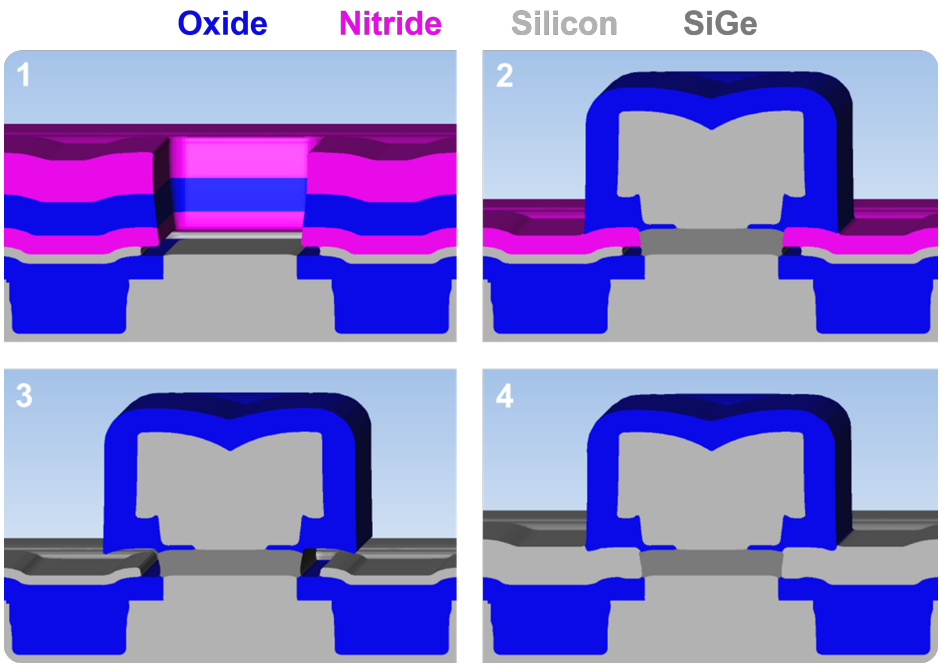

Figure II.19 | Process flow of the 1-step extrinsic base integration simulated with Coventor SEMulator 3D.

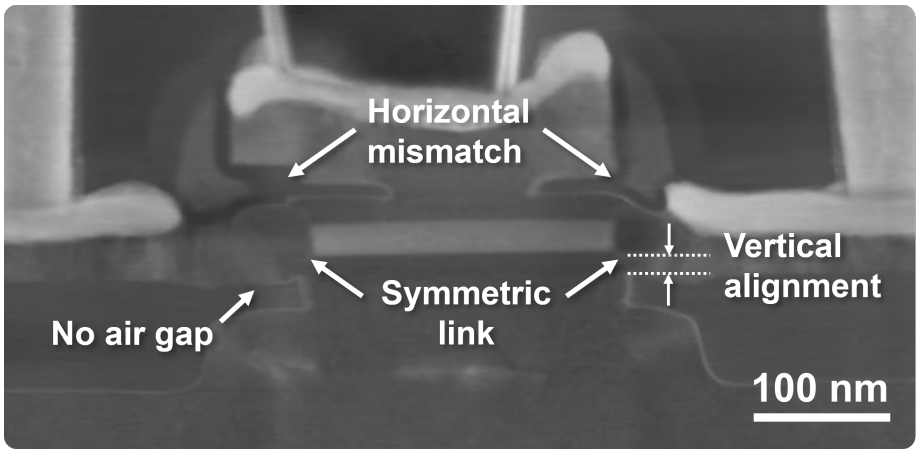

Figure II.20 | TEM cross-section of the first HBT realized with the 1-step extrinsic base integration

their sizing. The only requirement is that in Step 4 the two growth fronts are close enough to merge.

2.2.b Vertical alignment

Vertical misalignment between stack and epitaxies can be source of some problems.

For this reason, the device in Figure II.20 presents a parasitic base-collector junction on the sides where the extrinsic base has grown. Such condition can be source of leakages or loss of control over the junction. The vertical doping profile is designed to set the intrinsic device characteristics and define the transistor behavior: currents and breakdown voltages should therefore be dependent on the vertical doping profile only. The addition of a secondary junction on the sides of the collector can perturbate this ideal condition. Moreover, since the extrinsic base is heavily doped to reduce the extrinsic base resistance R_{sBx}, a perimetric component will add to the base-collector capacitance C_{BC}. Synopsis Sentaurus TCAD simulations (Figure II.21) highlighted that, due to boron diffusion from the extrinsic base, C_{BC} can depend up to 15 % on its perimetric component, generating a shift of some tens of GHz of f_{MAX}.

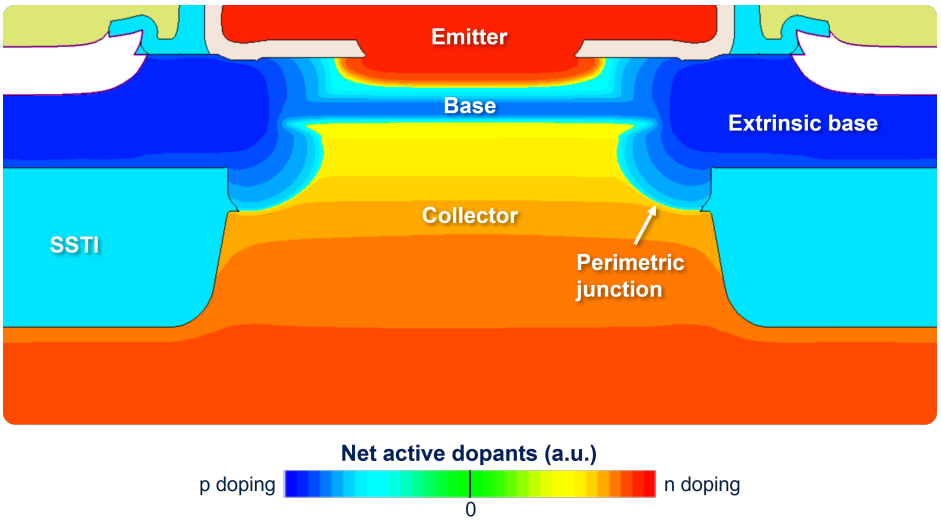

Figure II.21 | Synopsis Sentaurus TCAD simulation of the doping concentration obtained with a heavily-doped extrinsic base.

Since both stack and intrinsic base have quite fixed dimensions, the col-

lector epitaxy must serve to enforce the correct vertical alignment. This results in a slightly thinner collector epitaxy: its top must now align with the polysilicon bottom instead of reaching the oxide laying on it. Figure II.22 compares alignment between epitaxies and stack in the two extrinsic base integrations. The 2-steps integration requires the collector epitaxy to be about 20 nm thicker with respect to the one of the 1-step integration. Assuming collector doping is unchanged, the 1-step extrinsic base will have a more aggressive doping profile in the base-collector junction and adjustments will be needed to obtain the same characteristics and consequent figures of merit (V_{AF}, BV_{CBo}, junction C_{BC}).

In conclusion, the 1-step extrinsic base integration does not overcome the vertical alignment requirements of the 2-step integration.

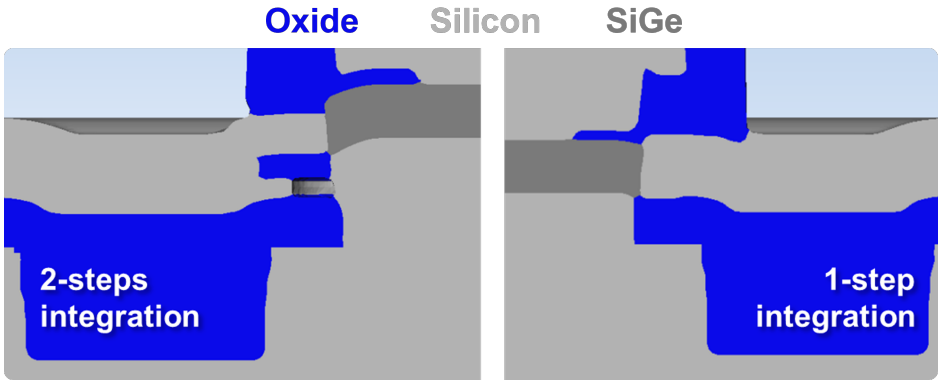

Figure II.22 | Comparison of vertical alignment in 2-steps and 1-step extrinsic base integrations.
Simulated with Coventor SEMulator 3D.

2.2.c Overlay mismatch tolerance

The device observed in Figure II.20 presents an important overlay mismatch between the emitter window and the external emitter patterning. The formation of the extrinsic base is however not impacted by this shift and the link with the intrinsic base is perfectly formed. This tolerance over overlay mismatch is in fact one of the main advantages of this integration. Since the base link is formed at the same time of the contact zone, there is no need to ensure a perfect vertical alignment of emitter, base link and air gap. A correct sizing of the air gap will ensure that a situation like the one in

Figure II.17 will not happen no matter the overlay. Notice also that the chemistry used for this integration is less sensitive to the cavity dimensions, meaning that overlay has very limited impact on the resulting link.

2.2.d Epitaxial growth parameters

The 1-step integration of the extrinsic base presents many advantages regarding the process parameters of the selective epitaxy.

Since base link and contact zone are grown at the same time, the epitaxy parameters will define dopants incorporation in both parts. This is a big advantage in device design since a simple SIMS will allow to know precisely the composition of the grown silicon.

A process window on boron concentration and germanium incorporation showed that this integration is very tolerant towards the epitaxy process parameters. Figure II.23 shows the results of this test on TEM cross sections where the crystalline orientation of the grains has been investigated with the ASTAR technique [50]. Four conditions have been tested with two different boron concentrations and with the optional presence of germanium. Analyses on the crystalline orientation show that the interface between monosilicon grown on the intrinsic base and polysilicon grown on the seed layer is essentially identical in the four conditions. Notice that the four devices present different overlays but are not impacted from it. The grain size is also independent to process parameters thanks to the seed layer imposing the initial dimension.

On the other hand, the 1-step integration allows less versatility in the design of the extrinsic base with respect to the 2-step integration. The absence of an independent epitaxy for the base link forces to have the same doping for the whole extrinsic base, evenutally leading to the perimetric capacitance observed in Figure II.21.

2.3 Electrical characterization of the two extrinsic base integrations

The 1-step extrinsic base integration has clear advantages in terms of robustness and simplicity but the advantage from an electrical standpoint still has to be proved.

The analysis of *DC* figures of merit will serve here to identify the possible advantage of the the proposed improved integration. In the following, the principal figures of merit measured on $0.2 \times 5\ \mu m^2$ devices produced with the

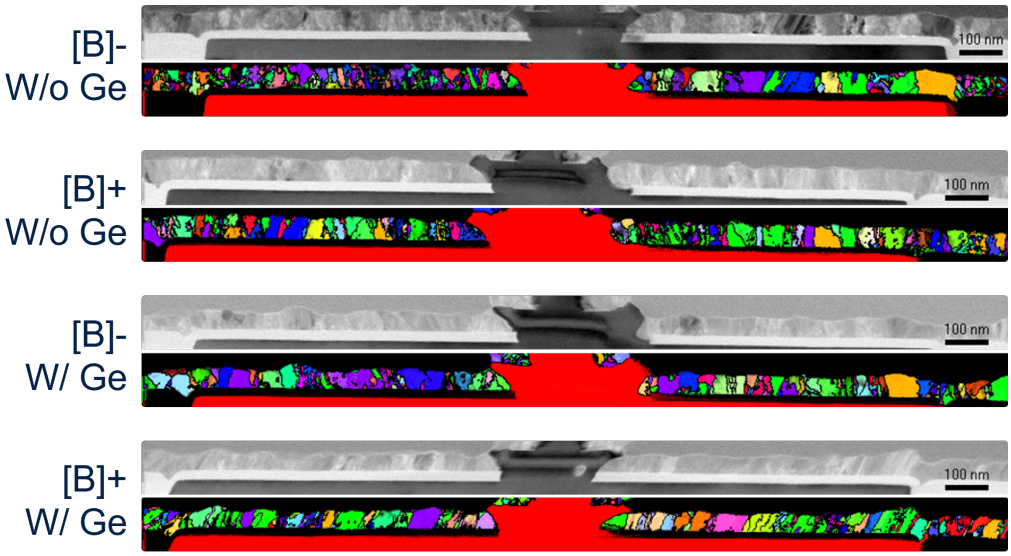

Figure II.23 | TEM cross section and ASTAR grain orientation analysis on 1-step extrinsic base realized with four different combinations of boron and germanium.

two extrinsic base integrations are reported. All the other process parameters are identical.

In this experiment, processes should allow to obtain the same boron concentration in the whole extrinsic base for the two integrations. Due to the reasons presented in Section 2.1.b, doping concentration in the base link of the 2-steps device can not be verified. Reported values for *DC* figures of merit are medians obtained from a minimum of 9 sites measured on at least two wafers.

Table II.4 reports the current-related figures of merit. The 2-step extrinsic base integration is clearly affected by base current leakages and the base ideality factor is heavily impacted. On the 1-step side, no particular flaw is highlighted: currents exhibit good ideality factors, even at low injection. This is a big leap considering that an η_{I_B} below 1.3 is expected for the final EXBIC integration.

The presence of current leakage requires an analysis of its components for better understanding its origins.

Currents measurements have been performed on devices featuring emitter windows with lengths spanning from 1 μm to 2 μm and widths of 170 nm tu 250 nm. The resulting values of perimetric and surfacical current extracted

Table II.4 | Current-related figures of merit measured on two EXBIC HBTs produced with different extrinsic base integrations. $0.2\times5\ \mu m^2$ reference devices.

		2-steps integration	1-step integration
Low injection $V_{BE} = 0.5$ V	I_C (nA)	11	16
	I_B (pA)	98	42
	Gain	1	562
Medium injection $V_{BE} = 0.7$ V	I_C (μA)	22	37
	I_B (nA)	183	15
	Gain	98	2376
High injection $V_{BE} = 0.9$ V	I_C (mA)	12	13
	I_B (μA)	53	18
	Gain	236	680
η	I_B	2.5	1.3
	I_C	1,0	1,1

at three injection levels ($V_{BE} = 0.5$ V, 0.7 V, 0.9 V) and for both integrations are reported in Table II.5. More details on the method used for extraction can be found in Appendix 1.

The 2-steps integration results having a massive contribution from the perimeter at low injection which progressively reduces at higher biases. Many effects can contribute to this phenomenon [1] but the exact origin is hard to tell. Seen the amount of problems with the base link listed in Section 2.1.b, the most accredited hypothesis is that defects are created during the base link epitaxy and introduce deep levels. The cleaning process was blamed at first but leakages persisted even after introducing the optimized process improving uniformity. Recalling the anomalous germanium distribution of the base link remarked in Figure II.15, it is assumed that the epitaxy conditions needed for ensuring selective growth could degrade the interface.

The 1-step integration, on the other hand, has low perimetric components at all three injections, depending mostly on the surface for its base current. Such values indicate healthy devices, where the carriers transit in the intrinsic device is almost unaffected by the extrinsic base, at least in terms of generation and recombination mechanisms.

A TCAD simulation of a 2-step device with [B] = 1e19 at/cm^3 in the base link is reported in Figure II.24 to help understand the presence of strong perimetric components in the base current I_B. Considering arsenic diffusion from

Table II.5 | Perimetric and surfacical component of the base current I_B at various injection levels extracted for both integrations of extrinsic base

(a) | Perimetric

	Injection		
	Low (pA/μm)	Medium (nA/μm)	High (μA/μm)
2-steps	51958	640	5
1-step	-14	-3	-1

(b) | Surfacical

	Injection		
Surfacical	Low (pA/μm)	Medium (nA/μm)	High (μA/μm)
2-steps	-414021	-5222	137
1-step	199	60	23

the emitter and the presence of an undoped capping layer between base and emitter, the depleted zone of the emitter-base junction extends laterally until touching the base link. Combining this with what observed in Figure II.15, it is possible that a grain boundary is present within the emitter-base depletion region of the 2-steps integration. This case is known to introduce intermediate energetic levels inducing junction leakage [41, 8] and can explain the degraded base current ideality factor obtained on the 2-step integration device. Moreover, defects can store charges and bias the junctions [4].

Junction-related parameters are reported in Table II.6.

Considering that the intrinsic base doping profile is identical in the two devices, the fact that highV_{AF} relates to lowV_{AR} indicates that the extrinsic base integration can have an impact on these figures of merit. These results indicate that, if no second-order effects occur, the 2-step integration is more doped close to the emitter side and the 1-step integration on the collector one.

Breakdown occurs at the same voltage at the base-collector junction but the 1-step integration withstands higher voltages on the emitter side. This suggests a similar doping level on the collector side and a more aggressive junction on the emitter side of the 2-steps integration. These results do not match the considerations on the Early voltages and suggest the presence of

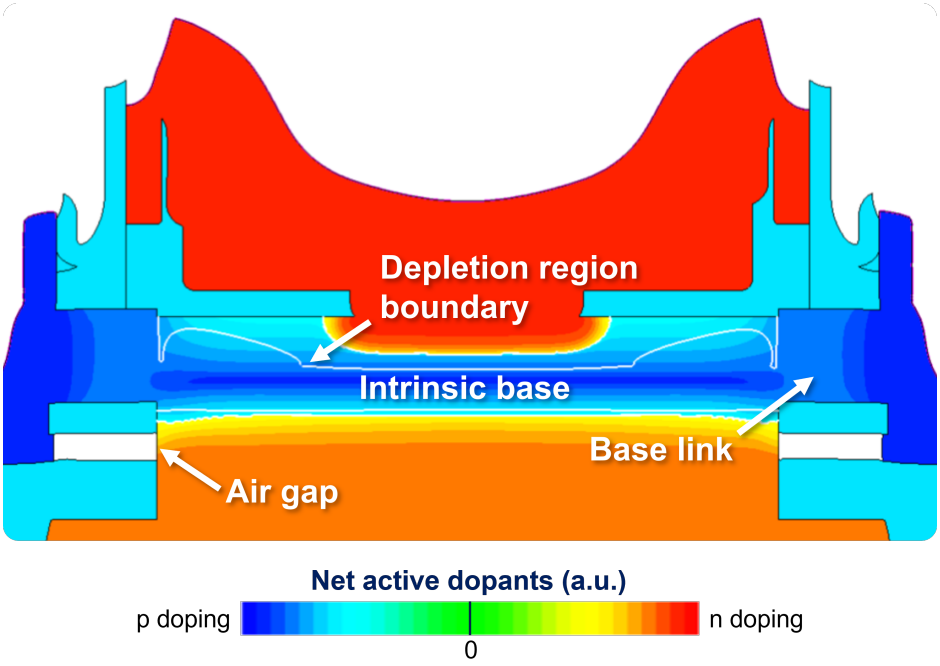

Figure II.24 | TCAD simulation depicting the depletion regions at V_{BE},V_{BC} = 0V in a 2-step extrinsic base integration with [B] = 1e19 at/cm^3 in the base link.

a second-order effect.

Concerning the other measured figures of merit, parasitics are reported in Table II.7.

Details about the extraction of base resistance components will be given in Section 2 Extrinsic base resistance is 40 % lower on the 1-step integration. Considering that boron concentration is identical in the base contact zone of the two integrations, the difference is attributed to the base link. Higher resistance obtained on the 2-steps integration can be linked both to high defectivity and insufficient doping.

Referring to base-collector capacitance C_{BC}, once again the 1-step integration proves its advantage by reducing its value by 42 %. The presence of air gaps in the final structure of the 2-steps integration does not give an advantage with respect to its counterpart. Emitter-base capacitance C_{EB} is almost identical in the two cases, again in contradiction with the previous

Table II.6 | Junction-related figures of merit measured on two HBTs produced with different extrinsic base integrations. $0.2 \times 5\ \mu m^2$ reference devices.

		2-steps integration	1-step integration
V_A	F (V)	82	111
	R (V)	1,8	0,8
BV	CEo (V)	1.7	1.5
	CBo (V)	4.9	4.9
	EBo (V)	1.8	2.3

Table II.7 | Parasitics measured on HBTs produced with different extrinsic base integrations. Capacitance measured on $0.2{\times}5\ \mu m^2$ reference devices. Base resistance extracted from dedicated structures.

		2-steps integration	1-step integration
Base resistance	Intrinsic (kΩ/sq)	6,0	5,4
	Extrinsic (Ω/sq)	757	458
Capacitance	EB (fF)	8,4	8,7
	BC (fF)	8,1	4,7

considerations over the doping profile. The actual doping concentration in the base link is still questioned since higher doping should imply higher capacitance.

Maximum frequencies are reported in Table II.8 for a final evaluation of the extrinsic base integration impact. Similar values of f_T indicate that the vertical doping profile is essentially identical, with a slight difference due to parasitics (cf. Equation (I.7)). The important improvement on R_B and C_{BC} obtained on the 1-step integration offers an improvement of almost 50 GHz in terms of f_{MAX}, proving once again the advantage of using this integration.

Table II.8 | Frequencies measured on two HBTs produced with different extrinsic base integrations. $0.2 \times 5\ \mu m^2$ reference devices, V_{BC} = -0.5 V.

		2-steps integration	1-step integration
Frequency	f_T (GHz)	305	317
	f_{MAX} (GHz)	280	327

In conclusion, analysis of the electric figures of merit proves the clear advantage of producing an EXBIC HBT with a 1-step extrinsic base integration. Section 2 will treat the optimization of the 1-step extrinsic base integration for minimizing the base resistance R_B and improving f_{MAX}.

3 Emitter module

The emitter module of an EXBIC HBT consists in two parts, namely oxide L-spacers fabrication and emitter deposition. Figure II.25 points out its main characteristics.

Many figures of merit depend on the effective emitter window sizing, such as emitter resistance R_E, base-emitter capacitance C_{BE} and the intrinsic/extrinsic ratio of the base resistance components (cf. Section 2). Spacers serve the purpose of tuning the junction sizing independently from the emitter window width and set a compromise on the FOM.

Following base selective epitaxy, L-shaped oxide spacers are realized by a simple deposition-etching cycle. The process is auto-aligned to the emitter window and requires no lithographic steps. After deposition of a thin liner of Tetraethoxysilane (TEOS) and a thicker silicon nitride sacrificial layer, selective plasma etching is used to remove excess nitride and form sacrificial D-spacers. A two-step wet etching removes the uncovered oxide first and the sacrificial nitride after. The effective emitter window, i.e. emitter-base junction size, depends on opening width which in turn is set by the sacrifical nitride layer thickness. As will be shown in Section 4 of Chapter III, emitter spacers also define the different contributions of base intrinsic and extrinsic components.

Emitter deposition is then realized by Chemical Vapour Deposition (CVD) and in-situ doped with arsenic. Deposition is performed after collector and base have been epitaxially grown in the emitter window and oxide L-spacers are realized. Since the emitter deposition process is non selective, a uniform layer of silicon is laid on the wafer. Depending on the underlying material, silicon crystallinity may vary. Indeed, epitaxial growth occurs where the base is uncovered and polysilicon is present elsewhere. Silicon cristallinity has an impact on its resistiviy and on dopants segregation, acting as a secondary effect on emitter resistance.

Interface quality is important for epitaxial growth as it can determine inclusion of impurities or impact cristallinity. Emitter-base interface cleaning requires to offer a perfect surface with no defect whatsoever. The presence of oxide spacers poses a limit to the etching possibilities and the underlying base requires maximum care to avoid any impact on doping profile.

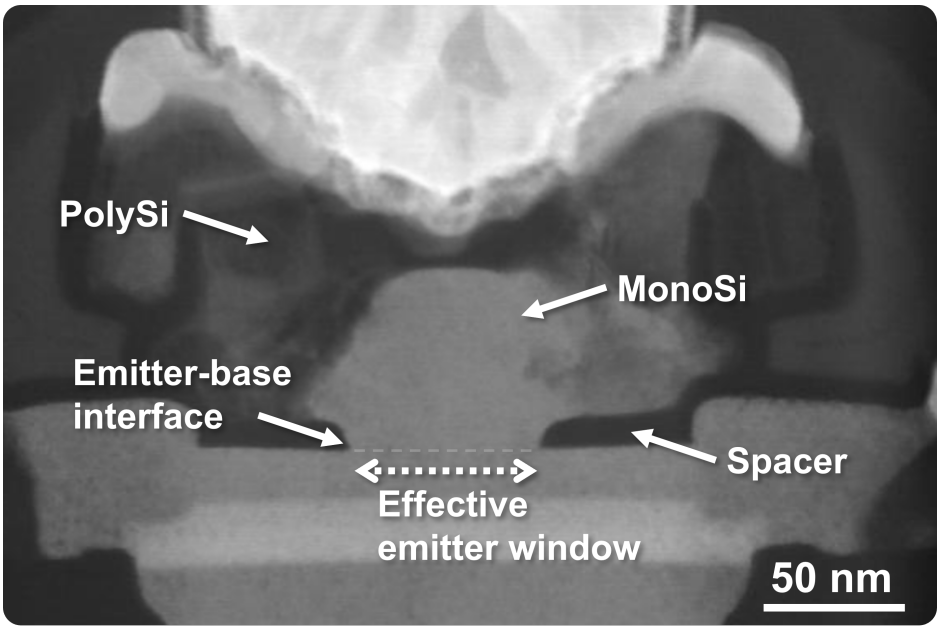

Figure II.25 | TEM cross-section depicting the main characteristics of the emitter in an EXBIC HBT.

3.1 Emitter-base interface cleaning

Cleaning processes are a key step in microelectronics fabrication. As seen in Section 2.1.b, epitaxies can be extremely sensitive to the presence of residual impurities up to the point of avoiding any growth. Emitter deposition is less sensitive to surface state due to its non-selective chemistry, meaning that growth will occur no matter what is present on the surface. TEM cross-sections enhanced with EDX spectroscopy (Figure II.26) highlights the presence of an interfacial oxide layer.

Technologies not based on heterojunctions exploit the presence of a controlled oxide layer at the emitter-base interface to increase current gain by limiting holes injection from the base. As a result, emitter resistance is degraded and a tradeoff is necessary [2, 13]. Advanced devices exploit the presence of SiGe in the base to improve electron injection through bandgap engineering. Devices exhibit improved current gain and would benefit more from the reduction of emitter resistance by the elimination of interfacial oxide [1]. Another well known phenomenon is arsenic segregation at the interface [1], which impacts the resulting profile and potentially limits electrical con-

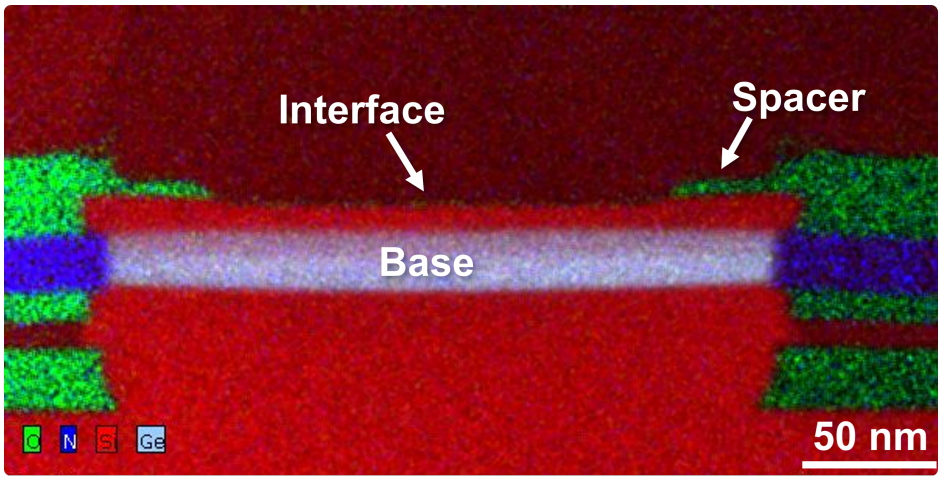

Figure II.26 | TEM + EDX cross-section highlighting the presence of an interface at the emitter-base junction. Picture taken after emitter deposition.

trol over the junction. Even though only a fraction between 25 % and 50 % of segregated arsenic is active [11], the total suppression of this phenomenon is preferable since hardly controllable.

Several cleaning techniques applied to the interface between base and emitter have been tested to minimize impurities at the interface, ensure a correct emitter growth and keep control of the doping profile. The elimination of interfacial impurities should have a beneficial effect on emitter resistance.

Three cleaning processes have been explored: hydrofluoric acid (HF) wet cleaning, fluorine salt gas etching (Siconi) and thermal treatment.

The etching amount of the presented HF and Siconi cleaning processes refer to the thermal silicon oxide etched on a blanket Si wafer, e.g. HF 10 A indicating an hydrofluoric acid cleaning step etching 10 Å of thermal oxide on a non-patterned wafer. Effective etched thickness of non-thermal oxides is normally higher due to their lower density with respect to thermal oxides and can be up to 4 times higher. Temperatures and duration time of the presented thermal treatments refer to the target temperature of the process and duration of wafer exposure, e.g. 700 °C 60 s referring to a 60 s permanence of the wafer in chamber at stable 700 °C. Time for stabilizing temperature is not considered.

Emitter spacers produced before the cleaning step are fundamental for ensuring correct emitter-base junction sizing and their consumption is taken

Table II.9 | Calculated diffusion lengths for a reference concentration of boron $[B] = 1e20\ cm^{-2}$.

Thermal treatment	800 °C 60 s	750 °C 60 s	700 °C 60 s	750 °C 300 s	700 °C 300 s	900 °C 60 s
Diffusion length	8,5 nm	4,1 nm	1,9 nm	9,2 nm	4,2 nm	26,8 nm

into account in this study. For such reason, 10 Å of equivalent etching budget is considered a good value when taking into account that SC1 cleaning should form a layer less than 1 nm thick. HF cleaning has been tested up to 20 Å in order to estimate the possible advantage of this solution, even though the etching budget is too high with respect to the acceptable process for the final device. Cleaning techniques down to 5 Å for HF and 7 Å for Siconi have been tested for minimizing spacers consumption. Different etching budgets have been obtained by varying the reaction time while keeping the other process parameters unvaried. This means that HF dilution and Siconi chamber pressure is identical for the tested etching budgets. HF 10 A is the reference technique for the standard B55X process flow and tested techniques will be considered viable if they improve emitter-base interface cleanliness.

Thermal treatments can cause dopants diffusion and impact the overall doping profile, possibly degrading device performance. Aiming to limit thermal budgets to the minimum, temperatures down to 700 °C have been tested. A maximum temperature of 900 °C has been considered. Wafer treatment times from 60 s up to 300 s have been examined in steady-temperature conditions considering both a minimum time for chamber temperature stability and a maximum time to limit dopant spread. Boron diffusion length has been evaluated considering Fick's second law [35] using the formula:

$$l = \sqrt{Dt} \tag{II.2}$$

where l is the diffusion length, D is boron diffusivity at $1e20\ cm^{-3}$ concentration for the chosen temperature and t is the wafer exposure time. Estimated diffusion lengths are reported in Table II.9. Resulting diffusion values are considered viable if lower than 10 nm and for this reason thermal treatments above 800 °C have not been considered viable due to their impact on boron diffusion in the base. Resulting boron profiles in the base will not be shown due to confidentiality reasons.

3.1.a Interface impurities

Impurity profiles of oxygen, fluorine and carbon measured in a span of 10 nm around the interface are shown in figure II.27. Notice that a higher amount of carbon on the base end of the profile is totally normal. Integrals calculated on the same curves are reported in figure II.28 to give an idea of total amount of impurities; HF 10 A levels are taken as reference.

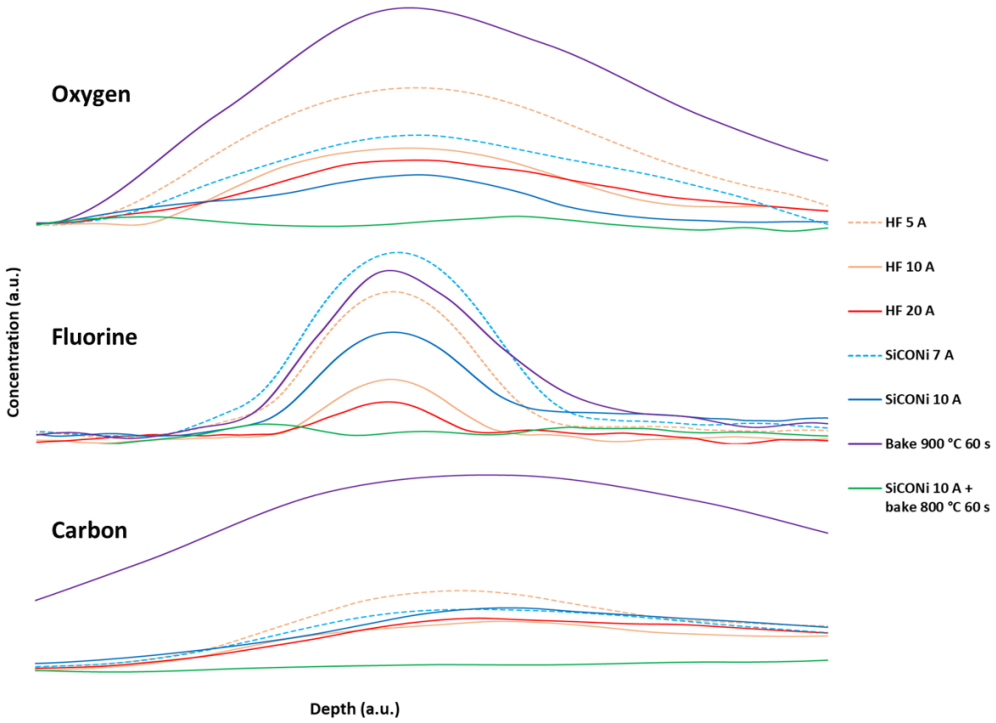

Figure II.27 | TOF-SIMS profiles of oxygen, fluorine and carbon measured in a span of 10 nm around the emitter-base interface. Detection limit of 1e18 at/cm^{-3}.

All the three measured impurities are detected at the interface of a wafer treated with the reference process HF 10 A.

Very high oxygen and fluorine levels are detected on the wafer treated with HF 5 A. Siconi 7 A is better at removing oxygen but leaves by far the highest amount of fluorine among the tested techniques. High levels of

carbon are found in the two cases. These processes underperform HF 10 A in the removal of all the measured species.

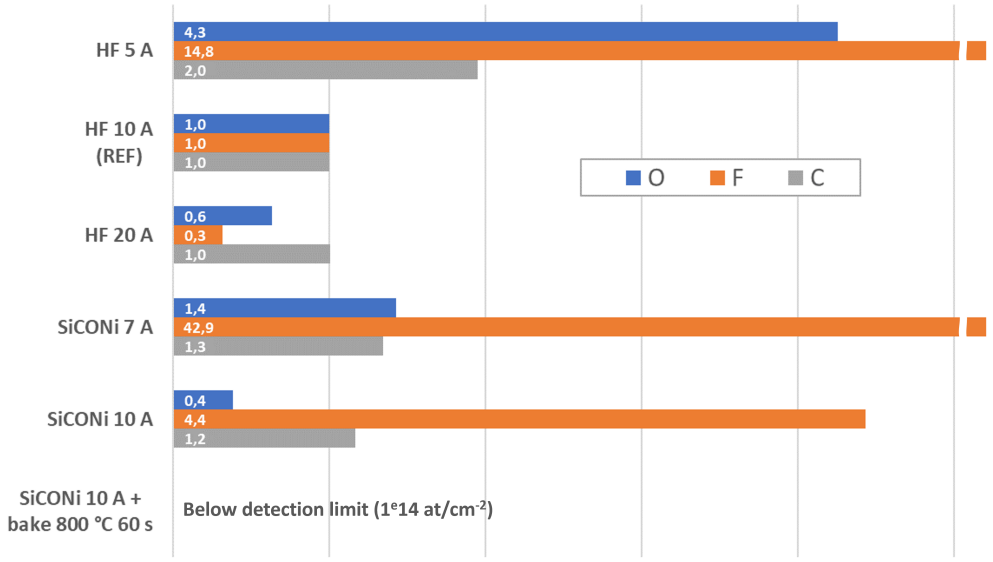

Figure II.28 | Relative total dose of oxygen, fluorine and carbon at the interface. Integration performed on the curves of figure II.27 over the same span. HF 10 A is taken as reference.

Siconi 10 A reduces oxygen by 50 % but leaves almost four times the amount of fluorine with respect to HF 10 A. Carbon levels are also increased by 10 %.

HF 20 A improves oxygen doses by 30 % and fluorine ones by 60 %, with carbon levels unchanged.

The 800 °C 60 s thermal treatment is responsible of the highest level of oxygen and carbon, along with an important fluorine dose. This technique is the least effective among the reported ones.

Siconi 10 A combined with a 800 °C 60 s thermal treatment could reduce all impurity levels below the TOF-SIMS detection limit of 1e18 at/cm^{-3}. Spacer consumption did not increase with respect to what observed with the Siconi 10 A process alone. Among the solutions listed in table II.9 (not reported in figure), 750 °C 300 s bake could obtain similar results. Other combinations could not improve impurity segregation.

Tested HF and Siconi processes do not exhibit proportionality between etching budget and impurity amount at the interface.

TOF-SIMS arsenic profiles obtained in a span of 10 nm around the interface are presented in figure II.29.

Arsenic segregation is observed for most techniques in correspondence to oxygen, fluorine and carbon peaks. The wafer treated with a 800 °C 60 s thermal treatment is affected by the highest level of arsenic at the interface. Measured profiles on wafers treated with HF 10 A, HF 20 A and Siconi 10 A are very close. Similar situation for the two processes at lower etching budget but with a higher arsenic peak. The only wafer not affected by interface segregation is the one treated with Siconi 10 A combined with a 800 °C 60 s thermal treatment.

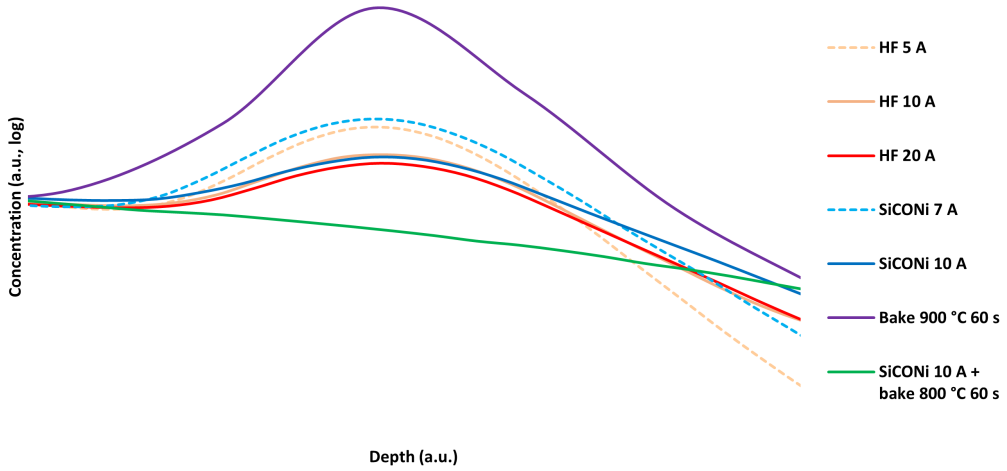

Figure II.29 | TOF-SIMS profiles of arsenic in a span of 10 nm around the emitter-base interface.

Thanks to the expertise and equipments of the Institut Matériaux Microélectronique Nanosciences de Provence (IM2NP), some samples have been studied with High Resolution Transmission Electron Microscopy (HR-TEM). This technique allows to obtain cross-section pictures with atomic-scale resolution. [1]

[1]The author wishes to thank Isabelle Berbezier, Elie Assaf and Luc Favre for these

HR-TEM cross-sections performed on wafers treated with HF 10 A (fig. II.30) highlight the presence of an interfacial layer less than 1 nm thick. Impurities of different type interrupt in some points the otherwise uniform layer. Lattice orientation of the emitter is different from the one observed in the base and some amorphous zones are visible close to the interfacial layer.

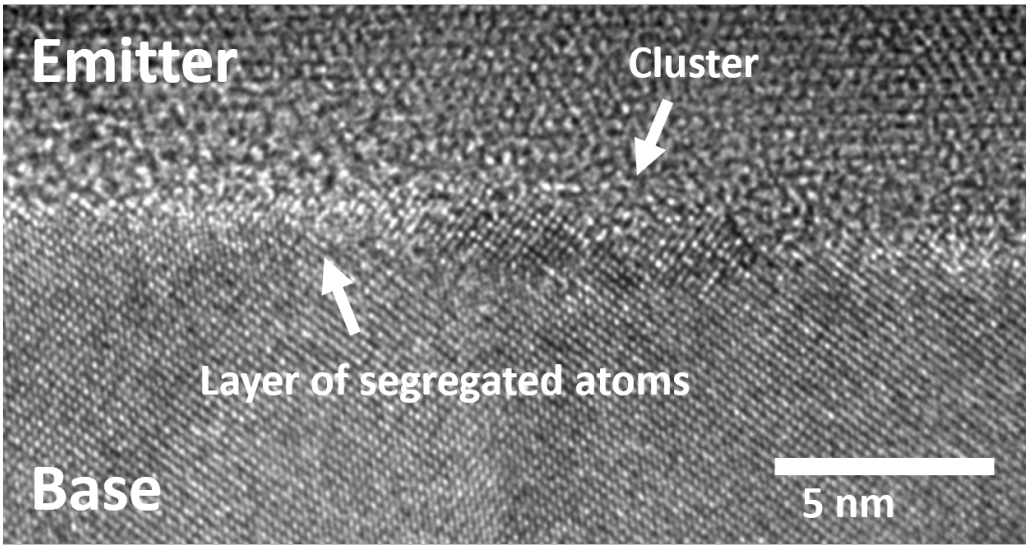

Figure II.30 | HR-TEM of the emitter-base interface of a device treated with HF 10 A. A layer of impurities is present all over, with some scattered clusters interrupting it. Crystalline orientation of the emitter differs from the base.

HR-TEM cross-sections of wafers treated with Siconi 10 A (fig. II.31) present a continuous crystal lattice between base and emitter. No layer of impurities is observed at the interface but a closer look (fig. II.31) highlights small clusters similar to the ones of figure II.30.

Wafers treated with either HF 5 A or Siconi 7 A present way higher residuals with respect to their counterparts at higher etching budgets. Since the quantity of impurities is extremely higher to what observed with other processes, thes solutions are held incapable of correctly removing the 1 nm oxide left from the $NH_4OH + H_2O_2$ reoxidizing clean. The very short process time required for these etching budgets can be too short for a complete reaction

analyses.

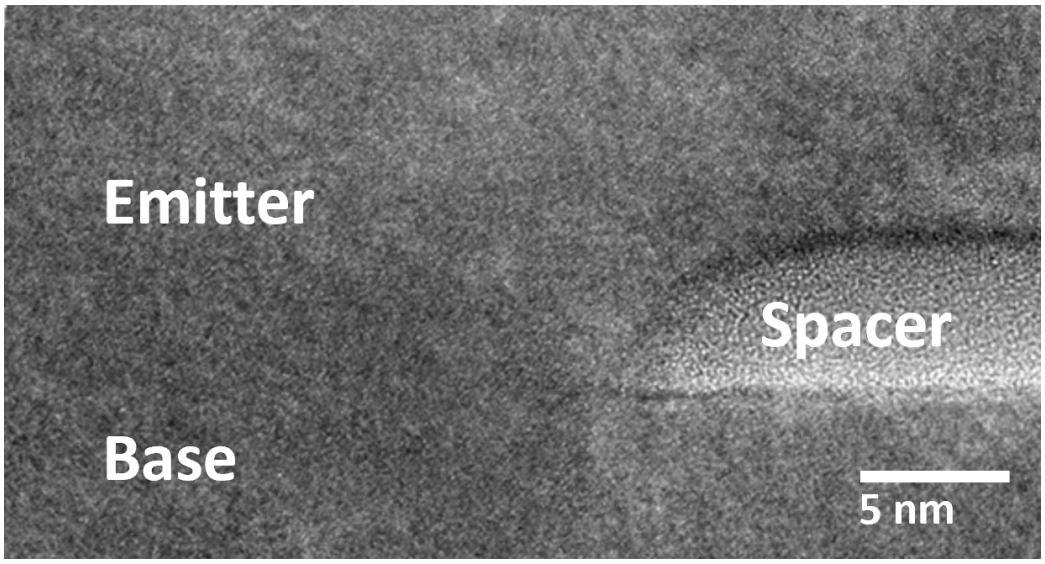

Figure II.31 | HR-TEM of the emitter-base interface of a device treated with Siconi 10 A. Lattice matching between emitter and base is good.

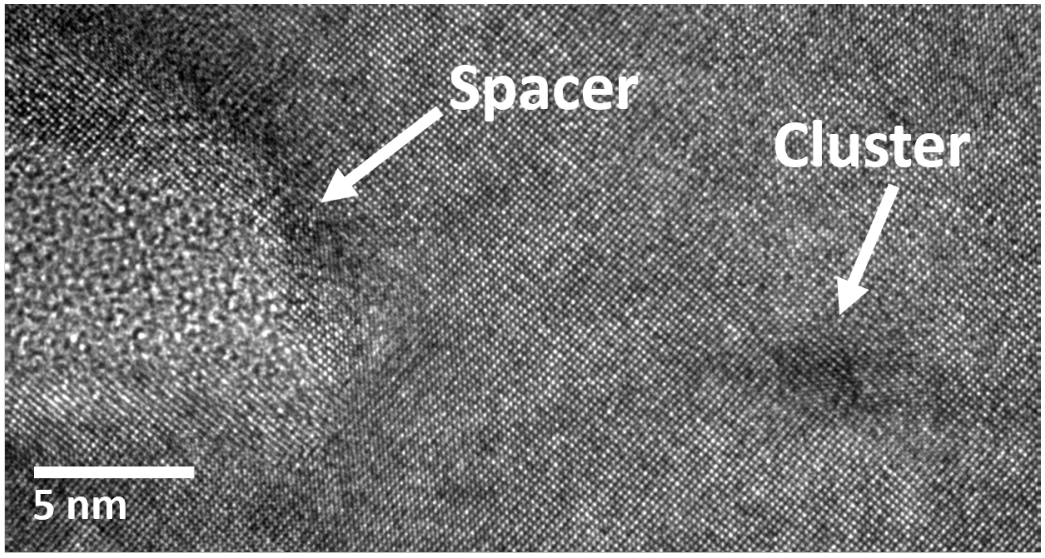

Figure II.32 | Detail of a cluster observed at the emitter-base interface of a device treated with Siconi 10 A.

to occur [62]. Either the oxide layer is not fully removed or the surface is not correctly passivated. Higher dilution and a longer process time could lead to better results with the same etching budget. Even though etching rates are higher on this kind of oxide, the capacity of entirely removing the impurity layer is still questioned.

Wafers treated with the reference HF 10 A cleaning process are affected by interface segregation of all the impurities. The uniform layer observed in cross sections could induce to think that the etching budget is still not sufficient to remove the initial oxide. Observing cross sections obtained on Siconi 10 A-treated wafers, it is however clear that 10 Å of etching budget is enough and a different mechanism is acting. Indeed, HF 20 A reduces oxygen impurities with respect to HF 10 A by only 30 % in spite of the doubled etching budget. Assuming that HF 10 A and HF 20 A-treated wafers are both perfectly cleansed prior to atmosphere exposure, the difference in impurities is explained with the transit from F-terminated to H-terminated surface at the increase of reaction time, which is known to decrease surface reoxidation [62]. The clear interfacial layer observed in figure II.30 is therefore attributed to surface reoxidation during the passage from the wet cleaning tool to the epitaxy chamber.

Both the HR-TEM cross sections highlight the presence of defect clusters. The fact that Siconi 10 A-treated wafers do not display a continuous layer at the interface proves that said clusters contain all the three measured impurities. In the case of HF-treated wafers, the reoxidation layer surrounds the clusters, meaning that they protected the surface from reacting with atmospheric oxygen and proving that clusters are adsorbed to the silicon surface. Remembering that Siconi is performed in-situ with respect to the epitaxy, the presence of defects on Siconi-treated wafers proves that they must have been adsorbed in a previous processing step, probably during spacers formation. This is further validated by the fact that all these processes have similar carbon levels regardless of chemistry or etching budget.

The 800 °C 60 s thermal treatment alone is totally ineffective at removing impurities. The oxide generated by the SC1 reoxidizing clean is still present on the surface at least in part. Elevated presence of fluorine and carbon shows that these elements are included in the oxide layer covering the wafer regardless of any HF or Siconi process.

The addition of a 800 °C 60 s thermal treatment to a Siconi 10 A cleaning demonstrated impurities reduction below TOF-SIMS detection limit, ideally representing a completely clean interface. The hypothesis of carbon contamination from the surface is compatible with what observed. Carbon particles

adsorbed from the atmosphere have passivated the oxide surface limiting Siconi reaction in some spots and the application of a correct thermal budget has led to desorption of the whole impurity cluster. Since the process is performed in non-oxidizing atmosphere, surface is perfectly clean and no impurity is integrated during emitter deposition. The described mechanism recalls some procedures documented in literature where a very thin passivation layer is generated by design and evaporated at will for obtaining an ultra pure silicon surface [33]. Dose integral calculated on the whole carbon profile of the device shows 9 % less carbon with respect to the wafer treated with a simple Siconi 10 A, confirming that interfacial carbon is not due to anomalous diffusion from the base. Exact origin of the impurity clusters is not clear and requires further investigation.

Regarding arsenic trapping, higher etching budgets imply smaller segregation but there is no strict correlation between the peak arsenic levels and those of the other impurities. Remarkably, the measured arsenic profiles on the HF 20 A-treated wafer are not far from what observed at 10 Å of etching budget. The fact that HF 10 A and Siconi 10 A lead to very close profiles regardless of the interfacial impurities is also interesting. These results suggest that arsenic segregation occurs mostly in correspondence to clusters and is not influenced by surface reoxidation on this scale. The arsenic profile measured on the wafer treated with Siconi 10 A + 800 °C 60 s thermal treatment however confirms that impurity segregation is related to arsenic trapping. The diffusion slope into the base is qualitatively smaller for profiles with higher peaks and Siconi-treated wafers diffuse more than their HF counterparts. If defects can act as trapping sites for arsenic atoms, they also constitute a diffusion barrier. The binding mechanism is so far unknown and requires specific investigation. The impact on electric figures of merit could be not negligible due to different levels of dopant activation. The doping profile of the base might need some adjustments to compensate different doping activations and diffusion slopes.

3.1.b Emitter resistance measurements

Based on the conclusions obtained over the previous results (Section 3.1.a), the most interesting cleaning processes have been selected for emitter resistance measurement. Chosen processes are: HF 10 A, Siconi 10 A and Siconi 10 A + 800 °C 60 s. Average measured values and standard deviations are listed in table II.10.

Tendencies on resistance values are in accordance with the measured levels

of residual oxygen oxide but not proportional. Variance is affected in the same way. Siconi 10 A + 800 °C 60 s is the best cleaning process among the tested ones.

Table II.10 | Average and standard deviation of emitter resistances measured on devices with different emitter-base interface cleaning processes. Processes to measure have been selected following the conclusions obtained from TOF-SIMS and HR-TEM analyses. $0.2 \times 5\ \mu m^2$ reference devices.

Cleaning technique	HF 10 A	Siconi 10 A	Siconi 10 A + 800 °C 60 s
Average (Ω)	4,55	2,91	1,75
Sigma (Ω)	1,89	1,21	0,34

The presence of an interfacial oxygen layer clearly impacts emitter crystallization of HF-treated wafers during the CVD process. If the layer is thin enough to be comprised in the crystalline strained transition layer [36], the emitter crystallizes adapting to the strain as observed in figure II.30. Variations in the layer thickness could imply different orientations of the emitter crystal lattice or result in the formation of polysilicon. High resistance values are related both to interfacial impurities and to lattice mismatch in the emitter. High variance in the measured values is related to the variable thickness of interfacial layer as a function of the exposure time to air and consequent crystalline orientation. In accordance with these observations, Siconi 10 A-treated wafers reduce emitter resistance by 36 %. Even if the interface is not perfectly cleansed, this result alone proves the advantage of Siconi cleaning. Resistance variance is still relatively high, and can be linked to the presence of carbon clusters. A perfectly clean surface is the best option possible among hte tested ones. Wafers treated with a Siconi 10 A in combination with a 800 °C 60 s thermal treatment reduced emitter resistance by 59 % and its variance by 82 % with respect to HF 10 A.

The available literature [56] indicates that lower impurity levels imply reduced 1/f noise. A Siconi 10 A + 800 °C 60 s cleaning process is therefore the best suitable for *RF* transistor operation. Noise measurements are however still needed to quantify the impact of the tested techniques.

4 Architecture review conclusion

The development process presented in this chapter was meant to address the limitations of the preliminary EXBIC architecture.

Started in May 2019, the architecture review process gave its last results at the beginning of 2022 when all the presented improvements have been integrated together on one device: at this point the Go To EXBIC architecture was defined as the target EXBIC architecture for the B55X. This integration differs from the previous one by implementing a single SSTI design combined with a 1-step extrinsic base integration.

Figure II.33 compares the morphology of the preliminary EXBIC architecture and the Go To EXBIC architecture.

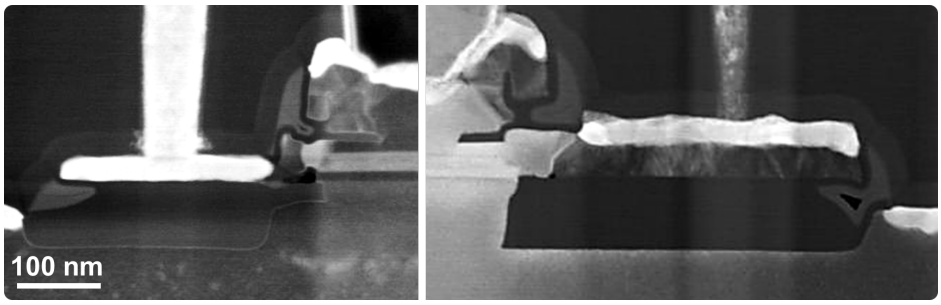

Figure II.33 | TEM cross-sections comparing the preliminary EXBIC architecture with the Go To EXBIC architecture.

Resuming the developments presented in this chapter, the problem solving process focused on the following aspects:

Collector Carbon plus phosphorus co-implantations have been optimized for defects suppression. Studies on the amorphization and recrystallization process due to ion implantation served to understand the mechanisms leading to device malfunctioning.

A new SSTI design has been conceived focusing on a more robust architecture. The new integration avoids problems related to overlay mismatch and step height.

Extrinsic base The original integration based on two epitaxies has been replaced by a simpler one featuring a single epitaxy process. The contact between intrinsic and extrinsic base has been improved thanks to a study on

the cleaning techniques. The new integration makes an economy of one step during stack deposition and two steps in the extrinsic base fabrication process.

Emitter The emitter has been improved thanks to a study on the emitter-base interface cleaning. The new process avoids the presence of impurities at the interface, with no arsenic segregation as a consequence. The total emitter resitance is reduced by 59 % with respect to the reference process.

Far from being a linear development process, the introduction of these features has been accompanied by the optimization of many aspects of the process integration which are very important for reaching the final goal. Notice that this work has been carried out in collaboration with many people, each one expert in a particular domain of device integration.

Specific photolithographic processes have been developed. The relatively small SSTI sizing demanded to study the best way for ensuring a correct shape. The very deep emitter window required for the single-SSTI integration led to the development of a specific process capable of etching a straight opening over all the different layers present in the stack.

Five different epitaxy processes have been studied for this integration, improving repeatability and process time for each one. The new SSTI design required to redevelop the collector epitaxy in accordance to the new needs. A broad range of dopant distributions, shapes and chemistries have been tested for reaching optimal results.

New characterization techniques have been tested and introduced to improve monitoring both in and outside the production line, offering valuable indications of the weak points.

Each process (also CMP, depositions, etc.) has been investigated both in terms of repeatability an reliability. Particular choices have been made in the scope of future volume production.

Figure II.34 shows the performance progression in terms of f_T and f_{MAX} in comparison with the DPSA-SEG HBT integrated in the STMicroelectronics' BiCMOS055 technology and the target for the EXBIC HBT to integrate in the next BiCMOS platform. Reported points relate to the best performance obtained on one or more process splits measured during the corresponding month/year. Performance improved all along the progressive implementation of refined processes and new device designs. Thanks to the

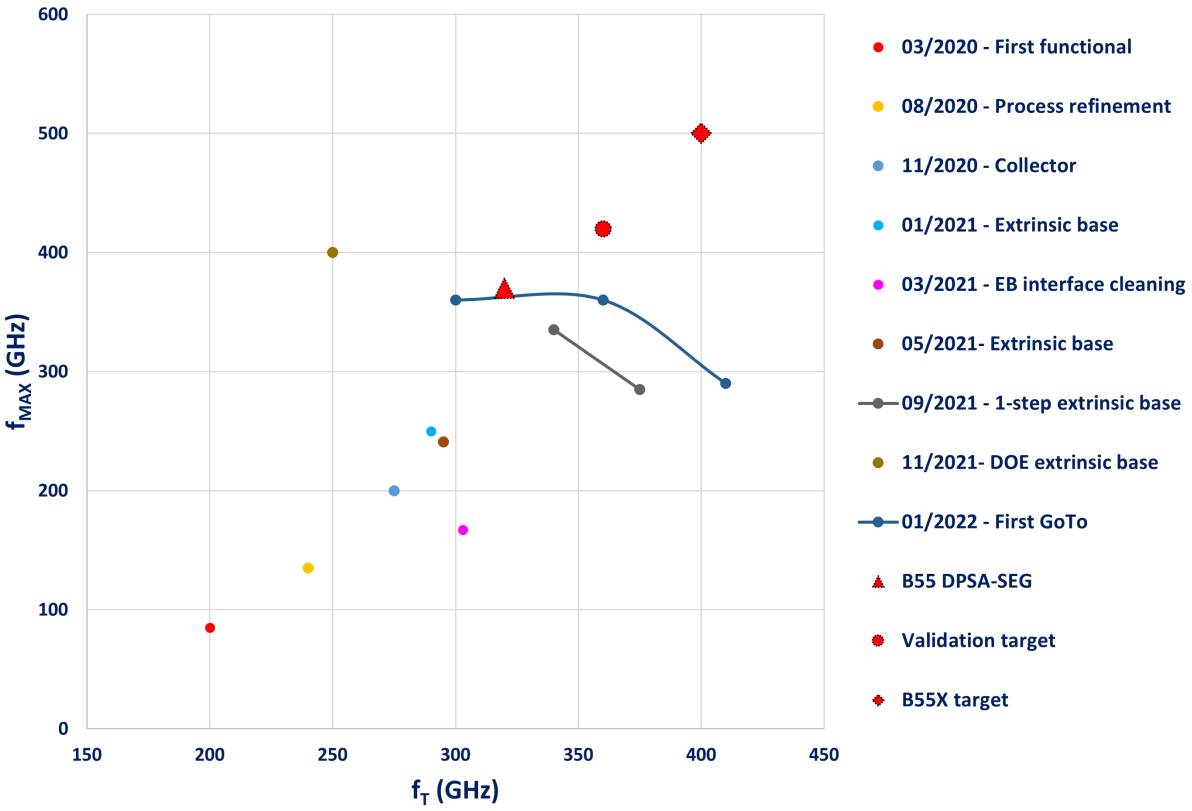

Figure II.34 | f_T and f_{MAX} progression on the lots producing during the development of the Go To EXBIC architecture. $0.2 \times 5\ \mu m^2$ reference devices.

presence of process splits, the possibility to tune the device performance has been demonstrated on the last lots produced.

Referring to the studies presented in this chapter, some milestones can be defined :

03/2021 First studies on emitter-base interface cleaning

09/2021 First demonstration of the 1-step extrinsic base integration

01/2022 Device integrating a complete Go To EXBIC architecture with refined fabrication processes; doping profiles not yet optimized

The final results demonstrated the capability of the EXBIC architecture to compete with what achieved on the DPSA-SEG one. Far from being optimized, the new architecture still requires to improve in order to reach the targeted 400/500 GHz f_T/f_{max} for the BiCMOS055X technology. Chapter III will explain the optimization process started to fill the gap.

Chapter III

Electrical optimization

This chapter presents the developments leading to the optimization of the Go To EXBIC architecture.

The problem solving process presented in Chapter II allowed to equal the performances obtained on B55 Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) but are still below the values targeted for the BiCMOS055X technology. A fine work of tuning is required to tweak all the device components to obtain a perfect synergy.

The results of all these modifications aim to finally achieve the target performance of f_T/f_{max} = 400/500 GHz with BV_{CEo} = 1.35 V.

Results of Chapter II allowed to define the new Go To EXBIC architecture by addressing the limitations observed on the first devices. Performance improvement followed the resolution of critical limitations found on the preliminary EXBIC architecture but some work is still to do. The first lot integrating GoTo EXBIC transistors, last one produced within the architecture optimization phase, featured f_T/f_{max} of 360/360 GHz, way far from the target performance of 400/500 GHz for the BiCMOS055X technology. There is fortunately still a good amount of work to do for obtaining an optimized device.

Figure III.1 lists the modules concerned by the optimization process and lists main scope for each one.

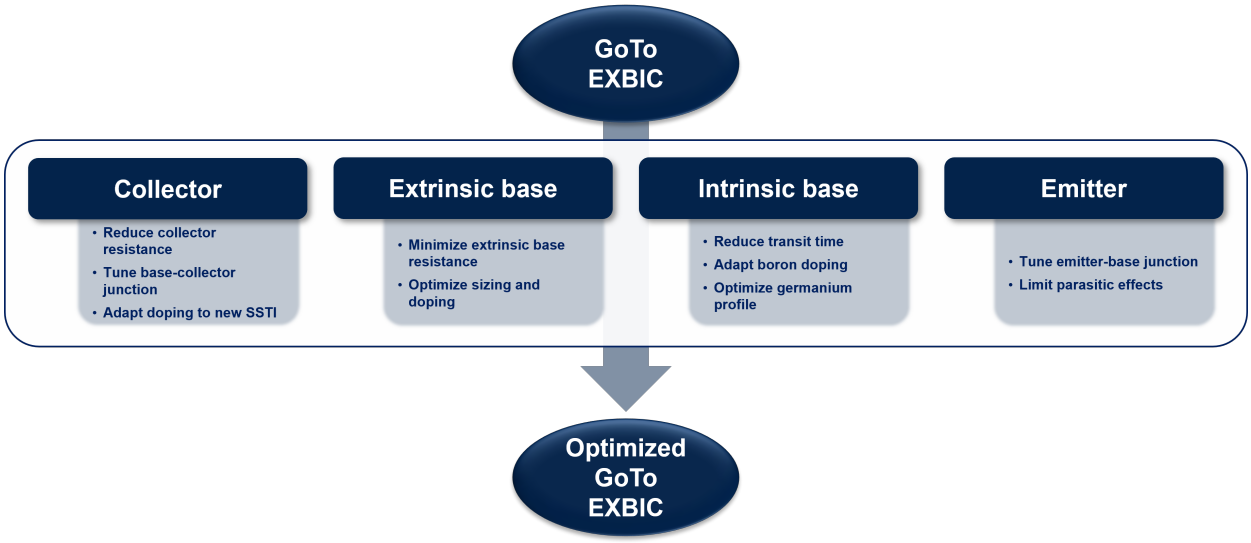

Figure III.1 | Modules impacted by the architecture optimization process and relative objectives.

Studies on ion-implantation-induced defects in the collector gave some clear indications on the doping strategy in order to avoid reliability issues, but no specific study has been conducted on the other figures of merit. Both considerations on collector resistance R_C minimization and base-collector junction tuning have been conducted. The introduction of a single-shaped SSTI also redefined the concept behind the collector integration, requiring to design a specific doping strategy.

The 1-step extrinsic base integration solved many problems of robustness and reduced the base resistance. Some parameters are however still to address, such as doping level, total thickness and others. Section 2 shows the results of such investigation in the scope of minimizing extrinsic base resistance R_{sBx}.

Heart of the device, the intrinsic base has not been touched yet. The many parameters linked to its design require a deep understanding of the underlying principles followed by a good knowledge on the possibilities offered by the epitaxy process. Its modification is tricky because it requires all the other components to adapt accordingly in order to express the best results. Section 3 details studies performed both on boron doping and germanium profile in the base.

On the emitter side, spacers have not been optimized yet. Knowing the importance of the emitter-base junction, the effective emitter window width can have profound effects. Section 4 investigates the relationship between emitter spacers width and performance.

1 Collector module

The collector structure has been defined and improved during the problem solving phase.

A Super Shallow Trench Isolation (SSTI) is obtained from a single 50-nm-deep trench in order to minimize the extrinsic component of the base-collector capacitance C_{BC}. A carbon plus phosphorus co-implantation is used to dope the substrate. Total surface amorphization is required for avoiding the formation of implantation-induced defects during recrystallization. As seen in Section 1.2.b of Chapter II, the single-trench SSTI structure forbids the use of a standard SIC between the trenches for tuning the base-collector junction and another solution is required.

Figure III.2 shows the two main functions of the collector implantation in this integration. Collector resistance R_C reduction is achieved by correctly designing the collector plus phosphorus implantation in order to minimize collector resistivity. Base-collector junction tuning is achieved by controlling phosphorus diffusion from the substrate up through the epitaxial collector.

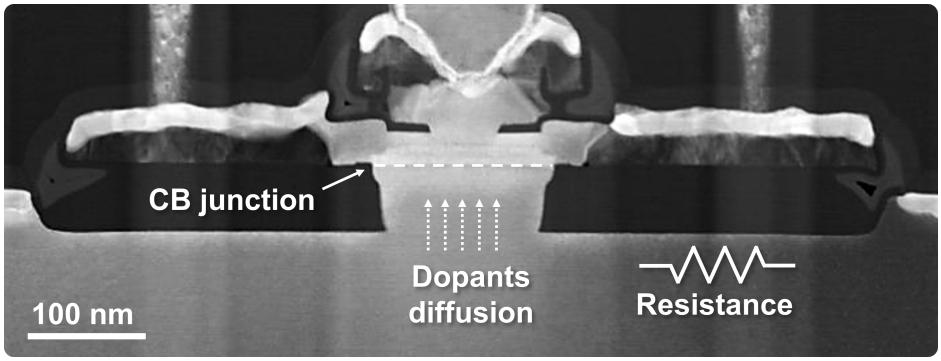

Figure III.2 | TEM cross-section depicting the two main contribution of collector implantation on device characteristics.

The collector resistance of an HBT depends from its complex structure and requires an adapted model.

Figure III.3 sketches the three principal components of the collector resistance on a Go To EXBIC architecture, excluding contact resistance.

Sinker resistance represents the vertical component below the contacts. Its value in the EXBIC HBT architecture is defined by the SSTI depth and

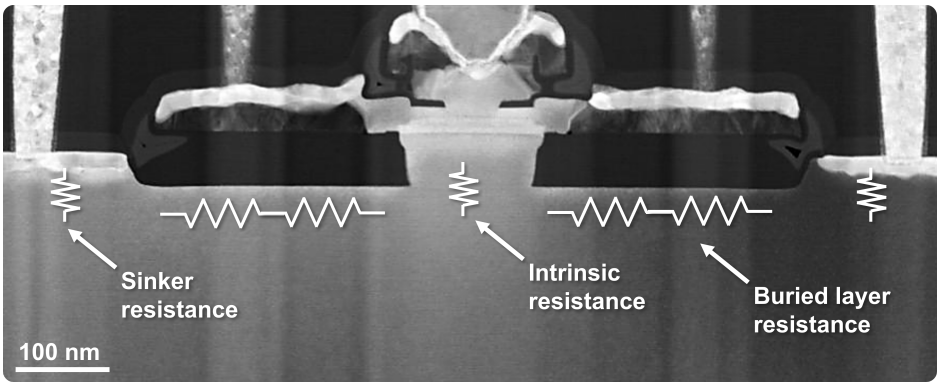

Figure III.3 | Collector resistance R_C components sketched on a TEM cross-section.

the doping distribution below the contacts. Specific ion implantations are dedicated to its minimization and are not investigated in this study.

The buried layer component makes the most of the collector resistance. Its value depends on the width of the SSTI and the doping profile below it. Even if collector doping could have an impact on the extrinsic component of base-collector capacitance C_{BC}[32], SSTI is thick enough to make it negligible with respect to the junction (intrinsic) capacitance. Its minimization requires a compromise with the extrinsic component of the base-collector capacitance C_{BC}. The SSTI depth has however been studied to minimize the interdependence between these two factors in this integration [5]. Notice that this component is called "buried layer" regardless of the actual collector integration.

The intrinsic component of the collector resistance is related to the portion comprised beween the resulting SSTI trenches and not included in the base-collector depletion zone. It follows that its value depends on SSTI depth, doping distribution and space between the SSTIs. As a consequence, its minimization depends on the many factors related to the base-collector junction such as intrinsic base-collector capacitance C_{BC} and breakdown voltages (cf. Section 2). The relative value of this component is however small compared to all the others and it will be considered as a secondary factor when designing the junction, even if it can impact the collector transit time τ_C.

The reference contact layout used in this study features collector contacts on both sides of the device. This solution is one among many others (cf. [6]) which allows to behalf both sinker and horizontal components by simply dou-

bling the contacts.

The first part of this section presents the studies focusing on collector resistance minimization.

The second part of this section explains the strategy adopted for tuning the base-collector junction and how it has been optimized.

The third part presents the effects due to variability of the epitaxial collector thickness.

Eventual considerations on the architecture limitations are presented and future studies defined.

1.1 Resistance reduction

Collector resistance R_C is the result of many factors determining how electrons flow through the substrate towards collector contacts.

Once the SSTI thickness has been set to 50 nm, the only way of reducing the buried layer resistance is to tune the carbon plus phosphorus co-implantation.

Plain wafer testing is used to better understand carbon plus phosphorus co-implantations and how the collector of an EXBIC HBT could be improved accordingly. Such work is also part of a deep study on the underlying phenomena of this doping technique presented by Dumas [18].

Results are successively combined with the conclusions of Section 1.1 on the defect-inducing mechanisms to define the best doping conditions for the integration of a complete device.

1.1.a Non-product wafer testing

A first round of testing on Non-Product (NP) wafers has been used to define the most interesting conditions for R_C reduction. Phosphorus doses d_P span from 1/5 up to 4 times the carbon dose d_C and carbon energies are either the reference e_C or twice. Conditions have been chosen regardless to the defect generation phenomena observed in Section 1.1. Wafers have been treated in an oven with multiple thermal treatments emulating the thermal budget seen by a fully-processed wafer. Thermally-induced phenomena such as recrystallization, dopant diffusion and defect evolution are as close as possible to what could be observed on a device.

Sheet resistances measured with the four-point probe method are plotted in Figure III.4. Standard deviation of the obtained values is below 1%. More details on the meaning of this figure of merit and how it depends on material characteristics are given in Appendix 2.

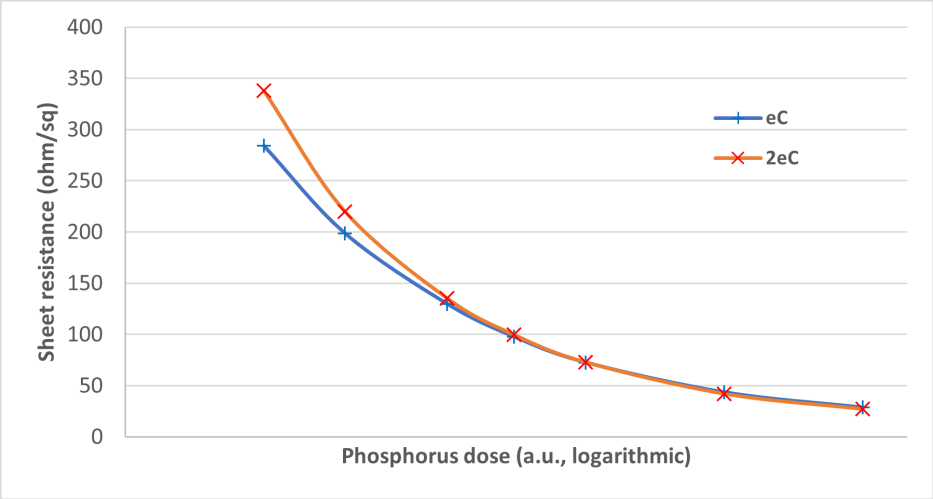

Figure III.4 | Sheet resistances measured on plain sheet wafers implanted with different carbon energies and phosphorus doses.

Measured resistances naturally decrease for increasing doses. The observed saturation at high phosphorus doses ($d_P \geq d_C$) is a normal effect at high-dose doping[60], posing a final limit to the achievable improvement of collector resistance R_C in these conditions. Low phosphorus doses are the ones showing a bigger difference depending on carbon energy, while for higher doses the discrepancy is minimal. Carbon pumping effect is related to presence of interstitial defects and can generate quite different outcomes on phosphorus diffusion depending on its positioning and the phosphorus/carbon dose ratio[16].

Figure III.5 displays phosphorus profiles obtained by Time Of Flight - Secondary Ion Mass Spectroscopy (TOF-SIMS) of four representative conditions which could help to better understand the measured resistances.

Comparing the profiles obtained at low phosphorus dose $d_C/5$, carbon positioning appears critical. Recalling what observed in Figure II.6, such conditions generate a buried amorphous layer inducing zipline dislocations after recrystallization. For low phosphorus doses, positioning of the amorphous layer will depend on carbon implantation conditions[14]. In accordance

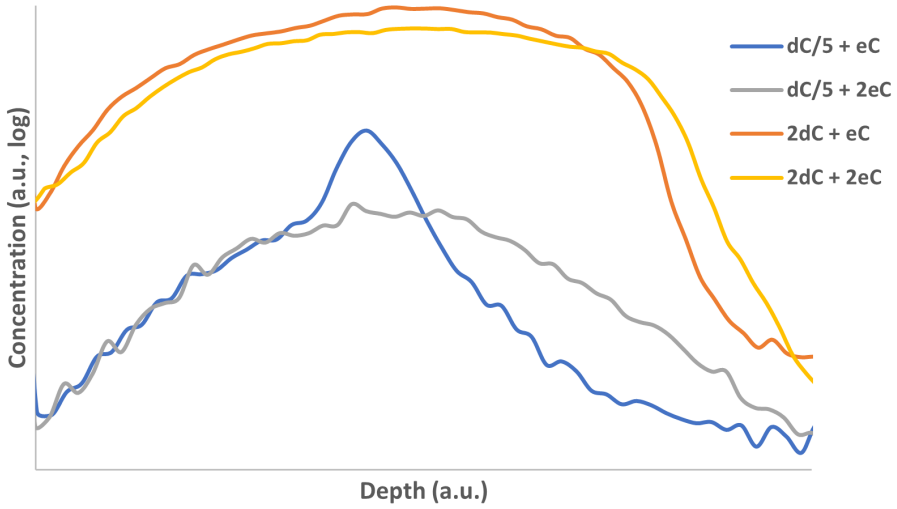

Figure III.5 | Phosphorus distributions obtained by TOF-SIMS on wafers implanted and annealed. Variation of relative phosphorus dose and carbon energy.

with carbon-related phenomena[17], an important rearrangement on deeper half of the phosphorus distribution is observed when combined with a carbon implantation performed at reference energy e_C. A doubled carbon energy $2e_C$ avoids Transient Enhanced Diffusion (TED)-induced long distribution tails but does not push phosphorus closer to the surface. It results that carbon energy has an important effect on low-dose phosphorus profiles due to defects interactions during recrystallization. The difference in measured resistance can therefore be explained considering how the doping profile can affect sheet resistivity both in terms of concentration and depth[42].

$2d_C$ profiles show that an increasing phosphorus dose minimizes the impact of carbon implantation energy on dopant distribution. Doses above $d_C/2$ are capable of totally amorphizing the substrate surface without defect formation during recrystallization (II.6). This means that carbon will mostly act on phosphorus distribution by regulating TED-related effects. The two curves tend to a rectangular shape, indicating that TED-enhanced diffusion occurs within a range while being suppressed after a certain limit. Considering the underlying principles of Transient Enhanced Diffusion[58], we can assume that the proportion between carbon concentration and implantation-induced interstitials modulates phosphorus diffusivity. Since the d_P/d_C ratio

can go up to four, we can easily state that TED will be effective at least around the phosphorus peak. Thanks to its positioning, carbon will be effective at the distribution end, where End Of Range (EOR) defects will be suppressed along with interstitials. It follows that carbon implantation energy has a limited impact on substrate resistance in these conditions. Higher carbon doses could have a different impact, containing phosphorous close to the surface.

1.1.b Device testing

Results obtained during NP wafer testing have to be confirmed on patterned wafers. Standard devices produced with a full process flow have been implanted with the best conditions for collector resistance R_C minimization. For each implantation condition, values are extracted on three different collector geometries with the method detailed in Appendix 3. Appendix 3 explains how these values are obtained from collector resistance measurements. Table III.1 compares sheet resistances measured on plain sheet wafers at given conditions and the corresponding buried layer sheet resistances R_{sBL} extracted on devices. The saturating tendency of resistivity for high doping doses is confirmed. Values on patterned wafers are however up to 50% higher than their full sheet counterpart. Considering the positioning of the phosphorus projected range $R_{p,P}$, more than one third of the total dose is expected to be lost in the SSTI during implantation. This value roughly matches the offset in resistivity, explaining why higher values are measured.

In conclusion, higher phosphorus doses are capable of drastically reducing the buried layer resistance but a saturating tendency is observed. Phosphorus doses above two times the carbon reference dose allow resistance values small enough for being acceptable. These conditions are compatible with the rules defined in Section 1 for avoiding recrystallization-induced defects.

1.2 Base-collector junction tuning

As seen in Section 1.2 of Chapter II, the single-trench SSTI design requires to develop a specific concept for tuning the base-collector junction.

The simplest solution is to exploit the collector implantations used for reducing buried layer resistance to also adjust junction behavior. Resistance saturation observed at high phosphorus doses (cf. Section 1.1.b) allows to tune the junction by varying doping without consistently impacting parasitics.

Table III.1 | Resistivity measured on NP and patterned wafers implanted with different carbon energies and phosphorus doses.

Resistivity measured on NP and patterned wafers implanted with different carbon energies and phosphorus doses. Values are in Ω/sq.

(a) | Plain wafer

		Phosphorus dose d_P			
		$d_C/2$	d_C	$2d_C$	$4d_C$
Carbon energy	e_C	130	73	43	28
	$2e_C$	135	73	42	27

(b) | Patterned wafer

		Phosphorus dose d_P			
		$d_C/2$	d_C	$2d_C$	$4d_C$
Carbon energy	e_C	190	100	65	41
	$2e_C$	/	/	63	40

Since the junction depends on the doping profile in the base as well, a reference base profile is chosen for a first testing cycle. Obtained results will eventually serve to understand how to improve the base profile and eventually start another optimization loop on the collector.

The same combinations of carbon and phosphorus ion implantations tested for collector resistance reduction have been reproduced for evaluating the behavior of the base-collector junction.

On a reference $0.2 \times 5\mu m^2$, a phosphorus dose spanning from half the reference carbon dose up to four times is combined with a carbon implantation at reference energy or two times it. DC parameters have been tested on at least 3 wafers per split on 9 different sites each; medians are reported. RF parameters have been measured on the best wafer among each split chosen following DC results.

Currents and related parameters are reported in Table III.2.

All splits behave correctly, with collector ideality factors η_{I_C} below 1.1 and base ideality factors η_{I_B} aligned with the previous results obtained with the 1-step extrinsic base integration (cf. Chapter II Section 2.3). Some collector current leakages are remarked for the $4d_C$ splits, likely due to a too much aggressive collector bringing the base close to pinch-off. Notice that

Table III.2 | Currents and related parameters measured on wafers implanted with various phosphorus doses and carbon energies. $0.2\times5\ \mu m^2$ reference devices.

	Carbon energy	e_C				$2e_C$	
	Phosphorus dose	$d_C/2$	d_C	$2d_C$	$4d_C$	$2d_C$	$4d_C$
Low injection $V_{BE} = 0.5$ V	I_C (nA)	13	13	13	21	14	21
	I_B (pA)	19	16	16	18	19	17
	Gain	803	930	1041	1435	1180	1489
Medium injection $V_{BE} = 0.7$ V	I_C (μA)	23	24	25	29	24	29
	I_B (nA)	8	8	7	7	7	7
	Gain	2869	3294	3445	4338	3505	3906
High injection $V_{BE} = 0.9$ V	I_C (mA)	3,1	3,9	6,9	7,8	7	7,7
	I_B (μA)	25	18	6	6	6	6
	Gain	121	208	1213	1231	1255	1217
η	I_B	1,3	1,3	1,3	1,3	1,3	1,3
	I_C	1,03	1,03	1,03	1,09	1,03	1,08

the single-trench SSTI integration avoids the functionality issues observed with the $d_C/2$ phosphorus split in Section 1.1.

At each injection level, collector currents increase with phosphorus dose. Increased carbon energy improves gain at $2d_C$ dopant concentration while degrades it at $4d_C$. It has however a limited impact on currents in accordance with the minimum shift on doping profiles observed in Figure III.5. Devices implanted with higher phosphorus doses exhibit increased collector currents thanks to the larger depletion region extending deeper into the base, limiting electron recombination (cf. Equation (I.1a)). Equation (I.1b) states that base current should be dependent on the emitter only, but it unexpectedly decreases at high phosphorus doses when the device is polarized at high injection. This effect could actually be linked to the impact that high current can have on junctions: if the mobile carriers concentration is comparable with the fixed ions one, junctions might be impacted as in the Kirk effect. Another possibility is that the total depletion approximation used to derive current equations is not valid in these conditions. It is also possible that, due to the high implantation dose, some phosphorus penetrated into the base modifying the doping profile. Current gains grow in accordance with splits, reflecting higher collector current obtained for higher phosphorus doses. Notice that

Table III.3 | Junction-related parameters measured on wafers implanted with various phosphorus doses and carbon energies. $0.2 \times 5\ \mu m^2$ reference devices.

	Carbon energy	e_C				$2e_C$	
	Phosphorus dose	$d_C/2$	d_C	$2d_C$	$4d_C$	$2d_C$	$4d_C$
V_A	F (V)	152	140	113	20	102	25
	R (V)	1,7	1,7	1,5	0,9	1,6	0,9
BV	CEo (V)	1,83	1,72	1,5	1,34	1,47	1,33
	CBo (V)	6,6	6,3	5,2	4,3	X	4,3
	EBo (V)	2,2	2,1	2,1	2,3	X	2,3
C	BC (fF)	3,9	4,1	5,3	8,3	5,6	8,6
	BE (fF)	6,2	6,1	6,2	6,4	6,4	6,3

the 10 times variation of high-injection gain is also partially due to higher base current of devices implanted with low phosphorus doses.

Measured junction-related parameters are reported in Table III.3.

Forward Early voltages V_{AF} decrease with increasing doping in accordance with theory. A sharp drop is observed for wafers implanted with a $4d_C$ dose, indicating that devices are close to pinch-off. Both breakdown voltage BV_{CBo} and base-collector capacitance C_{BC} are in accordance with a more aggressive base-collector junction. Collector-emitter breakdown voltage BV_{CEo} also varies in accordance with a more aggressive junction and the improved current gain. The sharp difference observed passing from $2d_C$ to $4d_C$ indicates that a critical dose is reached beyond which the base doping concentration is insufficient for ensuring good junction control. V_{AR} explains that the emitter-base junction is affected by collector splits for high phosphorus dose, as already hypothesized observing currents. Both breakdown voltage BV_{EBo} and emitter-base capacitance C_{BE} indicate that the emitter-base junction is not affected electrostatically from collector splits. This observation confirms that phosphorus did not act on the doping profile by penetrating into the base.

In Table III.4 measured resistances are reported. Base resistances do not exhibit any particular correlation with collector splits. Intrinsic base resistance values confirm that collector splits did not impact the base doping profile. Collector buried layer resistances are in perfect accordance with the

values reported in Table III.1.

Table III.4 | Resistances measured on wafers implanted with various phosphorus doses and carbon energies. Values extracted from measurements on dedicated structures.

Carbon energy	e_C				$2e_C$	
Phosphorus dose	$d_C/2$	d_C	$2d_C$	$4d_C$	$2d_C$	$4d_C$
B_{TOT} (Ω)	65	61	62	63	68	64
R_{sPBI} (Ω/sq)	5,45	5,10	5,19	5,17	5,48	5,33
R_{sBx} (Ω/sq)	694	683	704	734	635	642
R_{sBL} (Ω/sq)	191	104	65	41	64	40

Table III.5 reports measured maximum frequencies. f_T values have a clear tendency to increase with the phosphorus dose, in accordance with a more aggressive base-collector junction depleting more the base. In accordance with increasing values of base resistance and base-collector capacitance, f_{MAX} follows f_T frequency increase by a smaller proportion and even drops for very high phosphorus doses. Regarding the splits with doubled carbon energy, a little degradation of performance is observed with no particular advantage.

Table III.5 | Maximum frequencies measured on wafers implanted with various phosphorus doses and carbon energies. 0.2×5 μm^2 reference devices. V_{BC} = -0.5 V.

Carbon energy	e_C				$2e_C$	
Phosphorus dose	$d_C/2$	d_C	$2d_C$	$4d_C$	$2d_C$	$4d_C$
f_T (GHz)	170	200	300	410	300	395
f_{MAX} (GHz)	308	320	355	290	353	277,5

In conclusion, different combinations of phosphorus dose and carbon energy have been tested for the carbon plus phosphorus collector co-implantation. Results show that a phosphorus dose two times the carbon dose is the most performing solution, allowing good values of f_T and f_{MAX} without degrading device behavior. The increase in carbon energy has no real advantage. A review of these results will be needed once the base profile will be optimized.

1.3 Impact of epitaxial collector thickness variability

Epitaxial growth is subject to natural variability due to its very sensitive chemistry. Investigation on the impact of process variability on device performance allows to correctly define the requirements for an optimal device.

The passage from a ring-shaped SSTI to a single-trench integration doubled the epitaxy thickness, making the growth process even more sensitive to variability. Figure III.6 compares two devices featuring collector epitaxy thicknesses with almost 20 nm of difference.

The collector epitaxy is responsible for aligning the part of the device grown in the emitter window with the stack. The extrinsic base thickness is designed to form a good contact with the intrinsic base no matter the collector thickness (cf. Section 2) and base resistance should be unaffected. If the collector is too thick, a perimetric junction is formed between collector and extrinsic base, contributing to base-collector capacitance C_{BC} and eventually leading to non-idealities in other figures of merit.

The self-aligned process used to form emitter spacers is to some degree sensitive to the emitter window depth after base epitaxy (cf. Section 4) and the effective emitter window width W_{E0} can be affected by variations in the collector epitaxy thickness. Even if the two devices presented in Figure III.6 were produced with the same spacers integration, a variation of collector thickness around 20 nm led to a shift of almost 30 nm in W_{E0}. Since the emitter spacers are finely tuned to obtain good emitter-base junction behavior (cf. Section 4), such variation can have an important impact on figures of merit.

In the following, figures of merit measured on a standard $0.2{\times}5\ \mu m^2$ devices featuring different collector thicknesses as seen in Figure III.6 are compared to understand the consequences. Collector doping, intrinsic base profile and extrinsic base characteristics are identical. Notice that the compared wafers are not part of the same production lot, meaning that process variability could have an impact on measured figures of merit which should normally not be impacted by the collector epitaxy, e.g. base doping, defects, etc. Reported DC figures of merit are the median value of what obtained on 17 sites evenly spaced on the same wafer and RF values are obtained on the best die of the wafer.

Table III.6 reports figures of merit related to base and collector currents. Devices with a thicker collector are clearly affected by important current

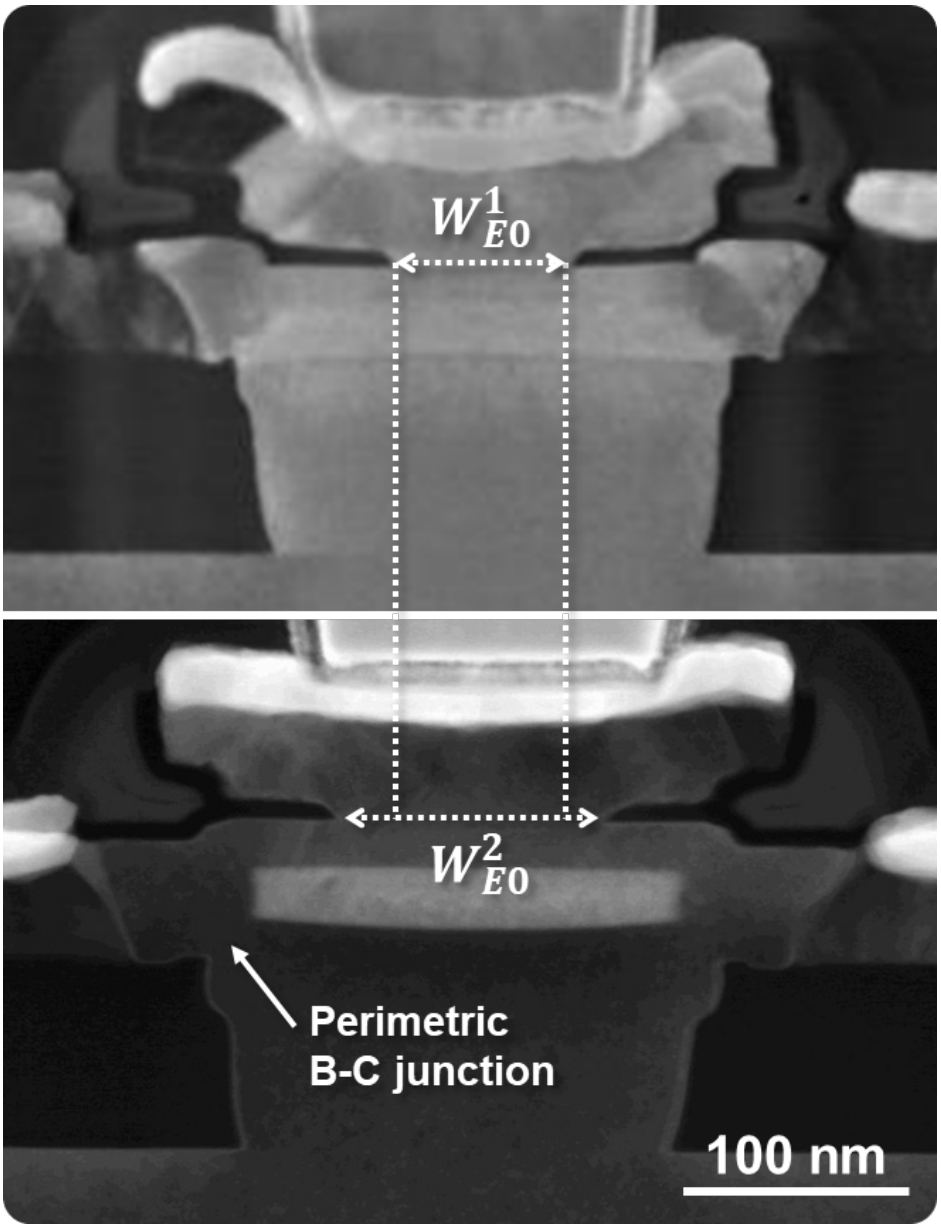

Figure III.6 | Comparison of two transistors featuring different epitaxial collector thicknesses.

leakages, particularly at low injection. Even if an increase of I_B is normal for a wider W_{E0} (cf Equation (I.1b)), a high η_{I_B} indicates the presence of non-idealities. For higher values of V_{BE}, the situation improves but is not sufficient to achieve adequate values of gain, which is below 400. A correct collector thickness is on the other hand capable of maintaining good values of gain at each polarization. As will be shown in Section 4, a very wide effective emitter window is usually linked to these kind of degradations in current behavior.

Table III.6 | Current-related figures of merit measured on devices featuring different collector thicknesses. $0.2 \times 5\ \mu m^2$ reference devices.

	Collector	REF	Thick
Low injection $V_{BE} = 0.5$ V	I_C (nA)	16	13
	I_B (pA)	22	237
	Gain	681	61
Medium injection $V_{BE} = 0.7$ V	I_C (μA)	26	26
	I_B (nA)	7	14
	Gain	3437	1851
High injection $V_{BE} = 0.9$ V	I_C (mA)	6	9
	I_B (μA)	4	23
	Gain	1614	363
η	I_B	1,35	1,71
	I_C	1,05	1,03

Junction-related figures of merit are reported in Table III.7. Measurement of BV_{CBo} was not possible on the thinner device due to a badly-regulated setup for breakdown detection and is not related to device malfunctioning. Transistors with the same collector doping obtained on other wafers typically exhibit values between 4.5 V and 5 V, implying that a thicker collector would lead to an increase in BV_{CBo} as it is normal for a less aggressive junction. A shift in BV_{CEo} is observed as a consequence, even if the low current gain of the thicker device does not seem to play a major role. This however confirms that currents have a secondary importance in defining this figure of merit. The emitter-base breakdown voltage BV_{EBo} benefits from the widening of the effective emitter window. As will be discussed in Section 4, such variation is linked to the onset of a perimetric emitter-base junction formed below the

emitter spacers where boron diffusing from the extrinsic base meets arsenic diffusing from the emitter. Forward Early voltage V_{AF} increases consistently with a thick collector thanks to the additional 20 nm of epitaxy making the base-collector junction less aggressive. V_{AF} benefits more from the wider spacers thanks to the contribution of boron diffusing from the extrinsic base.

Table III.7 | Junction-related figures of merit measured on devices featuring different collector thicknesses.

Junction-related figures of merit measured on devices featuring different collector thicknesses. $0.2 \times 5\ \mu m^2$ reference devices.

	Collector	REF	Thick
BV	CBo (V)	X	5,30
	CEo (V)	1,45	1,62
	EBo (V)	1,83	2,32
V_A	F (V)	36	90
	R (V)	1,1	1,5

Table III.8 reports parasitic resistances and capacitances measured on the same devices. Emitter resistance is naturally lower when spacers are narrower thanks to the increased area. Base resistance R_B is reduced for a thicker collector, thanks to the maximization of the section between intrinsic and extrinsic base ensuring an optimal contact. This variation clearly reflects on both component of the base resistance. Interestingly, C_{BC} increases with a thicker collector even if both V_{AF} and BV_{CBo} suggest a less aggressive behavior. Observing Figure III.6 it is immediately clear that such variation can be attributed to the perimetric junction between collector and extrinsic base, which does not affect the figures of merit linked to the vertical doping profile. C_{BE} is also degraded due to the wider effective emitter window leading to a wider emitter-base junction.

Resulting maximum f_T and f_{MAX} are reported in Table III.9. On a thicker device, less aggressive junctions and increased capacitances lead to 80 GHz less on f_T when compared to a thinner collector. A lower base resistance is not capable to compensate this effect and 10 GHz are still missing on f_{MAX}.

In conclusion, two devices featuring different thicknesses of epitaxial collector have been compared. This variation not only impacts vertical alignment with the stack but also the effective emitter window width due to the fabrication process of emitter spacers. Results indicate a total degradation of

Table III.8 | Parasitics measured on devices featuring different collector thicknesses. Base resistances extracted from measurements on dedicated structures, other values measured on Junction-related figures of merit measured on $0.2 \times 5\ \mu m^2$ reference devices.

	Collector	REF	Thick
R	Emitter (Ω)	3.8	3.4
	B_{TOT} (Ω)	73	65
	sBI (kΩ/sq)	6.5	5.6
	sBx (Ω/sq)	708	527
C	BC	5.3	5.6
	BE	7.2	7.7

Table III.9 | Maximum frequencies measured on devices featuring different collector thicknesses. $0.2 \times 5\ \mu m^2$ reference devices, V_{BC} = -0.5 V.

	Collector	REF	Thick
Frequencies	f_T	323	239
	f_{MAX}	393	381

performance due to 20 nm of excessive epitaxy thickness. The collector epitaxy thickness can therefore be considered a critical point in the integration of a single-trench SSTI in an EXBIC HBT, requiring particular attention.

1.4 Future studies

Results presented so far show a mature collector integration, with very few flaws. The study of defect-generating mechanisms due to collector implantation and the introduction of a single-trench SSTI allowed to obtain a good collector and the optimization of the carbon plus phosphorus co-implantation pushed the integration to its maximum.

Studies presented on collector doping have been performed without integrating the other optimized parts of the device. Particularly after the redesign of the base profile, some adjustments will be surely needed. Considering the relatively simple doping technique used for the collector, an adaptation of the phosphorus dose will be most probably sufficient for tuning the base-collector junction.

Regarding the collector epitaxy thickness variability, not much can be done from an integration standpoint. An extensive study on process parameters and their impact on the resulting epitaxy will allow to define best conditions for obtaining reliable devices.

Next sections will confirm the impact of perimetric effects on the base-collector junction mainly due to the extrinsic base, limiting the reduction of base resistance by increasing the doping level. Investigations both on architecture design or advanced doping techniques will serve to overcome this limitation and improving f_{MAX} without needing to find a compromise between base resistance and base-collector capacitance.

STMicroelectronics' B55 platform is capable of integrating three different HBT $f_T \times BV_{CEo}$ products on the same die, allowing to fulfill a wide variety of needs. Since the EXBIC collector doping is totally performed by ion implantation, a relatively simple solution has to be found in order to maintain the integration simplicity. Initial studies on the possibility to integrate more device flavors in an EXBIC-based BiCMOS technology have demonstrated its feasibility. Such studies will not be detailed here since not in the scope of

this work, but will surely be part of future technology developments.

2 Extrinsic base module

Section 2 of Chapter II allowed to define the 1-step extrinsic base integration. Even though a big improvement on electrical performance has been achieved by simply modifying the integration, proper optimization is required for maximizing the gains. The main objective is to minimize the extrinsic component of the base resistance R_{sBx} without considerably impacting the other figures of merit, e.g. currents, capacitances, breakdown voltages. Appendix 4 details how components of base resistance are obtained by model extraction.

Figure III.7 shows the parameters investigated for the 1-step extrinsic base optimization to reduce R_{sBx}.

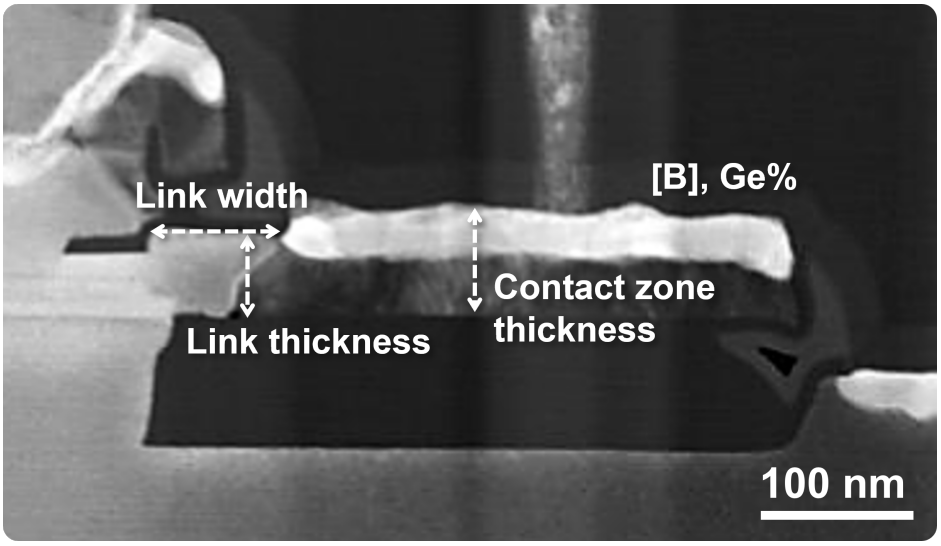

Figure III.7 | TEM cross-section highlighting the parameters investigated for the 1-step extrinsic base optimization.

The link between contact zone and intrinsic base can be modified both in terms of thickness and width. This link is important because it defines a big part of the extrinsic resistance due to the absence of salicidation. Both l and A of the link can be tuned in this way. Thickness of the contact zone opposes two opposite resistance minimization mechanisms. A thick contact zone increases the overall section A, reducing its resistance. If thickness is too high, the salicided portion of the contact polysilicon will be higher than the link, contributing to l. Extrinsic base resistivity ρ can be addressed by

modifying its doping. Boron concentration $[B]$ directly affects its resistivity, while germanium percentage $\%Ge$ may regulate some barrier effects occurring at the contact with the SiGe intrinsic base.

2.1 Extrinsic base thickness

The base link thickness defines the conductor section for the portion of the extrinsic base which is not silicided. It can also modulate boron diffusion from the extrinsic base into the intrinsic part, eventually impacting other figures of merit such as base-collector capacitance C_{BC}.

An experiment has been conducted on the link thickness to assess its optimal value. The sacrificial nitride present in the stack determines the cavity thickness where the link forms during extrinsic base epitaxy (cf. Section 2.2). Up to four sacrificial nitride thicknesses have been tested in combination with three extrinsic base epitaxy processes. Nitride thickness goes from 20 nm to 40 nm trying to maximize the contact section between link and intrinsic base. Epitaxy process splits allow to evaluate how the thickness of the contact zone or its boron concentration combine with the sacrificial nitride variations. Three contact zone conditions are reported: reference thickness + reference doping, increased thickness + reference doping and increased thickness and doping. Devices are produced with a ring-shaped SSTI and feature a 1-step extrinsic base integration.

Table III.10 reports the extracted extrinsic R_{sBx} and intrinsic R_{sBI} components of the base resistance for the tested process splits. Each extrinsic base split exhibits optimal extrinsic base resistance R_{sBx} for a sacrificial nitride thickness of 36 nm, while the intrinsic base resistance R_{sBI} decreases progressively with the link thickness.

Results can be interpreted with the help of Figure III.8 highlighting the impact of process splits on device morphology through TEM cross-sections combined with EDX.

Both devices feature a bit too thick intrinsic collector epitaxy, leading to an intrinsic base not perfectly aligned to the stack. A thinner link (Figure III.8 left) leads in this case to a choking point degrading base resistance. On the other hand, a thick link (Figure III.8 right) allows to contact the base on its whole thickness thus avoiding any bottleneck. Even though collector epitaxy thickness is supposed to properly align base and stack in an optimized device, process variability can induce some shifts which have to

Table III.10 | Extrinsic and intrinsic base resistances of devices with different sacrificial nitride thicknesses and contact zone characteristics. Values extracted from measurements on dedicated structures.

(a) | Reference extrinsic base.

Link thickness	20 nm	28 nm	36 nm	40 nm
R_{sBx} (Ω/sq)	1216	1039	839	907
R_{sBI} $(k\Omega/sq)$	7.4	6.9	6.9	6.7

(b) | Increased extrinsic base thickness.

Link thickness	20 nm	28 nm	36 nm	40 nm
R_{sBx} (Ω/sq)	596	512	479	486
R_{sBI} $(k\Omega/sq)$	7.0	7.0	6.7	6.6

(c) | Increased doping and extrinsic base thickness.

Link thickness	20 nm	28 nm	36 nm
R_{sBx} (Ω/sq)	368	399	368
R_{sBI} $(k\Omega/sq)$	7.5	6.7	6.6

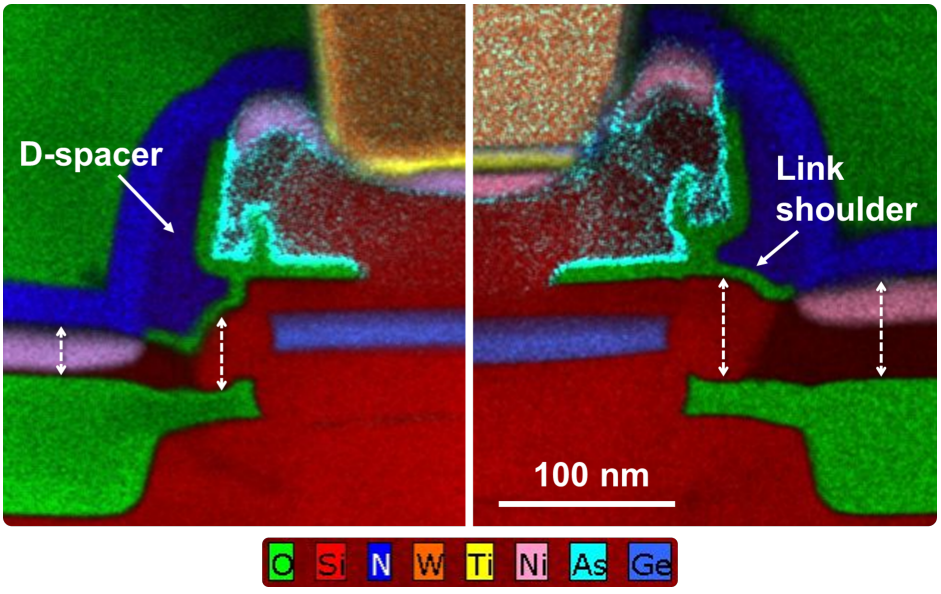

Figure III.8 | TEM cross-section + EDX coloring of two devices obtained within the base link thickness study. Left: 28 nm link, reference extrinsic base. Right: 36 nm link, thick extrinsic base.

be accounted for. These results explain the advantage of having a slightly thicker base link to compensate a sub-optimal alignment. In the event of a correct collector epitaxy, the emitter L-spacers would simply cover a part of the total link section but the connection between intrinsic and extrinsic base would be unchanged.

The found optimal link thickness value can be explained considering the impact it can have on the rest of the structure. Self-aligned CMOS D-spacers are produced at the end of the process flow to avoid a short-circuit between emitter and extrinsic base during silicidation. Due to the self-aligned process, the spacers will be modeled on the underlying device topology. A particularly thick base link can lead to the formation of a "shoulder" if it is thicker than the contact zone. The resulting topology will lead to wider D-spacers, increasing the distance between silicide and intrinsic base and therefore raising the extrinsic base resistance. Regarding the intrinsic base resistance R_{sBI}, its value decreases with the increase of the base link thickness because of a higher boron dose capable of diffusing from the extrinsic base into the intrinsic zone. Interestingly, boron concentration does not have a clear impact. Extrinsic base resistance is always minimized with a 36 nm-thick sacrificial nitride, implying that the contact zone can be optimized independently.

Evaluation of other figures of merit allows to determine the overall impact of tested process splits on the rest of the device. Measured values are reported in Table III.11.

Ideality factors are good for all tested process splits, but the thinnest link exhibits some base current leakage represented by a slightly higher η_{I_B}. It is possible that a thin cavity inhibits a correct link doping, therefore inducing leakages. Both direct and reverse Early voltages improve with a thicker link thanks to the higher boron dose diffusing into the intrinsic base. Early voltages are normally linked to the vertical (intrinsic) doping profile, which should not be impacted by the extrinsic components. BV_{CEo} and BV_{CBo} are essentially stable, while BV_{EBo} increases with a thicker link.

Due to the excessive collector thickness observed in Figure III.8, the base-collector capacitance C_{BC} is unsurprisingly impacted by these splits: a higher presence of dopants on the sides will in fact add a perimetric contribution to the overall capacitance. On the other hand, C_{BE} decreases with a thicker link, indicating a less aggressive junction in accordance with BV_{EBo} and V_{AR}. The previous considerations on increased boron diffusion in the intrinsic zone appear in contrast with the idea of a less aggressive emitter-base junction. Considering the complexity of this bidimensional junction, boron penetrating

Table III.11 | Electrical figures of merit of devices with different sacrificial nitride thicknesses and contact zone characteristics. $0.2\times5\ \mu m^2$ reference devices.

(a) | Reference extrinsic base.

	Link thickness	20 nm	28 nm	36 nm	40 nm
η	I_B	1.37	1.26	1.26	1.23
	I_C	1.03	1.02	1.02	1.02
V_A	F (V)	64	71	74	75
	R (V)	1.65	1.75	1.77	1.77
BV	CEo (V)	1.51	1.48	1.48	1.49
	CBo (V)	5.37	5.35	5.36	5.36
	EBo (V)	2.44	2.54	2.63	2.67
C	BC (fF)	7.23	7.22	7.26	7.29
	BE (fF)	7.52	6.99	6.89	6.77

(b) | Increased extrinsic base thickness.

	Link thickness	20 nm	28 nm	36 nm	40 nm
η	I_B	1.27	1.21	1.20	1.20
	I_C	1.03	1.03	1.02	1.02
V_A	F (V)	72	69	69	71
	R (V)	1.61	1.66	1.77	1.87
BV	CEo (V)	1.49	1.46	1.46	1.47
	CBo (V)	5.31	5.29	5.32	5.33
	EBo (V)	2.46	2.54	2.61	2.64
C	BC(fF)	7.31	7.41	7.31	7.46
	BE (fF)	7.55	7.16	6.94	6.95

(c) | Increased doping and extrinsic base thickness.

	Link thickness	20 nm	28 nm	36 nm
η	I_B	1.32	1.24	1.23
	I_C	1.02	1.02	1.02
V_A	F (V)	71	77	77
	R (V)	1.80	1.81	1.72
BV	CEo (V)	1.50	1.47	1.46
	CBo (V)	5.26	5.21	5.13
	EBo (V)	2.16	2.53	2.64
C	BC(fF)	7.57	7.60	7.65
	BE (fF)	7.94	7.24	7.11

from the sides is likely to act on the net active junction doping, contrasting the arsenic contribution. As a consequence, the net n-doping is lowered, making the junction less aggressive. These phenomena show that, even if the 1-step extrinsic base integration could resolve the main problems affecting the 2-step integration, some parasitic phenomena are still observed. Section 4 will explain how emitter spacers are used for minimizing these effects.

In conclusion, devices featuring four different base link thickness coupled with three different combinations of doping concentration and contact zone thickness have been tested. Results show that a totally independent optimization between intrinsic and extrinsic base is not always possible. In fact, the position of the extrinsic base combined with emitter diffusion below the L-spacers is likely to generate a secondary emitter-base junction with different characteristics with respect to the ones chosen for the intrinsic base. Current leakages can be for example related to an insufficient potential barrier allowing some carrier to pass when not expected.

2.2 Germanium percentage

The possibility to dope in-situ during the extrinsic base epitaxy offers a high degree of freedom when choosing the impurities to incorporate. Germanium is considered as a possible dopant on top of boron for the many effects it can have on the electric figures of merit. Considering the presence of germanium in the intrisic base, a potential barrier could arise, increasing the total base

resistance R_B. Germanium is also known for its action on boron diffusion [65] and could impact the resulting 2D doping profile, modifying junctions.

On wafers with identical extrinsic base boron concentration and thickness, three splits of germanium percentage have been tested: 0 %, 10 % and 20 %. *DC* figures of merit measured on reference 0.2x5 μm^2 devices are reported in Table III.12.

Table III.12 | Figures of merit obtained on devices featuring variations of germanium percentage in the extrinsic base. 0.2×5 μm^2 reference devices. Base resistances extracted from measurements on dedicated structures.

	$\%Ge$	0 %	10 %	20 %
η	I_B	1.19	1.17	1.16
	I_C	1.03	1.02	1.02
BV	CBo (V)	4.47	4.90	4.94
	CEo (V)	1.44	1.45	1.48
	EBo (V)	2.18	2.22	2.22
V_A	F (V)	43	42	40
	R (V)	2.1	1.8	1.6
R	B_{TOT} (Ω)	74	83	89
	PinchedB (kΩ/sq)	6.4	6.3	6.0
	ExBase (Ω/sq)	629	653	916

The impact of germanium on boron diffusion is likely to influence the health of the emitter-base junction as observed in other cases: η_{I_B} increases for lower germanium percentage, indicating a modulation of base current leakage. Collector ideality factor η_{I_C} slightly increases for the 0 % split, possibly for the same reason.

The impact of germanium on the base-collector junction can be observed both on breakdown voltage BV_{CBo} and forward Early voltage V_{AF}, both indicating an increase of boron on the base side for lower percentages. BV_{CEo} follows this trend. Regarding the emitter-base junction, BV_{EBo} slightly decreases at 0 % germanium possibly due to the increased base current leakages. V_{AR} confirms the increase of boron in the base due to modified diffusion, increasing by 30 % when reducing the germanium percentage.

Total base resistance R_{Btot} is clearly dependent from the splits. While extrinsic base resistances follow total base resistance decreasing with ger-

manium percentage, the intrinsic base increases. This phenomenon partially contradicts the hypothesis of increased boron diffusion from the extrinsic base to the intrinsic one modulated by germanium percentage. If boron diffusion was the only mechanism acting, an opposite tendency should be observed. Considering properties of SiGe alloys, literature reports a decrease in hole mobility for germanium percentages up to 30 % [38], which can explain the increase in extrinsic base resistance. Regarding the effect on R_{sBI}, the interaction between the vertical strain due to the SiGe profile in the base and the horizontal contribution of the extrinsic base could lead to complex 2D piezoresistive effects [57]. Advanced TCAD simulations considering strain-related effects and advanced TEM imaging could offer a better understanding of this complex phenomenon.

In conclusion, variations of germanium percentage in the extrinsic base spanning from 0 % up to 20 % have been tested. Higher percentages lead to a reduction of base current leakage and increase breakdown voltages, while lower percentages are related to better Early voltages. These effects are attributed to the modulation of boron diffusion induced by germanium. Low Ge percentages are capable of reducing the total base resistance by 16 % but the intrinsic and extrinsic components vary counter-intuitively with respect to the boron-diffusion hypothesis. SiGe alloy composition is held responsible both for hole mobility degradation and piezoresistive effect, explaining the observed behavior. Deeper analysis is required for validating the given hypotheses. Replacing germanium with other diffusion-reducing elements such as carbon could allow to modulate boron diffusion while avoiding any effect linked to germanium.

The split containing 0 % of germanium in the extrinsic base leads to the lowest base resistance. *RF* measurements are required to verify the impact on junction capacitance.

2.3 Boron concentration

Boron is the active dopant both for intrinsic and extrinsic base in an EXBIC HBT. If on one hand it would be natural to increase boron concentration to reduce the extrinsic base resistance, diffusion in the intrinsic base could negatively impact the other figures of merit. Three boron concentrations B1, B2 and B3 have been tested on devices with identical extrinsic base thickness and germanium percentage. The three tested concentrations span from orders of magnitude of 1e18 at/cm^3 (B1) to 1e20 at/cm^3 (B3). *DC*

figures of merit measured on reference 0.2x5 μm transistors are reported in Table III.13.

Table III.13 | Figures of merit obtained ondevices featuring variations of boron concentration in the extrinsic base. $0.2 \times 5\ \mu m^2$ reference devices. Base resistances extracted from measurements on dedicated structures.

	[B]	B1	B2	B3
η	I_B	1.16	1.17	1.18
	I_C	1.02	1.02	1.02
BV	CBo (V)	4.97	4.90	4.96
	CEo (V)	1.45	1.45	1.46
	EBo (V)	2.12	2.13	2.12
V_A	F (V)	39	38	37
	R (V)	1.8	1.9	1.8
R	B_{TOT} (Ω)	91	83	74
	sBI (kΩ/sq)	6.5	6.3	6.1
	sBx (Ω/sq)	896	716	613

Base ideality factor η_{I_B} slightly degrades with higher boron concentrations, even if the minimal difference is essentially negligible. η_{I_C} is totally unaffected.

Stable values of V_{AF} and BV_{CBo} prove that the base-collector junction is unaffected by the extrinsic base doping splits On the emitter-base side, BV_{EBo} and V_{AR} are also stable, indicating that boron did non affect the electrostatics of this junction.

Base resistances decrease of almost 20 % with increasing boron concentration, as expected. While the reduction of 30 % of the extrinsic component of resistance is the expected result, the effect on the intrinsic base resistance lowering by 6 % indicates that some boron could have penetrated into the intrinsic base. The variation on this last parameter is however relatively small and could be attributed to modeling error. This can be confirmed considering the absence of effects observed on breakdown and Early voltages. With respect to what observed on Section 2.2, no particular phenomenon is highlighted.

In conclusion, variations in boron concentration spanning from orders of magnitude of 1e18 at/cm^3 to 1e20 at/cm^3 have been tested, resulting in decreasing resistances for higher doses. The boron concentrations tested in this experiment did not affect the behavior of the intrinsic device and higher values could be tested. The test has to be repeated in combination with different germanium percentages in order to establish it is acting on boron diffusion as previously discussed.

The split containing boron in a concentration in the order of 1e20 at/cm^3 has the lowest base resistance. RF measurements are required to evaluate the impact on parasitic capacitances and determine the eventual advantage in terms of maxixmum f_T and f_{MAX}.

2.4 Future studies

Some results presented in this section highlighted the possible impact of germanium both on piezoresistivity and boron diffusion. Further investigations are required to see if such phenomenon could be exploited to enhance performances. The investigation of carbon doping could also allow to use higher boron concentrations while avoiding excessive diffusion in the intrinsic zone with consequent performance degradation.

Apart from this, studies presented in this section could be repeated when the rest of the device will be optimized in order to further tune the extrinsic base. Section 4 will treat how emitter spacers can be sized, partly acting on the same phenomena described in this section. If any modification of collector or emitter integration will be done, a completely new study will have to be performed with the new conditions.

3 Intrinsic base module

The intrinsic base is the pulsing heart of a bipolar transistor, affecting most of its figures of merit and ultimately defining its high-frequency performance.

The initial base doping profile used for Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) development is inherited from the DPSA-SEG architecture developed for the STMicroelectronics' BiCMOS055 (B55) technology. For confidentiality reasons, only relative sizes and doping levels will be presented in this section.

The intrinsic base is obtained by a single in-situ-doped selective epitaxy performed after collector growth. The result is a layer of Si and SiGe with a complex doping profile obtained in the emitter window and thinner than 50 nm. Figure III.9 depicts a schematic profile of the intrinsic base.

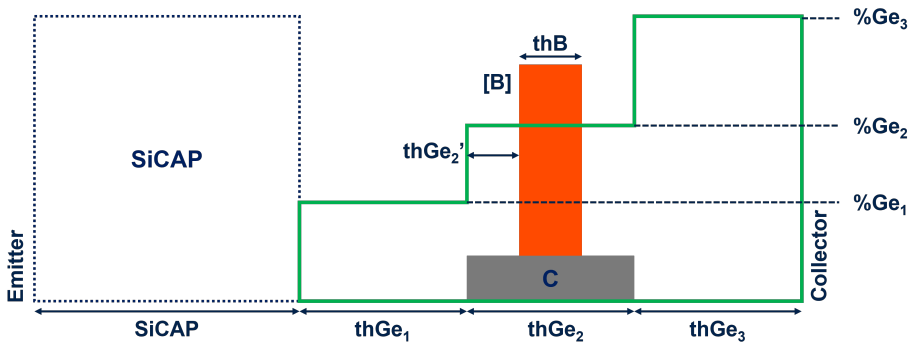

Figure III.9 | Schematic of the intrinsic base doping profile integrated in the EXBIC HBT.

Starting from the emitter, an undoped silicon capping layer (SiCAP) serves to buffer arsenic diffusion from the emitter, allowing to obtain a correct doping profile after diffusion induced by all the remaining steps in the process flow. Below the SiCAP, an increasing staircase-like germanium profile ensures to obtain a graded distribution after diffusion due to subsequent thermal treatments in the process flow, guaranteeing the onset of the built-in electric field. Each of the three steps (Ge_1, Ge_2 and Ge_3) can be modulated both in width ($thGe_x$) and germanium percentage ($\%Ge_x$). A very steep profile would maximize the drift component of electron transit in the base, requiring to incorporate as much germanium as possible in Ge_3 to maximize this effect. Germanium fraction does not go above 40 %. A boron layer

is conveniently placed in the central step of germanium, featuring its specific width thB and a boron concentration [B] that can go up to some 10^{20} atoms per cm^3. Carbon is present in the central step of germanium Ge_2 in a concentration sufficient for limiting boron diffusion through suppression of TED [28]. Germanium itself undergoes diffusion during the remaining processing steps, leading to a final smooth asymmetric shape. Boron diffusion is impacted by germanium concentration [65], leading to a slightly asymmetric doping profile. Figure III.10 shows reference boron and germanium profiles in the base obtained by TOF-SIMS at the end of the production flow.

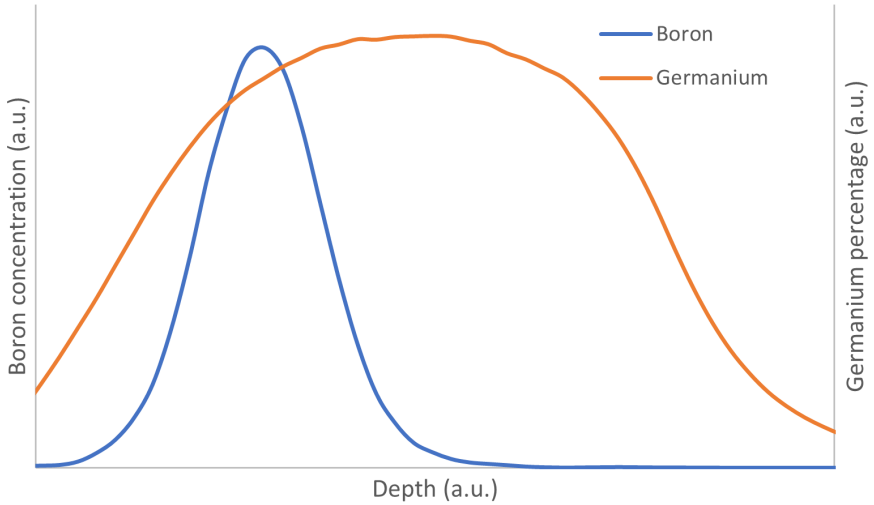

Figure III.10 | Boron and germanium profiles in the base obtained by TOF-SIMS at the end of the production flow

In this section, variations over the multiple parameters defining the intrinsic base doping profile will be investigated to understand how to get the most out of an EXBIC HBT.

Future studies will be defined based on the obtained results, seeking for further optimizations.

3.1 Boron concentration and doped layer width

Since the base doping profile is inherited by the previous DPSA-SEG, it is most probably not well adapted to the new EXBIC architecture. Considering the redesign and consequent optimization of both collector and extrinsic base, a review of the active dopant distribution in the base is required.

Variations on boron doping have been tested on wafers integrating $0.2{\times}5\ \mu m^2$ GoTo EXBIC HBTs featuring collector doping corresponding to a 60 Ω/sq buried layer resistance, reference extrinsic base and 100 nm effective emitter window width. Boron concentration goes from the reference value up to 2 and 3 times. The boron-doped layer can feature either reference thickness or be 9 % or 18 % thinner; the second germanium step thickness $thGe_2$ is adjusted accordingly.

Table III.14 reports average current gains and ideality factors for different splits of boron concentration and thickness of the doped layer. In accordance to Equation (I.1b), thinner layers allow more electrons to pass through the neutral base without recombining, increasing collector current and gain as a consequence. For the same mechanisms, higher boron density is related to higher recombination in the neutral base, reducing collector current and gain as a consequence. Comparing splits with different combinations of boron concentration and thickness, it is possible to find a compromise leading to similar gains with different profiles. For example, a profile with three times the reference boron concentration and -18 % thickness shows current gains comparable with those measured on a device with two times the reference boron concentration and reference thickness. It is therefore held possible to act on other figures of merit while keeping current characteristics almost constant. Base current ideality factors η_{I_B} are all below the limit value of 1.30, indicating that the characteristics are not impacted, as expected. Collector current ideality factor η_{I_C} is around 1.02 for most splits, indicating that boron variations act on currents in accordance with theory and without any undesired effect.

In Table III.15 are reported breakdown and Early voltages for the tested splits.

Even if an impact of boron concentration would normally be expected (cf. Equation (I.4)), base-collector breakdown voltages BV_{CBo} are all very close to the average value of 5.5 V, practically indicating that the tested splits have no impact on this figure of merit. Considering BV_{CBo} constant for all splits, the emitter-base breakdown voltage BV_{ECo} follows current gain

Table III.14 | Current gain and ideality factors for different boron layer thicknesses and dopant concentrations. $0.2 \times 5\ \mu m^2$ reference devices.

(a) | [B] = REF

	thB	REF	-9 %	-18 %
Current gain	Low injection, $V_{BE} = 0.5$ V	740	880	1130
	Medium injection, $V_{BE} = 0.7$ V	2510	2840	3280
	High injection, $V_{BE} = 0.9$ V	830	900	910
η	I_B	1.25	1.26	1.24
	I_C	1.02	1.03	1.03

(b) | [B] = 2 REF

	thB	REF	-9 %	-18 %
Current gain	Low injection, $V_{BE} = 0.5$ V	410	830	1330
	Medium injection, $V_{BE} = 0.7$ V	1630	2630	5750
	High injection, $V_{BE} = 0.9$ V	770	880	910
η	η_{I_B}	1.25	1.25	1.33
	I_C	1.01	1.03	1.05

(c) | [B] = 3 REF

	thB	REF	-9 %	-18 %
Current gain	Low injection, $V_{BE} = 0.5$ V	140	230	510
	Medium injection, $V_{BE} = 0.7$ V	630	870	1800
	High injection, $V_{BE} = 0.9$ V	345	500	715
η	I_B	1.3	1.25	1.27
	I_C	1.02	1.02	1.02

variations in accordance with Equation (I.5): higher current gains lead to lower breakdown voltages. Very low gains observed on splits with three times the reference boron concentration lead to breakdown voltages above the detection limit of 2 V, i.e. the threshold current set for detecting breakdown has not been attained before the maximum tested voltage of 2 V. Regarding the emitter-base breakdown voltage BV_{EBo}, a decrease is observed at increasing boron concentrations in accordance with Equation (I.4). A slight increase in base-emitter breakdown voltage is observed when reducing the doped layer thickness. The process adjustments required for modifying the epitaxy thickness could have altered the growth of successive layers, impacting this figure of merit. The observed variations relate to a less aggressive junction for thinner bases. SIMS analyses are required to confirm this hypothesis. Forward Early voltages do not exhibit a clear trend as a function of base doping. Considering only a tiny part of the base-collector depletion region is actually in the base due to the dose ratio with the collector, the tested splits generate only a negligible difference. Apart from the split with two times the reference boron concentration, V_{AF} tends to decrease in thinner bases. Regarding reverse Early voltages, a clear trend is visible both as a function of concentration and thickness. Higher doses are generally linked to higher voltages, thanks to the fact that the base results less depleted. Thinner bases are on the other hand affected by decreased voltages due to the reduced ratio between the undepleted and depleted zones of the base.

Parasitic resistances are reported in Table III.16.

Emitter resistances are mostly stable around 6 Ω, with no specific correlation with base splits. Total base resistance and more specifically the intrinsic base resistance is related to base splits. In accordance with theory, higher boron concentrations are related to lower resistances. Reducing the doped layer thickness has clearly an impact on resistance due to the reduced section of the conducting layer.

Extrinsic base resistances show a particular behavior, increasing for higher boron concentration and decreasing along with thickness. Considering a higher boron concentration than in the extrinsic base, a potential barrier is likely acting on holes, explaining the dose dependence. It is not clear how a thinner base would reduce the extrinsic base resistance. The quality of the extraction of this figure of merit is questioned. Akin to what observed for current gain, it is possible to reproduce similar resistances with different combinations of boron concentration and thickness, enabling a certain flexibility when choosing the best compromise with other figures of merit.

Maximum f_T and f_{MAX} measured on a golden die are reported in Ta-

Table III.15 | Breakdown and Early voltages for different boron layer thicknesses and dopant concentrations. $0.2 \times 5\ \mu m^2$ reference devices.

(a) | [B] = REF

	thB	REF	-9 %	-18 %
BV	CEo (V)	1.6	1.54	1.51
	CBo (V)	5.6	5.5	5.5
	EBo (V)	1.9	2	2.1
V_A	F (V)	68	64	46
	R (V)	1.9	1.7	1.5

(b) | [B] = 2 REF

	thB	REF	-9 %	-18 %
BV	CEo (V)	1.65	1.57	1.47
	CBo (V)	5.5	5.5	5.8
	EBo (V)	1.8	2	3.6
V_A	F (V)	65	59	69
	R (V)	2.4	1.7	1.1

(c) | [B] = 3 REF

	thB	REF	-9 %	-18 %
BV	CEo (V)	> 2	> 2	1.63
	CBo (V)	5.2	5.4	5.5
	EBo (V)	1.6	1.7	1.8
V_A	F (V)	120	101	76
	R (V)	2	2.5	1.8

Table III.16 | Parasitic resistances for different boron layer thicknesses and dopant concentrations. Values extracted from measurements on dedicated structures.

(a) | [B] = REF

	thB	REF	-9 %	-18 %
R	Emitter (Ω)	5.5	6.2	6,0
	B_{tot} (Ω)	75	71	81
	sBx (Ω/sq)	725	780	790
	sBI ($k\Omega/sq$)	5.3	5.6	6.4

(b) | [B] = 2 REF

	thB	REF	-9 %	-18 %
R	Emitter (Ω)	6,0	6.2	6.3
	B_{tot} (Ω)	48	64	121
	sBx (Ω/sq)	800	760	620
	sBI ($k\Omega/sq$)	3.2	5	12.1

(c) | [B] = 3 REF

	thB	REF	-9 %	-18 %
R	Emitter (Ω)	6.8	6.3	6.3
	B_{tot} (Ω)	29	36	48
	sBx (Ω/sq)	880	845	780
	sBI ($k\Omega/sq$)	1.4	2.1	3.4

Table III.17 | Maximum f_T and f_{MAX} measured on a golden die for different boron layer thicknesses and dopant concentrations. $0.2 \times 5\ \mu m^2$ reference devices, V_{BC} = -0.5 V

(a) | [B] = REF

thB	REF	-9 %	-18 %
f_T	270	265	276
f_{MAX}	360	348	348

(b) | [B] = 2 REF

thB	REF	-9 %	-18 %
f_T	259	282	291
f_{MAX}	376	364	340

(c) | [B] = 3 REF

thB	REF	-9 %	-18 %
f_T	252	258	275
f_{MAX}	385	390	360

ble III.17. The transit frequency is naturally related to the intrinsic base characteristics through the transit time. Thinner bases are naturally linked to faster devices thanks to the shorter path electrons have to cover. Higher doping concentration degrades the transit time, reducing f_T. f_{MAX} is subject to a trade-off between transit frequencies and base resistances, requiring a compromise. The best $f_T \times f_{max}$ product is obtained when doubling the boron concentration [B] and reducing the thickness of the doped layer thB by 9 %, with respect to the reference process.

In conclusion, variations over the doped layer of the intrinsic base have been tested, namely boron concentration [B] and thickness thB. The highest values of f_T and f_{MAX} have been obtained doubling the reference dopant concentration and shrinking the active dopant profile by 9 %. Measurements on other figures of merit suggest that this solution is capable of improving the high frequency performance without degrading the other figures of merit, practically offering a better compromise for the doping profile.

3.2 Future studies

Results obtained on the variations of boron show that the reference profile is not adapted to the EXBIC HBT architecture as defined by the present study. The main conclusion is that the boron profile could benefit both from an increase in concentration and a shrink. Best results have been obtained with two times the reference concentration and a shrink of 9 %.

A first round of testing requires to investigate boron positioning in order to determine whether the germanium slope is fully exploited or not. Without considering the eventual difference in boron diffusion due to germanium, a shift of f_T toward higher frequencies would confirm that the transit time can be further reduced by better exploiting the built-in electric field. The improved boron profile resulting from the previous studies should be used for this test. An adjustment of the SiCAP will be required to further adjust the figures of merit related to the emitter-base junction.

A second round of testing should review the germanium profile in all its parts once the boron peak is well placed. Some exploratory studies on the first two germanium steps Ge_1 and Ge_2 have already been started with the reference boron profile and the third germanium step Ge_3 will follow. Previous studies performed on the DPSA-SEG architecture [23] showed an improvement of 40 GHz on f_T. A fourth layer Ge_4 on the collector side could also be introduced as a buffer layer allowing to increase the germanium percentage $\%Ge_3$ without the risk of a barrier effect. On the other hand, a simplification of the doping profile could be interesting for reducing both complexity and cost.

4 Emitter module

The emitter of an Heterojunction Bipolar Transistor is responsible for defining its base current by regulating holes injection and recombination (cf. Equation (I.1b)). Important parasitics are related to the emitter, such as emitter resistance R_E and base-emitter capacitance C_{BE}.

The studies presented in Chapter II Section 4 allowed to solve most problems regarding the emitter and the only optimization left is the tuning of the effective emitter window width. Emitter doping has for the moment not been considered but some ideas will be presented in Section 4.2.

4.1 Spacers sizing

An experiment on the effective emitter window width W_{E0} has been performed with values spanning from 80 nm to 110 nm. Figure III.11 presents the TEM cross-section of a device obtained within this experiment. The tested device features standard 0.2×5 μm^2 emitter window, reference base profile and collector implants leading to 60 Ω/sq buried layer sheet resistance.

Measured currents at three injection levels (V_{BE} = 0.5, 0.7, 0.9 V; V_{BC}= 0 V) and corresponding base and collector ideality factors are reported in Table III.18. Particularly at low injection, current leakages are related to increasing effective emitter window widths, leading to a harsh degradation of η_{I_B} and a slight increase in η_{I_C} at W_{E0} = 110 nm. As described in Section 2, leakages are linked to the onset of a perimetric parasitic emitter-base junction which is responsible for non-idealities in the device behavior. The high variability of base current measurements ($\sigma_{\%} > 100\%$) complicates the analysis of surfacical and perimetric current components. A qualitative analysis can be done considering Equation (I.1b): base currents are expected to increase proportionally to the enlargement of the effective emitter window. The non-linear ratio between base currents and effective emitter window widths clearly shows the onset of an increasing additional current component for wider windows, particularly at low injection. Collector currents vary following the effective emitter window width variation. In accordance with the conclusions obtained in Chapter II Section 2 and Chapter III Section 2, current leakages could be reduced through an additional tuning of the extrinsic base doping. In such way, emitter outdiffusion in the base capping can be modulated, eventually mitigating the effects of the perimetric parasitic junction.

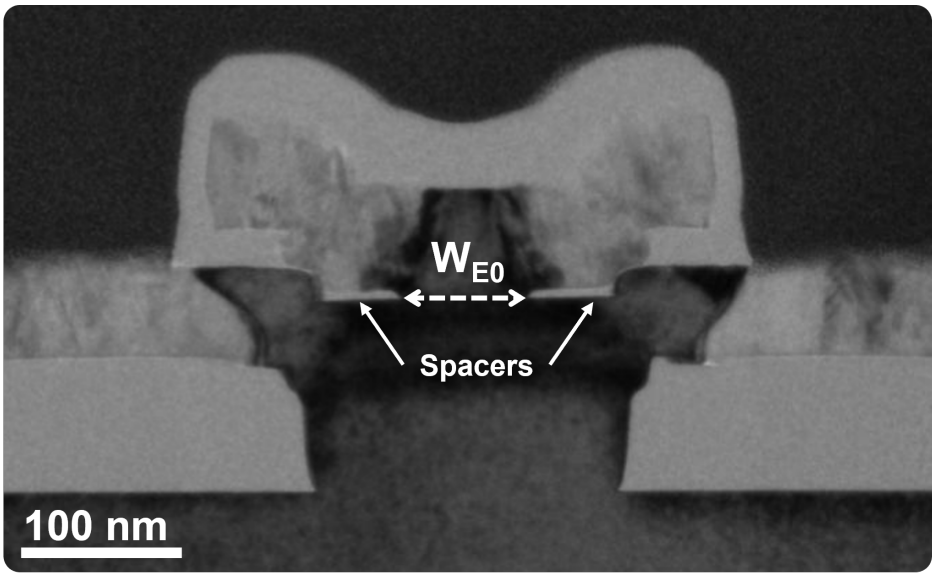

Figure III.11 | TEM cross-section of a device obtained within the experiment on the effective emitter window variation. Cut performed after extrinsic base epitaxy.

Table III.18 | Currents and related parameters measured on HBTs featuring different effective emitter window widths. $0.2 \times 5\ \mu m^2$ reference devices.

	W_{E0}	80	100	110
Low injection $V_{BE} = 0.5$ V	I_C (nA)	14	17	24
	I_B (pA)	17	73	203
	Gain	1011	409	379
Medium injection $V_{BE} = 0.7$ V	I_C (μA)	25	29	36
	I_B (nA)	7	9	12
	Gain	3419	3084	2936
High injection $V_{BE} = 0.9$ V	I_C (mA)	6	7	7
	I_B (μA)	4	5	5
	Gain	1541	1462	1529
η	Base	1,29	1,49	1,75
	Collector	1,04	1,04	1,06

Table III.19 reports breakdown and Early voltages of the tested devices. Measurement problems make the evaluation of BV_{CBo} impossible. It is however reasonable to assume that the base-collector breakdown voltage is unchanged since the spacers are intended to affect the emitter-base junction only. With this assumption, BV_{CEo} increases for wider windows due to lower current current gains. BV_{EBo} values cannot be related with the tested effective emitter window variations. Reverse Early voltages V_{AR} decrease with a wider window, representing an increasing contribution of the lowly-doped lateral junction as already observed on other figures of merit. Forward Early voltages are particularly low for the tested wafers, suggesting that devices are close to punch-through. Nevertheless, evaluation of the base-collector junction behavior is still possible. Decreasing values of V_{AF} are measured for wider windows, indicating that base-collector junction operation is impacted by the spacers width, degrading along with the increase of the effective emitter window width.

Table III.19 | Junction-related parameters of HBTs featuring different effective emitter window widths. $0.2 \times 5\ \mu m^2$ reference devices.

	W_{E0}	80	100	110
BV	CEo (V)	1.45	1.47	1.50
	EBo (V)	1.87	1.79	1.96
V_A	F (V)	36	34	30
	R (V)	1.3	1.2	1.0

Table III.20 reports parasitics extracted on tested devices. Emitter resistance R_E decreases sharply when W_{E0} passes from 80 nm to 100 nm, almost saturating for wider windows. Total base resistance R_B increases with a wider effective window. An extreme standard deviation, in some cases above 100 %, is remarked. An increase of R_{sBI} for shorter spacers confirms that a wider effective emitter window induces higher arsenic diffusion from the emitter. R_{sBx} should on the other hand decrease proportionally, but measurements do not confirm the expectations. Considering the observed impact of parasitic perimetric junctions on these devices, a second-order effect is likely to play a role in this case. Referring to Figure III.11, one may notice that the intrinsic base - identified by its darker shade due to Ge - is faceted on the sides. The presence of an interface between intrinsic and extrinsic base is likely playing a role in base resistance variability, affecting the quality of the results.

The good correlation between R_B and R_{sBI} leads to the conclusion that total base resistance is in this case mostly due to the intrinsic base contribution, making it the first parameter to evaluate when tuning the effective emitter window width.

Referring to capacitances, base-emitter capacitance C_{BE} increases with the emitter window coherently with the junction widening. Base-collector capacitance C_{BC} is on the other hand steady, confirming that the junction is not affected by the experiment. Considerations on capacitances validate what concluded on breakdown voltages.

Table III.20 | Parasitics extracted on HBTs featuring different effective emitter window widths. Capacitances from $0.2 \times 5\ \mu m^2$ reference devices. Resistances extracted from measurements on dedicated structures.

	W_{E0}	80	100	110
R	E (Ω)	8.4	7.2	7.0
	B_{tot} (Ω)	61	66	76
	sBI ($k\Omega/sq$)	5.8	5.9	6.6
	B_x (Ω/sq)	593	675	621
C	BE (fF)	7	8	9
	BC (fF)	5	5	5

Table III.21 reports maximum frequencies obtained for each W_{E0} on golden dies chosen among tested devices. Transit frequencies f_T remain steady around the value of 300 GHz, confirming that the vertical doping profile regulating transit time is unaffected by the effective emitter window width. The impact of parasitics results negligible.

Table III.21 | Transit and maximum oscillation frequencies extracted on HBTs featuring different effective emitter window widths. $0.2 \times 5\ \mu m^2$ reference devices, V_{BC} = -0.5 V.

W_{E0}	80	100	110
f_T	301	298	300
f_{MAX}	381	392	402

In conclusion, different values of effective emitter window width W_{E0}

spanning from 80 nm up to 110 nm have been tested by modifying the emitter spacers sizing. Considered the compromise between current leakages and maximum frequencies, the best value of W_{E0} is 100 nm.

4.2 Future studies

As said in the introduction of this section, emitter doping has not been for the moment investigated as no particular problem linked to this aspect has been highlighted. Further investigations will have to consider different arsenic concentrations or more complex doping profiles, trying to enhance the emitter-base junction and further reduce emitter resistance. A two-step doping profile could for example allow to decorrelate emitter-base junction tuning from emitter resistance minimization.

Some studies on the deposition chemistry (not detailed here) have been performed to increase the growth rate and therefore reduce the process time required for realizing the emitter. Another possible advantage of optimizing the deposition chemistry could be to further reduce process temperatures. In both cases, dopant diffusion could be reduced leading to more abrupt base doping profile and consequent transit time improvement.

A big part of the results detailed in this work are affected by the presence of a perimetric junction leading to current leakages, degradation of breakdown voltages and increased capacitances. Optimization of the emitter spacers showed that these undesired effects can be reduced to a some point but base resistance will increase consequently. As simple solution would be to shift the SiCAP above the emitter spacers, avoiding any perimetric effect. Considering the current integration, such solution would lead to an important increase in base resistance, degrading f_{MAX} which is still below the targeted value. A total redesign of the emitter integration could allow to overcome this limitation of the EXBIC architecture.

5 Load-pull measurements

Load-pull measurements allow to understand how the device is capable of delivering power to an optimized load at high frequency. The Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN) of Lille disposes of knowledge and tools able to perform such evaluations. [1] These are the first load-pull measurements ever performed on an EXBIC HBT and will define the reference for future studies.

On a 94 GHz load-pull measurement bench, different devices have been tested to evaluate the technological innovations described in this chapter. Input impedance matching is performed for every tested device in order to maximize power absorption and have a common ground for comparing measured performances.

First, the wafer is mapped to identify a good site for the measurement. Devices are standard 0.2×0.5 μm^2 transistors identical to those used for f_T/f_{MAX} measurements. Once the good transistor is found, a first round of testing scans multiple values of load impedance for a fixed -5 dBm input power level. In this way, the load is matched and the device is capable of delivering its maximum power. The optimal polarization is then sought, targeting to maximize power added efficiency PAE. Output power at maximum efficiency $P_{OUT}@PAE_{MAX}$ and power gain G_p are evaluated in these polarization conditions. The output power at 1 dB compression $P_{OUT} - 1dB$ is also evaluated to obtain an idea of the maximum power deliverable by the device and the corresponding $P_{ABS} - 1dB$ allows to evaluate input power withstanding.

Four different devices, each one featuring distinct integrations, have been selected for this analysis:

Device 1 An improved version of a B55 DPSA-SEG featuring f_T/f_{MAX} of 350/360 GHz

Device 2 One of the first devices integrated with the 1-step extrinsic base; f_T/f_{MAX} = 340/335 GHz

Device 3 An optimized 1-step-extrinsic-base device with f_T/f_{MAX} = 380/350 GHz

Device 4 A partially-optimized device featuring the Go To EXBIC architecture with f_T/f_{MAX} = 384/396 GHz

[1] The author wishes to thank Etienne Okada for the measurements.

Such selection is supposed to allow to understand the consequences of architecture or process modifications on power behavior of the device and eventually define new paths for improvement. Indeed, development is primarily oriented toward the increase of maximum frequencies and power behavior is mostly a consequence of improvements on other figures of merit.

Table III.22 reports both setup and measured values of load-pull measurements obtained on tested devices.

V_{CE} has been kept constant at 1.8 V to allow an easy comparison between devices. V_{CE} is on the other hand correspondent to the best biasing condition found for each device. The progressive increase in V_{CE} is related to the self-polarization phenomenon induced by device parasitic resistances due to voltage biasing. This value corresponds to the f_T peak shift observable on device characteristics and linked to the high-injection effects. Optimal impedances Z have been optimized in combination with bias voltage in order to perfectly match the load. Differences reflect variations in device architecture affecting the correspondent scattering matrix.

Table III.22 | Optimal bias and impedance of HBTs featuring different integrations. Currents are a consequence of the imposed voltages. 0.2×0.5 μm^2

	Device 1	Device 2	Device 3	Device 4
V_{CE} (V)	1.8	1.8	1.8	1.8
V_{BE} (V)	0.81	0.83	0.84	0.84
I_C (mA)	9.6	9.5	10.3	9.5
I_B (μA)	59	22	18	9
$\|Z\|$ (Ω)	0.7	0.7	0.65	0.8
$\angle$Z	116	120	115	135

Figure III.12 shows the output power P_{OUT} as a function of input absorbed power P_{ABS} and Figure III.13 the consequent gain G_p.

Device 4 exhibits a power gain G_p about 30% lower compared to other devices, which in turn have very similar values. Recalling the definition of maximum oscillation frequency (Chapter I Section 2.6), higher values of f_{MAX} should be related to higher power gain. A closer look to the setup used for f_{MAX} measurement shows that the peak was obtained at higher V_{BE} voltage compared to other devices (0.9 V), meaning that better gain

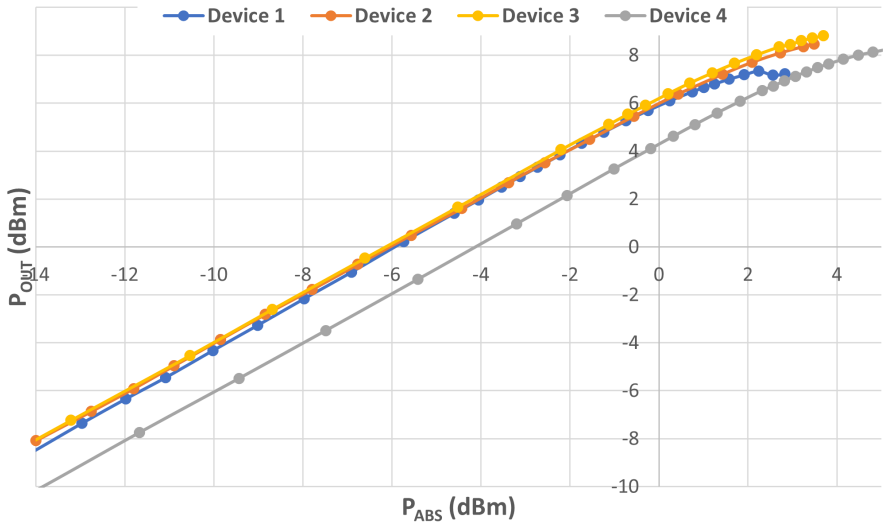

Figure III.12 | Output power P_{OUT} as a function of input absorbed power P_{ABS} measured on 0.2×0.5 μm^2 DPSA-SEG and EXBIC transistors.

could be obtained refining the setup. Measurements have to be performed again with a modified setup in order to maximize the gain.

Observing the output power at 1 dB compression $P_{OUT} - 1dB$ reported in Table III.23, some considerations on the architecture can be done. Device 1, consisting in a DPSA-SEG HBT, delivers the lowest power. Previous studies [24] clearly showed the impact of isolation structures on the ability of evacuating heat from the structure. An increase in device temperature has a detrimental effect on carriers mobility, degrading the overall performance. In accordance with that, Devices 2 and 3 increase the value of $P_{OUT} - 1dB$. The difference between these two transistors can be explained with the reduction of parasitics, in particular R_B, obtained thanks to the optimization of the 1-step extrinsic base. Device 4, consisting in a GoTo EXBIC, slightly reduces the value of $P_{OUT} - 1dB$. Even if the structure has lower parasitics compared to Devices 2 and 3, the new single-trench SSTI integrated on this device appears to have a detrimental effect. Notice also that Device 4 is capable to withstand higher values of P_{in} with respect to other devices in these bias conditions. This could be an interesting characteristics for circuit design, implying higher robustness and eventually avoiding the need for circuit protection. Imagining that a better gain G_p could be obtained with a correct setup, it is also possible that this transistor could deliver better

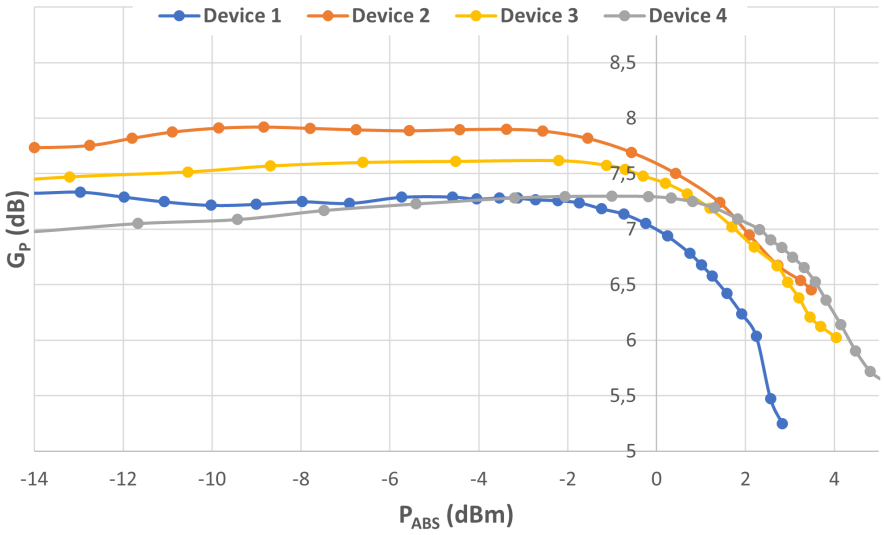

Figure III.13 | Power gain G_p as a function of input absorbed power P_{ABS} measured on 0.2×0.5 μm^2 DPSA-SEG and EXBIC transistors.

values of P_{OUT} compared to other devices. Sub-otimal biasing of Device 4 requires however a new round of measurement to assure that obtained values are actually comparable to those of other devices.

Figure III.14 reports the Power Added Efficiency (PAE) obtained on the four devices. Recalling the equation used for the definition of this figure of merit (cf. Equation (I.10)), a higher gain G_p is generally related to higher efficiency. Measured PAE values show however some differences with what observed on Figure III.13. Device 1 shows the lowest efficiency, followed by Device 4 which is capable to increase its efficiency by 3% in spite of his way lower power gain. Devices 2 and 3 are very close, with the first slightly better. The difference can be attributed to different DC power consumption, i.e. the power absorbed by the device for its operation in the specified bias point. This conclusion is confirmed observing the current values listed in Table III.22, indicating way different power consumption between the tested devices.

Values of $P_{OUT}@PAE_{MAX}$ and $G_p@PAE_{MAX}$ listed in Table III.23 confirm the tendencies observed for $P_{OUT} - 1dB$. Once again, the sub-optimal biasing of Device 4 limits the possible conclusions. A better setup leading

to higher gain G_p would imply higher values of P_{OUT} and a better PAE. If confirmed higher current gain implying lower DC power consumption would imply a consequent great improvement.

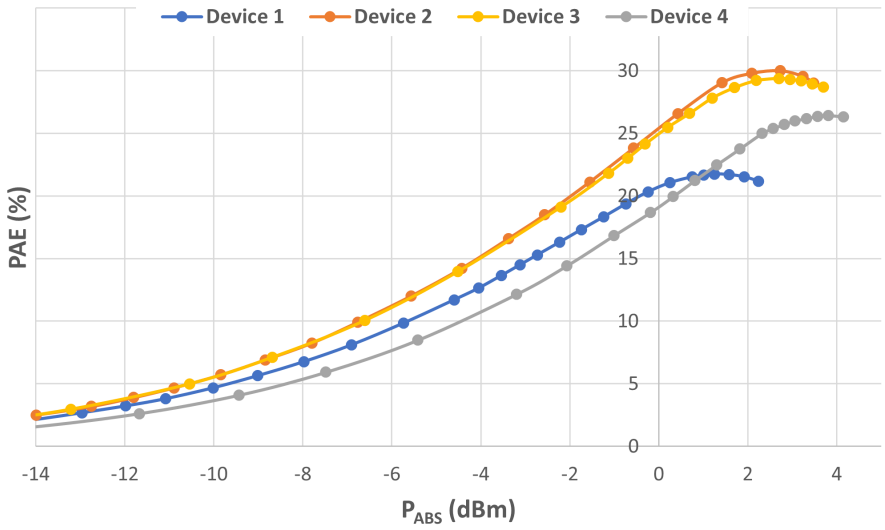

Figure III.14 | Power Added Efficiency PAE as a function of the input absorbed power P_{ABS} measured on 0.2×0.5 μm^2 DPSA-SEG and EXBIC transistors.

In conclusion, load-pull measurements compared a B55 DPSA-SEG HBT with three EXBIC HBTs representing different development steps. EXBIC transistors show clear advantages both in terms of output power P_{OUT} and power added efficiency PAE. Devices featuring a 1-step extrinsic base and ring SSTIs lead to the highest power gain G_p. The GoTo EXBIC HBT requires closer look to the measurement setup since results suggest that a better biasing could be used, leading to improvements on all figures of merit.

Considering the additional optimizations of the GoTo EXBIC architecture suggested in this chapter, better performances are expected in future. Even if the obtained results already demonstrate considerable improvements with respect to the DPSA-SEG architecture, a device capable of delivering target B55X performances is required for a definitive comparison.

Table III.23 | Results of load-pull measurements on 0.2×0.5 μm^2 DPSA-SEG and EXBIC transistors.

	Device 1	Device 2	Device 3	Device 4
f_T	350	340	380	384
f_{MAX}	360	335	350	396
$P_{OUT} - 1dB$ (dBm)	7.2	8.4	8.7	8.1
$P_{ABS} - 1dB$ (dBm)	1.9	3.2	3.4	4.8
$G_p@P_{OUT} - 1dB$ (dBm)	5.26	5.11	5.27	3.32
PAE_{MAX} (%)	23	30	29	26
$P_{OUT}@PAE_{MAX}$ (dBm)	6.8	8.4	8.4	7.6
$G_p@PAE_{MAX}$ (dB)	5.6	5.4	5.7	3.8

6 Optimization conclusion

Optimization studies presented in this chapter allowed to better understand the GoTo EXBIC architecture in the effort of reaching target performance of $f_T/f_{MAX} = 400/500$ GHz with $BV_{CEo} = 1.35$ V for the B55X technology.

Figure III.15 shows the performance progression in terms of f_T and f_{MAX} obtained during the optimization process and compares it with the results obtained on the first lot featuring GoTo devices.

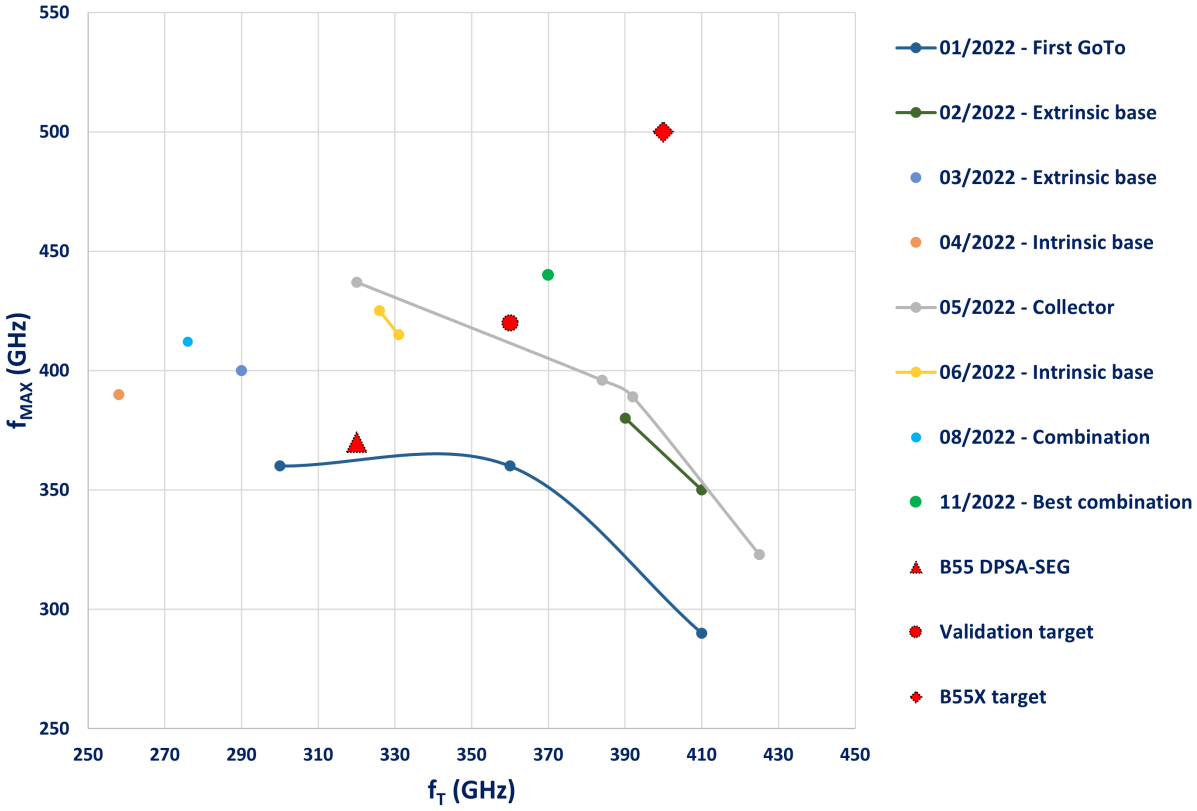

Figure III.15 | Chronological performance progression of best f_T/f_{max} for each lot produced in the optimization phase. $0.2 \times 5\ \mu m^2$ reference devices.

In the last 7 months of development, one lot per month has been produced to address each aspect detailed in this chapter. For comparison, 11 electrically-functional lots have been produced in more than two years during

the architecture review phase. Seen the limited time that could be dedicated to the optimization of the EXBIC HBT, results are comprehensibly not sufficient for reaching targeted f_T/f_{max}.

Results of the studies presented in this chapter allowed however to understand many aspects of the GoTo EXBIC architecture which can be resumed as follows:

Collector: Carbon energy and phosphorus dose can be tuned to minimize collector resistance

With enough phosphorus, the base-collector junction can be tuned with minimum variations of collector resistance

Variation of epitaxial collector thickness can have a strong impact both on perimetric effects and spacers sizing

Extrinsic base: Sizing and boron concentration are the most important parameters for resistance reduction

Optimization is limited by boron diffusion in the intrinsic base

Intrinsic base: Increase in boron concentration combined with profile shrink are beneficial

Boron could be better positioned with respect to germanium

Emitter: Spacers can be sized to regulate base current leakages

Due to its very complex doping profile, the base could not be completely studied and is now the hot topic for development. Thanks to the acquired knowledge, other parts of the device will eventually require an additional little adjustment when the final base doping profile will be set.

Intending to combine all the acquired knowledge, a lot has been produced integrating all the improved features presented in this chapter. Completed in august 2022, this lot could not deliver the expected results since it was affected by the excessive collector thickness described in Chapter III Section 1.3. A lot featuring the same splits but without the collector flaw has been successively produced, allowing to reach validation targets in november 2022.

Table III.24 compares technology target values, industrialization minimum values and results obtained on final silicon. While current gain, Early

voltages and breakdown voltages have been set for application needs, parasitics are defined through device modeling in order to assure target f_T/f_{max}. Results show that, even if f_T and f_{max} values are only slightly above the validation target, the other figures of merit are all well within the specifications and in some cases are even already fulfilling for the final technology performance. A glimpse to parasitics shows that, in the scope of improving maximum frequencies, R_B and C_{BC} minimization is still a challenge for future developments.

Table III.24 | Comparison of target values defined for main figures of merit and the ones obtained on the best silicon produced within this work.

NPN CBEBC $0.2 \times 5\ \mu m^2$		B55X targets	Validation target	Last silicon
Frequencies	f_T	400	> 360	370
	f_{MAX}	500	> 420	440
Current gain	$V_{BE} = 0.7\ V$	2250	> 650	2200
V_A	F (V)	100	> 50	105
	R (V)	1.4	> 1.2	1.37
BV	CBo (V)	4.5	> 4.1	5.1
	CEo (V)	1.44	> 1.3	1.48
R	E normalized ($\Omega/\mu m^2$)	1.5	< 1.8	1.6
	B_{TOT} (Ω)	18	< 26	25
	sBI ($k\Omega/sq$)	4	< 6	4
	Bx ($\Omega \cdot \mu m$)	40	< 70	40
	sBL (Ω/sq)	50	< 60	50
C	BC normalized (fF/μm^2)	7.6	< 8.5	8.1
	BC normalized (fF/μm^2)	20	< 23	19

Even if the GoTo EXBIC architecture was meant to achieve better f_{MAX} than the DPSA-SEG thanks to its lower parasitics, some limitations have been observed. In particular, the reduction of R_B is often compensated by the increase of C_{BC} and the onset of current non-idealities. While the collector-base junction is mostly affected by parasitic capacitances due to boron diffusion from the base, the emitter-base junction undergoes more complex bidimensional effects linked to arsenic diffusion below the spacers in

the SiCAP. A review of both of the emitter and collector integration could allow to decrease base resistance without the annoying contribution of negative effects.

Chapter IV

Conclusion

The developments and relative results presented in this work are here resumed.

A chronological presentation of the electrical results allows to understand the timing spent on each aspect of the development process.

Future studies are listed for reaching and exceeding the target BiCMOS055X performance.

The main objective of this work was to produce a Heterojunction Bipolar transistor (HBT) with the Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) architecture, reaching state-of-the-art performance of f_T/f_{MAX} = 400/500 GHz with BV_{CEo} = 1.35 V and considering the constraints of industrial fabrication on a 300 mm production line. The new HBT architecture is developed in the scope of the next STMicrolectronics BiCMOS technology based on a 55 nm CMOS platform: BiCMOS055X.

Figure IV.1 shows the progression in terms of f_T and f_{MAX} obtained on all the functional lots produced within this study.

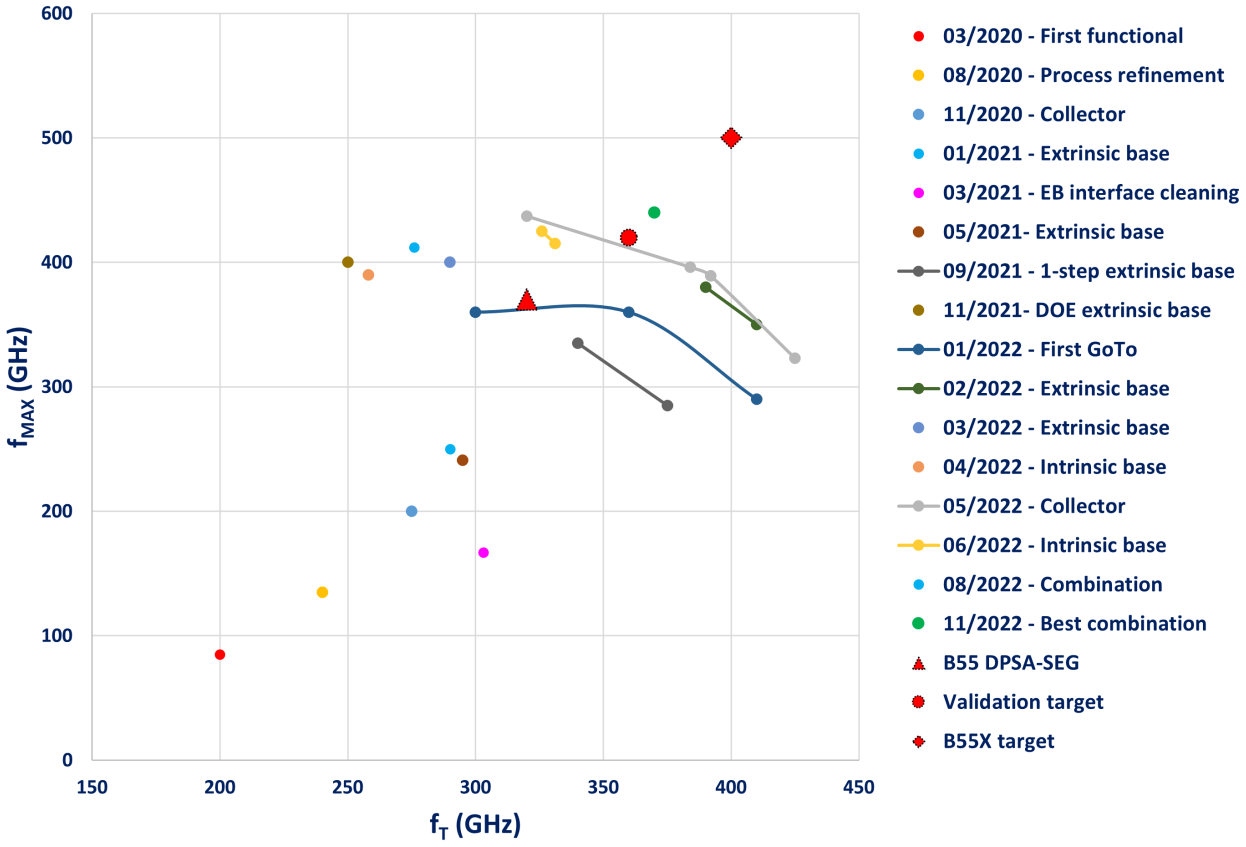

Figure IV.1 | Best f_T/f_{MAX} of all the functional lots produced within this work. Values obtained on reference 0.2×0.5 μm^2 transistors.

Thanks to two previous PhDs dedicated to the investigation of possible

evolutions of STMicroelectronics' DPSA-SEG HBT architecture [63, 23], the the preliminary EXBIC architecture has been defined at the beginning of this study. The EXBIC architecture is designed to overcome the limitation of the DPSA-SEG by addressing base resistance R_B which is the main parasitic limiting f_{MAX} increase. After almost an year of manufacturing tests, the first functional device has been realized, allowing to start the architecture review process.

Considerations on manufacturability and architecture evaluation through the analysis of electrical figures of merit were the main axes on which the architecture review process has been directed in almost two years of development, leading to the definition of the GoTo EXBIC architecture. The two most important advancements of this phase are the 1-step extrinsic base integration and the single-trench SSTI. The extrinsic base redesign allowed to obtain a more robust integration unaffected by many parasitic effects observed with the 2-step integration thanks to an important simplification in the fabrication process. The single SSTI integration allows better alignment between the newly-introduced SSTI and the rest of the device, allowing to further reduce parasitic base-collector capacitance while ensuring a more robust integration. Other important results of this phase are the improvement of the emitter-base interface cleaning process and the investigation of defect-generating mechanisms in the implanted collector. At the end of this phase, performance achieved with the B55 DPSA-SEG were already outdone thanks to f_T/f_{MAX} = 360/360 GHz with BV_{CEo} = 1.43 V. Figure IV.2 witnesses the results of this architecture review by comparing TEM cross-sections of a B55 DPSA-SEG, a preliminary EXBIC and a GoTo EXBIC HBT.

The production of the first functional GoTo device allowed to start the second phase of this work oriented on performance optimization. The studies performed in the last 7 months led to further improvements and better understanding of the device, resulting in f_T/f_{MAX} = 370/440 GHz with BV_{CEo} = 1.48 V obtained on the last device produced combining all the acquired knowledge. Even if a good overall increase in performance has been obtained with respect to the first devices, such results could not achieve targeted values of f_T/f_{MAX} = 400/500 GHz with BV_{CEo} = 1.35 V for the final device and further improvements are needed. Validation targets have however been hit, allowing to begin the considerations for a future industrialization of this technology.

Many axes of improvement have been defined and will be investigated in the coming months to fill the gap of 20 GHz f_T and 110 GHz f_{MAX}.

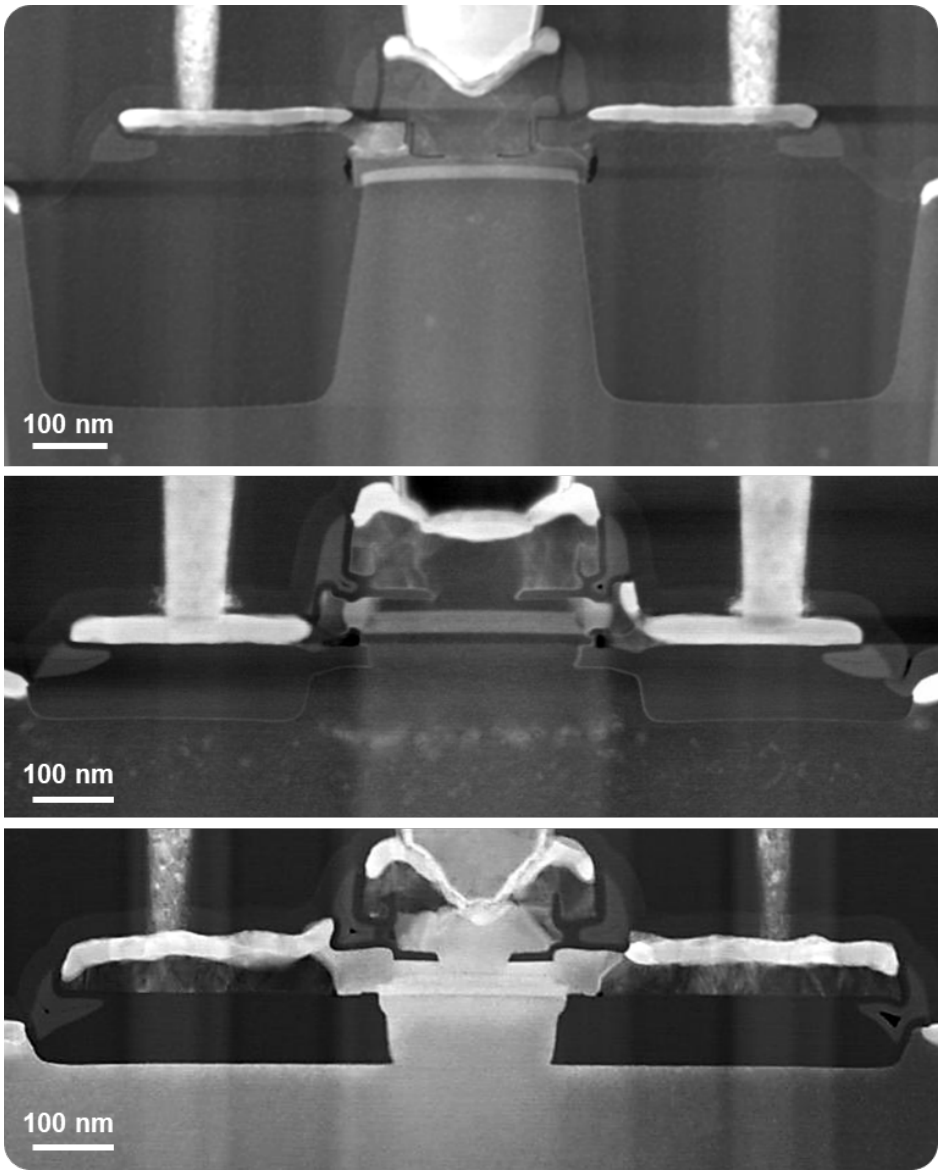

Figure IV.2 | TEM cross sections of HBTs. From top: B55 DPSA-SEG, preliminary EXBIC and GoTo EXBIC

Due to its very complex doping profile, the intrinsic base is yet to be optimized. Germanium doping profile and boron placement with respect to it must be better investigated for maximizing the high-frequency behavior. If on one side the germanium profile could be simplified, some new features could enhance its effect. Multiple lots addressing these questions are already being produced, ideally allowing to demonstrate a refined base profile in the coming months. The intrinsic base profile is at this point considered the main issue limiting performance.

Collector improvement will focus on the refinement of the epitaxial process in order to reduce thickness variability which has been shown to have a critical impact on performance. An adjustment of phosphorus dose will eventually be required once the base profile will be set.

Thanks to its 1-step integration, the extrinsic base can be considered mature and requiring only some further tuning when the other parts will be finally defined.

The emitter has been impacted in a minor way by this study due to its relatively simple integration. The impact of different emitter spacers is understood and an adjustment may be required once the intrinsic base profile will be set.

Even if not part of this work, a study on the co-integration of multiple HBTs featuring different $f_T \times BV_{CEo}$ products is required to match the offer available for the BiCMOS055 technology.

In the effort of reaching the maximum performance of $f_T/f_{MAX} = 400/600$ GHz with $BV_{CEo} = 1.35$ V expected for an EXBIC HBT, more advanced studies are defined.

Regarding the collector, advanced in-situ doping and more complex integrations will be investigated to reduce the important perimetric base-collector capacitance due to boron diffusion from the extrinsic base.

Some advanced studies on extrinsic base doping could be useful for limiting boron diffusion in the intrinsic device while minimizing the extrinsic component of base resistance.

More complex emitter doping profiles could be used for tuning the emitter-base junction and reducing emitter resistance independently. A review of the emitter integration could be useful in the scope of suppressing perimetric effects linked to arsenic diffusion in the base SiCAP.

Looking beyond the scope of this work, it is important to remember that the EXBIC architecture has been originally designed for being integrated

on SOI wafers and be compatible with STMicroelectronics' 28 nm FD-SOI CMOS platform (Cf. Chapter I Section 4.2). Even if these features were not included in this work, the interest for such application is still strong. Future advanced research projects will focus on this topic.

Appendix A

Modeling methods

1 Current components

Recalling Equation (I.1), currents of an ideal device depends on the junction area. A real HBT is a three-dimensional device where parasitic effects can occur on the sides of the junction and their impact on the overall current will depend on the junction perimeter. Currents can therefore be modeled as the sum of a surfacical and a perimetric component, each one dependent on junction geometry:

$$I = I_{surf} \times A + I_{perim} \times P \tag{A.1}$$

Where I is a current (base or collector), I_{surf} the surfacical component, A the junction surface, I_{perim} the perimetric components and P the junction perimeter.

The formula can be inverted to have an explicit dependence on the perimeter:

$$\frac{I}{A} = I_{surf} + I_{perim} \times \frac{P}{A} \tag{A.2}$$

Since device geometry is known by design and currents can be measured, it is possible to plot the points of Equation (A.2) to obtain the surfacical and perimetric components of current. Parameters will be obtained from the line extracted by the least squares method.

2 Sheet resistance

Resistance of a conductor can be described as:

$$R = \frac{L}{HW}\rho = \frac{L}{HW}\frac{1}{\sigma} \tag{A.3}$$

where L, H and W are the conductor length, height and width respectively; ρ the material resistivity and σ the material conductivity.

A conductor is called thin film when $H \ll L, W$, i.e. its thickness is negligible when compared to the other dimensions. Sheet resistance R_s is commonly used in these cases for expressing the electic properties of the material:

$$R_s = R\frac{W}{L} = \frac{\rho}{H} = \frac{1}{\sigma H} \tag{A.4}$$

Taking a n-doped wafer of net dopant vertical distribution $N(x)$, the electric conductivity in each point $\sigma(x)$ can be expressed as:

$$\sigma(x) = eN(x)\mu_e(x) \tag{A.5}$$

where e is the electron charge and $\mu_e(x)$ the electron mobility at depth x.

From Equation (A.3) we can express the infinitesimal resistance $dR(x)$ of the thickness (height H) comprised between x and $x + dx$ as:

$$dR(x) = \frac{L}{W}\frac{\rho(x)}{dx} = \frac{L}{W}\frac{1}{\sigma(x)dx} \tag{A.6}$$

Following Equations (A.4) and (A.5) the total sheet resistance R_S for a given dopant distribution can be expressed as:

$$R_s = \frac{1}{e\int_0^{x_j}\sigma(x)dx} = \frac{1}{e\int_0^{x_j}N(x)\mu_e(x)dx} \tag{A.7}$$

where x_j is the junction depth in the substrate.

3 Collector resistance

Figure A.1 depicts a representation of an HBT collector with contacts C_1 and C_2 on the two sides. Contacts are biased with a voltage $V_{C_1C_2}$ and the resulting current I_C is measured.

By means of Ohm's current laws, the extrinsic collector resistance R_{Cx} can be expressed in this model as:

$$R_{Cx} = \frac{V_{C_1C_2}}{I_C} = 2R_{sinker} + R_{BL} \tag{A.8}$$

where R_{sinker} is the resistance of each sinker and R_{BL} is the buried layer resistance, each measured in Ω.

Going deeper into the model, device geometry can be taken into account:

$$R_{Cx} = 2\frac{R_{sK}}{W_S W_{BL}} + R_{sBL}L_{BL} \tag{A.9}$$

Where R_{sK} is the sinker specific resistance in $\Omega \cdot \mu m^2$, W_S the sinker width, R_{sBL} the sheet resistance of the buried layer in $\Omega/\mu m^2$ ans L_{BL} the buried layer width.

Multiple R_{Cx} measurements performed on various device geometries can be fitted with a line by using the least squares method. The resulting line corresponds to the following equation:

$$R_{Cx}W_{BL} = 2\frac{R_{sK}}{W_S} + R_{sBL}L_{BL} \tag{A.10}$$

Resistance components can be obtained by the parameters of the equation fitting the measured extrinsic resistance R_{Cx} values:

$$\begin{cases} R_{sBL} = slope \\ R_{sK} = \frac{intercept \times W_S}{2} \end{cases} \tag{A.11}$$

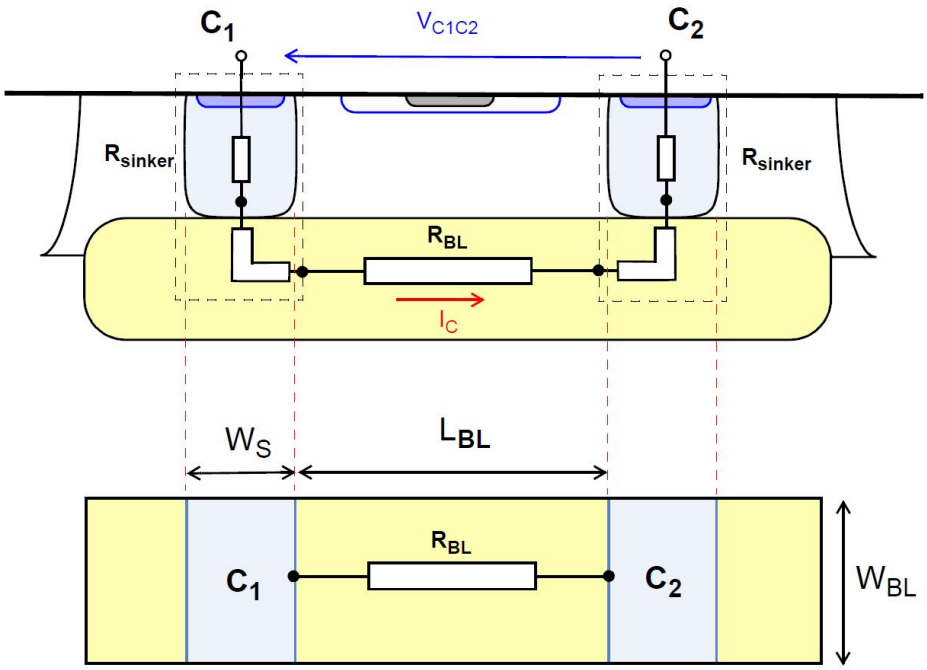

Figure A.1 | Schematic describing the model used for extracting the sinker and buried layer components of the collector resistance R_C. Courtesy of Didier Céli.

4 Base resistance

Referring to Figure A.2, the total base resistance R_B can be modeled with the following equation:

$$R_B = 2R_{sBx} + R_{sBI}\frac{W_{E0}}{L_E} \tag{A.12}$$

where R_{sBx} is the extrinsic base specific resistance in Ω/sq; R_{sBI} the intrinsic base sheet resistance in Ω/sq; W_{E0} the effective width of the emitter window; L_E the emitter length.

Parameters d, γRBI, W_{SP}, W_{BX} and W_{link} depicted in Figure A.2 are all correction factors accounting for the contribution of spacers, emitter diffusion in the base ans silicidation. W_{E0} can be obtained from W_E choosing one of this factors k and subtracting their width ($L_{E0} = L_E - 2k$). Even if a similar reasoning can be applied to L_E, the contribution of the correction factor is considered negligible. Similarly to what seen for collector resistance, measuring base resistance at different emitter window widths and lengths allows to obtain both R_{sBx} and R_{sBI} components. For a standard device, the correction factor k is set so that $W_E = 2W_{E0}$.

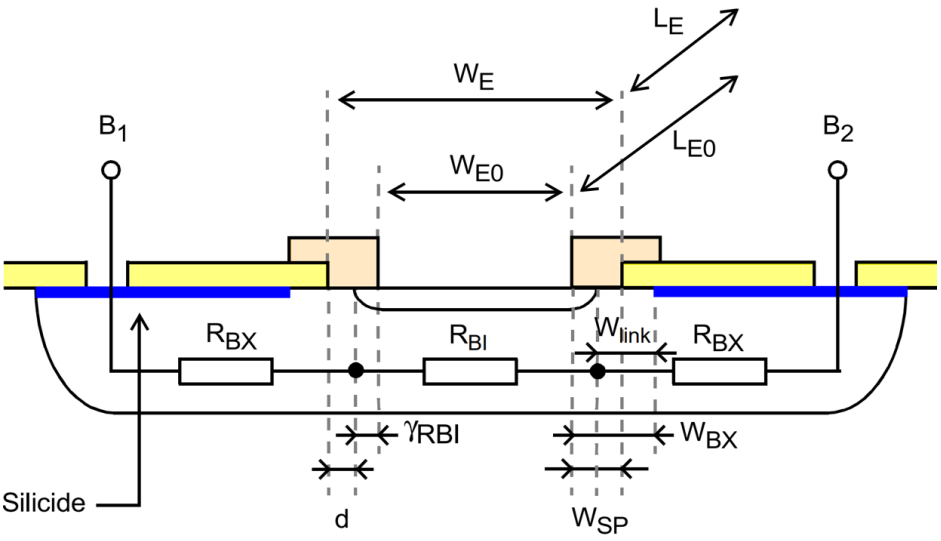

Figure A.2 | Schematic describing the model used for extracting the base resistance R_B components. Courtesy of Didier Céli.

Authors' publications

International conferences

- E. Brezza et al. "Optimized emitter-base interface cleaning for advanced Heterojunction Bipolar Transistors." European Material Research Society 2021 Fall Meeting

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- F. Deprat, J. Vives, M. Juhel, A. Valery, L. Justine, E. Brezza et al. "Investigation of Arsenic Transient Enhanced Diffusion From Emitter Process at 550 C Si: As RP-CVD Epitaxy Using Disilane Precursor". In: ECS Transactions 109.4 (2022), p. 159

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- E. Brezza et al. *Method for manufacturing a bipolar transistor and bipolar transistor capable of being obtained by such a method.* US Patent 11,417,756. 2022

- E. Brezza and A. Gauthier. *Bipolar transistor and manufacturing method.* US Patent App. 17/503,621. 2022

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Submitted papers

- E. Brezza et al. "Heterojunction bipolar transistor featuring a stressed implanted collector: defects formation and impact on functionality" . Microelectronics Reliability

- E. Brezza et al. "Optimized emitter-base interface cleaning for advanced Heterojunction Bipolar Transistors." Solid-State Electronics

Filed patents

E. Brezza et al. *Technique for doping an epitaxial collector*

J. Borrel, A. Gauthier, F. Hilario, L. Berthier, P. Dumas et E. Brezza. *Dummies for Implant Mask*

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Résumé

Le développement de la technologie BiCMOS055X de STMicroelectronics, une technologie BiCMOS basé sur un noeud CMOS 55 nm compatible avec une ligne de production 300 mm, requiert le développement d'une nouvelle architecture de Transistor Bipolaire à Hétérojonction (TBH). L'architecture *Epitaxial eXtrinsic Base Isolated from the Collector* (EXBIC) a été choisie en visant des valeurs de $f_T = 400$ GHz et $f_{MAX} = 500$ GHz avec une tension de claquage émetteur-collecteur $BV_{CEo} \geq 1.35$ V pour cette technologie.

Après la réalisation d'un premier dispositif fonctionnel, un plan d'amélioration est défini. Les différents aspects de la fabrication sont considérés afin de réduire la complexité du dispositif et améliorer sa robustesse. La performance électrique est améliorée à chaque introduction d'une nouvelle modification. Des nouvelles intégrations de collecteur et base extrinsèque sont proposées, ainsi définissant une nouvelle version de TBH EXBIC.

Sur l'architecture EXBIC améliorée, un procédé d'optimisation a été mené afin de régler les paramètres de chaque partie du composant. Les études ciblent l'amélioration des profils de dopage et la réduction des résistances parasites.

Les valeurs de $f_T \approx 380$ GHz et $f_{MAX} \approx 390$ GHz avec $BV_{CEo} = 1.4$ V atteintes sur le meilleur dispositif produit sont encore insuffisantes pour les exigences de la technologie BiCMOS055X. Des études futures sont définies afin de pouvoir atteindre et dépasser les performances souhaitées.

Abstract

The development of STMicroelectronics' BiCMOS055X technology, a next-generation BiCMOS technology based on a 55 nm CMOS node compatible with a 300 mm production line, requires the development of a new Heterojunction Bipolar Transistor (HBT) architecture. The Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) architecture has been chosen, aiming values of $f_T = 400$ GHz and $f_{MAX} = 500$ GHz with an emitter-collector breakdown voltage $BV_{CEo} \geq 1.35$ V for this technology.

After the realization of a first functioning device, a path for improvement is defined. Fabrication aspects are investigated, reducing device complexity and improving robustness. Electrical performance is steadily improved with the introduction of each new feature. New collector and extrinsic base integrations are proposed, defining an improved version of the EXBIC HBT architecture.

On the improved EXBIC architecture, an optimization process has been carried out by tuning the parameters of each device component. Studies target improved doping profiles and parasitic resistances reduction.

Best performances of $f_T \approx= 380$ GHz and $f_{MAX} \approx 390$ GHz with $BV_{CEo} = 1.4$ V could however not reach the values aimed for BiCMOS055X. Future studies are defined for reaching and trespassing targeted performance.