THESE

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Par

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Integrated Metrology Devices for The Study of Transport Properties in Silicon Nanostructures

Towards a direct zT metrology based on the transient Harman technique

Dispositifs de Métrologie Intégrée pour l'Etude des Propriétés de Transport dans les Nanostructures en Silicium

Vers une métrologie directe de zT basée sur la technique transitoire de Harman

Soutenue le 29 novembre devant le jury composé de :

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Mille Mercis

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أود أن أعبر عن امتناني العميق لوالديّ، الأب الحبيب **الحسين** الذي عمل بجد من أجلنا وساهم ماليًا في إكمال دراستي
،ولوالدتي، الأم الحنونة **فاضمة**، التي قدمت تضحيات كبيرة في حياتها لنحقق أعلى المراكز والإنجازات .هذا الإنجاز ليس فقط إنجازي
بل إنجاز هما أيضًا

إلى أمي، **فاضمة**، أريد أن أقول شكرًا لك على كونك أمًا، شقيقة، وصديقة لي .لقد كنتِ أكثر من مجرد دعم قوي، بل كنتِ شريكة في
هذا العمل بكل المعاني

Integrated Metrology Devices for The Study of Transport Properties in Silicon Nanostructures. Towards a direct *zT* metrology based on the transient Harman technique.

In thermoelectricity, silicon nanostructures represent an interesting alternative to conventional thermoelectric materials due to Si abundance, non-toxic nature, and its compatibility with CMOS technology. Researchers have investigated methods to enhance the silicon figure of merit *zT* by increasing the σ/κ ratio; decreasing the thermal conductivity κ by (i) using nanometric structure such as thin membranes or nanowires, (ii) roughening, (iii) oxidization of the surface achieved relatively low value of κ. Yet, few experimental measurements of *zT* in crystalline silicon nano-objects were presented with important data dispersion. Usually, the thermoelectric figure of merit is obtained through independent measurement of materials transport properties (κ, σ and *S*). The uncertainty of *zT* can easily reach 50% considering that each parameter has an uncertainty of 5% to 20%. Harman's technique is a simple and rapid method to measure *zT* directly in bulk materials. This thesis proposes an adaptation of the transient Harman technique for suspended crystalline nano-membranes. A correction factor is introduced to account for radiation, contact resistances, and Joule heating effects. Furthermore, a device implementation is presented, enabling direct access to *zT* through purely electrical measurements, eliminating the need for separate measurements of transport parameters. Additionally, elementary devices are examined to determine the transport properties of silicon, including thermal conductivity, Seebeck coefficient, and electrical conductivity. The measured Seebeck coefficient, showing similarity to Bulk Si near room temperature, raises a fundamental question concerning the relative contributions of electron diffusion and phonon transport.

Dispositifs de Métrologie Intégrée pour l'Etude des Propriétés de Transport dans les Nanostructures en Silicium. Vers une métrologie directe du *zT* basée sur la technique transitoire de Harman.

En thermoélectricité, les nanostructures de silicium représentent une alternative intéressante aux matériaux thermoélectriques conventionnels en raison de leur abondance, de leur caractère non toxique et de leur compatibilité avec la technologie CMOS. Les chercheurs ont étudié différentes méthodes visant à améliorer le facteur de mérite *zT* du silicium en augmentant le rapport σ/κ ; en diminuant la conductivité thermique κ en utilisant (i) des structures nanométriques telles que des membranes minces ou des nano-fils, (ii) en utilisant la rugosité de surface, (iii) en procédant à une oxydation de la surface, ce qui permet d'obtenir une faible valeur de κ. Cependant, peu de mesures expérimentales de *zT* sur des nano-objets en silicium cristallin ont été présentées, et ces données présentent une dispersion importante. Habituellement, le facteur de mérite est obtenu par une mesure indépendante des propriétés de transport des matériaux (κ, σ et S). L'incertitude de *zT* peut facilement atteindre 50 %, étant donné que chaque paramètre présente une incertitude de 5 % à 20 %. La technique de Harman est une méthode simple et rapide pour mesurer directement *zT* dans les matériaux bulk. Cette thèse propose une adaptation de la technique de Harman transitoire pour les nano-membranes cristallines suspendues. Un facteur de correction est introduit pour prendre en compte les effets du rayonnement, des résistances de contact et du chauffage par effet Joule. De plus, une mise en œuvre du dispositif est présentée, permettant d'accéder directement à *zT* par des mesures purement électriques, éliminant ainsi le besoin de mesures séparées des paramètres de transport. De plus, des dispositifs élémentaires sont examinés pour déterminer les propriétés thermiques du silicium, notamment la conductivité thermique, le coefficient de Seebeck et la conductivité électrique. Le coefficient Seebeck mesuré, montrant une similitude avec le Si bulk près de la température ambiante, soulève une question fondamentale concernant les contributions relatives de la diffusion des électrons et du transport des phonons.

General Introduction

Thermoelectricity, the conversion of heat fluxes into electrical energy, holds immense potential for sustainable energy harvesting and waste heat recovery. In this context, silicon nanostructures emerge as a captivating avenue due to their abundant availability, non-toxic nature, and compatibility with CMOS technology. Unlike conventional thermoelectric materials, silicon offers unique advantages. This thesis investigates the utilization of silicon nanostructures in thermoelectric applications, with a focus on enhancing silicon's thermoelectric characteristics and developing a precise efficiency measurement technique.

In the field of thermoelectricity, silicon nanostructures are being explored as a promising alternative to traditional thermoelectric materials. Silicon possesses a relatively high Seebeck coefficient (S), around 400µV/K, but its thermal conductivity (κ) is relatively high, approximately 149W/mK near room temperature, which results in a low figure of merit (zT). Efforts have been made to enhance silicon's figure of merit by improving the ratio of electrical conductivity (σ) to thermal conductivity (κ). This has involved investigating techniques such as using thin membranes or nanowires, controlled oxidation processes, and surface roughening to reduce κ while maximizing σ. The introduction of nanostructures into silicon has generated interest and research in this area. Researchers have developed Si-based micro thermoelectric generators (µTEGs) that have shown promise. For instance, Thierno-Bah *et al.*[1] achieved significant improvements by reducing the thickness of single-crystalline silicon to 70 nanometers and patterning the membrane with a network of "pores" approximately 40 nanometers in diameter and spaced at intervals of 100 nanometers ("pitch"). Under a temperature difference of 5.5 Kelvin, they achieved a notable power output of 4.5µW/cm². These findings highlight the potential of silicon nanostructures to enhance thermoelectric technology.

Despite these promising developments, challenges persist. One challenge is the variability in experimental zT measurements for crystalline silicon nano-objects. Calculating zT involves measuring κ, σ, and the Seebeck coefficient (S) independently, each with its uncertainties ranging from 5% to 20%. Thus, the resulting zT uncertainty can exceed 50%. Addressing this issue, the Harman technique offers a direct means to measure zT in bulk materials. This thesis introduces an adapted version of this technique for suspended crystalline nano-membranes, considering radiative effects, contact resistances, and Joule heating. Additionally, a device integration approach is presented, allowing direct zT determination through electrical measurements, simplifying the process. Complementary to these advancements, the study investigates fundamental devices that facilitate a comprehensive understanding of silicon's properties, this entails measuring and analyzing thermal conductivity, Seebeck coefficient, and electrical conductivity. The thesis is organized into four chapters:

Chapter1: Thermoelectric Properties of Silicon: Generalities and State of the Art.

In this first chapter, we explore the fundamentals of thermoelectricity and the relevance of silicon as a thermoelectric material. We report essential thermoelectric properties, including the Seebeck effect, Peltier effect, and Thomson effect, which are fundamental to the operation of thermoelectric devices. We also delve into the theory behind thermoelectric power-generating devices and discuss key transport properties such as thermal conductivity, electrical conductivity, and the Seebeck coefficient, all of which significantly impact the efficiency of thermoelectric materials. Furthermore, we examine the importance of material selection in thermoelectric applications, with a particular focus on silicon. Additionally, we explore various methods used to optimize silicon's thermoelectric performance, including nano-structuration, oxidization, surface roughness, and phonon engineering. Finally, we discuss the practical integration of silicon into thermoelectric

applications, particularly in micro thermoelectric generators configured for applications around room temperature.

Chapter 2: Theoretical Studies and Modeling of zT Figure of Merit Direct Measurement Adapted to Membranes.

Expanding upon the foundational insights presented in the previous chapter, the second chapter focuses on the challenges surrounding the determination of *zT* due to the data dispersion observed in experimental measurements of crystalline silicon nano-objects. This dispersion can be attributed to the uncertainty inherent in the separate measurement of *zT's* components. To address this challenge, we introduce a novel methodology inspired by the transient Harman method for directly measuring *zT* in nanostructured planar membranes. We begin by explaining the conventional "Harman technique"[2] and then present our adapted method designed for membrane-based measurements. This chapter also provides a comprehensive overview of the design of the measurement device specifically adapted for implementing the transient Harman technique on membranes. Furthermore, we derive a formula to calculate the intrinsic figure of merit (zT_i) of planar suspended membranes. This formula establishes a relationship between the *zT* value acquired using the conventional technique (zT_H), the membrane's geometric characteristics, and the correction terms applied to account for measurement losses.

In addition, computational modeling is conducted using the Finite Element Method (FEM) to evaluate our proposed technique across various scenarios of silicon thermal conductivity, encompassing bulk thermal conductivity and reduced thermal conductivity. These simulations facilitated a comparative analysis between *zT* values determined using the classical Harman method and our adapted membrane-based technique, validating the efficacy of our proposed approach.

Chapter 3: Fabrication of the Integrated Metrology Device Dedicated to Transient Harman Measurement of Silicon Nano-meshes.

The third chapter takes a turn toward practical implementation, focusing on the fabrication process of an integrated metrology device dedicated to transient Harman measurements of silicon nano-meshes. The primary objective is to fabricate this measurement device, accompanied by elementary devices instrumental in determining transport properties such as thermal conductivity, Seebeck coefficient, and electrical conductivity. These measurements encompass various membrane geometries and types, including both plain and patterned membranes. The chapter meticulously outlines the design phase, which encompasses the development of transient Harman demonstrators, doping level measurement platforms, Seebeck coefficient measurement devices, and thermal conductivity measurement devices.

The fabrication process, and realization of these devices, emphasizing their integration onto a Silicon On Insulator (SOI) wafer is detailed in a step-by-step manner, commencing with preliminary procedures such as wafer cleaning and alignment marker etching. Subsequently, we proceed to more intricate stages, including phononic engineering patterning, Si_xN_y deposition, cavities opening, sidewalls protection, metallization and the suspension of membranes using XeF_2 & Vapor HF etching. Furthermore, we address the challenges encountered during the realization process and provide practical solutions to overcome them. This chapter plays a vital role within the thesis, serving as the foundational infrastructure required to conduct experiments and extract results in the following chapter. It is noteworthy that this fabrication process aligns with the standard complementary metal–oxide–semiconductor (CMOS) fabrication process, ensuring compatibility with industrial silicon CMOS process lines.

Chapter 4: Characterization of the Fabricated Devices and Results.

In the fourth chapter, the spotlight shifts to the characterization of the devices developed throughout the thesis and the ensuing discussions of the achieved outcomes. The chapter is segmented into four sections, each dedicated to distinct measurement protocols and the impact of phonon engineering on specific properties. Starting with the measurement of the Seebeck coefficient, the chapter outlines conditions, procedures, and the influence of phonon engineering on this parameter in both p and n-type Si membranes. Following this, the subsequent sections cover electrical measurements using the conventional "Van Der Pauw" method, thermal conductivity measurements, and zT figure of merit measurements. Each section sheds light on the protocols, conditions, and the effects of phonon engineering. We thoroughly analyze and discuss the results and make comparisons with relevant literature to provide a comprehensive understanding.

Chapter 1 Thermoelectric properties of silicon: generalities and state of the art

Abstract

The first chapter explores thermal energy harvesting, with a specific focus on thermoelectric power generation. The study investigates the thermoelectric effect, transport properties, and optimization techniques, particularly for monocrystalline silicon. This chapter focuses mainly on improving the thermoelectric properties of monocrystalline silicon and its integration into micro thermoelectric harvesters in a planar configuration for near-temperature applications.

1.1 Thermoelectric Energy Harvesting for Sustainable Wireless Sensor Networks

The application of Wireless Sensory Networks (WSN) is fast growing within many sectors (including, but not restricted to security, industry, and aviation), playing the pivotal role of gathering and storing information. In fact, with significant advancement and investment in the technology, wireless sensors network market is forecasted to grow at a compound annual growth rate (CAGR) of 17.64% and be valued at approximately $123.93B USD by 2026 [3]. The vast majority of WSN currently rely on batteries to store and supply the energy required for their operation. However, the batteries are also considered a major limiting factor in the growth of WSN due to the significant costs and logistical challenges associated with individually replacing sensors with depleted batteries. Additionally, batteries also have the major drawback associated with their relatively large size and weight in microscopic applications.

Regarding the problem of battery lifetime, several solutions have previously been considered. They include “energy-aware Medium Access Control (MAC) protocols (SMAC [4], BMAC [5], XMAC [6]), power aware storage, routing and data dissemination protocols [7][8][9], duty-cycling strategies [10][11], adaptive sensing rate [12] and tiered system

architectures [13]. Though these solutions assist in marginally increasing battery life, they nevertheless only manage to 'kick the can down the road' as the batteries will continue being depleted and will ultimately need to be replaced. Furthermore, increased battery life can create other challenges like larger size and heavier weight, in addition to increased production costs.

The miniaturization of the wireless sensor nodes limits the use of batteries as a power source due to their large size. In microscopic scale the integration of batteries is very complex and difficult. Energy converters are sufficient to supply microscopic sensors with low energy requirements. Furthermore, they open the possibility to integrate the sensor, the energy supply and the communication circuit within one small smart system.

To address the challenge of size and bypass the issue of battery life, energy harvesting is often seen as a potential solution. Energy harvesting refers to scavenging energy or converting energy from one form to the other. The principle of energy harvesting is to extract small amounts of energy from various ambient sources of the environment. The available energy for harvesting is mainly provided by ambient sources such as: 1- light (artificial and natural lighting), 2- thermal sources, 3- mechanical vibration sources and also 4- ambient radio frequency. The abundance of heat, and wasted heat specifically, makes thermoelectric harvesting a particularly advantageous enterprise. Wasted heat is defined as the unused thermal energy given to the surrounding environment in the process of converting primary energy carriers to final use. It is estimated that 72% of global primary energy consumption is wasted, with wasted heat being dispersed into the environment at every step of the energy conversion process [14]. Looking at the electrical energy consumption in residential premises, close to two-thirds of the energy is wasted as heat in the extraction process at the power plants and approximately a further one-tenth of the energy is lost as heat in the transportation process. Around 60% of the energy extracted from power plants is lost as waste heat during its generation [15], and between 8% and 15% is lost as heat in the electrical lines for its transport and transformation [16]. Energy harvesting can increase efficiency, minimize cost and reduce maintenance requirements in WSNs. Moreover, large scale heat loss and the ability to redirect this wastage as a source of energy in the energy harvesting process, makes thermal energy harvesting a key consideration in moving forward with the ubiquitous growth of the WSNs.

1.2 Thermoelectric effect

Thermoelectric effects, initially examined during the first half of nineteenth century by T.J. Seebeck and J. Peltier, refers to the conversion of temperature differences into voltage and *vice versa* at the contact point of two distinct electrical conductors, known as the thermocouple (Figure 1-1). Thermoelectric devices, such as the Seebeck generator, employ thermoelectric effects in practical operations to control and measure temperature or generate voltage. The three thermoelectric effects are known as the Seebeck Effect, Peltier Effect and Thomson Effect.

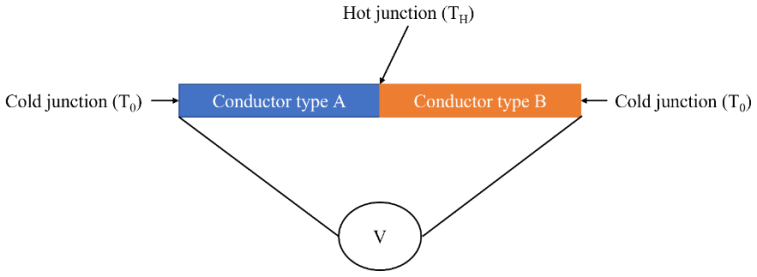


Figure 1-1: Principle of a thermocouple, illustrating the thermoelectric effect. The voltage (V) generated is proportional to the temperature difference (T_H - T_0) between the hot junction (T_H) and the cold junction (T_0).

1.2.1 Seebeck effect

Of the three individually discovered thermoelectric effects, Seebeck effect was the first, discovered by Thomas Seebeck in 1821. Seebeck demonstrated that an electromotive force could be created at the connection point of two different metals with a temperature difference. Observations made by Seebeck included the deflection of a needle when a bismuth-copper (Bi-Cu), forming a closed loop, was heated. Thus, the misleading term of thermomagnetic was coined. It was later understood that the deflection of the needle was the result of electrical potential thermally built in the thermocouple. The generated electric field (E) is given by the following equation:

$$E = -S.\nabla T$$

Equation 1- 1

Where S [$V.K^{-1}$] is the Seebeck coefficient (also known as thermopower), an intrinsic property of the material, and ∇T [$K.m^{-1}$] is the temperature gradient.

1.2.2 Peltier effect

The second thermoelectric effect was discovered shortly after, by Jean Peltier and is thus referred to as the Peltier effect. Inverse to the Seebeck effect, the Peltier Effect is the cooling or heating effect when an electric current is passed through a thermocouple. Although there are similarities between the Peltier effect and Joule's heat effect, which also converts electric current into heat, there are crucial differences between these two phenomena. Unlike the Joule heating effect, which is a completely irreversible effect that depends only on the square of the current density (the Joule effect always occurs regardless of the direction of current flow in the element), the Peltier effect is directional (its magnitude depends linearly on the current flow), the amount of heat pumped/released is directly proportional to the current, and is observed only at the junction of the thermocouple (not throughout the entire conductor, as in the Joule heating effect). The Peltier effect is represented as follows:

$$q = \pi.\mathrm{j}$$

Equation 1- 2

Where q [W] is absorbed/generated heat, j [A] is the electrical current and π [V] is the Peltier coefficient. The interrelation between the Seebeck and Peltier effects is represented by the following link between their coefficients: π = TS.

1.2.3 Thomson effect

Physicist William Thomson (Lord Kelvin) recognized the internal relation between the Seebeck Effect and Peltier Effect in 1855. The Thomson effect, as opposed to considering a thermocouple like the Seebeck and Peltier effects, describes the thermoelectric effect within a single homogenous conducting material in the presence of a large thermal gradient ∇T and electrical current j. Thomson Effect is described using the following equation:

$$q = \beta.\mathrm{j}.\Delta\mathrm{T}$$

Equation 1- 3

Where β [$V.K^{-1}$] is the Thomson coefficient and ΔT is the temperature difference between the two ends of the TE material. The Thomson coefficient is linked to the Seebeck coefficient through:

$$\beta = T\frac{dS}{dT}$$

Equation 1- 4

1.3 Theory of thermoelectric power generating devices

The principles of thermoelectric devices will be introduced here, with a discussion on thermoelectric material choice in subsequent pages (p.21). In principle, a power generating thermocouple device comprises two electrically different materials; namely, the n-type and p-type semiconducting materials. In an n-type material, the majority carriers being electrons, a gradient of heat will lead to a drift of electrons along the heat flux. Oppositely, in the p-type material, holes drift is involved. These semiconductors are connected in an electrically series and thermally parallel arrangement (as depicted in Figure 1-2) and are bridged at each end *via* a superior electrical and thermal conducting material. At the hot end, T_H, extraneously supplied heat ensures a higher temperature is maintained relative to the cold end, T_C, which is kept at a constant but lower temperature. The temperature difference created between the hot and cold junctions results in an electric current flowing through the load resistor (attached to the cold ends of the system) that closes the electric loop.

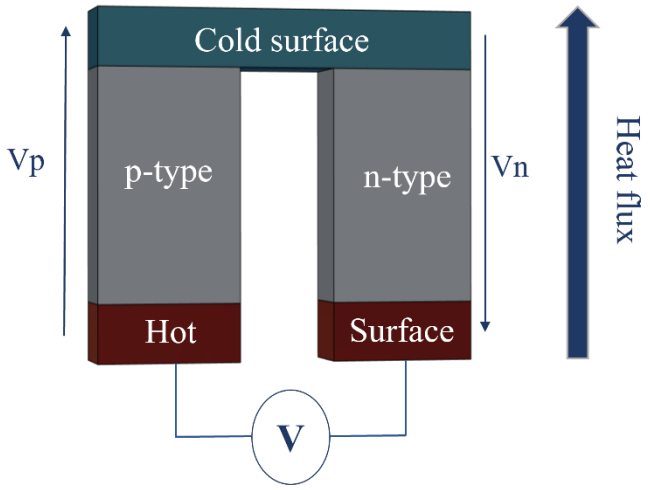


Figure 1-2: Thermoelectric power generating device principle.

Thermoelectric generators are evaluated by their efficiency that is given as a function of the Carnot efficiency η_{carnot} and the thermopiles' figure of merit *ZT*. With T_C, T_H, S_x, $\boldsymbol{\rho}_x$, κ_x, being respectively the temperature of cold and hot sources, Seebeck coefficient, electrical resistivity, and thermal conductivity of x-doped material (x = n, p).

$$\eta = \frac{Power\ supplied\ to\ load}{Heat\ absorbed\ at\ hot\ junction}$$

$$\eta = \eta_{carnot} \times \frac{\sqrt{(1+ZT)}-1}{\sqrt{1-ZT+\frac{T_C}{T_H}}}$$

$$\eta_{carnot} = 1 - \frac{T_C}{T_H}$$

Equation 1- 5

$$ZT = \frac{\left(S_p - S_n\right)^2}{\left(\sqrt{\rho_n \kappa_n} + \sqrt{\rho_p \kappa_p}\right)^2} \times \bar{T}$$
$$\bar{T} = \frac{T_C + T_H}{2}$$

Equation 1- 6

Maximizing the thermoelectric efficiency is achieved by increasing the figure of merit that is dependent on the thermoelectric material's transport properties. Good thermoelectric material must combine three main parameters: high electrical conductivity, high Seebeck coefficient and low thermal conductivity.

1.4 Thermoelectric transport properties

1.4.1 Thermal conductivity

Heat is transferred between objects via several mechanisms: conduction (between objects via direct physical contact), convection (though fluids and gas) and radiation (through electromagnetic radiation). In thermoelectric harvesting, composed of n-type and p-type semi-conductors discussed in p.17, heat is transferred through materials via conduction. Thermal conductivity is a material specific property and is defined as the material's ability to carry thermal energy in the presence of a thermal gradient. The equation for thermal conductivity is given by Fourier's law:

$$\vec{q} = -\kappa . \vec{\nabla} \mathrm{T}$$

Equation 1- 7

Where κ [W/m.K] is the material's thermal conductivity, q is the local heat flux density [W/m^2] and ∇T is the temperature gradient [K/m].

The two major mechanisms for conduction are the collective excitation of the lattice structure, termed phonons, and the transfer of energy by free charge carriers through the structure. In metal samples with high purity, the electronic contribution to conduction dominates that of phonons; this is a result of the high concentration of the delocalized electrons. The electron thermal conductivity of a material is related to its electrical conductivity by the Wiedemann-Franz law – good electrical conductors are also good thermal conductors – and the specific contribution of the electrons in conducting heat is given by Lorentz' number, L (L=1.6-2.5×$10^{-8}V^2.K^{-2}$):

$$\kappa_e = \sigma \cdot L \cdot T$$

Equation 1- 8

In insulators, on the contrary, it is the phonons that dominate the propagation of heat due to the relatively lower concentration of free electrons within the material's structure.

$$\kappa_{ph} = \frac{C_v \cdot L_{ph} \cdot v}{3}$$

Equation 1- 9

Where κ_{ph} is the lattice thermal conductivity related to the heat propagation through the lattice vibrations (phonons) depending on mean free path L_{ph}[m], sound velocity v[$m.s^{-1}$] and heat capacity per unit volume C_v[$J.K^{-1}.m^{-3}$].

In semiconductors, even though phonons are responsible for a major part of conduction, there can be instances when phonons and electrons can both play a significant role in thermal conductivity. Thus, the thermal conductivity of a semiconductor is given as a sum of both components: the phonon and electronic contributions.

$$\kappa = \kappa_e + \kappa_{ph}$$

Equation 1- 10

In an undoped semiconductor, the free charge density is equal to the intrinsic charge density (n_i). In a doped semiconductor (n or p), the charge density is equal to the sum of the intrinsic charge density of the material (n_i) and the density of free electrons (donor atoms, N_D) or free holes (acceptors, N_A). Semiconductors are generally classified in one of two states: extrinsic and intrinsic. At low temperatures (the thermal energy in a material is relatively low), the donor impurity atoms donate an electron, and the acceptor atoms accept an electron (donate a hole). The assumption of complete ionization is often used. Thus, for significant dopant concentration, the density of the majority carriers (the electrons for an n-doped material or the holes for a p-doped material) is almost equal to the density of the impurity atoms $n=n_i+N_D \approx N_D$. This case corresponds to the extrinsic regime. When the temperature rises and reaches a sufficient level, electron-hole pairs are generated directly under the effect of thermal motion and the concentrations n_i (p_i) of the corresponding charge carriers then rapidly predominate over those of the impurity atoms. The doped material is then in the intrinsic regime.

1.4.2 Electrical conductivity

Electrical conductivity is defined as the ability to carry electric charge and, like thermal conductivity, is material specific. Metallic bonds, where there are positive ions and large seas of delocalized electrons, are most favorable to electrical conductivity. The mobility and 'free' nature of these outer electrons allow them to move along the metallic lattice and thus carry electric charge. From the perspective of the energy band theory, there are sufficiently large number of electrons near the Fermi level leading to large electrical conductivity. The Fermi level of semiconductors is in the band gap, somewhere between the valence and conduction bands. The band gap, also known as the forbidden energy band, is an energy range without electronic states. As discussed earlier (p.18), semiconductors are classified as being in either intrinsic or extrinsic regimes; and the capacity of the semiconductor to conduct electricity is largely dependent on which of these two states it is in. At room temperature in the intrinsic scenario, the valence band is predominantly occupied, leading to a shortage of available holes for charge transport. Similarly, the conduction band is mostly unoccupied, resulting in a scarcity of electrons for charge transport. When in the extrinsic state, by either receiving dopant atoms or employing supplied energy to transfer electrons to the conduction band, resistance is reduced, and the semiconductor can behave as a metal (an electrical conductor). When a sufficiently high temperature is reached, the conduction resistance is reduced exponentially; the relationship can be presented as in the following equations:

$$\sigma(T) \approx \sigma_0 \cdot \exp\left[-\frac{E_G(T)}{k_B \cdot T}\right]$$

Equation 1- 11

$$\sigma(T) = \sigma_p(T) + \sigma_n(T)$$

Equation 1- 12

$$\sigma_n(T) = \mu_n(T) \cdot n(T) \cdot |q|$$

Equation 1- 13

$$\sigma_p(T) = \mu_p(T) \cdot p(T) \cdot |q|$$

Equation 1- 14

Where n and p are the holes and electrons concentrations, μ is their mobility [m^2/V/s], q is the electronic charge ($1.6.10^{-19}$Coulombs), E_G is the band gap energy [eV] and k_B is Boltzmann constant ($1.38.10^{-23}$ J/K).

1.4.3 Seebeck coefficient

With the Seebeck effect being the conversion of temperature difference into electromotive force, the Seebeck coefficient is a measure representing the material's ability to do such. The formal mathematical definition of Seebeck coefficient is represented as follows:

$$S = \frac{\Delta V}{\Delta T}\Big| \Delta T \to 0$$

Equation 1- 15

Linking the Seebeck Coefficient to electrical conductivity, Cutler *et al.* [17] redefined a more general formula called the Mott formula as a function of the electrical conductivity expressed as a function of energy E :

$$S = \frac{\pi^2 \cdot k_B^2}{3q} \cdot T \cdot \frac{\mathrm{d}(\ln[\sigma(E)])}{dE}\Big|_{E=E_F}$$

Equation 1- 16

Looking at semiconductors more closely, Fritzsche [18] expressed the Seebeck Coefficient as:

$$S_n = \frac{k_B}{q} \cdot \left(\frac{E_c - E_F}{k_B T} + A_n\right)$$

Equation 1- 17

$$S_p = \frac{k_B}{q} \cdot \left(\frac{E_v - E_F}{k_B T} + A_p\right)$$

Equation 1- 18

With E_c, E_v and E_F being the conduction band energy, the valence band energy and the Fermi level; A_p and A_n are material specific constants.

Having the effective densities of states in valence and conduction bands, the equation above can be further simplified to:

$$S_n = \frac{k_B}{q} \cdot \left(\ln\left(\frac{N_C}{n}\right) \quad + A_n\right)$$

Equation 1- 19

$$S_p = -\frac{k_B}{q} \cdot \left(\ln\left(\frac{N_v}{p}\right) + A_p \right)$$

Equation 1- 20

With N_c and N_v denoting the effective density of states in valence and conduction bands.

1.5 Thermoelectricity-Material choice

An efficient thermoelectric material should achieve the so-called "phonon-glass/ electron-crystal" limit[19]. Semi-conductors offer optimal compromise between S, σ and κ, resulting in the highest *zT* value. The optimal doping level that refers to the highest *zT* and power factor (PF) values of Si material at room temperature (T=300K) is 10^{19} cm^{-3}.

To distinguish between the figure of merit of a thermoelectric device and that of the thermoelectric material, we assign *ZT* for the device and *zT* for the material[20].

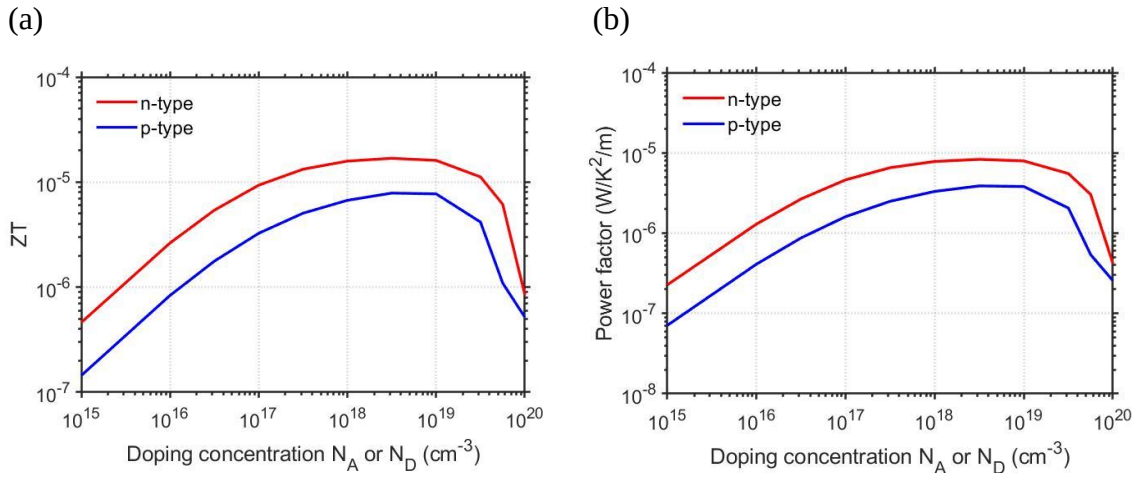


Figure 1-3: (a) Si zT as a function of doping concentration, (b) Si power factor as a function of doping level; blue line refers to p-type Si and red line to n-type Si [1].

The more commonly investigated thermoelectric materials are based on BiTe, Sb and Pb alloys. Especially the Bi_2Te_3 class is the reference material due to its high *zT* value (1.1 state-of-the-art, 0.7 industrial state-of-the -art). However, they remain expensive, harmful and feature low compatibility with low-cost and established CMOS processes. Cheap, ecofriendly and CMOS compatible materials based on silicon and germanium exhibit *zT*<<1 at room temperature. However, research has demonstrated different methods to enhance the thermoelectric efficiency of Si-based materials near room temperature (Figure 1-4). These methods rely on nanoscale effects, among which thermal conductivity reduction, to reach in some cases a figure of merit close to 1. Therefore, we will opt to use silicon as thermoelectric material in our device. Research has demonstrated the different methods to enhance the thermoelectric efficiency of Si material – this will be discussed in section 1.6.

[1] This plot has been obtained by M. Haras and modified by me based on bulk Si parameters. (unpublished)

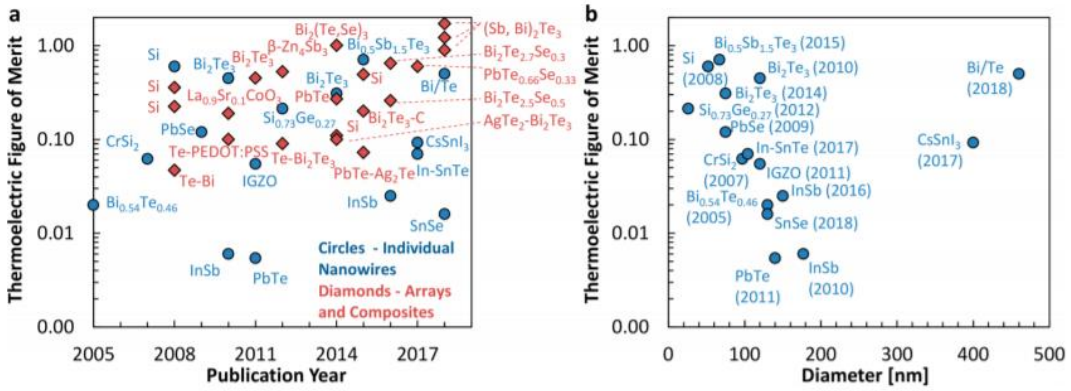


Figure 1-4: Reported thermoelectric figures of merit (zT) of representative nanowires at room temperature, (a) in chronological order and (b) as a function of wire diameter [21]

1.6 Optimization methods of zT figure of merit of silicon

In section 1.3 we gave the *ZT* figure of merit of a TE device and in this section, we will present the *zT* figure of merit of a TE material. The efficiency of a thermoelectric material is evaluated by its thermoelectric figure of merit (zT) .

$$zT = \frac{S^2\sigma}{\kappa}T$$

Equation 1- 21

Where T is the temperature, S is the Seebeck coefficient, σ is the electrical conductivity and κ is the thermal conductivity.

Thermal conductivity is a sum of two contributions dominating lattice κ_e and κ_{ph} (Equation 1- 10). Therefore, to enhance *zT*, *S* and the (σ/κ) ratio must be increased. Seebeck coefficient is proportional to the logarithm of the carriers' concentration (the Seebeck coefficient decreases with the carriers' concentration). Figure 1-5 shows the variation of Seebeck coefficient as a function of Si level doping and the temperature. Metals have small S due to their high density of free carriers. In contrast, insulators exhibit high S due to low carrier density that facilitates thermally induced movement of carriers from hot region to cold one. Besides, σ for insulators is very low. The figure of merit *zT* is expressed as $zT = S^2\sigma T/(k_e+k_{ph})$. In the metallic limit, k_e becomes dominant and equals LσT (Equation 1- 8). Consequently, *zT* can be simplified to $zT = S^2 / L$ in the case of a metallic scenario.

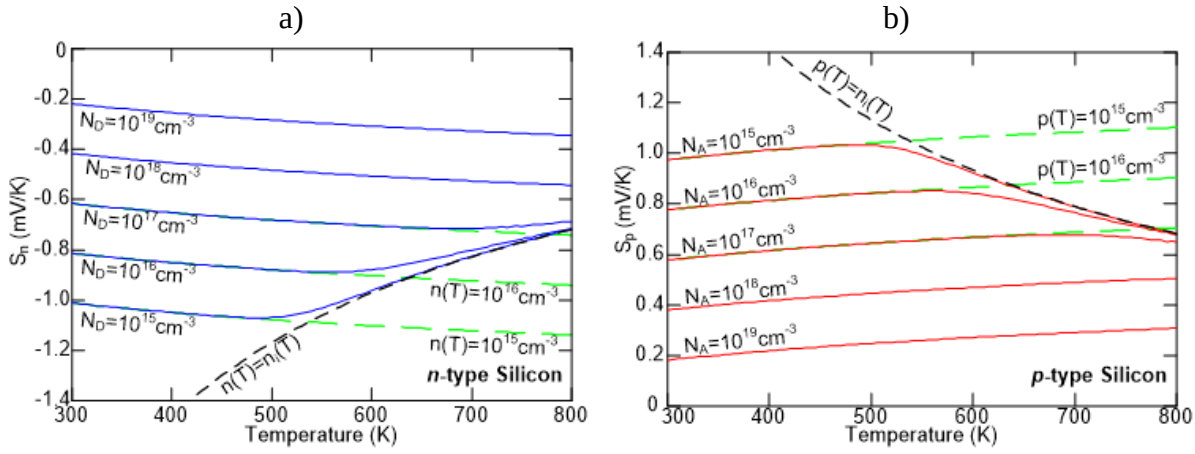


Figure 1-5: Silicon Seebeck coefficient versus temperature for different doping concentrations. Blue continuous line for n-type doping. Red continuous line for p-type doping. Green dashed line assuming carrier and doping concentrations equality and temperature independence. Black dashed line Seebeck coefficient in intrinsic semiconductor [2].

Research investigated to increase the (σ/κ) ratio by decreasing the thermal conductivity without affecting the electrical one through the partial suppression of lattice thermal transport. The phonons mean free path L_{ph} and the electrons mean free path L_e for Si bulk at room temperature differ by two orders of magnitude (L_{ph}~300nm, L_e~1.2nm) [22]. Moreover, at room temperature more than 85% of the κ value is contributed by the phonons which MFP is between 100 nm and 10 μm[23] (Figure 1-6).

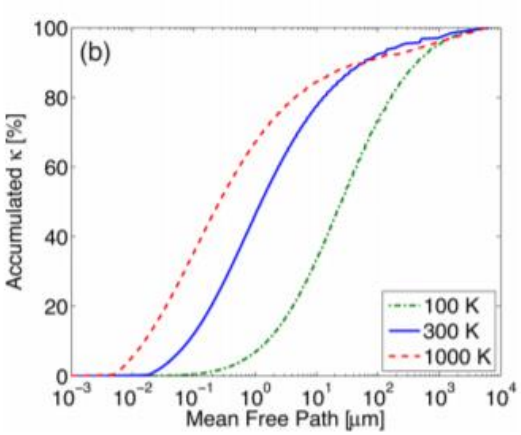


Figure 1-6: Accumulated silicon κ over wide range of phonon's free path for different temperatures[23].

Research developed various kind of studies on thermal transport allowing the thermal conductivity reduction such as:

1.6.1 Nano-structuration

Nano-structuration permits the reduction of thermal conductivity by the reduction of the heat flow carried by phonons. The interest in low-dimensional materials approach is to increase the internal interfaces (boundary scattering), the length scale being comparable to the phonon mean free path. Recent progress in nanotechnology enables the fabrication of materials with lower dimensions than L_{ph}. Hence, L_{ph} is shortened due to collision with the sample boundaries. Consequently, the thermal conductivity is reduced. Figure 1-7 illustrates the phonon propagation in bulk material and nanostructured material.

[2] This plot has been obtained by M. Haras and modified by me based on bulk Si parameters. (unpublished)

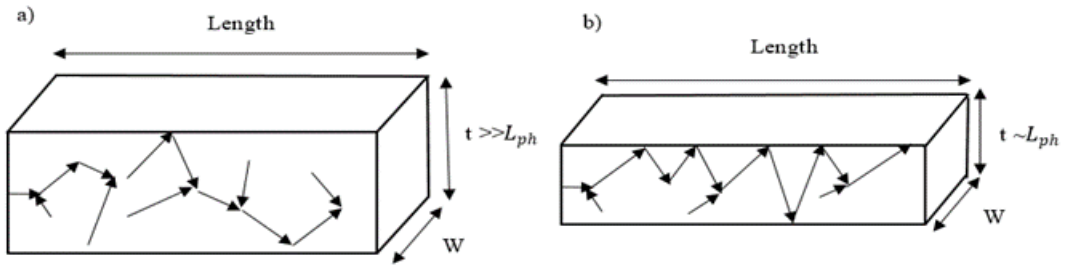


Figure 1-7: Phonon propagation in the material, a) in bulk material, b) in nanostructured material.

Improvement of the figure of merit *zT* has been established using different nanostructured systems 0D (quantum dots), 1D (Nanowires), and 2D (thin films). Therefore, the structure miniaturization represents a key to improve the thermoelectric properties of non-conventional materials such as Silicon and Germanium.

1.6.1.1 2D-silicon membranes and meshes

Thinning effect (2D effect) was experimentally confirmed for several Si thickness[24][25][26][27][28][29][30][31][32][33][34]. The observed reduction in thermal conductivity within thin films is a result of an interplay of intrinsic factors arising from their confined dimensions. These factors encompass interfaces, grain boundaries, and surfaces, introducing additional scattering sites for phonons. Consequently, boundary scattering is intensified, perturbing the smooth propagation of heat. In parallel, the restricted dimensions impose constraints on the mean free paths of phonons, limiting their ability to traverse longer distances before encountering scattering events. As a cumulative effect, this leads to an overall attenuation of heat conduction within thin films. Figure 1-8 graphically presents the relationship between Thermal conductivity and thickness for 2D silicon membranes and meshes (2D).

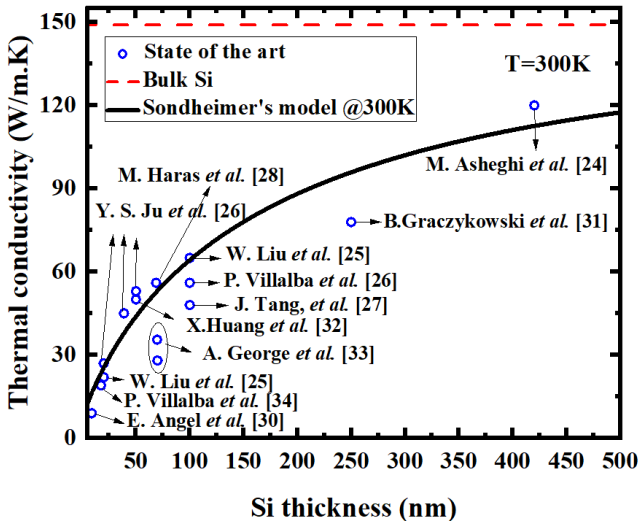


Figure 1-8: Thermal conductivity as a function of thickness for 2D silicon membranes and meshes (2D).

The silicon thinning allows a significant reduction of the thermal conductivity down to $9 W.m^{-1}.K^{1}$ for 9 nm thick silicon membrane [30], this incredible reduction opens the way for commercialized silicon thin films based thermoelectric energy harvesters compatible with CMOS technology.

1.6.1.2 1D- silicon nanowires

Silicon narrowing effect (1D effect) has been investigated by researchers [35][36] [37][38] for its potential in thermoelectric applications. The principle is the same as the thinning effect by developing silicon nanowires with the smallest possible diameter, owing to the reduction of the thermal conductivity by increasing the borders scattering and the quantum confinement phenomenon. Experimental confirmation of the reduction in silicon's thermal conductivity through nanowire integration is presented in Figure 1-9.

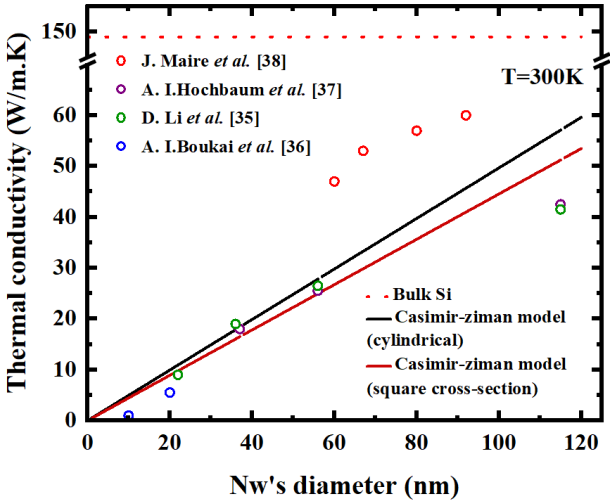


Figure 1-9: Thermal conductivity as a function of Si nanowire's diameter (1D).

1.6.1.3 0D- silicon quantum dots

Silicon germanium (SiGe) with an intrinsic lower thermal conductivity than silicon has attracted significant attention as a good thermoelectric material. Numerous scholars[39][40][41][42][43] have observed an additional reduction of the thermal conductivity to the thinning or narrowing effect. This additional reduction is caused by the augmented phonon scattering off the increased density of nano-grain boundaries. D. Li *et al.*[39] have noticed that alloy scattering of phonons in the SiGe segments is the dominant scattering mechanism in the superlattice nanowires in additional to the boundaries scattering. Figure 1-10 reviews the thermal conductivity at room temperature as a function of the Ge percentage.

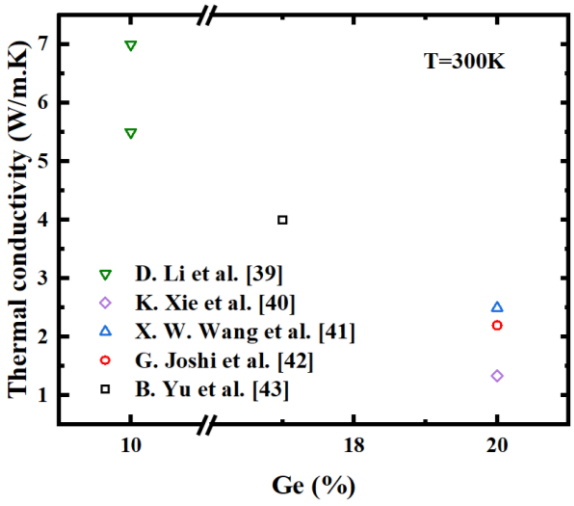


Figure 1-10: Thermal conductivity as a function of Ge percentage in Si (0D).

1.6.2 Oxidization and roughness

The thermal conductivity of nanostructured systems can be further decreased by roughening[32] [44] or oxidization [45] [46] of the surface. George *et al.*[45] studied the influence of an ultrathin Al film on 70 nm-thick Si membranes using three types of samples: Si membrane without aluminum, with aluminum of 0.5 nm set thickness and with aluminum of 1 nm set thickness. The thermal conductivity was independent of the thickness of deposited aluminum and it decreased from 35 to 23 $W.m^{-1}.K^{-1}$ and from 28 to 20 $W.m^{-1}.K^{-1}$ at room temperature for n-type and p-type samples, respectively. Moreover, the electrical conductivity was not affected by the aluminum film which leaded to an increase of the figure of merit *zT*. The results are given in Figure 1-11. Furthermore, a reduction of the thermal conductivity of more than 40% was experimentally demonstrated by Huang *et al.* [32] by roughening the Si surface with arrays of nano-cones (Figure 1-12) . Figure 1-13 (a) shows experimentally measured thermal decay times of both samples with and without nano-cones, a long decay time indicates lower heat conductance for constant heat capacity. In addition, 100-fold reduction in thermal conductivity of rough Si nanowire with diameter of about 50 nm synthesized by electrochemical route was reported by Hochbaum *et al.* [44] Figure 1-13 (b).

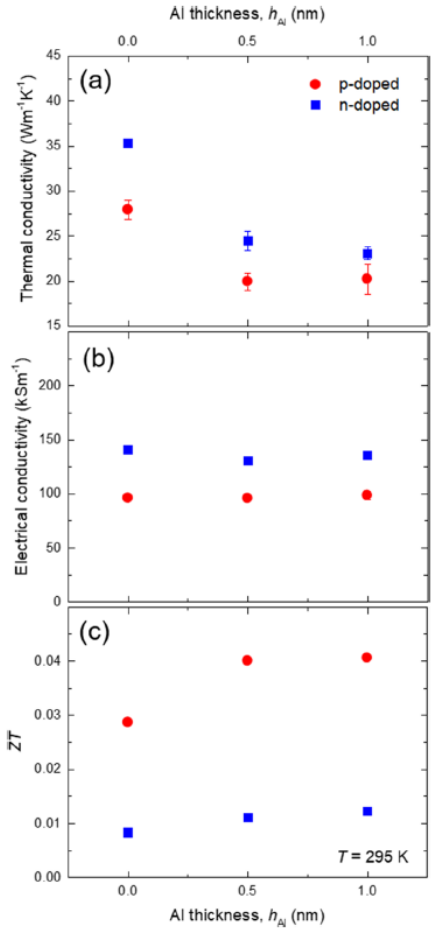


Figure 1-11: Measured (a) thermal conductivity, (b) electrical conductivity, and (c) figure of merit (zT) of Si membrane as a function of aluminum set thickness[45] .

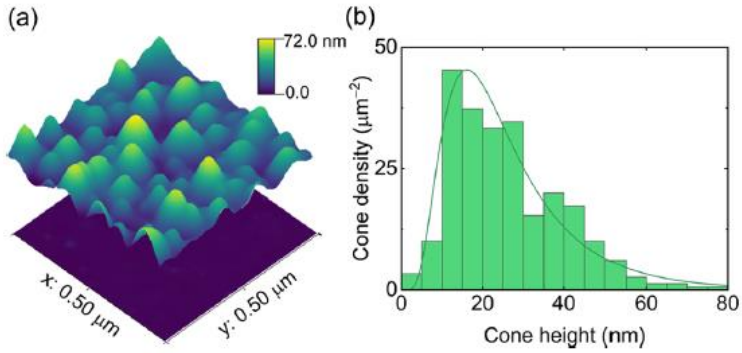


Figure 1-12: (a) AFM images of membranes with (upper) and without (lower) nanocones.(b) Histogram of nanocone height distribution [32].

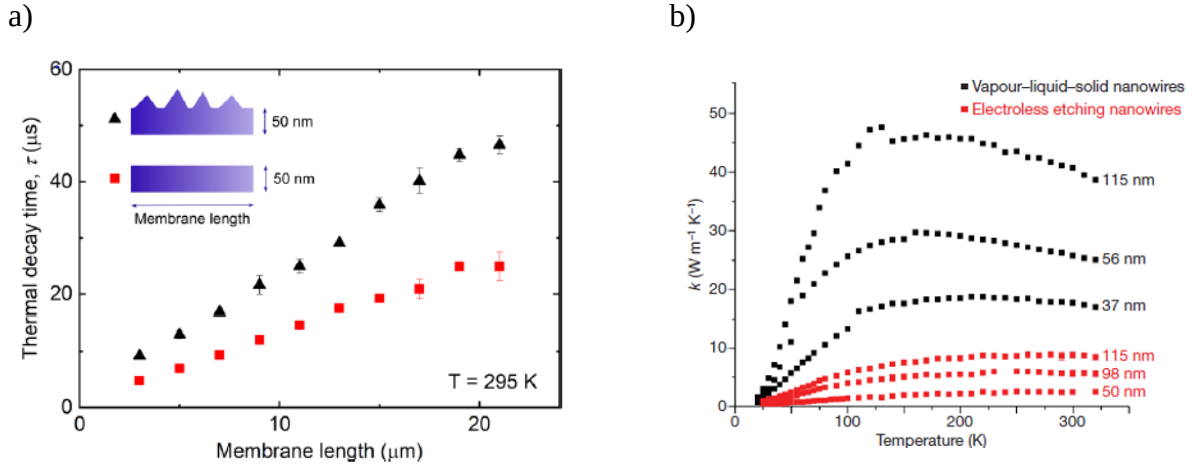


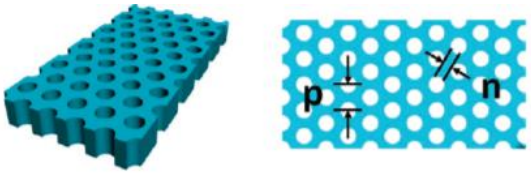
Figure 1-13:(a) Thermal decay time as a function of length of 50 nm-thick silicon membranes with and without nano-cones at 295K[32], (b) Thermal conductivity of rough Si nanowire (black lines) with different diameters and smooth one (red lines) as a function of temperature[44].

1.6.3 Phonon engineering

The Si thinning, narrowing, oxidization or roughness improves the (σ/κ) ratio. On the other hand, *zT* increases. However, it remains insignificant, due to the change being less than 1 (*zT* <1) at room temperature. The key to more develop the (σ/κ) ratio is to couple the thinning, narrowing, oxidization and roughness with a phononic engineering solution. Phonon engineering (PnCs) represents the nano-patterning of thin films [47] [31] [48] or nanowires [49] [46] [50] with two-dimensional (2D) arrays of holes. These arrays of holes serve as barriers (or additional scattering sites) to phonons during propagation. Thus, the thermal conductivity reduction. This reduction depends on the placement of holes[50] [51], their diameter[52][49] [53], periodicity[49] [46], the pitch (the distance between the pores' centers) and the neck (the distance between the edges of two neighboring pores).

Phononic engineering has been studied by both theoretical and experimental means. Tang *et al.* investigated the thermoelectric properties of 100 nm thin silicon membranes patterned with several phononic engineering patterns as given in Figure 1-14. Results show that the pitch and neck size between holes are the key parameters to further reduce thermal conductivity.

Moreover, the doping increases the probability of phonon scattering through the addition of impurities into material and thus the reduction of thermal conductivity.



	avg. pitch, p (nm)	avg. neck, n (nm)	avg. porosity, φ (%)	κ (Wm^{-1} K^{-1})
nonholey			0	50.9 ± 2.0
nonholey*			0	47.6 ± 1.7
350-pitch	350	152	~35	10.23 ± 0.44
140-pitch	140	59	~35	6.96 ± 0.34
55-pitch	55	23	~35	2.03 ± 0.07
55-pitch*	55	23	~35	1.73 ± 0.06

*Figure 1-14: Holey silicon geometry and the measured thermal conductivity at 300K, *denotes doped samples (Boron (5.10^{19} cm^{-3}))[52].*

Yanagisawa *et al.* combined narrowing, surface roughness and phonon engineering to increase the surface scattering rate. Hence, reduce thermal conductivity. Figure 1-15 describes the impact of the holes' diameter, the limiting dimensions, and the pitch size on κ of 1D Si rough and smooth PnCs at 295K and 4K. The neck and pitch size between holes play the most important roles in thermal conductivity reduction. Moreover, the thermal conductivity depends less on the period than on the surface roughness.

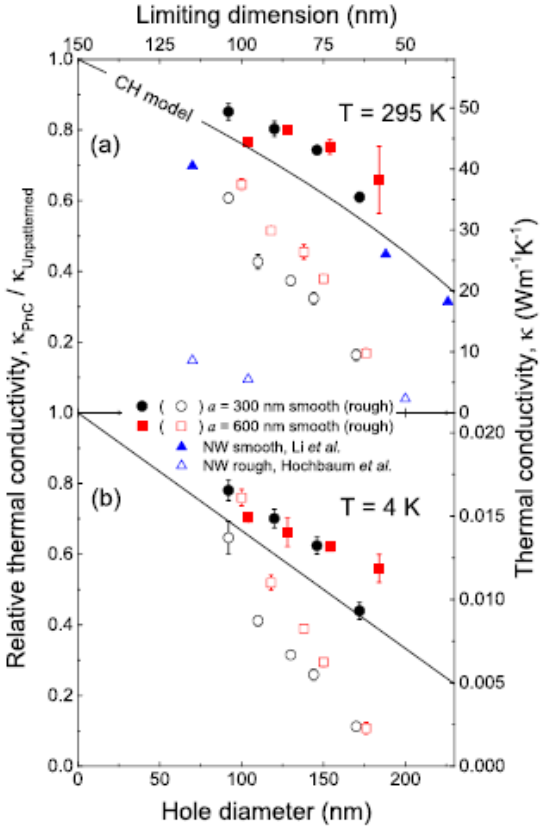


Figure 1-15:Measured thermal conductivity of 1D PnCs and nanowires (NWs) as a functions of the hole diameter and the limiting dimension (neck size) at (a) T=295K and (b) T=4K for pitch a=300 nm (black circles) and a=600 nm (red circles)[49].

In the same context, further research studied the impact of the placement of pores in the thermal conductivity. Wagner *et al.* [54] showed that the coherent acoustic phonon modes are suppressed with the introduction of disorder in pore alignment. Nakagawa *et al.* [51] found that the placement of pores has a strong influence on κ when the period is within the range of the thermal phonon mean free path. Maire *et al.* [55] demonstrated that Incoherent boundary scattering depends only on the shape, size, and separation of the holes, although coherent boundary scattering additionally depends on pores' disorder at low temperature (Figure 1-16) .

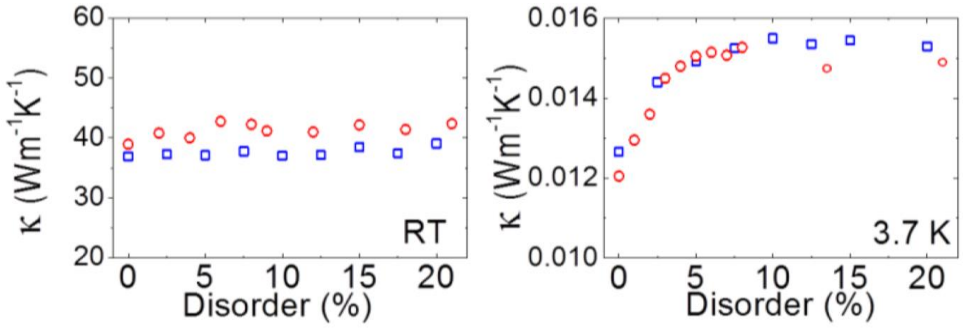


Figure 1-16: Thermal conductivity of the thermos-crystals with hole diameters d=135 nm (red dots) and d= 170 nm (blue dots) at room temperature and at 3.7 K.

Figure 1-17 gives the measured thermal conductivity of silicon phononic crystals (κ_h) / the thermal conductivity of plain silicon (κ_p) ratio at room temperature according to the volume fraction. Thermal conductivity close to amorphous Si limit was obtained by both Tang *et al.*[52] et Graczykowski *et al.* [31]. As can be seen in Figure 1-17, none of the analytical models - the effective medium theory or Mawxell-Eucklen - can describe the thermal conductivity result caused by the formation of phononic crystals in the Si membrane, since the thermal conductivity depends not only on the percentage of porosity (volume fraction), but also on the neck and pitch between the holes.

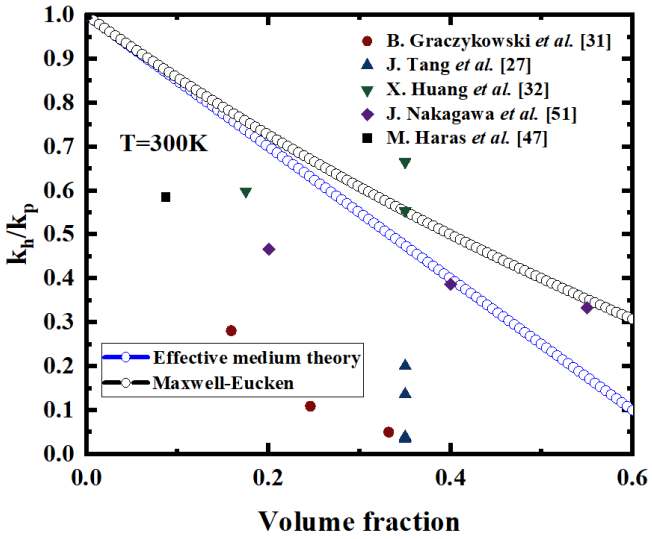


Figure 1-17: The thermal conductivity of silicon phononic crystals (κ_h) /the thermal conductivity of plain silicon (κ_p) ratio at 300K as a function of volume fraction, including the effective medium theory (blue circles) and Maxwell-Eucken (black circles) fitting.

Despite the relatively low value of κ achieved using nanometric structure, few experimental measurements of zT in crystalline silicon nano-objects are presented with significant data dispersion (Figure 1-18). Few measurements were made because each thermoelectric parameter had to be measured separately. Hence the fabrication of different devices. Direct measurement of zT with one device would be a good solution to study the efficiency of the thermoelectric material produced. In chapter 2, all methods for direct determination of zT are investigated.

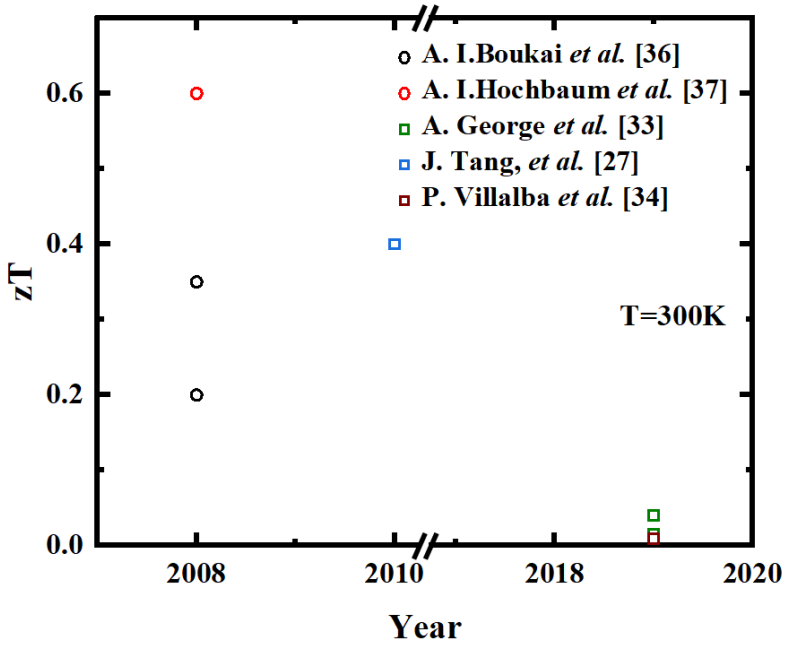


Figure 1-18: Reported values of zT for crystalline silicon planar configurations.

1.7 Integration of Si for thermoelectric applications

The improvement of the material's figure of merit due to the introduction of nanostructures has encouraged research in this area. Various Si-based micro thermoelectric generators (µTEGs) have been developed. Different designs and configurations were elaborated based on the heat flow direction / device leg growth: (i) Type lateral / lateral (in-plane configuration), (ii) Type vertical / lateral (cross-plane configuration and (iii) Type vertical / vertical (cross-plane configuration). In this thesis we focus on the in-plane configuration (Type lateral / lateral). In in-plane devices, heat flows along the surface, through the TE material which allows a better thermal gradient management. Consequently, it enhances the output voltage and output power. Exploiting the simple planar geometry and the compatibility with Si technology, one-dimensional (1D) nanowire structures grown by the CVD-VLS mechanism have been employed by Devila *et al.* [56]. The fabricated device is based on an architecture consisting of a thermocouple with a uni-leg (p-type) Si arrays. Figure 1-19 schematically illustrates the design of the proposed thermoelectric micro-generator (µTEG).

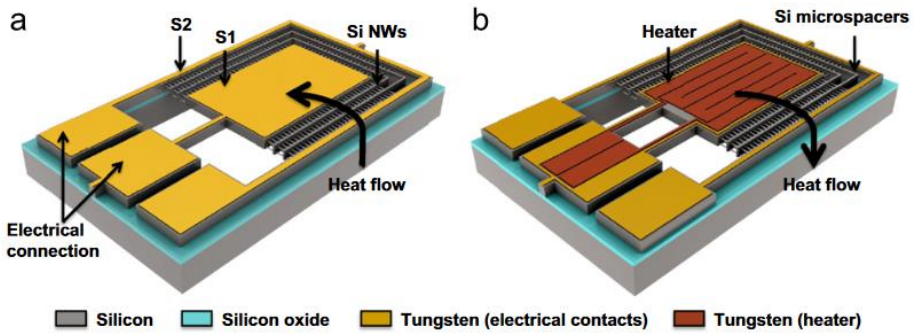


Figure 1-19: Sketch showing the design of the basic structure. (a) A thermally isolated suspended silicon mass (S1) is connected to the surrounding silicon bulk (S2) through silicon nanowires (Si NWs) allowing a planar temperature difference to be achieved, conforming in this way a thermos-element in which the Si NWs act as a nanostructured thermoelectric material; (b) sketch of a similar device showing an integrated heater employed both as heat source and sensor to control and characterize the temperature gradients attainable in the structure. Heat flow is reversed in this configuration[56].

The fabricated µTEG have shown Seebeck voltages up to 60 mV, 4.4 mV and generated power densities up to 1.44 mW/cm^2, 9 µW/cm^2 respectively, for ΔT=300 °C and ΔT=27 °C (across the nanowires), working as energy harvesters (Figure 1-20). Other monolithic planar µTEGs (p-type Si) with double thermal deflection was presented by Ziouche *et al.* [57]. In order to improve the heat flow path, a zig-zag thermopiles are embedded between a dielectric film and a layer of polyimide/BCB that electrically isolate it from two periodically etched Silicon wafers which serve as heat concentrator (HC) and heat evacuator (HEV). The µTEG topology proposed is depicted in Figure 1-21 (a). The µTEG was characterized at 3 different steps of the process: (i) before removing the Si µcolumns, (ii) after removing the Si µcolumns and (iii) after removing the oxidized porous Si. The results obtained are shown in Figure 1-21 (b). The maximum output power for a five-membranes-based µTEG is 12.3µW/cm^2 for an input power of 2 W/cm^2. Due to its high thermal resistance (44.3 K/W)[58], this µTEG allows a heat adaptation to any environment with a high thermal resistance.

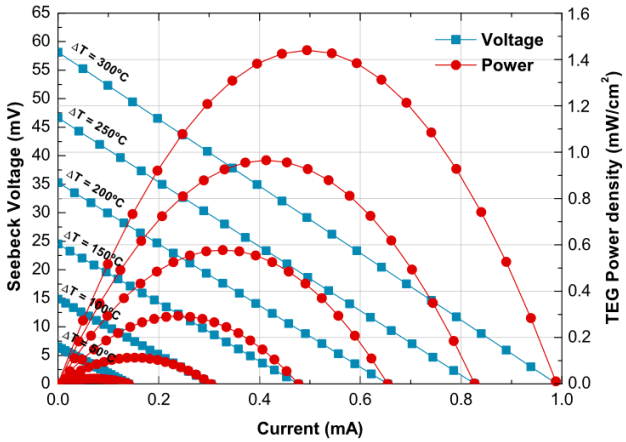


Figure 1-20: I–V and power density measurements at high temperature differences. I–V and power curves measured as a function of the temperature difference attained in a structure containing 9 Si NW arrays consecutively bridged. The power generated by the thermo-element (TEG Power) was obtained by measuring the generated voltages as a function of current for diverse temperature differences (DT), which were achieved by applying a DC current to the heater integrated in the structures[56].

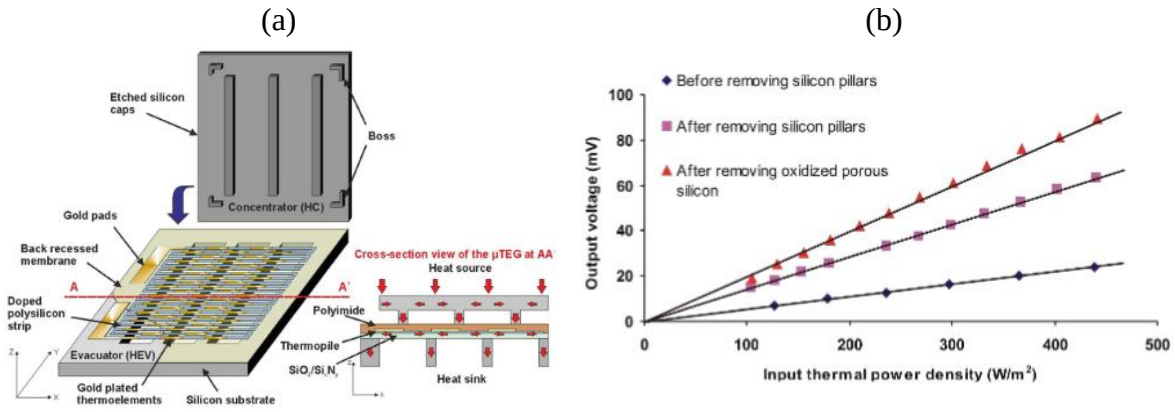


Figure 1-21: (a) 3D "exploded" structure and cross-section view of a 3-membranes planar µTEG. The red arrows symbolize heat paths; (b) Output voltage of the 5-membranes µTEG as a function of the input power density[57].

Two dimensions (2D) planar Si-based µTEGs containing ultra-thin single-crystalline Si membranes, 100nm in thickness, as the active TE material were developed by Perez-Marin *et al.*[59] . A power output of 4.5µW/cm^2 was achieved under a temperature difference of 5.5 K. Substantial improvements were achieved by Thierno-Bah *et al.*[1] by reducing the single-crystalline Si thickness to 70 nm and patterning the membrane with an opening of a network of "pores" of ~ 40 nm in diameter and spaced 100nm ("pitch") Figure 1-22. A µTEG with 5 suspended patterned thermopiles (PE) connected thermally in parallel and electrically in series generated a power density about 6.1 µW/cm^2 under a temperature difference of 5.5 K, that could reach few mW/cm^2 under a temperature difference higher than 100 K. In addition, Seebeck coefficient increases with PE. Hence, patterned thermopiles generate more tension.

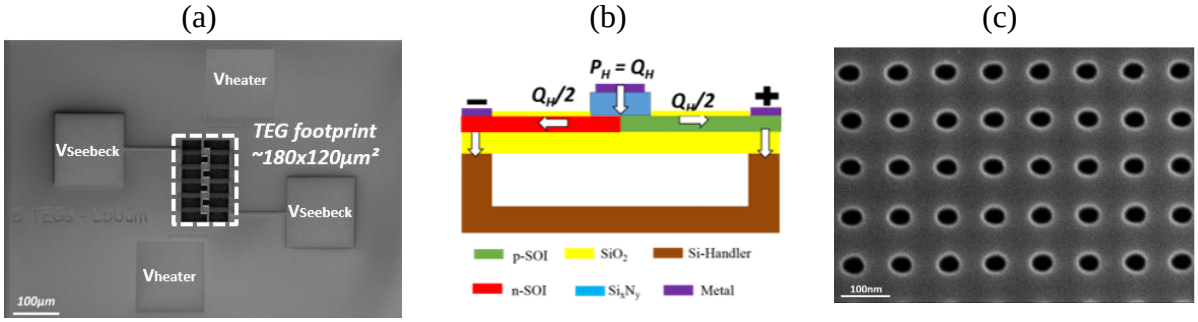


Figure 1-22: (a) µTEG made of 5 suspended thermopiles; (b) Cross section of the µTEG giving the heat flow direction; (c) Opening of a network of "pores" of ~ 40nm in diameter and spaced 100nm ("pitch")[1]

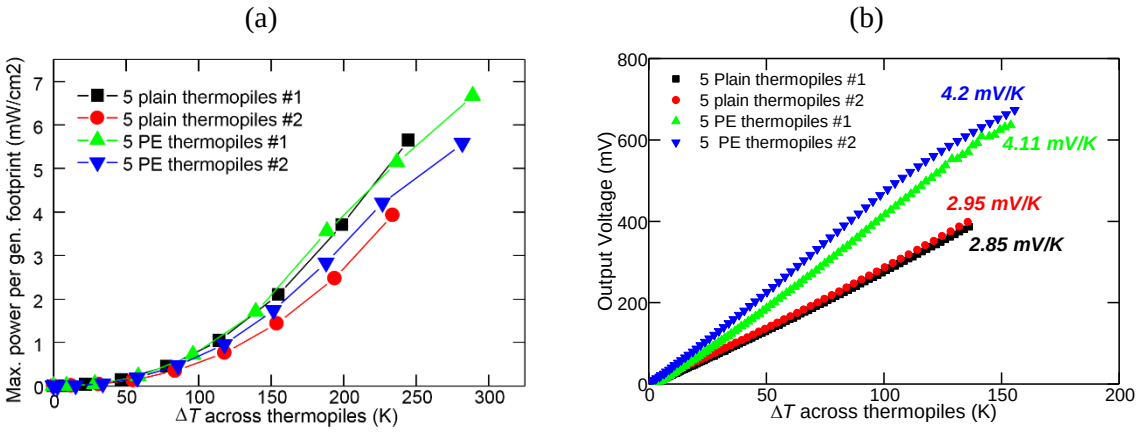


Figure 1-23: (a) Electric power generation per generator footprint of 2 samples of patterned thermopiles (PE) and 2 samples of plain membranes(plain) as a function of the temperature difference across the thermopiles; (b) The output voltage and the Seebeck coefficient of 2 samples of patterned thermopiles (PE) and 2 samples of plain membranes(plain) as a function of the temperature difference across the thermopiles[1].

These significant studies open up the opportunity to use silicon-based µTEGs for autonomous sensor nodes' power supplying. However, only few µTEGs were realized. [W. Liu et al.] [60] has shown that high *ZT* is not the only concern for a reliable, efficient and stable µTEG. Figure 1-24 summarizes the requirements to be taken into account for µTEG fabrication in 3 levels: material level, device level and system level.

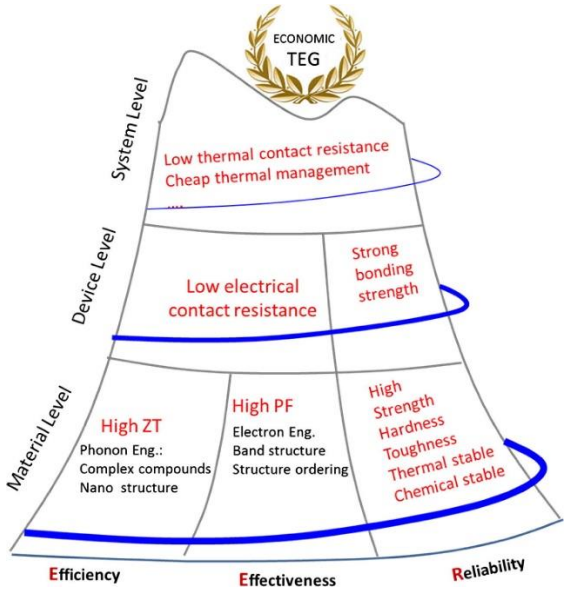


Figure 1-24: Hierarchical requirements for µTEG: the efficiency–effectiveness–reliability mountain[60].

Conclusion

This chapter presented an introduction to the main aspects of thermoelectric materials efficiency and characterization, with a brief introduction to the key theories needed in the discussion of subsequent chapters. In this chapter we discussed the selection choice made on silicon as thermoelectric material of our device. Furthermore, we presented all methods

investigated leading to improve the *zT* figure of merit of monocrystalline silicon material near room temperature. Examples of integration of silicon and sector of application were also presented in both planar and lateral configuration. Chapter 2 will review all different techniques used to measure the *zT* figure of merit directly on bulk thermoelectric material or millimetric material where the suspension of the TE material was achieved using wires. Furthermore, it will present a theoretical study and modeling of *zT* figure of merit direct measurement adapted to membranes.

Chapter 2 Theoretical studies and modeling of zT figure of merit direct measurement adapted to membranes.

Abstract

In the previous chapter, we highlighted the state-of-the-art on improving silicon thermoelectric properties in a planar configuration, by reducing the thermal conductivity component related to phonons. We saw that a relatively low value of thermal conductivity is achieved either by using nano-structuration, narrowing or oxidation. A few experimental measurements of *zT* figure of merit in crystalline silicon nano-objects were presented with significant data dispersion, as shown in Figure 1-18 chapter 1. This dispersion could be attributed to the determination of *zT*, which involves measuring the individual components of the thermoelectric figure of merit separately. It is important to acknowledge that significant uncertainty can be associated with each of these parameters. In fact, the uncertainty in *zT* can readily exceed 50%, considering that each material property may possess an uncertainty range between 5% and 20%. To address this limitation, in this chapter, we present a suitable methodology for direct zT measurement of nanostructured membranes in a planar geometry. This methodology is an adaptation of the transient Harman method. To understand this adapted approach, it's essential to first comprehend the conventional "Harman technique." Therefore, the initial section of this chapter provides an explanation of the conventional methodology.

In this chapter, we demonstrate our methodology using both theoretical (analytical formula) and computational (Finite element modeling) means. The theoretical aspects of the study aim at:

- Determining *zT* as a function of Joule heating for nanostructured planar configuration.
- Determining *zT* figure of merit as a function of correction terms.

And the physical aspects of the modeling study via FEM (Finite Element Modeling) intend to:

- Confirm the adapted methodology for direct *zT* measurement.
- Determining *zT* figure of merit of fabricated membranes using the adapted methodology for nanostructured thermoelectric materials.

2.1 zT direct measurement

The efficiency of thermoelectric materials is characterized by their figure of merit *zT*. Various research investigated on enhancing the conversion efficiency by increasing the *zT* figure of merit with improving the thermoelectric materials performance, rapid, simple and consistent technique to determine its performance is one of the important factors. There are several methods to determine *zT*, either using analytical or experimental approach where *zT* measured by experimentation can be obtained directly or indirectly. Generally, the thermoelectric figure of merit components is measured independently employing the individual measurements of the contributing material properties (κ, **ρ** and S). The uncertainty of *zT* could easily reach 50% considering that each parameter has an uncertainty of 5% to 20% [61].

$$\frac{\Delta z}{z} = 2\frac{\Delta S}{S} + \frac{\Delta \sigma}{\sigma} + \frac{\Delta D}{D}$$

Equation 2- 1

Harman's technique (1958)[2] is an easy and quick method to measure zT directly. The principle of this method is depicted in Figure 2-1(a). The TE material is suspended using two wires that will serve also for current injection in order to minimize the heat losses, 2 thermocouples are used for voltage measurement. For enabling equilibrium at different temperatures to be established rapidly, a heat sink is added as illustrates the Figure 2-1(b).

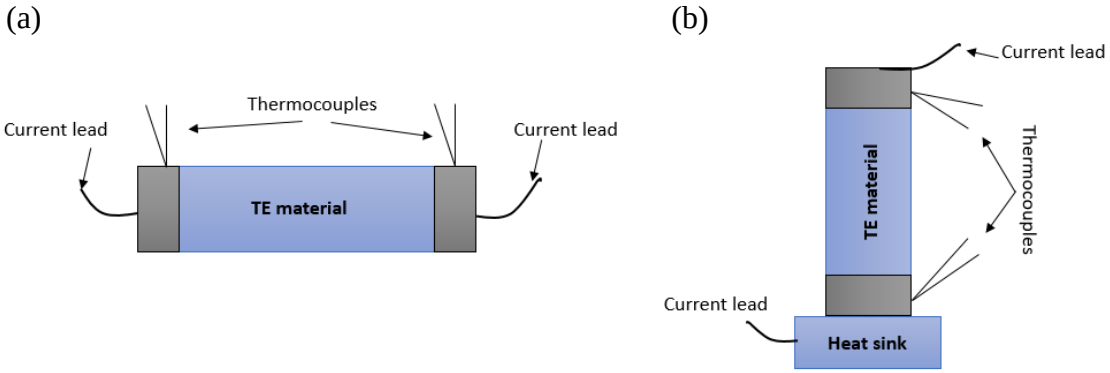


Figure 2-1: Harman's method principle (a) without heat sink; (b) with heat sink.

In Harman's technique the Joule heating and the heat losses occurring from within the sample being neglected. Figure 2-2 shows a schematic of Harman measurement method. Under Vacuum and adiabatic condition, a DC current I_{in} passes through the sample and a voltmeter measures electrical potential drop across the TE element. At the moment the current is injected, while temperature difference across the membrane is equal to 0, the measured voltage (V_R) corresponds to the multiplication of the current I_{in}, and electrical resistance (R). In the steady state, the heat flow through the sample due to the temperature difference will be equal to heat generated at the junction when an electrical current I_{in} flows through the sample due to the Peltier effect ($SI_{in}T = K\Delta T$). Therefore, the Seebeck equation can also be written in relation to the thermal conductance (K), Seebeck coefficient (S) and voltage drop in the electrode as:

$$V_S = S\Delta T = \frac{S^2 T I_{in}}{K}$$

Equation 2- 2

DC potential drop across the sample V_{dc} becomes $V_{dc} = IR + S\Delta T = V_R + V_S$.

The Harman zT is given as follows[2]:

$$zT = \frac{S^2T}{RK} = \frac{V_S}{V_R} = \frac{V_{dc}}{V_R} - 1$$

Equation 2- 3

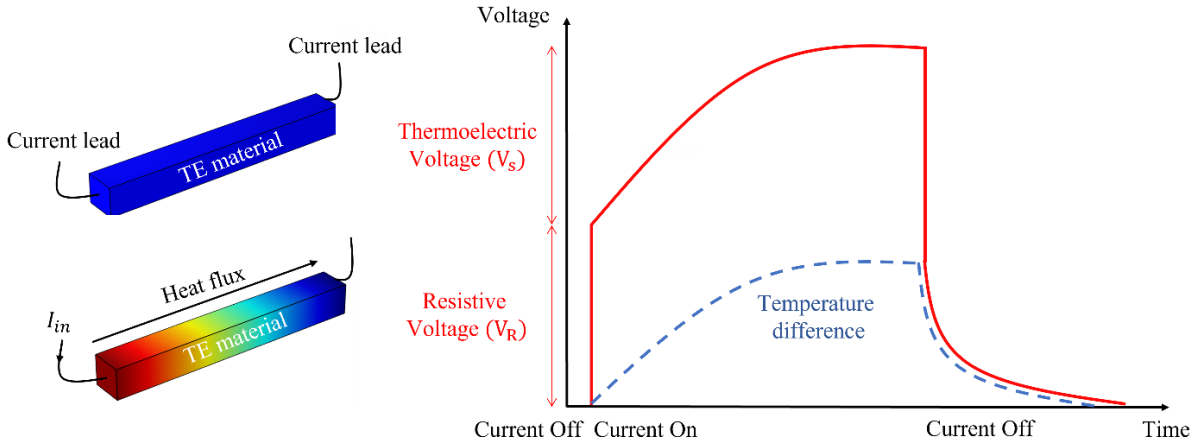


Figure 2-2: Schematic of Harman measurement method depicting i) the suspended thermoelectric element before and after injection of a DC current I_{in} ii) the measured voltage accross the sample versus time.

Nevertheless, this Harman method is neglecting the radiation and convection heat losses from the samples surfaces in addition to conduction heat loss from current and voltage wires. In 1965, M. R. Campbell et *al.* [62] suggested the first correction of Harman method taking into account radiation and convection that may involve in the experiment in the equation. Later in 2001, Gromov et *al.* [63] proposed a device based on classical Harman technique which provides the measurement of the three mainly parameters of thermoelectric modules: AC resistance, effective thermoelectric figure of merit and maximum temperature difference. Using an indirect *ZT* measurement method and by combining the measurement of Seebeck coefficient and electrical resistivity in one experimental set up. Kuznetsov et *al.* [64] showed that the calculated *ZT* value of single and segmented thermoelectric generator Bi_2Te_3 based materials is higher than the standard Bi_2Te_3 based material. The efficiency was 10% compared to 8.8% for the standard one. Another system to determine *ZT* directly was performed by Iwasaki et *al.* [65] in 2003, *ZT* figure of merit was given by measuring the resistance of both DC and AC method and it is presented by :

$$ZT = \frac{(\frac{R_{DC}}{R_{AC}} - 1)}{x}$$

Equation 2- 4

Where R_{DC} is the resistance value obtained by the DC method, R_{AC} is that obtained by the AC method and x is the rate of a heat leakage from a sample to a heat bath; when x = 1 it means that the sample is under a perfect adiabatic condition. Two years later, Iwasaki et *al.* [66] improved and replaced their system by a new one which gives simultaneous determination of the thermoelectric properties; κ, S, ρ and *ZT* figure of merit. Furthermore, their latest equipment provides an estimation of the temperature distribution in the sample induced by applying DC current, and of the thermal heat-flow created by low frequency AC current. Abrutin et *al.* [67]

included the heat loss from wires and voltage probes in the Harman method. They showed that the correction of the *ZT* value was considerably impacted by the Joule heat in current wires. The Harman method enables the direct measurement of *ZT* figure of merit at or below room temperature. Thus, Jacquot et *al.* [68] modified Harman method by adding a correction factor taking into account the heat loss by radiation at higher temperatures, the contact resistances and the geometry of the sample. An apparatus enabling to evaluate the *ZT* figure of merit based on Harman method and the three thermoelectric parameters simultaneously has been developed by Kwon et *al.* [69] The particularity of this new apparatus is that includes the LABVIEW software that allows not only controlling the system but also processing the data. Moreover, this apparatus can directly measure thermal conductivity by using guarded hot plate principle.

The application of Harman's technique to micro-structured materials is challenging because of the parasitic effects (electrical and thermal contact resistances and heat losses through the substrate and the electrodes used to apply electrical current to the sample). Harman's technique was extended [70] with extra terms taking into account the heat losses:

$$zT = (\frac{V_{DC}}{V_R} - 1)(1 + \frac{\beta P L^2}{12\kappa A} + \frac{\beta_c A_c L}{2\kappa A} + \frac{\kappa_1}{2\kappa A})$$

Equation 2- 5

Where β is the rate of radiation per unit area per unit temperature difference, P is the perimeter of the sample, L is the length, κ is the thermoelectric material TC, A is the cross-sectional area, β_c is the rate of radiation per unit area per unit temperature difference at the end of the sample, A_c cross-sectional area at the end of the sample, κ_1 is the conductance in parallel of each set of leads.

Experimental techniques considering the heat losses and the Joule heating effect are demonstrated by some research. [B. Kwon *et al.*][71] investigated on the determination of the parasitic terms by varying the sample's geometry and the lead wire types. Moreover, [E. Castillo *et al.*][72] employed the Harman technique under bipolar current excitation over a wide range of currents, in order to allow Peltier only and combined Peltier and Joule heating effects to control the temperature difference across the specimen. The experimental temperature, the resistive and Seebeck voltages were fitted using the developed thermoelectric model.

All the techniques discussed above are applied on bulk materials or millimetric structured materials, but they are not applied on thermoelectric materials at nanoscale as it is not possible to suspend it using two wires. The aim of this thesis is to adapt the technique studied by [B. Kwon *et al.*][71] to nanostructured silicon materials.

2.2 Design of direct zT measurement device

This section focuses on the device design for direct measurement of the *zT* figure of merit. It begins by presenting Harman's design approach for determining *zT* in bulk materials, followed by a customized design specifically adapted for the direct *zT* measurement of nanostructured membranes.

2.2.1 Direct zT measurement device for Bulk materials

In 1958, Harman conducted research aimed at developing a technique and methodology to accurately determine the thermoelectric performance of bulk materials[2]. One of his notable contributions was the development of the Harman technique, an experimental setup for direct measurement of the *zT* figure of merit, which quantifies the thermoelectric efficiency of a

material. The design of Harman's technique measurement device, illustrated in Figure 2-3, encompasses the following components:

i) Measured thermoelectric (TE) sample: The bulk material, typically in the form of a rectangular-shaped specimen, is carefully prepared and shaped to facilitate longitudinal current flow. It is important for the material to exhibit homogeneous properties, such as constant electrical conductivity and thermal conductivity throughout, without significant spatial variations.

ii) Thermocouples and current lead wires: Thermocouples and current lead wires are used in the measurement setup. These wires should be long and of small diameter to minimize heat conduction along them. The diameter of the leads through which current passes must be chosen carefully to ensure negligible heat flow while preventing excessive Joule heating.

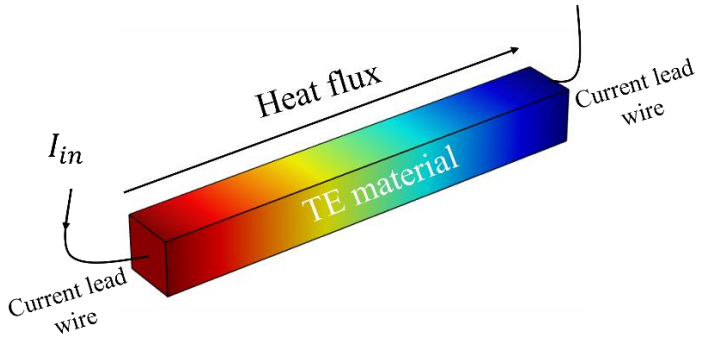


Figure 2-3: Direct zT figure of merit measurement device for bulk thermoelectric materials.

The *zT* measurement device for bulk materials does not require a sophisticated design, as the specimen can be suspended using the wires that serve the dual purpose of supporting the thermoelectric material, providing current injection, and facilitating voltage measurements. However, when dealing with nanostructured membranes, it is not feasible to suspend them using wires due to their smaller size compared to wire diameter. Consequently, alternative methods for suspension, current injection, and voltage measurement need to be investigated. The upcoming section will present a dedicated device for direct *zT* figure of merit measurement in nanostructured thermoelectric materials.

2.2.2 Direct zT measurement device for nanostructured materials

Inspired by Harman's study suggesting the suspension of the thermoelectric material to direct all heat flow through the thermoelectric material [2], we present a design for our *zT* direct measurement device adapted to nanostructured thermoelectric materials. The thermoelectric nanostructured elements in a planar configuration are called membranes and will be referred to as such henceforth.

Harman's direct *zT* measurement is effective only if the whole heat flux flows through the membrane. Therefore, to avoid heat flowing through the substrate, x-type (x being n or p) membranes must be fully suspended. Our suggested device is adapted to membranes and contains two identical suspended membranes, with electric terminals located at two points: *i)* the center of the platform which simultaneously serves as a current injecting point and the first voltage measurement point, and *ii)* both extremities of the membranes as a second voltage measurement point. There are two reasons for the decision to use two identical membranes in the same device instead of one suspended membrane. The first reason is purely mechanical: utilizing two membranes will increase the strength of suspended membranes during the

suspension. The second reason is to achieve symmetry, allowing us to extract two *zT* measurements from one device. Figure 2-4 shows the design of our sample.

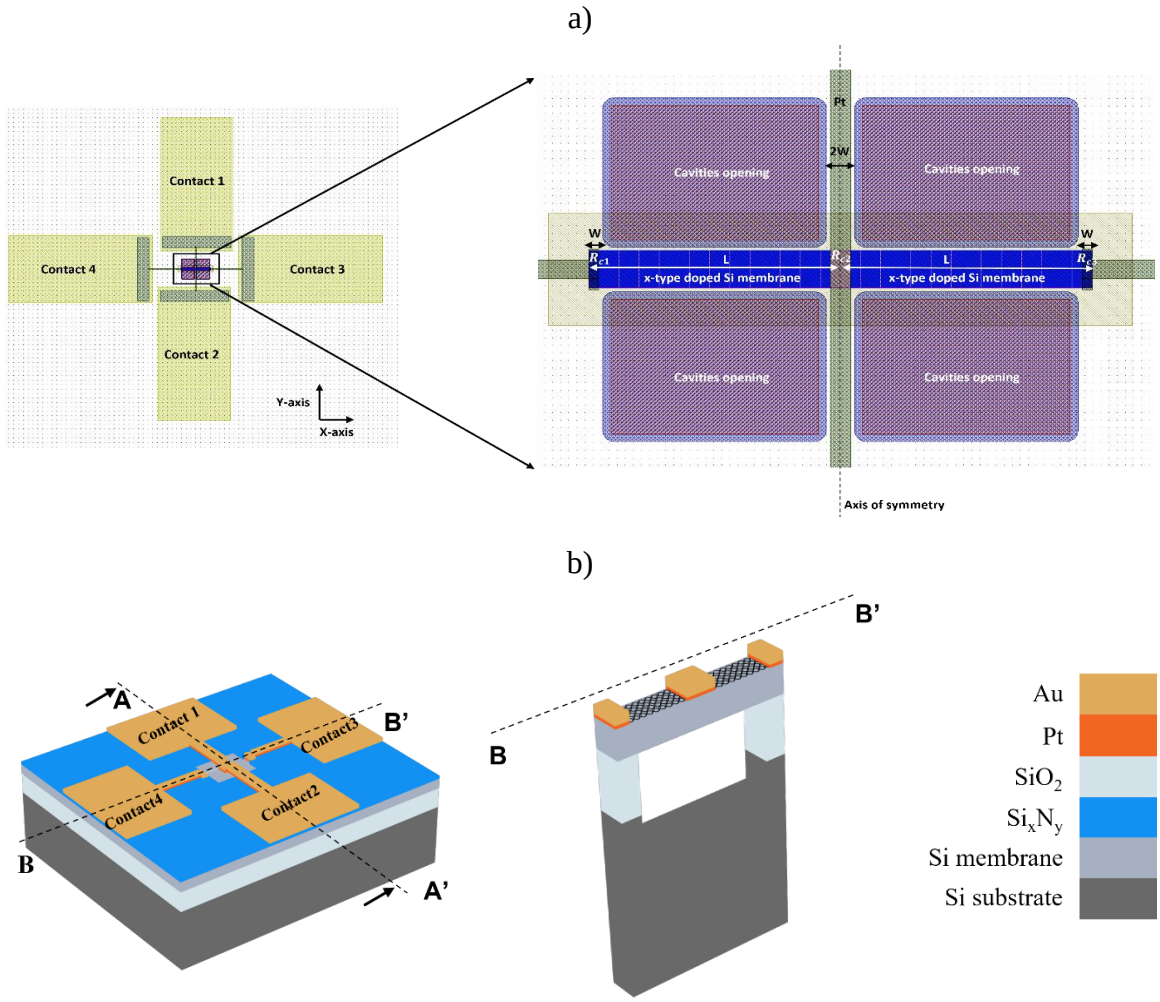


Figure 2-4: a) On the left, direct zT figure of merit measurement device adapted to membranes. On the right, close-up view of the direct zT figure of merit measurement device containing two symmetrical suspended membranes, electric terminals at the center for current injection for first voltage measurement and on sides for the second. b) On the left, 3D direct zT figure of merit measurement device adapted to membranes. On the right, longitudinal section of the direct zT figure of merit measurement device.

In the classical transient Harman method, the focus of study is a large-scale thermoelectric material. By disregarding all extrinsic factors, the *zT* figure of merit is determined by Harman as the ratio between the Seebeck voltage and the resistive voltage, as explained in detail in section 2.1. However, when applying the transient Harman method to analyze thin film membranes, it becomes crucial to account for significant losses stemming from various sources. These losses include electrical contact resistances, which arise at the interfaces between different electrical components due to imperfect conductivity. Additionally, there are losses attributed to the internal electrical resistance of the membrane, resulting from the inherent resistance within the thin film itself. Moreover, thermal contact resistances, caused by imperfect thermal conductivity at the interfaces between different materials, thereby impeding efficient heat transfer. Lastly, heat losses through convection, radiation, and conduction contribute to the overall reduction in the thermoelectric system's efficiency.

Convection entails the movement of heat through fluid motion, while radiation involves the emission of heat as electromagnetic waves, and conduction refers to heat transfer between solid materials. In principle, convection is effectively mitigated when working within a vacuum environment. To aid in comprehension, Figure 2-5 visually illustrates these factors. Subsequent sections of this manuscript will provide comprehensive details on the different types of heat transfer, addressing each one individually in a detailed manner.

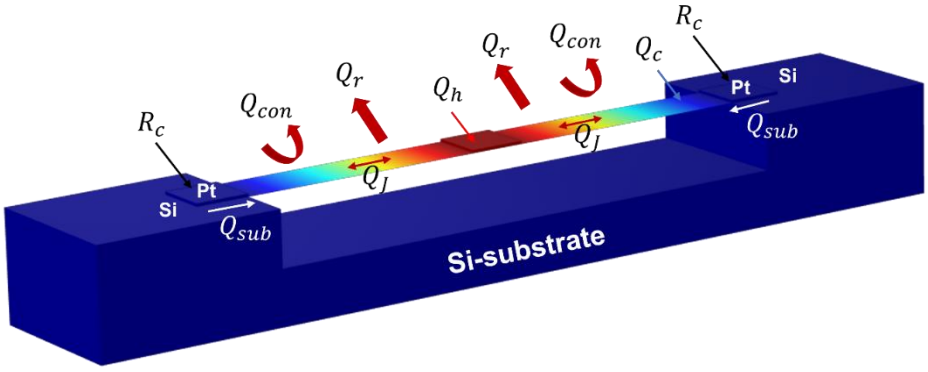


Figure 2-5: Schematic of zT direct measurement device adapted to membranes. When a DC current passes through the membrane, Joule heating (Q_J) raises the membrane's temperature. Heat flow from the membrane to the environment occurs via conduction through the anchors at the extremities (Q_{sub}), convection (Q_{con}), and radiation (Q_r). With a DC current, Peltier heating (Q_h) and Peltier cooling (Q_c) occur at each membrane extremity.

2.2.2.1 Heat transfer mechanisms

The transmission of thermal energy between physical objects is known as heat transfer. As per the second law of thermodynamics, heat naturally flows from a hotter object to a colder object. When objects and their surroundings achieve the same temperature, the state of the system is said to be in thermal equilibrium. Heat can fundamentally be transferred in three distinct modes, referred to as Conduction, Convection, and Radiation.

i. *Conduction:*

Conduction is the most common mode of heat transport within solid objects or between solid objects in contact. It is defined as the transfer of energy through matter from atom to atom or particle to particle.

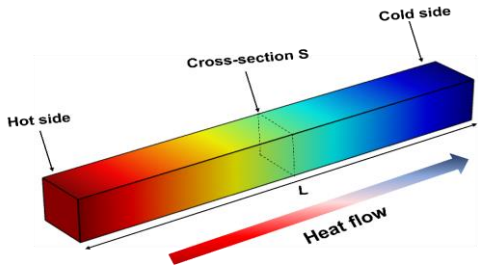


Figure 2-6: Thermal conduction.

Heat is transferred within an object through the movement of molecules in the hotter region, as they transfer their energy to molecules in the cooler region. This process, known as conduction, commonly occurs in solids and involves the diffusion of phonons or electrons. The thermal gradient present within the object drives this transfer of heat, resulting in the flow of energy from high temperature regions to low temperature regions.

Steady-state conduction occurs when the heat flowing into an object from one side is balanced by the heat flowing out from the other side. This means that the temperature difference that drives the conduction remains constant. Once the object reaches an equilibrium state, the distribution of temperatures within the object remains unchanged. In simpler terms, it is a situation when the heat going in equals the heat going out, and the temperature inside the object stays the same once everything is balanced.

The law of heat conduction, known as Fourier's law, asserts that the rate of heat transmission through a material is proportional to the negative gradient in temperature and the area through which the heat flows. The differential form of Fourier's law of thermal conduction shows that the local heat flux density φ [W/m^2] is s equal to the product of thermal conductivity $\boldsymbol{\kappa}$ [W/mK]and the negative local temperature gradient ∇T [K/m]. The heat flux density is the amount of energy that flows through a unit area per unit time.

$$\varphi(W.m^{-2}) = -\kappa.\nabla T$$

Equation 2- 6

ii. <u>Convection:</u>

Convection refers to the transfer of thermal energy within a moving fluid or between a moving fluid and a solid system. This energy transfer is carried out by two combined elementary transfer modes which are advection and/ or diffusion.

We refer to conducto-convection in the fluid when two materials with different temperatures in contact transfer heat both through conduction (from the solid medium to the fluid) and by convection (inside the fluid).

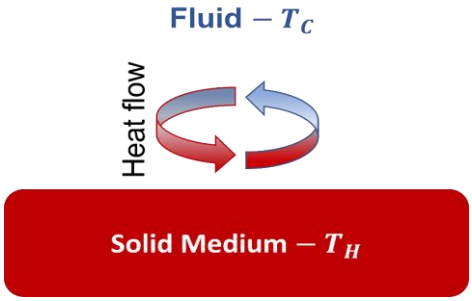


Figure 2-7: Thermal conducto-convection transfer.

The heat flux from a conducto-convection is given by Newton's law:

$$\varphi(W.m^{-2}) = h.(T_H - T_C)$$

Equation 2- 7

with h [W/m^2] being the conducto-convection transfer rate.

iii. <u>Radiation:</u>

Radiative heat transfer is the transfer of energy via thermal radiation, i.e., electromagnetic waves. It takes place in a vacuum or any transparent medium. (Solid or fluid or gas). At temperatures above absolute zero, all objects generate thermal radiation as a result of the random motions of matter's atoms and molecules.

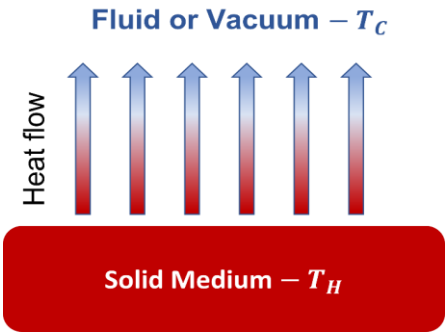


Figure 2-8: Thermal radiation method.

The heat flux from a thermal radiation is given by Stefan-Boltzmann formula:

$$\varphi(W.m^{-2}) = \varepsilon\sigma.(T^4 - T_0{}^4)$$

Equation 2- 8

With ε, σ, T_0 and T being respectively the emissivity of the material, the Stefan-Boltzmann constant ($5.670.10^{-8}$. W. m^{-2}. K^{-4}), temperature of surrounding, and object temperature. When the temperatures T_0 and T are not too far apart, the heat flux can be linearized to obtain a linear convection relation of the form:

$$\varphi(W.m^{-2}) = \beta.(T - T_0)$$

Equation 2- 9

with the coefficient of proportionality ($\boldsymbol{\beta}$) being the convective heat transfer coefficient [$W/m^2.K$]. For a blackbody, the radiative exchange coefficient $\boldsymbol{\beta}$ is equal to $4\sigma T_0^3$, at T_0=300K, $\boldsymbol{\beta}$ equals $6W.m^{-2}.K$. In the case of a gray body, the formula is extended by multiplying it by the total emissivity (or total absorptance), resulting in $\boldsymbol{\beta}$ equal to $4\sigma\,\varepsilon\,T_0^3$.

2.3 Theoretical study of zT direct measurement adapted to membranes

In this section, our focus is on the adaptation of the direct zT measurement approach originally developed by Harman[2] and subsequently refined by B. Kwon et al.[71] This adaptation is specifically aimed at nanostructured silicon materials. Our study begins with the application of Harman's technique to our suspended membrane, where we make the initial assumption that the heat generated by the Peltier effect is equal to the heat flow within the membrane. We then delve deeper into our analysis by introducing the Joule effect as a heat source, allowing us to investigate the influence of silicon's internal resistance on the determination of the *zT* figure of merit. Following this, we take into consideration additional variables, including radiation and conductive losses through the Pt arms. Due to the relatively compact dimensions of the silicon membrane, these losses play a significant role and require thorough consideration in our experimental measurements.

2.3.1 zT using Harman technique

When applying the Harman method to TE membranes, it is essential to eliminate any non-thermoelectric effects. This entails disregarding any electrical and thermal influences or parasites that could potentially impact the measured voltage.

The Harman measurement technique requires two distinct conditions: adiabatic and isothermal. In the adiabatic condition, the measurement is performed with adiabatic boundaries, preventing heat transfer between the TE sample and its surroundings. This condition is attained

by insulating the sample to maintain a constant temperature gradient within the TE material. On the other hand, the isothermal condition involves maintaining a uniform temperature across the entire TE membrane during the measurement, ensuring no temperature difference exists. This is accomplished by carefully controlling the heat distribution within the system. Figure 2-9 depicts the schematic of a *zT* direct measurement device tailored for membranes. The figure showcases the various factors considered within the Harman method.

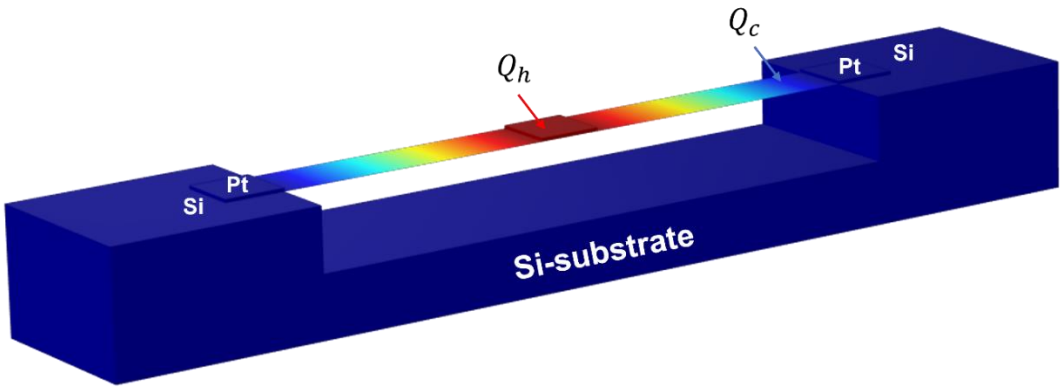


Figure 2-9: Schematic of zT direct measurement device adapted to membranes using Harman technique. When a DC current passes through the membrane, Peltier heating (Q_h) and Peltier cooling (Q_c) occur at each membrane extremity and heat flow through the membrane (Q_{Heat}).

The determination of the *zT* value using the Harman method can be summarized as follows (the steps sequence is illustrated on Figure 2-10): The experimental setup involves conducting measurements under adiabatic conditions, indicating that there is no heat transfer with the external environment. One method to accomplish this is by minimizing contact sizes and operating within a vacuum environment. During the interval from t_1 to t_2, a DC current (I_{in}) is applied to the thermoelectric (TE) sample, and the resulting voltage drop across the sample is measured using a voltmeter. Notably, these measurements are performed when there is no temperature difference across the membrane ($\Delta T = 0$), ensuring that the observed voltage (V_R) corresponds directly to the product of the injected current (I_{in}) and the electrical resistance (R) of the sample.

In the subsequent analysis, the system reaches a steady-state condition, and an intriguing relationship emerges between the heat flow through the sample (Q_{Heat}) due to the imposed temperature difference and the heat generated at the junction as a consequence of the Peltier effect induced by the flowing electrical current ($SI_{in}T = K\Delta T$). This equation establishes a vital connection encompassing the Seebeck coefficient (S), thermal conductance (K), and the voltage drop in the electrode (Equation 2- 10).

$$V_S = S\Delta T = \frac{S^2 T I_{in}}{K}$$

Equation 2- 10

During the period from t_2 to t_3, the electrical current is turned off, causing the voltage drop to decrease until it reaches the Seebeck voltage corresponding to the existing temperature difference (ΔT). As time progresses, the temperature difference gradually diminishes, leading to a decrease in the measured voltage, ultimately approaching zero. This drop in voltage is directly associated with the diminishing ΔT.

To sum up, Harman method involves measuring the DC potential drop across the thermoelectric (TE) sample (V_{DC}). This voltage is decomposed into two components: the voltage drop due to resistance (V_R) and the voltage drop due to the Seebeck effect (V_S). This relationship can be expressed as $V_{DC} = V_R + V_S$. Meanwhile, the figure of merit (zT) is determined by the Seebeck coefficient (S), temperature (T), electrical resistance (R), and thermal conductance (K). The equation $zT = (S^2T)/(RK)$ captures this relationship. Importantly, the figure of merit (zT) can also be expressed in terms of the measured voltages:

$$zT = \frac{S^2T}{RK} = \frac{V_S}{V_R} = \frac{V_{dc}}{V_R} - 1$$

Equation 2- 11

Equation 2- 11 elucidates the direct correlation between the measured voltages and the figure of merit (zT) within the Harman method.

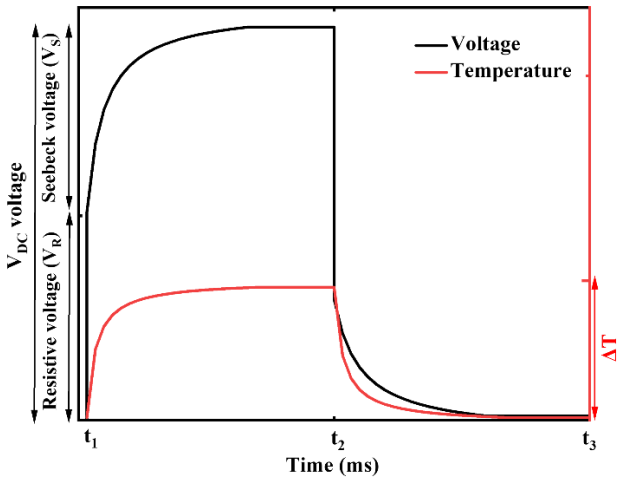


Figure 2-10: Schematic of the Harman measurement method depicting the measured voltage (black) and temperature difference (red) across the sample as a function of time.

2.3.2 zT considering Joule effect as heat source

Before taking into account all losses, we looked at the contribution of internal electrical resistance of thin film membrane in direct zT measurement. The internal resistance of Si thin film is significant, with a magnitude of some kilo-ohms. This is a situation very different from the usual use of the Harman technique when good thermoelectric materials (thus with low electrical resistivity) are measured. When the Peltier effect is not much larger than Joule heating, then a contribution from Joule heating has to be taken into account. Figure 2-11 depicts the schematic of a zT direct measurement device tailored for membranes. The figure showcases the various factors considered within the Harman method considering Joule heating (Q_J). We introduce an axis of symmetry positioned at the center, considering identical membranes. Consequently, the analysis is centered on a single membrane, and by symmetry, we can deduce the same zT value for the second membrane.

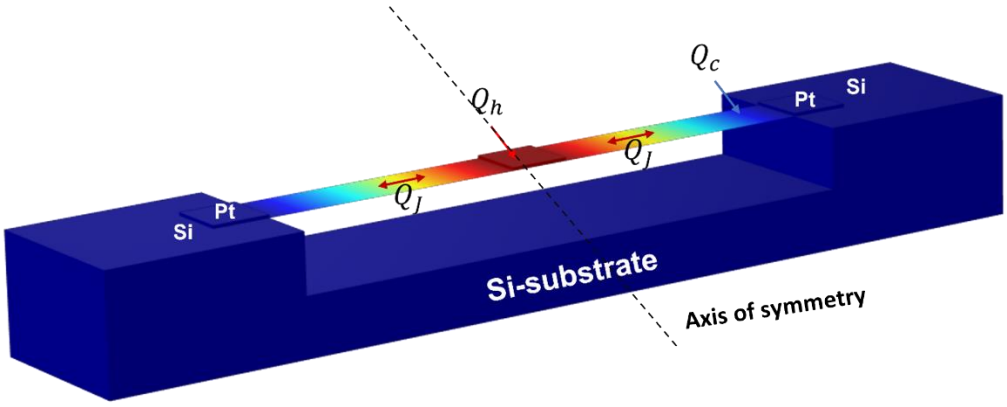


Figure 2-11: Schematic of zT direct measurement device adapted to membranes using Harman technique and considering the Joule heating effect. When a DC current passes through the membrane, Joule heating (Q_J) raises the membrane's temperature.), Peltier heating (Q_h) and Peltier cooling (Q_c) occur at each membrane extremity and the heat flows through the membrane (Q_{Heat}).

Considering the influence of Joule heating (Q_J), where half of it dissipates to the cold side and the other half to the hot side, the formula for the cooling power at the center of the membrane (hot side) is adjusted as depicted by the following equation:

$$Q = SIT - \frac{1}{2}RI_{in}^2 - K\Delta T$$

Equation 2- 12

Under adiabatic condition (Q = 0), ΔT temperature difference across Si membrane is written as a function of Seebeck coefficient, internal resistance, thermal conductance and injected current I_{in}.

$$\Delta T = \frac{1}{K}\left(STI_{in} - \frac{1}{2}RI_{in}^2\right)$$

Equation 2- 13

Equation 2- 13 can be read this way: if we could neglect the internal Joule heating, the total temperature increase would result from the Peltier effect only. However, because Joule effect adds an internal source of heat, half of which flows against the Peltier effect, the net increase of temperature is lowered.

Using Equation 2- 13 , we can replace ΔT in thermoelectric voltage Equation 2- 14. Thus, giving the thermoelectric voltage as a sum of two components: the intrinsic thermoelectric voltage (V_{S0}) and the voltage created due to Joule effect (V_{SJ}). While the first one is proportional to *zT*, the later one is not and should be suppressed.

$$V_S = |S|\Delta T = |S|\frac{1}{K}\left(STI_{in} - \frac{1}{2}RI_{in}^2\right)$$
$$V_S = V_{S0} + V_{SJ}$$

Equation 2- 14

$$V_{S0} = \frac{S^2TI_{in}}{K},\ V_{SJ} = -|S|\frac{RI_{in}^2}{2K}$$

Hence, *zT* figure of merit is equal to

$$zT = \frac{S^2T}{RK} = \frac{V_{S0}}{V_R}$$

Equation 2- 15

With V_R is the resistive voltage:

$$V_R = RI_{in}$$

Equation 2- 16

To determine *zT*, we take out V_{S0} from V_S by using two opposite current injection regimes as shown in Figure 2-12. Regime 1 (from 0 to t_1): Injection of positive direct current (I_{in} = I). At t = 0, the detected voltage is the resistive voltage V_R. The induced current generates a temperature difference through the membrane. At saturation in regime 1, the measured voltage is equivalent to the sum of the resistive voltage and the thermoelectric voltage ($V_R + V_{S0} + V_{SJ}$). Regime 3 (from t_2 to t_3): Injection of negative direct current (I_{in} = - I). The induced current generates an opposite temperature difference through the membrane. At the saturation in regime 3, the measured voltage is equivalent to the sum of the resistive voltage and the thermoelectric voltage ($-V_R - V_{S0} + V_{SJ}$). The fact that V_{SJ} is a quadratic function of I_{in}, enables us to distinguish V_{S0} and utilize it to calculate *zT*. Between these two regimes, we have regime 2 (from t_1 to t_2), where no current is injected in the system in order to allow the membrane to go back to its initial conditions ($\Delta T = 0$).

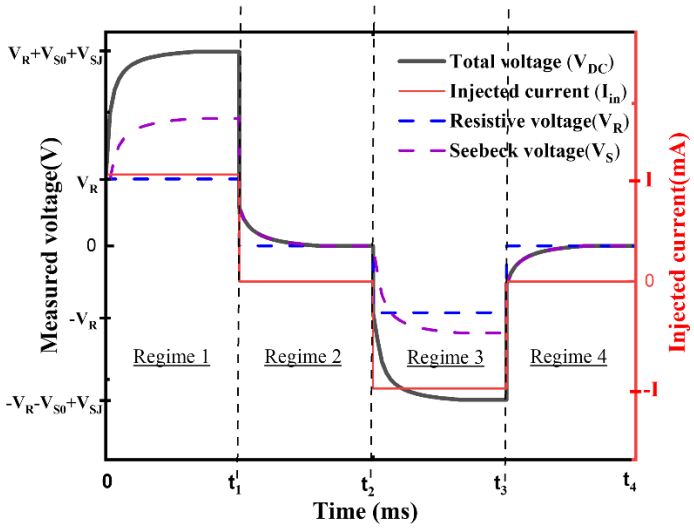


Figure 2-12: V_{s0} extraction method using two opposite values of injected current. Injected current in the system (red line), measured total voltage (V_{DC}) across membranes (black line), measured Seebeck voltage (V_S) across membranes (purple dashed line), measured resistive voltage (V_R) across membranes (blue dashed line) are reported as a function of time.

In summary, for a nanostructured TE material under ideal conditions where Joule heating is considered as a heat source (in addition to the Peltier effect) the *zT* figure of merit can be calculated as follows:

a. Employ two opposing DC currents to eliminate the Joule heating contribution from the Seebeck voltage and determine the Seebeck voltage (V_{S0}).
b. Measure the resistive voltage (V_R) either by injecting a DC current and measuring the resulting voltage before creating a temperature difference across the TE material, or by injecting a high-frequency AC current to suppress the Peltier effect.

Once both V_{S0} and V_R are determined, the *zT* value is obtained by taking the ratio of V_{S0} to V_R. Furthermore, in a periodic situation with an injected current in the form of square waves, each having the same duration, it's important to note that the average value of the measured voltage is not zero. Additionally, the maximum amplitude of this measured voltage can be calculated as $2(V_R + V_{S0})$. This technique provides insights into the behavior of the measured voltage in response to the square wave current input and allows us to distinguish V_{S0} from V_S.

2.3.3 zT considering all losses terms

In this section, our investigation focuses on determining the figure of merit (*zT*) of our nanostructured membranes, taking into account heat losses and Joule heating sources. To ensure an accurate and comprehensive analysis, we consider various hypotheses and assumptions. The conditions considered in this study include:

- Temperature uniformity: The temperature difference (ΔT) along the membrane is low, typically within a practical range of ≤ 40K. As a result, properties such as the Seebeck coefficient (S), electrical resistivity (ρ), and thermal conductivity (κ) are treated as constants along the membrane.
- Negligible effects of measurement pads: The measurement pads are positioned far from the membrane, resulting in a temperature difference (ΔT) of zero at the interface. Consequently, thermal losses and the Seebeck effect in the lead wires are disregarded.
- Negligible Pt-thermocouple effect: The Seebeck coefficient of platinum (S_{Pt}) is considered negligible compared to the Seebeck coefficient of silicon (S_{Si}), with S_{Pt} being approximately -3µV/K at 300K.
- Vacuum conditions: All measurements are conducted under vacuum, allowing the neglect of convective heat losses (convection).
- Platinum dimensions: The width of platinum at the center of the membrane is twice that of the platinum at the sides, denoted as $R_C = R_{C1} = R_{C3} = R_{C2}/2$ (as depicted in Figure 2-14-a).
- In the subsequent section, the thermoelectric material under investigation is an n-type material.

Figure 2-13 provides a visual overview of the device configuration and highlights the comprehensive consideration of various factors within the Harman method. In particular, the figure encompasses the incorporation of all losses.

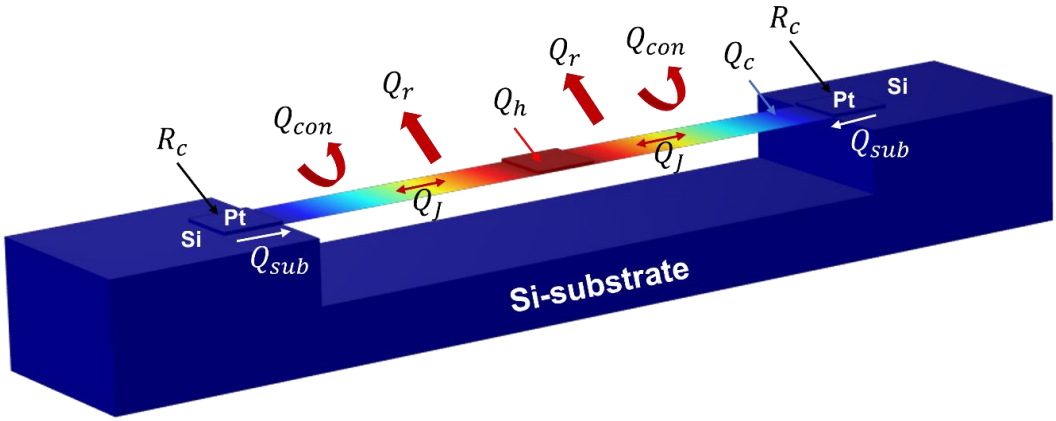


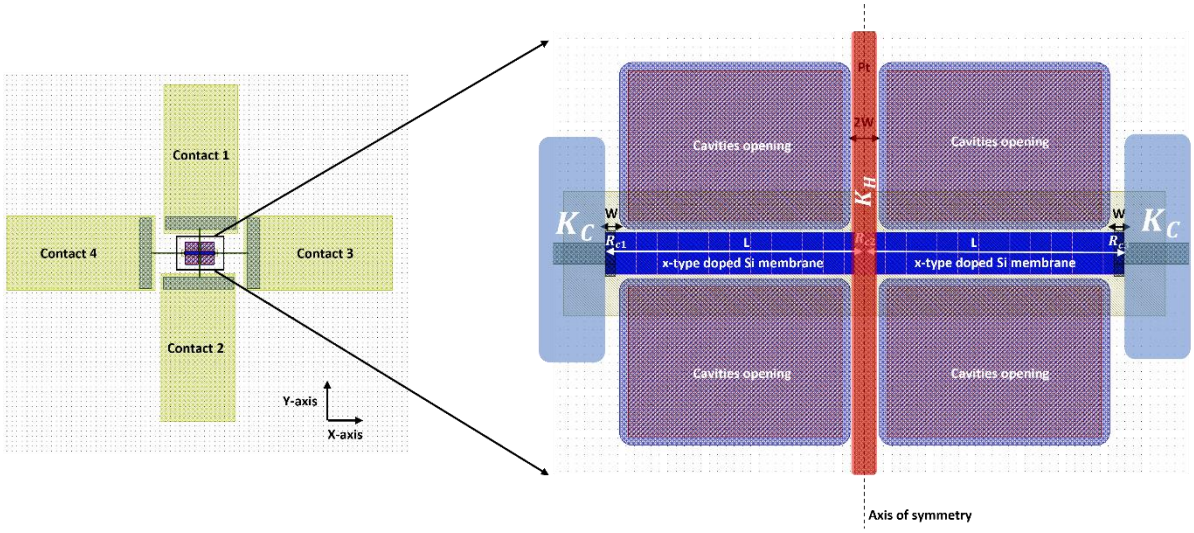
Figure 2-13: Schematic of zT direct measurement device adapted to membranes. When a DC current passes through the membrane, Joule heating (Q_J) raises the membrane's temperature. Heat flow from the membrane to the environment occurs via conduction through the anchors at the extremities (Q_{sub}), convection (Q_{con}), and radiation (Q_r). With a DC current, Peltier heating (Q_h) and Peltier cooling (Q_c) occur at each membrane extremity.

The measurements are conducted under adiabatic conditions, where the system is thermally isolated from its surroundings, ensuring no thermal exchange occurs with the external environment. When considering the membrane as our adiabatic system, heat losses occurring within this system are as follows:

- **Conduction Losses:** These are heat losses through the following components:
  - Platinum Arm at the Center (K_H)
  - Platinum Trail and Substrate at the Cold Side (K_C)
- **Radiation Losses (Qr)**
- **Contact resistances**: at the interface Pt/Si (RCx) with x = 1, 2, 3.
- **Platinum Resistance (R_{Pt}):** Heat dissipation arises due to the electrical resistance of the platinum material.

By considering these parasitic factors, we aim to obtain a comprehensive understanding of the *zT* figure of merit in our nanostructured membranes. Practically, heat losses and Joule heating have an effect on the temperature distribution of the sample, resulting in a difference between *zT* derived by the classical Harman method (zT_H) and the intrinsic (zT_i). Figure 2-14-a illustrates the layout of the *zT* measurement device, highlighting the conduction losses through the center (K_H) in red and through the substrate (K_C) in cyan. To simplify the study, an axis of symmetry is placed at the center, assuming identical membranes. Thus, the analysis focuses on a single membrane, and by symmetry, we can infer the same zT_i for the second membrane. Figure 2-14-b depicts the thermal-electrical analogy of all the parasitic terms on the studied membrane, represented by a blue rectangle. To further simplify the electrical circuit, the resulting radiative heat resistance and the Joule heating source are positioned at the center of the membrane at the average temperature ($\bar{T}$), as shown in Figure 2-14-c.

a)



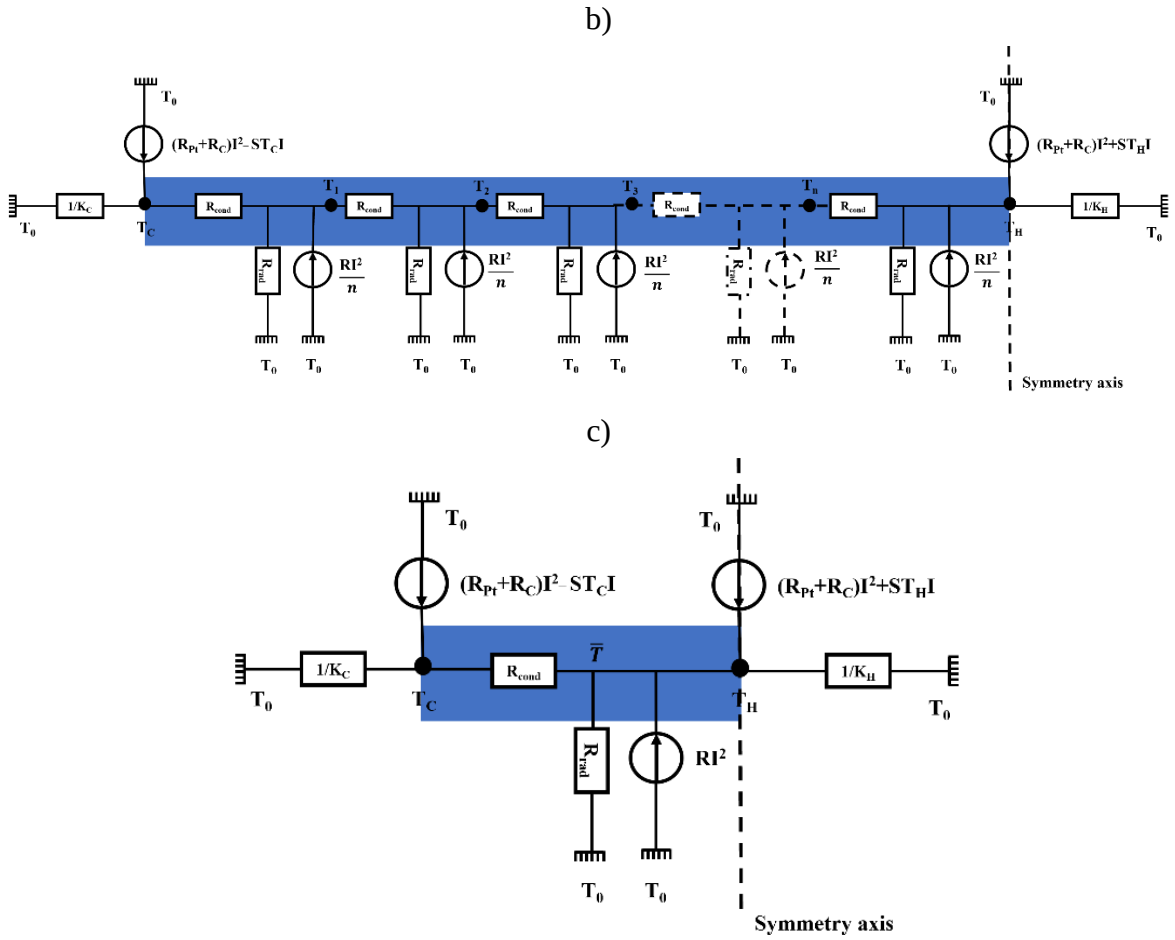


Figure 2-14:a) Layout of the zT measurement device illustrating conduction losses through the center (K_H) in red and through the substrate (K_C) in blue light. b) Thermal-electrical analogy of parasitic terms on the studied membrane, showcasing the various factors influencing the zT measurement. c) Simplified electrical circuit representation with the placement of radiative heat resistance (R_{rad}) and Joule heating source (RI^2) at the center of the membrane at the average temperature ($\bar{T}$)across the membrane.

We develop a thermoelectric relationship that accounts for all parasitic thermal effects specific to nanostructured membranes. To do so, I follow the methodology of Kwon *et al.*[71] i.e. to quantify the energy balance in two subparts of the membrane, This involves formulating energy balance equations for two distinct areas(Figure 2-15-a): the cold side area (depicted in Figure 2-15-b) and the remaining portion of the membrane (illustrated in Figure 2-16). To introduce a controlled heat source, we position it at the center of the platform, allowing the heat to be dissipated through the membranes towards the bulk silicon anchors. This comprehensive approach enables a thorough examination of the energy flow and thermal behavior within the membrane structure.

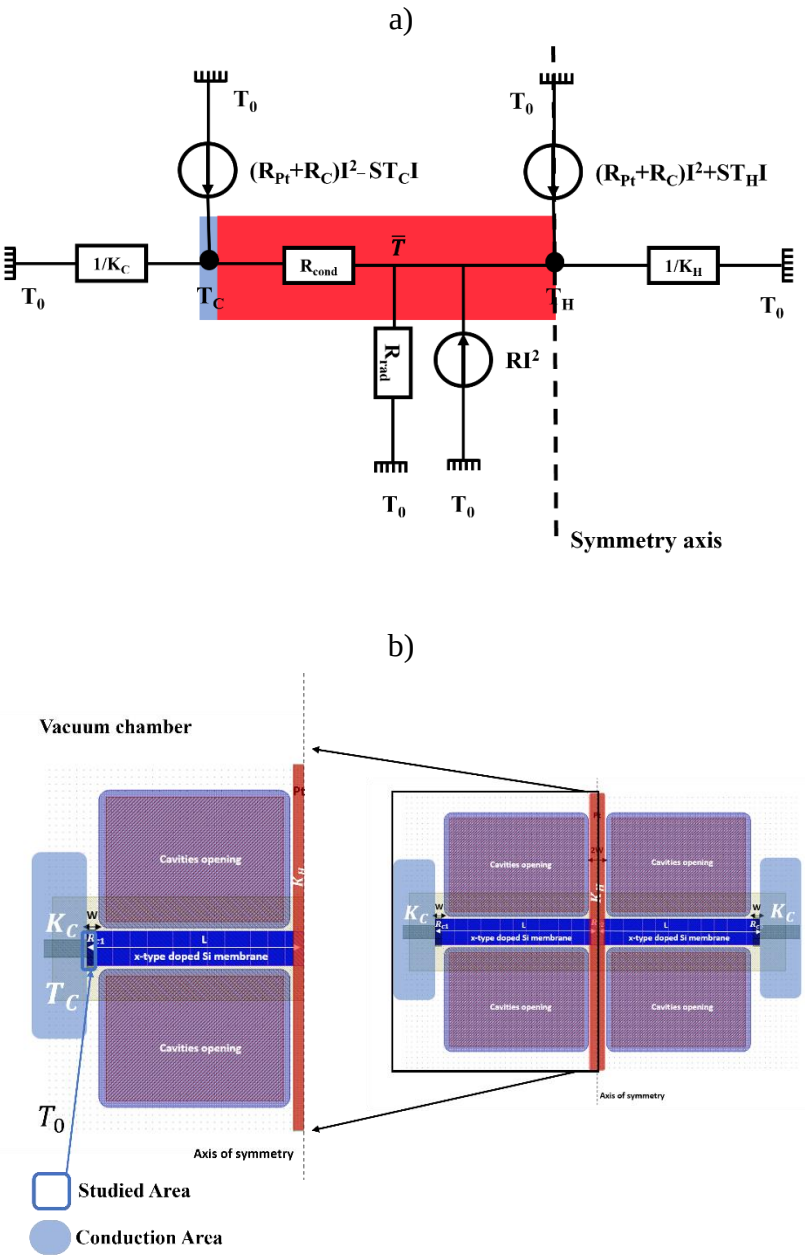


Figure 2-15: a) Simplified electrical circuit representation with the two distinct studied areas; cold side (blue) and the remaining portion of the membrane (red). b) On the right, zT direct measurement device adapted to membranes. On the left, close up view of one suspended Si membrane defining the cold side area (blue bordered square without fill in), conduction area (blue square with fill in) and all parasitic terms taken into consideration for determination of energy balance equation in cold side area.

For a Harman measurement sample with DC current, an energy balance for the cold-side surface with temperature T_C is:

$$S_{Si} I_{in} T_C = (R_C + R_{pt}) {I_{in}}^2 + K_C (T_0 - T_C) + \kappa \frac{A \Delta T}{L}$$

Equation 2- 17

L is membrane's length, A is membrane's cross-section area, K_C is the thermal conductance of Pt and substrate, T_0 is the reference temperature, R_C is the electrical contact resistance between Pt and Si, R_{Pt} is the electrical resistance of Pt, and κ is the thermal conductivity of x-doped Si membrane with x is n-type or p-type.

The energy balance analysis will now be performed for the remaining section of the sample, encompassing the hot side contact with temperature T_H and extending along the membrane (Figure 2-16). The energy balance equation for this assessment is as follows:

$$S_{Si} I_{in} T_H + (R + R_C + R_{pt}) {I_{in}}^2 = K_H (T_H - T_0) + \kappa \frac{A\Delta T}{L} + \beta P L (\bar{T} - T_0)$$

Equation 2- 18

Where β is the radiative heat transfer coefficient, P is the membrane's perimeter, $\bar{T}$ and is the average temperature across the membrane.

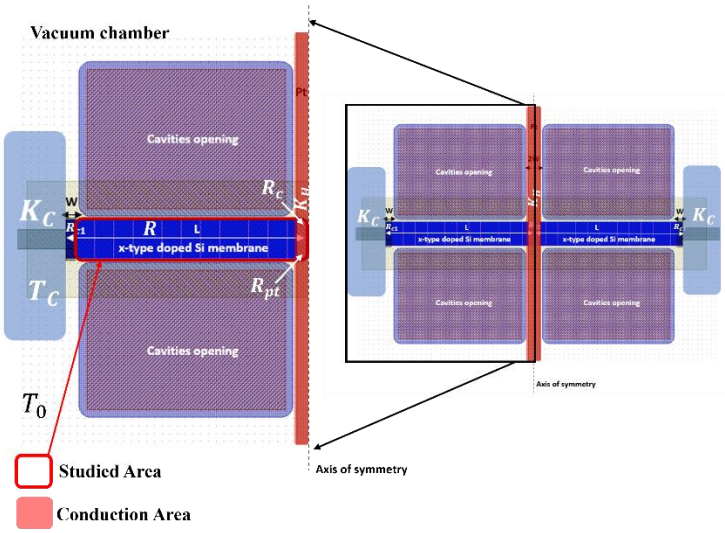


Figure 2-16: On the right, zT direct measurement device adapted to membranes. On the left, close up view of one suspended Si membrane defining the studied area (red bordered square without fill in), conduction area (red square with fill in) and all parasitic terms taken into consideration for the determination of the energy balance equation at studied area.

By combining these two energy balances (Equation 2- 17 and Equation 2- 18) and putting them into the equation as a function of Vdc, we obtain the extended Harman relation as:

$$zT_i = \left(\frac{V_{dc}}{V_R} - 1\right)\left(1 - \frac{\rho L^2 {I_{in}}^2}{2A^2\kappa\Delta T} + \frac{K_C L}{2A\kappa\Delta T}(T_O - T_C) + \frac{K_H L}{2A\kappa\Delta T}(T_H - T_O) + \frac{\beta P L^2}{2A\kappa\Delta T}(\bar{T} - T_O)\right)$$

Equation 2- 19

And as a function of zT_H as:

$$zT_i = zT_H \left(1 + \left(\frac{K_C}{2\kappa\Delta T}(T_O - T_C) + \frac{K_H}{2\kappa\Delta T}(T_H - T_O)\right)\frac{L}{A} + \left(\frac{\beta P A(\bar{T} - T_O) - \rho I^2}{2\kappa\Delta T}\right)\frac{L^2}{A^2}\right)$$

Equation 2- 20

Equation 2- 20 gives the intrinsic figure of merit (zT_i) as a function of the membrane's shape factor, which is defined as L/A. The ratio of zT_i to zT_H is signified as a correction factor,

composed of two terms; the first term is the difference between radiative heat loss and Joule heating which is, then, divided by the conductive heat flow within the sample. The second term is the sum of the ratio of the thermal conductances between the platinum arm at the center (K_H), the platinum wire and substrate at cold side (K_C) and membrane. Due to the symmetrical concept of contacts at extremities of each membrane, losses by the platinum resistance and the contact resistance are eliminated.

The modified Harman's technique Equation 2- 20 enables the determination of the intrinsic figure of merit (zTi) based on measurement of the classical Harman's technique (zT_H). The accurate determination of various loss terms that depend on factors beyond just the material properties can indeed be challenging. In our approach, we aim to determine zT_i without the need to explicitly calculate these factors. Instead, we will employ a graphical method by plotting the reciprocal of zT_H, which represents our measurement, as a function of L/A. Subsequently, we will fit this data using a second-order polynomial equation. This method allows us to derive an effective zT_i value without directly quantifying the extrinsic factors. The relation between zT_H and zTi is expressed as:

$$\frac{1}{zT_H} = \frac{1}{zT_i}\left(1 + \left(\frac{K_C}{2\kappa\Delta T}(T_O - T_C) + \frac{K_H}{2\kappa\Delta T}\ (T_H - T_O)\right)\frac{L}{A} + \left(\frac{\beta PA(\bar{T} - T_O) - \rho I^2}{2\kappa\Delta T}\right)\frac{L^2}{A^2}\right)$$

Equation 2- 21

Therefore, ($1/ zT_H$) is approximated as a second polynomial function of the membrane shape factor. The correction factor decreases in the following two cases: (i) the conductive heat flow within the membrane becomes larger against the heat losses and Joules heating (ii) membrane shape factor becomes small. If L/A = 0, the intrinsic Harman figure of merit becomes equal to classic Harman's figure of merit. Our study aims to measure different membrane geometries in order to obtain zT_H data as a function of L/A. Thus, the intrinsic figure of merit (zT_i) can be determined by fitting the obtained zT_H data with a second order polynomial.

2.4 Modeling study of zT direct measurement adapted to membranes

To assess the reliability of our modified transient Harman technique, we have chosen to use Finite Element Method (FEM). This decision is based on several key reasons. Firstly, our analytical formula lacks the capability to provide accurate magnitude estimates, necessitating quantitative results that FEM can provide. Additionally, FEM allows us to create a model that considers the spatial distribution of temperature, which is more realistic than our initial assumption of a uniform temperature gradient. Moreover, alongside our device fabrication efforts, this approach allows us to validate our methodology and build a model that can be refined using real-world data, aligning our theoretical framework with practical findings.

This section focuses on providing a comprehensive understanding of the finite element method, including the definition of the method itself, the equations and boundary conditions employed, and the presentation of the obtained results.

2.4.1 Finite Element Method definition

Finite Element Method (FEM) is a method that solves continuous partial differential equations systems by reducing the problem onto a discrete set of nodes in space. These functions are then transformed into simple vectors (in a vector space), which may be handled by numerical methods. It is a common technique for numerically resolving differential equations that appear in engineering and mathematical modeling. The conventional topics of

structural analysis, heat transfer, fluid flow, mass transport, and electromagnetic potential are typical areas of interest.

To solve a problem, the FEM subdivides a large system into smaller, simpler parts that are called finite elements. This is achieved by a particular space discretization in the space dimensions, which is implemented by the construction of a mesh of the object: the numerical domain for the solution, which has a finite number of points. The finite element method formulation of a boundary value problem finally results in a system of algebraic equations. The method approximates the unknown function over the domain [73]. The simple equations that model these finite elements are then assembled into a larger system of equations that models the entire problem. The FEM then approximates a solution by minimizing an associated error function via the calculus of variations.

2.4.2 Heat transport equations definition

To evaluate the consistency of our adapted transient Harman technique, FEM is used. Thermoelectric coupling is based on the simultaneous solving of carrier and heat transport equations. All the following equations are local, but for the sake of clarity, the space dependence is omitted. According to the non-isothermal drift diffusion model [74] , the current densities are provided and the assumption is that majority carriers control transport.

$$\overrightarrow{J_x}(T) = \sigma_x(T) \cdot \left[\vec{E} + |S_x(T)| \cdot \vec{\nabla}(T)\right]$$

Equation 2- 22

With σ_x, S_x and $\vec{E}$ being the electrical conductivity, the Seebeck coefficient and the local electrical field where x stands for n or p, depending on the doping area.

$$\sigma_x(T) = q.\mu_x(T).x(T)$$

Equation 2- 23

$$S_n(T) = -\frac{k_B}{q} \cdot [3/2 + ln\,(\frac{N_C(T)}{n(T)})]$$

$$S_p(T) = \frac{k_B}{q} \cdot [3/2 + ln\,(\frac{N_V(T)}{p(T)})]$$

Equation 2- 24

$$n(T) = \frac{N_D}{2} + \sqrt{\frac{N_D^2}{4} + n_i^2(T)}$$

$$p(T) = \frac{N_A}{2} + \sqrt{\frac{N_A^2}{4} + n_i^2(T)}$$

$$n_i(T) = \sqrt{N_C(T) \cdot N_V(T)} \cdot exp\,(-\frac{E_G(T)}{2 \cdot k_B \cdot T})$$

Equation 2- 25

$$N_C(T) = 2 \cdot \left(\frac{2\pi \cdot k_B \cdot T \cdot m_e}{h^2}\right)^{3/2}$$

$$N_V(T) = 2 \cdot \left(\frac{2\pi \cdot k_B \cdot T \cdot m_h}{h^2}\right)^{3/2}$$

Equation 2- 26

With k_B being the Boltzmann constant ($1.38.10^{-23}$ J/K), q the elementary charge ($1.62.10^{-19}$ C), h the Planck constant ($6.62.10^{-34}$ m^2 Kg/s), p(T) and n(T) are the hole and electron densities respectively. Where $N_V(T)$ and $N_C(T)$ denote the effective density of states in valence and conduction bands respectively. The doping level in the thermoelectric elements is set to $10^{19}cm^{-3}$ for which the figure-of-merit (zT) is optimal [75], represented by N_D and N_A for the n and p doped elements respectively. The S_p and S_n terms represent the p and n doped Seebeck coefficient, given by the Mott law [76] and defined in the previous chapter. Finally, $E_G(T)$ is the energy gap of the semiconductors, σ_x the electrical conductivities while μ_x are mobilities of the p and n regions respectively (these mobilities are given by the Arora model [77]). The mobilities of p and n regions are given by the below equation:

$$\mu_n(N_D, T) = \mu_{min} \cdot \left(\frac{T}{300}\right)^{\alpha} + \frac{\mu_{max} \cdot \left(\frac{T}{300}\right)^{\beta}}{1 + \frac{N_D}{N_{ref} \cdot \left(\frac{T}{300}\right)^{\gamma}}}$$

$$\mu_p(N_A, T) = \mu_{min} \cdot \left(\frac{T}{300}\right)^{\alpha} + \frac{\mu_{max} \cdot \left(\frac{T}{300}\right)^{\beta}}{1 + \frac{N_A}{N_{ref} \cdot \left(\frac{T}{300}\right)^{\gamma}}}$$

Equation 2- 27

Table 2-1: silicon maximal and minimal mobilities and coefficients for the Arora model [77].

Material	μ_{min} ($cm^2/V/s$)	μ_{max} ($cm^2/V/s$)	N_{ref} (cm^{-3})	α	β	γ
n-type Si	88	1252	$1.432 \cdot 10^{17}$	-0.57	-2.33	2.546
p-type Si	54.3	407	$2.67 \cdot 10^{17}$			

At high temperatures beyond 100K, conduction is limited by phonon-phonon collisions. Indeed, as temperature increases, modes with larger wavevectors become increasingly populated, allowing for collisions where the sum of the incident wavevectors exceeds the Brillouin zone boundary (Umklapp processes). These modes are the only ones that contribute to reducing the phonon momentum through transfer to the lattice. As a result, thermal conductivity decreases as:

$$\kappa = \kappa_0 \left(\frac{T_0}{T}\right)^{\delta}$$

Equation 2- 28

Where T_0=300K and κ_0 is the thermal conductivity at 300K. A typical value for the coefficient δ, obtained from literature data, is 1.65[78].

2.4.3 *Physical modeling of zT direct measurement on a thin film*

To assess the modified Harman's technique, Finite Element Modeling (FEM) is performed using Software "Comsol Multiphysics". The objective is to quantify how the method adapts to sizes and orders of magnitudes found in our suspended membranes. Figure 2-17 gives the design of our device in Comsol Multiphysics. In this design, no contacts are needed because all measurements are taken directly from the desired area.

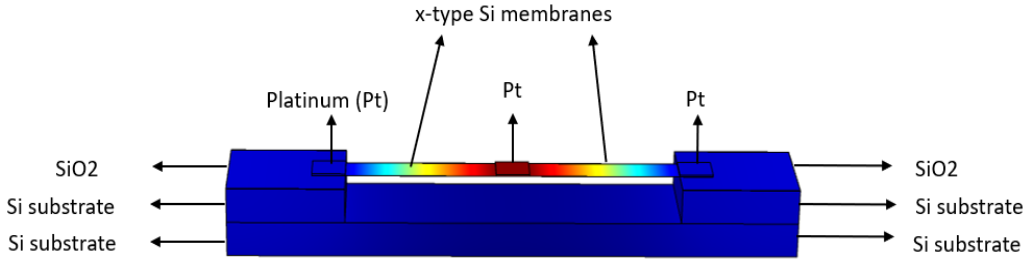


Figure 2-17: Design of zT direct measurement device adapted to membranes in Comsol Multiphysics, showing the evolution of the thermal gradient across the planar Si membranes.

Modeling is performed with the following boundary conditions in place:

- The studied membrane is of length equal to 60μm, width equal to 10μm and thickness equal to 60 nm.
- Current injection, voltage and hot temperature measurements occur at the center of the platform.
- The heat is routed to the cold substrate by thermal conduction through the silicon membranes and the anchors at the extremities of the membranes.
- All measurements are performed under vacuum and near room temperature (no conducto-convection).
- Thermal radiation is neglected.
- The bottom silicon substrate temperature is fixed at 300K using a heat sink to enable equilibrium at different temperatures to be established quickly.
- Both ends of the membranes are connected to the ground.
- Two thermal conductivities are considered:
    - 35 W/m.K: reduced thermal conductivity achieved by Haras *el al.* [79][3]
    - 149 W/m.K: Bulk silicon thermal conductivity.

The modeling section can be divided into 2 subsections: *i)* direct *zT* determination using Harman technique, *ii)* direct *zT* determination taking into account Joule heating source.

2.4.3.1 *zT direct measurement using Harman technique*

In this section, we will employ the finite element modeling (FEM) approach to investigate the influence of thermal losses at the nanoscale. We will assess their impact on both bulk materials and thin films. Additionally, two variations of the Harman technique will be

[3] The choice of this value is somewhat arbitrary. The objective was to assess the difference between bulk and thin membranes using realistic values.

utilized: the Classical Harman technique for determining *zT* in bulk materials and a modified Harman technique specifically adapted for membrane analysis. The measurement conditions discussed earlier will be consistently applied across all the *zT* determination techniques in our analysis.

The modeling analysis in this study focuses on investigating the influence of Joule heating on the *zT* figure of merit. The parasitic terms considered in the modeling include the Joule heating sources and contact electrical resistances. Notably, the measurement setup does not involve the use of probes, and instead, voltage determination and current injection are performed using terminals in the software "Comsol Multiphysics". Additionally, the design does not account for heat losses through the wires to the measurement pads during experimental conditions.

The analysis commences with the direct *zT* measurement using the Classical Harman technique for both bulk Si and nanostructured Si. A DC current is introduced at the central terminal, and subsequently, the voltage between the center (representing the first side of the membrane) and the side (representing the second side of the membrane) is measured. By determining the resistive voltage in the absence of a temperature difference and the thermoelectric voltage at steady state (where the temperature difference reaches 40K), the *zT* figure of merit is calculated as the ratio of these two voltages. Figure 2-18-a and Figure 2-18-c showcase the measured voltage and the created temperature difference over time for both thermal conductivities 35W/m.K and 149W/m.K, while a detailed view of the increasing slope from the initial state to steady state is presented in Figure 2-18-b and Figure 2-18-d.

The classical Harman technique requires the TE material under study to be homogeneous, with constant transport properties. As a result, the modeling analysis is conducted at a low temperature difference of 40K. The measured voltage exhibits an increasing trend as the temperature difference increases. Once the steady state is reached, where the temperature difference across the membrane remains constant, the measured voltage also becomes constant. When the current is cut off, the measured voltage drops to the Seebeck voltage corresponding to the instantaneous temperature difference and decreases as the temperature difference decreases. Figure 2-18-d illustrates that the resistive voltage generated significantly surpasses the thermoelectric voltage. This observation emphasizes that the internal resistance of Si is relatively high, on the order of several kilohms, and this contributes to the increase in V_{SJ}, which is directly proportional to the temperature difference (ΔT). Utilizing the Classical Harman technique ($zT_H=(V_{DC}/V_R)$ -1) in this scenario yields a *zT* value of 0.026 for a thermal conductivity of 35W/m.K and 0.021 for a thermal conductivity of 149W/m.K.

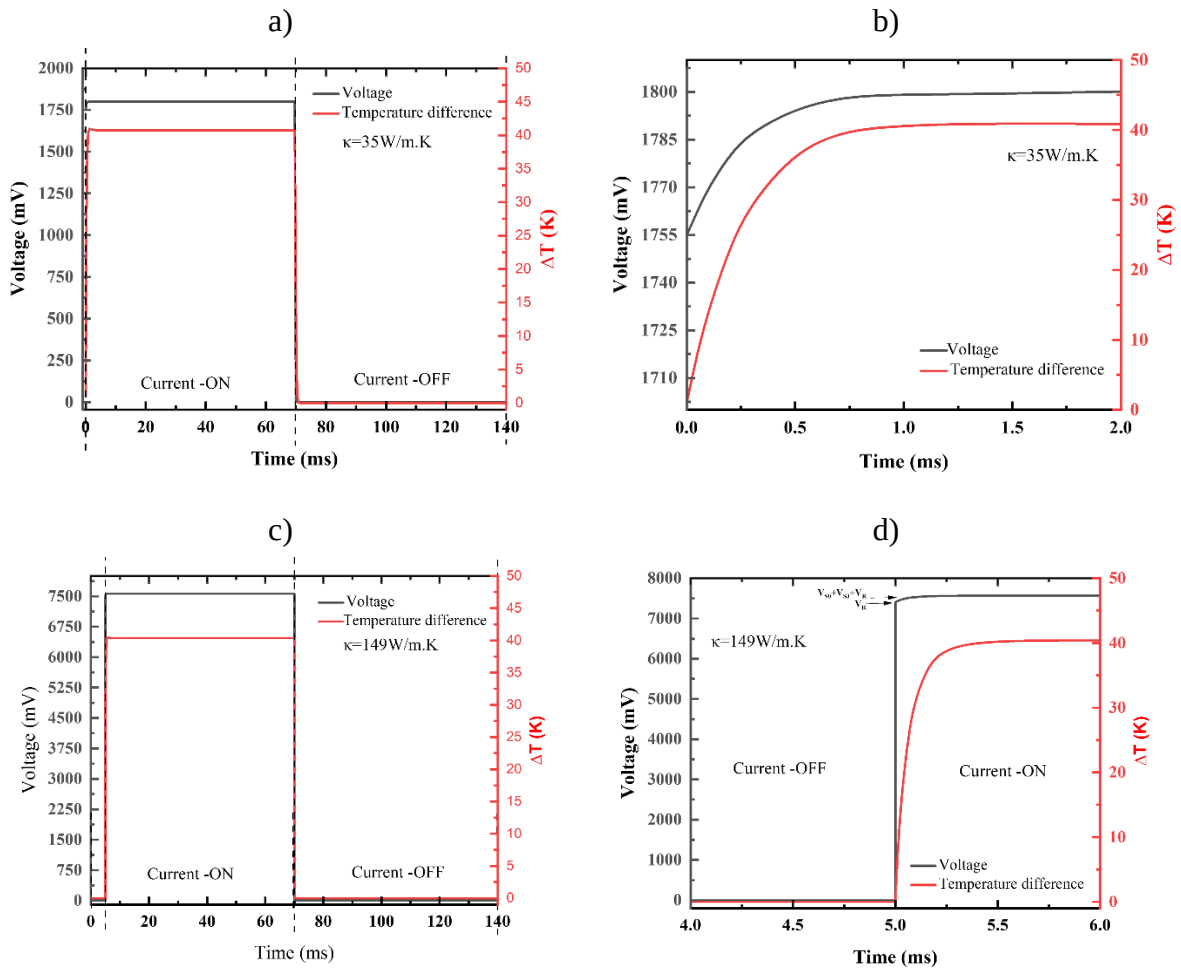


Figure 2-18: (a,c)Measured voltage and temperature difference across membrane with varying thermal conductivity. (b,d) Close-up: Rising slope analysis of bulk and nanostructured Si.

To compare the Classical Harman *zT* with the analytical *zT* calculated using the formula, the electrical conductivity and Seebeck coefficient values of the membrane are extracted from Comsol. Table 2-2 provides a summary of the calculated Seebeck coefficient and electrical conductivity using Equation 2- 24 and Equation 2- 23. By applying the *zT* formula, which relates the transport properties, we find that the analytical *zT* figure of merit equals 0.00145 for Bulk Si (149W/m.K) and 0.00619 for nanostructured Si (35W/m.K).

Table 2-2:Analytical zT figure of merit for both thermal conductivities; 149W/m.K and 35W/m.K.

Thermal conductivity	Seebeck coefficient	Electrical conductivity	Figure of merit@340K
149W/m.K	263 μV/K	9206.5 S/m	0.00145
35W/m.K	263 μV/K	9206.5 S/m	0.00619

The significant distinction between the analytical figure of merit and the one derived from the classical Harman technique stems from the omission of Joule effect heating in the Harman technique. The subsequent section focuses on addressing the exclusion of this term within the Harman technique.

2.4.3.2 zT direct measurement considering Joule heating source

The previous section demonstrated that the internal resistance of Si plays a crucial role and exceeds the thermoelectric voltage. Consequently, the classical Harman technique, which directly determines *zT*, is not applicable in this case. To address this limitation, an adapted technique was presented (section 2.3.2) for extracting the Joule heating effect. In this section, we evaluate the efficiency of this technique by employing Finite Element Method simulations.

The introduced technique employs two distinct current injection regimes with opposite polarities to effectively eliminate the Joule heating effect that contributes to the thermoelectric voltage. Figure 2-19 showcases the temporal variations of the temperature difference and the injected current within the nanostructured membrane, which possesses a thermal conductivity of 35W/m.K.

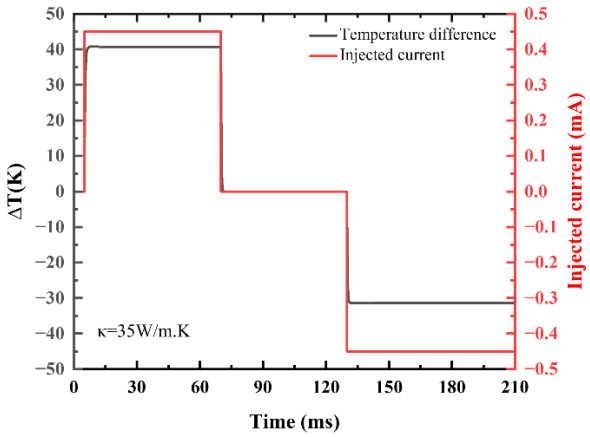


Figure 2-19: Temperature Difference and Injected Current at the center of the planar Si membranes (of length equal to 60µm, width equal to 10µm and thickness of 60nm) over Time in Nanostructured Si Membrane.

Figure 2-19 provides evidence supporting the temperature-dependent nature of the internal parameters of the thermoelectric element. It demonstrates that when a positive current (I_{in} = I) is injected, the temperature difference across the membrane reaches 40K, surpassing the temperature difference observed when a negative current (I_{in} = -I) is injected. This observation further highlights the influence of the current direction on the temperature distribution within the thermoelectric system.

Figure 2-19 illustrates the measured voltage across the membrane during the injection of two opposite currents. Consistent with previous observations, the resistive voltage (V_R) is found to exceed the thermoelectric voltage. At steady state, the measured voltage is a combination of the resistive voltage and the thermoelectric voltage, which consists of the voltage resulting from the Joule effect (V_{SJ}) and the intrinsic thermoelectric voltage (V_{S0}) (as explained in Section 2.3.2). Subsequently, when the positive current is discontinued and the temperature difference returns to zero, the negative current is applied. This leads to the generation of a new temperature difference that reaches a steady state, with the center of the membrane becoming cold and the sides becoming hot. In this case, the measured voltage is the negative of the previously determined resistive voltage, plus the voltage resulting from the Joule effect (V_{SJ}) (since it is a quadratic function of current), and minus the intrinsic thermoelectric voltage (V_{S0}).

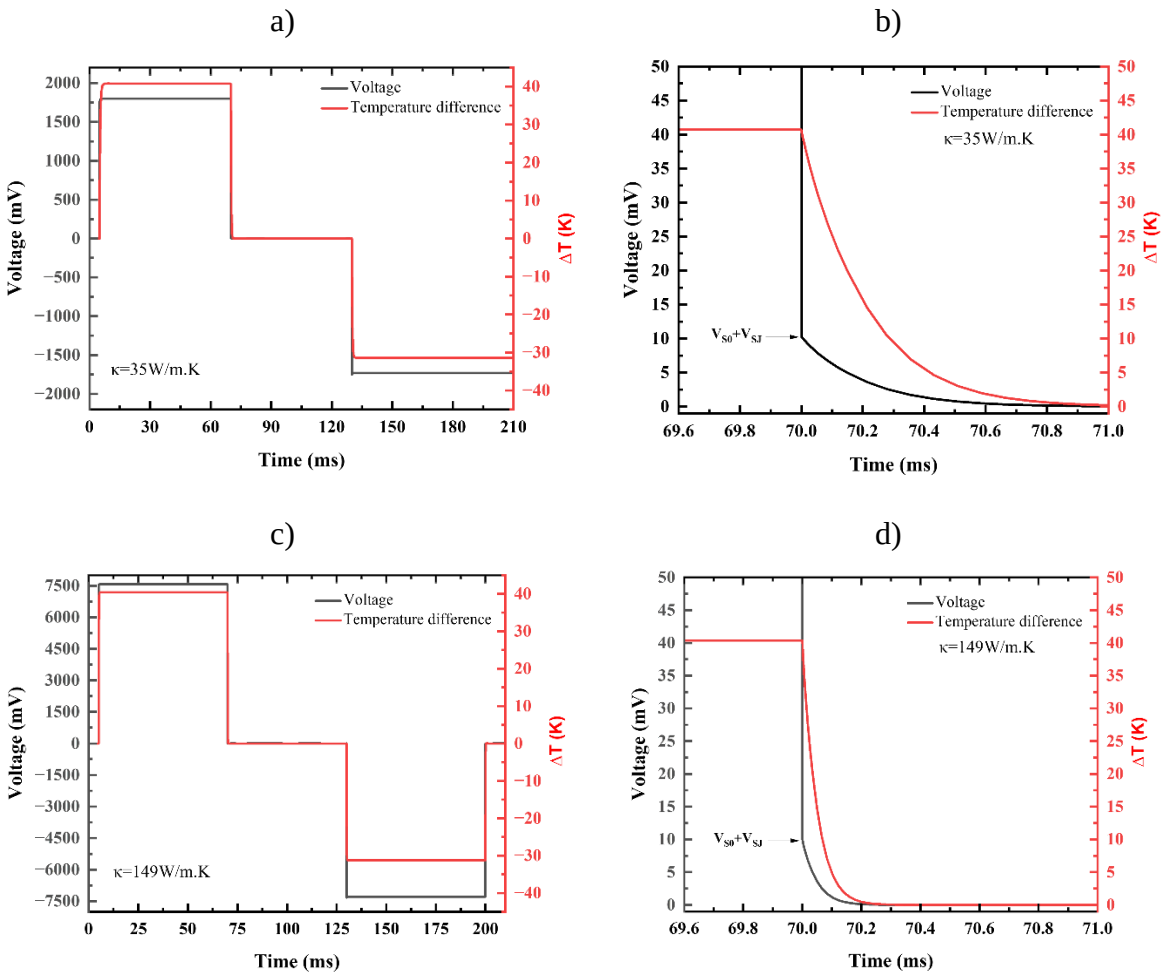


Figure 2-20: (a,c) Voltage and temperature profiles for different thermal conductivities. (b,d) A close-up of the cooling slope and Seebeck voltage for different thermal conductivities.

Figure 2-20-b and Figure 2-20-d demonstrate that the nanostructured Si, with a thermal conductivity of 35W/m. K, requires a certain amount of time to return to its initial state of no temperature difference after the current is disconnected. In comparison, the Bulk Si with a thermal conductivity of 149W/m.K exhibits a faster restoration to a null temperature difference. This behavior can be explained by considering the differences in thermal transport mechanisms between the two materials. The nanostructured Si, due to its lower thermal conductivity, has a higher thermal resistance, which slows down the dissipation of heat and the equalization of temperature across the membrane after the current is turned off. In contrast, the Bulk Si, with its higher thermal conductivity, allows for faster heat dissipation and a quicker restoration to a null temperature difference. The time delay observed in the nanostructured Si membrane, with its lower thermal conductivity, presents a greater opportunity to accurately track the Seebeck voltage using the experimental setup.

The *zT* figure of merit, determined using two opposite current injection regimes for both bulk silicon thermal conductivity and nanostructured Si thermal conductivity under a temperature difference of 40K, is summarized in Table 2-3. Notably, the determined *zT* figure of merit aligns closely with the Analytic figure of merit presented in Table 2-2. This close comparison is attributed to the extraction of the voltage resulting from the Joule effect (V_{SJ}), which surpasses the intrinsic thermoelectric voltage (V_{S0}).

Table 2-3: Measured zT figure of merit of both thermal conductivities; 149W/m.K and 35W/mK.

$V_R + V_{S0} + V_{SJ}$ **(mV)**	V_R **(mV)**	$V_{SJ} - V_R - V_{S0}$ **(mV)**	V_{SJ} **(mV)**	V_{S0} **(mV)**	***zT @ ΔT=40K***	***Analytic zT @ΔT=40K***	**κ (W/m.K)**
7564.58	7406.62	-7280.64	141.97	15.99	0.0021	0.00145	149
1799.82	1754.27	-1729.90	34.96	10.60	0.0060	0.00619	35

In this modeling approach, the only parasitic term considered is the Joule heating. By implementing two opposite currents, the extraction of this heating source from the *zT* figure of merit becomes possible. However, in experimental settings, the thermal losses extend beyond the Joule heating created by the internal resistance of Si. Additional factors such as radiation, thermal conduction through wires to pads, and through the substrate cannot be disregarded. Consequently, further considerations are necessary to eliminate these losses.

To mitigate these additional losses effects in practical experimental scenarios, we should apply this *zT* determination method to membranes with varying lengths and widths. By extrapolating the results of $1/zT_H$ when L/A equals 0, the intrinsic figure of merit (zTi) can be determined using the following formula:

$$\frac{1}{zT_H} = \frac{1}{zT_i}\left(1 + \left(\frac{K_C}{2\kappa\Delta T}(T_O - T_C) + \frac{K_H}{2\kappa\Delta T}\ (T_H - T_O)\right)\frac{L}{A} + \left(\frac{\beta PA(\bar{T} - T_O) - \rho I^2}{2\kappa\Delta T}\right)\frac{L^2}{A^2}\right)$$

2.4.3.3 Direct zT with Nanostructured Membranes: Experimental Parameters

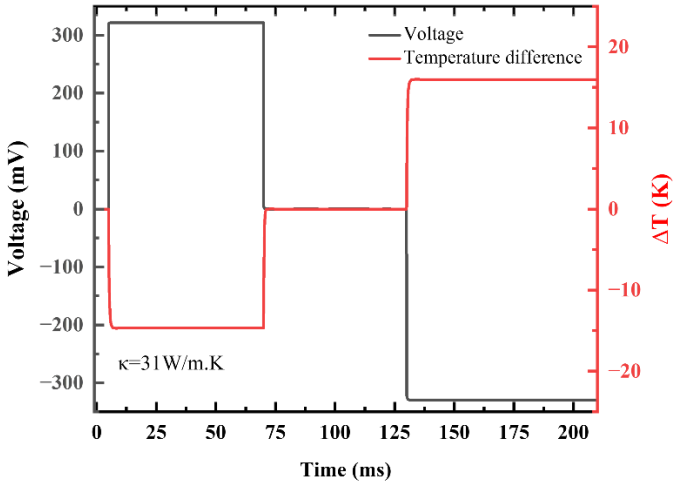
The *zT* figure of merit is recalculated using experimental values obtained from our fabricated membranes. Chapter 4 focuses on characterizing the devices developed in this thesis and presents the measured transport properties of the membranes we fabricated. The thermal conductivity, Seebeck coefficient, and electrical conductivity values used in Comsol Multiphysics (Table 2-4) are derived from the plain p-type membranes.

Table 2-4: Experimental values of plain p-type Si membrane.

Thermal conductivity	Seebeck coefficient	Carrier concentration
31W/m.K	424μV/K	$1.219.10^{19}$ cm^{-3}

For the direct determination of the *zT* figure of merit, a planar membrane with a thickness of 60nm, width of 10µm, and length of 60µm was utilized under a temperature difference of 15K across the membrane. In Figure 2-21-a, the voltage across the membrane was measured over time while injecting opposite currents. Figure 2-21-b displays the temperature distribution in the membrane when a current of 0.1mA was injected. In contrast to the previous study, the current study observed a cooling effect at the center of the membrane rather than a heating effect. In a p-type thermoelectric material, when a positive current is injected, the majority carriers, which are holes, move in the direction of the current. As these holes move away from the junction, a cooling effect occurs at that location due to the Peltier effect. Consequently, the temperature difference between the center of the membrane and the sides is negative during the initial regime when a positive current is injected.

a)



b)

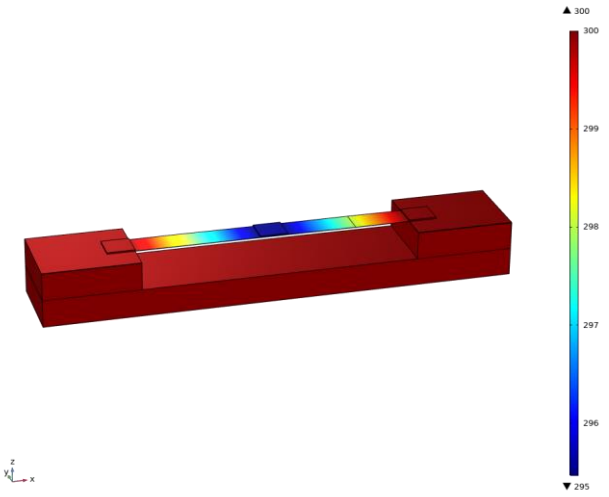


Figure 2-21: a) Measured Voltage and Temperature Profiles across the plain p-type membrane using the measured transport properties. b) Temperature profiles in the plain-p type membrane with an injected current equal to 0.1mA.

Table 2-5 presents the calculated *zT* figure of merit obtained through the modified Harman techniques. The measured voltage resulting from the Joule effect (V_{SJ}) is negative, which aligns with the provided formula, considering that the Seebeck coefficient of a p-type membrane is positive.

$$V_{SJ} = -|S|\frac{RI_{in}^2}{2K}$$

Table 2-5: Measured zT figure of merit of plain p-type membrane using the measured transport properties.

$V_R + V_{S0} + V_{SJ}$ (mV)	V_R (mV)	$V_{SJ} - V_R - V_{S0}$ (mV)	V_{SJ} (mV)	V_{S0} (mV)	zT @ ΔT=15K
321.89	319.27	-329.65	-3.88	6.50	0.020

The experimental data yielded a higher *zT* figure of merit compared to the simulation data. This discrepancy can be attributed to the approach taken in the simulation, where the Seebeck coefficient and electrical conductivity were determined based on the heat transport properties and doping level. Additionally, in the simulation we employed the Mott formula for the Seebeck coefficient determination, which accounts solely for the electronic contribution. A more detailed explanation, including the measurement of the Seebeck coefficient, is provided in Chapter 4 within the dedicated section on Seebeck coefficient measurement.

In addition to the previous study, calibration curves were also prepared. Figure 2-22(a) shows the necessary current for a 30K temperature difference across different thermal conductivity values. Additionally, Figure 2-22(b) assists in determining thermal conductivity values based on the temperature difference observed across the membrane. These data correspond to a membrane with measurements of 70nm in thickness, 10µm in width, and 60µm in length.

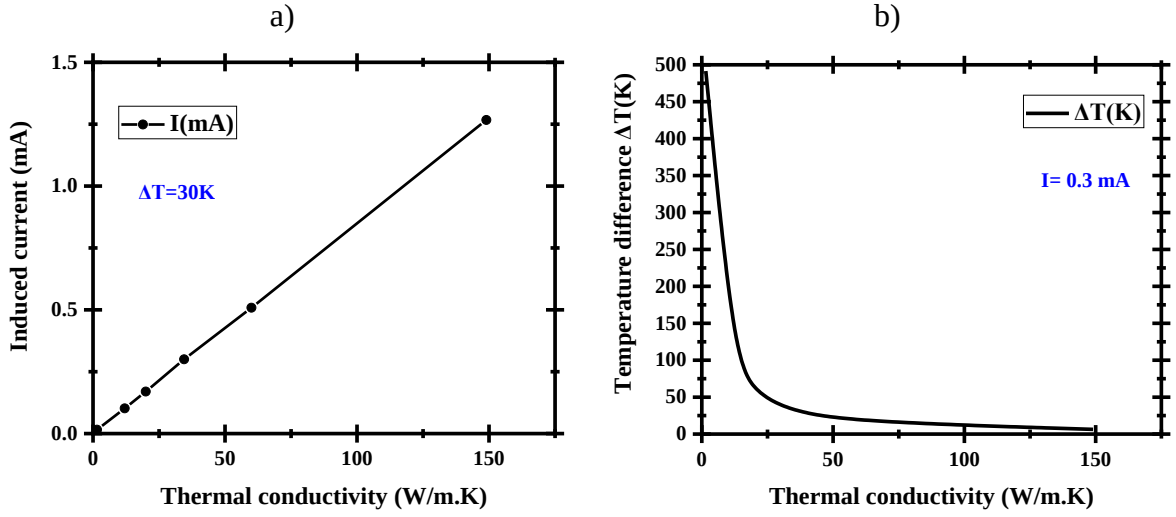


Figure 2-22: Calibration curves: (a) Current vs. thermal conductivity at 30K temperature difference, and (b) Thermal conductivity vs. temperature difference across the membrane (70nm thickness, 10µm width, 60µm length).

Conclusion

This chapter presented an alternative accurate method for direct *zT* figure of merit measurement of nanostructured planar membranes. The studied device is made of two identical suspended membranes with two contacts at the center for current injection and the first voltage measurement, and an additional contact at the extremity of each membrane for the second voltage measurement (the potential difference across the membranes can be derived from these two voltage measurements). The intrinsic figure of merit (zT_i) of planar suspended membranes was given as a function of *i)* Harman figure of merit (zT_H), *ii)* radiative heat loss, *iii)* Joule

heating, *iv)* conductive heat flow across the planar Si membrane and *v)* thermal conductance between the platinum arm at the center, the platinum trail and substrate at cold side.

This chapter also dealt with the finite element modeling (FEM) of *zT* figure of merit direct measurement of a planar Si membrane using the suggested methodology adapted to membranes. The modeling studied *zT* figure of merit of planar Si membranes using two values of silicon thermal conductivity; bulk thermal conductivity and reduced thermal conductivity. It is demonstrated that, unlike in typical thermoelectric materials, silicon exhibits a significantly high internal resistance, leading to substantial Joule heating. This dominant influence of internal resistance in silicon renders the classical Harman technique inapplicable, as it overestimates the thermoelectric voltage in the *zT* figure of merit and inaccurately estimates the magnitude of *zT* for silicon. Furthermore, the modeled *zT* figure of merit using the adapted Harman technique is found to be comparable to those calculated using analytical formulas. This outcome confirms the applicability and validity of the proposed physical modeling approach.

In the upcoming chapter, we will focus on the fabrication process of an integrated metrology device designed specifically for the transient Harman measurement of silicon nano-meshes. The objective is to apply the Modified Harman approach to a practical device and investigate its performance.

Chapter 3 Fabrication of the integrated metrology device dedicated to transient Harman measurement of silicon nano-meshes:

Abstract

In this chapter, the fabrication process of an integrated metrology device dedicated to transient Harman measurement of silicon nano-meshes is described. The main goal is the realization of the integrated measurement device, but also elementary devices that allow the determination of thermoelectric (TE) properties (thermal conductivity, Seebeck coefficient, and electrical conductivity) in order to compare the measured *zT* figure of merit and the analytical *zT* figure of merit.

First, the design of the devices is presented before the fabrication process is described in detail and finally the devices are presented after realization. The devices are fabricated upon the Silicon On Insulator (SOI) wafer with an active silicon (Si) layer of 69 nm thickness.

3.1 Design

Integrated metrology devices dedicated to transient Harman measurement of silicon nano-meshes aiming to directly measure *zT* figure of merit are designed and fabricated with secondary devices. These devices serve to determine the thermal TE properties separately; these properties are then used for determination of the analytic *zT* figure of merit.

Our fabricated sample contains several devices. The first device is dedicated to direct measurement of *zT* figure of merit and the subsequent three devices are used to measure resistivity, Seebeck coefficient and thermal conductivity. All these measurements are valid for a diverse set of suspended planar silicon membrane geometries for both non-phonon and phonon engineered versions.

Figure 3-1 gives the 3-inch wafer containing the following devices:

1- Transient Harman devices
2- Doping level measurement platforms
3- Seebeck coefficient measurement devices

4- Thermal conductivity measurement devices

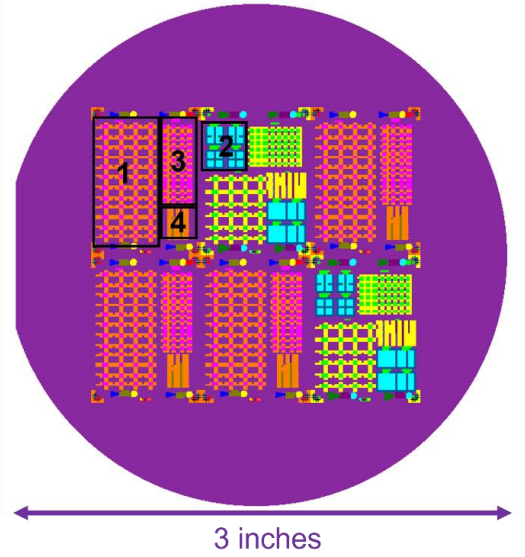


Figure 3-1: Devices contained on the 3inch wafer overview.

To ensure that the measured thermoelectric properties are associated with the appropriate demonstrators, all devices are fabricated on the same wafer. This is feasible because all device realization techniques used are compatible (these techniques are discussed in section 3.2). To explore the impact of phonon engineering on thermoelectric properties and performances (*zT* figure of merit), the phonon and non-phonon engineered versions of all devices are created and implemented for both Si-type materials (n-type and p-type).

The wafer contains six cells (Figure 3-1), four of which are identical cells containing transient Harman devices, Seebeck coefficient measurement devices and thermal conductivity measurement devices for a wide range of suspended planar silicon membrane geometries (Figure 3-2) . For this analysis, samples were fabricated at lengths of 20μm, 60 μm,100 μm and 140 μm; each length being individually fabricated three times with widths of 10 μm, 20 μm and 30 μm; equaling a total number of 12 geometries in both non-phonon engineered (NPE) and phonon engineered (PE) versions for each doping type (n-type and p-type) as detailed in Table 3-1.

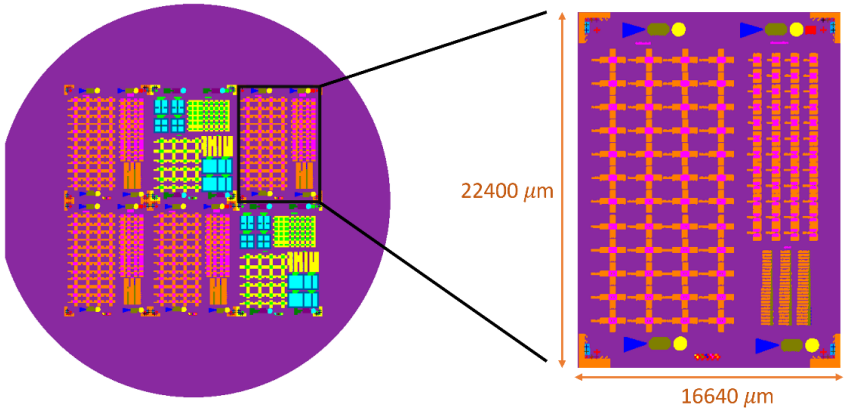


Figure 3-2: Cell containing transient Harman devices, Seebeck coefficient measurement devices and thermal conductivity measurement devices for a wide range of suspended planar silicon membrane geometries.

Table 3-1: This table describes the breakdown of all 48 samples with their specific width and length. Of these 48, there were 24 n-type samples indicated in orange; the other 24 were p-type indicated in blue.

	Width (μm)					
Length (μm)	10		20		30	
20	NPE	PE	NPE	PE	NPE	PE
60	NPE	PE	NPE	PE	NPE	PE
100	NPE	PE	NPE	PE	NPE	PE
140	NPE	PE	NPE	PE	NPE	PE

The other two identical cells (Figure 3-3) contain, in additional to the three devices mentioned above, a doping level measurement platform for each of the phonon and non-phonon engineered silicon membranes for both Si-type materials (n-type and p-type). The membranes' geometry range in the two cells containing doping level measurement platforms is reduced due to technological reasons (for this analysis, samples are fabricated at lengths of 20μm and 60 μm; each length being individually fabricated three times with widths of 10 μm, 20 μm and 30 μm. This equaled a total number of 6 geometries). The external cell dimensions are 16640 μm x 22400 μm because the maximum sample dimensions should not exceed 2.5cm*2.5cm for characterization under vacuum.

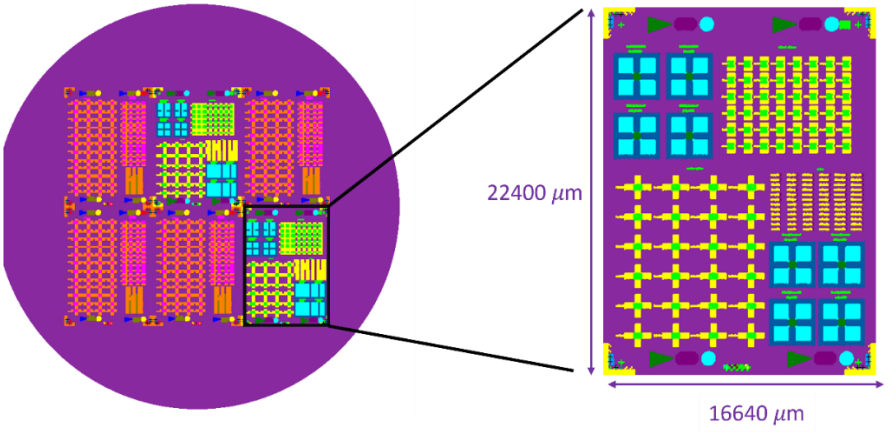


Figure 3-3: Cell containing doping level measurement platform, transient Harman devices, Seebeck coefficient measurement devices and thermal conductivity measurement devices for each of the phonon and non-phonon engineered membranes for both Si-type (n-type and p-type).

In addition to the four devices of interest mentioned above, the cell includes two technologically significant components:

i) <u>First significant component, alignement markers:</u>

The primary use of alignment marks is e-beam alignment with nanometric precision, the e-beam lithography equipment has a 30nm alignment precision. When using four markers

(20µm*20µm) per cell, as in the scheme shown Figure 3-4, common misalignments can be considerably reduced. The cell's external dimensions should be made up of a finite number of 320 μm x 320 μm squares. When doing lithography, this corresponds to the exposure field; the machine carrying out this process can expose the design inside the exposure field without moving the wafer stage. Additionally, the most important component of the device must be positioned in the center of the exposure field to ensure the best degree of precision. To verify that the relative location of the individual layers corresponds to that of the design, the lithography machine identifies the markers and performs the exposure based on their actual placements. Regardless of any human-induced movement while the wafer is being loaded into the machine, the relative positioning between various layers is kept constant. Crosses are added in the bottom of each cell as indicators for each layer (to assess the alignment quality). The internal cross will not be in the center of the area bounded by four triangles if the alignment is not exact (Figure 3-4). If the result is such that the revealed layer's placement is not consistent with the design, the step needs to be repeated to achieve correct placement.

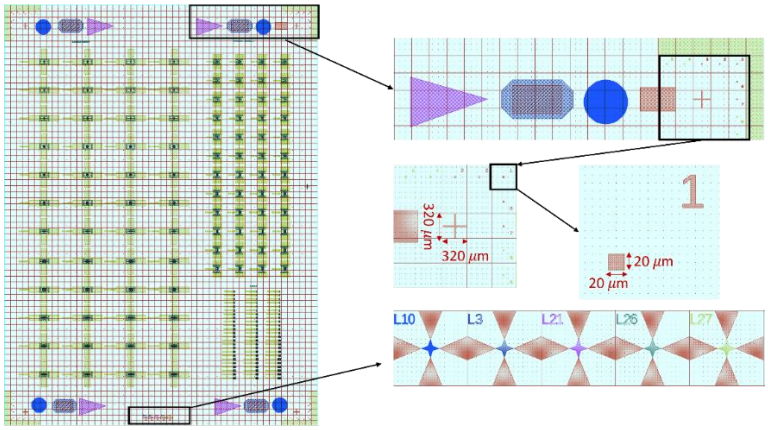


Figure 3-4: Cell containing transient Harman devices, Seebeck coefficient measurement devices and thermal conductivity measurement devices for a wide range of suspended planar silicon membrane geometries with a close-up view on the end point detection windows (top), alignment markers (middle) and alignment verification crosses (bottom).

In summary, alignment markers allow:

a) Precise stacking of the various layers onto each other
b) Alignment verification of the written layer during lithography exposure and development.

ii) <u>Second significant component, end point detection window:</u>

The end point detection windows used while completing the Reactive Ion Etching (RIE) process are the second technologically significant component in the cell. The end point signal, which represents the RIE's progress, can be measured thanks to the end point detection windows. This enables the etching to end at a specified layer using camera endpoint monitor based on real time laser interferometry, which provides high detection of film thickness during the etching process. This camera includes a 670 or 905 or 980 nm laser and it is mounted on the dry etch process chamber with a direct top view of the wafer (Figure 3-5(a)), which generates a small laser spot on the sample surface (Figure 3-5(b)). Interference occurs when monochromatic light hits the sample surface, resulting in different optical path lengths due to film thickness and height variations in the film. This allows the etch rate and thus thickness to be monitored in real time.

a) b)

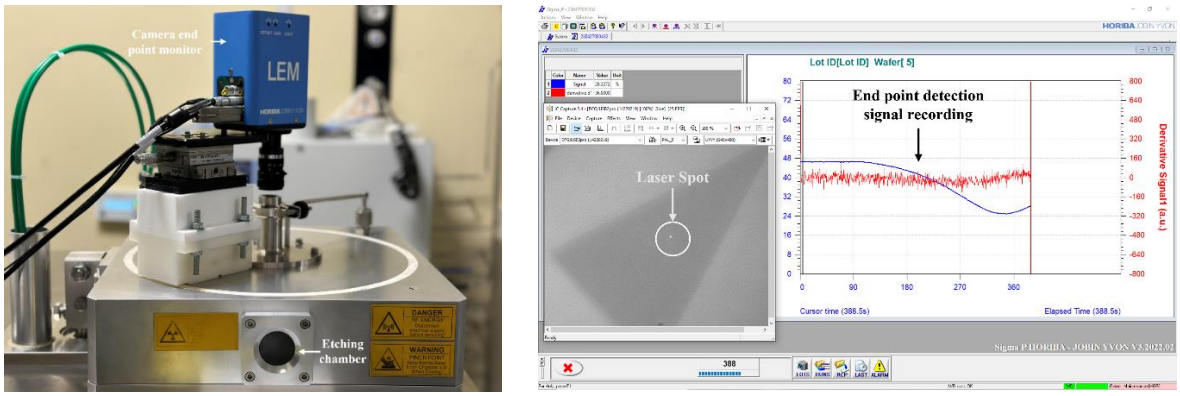


Figure 3-5: a) Camera end point monitor mounted on the dry etching chamber, b) Laser spot and the end point detection signal recording.

Before outlining the realization process, the devices' designs are described below. Each layer in the layout program is assigned a number and a color. The endpoint detection windows and the alignment quality indication are identified by these numbers. The used layers and the accompanying descriptions are included in the table below (Table 3-2). The other devices are likewise created using the same terminology for layering.

Table 3-2: Layer color code and description highlighting fabrication process and associated technological process.

Color	***Layer number***	***Description***	***Step number***	***Processing technology***
	L16	**Alignment markers**	**Preliminary step**	
	L1	**Phonon engineering patterning**	**Step 1**	**RIE**
	L3	**Cavities opening**	**Step 4**	
	L52	**Membranes n-type doping**	**Step 2**	
	L53	**Van Der Pauw n-type doping**	**Step 2**	**Implantation**
	L51	**Membranes p-type doping**	**Step 2**	
	L50	**Van Der Pauw p-type doping**	**Step 2**	
	L27	**Gold evaporation**	**Step 7.2**	
	L26	**Membranes Pt evaporation**	**Step 7.1**	**Evaporation**
	L30	**Van Der Pauw Pt evaporation**	**Step 7.1**	
	L21	**Si_xN_y removal from membranes**	**Step 6**	**RIE**
	L2	**Membranes suspension**	**Step 8**	

3.1.1 *Transient Harman demonstrators*

Several transient Harman demonstrators with different geometries are studied in order to determine the correction factor caused by the parasitic terms in Harmans method as explained in chapter 2.

As shown on Figure 3-6, the metallic contacts occupy most of the space in the device construction. To enable the positioning of the measuring needles necessary for characterization, and to be able to take multiple measurements, the measurement contacts must be enlarged. Additionally, it should be noted that the device consists of two identically suspended membranes and one current injecting point that is positioned in the topology's center. This indicates that the topology is symmetrical, as it was intended, in relation to the x and y axes.

Applying transient Harman method, two contacts are required at the center of the membrane to inject the current (contact 1 and contact 2). Two additional contacts are required to measure the potential difference between the center and the ends of the membrane (contact 3 and contact 4). The latter two contacts can be utilized due to device symmetry; identical membranes are placed in the same measurement conditions and only one membrane's properties may be measured. The measurement contacts are fabricated in gold (Au) due to its favorable characteristics such as high electrical conductivity (σ) and low hardness.

The devices have identical thickness (to the nearest nanometer) and therefore their surface area are solely dependent on L and W as shown in Figure 3-2. Thus, each device in the cell is labelled with the membrane dimensions (L and W), type of doping and the nature of its membrane (phononic engineering or plane).

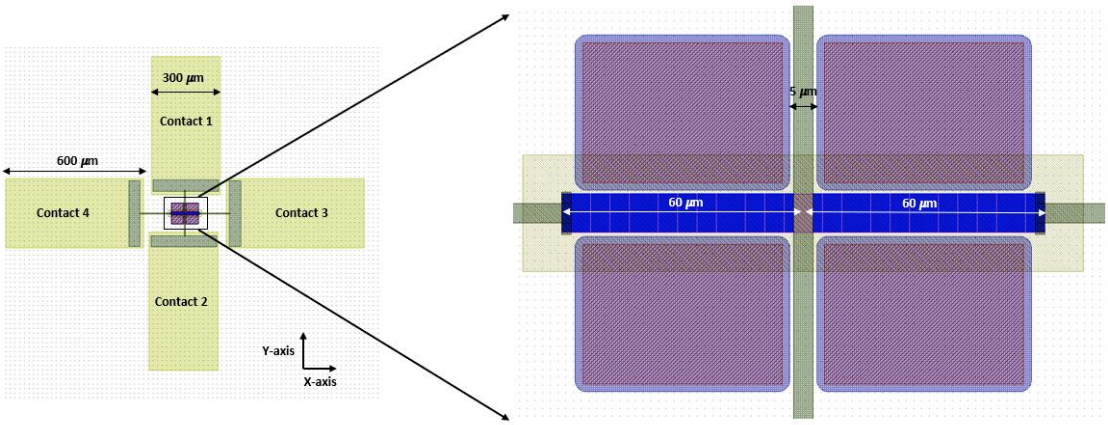


Figure 3-6: Design of transient Harman measurement platform.

3.1.2 *Doping level measurement platforms*

The Four-probes measurement platforms are specifically designed to measure the doping level in silicon membranes. These platforms (Figure 3-7) are used to measure the electrical resistivity of both n and p doped silicon layers, though not simultaneously. The silicon layer is separated from the wafer by the creation of cavities around it. To provide an electrical connection, platinum layers are then deposited at the Si layer's edges. The contacts are required to be as symmetrical and ohmic as feasible. Finally, the wafer includes a silicon phonon engineered layer and a non-phonon engineered layer for each doping nature to enable a preliminary analysis of the effects of phononic engineering on the resistance and resistivity of the Si sheet.

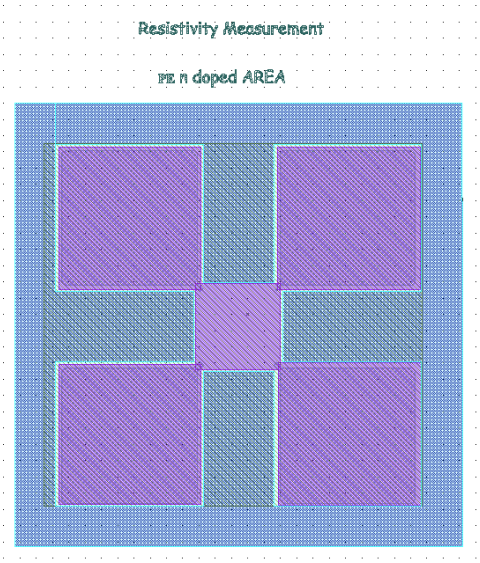


Figure 3-7: Van Der Pauw resistivity measurement device.

3.1.3 Seebeck coefficient measurement devices

Figure 3-8 presents the design of the proposed devices dedicated to measuring Si membrane's Seebeck coefficient. The suspended Si membrane is connected to 2 metallic pads, fabricated in gold (Au), to measure the Seebeck voltage created due to the temperature difference through the membrane. This temperature gradient is created by the heater placed close to the edge of the membrane. To ensure precise measurement of the temperature difference across the membrane, each device is equipped with two heaters. These heaters play a crucial role in creating a controlled temperature gradient. By strategically placing the heaters near the edges of the membrane, they generate a varying temperature profile that spans the suspended structure. This temperature gradient is essential for accurately measuring the Seebeck coefficient. The presence of dual heaters adds an extra level of reliability and accuracy to the temperature measurement process, enabling more robust and meaningful experimental results. The heater is fabricated in platinum (Pt) in a serpentine form. The 4 pads connected to the platinum heater enable concurrent modeling of the hot source by Joule effect and also verifying the absence of the current leakage.

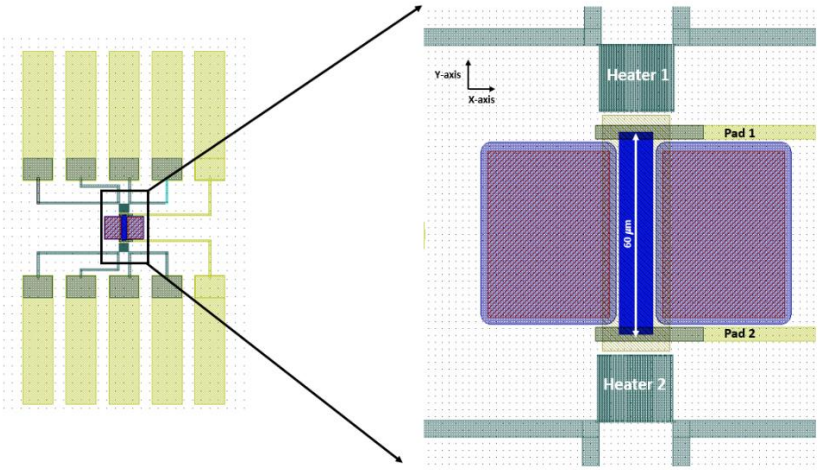


Figure 3-8: Seebeck coefficient measurement device.

3.1.4 Thermal conductivity measurement devices

In this section, the final set of devices, aiming to measure the thermal conductivity of the fabricated suspended membranes through Raman thermometry, are introduced. Two types of silicon membranes are designed for each doping nature (n-type and p-type): phononic engineered membranes and non-phononic engineered membranes. The phononic engineered membranes are further categorized into two subgroups: fully patterned membranes and patterned membranes with a non-patterned circle of 10μm at the center. This differentiation enables the examination of the effects of laser spot injection on both the patterned and non-patterned surfaces of the phononic membranes during Raman measurements. Cavities openings are planned to allow the silicon membrane's suspension (Figure 3-9).

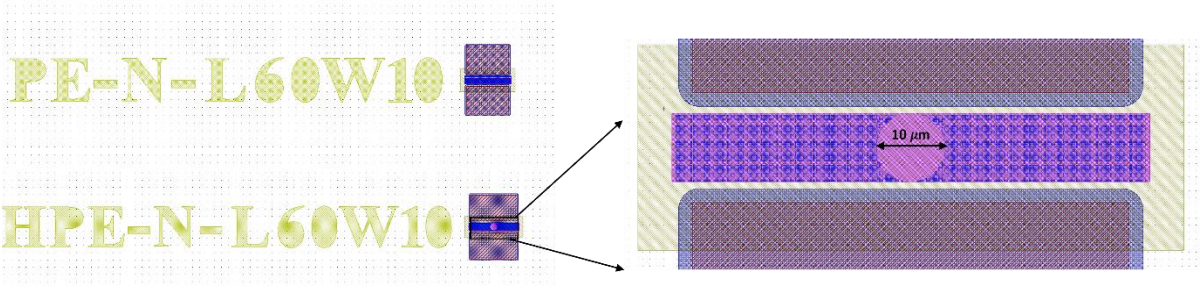


Figure 3-9: Thermal conductivity measurement devices.

3.2 Fabrication

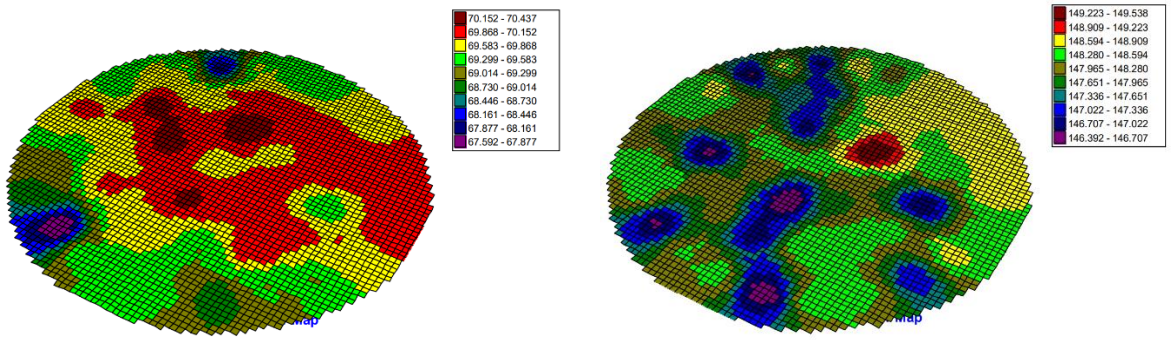
The devices are fabricated from an SOI (Silicon on Insulator) wafer sourced externally from SOITEC. This fabrication process is compatible with different SOI and Buried-Oxide (BOX) thicknesses; in this study a 70nm thick silicon top layer (henceforth, for the sake of brevity, referred to as SOI), a 145nm thick BOX layer and 745µm silicon substrate layer was used. The suggested fabrication method below can be tailored for various SOI and Box thicknesses, including different thin-film materials, by appropriately altering the etching times. Table 3-3 describes the technical specification of the 70/145 SOI wafer.

Table 3-3: The technical specification of the used SOI wafer.

Parameter	***Unit***	***Value***
Wafer diameter	Inch (mm)	3" (76.2)
SOI thickness (top layer)	nm	70 ± 10
Buried oxide thickness (Box)	nm	145 ± 6
Wafer thickness	μm	710-740
Crystal orientation		100
SOI resistivity	Ω.cm	8.5-11.5
Doping type/species		P type/ Boron
Manufacturer		SOITEC

The thickness of the SOI and Box layers are measured using an ellipsometer to assess the wafer's homogenous quality. To attain a high mapping resolution, 49 measurements were taken as shown in the full wafer mapping in Figure 3-10.

a) b)



SOI thickness (nm)		
Average	Maximum	Minimum
69.67	70.43	67.59

Box thickness (nm)		
Average	Maximum	Minimum
148.07	149.54	146.39

Figure 3-10: Full wafer SOI and Box thicknesses 49-point mapping highlighting the thickness dispersion a) SOI thickness mapping; b) Box thickness mapping.

It is demonstrated in Figure 3-10 that the thickness of employed SOI wafer is tightly controlled and has little variation from the nominal value. This is crucial because it allows for the justification of the assumption that all membranes manufactured on this wafer have the same Si thickness.

The realization process consists of:

- Patterning the top layer of a Silicon-On-Insulator (SOI) wafer by means of e-beam lithography and Reactive-Ion-Etching (RIE)
- SOI electrical properties modification by means of ion implantation.
- Materials deposition on SOI top layer by means of Low-Pressure-Chemical-Vapor-Deposition (LPCVD) and e-beam evaporation.
- Thermal insulation of the top layer from the other layers of the SOI by XeF2 and HF vapor etching.

The fabrication procedure (Figure 3-11) is divided into 8 parts with a preliminary step.

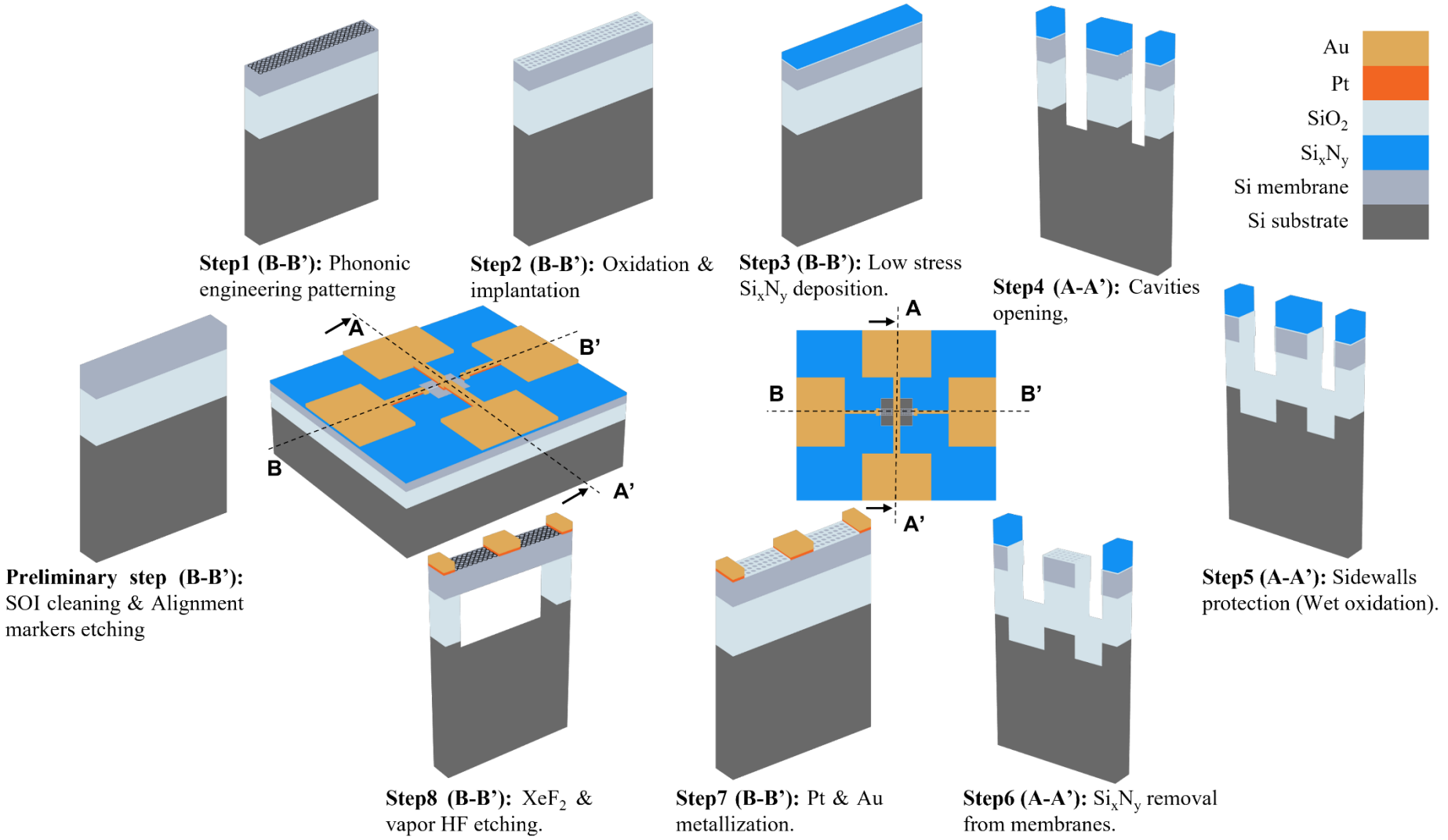


Figure 3-11: Fabrication process steps.

3.2.1 *Preliminary step: wafer cleaning and etching of alignment markers*

The initial stage in the device fabrication process is cleaning the 3-inch wafers using the method introduced in Table 3-4. The wafers are cleaned by immersing them in a SVC14 Remover solution heated to 70°C for at least two hours, followed by an acetone and isopropanol (IPA) rinse as shown in Figure 3-12 After that, the cleaning continues with a 5minute 1000 W μ-wave O_2 plasma treatment, then a 10-minute Piranha (H_2SO_4 and H_2O_2) attack to remove any remaining organic matter. The wafers are then submerged for 30 seconds in a 10% HF solution to remove any remaining silicon oxide layer.

Table 3-4: Wafers cleaning procedure

Product	***Step description***	***Step parameters***	
		Temperature (°C)	***Time (min)***
SVC14 Remover	Wafer protection resist layer stripping	**70**	**120**
1000 W μ-wave O_2 plasma	Organic residuals stripping	**25 → 45**	**5**
30ml 95%H_2SO_4 + 10ml 30%H_2O_2 (Piranha)		**Room**	**10**
10% HF	Native SiO_2 stripping	**Room**	**1**

a) b)

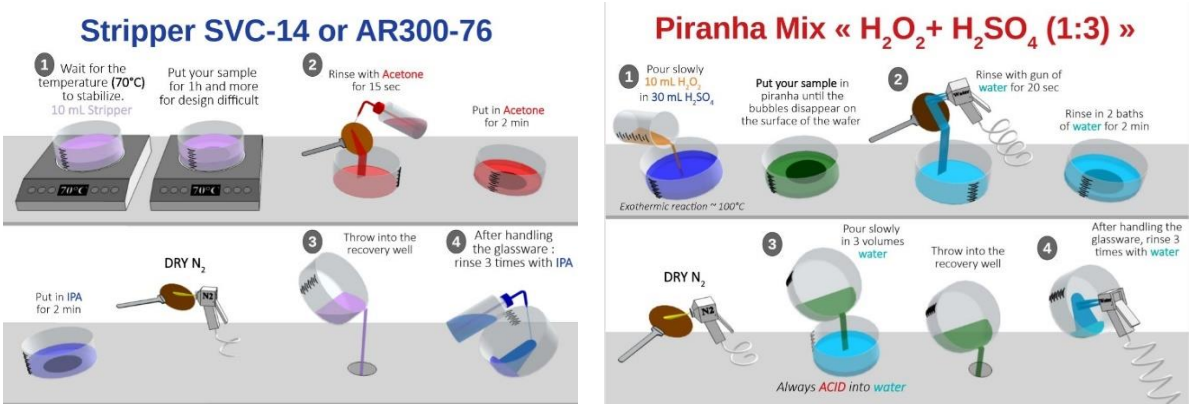


Figure 3-12: Wafers cleaning procedure a) Resist stripping, b) Piranha process[4].

After the wafers have been cleaned, the subsequent step is to pattern the alignment markers enabling the accurate superposition of the various layers. Reactive ion etching and electron beam (e-beam) lithography are the techniques used to pattern the markers. Alignment marks are created using electronic beam lithography and a positive resist (EL13% MAA8.5). To guarantee that the resist will last the lengthy etching operations required to create alignment markings, a 2 μm thick resist layer is used. Table 3-5 provides a description of the resist spin coating technique.

[4] Schematic made by Saliha OUENDI, an engineer in Lithography group at IEMN.

Table 3-5: EL13% MAA 8.5 resist spin-coating procedure

Process	*Step description*	*Step parameters*	
Pre-coating heating on heating plate	Removing organic residuals and drying the wafer	**Temperature**	**150°C**
		Time	**5 min**
Cooling the wafer to room temperature	Aiming to prevent excessive vaporization of resist when placed immediately on a heated wafer	**Time**	**1-2 min**
Spin-coating	EL13%-MAA 8.5 (2μm)	**Resist ID**	**EL13%**
		cover	**Open**
		Speed	**1000 rpm**
		Acceleration	**1000 rpm/s**
		Time	**12 s**
Annealing on heating plate	Heating the wafer to dry the resist. To avoid thermal stress the heating speed is controlled	**T_{start}**	**80°C**
		Time	**1 min**
		T_{end}	**180°C**
		Time	**10min**
Cooling the wafer to the room temperature	Resist and wafer thermal relaxation	**Temperature**	**Room**
		Time	**1-2 min**

The lithography procedure is then carried out as shown in Table 3-6.

Table 3-6: Lithography exposure procedure for alignment markers

Process	*Step parameters*	
Lithography exposure	**Dose**	**450μC/cm^2**
	Current	**25nA**
	Resolution	**25nm**
	Exposed layer	**Layer n° 16**

Table 3-7 summarizes the development of resist after electron beam exposure.

Table 3-7: EL13% MAA 8.5 Development procedure

Process	*Step parameters*	
Resist development	**Product**	**MIBK/IPA (1/2)**
	Time	**60s**
	Agitation	**100-130rpm**
Post development treatment	**Isopropanol (IPA) rinse**	**30s**

	Nitrogen dry blow	**Till the wafer is dry**

Following development, the next step is to etch alignment markers using Reactive Ion Etching (RIE). To enable proper layer alignment by the e-beam machine in subsequent steps, it is vital that deep alignment markers are etched at this stage. The lithography machine uses an electron beam contrast approach to locate the marker, making it simple to localize deep markings. The SOI layer (69 nm), the box layer (145 nm), and a few micrometers of the silicon substrate are etched down to expose the markers. The various steps for patterning alignment markers are detailed in Table 3-8. An endpoint detection signal is measured during the etching of the alignment markers, providing for accurate work over the etching process and the ability to adjust the etching recipe based on the target material or stop the etching when necessary. It is also possible to determine the etching rate by knowing the thickness of each layer of the stack to be etched and the end point detection signal. The end point detection signal, etched profile characterization, and SEM images of the etched alignment markers are shown in Figure 3-13.

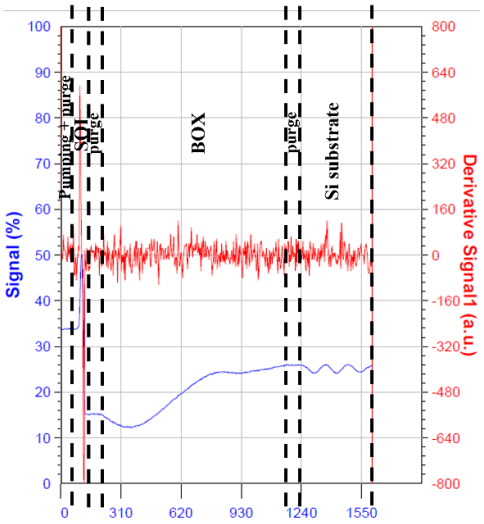
Table 3-8: Alignment markers etching procedure.

Process	***Target material(s)***	***Step parameters***	
Reactive Ion Etching	**SOI top layer (69nm)**	**Power**	**30W**
		SF_6/Ar flow	**10sccm/10sccm**
		Pressure	**10mTorr**
		Time	**50s**
	BOX (145nm)	**Power**	**100W**
		$CF_4/N_2/O_2$ flow	**40sccm/40sccm/5sccm**
		Pressure	**30mTorr**
		Time	**16 min**
	Si substrate	**Power**	**30W**
		SF_6/Ar flow	**10sccm/10sccm**
		Pressure	**10mTorr**
		Time	**6 min**

Resist stripping	**EL13%MAA8.5**	**μ-wave O_2 plasma**	**Power**	**1000W**
			Time	**5min**
			O_2 flow	**525sccm**
		SVC 14	**Temperature**	**70°C**
			Time	**2h**
		Acetone rinsing	**Temperature**	**room**
			time	**2min**
		IPA rinsing	**Temperature**	**room**

		time	**2min**
	Drying	**Nitrogen dry blow**	

a)



b)

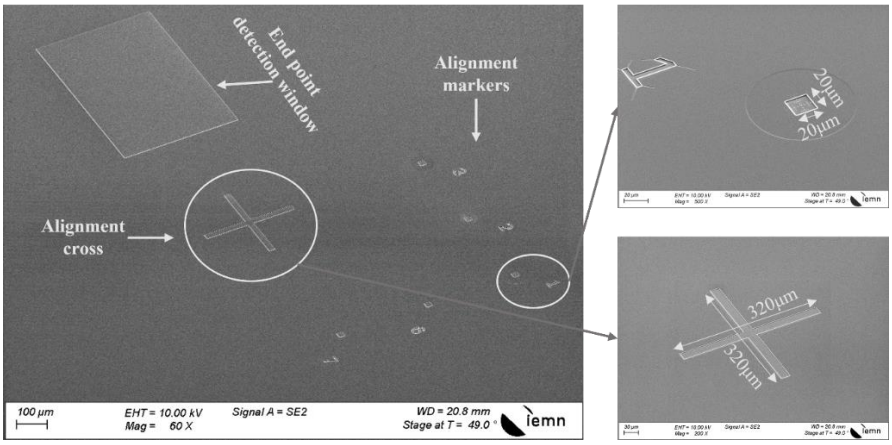


Figure 3-13: a) The end point detection signal (blue) and its derivative (red), b) SEM images of the etched alignment markers, end point detection window and the alignment cross.

3.2.2 Step 1: Phononic engineering patterning

Following the alignment markers patterning discussed above, we will now highlight the phononic crystal patterning on silicon membranes. Reactive ion etching and e-beam lithography are used to carry out this procedure. Two approaches are described below that can be used to pattern the phononic crystal network.

a) Dots-on-the-fly method:

The first approach is the dots-on-the-fly technique [Trasobares et al. 2014; Lacatena et al. 2014][80], it relies on setting the e-beam machine's beam step size (BSS) to the desired phononic crystal network pitch, employing higher current (10nA), and lowering the electron

dose (10–80 µC/cm^2) in order to obtain regularly spaced pixels. Each pixel corresponds to the distance between the dots. Indeed, the trick is to draw a simple geometry (i.e. a large square pattern) Figure 3-14 (left), so as to generate the pattern only once, but to not to provide it the sufficiently high dose and small BSS to perform the desired writing of the full feature. The image obtained appears as a "pixelization" of the desired object (Figure 3-14 right). The technique works because the electron beam size is about 12 nm for the required current, whatever the BSS.

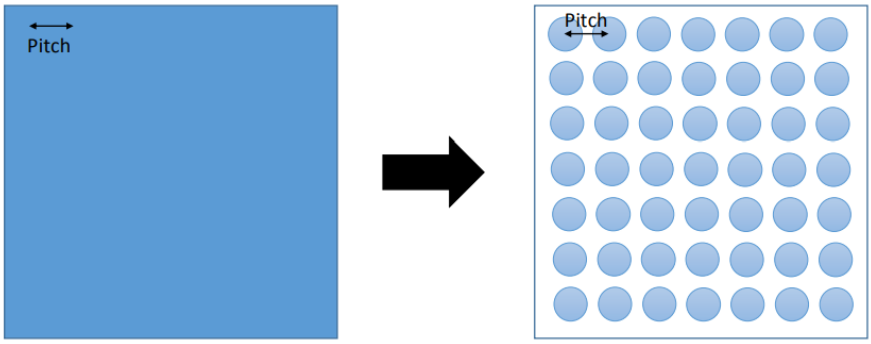


Figure 3-14: Dots on the fly principle[81].

This method results in a significant increase in writing speed and makes it possible to fabricate highly dense and resolute phononic crystal patterns. However, the dots on the fly technique prevents us from fully opening the phononic crystals (Figure 3-15).

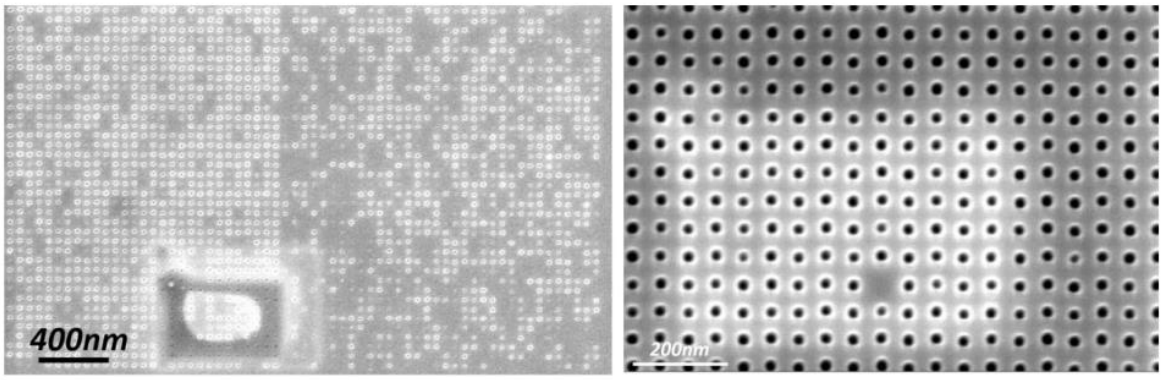


Figure 3-15: Partially opened phononic crystals networks after dots on the fly technique[81].

b) <u>Overdosing method:</u>

The second approach entails creating a series of small squares (2x2 nm^2) using the smallest e-beam machine's BSS and overdosing (hundredths of mC/cm^2) each square in order to open more than the square dimensions (Figure 3-16). The pitch is now determined by the design rather than the BSS of the e-beam machine. This technique enables the design of various phononic crystal network forms and the controlled opening of the patterns (Figure 3-16). But exposing the squares one at a time significantly lengthens the lithography times.

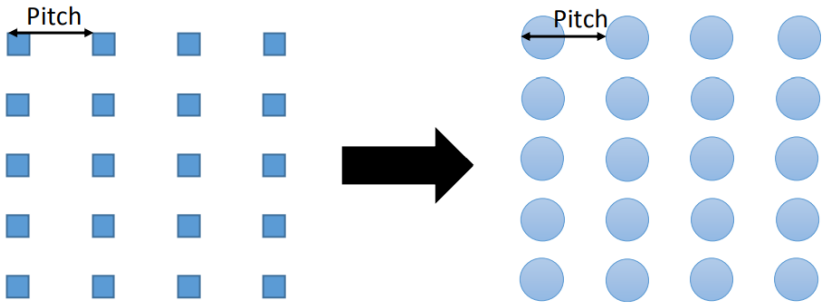


Figure 3-16: Overdosing methodology principle[81].

Despite a longer lithography time, this research proceeded to pattern the pores using the overdosing process, allowing for more patterning precision than the dots-on-the-fly method.

Etching patterns requires several steps (Figure 3-17), the first of which is to spin coat the positive CSAR62 resist on the wafer. Table 3-9 provides a description of the resist spin coating technique.

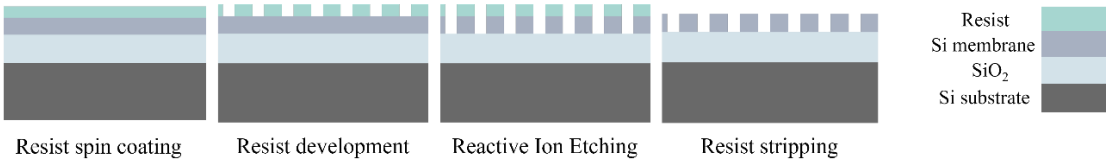


Figure 3-17: Phononic engineering patterning steps.

Table 3-9: CSAR62 Resist spin coating technique.

Process	***Step description***	***Step parameters***	
Pre-coating heating on heating plate	Removing organic residuals and drying the wafer	**Temperature**	**150°C**
		Time	**5 min**
Cooling the wafer to room temperature	Aiming to prevent excessive vaporization of resist when placed immediately on a heated wafer	**Time**	**1-2 min**
Spin-coating	To obtain the 310nm thick resist layer, spin coat the electronic resist on the wafer.	**Resist ID**	**CSAR 62**
		Cover	**Open**
		Speed	**3000 rpm**
		Acceleration	**1000 rpm/s**
		Time	**8 s**
Annealing on heating plate	Heating the wafer to dry the resist	**Temperature**	**150°C**
		Time	**1 min**
Cooling the wafer to the room temperature	Resist and wafer thermal relaxation	**Temperature**	**Room**
		Time	**1-2 min**

The lithography procedure, following on from the previous step, is then carried out as shown in Table 3-10.

Table 3-10: Lithography exposure parameters for patterns.

Process	*Step parameters*	
Lithography exposure	**Dose**	**300mC/cm^2**
	Current	**300pA**
	Resolution	**100 nm**
	Exposed layer	**Layer n° 1**

The development of resist after e-beam exposure is done according to procedure specified in the Table 3-11.

Table 3-11: CSAR62 development parameters.

Process	*Step parameters*	
Resist development	**Product**	**ARP 600-546**
	Time	**90s**
Post development treatment	**Isopropanol (IPA) rinse**	**30s**
	Nitrogen dry blow	**Till the wafer is dry**

After the development of the CSAR62 resist, Cl_2/Ar RIE etching is performed to open the phononic crystal in the SOI layer, as shown in Table 3-12.

Table 3-12: Cl_2/Ar RIE etching and resist stripping parameters.

Process	*Target material(s)*	*Step parameters*		
Etching	**Holes Patterning**	**Power**	**80W**	
		Cl_2/Ar flow	**30sccm/10sccm**	
		Pressure	**10mTorr**	
		Time	**3 min**	
Resist stripping	**CSAR62**	**μ-wave O_2 plasma**	**Power**	**1000W**
			Time	**5min**
			O_2 flow	**525sccm**
		SVC 14	**Temperature**	**70°C**
			Time	**2h**
		Acetone rinsing	**Temperature**	**room**
			time	**2min**
		IPA rinsing	**Temperature**	**room**
			time	**2min**
		Drying	**Nitrogen dry blow**	

The duration of the etching procedure is estimated to be 3 minutes. The SEM pictures (Figure 3-18) of cleaved holes confirm the holes opening until the box has been reached. Moreover, the pictures show an anisotropic profile of the holes.

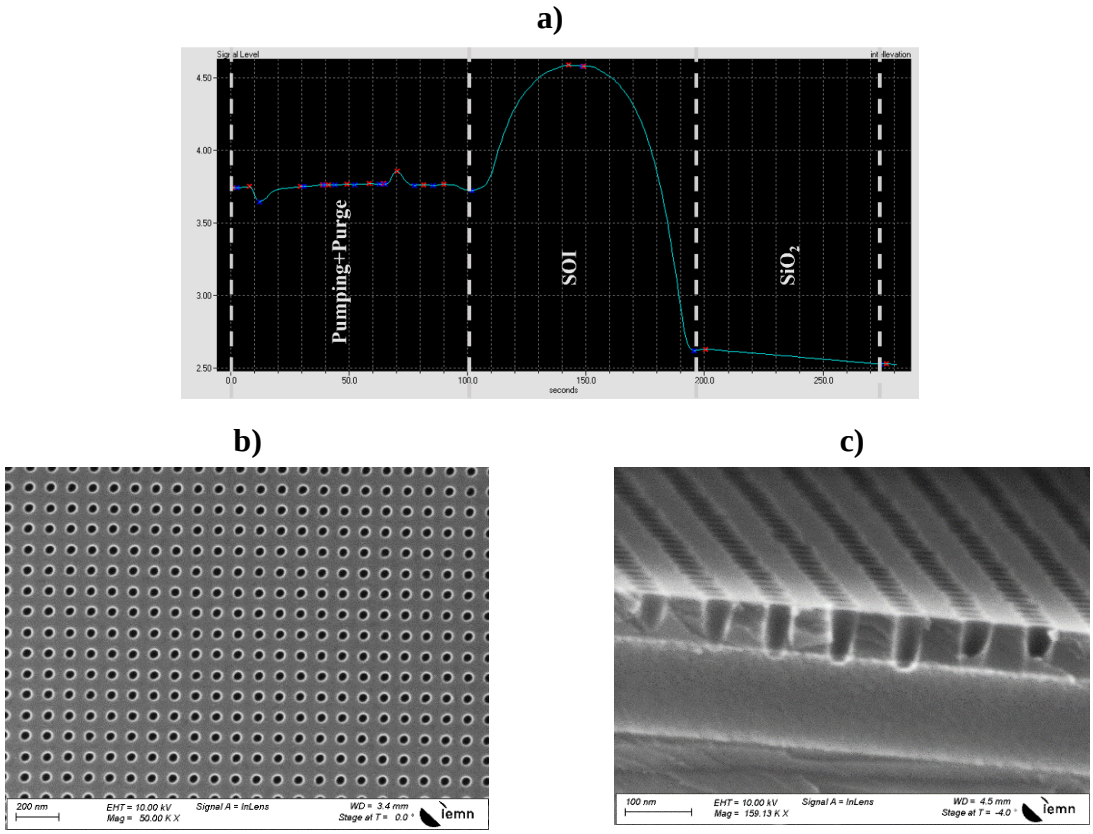


Figure 3-18: a) End point detection signal of Si membrane patterning process. SEM images of a) patterned holes, b) holes cross section view.

3.2.3 Step 2: SOI oxidation & Ion implantation

Diffusion and ion implantation are two methods of adding impurities into semiconductors (Silicon - Si) to impact the majority carrier type and layer resistivity. Diffusion is one of the most common methods for introducing dopants into semiconductors. This approach takes into account the dopant's mobility at the atomic level, and the process is driven by the concentration gradient. Another method of introducing impurities (dopants) into semiconductors is ion implantation. This method uses a low temperature. For the introduction of dopants, this is seen as an alternative to high-temperature diffusion. A beam of extremely intense ions is directed at the desired semiconductor during this operation. The crystal structure is distorted, as a result of ions colliding with the atoms in the lattice. A rapid thermal annealing (RTA, >= 900°C for 5-60 minutes) is the next process that is used to fix the distortion issue after implantation [82] [Narayan et al. 1983].

The main distinction between ion implantation and diffusion is that ion implantation occurs at low temperatures, permitting the use of resist as a mask. Whereas diffusion occurs at high temperatures, which restricts the mask options to silicon oxide or silicon nitride, both of which are significantly more difficult to strip. The junction depth and dopant concentration can both be adjusted during ion implantation, but not during the diffusion process. While ion

implantation has an anisotropic dopant profile, diffusion has an isotropic dopant profile (Table 3-13).

Table 3-13: Ion implantation and Diffusion comparison.

Ion implantation is a low-temperature procedure used to modify a material's chemical and physical properties.	***Diffusion*** is described as the movement of impurities inside a substance.
Isotropic and very directional	Isotropic and mainly includes lateral diffusion
Done at low temperatures → Resist can be used as mask	Done at high temperatures → Hard mask (SiO_2 or SiN) needed
Amount of dopant can be controlled	Amount of dopant cannot be controlled
May damage the surface of the target	Does not damage the surface of the target
More expensive because it requires specific equipment	Comparatively less expensive

For low energy ion implantation, the effect of channeling in the ion implantation method becomes a significant issue. With decreasing energy, the critical angle for axial and planar channeling increases. This results in a higher chance of channeling with a decrease in ion energy. The industry's solution to the channeling issue is to use a specific tilting angle between the surface normal and the ion implantation direction. This random configuration will raise the probability of ions scattering, which in turn will lessen the channeling effect [83]. Another potential solution is to do ion implantation through an amorphous layer placed or grown on the target. This amorphous layer is often made of silicon oxide. The channeling effect decreases as silicon dioxide layer thickness increases (Figure 3-19). Even in highly symmetrical structures like silicon, these two remedies cannot totally eliminate the channeling effect; nevertheless, they can lessen its effects on ion implantation. In order to reduce the channeling effect during implantation, an amorphous silicon oxide layer serves as a screen in the initial step of the ion implantation process.

Ion implantation doping is employed to produce p and n-doped areas to study the thermoelectric properties of both n-type and p-type silicon membranes.

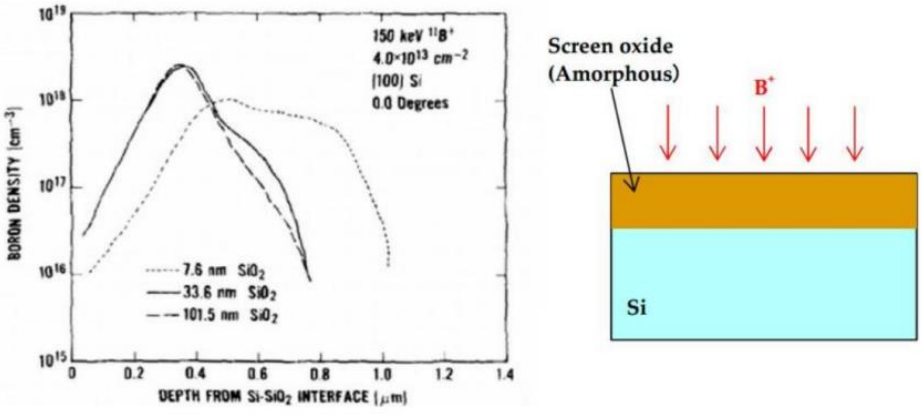


Figure 3-19: Boron dopant profile with various screen oxide thickness [83].

a) <u>SOI oxidation:</u>

The SOI oxidation will not only work as a screening layer for ion implantation, but it will also protect the SOI layer from XeF_2 etching and act as a barrier layer during reactive ion etching. To ensure a higher tightness to the XeF_2 gas, the oxide is grown by low pressure chemical vapor deposition (LPCVD) as opposed to being deposited by plasma enhanced chemical vapor deposition (PECVD). The LPCVD oxidation or thermal oxidation involves injecting an oxidizing chemical onto a wafer and causing it to react at a high temperature (800–1200°C). According to this reaction, the oxidizing agent can be produced from water vapor (wet oxidation, Equation 3- 2) or molecular oxygen (dry oxidation, Equation 3- 1).

$$Si_{(s)} + O_{2(g)} \rightarrow SiO_{2(s)}$$

Equation 3- 1

$$Si_{(s)} + 2H_2O_{(g)} \rightarrow SiO_{2(s)} + 2H_{2(g)}$$

Equation 3- 2

Thermal oxidation is accompanied by silicon substrate consumption (Figure 3-20). Silicon is the source of about 45% of the grown oxide [84]. The oxide thickness is nevertheless constrained by silicon consumption. In fact, the oxide thickness is controlled by silicon availability and device applications in addition to its function (protection layer, screen layer, etc.). In this study, the SOI layer after oxidation should not be thin (less than 55nm) because doing so increases the risk of raising electrical resistance, which would limit the performance of the created thermoelectric material. Therefore, it decreases the *zT* figure of merit. For this project, we proceeded to build an oxide layer 16 nm thick, which reduced the SOI thickness to less than 10 nm. Dry oxidation was used because it provides an acceptable growth uniformity and reproducibility (Figure 3-21).

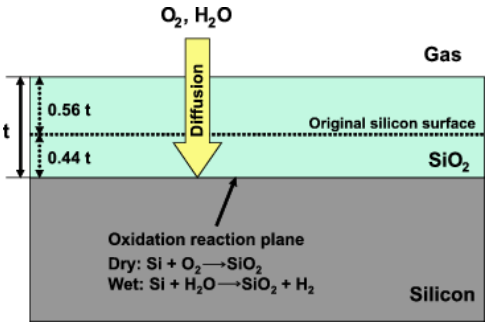


Figure 3-20: The basic process for the oxidation of silicon [84].

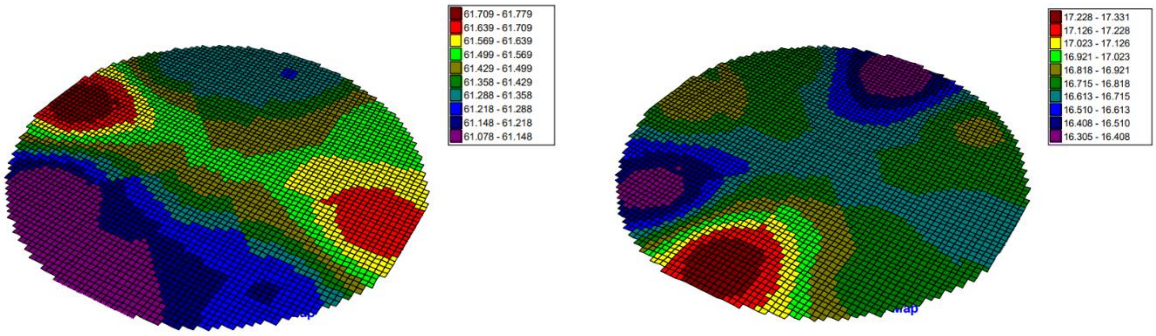
Table 3-14 presents the SiO_2 growth procedure and outlines the five steps required to realize the SOI oxidation step. First, a cleaned wafer is introduced into the oven preheated to 500°C and filled up with nitrogen (N_2). Then, a heating ramp of 10°C/min raises the oven temperature to the final value of 900°C, reducing the thermally induced mechanical stress. When the thermal conditions are stabilized, the oxygen (O_2) and Nitrogen (N_2) are introduced into the tube with a flow of 2slm and 0.2slm respectively for 30 min. The aim of this step is to initiate the thermal oxidation with a uniform layer of dry SiO_2. Following this, the main SiO_2 growing step starts by introducing O_2 with the flow rate of 2slm – the growth duration is 42min. To finalize the process, the temperature has gradual decrease with nitrogen flow of 2slm.

Table 3-14: Dry oxidation parameters.

Process	*Step description*	*Step parameters*		
Wafer cleaning	Organic residuals stripping	**H_2SO_4: H_2O_2 1:1**	**Temperature**	**room**
			Time	**20min**
		Deionized (DI) water rinse	**Temperature**	**room**
			Time	**2min**
		Drying	**Nitrogen dry blow till the wafer is dry**	
	Native SiO_2 stripping	**1% HF**	**Temperature**	**room**
			Time	**1min**
		Deionized (DI) water rinse	**Temperature**	**room**
			Time	**2min**
		Drying	**Nitrogen dry blow till the wafer is dry**	
SOI oxidation	Wafer introduction	**Temperature**	**500°C**	
		N2 Gas flow	**2slm**	
	Heating	**Heating 1 (10°C/min)**	**Temperature**	**500°C→ 675°C**
			Time	**30min**
		Heating 2 (10°C/min)	**Temperature**	**675°C →900°C**
			Time	**60min**
	Pre-oxidation	**Temperature**	**900°C**	
		N_2/O_2 Gas flow	**2/0.2slm**	
		Time	**30min**	
	Oxidation	**Temperature**	**900°C**	
		O_2 Gas flow	**2slm**	
		Time	**42min**	
	Cooling	**Temperature**	**900°C→500°C**	
		N_2 Gas flow	**2slm**	
		Time	**60min**	

Figure 3-21 shows the ellipsometer-measured thicknesses of the developed oxide and residual SOI layers. The above recipe enables the formation of an average oxide that is 16.7 nm thick and has good uniformity (17.3–16.305 nm) for a target thickness of 16 nm.

a) b)



SOI thickness (nm)		
Average	Maximum	Minimum
61.394	61.779	61.078

SiO_2 thickness (nm)		
Average	Maximum	Minimum
16.736	17.331	16.305

Figure 3-21: Full wafer SOI and SiO_2 thicknesses 49-point mapping highlighting the thickness dispersion a) SOI thickness mapping; b) SiO_2 thickness mapping.

b) <u>Ion implantation</u>

i) <u>Ion implantation parameters</u>

After the oxidation, we are interested in the ion implantation. It is first necessary to find the ion implantation parameters such as energy, dose and minimal thickness of the mask. This is done through the use of (SRIM)/(TRIM) software. Stopping and Range of Ions in Matter (SRIM) is a collection of computer programs that calculate ion interactions with matter; at its heart, is the program Transport of Ions in Matter (TRIM). In addition to being widely employed in other areas of radiation material science, SRIM also has applications in the fields of ion implantation research and technology.

Figure 3-22 shows the software interface, which is divided into three sections: the dopant nature and energy definition zone (1), the target's stack definition (2), and the materials forming the stack definition (3) Layer thicknesses are represented by the stacks' width.

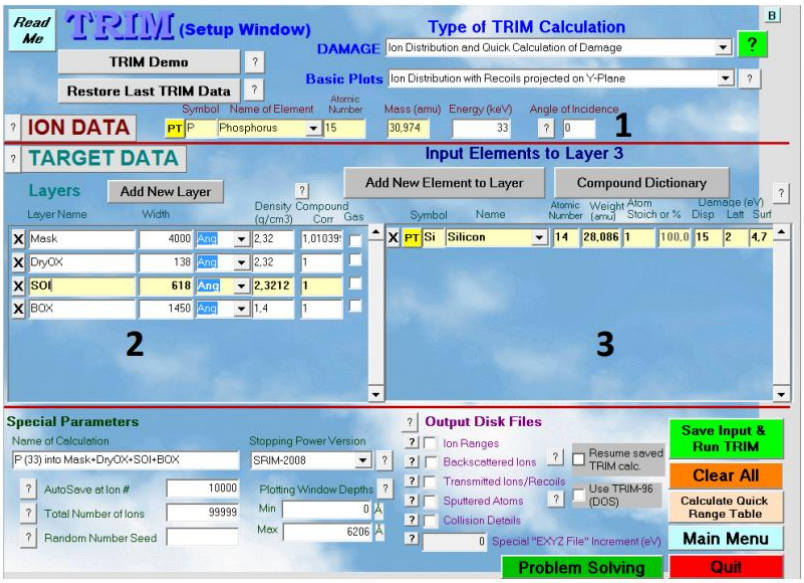


Figure 3-22: Ion implantation "Monte-Carlo" modeling interface.

To allow most ions to penetrate and remain in the SOI layer, we first focused on determining the ideal dopant energy. As a result, modeling is done without using any stack-level masks. As per the modeling, the ideal energies for phosphorous dopants and boron dopants are 12 keV and 33 keV, respectively. The propagation and dispersion of ions into the stack are shown Figure 3-23. The implantation dose corresponding to the desired dopant concentration over the y-axis of the ion distribution is also provided by the same modeling results. The ideal doping level for a thermoelectric material is around 10^{19} atoms.cm^{-3} (Chapter1, section 1.5), and taking into account the distribution of ions, the implantation is carried out for n dopants at 2. 10^{14} atoms.cm^{-2} and for p dopants at 1.7.10^{14} atoms. cm^{-2}.

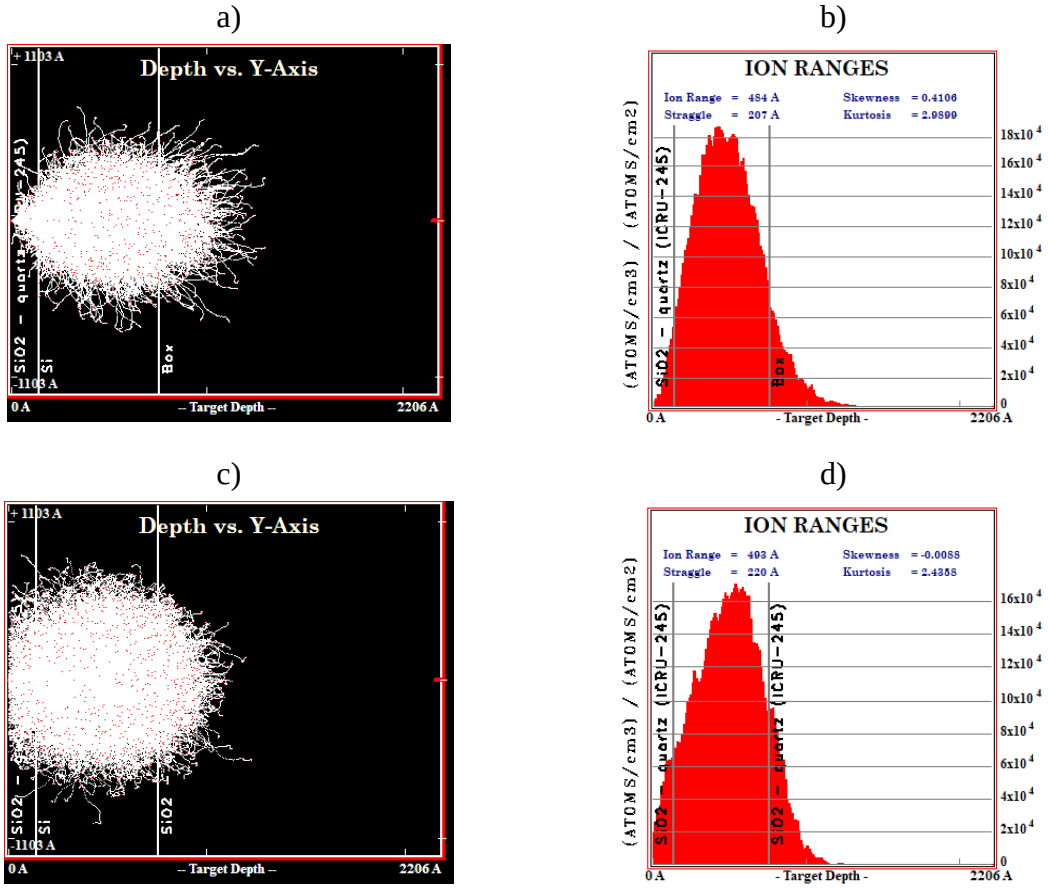


Figure 3-23: Boron and phosphorous implantation simulation of a silicon layer. Ions propagation into the target stack for a Boron dopant (a) and phosphorous dopant (c), Ions distribution for a Boron dopant (b) and phosphorous dopant (d).

Once the ideal energies were determined, we were interested in the thickness of the mask, which would allow us to protect the areas where we did not want to implant. We considered using a 400nm CSAR62 resist because ion implantation allowed us to employ a resist as a mask. Figure 3-24 results demonstrate that the 400nm are sufficient to prevent the implantation of undesirable regions. However, the decision to use 700 nm thick resist has been made.

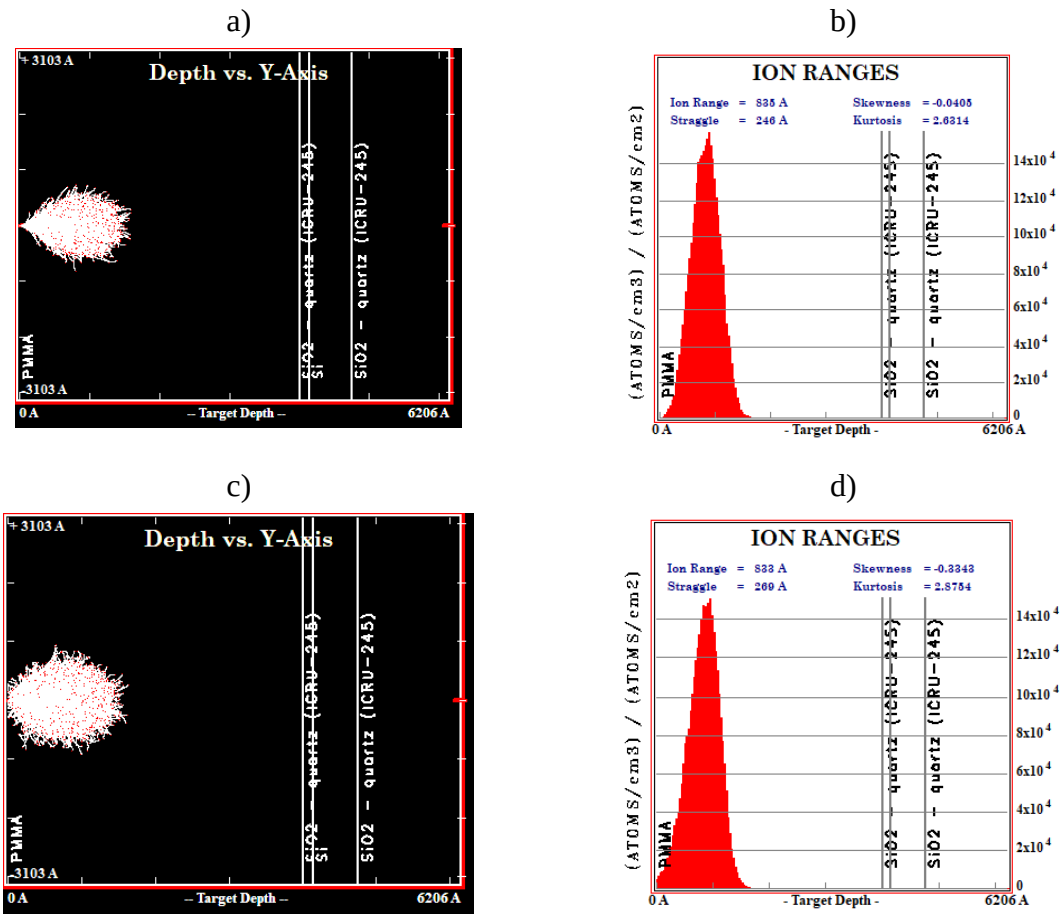


Figure 3-24: 400nm CSAR62 resist mask investigation. Ions propagation into the target stack for a Boron dopant (a) and phosphorous dopant (c), Ions distribution for a Boron dopant (b) and phosphorous dopant (d).

Once the implantation settings have been determined, the p and n doping are carried out in accordance with the process flow shown in Table 3-17. To expose the areas allocated to doping, an e-beam lithography is implemented. Simultaneous boron or phosphorous doping, resist stripping, and rapid thermal annealing (RTA) at 900 °C for 5 min in a nitrogen (N_2) atmosphere are all carried out. For the other type of dopant (phosphorous doping), the procedure is repeated.

Table 3-15 provides a description of the resist spin coating technique.

Table 3-15: CSAR62 Resist spin coating procedure.

Process	***Step description***	***Step parameters***	
Pre-coating heating on heating plate	Removing organic residuals and drying the wafer	**Temperature** **Time**	**150°C** **5 min**
Cooling the wafer to room temperature	Aiming to prevent excessive vaporization of resist when placed immediately on a heated wafer	**Time**	**1-2 min**
Spin-coating		**Resist ID** **cover**	**CSAR 62** **Open**

	To obtain the 700nm thick resist layer, spin coat the electronic resist on the wafer.	**Speed**	**1500 rpm**
		Acceleration	**1000 rpm/s**
		Time	**35 s**
Annealing on heating plate	Heating the wafer to dry the resist	**Temperature**	**150°C**
		Time	**1 min**
Cooling the wafer to the room temperature	Resist and wafer thermal relaxation	**Temperature**	**Room**
		Time	**1-2 min**

The electron beam lithography (exposed layers: Layer n°51 and n°50 for p-type and Layer n°52 and n°53 for n-type) procedure is then carried out as shown in Table 3-16.

Table 3-16: E-beam lithography parameters for ion implantation.

Process	***Step parameters***	
Lithography exposure	**Dose**	**340μC/cm^2**
	Exposed layer	**Layer n°51/n°52**
	Current	**25nA**
	Resolution	**25nm**
	Dose	**410μC/cm^2**
	Exposed layer	**Layer n° 50 / n°53**

The development and ion implantation are performed according to procedure specified respectively in the Table 3-11 and Table 3-17.

Table 3-17: Ion implantation procedure.

Process	***Step description***	***Step parameters***	
Implantation	Boron doping	**Energy**	**12KeV**
		Dose	**2.10^{14} atoms.cm^{-2}**
	Phosphorous doping	**Energy**	**33KeV**
		Dose	**$1.7.10^{14}$ atoms.cm^{-2}**
Resist stripping	SVC 14 remover	**Temperature**	**70°C**
		Time	**2h**
	Acetone rinsing	**Temperature**	**Room**
		time	**2min**
	IPA rinsing	**Temperature**	**Room**
		time	**2min**
	Drying	**Nitrogen dry blow till the wafer is dry**	

Rapid Thermal Annealing (RTA)	Annealing under N_2	**Temperature**	**900°C**
		Time	**5min**

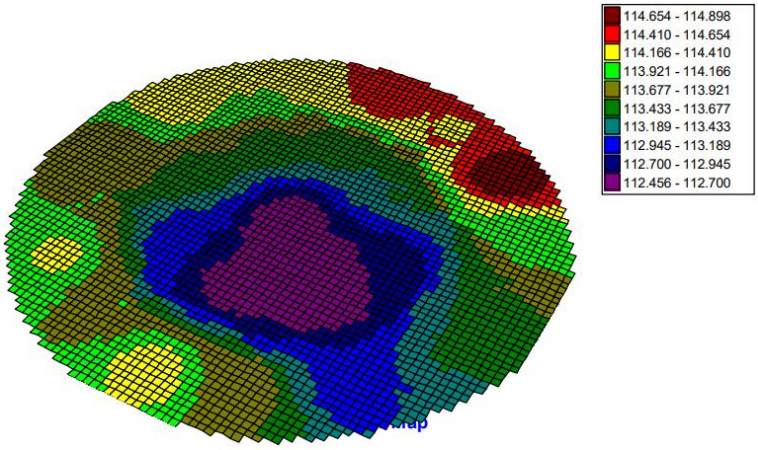
3.2.4 Step 3: SixNy deposition

Following ion implantation, a 113.7nm thick (Figure 3-25) silicon nitride layer is deposited to isolate the metallic components of the final device from the characterized Si membrane, and then to strengthen the mechanical properties of the suspended membranes. Non-stoichiometric silicon nitride Si_xN_y with low stress (29.4 MPa –internal data) is deposited using LPCVD because it ensures the deposition of a low-stress silicon nitride layer, which is required to avoid mechanical bending of the suspended nanostructures.

The silicon-nitride deposition is carried out according to the recipe in Table 3-18. The wafer is first placed in a 350°C preheated oven. Gas is evacuated from the oven while it is heating at a rate of 5°C/min, resulting in a pressure range of 5–20mTorr when the oven reaches its final temperature of 800°C. After that, an oven purge with ammonia (NH_3) is carried out for 10 minutes at a flow rate of 12.8sccm and a pressure of 100mTorr. Prior to executing the deposition, this purge is done to thoroughly fill the oven with NH_3. Following the reaction of NH_3 with SiH_2Cl_2 at flow rates of 12.8 and 77.2sccm, respectively, SixNy is deposited. Deposition takes 40 minutes for 113.6nm of SixNy deposited. Purging with NH_3 is the last step. By keeping the cooling ramp below -5°C/min, mechanical stress caused by heat is reduced.

Table 3-18: Si_xN_y deposition process.

Recipe steps	Temperature (°C)	Pressure (mTorr)	Gas composition	Gas flow (sccm)	Duration (min)
Wafer introduction	350				
Furnace heating	350 → 800	5-20			90
Ammonic purge	800	100	NH_3	12.8	10
Si_xN_y deposition	800	100	SiH_2Cl_2/NH_3	77.2/12.8	40
Ammonic purge	800	100	NH_3	12.8	5
Furnace cooling	800 → 350				90



Si_xN_y thickness (nm)		
Average	Maximum	Minimum
113.690	114.898	112.456

Figure 3-25: Full wafer SixNy thickness mapping.

3.2.5 Step 4: Cavities Opening

Cavities are opened around the silicon membranes to prepare for the silicon membranes suspension in the final step (step8) of the process (Figure 3-26). The process is similar to the alignment markers patterning recipe, except that the etching is done through the deposited silicon nitride, thermal oxide, thin SOI layer, BOX and several nm of the silicon substrate.

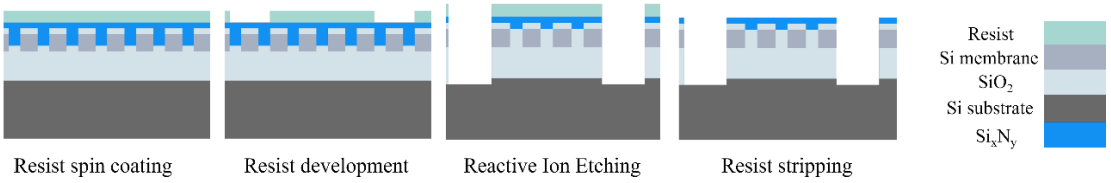


Figure 3-26: Cavities opening process steps.

The resist spin coating of a 2 μm thick resist layer (EL13%MAA8.5), electron beam lithography (exposed layers: Layer n°3) and development are carried out in accordance with the procedures outlined in Table 3-5, Table 3-6 and Table 3-7. Reactive Ion Etching (RIE) step for opening cavities is detailed in Table 3-19.

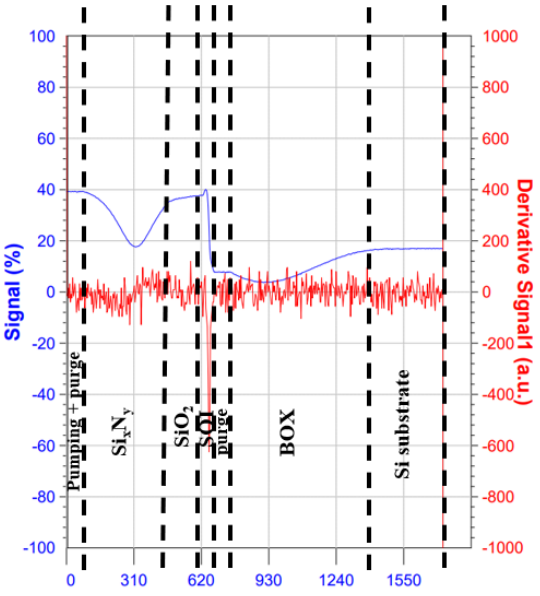
Table 3-19: Reactive ion etching for cavities opening procedure.

Process	***Target material(s)***	***Step parameters***	
Reactive Ion Etching	**Si_XN_y/SiO_2/SOI top layer (113.6nm/16.7nm/61.7nm)**	**Power**	**30W**
		SF_6/Ar flow	**10sccm/10sccm**
		Pressure	**10mTorr**
		Time	**10min**
	BOX (145nm)	**Power**	**100W**

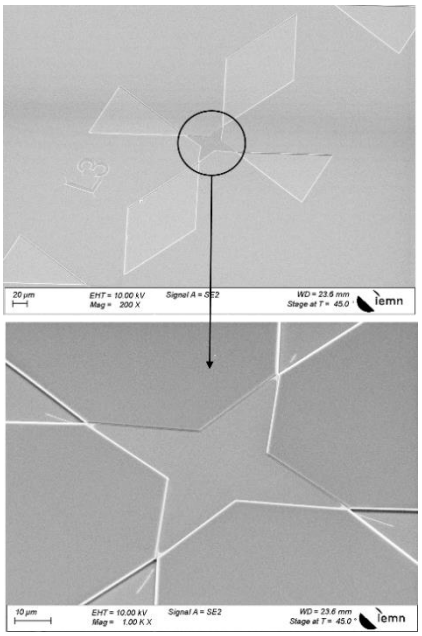
		$CF_4/N_2/O_2$ flow	**40sccm/40sccm/5sccm**
		Pressure	**30mTorr**
		Time	**16 min**
Resist stripping	**EL13%MAA8.5**	**Depicted in Table** 3-8	

Figure 3-27 shows the etching endpoint detection signal of cavities opening (a), SEM images of the alignment marker cross in the middle of the triangles, which confirms that the alignment during the E-beam lithography was correct (Figure 3-27(b)) and SEM images of the cavities created around the membrane in both devices; zT direct measurement device (Figure 3-27 (c)) and Seebeck coefficient measurement device (Figure 3-27 (d)).

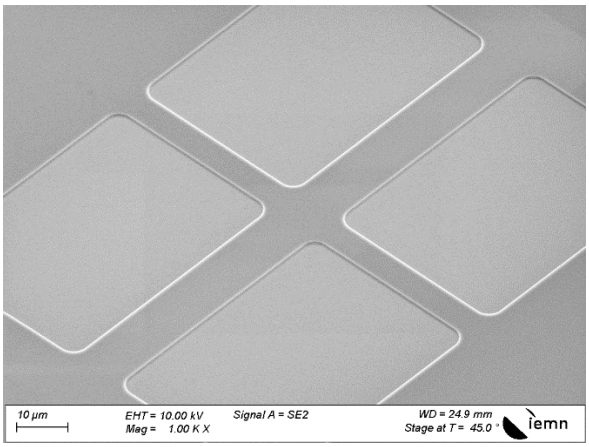
a)



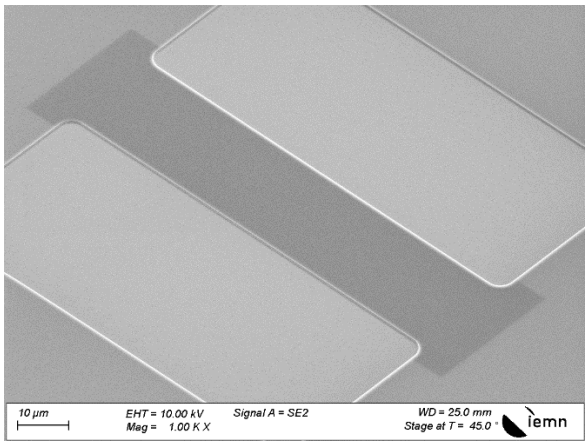
b)



c)



d)



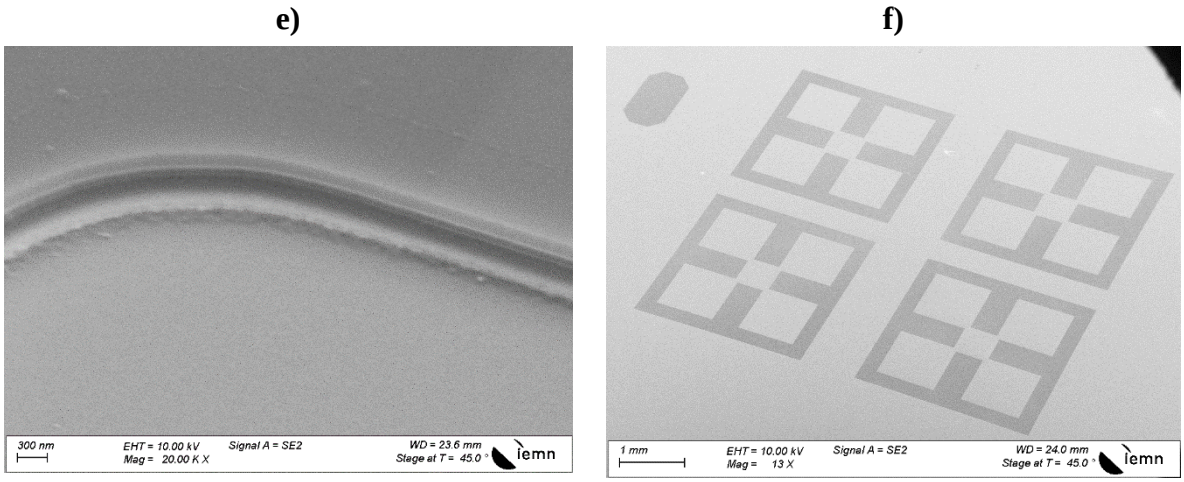


Figure 3-27: a) End point detection signal of cavities opening, SEM images of b) alignment cross marker, c) zT direct measurement device, d) Seebeck coefficient measurement device, e) close-up view on the opened cavities showing the different etched layers and f) resistivity measurement devices.

3.2.6 Step 5: Sidewalls protection

A disadvantage of the cavities opening process (step 4) is that the SOI sidewalls are no longer covered when the cavities are etched and this must be resolved prior to metallization step (step7) in order to prevent the SOI from chemical damage that may occur during the subsequent technical procedures. Indeed, there are two main factors to consider: First, the metal will contaminate the oven used for thermal oxide growth, and second, the 900°C temperature utilized for thermal growth could cause melting and vaporization of the metal. These technological considerations require that the SOI protection be carried out before metallization.

A wet oxidation process is performed to grow SiO_2 at places where the Si is exposed (sidewalls of the SOI and the bottom of the cavities). This wet SiO2 growth process is reported in Table 3-20. The sidewalls protection stage permits both the inner surface of the cavities and the lateral exposed SOI layer to oxidize (Figure 3-28).

Table 3-20: Wet oxidation parameters.

Process	*Step description*	*Step parameters*		
SOI oxidation (16 nm)	Wafer introduction	**Temperature**	**500°C**	
	Heating	**Heating up (10°C/min)**	**Temperature**	**500°C→ 850°C**
			Time	**30min**
		Heating up Torch	**Time**	**20min**
	Stabilization	**O_2 Gas flow**	**1.5slm**	
		Time	**5min**	
	Pyro (ignition of the torch)	**H_2 Gas flow**	**2.5slm**	
		Time	**1min**	
	Oxidation	**Temperature**	**850°C**	

	H_2/O_2 Gas flow	**2.5/1.5slm**
	Time	**8.5min**
Purge	**O_2 Gas flow**	**2.5slm**
	Time	**3min**
	Temperature	**850°C→500°C**
	N_2 Gas flow	**2slm**
Cooling		
	Time	**60min**

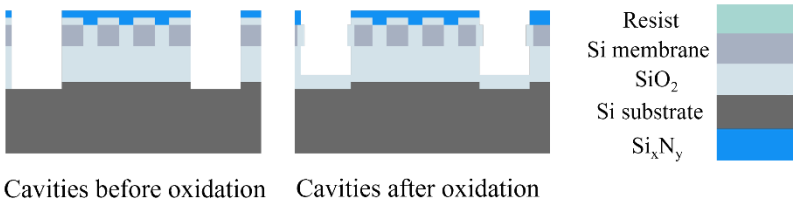


Figure 3-28: Wet oxidation process.

3.2.7 Step 6: SixNy removal

To allow electric current to flow through the membranes and to prevent the presence of a parallel conduction channel in silicon nitride (Si_xN_y), it must be removed from the silicon membranes. As shown in the Figure 3-29, a subsequent stage of e-beam lithography writing and reactive ion etching is used to remove the silicon nitride from the membranes. The etching continues until the endpoint detection signal indicates that the silicon nitride has been completely removed and the dry oxide has been exposed to the etchants. Figure 3-30 (a)shows a representation of the endpoint signal.

Following the procedures detailed in Table 3-5, Table 3-6 and Table 3-7 , the process involves applying a resist layer with a thickness of 2µm (EL13% MAA8.5), utilizing electron beam lithography to expose specific layers (Layer n°21), and undergoing development. Additionally, to remove Si_xN_y from membranes, Reactive Ion Etching (RIE) is employed following the instructions specified in Table 3-21.

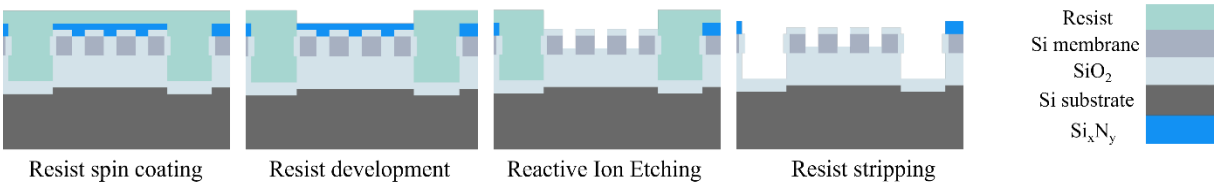


Figure 3-29: SixNy removal process.

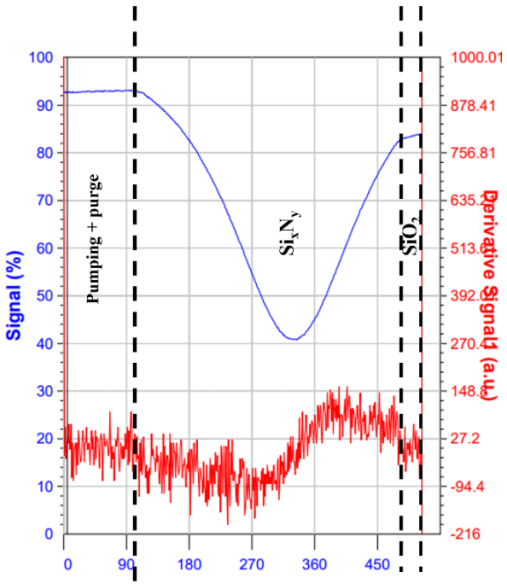
Table 3-21: Reactive Ion Etching (RIE) procedure for SixNy removal.

Process	***Target material(s)***	***Step parameters***	
Reactive Ion Etching	**Si_XN_y (113nm)**	**Power**	**30W**

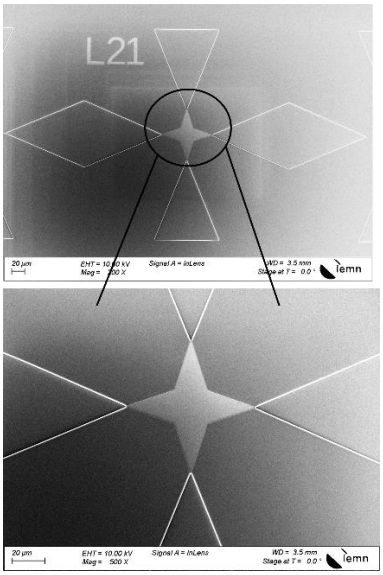
		SF_6/Ar flow	**10sccm/10sccm**
		Pressure	**10mTorr**
		Time	**7min30s**
Resist stripping	**EL13%MAA8.5**	**Depicted in Table** 3-8	

Figure 3-30 showcases a collection of images taken after the removal of Si_xN_y from the membranes. These images include: (a) a signal indicating the endpoint of Si_xN_y removal from membranes and Van Der Pauw structures, (b) SEM images of the alignment marker cross positioned at the center of the triangles, confirming the accuracy of E-beam lithography alignment, (c) SEM images of the zT direct measurement device, (f) SEM images of the Seebeck coefficient measurement device, and a detailed view of the membrane (d) and the pores (e) on the membranes after Si_xN_y removal.

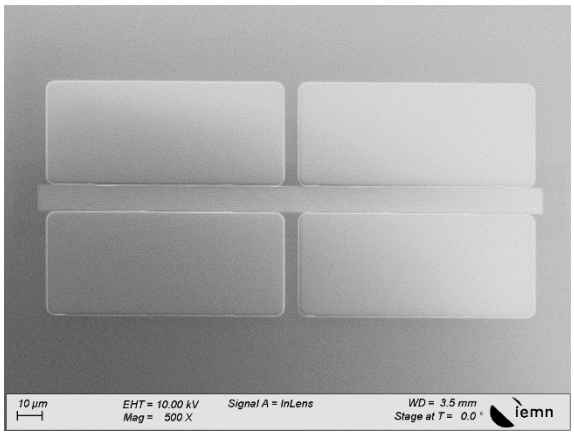
a)



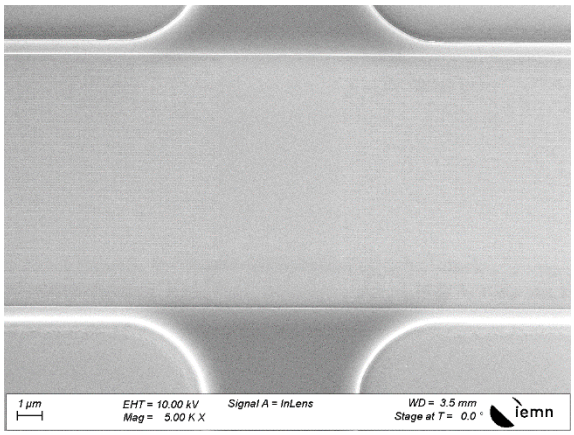
b)



c)



d)



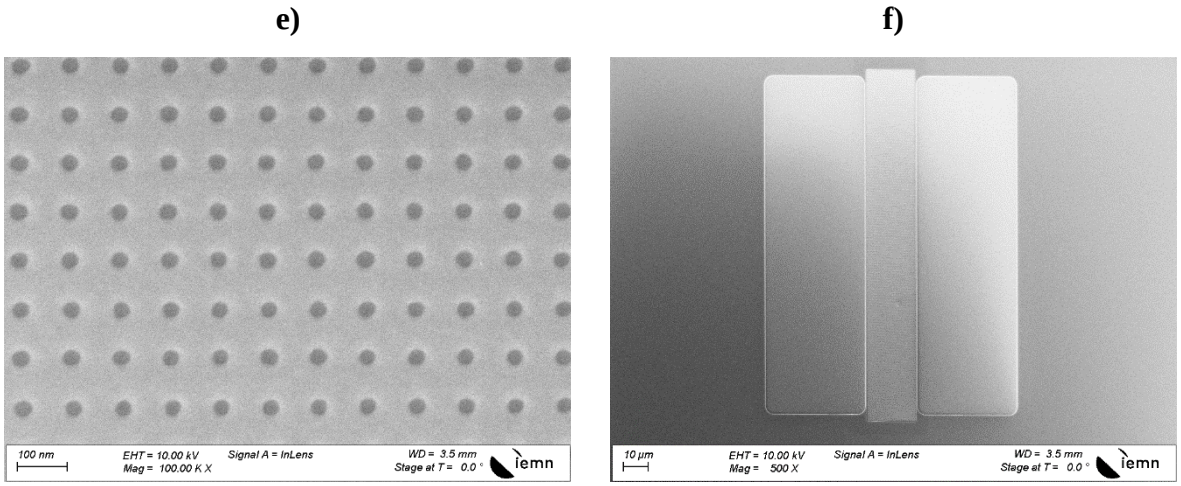


Figure 3-30: a) End point detection signal of SixNy removal step from membrane, SEM images of b) alignment cross marker of layer 21, c) SixNy removal from Si membranes in direct zT measurement device, d) close-up view of patterned Si membrane, e) patterns in Si membrane and f) SixNy removal from Si membranes in Seebeck coefficient measurements device.

3.2.8 Step 7: Metallization

After growing the protective oxide on the sidewalls of the SOI, our next focus is on metallizing the devices. This stage involves depositing metals to ensure the electrical connectivity of the membranes and metals required for characterizing the devices. The deposition process is carried out using e-beam lithography and e-beam evaporation techniques. Prior to the evaporation of metals, a brief Ar plasma etching step is conducted at low power (250 eV) and for a duration of two minutes to eliminate any potential contaminants present on the samples.

3.2.8.1 Platinum metallization

The goal of depositing platinum is to produce platinum heaters that imitate the hot source found in Seebeck coefficient measurement devices using the Joule effect (Figure 3-8). Furthermore, platinum is employed to establish "ohmic" contacts on the silicon membranes (Figure 3-6, Figure 3-8,Figure 3-7), which are crucial for facilitating the characterization of the devices.

Prior to metal evaporation, it is necessary to eliminate the silicon oxide layer grown on the silicon membranes in order to establish proper contact. This is accomplished by subjecting the sample to a 20-second treatment with buffered oxide etchant (BOE) just before loading it into the evaporation chamber. The use of BOE is preferred over HF to prevent the embrittlement or damage of the resist material. To remove the metal from areas other than the designated ohmic contacts, the resist material beneath the metal is stripped away first, followed by the removal of the metal above it. Alternatively, a reactive-ion-etching process can be employed instead of the BOE treatment. The advantage of using BOE lies in its faster operation compared to reactive-ion-etching, while also ensuring the complete removal of silicon oxide from the membrane without etching the SOI layer.

The process of e-beam lithography entails utilizing a 700nm thick CSAR62 resist, followed by the evaporation of a 20nm layer of platinum and a subsequent rapid thermal annealing (RTA) step after removing the resist. The specific steps involved in this process are outlined in Table 3-15, Table 3-22, Table 3-11 and Table 3-23 .

Table 3-22: E-beam lithography parameters for Pt evaporation

Process	*Step parameters*	
Lithography exposure	**Dose**	**340μC/cm^2**
	Exposed layer	**Layer n°26**
	Current	**25nA**
	Resolution	**25nm**
	Dose	**410μC/cm^2**
	Exposed layer	**Layer n° 30**

Platinum silicide (PtSi) is commonly used in electronics for its low-resistance contacts. The formation of PtSi involves annealing a Pt layer on a silicon substrate at 400°C in the presence of N_2H_2 gas. Two sequential reactions occur during the annealing process: platinum diffusion into silicon to form Pt_2Si, followed by silicon diffusion into Pt_2Si to form PtSi. According to Larrieu *et al.* [85], Figure 3-31 (a) demonstrates that to achieve complete silicidation of platinum, the annealing process must be carried out at a minimum temperature of 338°C. Additionally, Breil's research [86], depicted in Figure 3-31 (b), indicates that an annealing temperature of around 450°C and a duration of two minutes using rapid thermal annealing (RTA) under N_2H_2 result in lower and more consistent PtSi sheet resistance. Based on these findings, the platinum silicidation in this study is performed at 450°C for 2 minutes under N_2H_2.

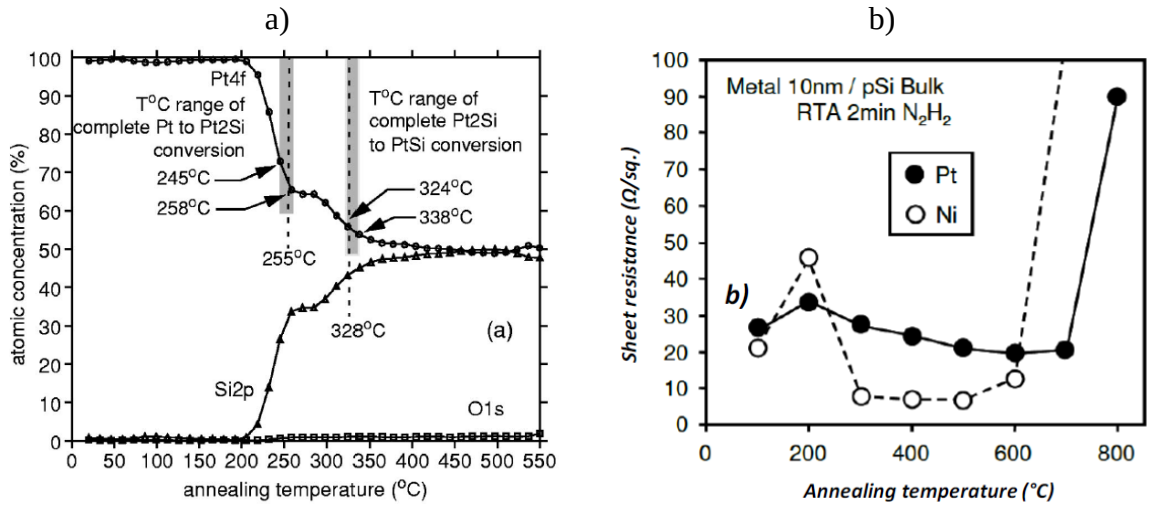


Figure 3-31: a) Platinum silicide formation mechanism and kinetic [85] and b) PtSi sheet resistance with respect to the annealing temperature[86].

Similar to thermal oxidation, the silicidation process involves silicon consumption (Figure 3-32). At the end of the process, the PtSi layer is nearly twice as thick as the initially deposited Pt layer, with approximately two-thirds of this additional thickness originating from silicon consumption [85]. To ensure mechanical strength and prevent complete depletion of the silicon layer after silicidation, a deliberate decision has been made to deposit only 20nm of Pt on top of the 60nm Si layer.

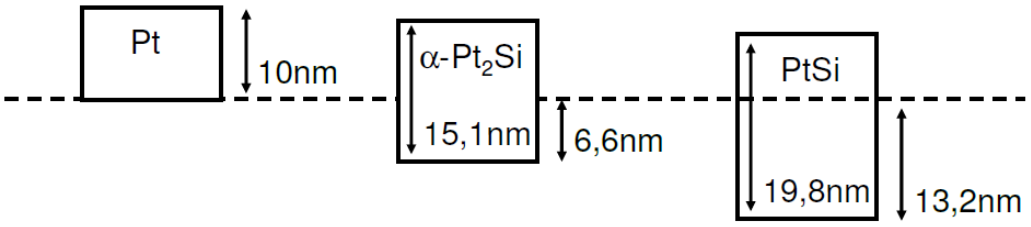


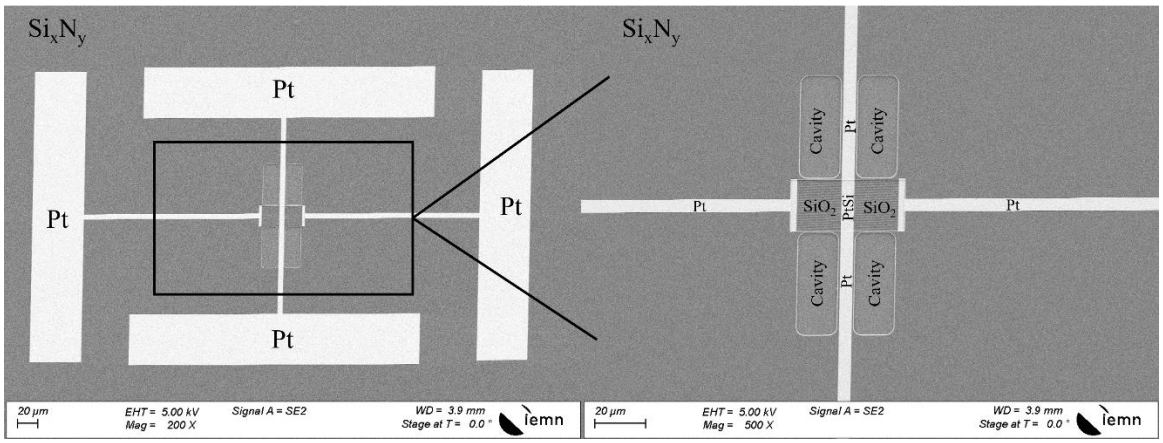
Figure 3-32: Thickness of consumed silicon and thickness of formed silicide for the different phases of the Pt-Si system[86].

Table 3-23: Pt evaporation parameters.

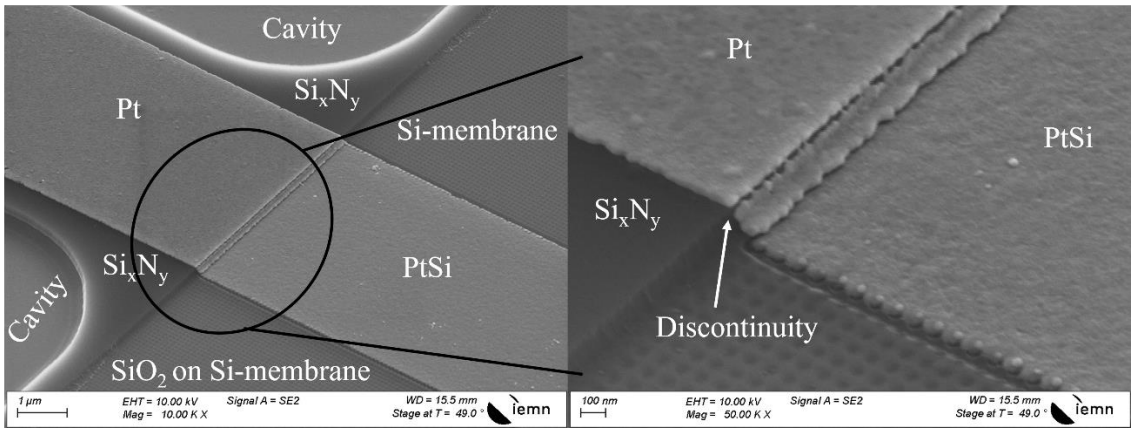
Process	***Target material(s)***	***Step parameters***	
BOE (7:1): Buffered oxide etchant	**Remove the silicon oxide grown on the silicon membranes to allow contact between Pt/Si**	**Time**	**20sec**
Ar etching	**Si**	**Power**	**250eV**
		Time	**2min**
Pt evaporation	**Pt/Si**	**Thickness**	**20nm**
		Rotation	**5rpm**
Lift-Off	**CSAR62**	**Depicted in step 1.4 without μ-wave O_2 plasma**	
RTA	**Ohmic contact (PtSi)**	**Temperature**	**450°C**
		N_2H_2 Gas flow	**500sccm**
		Time	**4min**

In Figure 3-33, a set of SEM images is presented, showcasing various devices that were subjected to a Pt evaporation step as part of the fabrication process. These images offer a closer look at the devices' structures and features following the deposition of Pt. Figure 3-33(a) displays a zT figure of merit device. Figure 3-33(b), presents a magnified view of the Pt arm within the zT figure of merit measurement device, demonstrating the lack of continuity or connection between the membrane and the contact. Figure 3-33(c) focuses on a Seebeck coefficient measurement device. Additionally, Figure 3-33(d) provides a detailed examination of the Seebeck coefficient measurement device after the Pt evaporation step. Finally, Figure 3-33(e) captures a Van Der Pauw measurement device. These SEM images serve as visual evidence confirming the successful implementation and quality of the Pt evaporation step in the fabrication process.

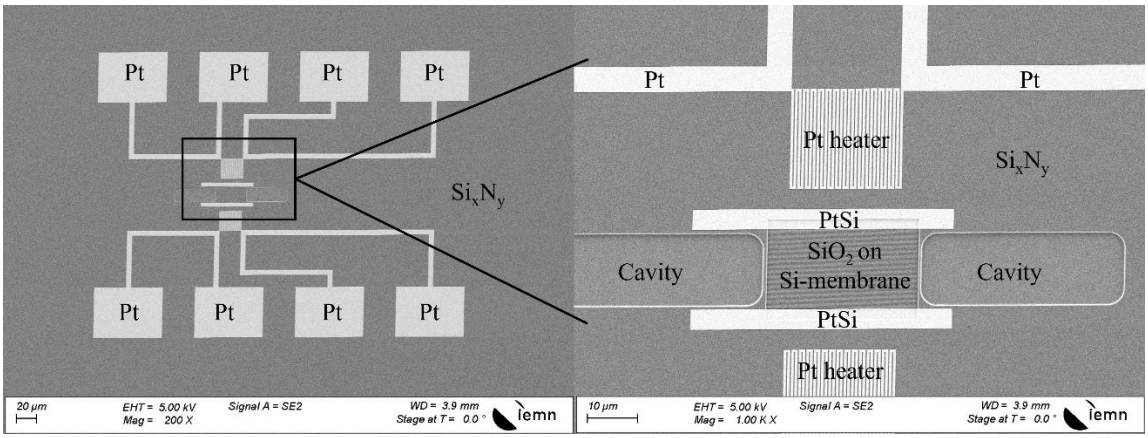
a)


Si$_x$N$_y$
Pt
Pt
Pt
Pt
Si$_x$N$_y$
Cavity
Pt
Cavity
Pt
SiO$_2$
PtSi
SiO$_2$
Pt
Cavity
Pt
Cavity
20 µm
EHT = 5.00 kV
Mag = 200 X
Signal A = SE2
WD = 3.9 mm
Stage at T = 0.0 °
20 µm
EHT = 5.00 kV
Mag = 500 X
Signal A = SE2
WD = 3.9 mm
Stage at T = 0.0 °

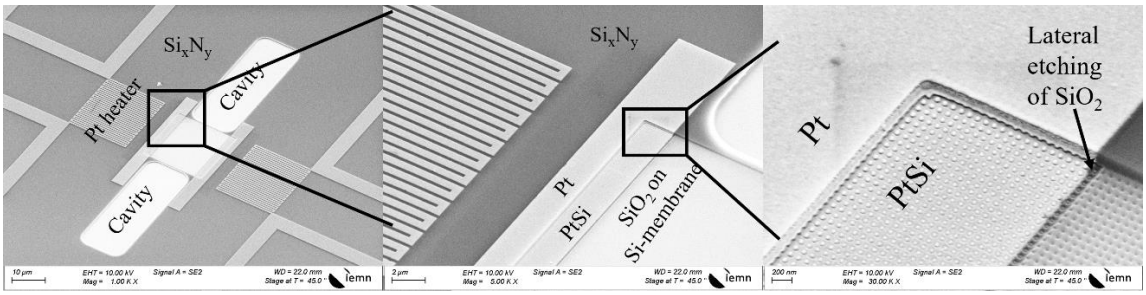
b)


Cavity
Si$_x$N$_y$
Pt
Si-membrane
Si$_x$N$_y$
PtSi
Cavity
SiO$_2$ on Si-membrane
Pt
PtSi
Si$_x$N$_y$
Discontinuity
1 µm
EHT = 10.00 kV
Mag = 10.00 K X
Signal A = SE2
WD = 15.5 mm
Stage at T = 49.0 °
100 nm
EHT = 10.00 kV
Mag = 50.00 K X
Signal A = SE2
WD = 15.5 mm
Stage at T = 49.0 °

c)


Pt
Pt
Pt
Pt
Si$_x$N$_y$
Pt
Pt
Pt
Pt
Pt
Pt
Pt heater
Si$_x$N$_y$
PtSi
Cavity
SiO$_2$ on
Si-membrane
Cavity
PtSi
Pt heater
20 µm
EHT = 5.00 kV
Mag = 200 X
Signal A = SE2
WD = 3.9 mm
Stage at T = 0.0 °
10 µm
EHT = 5.00 kV
Mag = 1.00 K X
Signal A = SE2
WD = 3.9 mm
Stage at T = 0.0 °

d)



e)

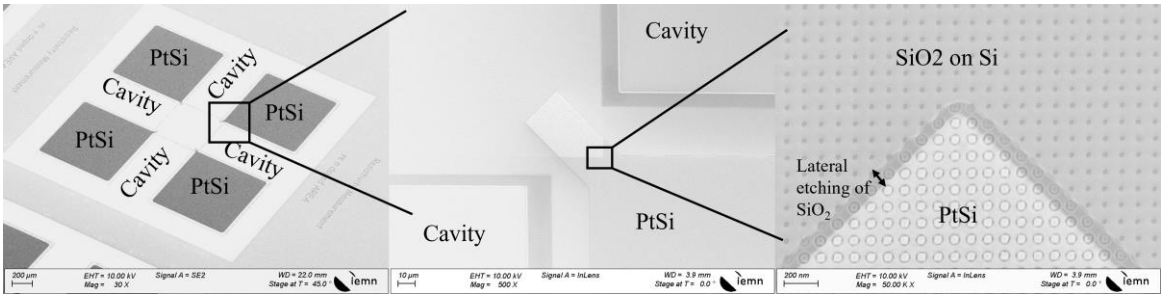


Figure 3-33: SEM images of a) zT figure of merit device, b) close-up view of Pt arm in zT figure of merit measurement device, c) Seebeck coefficient measurements device, d) close-up view of Seebeck coefficient measurement device and e) Van Der Pauw measurement device.

3.2.8.2 Gold metallization

After completing the Pt metallization process, the subsequent step entails applying Au metallization. This serves two purposes: i) constructing structured pads (Figure 3-6, Figure 3-8) to establish contact with the measurement probes, and ii) creating device labels (Figure 3-34(a)). Pure Au is chosen for these pads because of its softness and ductility. This decision is based on the fact that the soft characteristics of Au assist in minimizing the contact resistance between the measurement probes and pads, thereby reducing interface resistance. We have decided to deposit a layer of 400nm Au in order to ensure continuity between the Si membrane and the measurement pads. This choice was made to address the issue of discontinuity observed in the Pt layer (Figure 3-33(b)), which resulted from the removal of Si_xN_y from the Si membrane, causing a gap to form between the membrane and the pads. Additionally, a layer of Cr is included as an adhesive layer between the Pt and Au layers. This Cr layer helps enhance the adhesion between the two metals, ensuring a more robust and reliable connection.

To address the issue of lateral etching caused by the BOE (Figure 3-33(d),Figure 3-33(e)) in the previous step, and to prevent the Si membrane from being attacked by XeF_2, we decided to use a wider width for the Au layer. By employing Pt/Cr/Au on the Si membrane instead of directly applying Cr/Au on Si, unfavorable interactions between Au and Si are avoided, as they do not form a compatible combination. It is worth noting that in future devices, this step may not be necessary, and the Au width can be equal to the PtSi width. This is possible by utilizing a resist in the XeF_2 machine, which we were initially unaware of, compelling us to explore alternative solutions.

Gold evaporation is performed using the following procedure. Firstly, the positive tone EL13%-MAA8.5/ PMMA3% resist is spin coated on the wafer according to procedure specified in the Table 3-24. Electron beam lithography is subsequently performed according to the details listed in Table 3-25.

Table 3-24: EL13% MAA 8.5/ PMMA 3% resist spin-coating procedure.

Process	*Step description*	*Step parameters*	
Pre-coating heating on heating plate	Removing organic residuals and drying the wafer	**Temperature**	**150°C**
		Time	**5 min**
Cooling the wafer to room temperature	Aiming to prevent excessive vaporization of resist when placed immediately on a heated wafer	**Time**	**1-2 min**
Spin-coating	EL13%-MAA 8.5 (600nm)	**Resist ID**	**EL13%**
		cover	**Close**
		Speed	**2900 rpm**
		Acceleration	**1000 rpm/s**
		Time	**12 s**
		cover	**Open**
		Speed	**500 rpm**
		Acceleration	**1000 rpm/s**
		Time	**6 s**
Annealing on heating plate	Heating the wafer to dry the resist. To avoid thermal stress the heating speed is controlled	**T_{start}**	**80°C**
		Time	**1 min**
		T_{end}	**180°C**
		Time	**10min**
Cooling the wafer to the room temperature	Resist and wafer thermal relaxation	**Temperature**	**Room**
		Time	**1-2 min**
Spin-coating	PMMA 3% (70nm)	**Resist ID**	**PMMA3%**
		cover	**Close**
		Speed	**3400 rpm**
		Acceleration	**1000 rpm/s**
		Time	**12 s**
		cover	**Open**
		Speed	**500 rpm**
		Acceleration	**1000 rpm/s**
		Time	**6 s**
Annealing on heating plate	Heating the wafer to dry the resist. To avoid thermal stress the heating speed is controlled	**T_{start}**	**80°C**
		Time	**1 min**
		T_{end}	**180°C**

		Time	**10min**
Cooling the wafer to the room temperature	Resist and wafer thermal relaxation	**Temperature**	**Room**
		Time	**1-2 min**

The lithography process for layer n°27 follows the parameters provided in Table 3-25. The measurement pads constitute the largest portion of the device design (Figure 3-6) and employing a low exposure current and precise beam step size would lead to excessively long exposure times. To circumvent this issue, the current is increased to expedite the lithography process.

Table 3-25: Lithography exposure parameters for Au evaporation.

Process	***Step parameters***	
Lithography exposure	**Dose**	**600μC/cm^2**
	Current	**50nA**
	Resolution	**25nm**
	Exposed layer	**Layer n° 27**

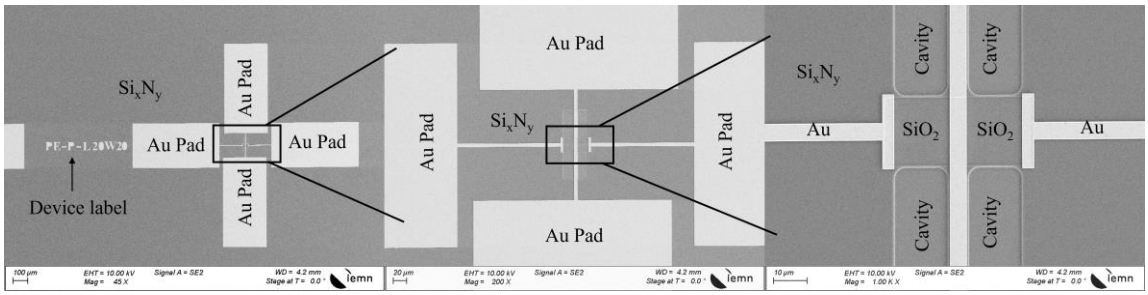
After the lithography the development is performed according to the specification detailed in Table 3-7. Consequently, the Au is evaporated on the wafer using the sequence specified in Table 3-26.

Table 3-26: Pt/Cr/Au evaporation parameters.

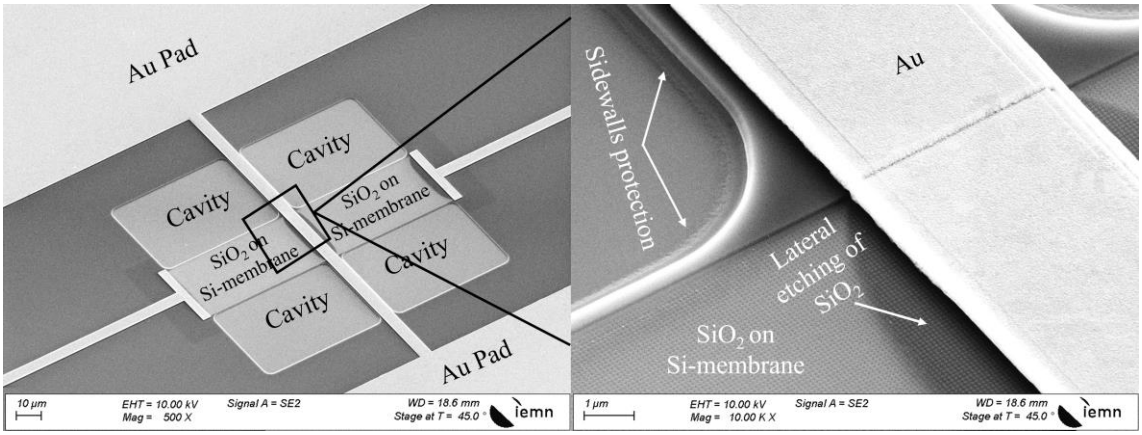
Process	***Target material(s)***	***Step parameters***	
Ar etching	**Si**	**Power**	**250eV**
		Time	**2min**
Pt/Cr/Au evaporation	**Pt/Cr/Au**	**Thickness**	**15nm/40nm/400nm**
		Tilt /rotation	**15°/5rpm**
Lift-Off	**EL13%/PMMA3%**	**Depicted in Table 3-8 without μ-wave O_2 plasma**	

Following the completion of the lift-off process, the Au contact pads are successfully transferred onto the wafer and are ready for utilization. SEM photos in Figure 3-34 clearly demonstrate that the measurement pads are precisely defined and exhibit no signs of peel-off or detachment. Furthermore, it is noteworthy to mention that the issue of discontinuity, which was previously observed, has been resolved. We have thus achieved a seamless continuity between the membrane and the measurement pads, as depicted in the SEM photos in Figure 3-34 (d).

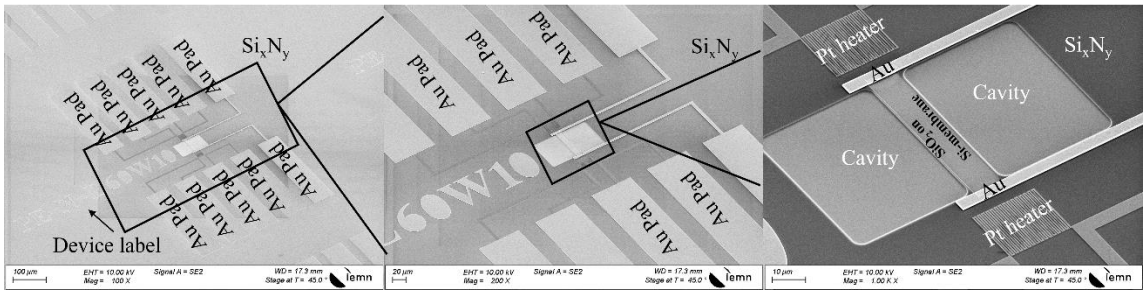
a)



b)



c)



d)

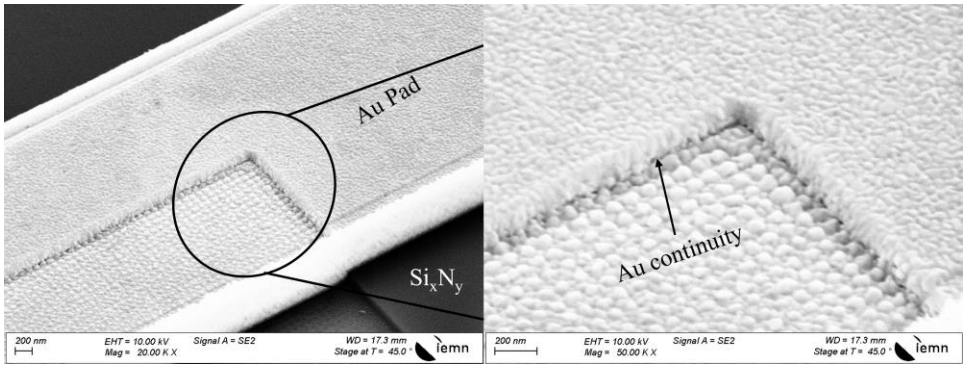


Figure 3-34: SEM images after gold evaporation for a) zT figure of merit direct measurement device, b) Close up view of zT direct measurement device, c) Seebeck measurement device and d) close up view of Au/PtSi contact.

3.2.9 *Step8: XeF2 & Vapor HF etching*

To ensure thermal insulation of the silicon membranes from the rest of the SOI substrate, the final steps of device fabrication involve their suspension. However, before proceeding with the suspension, it is crucial to cut the wafer, which contains six cells, into separate individual units. This wafer cutting procedure should be carried out prior to the membrane suspension to prevent any potential damage to the suspended membranes. Prior to the cutting process, a protective layer of 2µm resist (EL13%MAA8.5) is applied through spin coating to protect the sample. This step, as illustrated in Table 3-5, ensures the protection of the membranes during the cutting procedure. Subsequently, as depicted in Table 3-26, the resist layer is stripped off to restore the original configuration of the sample.

In step5, we implemented sidewall protection by growing a 16nm thick wet SiO_2 layer. This fabrication process, outlined in Table 3-20, involves the growth of silicon dioxide in areas where the silicon is exposed to oxidizing agents. As a result, wet SiO_2 is formed on the sidewalls of the SOI and at the bottom of the cavities. To etch the silicon substrate within the cavities, it is necessary for the silicon to be exposed while selectively removing the SiO_2 only from the cavities without affecting the wet SiO_2 used as sidewall protection for the SOI. To achieve this, a lithography step is performed to define the regions where the wet SiO_2 will be exposed during the etching process. Simultaneously, the exposed layer shields the sidewall protection of the SOI from the etching. Consequently, only the SiO_2 layer located at the bottom of the cavities is exposed to the etching process. To incorporate the exposed layer into the device, a lithography process is employed; the lithography process can only be carried out when the electro-sensitive resist is spin-coated onto the wafer. The specific spin coating procedure is provided in Table 3-5. After spin coating, the lithography exposure takes place following the steps outlined in Table 3-27 and once the lithography is completed, the development of the wafer is performed according to the specifications outlined in Table 3-7.

Table 3-27: Lithography exposure parameters for membranes exposure.

Process	***Step parameters***	
Lithography exposure	**Dose**	**450μC/cm^2**
	Current	**25nA**
	Resolution	**25nm**
	Exposed layer	**Layer n° 2**

The removal of SiO_2 from the cavities is achieved through Reactive Ion Etching (RIE). The etching recipe employed is identical to the one used for etching the alignment markers or the cavities during the Box etching process. This etching procedure utilizes a combination of CF_4, N_2, and O_2 in its chemistry. This RIE process continues until complete etching of the oxide is achieved, with a slight over-etch of the silicon substrate to ensure the removal of all remaining oxide, as depicted in Figure 3-35. The utilization of RIE is preferred over chemical bath methods such as BOE or HF, as it avoids the unintentional etching of the oxide layer grown on the sidewalls of the SOI. The specific details of the etching procedure can be found in Table 3-28.

Following the RIE, the resist is not stripped since it serves as a protective mask for the subsequent XeF_2 vapor etching process.

Table 3-28: RIE parameters for membranes exposure.

Process	*Target material(s)*	*Step parameters*	
Reactive Ion Etching	**SiO_2 (16nm)**	**Power**	**100W**
		$CF_4/N_2/O_2$ flow	**40sccm/40sccm/5sccm**
		Pressure	**30mTorr**
		Time	**7min**

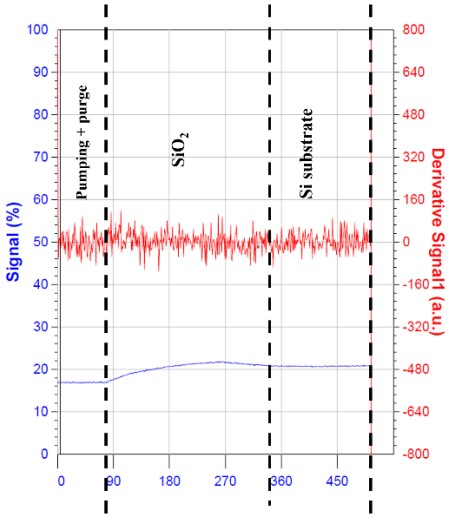


Figure 3-35: Si exposure end point detection signal.

3.2.9.1 Step8.1: XeF2 etching

Step 8.1 should be executed promptly following the removal of SiO_2 from the cavities to minimize the formation of native SiO_2. Once the SiO_2 etching in the cavities is completed, the Si substrate can be under-etched to release the SOI-Box membrane from the substrate. Releasing the SOI-Box membrane necessitates the utilization of an isotropic etching procedure. This step is crucial for detaching the suspended membrane from the Si substrate. The theoretical thickness of the membrane is 60nm+145nm, emphasizing the need for a gentle etching process that does not impose mechanical stress on the suspended membrane. Initially, wet etchant baths like KOH or TMAH were considered, but due to the thinness of the SOI-Box layers (~60nm + 145nm), concerns such as stiction and capillary forces emerged. Therefore, dry etching using the gaseous phase of XeF_2 was preferred. XeF_2 enables isotropic etching of the silicon substrate while exhibiting excellent selectivity to oxide, thus allowing the SiO_2 layer to serve as an etching mask.

The device developed in this thesis was released from the Si substrate using a dry XeF_2 etching technique. The etching process is performed in cycles, as specified in Table 3-29. The etching chamber is filled with the etchant gas at a pressure of 4 Torr, and each etching cycle lasts for 15 seconds. At the end of each cycle, the chamber is pumped out to a pressure of 1Torr to remove the byproducts (Xe and SiF_4) as well as any residual etchant. This process is repeated until the SOI-BOX layers are fully suspended. Generally, achieving full suspension of the SOI-

BOX layers with a width of 10µm necessitates five cycles of etching. However, to suspend SOI-BOX layers of various widths, including 20µm, and 30µm, an additional six cycles of etching are required.

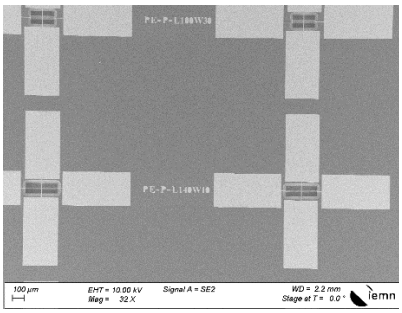
Table 3-29: Si substrate under etching using XeF_2 in gaseous phase.

Process	*Target material(s)*	*Step parameters*	
XeF_2 Etching	**Si**	**Operating mode**	**Advanced normal**
		XeF_2 pressure	**4Torr**
		Pump out pressure	**1Torr**
		Single cycle duration	**15s**
		Number of cycles till complete suspension (W=10µm, 20µm, and 30µm)	**11**

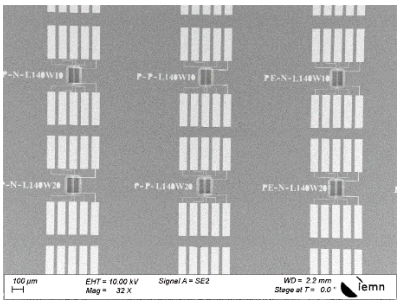
The etching process using XeF_2 exhibits a non-uniform etching rate per cycle. At the initial cycles of etching, the removal rate is lower compared to the later cycles. This variation is attributed to the presence of a thin layer of native SiO_2 that forms on the surface of the wafer prior to its introduction into the etching chamber in step8.1. Between step8 and step8.1, the exposed Si is subject to ambient air, resulting in the growth of a native SiO_2 layer. Consequently, during the initial XeF_2 etching cycles, it is necessary to penetrate through this thin native SiO_2 layer before reaching the Si substrate. The release of the membrane during the suspension process causes the removal of residual materials present in the Si_xN_y, wet SiO_2, SOI, and Box layers. As a result, the suspended membrane and the borders of the cavity may experience a metastable state, leading to sagging either upwards or downwards. This membrane bending can introduce significant mechanical challenges for the intended structure because stress tends to concentrate in sharp corners of the design, increasing the likelihood of crack formation. To mitigate this issue, all layers intended for etching processes (layer n°2, layer n°3, and layer n°21) feature rounded corners.

Figure 3-36 presents SEM images of suspended membranes utilized in a range of devices, including direct zT measurement devices (a), Seebeck coefficient devices (b), and thermal conductivity measurement devices (c). The images offer both top and tilt views of the suspended membranes in the respective devices, showcasing their structures and dimensions. This includes top views of the suspended membranes in zT measurement devices (d) and Seebeck measurement devices (f), and tilt views of the suspended membranes in Seebeck measurement devices with widths of 10 micrometers (g), 20 micrometers (h), and 30 micrometers (i). Additionally, top views are shown for suspended membranes in thermal conductivity measurement devices with widths of 10 micrometers (j) and 30 micrometers (l), while tilt views are provided for suspended membranes in thermal conductivity measurement devices with widths of 10 micrometers (k) and 30 micrometers (m). These SEM images offer valuable insights into the structural characteristics of the devices, aiding in the characterization and performance analysis of each device type.

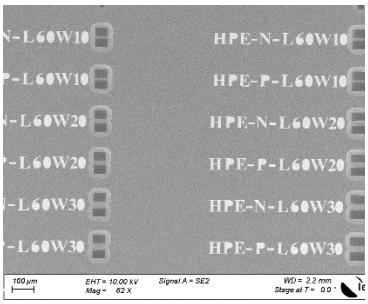
a)



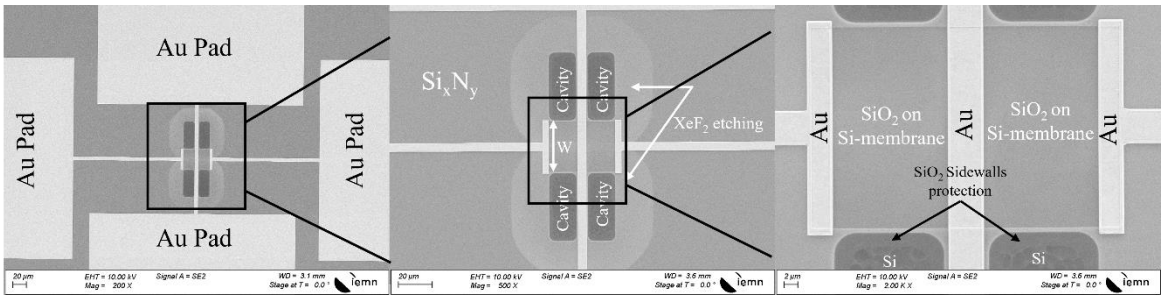
b)



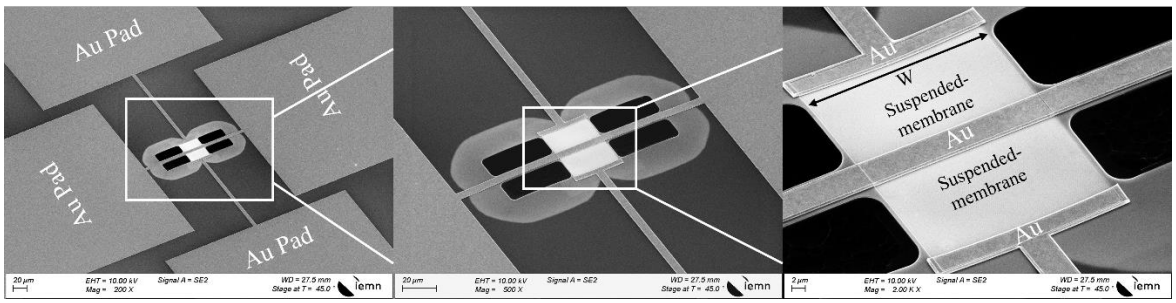
c)


HPE-N-L60W10
HPE-P-L60W10
HPE-N-L60W20
HPE-P-L60W20
HPE-N-L60W30
HPE-P-L60W30

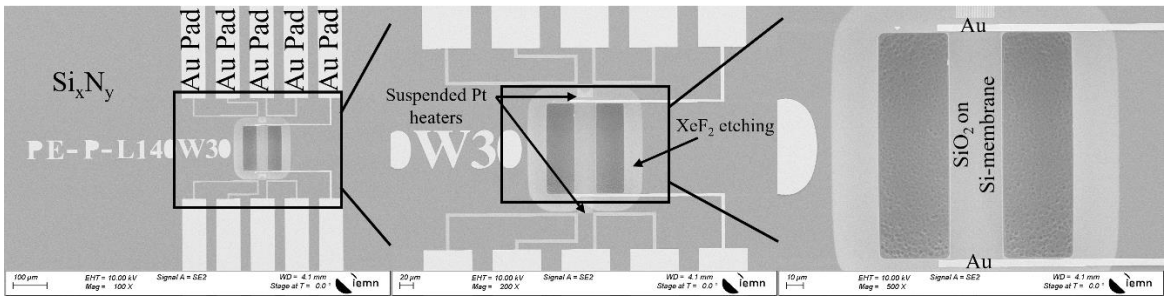
d)


Au Pad
Au Pad
Au Pad
Au Pad
Si_xN_y
Cavity
Cavity
Cavity
Cavity
W
XeF_2 etching
Au
SiO_2 on Si-membrane
Au
SiO_2 on Si-membrane
Au
SiO_2 Sidewalls protection
Si
Si

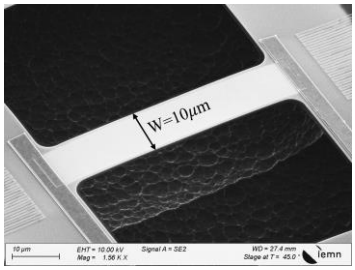
e)


Au Pad
Au Pad
Au Pad
Au Pad
Au
W
Suspended-membrane
Au
Suspended-membrane
Au

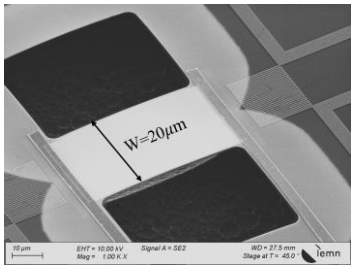
f)


Si_xN_y
Au Pad
Au Pad
Au Pad
Au Pad
Au Pad
PE-P-L140W30
Suspended Pt heaters
XeF_2 etching
Au
SiO_2 on Si-membrane
Au

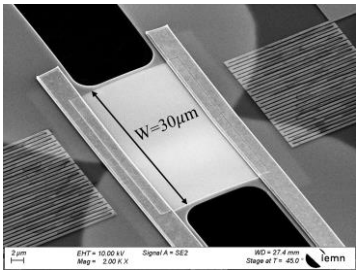
g)


W=10μm

h)


W=20μm

i)


W=30μm

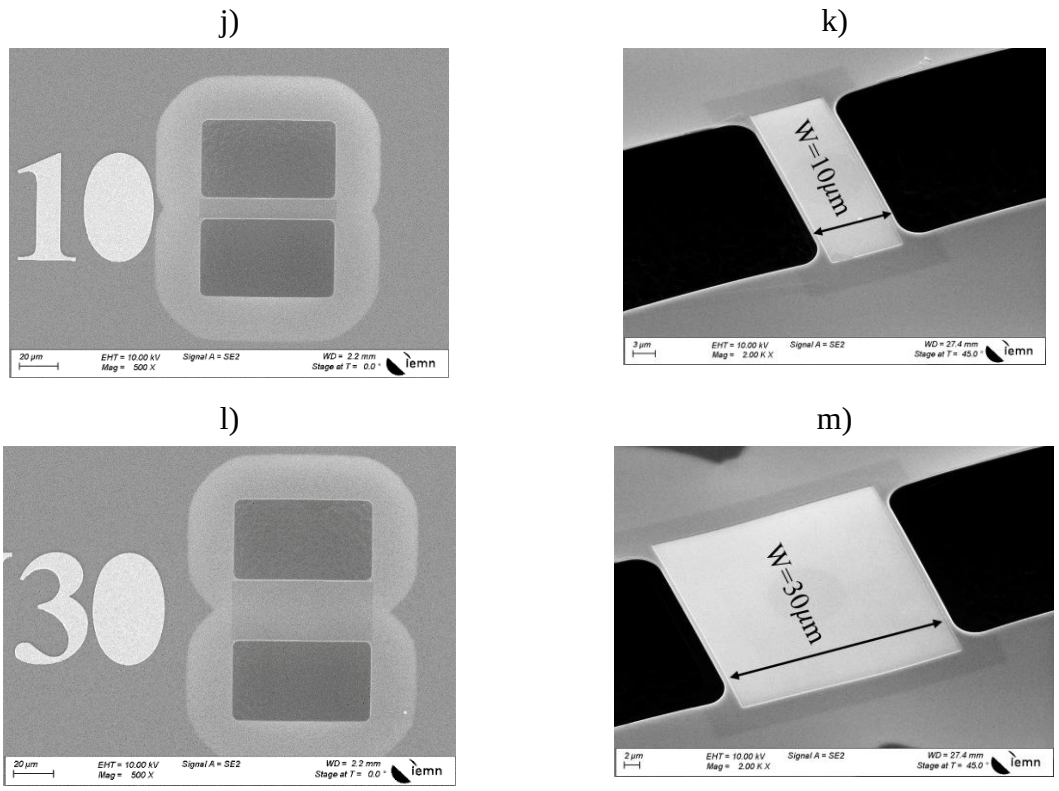


Figure 3-36: SEM images showcasing various suspended membranes used in a) direct zT measurement devices, b) Seebeck coefficient devices, c) and thermal conductivity measurement devices. Additionally, the figures present a top view of suspended membranes in d) zT measurement devices, f) Seebeck measurement devices and in thermal conductivity measurement devices with widths of j) 10μm and l) 30μm. Furthermore, a tilt view of suspended membranes in e) zT measurement devices, in Seebeck measurement devices with widths g) of 10μm h), 20μm and i) 30μm and in thermal conductivity measurement devices with widths of k) 10μm and m) 30μm.

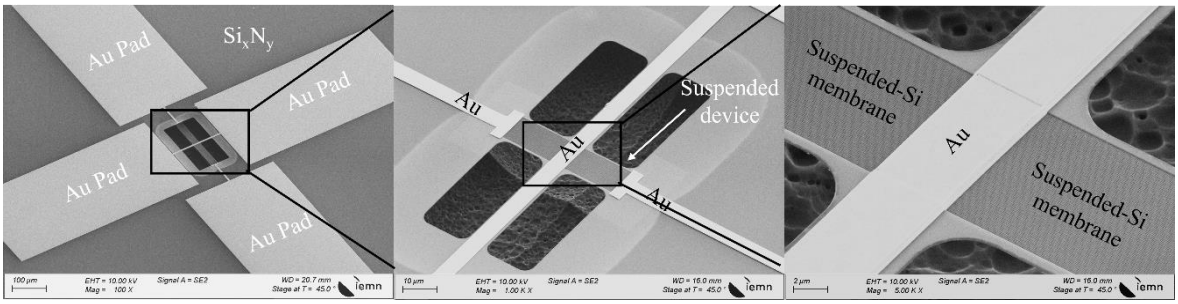
3.2.9.2 Step8.2: HF Vapor etching

The final step of the device fabrication process involves etching the Box layer from the membrane. Traditionally, wet etching techniques using HydroFluoric (HF) acid have been employed for this purpose. However, wet etching can be detrimental to the suspended membranes due to issues such as stiction, capillary forces, and nitrogen sample drying. To address these concerns, a dry etching method utilizing vapor HF is implemented instead. This technique significantly reduces the mechanical stress that occurs during etching and is conducted in a low-pressure environment. An advantage of dry etching is that it eliminates the need for rinsing or nitrogen drying after the etching process, as there are no reactive solutions involved. The etching mechanism of SiO_2 with HF gas involves a reaction where all resulting by-products are volatile, facilitating easy evacuation from the etching chamber. In the current case, HF etching is employed to remove the remaining SiO_2 layers fabricated in step1 and the 145nm thick Box layer located at the bottom of the SOI. The etching process adheres to the specifications provided in Table 3-30. Furthermore, Figure 3-37 illustrates several scanning electron microscope (SEM) images depicting the silicon membranes following the vapor HF etching process.

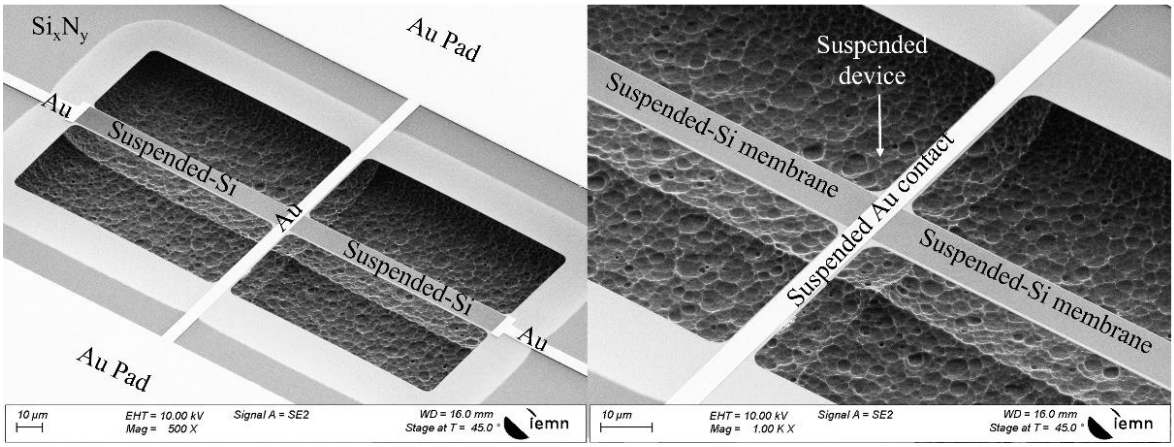
Table 3-30: Specifications of SiO2 etching using vapor HF method.

Process	*Step parameters*	
Pre-etching heating on heating plate	**Temperature**	**250°C**
	Duration	**2min**
Box under etching	**HF flow**	**310sccm**
	C_2H_5OH flow	**350sccm**
	N_2 flow	**1250sccm**
	Single cycle duration	**4min**
	Number of cycles	**1**
	Etch rate	**38nm/min**
Pre-etching heating on heating plate	**Temperature**	**250°C**
	Duration	**2min**

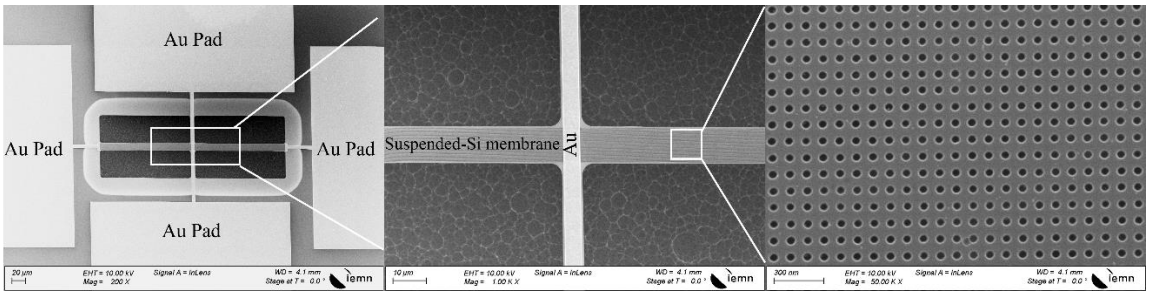
a)



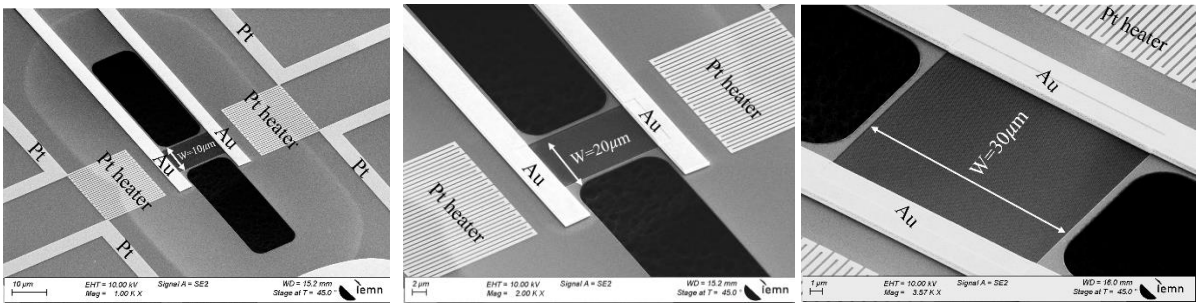
b)



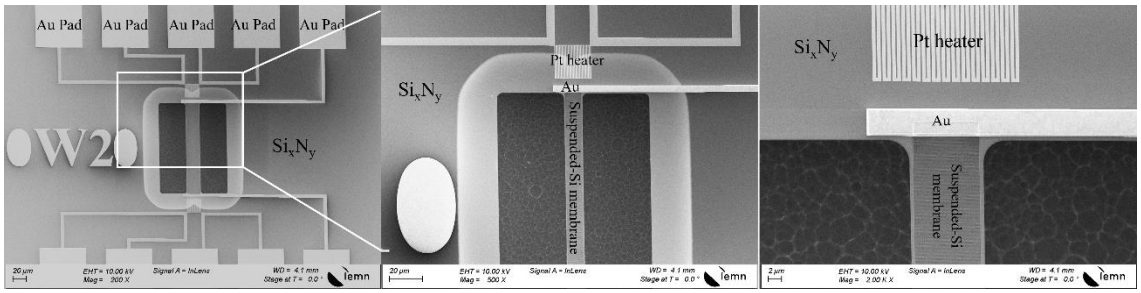
c)


Au Pad
Au Pad
Au Pad
Au Pad
Suspended-Si membrane
Au

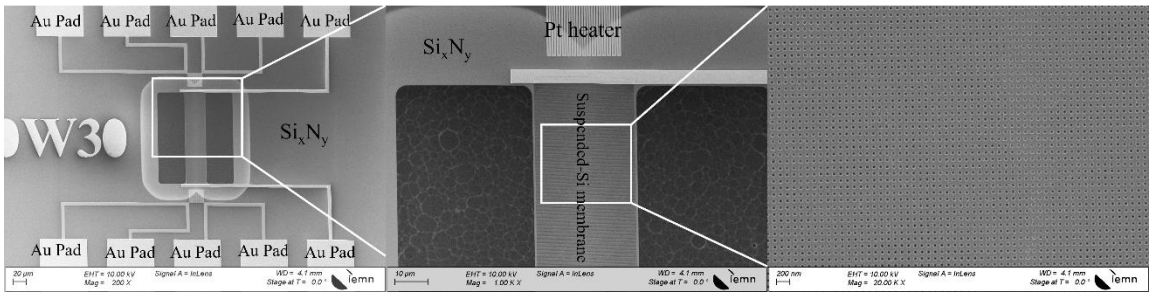
d) e) f)


Pt
Pt heater
Au
W=10μm
Pt heater
Pt
Pt
Pt heater
Au
W=20μm
Au
Pt heater
Pt heater
Au
W=30μm
Au

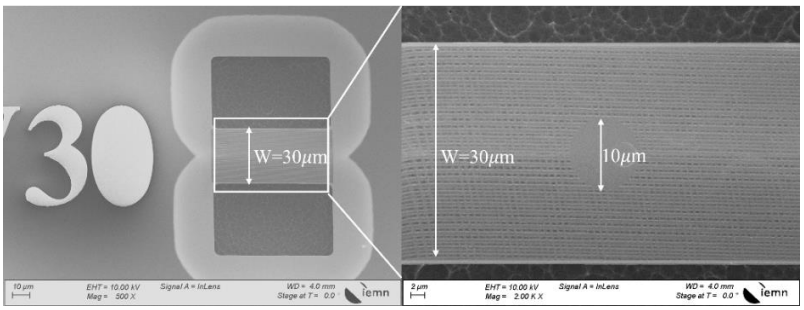
g)


Au Pad
Au Pad
Au Pad
Au Pad
Au Pad
W20
Si$_x$N$_y$
Si$_x$N$_y$
Pt heater
Au
Suspended-Si membrane
Si$_x$N$_y$
Pt heater
Au
Suspended-Si membrane

h)


Au Pad
Au Pad
Au Pad
Au Pad
Au Pad
W30
Si$_x$N$_y$
Au Pad
Au Pad
Au Pad
Au Pad
Au Pad
Si$_x$N$_y$
Pt heater
Suspended-Si membrane

i)


W30
W=30μm
W=30μm
10μm

j)

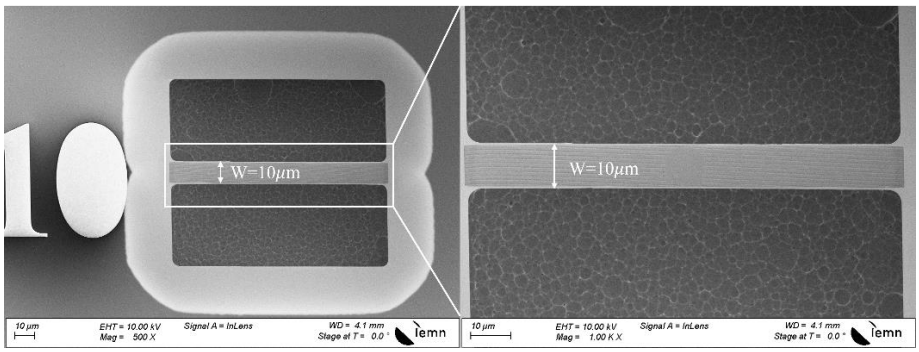


Figure 3-37:SEM images obtained after HF vapor step highlighting various aspects of the fabricated devices. a) Displays suspended Si membranes in direct zT measurement devices, b) offers a close-up view of the suspended Si membranes and a part of the suspended contact within the direct zT measurement devices. c) Zooms in on the pores present in the suspended membranes in the direct zT measurement device illustrating the effective removal of all silicon oxide grown during step1. A Tilt views of released Si membranes in Seebeck coefficient devices demonstrating their different widths d) 10μm e), 20μm and f) 30μm. Additionally, g) provides a close-up view of the suspended Si membranes in the Seebeck measurement devices. h) Showcase a detailed view of the pores in the suspended membranes in the Seebeck measurement device, indicating the successful removal of all silicon oxide grown during step1. Finally, the top view of suspended membranes in thermal conductivity measurement devices with widths of i) 30μm and j) 10μm is presented.

Additional information pertaining to the fabricated devices, including sample quantities, employed geometries, labeling procedures, and configurations, can be found in the appendix 1 for comprehensive reference.

Conclusion

This chapter has presented a comprehensive overview of the fabrication process of an integrated metrology device dedicated to transient Harman measurement of silicon nano-meshes and the elementary devices for the determination of thermal properties such as thermal conductivity, Seebeck coefficient, and electrical conductivity.

The chapter commenced by introducing the design of the devices, providing a thorough explanation of their structural components and operational principles. This design phase ensured that the devices were well-suited for the intended measurements and analysis. Subsequently, the fabrication process was described in detail, outlining the specific steps involved in creating each device. Detailed explanations and illustrations were provided, including SEM images at various stages of the process. These images aimed to enhance the clarity of the fabrication steps and also serve as visual evidence of the progress and quality of the fabricated devices. Finally, this fabrication process aligns with the standard complementary metal–oxide–semiconductor (CMOS) fabrication process, ensuring compatibility with industrial silicon CMOS process lines.

It's worth noting that the integrated metrology device designed for transient Harman measurements of silicon nano-meshes presented a more complex fabrication process compared to the metrology device dedicated for transient Harman measurements of bulk materials.

Chapter 4 Characterization of the fabricated devices and results

Abstract

This chapter aims at characterizing the devices developed in this thesis and discuss the obtained results. It is divided into four sections, each focusing on different aspects of measurement protocols and the impact of phonon engineering on specific properties. The first section addresses the measurement of the Seebeck coefficient. It describes the measurement protocol, including conditions and procedures, and examines the influence of phonon engineering on the Seebeck coefficient. The second section discusses electrical measurements. It outlines the measurement protocol and conditions and explores the impact of phonon engineering on electrical conductivity. The third section focuses on thermal conductivity measurements. It describes the measurement protocol and conditions and investigates the impact of phonon engineering on thermal conductivity. Finally, the fourth section covers direct *zT* measurements. It describes the measurement protocol and conditions, emphasizing the significance of accurate *zT* values for assessing device performance.

4.1 Seebeck coefficient measurements

In this section, we focus on the characterization of the Seebeck coefficient, which is one of the important thermoelectric transport properties of the developed devices. This characterization encompasses both phononic and non-phononic devices, considering their respective p-type or n-type characteristics, as well as different geometries discussed in Chapter 3. Our approach begins by introducing the fundamental principles of the measurement protocol for determining the Seebeck coefficient. Subsequently, we provide an in-depth analysis of the measurement conditions employed during the experiments. Finally, we present the obtained results, which offer insights into the thermoelectric behavior and performance of the devices under investigation.

4.1.1 Measurement protocol

4.1.1.1 Principle

The principle of the Seebeck coefficient measurement involves evaluating the voltage generated (Seebeck voltage) across a temperature gradient applied to a thermoelectric material

(Figure 4-1). The measurement setup typically consists of a thermoelectric (TE) sample, with one end exposed to a hot temperature source and the other end to a cold temperature sink. When a temperature gradient is established, charge carriers (electrons or holes) within the material experience a thermoelectric effect, resulting in the generation of a voltage. By measuring this voltage difference and the corresponding temperature gradient, the Seebeck coefficient can be calculated. The Seebeck coefficient reflects the material's ability to convert temperature differences into electrical potential, indicating its suitability for thermoelectric applications.

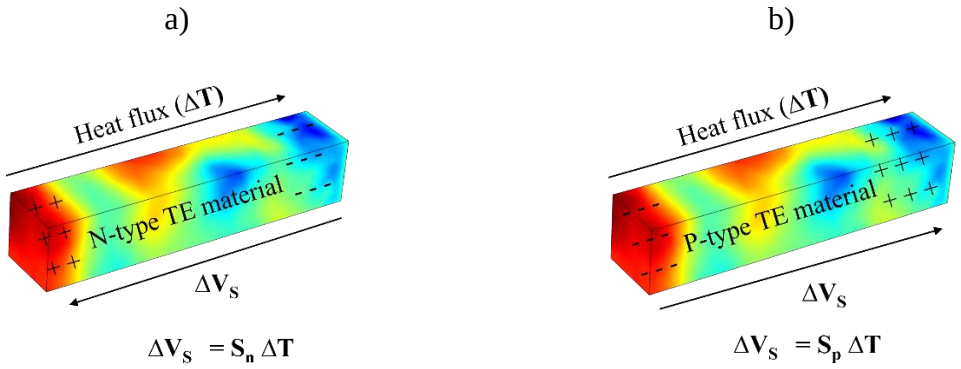


Figure 4-1: Seebeck voltage in both a) n-type (S_n<0) and b) p-type (S_p>0) thermoelectric materials.

In our specific case (Figure 4-2), the thermoelectric (TE) material under investigation is suspended. To establish the required temperature gradient, a platinum (Pt) heater is positioned in close proximity to one side of the TE material. This arrangement ensures that the Pt heater and the TE material reach the same temperature. Additionally, another heater is placed on the opposite side of the TE material. By measuring the resistance variation of both Pt heaters, the temperature gradient within the TE material can be determined. This approach allows for accurate characterization of the Seebeck coefficient by precisely controlling the temperature conditions and measuring the resulting voltage generated across the TE material.

In p-type thermoelectric (TE) materials, the Seebeck voltage is positive (ΔV_{Sp}), while in n-type TE materials, it is negative (ΔV_{Sn}). This polarity difference arises from the behavior of the dominant charge carriers. In p-type materials, positively charged holes move from the hotter side to the colder side, resulting in a positive accumulation of charge and a positive Seebeck voltage. In contrast, in n-type materials, negatively charged electrons migrate from the hotter side to the colder side, leading to a negative accumulation of charge and a negative Seebeck voltage. This distinction in polarity is crucial for understanding and utilizing the thermoelectric effect in TE materials.

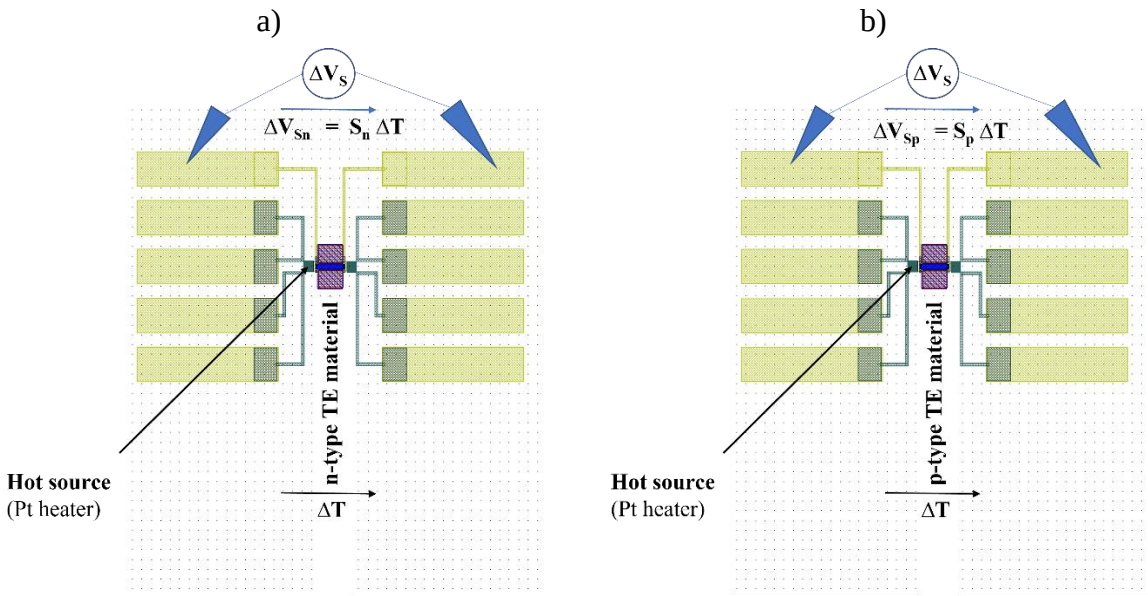


Figure 4-2: Seebeck coefficient measurement principle in both a) n-type and b) p-type TE materials.

The hot source in the Seebeck coefficient measurement setup is provided by a Pt heater. It is important to note that the electrical resistance (resistivity) of Pt increases with temperature due to the carriers' lifetime associated with electron-phonon collisions. At a given temperature T, the electrical resistance can be defined as:

$$R_{Pt}(T) = R_{Pt}(T_0).(1 + \alpha.\Delta T)$$

Equation 4- 1

Where $R_{Pt}(T)$ is the resistance at temperature T, $R_{Pt}(T_0)$ is the resistance at a reference temperature T_0, and α is the temperature coefficient of resistance. This equation captures the temperature dependence of Pt's electrical resistance, allowing us to determine the temperature change by measuring the resistance or variation of resistance. By comparing the measured resistance at a given temperature to the reference resistance at temperature T_0, we can calculate the corresponding temperature difference. This relationship enables us to accurately determine the temperature change within the Pt heater based on the measured electrical resistance.

Building upon the principle of the measurement protocol, we now turn our attention to the characterization conditions, which establish the necessary parameters and settings to ensure accurate and consistent measurements of the Seebeck coefficient.

4.1.1.2 Characterization conditions

In this section, the characterization process consists of two main parts. i) Firstly, we perform the calibration of the Pt heater serpentine to extract the temperature coefficient of resistance (TCR), denoted as α. This calibration involves varying the chuck's temperature while applying a low voltage bias to the heater, ranging from -10mV to 10mV with a step of 0.1mV. The choice of this low voltage range is to avoid heating the membrane through Joule effect. By registering the variation in Pt electrical resistance with temperature, we can extract α using Equation 4- 2.

$$\alpha = (R_{Pt}(T) - R_{Pt}(T_0))/(R_{Pt}(T_0).\Delta T)$$

Equation 4- 2

ii) The second part involves biasing the Pt heater with a variable voltage. With the knowledge of α, we convert the increase in electrical resistance due to the voltage variation into temperature using Equation 4- 3.

$$\Delta T = T - T_0 = \frac{R_{Pt}(T) - R_{Pt}(T_0)}{R_{Pt}(T_0).\alpha}$$

Equation 4- 3

To determine the temperature difference across the membrane, the resistances of both heaters placed on either side of the TE material are measured. The temperature difference (ΔT_H) created by the first Pt heater, serving as the hot source for the TE material, and the temperature difference (ΔT_C) in the second Pt heater placed on the other side of the membrane are both determined using Equation 4- 3. By subtracting the temperature difference created in the hot Pt heater from the temperature difference in the second heater, the temperature difference (ΔT_m) across the membrane is determined, as shown in Equation 4- 4. Additionally, the temperature gradient generated by biasing the Pt heater leads to the generation of a Seebeck voltage. These characterizations provide essential data on the temperature coefficient of resistance, temperature differences, and Seebeck voltage.

$$\Delta T_m = \Delta T_H - \Delta T_C = T_H - T_C$$

Equation 4- 4

i) Pt heater serpentine calibration

The characterizations are performed using a four-probe DC point probes measurement setup. This setup involves connecting the probes to an HP/Agilent 4155C semiconductor parameter analyzer, which serves as an accurate voltage source and current or voltage measurement unit. The HP4155C includes four source monitor units (SMU), capable of functioning as voltage source-current measurement units or current source-voltage measurement units. Additionally, it has two voltage measurement units (VMU) dedicated solely to voltage measurement and two voltage source units (VSU). In our measurements, the SMUs are utilized as voltage source-current measurement units, while the VMUs are used for voltage measurements. This is because the VMUs provide enhanced voltage measurement accuracy, with a precision of $\pm 0.2\mu V$ compared to $\pm 2\mu V$ and $\pm 1nA$ for the SMUs. The VMUs are specifically employed for potential difference measurements between two points.

The device under test is voltage biased through the SMUs on two contacts. The potential difference induced by the current from the voltage-biased contacts is measured using the VMUs on the other two contacts. This configuration allows us to determine the central Pt serpentine heater's properties without considering the resistance of the pads. Figure 4-3 provides a comprehensive overview of the measurement platform and its components; a) The measurement platform is depicted, showcasing the setup used for characterizations. b) A close-up view is presented, highlighting the precise positioning of the probes on the sample. c) The figure displays the probes' positioning in the layout, illustrating their specific arrangement on the device. d) The electrical circuit analogy of the Pt heater calibration is also included, outlining the circuitry and connections involved in this process. These visual representations provide a comprehensive overview of the Pt heater calibration process, including the measurement setup, equipment, probe positioning, and electrical circuitry involved.

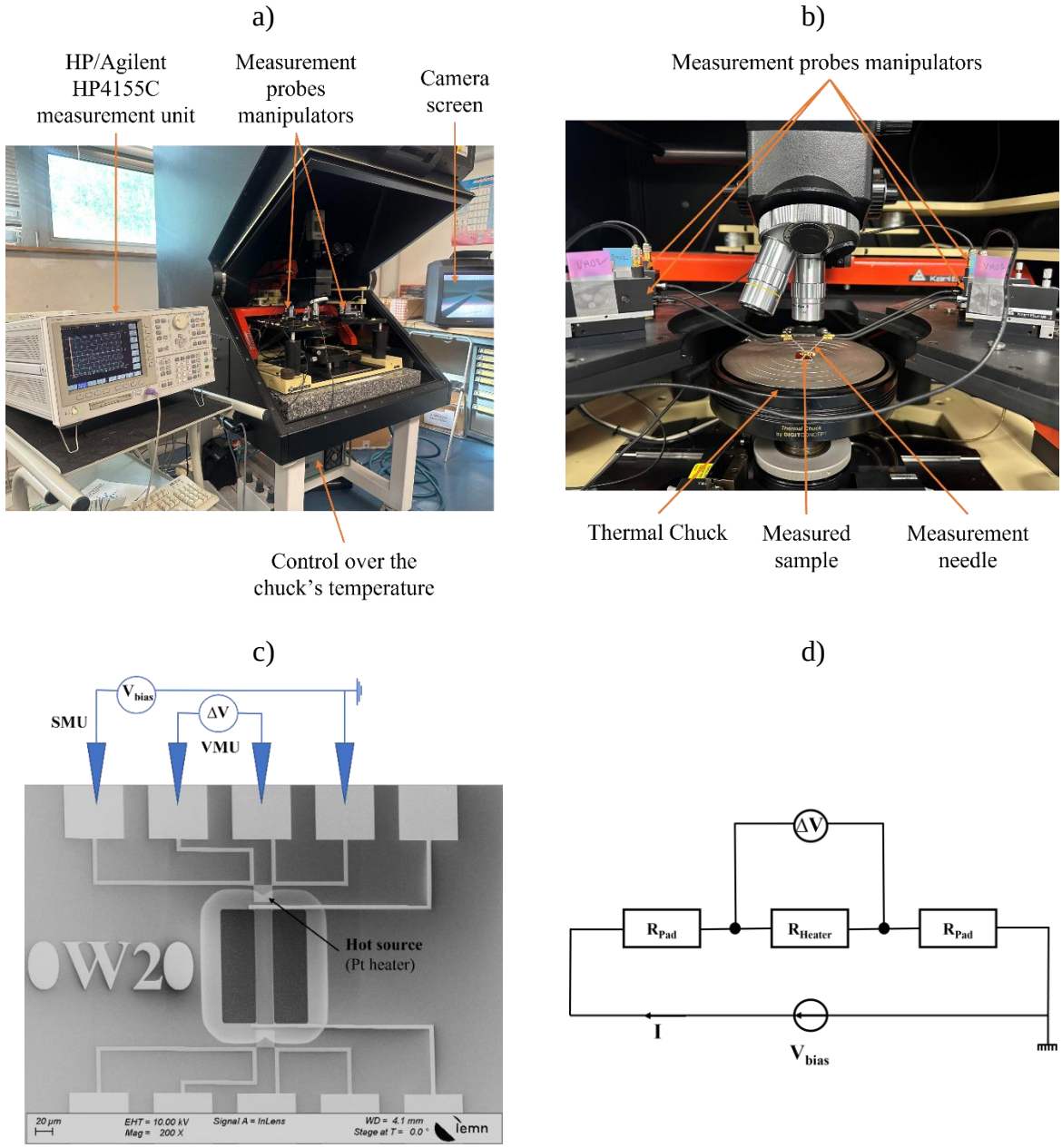


Figure 4-3: Pt heater calibration. (a) Measurement platform showcasing the setup used for characterizations. (b) Close-up view of the measurement set-up. (c) Probes' positioning in the Seebeck coefficient measurement device. (d) Electrical circuit analogy of the Pt heater calibration.

The measurement protocol for determining the Pt temperature coefficient of resistance (TCR) follows the procedure described above. The chuck's temperature is varied from ambient (23°C) to approximately 45°C, while a range of voltages (-10mV, 0.1mV, 10mV) is applied to the heaters. These voltage levels are intentionally kept at a modest range to prevent notable Joule effect-induced self-heating. This approach allows us to observe the effect of temperature variation on the Pt electrical resistance, as illustrated in Figure 4-3(c).

As expected, the electrical resistance of Pt exhibits a linear increase with the temperature of the chuck, as illustrated in Figure 4-4, in accordance with Equation 4- 5. By applying this

equation to the measured resistance values obtained from the three devices, the TCR α_i (where 'i' represents the device number) of each device is determined based on the fitting equation correlating the electrical resistance and the chuck's temperature (Equation 4- 6). The average TCR (α) value is calculated from the three measured α_i values (Equation 4- 8). To estimate the uncertainty or error in the calculated TCR (α) value, the error propagation calculation method is employed. This method involves propagating the uncertainties associated with the measured resistance values and the temperature readings to determine the overall error in the TCR (α) calculation. This approach enables us to consider measurement errors and provide a more dependable estimation of the TCR (α_i) values for the Pt heaters in the three devices. Considering that the final estimation of the TCR (α) is obtained through the fitting equation, we can propagate the $\Delta\alpha_i$ error using the Equation 4- 7. The approximate value of the final error $\Delta\alpha$ is calculated using Equation 4- 9 and is determined to be around 2%.

$$R_{Pti}(T) = a_i + b_i \Delta T$$

Equation 4- 5

With a_i and b_i being respectively the intercept and slope of the fitting equation of each device.

$$\alpha_i = b_i / a_i$$

Equation 4- 6

$$\Delta\alpha_i = \sqrt{(\frac{\partial \alpha_i}{\partial b_i}\Delta b_i)^2 + (\frac{\partial \alpha_i}{\partial a_i}\Delta a_i)^2}$$

Equation 4- 7

With Δa_i represents the error in the intercept, while Δb_i represents the error in the slope of the fitting equation for each device, as determined using Origin software.

$$\alpha = \frac{\sum_{i=1}^{n} \alpha_i}{n}$$

Equation 4- 8

$$\Delta\alpha = \sqrt{\sum_{i=1}^{n} (\frac{\partial \alpha}{\partial \alpha_i}\Delta\alpha_i)^2}$$

Equation 4- 9

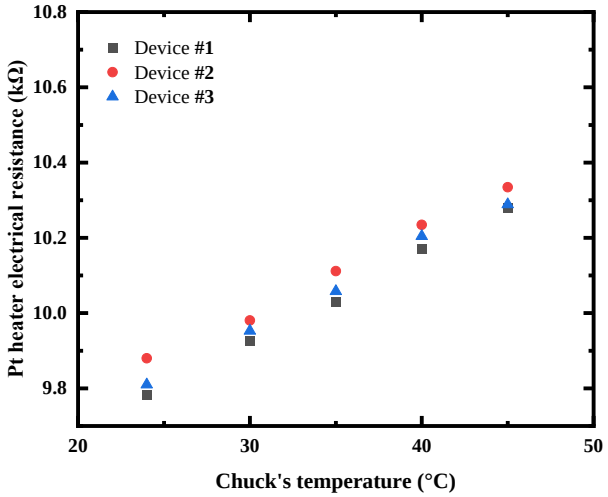


Figure 4-4: Pt electrical resistance variation with the chuck's temperature for three different devices.

The calculated TCR (α) is $2.49.10^{-3}\,K^{-1} \pm 5.10^{-5}\,K^{-1}$ and will be used as a common TCR to determine the temperature difference in all devices. Since all the measured devices are located on the same chip and were subjected to the same process, it can be assumed that the Pt TCR of the demonstrators is equal or at least close (taking into account measurement errors related to the dispersion of one device to another on the wafer.).

ii) Seebeck coefficient measurement

After calibrating the Pt heater, which constitutes the initial phase of measuring the Seebeck coefficient, we present the subsequent part of Seebeck coefficient measurement. This phase relies on measuring the voltage generated (Seebeck voltage) as a consequence of the temperature gradient across the membrane. To establish the temperature gradient, we subject the first Pt heater (heater 1) to a variable voltage bias. With knowledge of α, we convert the resulting increase in electrical resistance into temperature (ΔT_H) using Equation 4- 3. Simultaneously, the temperature difference (ΔT_C) in the second Pt heater (heater 2) is determined by measuring the increase in resistance in its corresponding heater. By subtracting the two temperature differences, we derive the temperature difference (ΔT_m) across the membrane. We also took into account the errors associated with the measurement process, including the error of the temperature coefficient of resistance (TCR) determined earlier. Additionally, we employ a voltmeter to measure the voltage generated.

Figure 4-5 illustrates the measurement protocol employed for determining the Seebeck coefficient. The measurements are conducted using a face-to-face configuration with five probes, as depicted in Figure 4-5 (b). In this setup, the first probe is connected to the Keysight/Agilent E5281B SMU module, which applies bias to heater 1 (Pt heater). The second and third probes are connected to the Keysight/Agilent E5281A ATTO level high-resolution SMU module, enabling the measurement of the voltage across heater 1 using a "null" current source. The fourth probe is connected to the ground. For the second heater (heater 2), the four probes (probe 6, 7, 8, and 9) are connected to an Agilent 34461A four-wire ohmmeter, allowing the measurement of the heaters' resistance. Additionally, an amperemeter (Agilent 34401 A) is connected in series with the Agilent 34461A four-wire ohmmeter to control the injected current. By adjusting the calibration measurement range, very low current can be injected to avoid the Joule effect in the heater. Finally, the remaining two probes (probe 5 and 10), which are linked to the membrane, are connected to an Agilent 34461A voltmeter. This setup allows the sensing of the voltage ($\Delta V_{Seebeck}$) generated by the temperature difference (ΔT_m) across the membrane.

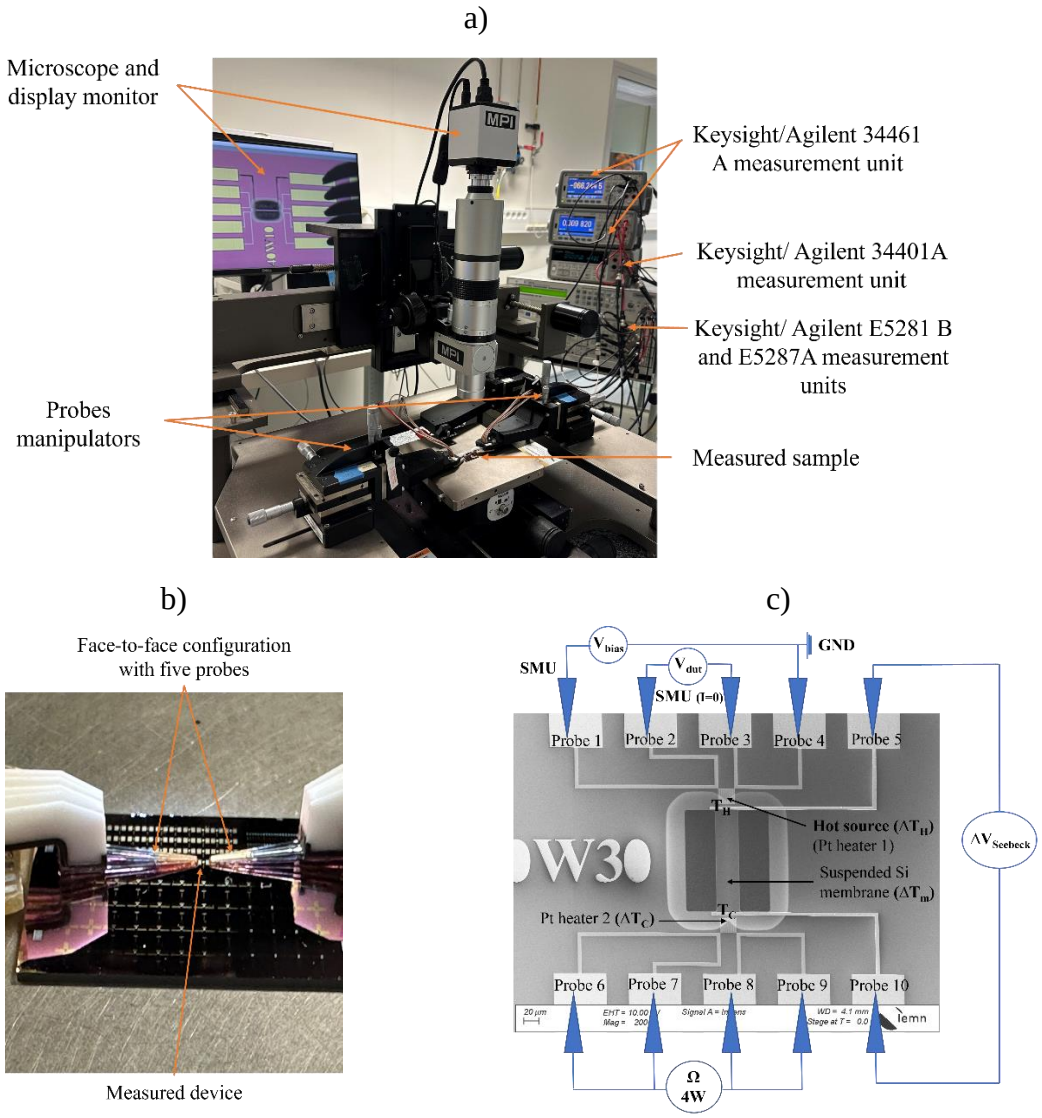


Figure 4-5: Seebeck coefficient measurement, a) platform displaying the setup utilized for characterizations., b) a close-up view of the face-to-face configuration with 5 probes., c) positioning of probes in the Seebeck coefficient measurement device.

The initial step in the Seebeck coefficient measurement protocol involves determining the reference resistance ($R_{Pt}(T_0)$) of both heaters at room temperature. This is essential for calculating the temperature difference across each heater once bias is applied to heater 1. The reference resistance for heater 2 can be directly obtained by reading its value from the connected four-wire ohmmeter. To determine the reference resistance of heater 1, a low voltage range of -10mV to 10mV is applied with a step size of 0.1mV, as explained during the calibration phase. The reference resistance is then determined by calculating the derivative of the measured voltage (V_{dut}) across probes 2 and 3 with respect to the current. Once the reference resistances for both heaters are established, heater 1 is biased using a voltage range that varies from 2.5V to 12V with a step size of 2.5V.

The voltage bias control for heater 1 in the Seebeck coefficient measurement setup was achieved through the utilization of IC-CAP software. IC-CAP software enabled automated measurements and efficient data acquisition. The determination of heater 1 resistance at different temperatures was conducted using IC-CAP, leveraging its robust mathematical models

and algorithms. Furthermore, essential parameters including resistance determination and voltage Seebeck measurements ($\Delta V_{Seebeck}$) were directly obtained from the connected instruments, ensuring the acquisition of precise and dependable results.

4.1.2 Seebeck coefficient measurements results

In this section, we present the findings of the Seebeck coefficient measurements conducted on both plain and phononic membranes in both p-type and n-type configurations, considering various geometries. This section is divided into two parts.

The first part focuses on studying the management of thermal gradient within the sample and investigating the impact of phonons and geometry on the thermal gradient across the membranes. This analysis provides valuable insights into the thermal transport dynamics and how factors such as phonons and membrane geometry affect the temperature distribution.

The second part delves into examining the dependence of the Seebeck coefficient on phonons, membrane geometry, and the type of material (n-type or p-type). By exploring these dependencies, we gain a deeper understanding of how the Seebeck coefficient is influenced by phonon behavior, membrane structure, and the type of dopants present in the material (n-type or p-type).

4.1.2.1 Temperature gradient management

The investigation of temperature gradient management encompasses the study of two factors: (i) phonon engineering patterns and (ii) membranes' geometry.

i) ***Phononic engineering impact on the temperature gradient management***

The impact of phonon engineering on temperature gradient management is assessed by examining the temperature difference across silicon membranes under the same heating power. Since the devices are identical except for the phonon engineering, any difference in temperature across the silicon membranes can be attributed solely to the phonon engineering.

The methodology for these measurements is explained in Section 4.1.1.2. Figure 4-6 illustrates the temperature difference across the same silicon membranes in response to the heating voltage (left) and heating power (right), accompanied by the corresponding errors. The p-type plain membrane is represented in red, while the p-type phonon-engineered (PE) membrane is depicted in black. As expected, it is observed that the temperature difference across the membrane increases quadratically with the heating voltage. Figure 4-6 b presents the temperature difference across the membrane. Notably, for a given amount of heat power, the PE membranes exhibit a higher temperature difference across the membrane, resulting in improved thermal gradient management, or reduced thermal conductance, through the membrane as anticipated. It is important to consider that as the temperature difference (ΔT_m) increases in magnitude, the associated error in its measurement also increases.

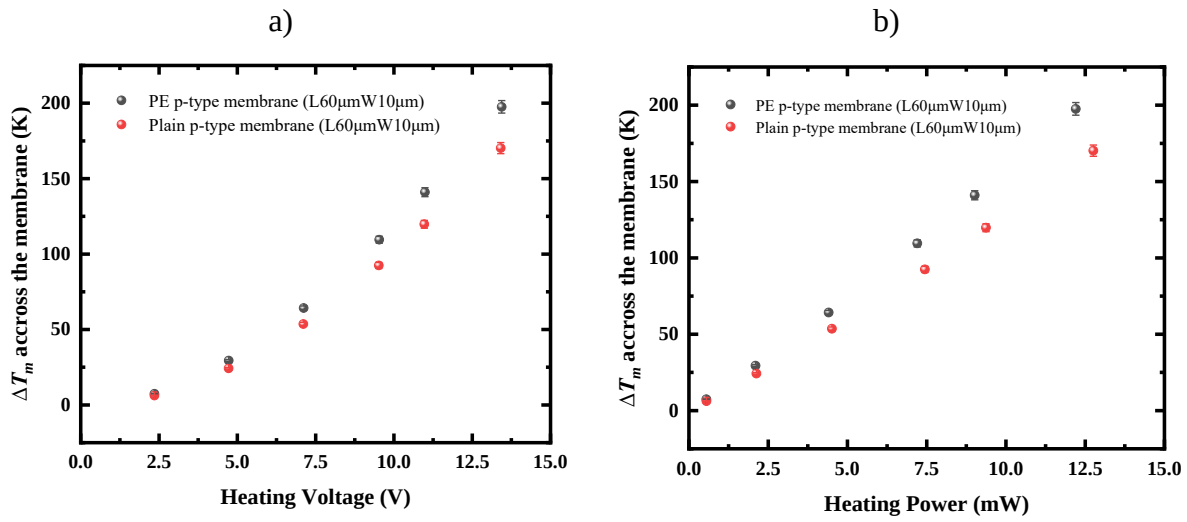


Figure 4-6: The temperature difference across the same p type silicon membrane in response to a) the heating voltage, b) and heating power. The plain membrane is represented in red, while the phonon-engineered (PE) membrane is depicted in black.

Phonon engineering plays a crucial role in enhancing the management of thermal gradients in membranes. This improvement stems from the increased thermal resistances exhibited by silicon membranes that have undergone the phonon engineering process. However, it is challenging to precisely determine the enhancement factor between the thermal resistances of plain and phonon engineered membranes across the temperature difference depicted in Figure 4-6. This difficulty arises due to the presence of parallel thermal resistance introduced by the substrates and the surrounding environment of the membrane. The combined effect of these factors makes it challenging to isolate and quantify the specific contribution of the phonon engineering process to the overall thermal gradient management in the membranes.

ii) ***Membranes' geometry impact on the temperature gradient management.***

The influence of membranes' geometry on temperature gradient management is evaluated by analyzing the temperature difference across silicon membranes subjected to the same heating power. Figure 4-7-a summarizes the temperature difference across the p-type phononic membranes with different length and width ranging from 20 μm to 100 μm for length and 10 μm to 30 μm for width. Furthermore, Figure 4-7-b illustrates the temperature difference across p-type phononic membranes with varying widths but the same length 60μm, while Figure 4-7-c displays the temperature difference across p-type phononic membranes with different lengths but the same width 10μm. It can be observed that the temperature difference increases with membrane length and decreases with membrane width.

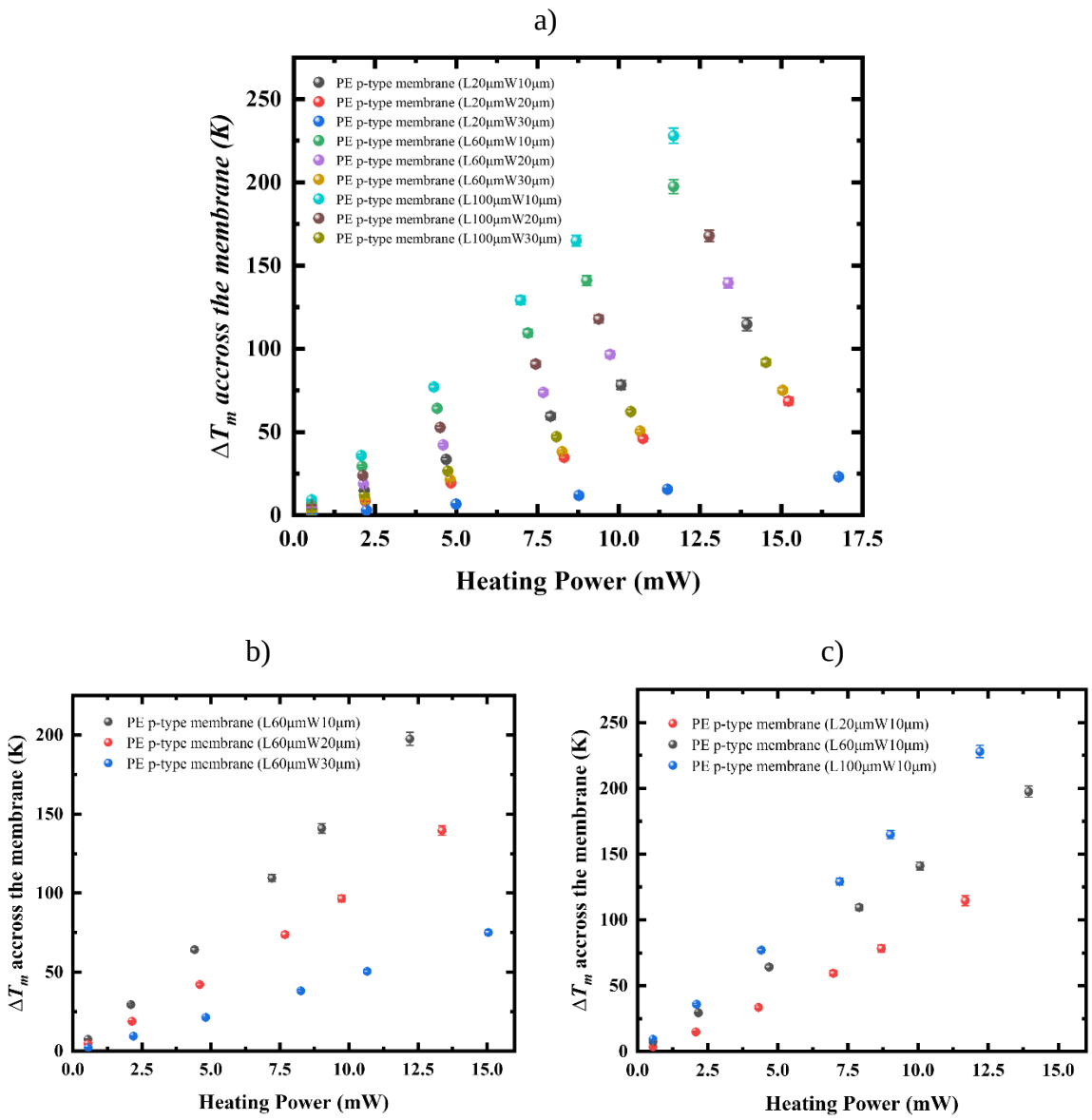


Figure 4-7: The temperature difference across p type silicon PE membranes with a) with different length and width ranging from 20 μm to 100 μm for length and 10 μm to 30 μm for width b) varying widths but the same length 60μm, b) different lengths but the same width 10μm.

The increase in thermal gradient with length can be attributed to the longer pathway for heat conduction within the membrane. As the length of the membrane increases, heat has to travel a greater distance, resulting in a larger temperature difference across the membrane. On the other hand, the decrease in thermal gradient with width can be explained by the increased cross-sectional area available for heat conduction. A wider membrane provides more pathways for heat to distribute, allowing for a more even distribution of temperature and reducing the temperature difference across the membrane. Therefore, as expected, it can be concluded that a membrane with a greater length and narrowed width represents the configuration that achieves the highest temperature gradient.

4.1.2.2 Seebeck coefficient measurements

The Seebeck coefficient was investigated for both phononic and non-phononic devices, considering their respective p-type or n-type characteristics. The measurement procedure is described in detail in Figure 4-5, and the results are presented in Figure 4-8. Figure 4-8 illustrates the relationship between the Seebeck voltage and the temperature difference across the membrane. The dataset includes measurements for various configurations: The data includes measurements for: Figure 4-8-a) plain p-type membrane with a length of 60μm and a width of 10μm, Figure 4-8-b) phononic-engineered (PE) p-type membrane with a length of 60μm and a width of 10μm, Figure 4-8-c) plain n-type membrane with a length of 20μm and a width of 10μm, and Figure 4-8-d) PE n-type membrane with a length of 20μm and a width of 10μm. The slope of each curve in Figure 4-8 corresponds to the Seebeck coefficient value.

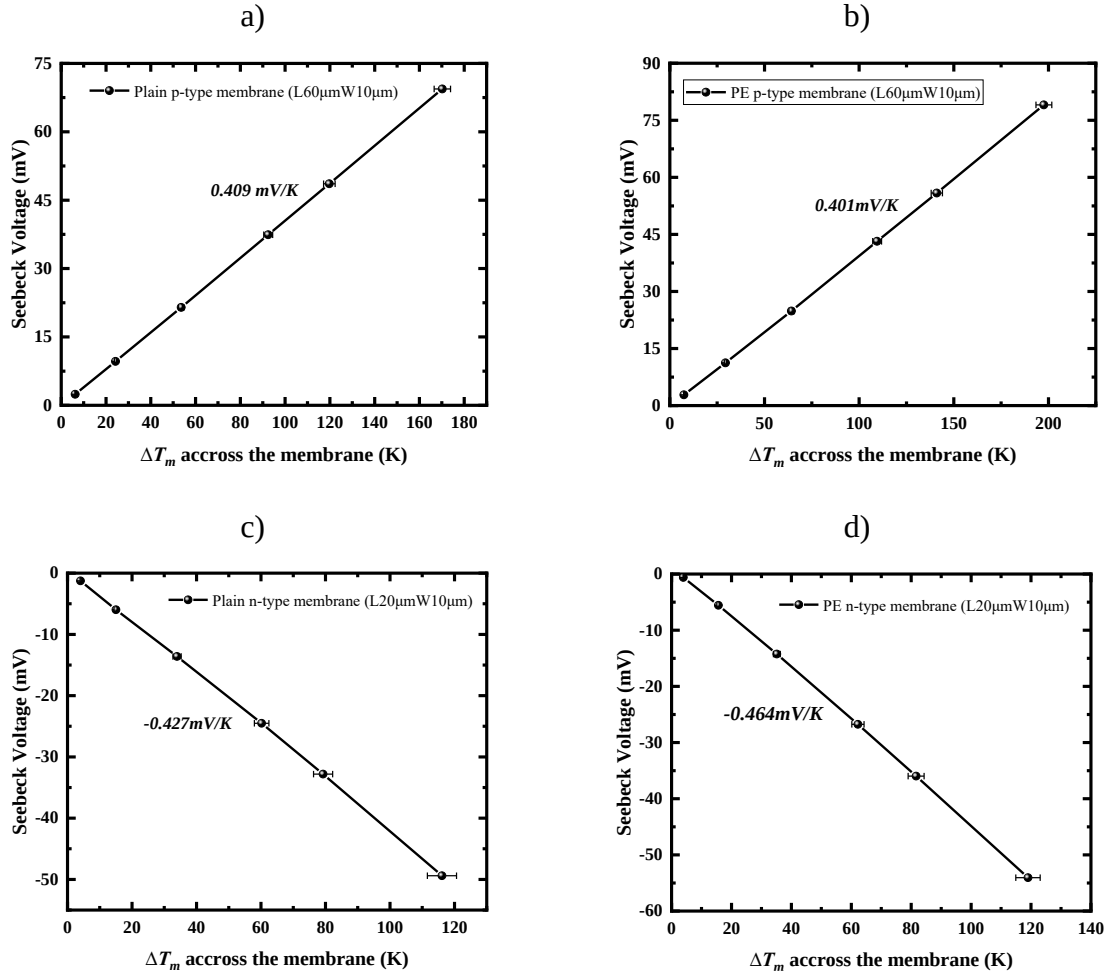


Figure 4-8: Seebeck voltage as a function of the temperature gradient across different membranes; a) plain p type membrane, b) PE p type membrane, c) plain n type membrane, d) PE n type membrane.

To obtain the mean value for each type of membrane, the average Seebeck coefficient is calculated by considering multiple membranes with different lengths and widths. These mean values, along with their corresponding errors, are presented in Table 4-1. The errors are determined using the error propagation calculation method, which takes into account the errors associated with the temperature difference calculations using the temperature coefficient of resistance (TCR).

Table 4-1: presents the values of the Seebeck coefficient for different types of membranes investigated in this study. The membranes included in the table are plain p-type membranes, phononic-engineered (PE) p-type membranes, plain n-type membranes, and PE n-type membranes.

	Plain p-type membranes	PE p-type membranes	Plain n-type membranes	PE n-type membranes
S [mV/K]	0.424	0.440	- 0.451	- 0.504
ΔS [mV/K]	$1.50.10^{-3}$	$1.14.\ 10^{-3}$	$1.58.\ 10^{-3}$	$2.81.\ 10^{-3}$

The table provides a comprehensive overview of the mean Seebeck coefficients for different membrane types, allowing for a quantitative comparison and analysis. The error values associated with each mean coefficient provide a measure of the uncertainty in the measurements, enabling a more accurate assessment of the results. The calculation methodology for determining these errors is explained in detail in Section 4.1.1.2.

The absolute values of the Seebeck coefficient exhibit comparability among all membrane types, irrespective of whether they are phononic-engineered (PE) or plain, and regardless of their p-type or n-type characteristics. This observation is depicted in Figure 4-9, where the measured absolute Seebeck voltage is plotted against the temperature difference across the membrane. It emphasizes the intrinsic nature of the Seebeck coefficient, which is predominantly influenced by the fundamental properties of the material rather than its geometric arrangement. This robustness of the Seebeck coefficient as a material-specific parameter underscores its strong correlation with crucial factors such as composition, doping levels, and electronic structure.

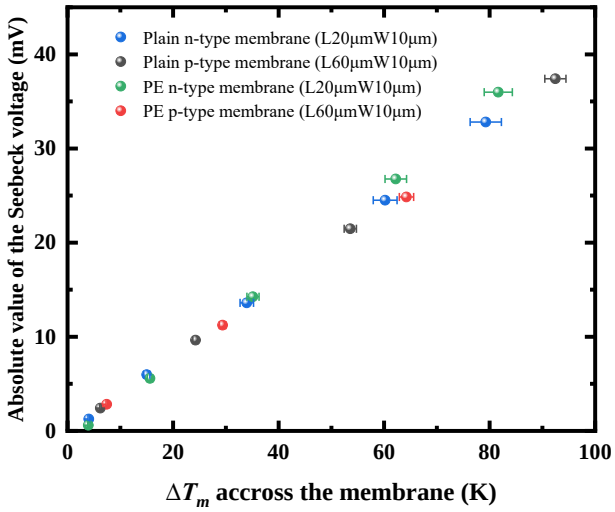


Figure 4-9: The absolute measured Seebeck voltage as a function of the temperature difference across different Si membranes. The data points represent different membrane types: phononic-engineered (PE) p-type membrane is represented in red, plain p-type membrane in black, plain n-type membrane in blue, and PE n-type membrane in green.

Our research focused on investigating the Seebeck coefficient of silicon (Si) membranes, both plain and phononic-engineered, for both n-type and p-type characteristics. We compared the measured Seebeck coefficient of our Si membranes with the Seebeck coefficient of bulk Si. Remarkably, we found that our measured Seebeck coefficient closely aligns with that of bulk Si[87](Figure 4-10). Furthermore, when comparing our results with the literature

values for Si-On-Insulator (SOI) materials, we observed consistency with the reported values [88].

In a degenerate semiconductor, the total Seebeck coefficient (S_{tot}) is influenced by two specific components: the diffusive contribution (S_{diff}) and the phonon drag contribution (S_{drag}). The diffusive contribution originates from the migration of charge carriers in response to temperature gradients, while the phonon drag contribution arises from the exchange of momentum between the non-equilibrium phonon populations and the charge carriers. Geballe and Sadhu reported that S_{ph} is significantly observed in bulk Si at room temperature [89][90].

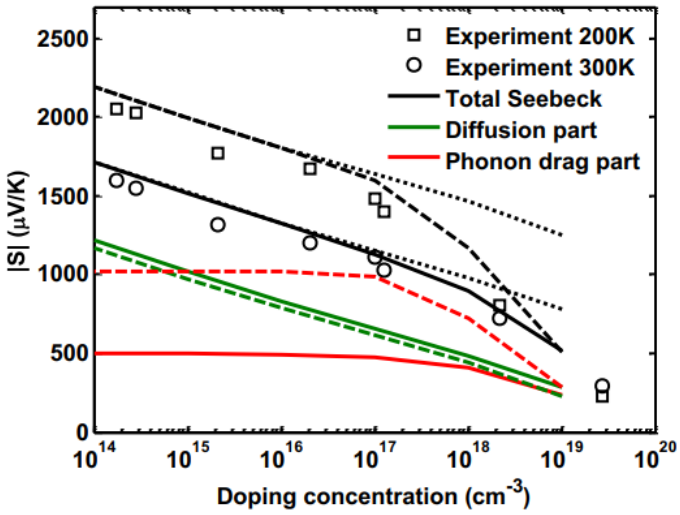


Figure 4-10: Calculated Seebeck coefficient with respect to doping concentrations for n-type silicon at 300 K and 200 K on a semi-log plot. The solid lines describe the calculated results at 300 K and dashed lines represent those at 200 K. Circles and squares are taken from the experiment [89]. At each temperature the total Seebeck coefficient (black) as well as the decomposition into the phonon drag part (red) and diffusion part (green) is shown. Dotted lines are the total Seebeck coefficient calculated using the low doping level value of the phonon drag contribution and assuming this value will not be reduced as the doping concentration increases (i.e., neglecting the "saturation" effect). Compared with the dotted lines, the experimental Seebeck coefficient has a further decrease beyond 10^{17} cm^{-3} doping concentration, which is due to the decrease of the phonon drag contribution. This is captured by considering electron scattering of phonons and the resulting Seebeck coefficient (black solid lines for 300 K and black dashed lines for 200 K) agrees with experiments across the full range of doping concentrations [87].

We delved into the study conducted by H.Ikeda *et al.*[91], which specifically examined the contribution of the phonon drag effect to the Seebeck coefficient in p-doped ultrathin SOI layers with varying thicknesses. While phonon drag is commonly associated with low temperatures and bulk Si, F. Salleh *et al.*[88] demonstrated its significant influence near room temperature, particularly in the lightly doped region ($N_D < 10^{19}$ cm^{-3}, Where N_D is the doping level), with its dependence on carrier concentration evident in Figure 4-11. The Seebeck coefficient (Equation 4- 10) was found to be a combination of two components: one related to electrons (S_e) and the other to phonons (S_{ph}).

$$S_{total} = S_e + S_{ph}$$

Equation 4- 10

Figure 4-11 plots the Seebeck coefficient as a function of carrier concentration, with broken, dotted, and solid lines representing the total Seebeck coefficient (S_{total}), electron-related Seebeck coefficient (S_e), and phonon-related Seebeck coefficient (S_{ph}), respectively. The filled square represents the reported S_{ph} value for bulk Si.

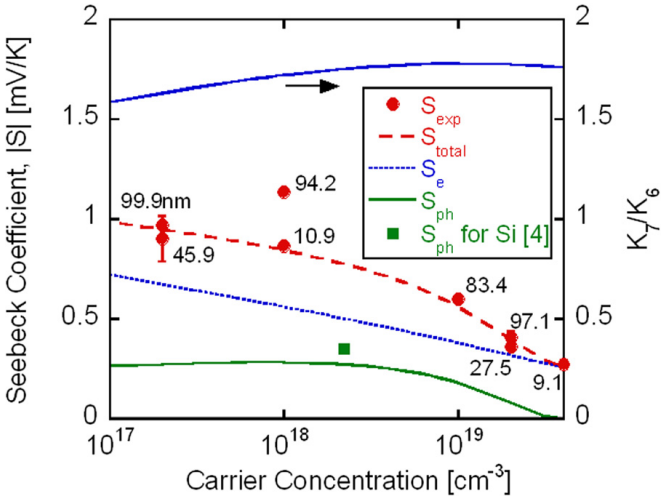


Figure 4-11: (Left y-axis) S and (right y-axis) ratio of the parameter integral, as a function of carrier concentration. The broken, dotted, and solid lines represent S_{total}, S_e, and S_{ph}, respectively. The filled square represents the reported S_{ph} value for bulk Si[92].

Additionally, H. Ikeda *et al.*[91] investigated the Seebeck coefficient of SOI layers with various thicknesses and found a close resemblance to the Seebeck coefficient of bulk Si for thicknesses above 6 nm. This observation suggests that the quantum confinement effect, which impacts electronic properties due to reduced dimensions, is not significant in Si layers as thin as 6 nm. Moreover, an enhancement of the Seebeck coefficient was observed at higher impurity concentrations ($N_D > 10^{19}$ cm^{-3}, Where N_D is the doping level), likely linked to the formation of an impurity band. Calculations of the impurity band density of states (DOS) indicated its considerable influence above approximately $10^{19}cm^{-3}$. Figure 4-12(a) presents the absolute Seebeck coefficient of silicon-on-insulator (SOI) wafers plotted against the carrier concentration. The solid line represents the calculated values, while the broken and dotted lines serve as visual aids. The Seebeck coefficient demonstrates a notable dependence on the carrier concentration, as depicted in the graph. In Figure 4-12(b), the energy derivative of the density of states (DOS) at the Fermi energy is shown as a function of impurity concentration. This derivative is computed based on three distinct influences of heavy doping: the creation of an impurity band resulting from the overlap of bound electron wave functions, the shift of ionization energy (ED) of an impurity atom due to screening by conduction electrons, and the scattering of electronic states near the conduction band edges caused by atomic arrangement disorder. The broken line in the graph is included as a visual reference.

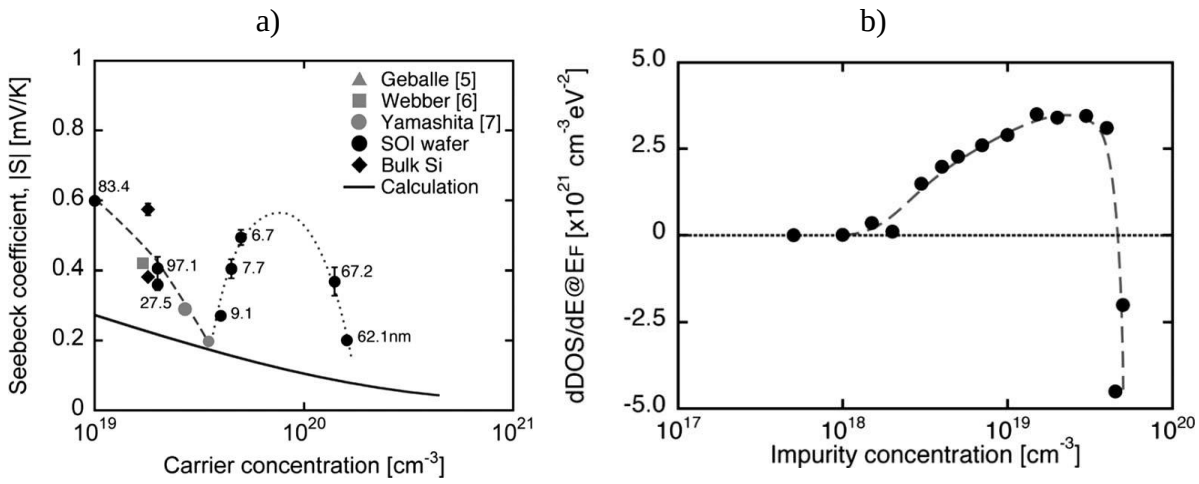


Figure 4-12:a) Absolute Seebeck coefficient of SOI wafers as a function of carrier concentration. The solid line represents the calculated value, and the broken and the dotted lines are drawn as an eye-guide. b) Energy derivative of DOS at the Fermi energy, computed on the basis of the three influences of the heavy doping, as a function of impurity concentration. The broken line is drawn as an eye-guide [91].

Figure 4-13 provides a comprehensive summary of these findings, indicating that the Seebeck coefficient is influenced by phonon drag at carrier concentrations below $3.5.10^{19}cm^{-3}$. Conversely, for SOI layers with carrier concentrations above this threshold, the Seebeck coefficient is primarily governed by the DOS distribution.

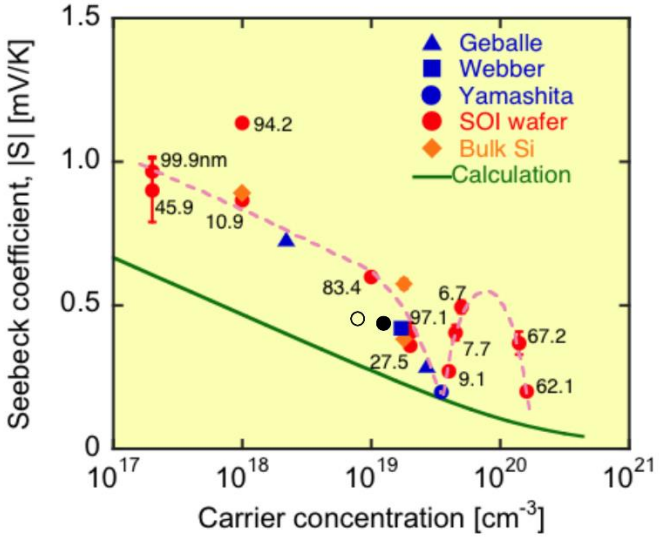


Figure 4-13: Seebeck coefficient of ultrathin SOI layers as a function of carrier concentration [93] Our experimental data is represented by black circles, where filled circles denote p-type Si membranes and open circles represent n-type Si membranes.

Notably, the observed contribution of phonon drags and the influence of the impurity band density of states are specific to Si on insulator materials. In a related study by Veerappan Manimuthu *et al.*[94], the Seebeck coefficient of germanium (Ge) on insulator layers (GOI) was investigated. They discovered that the measured values of the Seebeck coefficient in GOI closely matched the theoretical values (Figure 4-14). This finding indicates the absence of

phonon drag contribution in GOI layers, a contrast to what is typically observed in SOI layers. The disparity between Si and Ge can be attributed to variations in their material parameters.

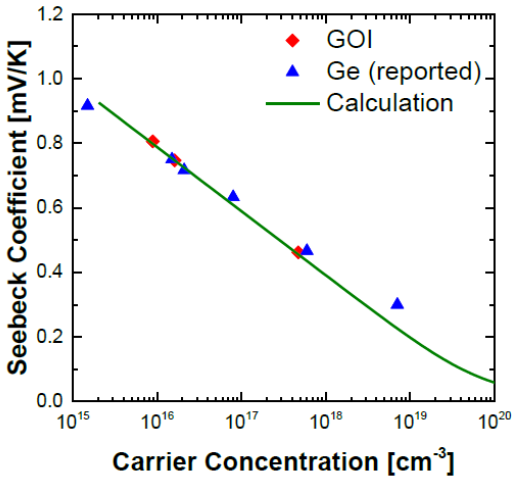
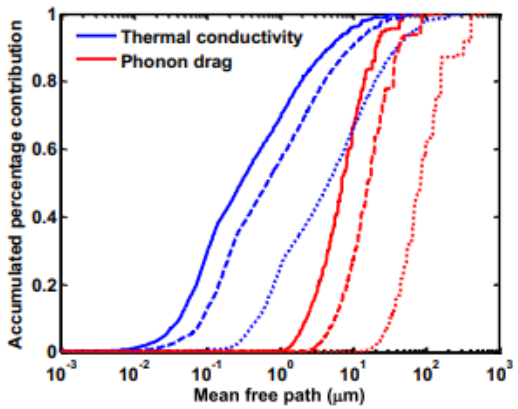


Figure 4-14: Seebeck coefficient (S) of GOI layer as a function of carrier concentration. The solid line represents the theoretical calculated values of the Seebeck coefficient of Ge [94].

In summary, when considering an SOI wafer, the phonon drag contribution significantly affects the total Seebeck coefficient. This suggests that we have the potential to decrease thermal conductivity without compromising the Seebeck coefficient considerably. As depicted in Figure 4-15-a, achieving this involves the strategic design of a phonon filter that selectively targets certain mean-free-path phonon modes. At 300 K, phonons with mean free paths shorter than 1 μm contribute approximately 70% to the total thermal conductivity while having a minimal impact on the phonon drag effect. This implies that by "filtering out" these phonon modes, we could potentially reduce thermal conductivity by 70% without significantly affecting the Seebeck coefficient. Furthermore, Figure 4-15-b illustrates the phonon drag Seebeck coefficient under various upper thermal conductivity bounds. In the context of heavily doped silicon, there was a prevailing belief that the phonon drag effect would be entirely suppressed, particularly when attempting to lower thermal conductivity. However, Zhou *et al.*[87] demonstrated that even in a heavily doped n-type silicon sample with a low thermal conductivity value (4 W/m.K), a phonon drag contribution of approximately 25% relative to the diffusive contribution can still exist.

a)



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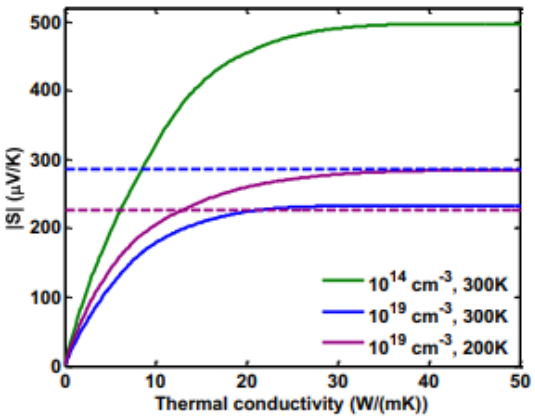


Figure 4-15: a) Phonon mode-specific accumulated contributions to the phonon drag Seebeck coefficient and the thermal conductivity with respect phonon mean free path. Solid lines show the contribution at 300 K, and dashed lines are used at 200 K and dotted lines at 100 K. These results are obtained for lightly doped n-type silicon. b) Contribution of the most preferable modes to the phonon drag Seebeck coefficient at different reduced thermal conductivity values[87].

4.1.2.3 Temperature Difference Confirmation: An Insight from Thermal Measurements

This section addresses the confirmation of the temperature difference measured across the suspended silicon membrane discussed in Section 4.1. The temperature variation across the membrane was initially determined using electrical measurements, involving the evaluation of Pt heater resistance changes and the Temperature Coefficient of Resistance (TCR) of the Pt heaters. Subsequently, a thermal measurement method (Transient Thermo-Reflectance) was employed to validate the results obtained through the electrical measurements.

Transient Thermo-Reflectance (TTR) is a technique applied in thermal science and materials research to study temperature profiles within thin film materials. This method relies on observing how a material responds to a controlled heat pulse, primarily by monitoring changes in the reflectance of a laser beam directed at the material's surface over time. By analyzing these changes following the heat pulse, TTR allows for insights into the propagation of temperature within the material, facilitating the examination of its thermal properties on the micro and nanoscale.

Similar to electrical temperature measurements across the membrane, thermal measurement involves a calibration process. This step is crucial for determining the coefficient of reflectance (CTR), which defines the relationship between the TTR signal and temperature variations. In our specific case, we determined two CTR values: one for Pt heaters to measure their temperature and another for the Si membrane to directly assess the temperature difference across the membrane. The process involves precise calibration steps, including selecting the appropriate wavelength for the probe laser beam, which is critical for maximizing reflectance changes in response to temperature variations in each material. We chose a wavelength of 530 nm for Pt heaters and a wavelength close to UV, specifically 365 nm, for the Si membrane since it is much more absorptive than in the visible range. Temperature control via the thermal chuck ranged from 25°C to 80°C. Controlled heating ramps were applied to the sample while monitoring changes in the surface reflectance. The resulting data were utilized to construct calibration curves for each material, elucidating the relationship between the TTR signal and actual temperature variations. In our experiments, we found CTR values of 1.21×10^{-4} K^{-1} for Pt and 1.37×10^{-4} K^{-1} for Si. These values serve as essential conversion factors, enabling the derivation of temperature profiles within the Pt heaters and the suspended Si membrane.

The membranes under study are plain p-type membrane of length equal to 60μm and width 10μm and plain n-type membrane of length equal to 20μm and width equal to 20μm. Figure 4-16-a illustrates the configuration of the experimental setup employed for Transient thermo-reflectance. The TTR experiment was conducted systematically with the following steps: Firstly, the focus zone was carefully chosen for accurate measurements. Subsequently, the TTR signal reference was obtained by employing a laser beam with a x20 magnification lens. Following this, probes were positioned as depicted in Figure 4-16-b, and heater 1 was subjected to biasing using a voltage range ranging from 2.5V to 10V, with a step size of 2.5V, mimicking the approach used in Seebeck measurement experiments. The acquired TTR signal was then captured and processed using SanjAnalyser, a software tool specialized for data analysis in TTR experiments. SanjAnalyser assists in signal processing, data visualization, and

temperature profile extraction. Lastly, the temperature difference across both the membrane and the Pt heaters was determined individually. This determination was made by considering the wavelength used for measurement (530nm for Pt and 365nm for Si) and the Coefficient of Transient Reflectance (CTR) applied within the SanjAnalyser software.

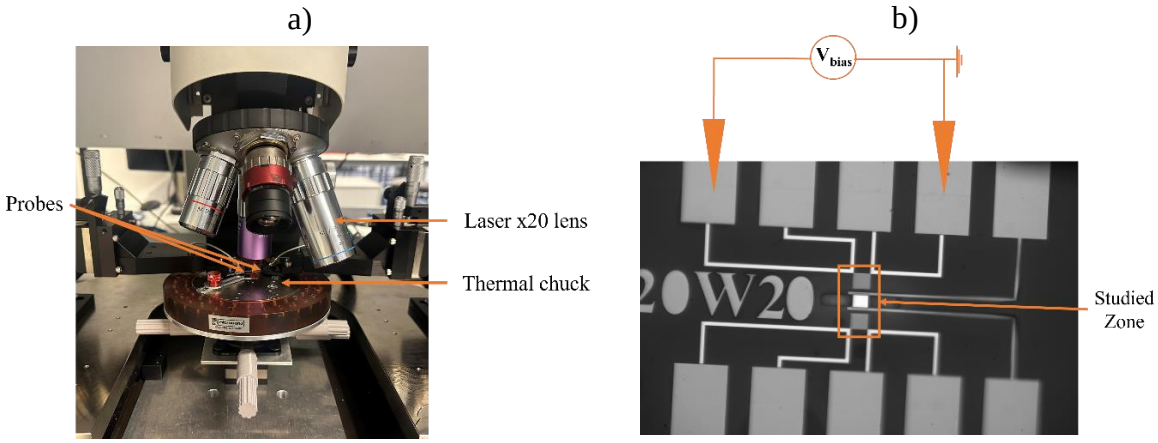
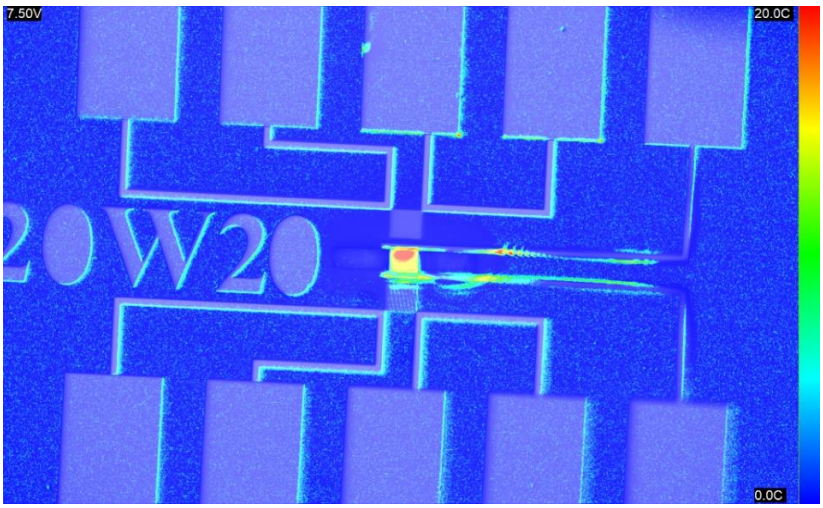


Figure 4-16: (a) Experimental Setup Configuration for Transient Thermo-Reflectance (TTR) Measurement. (b) A Reference Image via TTR, Demonstrating Probe Placement for Voltage Bias.

For the suspended n-type membrane, measuring 20µm in length and 20µm in width, the average temperature difference (ΔT_H) of Pt heater 1 was determined to be 16.21K. This measurement was conducted using a wavelength of 530nm and a CTR of 1.2×10^{-4} K^{-1} while applying a bias voltage of 7.5V to heater 1. Notably, this temperature closely approximated the temperature difference observed across the suspended Si membrane (ΔT_m) under the same bias voltage. In the case of the Si membrane, a wavelength of 365nm was employed for measurement, along with a CTR value of $1.37\times10^{-4}K^{-1}$, yielding a temperature difference of 15.93K. Remarkably, this determined temperature difference across the Si membrane through TTR closely mirrored the temperature difference determined through electrical measurement during the Seebeck coefficient measurement, which was recorded at 15.20K. Figure 4-17 illustrates Thermal Transient Reflectance (TTR) images of an n-type Si plain membrane with dimensions (L=20µm, W=20µm) subjected to a voltage bias of 7.5V. The figure presents two scenarios: a) employing a 530 nm wavelength with a Pt Coefficient of Thermal Reflectance of 1.2×10^{-4} K^{-1}, and b) utilizing a 365 nm wavelength with a Si CTR of 1.37×10^{-4} K^{-1}. Additionally, (c,d) depict TTR images of a Si plain membrane with dimensions (L=60µm, W=10µm) under a voltage bias of c) 2.5V and d) 5V, both using a 365 nm wavelength and a Si CTR of 1.37×10^{-4} K^{-1}.

a)



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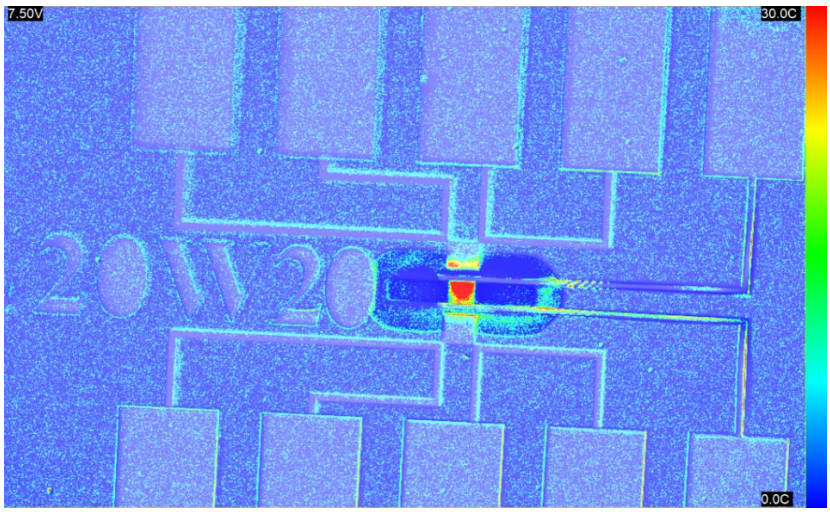
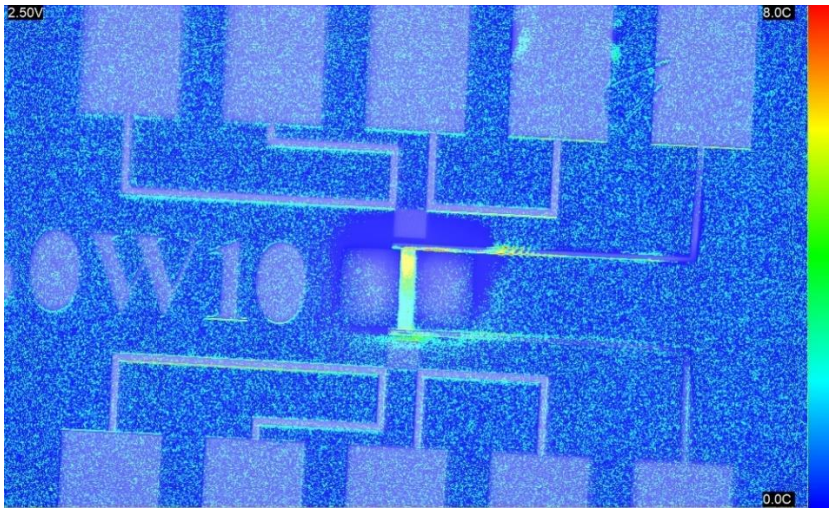


c)



d)

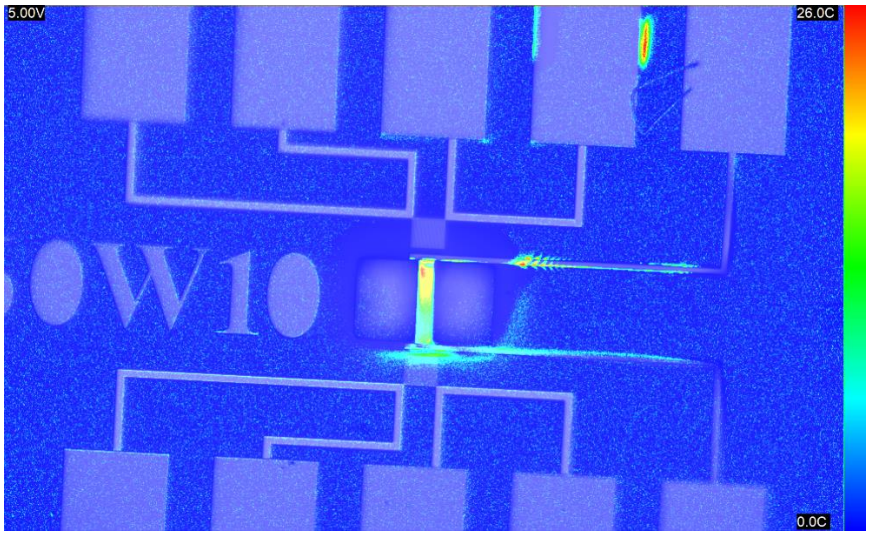


Figure 4-17: Thermal Transient Reflectance (TTR) images of n-type Si plain membranes under various conditions. (a,b) Showcases (L=20µm, W=20µm) membranes under a 7.5V voltage bias, with (a) employing a 530 nm wavelength and Pt Coefficient of Thermal Reflectance (CTR) of 1.2×10^{-4} K^{-1}, and (b) using a 365 nm wavelength with Si CTR of 1.37×10^{-4} K^{-1}. In (c,d), TTR images for (L=60µm, W=10µm) membranes under voltage biases of (c) 2.5V and (d) 5V, both utilizing a 365 nm wavelength and Si CTR of 1.37×10^{-4} K^{-1}.

The temperature difference (ΔT_m) observed across the suspended plain Si membrane through both electrical and thermal measurements are nearly identical (Figure 4-18), validating the accuracy of the previously determined Seebeck coefficient. Any minor discrepancies between the thermal and electrical measurements may be attributed to potential measurement errors in both the Coefficient of Thermal Reflectance (CTR) and Thermal Coefficient of Resistance (TCR) values for silicon.

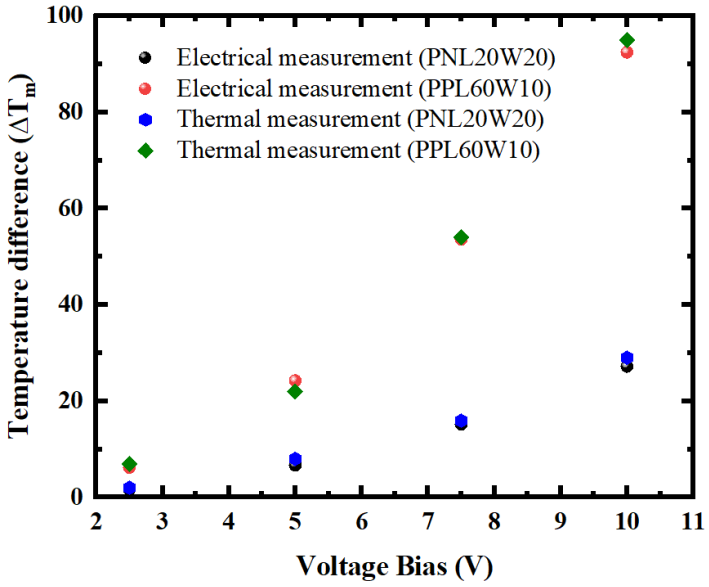


Figure 4-18: Temperature difference as a function of voltage bias for PNL20W20 and PPL60W10 Samples: Comparison of electrical and thermal measurement techniques.

4.2 Doping level / Electrical conductivity measurements

In this section, our primary focus is on characterizing the electrical conductivity, which represents the second thermoelectric transport property discussed in this chapter. This characterization covers both phononic and non-phononic devices, taking into account their distinct p-type or n-type characteristics. Our approach initiates by introducing the fundamental principles of the measurement protocol used to determine the electrical conductivity. Subsequently, we delve into a comprehensive analysis of the measurement conditions employed throughout the experimental investigations.

4.2.1 Measurement protocol

4.2.1.1 Principle

The measurement of electrical conductivity is carried out using the widely adopted "Van Der Pauw (VDP)" method. This method, introduced by Van Der Pauw in 1958 [95] and further developed by Ramadan et al. in 1994 [96], is commonly used for determining the resistivity and Hall coefficient of a sample. One of the key advantages of this method is its ability to measure the average conductivity of samples with arbitrary shapes, as it approximates a two-dimensional geometry by employing four probes positioned along the sample's perimeter. However, to ensure accurate measurements using the VDP method, certain conditions must be met, including a flat and uniformly thick sample shape, absence of isolated holes, homogeneity and symmetry of the sample, and precise placement of electrical contacts at the sample's edge in a symmetrical arrangement (Figure 4-19).

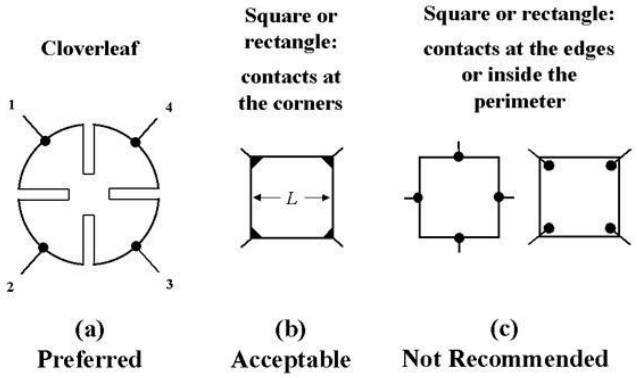


Figure 4-19: Samples' choice for VDP electrical conductivity measurements

The Van der Pauw (VDP) measurement principle involves placing four contacts (numbered from 1 to 4) at arbitrary positions on the sample (Figure 4-19 a). By applying a direct current (I_{14}) from contact 1 to 4, the potential difference (V_{43}) at the other two contacts is measured to determine the sample's "vertical" resistance (R_V) using the equation $R_V = V_{43}/I_{12} = V_{12}/I_{43}$. Similarly, the sample's "horizontal" resistance (R_H) is defined as $R_H = V_{23}/I_{14} = V_{14}/I_{23}$.

The electrical resistivity of the sample is determined based on the Van der Pauw theorem, which states that there exists a relationship between R_V and R_H. This relationship can be expressed as:

$$\exp\left(-\frac{\pi.t}{\rho}.R_V\right) + \exp\left(-\frac{\pi.t}{\rho}.R_H\right) = 1$$

Equation 4- 11

Where t is the sample's thickness and ρ [Ω.cm] is its electrical resistivity. The resolution of this equation is straightforward if the sample possesses a symmetrical shape, and the contacts are arranged symmetrically (Figure 4-19 a or b). In this case, the contacts and resistances are all equivalent, and the electrical resistivity can be defined as:

$$\rho = \frac{\pi . t}{\ln (2)} \, R_V = \frac{\pi . t}{\ln (2)} \, R_H$$

Equation 4- 12

However, if the sample is not symmetrical or the contacts are arranged arbitrarily, solving Equation 4- 11 becomes more challenging. In such cases, the electrical resistivity can be approximated as:

$$\rho = \frac{\pi . t}{\ln (2)} \times \frac{R_V + R_H}{2} \times F \times (Q)$$

Equation 4- 13

Where Q and F are the symmetry and correction factors respectively. F is a correction factor for geometrical asymmetry and not for material anisotropy or inhomogeneity. It is a function of the symmetry factor Q, defined as:

$$Q = \frac{R_V}{R_H}$$

Equation 4- 14

F is normally obtained by reference to graphs. However, if the asymmetry is not too large (Q<10), the following approximation can be used:

$$F = 1 - 0.34657A - 0.09236A^2$$

Equation 4- 15

Where:

$$A = [\frac{R_V - R_H}{R_V + R_H}]^2 = [\frac{Q - 1}{Q + 1}]^2$$

Equation 4- 16

It is important to note that the electrical resistivity obtained in this condition is less accurate, emphasizing the importance of designing a symmetrical measurement platform and arranging the contacts symmetrically (Figure 4-19 a or b) whenever possible.

4.2.1.2 Characterization conditions

The electrical measurements are conducted using the HL5500PC, a fully integrated Hall Effect Measurement System. This system is designed to deliver accurate and reliable measurements of important parameters such as resistivity, carrier concentration, and mobility in semiconductor materials. It serves as a comprehensive tool for researchers and engineers to characterize the electrical properties of diverse semiconductor samples. The HL5500PC is capable of accommodating various sample geometries, including the widely used Van der Pauw, bar, and bridge shapes. This versatility enables measurements on different types of samples, accommodating the specific requirements and preparation techniques employed in research.

The measurements are performed on a "cloverleaf" architecture platform, as shown in Figure 4-19-a. The layer of interest is positioned at the center of the platform, while the electrical contacts are symmetrically arranged at the extremities. This arrangement ensures accurate and reliable measurements, minimizing any potential asymmetry or bias introduced during the measurement process (as discussed in Section 4.2.1.1).

In the experimental setup, the sample is centrally positioned within a PTFE sample holder, and the four probes are carefully placed onto the corresponding contact positions on the sample (Figure 4-20-b). Before proceeding with the measurement of resistivity and Hall coefficient, it is essential to ensure the quality of the electrical contacts. This is achieved by measuring the resistance between each pair of probes (R_{12}, R_{23}, R_{34}, R_{41}, R_{13}, R_{24}) and by generating I-V curves between contacts 12 and 34. The measurement platform and configurations used for this process are illustrated in Figure 4-20-a.

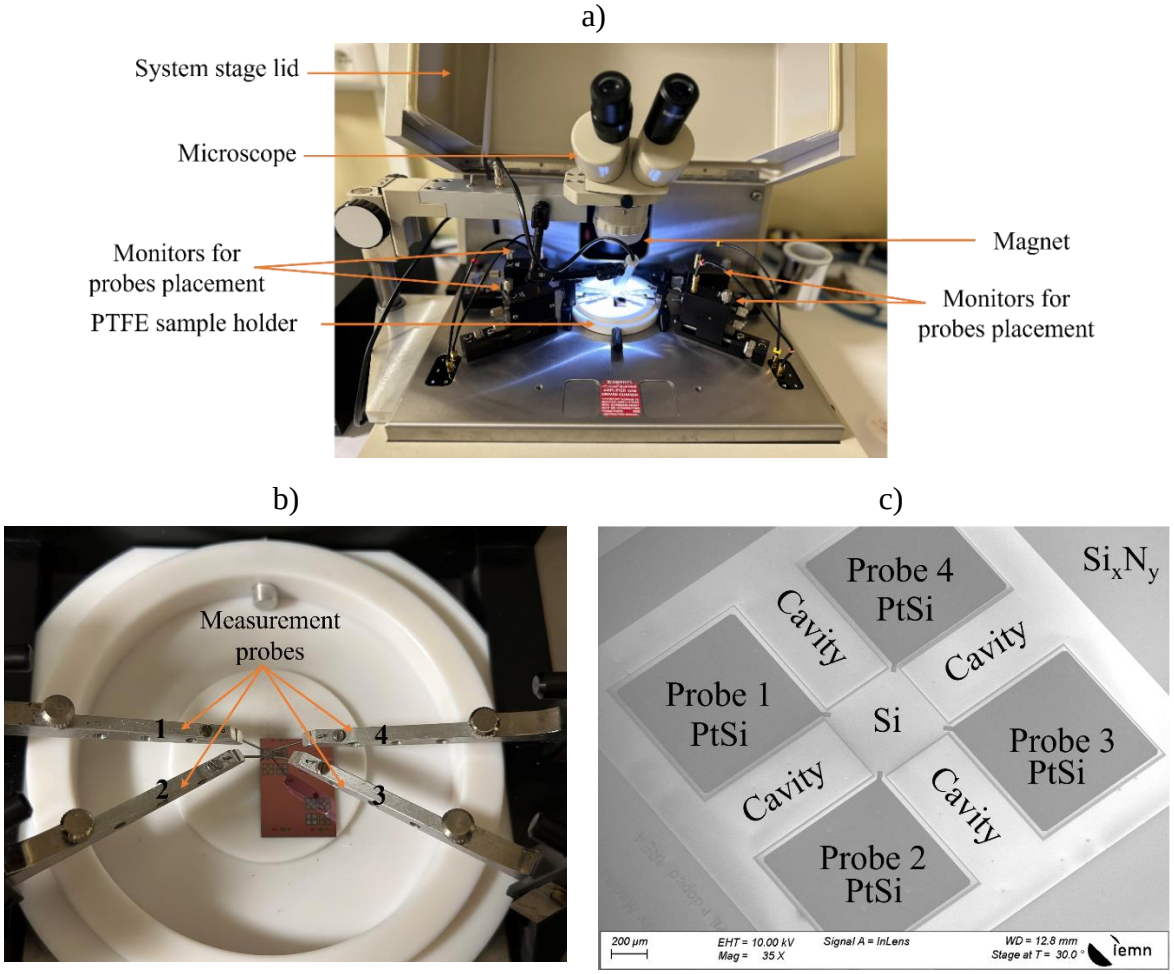


Figure 4-20: The setup used for electrical resistivity measurements, a) the platform used for characterizations, b) a close-up view of the probes positioned on the sample, c) SEM image of the VDP structure, emphasizing the positioning of the probes for the measurements.

In the HL5500PC, the resistivity will be measured with the same value of the constant current I for all six possible permutations. Also, the voltages V_{XY} are measured for both current directions and averaged in order to cancel thermoelectric effect and other effects.

For the Hall effect measurement, a constant current I is injected at two non-adjacent contacts and the difference in potential measured across the remaining two contacts, for a

constant magnetic field B perpendicular to the sample surface. The Figure 4-21 illustrates the general Van Der Pauw arrangement for measuring the Hall effect in semiconductors.

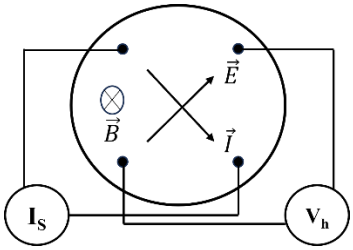


Figure 4-21: Generalized Hall effect arrangement.

The Hall coefficient, denoted as R_H [m^3/C], plays a crucial role in characterizing the electrical properties of a conductive sample with a parallelepiped shape. It quantitatively relates the Hall voltage (V_H) to the applied magnetic field strength (B) and current density (I) in the sample. The Hall voltage V_H is generated orthogonally to both the direction of the current and the magnetic field. Mathematically, it can be expressed as:

$$V_H = \frac{R_H \times B \times I}{t}$$

Equation 4- 17

Where, t represents the thickness of the sample. Because the contacts have a finite size, an additional voltage measurement is carried out, with no applied magnetic field, to determine the voltage drop due to a misalignment of the contacts. This quantity is then zeroed from the Hall voltage during a Hall effect measurement, thereby increasing the sensitivity of the instrument. The Hall coefficient is computed from Equation 4- 13 for an average value of V_H. This average is based on the V_H values measured for all possible permutations of contacts, current and magnetic field directions.

The carrier density (N) of the sample can be determined using the measured Hall coefficient (R_H). In the case of VDP method, the relationship between carrier density and Hall coefficient is given by:

$$N = \frac{1}{q.R_H} \ [cm^{-3}]$$

Where q is the elementary charge of an electron or hole. Additional information regarding the software utilized for this measurement can be found in Appendix 2.

4.2.2 Doping level / Electrical conductivity measurements results

In this section, we will present the results obtained from the characterization of plain membranes, encompassing both p-type and n-type membranes. These membranes were subjected to the measurement methodology described earlier (section 4.2.1.2) and shown in Figure 4-20. However, it is important to note that due to certain limitations, such as the detachment of PtSi contacts from the phononic silicon layer during the HF vapor step as shown in Figure 4-22, the results presented here will only pertain to the plain membranes. Regrettably, it was not feasible to fabricate new samples within the given time frame, as the total fabrication process typically takes around 6 to 8 weeks.

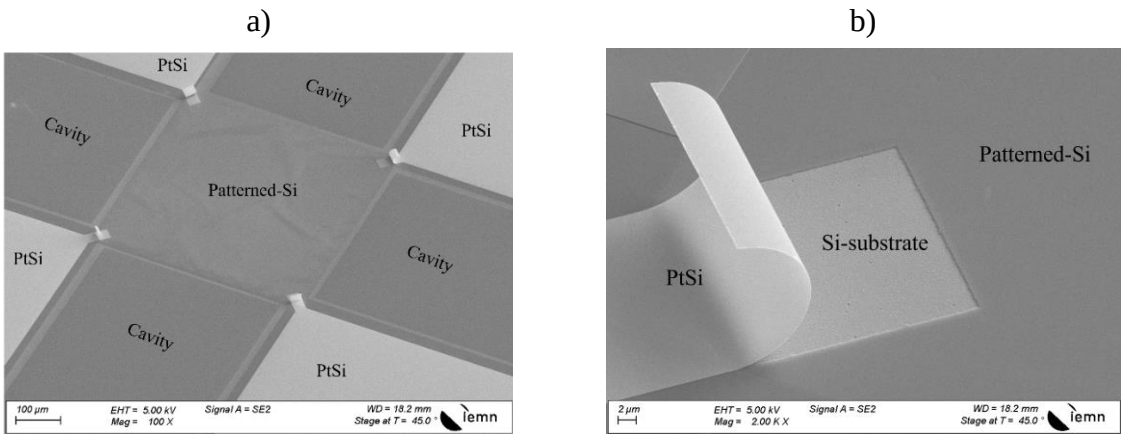


Figure 4-22: SEM images of a) Vander Pauw structures for patterned Si and b) a close-up view on the detached contact from the membrane.

The designed and fabricated chip in our study includes four distinct structures dedicated to measuring the electrical resistivity of p-type and n-type membranes, both plain and phononic-engineered (PE). Each of these four combinations is replicated twice on the same chip, providing dual measurements for enhanced accuracy. Furthermore, our 3 inches wafer contains 2 chips that include the electrical measurement devices. To ensure consistency and reliability in our measurements, the doping level of each membrane configuration was carefully determined. The mean values of the four devices within each configuration were calculated, and the associated standard error was taken into account. These results are presented in Table 4-2, which displays the mean doping level values for the plain p-type and plain n-type membranes.

Additionally, Table 4-2 provides the electrical resistivity and electrical conductivity values for the 60nm thick plain p-type and n-type membranes, including the standard error values of each parameter, accounting for the uncertainties associated with the measurements. These values are crucial in understanding the transport properties of the membranes and determination of the *zT* analytical figure of merit.

Table 4-2: The electrical resistivity, electrical conductivity and doping level of plain p-type and n-type membranes.

	Carriers concentration [cm^{-3}]	Electrical resistivity [Ω.cm]	Electrical conductivity [S.cm]
Plain p-type membranes	$1.2.10^{19} \pm 0.7\%$	$0.01 \pm 0.5\%$	$100.8 \pm 0.5\%$
Plain n-type membranes	$7.2.10^{18} \pm 1\%$	$0.007 \pm 0.5\%$	$131.8 \pm 0.5\%$

The choice of a doping level of 10^{19} cm^{-3} was based on optimizing the figure of merit (*zT*), as discussed in Chapter 1. This particular doping level was identified as the most favorable for achieving high thermoelectric performance in the membranes, balancing carrier concentration and mobility to enhance thermoelectric efficiency.

4.3 Thermal conductivity measurements

In recent decades, various methodologies have been developed for measuring thermal conductivity, including specific techniques for nanodevices. However, many experimental techniques encounter challenges related to the use of metallic layers for temperature probes, which can lead to heat losses at the interfaces. Techniques such as Direct Current (DC)[97][98] and 3ω methods[99][100], Time Domain Thermo Reflectance (TDTR)[101], and Scanning Thermal Microscopy (SThM)[102][103] heavily rely on metallic probes and interface properties. The latter technique also requires precise knowledge of probe tip geometry and thermal properties, necessitating accurate Finite Element Method (FEM) analysis. In contrast, our laboratory employs a contactless micro-Raman thermometry (μRT)[104][105][106] technique, which offers advantages by directly heating the membrane through light absorption. This technique offers several advantages, including direct heating of the membrane through light absorption, eliminating the need for metallic probes and reducing interface-related uncertainties. The μRT technique enables accurate measurements with a simple experimental configuration, as the temperature is directly proportional to the Raman shift. When combined with the free-standing beam-like (FSBL) topology of the membrane, it facilitates straightforward measurements of the thermal conductivity. However, it is important to note that the accuracy of μRT relies on precise estimation of absorption, which requires reliable simulations and refractive index values from the literature.

In the following section, we focus on characterizing the thermal conductivity, which is the third and last thermoelectric transport parameter to be determined. We describe the experimental setup used for thermal conductivity measurements, including the characterization conditions. These measurements cover both phononic and non-phononic devices, specifically targeting p-type Si membranes. The obtained results from these measurements are presented and thoroughly analyzed.

4.3.1 Measurement protocol

4.3.1.1 Principle

Micro Raman thermometry is a characterization method that utilizes Raman spectroscopy to determine the thermal conductivity of membranes. It operates based on the principle of Raman scattering, where monochromatic light is inelastically scattered. By applying an incident laser beam (Figure 4-23), the suspended membrane is heated, leading to the establishment of a steady-state heat flow and the formation of a temperature gradient. This gradient is influenced by the specific geometry, structural conditions, and convective effects of the sample configuration.

To establish the relationship between absorbed power (P_{abs}), temperature at the heating spot (T_0), and thermal conductivity (κ), the heat equation can be solved either analytically or numerically. The determination of P_{abs} involves evaluating the absorption (A), which can be obtained through parallel transmission and reflection measurements conducted alongside the micro-Raman thermometry setup (μRT). Alternatively, a numerical correction can be applied to the literature dielectric constant to estimate the absorption. Additionally, detecting the transmitted beam power enhances the reliability of the experimental measurements, as it allows for the quantification of absorbed radiation. However, the inherent free-standing beam-like topology of fabricated membranes poses challenges in accessing the bottoms of the cavities, necessitating analytical estimation of absorption values.

In the scenario of a large-scale membrane being heated by a laser in a vacuum, the 2D radial heat propagation can be described using a modified form of Fourier's law, as represented by Equation 4- 18, where *t* is the thickness.

$$\frac{P_{abs}}{2\pi rt} = -\kappa \nabla T$$

Equation 4- 18

To enhance the accuracy of the measurements, it is advisable to calculate multiple ΔT_0 points. These can be determined by either varying P_{abs} while keeping the location constant or varying the position while maintaining a constant temperature. This comprehensive approach enables a more precise characterization of the thermal conductivity of the membranes under investigation, contributing to a thorough understanding of their thermoelectric properties.

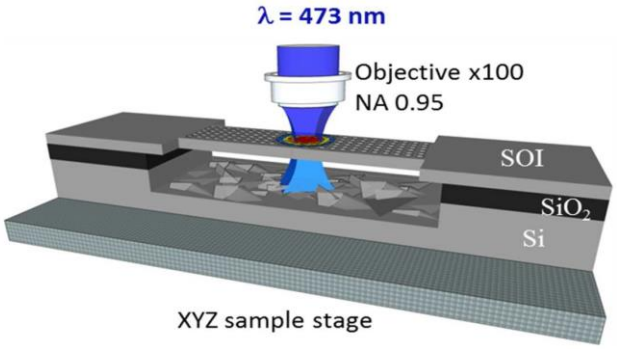


Figure 4-23: Schematic representation of the phononic membrane measurement process of the μRT experiment utilizing one laser source[106][5].

4.3.1.2 Characterization conditions

We employed Raman thermometry methodology to investigate and determine the thermal conductivity of our suspended membranes. The membranes under study are exclusively p-type and come in two configurations: plain membranes and phononic membranes. These membranes vary in terms of their width and length. Figure 4-24-a illustrates the configuration of the experimental setup employed for micro-Raman thermometry. The setup includes several components, namely a vacuum chamber, instruments for temperature and vacuum measurements), a microscope objective and a power meter for measuring the incident power. In addition, Figure 4-24-c provides a schematic of a Raman microscope analogous to LabRAM HR confocal system from Horiba Jobin-Yvon72. This system utilizes a continuous-wave diode-pumped laser with a wavelength of 473.11 nm for the Raman measurements.

[5] Image courtesy of A. Massoud.

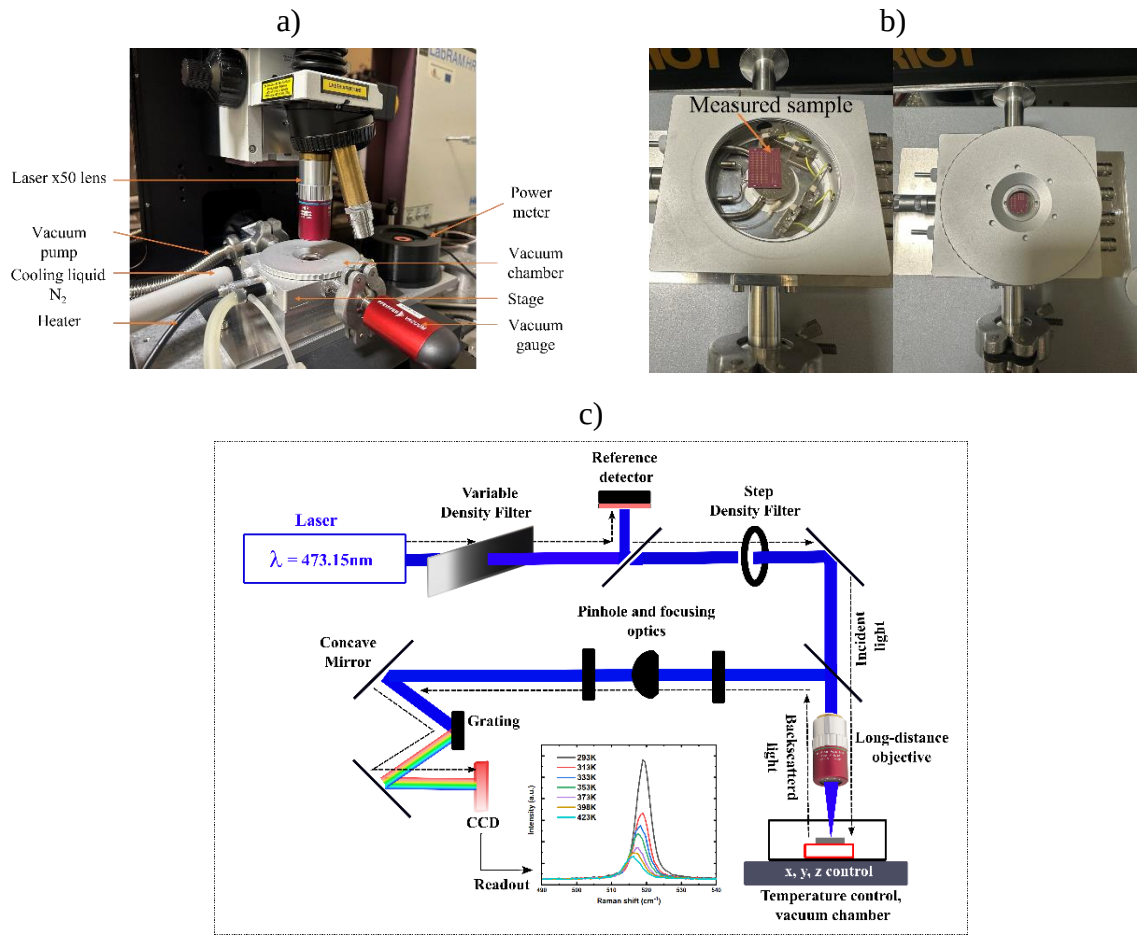


Figure 4-24: Experimental Setup for Micro Raman-Thermometry. a) The configuration of the experimental setup utilized for micro-Raman-thermometry. b) a close-up view of the measured sample within the vacuum chamber. c) a schematic of a Raman microscope analogous to LabRAM HR confocal system from Horiba Jobin-Yvon used with 473.11 nm continuous-wave diode-pumped laser (credited to Akash Patil).

In order to minimize convective heat losses, all measurements are conducted under a vacuum pressure of approximately 8.93×10^{-3}mbar. This vacuum environment helps prevent convective heat losses from the membrane and ensures that the absorbed heat remains localized within the membrane, enabling us to obtain precise and reliable measurements of thermal conductivity. In addition, the holder substrate is maintained at a constant temperature equal to room temperature (T=23°C) to obtain measurements of the thermal conductivity near room temperature. The laser beam used in the experiments has an initial power of $P_0 \approx 13$mW and a wavelength of 473.11nm. Two density filters, among which one is a linearly varying filter mounted on a translation are employed to attenuate the laser beam. The filters are characterized by their optical density number (OD), which is defined as the logarithm of the ratio of the initial power (P_0) to the incident power (P), with OD_R = [4, 3, 2, 1, 0.6, 0.3] for set-up and OD_C = [0.1, 0.5, ...] for changeable filters. Thus, by combining different OD_R and OD_C values, various incident powers can be achieved. The beam is focused with a lens x (NA= 0.42, r_0=0.69μm, where r_0 is a theoretical beam radius at a focal plane). To determine the actual size of the laser beam when using the x50 lens, we referred to the work conducted by S. Didenko *et al.*[107] , who employed the commonly used knife method. According to their findings, the real laser beam size was measured to be 1.5µm.

The Raman thermometry characterization measurements methodology involves three key steps: 1) Variation of Raman Shift with Absorbed Power, 2) Variation of Raman Shift with Temperature, 3) Correlation between Raman Shift and Temperature Difference.

4.3.1.2.1 Variation of Raman Shift with Absorbed Power

In this step of the Raman thermometry measurement methodology, the primary focus is on investigating the relationship between the Raman shift and different absorbed powers. To achieve this, the incident power directed onto the sample is deliberately varied in a systematic manner. Starting from an initial power level of 0.2mW, the incident power is incrementally increased with a step size of 0.2mW until it reaches a maximum value of 1mW. At each power level, the resulting Raman shift is measured and carefully recorded. This step helps establish the relationship between absorbed power and the resulting change in the Raman shift. Figure 4-25-a displays the characteristic Lorentz distributions obtained from measurements on a plain p-type Si membrane with dimensions of 20µm in length and 10µm in width for an incident power levels equal to 0.2mW.

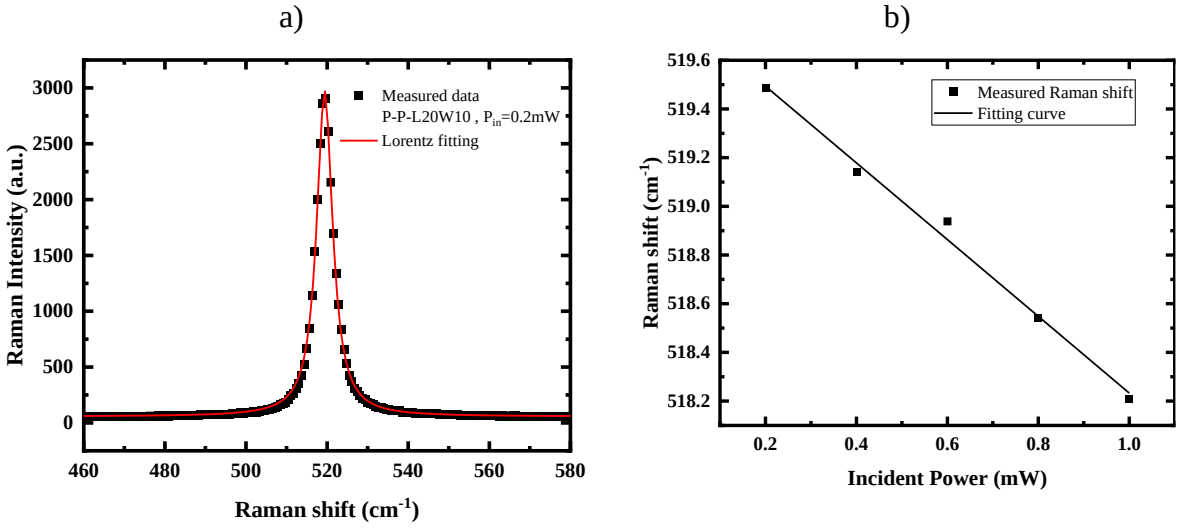


Figure 4-25: a) the characteristic Lorentz distributions obtained from measurements on a plain p-type Si membrane with dimensions of 20µm in length and 10µm in width for an incident power levels equal to 0.2mW. b) Variation of Raman shift as a function of the incident power of a p-type plain membrane, t=60nm, L=20µm, W=10µm.

The Raman shift peak exhibits a linear relationship with the absorbed power, where the slope of this relationship provides information about the variation of the Raman shift with absorbed power. For the p-type plain membrane (measuring 60µm in length and 10µm in width), the calculated slope is determined to be $\partial\omega/\partial P|_{T=300K}$ = -1.576 cm^{-1}/mW. By dividing this variation by the change in the Raman shift with temperature (which will be discussed in the upcoming section), it becomes possible to ascertain the variation of temperature with absorbed power ($\partial T/\partial P$) (Figure 4-26-b). The subsequent section focuses on investigating the relationship between the Raman shift and temperature.

4.3.1.2.2 Variation of Raman Shift with Temperature

The fundamental work conducted by M. Balkanski *et al.* [108] focused on investigating the cubic and quadratic contributions of anharmonic effects on the Raman shift and the optical (LO) phonon. The approach employed in their study is based on the Klemens model [109], which takes into account three and four anharmonic phonon interactions. This comprehensive

approach ensures accurate treatment and alignment with experimental results, particularly at high temperatures ranging from 800 K to 1400 K (as depicted in Figure 4-26). The research demonstrated that both the Raman shift (Δ) and damping constant (Γ) exhibit temperature dependencies that can be expressed as sums of cubic, quadratic, and higher-order terms in the anharmonic Hamiltonian (Equation 4- 19).

$$\Gamma = \mathrm{A}(1 + \frac{2}{e^{x} - 1}) + B(1 + \frac{3}{e^{y} - 1} + \frac{3}{(e^{y} - 1)^{2}})$$

Equation 4- 19

Where $x=\hbar\omega_0/2k_BT$, $=\hbar\omega_0/3k_BT$, A= 1.295 and B = 0.105 (anharmonic constants from [108] [110]).

Another approach to express the anharmonicity is by deriving the Raman shift Ω(T) as a function of contributions from three and four phonon processes. These processes exhibit analogous temperature dependencies (Equation 4- 20).

$$\Omega(T) = \omega_0 + \Delta(T)$$

Equation 4- 20

With

$$\Delta(T) = C\left(1 + \frac{2}{e^{x} - 1}\right) + D(1 + \frac{3}{e^{y} - 1} + \frac{3}{(e^{y} - 1)^{2}})$$

Equation 4- 21

With ω_0 is the shift at 0K, equals to 528 cm^{-1}, C and D are constants with the values -2.96 cm^{-1} and -0.174 cm^{-1}, respectively. Also, it is simplified: $x=\hbar\omega_0/2k_BT$, $=\hbar\omega_0/3k_BT$. The D terms represents the four phonons contribution which allows a better fitting at high temperatures.

The relationship between the Raman shift and temperature above room temperature is commonly characterized as linear. By expanding the expressions for thermal expansion and anharmonic phonon-phonon coupling, as described in references [108] and [111], and considering only the linear terms in a Taylor series, it is possible to derive the slope of this relationship.

$$\frac{d\omega}{dT} = -3\omega_0\gamma\alpha + \frac{k_B}{hc\omega_0}(4A + 9B)$$

Equation 4- 22

With γ is Grüneisen parameter, α the coefficient of linear thermal expansion, and A and B are the cubic and quartic anharmonic constants, respectively.

An alternative approach involves deriving Equation 4- 20 that relates the line position-shift to temperature. By taking the derivative of this equation with respect to temperature and substituting the value of room temperature (300 K), we can obtain the parameter $\chi_T = \partial\omega/\partial T|_{T=300K}$. Through our calculations, we determined that χ_T is equal to -0.022, which is consistent with previous reports and suggests agreement with existing literature on the topic.

a) b)

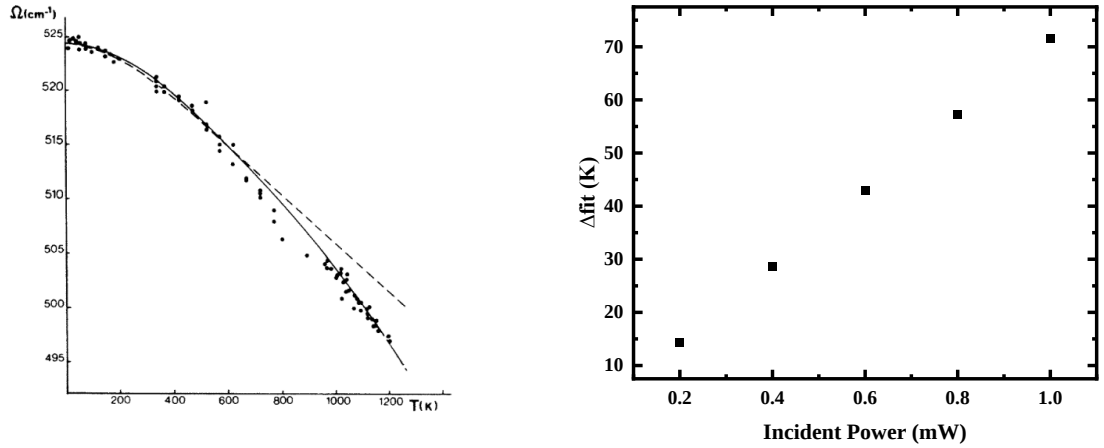


Figure 4-26:a) From Balkanski et al. [108], Raman shift as a function of temperature. The solid and dashed curves are model fit accounting for free- and four-phonon and only free-phonon processes respectively. Thick line is a guide to the eye highlighting the idea of linear approximation between 300K and 800K. b) The experimental temperature difference across the p-type membrane with t=60nm, L=60μm and W=10μm as a function of the incident power.

The presented Figure 4-26-a illustrates the fitting of the measured Raman shift as a function of temperature (T). In the temperature range from 300K to 800K, where the high-temperature limit is not exceeded, a linear fit is applied. This linear fit corresponds to a theoretical model that does not take into account the four-phonon contribution to anharmonicity. The linear fit closely approximates the experimental data, indicating that the Raman shift can be effectively utilized as a linear response to changes in temperature within this temperature range.

4.3.1.2.3 Correlation between Raman Shift and Temperature Difference

In this final step, the Raman shift is correlated with the temperature difference across the membrane. At this point, a Finite Element Method (FEM) model of the device under test is developed. The purpose of this model is to replicate the heat transport conditions observed in the experiments and analyze the thermal behavior of the system. In the FEM model, the thermal conductivity of the material is systematically adjusted to match the temperatures observed experimentally. This tuning process ensures that the simulated temperatures in the model align with the measured temperatures, allowing for accurate characterization of the material's thermal conductivity. To construct an appropriate FEM model, the absorption properties of the nanopatterned material need to be evaluated. Rigorous Coupled-Wave Analysis (RCWA) is employed to assess the absorption properties of the material.

i) Absorption estimation

As described in section 4.3.1.1, accurately modeling the heat transfer in the membrane requires precise knowledge of the absorbed heat, denoted as P_{abs}. This value can be estimated by measuring the power of the incident laser beam, P_{in}, and calculating the absorption coefficient, A, of the membrane: $P_{abs} = A.P_{in}$. During the experiment, the power of the laser beam was measured using a Si power meter.

The RCWA (Rigorous Coupled-Wave Analysis) method is employed to determine the absorption coefficients of both plain membranes and patterned membranes. This method is based on the principles of wave optics and provides a rigorous solution for the interaction of

electromagnetic waves with periodic structures. In RCWA, the incident electromagnetic field is decomposed into its constituent plane waves, and the diffraction and scattering phenomena are taken into account by solving Maxwell's equations. By analyzing the transmission and reflection coefficients of these plane waves, the absorption coefficients of the membranes can be calculated. The RCWA analysis was done by Etienne BLANDRE, assistant professor at Junia-ISEN/IEMN.

Figure 4-27 illustrates the absorption coefficient of plain membranes as a function of membrane thickness (Figure 4-27-a) using the RCWA method. Additionally, the absorption coefficient of a patterned membrane with a thickness of 60nm and a pitch of 100nm is shown as a function of the holes' diameter (Figure 4-27-b). The refractive index used in these calculations is obtained from Palik [112](n = 4.463 + i*0.0367).

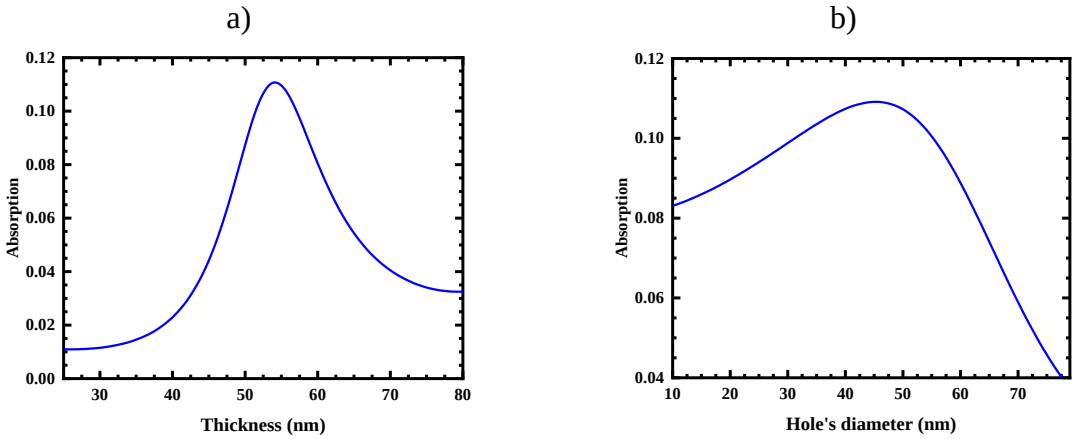


*Figure 4-27: RCWA absorption coefficient as a function of (a) thickness of plain membranes and (b) hole's diameter of a 60nm thick patterned membrane with a 100nm pitch. The calculations are based on the refractive index obtained from Palik (n=4.463+ i*0.0367).*

In order to determine the diameters of our patterned membranes, Scanning Electron Microscopy (SEM) images were analyzed, as shown in Figure 4-28. The diameter of the white shell rim around the holes corresponds to the largest diameter of the hole (top diameter), while the diameter of the dark area represents the bottom hole diameter. The truncated cone shape of the holes represents a significant improvement compared to previous work. For this study, the averaged diameter/radius, calculated by averaging the top- and bottom-hole diameters, will be used as a structural characteristic in the analysis of experimental data. The average diameter of our membrane is determined to be 45.95nm. As depicted in Figure 4-27-b, the absorption of a patterned membrane with diameters ranging from 45nm to 50nm exhibits similar behavior.

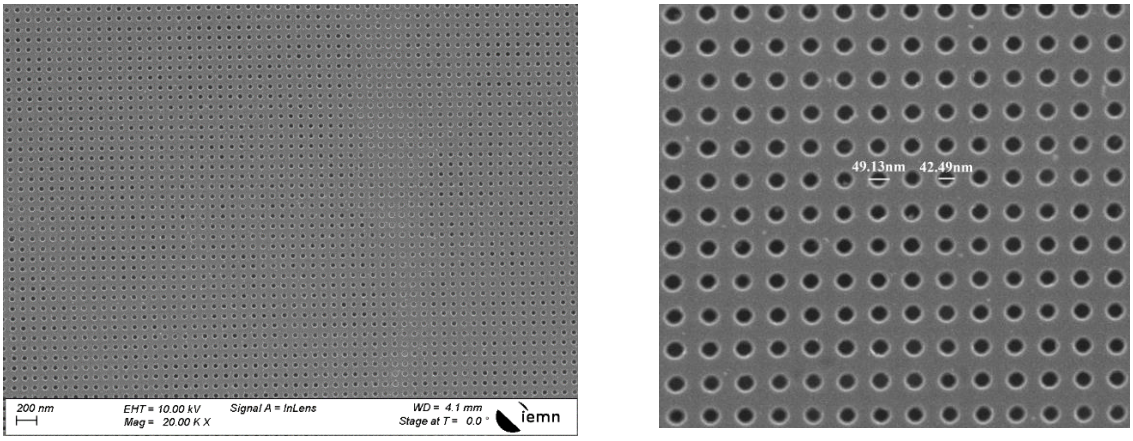


Figure 4-28: Scanning Electron Microscopy image of periodic patterned nano-holes in silicon.

ii) Finite Element Modelling

To gain a quick understanding of the problem, an electrical analogy is employed to model the heat transfer in the studied membranes. By considering zero convection and a simple slab-like geometry, the thermal resistance R[K/W] can be used to relate the temperature difference (ΔT) to the heat flux ($\Delta T = P_{abs}.R$), similar to how electrical resistance relates voltage to electrical current (U = IR). Figure 4-29-a represents this analogy for two parallel thermal resistors. The concept behind this analogy is that the heat paths from the laser hot spot (heat source spot) to the cold ends of the membrane (illustrated in Figure 4-29-b) can be regarded as two parallel resistors. The resistance of these paths varies with the position x of the laser spot:

$$R_{l/r} = \frac{R_k(\frac{L}{2} \pm x)}{wt}$$

Equation 4- 23

Where L, w and t are length, width, and thickness of the membrane slab respectively. R_k is thermal resistivity [Km/W].

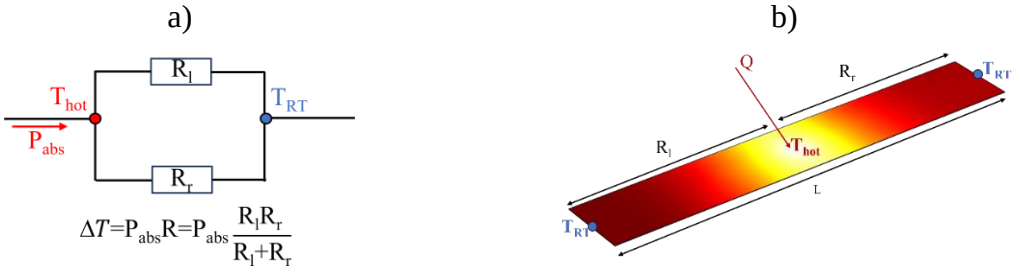


Figure 4-29: a) Electrical analogy of two thermal resistors that corresponds to the right and left paths. b) Plain Si membrane in the form of a slab with spots of laser heating at the center and room temperature heat-sink at the ends.

In this simplified model, the thermal conductivity can be generally expressed as [remark: ΔT(x) is a parabola (Figure 4-30); therefore, there is no parabolic dependence of κ vs. x, as it may seem in the formula].

$$\kappa = \frac{1}{R_k} = \frac{P_{abs}}{\Delta T(x)} \frac{L}{4wt} (1 - \frac{4x^2}{L^2})$$

Equation 4- 24

In our measurements, where the laser spot is positioned at the center of the membrane, the expression for the thermal conductivity is as follows:

$$\kappa = \frac{P_{abs}}{\Delta T}\frac{L}{4wt}$$

Equation 4- 25

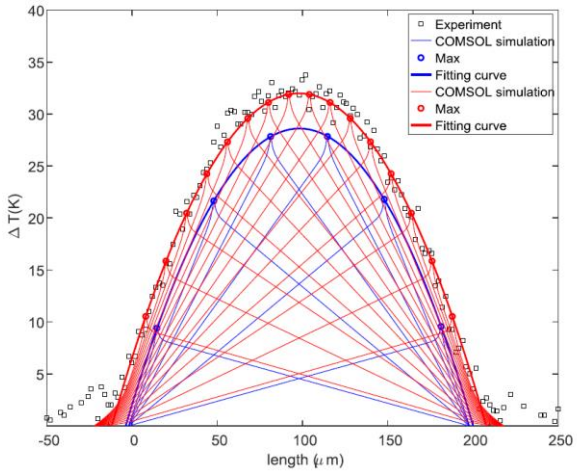


Figure 4-30: Temperature profiles (thin lines) in the Si plain membrane for parameterized laser spot positions (along the membrane length), calculated by COMSOL solver with the simple slab (blue) and device (red) geometries. Scatter points are profile's maximums, measured experimentally. Thick lines are second degree polynomials which are used to fit the maximums' points. Experimental data points of the profiles envelope were obtained by the Raman micro thermometry measurements[107].

In principle, Equation 4- 25 can be used to fit the thermal conductivity in both the T-profile method and P-variation methods when considering a simple slab geometry and a uniform heat source distribution in a vacuum. However, the actual device geometry is more complex, and the heat source distribution is non-uniform, following a Gaussian shape (Equation 4- 26) with a standard deviation σ = 1.5μm. This standard deviation value is obtained from S. Didenko [107] for a x50 lens.

$$P_{abs}(x,y) = \frac{AP_{in}}{2\pi\sigma^2}e^{\frac{-(x^2+y^2)}{2\sigma^2}}$$

Equation 4- 26

Taking into consideration the complex device geometry, the non-uniform heat source distribution, and the measured values of the standard deviation, a Finite Elements Model (FEM) was developed to simulate and analyze the thermal conductivity. This model incorporates the specific characteristics and parameters of the experimental setup, allowing for a more accurate representation of the heat transfer processes in the system. By utilizing the Comsol software, the model enables a comprehensive investigation of thermal conductivity under realistic conditions, providing valuable insights into the thermal behavior of the device.

The crucial aspect of the device geometry that significantly impacts heat propagation compared to the simple slab case is the presence of the SOI "wings." These wings are formed due to etching around the cavity, as depicted in Figure 4-31-a. They can be considered as extensions of the membrane. The width of the SOI wing, which is a critical parameter, has been determined through SEM analysis, as illustrated in Figure 4-31-b, and is measured to be 20μm. Additionally, it's important to consider also the SiN remaining on the sides of the membranes

and on top of the wings. The width of the SiN on the membrane's sides is 625nm, and its thermal conductivity is 1.55W/mK[6]. This dimension plays a crucial role in determining the heat transfer characteristics and should be taken into account for accurate modeling and analysis of the thermal behavior in the device.

a) b)

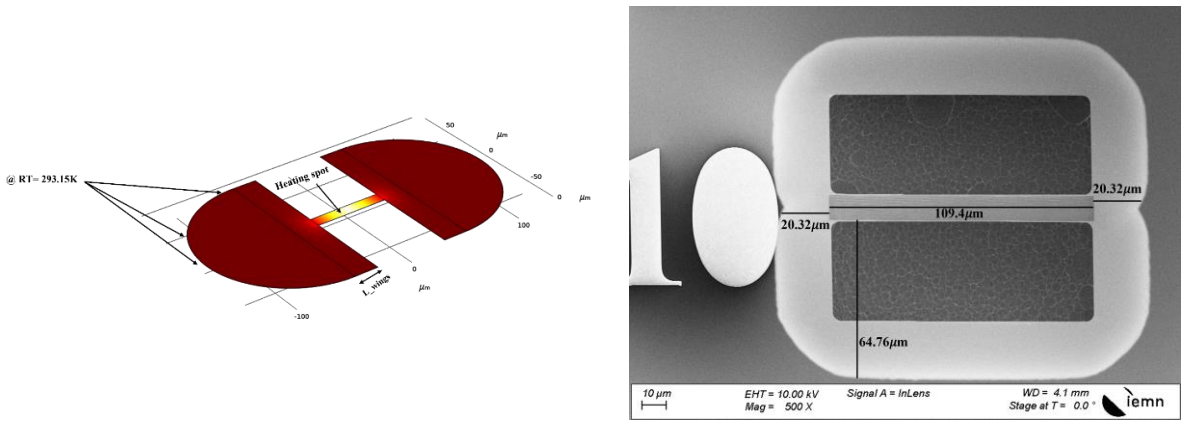


Figure 4-31: a) COMSOL model for thermal conductivity fitting using experiment geometry and Finite Element Model analyses for heat transfer. b) Scanning Electron Microscopy image of the suspended membrane, showcasing the width of the created wings.

Figure 4-32 illustrates the membrane model used for determining the thermal conductivity. Room temperature boundary conditions are imposed at the sides of the membrane. Figure 4-32-b displays the temperature profiles of heat propagation in the Si membrane, considering different thermal conductivity values, for various laser power levels incident at the middle of the membrane. The black data points represent the experimental μTR values obtained.

a) b)

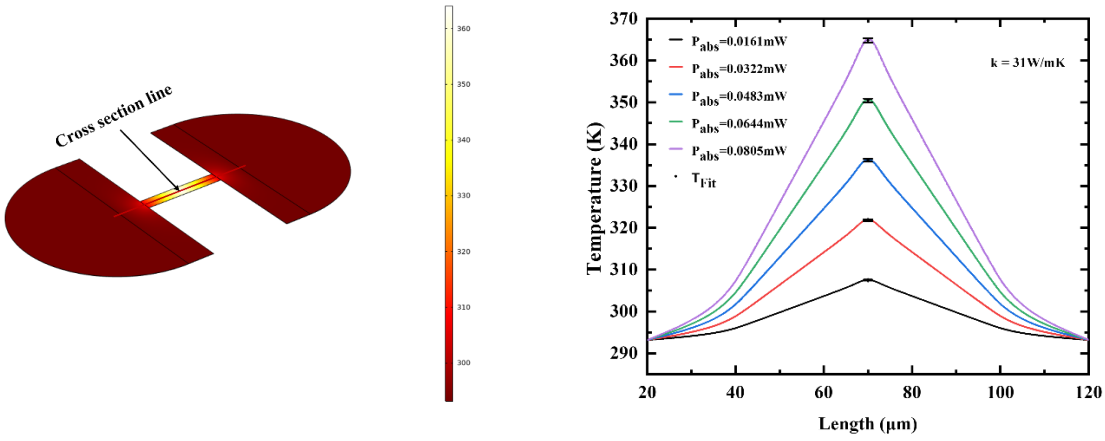


Figure 4-32: FEM modelling of Plain membrane, (a) Color maps of the temperature distribution in Si plain membrane established due to the heat absorption (P_{abs}=0.0805mW) at a hot spot at the center of the membrane. The red line is a cross-section along which the gradients are plotted (b) Simulated temperature profiles (solid lines) of the heat propagating in the Si plain membrane for parameterized power of the laser light incident into the middle of the membrane, and for different values of thermal

[6] Result achieved by Corentin Mercier, a PhD student within our research team.

conductivity. Black points are μTR experimental values. Membrane has the thickness t=60 nm, length = 60μm and width w = 10μm. Absorption A = 8.05%. Wings size of the device geometry equals 20μm.

The fitting of thermal conductivity relies on a temperature value obtained by considering the absorbed power. This temperature value is expressed as $T_{Comsol} = T(P_{abs}=0) + b * P_{abs}$, where the first term denotes the ambient temperature in the model, and the second term represents the temperature shift predicted from the absorbed power. By accounting for the rise in temperature caused by the absorbed power, this equation enables the estimation of thermal conductivity based on the corresponding temperature changes. The thermal conductivity is determined by fitting the maximum gradient at the center of the membrane, known as the hot spot position, to the experimental temperature values. In the case of a plain p-type membrane with a thickness of 60nm, the model fit yields an estimated thermal conductivity value of approximately 31W/mK.

4.3.2 Thermal conductivity measurements results

Measurements were performed on p-type membranes of varying lengths and widths, as well as different membrane types. The devices have been categorized based on their length, width, and membrane type, as outlined in Table 4-3. All these membranes have a uniform thickness of approximately 60nm.

Table 4-3: Device Labels and Corresponding Characteristics: Membrane Length, Width, and Type, All with a Uniform 60nm Thickness

Device label	Length (μm)	Width (μm)	Type of Si membrane
P-P-L20W10	20	10	Plain
P-P-L60W10	60	10	Plain
P-P-L100W10	100	10	Plain
PE-P-L20W10	20	10	Phononic
PE-P-L60W10	60	10	Phononic
PE-P-L100W10	100	10	Phononic
HPE-P-L20W10	20	10	Phononic with platform
HPE-P-L60W10	60	10	Phononic with platform
HPE-P-L100W10	100	10	Phononic with platform

The patterned membranes have an averaged diameter of 45.8nm with a pitch of 100nm. The plain p-type membranes demonstrate comparable thermal conductivity, indicating that the thermal conductivity is primarily influenced by the thickness rather than the length and width. Similarly, phononic membranes exhibit similar thermal conductivity across the different geometries. Figure 4-33 illustrates simulated temperature profiles (solid lines) for heat propagation in various silicon membranes. In Figure 4-33-a and Figure 4-33-b, we observe simulations on plain p-type Si membranes, exploring different thermal conductivity values and focusing on $\boldsymbol{\kappa}$=31W/mK, with laser power incident at the membrane center and an 8.05% absorption rate. Figure 4-33-c shifts to p-type Si phononic membranes, considering $\boldsymbol{\kappa}$=18W/mK, 10.9% absorption, hole diameter (45.8nm), pitch (100nm), and 20μm-sized wings

in the device geometry. Experimental μTR data points are marked in black, providing a basis for comparison. Membrane dimensions are uniform (t=60 nm, L=60μm, W=10μm).

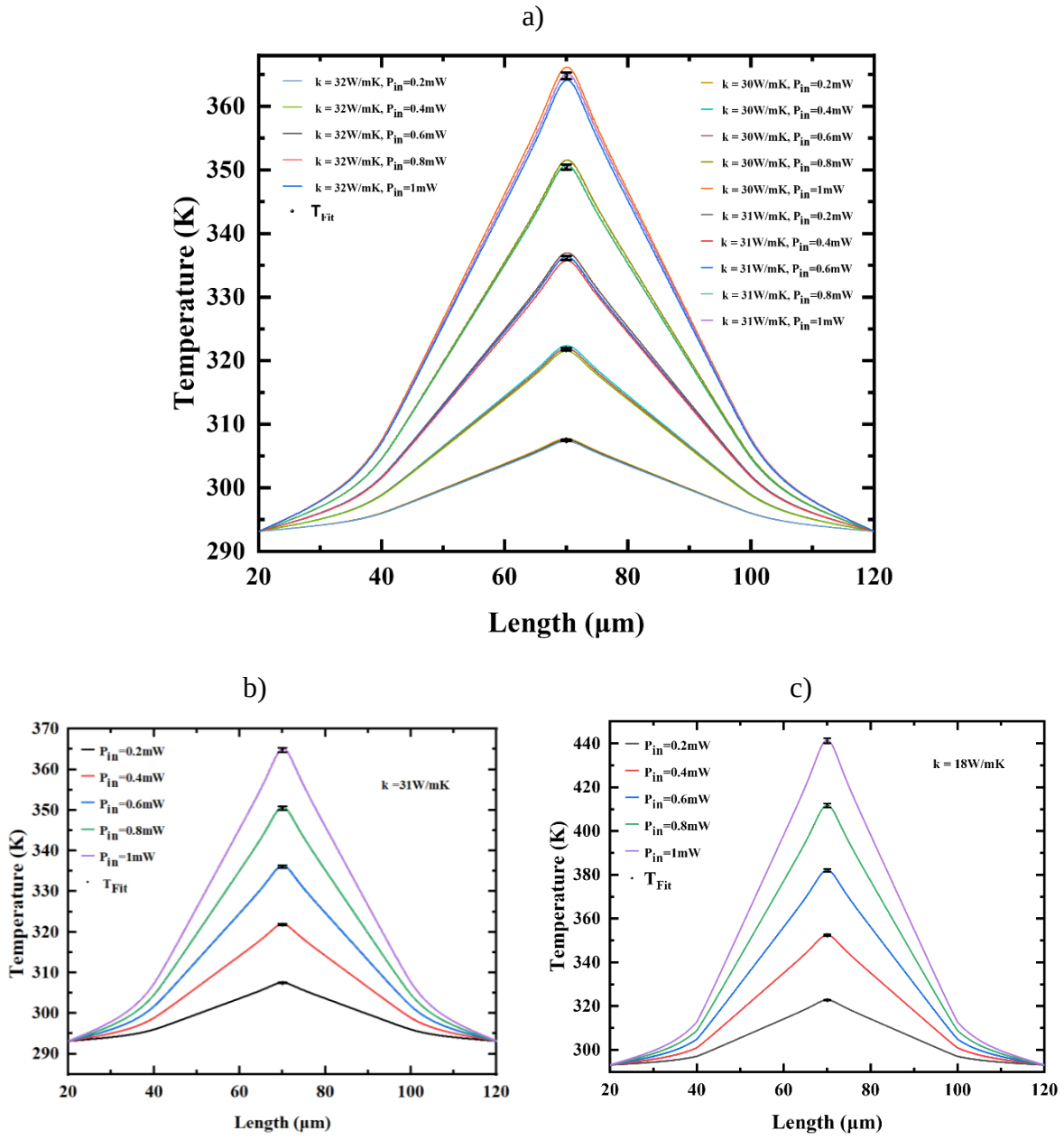


Figure 4-33: FEM-simulated temperature profiles (solid lines) of the heat propagating in the (a,b) p-type Si plain membrane for parameterized power of the laser light incident into the middle of the membrane, absorption A = 8.05%. (a) for different values of thermal conductivity (b) for κ=31W/mK. (c) p-type Si phononic membrane for parameterized power of the laser light incident into the middle of the membrane, κ=18W/mK, absorption A = 10.9%, hole's diameter 45.8nm and pitch = 100nm. Black points are μTR experimental values. Membrane has the thickness t=60 nm, L=60μm and W=10μm. Wings size of the device geometry equals 20μm.

In order to mitigate the phononic effect in the experimental setup, a new design of phononic membranes was implemented (Figure 4-34-a) referred to as HPE. This design involved incorporating a non-perforated platform at the center of the membrane with a diameter larger than the size of the incident laser beam. The purpose of this platform is to act as the focal

point for the laser beam during the P-variation measurement. By introducing a region without any perforations, it is expected that the influence of phononic interactions will be significantly reduced.

a) b)

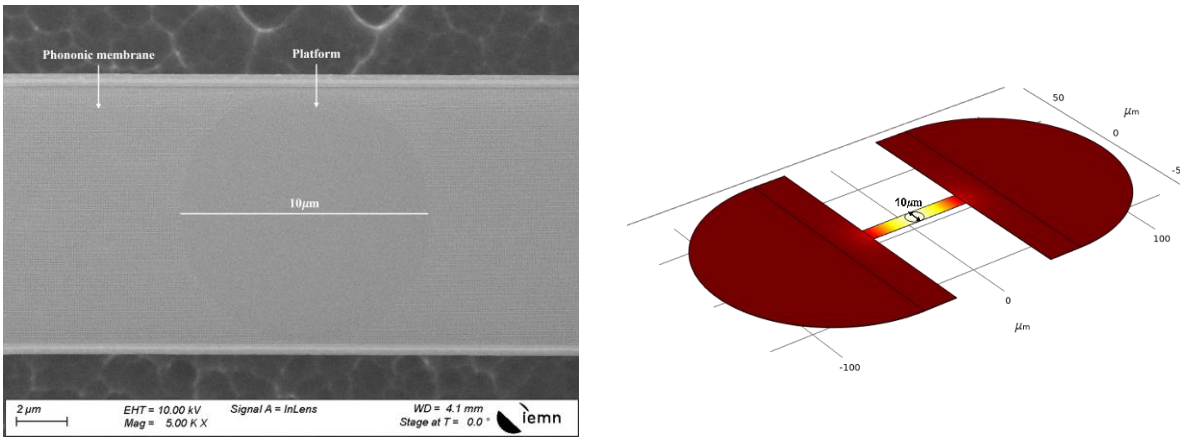


Figure 4-34: a) Scanning Electron Microscopy (SEM) image of a fabricated 60nm-thick Si Phononic membrane with a 100nm pitch and a plain 10μm diameter platform positioned at the center of the membrane. b) Finite Element Modeling (FEM) representation of the patterned membranes with an unpatterned diameter at the center (HPE) device, illustrating the contour of the platform.

Similar to the plain (P) and phononic membranes (PE), three different devices with distinct geometries were investigated: HPE-P-L20W10, HPE-P-L60W10, HPE-P-L20W10 and HPE-P-L100W10. These devices have a thickness of 60nm, with holes averaging a diameter of 45.8nm and a pitch of 100nm. The thermal conductivity determined using the HPE devices was found to be comparable to that determined using the phononic membranes (PE) as depict the Figure 4-35.

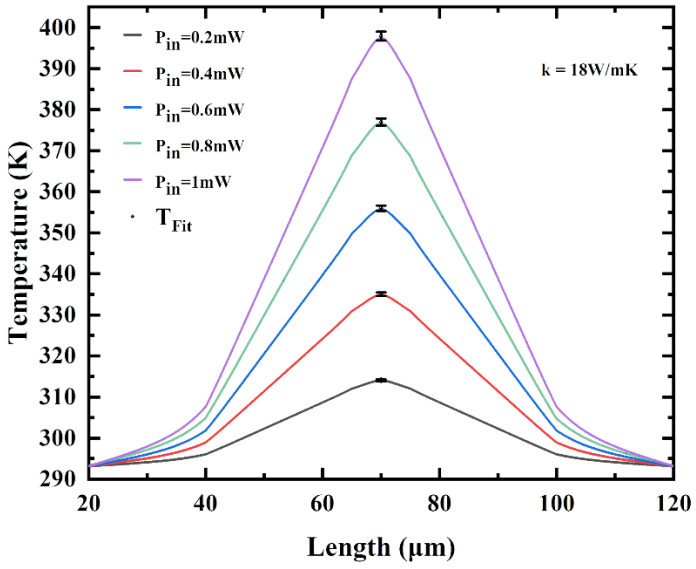


Figure 4-35: FEM-simulated temperature profiles (solid lines) of the heat propagating in the p-type Si phononic membrane with platform for parameterized power of the laser light incident into the middle of the platform, κ=18W/mK. Black points are μTR experimental values. Membrane has the thickness t=60 nm, L=60μm and W=10μm. Absorption A = 10.9%, hole's diameter 45.8nm and pitch = 100nm. Wings size of the device geometry equals 20μm.

Table 4-4 provides a comparison of different types of membranes with a thickness of 60nm: plain membrane (P), phononic membrane (PE), and phononic membrane with a platform (HPE). The phononic membranes feature holes with a diameter of 45.8nm and a pitch of 100nm. Additionally, the HPE membrane includes a platform with a diameter of 10µm.

One interesting finding from the table is that the thermal conductivity obtained using the platform at the center of the patterned membrane is equivalent to that of the patterned membrane without the platform. This suggests that the presence of the platform does not significantly impact the thermal conductivity of the phononic membrane. The thermal conductivity values for both the patterned membrane and the HPE membrane remain consistent, indicating that the platform does not introduce any noticeable thermal conductivity modifications in this specific configuration. Regarding the distinction between PE-P-L20W10 and HPE-P-L20W10, it's important to note that since the measurements are carried out on a single platform, we have concerns regarding its stability throughout the measurement process on PE-P-L20W10. Furthermore, when dealing with a larger membrane (L=100µm), the temperature at the membrane's center experiences a considerable increase (reaching 400K with a P_{abs} of 0.0436mW). This substantial temperature difference can potentially lead to an underestimation of thermal conductivity. It's essential to emphasize that the thermal conductivity is sensitive to temperature, and when there is a significant temperature difference, it can introduce non-uniformity in the temperature gradient.

Table 4-4;Thermal conductivity values for different type of membranes of thickness 60nm; plain membrane (P), phononic membrane (PE) and phononic membrane with platform (HPE). Hole's diameter = 45.8nm, pitch=100nm, platform diameter= 10µm.

	Plain membranes (P)	Phononic membranes (PE)	Phononic membranes with platform (HPE)
L=20µm W=10µm	32W/mK	25W/mK*	14W/mK
L=60µm W=10µm	31W/mK	18W/mK	18W/mK
L=100µm W=10µm	25W/mK	11W/mK	10.5W/mK

Incorporating patterns into the membrane design results in a notable decrease in thermal conductivity, with a reduction of about 56% observed for membranes with lengths of 20µm and 100µm, and a 42% reduction for membranes with a length of 60µm. This decrease can be attributed to several factors. Firstly, the introduction of patterns creates additional interfaces and boundaries within the membrane. These interfaces act as scattering sites for heat-carrying phonons, impeding their efficient propagation and resulting in a decrease in overall thermal conductivity. Secondly, the presence of patterns enhances phonon-phonon scattering interactions, leading to increased thermal resistance and reduced thermal conductivity. The patterns also introduce localized regions of reduced material density, which in turn increases the phonon scattering mean free path and further contributes to the decrease in thermal conductivity. Figure 4-36 illustrates the relationship between the thermal conductivity ratio of the phononic membrane to the thermal conductivity of the plain membrane and the porosity of the membrane.

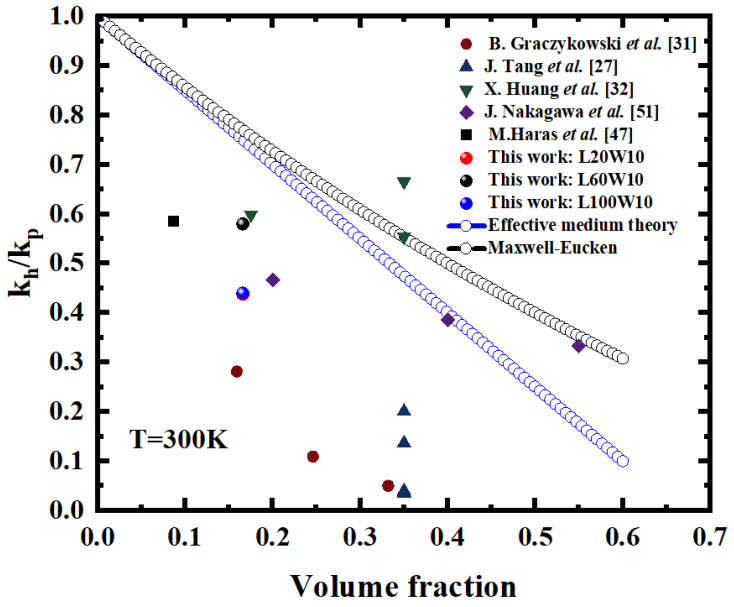


Figure 4-36: The ratio of the phononic membrane to the thermal conductivity of the plain membrane as a function of the porosity. The graph includes experimental data from previous studies, as well as data from this current work, along with results obtained from effective medium theory and Maxwell-Eucken models.

4.4 Figure of merit (zT) determination

4.4.1 Analytical figure of merit (zT)

The power factor of a thermoelectric material, represented by ($S^2\sigma$), is a measure of its ability to convert temperature gradients into electrical power. It combines the square of the Seebeck coefficient (S), which relates the voltage generated to the temperature difference, with the electrical conductivity (σ) of the material. The power factor quantifies the efficiency of a thermoelectric material in converting thermal energy into electrical energy.

In the case of the membranes studied, the power factor can be determined based on the measurements of the Seebeck coefficient and electrical conductivity. However, since the electrical conductivity measurements were conducted only on plain membranes, the experimental values of the power factor and the thermoelectric figure of merit (zT) are available only for plain membranes. Nevertheless, it is possible to estimate the power factor and zT for phononic membranes by assuming that the reduction in electrical conductivity in these membranes is solely due to the patterned structure, rather than other factors. Both Vander Pauw structure of the phonon-engineered membrane and the plain membranes are located on the same chip and in close proximity to each other. Additionally, both membranes undergo identical doping conditions. Consequently, the electrical conductivity of the phonon-engineered membranes is determined using the effective medium theory (EMT) given by Equation 4- 27

$$\frac{\sigma_{PE}}{\sigma_P} = \frac{1-\text{ø}}{1+\text{ø}}$$

Equation 4- 27

With ø, σ_{PE}, σ_P are the porosity, electrical conductivity of patterned membranes and electrical conductivity of plain membranes, respectively. Porosity (ø) refers to the extent of surface area covered by holes in relation to the overall surface area of a plain layer. It can be visualized as

the surface area occupied by a single hole over a square with a side length equal to the pitch of the phononic lattice. By applying the following equation, the porosity can be determined. In the specific case of a phononic lattice composed of holes with a diameter of 45.8nm and spaced at a pitch of 100nm, the lattice exhibits a porosity of approximately 16.47%.

The analytical power factor of phononic and plain membranes in both n-type and p-type configurations is presented in Table 4-5. The power factor of the n-type material is slightly higher than that of the p-type material, primarily because of its higher electrical conductivity compared to the p-type material. Additionally, both the phononic and plain configurations exhibit similar power factors. This similarity can be attributed to the compensation effect resulting from a slight increase in the Seebeck coefficient and a reduction in electrical conductivity due to the patterned structure of the membranes.

Table 4-5: The analytical power factor of plain and phonon membranes in both n-type and p-type configurations.

	Plain p-type membranes	PE p-type membranes	Plain n-type membranes	PE n-type membranes
$S^2\sigma$ [W/mK^2]	0.0018	0.0014	0.0027	0.0024
$\Delta(S^2\sigma)$ [W/mK^2]	$\pm$ 1.60.10^{-5}	$\pm$ 1.26.10^{-5}	$\pm$ 2.17.10^{-5}	$\pm$ 3.0.10^{-5}

Figure 4-37 presents a graph that showcases the correlation between power factor ($S^2\sigma$) and doping level for both n-type (blue) and p-type (red) silicon at a temperature of 300K. The power factor values are plotted on the y-axis, while the doping level is represented on the x-axis. The graph includes our own experimental measurements for comparison. Among our measurements, the highest power factor achieved was 2.7.10^{-3}W/mK^2, corresponding to a specific doping level of 7.2.10^{18} cm^{-3}(n-type). In addition to our data, the graph also displays information on p-type nanostructured silicon. Specifically, it includes results from studies involving nanowires[37][113], holey silicon[27][114][115][116], and ultrathin solid films. Comparing these different nanostructures, it becomes apparent that the power factor of nanowires, as reported in reference [37], is significantly higher than that of other nanostructures studied in the literature.

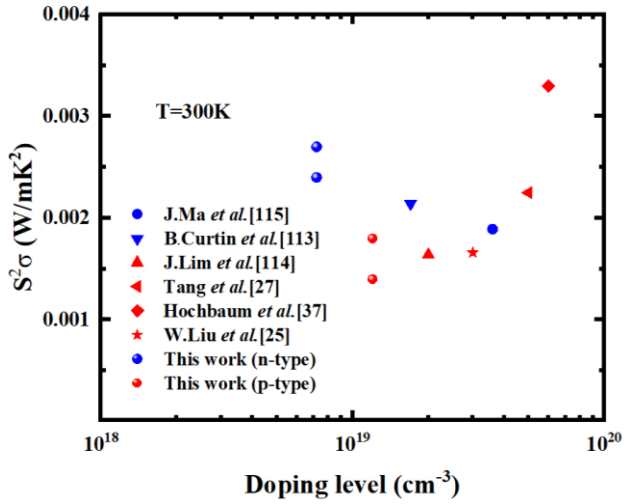


Figure 4-37: Power factor as a function of doping level. The graph includes experimental data from previous studies, as well as data from this current work, encompassing both n-type silicon (indicated in blue) and p-type silicon (represented in red) at a temperature of 300 K.

As detailed in section 4.1.2.2, the existence of phonon drag effect led to an elevation in the Seebeck coefficient. Consequently, this increase in the Seebeck coefficient contributed to an overall enhancement in the power factor. By dividing the power factor by the thermal conductivity, the figure of merit (*zT*) can be calculated. Table 4-6 provides the *zT* figure of merit at room temperature (300K) for both n-type and p-type membranes in both plain and patterned configurations. When calculating the *zT* figure of merit, it is assumed that both the p-type and n-type membranes have the same thermal conductivity and the thermal conductivity value applied is derived from the results obtained from membranes with L=60μm and W=10μm.

Notably, the *zT* figure of merit for patterned membranes is higher compared to plain membranes, primarily due to their reduced thermal conductivity resulting from the patterned structure. Furthermore, the *zT* figure of merit for patterned membranes is shown to be approximately seven times higher than that of bulk materials. This indicates the significant enhancement in thermoelectric performance achieved through the patterned structure, which effectively reduces thermal conductivity and boosts the overall figure of merit.

Table 4-6: The analytical zT figure of merit at room temperature (300K) for both n-type and p-type membranes in both plain and patterned configurations.

	Plain p-type membranes	PE p-type membranes	Plain n-type membranes	PE n-type membranes
zT @ 300K	0.017	0.023	0.026	0.04

The presence of phonon drags at temperatures near room temperature in membranes has provided an opportunity to enhance the Seebeck coefficient. As a result, the power factor of these membranes has increased, reaching a level comparable to that of Bulk Si at similar temperatures. Additionally, the reduced thermal conductivity observed in the membranes compared to Bulk Si has contributed to a further increase in the figure of merit. To achieve a higher figure of merit (*zT*), it is recommended to focus on utilizing the phonon drags to further enhance the Seebeck coefficient while concurrently reducing the thermal conductivity. By capitalizing on these two aspects, it is possible to achieve an even greater figure of merit, thereby improving the overall thermoelectric performance of the membranes.

Table 4-7 compares our findings with those from previous studies, focusing on the Seebeck coefficient, electrical conductivity, thermal conductivity, and *zT* figure of merit. This table helps us see where our work fits into the existing research. The impact of different silicon geometries (thin film, nanowire or holey Si) and type of doping (p-type or n-type) are also considered.

Table 4-7: Comparison of Seebeck coefficient, electrical conductivity, thermal conductivity, and zT figure of merit at room temperature across various silicon geometries and doping types.

Authors	**Si material**	**|S| [μV/K]**	**σ [kS/m]**	**κ [W/m.K]**	**zT @ 300K**
Boukai *el al.* [36]	Nanowire (p-type)	234.52	N/A	3.97	0.24
Hochbaum *et al.* [37]	Nanowire	240	67	1.6	0.6
J.Lim *et al.* [114]	Holey Si (p-type)	270	9	4	0.05
		470	1	3.5	0.015

A.George *et al.* [33]	Thin film (p-doped)	168	99	20	0.03
	Thin film (n-doped)	84	149	23	0.01
J.Tang *et al.* [27]	Holey Si ribbon (p-type)	260	33.34	1.6	0.4
P.Ferrando-Villalba *et al.* [34]	Thin film	150	38.46	55	0.0093
R.Yanagisawa *et al.*[117]	Holey Si (n-type)	107	80	11	0.022
	Thin film (n-type)	107	85	26	0.011
This Work	Thin film (p-type)	424	10.077	31	0.017
	Holey Si (p-type)	440	7.22	18	0.023
	thin film (n-type)	451	13.18	31	0.026
	holey Si (n-type)	504	9.45	18	0.04

Among the various silicon geometries examined, Si nanowires exhibit a higher *zT* figure of merit, mainly due to their low thermal conductivity, which falls below the amorphous silicon limit. However, the specific reasons behind this superior performance are still not fully understood. Additionally, optimizing *zT* proves challenging due to the interconnected nature of transport properties, presenting a complex hurdle in the field of thermoelectric research.

4.4.2 Direct measured figure of merit (zT)

After calculating the analytical *zT* figure of merit, this section of the study focuses on investigating the characterization conditions required for direct zT measurements. It aims to propose a specific set-up that can be used to directly measure the *zT* value of the silicon nano-meshes. The purpose of this part is to outline the necessary parameters, equipment, and measurement techniques that will enable the direct determination of the *zT* figure of merit.

4.4.2.1 Principle

The principle of direct zT measurement, as explained in Chapter 2, is based on evaluating the Harman zT figure of merit. In Chapter 2, the intrinsic figure of merit is developed and presented through Equation 4- 28:

$$\frac{1}{zT_H} = \frac{1}{zT_i}\left(1 + \frac{\beta PA(\bar{T} - T_O) - \rho I^2}{2\kappa\Delta T}\frac{L^2}{A^2} + \frac{L}{A}\left(\frac{K_C}{2\kappa\Delta T}(T_O - T_C) + \frac{K_H}{2\kappa\Delta T}(T_H - T_O)\right)\right)$$

Equation 4- 28

In the equation, zT_H represents the direct figure of merit obtained using the Harman technique. The length of the membrane is denoted by L, while A refers to the cross-sectional area of the membrane. K_C represents the thermal conductance between the platinum (Pt) layer and the substrate. T_0 signifies the ambient temperature. The radiative heat transfer coefficient is represented by $\boldsymbol{\beta}$. P denotes the perimeter of the membrane. $\bar{T}$ represents the average temperature across the membrane. K_H signifies the thermal conductance between the platinum arm at the center of the membrane. The temperature difference between the hot temperature (T_H) at the center of the membrane and the cold temperature (T_C) on the side of the membrane

is denoted as ΔT. **ρ** represents the electrical resistivity, and $\boldsymbol{\kappa}$ refers to the thermal conductivity. These parameters collectively contribute to the calculation of the intrinsic figure of merit (zT_i), providing insights into the thermoelectric performance of the nanostructured membranes.

The direct measurement of the zT figure of merit is carried out through a specific procedure. Initially, the *zT* figure of merit is determined using the Harman technique. By varying the dimensions of the membranes, specifically the length and width, different L/A ratios are achieved. Harman's figure of merit is then measured for each membrane with a distinct L/A ratio. To further analyze the data, the inverse of the measured Harman figure of merit is plotted as a function of the L/A ratio. By fitting this curve and ensuring it passes through the point where L/A equals zero, the inverse of the intrinsic figure of merit of the membrane can be determined. According to Equation 4- 28, the inverse of the intrinsic figure of merit ($1/zT_i$) is equal to the inverse of the Harman figure of merit ($1/zT_H$) as the L/A ratio approaches zero.

Harman's technique, as explained in Chapter 1, allows for the determination of the figure of merit (zT_H) based on two voltages: the resistive voltage (V_R) and the thermoelectric voltage (V_S). The resistive voltage is measured in the absence of temperature difference across the membrane. This can be achieved by either measuring the resulting voltage at the same time as injecting the direct current (I_{DC}), ensuring that the measured voltage corresponds to a null temperature difference across the membrane, or by injecting an alternating current (I_{AC}) with a sufficiently high frequency to suppress the Peltier effect (heating and cooling cycles). On the other hand, the thermoelectric voltage (V_S) is determined after establishing a constant temperature difference across the membrane while injecting a direct current at the center of the membrane. The ratio between the thermoelectric voltage and the resistive voltage provides the Harman zT_H figure of merit.

4.4.2.2 Characterization conditions

The direct measurement of the figure of merit indeed requires careful attention to various conditions and accuracy to ensure reliable results. Several factors need to be considered to achieve accurate and precise measurements. Firstly, precise control and stabilization of temperature gradients are crucial. To minimize unwanted heat transfer and temperature variations, measurements are typically performed under vacuum conditions to avoid convection and conduction with air. Additionally, fixing the temperature of the sample holder at a specific temperature allows for the establishment of a constant temperature difference across the sample. Secondly, electrical measurements must be carried out with high precision. This involves minimizing noise levels, calibrating the measurement equipment accurately, and reducing any electrical interference that could affect the measured voltages. Proper grounding and connection of all electrical components is essential. Using a high-resolution oscilloscope with a microsecond time resolution is recommended to accurately determine the resistive voltage. Furthermore, the choice of the injected current should be based on the desired temperature difference across the sample. It is important to use a thermal camera to monitor and ensure a consistent temperature difference during measurements. This allows for real-time temperature mapping across the sample and ensures that all measurements with different L/A ratios are conducted under the same temperature conditions.

Overall, attention to these conditions, such as vacuum environment, proper grounding, high-resolution measurements, and real-time temperature monitoring, is crucial to achieve accurate and reliable direct measurements of the figure of merit.

In Chapter 3, the devices specifically designed for the measurement of the direct figure of merit are introduced. These devices allow for the variation of the L/A ratio by adjusting their

width, with options of 10, 20, and 30 for each length (20, 60, 100, and 140). Unfortunately, the measurement of the direct figure of merit could not be performed as planned due to the malfunctioning of the thermal camera. The thermal camera, which is a crucial tool for this measurement, experienced technical issues and could not be repaired in a timely manner. However, there is a silver lining to this setback, as plans are underway to replace the thermal camera with a new thermoreflectance camera that offers enhanced functionalities and better resolution compared to the previous infrared thermal camera. Consequently, the prepared devices will be carefully stored in the cleanroom until the new thermal camera arrives. They will then be characterized and utilized for future research projects by the team.

Conclusion

In conclusion, this chapter focused on the characterization of the transport properties of the fabricated devices, including plain and phonon membranes. Each transport property, namely electrical conductivity, thermal conductivity, and Seebeck coefficient, was thoroughly discussed, covering the underlying principles, characterization conditions, and the obtained results. Through our investigations, we discovered that the presence of phonon drags played a significant role in increasing the measured Seebeck coefficient. Moreover, we demonstrated that the phonon engineering process did not impact the behavior of electrons and instead led to a remarkable reduction in thermal conductivity, reaching a factor of 39% decrease compared to plain membranes.

In addition to studying the transport properties, we also examined the power factor and the figure of merit (zT). We provided an analytical zT value of 0.034 for n-type phononic membranes, which was found to be seven times higher than that of Bulk Si membranes at room temperature. Furthermore, this chapter presented the characterization conditions necessary for the direct measurement of the zT figure of merit. By outlining the principles and requirements of this measurement technique, we laid the groundwork for future investigations and experiments in this area.

Overall, this chapter provided a comprehensive understanding of the transport properties of the fabricated devices, highlighted the contributions of phonon drags on the Seebeck coefficient, demonstrated the effect of phonon engineering on thermal conductivity reduction, and presented the analytical power factor and the analytical zT figure of merit. The conditions for characterizing direct zT measurements were also addressed. Nevertheless, the absence of the necessary setup for direct zT measurement made it impractical to implement the transient Harman method. Nonetheless, there is very little left to be done.

General Conclusion

This thesis focused on the development of integrated metrology devices for the study of transport properties in silicon nanostructures. Our research endeavors are directed towards establishing a direct zT metrology framework based on the transient Harman technique.

The first part of this thesis provided a comprehensive overview of thermoelectricity, covering its fundamental principles. This included an explanation of the thermoelectric effect, which comprises the Seebeck effect, Peltier effect, and Thomson effect. We also discussed the theory of thermoelectric power generation devices, focusing on device efficiency and introducing the concept of the *zT* figure of merit. Furthermore, we studied the key transport properties that influence the efficiency of thermoelectric materials. This involves an analysis of thermal conductivity, electrical conductivity, and the Seebeck coefficient, highlighting their roles in determining material performance. Moreover, we reviewed various methodologies aimed at improving the thermoelectric properties of silicon (material of interest for this thesis), with a particular emphasis on strategies to reduce its thermal conductivity. Finally, we discussed the practical integration of silicon into thermoelectric applications, particularly in micro-thermoelectric generators optimized for operation around room temperature.

The second part dealt with the challenges surrounding the determination of *zT* accurately. In Chapter 2, we proposed an adaptation of the conventional transient Harman technique [2], originally designed for bulk materials, to provide direct access to zT through purely electrical measurements. This adaptation eliminates the necessity for separate measurements of transport parameters in suspended crystalline nano-membranes. The adapted transient Harman technique to nanomembranes was studied using both theoretical (analytical formula) and computational (Finite element modeling) means. The importance of internal resistance in silicon becomes evident, introducing an additional heat source alongside the heat generated at the junction due to the Peltier effect. Consequently, the conventional Harman technique is no longer applicable, as it relies on the principle that the heat generated at the junction equals the heat flow through the sample due to the imposed temperature difference. To address this issue, we demonstrated that the Seebeck voltage can be expressed as a sum of two components: the intrinsic thermoelectric voltage (V_{S0}), which is proportional to *zT*, and the voltage resulting from Joule heating effects (V_{SJ}), which should be eliminated. We presented a method to eliminate the Joule heating effect from the measured *zT* by using two opposing DC currents to cancel out the Joule heating contribution, allowing for the determination of the Seebeck voltage (V_{S0}). Furthermore, we developed a thermoelectric relationship that accounts for all thermal losses specific to nanostructured membranes, and we expressed the intrinsic zT (zT_i) as a function of the classical Harman (zT_H), the membrane's shape factor (L/A), and a correction factor to consider radiation, contact resistances, and Joule heating effects. This zT_i is determined using a graphical method by plotting the reciprocal of zT_H, which represents our measurement, as a function of L/A. Subsequently, we fit this data using a second-order polynomial equation. This method enables us to derive an effective zT_i value without directly quantifying the extrinsic factors. The relationship between zT_H and zT_i is expressed as:

$$\frac{1}{zT_H} = \frac{1}{zT_i}\left(1 + \left(\frac{K_C}{2\kappa\Delta T}(T_O - T_C) + \frac{K_H}{2\kappa\Delta T}(T_H - T_O)\right)\frac{L}{A} + \left(\frac{\beta PA(\bar{T} - T_O) - \rho I^2}{2\kappa\Delta T}\right)\frac{L^2}{A^2}\right)$$

Chapter 2 also involved Finite Element Modeling (FEM) of the adapted transient Harman technique for nano-meshes. The modeling studied *zT* under various scenarios of silicon thermal conductivity, including bulk thermal conductivity and reduced thermal conductivity[79]. The modeling studies reported:

- A difference between the zT figure of merit determined using the classical Harman technique and the analytical formula of zT (utilizing transport property values), This discrepancy is attributed to the additional heating source introduced by the internal electrical resistance of the Si membrane.
- A gain on time delay in heat dissipation after current cutoff for nanostructured materials with low thermal conductivity.

The modeling studies provided calibration curves for determining thermal conductivity based on the temperature difference created across the membrane when injecting a current of 0.3mA, or to ascertain the required current injection based on the membrane's thermal conductivity to achieve a 30K temperature difference.

The third part focused on the design and realization of an integrated metrology device dedicated to transient Harman measurements of silicon nano-meshes. These devices were fabricated with and without phonon engineering to investigate the impact of phonon engineering on thermoelectric performance, and they featured various geometries. Additionally, to complement the transient Harman measurements, we created elementary devices capable of assessing transport properties such as thermal conductivity, Seebeck coefficient, and electrical conductivity on the same wafer. These additional devices aimed to facilitate the examination of how phonon engineering affects silicon's thermoelectric properties, including the Seebeck coefficient, thermal conductivity, and electrical conductivity. Furthermore, they allowed us to compare the directly measured *zT* figure of merit to the analytical determined *zT*. In total, we fabricated 48 devices for the transient Harman technique and 48 samples for Seebeck coefficient measurements, encompassing different geometries in both n and p type membranes including both phononic and plain configurations. We also manufactured 96 thermal conductivity platforms, which included different geometries, various doping levels, plain and phononic membranes, and phononic membranes with platforms. The devices were realized from a SOI wafer according to a CMOS compatible process whose main steps were:

- The SOI wafer’s top layer patterning by means of e-beam lithography and Cl2/Ar Reactive-Ion-Etching (RIE)
- SOI electrical properties modification by means of ion implantations.
- Materials deposition on that top layer by means of Low-Pressure-Chemical-Vapor-Deposition (LPCVD) and e-beam evaporation.
- Thermal insulation of the top layer from the others layer of the SOI by XeF2 and HF vapor etching.

It's worth noting that the integrated metrology device designed for transient Harman measurements of silicon nano-meshes presented a more complex fabrication process compared to the metrology device dedicated for transient Harman measurements of bulk materials.

The fourth and last part detailed the characterizations of the different realized devices. Starting with the Seebeck coefficient measurements platform, it was vital before any characterization to accurately calibrate the Pt heaters in order to determine the temperature difference across the membrane via an electrical measurement using the thermal coefficient of resistance (TCR) as the heating power was delivered to the silicon membranes through the Joule effect occurring in the Pt heater serpentines. Once the heaters calibrated, the devices were characterized. The devices’ characterizations reported:

- A better thermal gradient management through the silicon membranes thanks to the phonon engineering (cf. Figure 4-7). This improvement was explained by the increase of

the silicon membranes' thermal resistances with the phonon engineering (already demonstrated by previous works [79][81] [1].

- A high Seebeck coefficient value for both phononic and plain membranes thanks to the presence of the phonon drags. (cf. Figure 4-9)
- Thermal measurements indicated a comparable temperature difference across the membrane.

Furthermore, thermal conductivity measurements were carried out under vacuum conditions near room temperature. These measurements determined a thermal conductivity of 31 W/m·K for a 60 nm thick Si membrane and κ= 18 W/m·K for a 60 nm thick phonon-engineered Si membrane. This represents an 88% reduction in thermal conductivity compared to bulk Si material and a 42% reduction compared to plain Si membranes.

In terms of power generation, the power factor of our fabricated devices exhibited superior performance compared to state-of-the-art silicon thin films at room temperature. However, when compared to state-of-the-art Si nanowires, the performance was relatively lower (cf. Figure 4-37). Notably, a zT figure of merit of 0.04 was reported using a 60 nm thick phonon-engineered Si membrane. This zT figure of merit is 40 times higher than that of bulk Si (0.001).

Perspectives

Short Term:

1. **Direct zT Measurements**: The fabricated integrated metrology devices for transient Harman measurements of silicon nano-meshes are ready for characterization. Additionally, the groundwork for direct zT measurements has been laid, awaiting the arrival of Transient Thermo-Reflectance equipment to the lab. This equipment will enable the direct determination of zT, providing valuable insights into the thermoelectric performance of these silicon nanostructures.
2. **Temperature-Dependent Thermal Conductivity**: The devices designed for thermal conductivity measurements can be utilized to investigate the impact of temperature on silicon's thermal conductivity. By conducting measurements across different temperature ranges, we can gain a comprehensive understanding of how thermal conductivity varies with temperature, which is crucial for optimizing thermoelectric applications.
3. **Low-Temperature Seebeck Coefficient**: The Seebeck coefficient measurement devices can be employed to characterize the Seebeck coefficient at lower temperatures. This extended temperature range analysis will enhance our comprehension of phonon drag effects and further refine our understanding of the material's thermoelectric behavior.

Medium to Long Term:

This thesis, along with prior research studies [91],[88], has consistently highlighted the presence of the phonon drag effect in Silicon on Insulator (SOI) at or near room temperature. This phenomenon is characterized by an augmentation of the Seebeck coefficient within the SOI layer, consequently bolstering its power factor. Notably, the SOI layer demonstrates a notable characteristic of low thermal conductivity, further contributing to an overall improvement in the figure of merit. Consequently, the exploration of pathways to enhance the power factor by harnessing the potential of phonon drag effects emerges as a promising research avenue.

While previous investigations have successfully demonstrated the feasibility of reducing thermal conductivity up to the limits of amorphous Si, such reductions often come hand in hand with a decline in the Seebeck coefficient. To capitalize on phonon drags, a comprehensive exploration into the geometry and doping levels of thermoelectric materials is required. In the context of bulk materials, studies have revealed that the Seebeck coefficient attributed to phonon drags contributes roughly 50% to the total Seebeck coefficient [118].

In the domain of nanostructured materials, the introduction of boundary scattering disrupts phonon mean free paths, subsequently impacting the Seebeck coefficient associated with phonons. Even in thin silicon films with thicknesses hovering around 100nm, the presence of phonon drags remains evident, as supported by relevant literature [119]. These findings show the possibility of conducting an optimization study that considers the collective influence of diverse parameters governing phonon drags. Much similar to the optimization efforts targeted at enhancing the zT figure of merit, this endeavor would involve a detailed examination of

factors encompassing thermoelectric material geometry, doping levels, and other pertinent variables.

In summary, the avenue of exploration offered by phonon drags holds great promise for further elevating the zT figure of merit. Importantly, this research direction affords the prospect of decreasing thermal conductivity significantly while retaining the Seebeck coefficient to a substantial degree. As illustrated in Figure 4-15, accomplishing this objective entails the strategic development of a phonon filter designed to selectively target phonon modes characterized by shorter mean free paths. At an operating temperature of 300 K, phonons with mean free paths shorter than 1μm contribute to approximately 70% of the total thermal conductivity while exerting minimal influence on the phonon drag effect. Consequently, by effectively "filtering out" these phonon modes, it becomes conceivable to attain a substantial reduction of up to 70% in thermal conductivity, all without significantly compromising the Seebeck coefficient.

Appendix 1

This appendix serves as an additional section complementing Chapter 3, offering a deeper understanding of the devices manufactured within that chapter. It provides supplementary details, encompassing device geometries, labels, configurations.

The realized devices

Chapter 3 detailed the delicate fabrication process of an integrated metrology device, known as "*zT* direct measurement devices," which serves the purpose of conducting transient Harman measurements on silicon nano-meshes. However, to fully characterize and understand the performance of the developed demonstrator, it was necessary to construct additional elementary devices capable of extracting crucial thermoelectric properties. These properties include thermal conductivity, Seebeck coefficient, and electrical conductivity. In the upcoming sections, we will delve into the fabrication and functionality of these distinct devices, shedding light on their role in the overall characterization process.

zT figure of merit direct measurement devices

To ascertain the correction factor arising from the parasitic terms in the Harman method, a series of transient Harman demonstrators with diverse geometries are manufactured. These demonstrators are specifically designed and fabricated to investigate the impact of the parasitic terms, as elucidated in Chapter 2. The objective is to quantify the magnitude of these parasitic effects and understand their influence on the accuracy and reliability of the Harman method. Moreover, in order to examine the influence of phonon engineering on thermoelectric properties and performances, the direct *zT* figure of merit measurement device (Figure 1) is fabricated in two variations: phonon and non-phonon engineered. These devices are utilized to quantify the impact of phonon engineering on the *zT* figure of merit, focusing on Si-type materials in both n-type and p-type configurations. The goal is to evaluate how the manipulation of phononic properties affects the thermoelectric performance and efficiency of the fabricated devices.

To differentiate between each device, specific labels (Figure 1) were assigned to indicate their characteristics. The labeling scheme consists of three parts: the first part represents the type of membranes used, where "P" denotes plane membranes and "PE" represents phonon engineered membranes. The second part indicates the type of material employed, with "p" indicating p-type material and "n" representing n-type material. Lastly, the labeling includes dimensions of the membranes, specified as "LxWy," where "L" denotes the length and "W" signifies the width of the membrane.

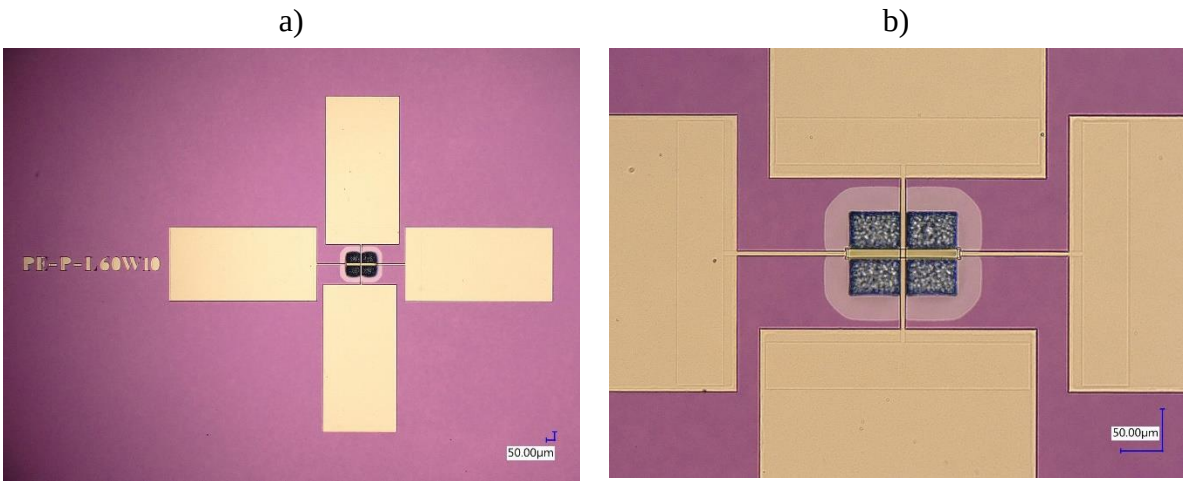


Figure 1: The optical microscope images showcase a) the fabricated zT direct measurement device, b) a close-up view of the Si suspended membrane within the zT direct measurement device.

Electrical conductivity measurement devices

The second device, as shown in Figure 2, is designed to determine the electrical conductivity of the silicon layer and assess the doping level following ion implantations, utilizing the Van Der Pauw methodology. The chip comprises eight cells, consisting of four cells with p-doped silicon and four cells with n-doped silicon. Both the p-doped and n-doped versions include configurations with and without phonon engineered layers. Located at the center of each cell is the silicon doped layer. At the four corners of the cell, platinum silicide contacts are positioned for conducting electrical conductivity measurements using a four-probe resistive measurement technique. To isolate the platform from the rest of the SOI wafer, cavities are etched around it.

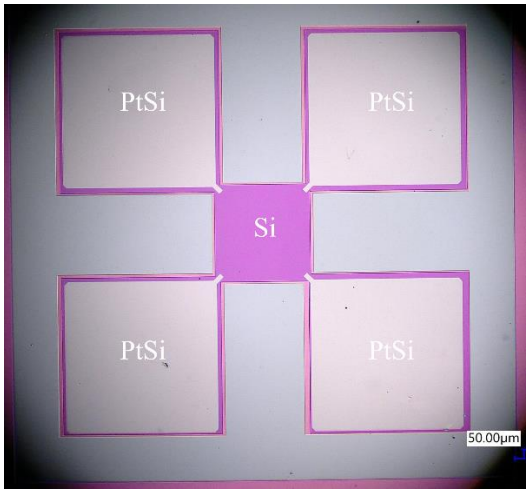


Figure 2: Microscope image of the fabricated Van Der Pauw structure, for the measurement of the electrical conductivity.

Seebeck coefficient measurement devices

The third category of fabricated devices consists of Seebeck coefficient measurement devices (Figure 3), which are specifically designed to measure the Seebeck coefficient of a particular thermoelectric material. These devices feature a suspended Si membrane that is

connected to two metallic pads made of gold (Au). These pads serve the purpose of measuring the Seebeck voltage generated as a result of the temperature difference across the membrane. To create this temperature gradient, a heater is strategically placed near the edge of the membrane. In fact, each device incorporates two heaters to ensure accurate temperature difference measurement across the membrane. These heaters are fabricated in a serpentine form using platinum (Pt). The four pads connected to the first platinum heater allow for simultaneous modeling of the hot source through the Joule effect, while also verifying the absence of current leakage. Additionally, they facilitate the measurement of the cold temperature using the second heater. The Seebeck measurement devices are fabricated for various types of devices, including plain membranes and phononic membranes, with both p and n-type doped membranes. Moreover, different membrane geometries are incorporated for each type of device.

a) b)

Figure 3: The microscope images showcase a) the fabricated Seebeck coefficient measurement device, b) a close-up view of the Si suspended membrane within the Seebeck coefficient measurement device.

Thermal conductivity measurement devices

The final set of devices consists of thermal conductivity measurement devices (Figure 4) that are specifically designed to determine the thermal conductivity of fabricated suspended membranes using Raman thermometry. These devices are capable of characterizing the thermal properties of the membranes. Two types of silicon membranes are created for each doping nature, namely n-type and p-type: phononic engineered membranes and non-phononic engineered membranes. The phononic engineered membranes are further divided into two subgroups: fully patterned membranes and patterned membranes with a non-patterned circle of 10μm at the center. This categorization allows for the investigation of the impact of laser spot injection on both the patterned and non-patterned surfaces of the phononic membranes during Raman measurements. Furthermore, these thermal conductivity measurement devices are fabricated in multiple geometries for each configuration, including phononic, plane, and phononic with unpatterned circles.

In addition to the abbreviations utilized to discern whether the membranes are phonon-engineered or non-phonon-engineered and identify their p or n type material, as well as provide information about their geometry, the thermal conductivity devices also employ an additional abbreviation. This abbreviation, “HPE”, refers to the phononic membranes featuring a non-patterned circle positioned at the center.

a) b)

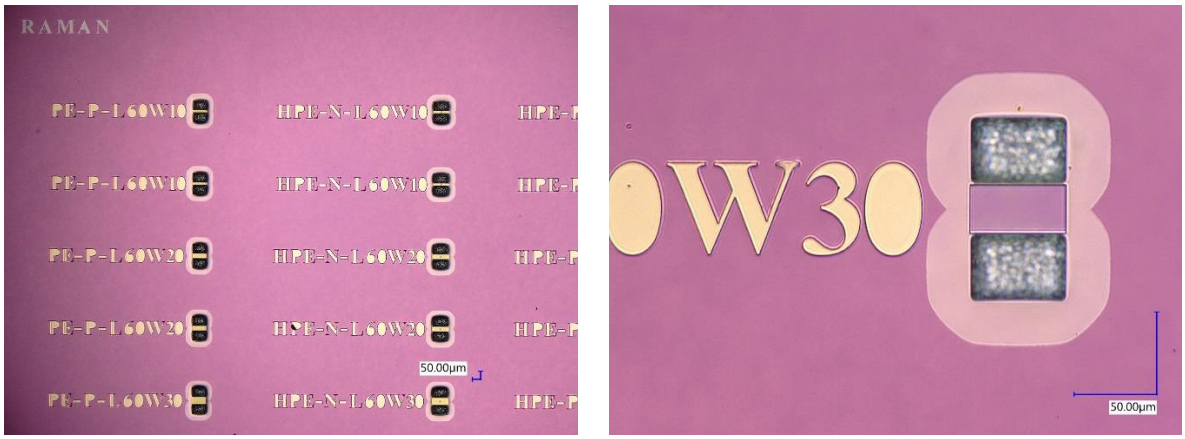


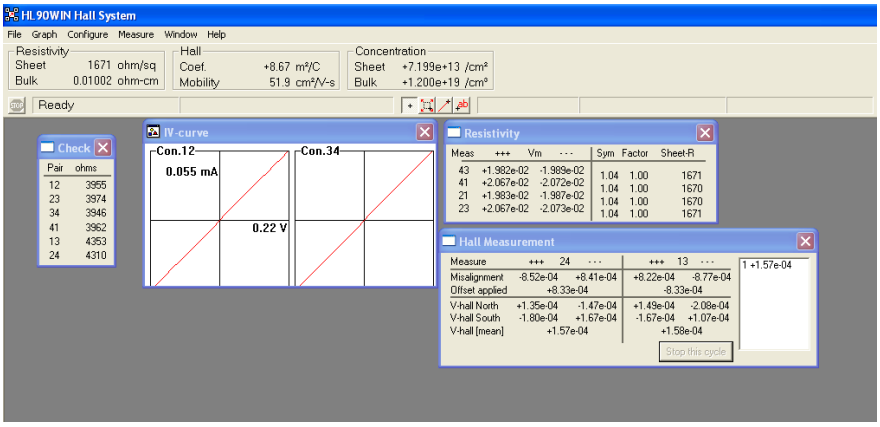
Figure 4: The microscope images showcase a) the fabricated Thermal conductivity measurement device, b) a close-up view of the Si suspended membrane within the thermal conductivity measurement device.

Appendix 2

Doping level/Electrical conductivity measurement software:

The HL90WIN Hall System software was utilized to conduct the Hall effect measurements, offering extensive functionality for analyzing the parameters associated with the Hall effect. Figure 1 presents the results obtained from the measurement of a 60nm thick plain p-Si layer (depicted in Figure 1-a) and n-Si layer (depicted Figure 1-b). The figure comprises four windows, each designed for a specific purpose. The first window displays the outcomes of the contact check phase, ensuring the reliability of the electrical contacts. The second window exhibits the I-V curves for contacts 12 and 34, providing valuable insights into the electrical behavior of the sample. The third window is dedicated to resistivity measurements, presenting the measured V_{XY} voltage, symmetry factor, and sheet electrical resistance (**ρ**/t). Lastly, the fourth window focuses on Hall measurements, which enable the determination of the carrier concentration in the Si membranes. To facilitate ease of access, the top bar of the software's global window prominently displays significant parameters related to the Hall effect measurements. These parameters encompass the Hall constant, resistivity, Hall coefficient, electron or hole mobility, and carrier concentration. With their prominent display in the top bar, these values can be quickly referenced and analyzed, facilitating the interpretation of the obtained results.

a)



b)

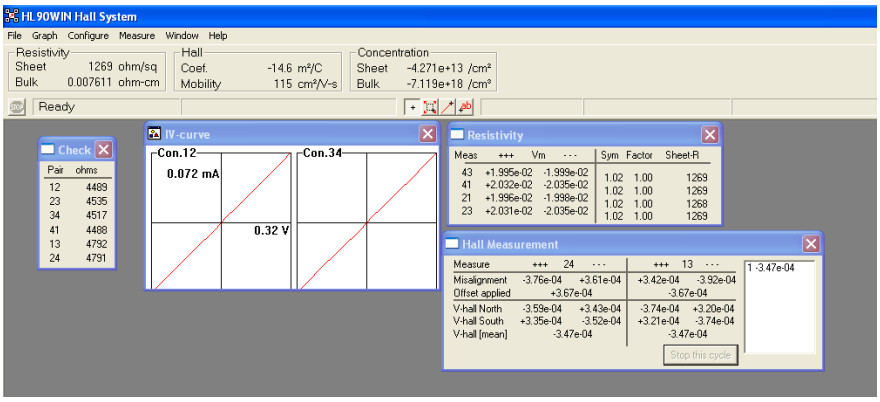


Figure 1: Electrical resistivity and carrier concentration of a 60nm plain membranes a) p-type, b) n-type.

Scientific Production

Journals:

[1] H. Ikzibane *et al.*, "In preparation"

[2] **T.-M. Bah**, S. Didenko, D. Zhou, H. Ikzibane, S. Monfray, T. Skotnicki, E. Dubois, J.F.Robillard "A CMOS compatible thermoelectric device made of crystalline silicon membranes with nanopores," Nanotechnology, vol. 33, no. 50, p. 505403, Sep. 2022.

Conferences:

[1] **H. Ikzibane**, J. Canosa, E. Dubois, J.-F. Robillard, "Integrated metrology devices dedicated to transient Harman measurement of silicon nano-meshes," Workshop for multi-functional materials, Valenciennes, France, June 2023.

[2] **J. F. Robillard**, H.Ikzibane, A.Massoud, V. Lacatena, M. Haras, S. Didenko, S. Monfray, J.M.Bluet, P.O.Chapuis, E.Dubois, "Heat transfer in silicon nano-membranes: application to thermoelectricity," in The 20th international symposium on the Physics of Semiconductors and Applications (ISPSA20), Jaeju, South Korea, Jul. 2022.

[3] **H. Ikzibane**, J. Canosa, E. Dubois, J.-F. Robillard, "Integrated metrology devices dedicated to transient Harman measurement of silicon nano-meshes," in Nanoscale and Microscale Heat Transfer VII - Eurotherm, Palermo, Italy, May 2022.

[4] **J. Canosa**, H.Ikzibane, B.Brisuda, N. Mingo, O.Bourgeois, E. Dubois, J.F.Robillard, "Suspended crystalline silicon thermometry devices: towards quantum nanophononics" in Nanoscale and Microscale Heat Transfer VII - Eurotherm, Palermo, Italy, May 2022.

[5] **H. Ikzibane**, T-M. BAH, J.-F. Robillard, E. Dubois, "Design, modelling and fabrication of integrated devices dedicated to transient Harman measurement of silicon Membrane-Based Thermoelectric Energy Harvester" in Journée virtuelle de la thermoélectricité , Lille, France, Dec. 2021.

[6] **H. Ikzibane**, J.-F. Robillard, E. Dubois, "Design and modelling of integrated devices dedicated to transient Harman measurement of silicon nano-meshes" in Virtual Thermoelectric Conference (VCT2020), Jul. 2020.

[7] **H. Ikzibane**, T-M. BAH, J.-F. Robillard, E. Dubois, "Silicon based microscale thermoelectric Energy Harvester" in Nanoscale Heat Transport Days, Paris, France, Jan. 2020.

[8] **H. Ikzibane**, T-M. BAH, J.-F. Robillard, E. Dubois "Thermal conductivity reduction of a Silicon Membrane-Based Thermoelectric Energy Harvester" in Journées nationales de thermoélectricité (Jnte), Metz, France, Jan. 2020.

Seminar:

[1] H. Ikzibane, E. Dubois, J.-F. Robillard, "Integrated metrology devices dedicated to thermoelectric energy harvesting," ST-IEMN Common lab seminar, Crolles, France, Nov. 2022.

[2] **H. Ikzibane**, E. Dubois, J.-F. Robillard, "Integrated metrology devices dedicated to thermoelectric energy harvesting," ST-IEMN Common lab seminar, Online, France, Nov. 2021.

[3] **H. Ikzibane**, E. Dubois, J.-F. Robillard, "Design, modelling and fabrication of integrated metrology devices dedicated to Thermoelectric Energy Harvesting," ST-IEMN Common lab seminar, Online, France, Oct.2020.

Activities:

[1] **H. Ikzibane**, "IEEE Lille Student Branch Kickoff Meeting [Chapters]," IEEE Solid-State Circuits Mag., vol. 14, no. 1, pp. 84–85, 2022.

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