THÈSE

Présentée à l'Université de Lille
École doctorale 632 : Science de l'ingénierie et des systèmes

En vue d'obtenir le grade de

DOCTEUR

en

"Électronique, Microélectronique, nanoélectronique et Micro-ondes"

Novel Hybrid Approach to 2 step SAR Assisted ADC with Bidirectional Digital Slope for Low Power Applications

Nouvelle approche du SAR hybride à 2 étages, assisté d'une pente digitale bidirectionnelle pour des applications à faible consommation d'énergie.

Préparée en collaboration avec:

STMicroelectronics, Grenoble, France
Le laboratoire IEMN, Lille, France

Présentée le 8 Décembre 2023 par :

Jean-Baptiste CASANOVA

Jury

M. Haralampos Stratigopoulos	DR, HDR - LIP6 – Sorbonne Université	Président du Jury
M. Dominique Dallet	PR, HDR - IMS Bordeaux	Rapporteur
M. Daniel Dzahini	IGR, HDR -TIMA-Grenoble INP	Rapporteur
Mme Caroline Lelandais- Perrault	MCF, Ph.D - GEEPS – Centrale-Supelec	Examinatrice
M. Chadi Jabbour	MCF, HDR - Télécom Paris	Examinateur
Mme Sandrine Nicolas	Ing - STMicroelectronics	Encadrante
Mme Danika Perrin	Ing -STMicroelectronics	Encadrante
M. Andreas Kaiser	DR, HDR - Junia, Université de Lille	Directeur de Thèse

À mon grand-père

Résumé

Dans un contexte d'objets toujours plus connectés, la réalisation de chaînes de réception radio faible consommation devient un défi. Dans le cadre d'un financement Cifre ST-IEMN, cette thèse aborde l'enjeu des performances de l'ADC afin d'alléger les contraintes de la chaîne radio analogique. Un ADC présentant 68dB de SNDR à une cadence de 64MS/s avec une consommation inférieur à 300µW est ciblé pour ces travaux.

Après une analyse de l'état de l'art cette thèse propose une innovation de l'approche des convertisseurs SAR hybrides assistés de convertisseur à rampes. Une approche pseudo différentielle permet de diviser par deux la consommation et le temps de conversion de l'étage rampe. Une modélisation complète du système en VerilogA a permis de démontrer la fonctionnalité de la nouvelle architecture ainsi que l'implémentation d'algorithme de calibration. A partir de mesures publiées sur des réalisations similaires, les performances en termes de consommation de l'ADC sont extrapolées. En gardant une marge d'erreur de 30% l'ADC présente une consommation inférieure à 250µW, un SNDR de 67.1 dB pour un échantillonnage de 64MS/s. Ces résultats permettent d'estimer une figure de mérite de Schreier au-delà de 178dB. Une étude des effets non linéaires dues à la bande passante limité du comparateur temps continu de l'étage rampe est également proposée. Leur impact sur la conversion est exprimé en fonction d'un unique paramètre et une correction à partir de ce paramètre est proposé. Cette méthode est comparé à l'état de l'art et montre un gain significatif en performance pour l'application visée.

Abstract

In a context of increasingly connected objects, the creation of low-power radio reception chains is becoming a challenge. As an industrial partnership Ph.D between STMicroelectronics and IEMN lab, this thesis studies the ADC performance challenge in order to alleviate the constraints of the analogue chain. An ADC with 68dB SNDR at 64MS/s and a power consumption of less than 300µW is targeted for this work.

Following an analysis of the state of the art, this thesis proposes an innovative approach to hybrid SAR ADCs assisted by ramp converters. A pseudo-differential approach is used to halve the power consumption and conversion time of the ramp stage. Full modelling of the system in VerilogA was used to demonstrate the functionality of the new architecture and the implementation of a calibration algorithm. ADC power consumption was extrapolated from published measurements of similar systems. With a margin of error of 30%, the ADC has a power consumption of less than 250µW and an SNDR of 67.1dB at a sampling rate of 64MS/s. These results allow an estimate of a Schreier figure of merit above 178dB. A study of the non-linear effects due to the bandwidth limitation of the ramp stage's continuous time comparator is also proposed. Their impact on conversion result is expressed in terms of a single parameter and a correction as a function of this parameter is proposed. This method is compared with the state of the art and shows a significant gain in performance for the targeted application.

Table of Content

SCIENTIFIC PRODUCTION **13**

GENERAL INTRODUCTION **14**

INTRODUCTION GENERALE (FRANÇAIS) **17**

Chapter 1

1.1 RF-RX CHALLENGES **21**

1.1.1 CHALLENGES IN RX FRONT-END DEVELOPMENT 21

1.2 ADC IN RF RECEIVER CHAIN **23**

1.2.1 ADC KEY PARAMETERS 23
1.2.2 INTERACTION BETWEEN ADC AND RX FRONT END 25
1.2.3 ADC SPECIFICATIONS 27

1.3 SURVEY OF ADC STATE OF THE ART **29**

1.3.1 METRICS AND TOOLS TO COMPARE. 29
1.3.2 GRAPHS AND ARCHITECTURES 30

Chapter 2

2.1.1 MAIN ADCS ARCHITECTURES **34**

2.1.1 FLASH, OVERSAMPLED, AND PIPELINED ARCHITECTURES 34
2.1.1.1 Flash Topology *35*
2.1.1.2 ΣΔ topology *36*
2.1.1.3 Pipelined topology *38*
2.1.2 SUCCESSIVE APPROXIMATION REGISTER (SAR) 40

2.2 QUANTITATIVE ANALYSIS OF THE ADC SURVEY **45**

2.2.1 OVERALL SURVEY, SILICON MEASUREMENTS FROM [11] 45
2.2.2 OVERALL SURVEY, FILTERED SILICON REALIZATIONS 46

2.3 HYBRID SAR ARCHITECTURES **48**

2.3.1 HYBRID SAR PIPELINE 48
2.3.1.1 Amplify and quantize the residue *48*
2.3.1.2 State of the art performance *49*
2.3.2 HYBRID SAR NOISE SHAPING 50
2.3.2.1 Noise Shaping SAR (NS-SAR) Overview *50*
2.3.2.2 State of the art performance *51*
2.3.3 TIME-BASED APPROACHES TO HYBRID SAR ADCS 53
2.3.4 HYBRID SAR TDC [69] 54

2.3.4.1 Overall architecture ... 54
2.3.4.2 Performances and drawbacks ... 55
2.3.4.3 Calibration and repeatability ... 56
2.3.5 HYBRID SAR DS [3] ... 57
2.3.5.1 Overall architecture ... 57
2.3.5.2 Advantages and drawbacks ... 59
2.4 CONCLUSION ... 60

Chapter 3

3.1 PROPOSED ARCHITECTURE ... 63
3.1.1 CONCEPTS AND CHALLENGES OF THE ARCHITECTURE ... 63
3.1.1.1 Use of the SAR LSB as information ... 65
3.1.2 ERROR SOURCES AND CORRECTION ... 70
3.1.2.1 Comparator offset and noise in the SAR ... 70
3.1.2.2 Inter stage redundancy ... 73
3.1.2.3 SAR redundancy ... 74
3.1.2.4 Offset calibration ... 76
3.1.2.5 CT-CMP Latency ... 77
3.1.2.6 Latency correction ... 79
3.1.2.7 DAC non idealities ... 81
3.1.2.8 Noise balance ... 82
3.1.2.9 Extra capacitance impact on dynamic ... 84
3.2 SIZING OF THE PROPOSED ARCHITECTURE ... 85
3.2.1 BIT REPARTITION BETWEEN STAGES ... 85
3.2.2 NOISE BALANCE IN THE PROPOSED ARCHITECTURE ... 87
3.2.3 DETAILS OF PROPOSED ARCHITECTURE ... 89
3.2.5 2ND STAGE DIGITAL SLOPE DESCRIPTION ... 91
3.3 VERILOGA MODEL ... 95
3.3.1 DESCRIPTION OF THE VERILOGA MODEL ... 95
3.3.2 TESTBENCH AND SIMULATION RESULTS ... 97
3.3.3 POWER CONSUMPTION ESTIMATION ... 100
3.3.4 COMPARISON WITH STATE OF THE ART ... 103
3.4 CONCLUSION ... 104

Chapter 4

4.1 2ND STAGE CT-CMP DESIGN ... 107
4.1.1 STATE OF THE ART OF CONTINUOUS TIME COMPARATOR ... 107
4.1.2 DESIGN SPECIFICATION OF THE CT-CMP IN BIDIRECTIONAL DS ARCHITECTURE ... 109
4.1.3 CT-CMP, 2 STAGE AMPLIFIERS DESIGN IN 18NM TECHNOLOGY ... 110
4.2 NON LINEARITY BEHAVIOR DUE TO BANDWIDTH RESTRICTION ... 113

4.3 FOLDED CASCODE CT-CMP 115

4.4 BIAS AND START-UP STAGE 117

4.5 LAYOUT AND PLS RESULTS 121

4.6 CONCLUSION 125

Chapter 5

5.1 NON-LINEARITY IN CT-CMP 128

5.2 NON-LINEARITY COMPENSATION 130

5.2.1 COMPENSATION OF THE NON-CONSTANT DELAY AT THE BEGINNING OF THE RAMP 131

5.2.2 COMPENSATION OF THE NON-CONSTANT DELAY AT THE END OF THE RAMP 133

5.2.3 VALIDATION OF THE LINEARIZATION WITH POST-LAYOUT SIMULATIONS 134

5.3 DIGITAL POST-CORRECTION 137

..... 138

5.3.1 DELAY MODEL 138

5.3.2 MODEL BASED OUTPUT ERROR CORRECTION 139

5.3.4 VALIDATION OF OUTPUT ERROR CORRECTION WITH SIMULATED DATA 141

5.3.4 PRACTICAL IMPLEMENTATION OF DIGITAL POST CORRECTION 141

5.5 CONCLUSION 143

Chapter 6

6.1 CONCLUSION 145

6.2 FUTURE WORK 147

List of Figures

Figure 1 – a) Block diagram of mixed analog-digital super-heterodyne receiver b) Spectrum representation of signal before and after down conversion 21
Figure 2 - Representation of frequency sampling and mirror frequency on first and second Nyquist 22
Figure 3 – Bock diagram of a superheterodyne receiver frontend 23
Figure 4 – Inspired from [9] Receiver signal, noise flow diagram and ADC parameter 25
Figure 5 - Example of tradeoff between RF front end and ADC (a) ADC relaxed (b) Front-end relaxed 26
Figure 6 - Dimensioning of the minimum SNR compared to the I/C standard requirement 28
Figure 7 - Walden FOM plot compared to sampling frequency (1997-2020) from [11] 31
Figure 8 - Schreier FOM plot compared to sampling frequency (1997-2020) from [11] 31
Figure 9 - Main performance trends of ADC topologies, inspired by [31], with data of [12]. The star symbol identifies the target specifications for this work as defined in chapter 1. 34
Figure 10 - Concept representation of flash ADC 35
Figure 11 - Simplified block representation of a $\Sigma\Delta$ ADC 36
Figure 12 - Block diagram of a m bits unit stage in a pipelined ADC 39
Figure 13 -Example of transfer function of a 1.5-bit pipeline stage introducing a redundancy of 0.5 bits 39
Figure 14 - Block diagram of a charge redistribution SAR ADC (a) zoom on switches (b) 41
Figure 15 - Block diagram of a differential top plate sampling SAR ADC architecture 42
Figure 16 - Example of 3 bit differential SAR operation 43
Figure 17 - Quotient of power over the frequency compared to SNDR on the whole B. Murmann Survey. 45
Figure 18 - Nyquist frequency compared to SNDR on the whole B. Murmann Survey. 46
Figure 19 - Plot of filtered ADC - Power/Frequency in function of the SNDR 47
Figure 20 - Plot of filtered ADC – F_in high frequency equivalent to the bandwidth of Nyquist ADC compared to SNDR 47
Figure 21 - Block representation of a pipelined SAR architecture 48
Figure 22 – From [11] energy efficiency depending on resolution for realizations close to the target. 49
Figure 23 - Generic block diagram of an NS-SAR ADC 50
Figure 24 - From [65] comparison of simulated comparator noise effect and DAC mismatch and settling error effect on SAR architecture with and without fully passive noise shaping (FPNS) 51
Figure 25 – From [11] energy efficiency depending on resolution for realizations close to the target including with focus on NS-SAR architectures. 52
Figure 26 - From [11] energy efficiency depending on resolution for realizations close to the target. 53
Figure 27 – From [69], block (a) and timing diagram (b) of the proposed architecture (single-ended SAR ADC for simplicity) 54
Figure 28 - Temporal representation of the differential VTC presented in [69] 55
Figure 29 - From [69], Simulated tradeoff between the VTC latency, power consumption, THD, and input referred noise. 56
Figure 30 – From [3], block diagram of the SAR assisted DS ADC 57
Figure 31 - Example of second stage [3] digital slope time operation for positive and negative residue 58
Figure 32 - From [3], implementation of the 6-bit digital slope fine ADC 59
Figure 33 – General concept of the bi-directional digital slope SAR assisted ADC – 12 bit example 63
Figure 34 - Representation of the comparator consumption for the second stage 64

Figure 35 - Illustration of 2nd stage monotonic digital slope behavior for a residue > 0 65
Figure 36 - different approaches of digital slope based on residue sign: double monotonic digital slope for a negative residue (a) and a positive residue (b) - single bidirectional digital slope for a negative residue (c) and a positive residue (d) 66
Figure 37 - Time voltage diagram of a fully differential bidirectional digital slope for a negative residue (a) and a positive residue (b) 67
Figure 38 - temporal voltage representation of proposed pseudo differential bidirectional digital slope for negative residue (a) and positive residue (b) 68
Figure 39 - Temporal voltage representation of SAR sign error causing bidirectional digital slope divergence. (Negative voltage residue and positive sign behavior) 69
Figure 40 - Temporal voltage representation of SAR sign error corrected by 4 step redundancy. (Negative voltage residue and positive sign behavior) 69
Figure 41 - Systemic non idealities representation of the comparators in the proposed architecture 70
Figure 42 - Temporal voltage representation of sign error due to offset. Wrong sign decision taken by the SAR (a) and ramps presented at the second stage comparator (b) compared to the voltage present in the CDAC (Vxp) 71
Figure 43 - Bidirectional ramps through time for a voltage residue greater than the 2nd stage dynamic 72
Figure 44 - Representation of the voltage residue equivalent code through 9 bit SAR example process with, bit decision area (a), example of non-error conversion without redundancy (b), example of conversion with error without redundancy (c), and example of conversion with error and extra step redundancy on 6th comparison to correct the code (d) 75
Figure 45 - Proposed architecture with offset calibration dedicated CDAC- concept diagram block 76
Figure 46 - Representation of the voltage evolution in the proposed foreground calibration on the top plate of the CDAC (a) and seen by the comparator presenting offset (b) 77
Figure 47 - Representation of the second stage comparator latency compared to ideal output with bidirectional slope 78
Figure 48 – Timing diagram of the proposed delay measurement of the comparator using redundancy as expected result. 79
Figure 49 – 3 bit + 1 bit redundancy delay line equivalent thermometric code with proposed digital correction for 6T CT-CMP delay 80
Figure 50 - Noise model in CDAC based ADC in the evaluation phase with Cj capacitance switched amongst Cs capacitance used in the sampling phase. 82
Figure 51- From [87], energy consumption by conversion step of a strong-arm comparator as a function of its input referred noise. Simulated 5fF capacitive load in 65nm. 86
Figure 52 - SAR-Assisted Two stages differential DS block schematic 89
Figure 53 - Proposed ADC time sequence for 64MS/s 90
Figure 54 – Bloc-level representation of the differential CDAC used in the ADC for SAR, TDC and calibration purpose. [VrefP = VDD ; VrefN = GND] 90
Figure 55 - Operation of a bidirectional 2nd stage digital slope (a) for positive residue - (b) for negative residue 92
Figure 56 - 2nd stage: 3 bits Digital slope + 1 bit redundancy 93
Figure 57 - 3 bit pseudo differential Digital Slope with redundancy (a) for positive residue (b) for negative residue 94
Figure 58 - Representation of VerilogA model of the SAR-Assisted Two stages differential DS block schematic including noise, offset and calibration 96
Figure 59 - Cadence VerilogA model cellview with block representation of the test bench simulated in Spectre 97

Figure 60 - Simulated 8192 points FFT of the proposed ADC with noise, offset models – Calibration OFF. 98
Figure 61 - Simulated 8192 points FFT of the proposed ADC with noise, offset models and mismatch (1 draw) Calibration ON. 99
Figure 62 - Power consumption breakdown measurements from [3] 100
Figure 63 - Extrapolated power consumption breakdown for SAR assisted bidirectional ADC from [3] measurements. 102
Figure 64 - From figure 2.17 – From B.Murmann survey, energy efficiency depending on resolution for realizations close to the target including proposed work placed with extrapolated power consumption performances 104
Figure 65 – From [3], schematic of low noise low power CT-CMP 107
Figure 66 – Block representation of two stages amplifier followed by an inverter cell 108
Figure 67 - Design of 2 stages amplifier CT-CMP based on [3] and [73] 110
Figure 68 - Transfer function of the 2-stage amplifier CT-CMP schematic (first stage transfer function - red / second stage transfer function - yellow) – no offset correction 111
Figure 69 – Simulated delay on the output caused by the CT-CMP (time compared between input cross and output rising edge) 112
Figure 70 - (a) First order model of the CT-CMP - (b) Time domain response of the comparator for an input voltage ramp 113
Figure 71 – Cadence (a) and Matlab (b) simulation of first order model CT-CMP 114
Figure 72 - Delay simulated depending of the input for several bandwidth 114
Figure 73 - Schematic of the proposed folded cascode CT-CMP to increase bandwidth. 115
Figure 74 - Transfer function of the proposed folded cascode CT-CMP – no offset correction 117
Figure 75 - Schematic of the proposed bias stage used to start-up the comparator. 118
Figure 76 - Timing diagram of the start-up command 119
Figure 77 - (a) Sequence of start & stop to measure comparator timing - (b) Zoom on start-up 121
Figure 78 - Layout of the folded cascode CT-CMP 122
Figure 79 - Transfer function of the proposed folded cascode CT-CMP with schematic and RCc view – no offset correction 123
Figure 80 - Offset Monte Carlo histogram simulation for RCc view – systematic offset corrected 125
Figure 81 - Temporal model representation of the input and output linearized of the CT-CMP for a given bandwidth. 128
Figure 82 – Simulated unsigned output code vs. ideal unsigned output code over the ±4 bit input range (LSB = 400µV, BW = 637MHz, Timestep 50ps, 16 steps) 129
Figure 83 - Temporal model representation of the input and output linearized of the CT-CMP for a given bandwidth with ramp extension 131
Figure 84 - Temporal model representation of the input and output of the CT-CMP for a given bandwidth with ramp extension and shifted input to compensate first distortion. 132
Figure 85 – Simulated unsigned output code vs. ideal unsigned output code over the ±4 bit input range (LSB = 400µV, BW = 180MHz, Timestep 50ps, 16 steps) 134
Figure 86 – Simulated unsigned output code vs. ideal unsigned output code over the ±4 bit input range (LSB = 400µV, BW = 180MHz, Timestep 50ps, 32 ramp steps in total) 135
Figure 87 - Output code for RCc simulation and theoretical perfect behavior 136
Figure 88 - Output code for RCc simulation (corrected by a 14 step constant offset) and theoretical perfect behavior 137

Figure 89 - Output code for RCc simulation (corrected by a 14 step constant offset) and output code predicted by mathematical model 138
Figure 90 - Linearized model transient simulation 139
Figure 91 - Model correction for one sided sign output codes for 180MHz of f_(-3dB) 140
Figure 92 - Model correction for one sided sign output codes for 180MHz of f_(-3dB) [quantized correction] 140
Figure 93 - Simulated results of RCc view with ramp extension and post digital correction compared to ideal output. 141

List of Tables

Table 1- Specifications of the aimed ADC for this work 29
Table 2 - Flash ADCs in the literature 36
Table 3 - Σ Δ ADCs in the literature 38
Table 4 - Pipeline ADCs in the literature 40
Table 5 – Remarkable SAR ADCs in the literature 44
Table 6 - Detailed performances of highlighted pipelined SAR ADC realizations in Figure 22 49
Table 7 - Detailed performances of highlighted NS SAR ADC realizations in Figure 25 52
Table 8 - Detailed performances of highlighted hybrid SAR-Time domain ADC realizations presented in Figure 26 54
Table 9 - Summarize of simulated model performance compared to state of the art 103
Table 10 - Performances specification of the proposed CT-CMP 109
Table 11 - Transistors sizing of CT-CMP 2 stage amplifier 111
Table 12 - Transistor sizing of CT-CMP folded cascode architecture 116
Table 13 - Transistors sizing of CT-CMP cascode bias/start stage 120
Table 14 - Resume of comparators performances (2stage, folded with schematic and extracted views) – no offset correction 123
Table 15 - Resume of comparators performances with offset correction (2stage, folded with schematic and extracted views) 124
Table 16: Maximum value of measurable τ /t_step for ramps lengths of 16, 32 and 64 steps. From (5.9) 142
Table 17 - Summarize of simulated model performance compared to updated state of the art 146

Scientific Production

Related to the Thesis :

International Conference:

- **J. -B. Casanova**, D. Perrin, S. Nicolas and A. Kaiser, "**A Very Low Power 12 bit 64-MS/s 2 step SAR Assisted Bidirectional Digital Slope ADC**," *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181656.

Patent:

- **J. -B. Casanova**, S. Nicolas, D. Perrin, "**CAPACITANCE SWITCHING SCHEME FOR DIGITAL SLOPE ADC**", Patent ID 83130816, Ref N° 22-GR2-0455FR01,2022.

Non related to the Thesis :

International Conference:

- Nicolas Goux, **Jean-Baptiste Casanova**, Gaël Pillonnet, and Franck Badets. 2020. **A 640pW 32kHz switched-capacitor ILO analog-to-time converter for wake-up sensor applications**, ISLPED '20: Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design. Association for Computing Machinery, New York, NY, USA, 43–48. https://doi.org/10.1145/3370748.3406582

Journal:

- N. Goux, **J. -B. Casanova**, G. Pillonnet and F. Badets, "**A 6-nW 0.0013-mm² ILO Bandpass Filter for Time-Based Feature Extraction**," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 306-309, 2020, doi: 10.1109/LSSC.2020.3016716.

Patent:

- Franck Badets, **Jean-Baptiste Casanova**, "**SUMMING CIRCUIT WITH MULTI INJECTION PHASE**", Patent, EP21209011.2, US20220164632A1, 2021.

General Introduction

Wireless devices have known a significant grown though past decades, specifically in terms of short-range communications. The exponential growth of devices aimed to communicate each other imposed new way to consider emission and reception of data. The authorized frequency being clearly delimited in each continent put every communicating device in a narrow crowdy spectral area. The design and the legislation around the communicating system became more and more aggressive through years, specifically to transfer more data, faster while consuming less energy. The minimal power of signal to detect has also been set lower through years as the maximum signal emitted became stronger. This in a context with several devices communicating together makes severe constraints on receiver circuits.

In the context of wireless communication, the receiver is a system composed of several sub-systems. The antenna, the analog front-end, the analog to digital conversion and the digital signal processing functions are all at least required to receive and process wireless data. All these functions interact with each other and are considered to reach targeted performances. In the context of SoC (System on Chip) receiver the considerations can be different. In ST Microelectronics, wireless telecommunicating devices are developed on SoC with both receiver and transceiver functions. The complexity and interactions of each function is thus increased as for the power management or the clock generation. The power consumption also become a challenge to present a competitive industrial product.

This manuscript is the result of a CIFRE PhD program from a collaboration between STMicroelectronics, Grenoble, France and the IEMN Laboratory at the University of Lille, France. This thesis aims to address industrial challenges in analog to digital converter design, notably the continuous demand on reduction of the power consumption. The context of the work is the future industrial development of advanced radio frequency devices similar to those in the Spirit [1] or BlueNRG [2] product portfolios for sub-gigahertz and Bluetooth short range radios from STMicroelectronics.

The analog to digital conversion functions represents a key parameter for the performance of the global receiver functions. Indeed, the analog front-end parameters such as gain, or noise can be alleviated by the ADC (Analog to digital converter) performances. The targeted performances for this work have been identified in a 12 bit 64MS/s ADC presenting a power consumption below 300µW. The possibility to present two modes of functioning is also required. A high precision mode presenting the discussed performances and a lower power mode presenting at least 9 bit for the same sampling frequency.

This manuscript presents an enhanced ADC topology targeted to fulfill these industrial requirements while presenting sufficient performances to relax future generations of front ends in SoC receivers. The objectives of this work can be summarized as:

- Find an architecture able to fulfill the targeted ADC requirements.
- Develop a resilient architecture sized for industrial requirements.
- Propose an architecture with modularity by having two modes of functioning.
- Reduce power consumption.
- Reduce the required area.

The study starts with an analysis of the ADC impact on the receiver analog front-end. The targeted specifications are then detailed before a state-of-the-art survey. The state-of-the-art analysis starts with the most widely used architectures compared to the targeted specifications. Hybrid topologies are also discussed, and the analysis converges to a SAR Digital Slope hybrid ADC. This architecture looks the most promising and after an analysis of the strength and the weakness of the hybrid topology, an improvement is proposed.

The proposed ADC presents a new way to execute the second stage processing with a pseudo differential approach. The bidirectional ramps proposed in this work enable the second stage to convert its input in a time twice shorter compared to the existing method. Because the consumption of this stage is linear with its time on converting, the proposed architecture divides power consumption of the second stage by two. The proposed architecture is conceptually detailed with offset and latency calibration as with built-in redundancy to correct internal errors. The VerilogA model used to implement the ADC is then discussed before presenting the result simulated confirming the theoretical sizing of the ADC. The power consumption extrapolated from [3] with an arbitrary 30% of margin allows to compare the proposed ADC favorably with state of the art.

The present manuscript is organized in 5 chapters as :

- Chapter 1 : This first chapter presents the discussion between analog front end performances and ADC performances. It allows to underline the importance of sampling frequency and resolution in the global receiver design.

- Chapter 2 : This chapter presents a survey of the state of the art in ADC realizations. Main topologies as SAR, pipeline or oversampled structures are discussed. The classical

structures being too far of the target of this work, hybrid architectures are discussed, mainly with SAR topology. The most interesting realizations are discussed in detail and converge to SAR assisted topology with Digital Slope second stage.

- Chapter 3 : The third chapter presents the proposed ADC topology. A structural presentation is first given with theoretical considerations and interactions. Then the sizing of the proposed ADC is detailed before the model implementation. The VerilogA model is presented as the simulation results obtained with it. An extrapolation of the power consumption from [3] is detailed.

- Chapter 4 : This chapter provides information on the designed CT-CMP used in the proposed second stage. This design has been done in a 18nm node to validate second stage implementation. Schematic and post-layout results are presented, then the impact of parasitic degrading the bandwidth of the comparator is discussed as its impact on the system.

- Chapter 5 : The last chapter presents methods to overcome the low bandwidth impact. Methods from state of the art are presented as their weakness about low power design. A new post digital correction is detailed theoretically then applied to previous post layout results to show digital improvements without extra consumption.

Introduction générale (Français)

Les dispositifs sans fil ont connu une croissance significative au cours des dernières décennies, notamment en termes d'objets communicants à courte portée. La croissance exponentielle des dispositifs destinés à communiquer entre eux a imposé une nouvelle manière de considérer l'émission et la réception de données. La fréquence autorisée étant clairement délimitée sur chaque continent, chaque dispositif communicant se retrouve dans un espace fréquentiel étroit et encombré. La conception et la réglementation autour du système de communication sont devenues de plus en plus agressives au fil des ans, notamment pour transférer plus de données, plus rapidement, tout en consommant moins d'énergie. La puissance minimale du signal à détecter a également été réduite au fil des ans, tandis que le signal maximal émis est devenu plus fort. Dans un contexte où plusieurs dispositifs communiquent ensemble, cela impose des contraintes sévères sur les circuits récepteurs.

Dans ce contexte des communications sans fil, le récepteur est un système composé de plusieurs sous-systèmes. L'antenne, le front-end analogique, la conversion analogique-numérique et les fonctions de traitement numérique du signal sont tous au moins nécessaires pour recevoir et traiter les données sans fil. Toutes ces fonctions interagissent les unes avec les autres et sont dimensionnées pour atteindre les performances ciblées. Dans le contexte d'un récepteur SoC (System on Chip), les considérations peuvent être différentes. Chez ST Microelectronics, les dispositifs de télécommunication sans fil sont développés sur SoC avec à la fois des fonctions de réception et de transmission. La complexité et les interactions de chaque fonction sont ainsi augmentées, tout comme la gestion de l'alimentation ou la génération de l'horloge. La consommation d'énergie devient un défi pour présenter un produit industriel compétitif.

Ce manuscrit est le résultat d'un programme de doctorat CIFRE issu d'une collaboration entre STMicroelectronics, Grenoble, France et le Laboratoire IEMN de l'Université de Lille, France. Cette thèse vise à relever les défis industriels liés à la conception de convertisseurs analogique-numérique, notamment dans ce contexte de demande continue de réduction de la consommation d'énergie. La projection de ce travail est le développement industriel futur de dispositifs radiofréquences avancés similaires à ceux des portefeuilles de produits Spirit ou BlueNRG pour les radios sub-gigahertz et Bluetooth à courte portée de STMicroelectronics.

La fonction de conversion analogique-numérique représente un paramètre clé pour les performances des fonctions globales du récepteur. En effet, les paramètres du front-end analogique tels que le gain ou le bruit peuvent être atténués par les performances de l'ADC (convertisseur analogique-numérique). Les performances ciblées pour ce travail ont été identifiées dans un ADC de 12 bits à 64 MS/s présentant une consommation électrique inférieure à 300 µW. La possibilité de présenter deux modes de fonctionnement est également requise. Un mode haute précision présentant les performances discutées et un mode basse consommation présentant au moins 9 bits pour la même fréquence d'échantillonnage.

Ce manuscrit présente une topologie d'ADC améliorée visant à répondre à ces exigences industrielles tout en présentant des performances suffisantes pour simplifier les futures générations de front-ends dans les récepteurs SoC. Les objectifs de ce travail peuvent être résumés comme suit :

• Trouver une architecture capable de répondre aux exigences ciblées de l'ADC.

• Développer une architecture résiliente adaptée aux exigences industrielles.

• Proposer une architecture avec une modularité en ayant deux modes de fonctionnement.

• Réduire la consommation d'énergie.

• Réduire la surface requise.

L'étude commence par une analyse de l'impact de l'ADC sur le front-end analogique du récepteur. Les spécifications ciblées sont ensuite détaillées avant une étude de l'état de l'art. L'analyse de l'état de l'art commence par les architectures les plus largement utilisées comparées aux spécifications ciblées. Les topologies hybrides sont également discutées, et l'analyse converge vers un ADC hybride SAR Digital Slope (pente numérique). Cette architecture semble la plus prometteuse et après une analyse des forces et des faiblesses de la topologie hybride, une amélioration est proposée.

L'ADC proposé présente une nouvelle façon d'exécuter le traitement du deuxième étage à pente numérique avec une approche pseudo différentielle. Les rampes bidirectionnelles proposées dans ce travail permettent au deuxième étage de convertir son entrée en un temps deux fois plus court par rapport à la méthode existante. Comme la consommation de cet étage est linéaire avec son temps de conversion, l'architecture proposée divise la consommation électrique du deuxième étage par deux. L'architecture proposée est détaillée conceptuellement avec une calibration des décalages et des latences ainsi qu'une redondance intégrée pour corriger les erreurs internes. Le modèle VerilogA utilisé pour implémenter l'ADC est ensuite discuté avant de présenter les résultats simulés confirmant le dimensionnement théorique de l'ADC. La consommation électrique extrapolée à partir de [3] avec une marge arbitraire de 30 % permet de comparer favorablement l'ADC proposé avec l'état de l'art.

Le présent manuscrit est organisé en 5 chapitres :

• Chapitre 1 : Ce premier chapitre présente la discussion entre les performances du front-end analogique et les performances de l'ADC. Il permet de souligner l'importance de la fréquence d'échantillonnage et de la résolution dans la conception globale du récepteur.

• Chapitre 2 : Ce chapitre présente une étude sur l'état de l'art des réalisations d'ADC. Les principales topologies telles que SAR, pipeline ou les structures suréchantillonnées sont discutées. Les structures classiques étant trop éloignées de la cible de ce travail, les architectures hybrides sont étudiées, principalement avec la topologie SAR. Les réalisations les plus intéressantes sont présentées en détail et convergent vers la topologie assistée SAR avec deuxième étage à pente numérique.

• Chapitre 3 : Le troisième chapitre présente la topologie de l'ADC proposée. Une présentation structurelle est d'abord donnée avec des considérations théoriques et le détail de ses interactions. Ensuite, le dimensionnement de l'ADC proposé est présenté avant l'implémentation du modèle. Le modèle VerilogA est détaillé ainsi que les résultats de simulation obtenus avec lui. Une extrapolation de la consommation électrique à partir de [3] est explicitée.

• Chapitre 4 : Ce chapitre fournit des informations sur le comparateur temps continu (CT-CMP) conçu et utilisé dans le deuxième étage proposé. Cette conception a été réalisée avec une technologie 18nm SOI pour valider l'implémentation du deuxième étage. Les résultats schématiques et post-extracts sont présentés, puis l'impact des parasites dégradant la bande passante du comparateur est discuté ainsi que son impact sur le système.

• Chapitre 5 : Le dernier chapitre développe des méthodes pour surmonter l'impact de la faible bande passante. Les méthodes de l'état de l'art sont présentées ainsi que leurs faiblesses en matière de conception à faible consommation d'énergie. Une nouvelle correction post-digitale est détaillée théoriquement puis appliquée aux résultats précédents en post-traitement pour montrer des améliorations numériques sans consommation supplémentaire.

Chapter 1

RX chain & ADC

1.1 RF-RX CHALLENGES 21

1.1.1 CHALLENGES IN RX FRONT-END DEVELOPMENT 21

1.2 ADC IN RF RECEIVER CHAIN 23

1.2.1 ADC KEY PARAMETERS 23

1.2.2 INTERACTION BETWEEN ADC AND RX FRONT END 25

1.2.3 ADC SPECIFICATIONS 27

1.3 SURVEY OF ADC STATE OF THE ART 29

1.3.1 METRICS AND TOOLS TO COMPARE. 29

1.3.2 GRAPHS AND ARCHITECTURES 30

1.1 RF-RX Challenges

1.1.1 Challenges in RX front-end development

Over the past years the number of connected devices has grown exponentially through massive use in domestic, industrial, and urban networks. This forces receiver circuits to handle a crowdy spectral environment and coexistence of multiple systems and networks has become a major concern. Receiver circuits are mainly composed of a mostly analog RF front-end and a digital core for baseband processing. Naturally, the interface between these two functions, the analog-to-digital converter is of key importance for the receiver performances. A RF front end is usually composed of analog blocks dedicated to a particular application or protocol. The data converter must also be sized coherently to optimize the global power efficiently. If the performances are not matched, the overdesigned sections will consume unnecessary energy. The context of this work are applications such as Sub-Ghz and Bluetooth short range radio communications for IoT requiring high performance and low power. The specifications of the different blocks are thus determined by these applications [4]. The converter is a key parameter to reach global performance and system optimization [5]. This global streamlining is possible thanks to the dedicated application unlike approaches such as software defined radio for example. A receiver addressing a wide range of protocols cannot be sized in an optimal way for a specific application and requires extremely high ADC performance [6].

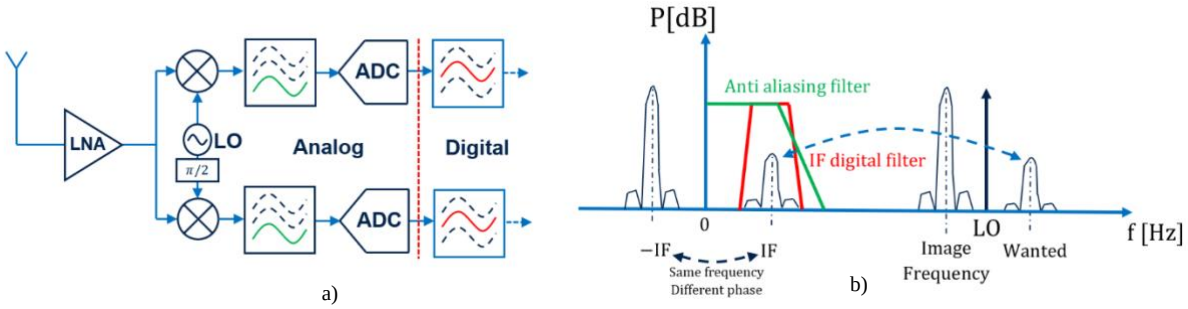

Figure 1 – a) Block diagram of mixed analog-digital super-heterodyne receiver b) Spectrum representation of signal before and after down conversion

For every wireless system like mobile phone, broadcasting, radioastronomy, etc. a strictly defined frequency band is given. From a transmitter perspective this means to not emit outside this band, and from a receiver perspective, this means that signals received outside the limits should not be processed. To achieve such selective reception, a well-known architecture is the super-heterodyne receiver. The wanted signal is amplified then split in two orthogonal branches downconverted from the RF carrier frequency to an intermediate frequency (IF) [7]. It is a choice to have an IF different of 0 (Zero

IF structure), this alleviates the requirements and the processing of offset along the reception chain. The purpose of downconverting the signal is to avoid the system working at high frequency. The system presents then a baseband analog section consuming less energy and with relaxed constraints. However, down conversion performs by construction a spectrum folding (Figure 1), i.e. two frequency bands are translated to the same IF frequency band. Signals in the unwanted frequency band would be super-imposed to the wanted signal and treated by the rest of the circuit. The two branches representing imaginary and real part of the signal (called respectively I & Q) allow the digital part of the system to suppress the image frequency folded on the wanted signal thanks to phase difference. Nevertheless, the ADC presents also down-conversion behavior around its sampling frequency (Shannon theorem) thus an antialiasing filter is then required before the analog to digital conversion. This increases area and power consumption.

As mentioned above, the sampling process of the ADC input signal also down-converts signals in the bands around the multiples of the sampling frequency to the baseband. Unwanted signals can thus be super-imposed to the wanted signal through the conversion. An anti-aliasing filter is thus required to suppress high frequency signals before the sampling as represented in Figure 2. In the targeted systems, the sampling frequency is higher than the IF and the signal bandwidth. The antialiasing filter allows thus to reduce unwanted signal in band and to avoid frequency folding on the wanted signal. There is a trade-off between the IF and the sampling frequency, as shown in Figure 2 representing the first and second Nyquist respect to a multiple of the sampling frequency will be down converted to IF frequency. The first unwanted signal that could be down converted on the band of interest is therefore located at Fs-IF. That means that the closer the IF is to half the sampling frequency, the more the antialiasing filter needs to be be selective [8]. The sampling frequency is a key parameter to reduce antialiasing filter constraints.

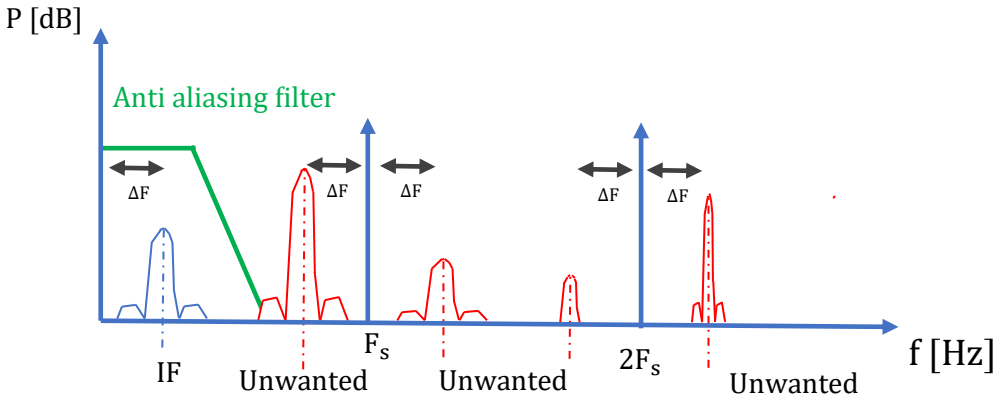

Figure 2 - Representation of frequency sampling and mirror frequency on first and second Nyquist

Furthermore, the RF receiver chain is a system with high level of interdependencies between the different blocks. Key parameters are gain, noise, non-linearity and power-consumption. The receiver frontend is shown on Figure *3*. This work addresses the tradeoff between front-end constraints and ADC performance by proposing a new low power ADC sized for RX chain requirement. Obviously, solutions must be reliable, reproducible and resilient with small area.

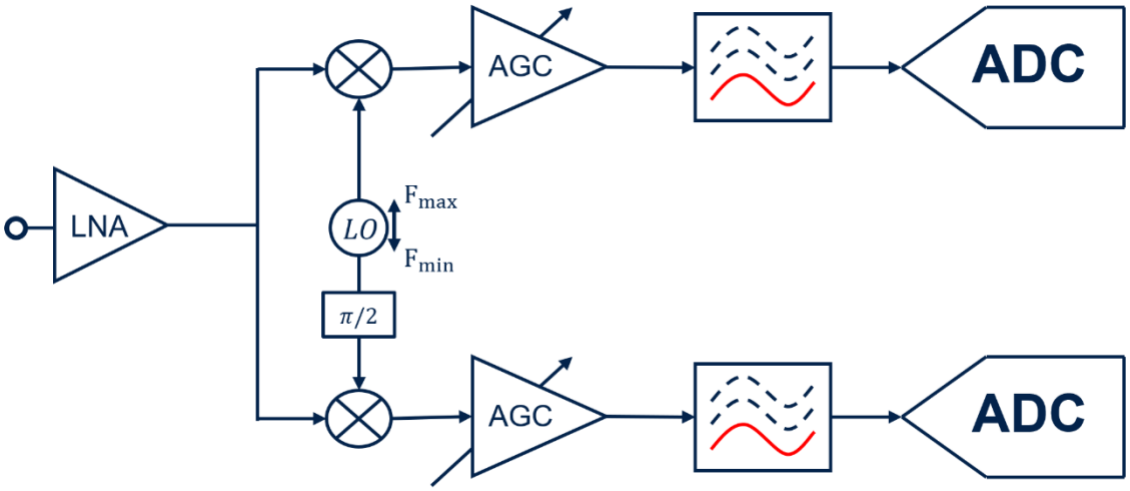

Figure 3 – Bock diagram of a superheterodyne receiver frontend

1.2 ADC in RF receiver chain

1.2.1 ADC key parameters

In a simplified approach, an analog to digital converter (ADC) is a linear transformer from analog signals such as voltage or current to the digital domain. The conversion is as foretold cadenced by a sampling frequency F_s with a given resolution defined by the minimal fraction of analog signal that can be discriminated called the quanta q. Consequently, a signal $S_n + \varepsilon$ should be converted at S_n as long as the relation $-\frac{q}{2} \leq \varepsilon \leq \frac{q}{2}$ is verified. If the quantization error ε can be seen as uniformly distributed across the quantization interval, the mean-squared value of ε will then be:

$$E(\varepsilon^2) = \frac{1}{q}\int_{-\frac{q}{2}}^{\frac{q}{2}} \varepsilon^2 d\varepsilon \tag{1.1}$$

From equation (1.1), it is commonly admitted to define the rms quantization error voltage as $e_{qns}^2 = E(\varepsilon^2)$. By solving the integral, we can define:

$$e_{qns}^2 = \frac{1}{12} q^2 \tag{1.2}$$

Because an ADC is an amplitude quantized system using n binary weighted bits quantization levels, in the case of a large pure sine signal, its maximum peak-to-peak amplitude can be defined as:

$$A_{pp_{max}} = 2^n q \tag{1.3}$$

With equation (1.2) and (1.3) the maximum signal to quantization noise ratio can be expressed in linear domain and in decibels as:

$$SNR_{RMS} = 2^n \sqrt{1.5} \;\; \rightarrow \;\; SNR = (n * 6.02 + 1.76)\, dB \tag{1.4}$$

Other noise sources in the conversion process contribute degrade the SNR from its theoretical value. From a general point of view, the SNR is described as:

$$SNR = 20. \log\left(\frac{S}{N}\right) dB \tag{1.5}$$

With S being the RMS value of the maximum signal and N representing the total RMS noise power including the quantization noise. Furthermore, the converter also presents non-linearities impacting the signal integrity. Non-linearity create spurious signals in the converted spectrum. It is commonly admitted that the total harmonic distortion (THD) allows to appreciate the non-linearity of a converter. This parameter is obtained by a FFT spectrum analysis of the converter output for a pure sine input. With a pure sine input, only the fundamental tone of the sine must be visible, but the non-linearity induced by the ADC create harmonics of the input. The definition of the THD is then:

$$THD = 10 \log\left(\frac{A_F^2}{A_{H2}^2 + A_{H3}^2 + A_{H4}^2 + \cdots}\right) dB \tag{1.6}$$

With A_F^2 representing the power of the fundamental tone and A_{Hx}^2 representing the power of the x^{th} harmonics. Combining SNR and THD allows to define a global performance parameter called the signal to noise and distortion ratio (SNDR) as:

$$SNDR = -10 \log\left(10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}}\right) dB \tag{1.7}$$

The SNDR measures the ratio of the power of wanted signal and the power of all unwanted signals. This parameter gives a good indication of the overall performance of an ADC. The value of the SNDR can be expressed as an equivalent number of bits :

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.8}$$

The ENOB allows to express the performance of an ADC by expressing the SNDR in the same domain as the main specification of an ADC, i.ex. the theoretical resolution expressed as the number of bits.

1.2.2 Interaction between ADC and RX front end

From the discussion above it has been discussed qualitatively the implications between sampling frequency and filtering, the correlation between gain and SNR, this section goes more deeply into dimensioning the RX front-end taking account the ADC parameters.

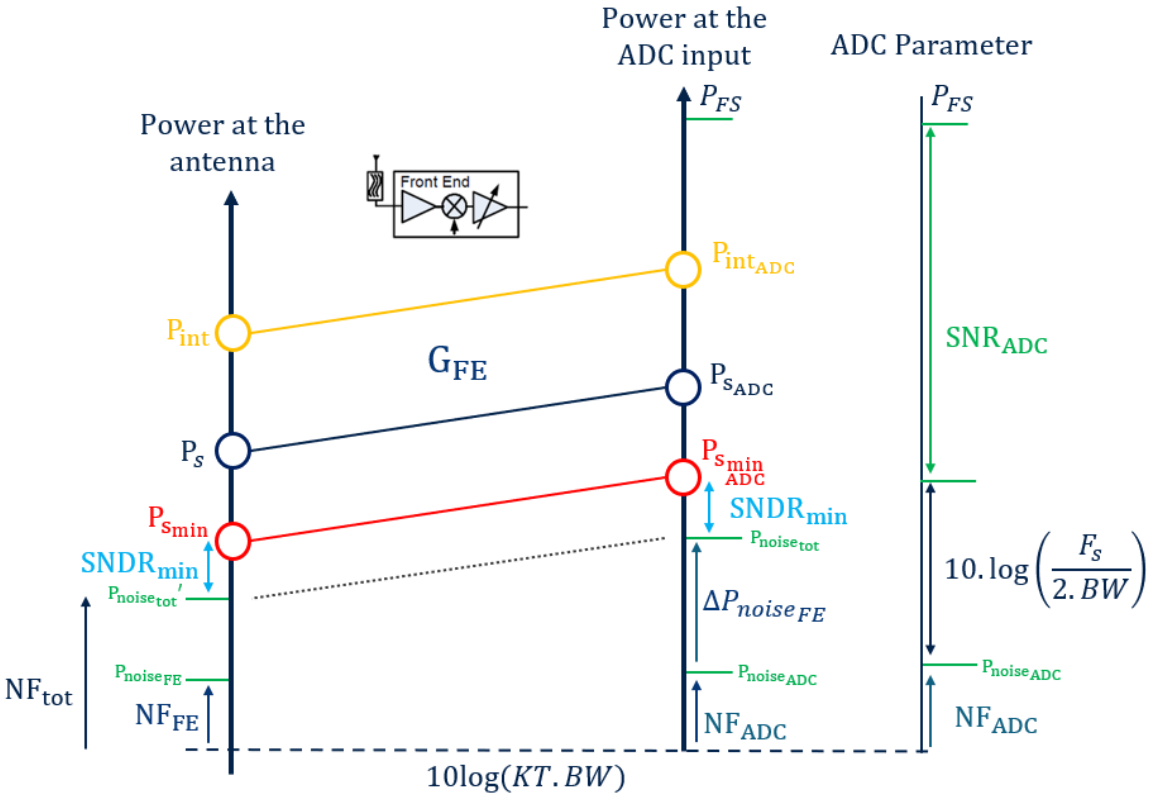

Figure 4 – Inspired from *[9]* Receiver signal, noise flow diagram and ADC parameter

Figure 4 shows the transcription of parameters as SNDR from the ADC to the receiver chain [9]. On the left of the figure is drawn the power presented at the antenna with different notable values. The example of the Figure 4 presents a interferer power, the wanted signal power and the minimum power accepted by the system $(P_{Int}, P_s, P_{s,min})$. The NF of the front-end is brought back to the antenna and

scaled with the thermal noise of the antenna, which allows to represent the power of noise induced by the analog front end $\left(NF_{FE}, P_{noise_{FE}}\right)$. After gain consideration (G_{FE}), the power of different input components are represented at the input of the ADC. . The noise added by the ADC (NF_{ADC}) is represented from the thermal noise and added to the noise brought by the front end to obtain total noise $\left(P_{noise,_{tot}}\right)$. A minimal SNDR is given by the digital section of the system regarding the protocol and BER targeted $(SNDR_{min})$.

This kind of translation admits that noises are uncorrelated, but it allows to dimension the chain in term of noise figure (NF), and gain. By construction ADC are highly linear blocks, the challenges for the chain regarding the IP3 and linearity consideration for example are for block above ADC. But to dimension the gain of the chain for a given minimal power at the antenna, the SNR of the ADC is key parameter as translated to the NF_{ADC}. Increasing the SNR of the ADC can allow to relax the NF or to reduce the gain of the front-end chain or a mix of both. Careful system level design and optimization of the system is required to minimize the power consumption of the RX front end.

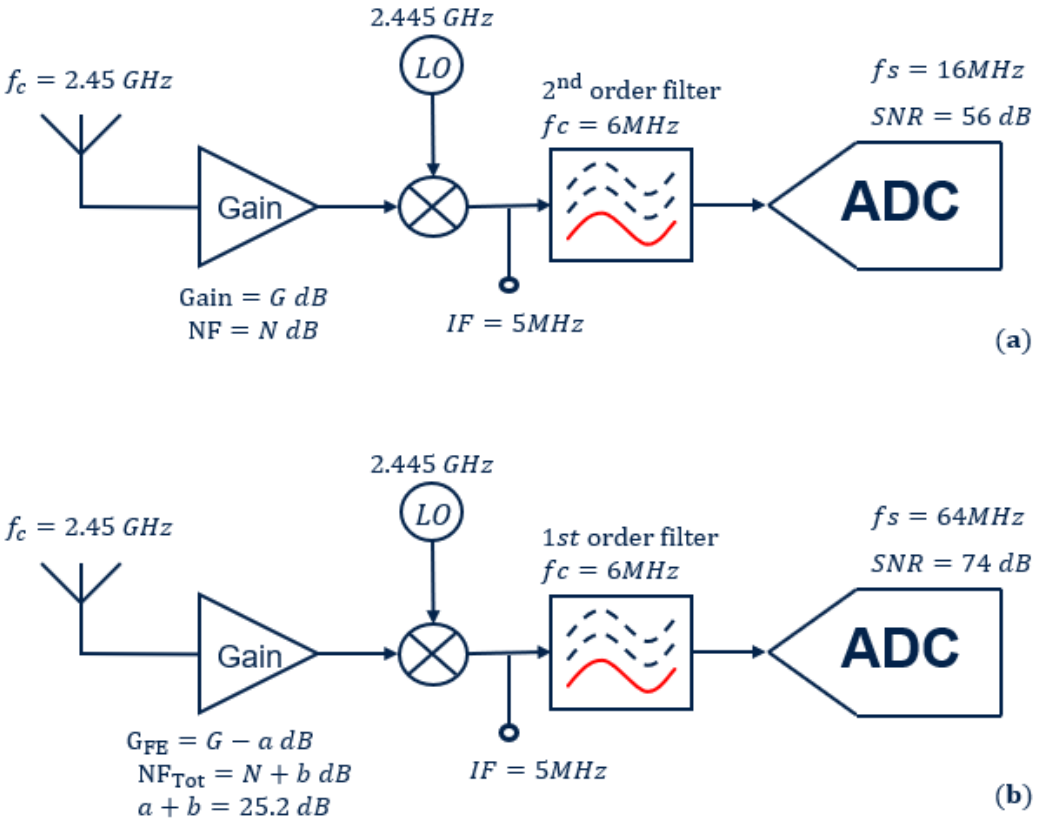

Figure 5 - Example of tradeoff between RF front end and ADC
(a) ADC relaxed
(b) Front-end relaxed

On Figure 4, these system elements are aligned with key parameters of the converter in regards of RX chain interaction. As represented on the right of Figure 4, the noise of the ADC depends on its resolution (SNR), its oversampling ratio by the term $10\log\left(\frac{f_{sample}}{2.BW}\right)$ and the noise floor as $NF_{adc} = P_{FS} - SNR_{adc} - 10\log\left(\frac{f_{sample}}{2.BW}\right)$. From those elements with given specifications for the RX chain it's possible to draw tradeoff between RF front end and ADC.

In Figure 5 are drawn two simplified RX chains with the same specification, carrier frequency at 2.45 GHz, IF at 5MHz, BW = 1MHz and $P_{FS,adc} = 8\text{dBm}$. Let's assume that the $SNDR_{min}$ is the same for both structures. As seen on Figure 4, $SNDR_{min}$ could be written as $SNDR_{min} = P_{FS,adc} - SNR_{adc} - 10\log\left(\frac{f_{sample}}{2.BW}\right) - NF_{tot} - G_{FE}$. To relax the constraints on gain and noise, the Figure 5 (b) proposes an ADC with 18 dB more on its SNR than Figure 5 (a) and a sampling frequency 5.3 times greater which make a gain of 7.2 dB SNR through OSR. For the same $SNDR_{min}$, and for the same performances as a system, 25.2 dB can be divided between front end elements allowing more noise in the front end or gain reduction. In terms of filtering, the second order filter required in Figure 5 (a) can be replaced by a first order filter with same cut frequency. Attenuation is then increased by ~9 dB as for the second order filter at 16MS/s: $att_{mirror,16M} = -40\log(16M - 5M) + 40\log(6M) - 3 \approx -13$ dB and for the first order filter at 64MS/S : $att_{mirror,64M} = -20\log(64M - 5M) + 20\log(6M) - 3 \approx -22$ dB

To resume this example, by adding 3 bits and multiplying the sampling frequency by 4, the front end can reduce its gain and increase its NF in a range of more than 25 dB. The antialiasing filter could go through a second order to a first order for the same cutoff frequency and attenuation is still greater. This shows the impact of the ADC performances on the chain sizing.

The aspect of ADC's distortion hasn't been discussed here because the main concerns are about really small signals.. In the context of this work and as represented on Figure 3, an automatic gain control is present before the converter and assure that no strong signal is presented at the input to avoid saturation of the converter.

1.2.3 ADC Specifications

As said in introduction, nowadays receivers are drowned in a crowded spectral environment. Different protocols coexist at the same time and share bandwidth with adjacent channels. This is really challenging for the receiver chain because those adjacent signals are close to the bandwidth of interest, so hard to filter, and could be more powerful than the wanted signal. The receiver chain must be resilient to this kind of situation, and the standards give the requirements in terms of perturbation by a in band

interferer [1]. With the requirements of the standard it's possible to give a minimum SNR for the converter. On Figure 6 is represented how to translate this to the ADC parameters [9]. The SNR is shown as:

$$SNR_{ADC} = P_{FS} - Margin - \left(\frac{I}{C}\right) - SNR_{Min} \tag{1.9}$$

where I/C is Interfere to Carrier power ratio and SNR_{MIN} is minimum SNR required for signal decoding. A Margin is added to account for channel variations and allows some headroom for the automatic gain control.

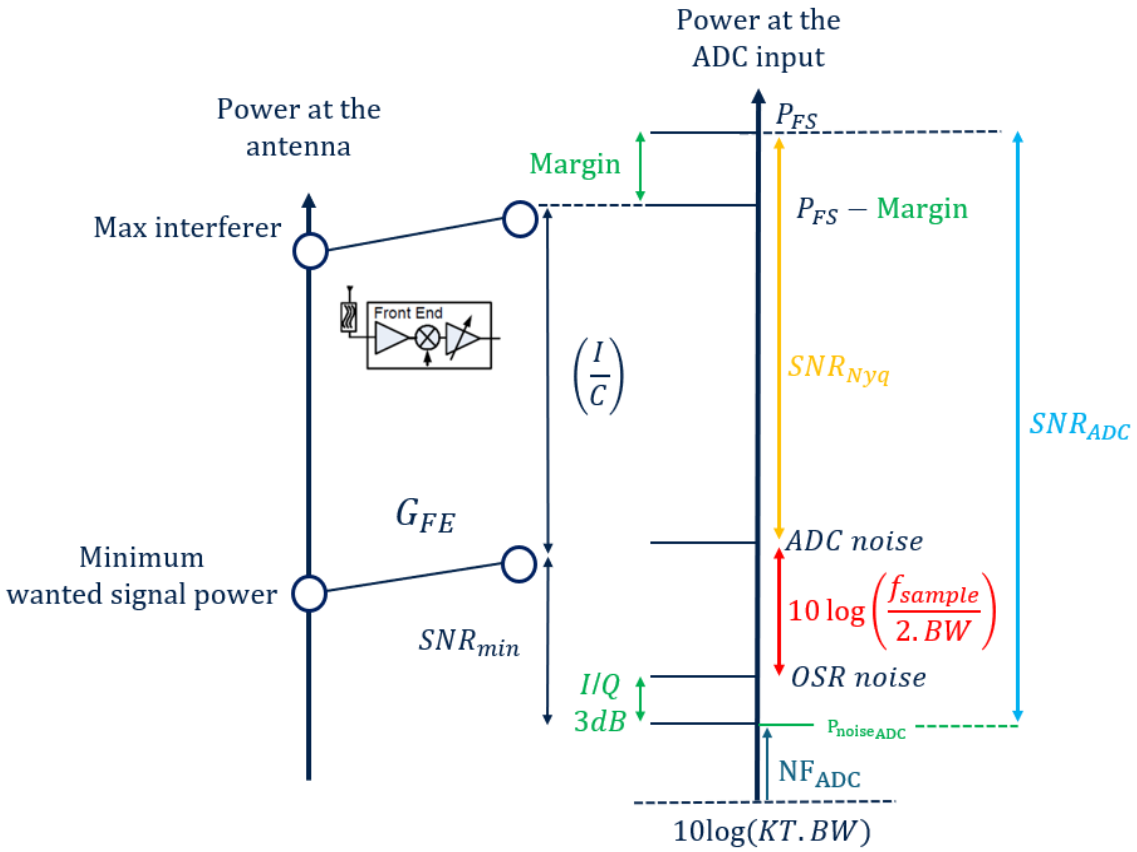

Figure 6 - Dimensioning of the minimum SNR compared to the I/C standard requirement.

Because of confidentiality on the STMicroelectronics products development, no details can be given for the different values for the reference case. With the given values in the worst case of interferences the calculation shows that the SNR at Nyquist frequency of the ADC must be at least 67 dB. This result comes from the analysis described in Figure 6 and is computed with a sampling frequency of 64MS/s for a signal bandwidth of 100KHz.

With front-end and system on chip (SOC) tradeoff considerations the objective has been fixed on a 12 bits ADC with a sampling frequency of 64MS/s . From the previous generation of ADCs this will bring resilience to interference by increasing the sampling frequency. Also relax the design of the front-end and bring more flexibility in digital signal processing (DSP) by increasing the resolution. The power consumption is targeted to 300µW. The target specifications are summarized in Table 1.

Table 1- Specifications of the aimed ADC for this work

ADC number of bits	12
Sampling Frequency	64MHz
SNR	67 dB
SNDR	65 - 67 dB
Power consumption	< 300µW

1.3 Survey of ADC state of the art

1.3.1 Metrics and tools to compare.

A large variety of ADC architectures exists addressing different types of specifications. To guide the architecture choice for this work, a first comparison of these architecture with relevant metrics is useful as good metrics to compare them. Commonly used metrics are the figure of merit (FOM) of Schreier and the figure of merit of Walden. Both metrics are attempts to allow performance comparison between very different implementations independently of the specific resolution or sampling frequency of a particular implementation.

The first FOM proposed by Schreier [10] quantifies performance by associating effective conversion range and ratio of bandwidth and power consumption. The ratio is described in a log function to express the value in dB. A higher value of the FOM indicates better performance. This FOM underlines the capacity of a converter to reach high effective resolution and while consuming low energy for a conversion while regarding the sampling frequency used. It is usually described as :

$$FOM_{Schreier}[dB] = SNDR[dB] + 10\log\left(\frac{f_{sample}[Hz]}{2.P[W]}\right) \quad (1.10)$$

Where P represents the power consumed in watt, this figure of merit allows to underline the tradeoff between SNDR and consumption. At the beginning of this work the envelope (best performance presented in state of the art) of this figure of merit was 185 dB.

The second, FOM Walden quantifies the energy consumed by the converter and compare it with its effective resolution (ENOB). The energy is calculated with the ratio of the power consumption and the sampling frequency, representing the energy consumed for one conversion divided by the effective number of codes (2^{ENOB}) of the ADC. A lower FOM expresses higher performance in terms of the energy efficiency of a design with respect to its effective resolution. This FOM is defined as:

$$FOM_{Walden}\left[\frac{fJ}{conv}\right] = \frac{P[fW]}{2^{\frac{SNDR\,[dB]-1.76}{6.02}} f_{sample}[Hz]} \tag{1.11}$$

In the Walden's FOM, the energy per conversion is expressed in fJ which close to the order of magnitude of the best ADCs at this time. This FOM_{Walden} is mostly used to compare high data rate converters. The envelop (best performance presented in state of the art) from the beginning of this work was $1\,\frac{fJ}{conv}$.

The specifications presented in Table 1 considered with 300µW of power consumption presents a $FOM_{Schreier} = 177.3$ dB and $FOM_{Walden} = 2.3\,\frac{fJ}{conv}$.

1.3.2 Graphs and architectures

To compare the described specification with state of the art realizations, the Boris Murmann survey on the ADC is used. This is a useful tool to compare existing ADC realized on silicon, the survey references only ISSCC and VLSI production on converter. In its 2020 version [9], this survey gives a picture of the state of the at the beginning of this work.

The described FOMs of the survey data can be plotted as a function of the sampling frequency as shown in Figure 8 and Figure 7. These figures of allow to place the proposed specification on the graph. The orange circle shows with some margin the target performance compared to other realizations.

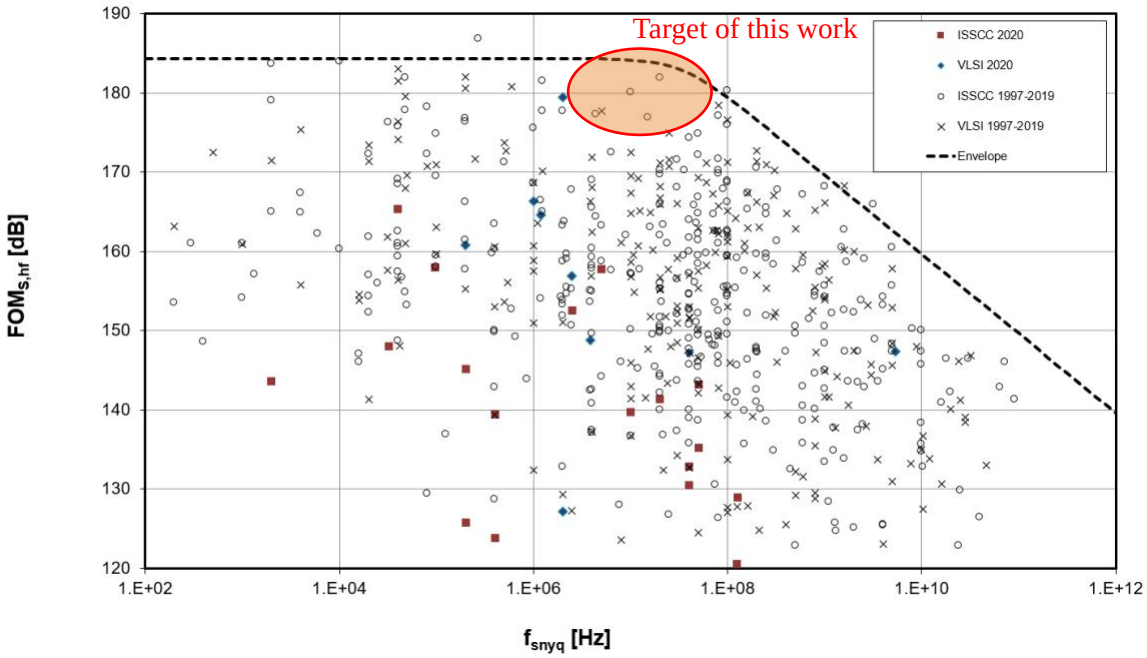

Figure 8 - Schreier FOM plot compared to sampling frequency (1997-2020) from [11]

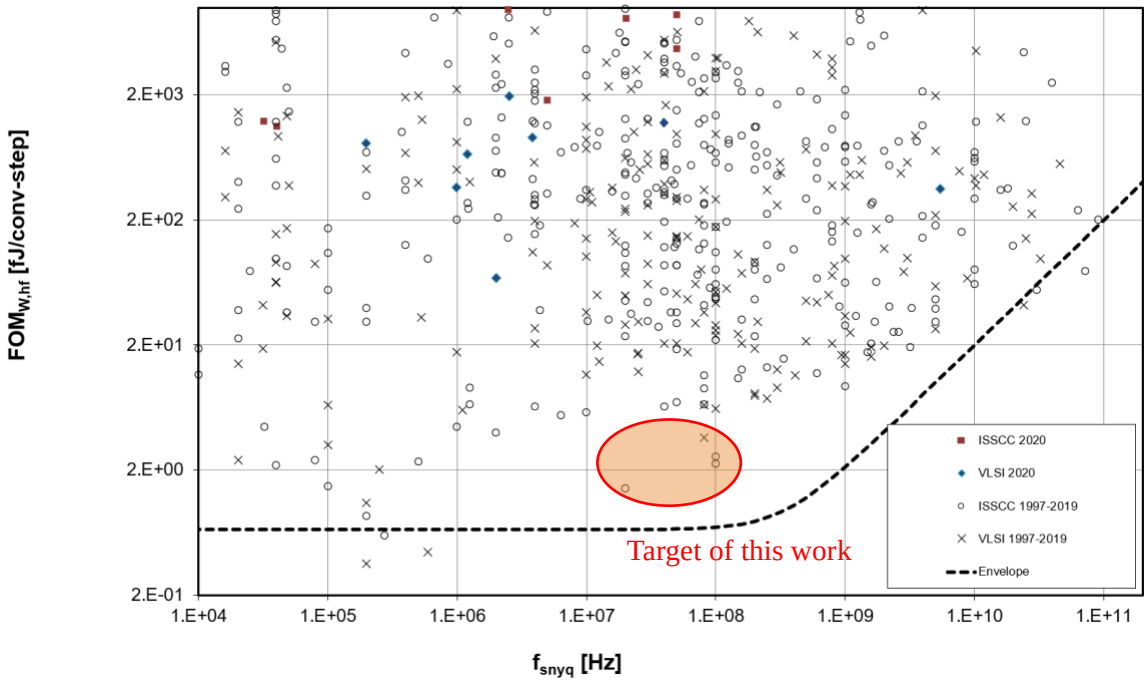

Figure 7 - Walden FOM plot compared to sampling frequency (1997-2020) from [11]

The target specification challenges the state of the art as shown on Figure 8 and Figure 7.

The next chapter will go deeper into the study of ADC architectures and 2020 state of the art to underline the direction taken to address the given specifications.

Chapter 2

State of the Art

2.1.1 MAIN ADCS ARCHITECTURES 34

2.1.1 FLASH, OVERSAMPLED, AND PIPELINED ARCHITECTURES 34

2.1.1.1 Flash Topology 35

2.1.1.2 $\Sigma\Delta$ topology 36

2.1.1.3 Pipelined topology 38

2.1.2 SUCCESSIVE APPROXIMATION REGISTER (SAR) 40

2.2 QUANTITATIVE ANALYSIS OF THE ADC SURVEY 45

2.2.1 OVERALL SURVEY, SILICON MEASUREMENTS FROM [11] 45

2.2.2 OVERALL SURVEY, FILTERED SILICON REALIZATIONS 46

2.3 HYBRID SAR ARCHITECTURES 48

2.3.1 HYBRID SAR PIPELINE 48

2.3.1.1 Amplify and quantize the residue 48

2.3.1.2 State of the art performance 49

2.3.2 HYBRID SAR NOISE SHAPING 50

2.3.2.1 Noise Shaping SAR (NS-SAR) Overview 50

2.3.2.2 State of the art performance 51

2.3.3 TIME-BASED APPROACHES TO HYBRID SAR ADCS 53

2.3.4 HYBRID SAR TDC [69] 54

2.3.4.1 Overall architecture 54

2.3.4.2 Performances and drawbacks 55

2.3.4.3 Calibration and repeatability 56

2.3.5 HYBRID SAR DS [3] 57

2.3.5.1 Overall architecture 57

2.3.5.2 Advantages and drawbacks 59

2.4 CONCLUSION 60

2.1.1 Main ADCs Architectures

2.1.1 Flash, oversampled, and pipelined architectures

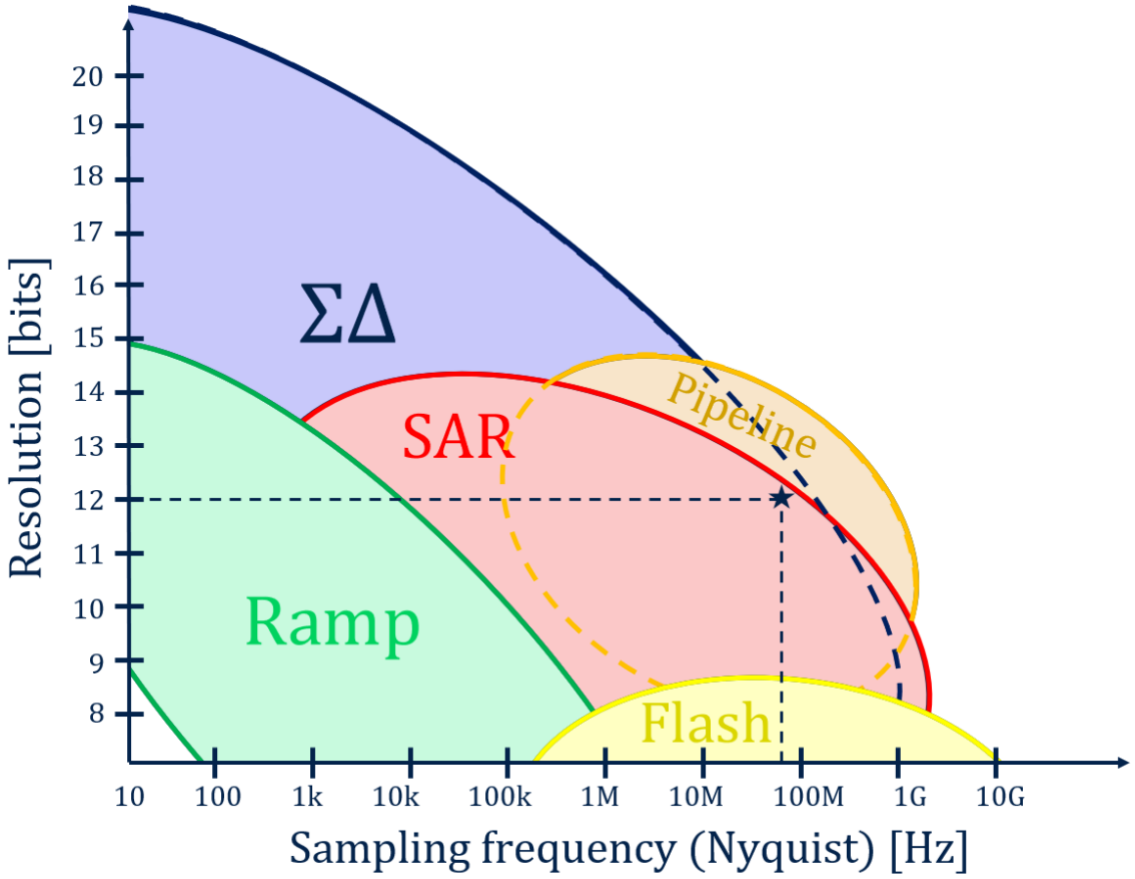

Figure 9 - Main performance trends of ADC topologies, inspired by *[31]*, with data of *[12]*. The star symbol identifies the target specifications for this work as defined in chapter 1.

It is well known that in analog to digital conversion, some concepts have been so widely used that they are today classified in different topologies called main architectures. A survey of different ADC realizations published in ISSC and VLSI held by Boris Murmann [11] has been used at the beginning of this work in 2020, the version updated in 2023 is referenced as [12]., This chapter shows the challenges with respect to the state of the art in terms of architecture to meet the target specifications set for the this work. The main questions of this chapter are: What is the best topology to resolve the specification given in chapter 1? Can it be designed to meet industrial constraints? What improvements can be applied to the most relevant architectures to make them more effective in regard of the target?

Figure 9 shows the main architecture suitable for the target specifications in terms of resolution and bandwidth. Power consumption, area, linearity etc. are not considered at this stage. With 12 bit and

64MS/s as target, the SAR, the Pipeline, and the sigma-delta (ΣΔ) topologies seem to able to reach this area in terms of speed and precision. Because Figure 9 is an approximative representation of what is possible, the following sections will outline the challenges of each architecture, and how to find the good structure, if there is one.

2.1.1.1 Flash Topology

The essence of a flash architecture is to instantly compare the input signal to every discrete level possible in the ADC resolution. This means 2^n different voltage level for a n bit converter. Generating those voltages and comparing the signal with precision consumes energy proportional to the number of levels. So, the power consumption grows exponentially with the resolution [13].

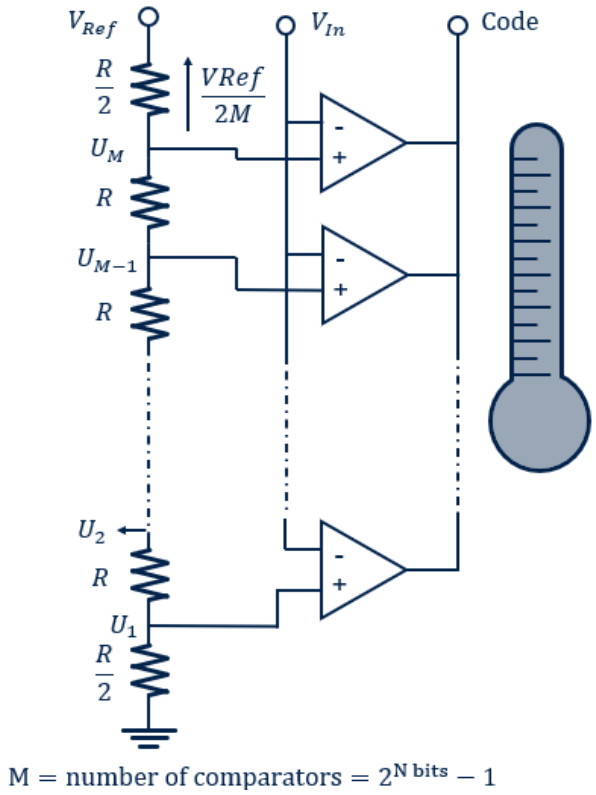

Figure 10 - Concept representation of flash ADC

On Figure 10 is represented a simple flash as described previously. The input is compared with every voltage equivalent to a code. This is described as thermometric code because similarly to a thermometer, the number of outputs with code 1 grows proportionally to the input voltage. Every code below the input equivalent code would be set as a "1", and every greater code would be set as a "0".

Some technics as folding or interpolating presented in [14] brought higher resolutions without exponential growth of the circuit complexity. In the context of this work, silicon realizations aimed for wireless

communication present good performances [15] but still a consumption of several hundreds of milliwatts which is not the target of this work. This type of structure is fast by construction, as shown in [16] reaching 2GS/s without interleaving, but consuming ~20mW for 6.5 bits ENOB. This is beyond the total energy budget of a complete receiver chain.

Table 2 - Flash ADCs in the literature

Ref.	Architecture	Techno [nm]	F_{snyq} $[Hz]$	Res.	SNDR [dB]	Supply [V]	Power [W]	FOMs [dB]
[14]	Folding and interpolation	1000	50M	12	63.6	5	300m	142.8
[15]	Folding and interpolation	600	50M	12	64	3.3	850m	138.6
[16]	Flash	65	2G	8	40.7	1.3	21m	171.8

Table 2 draws performances of previously cited realizations, showing a non-exhaustive picture of the possibility in state of the art for flash ADC.

From this analysis, it can be concluded that this architecture is not suitable by itself for the application of this work.

2.1.1.2 ΣΔ topology

The concept of Oversampling (OS) can be used most of the classical topologies. One of the main advantages of having a sampling frequency greater than the target bandwidth is to reduce the power spectral density of the noise in the band after filtering [13]. This method increases the ENOB by ~X bits where $X \approx \frac{OSR}{4}$ and OSR defines the oversampling ratio as $OSR = \frac{fs}{2*BW}$, where fs is the sampling frequency and BW is the bandwidth of the signal to convert. From this point reaching high resolution with oversampling looks easy but to get for example 16 more bits the OSR must be $\sim 4^{15}$ so an order of magnitude of 10^9 which doesn't look a so good trade-off after all. From this observation, different

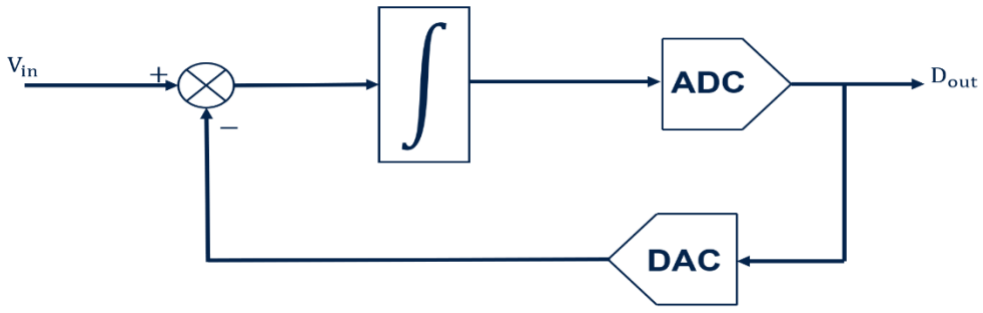

Figure 11 - Simplified block representation of a *ΣΔ* ADC

variants have been proposed and sigma-delta (ΣΔ) modulation is the most widespread one [17]. The main idea of the sigma-delta (ΣΔ) modulator is to shape the quantization noise. A ΣΔ modulator as drawn on Figure 11 has a feedback loop that subtracts previous output from the input. Because of the OSR, the wanted signal at the input can be considered constant for several clock cycles. At each clock cycle, the feedback loop subtracts the last quantified input from the current input with a low resolution. Because the wanted signal is considered static, each conversion represents successive quantification error for the current input. With the integrator in the forward path, the system behaves as a low pass filter for the input signal and as a high pass filter for the feedback loop. Because the feedback loop propagates the quantification error, the quantization noise is attenuated at low frequencies. The ΣΔ modulator presents thus two different transfer functions, one for the signal and one for the noise, respectively called STF and NTF. Applying a dedicated transfer function to the noise (NTF) is called noise shaping. The presented ΣΔ modulator in Figure 11 is thus a low-pass type oversampled architecture, the wanted signal bandwidth is at low frequency where the power of the noise is decreased by the noise shaping. The ΣΔ modulator increases the benefits of the OSR by concentrating the noise power spectral density at high frequency. After eliminating the high frequency noise by digital filtering, the SNR at the output is enhanced in the bandwidth of interest. The impact of system non idealities such as matching or offset are also reduced because these are in the feedback loop also noise shaped. As discussed in the previous chapter, increasing the sampling frequency as it is mandatory to reach OSR benefits, also relaxes the constraint of the antialiasing filter in front of the ADC.

In comparison with previous example, for the same target of a +16 bits of ENOB, a first order ΣΔ modulator needs an OSR of "only" 1663 compared to 10^9 [10] for a 1 bit flash converter. Nevertheless, to limit the sampling rate, the OSR must be reduced. In order to keep high SNR the order of the ΣΔ modulator can thus be increased by adding more integrator stages in the forward path but at the cost of degraded stability [18] [19] [20]. Another topology composed of cascaded stages of low order ΣΔ modulators (called MASH) [21] address the stability problem by making it dependent of the individual sub modulator stability [22]. In the MASH architecture, the digital output of each sub modulator is treated by a dedicated digital filter and the global performances depend on the matching between digital and analog filter for each sub modulator [23].

For radio targets, some realizations use continuous time ΣΔ modulator (CT-ΣΔ) as converter which relaxes the front end design discussed in Chapter 1 [24] [25]. The CT-ΣΔ modulator reproduces the system presented in Figure 11 but in continuous time [26]. In classical ΣΔ modulator implementations, the sampling is done before the integrator function, in CT-ΣΔ sampling occurs after the integration states. This means that the output of the integrator is continuous which brings

useful properties such as a built-in antialiasing behavior [10]. However, the CT-ΣΔ modulator suffers from many non-idealities as excess delay in the quantizer, time constant variation in the loop filter, clock jitter and so forth.

Table 3 draws performances of previously cited realizations, showing a non-exhaustive picture of the ΣΔ state of the art (F_{snyq} represents the equivalent Nyquist frequency).

Table 3 - ΣΔ ADCs in the literature

Ref.	Architecture	Techno [nm]	$F_{s_{nyq}}$ $[Hz]$	OSR	SNDR [dB]	Supply [V]	Power [mW]	FOMs [dB]
[19]	ΣΔ	130	10M	8	70.7	1.2	8.1	158.6
[21]	2nd Order MASH ΣΔ	600	2.5M	8	89	5	550	152.6
[23]	1-0 MASH ΣΔ	65	30M	8	64	1.25	37	150.1
[25]	3rd Order CT-ΣΔ	65	2M	4	67.4	1.3	0.131	166.2

To conclude this brief description of oversampling topologies underlining ΣΔ modulator implementations, there is a real interest in oversampling technics to reach requirements in terms of SNR. Moreover, noise shaping, cascaded structures, and continuous time approach increase SNR providing better stability and/or aliasing filtering which is an asset in the RX chain. Nevertheless, high OSRs induce constraints on the clock generation for a high bandwidth applications. A fast clock needs to be generated which can be a solid argument to not choose this topology in a SOC implementation. The consumption required for clock generation is not taken into account in Table 3.

Given the reported performances including power consumption indicated by the Schreier figure of merit, ΣΔ ADCs seem not to be the most suitable approach for the given application and specifications.

2.1.1.3 Pipelined topology

This pipeline architecture segments the conversion of the input into several steps done by successive stages. Each stage resamples the output of the previous stage allowing stages to work concurrently, each stage handling one portion of successive inputs. When the first stage is converting an input, the second is converting what the first left at the end of his previous conversion and so on. To realize this mechanism, the pipeline is built with a unit stage represented in Figure 12 Each stage samples its input, a sub-ADC converts this input with a defined resolution, the result is then converted back to the analog domain and subtracted from the sampled input giving what is called the residue. The maximum

amplitude of the residue is equal to one LSB step of the stage. The residue is then amplified to provide a full-scale input to the next stage.

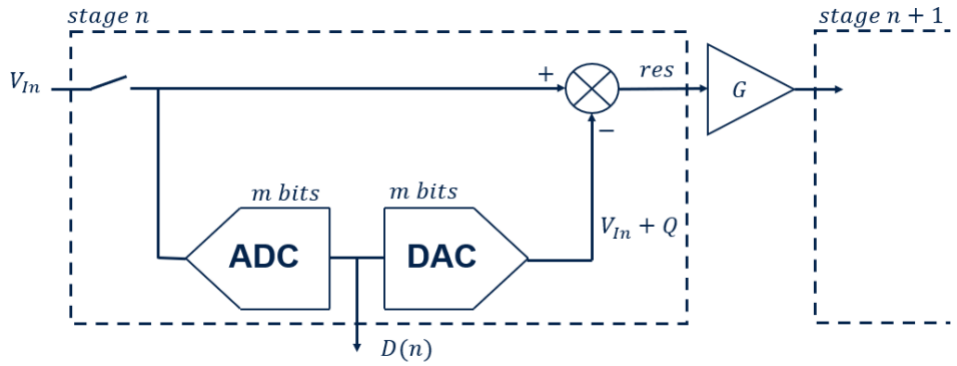

Figure 12 - Block diagram of a m bits unit stage in a pipelined ADC

Pipelining has the potential for reaching high conversion rates [27] [28] as each stage has a resolution of only a few bits. Pipeline ADC with 12-bit resolution at Nyquist is reachable [29] but the precise amplification is a major challenge (see explanations in [29]). Gain errors and non-linearities of the amplifiers can severely degrade the ADC performance. Background calibration as in B. Hershberg's work [30] is an approach relaxing the constraints by compensating errors in the digital domain.

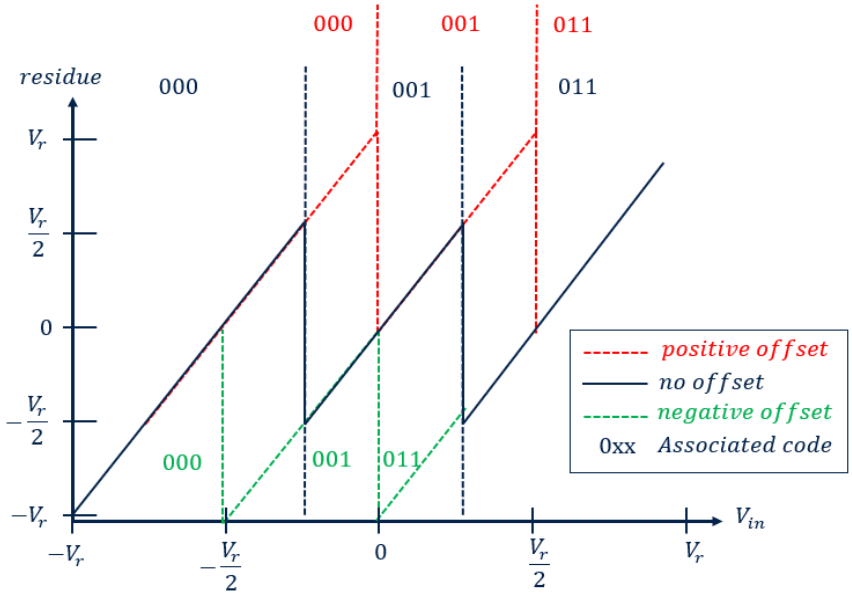

Figure 13 -Example of transfer function of a 1.5-bit pipeline stage introducing a redundancy of 0.5 bits

The introduction of redundancy (or overlapping) is another widespread technique to correct errors of a previous stage in the subsequent steps [31]. Figure 13 shows as an example the transfer function of sub-ADC stages with 1.5 bit dynamic. By adding 0.5 dynamic range to the individual stage, offset errors of up to $\pm\frac{V_r}{2}$ can be corrected with adequate digital recombination.

Pipeline topologies present further interesting features. As the signal is amplified at each stage, requirements in terms of noise performance of each stage can be successively relaxed along the pipeline because their contribution is divided by the gain of the previous stage. This allows to scale down the power consumption of the ADC. Selected pipeline ADC realizations are presented in Table 4. However, the Schreier figure of merit does not exceed 165 dB, even for recent implementations in 28nm technology. This is below the figure of merit needed for the low power communication application targeted in this work.

Table 4 - Pipeline ADCs in the literature

Ref.	Architecture	Techno [nm]	F_{snyq} $[Hz]$	SNDR [dB]	Supply [V]	Power [mW]	FOMs [dB]
[29]	Pipeline	180	30M	72	1.3	6	166
[32]	Pipeline	90	40M	71	1.2	47.3	157.3
[33]	Pipeline	28	280M	64	1	13	164.3
[34]	Pipeline	65	50M	67.7	1	4.07	165.6

2.1.2 Successive Approximation Register (SAR)

The successive approximation register is a very popular architecture based on a binary search algorithm. Figure 14 (a) presents a block diagram of traditional implementation of a SAR converter [35]. A CDAC (Capacitive Digital to Analog Converter) is used to sample the input signal then to perform the binary search algorithm. The CDAC is an array of capacitors sized in powers of 2 in regard of a unit capacitor (C_u), each capacitor corresponding to a bit weight for the conversion. For an n-bit SAR, capacitor values range from C_u to $2^{n-1}C_u$. A supplementary unit capacitor is present so that the total capacitance of the array is $C_{Tot} = 2^n \cdot C_u$. The top plates of the capacitors are connected to the comparator inputs, while the bottom plates are switched to the appropriate reference voltage.

Several switching schemes exist. Figure 14 (b) shows the so-called “Bottom-plate sampling” scheme. During the sampling phase the bottom plate switch is connected to the input while the top plate is connected to a fixed voltage (the ground in Figure 14). After the sampling phase the top plate of the CDAC is disconnected of the voltage source inducing a floating node voltage at the input of the comparator. The binary search algorithm drives the bottom plate switches starting from the MSB (most significant bit) to the LSB (less significant bit). Thanks to the charge conservation principle the floating

node voltage is equal to the difference of the reference voltage weighted by the CDAC input code and the input voltage. The comparator is used as an arbiter during the conversion process from MSB to LSB.

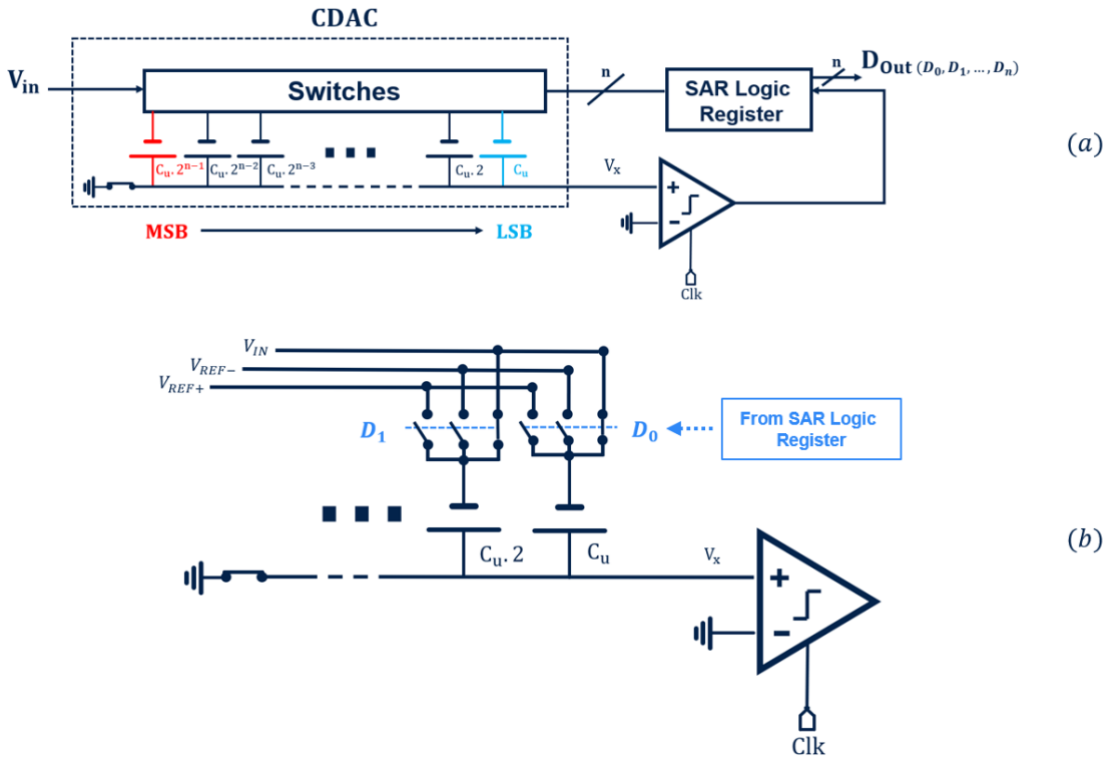

Figure 14 - Block diagram of a charge redistribution SAR ADC (a) zoom on switches (b)

The SAR topology is popular because no linear active analog blocks such amplifiers are required which places it in a favorable position for low power applications [36]. SAR ADCs are therefore digital friendly since the only analog block required is one comparator. This also comes with area reduction scaling well with technology node shrinking. Nevertheless, in regards of the performances targeted, the CDAC of the SAR represents a bottleneck requiring design considerations. By sampling the input in the CDAC, the thermal noise voltage of the sampling switch is integrated and added to the input voltage stored [13]. The rms value of this noise is defined as $\frac{K*T}{C}$, with K the Boltzmann constant, T the temperature in Kelvin and C the value of the total capacitance used to hold the input voltage. This well-known parameter can limit the level of integration and the speed of SAR ADC if a high total capacitance value is required in regard of the SNR target. Some technics such as split capacitors [37] have been introduced to reduce capacitor value without increasing the noise. However, the capacitances must present matching performances better than 1% for SAR up to 10 bits of ENOB with classical CDAC implementations (Figure 14) [38]. For split capacitor arrays the mismatch requirement is way more aggressive and requires calibration to reach an ENOB beyond 8 bits [39] [40].

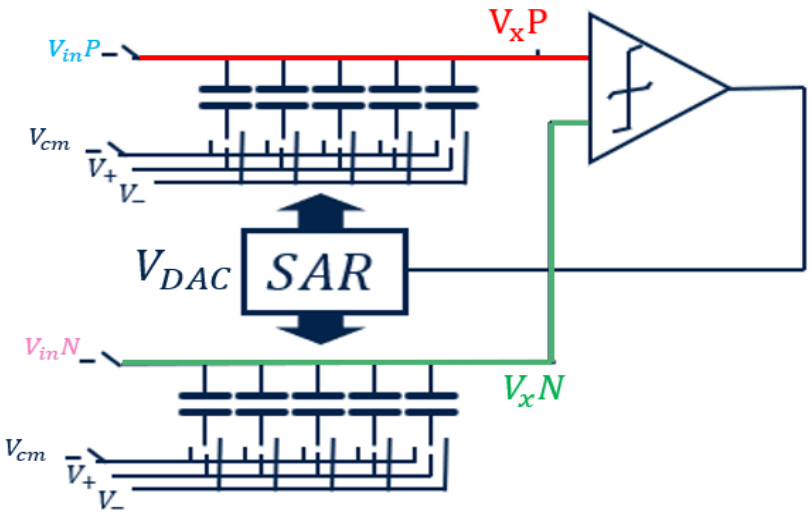

Figure 15 - Block diagram of a differential top plate sampling SAR ADC architecture

From the power consumption point, of view, the sampling strategy can be enhanced by sampling the input voltage directly to the input of the comparator, the so-called "top plate sampling". This widespread method represented on Figure 15 in a differential version reduces the energy consumed by the converter below the mW range [36]. Compared to "bottom plate sampling", "top plate sampling" allows to save one CDAC operation after the sampling phase. Indeed, the input voltage is directly set on the floating node at the end of the sampling phase. This allows top plate sampling topology to perform the MSB evaluation directly at the end of the sampling phase without CDAC switching. Another improvement compared to the classical approach is the use of a common mode voltage at half the voltage headroom instead of the ground. This will relax the system in terms of energy waste because the charge and the discharge of the capacitances are thus centered with respect to the voltage headroom. The common mode at the comparator input is set by the common mode of the differential input voltage in the sampling phase.

Figure 16 depicts an example of time operation occurring in a top plate sampling SAR conversion. After the sampling phase, the two input nodes of the comparator, called here V_xP and V_xN, become floating. The first comparison is done immediately after the sampling [13], the result is transferred to the digital state machine implementing the SAR algorithm and the value of an internal variable represented as V_{DAC} is adjusted. V_{DAC} represents the reference voltage weighted by the current input code of the CDAC. This code converges along the successive operations to the value that minimizes the difference $V_{in}-V_{DAC}$. Without error along the conversion, the voltage from the CDAC can be described with eq. :

$$V_{DAC}(x) = \frac{V_{fullscale}}{2^{x+1}}\, E\left[V_{in} \cdot \frac{2^{x}}{V_{fullscale}}\right] \tag{2.1}$$

With $V_{DAC}(x)$ the value of the converted voltage at the x^{th} operation amongst n, the $V_{fullscale}$ representing the voltage swing convertible by the SAR. $E[\,]$ describes the function $integer$, keeping only integer part of its input, and V_{in} representing the sampled input voltage. The sign of the floating node voltage, equal to $V_{in} - V_{DAC}(x)$, determines the value of the current bit in the code.

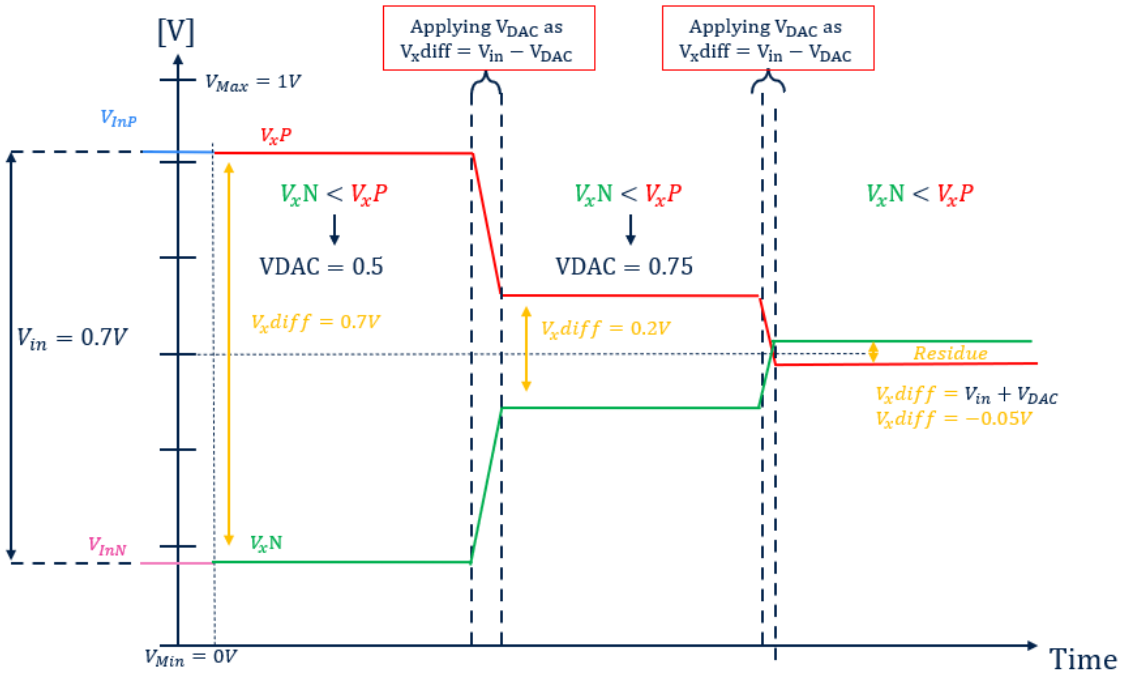

Figure 16 - Example of 3 bit differential SAR operation

Silicon realizations have demonstrated high speed capabilities reaching hundreds of MS/s [41], as well as resolutions of up to 86.7 dB SNDR [42] thanks to calibration strategies of undesirable phenomena. Also, low power consumption can be achieved with realizations consuming less than 600µW for targeted specifications [43]. The high figures of merit of the most remarkable SAR realizations show the interest of the SAR architecture for high performance ADCs in mid-range resolution and sampling frequencies.

Table 5 – Remarkable SAR ADCs in the literature

Ref.	Architecture	Techno [nm]	F_{snyq} $[Hz]$	SNDR [dB]	Supply [V]	Power [W]	FOMs [dB]
[36]	SAR	40	1M	68.1	1.1	31µ	170.2
[42]	SAR	180	6k	86.9	1	468n	184.95
[43]	SAR	40	40M	69	-	591µ	174.3
[44]	SAR	65	1M	54.4	1	1.9µ	168.6

Nevertheless, challenges remain to meet the targeted performance of this work. One of the key elements in the SAR is the clocked comparator. The dynamic comparator based on the strongARM latch [45] [46] enabling fast decisions thanks to its strong positive feedback and its full swing outputs is widely used. It also has no static power consumption. The dynamic power consumption of the comparator still depends on speed and noise requirements. This limitation has been underlined in Bindra publication [47] which proposes a novel dynamic bias architecture. However, energy consumption per comparison is still too high to reach the targeted efficiently with simple SAR architecture [48].

In consequence reach 12 bit at 64Ms/s and power consumption below 300µW is difficult to reach with a simple SAR [47] [49]. To overcome this challenge, dynamic comparator biasing has been proposed [50]. By tolerating high noise levels of the comparator on the first comparisons, the power consumption is reduced. However, decision errors are introduced that can be later on corrected thanks to built-in redundancy [50] [51]. SAR topologies also suffer from energy lost in the CDAC during the conversion. Capacitances are charged to the input, then the binary algorithm makes charges move at every comparison, losing a lot of energy displacing charges the same way for every input even when it's not needed. Proposals to overcome this energy waste have been presented in [52] or [53] by adding more steps or more comparators with different threshold voltage. This allows to reduce the power consumption of the CDAC by up to 40%. Furthermore, architectures combining the SAR ADC with other ADC structures for the LSB stages, so-called hybrid SAR ADCs, allow significant performance enhancements.

The next section will present a quantitative analysis of reported ADCs base on data from [11] collected amongst VLSI and ISSCC ADC publications.

2.2 Quantitative analysis of the ADC survey

2.2.1 Overall survey, silicon measurements from [11]

Based on data from [11] at the time of the start of this PhD thesis, Figure 17 plots silicon realization from 1997 to 2020. The Y-axis represents the ratio between power and the effective bandwidth while the X-axis represents the SNDR. From this figure the target of the thesis can be clearly placed on the graph. It can be seen that only few realizations are close to the targeted performances.

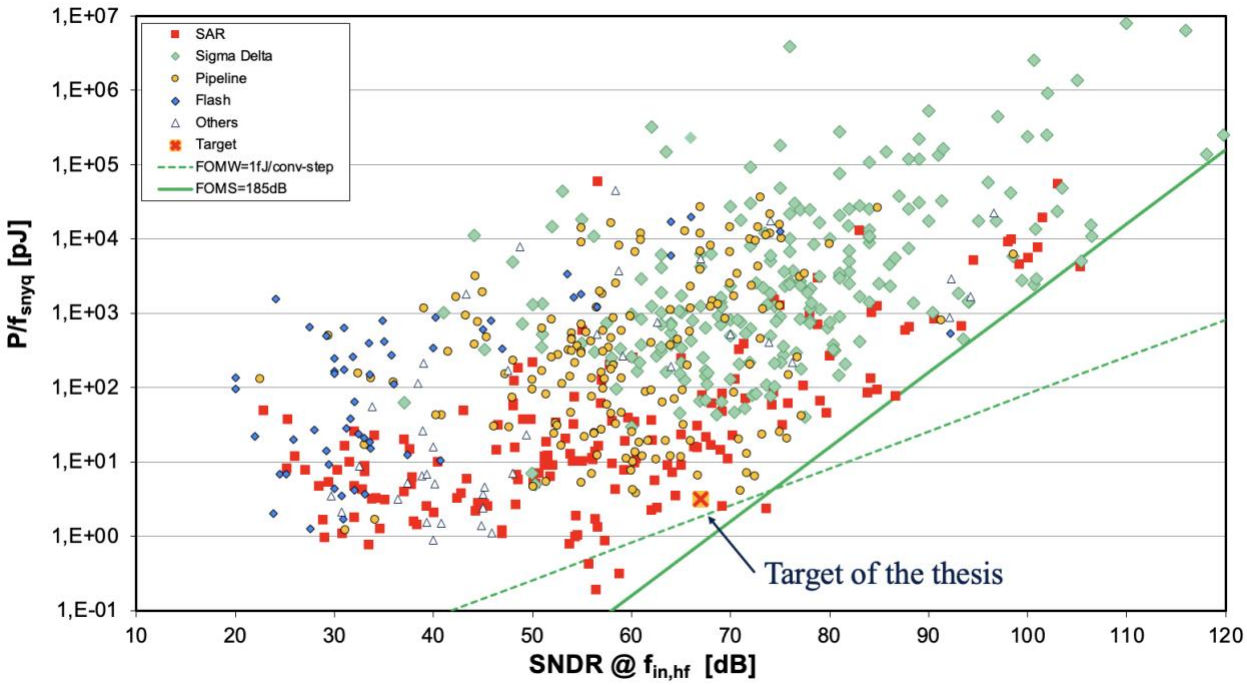

Figure 17 - Quotient of power over the frequency compared to SNDR on the whole B. Murmann Survey.

Figure 18 completes Figure 17 showing the frequency used for the measurements of the ADCs called $f_{in,hf}$, corresponding to the Nyquist equivalent frequency. It is important to specify this parameter while comparing oversampled and Nyquist architecture.

From this figure, again, no clear conclusion can be draw while a lot of realization achieve the couple speed and resolution on Figure 18 but very few are close on Figure 17. This shows that the challenge is consumption. 300µW is aggressive for these specifications. To make this point more evident, a filter can be added to the previous figures.

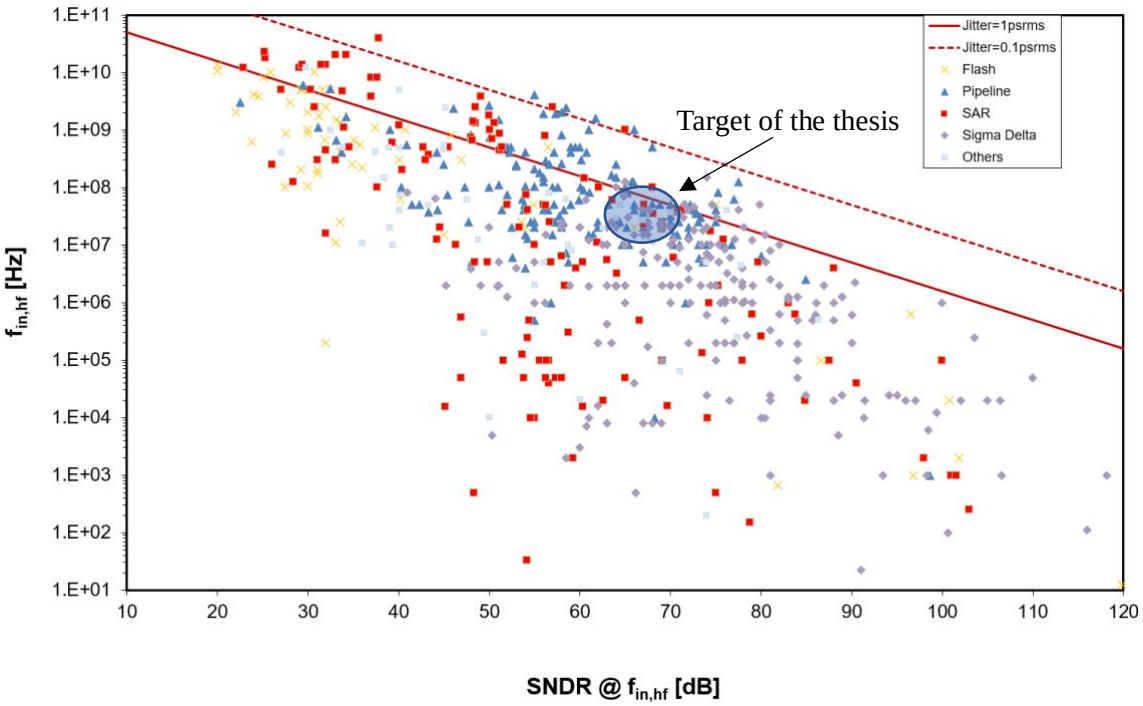

Figure 18 - Nyquist frequency compared to SNDR on the whole B. Murmann Survey.

2.2.2 Overall survey, filtered silicon realizations

The filters added to make more effective comparisons shouldn't be too restrictive to not miss an interesting realization too old to be competitive with new technologies nodes. First, only publications from 2002 to 2020 have been considered. Secondly, the SNDR had to be greater than 50 dB (8 bits of ENOB). And finally, the maximum power consumption was set to 1.5mW to approach the targeted performance with some margin. This selection performed in B. Murmann's data base decreases drastically the number of realizations to compare while maintaining a wide enough selection. Many implementations have been removed by the filtering process compared to Figure 17 and Figure 18.

Figure 19 and Figure 20 show that pipeline and flash realizations do not match the filter requirements and so have been automatically removed. SAR and ΣΔ ADCs are mainly represented with silicon already measured, but in the area spotted for the specification on both graphs, very few realizations are present. Nevertheless, the current plot (Figure 19 and Figure 20) classify ADC realizations with the major topologies. However, the individual realizations present numerous techniques to enhance the performance. These technics can be considered for the most interesting part as hybrid, taking advantage of multiple topologies combined in the same converter. The sigma delta converters are still shown on the plot but it is clear that the resolution targeted here is below the need of a sigma delta

topology in terms of SNDR. The main focus is therefore placed on SAR based converter and the next section details the principal hybrid architectures present in the survey data in [11].

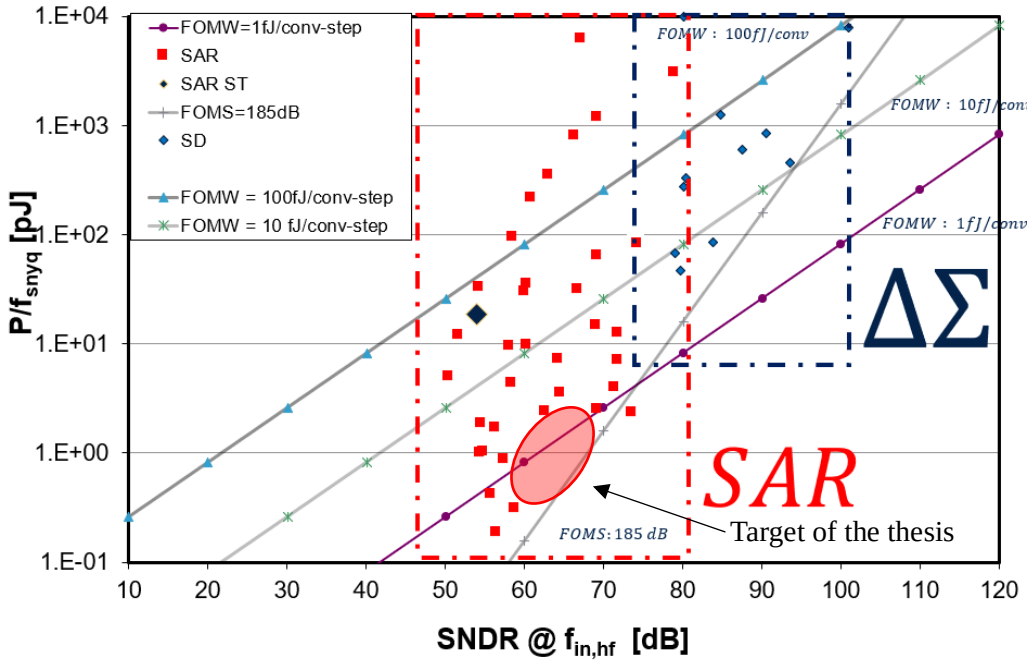

Figure 19 - Plot of filtered ADC - Power/Frequency in function of the SNDR

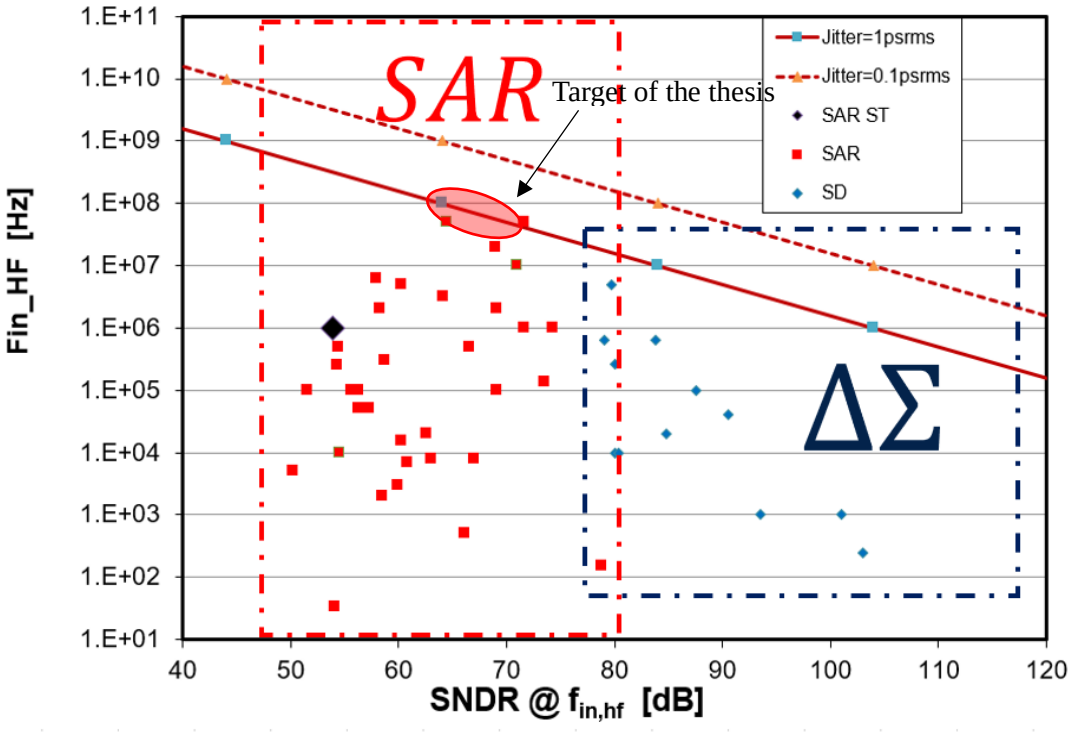

Figure 20 - Plot of filtered ADC – F_in high frequency equivalent to the bandwidth of Nyquist ADC compared to SNDR

2.3 Hybrid SAR Architectures

2.3.1 Hybrid SAR Pipeline

2.3.1.1 Amplify and quantize the residue

The SAR Pipeline architecture is based on the principles of the pipelined ADC presented in 2.1.1.3 by replacing the individual stages with a SAR ADCs. The advantage of the SAR is that the SAR includes intrinsically the DAC and the residue of the conversion is directly available without any further modifications. The hybrid idea is to benefit from best of properties of both architectures, the digital friendly low power SAR architecture on one side and the high speed high resolution capabilities of the pipeline architecture.

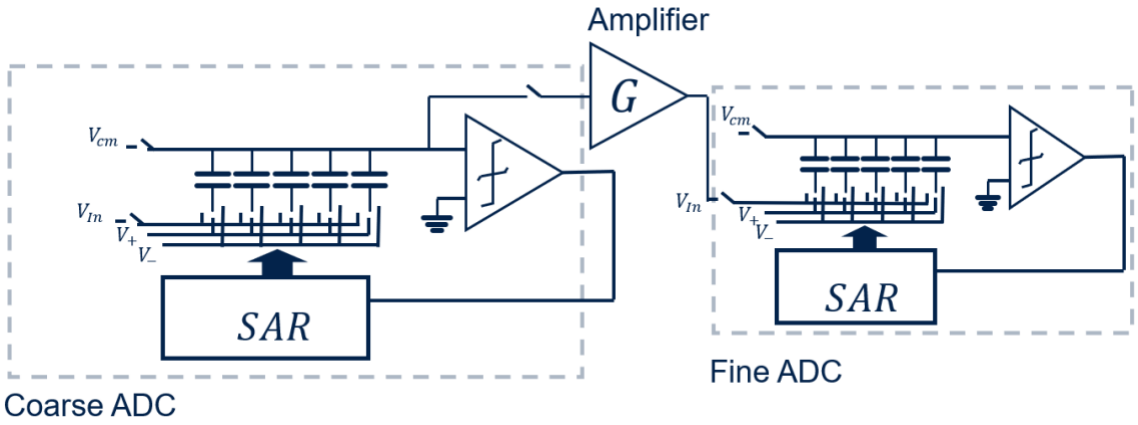

Figure 21 - Block representation of a pipelined SAR architecture

Figure 21 shows an example of a two stage SAR pipeline. The key element is the fixed gain amplifier rescaling the residue of the first stage to the full-scale voltage of the 2nd stage input. As SAR architectures are able to provide resolutions up to 8 bits without particular calibration efforts, SAR pipeline architectures typically have only 2 stages [54]. The two SAR stages can work at the same time on different samples thanks to the resampling at the input of the 2nd stage. A the end of the conversion cycle the amplifier transfers the first stage's residue to the second stage with a fixed gain. The sampling in the first stage has to respect the noise requirements of the whole converter where requirements in the second stage are relaxed by the gain stage. Redundancy is typically used to correct decision errors, due to settling and comparator noise that occur in the first stage. However, redundancy cannot correct KT/C sampling noise and is sensitive to interstage gain error and amplifier linearity. Special attention must be given to those non idealities. Specific strategies such as calibration or particular design techniques can ensure the preservation of the linearity [55] of the amplifier. The interstage is the most critical component and tends to be power hungry in order to meet the noise, precision and linearity requirements, limiting the overall

performance gains of the pipeline. A well explained proposition with complex timing dependency and low headroom voltage [56] has been presented in 2022. Showing the complexity needed to reach 175dB on Schreier's FoM with 2 stages SAR Pipeline [57].

2.3.1.2 State of the art performance

As in Figure 19, the closest silicon performance from 2015 to 2020 are plot on Figure 22.

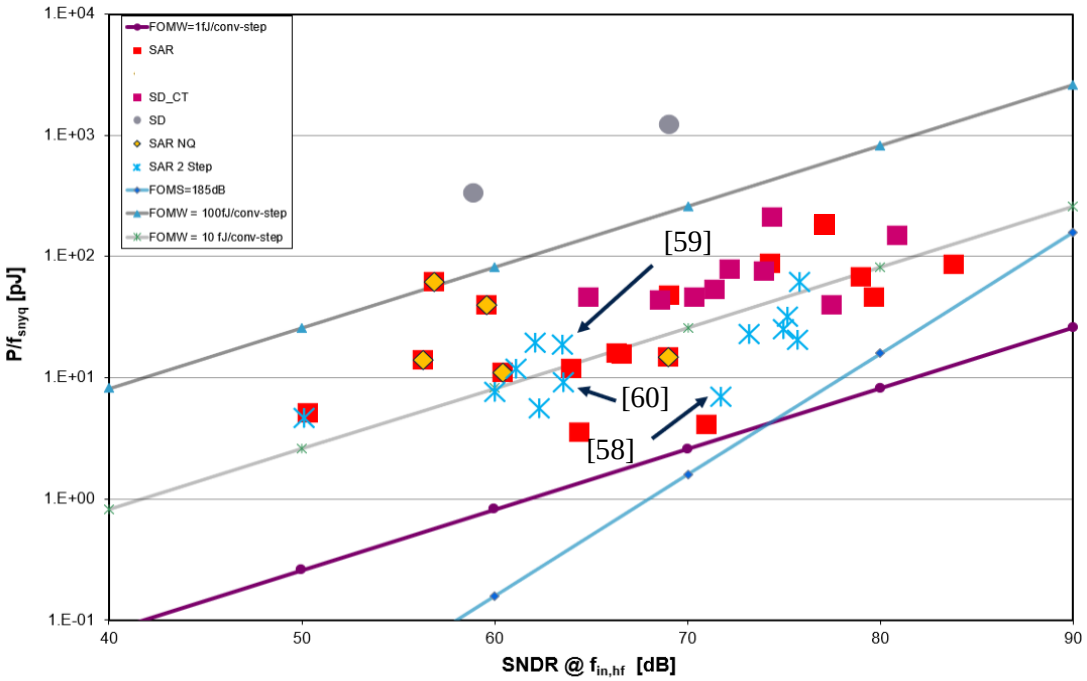

Figure 22 – From *[11]* energy efficiency depending on resolution for realizations close to the target.

The pipelined SAR are highlighted with the more energy efficient propositions in [11]. The most relevant for this work are detailed in Table 6.

Table 6 - Detailed performances of highlighted pipelined SAR ADC realizations in Figure 22

Reference	Year	SNDR [dB]	FOMs [dB]	BW [Hz]	Power [W]
[58]	2020	71.7	180.2	50M	700µ
[59]	2017	63.5	167.7	165M	6.23m
[60]	2020	63.6	171	125M	2.3m

The highest FOM is achieved by the work presented by Hung et al. [58]. It describes an efficient approach without calibration to limit the gain and the bandwidth of the op amp while reaching high performances with a weighted averaging correlated level shifting technique. This still transfers the challenge to power supply stability and consumes extra area (0.018mm²) for level shifting capacitance needed in this architecture. Regarding yield and cost requirements for industrial applications this architecture seems not to be appropriate. From the state of the art available in 2020, at the beginning of

this work, it has been concluded that it would be difficult to reach the targeted performance with a pipelined SAR architecture.

2.3.2 Hybrid SAR Noise Shaping

2.3.2.1 Noise Shaping SAR (NS-SAR) Overview

As discussed in 2.1.1.2, oversampling is widely used in ADCs to enhance SNR performance and reduce anti-aliasing requirements. Noise shaping allows to increase its effectiveness reducing the noise power in the useful frequency band. Combining oversampling and noise shaping techniques with the SAR architecture has been identified as a possible way to extend the SAR resolution with low overhead. This has been an active domain of research over the past 10 years with a number of noise shaping SAR implementations [61].

On Figure 23 is represented a generic noise shaping SAR ADC (NS-SAR ADC) architecture. The fundamental principle is to feed the conversions error (residue) through a noise shaping filter to the

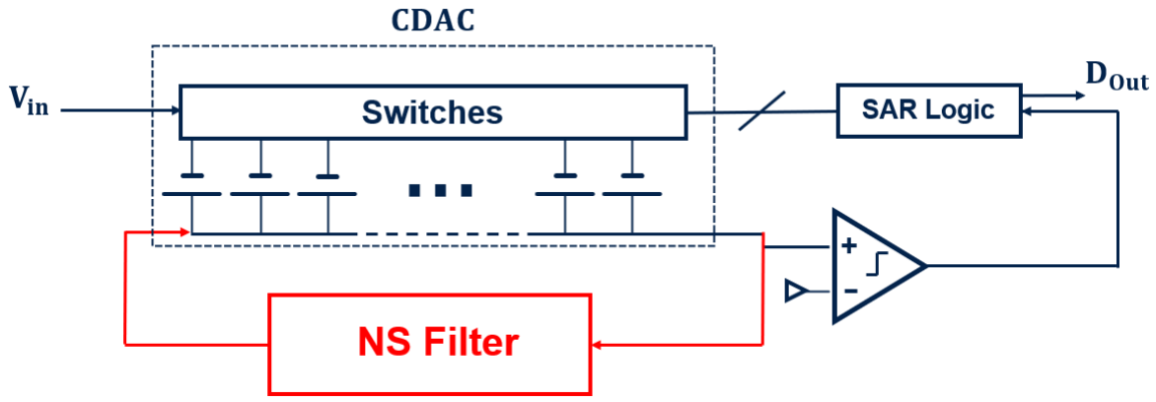

Figure 23 - Generic block diagram of an NS-SAR ADC

conversion steps of the subsequent input samples. Different topologies have been proposed to realize this function. For example the cascaded-integrator-feed-forward (CIFF) based on FIR or IIR filters [62] [63] demonstrated good performances. This comes at the cost of a high gain OTA or dynamic amplifier [64] to implement the filtering function. However, dynamic amplifiers are sensitive to PVT variations and present complex timing dependencies, while OTA implementations suffer from higher power consumption and area requirements.

Alternatively, fully passive filters can be used for the error feedback [65]. This is realized essentially with switches and extra capacitances used to integrate and sum previous samples [66]. However, the noise shaping is less aggressive, and the improvement of the SNR is modest compared to active noise shaping architectures.

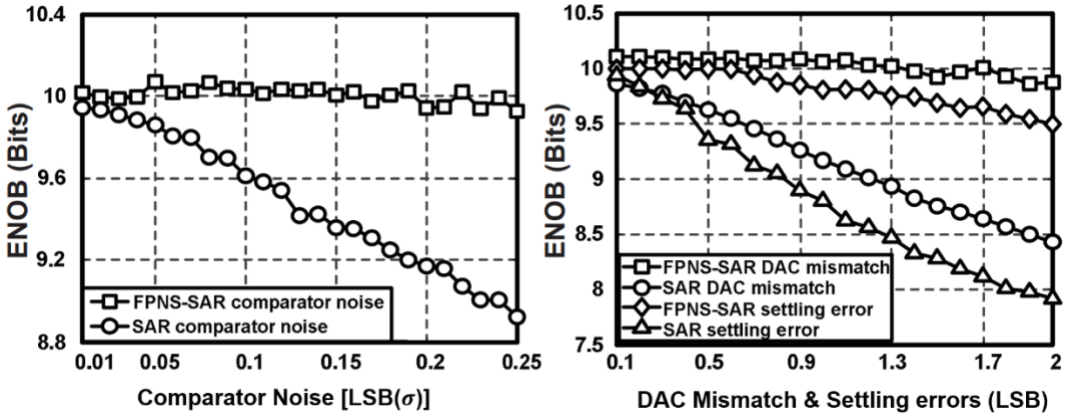

Figure 24 - From *[65]* comparison of simulated comparator noise effect and DAC mismatch and settling error effect on SAR architecture with and without fully passive noise shaping (FPNS)

As shown in Figure 24, Chen's work [65] showed that a noise transfer function realized without OTAs still alleviates comparator noise, incomplete settling error and mismatch to some extent. The fully passive topology in this example for a 65nm process reaches a Schreier's FoM of 165 dB for a first order noise shaping topology. A Schreier's FoM of 178 dB has been demonstrated in a 40nm process for a second order noise shaping in [66]. Li et al. presented a 10 MS/s second order SAR noise shaping [66] with an OSR of 8 and an optimization of noise transfer function's zeros through controllable gain. This relaxes the noise from added thermal noise through switched capacitances which is non negligible in the fully passive topology. However, these results require a complex continuous background calibration algorithm making a rise in frequency challenging. With 625 KHz of useful bandwidth, this realization presents interesting performance but looks not to be adapted for wider bandwidth without extra cost.

Fully passive NS-SAR make the connection between SAR and ΣΔ ADC in terms of resolution and power consumption. It still looks hard to reach 32MHz of effective bandwidth through an oversampled architecture without a consumption reaching the milliwatt range.

2.3.2.2 State of the art performance

Figure 25 shows the state of the art of SAR architectures close to the targeted performances over 5 years prior to the start of this work.

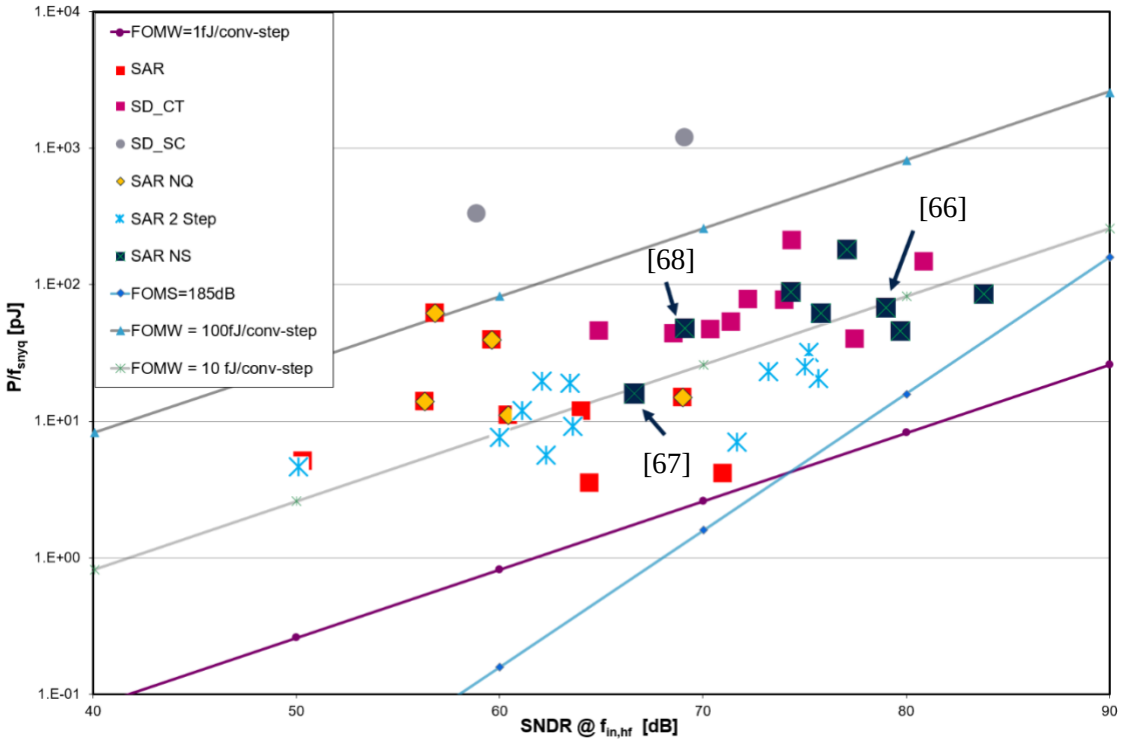

Figure 25 – From *[11]* energy efficiency depending on resolution for realizations close to the target including with focus on NS-SAR architectures.

NS-SAR architectures are highlighted in Figure 25. Lin's work [67] [68] present passive noise shaping in 14 nm FinFet with SNDR metrics in the range of this work's target. 25MHz [68] and 40MHz [67] effective bandwidth have been demonstrated for a consumption of respectively of 2.4mW and 1.25mW.

Table 7 - Detailed performances of highlighted NS SAR ADC realizations in Figure 25

Reference	Year	SNDR [dB]	FOMs [dB]	Eff BW [Hz]	Fs [MS/s]	Power [W]
[66]	2018	79	178	625K	10M	84µ
[67]	2019	66.6	171.7	40M	320M	1.25m
[68]	2017	69.1	169.3	25M	300M	2.4m

From the overview in this section non exhaustively represented in Table 7, NS-SAR looks promising architecture to provide low consumption for resolutions beyond 13-14 bits of ENOB. The target performances for this don't require such high SNR but a bandwidth of 32MHz. Like with ΣΔ ADCs, the target of mid-resolution (12bit) and several tens of MHz of bandwidth seams not really optimal in terms of energy consumption for NS-SAR converter topologies.

2.3.3 Time-based approaches to hybrid SAR ADCs

Among the data from [11], two architectures underlined in Figure 26 present remarkable performance in close proximity with the target for this work [69] [3].

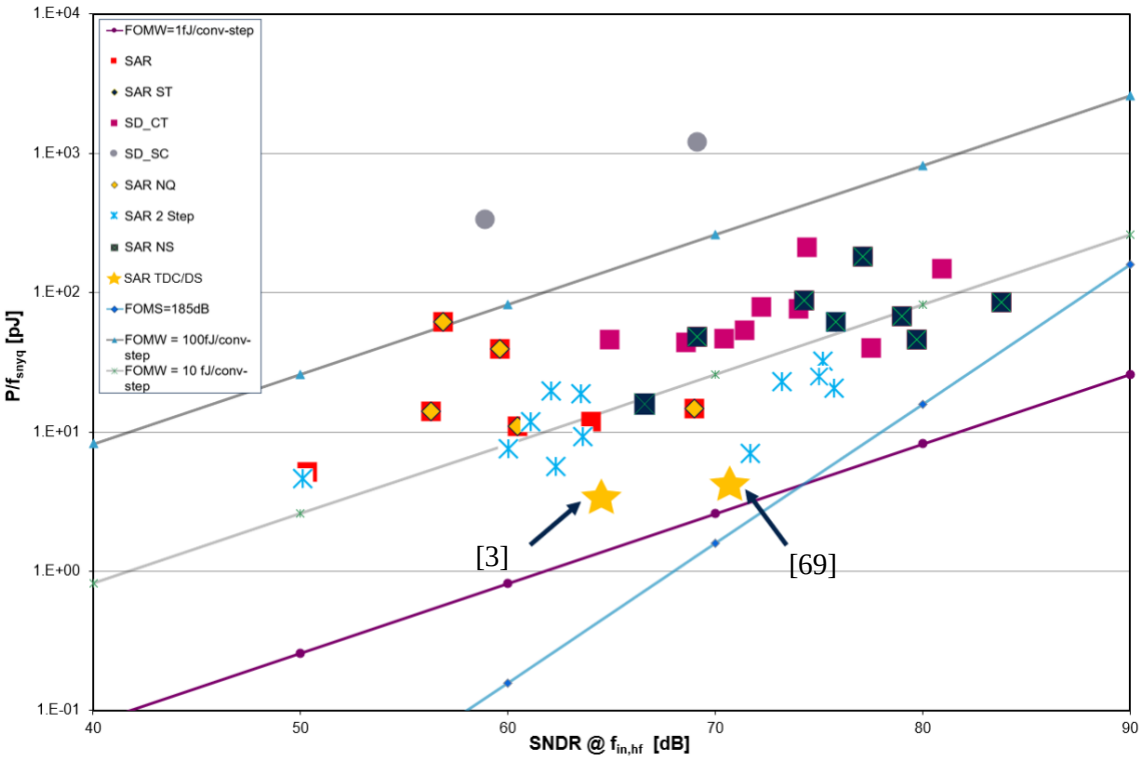

Figure 26 - From *[11]* energy efficiency depending on resolution for realizations close to the target.

These two hybrid architectures use a 2-step approach without adding any amplification stage. The SAR topology is used for the coarse conversion and a time-based approach for further quantization of the remaining residue. The key concept is to reuse the residue directly as the input to the second stage and tightly integrate the 2nd stage conversion into the SAR architecture. The conversion of the residue is based on a ramp concept, the time difference from the starting point of the ramp to the zero-crossing being proportional to the value of the residue. This time difference is in turn transposed to the digital domain with a TDC. The two implementations in the state-of-the-art use however very different approaches in terms of practical implementation. [69] uses a voltage -to-time conversion (VTC) with a continuous discharging ramp to produce pulse duration proportional to the residue value. The pulse duration is the quantized by the time-to-digital converter (TDC). [3] produces a staircase switched capacitor digital slope (DS) ramp directly integrated into the CDAC. Again, a non-quantized time-domain pulse is generated and the converted to the digital domain with a TDC. However, the delay-line of the TDC is used as the control unit for the staircase ramp. This perfectly matches by construction the time constants of the DS and the TDC.

Table 8 - Detailed performances of highlighted hybrid SAR-Time domain ADC realizations presented in Figure 26

Reference	Year	SNDR [dB]	FOMs [dB]	BW [Hz]	Power [W]
[69]	2019	71	182	10M	82µ
[3]	2016	64	176	50M	350µ

Table *8* gives the main performances of the two architectures. The performances are close to the target of the present work. This type of architecture appeared to have significant potential with further work needed to improve robustness and to introduce architectural refinements that could improve performance beyond the state of the art. The following subsections will give a more in-depth analysis of these two realizations.

2.3.4 Hybrid SAR TDC [69]

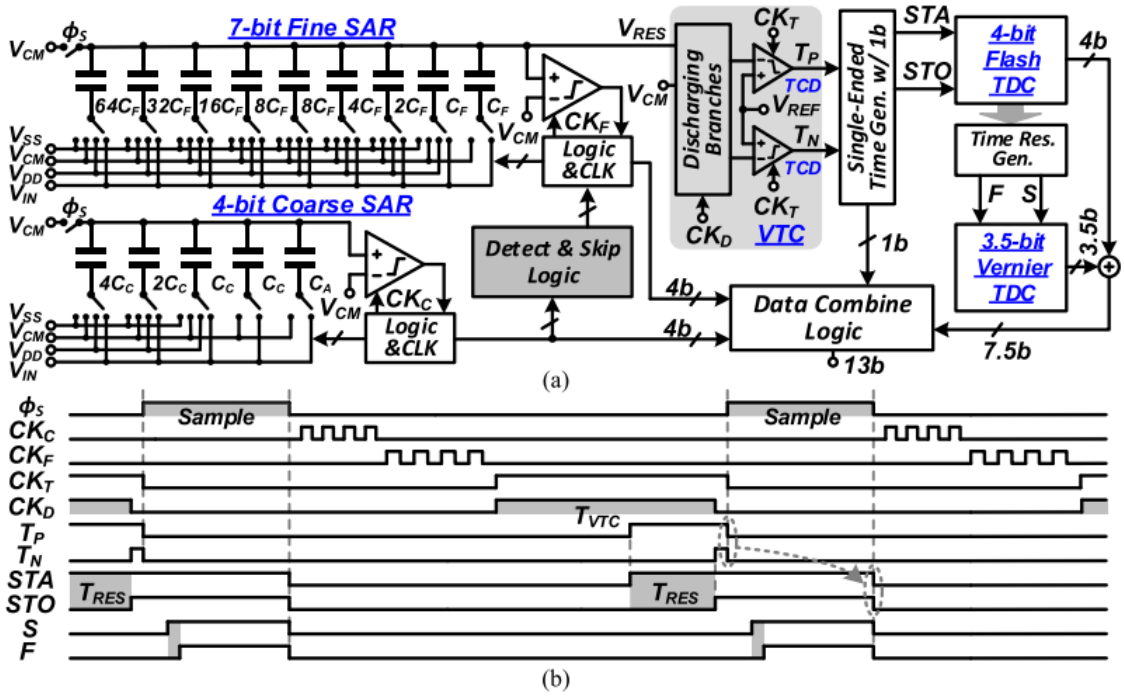

Figure 27 – From *[69]*, block (a) and timing diagram (b) of the proposed architecture (single-ended SAR ADC for simplicity)

2.3.4.1 Overall architecture

In Zang's implementation [69] several techniques are used to reach an energetic optimum with the speed and resolution expected.

As can be seen in Figure 27, two asynchronous SARs are used in the first stage. Both sample the

same input in parallel, then the first one, called coarse SAR converts the residue with low resolution but at high speed. Indeed, the sampling capacitance of the coarse SAR is smaller, so the conversion is faster. Once the 4th first bit has been converted, the same digital code is applied to the fine ADC's CDAC, this is called "detect & skip". A 1 bit of redundancy is introduced inside the fine SAR's conversion to correct any conversion errors in the coarse ADC. When the fine SAR's conversion is done, two current sources labled as "Discharging Branches" are switched on.

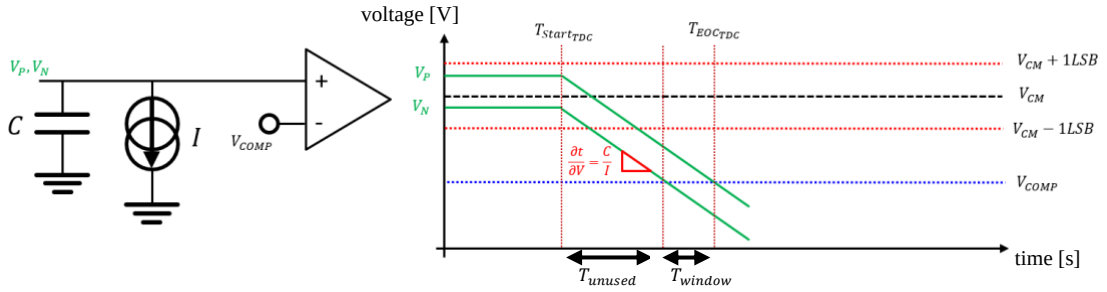

Figure 28 - Temporal representation of the differential VTC presented in *[69]*

A negative current is applied on both differential nodes as represented Figure 28. Each node is connected to a comparator with identical threshold voltages. The first crossing detected starts the time window and the second one ends it. A voltage to time conversion is thus implemented. The first comparator toggling also gives the sign information. Then a delay line used as a flash TDC converts this time window with 4 bits, including 1 bit of redundancy for correction of comparator offset and residual conversion errors in the SAR stages. Foreground offset calibration is also required to avoid saturation of the TDC. A second vernier TDC stage is launched in parallel to increase the resolution. At the end of the conversion, the different results are combined to form a valid 13 bit output.

2.3.4.2 Performances and drawbacks

As mentioned in Table 8, the presented architecture reaches 71 dB of SNDR at sampling frequency for 20MS/s. Thanks to very low power consumption of 82µW a record Schreier FoM for this resolution (~182 dB) is achieved with respect to the state of the art in 2020. A PVT tracking design is also proposed to match VTC and TDC gains. Discharging current sources are correlated to the unit delay of the delay line to create dependency between stage's time constant. Current sources are implemented as a series and parallel combination of more than 120 transistors thus consuming extra area (0.053mm²). The low power performance is also achieved through a very low supply voltage of only 600mV. The converter's consumption is mainly shared between SAR (36%) and the VTC (39%). The TDC (17%) and clock generation (8%) make up the remaining power consumption.

As seen from the timing diagram in Figure 27, all the depicted operations must take place in a 50ns window to reach the 20MS/s of the converter. Time is a challenge in this design as evidenced by the speed enhancement technics for the SAR and the pipelining of the vernier stage. Indeed, there is a unused time inherent to the proposed VTC as underlined in Figure 28, because the threshold voltages used as reference for the comparator is lower than the theoretical limit $V_{CM} - 1LSB$. This is necessary to take into account the limited bandwidth of the comparators. The comparator delay at the beginning of the ramp is indeed not constant, introducing a nonlinear voltage-to-time conversion. This phenomenon is studied in detail in chapter 5 of this thesis. As shown in Figure 29, the authors underlined the non-linearity induced when the threshold voltage is too close to the common mode voltage. The latency of the TDC in the design is 10ns, which represents 20% of the total time frame, but brings at the same time a THD of -65 dB. Furthermore, the comparator threshold voltage noise adds directly to the signal and is a critical parameter in this architecture.

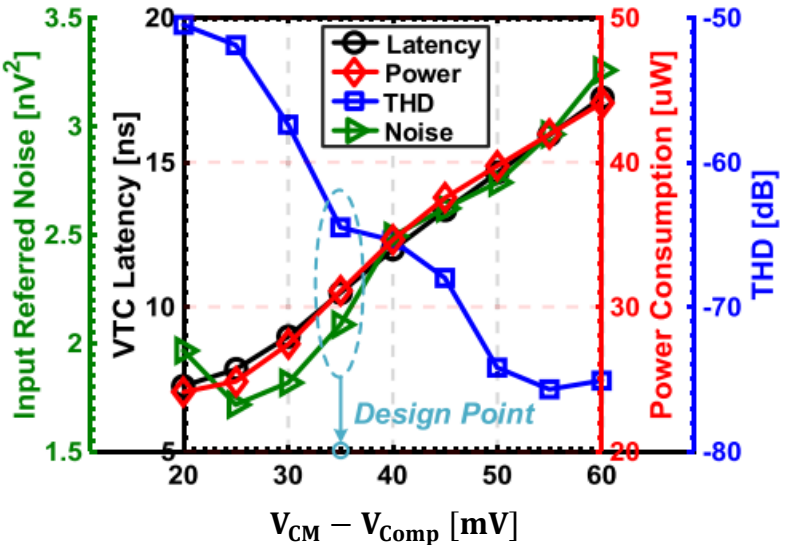

Figure 29 - From *[69]*, Simulated tradeoff between the VTC latency, power consumption, THD, and input referred noise.

2.3.4.3 Calibration and repeatability

As forementioned a complex and hardly scalable PVT tracking scheme is proposed in this architecture, as well as a need of foreground offset calibration. Both take place in the 120 transistors current matrix, a branch dedicated to calibration is presented to create a difference between the two discharging currents to calibrate the VTC gain error. This requires precise voltage generation for calibration as well as precise measurements. No proposition is made for a built-in calibration, so further investigations are needed to check global robustness of this architecture.

However, Zang's work presents a PVT robust hybrid SAR ADC with outstanding figures of merits and inspiring method to reach target resolution of 12 bits with ultra-low power performances. However, it seems challenging to keep the energy performance with a higher sampling frequency not speaking of the additional power consumption that might be needed the calibration circuit or and the low-noise reference voltage generation.

2.3.5 Hybrid SAR DS [3]

2.3.5.1 Overall architecture

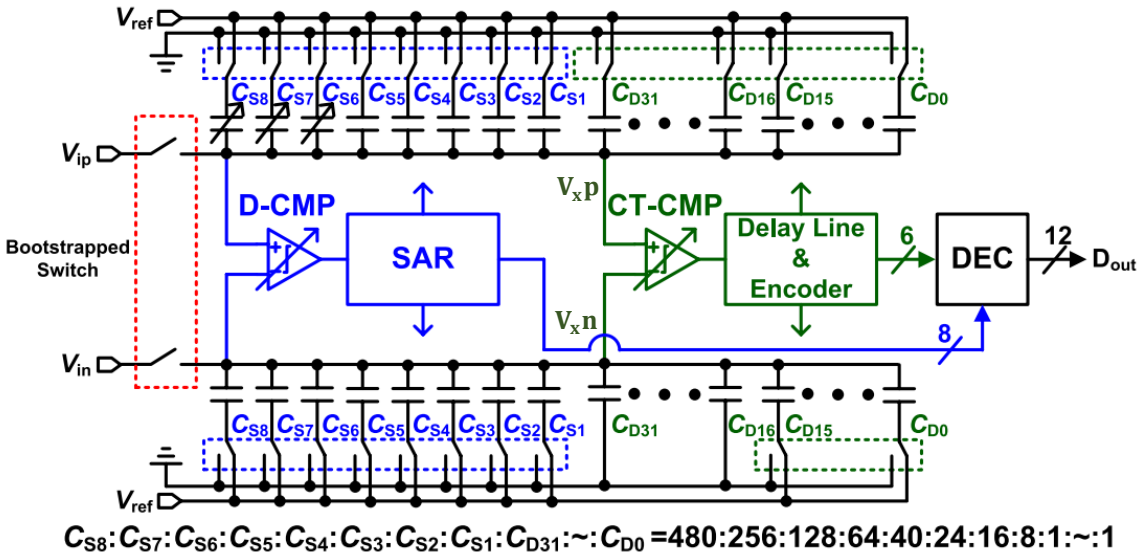

Figure 30 – From [3], block diagram of the SAR assisted DS ADC

Figure 30 represents the overall architecture of the hybrid SAR-DS ADC described by Liu in [3]. The CDAC and SAR discrete time comparator and logic can be seen on the left-hand side. On the right-hand side appears an additional array of 32 unit capacitors used for the implementation of the digital slope voltage ramp. A continuous time comparator and the delay line of the TDC complete the circuitry of the DS stage of the ADC.

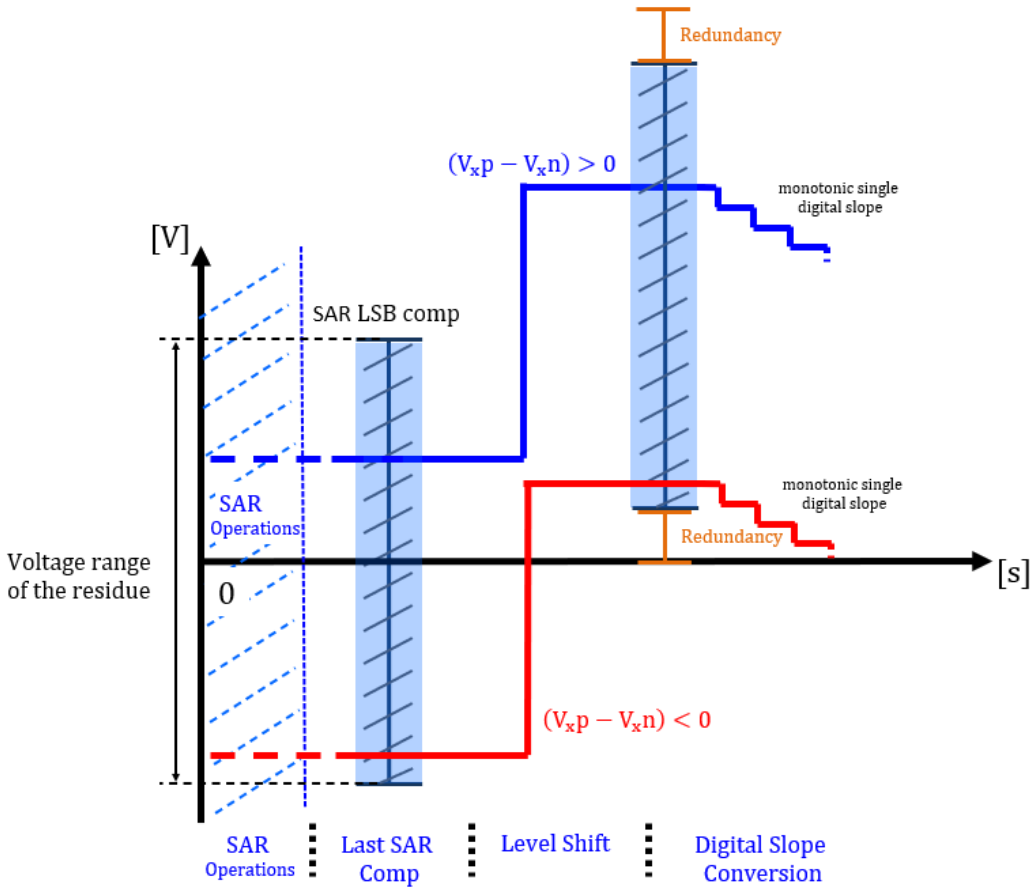

Figure 31 - Example of second stage *[3]* digital slope time operation for positive and negative residue

The SAR uses top plate sampling CDAC and a monotonic capacitance switching scheme introduced by the same authors in a previous publication [70]. This switching scheme allows only to discharge capacitors bringing the common mode of the top-plate nodes close to 0 at the end of the conversion. This switching scheme optimizes the energy consumed by the CDAC. Once the monotonic SAR has done the coarse conversion (here 8 bits with 1 bit of redundancy), the second stage converts the residue stored in the CDAC on nodes V_xp and V_xn. Figure 31 illustrates the operation done by Liu's second stage with two examples, respectively having positive and negative polarity. Once the last SAR conversion is done, a negative fixed voltage step of half the second stages full scale range is applied on the floating node V_xn. The differential residue voltage is now positive regardless of the initial polarity. A decreasing ramp controlled by the delay line of the TDC is then generated by the CDAC extension on the node V_xp. The zero-crossing at the input of the continuous time comparator will generate a rising edge that latches the state of the delay line. The state of the delay line represents the value of the residue in a thermometric digital code. Detail of the architecture of the 2nd stage are shown in Figure 32.

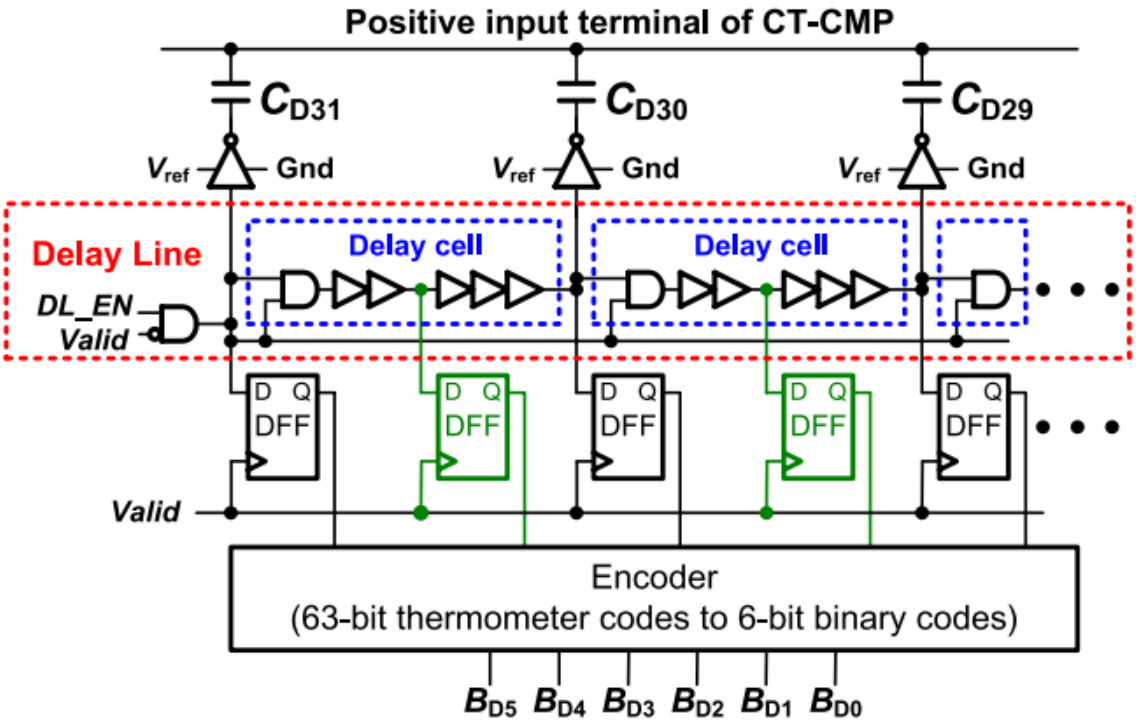

Figure 32 - From *[3]*, implementation of the 6-bit digital slope fine ADC

The SAR ADC resolution is 7 bits with a redundancy step embedded in the conversion. The DS-sub ADC full scale range is twice the maximum value of the theoretical range for the SAR ADC residue, adding an extra bit of redundancy to correct residual errors introduced by the SAR ADC. The bandwidth of the continuous-time comparator has a bandwidth of 80 MHz which transforms the staircase ramp into a almost perfect continuous ramp. This allows to use interpolation in the TDC to double the resolution, i.e. 6 bits for a total of 32 steps in the ramp. The total resolution of the ADC is 12 bits after recombination of the SAR and DS ADC outputs.

A foreground offset calibration is mentioned. The inputs on the common mode are shorted to measure the offsets of both comparators. A mismatch calibration mechanism is also put in place through the first 3 MSB capacitance of the DAC that can be trimmed. Finally, to save power, the continuous-time comparator of the DS sub-ADC is turned off during the SAR ADC conversion.

2.3.5.2 Advantages and drawbacks

The overall performances as depicted in Table 8 are close to the target. Various calibrations are mentioned with respect to DAC mismatch and comparator offset. However, these calibrations do not seem to be implements on-chip.

The main advantage of the DS architecture is the match of the ramp's slope and the gain of the TDC, eliminating one of the critical points in the continuous ramp architecture. Low comparator

bandwidth can restore high resolution with interpolation in the TDC despite a limited number steps in the staircase ramp/

Nevertheless, the DS architecture proposed by Liu also presents some time penalties. Indeed, the single sided ramp induces more steps than required for positive residues and increases the conversion time and power consumption. Furthermore, the low comparator bandwidth increases the latency and probably the startup time for the comparator. No detailed data is available on these points in the publication.

The power consumption of the converter is 305µW for 100MS/s which is close to the targeted specifications for this work. This architecture seems very promising, in particular with respect to industrial robustness criteria. The intrinsic sensitivity to PVT variations seems to be low thanks to the intrinsic matching between the ramp slope and the TDC gain. The reported figure of merit is below the one reported in [69]. However, there seems to be room for further improvement regarding the architecture of the DS stage. The reported resolution and speed are close to the target of this work.

2.4 Conclusion

This chapter presented a large overview of ADC architectures. Hybrid SAR ADC architectures combine the SAR architecture with other techniques such as pipelining, oversampling or time-domain encoding. These architectures emerge in the state of the art as being capable to reach high conversion speed and resolutions beyond 10 bits. Among the various possible hybrid architectures the digital-slope hybrid SAR ADC architecture has been identified to be extremely promising for the target application specifications. Further improvements are needed to reach still lower power consumption and industrial robustness. The research work of this thesis is an attempt to respond to these two objectives.

The next chapters will present an enhanced 2 step SAR assisted by ramp topology targeting a reduced conversion time and power consumption. An embedded calibration scheme will also be proposed to reach high robustness by leveraging the already present hardware.

Chapter 3

2 Step SAR-Bidirectional Digital Slope ADC Architecture

3.1 PROPOSED ARCHITECTURE 63

3.1.1 CONCEPTS AND CHALLENGES OF THE ARCHITECTURE 63

3.1.1.1 Use of the SAR LSB as information 65

3.1.2 ERROR SOURCES AND CORRECTION 70

3.1.2.1 Comparator offset and noise in the SAR 70

3.1.2.2 Inter stage redundancy 73

3.1.2.3 SAR redundancy 74

3.1.2.4 Offset calibration 76

3.1.2.5 CT-CMP Latency 77

3.1.2.6 Latency correction 79

3.1.2.7 DAC non idealities 81

3.1.2.8 Noise balance 82

3.1.2.9 Extra capacitance impact on dynamic 84

3.2 SIZING OF THE PROPOSED ARCHITECTURE 85

3.2.1 BIT REPARTITION BETWEEN STAGES 85

3.2.2 NOISE BALANCE IN THE PROPOSED ARCHITECTURE 87

3.2.3 DETAILS OF PROPOSED ARCHITECTURE 89

3.2.5 2ND STAGE DIGITAL SLOPE DESCRIPTION 91

3.3 VERILOGA MODEL 95

3.3.1 DESCRIPTION OF THE VERILOGA MODEL 95

3.3.2 TESTBENCH AND SIMULATION RESULTS 97

3.3.3 POWER CONSUMPTION ESTIMATION 100

3.3.4 COMPARISON WITH STATE OF THE ART 103

3.4 CONCLUSION 104

3.1 Proposed Architecture

3.1.1 Concepts and challenges of the architecture

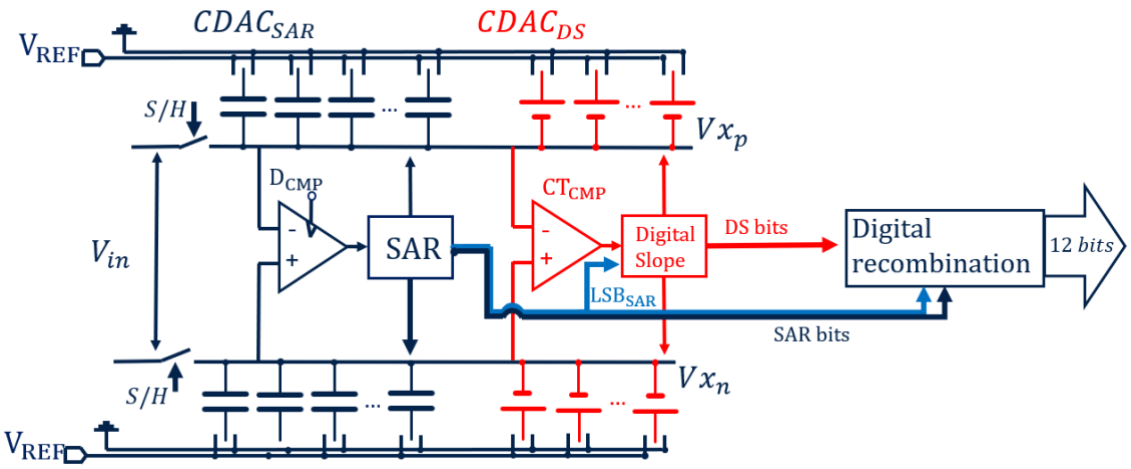

Figure 33 – General concept of the bi-directional digital slope SAR assisted ADC – 12 bit example

This chapter introduces an enhanced architecture of a SAR assisted 2 step ADC where the SAR residue is quantized by a bidirectional digital slope time-based converter. The architecture is composed of a SAR stage as coarse converter and a bidirectional ramp stage based on digital slope as fine converter as presented in Figure 33. While the general concept is similar to [3], several innovations have been introduced, most importantly the introduction of a bidirectional digital slope and the use of the final SAR bit to determine direction of the digital slope.

The main principle of a two stage SAR assisted converter is the reuse of the residue of the SAR conversion as an input to the second stage. As represented in Figure 16, the residue voltage Vx_p-Vx_n left by a k-bit SAR at the end of the conversion represents ideally the k-1 bit quantization error of the SAR. As the input is first sampled on the CDAC, the residue voltage on the floating node is in practice equal to the difference between the input voltage and the voltage produced by the CDAC with the k-1 MSBs resulting from the SAR conversion.

$$V_{res} = V_{in} - V_{CDAC} \tag{3.1}$$

Where V_{res} in the differential structure is the voltage difference ($Vx_p - Vx_n$). Therefore, the residue contains also the potential conversion errors of the SAR due to various error sources such as settling errors or comparator offset and noise.

The architecture presented here introduces a novelty in the operation of the second stage. The previous chapter highlighted the correlation between power consumption and conversion time of the second stage. To optimize consumption, the active blocks of the 2nd stage are usually turned off during the SAR conversion and then turned on at the beginning of the second part of the conversion. The most consuming block for a ramp topology [69] [3] is the continuous time comparator used to detect the crossing of the input ramp. As represented on Figure 34, the comparator must be started prior to the conversion and then consumes energy continuously until the cross detection switches it off. The time spent consuming energy with the continuous time comparator is divided into different sections. During startup (T_{start}) there is a dynamic component due to the charging of internal nodes. The ramp by itself can be subdivided into several portions. First there is an unused time due to a voltage step mandatory to convert positive and negative residue value or due to a time window generation with comparator and threshold voltage [69]. This unused time as presented in previous chapter [69] [3] (T_{Unused}) is spent before the start of the conversion. On Figure 34 is represented a voltage shift as implemented in [3] inducing in this example 8 unused step for this sign of residue. To correct errors in certain limits, redundancy is implemented and corresponds to the extra steps introduced to handle conversion errors of the SAR stage, extra time is thus spent on those steps (T_{redun}). Then the rest of power is spent during a time proportional to the input (T_{use}). Because the redundancy can be implemented in time windows before and after the time window corresponding to the input, on Figure 34 (T_{use}) and (T_{redun}) are represented together. The comparator is turned off once its output has rised.

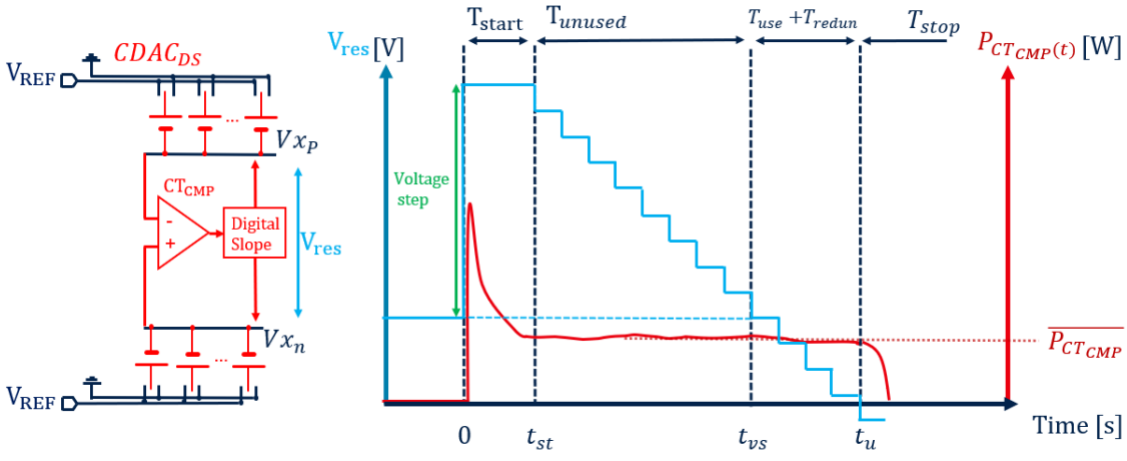

Figure 34 - Representation of the comparator consumption for the second stage

The comparator being switched on only over a part of the conversion period, as represented on Figure 34, it can be segmented in different time segments where an energy start (E_{start}) is consumed on T_{start} and (E_{stop}) during the turning off phase T_{stop}. Once the comparator is switched on, its power consumption is

mainly static, so around a mean value as $\overline{P_{CT_{CMP}}}$ represented on Figure 34. The energy consumed by the comparator can be expressed as:

$$E = E_{start} + \overline{P_{CT_{CMP}}}.(\mathrm{T_{Unused}} + \mathrm{T_{redun}} + \mathrm{T_{use}}) + E_{stop} \qquad (3.2)$$

The energy consumed and so the equivalent power consumption of the block has a proportional part equivalent to the time spent with the comparator on.

The proposed architecture presents a structural improvement reducing on-time of the second stage by cancelling $\mathrm{T_{Unused}}$ while maintaining the same resolution.

3.1.1.1 Use of the SAR LSB as information

From a systemic perspective, the sign of the residue during the successive steps of the SAR conversion is used successively to determine the output bits from MSB to LSB. In practice, the LSB represents the sign of the residue.

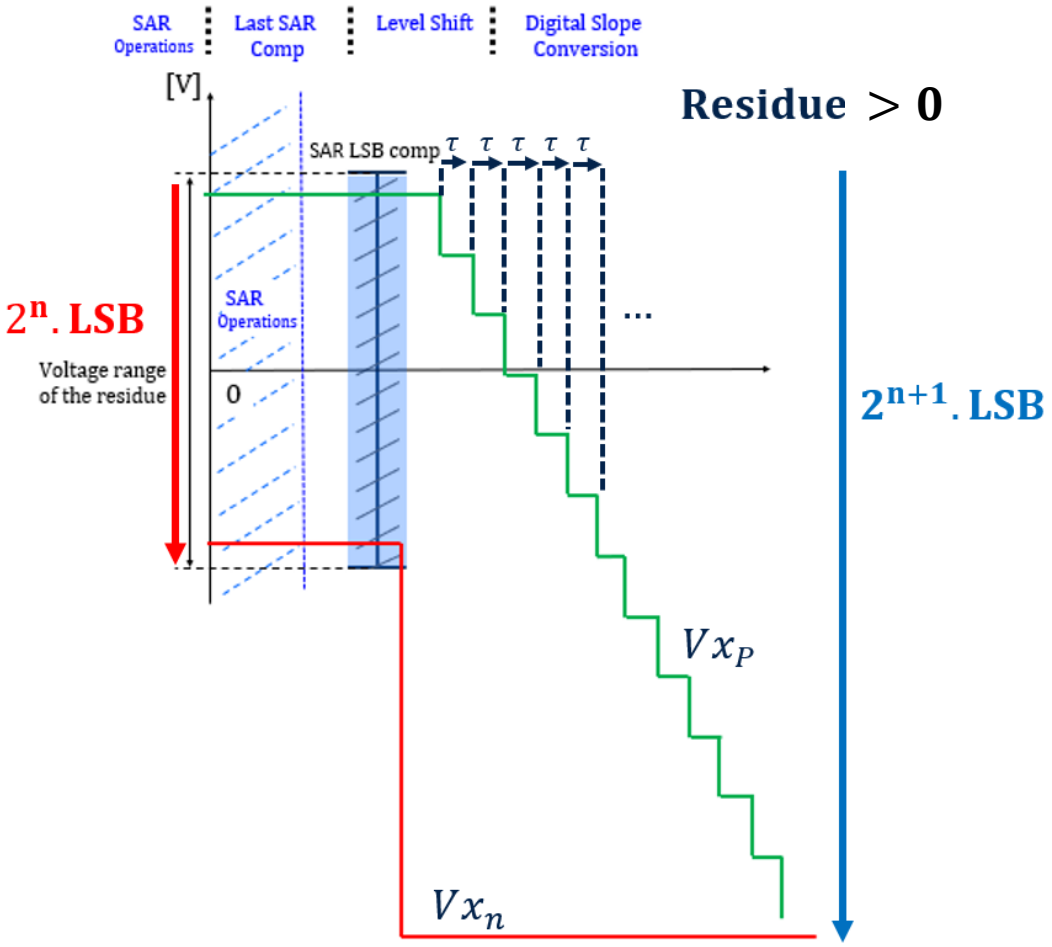

Figure 35 - Illustration of 2nd stage monotonic digital slope behavior for a residue > 0

As previously discussed, the state of the art doesn't take advantage of SAR's last bit information, in VTC [69] and DS [3] approach the ramps are generated independently of the first stage. This induces unused time for both presented architectures and a possible improvement in power consumption. Figure 35 underlines the extra steps done by a monotonic digital slope [69] which does not use sign information, consequently the slope has only one polarity. Figure 35 draws the operations of a monotonic digital slope and the dynamic of the residue is indicated on the left of the figure. To convert the residue as presented in Figure 35 with a n bit second stage based on thermometric code it requires 2^n steps. Because of the monotonic aspect of the slope, 2^{n+1} steps are required, as the sign of the residue is not taken into account. This is because a decreasing monotonic slope as represented in Figure 35 cannot convert a negative residue. Likewise, an increasing monotonic slope cannot convert positive residue. However, the input residue rang is symmetric around 0V thus both signs can be present on the residue. To overcome this a voltage shift is added on purpose to guarantee the sign of the starting voltage of the ramp. With this mechanism as represented on Figure 35, even a negative residue is positive after the voltage shift. On the other hand for code presenting already the "good" sign as positive residue in Figure 35 example, these

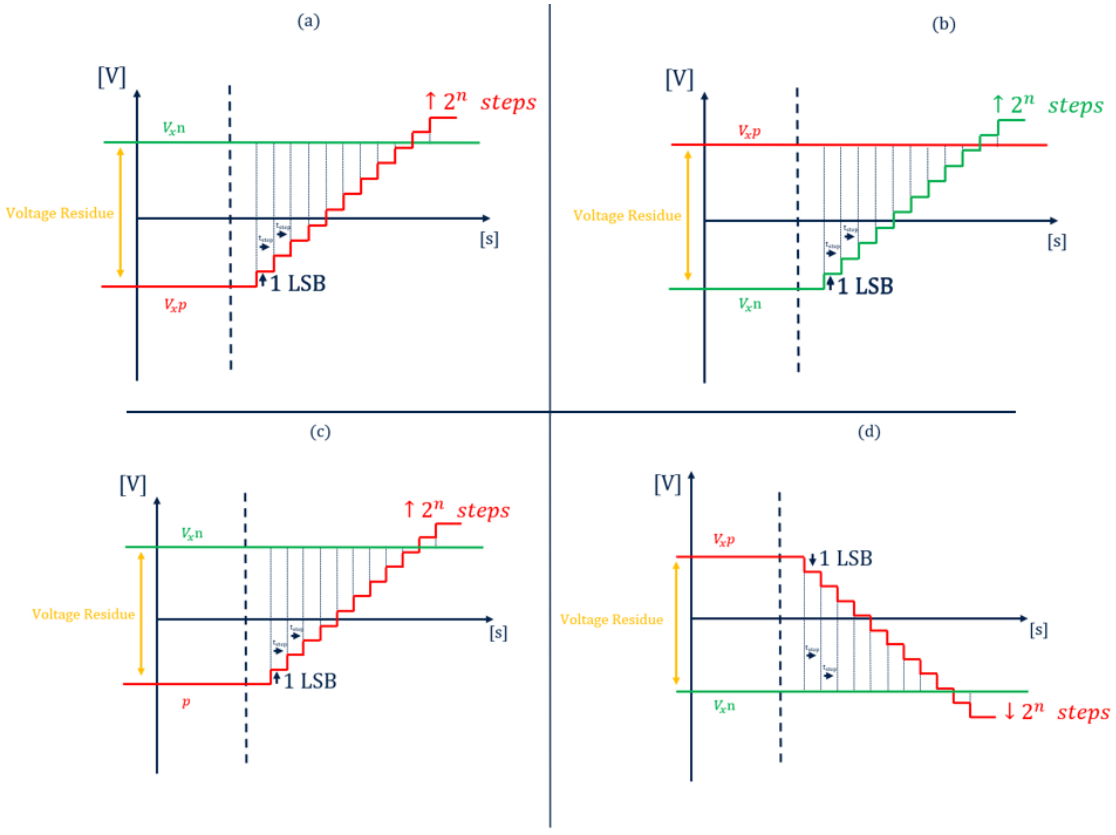

Figure 36 - different approaches of digital slope based on residue sign: double monotonic digital slope for a negative residue (a) and a positive residue (b) - single bidirectional digital slope for a negative residue (c) and a positive residue (d)

extra codes are not compulsory and add extra time, thus extra power consumption. The unit time step of the digital slope is represented as τ in Figure 35. The novel approach of the conversion assisted by a digital slope proposed in this work takes advantage of the LSB of the SAR which gives the sign of the residue. Different approaches could be implemented taking sign information into account. Figure 36 draws different methods for both residue signs, the first is to have two monotonic digital slopes implemented. Each monotonic digital slope could thus be started regarding the residue sign. This implies to have a similar ramp generation on both floating nodes and use only one at a time, each node must so present 2^n unit capacitances to generate its ramp. This solution is an improvement in regard to the monotonic digital slope implemented in [3] because less voltage steps are required. Nevertheless, the whole ramp generation must be duplicated on both floating nodes (Figure 36 a & b). Another way could be to keep the ramp generation only on one dedicated floating node but with two ramp signs. In regards of the residue sign, the direction of the ramp would adapt to ensure a crossing at the input of the comparator regardless of the residue's sign (Figure 36 c & d). This implies to generate 2^n steps in both directions on the same floating node. This solution also suppresses the need of an extra voltage step before the ramp start to guarantee the crossing no matter the sign. Nevertheless, the input common mode voltage of the comparator at the crossing time is in both situations dependent on the input value. To alleviate this phenomenon a differential approach could also be implemented as drawn in Figure 37. Here each step is generated symmetrically on both floating nodes. Although this approach maintains the common mode voltage at the input of the comparator constant, it increases complexity of the CDAC. Unlike monotonic ramps, the differential approach requires to apply half LSB steps at the same time on both floating nodes to generate an LSB step. This implies implementing capacitances with halved unit value in the CDAC used to generate the ramps. Moreover, 2^n unit capacitances must be switched on both nodes and for two possible directions of the ramp. To overcome the discussed implementation challenges, a pseudo differential approach allows to maintain the common mode voltage approximately constant at the input of the comparator while implementing 2^{n-1} steps per floating node for either residue sign.

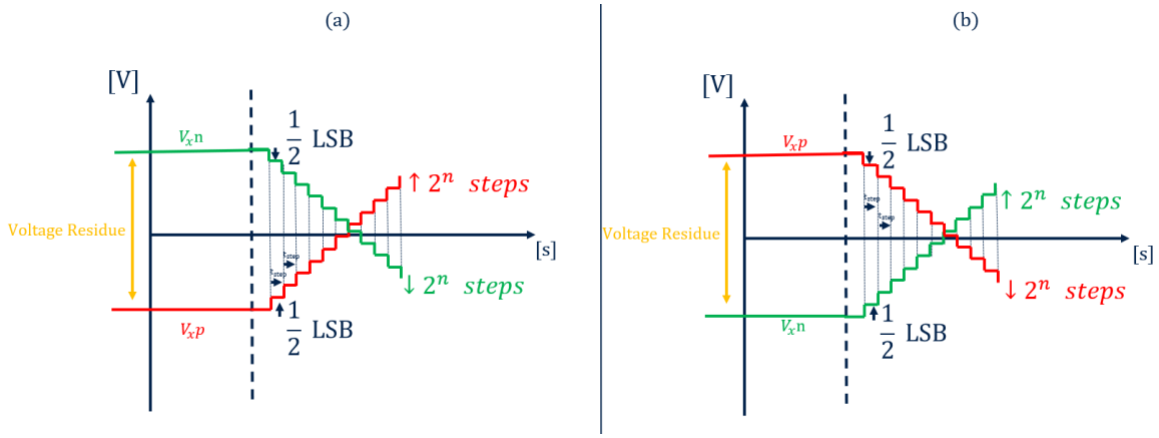

Figure 37 - Time voltage diagram of a fully differential bidirectional digital slope for a negative residue (a) and a positive residue (b)

Figure 38 depicts the proposed pseudo differential bidirectional digital slope. Both nodes are used as ramps converging to cross. Contrary to the differential bidirectional digital slope presented in Figure 37, the voltage steps are not processed at the same time thus the voltage steps of 1 LSB are done only on one floating node voltage at a time. This permits to not halve the values of unit capacitance compared to a monotonic implementation. Furthermore, the number of steps are shared between branches, which implies two times less voltage steps for each floating nodes.

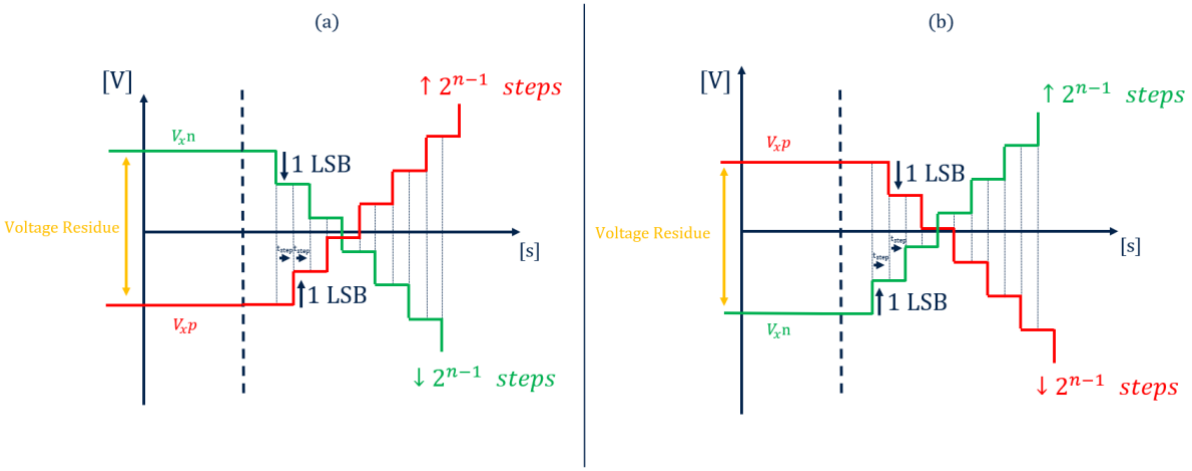

Figure 38 - temporal voltage representation of proposed pseudo differential bidirectional digital slope for negative residue (a) and positive residue (b)

As discussed and compared to a monotonic implementation [3], the proposed implementation does not require extra voltage steps to converge, no matter the sign. The floating node voltages converge to the common mode to cross each other. Furthermore because of this convergence, the common mode voltage at the input of the comparator varies in a delimited voltage range $\left[\pm\frac{1}{2}LSB\right]$. The pseudo differential bidirectional ramp approach reduces both the conversion time and the average consumption by a factor of two compared to a monotonic ramp by using the sign information of the residue because only half of the steps are required for the same resolution.

Nevertheless, this differential approach of the ramp conversion requires some precautions concerning the sign transmitted by the SAR. Indeed, Due to comparator noise and offset, the actual sign of the residue could be different from the one determined by the SAR comparator. Because this system creates an interdependency between stages, errors could seriously impact the performances of the ADC. Figure 39 shows an example of a situation to avoid where the sign of the residue is negative while the D-CMP indicates a positive sign. The ramps will never cross in this case, as the expected starting point is different from the actual one. An error will occur producing a missing or false code.

To prevent such a situation, redundancy needs to be introduced by adding a voluntary offset and extra steps to the digital slope. By subtracting the offset added on purpose at the end of the conversion in the digital domain, it will give the correct code for the converted residue despite the sign error introduced by the SAR. The added offset must be sized large enough to cover the range of possible occurrence of sign errors. Figure 40 shows the same situation as in Figure 39 with 4 steps of redundancy added. This is translated in the opposite way of the ramp before the start of the conversion. The modified residue is now positive, a crossing of the ramps occurs after 2 steps. At the end of the conversion, the 4 extra steps are subtracted from the result, giving the correct code of -2. Although this technique ensures the integrity of the conversion in a bidirectional structure, it adds extra steps. Careful analysis and design are needed to minimize the number of extra steps. Calibration of the discrete time comparator in the SAR can be envisaged as describe later in this chapter to reduce the range of the required redundancy.

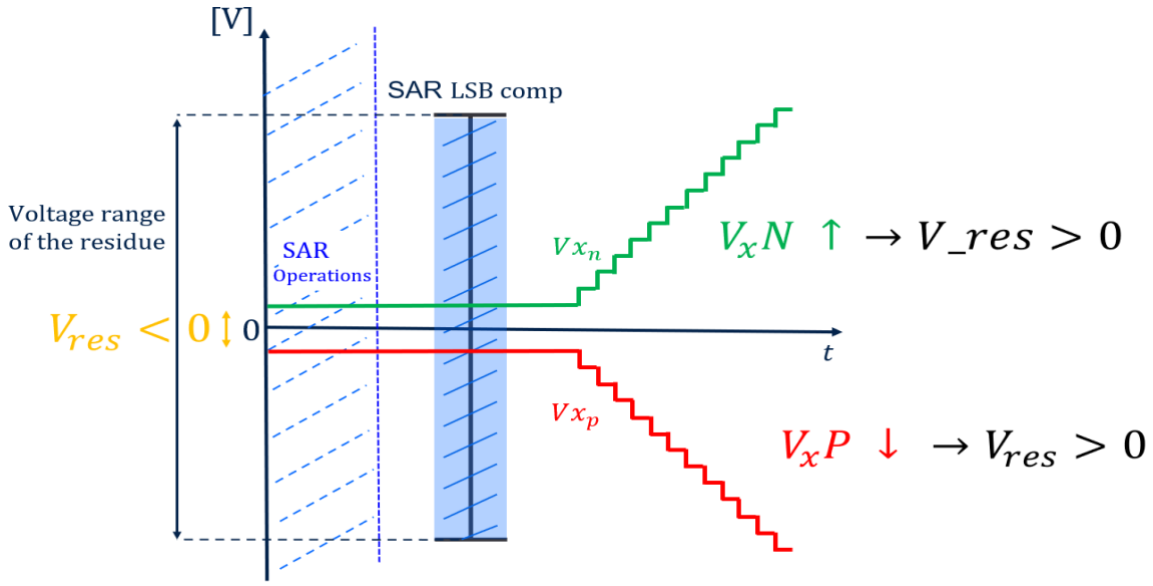

Figure 40 - Temporal voltage representation of SAR sign error causing bidirectional digital slope divergence. (Negative voltage residue and positive sign behavior)

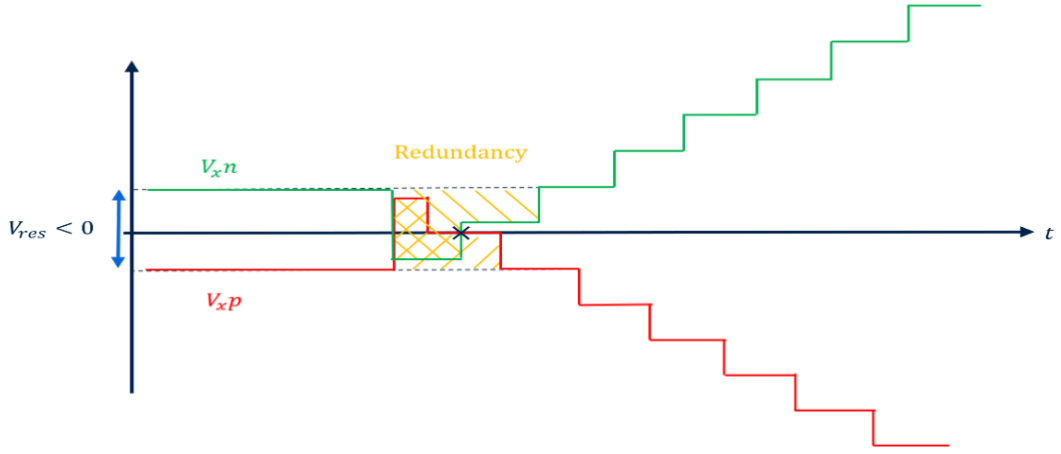

Figure 39 - Temporal voltage representation of SAR sign error corrected by 4 step redundancy. (Negative voltage residue and positive sign behavior)

3.1.2 Error sources and correction

In a two-step architecture non ideal effects of both stages affect the integrity and precision of the conversion. In the proposed architecture both stages share the top-plate nodes of the CDAC holding the conversion residue used successively by the 2 stages for their conversion. These nodes are permanently connected to their respective comparators, D-CMP for the SAR and CT-CMP for the digital slope (see Figure 33). As seen before, errors of the first stage can affect the operation of the second stage. Furthermore, the sharing of the top-plate node adds additional interactions. As an example, transition of the respective comparators from the on-state to the off-state or vice versa can modify the charge balance of the top plate nodes and slightly change the value of the residue voltage. Care must be taken in analyzing the different error sources and where necessary seek a way to compensate or avoid these errors.

3.1.2.1 Comparator offset and noise in the SAR

Along the SAR conversion the residue keeps the sum of decision errors, a mistaken decision took at the beginning of the SAR conversion is still present at the input of the second stage on the residue. This would not obviously induce divergent behavior in the second stage but degrade the performances of the ADC because coarse errors can represent several LSBs. If a bit evaluation in the SAR is done with an error of amplitude ε, the residue at the end is equal to:

$$V_{res} = V_{res_{ideal}} + \varepsilon \tag{3.3}$$

Where V_{res} is the residue presented with the error previously done and $V_{res_{ideal}}$ is the value of the residue expected without error.

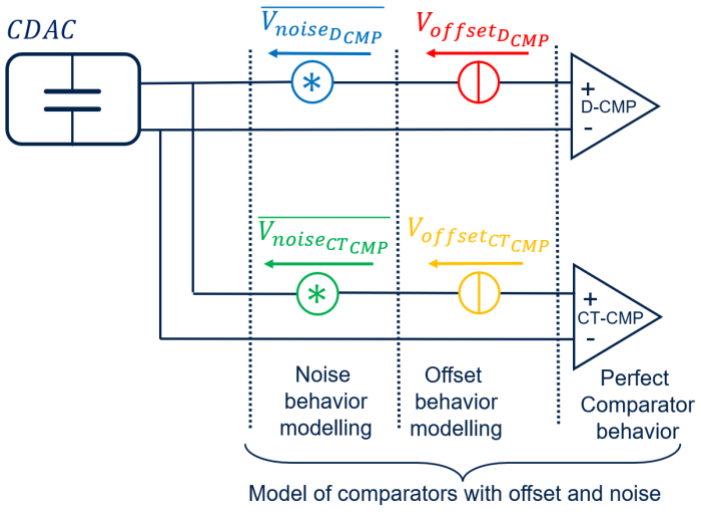

Figure 41 - Systemic non idealities representation of the comparators in the proposed architecture

Main decision error sources inducing ε described in (3.3), are offset and noise of the D-CMP. Figure 41 shows the model used in this work where comparator offset and noise are modeled as additional voltage sources in series with the comparator input. The values of the offset and noise sources are determined as the output offset and noise voltages divided by the gain of the comparator. This section details the impact of these non-idealities induced by the comparators on the system and proposes ways to correct and size it before doing noise budget of the proposed ADC with DAC non idealities.

The ε value described in (3.3) represents a residual code error after decision mistake through the SAR process. In the hypothesis that this value is only induced by the noise, this means that at some SAR decision the input voltage plus the noise presents a different sign than the input voltage. The input referred noise voltage is thus more important than the residue at that time of the conversion and their signs are different. The comparator gives then a wrong information on the bit evaluation and the code stored represents this error. In the case of the offset, the extra voltage converted is constant along the SAR process, but the mechanism is the same. If at a decision time, the offset voltage brought to the input is more important and with different sign than the input voltage, a decision mistake occurs. If this error occurs on the last SAR decision, caused by the noise or the offset, a sign error results as presented in Figure 39.

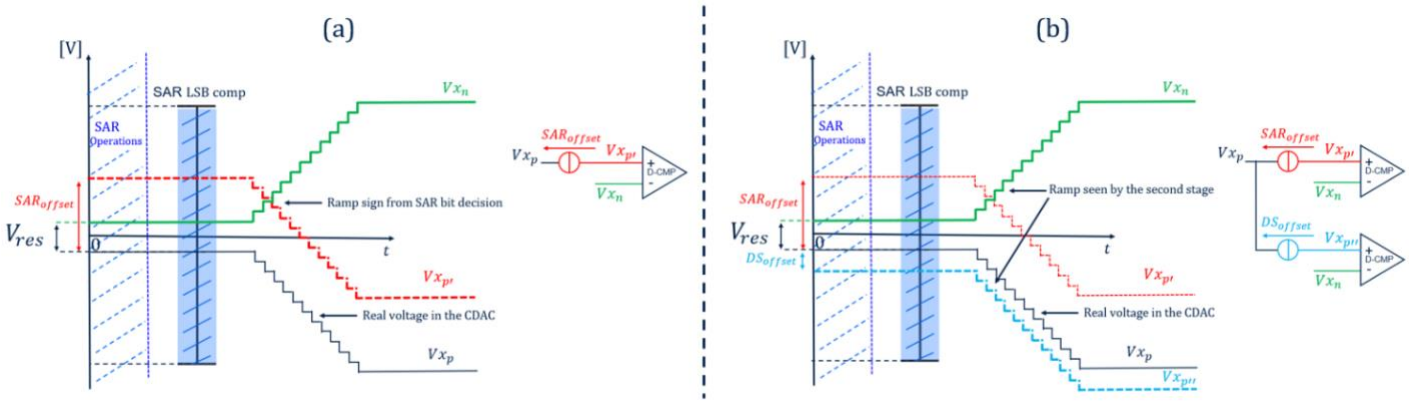

Figure 42 - Temporal voltage representation of sign error due to offset. Wrong sign decision taken by the SAR (a) and ramps presented at the second stage comparator (b) compared to the voltage present in the CDAC(Vx_p)

Regarding the offset, two comparators are present in the system which induces interactions on the behavior of the second stage. Because the last decision of the first comparator determines the direction of the ramp, the difference of the offset of both comparators can induces divergence.

Figure 42 (a) shows an error made on the SAR LSB evaluation and its equivalent ramp through second stage. In this example the residue stored in the CDAC is negative but due to the negative offset of DT comparator the SAR evaluates it as positive. Furthermore, the CT comparator presents a negative

offset drawn on Figure 42 (b) which adds to the DS comparator offset increasing the error. Due to the errors made by the comparators the ramps are divergent, and no crossing will occur. Redundancy as presented in Figure 40 could overcome this phenomenon but it must be sized coherently with the offset range of both comparators.

Furthermore from (3.3), depending on the ε value, V_{res} could also be greater than $V_{res_{max}}$, which could induce a situation as drawn on Figure 43. As in the example given in Figure 39, no crossing occurs, the 2nd stage data is then lost.

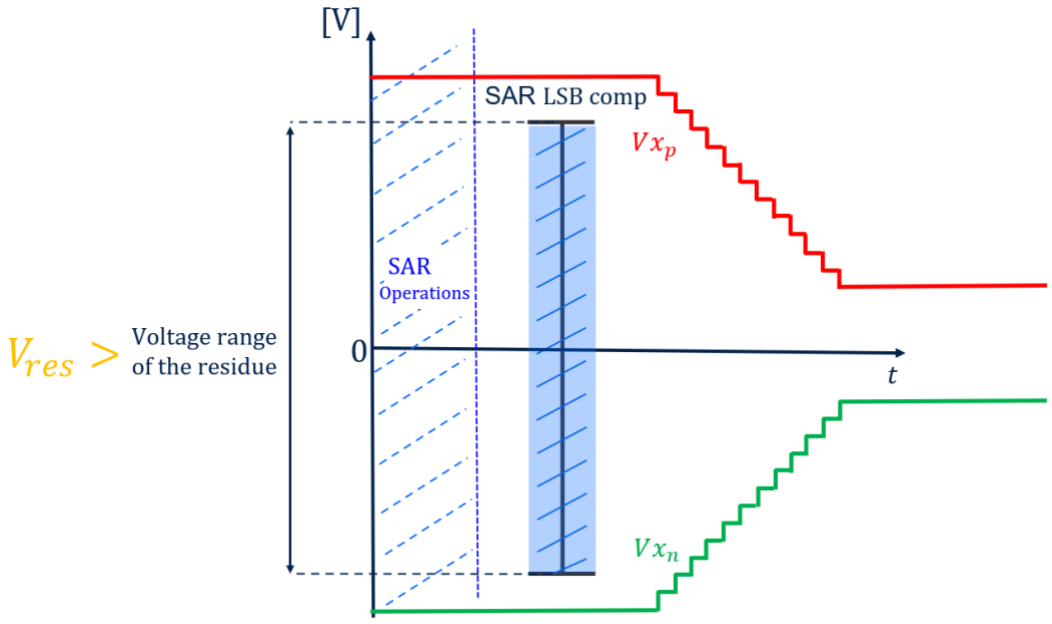

Figure 43 - Bidirectional ramps through time for a voltage residue greater than the 2nd stage dynamic

From Figure 43 it can be seen that extra steps at the end of the ramps would be able to correct this extra dynamic as redundancy presented in Figure 40. In a symmetrical way to the added steps at the beginning of the ramp, it is also necessary to add steps after the maximum theoretically expected code. The range to add also depends on the offset and noise of the comparator D-CMP as represented in Figure 41. Two redundancies are therefore required for the bidirectional slope.

The second stage redundancy must be sized coherently with the D-CMP noise and offset of both comparators. To describe the noise of the SAR comparator, it is considered gaussian thus the standard deviation (σ) of this noise is equal to the RMS voltage $\left(V_{D_{cmp}noise_{RMS}}\right)$ brought to the input of the comparator (modeled in Figure 41). Assuming gaussian noise distribution, it is then possible to express inter stage redundancy implemented in the second stage through these different parameters as described in the following sub-section.

3.1.2.2 Inter stage redundancy

To express the required dynamic of the redundancy implemented in the second stage, a worst case scenario must be described. As discussed, this correction must address two types of errors in the second stage. One is a sign error made by the SAR which the second stage must correct. The second is a residue too large compared to the theoretical full scale of the second stage.

Both situations can be described according to equation (3.3) with the variable ε representing the extra voltage to cover with the redundancy. This error describes an error made in the first stage and transferred to the second stage through the CDAC code. The noise $\left(\mathrm{V}_{\mathrm{noie}_{\mathrm{SAR}}}\right)$ and the offset $\left(\mathrm{V}_{\mathrm{off}_{\mathrm{SAR}}}\right)$ of the D-CMP are the parameters take in account here. Nevertheless, the offset $\left(\mathrm{V}_{\mathrm{off}_{\mathrm{DS}}}\right)$ of the CT-CMP also induces an equivalent shift to input voltage seen by the CT-CMP. These 3 parameters are then used to size the inter stage redundancy. The instantaneous noise voltage of the D-CMP is considered within 3σ range for the sizing of the redundancy which is commonly admitted in analog design. An extension of the equation (3.3) describes the voltage residue converted by the second stage including noise and offset of the comparators:

$$V_{res} = V_{res_{ideal}} + \left(\mathrm{V}_{\mathrm{off}_{\mathrm{SAR}}} + \mathrm{V}_{\mathrm{noise}_{\mathrm{SAR}}}\right) + \mathrm{V}_{\mathrm{off}_{\mathrm{DS}}} \tag{3.4}$$

The inter stage redundancy implemented in the second stage must then be able to cover the excursion of these 3 parameters added to every ideal voltage residue. It can be described as:

$$\mathrm{redundancy}_{\mathrm{dyn}} > \left(\mathrm{V}_{\mathrm{off}_{\mathrm{SAR}_{max}}} + \mathrm{V}_{\mathrm{noise}_{\mathrm{SAR}_{max}}}\right) + \mathrm{V}_{\mathrm{off}_{\mathrm{DS}_{max}}} \tag{3.5}$$

The maximums offset value possible regarding PVT and temperature variation must then be known to size the interstage redundancy in accordance with (3.5). It can be seen that the need of voltage dynamics in interstage redundancy could be important regarding the voltage full scale of the second stage. As a trade off in this system proposition, an offset calibration scheme is proposed to reduce their impact during conversion. It thus relaxes the dynamic voltage requirement for the interstage redundancy.

The two discussed interstage redundancies required could be sized differently according to the excursion of these parameters. For the model presented in this work both redundancies have been sized similarly. This allows an optimized system implementation presented in next sections.

However, this analysis of the errors transmitted to the second stage is correct as long as the comparators are the main contributors to this error. In fact, the CDAC and the reference voltage could also induce errors in the first stage bit decisions. One of the error mechanisms is incomplete settling of the

floating node voltage which depends on the size of the bottom plate switches and the voltage reference output impedance. This work does not address the voltage reference study and is ahead of schedule compared to the global system. However, an additional error correction is implemented in the SAR architecture to relax the requirements put on switches and reference voltage and thus make the effect of these errors on the 2nd stage negligeable compared to the errors of the comparators.

3.1.2.3 SAR redundancy

The firsts conversion steps are the most critical in the SAR algorithm due to the contribution of the settling error that is proportional to the step size. To guarantee that the first comparison errors cannot impact the second stage another redundancy scheme is introduced in the SAR. This correction is made by adding a step to the SAR algorithm which allows to reduce the error below 1 SAR LSB [71].

Figure 44 (a) shows a representation of the evolution of the residue during the SAR algorithm for different situations. The residue is represented along the SAR conversion with its equivalent digital code for reading simplification and rescaled to the relative value of each bit. The binary search algorithm is unrolled from left to right. If the equivalent code is greater than the mid code of the current range of the bit, half the current dynamic is subtracted before the next comparison, otherwise, nothing is done. Figure 44 (b) presents a 9 bit example of SAR conversion without error and Figure 44 (c) draws the same situation with an error of 7 SAR LSB occurring at the 5th comparison that could be a settling error. The error is stored in the residue which now exceeds the dynamic of the next bit ranges. The error appears in the 5 LSB of the final digital code [01111 (=15) instead of 10110 (=22)]. To mitigate such errors, the CDAC values are modified, and a redundancy step is introduced, the numerical weight of each bit must then be coherent with these modifications for the recombination of the code. To apply this redundancy, a part of the MSB capacitance representing 16 SAR LSB in Figure 44 is removed from the MSB equivalent capacitance. This induces smaller voltage shift after the first comparison, thus increasing the voltage dynamic of next comparisons. Once the bit decision corresponds to the removed dynamic from SAR in the example 16 LSB SAR, it is operated two times to remove the extra dynamic present until there. This extra comparison in the SAR process allows bit recombination from b[9] to b[4] with a recovery range of $\pm 8LSB$ in this example. To recombine code, the sum of each bits must no longer be weighted with powers of 2 but with the equivalent weight along the conversion (in Figure 44 (d), b[8] is no longer equivalent to code 255 but to code 255+16 and so on). As can be seen on Figure 44 (d), the decision error at the 5th comparison is now corrected in the subsequent steps.

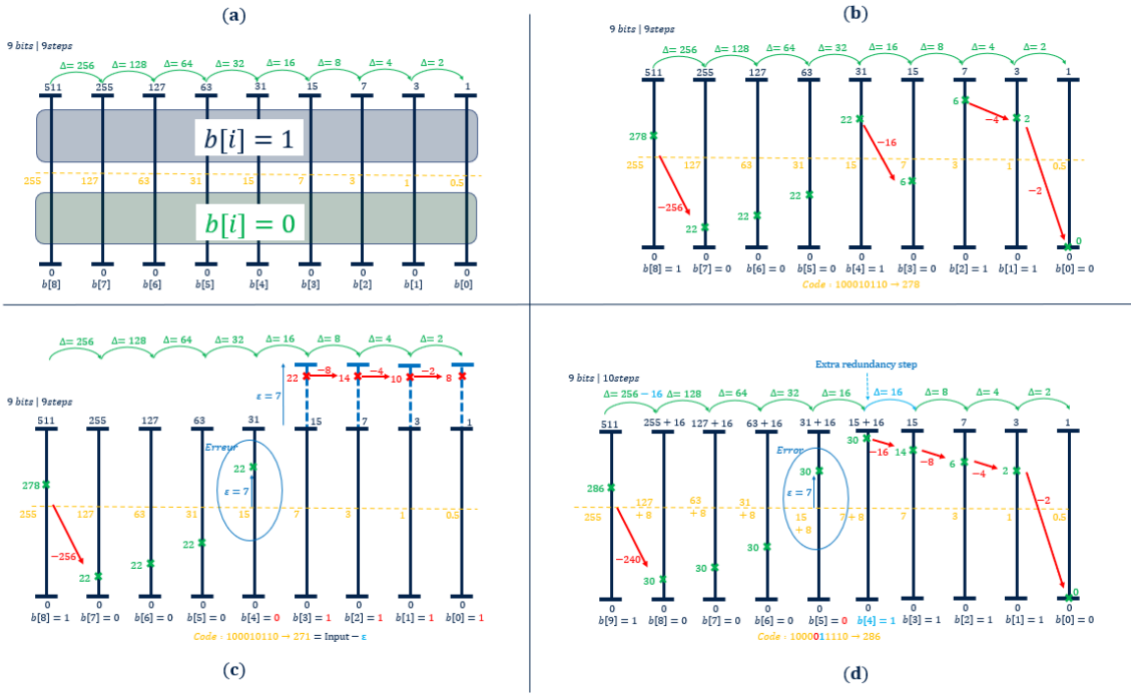

Figure 44 - Representation of the voltage residue equivalent code through 9 bit SAR example process with, bit decision area (a), example of non-error conversion without redundancy (b), example of conversion with error without redundancy (c), and example of conversion with error and extra step redundancy on 6th comparison to correct the code (d)

With this added redundancy in the system, harmful errors occurring during the first conversion steps of the SAR can be corrected and will not affect the second stage No matter the kind of phenomena causing the error, settling time of the capacitance, charge injection or noise, if the error is done before the extra redundancy step and within the redundancy dynamic, the correction is invisible for the second stage.

The presented built-in CDAC redundancy allows the system to correct errors made on the first bit evaluation of the SAR. This permits the previous analysis to consider the comparator as the main error contributor for the second stage along the last SAR bit evaluation are mainly impacted by it. However, the switches and the voltage references must be designed in accordance with the built-in SAR redundancy to achieve efficient correction. The example presented in this section looks like a reasonable tradeoff.

As discussed in the previous section, the comparators offset must be calibrated. The next section presents the proposed calibration and compensation scheme implemented in the CDAC.

3.1.2.4 Offset calibration

Offset introduces a serious challenge to reach 12 bits resolution with the lowest consumption. Sizing offset by design of the comparators would require large transistors for the differential pairs in both comparators. This will add extra coupling capacitance, lower the bandwidth and so the speed of the ADC while adding extra surface and consumption. To avoid this non ideal optimization, a foreground calibration scheme is proposed by adding extra capacitances to the CDAC, dedicated to measure and correct offsets of the D-CMP and the CT-CMP. The extra part of the CDAC is used in a calibration phase to measure the offset of each comparator. Then during the conversion phase, the opposite voltage is applied by the extra CDAC to cancel the offset effect. As the two comparators are never used simultaneously, a single calibration DAC can be used to correct offsets of both comparators. Figure 45 shows the proposed architecture with an extra 12 bit LSB precision CDAC ($CDAC_{Calib}$) dedicated to offset measurement and cancellation.

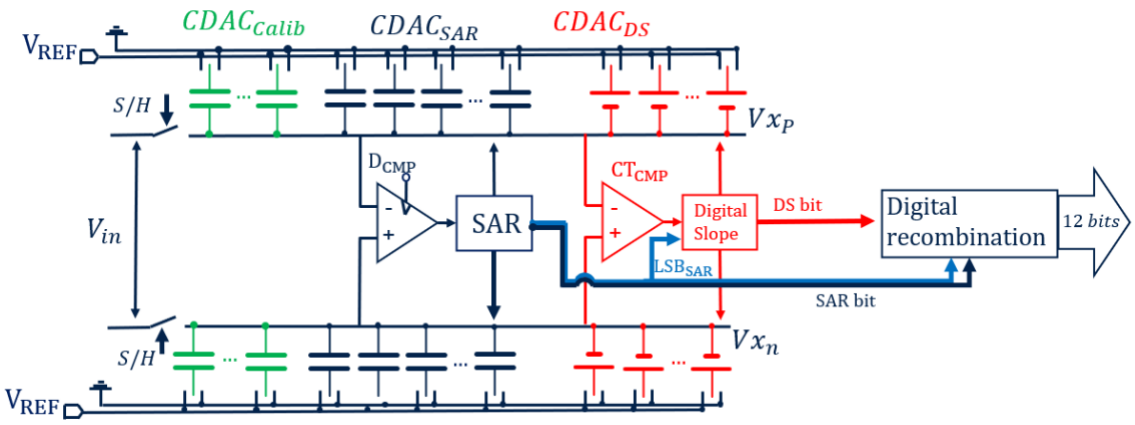

Figure 45 - Proposed architecture with offset calibration dedicated CDAC- concept diagram block

The proposed foreground calibration for the D-CMP works as follows: A zero differential voltage around the common mode voltage is first sampled into the CDAC. The input voltage seen by the D-CMP is thus equal to 0+$V_{off_{SAR}}$ because the sampled voltage is null. Only the calibration CDAC is then used with a SAR algorithm to encode the value of the offset. The code obtained correspond then to the offset of the D-CMP, this code is stored at the end of the calibration. To correct offset, the stored code is applied to the calibration CDAC after the sampling phase during normal operation of the SAR to cancel the effect of the D-CMP offset. Figure 46 shows the evolution of floating node voltages during the calibration scheme on the top plate of the CDAC (Figure 46 (a)) and seen by the comparator with offset added to its input (Figure 46 (b)).

The maximum offset value that can be corrected depends on the range of $CDAC_{Calib}$. Furthermore, the calibration algorithm is also suffering from comparator errors induced by noise. To overcome this, the calibration protocol can repeat several times the measurement of the offset and then use the mean value for the offset correction. Because offset can also be influenced by temperature or supply voltage changes, the offset calibration can be done at regular intervals to update the correction code.

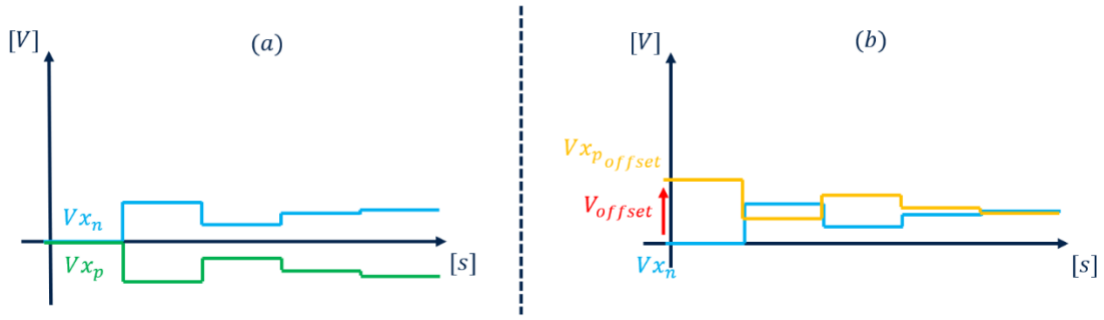

Figure 46 - Representation of the voltage evolution in the proposed foreground calibration on the top plate of the CDAC (a) and seen by the comparator presenting offset (b)

The CT-CMP offset measurement is done in a similar way. An extra latch is required at CT-CMP output for this purpose as this comparator is not working natively in discrete time. The calibration process uses a specific clock with a clock frequency compatible with the limited bandwidth of the continuous-time comparator. As the calibration is done in foreground during idle times the clock frequency can be chosen sufficiently low to eliminate possible settling errors.

Once both comparator offsets are measured, the corresponding codes can be fed to the $CDAC_{calib}$ when the D-CMP and C-CMP are effectively used. The residual offset of the comparators is reduced below 1 LSB (defined as the 12 bit LSB of the global converter). As discussed before, interstage redundancy will correct the error due to the residual offset of the D-CMP. The residual offset of the CT-CMP however cannot be corrected and will limit the precision of the ADC.

3.1.2.5 CT-CMP Latency

Through previous sections, the impact of the first stage on the second has been discussed as the techniques to reduce it. In this section the second stage errors are discussed independently of the first stage.

In the Digital Slope architecture the digital slope is directly driven by the delay line which makes it to a first order independent of delay errors in the delay line. The steepness of the digital slope is directly proportional to the average time delay of the elementary delay elements. Standard variation of the time

delay of delay elements has a negligeable effect as long as the variation remains small compared to the mean value.

The CT-CMP latency and noise remain the main sources of impairments as the offset is corrected and the residual offset should be below 1 LSB. The noise presented by the CT-CMP cannot be corrected nor compensated by the system and directly affects the result of the overall conversion. The comparator must therefore be designed to meet the performance requirements for the overall ADC, which is 12 bit resolution in the present case.

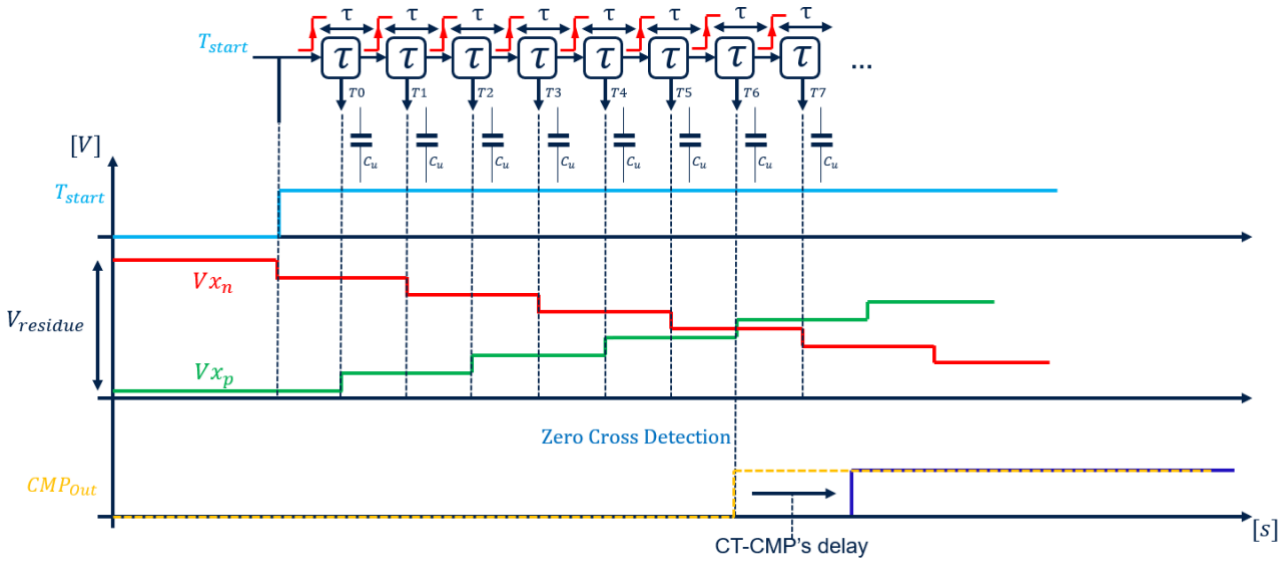

Figure 47 - Representation of the second stage comparator latency compared to ideal output with bidirectional slope

The latency of the CT-CMP directly impacts the output code of the second stage by counting extra time after the cross voltage at the input. This latency is considered constant in this section and a more detailed discussion will be presented in chapters 4 and 5 studying the impact of the CT-CMP bandwidth on the performance. To underline this phenomena Figure 20 depicts a conversion as shown in Figure 6 where the delay line is partially represented to underline the link between ramp steps and crossing detection with delay. In the given representation, the input voltage crossing occurs at T6. An ideal comparator would switch instantaneously, but due to the latency the comparator response to the crossing appears with a dely. The code latched in the delay line is larger than the expected one. This latency considered constant here is equivalent to a time offset which can be corrected digitally if its known.

A constant delay adds a fixed number to the output code which corresponds to the quantized comparator latency. If for example the CT-CMP latency is equal to 2 delay line units, this means that the minimum code observable is the value of 2 in the second stage. This value must be subtracted from each code to

correct the latency impact. The effective quantization error is however modified, as the comparator latency is itself quantized. This inherently can add an additional constant error of up to 1 LSB which behaves the same way as an offset on the signal. The disadvantage is however of the bi-directional ramp architecture is however that this error changes sign with the ramp direction. Indeed, the 2nd stage always outputs a positive value, the sign is then corrected depending on the residue sign-bit provided by the SAR.

3.1.2.6 Latency correction

Because the latency of the CT-CMP is analog to an offset voltage, le latency can be determined by providing a known ramp starting point to the system and then start the conversion. Figure 48 presents the timing diagram of the delay line controlling the digital slope along the latency measurement. A known quantized voltage is present at the begin of the ramp and allows to predict the crossing voltage point and consequently the ideal output code. Due to the delay on the rising edge of the comparator output signal, the measured code will higher than expected. The difference between measured and expected code represents the latency quantified with a unit delay resolution.

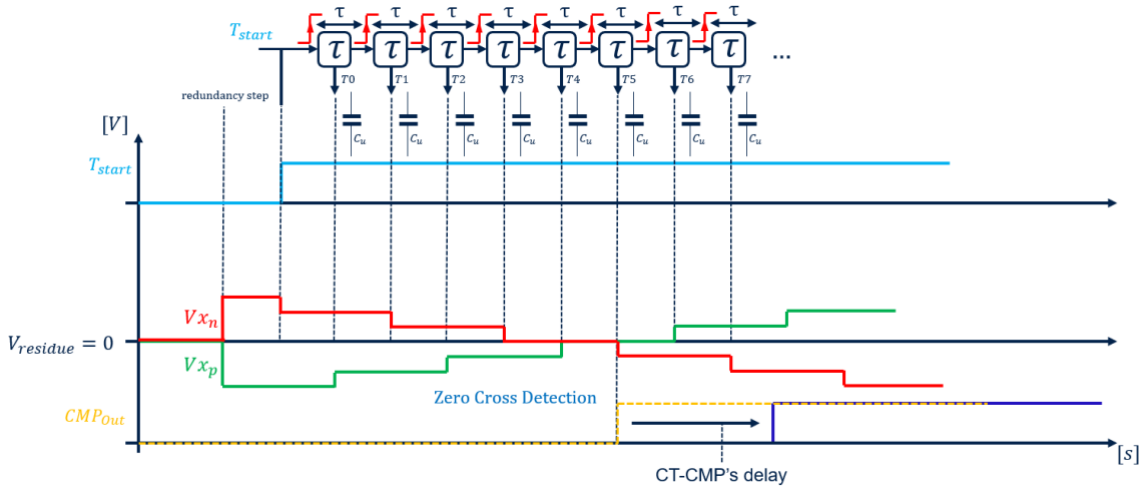

Figure 48 – Timing diagram of the proposed delay measurement of the comparator using redundancy as expected result.

Some precautions need to be taken in the actual calibration procedure. Indeed, comparator offset will also affect the latency measurement with an error that depends on the ramp direction. Thus, the offset voltage must be measured and compensated before proceeding to the latency measurement. To get a more accurate result, averaging is also proposed for the latency measurement. Once the latency is known, its equivalent digital offset can be subtracted to every code converted by the second stage. It must also be kept in mind that the calibration is effective as long as the comparator latency can be considered to remain constant. It should be checked to what extend temperature or supply voltage variations affect the latency. It could be necessary to recalibrate the ADC after an appropriate laps of time.

A final consideration regarding the latency calibration is the fact that the delay line also needs to be modified. Indeed, for an input voltage corresponding to a code close to the end of the ramp, the extra time delay due to the comparator latency will cause an overflow of the delay line. For a given example of a 3 bit DS with an additional bit for redundancy, the output code has 16 possible values representing input values from [-4;11] corresponding to the ideal range [0;7] extended on both ends with 4 extra codes. If the comparator latency adds 3 LSB of offset on every code, the code '8' is pushed to the end of the line and codes '9', '10' and '11' will never appear. To avoid this situation as in Liu's work the delay line must be extended with delays not connected to capacitors. The number of extra stages must provide enough overhead for the maximum expected latency. Figure 49 represents an example for a 3 bit plus 1 bit redundancy delay line designed for a 6 unit delay comparator latency. The digital correction has to shift the output code by 6 unit values as represented in the right part of the figure. Therefore, at least 6 extra delay elements are needed to prevent the loss of information. The comparator latency adds some extra time to the conversion operation as delay introduced by the comparator can note be used for any other purpose and increases the initial conversion time.

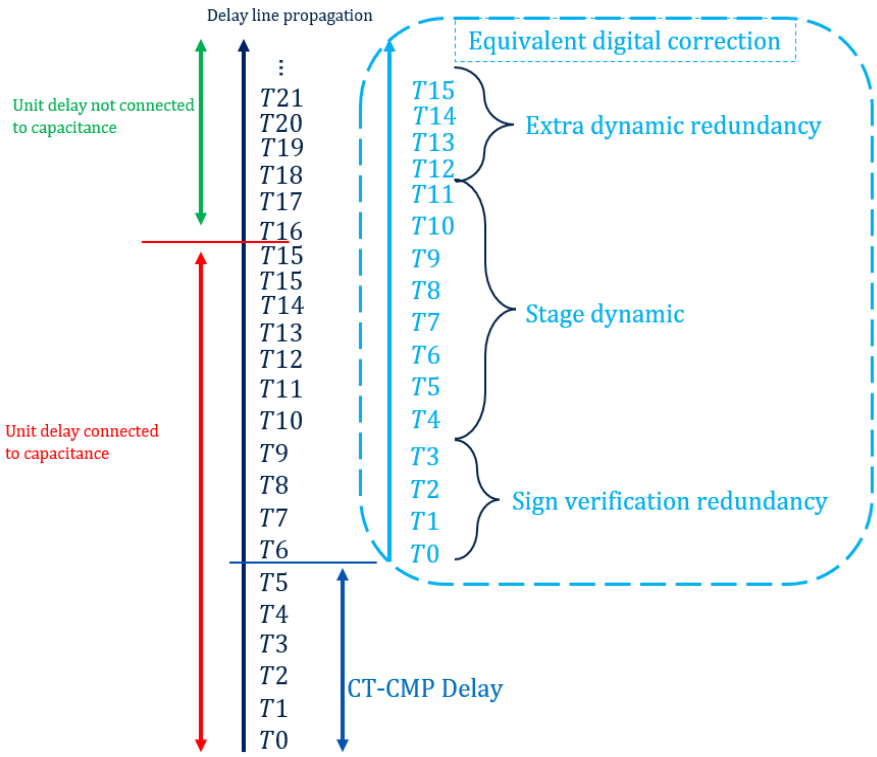

Figure 49 – 3 bit + 1 bit redundancy delay line equivalent thermometric code with proposed digital correction for 6T CT-CMP delay

3.1.2.7 DAC non idealities

Another critical block in the proposed ADC is the CDAC, used as sampling capacitance and analog feedback for both converter stages. The CDAC can introduce errors, namely settling errors and matching errors. Redundancy can correct settling errors as described earlier.

The matching of the capacitance can alter the capacitive ratios and so the equivalent voltage conversion of a digital word. To ensure that the differential non ideality of code (DNL) cannot cause missing codes, its maximum amplitude must be less than one LSB of the ADC. If two successive DNL errors occur the same polarity, the sum must remain under a LSB so:

$$|\mathrm{DNL_{max}}| < \frac{1}{2}\mathrm{LSB} \tag{3.6}$$

In a binary weighted CDAC, the highest DNL errors are expected at the transitions where a large number of capacitors are switched. The most critical transition is the one form '1000000…' and '0111111…' as all capacitors are switched. The corresponding DNL is called $\mathrm{DNL_{mid}}$. The proposed CDAC is composed of unit capacitances grouped to form the binary scaling of the CDAC which allows to express $\mathrm{DNL_{mid}}$ as:

$$|\mathrm{DNL_{max}}| = DNL_{mid} = \frac{\left(\sum_{i=0}^{n-1}\sqrt{w_i}\right).\sigma_u}{2.C_u} \tag{3.7}$$

Where w_i represents the weight of the successive capacitances present in the CDAC from LSB to MSB. The parameter $\frac{\sigma_u}{2.C_u}$ expresses the unit capacitance variation. Note that the factor two arises because of the differential implementation. This property is used to size the CDAC correctly in regard to the non-linearity impact on the ADC performance.

The CDAC also induces noise [72], both during the sampling and during the switching of its capacitance through conversion algorithms. This is due to the thermal noise of the switch component, usually MOS transistors. This noise is integrated by the capacitance and is well known in the sizing of ADC (given in the next section) during the sampling phase.

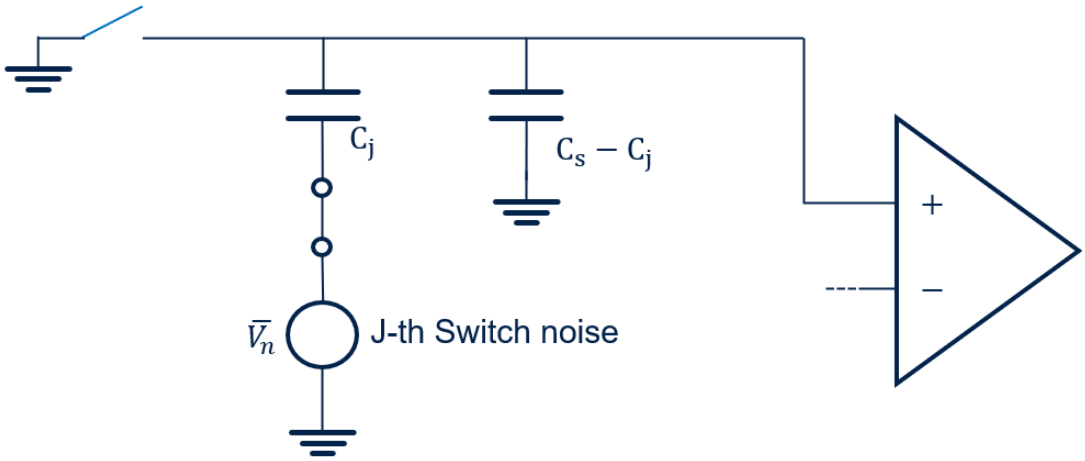

Figure 50 - Noise model in CDAC based ADC in the evaluation phase with Cj capacitance switched amongst Cs capacitance used in the sampling phase.

But noise added by the switching of successive capacitance C_j during evaluation phase as represented in Figure 50 is also to consider and can be modeled as:

$$Pn_{DAC} = \frac{2KT.C_s}{C_j.(C_s - C_j)}.\left(\frac{C_j}{C_s}\right)^2 \quad (3.8)$$

3.1.2.8 Noise balance

The previous sections describe the major non idealities and their impact on the performance for the proposed architecture. This section addresses the noise balance, not taking into account non-linear effects that will contribute to the SNDR. The performances in terms of will depend on the design choices for the circuit implementation and the tradeoffs taken for redundancy and correction schemes. To quantify the SNR in dB, the signal power signal must be compared to the total noise power as shown in equation (3.9).

$$SNR[dB] = 10.\log\left(\frac{p_{sig}}{p_{noise}}\right) \quad (3.9)$$

The actual signal power depends on the use of the ADC. However, to specify performance and to compare the ADC rigorously with other ADC realizations, reference input signal must be considered. Classically a full-scale sinusoidal signal (constant wave) is used as reference:

$$SNR[dB] = 10.\log\left(\frac{\left(\frac{V_{FS,pp}}{2\sqrt{2}}\right)^2}{p_{noise}}\right) \tag{3.10}$$

With the given equation (3.10), where $V_{FS,pp}$ is the full-scale peak to peak input voltage. The maximum allowable noise power can then be expressed as a function of $V_{FS,pp}$ and the targeted signal to noise ratio:

$$p_{noise}[V^2] = \frac{\left(\frac{V_{FS,pp}}{2\sqrt{2}}\right)^2}{10^{\frac{SNR[dB]}{10}}} \tag{3.11}$$

The total noise allowed in the overall ADC can be sized with the target SNR and the available full-scale signal amplitude which is typically close to the supply voltages. Different contributors will contribute to the noise power. I. e., the CT-CMP noise is directly added to the total noise power as it cannot be compensated in the circuit. On the other hand, the noise induced by the SAR DT-CMP is not taken in account, considered as being corrected by the redundancy scheme. Considering a 3σ margin for the maximum instantaneous noise sample, the redundancy must be sized as:

$$Dyn_{redundancy}[V] > 3.V_{D_{cmp}noise_{RMS}} \tag{3.12}$$

To allow correction of the comparator noise with high reliability. Offsets and the CT-CMP latency produce constant errors and don't contribute to the noise budget. Their effect on ADC accuracy is corrected by the foreground calibration and digital post-treatment.

The remaining contributions are intrinsic ADC noise sources due to sampling and quantization noise. The noise sources are described as follows:

$$\mathrm{Q_{noise}[V^2]} = \frac{\left(\frac{\mathrm{V_{FS,pp}}}{2^{\mathrm{n}}}\right)^2}{12} \tag{3.13}$$

$$\mathrm{Sampling_{noise}[V^2]} = 2\frac{\mathrm{KT}}{\mathrm{C_s}} \tag{3.14}$$

Where C_s is the total capacitance of each half of the differential CDAC. Note that the factor 2 arises from the differential implementation.

With the analysis of errors sources and corrections implemented in the architecture, the overall noise power can be expressed as:

$$\mathrm{p_{noise}[V^2]} = \mathrm{Q_{noise}} + \mathrm{Sampling_{noise}} + \mathrm{Pn_{DAC}} + \mathrm{CT\text{-}CMP_{noise}} \quad (3.15)$$

As discussed previously, this work does not address the design and contributions of the voltage reference. Thanks to the SAR built-in redundancy the constraints put on voltage references and switches are relaxed but their impact on noise performances must be consider for realization. A regulated power supply such as LDO would probably be required to have sufficiently low noise level.

3.1.2.9 Extra capacitance impact on dynamic

The proposed SAR assisted topology is sensitive to the variation of its CDAC value and extra capacitance not switched by the algorithms. Because the sampling capacitance and the CDAC are the same, if extra capacitance as parasitic or voluntary added like the $\mathrm{CDAC_{Calib}}$ section is present, the dynamic of the ADC is reduced [71]. The dynamic of the proposed ADC corresponds to the dynamic of its CDAC represented $V_{FS,pp}$ in (3.10) and it can be expressed as:

$$V_{FS,pp}[\mathrm{V}] = \frac{\mathrm{C_{DAC}}}{C_s} V_{DAC,pp} \quad (3.16)$$

With $\mathrm{V_{DAC,pp}}$ representing the voltage swing of the CDAC according to its voltage references. With no extra capacitance, the sampling capacitance can be expressed as:

$$C_s = C_{DAC} \quad (3.17)$$

Equation (3.17) is not realistic as even with careful design parasitic capacitances need to be taken into account. In addition, extra capacitances can be added on purpose it is the case in the proposed ADC architecture. We therefore define

$$C_s = C_{DAC} + C_h \quad (3.18)$$

with C_h being the total additional capacitance present on the floating node. This additional capacitance is not used by the CDAC and reduces the equivalent dynamic as described in (3.16).

Parasitic capacitances on the top plate can thus degrade the SNR by reducing the maximum allowable input signal amplitude as shown in (3.10). Other additional capacitances such as the $\mathrm{CDAC_{Calib}}$ section and the capacitors for the digital ramp also contribute to the reduction of the dynamic range. For example, with a $\mathrm{V_{DAC,pp}}$ of 1.8V and an extra capacitance equal to 12% of the CDAC capacitance, the SNR is degraded by 0.98dB. However, a full scale input signal amplitude close to the power supply voltage is not always possible. In the the power supply is used as a reference, the extra capacitance can be

used to resize the input voltage dynamic of the ADC to match the available signal amplitude in the system [71].

3.2 Sizing of the proposed architecture

3.2.1 Bit repartition between stages

In this section details are given concerning the quantitative values in the architecture. Theoretical concepts have been developed in the previous sections and practical choices and optimization are given here.

From a versatile perspective, the proposed ADC must be used in multiple situations with a good energy performance. The industrial context of this work guides architecture design to propose different uses of the developed ADC. Two different use cases are required: for the less exigent situations ~9 bit ENOB are sufficient for the overall ADC, while for other situations the full performance of the ADC is needed as defined in chapter 1. To satisfy this constraint this work proposes two modes with its two stages ADC by turning off the second stage in 9 bit performance. This will lead to the following bit repartition between stages.

To distribute the 12 bit resolution targeted in this work different aspects have been take in consideration:

- 1: The SAR consumption mostly due to the D-CMP comparator, which tends to increase exponentially with the resolution (comparator consumption in regards of resolution given in Figure 51)
- 2: The DS consumption is proportional to the time spent with the CT-CMP on, and so with the length of the delay line.
- 3: Redundancy requirements of the second stage depend on the coarse resolution sizing.
- 4: Sampling capacitance value impacts the thermal noise parameter of the ADC but also the consumption of the previous block in the system. A fast sampling requirement on large sampling capacitance needs important power consumption.
- 5: The $\mathrm{CDAC}_{\mathrm{calib}}$ used for the offset calibration will reduce the dynamic as well as the top plate capacitance parasitic.
- 6: The targeted 64MS/s sampling frequency allows 15.6ns for the total conversion time.

With the previous aspects the overall ADC has been designed with:

- 9 bits on the coarse ADC SAR + 1 bit of redundancy.

- 3 bits on the fine ADC DS + 1bit of redundancy.

The above segmentation has been setup as a good compromise for both use cases.

SAR ADC with 9 bit of resolution is a well-known topology, proven energy efficient.

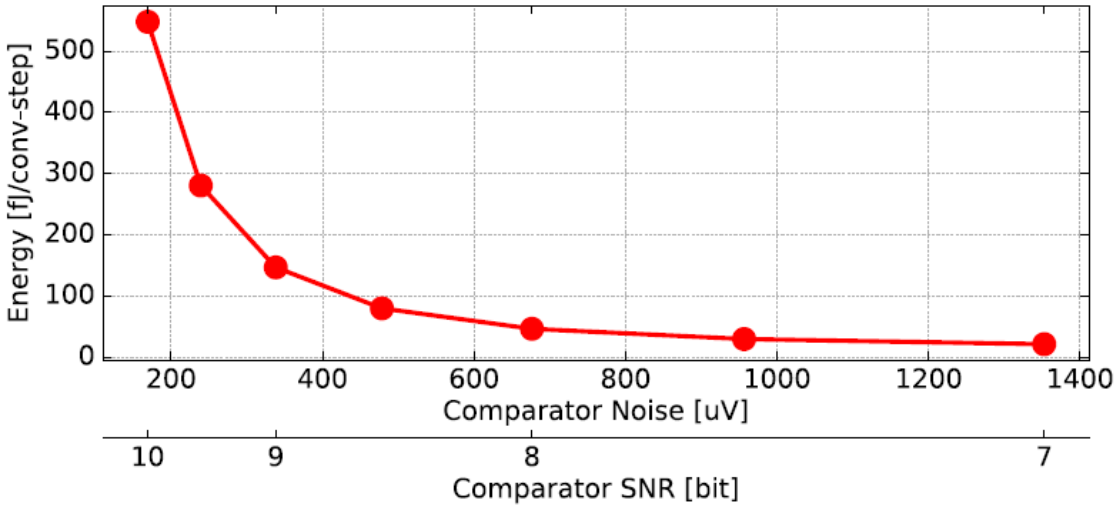

Figure 51- From *[87]*, energy consumption by conversion step of a strong-arm comparator as a function of its input referred noise. Simulated 5fF capacitive load in 65nm.

As a standalone ADC, 9 bit SAR is enough to ensure the low resolution mode asked by the industrial context of this work, while remaining interesting compromise in terms of resolution and power consumption as shown Figure 51 with the energy consumed by a strong arm comparator in a SAR topology regarding its effective resolution. The DS stage used to reach expected 67 dB of SNR given in chapter 1 sized with 3 bit plus 1 of redundancy has to use 16 unit delay in the delay line. This is reasonable stage size for which its consumption is proportional to its length. The unit delays are intended to be as short as the technology allows it to reduce the time spent in the second stage of conversion. The continuous time comparator being anyway constraint by its noise added to the overall noise, its timing performances must be challenged to ensure optimized use of the second stage. The built-in redundancy added in the SAR is aimed to correct potential errors in the 6 first steps. The 1 bit redundancy in the second stage is sized to correct LSBs SAR errors and ensure correct behavior of the second stage in presence of SAR errors.

3.2.2 Noise balance in the proposed architecture

With details of implementation and analysis of major noise contributors done in the previous sections, the overall sizing of the architecture follows.

From a system point of view as aforementioned the value of the CDAC capacitance has impact on the previous block in the chain. The timing constraints require the sample and hold circuit to charge with precision the sampling capacitance in a minimum time. For a given time imposed by the settling precision require for the conversion, the S/H consumption is proportional to the size of the capacitance. Because the ADC is designed with 12 bit resolution, this represents a theoretical SNR of 74 dB which is higher than the 67 dB targeted. Margin is thus available to make trade offs and to reduce the consumption from previous block in the chain. The sampling capacitor has been sized to make the sampling noise power equal to the quantification noise power:

$$\frac{Q^2}{12} \approx 2\frac{KT}{C_{DAC}} \tag{3.19}$$

This choice induces directly a 3 dB loss on the SNR but the CDAC value is downsized to $0.615fF$.

The layout is done with custom capacitance pattern targeted to implement each capacitance present in the CDAC. Parasitic capacitances are evaluated with post layout simulation.

Full scale of the ADC is impacted by top plate parasitic capacitance, and thus SNR is reduced as expressed in (3.16), by considering the part of the CDAC used by the calibration and the parasitic capacitance. From a ideal differential full scale of 1.8V, the effective differential full scale is expected around 1.62V. This affects the SNR and the effective noise sized in (3.19).

By knowing the voltage dynamic of the ADC, the budget can be described from the target of this work at 67 dB as:

- (3.10): $SNR = 10.\log\left(\frac{\left(\frac{1.62V_{pp}}{2\sqrt{2}}\right)^2}{p_{noise}}\right) = 67$ dB
- (3.11): $p_{noise}[V^2] = \frac{\left(\frac{1.62\,V_{pp}}{2\sqrt{2}}\right)^2}{10^{\frac{68\,dB}{10}}} \approx 65\text{nV}^2$

The noise power of the different contributors added together must be below the global allowable noise power of 65nV² to reach targeted performances.

Because the parasitic capacitances affect the expected noise from the CDAC switching. From equation (3.8) the noise is estimated in regards of the switching scheme of the SAR. With the proposed split monotonic CDAC, the noise power added to the input voltage of the comparator is divided by 4 because switched capacitances are half smaller in regards of the overall CDAC than classical switching scheme. With the implementation of thermometric MSB to reduce mismatch impact, the biggest capacitance to switch is also smaller which reduces the added noise. From equation (3.8), an extension of the formula is used to take the bottom plate capacitance in account as:

$$Pn_{DAC} = \frac{2KT}{C_{bp} + \frac{C_j.(C_s - C_j)}{C_s}} . \left(\frac{C_j}{C_s}\right)^2 \tag{3.20}$$

Where C_{bp} represents the bottom plate parasitic capacitance. With the discussed value the noise induced by the switch of CDAC estimated with (3.20) and the thermometric representation of the 3 MSB in the SAR is expected as:

$$Pn_{DAC} = 3.24nV^2 \tag{3.21}$$

To complete numerical values considered in the total noise (3.15), the quantification (3.13) and sampling (3.14) noises are evaluated as:

$$\mathrm{Q_{noise}[V^2]} = \frac{\left(\frac{1.62}{2^{12}}\right)^2}{12} = 13nV^2 \tag{3.22}$$

$$\mathrm{Sampling_{noise}[V^2]} = 2\frac{\mathrm{KT}}{615fF + C_{par}} = 12nV^2 \tag{3.23}$$

The quantization noise is slightly higher than the sampling noise, because the sizing of the capacitance has been made before determining not taking into account the parasitic capacitance (C_{par}). The sampling noise is therefore slightly lower than quantization noise.

The noise budget for the D-CMP, it is determined for 3σ peak noise voltage equal to half a SAR LSB. This gives a noise power as:

$$V_{D_{cmp}noise_{RMS}} < \frac{1.62}{6 * 2^9} \approx 527\mu V_{RMS} \tag{3.24}$$

From this point the minimal inter stage redundancy required to cover noise and residual offset for the second stage is thus equal to ± 3 $\mathrm{LSB_{12\ bit}}$. To add margin, ± 4 $\mathrm{LSB_{12\ bit}}$ are implemented in the inter stage redundancy.

The noise budget of the CT-CMP appears relaxed compared to other realizations [3]. The noise power budget for the CT-CMP is:

$$\text{CT-CMP}_{\text{noise}} = 23.76\ nV^2 \tag{3.25}$$

The input referred noise of the CT-CMP considered as white noise over the comparator bandwidth must then present an RMS value below:

$$\text{IRN}_{\text{CTcmp}_{\text{RMS}}} < 154.14\mu\text{V}_{\text{RMS}} \tag{3.26}$$

With the pre-mentioned noise budgets, a additional margin exists with respect to the maximum allowable noise power :

$$Margin = p_{noise} - (Pn_{DAC} + \text{Sampling}_{\text{noise}} + \text{Q}_{\text{noise}} + \text{CT-CMP}_{\text{noise}}) = 13\text{nV}^2$$

The presented margin allows to design and target specifications while keeping some security in regard of the silicon realization.

3.2.3 Details of proposed architecture

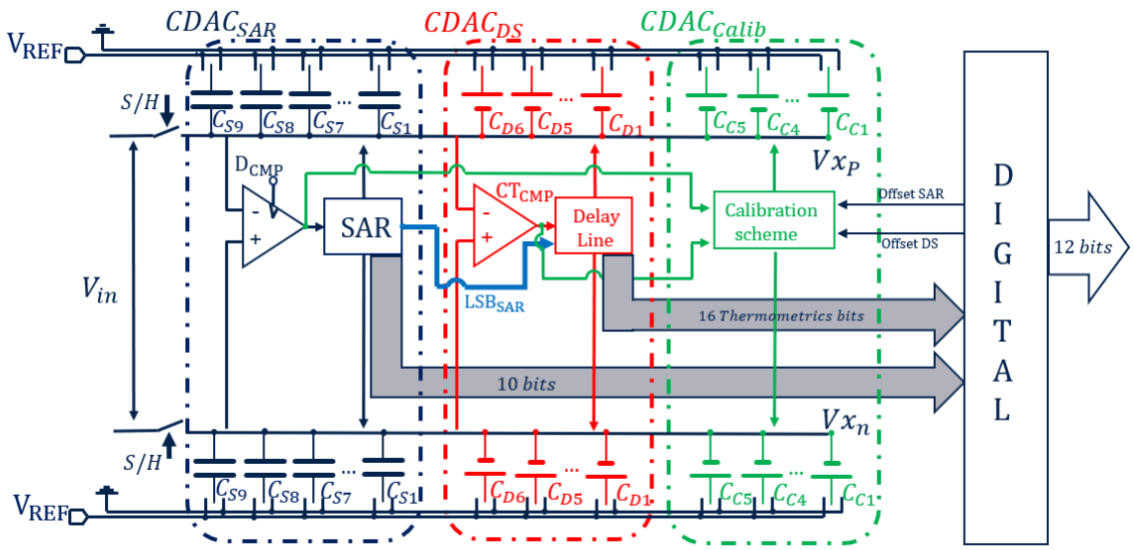

Figure 52 - SAR-Assisted Two stages differential DS block schematic

To realize the proposed architecture of SAR assisted 2 step ADC in accordance with the previous sizing all the previous concepts are put together in the same architecture. The architecture is thus composed of a 9 bit (plus 1 bit of redundancy) SAR stage as coarse converter and a 3 bit (plus 1 bit of redundancy) bidirectional ramp stage based on digital slope as fine converter presented in Figure 52. The aforementioned calibration section to correct offsets is also implemented in the CDAC of the proposed ADC. This ADC is targeted for a 18nm CMOS FDSOI technology with 0.9V supply voltage.

The core of the converter is a DAC based on capacitance switching, both coarse and fine ADC use different portions of the same CDAC one after another. The main concept in this architecture is residue sharing. As input is sampled into the CDAC, the SAR algorithm is implemented through the CDAC. All the information is still stored in capacitance at the end of the coarse operations. Once the first stage has done its conversion the second stage with more precision is turned on to convert the residue and thus finish the conversion process.

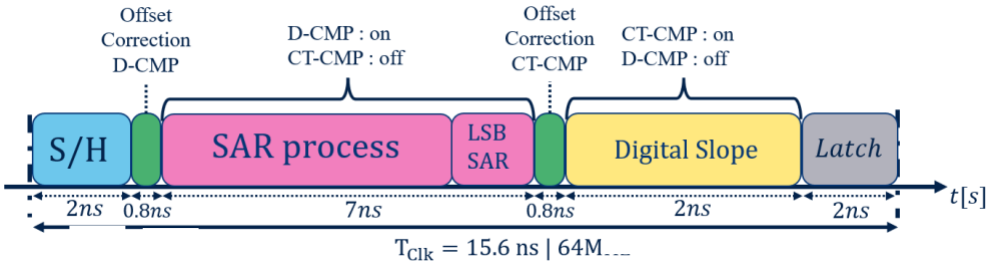

Figure 53 - Proposed ADC time sequence for 64MS/s

To avoid extra clock generation and reach the timing performances depicted in Figure 53, the SAR stage is made asynchronous. The last bit of the SAR is used by the digital slope stage to determine direction of the ramps in the second stage. Once both stages have completed their conversion the data is stored before digital recombination. As shown in Figure 53 the structure is not pipelined because both stages work on the same CDAC. The two stages operate sequentially: first the input is sampled into the CDAC, then the SAR converts MSBs before letting the DS convert the LSBs. The data are then stored into digital memory for post treatment. All these operations must be done in a 15.6ns window to reach the targeted 64MS/s conversion rate. The next sections will present the details of the SAR stage and the Digital slope stage.

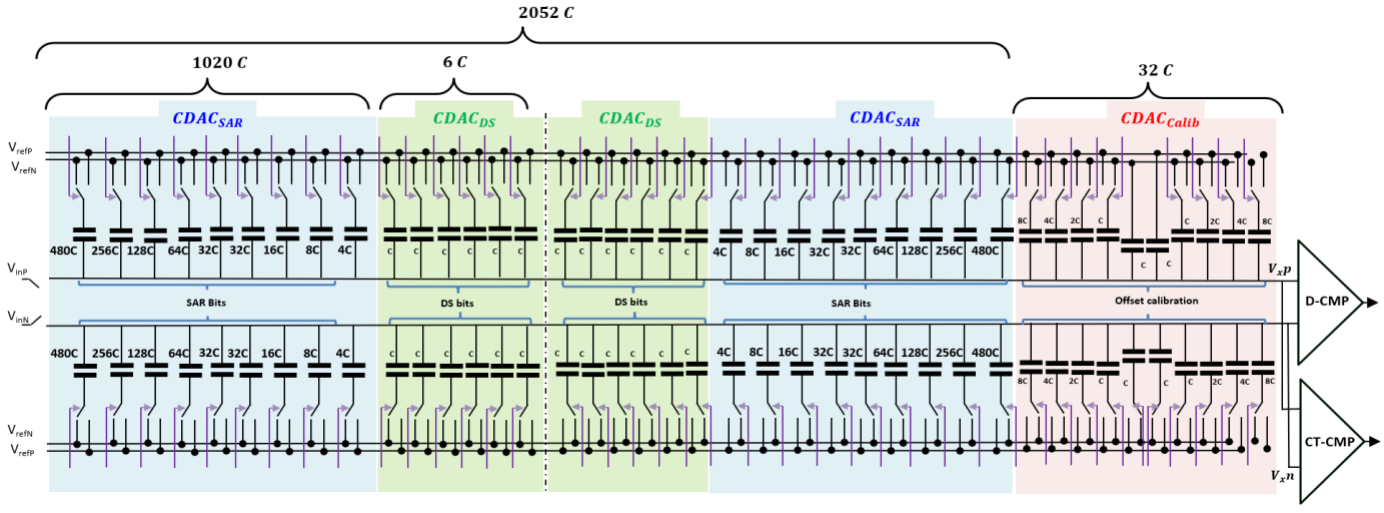

Figure 54 – Bloc-level representation of the differential CDAC used in the ADC for SAR, TDC and calibration purpose. [VrefP = VDD ; VrefN = GND]

From Figure 54, the calibration implemented in the CDAC allows an offset calibration within $\pm 16\ LSB$ coverage within $\pm 0.5\ LSB$ of accuracy by switching only one of the LSB capacitance for precision.

3.2.5 2nd stage Digital Slope description

The DS stage use in the proposed ADC presents a novel way to switch capacitances to optimize time spent with the second stage turn on. A novel switching scheme is also proposed to reduce the number of capacitances required for redundancy while increasing the effective resolution by 1 bit compared to the differential use of the CDAC.

As discussed, the proposed solution is pseudo differential digital slope because it consists in switching alternatively capacitors on the positive and negative branches. This alternate switching of the unit capacitors on both positive and negative branches increases the step resolution by 1 bit compared to a differential switching with the same CDAC (C instead of $2C$ changing state at a given time). This also keeps the common mode voltage at ramp crossing within 1 DS-ADC LSB window. Furthermore, slopes in the positive or negative direction can easily be created thanks to the split switching scheme adopted in the CDAC architecture, presented in Figure 54. This allows conversion of positive or negative residue voltages with the sign bit of the SAR ADC determining the direction which halves the range that needs to be covered by the digital slope. Figure 31 represents differential voltage evolution of a 2nd stage monotonic digital slope as presented in Figure 35, for both positive and negative residue.

The proposed bidirectional implementation halves the dynamic required by the second stage as depicted in Figure 55 by using the sign of the residue. A small level shift voltage is however implemented to correct any residual offset and noise errors of the SAR comparator as previously discussed.

To implement the ramps described in Figure 55, a 3 bit pseudo differential DS stage has been implemented as shown in Figure 56. To match the dynamic of the second stage with the residue, the total capacitance used to generate the ramp must be as large as the LSB SAR equivalent capacitor. In accordance with Figure 54, the capacitor switched by the second stage must represent at least 4-unit capacitance on each side of the CDAC. Because one bit of redundancy must be implemented, the second stage total capacitance value is twice. The capacitor array section dedicated to DS algorithm represented in green in Figure 54 is composed of 6 capacitors pairs on each side. When sampling the input signal, half of the 6 capacitors pairs is connected to VDD and the other to GND. The detailed bidirectional conversion is shown in Figure 57 for respectively positive and negative residues. In regards of implementation in Figure 56 and residue conversion examples in Figure 57, detailed switching procedure uses different capacitances depending on the sign. For a negative residue. first capacitors C1, C2, C13, and C14 are

switched simultaneously to create a 4 LSB offset. Then the conversion starts on the rising edge of T_{st} and C12 to C7 on positive side (Vx_p) and C24 to C19 on the negative side (Vx_n) are alternatively switched to generate the digital slope creating 12 LSB steps. The final 4 LSB steps are created by switching C2, C14, C13 and C1 successively to their original state. The ramp crossing voltage depends on the value of the residue, but it always occurs within a ± 0.5 LSB window around the common mode voltage. Operations for positive residue is similar with other half of the 6 capacitors pair, and slopes are inverted. Each capacitance bottom plate in DS stage is driven by the appropriate outputs of the delay line.

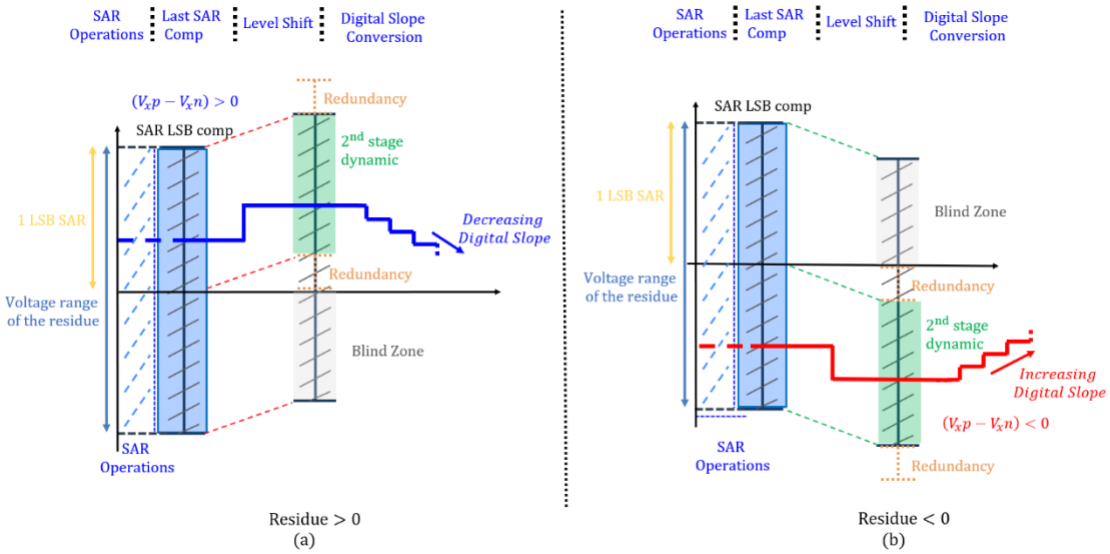

Figure 55 - Operation of a bidirectional 2nd stage digital slope (a) for positive residue - (b) for negative residue

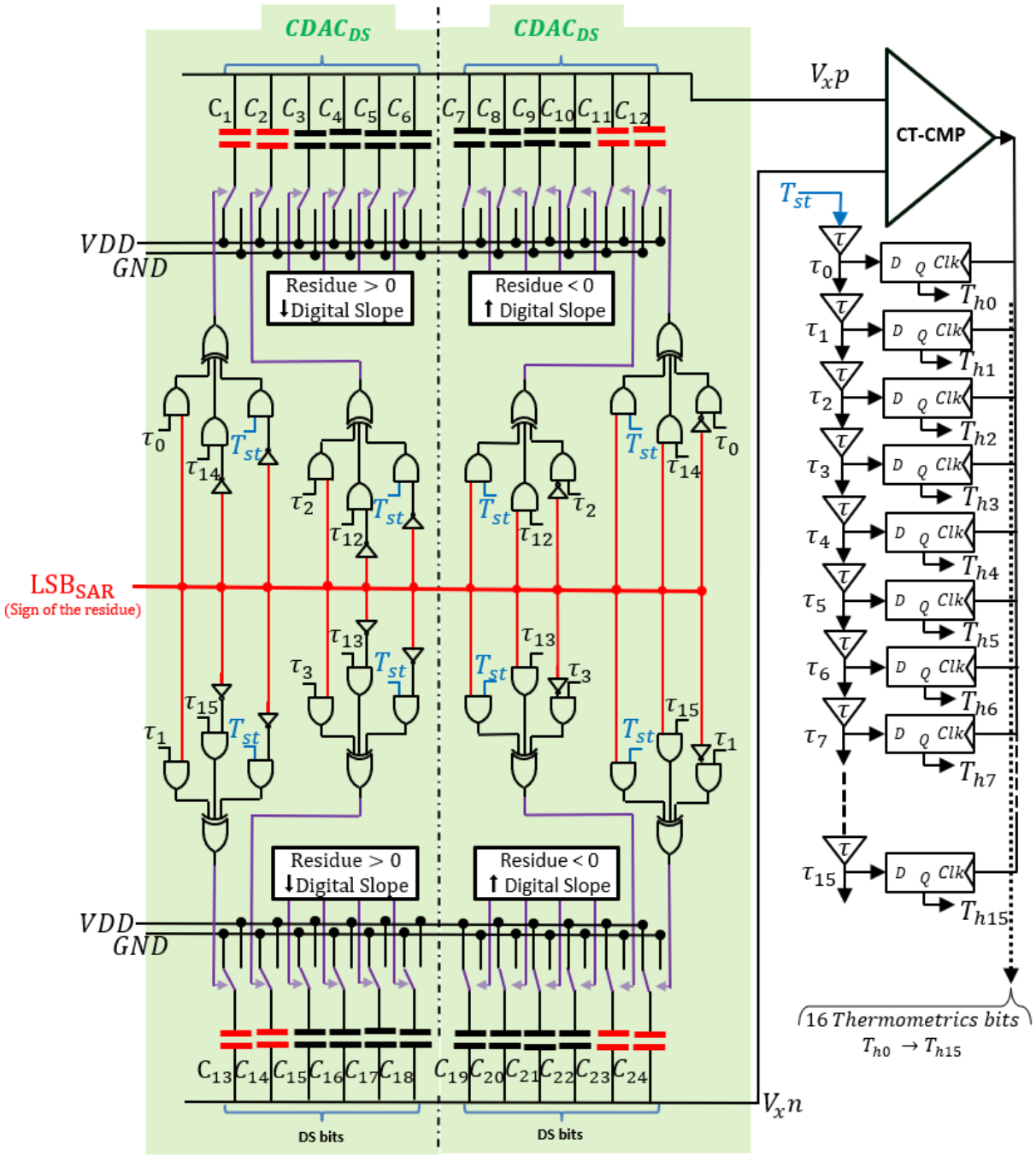

Figure 56 - 2nd stage: 3 bits Digital slope + 1 bit redundancy

This pseudo differential implementation speeds up the overall conversion while reducing the number of capacitances used for redundancy (6 instead of 8). Bidirectional slopes are generated without reducing the size of unit capacitors thanks to the alternate switching scheme. Furthermore, the common mode variation for the comparator switching point is limited to one overall LSB voltage step.

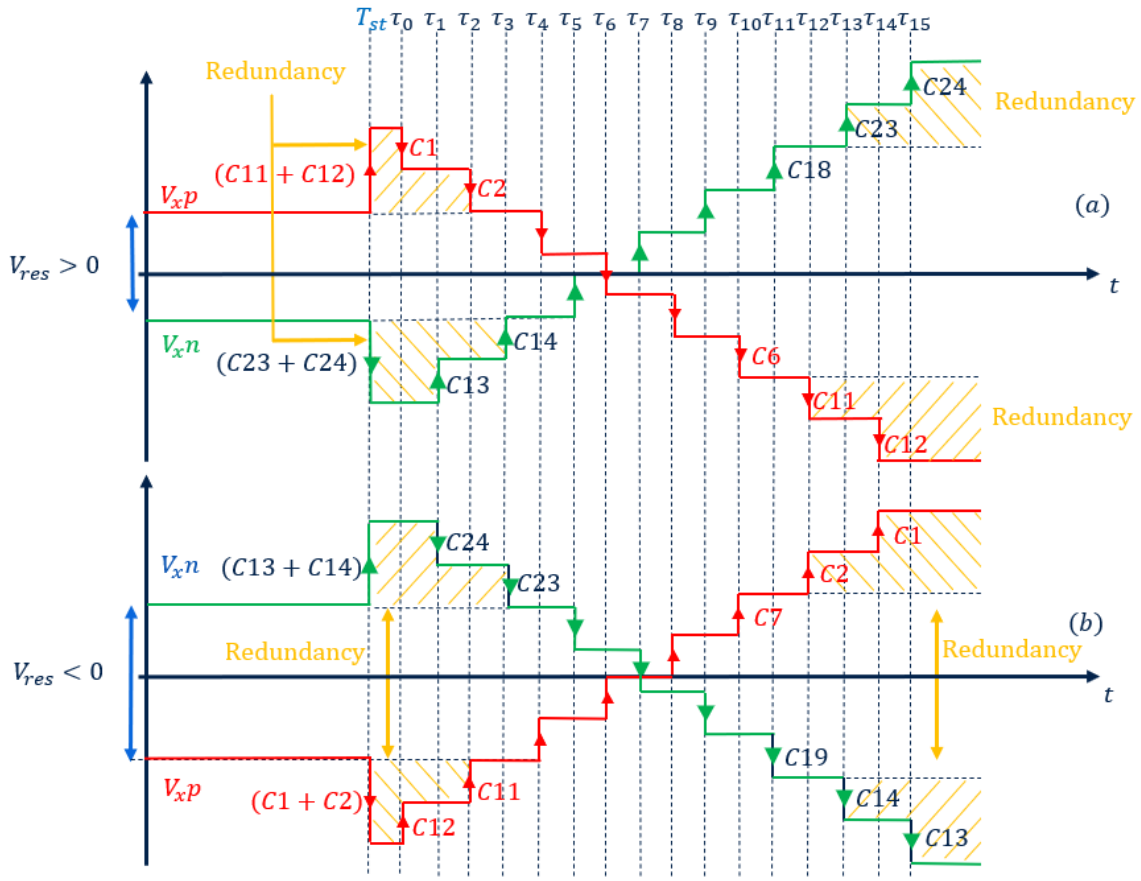

Figure 57 - 3 bit pseudo differential Digital Slope with redundancy (a) for positive residue (b) for negative residue

The delay line used in the second stage is sized with 50ps of unit delay as in [3]. This value has been demonstrated feasible and allows a short time for second stage conversion. The targeted 18nm technology could probably realize shorter unit delays but this aspect has not been pushed yet. Nevertheless, shorter delays induce faster ramps and thus a bigger impact of the latency on the codes. With 50ps of unit delay the time required for the 4 bit of the second stage represents 800ps. To overcome the latency difficulties, the size of the delay line has been doubled as 32 delays have been implemented. As discussed, only 16 delays are connected to capacitance. The extra delays need only to compensate the static latency. Furthermore, doubling the size of the delay line looked a reasonable trade-off.

This section presented the overall analysis and principles of the proposed architecture and derived the sizing of the various elements to meet the requirements. To validate the global performances, the next section presents a VerilogA model implementation of the presented architecture with the sizing of the elements derived in this section.

3.3 VerilogA model

3.3.1 Description of the VerilogA model

To validate the analysis and the performances of the proposed structure, a VerilogA implementation of the whole ADC has been developed. This step in the work is intended to be used as a working predesign, aimed to settle the test bench before transistor design. In the industrial development process, once the overall performances validated, blocks of the model will later be replaced by their transistor level descriptions. This iterative method ensures efficient development of the proposed ADC and an accurate way to study block- level impact on the global architecture. The Verilog A model of the core elements has been developed with functional granularity:

- Supply voltage is generated by perfect voltage sources.
- The CDAC is modeled as represented in Figure 54 with ideal switches. Additional capacitors are added in parallel to each capacitor of the CDAC to represent capacitance variations dues to mismatch. A random draw is modeled with standard deviation of 1.25% on unit elements. Only 1 draw is implemented and simulated. This limits the analysis of the mismatch performances and would require better tools than those used to model the architecture.
- Comparators are modeled as depicted in Figure 41 plus an intrinsic latency. An ideal comparator with programmable latency is described in VerilogA and offset and noise is modeled as series elements at the input. The “cross” function of VerilogA is used as event trigger for the comparator. For the D-CMP, the cross function is triggered by the clock input. For the CT-CMP, the cross function is triggered by a crossing voltage of the inputs. Noise and offset are modeled at the input of both comparators.
- The delay line is modeled with perfect delay units of 50ps.
- Both algorithms are described with state machines described in VerilogA, driving CDAC switches, starting the delay line and reading comparators output.
- A 3rd state machine controls the calibration phase. This digital section of the ADC is controlled by external signals selecting conversion mode or calibration mode and which calibration mode must be done. The desired calibration can also be chosen among measurement of the D-CMP offset, measurement of the CT-CMP offset and measurement of the CT-CMP delay. The averaging is also done outside of the ADC, a TOP digital circuit is required to launch for example D-CMP offset measurements several times and average the results.
- Noises sources are modeled by a custom Verilog block used as random voltage generators mounted in series. They are described in VerilogA. To use these blocks in series, they must

present a voltage between each node. This behavior is difficult to implement in VerilogA and makes the simulation slow, so they are described as voltage follower. The block is described to copy its input voltage value on its output voltage node, which is equivalent to a null voltage between input and output. To make the noise function, a random value is computed by the block within a standard deviation sized coherently with the system description then added to the output voltage. The random number distribution is gaussian and standard deviation is parametrized to reuse the same block for the different noise sources. To alleviate the simulation complexity, the noise generator does not add noise continuously which would explode the transient simulation. Because the system is discrete, the noise generator is driven by perfect clock events. These clock events are not required in the final implementation, they are only used for modeling. They allow to add noise before voltage evaluation by the discrete system or after sampling. Noise is reevaluated for each voltage comparison and every sample in conversion and calibration mode.

- Comparator offsets are modeled with perfect voltage generators in series with one of the inputs of each comparator.
- The state machine driving the SAR algorithm also controls the digital slope start. Once the last bit in the SAR algorithm is evaluated, the state machine gets the information, and the SAR operations stop. The voltage generated by $CDAC_{Calib}$ switches from D-CMP to CT-CMP offset, the state machine changes the digital word to convert from D-CMP offset to CT-CMP offset after an analog delay of 10 ps. Meanwhile a startup signal is sent to the CT-CMP to switch it on, 0.7 ns is then spent to ensure the good start of the comparator and then the ramps start.

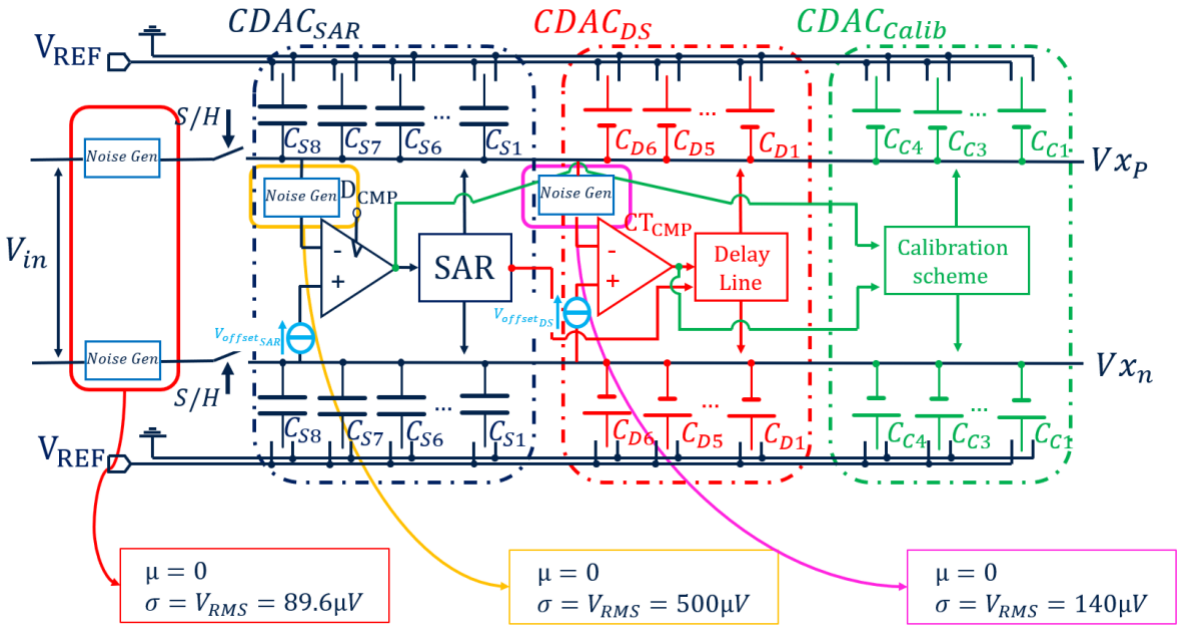

Figure 58 - Representation of VerilogA model of the SAR-Assisted Two stages differential DS block schematic including noise, offset and calibration

A schematic representation of the VerilogA implementation based on Figure 52 is given in Figure 58. The different blocks modeled are represented with their connections. The values used in noise generators are also described in the schematic representation. It must be underlined that noise contributions of the switches in the CDAC have not been take into account in the VerilogA model. The analysis of the noise balance including CDAC noise (3.15) suggests that this noise contribution does not impact significantly the ADC performance. Simulations have been done with and without parasitic capacitance implemented in the model to confirm the impact described in (3.16). These parasitic capacitances have been implemented with dedicated parallel capacitances in the modelled cell view with an order of magnitude of hundreds of aF for the split MSB capacitor used in the SAR.

3.3.2 Testbench and simulation results

With the previously described model, a two-step simulation process has been set up to analyze the performances of the architecture. The test bench used for simulation is detailed in Figure 59. Two digital blocks interfacing with the ADC allows calibration phase and bit recombination, they are modeled in VerilogA. The first digital block controls the calibration phase of the ADC. The second block recombines the outputs produced by the SAR and DS including the errror correction with the redundant bits to provide the expected 12 bit output at the end of the conversion.

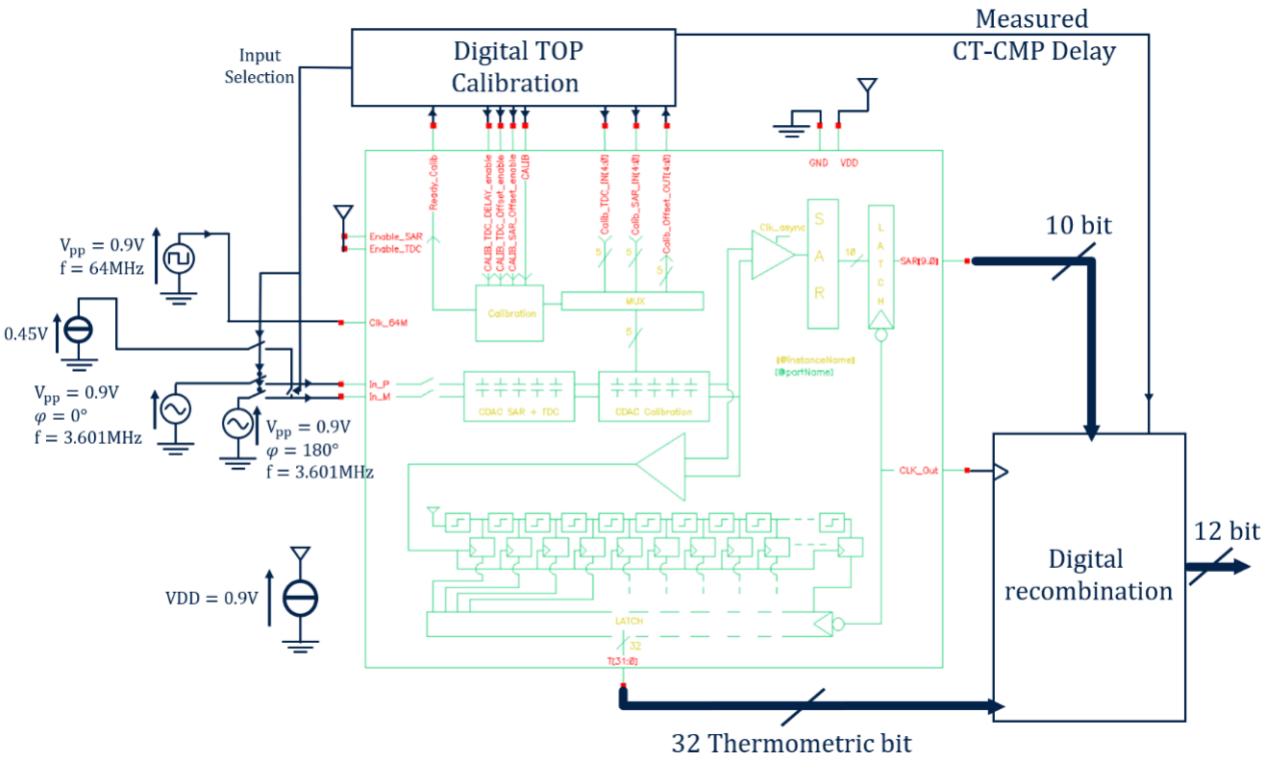

Figure 59 - Cadence VerilogA model cellview with block representation of the test bench simulated in Spectre

The first phase of the simulation represents the foreground calibration, the input voltages are thus set to the common mode voltage before shifting for the wanted input to convert. Sequentially offset measurements are repeated 100 times (for each comparator) with constant input (the number is a parameter in the "Digital Top Calibration" block). Comparators offsets are then stored in the digital calibration block and transmitted to the appropriate inputs of the ADC model. After the offset measurement, the CT-CMP latency is measured in foreground calibration also with 100 repetitions before being transmitted to the recombination block. Different values of delay have been simulated within the range of 16 extra unit delays added to the delay line.

Once the foreground measurements are done, the input is switched to a sinusoidal voltage generator providing a signal coherent with the ADC full scale. 8192 samples are converted conversions are done. 8192 conversions are chosen to present good frequency resolution in the following spectrum plot. The input sinus frequency is chosen to guarantee every code measurement according to the following formula:

$$\frac{N_{points}}{N_{prime}} = \frac{F_s}{F_{in}} \tag{3.27}$$

N_{points} represents the number of wanted points for the simulation (8192), N_{prime} is a prime number, F_s is the sampling frequency and F_{in} is the frequency to present at the input. With a prime number of 461, a sampling frequency of 64MS/s and a wanted number of points of 8192, the input frequency to guarantee accurate conversion of the sinus through the whole dynamic is 3.601MHz. This setup allows to avoid power leakage in the spectrum plot.

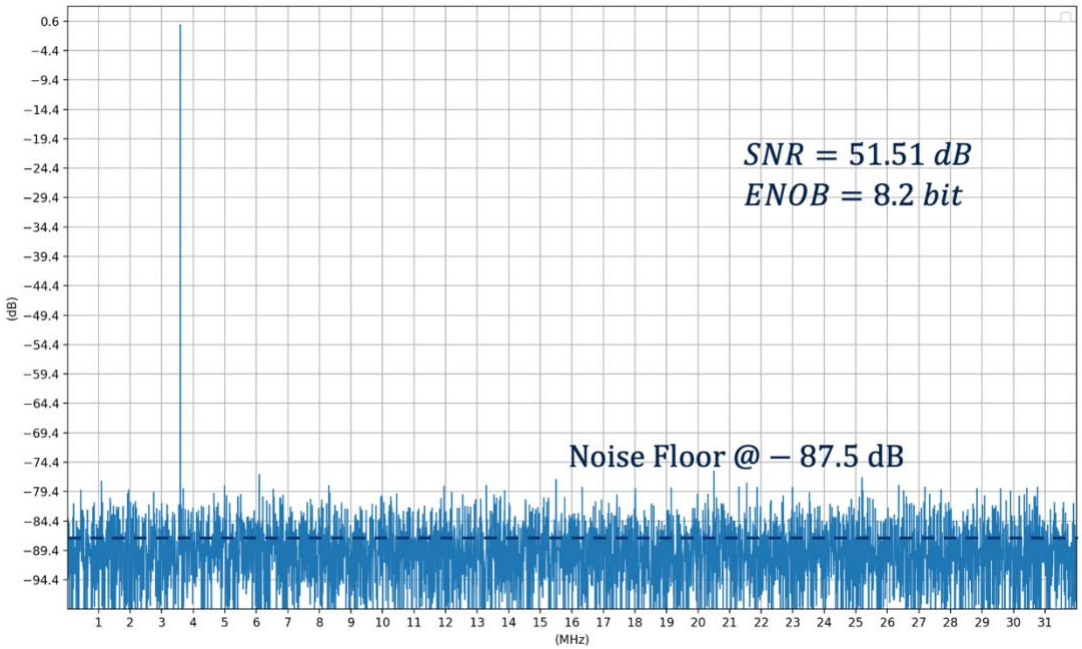

Figure 60 - Simulated 8192 points FFT of the proposed ADC with noise, offset models – Calibration OFF.

To underline the architecture sensitivity to a difference of offset between the two comparators, the simulations resulting FFT plots presented in Figure 60 and Figure 61 are run with 10mv of offset difference. The dynamic comparator of the SAR is simulated with -7mV of offset while the CT-CMP of the second stage presents 3mV of offset. In this scenario the calibration is once turned off and results are plotted with the FFT presented in Figure 60. Then the calibration is turned on and the FFT results are plotted on Figure 61. Without calibration the average noise floor is at -87.5 dB with respect to full scale presenting a SNR of 51.51 dB for an ENOB of 8.2 bits. This level of performance corresponds roughly to the one that can be expected from the 9-bit SAR, the second stage does not provide any improvement. With calibration turned on, the noise floor level is reduced by 16.5 dB and simulated SNR and SNDR are respectively 67.91 dB and 67.12 dB with respect to full scale and spurious signals coming from nonlinearities and saturation effects added. The above-mentioned added capacitance to the CDAC used to model the variability and the distortion induced are only simulated in the plot FFT plot presented in Figure 61 with the calibration turned on. The resulting SNR is equal to the targeted value confirming the method used in the models. A third harmonic is visible on Figure 61 due to the mismatch of the capacitances added in the modeled CDAC. This nonlinear behavior induces THD but still in the targeted performances. To have an exhaustive representation of the mismatch impact, a Monte Carlo simulation is required but it would be very time-consuming simulation to realize due to the important amount of data.

With the presented model, the analysis of the proposed structure has been verified. The simulated SNR shows that only noises considered impact the overall performances. The noise of the SAR is not present on the measurement and even with noise and offsets, the bidirectional digital slope converts and

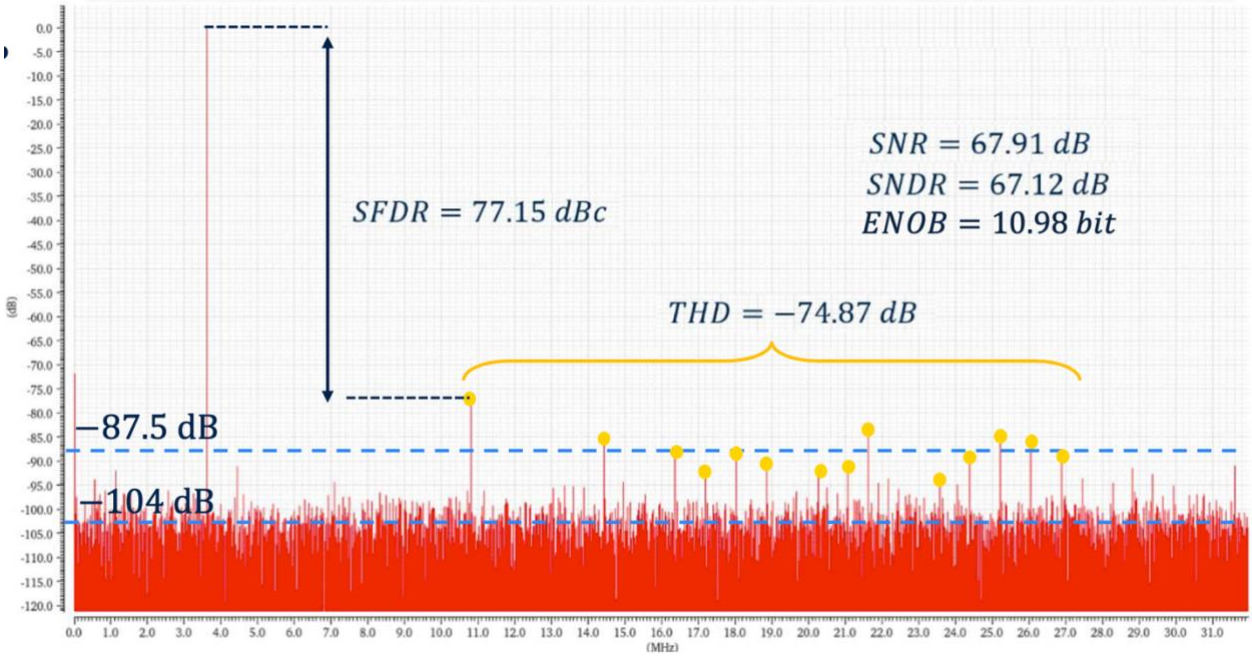

Figure 61 - Simulated 8192 points FFT of the proposed ADC with noise, offset models and mismatch (1 draw) *Calibration ON*.

corrects the residue without missing codes. The correction schemes implemented as redundancy and calibration allows then to realize a functional bidirectional digital slope.

3.3.3 Power consumption estimation

To compare the proposed ADC to others realization, the key parameter is power consumption. Because the VerilogA model presented above cannot provide any information on power consumption, the power consumption of the proposed architecture has been modeled by extrapolating experimental data of a similar circuit published by Liu [3]. Figure 62 shows the power consumption breakdown of the circuit in [3].

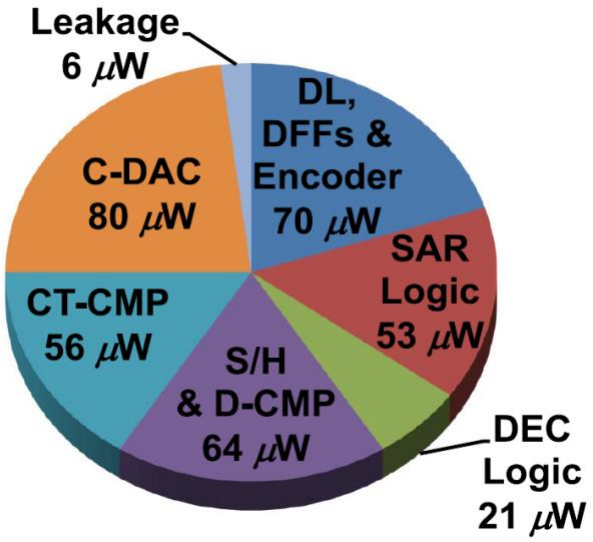

Figure 62 - Power consumption breakdown measurements from *[3]*

To compare with DS architectures identified in the previous chapter, Table 9 summarizes the simulated performances of the described model and the corresponding performances in the state of the art.

To achieve a similar breakdown of the power consumption for the propose ADC architecture, the power consumption reported in [2] has been scaled for each block by taking into account the implementation differences and appropriate error margins.

- The power consumption linked to the CDAC scales with the power supply, total capacitance and sampling rate. The scaling is therefore given by the following expression, including a 30% error margin :

$$P'_{CDAC} = P_{CDAC} * \frac{64}{100} * \frac{0.615}{0.9} * 1.3 = 45.5\mu W \quad (3.28)$$

Where $P_{CDAC}{}'$ is the power consumption of the proposed architecture and P_{CDAC} the power consumption reported for the circuit in [2].

- The section "$DL, DFFs$ & $encoder$" represents the delay line with its latching circuitry. The power consumption scales with the supply voltage, the number of stages in the delay line and the sample frequency. The scaled power consumption is given by:

$$P'_{DL} = P_{DL} * \frac{64}{100} * \frac{16}{64} * 1.3 = 14.6\mu W \tag{3.29}$$

Where the factor (16/64) is ratio of delay cells in the delay line.

- The SAR logic used to drive SAR algorithm scales with the number steps in the algorithm and the sampling rate:

$$P'_{SAR_{logic}} = P_{SAR_{logic}} * \frac{64}{100} * \frac{10}{8} * 1.3 = 55.2\mu W \tag{3.30}$$

- The logic used for bit decoding represented as "Digital Recombination" in Figure 59 scales also with the sample rate. In absence of details on its structure the extrapolation cannot be more precise. The estimated value is given by:

$$P'_{DEC_{logic}} = P_{DEC_{logic}} * \frac{64}{100} * 1.3 = 17.5\mu W \tag{3.31}$$

- The power consumption of the sample and hold circuit and the D-CMP are given together in Figure 62. It is difficult to precisely extrapolate the consumption from the aggregate date. The power consumption of the sample & hold varies with the sampling rate and the total capacitance of the CDAC, while the power consumption of the D-CMP depends on noise requirements and bandwidth requirements and the number of steps in the algorithm. The proposed approximation takes into account the reduced sample rate and the increase in the number of steps:

$$P'_{S\&H:SAR} = P_{S\&H:SAR} * \frac{64}{100} * \frac{10}{8} * 1.3 = 45.5\mu W \tag{3.32}$$

- The continuous time comparator of both architecture is targeted with same input referred noise as described in [3]. On the other hand, the on-time of the comparator is divided by four due to the shorter delay line. The consumption also scales with the sample rate. The resulting estimate is :

$$P'_{CT_{CMP}} = P_{CT_{CMP}} * \frac{64}{100} * \frac{16}{64} * 1.3 = 12\mu W \tag{3.33}$$

- The leakage does not scale with any parameter. With leakages considered equal and with margin, the equivalent power consumed increases:

$$P'_{leakage} = P_{leakage} * 1.3 = 7.808\mu W \quad (3.34)$$

With the previous proposed sizing a global consumption scaled on [3] is calculated with a 30% margin. The extrapolated power consumption breakdown is presented in Figure 63 for a total estimated power consumption of $200\mu W$.

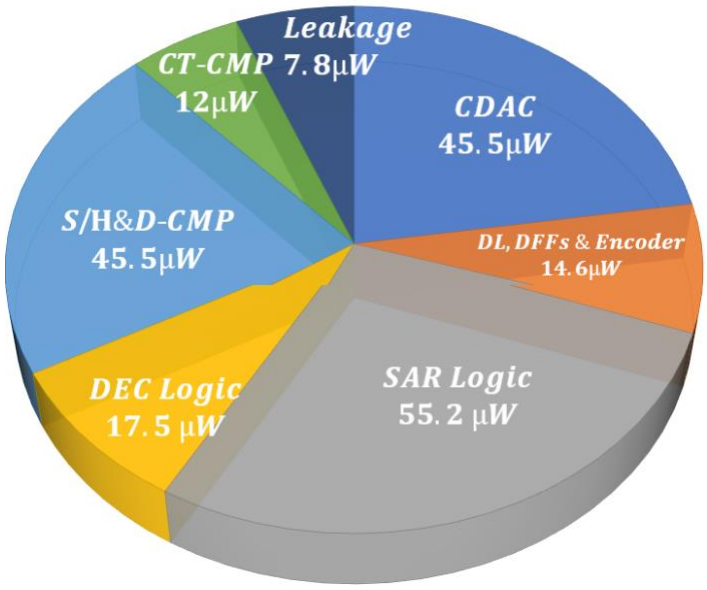

Figure 63 - Extrapolated power consumption breakdown for SAR assisted bidirectional ADC from *[3]* measurements.

3.3.4 Comparison with State of the Art

Once the system proven robust with VerilogA model and power consumption estimated with a reasonable margin. The proposed SAR 2 step assisted bidirectional digital slope can be compared to the state of the art for a first overview of its relevance. Figure 64 draws from previous state of the art chapter the position of the proposed architecture in regards of ADC explored in chapter 2.

With 67.1 dB SNDR and 203µW of power consumption under 64MS/s, the proposed ADC develops a Schreier figure of merit of 179.1 dB. Which compares favorably compared to state of the art. Table 9 shows the positioning of the proposed ADC with respect to similar ADCs based on the data from Boris Murmann.

Table 9 - Summarize of simulated model performance compared to state of the art

	This Model	VTC [69]	Monotonic [3] DS
Techno	**18nm (target)**	65nm	28nm
Year	**2022**	2019	2016
Resolution [bits]	**12**	13	12
Sample rate [MS/s]	**64**	20	100
SNDR [dB]	**67.12***	71.5	65.67
Csample [pF]	**0.615**	4	0.9
Noise CT-CMP [μV_{RMS}]	**157**	45.6	150
Consumption [µW]	**204****	82	350
2nd stage common mode variation	**± 0.5 LSB**	--	$\geq -64LSB$
$FOM_{Schreier}$ [dB]	**179.1****	182.4	177.2

* Simulated with noise, offset and mismatch models
** Extrapolated from Monotonic DS measurements

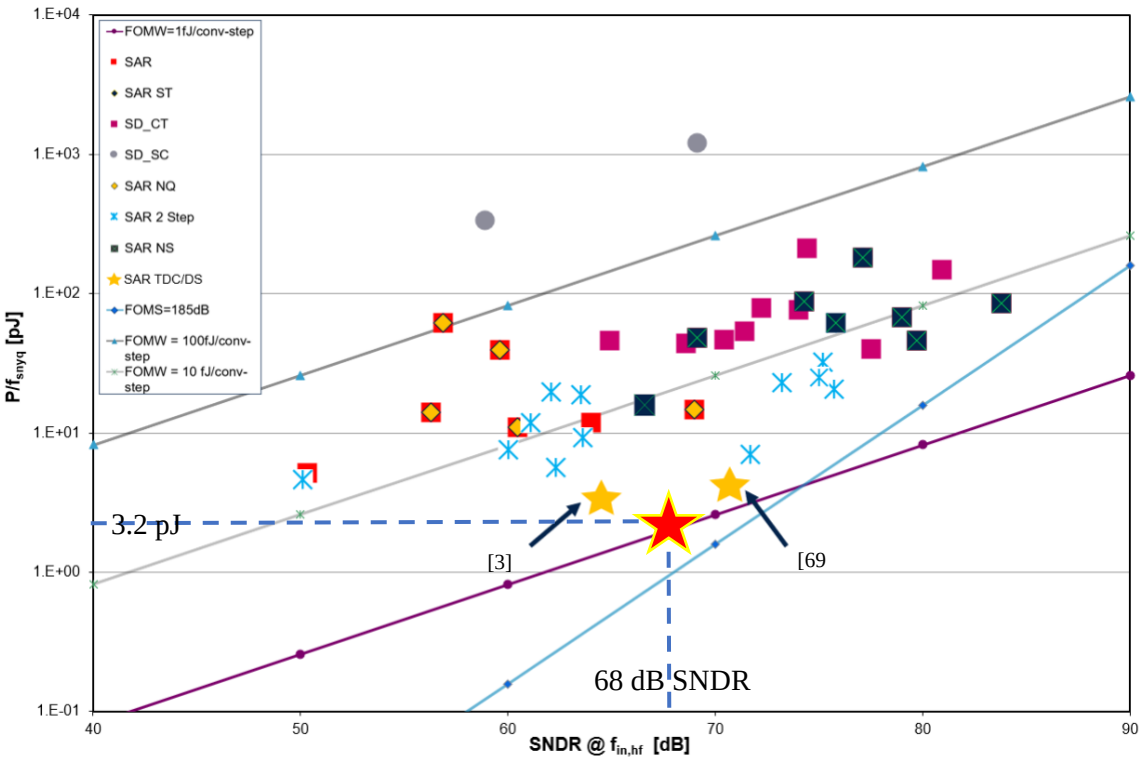

Figure 64 - From figure 2.17 – From B.Murmann survey, energy efficiency depending on resolution for realizations close to the target including proposed work placed with extrapolated power consumption performances

3.4 Conclusion

This chapter introduces the bidirectional digital slope converter and details the main characteristics and advantages of its use as fine converter in a SAR assisted ADC. The challenges are also described with proposals for the calibration algorithms. A complete methodology for the sizing of the overall ADC is derived. A detailed behavioral model based on the analysis of the structure is proposed and simulated to confirm expected results.

In order to compare the proposed ADC with State of the Art realizations, a power consumption extrapolation from a published silicon chip with similar architecture is proposed. Scaling of the performance is detailed with an important margin of 30%. The extrapolated results place the proposed ADC as a relevant architecture for the target performances with Schreier FOM very close to the best reported ADCs with similar specifications.

The fine converter is the key component of the architecture as discussed in this chapter. The second stage must correct errors made by the first one while maintaining good overall performances. The continuous time comparator being the most critical block as its noise is directly added to the signal. The

timing of this block is also critical, in particular the extra time consumed for correct startup during each conversion cycle.

The next chapter presents the design of the continuous time comparator targeted for the presented ADC in 18nm CMOS FD-SOI technology.

Chapter 4

2nd stage comparator design

4.1. 2ND STAGE CT-CMP DESIGN 107

4.1.1 STATE OF THE ART OF CONTINUOUS TIME COMPARATOR 107

4.1.2 DESIGN SPECIFICATION OF THE CT-CMP IN BIDIRECTIONAL DS ARCHITECTURE. 109

4.1.3 CT-CMP, 2 STAGE AMPLIFIERS DESIGN IN 18NM TECHNOLOGY 110

4.2 NON LINEARITY BEHAVIOR DUE TO BANDWIDTH RESTRICTION 113

4.3 FOLDED CASCODE CT-CMP 115

4.4 BIAS AND START-UP STAGE 117

4.5 LAYOUT AND PLS RESULTS 121

4.6 CONCLUSION 125

4.1 2nd stage CT-CMP design

Previous chapters underlined the key impact of the second stage on the overall ADC performances (noise and power consumption). The CT-CMP is a major part of the second stage impact as its noise is directly added to the converted signal and the power consumption of the stage is proportional to the time spent with the comparator on. The comparator must be switched on at the end of the SAR process and switched off at the end of the second stage conversion. The targeted performances are 154µV RMS of input referred noise and 234µW of instantaneous power consumption. This section details state of the art continuous comparator and the proposed design in 18nm CMOS FD-SOI technology.

4.1.1 State of the art of continuous time comparator

The main reference of this work [3] describes its proposition of continuous time comparator as low power compared to dynamic comparator. The proposed CT-CMP presents a low bandwidth to filter the ramp steps which allows interpolation by linearizing the digital slope into a ramp. This increases the second stage resolution proposed in [3] by 1 bit.

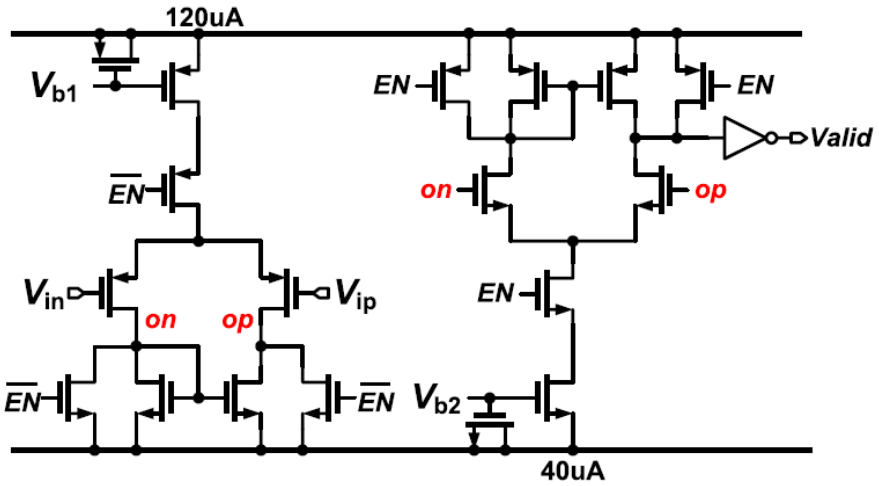

Figure 65 – From *[3]*, schematic of low noise low power CT-CMP

Depicted in Figure 65, the CT-CMP proposed by Liu & al. in [3] is composed of two amplifier stages followed by a latch. Both stages present a differential pair with a common current source, however the first stage output is differential and feeds the second stage input. The second stage output is single and connected to an inverter stage. Because the sign of the ramp is known thanks to the voltage shift done before starting the ramp [3] the initial state of the inverter is also predictable. The p-type differential input

pair matches with the common mode voltage of around 100mV [70]. The comparator is designed to have high open loop gain and low bandwidth compared to the digital slope step frequency. In Liu's [3] design the digital slope has a step every 100ps (10GHz rate) and the CT-CMP is designed with 100 MHz -3dB frequency which is 100 times lower than the voltage step rate. The comparator acts as low pass filter with respect to the digital slope. This is amis to suppress signal dependent effects, to linearize the steps and so to increase the resolution by interpolation. 1 bit step interpolation is used as the delay line has a 50ps time-step resolution.

The comparator drawn in Figure 65 has an average power consumption of 56µW seen through the conversion period as drawn in Figure 62 of Chapter 3, with the first stage using 120µA and the second stage 40µA of current. From this instantaneous power consumption and the power through the conversion period, we can estimate the mean time with the comparator on at 3.9ns. The delay line being composed of 32 elements, it makes a maximum theoretical time of 3.2 ns and so an average time of 1.6ns. The extra time spent by the comparator can be explained by the delay compensation with extra delays mentioned in the reference but not quantified.

The concept of two cascaded amplifier stages in the comparator design is proposed to reach high gain despite difficulty to reach high bandwidth performance. As represented on Figure 66, with two amplifiers stages described with gain (G_1 and G_2) and input referred noise (IRN_1 and IRN_2), the overall gain of the chain is product of both unitary gain and the overall IRN is mainly represented with the first amplifier stage noise. As described in signal theory with Friss formula, the second stage noise is reduced by the first amplifier gain. A systematic offset is nevertheless inherent in this structure because of the threshold voltage of the digital block at the 2nd amplifier output. The voltage presented at the input of the inverter at the node denoted V_s on Figure 66 when the input is crossing is not correlated with the voltage

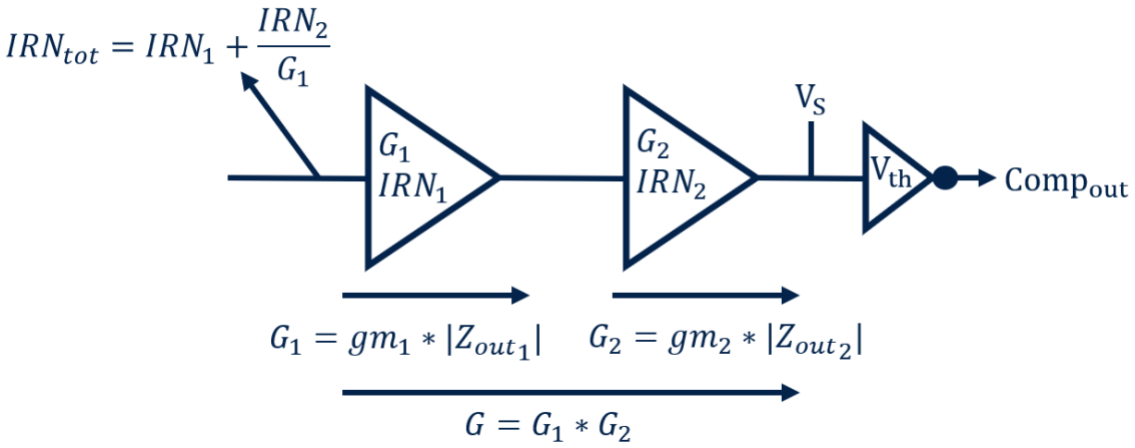

Figure 66 – Block representation of two stages amplifier followed by an inverter cell

threshold of the inverter stage. This induces an offset which varies with temperature and process. This offset seen by the input is reduced by the gain of the amplifiers. In the structure presented in [3] the gain of each stage is equal to the product of differential pair transconductance and real output impedance. The current flow in Figure 65 described for the first stage is meant to reduce noise impact on the input. As discussed before, the second stage noise requirement is relaxed by the first stage gain. The comparator bandwidth in [3] decreases with high output impedance composed of transistor's equivalent output resistance and the load capacitance. Other parameters such as parasitic capacitance and wire resistance also present an impact quantifiable after layout realization which contributes to the decrease of the bandwidth. The trade-off to reach high gain and low bandwidth in this structure is thus interesting. This simple structure of cascaded amplifiers followed by a latch ensures the wanted behavior with a favorable tradeoff.

4.1.2 Design Specification of the CT-CMP in bidirectional DS architecture.

The technology node targeted for this work is 18nm FD-SOI CMOS. The first specifications inherent of the SOC and technological targets is the voltage supply fixed to 0.9V.

In the proposed CT-CMP the bandwidth has been sized accordingly with the extra delays added in the delay line to compensate extra latency. A bandwidth greater than 195MHz must present short enough latency to be fully quantized by the extra delays discussed in chapter 3.

Table 10 resumes the design specification for the proposed CT-CMP.

Table 10 - Performances specification of the proposed CT-CMP

	Targeted for this work	From [3]
Parameter	**Value**	
Voltage Supply [V]	0.9	0.9
Power consumption [µW]	< 234	160
Input referred noise [µW]	< 154	150
Bandwidth [MHz]	> 195	100

4.1.3 CT-CMP, 2 stage amplifiers design in 18nm technology

A first approach from the literature examples in [3] and [73] is based on two differential amplifiers stages with a single-ended output connected to an inverter stage. Figure 67 draws the first design of CT-CMP amplifier stages proposed in this work. Based on the structure in Figure 65, this design is intended to reach performances close to the one described in [3].

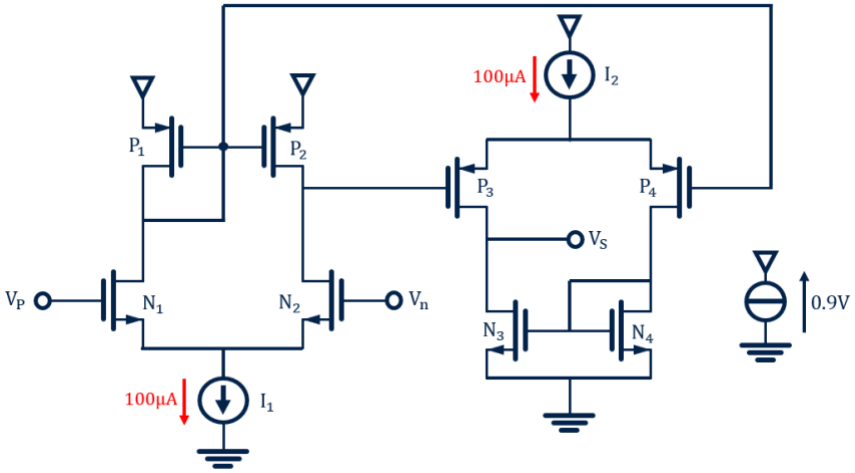

Figure 67 - Design of 2 stages amplifier CT-CMP based on *[3]* and *[73]*

For homogeneity in the SOC the first design has been made only with regular well transistors, planned to be the majority of the transistors used in the analog RF chain because of the density. Indeed, flip well transistors require dedicated boxes with unused space between them which degrades the area efficiency of the circuit.

With transistors sized as described in Table 11, the transfer function drawn in Figure 68 is obtained.

The differential gain by stage in this amplifier is equal to:

$$A_d = \frac{gm}{gd} \tag{4.1}$$

With gm the transconductance of transistors present in the differential pair and gd the output conductance present on the output. The gain in the comparator shown in Figure 67 is:

$$A_d = \frac{gm}{gd_{P2} + gd_{N2}} * \frac{gm'}{gd_{P3} + gd_{N3}} \tag{4.2}$$

With gm transconductance of the first stage and gm' transconductance of the second stage.

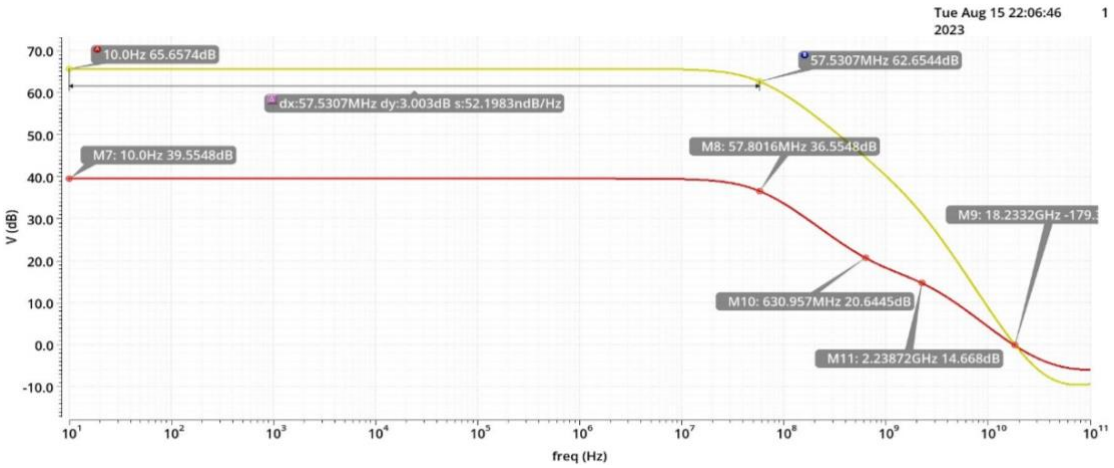

Figure 68 - Transfer function of the 2-stage amplifier CT-CMP schematic (first stage transfer function - red / second stage transfer function - yellow) – no offset correction

The gain in each stage described with (4.1) and the overall gain (4.2) corresponds to the transfer function drawn in Figure 68. To obtain high gain the transistors are sized to have high transconductance as seen in Table 11. The input pair of each stage is sized with important width, the length value is also greater than minimum allowed by the technology to reduce mismatch. The load transistors used in current mirror (P_1, P_2, N_3, N_4) are sized with smaller $\left(\frac{W}{L}\right)$ to increase output load without extra capacitance. The bandwidth of this structure is dominated by the first pole of each amplifier stage proportional to the sum of the conductance of load and gain transistor divided by the load capacitance. The load capacitance is mainly the inverter stage output circuit then the parasitic capacitances of load and transconductance transistors. The trade-off to reach high gain and high bandwidth is thus difficult with this topology because wider transistors bring more gain but also more parasitic capacitance.

Table 11 - Transistors sizing of CT-CMP 2 stage amplifier

Name	Width	Length	Type
N1	7.9µ	90n	Regular Well
N2	7.9µ	90n	Regular Well
N3	800n	18n	Regular Well
N4	800n	18n	Regular Well
P1	2.9µ	90n	Regular Well
P2	2.9µ	90n	Regular Well
P3	6.8µ	70n	Regular Well
P4	6.8µ	70n	Regular Well

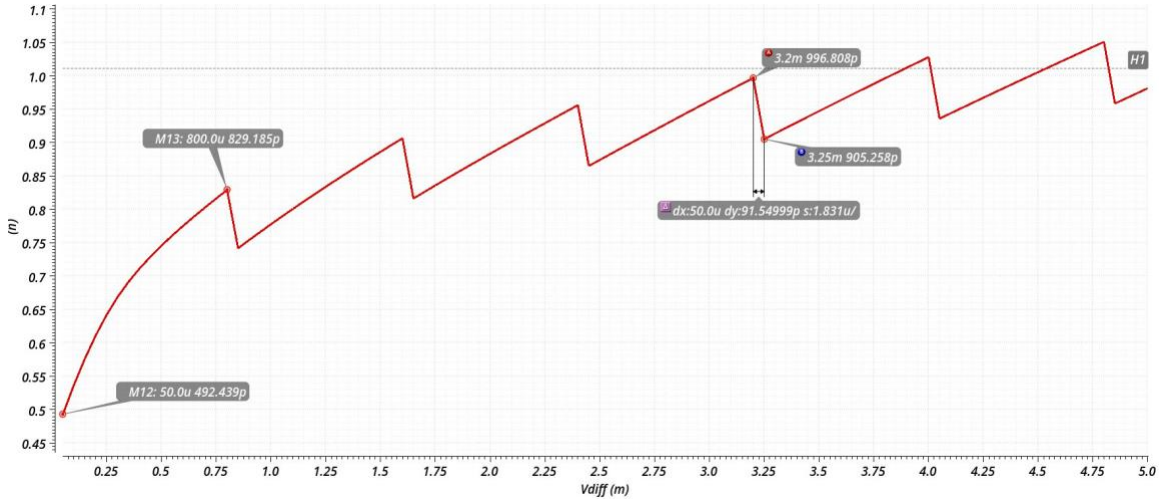

Figure 69 – Simulated delay on the output caused by the CT-CMP (time compared between input cross and output rising edge)

This first design reaches more than 65dB open loop gain and 57MHz -3dB bandwidth. These performances are coherent with chosen topology but with the first simulations a non-linearity caused by the low bandwidth appeared non negligeable. The designed comparator in 18 nm technology has been introduced in the VerilogA model of the global ADC to validate behavior of the overall conversion. Without switch on and switch off consideration, the on time of the comparator presented an important value unable to match low power considerations aimed for this work. Moreover, the expected latency presented nonlinear behavior dependent of the input voltage. Figure 69 shows a simulation result of the extra latency of the comparator in function of its input. The latency is defined as the time spent between the input voltage crossing and the output rising edge. This time is thus added to the time representing the input value. The simulation is presented for a positive polarity residue with initial input voltage represented as Vdiff in Figure 69. The time is reference to input voltage cross showing only the effective comparator delay. This simulated latency was not constant as expected but input dependent and larger than the correctable value of the latency. Compensate a large latency means to let the comparator on during a long time and lose low power benefits and time gain brought by the bidirectional approach. The digital output code gets saturated by this extra latency in conversion situation. The second stage wasn't able to convert SAR residue.

The next subsections described the analysis of this phenomena correlated to the bandwidth with matlab models.

4.2 Non linearity behavior due to bandwidth restriction

In a first-order approach, the CT-CMP with a structure such as described in the previous section based on cascaded amplifiers can be modeled as a gain followed by a low pass filter and the output inverter. With this model shown on Figure 70 (a) the operation of the DS stage can be analyzed in detail.

The input of the comparator is a differential voltage ramp. For the sake of simplicity it is represented as single ramp in Figure 70 representing the differential voltage at the input of the comparator. The input ramp is composed of steps with a period Δt. With regard to the equivalent bandwidth of the comparator, those steps can be considered linearized as mentionned in references [3].

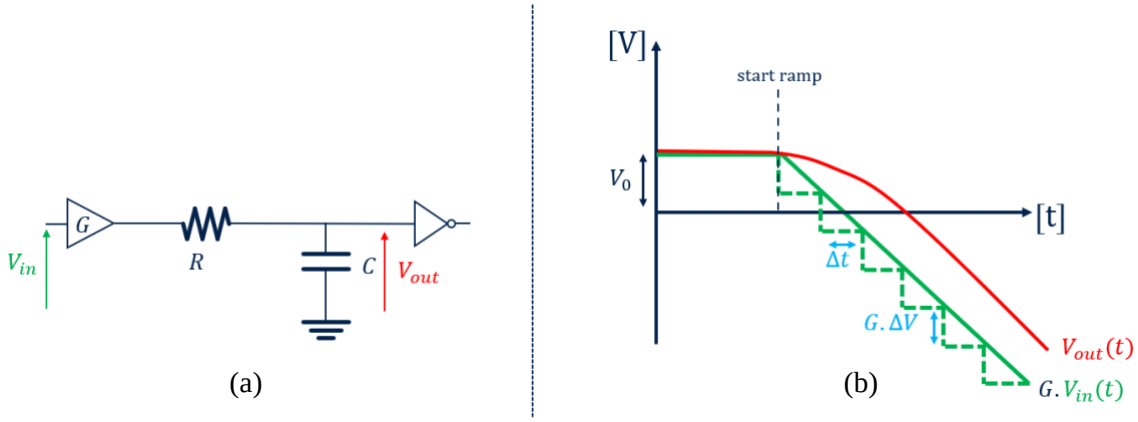

Figure 70 - (a) First order model of the CT-CMP - (b) Time domain response of the comparator for an input voltage ramp

The time domain response of a first order low pass filter to a ramp is firstly a transient behavior following exponential description. Then the output is a steady linear voltage ramp corresponding to the input delayed by the time constant of the filter. The transient behavior shown in Figure 70 (b) corresponds to the phenomena observed on Figure 69. By linearizing the system with Laplace, the voltage output of the system can be described as:

$$V_{out}(t) = V_0 - \alpha\left(t - \frac{1 - e^{-\omega_{-3dB}.t}}{\omega_{-3dB}}\right) \tag{4.3}$$

With α the ramp coefficient, ω_{-3dB} the bandwidth of the low pass filter equivalent, and V_0 the starting voltage for the ramp. Nevertheless this model is a linear approximation of the comparator behavior. To be more accurate a Matlab model of the time response to the actual voltage steps has been implemented to validate the behavior depicted on Figure 69.

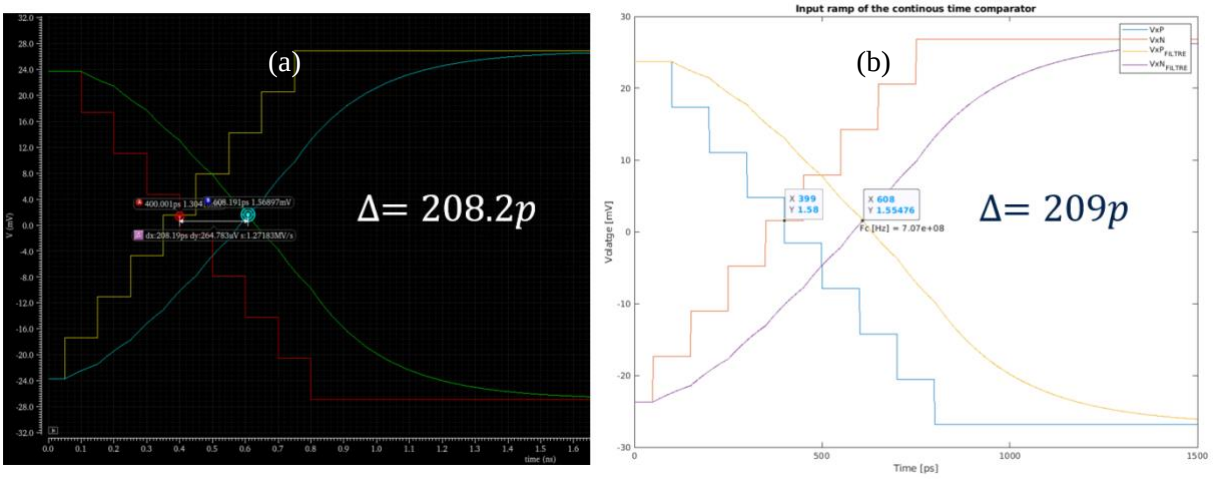

Figure 71 – Cadence (a) and Matlab (b) simulation of first order model CT-CMP

Figure 71 shows the results of 2 different descriptions of the model drawn on Figure 70 (represented as differential signals in Figure 71). In Cadence the model is described electrically, in Matlab, the model is described with differential equation of the successive steps. The time between the input cross voltage and the output cross voltage (corresponding to the output of the comparator) is the extra latency of the system, it is given as Δ in Figure 71. Figure 71 shows simulated transient responses for both models and validates that the theoretical description (Figure 71 (b)) follows the electrical behavior (Figure 71 (a)). By parametrizing the Matlab simulations, an important number of bandwidth spanning the whole input dynamic can be simulated.

Figure 72 draws the extra latency (Δ in Figure 71) depending of the input voltage for several CT-CMP bandwidth values. The wanted behavior with a constant latency as previously discussed in chapter

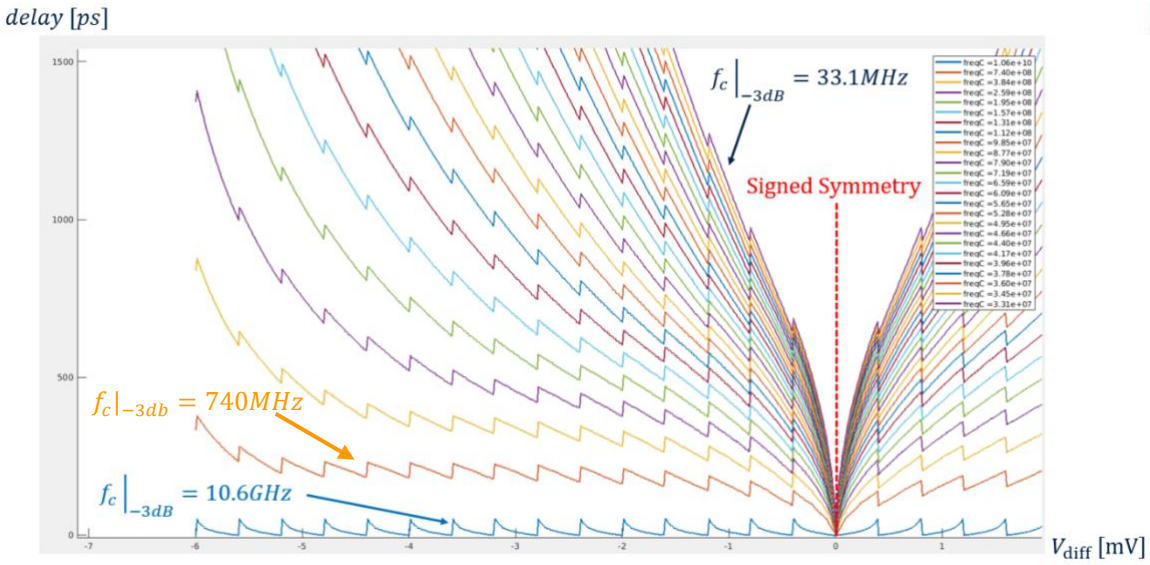

Figure 72 - Delay simulated depending of the input for several bandwidth

3 is thus reached by designing the CT-CMP with a bandwidth presenting flat latency response for the major part of the input dynamic. A bandwidth with a cutoff frequency at 740MHz as represented on Figure 72 for example presents the targeted behavior. The bandwidth of the comparator is thus critical for linearity of the second stage conversion. This can be seen in (4.3), and the same behavior shown in Figure 69 can be observed around the null differential voltage.

Due to this analysis and conclusion, the next subsection details another design of CT-CMP to increase bandwidth and alleviate input dependencies.

4.3 Folded Cascode CT-CMP

The CT-CMP designed for this work tends then to explore the trade-off between gain, bandwidth and consumption.

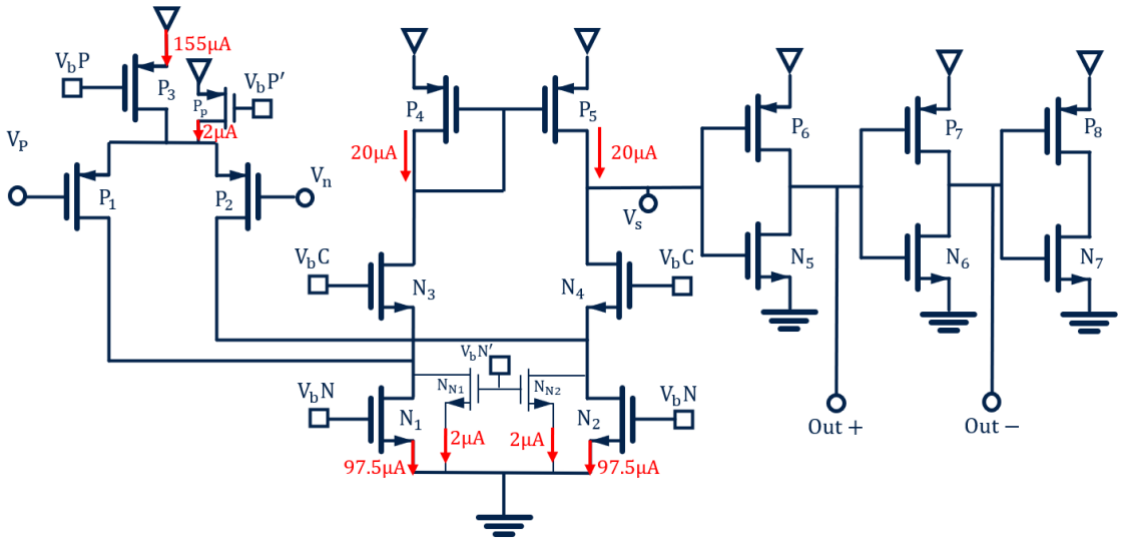

Figure 73 - Schematic of the proposed folded cascode CT-CMP to increase bandwidth.

Amongst different structures of amplifiers, the folded cascode topology has been chosen to place the dominant pole on the output. The bandwidth is then determined by the output impedance and the load capacitance. Unlike the cascaded amplifier presented in previous sections, the output is isolated by a cascode stage. Nevertheless, because of the saturation voltage of the transistors, it is not possible to put 4 MOS transistors saturated in series between the supply and the ground. With respect to a classical topology [74] the cascode transistors isolating the PMOS current mirror $P_4 - P_5$ have been removed. This induces lower output impedance thus less gain. To reach high transconductance, the input pair must be wide, which brings parasitic capacitance. In the folded cascode structure the input differential pair is isolated from the output node by the folded cascode transistors. Higher gain can be implemented with

more important input-pair transconductance without modifying the amplifier bandwidth. With equation (4.2) terminology, the cutoff frequency of the amplifier part of the comparator can be described as:

$$f_{-3dB} = \frac{gd}{2\pi . C_l} = \frac{gm}{2\pi . A_d . C_l} \quad (4.4)$$

With C_l representing the load capacitance and A_d the differential gain expressed in (4.1).

The transistor sizing is summarized Table 12. Flip well transistors are used in this design to optimize performance thanks to the lower V_{th}. Input pair, cascode transistors and the digital output stage are designed with flip well transistor to increase the voltage headroom of the current sources and the speed at minimum width and length size for digital cell. Current sources and current mirrors are implemented with regular well transistors to increase matching in regards of the technology performance.

Table 12 - Transistor sizing of CT-CMP folded cascode architecture

Transistor	Width	Length	Type
N1	9µ	200n	Regular Well
N2	9µ	200n	Regular Well
N3	1µ	70n	Flip Well
N4	1µ	70n	Flip Well
N5	74n	18n	Flip Well
N6	74n	18n	Flip Well
N7	74n	18n	Flip Well
N_N1	200n	200n	Regular Well
N_N2	200n	200n	Regular Well
P1	40µ	70n	Flip Well
P2	40µ	70n	Flip Well
P3	16µ	70n	Regular Well
P4	2µ	18n	Regular Well
P5	2µ	18n	Regular Well
P6	74n	18n	Flip Well
P7	74n	18n	Flip Well
P8	74n	18n	Flip Well
P_P	200n	18n	Regular Well

The folded cascode CT-CMP presents high bandwidth performances with 820MHz 3dB cut-off frequency and 43.5dB of gain. The transfer function of the comparator is drawn in Figure 74 and presents gain-bandwidth product of 126.3GHz. The unity frequency gain is only at 21GHz du to non-dominant poles and zeros. The input referred noise simulated at schematic level is 76µV RMS which is below the specification of 154 µV RMS.

With this bandwidth the non-linearity brought by the bandwidth limitation is reduced and presents only DNL smaller than half LSB on first codes. The static delay to correct is around 200ps which represents 4 units delays for the delay line. The presented performances postition the folded cascode topology favorably compared to a two stages approach for the realization of a CT-CMP.

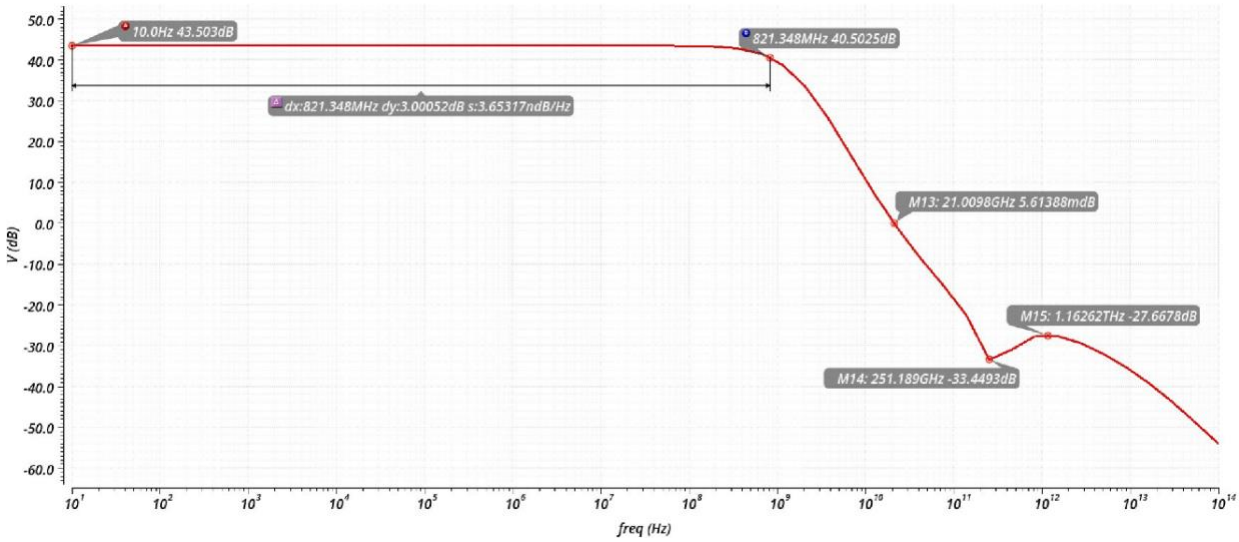

Figure 74 - Transfer function of the proposed folded cascode CT-CMP – no offset correction

Next section discusses the bias stage and switch on-off management circuitry.

4.4 Bias and Start-up stage

The comparator needs to be switched on in a short time to reach short conversion time and low power consumption. This section details the bias stage used to switch on the comparator.

In reference realizations, the start-up of the comparator is implemented with series transistors used as switches to start and stop the current flow into the branches. Because of the difficulty of keeping 3 series transistors saturated in the selected technology with 0.9V of voltage headroom, series switches cannot be implemented even with low drain source voltages. Because the comparator needs to be switched on and

off in a short time to reduce power consumption of the second stage and to avoid extra management circuitry, the bias stage drives the on and off of the CT-CMP

Figure 75 details the proposed bias and start-up circuit. The current brought by the SOC's power management unit, considered ideal in these simulations, is 1µA. This current is then copied with a 10x factor into the main branch which is always on. This branch is used as reference with transistor N_{b1} generating the V_bN master voltage of transistors N_1 and N_2 in Figure 73. The branch used to generate the cascode bias voltage is also always on and consumes 5µA with transistor N_{c1} and P_{c1}. These two always on branches add static consumption to the comparator. Switches are inserted to connect a second branch

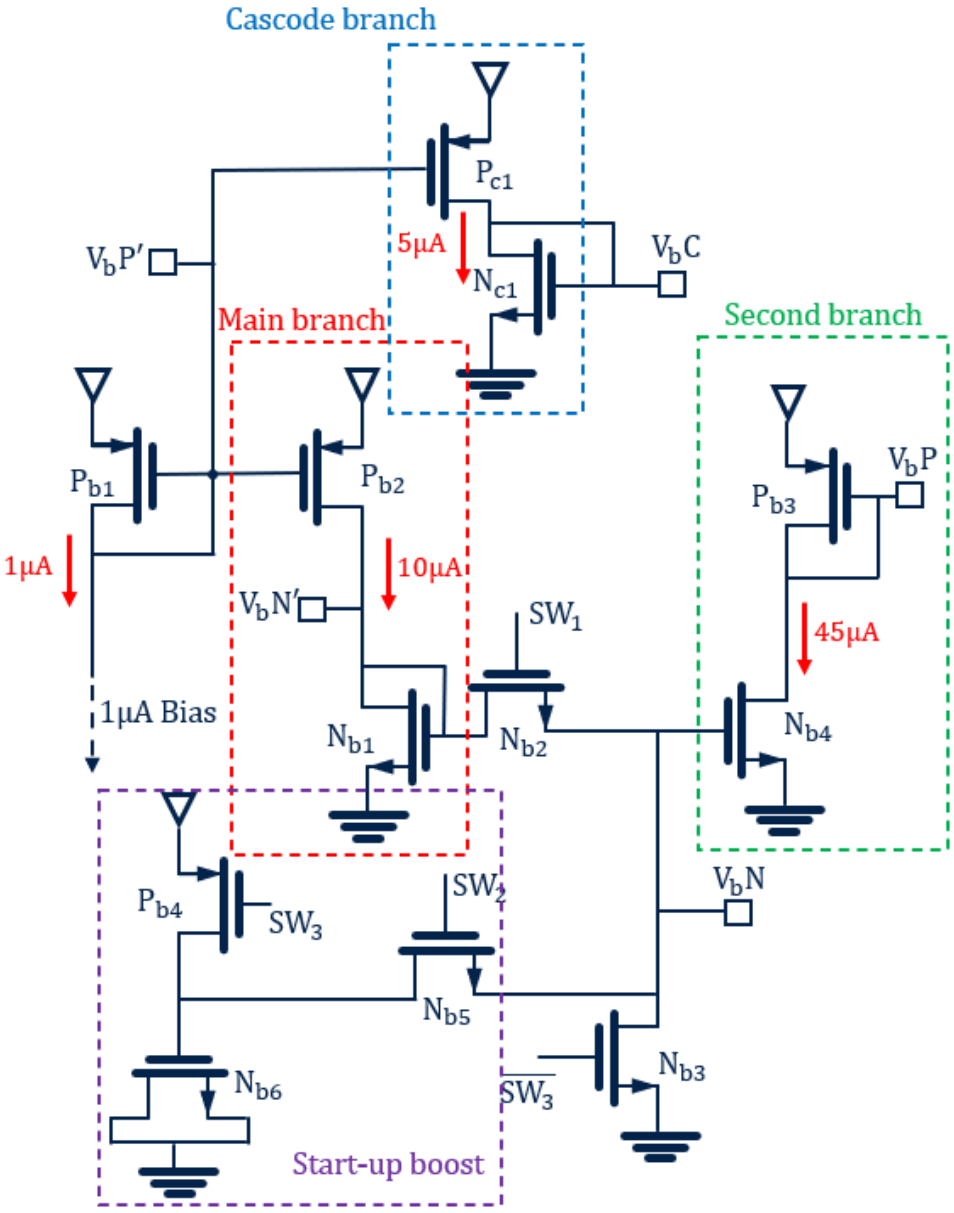

Figure 75 - Schematic of the proposed bias stage used to start-up the comparator.

composed of transistors N_{b4} and P_{b3} used to generate the master voltage V_bP for the input pair current source P_3 on Figure 73. Thanks to the added switches N_{b2} and N_{b3}, the V_bN node can be disconnected from the reference and the nodes V_bN and V_bP can respectively be pulled to 0V and VDD to turn the comparator off.

Because of many transistors connected to the V_bN node, the parasitic capacitance is important which slows the start-up of the comparator. To reduce the time spent to charge the capacitance on V_bN node, extras switches are added to briefly connect a pre-charged MOS capacitor to the node as a start-up boost as shown on Figure 75. The charge sharing between capacitances establishing the level of the node V_bN to a voltage close to the wanted voltage thanks to an appropriate sizing of the MOS capacitor. A short analog delay determines the interval for the charge sharing. The MOS capacitance is then disconnected and the switch N_{b2} is closed to connect the main branch to V_bN . The start-up boost circuit also reduces coupling effects in the CT-CMP during the start-up which can degrade start-up performance. The Timing diagram for the proposed start-up scheme is presentes in Figure 76.

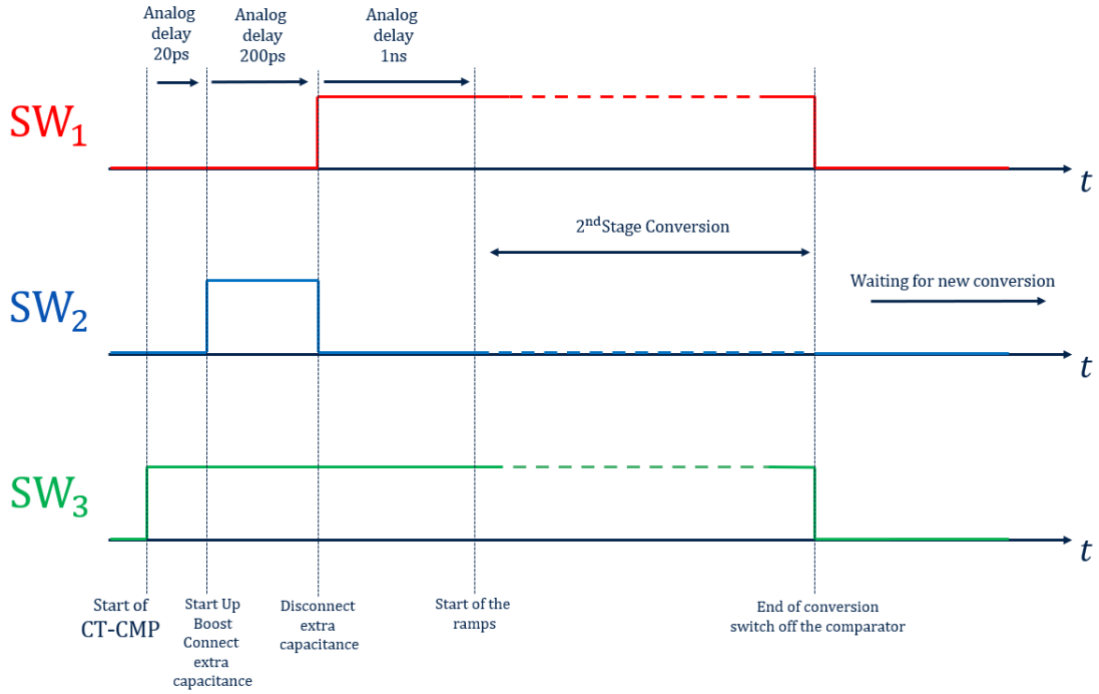

Figure 76 - Timing diagram of the start-up command

To further reduce start-up time, small current sources are added in the comparator. As represented on Figure 73, transistors N_N1, N_N2 and P_P maintain a small current flow in the comparator to avoid complete discharge of internal nodes to VDD or ground. This allows to maintain off-state node voltages as close possible to the on-state voltage and reduces startup time without important extra current power consumption. The corresponidng gate bias voltages are generated in the bias stage with nodes V_bN' and

V_bP'. This added current represents around 4µA in the comparator power budget. These 4µA are consumed continuously.

The sizing of the transistors for the bias stage is presented in Table 13, the type and size are coherent with the ones given in Table 12 for the comparatore core.

Table 13 - Transistors sizing of CT-CMP cascode bias/start stage

Name	Width	Length	Type
N_{b1}	1µ	200n	Regular Well
N_{b2}	3µ	18n	Flip Well
N_{b3}	2µ	18n	Flip Well
N_{b4}	4µ	200n	Regular Well
N_{b5}	3µ	18n	Flip Well
N_{b6}	9µ	200n	Regular Well
N_{c1}	84n	70n	Flip Well
P_{b1}	100n	18n	Regular Well
P_{b2}	1µ	18n	Regular Well
P_{b3}	4µ	70n	Regular Well
P_{b4}	1µ	100n	Regular Well
P_{c1}	400n	18n	Regular Well

The presented design reaches a start-up time under 600 ps for a typical schematic simulation. Process and temperature will affect this value and can reach ‘1ns’ of start-up time from single corner simulations. This start-up time is correct and allows the system to efficiently use the second stage by quickly turning on the CT-CMP. A sequence of start and stop with null comparator input voltage is simulated and shown in Figure 77 to see if there is a dependency on the previous state. There is no relevant dependency. The turning off phase seen on Figure 77 represents ns to establish and bias the amplifier with voltage close to the on state. That is because small current sources are added in parallel of the current sources $(N1, N2 \text{ \& } P3)$ represented in Figure 73 to add always on current.

The designed folded cascode CT-CMP presents adequate performances based on schematic level simulations to reach low noise, low consumption, fast start-up phase and high bandwidth limiting the non-linearity effects. The proposed bias start-up consumes some static power which could be improved for

next generations. However, parasitic elements are added with the layout phase and proved to be non negligeable as discussed in the next section.

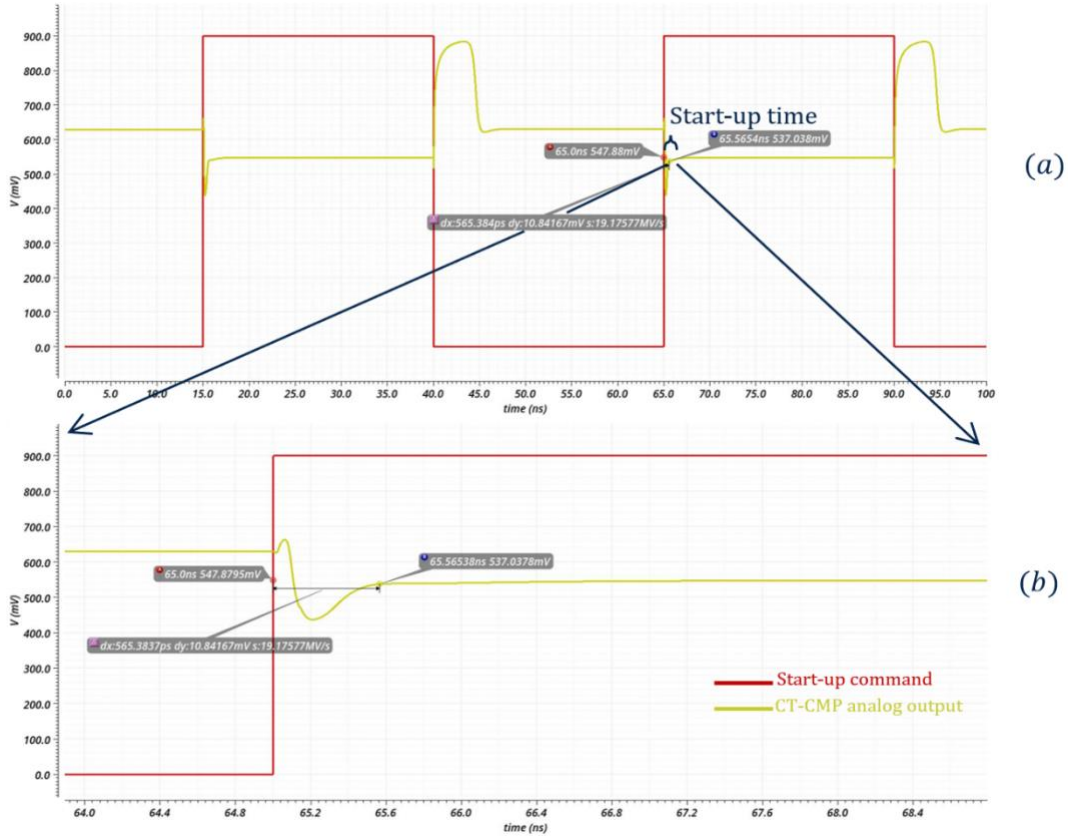

Figure 77 - (a) Sequence of start & stop to measure comparator timing - (b) Zoom on start-up

4.5 Layout and PLS results

With the support of ST team, a layout of the folded cascode CT-CMP has been done in 18nm FD-SOI CMOS Technology. The layout provides more accurate data on parasitics thanks to extraction of parasitic capacitances and resistances directly from the layout. The technology presents highly resistive wires and several process constraints adding dummies for density purpose which increase the number of parasitic capacitances. The layout is presented in Figure 78, carefully realized to reduce extra capacitance on the output voltage node to minimize bandwidth reduction. Main components are highlighted in Figure 78. Scales are expressed in µm. The comparator represents an area of 336µm². Simulations shown previously at schematic level have again been performed after parasitic extraction. Three abstraction

levels of parasitics named R, Cc and RCc are used. They correspond to the following extraction parameters:

- R: Only resistive parasitics are extracted
- Cc: Only capacitive parasitics are extracted
- RCc: Both resistive and capacitive parasitics are extracted

From layout parasitic extraction RCc, Figure 79 shows the simulated transfer function of schematic CT-CMP already seen in Figure 74 compared to post extract simulation. It can be seen that gain increased by 4dB and bandwidth decreased by 500MHz. This is due to parasitic resistance in bias stage reducing current in the comparator and consequently the power consumption. However, the performances are degraded as it can be seen in Table 14.

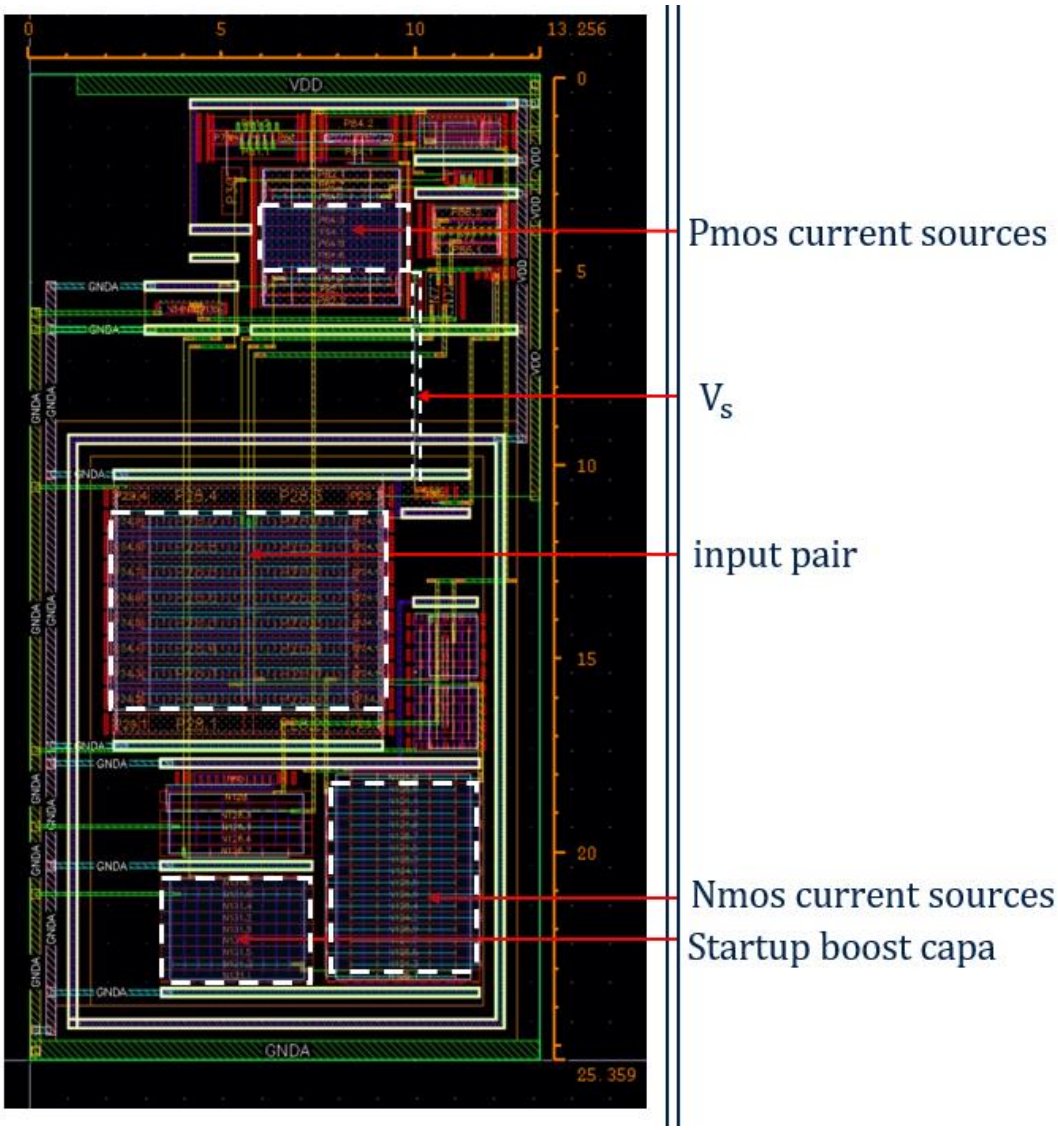

Figure 78 - Layout of the folded cascode CT-CMP

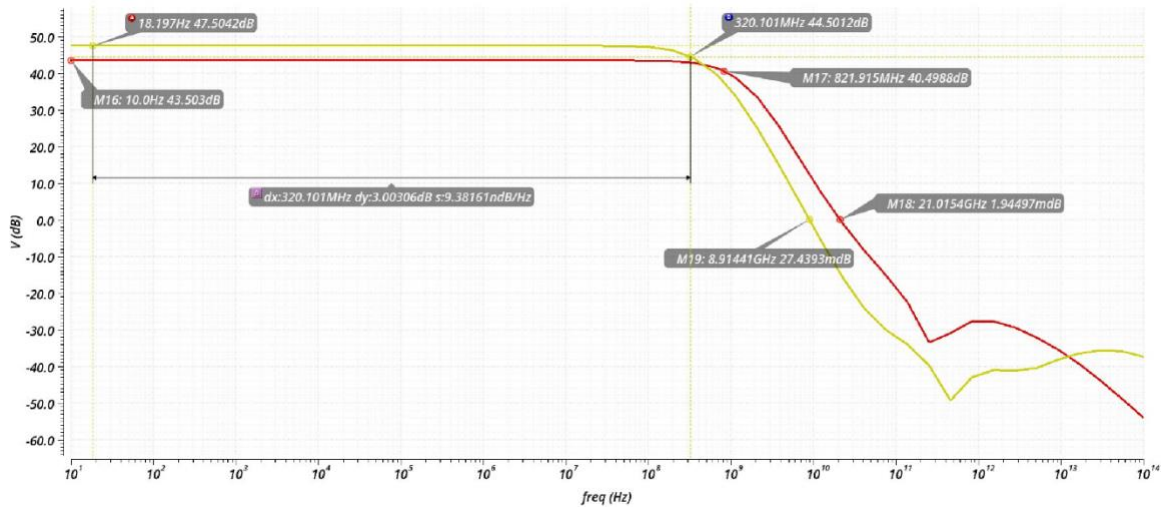

Figure 79 - Transfer function of the proposed folded cascode CT-CMP with schematic and RCc view – no offset correction

With the different parasitic extracted views, the impact of extra resistance and capacitance from the layout can be underlined. The schematic and R extraction view detailed in Table 14 shows gain, bandwidth, noise, and consumption performances. This is coherent with extra resistance. Less current in the MOS branches induces less consumption and consequently increased gain and lower bandwidth. With higher gain the input referred noise is also diminished. From comparison between schematic and Cc extracted view, performances are also modified. No variation in gain, independent of the capacitance, lower bandwidth, and less noise can be seen. Extra capacitances filter the noise and reduce the bandwidth. From RCc comparison, a mix of all the mentioned phenomena is presents with higher gain lower

Table 14 - Resume of comparators performances (2stage, folded with schematic and extracted views) – no offset correction

Parameter	2 stage amp sch	Folded sch	Folded R	Folded CC	Folded RCC
Gain	65 dB	43. 5dB	47.5 dB	43.8 dB	47.5 dB
Bandwidth (-3dB)	57MHz	820MHz	482MHz	600MHz	320MHz
Power (DC)	180µW*	237µW	201µW	236µW	201µW
Noise(IRN)	49.43µV_{RMS}	93.8 µV_{RMS}	72µV_{RMS}	83µV_{RMS}	61.03µV_{RMS}
Switch-on time	No data**	565ps (2% precision) 1. 2n (1% precision)	631ps (2% precision) 647ps (1% precision)	557ps (2% precision) 915ps (1% precision)	657ps (2% precision) 737ps (1% precision)

* No bias
** No startup implemented

bandwidth and less consumption. The reduced bandwidth has a very negative impact on the ADC linearity. Methods to reduce this impact on the ADC linearity will be proposed in the following chapter.

As discussed in Chapter 3, a calibration offset scheme is present in the proposed ADC. Because the CT-CMP is composed of an amplifier stage and an inverter stage, a systematic offset is present. This is caused by the difference between the voltage threshold of the inverter and the output voltage presented by the amplifier at the crossing time is intrinsic to the architecture. This systematic offset is dependent on the reference voltage, process and temperature variation. To measure this systematic offset a DC simulation spanning input differential voltage is done and the input voltage causing output variation of the inverter is then considered as the systematic offset. To correct this offset the part of the CDAC dedicated to calibration is then used. This method modifies the bias point of the amplifier and can induce important variations on the amplifier stage parameters such as bandwidth. The performances obtained after systematic offset calibration are presented in Table 15.

Table 15 - Resume of comparators performances with offset correction (2stage, folded with schematic and extracted views)

Parameter	2 stage amp sch	Folded sch	Folded R	Folded CC	Folded RCC
Gain	65 dB	44. 5dB	49.32 dB	44.58 dB	49.32 dB
Bandwidth (-3dB)	57MHz	445MHz	254.7MHz	341.3MHz	178.5MHz
Power (DC)	180µW*	244.5µW	210µW	244µW	210µW
Noise(IRN)	49.43µV_{RMS}	76.36 µV_{RMS}	56.64µV_{RMS}	70.29µV_{RMS}	50.55µV_{RMS}
Systematic Offset	/	-2.005mV	-1.404mV	-1.881mV	-1.404mV

* No bias

As presented in Table 15, the bandwidth and gain of the CT-CMP with offset corrected are different than the amplifier performances simulated in previous paragraphs. This is due to a variation of the gm of the input differential pair as seen in equation (4.1) and (4.4). Also the performances show nonlinear variations compared to Table 14 due to lower VDS in current source P3 in Figure 73.

To quantify offset correction capacity of the proposed calibration scheme on the designed comparator, Monte Carlo simulations with 1000 steps have been run on the folded cascode structure. The maximum offset simulated for the schematic view is ±13.2 mV considering the systematic offset of the structure. With the layout RCc extracted view, the Monte Carlo simulation has been done considering same parameters plus the matching and the TSI (silicon film thickness) matching inherent of SOI

technology nodes [75]. The bias used is presented in Figure 75 with 1µA of input reference current and RCc post extract view. The offset is measured from DC simulation of the comparator response as for the systematic offset. Figure 80 shows the histogram of Monte Carlo offset measurement with systematic offset corrected through process and mismatch variations.

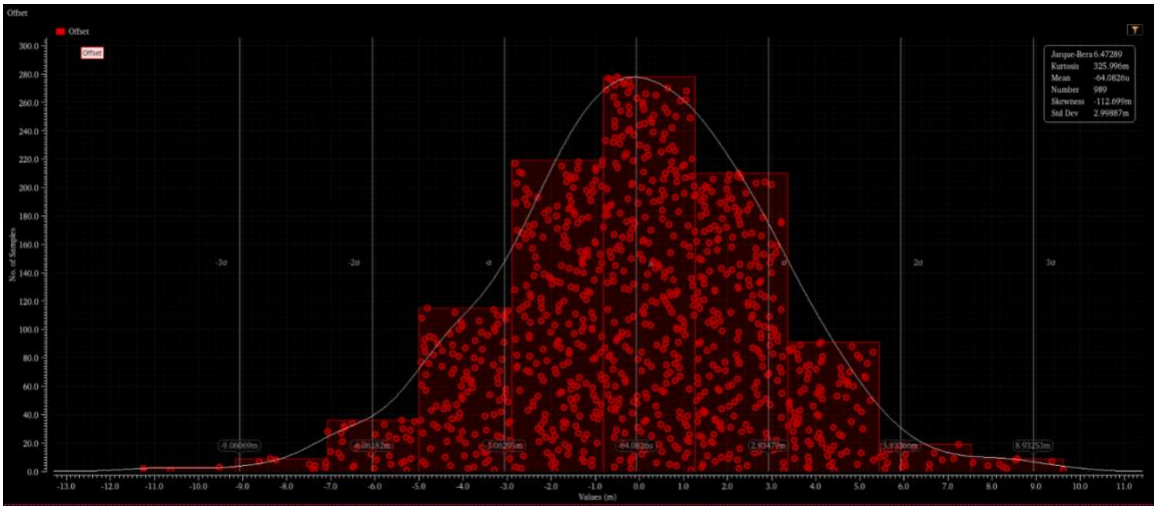

Figure 80 - Offset Monte Carlo histogram simulation for RCc view – systematic offset corrected

The Monte Carlo simulation shows that the offset for the layout RCc view is within ±12mV range which means that correction CDAC implemented and discussed in Chapter 3 presents sufficient dynamic to correct worst case offset including mismatch. Nevertheless, once the systematic offset of the comparator is corrected the input bias is changed from optimal bias point and the observed bandwidth decreases below the previously simulated value. Table 15 resumes the performances of views presented in Table 14 once the systematic offset is corrected. Important bandwidth degradations are induced which will increase non linearity previously discussed.

4.6 Conclusion

This chapter presents an overview of the CT-CMP architectures for SAR assisted DS ADC topologies. Amplifier based structures with low bandwidth are commonly used to filter the staircase ramp at the input of the comparator but they induce delay and, more importantly, non linear errors on some codes. System-level technics could reduce this impact but with increased conversion time and power consumtion. A theoretical anlysis predicts that at CT-CMP bandwidth of 740MHz would allow to reduce the non-linear errors below 1 LSB. A folded cascode amplifier based CT-CMP is proposed in order to increase sufficiently the bandwidth. Another bottleneck is the startup time of the CT-CMP. An innovative

bias and start-up is proposed adding switched boost capacitor to reduce the startup time. Nevertheless, when including parasitic elements from the layout and offset correction, the bandwidth performance is significantly degraded. The non linearity has been reduced but is still significant. Futher increase of the bandwidht would require more power and circuit area. As an alternative, the next chapter will explore system level technics to overcome the effects of the limited bandwidth of the comparator.

Chapter 5

CT-CMP Non-linearity compensation and correction

5.1 NON-LINEARITY IN CT-CMP 128

5.2 NON-LINEARITY COMPENSATION 130

5.2.1 COMPENSATION OF THE NON-CONSTANT DELAY AT THE BEGINNING OF THE RAMP 131

5.2.2 COMPENSATION OF THE NON-CONSTANT DELAY AT THE END OF THE RAMP 133

5.2.3 VALIDATION OF THE LINEARIZATION WITH POST-LAYOUT SIMULATIONS 134

5.3 DIGITAL POST-CORRECTION 137

..... 138

5.3.1 DELAY MODEL 138

5.3.2 MODEL BASED OUTPUT ERROR CORRECTION 139

5.3.4 VALIDATION OF OUTPUT ERROR CORRECTION WITH SIMULATED DATA 141

5.3.4 PRACTICAL IMPLEMENTATION OF DIGITAL POST CORRECTION 141

5.5 CONCLUSION 143

5.1 Non-linearity in CT-CMP

The concept of the second stage is to detect a sign change on its input in response to the ramps applied at the input of the continuous time comparator. Because the comparator is presenting low pass transfer function which can itself be modeled as linear time invariant circuit, its dynamic response to the ramp produces varying time delay at its output. The time dependent delay produces a non-linear relation between the input voltage and the transition time at the output of the comparator quantized be the delay line in the converter.

With the approximate model given in chapter 4 (Fig. 4.6) describing the comparator with an embedded 1st order low pass filter, the static latency and the impact of the dynamic response can be studied with a mathematical model in MATLAB.

The time domain input signal and the output signal of the preamplifier in the comparator given by the MATLAB model scaled to the same amplitude are shown in Figure 81. For better clarity, the staircase ramp input signal shown represents the differential input voltage at the comparator input with negative slope. The input ramp has -400µV steps (1 LSB) every 50ps. A corresponding linear ramp with the same

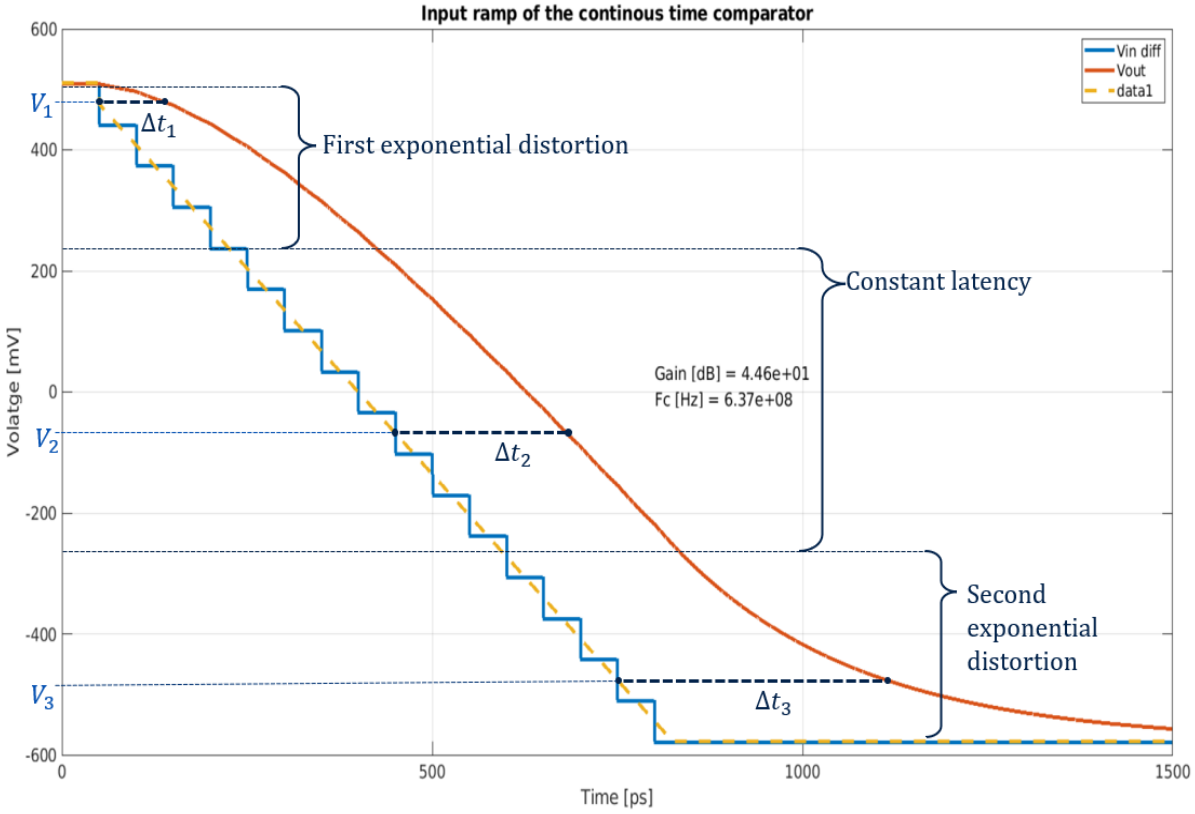

Figure 81 - Temporal model representation of the input and output linearized of the CT-CMP for a given bandwidth.

starting point is also shown for comparison purposes. The comparator's preamplifier gain and bandwidth in this example are respectively 44,6 dB and 637 MHz.

In Figure 81 the redundancy and offset steps applied prior to the start of ramp are not represented and the input voltage is considered to be well established at the starting point of the ramp. Furthermore, the ramp is shown here for a midrange value of the SAR ADC residue at the end of the 1st step conversion. In practice, the ramp starting point will be the actual value of residue of the SAR, changing the comparator's input crossing point accordingly.

As can be seen in Figure 81, the time domain model clearly shows the dependency of the latency on the position of the input crossing point in the ramp. Consequently, the output codes produced for cross-points close to the beginning and end of the ramp are incorrect with respect to a constant delay model such as used in the literature [3] [73]. In Figure 81 several examples are indicated : i.e. if the crossing occurs at the level of V_1, the latency Δt_1 is shorter than the latency Δt_2 for a crossing at level V_2. Because the comparator presents a first order filter response, an exponentially decreasing delay error is introduced at the start of the ramp. The response tends progressively towards a constant latency equal to the time constant of the filter. Reference [76] mentions this problem for the case of a linear ramp signal and proposes a mathematical model for the response. Symmetrically, a similar behavior but with the effect of increasing the latency can be observed at the end of the ramp reproducing the form of the transient

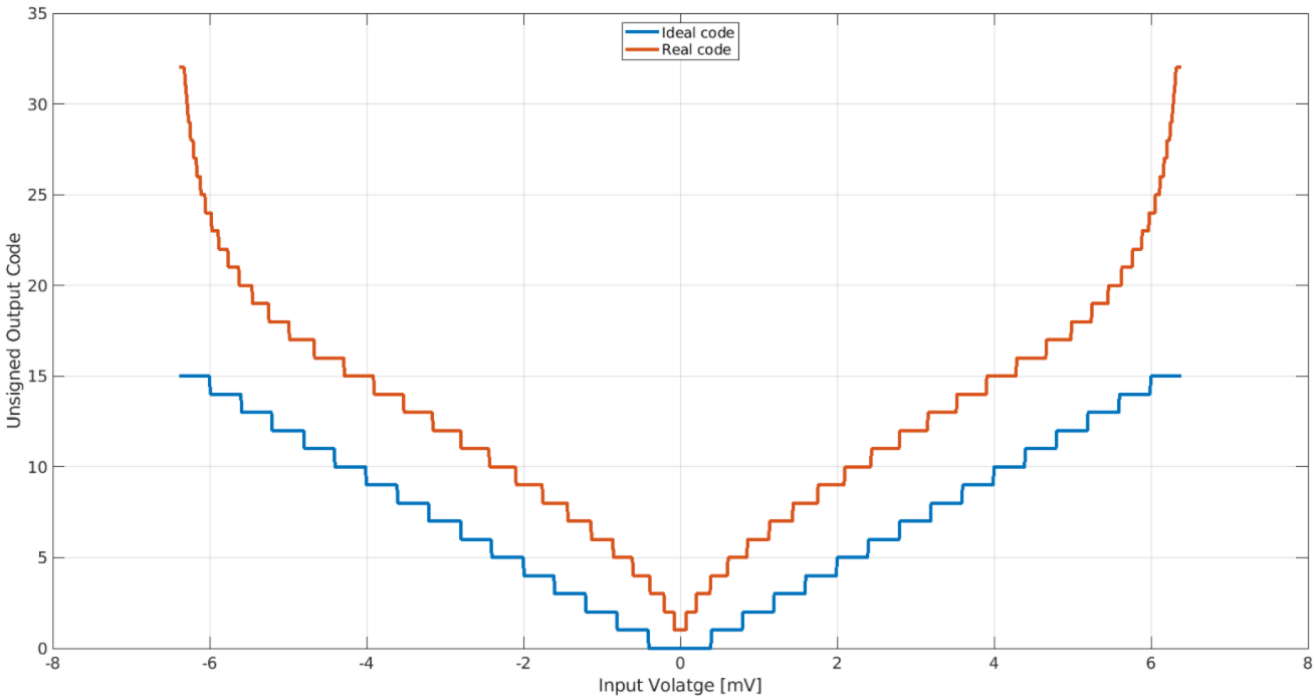

Figure 82 – Simulated unsigned output code vs. ideal unsigned output code over the ±4 bit input range (LSB = 400µV, BW = 637MHz, Timestep 50ps, 16 steps)

response of a 1st order low-pass filter to the finite length ramp input.

Figure 82 shows the produced code as a function of the input voltage (residue + redundancy step) applied to the second stage for the complete system with both positive and negative slope ramps. The crossing point in the ramp is directly proportional to the absolute value of 2nd stage input voltage. Due to the sign dependent bidirectional ramp architecture, the raw codes are symmetrical with respect to the zero input. As expected, the codes for input voltage close to 0V are affected by the first exponential behavior represented on Figure 81 because the crossing point is reached shortly after the start of the ramp. In the mid-range the output codes are approximately proportional to the input voltage as the latency is constant. For higher input voltages the code values increase exponentially. For the maximum input voltage the value of the code is represented by the maximum value because the latency is beyond the time interval of observation determined by the length of the delay line and the crossing is actually not detected in the mathematical model.

The following sections discuss different approaches to overcome the nonlinear effects of the CT-CMP. The next section studies the possibility of adding additional steps to the ramp, while the 3rd section introduces a novel approach based on remapping the digital codes.

5.2 Non-Linearity Compensation

The simplest approach to avoid non-linear conversion errors is to increase the number of steps in the ramp and delay line in order use only the portion of the ramp where the latency is constant as shown in Figure 83. This comes at the cost of increased conversion time and higher power consumption degrading both conversion speed and efficiency.

The relations between conversion accuracy, comparator bandwidth and the required number of additional ramp steps are discussed in the following sub-sections both for the beginning and the end of the ramp. The effectiveness of the approach is then checked for the proposed architecture with time-domain system simulations including transistor level simulation of the comparator with back annotated parasitics (resistors and capacitors) to verify that the results are not degraded by other non-linear effects not included in the simple mathematical model.

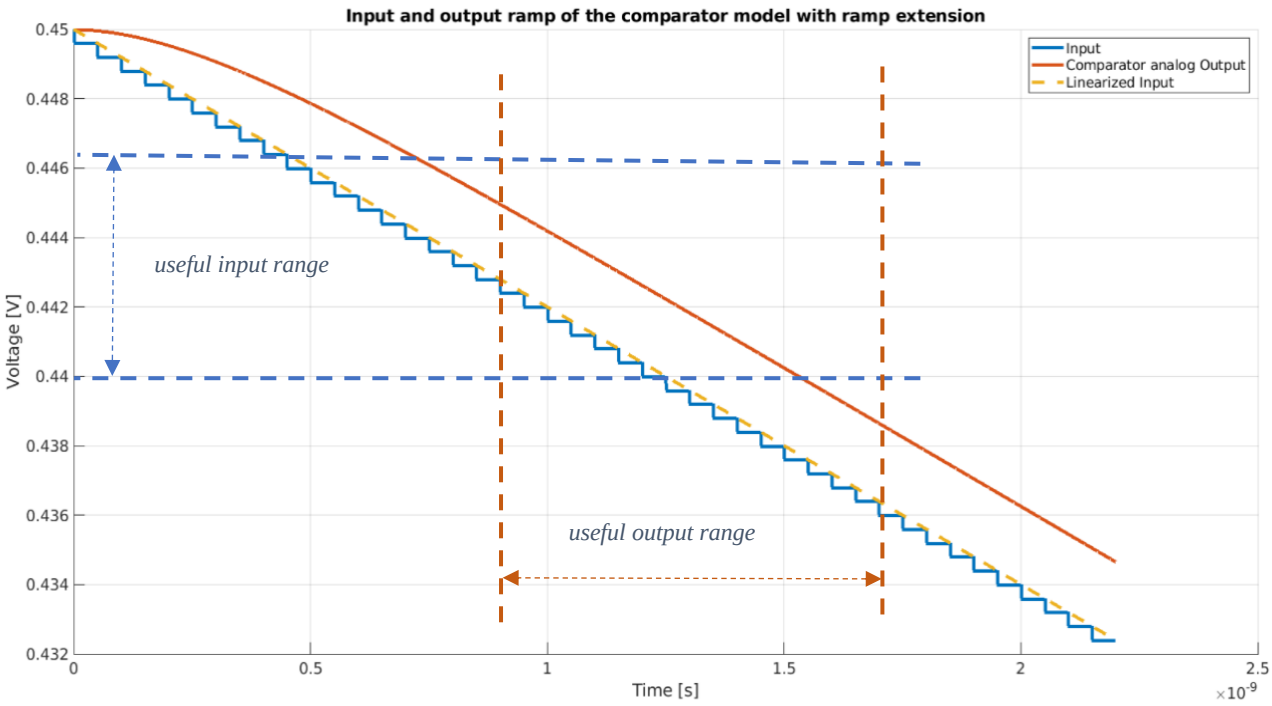

Figure 83 - Temporal model representation of the input and output linearized of the CT-CMP for a given bandwidth with ramp extension

5.2.1 Compensation of the non-constant delay at the beginning of the ramp

To avoid conversion errors due to the non-constant delay at the beginning of the ramp, it is possible to add extra steps to the ramp as well as a corresponding offset to the input voltage [76]. In example, if k extra steps and an input offset of k*V_{LSB} are added, the zero crossing at the input of the CT-CMP occurs at the earliest after k+1 steps. The number of steps must be determined such that conversion error due to the non-constant delay is below the targeted accuracy after k steps. If the initial quantized comparator latency is equal to j timesteps, the total latency seen at the system level becomes now j+k timesteps as shown in Figure 84. No changes are necessary at the system level as the algorithm described in chapter 3 will correctly determine the j+k timestep latency .

The number of required steps can be determined approximately from the mathematical model for a linear ramp :

$$V_{out}(t) = V_0 - \frac{V_{LSB}}{t_{step}}\left(\mathrm{t} - \frac{1 - e^{-\omega_{-3dB}.t}}{\omega_{-3dB}}\right) \tag{5.1}$$

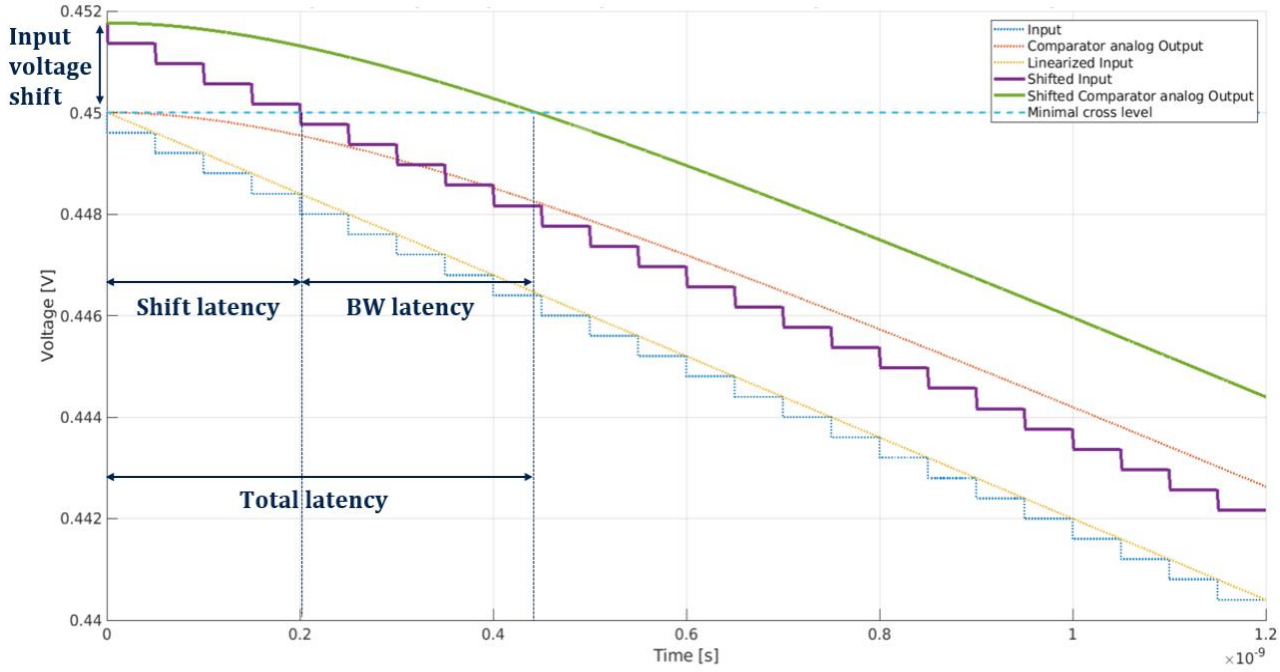

Figure 84 - Temporal model representation of the input and output of the CT-CMP for a given bandwidth with ramp extension and shifted input to compensate first distortion.

With $\frac{V_{LSB}}{t_{step}}$ the ramp coefficient, ω_{-3dB} the bandwidth of the equivalent low pass filter and V_0 the starting voltage of the ramp. By setting t to k*t_{step}, substituting $1/\omega_{-3dB}$ by $\tau = {}^{1}/_{\omega_{-3dB}}$ and rearranging the terms, the corresponding output voltage is :

$$V_{out}(\mathrm{k} * t_{step}) = V_0 - \frac{V_{LSB}}{t_{step}}(\mathrm{k} * t_{step} - \tau) + \frac{V_{LSB}}{t_{step}} * \tau * e^{-\frac{k*t_{step}}{\tau}} \qquad (5.2)$$

The first term of the right hand side is the starting voltage of the ramp, the second term represents the ideal linear ramp delayed by τ, and the third term the difference bewteen the actual and the ideal value of the output at t= k*t_{step}. Assuming that this voltage difference is equal or less than V_{LSB} , we can approximate the resulting conversion error normalized to 1 LSB as

$$\varepsilon = \frac{\tau * e^{-\frac{k*t_{step}}{\tau}}}{t_{step}} \qquad (5.3)$$

An approximate minimum number of timesteps can the be calculated as

$$k = \frac{\tau}{t_{step}} * \ln\left(\frac{\tau}{\varepsilon * t_{step}}\right) \tag{5.4}$$

In the example of Figure 82, $\frac{\tau}{t_{step}} = 4.8$ and by setting $\varepsilon = 1$ in equation (5.4) gives $k = 7.5$. When checking this value with respect to Figure 82, this results in an "overdesign". Setting $\varepsilon = 2$ gives $k = 4.2$. When using k=4, the quantized total latency will be $9 * t_{step}$with a maximum error below2 LSB. More generally speaking, the ratio $\frac{\tau}{t_{step}}$ is the key parameter determining the dimensioning of the staircase ramp and the length of the delay line of the converter.

5.2.2 Compensation of the non-constant delay at the end of the ramp

The sudden stop at the end of the ramp increases the theoretical delay exponentially due to the filter low-pass function. Additionally, the static differential input voltage at the comparator input for a crossing point at the end of the ramp becomes very small, thus further increasing the response time of the comparator. A very simple way of avoiding this increase of the delay is to add a few extra steps to the end of the ramp. Indeed, continuing the ramp until the comparator has toggled will maintain the latency constant. The duration of the extra steps should be equal or slightly larger than the latency of the comparator. The extra steps don't increase the conversion time, so no degradation of the conversion speed and only very slight increase of the power consumption occurs due to the switching of the extra capacitors in the ramp. Indeed, these capacitors will only be switched for input voltages close to the maximum range and should therefore not have any significant impact on power consumption.

In the example given in Figure 82, the intrinsic comparator delay is between 4 and 5 timesteps. Looking at the results in Figure 82 shows that 4 steps beyond the normal end of the ramp should be sufficient to limit the increase of the comparator delay.

5.2.3 Validation of the linearization with post-layout simulations

The above methods have been applied to a practical example based on the comparator described in chapter 4. The 2nd stage has been simulated with the transistor level schematic of the comparator including post-layout extraction of parasitic elements in order to check the effectiveness of the ramp extension on the linearity of the ADC. The designed comparator including layout parasitics has a bandwidth of 180 MHz as opposed to the 637 MHz bandwidth in the initial design. The corresponding theoretical delay of the comparator is $\tau = 882\ pS$, equivalent to 17.7 timesteps of 50ps. For comparison purposes, the theoretical response of the 2nd stage with 16 steps given in Figure 82 for a 637 MHz bandwidth has been recalculated with the 180 MHz bandwidth as shown in Figure 85.

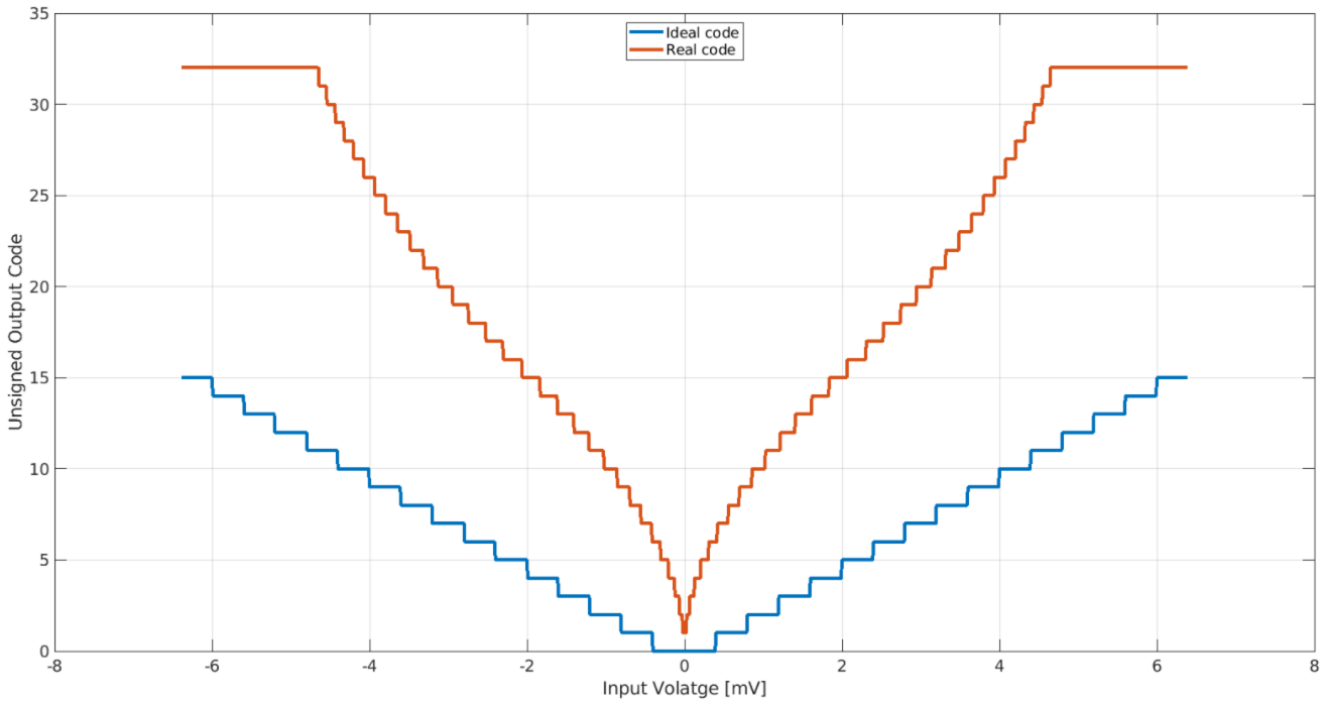

Figure 85 – Simulated unsigned output code vs. ideal unsigned output code over the ±4 bit input range (LSB = 400µV, BW = 180MHz, Timestep 50ps, 16 steps)

One can easily see that the response has been severly degraded with the reduced bandwidth and no section can be identified where the output follows the input with an approximately constant delay. For this exploration, the number of capacitors for ramp generation has then been doubled to reach 32 steps instead of the 16 steps for the initial ramp. The offset at the starting of the ramp to include redundancy is left unchanged with an offset corresponding to 4 LSB equivalent to 4 elementary steps and are included in the 32 steps. Consequently, the ramp effectively starts at -1.6mV for a positive residue value. The results are shown for crossing points from -1.6mV to 4.8mV assuming a positive residue at the output of the SAR.

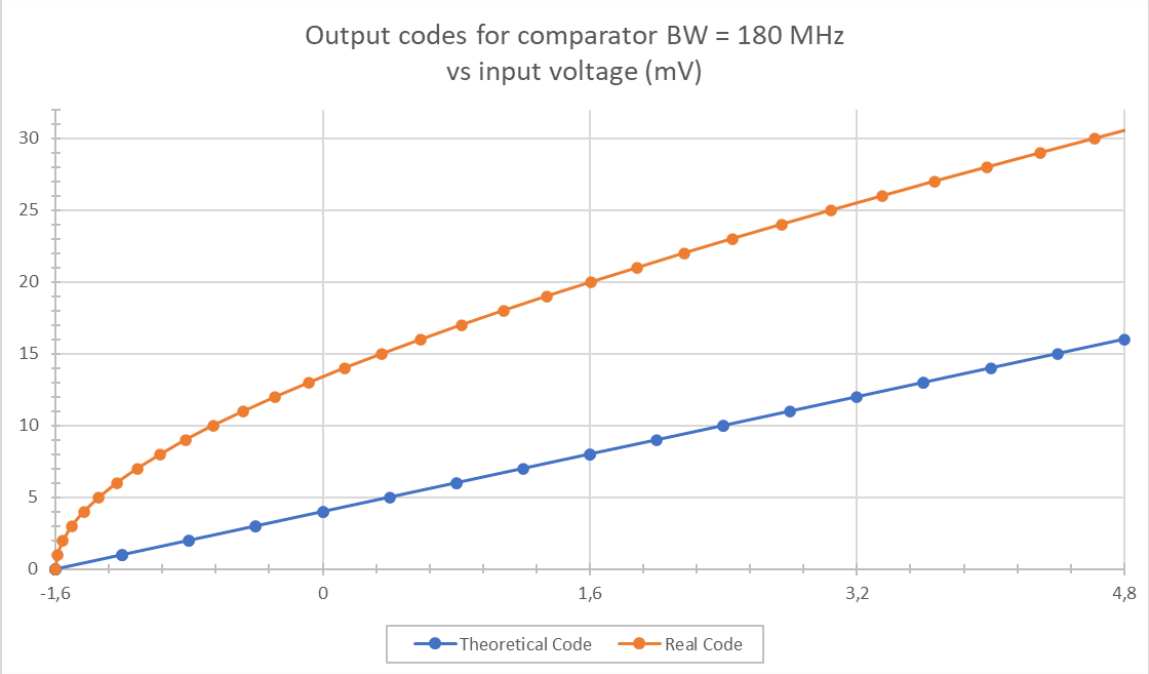

Figure 86 – Simulated unsigned output code vs. ideal unsigned output code over the ±4 bit input range (LSB = 400µV, BW = 180MHz, Timestep 50ps, 32 ramp steps in total)

As it can be seen on Figure 86, the effect of the ending of the ramp disappears, but the final constant offset of 18 steps is not attained at the end of the ramp.

From the RCc extracted view of the comparator presented in the previous chapter the same analysis as in Figure 86 has been done with time-domain simulation at transistor level for a variation of the residue voltage from 0 to 4.8 mV and 0 to -4.8mV. The initial offset step (4 LSB = 1.6mV) is added prior to the simulation, so the ramp actually starts at respectively at -1.6mV and 1.6mV for positive and negative residue values. The simulation also includes the startup phase of the comparator and the offset correction. Simulation runs corresponding to crossing point during the first 4 steps (corresponding to the redundancy steps) were not successful. Results are shown in Figure 87 for crossing points from 0 to 4.8

mV and 0 to -4.8 mV. The same behavior as the theoretical 1st order model for the same bandwidth of 180MHz and the same input voltage span (-1.6 mV to 4.8 mV) is obtained. The maximum delay observed is 14 time steps, consistent with the mathematical model which predicts the same value.

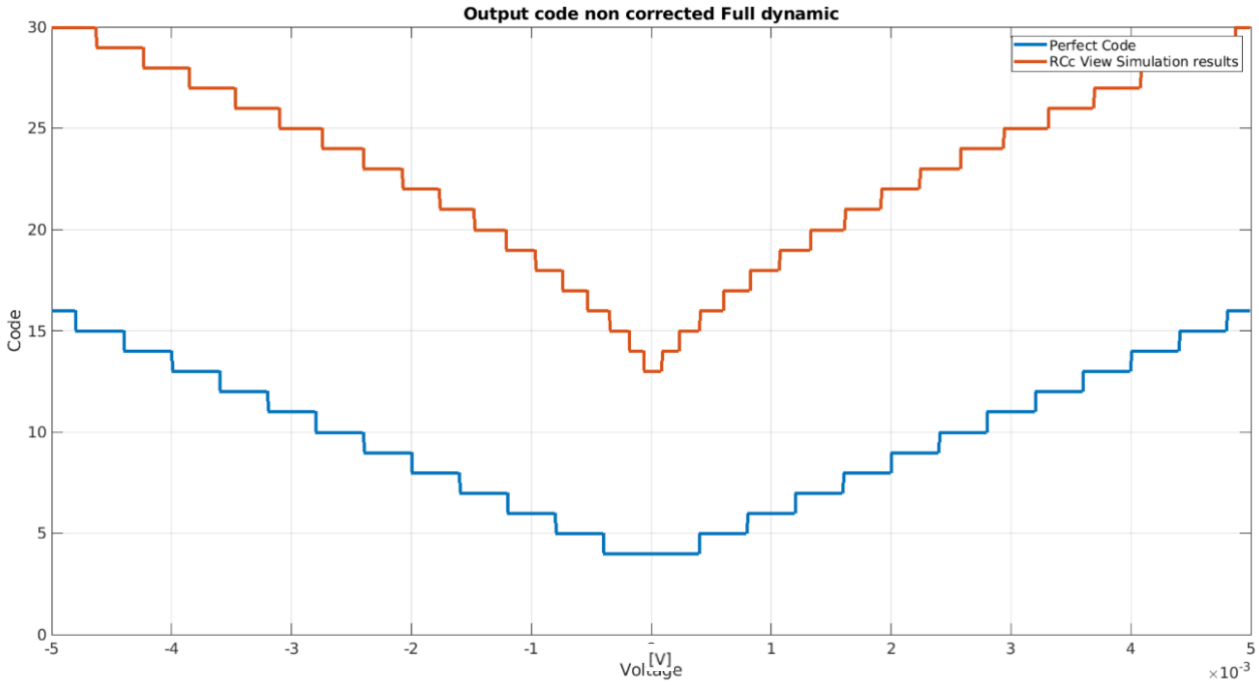

Figure 87 - Output code for RCc simulation and theoretical perfect behavior

Figure 88 presents the same data, but with an offset of -14 codes applied to the simulated output codes to subtract the maximum observed delay. This shows that the actual difference between the theoretical and the simulated output is within a one LSB limit from a zero-crossing value greater than 1.6mV, corresponding to 4 additional steps of the input ramp after the redundancy steps. It can also be seen that the response of the system is slightly different for positive and negative residues. The sign of the residue changes the direction of the ramps, and also the direction of the transition at the output of the comparator. The response of the comparator is slightly different because it includes a differential to single ended conversion in the second stage. Furthermore, the response time of the output inverter is not identical for positive and negative transitions. The combination of these two effects is responsible for the observed dissymmetry.

From this simulation it can be seen that the useable range of the stage is limited to 8 steps when a 1 LSB error tolerance is accepted. In order to reach the targeted 16 step range, 8 additional steps would be needed, pushing the ramp length from 32 to 40 steps and to add an additional offset of 8 LSB steps at the beginning of the ramp.

Furthermore, we can also compare the results of the time domain simulation with the predicted output for each quantization step from the model as shown in Figure 89.

The agreement between model and simulation is relatively close, despite some errors of up to 2 LSB that appear.

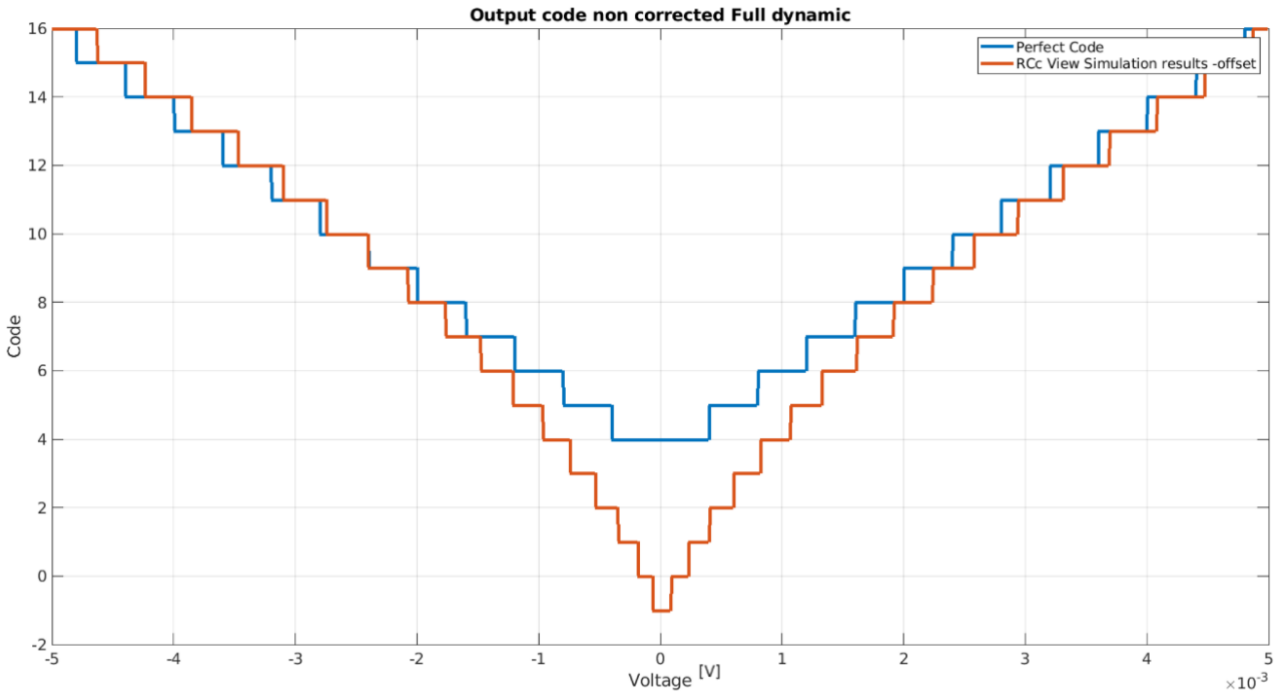

Figure 88 - Output code for RCc simulation (corrected by a 14 step constant offset) and theoretical perfect behavior.

5.3 Digital Post-Correction

The previous section presented a circuit and system level approach to mitigate the effect of the non-constant delay at the start and end of the staircase ramp. However, this approach adds extra timesteps and degrades both conversion speed and power consumption. This section explores an alternative approach by attempting to correct the variable delay by a digital post correction. The following subsections present the delay model, the practical implementation of the delay correction and the methodology to determine the key parameter of the model.

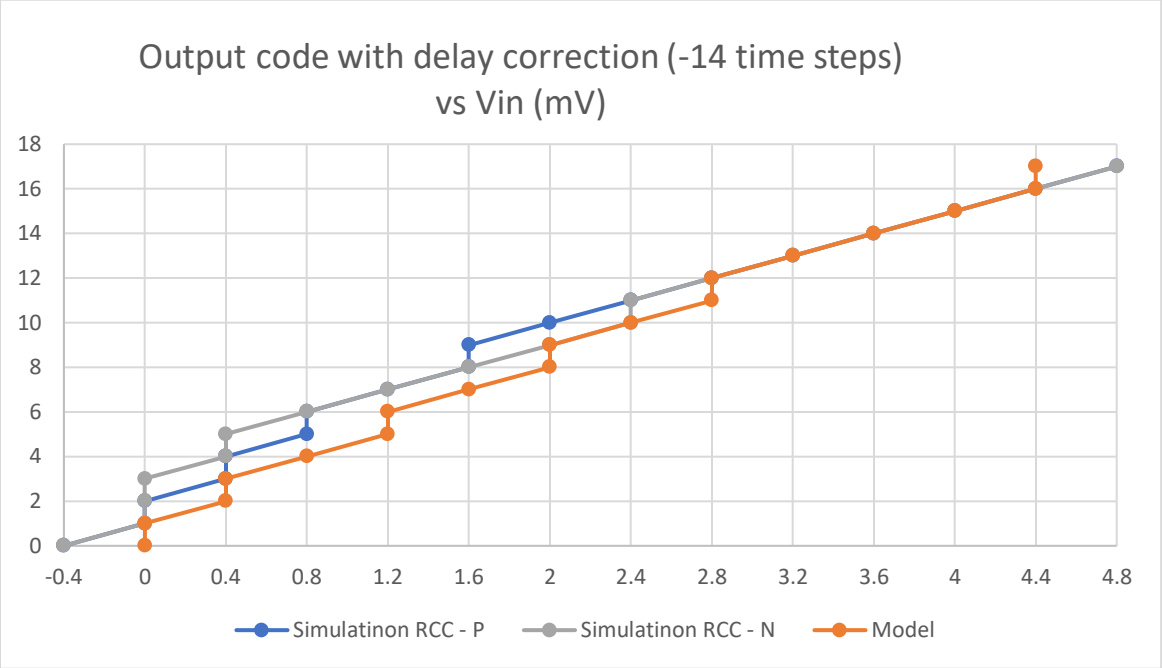

Figure 89 - Output code for RCc simulation (corrected by a 14 step constant offset) and output code predicted by mathematical model

5.3.1 Delay model

From the model for a continuous ramp discussed in section 5.2.1 a theoretical model for the delay can be derived. Figure 90 shows input and output signals of the first order lowpass filter assuming a linear ramp applied to its input.

From equation (5.1) and by substituting $\tau = {}^{1}/_{\omega_{-3dB}}$ we can isolate the time dependent latency $\Delta t(t')$ introduced by the low pass filter as observed at the output at t=t' is

$$\Delta t(t') = \tau(1 - e^{-\frac{t'}{\tau}}) \tag{5.5}$$

With τ the latency when the ramp is well established. If a zero crossing is detected at the output at time t'_1, the corresponding zero crossing at the input has occurred at

$$t_1 = t'_1 - \Delta t(t'_1) = t'_1 - \tau(1 - e^{-\frac{t'_1}{\tau}}) \tag{5.6}$$

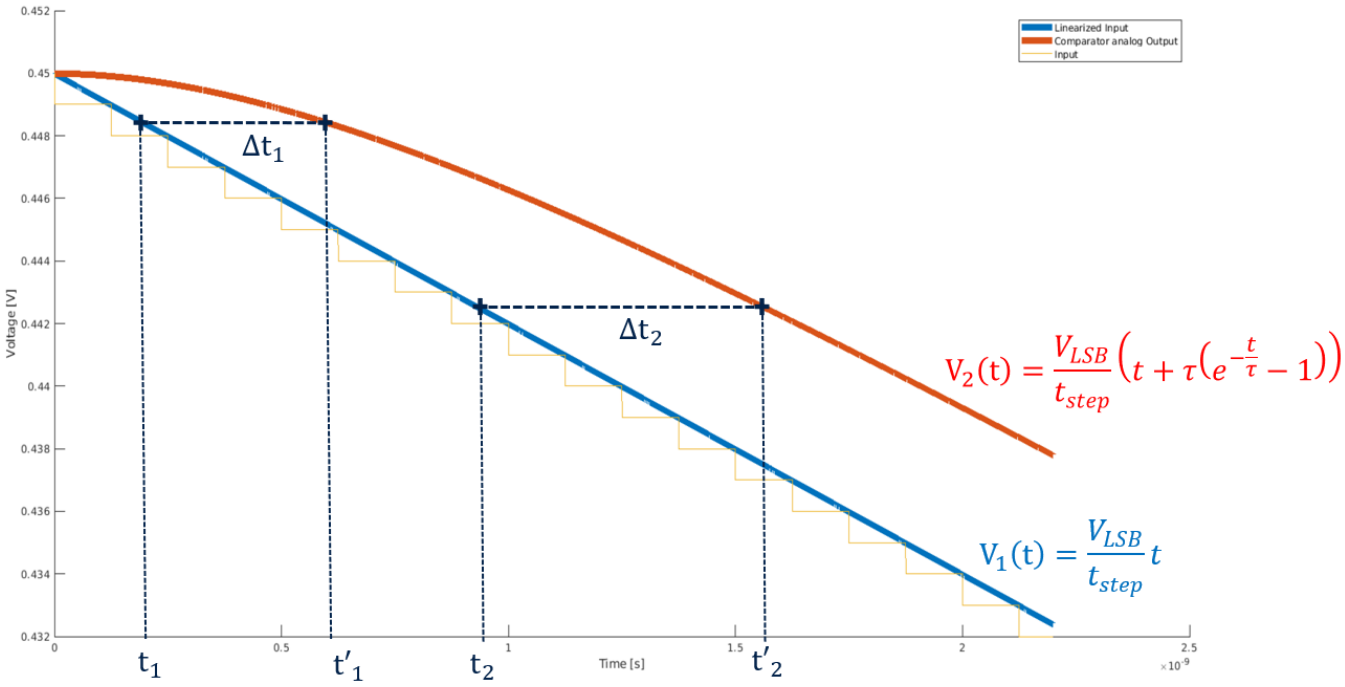

Figure 90 - Linearized model transient simulation

The actually observed transitions are quantized by the delay line, and the possible observed values of t'_1 representing the cross time of the comparator output are multiples of the unit delay t_{step} of the delay line. A corrected output code can be computed by subtracting a quantized version of the delay given by (5.6):

$$C_C = C - \left(\frac{\tau}{t_{step}}\left(1 - e^{-\frac{C.t_{step}}{\tau}}\right)\right) \tag{5.7}$$

Where C_C is the corrected output code, C is the output code with latency and t_{step} is the unit time step of the ramp, here 50ps. However the corrected code is on continuous scale.

$$C_{Cq} = C - E\left(\frac{\tau}{t_{step}}\left(1 - e^{-\frac{C.t_{step}}{\tau}}\right)\right) \tag{5.8}$$

To produce a quantized output code, the integer part only of the correction has to be taken into account as shown in equation (5.8) where E is the function giving the integer part of the argument.

5.3.2 Model based output error correction

Figure 92 draws the equivalent output codes from Figure 90 transient simulation on full unsigned dynamic. The response for a 32 step ramp with 180MHz comparator bandwidth is computed. The correction given by equation (5.7) is then applied. The corrected code obtained with (5.7) are compared with ideal expected code also represented on Figure 92. This result shows that theoretically with only one parameter the distortion induced by the ramp starting response could be compensated without extra power

consumption on the CT-CMP. Figure 91 shows the same results with the quantized correction given by

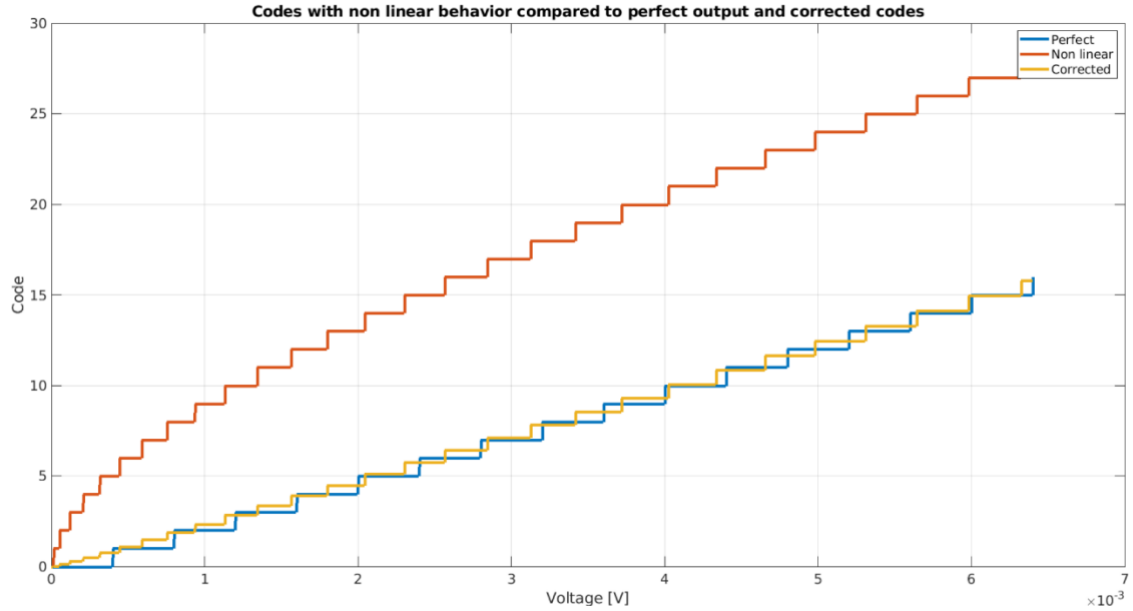

Figure 91 - Model correction for one sided sign output codes for 180MHz of f_(-3dB)

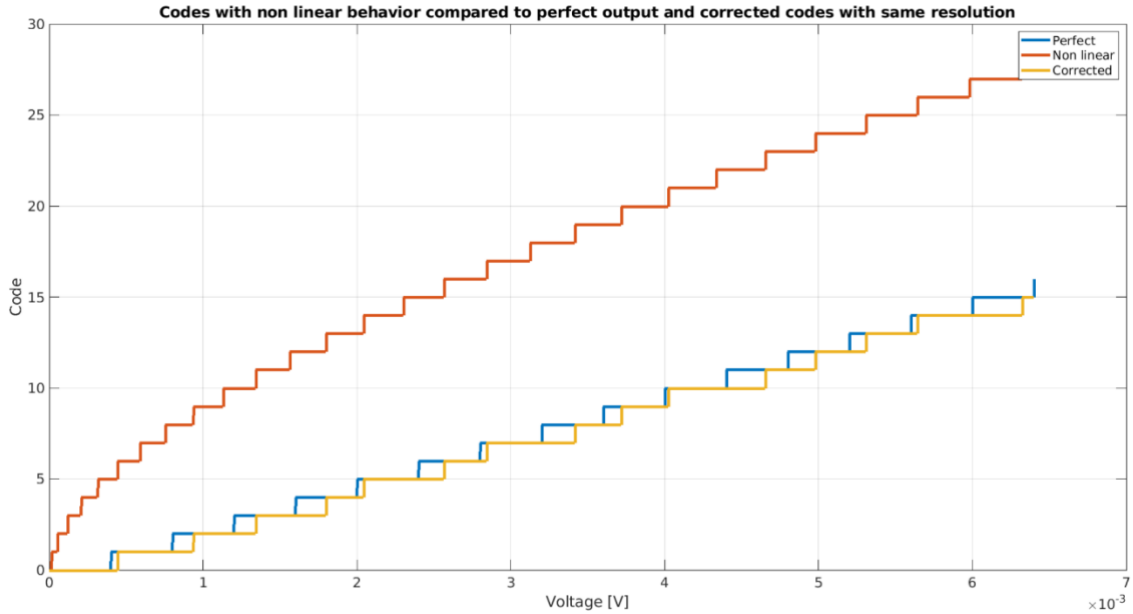

Figure 92 - Model correction for one sided sign output codes for 180MHz of f_(-3dB) [quantized correction]

equation (5.8).

A difference of 1 LSB appears between the ideal and the corrected quantized code. This is due to the fact that the transition times are not aligned with the LSB steps of the input signal due to the time-varying delay. As seen in the previous section, the method consisting in adding additional steps at the

beginning of the ramp produces a similar result. However, the proposed correction avoids increase in conversion time and power consumption due to the additional steps at the beginning of the ramp

5.3.4 Validation of output error correction with simulated data

The method proposed in the previous subsection has been applied to the output data from the simulation described in section 5.2 with the correction from the theoretical model described in the previous subsection.

As can be seen from the results plotted in Figure 93, the proposed mix of compensation and correction shows efficient results. Even with a low bandwidth of 180MHz the codes corrected present DNL but no missing or jump of codes as before the correction. An optimization on corresponding algorithm in form of a lookup table could enhance the present DNL of the second stage.

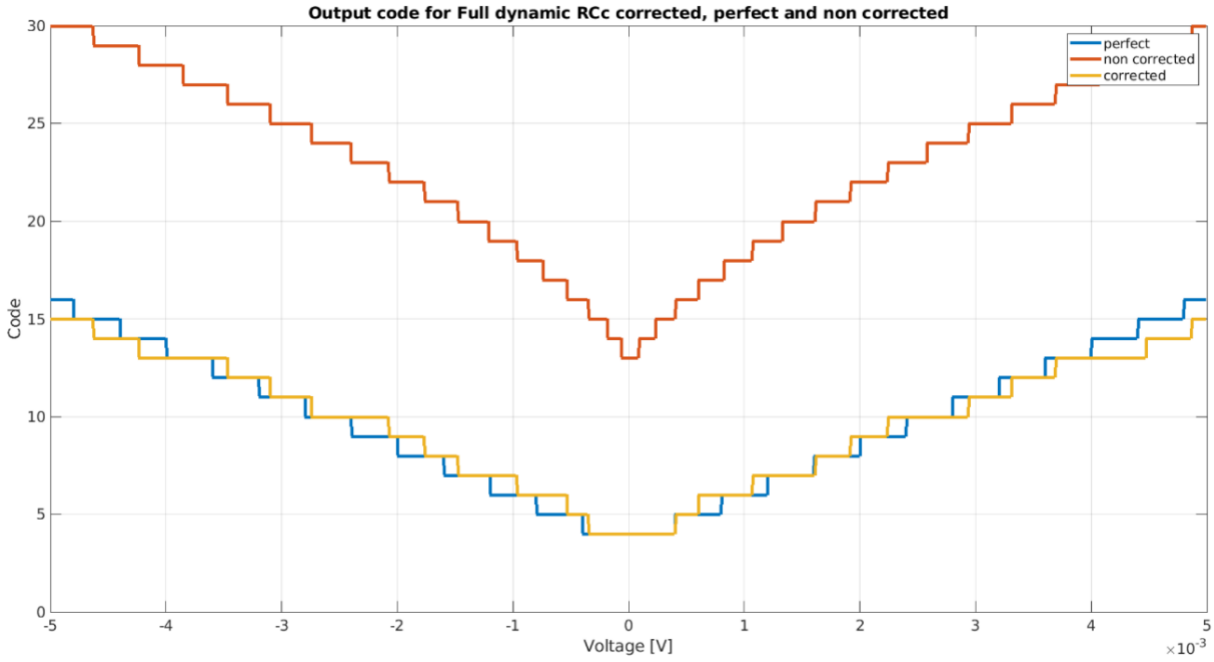

Figure 93 - Simulated results of RCc view with ramp extension and post digital correction compared to ideal output.

The proposed correction-compensation scheme achieves efficient results even in low value codes despite the bandwidth distortion. No extra time is required except ramp and delay line extension.

5.3.4 Practical implementation of digital post correction

Several approaches are possible to practically implement the proposed digital post correction. The most general approach would be to determine the parameter $\frac{\tau}{t_{step}}$ and apply the appropriate correction through the mathematical formula of equation (5.8). However, two difficulties arise: the first one is to determine the parameter $\frac{\tau}{t_{step}}$. This can be done by measuring the delay for a crossing point close to the

end of the ramp. The minimum length of the ramp for measuring $\frac{\tau}{t_{step}}$a with a 1 LSB precision can be obtained from equation (5.4) by setting $\varepsilon\ to\ 1$:

$$l_{min} = \frac{\tau}{t_{step}} * \ln\left(\frac{\tau}{t_{step}}\right) \tag{5.9}$$

Where l_{min} is the minimum number of steps for the ramp and τ the value of the time constant to be determined with 1 LSB precision. The maximum $\frac{\tau}{t_{step}}$ covered for reasonable ramp lengths is given in Table 16:

Table 16: Maximum value of measurable τ/t_step for ramps lengths of 16, 32 and 64 steps. From (5.9)

Number of useful ramp steps	**Total number of ramp steps**	**Maximum measurable $\frac{\tau}{t_{step}}$**
16	23	7
32	44	12
64	85	21

It can easily be seen that the required number of steps rapidly increases with the $\frac{\tau}{t_{step}}$ ratio and ratios beyond 20 appear to be impractical. The effective ramp length must also include a number of extra steps equal to the ratio $\frac{\tau}{t_{step}}$, the corresponding total number of ramp steps is also indicated in the table 1.

The second difficulty for the general correction approach is the implementation of the correction function given by (5.8) which requires a certain amount of computational effort. Further investigations are needed to quantify precisely this effort.

An alternative approach would be to remap delay line outputs directly either by bit-shifting or by using a lookup table to determine the delay offset to add to the code. This lookup table could either store a set of corrections chosen as a function of the measured $\frac{\tau}{t_{step}}$ or it could be generated on-chip from the measured $\frac{\tau}{t_{step}}$. Circuit level implementation has not been studied in detail in the framework of this thesis and is subject to future work.

5.5 Conclusion

This chapter presents an overview of nonlinear phenomena due to the limited bandwidth of the CT-CMP and their impact on the performance of the converter stage. Different technics to mitigate the non-linear effects of the converter latency are studied. A new method mixing an algorithmic correction of the errors at the starting of the ramp associated to an end-of-ramp extension of the ramp allows to correct the errors without increase of conversion time and minimal increase of power consumption.

Complete transistor level implementation of the proposed method will be the subject of future work.

Chapter 6

Conclusion and Future Work

6.1 CONCLUSION 145
6.2 FUTURE WORK 147

6.1 Conclusion

This research work has been focusing on new ADC architectures targeted for low power radio telecommunication such as Bluetooth and sub-GHz protocols. The system level consideration of ADC function in a reception chain has been presented. Then, the targeted specifications in coherence with STMicroelectronics requirements for next generation of products have been established. This work has been focusing on the proposition of a new ADC architecture able to address 64MS/s, 67dB of SNR while presenting less than 300µW of power consumption.

Considering these challenging specifications, the state of the art of the ADC has been studied through Boris Murmann's survey [11] and the most relevant ADC publications. In regards of silicon measurements published, classical ADC topologies such as flash, pipeline, $\Delta\Sigma$ and SAR have not been identified as able to reach the targeted performances of this work. On the other hand, hybrid structures mixing these classical topologies have been more present over the past years and show interesting performances. The challenges of these new hybrids have been studied through system considerations for system on chip implementation and the most relevant hybrids have been identified with SAR based topologies. SAR ADCs assisted with ramp [3] [69] present the most energy efficiency performances across targeted sampling rate and resolution. By using directly the voltage residue stored in capacitive DAC at the end of SAR conversion process, these hybrid topologies avoid the challenging and power consuming amplifier function used in pipeline based topologies. The residue is quantified thermometrically with ramp conversion associated to a counter implement with a delay line function. Most recent silicon implementation [73] present SAR assisted ADCs with ramp realization using a ring oscillator instead of a delay line to pilot ramp steps. This publication shows recent enthusiasm for this type of SAR based hybrid with important energy efficiency and a figure of merit of Schreier above 174 dB. The present thesis work proposes a new hybrid SAR based ADC using a bidirectional ramp to convert SAR residue. This new way to use ramps allows to divide the second stage conversion time by a factor 2, which also decreases the second stage power consumption. The proposed ADC architecture has been modeled with VerilogA description to validate system behavior and implement built-in calibration and correction scheme.

The system level description of different blocks paves the way to circuit realization while allowing performance evaluation based on behavioral description. A built-in calibration scheme and dedicated calibration hardware proposed in this work allows coherent sizing of the different blocks of the ADC. Global system simulations show achievable performances with realistic block performances and allows to extrapolate power consumption from state of the art publications [3].

The second stage used in the proposed hybrid SAR assisted bidirectional digital slope has been partially refined through the design and layout of the continuous time comparator. This block represents the most critical block of the second stage to reach high speed and linearity with low noise and power consumption. The proposed design of the CT-CMP shows the impact of bandwidth on linearity and latency seen in the second stage conversion. Post layout simulations taking parasitic extraction into account underline the challenge to achieve sufficient performances on advanced technology nodes while maintaining low power consumption. A digital post correction is then proposed to address linearization with minimal extra power consumption.

From the writing of this thesis, updated bibliography [12] shows that other propositions of SAR assisted with ramp have been published. H. Zhao et al. proposed in 2022 a second stage based on ring oscillator delay line [73]. Two pipelined second stages used in a ping pong switching scheme allows this proposition to reach 260MS/s with a SAR assisted digital slope topology. In 2023 a SAR assisted with VTC based ramp proposed also ping pong scheme with pipelined second stages using a dynamic amplifier to relax the second stage conversion [77]. Nevertheless, This simulated architecture targeted for 400MS/s presents important power consumption above 9mW. With an updated version of Table 9 presented in Chapter 3, Table 17 presents comparison with updated state of the art.

Table 17 - Summarize of simulated model performance compared to updated state of the art

	This Model [86]	SAR - VTC [69]	Monotonic DS [3]	Pipelined SAR - Ring TDC [73]	SAR - VTC [77]
Techno	**18nm (target)**	65nm	28nm	22nm	28nm (simulated)
Year	**2022**	2019	2016	2022	2023
Resolution [bits]	**12**	13	12	12	12
Sample rate [MS/s]	**64**	20	100	260	400
SNDR [dB]	**67.12***	71.5	65.67	63.5	63.3
Csample [pF]	**0.615**	4	0.9	1.2	1.9
Noise CT-CMP [μV_{RMS}]	**157**	45.6	150	--	--
Consumption [µW]	**204****	82	350	970	9600
2nd stage common mode variation	$\pm$**0.5 LSB**	--	$\geq -64LSB$	--	--
$FOM_{Schreier}$ [dB]	**179.1****	182.4	177.2	171.8	166.49

* Simulated with noise, offset and mismatch models
** Extrapolated from Monotonic DS measurements

6.2 Future Work

From the work presented in this thesis, some path should be followed to push further the development and efficiency of the proposed SAR assisted bidirectional digital slope ADC.

To improve the proposed solution and its integration in a global system on chip, the voltage references must be designed and sized coherently with the need of the ADC conversion process. To dig further in the power efficiency of the second stage, an unexplored way could be to address the offset correction scheme to maximize CT-CMP performances. The proposed offset correction addresses systematic CT-CMP offset considering the amplifier and the output inverter function without distinction. This makes the amplifier bias dependent on the output inverter threshold which can decrease the CT-CMP performances as seen in chapter 4. The bandwidth of the comparator can then be affected which impacts the whole second stage conversion. Instead, the offset calibration could be more precise with a calibration through the inverter threshold trimming which could be achieved in the FD-SOI technology through back gate control. On the other hand, a post digital correction as discussed in chapter 5 guarantees more reliable performances by allowing more bandwidth dispersion in the CT-CMP performances. The proposed post correction scheme should be implemented with a reliable bandwidth measurement technic which could be based on foreground measurement as for the offset measurements. The delay line used to quantify ramp steps could be implemented with a ring oscillator as proposed in [73] to address time step matching and PVT reliability in the time quantization. Back-gate biasing could again offer the possibility to track PVT variations if necessary.

Finally, the ultimate goal is to design the whole ADC with an efficient correction scheme to guarantee the energy efficiency as well as the industrial robustness of the architecture. The proposed architecture could also benefit from interpolation in the second stage [3] [73], not discussed in this work, to address higher resolution performances.

This new SAR assisted bidirectional digital slope topology could then be used in higher sampling rate or higher resolution applications while maintaining high energy efficiency.

Bibliography

[1] STMicroelectronics, «Low data rate, low power sub-1GHz transceiver, SPIRIT1 datasheet,» https://www.st.com/resource/en/datasheet/spirit1.pdf, August 2021.

[2] STMicroelectronics, «Bluetooth Low Energy wireless system-on-chip, BlueNRG-2 datasheet,» https://www.st.com/resource/en/datasheet/bluenrg-2.pdf, September 2021.

[3] C. C. Liu, M. C. Huang et Y. H. Tu, «A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC,» IEEE Journal of Solid-State Circuits, 2016.

[4] W. Sheng, A. Emira et E. Sanchez-Sinencio, «"CMOS RF receiver system design: a systematic approach,» IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 53, no. 5, pp. 1023-1034, 2006.

[5] A. Hu, D. Liu, Z. Jin, C. Zhang, K. Zhang et L. Liu, «RF Transceiver System Design: From Protocols to Specifications,» IEEE 13th International Conference on ASIC (ASICON), Chongqing, China, 2019.

[6] J. Mitola, «Software radios: Survey, critical evaluation and future directions,» IEEE Aerospace and Electronic Systems Magazine, vol. 8, no. 4, pp. 25-36, April 1993.

[7] K. S. Shanmugan, «Digital and Analog Communication Systems.,» New York : Wiley, 1979, pp. 277–297.

[8] J. Crols et M. S. J. Steyaert, «Low-IF topologies for high-performance analog front ends of fully integrated receivers,» in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998.

[9] R. M. P. H. A. v. R. Wei Deng, «An Alternative Design Flow for Receiver Performance Optimization,» IEEE Radio and Wireless Symposium, 2008.

[10] G. C. Temes, R. Schreier et S. Pavan, Understanding Delta-Sigma Data Converters, IEEE Press Series on Microelectronic Systems, 2017.

[11] B. Murmann, «ADC Performance Survey 1997-2020,» [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html..

[12] B. Murmann, «ADC Performance Survey 1997-2023,» [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html..

[13] R. v. d. Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, Springer, 2003.

[14] P. Vorenkamp et R. Roovers, «A 12 b 50 M sample/s cascaded folding and interpolating ADC,» IEEE International Solids-State Circuits Conference, 1997.

[15] H. Pan et e. al., «A 3.3-V 12b 50-MS/s A/D Converter in 0.6-µm CMOS with over 80-dB SFDR,» chez *Analog Circuit Design*, Springer, 2000, pp. 47-57.

[16] S. Zhu et e. al., «A 2GS/s 8b flash ADC based on remainder number system in 65nm CMOS,» Symposium on VLSI Circuits, Kyoto, Japan, 2017.

[17] H. Inose, Y. Yasuda et J. Murakami, «A Telemetering System by Code Modulation - Δ-ΣModulation,» IRE Transactions on Space Electronics and Telemetry, vol. SET-8, no. 3, pp. 204-209, Sept. 1962.

[18] S. Hein et A. Zakhor, «On the stability of sigma delta modulators,» IEEE Transactions on Signal Processing, vol. 41, no. 7, pp. 2322–2348, 1993.

[19] T. Oh, N. Maghari et U. -K. Moon, «A 5MHz BW 70.7dB SNDR noise-shaped two-step quantizer based ΔΣ ADC,,» 2012 Symposium on VLSI Circuits (VLSIC), Honolulu, HI, USA, , 2012.

[20] B. Boser et B. Wooley, «The design of sigma-delta modulation analog-to-digital converters,» IEEE Journal of Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

[21] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. D. Muro et S. W. Harston, «A cascaded sigmadelta pipeline a/d converter with 1.25 mhz signal bandwidth and 89 db snr,» IEEE Journal of Solid-State Circuits, vol. 32, no. 12, pp. 1896–1906, 1997.

[22] T. C. Leslie et B. Singh, «An improved sigma-delta modulator architecture,» IEEE International Symposium on Circuits and Systems, New Orleans, LA, USA, 1990.

[23] -C. S. Lee, B. Elies et Y. Chiu, «An 85dB SFDR 67dB SNDR 8OSR 240MS/s ΔΣ ADC with nonlinear memory error calibration,» Symposium on VLSI Circuits (VLSIC), Honolulu, HI, USA, 2012.

[24] L. J. Breems, E. J. van de Zwan, E. C. Dijkmans et J. H. Huijsing, «A 1.8 mW CMOS ΣΔ modulator with integrated mixer for A/D conversion of IF signals,» IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition, San Francisco, CA, USA, 1999.

[25] R. Kaald, T. Eggen et T. Ytterdal, «A 1 MHz BW 34.2 fJ/step Continuous Time Delta Sigma Modulator With an Integrated Mixer for Cardiac Ultrasound,» IEEE Transactions on Biomedical Circuits and Systems, vol. 11, 2017.

[26] R. Schreier et B. Zhang, «Delta-sigma modulators employing continuous-time circuitry,,» IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 43, no. 4, pp. 324-332, 1996.

[27] S. Chiang, H. Sun et B. Razavi, «A 10-Bit 800-MHz 19-mW CMOS ADC,» IEEE Journal of Solid-State Circuits, vol. 49, 2014.

[28] Z. Zheng et e. al., «16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation,» 2020, IEEE International Solid- State Circuits Conference - (ISSCC).

[29] H. Venkatram et e. al., «A 48 fJ/CS, 74 dB SNDR, 87 dB SFDR, 85 dB THD, 30 MS/s pipelined ADC using hybrid dynamic amplifier,» Symposium on VLSI Circuits Digest of Technical Papers, Honolulu, 2014.

[30] B. Hershberg, N. Markulic, J. Lagos, E. Martens, D. Dermit et J. Craninckx, «A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm,» IEEE Symposium on VLSI Circuits, Honolulu, 2020.

[31] F. Rarbi, «Conception d'un convertisseur analogique numérique pipeline de grande dynamique et de faible consommation pour le codage des signaux de détecteurs à forte granularité (Ph.D),» Université de Grenoble, Institu Polytechnique de Grenoble, Grenoble, France, 2010.

[32] R. E. Rad et e. al., «A Low Power 12-Bit Pipeline ADC with 40 MS/s using a Modified OP-AMP,,» International Conference on Electronics, Information, and Communication (ICEIC), 2020.

[33] R. Sehgal, F. Van Der Goes et K. Bult, «A 13-mW 64-dB SNDR 280-MS/s Pipelined ADC Using Linearized Integrating Amplifiers,,» IEEE Journal of Solid-State Circuits, vol. 53, no. 7, pp. 1878-1888, 2018.

[34] S. Lee., A. P. Chandrakasan et H. -S. Lee, «A 12 b 5-to-50 MS/s 0.5-to-1 V Voltage Scalable Zero-Crossing Based Pipelined ADC,,» IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1603-1614, 2012.

[35] J. L. McCreary et P. R. Gray, «All-MOS charge redistribution analog-to-digital conversion techniques. I,» IEEE Journal of Solid-State Circuits, vol. 10, no. 6, pp. 371-379, 1975.

[36] J. Shen, A. Shikata, A. Liu et F. Chalifoux, «A 12-Bit 31.1UW 1MS/S SAR ADC with On-Chip Input-Signal-Independent Calibration Achieving 100.4DB SFDR Using 256FF Sampling Capacitance,,» IEEE Symposium on VLSI Circuits, Honolulu, 2018.

[37] Y. Zhu, C. -H. Chan, U. -F. Chio et S. -W. Sin, «A voltage feedback charge compensation technique for split DAC architecture in SAR ADCs,» IEEE International Symposium on Circuits and Systems (ISCAS), Paris, France, 2010.

[38] X. Yue, «Determining the reliable minimum unit capacitance for the DAC capacitor array of SAR ADCs,,» Microelectronics Journal, Volume 44, Issue 6, Pages 473-478, 2013.

[39] Z. Li, Y. Lu et T. Mo, «Calibration for split capacitor DAC in SAR ADC,» IEEE 10th International Conference on ASIC, 2013.

[40] N. Collins, A. Tamez, L. Jie, J. Pernillo et M. P. Flynn, «A Mismatch-Immune 12-Bit SAR ADC With Completely Reconfigurable Capacitor DAC,,» IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 11, pp. 1589-1593, 2018.

[41] C. Chan et e. al., «16.4 A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration,» IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, 2017.

[42] K. Choo, H. An, D. Sylvester et D. Blaauw, «27.2 14.1-ENOB 184.9dB-FoM Capacitor-Array-Assisted Cascaded Charge-Injection SAR ADC,» IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, 2021.

[43] J. Liu, X. Tang, W. Zhao, L. Shen et N. Sun, «16.5 A 13b 0.005mm2 40MS/s SAR ADC with kT/C Noise Cancellation,» IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco,

2020.

[44] M. v. Elzakker, E. v. Tujil, P. Geraedts et D. Schinkel, «A 10-bit Charge-Redistribution ADC Consuming 1.9 µ W at 1 MS/s,» IEEE Journal of Solid-State Circuits, vol. 45, no. 5, pp. 1007-1015, 2010.

[45] D. Schinkel, E. Mensink, E. Klumperink, v. E. Tujil et B. Nauta, «A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time,» IEEE International Solid-State Circuits Conference. Digest of Technical Papers,, 2007.

[46] B. Razavi, «The StrongARM Latch [A Circuit for All Seasons],» IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, 2015.

[47] H. S. Bindra, C. E. Lokin, D. Schinkel, A. Annema et B. Nauta, «A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise,» IEEE Journal of Solid-State Circuits, 2018.

[48] H. S. Bindra, A. Annema, S. Louwsma et B. Nauta, «A 0.2 - 8 MS/s 10b flexible SAR ADC achieving 0.35 - 2.5 fJ/conv-step and using self-quenched dynamic bias comparator,» Symposium on VLSI Circuits, Kyoto, 2019.

[49] P. Harpe, «Successive Approximation Analog-to-Digital Converters: Improving Power Efficiency and Conversion Speed,» IEEE Solid-State Circuits Magazine, vol. 8, 2016.

[50] P. Harpe, Y. Zhang, G. Dolmans, K. Philips et H. De Groot, «A 7-to-10b 0-to-4MS/s flexible SAR ADC with 6.5-to-16fJ/conversion-step,» IEEE International Solid-State Circuits Conference, San Francisco, 2012.

[51] S. Sunny, Y. Chen et C. C. Boon, «A 4.06 mW 10-bit 150 MS/s SAR ADC With 1.5-bit/cycle Operation for Medical Imaging Applications,» IEEE Sensors Journal, vol. 18, 2018.

[52] S. Dong. et C. Liu, «A Two-Step Single-Side Capacitor-Reversal High-Efficiency Switching Scheme for SAR ADCs,» 7th International Conference on Integrated Circuits and Microsystems (ICICM), Xi'an, 2022.

[53] C. C. Liu, S. Chang, G. Huang, Y. Lin et C. Huang, «A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18µm CMOS,» Symposium on VLSI Circuits, Honolulu, 2010.

[54] A. ElShater et e. al., «A 10mW 16b 15MS/s Two-Step SAR ADC with 95dB DR,» IEEE International Solid-State Circuits Conference, 2019.

[55] M. J. Seo, Y. D. Kim, J. H. Chung et S. T. Ryu, «A 40nm CMOS 12b 200MS/s Single-amplifier Dual-residue Pipelined-SAR ADC,» Symposium on VLSI Circuits, Kyoto, 2019.

[56] H. Yoon, T. Kim, Y. Kwon et Y. Chae, «A 50 MS/s 65 dB-SNDR Pipelined SAR ADC using Capacitively Degenerated Two-Stage Dynamic Amplifier,» IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, 2022.

[57] C. K. Hsu et N. Sun, «A 75.8dB-SNDR Pipeline SAR ADC with 2nd-order Interstage Gain Error Shaping,» Symposium on VLSI Circuits, Kyoto, 2019.

[58] T. C. Hung, J. C. Wang et T. H. Kuo, «16.4 A Calibration-Free 71.7dB SNDR 100MS/s 0.7mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme,» IEEE International Solid- State Circuits Conference - (ISSCC), 2020.

[59] H. Huang, S. Sarkar, B. Elies et Y. Chiu, «A 12b 330MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation,» IEEE International Solid-State Circuits Conference (ISSCC), 2017.

[60] Y. Lyu et F. Tavernier, «A 1 GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9 dB FoMS,» IEEE Symposium on VLSI Circuits, 2020.

[61] P. Harpe, H. Li et Y. Shen, «Low-power SAR ADCs: trends, examples and future,» IEEE 45th European Solid State Circuits Conference (ESSCIRC), 2019.

[62] J. A. Fredenburg et M. P. Flynn, «A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC,» IEEE Journal of Solid-State Circuits, 2012.

[63] Y. S. Shu, L. T. Kuo et T. Y. Lo, «An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS,» IEEE Journal of Solid-State Circuits, 2016.

[64] M. Miyahara et A. Matsuzawa, «An 84 dB dynamic range 62.5–625 kHz bandwidth clock-scalable noise-shaping SAR ADC with open-loop integrator using dynamic amplifier,» IEEE Custom Integrated Circuits Conference (CICC), 2017.

[65] Z. Chen, M. Miyahara et A. Matsuzawa, «A 9.35-ENOB, 14.8 fJ/conv.-step fully-passive noise-shaping SAR ADC,» Symposium on VLSI Circuits (VLSI Circuits), 2015.

[66] S. Li, B. Qiao, M. Gandara, D. Z. Pan et N. Sun, «A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure,» IEEE Journal of Solid-State Circuits, 2018.

[67] Y. Z. Lin, C. Y. Lin, S. C. Tsou, C. H. Tsai et C. H. Lu, «A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET,» IEEE International Symposium on Circuits and Systems, 2019.

[68] Y. Z. Lin, C. H. Tsai, S. C. Tsou, R. X. Chu et C. H. Lu, «A 2.4-mW 25-MHz BW 300-MS/s Passive Noise Shaping SAR ADC with Noise Quantizer Technique in 14-nm CMOS,» IEEE Symposium on VLSI Circuits, 2017.

[69] M. Zang, C. H. Chan, Y. Zhu et R. P. Martins, «A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques,» IEEE Journal of Solid-State Circuits, 2019.

[70] C. C. Liu, S. J. Chang, G. Y. Huang et Y. Z. Lin, «A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure,» IEEE Journal of Solid-State Circuits, 2010.

[71] P. J. A. Harpe et e. al, «A 26 µW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios,» IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 7,, 2011.

[72] Y. -H. Chung, C. -W. Yen et C. -H. Tsai, A 12-bit 1-MS/s 26-µW SAR ADC for Sensor, Physical Sciences Reviews, 2018.

[73] H. Zhao et F. F. Dai, «A 0.97mW 260MS/s 12b Pipelined-SAR ADC with Ring-TDC-Based Fine Quantizer for PVT Robust Automatic Cross-Domain Scale Alignment,» IEEE International Solid-State Circuits Conference (ISSCC), 2022.

[74] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, Inc., USA., 2000.

[75] A. Cros et e. al., Analysis of process impact on local variability thanks to addressable transistors arrays, International Conference on Microelectronic Test Structures (ICMTS), 2014.

[76] H. Park, C. Yu, H. Kim, Y. Roh et J. Burm, «"Low Power CMOS Image Sensors Using Two Step Single Slope ADC With Bandwidth-Limited Comparators & Voltage Range Extended Ramp Generator for Battery-Limited Application,» *IEEE Sensors Journal*, vol. 20, pp. 2831-2838, 2020.

[77] Y. Zhao, Y. Xiang, F. Ye et J. Ren, «A 400-MS/s 12-bit Voltage-Time Hybrid ADC with a Ping-Pong SAR TDC for Speed Enhancement,» IEEE International Symposium on Circuits and Systems (ISCAS), 2023.

[78] D. Zhang, C. Svensson et A. Alvandpour, «Power consumption bounds for SAR ADCs,» European Conference on Circuit Theory and Design (ECCTD), 2011.

[79] Z. Su, H. Wang, H. Zhao, Z. Chen, Y. Wang et F. F. Dai, «A 280MS/s 12b SAR-Assisted Hybrid ADC with Time Domain Sub-Range Quantizer in 45nm CMOS,» IEEE Custom Integrated Circuits Conference (CICC), 2019.

[80] B. Razavi, «Design considerations for direct-conversion receivers,» in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 6, pp. 428-435, June 1997.

[81] F. Rarbi, D. Dzahini et L. Gallin-Martel, «A Power Efficient 12-bit and 25-MS/s Pipelined ADC for the ILC/Ecal Integrated Readout,» IEEE Transactions on Nuclear Science, vol. 57, 2010.

[82] J. Liu, X. Tang, W. Zhao, L. Shen et N. Sun, «A 13b 0.005mm2 40MS/s SAR ADC with kT/C Noise Cancellation,» IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, 2020.

[83] B. P. Ginsburg et A. P. Chandrakasan, «An energy-efficient charge recycling approach for a SAR converter with capacitive DAC,» IEEE International Symposium on Circuits and Systems, 2005.

[84] B. P. Ginsburg et A. P. Chandrakasan, «500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC,» IEEE Journal of Solid-State Circuits, 2007.

[85] K. Choo, H. An, D. Sylvester et D. Blaauw, «14.1-ENOB 184.9dB-FoM Capacitor-Array-Assisted Cascaded Charge-Injection SAR ADC,» IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, 2021.

[86] J. -B. Casanova, D. Perrin, S. Nicolas et A. Kaiser, «A Very Low Power 12 bit 64-MS/s 2 step SAR Assisted Bidirectional Digital Slope ADC,» IEEE International Symposium on Circuits and Systems (ISCAS), 2023.

[87] A. F. Bocco, F. Solis, B. T. Reyes et M. R. Hueda, «Noise and Energy Consumption Analysis of SAR and SAR-Pipelined ADCs,» Argentine Conference on Electronics (CAE), 2022.