# Development of FETs based on ultra-wide band gap materials for high voltage power electronics

# Développement de FET basés sur des matériaux à bande interdite ultra-large pour l'électronique de puissance haute tension

## Thèse

présentée à l'Université de Lille, faculté des Sciences et Technologies Institut d'Electronique, de Microélectronique et de Nanotechnologies (IEMN) UMR CNRS 8520 par

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# *Table of Contents*

# *Abstract*

Wide Bandgap Semiconductors (WBG) such as Silicon Carbide (SiC) and Gallium Nitride (GaN) show superior material properties to Silicon. However, the even wider bandgap material or dielectric such as Aluminium Gallium Nitride (AlGaN) or Aluminium Nitride (AlN) material system gives the flexibility of creating heterojunctions while dramatically broadening the device design space for medium/high power conversion systems. This thesis will focus on the demonstration of Ultrawide Bandgap (UWBG) semiconductors for developing high-voltage Field-Effect Transistors (FETs). In this context, an approach based on downsizing GaN channel thickness grown on bulk AlN substrates has been developed. The evolution of on-state current density and breakdown voltage has been realized with different GaN channel thicknesses. A high AlN lateral breakdown field of up to 10 MV/cm has been experimentally demonstrated. On the other hand, the integration of bulk AlN substrates to current Silicon foundries is challenging. Thus, it can be said that " What can be done on Silicon, will be done on Silicon." Addressing this challenge, we took an approach toward the demonstration of novel AlGaN channel-based Heterostructure FETs (HFETs) on Silicon for high-voltage applications. The impact of Al composition in the barrier and channel layers on the electrical and thermal performance of various AlGaN/AlGaN HFETs has been studied. Later, we demonstrate robust AlGaN channel HFETs on bulk AlN suitable for extreme power electronics with more than 2 kV breakdown voltage. The major challenge for AlGaN-based HFETs is to develop ohmic contact to the channel addressing which we demonstrated high current density (> 0.2 A/mm) Al-rich AlGaN channel HFETs on Silicon with more than 4 MV/cm average transistor breakdown electric field. This ongoing development in AlGaN HFETs highlights a promising direction that potentially leads to more sustainable and efficient power electronic solutions with smaller device dimensions along with better high voltage/high-temperature operation capabilities.

# *Résumé*

Les semi-conducteurs à large bande interdite (WBG) tels que le carbure de silicium (SiC) et le nitrure de gallium (GaN) présentent des propriétés physiques supérieures à celles du silicium. Cependant, les matériaux ou diélectriques à bande interdite encore plus large, tels que le nitrure d'aluminium et de gallium (AlGaN) ou le nitrure d'aluminium (AlN), permettent de créer des hétérojonctions tout en élargissant considérablement les possibilités de conception des dispositifs pour les systèmes de conversion d'énergie à moyenne/haute puissance. Cette thèse se concentrera sur la démonstration de semi-conducteurs à bande passante ultra-large (UWBG) pour le développement de transistors à effet de champ (FET) à haute tension. Dans ce contexte, une approche basée sur la réduction de l'épaisseur du canal GaN a été développée sur des substrats d'AlN. L'évolution de la densité de courant à l'état passant et de la tension de claquage a été réalisée avec différentes épaisseurs de canaux GaN. Un champ de claquage latéral élevé de l'AlN allant jusqu'à 10 MV/cm a été démontré expérimentalement. D'autre part, l'intégration de substrats d'AlN dans les fonderies de silicium actuelles est un défi. On peut donc dire que "ce qui peut être fait sur le silicium sera fait sur le silicium". Pour relever ce défi, nous avons adopté une approche visant à démontrer de nouveaux HFET à base de canaux AlGaN sur substrat de silicium pour des applications à haute tension. L'impact de la composition en Al des couches de barrière et du canal sur les performances électriques et thermiques de divers HFET AlGaN/AlGaN a été étudié. Par la suite, nous avons démontré la robustesse des HFET à canal AlGaN sur AlN massif, appropriés à l'électronique de puissance en conditions extremes et une tension d'operation supérieure à 2 kV. Le principal défi pour les HFET à base d'AlGaN est de minimiser les résistances de contacts de source et de drain. Nous avons pu démontrer une densité de courant élevée (> 0,2 A/mm) ainsi que des transistors à canal AlGaN riche en Al sur substrat de silicium avec un champ électrique de claquage moyen supérieur à 4 MV/cm. Ces résultats mettent en evidence une approche prometteuse qui pourrait potentiellement conduire à des solutions pour une électronique de puissance plus durable et plus efficace avec des dimensions de dispositifs réduites ainsi que des capacités de fonctionnement à haute tension/haute temperature accrues.

# *List of Figures*

# *List of Tables*

# *General Introduction*

Worldwide electricity consumption is predicted to surpass 50 petawatt hours by 2050. The gradual decline in fossil fuel reserves and increase in CO emissions will eventually lead to the development of renewable and sustainable power generation. In this frame, the need for power conversion, transmission, and distribution will be essential, which can be achieved by developing efficient power electronics. Si-based MOSFETs and IGBTs were major electronic devices that initiated the development of power conversion systems. However, these devices' electrical losses and material-specific limitations will not meet future conversion efficiency demands.

Wide band gap (WBG) semiconductors with their superior material properties over conventional silicon devices offer even faster, powerful, and compact devices. In the last decade, GaN and SiC gained significant attention in the semiconductor industry for the development of commercial devices capable of withstanding high voltage (up to 1200 V), high current (up to 150 A), and high temperature with up to 99% efficiency. Despite the given advantages, these WBG semiconductors are limited by their critical breakdown field, which is less than 3 MV/cm. Moreover, SiC MOSFETs and IGBTs are almost 3 times more costly than their counterpart Si-IGBTs. As the WBG technology evolves, the scope for dramatic improvements lessens, leading to a plateau in high-voltage performance enhancements. This scenario has led to the exploration of ultra-wide-bandgap (UWBG) materials defined by a bandgap larger than 3.4 eV. The UWBG semiconductors AlGaN alloys can push the critical electric field up to 10-12 MV/cm by varying Al content and the polarization fields enable the development of heterostructures consisting of a two-dimensional electron gas (2DEG) at the AlGaN/AlGaN interface. Thus, AlGaN alloys might offer higher breakdown voltages surpassing the WBG semiconductor limitations enabling multiple kilo-volt device operation. This thesis aims to demonstrate the fabrication and characterization of novel AlGaN-channel based transistors for high-voltage applications.

This work has been carried out within several French National projects listed below:

- BREAkuP (n°ANR-17-CE05-00131) - ultra-wide Bandgaps for futuRE high-power electronic ApPlications. Within this project, we demonstrated the first series of GaN HEMTs fabricated on bulk AlN. This project was completed in collaboration with CNRS laboratories IEMN, CRHEA, and Institut Néel.
- HBV (n°IA-11-LABX-0014) – High Breakdown Voltage – This project aimed for the development of transistors delivering superior breakdown voltage by using UWBG semiconductors. A part of this project was performed in collaboration with IEMN, CRHEA, L2C, GREYC, and Néel.
- ACTION (n°ANR-22-CE05-0028) - novel AlGaN Channel Transistors for hIgh vOltage applicatioNs - targets the development of AlGaN channel transistors on large diameter Si substrates. This project is ongoing with collaborative partners IEMN, Néel, CRHEA, and industrial partner EasyGaN.

The organization of the thesis is divided into 3 chapters:

Chapter 1: This chapter starts with an introduction to power electronics and wide band gap semiconductors along with a brief history of power devices. Then, the material properties of GaN along with a detailed device fabrication process are explained including their associated challenges. A study based on GaN HEMTs is shown covered by an experiment based on silicon and AlN substrate to understand their impact on device electrical characteristics. Furthermore, we delve into the challenges, industrial prospects, and environmental impacts of GaN-based devices. Finally, with the introduction of AlGaN material properties, the state-of-the-art AlGaN channel devices are presented.

Chapter 2: We will demonstrate the benefits of bulk AlN for high-voltage power electronics with the introduction of a series of GaN HEMTs fabricated on bulk AlN substrates. This chapter will detail a study showing the impact of GaN channel thickness downscaling on the device performance and 2-DEG properties. Moreover, electric field imaging of GaN channel MISHEMTs is discussed to evaluate the electrical breakdown phenomena.

Chapter 3: This chapter focuses on the novel AlGaN channel HFETs and has been divided into several studies. Firstly, AlGaN-on-Si transistors with various Al compositions in the channel are explored along with their high-temperature operation to understand the

impact of Al in the channel. Then, extreme AlGaN-on-AlN power transistors have been fabricated resulting in high-voltage and high-temperature performance. Moreover, self-heating temperature measurements were also carried out by Raman spectroscopy to understand the evolution of channel temperatures. Finally, a study based on the development of ohmic contacts to the AlGaN channel has been demonstrated yielding in state-of-the-art device performance.

# *Chapter-01 Introduction*

With the advancements in the technological era and the rising energy consumption, the use of power semiconductors leads towards efficient power generation, conversion, transmission, and distribution. The power semiconductor industry has been dominated by silicon for decades but recent advancements in compound semiconductors are clearly changing the scenario. The discovery of III-Nitride compound semiconductors such as GaN and SiC due to their unique and superior material properties has revolutionized the recent power electronics industry. These WBG semiconductors offer the advantage of high-power efficiency along with reduced size and weight while delivering high power density.

This chapter will begin with an introduction to power electronics and their applications followed by an introduction to WBG semiconductor materials. Next, the aspects of energy consumption and the need for efficient power electronics will be presented followed by a glimpse of current semiconductor market trends. Furthermore, the III-Nitride materials will be discussed briefly along with their use in developing heterostructures field effect transistor (HFET) technology along with their merits and demerits. Finally, current state-of-the-art technology based on UWBG AlGaN will be shown concluding the aim of this thesis work.

## 1.1 Introduction to Power Electronics

Power electronics play a vital role in the efficient control, conversion, and conditioning of electricity in modern society influencing a wide range of applications. It all began with the idea of a simple switch to control the flow of current that aspired to become modern-day FETs. Power electronics involves semiconductor devices such as diodes, transistors (such as MOSFETs and IGBTs), and thyristors that can handle high voltages, and high currents along with faster switching. The development of any electronic system starts with the design and conception of a circuit followed by material growth and device nano-micro fabrication. The micro/nano devices are then assembled into application-specific integrated circuits to realize efficient transfer and control of power in various systems.

Until the early 20$^{th}$ century, bulky vacuum tubes controlled electrical signals with high power consumption. In 1925, physicist Julius E. Lilienfeld introduced the concept of field effect in semiconductors patented with a fascinating experiment to control the electric current based on a three-electrode structure. However, his attempts to develop a functional semiconductor device were not fruitful because of the limited resources. The foremost devices for solid-state power semiconductors were rectifiers made of copper oxide, which found use in the early versions of battery chargers and radio equipment power supplies. L.O. Grundahl and P. H. Geiger introduced these devices in 1927. In 1945, German physicist Heinrich Welker patented the junction field effect transistors (JFET) working on the principle of charge flow control in the depletion region. On December 27, 1947, John Bardeen and Walter Brattain successfully demonstrated the first bipolar point-contact transistor at Bell Laboratories in New Jersey. However, the first transistor was not ready for commercial applications. During this period, germanium was the desirable choice of material for semiconductor applications due to its low bandgap and high carrier mobility [1]. After several attempts to develop a functional FET, a bipolar junction transistor (BJT) was invented by Shockley in 1948. Simultaneously, in August 1948, German physicists Herbert Mataré and Heinrich Welker applied for a patent on an amplifier based on the minority carrier injection, which they called "*Transistron*" in Aulnay-sous-Bois, France [2]. The *Transistron* was developed independently of Bell laboratories in France and was later commercially developed for French telecommunication and military applications.

In 1948, based on his research on surface physics Bardeen secured a patent for an insulate-gate field effect transistor (IGFET) featuring an inversion layer crucial in confining the minority carriers, thus enhancing modulation and conductivity. Bardeen's patent and concept of the inversion layer are fundamental to the current complementary metal-oxide-semiconductor (CMOS) technology. In 1950, W. Shockley proposed a three terminal solid-state semiconductor device with alternating P-N-P-N layers called silicon-controlled rectifier (SCR) or thyristor. The three terminals are namely anode, cathode and gate. In 1952, R.N. Hall demonstrated first germanium power diode with impressive reverse blocking voltage of 200V and current rating of 35 A. The transistor applications began in many electronic devices replacing vacuum tubes by the early 1950s [3]. Later in 1956, the trio Bardeen, Brattain, and Shockley were honored with the Nobel Prize in Physics for their work on semiconductors and the discovery of the transistor effect. In the same year, General Electric commercially released the first thyristor devices. Silicon rectifiers, with their larger band gap, provided greater reverse voltage capacity and could operate at higher temperatures. By the late 1950s, alloy junctions had been developed that could handle up to 500 volts. The late 1950s also saw the combination of diffused junctions and mesa technology, a crucial step that later enabled reverse blocking capabilities of several kilovolts. By 1958, Jack Kilby at Texas Instruments showed the working example of an integrated circuit (IC) for which, he was awarded jointly the Nobel Prize in Physics in 2000.

In 1959, Mohamed Atalla and Dawon Kahng invented the highly scalable metal-oxide-semiconductor field effect transistor (MOSFET) which superseded the principle of both the BJT and JFET fabricated by growing an insulating silicon-oxide layer on semiconducting silicon. The first MOSFET was almost 100 times slower than contemporary BJTs but it was worthy for the ease of fabrication and its applications in IC. In 1961, the Gate Turn-Off Thyristor (GTO) marked a significant advancement in power electronics by combination of the fast-switching capabilities of a transistor with the low conduction losses characteristic of a SCR. In 1963, Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor Inc., California, developed CMOS Technology. Combining the logic of NMOS and PMOS processes and demonstrating its application as an inverter and ring oscillator, they demonstrated low standby power density and high switching power density that can be

realized in a circuit with a very high packing density enabling the integration of over 10,000 transistors into a single IC [3].

Following the introduction of the GTO, another major development occurred in 1964 with the creation of the TRIAC, or bidirectional AC switch, by General Electric. The TRIAC was primarily designed for 60 Hz applications, particularly in consumer lighting and motor speed control. Its bidirectional current flow capability made it an ideal component for controlling AC power where both positive and negative current flow needed to be managed. By the mid-1960s, mesa junctions had been optimized to theoretically allow for avalanche breakdown voltages up to 9000 V [4], [5]. Additionally, improvements in device packaging minimized thermal and mechanical stress on the chip, led to increased current handling capacities. Today, thyristors with a diameter of 77 mm are available, capable of sustaining continuous currents of 5000 A and reverse voltages of 3000 V with a maximum junction temperature of 125°C weighing almost up to 2 kg. However, the SCR needs an additional circuitry to reduce the anode-cathode current below the holding current to change the SCR from the conducting state to the blocking state. By 1970, power MOSFETs emerged featuring vertical structure. When compared with the BJT, MOSFET had the advantageous features of a high-input impedance, high switching speed, ease of paralleling, and a much superior safe operating area (SOA) making it attractive for computer and automotive electronics. Power MOSFETs were limited to 200V due to the drastic increase in on-resistance with the increasing blocking voltage; this hindered the progress of developing high current devices. To overcome this limitation and target higher voltage systems, a new class of power devices based upon the combination of BJT and MOS concept were developed called insulated-gate bipolar transistor (IGBT). By 1979, Jayant Baliga successfully developed the first IGBT at General Electric.

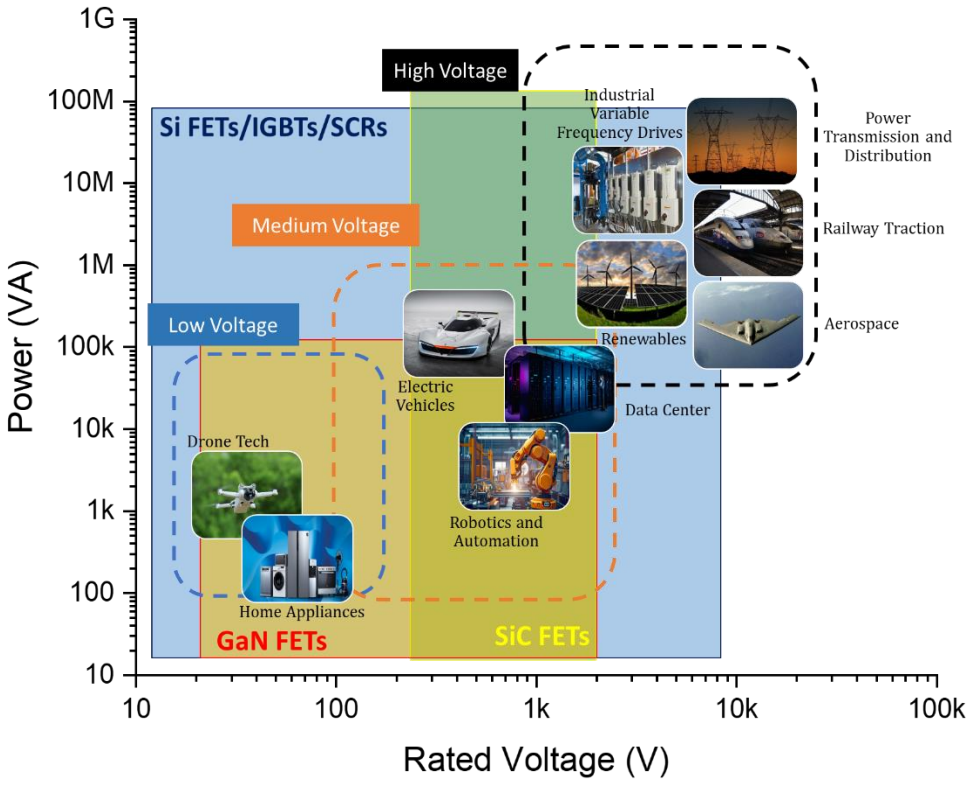



*Fig. 1. 1 Power semiconductor devices applications according to the voltage range and rated power*

The development of high-speed and compact computers began with the emergence of efficient microprocessors in the 1980's and the implementation of deep sub-micron CMOS technology. In 1983, Baliga et al. presented the results of insulated gate rectifier (IGR) suggesting suppression of a parasitic thyristors action and the rectifier was a clear representation of MOS gated bipolar transistor [6]. However, their switching speed was slow and the reverse biased SOA were small to replace BJT. To resolve this issue, Nakagawa et al. presented concept of non-latch-up 1200 V 75 A Bipolar MOSFET with large SOA [7]. Over the decades, MOSFETs and IGBTs emerged to be key component in power electronic systems with the development of innovative structures which evolved to produce high power density and lower die footprint sizes [8]–[10].

The applications of power electronic devices can be differentiated based on their rated voltage such as low voltage, medium voltage, and high voltage with their corresponding maximum voltage limited by 200 V, 1.2 kV, and more than 1.2 kV respectively. The various domains of applications are highlighted according to the rated voltage with their required

power rating as shown in *Fig. 1.1*. The various applications of power electronics can be described as follows:

1.) Renewable Energy Systems
    - DC-DC boost converter
    - Inverter
2.) Electric Vehicles (EVs)
    - Motor control unit
    - Inverter
    - Bidirectional AC-DC converter
    - LiDAR
3.) Consumer Electronics
    - Wireless chargers
    - Power adapters
4.) Power system
    - Flexible AC Transmission System (FACTS)
    - Power factor correction (PFC)
    - High Voltage Direct Current (HVDC) Transmission
    - Smart grid
5.) Aerospace and Defense
    - Satellite and aircraft systems
    - Radar systems
6.) Medical applications
    - X-Ray machines
    - MRI machines
    - CT scan
7.) Industrial applications
    - Variable frequency drive (VFD)
    - Automation systems
    - Uninterruptible power supply (UPS)

Silicon power devices cover the majority of power electronics applications from small ICs to bulky high-voltage converters. However, the evolution of modern-day power electronics has been significantly driven by advancements in material science with the introduction of WBG materials, such as GaN and SiC. Their high band gap (> 3 eV) and almost 10× higher electric field strength allows them to operate at much higher voltages with low on-resistances compared to Si devices. Moreover, the high electron mobility and saturation velocity allow the WBG FETs to operate at higher switching frequencies. Additionally, their high thermal conductivity enables high-temperature operation beyond the limits of Si. The material parameters for Si, GaN and SiC has been shown in *Fig. 1.2*

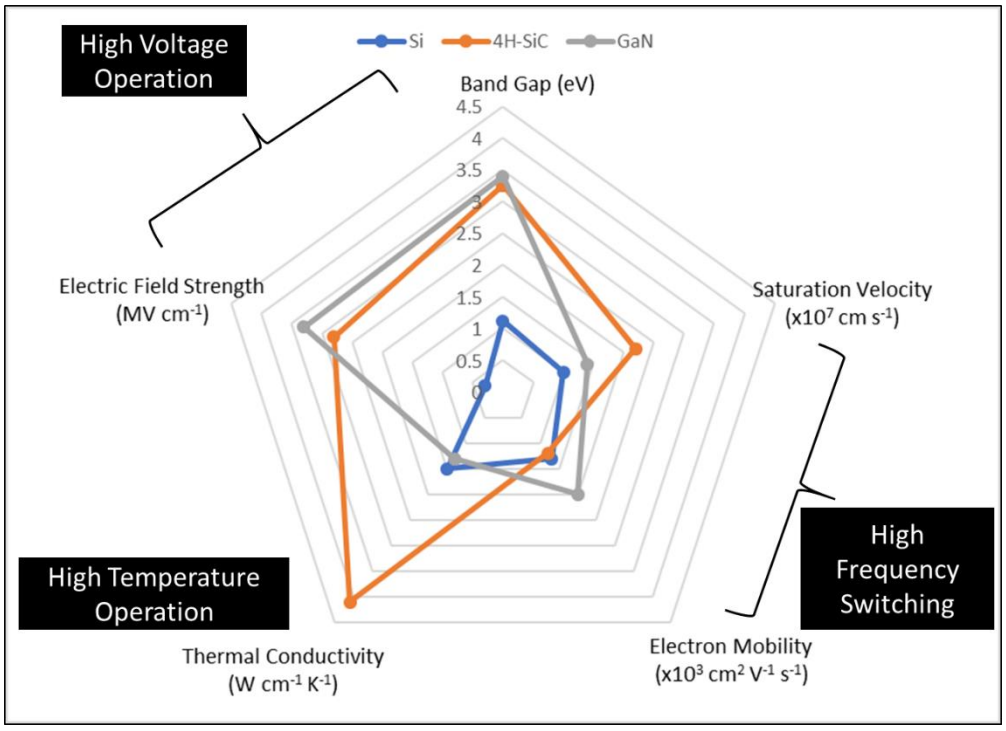



*Fig. 1. 2 Radar chart showing material properties of Si, GaN and SiC*

# 1.2 Gallium Nitride (GaN)

## 1.2.1 Crystal properties

The III-Nitride group shares three crystal structures: the wurtzite, zincblende, and rocksalt structures. Under ambient conditions, GaN shows a wurtzite structure ($P6_3mc$ – space group) defined by a hexagonal unit cell, resulting in two lattice constants, c and a. It consists of six atoms of each type. The structure is formed from two interlocking Hexagonal Close Packed (HCP) sublattices, with each lattice featuring a single type of atom offset along

the c-axis by 5/8 of the cell height. The wurtzite structure shows ABABAB type stacking sequence of closely packed diatomic planes in the {0001} direction. The structure consists of two interpenetrating face-centered cubic sublattices, offset by one-quarter of the distance along a body diagonal. Each atom in the structure may be viewed as positioned at the center of a tetrahedron, with its four nearest neighbors defining the four corners of the tetrahedron. Fig. 1.3 shows the crystal structure of GaN along with the crystal planes and their directions. The rocksalt (NaCl) structure can be induced in GaN under very high-pressure conditions around 50 GPa. The zinc blend structure has a cubic unit cell (F43m – space group) with the position of the atoms in the unit cell identical to the diamond crystal structure. However, the bandgap of cubic GaN is lower than wurtzite GaN despite of high electron mobility and can only be grown on (011) crystal planes of cubic Si [11]. The cubic GaN is a metastable phase whereas the wurtzite GaN is a stable phase [12]. Hence, wurtzite is the most commonly used GaN crystal structure suitable for power device fabrication. As shown in the figure, depending on the growth techniques, wurtzite GaN can be grown on a substrate starting from the N-face and ending at the Ga-face known as N-polar GaN. The GaN crystal starting from Ga-face and N-face on the surface is known to be Ga-polar or metal polar GaN. The latter is most widely used in the fabrication of HEMTs and HFETs since N-polar GaN deals with material growth and reliability related challenges.

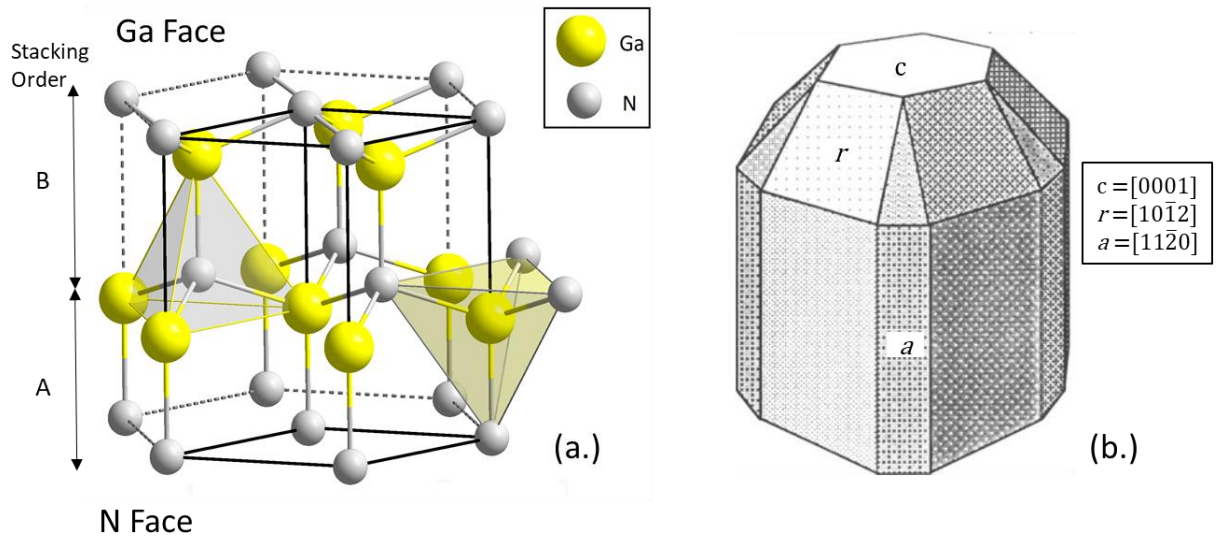



*Fig. 1. 3 Schematic view of GaN (a.) crystal structure (b.) crystal planes and direction in hexagonal symmetry*

The lattice parameters of GaN depends on the stoichiometry, defects and carrier concentration. The dependence of lattice parameter on temperature can be quantified by thermal expansion coefficient, defined by $\Delta a/a$. Measurements made over the temperature range of 300-900 K indicate the mean coefficient of thermal expansion of GaN in the c plane to be $\Delta a/a = 5.8\times10^{-6}\ K^{-1}$ [13]. GaN along the c-axis shows thermal conductivity up to 253 W/m. K as demonstrated by Shibata *et. al* verifying GaN as one of the promising materials for high-power switching [14].

GaN is an exceedingly stable compound and exhibits significant hardness. The room temperature hardness of bulk single-crystal GaN is 10.2 GPa and it shows a decrease in hardness at 1200° C temperature [15]. In the hexagonal wurtzite structure, GaN has a molecular weight of 83.727 gm/mol. At room temperature, the lattice parameters are $a_o$ = 3.1892± 0.0009 Å and $c_0$ = 5.1850± 0.0005 Å. The variability of the lattice constant in early versions of GaN can indeed be attributed to several factors including growth conditions, impurity concentrations, and film stoichiometry. The incorporation of impurities can lead to either contraction or expansion of lattice depending on their type. Different growth temperatures, pressures, and substrate materials can lead to variations in the lattice structure.

### 1.2.2 Epitaxy techniques

The first synthesis of GaN was made in the early 1930s however, due to limited material understanding it remained unexplored for several decades [16]. A major drawback of GaN is that native substrates are not yet available in large quantities and dimensions. This is, in part, due to the low solubility of nitrogen in Ga and the high vapor pressure of nitrogen on GaN. As a result, the bulk growth must resort to high temperatures and high pressures. Incorporating stoichiometric quantities of nitrogen into the film is indeed a major challenge in the growth of Group-III nitrides like GaN, AlN, etc. Achieving the right stoichiometry is crucial for the formation of high-quality nitride films, which directly affects the performance of GaN HEMTs. Substrate surface preparation is the foundation of achieving a high-quality epitaxy. The commonly used growth techniques include Hydride Vapor Phase Epitaxy (HVPE), Metal Organic Chemical Vapor Deposition (MOCVD), and Molecular Beam Epitaxy (MBE).

HVPE is a prominent growth technique used for the production of GaN crystals. HVPE involves the reaction of gaseous hydrogen chloride with liquid or solid gallium to form gallium chloride, which then reacts with ammonia to produce GaN. In this procedure, chloride gas undergoes a reaction with a source of gallium within a temperature range of 800-900°C, resulting in the formation of a gaseous phase within the source zone. Following this initial reaction, the gaseous product is then conveyed to a nitrogen-rich area within the deposition zone, where temperatures are elevated to 1000-1100°C [17]. It is in this environment that the product reacts further with nitrogen, leading to the crystallization of gallium nitride (GaN). HVPE is valued for its efficiency in producing large-area GaN substrates with good crystalline quality. The most significant advantages of HVPE growth include the atmospheric pressure condition and a high growth rate on the order of several hundreds of micrometers per hour [18].

In MOCVD, Trimethylgallium (TMGa) or Trimethylaluminum (TMAl) reacts with $NH_3$ on a 1000°C heated substrate. MOCVD is favored for its ability to precisely control the composition and thickness of the thin films, making it ideal for fabricating complex semiconductor structures with high purity and uniformity essential for HEMT devices. A typical range of growth temperatures involved in the MOCVD process is ~ 500 to 1200 °C. MOCVD growth can also be carried at either atmospheric pressure or low pressure ($10^{-2}$-$10^{-3}$ Torr) which eventually reduces the cost of maintenance. Additionally, growth rates up to 5 μm/h can be achieved [19]. However, the need for toxic gases and compounds increases the overall cost with the need for proper protection and exhaust systems.

In MBE, the thin films are grown by firing off metal atoms onto a heated substrate for reaction. MBE usually works in the ultra-high vacuum around $10^{-9}$ – $10^{-11}$ Torr pressures, due to which it is compatible with in-situ diagnostics such as Reflection High-Energy Electron Diffraction (RHEED), Auger electron spectrometry, etc. RHEED gun can keep track of the thickness on an atomic scale by employing various patterns on the surface of the substrate. Typically, 0.3-1 μm/h growth rates are employed along with variations in the nucleation and growth temperature to obtain high-quality thin films [20]. The typical growth temperatures in MBE are much lower as compared with MOCVD. All the heterostructures used in this thesis work are grown using the ammonia source MBE technique.

## 1.3 GaN HEMTs

### 1.3.1 History of HEMTs

The high electron mobility transistors (HEMTs) are field effect transistors having lateral architecture containing a 2-DEG at the interface of barrier and channel generated by a combination of polarization effects including spontaneous and piezoelectric polarization in the materials. In 1979, physicist Takashi Mimura, while working at Fujitsu, Japan, invented the HEMTs that use the field effect to control electrons at the interface of a single heterojunction. GaAs MOSFETs that could offer high-speed performance compared to Si MOSFETs motivated his research. Independently, in the same year Daniel Delagebeaudeuf and Tranc Nuyen filed a patent for a heterojunction field effect transistor (HFET) developed using GaAs/AlGaAs doped heterojunctions while working at Thomson-CSF in Paris, France [21]. In 1986, Fujitsu, Japan demonstrated GaAs/AlGaAs HEMT for high-performance very large-scale integration (VLSI) technology along with the self-alignment device fabrication [22]. By 1990, HEMTs based on GaAs/AlGaAs and AlInAs/GaInAs grown on InP substrates demonstrated high performances with their operation up to 95GHz showing great potential for developing millimeter-wave low-noise amplifiers, exhibiting world-record performances for three-terminal semiconductor devices [23]–[25]. However, the high performance of these devices is accompanied by challenges such as low breakdown voltage, issues of thermal dissipation, kink effects, surface degradation, contact degradation, device burnout, etc. [26]. In 1992, Asif Khan *et. al* observed and confirmed the presence of a 2-DEG in GaN/AlGaN heterojunction demonstrating its high electron mobility [27], [28]. A year later, they demonstrated the first operation of AlGaN/GaN HEMT grown on sapphire substrates, benchmarking the wide-bandgap material for power electronics [29].

### 1.3.2 Formation of 2-DEG

GaN HEMTs or heterojunction field effect transistors (HFETs) are derived from the formation of highly mobile 2-DEG at the heterojunction of AlGaN/GaN without any external doping. Firstly, there is a conduction band bending phenomenon in the AlGaN due to the internal polarization fields resulting in the accumulation of electrons at the interface. Secondly, due to fermi level alignment at the heterojunction, the electrons at the interface will form a 2-DEG [30]. The 2-DEG formation can be explained by the existing donor states on the surface of the AlGaN barrier [31]. The spontaneous ($P_{SP}$) polarization and piezoelectric ($P_{PZ}$) polarization generated in the heterostructure can be simplified with the total polarization ($P_{TOT}$) = $P_{SP}$ (AlGaN) - $P_{SP}$ (GaN) + $P_{PZ}$ (AlGaN), considering relaxed GaN channel. The total sheet charge density of 2-DEG can be given by:

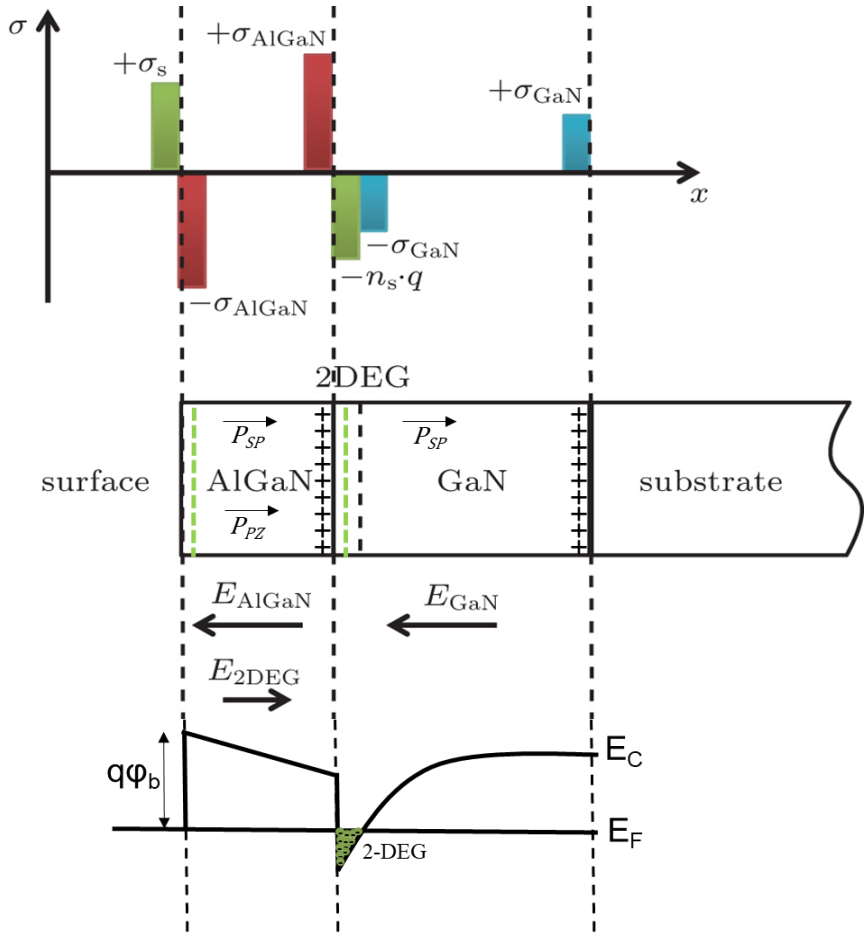



*Fig. 1. 4 Charge distribution profile along with conduction band diagram of an AlGaN/GaN heterostructure*

$$n_s = \frac{\sigma_{AlGaN}}{q} - \frac{\varepsilon}{q^2 d}\left(q\varphi_b + E_f - \Delta E_c\right) \qquad (1.1)$$

where $\sigma_{AlGaN}$ is the net polarization-induced charge density in the AlGaN layer, d is the thickness of the AlGaN layer, $n_s$ is the sheet density of 2-DEG, q is the electron charge, and ε is the dielectric constant of AlGaN, $\varphi_b$ is the surface barrier height, $E_f$ is the Fermi level position with respect to the GaN conduction-band edge at the AlGaN/GaN interface, and $\Delta E_c$ is the conduction band discontinuity between GaN and AlGaN as shown in Fig. 1.4. The 2-DEG thickness is estimated to be around 2-5 nm. As the thickness of the AlGaN layer is further increased, the 2-DEG density will tend to saturate approaching the value of total polarization-induced charge until the critical thickness after which the barrier tends towards relaxation. This total polarization-induced charge density can be controlled by varying the Al composition in the barrier [32]. The optimal range for the mole fraction in AlGaN/GaN structures is typically between 0.2 and 0.4 [33]. These values are ideal because they generate a substantial polarization charge, which is crucial for creating electrons in the 2-DEG. Moreover, they provide sufficient conduction band discontinuity at the AlGaN/GaN heterojunction, ensuring effective electron confinement. However, higher molar fractions can exacerbate thermal and lattice mismatches between AlGaN and GaN, leading to increased defect density and rougher interfaces affecting the overall performance of the device.

### 1.3.3 GaN HEMT Structure

The GaN HEMTs are usually fabricated with source/drain ohmic contacts to channel the flow of electrons in 2-DEG and Schottky gate contact to modulate the 2-DEG channel as shown in Fig. 1.5. The detailed explanation of GaN HEMT fabrication process and characterization techniques are described in the next section. The typical GaN HEMT structure can be exploited into various epi-layers described as follows from top to bottom:

I. **Cap:** The cap layer in HEMTs serves two critical functions that enhance the device's overall performance. Firstly, it reduces the remote Coulomb scattering of electrons in 2-DEG, which effectively enhances the channel mobility. This improvement in mobility is crucial for achieving faster electron transport and better device efficiency. Secondly, the cap plays a role in reducing the peak electric field at the drain-side gate edge, which contributes

to improved device breakdown voltage. This enhancement in breakdown voltage is vital for the robustness and reliability of the device, especially under high-voltage operations. Usually, the cap layer is made up of GaN or SiN.

II. **Barrier:** The barrier layer enables the formation of a 2-DEG channel at the AlGaN/GaN heterojunction. The thickness and Al content of the barrier will directly affect the 2-DEG properties and hence the transistor threshold voltage, which is tunable. Moreover, it improves the electron confinement in the channel and minimizes the leakage current. The barrier layer for the GaN channel is usually composed of compound semiconductors such as AlGaN, AlN, AlInN, InP, or InAlGaN [34]–[37].

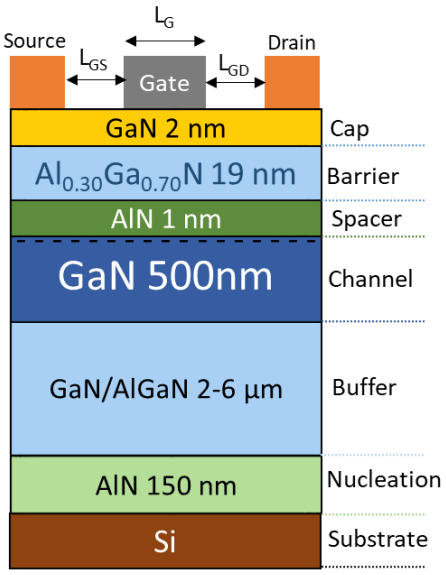



*Fig. 1. 5 Schematic cross-sectional diagram of AlGaN/GaN HEMTs*

III. **Channel:** The channel layer facilitates the control of 2-DEG charges by applying a voltage across source-drain contacts. The source-drain contact resistances and drift velocity of electrons flowing from source to drain (channel resistance) will largely determine the output performance of transistors. The thermal stability of the GaN channel allows the devices to operate at much higher temperatures compared to Si FETs.

IV. **Spacer:** The spacer layer enhances the 2-DEG properties and maintains high electron concentration. It reduces the scattering and electron trapping effects

at the AlGaN/GaN interface, reducing the current collapse and eventually improving the device's performance.

V. **Buffer:** The buffer layer is typically located between the substrate and active layers used to improve the quality of the GaN channel. It prevents the threading dislocations and defects propagating from the substrate towards the channel by burying the defects and bending the dislocations in its vicinity, preserving the quality of the channel. It also provides the electrical isolation of the active area of HEMTs from the substrate and prevents leakage currents. The buffer layer helps with strain management providing the lattice transition from substrate to channel and helps in improving the channel electron confinement. The controlled doping of buffer highly positively influences the device operation under high-stress conditions and improves device reliability and breakdown voltage. The buffer can be made up of various epitaxial configurations such as:

   a. **Superlattice buffer**: The typical superlattice configuration consists of alternating GaN/AlN layers of less than 20 nm thickness grown for around 4-6μm thickness eventually improving the strain relaxation in layers while providing high insulation and better 2-DEG confinement. They also reduces the dispersion and highly improves the device reliability [38], [39].
   b. **Step graded buffer:** The step-graded buffer layer is usually made up of multiple AlGaN layers stacked in decreasing Al content from the substrate. This allows the mitigation of defects and dislocations originating from the substrate [40].

VI. **Nucleation:** The nucleation layer is key to successful GaN epitaxy over variety of substrates. It acts as an intermediate layer to compensate for the lattice mismatch and thermal expansion coefficient difference between GaN channel and various substrates and facilitates the crack free growth of GaN. It acts as seed layer of buffer layers.

| Material | Cost per wafer ($) | Thermal Conductivity (W/m. K) | Thermal expansion coefficient ($10^{-6}$ $K^{-1}$) | Maximum Size Available (mm) | Critical Breakdown Field (MV/cm) |
|---|---|---|---|---|---|
| Si | 20-80 | 150 | 2.5 | 300 | 0.3 |
| Sapphire | 100-200 | 20-30 | 5-6 | 300 | 0.4 |
| SiC | 1300-1800 | 370 | 3 - 5 | 200 | 2-3 |
| Bulk GaN | 3000 | 230 | 3-4 | 100 | 2-3 |
| Bulk AlN | 5000 | 320 | 4.5 | 50 | 16 |

*Table 1. 1 Comparison of material properties, cost and availability for various substrates*

**VII.** **Substrate:** The choice of substrate material involves a trade-off between the performance, cost and manufacturing capability. The various substrates include Si, sapphire, SiC, bulk GaN and bulk AlN. SiC is widely used for RF applications due to its high thermal conductivity, enabling efficient high frequency switching. Moreover, bulk GaN and AlN are one the most suitable substrates for GaN HEMT epitaxy due to their low lattice mismatch with GaN combined with high thermal conductivity and exceptionally high breakdown field (up to 15 MV/cm) compared to Si (see table 1.1). Silicon remains the prior choice of substrate for industry in order to develop cost–effective electronics. However, it comes with challenges in thermal management and defect control. In this thesis work, HFETs have been fabricated based on an approach to create extreme BV device on AlN and on the contrary a cheaper counterpart based on silicon substrates aiming to overcome GaN-on-Si lateral device operating voltage limitations.

**VIII.** **Source/Drain Contacts:** The Source/Drain contacts are fabricated in order to obtain ohmic contacts to the 2-DEG and control the flow of electrons from source to drain. The schematic of typical contacts and the associated resistances are shown in Fig. 1.6. The contacts directly deposited on top of the barrier give a higher resistance path to the 2-DEG. This increases the on-state resistance that indeed lowers the performance of device and induces higher conduction losses. To overcome this issue, partial barrier etched contacts are performed under the source/drain region reducing the overall

contact resistance. Generally, Ti/Al/Ni/Au metal stack is used to fabricate source/drain ohmic contacts to GaN HEMTs.

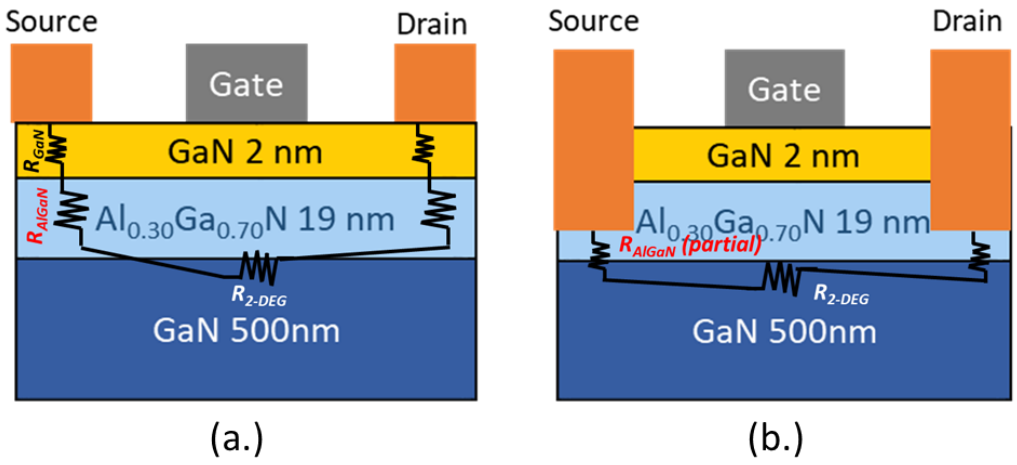



*Fig. 1. 6 Schematic of AlGaN/GaN HEMTs source/drain contacts with (a.) contacts deposited on top of barrier and (b.) barrier etched contacts along with their contact resistances.*

**IX.** **<u>Gate Contact:</u>** Ni/Au gate contact is often used to achieve Schottky contacts to deplete the 2-DEG. Ni/Au forms a thermally stable Schottky barrier with sufficient barrier height and has high structural integrity necessary for high power applications. For HEMTs or HFETs, usually gate dielectric is used in order to avoid gate leakage current under high electric field with improved field distribution and it acts as a passivation to 2-DEG improving the sheet resistance. The gate dielectric material such as oxide and nitride are commonly used as gate dielectric to constitute metal oxide semiconductor (MOS) and metal insulator semiconductor (MIS) - HEMTs respectively. MISHEMTs or MISHFETs are the choice of devices fabricated throughout this thesis work and used as a test vehicle. Moreover, the impact of SiN on the HFET performance is shown later in section 3.2.6.

### 1.3.4 Device Fabrication Process

The device fabrication has been developed in the central micro-nano fabrication (CMNF) 1600 $m^2$ ISO6 clean room at the Institute of Electronics, Microelectronics and Nanotechnology (IEMN) laboratory. The on-wafer high voltage characterization up to 10 kV has been realized at the Microwave, Optics, and Photonics characterization center (CHOP) facility of IEMN. The HEMT fabrication begins with the dicing of samples using various equipment such as a saw cutter, laser dicing, or diamond point cutter. Since these are novel heterostructures, the wafers are diced into small pieces of approximately 2 cm × 2 cm or quarter pieces depending on the size and type of the substrate. Multiple samples are derived from each wafer necessary for the process optimization at each step and to conclude the

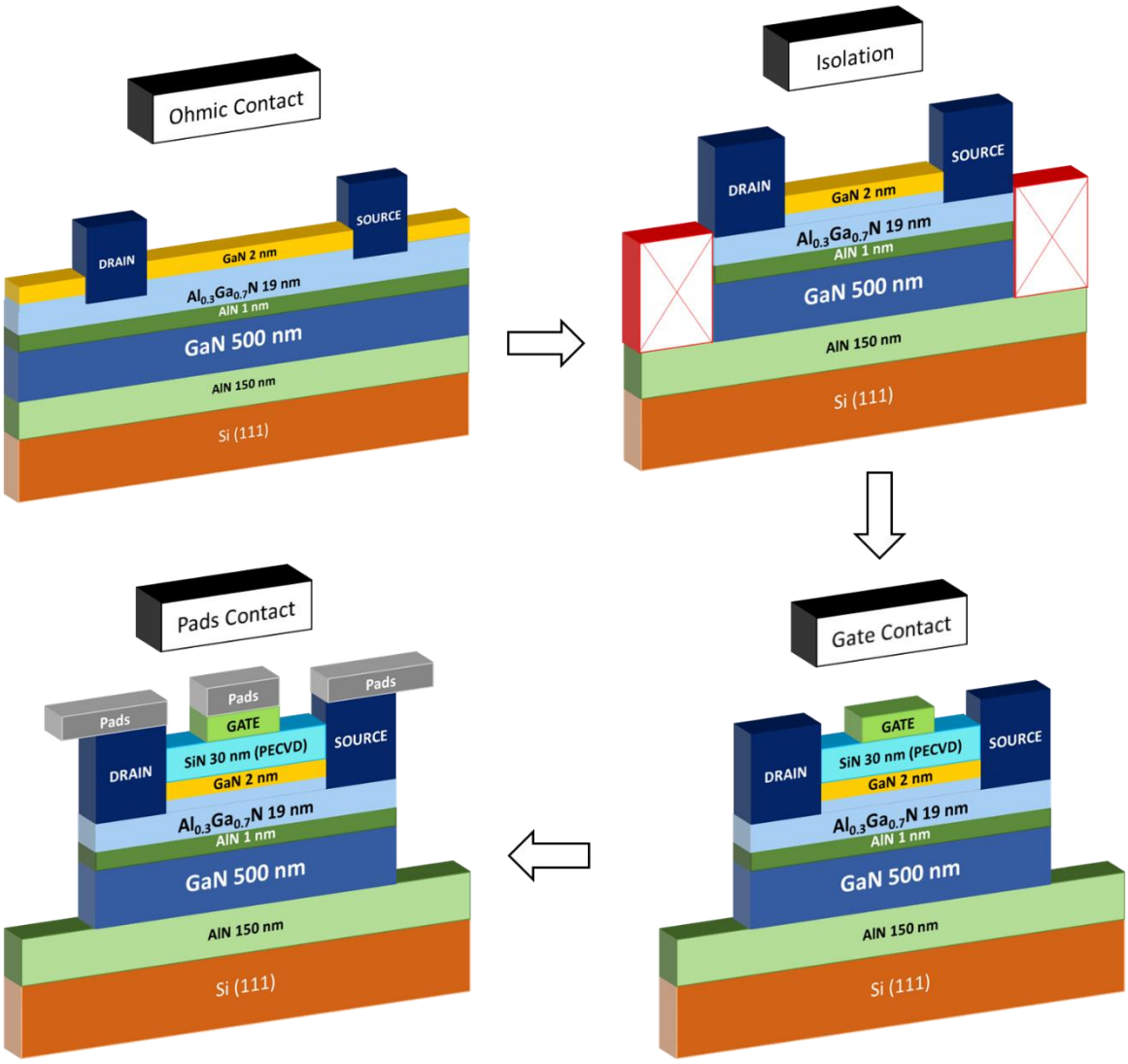



*Fig. 1. 7 Schematic fabrication flow diagram of GaN HEMTs*

design of experiments. After dicing, the samples are cleaned by standard cleaning process first with acetone and then with isopropyl alcohol (IPA) to get rid of surface contaminants and wafer dust [41]. Finally, the samples are dried using nitrogen gas.

The device processing begins with the formation of source/drain ohmic contacts followed by isolation of the device's active area. Afterward, on-wafer measurements are carried out inside the clean room to verify the 2DEG properties of heterostructures and the quality of ohmic contacts. The surface is passivated after the isolation followed by the deposition of gate and pad contacts as shown in Fig 1.7.

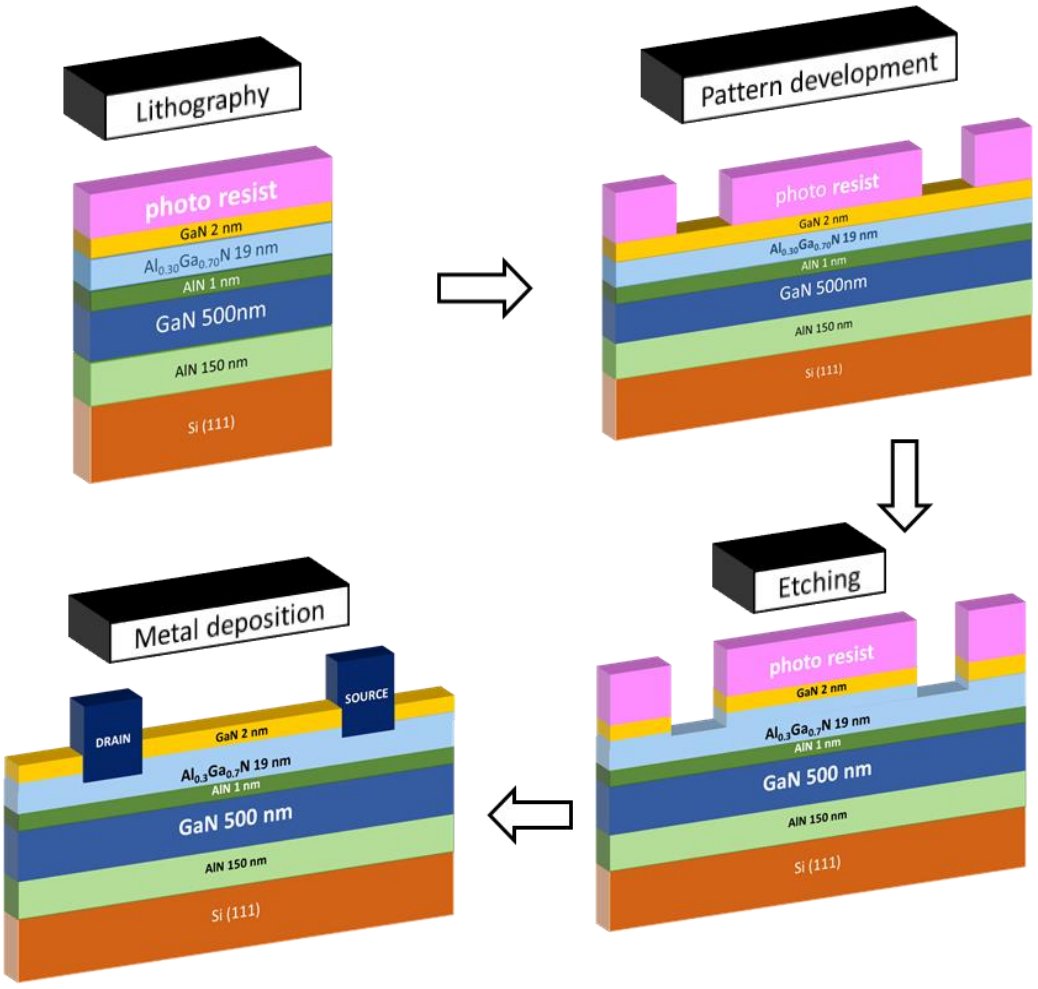



*Fig. 1. 8 Schematic of ohmic contact fabrication*

### *a) Ohmic contact development*

i. Source/Drain Contact Fabrication Process

Typically, a 2-3 µm thick bilayer photoresist stack consisting of LOR10A and S1818 are used for contact development. However, during the fabrication of heterostructures grown on bulk AlN substrates, the bilayer lift-off technique showed retention and re-deposition of metal particles. The lift-off profile was not clean as well, which might be caused to partial barrier etching prior to metallization or due to the thin undercut of S1818 photo resist. Hence, a new lift-off recipe was developed using a single-layer ARP5320 photoresist. The new recipe uses a 2 µm layer of diluted ARP5320 photoresist reducing the lithography processing time by almost 60% as compared to the bilayer photoresist with a notable improvement of the lift-off profile and excellent contact edge acuity (see Fig. 1.9). The ohmic contact fabrication can be realized into photolithography and development of mask pattern followed by barrier etching and metal deposition as shown in Fig. 1.8. The development of source/drain contact starts with the deposition of hexamethyldisilazane (HMDS), which acts as an adhesion promoter for the resist. Then, ARP5320 photoresist is deposited followed by a 4 min post-bake at 100°C. The devices are then aligned with photo mask using Suss Microtech MA6 aligner and exposed to a UV lamp (365 nm) at around 360-370 watts lamp power. Finally, the patterns are revealed on the sample using the AR 300-26 developer solution.

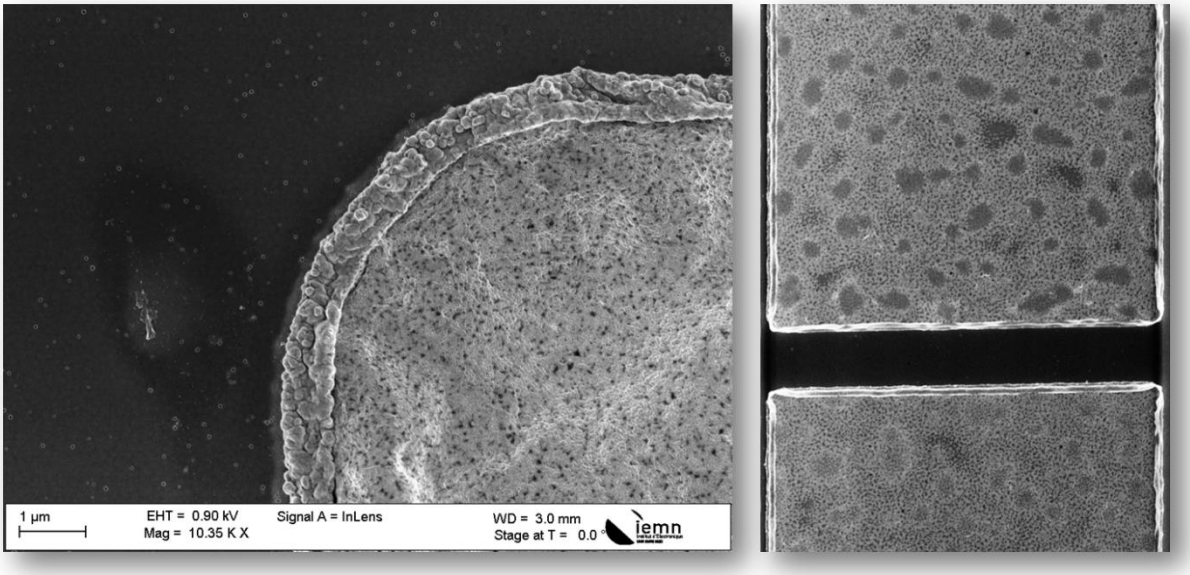



*Fig. 1. 9 SEM images of ohmic contacts after RTA*

To achieve ohmic behavior, the contact must be in close proximity to the 2DEG. Hence, a recessed barrier etching technique is applied, where approximately 2/3rd of the barrier thickness is etched. The devices are moved to inductively coupled plasma-reactive ion etching (ICP-RIE) tool for the GaN/AlGaN etching using low-power $Cl_2$/Ar or high-power $BCl_3/SF_6$ plasma chemistry [42]–[44]. After dry etching, the contact surface is treated in a HF-incorporated buffered oxide etch (BOE) solution for 30s to remove the native oxide from the surface prior to metallization [45]. The metallization was realized in Plassys MEB550S e-beam evaporator system. The samples are mounted on the holder and kept in the load lock, which is then transferred to the main chamber for required metal stack deposition. The deposition of Ti (12nm)/ Al (200nm)/ Ni (40nm)/ Au (100nm) metal stack is performed using e-beam evaporation under a high vacuum [34]. After metallization, the samples are immersed in the SVC-14 solution heated at 70°C for 1-2 hours for the metal lift-off followed by standard cleaning. The samples undergo rapid thermal annealing (RTA) at 825°C for 30 seconds optimized for GaN channel HEMTs under constant 250 SCCM nitrogen flow concluding the fabrication of source/drain contacts. It can be pointed out that RTA at CMNF using Annealsys AS-one can be ramped up to 1300°C at a maximum rate of 200°C/s.

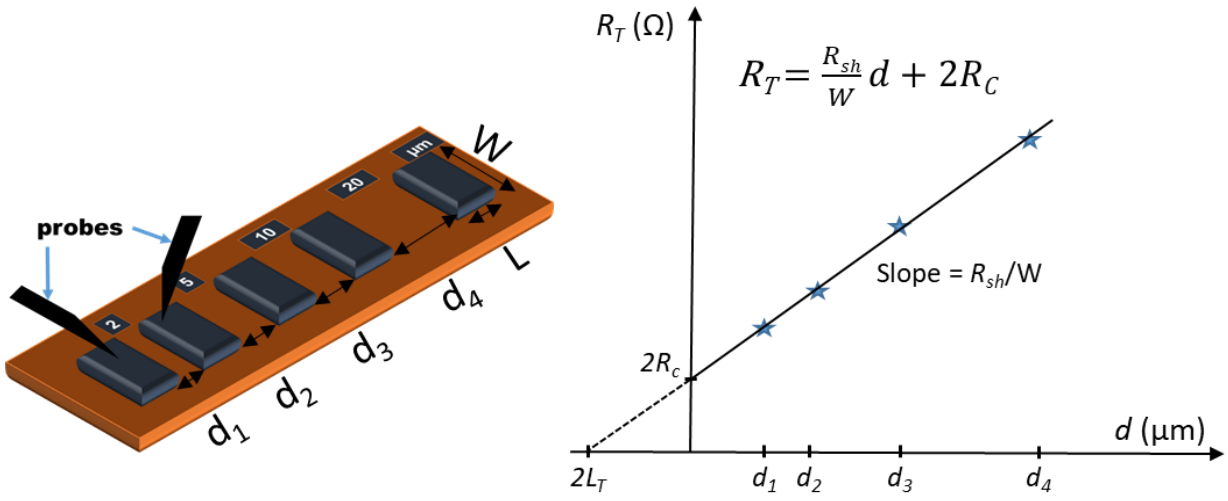



*Fig. 1. 10 Schematic of TLM bar pattern with various contact spacing (left) and Graphical description of TLM (right)*

ii. Contact resistance measurement

The current-voltage (I-V) characteristics and drain/source contact resistance (4-point probe measurement) were carried out using a Transfer length method (TLM) bar pattern with different spacing, using Keithley 2612B source measurement unit (SMU) paired with HP 3478A multimeter [46], [47]. The TLM consists of L × W rectangular contacts with various spacing (see Fig. 1.10) from $d_1$ - $d_4$. The total resistance ($R_T$) measured between two adjacent contacts comprises two probe contact resistances along with the semiconductor resistance [see Fig. 1.10 (right)]. Here, $R_{SH}$ is the sheet resistance and $R_C$ is the contact resistance. The sheet resistance can be calculated by the slope of the total resistance as a function of contact spacing (d). The $R_C$ is extracted from the y-intercept. The x-intercept extrapolation reveal the transfer length ($L_T$) which is the effective length of the charge transport. The I-V characteristics of GaN-on-AlN HEMTs (see Fig. 1.11) show perfectly ohmic behavior with currents of more than 1 A/mm when biased up to 5V. After several optimization steps, by varying the recessed barrier etch depth and annealing temperature, state-of-the-art ohmic contacts as low as 0.126 Ω.mm with contact resistivity (ρ) of 4.95 × $10^{-7}$ Ω.cm$^2$ and a TLM sheet resistance of 318 Ω/square has been measured for GaN-on-AlN using the TLM method as shown in Fig. 1.11 (right).

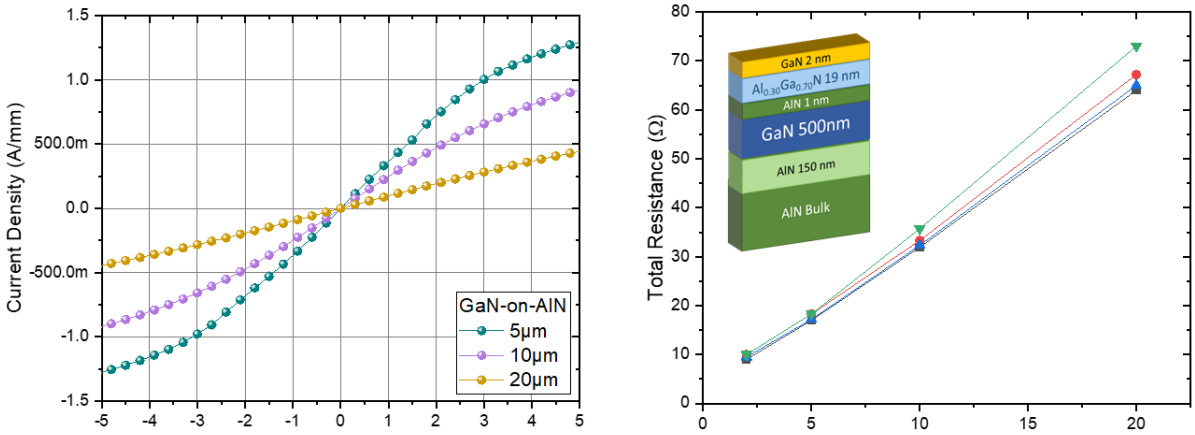



*Fig. 1. 11 I-V characteristics (left) and Total resistance vs TLM spacing (right) for GaN-on-AlN with the inset showing the cross-sectional schematic of structure.*

### *b) Device Isolation*

The device isolation can be realized using mainly two techniques:

1.) MESA isolation

2.) Ion implantation

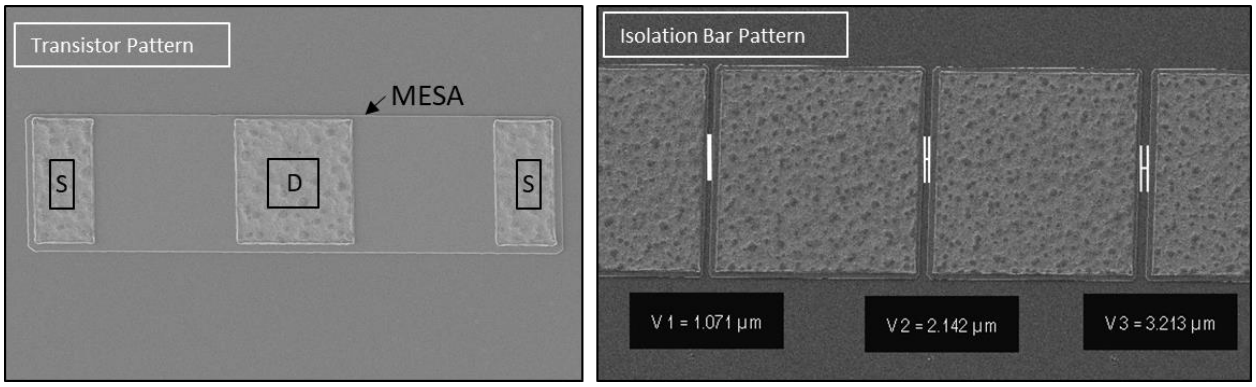



*Fig. 1. 12 images of MESA isolated transistor pattern (Left) and Isolation bar pattern (Right)*

The mesa process isolates the active area with the island formation by dry etching of epi-layers whereas implantation technique works by changing the material property around the active area using a high-energy ion beam [48]. Since we target low-cost device processing and submicron thick heterostructures, all samples in this work have been MESA isolated. In the initial device processing, only photoresist mask was used for the MESA isolation which led to the re-deposition of "burned" resist contaminating the surface of sample when etched in ICP-RIE, which might lead to parasitic leakage current. Henceforth, $SiO_2$ mask has been integrated into the process to prevent surface contamination. The process of device active area isolation begins with the deposition of 200 nm $SiO_2$ mask at 300°C using plasma enhanced chemical vapor deposition (PECVD) technique. Secondly, devices are spin-coated with S1818 photoresist and exposed under UV lamp followed by the mask pattern development using MF-322 developer solution. Afterwards, the $SiO_2$ mask is patterned using reactive ion etching technique with $SF_6$ plasma followed by residual resist removal using a heated SVC-14 solution. Then, the GaN and AlGaN layers are etched using $Cl_2$/Ar plasma in the ICP-RIE tool. Finally, the $SiO_2$ mask is removed using BOE 7:1 solution and the step of MESA is measured using a profilometer. The SEM images of MESA isolated structures are shown in Fig. 1.12 where the left image shows the isolated active area of the transistors with source and drain contacts and the right image shows the isolated bar pattern along with the contact spacing. After isolation of the active area, the contact resistance and I-V characteristics are verified. Hall Effect measurements and buffer breakdown characteristics are performed on-wafer to verify 2DEG properties and buffer leakage current respectively.

### *c) Gate contact development*

Before gate development, the sample surface is passivated with 30 nm SiN at 340°C using plasma-enhanced chemical vapor deposition (PECVD). The gate contact fabrication begins with the ARP5320 photolithography process similar to the ohmic contact process after which Ni (20 nm)/ Au (200 nm) metal stack is deposited using e-beam evaporation. Finally, the samples are immersed in SVC-14 at 70°C for 2 hours concluding the fabrication of Schottky contacts. The fabricated HEMTs have two gate fingers (see Fig. 1.13) with gate width ($W_G$) x gate length ($L_G$) = 50 × 2.5 µm and $L_{SG}$ = 2.5 µm with various $L_{GD}$ from 5-40 µm. Post-metallization, the gate leakage current is verified using a circular diodes pattern.

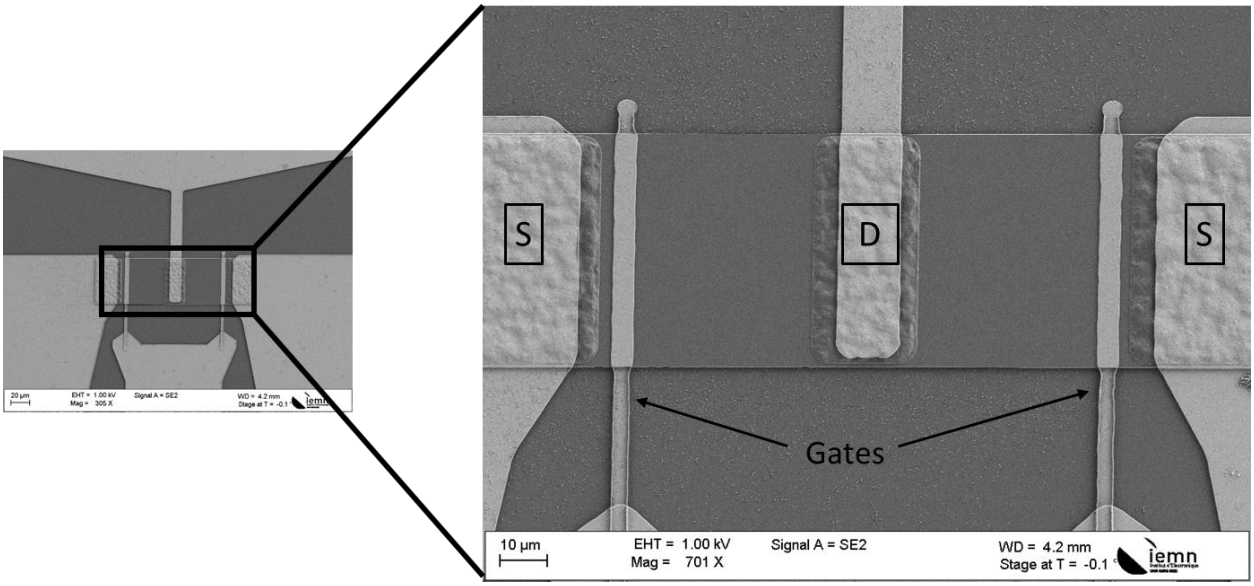



*Fig. 1. 13 SEM Image of Transistors with dual gate configuration*

### *d) Pads contact step*

The fabrication of pads is necessary to prepare the HEMT for on-wafer electrical measurements and facilitates the use of coplanar probes or needles. The contact fabrication starts with the ARP5320 photolithography process similar to the ohmic contact process. Then, the SiN passivation is etched selectively in order to connect the ohmic contacts with pads, using reactive ion etching (RIE) tool with $SF_6$ plasma. E-beam evaporation of Ti (100nm)/ Au (200nm) metallization followed by lift-off in heated SVC-14 concludes the MISHEMTs fabrication process.

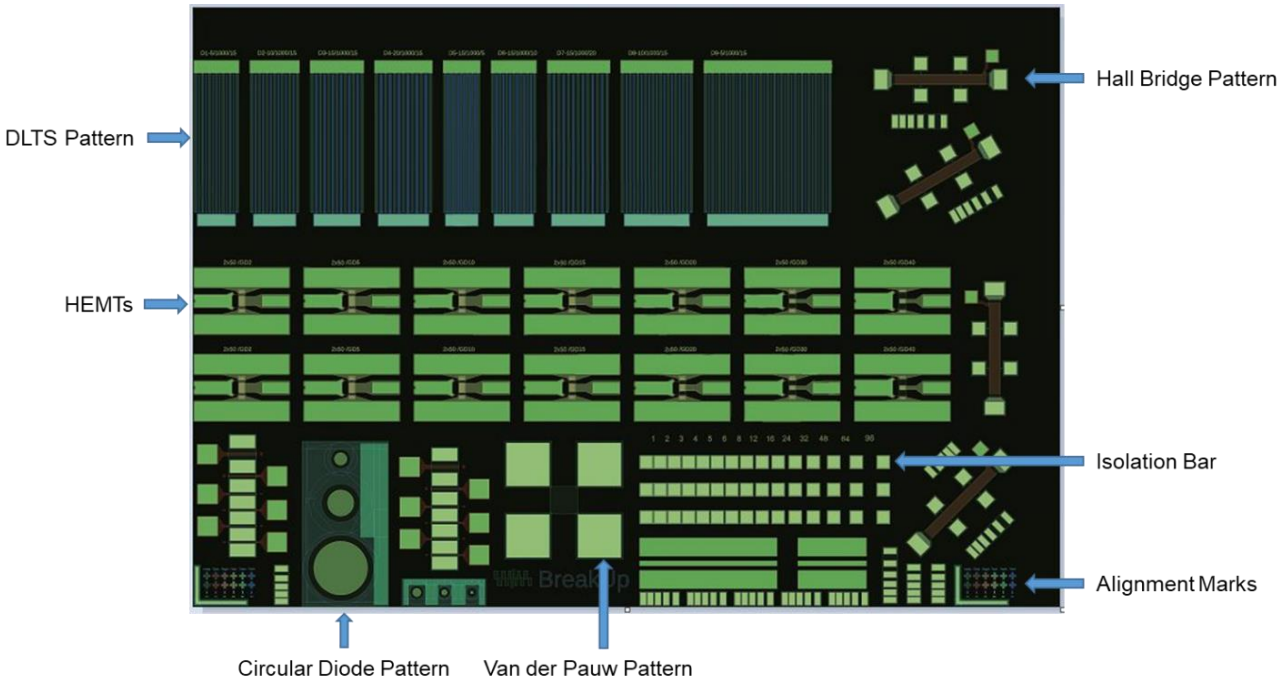



*Fig. 1. 14 Schematic of device Fabrication mask*

### *e) Fabrication Mask*

A mask set dedicated to high voltage HFETs has been designed to evaluate several aspects of epi-structure such as the DC performance of HFETs and its 2DEG properties along with the buffer quality and to perform advanced physics-based characterizations such as deep-level transient spectroscopy (DLTS), Hall bridge measurements. This study has been carried out by using an optical layout design called "BREAKUP" (see Fig. 1.14) which consists of optical photolithography steps. The mask consists of a set of process monitor patterns, alignment marks, and transistors with various $L_{GD}$. The lower part of the layout shows the circular diode pattern with various diameters that are used to verify the Schottky contact

characteristics followed by Van der Pauw pattern on the right used to verify the 2DEG properties such as electron mobility, charge concentration, and sheet resistance. The 100 × 100 µm isolation bar patterns are located to the right of the Van der Pauw pattern, with various contact spacing from 1-96 µm. Multiple transmission line measurement (TLM) patterns with contact spacing of 2 µm, 5 µm, 10 µm, and 20 µm can be seen below the isolation bar pattern to measure the maximum current density and contact resistance. The middle part of the layout comprises two rows of transistors with various $L_{GD}$ from 2-40 µm. The top of the mask layout shows the DLTS and Hall bridge pattern used to realize the trapping effects and understand electron transport.

### 1.3.5 HEMT Electrical Characterization

***a) High Voltage Test Bench***

The electrical measurements of fabricated devices were carried out at the ISO8 certified CHOP center in IEMN. The high voltage DC measurements were performed on a MPI TS150-HP probe station setup in a black box with coaxial cables connected to the Keysight B1505A power device analyzer/curve tracer that can accurately on-wafer measure up to 10 kV /20 A when operated in conjunction with Keysight N1268A ultra high voltage expander unit (see Fig. 1.15). Characterization engineer of CHOP facility Etienne Okada has realized the HV bench setup. The electrical measurements were performed at constant room

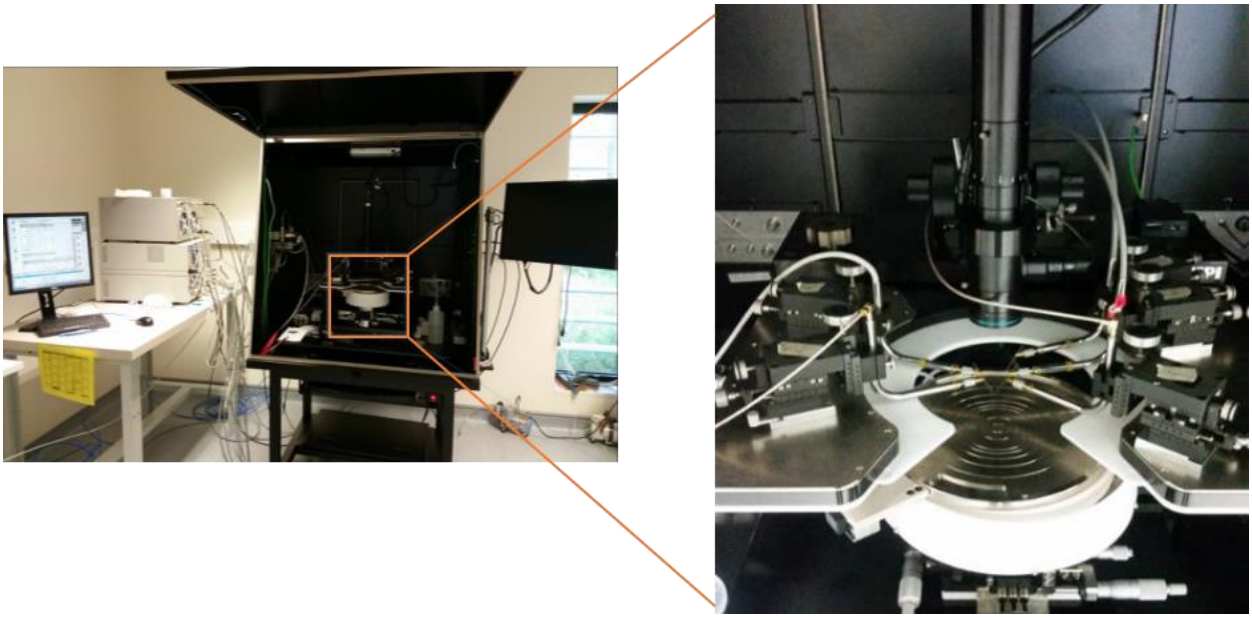
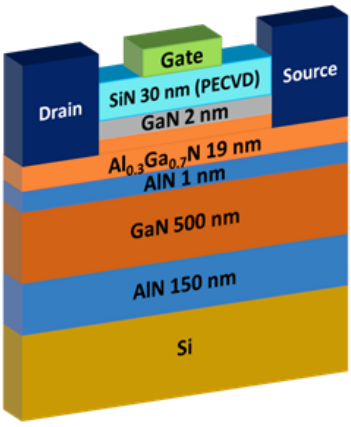
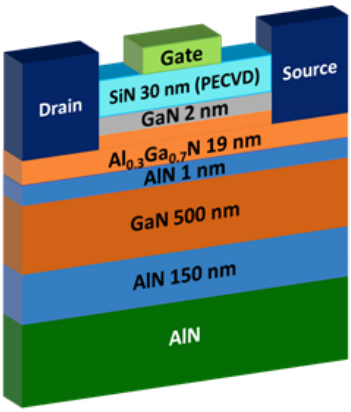


*Fig. 1. 15 High voltage characterization bench setup*

temperature with devices immersed in 3M-Fluorinert FC-40 which has a high dielectric strength (46 kV for a 2.54 mm gap) that prevents arcing in the air.[49]

### *b) DC characterization (GaN-on-Si vs GaN-on-AlN)*




| 500 nm GaN channel | Sheet Resistivity [ohm/sq] | Electron Mobility [cm²/V.s] | 2DEG Concentration [1/cm²] |
|---|---|---|---|
| GaN-on-Si | 800 | 950 | $8.2 \times 10^{12}$ |
| GaN-on-AlN | 330 | 1920 | $1.0 \times 10^{13}$ |

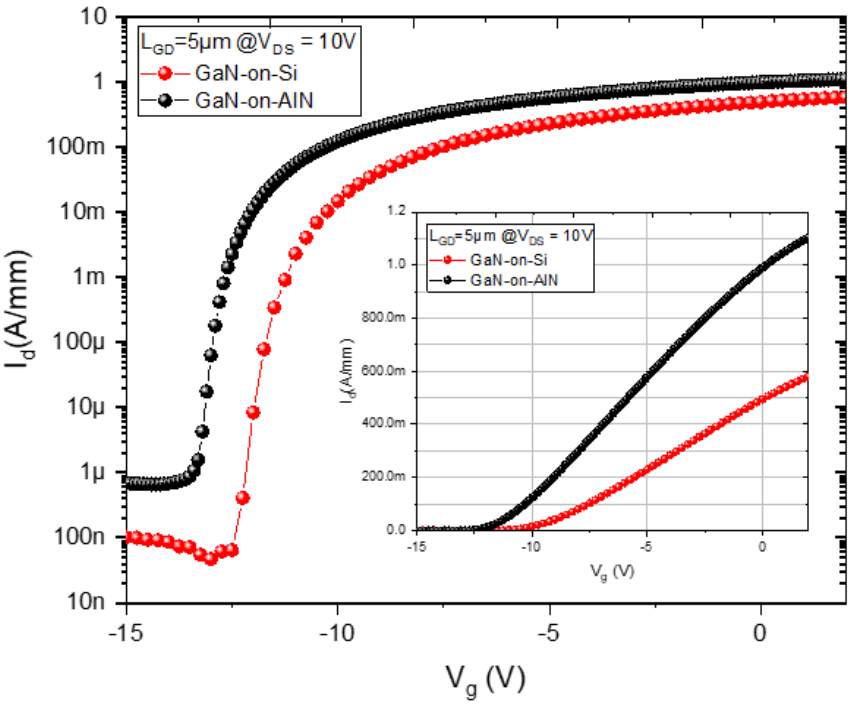



*Fig. 1. 16 Schematic of GaN-on-Si and GaN-on-AlN MISHEMTs (left) with their transfer characteristics and 2DEG properties*

To evaluate and understand the impact of the substrate on GaN HEMTs operation, an experiment was performed based on AlGaN/GaN heterostructures grown on 3-inch bulk Si and 1-inch bulk AlN wafers. The device structure consists of a 19 nm thick $Al_{0.3}Ga_{0.7}N$ barrier and a 500 nm GaN channel with a 150 nm nucleation layer grown on silicon and bulk AlN substrates (see Fig. 1.16). The devices were capped with a 2 nm GaN layer. Source/Drain contacts were fabricated with standard Ti/Al/Ni/Au stack followed by RTA at 825°C to get ohmic behavior. The active area of the devices was isolated down to the GaN channel. MISHEMTs were fabricated on these heterostructures with a 30 nm PECVD SiN below the gate. DC characterization was carried out on transistors having $L_G$= 2-3 µm and with various

gate-drain spacing from 2-40 µm. The DC measurements give information on the off-state leakage current, maximum on-state current, threshold voltage, and sub-threshold swing. Hall Effect measurements of GaN-on-AlN show quite comparable 2DEG concentration and twice better electron mobility as compared to GaN-on-Si owing to better epi-quality on AlN.

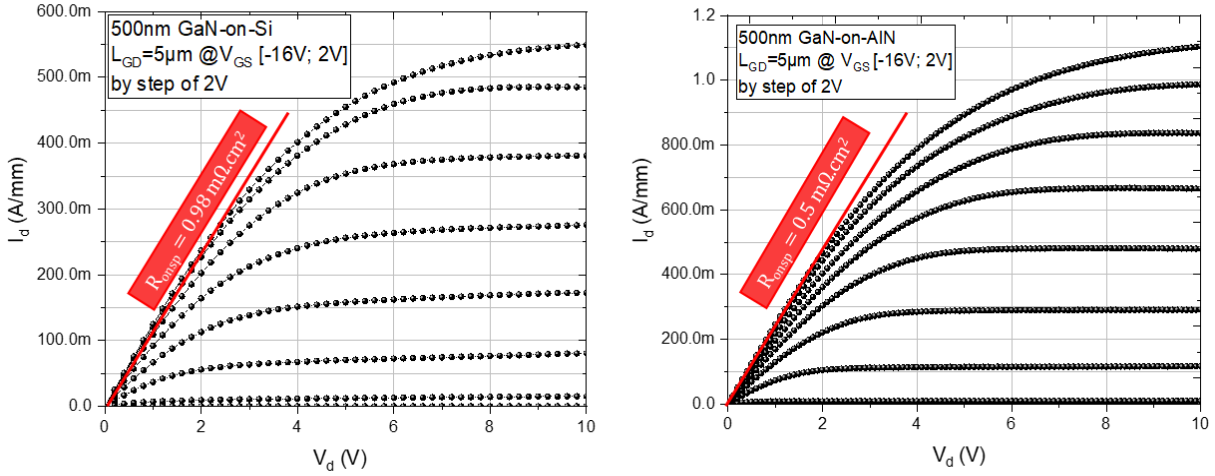



*Fig. 1. 17 Output characteristics of GaN-on-Si (left) and GaN-on-AlN (Right) MISHEMTS*

The transistor on-off current ratio ($I_{ON}/I_{OFF}$) shows the ability to switch devices and portray static current consumption that can be determined from the semi-log transfer characteristics as shown in Fig 1.16 for MISHEMTs with $L_{GD}$ = 5 µm at $V_{DS}$ = 10 V. However, for ideal high voltage application devices a high $I_{ON}/I_{OFF}$ ratio is targeted to minimize the off-state power loss, which in turn will reduce the static current consumption and eventually reduce the gate switching speed. The 500 nm GaN channel structures on silicon and AlN substrates reveal $I_{ON}/I_{OFF}$ of 9.6 × $10^5$ and 1.3 × $10^6$ respectively. The linear transfer characteristics in the inset reveals the threshold voltage and maximum current density at given biasing conditions. The maximum on-state currents for the heterostructures are in agreement with their sheet resistance for both structures. The output characteristics shows evolution of drain current density with the applied drain-source voltage for different gate biases. The product of device active area with inverse of slope of the tangent in the linear regime of output characteristics for saturation current at $V_{GS}$ = 0 V gives specific on-state resistance. Fig. 1.17 shows $I_D$-$V_D$ characteristics of GaN-on-Si (left) and GaN-on-AlN (right) for $V_{DS}$ = 10 V and gate bias sweep from - 16 V to + 2 V. A maximum drain current density of

1.1 A/mm was measured at $V_{GS}$ = + 2 V for GaN-on-AlN HEMTs with specific on-resistance as low as 0.5 mΩ.cm².

### *c) Buffer breakdown measurements*

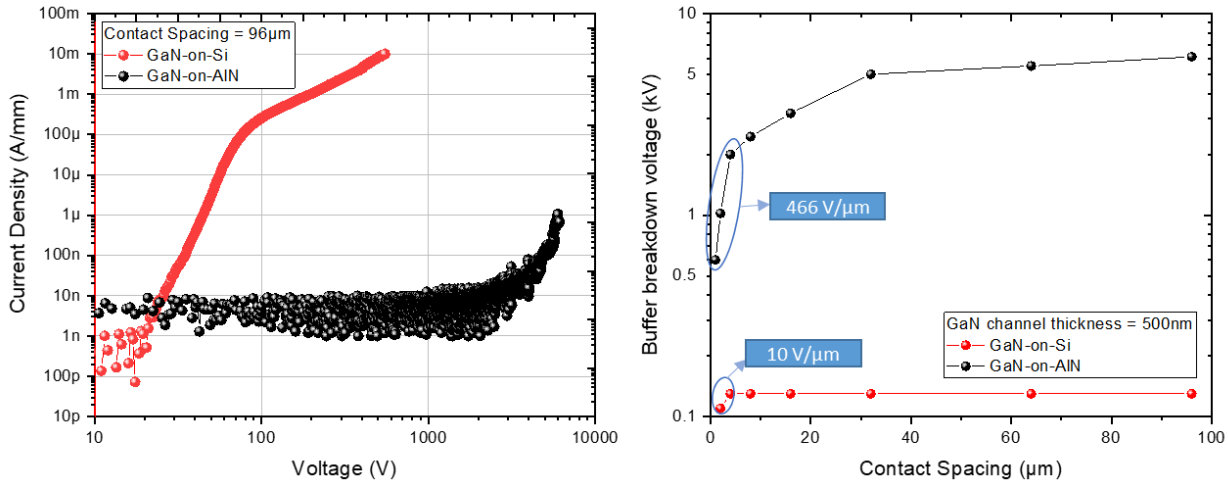



*Fig. 1. 18 Lateral breakdown characteristics for GaN-on-Si and GAN-on-ALN for 96 µm contact spacing (left) and evolution of buffer breakdown voltage with increasing contact spacing*

The buffer breakdown measurements reveal the voltage withstanding capabilities and to determine the leakage current density of the epitaxy below the active layers of transistors. The lateral breakdown measurements were carried out using isolation bar pattern on wafer with various contact spacing from 1 µm to 96 µm with the samples immersed in fluorinert liquid. The evolution of leakage current density with applied bias is shown in Fig. 1.18 (left) for GaN-on-Si and GaN-on-AlN with 96 µm contact spacing and both devices are mesa etched down to the GaN channel. GaN-on-Si HEMTs show almost linear increment of leakage current density at low bias with leakage current density reaching 10 mA/mm at 540 V whereas GaN-on-AlN showed very low leakage up to 100nA/mm up to 5000 V. The GaN-on-AlN devices shows almost around 140× times improvement in the voltage blocking capability at 100 nA/mm. The buffer breakdown voltage evolution with various contact spacing is shown in Fig. 1.18 (right). Here, we can observe the electrical breakdown field evolves from around 0.5 MV/cm for GaN-on-Si that rises up to 6 MV/cm for GaN-on-AlN considering low contact spacing (< 5 µm). The saturation in breakdown voltage can be observed in GaN-on-AlN devices due to increasing defect density with larger spacing. This is why moving towards AlN substrate gives a huge advantage over the reduction of device dimensions on a large scale as compared to conventional Si-based FETs.

### *d) Transistor breakdown measurements*

The destructive 3-terminal electrical breakdown measurements are realized for MISHEMTs by fixing $V_G < V_{TH}$ and observing the evolution of drain and gate leakage currents by increasing the applied drain-source bias. The transistor breakdown characteristics for devices with $L_{GD}$ = 40 µm and $L_G$ = 3 µm are shown in Fig. 1. 19. Here, the GaN-on-Si devices showed low gate leakage until 5V with logarithmic increment of drain leakage current demonstrating the electron injection through silicon that eventually increases the gate leakage current leading to catastrophic material breakdown. On the other side, GaN-on-AlN devices showed a matching of low drain and gate leakage characteristics, revealing the absence of electron injection into the bulk AlN substrate despite the use of submicron thick heterostructure epitaxy. The rather low transistor breakdown voltage and high off-state leakage current as compared to lateral breakdown characteristics can be attributed to the quality of top-epi layers and surface contamination.

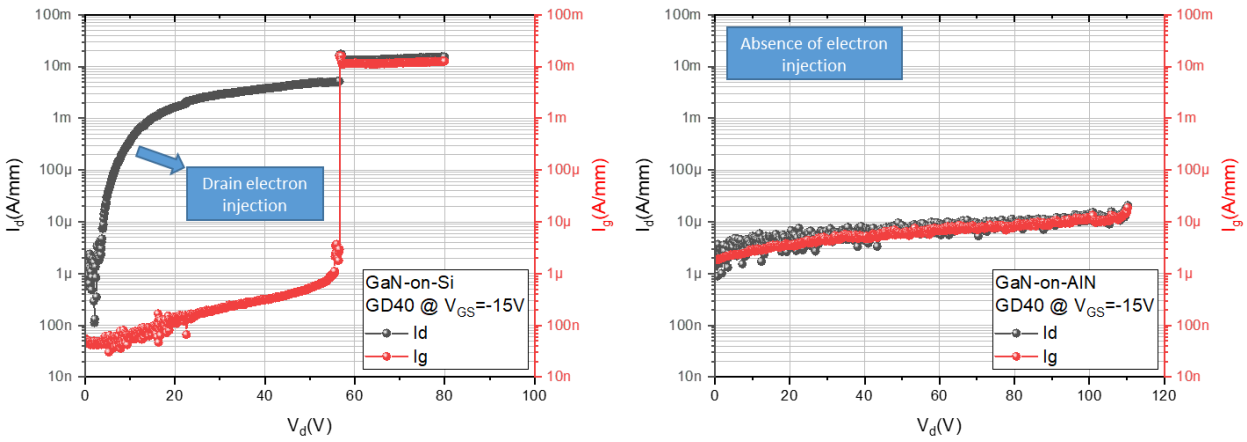



*Fig. 1. 19 Transistor breakdown characteristics for GaN-on-Si (left) and GaN-on-AlN (right) for devices with $L_{GD}$ = 40 µm*

### *e) Conclusion*

The reliable operation of transistors requires not only high-quality epitaxy but also the incorporation of appropriate fabrication process design and equipment-specific optimization for each step. The measurements necessary to characterize the MISHEMTs were shown with devices based on two different substrates, GaN-on-Si and GaN-on-AlN. The 2x better 2DEG mobility of GaN-on-AlN as compared to GaN-on-Si can be verified from the Hall Effect measurements owing to the high-quality epitaxy on a low lattice mismatch substrate. Both devices showed a high $I_{ON}/I_{OFF}$ ratio of up to $10^6$. The maximum current

density up to 1.1 A/mm has been measured giving specific on-resistances of less than 1 mΩ. $cm^2$. The buffer breakdown measurements of GaN-on-Si showed around 0.5 MV/cm of electrical breakdown field that increased to 6 MV/cm for GaN-on-AlN using 1 μm contact spacing. Furthermore, AlN shows no electron injection into the substrate, which is one of the major causes of electrical failure in GaN-on-Si based FETs used for high-voltage applications. Thus, it can be concluded that bulk AlN substrate may pave the way for pushing device operation into the kV regime. Hence, a study based on variation in GaN channel thickness has been accomplished with the heterostructures grown on bulk AlN substrates. The next chapter will go into details about the structural and electrical impacts of downscaling GaN channel thickness on bulk AlN.

### 1.3.6 Challenges of GaN-on-Si HEMTs

GaN HEMTs on Si have shown great promise and over 10× better performance than Si FETs in terms of power handling capabilities and switching performance. However, there are several limitations or rather challenges associated with GaN-on-Si technology.

I. **Dynamic on-resistance:** The current collapse due to buffer trapping, surface trapping, and gate instabilities has been a primary challenge for the development of GaN-on-Si HEMTs. In order to compensate the donor-type (Si or O) impurities during the epitaxy, C dopant impurities are incorporated within the GaN buffer in order to achieve low leakage current within the buffer layers [50], [51].

II. **Thermal Mismatch:** Due to large thermal mismatch of around 54% between GaN and Si, thick crack free GaN epi-layers are quite difficult to grow. The crack forms when the GaN layer is cooled to room temperature due to large in-plane thermal expansion coefficient mismatch between GaN and Si that produces large tensile strain in GaN. In 2017, Tanaka *et. al* demonstrated selective area growth (SAG) of 18 μm thick GaN layers on Si substrates showing a dislocation density of $1.1 \times 10^7$ $cm^{-2}$ [52]. Moreover, recently thicker GaN epitaxy with crack free buffer up to 15 μm have been demonstrated by applying QST engineered substrate that shows a thermal mismatch of around 1% with GaN [53].

III. **Lattice Mismatch:** GaN-on-Si shows around 16% of in-plane lattice mismatch that leads to threading dislocations, point defects, trapping and the possibility of higher defect incorporation in the channel. To deal with this issue, growers have developed superlattice and stepgraded buffer growth techniques to compensate for the lattice mismatch resulting in high quality epi-layers. However, the combination of AlN/GaN superlattice buffer and intentional Fe or C doping can provide highly resistive buffer sufficient enough for 1200 V power electronics applications along with low trapping effects [38], [54].

IV. **Wafer Bowing:** The tensile stress in the GaN layer due to thermal mismatch and lattice mismatch leads to warping on the wafer. The wafer bowing significantly influences the yield, performance, and reliability of fabricated devices. Tham *et. al* showed a 50% reduction in wafer bowing the AlGaN/GaN heterostructures grown on Silicon-on-Insulator (SOI) substrates as compared to Si substrates giving high output yield and improved uniformity of 2-DEG properties [55].

V. **Thermal Budget:** The main challenge for advanced electronic applications is to reduce the thermal budget of the process to grow high-quality layers. This allows the integration of GaN HEMTs to monolithic ICs and CMOS. The thermal budget performs in-situ thermal cleaning that removes any traces of surface contamination before the growth is initiated. Moreover, the thermal budget helps with stress mitigation throughout the structure by varying the temperature accordingly during epitaxial growth.

VI. **Normally Off Device:** Generally, GaN HEMTs are depletion mode devices having negative pinch-off voltage. However, this limits their applications due to safety-related concerns and residual power loss in converters. This necessitates the need for enhancement mode (e-mode) or normally off device mode to ensure safe operation and fault protection. There are several approaches such as p-GaN (Mg doped) layer below gate, cascode configuration, and recessed gate structure to enable e-mode device operation [54], [56]–[58].

GaN lateral devices come with significant challenges of reducing the intrinsic and extrinsic resistance and increasing the breakdown voltage. On the contrary, GaN-based vertical devices offer significant advantages for high-power applications, including compact size, high breakdown voltage, and reliability while facing substantial challenges [59]–[61]. The high cost and complexity of producing high-quality GaN substrates, along with technological hurdles in manufacturing, have slowed the progress of vertical device technology compared to the more mature lateral structure technology [62]. However, recently with the demonstration of avalanche breakdown on Si and bulk GaN substrates, GaN vertical devices pave the way for high-voltage switching devices [63]–[65]. Despite these challenges, the potential of vertical devices for high-power applications continues to drive research and development efforts in the semiconductor industry.

### 1.3.7 Industrial Outlooks

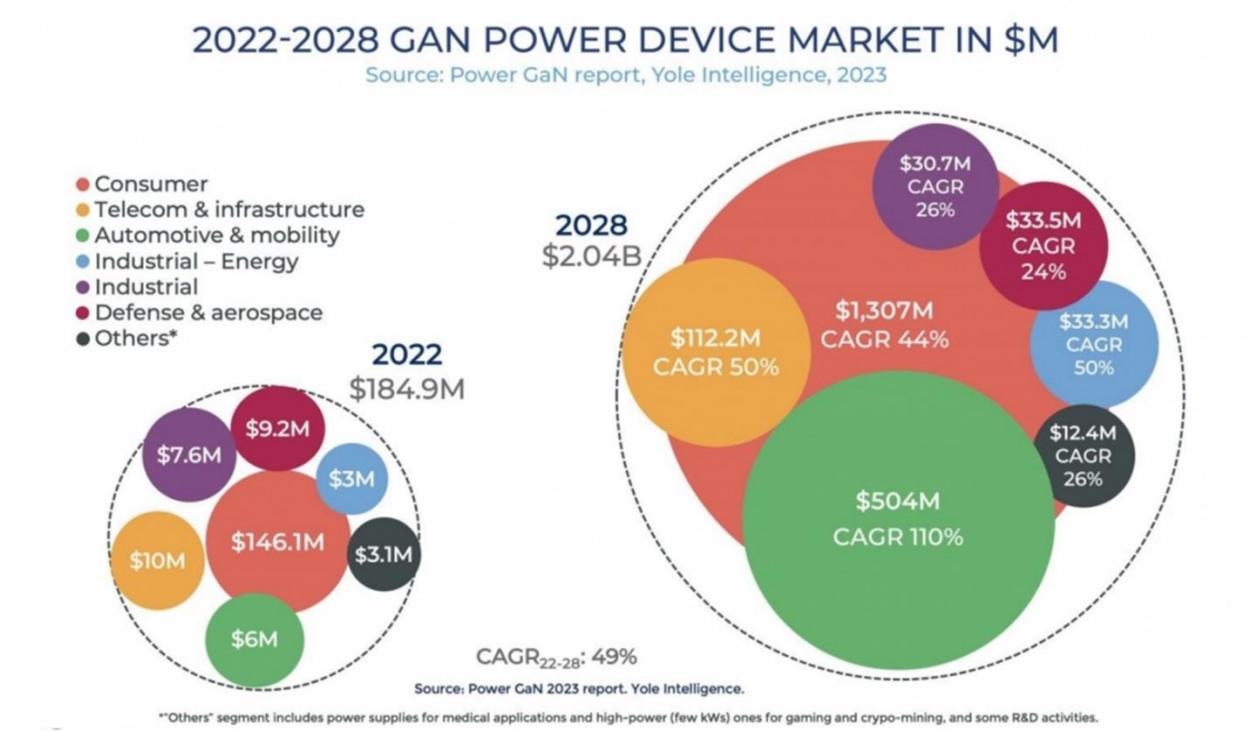



*Fig. 1. 20 GaN power device market share prediction 2022-2028 (source: Yole Group) [63]*

The Power GaN 2023 report by Yole Intelligence, a division of Yole Group, highlights fast chargers and adapters to be the primary driving force behind power GaN devices with their power reaching up to 300W. The adoption of GaN in automotive has evolved rapidly, focusing mainly on the onboard chargers and DC-DC converters. The GaN power device market is evolving rapidly at the compound annual growth rate (CAGR) targeted at 49% by 2028 (see Fig. 1.20).

The GaN power device application in consumer electronics is growing rapidly with a target reaching US$1.3 billion market by 2028. The industrial adaption of GaN reported in 2022 from substrate to systems shows quite dynamic supply chain (see Fig. 1.21) with majority of Chinese suppliers and manufacturers. The power GaN device market is experiencing significant growth across a variety of applications. This growth is reflected in the market's projected valuation, which is expected to reach around US$2.04 billion by 2028 representing a CAGR of approximately 49% from 2022 to 2028 [66]. The Chinese company Innoscience is investing more than $400m to expand its 8-inch wafer capacity from 10,000 to 70,000 wafers per month by 2025.

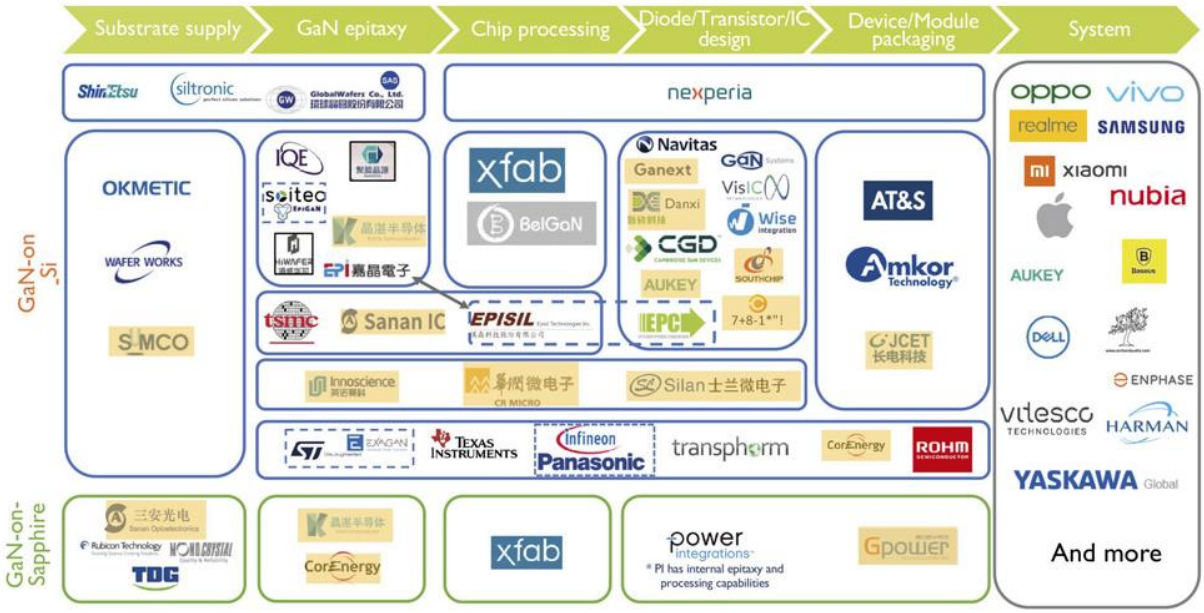



*Fig. 1. 21 Global power GaN supply chain (source: Yole Group)*

Commercial GaN HEMTs and SiC MOSFETs are available with drain-source breakdown voltage ($BV_{DSS}$) up to 1700 V and $I_{Dmax}$ up to 60 A in continuous mode of operation along with junction temperature ($T_j$) sustainability up to 200°C. The product of gate charge ($Q_G$) and on-resistance ($R_{DS(on)}$) gives the switching figure of merit for power devices. The $Q_G$ helps determine the switching time at any given gate drive current. Here, Table 1.2 summarizes the output characteristics and switching FOM for various commercial devices available from different suppliers. While comparing the 1200 V/30 A GaN HEMTs and SiC MOSFET, it can be noted that GaN HEMT has 10× better switching FOM and 1.5× lower on-resistance than SiC MOSFET.

| Company | Product | $BV_{DSS}$ (V) | $I_{Dmax}$ (A) | $R_{DS(on)}$ (mΩ) | $T_j$ (°C) | $Q_G$ (nC) | Switching FOM [$R_{on}.Q_G$] (Ω.nC) |
|---|---|---|---|---|---|---|---|
| STMicroelectronics | GaN HEMT | 650 | 25 | 49 | 150 | 5.4 | 0.265 |
| STMicroelectronics | SiC MOSFET | 1700 | 43 | 64 | 200 | 101 | 6.464 |
| GaNPOWER | GaN HEMT | 1200 | 30 | 52 | 150 | 8.25 | 0.429 |
| GaN Systems | GaN HEMT | 650 | 60 | 25 | 150 | 14.2 | 0.355 |
| OnSemi | SiC MOSFET | 1200 | 30 | 80 | 175 | 56 | 4.480 |

*Table 1. 2 Commercial WBG power devices along with their technical specifications and switching FOM*

The 650V GaN HEMT by GaN Systems shows more than 50% current collapse when operating at $T_j$ =150°C as compared to device operation at $T_j$ = 25°C with similar biasing conditions as shown in Fig. 1.22(a.). The power dissipation temperature derating of 650 V GaN HEMT is shown in Fig. 1.22(b.) indicating the maximum allowable power dissipation at a given casing temperature. The device can safely handle up to 460W power dissipation from 0°C to 25°C case temperature [67]. The device power dissipation limit drops linearly at the rate of 3.68 W/°C in the case temperature. Hence, when operating at 150°C case temperature, the device cannot dissipate any heat, requiring the implementation of heat sinks and cooling systems eventually limiting the device operation below 150°C environment.

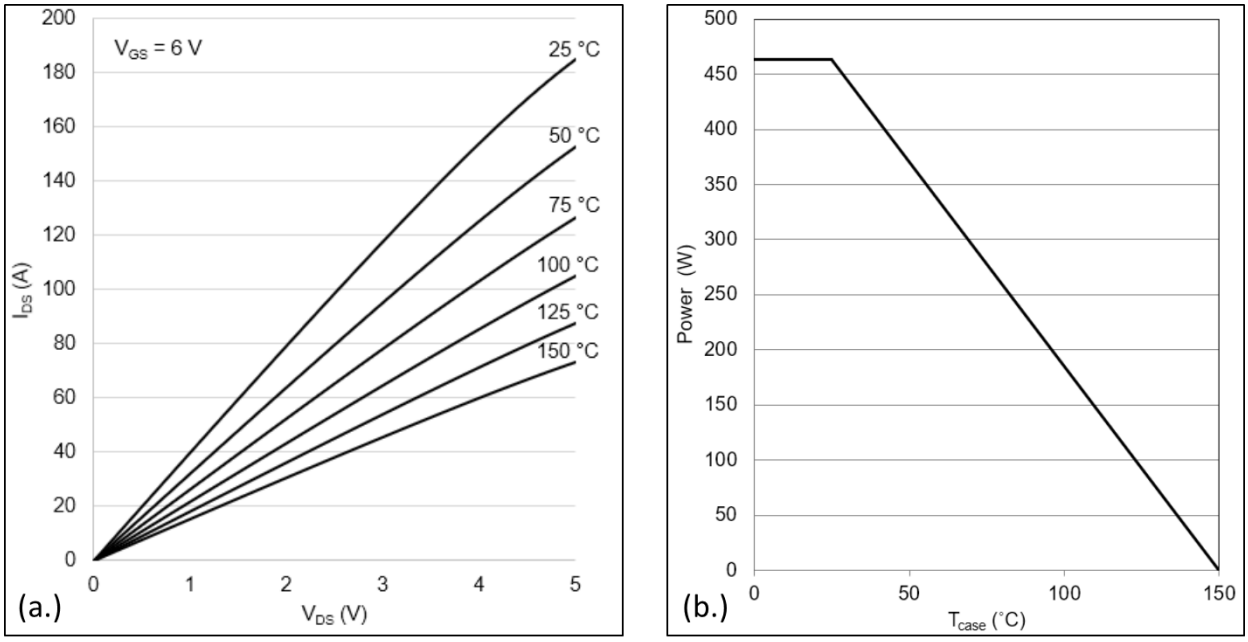



*Fig. 1. 22 GaN systems top-side cooled 650V E-mode GaN transistor (a.) $T_j$ dependence of $I_{DS}$ - $V_{DS}$ at $V_{GS}$ = 6 V and (b.) power dissipation temperature derating [67]*

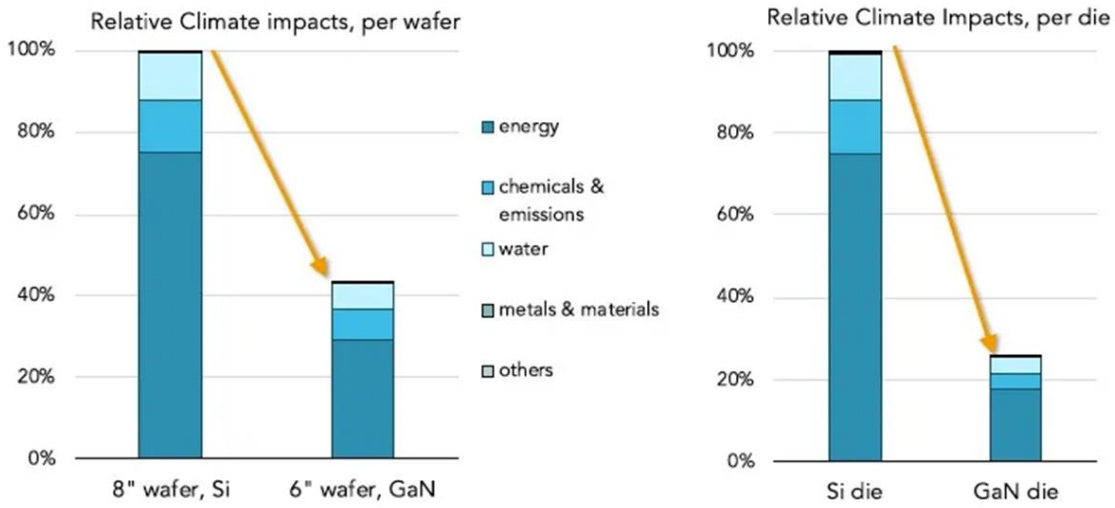



*Fig. 1. 23 Comparison of Fab energy/material usage for GaN and Si (source: www.powerelectronicsnews.com)*

### 1.3.8 Environmental Impacts

Since GaN offers such high breakdown voltages along with low on-resistance and high switching efficiencies, the required die size for a given application is much smaller compared to current Si devices for a given power rating. Thus, smaller chips enable more devices per wafer, which equates to comparatively less material and energy used in wafer processing. According to Navitas, in 2020 GaN power FETs showed up to 4× reduction in $CO_2$ emissions

contrary to conventional Si FETs. The $CO_2$ emissions are predicted to reduce by 10× per component by 2024 (see Fig. 1.24(a)). Figure 1.24(b.) shows estimation on the basis of Si-based 6.2kW residential inverters assuming GaN-based inverter enables 40% reduced power loss and 25% lower inverter costs demonstrating GaN's ability to increase micro-inverter speeds by 10x and enable a significant cost reduction [68].

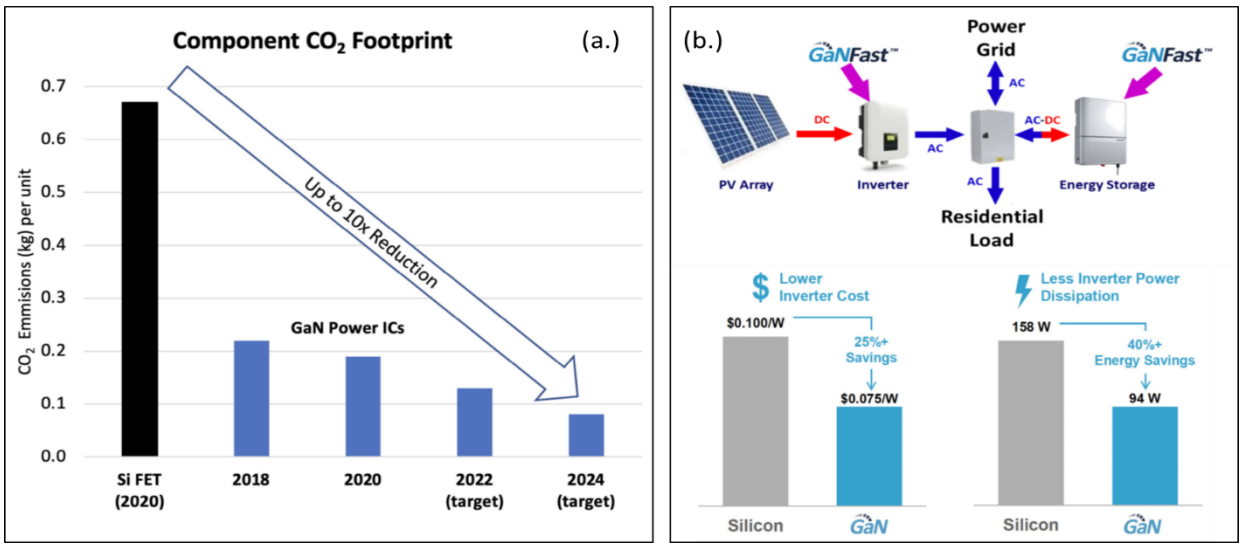



*Fig. 1. 24 (a.) $CO_2$ footprint comparison between GaN and Si device production (b.) Cost estimation of GaN replacing Si based power electronics in a solar PV system (source: Navitas Semiconductors)*

The number of GaN dies per wafer on a 150 mm GaN-on-Si wafer is 1.7× greater than the MOSFET dies on a 200mm silicon wafer. Furthermore, GaN device fabrication involves fewer furnace steps, leading to reduced energy consumption in fabrication as compared to silicon wafer processing. Figure 1.23 illustrates a comparison of energy and materials/chemicals used in manufacturing GaN and Si power devices, both at wafer and die levels. Notably, energy consumption at the die level for GaN is considerably less than 70% of that for silicon. The 6-inch GaN wafer has almost 60% lower climate impacts as compared to 8-inch Si. Applying GaN to every mobile application would save over 9 billion kWh and over 6 billion kg of $CO_2$ by 2025, equivalent to 1.3 million IC engines and passenger vehicles, or almost 14 billion barrels of oil. Considering manufacturing, GaN is around 10× more sustainable than SiC.

### 1.3.9 Power GaN Applications

***a) EV Battery Chargers***

In the electric vehicle (EV) sector the size, weight and power (SWaP) are critical, making GaN promising candidate for on-board electronics such as motor-drive inverter, battery charger, accessory power module (APM), etc. The application of WBG semiconductors in onboard EV battery chargers, such as a 7.2 kW model, is highly advantageous due to several factors:

1. These chargers operate at around 80-260 V AC and generates the DC outputs in the range of 250-450 V which is well within the limits of WBGs.
2. WBGs can easily tolerate the output currents.
3. Compared to inverters and APMs, EV charger requires more passive components, leading to them being the largest onboard electronic part.

The charger topology involves AC/DC conversion for both grid-to-DC and power factor correction (PFC), a DC/AC conversion to transform DC into high frequency AC, and a final AC/DC stage to rectify high frequency AC back to DC for battery charging (see Fig. 1.25(a)). Components like the grid inductor, resonant capacitor and inductor, transformer, and output capacitor are crucial, and are linked to the switching frequency. Liu *et. al* demonstrated 7.2 kW battery charger based on commercial ROHM SiC MOSFETs and GaN Systems GaN HEMTs [69]. They demonstrated 98% system efficiency at the rated power for GaN and SiC based chargers as shown in Fig. 1.25(b.). Their GaN charger reaches power density of 4 kW/L whereas SiC charger yields 3.3 kW/L. In 2017, Su *et. al* demonstrated a 6.6 kW GaN based isolated charger converter with high power density of 10.5 kW/L [70]. They compared 6.6 kW GaN charger with a 5 kW Si-based charger where the GaN based converter showed 50% reduction in volume and 75% reduction in weight at 2.5× higher switching frequency compared to Si-counterpart. In 2019, Qi *et. al* demonstrated a 3.3 kW bi-

directional DC-DC converter prototype using their 650V 49mΩ cascode GaN FETs with efficiency up to 98% [71].

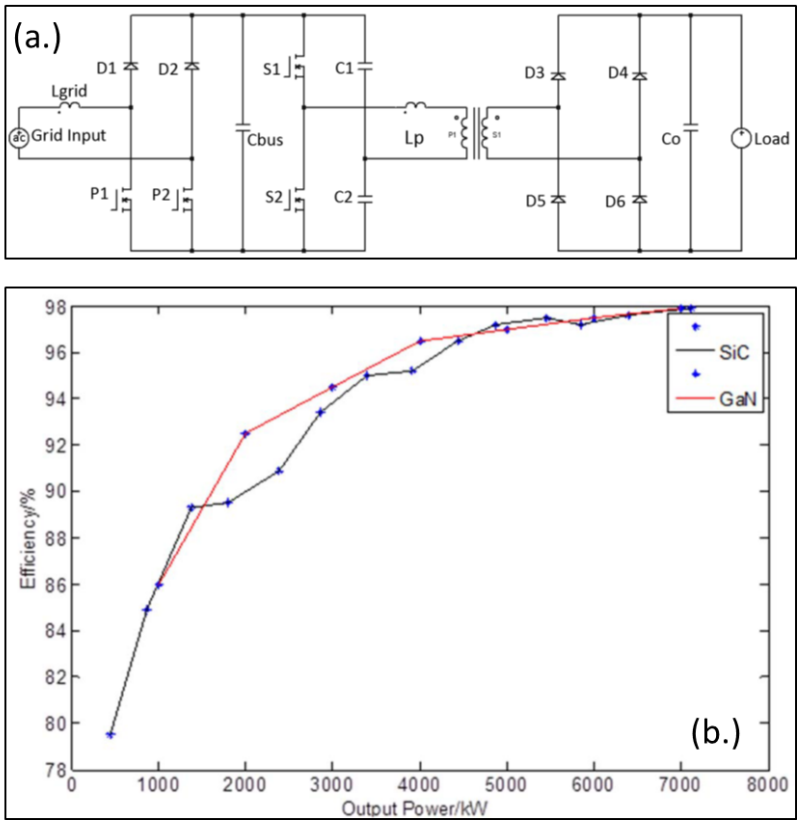



*Fig. 1. 25 (a.) Conventional isolated charger circuit diagram (b.) Experimental efficiency of GaN and SiC based charger at $V_{out}$ = 400 V, Power = 0.5~7.2 kW [71]*

### *b) Flexible AC Transmission System (FACTS)*

The primary goal of FACTS is to increase the power transmission capacity and maintain grid stability by controlling the reactive power flow to minimize losses and improve the system's ability to handle transients. Generally, Si thyristors and IGBTs are being incorporated into FACTS devices capable to switch thousands of amps at voltages of 1-10 kV [72]. FACTS devices include Static Synchronous Compensators (STATCOMs), Static Synchronous Series Compensators (SSCs), and Unified Power Flow Controllers (UPFCs), Static Var Compensator (SVC) and other thyristors based series and shunt compensators [73]. In 2021, Ma *et. al* demonstrated 2 kVA three-phase STATCOM system prototype based on GaN HEMTs based voltage-source inverter (VSI) functioning as a fast reactive power regulator [74].

### 1.3.10 Limitations of GaN-on-Si HEMTs for high voltage power electronics

In the last decade, GaN-on-Si HEMTs have demonstrated promising performance for developing high power switches with minimal losses and low cost. The lateral device architecture limits the high voltage applications of GaN-on-Si with major commercial devices available up to 650 V operation [75]. The major drawback of GaN-on-Si for high voltage applications is due to the lateral and vertical parasitic conduction in the epi-structure. The lateral leakage through the epi-layers and surface has been well controlled with the improved material quality, applying appropriate passivation and by introduction of high-k dielectrics. However, the vertical leakage towards the conductive substrate with the presence of parasitic channel at AlN/Si interface is a major concern, since the electric field crosses thick buffer and interlayers under high voltages [76]. Thus GaN-on-Si vertical leakage strictly limits the device performance in HV regime considering a typical buffer configuration. Moreover, the 3 MV/cm critical electric field limitation of GaN hinders pushing the lateral devices in high voltage regime which might be improved by implementing various field plate structures (multiple grated field plates, slanted field plates) that indeed increases the fabrication complexity [77], [78]. The high vertical field peak at the drain edge of the gate dominates the degradation of GaN HEMTs at high voltages by creating lattice damage due to inverse piezoelectric effect [79], [80]. For low frequency operation, conduction loss ($I^2R_{on,sp}$) is dominating. Considering these high voltage degradation mechanisms, increasing the bandgap of channel by introducing Al could contribute to increase the overall critical electric field strength of the devices that might push the devices in high voltage regime [81].

## 1.4 Power Device Figure of Merit

To understand the trend and impact of material parameters on the performance of devices, various figure of merits (FOM) have been formulated based on the conduction loss and /or switching loss. For power switching applications, the combination of high breakdown voltage ($V_B$) along with low specific on-resistance ($R_{on,sp}$) is necessary. The Baliga figure of merit (BFOM) compares materials by assuming that the unipolar power device loss is dominated by conduction loss applicable to vertical devices [82].

$$BFOM = \frac{V_B^2}{R_{on,sp}} = \varepsilon\mu E_c^3 \qquad (1.2)$$

Here, ε is the material specific dielectric constant, μ is the bulk electron mobility and $E_C$ is the critical electric field. Modern power electronic converters are targeted for smaller foot prints and increased power density. Thus, it can be beneficial to compare materials based on the device chip area, which can be compared by chip area figure of merit (HCAFOM) [83].

$$HCAFOM = \varepsilon E_c^2 \sqrt{\mu} \qquad (1.3)$$

Considering lateral device architecture, the flow of current is parallel to the cross-sectional area of the device. The breakdown voltage for a lateral device can be given by $V_B = E_c L$, where L is the channel length. The specific on-resistance for lateral devices can be given by

$$R_{on,sp} = R_{sh} \frac{L}{W} = \frac{L^2}{q\mu_{ch} n_s} \qquad (1.4)$$

Here, $R_{sh}$ is the sheet resistance ($R_{sh} = 1/ q\mu_{ch} n_s$), W is the channel width, q is the electron charge, $\mu_{ch}$ is the 2-DEG electron mobility and $n_s$ is the 2-DEG charge concentration. The lateral device figure of merit (LFOM) for power devices can be given by

$$LFOM = \frac{V_B^2}{R_{on,sp}} = q\mu_{ch} n_s E_c^2 \qquad (1.5)$$

The performance of lateral power devices made from various semiconductor materials can be evaluated by LFOM. Considering the BFOM and LFOM, the $\frac{V_B^2}{R_{on,sp}}$ is considered as FOM for power semiconductor devices. The comparison of material parameters and their FOM for various materials can be seen in Table 1.3. The BFOM and HCAFOM have been derived and normalized to GaN [84], [85]. It can be noted that in WBGs, GaN outperforms SiC and Si with a better FOM. However, the novel UWBG materials show excellent FOM portraying their advantages for high-performance power electronics with reduced device dimensions and increased power density. Considering AlGaN alloys, their estimated BFOM and HCAFOM reveals 2-10 times better performances as compared to GaN. Hence, AlGaN can be considered as a strong candidate for the development of high power density devices.

| Material | $E_G$ (eV) | $\varepsilon$ | $\mu$ (cm$^2$/V. s) | $E_c$ (MV/cm) | $\lambda$ (W/cm. K) | $V_S \times 10^7$ (cm/s) | BFOM | HCAFOM |
|---|---|---|---|---|---|---|---|---|
| Si | 1.12 | 11.9 | 1240 | 0.3 | 1.45 | 1 | 0.0003 | 0.01 |
| 4H-SiC | 3.23 | 9.7 | 980 | 3.1 | 3.7 | 2 | 0.224 | 0.5 |
| GaN | 3.4 | 10.4 | 1000 | 3-3.5 | 2.53 | 1.5-2 | 1 | 1 |
| AlN | 6.2 | 9.76 | 426 | 15-16 | 3.19 | 1.4 | 12 | 12.22 |
| $\beta$-$Ga_2O_3$ | 4.9 | 10 | 150 | 10.3 | 0.27 | 1.1 | 1.3 | 2.8 |
| Diamond | 5.5 | 5.7 | 2000 | 13 | 23 | 2.3 | 19.8 | 10.57 |

*Table 1. 3 Comparison of WBG and UWBG material properties along with their FOM*

# 1.5 UWBG semiconductor – Aluminium Gallium Nitride (AlGaN)

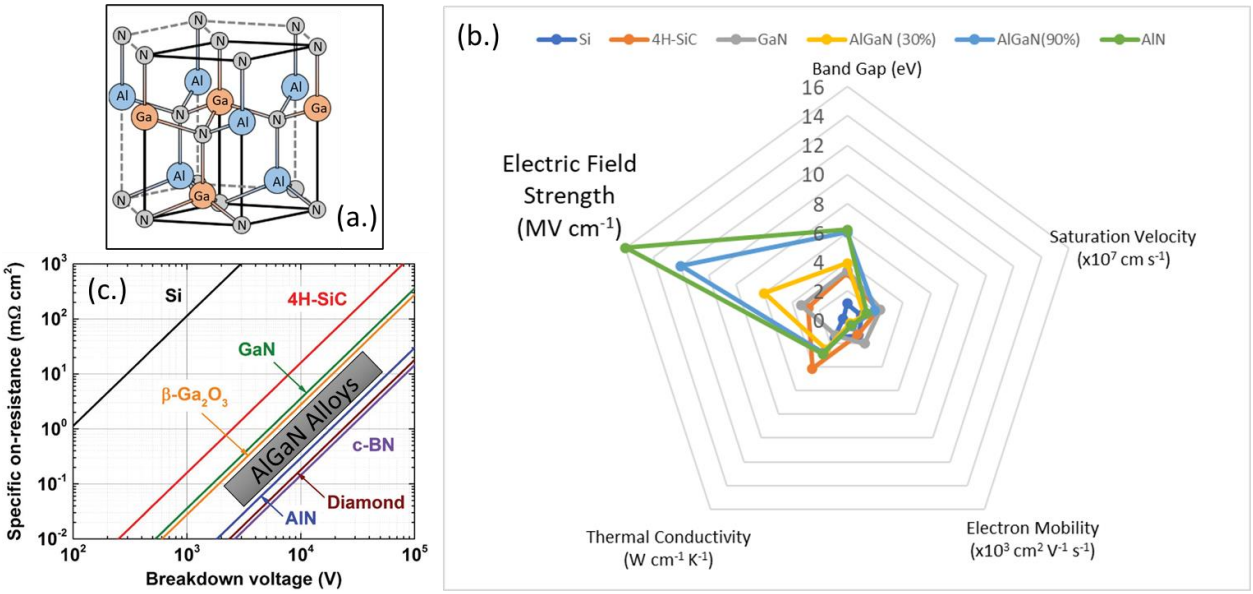



*Fig. 1. 26 (a.) Schematic of crystal structure for AlGaN with 60% Al content, (b.) Radar chart showing material properties of WBG semiconductors and AlGaN alloys and (c.) BFOM evolution for various WBG and UWBG semiconductors*

To enable multiple kilovolts operation of lateral FETs, UWBG materials ($E_g$ >3.4eV) are attractive since the blocking voltage capabilities scales with the material bandgap. $Al_xGa_{1-x}N$ alloys give control over Al composition offering a bandgap range of up to 6eV, therefore substantially improving the electric breakdown strength [84]. Since the late 2000s, AlGaN/AlGaN heterostructures have gained some attention for developing UWBG based heterostructure field effect transistors (HFETs) for high-voltage and high-temperature power electronics [86]–[89]. The typical atomic distribution probability of the wurtzite structure arrangement is represented in Fig. 1.26 (a.) for an AlGaN alloy with 60% Al composition. Fig 1.26 (b.) shows a radar chart highlighting the superior electric field strength

of AlGaN alloys over WBGs. The lattice parameters $a_0$ and $c_0$ of AlGaN alloys can be calculated based on the interpolation of GaN and AlN lattice parameters depending on the Al content, given by

$$a_0\ (Al_xGa_{1-x}N) = x.a_0\ (AlN) + (1-x).a_0\ (GaN) \quad (1.6)$$

$$c_0\ (Al_xGa_{1-x}N) = x.c_0\ (AlN) + (1-x).c_0\ (GaN) \quad (1.7)$$

The high electric breakdown field beyond the limits of GaN and tunable Al composition in the channel paves the way for AlGaN channel HFETs leading to devices with superior Baliga figure of merit (BFOM) [90]. The BFOM evolution represented by the specific on-resistance and breakdown voltage of various semiconductors shows that AlGaN alloys can offer significantly higher performances compared to GaN and SiC (see fig 1.26 (c.)). The spontaneous and piezoelectric polarization by using AlGaN as a channel and barrier can be exploited to form a 2-DEG or 2-DHG. For a 2-DEG formation in $Al_XGa_{1-X}N/Al_YGa_{1-Y}N$ heterostructures, X>Y strictly. The example of a 1-D Schrödinger-Poisson solver to extract the generated 2-DEG charge concentration using Nextnano software is shown in Fig. 1. 27. The structure used for simulation is composed of a 450 nm AlGaN channel followed by a 15nm AlGaN barrier along with a 1nm AlN in between to conclude the AlN/AlGaN heterostructures. The effect of increasing AlN spacer thickness can be observed with a reduction in 2-DEG density. These results of 2-DEG density are without consideration of surface states. Hence, we can use AlGaN/AlGaN heterostructures to develop a field effect transistor with a 2-DEG density of around $10^{13}$ $cm^{-2}$. However, the electron mobility drops significantly due to alloy scattering. More details on electron transport in AlGaN/ AlGaN HFETs will be shown in Chapter 3. The three structures selected for the fabrication of AlGaN channel HFETs on silicon presented later are selected based on this matrix assuming similar 2-DEG concentration for various Al compositions in the channel.

| Barrier-Al (X%) | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 | 80 | 90 | 100 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Channel-Al (X%) | 2D Electron Gas Concentration (× $10^{13}$ $cm^2$) | | | | | | | | | | |
| **0** | X | 0.218 | 0.51 | 0.89 | 1.34 | 1.90 | 2.62 | 3.50 | 4.51 | 5.63 | 6.85 |
| **10** | X | X | 0.24 | 0.59 | 1.03 | 1.55 | 2.23 | 3.08 | 4.09 | 5.20 | 6.44 |
| **20** | X | X | X | 0.26 | 0.67 | 1.17 | 1.79 | 2.59 | 3.56 | 4.67 | 5.92 |
| **30** | X | X | X | X | 0.28 | 0.75 | 1.33 | 2.04 | 2.96 | 4.07 | 5.30 |
| **40** | X | X | X | X | X | 0.30 | 0.83 | 1.49 | 2.33 | 3.37 | 4.57 |
| **50** | X | X | X | X | X | X | 0.32 | 0.92 | 1.65 | 2.61 | 3.75 |
| **60** | X | X | X | X | X | X | X | 0.34 | 1.00 | 1.82 | 2.88 |
| **70** | X | X | X | X | X | X | X | X | 0.36 | 1.09 | 2.00 |
| **80** | X | X | X | X | X | X | X | X | X | 0.37 | 1.16 |
| **90** | X | X | X | X | X | X | X | X | X | X | 0.38 |
| **100** | X | X | X | X | X | X | X | X | X | X | X |

*Fig. 1. 27 Simulated AlGaN/AlGaN Matrix showing the 2-DEG concentration per $cm^2$ for various Al content in the barrier and channel*

## 1.6 Towards State-of-the-Art AlGaN channel HFETs

In 2008, Nanjo and colleagues from Mitsubishi Electric Corporation, Japan pioneered the development of AlGaN channel HFETs by incorporating 20% Al into the channel layer, achieving a peak drain current of 130 mA/mm at a gate-source voltage of +2 V on a sapphire substrate [81]. Subsequently, they also demonstrated AlGaN channel HFETs, which exhibited an impressive breakdown voltage of 1650 V across a 10 µm gate-drain spacing [86]. In 2010, Tokuda and his team introduced $Al_{0.86}Ga_{0.14}N/Al_{0.51}Ga_{0.49}N$ HFETs on a freestanding AlN substrate, showing a breakdown voltage of 1800 V for a 15µm gate-drain spacing and a maximum drain current density of 25.2 mA/mm [87]. The early demonstration of high breakdown voltages (> 1200 V) set a benchmark showing the potential of AlGaN channel HFETs for high-power applications. However, one of the major challenges of AlGaN channel HFETs is to optimize source-drain ohmic contacts to achieve high current density

(comparable or at least close to that of GaN) especially when using higher Al mole fraction in the channel [91]. The following year, Hashimoto's group reported an $Al_{0.89}Ga_{0.11}N/Al_{0.51}Ga_{0.49}N$ HFET with a high 2-DEG carrier concentration of $2.48 \times 10^{13}$ $cm^{-2}$ on both sapphire and AlN substrates [92]. In 2016, Baca et. al developed $AlN/Al_{0.85}Ga_{0.15}N$ HFETs on sapphire, demonstrating low gate leakage and a high on/off current ratio exceeding $10^7$, along with a breakdown voltage of 800 V [93]. They further showed the temperature stability of $Al_{0.85}Ga_{0.15}N/Al_{0.70}Ga_{0.30}N$ HFETs on sapphire substrates across a -50°C to 200°C range in 2017 [89]. In 2019, Douglas et al. showcased enhancement-mode $Al_{0.45}Ga_{0.55}N/Al_{0.30}Ga_{0.70}N$ HFETs with a p-$Al_{0.30}Ga_{0.70}N$ gate, achieving a threshold voltage of + 0.3 V for a 3 μm gate length [94].

In 2019, Sandia National Laboratories, USA demonstrated extreme temperature operation of $Al_{0.85}Ga_{0.15}N/Al_{0.7}Ga_{0.3}N$ HEMTs with 58% reduction in DC output with low off-state leakage current at 500°C along with minimal loss in switching current [95]. The high-temperature operation up to 500°C reveals robust performance of AlGaN channel HFETs which is not possible to achieve with GaN HEMTs. Razzak and his team designed compositionally graded drain-source contacts for $Al_{0.75}Ga_{0.25}N$ channel HFETs on AlN, achieving a maximum drain current density of 635 mA/mm and low contact resistance of $3.3\times10^{-5}$ $\Omega\cdot cm^2$ [96]. In 2021, Abid et al. demonstrated $AlN/Al_{0.50}Ga_{0.50}N$ HEMTs on sapphire with n+ GaN regrowth drain-source contacts, with a breakdown voltage exceeding 4400 V and a maximum drain current density of 100 mA/mm, supported by a buffer breakdown field as high as 5 MV/cm [97]. In 2022, a detailed study on the charge control and transport properties of polarization-induced 2-DEGs in AlN/AlGaN/AlN double heterostructures with Al mole fraction up to 0.74 has been shown by Singhal et al. giving an overview of alloy scattering based on temperature-dependent transport properties [98]. Hence, the 2-DEG properties and overall crystal quality of AlGaN/AlGaN heterostructures can be improved by employing bulk AlN substrates. Later they demonstrated $Al_{0.25}Ga_{0.75}N$ channel HFETs with 0.23 Ω.mm contact resistance with a maximum drain current density of 280 mA/mm [99]. In 2023, Mamun et. al showed the operation of $Al_{0.64}Ga_{0.36}N$ channel HFETs on AlN with low ohmic contact resistance of 4.3 Ω.mm giving a peak drain current of 610 mA/mm along with a high 3-terminal breakdown field of 3.74 MV/cm resulting in a BFOM of 460 $MW/cm^2$ [100].

These developments underscore a continued focus on optimizing AlGaN channel HEMTs, predominantly on sapphire or bulk AlN substrates, with limited exploration into cost-effective, large-diameter silicon substrates. These results demonstrate the high electric field strength capabilities of AlGaN alloys that clearly surpass the theoretical limitation of GaN HEMTs. The state-of-the-art AlGaN channel devices are illustrated in Fig. 1.28 demonstrating the evolution of maximum on-state current ($I_{DSMax}$) against the breakdown voltage represented by their respective Al composition in the channel [86], [89], [90], [93], [96], [97], [101]–[106].

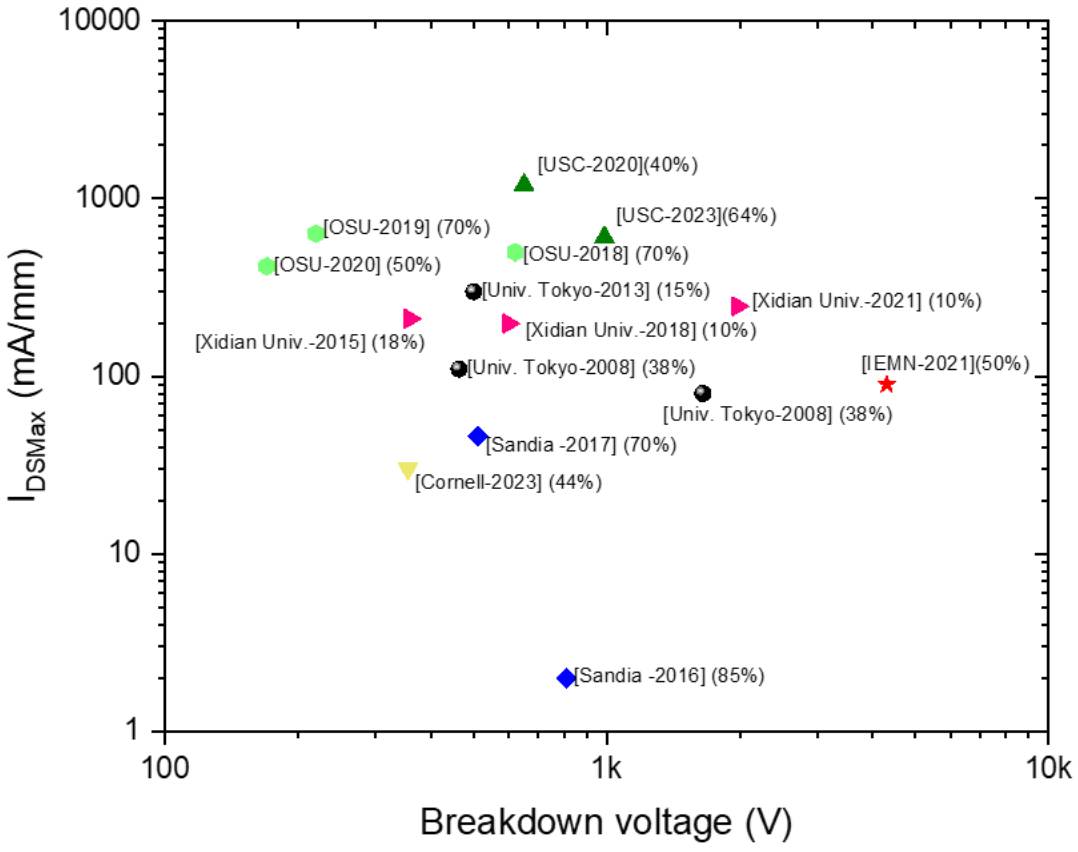



*Fig. 1. 28 State-of-the-art AlGaN channel devices*

# *Chapter-02 Bulk AlN Substrate for High Voltage Power Electronics*

GaN-on-Si technology has been leading the FETs industry for the development of fast switching devices, which can sustain high voltages while maintaining low on-resistances. Commercial E-mode GaN devices are available in the market in present days that can withstand up to 1200 V with high-temperature operation capabilities reaching 150°C [107]–[110]. Since lateral GaN devices do not show avalanche breakdown, there is still room to squeeze out the material-specific capabilities of GaN to obtain fast switching reaching the kilovolt regime. However, *are silicon substrates sufficient to reach the kilovolt (> 1200 V) regime with lateral device architecture?*

Firstly, the growth of GaN-on-Si comes with many challenges such as high lattice mismatch of 16% along with the drawback of high thermal mismatch that is up to 54% [111], [112]. These issues become highly challenging for the epitaxy growers in order to create low density of defects in the GaN channel and uniform high-quality epi-structure yield on large wafer diameters. This becomes worse with sapphire substrates due the lower thermal dissipation making it unsuitable for high-temperature operation [113]. Secondly, one might consider using SiC substrates that have only 3.5% and 30% of lattice and thermal mismatch respectively, enabling high-quality heterostructures as adopted for RF applications. However, the limited critical electric field strength of SiC substrates hinder their application to reach the multiple kV regime using GaN lateral device architecture with submicron thick epitaxy [114]. Thus, one might think *is there any possibility of reaching multiple kilovolt operation using conventional AlGaN/GaN heterostructures?*

This is where bulk Aluminum Nitride substrates come into play with their exceptional insulating properties with a critical electric breakdown field capable of reaching 15 MV/cm along with low lattice and thermal mismatch as well as high thermal conductivity, which are quite comparable to SiC substrates [115]. This chapter describes the MIS-HEMT fabrication and electrical performances of AlGaN/GaN heterostructures grown on bulk AlN substrates. This study will eventually show the GaN channel downscaling experiments by varying the GaN channel layer thickness from 500 nm to 8 nm grown on bulk AlN. The exploitation of DC and high voltage performances of these devices are discussed with respect to their specific challenges and limitations that can eventually lead to state-of-the-art GaN HEMTs on bulk AlN.

## 2.1 Bulk Aluminum Nitride substrate for power electronics

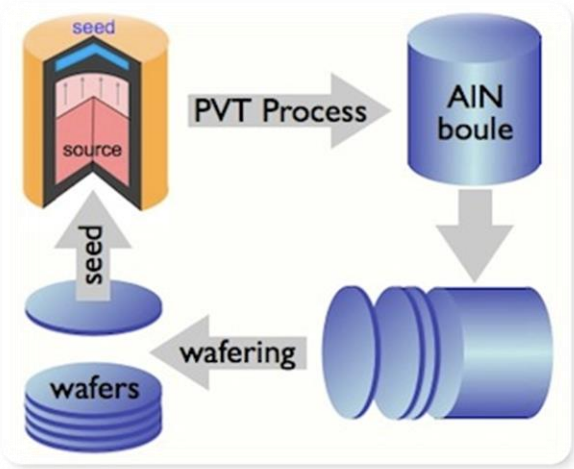



*Fig. 2. 1 Bulk AlN wafer processing flow diagram*

Aluminum Nitride (AlN) material has been widely used in the micro/nano-fabrication of power electronics due to its excellent electrical insulation and high thermal conductivity up to 300 W/m.K. It could be used for a broad range of applications from ceramics used for device packaging to monolayers for thermal dissipation in high power electronics applications [116]–[119]. This led to the development of bulk AlN crystals from seed using the physical vapor transport (PVT) process to obtain high-quality substrates (see Fig 2.1). The C-plane 400 µm thick AlN substrates used in this work have been commercially purchased from HexaTech, Inc., which provides high quality wafers with dislocation density $< 10^4$ $cm^{-2}$ [120], [121]. AlN provides a better platform for the growth of GaN/AlGaN

hetero!structures due to its low lattice mismatch typically < 3% along with low thermal mismatch. On top of this, with the virtue of its critical electric field of up to 16 MV/cm, AlN stands as a promising candidate for GaN/AlGaN based heteroepitaxy suitable for high voltage power electronics.

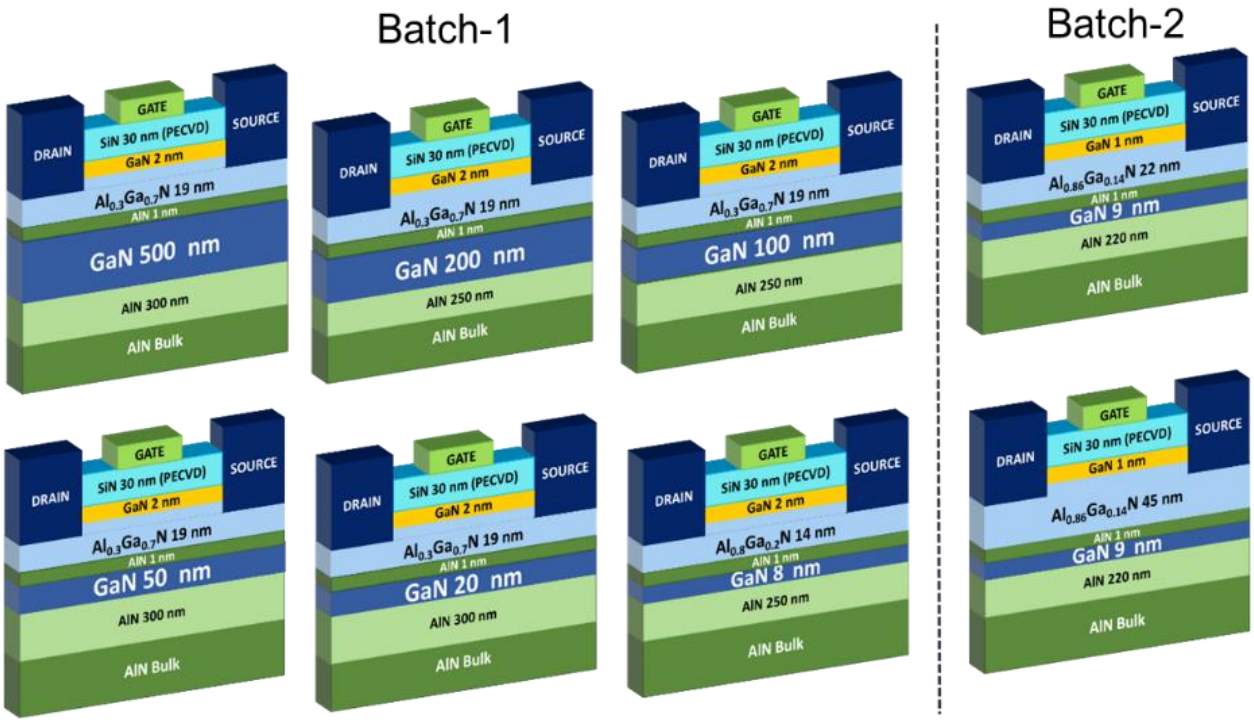



*Fig. 2. 2 Cross-sectional schematic structures of fabricated GaN channel MISHEMTs on AlN*

## 2.2 Fabrication of GaN channel MIS-HEMTs on bulk AlN substrate

To evaluate the effect of the GaN channel thickness on structural and electrical properties, a series of HEMT structures were grown by ammonia source molecular beam epitaxy ($NH_3$-MBE) in a Riber Compact 21 reactor with a thin AlN buffer layer and GaN channel of thickness varying from 500 nm to 8 nm. Typical AlGaN barrier of 19 nm thick and 30% Al content along with 1 nm AlN spacer was grown on top of GaN channel followed by a 2nm GaN cap as shown in Fig.2.2. A device with 82% Al content in the 14 nm thick AlGaN barrier with 8 nm GaN channel was also grown. The conduction band energy diagram of various GaN channel thicknesses is shown in Fig.2.3. The reduction in quantum well peak below the Fermi level can be justified by the reduction of polarization charges with channel downscaling that can be verified by Hall Effect measurements. The band diagram of

heterostructures were simulated with 1-D Poisson-Schrödinger solver using the software nextnano. The simulations revealed the quantum well of an 8nm thin GaN channel rose above the fermi level considering fully relaxed GaN channel, indicating the absence of 2DEG. This absence of 2DEG might be compensated by adapting a thick Al-rich AlGaN barrier [122], which can be confirmed by the conduction band edge profile of 9 nm GaN channel HEMT. Hence, another batch based on 9 nm thin GaN channel was grown followed by a 22 nm and 45 nm AlGaN channel with 86% Al composition.

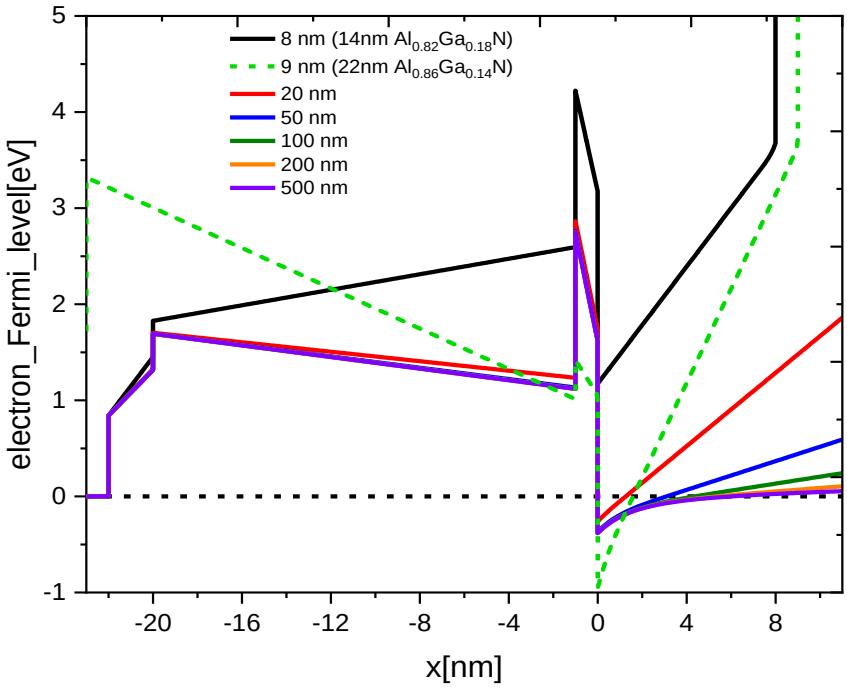



*Fig. 2. 3 Conduction band profile for relaxed GaN channel HEMTs with various thickness*

## 2.2.1 Structural characterization

The AFM characterization of the structures reveals a change in the surface morphology while reducing the GaN channel thickness, with root mean square (RMS) roughness progressively reduced from about 1 nm to less than 0.15 nm. The kinetic roughening induced growth mounds can be observed for 500 nm GaN channel that varies to a step flow growth morphology for ≤ 50 nm thin GaN channel as shown in Fig. 2.5. The FWHM of XRD rocking curves reveals the sharp AlN peaks revealing the high crystalline quality of AlN substrates along with low threading dislocation density (see Fig.2.4 [Top]). The broadening of the diffraction peaks of GaN XRD curves with reduction in channel thickness

indicates the degradation of GaN crystal quality. The GaN channel relaxation rate changes drastically from 0-50% for 50 nm thick GaN channel, which goes all the way to 100% for 500nm thick GaN channel. Thus, 20-50 nm thickness of GaN channel shows a high change in the strain relaxation rate.

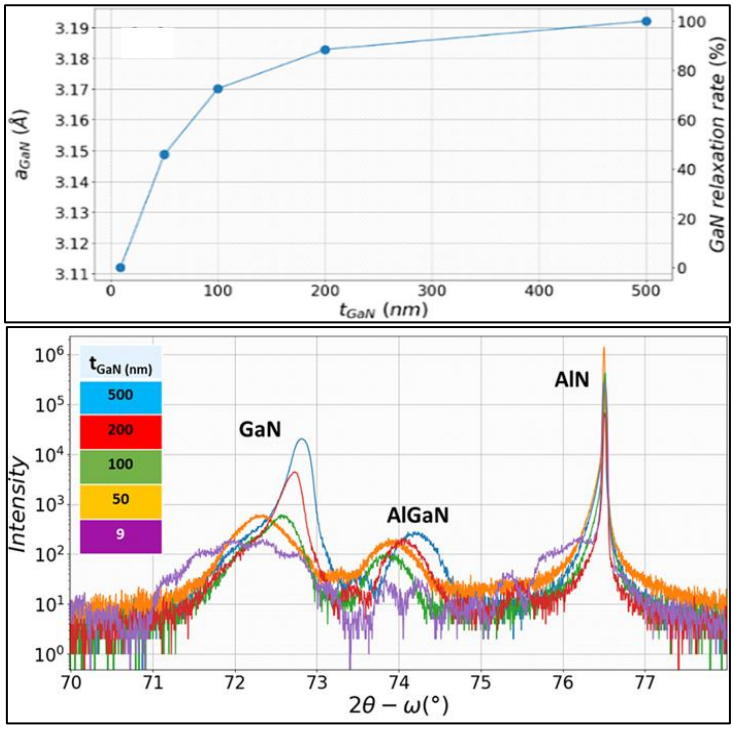



*Fig. 2. 4 Evolution of strain relaxation rate with GaN channel thickness [Top], XRD 2theta-omega scans performed around (004) reflections for various GaN channel HEMTs [Bottom]*

The Scanning transmission electron microscopy (STEM) was performed on FIB (focused ion beam) prepared sample cross sections using a FEI-Tecnai operated at 200 kV. High angle annular dark field (HAADF) STEM images shows a change in the contrast and a decrease in the defect density above 20–30 nm thick region from the GaN/AlN interface as seen in Fig. 2.6. Moreover, an additional transition region with a slower change in the

dislocation arrangement can be observed in the 500 nm channel at around 200 nm from the GaN/AlN interface, which is usually observed in GaN-on-Si epitaxy.

This hypothesis shows that the channel thickness downscaling increases the GaN channel compressive strain with a compromise to being closer to highly defective nucleation region close to GaN/AlN interface whose critical thickness can be estimated around 10 nm [123]. This strain increment with GaN channel thickness downscaling will eventually increase the in-plane lattice mismatch with 30% Al content AlGaN barrier. This might induce cracks, eventually concluding necessity of pseudomorphic growth as shown by XRD measurements.

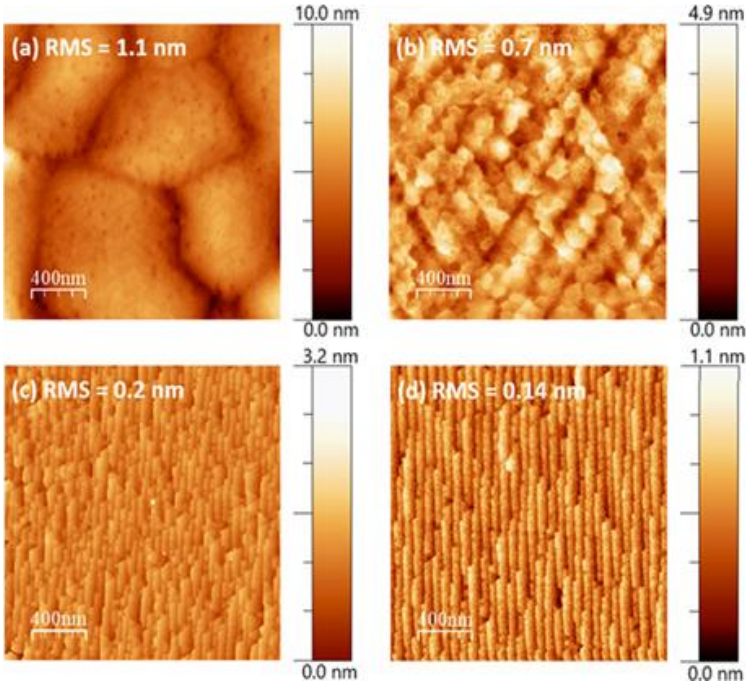



*Fig. 2. 5 AFM images of the surface of HEMTs with (a) 500nm, (b) 50nm, (c) 20nm and (d) 8nm GaN channel thickness.*

Due to this reason, a high Al content has to be introduced in the barrier in order to keep the in-plane lattice parameter close to AlN [123]. This led to growth of thick AlGaN barrier on thin GaN channel configuration for obtaining a crack free structure. Hence, the second batch of structures comprises a 9 nm GaN channel along with a 22 nm and 45 nm AlGaN barrier with 86% Al content [see Fig 2.2] on bulk AlN.

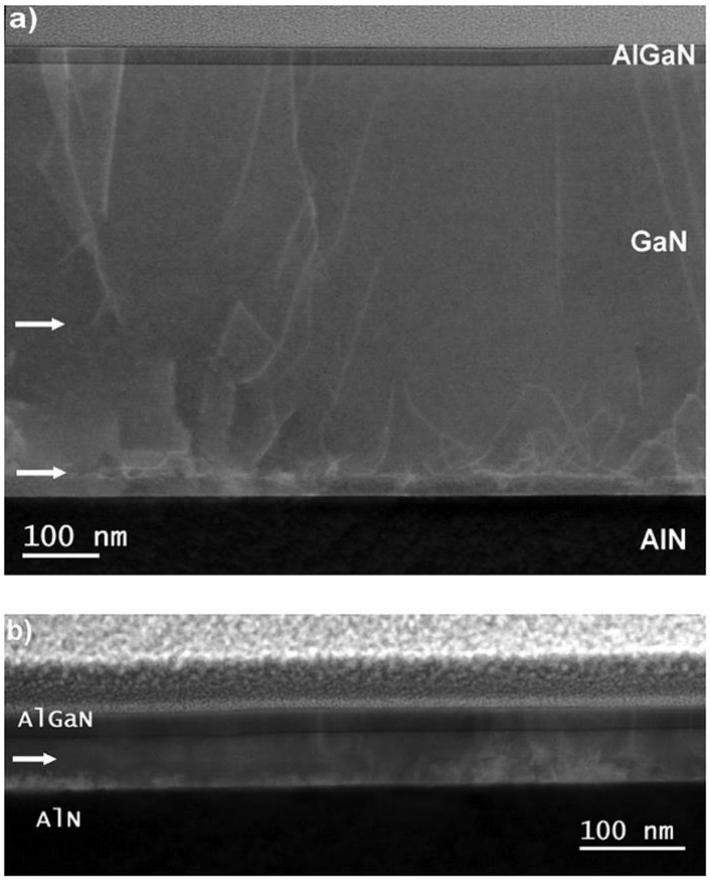



*Fig. 2. 6 Cross-sectional high angle annular dark field (HAADF)-STEM images of HEMT structures grown on the AlN substrate with GaN channel thicknesses of 500 (a) and 50 nm (b). The white arrow close to the GaN/AlN interface shows the upper limit of the first transition region in (a) and (b). The second arrow in (a) is located at about 200 nm above the first transition region and corresponds to an additional decrease in the defect density.*

## 2.2.2 Device fabrication

The device fabrication started with the development of source/drain ohmic contacts by e-beam evaporation of Ti/Al/Ni/Au metal stack after partial barrier etching using $Cl_2$/Ar and $BCl_3/SF_6$ chemistry with ICP-RIE tool. The devices were subjected to rapid thermal annealing (RTA) at 825°C for the devices with 30% Al composition in AlGaN barrier and 850°C for the devices with > 80% Al composition in AlGaN barrier under constant nitrogen flow. The active area of all devices were mesa isolated down to the AlN layer by $Cl_2$/Ar plasma using ICP-RIE. A 30 nm thin layer of SiN was deposited using plasma enhanced chemical vapor deposition (PECVD) at 340°C followed by evaporation of Ni/Au gates. Finally, Ti/Au pads were evaporated concluding the fabrication of MIS-HEMTs. The fabricated transistor design is as follow: $L_G$ = 3 µm, $L_{GD}$ from 5 – 40 µm and $W_G$ = 50 µm.

## 2.3 DC characterization

### 2.3.1 Impact of GaN channel thickness on 2DEG

Hall Effect measurements on van der Pauw pattern shows the degradation of electron mobility in the 2DEG with GaN channel downscaling, which is due to the increase in scattering effects linked to the roughness of GaN interfaces and also partially due to electron trapping since the 2-DEG gets closer to the defective GaN/AlN interface [124]. The electron mobility of the 2-DEG reduces from almost 2000 $cm^2/V.s$ for 500 nm thick GaN channel to less than 500 $cm^2/V.s$ for 50 nm thick GaN channel structures. The electron trapping might also contribute to the reduction in 2DEG density alongside the reduction in the polarization discontinuity due to the increasing strain in thinner GaN channels as shown in Table 2.1. This leads to loss of 2DEG charges all the way from $10^{13}$ $cm^{-2}$ to $2\times10^{12}$ $cm^{-2}$ while downscaling GaN channel thickness from 500nm to 8nm, respectively. GaN channel thickness reduction also brings challenge for the ohmic contact formation to the 2DEG. Fig.2.7 shows I-V characteristics of TLM bar with a 5µm contact spacing for various GaN channel HEMTs. The trend shows 4 times reduction in current while reducing from 500 nm to 50 nm the GaN channel thicknesses. For devices below 50 nm GaN channel, the non-ohmic behavior of the contacts starts appearing mainly due to implementation of Al-rich AlGaN barrier that leads to higher concentration of native oxide formation on the surface. The contact to 2DEG in thin

| GaN Channel Thickness (nm) | GaN relaxation rate (%) | Hall electron mobility ($cm^2/V.s$) | 2-DEG density ($10^{13}$ $cm^{-2}$) | Sheet Resistance (Ω/Sq.) | Contact Resistance (Ω.mm) |
|---|---|---|---|---|---|
| 500 | 100 | 1920 | 1 | 330 | 0.147 |
| 200 | 88 | 1700 | 0.9 | 410 | 0.48 |
| 100 | 72 | 930 | 0.8 | 840 | 3.2 |
| 50 | 50 | 460 | 0.78 | 1700 | 0.92 |
| 20 | 8 | 310 | 0.22 | 9000 | - |
| 8 | 0 | 149 | 0.2 | 21500 | - |
| 9 | 0 | 480 | 1.2 | 1050 | - |
| 9 | 0 | 450 | 1.6 | 880 | - |

*Table 2. 1 Hall Effect Measurements, Contact Resistance and channel relaxation rate for various GaN channel HEMTs*

GaN channel devices may be improved by using n+ GaN regrowth strategy and/or by implementation of different metal stacks [93], [97], [102], [125], [126].

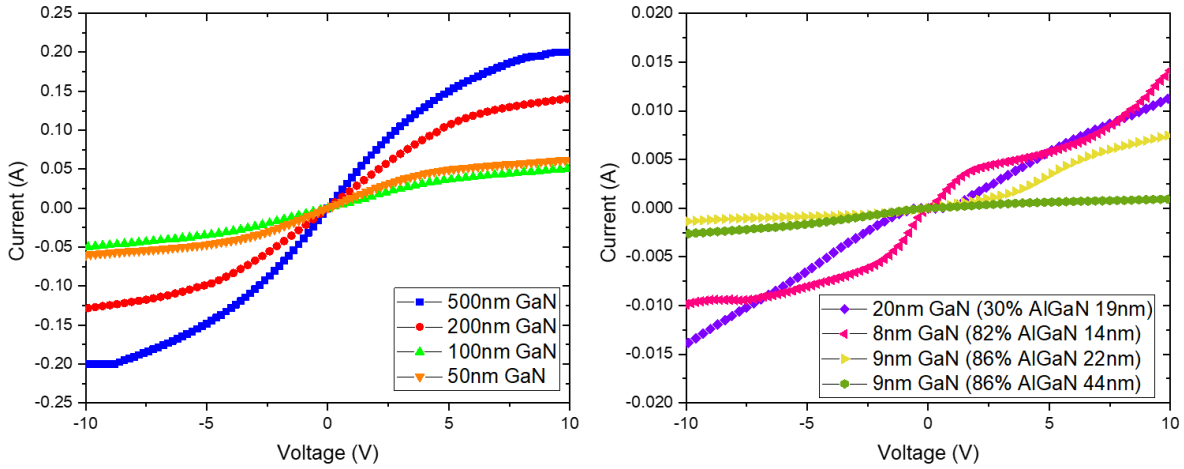



*Fig. 2. 7 Current-Voltage characteristics of various GaN channel HEMTs for 5µm TLM contact spacing*

## 2.3.2 Transfer Characteristics

Transfer characteristics for different GaN channel thicknesses are shown in Fig. 2.8. Back and forth sweeps of the drain and gate currents at different gate biases and fixed drain bias of 10 V provides indications of trapping effects through the hysteresis $I_d$-$V_g$ characteristics. Majority of the devices until 50 nm thick GaN channel showed low off-state leakage current and high on-state current, which is in agreement with their sheet resistance evolution. The forward-reverse $I_d$-$V_g$ sweeps shows increase in the positive shift in threshold voltage while reducing the GaN channel thickness. This indicates the charge-trapping effects below the

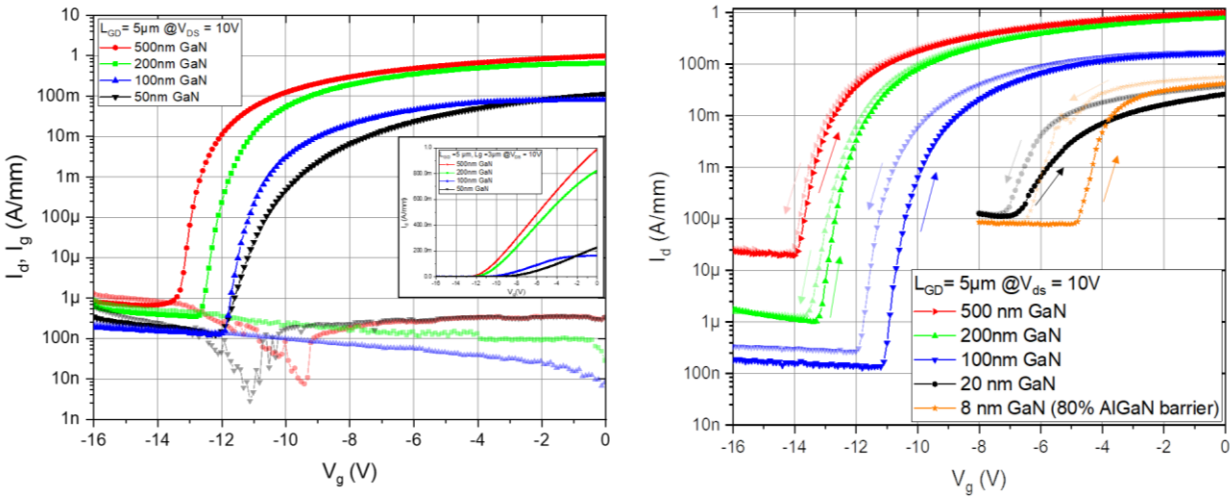



*Fig. 2. 8 [Left] Transfer characteristics of GaN HEMTs with 500nm, 200nm, 100nm and 50nm channel thickness in semi-log and linear scale and [Right] Forward-Reverse Id-Vg sweeps for various GaN channel HEMTs*

gate that is typically generated within the layers above 2-DEG. The $I_d$-$V_g$ hysteresis in 8 nm GaN channel device double sweep resembles to high trapping in the Al-rich barrier typically caused by higher lattice mismatch with GaN and the closeness of 2DEG to the defective GaN/AlN interface.

### 2.3.3 Output Characteristics

The DC output characteristics of a 2×50 µm GaN channel HEMTs with various channel thickness for devices with $L_{GD}$ = 5 µm and $L_G$ = 3 µm are shown in Fig. 2.9, 2.10, and 2.11. The maximum drain current density evolves from 1.1 A/mm to 150 mA/mm for 500nm and 50 nm GaN channel HEMTs respectively, which is in accordance with increase in their static on-resistance from 0.5 mΩ.cm$^2$ to 4 mΩ. cm$^2$. The reduction of maximum drain current density in thin GaN channel HEMTs can be justified by the decrease in 2DEG mobility and degradation in ohmic contacts. However, the output characteristics showed Schottky turn-on behavior for the devices with GaN channel thickness below 20 nm indicating the challenge to obtain ohmic behavior of source/drain contacts.

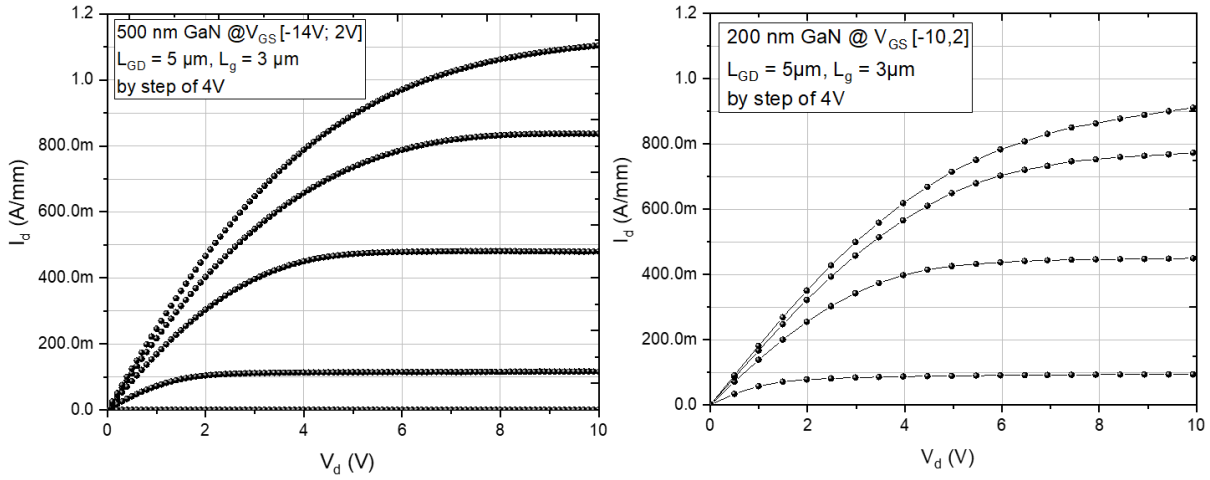



*Fig. 2. 9 Output characteristics for 500 nm and 200 nm thick GaN channel MISHEMTs*

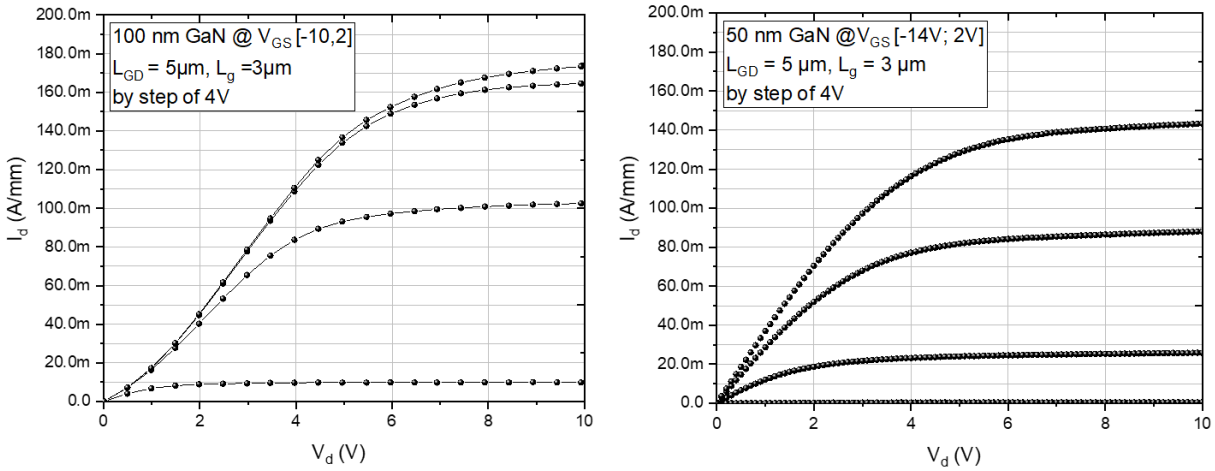



*Fig. 2. 11 Output characteristics for 100nm and 50nm thick GaN channel MISHEMTs*

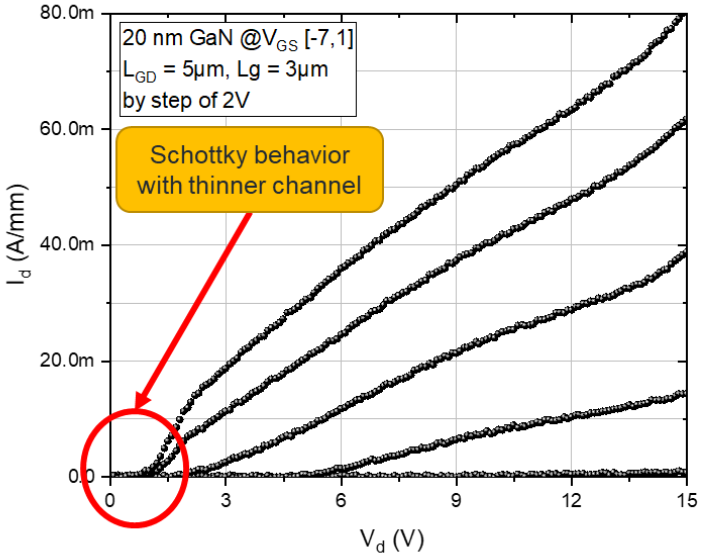



*Fig. 2. 10 Output characteristics 20nm thin GaN channel HEMTs*

## 2.3.4 Buffer breakdown measurements

The high voltage measurements were realized using Keysight N1268A Ultra High Voltage Expander Unit (UHVU) operating in conjunction with a Keysight B1505A Power Device Analyzer / Curve Tracer. The samples were immersed in fluorinert-FC40 liquid during the measurements to avoid arcing in air. Fig. 2.12 shows the lateral buffer BV between 100 × 100 $\mu$m isolated ohmic contacts with various distances. The left plot shows the leakage current density below 1 $\mu$A/mm for 96 $\mu$m contact spacing up to 6 kV and 9 kV for 500nm

and 8 nm thick GaN channel respectively, revealing the absence of parasitic leakage through mesa sidewalls. A buffer breakdown electric field of more than 7 MV/cm was measured for low contact spacing which is well beyond the electrical breakdown field measured on the devices grown on other substrates [38], [40], [127]. However, a drop in the buffer breakdown field can be observed in Fig. 2.13 [left] corresponding to the increased defect density with contact spacing. The evolution of buffer breakdown voltage with two terminal contact spacing for various GaN channel devices as shown in Fig. 2.13 [right] reveals the superior voltage blocking capability of AlN substrate.

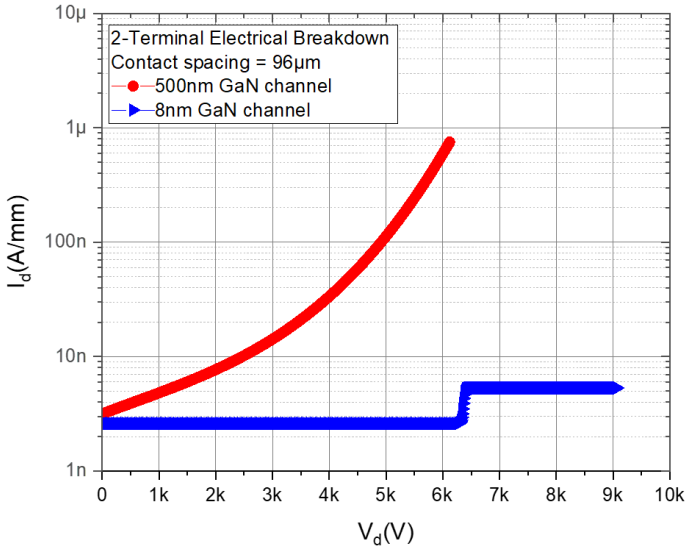



*Fig. 2. 13 Buffer leakage current characteristics for 500nm and 8nm GaN channel devices with 96µm contact spacing*

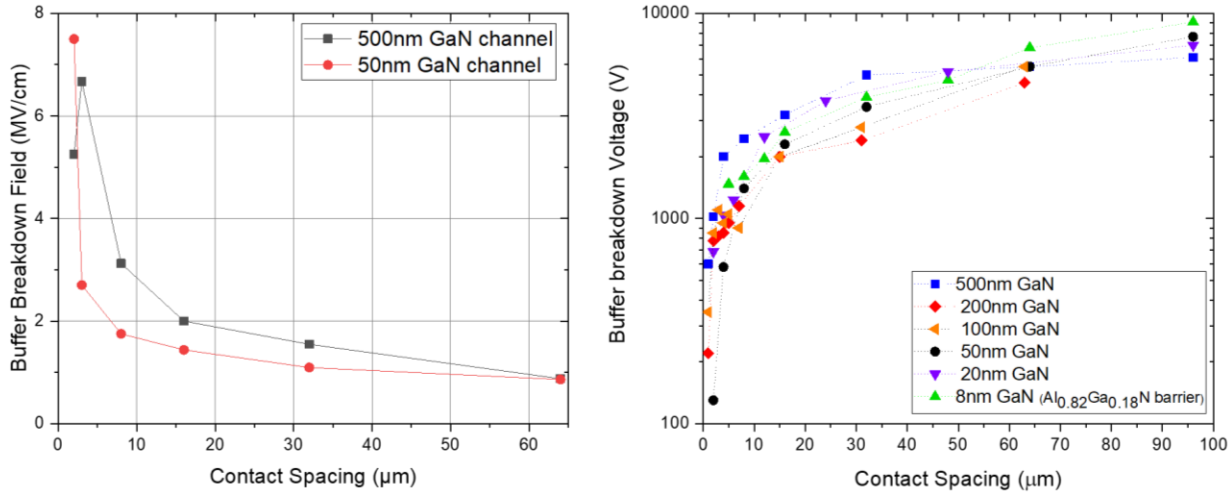



*Fig. 2. 12 [Left] Evolution of buffer breakdown electric field with two terminal contact spacings and [Right] Summary of AlN breakdown voltage with various contact spacings*

## 2.3.5 Transistor breakdown measurements

The three-terminal breakdown behavior of transistors fabricated with $L_{GD}$ = 40 $\mu$m and $L_G$ = 3 µm on HEMT structures with 500 nm, and 50 nm thick GaN channels is shown in Fig. 1.14. Interestingly, the 50 nm channel transistor delivered about 10 times higher breakdown voltage (BV) (defined at 100 $\mu$A/mm) than the 500 nm thick channel and reached more than 1400 V with static $R_{on}$ = 32 mΩ cm$^2$. The 20 nm GaN channel device showed hard breakdown up to 3000 V but with high gate leakage as shown in Fig. 2.15 [left], which is typically coming from top epilayers. Similarly, the 8 nm GaN channel devices showed very high leakage resulting in unreliable electrical measurements. The scaling of devices with off-state leakage current below 100 µA/mm is shown in Fig. 2.15 [right] with different gate-drain spacings. The present results also show that none of the two structures suffers electron injection into the AlN substrate unlike GaN-on-Si devices [128], [129]. These high voltage performances pave the way for devices able to switch multiple kilovolts using bulk AlN substrate and thin GaN channel configuration owing to the epitaxial challenges.

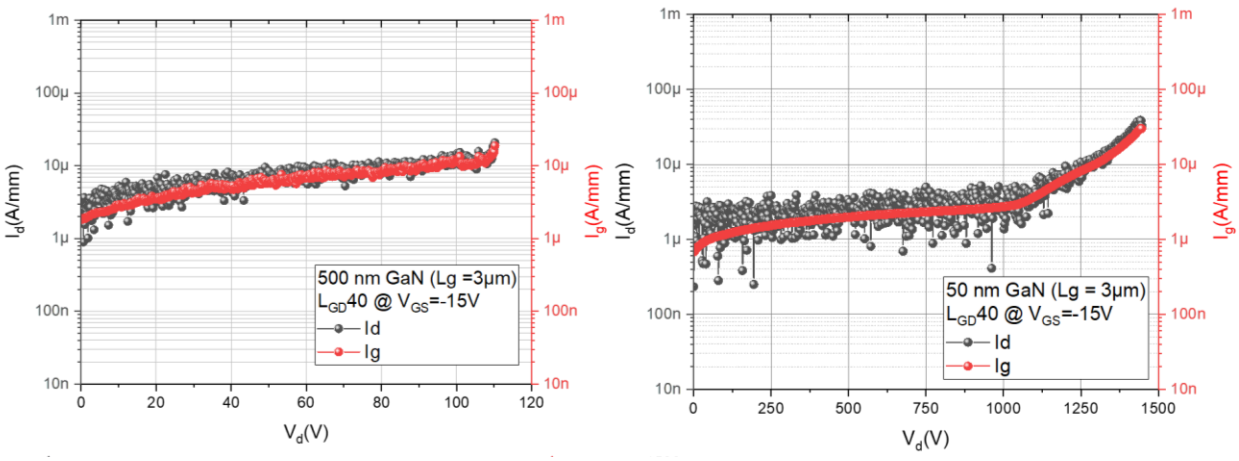



*Fig. 2. 14 Transistor breakdown characteristics for MISHEMTs with Lgd = 40 µm and Lg = 3 µm for [Left] 500 nm thick GaN channel and [Right] 50 nm thin GaN channel*

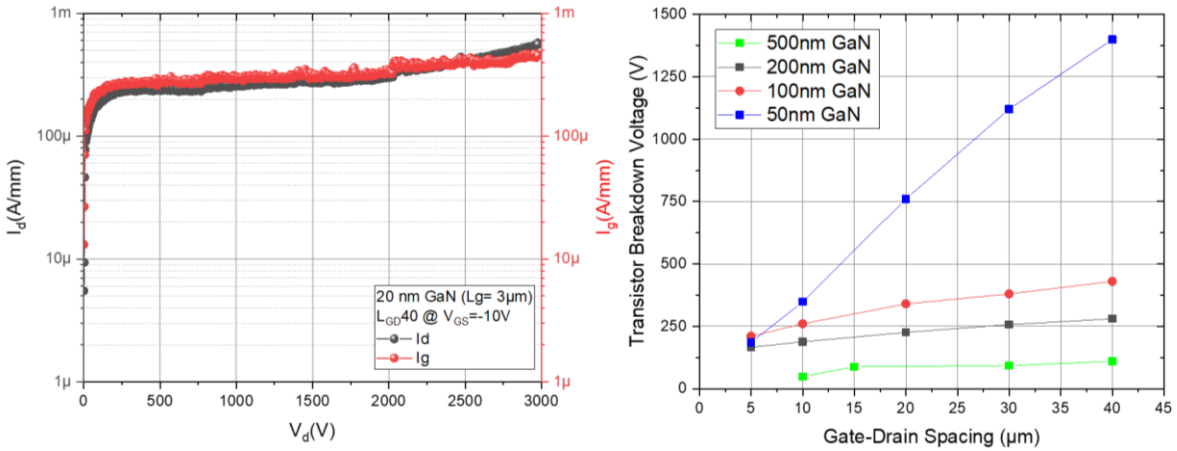



*Fig. 2. 15 [Left] Transistor breakdown characteristics for MISHEMTs with $L_{GD}$=40µm and $L_G$=3µm for 200nm thick GaN channel and [Right] Summary of transistor breakdown voltage with various gate-drain spacing for different GaN channel MISHEMTs with gate leakage below 100µA/mm*

## 2.4 Electric Field Imaging in GaN-on-AlN MISHEMTs

In collaboration with NEEL-CNRS, Grenoble, we performed a detailed analysis of electron beam-induced current to investigate the effect of the GaN channel thickness on the breakdown mechanisms. The two samples previously analyzed by TEM (500 nm and 50 nm GaN channel devices) were measured in a scanning electron microscopy (SEM, FEI F80) system. The measurement was performed at room temperature (300 K). The electron beam irradiation was performed under vacuum at $1.9\times10^{-6}$ Torr. The energy loss between the e-Gun and the sample was negligible. Electron beams at the accelerating voltages of 15 kV were

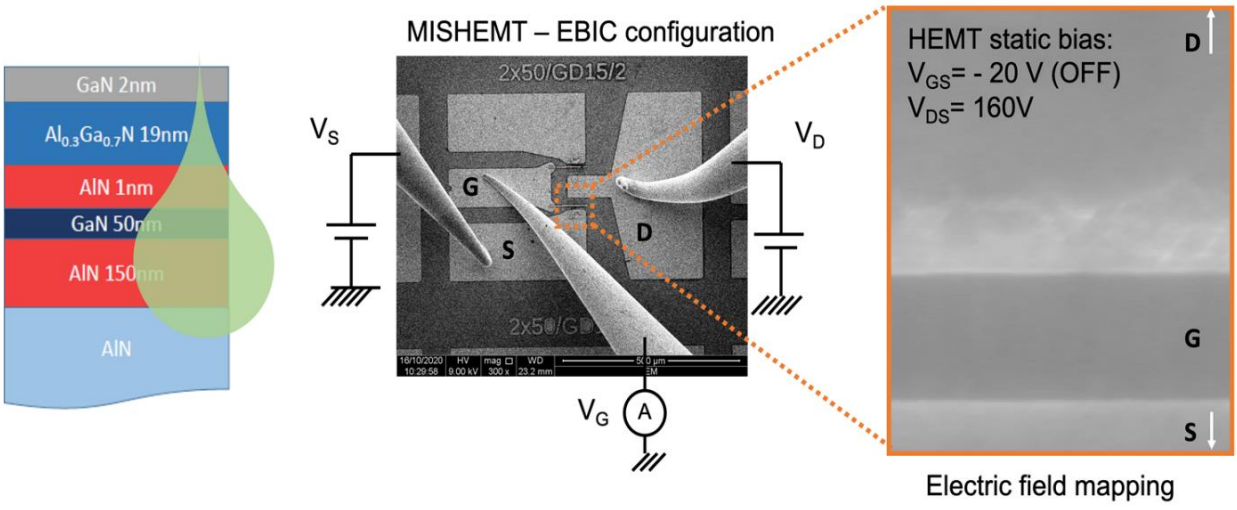



*Fig. 2. 16 [Left] Cross section of 50 nm GaN channel HEMT with superimposed schematic peer of electron beam irradiation (green), [Middle] configuration of the electron beam induced current measurement used on the MISHEMT and [Right] Mapping of the space charge region nearby gate electrode.*

irradiated on top of the MISHEMT. Here, the maximum penetration depths of the 15 keV electron beams estimated through the Monte Carlo simulation were 300 nm with a typical peer distribution as shown in Fig. 1.16 [left]. The beam current was measured to be 100 pA and the signal was modulated thanks to the modulation of the beam blanker at a frequency of 50 kHz. A lock in amplifier was used to measure the beam current. We performed a mapping of electron beam induced current close to the gate electrode where the depletion region induces an electric field in the case of reverse bias of the HEMT. Under the electron beam irradiation, electron–hole pairs were created and those created within the near electrode field region were separated, generating an EBIC current.

The plots above show the extension of the space charge region from the gate to the drain for a gate voltage of $V_{GS}$= -20 V and $V_{DS}$ starting from 0 to 45 V for 500 nm GaN channel (left) and from 0 to 380 V for 50 nm GaN channel (right). In both cases, we observe a linear extension of the space charge region with a slope of 7.2 nm/V in the case of 50 nm GaN device and 6.2 nm/V in case of 500 nm GaN device. The linear extension of the space charge region has been already observed in 2D system with a slope of $W/V = \varepsilon_S/qn_s$, where W is the space charge region, V the applied voltage bias, $\varepsilon_S$ the static dielectric constant, q the elementary charge and $n_s$ the sheet density of carrier [130], [131]. From the slope measured for the two samples, one can infer the carrier $n_s = 7.1\times10^{12}$ $cm^{-2}$ for 50 nm GaN device and $n_s = 8.2\times10^{12}$ $cm^{-2}$ for 500 nm GaN device, which is in good agreement with the Hall effect measurements. The EBIC signal is not homogeneous in the space charge region for 50 nm GaN device probably due to the presence of local defects that are locally disturbing the electric field distribution. However, the electrical breakdown was not observed in the case of 50 nm GaN device up to the voltage limit of the experiment (380 V). In order to investigate in more detail the breakdown mechanisms, cathodoluminescence measurements have been performed at 5K and room temperature (RT) to map the presence of defects. A 10 keV e-beam energy has been used and mapping has been performed at an emission wavelength of 360 nm at 5K and room temperature. The results are compared for different biases and with EBIC images in Fig 2.17. Some defects cancel the near-band edge emission creating a dark area in CL images. A strong electric field occurs in the same region as revealed by the bright area of the EBIC

image. More investigations will be needed in order to clarify the origin of the defect at the origin of the breakdown.

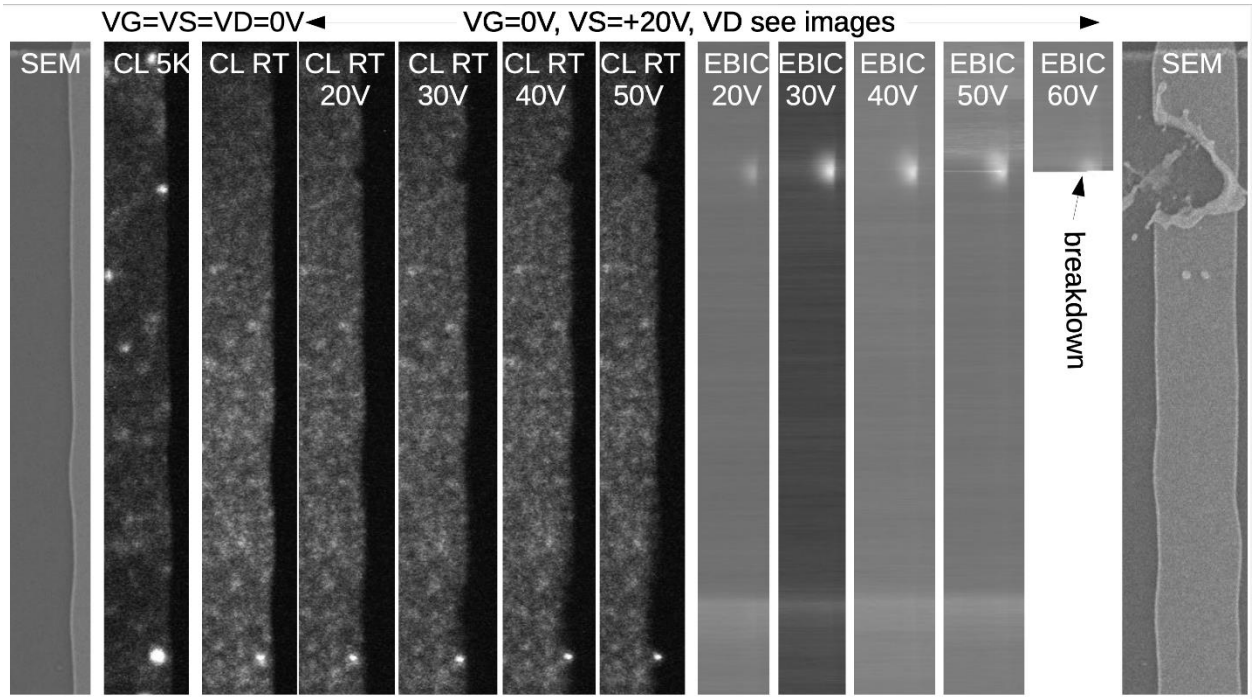



*Fig. 2. 17 Cathodoluminescence mapping at 360 nm at 5 K and RT under different bias. EBIC measurements using the same bias polarization and SEM images before [Left] and after breakdown [Right]*

## 2.5 Conclusion

This chapter shows an experimental demonstration of GaN channel MISHEMTs on bulk AlN grown by ammonia source MBE. The GaN channel thickness downscaling showed a gradual decrease in strain relaxation while going from 500 nm to 50 nm channel thickness whereas sub 20 nm GaN channel devices showed a fully strained channel and its consequence is reflected in their low 2DEG density. The critical GaN channel thickness related to the high defect density region is estimated to be around 20-30 nm thick from the GaN/AlN interface, that degrades the 2DEG mobility. To compensate the reduction in 2DEG density, 9nm fully strained thin GaN channel devices with thick Al-rich AlGaN barrier were fabricated enhancing the 2DEG density up to $1.6 \times 10^{13}$ $cm^{-2}$. However, the thin GaN channel HEMTs were not functional due to high surface leakage.

GaN channel HEMTs with ohmic contacts as low as 0.3 Ω.mm were obtained for which the contact resistances kept degrading with channel downscaling. The transfer characteristics showed fully functional GaN-on-AlN HEMTs with low off-state leakage down to 50 nm thick GaN channel device and high off-state leakage for sub 20 nm thick GaN channel devices. The devices showed current density as high as 1.1 A/mm for thick channel device. The buffer breakdown measurements revealed up to 7 MV/cm electric breakdown field with low leakage current highlighting the benefits of ultra-wide bandgap material beyond the capabilities of GaN and SiC wide bandgaps. The 50nm thin GaN channel device showed hard breakdown voltage around 1400 V that is almost 14× higher than the 500 nm GaN HEMT. The breakdown I-V characteristics confirm the absence of electron injection into the substrate for an identical gate-drain leakage current profile. Transistor breakdown measurements showed increase in breakdown voltage with reduction in channel thickness, where it can be assumed that the electric field peak spreads more into AlN with thinner channel devices. The 20 nm thin GaN channel HEMTs showed breakdown voltages up to 3000 V demonstrating the multi-kilovolt capability of thin GaN channel HEMTs fabricated on bulk AlN. However, considering the critical field strength, GaN is the lowest band gap material in the epi-structure which limits its high voltage withstanding capabilities, and could thus be further improved by incorporating aluminum in the channel. This brings us to the development of a new series of FETs, realized by growth of AlGaN/AlGaN heterostructures. The next chapter will present a study based on novel AlGaN channel demonstrating an approach towards development of high voltage FETs.

# *Chapter-03 AlGaN channel HFETS on Si and bulk AlN*

In the previous chapter, the benefit of using bulk AlN substrates has been demonstrated experimentally with up to 7.5 MV/cm lateral breakdown electric field. However, when compared to conventional silicon substrates, the cost of 50 mm AlN substrates is almost 100 × higher than 200 mm Si substrates. Additionally, the majority of semiconductor fabs support 200 mm or 300 mm wafer diameter with CMOS-compatible foundry process. In the short-term, the major drawback for moving to bulk AlN substrate might be the industrial integration with the currently available foundries and the availability of large-diameter substrates. This brings us back to silicon, cheap and vastly available.

This chapter will demonstrate the DC performance of novel AlGaN channel HFETs on silicon substrate with various Al compositions in the channel. To our knowledge, the devices presented in this work are the first-ever operation of AlGaN/AlGaN MISHFETs on silicon. The evolution of electron mobility with different Al compositions in the channel and the electron transport properties have been investigated by performing Hall Effect measurements under varying temperature conditions. High-temperature DC characterizations have been realized on various AlGaN channel devices to determine their thermal reliability. Furthermore, the impact of gate dielectric on the device's DC performance will be discussed. To push the devices in the kV regime, AlGaN channel HFET on bulk AlN has been developed to exploit its high-voltage operation. Later, a study based on the HV reliability of GaN and AlGaN channel HFETs on bulk AlN will be presented. Finally, the major challenges and merits of AlGaN channel HFETs will conclude this work.

## 3.1 AlGaN channel HFETs on Si

Submicron buffer-less AlGaN / AlGaN heterostructures were grown by MBE on Si (111) substrate with a 200 nm thin AlN nucleation layer, a 450 nm AlGaN channel, a 1 nm thin AlN spacer, a 10 nm AlGaN barrier, and a 1 nm GaN cap layer (see Fig. 3. 1 (Left)). In the given structures, $Al_xGa_{1-x}N$ channels are composed of 10%, 30%, and 60% Al as shown in sample_A, sample_B, and sample_C, respectively. The Al content in the barrier must be higher than the channel in order to generate a 2DEG at the interface. The conduction band profile of the given structures shows the reduction in 2DEG density with increasing Al content in the channel. The decrease in polarization-induced 2DEG charges by going towards the Al-rich channel can be linked to the reduction in the difference between Al content in the barrier and channel (ΔAl %).

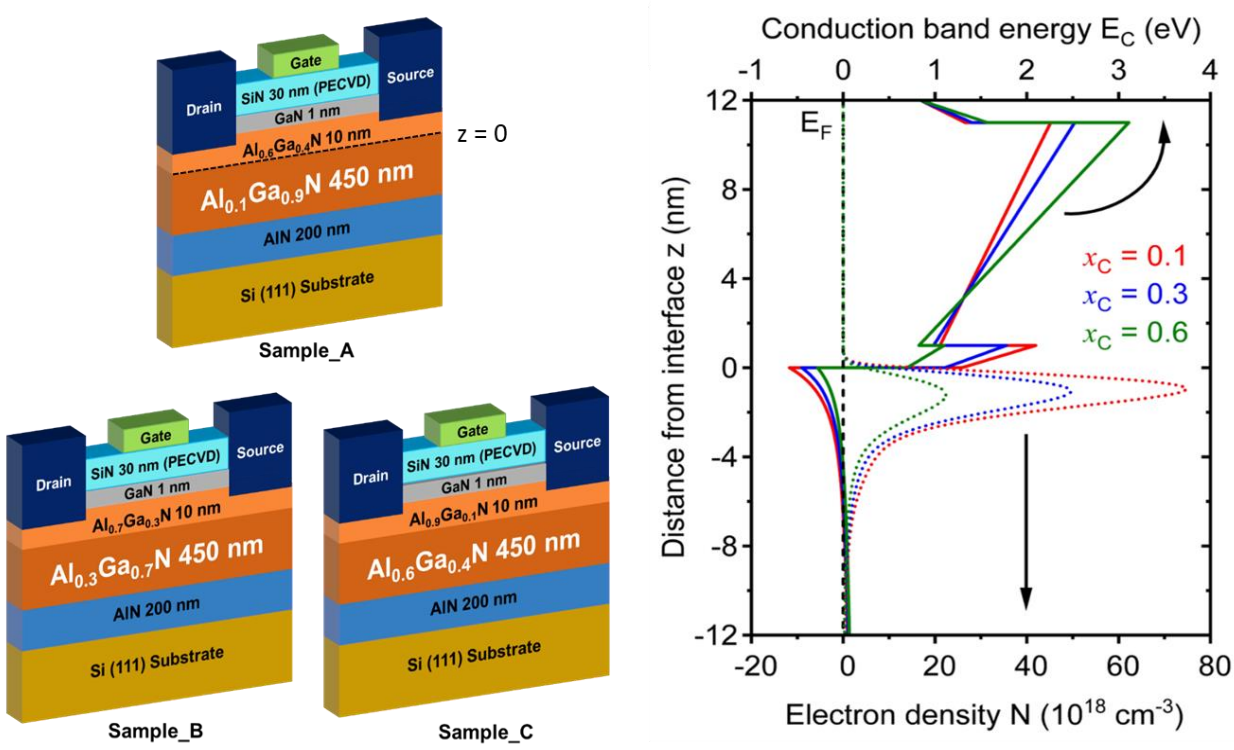



*Fig. 3. 1 Cross-sectional schematic structure (Left) and conduction band profile with simulated channel electron density (Right) for the AlGaN channel HEMTs with various Al compositions*

### 3.1.1 Device Fabrication and structural characterization

Drain and source contacts were fabricated by partially etching the AlGaN barrier using ICP-RIE followed by e-beam evaporation of Ti/Al/Ni/Au metal stack with a 30s wet etch in BOE solution prior to the metallization. Subsequently, the optimum RTA for these devices has been set to 850°C for sample_A and 875°C for sample_B and sample_C. The $L_{GD}$ and $L_{GS}$ are 5 to 40 µm and 2.7 µm, respectively. A 220 nm thick mesa isolation was achieved using $Cl_2$/Ar plasma by ICP etching technique. A 30 nm thick PECVD SiN aided in the passivation of the device surface while being used as a gate dielectric. Finally, a 220 nm

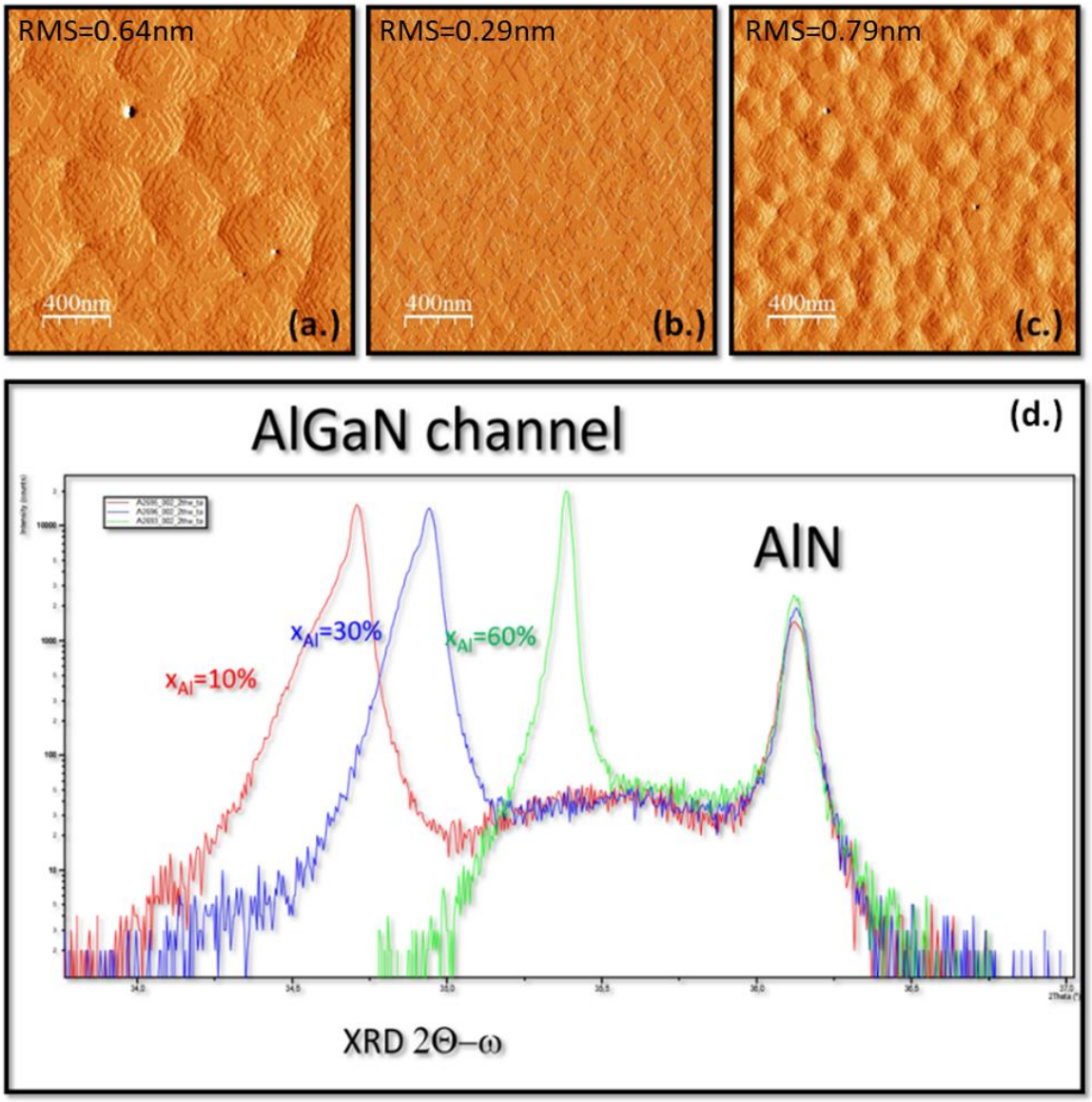



*Fig. 3. 2 AFM scans for heterostructures with (a.) 10%, (b.) 30% and (c.) 60% AlGaN channel. (d.) XRD 2θ-ω scans for AlGaN channel HFETs*

Ni/Au metal stack was evaporated on top of SiN to fabricate gate electrodes with 3μm gate lengths, yielding metal insulator semiconductor (MIS) - HFETs. Fig. 3.2 shows the surface morphology of various AlGaN channel HEMTs by atomic force microscopy (AFM) images over a scan area of 2 × 2 μm. These scans derive a root-mean-square roughness of 0.64 nm, 0.29 nm, and 0.79 nm for 10% (a.), 30% (b.), and 60% (c.) Al composition in the AlGaN channel respectively. The roughness increases as expected with the Al-content into the channel but remains below 1 nm in both cases reflecting a decent crystal quality. Fig. 3.2(d.) shows (002) X-Ray Diffraction (XRD) profile cover angles of 33°-37° along the omega axis. We can see the shift in diffraction angle while moving from 30% to 60% AlGaN channel suggesting increment of compressive strain in the channel. However, interestingly the FWHM shows improvement in crystal quality while increasing the Al-content, which may be supported by the gradual reduction in lattice mismatch with the AlN nucleation.

### 3.1.2 DC characterization

Hall Effect measurements were realized using Van der Pauw pattern and Hall bar pattern. Electrical measurements at room temperature were carried out using a Keysight B1505A Power Device Analyzer / Curve Tracer. The buffer breakdown measurements were performed with the samples immersed in Fluorinert FC-40. The transfer characteristics of the fabricated devices indicate that the MIS-HEMTs are fully operational, displaying a high on-off ratio in both samples with on-state current levels that align with the sheet resistances (refer to Table I). The transfer characteristics were evaluated at a drain-source voltage ($V_{DS}$) of 4V for devices with $L_{GD}$ of 5 μm, as depicted in Fig. 3. 3(a). The TLM measurements yielded a specific contact resistance ($R_C$) of 0.64 Ω.mm and 4.3 Ω.mm, with the maximum drain current reaching 800mA/mm and 90 mA/mm for sample_A and B respectively as illustrated in Fig. 3.3 with $V_{GS}$ swept from -10 V to +4 V. The extracted specific contact resistance for Sample_A, B, and C is 2.9 mΩ.cm$^2$, 9.8 mΩ.cm$^2$ and 120 mΩ.cm$^2$ respectively. In the case of sample_B, the drain-source contacts displayed non-ohmic behavior, leading to a limited $I_{Dmax}$ of 17 mA/mm, as depicted in Fig. 3(d). This outcome aligns with previously reported results from other research groups [91], [132]–[134]. It is worth noting that selective regrowth has demonstrated the potential to address this issue to a significant extent [97]. Additionally,

local implantation could be considered when employing high Al-content AlGaN channels [135], [136].

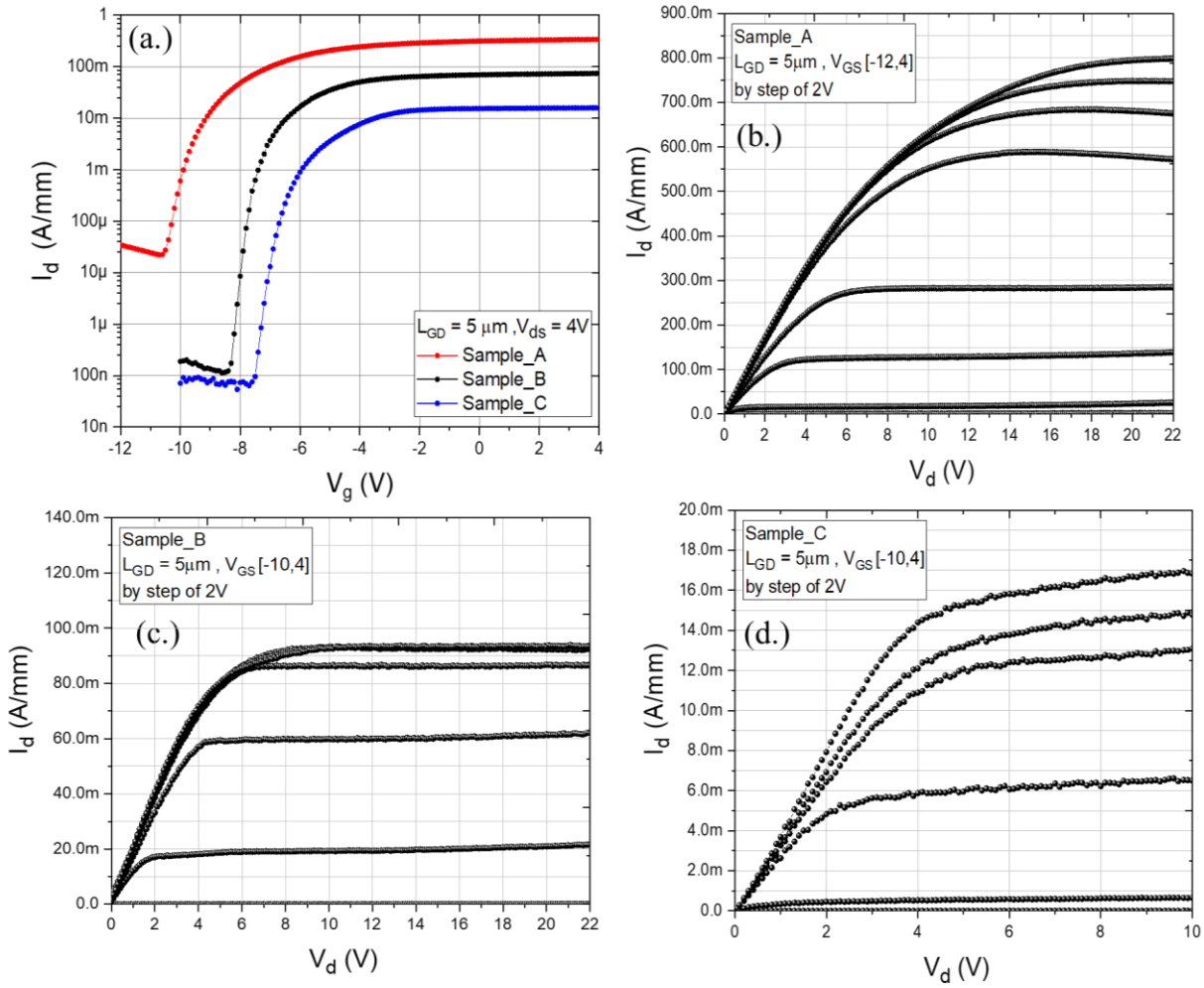



*Fig. 3. 3 (a.) Transfer characteristics and Output characteristics of (b.)10%, (c.)30%, and (d.)60% AlGaN channel HFETs*

| Samples | Sheet Resistance [kΩ/□] | Electron Mobility [cm²/V. s] | 2DEG Concentration [1/cm²] |
|---|---|---|---|
| **Sample_A** | 1.2 | 450 | $1.1\times10^{13}$ |
| **Sample_B** | 1.8 | 323 | $1.1\times10^{13}$ |
| **Sample_C** | 7.3 | 137 | $6.3\times10^{12}$ |

*Table 3. 1 Hall Effect measurements of AlGaN channel HEMTs*

### 3.1.3 Buffer Breakdown Characteristics

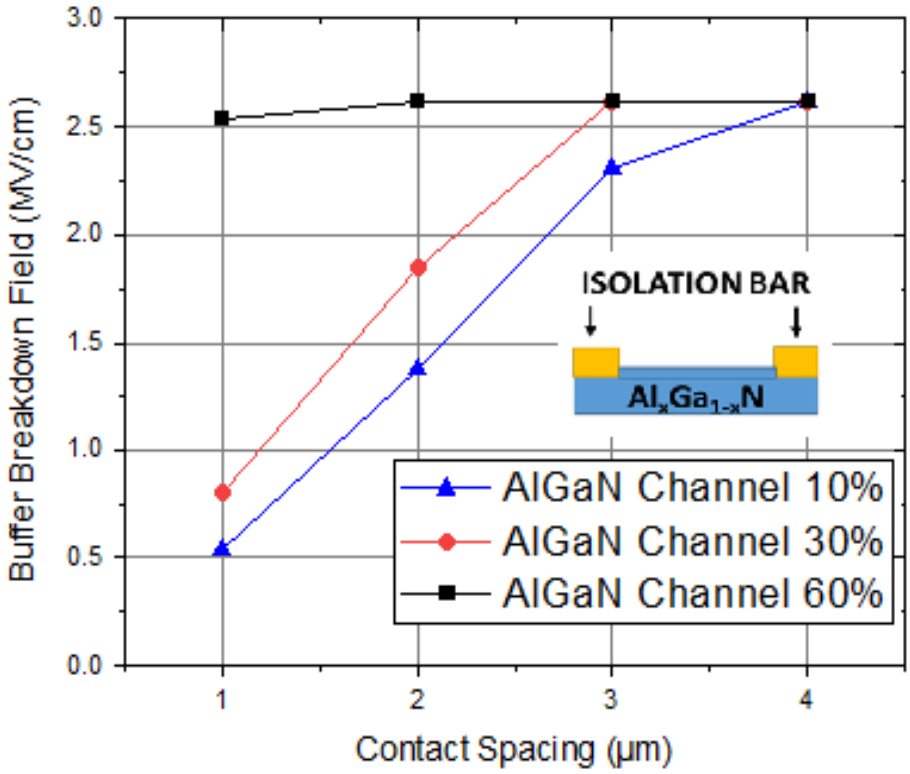



*Fig. 3. 4 Buffer breakdown field as a function of contact spacing*

Fig. 3.4 illustrates the buffer breakdown field evolution with varying two-terminal contact spacing in fabricated AlGaN channel HEMTs. We conducted electrical measurements using 100×100 μm contact patterns on an isolated bar. It is noteworthy that we observed a significant increase in the buffer breakdown field, going from 0.54 MV/cm to 2.54 MV/cm when altering the Al content from 10% to 60% in the $Al_XGa_{1-X}N$ channel, for a 1 μm contact spacing. In all scenarios, the buffer breakdown voltage saturation is primarily influenced by the injection of electrons through the silicon substrate. However, this saturation effect becomes apparent in 10% and 30% AlGaN channel transistors when the contact spacing is 4μm and 3μm, respectively. Consequently, Al-rich AlGaN channel demonstrates a notable electrical breakdown field that holds great promise for downsizing lateral power switches.

### 3.1.4 Transistor Breakdown Characteristics

The advantage of higher Al content in the channel in terms of blocking voltage is also evident at the transistor level. In fact, in Fig. 3.5 (a), we can see the off-state 3-terminal

breakdown voltage at $V_{GS}$ = -12 V for 10% AlGaN channel and $V_{GS}$ = -10 V for 30% and 60% AlGaN channel transistors with a gate-drain spacing of 5 µm. The Al-rich AlGaN channel HEMTs demonstrate superior voltage handling compared to those with a 10% AlGaN channel, especially when considering the submicron-thickness of heterostructures. A significant reduction in leakage current is observed along with an increase in the blocking voltage as the Al content is increased in the channel. This trend is consistent across various gate-drain spacing, as illustrated in Fig. 3.5 (b), and can be attributed to the wider bandgap of Al-rich AlGaN channel. It is worth emphasizing that the rather restricted breakdown voltage, measuring less than 200 V, is primarily due to the overall structure's thickness which is well below 1 µm. This condition leads to electron injection issues at the AlN/Si interface. To address this limitation, the incorporation of Al-rich AlGaN buffer layers can be employed to enhance the distribution of the electric field within the structure, ultimately achieving blocking voltages in the range of multiple kilovolts [86], [125], [126].

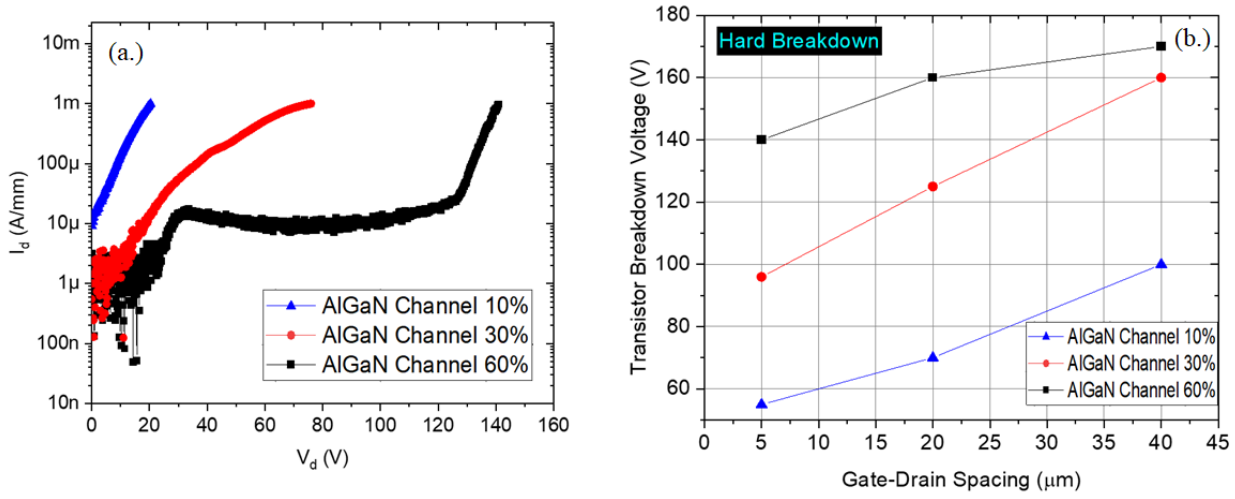



*Fig. 3. 5 (a.) Off-state 3-terminal breakdown voltage for transistors at $V_{GS}$ = – 12 V for 10% AlGaN channel HFETs and $V_{GS}$ = – 10 V for 30% and 60% AlGaN channel HFETs with a gate-drain spacing of 5 µm, (b.) for various gate-drain spacing.*

### 3.1.5 High-Temperature DC Characterization

The samples were mounted on a thermal stage inside a cryostat for variable temperature measurements. Their DC (T) measurements were performed with a Keithley 2612B Source Measure Unit in a dark environment, with a temperature range from 300 K to 600 K. The temperature-dependent characteristics of AlGaN channels containing 10%, 30%,

and 60% Al are presented in Fig. 3.5 (a), (b), and (c), respectively. These figures reveal the excellent operational performance of the transistors, demonstrating their stability at temperatures as high as 600 K. Analyzing the transfer characteristics ($J_{DS}$-$V_{GS}$) at $V_{DS}$ = 4 V, we extracted several key parameters, including the on-state current density ($J_{on}$) at $V_{GS}$ = + 2V, the off-state current density ($J_{OFF}$) at the threshold voltage (Vth), the maximum transconductance ($Gm_{max}$) derived from the transfer characteristic, and the subthreshold slope (S) measured at the threshold voltage. These temperature-dependent parameters are illustrated in Fig. 3.5 (d), (e), and (f), respectively. Notably, the off-state current density increases by one-fold for 10% Al content and twofold for 30% and 60% Al content channels. However, it is essential to highlight that the off-state current density remains lower for 30% and 60% AlGaN channel HEMTs compared to the 10% AlGaN channel HEMT across the entire temperature range. HFETs with 10% and 30% Al content exhibit a 30% reduction in on-state current density over the studied temperature range, a significant improvement compared to conventional GaN channel HEMTs. In contrast, HFETs with 60% Al content experience an increase in on-state current density as the temperature rises. This behavior might be attributed to the notable increase in carrier density that will be explained later. The evolution of maximum transconductance mirrors that of the on-state current density, declining for 10% and 30% Al content and increasing for 60% Al content. The subthreshold slope appears to be similar for 10% and 30% Al content but is higher for 60% Al content, indicating a more favorable $I_{ON}/I_{OFF}$ switching ratio for Al-rich AlGaN channel HEMTs. Despite the device with 60% Al content having higher contact resistance compared to those with 10% and 30% Al content, its temperature-dependent performance underscores its significant potential for high-temperature power switching applications. Hence, to study the impact of temperature variation on the 2DEG properties of the fabricated devices, we performed temperature-dependent Hall Effect measurements.

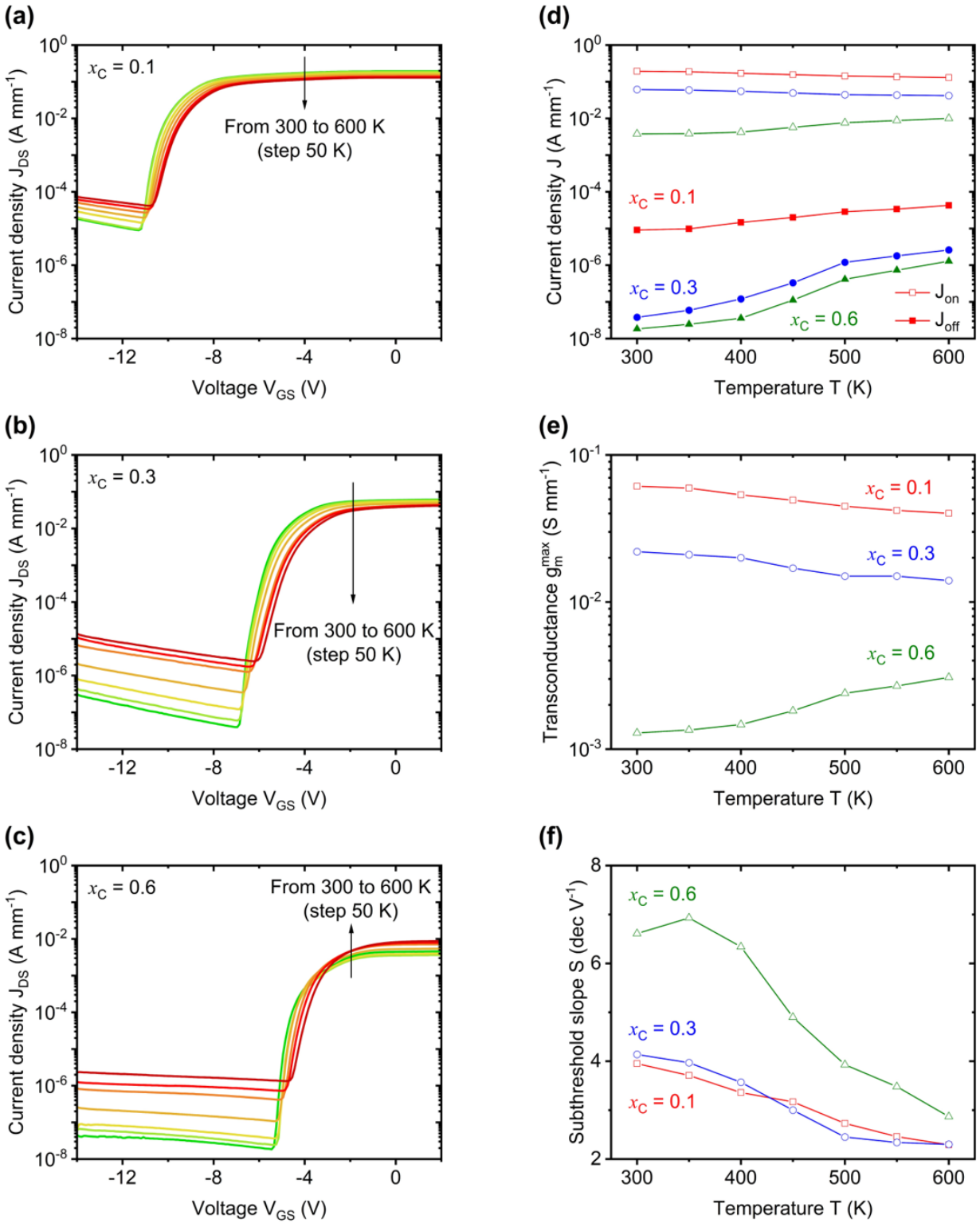



*Fig. 3. 6 Transfer characteristic $J_{DS}$ ($V_{GS}$) as a function of temperature for AlGaN channels with (a) 10%, (b) 30% and (c) 60% of Al. Temperature dependence of (d) the on/off current densities, (e) the maximum transconductance and (f) the subthreshold slope.*

### 3.1.6 Electron Transport in AlGaN channel HFETs on Si

Hall Effect measurements were conducted using a Hall bridge setup of four arms, as illustrated in Fig. 3.7. The Hall bridge has dimensions of 700 µm in length, and 70 µm in width (W), and the arms are 283 µm apart (D). A Keithley 6220 was used to apply the current between contacts 1 and 2, whereas a Keithley 2010 was used to measure voltage between contacts 3 and 5 (or 4 and 6) for determining resistivity between contacts 3 and 4 (or 5 and 6) for Hall voltage measurements. These measurements were carried out over a temperature range from 10 to 600 K.

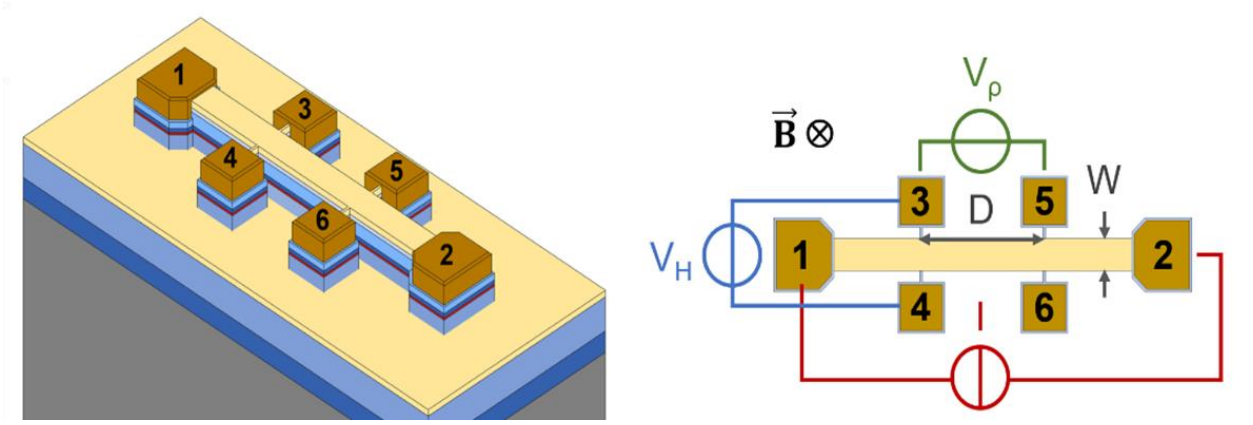



*Fig. 3. 7 3D schematic view of the Hall bridge (Left) and Electrical characterization setup of Hall measurements in Hall bridge configuration (Right)*

The measured sheet resistance and 2DEG density over the temperature range 10 K-600 K is illustrated in Fig. 3.8. From 10 to 125 K, the sheet resistance is slowly decreasing. In contrast, the Hall density is roughly constant for heterostructures with 10% and 30% of Al in the channel. From 125 to 400 K and for these two Al molar fractions, the sheet resistance increases, which is expected from a 2DEG conduction mode. From 400 to 600 K, a drop of sheet resistance is observed as well as a rapid increase of the Hall density. For the structure with 60% of Al in the channel, an increase of the Hall density is observed on the whole temperature range. Table 3.2 summarizes the value of Hall density ($n_H$) and Hall mobility ($\mu_H$) obtained at 10, 300, and 600 K. The 60% AlGaN channel heterostructure exhibits a higher increase in 2DEG density compared to the 10% and 30% ones, attributed to the shallower quantum well depth (as depicted in Fig. 3.1(right)), facilitating sub-band filling as the temperature rises [137]. One plausible explanation for this significant Hall density increase is the consideration of parallel conduction, where the Hall density comprises

contributions from carriers in both the 2DEG and the bulk channel. The conductivity is influenced by two primary factors: the 2DEG (two-dimensional electron gas) and bulk carriers. At low temperatures, it can be expected that bulk carriers remain immobilized, leading to the Hall density being equivalent to the 2DEG density, which remains constant regardless of temperature. Consequently, any alterations in the Hall density are to be attributed to the thermal activation of bulk carriers. These assumptions hold true only when the 2DEG and bulk carrier densities are within a similar order of magnitude. Hence, the increase in Hall density resulting from the activation of bulk donors could account for the decrease in resistivity.

| Channel Al fraction $x_C$ | $n_H$ ($\times 10^{13}$) ($cm^{-2}$) | | | $\mu_H$ ($cm^{-2}$ $V^{-1}$ $s^{-1}$) | | |
|---|---|---|---|---|---|---|
| | T = 10 K | T = 300 K | T = 600 K | T = 10 K | T = 300 K | T = 600 K |
| 10% | 1.60 | 1.88 | 3.78 | 582 | 390 | 196 |
| 30% | 1.35 | 1.41 | 2.82 | 287 | 228 | 116 |
| 60% | 0.41 | 0.57 | 0.71 | 123 | 99 | 82 |

*Table 3. 2 2-DEG concentration and electron mobility values extracted at 10,300 and 600K by Hall Effect measurements*

The electron mobility, displayed in Fig. 3.8(c), exhibits a distinct temperature-dependent pattern. It can be divided into two segments: a stable mobility from 10 to 225 K and a declining mobility from 225 to 600 K. The transition at 225 K is closely linked to the change in sheet resistance at the same temperature. The reduction in sheet resistance at temperatures above 400 K appears to balance out the rise in Hall density, thereby preserving the overall mobility profile that may eventually improve the current collapse usually seen with conventional GaN HEMTs. Hence, it can be deduced that Al-rich AlGaN channel HFETs demonstrate superior high-temperature performance which can be useful for extreme-temperature power switching applications surpassing the 300°C operational limitation of GaN HEMTs. However, along with high-temperature stability, high breakdown voltage is essential for power FETs to target converters with low bulk density and higher power ratings. To push the operation of AlGaN in the kV regime we decided to move towards the development of AlGaN channel HFET on bulk AlN.

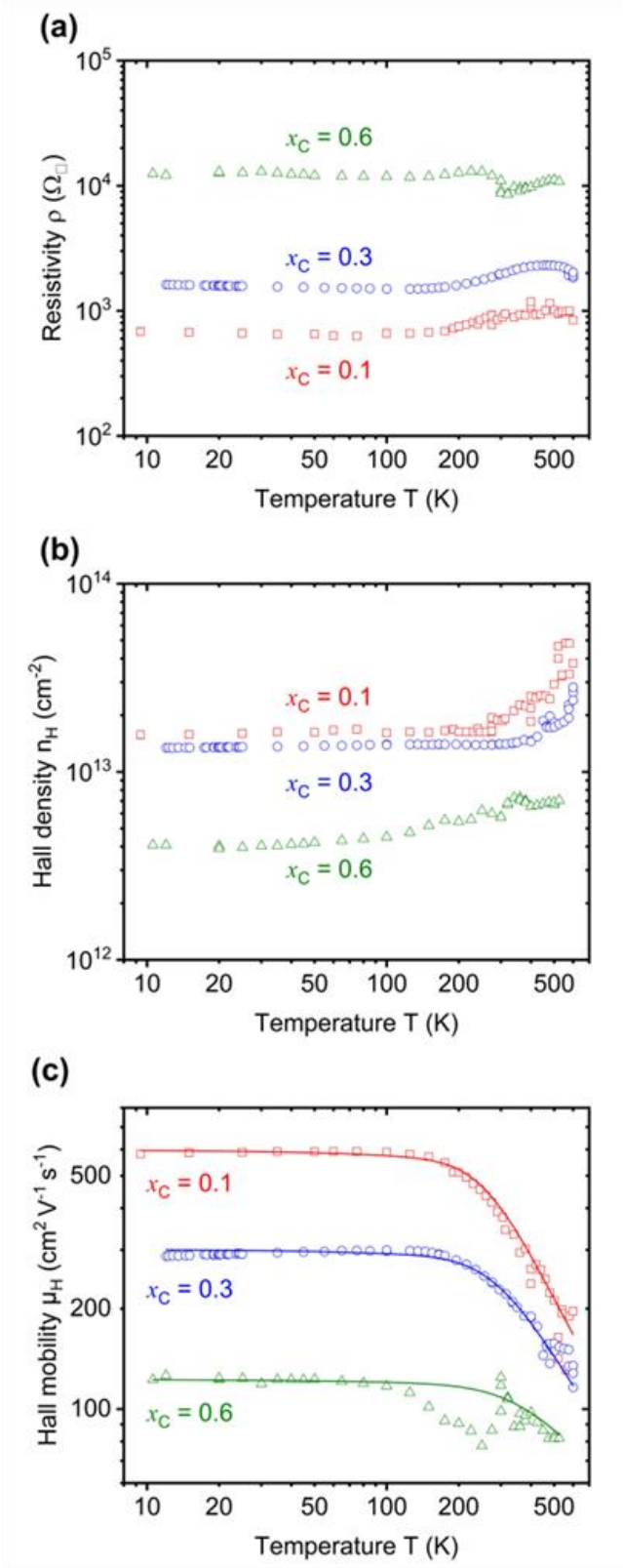



*Fig. 3. 8 Temperature Hall Effect results for various AlGaN channel HFETs. Evolution of (a.) Sheet Resistance (b.) 2DEG concentration and (c.) Electron mobility (symbol) with calculated low field mobility (line)*

## 3.2 AlGaN channel HFETs on bulk AlN

In the previous chapter, we examined the thin GaN channel HEMTs on bulk AlN for their HV operation. High voltage reliability and robustness of FETs are critical prerequisites for pushing the devices towards real applications. Extensive work has been performed over the years on GaN HEMTs for RF and power devices, to understand the trapping, de-trapping, and material degradation mechanisms using a time-dependent step stress measurement technique. To illustrate, several companies have successfully launched 650V GaN HEMTs making huge industrial penetration in the world of Si-FETs. However, the device's operational voltage capabilities are overdesigned because of the absence of avalanche breakdown in GaN lateral devices. Therefore, pushing the safe operating area closer to the actual breakdown voltage is needed. Hence, to enable reduced device dimensions for a given voltage range, the safe operating area should be closer to the hard breakdown voltage depending on the material reliability and targeted application. In this part of the work, we experimentally demonstrate the reliability and robustness of the fabricated GaN and AlGaN channel devices close to their hard breakdown voltages, eventually evaluating safe operating voltages.

### 3.2.1 Device fabrication and structural characterization

The GaN and AlGaN channel heterostructures were fabricated using $NH_3$-MBE within a Riber Compact 21 reactor, employed on c-plane Al-polar 2-inch diameter commercial bulk AlN substrates from HexaTech, Inc. (AlN-10 series) [138]. Initially, 90 nm and 250 nm thick AlN buffer layers were regrown in the temperature range of 850-900°C for the AlGaN channel heterostructure and the GaN channel heterostructure, respectively [17, 18]. Subsequently, the growth temperature was lowered to 790-800°C for both heterostructures to facilitate the growth of the remaining epilayers, as depicted in Fig. 3.9. The surface smoothness of both heterostructures was confirmed using AFM, with an RMS roughness measuring less than 1 nm for scans conducted on 2 x 2 $\mu m^2$ and 10 x 10 $\mu m^2$ areas. High-resolution XRD analysis, as displayed in Fig. 3.9 (bottom), indicates that the strain relaxation rate of the GaN channel layer is limited to 71%, and the FWHM of the (302) omega scan peak associated with this layer is 0.7°. These findings suggest that the GaN channel thickness is insufficient to effectively filter out the majority of threading dislocations that originate at the

interface with the AlN buffer layer, as observed in analogous structures with GaN channel thickness ranging from 8 nm to 500 nm [139]. In contrast, HRXRD analysis of the $Al_{0.23}Ga_{0.77}N$ channel reveals that the layer is almost entirely strain-relaxed (86% relaxation rate), with the FWHM of the (302) omega scan peak for this layer measuring 0.64°. Consequently, the $Al_{0.23}Ga_{0.77}N$ channel exhibits slightly better crystal quality than the GaN channel heterostructure, with fewer threading dislocations owing to the smaller lattice mismatch strain with AlN, combined with a greater thickness. Additionally, since the majority of dislocations are nucleated and bent near the channel/AlN interface a primary distinction between the two structures is that the thicker channel allows for an increased separation between the 2DEG induced at the top of the channel and the flawed bottom interface [139].

The device fabrication process commenced with a partial etching of the AlGaN barrier in both cases, using $BCl_3/SF_6$ chemistry with ICP-RIE etching, followed by a surface wet treatment using BOE 7:1 solution. Subsequently, electron beam evaporation was used to deposit Ti/Al/Ni/Au contacts, performed within a Plassys MEB550SL, followed by RTA at 825°C and 850°C for GaN and AlGaN channel HFETs, respectively. Mesa isolation of the devices was achieved by ICP etching all the way down to the AlN substrate. Prior to the electron beam evaporation of Ni/Au gate contacts, a 30 nm SiN dielectric layer was deposited via PECVD to passivate the device surface. The $L_{GD}$ was varied from 5-40 μm, while the gate length $L_G$ measured 3 μm, and the $L_{GS}$ was 2 μm. Finally, the fabrication process concluded with the evaporation of Ti/Au pads, finalizing the construction of the metal-insulator-semiconductor (MIS)-HFETs.

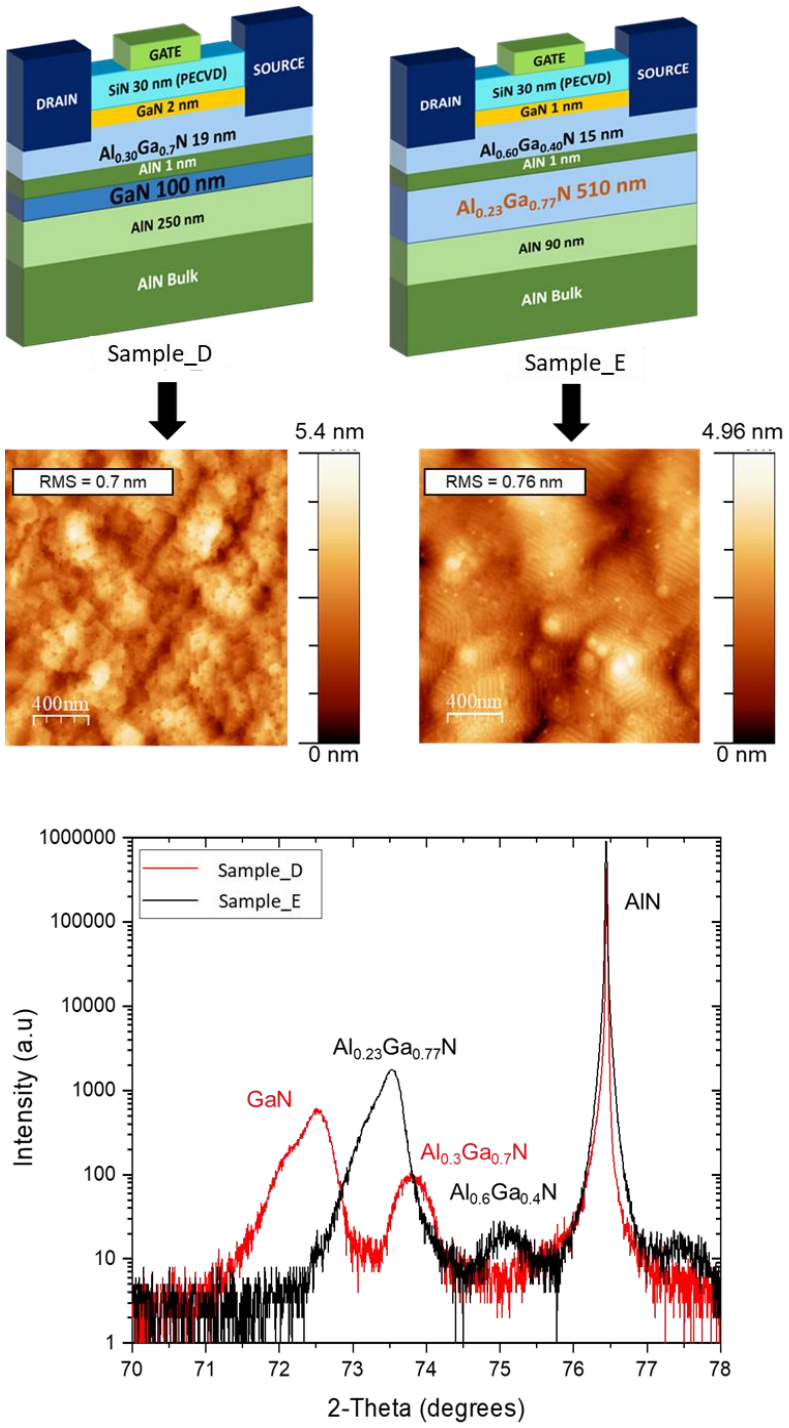



*Fig. 3. 9 Cross-sectional schematics of GaN channel (Sample_D) and AlGaN channel (Sample_E) heterostructures on bulk AlN along with their AFM scans and XRD scans*

### 3.2.2 DC Characterization

Hall measurements were carried out on wafers using the Van der Pauw pattern. In the case of GaN channel device, the 2-DEG mobility is observed to decrease as the channel size is reduced. This is attributed to increased scattering effects and the potential impact of the regrowth interface, which is in closer proximity to the 2-DEG than in AlGaN channel HEMTs [140]. GaN channel HEMTs exhibit a 2-DEG mobility of approximately 840 $cm^2/(V{\cdot}s)$ for a 100 nm thick channel, which is notably lower than the typical value of over 1500 $cm^2/(V{\cdot}s)$ for thicker GaN channels [139]. On the other hand, AlGaN channel HEMTs demonstrate a respectable electron mobility of approximately 340 $cm^2/(V{\cdot}s)$ with a 2-DEG electron density in the range of $10^{13}$ $cm^{-2}$, as indicated in Table 3.3.

| Sample | Sheet Resistance [ohm/sq.] | Mobility [$cm^2/V.s$] | Concentration [$cm^{-2}$] |
|---|---|---|---|
| GaN channel | 895 | 840 | $8 \times 10^{12}$ |
| $Al_{0.23}Ga_{0.77}N$ channel | 1550 | 342 | $1.18 \times 10^{13}$ |

*Table 3. 3 Hall Effect measurements extracted 2DEG properties for GaN and AlGaN channel MISHFETs*

High-voltage electrical measurements were performed using a Keysight B1505A Power Device Analyzer/Curve Tracer in conjunction with a Keysight N1268A UHV Expander Unit, with the samples submerged in fluorinert FC-40. The transfer characteristics of the samples at a $V_{DS}$ = 10V, along with their respective gate-leakage current characteristics, are depicted in Fig. 3.10 (left). These measurements reveal that the devices under examination exhibit minimal trapping below the gate, as evidenced by the low hysteresis between forward and reverse sweep of transfer characteristics as indicated by the arrows. The output characteristics of GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs, as shown in Fig. 3.10 (right), indicate an $I_{DSmax}$ of approximately 180 mA/mm and 320 mA/mm, respectively. The specific $R_{on}$, calculated at $V_{GS}$=0V in the linear regime, is roughly 4 $m\Omega{\cdot}cm^2$ for transistors with $L_{GD}$=5 µm in both cases. However, improvements in ohmic contact resistances are still needed which is confirmed by the Schottky turn-on observed at low bias in the output characteristics. In recent years, various research groups have been working on developing different techniques, such as n+ GaN regrowth, graded contacts, doped barrier contacts, and various

metal stack schemes, to achieve ohmic contact resistances as low as $1.9 \times 10^{-6}$ Ω·cm$^2$ [96], [125], [133].

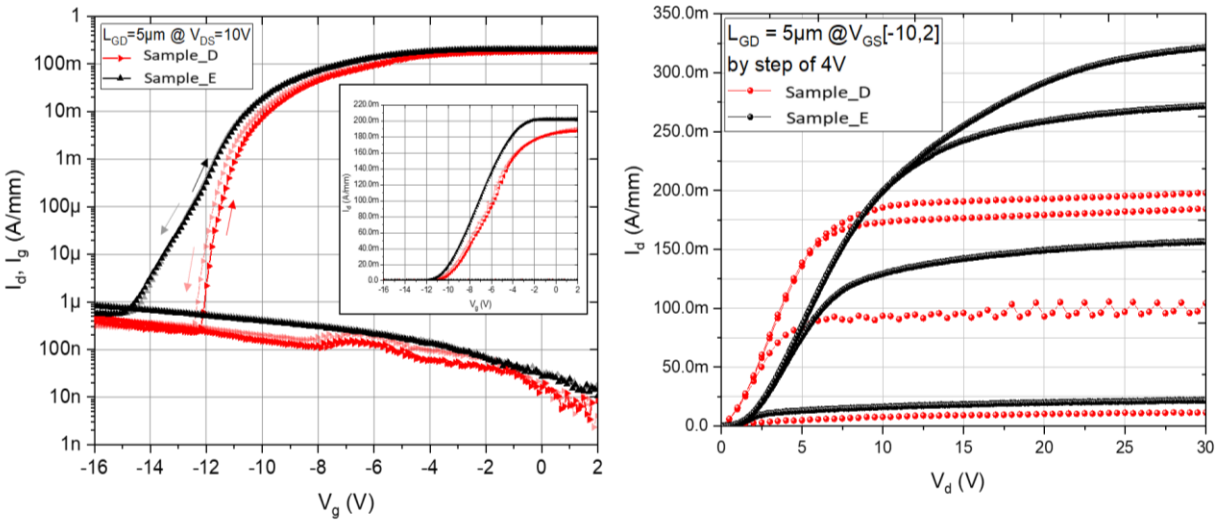



*Fig. 3. 10 Transfer characteristics (left) and Output characteristics (right) of fabricated GaN and AlGaN channel MISHFETs on AlN*

### 3.2.3 AlN breakdown characteristics

Fig. 3.11 (a) illustrates the electrical breakdown characteristics of AlN substrate with a 1 μm contact spacing and a contact area of 100 μm × 100 μm. It is noteworthy that the average electrical breakdown voltage exceeds 1000V while maintaining a leakage current density below 10 μA/mm. The inset in Fig. 3.11 (a) highlights a remarkable buffer breakdown field of up to 10 MV/cm, even with close contact spacing, demonstrating the potential of UWBG materials. In Fig. 3.11 (b), we observe the two-terminal breakdown behavior of AlN with varying contact spacing. Breakdown voltages reach as high as 7kV with a 63μm contact spacing. The inset diagram further illustrates that the mesa heights for GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs are 380 nm and 620 nm, respectively, well within the AlN substrate.

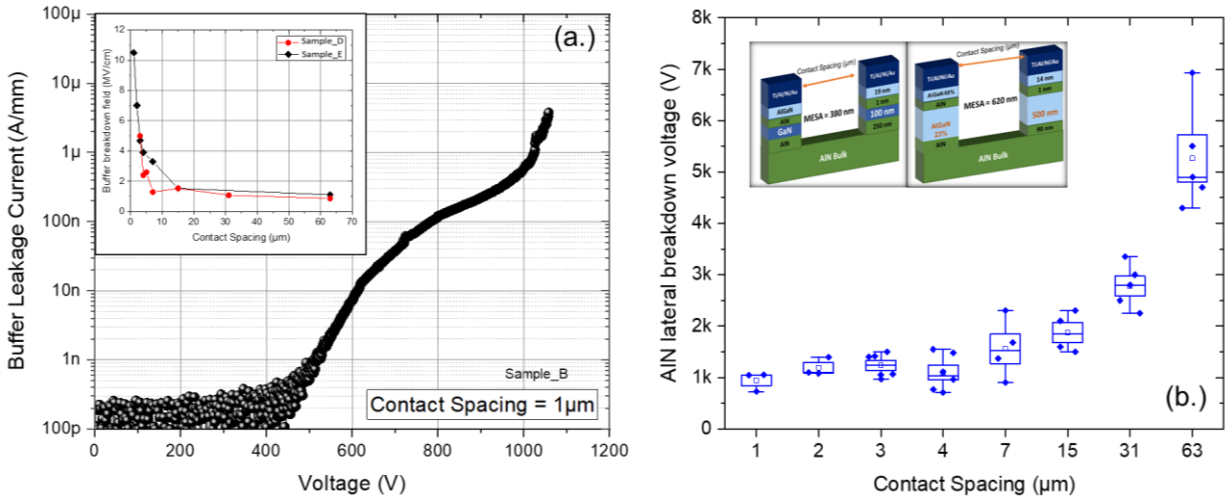



*Fig. 3. 11 Buffer leakage current characteristics for 1µm contact spacing (Left) and Mean values of AlN lateral breakdown voltage for various contact spacing of GaN and AlGaN channel MISHFETs.*

### 3.2.4 Transistor breakdown characteristics

The 3-Terminal breakdown characteristics, as depicted in Fig. 3.12 (a), indicate that the onset of hard breakdown is triggered by the gate-leakage current in both samples. Remarkably, $Al_{0.23}Ga_{0.77}N$ channel HFETs exhibit a significantly higher breakdown voltage, reaching as high as 2500V, which is four times greater than that of thin GaN channel HFETs, particularly for larger $L_{GD}$. In Fig. 3. 12 (b), the graph illustrates the variation in transistor blocking voltage at different gate-drain spacings for a gate leakage current density of 100 µA/mm. As anticipated, this data highlights that $Al_{0.23}Ga_{0.77}N$ channel HFETs possess five

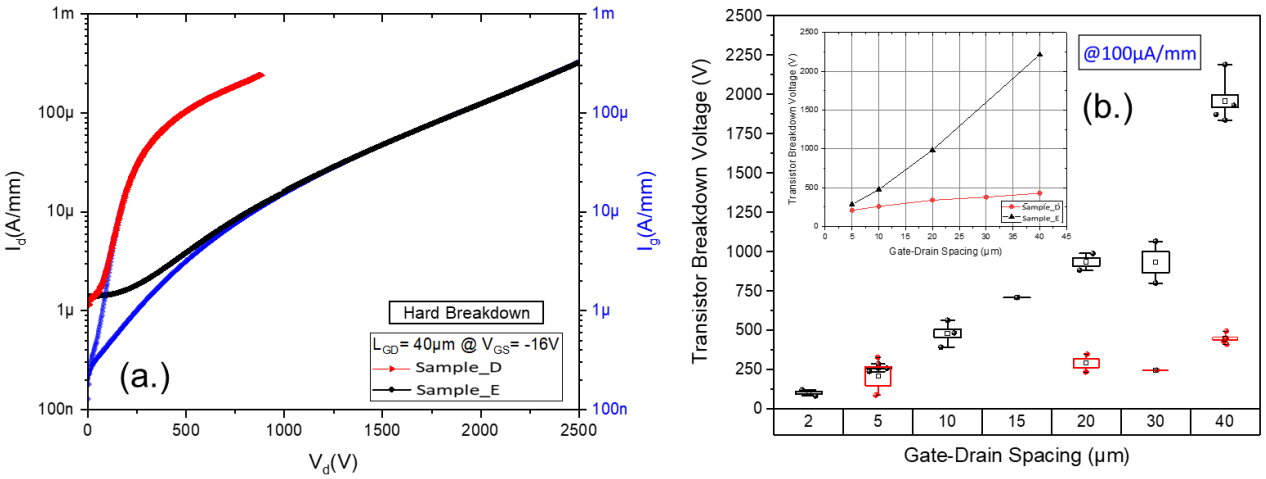



*Fig. 3. 12 (a.) Hard electrical breakdown characteristics for transistors with a gate-drain spacing of 40 µm at VGS = -16V and (b.) Mean value of transistor blocking voltage for various LGD of GaN and AlGaN channel MISHFETs*

times the blocking voltage per micron compared to GaN channel HFETs. This demonstrates the high-voltage blocking capabilities of AlGaN channel HFETs. It is worth noting that no post-passivation was done apart from the 30nm SiN below the gate.

Ensuring the high voltage reliability and robustness of FETs is a fundamental necessity for advancing these devices into practical real-world applications. Over the years, substantial research efforts have been dedicated to GaN HEMTs in the domains of RF and power devices, to comprehend trapping, de-trapping, and material degradation mechanisms, achieved through the application of time-dependent step stress measurement techniques [80], [115], [141]–[145].

### 3.2.5 High voltage robustness test

We conducted an off-state stress experiment involving a gradual increase of $V_{DS}$ on transistors with $L_{GD}$= 40 µm, bringing them close to the hard breakdown voltage for both GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs. As illustrated in Fig. 3.13 (a), the devices were

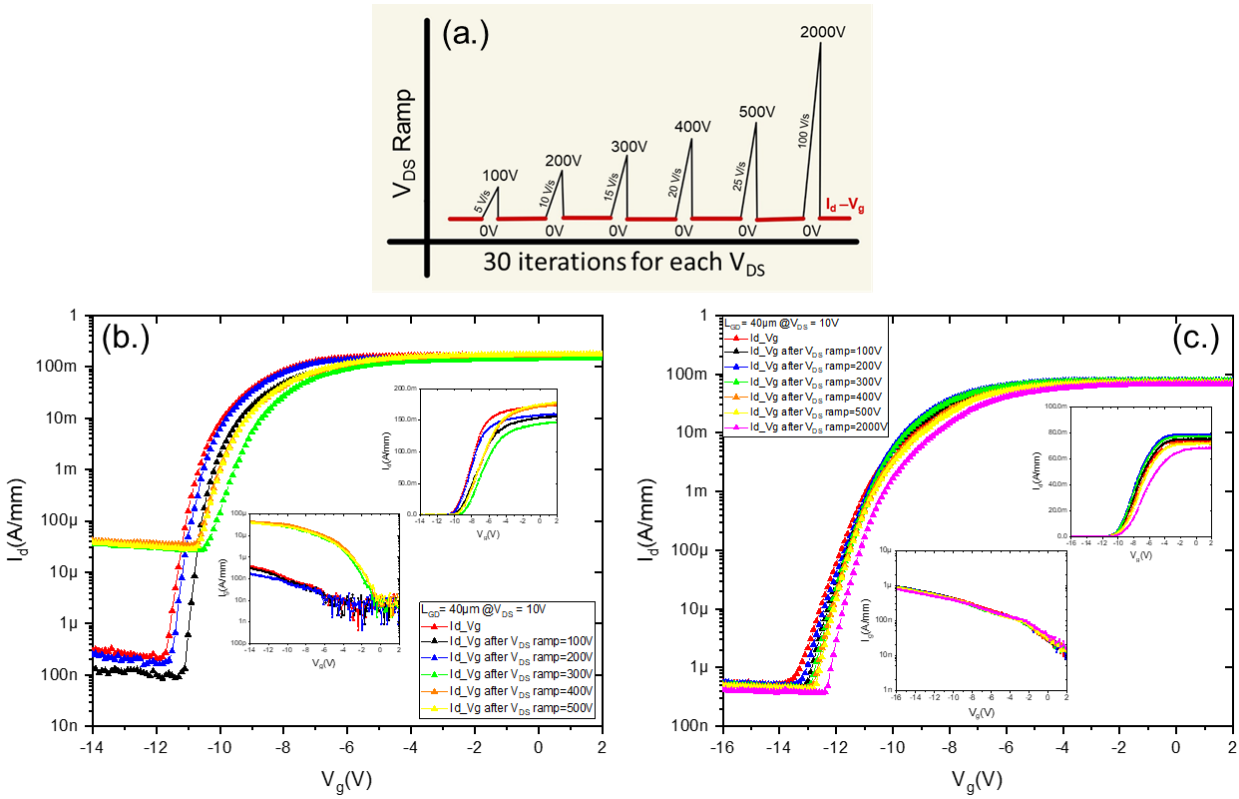



*Fig. 3. 13 (a.) Robustness test schematic for various $V_{DS}$ stress voltages, Transfer characteristics measured after each $V_{DS}$ ramp for (b.) GaN channel MISHFETs and (c.) AlGaN channel MISHFETs with their insets showing gate leakage current density and linear transfer characteristics.*

subjected to incremental voltage steps, with each $V_{DS}$ ramp repeated 30 times to ensure the stability of the device's off-state leakage path and to identify any potential device degradation. Each $V_{DS}$ ramp was completed within 20 seconds, and the transfer characteristics of the devices were measured within 10 seconds after each ramp. It is worth noting that the off-state leakage current density remained fairly constant until the $V_{DS}$ ramp reached 200V, after which a twofold increase in gate leakage current starting at $V_{DS}$ ramp = 300V is observed for GaN channel HFETs. This led to the establishment of an irreversible gate current leakage path, as depicted in Fig. 3.13 (b), confirmed after several weeks, indicating persistent degradation that might be attributed to the inverse piezoelectric effects [142]. In contrast, $Al_{0.23}Ga_{0.77}N$ channel HFETs exhibited remarkable performance with stable device operation up to 2000V, approaching hard breakdown voltages, as shown in Fig. 3.13 (c). This exceptional robustness of $Al_{0.23}Ga_{0.77}N$ channel HFETs under high voltages underscores the advantages of utilizing ultra-wide bandgap materials.

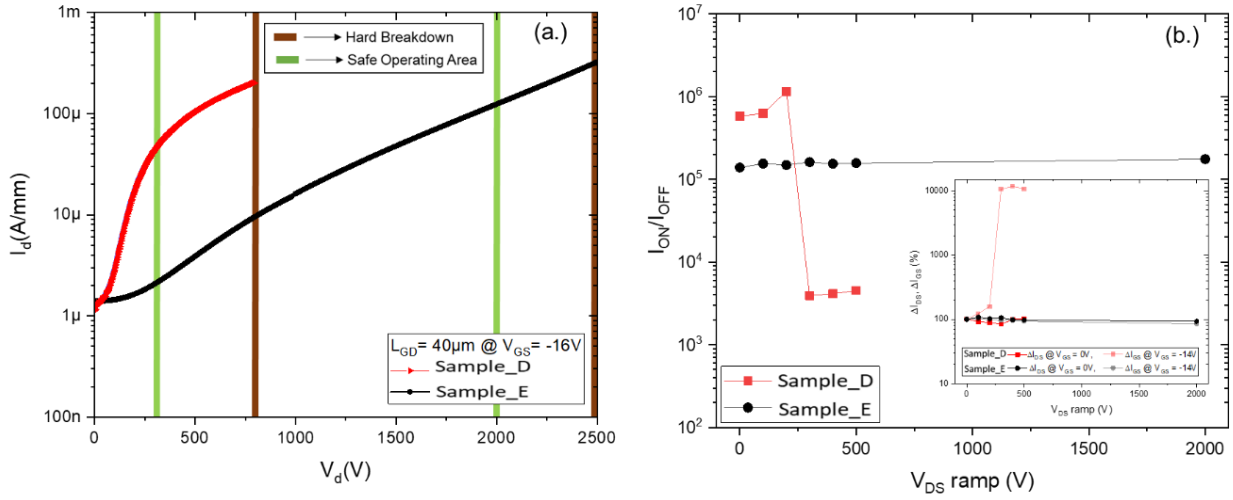



*Fig. 3. 14 (a.) Transistor voltage derating defined on drain leakage current against applied $V_{DS}$ (b.) The maximum change in gate leakage current density (inset - $I_{ON}/I_{OFF}$ ratio) for GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs for various $V_{DS}$ ramp iterations..*

When assessing the robustness of the transistors, it becomes possible to establish a voltage derating for these devices by defining the safe operational off-state blocking voltage based on the hard breakdown voltage. In our measurements, the hard breakdown voltage for GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs was found to be 780 V and 2500 V, respectively. As represented in Fig. 3.14 (a), the safe operating off-state voltage for both GaN and $Al_{0.23}Ga_{0.77}N$ channel HFETs is determined as the voltage at which these devices exhibit degradation in off-state leakage current, as indicated by the vertical green lines. It is evident that around

65% voltage derating is necessary for ensuring safe off-state operation in thin GaN channel transistors. Conversely, $Al_{0.23}Ga_{0.77}N$ channel transistors require only a 20% voltage derating from their hard breakdown voltage, despite their relative immaturity. This requirement is even lower than the 30% voltage derating observed in state-of-the-art commercial GaN HEMTs and FETs [108], [146]. In Fig. 3.14 (b), we observe the maximum change in gate leakage current during robustness tests, normalized to 100% for fresh devices. $Al_{0.23}Ga_{0.77}N$ channel HFETs exhibit a maximum change in gate leakage of less than 200nA/mm up to 2000V, demonstrating the stability of gate leakage current and maintaining a highly stable $I_{ON}/I_{OFF}$ ratio (as shown in the inset of Fig. 3.14 (b)). In contrast, GaN channel HFETs experience significant fluctuations in leakage from the fresh device after each $V_{DS}$ sweep due to the generation of permanent leakage paths.

### 3.2.6 Impact of SiN and High-Temperature Operation

In the early 2000s, GaN HEMTs displayed sensitive sheet charges on the surface that have been responsible for the current collapse and high RF dispersion under high drain bias. These effects of surface trapping states can be suppressed or controlled by SiN passivation [147]. The gate dielectric is an important parameter that is carefully optimized in order to suppress the peak electric field on the gate edge of the drain side and aids surface passivation, giving better 2-DEG confinement. However, the gate dispersion effects due to SiN under hot electron stress are significant and might be further improved by in-situ SiN passivation [148], [149]. Hence, we fabricated AlGaN channel MIS-HFETs and metal-

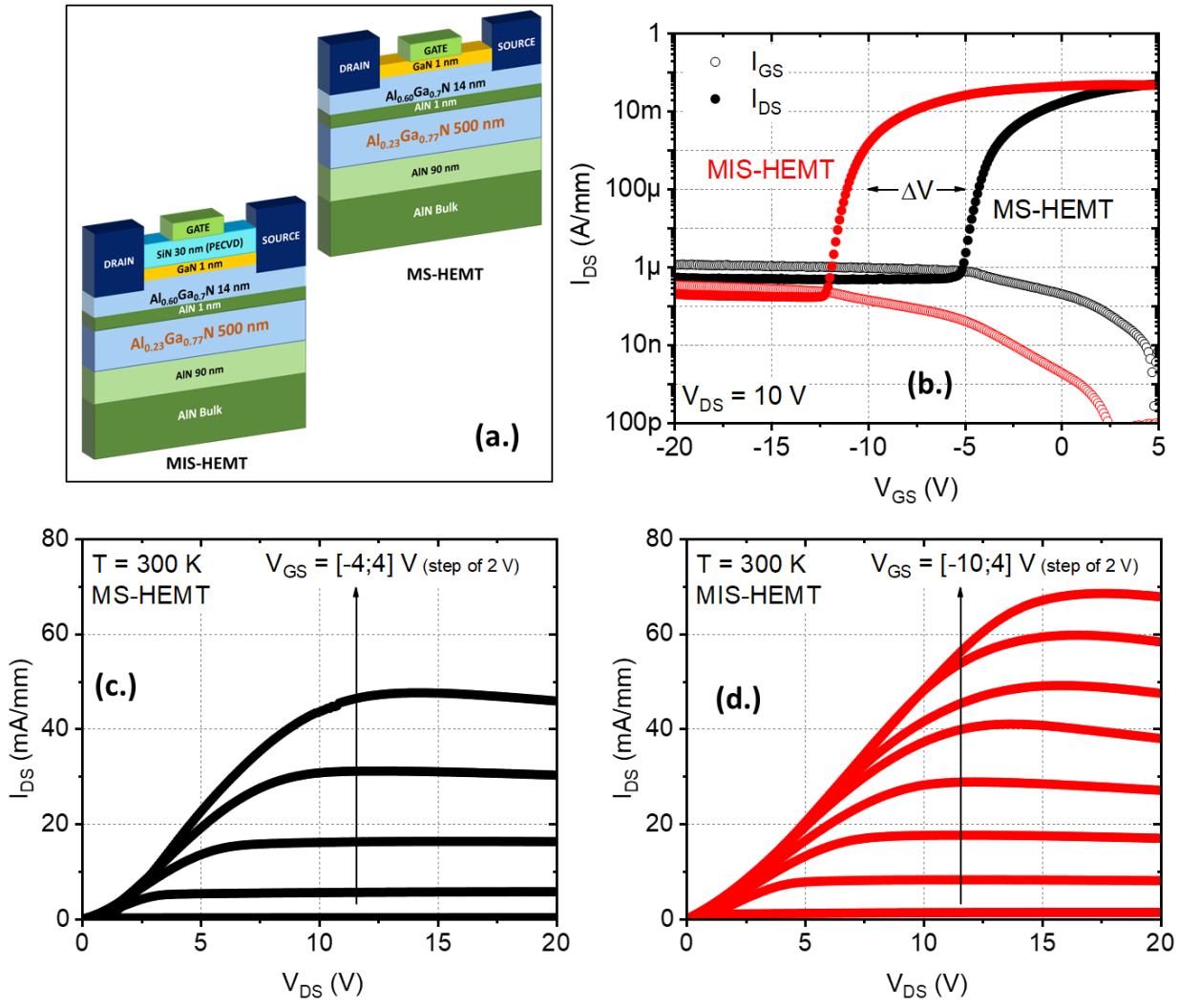



*Fig. 3. 15 (a.) Schematic of structures with and without SiN passivation, (b.) transfer characteristics measured at $V_{DS}$=10V, output characteristics of (c.) MS-HEMT (without SiN) and (d.) MI SHEMT (with SiN)*

semiconductor (MS)-HFETs to understand the impact of SiN on the device's DC characteristics and the breakdown voltage. Furthermore, their high-temperature DC measurements were carried out with a Keithley 2612B Source Measure Unit in a dark environment, with a temperature range from 300K to 600K. Fig. 3.15 (a) illustrates the schematic diagram of fabricated MIS-HFETs and MS-HFETs. The transfer characteristics of fabricated MIS-HFETs and MS-HFETs with $L_{GD}$=20 µm and $L_G$=3 µm measured at $V_{DS}$ = 10V showed low drain current leakage with more negative $V_{TH}$ for MISHEMTs and lower off-state leakage owing to 30nm SiN below gate (see Fig. 3.15 (b)). The output characteristics showed 20mA/mm higher currents for MIS-HEMTs at $V_{GS}$ = 4V confirming better 2DEG confinement

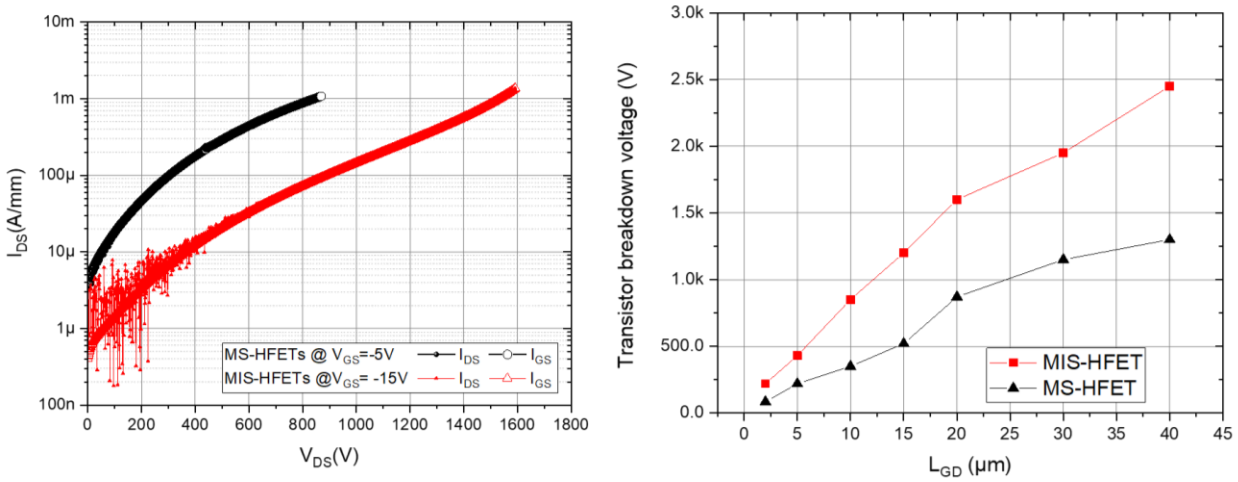



*Fig. 3. 16 Transistor breakdown voltage for devices with $L_{GD}$=20 µm (left) and Evolution of transistor breakdown voltage with various $L_{GD}$ (right) for MIS-HFETs and MS-HFETs*

as shown in Fig. 3.15 (c), (d). The transistor breakdown measurements reveal almost 3× improvement in breakdown voltage with 30nm SiN gate dielectric as defined at 100µA/mm, shown in Fig. 3.16 (left). The breakdown voltage slope of around 36V/µm for MS-HFETs rises to almost 77V/µm for MIS-HFETs up to 20 µm gate-drain spacing, summarizing the improved electrical breakdown performance and lower off-state leakage characteristics using SiN as gate dielectric. The DC (T) measurements reveal excellent output characteristics for both structures with low current dispersion up to 600 K. Fig. 3.17 (a),(b.) illustrates the drain and gate leakage characteristics of MS-HEMTs with consistent $V_{TH}$ over the measured temperature range due to large Schottky barrier height at the metal-semiconductor interface [150]. However, the MIS-HFETs showed a positive shift in $V_{TH}$ evolving with temperature as illustrated in Fig.3.17 (c). The increase of $I_{GS}$ with temperature at $V_{GS}$ = 0V shows the impact

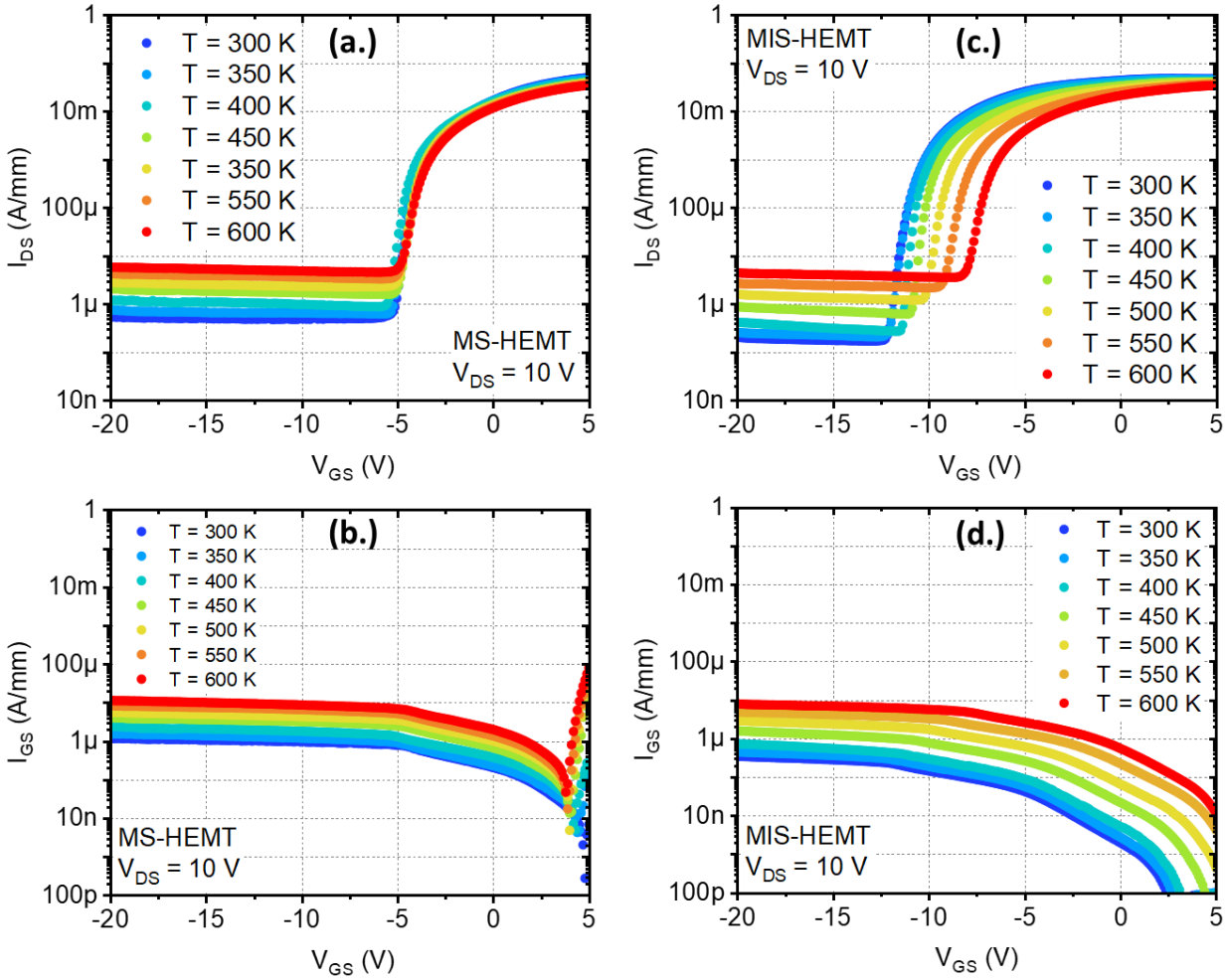



*Fig. 3. 17 Transfer characteristics along with gate current leakage evolution with applied $V_{DS}$ = 10V for AlGaN channel (a.), (b.) MS-HEMT and (c.), (d.) MIS-HEMT measured over 300 K – 600 K temperature range.*

of interface trapping caused by the increased acceleration of kinetic electrons through the dielectric with increasing temperature [151]. The normalized change in maximum drain current density measured at various temperatures is shown in Fig. 3.18 (a), where the MIS-HFETs and MS-HFETs showed 10% and 15% drain current dispersion at 400 K. The dispersion is consistent with the increasing temperature with lower values for MIS-HFETs. The evolution of $V_{TH}$ instability with temperature for MIS-HFETs and MS-HFETS is shown in Fig. 3.18 (b). The change in threshold voltage $\Delta V_{TH}$ = 4V measured from 300 – 600K may be due to the presence of SiN/AlGaN interface trap states [152]–[154]. The electron trapping from the 2DEG eventually reduces the electron concentration at the AlGaN/AlGaN interface resulting in less negative $V_{TH}$ [155]. More detailed analysis of surface and bulk trapping, time-

dependent dielectric breakdown (TDDB) analysis, and bias-temperature instability (BTI) measurements are necessary to study the impact of SiN on dispersion effects under high voltage.

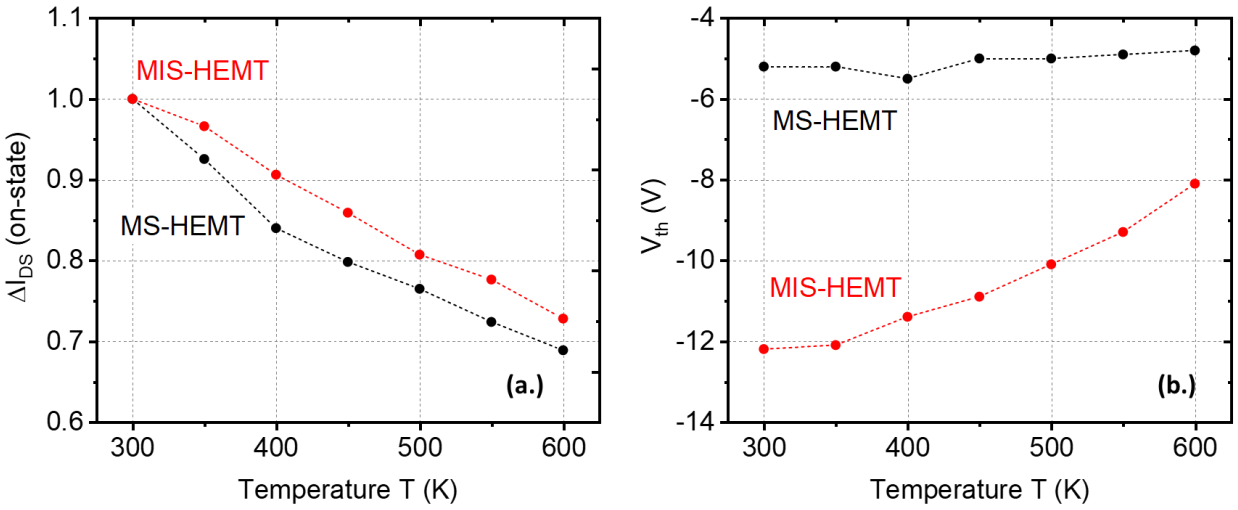



*Fig. 3. 18 (a.) Change in on-state drain current density normalized at 300 K and (b.) threshold voltage evolution measured over 300 K - 600 K temperature range.*

### 3.2.7 Self-Heating Temperature Measurements

The GaN and AlGaN-based HFETs on AlN demonstrated high voltage operation with considerable on-state currents. However, during continuous operation, the channel temperature rises due to the generation of peak electric field hotspot at the drain side of the gate edge, eventually inducing dispersion in output currents. This can damage the material lattice permanently and impact the reliability of power HFETs. Hence, the determination of a well-dissipated channel is a must to reduce self-heating induced degradation. Thus, a 500nm thick GaN and AlGaN channel based HFETs fabricated on bulk AlN are used in this study to evaluate the impact of bulk AlN as well as GaN and AlGaN channel on the device operating temperature. The devices used in this experiment were composed of $L_G$ = 3µm, $L_{GD}$ = 10µm, and $L_{GS}$ = 2 µm. Fig. 3.19 shows the schematic diagram of GaN and AlGaN channel MIS-HFETS along with the cerium oxide ($CeO_2$) microparticles, which act as micro-Raman thermometers, were scattered in ethanol solution and then deposited on the device surface by spin-coating.

The self-heating temperatures of the biased components were estimated using Raman spectroscopy by researchers at GREYC laboratory, CAEN, France. A Helium-neon laser was used as an excitation source with a wavelength of 632.8 nm, and Raman spectra were measured in a backscattering configuration at room temperature using an InVia RENISHAW Raman spectrometer. The devices were placed on an XYZ mapping stage controlled by a computer with a step size of 0.1 µm. A microscope allowed to focus the excitation laser on the sample and to collect the Raman scattered signal to achieve a high spatial resolution. So, the spatial and spectral resolutions were 0.8 µm and 1.0 $cm^{-1}$, respectively. The temperature accuracy estimated from the phonon frequencies and linewidth changes is close to 5 K. In this experiment, we have extracted the operating

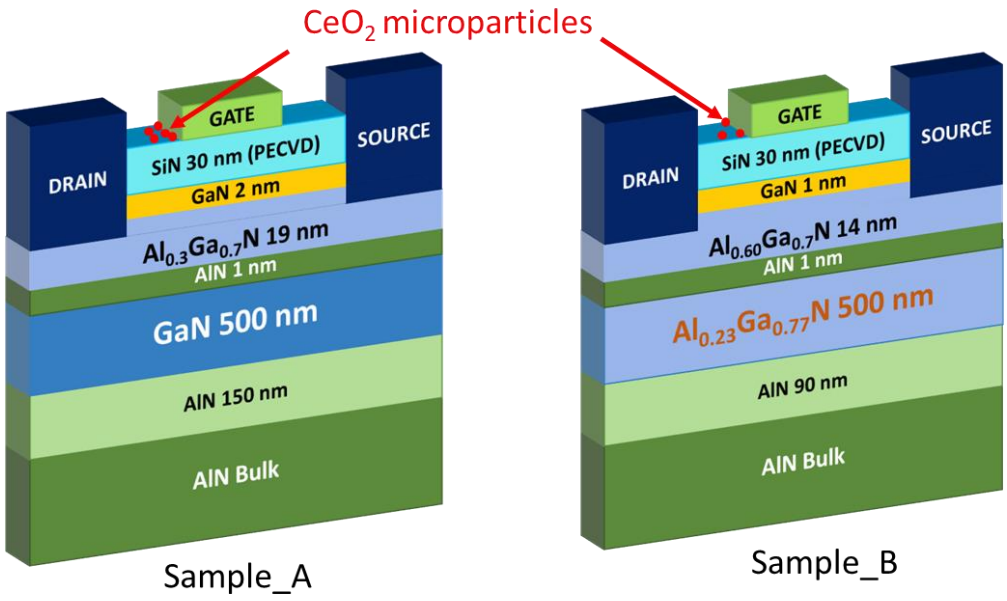



*Fig. 3. 19 Schematic of GaN and AlGaN channel MIS-HFETs with surface deposited $CeO_2$ microparticles.*

temperature of the device surface from the $F_{2g}$ ($\delta CeO_2$) mode of the $CeO_2$ microparticles and that of a volumetric AlN layer average from $E_2$(high) mode [156], [157].

To extract the self-heating temperature of biased AlGaN/(Al)GaN HEMTs, the changes in the phonon frequencies and linewidths related to the $\delta CeO_2$ and $\delta$AlN Raman modes with increasing temperature have been measured by using a Linkam TS-1500 high-temperature cell. This equipment enables a material sample up to 7 mm in diameter to be held at the desired temperature, which can vary from ambient up to 1500 °C with a temperature accuracy of 1 K. The top lid seals the chamber and has a small glass window mounted above

a ceramic crucible, which contains the sample. The technological structure of the GaN-based devices measured to obtain the calibration curves is the same as that of biased components thermally characterized.

Fig 3.20 (a.) and (b.) demonstrate the calibration of Raman shift (δ) and linewidth shift (Γ) for the surface deposited $CeO_2$ microparticles and AlN substrate for GaN and AlGaN channel HFETs respectively. The decrease in Raman phonon frequencies for $\delta CeO_2$ and δAlN modes can be observed for both the samples with the increasing temperature. However, the effect of temperature is more pronounced on the phonon frequencies than on their line widths as observed in the calibration curves shown in Fig. 3.20 [158]. The increase in linewidth is visible for both $CeO_2$ and AlN modes with a rise in the temperature.

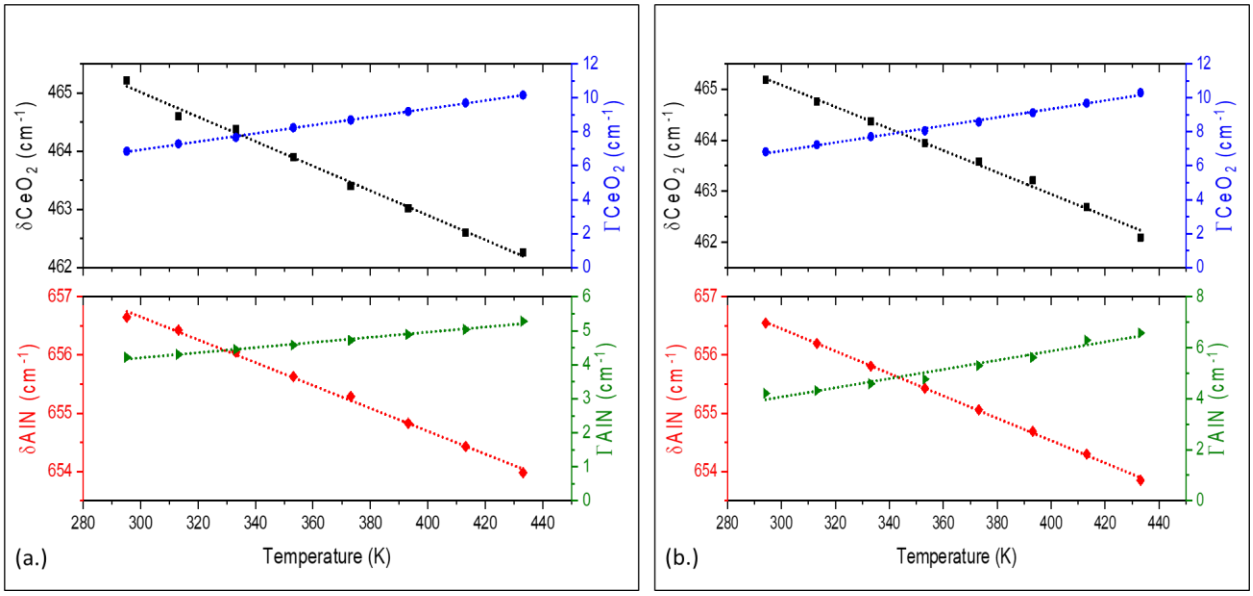



*Fig. 3. 20 Temperature dependence of δAlN (substrate/nucleation) and $\delta CeO_2$ (close to the gate) along with their linewidth shift for (a.) 500nm GaN channel HEMT and (b.) 500nm AlGaN channel HFET*

The impact of dissipated power ($P_D$) on the self-heating temperature is estimated from the change in phonon frequencies related to $CeO_2$ and AlN for GaN and AlGaN channel HFETs. Fig 3.21 (a.) shows a linear increase in self-heating temperatures for the surface near the hotspot of GaN channel HEMT and also for the bulk AlN substrate [159]–[161]. However, for AlGaN channel HFETs, the temperature change follows a quadratic fitting showing a high rate of temperature change with dissipated power as compared to the GaN channel indicating higher channel temperatures as expected from the incorporation of Al in the channel [84]. This low dissipated power non-linearity in the thermal resistance ($R_{th}$) for AlGaN channel

HFET can be attributed to saturation of on-state current and also due to its non-ohmic device behavior (see Fig 3.10). Considering the linear regime, the extracted values of $R_{th}$ for GaN and AlGaN channel HFETs are 7.3°C mm/W and 12.3 °C mm/W, respectively. The thermal resistance of the AlN substrate is below 3°C mm/W. The GaN channel HEMT shows a temperature change (ΔT) of around 54°C whereas the AlGaN channel HFET shows ΔT=94°C at 9W/mm dissipated power. This experimentally proves that AlGaN channel HFETs have much higher channel temperatures compared to GaN channel HEMTs for a device with $L_{GD}$=10µm. However, the high-temperature operation of AlGaN channel HFETs showed < 30% dispersion in on-state current measured up to 600K. Hence, AlGaN channel HFETs can operate at high channel temperatures with low dispersion which is mainly a consequence of increased alloy scattering [98], [162].

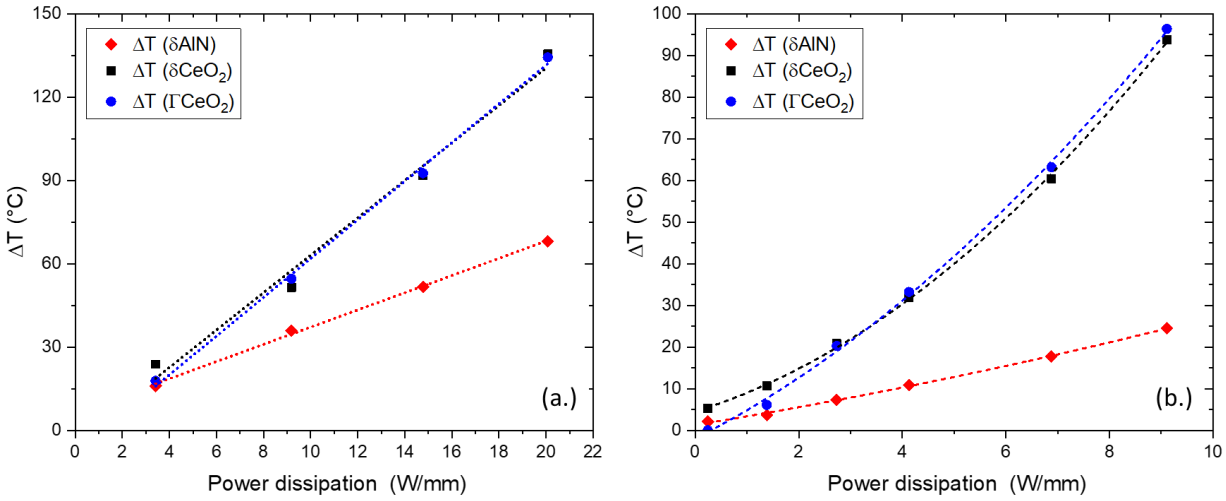



*Fig. 3. 21 Impact of power dissipation on the self-heating temperatures (ΔT) measured from $\delta CeO_2$, $\Gamma CeO_2$, and δAlN components for (a.) GaN channel HEMTs (linear fit) and (b.) AlGaN channel HFETs (quadratic fit)*

### 3.2.8 State-of-the-Art

The state-of-the-art AlGaN channel HFETs with Al composition below 50% in the channel are demonstrated in Fig. 3.22. All the other work presented in this plot uses source/drain (ohmic) contact optimization techniques such as n+ GaN regrowth, different metal stacks, graded barrier, doped barrier, and hybrid contacts whereas no source/drain contact optimization was done in this work. This shows the huge potential for low Al-content AlGaN channels on bulk AlN to outperform GaN HEMTs with high current density alongside high breakdown voltages. This high voltage performance combined with high-temperature stability and high voltage robustness gives room for AlGaN-based HFETs for developing extreme power devices surpassing conventional IGBTs and MOSFETs for efficient switching in kV's. However, the charge trapping effects within AlGaN HFETs are yet to be explored which is crucial for dynamic switching and determining the efficiency of the power devices.

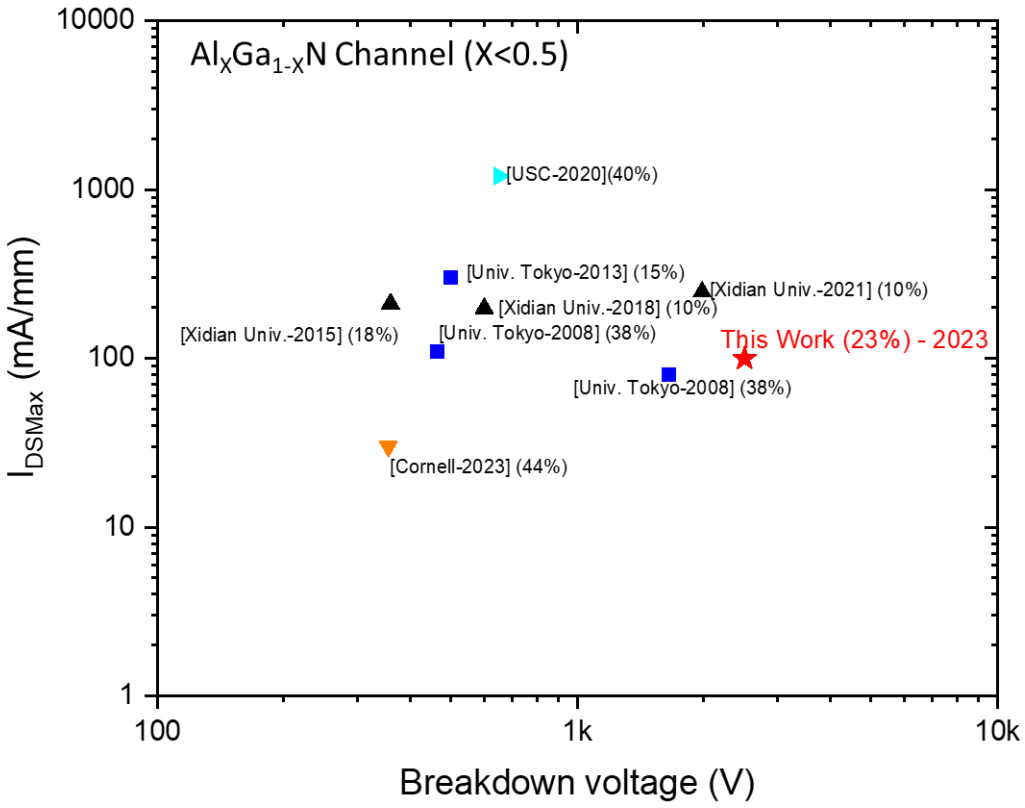



*Fig. 3. 22 State-of-the art AlGaN channel HFETs with <50% Al content in the channel.*

## 3.3 Ohmic contact to Al-rich AlGaN

### 3.3.1 Device Fabrication

The device structure is composed of a thin (380nm) and thick (1010nm) AlGaN channel with 60% Al content with a 10nm thin 90% AlGaN barrier and 1nm AlN spacer. Considering the buffer, the sample_A contains a 200nm AlN nucleation below the channel whereas the sample_B contains a 360nm $Al_{0.15}Ga_{0.85}N$ interlayer sandwiched between 200nm AlN as shown in Fig. 3.23 The device fabrication started with source/drain contact patterning using a 200nm $SiO_2$ mask and the patterns were etched in ICP-RIE by tens of nm

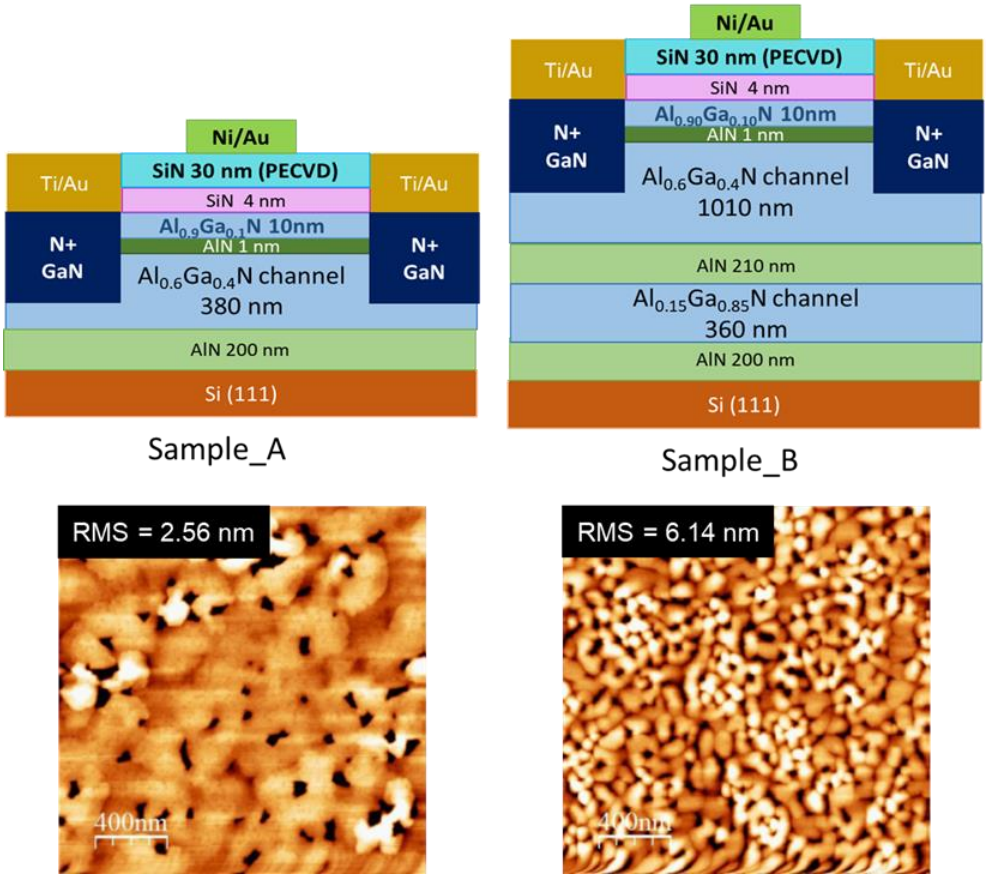



*Fig. 3. 23 Schematic diagram of sample_A (thin AlGaN channel) and sample_B(thick AlGaN channel) HFETs along with the AFM scans of GaN n+ contacts after regrowth.*

below the 2-DEG in order to implement selective area regrowth aiming to achieve high current density with Al-rich AlGaN channel [97]. The 100nm GaN regrowth was achieved by $NH_3$-MBE with an estimated Si doping concentration of $1.1 \times 10^{20}$ $cm^{-3}$ and $3.4 \times 10^{20}$ $cm^{-3}$ for sample_A and sample_B respectively. The AFM scans after regrowth reveals RMS roughness of 2.56 nm and 6.14 nm for sample_A and sample_B respectively as shown in Fig. 3.23.

| Sample | Sheet Resistance [ohm/sq.] | Mobility [$cm^2/V.s$] | Concentration [$cm^{-2}$] |
|---|---|---|---|
| Sample_A | 5906 | 141 | $7.47 \times 10^{12}$ |
| Sample_B | 1908 | 206 | $1.59 \times 10^{13}$ |

*Table 3. 4 Hall Effect measurements extracted 2DEG properties for thin and thick AlGaN channel MISHFETs*

The n+ GaN regrowth was achieved along with the metal contacts fabricated by e-beam evaporation of Ti/ Au metal stack with a 30s wet etch in BOE solution before the metallization. The $L_{GD}$ and $L_{GS}$ are 5 to 40 µm and 1.5 µm, respectively. A 220 nm and 340 nm MESA isolation was achieved using $Cl_2$/Ar plasma by ICP-RIE for sample_A and sample_B respectively. A 30 nm thick PECVD SiN aided in the passivation of the device surface while being used as a gate dielectric. Finally, a 220 nm Ni/Au metal stack was evaporated on top of SiN to fabricate gate electrodes with 2.5µm gate length, yielding MISHFETs. The SEM picture of isolation bar pattern after mesa isolation for sample_A is illustrated in Fig. 3. 24 showing the n+-GaN layer with Ti/Au metal contacts atop along with their measured distances.

The Hall effect measurements (table 3.4) of these samples reveals low 2-DEG concentration of $7.47 \times 10^{12}$ $cm^{-2}$ and 141 $cm^2$/ V. s electron mobility for thin AlGaN channel structure, whereas the thicker channel structure comparatively shows 45% higher 2-DEG

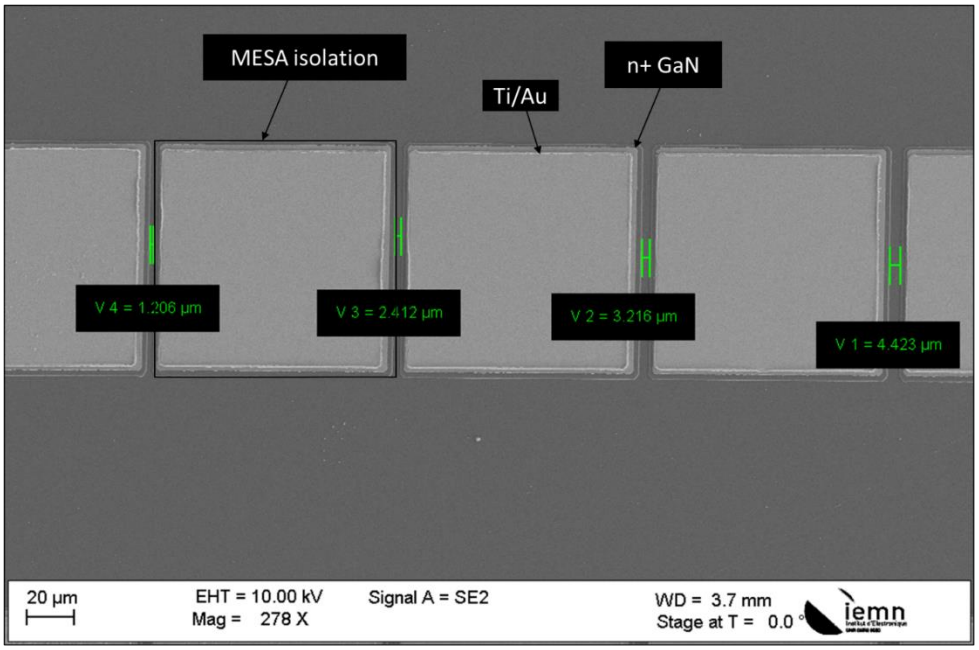



*Fig. 3. 24 SEM image of isolated bar pattern showing various regions of contacts along with their spacing.*

mobility along with double 2-DEG concentration. The 2-DEG properties of 1µm thick AlGaN channel device is among state of the art Al-rich AlGaN channel HFETs [89], [99].

### 3.3.2 DC Characterization

Electrical measurements at room temperature were carried out using a Keysight B1505A Power Device Analyzer / Curve Tracer. The transfer characteristics of the fabricated devices indicate that the MIS-HEMTs are fully operational, displaying a high on-off ratio (>$10^6$) in both samples with on-state current density in agreement with the sheet resistances (refer to Table 3.3). The transfer characteristics were evaluated at a drain-source voltage ($V_{DS}$) of 10V for devices with $L_{GD}$ of 350 nm and 510 nm for sample_A and sample_B

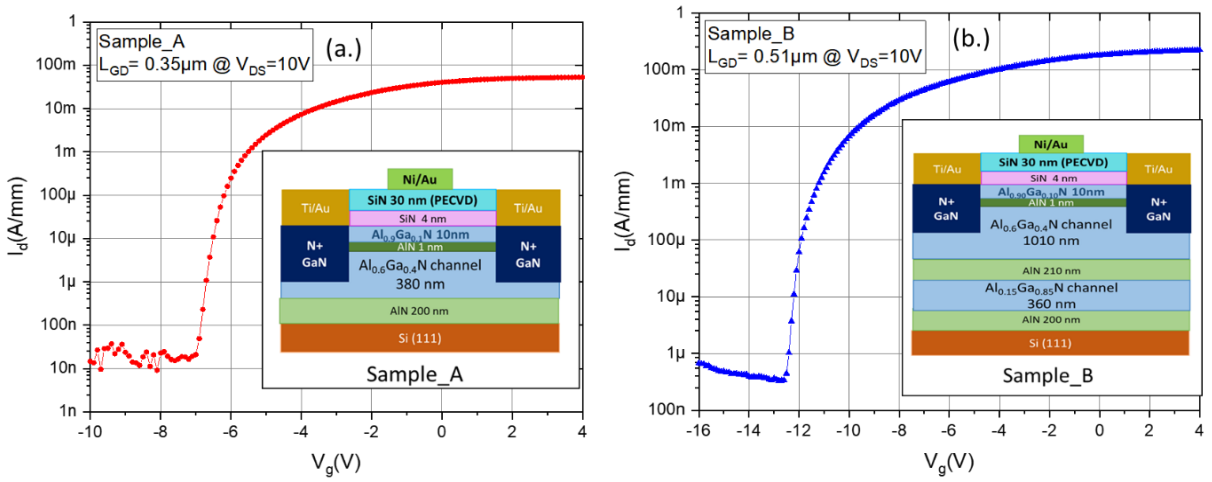



*Fig. 3. 26 Transfer characteristics of Al-rich AlGaN channel HFETs with (a.) thin AlGaN channel and (b.) thick AlGaN channel measured at $V_{DS}$ = 10V.*

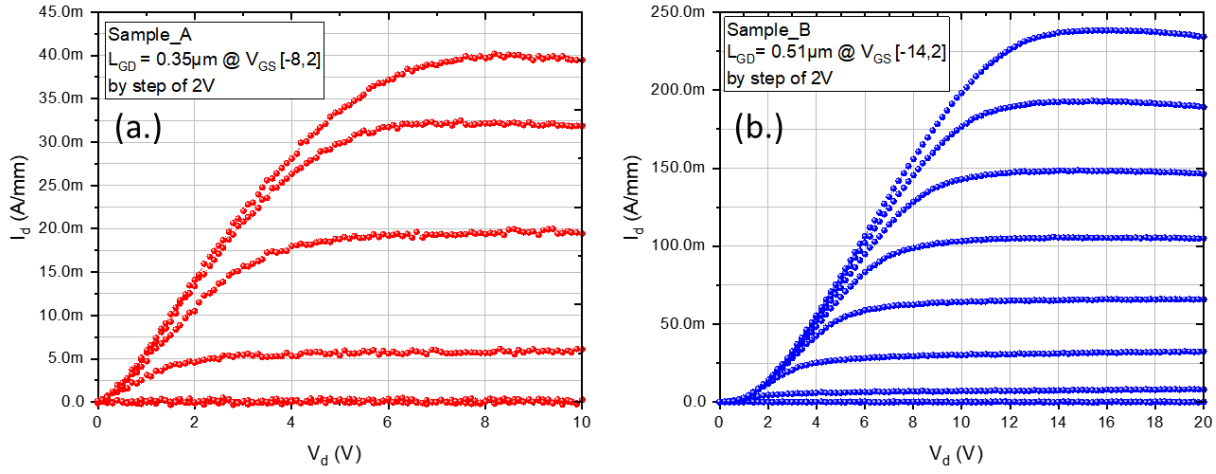



*Fig. 3. 25 Output characteristics of Al-rich AlGaN channel HFETs with (a.) thin AlGaN channel (sample_A) and (b.) thick AlGaN channel (sample_B) measured at $V_{DS}$ = 10V.*

respectively, as depicted in Fig. 3.26. The maximum drain current reached 40mA/mm and 235 mA/mm for sample_A and B respectively with $V_{GS}$ swept from -10 V to +4 V. The extracted specific contact resistance for sample_A and sample_B are 8.24 mΩ.cm$^2$, and 2.63 mΩ.cm$^2$ respectively. In the case of sample_B, the drain-source contacts displayed Schottky turn-on behavior as depicted in Fig. 3.25 (b). This turn-on behavior is supposed to be major consequence of surface oxidation. Therefore, surface preparation before regrowth and metallization, along with optimization of the etching technique before regrowth are necessary to achieve low-resistance source/drain contacts. Moreover, the doping concentration of Si might exhibit a knee behavior beyond a certain value of dopants with an Al-rich AlGaN channel eventually impacting the quality of ohmic contacts [160], [161].

### 3.3.3 Buffer breakdown characteristics

The measurements were realized using a Keysight B1505A Power Device Analyzer / Curve tracer. The samples were immersed in fluorinert-FC40 liquid during the measurements to avoid arcing in air. Fig. 3.27 shows the lateral buffer breakdown field between 100 × 100 $\mu$m isolated ohmic contacts with various short distances. As expected, the lower contact spacing shows a breakdown field averaging 2.4 MV/cm for sample_B. An

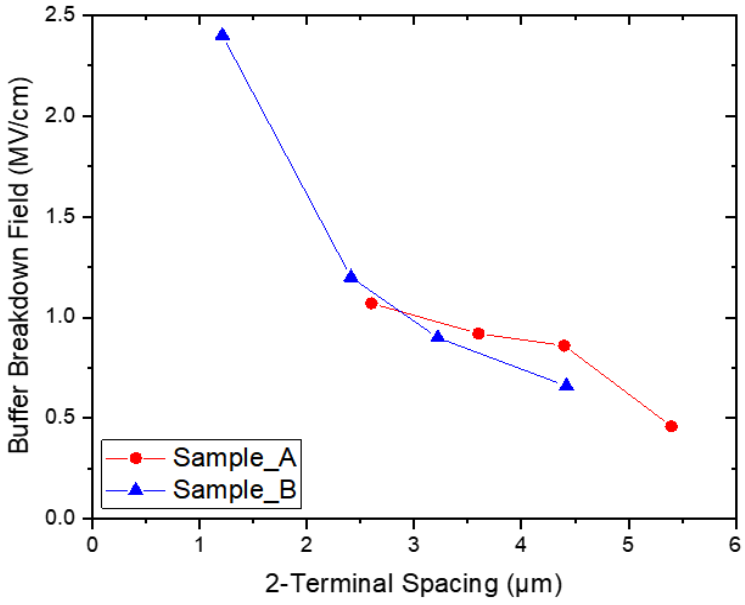



*Fig. 3. 27 Buffer breakdown electric field evolution with contact spacing*

approach towards optimization of the high resistive buffer may lead to much higher buffer breakdown fields beyond the limitations of GaN HEMTs.

### 3.3.4 Transistor breakdown characteristics

The transistor breakdown measurements for sample_A and sample_B are shown in Fig. 3. 29 The drain and gate leakage characteristics show almost 2-fold difference in both structures revealing the breakdown is initiated by the drain current injection into the silicon substrate. The devices with very low gate-drain spacing below 1 µm show high electrical breakdown voltage of around 175 V and 285 V at $V_{GS}$ =-7 V and $V_{GS}$ =-14 V for sample_A and sample_B respectively. These breakdown values summarize a very high 3-terminal breakdown field of more than 5 MV/cm. The summary of transistor breakdown voltages with

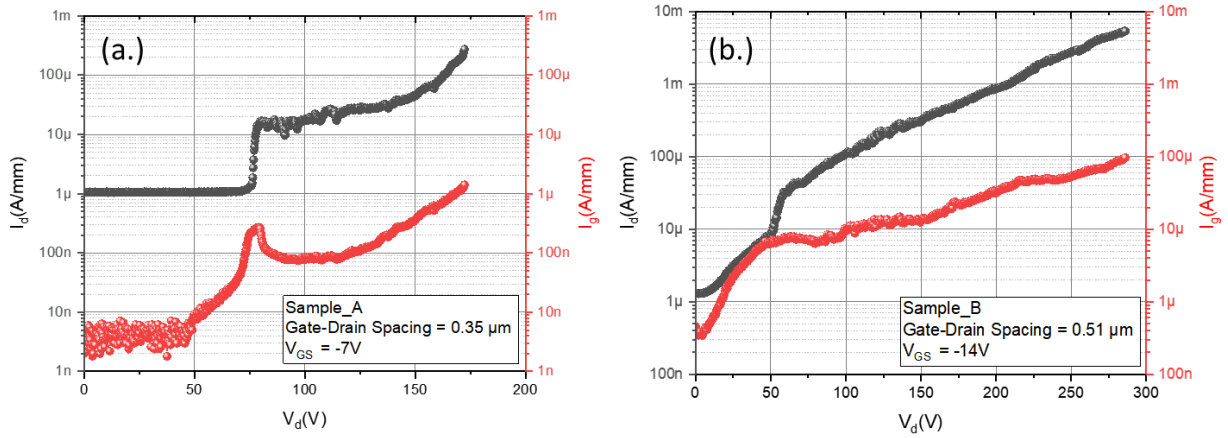



*Fig. 3. 28 Transistor breakdown characteristics of (a.) thin AlGaN channel and (b.) thick AlGaN channel MISHFETs*

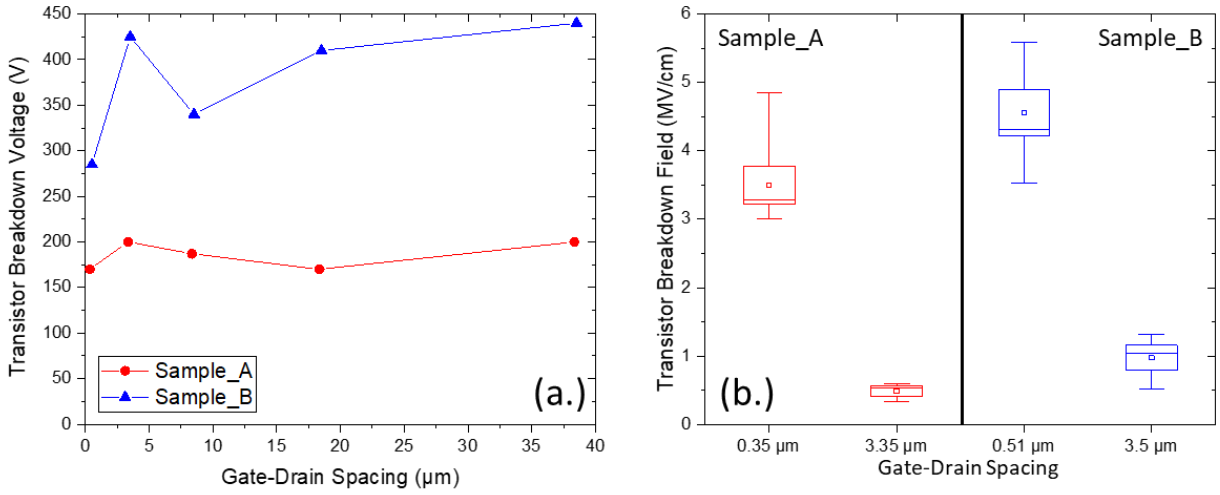



*Fig. 3. 29 Summary of (a.) transistor breakdown voltage with gate-drain spacing and (b.) evolution of transistor breakdown field with gate-drain spacing.*

different gate-drain spacing is shown in Fig. 3.28(a.), demonstrating a saturation in breakdown voltage due to Si substrate starting from low GD spacing. The transistor breakdown voltage saturates around 200 V and 425 V for sample_A and sample_B respectively. The impact of this saturation is visible in the breakdown field plot shown in Fig. 3.28(b.) with the sharp decrement of transistor breakdown field with increased gate-drain spacing. The thin AlGaN channel structure showed an average breakdown field of 3.5 MV/cm for 0.35 µm GD spacing which reduces to almost 0.5 MV/cm for 3.35 µm GD spacing. The 1µm thick AlGaN channel HFETs showed a scaling from 4.5 MV/cm breakdown field to almost 1 MV/cm. These results favorably compares to the state-of-the-art AlGaN channel devices worldwide. The high breakdown field of AlGaN channel HFETs on Si is demonstrated in Fig. 3.30 which is beyond the theoretical limits of GaN.

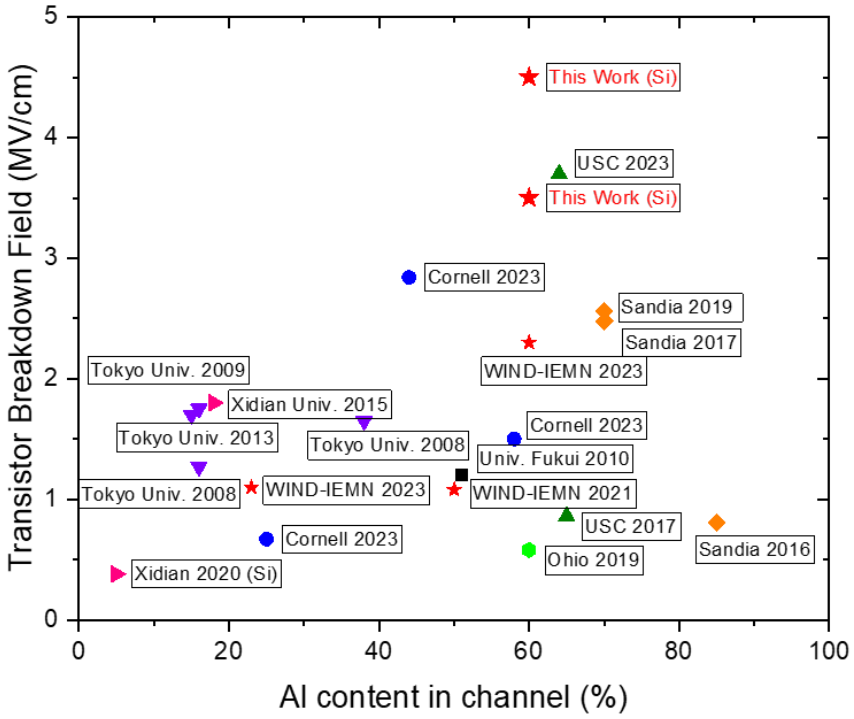



*Fig. 3. 30 State-of-the-art AlGaN devices with the transistor breakdown field evolution with Al content in the AlGaN channel*

## 3.4 Conclusion

To summarize the first part, we have successfully demonstrated the first AlGaN/AlGaN MIS-HFETs on silicon substrates, incorporating various channel compositions with Al mole fractions of 0.1, 0.3, and 0.6. Notably, AlGaN channel devices exhibited an impressive buffer breakdown field exceeding 2.5 MV/cm, which is nearly 8× higher than the critical electric field of silicon. A key discovery from this work is the potential to achieve such a high buffer breakdown field while significantly reducing the device dimensions to submicron gate-drain distances. These results underscore the potential for advancing beyond traditional GaN devices, enabling the development of highly miniaturized components capable of operating at high voltage levels. Additionally, the DC characteristics at various temperatures indicate exceptional thermal stability in Al-rich AlGaN channel devices, suggesting the possibility of creating robust power electronics on silicon substrates suitable for harsh environments, which is a more cost-effective alternative than GaN and AlN bulk substrates. The primary challenge ahead lies in optimizing the design of ohmic contacts to Al-rich $Al_xGa_{1-xN}$ channels to ensure power devices with both high breakdown fields and low on-state resistances. Implementing thick Al-rich buffer layers may offer a solution for producing AlGaN channel HEMTs with multiple kilovolts of breakdown voltage on large-diameter silicon substrate wafers.

In the second study, AlGaN channel and GaN channel HFET heterostructures were epitaxially grown on AlN bulk substrates. HRXRD and AFM scans revealed superior crystal quality and lower surface roughness in $Al_{0.23}Ga_{0.77}N$ channel HFETs as compared to the GaN channel HFETs. This improvement is attributed to the reduced lattice mismatch between $Al_{0.23}Ga_{0.77}N$ and the AlN substrate. $Al_{0.23}Ga_{0.77}N$ channel devices exhibited a maximum drain current density up to 320 mA/mm and specific $R_{ON}$ as low as 4 $m\Omega.cm^2$ in the linear operating region, despite ongoing optimization possibilities for the drain/source ohmic contacts. Lateral breakdown measurements demonstrated the high-quality nature of the AlN bulk material, with a critical breakdown field reaching 10 MV/cm with narrow contact spacings. Transistor breakdown voltages were found to scale with gate-drain spacing for both device types. $Al_{0.23}Ga_{0.77}N$ channel devices exhibited a hard breakdown voltage of up to 2500 V, in contrast to 780V for GaN channel HFETs. The Lateral power figure of merit for the fabricated

$Al_{0.23}Ga_{0.77}N$ and GaN channel HFETs is approximately 120 MW/cm$^2$ and 32 MW/cm$^2$, respectively. Remarkably, $Al_{0.23}Ga_{0.77}N$ channel HFETs delivered reliable performance up to 2000 V, while GaN channel HFETs exhibited permanent degradation after reaching 300 V during on-wafer testing. These robustness tests further confirmed the reliability of $Al_{0.23}Ga_{0.77}N$ channel HFETs, with only a 20% voltage derating compared to the more substantial 50% derating observed in the case of GaN channel HFETs. The DC (T) measurements on $Al_{0.23}Ga_{0.77}N$ channel HFETs show reliable high-temperature operation measured in the 300 K - 600 K temperature range. The $Al_{0.23}Ga_{0.77}N$ channel MS-HFETs showed high threshold voltage stability up to 600 K. However, $Al_{0.23}Ga_{0.77}N$ channel MIS-HFETs showed a positive shift in threshold voltage attributed to the SiN trapping effects below the gate. Thus, the investigation of BTI, threshold voltage instability, trapping, and de-trapping effects in the heterostructures under high voltages are essential to ensure reliable high-temperature operation with low dispersion. The self-heating temperature measurements $Al_{0.23}Ga_{0.77}N$ channel MISHFETs revealed almost 1.7× higher channel temperatures owing to low thermal conductivity as compared to GaN channel HEMTs.

Novel AlGaN channel HFETs show huge potential for the development of kV regime power switches under harsh environments owing to their superior material properties. The major challenge associated with Al-rich devices is to develop ohmic contacts to the 2DEG. To address this issue, we have demonstrated selective area regrowth of Si-doped GaN in the source/drain region, an approach towards ohmic contact development to Al-rich AlGaN channel HFETs. The thick $Al_{0.6}Ga_{0.4}N$ channel HFETs demonstrated state-of-the-art $I_{DSmax}$ = 235 mA/mm with an associated specific $R_{ON}$ = 2.63 mΩ.cm$^2$ [97]. These structures showed a very high transistor breakdown field of more than 5 MV/cm for less than 1 μm gate-drain spacing which is not reachable with GaN HEMTs resulting in LFOM = 30 MW/cm$^2$. Moreover, buffer optimization on Si is a key to scaling up such high electric fields for mm-sized power devices. Furthermore, the optimization of ohmic contacts, surface preparation, grading, and doping of the contacts or in the barrier may conclude AlGaN-based HFETs with several GW/cm$^2$ FOM.

# General Conclusion

The reliable operation of transistors requires not only high-quality epitaxy but also the incorporation of appropriate fabrication process design and equipment-specific optimization for each step. The validation of the substrate is essential to verify the structural and electrical quality of the heterostructures grown on top. This initiated a study of GaN channel HFETs grown on Silicon and bulk AlN substrates. The measurements necessary to characterize the MISHEMTs were shown. Both GaN-on-Si and GaN-on-AlN devices showed a high $I_{ON}/I_{OFF}$ ratio of up to $10^6$. The maximum current density up to 1.1 A/mm has been measured yeilding specific on-resistances of less than 1 mΩ. $cm^2$. The buffer breakdown field measurements of GaN-on-Si showed around 0.5 MV/cm which increased to 6 MV/cm for GaN-on-AlN using 1 μm contact spacing. Furthermore, AlN shows no electron injection into the substrate during device operation, which is one of the major causes of electrical failure in GaN-on-Si based FETs used for high-voltage applications. Thus, it can be concluded that bulk AlN substrate may pave the way for pushing device operation into the kV regime. Hence, a study based on variation in GaN channel thickness has been accomplished with the heterostructures grown on bulk AlN substrates.

The next chapter shows an experimental demonstration of GaN channel MISHEMTs on bulk AlN grown by ammonia source MBE. The GaN channel thickness downscaling showed a gradual decrease in strain relaxation while going from 500 nm to 50 nm channel thickness whereas sub 20 nm GaN channel devices showed a fully strained channel and its consequence is reflected in their low 2DEG density. The critical GaN channel thickness related to the high defect density region is estimated to be around 20-30 nm thick from the GaN/AlN interface, that degrades the 2DEG mobility. To compensate the reduction in 2DEG density, 9nm fully strained thin GaN channel devices with thick Al-rich AlGaN barrier were fabricated enhancing the 2DEG density up to $1.6 \times 10^{13}$ $cm^{-2}$. However, the thin GaN channel HEMTs were not functional due to high surface leakage. GaN channel HEMTs with ohmic contacts as low as 0.3 Ω.mm were obtained for which the contact resistances kept degrading with channel downscaling.. The buffer breakdown measurements revealed up to 7 MV/cm electric breakdown field with low leakage current highlighting the benefits of ultra-wide

bandgap material beyond the capabilities of GaN and SiC wide bandgaps. The 50nm thin GaN channel device showed a hard breakdown voltage of around 1400 V which is almost 14× higher than the 500 nm GaN HEMT. The breakdown I-V characteristics confirm the absence of electron injection into the substrate for an identical gate-drain leakage current profile. Transistor breakdown measurements showed an increase in breakdown voltage with a reduction in channel thickness, where it can be assumed that the electric field peak spreads more into AlN with thinner channel devices. 20 nm thin GaN channel HEMTs showed breakdown voltages up to 3000 V demonstrating the multi-kilovolt capability of thin GaN channel HEMTs fabricated on bulk AlN. However, considering the critical field strength, GaN is the lowest band gap material in the epi-structure which limits its high voltage capabilities, and could thus be further improved by incorporating aluminum in the channel. This led us to the development of a new series of FETs, realized by the growth of AlGaN/AlGaN heterostructures. The next chapter presented a study based on a novel AlGaN channel demonstrating an approach towards the development of high-voltage FETs.

To summarize the first study of this chapter, we have successfully demonstrated the first AlGaN/AlGaN MIS-HFETs on silicon substrates, incorporating various channel compositions with Al mole fractions of 0.1, 0.3, and 0.6. Notably, AlGaN channel devices exhibited an impressive buffer breakdown field exceeding 2.5 MV/cm, which is nearly 8× higher than the critical electric field of silicon. A key discovery from this work is the potential to achieve such a high buffer breakdown field while significantly reducing the device dimensions to submicron gate-drain distances. These results underscore the potential for advancing beyond traditional GaN devices, enabling the development of highly miniaturized components capable of operating at high voltage levels. Additionally, the DC characteristics at various temperatures indicate exceptional thermal stability in Al-rich AlGaN channel devices, suggesting the possibility of creating robust power electronics on silicon substrates suitable for harsh environments, which is a more cost-effective alternative than GaN and AlN bulk substrates. The primary challenge ahead lies in optimizing the design of ohmic contacts to Al-rich $Al_xGa_{1-x}N$ channels to ensure power devices with both high breakdown fields and low on-state resistances. Implementing thick Al-rich buffer layers may offer a solution for

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Novel AlGaN channel HFETs show huge potential for the development of kV regime power switches under harsh environments owing to their superior material properties. The major challenge associated with Al-rich devices is to develop ohmic contacts to the 2DEG. To address this issue, we have demonstrated selective area regrowth of Si-doped GaN in the source/drain region, an approach towards ohmic contact development to Al-rich AlGaN channel HFETs. The thick $Al_{0.6}Ga_{0.4}N$ channel HFETs demonstrated state-of-the-art $I_{DSmax}$ =

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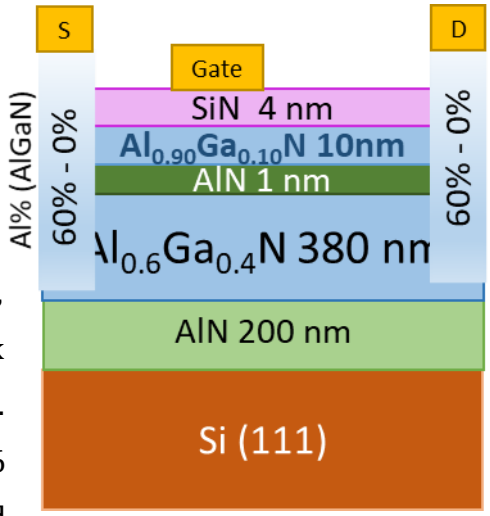
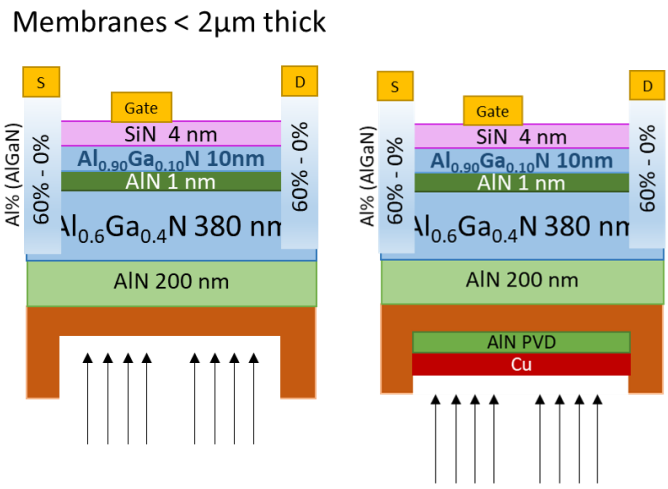
# Prospects

## Ohmic contact to AlGaN channel



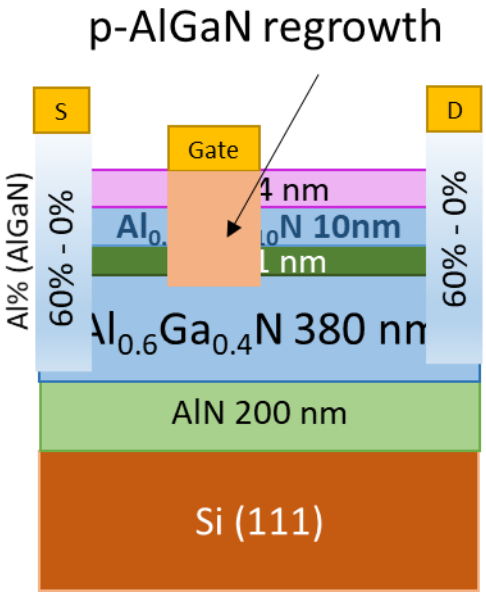

A low-resistance ohmic contact is created by minimizing the potential barrier between a metal and a semiconductor. Ideally, an n-type ohmic contact would feature minimal or zero Schottky barrier height at the interface of the metal and semiconductor, achievable through the alignment of the metal work function with the semiconductor's electron affinity. However, the inherently low electron affinity of AlN (0.6 eV) results in higher Schottky barriers when interfaced with Al-rich AlGaN, resulting in poor electron tunneling. Consequently, this leads to ohmic contacts that are highly resistive. However, taking the heterostructure grading approach by manipulating the Al alloy composition in the AlGaN channel and gradually transitioning from a wider bandgap to a narrower bandgap beneath the ohmic contacts seems to be attractive. This can also help with the lateral diffusion of electrons at the channel/ regrowth interface. This technique effectively increases the electron affinity along the graded layer, resulting in a higher electron affinity at the metal-semiconductor interface. This method has been effective in reducing the ohmic contact to the AlGaN channel [87], [93], [162]. Hence, one of the prospects of this thesis work will be to implement graded AlGaN regrowth in the source/drain contacts region to demonstrate the low-resistance ohmic contacts to Al-rich AlGaN channel on silicon.

## Local Substrate Removal




Among all the available substrates, Si is the most suitable choice for epitaxial growth due to its low cost and large size availability. However, devices fabricated on Si have the disadvantage of poor breakdown voltage due to their 0.3 MV/cm critical field strength. However, silicon can be locally removed using various physical and chemical approaches eventually removing the limitations of vertical leakage through silicon. Local substrate removal technique has been demonstrated for a decade giving exceptional device performances. The idea is to remove silicon and deposit AlN by Physical vapor deposition and then electroplate Cu to provide mechanical stability to the membrane and also aid in heat dissipation.

## Normally-Off Operation




The enhancement mode threshold voltages with positive turn-on voltages are essential for a fail-safe operation of transistors. The e-mode GaN HEMTs have been realized using a p-GaN regrowth below the gate that elevates the conduction band above the fermi level, thereby causing a local depletion of 2-DEG but showing high gate leakage currents. To overcome this limitation, regrowth of p-AlGaN below the gate is essential to compensate for the 2DEG and create a barrier strong enough to block reverse gate leakage current. Recently, Sandia Laboratories demonstrated Al-rich AlGaN channel devices with p-AlGaN regrowth under the gate giving a threshold voltage of +3.5V with low leakage currents [163]. A study related to the impact of p-doping, the etch depth, and surface treatment before regrowth on the gate characteristics of AlGaN HFETs on silicon can be realized.

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# *Scientific Contributions*

## ✓ *Conferences Talks*

**J. Mehta**, I. Abid, R. Elwaradi, Y. Cordier, F. Medjdoub, "AlGaN channel high electron mobility transistors on bulk AlN substrate", International Workshop on Nitride Semiconductors (IWN), Berlin, 2022.

**J. Mehta**, I. Abid, J. Bassaler, J. Pernot, P. Ferrandis, M. Nemoz, Y. Cordier, S. Rennesson, S. Tamariz, F. Semond, and F. Medjdoub, "Towards high buffer breakdown field and high temperature stability AlGaN channel HEMTs on silicon substrate", Compound Semiconductor Week (CSW), Michigan, 2022.

**J. Mehta**, I. Abid, T.H. Ngo, Y. Cordier, F. Medjdoub, "AlGaN/GaN HEMTs on AlN substrate for power electronics", WOCSDICE-EXMATEC, Bristol, 2021.

J. Bassaler, **J. Mehta**, I. Abid, L. Konczewicz, S. Juillaguet, S. Contreras, S. Rennesson, S. Tamariz, M. Nemoz, F. Semond, J. Pernot, F. Medjdoub, Y. Cordier, and P. Ferrandis, "Exploring gate leakage mechanisms in AlGaN channel high electron mobility transistors as a function of Al composition, gate stack configuration, and temperature", E-MRS Fall, Warsaw, 2023.

J. Bassaler, **J. Mehta**, I. Abid, L. Konczewicz, S. Juillaguet, S. Contreras, M. Nemoz, S. Tamariz, S. Rennesson, F. Semond, Y. Cordier, J. Pernot, F. Medjdoub, and P. Ferrandis, "Investigation of electron mobility in AlGaN channel heterostructures with different Al content", E-MRS Spring, Strasbourg, 2023.

Abid, Y. Hamdaoui, **J. Mehta**, and F. Medjdoub, "High Breakdown Field and Low Trapping Effects up to 1400 V in Normally Off GaN-on-Silicon Heterostructures", ECRES, Istanbul, 2022.

R. Elwaradi, C. Bougerol, **J. Mehta**, M. Nemoz, F. Medjdoub and Y. Cordier, "Investigation on GaN channel thickness downscaling in high electron mobility transistor structures grown on AlN bulk substrate", WOCSDICE-EXMATEC, Ponta Delgada, 2022

F. Donatini, **J. Mehta**, I. Abid, Y. Cordier, F. Medjdoub and J. Pernot, "Electric Field Imaging in AlGaN/GaN High Electron Mobility Transistors grown on AlN substrates", IWN, Berlin, 2022.

J. Bassaler, **J. Mehta**, L. Konczewicz, S. Juillaguet, S. Contreras, S. Rennesson, S. Tamariz, M. Nemoz, F. Semond, J. Pernot, F. Medjdoub, Y. Cordier, and P. Ferrandis, "High temperature stability of electron mobility in AlGaN channel heterostructures with different Al fractions", ICNS, Fukuoka, 2023.

## ✓ *Invited Talks*

F. Medjdoub and **J. Mehta**, "Pushing the breakdown voltage and temperature capabilities of GaN HEMTs by using UWBG Al-rich channel", E-MRS, Warsaw, 2023.

F. Semond, S. Rennesson, E. Carneiro, **J. Mehta**, and F. Medjdoub, "From research to production: how MBE can unlock GaN-on-Si technology", ICMBE, Sheffield, 2022.

F. Medjdoub, **J. Mehta**, I. Abid, Y. Cordier and F. Semond, "AlGaN Channel HEMTs for High Voltage Applications", MRS Spring Meeting and Exhibit, Honolulu, 2022.

## ✓ *Journals*

**J. Mehta**, I. Abid, R. Elwaradi, Y. Cordier, F. Medjdoub, "Robust $Al_{0.23}Ga_{0.77}N$ channel HFETs on bulk AlN for high voltage power electronics", e-Prime - Advances in Electrical Engineering, Electronics and Energy – special issue on "wide bandgap semiconductors", 5 (2023), 100263.

**J. Mehta**, I. Abid, J. Bassaler, J. Pernot, P. Ferrandis, M. Nemoz, Y. Cordier, S. Rennesson, S. Tamariz, F. Semond, and F. Medjdoub, "High Al-content AlGaN channel high electron mobility transistors on silicon substrate", e-Prime - Advances in Electrical engineering, Electronics and Energy, 3 (2023), 100114.

R. Elwaradi, **J. Mehta**, T.H. Ngo, M. Nemoz, C. Bougerol, F. Medjdoub, and Y. Cordier, "Effects of GaN channel downscaling in AlGaN–GaN high electron mobility transistor structures grown on AlN bulk substrate", Journal of Applied Physics, 133 (2023), 145705.

I. Abid, Y. Hamdaoui, **J. Mehta**, J. Derluyn and F. Medjdoub, "Low Buffer Trapping Effects above 1200 V in Normally off GaN-on-Silicon Field Effect Transistors", MDPI micromachines, 13 (2022), 1519.

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J. Bassaler, **J. Mehta**, L. Konczewicz, S. Juillaguet, S. Contreras, S. Rennesson, S. Tamariz, M. Nemoz, F. Semond, J. Pernot, F. Medjdoub, Y. Cordier, and P. Ferrandis, "Al-rich AlGaN channel heterostructures on silicon: a relevant approach for high-temperature stability of electron mobility", submitted to Advanced Electronic Materials.

J. Bassaler, **J. Mehta**, L. Konczewicz, S. Juillaguet, S. Contreras, S. Rennesson, S. Tamariz, M. Nemoz, F. Semond, J. Pernot, F. Medjdoub, Y. Cordier, and P. Ferrandis, "Temperature operation of AlGaN channel high electron mobility transistor on silicon: impact of Al fraction on device performances", to be submitted in Physical Review Applied

J. Bassaler, **J. Mehta**, L. Konczewicz, S. Juillaguet, S. Contreras, S. Rennesson, S. Tamariz, M. Nemoz, F. Semond, J. Pernot, F. Medjdoub, Y. Cordier, and P. Ferrandis, "Trap detection in an AlN on Si (111) layer and in an $Al_{0.60}Ga_{0.40}N$ channel heterostructure grown on Si (111) substrate", to be submitted in APL special topic (ultra)wide bandgap semiconductors

J. Bassaler, **J. Mehta**, L. Konczewicz, S. Juillaguet, S. Contreras, S. Rennesson, S. Tamariz, M. Nemoz, F. Semond, J. Pernot, F. Medjdoub, Y. Cordier, and P. Ferrandis, "High-temperature stability of an $Al_{0.30}Ga_{0.70}N$ channel high electron mobility transistor grown on a Si (111) substrate", to be submitted in Physical Review Applied