Joint PhD thesis from University of Lille and University of Ghent

Development of novel GaN-on-Silicon Vertical power devices

by

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Cotutelle de thèse de doctorat entre l'Université de Lille et l'Université de Ghent

Développement de nouveaux composants de puissance verticaux GaN-sur-Silicium

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Abstract

This thesis explores the development of novel vertical GaN-on-Silicon power devices, aiming to achieve high performance in the 600-1200 V range with reliable operation, including avalanche capability. As modern society's demand for energy grows, there is an urgent need for more efficient power electronics. Traditional silicon-based devices have reached their physical limits, driving the search for alternative materials. Gallium Nitride (GaN) presents a promising solution due to its superior physical properties and cost-effectiveness when grown on silicon substrates.

The research begins with a comprehensive review of the current state of GaN-on-Silicon devices, highlighting the need for vertical configurations over traditional lateral designs. The use of vertical designs is motivated by their ability to enhance reliability, particularly in terms of breakdown behavior at high voltages.

Simulation studies using Silvaco software were conducted to optimize the design of GaN-on-Silicon P-I-N diodes, targeting improved performance in both on-state and off-state conditions. The thesis also delves into the fabrication processes, discussing the optimization of ohmic contacts, mesa formation, edge termination, and buffer layer etching. Techniques such as polyimide passivation and thick copper heatsinks were employed to enhance thermal management and mechanical stability.

Key findings include a significant reduction in leakage current and improved off-state performance through advanced epitaxial growth techniques and innovative buffer designs. The first demonstration of avalanche capability in vertical GaN devices on silicon substrates, achieving high breakdown voltages up to 1200 V, is presented. Additionally, a pseudo-vertical GaN-on-Silicon trench MOSFET was developed, demonstrating promising initial performance metrics.

This work lays the groundwork for further advancements in GaN-on-Silicon technology, highlighting its potential as a cost-effective, high-performance solution for future power electronic applications.

Keywords: GaN-on-Silicon, Power devices, 600-1200 V application, vertical, P-i-N diode, Trench MOSFET, Avalanche, local substrate removal, N face ohmic contact, Bevelled-mesa edger termination.

Résumé

Cette thèse explore le développement de nouveaux dispositifs de puissance verticaux GaN sur silicium, visant à atteindre de hautes performances dans la gamme de 600 à 1200 V avec une fiabilité opérationnelle, incluant la capacité de claquage avalanche. Avec l'augmentation de la demande en énergie de la société moderne, il devient impératif de développer des composants électroniques de puissance plus efficaces. Les dispositifs à base de silicium traditionnels ont atteint leurs limites physiques, ce qui incite à rechercher des matériaux alternatifs. Le nitrure de gallium (GaN) s'avère être une solution prometteuse en raison de ses propriétés physiques supérieures et de son coût de fabrication réduit lorsque sa croissance est réalisée sur substrat en silicium. La recherche commence par une revue complète de l'état de l'art actuel des dispositifs GaN sur silicium, soulignant la nécessité d'architectures verticales par rapport aux conceptions latérales traditionnelles. L'utilisation de composants verticaux est motivée par leur capacité à améliorer la fiabilité, notamment en ce qui concerne le comportement au claquage à haute tension.

Des études de simulation utilisant le logiciel Silvaco ont été menées pour optimiser la conception des diodes P-I-N en GaN sur silicium, afin d'améliorer les performances en régime passant et bloqué. La thèse aborde également les procédés de fabrication, en discutant de l'optimisation des contacts ohmiques, de la formation de mesa, de la terminaison des bords et de la gravure des couches tampons. Des techniques telles que la passivation au polyimide et des dissipateurs thermiques en cuivre épais ont été employées pour améliorer la gestion thermique et la stabilité mécanique.

Les résultats clés incluent une réduction significative du courant de fuite et une amélioration des performances à l'état bloqué de la diode grâce à des techniques de croissance épitaxiale avancées et à des conceptions innovantes de couches tampons. La première démonstration du claquage par avalanche dans des composants verticaux GaN sur substrat de silicium est présentée, atteignant une tenue en tension élevée allant jusqu'à 1200 V. De plus, un transistor de type TMOSFET pseudo-vertical en GaN sur silicium a été développé, démontrant des performances préliminaires prometteuses.

Ce travail fonde les bases de futurs progrès dans la technologie GaN sur silicium verticale, soulignant son potentiel en termes de ratio performance / coût pour les futures applications en électronique de puissance.

Samenvatting

Deze thesis onderzoekt nieuwe, verticale GaN-op-silicium vermogenscomponenten, gericht op betrouwbare prestaties in het bereik van 600-1200 V, inclusief de mogelijkheid tot lawine-doorslag. Door de groeiende energiebehoefte van de moderne samenleving is er nood aan efficiëntere vermogenselektronica. Traditionele siliciumcomponenten hebben hun fysieke grenzen bereikt, waardoor alternatieve materialen nodig zijn. Galliumnitride (GaN) gebaseerde componenten zijn hierbij veelbelovend, vanwege de superieure materiaaleigenschappen van GaN in combinatie met de mogelijkheid om GaN epilagen op een kosteneffiënte manier te groeien bovenop siliciumsubstraten.

De studie begint met een uitgebreid literatuuroverzicht van de huidige stand van GaN-op-silicium componenten. Hierbij wordt het belang van verticale configuraties benadrukt, aangezien deze ontwerpen de betrouwbaarheid verbeteren, vooral bij hoge spanningen. Via simulaties met Silvaco-software werd het ontwerp van GaN-op-silicium P-I-N diodes geoptimaliseerd. Vervolgens werden deze P-I-N diodes gefabriceerd en uitvoerig getest. In de thesis worden kritische fabricageprocessen besproken, zoals de optimalisatie van ohmse contacten en thermisch beheer. Belangrijke bevindingen betreffen onder andere de vermindering van lekkage en verbeterde prestaties in de sper-toestand. Hierbij werd voor de eerste keer lawine-doorslag in een verticale GaN-op-silicium component gedemonstreeerd, met doorbraakspanningen tot 1200 V.

Acknowledgments

Completing this thesis has been a journey marked by perseverance, growth, and collaboration. It would not have been possible without the support, encouragement, and guidance of many wonderful people to whom I am deeply grateful.

First and foremost, I am immensely thankful to Dr. Farid Medjdoub for his unwavering guidance, insightful feedback, and constant encouragement throughout this research. His mentorship has been invaluable, shaping both the direction of this work and my development as a researcher. Beyond the professional support, I am particularly grateful for his personal help, which provided me with strength and confidence during challenging moments. I am also deeply grateful to Professor Christophe Detavernier for his valuable contributions, whose advice and support provided important perspectives that enriched this thesis.

I extend my heartfelt gratitude to my family, who have stood by me through every challenge. Their sacrifices and unwavering belief in me gave me the strength to pursue my dreams, even when the path was difficult and uncertain. Their love and support provided me with the courage and motivation to overcome every hurdle I faced.

To my wife, Salma, who has been my steadfast companion, my gratitude is beyond words. Her patience, understanding, and support have been my anchor during the most challenging moments of this journey. She has been my greatest source of strength, and her presence has been a constant reminder of the importance of love and resilience.

I also want to recognize the incredible support and camaraderie of my colleagues, who quickly became my second family. Their friendship, collaboration, and shared experiences have made this journey deeply rewarding. I am especially grateful to Idriss Abid for his guidance and assistance, and to Professor Katir Ziouche, whose support and advice have been invaluable throughout my research.

Finally, I would like to express my sincere gratitude to the Examination Committee for their time, effort, and constructive feedback throughout this process. Their insightful questions and thoughtful comments have significantly contributed to the improvement of this thesis, and I am honored by their thorough evaluation and support.

I thank everyone who has contributed, directly or indirectly, to the completion of this thesis. Your encouragement, knowledge, and kindness have been invaluable, and I am truly grateful to have had the opportunity to work alongside such remarkable individuals.

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Introduction

The development of modern society has led to an increased demand for energy while raising concerns about consumption and environmental impact. The shift towards electrical solutions, such as electric vehicles, requires significant changes to reduce environmental footprints. At the centre of these discussions, semiconductors have gained attention due to the high-energy consumption of existing circuit and system devices, primarily based on silicon technology. Silicon, however, has reached its physical limits and can no longer meet the growing requirements of power electronics.

To address these limitations, materials like silicon carbide (SiC) have emerged, offering superior physical properties but at a high fabrication cost. However, for power electronics applications, cost-effectiveness is a critical factor. This makes gallium nitride (GaN) a promising candidate. GaN can meet the requirements for power electronics in the 600-1200 V range, providing excellent physical properties while maintaining lower fabrication costs. One way to reduce these costs is by growing GaN on silicon substrates, thus leveraging the advantages of both technologies.

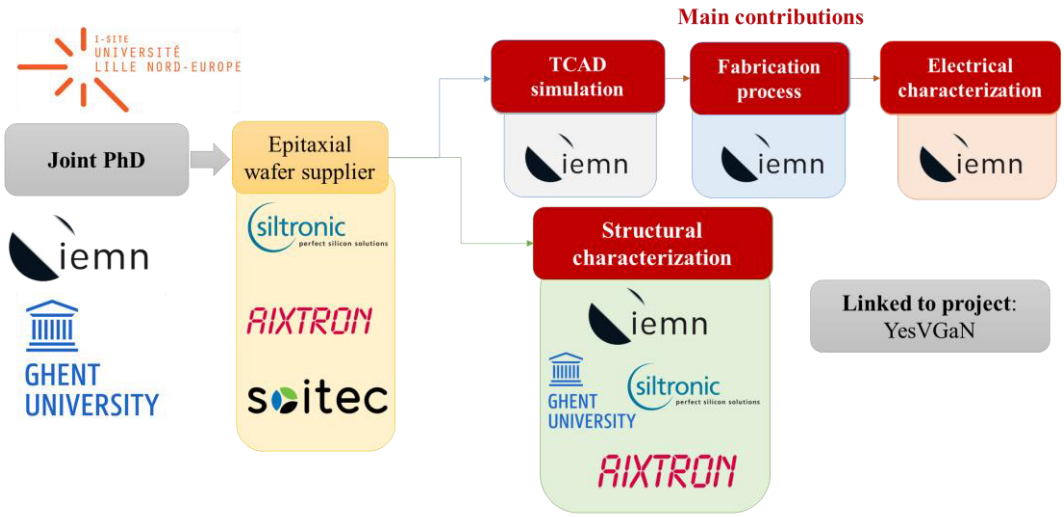
In the last two decades, lateral GaN-on-silicon high-electron-mobility transistors (HEMTs) have been extensively studied. However, these devices still suffer from reliability issues and require larger device sizes as compared to existing power transistors. To fully unlock the potential of GaN-on-silicon, a vertical design can be employed. This already proven architecture for silicon and SiC devices, utilizes junction-based structures to achieve reliable performance.

In power electronics, device reliability is crucial, particularly regarding breakdown behavior at high voltages. Therefore, achieving avalanche capability is essential for many applications, enabling the device to deliver soft breakdown without experiencing damages.

This thesis aims to develop new vertical GaN-on-silicon power devices that demonstrate high performance in the 600-1200 V range while ensuring reliable operation, including avalanche capability. It focuses on the design strategies, fabrication techniques, and performance optimization necessary for advancing power electronics. This PhD is a part of the European project YesVGaN, which gathered more than 23 industrials and research partners coordinated by the company Bosch. The main goal of this project was to develop

new power devices with high performance and low cost of fabrication, directly linked to the PhD objectives.

This thesis is part of a joint PhD between the University of Lille and Ghent funded by the I-Site program. The wafers used in this work were provided by Siltronic and Aixtron. The device simulation, fabrication process and electrical characterization were conducted at IEMN, while the structural and material characterization involved collaboration between IEMN, Ghent University, Siltronic, and Aixtron. My main contributions include the structure design based on TCAD simulation, the development of the fabrication process, the electrical and structural characterization.



The research is organized into several chapters, each addressing key aspects of this development.

Chapter 1 provides an in-depth review of the current state-of-the-art in GaN-on-silicon substrate devices. It emphasizes both the physical properties—such as avalanche capability, on-state, and off-state characteristics—and the material properties, including dislocation filtering and defect reduction. The discussion moves from lateral HEMT to vertical architectures, establishing the critical need for vertical GaN-on-silicon devices. This chapter identifies P-I-N diodes as the primary test vehicle for exploring vertical designs.

Chapter 2 focuses on the use of TCAD simulations with Silvaco software to investigate the interactions within GaN-on-silicon P-I-N diodes. These simulations are crucial for guiding the optimum design of the P-I-N diodes, ensuring high performance in both on-state and off-state conditions. The results demonstrate the necessity of employing a fully vertical design to achieve the required electrical characteristics.

Chapter 3 details the fabrication process optimization for vertical GaN-on-silicon devices. This chapter outlines the key steps, including the development of ohmic contacts, mesa formation, edge termination, local substrate removal, and buffer layer etching. It also addresses the challenges related to backside processing and introduces methods such as polyimide passivation for mechanical reinforcement and improvements to N-face ohmic contacts using HCl treatment, along with the integration of a thick copper heatsink for better thermal management.

Chapter 4 presents the key outcomes of this research, demonstrating significant reductions in leakage current and improvements in off-state performance through innovative epitaxial growth techniques and buffer designs, such as SiN thin layer insertion and island-based configurations. The findings include the first demonstration of avalanche capability in vertical GaN devices on silicon substrates for both pseudo-vertical and fully vertical structures. High breakdown voltages up to 1200 V were achieved, and a detailed comparison between different vertical designs was conducted. This chapter finally highlights the successful fabrication of a fully vertical structure with low on-resistance (Ron) and high current capacity>10 A.

Chapter 5 explores the final contribution of the thesis with the demonstration of a pseudo-vertical GaN-on-silicon trench MOSFET transistor. This chapter presents the

TCAD-based design and initial proof of concept, achieving a 300 V breakdown voltage, a 2 $m\Omega.cm^2$ on-resistance, and a high current density exceeding 2 kA/cm^2. Suggestions for further performance improvements are also discussed.

Chapter 1: GaN on Silicon heterostructure for power electronics

In this chapter, the general history and context of power electronics will be discussed, providing a comprehensive benchmark of power device materials. The physics and advantages of Gallium Nitride (GaN) will then be highlighted. Finally, a state-of-the-art review, including the proposed GaN-on-Silicon technology presented in this work, will be provided.

1.1.1 Framework

1.1.1.1 Overview

In 1902, Peter Cooper Hewitt invented the mercury arc rectifier, which converts alternating current (AC) to direct current (DC). This invention marked the first milestone in the field of electronics dedicated to the conversion and control of electrical power, known as power electronics. As scientific progress continued, the mercury-arc-valve power system was eventually replaced by semiconductor systems, particularly silicon-based devices. Silicon has dominated the power electronics field since its introduction, undergoing continuous development and improvement[1].

Power electronics can be categorized into three main fields[2]:

- Low operating current (<1A)
- Small power circuit (<200V)
- medium voltage (200V-1200V)
- High voltage (>1200 V)

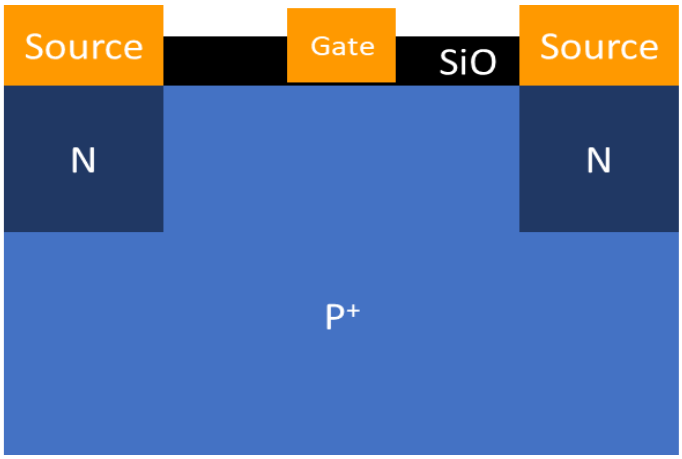


Figure 1-1 : Schematic cross section of a lateral Silicon MOSFET

Thanks to its low on-resistance and high switching frequency, silicon transistors, especially MOSFETs, effectively meet the requirements for low operating current and small power circuit applications. Silicon transistors also offer high potential for development and integration. However, traditional MOSFETs faced limitations in high voltage applications due to their lateral structure, which leads to Trade-off between high on-resistance (Ron) and high breakdown voltage (Figure 1-1)[2]. Consequently, the development of new transistors with high performance for applications exceeding 200V has become essential.

By adding an undoped or lightly doped semiconductor layer, known as the intrinsic layer (I layer), between the p-type and n-type doped layers, a new type of junction called the P-I-N junction has been developed[3]. This innovation paved the way for the invention of new devices. In a standard P-N junction, the maximum electric field is confined to the middle of the junction (Figure 1-2.a). In contrast, the P-I-N junction can gradually spread the high electric field distribution within the intrinsic region (Figure 1-2.b). This means that, for the same bias, the peak electric field within a P-N junction is much larger (restricted to the middle of the junction) compared to the P-I-N junction (within which the electric field is spread in the entire I layer). The intrinsic layer is referred to as the drift region of the junction.

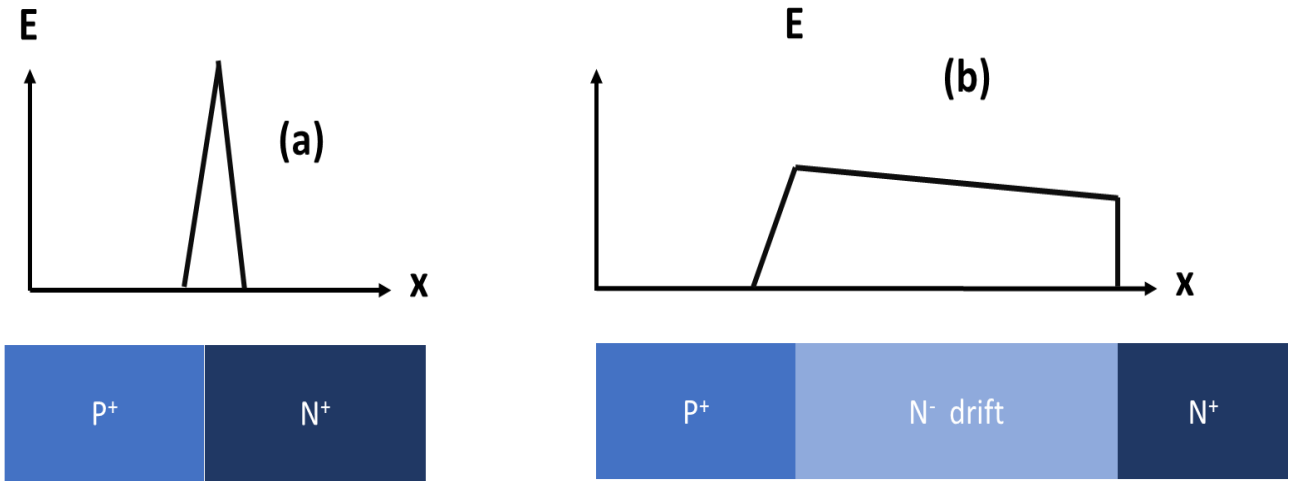


Figure 1-2 : Electric field distribution for the same voltage of (a) PN junction and (b) PIN junction.

1.1.1.2 History of Silicon power devices

The first P-I-N junction-based transistor, introduced by Hitachi in 1969, was called V-groove MOSFET (Figure 1-3.a)[4]. Despite the good performance of these devices, they were eventually replaced due to electron trapping issues within the oxide layer and difficulties in fabrication. The replacements were VDMOSFET (planar power MOSFET transistors) and UMOSFET (trench MOSFET transistors)[5]. The VDMOSFET, or Vertical Diffused MOSFET (Figure 1-3.b), is considered the most commonly used power electronic transistor within the 200-600V voltage range, and it is based on the N-(P-I-N) junction.

It is well known that lateral MOSFETs have low on-resistance (Ron) for low-voltage applications. However, at higher voltage, Ron increases drastically due to the thickness of the drift region. For example, in applications requiring 600V, the drift region thickness exceeds 40 µm [6]. The operating frequency of VDMOSFETs is in the range of 100 kHz. Nevertheless, VDMOSFET transistors suffer from high Ron due to the JFET channel[7]. Since the two inversion channels are not isolated, an electron-trapping path is created, increasing the resistance. To mitigate these parasitic effects, the trench MOSFET (U-MOSFET) (Figure 1-4.a) and the super junction MOSFET (SJ-MOSFET) (Figure 1-4.b) were developed [8].

The JFET channel of the VDMOSFET is a major issue. This channel is generated below the gate, leading to the idea of suppressing this area by etching. The etching process allows the gate to have a trench form (U shape) by creating a trench in the structure (U-MOSFET) (Figure 1-4.a)[5]. The electron path starts from the source, crosses the inversion layer, and finishes with accumulation at the edge of the trench through the drift region. With this technology, the Ron of the MOSFET is drastically reduced, while maintaining device performance. However, the trench gate form introduces a weakness due to the peak electric field within the oxide, which decreases the device lifetime. Various solutions have been proposed to address this issue, such as increasing the oxide thickness and rounding the angles [9].

The super junction MOSFET (Figure 1-4.b) features two P-doped walls that create a compensation region, reducing the on-state resistance and internal charges. The SJ-MOSFET is significant in radiofrequency applications (switching frequency >100 MHz) due to its low Ron. Furthermore, the P-wall enhances avalanche breakdown by

influencing the impact ionization current. The SJ-MOSFET demonstrates performance that surpasses the limitations of silicon.

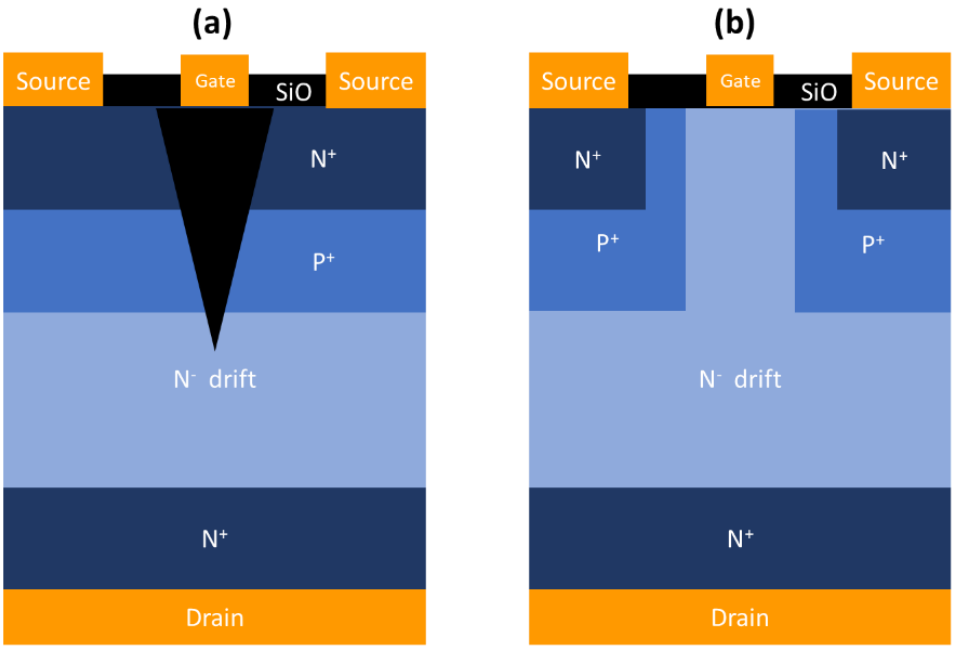


Figure 1-3 : (a) Silicon VMOSFET (b) Silicon VDMOSFET

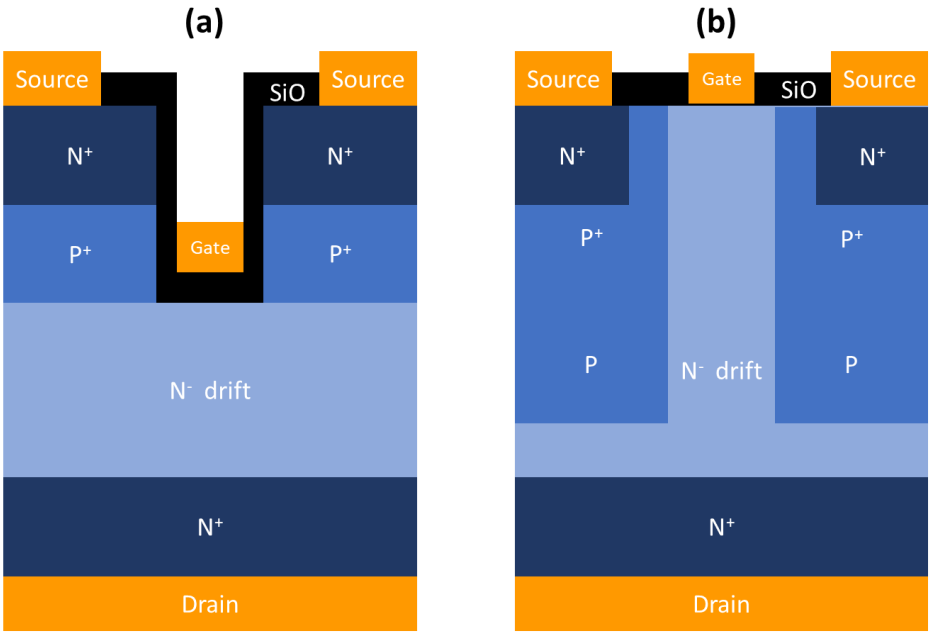


Figure 1-4 : (a) Silicon UMOSFET (b) Silicon SJ-MOSFET

1.1.1.3 Benchmark of power device semiconductors

Semiconductor materials can be characterized by several parameters, including critical electric field, band gap, mobility, and saturation speed, among others. Silicon power devices have dominated power applications for the past several decades. However, due to inherent physical limitations, their dominance is beginning to wane. These limitations have slowed down the development of silicon-based power devices. To overcome this bottleneck, wide bandgap semiconductors have been proposed to further push the limits of power electronic applications.

Material	**Si**	**SiC**	**GaN**
band gap Eg (eV)	1.1	3.2	3.4
Dielectric constant (ε)	11.9	9.7	9.5
Critical electric field (MV/cm^2)	0.3	3	2.8-3.4
Electron Mobility($cm^2/V.s$)	1400	950	900/2000
Thermal conductivity σth(W/cm.k)	1.5	4.5	1.5
Electron saturation speed Vsat ($10^7 cm/s$)	1	2	2.5
Fabrication cost	--	++	-(with Si substrate) +++(with GaN substrate)

Table 1 : Benchmark of power electronic material physical properties

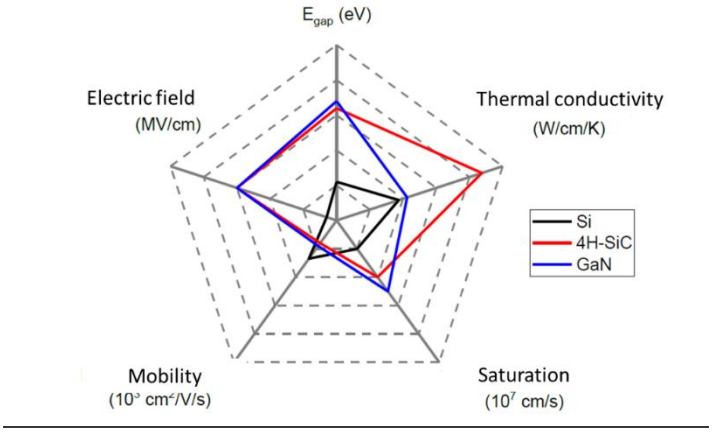


Figure 1-5 : Comparison of Si vs GaN vs SIC

GaN (Gallium Nitride) is a strong candidate to replace silicon in power electronics due to its superior properties. It has a much higher critical electric field (E_C (GaN) = 38 × E_C (Si)), avalanche capability, large bandgap, and high electron velocity. Additionally, GaN offers a flexible choice of substrates depending on the targeted cost of fabrication, including silicon (Si), GaN, and sapphire. In contrast, Silicon Carbide (SiC) is much less available and a more expensive substrate.

1.1.2 Current market growth and applications

Power electronics market has been growing steadily since the electronic revolution in the latter half of the 20th century [10], [11], [12]. Now, more than ever, the demand for power electronics applications has reached unprecedented levels. This surge is driven by the global shift towards renewable energy, which necessitates efficient control and conversion of electrical energy using devices that minimize losses.

To understand device losses, consider a typical power electronic conversion circuit (Figure 1-6). In these circuits, devices function as power switches that alternate between two operation modes: discharge and storage, following the control signal (on and off states). In an ideal scenario, the current follows the control signal instantaneously. However, in reality, a delay occurs, resulting in the simultaneous presence of current and voltage in the same area, which adds to the power loss. Additionally, self-heating losses are generated, depending on the material properties (Figure 1-7). These losses are critical factors in the design and efficiency of power electronic devices and understanding them is essential for developing more efficient and reliable systems.

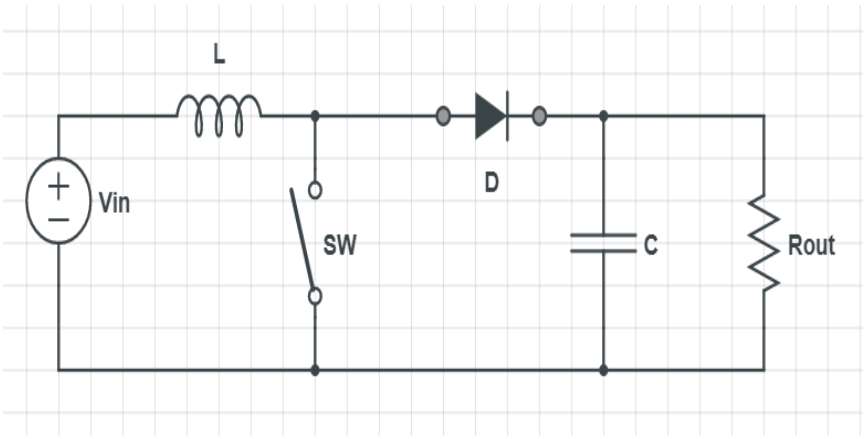
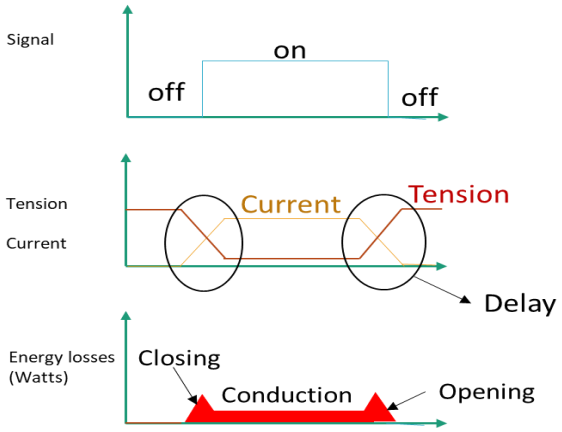


Figure 1-6 : Example of boost conversion circuit



Losses due to the switching of the transistors: P=V*I

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_L + P_T + P_D + P_f + P_r}$$

Figure 1-7 : command signal, current and voltage response, and losses generated while switching the transistor (Pf+Pr)

Given these factors, the power electronics market is projected to grow to $33 billion by 2028. This predication was made by Yole group, an international company, recognized for its expertise in the analysis of markets and technological developments. As shown in Figure 1-8, silicon remains the most widely used material in power electronics. However, this trend may shift over time as new materials gain prominence in the market. Over the past year, the top three power electronics companies have experienced revenue boosts thanks to silicon carbide (SiC), which is extensively used in electric vehicles and photovoltaic power systems. SiC is primarily utilized in the 600-1200V range, attempting to fill the gap left by silicon in this range; however, this technology remains expensive.

This is where Gallium Nitride (GaN) comes into play. GaN theoretically overcomes the main drawbacks of both SiC and silicon materials. Figure 1-9 illustrates the growth of the Gallium Nitride market share, projected to reach a revenue of $2 billion by 2028. Emerging technologies have the potential to further increase GaN's market revenue.

In this thesis, we demonstrate a new fully vertical GaN technology that shows significant promise as a potential solution for future power electronic applications.

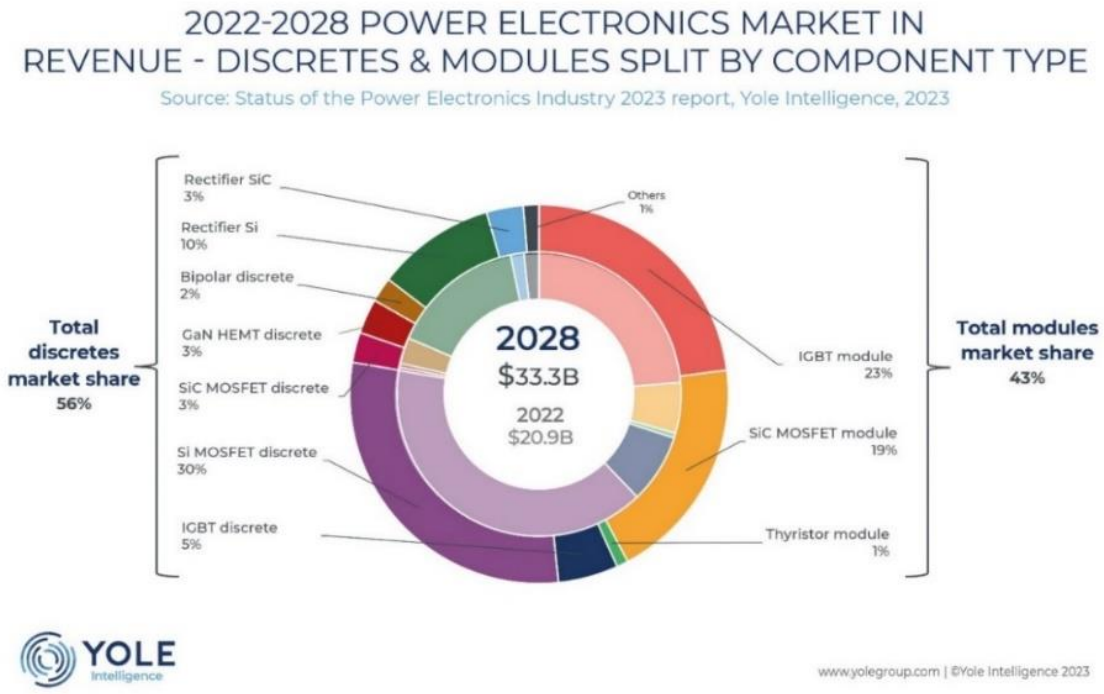


Figure 1-8 : Power electronics market share growth from 2022 to 2028 from the website of Yole group 2023 "https://www.yolegroup.com/"

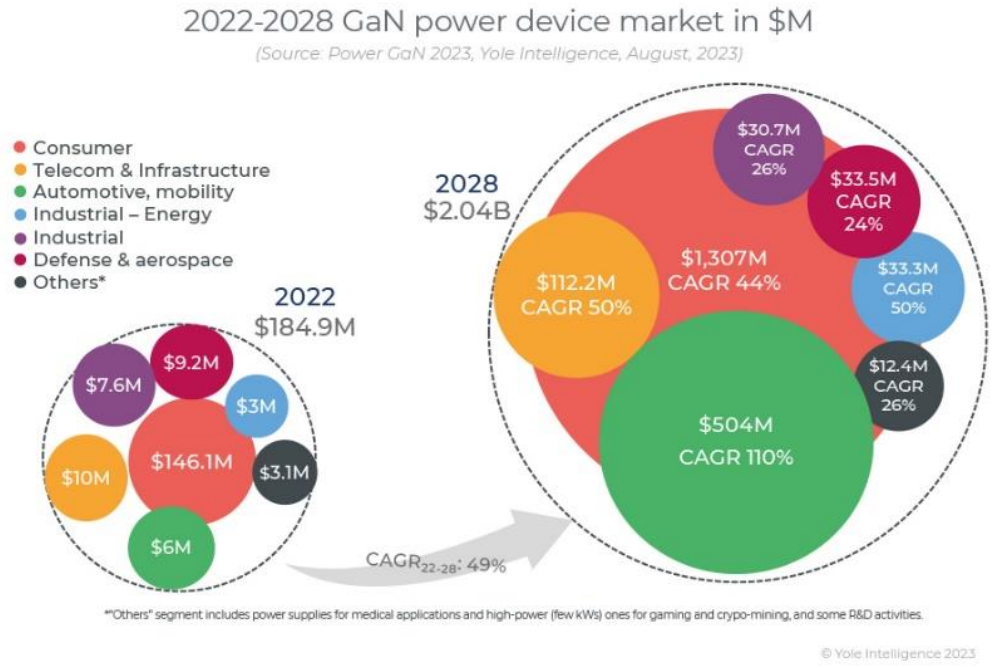


Figure 1-9 : GaN market growth from 2022 to 2028 from the website of Yole group 2023 "https://www.yolegroup.com/"

1.2 GaN based power devices

1.2.1 Physical properties

1.2.1.1 GaN Crystal

The group III atoms of the periodic table can bond with nitrogen (N) in the solid state to form nitride semiconductors such as AlN, InN, and GaN. These chemical elements can crystallize in different forms depending on the growth conditions and polarity. Under thermally stable conditions, GaN typically forms a hexagonal crystal structure known as wurtzite (Figure 1-10.a). In this structure, each gallium atom bonds with four nitrogen atoms, creating an arrangement where the spacing between atoms is denoted by the parameters a and c.

The wurtzite form is the most common crystal structure for GaN, especially for High Electron Mobility Transistors (HEMTs), which will be discussed later. This crystal structure lacks symmetry around the (0001) axis, resulting in two different growth polarities:

- Ga-polarity (0001) (Figure 1-10.b): Growth starts with nitrogen atoms and ends with gallium atoms.
- N-polarity (000-1) (Figure 1-10.b): Growth starts with gallium atoms and ends with nitrogen atoms.

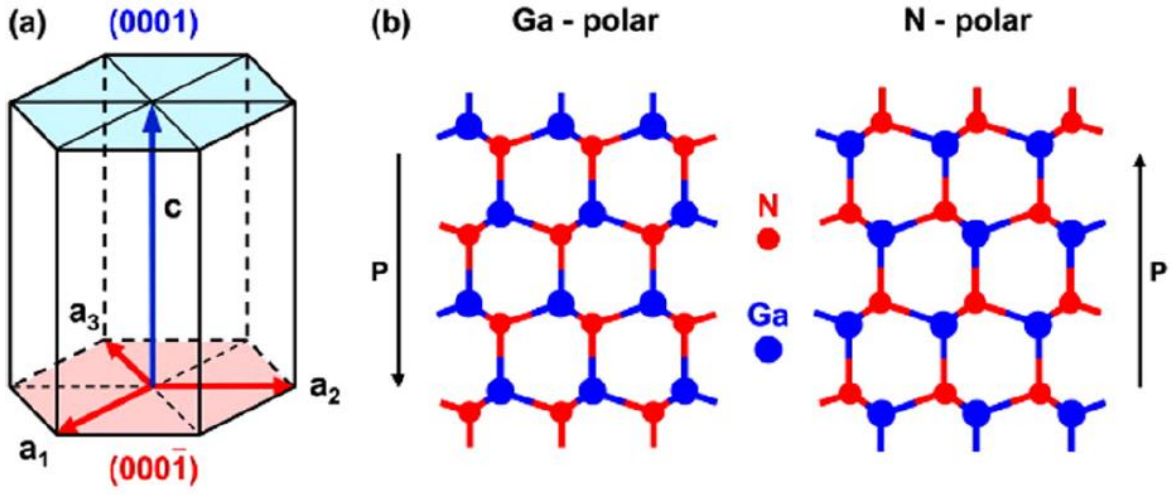


Figure 1-10 : Wurtzite crystal with two different polarity (a) Ga-face and (b) N-face [13]

The difference in polarity affects the surface properties of the crystal. Most GaN devices exhibit Ga-polarity, where the top surface is referred to as the Ga-face, and the bottom surface as the N-face. It is important to note that the N-face (bottom surface) has N-polarity. The N-polarity surface has higher chemical activity and lower mobility compared to the Ga-face, which explains the preference for using the Ga-face for power electronics applications.

1.2.1.2 Polarization effect properties of GaN

The nature of the GaN wurtzite crystal is not perfectly regular, with a slightly asymmetrical phase. Ideally, the ratio between the lattice constants c and a is 1.633, but in the case of GaN, this ratio is 1.637 due to environmental factors. This configuration results in a nonzero sum of dipole moments within a single tetrahedron, leading to spontaneous polarization (P_{sp}), which induces an internal electric field oriented from the Ga to the N direction due to the difference in electronegativity of the atoms. Figure 1-10.a illustrates the conventional direction of P_{sp} on the [0001] face. Additionally, with this configuration, III-nitride materials exhibit a piezoelectric (P_{pe}) effect due to crystal deformation[14], [15].

The properties of III-nitride materials, particularly GaN, facilitate the development of heterostructure technologies. The most notable example is the AlGaN/GaN technology. By growing AlGaN on an a GaN layer, the crystal stress increases due to the lattice mismatch, as a(GaN) > a(AlGaN), resulting in tensile strain. In this case, P_{pe} and P_{sp} are parallel and oriented in the same direction toward the GaN substrate. The total polarization P in the same layer is the sum of P_{pe} and P_{sp} : $P= P_{pe} + P_{sp}$. Therefore, the total polarization P is also oriented toward the GaN substrate (from the Ga-face to the N-face). A polarization charge density δ is induced with each gradient of PP:

$$\boldsymbol{\delta = \nabla P} \qquad \textbf{Equation 1}$$

By taking into account the variation of polarization inside the AlGaN/GaN heterostructure, the equation becomes

$$\boldsymbol{\delta(Psp + Ppe) = |P(GaN) - P(AlGaN)| = |Psp(GaN) - (Psp(AlGaN) + Ppe(AlGaN)|} \qquad \textbf{Equation 2}$$

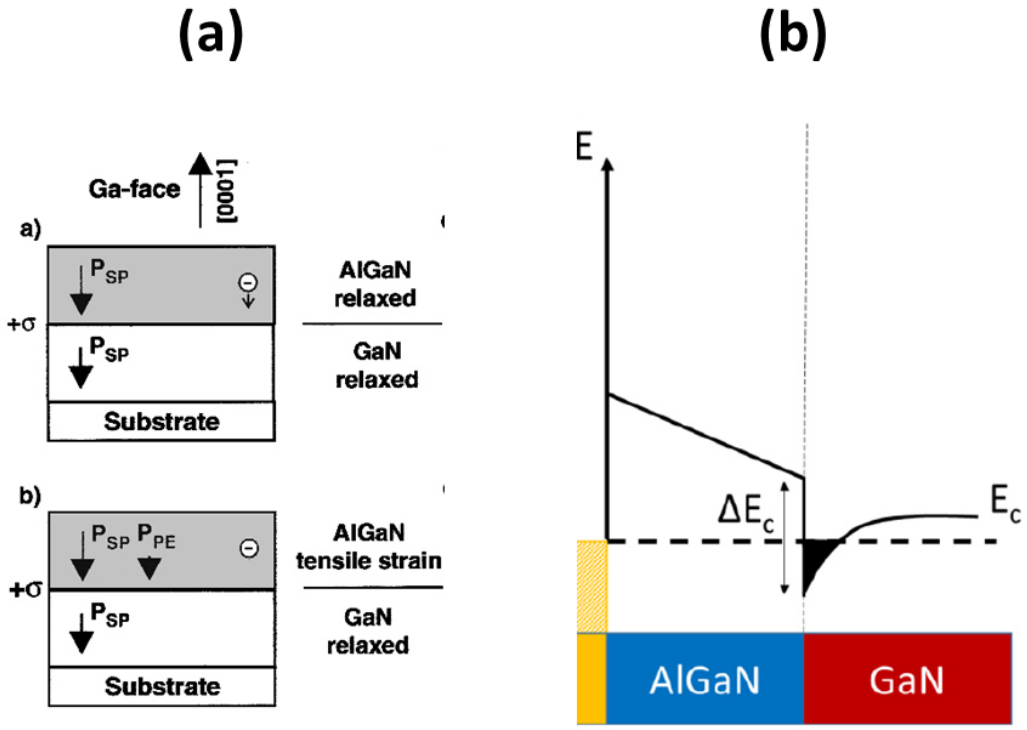


Figure 1-11 : (a) Polarization effect of AlGaN/GaN heterostructure (b) Schematic band diagram of AlGaN/GaN heterostructure[14], [15].

The difference in energy gaps between AlGaN and GaN creates a discontinuity in the band diagram (Figure 1-11.b). Additionally, the induced polarization sheet charge is positive (+δ) (Figure 1-11.a). In this scenario, the presence of free electrons that neutralize this positive charge is highly probable, leading to the formation of a two-dimensional electron gas (2DEG) where the triangular quantum well drops below the Fermi level (Figure 1-11.b). The 2DEG is a crucial feature of this technology, enabling the development of high electron mobility transistors (HEMTs)[16], [17], [18], [19], [20].

1.2.1.3 Junction based structures

Like any semiconductor, GaN can be doped with N-type and P-type dopants to create epitaxial junction-based devices. The most common dopants for GaN are Silicon (Si) for N-type and Magnesium (Mg) for P-type doping. Similar to silicon, power junction-based structures in GaN devices include a drift region to sustain high electric fields and support high breakdown voltages. A key property of these structures is impact ionization.

Under high electric field, electrons (or holes) gain sufficient energy to ionize other atoms, leading to the generation and multiplication of additional charge carriers, which results in a rapid increase in current (Figure 1-12). Impact ionization is characterized by the ionization coefficients α_n for electrons and α_p for holes. The ionization impact coefficient is defined as the number of charge carriers generated by a single electron (or hole) while crossing 1 cm of the depletion layer in the direction of the electric field. The ionization coefficients can be described using Chynoweth's law[2]:

$$\boldsymbol{\alpha = ae^{-\frac{b}{E}}} \qquad \textit{Equation 3}$$

In this context, E represents the applied electric field, while a and b are constants that depend on the intrinsic properties of the semiconductor. Before the generation of significant leakage current, a soft breakdown occurs due to impact ionization, which helps limiting damages to the devices. This phenomenon is known as avalanche capability or avalanche breakdown. The avalanche breakdown point is reached when the impact ionization rate becomes infinite.

The total number of generated electron-hole pairs at a distance x can be defined by[2]:

$$\boldsymbol{M(x) = \frac{e^{\int_0^x (\alpha_n - \alpha_p) dx}}{1 - \int_0^W \alpha_p [e^{\int_0^x (\alpha_n - \alpha_p) dx}] dx}} \qquad \textit{Equation 4}$$

Using the last definition, the avalanche breakdown occurs when the multiplication factor M tends towards infinity (i.e., when the denominator becomes zero). By assuming that α_p and α_n are equal, the avalanche breakdown condition can be defined as follows:

$$\boldsymbol{\int_0^W \alpha dx = 1} \qquad \textit{Equation 5}$$

This equation is used to determine the breakdown voltage of different devices. In addition, the avalanche breakdown voltage increases with increasing temperature. More specifically, phonon scattering causes a delay in the onset of impact ionization, requiring a higher reverse bias at elevated temperatures to achieve the same energy levels. Essentially, as temperature rises, the soft breakdown point for devices with avalanche capability increases according to the following relationship:

$$\boldsymbol{BV(T) = BV_{294K}(1 + \alpha \Delta T)} \qquad \textit{Equation 6}$$

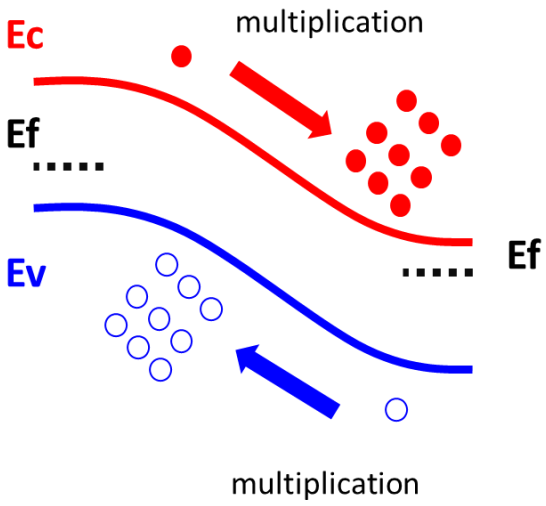


Figure 1-12 : Generation of charge carriers by ionization impact multiplication of electrons or holes

Although GaN benefits from avalanche capability [21], the quality of the growth and fabrication process plays an important role in enabling this benefit. As discussed earlier, PiN structures can withstand high electric fields while showing high current spreading due to the use of a drift region thickness as a depletion region. During the on-state, the injection of a large concentration of minority carriers reduces the resistance of the drift region. This design is known as the punch-through architecture (Figure 1-13.a).

The forward conduction mechanism of this design can be divided into four regimes (Figure 1-13.b)[2]:

- Space Charge Regime: At low current levels and low voltage, the current is proportional to (qVon/2kT). In this regime, the current flow is controlled by the space charge within the depletion region.
- Low-Level Injection Regime: When the minority carrier injection within the drift region controls the current flow and the concentration of minority carriers is lower than the doping concentration, the current becomes proportional to (qVon/kT).
- High-Level Injection Regime: At higher bias levels, the injected carrier concentration exceeds the doping concentration of the drift region, leading to an increase in current density. This is known as the high-level injection condition, where the current is proportional to (qVon/$2kT$).
- Ohmic Regime: At high bias, the current density increases sufficiently so that recombination rates dominate the injected carrier density within the drift region.

The current increases drastically and depends linearly on the applied voltage Von. In this regime, the resistance $R=\delta V/\delta$J can be extracted and calculated.

In the off-state, the electric field of the punch-through design has a trapezoidal distribution (Figure 1-13.a). This means that the electric field varies gradually along the drift region. Due to the different doping concentrations, a rapid drop of the electric field occurs at the N-/N+ interface. The breakdown voltage supported by the punch-through architecture can be expressed as follows[2]:

$$\boldsymbol{BV = EcWp - \frac{qN_dWp^2}{2\varepsilon_r}} \qquad \textit{Equation 7}$$

where :

- N_d is the doping concentration of the drift region.
- Ec is the electric field at the junction.
- Wp is the depletion region thickness (drift region thickness).
- ε_r is relative permittivity which is equal to $\varepsilon_0\varepsilon_{GaN}$.
- q is the elementary charge.

With this equation, we can determine the breakdown voltage knowing the electric field at the junction and vice versa.

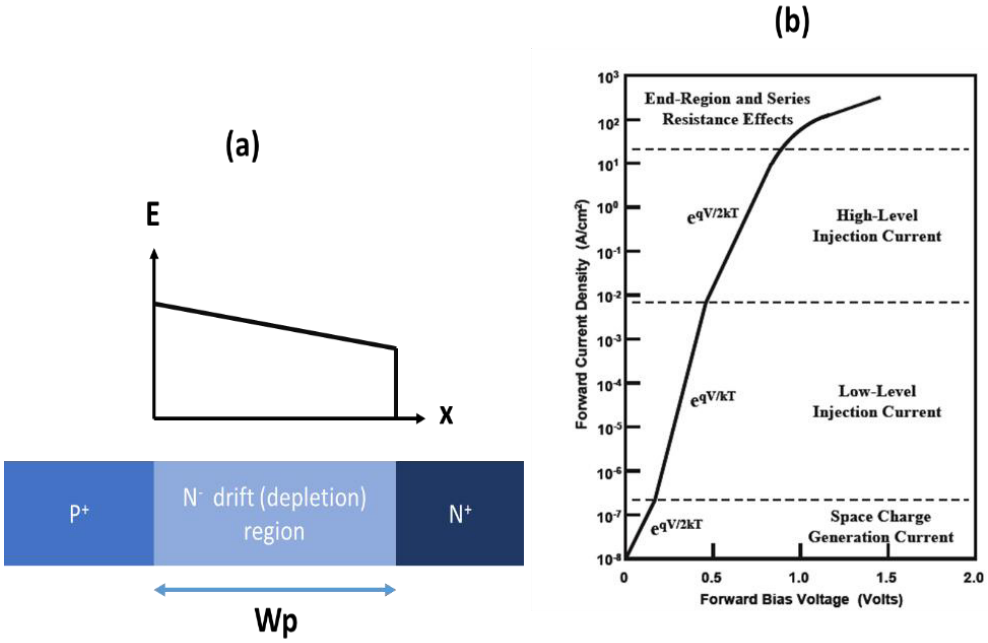


Figure 1-13 : (a) Punch through architecture showing the distribution of the electric field (b) forward current mechanism of the Punch through architecture

$$Vpt = \frac{qNd(2d)^3}{2\varepsilon} \qquad \textit{Equation 8}$$

$$J = \frac{qW_p ni}{\tau_{sc}} \qquad \textit{Equation 9}$$

To deplete the drift region, the required Vpt can be calculated using Equation 8. If the applied voltage Voff > Vpt, the depletion region size becomes independent of the voltage. Additionally, the leakage current of these structures in the ideal case can be calculated using Equation 9, where n_i is the intrinsic carrier concentration of the GaN, and τ_{sc} is the space charge lifetime. However, this equation describes the ideal case where the growth and process are perfect and do not induce any additional mechanisms of leakage current. Figure 1-14 shows the different leakage current mechanisms, such as variable range hopping (VRH) and trap-assisted space charge limited current (SCLC).

The leakage current in a PIN diode is influenced by several mechanisms, including Variable Range Hopping (VRH) and Trap-Assisted Space Charge Limited Current (TASCLC), each becoming predominant under different conditions dictated by the diode's design and the voltage applied.

VRH describes a charge transport process in disordered semiconductors, where carriers traverse by hopping between localized states with variable probabilities. This transport is affected by the energy barriers between these states, their spatial distances, and is sensitive to changes in temperature and electric field. In diodes featuring a punch-through configuration, VRH can play a major role in leakage current, particularly under low-temperature conditions. Conversely, TASCLC occurs when charge carriers moving through the semiconductor encounter traps—localized defect states or impurities that can capture them. In punch-through diodes subjected to higher voltages, these traps may become filled with the injected carriers, leading to a space-charge limited condition. Under such circumstances, the current increases more sharply as it becomes less dependent on voltage in a linear fashion. This phenomenon results in elevated leakage currents as the thermally excited carriers are released from the traps, thereby enhancing conduction through the diode[22], [23].

Another junction-based structure configuration that withstands low voltage compared to the punch-through architecture, but can be used in specific applications, is the Schottky rectifier. In this design, a Schottky contact is added at the top of the drift region. During

the on-state current, majority carrier transport dominates (with no significant minority carrier transport). With this configuration, the Schottky diode demonstrates a high switching capability at high frequencies.

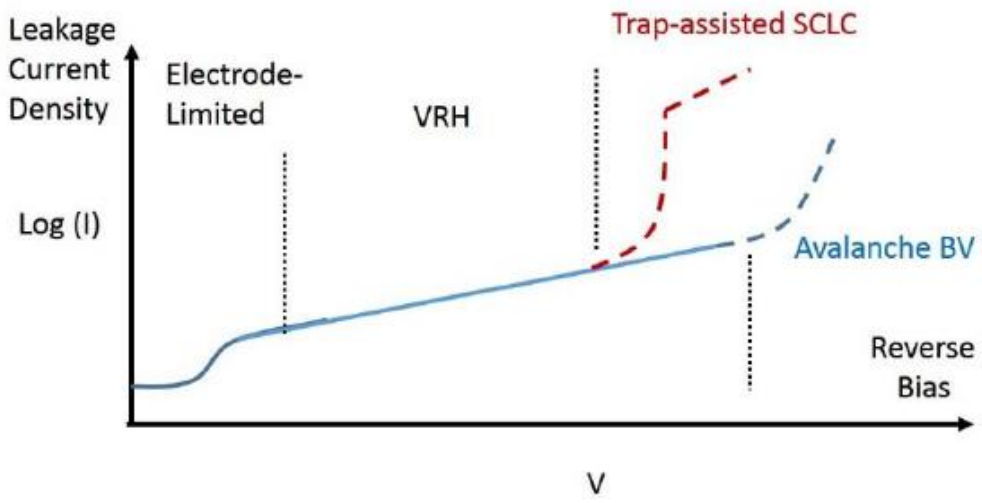


Figure 1-14 : Various leakage current mechanism of diode [22], [23]

Moreover, the electric field distribution decreases gradually within the off-state into the drift region. However, the major issue with the Schottky barrier is the peak electric field at the surface, which leads to a lower breakdown voltage compared to the punch-through design (Figure 1-15).

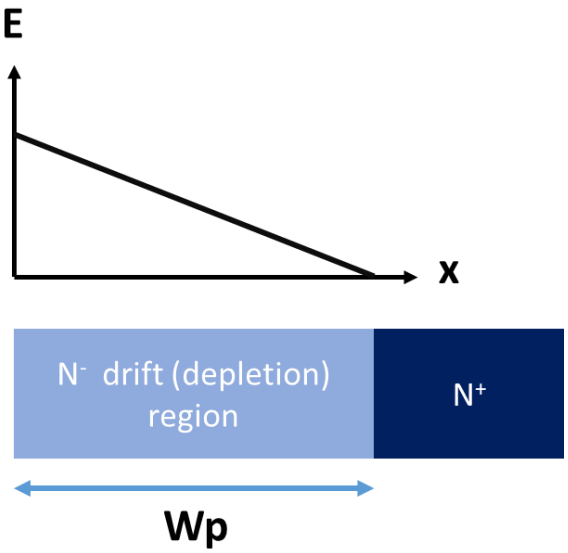


Figure 1-15 : Schottky rectifier structure showing the distribution of the electric field

1.2.2 Growth substrate

The cost of fabrication is a decisive element in the industrialization of power materials, with budgets primarily determined by application needs. For radiofrequency applications, the cost is less critical than for high-voltage applications. In the 600-1200 V range, end users and customers require a reduced fabrication cost. For this reason, silicon technology was long unbeatable in this field. However, due to high losses of Si-based technology, the more expensive SiC technology [24] finally penetrated the market as industrial players and related research community keep pushing for new WBG (Wide bandgap materials) technologies.

GaN technology is very promising due to its large and flexible choice of substrates. GaN heterostructures and junction-based structures can be grown on GaN native substrates, which have an ideal lattice match, leading to low dislocation density [25], [26], [27], [28], [29], [30]. The main drawback of this substrate is the high cost of fabrication and the current limited size to 4 inches[31].

The second alternative is the SiC substrate, which offers state-of-the-art results in RF millimeter-wave applications owing to its excellent thermal conductivity [32], [33]. However, the cost of this technology is rather high for power electronics and can be easily replaced by SiC-based MOSFETs that already demonstrated suitable performance[24]. Another drawback of using SiC substrate is the difficulty to access the bottom layer of the epitaxy, which is needed for many device architectures.

GaN on sapphire substrates has dominated the optoelectronics field with good performance and affordable costs. Recently, GaN on sapphire has started to attract more attention for high-voltage applications (1200 V +)[34], [35], [36]. However, the poor thermal conductivity coefficient may generate severe power / size / reliability limitations. The compressive strain between GaN and sapphire induces defects and high dislocation density. Additionally, there is also no easy access to the bottom layer of the epitaxy unless a debonding and substrate transfer technology is developed[37].

As discussed before, the cost of silicon fabrication is unbeatable. This is why it is attractive to develop cost-effective GaN-on-silicon substrate devices. GaN-on-Si HEMTs have been used for the last two decades for high-voltage applications[38], [39], [40], [41]. Progress in this area has allowed a significant reduction in dislocation density, enabling high

growth quality. In the last five years, there have been an increasing industrial interest to use GaN-on-Si technology for RF applications, proving the attractiveness of the silicon substrate. One major advantage of the silicon substrate is the possibility of accessing the bottom layer of the epitaxy using a well mastered local substrate removal (which will be discussed later)[42]. Access to the bottom layer can be very useful for removing the buffer layer (where dislocation concentration is likely the highest), preventing premature breakdown induced by the low breakdown field of the substrate, and improving electric field management by using a heat sink on the backside extremely close to the junction.

	Sapphire	**Si**	**SiC**	**GaN (Bulk)**
Size	2”-6”	2”-12”	2”-4”	2”-4”
Cost	+	-	++	+++
Resistivity ρ (Ω.cm)	> 10^{11}	> 10^{4}	> 10^{4}	> 10^{4}
Lattice constant a_0 (Å)	2.747	3.840	3.080	3.189
Thermal conductivity (W/cm.K)	0.5	1.5	5	1.5
Heat expansion coefficient (× 10^{-6} K^{-1})	7.5	2.59	4.7	5.59
Difference in the lattice constant from GaN (%)	16.1 Compressive strain	-16.9 Tensile strain	3.5 Compressive strain	0
Difference in the heat expansion coefficient from GaN (%)	-25.5	115.8	18.9	0
Main application areas	Opto-electronics power electronics	High-Frequency and power electronics	High-Frequency electronics, opto-electronics	High-Frequency and power electronics, opto-electronics

Table 2: Comparison of growth substrate for GaN

From the above (table 2), the silicon substrate is currently considered the best solution based on performance / cost ratio for growing GaN hetero- and junction-based structures.

To grow GaN-based structures on a silicon substrate, transition layers must be added. Typically, the growth starts with a thin AlN nucleation layer (Figure 1-16.a), which significantly reduces dislocation density and enhances the quality of the GaN layers. Therefore, the quality of the AlN layer should be optimized to minimize any adverse effects on the performance of the active area.

To ensure a smooth transition between the silicon substrate and the GaN layer, buffer layers are added. Depending on the application, various buffer configurations have been developed. One common approach is the step-graded buffer (Figure 1-16.b). In this approach, multiple thin AlGaN layers are deposited with a gradual decrease in Al content. Within each layer, partial relaxation of the lattice mismatch is allowed between the GaN active layers and the silicon substrate. This reduces strain and dislocation density. The step-graded buffer offers good electron confinement and can withstand high voltages[43], [44], limiting substrate trapping and premature breakdown issues due to the difference between the critical electric field of silicon and GaN. However, the major drawback of the step-graded buffer is the rather high dislocation density and the difficulty to control their propagation through the active layers.

The second buffer layer approach is the so-called superlattice buffer (Figure 1-17). In this case, very thin pairs of AlN and GaN layers are alternated throughout the buffer thickness[42], [45], [46]. With this configuration, the build-in strain decreases gradually in the direction of the active layer, as each alternation of AlN and GaN allows significant relaxation of lattice mismatch. The superlattice buffer provides better control of dislocation density, as dislocations are bent by the periodic variations in lattice mismatch. The electron and breakdown capabilities of the superlattice buffer outperform the drawbacks of the step-graded buffer [47]. The control of the periodic thicknesses of the AlN/GaN layers is crucial for the quality of the grown epitaxy.

An enhanced version of the superlattice buffer has been developed to further reduce dislocation density using AlN/$Al_xGa_{1-x}N$ as the periodic layers and implementing island growth (Figure 1-18)[48]. This technique annihilates dislocations through bending effects, reducing the probability of dislocation density spreading and defect issues. The growth of this specific superlattice-based buffer layers starts with islands using precise geometrical parameters that are crucial for bending and minimizing dislocations.

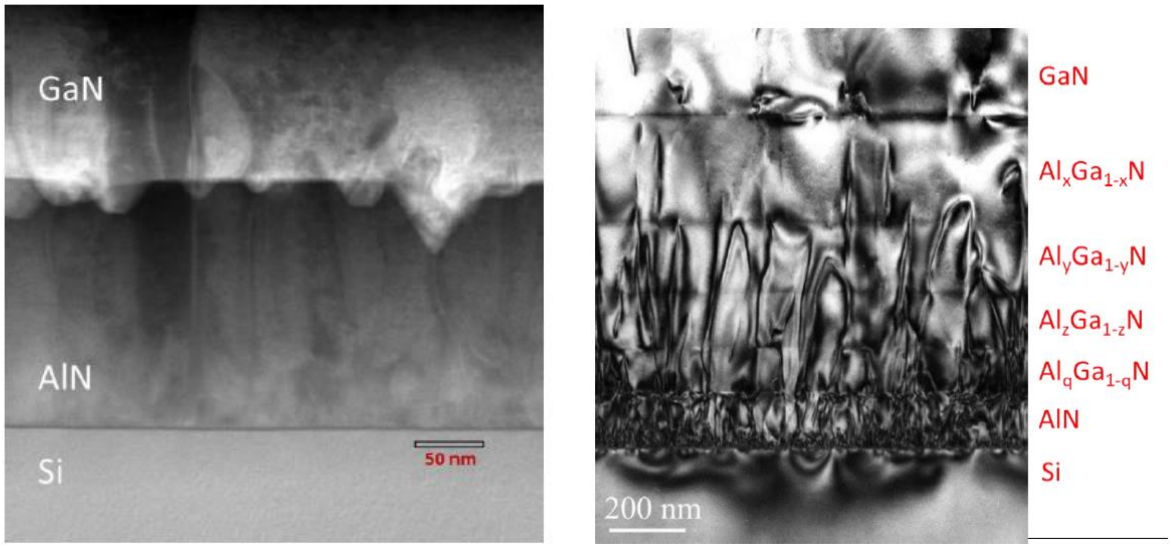


Figure 1-16 : (a) SEM image of a growth of GaN and AlN nucleation layer on Si substrate (b) step graded buffer [47]

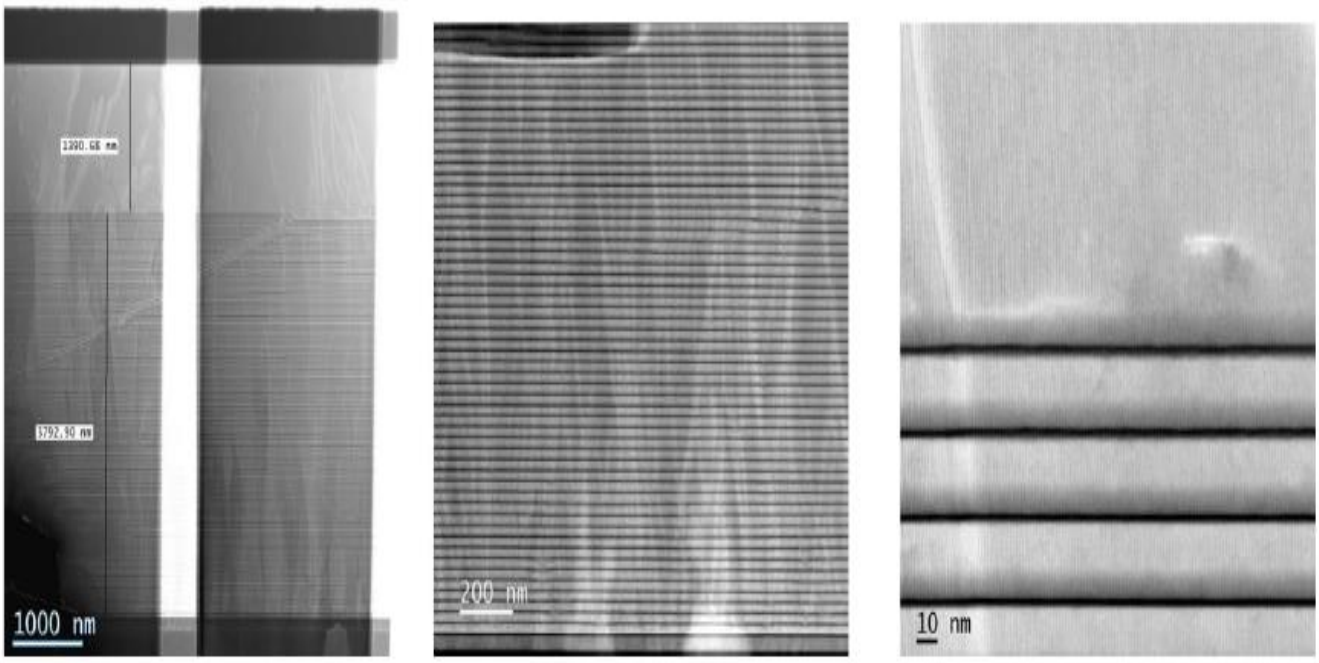


Figure 1-17 : SEM image of a superlattice buffer with different zoom where we can see AlN/GaN periodic layer[47]

Other recent buffer configurations between involve using a superlattice buffer with a thin SiN layer insertion (Figure 1-19). This approach strongly reduces the dislocation density from 10^8 cm^{-2} to the mid-low 10^7 cm^{-2}, improving the device performance and reducing the leakage current[49].

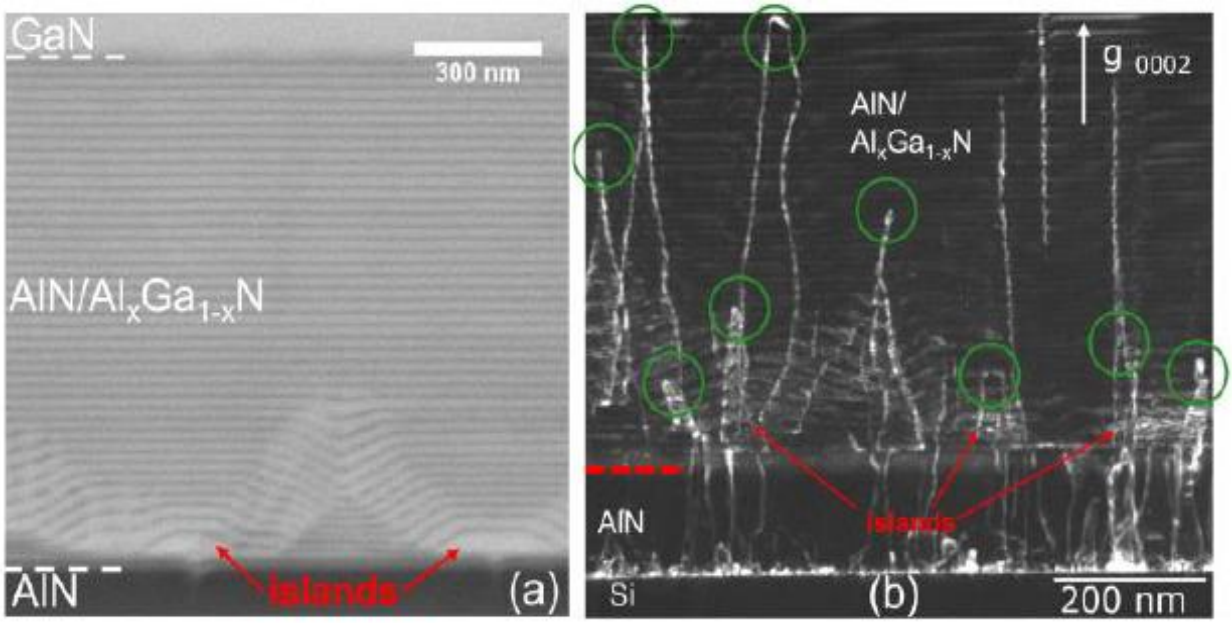


Figure 1-18 : (a)SEM image of the enhanced superlattice buffer using islands growth (b)TEM image of the enhanced superlattice buffer with island growth (red circle) and annihilated dislocation (green circle)[48]

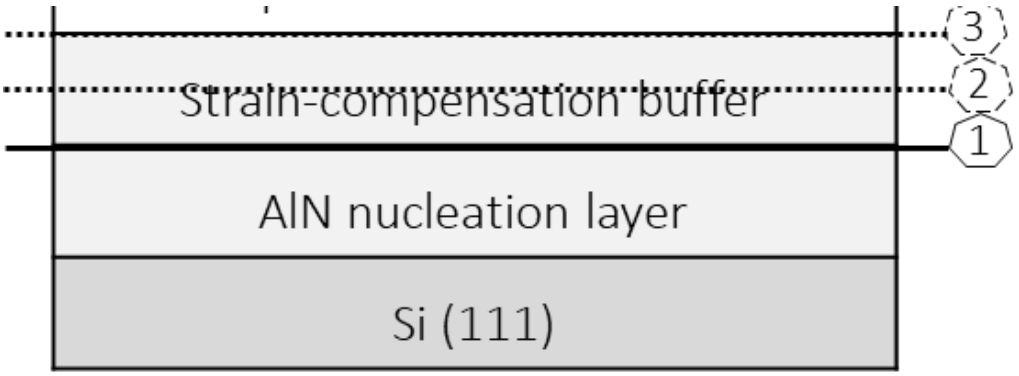


Figure 1-19 : Schematic of SiN layer insertion within the buffer [49]

The choice of the buffer is a critical element that depends on the application and the epitaxy used, which will be discussed later.

1.2.3 Lateral structure

During the last two decades, significant efforts have been made to fabricate reliable GaN devices for 600-1200 V application range[13], [44], [46]. The most common device is the High Electron Mobility Transistor (HEMT), which has a lateral structure based on the AlGaN/GaN heterostructure and utilizes a two-dimensional electron gas (2DEG) for its

functionality (Figure 1-20). As mentioned before, crystal stress induces a polarization effect in the GaN and AlGaN layers. Due to the bandgap discontinuity between AlGaN and GaN, a 2DEG is created at the interface. This means that, in its natural state, the HEMT transistor conducts current without any applied voltage on the gate, making it a normally-on transistor.

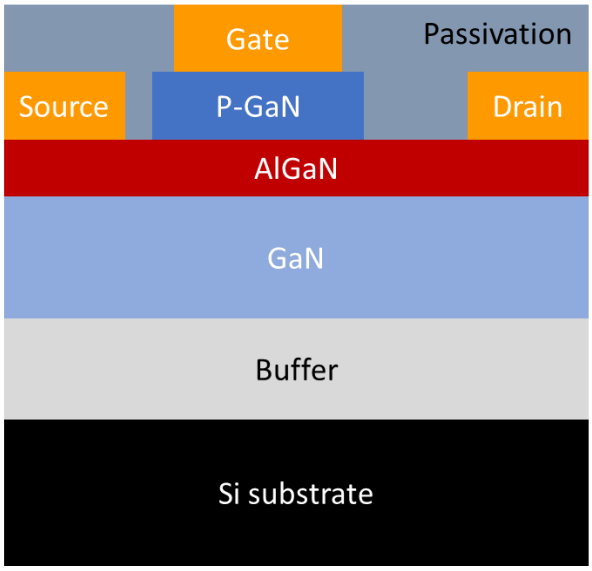


Figure 1-20 : Schematic cross section of a standard High electron mobility transistor [47]

To achieve full control of the transistor, the device design should enable normally-off capability. Several solutions have been proposed in the literature. One of them is the addition of a P-GaN layer below the gate[50], [51].

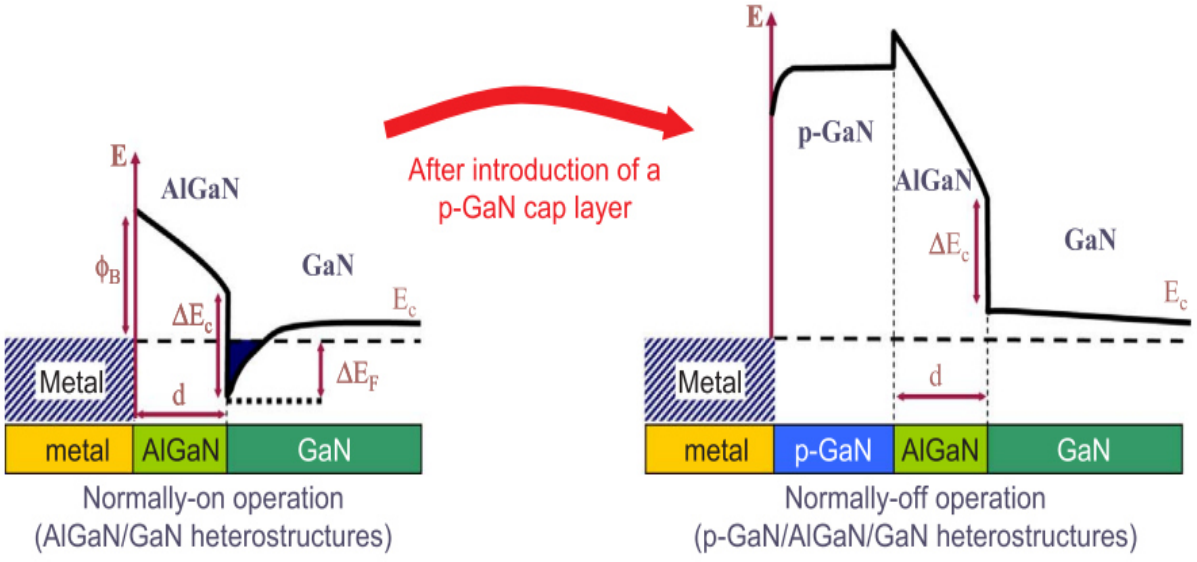


Figure 1-21 : Band diagram of HEMT transistor before and after the introduction of the P-GaN layer below the gate [51]

Figure 1-21 shows the band diagram before and after adding the P-GaN layer. Without any applied gate bias, the 2DEG position is below the Fermi level, which implies continuous electron transport. By adding the P-GaN layer, the 2DEG position is raised higher than the Fermi level, resulting in a complete 2DEG depletion. Owing to the high 2DEG mobility ($\mu > 2000 cm^2/V.s$), the HEMT exhibits high on-state performance with low Ron. However, these performances can be harmed by trapping issues resulting in a dynamic Ron degradation caused for instance by carbon background doping and other surface trapping phenomena. Moreover, the HEMT device is highly sensitive to defects.

In off-state, the breakdown voltage of HEMTs is basically limited by the critical electric field of the silicon substrate. At high voltage, the distribution of the electric field is not homogeneous, generating electric field peaks affecting the device performance, such as the electric field at the gate edge, at the buffer, and at the buffer / silicon substrate. The critical electric field of silicon is ten times lower than that of GaN. Ideally, buffer configurations like superlattice buffers should withstand the high electric field. However, due to growth defects and process-induced damages, the electric field generally reaches the substrate. To address this, the silicon substrate can be locally removed from the backside of the transistor (Figure 1-22.a). A drastic improvement of breakdown voltage can be observed (Figure 1-22.c) after local substrate removal[42].

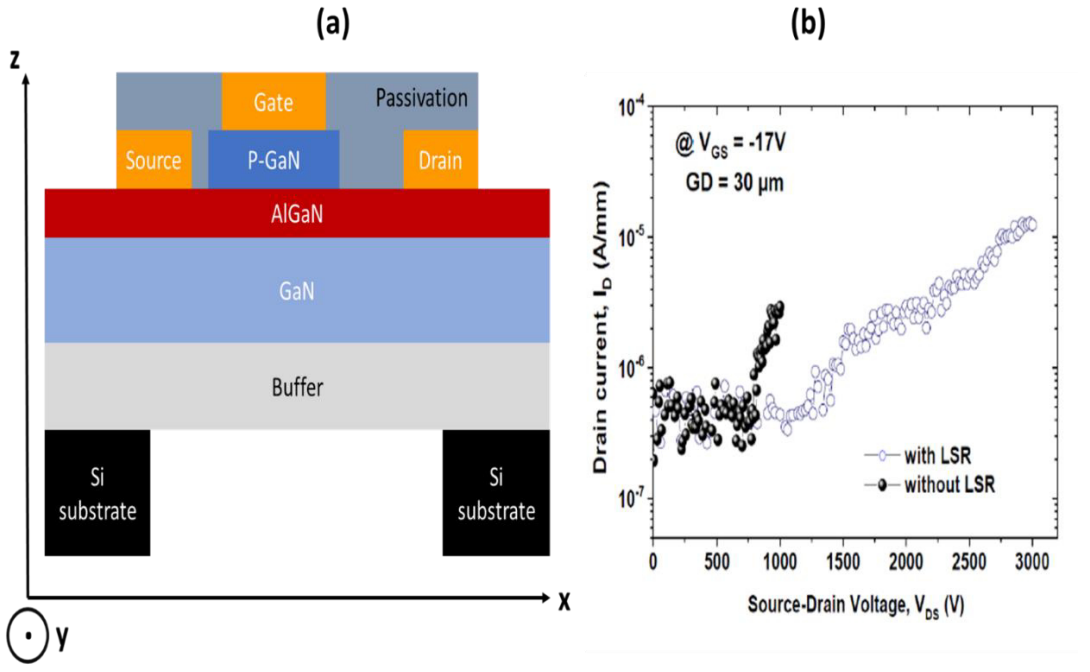


Figure 1-22 : (a) HEMT with local substrate removal (b) off state measurements of HEMT transistor with and without local substrate removal [47]

Despite their off-state capabilities, rather large device sizes are needed HEMTs to reach high breakdown voltages. In turn, it is necessary to enlarge the transistors along the x-axis (Figure 1-22.a) by increasing the drain-gate distance[50]. Additionally, increasing the device size along the y-axis allows for higher current. These design parameters result in a large device size along the x and y axes, which limits the number of devices per wafer and makes lateral HEMTs less competitive as compared to vertical devices for medium and high voltage operation (> 650 V).

The breakdown of lateral GaN HEMTs is characterized as a hard breakdown as opposed to soft avalanche breakdown, where the leakage current mechanism is dominated by dislocations, defects, due to excessive electric field peak. Consequently, no impact ionization current occurs in GaN lateral HEMT structures, resulting in the absence of avalanche capability in this configuration. As a result, the operational voltage of HEMT devices is much lower than the hard breakdown voltage. For instance, a device with a hard breakdown voltage of 2000 V is typically derated to an operational voltage of less than 1000 V.

The main drawbacks of GaN HEMT devices can be summarized as follows:

- Trapping issues due to defects and surface charges (close to the 2DEG).
- Large device area due to the increased lateral dimensions for higher voltage operation.
- Hard breakdown due to the absence of avalanche capability.

For these reasons, HEMT-based devices face significant challenges for commercialization at 650 V and above. Therefore, a new technology should be developed that incorporates avalanche capability and utilizes the vertical dimension to reduce the size of the device.

1.2.4 Vertical structure

At the beginning of this chapter, the transition from lateral to vertical architecture design for silicon-based devices was discussed and justified by the benefits of vertical design. In the case of GaN, vertical HEMTs known as CAVET (Figure 1-23)[52], has already been demonstrated. However, the technology is rather complex and not mature enough limiting the device and reliability performances.

The better approach is to use a structure without the 2DEG to reduce the device's sensitivity to trapping issues induced by the electric field. Vertical GaN junction-based structure is attractive in this frame, where P-doping and N-doping are the primary factors in on- and off-state conditions. Similar to silicon, the use of junction-based technology with a drift region could unlock new possibilities for GaN devices.

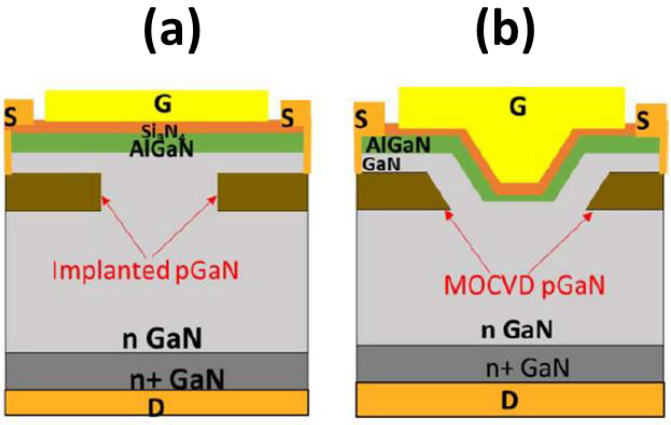


Figure 1-23 : CAVET based structure with a normally on (a) and off (b) design[52]

Vertical GaN junction-based devices are potential candidates to surpass the limitations of existing technology, offering outstanding performance owing to GaN properties such as high electric field strength (allowing for thinner devices with high blocking capability) and high electron mobility (enabling high current spreading)[53], which are essential for both on- and off-state performance. Vertical GaN-based structures also benefits from mature and comprehensive physics, enabling non-complex device design and ensuring reliable performance[2], [3], [54]. Additionally, it leverages impact ionization properties, enabling soft breakdown with avalanche capability, which underscores the need for developing this type of structure[26], [55], [56], [57], [58]. Furthermore, since the architecture is vertical (aligned with the Z-axis), the device can withstand high voltages with small sizes, and thus high integration unlike lateral HEMT structures.

To summarize, the main advantages of using junction-based structures are:

- Non-complex design with mature, comprehensive physics.
- High design flexibility.
- High integration with small device fingerprint on the wafer.
- Reliable performance.
- Low cost of fabrication if grown on foreign substrates.

The most typical junction-based structures are the Schottky rectifier[59], P-i-N diode[56], and TMOSFET (Figure 1-24)[60]. The choice of device type depends on the application. For example, the Schottky rectifier has a moderate breakdown voltage with high switching capability, while the PiN punch-through diode is designed for high breakdown voltage with low Ron and acceptable switching capability.

All junction-based devices rely on the drift region to withstand the high breakdown field. The doping and thickness of the drift region (I layer) should be optimized according to the targeted breakdown voltage and Ron of the devices. From Equation 7, higher doping of the drift region reduces the breakdown voltage. Additionally, higher doping allows for better current spreading and thus lower resistance. For a given doping concentration, the breakdown voltage can also be adjusted by the drift region thickness. A thicker drift region provides a larger surface to further spread the electric field, thereby increasing the breakdown voltage. However, a thicker drift region also means a longer distance for charge carrier transport, which increases Ron. Therefore, the doping and thickness of the drift region must be wisely balanced to meet the specific requirements of the targeted structure.

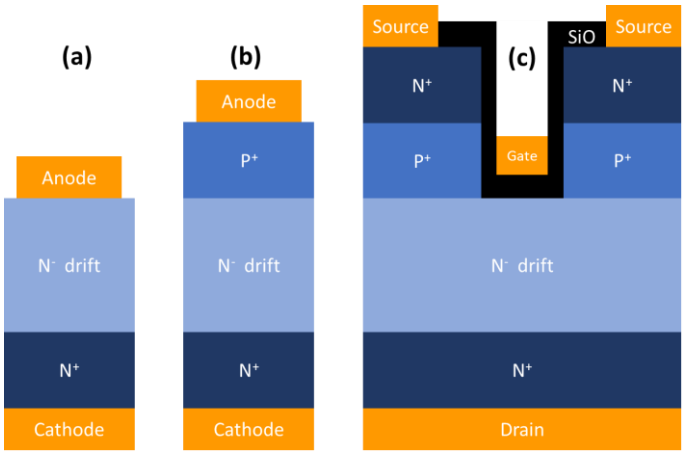


Figure 1-24 : Design of (a) Schottky rectifier, (b) PIN diode and (C) T-MOSFET

As mentioned before, silicon is a typical N-type dopant for GaN and is readily accessible. This type of doping is currently well-matured and does not have activation issues. However, the growth of GaN by metal-organic chemical vapor deposition (MOCVD) often includes a carbon concentration incorporation that must be reduced to prevent C-compensation of N-doping[61], [62], [63], [64], [65]. Carbon acts as a P-type dopant in GaN and a residual concentration during growth is typically observed. In lightly N-doped

layers (like the drift region), carbon can reduce the net-ionized doping concentration significantly.

To achieve high current density, a bottom highly N+ doped layer is used, where electrons are the majority carriers and holes are the minority carriers. This layer is primarily connected to the drain in transistors or to the cathode in diodes.

To ensure a proper switching operation for the diode, a barrier should be added on top of the drift layer. Two solutions are proposed: the first is adding a Schottky contact with a high metal work function, leading to a Schottky rectifier design. The second option is adding a P-doped layer on top, resulting in PIN punch-through diodes. The P-doped layer is critical because its doping concentration directly influences the blocking capability and current spreading. Magnesium is used for P-doping GaN, but this type of doping is highly susceptible to hydrogen passivation and suffers from limited activation efficiency (around 1%)[66], [67], [68], [69], [70].

To develop T-MOSFETs (trench metal-oxide-semiconductor field-effect transistors), an additional N+ doped layer is added on top of the PIN diode. This layer serves as the source layer for electrons. The current in the T-MOSFET is controlled by the gate bias. When a positive bias is applied to the gate, an inversion layer is created at the vertical P/oxide interface. This creates a path for electron transport between the N+ layer and the N- layer. When a positive voltage is applied to the drain, the current flows vertically from source to drain through the inversion layer of the P and the N- layers.

1.2.5 GaN on Silicon vertical based devices as potential solution

Most of vertical GaN devices are based on the N-N+ layer structure, where the N+ layer is the bottom layer, which is used for the backside contact. The corresponding fabrication process must be optimized in order to avoid generating parasitic leakage current or high contact resistances directly affecting the device performance. Ideally, the use of GaN-on-GaN-based devices with a doped N+ substrate is the “natural” approach. However, as discussed earlier, GaN substrates cost of fabrication and size limitations do not currently comply with cost-effective power applications. Developing high quality GaN-on foreign

substrate, in particular GaN-on-silicon vertical power devices would be ideal. Several critical points need to be optimized in this frame:

- Dislocation Density and Defects: Minimizing dislocation density and defects is crucial to unlocking the full performance potential of these devices. Vertical charge transport are less sensitive to dislocation density issues compared to lateral structures in on-state. However, in off-state condition, uncontrolled dislocations can create additional leakage paths, dominating the avalanche capability and leading to hard breakdown [22][13].
- Growth of Thick GaN Epitaxy on Silicon: This is a major challenge due to the tensile strain that can create cracks when excessively increasing the epi-thickness. Optimizing the nucleation and buffer layers can help mitigate this issue[71], [72], [73], [74], [75], [76].
- Ensuring a low contact resistance to the Bottom Layer: For vertical GaN on silicon, a connection to the bottom N+ layer must be ensured with low contact resistances. This can be achieve in a quite straightforward way using a pseudo-vertical design (Figure 1-25.a). In this design, a mesa window is created by deep etching in order to reach the bottom N+ layer. However, in the case of fully vertical architectures, the backside N+ layer needs to be connected with a proper vertical alignment to the frontside. The development of local substrate removal techniques to access the backside is now well mastered on silicon substrates resulting in rather thin membranes in the order of micrometers that can still be handled with high uniformity despite fragility issues (Figure 1-25.b).

In summary, while the development of vertical GaN-on-silicon devices offers promising potential, addressing dislocation density, ensuring the growth of thick GaN epitaxy, and achieving low contact resistances to the bottom layer are critical challenges that need to be addressed. The development of vertical GaN-on-silicon devices has attracted significant attention from both academic and industrial communities due to their promising performance and low fabrication cost. In the next section of this chapter, I will present an overview of the progress made in GaN-on-silicon vertical devices. For a fair benchmark, GaN-on-GaN and GaN-on-foreign vertical devices will be also presented.

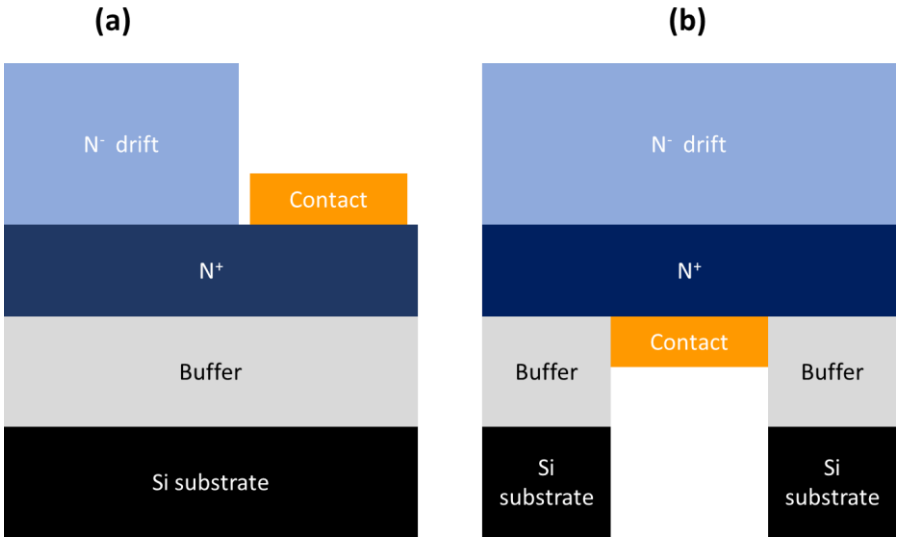


Figure 1-25 : Schematic cross section of (a) pseudo vertical and (b) fully vertical architecture.

1.3 State of the art of GaN diodes

1.3.1 Baliga Figure of merit

Power devices can be characterized by several figure of merits such as the on-state resistance (Ron) and the breakdown voltage. These parameters depend on the intrinsic electrical properties of the material as follows[2], [3], [77], [78]:

$$\boldsymbol{Ron = \frac{4BV^2}{\varepsilon \mu_n {E_c}^3}} \qquad \textit{Equation 10}$$

This equation describes the dependence between the on-state resistance (Ron), the breakdown voltage (BV), the mobility, and the critical electric field of the semiconductor. It provides a strong indication of the material's performance. Figure 1-26 shows the relationship between Ron and BV (Equation 10), where it can be observed that the physical limit of GaN is significantly superior to that of silicon. In the 600-1200 V range, the ideal Ron of GaN is 1000 times lower than that of silicon.

GaN-based devices can thus be benchmarked by plotting the breakdown voltage and the extracted Ron of the devices. The desirable performance should be near the ideal Ron(BV) curves. This comparison is called Baliga's benchmark, where the figure of merit can be presented as follows:

$$\boldsymbol{BFOM = \frac{\varepsilon \mu_n {E_c}^3}{4} = \frac{BV^2}{Ron}} \qquad \textit{Equation 11}$$

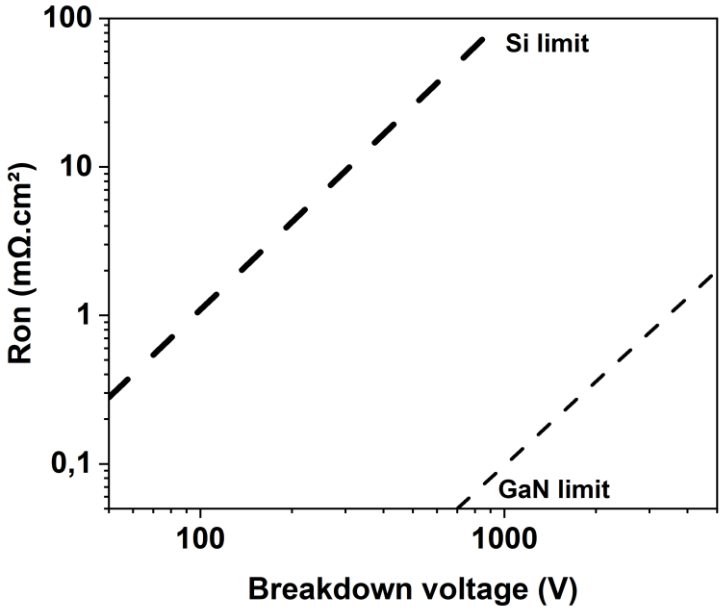


Figure 1-26 : Ideal Ron(BV) of silicon and GaN

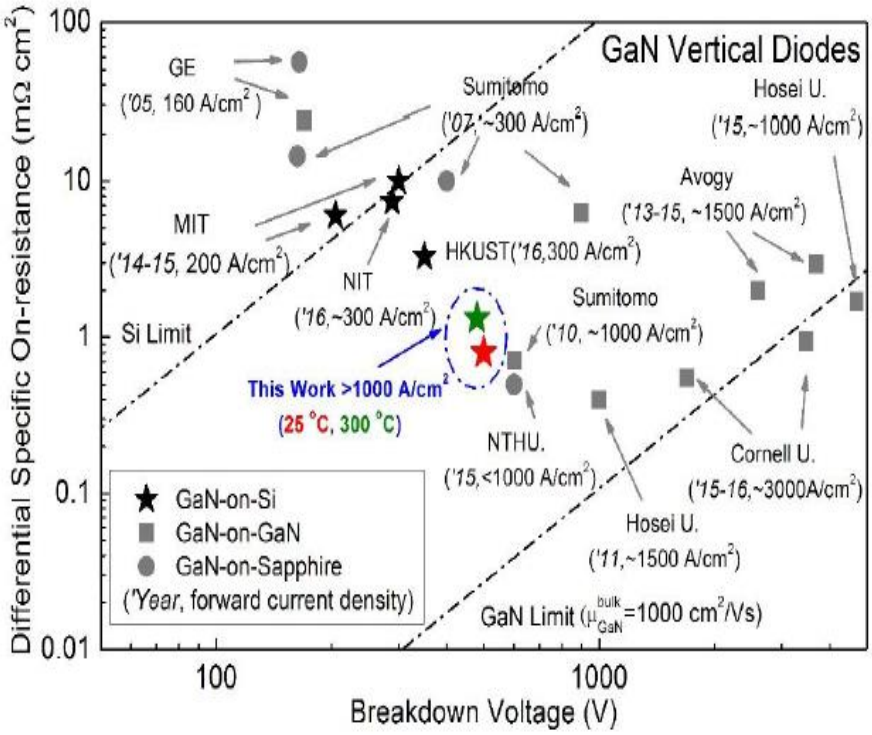
In this way, the device performance can be fairly compared, allowing for a clear comparison of different devices and technologies by plotting their breakdown voltage and on-state resistance, with the goal of approaching the ideal Ron (BV) limit, thus highlighting advancements and improvements in GaN power device technology.

1.3.2 The progress of vertical GaN-on-Silicon power devices

Vertical GaN-on-Silicon devices have attracted significant attention over the last decade, with P-I-N diodes being the primary focus of development. In 2014, MIT demonstrated the first pseudo-vertical P-I-N diode based on a silicon substrate, achieving a breakdown voltage of over 300 V and a rather high Ron[79]. This marked the beginning of the development of vertical GaN-on-Silicon devices. MIT continued to work on P-I-N diodes, enhancing the device performance to achieve a breakdown voltage of 500 V with a low Ron of less than 1 mΩ.cm^2 (Figure 1-27)[80].

The structures used in these developments include both pseudo-vertical and fully vertical architectures. The fabrication process of the fully vertical design involves bonding and debonding on silicon substrates (Figure 1-28). More specifically, the frontside is bonded on silicon substrate by thermal compression of gold. Subsequently, the backside silicon and buffer layers are fully etched.

(a)



(b)

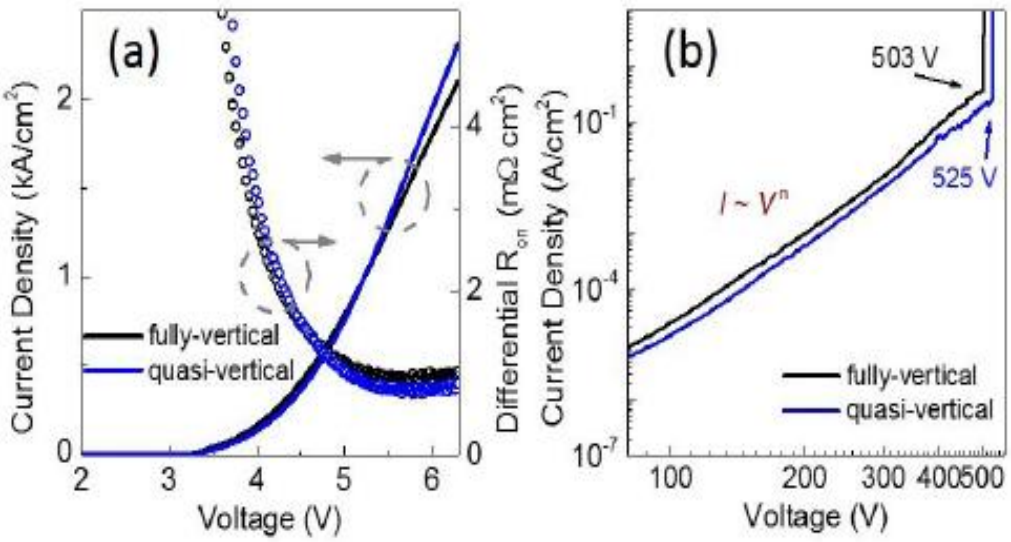


Figure 1-27 : (a) Baliga benchmark from MIT work of vertical GaN power devices (b) Characterization of the developed PiN diodes

The full substrate etching of vertical heterostructures is complex and prone to failure, resulting in a low yield of active devices per sample. The yield is further reduced when applied to large wafer diameters. Therefore, the use of local substrate removal remains a more efficient approach. In 2018, MIT demonstrated a fully vertical P-I-N diode using local

substrate removal [81] as used in previously reported works for lateral HEMTs [82], achieving a high breakdown voltage of 720 V and a low Ron of 0.35 mΩ·cm² (Figure 1-29).

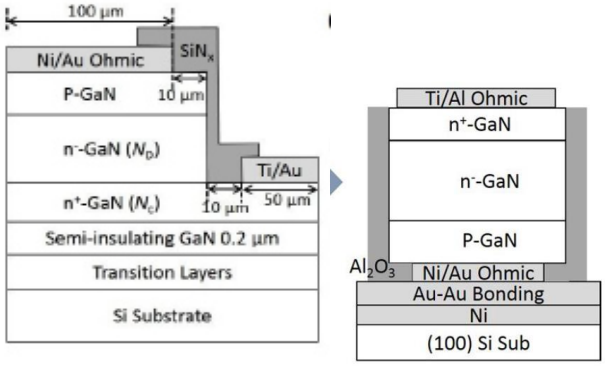


Figure 1-28 : Design architectures of the developed PiN diode by MIT

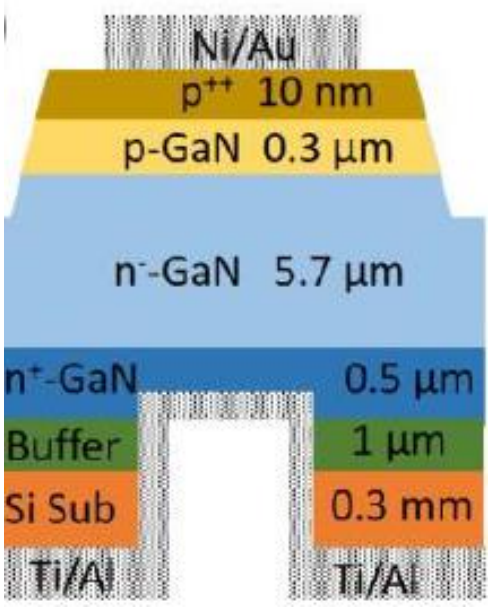


Figure 1-29 : Developed fully vertical PiN diode using local substrate removal by MIT

Recent progress in vertical GaN-on-Silicon diodes has achieved promising results, including 1000 V class devices[83], [84], [85]. Most developed P-I-N diodes in the literature have a pseudo-vertical design, which suffers from current spreading issues related to the design[86], [87], [88], [89], [90], [91], [92], [93]. This explains the use of small diodes to demonstrate low on-state resistance but limited on-state current level.

Fabrication of the fully vertical architecture is essential to extract the full performance of vertical GaN-on-Silicon devices. In particular, the backside ohmic contact on top of the N-face backside GaN crystal needs to be assessed and optimized with respect to the unusual

polarity. One of the challenges lies in the local substrate approach, which prevents the use of standard photolithography techniques to evaluate the backside contact quality.

Vertical GaN-on-GaN and GaN-on-Sapphire devices have already demonstrated a key figure of merit : the avalanche capability, which will be discussed later. This feature is mandatory for reliable devices with stable performance. Unfortunately, avalanche capability has not been demonstrated in vertical GaN-on-Silicon devices due to the high dislocation density that creates additional leakage mechanisms, thereby hindering avalanche capability. Moreover, the quality of the fabrication process can also impact the breakdown voltage by inducing damages to the crystal. Thus, high-quality processing and growth optimization for vertical GaN-on-Silicon devices up to 1200 V need to be achieved.

1.3.3 An overview of vertical GaN on GaN, Sapphire and SiC PiN diodes

To establish a fair benchmark for vertical GaN-on-silicon P-I-N diodes, this section presents a literature review of reported vertical GaN P-I-N diodes on various substrates, including GaN, sapphire, and SiC.

1.3.3.1 Vertical GaN on GaN PiN diodes

Thanks to the use of native substrates, vertical GaN diodes exhibit high performance characteristics, including low on-resistance (Ron), high breakdown voltage, and avalanche capability. These advantages are attributed to the low lattice mismatch and the ability to grow thick layers. As evidence in 2022 [94] Sandia National Laboratories reported a study demonstrating a P-I-N diode with a 50 µm drift region (Figure 1-30), achieving a breakdown voltage over 6000 V with avalanche capability (Figure 1-31. a). Additionally, a low on-resistance of 10 $m\Omega.cm^2$ was obtained in on-state (Figure 1-31. b).

Several other studies in the literature also demonstrate the high performance of vertical GaN-on-GaN P-I-N diodes. [55], [56], [57]. However, the industrial use of GaN-on-GaN for power electronics in the 600-1200 V range is excluded for the moment due to the limited availability of large wafer sizes and the related high cost.

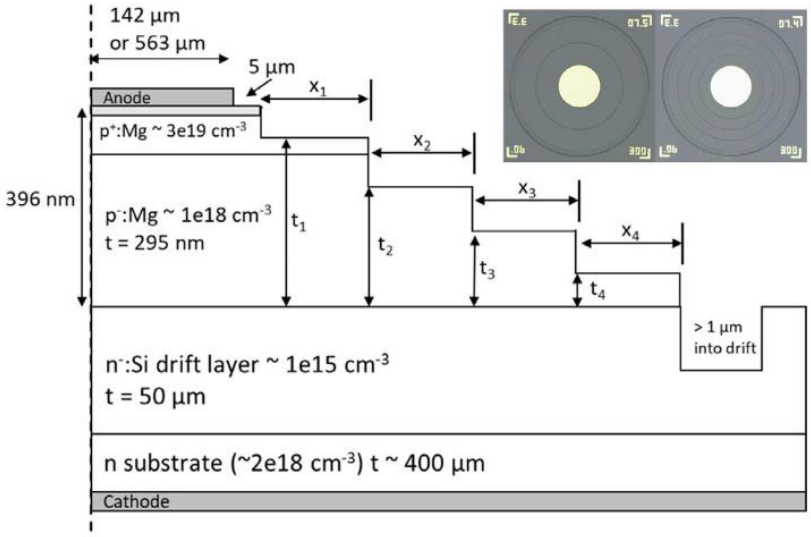


Figure 1-30 : Schematic cross section of vertical GaN on GaN PiN diode from Sandia National Laboratories[94]

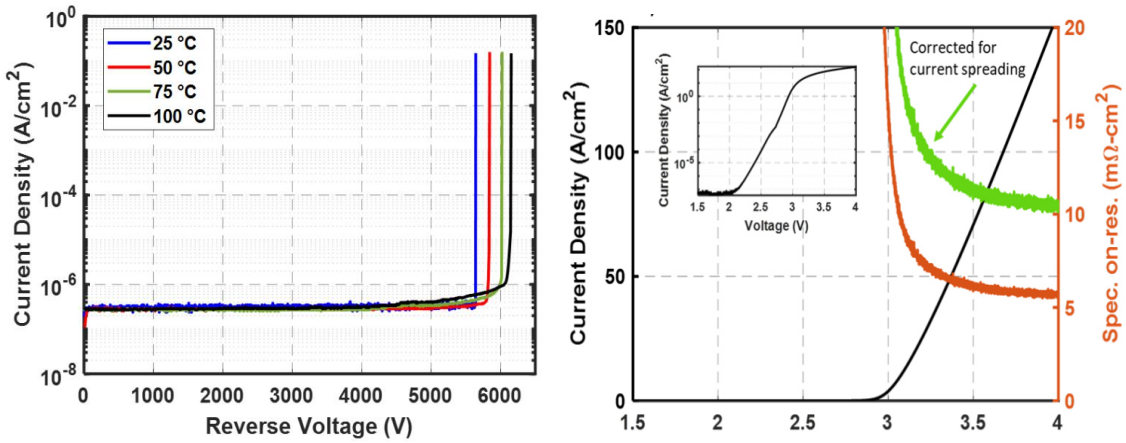


Figure 1-31 : (a) off state and (b) on state characteristics of vertical GaN on GaN PiN diodes from Sandia National Laboratories

1.3.3.2 Vertical GaN on Sapphire diodes

Several publications have discussed the fabrication of P-I-N diodes on sapphire substrates. Unlike GaN-on-GaN devices, only pseudo-vertical design is typically employed for GaN-on-sapphire. To achieve a fully vertical design when grown on sapphire, the active region must be transferred through a substrate debonding process. One approach involves the laser lift-off technique to remove the sapphire substrate and fabricate fully vertical Schottky diodes [37]. This process employs a laser to separate the GaN layer from the sapphire substrate.

Using a sapphire substrate, a thick GaN drift layer can be grown with a high quality, [35] which enabled vertical GaN-on-sapphire P-I-N diodes with a 10 µm drift region, and a

breakdown voltage of 1350 V but without avalanche capability (Figure 1-32). Moreover, [36] demonstrates the possibility of achieving avalanche soft breakdown on a sapphire substrate (Figure 1-33). However, due to the complexity of the laser lift-off process, this technology has not been adopted yet.

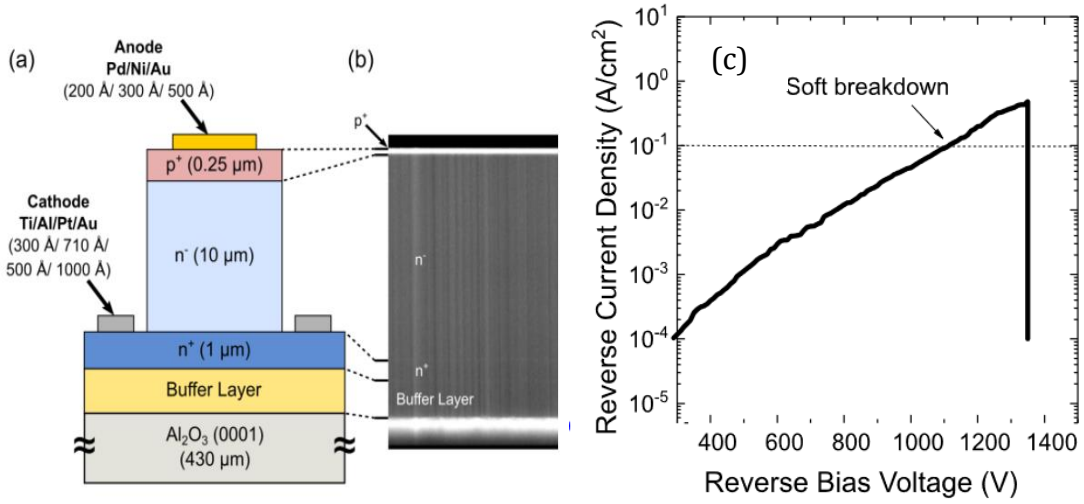


Figure 1-32 : (a) schematic and (b) SEM cross section of the developed GaN on Sapphire PiN diodes delivering 1350 V breakdown voltage [35].

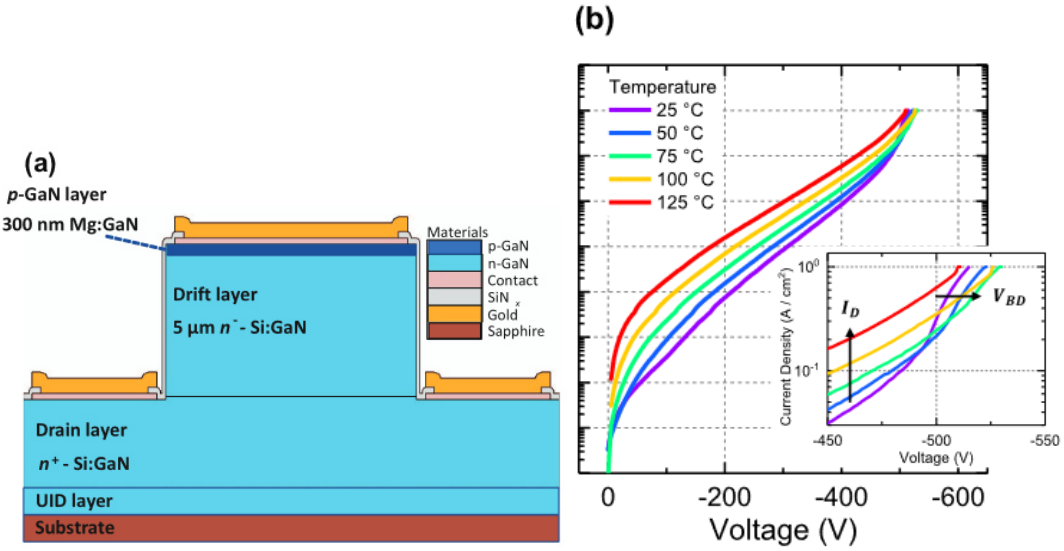


Figure 1-33 : (a) schematic cross section of a vertical GaN on Sapphire PiN [36] diode with avalanche capability (b)

1.3.3.3 Vertical GaN on SiC diodes

For the first time, a fully vertical GaN-on-SiC P-I-N diode has been demonstrated [95], showing a breakdown voltage of 850 V (Figure 1-34) without avalanche capability and a low on-resistance (Ron) of 0.25 mΩ·cm^2. This fully vertical design was made possible by

utilizing a conductive substrate and buffer layers. Further scaling of the breakdown by growing a thicker drift layer as well as avalanche soft breakdown still need to be demonstrated.

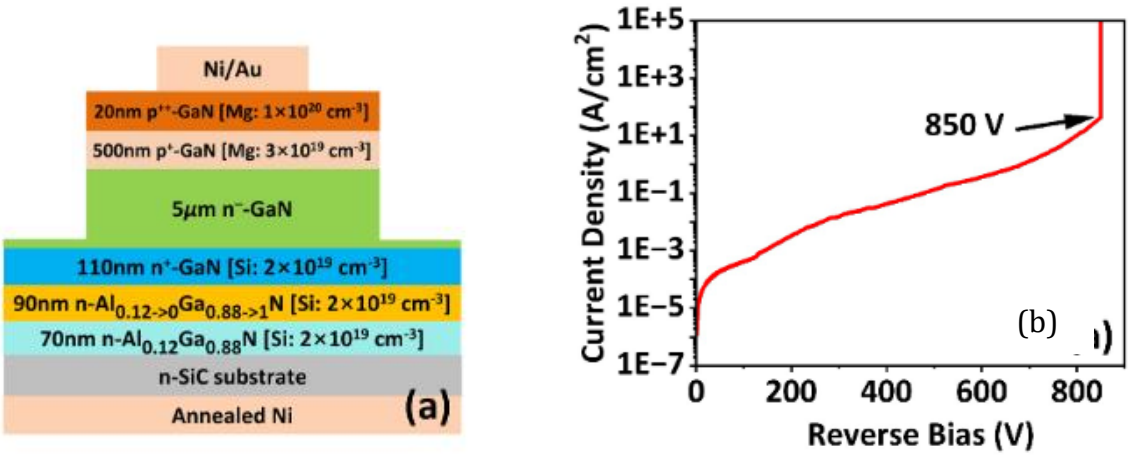


Figure 1-34 : (a) schematic cross section of vertical GaN on SiC PiN diodes and (b) off state characteristic [95].

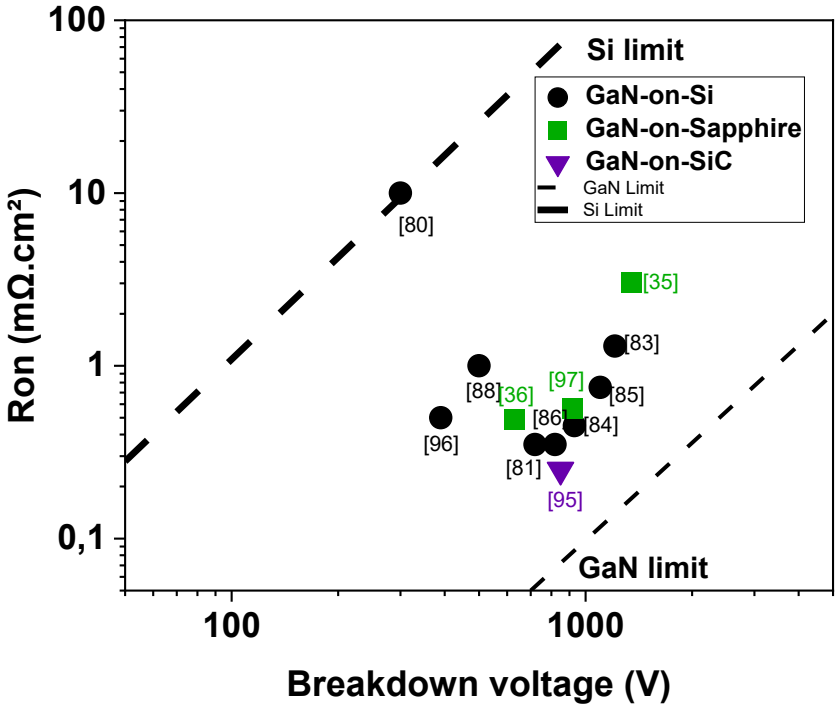


Figure 1-35 : Baliga benchmark of GaN-on-Silicon vertical PiN diodes[35], [36], [80], [81], [83], [84], [85], [86], [88], [95], [96], [97]

1.4 Conclusion

Figure 1-35 shows the current benchmark of vertical GaN P-I-N diodes on foreign substrate breakdown voltage versus Ron. It should be noted that:

- Diodes in [36]show avalanche capability
- Fully vertical GaN-on-Silicon : [77], [78], [84]
- Fully vertical GaN-on-Sapphire : No references found
- Fully vertical GaN-on-SiC : [95]

The current progress of vertical GaN-on-Silicon devices is promising, owing to the excellent physical properties of GaN and the development of new process techniques. Recent trends indicate that vertical GaN-on-Silicon is an undeniable solution to address the issues associated with lateral GaN-on-Silicon HEMTs as well as the high fabrication costs of SiC. However, there are still hurdles to be overcome for the industrial future development of vertical GaN-on-Silicon-based devices. In this work, we aim to contribute to the optimization of this new technology by addressing some related challenges. This work focuses on vertical diodes, enabling to develop advanced processing, to support the growth optimization and moreover gain knowledge would be transferable to transistors. Briefly, the objectives of this thesis are as follows:

- Optimization of vertical GaN-on-Silicon diode design using TCAD simulations.
- Development of high-quality processing for fully vertical structures.
- Assessment of the backside N-face ohmic contacts in fully vertical structures.
- Comprehensive comparison of pseudo-vertical and fully vertical architectures.
- Demonstration of high current spreading in large diode sizes in fully vertical devices.
- Demonstration of avalanche capability in high voltage fully vertical GaN-on-Silicon devices.

Chapter 2: Vertical power based device design

In this chapter, we analyse vertical GaN-on-Silicon-based diodes. A comprehensive study of the device physics is essential to understand the interplay between different parameters. TCAD simulation is a valuable tool that can provide trends of device performance and further understand the device physics when using proper simulation models. Simulation is a cost-effective method for designing electronic devices, offering optimized time consumption compared to traditional process and fabrication methods.

One of the best-known TCAD simulation software for gallium nitride is Silvaco, which has an updated database of the latest physical interactions of materials reported by both academia and industry. In this chapter, we describe Silvaco TCAD simulation and present detailed TCAD simulation studies of the different epilayers included in vertical GaN-on-Silicon diodes. We then propose an optimization of the design, including doping and layer thicknesses to achieve our objectives, focusing on demonstrating avalanche capability and reaching 1200V class vertical GaN-on-Silicon diodes with high current spreading.

2.1.1 Silvaco Software

SILVACO (Silicon Valley Corporation) offers an integrated suite of software tools designed for the design, modeling, and simulation of semiconductor devices, enabling engineers to predict device performance before fabricating prototypes. This capability is particularly beneficial in research and development settings, as it streamlines testing processes and significantly lowers the costs associated with designing and producing electronic components. The TCAD-SILVACO platform incorporates sophisticated physical models that leverage efficient numerical methods, innovative meshing strategies, and advanced optimization techniques, delivering simulation results that closely align with experimental data. One of the key strengths of this simulation tool is its ability to visualize and provide deeper insights into complex physical phenomena that are challenging to measure and observe directly[98].

Figure 2-1 illustrates the block diagram of the simulation modules utilized in TCAD-SILVACO. The DECKBUILD module serves as the interface for defining simulation input parameters, which detail the technological processes and physical phenomena to be modeled. Within this environment, users can configure simulations using various tools like ATHENA, ATLAS, and SSUPREM3. The output of these simulations, including

technological parameters (such as junction depth and carrier concentration) and electrical characteristics (such as threshold voltage and current), can be viewed in the output window. The TONYPLOT module is used for visualizing the structure and analyzing output parameters such as quantum efficiency, spectral response, and I-V characteristics, providing a comprehensive view of the simulation results. This modular approach enables efficient setup and analysis of semiconductor device simulations, enhancing the ability to predict device behavior before fabrication.

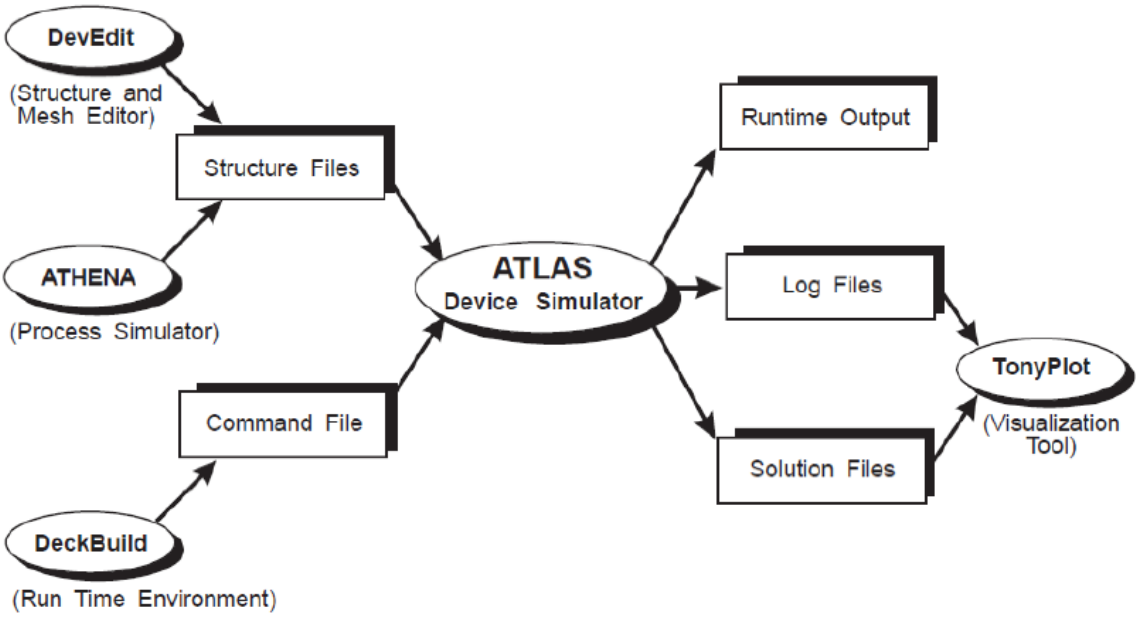


Figure 2-1 : SILVACO diagram bloc[98]

ATLAS is a versatile two-dimensional (2D) simulation tool designed for modeling semiconductor devices, capable of predicting their electrical characteristics under various operating conditions, including steady-state, transient, and frequency regimes. Beyond electrical performance, ATLAS provides insights into the internal distribution of key electrical variables such as current density and electric field vectors. It enables the simulation of a wide range of devices, such as diodes and transistors, by representing them as a mesh grid where each node is defined by parameters like material type, doping profile, and dopant concentration. This detailed node-based approach allows for precise calculation of properties such as carrier density and electric field intensity across the device. Electrodes are modeled as surface boundaries with specified conditions, like applied voltage, facilitating accurate simulation of electrical behavior. In conjunction with the ATHENA module, which simulates the fabrication processes, ATLAS can model

complex device structures with high fidelity, reflecting real-world manufacturing steps and resulting geometries. TONYPLOT, on the other hand, is the dedicated visualization tool within the TCAD-SILVACO suite. It offers comprehensive capabilities for plotting and analyzing simulation results, including structural visualizations, doping profiles, and electrical characteristics of semiconductor devices. Depending on the nature of the simulation, TONYPLOT can represent these characteristics in one, two, or three dimensions, making it an essential tool for interpreting and presenting simulation outcomes.

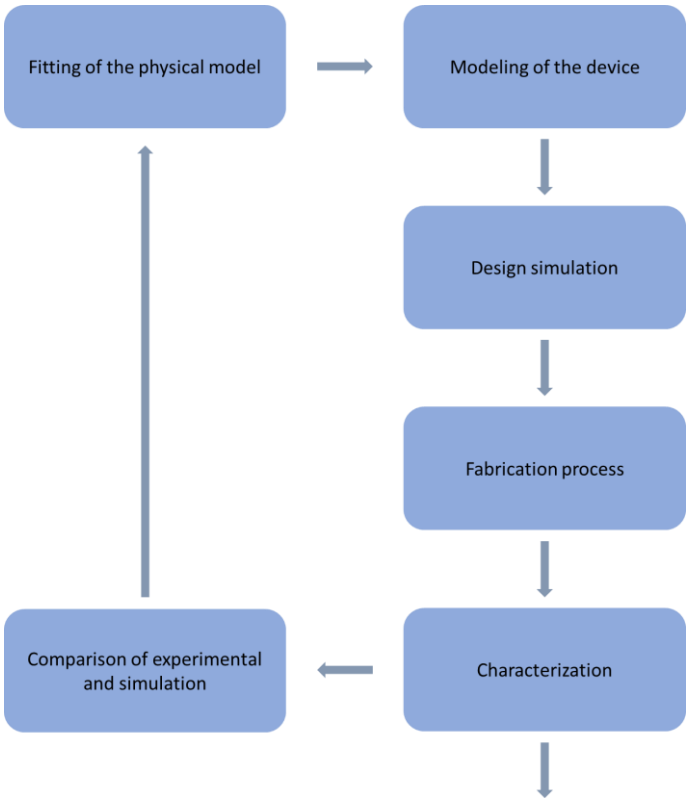


Figure 2-2 : simulation and process design optimization flow

SILVACO's Atlas simulation can predict device performance. However, for optimized and accurate simulations, a feedback loop should be maintained between simulation and experimentation. This can be achieved by benchmarking experimental results against simulations to identify discrepancies. To overcome these differences, physical models should be adapted and fitted by either changing the physical model or adjusting the parameters in Atlas.

Accurate simulation of GaN-based devices requires enhanced physical models. To support this, the Silvaco software database is regularly updated with the latest advancements

from both academia and industry. Therefore, this TCAD tool provides a wide range of models covering both 2DEG- and junction-based structures. The understanding of GaN physical properties, especially for GaN HEMT devices, is still evolving due to the complex epitaxial interactions between layers. For junction-based structures, models leverage the maturity of silicon to predict device performance, and by incorporating the physical properties of GaN, Silvaco TCAD can reliably predict device performance[99], [100], [101], [102], [103], [104].

2.1.2 Simulation of GaN based devices

As mentioned before, the Silvaco database ensures a variety of physical models that support the properties of GaN. In this section, we will provide an overview of the principal GaN simulation models.

2.1.2.1 Mobility

To describe the mobility of GaN, μ_n and μ_p, the GaNsat built-in model is used. It is based on the fitting of bulk nitride Monte Carlo simulation. This is ensured using the following equation [98]:

$$\mu_n = \frac{\mu_{n0}(T,N) + \mathrm{VSATN}\dfrac{E^{\mathrm{N1N}\cdot\mathrm{GANSAT}-1}}{\mathrm{ECN}\cdot\mathrm{GANSAT}^{\mathrm{N1N}\cdot\mathrm{GANSAT}}}}{1+\mathrm{ANN}\cdot\mathrm{GANSAT}\left(\dfrac{E}{\mathrm{ECN}\cdot\mathrm{GANSAT}}\right)^{N2N\cdot\mathrm{GANSAT}}+\left(\dfrac{E}{\mathrm{ECN}\cdot\mathrm{GANSAT}}\right)^{\mathrm{N1N}\cdot\mathrm{GANSAT}}}$$

$$\mu_p = \frac{\mu_{p0}(T,N) + \mathrm{VSATP}\dfrac{E^{\mathrm{N1P}\cdot\mathrm{GANSAT}-1}}{\mathrm{ECP}\cdot\mathrm{GANSAT}^{\mathrm{N1P}\cdot\mathrm{GANSAT}}}}{1+\mathrm{ANP}\cdot\mathrm{GANSAT}\left(\dfrac{E}{\mathrm{ECP}\cdot\mathrm{GANSAT}}\right)^{N2P\cdot\mathrm{GANSAT}}+\left(\dfrac{E}{\mathrm{ECP}\cdot\mathrm{GANSAT}}\right)^{N1P\cdot\mathrm{GANSAT}}}$$

Where :

- $\mu_{(n,p)0}$ describes the low field mobility.
- E describes the electrical field.
- EC(P,N) describes the critical electric field
- VSAT(P,N) describes the saturation velocity

The GaNsat model allows the simulation of mobility for both electrons and holes, incorporating velocity saturation modeling. This can be applied to both high electric field and low electric field, making it beneficial for simulating both on-state and off-state conditions (Figure 2-3)[98].

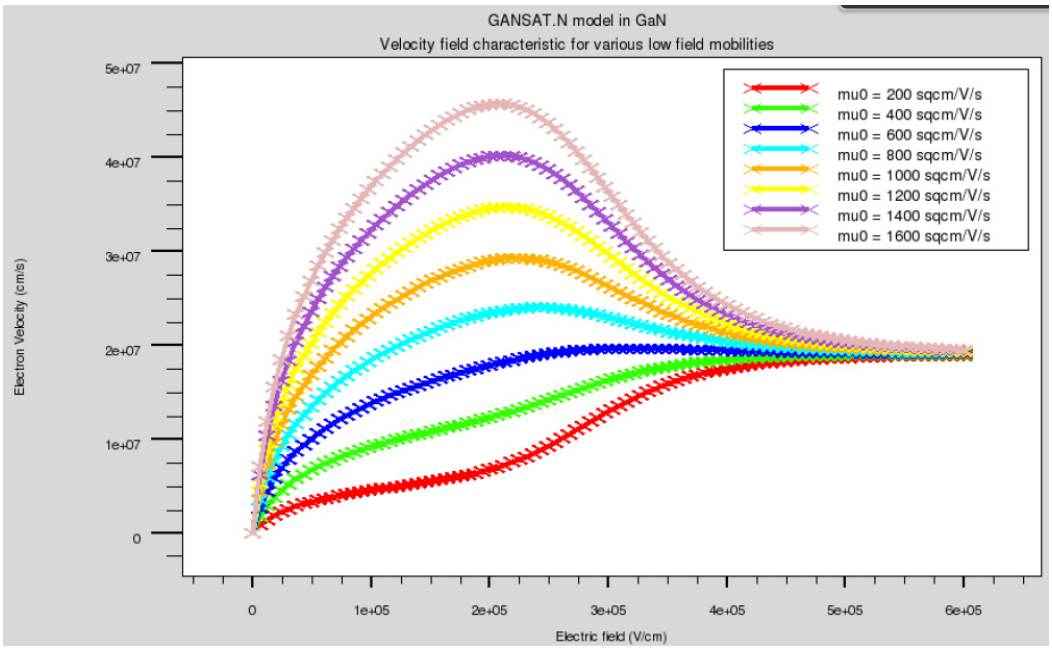


Figure 2-3 : Electron velocity versus Electric field for different μ0

2.1.2.2 Carrier recombination

Concerning carrier recombination, the Shockley-Read-Hall (SRH) recombination model is used to describe the recombination of electrons and holes. This occurs when a defect state captures an electron from the conduction band, which then recombines with an existing hole from the valence band. The excitation in the forbidden bandgap releases a phonon instead of a photon. The following equation describes the Shockley-Read-Hall (SRH) recombination[98]:

$$R_{SRH} = \frac{pn - n_{ie}^2}{\mathrm{TAUP0}\left[n + n_{ie} exp\left(\frac{\mathrm{ETRAP}}{kT_L}\right)\right] + \mathrm{TAUN0}\left[p + n_{ie} exp\left(\frac{-\mathrm{ETRAP}}{kT_L}\right)\right]}$$

Where :

- ETRAP describes the difference of energy between the trap and intrinsic fermi level.
- T_L describes the lattices temperature.
- TAU(P,N)0 describes the electron and holes lifetimes

2.1.2.3 Breakdown mechanism

One of the critical parameters in the simulation of GaN power devices is the off-state characteristic. The breakdown point, avalanche capability, and accurate off-state behavior are related to ionization impact phenomena. For accurate simulation, the Selberherr's Impact Ionization Model is used. This model provides good predictions of ionization impact phenomena with enhanced and accurate calculations compared to existing models. The coefficient α (Equation 3) is described by Selberherr's Impact Ionization Model as follows[98]:

$$\alpha_n = \mathrm{AN} exp\left[-\left(\frac{\mathrm{BN}}{E}\right)^{\mathrm{BETAN}}\right]$$

$$\alpha_p = \mathrm{AP} exp\left[-\left(\frac{\mathrm{BP}}{E}\right)^{\mathrm{BETAP}}\right]$$

Where :

- E describes the applied electric field
- AP, BN, BP, BETAN, and BETAP describes the fixed Selberherr's Impact Ionization Model coefficient which are used in the fitting of the ionization impact breakdown.

Additional electron generation can be produced via band bending under high electric field. This electron tunnelling between the conduction and valence bands can be described using the band-to-band tunnelling model, as represented by the following equation[98]:

$$G_{BBT} = D\ \mathrm{BB.A}\ E^{\mathrm{BB.GAMMA}} exp\left(-\frac{\mathrm{BB.B}}{E}\right)$$

Where :

- E is the applied electric field

- D defines a statical coefficient
- BB.A, BB.A and BB.Gamma represents the electron effective mass depending parameters

In addition to the ionization impact current, an additional leakage current is induced by the threading dislocation density. This leakage current can be described using the non-local variable hopping mobility model. The additional current density can be represented as follows[98]:

$$J_{vhop} = \frac{Q\ NLVHOP.AF\ NLVHOP.ND}{\left(1 + 2\exp\left[\frac{NLVHOP.SIGMA}{KT}\right]^2 / \left(\exp\left(\frac{QNLVHOP.TTDF}{KT}\right) - 1\right)\right)}$$

The use of this model requires accurate fitting of the different coefficients and solving the driving force F. Additionally, since this model involves more complex calculations using quantum meshing, the simulation time increases drastically, especially for thick devices.

Using the described models, we will present a comprehensive study of vertical GaN-on-Silicon devices, including:

- A benchmark of Schottky and P-I-N diodes performances.
- Understanding the impact of different parameters on the P-I-N diode.
- Comparison of fully vertical and pseudo-vertical device behavior.
- Study of the mesa depth impact on the device performance.

2.2 Benchmark of Schottky and P-I-N diode performances

The choice of the device type is crucial in power electronics and depends on the specific application. In this work, we aim to develop 1200 V class diodes. Two structures are simulated based on a:

- Schottky diode structure (Figure 2-4.a) : 800 nm thick N^+ layer with a doping of 5×10^{18} cm^{-3}, and 4.5 µm thick drift region with an N-doping of 1×10^{16} cm^{-3}.
- PIN diode structure (Figure 2-5.b) : 800 nm thick N^+ layer with a doping of 5×10^{18} cm^{-3}, and 4.5 µm thick drift region with an N-doping of 1×10^{16} cm^{-3} and 700 nm thick P-layer with a doping of 3×10^{17} cm^{-3}.

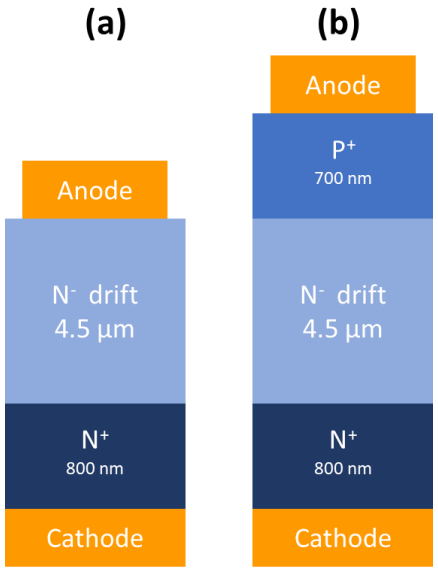


Figure 2-4 : Simulated structures using Silvaco of (a) SBD Schottky diodes (b) PIN diodes

In the case of the Schottky diode, the electric field in reverse condition is located at the interface between the Schottky contact and the semiconductor, which means directly on the surface (Figure 2-5). In contrast, the electric field peak in the P-I-N diode is buried inside the junction (Figure 2-6). The vertical cross-section illustrates the electric field distribution for both Schottky and P-I-N diodes at -200 V. The difference in the electric field peak is clear and thus shows that the P-I-N diode is capable of delivering a higher breakdown voltage owing to the electric field confinement within the junction. Moreover, the leakage current of the P-I-N diode is lower because the junction maintains a natural barrier via the depletion region, unlike the barrier created by the Schottky metal.

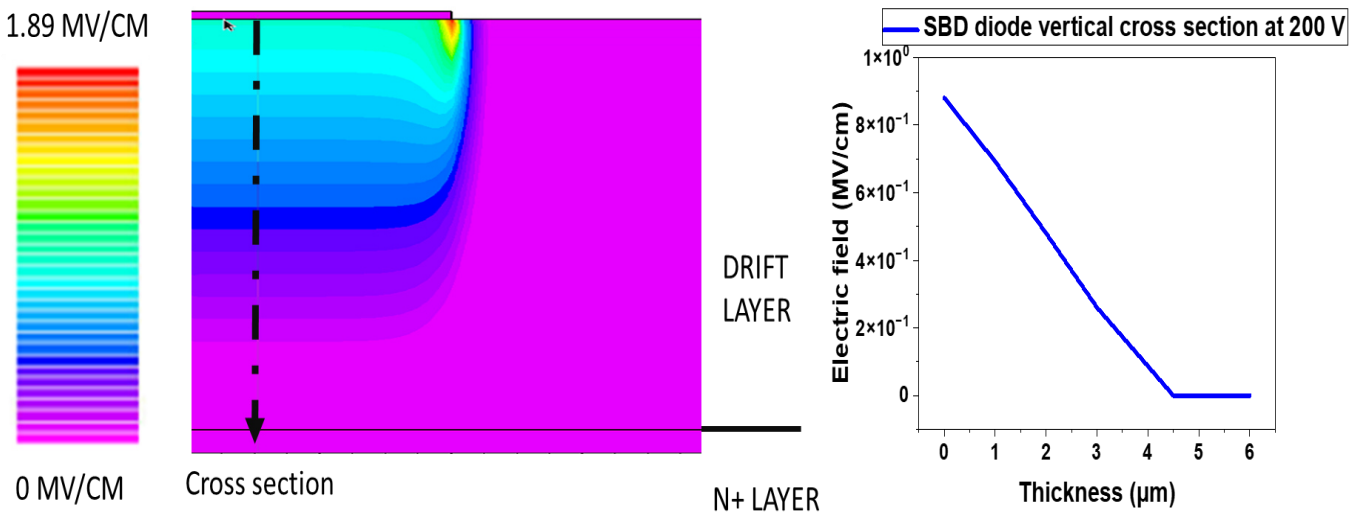


Figure 2-5 : Distribution and cross section of a Schottky diode electric field at -200 V

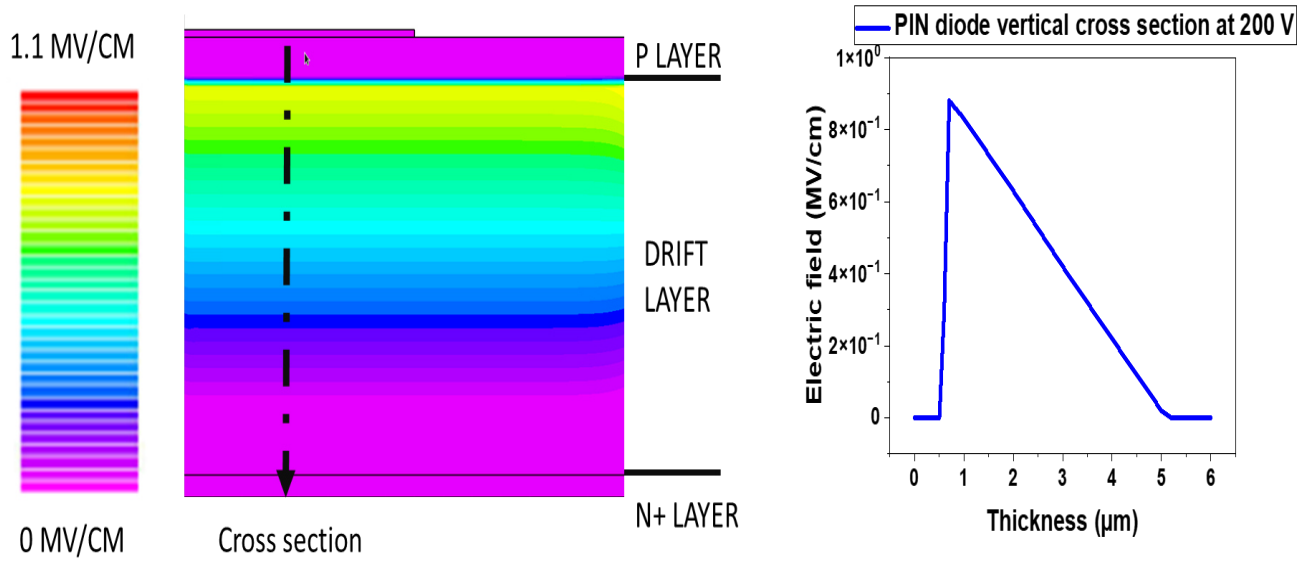


Figure 2-6 : Distribution and cross section of a PIN diode electric field at -200 V

2.3 Comparison of fully vertical and pseudo vertical PIN diodes

The vertical structure relies on doping layers to achieve high and reliable performance, including avalanche capability. There are two possible design options :

- Pseudo-vertical design (Figure 2-7.a): In this case, the bottom layer is accessed from the front side. This design is the most commonly reported in the literature.
- Fully vertical design (Figure 2-7.b): more challenging to achieve due to backside process complexity and device fragility.

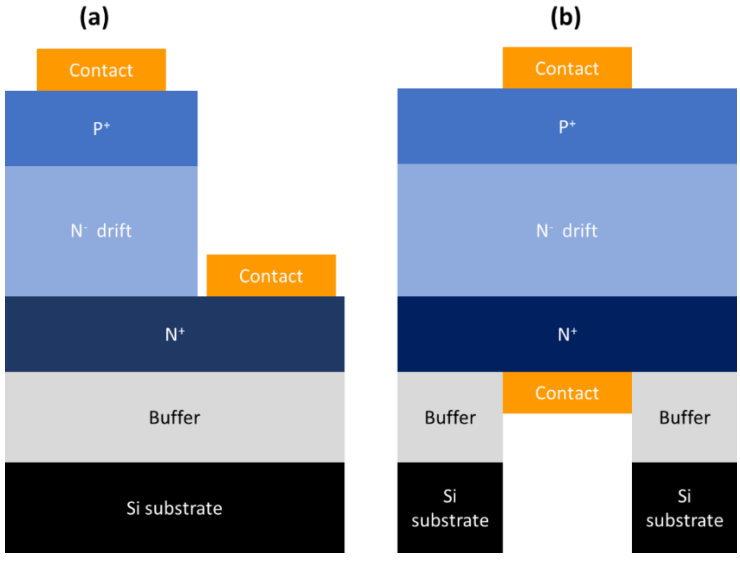


Figure 2-7 : (a) pseudo vertical and (b) fully vertical GaN on Silicon PIN diode

Even though the process of the pseudo-vertical design is easier, the related on-state behavior is a significant drawback. In the pseudo-vertical structure, the current crowds at the edge of the N+ layer, adding additional resistance [22], [89], [105] Figure 2-12. Figure 2-8 shows the current density distribution in a pseudo-vertical P-I-N diode at +10 V, indicating the crowding effect of charge carriers. The current flows vertically until it reaches the N+ layer, where it changes direction to a lateral flow. This crowding effect affects the on-state performance and depends on the anode size.

Figure 2-9 shows the current distribution of a pseudo-vertical P-I-N diode with different anode areas at +10 V. For larger anode areas, the current is not uniformly distributed anymore below the contact. This directly impacts the Ron; which increases with the anode area (Figure 2-10). This is explained by the crowding of charge carriers on the N+ layer, creating a critical length below the contact (see Figure 2-8). The contact needs to be smaller than this critical length. The crowding effect also enhances the thermal dissipation issues through the device.

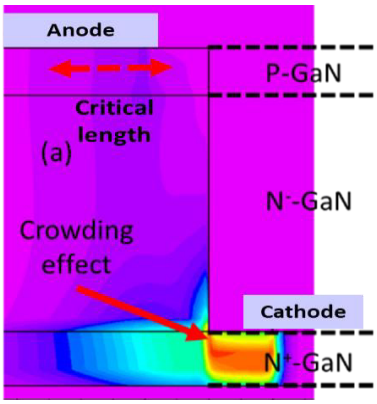


Figure 2-8 : Current distribution of a pseudo vertical PIN diode at +10 V

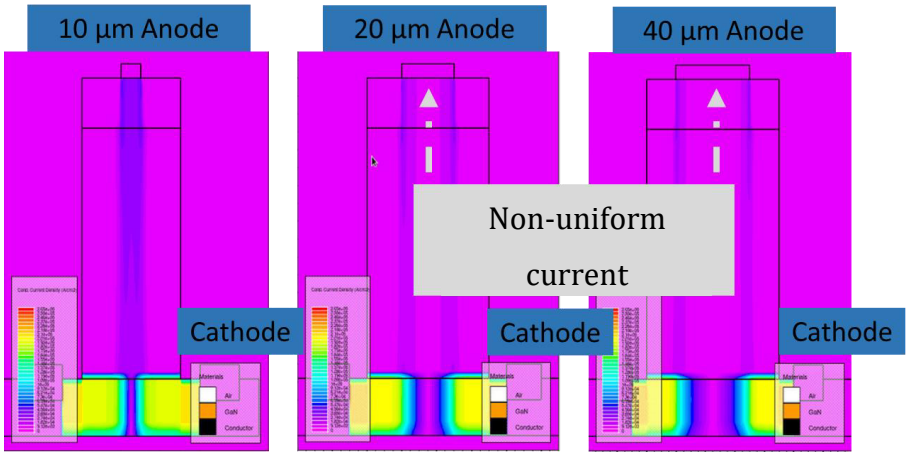


Figure 2-9 : TCAD simulation of current distribution at +10 V vs different anode sizes

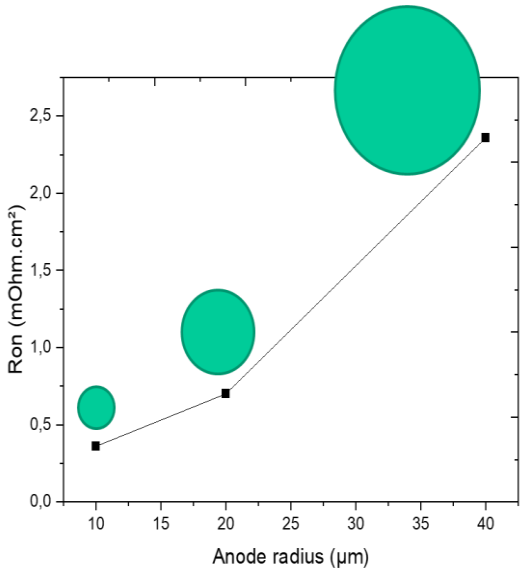


Figure 2-10 : Ron vs anode radius of pseudo vertical PIN diodes

The additional series resistance (Figure 2-12) is affecting the Ron by two factors: the change in the current transport direction and the anode-cathode distance. In this frame, we carried out some simulation of pseudo-vertical P-I-N diodes with an anode diameter fixed to 30 µm and two different mesa diameters (70 µm, and 50 µm). It can be pointed out that the anode diameter is used for the normalization of Ron (on-state resistance) and J (current density). By decreasing the mesa size from 70 µm to 50 µm, Ron decreases (Figure 2-11). This is attributed to the reduction of the lateral transport distance in the N+ layer. Consequently, this parameter should be taken into account in the extraction of Ron in pseudo-vertical structures, as it can impact the device's capability to spread the current and thus achieve low Ron.

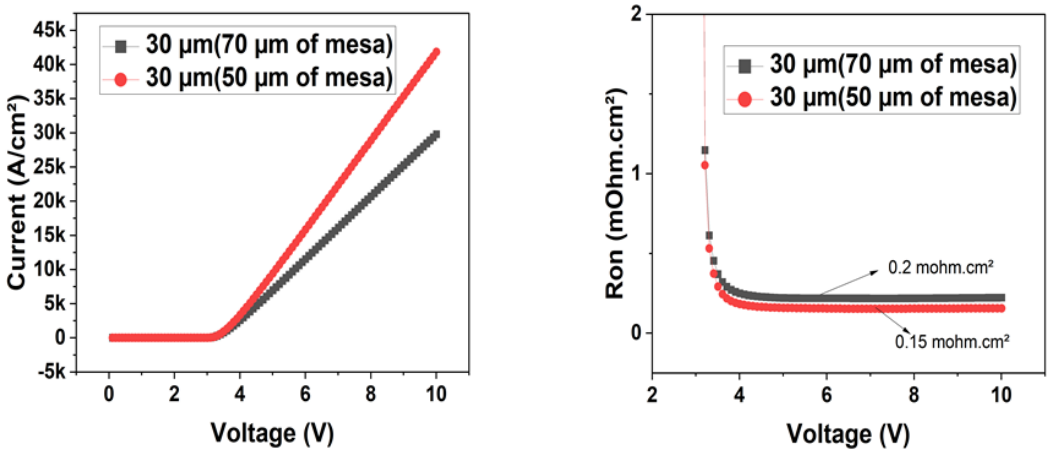


Figure 2-11 : Extracted J(V) and Ron(V) from TCAD simulation of pseudo vertical PIN diodes using two mesa diameters

The Ron limitation of the pseudo-vertical structure reduces the attractiveness of this design for vertical power electronics. The use of large devices is indeed essential to generate high current. Figure 2-13 shows that in more than 80% below the contact area, the current is not flowing in the case of pseudo-vertical diodes with large anode sizes. In contrast, for the same structure mentioned before, the fully vertical P-I-N diode exhibits a uniform current distribution (at +10 V) below the contact toward the N+ layer. That is why, developing fully vertical architecture is essential to unlocking the full potential of vertical GaN devices. However, due to the simplicity of pseudo-vertical fabrication process, small diodes (< 20 µm) can be used as a short-loop vehicle test to quickly evaluate the device performance.

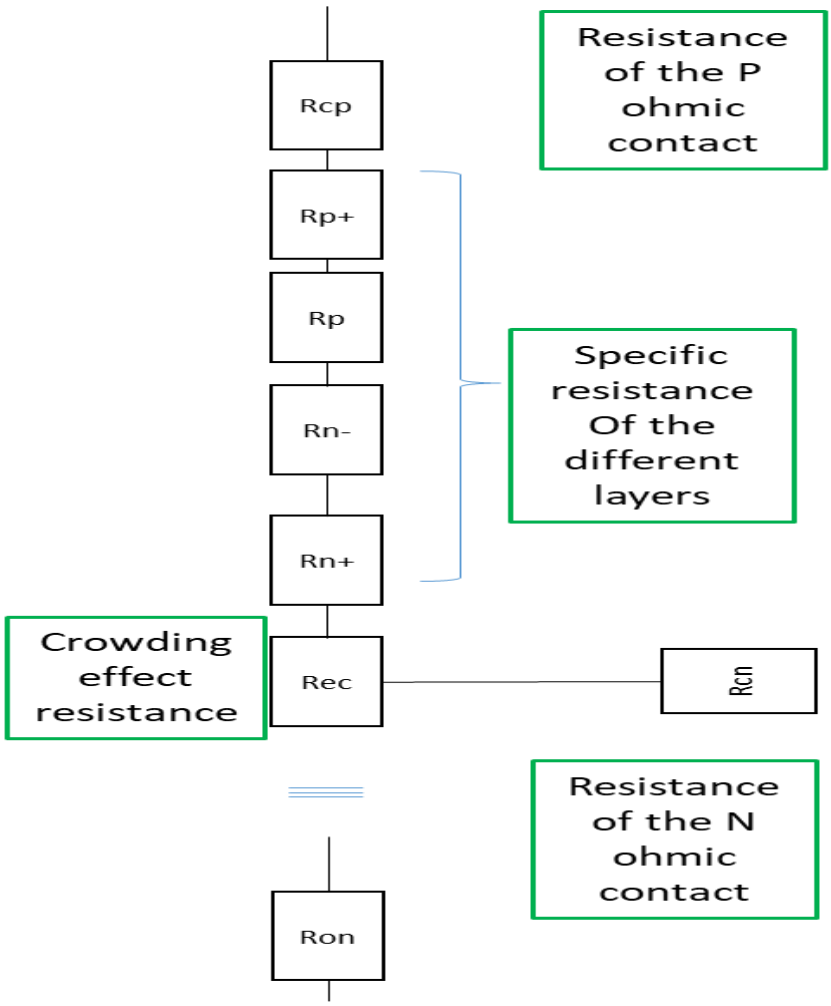


Figure 2-12 : Serial resistances of pseudo vertical diodes

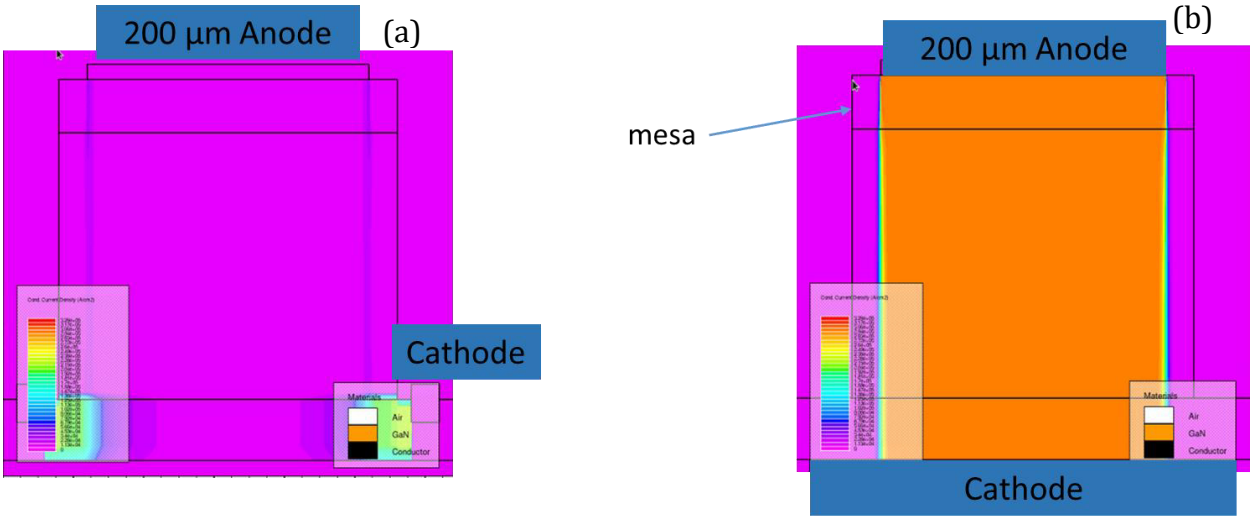


Figure 2-13 : Current distribution of large diode size (200 µm) with (a) pseudo vertical and (b) fully vertical configuration at +10 V forward bias

2.4 Optimization of vertical GaN-on-silicon PIN diode design

In this section, the different epilayers and the critical edge termination process step of P-I-N diodes are analyzed with respect to both on-state and off-state performance with the aim of achieving the goal of 1200 V class diodes.

2.4.1 P layer

The P layer in P-I-N diodes plays a crucial role in the overall device performance. When forward current flows, the P layer injects holes into the drift region, enhancing recombination of charge carriers and reducing the forward voltage drop. Under reverse bias, this layer forms a wide depletion region with the drift region, aiding in the blocking capability of the device. This can only be maintained if the doping concentration of the P layer is much higher than that of the drift region. In this case, the depletion region is fully formed in the drift region, pushing the electric field far from the surface, as illustrated in Figure 2-6.

The doping of the P layer is challenging due to doping activation issues. In the literature, P doping is typically in the order of 10^{17} cm^{-3}. Figure 2-14 describes the dependence of the off-state and on-state performance on P doping (using the same structure described in the last section). This parameter influences the forward current because high doping

increases the recombination rate of electron-holes (see Figure 2-14(a)) while injecting sufficient holes into the drift region.

Regarding the blocking capability, we observe a dependence of the electric field on the doping at 200 V of reverse bias (Figure 2-14(b)). Using a doping concentration greater than 1×10^{17} cm^{-3} allows for significant reduction of the electric field and an optimized field distribution in the drift region, which can be explained by the depletion of the electrical space charge region within the drift region. In the case of high P layer doping, the device has a better electric field confinement, which is beneficial in protecting the device from premature breakdown related to the proximity of the field to the surface.

To address the challenges of P doping activation, this parameter was fixed at 3×10^{17} cm^{-3} providing a good balance between the electric field confinement and on-state performance (Ron < 1 $m\Omega.cm^2$), which also complies with the experimental low active P doping characteristic of GaN,

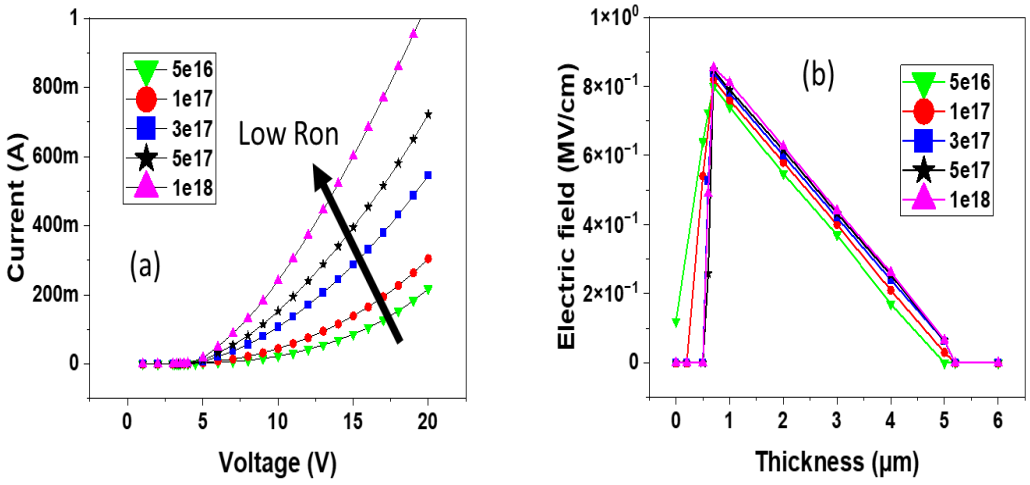


Figure 2-14 : (a) I(V) on state characteristics versus P doping (b) vertical electric field distribution versus P doping at 200 V

Since the electric field peak is located at the P-drift region junction, the thickness of the P layer must be taken into account. A thicker P layer makes the electric field further away from the surface, protecting the device from premature breakdown, as shown in Figure 2-16. For a 100 nm thickness of the P layer, the electric field reaches the surface at -200 V. It can be observed that starting from 500 nm of P layer thickness, the electric field is well confined inside the structure. However, increasing the P layer thickness could also increase the Ron of the device, as observed from the I(V) on-state curves in Figure 2-15,

which show the forward current extracted from TCAD simulation for different P layer thicknesses. The larger electron path in the thick P layer, which reduces the recombination rate, explains the increase in Ron.

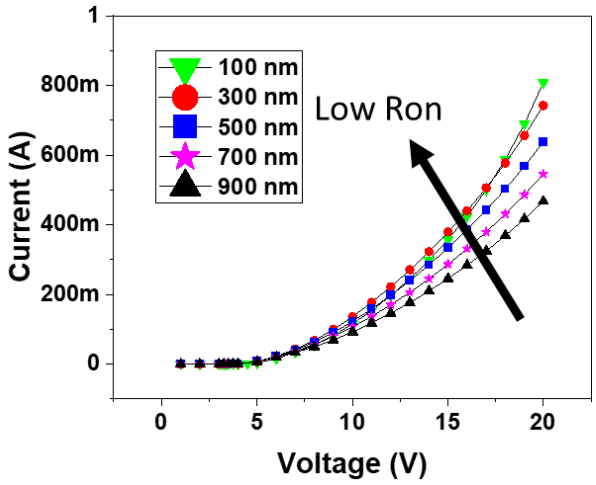


Figure 2-15 : Forward characteristics of the PIN diode with various thickness of the P.

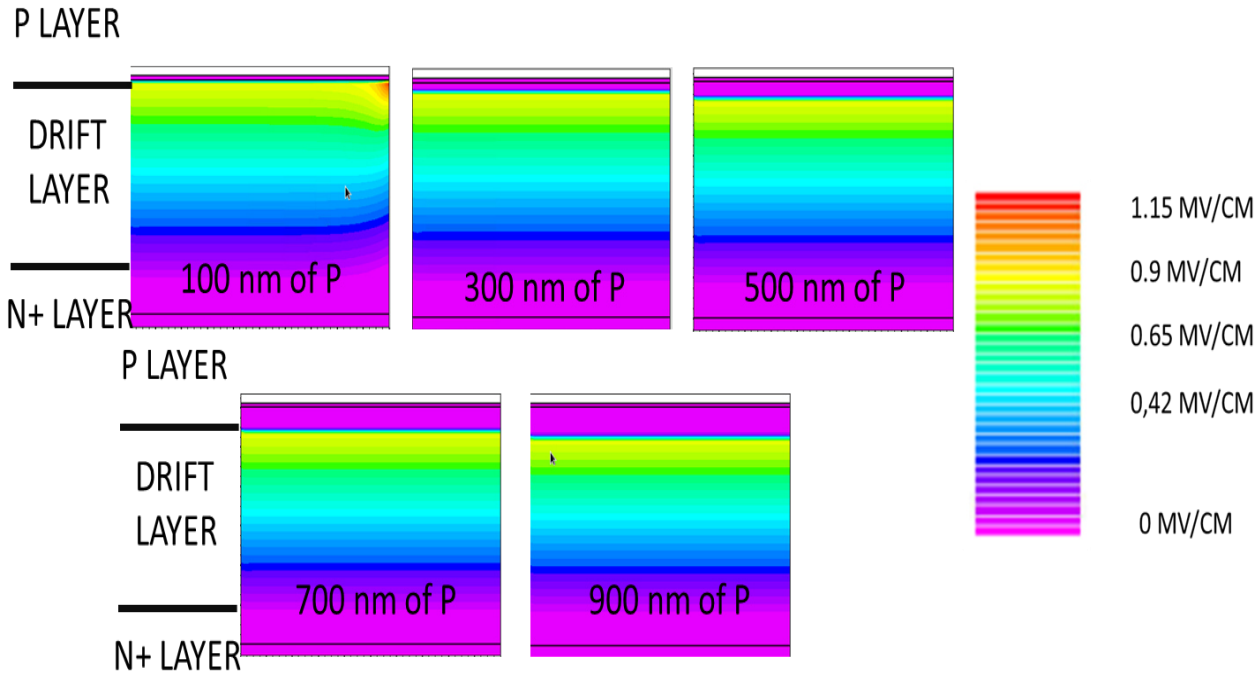


Figure 2-16 : Electric field distribution at 200 V reverse voltage for a PIN diode with various P layer thickness

As mentioned before, it is desirable to confine the electric field within the structure, away from the surface. The slight increase in Ron can be counterbalanced by the high blocking and protective capability of the thick P layer, which is particularly needed in the case of vertical GaN-on-Silicon P-I-N diodes due to the high threading dislocation density,

typically in the order of 10^{11} cm^{-2}. Therefore, for the next sections, the P layer thickness has been fixed at 700 nm with a doping concentration of 3×10^{17} cm^{-3}

2.4.2 N^- drift layer

Another essential layer of the P-I-N diode is the drift region, which separates the highly N and P type doped layers. This region confines and withstands the high electric field due to the depletion region that gradually extends through the thickness of this layer. Additionally, this region affects the current spreading capability, as it needs to be generally lightly doped. In this part, we will study the impact of drift region doping and thickness on the device performance using the same structure described previously.

The drift region should be lightly doped to meet two criteria:

- Allowing significant current spreading in on-state condition.
- Blocking the leakage current using the depletion region created with the P layer in off-state.

Figure 2-17 shows the I(V) curve of a P-I-N diode (using the same structure described previously) for different drift region doping levels. It can be clearly seen that higher doping of the drift region reduces Ron. This is due to the higher number of donors, which play an important role in the recombination rate of electron-hole pairs. However, high doping levels in the drift region induce a depletion zone on both sides (in the P and N- layers), altering the profile of the electric field distribution. Instead of a fully depleted region in the drift region (when Na >> Nd), high doping of this layer (when Nd = Na) results in a depletion zone in the P layer, pushing the electric field towards the surface and resulting in lower breakdown voltage. Figure 2-18 illustrates the impact of the drift region doping on the electric field distribution (extracted at 200 V reverse voltage). For a doping concentration of 1×10^{17} cm^{-3}, the electric field is almost entirely confined in the P/drift junction, with a high electric field peak (> 2 MV/cm) following a triangular distribution towards the surface along the drift layer. By decreasing the doping, the electric field starts to spread more gradually in the drift region while reducing the electric field peak, reaching 0.6 MV/cm in the case of a 5×10^{15} cm^{-3} doping with a trapezoidal distribution.

The best doping trade-off of the drift region was found to be in the order of 1×10^{16} cm^{-3}, which allows high blocking capability while correctly spreading the current.

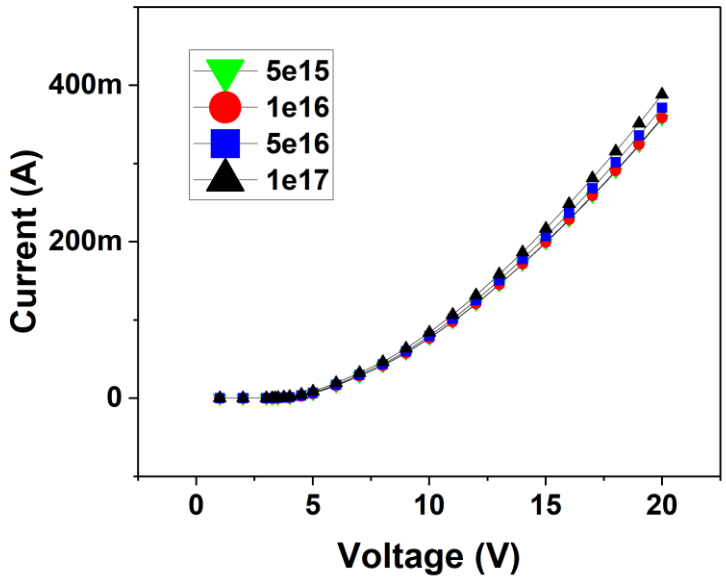


Figure 2-17 : Forward characteristics of PIN diodes versus drift region doping variation

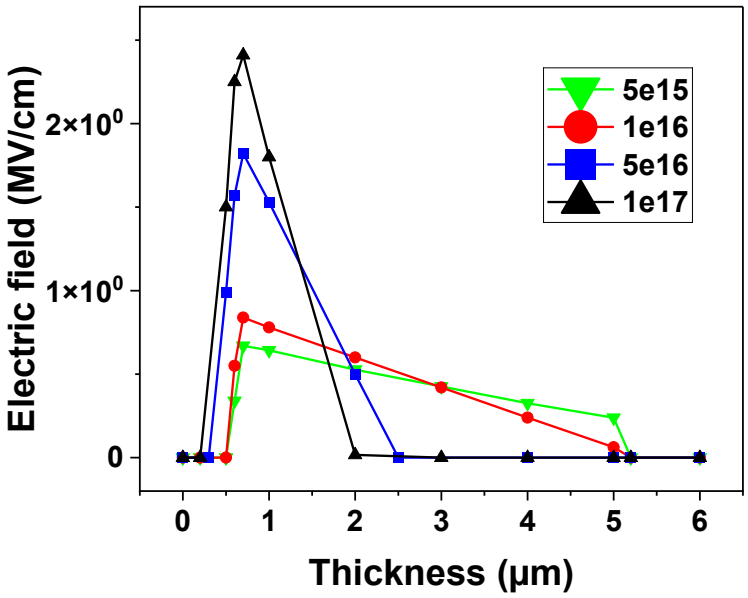


Figure 2-18 : Electric field vertical cross section distribution versus drift region doping

The thickness of the drift region is the driving force of vertical GaN-on-Si power device blocking voltage. Using the previous structure with a fixed doping concentration for the drift region, TCAD simulation was used to study the impact of varying the drift region thickness on both forward current and reverse mode performance.

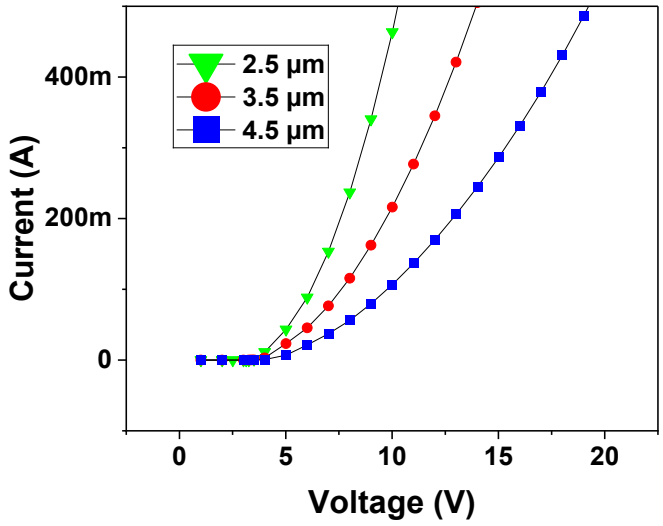


Figure 2-19 : Forward characteristics of PIN diodes with different drift region thickness

In on-state, a thinner drift layer allows for a reduction in Ron, which can be explained by the shortened electron path from the N+ layer to the P layer. This effect can be observed in the case of a drift region thickness of 3.5 µm, which has a better I(V) slope than a 4.5 µm drift region (Figure 2-19). The electric field profiles of various PIN diode drift region thicknesses were extracted at 200 V bias from both the P/drift and drift/N+ junctions (see Figure 2-20 (a)). At 200 V reverse bias, the thinner drift region thicknesses (< 3.5 µm) exhibit two electric field peaks at the junctions. Conversely, thicker drift regions show only one similar peak of the electric field at the P/drift junction.

Figure 2-20 (b) illustrates the evolution of the breakdown voltage (extracted at 10 µA) versus the drift region thickness. To achieve the target of 1200 V, it is essential to use a thick drift region (> 7.5 µm) with low doping (1×10^{16} cm-3), while maintaining a P doping of 3×10^{17} cm^{-3} with a thickness of 700 nm.

Figure 2-21 highlights the evolution of the electric field in a PIN diode using a 7.5 µm drift region thickness. At low reverse bias, an electric field peak appears at the P/drift junction, noticeable from the 50 V case. As the bias increases from 50 V to 400 V, the electric field spreads within the drift region towards the N+ junction. Beyond this voltage, a significant leakage current appears due to the electric field distribution close to the N+ layer. This is even more pronounced at 600 V (see Figure 2-20.b) while the drift region becomes fully depleted. At higher reverse voltage (> 1000 V), the electric field peak further increases at

both P/drift and drift/N+ junctions until reaching a critical electric field leading to two potential outcomes:

- ❖ A sudden increase in current without damaging the device, indicative of a soft breakdown.
- ❖ Destructive breakdown causing harmful damages to the device.

In theory, GaN PIN diodes are expected to exhibit soft breakdown due to their avalanche capability, as discussed earlier. However, factors such as process fabrication and material quality can influence the avalanche breakdown, potentially leading to hard breakdown of the device. This aspect will be explored further in subsequent chapters.

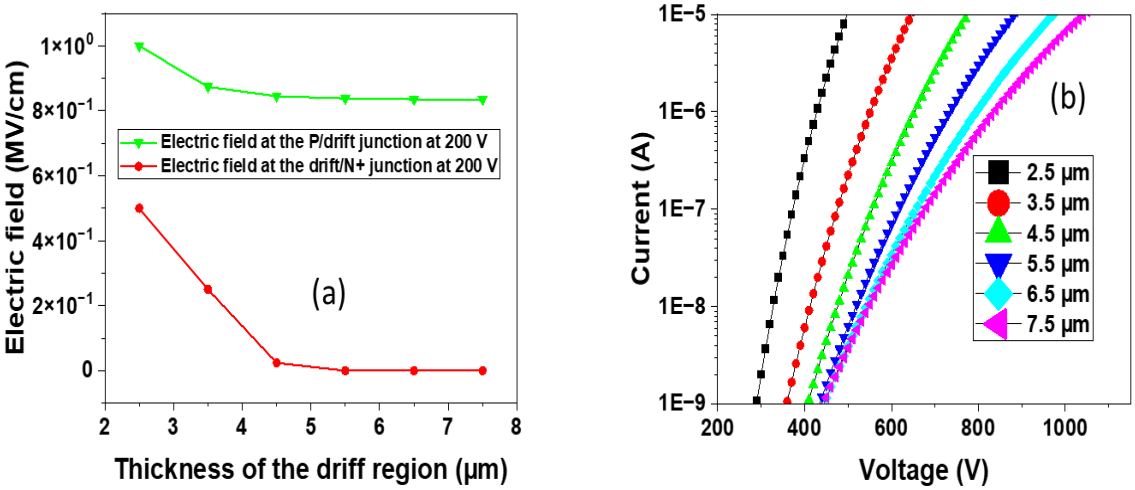


Figure 2-20 : (a) Electric field peak at the junction of the Pin diodes versus the drift region thickness (b) TCAD simulation of the I(V) curves in the reverse bias condition

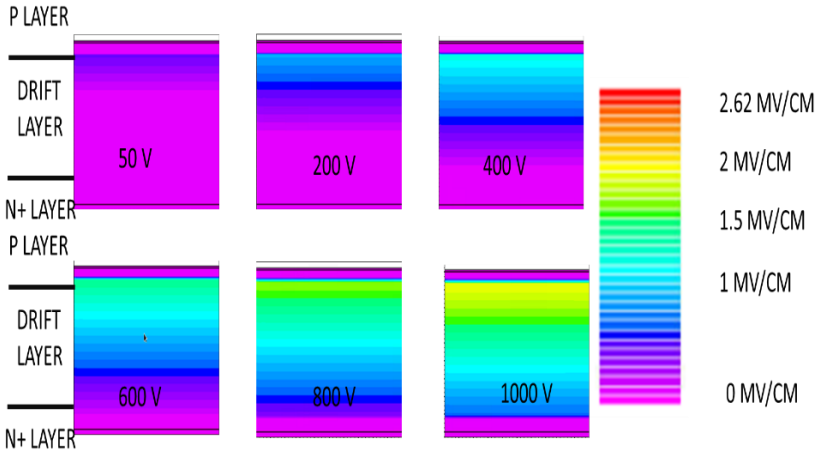


Figure 2-21 : Evolution of the electric field distribution for a PIN diode using a 7.5 µm drift layer thickness for various reverse bias (from 50 V to 1000 V)

2.4.3 N^+ layer

The bottom N+ layer enables the backside contact. This layer is the source of electron that will be injected in the drift layer. In reverse bias, the doping (> 1×10^{18} cm^{-3}) and the thickness have no impact on the electric field (see Figure 2-22). This indicates a non-dependence of the PiN diode off-state behavior on the bottom N+ layer.

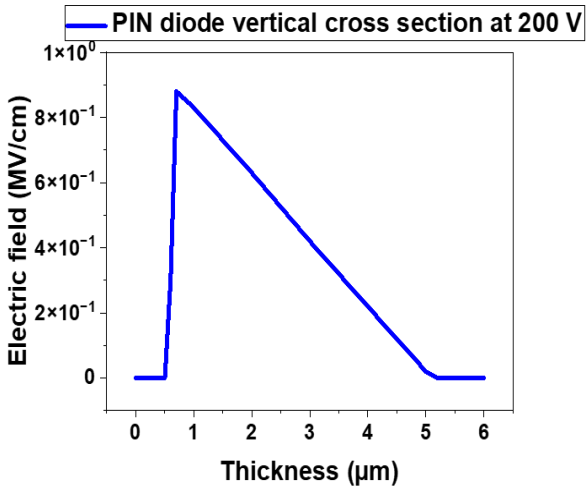


Figure 2-22 : Vertical cross section of the electric field for a variation of the N+ parameters

Figure 2-23.a shows the forward characteristics of the diode with various N+ layer doping (thickness = 800 nm). As can be observed, higher N+ doping enhances the current spreading of the device and decrease the Ron thanks to the increased electron concentration. The doping concentration is fixed to 5×10^{18} cm^{-3} in order to avoid defects during the growth when using excessive doping level approaching 1×10^{19} cm^{-3}.

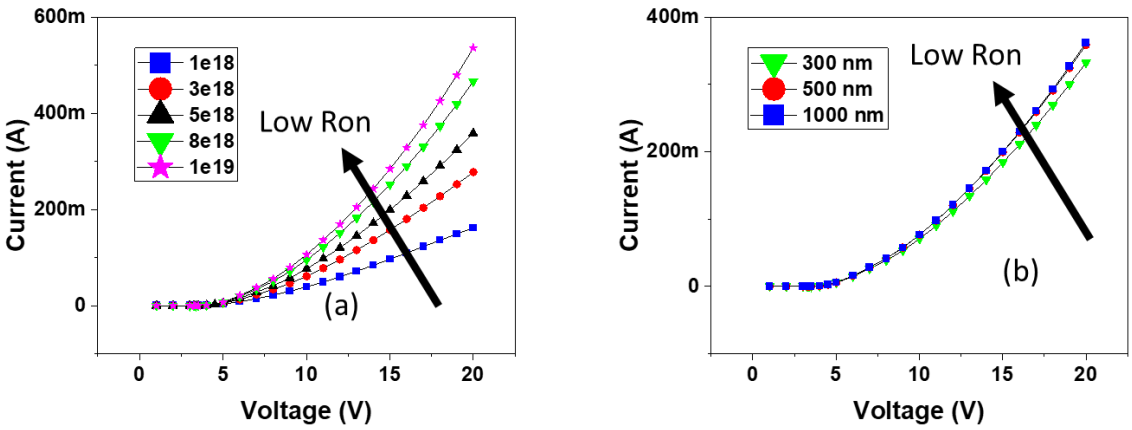


Figure 2-23 : Forward characteristics versus N+ layer doping (a) and versus N+ layer thickness (b)

Figure 2-23.b presents the forward characteristics of PIN diodes with various N+ thickness (doping = 5×10^{18} cm^{-3}). Rather similar on-state characteristics have been extracted resulting in an identical Ron for the various N+ thickness. This figure indicates that the N+ layer thickness has no impact on the on-state behavior, which is beneficial for the growth of vertical GaN-on-Silicon. Indeed, lower N+ thickness can be used and thus less contribute to the total epi-thickness limited by strain issues.

2.5 Edge termination design for fully vertical GaN-on-Silicon PIN diodes

For high voltage applications, the interaction of devices with the environment must be taken in account. In particular, a critical edge peak appears under reverse bias, which is called edge termination. This termination can be managed following several methods such as implantation, mesa, passivation…

To optimize the edge termination design, TCAD simulations were conducted on vertical PIN diodes using Silvaco. In this study (Figure 2-24), a mesa with a 75° negative bevel was employed, known to enhance breakdown voltage by alleviating electric field crowding [54]. As shown in references [102], [106], [107], [108], the bevelled mesa allows more uniform and stable breakdown voltage.

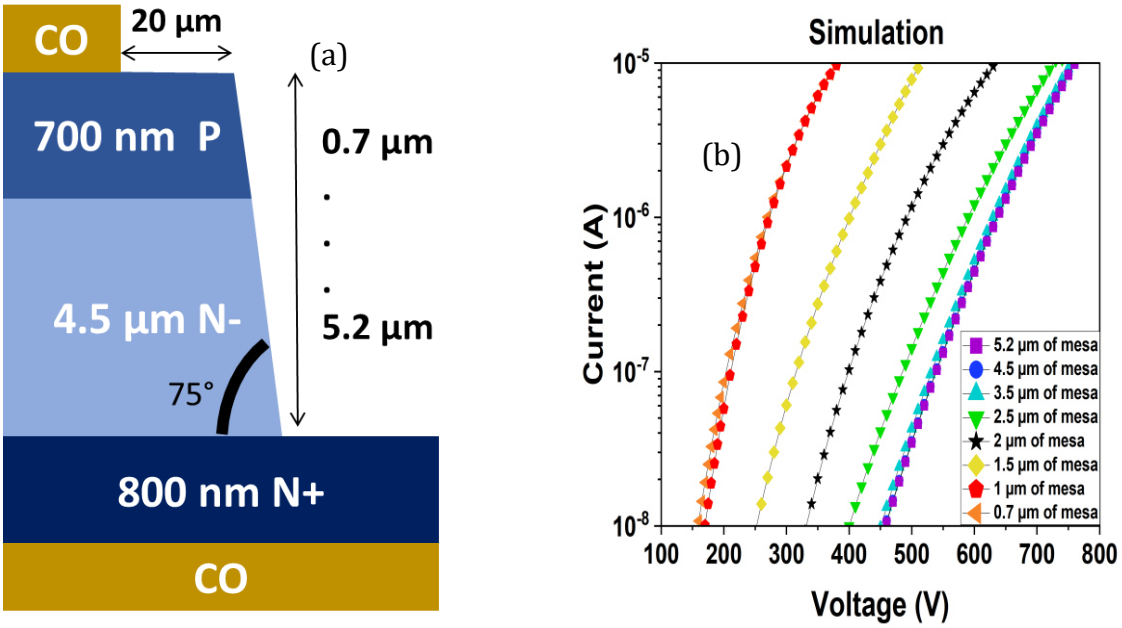


Figure 2-24 : (a) Vertical PIN diode design with different mesa depth (b) reverse leakage current vs mesa depth

Various mesa depths were evaluated (0.7 µm, 1 µm, 1.5 µm, 2 µm, 2.5 µm, 3.5 µm, 4.5 µm, and 5.2 µm), revealing a significant decrease in leakage current when the mesa depth is

increased up to 2.5 µm. The blocking voltage is clearly enhanced at 10 µA as the current flow is prevented for deeper mesa (see Figure 2-25). For mesa depths below 2.5 µm, the sidewall residual leakage creates a path leading to increased leakage currents. Specifically, at 10 µA leakage current, the peak electric field within the PIN diode occurs between the P and N- layers, contributing to sidewall leakage when the mesa depth is too close to this peak (Figure 2-26). Consequently, this configuration results in a lower breakdown voltage (defined as 10 µA of leakage current), observed to be below 640 V for shallow mesa depths. Conversely, with a deep mesa depth (i.e. 5.2 µm), the breakdown voltage was enhanced, reaching 760 V in this case.

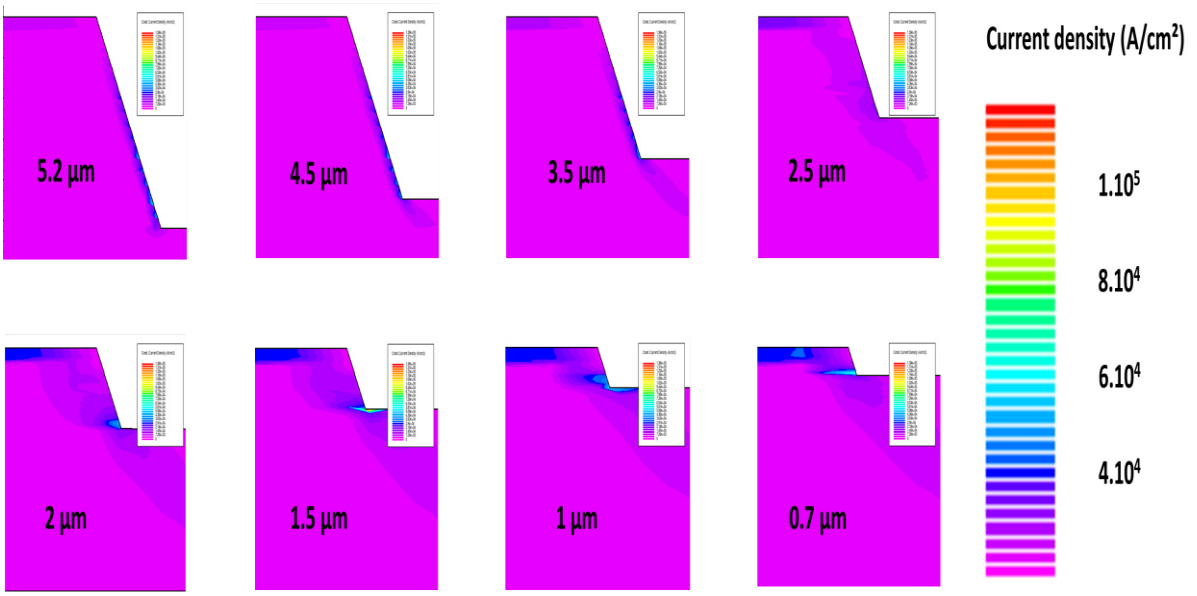


Figure 2-25 : Current density distribution at 10-µA leakage current vs mesa depth

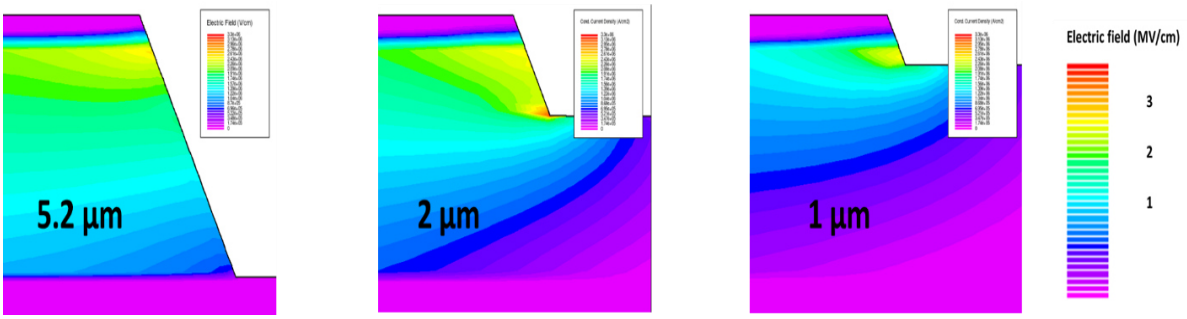


Figure 2-26 : Electric field distribution at 10 µA leakage current of 5.2 µA (760 V), 2 µA (640 V) and 1 µm (370 V)

In addition to affecting leakage current, mesa depth also significantly impacts the peak electric field, a critical parameter to prevent early and destructive breakdown in GaN-based devices. Figure 2-27 illustrates the electric field distribution of vertical PIN diodes with varying the mesa depth. For mesa depths below 2 µm, there is a noticeable high electric field peak at the mesa edge (> 3 MV/cm), which can definitely damage GaN devices. However, as the mesa depth increases beyond 2.5 µm, the peak electric field at the edge decreases significantly from 2.5 MV/cm for a mesa depth of 2.5 µm to less than 0.5 MV/cm for a mesa depth of 5.2 µm. This reduction demonstrates the benefits of deeper mesas as edge terminations for fully vertical GaN-on-Silicon PIN diodes, effectively enhancing device robustness against premature breakdown issues.

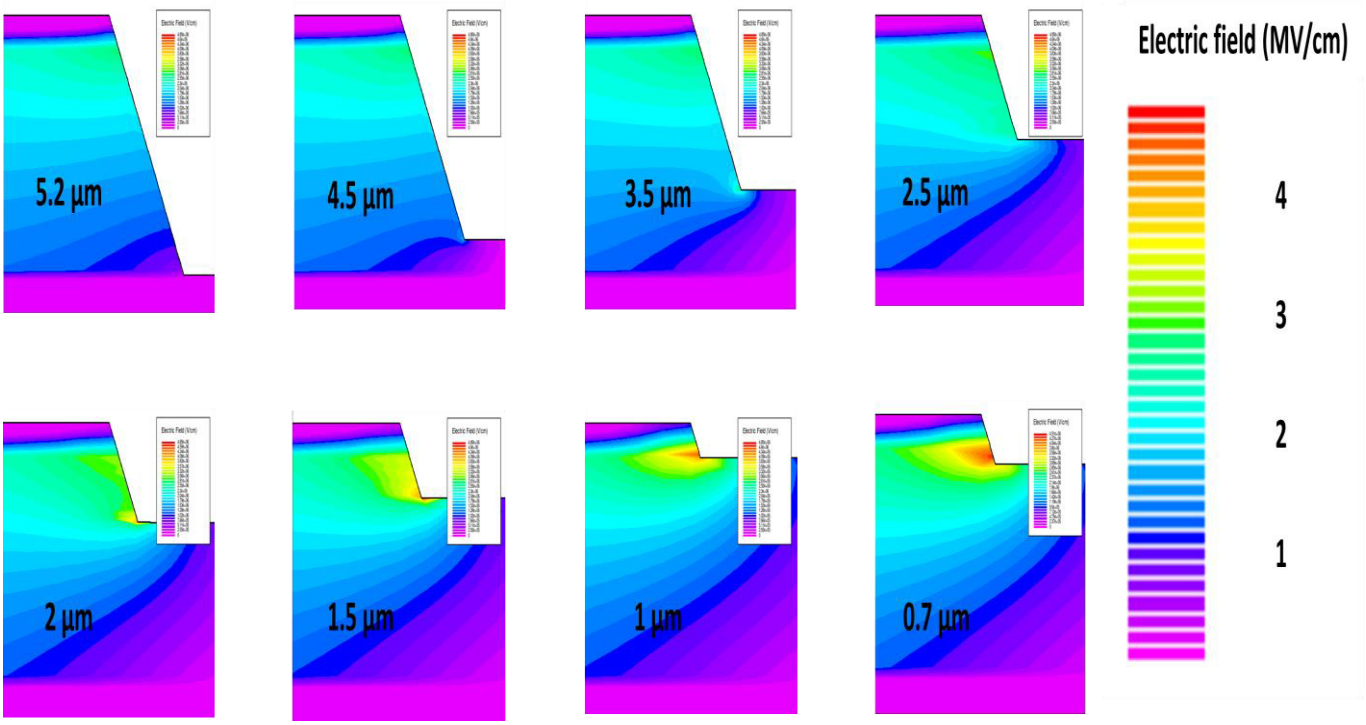


Figure 2-27 : Electric field distribution at 820 V of different mesa depth

2.6 Conclusion

In this chapter, we studied and optimized the parameters of the vertical GaN PIN diode with the aim of achieving 1200 V class diodes. The drift region thickness was determined to be critical, requiring a thickness of about 7.5 µm with a doping level around 1×10^{16} cm^{-3} for optimal performance. The doping of the P top layer, starting from 3×10^{16} cm^{-3}, plays a crucial role by ensuring the electric field peak to be kept

away from the surface and minimizing reverse bias leakage current. The N+ layer with a doping above 1×10^{18} cm^{-3} facilitates efficient electron injection into the drift region, crucial for enhancing the forward current performance.

From a structural perspective, our studies demonstrated that fully vertical GaN PiN diodes exhibit superior on-state performance compared to a pseudo-vertical design. Additionally, optimizing mesa depth effectively reduces the edge electric field, contributing to improved breakdown characteristics.

While this chapter focused on the theoretical aspects of the vertical PiN diodes, the experimental fabrication of thick, fully vertical GaN-on-Silicon PIN diodes with deep mesa presents practical challenges. The next chapter will address these challenges by presenting a process flow and optimizing material quality to achieve these demanding device specifications.

Chapter 3: Vertical GaN-on-Silicon Power devices process development

3.1 Introduction :

This chapter presents our process development of vertical GaN-on-Silicon power devices targeting state of the art performances and high figure of merit. We will focus on the fabrication of vertical GaN-on-Silicon diodes. From the previous section, we have concluded that the use of an optimized PiN diode with a thick drift region is essential to reach the 1200 V class. This need to be combined with the use of a fully vertical design and deep mesa etching as edge termination to unlock the complete capability of this technology including high current spreading (low Ron) mainly dependent on the device size as well as the avalanche capability.

From a practical point of view, the development of vertical GaN on Silicon PIN diode with the desirable performances is challenging due to two factors: the growth quality and the process fabrication :

The growth is generally carried out by Metal Organic Chemical Capor Deposition (MOCVD) that needed to be optimized to reduce the threading dislocation density, which increases the leakage current in reverse bias condition, and to alleviate the strain, in particular when growing thick layers. The growth optimization can be achieved by using specific buffer configurations, controlling the impurity concentration (low Carbon and hydrogen concentration) and accurately fixing the active doping (especially for the P doping of GaN).

The process quality is critical for the device performances as steps need to be carefully optimized. Depending on the targeted architecture, several challenges need to be addressed. In general, the process must:

- not induce any damage affecting the device performances.
- Ensure appropriate thermal management.
- Preservethe high reliability of the devices.

In this chapter, we will present an optimization of the fabrication process flow for vertical GaN-on-Silicon diodes. We will start by describing the targeted structures and

defining each process steps. An overview of the number of processed samples will be also presented.

3.2 Targeted structure

3.2.1 Pseudo vertical GaN-on-Si diodes

Figure 3-1 presents a schematic cross section of the pseudo vertical PiN diode. As mentioned in chapter 2, this structure suffers from the crowding effect that damages the Ron especially for large anode area. However, this design can be used as a short loop process to extract the device performances. In the case of diodes, two contacts need to be formed: the cathode on the N+ layer and the anode on the top layer (P-GaN in the case of PIN diode or drift region in the case of Schottky diode). To form the cathode on the N+ layer, an etching step is needed to access this bottom layer. The deep mesa etching serves simultaneously as edge termination of the devices. In pseudo vertical GaN-on-Si diodes, the process is mainly carried out on the front side of the wafer, which has a Ga-face orientation.

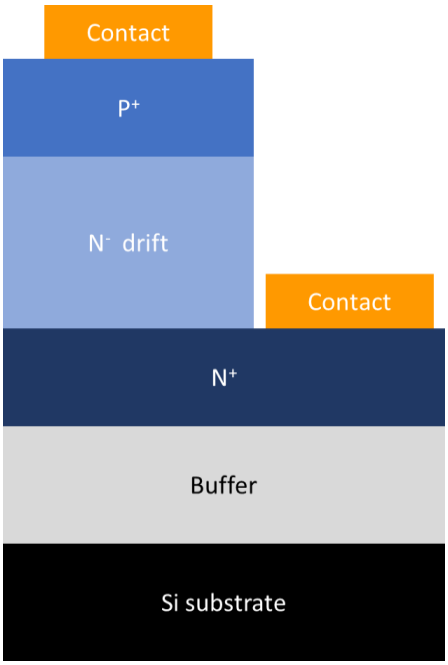


Figure 3-1 : pseudo vertical GaN-on-Si PiN diode

To summarize, the basic process of the pseudo vertical design contains three steps:

- Mesa etching
- N+ bottom ohmic contact
- P top ohmic contact

3.2.2 Fully vertical GaN-on-Silicon PIN diode

Figure 3-2 present the schematic cross section of the fully vertical GaN on Si PiN diode. This design potentially deliver superior performance compared to the pseudo vertical design (as seen in TCAD study). In this design the anode is contacted on top layer from the font side and the cathode on the N+ bottom layer from the backside, which implies two blocks of frontside and backside processing. Concerning the front side processing the contact is deposited on the top layer and the deep mesa is added as edge termination. From the backside, the silicon substrate and buffer are locally removed then the backside contact is formed.

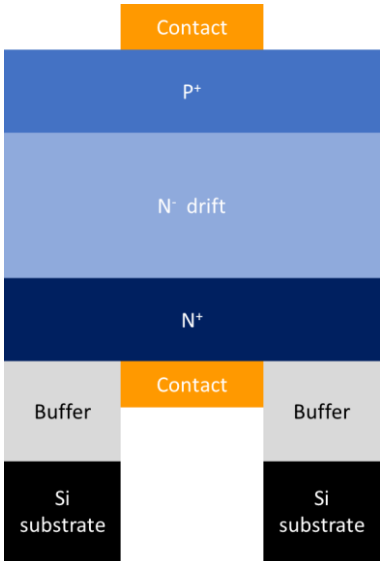


Figure 3-2 : Schematic of a fully vertical GaN-on-Si PiN diode

To summarize, the process of the fully vertical design contains two steps for the frontside:

- Mesa (edge termination)
- P type ohmic contact

And two steps for the backside :

- Silicon substrate and buffer local removal
- N+ backside ohmic contact

It can be pointed out that the order of processing steps can be adapted between the frontside and the backside. Furthermore, the deep mesa and the silicon and buffer removal results in devices with reduced thickness, increasing fragility. Also, the backside N ohmic contact is deposited on top of the N-face polarity of the GaN layer, which has

different physical properties than Ga face. These elements have to be taken into consideration.

Overall, the pseudo vertical and the fully vertical structure share almost the same processing from the front side (P-GaN ohmic contact and mesa etching). In the next section, the processing optimization will be described through basic electrical characterization assessment with respect to the device design. The full device characterization will be described in the next chapter.

3.3 Frontside fabrication process optimization for vertical GaN-on-Silicon PIN diodes

The frontside processing combines multiple points of optimization to achieve high performances: mesa etching, ohmic contact and layout design. Furthermore, the device strengthening must be considered in the case of fully vertical structure as the resulting membranes are expected to be fragile.

3.3.1 P-type ohmic contact optimization

The P-GaN ohmic contact is a key parameter in the performances of the PiN diodes, which impact both the on-state and off-state behavior, as seen in chapter 2. These parameters depend on the activation of P-doping, the metal stack used on top and the annealing conditions.

The most widely used P-doping species for GaN is Magnesium [Mg], which is very sensitive to passivation with hydrogen. During MOCVD growth, the Hydrogen is hard to control. This requires proper growth optimization to enhance the active doping of Mg, which is generally achieved by high temperature annealing. For a given doping, the active doping typically does not exceed 1% of the nominal doping.

To form an ohmic contact to a P-type GaN layer, the metal composition should have a high work function. To obtain these specifics properties, standard metal stack can fulfill the need. The annealing and the composition of the metal stack have thus to be tuned in order to enhance the work function and reduce the contact resistances.

3.3.1.1 Metal annealing tuning

RTA annealing is a commonly used method to form the contacts without a significant increase of the work function. The Pd and Ni are known for their high work function, 5.12 eV and 5.15 eV, respectively. A metal stack of 10 nm thick Pd, 20 nm thick Ni and 30 nm thick Au [109], [110], [111], [112] with TLM pattern is deposited on top of the P-GaN layer with a doping of 5×10^{19} cm^{-3} corresponding to 3×10^{17} cm^{-3} active doping. Figure 3-3 shows the TLM measurement of the Pd/Ni/Au composition as deposited and after RTA annealing at 600°C. A poor ohmic contact quality was obtained in both cases with a high contact resistance. To generate a higher work function metal, NiO (nickel oxide) is a promising metal candidate[113]. To create this oxidation, the nickel is annealed at a high temperature in O2 environment. Using the same stack (Pd/Ni/Au), the metal was annealed at 550°C for 10 min in mixed environment of N_2 and O_2. Figure 3-3 highlights also the TLM measurement of the metal stack after this specific annealing. A high quality ohmic contact with an enhanced current (I(10V) = 2 mA) was obtained compared to both RTA and as deposited measurement (I(10V) < 500 µA). The contact resistances were thus drastically reduced thanks to the NiO oxide high work function.

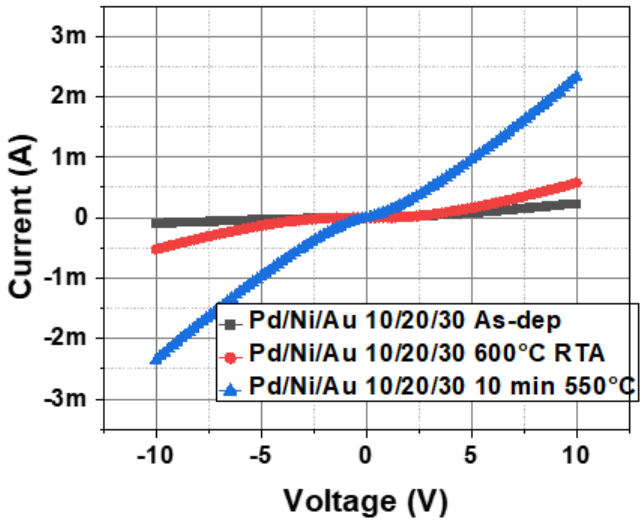


Figure 3-3 : TLM measurements of Pd/Ni/Au P-GaN ohmic contact as deposited with RTA and with 550°C for 10 min using N_2+O_2 annealing

3.3.1.2 Metal stack optimization

The NiO formation is beneficial for the reduction of P-type GaN contact resistances. However, the optimization of the metal stack is also essential. Figure 3-4 shows TLM

measurements of three different metal stacks before and after annealing (10 min at 550 °C in N_2+O_2):

- Pd(10 nm)/Ni(20 nm)/Au(30 nm)
- Pd(10 nm)/Ni(40 nm)/Au(100 nm)
- Ni(20 nm)/Au(200 nm)

By increasing the Ni and Au thicknesses, the TLM measurements show a very similar behavior as the reference metal stack. This suggests that the formation of NiO is limited by the Pd film between the P-GaN and the Ni, which may be beneficial to be removed. In the same Figure 3-4, a superior performances of Ni/Au stack with higher current, and thus lower contact resistance can be observed. The better contact quality is attributed to the formation of NiO on the top of the P-GaN [114], [115], [116], [117].

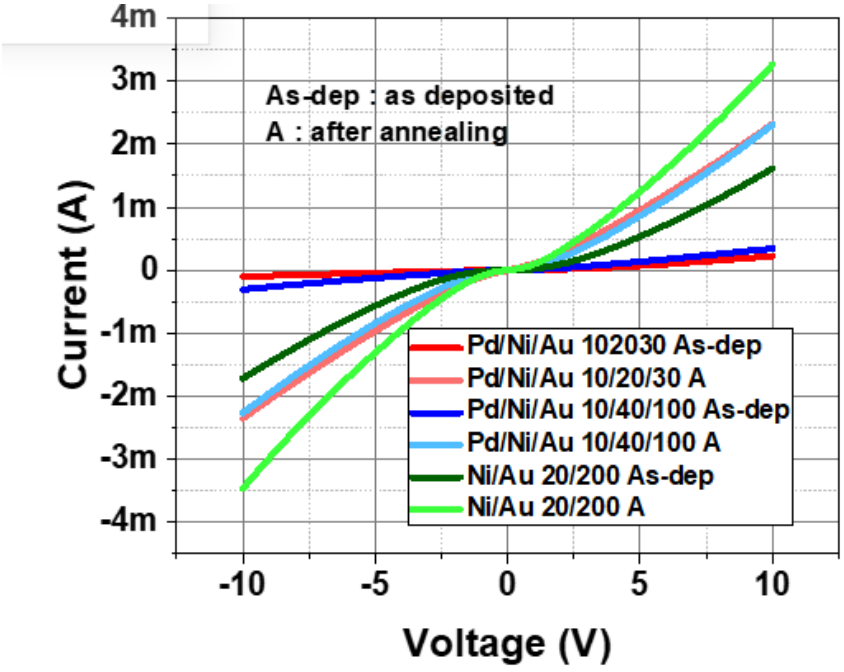


Figure 3-4 : TLM measurement of various P-GaN ohmic contact metal stack as deposited and after annealing showing the benefit of using Ni(20 nm)/Au(200 nm)

3.3.1.3 P-GaN doping and related activation

In addition to the processing conditions, the P-GaN ohmic contact quality can be enhanced with the optimization of the doping profile and activation[118], [119], [120], [121]. Table 3 show a variation of the P layer doping, thickness and activation conditions (A, B and C) in the range of 750°C-850°C (Figure 3-5.a). An additional 20 nm thick P+ highly doped

GaN layer is added on top of the P doped layer, with 10^{20} cm^{-3} of Mg concentration (sample F and H), see Figure 3-5.b.

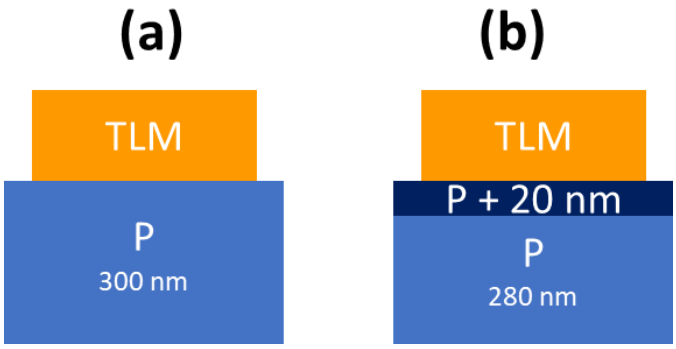


Figure 3-5 : P GaN layer thickness without (a) and without (b) the P^+ top layer.

Sample ID	P-Layer parameters	Activation condition
A (BW…751)	300 nm-2e19	C
B (BW…756)	300nm-2e19	B
C (BW…761)	300nm-8e19	A
D (BW…771)	300nm-5e19	A
E (BW…776)	300nm-2e19	A
F (BW…746)	20nm-1e20 280nm-2e19	A
H(BW…)675	20nm-1e20 280nm-2e19	B

Table 3 : P layer doping and activation with various conditions

The first comparison concerns the impact of the activation conditions on the contact resistance of 300 nm thick and 2×10^{19} cm^{-3} P doped GaN layer. Sample A, B and C have been activated using the conditions C, B and A, respectively. The activation temperatures were varied within the range of 750°C to 850°C. The specific activation parameters were not disclosed due to confidentiality requirements set by the epitaxy provider. TLM performances has been observed highlighting the impact of the activation condition using the Ni/Au metal stack. The highest TLM current and low barrier are shown by sample B with the B-activation (Figure 3-6). This condition represents the best trade-off for

activation, achieving acceptable performance at the highest temperature considered. It demonstrates the necessity for sufficient activation energy for P-doping. However, excessive activation temperatures can lead to damages of the active layer.

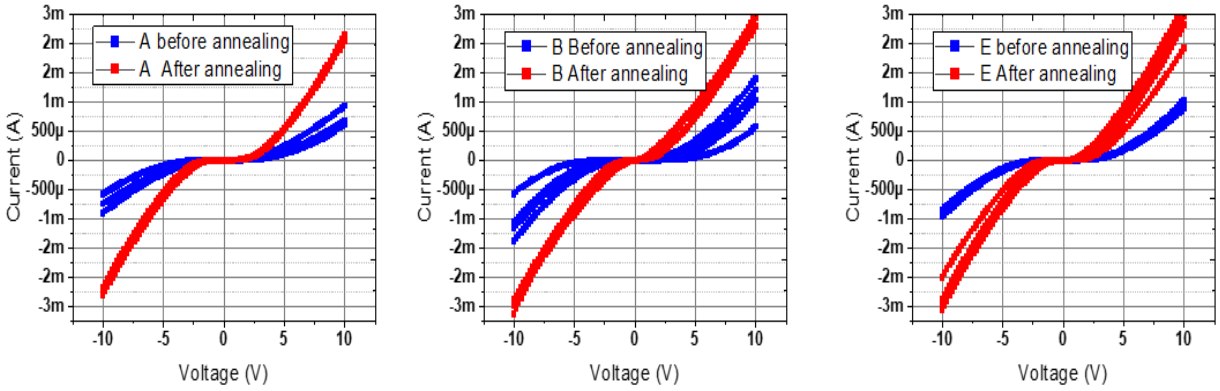


Figure 3-6 : TLM measurements of p-type ohmic contacts, deposited on 300 nm thick and 2×10¹⁹ cm⁻³ P doped GaN layer using condition A (sample E), B (sample B) and C (sample A)..

Figure 3-7 underlines the impact of adding the P+ (highly doped layer) on top of the P layer, using the optimum condition B. This comparison is performed between sample B (without the P+ layer) and H (with the P+layer). Adding the P+ layer increases drastically the current by 65% and decreases the barrier at low voltages. The increase of the active doping enabled by the additional highly doped thin film induces more minority of electrons, which is clearly beneficial to the ohmic contact quality.

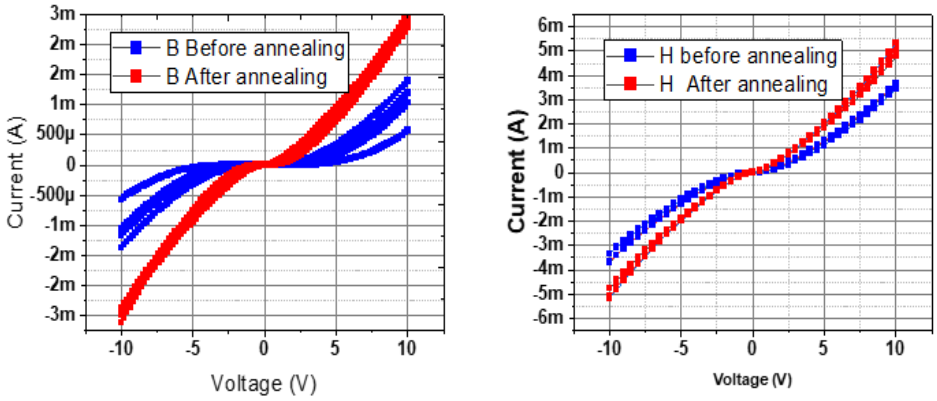


Figure 3-7 : TLM measurements of ohmic contacts, deposited on 300 nm thick and 2×10¹⁹ cm⁻³ P doped GaN layer using condition B (sample B) and deposited on 20 nm thick and 10²⁰ cm⁻³ P+ doped layer on top of 280 nm thick and 2×10¹⁹ cm⁻³ P doped GaN layers sample (H).

3.3.2 N+ Ga-face layer ohmic contact evaluation

The Ron of the devices depends mainly on the injected electrons from the N+ towards the drift region. In the case of the pseudo vertical design, the N+ is contacted from the frontside (Ga-face) after mesa etching. In general, the ohmic contact of such a layer is quite straightforward to obtain thanks to the low work function, the high active doping of this layer and the simple formation of Ti-N bound with annealing. Ti(12 nm))/Al(200 nm)/Ni(40 nm)/Au (100 nm) metal stack is widely used as N-type ohmic contact [122], [123], [124]. Figure 3-8 show the TLM measurement of this metal stack, on a 500 nm thick with 5×10^{18} cm^{-3} N+ GaN doped layer, as deposited, after RTA (750°C) and after 550°C for 10 min annealing (similar to the the P-GaN ohmic annealing conditions).

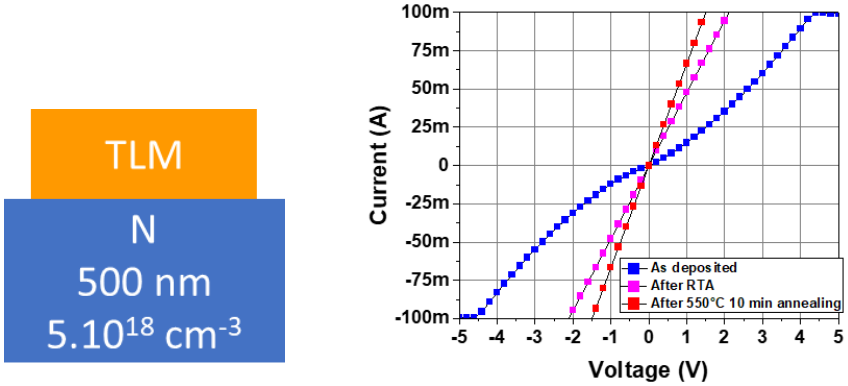


Figure 3-8 : TLM measurements of N+ ohmic contact (Ti/Al/Ni/Au) as deposited, with 750°C RTA and with 550°C annealing

The RTA improvement is visible on the performance of the ohmic contact with low contact resistances (0.35 Ω.mm), compared to the as deposited metal stack that shows a non-linear current-voltage behavior. To further enhance the quality of this parameter, the 550°C for 10 min annealing allows to even higher current at low voltage (1 V) compared to RTA. This translates to a lower contact resistance in the order of 10^{-6} ohm.cm^2. The lower resistance observed with the extended annealing at 550°C for 10 minutes can be attributed to a more uniform and gradual diffusion of metal atoms, promoting better alloy formation. This process also enhances surface morphology and optimizes the interfacial properties between the metal and GaN, resulting in a more efficient ohmic contact with reduced resistance. The use of this annealing is also beneficial in the overall device fabrication as only one annealing is thus necessary for both P- and N-type ohmic contacts.

3.3.3 Beveled mesa as optimized edge termination solution

3.3.3.1 Development of mesa etching recipe

The edge termination is a critical element in high voltage devices to avoid premature breakdown. As discussed in the last chapter, the peak electric field at the edge can be drastically reduced using deep mesa in the case of fully vertical structure, which implies the use of etching method as selective p-type doping is not available for GaN. Moreover, in the case of pseudo vertical devices the deep mesa allows accessing and contacting the N+ GaN layer, in addition to edge termination crucial role.

Mesa etching must fulfill various criteria. A non-optimized etching can lead to damage of the sidewall that increases the reverse leakage current. It can also result in a non-uniform breakdown voltage due to the formation of localized peak electric field. Furthermore, etching contamination can produce additional parasitic leakage current.

As seen in references [102], [106], [108] ,the beveled mesa etching profile improved drastically the breakdown voltage and its uniformity, especially when combined with a sidewall proper passivation. The initial etching optimization started with the choice of the mask. Two options were available: a hard mask using metal such as Nickel (Ni) or an oxide mask using Silicon dioxide (SiO2). The Ni-mask metal was found to increase the contamination inside the etching chamber [125] due to the redeposition effect by sputtering inducing sidewall leakage current. Moreover, the Ni-mask metal removal after etching is performed using wet etching [126] that can also increase the contamination of the devices.

The advantages of using SiO2 mask are visible with the easiness of the deposition and removal of this layer using BOE or HF wet treatment, and with the flexibility of the sidewall profile (angle of sidewall) definition[127], [128]. To deposit the Silicon oxide, we used a Plasma Enhanced Chemical Vapor Deposition at 300°C (PECVD)[129]. The relatively low temperature preserves the properties of the top layer compared to the LPCVD (Low Pressure Chemical Vapor Deposition) where the deposition is generally carried out at high temperature (>800°C)[130]. Figure 3-9 shows the TLM measurement comparison of P-GaN (with high doping > 5×10^{17} cm^{-3}) ohmic contact with different types of SiO2 (100 nm thick) deposition: PECVD or LPCVD. The metal deposition method was part of this experiment using either evaporation or sputtering. The lowest contact

resistances have been obtained on sample B2 where the Sio2 mask was deposited using PECVD and ohmic contact was metalized using evaporation and PECVD. This can be explained by the high thermal budget of SiO2 LPCVD deposition that damages the properties of the P-layer as well as the high quality of the evaporation metal films compared to sputtering method[131], [132].

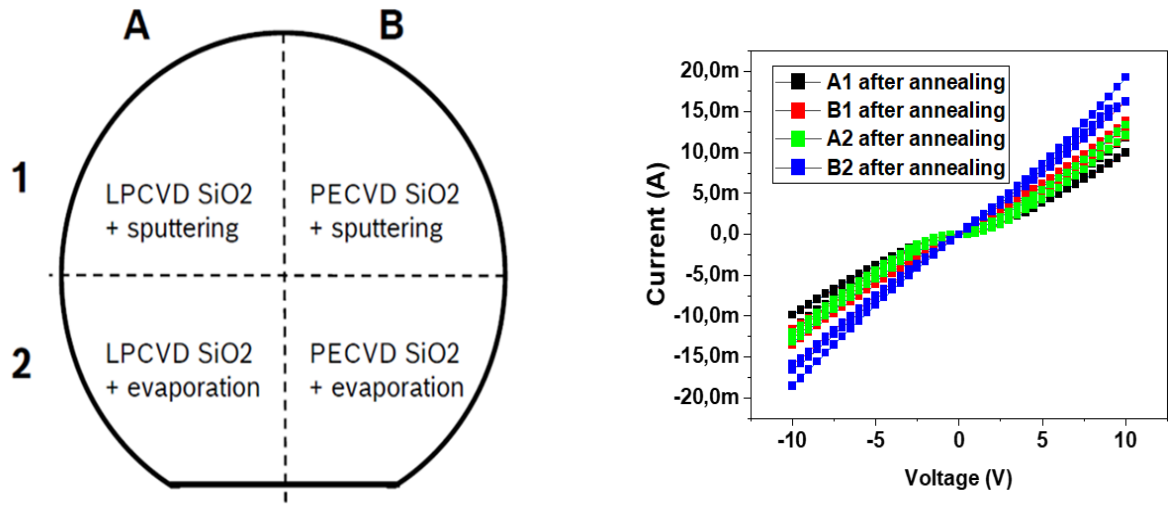


Figure 3-9 : schematic description of the processed samples and related TLM measurement plots for the different configurations of SiO2 deposition and ohmic contact metallization.

To pattern the profile of SiO2 mask after PECVD deposition, we used standard photolithography method with S18XX resist family that is well suited for etching vertical sidewalls. After the resist deposition, the SiO2 mask is etched using Reactive ion etching (RIE) through the opened patterns of the resist. This method of etching allows for obtaining beveled sidewalls of the SiO2 hard mask unlike wet etching. During the RIE etching, a high power SF6 plasma was used. Then, high O_2 plasma followed by SVC wet removal are added to strip the resist. Figure 3-10 show a SEM image of the SiO2 after RIE etching. We can notice a clean surface without any remaining resist. Additionally, we can observe two circles on the upper and lower level of SiO2 mask indicating a beveled profile of the sidewalls.

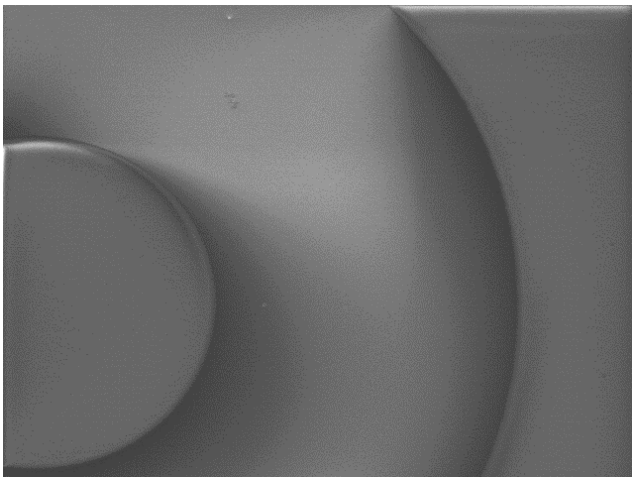


Figure 3-10 : SEM image of SiO2 after resist removal and RIE etching indicating a clean surface and beveled sidewalls

To etch the GaN mesa area, we used an inductively coupled plasma etching reactive ion etching (ICP-RIE). For this purpose, a Cl_2/Ar based recipe is developed with low sidewall damages and beveled profile of the sidewalls. Figure 3-11.a presents an SEM image of the diode after mesa etching where we can observe the quality and the profile of the sidewall angle. These results were obtained with the adjustment of the Cl_2 and Ar flow and pressure inside the ICP chamber. Also, the ICP-RIE power has been optimized to enhance the balance between the chemical and physical etching, since the physical etching is mainly responsible of the sidewall damages.

SEM cross section images of the diode after the mesa ICP-RIE etching obtained by focus ion beam (FIB) appears in Figure 3-11.b. The beveled profile of the sidewalls after etching is well confirmed with an angle around 75°.

(a) (b)

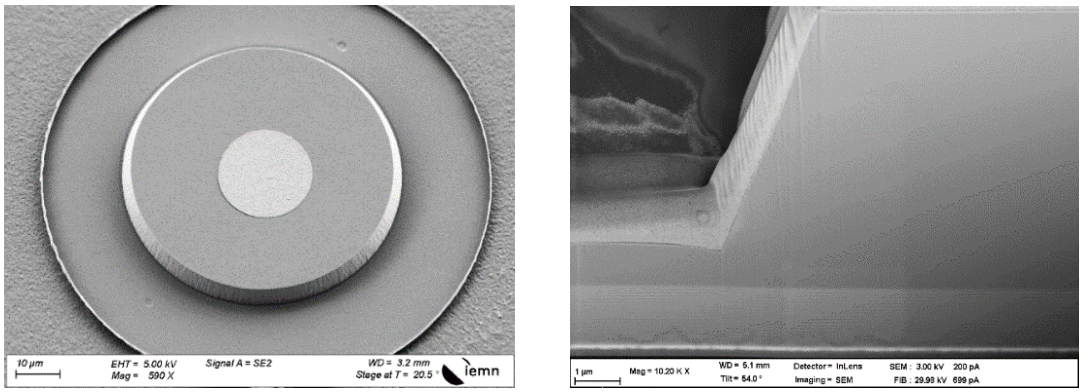


Figure 3-11 : (a) SEM image of a PIN diode at the end of the process (b) FIB vertical image of the beveled side wall of the PIN diode

3.3.3.2 Impact of layout design on off-state performances

The choice of layout design of the structure is essential since a non-suitable design can lead to premature breakdown, non-reliable performances and thermal dissipation issues, especially in the case of a pseudo vertical structure where the crowding effect increases the self-heating in the N+ layer. To evaluate the impact of the layout design on the reverse characteristics, we use two-Schottky diodes with 3 µm and 4 µm as drift region thickness with pseudo vertical architecture. Concerning the layout patterns, rectangular (Figure 3-12.b) and circular diodes have been compared (Figure 3-12.c).

- D1, D2 and D3 correspond to rectangular diodes with large, medium and small area, respectively (Figure 3-12.b).
- C1, C2 and C3 correspond to rectangular diodes with large, medium and small area (Figure 3-12.c).

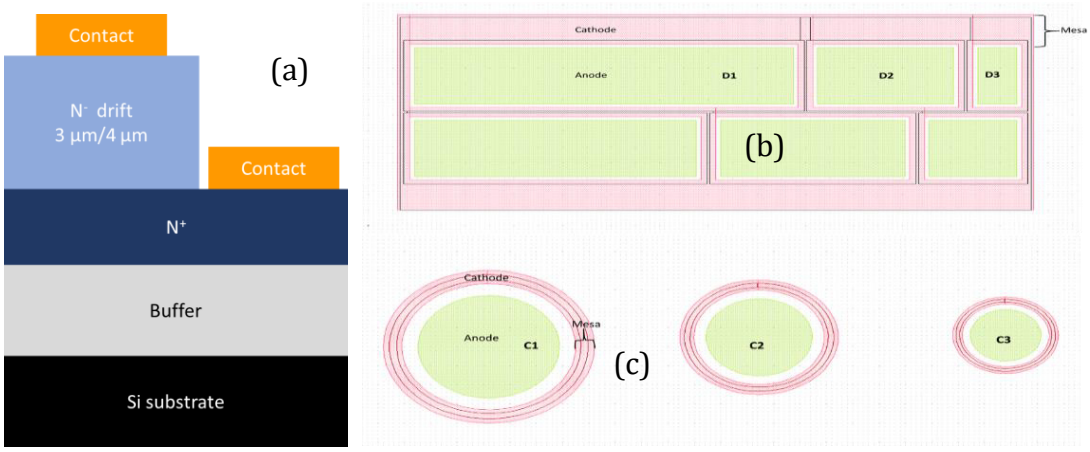


Figure 3-12 : (a) schematic cross section of the Schottky diodes with 3 µm and 4 µm thick drift region used as test devices to check the impact of (b) rectangular and (c) circular layout design on the breakdown performances

Figure 3-13 presents the reverse characteristics of the Schottky diode (with 3 µm and 4 µm thick drift region) for various diode area. In the case of rectangular layout (Figure 3-13.a and .b) an average breakdown voltage of 100 V and 300 V has been extracted for the 3 µm and 4 µm Schottky diodes, respectively. This corresponds to an average breakdown electrical field (calculated with BV/thickness) of these devices that do not exceed 1 MV/cm. In addition, a severe non-uniformity of the breakdown measurements is observed where the leakage current shows a random behaviour for the same anode area. On the other hand, the circular diodes, for both Schottky diodes (Figure 3-13.c and .d), show a higher electric field (> 1 MV/cm) with a more uniform breakdown distribution for

the same anode area compared to the rectangular diodes. For the small diode C3, a high breakdown has been observed with 500 V for the 4 µm drift layer diodes and 300 V for 3 µm drift layer diodes. Moreover, if we compare the leakage current, we notice lower current in the case of the circular diode.

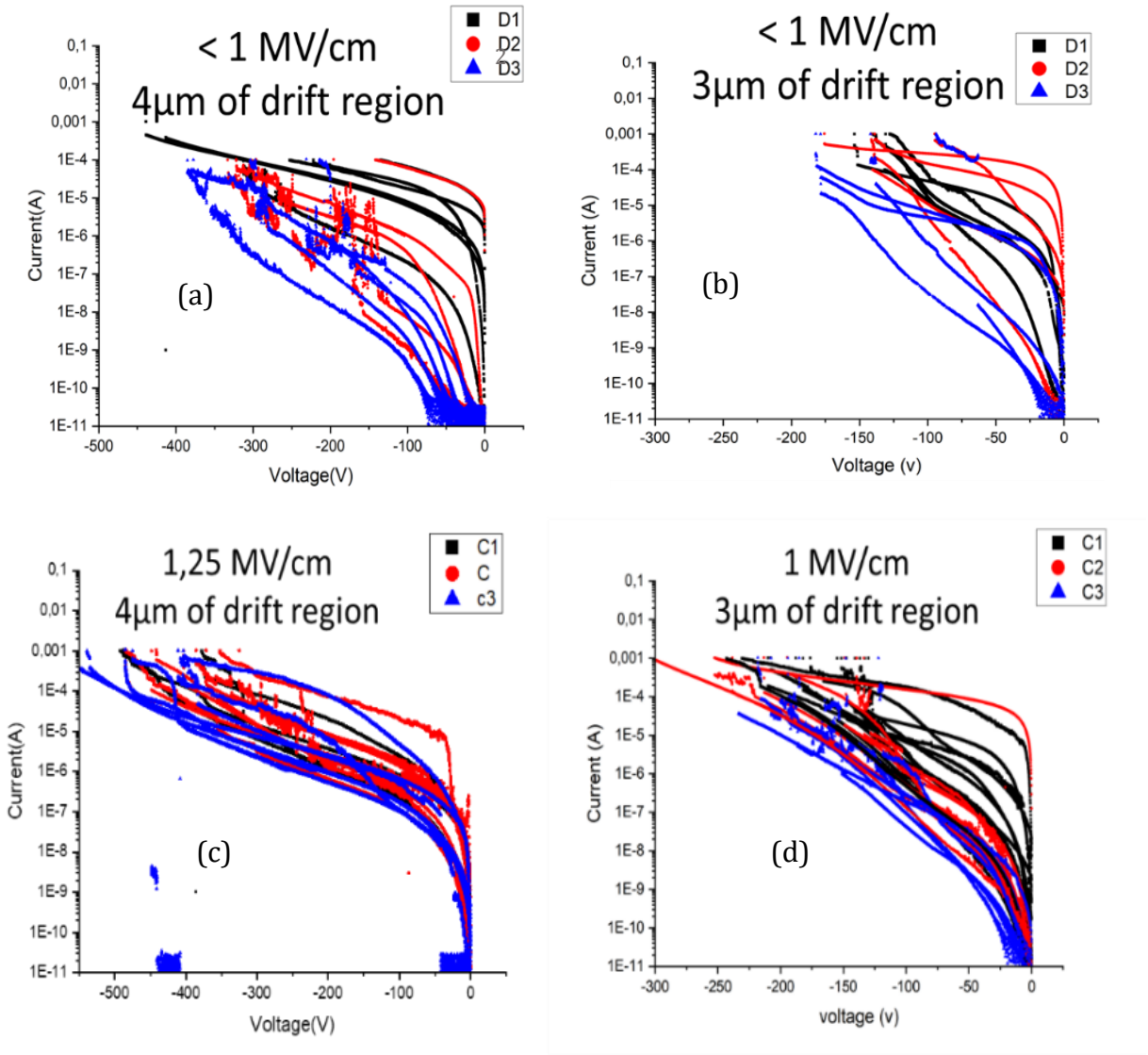


Figure 3-13 : breakdown measurement distribution across the samples of rectangular diodes from the 4 µm (a) and 3 µm drift layer structures (b) Schottky diode. breakdown measurement of circular diodes from the 4 µm (c) and 3 µm drift layer structures (d)

The difference of the rectangular diode performances as well as the variation of the leakage current with this layout can be explained with the crowding of the peak electric field around the sharp angle of the design. In addition, this also increases the self-heating issues in the N+ layer that impacts the reverse characteristics. To avoid the sharp angles,

the use of a circular design is desired, which allows for more uniform and higher breakdown voltage.

As we showed the benefits of circular diodes, the layout design has been implemented in our new mask-set (see Figure 3-14) to include an extensive diode scaling (from 1 mm down to 20 µm diode diameter) with a spacing of 20 µm between the anode/mesa and mesa/cathode (in the case of pseudo vertical structure). The large circle within the cells corresponds to the membrane opening, which will be used for the backside processing.

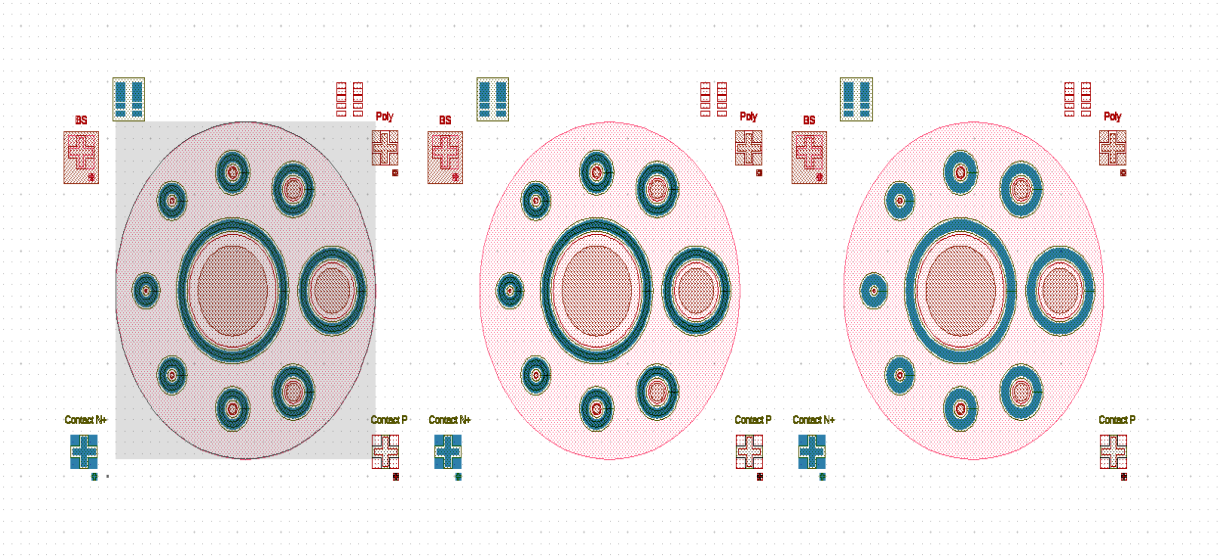


Figure 3-14 : final layout design of the diode showing circular cells of didoes with various diode area. The large circles encountering the diodes are the backside membrane circles

3.3.3.3 Deep mesa etching for fully vertical GaN-on-Silicon

In the previous chapter, we demonstrated that the deep mesa etching allows for a drastic reduction of both edge peak electrical field and leakage current. To confirm the simulation, fully vertical PIN diodes (Figure 3-15.a) with various mesa etching was used. Figure 3-15.b describes the evolution of the extracted reverse bias at 10 µA leakage current versus mesa etching from both simulation and measurement. The mesa etching corresponds to the etch part of the P-layer and the drift layer. The good matching between the measurement and simulation confirms the TCAD simulation predictions. Starting from 60 % of total thickness etching, the breakdown voltage remains constant owing to the significant reduction of the edge peak electric field. From this, the use of an optimized deep mesa etching as edge termination appears to be a proper way to achieve a high breakdown voltage, which will be beneficial for unlocking the avalanche capability.

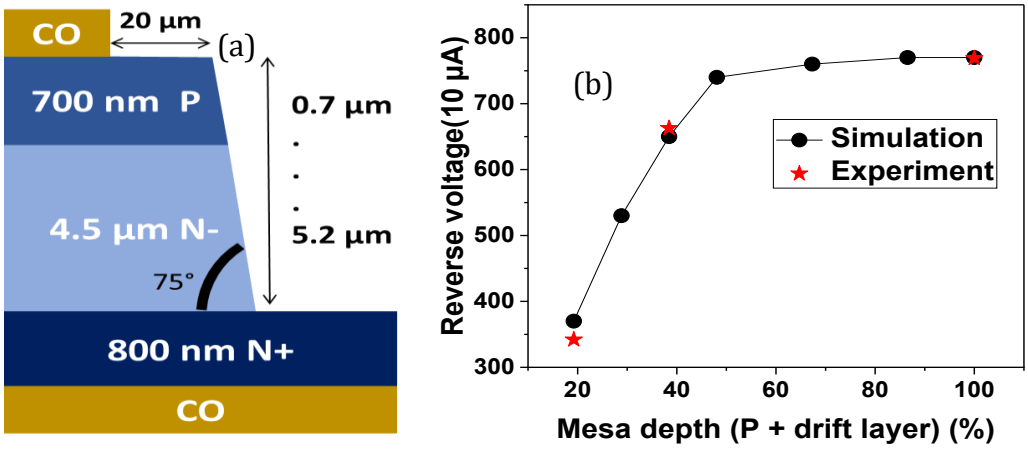


Figure 3-15 : (a) schematic cross section of the PIN diode design used in the extraction of reverse voltage at 10 µA leakage current (b) from both simulation and measurements.

It can be pointed out that to obtain the structure of Figure 3-15.a, we used the backside process optimization, which will be described in the next section of this chapter.

3.3.4 Strengthen the fully vertical devices by means of polyimide passivation.

For the front side processing, we have demonstrated the need of a deep mesa etching as an optimized edge termination solution. However, in the case of fully vertical design, the use of deep mesa in the frontside combined with backside substrate removal makes the devices quite fragile. Indeed, the resulting total thickness across the samples is significantly reduced, especially within the mesa region (equal to the N+ thickness plus the remaining thickness of the drift layer). This low thickness increases the probability of device cracks during further processing. Therefore, the mechanical robustness of fully vertical GaN-on-Silicon devices must be addressed within the process flow.

To enhance the mechanical device robustness, several solutions were studied such as the addition of thick SiO2 passivation and flexible resist. The SiO2 solution was found to be effective in reducing the number of cracked devices, but still more than more than 60 % of devices were damaged. Plus, the SiO2 thickness deposited by PECVD is limited to about 2 µm.

The second option is the flexible resist such as thick polyimide passivation. The polyimide is a negative resist that can be patterned using standard lithography methods. Then, a 1 h

long annealing is applied to this resist. The thickness of polyimide can be adjusted in a flexible way, in our case to 10 µm. Figure 3-16 shows schematic cross section with SEM images of the fully vertical GaN-on-Silicon PiN diodes after polyimide passivation. Two scenarios are considered: in the first one the polyimide covers only the sidewalls of the PIN diodes and in the second case the polyimide fills in all the mesa opening.

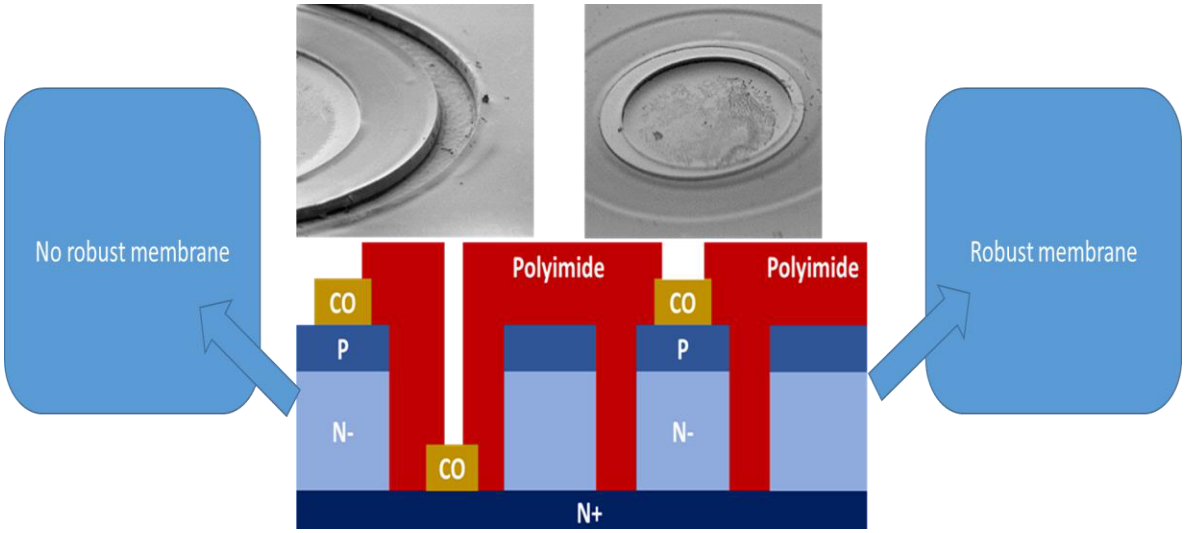


Figure 3-16 : Schematic cross section with SEM images of polyimide covering the sidewalls of the PIN diodes and filling the mesa etching.

When the polyimide covers only the sidewalls of the PIN diodes, the device mechanical fragility is reduced but the cracks are still occurring, especially for large mesa area. The best solution is to fill in completely the mesa to fully suppress the resulting damages. After complete frontside and backside processing, 100 % of the devices survived. Figure 3-17 shows vertical SEM/FIB cross section images. As can be observed, the polyimide covers the mesa opening, replacing the removed part of GaN. We will see in the backside processing section, the benefits of using polyimide passivation, which enables the implementation of thick backside metallization.

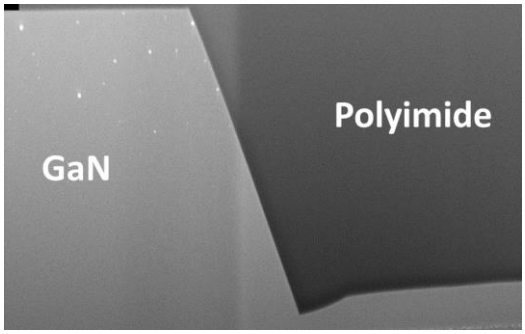


Figure 3-17 : vertical SEM/FIB cross section images of a PiN diode after polyimide passivation.

3.4 Backside processing optimization

The most innovative part of the fully vertical GaN-on-Silicon fabrication flow is the backside processing. An N+ backside layer access should be created by removing the Silicon substrate and the buffer layers locally. As discussed in chapter 1, several methods can be employed to access the N+ backside, including complete substrate removal through front-side bonding. However, this approach is prone to failure due to the significant strain issues, limiting its application on a full wafer scale. A more effective alternative is local substrate removal, which reduces failure rates and minimizes mechanical issues across the entire wafer.

After the local substrate removal, the ohmic contacts to the N-face N+ GaN backside layer need to be developed. In this section, a process optimization allowing for vertical GaN-on-Silicon PIN diode state-of-the-art performances will be described.

3.4.1 Silicon local removal

Generally, the thickness of the Si is below 1 mm. In our case, a substrate thickness up to 1.3 mm has been used to prevent strain relaxation issues, especially during the cooling after growth. To fully remove the Si substrate, direct etching would increase drastically the processing time. That is why, we first thin down the substrate before etching. The Silicon local removal thus combines a thinning and etching process.

3.4.1.1 Thinning of the substrate calibration

The substrate thinning is performed using a Grinder (Figure 3-18). First, the sample is cleaned and bonded to a silicon wafer using wax. A specific wax is used, which can be easily stripped afterwards. To enhance the surface adhesion, the bonding is released with a low pressure. To maintain a stable mechanical constraint, the thinning removal rate has been fixed to 5µm/min with a high flow of water, which is key for the thermal management during thinning. Moreover, the total thickness should not be below 200 µm after thinning to avoid device breakage. On the other hand, to enhance the metallization adhesion within the membranes, the thickness of Si should not be higher than 500 µm. For these reasons, we chose to thin down the silicon substrate to 300 µm.

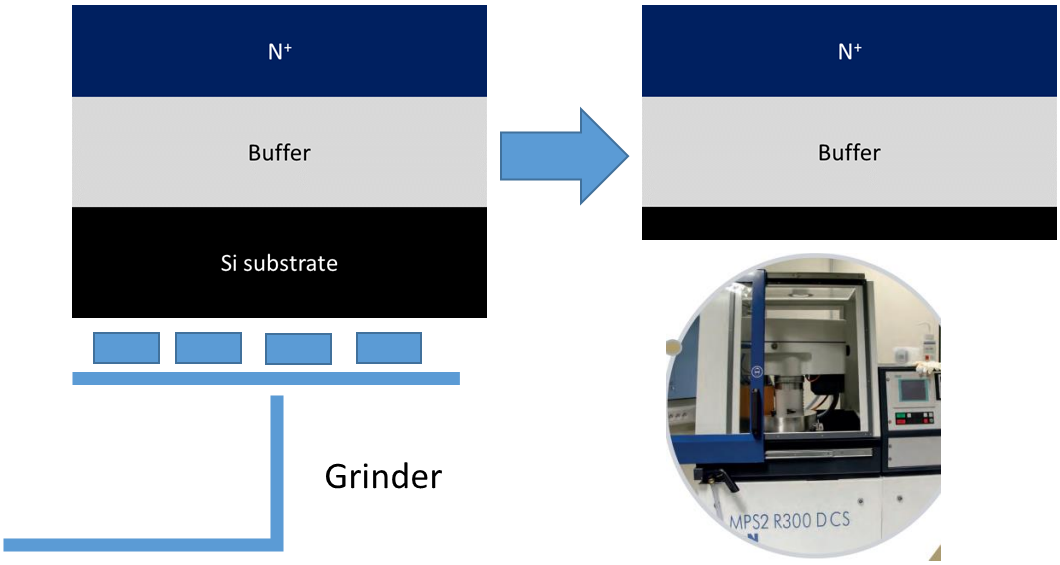


Figure 3-18 : schematic cross sections of the Silicon substrate thinning from 1.3 mm down to 300 µm with an image of the Grinder

3.4.1.2 Deep local etching of Silicon substrate

After thinning the substrate, the 300 µm of silicon must be removed locally to create the access towards the N+ layer. The best-known method of deep silicon etching is the deep reactive ion etching (DRIE). An 18 µm thick of SPR220 µm resist is deposited and patterned using standard lithography. To obtain a smooth surface after etching, the lithography conditions was optimized. Figure 3-19 shows the silicon surface without (a) and with (b) optimization of thick resist deposition. Indeed, a thicker resist leads to an increased time of resist relaxation of more than 2 hours but reduces the internal stress of the layer ensuring a uniform adhesion on the surface. The optimization of the lithography step also allows for a better transfer of the patterns, the circle contours being well defined after a long resist relaxation.

(a) (b)

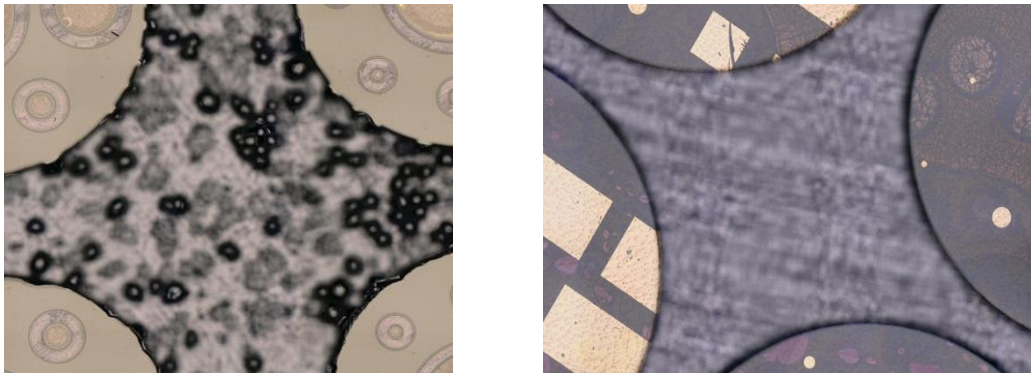


Figure 3-19 : silicon surface without (a) and with (b) optimization of thick resist deposition, highlighting the surface roughness and the circle opening.

After patterning the SPR220 mask, we etch the silicon substrate locally using DRIE, which relies on multiple cycles of C_4F_8 (octafluorocyclobutane) passivation deposition and SF6 etching. With this loop cycle, the SF6 etches in an anisotropic way the silicon while the sidewalls are protected by the C_4F_8. In addition, the SF6 based plasma silicon etching is very selective to GaN. Silicon DRIE depends on the opening size. Figure 3-20 shows the silicon removal corresponding to 180 etching cycles. The larger the opening the deeper the etching. Therefore, the choice of the opening size is essential for the uniformity of etching. On the other hand, we can observe the negative bevelled sidewall (angle > 90 °). This will create issues during the backside metallization as the corners will not be covered, and thus resulting in a discontinuity of the metal inside the membranes.

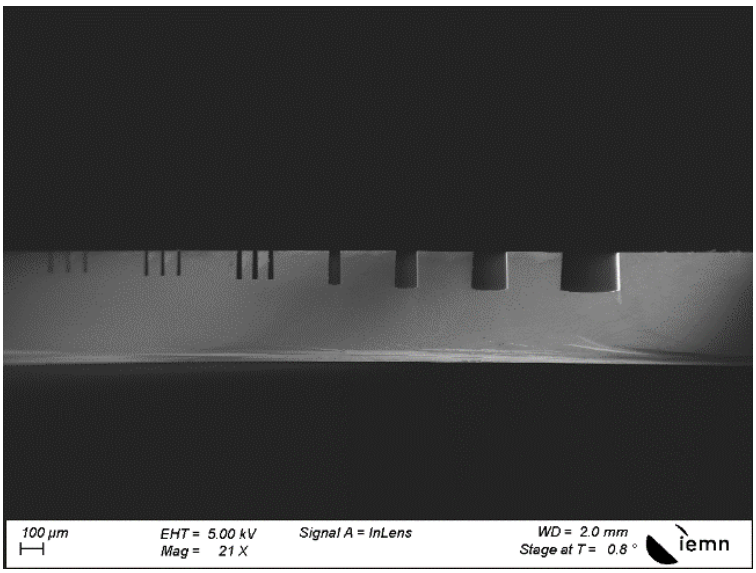


Figure 3-20 : SEM image of the silicon after 180 cycles of DRIE showing a non-uniform etching that depends on the opening size.

To prevent any metal discontinuity, the DRIE etching condition needs to be tuned. Figure 3-21 presents an SEM image of silicon following the optimization of the DRIE recipe. This improvement is achieved by adjusting the etching and passivation cycles, specifically by increasing the passivation time. The extended passivation duration provides enhanced protection to the sidewalls, resulting in more vertical etching. A vertical sidewall was obtained with an angle around 90°. To avoid the non-uniformity during etching, a unique size of backside circle opening was used, covering all the whole frontside diodes as shown in Figure 3-22.

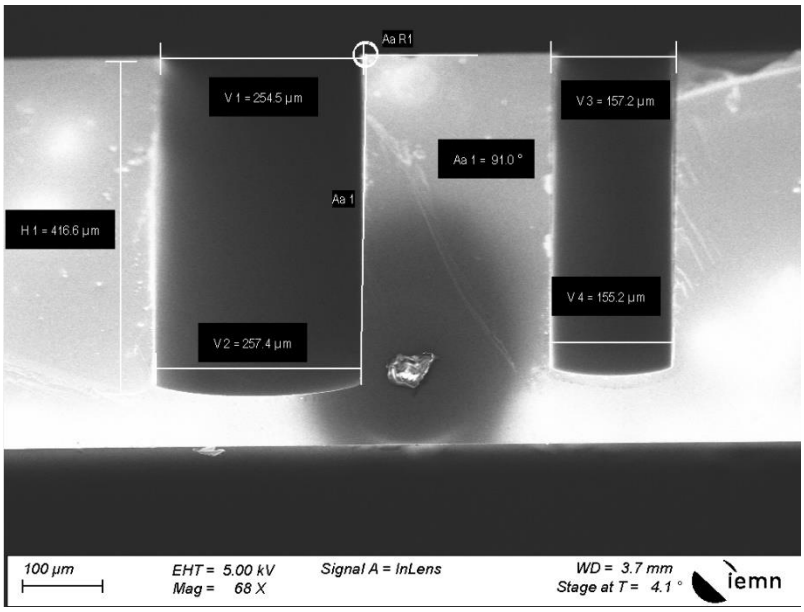


Figure 3-21 : SEM image of the silicon after 180 cycles of DRIE and the optimization of DRIE recipe showing vertical sidewalls of 90°.

After the silicon local removal, we can see the frontside diodes by transparency. Figure 3-22 shows the precise alignment, the smooth surface, and uniform etching after silicon DRIE local removal.

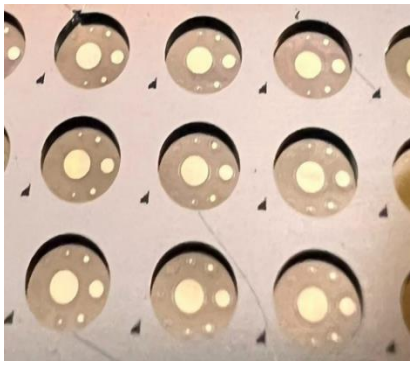


Figure 3-22 : optical backside image of the membranes after local substrate removal showing a precise alignment, a smooth surface and uniform etching. The frontside diode contacts are visible through the GaN film.

3.4.2 Buffer etching

3.4.2.1 ICP recipe optimization

After the silicon removal, we etch the buffer layers using an ICP system. Processing induced damages nor additional strain issues have to be avoided during the buffer etching. Furthermore, this etching is critical because of the short etching distance with the devices having a reduced thickness. On the other hand, the etching of this layer is advantageous for the suppression of the leakage current path. Indeed, the buffer layers

"absorb" a large part of the dislocations. Figure 3-23.a shows the resulting surface after buffer layers etching without optimization of the etching recipe. A severe waviness of the surface is created, indicating stress induced issues, actually due to thermal dissipation during the buffer etching. To overcome this problem, a Fomblin oil has been added between the frontside and the holder to enhance the thermal dissipation. Furthermore, a Cl_2-based recipe was employed instead of a BCl_3-based one, along with a reduction in RIE power from 300 W to 100 W, reducing with physical etching damage. This adjustment significantly increased the etching duration, effectively doubling the process time. In addition, the etching is done using a cycle of less than 1 minute. We can observe the resulting surface after optimization of the buffer etching, where the waviness of the surface completely disappeared, see Figure 3-23.b.

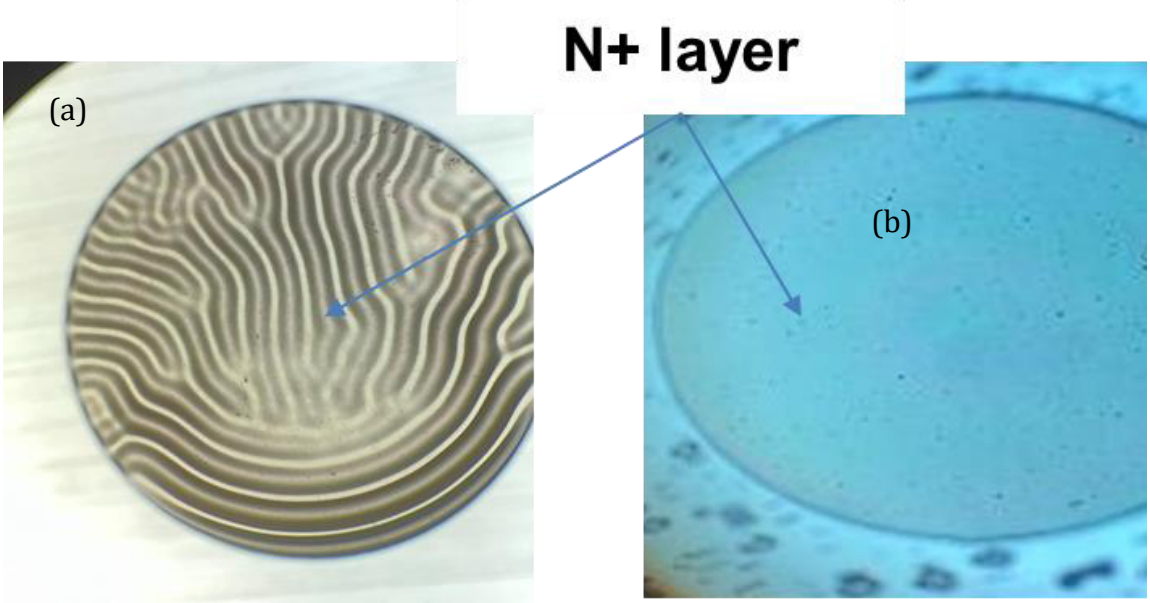


Figure 3-23 : backside optical image of the surface after buffer layers etching with non-optimized conditions (a) and optimized conditions (b)

3.4.2.2 Etching depth control

Due to the membrane's critical etching depth, standard etching monitoring methods could not be used, such as the step control using profilometer for instance. Considering that each layer has its own electrical signature, the etching time was calibrated using direct current measurement on the surface (without metals) at 30V. This provided the following etching profile:

- nA for the buffer,

- mA for the N+ layer,
- µA for the N- layer.

Consequently, the etching timing can be properly calibrated for each layer. Figure 2-24 presents the evolution of the measured current versus time of etching. Starting from 7 min of etching, the depth reaches the N+ layer.

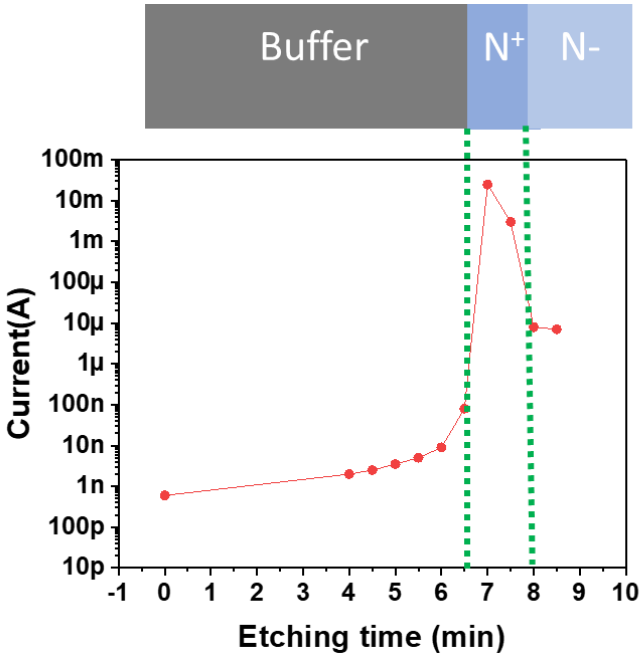


Figure 3-24 : Current (time of etching) curves to monitor the etching depth.

3.4.3 N face N+ GaN ohmic contacts

The development of a fully vertical architecture based on GaN grown on silicon or Sapphire substrate is challenging. The development of fully vertical GaN devices on Silicon substrate is achievable by means of a local substrate and buffer layer removal. In this case, several challenges needed to be addressed including an optimized removal of Si and buffer layers without damaging the active de-vice layers with a precise etching control to preserve the N+ layer thickness and the optimization of the backside ohmic contact by means of transmission line measurement. Indeed, one of the key challenges is the development of the backside ohmic contact on N-face polarity of the n+ doped GaN layer. This change of crystal polarity in GaN alters the physical properties of the material and

influences the device performances. Unlike Ga-face (Figure 3-25. b), the formation of low resistive ohmic contacts on the nitrogen face of n+ layer is more complex due to the inversed polarity from the back-side, the atom position in Wurtzite crystal of GaN is prone to high oxidation (Figure 3-25. a)[133]. This problem is faced with the vertical GaN-on-GaN structure in the field of power electronics and optoelectronics.[134], [135], [136], [137], [138], [139], [140], [141], [142] However, this parameter has not been assessed on Silicon substrate due to the non-planar surface of the membrane, limiting the use of standards lithography method. In this work, TLM lift-off inside GaN on Silicon membranes using laser direct lithography has been developed allowing proper characterization of the specific contact resistance on top of the N-face n+ doped GaN backside layer. The electrical results are supported by X-ray photoelectron spectroscopy (XPS) and scanning electron microscopy (SEM) analysis to reveal the impact of the wet treatment. Then, we propose a simple approach to overcome the limitation of the N-face N-GaN ohmic contact. A high temperature HCl based wet treatment of the GaN surface was developed, which significantly enhanced the ohmic contact quality under specific treatment conditions.

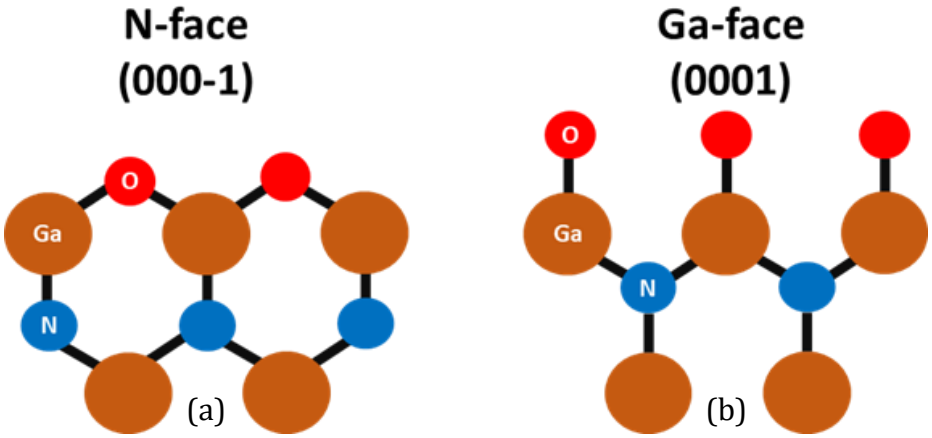


Figure 3-25 : Side view diagram of the N-face (a) and Ga-face (b) GaN in the presence of oxygen atoms

A GaN-based PIN diode heterostructure was grown on a 6-inch silicon substrate using metal-organic chemical vapor deposition (MOCVD). The GaN epitaxy started with the growth of a thick buffer layer, followed by an 800 nm n+ doped GaN layer with a Si-doping concentration of 5×10^{18} cm^{-3}. Subsequently, a 3.5 µm n- doped GaN drift layer was grown with a Si-doping concentration of 3×10^{16} cm^{-3} corresponding to a net doping of 9×10^{15} cm^{-3} considering the residual carbon concentration. The growth was completed with a p-

type GaN layer on top, doped with 2×10^{19} cm^{-3} of Magnesium (Mg), resulting in a hole concentration of 3×10^{17} cm^{-3} as assessed by Hall effect measurements.

To avoid robustness issues of the membranes, the vertical GaN fabrication process started with the bonding of the front side on a silicon substrate by thermal compression of gold at 300°C (Figure 3-26.a). The metal used for bonding was Ti (100 nm)/Au (200 nm), deposited by evaporation on both the silicon substrate and the PIN diode front side. The backside process began with thinning the Si substrate from 1 mm down to 150 µm, followed by the deposition and patterning of a thick resist layer using standard lithography. This resist layer served as a mask during the local removal of Si using deep reactive-ion etching. The buffer layer was subsequently removed using a Cl2 ICP (inductively coupled plasma)-based recipe. As discussed in section 3.4.2.2, due to the membrane's critical etching depth, etching control is monitored via the electrical conductivity measurements (Figure 3-24).

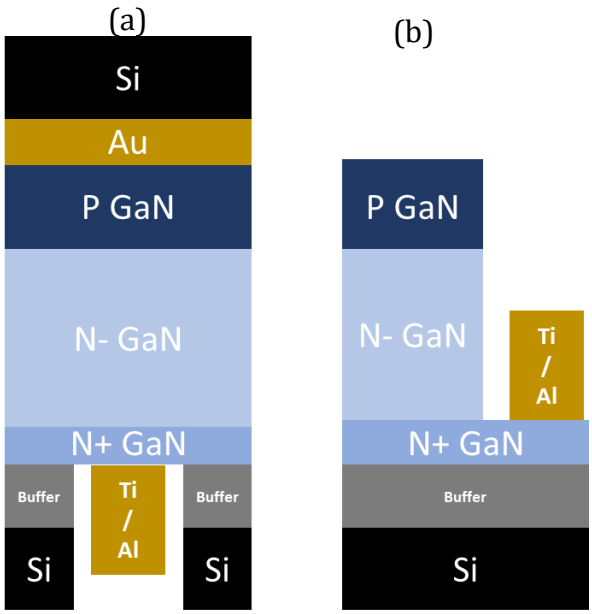


Figure 3-26 : Schematic overview of the studied samples to characterize the ohmic contacts on N-face GaN layer, samples B-D (a) and Ga-face GaN layer, sample A

Standard photolithography based on hard mask to pattern the TLM through the resist was not feasible due to the large gap between the GaN membrane surface and the optical exposure level. Therefore, direct laser writing was applied to achieve the TLM patterns. The vertical device processing concluded with the deposition of a Ti (25 nm)/Al (100 nm) contact layer using evaporation and subsequent lift-off on the backside (Figure 3-27). The aforementioned recipe was used to generate several samples from the same wafer

avoiding any epi-variation. The various samples were used to define a design of experiment prior to the deposition of the contact layer as follows:

- Control samples B1 and B2 were metallized without any treatment, with a delay of 10 minutes and 24 hours after buffer etching, respectively.
- To investigate the time dependence, samples C1, C2, C3, and C4 were treated with HCl (37%) at 70°C for 1 min, 2 min, 3 min, and 5 min prior to metallization, re-spectively.
- To investigate the temperature dependence, samples D1, D2, and D3 were treated with HCl (37%) for 1 minute at room temperature, 55°C, and 70°C prior to metalliza-tion, respectively.
- An additional sample, referred to as sample A, was prepared with a pseu-do-vertical structure. This configuration involved contacting the n+ layer from the front side on the Ga-face after ICP mesa etching (Figure 3-26.b) to compare the Ti/Al ohmic contact quality with the N-face from the same GaN layer.

Transmission line measurements (TLMs) were performed to assess the electrical quality of the ohmic contacts in all cases as described in[143], [144]. Rectangular 50×100 μm^2 TLM pads have been used with 5 µm, 10 µm, 15 µm and 20 µm contact spacing (Figure 3-27) to extract the specific contact resistance. I(V) measurements within the range of [-10 V ; 10 V] between 10 µm contact spacing are used to compare the contact quality of the various applied treatment. KEITHLEY 2612B enabling both 2 probes and 4 probes measurements has been employed for the extraction of I(V) measurements and specific contact resistance extraction, respectively.

In addition to electrical characterization, the samples were also structurally characterized using XPS and SEM. X-ray Photoelectron Spectroscopy (XPS) is a powerful technique for analysing the surface composition and chemical state of materials. In XPS, X-rays are directed at a sample, causing core electrons to be ejected. By measuring the kinetic energy of these ejected electrons, we can determine their binding energy, which helps identify the elements present, their concentrations, and their chemical states. This makes XPS an essential tool for studying the surface chemistry of materials, thin films, and coatings. This technique was used to study the N face surface after HCL treatment in the previous chapter. XPS analysis have been performed right after the HCl treatment using a Sigma

Probe instrument of Thermo Fisher Scientific Inc. with a base pressure of approximately 10^{-9} mbar. A monochromatic Al Kα X-ray source is used as the excitation source. The spectra are calibrated by setting the N-Ga component in the N1s spectra to 397.7 eV[145], [146], [147], [148]. Next, the O-Ga to Ga ratio in the Ga3d spectra is determined by fitting the spectra using CasaXPS (Casa Software Ltd.). The error on the atomic concentrations obtained via CasaXPS is typically estimated to be roughly 10% of the reported value. After XPS, SEM images are obtained from the samples using an FEI Quanta 200F instrument. Cross-sectional images are obtained after cleaving the samples.

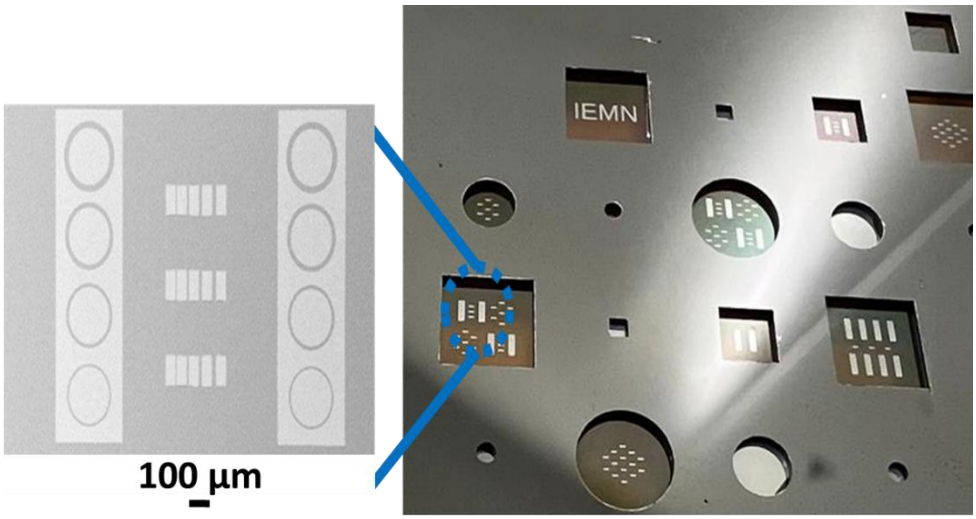


Figure 3-27 : SEM and optical images of vertical GaN membranes with TLM patterns after metallization and lift-off. The rectangular membranes width are 1 mm, 3 mm and 5 mm. The circular membranes diameters are 1 mm, 3 mm and 5 mm.

Figure 3-28.a shows TLM measurements on the N-face for a 10-minute delay between the buffer etching and the deposition of metal (sample B1). The IV characteristics reveal a poor linear behavior although a rather high current of 100 mA at 4.5 V is observed resulting in 2.4×10^{-4} Ω.cm^2 specific contact resistance. When increasing the delay to 24 hours (sample B2), the measured current drops to 40 mA at 5 V due to much higher specific contact resistance $>10^{-3}$ Ω.cm^2. These results suggest that an oxidation phenomenon occurs during the delay time. An HCl (37%)-based wet treatment was developed with a temperature initially fixed at 70°C in agreement with reported results in [149] demonstrating the need of high temperature to efficiently remove the native oxide.

Figure 3-28.b shows the time dependence of the HCl wet treatment at 70°C on the ohmic specific contact resistance. Up to 3 min time duration (samples C1, C2, and C3), the HCl

treatment reduces significantly the specific contact resistance down to 9×10^{-6} Ω.cm^2 without additional annealing (see Figure 3-28. c), making this approach fully compatible with any frontside post-process. On the other hand, when further increasing the treatment time up to 5 min and above (sample C4), the quality of the ohmic contacts severely deteriorates, and the extracted current drops dramatically, indicating a surface degradation due to prolonged treatment.

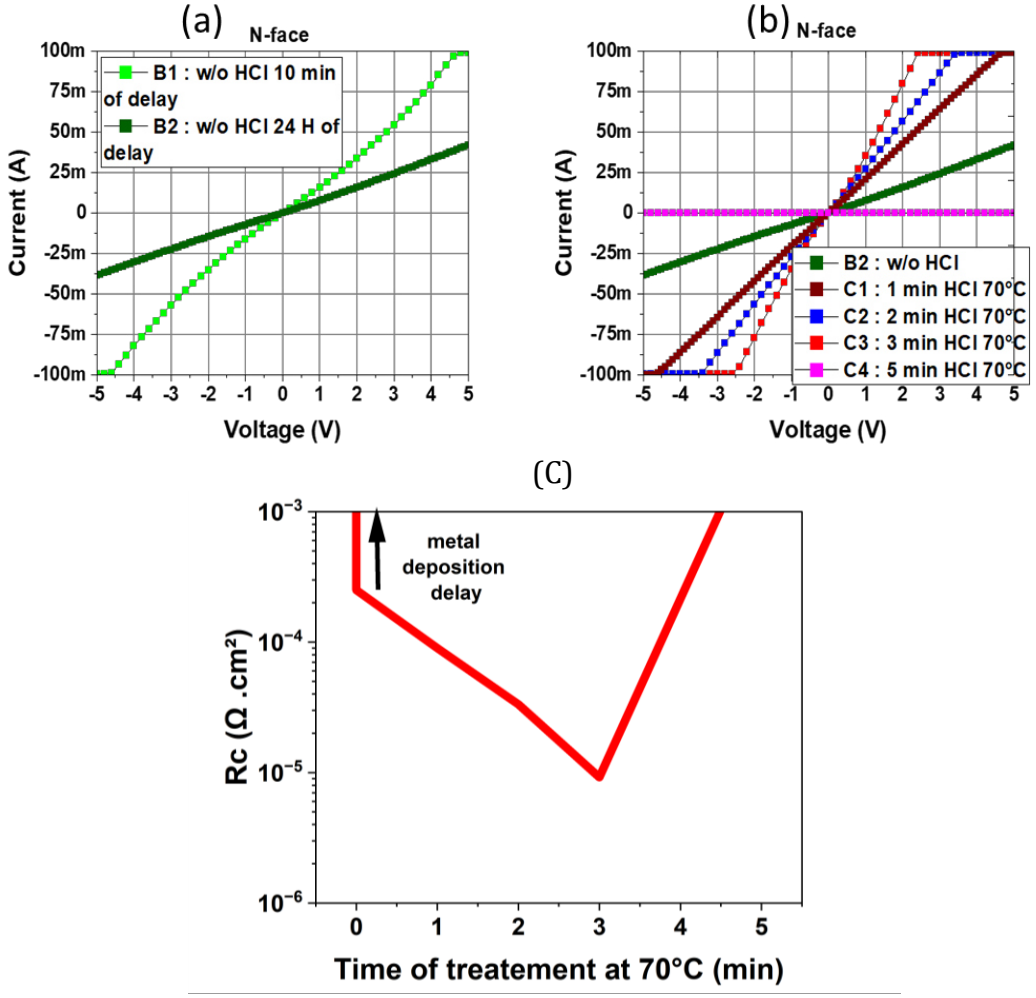


Figure 3-28 : (a) TLM measurements of the N-face ohmic contact without treatment after various time dura-tions between buffer etching and metal deposition. (b) N-face TLM measurements comparison of different HCl treatment times (0–5 min) at 70 °C. (c) Rc versus time of treatment at 70°C

An additional test was performed in order to get some initial insights about the thermal stability of the ohmic contacts. Sample C3 (using the optimum conditions of 3 min HCl treatment at 70 °C) has been introduced in an oven in rich N2 environment at 300 °C for 1 h. Figure 3-29 shows the electrical current-voltage TLM measurements before and after 1 h thermal stress at 300 °C. The identical IV curves clearly indicate that the ohmic

contacts are stable with no short-term impact of the temperature on the applied wet pretreatment.

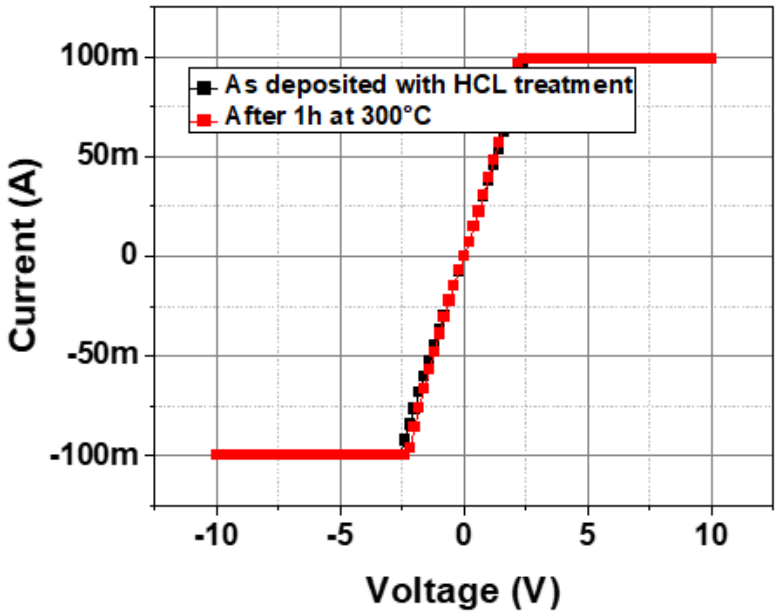


Figure 3-29 : TLM measurements of the N-face ohmic contact with HCl pretreatment before and af-ter thermal stress during 1 h at 300°C

To observe the chemical modification of the GaN surface with the HCl treatment, various N-face and Ga-face samples have been treated with HCl at 70 °C for time duration ranging between 1-20min and immediately measured by XPS. The oxidation state of the surface can be determined by deconvolution the Ga3d spectra into three peaks: Ga-N, Ga-O and Ga-Ga at a binding energy of 20.0-20.1eV, 20.5-21.0eV and 18.5-19.1eV, respectively. [145], [147], [148] As an example, the deconvolution of the Ga3d spectrum of the 5 min HCl treated N-face sample can be found in Figure 3-30.a. Using these fits, the O-Ga to Ga ratio is then calculated and plotted as a function of HCl treatment time at 70 °C in Figure 3-30.b. The data shows that the untreated N-face is oxidized to a greater extent than the untreated Ga-face. In addition, the HCl treatment is observed to reduce the N-face upon treatment time, while even after a treatment time of 20 min, the Ga-face remains roughly unaffected. These findings correspond well to the electrical results, showing no impact of the HCl treatment for the Ga-face, while an initial increase in contact quality is found upon removal of the Ga-O surface species for the N-face. The latter is also in agreement with

literature, reporting that the removal of native oxide from the GaN surface is crucial to obtain low resistance ohmic contacts[138], [150].

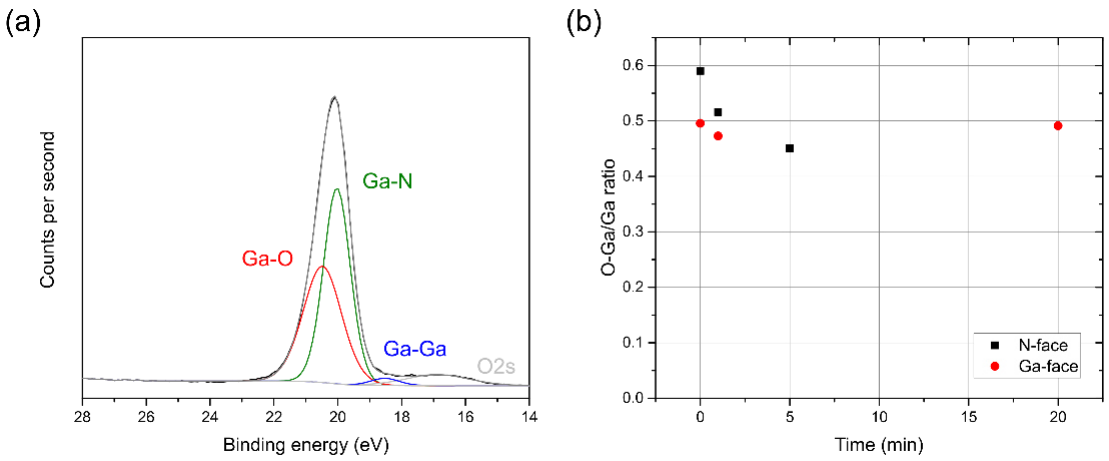


Figure 3-30 : (a) Ga3d spectra of the 5min HCl-treated N-face sample demonstrating how the spectra is fitted. (b) O-Ga/Ga ratio in the Ga3d spectra as measured by XPS as a function of HCl treatment time at 70 °C for N-face (squares) and Ga-face (circles).

SEM images display that the HCl treatment not only reduces the N-face but can also be associated with the formation of hexagonal pyramid-shaped features at the surface, as displayed in Figure 3-31. While the Ga-face again remains unaffected even after 20 min HCl treatment at 70 °C (Figure 3-31.d), the features are observed to enlarge upon treatment time for the N-face (Figure 3-31.a-c). After 5 min HCl treatment, the height and width of the features is estimated to be approximately 128 nm and 166 nm, respectively (Figure 3-31 .e). Similarly,[151] report the formation of sixfold nanopyramids on N-face GaN after etching for 45 min in 2 M KOH at 90 °C whereas the Ga-face is observed to remain smooth. Their observations demonstrate that the hexagonal pyramid shape originates from preferential etching of crystal-line planes. Also in [146], [152] report the formation of pyramid shapes which are observed to increase upon time after etching in heated KOH or H3PO4 solutions.

The formation of these features is accompanied by an increase in roughness of the surface. Hypothetically, this increase in roughness might explain why the 5 min HCl treated sample behaves poorly in comparison to the 3 min HCl treated sample as ob-served by TLM. This would suggest that an optimal HCl treatment time exists on N-face GaN, showing the perfect trade-off between native oxide removal and surface roughness increase to obtain the lowest specific contact resistance.

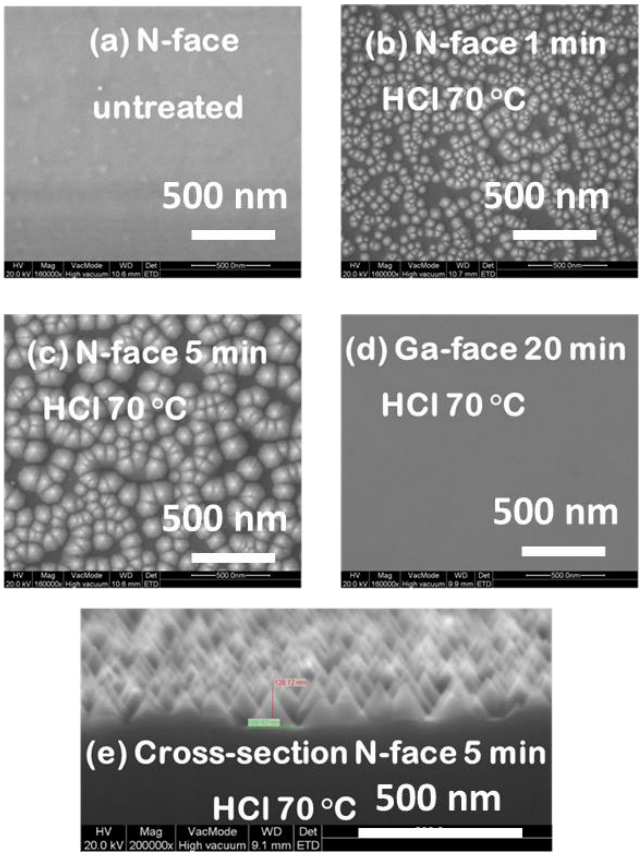


Figure 3-31 : SEM images of the HCl treated GaN surfaces.

Figure 3-32.a compares TLM measurements of different samples treated with HCl for 1 minute at various temperatures to study the impact of treatment temperature on the ohmic contact quality. Sample B2 is the control sample without any treatment. It can be observed that room temperature (RT) treatment (sample D1) improves the TLM characteristics with a higher current. This is also the case for the 55°C treatment (sample D2) delivers still high specific contact resistance $>10^{-3}$ Ω.cm2. The most effective treatment temperature was found to be at 70°C (sample C1), resulting in a significant-ly improved current level with an associated specific contact resistance of 7-8 10^{-5} Ω.cm^2. It is important to note that additional samples were treated with longer treatment times at RT and 55°C, but the ohmic specific contact resistance never reached the ones achieved at 70°C.

For a fair benchmark, specific contact resistance on Ga-face n+ GaN layer were measured with (sample A1) and without HCl treatment at 70°C (sample A2) (Figure 3-32.b). Despite the absence of pretreatment, Ga-face specific contact resistances are comparable to the N-face in sample B1 immediately between buffer etching and metallization. Furthermore,

no impact of HCl wet treatment at 70°C was observed on Ga-face ohmic contacts that generally require extra annealing to further reduce the specific contact resistance. These results confirm that the properties of N-face are significantly different from those of Ga-face GaN layer, suggesting that the native oxide of N-face GaN layer is the major factor influencing the ohmic contact quality but can be mitigated using a proper wet pretreatment without any annealing.

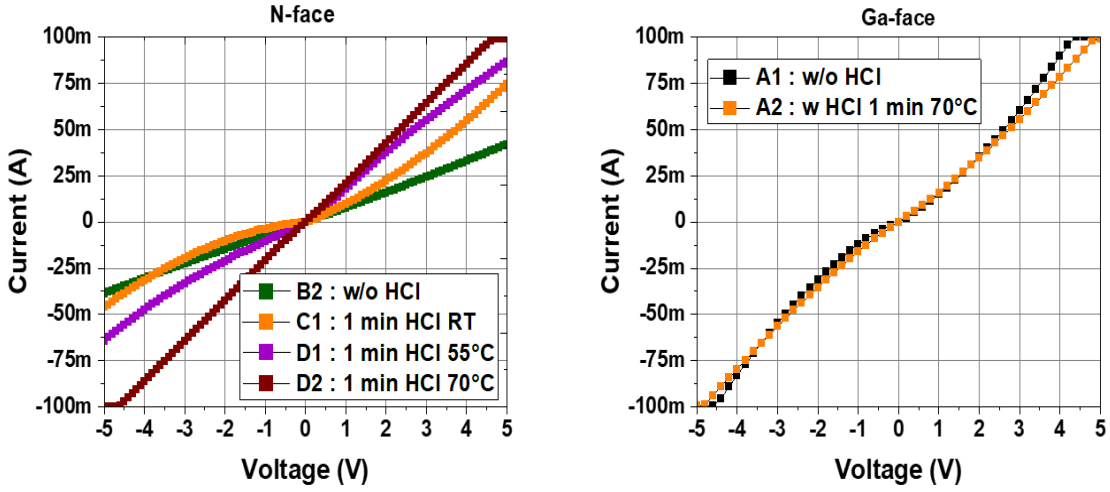


Figure 3-32 : (a) N-face TLM measurements for samples treated with HCl treatment at different temperature (RT, 55°C, and 70°C) (b) Ga-face TLM measurements comparison with and without HCl treatment

Table 4 summarizes the sample while indicating the polarity, the treatment and the extracted specific contact resistance.

Sample	Polarity	Treatment	Specific contact resistance (Ω.cm²)
A1	Ga face	No treatment	10^{-4}
A2	Ga face	1 min 70°C of HCL	10^{-4}
B1 (no delay)	N face	No treatment	2.4×10^{-4}
B2 (24 H delay)	N face	N treatment	High
C1	N face	1 min 70°C of HCL	$7\text{-}8\times10^{-5}$
C2	N face	2 min 70°C of HCL	3.3×10^{-5}
C3	N face	3 min 70°C of HCL	9.10^{-6}
C4	N face	5 min 70°C of HCL	High
D1	N face	1 min RT of HCL	High
D2	N face	1 min 55°C of HCL	High

Table 4: Summary of the samples, polarity and the specific contact resistance

N-face backside ohmic contacts in fully vertical GaN-on-Silicon PIN diodes are assessed. Direct laser writing lithography enabled to pattern TLMs inside the membrane, as standard photolithography could not be used in this frame. TLM measurements from as deposited metal stack showed high specific contact resistance, which degrades over time

between membrane opening and metal deposition. This suggests a gradual oxidation of the N-face GaN. Therefore, an HCl treatment was developed and found to be effective in reducing specific contact resistance and improving the maximum current. The optimum HCl treatment was found to be 3 minutes at 70°C while the contacts were severely degraded for longer time. It can be pointed out that short-term thermal stability up to 300°C shows no degradation of the optimized ohmic contacts. XPS analysis revealed a clear reduction in Ga-oxide with the HCl treatment. Moreover, SEM images showed the formation of pyramids, especially for prolonged HCl treatment explaining the ohmic contact drastic degradation for longer time. Finally, it has also been shown that the treatment temperature of 70°C is critical as much lower improvement occurs when reducing the temperature. This simple approach can be used for fabricating any types of fully vertical GaN-on-silicon devices as no extra annealing is required to achieve negligible backside specific contact resistance and thus fully compatible with frontside processing, which is very desirable in respect of the fragility of the membrane due to the reduce devices thickness.

3.4.4 Thick copper electroplating

The N+ layer plays an important role in electron sourcing but needs proper thermal management to avoid degradation under high on-state current of several amperes and more. In the case of fully vertical devices, the backside metal has to be thickened to dissipate the heat. A well-known solution is the use of thick copper electroplating. Prior to that, a thick Ti/Au metal (>1 µm) is added to the backside layer to ensure the continuity of the metal contact along the membranes, especially around the corners. Using thick copper electroplating is clearly beneficial for large diode areas that theoretically can spread high current, but the electroplating conditions still require optimization. Figure 3-33 show the copper grains electroplating before (a) and after optimization (b). With thick electroplating, a non-homogenous surface due to strain issues can be observed, which can damage the membranes or the sample. By changing the deposition parameters (temperature, rotation, spacing, and solution), the homogeneity can be enhanced with a smoother surface. The temperature of the deposition has been increased from 20 to 45 °C to enhance the reaction within the solution. Concerning the solution rotation, a 300 laps per minute has been used to move the solution inside the membrane so that a uniform deposition of the copper on the Si and membrane can be ensured. Depending on the

sample size, spacing between the copper electrode (anode) and the sample (cathode), must be adapted in order to have an homogenous deposition with a uniform flow of the current line. Instead of using a lab made copper electrolyte solution ($CuSO_4$:0.6 mol/L ; H_2SO_4:1.85 mol/L ; NaCl:100 mg/L)[153], we ought to use a commercialized solution from Dr Galva company. A first deposition was made with 15 mA/cm^2 current density during 30 min to ensure a high-quality film deposition with thin homogenous grain on the sidewall of the membranes. Then, we increase gradually the current density up to 225 mA/cm^2 for a total time of 4 hours. With the optimized deposition, up to 300 µm thick copper electroplating has been deposited with a quite smooth and uniform surface. This is shown with the optical image (Figure 3-34) of the device backside after electroplating. In this next chapter the impact of the thick copper electroplating will be presented.

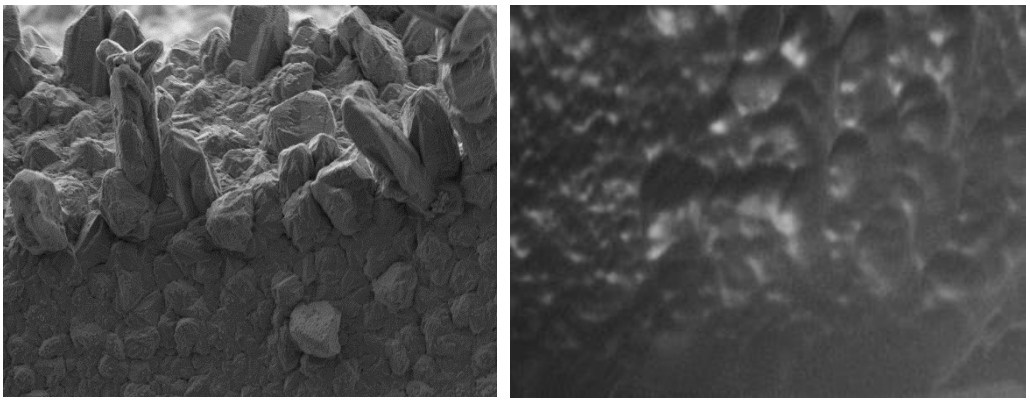


Figure 3-33 : SEM image of electroplated copper film before (a) and after (b) the optimization of the deposition conditions

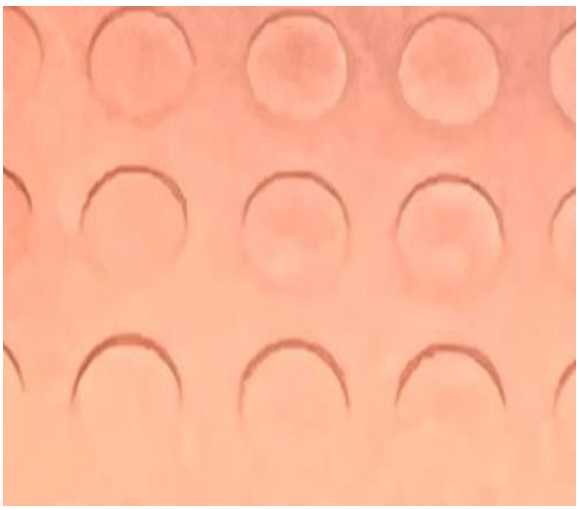


Figure 3-34 : optical image of the backside after thick Cu electroplating.

3.5 Conclusion

In this chapter, the optimized process fabrication of fully vertical and pseudo vertical GaN-on-Silicon PIN diode has been described. An optimization of both frontside and backside steps has been carried out in order to allow the achievement of high and reliable device performances. With the bevelled deep mesa, the edge electric field is reduced allowing a low leakage current. In addition, the optimization of the metal stack and subsequent annealing for both N and P ohmic contact is greatly beneficial for both on and off-state. Furthermore, the thick polyimide passivation strengthens the mechanical robustness of the membranes after deep mesa. Concerning the backside, we ensured that the local substrate removal and buffer do not induce any damages to the devices including waviness of the surface due to strain issues. Then, state-of-the-art N face ohmic contact resistances has been achieved, which is attributed to the native oxide removal by means of a high temperature HCl wet treatment. Finally, a thick Cu electroplating has been implemented with the aim of enhancing the thermal management and further increase the robustness of the devices. Although the developed process concerns vertical GaN-on-silicon diodes, it can be pointed out that many steps (such as mesa edge termination, the polyimide passivation and the backside processing) can be applied to the transistor fabrication.

In the next chapter, we will present the electrical characterizations of the developed devices based on the optimized fabrication process.

Chapter 4: Development of high quality vertical GaN with silicon substrate PIN diodes

4.1 Introduction

In the previous chapter, the design and process of fabrication were discussed while presenting several optimizations aiming for high quality vertical GaN-on-Silicon devices. To reach this proof of concept, the work is mainly focused on PIN diodes development. All the demonstrated studies in this work could be transferred to other types of devices such as Trench MOSFET. In this chapter, we will present several studies of vertical PIN diodes including various buffer configurations, drift layer thickness scalability, and the demonstration of avalanche capability for a vertical GaN-on-silicon heterostructure. Finally, we will describe our optimized vertical PiN diodes combining avalanche breakdown capability at 1200 V with high on-state current > 10 A. Before the results description, we will present briefly the characterization method used to extract the off-state and on-state performances.

4.2 High voltage test bench tool description

To evaluate the electrical device performance, we used a high voltage test bench (HVB) that is presented in the Figure 4-1. It contains multiple modules that support high voltage measurements up to 10 kV and high current capability up to 20 A allowing for multiple terminal measurements. Furthermore, it gives the flexibly to perform both lateral and vertical sweeps by connecting the chuck to the ground. In the case of lateral high voltage measurements, we immerge the devices in a Fluorinert solution to avoid electrical arcing in air between the probes. Also, low voltage forward and off-state characteristics of the vertical devices can be evaluated for both pseudo and fully vertical architectures. It can also be used for TLM measurement of ohmic contacts. Although most of the measurements with are performed at room temperature, the HVB test bench was upgraded during this work to allow measurements at high temperature up to 200°C by adding a thermal resistance to the chuck.

Figure 4-1 : Photography of the high voltage test bench

4.3 Reduction of off-state leakage current using a SiN interlayer inside the buffer

4.3.1 Device structure and process

Novel vertical GaN on Silicon PIN diode have been grown on 8" Si wafers using an MOCVD industrial reactor by AIXTRON company. Figure 4-2 describes the structure showing the doping and thickness of the 5 wafers:

- Samples 1(.X) corresponds to 3.5 µm thick drift region devices.
- Samples 2(.X) corresponds to 5.5 µm thick drift region devices.

The goal of this study is to understand the impact of the buffer configuration on the reduction of leakage current using a SiN layer insertion. A step graded buffer is used on top of a 200 nm AlN nucleation layer, 250 nm $Al_{30}Ga_{70}N$ layer, 50 nm AlN layer and 250 nm $Al_{30}Ga_{70}N$ layer. based on this buffer configuration, the SiN insertion is as follows:

- Samples 1 and 2 are reference samples without SiN layer.
- Sample 1.1 and 2.1 are heterostructures with one SiN layer, between the nucleation layer and $Al_{30}Ga_{70}N$ layer.
- Sample 1.2 is the device with two SiN layers located between the nucleation layer and $Al_{30}Ga_{70}N$ layer, the second SiN being inserted between the AlN and $Al_{30}Ga_{70}N$ layer.

During this study, the device has been processed using a pseudo vertical design, which is sufficient to extract the off-state performances of the devices.

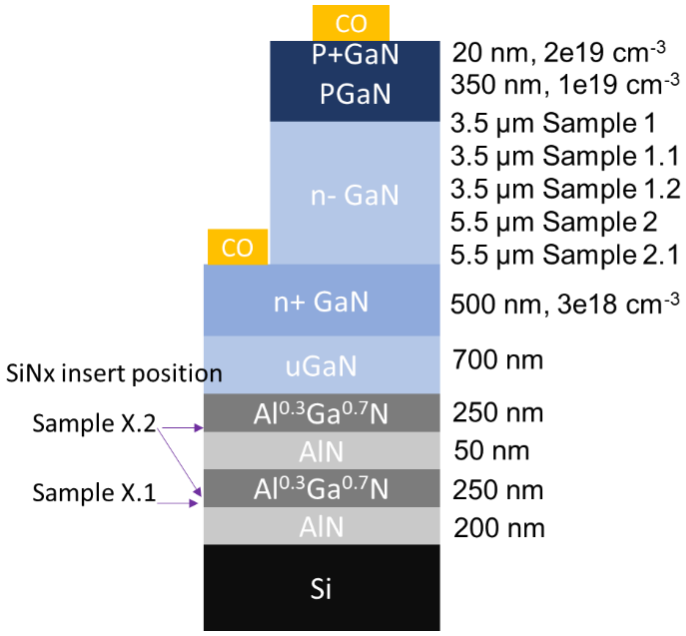


Figure 4-2 : schematic cross section of the device structures including SiN layer within the buffer

4.3.2 Results and discussion

Figure 4-3 presents the off-state measurement for sample 1, 1.1 and 1.2 with large 1 mm-diameter and small 100 µm-diameter diode. The breakdown voltage is uniform for small diodes with a breakdown voltage of 670 V. However, a non-uniform breakdown has been observed on the large diodes, as described in table 4. This can be explained by the high amount of dislocation density and defects covered by a larger surface increasing the probability of a premature breakdown voltage. The same observation appears for sample 2 and 2.1 (Figure 4-4), the small diode shows a high breakdown voltage of 950 V but highly non-uniform for the large diodes. A high electric field average (BV/thickness of the drift) has been extracted of about 1.9 MV/cm, which corresponds to more than 2.4 MV/cm peak electric field at the junction, calculated using equation 7.

The insertion of SiN layer within the buffer allows for a significant reduction of the leakage current. The single SiN-insert in sample 1.1 and 2.1 reduce the leakage current by 40 % at 600 V and 900 V, respectively, compared to the reference 1 and 2 samples (see Figures 4-3 and 4-4). By adding another SiN layer within the buffer, which corresponds to sample 1.2, the leakage current is reduced by almost 80 % at 600 V comparing to sample 1. The reduction of the leakage current is attributed to the reduction of the electrical active

dislocation density. Indeed, the extracted dislocation density using XRD without SiN is in the range of 10^8 cm^{-2}. For samples with SiN inserted layers, the dislocation density drops to mid-low 10^7 cm^{-2}, see reference[49]. The correlation between the dislocation density extraction and the off-state measurement confirms the interest of this approach. However, it is worth noting that the breakdown voltage for the entire samples is destructive showing no avalanche capability.

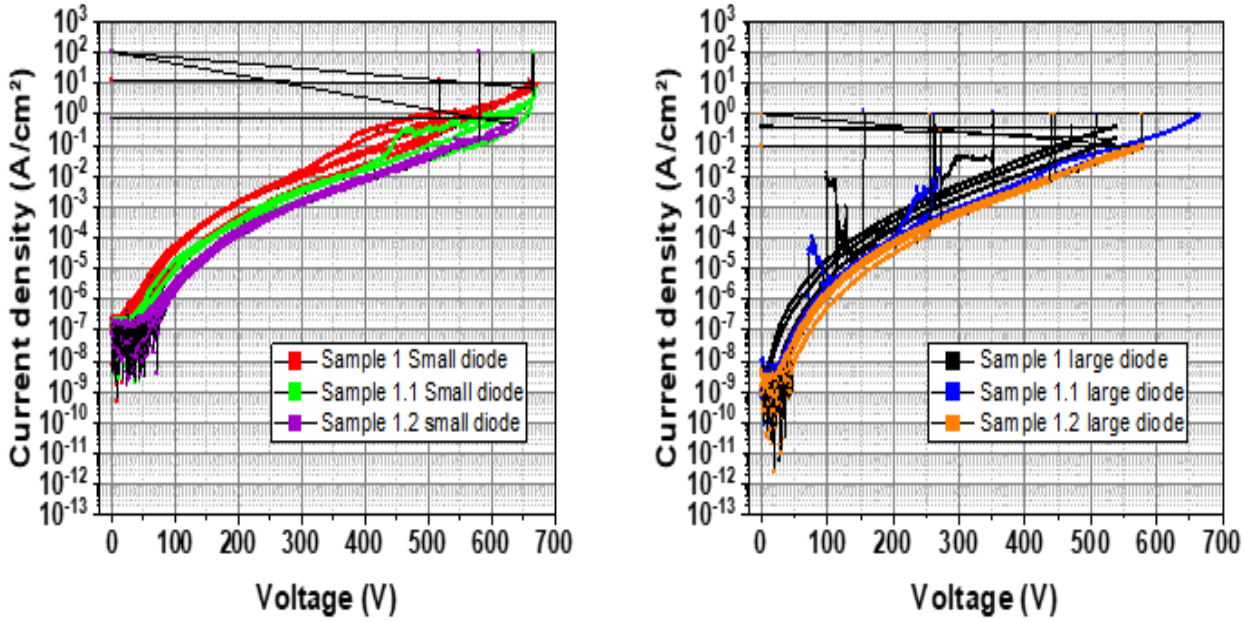


Figure 4-3 : reverse characteristics for small and large diodes of sample 1, 1.1 and 1.2.

	BV (V) d=0.1 mm	*E(MV/cm) d=0.1mm*	*BV (V) d=1 mm*	*E(MV/cm) d=1mm*
Sample 1	*670*	*1.9*	*150-630*	*0.4-1.9*
Sample 1.1	*670*	*1.9*	*150-660*	*0.4-1.9*
Sample 1.2	*670*	*1.9*	*150-650*	*0.4-1.9*

Table 5 : summary of the off-state measurements of samples 1, 1.1 and 1.2

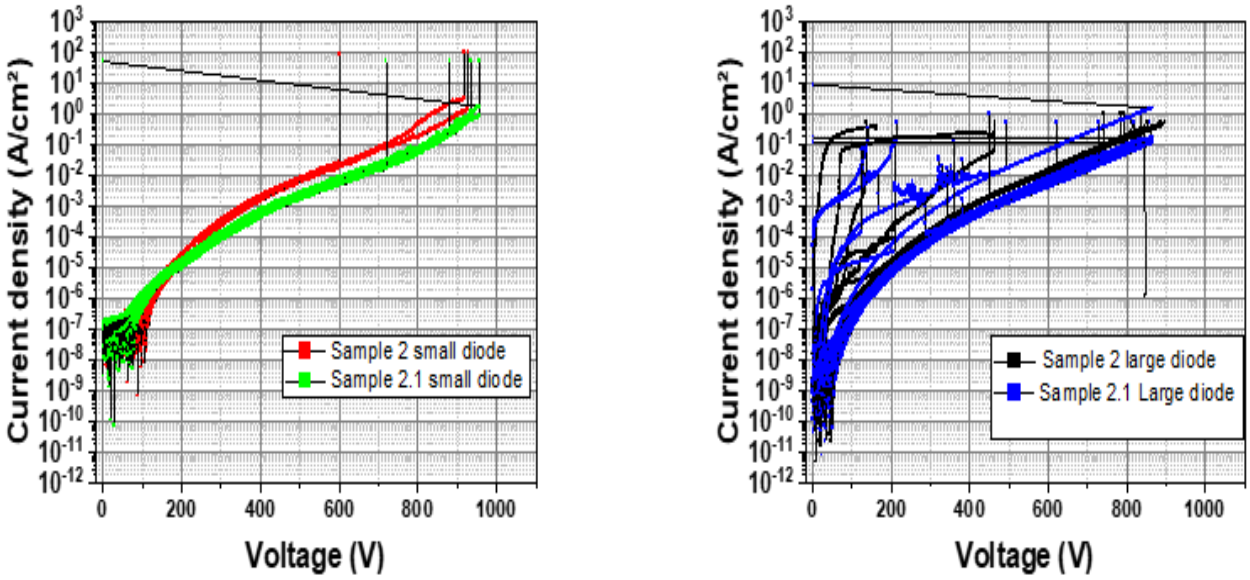


Figure 4-4 : reverse characteristics for small and large diodes of samples 2 and 2.1.

	BV (V) d=0.1 mm	*E(MV/cm) d=0.1mm*	*BV (V) d=1 mm*	*E(MV/cm) d=1mm*
Sample 1	*950*	*1.8*	*150-900*	*0.4-1.8*
Sample 2.1	*950*	*1.8*	*150-900*	*0.4-1.8*

Table 6 : Table 7 : summary of the off-state measurements of samples 1, 1.1 and 1.2

Figure 4-5 shows the on-state characteristics of the samples. A non-uniform Vth has been observed due to an activation problem of the P layer. Nevertheless, the samples 1, 1.1 and 1.2 have a similar Ron of 0.8 mΩ.cm^2. Samples 2 and 2.1 shows a Ron around 1 mΩ.cm^2. From these results, we can deduce that the SiN layer insertion has no impact on the forward characteristics of the devices.

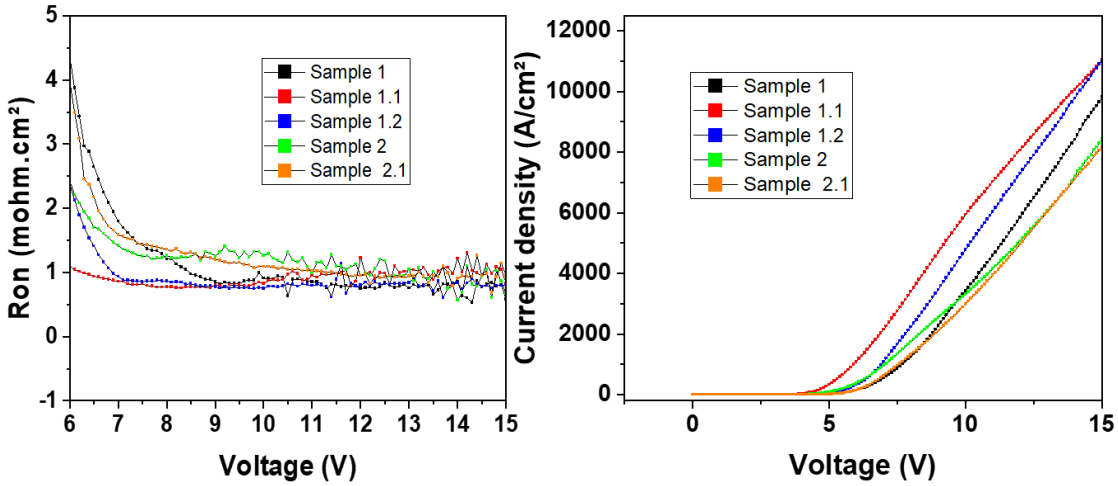


Figure 4-5 : Forward characteristics of the devices with and without SiN layer insertion

4.4 Enabling high quality thick epitaxy using island growth inside the buffer

In this section a detailed description of the epilayer growth used to achieve high thicknesses on silicon substrate is presented.

4.4.1 Device structure growth and process

The epitaxial growth process was performed by Siltronic company using a commercial Veeco vertical rotating disc MOCVD reactor, configured with a 5 × 6" susceptor. They grew the epitaxial layers on boron-doped Si(111) substrates, which had thicknesses of 1000 µm and 1300 µm. TMAl, TMGa, NH3, SiH4, and Cp2Mg as precursors, with H_2 and N_2 as carrier gases have been used. During the growth, the wafer curvature using a DRT-210 Veeco deflectometer was monitored. Before starting the growth, the substrates were annealed in-situ in an H_2 environment at 1050 °C to remove surface oxides and contaminants. A 200 nm thick AlN nucleation layer was then deposited, followed by a 40 nm thick AlGaN transition layer. Additionally, a superlattice (SL) comprising 41 periods of AlN/$Al_{0.1}Ga_{0.9}N$, each about 33 nm thick, was created, resulting in a total buffer thickness of approximately 1.6 µm. The growth conditions were optimized in a way to favour island growth within the superlattice, with island coalescence and a shift to a 2D growth mode occurring around 15 SL periods away from the AlGaN/SL interface. This island growth mechanism was essential for reducing threading dislocation density (TDD) and minimizing compressive stress relaxation in the subsequent active GaN layers.

The active GaN layers, structured from bottom to top, included: a 500 nm thick n+ GaN drain layer ([Si] ~ 5×10^{18} cm^{-3}, n ~ 5×10^{18} cm^{-3}); n- GaN drift layers of varying thicknesses (3/3.5/4.5/5.5/6/6.5/7.4 µm) with ([Si] ~ 3×10^{16} cm^{-3}, n ~ 0.9×10^{15} cm^{-3}); a p-type GaN layer (Mg ~ 2-5×10^{19} cm^{-3}, p ~ 3×10^{17} cm^{-3}); and optionally, a 20 nm thick p++ GaN cap-layer (Mg ~ 1×10^{20} cm^{-3}). These active layers were grown at a surface temperature of 1010 °C and a pressure of 250 mbar. The V/III ratio for the layers was adjusted by varying the TMGa supply, with ratios of ~ 90 (drain), 350 (drift), and 400 (pGaN), while keeping a constant NH3 flow of 50 slm. In-situ activation of the p-GaN was applied in a hydrogen-free environment. Quasi-vertical circular PIN diodes were fabricated, using the process flow described in the previous section.

4.4.2 Results and discussion

4.4.2.1 Strain engineering

For the growth of the P-i-N structures, island growth within the AlN/$Al_{0.1}Ga_{0.9}N$ superlattice (SL) buffer has been employed. Atomic force microscopy (AFM) investigations, as detailed in [48], determined the island density in the initial part of the SL to be approximately 5×10^{8} cm^{-2}. Additionally, scanning electron microscopy (SEM) cross-sections revealed that most islands formed on V-pits present in the AlN nucleation layer. Figure 4-6.a shows the filled V-pits and islands within the SL, with the dark and bright layers corresponding to AlN/$Al_{0.1}Ga_{0.9}N$, respectively. Island coalescence was achieved after around 15 SL periods, leading to flat interfaces between the SL layers. The tilted side facets of the islands helped bending a significant portion of the dislocations, drastically reducing the threading dislocation density (TDD). Figure 4-6.b also displays a transmission electron microscopy (TEM) analysis under weak beam dark-field conditions using g0002 to visualize the dislocations. The TEM image predominantly shows mixed dislocations (a + c Burger's vector). Additional TEM investigations using g1-100 and g11-20 confirmed that island growth effectively reduces the TDD of pure edge dislocations with a Burger's vector (not shown). Since dislocations with an edge component contribute to compressive stress relaxation, the findings in [48] demonstrated that island growth is essential for incorporating sufficient compressive stress in the subsequent active GaN layers. This compensation is crucial to counteract the thermal expansion coefficient (TEC) mismatch.

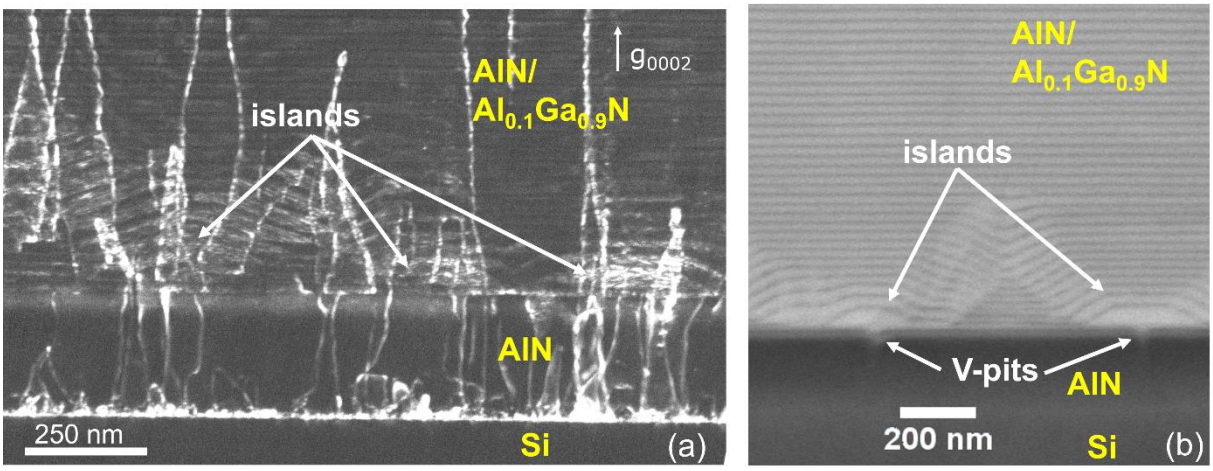


Figure 4-6 : (a) The weak beam dark field TEM cross-section using g0002 reveals c-type (mixed and screw) dislocations in the AlN nucleation layer and the lower part of the SL buffer. A significant number of threading dislocations (TDs) are bent and annihilated due to the island growth mechanism (b) The SEM cross-section illustrates the formation of islands in the SL above V-pits created in the AlN nucleation layer. Complete island coalescence is observed after approximately 15 SL periods away from the AlGaN/SL interface, highlighting the effectiveness of the growth process.

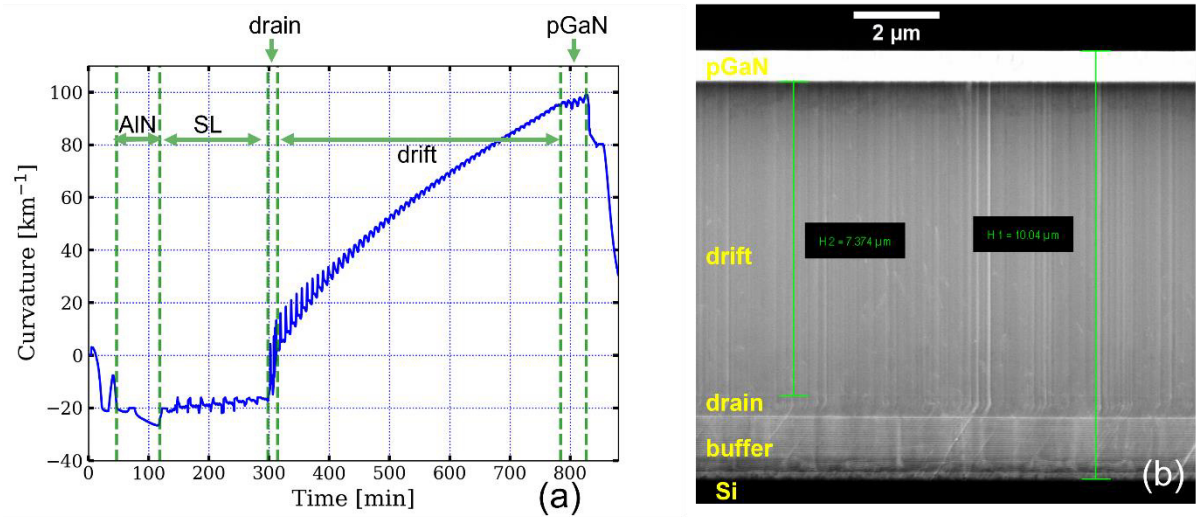


Figure 4-7 : (a) The in-situ measured curvature during the growth of a GaN-on-Si P-i-N structure with a 7.4 µm thick drift layer shows that the spikes observed in the buffer and GaN layers are measurement artifacts. The nearly constant curvature slope in the drift layer indicates minimal compressive stress relaxation. (b) The SEM cross-section of the epitaxial layer structure provides a detailed view of the layers, demonstrating the quality and uniformity of the growth.

Figure 4-7.a illustrates the in-situ curvature measurements of a GaN-on-Si P-i-N structure featuring a 7.4 µm thick drift layer, resulting in a total epitaxial thickness of 10 µm, grown on a 1300 µm thick Si(111) substrate. Additionally, Figure 4-7.b provides an SEM cross-section of the structure. Positive curvature indicates a convex wafer shape, while negative curvature denotes a concave shape. The sharp peaks observed are artifacts due to Fabry-

Perot interferences. According to the Stoney equation, the incremental stress (i.e., the instantaneous incorporated stress of the growing layer) is proportional to the curvature slope[154]. For the 7.4 µm thick drift layer, an almost linear curvature slope was observed, indicating an average incorporated compressive stress of -0.9 GPa, as derived using the method outlined in [43]. Considering the temperature-dependent thermal expansion coefficients (TECs) for GaN and Si provided in a[155], the thermally generated tensile stress from cooling down from 1010°C to room temperature is approximately 0.8 GPa. This suggests that the optimized buffer layer introduces sufficient compressive stress in the GaN layers to offset the TEC mismatch. Ex-situ bow measurements of the complete wafer, excluding a 3 mm edge, revealed a convex bow of 21 µm, measured as the peak-to-valley height distance. Furthermore, the epitaxial layers remained crack-free with a 5 mm edge exclusion.

For the growth of thick GaN layers, increasing the substrate thickness from 1000 µm to 1300 µm proved beneficial in minimizing slip-line formation and reducing the risk of wafer breakage. Figure 4-8 presents X-ray topography images using the Si(333) reflection for P-i-N structures with 5 µm and 7.4 µm thick drift layers grown on 1000 µm and 1300 µm thick Si(111) substrates, respectively. The images clearly demonstrate that increasing the substrate thickness effectively reduces {110} slip-lines in the Si substrate.

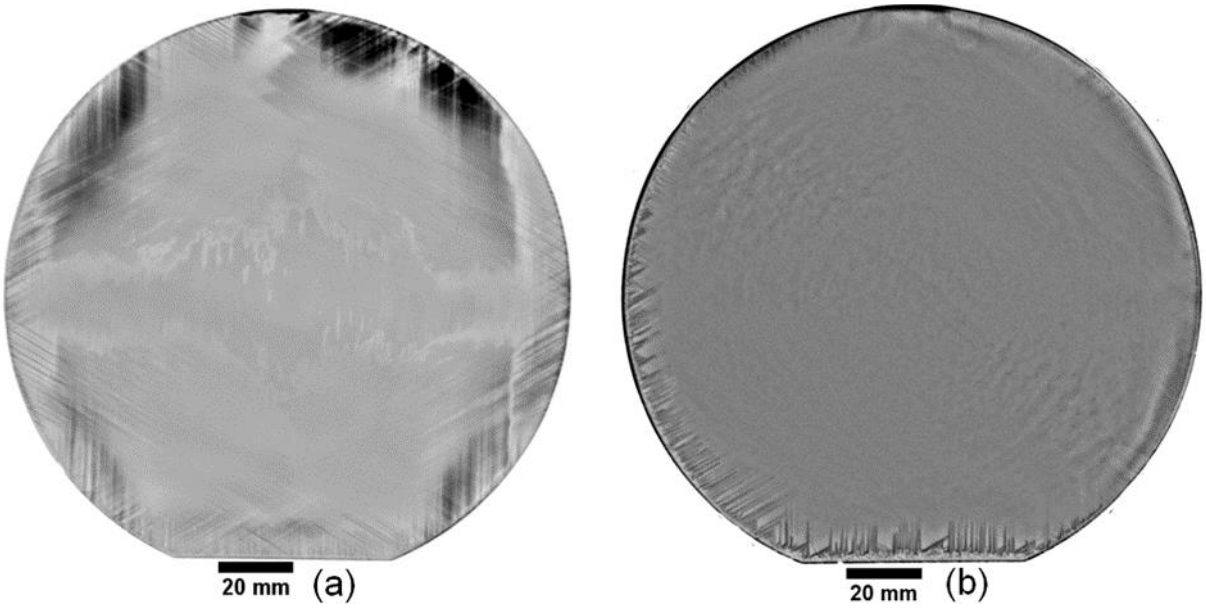


Figure 4-8 : X-ray topography (XRT) images using the Si(333) reflection illustrate GaN-on-Si P-i-N structures with 4.5 µm and 7.4 µm thick drift layers grown on 1000 µm (Figure a) and 1300 µm (Figure b) thick Si(111) substrates, respectively. These images clearly reveal the presence of slip lines running along the Si{110} directions

To estimate the threading dislocation density (TDD), X-ray diffraction ω-scans of the (0002) and (10-12) reflections were conducted using a triple-axis setup, and the full width at half maximum (FWHM) was evaluated. For the sample with a 3.5 µm thick drift layer, the FWHM values were 382 and 448 arcsec for the (0002) and (10-12) reflections, respectively. This corresponds to a TDD of approximately 1×10^{9} cm^{-2}, calculated using the method described in [156]. For the sample with a 7.4 µm thick drift layer, the FWHM values were 220 and 263 arcsec for the (0002) and (10-12) reflections, respectively, resulting in a TDD of approximately 5×10^{8} cm^{-2}. These findings indicate that increasing the drift layer thickness further reduces the TDD.

4.4.2.2 Doping optimization

Secondary ion mass spectroscopy (SIMS) analysis for a P-i-N structure with a 4 µm thick drift layer were conducted by EAG Laboratories at the wafer's center, revealing the doping profile shown in Figure 4-9. In the drift layer, the average carbon ([C]) and silicon ([Si]) concentrations were 1×10^{16} cm^{-3} and 3×10^{16} cm^{-3}, respectively, while the oxygen level was below the detection limit of 2×10^{15} cm^{-3}. Electrochemical capacitance-voltage (ECV) measurements on a dedicated n-/n+ test structure, where the n- layer was grown under the same conditions as the drift layer, indicated a net ionized donor concentration of 0.9×10^{16} cm^{-3}. Hall effect measurements of the same drift layer grown on an insulating buffer confirmed a free electron density of 1×10^{16} cm^{-3} and a high electron mobility of 756 cm^{2}/Vs.

For a [C] concentration of approximately 4×10^{16} cm^{-3}, achieved by growing the drift layer at a lower temperature of 990°C, insulating behavior was observed, and the net ionized donor concentration was below 10^{15} cm^{-3}, making it unmeasurable via ECV. This underscores the role of carbon as a deep acceptor and the necessity of its suppression to prevent carrier compensation and electrical insulation of the drift layer, as also reported in [157].

For the drift layer, a low growth rate of about 1 µm/hr and an NH3 flow of 50 slm (hardware limit) were utilized. While increasing the growth temperature could further

reduce the carbon concentration, it also led to meltback etching at the wafer bevel. The drain layer, grown at a higher rate of around 4 µm/hr, exhibited a significantly higher [C] background. Additionally, there was an increase in [C] from the beginning to the end of the drain layer due to the curvature change from concave to convex (as seen in Figure 4-8), resulting in a lower temperature at the wafer center due to a gap between the susceptor and substrate.

Despite this, transfer length measurements of the drain layer revealed a low sheet resistance of about 61 Ω/sq, and Hall effect measurements on test structures showed a free electron density of 5×10^{18} cm^{-3}. The drain layer thickness was kept intentionally low (approximately 500 nm) to reduce compressive stress relaxation, which is exacerbated for [Si] > 1×10^{18} cm^{-3}. Using germanium (Ge) as an n-type dopant could allow for a thicker drain layer since Ge does not enhance compressive stress relaxation [158].

SIMS analysis showed a relatively low activation ratio ([Mg]/[H]) of 1.5, which could be improved by employing activation conditions with a higher thermal budget. However, this may also lead to surface degradation, such as the formation of Ga droplets. Hall measurements indicated a similar resistivity of approximately 2 $\Omega.cm^{-2}$ in the p-GaN layer with and without a p++ cap layer. Nevertheless, I-V characteristics clearly showed that the ohmic contacts significantly improved with the addition of the p++ cap layer.

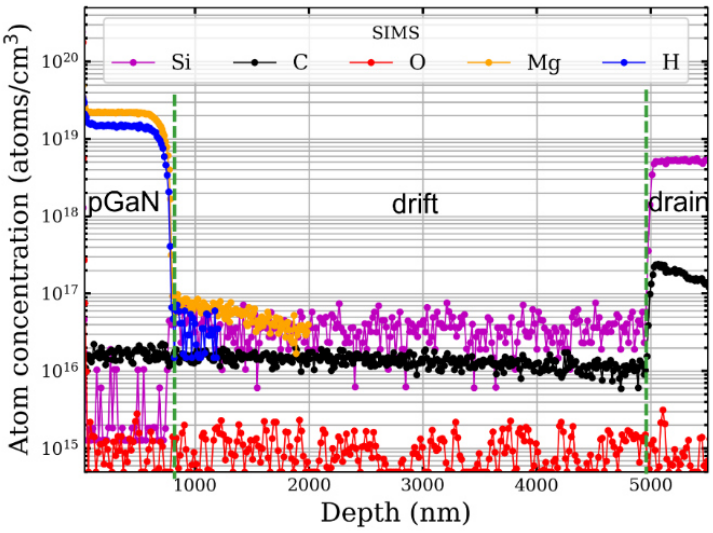


Figure 4-9 : Impurity concentrations in the active layers of a GaN-on-Si P-i-N structure were measured using SIMS.

4.4.2.3 Electrical characterization

Figure 4-10 presents the typical forward J-V characteristics and specific on-resistance Ron of the quasi-vertical P-i-N diodes, with current normalized to the anode area. The turn-on voltage, measured at a current density of 100 A/cm^2, was approximately 3.45 V for diodes with a p++ cap layer and about 3.85 V for those without. Ron ($\partial V/\partial J$) was extracted in the linear regime of the J-V characteristics, showing a consistent value < 0.4 mΩ.cm^2 for all diodes. The linear regime was achieved at around 6 V for diodes with the p++ cap layer and approximately 10 V for those without.

These results demonstrate that contact formation is significantly improved by incorporating a p++ cap layer, thereby reducing the threshold voltage. Additionally, the small anode diameter of 20 µm effectively suppresses the effect of current crowding. It is worth noting that the current crowding issue could be mitigated by using a fully vertical structure, which would allow for larger diodes.

The data also indicate that the thickness of the drift layer does not impact Ron,sp, suggesting that the resistivity of the drift layer is not a limiting factor. This is attributed to the optimized doping concentration and the high mobility of the drift layer.

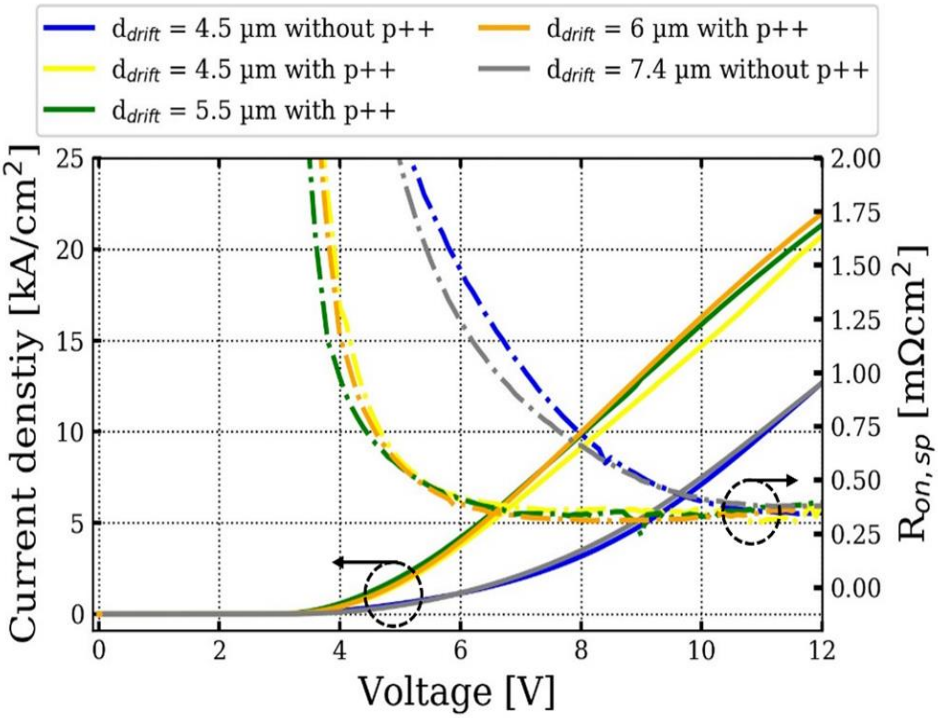


Figure 4-10 : 20 µm diode diameter Forward J-V characteristics and Ron,sp of GaN-on-Si P-i-N diodes with varying drift layer thicknesses, with and without a p++ cap layer, show a notable reduction in threshold voltage when the p++ cap layer is employed.

For a more in-depth analysis of the on-state behavior of the diodes, I(V) and Ron(V) measurements were conducted at various temperatures (Figure 4-11.a and b). Elevated temperatures slightly decrease Vth and enhance the current spreading due to increased thermal diffusion of carriers and narrowing of the bandgap. However, in the second regime (beyond 12 V), the degradation of Ron is more pronounced at high temperature, confirming the thermal dissipation challenges associated to the pseudo-vertical design. Increasing the thickness of the n+ layer can mitigate the thermal dissipation issue, but at the expense of an additional resistance resulting from the crowding effect.

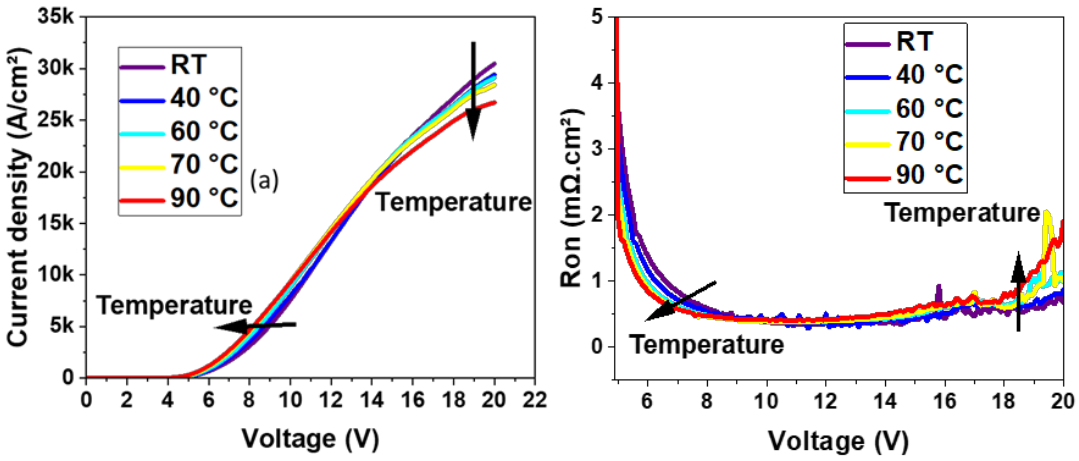


Figure 4-11 : (a) Forward current characteristics and (b) Differential on-state resistance measurements at various temperatures from the fabricated PIN diodes.

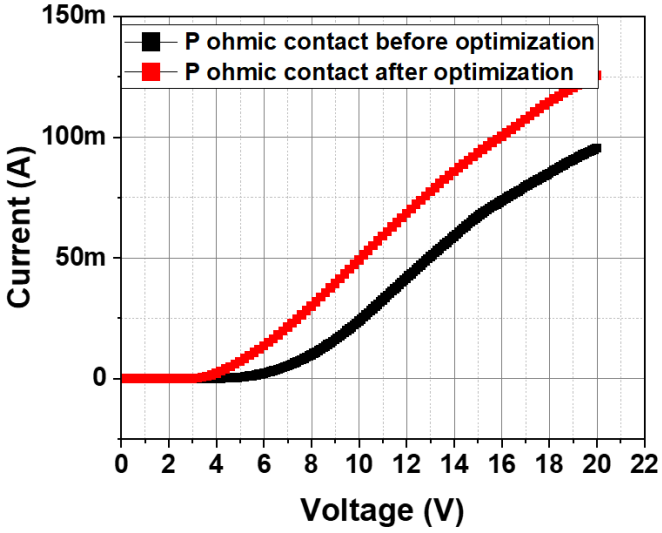


Figure 4-12 : Forward characteristics before and after P-type ohmic contact optimization

The results presented in this part were performed prior to the optimization of P-type ohmic contacts (described in the last chapter). Figure 4-12 shows the forward characteristics before and after the P-type ohmic contact optimization. The quality of the contact has a direct impact on the Vth. A reduction of the Vth from > +6 V to +4 V has been observed after optimization of this key parameter, while yielding a similar Ron.

Figure 4-13 displays the typical reverse J-V characteristics of the P-i-N diodes, and the breakdown voltage (BV) extracted at a current density of 1 A/cm^2 for various drift layer thicknesses. The breakdown voltage shows a linear increase with the drift layer thickness, with an average breakdown field (VB/drift) of approximately 1.7-1.8 MV/cm. Using the analytical equation for a punch-through design, the critical electric field is estimated to be > 2.3 MV/cm, which is lower than the theoretical value of 3.3 MV/cm for GaN. This discrepancy arises because the approximation does not account for electric field peaks at the electrode edges. However, optimized sidewall treatment effectively suppressed sidewall parasitic leakage current.

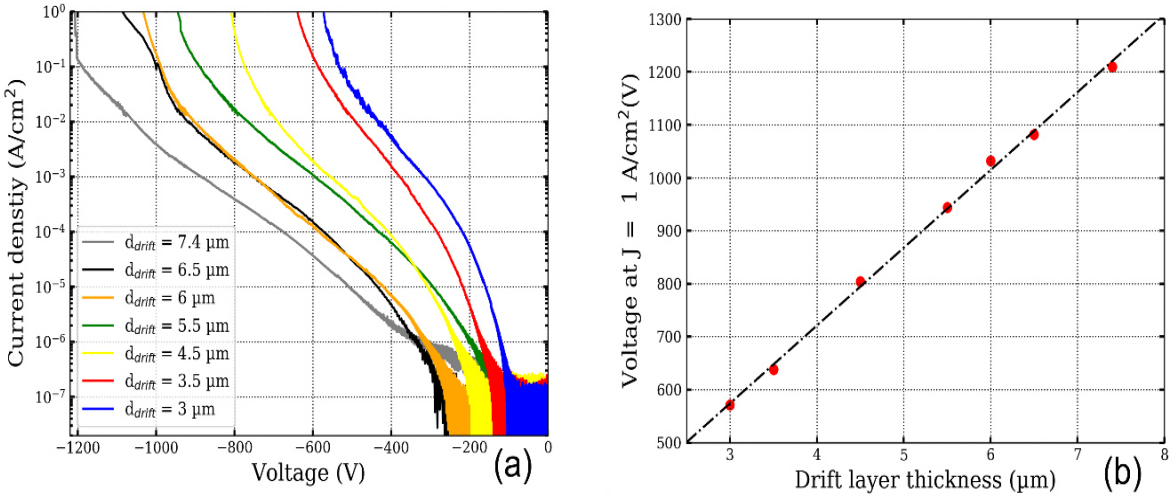


Figure 4-13 : (a) Reverse J-V characteristics of GaN-on-Si P-i-N diodes with various drift layer thicknesses. (b) Breakdown voltage (measured at J = 1 A/cm^2) as a function of the drift layer thickness for 100 µm diode diameter.

Interestingly, the leakage current for a given voltage decreases with increasing drift layer thickness. The P-i-N diodes with a 7.4 µm thick drift layer exhibited a remarkably low leakage current, reaching 1 µA/mm^2 at around 650 V. This performance is significantly better than previously reported GaN-on-Si and GaN-on-sapphire P-i-N diodes, indicating excellent material quality and effective sidewall leakage suppression. It is generally believed that leakage current in GaN-on-Si PN diodes is dominated by variable range

hopping and space charge-limited current, both of which depend on the electric field. The electric field at the P-i-N junction increases more rapidly with increasing bias for thinner drift layers due to a faster transition from a non-punch-through to a punch-through electric field distribution, leading to higher leakage currents. However, to fully understand the dominant leakage mechanism, temperature-dependent J-V characteristics would be necessary, which is beyond the scope of this work.

Nonetheless, this study demonstrates that increasing the drift layer thickness reduces leakage current, and high TDD does not pose a significant issue.

4.5 Temperature dependence assessment of the avalanche breakdown on 800 V and 1200 V vertical GaN-on-Si P-I-N

4.5.1 Device structure and process

In this section, 4.5 µm pseudo vertical and 7.4 µm fully vertical PIN diodes previously described (4.4.1) are further studied versus temperature to assess the avalanche capability of the device.

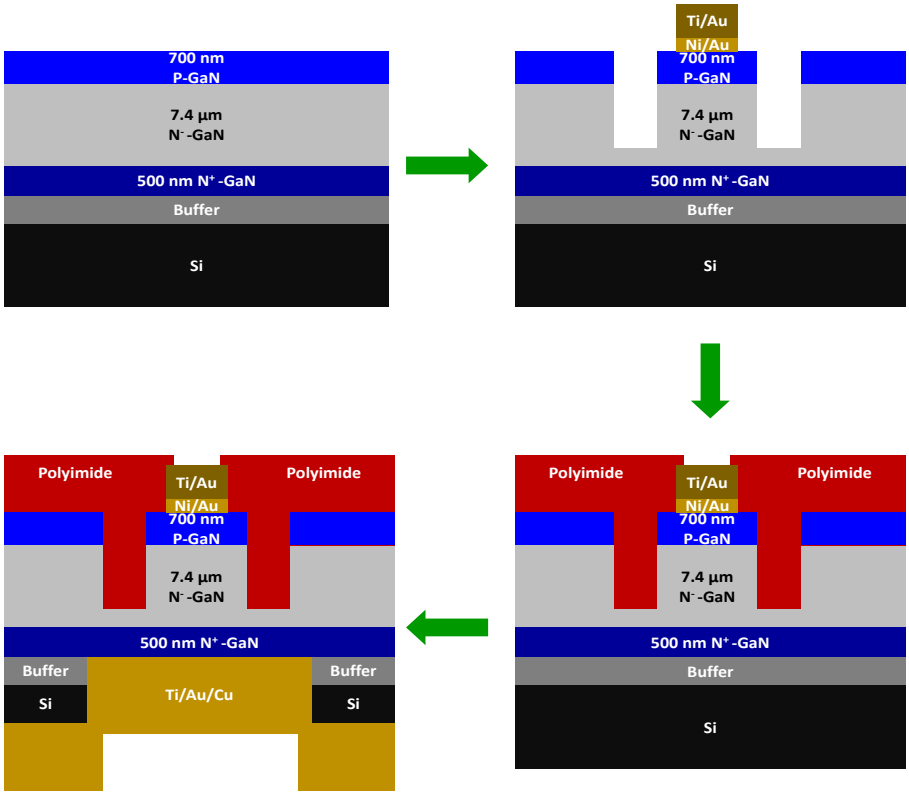


Figure 4-14 : Schematic cross section of fully vertical PIN diode fabrication process flow.

Fabrication and growth process were already detailed in the previous part of the thesis (see Sections 4-6 and 4-7). Figure 4-14 summarizes the fabrication process steps of the 7.4 µm fully vertical structure, while Figure 4-15 shows a cross-sectional image of the vertical 7.4 µm P-I-N diodes obtained using focused ion beam (FIB) imaging.

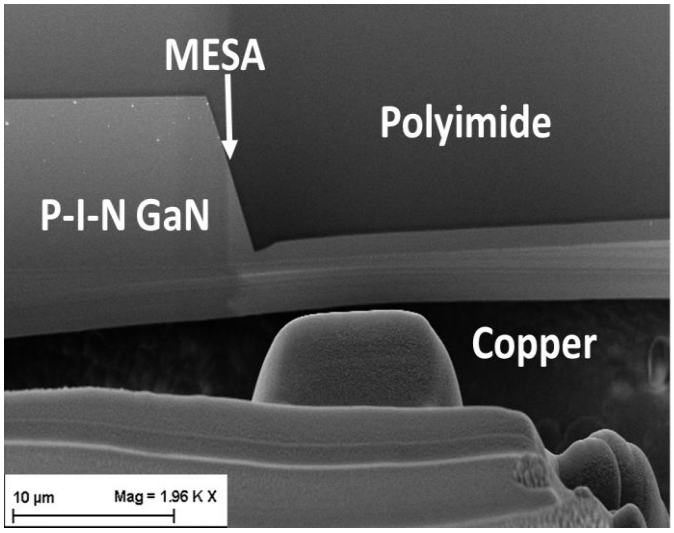


Figure 4-15 : Focused ion beam cross section image of the GaN-on-Si vertical diodes

4.5.2 Temperature dependence of off-state characteristics: avalanche assessment

4.5.2.1 Pseudo vertical P-i-N diode with 4.5 µm drift region

Typical reverse characteristics of the fabricated 4.5 µm pseudo vertical GaN-on-Si p-n diodes are shown in Figure 4-16. The diodes exhibit a high blocking capability (BV) above 800 V, corresponding to a high electric field at the p-n junction of 2.3 MV/cm. This translates to an average electric field across the drift layer close to 2 MV/cm. Moreover, a uniform breakdown voltage across the sample was observed with similar values as a function of the anode sizes (up to 1000 µm diameter). Further improvement of the edge termination process may allow withstanding an even higher critical field. Low leakage current density is observed to be below 10^{-1} A/cm^2 all the way to 700 V. This is a strong indicator of the good material quality as well as the reduction of sidewall parasitic leakage current achieved through the optimized mesa etching step. Additionally, it provides solid evidence of low electrically active dislocations within the structure (although this has not

yet been assessed). Figure 4-16.b shows a zoom around the breakdown of leakage current for reverse biased p-n diodes with a temperature variation from room temperature up to 100°C. It can be pointed out that the diode survived many voltage sweeps up to 800 V suggesting avalanche capability. A clear avalanche breakdown signature is observed, as the blocking voltage increases with temperature. This is the first demonstration of avalanche capability in 800 V-class P-i-N diodes resulting in a state-of-the-art BFOM of approximately 2 GW/cm^2 and thus represents a key feature that highlights the potential of vertical GaN-on-silicon heterostructures for power electronics. These results pave the way for medium voltage vertical GaN-on-Si based power devices.

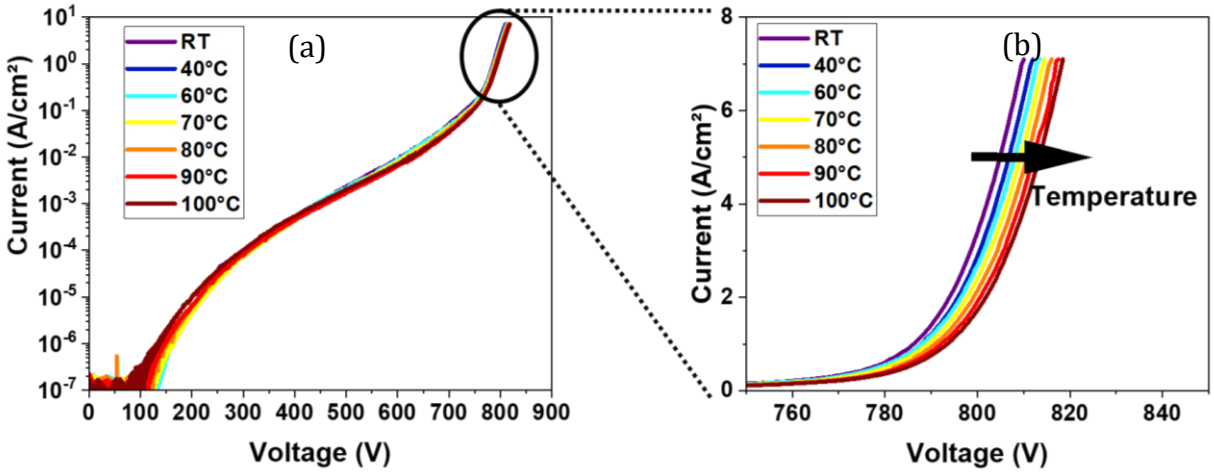


Figure 4-16 : Temperature dependence of pseudo vertical GaN-on-silicon 4.5 µm PIN diode reverse characteristics (b) Zoom of the breakdown region indicating the increasing of the breakdown with temperature thickness for 100 µm diode diameter

4.5.2.2 Fully vertical P-i-N diodes with 7.4 µm drift region

Figure 4-17 presents the reverse characteristics of 7.4 µm fully vertical P-i-N diodes with various anode size (from 50 µm to 1000 µm). We can observe a uniform breakdown voltage > 1200 V. The increase of diode diameter does not affect both the leakage current and the breakdown voltage. This reflects the high growth and processing quality as larger area potentially involves more defects through the heterostructure or the mesa sidewalls.

Figure 4-18 plots typical reverse characteristics of the 7.4 µm fully vertical GaN on Silicon P-i-N diodes at various temperatures. At room temperature, a high breakdown voltage of 1230 V and low leakage current are observed. The P-i-N diode breakdown voltage translates to a high critical electrical field at the junction (> 2.2 MV/cm) with an average

electric field across the drift layer of 1.66 MV/cm. No additional leakage path was induced by the device processing owing to the optimized deep mesa etching [5]. Moreover, the P-i-N diode exhibits a soft breakdown, hinting at the avalanche capability. It can be pointed out that this is an essential feature for the industrialization of these new types of devices.

(a)

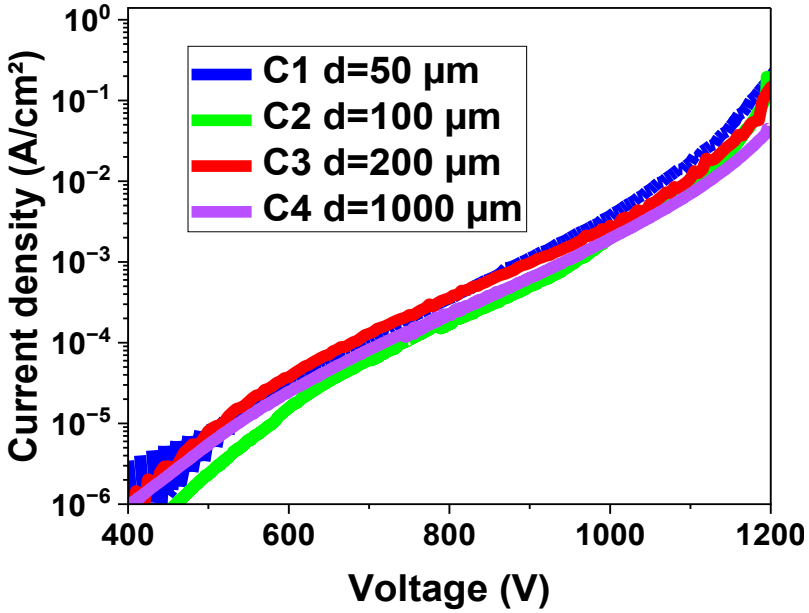


Figure 4-17 : thickness for 100 µm diode diameter Reverse characteristics of fully vertical PiN diodes with various anode size for 7.4 µm drift layer thickness

(b)

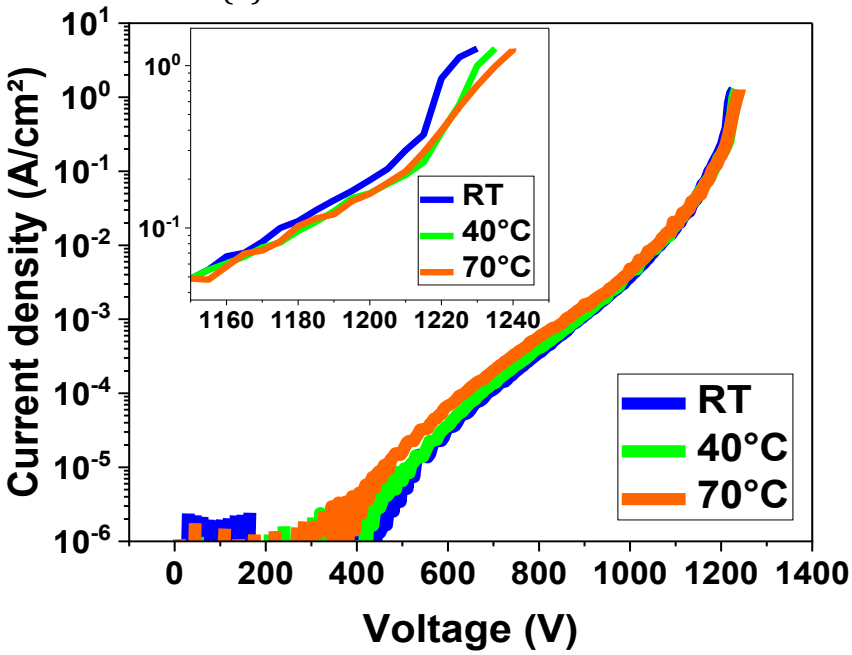


Figure 4-18 : 100 µm diode diameter Typical reverse characteristics of fully vertical P-i-N diodes at various temperatures of the fully vertical 7.4 µm PiN diode

The avalanche breakdown provides indeed a safe leakage current path that protects the devices from irreversible damages. In this case, the leakage current is induced by the impact ionization of the accumulated carriers when exceeding a specific energy. Increasing the temperature causes a delay in the onset of impact ionization due to phonon scattering. Therefore, a higher reverse bias is needed at higher temperatures to achieve the same energy level. In other words, when the temperature increases, the soft breakdown voltage increases as seen in Figure 4-18 showing the temperature dependence of BV, which were measured on the exact same device for each temperature, confirming the signature of the avalanche capability slightly above 1200 V.

4.6 Comparison of fully and pseudo vertical performances

4.6.1 Device structure and process

In this part, the fully vertical and pseudo vertical 4.5 µm P-i-N on state characteristics are compared. Both pseudo and fully vertical (Figure 4-19.a, b and c) have been fabricated on the same wafer allowing a proper and direct comparison without any growth and processing variation (see chapter 3).

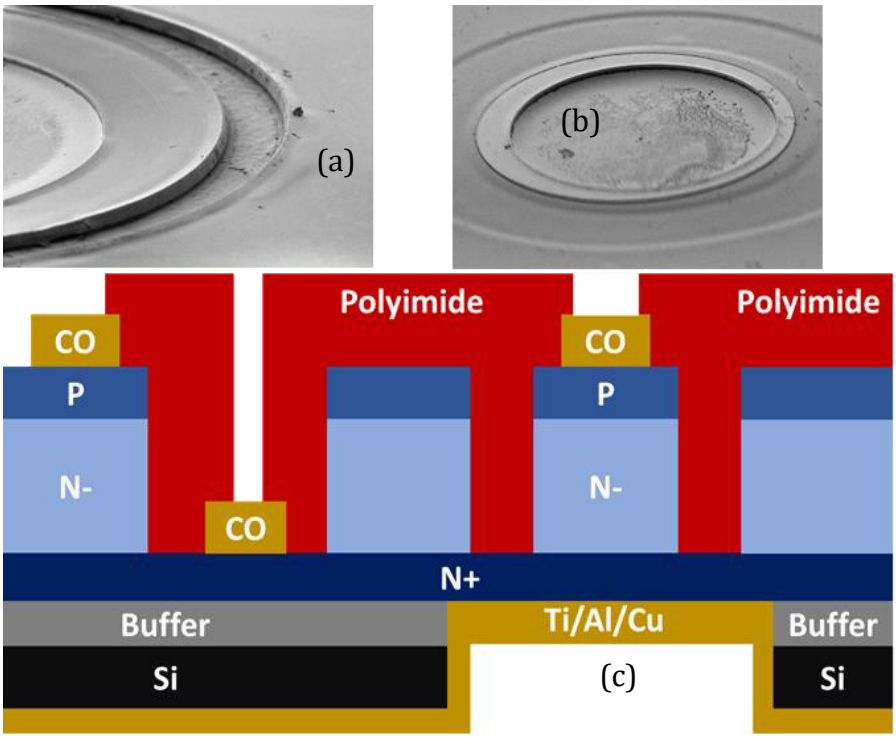


Figure 4-19 : 100 µm diode diameter SEM image of PV (a) and FV (b) GaN-on-Si P-i-N diodes. (c) Schematic cross section of Pseudo vertical and Fully vertical GaN-on-Si P-i-N diodes on the same sample

4.6.2 Results and discussion

Regardless of the size, the fully and pseudo vertical GaN-on-Si diodes show similar high blocking capability with an average hard breakdown of 820 V (Figure 4-20.a) corresponding to a critical breakdown field close to 2.3 MV/cm despite the absence of field plates. A uniform breakdown was also observed on large diodes (anode diameter = 1 mm). The leakage current density is quite low compared to the previously reported GaN-on-Si P-i-N diodes from the literature, which reflects the high material and processing quality such as the reduction of sidewall leakage and electrically active dislocations through the GaN drift layer.

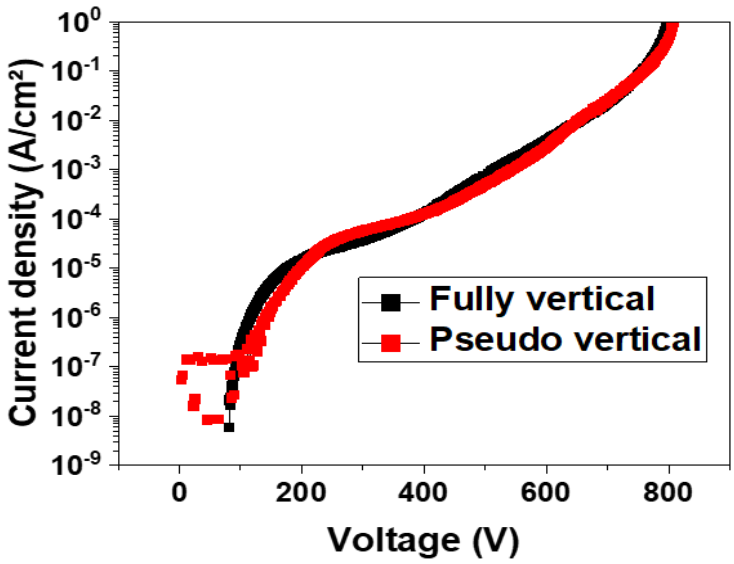


Figure 4-20 : Reverse characteristics of fully and pseudo vertical 4.5 µm drift thickness

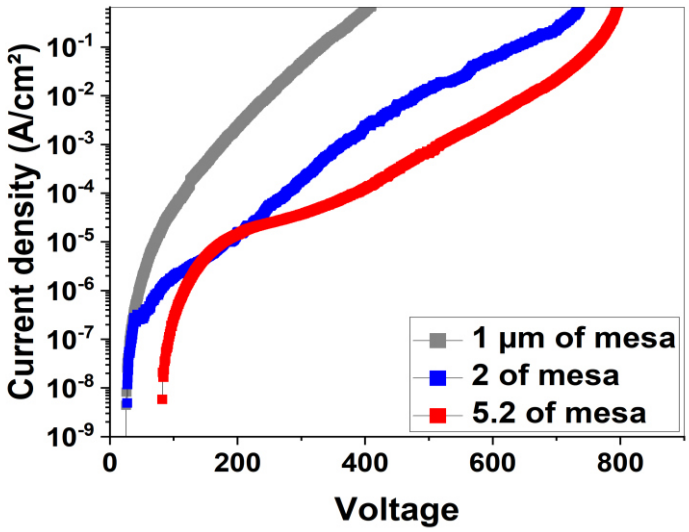


Figure 4-21 : off-state measurement of the fully vertical 4.5 µm P-i-N diode using various mesa etching depth

Figure 4-21 presents the off-state measurements of the fully vertical design using various mesa etching depths. These measurements are compared with the TCAD simulation results shown in Figure 3-15. The strong correlation between the experimental results and the TCAD predictions confirms the advantages of deep mesa etching and the effectiveness of TCAD simulations in predicting device performance, highlighting the benefits of a deep beveled mesa.

The forward characteristics of the pseudo and fully vertical 4.5 µm drift P-i-N diodes were evaluated. It is well known that current crowding effects occur in pseudo vertical configuration affecting the on-state current, especially in large diodes as illustrated in our TCAD simulations (Figure 2-13). This results in a degradation of the specific on-state resistance, which strongly increases with the diode size.

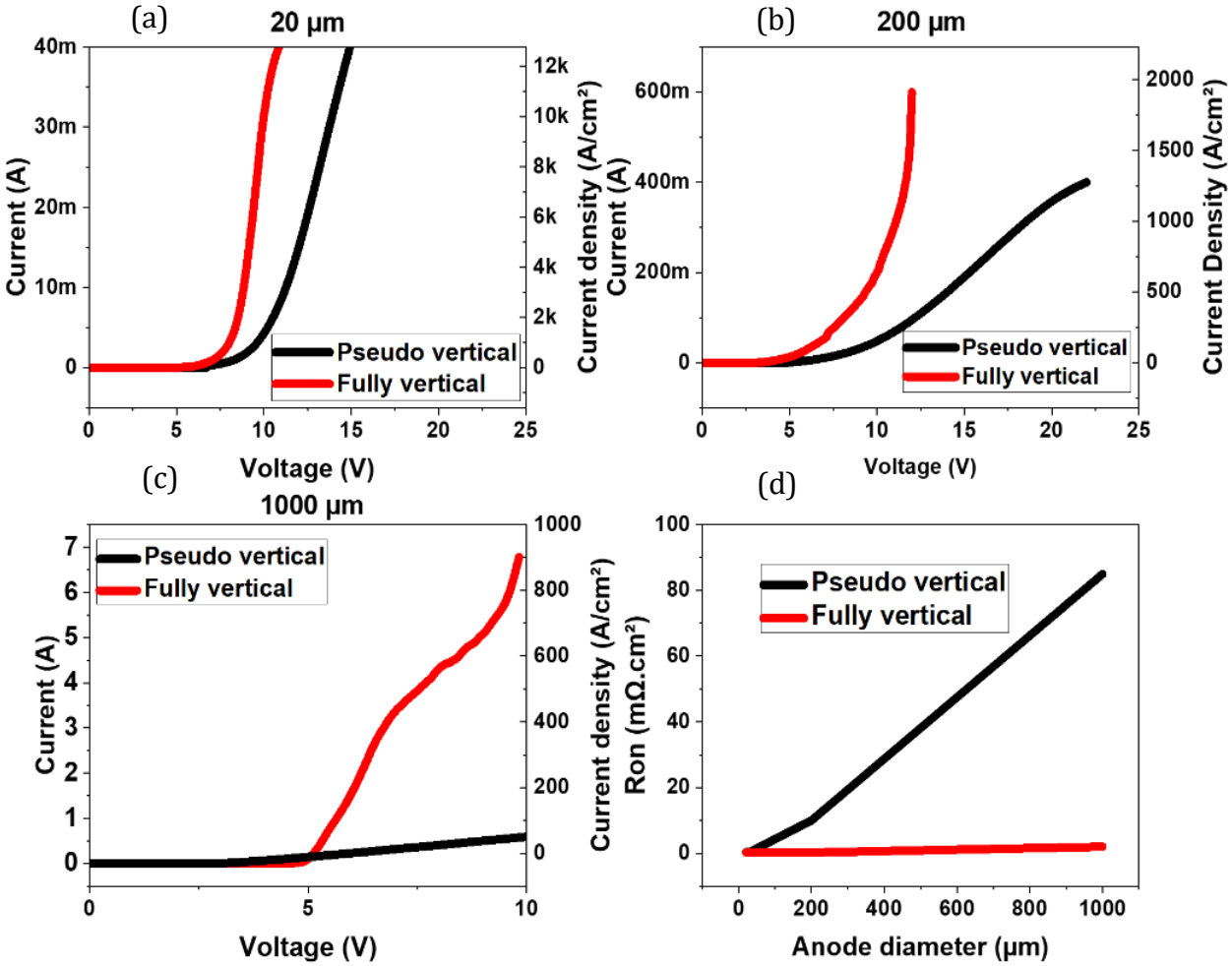


Figure 4-22 : (a) 20 µm, (b) 200 µm and (c) 1000 µm forward characteristics of FV and PV 4.5 µm vertical P-i-N diodes (d) Ron dependence on anode size.

Figure 4-22 shows the forward current and the corresponding differential R_{ON} of various diode sizes for both pseudo and fully vertical configurations. The devices exhibit a high current density with low differential R_{ON} < 0.35 mΩ.cm^2 for the pseudo vertical diodes against < 0.2 mΩ.cm^2 for the fully vertical diodes when using small device size. However, for larger diode size, R_{ON} degrades drastically in the case of pseudo vertical diodes (see Figure 4-22.d) to reach for instance 10 mΩ.cm^2 for 200 µm diodes. Unlike pseudo vertical diodes, R_{ON} remains extremely low (around 0.25 mΩ.cm^2) as a function of the diode size (up to 200 µm of diameter). The low R_{ON} in the fully vertical configuration is attributed to the suppression of the current crowding effect that scales with the device dimensions. This, in turn, enables high on-state current as seen from the 1000 µm diode diameter delivering 7 A at 10 V with low Ron < 2 mΩ.cm^2 for FV compared to PV Ron around 85 mΩ.cm^2 (Figure 4-22.c and d). It can be noticed that the 1 mm fully vertical P-i-N diodes are expected to generate even higher current level well above 10 A with a further optimized heat sink, as shown in the next study.

In this section, we investigated the potential of fully vertical GaN-on-Si technology. With a 4.5 µm thick drift layer, fully vertical GaN-on-Si large P-i-N diodes show high on-state current with low on-state resistance unlike pseudo-vertical diodes severely limited by current crowding effects.

4.7 Demonstration of high on-state current on 1200 V class fully vertical GaN on Silicon PiN diodes.

In this part, we combined the optimized process fabrication on the high quality 10 µm thick total epi-thickness enabled by the engineered buffer to demonstrate state-of-the-art fully vertical P-i-N diode with low Ron and high current > 10 A. Here we used the fully vertical P-i-N diode with 7.4 µm drift region thickness and 1200 V avalanche breakdown (see section 4.5)

Figure 4-23 shows the forward current density versus voltage characteristics and RON,sp of representative fully-vertical circular P-i-N diodes with various anode diameters. For small diodes (≤ 200 µm), CW DC measurements were performed while large 1 mm diodes were measured in pulsed mode with a duty cycle of 0.5% and a pulsed width of 1 ms. A similar threshold (Vth) of +5V was observed across all diodes by linear extrapolation. An

excellent on-state current scaling capability of the fully vertical diodes is observed with a current spreading ranging from 100 mA to 11.6 A at a voltage of 8.5 V. Figure 4-24.a shows the Ron,sp and related current density of different anode areas extracted from the I(V) measurements. For a small anode size (diameter = 50 µm), the Ron,sp is about 0.48 $m\Omega.cm^2$. When the diode size increases, a slight degradation of Ron,sp and current density was noticed. This is attributed to the thermal dissipation that can be further improved by optimizing the Copper heat sink at the n+ GaN bottom layer interface and the use of proper packaging. Nevertheless, the diodes deliver an unprecedented high current with more than 11.5 A for a 1 mm anode diameter (see Figure 4-24.b). To the best of our knowledge, this is the first demonstration of high current operation (above 10 A) for vertical GaN-on-Silicon devices.

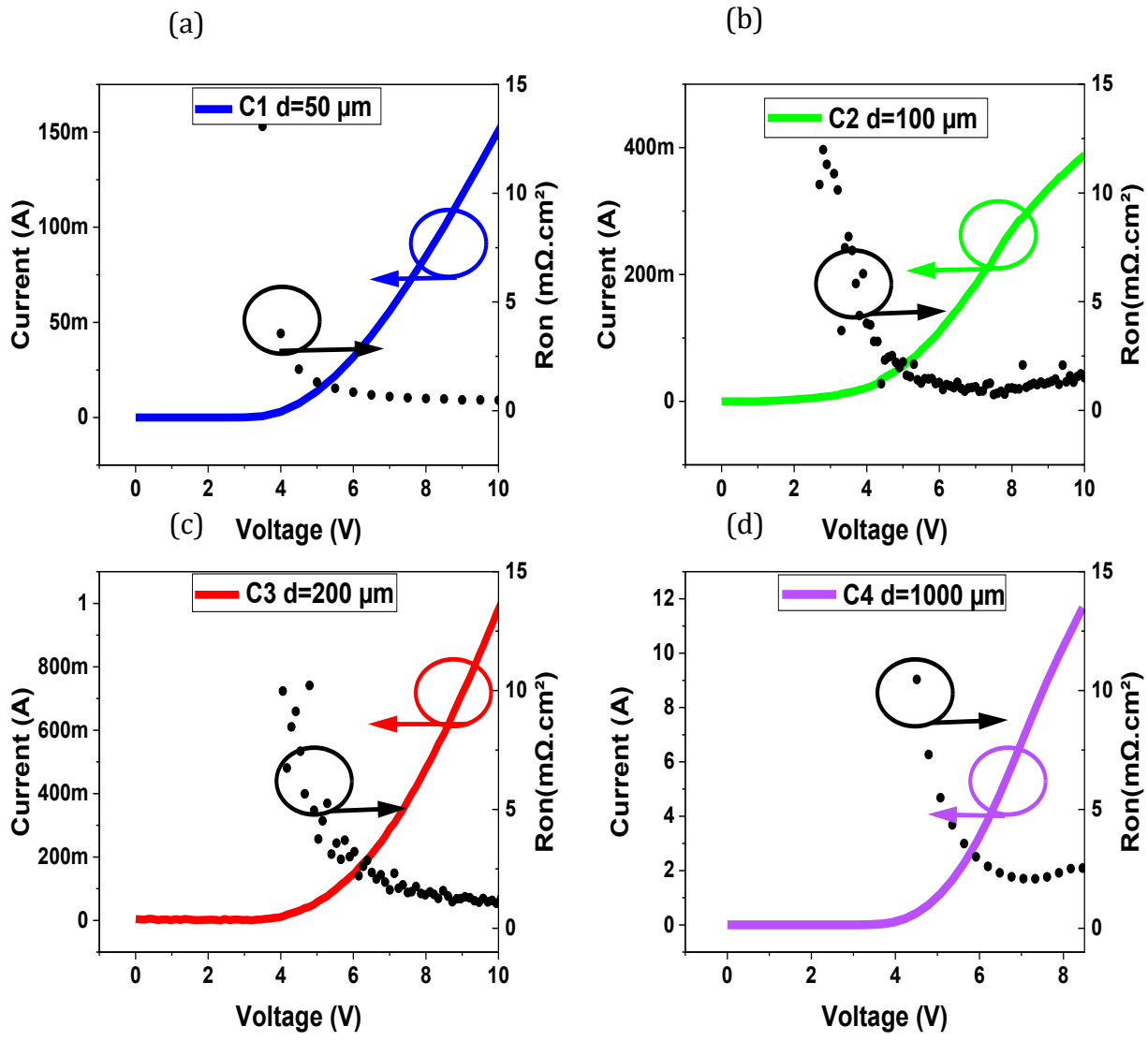


Figure 4-23 : Forward characteristics of fully vertical P-i-N diodes with various anode sizes (a) C1(d=50 µm), (b) C2(d=100 µm), (c) C3(d=200 µm) and (d) C4 (d=1000 µm)

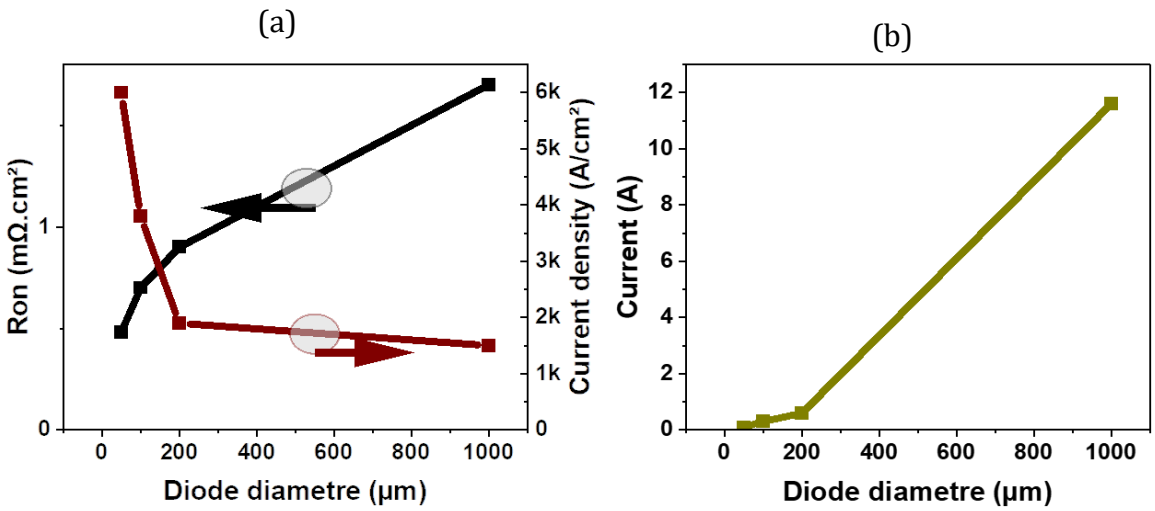
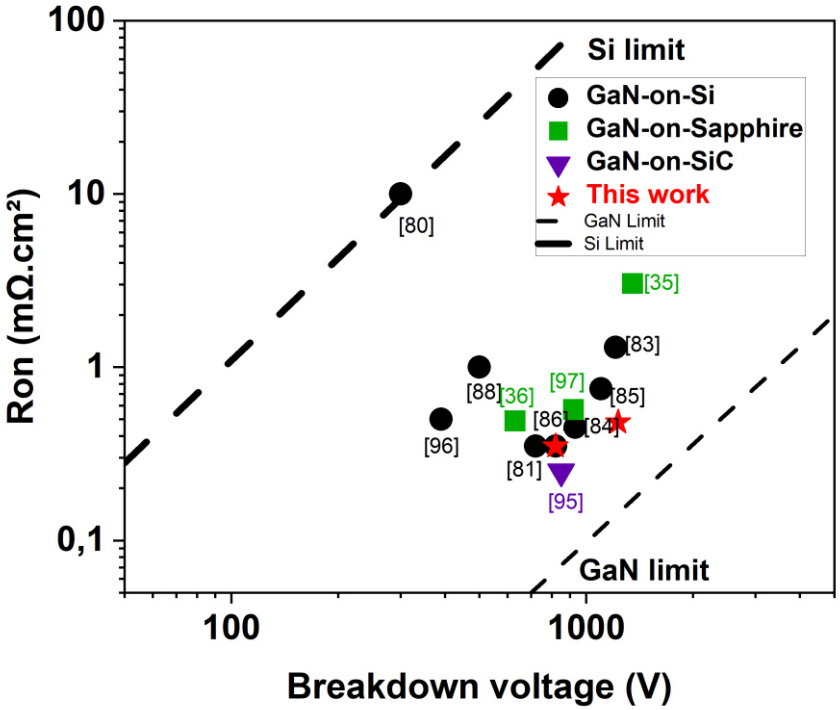


Figure 4-24 : (a) The extracted Ron, on-state current density and (b) Forward current measurement versus diode anode diameter at 8.5 V

4.8 Conclusion

This work demonstrates high quality fully vertical GaN-on-Silicon P-i-N diodes with state-of-the-art performances. While achieving 1200 V blocking voltage, the demonstrated diodes exhibit an avalanche soft breakdown signature and deliver high on-state current (> 10 A) despite a thermal management that could be further improved with the use of an optimized heat sink and proper packaging. Figure 4-25.a benchmarks the fabricated diodes with reported pseudo and fully vertical GaN-on-foreign substrate P-i-N diodes from the literature using Baliga figure of merit (BFOM). The demonstrated fully vertical diodes in this work deliverer a BFOM of 4 GW/cm^2 for the 4.5 µm PiN diodes and BFOM of 3.17 GW/cm^2 for the 7.4 µm PIN diodes, which is superior to the reported vertical GaN P-i-N diodes on foreign substrates. Furthermore, Figure 4-25.b highlights the outstanding performance combining both 1200 V blocking voltage and high on-state current as compared to the reported fully vertical GaN-on-Silicon devices. It should be specified that the main drawback for the pseudo vertical architecture is the Ron degradation when increasing the anode size due to the current crowding effect. That is why the reported pseudo vertical diodes typically employ small anode sizes to extract the Ron, which results in limited on-state current. This makes the use of fully vertical configuration mandatory for large anode sizes.

(a)



(b)

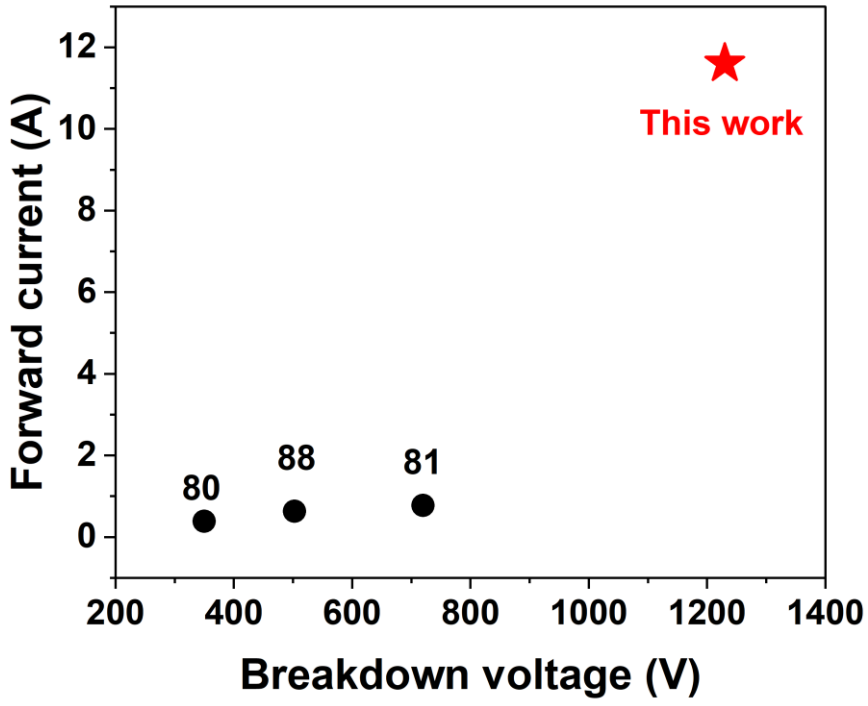


Figure 4-25 : (a) Benchmark of fully and pseudo-vertical small GaN-on-foreign substrate PIN diodes. (b) Benchmark of on-state current versus breakdown voltage of fully vertical GaN on Silicon PIN diodes.

In addition, a signature of avalanche soft breakdown capability is demonstrated for the first time for GaN on silicon substrate devices. During this work, multiples goals have been reached fully vertical heterostructures such as :

- Optimization of vertical GaN-on-Silicon diode design using TCAD simulations.
- Development of high-quality processing.
- Assessment and optimization of the backside N-face ohmic contacts.
- Comprehensive comparison between pseudo-vertical and fully vertical architectures.
- Demonstration of high on-state current with large diode dimensions.
- Demonstration of avalanche capability up to 1200 V voltage operation.

These promising results show the significant potential of cost-effective GaN-on-Silicon devices for medium voltage power electronic applications; currently not reachable by GaN-based devices grown on large diameter silicon substrate such as standard lateral HEMTs or pseudo-vertical devices.

Most of the process bricks developed during this work are transferable to vertical transistors such as the trench MOSFET. In the next chapter, we will present some initial results of fully vertical trench MOSFETs fabrication based GaN on Silicon substrate.

Chapter 5: Development of GaN on Silicon MOSFETs : Road to fully vertical transistors

In the previous chapter, we demonstrated high-quality vertical GaN-on-silicon P-I-N diodes with superior and reliable performance as compared to GaN on other foreign substrates. This includes excellent on-state current > 10 A, a high breakdown voltage > 1200 V, low on-resistance (Ron), and avalanche capability. These results clearly indicate that the process and growth quality are sufficiently mature to consider more complex device architectures such as transistors. This combination of techniques can be readily adapted to other types of vertical devices, particularly those involving deep bevelled mesa structures and backside processing, such as N-polar ohmic contacts. In this chapter, we will present some initial results of a vertical transistor using GaN-on-silicon technology, specifically focusing on a trench MOSFET design.

5.1 Structure design

As discussed in the first chapter, the transistor structure includes an additional N+ doped layer compared to the diode, forming an N+/P/N-/N+ junction. This type of transistor primarily relies on a field-effect, three-terminal design comprising the gate, drain, and source[2], [3]. The current flows from the source to the drain, controlled by the gate, as illustrated in Figure 5-1.

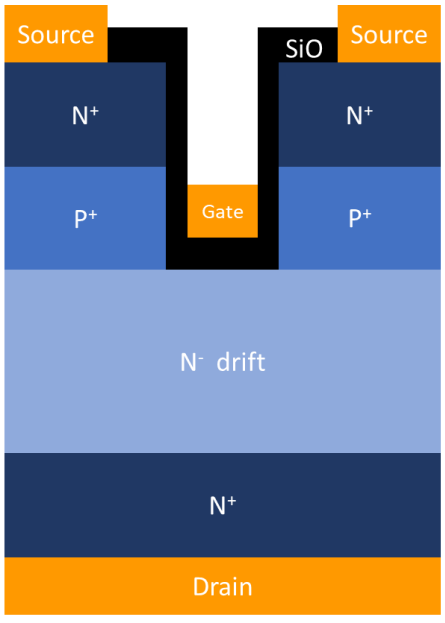


Figure 5-1 : Vertical GaN on Silicon TMOSFET.

Vertical transistors device design must carefully consider parameters such as the position, thickness, doping levels, and shape of various layers for achieving optimum performance. Electrons in vertical structures originate from the source and flow through the inversion P-layer (see Figure 5-2). To eliminate the JFET current, it is more suitable to use a trench gate structure[159]. The P-layer should be sufficiently doped to establish a substantial threshold voltage, as it forms a P-I-N junction that withstands the applied voltage. Furthermore, due to the differences in doping concentrations, the depletion region extends into the drift region, effectively blocking leakage current in the off-state (when no voltage is applied to the gate). After crossing the P-layer, electrons disperse into the drift region, which should be lightly doped to allow electron flow. However, the doping level in the drift region must be lower than that of the P-layer to maintain blocking voltage capability. If the drift region is too heavily doped, it will reduce the breakdown voltage by increasing the likelihood of impact ionization[160].

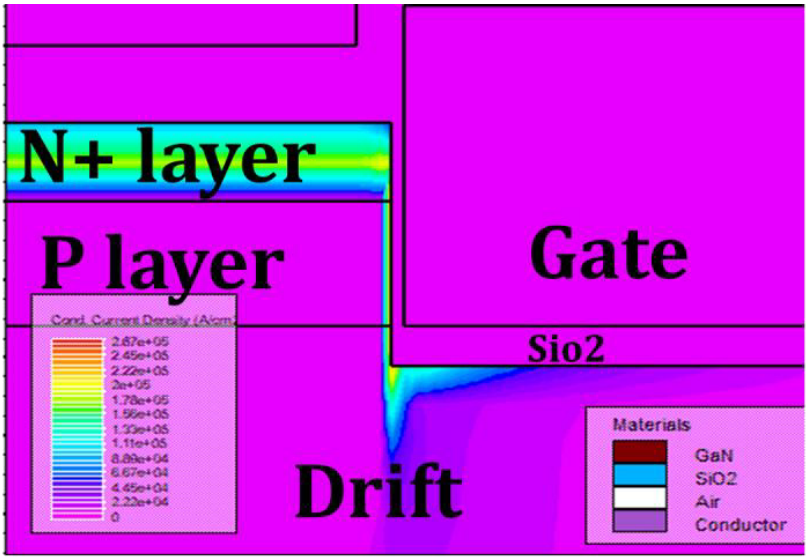


Figure 5-2 : Inversion channel created within the P layer

To summarize, all the parameters taken into consideration in this work appear in the following table. In the next section, we calibrated a simulation model experimental results from the literature corresponding to the first vertical GaN MOSFETs on silicon substrate, see reference [161]. This enables to highlight the limitations of this structure and explore solutions that could help optimizing the performances.

Parameter	Consideration
Gate shape	U-Trench gate with different angle of the sidewalls.
Gate position	In the middle of the structure.
Oxide thickness	Sufficient to have positive Vth, and to withstand the high electric field
N+ source/drain doping and thickness	Sufficient to have a good ohmic contact.
N+ source/drain position	Between source and P+ layer and the gate/ below the drift region
P layer doping thickness	Sufficient to have a positive Vth, larger than the drift region doping
P wall doping and position (If existed)	Larger than the drift region, near the gate otherwise this will create electrons trapping problems.
P wall thickness	Sufficient to block the current and guide the flux of current
Drift region thickness	It depends on the application; the larger thickness the higher breakdown but at the expense of Ron
Drift region doping	Sufficient to have a small Ron without impacting the performance.
Ron	the sum of the resistors in series (source and drain contact, channel, accumulation below the gate, drift region)

As initial studies, the T-MOSFET epi-design from the bottom to the top is as fellow:

- A 800 nm of N+ layer with a doping of 5×10^{18} cm^{-3}
- A 4000 nm of N- drift layer with a doping of 1×10^{16} cm^{-3}
- A 300 nm of P layer with a doping of 5×10^{19} cm^{-3}, corresponding to 3×10^{17} cm^{-3}
- A 200 nm of N+ layer with a doping of 5×10^{18} cm^{-3}

Additionally, the trench width has been set to 10 µm, with a 10 µm distance maintained between the source and gate. To avoid peak electric fields near the P/drift region and the JFET channel, the trench depth must exceed 600 nm. The gate oxide thickness within the trench has been fixed at 40 nm.

Using Silvaco TCAD tools and the same physical parameters outlined in chapter 2, the off-state and on-state characteristics of the TMOSFET were analyzed. Theoretically, the TMOSFET should achieve a breakdown voltage similar to that of a P-I-N body diode. For a 4 µm drift region, the estimated breakdown voltage is around 720 V (see Figure 4-13). However, the simulation predicts a lower breakdown voltage of 600 V, as shown in Figure 5-3. This discrepancy can be attributed to the modification of the electric field caused by the trench gate. Figure 5-4 illustrates the electric field distribution during the breakdown of the trench MOSFET, showing multiple peaks below the source within the body pn diode and within the oxide in the trench gate.

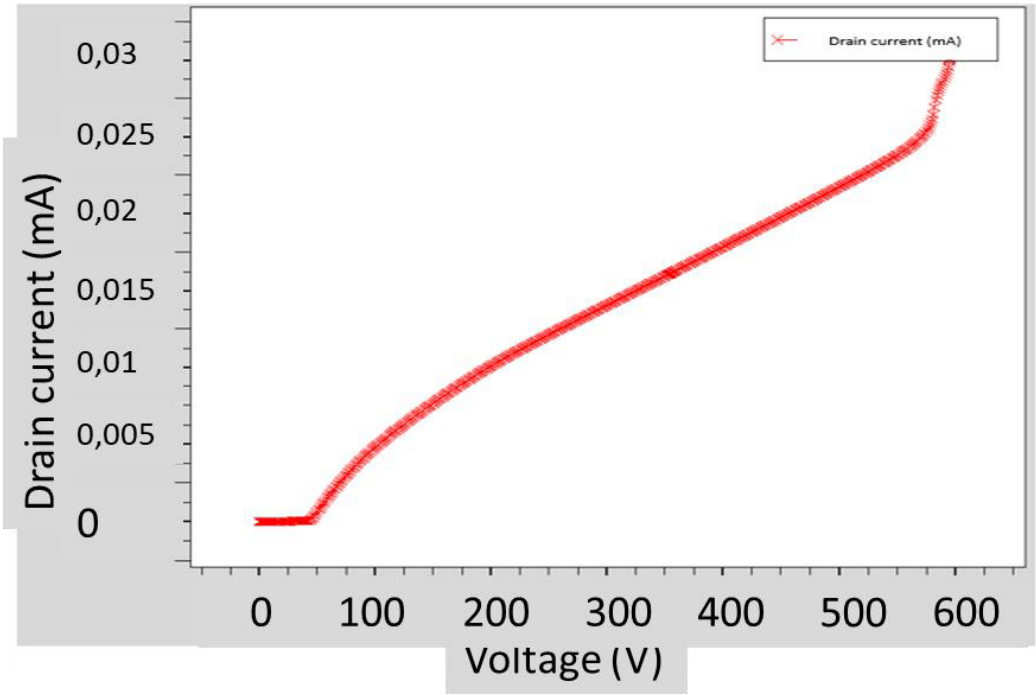


Figure 5-3 : Off state prediction by TCAD silvaco of the 4 µm TMOSFET breakdown voltage

We observe that the oxide layer withstands a maximum electric field of 5 MV/cm, a value that can be adjusted by varying the oxide thickness (Figure 5-5). To reduce the electric field, the oxide thickness can be increased. However, a careful trade-off must be respected between the breakdown voltage and the threshold voltage of the device, as a thicker oxide film will result in an excessive threshold voltage[125], [162].

The gate trench angle also affects the electric field within the oxide. As shown in Figure 5-6, decreasing the trench angle reduces the electric field. However, using a lower trench angle shifts the threshold voltage (Vth) and increases the on-resistance (Ron), as

illustrated in Figure 5-7. A vertical sidewall angle of the trench creates a 90° channel in the P-layer (Figure 5-2), enabling vertical charge transport between the source and drain. Additionally, after flowing through the channel, electrons accumulate beneath the gate, forming a region that facilitates charge transport. When the trench angle is larger, more electrons can accumulate beneath the gate, enhancing current injection[163].

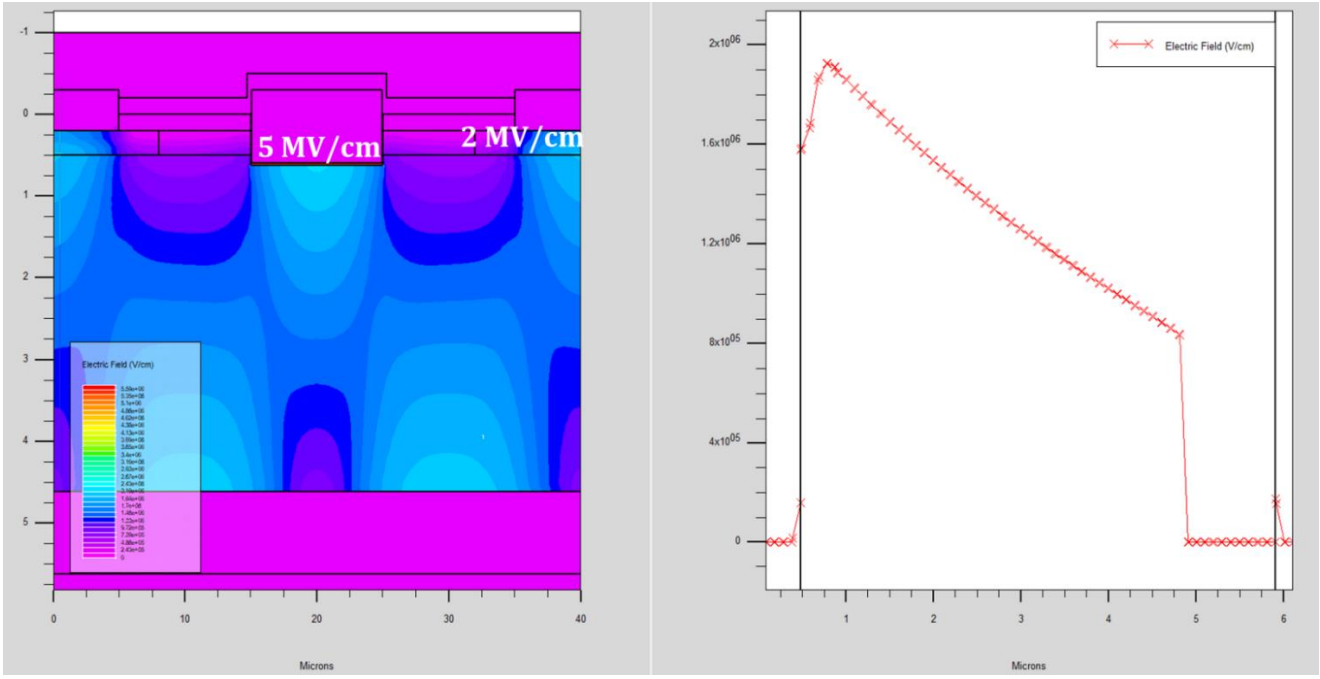


Figure 5-4 : Electric field distribution of the TMOSFET 4 µm drift region at the breakdown voltage.

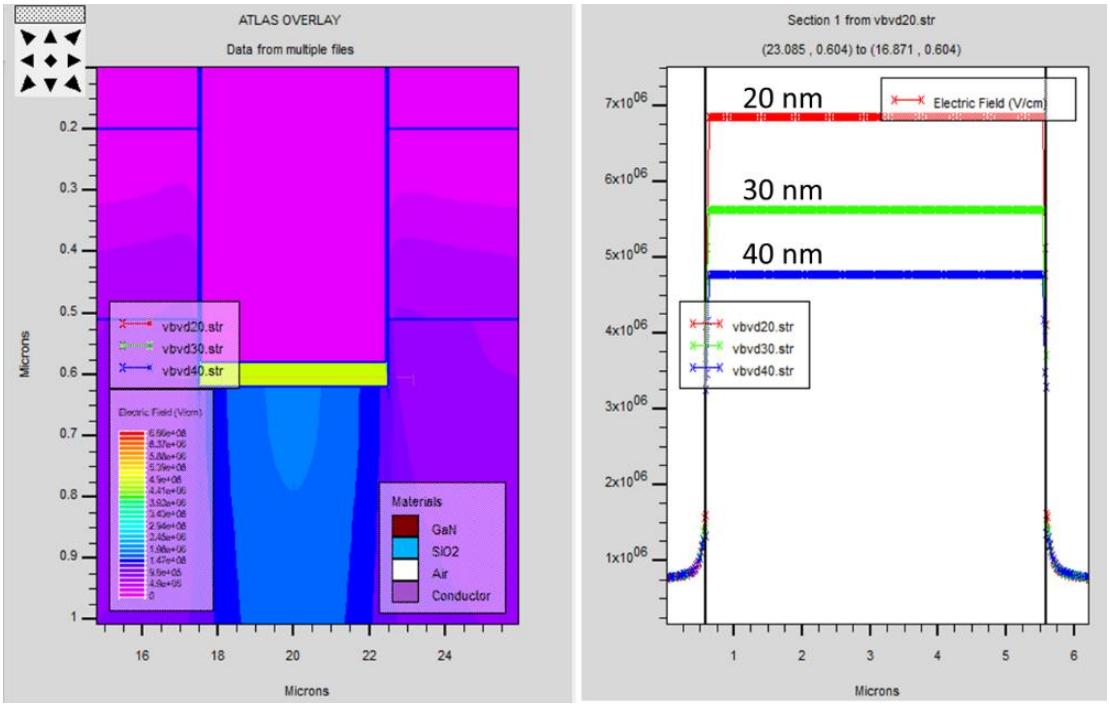


Figure 5-5 : Electric field dependence on the oxide thickness at the breakdown voltage

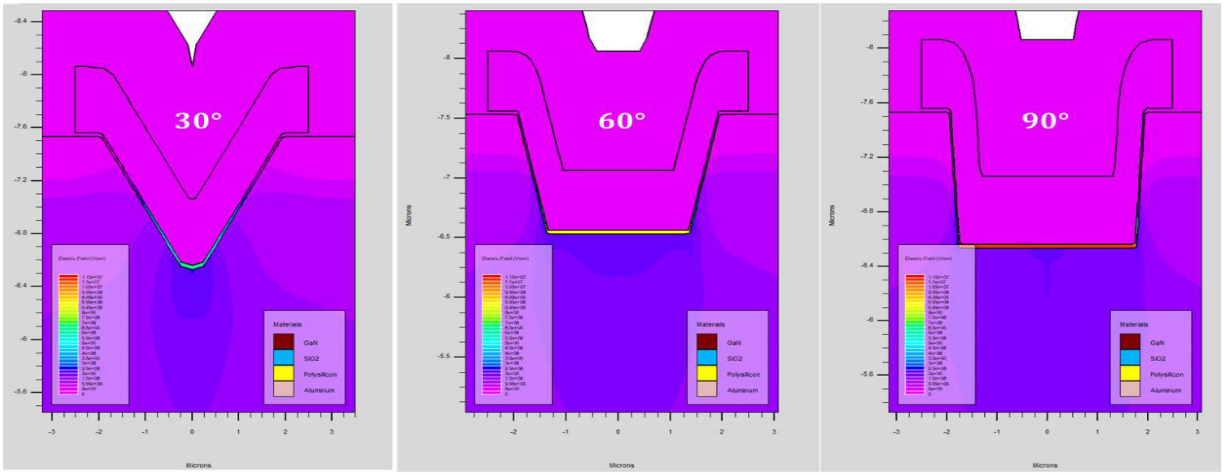


Figure 5-6 : Electric field dependence of the trench angle.

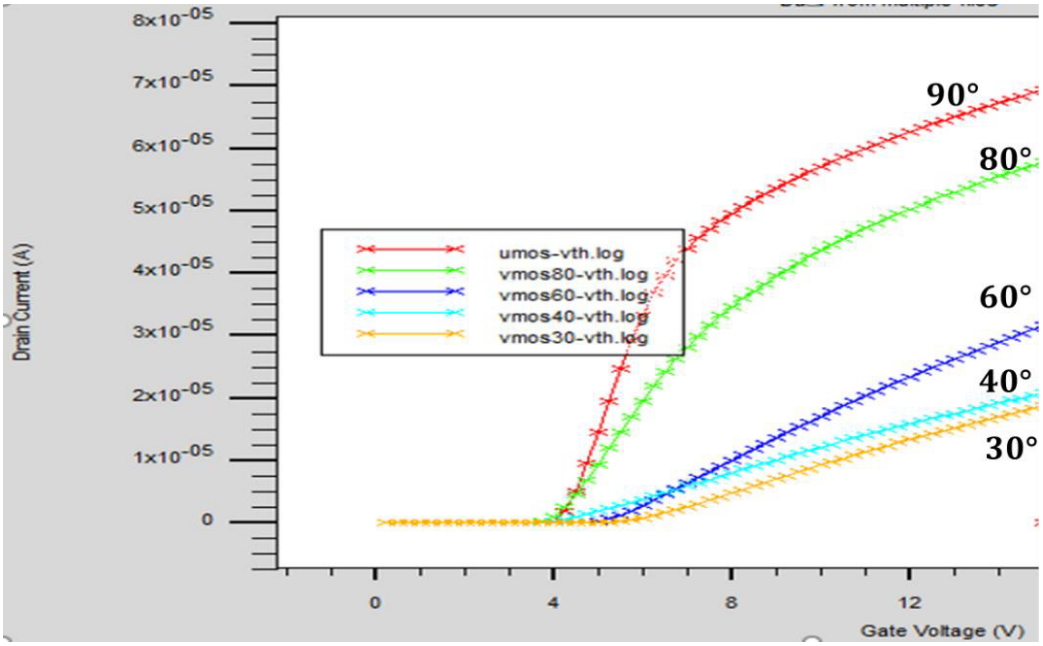


Figure 5-7 : on state characteristics comparison of TMOSFET with various trench angles.

The second parameter to consider in the off-state is the P-I-N body diode located beneath the gate, which must align with the studies discussed in chapter 2. Although the electric field peaks within the structure are lower than the critical field of both SiO_2 and GaN, breakdown voltage is still observed. To understand this, the ionization generation rate profile is plotted in Figure 5-8, showing a high rate near the trench edges. This suggests that breakdown occurs due to avalanche phenomena. Specifically, the high electric field near the gate increases the generation rate of charge carriers up to a certain voltage at which appears a current spike, as shown in Figure 5-8.

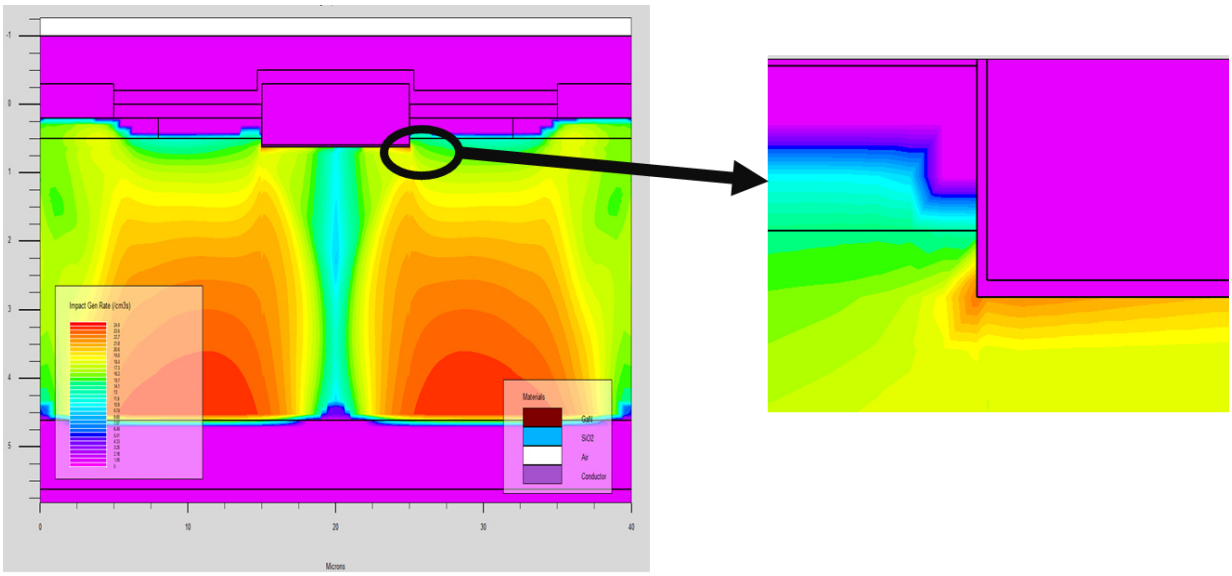


Figure 5-8 : Ionization impact generation rate distribution at the breakdown voltage

5.2 Preliminary development of vertical GaN-on-Silicon MOSFET

5.2.1 Fabrication process

As the final contribution of this work, a TMOSFET has been developed as a proof of concept. For this purpose, an N+/P/N-/N+ layer structure was grown on a 1.3 mm thick silicon substrate. The buffer layer used is similar to the one described in section 4.6.2.1, with a thickness of 1.5 µm. The structural parameters from top to bottom are as follows:

- A 800 nm of N+ layer with a doping of 5×10^{18} cm^{-3}
- A 3500 nm of N- drift layer with a doping of 1×10^{16} cm^{-3}
- A 500 nm of P layer with a doping of 5×10^{19} cm^{-3}, corresponding to 3×10^{17} cm^{-3} active doping
- A 330 nm of N+ layer with a doping of 5×10^{18} cm^{-3}

A pseudo-vertical design was chosen for this initial study. While several papers in the literature discuss the alignment of the trench gate along the a- and m-planes of the transistor [164], this aspect was not considered in this work, as the transistor has a circular design.

To fabricate the TMOSFET, a mesa was created using ICP etching to reach the N+ layer, similar to the mesa developed for the P-I-N diodes. The same mesa-etching recipe was applied to create a trench gate with a depth of 1.4 µm. A Ti/Al/Ni/Au stack was used as

the ohmic contact for both source and drain terminals, followed by an annealing process. A 100 nm SiO_2 layer was deposited using PECVD to serve as the gate oxide, and then a Ni/Au gate metal was deposited by evaporation.

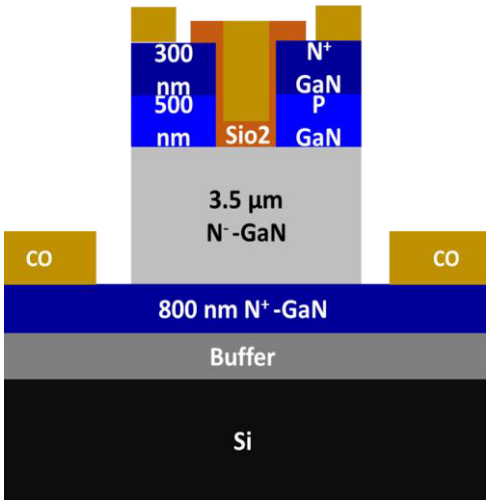


Figure 5-9 : schematic cross section of the fabricated TMOSFETs

Figure 5-9 illustrates the schematic cross-section of the fabricated transistor. Additionally, a focused ion beam (FIB) image was taken (see Figure 5-10), providing a detailed view of the vertical cross-section of the device. The trench gate has a length of 30 µm, with a distance of 20 µm between the gate/source and the source mesa.

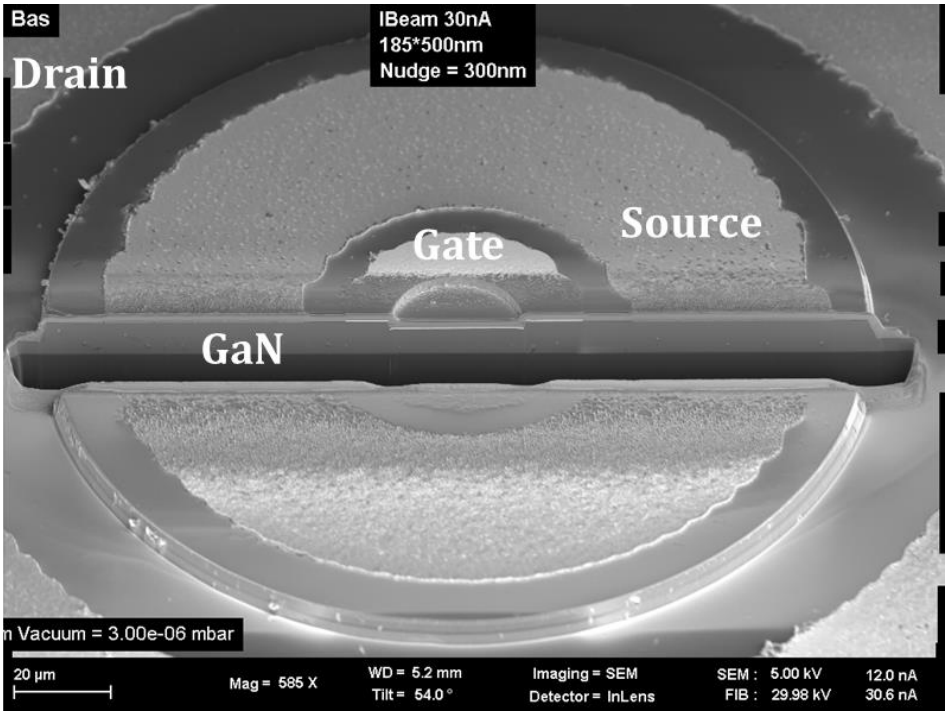


Figure 5-10 : FIB image of a vertical GaN on Silicon TMOSFET

5.2.2 Device characterization

Figures 5-11.a and 5-11. b display the output characteristics of the pseudo-vertical GaN-on-silicon TMOSFET. A positive threshold voltage of +5 V was extracted for the device(Figure 5-11.a), which aligns with expectations given the use of a thick SiO_2 layer as the gate oxide. However, the normalized current density, based on the trench area, is high even below Vth, indicating a potential design issue.

Regarding the drain-source current (Ids) versus drain-source voltage (Vds) characteristics, Figure 5-11.b shows the measurements for TMOSFETs with trench lengths of 30 µm and 15 µm. The gate-source voltage (Vgs) ranges from 0 to 20 V. A high current density, exceeding 2 kA/cm^2, is observed for both trench lengths. The larger trench exhibits quicker saturation compared to the smaller one, which can be attributed to the measurement issues due to props parasitical capacitance.

An on-resistance (Ron) of 1.5-2 mΩ·cm^2 was extracted for both pseudo-vertical TMOSFETs, suggesting high channel mobility. In fact, the channel resistance constitutes the largest portion of the series resistance within the MOSFET, which corresponds to the overall Ron of the device. To accurately determine the channel mobility, further optimization of the process is required to enhance the saturation behavior of the device [165].

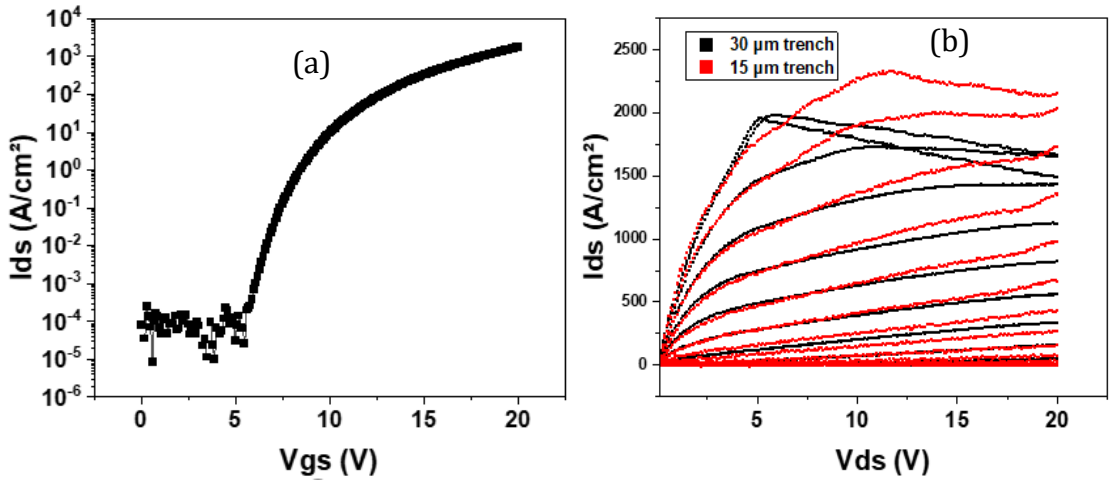


Figure 5-11 : (a) Ids(Vds) with a Vgs of [0;20V] and (b) Ids(Vgs) with Vds=10 V on-state characteristics of the pseudo vertical GaN on Silicon TMOSFET

Figure 5-12.a shows the off-state characteristics of the TMOSFET, where a breakdown voltage of 300 V was observed. As previously discussed, the off-state drain-source current

(Ids) is notably high, confirming the need for further process optimization. The current is normalized using the mesa area. The breakdown voltage is lower than predicted by the Silvaco simulation (Figure 5-12. b), which was estimated to be about 500 V for a drift layer thickness of 3.5 µm. Additionally, the P-I-N diodes using similar 3.5 µm drift layer delivered a high breakdown voltage exceeding 600 V with avalanche capability.

Given the identical growth conditions for both the P-I-N diodes and the TMOSFETs, the lower performance of the transistor is clearly attributed to the device fabrication. Most likely, the increased proximity of the high electric field to the surface due to the implementation of the trench gate is the one the root cause.

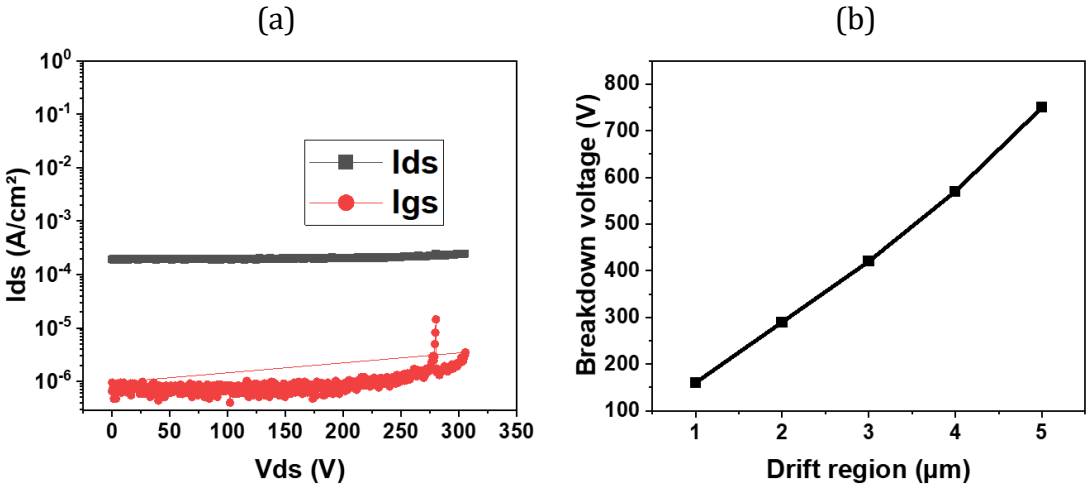


Figure 5-12 : (a) Typical off-state characteristics of the pseudo vertical TMOSFETs (b) Breakdown voltage vs drift layer thickness prediction using TCAD simulation

5.3 Potential improvement of vertical trench MOSFETs

The fabrication of the vertical GaN-on-silicon MOSFET represents the final contribution of this thesis, aiming to provide preliminary results that can be further enhanced through process and design optimization. In this context, several suggestions are proposed to improve the performance of these devices.

5.3.1 Process optimization

Figure 5-13 shows an SEM image near the trench gate of the pseudo-vertical TMOSFET, where the black-colored layer represents the SiO_2 layer. It can be observed that the oxide thickness on the planar surface (approximately 100 nm) differs from that on the sidewall (around 50 nm). This discrepancy arises from the non-uniform, or non-conformal,

deposition characteristics of PECVD, which result in varying thicknesses on different surfaces. To overcome this, alternative deposition methods like Atomic Layer Deposition (ALD) can be used. ALD provides a more uniform coating, even within trenches, and offers higher film quality because its longer deposition time allows for a denser and more consistent layer formation across all surfaces.

Another parameter to consider is the trench etching recipe. A rather rough surface can be observed on the trench sidewalls in Figure 5-13, caused by etching damage to the surface. This can be mitigated by using a low damage etching recipe or by smoothing the surface with a directional wet etching process following ICP etching of the trench. A commonly used solution for this purpose is TMAH (Tetramethylammonium hydroxide)[166], [167], [168], [169], [170].

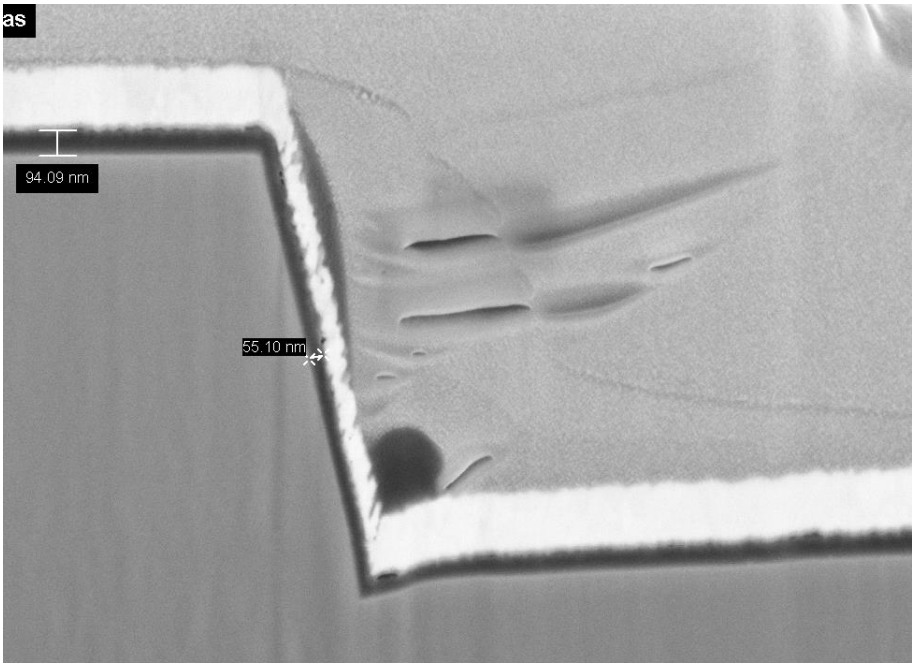


Figure 5-13 : SEM image of the pseudo vertical GaN on Silicon TMOSFET trench gate. The thickness of the oxide is around 100 nm on planar surface and 50 nm on the sidewalls of the trench.

In addition, polyimide passivation can be applied to both the mesa sidewalls and the trench gate, which could help reduce electrical field peaks at the edges and within the trench[171], [172].

As a final point and by analogy with the fully vertical P-I-N diodes (see Chapter 4), the on-state performance of the device can be enhanced by adopting a fully vertical architecture.

This approach would help reduce thermal dissipation issues and improve reliability by distributing the current vertically, thereby minimizing current crowding effects.

5.3.2 Design optimization

In this section, we demonstrate the effectiveness of the P-wall in minimizing leakage current under off-state conditions. The P-wall is a deep, highly P-doped layer located beneath the source and N-layer. With such a high doping concentration, the depletion region extends further into the drift region than in a standard structure, enhancing the current-blocking capability. Additionally, the deeper location of the P-wall shifts the high electric field away from the surface, thereby protecting the frontside contacts. To validate these theoretical considerations, TCAD simulations were conducted using Silvaco software, using the same model parameters as in previous simulations.

The simulated structure (Figure 5-14) retains the parameters of the initial design but includes two P-walls with a doping (hole) concentration of 10^{18} cm^{-3}, a width of 8 µm, and a thickness of 1 µm.

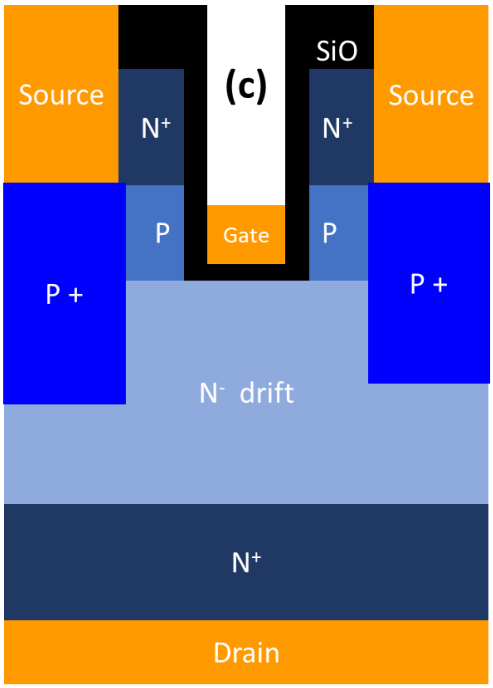


Figure 5-14 : Schematic of a P-wall TMOSFET, which are located below the source with a thickness of 1 µm

In off-state, the P-wall plays a crucial role, enabling a significant reduction of the leakage current while increasing the breakdown voltage (BV), as demonstrated in Figure 5-15.

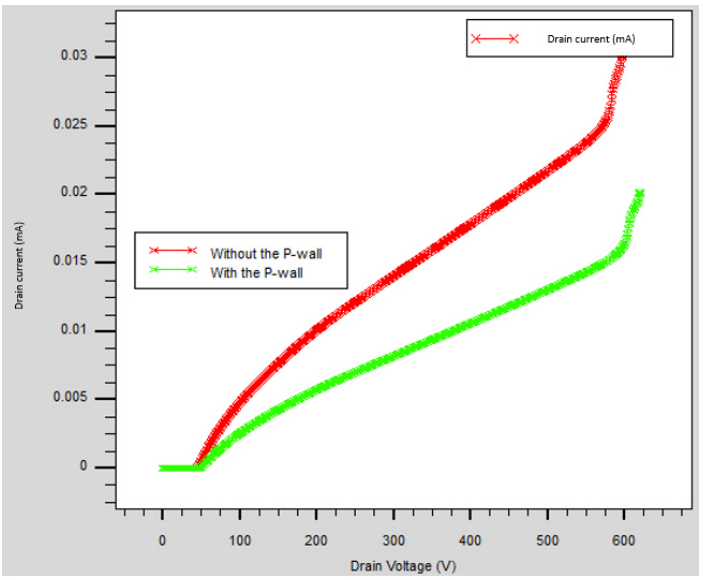


Figure 5-15 : Simulation of the BV of the UMOSFET (560V with I=25 µA) and P-wall TMOSFET(629 V and 15 µA)

Additionally, the peak electric field is now located at the P-wall/I-drift junction (Figure 5-16.a), enabling an enhanced critical breakdown field reaching approximately 2.4 MV/cm^2 (Figure 5-16.b), which is higher than the standard structure but does not adversely affect the device's reliability. The P-wall effectively shifts the peak electric field away from the front side, thereby protecting the gate, source, and N-layer. Furthermore, the P-wall reduces the stress on the oxide by lowering the electric field by 10% (from 5.7 MV/cm^2 to 5.2 MV/cm^2).

(a) (b)

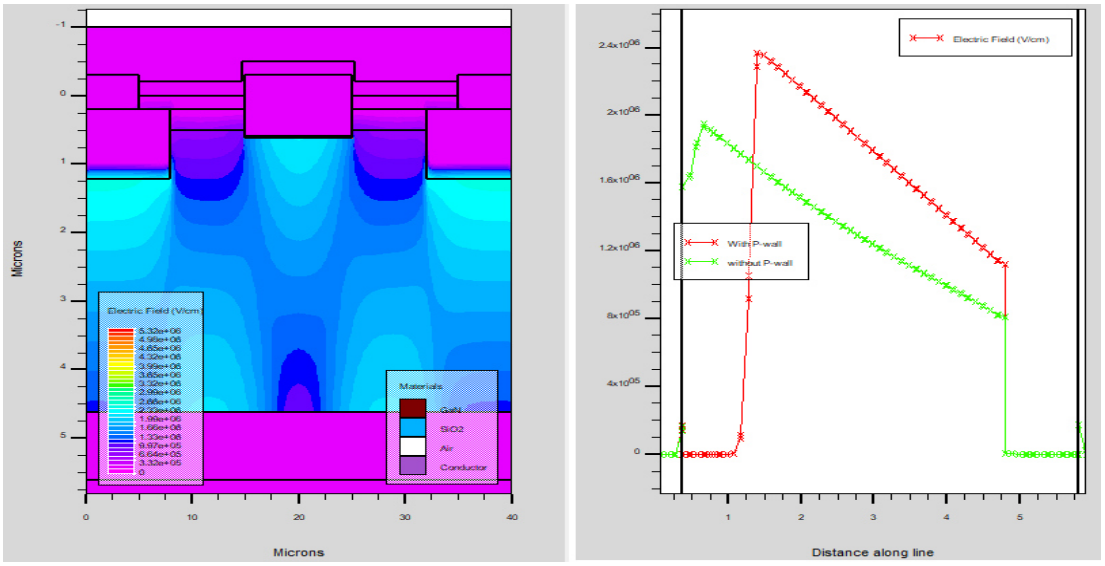


Figure 5-16 : (a) electric field distribution inside the P-wall structure. (b) Vertical cross section below the source that describes the evolution of the electric field of TMOSFET and P-wall MOSFET at the breakdown voltage.

In SJ-MOSFET silicon transistors (super junction transistors), the thickness of the P-wall is typically equal to the drift region. However, for GaN semiconductors, deep implantation is not yet feasible. As a result, the thickness of the P-wall in the simulations is limited to a maximum of 2 µm, with variations tested at 0.3 µm, 0.5 µm, 1 µm, and 2 µm. For the 0.3 µm, 0.5 µm, and 1 µm cases, the performance is quite similar, with a breakdown voltage (BV) of around 629 V (Figure 5-17a). Thicker P-wall seems to be effective to further drop the leakage current at blocking current (13 µA for 0.3 µm versus 10 µA for 1 µm).

In the 2 µm case, a further reduction in leakage current is observed while maintaining a similar breakdown voltage (Figure 5-17a). This effect is due to the superposition of the electric field near the drain and around the P-wall (Figure 5-17b), which is constrained by the material properties in this scenario. All configurations exhibit similar on-state characteristics.

(a) (b)

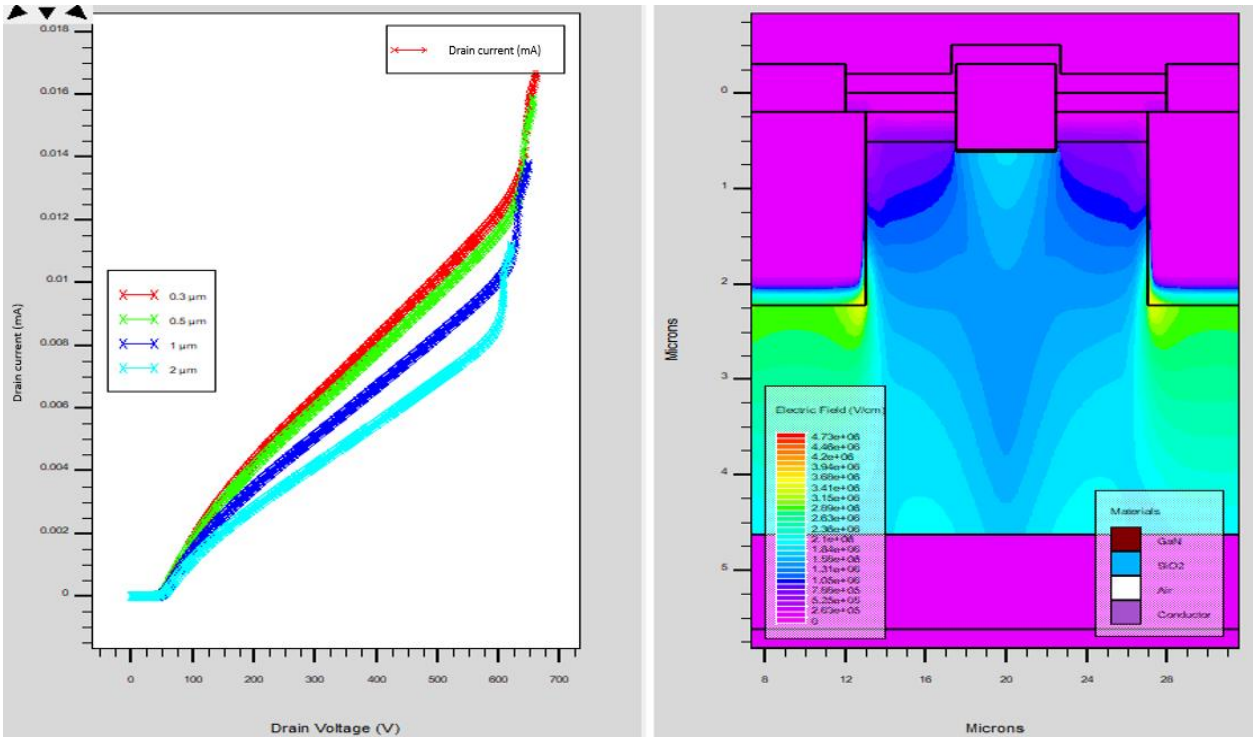


Figure 5-17 :: (a) Simulation of the impact of the P-Wall thickness variation on BV (b) electric field profile of the 2 µm P-wall thickness that shows the high electric field at the P-wall (3.2 MV/cm²)

5.4 Conclusion

In this chapter, vertical GaN-on-silicon TMOSFETs were studied. An initial pseudo-vertical device fabrication showed a breakdown voltage of 300 V and an on-resistance (Ron) of 2

mΩ.cm^2 with a high current density (> 2 kA/cm^2). Additionally, TCAD simulations were conducted, highlighting the need for optimization in both design and processing in order to fully unlock the potential of GaN-on-silicon TMOSFETs. To achieve this:

- The trench gate could be significantly optimized (conformal high-quality oxide needed)
- P-walls must be implemented.
- Fully vertical architecture has to be employed as seen from PIN diodes in chapter 4

Figure 5-18 benchmarks vertical GaN transistors on foreign substrates. While several papers discuss trench MOSFETs on foreign substrates, particularly sapphire, few have explored the blocking capability of these devices[173]. In the case of silicon, only one study was found that includes both pseudo-vertical and fully vertical designs [161]. Advances in process and growth techniques for silicon substrates will undoubtedly contribute to the development of these new technologies, positioning them as strong candidates for commercialization.

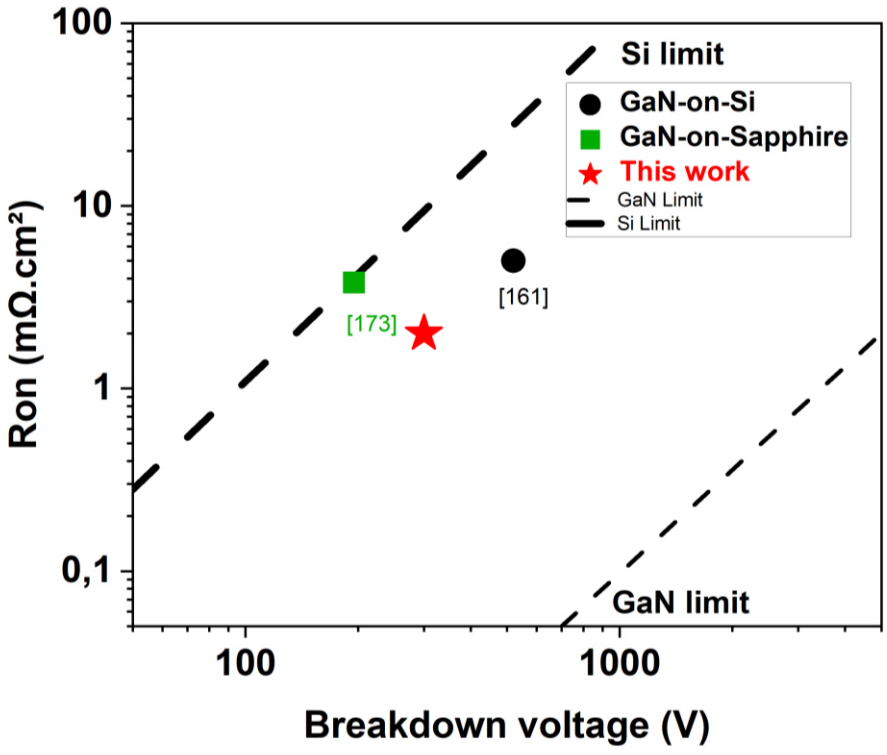


Figure 5-18 : Baliga figure of merit of vertical GaN on foreign substrate TMOSFETS

General conclusion

In the quest to develop new power devices that meet the demands of modern technology and progress, a race between different semiconductor materials has begun. While silicon power devices have dominated the market for decades, silicon carbide (SiC) has gained ground over the last five years. SiC power devices are intended to overcome the physical limitations of silicon, offering superior physical properties. However, the cost of fabricating these devices remains quite high, particularly for high-voltage applications.

As a strong alternative, gallium nitride (GaN) has attracted significant interest from both the research and industrial communities. GaN combines excellent physical properties, such as a high critical electric field, avalanche capability, and high electron mobility, with a more flexible fabrication cost. This cost flexibility is due to the variety of available substrates for growth, including gallium nitride itself (a very expensive option), sapphire (a cheaper option), and silicon (another cost-effective choice). To meet application requirements, major progress has been made in GaN growth on foreign substrates to reduce dislocation and defect density, achieving high-quality epitaxy.

GaN on foreign substrates can be implemented in two main architectures: lateral and vertical. The lateral structure, however, does not offer reliable performance at medium and high voltage range (e.g., lacks avalanche capability and poor electric field management) and consumes significant wafer space, reducing the number of devices per wafer. Conversely, the vertical structure addresses these issues with a junction-based design. This technology is easier to handle due to its similarity to existing vertical silicon and SiC devices, such as Schottky diodes, PiN diodes, and trench MOSFETs.

However, implementing vertical GaN-on-foreign-substrate technology presents challenges due to the need for backside processing. For this reason, many related studies employ a "pseudo-vertical" structure, where backside layer access is achieved through a frontside etching. Nonetheless, to unlock the full potential of these emerging types of devices, a fully vertical structure is essential, for which silicon substrate is an attractive option. The use of a silicon substrate allows access to the backside through deep silicon etching with DRIE and substrate thinning.

This work aimed to develop high-quality vertical GaN-on-silicon devices to validate the theoretical hypotheses surrounding this technology. The target application range was set between 600-1200 V, with a focus on diode development as a proof of concept.

To achieve these goals, the first chapter discussed the current progress and state-of-the-art of GaN-on-silicon substrate devices, emphasizing both the physical properties (such as avalanche, on-state, and off-state mechanisms) and material properties (including dislocation filtering and defects) from lateral HEMT structures to vertical structures. This chapter demonstrated the necessity of vertical GaN-on-silicon devices, and the P-I-N diodes were chosen as test vehicle for developing the vertical structure.

In the second chapter, TCAD simulations were conducted using Silvaco software to understand the various interplay / trade-off within the GaN-on-silicon P-I-N diode. These simulations guide the optimal design of the P-I-N structure to achieve high on-state and off-state performance. This chapter also established the importance of employing a fully vertical design.

The third chapter presented the optimization of the fabrication process, including steps such as ohmic contacts, mesa formation, edge termination, local substrate removal, and buffer etching. To mitigate the mechanical issues due to the reduced thickness of devices after backside processing, a thick polyimide passivation layer was applied to strengthen the devices. Additionally, the N-face ohmic contact on the backside was improved using HCl treatment, and a thick copper heatsink layer was implemented on the backside.

The fourth chapter highlighted the key findings of this thesis. By using different epitaxial sources and designs, we demonstrated a significant reduction in leakage current in the off-state by employing a SiN-based buffer, which effectively reduces dislocation density. An alternative island-based buffer was also utilized, leading to the first demonstration of avalanche capability in vertical GaN devices on silicon substrates, for both pseudo-vertical and fully vertical structures. Furthermore, using the same buffer, high-quality breakdown scaling with drift thickness was achieved, reaching 1200 V blocking voltage with a 7.4 µm drift thickness. We also conducted an experimental comparison between pseudo-vertical and fully vertical designs. The process developed in the third chapter enabled the fabrication of the first fully vertical structure with a low on-resistance (Ron) of 0.48

$m\Omega \cdot cm^2$, high breakdown voltage with avalanche capability at 1200 V, and an on-state current well-above 10 A.

Chapter 5 presented the final contribution of this thesis, which involves the demonstration of pseudo-vertical GaN-on-silicon trench metal-oxide-semiconductor field-effect transistors (TMOSFETs). We provided some TCAD design of the transistor with a preliminary proof of concept, achieving a 300 V breakdown voltage, a 2 $m\Omega \cdot cm^2$ on-resistance, and a current density greater than 2 kA/cm^2. Further improvements in performance are suggested in this chapter.

The results of this thesis provide strong evidence of the feasibility of vertical GaN-on-silicon devices.

To further advance the development of vertical power devices, several research paths can be pursued. In this section, we will outline potential directions and future work that could build upon the findings of this thesis.

7.1 Improvement of the GaN-on-Silicon P-I-N and TMOSFET performances

A clear direction for future work is to enhance the performance of the demonstrated devices within this work. For instance, the leakage current of the P-I-N diodes could be further minimized by tuning the doping concentration in the drift region. Additionally, the avalanche capability could be evaluated using emission microscopy or electroluminescence measurements, which provide valuable insights into the current generated by impact ionization (see Figure 7-1). Furthermore, optimizing the TMOSFET fabrication process could improve both the on-state and off-state behavior of the device.

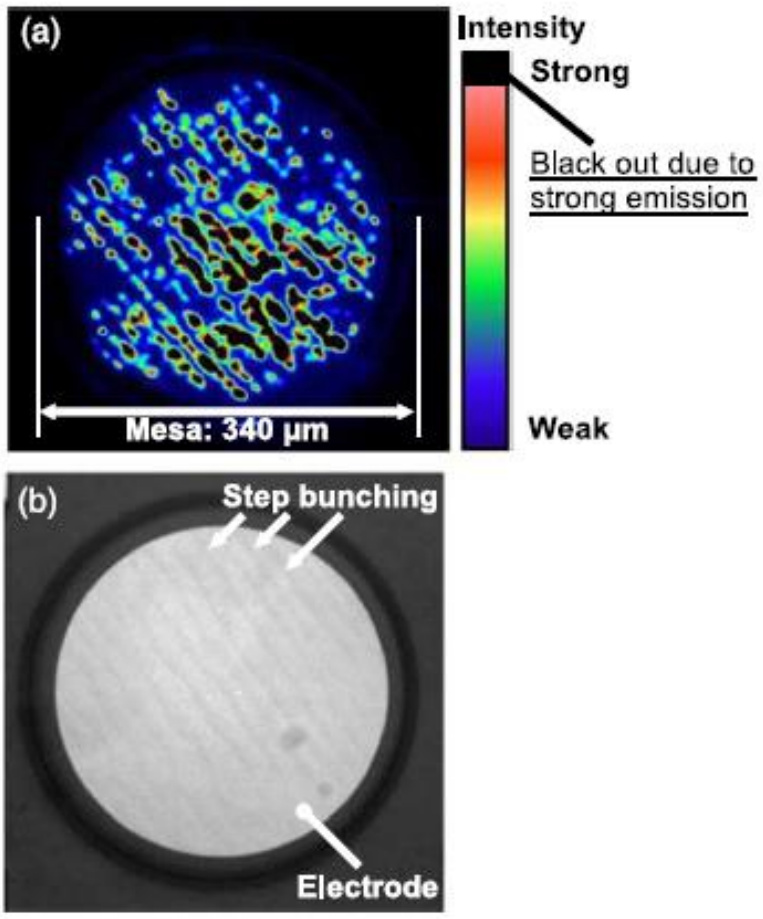


Figure 7-1 : emission microscopy on a GaN-on-GaN PiN diode with avalanche breakdown [57]

7.2 Implantation of the P wall in the vertical GaN on Silicon devices

From a TCAD simulation perspective, P-walls significantly enhance the off-state behavior of the TMOSFET (Figure 5-17 and 7-2). This technology could also be applied to other devices, such as P-I-N diodes. However, incorporating P-walls presents challenges from a growth standpoint as no selective p-type doping is currently available for GaN material. Nevertheless, several techniques could be employed to introduce the P-walls:

- Selective implantation and activation at high temperature of the Mg P-doping
- Etching and regrowth by MOCVD or MBE the P-walls
- The use of NiO film as a P-type layer.

The implantation of Mg P-doping in GaN epitaxy remains challenging, with only a small fraction of the dopants typically being activated. As an alternative, the epitaxial layer can be etched to allow for the regrowth of P-doped walls within the etched regions, a technique well-established for lateral structures. However, no demonstrations have yet been successfully conducted for vertical structures.

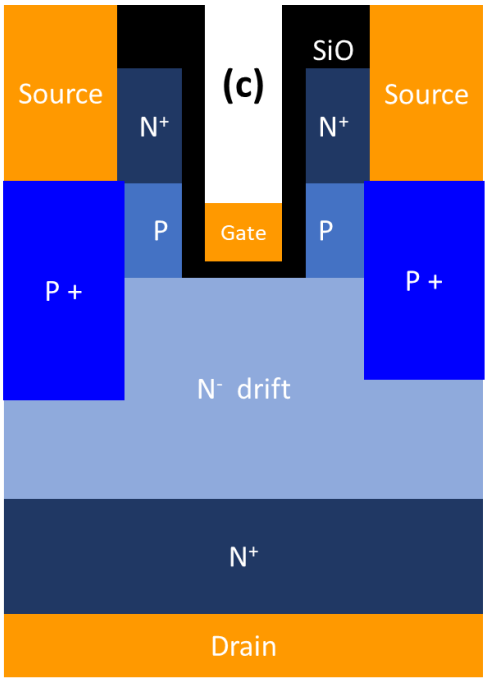


Figure 7-2 : schematic cross section of the P-wall based vertical transistors [57]

Additionally, it was recently discovered that a P-type NiO layer can serve as a substitute for the P-doped GaN layer (Figure 7-3). This film is intrinsically P-doped, and the doping level can be easily adjusted by modifying the O_2 flow during sputtering deposition. This

approach operates similarly to the etching and regrowth method; however, instead of growing a P-doped GaN layer, a NiO film is sputtered onto the surface.

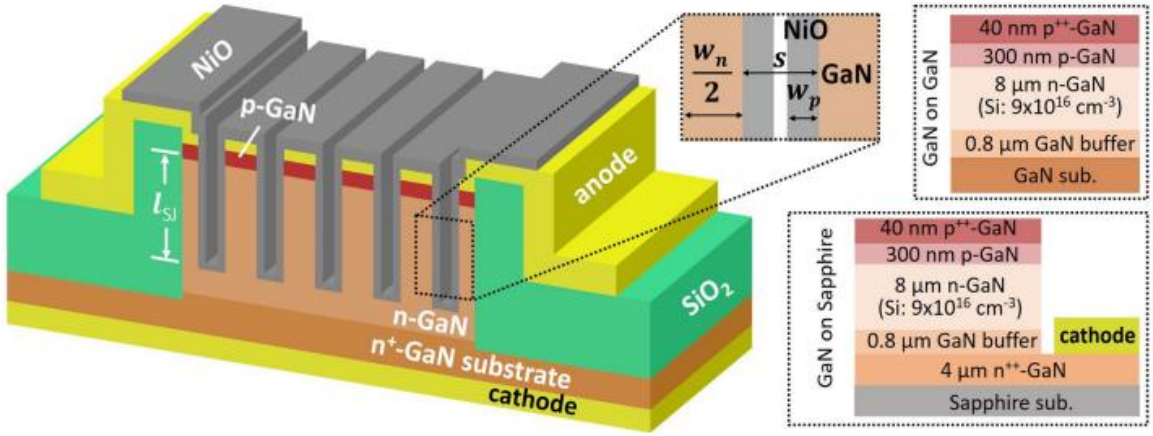


Figure 7-3 : Super junction GaN-on-GaN diode using P-NiO as a P wall [174]

7.3 Engineered substrates technology as an alternative for direct growth

The well-known smart cut technology could be used as an alternative engineered substrate for vertical epitaxy. This technology is widely used for RF, with Silicon on insulator technology, and for power applications with SmartSiC technology. Figure 7-4 outlines the specific fabrication flow for creating such an engineered substrate. This flow involves several key steps: ion implantation, surface preparation for pre-bonding, conductive bonding of the donor wafer onto the target substrate, thermal splitting, and subsequent surface finishing. Additionally, the process incorporates a GaN donor refresh cycle, enabling the production of multiple samples from a single donor wafer. However, to align with the specific demands of power GaN technology, adaptations to the Smart-Cut process are necessary.

The Vertical engineered substrate is an advanced engineered material that will combine GaN with polycrystalline silicon carbide (poly-SiC), specifically designed for 1200 V vertical FET transistors on 200 mm wafers. Building on the SmartSiC product concept, this substrate features a highly conductive poly-SiC handle, which significantly enhances electrical and thermal performance, enabling higher power densities and efficient backside cooling compatible with existing SiC assembly processes. The development of

the Vertical engineered substrate addresses the current limitations of GaN bulk wafers, constrained to 100 mm diameter. The main challenges involve achieving a high-quality GaN epi-ready surface with a low dislocation density (targeting $1 \cdot 10^7$ cm^{-2} or below) and developing a poly-SiC handle with ultra-low electrical resistivity (<5 mΩ·cm) and high thermal conductivity (90% of monocrystalline SiC performance). Additionally, the Smart-Cut process must be adapted to create an ultra-high conductivity-bonding interface between the GaN and poly-SiC layers without requiring an additional buffer layer.

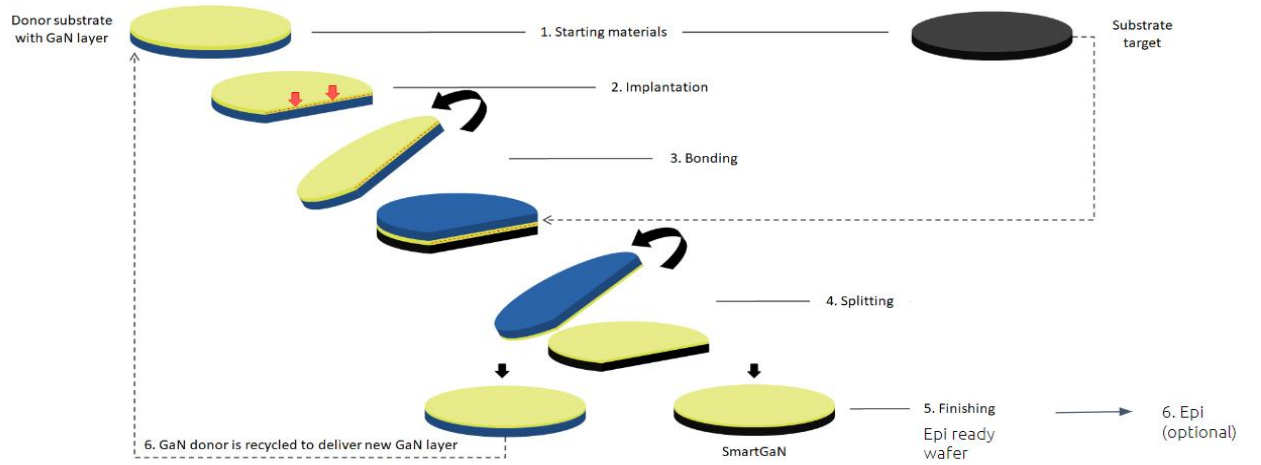


Figure 7-4 : Schematic of Smart-Cut process for GaN engineered substrates.

Publications related to this thesis

❖ Journal

1. I. Abid, **Y. Hamdaoui**, J. Mehta, J. Derluyn, et F. Medjdoub, « Low Buffer Trapping Effects above 1200 V in Normally off GaN-on-Silicon Field Effect Transistors » , Micromachines, vol. 13, no 9, p. 1519, sept. 2022, doi : 10.3390/mi13091519.
2. **Y. Hamdaoui**, I. Abid, S. Michler, K. Ziouche, et F. Medjdoub, « Demonstration of avalanche capability in 800 V vertical GaN-on-Silicon diodes » , Applied Physics Express, vol. 17, no 1, p. 016503, déc. 2023, doi : 10.35848/1882-0786/ad106c.
3. **Y. Hamdaoui**, S. Vandenbroucke, S. Michler, K. Ziouche, M. Minjauw, C. Detavernier and F. Medjdoub « Optimization of non-alloyed backside ohmic contacts to N-face 2 GaN for fully vertical GaN-on-Silicon based power devices». Micromachines, 15(9), 1157, Septembre 2024 : https://doi.org/10.3390/mi15091157
4. S. Michler, **Y. Hamdaoui**, S. Thapa, G. Schwalb, S. Besendörfer, K. Ziouche, M. Albrecht, F. Brunner, F. Medjdoub, and E. Meissner « Epitaxy of > 7 µm Thick GaN Drift Layers on 150 mm Si(111) Substrates Realizing Vertical PN Diodes with 1200 V Breakdown Voltage», Submitted paper to physica status solidi (a).
5. **Y. Hamdaoui**, S. Michlerson, A. Bidaud, K. Ziouche, and F. Medjdoub « 1200V fully vertical GaN on Silicon P i N diodes with avalanche capability and high on state current above 10 A», Submitted paper to IEEE transaction on electron device.

❖ International Conferences

1. 14th Topical Workshopon Heterostructure Micro- electronics (TWHM) on august 2022, Hiroshima, Japan « Local substrate removal for next generation GaN-on-Silicon powr transistors» **Y. Hamdaoui**, I. Abid, K. Ziouche and F. Medjdoub.
2. 46th Workshopon Compound Semiconductor Devices and Integrated Circuits(WOCSDICE2023), May 2023, Palermo, Italy « High quality drift layer thickness scaling in vertical GaN-on-Silicon PIN diodes» **Y. Hamdaoui**, I. Abid, S. Michler, K. Ziouche and F. Medjdoub.

3. Compound semiconductor week 2023, May 2023, Jeju, South Korea «Towards High Performance Fully Vertical GaN-on-Silicon PIN Diodes» **Y. Hamdaoui**, I. Abid, S. Michler, K. Ziouche and F. Medjdoub.
4. 14th International Conference on Nitride Semiconductors (ICNS-14), November 2023, Nagoya, Japan « Process optimization of Fully Vertical GaN on Silicon PIN diodes » I. Abid, **Y. Hamdaoui**, S. Michler, K. Ziouche and F. Medjdoub.
5. 14th International Conference on Nitride Semiconductors (ICNS-14), November 2023, Nagoya, Japan « Epitaxy of thick GaN drift layers on Si 111 forvertical power devices » S. Michler, **Y. Hamdaoui**, I. Abid, K. Ziouche and F. Medjdoub.
6. 14th International Conference on Nitride Semiconductors (ICNS-14), November 2023, Nagoya, Japan « Dislocation density reduction for vertical GaN devices on 200mm Si » Z. Gao, **Y. Hamdaoui**, I. Abid, F. Medjdoub, E. Meissner, S. Besendörfer, M. Heuken.
7. GaN Marathon 2024, Juin 2024, Verona, Italy «High quality fully versus pseudo vertical GaN-on-Silicon pn diodes» **Y. Hamdaoui**, I. Abid, S. Michler, K. Ziouche and F. Medjdoub.
8. 15th Topical Workshopon Heterostructure Micro-electronics (TWHM) on august 2024, Miyagi, Japan «High performance fully vertical GaN on Silicon PIN diodes for next generation power devices» **Y. Hamdaoui**, S. Michler, K. Ziouche and F. Medjdoub.
9. 12th International Workshop on Nitride Semiconductors (IWN), Octobre 2024 Hawaii, USA «Recent progress of vertical GaN-on-Silicon devices» **Y. Hamdaoui**, S. Michler, K. Ziouche and F. Medjdoub.
10. 12th International Workshop on Nitride Semiconductors (IWN), Octobre 2024 Hawaii, USA «Vertical GaN devices: degradation physics and recent case studies» M. Meneghini, M. Fregolent, N. Zagni, **Y. Hamadoui**, A. Marcuzzi, D. Favero, C. De Santi, M. Buffolo, E. Bahat-Treidel, E. Brusaterra, F. Brunner, O. Hilt, C. Huber, F. Medjdoub, G. Meneghesso, G. Verzellesi, P. Pavan, and E. Zanoni.
11. 70th Annual IEEE International Electron Devices Meeting (IEDM), December 2024, San Francisco,USA «Vertical GaN Devices: Reliability Challenges and Lessons Learned from Si and SiC» M. Meneghini, M. Fregolent, N. Zagni, **Y. Hamadoui**, A. Marcuzzi, D. Favero, C. De Santi, M. Buffolo, E. Bahat-Treidel, E.

Brusaterra, F. Brunner, O. Hilt, C. Huber, F. Medjdoub, G. Meneghesso, G. Verzellesi, P. Pavan, and E. Zanoni

❖ Press release

- Interview with Compound semiconductor magazine about Realising avalanche in GaN-on-silicon diodes, Monday 11th March 2024 : https://compoundsemiconductor.net/article/118882/Realising_avalanche_in_GaN-on-silicon_diodes

❖ Awards

- The Best Poster Award during the Materials and Electrical Energy (MEDEE) event, April 2024, Béthune, France.
- The best presentation during IEEE/Dei summer school SSI2, July 2022, Bressanone, Italy.

References

[1] D. Tiku, "dc Power Transmission: Mercury-Arc to Thyristor HVdc Valves [History]," *IEEE Power and Energy Mag.*, vol. 12, no. 2, pp. 76–96, Mar. 2014, doi: 10.1109/MPE.2013.2293398.

[2] B. J. Baliga, *Fundamentals of power semiconductor devices*. New York, NY: Springer, 2008.

[3] B. J. Baliga, *Advanced High Voltage Power Device Concepts*. New York, NY: Springer New York, 2012. doi: 10.1007/978-1-4614-0269-5.

[4] F. E. Holmes And C. A. T. Salama "Vmos-NEW MOS INTEGRATED CIRCUIT TECHNOLOGY" Solid-State Electronics, 1974, Vol. 17, pp. 791-797

[5] C. Bulucea and R. Rossen, "Trench DMOS transistor technology for high-current (100 A range) switching," *Solid-State Electronics*, vol. 34, no. 5, pp. 493–507, May 1991, doi: 10.1016/0038-1101(91)90153-P.

[6] M. Harada, T. Minato, H. Takahashi, H. Nishihara, K. Inoue, and I. Takata, "600 V trench IGBT in comparison with planar IGBT-an evaluation of the limit of IGBT performance," in *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics*, Davos, Switzerland: Hartung-Gorre Verlag, 1994, pp. 411–416. doi: 10.1109/ISPSD.1994.583811.

[7] N. Tokura, S. Takahashi, and K. Hara, "The DMOS consisting of channel region defined by LOCOS (LOCOS-DMOS): a new process/device technology for low on-resistance power MOSFET," in *[1993] Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs*, Monterey, CA, USA: IEEE, 1993, pp. 135–140. doi: 10.1109/ISPSD.1993.297124.

[8] Y. Oonishi, A. Ooi, and T. Shimatou, "Superjunction MOSFET".

[9] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The Trench Power MOSFET—Part II: Application Specific VDMOS, LDMOS, Packaging, and Reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017, doi: 10.1109/TED.2017.2655149.

[10] L. Dorn-Gomba, J. Ramoul, J. Reimers, and A. Emadi, "Power Electronic Converters in Electric Aircraft: Current Status, Challenges, and Emerging Technologies," *IEEE Trans. Transp. Electrific.*, vol. 6, no. 4, pp. 1648–1664, Dec. 2020, doi: 10.1109/TTE.2020.3006045.

[11] F. Blaabjerg, H. Wang, I. Vernica, B. Liu, and P. Davari, "Reliability of Power Electronic Systems for EV/HEV Applications," *Proc. IEEE*, vol. 109, no. 6, pp. 1060–1076, Jun. 2021, doi: 10.1109/JPROC.2020.3031041.

[12] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. D: Appl. Phys.*, vol. 51, no. 16, p. 163001, Apr. 2018, doi: 10.1088/1361-6463/aaaf9d.

[13] M. Meneghini *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *Journal of Applied Physics*, vol. 130, no. 18, p. 181101, Nov. 2021, doi: 10.1063/5.0061354.

[14] O. Ambacher *et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 87, no. 1, pp. 334–344, Jan. 2000, doi: 10.1063/1.371866.

[15] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures,"

Journal of Applied Physics, vol. 85, no. 6, pp. 3222–3233, Mar. 1999, doi: 10.1063/1.369664.

[16] U. K. Mishra, P. Parikh, and Yi-Feng Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002, doi: 10.1109/JPROC.2002.1021567.

[17] L. Shen *et al.*, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 457–459, Oct. 2001, doi: 10.1109/55.954910.

[18] F. A. Marino, N. Faralli, D. K. Ferry, S. M. Goodnick, and M. Saraniti, "Figures of merit in high-frequency and high-power GaN HEMTs," *J. Phys.: Conf. Ser.*, vol. 193, p. 012040, Nov. 2009, doi: 10.1088/1742-6596/193/1/012040.

[19] C.-T. Ma and Z.-H. Gu, "Review of GaN HEMT Applications in Power Converters over 500 W," *Electronics*, vol. 8, no. 12, p. 1401, Nov. 2019, doi: 10.3390/electronics8121401.

[20] T. Mimura, "The early history of the high electron mobility transistor (HEMT)," *IEEE Trans. Microwave Theory Techn.*, vol. 50, no. 3, pp. 780–782, Mar. 2002, doi: 10.1109/22.989961.

[21] H. P. Maruska and D. A. Stevenson, "Mechanism of light production in metal-insulator-semiconductor diodes; GaN:Mg violet light-emitting diodes," *Solid-State Electronics*, vol. 17, no. 11, pp. 1171–1179, Nov. 1974, doi: 10.1016/0038-1101(74)90161-0.

[22] Y. Zhang, A. Dadgar, and T. Palacios, "Gallium nitride vertical power devices on foreign substrates: a review and outlook," *J. Phys. D: Appl. Phys.*, vol. 51, no. 27, p. 273001, Jul. 2018, doi: 10.1088/1361-6463/aac8aa.

[23] Y. Zhang "GaN-based Vertical Power Devices", PhD thesis at MIT, June 2017.

[24] M. Buffolo *et al.*, "Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives," *IEEE Trans. Electron Devices*, vol. 71, no. 3, pp. 1344–1355, Mar. 2024, doi: 10.1109/TED.2023.3346369.

[25] J. S. Lundh *et al.*, "Experimental Validation of Robust Hybrid Edge Termination Structures in Vertical GaN p-i-n Diodes With Avalanche Capability," *IEEE Electron Device Lett.*, vol. 45, no. 5, pp. 873–876, May 2024, doi: 10.1109/LED.2024.3377532.

[26] O. Aktas and I. C. Kizilyalli, "Avalanche Capability of Vertical GaN p-n Junctions on Bulk GaN Substrates," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 890–892, Sep. 2015, doi: 10.1109/LED.2015.2456914.

[27] S. Chen and G. Wang, "High-field properties of carrier transport in bulk wurtzite GaN: A Monte Carlo perspective," *Journal of Applied Physics*, vol. 103, no. 2, p. 023703, Jan. 2008, doi: 10.1063/1.2828003.

[28] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical Power p-n Diodes Based on Bulk GaN," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 414–422, Feb. 2015, doi: 10.1109/TED.2014.2360861.

[29] C. Gupta *et al.*, "In Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET) on Bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 353–355, Mar. 2017, doi: 10.1109/LED.2017.2649599.

[30] J. Schalwig *et al.*, "Hydrogen response mechanism of Pt–GaN Schottky diodes," *Applied Physics Letters*, vol. 80, no. 7, pp. 1222–1224, Feb. 2002, doi: 10.1063/1.1450044.

[31] S. Xia, Y. Zhang, J. Wang, J. Chen, and K. Xu, "HVPE growth of bulk GaN with high conductivity for vertical devices," *Semicond. Sci. Technol.*, vol. 36, no. 1, p. 014009, Jan. 2021, doi: 10.1088/1361-6641/abca4e.

[32] K. Harrouche, S. Venkatachalam, F. Grandpierron, E. Okada, and F. Medjdoub, "Impact of undoped channel thickness and carbon concentration on AlN/GaN-on-SiC HEMT performances," *Appl. Phys. Express*, vol. 15, no. 11, p. 116504, Nov. 2022, doi: 10.35848/1882-0786/ac9c46.

[33] K. Harrouche, R. Kabouche, E. Okada, and F. Medjdoub, "High Performance and Highly Robust AlN/GaN HEMTs for Millimeter-Wave Operation," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1145–1150, 2019, doi: 10.1109/JEDS.2019.2952314.

[34] C. Gupta, Y. Enatsu, G. Gupta, S. Keller, and U. K. Mishra, "High breakdown voltage p-n diodes on GaN on sapphire by MOCVD: High breakdown voltage p-n diodes," *Phys. Status Solidi A*, vol. 213, no. 4, pp. 878–882, Apr. 2016, doi: 10.1002/pssa.201532554.

[35] S. E. Harrison, Q. Shao, C. D. Frye, L. F. Voss, and R. J. Nikolic, "1.1 kV vertical p-i-n GaN-on-sapphire diodes," in *2018 76th Device Research Conference (DRC)*, Santa Barbara, CA: IEEE, Jun. 2018, pp. 1–2. doi: 10.1109/DRC.2018.8442240.

[36] E. Brusaterra *et al.*, "Optimization of Vertical GaN Drift Region Layers for Avalanche and Punch-Through Pn-Diodes," *IEEE Electron Device Lett.*, vol. 44, no. 3, pp. 388–391, Mar. 2023, doi: 10.1109/LED.2023.3234101.

[37] W. Qi *et al.*, "0.58 mΩ·cm^2/523 V GaN Vertical Schottky Barrier Diode With 15.6 kA/cm^2 Surge Current Enabled by Laser Lift-Off/ Annealing and N-Ion Implantation," *IEEE Electron Device Lett.*, vol. 45, no. 6, pp. 964–967, Jun. 2024, doi: 10.1109/LED.2024.3390125.

[38] W. Saito *et al.*, "High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003, doi: 10.1109/TED.2003.819248.

[39] D. Maier *et al.*, "Testing the Temperature Limits of GaN-Based HEMT Devices," *IEEE Trans. Device Mater. Relib.*, vol. 10, no. 4, pp. 427–436, Dec. 2010, doi: 10.1109/TDMR.2010.2072507.

[40] I. Abid *et al.*, "AlGaN Channel High Electron Mobility Transistors with Regrown Ohmic Contacts," *Electronics*, vol. 10, no. 6, p. 635, Mar. 2021, doi: 10.3390/electronics10060635.

[41] F. Medjdoub, M. Zegaoui, B. Grimbert, N. Rolland, and P.-A. Rolland, "Effects of AlGaN Back Barrier on AlN/GaN-on-Silicon High-Electron-Mobility Transistors," *Appl. Phys. Express*, vol. 4, no. 12, p. 124101, Nov. 2011, doi: 10.1143/APEX.4.124101.

[42] I. Abid, E. Canato, M. Meneghini, G. Meneghesso, K. Cheng, and F. Medjdoub, "GaN-on-silicon transistors with reduced current collapse and improved blocking voltage by means of local substrate removal," *Appl. Phys. Express*, vol. 14, no. 3, p. 036501, Mar. 2021, doi: 10.35848/1882-0786/abdca0.

[43] S. Ghosh, A. M. Hinz, M. Frentrup, S. Alam, D. J. Wallis, and R. A. Oliver, "Design of step-graded AlGaN buffers for GaN-on-Si heterostructures grown by MOCVD," *Semicond. Sci. Technol.*, vol. 38, no. 4, p. 044001, Apr. 2023, doi: 10.1088/1361-6641/acb9b6.

[44] L. Yang *et al.*, "The DC Performance and RF Characteristics of GaN-Based HEMTs Improvement Using Graded AlGaN Back Barrier and Fe/C Co-Doped Buffer," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4170–4174, Aug. 2022, doi: 10.1109/TED.2022.3179675.

[45] X. Chen *et al.*, "Enhanced breakdown voltage and dynamic performance of GaN HEMTs with AlN/GaN superlattice buffer," *J. Phys. D: Appl. Phys.*, vol. 56, no. 35, p. 355101, Aug. 2023, doi: 10.1088/1361-6463/acd069.

[46] L. Heuken *et al.*, "Analysis of an AlGaN/AlN Super-Lattice Buffer Concept for 650-V Low-Dispersion and High-Reliability GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 1113–1119, Mar. 2020, doi: 10.1109/TED.2020.2968757.
[47] I. Abid "Nouveaux composants électroniques à base du matériau AlN pour les futures applications de puissance," PhD thesis at the university of Lille, France, July 2021.
[48] S. Michler, S. Thapa, S. Besendörfer, M. Albrecht, R. Weingärtner, and E. Meissner, "Utilizing Island Growth in Superlattice Buffers for the Realization of Thick GaN-on-Si(111) PIN-Structures for Power Electronics," *Physica Status Solidi (b)*, p. 2400019, Mar. 2024, doi: 10.1002/pssb.202400019.
[49] Z. Gao *et al.*, "Dislocation density reduction for vertical GaN devices on 200 mm Si". 14th International Conference on Nitride Semiconductors (ICNS-14), Nagoya, Japan Nov 2023.
[50] I. Abid, Y. Hamdaoui, J. Mehta, J. Derluyn, and F. Medjdoub, "Low Buffer Trapping Effects above 1200 V in Normally off GaN-on-Silicon Field Effect Transistors," *Micromachines*, vol. 13, no. 9, p. 1519, Sep. 2022, doi: 10.3390/mi13091519.
[51] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Materials Science in Semiconductor Processing*, vol. 78, pp. 96–106, May 2018, doi: 10.1016/j.mssp.2017.09.027.
[52] D. Ji *et al.*, "Normally OFF Trench CAVET With Active Mg-Doped GaN as Current Blocking Layer," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 805–808, Mar. 2017, doi: 10.1109/TED.2016.2632150.
[53] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "100 A Vertical GaN Trench MOSFETs with a Current Distribution Layer," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Shanghai, China: IEEE, May 2019, pp. 303–306. doi: 10.1109/ISPSD.2019.8757621.
[54] T. Pu, U. Younis, H.-C. Chiu, K. Xu, H.-C. Kuo, and X. Liu, "Review of Recent Progress on Vertical GaN-Based PN Diodes," *Nanoscale Res Lett*, vol. 16, no. 1, p. 101, Dec. 2021, doi: 10.1186/s11671-021-03554-7.
[55] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, and D. Bour, "High Voltage Vertical GaN p-n Diodes With Avalanche Capability," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3067–3070, Oct. 2013, doi: 10.1109/TED.2013.2266664.
[56] K. Fu, Z. He, C. Yang, J. Zhou, H. Fu, and Y. Zhao, "GaN-on-GaN p-i-n diodes with avalanche capability enabled by eliminating surface leakage with hydrogen plasma treatment," *Applied Physics Letters*, vol. 121, no. 9, p. 092103, Aug. 2022, doi: 10.1063/5.0107677.
[57] H. Fukushima *et al.*, "Vertical GaN p–n diode with deeply etched mesa and the capability of avalanche breakdown," *Appl. Phys. Express*, vol. 12, no. 2, p. 026502, Feb. 2019, doi: 10.7567/1882-0786/aafdb9.
[58] D. Ji, B. Ercan, G. Benson, A. K. M. Newaz, and S. Chowdhury, "Robust avalanche in GaN leading to record performance in avalanche photodiode," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, Dallas, TX, USA: IEEE, Apr. 2020, pp. 1–4. doi: 10.1109/IRPS45951.2020.9129299.
[59] G. T. Dang *et al.*, "High voltage GaN Schottky rectifiers," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 692–696, Apr. 2000, doi: 10.1109/16.830981.
[60] A. T. Binder *et al.*, "Gate protection for vertical gallium nitride trench MOSFETs: The buried field shield," *e-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 5, p. 100218, Sep. 2023, doi: 10.1016/j.prime.2023.100218.

[61] K. Matsumoto *et al.*, "Opportunities and challenges in GaN metal organic chemical vapor deposition for electron devices," *Jpn. J. Appl. Phys.*, vol. 55, no. 5S, p. 05FK04, May 2016, doi: 10.7567/JJAP.55.05FK04.
[62] A. Armstrong *et al.*, "Impact of carbon on trap states in *n* -type GaN grown by metalorganic chemical vapor deposition," *Applied Physics Letters*, vol. 84, no. 3, pp. 374–376, Jan. 2004, doi: 10.1063/1.1643540.
[63] G. Piao *et al.*, "Study of carbon concentration in GaN grown by metalorganic chemical vapor deposition," *Journal of Crystal Growth*, vol. 456, pp. 137–139, Dec. 2016, doi: 10.1016/j.jcrysgro.2016.08.030.
[64] A. Agarwal, C. Gupta, Y. Enatsu, S. Keller, and U. Mishra, "Controlled low Si doping and high breakdown voltages in GaN on sapphire grown by MOCVD," *Semicond. Sci. Technol.*, vol. 31, no. 12, p. 125018, Dec. 2016, doi: 10.1088/0268-1242/31/12/125018.
[65] A. E. Wickenden, D. D. Koleske, R. L. Henry, M. E. Twigg, and M. Fatemi, "Resistivity control in unintentionally doped GaN films grown by MOCVD," *Journal of Crystal Growth*, vol. 260, no. 1–2, pp. 54–62, Jan. 2004, doi: 10.1016/j.jcrysgro.2003.08.024.
[66] W. G. Filho *et al.*, "Mg activation anneal of the p-GaN body in trench gate MOSFETs and its effect on channel mobility and threshold voltage stability," *Applied Physics Letters*, vol. 124, no. 11, p. 113502, Mar. 2024, doi: 10.1063/5.0191973.
[67] C. Guarneros and V. Sánchez, "Magnesium doped GaN grown by MOCVD," *Materials Science and Engineering: B*, vol. 174, no. 1–3, pp. 263–265, Oct. 2010, doi: 10.1016/j.mseb.2010.03.022.
[68] T. S. Jeong *et al.*, "Room-temperature luminescence study on the effect of Mg activation annealing on p-GaN layers grown by MOCVD," *Journal of Crystal Growth*, vol. 280, no. 3–4, pp. 401–407, Jul. 2005, doi: 10.1016/j.jcrysgro.2005.04.014.
[69] M. E. Zvanut, Y. Uprety, J. Dashdorj, M. Moseley, and W. Alan Doolittle, "Passivation and activation of Mg acceptors in heavily doped GaN," *Journal of Applied Physics*, vol. 110, no. 4, p. 044508, Aug. 2011, doi: 10.1063/1.3626461.
[70] J. Wang *et al.*, "Investigation on minority carrier lifetime, diffusion length and recombination mechanism of Mg-doped GaN grown by MOCVD," *Journal of Alloys and Compounds*, vol. 870, p. 159477, Jul. 2021, doi: 10.1016/j.jallcom.2021.159477.
[71] A. Tanaka, W. Choi, R. Chen, and S. A. Dayeh, "Si Complies with GaN to Overcome Thermal Mismatches for the Heteroepitaxy of Thick GaN on Si," *Advanced Materials*, vol. 29, no. 38, p. 1702557, Oct. 2017, doi: 10.1002/adma.201702557.
[72] J.-H. Boo, C. Rohr, and W. Ho, "MOCVD of BN and GaN thin films on silicon: new attempt of GaN growth with BN buffer layer," *Journal of Crystal Growth*, vol. 189–190, pp. 439–444, Jun. 1998, doi: 10.1016/S0022-0248(98)00323-6.
[73] A. Dadgar, "Sixteen years GaN on Si," *Physica Status Solidi (b)*, vol. 252, no. 5, pp. 1063–1068, May 2015, doi: 10.1002/pssb.201451656.
[74] Y. Honda, Y. Kuroiwa, M. Yamaguchi, and N. Sawaki, "Growth of GaN free from cracks on a (111)Si substrate by selective metalorganic vapor-phase epitaxy," *Applied Physics Letters*, vol. 80, no. 2, pp. 222–224, Jan. 2002, doi: 10.1063/1.1432764.
[75] E. Calleja *et al.*, "Effect of Ga/Si interdiffusion on optical and transport properties of GaN layers grown on Si(111) by molecular-beam epitaxy," *Phys. Rev. B*, vol. 58, no. 3, pp. 1550–1559, Jul. 1998, doi: 10.1103/PhysRevB.58.1550.
[76] W. Gonçalez Filho *et al.*, "Development and analysis of thick GaN drift layers on 200 mm CTE-matched substrate for vertical device processing," *Sci Rep*, vol. 13, no. 1, p. 15931, Sep. 2023, doi: 10.1038/s41598-023-42747-1.

[77] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074011, Jul. 2013, doi: 10.1088/0268-1242/28/7/074011.
[78] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989, doi: 10.1109/55.43098.
[79] Yuhao Zhang *et al.*, "Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015, doi: 10.1109/TED.2015.2426711.
[80] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Fully Vertical GaN p-i-n Diodes Using GaN-on-Si Epilayers," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016, doi: 10.1109/LED.2016.2548488.
[81] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, "720-V/0.35-m $\Omega \cdot$ cm 2 Fully Vertical GaN-on-Si Power Diodes by Selective Removal of Si Substrates and Buffer Layers," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 715–718, May 2018, doi: 10.1109/LED.2018.2819642.
[82] N. Herbecq *et al.*, "1900 V, 1.6 mΩ cm 2 AlN/GaN-on-Si power devices realized by local substrate removal," *Appl. Phys. Express*, vol. 7, no. 3, p. 034103, Mar. 2014, doi: 10.7567/APEX.7.034103.
[83] X. Guo *et al.*, "1200-V GaN-on-Si Quasi-Vertical p-n Diodes," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2057–2060, Dec. 2022, doi: 10.1109/LED.2022.3219103.
[84] F. Jia *et al.*, "930V and Low-Leakage Current GaN-on-Si Quasi-Vertical PiN Diode With Beveled-Sidewall Treated by Self-Aligned Fluorine Plasma," *IEEE Electron Device Lett.*, vol. 43, no. 9, pp. 1400–1403, Sep. 2022, doi: 10.1109/LED.2022.3195263.
[85] X. Liu *et al.*, "GaN-on-Si Quasi-Vertical p-n Diode With Junction Termination Extension Based on Hydrogen Plasma Treatment and Diffusion," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 1636–1640, Apr. 2023, doi: 10.1109/TED.2023.3247366.
[86] R. Abdul Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si Quasi-Vertical p-i-n Diodes With BFOM of 2.0 GW/cm2," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.
[87] C. Huber, J. Baringhaus, and M. Henn, *Towards Vertical GaN Power Transistors on Foreign Substrates: The European YESvGaN Project*. DE: VDE VERLAG GMBH, 2023. Accessed: Feb. 12, 2024. [Online]. Available: https://doi.org/10.30420/566091002
[88] Y. Zhang *et al.*, "High-Performance 500 V Quasi- and Fully-Vertical GaN-on-Si pn Diodes," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 248–251, Feb. 2017, doi: 10.1109/LED.2016.2646669.
[89] Z. Bian *et al.*, "Leakage mechanism of quasi-vertical GaN Schottky barrier diodes with ultra-low turn-on voltage," *Appl. Phys. Express*, vol. 12, no. 8, p. 084004, Aug. 2019, doi: 10.7567/1882-0786/ab3297.
[90] Y. Li *et al.*, "Quasi-Vertical GaN Schottky Barrier Diode on Silicon Substrate With 10 10 High On/Off Current Ratio and Low Specific On-Resistance," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 329–332, Mar. 2020, doi: 10.1109/LED.2020.2968392.
[91] X. Guo *et al.*, "Nitrogen-Implanted Guard Rings for 600-V Quasi-Vertical GaN-on-Si Schottky Barrier Diodes With a BFOM of 0.26 GW/cm 2," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5682–5686, Nov. 2021, doi: 10.1109/TED.2021.3108951.
[92] X. Guo *et al.*, "High-Voltage and High-I ON /I OFF Quasi-Vertical GaN-on-Si Schottky Barrier Diode With Argon-Implanted Termination," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 473–476, Apr. 2021, doi: 10.1109/LED.2021.3058380.

[93] J. Chen *et al.*, "High-performance quasi-vertical GaN Schottky barrier diode with anode selective fluorine treatment," *Semicond. Sci. Technol.*, vol. 34, no. 11, p. 115019, Nov. 2019, doi: 10.1088/1361-6641/ab420c.

[94] L. Yates *et al.*, "Demonstration of >6.0-kV Breakdown Voltage in Large Area Vertical GaN p-n Diodes With Step-Etched Junction Termination Extensions," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 1931–1937, Apr. 2022, doi: 10.1109/TED.2022.3154665.

[95] J. Li, R. Zhu, K. M. Wong, and K. M. Lau, "Fully Vertical GaN-on-SiC p-i-n Diodes With BFOM of 2.89 GW/cm ^{2}," *IEEE J. Electron Devices Soc.*, vol. 12, pp. 318–321, 2024, doi: 10.1109/JEDS.2024.3386857.

[96] Y. Zhang *et al.* "GaN-on-Si Vertical Schottky and p-n Diodes," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 618–620, Jun. 2014, doi: 10.1109/LED.2014.2314637.

[97] B.-S. Zheng *et al.*, "Suppression of Current Leakage Along Mesa Surfaces in GaN-Based p-i-n Diodes," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 932–934, Sep. 2015, doi: 10.1109/LED.2015.2458899.

[98] Silvaco, Inc., "Atlas User Manual DEVICE SIMULATION SOFTWARE" https://www.silvaco.com/, Santa Clara, USA, December 2020.

[99] A. Douara, B. Djellouli, A. Rabehi, A. Ziane, and N. Belkadi, "I-V Characteristics Model for AlGaN / GaN HEMTs Using Tcad-Silvaco," *JNTM*, vol. 4, no. 2, pp. 16–24, 2014, doi: 10.12816/0010326.

[100] W. He *et al.*, "1.3 kV Vertical GaN-Based Trench MOSFETs on 4-Inch Free Standing GaN Wafer," *Nanoscale Res Lett*, vol. 17, no. 1, p. 14, Dec. 2022, doi: 10.1186/s11671-022-03653-z.

[101] J. Montes *et al.*, "Demonstration of mechanically exfoliated β -Ga2O3/GaN p-n heterojunction," *Applied Physics Letters*, vol. 114, no. 16, p. 162103, Apr. 2019, doi: 10.1063/1.5088516.

[102] K.-W. Nie *et al.*, "Highly Enhanced Inductive Current Sustaining Capability and Avalanche Ruggedness in GaN p-i-n Diodes With Shallow Bevel Termination," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 469–472, Mar. 2020, doi: 10.1109/LED.2020.2970552.

[103] R. Pieper, S. Michael, and D. Reeves, "Comparison of analytic and numerical models with commercially available simulation tools for the prediction of semiconductor freeze-out and exhaustion," in *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002.*, Tulsa, OK, USA: IEEE, 2002, p. I-40–3. doi: 10.1109/MWSCAS.2002.1187148.

[104] R. Dutta, T. Tamang, P. Paul, and N. Paitya, "Comparative Study of AlGaN/GaN, InAlN/GaN and AlGaAs/GaAs based High Electron Mobilty Transistors Using Silvaco for High-Frequency Applications," in *2020 4th International Conference on Trends in Electronics and Informatics (ICOEI)(48184)*, Tirunelveli, India: IEEE, Jun. 2020, pp. 137–142. doi: 10.1109/ICOEI48184.2020.9142891.

[105] Y. Zhang, M. Sun, D. Piedra, J. Hennig, A. Dadgar, and T. Palacios, "Reduction of on-resistance and current crowding in quasi-vertical GaN power diodes," *Applied Physics Letters*, vol. 111, no. 16, p. 163506, Oct. 2017, doi: 10.1063/1.4989599.

[106] K. Nomoto *et al.*, "GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ-cm2: A record high figure-of-merit of 12.8 GW/cm2," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, USA: IEEE, Dec. 2015, p. 9.7.1-9.7.4. doi: 10.1109/IEDM.2015.7409665.

[107] C. Han, M. Wang, X. Liu, and B. Shen, "Design of Beveled Edge Termination in GaN Vertical p-i-n Diodes: A Simulation Study," in *2022 10th International Symposium on*

Next-Generation Electronics (ISNE), Wuxi, China: IEEE, May 2023, pp. 1–3. doi: 10.1109/ISNE56211.2023.10221630.

[108] Z. Xu, T. Detchprohm, S.-C. Shen, A. N. Otte, and R. D. Dupuis, "Edge Termination Engineering with Shallow Bevel Mesas for Low-Leakage Vertical GaN-based p-i-n Avalanche Photodiode".

[109] H. W. Jang *et al.*, "Low-resistance and thermally stable ohmic contact on p-type GaN using Pd/Ni metallization," *Applied Physics Letters*, vol. 79, no. 12, pp. 1822–1824, Sep. 2001, doi: 10.1063/1.1403660.

[110] W. Wang *et al.*, "Performance Improvement of GaN Based Laser Diode Using Pd/Ni/Au Metallization Ohmic Contact," *Coatings*, vol. 9, no. 5, p. 291, Apr. 2019, doi: 10.3390/coatings9050291.

[111] H. W. Jang, H. K. Cho, J. Y. Lee, and J.-L. Lee, "Microstructural and Electrical Investigation of Low Resistance and Thermally Stable Pd/Ni Contact on p-Type GaN," *J. Electrochem. Soc.*, vol. 150, no. 3, p. G212, 2003, doi: 10.1149/1.1544636.

[112] H. K. Cho, T. Hossain, J. W. Bae, and I. Adesida, "Characterization of Pd/Ni/Au ohmic contacts on p-GaN," *Solid-State Electronics*, vol. 49, no. 5, pp. 774–778, May 2005, doi: 10.1016/j.sse.2005.01.020.

[113] T. Maeda, Y. Koide, and M. Murakami, "Effects of NiO on electrical properties of NiAu-based ohmic contacts for *p* -type GaN," *Applied Physics Letters*, vol. 75, no. 26, pp. 4145–4147, Dec. 1999, doi: 10.1063/1.125564.

[114] H. W. Jang, S. Y. Kim, and J.-L. Lee, "Mechanism for Ohmic contact formation of oxidized Ni/Au on *p* -type GaN," *Journal of Applied Physics*, vol. 94, no. 3, pp. 1748–1752, Aug. 2003, doi: 10.1063/1.1586983.

[115] L.-C. Chen *et al.*, "Microstructural investigation of oxidized Ni/Au ohmic contact to *p* -type GaN," *Journal of Applied Physics*, vol. 86, no. 7, pp. 3826–3832, Oct. 1999, doi: 10.1063/1.371294.

[116] L.-C. Chen *et al.*, "Oxidized Ni/Pt and Ni/Au ohmic contacts to *p* -type GaN," *Applied Physics Letters*, vol. 76, no. 25, pp. 3703–3705, Jun. 2000, doi: 10.1063/1.126755.

[117] C. Mauduit *et al.*, "Importance of layer distribution in Ni and Au based ohmic contacts to p-type GaN," *Microelectronic Engineering*, vol. 277, p. 112020, May 2023, doi: 10.1016/j.mee.2023.112020.

[118] K. Fu *et al.*, "Characterization of MOCVD regrown p-GaN and the interface properties for vertical GaN power devices," *Semicond. Sci. Technol.*, vol. 36, no. 1, p. 014005, Jan. 2021, doi: 10.1088/1361-6641/abc7d1.

[119] A. Uedono *et al.*, "Dopant activation process in Mg-implanted GaN studied by monoenergetic positron beam," *Sci Rep*, vol. 11, no. 1, p. 20660, Oct. 2021, doi: 10.1038/s41598-021-00102-2.

[120] M. Li *et al.*, "Activation of Mg impurities in epitaxial p-GaN with rapid thermal annealing assisted supercritical fluid treatment," *Appl. Phys. Express*, vol. 16, no. 5, p. 055501, May 2023, doi: 10.35848/1882-0786/accdb3.

[121] T. Narita *et al.*, "Progress on and challenges of p-type formation for GaN power devices," *Journal of Applied Physics*, vol. 128, no. 9, p. 090901, Sep. 2020, doi: 10.1063/5.0022198.

[122] Z. X. Qin *et al.*, "Study of Ti/Au, Ti/Al/Au, and Ti/Al/Ni/Au ohmic contacts to n -GaN," *Applied Physics A: Materials Science & Processing*, vol. 78, no. 5, pp. 729–731, Mar. 2004, doi: 10.1007/s00339-002-1989-0.

[123] S. Ruvimov *et al.*, "Microstructure of Ti/Al and Ti/Al/Ni/Au Ohmic contacts for *n* -GaN," *Applied Physics Letters*, vol. 69, no. 11, pp. 1556–1558, Sep. 1996, doi: 10.1063/1.117060.

[124] Z. Z. Chen *et al.*, "Ohmic contact formation of Ti/Al/Ni/Au to n-GaN by two-step annealing method," *Materials Science and Engineering: B*, vol. 111, no. 1, pp. 36–39, Aug. 2004, doi: 10.1016/j.mseb.2004.03.014.
[125] R. Khadar, "GaN vertical power devices on silicon substrates", PhD thesis at EPFL, Switzerland, 2021.
[126] H. Ahmad *et al.*, "Cascaded Ni hard mask to create chlorine-based ICP dry etched deep mesas for high-power devices," *Semicond. Sci. Technol.*, vol. 36, no. 12, p. 125016, Dec. 2021, doi: 10.1088/1361-6641/ac3372.
[127] L.-B. Chang, S.-S. Liu, and M.-J. Jeng, "Etching Selectivity and Surface Profile of GaN in the Ni, SiO 2 and Photoresist Masks Using an Inductively Coupled Plasma," *Jpn. J. Appl. Phys.*, vol. 40, no. 3R, p. 1242, Mar. 2001, doi: 10.1143/JJAP.40.1242.
[128] S. Zhou, B. Cao, and S. Liu, "Dry etching characteristics of GaN using Cl2/BCl3 inductively coupled plasmas," *Applied Surface Science*, vol. 257, no. 3, pp. 905–910, Nov. 2010, doi: 10.1016/j.apsusc.2010.07.088.
[129] K. H. Baik *et al.*, "Effect of PECVD of SiO2 passivation layers on GaN and InGaP," 2001.
[130] M. Henn, C. Huber, D. Scholten, and N. Kaminski, "Effects of the LPCVD Gate Dielectric Deposition Temperature on GaN MOSFET Channels and the Root Causes at the SiO 2 -GaN-Interface," *IEEE Trans. Electron Devices*, vol. 71, no. 3, pp. 1553–1560, Mar. 2024, doi: 10.1109/TED.2023.3347208.
[131] M. Swain, D. Bhattacharya, K. G. Bhushan, and S. Basu, "Deposition of a nickel film by DC magnetron sputtering and its characterization," presented at the INDIAN VACUUM SOCIETY SYMPOSIUM ON THIN FILMS: SCIENCE AND TECHNOLOGY, Mumbai, India, 2012, pp. 182–184. doi: 10.1063/1.4732408.
[132] R. Koch, "Stress in Evaporated and Sputtered Thin Films – A Comparison," *Surface and Coatings Technology*, vol. 204, no. 12–13, pp. 1973–1982, Mar. 2010, doi: 10.1016/j.surfcoat.2009.09.047.
[133] T. K. Zywietz, J. Neugebauer, and M. Scheffler, "The adsorption of oxygen at GaN surfaces," *Applied Physics Letters*, vol. 74, no. 12, pp. 1695–1697, Mar. 1999, doi: 10.1063/1.123658.
[134] R. B. Chung, H.-T. Chen, C.-C. Pan, J.-S. Ha, S. P. DenBaars, and S. Nakamura, "The polarization field dependence of Ti/Al based Ohmic contacts on N-type semipolar GaN," *Applied Physics Letters*, vol. 100, no. 9, p. 091104, Feb. 2012, doi: 10.1063/1.3690878.
[135] T. Jang, S. N. Lee, O. H. Nam, and Y. Park, "Investigation of Pd/Ti/Al and Ti/Al Ohmic contact materials on Ga-face and N-face surfaces of n-type GaN," *Applied Physics Letters*, vol. 88, no. 19, p. 193505, May 2006, doi: 10.1063/1.2201881.
[136] S. Young Moon, J. Ho Son, K. Jin Choi, J.-L. Lee, and H. W. Jang, "Indium as an efficient ohmic contact to N-face *n* -GaN of GaN-based vertical light-emitting diodes," *Applied Physics Letters*, vol. 99, no. 20, p. 202106, Nov. 2011, doi: 10.1063/1.3662421.
[137] H. Seo, Y.-J. Cha, A. B. M. H. Islam, and J. S. Kwak, "Improvement of Ti/Al ohmic contacts on N-face n-type GaN by using O2 plasma treatment," *Applied Surface Science*, vol. 510, p. 145180, Apr. 2020, doi: 10.1016/j.apsusc.2019.145180.
[138] A. Motayed, M. Jah, A. Sharma, W. T. Anderson, C. W. Litton, and S. N. Mohammad, "Two-step surface treatment technique: Realization of nonalloyed low-resistance Ti/Al/Ti/Au ohmic contact to n-GaN," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 22, no. 2, pp. 663–667, Mar. 2004, doi: 10.1116/1.1667506.

[139] L. Redaelli, A. Muhin, S. Einfeldt, P. Wolter, L. Weixelbaum, and M. Kneissl, "Ohmic Contacts on N-Face n-Type GaN After Low Temperature Annealing," *IEEE Photon. Technol. Lett.*, vol. 25, no. 13, pp. 1278–1281, Jul. 2013, doi: 10.1109/LPT.2013.2261808.

[140] R. Zhou *et al.*, "Effect of surface stoichiometry on the non-alloyed ohmic contact to N-face n-GaN," *Solid-State Electronics*, vol. 171, p. 107863, Sep. 2020, doi: 10.1016/j.sse.2020.107863.

[141] Z. Fogarassy *et al.*, "Structural and electrical investigation of Al/Ti/TiN/Au based N-face n-GaN contact stack," *Materials Science in Semiconductor Processing*, vol. 175, p. 108250, Jun. 2024, doi: 10.1016/j.mssp.2024.108250.

[142] D. Khachariya *et al.*, "Chemical treatment effects on Schottky contacts to metalorganic chemical vapor deposited n-type N-polar GaN," *Journal of Applied Physics*, vol. 128, no. 6, p. 064501, Aug. 2020, doi: 10.1063/5.0015140.

[143] S. Grover, S. Sahu, P. Zhang, K. O. Davis, and S. K. Kurinec, "Standardization of Specific Contact Resistivity Measurements using Transmission Line Model (TLM)," in *2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS)*, Edinburgh, UK: IEEE, May 2020, pp. 1–6. doi: 10.1109/ICMTS48187.2020.9107911.

[144] G. K. Reeves and H. B. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Electron Device Lett.*, vol. 3, no. 5, pp. 111–113, May 1982, doi: 10.1109/EDL.1982.25502.

[145] M. Grodzicki, J.-G. Rousset, P. Ciechanowicz, E. Piskorska-Hommel, and D. Hommel, "XPS studies on the role of arsenic incorporated into GaN," *Vacuum*, vol. 167, pp. 73–76, Sep. 2019, doi: 10.1016/j.vacuum.2019.05.043.

[146] Y. Jung *et al.*, "Chemical Etch Characteristics of N-Face and Ga-Face GaN by Phosphoric Acid and Potassium Hydroxide Solutions," *J. Electrochem. Soc.*, vol. 159, no. 2, pp. H117–H120, 2011, doi: 10.1149/2.039202jes.

[147] K. Prabhakaran, T. G. Andersson, and K. Nozawa, "Nature of native oxide on GaN surface and its reaction with Al," *Applied Physics Letters*, vol. 69, no. 21, pp. 3212–3214, Nov. 1996, doi: 10.1063/1.117964.

[148] S. S. Kushvaha *et al.*, "Structural, optical and electronic properties of homoepitaxial GaN nanowalls grown on GaN template by laser molecular beam epitaxy," *RSC Adv.*, vol. 5, no. 107, pp. 87818–87830, 2015, doi: 10.1039/C5RA11361J.

[149] B. S. Choi *et al.*, "Wet etching of Ga_2O_3 epitaxy film using a HCl-based solution," *Journal of the Korean Crystal Growth and Crystal Technology*, vol. 32, no. 1, pp. 40–44, Feb. 2022, doi: 10.6111/JKCGCT.2022.32.1.040.

[150] J.-S. Jang, S.-J. Park, and T.-Y. Seong, "Effects of Surface Treatment on the Electrical Properties of Ohmic Contacts to (In)GaN for High Performance Optical Devices," *phys. stat. sol. (a)*, vol. 194, no. 2, pp. 576–582, Dec. 2002, doi: 10.1002/1521-396X(200212)194:2<576::AID-PSSA576>3.0.CO;2-W.

[151] H. M. Ng, N. G. Weimann, and A. Chowdhury, "GaN nanotip pyramids formed by anisotropic etching," *Journal of Applied Physics*, vol. 94, no. 1, pp. 650–653, Jul. 2003, doi: 10.1063/1.1582233.

[152] S.-C. Han *et al.*, "Formation of Hexagonal Pyramids and Pits on V-/VI-Polar and III-/II-Polar GaN/ZnO Surfaces by Wet Etching," *J. Electrochem. Soc.*, vol. 157, no. 1, p. D60, 2010, doi: 10.1149/1.3253564.

[153] J. Streque, "Dispositifs d'Affichage de Sensations Tactiles à Base de Microsystèmes Électro-Mécaniques (MEMS) Magnétiques: Conception, Réalisation et Tests", PhD thesis at Centrale Lille, France, 2011.

[154] A. Krost, A. Dadgar*, G. Strassburger, and R. Clos "GaN-based epitaxy on silicon: stress measurements," phys. stat. sol. (a) 200, No. 1, 26–35 (2003) / DOI 10.1002/pssa.200303428

[155] C. Roder, S. Einfeldt, S. Figge, and D. Hommel, "Temperature dependence of the thermal expansion of GaN," *Phys. Rev. B*, vol. 72, no. 8, p. 085218, Aug. 2005, doi: 10.1103/PhysRevB.72.085218.

[156] M. A. Moram and M. E. Vickers, "X-ray diffraction of III-nitrides," *Rep. Prog. Phys.*, vol. 72, no. 3, p. 036502, Mar. 2009, doi: 10.1088/0034-4885/72/3/036502.

[157] T. Tanaka, N. Kaneda, T. Mishima, Y. Kihara, T. Aoki, and K. Shiojima, "Roles of lightly doped carbon in the drift layers of vertical n-GaN Schottky diode structures on freestanding GaN substrates," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, p. 041002, Apr. 2015, doi: 10.7567/JJAP.54.041002.

[158] A. Dadgar, J. Bläsing, A. Diez, and A. Krost, "Crack-Free, Highly Conducting GaN Layers on Si Substrates by Ge Doping," *Appl. Phys. Express*, vol. 4, no. 1, p. 011001, Jan. 2011, doi: 10.1143/APEX.4.011001.

[159] R. Kaur, "A Review on Power MOSFET Device Structures," *IJRASET*, vol. V, no. X, pp. 208–218, Oct. 2017, doi: 10.22214/ijraset.2017.10034.

[160] A. Bazigos *et al.*, "A Physics-Based Analytical Compact Model for the Drift Region of the HV-MOSFET," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1710–1721, Jun. 2011, doi: 10.1109/TED.2011.2119487.

[161] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully Vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, Mar. 2019, doi: 10.1109/LED.2019.2894177.

[162] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Effects of p-GaN Body Doping Concentration on the ON-State Performance of Vertical GaN Trench MOSFETs," *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 970–973, Jul. 2021, doi: 10.1109/LED.2021.3080260.

[163] S. A. Suliman *et al.*, "The impact of trench geometry and processing on the performance and reliability of low voltage power UMOSFETs," in *2001 IEEE International Reliability Physics Symposium Proceedings. 39th Annual (Cat. No.00CH37167)*, Orlando, FL, USA: IEEE, 2001, pp. 308–314. doi: 10.1109/RELPHY.2001.922920.

[164] C. Gupta *et al.*, "Comparing electrical performance of GaN trench-gate MOSFETs with a-plane and m-plane sidewall channels," *Appl. Phys. Express*, vol. 9, no. 12, p. 121001, Dec. 2016, doi: 10.7567/APEX.9.121001.

[165] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistors on GaN Bulk Substrates," *Appl. Phys. Express*, vol. 1, no. 1, p. 011105, Jan. 2008, doi: 10.1143/APEX.1.011105.

[166] Y. Wang *et al.*, "High-Performance Normally-Off Al2O3/GaN MOSFET Using a Wet Etching-Based Gate Recess Technique," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1370–1372, Nov. 2013, doi: 10.1109/LED.2013.2279844.

[167] M. Kodama *et al.*, "GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistor Fabricated with Novel Wet Etching," *Appl. Phys. Expr.*, vol. 1, p. 021104, Feb. 2008, doi: 10.1143/APEX.1.021104.

[168] D. I. Shahin, T. J. Anderson, and A. Christou, "(Invited) Achieving Vertical Trench-Gate GaN MOSFETs via Process Optimization," *ECS Trans.*, vol. 80, no. 7, pp. 139–145, Aug. 2017, doi: 10.1149/08007.0139ecst.

[169] Y.-C. Chu *et al.*, "Performance Comparisons of GaN Vertical Transistors with Sidewalls Treated by TMAH and H3PO4 Solutions," *IEEE Electron Device Lett.*, pp. 1–1, 2024, doi: 10.1109/LED.2024.3448196.

[170] Y. Zhang *et al.*, "Trench formation and corner rounding in vertical GaN power devices," *Applied Physics Letters*, vol. 110, no. 19, p. 193506, May 2017, doi: 10.1063/1.4983558.

[171] P. Godignon, J. Montserrat, J. Rebollo, and D. Planson, "Edge Terminations for 4H-SiC Power Devices: A Critical Issue," *MSF*, vol. 1062, pp. 570–575, May 2022, doi: 10.4028/p-lom714.

[172] Faculty of Engineering and Green Technology, Universiti Tunku Abdul Rahman, Kampar, Malaysia, K. H. Yeap, H. Nisar, Faculty of Engineering and Green Technology, Universiti Tunku Abdul Rahman, Kampar, Malaysia, V. Dakulagi, and Department of Electronics and Communication Engineering, Guru Nanak Dev Engineering College, Karnataka, India, "Warpage Reduction for Power MOSFET Wafers," *Electrica*, vol. 21, no. 2, pp. 173–179, May 2021, doi: 10.5152/electrica.2021.21019.

[173] C. Gupta, S. H. Chan, Y. Enatsu, A. Agarwal, S. Keller, and U. K. Mishra, "OG-FET: An In-Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1601–1604, Dec. 2016, doi: 10.1109/LED.2016.2616508.

[174] M. Xiao *et al.*, "First Demonstration of Vertical Superjunction Diode in GaN," in *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA: IEEE, Dec. 2022, p. 35.6.1-35.6.4. doi: 10.1109/IEDM45625.2022.10019405