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RFSOI Technology Development by means of new substrate methodologies for 5G Applications

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Développement de la technologie RFSOI au moyen de nouvelles méthodologies de substrat pour les applications 5G

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Chi più alto sale, più lontano vede.
Chi più lontano vede, più a lungo sogna.

Walter Bonatti

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Glossary

Body Contact (BC) A MOSFET configuration that permits to control body potential via a dedicated pad.

Buried Oxide (BOx) The oxide layer buried into a SOI substrate.

Complementary Metal Oxide Semiconductor (CMOS) A logic family based on n- and p-type MOSFET devices, dominant in nowadays digital circuits.

Contact Etch Stop Layer (CESL) A layer employing for defining contacts in a MOSFET that can also be used as stressor method.

Energy-Dispersive X-ray Spectroscopy (EDX) An Analytical technique used for the elemental analysis or chemical characterization of a sample based on the study of its emission spectrum.

Figure of Merit (FoM) A numerical quantity based on one or more characteristics of a system or device that represents a measure of efficiency or effectiveness.

Floating Body (FB) A MOSFET configuration for which the body potential cannot be controlled, leaving the body floating.

Fully-Depleted SOI (FDSOI) A semiconductor technology that uses a thin layer of silicon on an insulating substrate to create transistors with fully depleted channels.

High-Resolution X-ray Diffraction (HRXRD) Analytical technique used to characterize the structural properties of crystalline materials.

Low-Noise Amplifier (LNA) An electronic amplifier designed to amplify very weak signals while adding minimal noise to the signal.

Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) A type of transistor for which a conductive channel between two terminals is formed by varing the potential drop across an oxide.

Millimeter Waves (mmWaves) Electromagnetic waves with frequencies between 30 GHz and 300 GHz, corresponding to wavelengths of 1 to 10 millimeters

Partially-Depleted SOI (PDSOI) A semiconductor technology where the silicon layer on an insulating substrate is thick enough that the transistor channel is only partially depleted of charge carriers during operation.

Power Amplifier (PA) An electronic device that amplifies low-power signals to a higher power level.

Precession Electron Diffraction (PED) Analytical technique used to characterize the strain content in a sample based on the study of its electron diffraction pattern.

RF Front End Module (RF FEM) The assembly of components that processes radio frequency signals before the digital baseband system.

RF switch An electrical components that isolates the transmitter and receiver portions of an RF FEM.

Short Channel Effects (SCE) The assembly of parasitic effects that occur in a MOSFET when channel length is drastically reduced.

Silicon On Insulator (SOI) Particular type of silicon substrate featuring an oxide layer buried below the surface.

Stress Memorization Technique (SMT) A method to induce stress into a MOSFET channel by depositing an intrinsically stressed layer.

Technolgy Computer-Aided Design (TCAD) Design of semiconductor devices with the help of computer simulations.

1

Introduction to RF and mm-Waves world

In recent years, the explosive increase in mobile data usage has led to a greater demand for improving the performance of RF Front-End Modules (FEMs). Devices now need to support a wide range of spectrum bands, from low to high, to accommodate various technologies like 5G, 4G, 3G, WiFi, Bluetooth, and Near Field Communications [1, 2, 3]. This requires enhancements in RF FEM capabilities to manage these frequency bands effectively. On one side, addressing this need involves refining circuit design. On the other, semiconductor companies are tasked with producing transistors that offer superior performance in terms of frequency operation, power handling, and energy consumption. In particular, the improvements of transistors' transconductance, and current and power cutoff frequencies (f_{T} and f_{MAX}) is essential for the development of the next generation of Low-Noise Amplifiers (LNAs) and Power Amplifiers (PAs). For switches, the ideal transistor would exhibit minimal On resistance, R_{ON}, and Off capacitance, C_{OFF}, without compromising on high breakdown voltage values.

The first chapter of this thesis will be the starting point of this work and will aim to explain the reasons for this study in a complete yet concise manner. Initially, an overview of a basic RF Front-End Module's architecture will be given in Section 1.1, outlining and explaining the role of its building blocks. We then focus on the description of the main components of an RF FEM, demonstrating how their performances are tightly related to those of transistor devices. In particular, LNA and RF switch devices will be addressed since the transistor devices developed and presented in this work have applications for these two components, leaving the PAs for future work. The figures of merit for LNAs and RF switches will be discussed in more detail in Section 1.2. Section 1.3 will present the motivations driving researchers and engineers to develop devices and circuits in the mm-Waves range, highlighting the advantages and potential applications. In Section 1.4, we will review and compare the various existing technologies, explaining why silicon-based technologies are crucial in this field. This section will also address the differences

between SiGe HBT and RF SOI transistors. Additionally, the CMOS65SOIMMW technology will be introduced and compared to other market competitors. Finally, we will discuss the methods used to enhance device performance and outline the organization of the manuscript.

1.1 RF Front-End Module

1.1.1 Transceiver

"RF Front-End Module" defines the crucial portion of a telecommunication standard circuitry between antenna and the digital baseband system, primarily consisting of a transceiver, which in turn is constitued of a transmitter and a receiver (hence the name $trans - ceiver$) [4] (Fig. 1.1).

The transmitter component of the FEM is tasked with the modulation of a baseband information signal onto a high-frequency carrier wave. This modulated signal is then propelled through an antenna, reaching its target destination. The transmitter's architecture includes a generator for the carrier signal, a modulator, and typically, a high-frequency PA. The PA is strategically placed before the antenna to enhance the signal's power, ensuring effective transmission over the required distances [5].

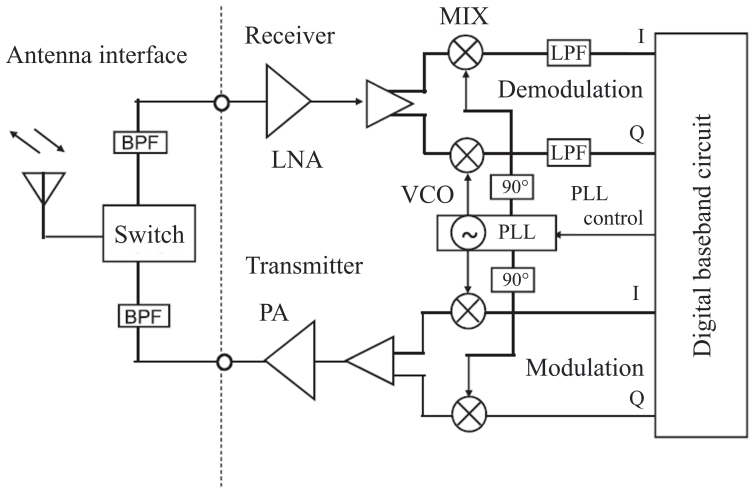


Fig. 1.1.: A schematic representation of a common FEM transceiver is shown in figure. In particular, the antenna interface with the block dedicated to the switches that separate the receiver and transmitter can be distinguished. Some specific components are also reported, such as Bandpass Filters (BPFs), Voltage Controlled Oscillators (VCOs), mixer (MIX), Phase-Locked Loops (PLL), and Lowpass Filters (LPFs).

The receiver serves as the counterpart to the transmitter, executing the reverse operation. Its primary function is to isolate and retrieve the desired modulated carrier signal from the myriad of signals and interferences in the transmission environment. The receiver then amplifies and demodulates this signal to extract the embedded information [6, 7]. This process is typically more complex than the transmitter's function due to the weak nature of incoming signals. A receiver must be designed with a high dynamic range, low noise floor, excellent selectivity, and very high gain to overcome these challenges effectively. To meet these needs, the receiver employs a strategic combination of bandpass filters and Low-Noise Amplifiers. LNAs play a vital role in amplifying the incoming signal with as little added noise as possible, preserving the integrity of the information. Demodulation stage follows, where the information signal is separated from the carrier wave using a demodulator, finally recovering the orginal information content.

As transmitter and receiver share the same antenna in a tranceiver, maintaining a high degree of isolation between the two blocks is imperative. This precaution is necessary to prevent the powerful outgoing signal from the transmitter from overwhelming the receiver, which could lead to saturation and compromise its performance. RF switches are usually employed for this scope, providing high isolation level between the two blocks. The key to a transceiver's successful operation lies in the ability to achieve substantial isolation between its receiver and transmitter components. This, coupled with proficient power control strategies, forms the backbone of a well-functioning transceiver system.

1.1.2 Low-Noise Amplifier

In the signal reception process, the LNA respresents the first stage of amplification and is a pivotal factor in determining the sensistivity of the entire receiver. The primary challenge for an LNA is to amplify the signal cleanly, increasing its strength without introducing additional noise that could degrade the signal quality.

The performance of a receiver with multiple cascaded stages, denoted as N stages, hinges on each stage's gain and noise characteristics. These are quantified by the stage's available power gain, G, and its noise factor, F. The overall noise factor for the entire cascaded system can be calculated using Friis' formula [8]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + ... + \frac{F_{\text{N}} - 1}{G_1 G_2 ... G_{\text{N-1}}} \tag{1.1}$$

This formula is instrumental in assessing the cumulative impact of each stage's noise contribution on the system's total performance. It can be demonstrated that the two-ports networks should be arranged in a sequence that corresponds to their noise factor, from the lowest to the highest. This configuration ensures that the initial stage, with its low noise factor and large gain value, minimizes the noise contributions from the stages that follow. Moreover, enhancing the dynamic range to ensure linearity, lowering power consumption, and keeping the input reflection coefficient within acceptable limits across the desired bandwidth are also required for improving the LNA performances. Balancing these factors is crucial for the LNA to perform at its best within the receiver system.

Throughout the evolution of LNAs, both field-effect transistors (FETs) and bipolar transistors have been utilized in their construction. Within the field-effect category, various types of transistors such as MOSFETs, along with their advanced forms like SOI [9], FinFETs [10], and nanowire FETs, as well as high electron mobility transistors (HEMTs) [11], are included. For high-frequency bipolar devices, the most commonly used are SiGe HBTs [12], GaAs HBTs, and InP HBTs [13], where HBT stands for heterojunction bipolar transistor.

As for an LNA the most important factors are noise and gain, even for transistor devices the most pertinent FoMs include NF_{MIN}, which represents the minimum noise figure, the maximum current gain frequency f_T and the maximum power gain frequency f_{MAX}. These FoMs, which will be discussed in greater detail later in the next section (cf. Section 1.2), are intrinsically related to the LNA frequency working range and performances. As an example, a common linearity figure of merit, which is proportional to the third-order intercept point (IIP3), can be used for LNAs. It involves the second-order derivative of f_T or f_{MAX} with respect to the gate-source voltage (V_{GS}) [4]:

$$IIP3 \propto \left[\frac{f_T}{\frac{\partial^2 f_T}{\partial V_{GS}^2}} \right] \text{ or } IIP3 \propto \left[\frac{f_{MAX}}{\frac{\partial^2 f_{MAX}}{\partial V_{GS}^2}} \right] \tag{1.2}$$

In the design phase of an LNA, it is crucial to bias the transistors optimally to achieve the best possible gain and linearity. This ensures that the LNA operates effectively within its intended application, providing clear signal amplification with minimal distortion.

1.1.3 Switches

For a transceiver to operate effectively, it is critical to ensure robust isolation between the transmitter and receiver sections. This is commonly accomplished with the strategic use of filters and switches to segregate the operational paths (Fig. 1.2). Both p-i-n (PIN) diodes and Schottky diodes are viable options for such switches, capable of alternating between forward and reverse bias states. However, they necessitate a direct bias voltage to be applied to the RF signal port, typically through a low-pass filter, and their integration with transistor technology can be expensive. FETs offer an alternative with the benefit of a third terminal, which permits the control voltage to be isolated from the signal path, eliminating the need for additional filtering. Historically, GaAs p-HEMTs or Silicon-on-Sapphire were the preferred choices for RF switches due to their superior performance over Silicon-based technologies [14, 15]. Yet, continuous advancements have seen CMOS technology overtake these older methods [16]. The advent of RFSOI solutions has significantly cut costs while greatly enhancing integration capabilities.

The critical performance metrics for a switch are its insertion loss, IL, and isolation, I. For the series portion of a switch (as reported in Fig. 1.2) characterized by R_{SW} and C_{SW}, the insertion loss and isolation can be calculated as:

$$IL = 20 \cdot log_{10}(1 + \frac{R_{\mathrm{SW}}}{2 \cdot Z_0}) \text{ and } I = 10 \cdot log_{10}[1 + (4\pi f \cdot C_{\mathrm{SW}} \cdot Z_0)^{-2}] \tag{1.3}$$

Similarly, the insertion loss and isolation of the shunt portion is obtained from

$$IL = 10 \cdot log_{10}[1 + (\pi f \cdot C_{\mathrm{SW}} \cdot Z_0)^2] \text{ and } I = 20 \cdot log_{10}(1 + \frac{Z_0}{2 \cdot R_{\mathrm{SW}}}) \tag{1.4}$$

Usually we can define $R_{SW} = n \cdot R_{ON}$ and $1/C_{SW} = n/C_{OFF}$, where R_{ON} and C_{OFF} are the On resistance and the Off capacitance of the single transistors and n the number of stacked transistors in the switch. Hence, these formulas reveal that switch's performance is heavily influenced by the characterisitics of the single transistors that compose it. Both components, R_{ON} and C_{OFF}, should ideally be minimized. Indeed, the insertion loss of an RF switch can adversely affect the system's overall performance, potentially increasing the receiver's noise figure, diminishing the transmitter's output power, and lowering the power-added-efficiency of the PA. Thus, reducing the insertion loss of the antenna switch is a vital design consideration. Moreover, given that the switch must manage the substantial signal

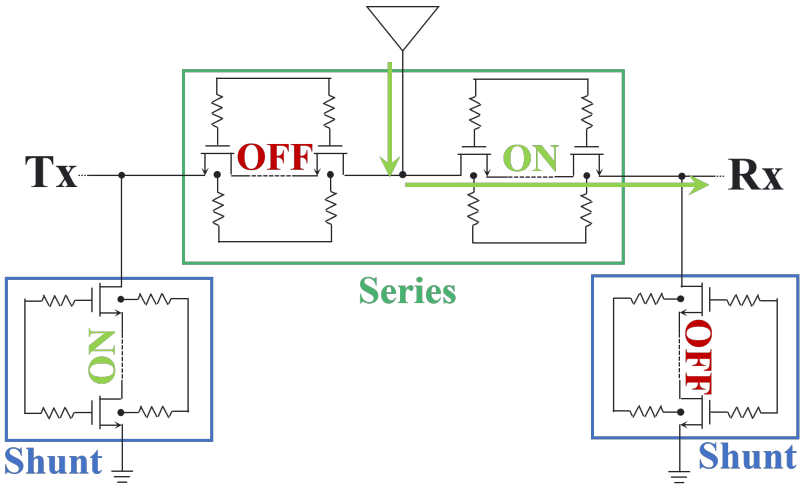


Fig. 1.2.: The circuit of an RF switch is schematically represented. The transducer (Tx) and the receiver (Rx) are alternately connected to the antenna through the activation (On state) and deactivation (Off state) of the two portions of the switch connected in series. The shunt portions are used to reduce signal power losses.

from the transmitter, it is essential that its transistors have a high breakdown voltage to handle these demands safely.

1.2 RF Figures of Merit

In the previous section, we introduced Low Noise Amplifier (LNA) and RF switch devices, key components of Front-End Modules. The figures of merit (FoMs) for the transistors that constitute these elements vary significantly. While for LNAs, the primary FoMs include the transition frequency f_T, the maximum oscillation frequency f_{MAX}, and the minimum noise figure NF_{min}, for RF switches the most pertinent FoMs are the On resistance R_{ON}, the Off capacitance C_{OFF}, and the RF breakdown voltage, also called RFV_{MAX}. In this thesis, only f_T and f_{MAX} will be considered for LNA devices, leaving the analysis of NF_{min} to future studies. These FoMs are essential for determining how performant LNA and switch components are, and their improvement is necessary for pushing further the capabilities of RF FEMs. In this chapter, we will analyze and explain the considered figures of merit, highlighting the specific transistor characteristics they depend on. Firstly, LNA FoMs will be examinated. Subsequently, the following section will be dedicated to the RF switch devices FoMs, providing a comprehensive overview of how they are measured through the usage of "shunt" and "series" configurations and explaining RF breakdown.

1.2.1 The LNA FoMs f_T and f_{MAX}

f_T and f_{MAX} are two of the most important FoMs for LNA devices. Semiconductor companies have always targeted to address higher values of these parameters to enable the production of FEMs that could work at higher frequencies. f_T and f_{MAX} can be explained by using the scheme of a two-port network for describing a transistor, as the one reported in Fig 1.3. In this scheme the port numbered as 1 represents the gate, the node usually used to inject the input signal in the transistor, while port 2 can be seen as the drain [17]. Assuming a linear behavior of such device, the current flowing through it can be described as follows:

$$\begin{aligned} I_1 &= Y_{11}U_1 + Y_{12}U_2 \\ I_2 &= Y_{21}U_1 + Y_{22}U_2 \end{aligned} \quad \text{or} \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \end{bmatrix} \quad \text{or} \quad \mathbf{I} = \mathbf{YU} \tag{1.5}$$

The matrix introduced in the vectoral form of the linear system is the **Y**-matrix, also called the admittance matrix. It consists of the input and output admittances, Y_{11} and Y_{22} respectively, and the transfering admittanced, Y_{12} and Y_{21}. The transition frequency f_T is the frequency at which the current gain of a transistor drops to 1 (0 dB). Current gain, h_{21}, is defined as the ratio between the drain current and the gate current, which in terms of **Y**-matrix can be approximated to

$$h_{21} \approx \frac{Y_{21}}{Y_{11}} \tag{1.6}$$

Since Y_{21} represents the transadmittance of the MOSFET and Y_{11} is associated to input capacitances, we can write:

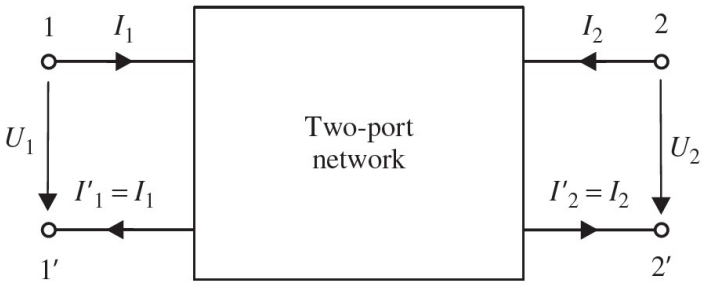


Fig. 1.3.: The diagram of a two-port network is reported with the definition of currents and voltages.

$$Y_{21} = g_{\mathrm{m}} - j\omega C_{\mathrm{GD}}$$
$$Y_{11} = j\omega(C_{\mathrm{GS}} + C_{\mathrm{GD}}) \tag{1.7}$$

g_{m}, C_{GD}, and C_{GS} are the transconductance, gate-to-drain and gate-to-source capacitance, respectively. These parameters can be extracted from the small-signal equivalent circuit anaysis, which is discussed in detail in Appendix A. As said f_{T} is the frequency at which $h_{21} = 1$, and from Eq. 1.7 this brings to the condition

$$f_{\mathrm{T}} \approx \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{GD}} + C_{\mathrm{GS}})} \tag{1.8}$$

which is the common formula used for describing f_{T} as a function of transistor's characteristics [18, 19, 20, 21]. f_{T} is hence a measure of the maximum frequency at which a transistor can amplify a signal. As usually devices reach way higher frequencies than the ones handled by usual measurement equipments, the value of f_{T} is obtained by performing **S**-parameters measurements at different frequencies f and from the h_{21}-vs-f plot the value is extrapolating on the -20 dB/dec current-gain slope (Fig. 1.4). Improving this figure of merit is essential for several reasons, such as enabling LNA to operate over a broader bandwidth, which is crucial for accomodating

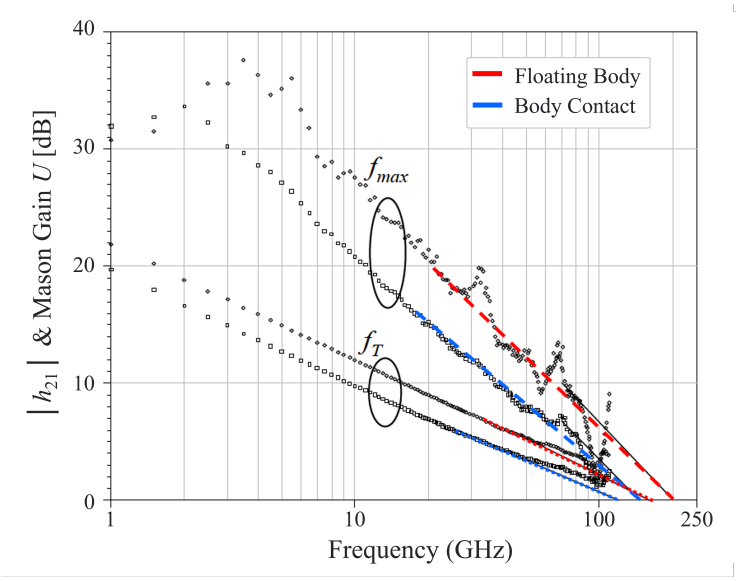


Fig. 1.4.: Given the limited capacity of the measuring instruments, f_{T} and f are extracted through extrapolation of the h_{21} and U curves upon reaching the value of 0 dB. In the body contact configuration, the additional parasitic capacitance between the body and the gate determines the degradation of the maximum performance that a device can achieve.

various communication standards and enhancing versatility. As reported by Eq. 1.8, one can reduce parasitic capacitances or increase g_{m}, which in particular depends on electrons mobility. Among other methods, the latter can be enhanced by inducing tensile strain in the silicon channel, as will be seen in the following chapters (cf. Appendix B).

Despite the widespread reference to the transit frequency f_{T} in literature due to its ease of extraction and the reliable analytical expressions that have been repeatedly validated, the maximum oscillation frequency f_{MAX} serves as a more practical figure of merit.

f_{MAX} is the frequency at which the power gain of a device drops to 1 (0 dB) when considering the contributions of both the transconductance and the parasitic capacitances and resistances of a MOSFET. Unlike f_{T}, which is limited by current transfer capability, f_{MAX} also considers resistive losses and parasitic reactances that accumulate at high frequencies. f_{MAX} can be explained by means of the unilateral power gain (U) of Mason [22, 23]. This is a measure that accounts for feedback effects (Y_{12}) and represents the maximum gain that can be obtained from a device when it is made unilaterally stable (i.e. by eliminating reverse feeback effects). The expression for U for a MOSFET is given by

$$U = \frac{|Y_{21}|^2}{4[Real(Y_{11})Real(Y_{22})]} \tag{1.9}$$

At high frequencies, resistive losses and parasitic capacitances dominate, reducing the power gain, and f_{MAX} can be rewritten as a function of transistor's characteristics [20, 24]:

$$f_{\mathrm{MAX}} \approx \frac{f_{\mathrm{C}}}{2\sqrt{(R_{\mathrm{g}} + R_{\mathrm{d}} + R_{\mathrm{s}})(g_{\mathrm{DS}} + g_{\mathrm{m}}\frac{C_{\mathrm{GD}}}{C_{\mathrm{GS}}})}} \tag{1.10}$$

with f_{C} being:

$$f_{\mathrm{C}} = \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{GS}}} \tag{1.11}$$

In Eq. 1.10, R_{g}, R_{d}, and R_{s} are the so-called extrinsic resistances of gate, drain, and source, respectively, while g_{DS} is the conductance of the device, which can all be extracted from the small-signal equivalent circuit analysis (cf. Appendix A). Similar to the transit frequency, f_{MAX} is extrapolated from power gain measurements at

lower frequencies, following the -20 dB/dec power gain slope (Fig. 1.4). Enhancing f_{MAX} means that the transistor can sustain power gain and be more stable at higher frequencies, which is vital for efficient signal amplification. From Eq. 6.6, improving f_{MAX} means improving g_{m} but also reducing parasitic capacitances and resistances.

1.2.2 RF switch FoMs

If on one hand for LNA devices working frequencies are the main properties defining transistors capabilities, for switch applications the ability to mantain low power losses assumes importance. As introduced in the previous chapter, RF switches performances can be described by the insertion loss and isolation, which are defined as

$$IL = 10 \cdot log_{10}[1 + (\pi f \cdot C_{\mathrm{SW}} \cdot Z_0)^2] \text{ and } I = 20 \cdot log_{10}(1 + \frac{Z_0}{2 \cdot R_{\mathrm{SW}}}) \tag{1.12}$$

with $R_{\mathrm{SW}} = n \cdot R_{\mathrm{ON}}$ and $C_{\mathrm{SW}} = n/C_{\mathrm{OFF}}$, where n is the number of stacked transistors in the switch. Eq. 1.12 show that switches are strongly impacted by the R_{ON} and C_{OFF} of the devices that compose them. R_{ON} is the resistance of a transistor in its On state, while C_{OFF} is the drain-source capacitance of the same transistor when it is turn into the Off state. These two properties can be evaluated by conducting **S**-parameters measurements on two different device configurations.

R_{ON} is obtained using the device in the so-called "shunt" configuration, as the one reported in Fig 1.5a. This configuration inherently eliminates losses from pads and connections, without requiring additional dummy structures, and permits the extraction of the Tee-Matrix, that is the inductance matrix **Z**. Considering Fig. 1.5a, if one knows all Z_{i} but Z_3 ($\approx R_{\mathrm{ON}}$), R_{ON} can be extracted from the elements Z_{12} and Z_{21} as

$$R_{\mathrm{ON}} = \frac{1}{2} Re(Z_{12} + Z_{21}) \tag{1.13}$$

R_{ON} represents the resistance of the transistor's channel isolated from extrinsic contributions (Fig. 1.6). Its value depends purely on factors related to conduction in the channel, such as the gate length L_{G}, the amount of charge in the inversion layer, and electron mobility. Electron mobility is influenced by channel doping and the presence of strain. Similar to LNA devices, introducing strain in RF switch devices enhances electron mobility, significantly reducing R_{ON}.

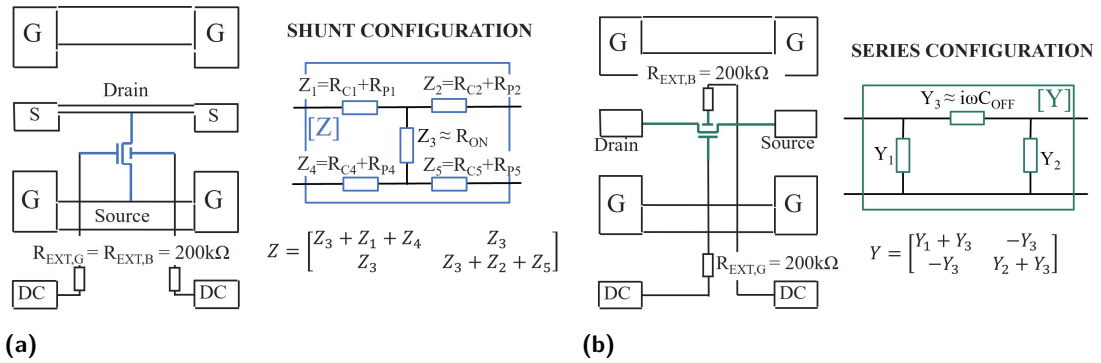


Fig. 1.5.: Schematic representations of a device in a) shunt and b) series configuration are shown with the corresponding impedance and admittance matrix, employed to extract R_{ON} and C_{OFF}.

Similarly, C_{OFF} is extracted from an identical device configured in "series" (Fig. 1.5b). This ensures consistent measurement conditions for C_{OFF} and enables the extraction of the Pi-Matrix, that is the admittance matrix $\mathbf{Y}$. From this, one can obtain C_{OFF} as

$$C_{\mathrm{OFF}} = -\frac{1}{2} Im(Y_{12} + Y_{21})/\omega \tag{1.14}$$

C_{OFF} consists of the gate-to-drain/source capacitance C_{GDS} and the body-to-drain/source capacitance (C_{BDS}), as described by the following formula:

$$C_{\mathrm{OFF}} = \frac{C_{\mathrm{GDS}} + C_{\mathrm{BDS}}}{2} \tag{1.15}$$

With $C_{\mathrm{GDS}} = 2 \cdot C_{\mathrm{GD}} = 2 \cdot C_{\mathrm{GS}}$ and $C_{\mathrm{BDS}} = 2 \cdot C_{\mathrm{JUNC}}$. C_{GD} or C_{GS} can be further broken down into three parallel components: C_{IF}, C_{OF}, and C_{OV} [25]. These three capacitances are represented in Fig. 1.6: C_{IF} is the so-called inner-fringing capacitance, the gate-junctions capacitances internal to the device. Similarly, C_{OF}, the outer-fringing capacitance, forms between gate and junctions but externally, passing through the spacers. Finally, C_{OV} is the overlap capacitance, that is the portion of the total capacitance C_{OX} covered by L_{OV}, which is the extension of the overlap of the Lightly Doped Drain (LDD) with the gate. The improvement of C_{OFF} requires the reduction of these parasitic capacitances. C_{IF} normally assumes the highest values of the three, thus being the contribution that impacts the most Off-state performance. As will be shown in the next chapters, its value is strongly impacted by the SOI thickness t_{SOI}, and it reduces when t_{SOI} decreases (cf. Chapter 2).

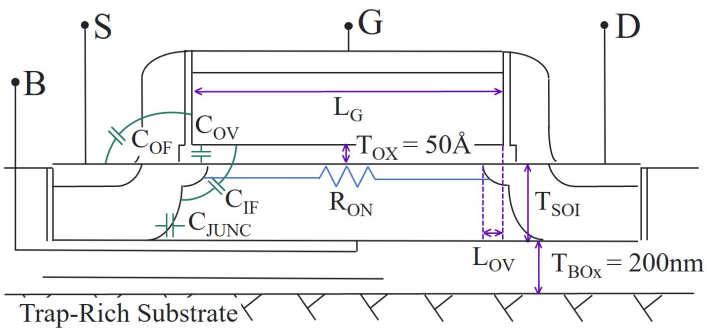


Fig. 1.6.: Schematic representation of an RF switch device showing the three components of $C_{\text{G-DS}}$, C_{OF}, C_{IF}, and C_{OV}, and the ON channel resistance R_{ON}.

Evaluating these two figures of merit alone is insufficient to fully describe the performance of transistors for switch applications. It is also necessary to consider the maximum power that can be transmitted through the device without significant attenuation. This involves studying the device's linearity and how a signal is distorted. This study is conducted by measuring the output power P_{OUT} of the fundamental and of the second and third harmonic H_2 and H_3 as a function of the input power P_{IN}, as shown in Fig. 1.7. The measurement is typically carried out in the Off state in a shunt configuration, the same used for evaluating R_{ON}. This subjects the device to higher electrical stress. The nature of the initial signal degradation, resulting in harmonic generation, is not yet fully understood. However, it appears to be related to the generation of parasitic effects in the substrate and to the extrinsic capacitances of the DUT [26, 27, 28, 29, 30, 31, 32, 33]. Increasing the power eventually leads to a marked increase in harmonics, causing a reduction in the fundamental power by 1 dBm. The input power at which this increase occurs is known as the compression point P_{1dBm}, marking the breakdown point of the device, beyond which its response is no longer linear, rendering it unsuitable as a switch. The compression point value is often converted into volts and referred to as RFV_{max}, according to the following formula:

$$RFV_{\text{max}} = \sqrt{10^{\frac{P_{\text{1dBm}}}{10}-1}} \tag{1.16}$$

This conversion is a convention that facilitates comparison with DC breakdowns. The origin of the breakdown and the factors influencing RFV_{max} are still under debate. This thesis contributes significantly to explaining the phenomenon, relating it to three commonly observed events in DC (cf. Chapter 2): the triggering of the parasitic NPN bipolar, Gate-Induced Drain Leakage (GIDL), and punch-through between drain and source. Controlling these phenomena through device fabrication

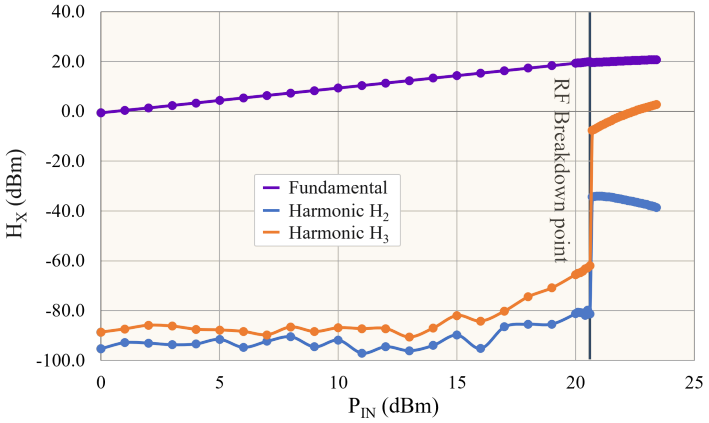


Fig. 1.7.: The graph shows the linearity measurement of an RF switch device. The input power level at which harmonics increase drastically marks the point where the switch device loses its linearity and, therefore, can no longer be used for this purpose. This point is known as $P_{1\mathrm{dBm}}$, but it is more commonly converted into volts, thus obtaining the RFV_{max} value of the device.

process optimization increases RFV_{max} and the maximum RF powers that can be used.

1.3 The reasons for moving towards mm-Waves

As we saw, the RF Front-End Module is essential in wireless communication, as it acts as the bridge between the airwaves and electronic devices. This module uses components like Low Noise Amplifiers, Power Amplifiers, and RF switches to handle signals of various bandwidths, depending on both the design of these components and the performance of the transistors they are made of. The frequency range for which an FEM can be used depends on the characteristics of the devices that compose it and its circuit. To date, frequencies below 3 GHz have been adopted for most telecommunications applications. Especially driven by the need for faster wireless data transfer, the industry has moved to using higher frequency bands as they can support wider bandwidths, recently entering the so called millimeter-Waves range.

The term "millimeter-Waves bands" is applied to the two bands called Super High Frequency (SHF) and Extremely High Frequency (EHF), which cover the spectrum range between 3 GHz to 30 GHz and 30 GHz to 300 GHz, respectively, which corresponds to wavelengths of one to one hundred millimeters [34] (Fig. 1.8).

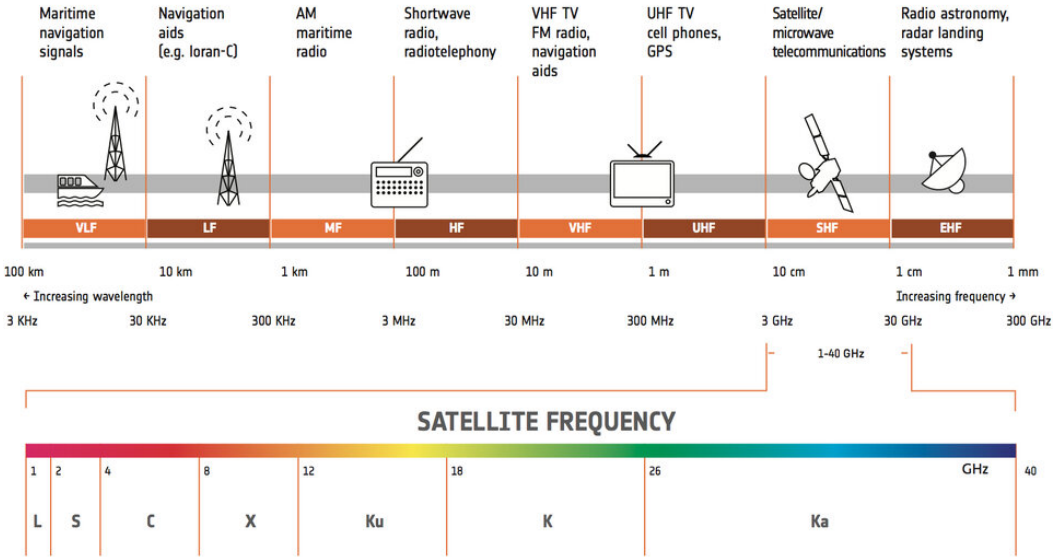


Fig. 1.8.: The electromagnetic spectrum normally used today ranges from a few KHz to 300 GHz. In the figure, the different applications for each frequency range are shown. To date, the mm-Waves spectrum is reserved only for telecommunications via satellites or in astronomical telescopes, but in the near future, it will also be used for terrestrial broadband telecommunications and more.

Historically, this RF spectrum segment has remained relatively untapped for commercial wireless applications. Indeed, in the contemporary communication landscape, traditional AM/FM broadcasting, high-definition terrestrial television, cellular networks, satellite communications, Global Positioning System (GPS), and wireless fidelity (WiFi) use the radio frequency spectrum below 3 GHz [35]. This portion of the RF spectrum is becoming densely populated, leveraging its advantageous propagation properties. Hence, the first reason for the growing interest in harnessing mmWaves spectrum is the need to employ new uncongested spectra for addressing the growing demand for wireless services [36, 37].

Together with the benefit of a less populated spectrum, mmWaves has the major advantage of hosting larger bandwidths, which results in higher data rates for communication systems. Based on Shannon's Theorem [38], the maximum data-rate of a communication channel, known as channel capacity C is related to the frequency bandwidth of the channel BW and the signal-to-noise ratio, SNR, in the following, yet simplified, manner:

$$C = BW \cdot log_2(1 + SNR) \tag{1.17}$$

Hence, the easier way for improving the communication data rate is increasing BW of the channel. In turns, for allocating more bandwidths higher carrier frequencies than the common ones should be used, thus employing frequencies higher than 3 GHz, that is in the mmWaves range.

Thus, one of the paramount advancements facilitated by millimeter waves technology is the advent of high-speed wireless access. The development of mm-Waves integrated circuits has been instrumental in the adoption of the 5G mobile communications standard, which is characterized by its expansive bandwidth capacity [34, 39, 40, 41, 42, 43]. This capability translates into elevated data transfer rates and more extensive network coverage. The implementation of the 5G standard necessitates the distribution of operational frequencies across low, mid, and high spectrum bands to optimize performance and coverage. In particular, the high-band spectrum, in the 26/28/40/66-71 GHz range [44], is designated for ultra-fast broadband services, capable of supporting peak download speeds of at least 20 Gbps and ensuring a consistent 100 Mbps user experience data rate in densely populated urban environments. Furthermore, these high-band frequencies facilitate ultra-reliable, low-latency communications with latency as low as 1 ms and are conducive to massive machine-type communications. 5G is expected to be the essential feature for creating the so-called Internet of Things (IoT), a network of physical devices, vehicles, appliances, and other physical objects that are embedded with sensors, software, and network connectivity, allowing them to collect and share data in real time, opening the doors for a potential revolution of our daily lives, industry, healthcare, and logistics [45, 46, 47, 48].

Another important advantage of millimeter-Waves technology is that it offers a distinct benefit in terms of antenna design, where the shorter radio wavelengths necessitate smaller antennas. This reduction in wavelength directly correlates with a decrease in the physical area required for antenna fabrication, allowing for more compact antenna structures. While smaller antennas inherently possess reduced effective aperture sizes, leading to lower antenna gains, this limitation can be effectively mitigated through the deployment of multi-antenna arrays. Multi-antenna arrays capitalize on the concept of "beam forming", an advanced signal processing technique that enhances the SNR of received signals, suppressing unwanted interference, and directs the focus of transmitted signals towards specific geographic locations (Fig. 1.9). The application of beam forming not only augments antenna gain but also introduces spatial diversity, bolstering the system's robustness against multi-path

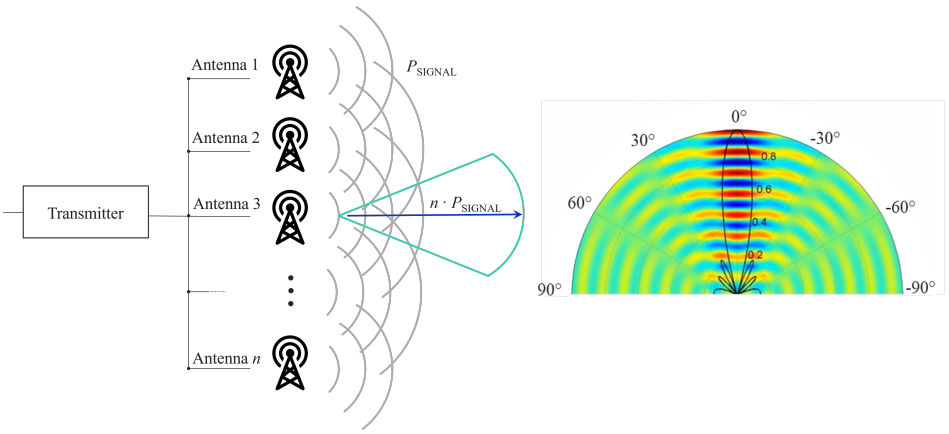


Fig. 1.9.: The concept of beam forming is schematically represented. Thanks to an array of antennas transmitting the same signal, constructive interference ensures that in a certain direction the signal itself is transmitted with much greater power than that generated by the individual antennas

fading phenomena. The principal advantage of employing a multi-antenna array architecture lies in the significant gain increase afforded by the directional antenna array pattern. This heightened gain is crucial for sustaining high data transmission rates, which are projected to reach 1-10 Gb/s, particularly within typical indoor environments. Furthermore, the use of an antenna array facilitates spatial power combining, which substantially streamlines the design complexities associated with the transmitter [49, 50].

Beam forming extends its utility beyond data communication systems, finding a pivotal role in automotive radar technology through "beam steering" (Fig. 1.10). This application is instrumental in detecting obstacles, significantly mitigating the incidence of vehicular crashes and associated fatalities. Automotive radar systems utilize a radio frequency signal, typically in the form of a time-bound pulse, which is directed towards potential targets. The reflected or scattered signals carry critical information about the target's contours, distance, and velocity, discernible through the timing and morphology of the signal returns. Importantly, the radar's resolution is inversely related to the carrier frequency, underscoring the necessity for high-frequency operation to achieve finer detail: by employing mmWaves spectrum a resolution of 5 cm can be achieved. The simultaneous scanning and processing of information to identify and track multiple objects surrounding a vehicle is a complex challenge, even for sophisticated signal processing algorithms. Consequently, the optimal strategy involves sequentially scanning different sectors around the vehicle. Mechanical steering methods are deemed unsuitable for vehicular systems due to their slow response, high costs, complications in sensor integration within automotive environments, and increased likelihood of failure stemming from mechanical wear

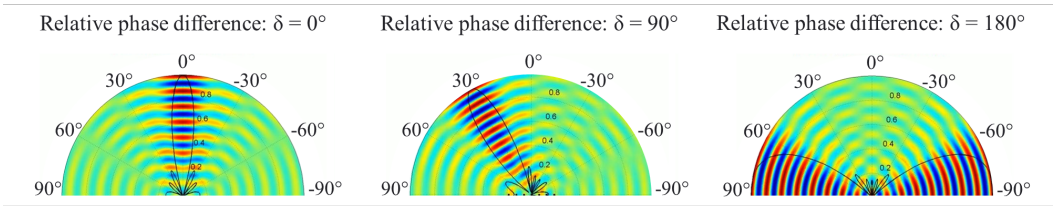


Fig. 1.10.: The concept of beam steering is schematically represented. If the phase between the signals generated by the individual antennas of an array varies, the direction in which constructive interference will occur also changes. In this way, it is possible to direct the transmitted signal towards a specific target. This approach is particularly useful in the automotive sector for detecting obstacles in front of a vehicle.

and damage. Phased array technology is a well-established method that enables electronic manipulation of the electromagnetic wavefront, achieving beam steering without moving parts. A phased array transmitter can generate a focused beam that is electronically directed to specific angles within a narrow field of view. Correspondingly, a phased array receiver is selectively responsive to reflected signals arriving from predetermined angles, which can be electronically adjusted. This capability of the phased array system minimizes the adverse effects of multipath reflections and interference, while simultaneously providing comprehensive spatial coverage [49, 51].

1.4 Technology benchmark

The aforementioned examples represent merely a fraction of the vast potential that millimeter-Waves technology holds for enhancing our daily lives.

To fully realize the potential of this technology, several critical issues must be addressed, chief among them being the semiconductor technology employed. Currently, compound semiconductors are widely used in mm-Waves technology. However, there is a pressing need to advance silicon-based technologies to facilitate broader adoption. As will be explained in this chapter, transitioning to silicon promises better system integration and a reduction in manufacturing costs, which are pivotal for the widespread implementation of mm-Waves applications.

In the forthcoming section, we will examine the existing technologies that harness mm-Waves, providing a comparative analysis of their performance benchmarks. We will then compare the different silicon technologies, including SiGe HBTs and Partially-Depleted and Fully-Depleted Silicon-On-Insulator.

1.4.1 Comparison of technologies performance

The graph presented in Fig. 1.11 provides a comparative overview of the most recent f_T/f_{MAX} values for various currently available RF technologies, highlighting the performance differences among them. The technologies examined include CMOS, bipolar, and HEMT, spanning both silicon and compound semiconductor materials.

Compound semiconductor bipolar technologies, such as InP/GaAsSb (Fig. 1.12a), occupy the high end of the f_T/f_{MAX} spectrum. These technologies leverage the high electron mobility inherent in their materials to achieve exceptionally high operating frequencies, enabling applications that exceed 1 THz [52, 53, 54]. Such capabilities are crucial for ultra-high-speed wired and wireless communication systems. However, despite their impressive performance, the industrialization of these technologies remains challenging, limiting their use in everyday devices like smartphones, computers, and antennas.

In contrast, HEMT devices based on more common compound semiconductors, such as GaN and GaAs, offer a more practical alternative. Although their performance is somewhat lower compared to compound semiconductor bipolar technologies, they still achieve significant f_T/f_{MAX} values, reaching up to 450/500 GHz [55, 56, 57]. The high electron mobility in the "2D Electron Gas" is a key factor in their performance (Fig. 1.12b), making these devices highly desirable for integration on silicon or sapphire substrates.

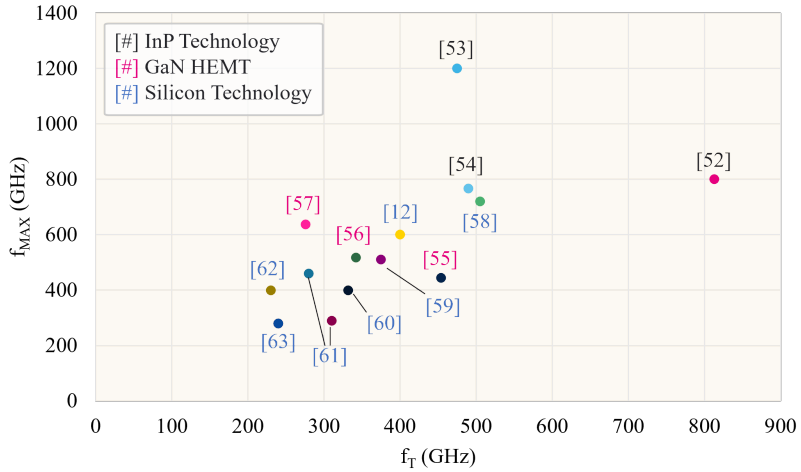


Fig. 1.11.: The benchmark in terms of f_T and f_{MAX} of the existing technologies today is reported here. As can be seen from the graph, technologies based on materials other than silicon offer high performance, particularly due to a much higher electron mobility.

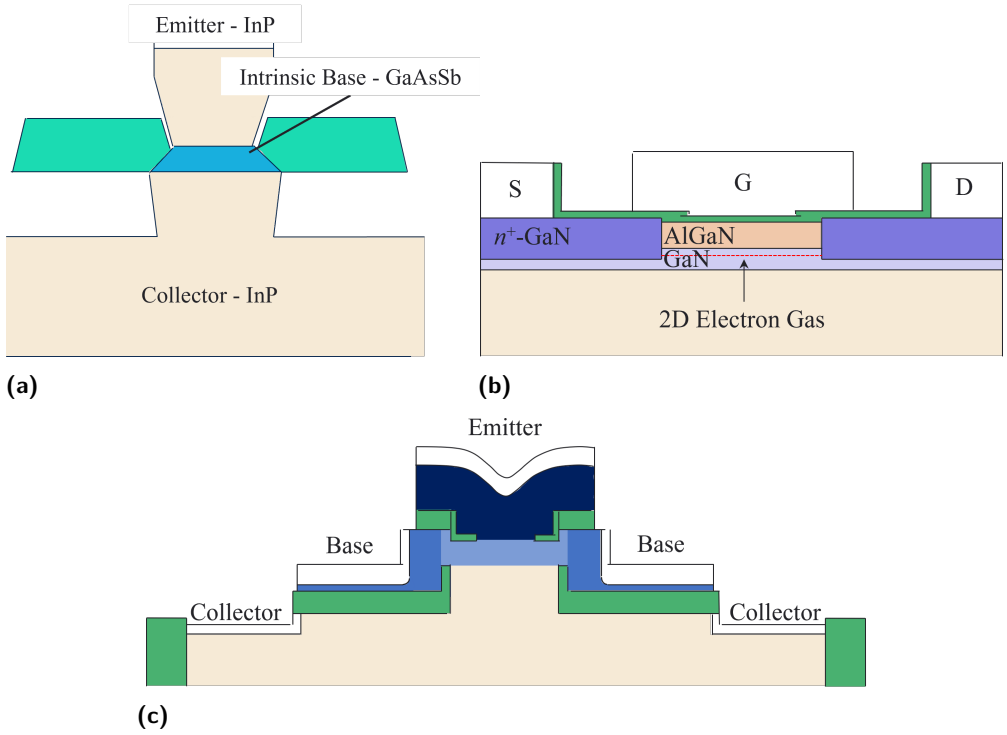


Fig. 1.12.: The figure schematically shows the structures of a) an InP-based bipolar transistor, b) a GaN-based HEMT device, and c) a SiGe HBT bipolar transistor. These technologies currently offer the highest RF performance. However, the high cost and difficult integration of GaN and HBT devices make these technologies unsuitable for cellular or PC applications, while in the case of InP, the devices built to date remain purely an experimental and research concept.

The considerable effort required to achieve high-performance metrics in compound semiconductor technologies has spurred advancements in silicon-based devices, such as heterojunction bipolar transistors (HBTs) and CMOS technologies (both bulk and SOI). Despite their relatively lower performance, silicon-based technologies remain preferred for many applications. Recent developments have led to the fabrication of silicon-based devices with competitive performance metrics. For instance, SiGe HBT devices (Fig. 1.12c) now report f_t/f_{max} values around 450 GHz, while CMOS technologies achieve values of 250/350 GHz [12, 58, 59, 60, 61, 62, 63]. Notably, a few years ago, HBTs were limited to 100 GHz, and CMOS technologies were not even considered viable for RF applications. The substantial improvements in silicon-based technology performance have been pivotal in broadening the accessibility of fast communication systems. These advancements have made high-speed communication technologies more widely available, facilitating their integration into a broader range of consumer and industrial applications.

1.4.2 Silicon Technology in mmWaves

The landscape of semiconductor technology has undergone a significant transformation in the past few decades, with CMOS and SiGe BiCMOS transistors achieving new heights in frequency capabilities. This advancement has paved the way for sophisticated integrated circuits that cater to the upper echelons of the microwave and millimeter-Waves spectrum. Silicon-based digital circuits, including those for signal processing and data conversion, have seen dramatic improvements, bolstering the case for increased research funding and technological development.

Initial millimeter-Waves integrated circuits (MMW ICs) emerged in the late 1970s and early 1980s [64, 65]. At that time, compound semiconductors like Gallium Arsenide (GaAs) and Indium Phosphide (InP) were favored for their high-performance characteristics. GaAs was particularly notable for its high electron mobility, allowing transistors to function at frequencies above 250 GHz, and its wide bandgap, which made it less sensitive to temperature compared to silicon transistors [66]. Additionally, GaAs devices typically exhibited lower noise at high frequencies due to reduced parasitic effects. Despite these advantages, GaAs-based transistors did not meet all performance criteria for certain uses, prompting the exploration of other materials like InP and Gallium Nitride (GaN). InP is known for even higher electron mobility than GaAs and Si, making it ideal for high-power, high-frequency MMICs. GaN is sought after for high-voltage and high-efficiency applications [67, 68].

Post-2000, silicon-based technologies began to outpace III-V-based technologies for some uses, thanks to significant advancements and rapid progress. Silicon technology was seen as promising, with the potential to match or surpass the performance of III-V-based technologies swiftly. Furthermore, silicon technology boasts superior integration capabilities compared to compound semiconductor technologies.

Silicon now demonstrates compelling performance for frequencies in the mm-Waves range, and while it may not yet match compound semiconductors in power amplification, its proficiency has led to significant integration of RF and digital components within the same CMOS processes. This has been a game-changer in wireless communications, enabling the creation of sophisticated and efficient System On Chips (SoCs).

SoCs have revolutionized wireless system design by consolidating multiple functions onto a single chip (Fig. 1.13), enhancing system performance, and expanding the possibilities for wireless communication and signal processing. When contrasted with traditional multi-chip-module (MCM) approaches, SoCs offer reduced costs, lower complexity, and decreased power consumption. Moreover, SoCs provide robustness

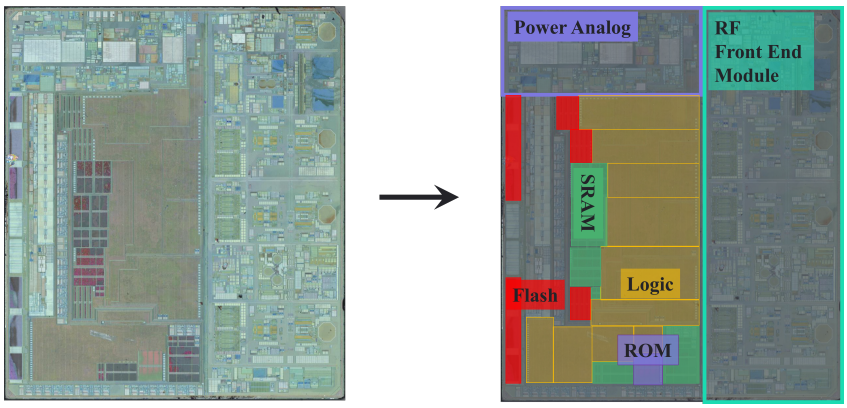


Fig. 1.13.: The figure shows an example of a System on Chip highlighting the portions dedicated to different operations [70]. As you can see, RF, power, and digital circuits are integrated into the same chip, greatly increasing the system's final performance.

through on-chip calibration and built-in self-test, which are particularly beneficial in demanding environments and applications [66, 69].

The ability to integrate analog, mixed-signal, and digital components on a single silicon die or package presents a significant advantage for high-performance mm-Waves systems. The burgeoning potential to integrate a higher density of RF components in CMOS suggests a path to substantially lower system costs. While III-V transistors may offer cost benefits at relaxed lithography dimensions, especially for RF-centric devices, CMOS demonstrates a clear advantage when integrating even modest amounts of digital logic, outperforming compound semiconductor solutions [49, 71].

RF CMOS vs BiCMOS

Cellular networks are fundamentally structured into two primary sectors: the infrastructure, which orchestrates the connectivity backbone, and the user terminal, which interfaces with the end-users (Fig. 1.14). These sectors are inherently distinct, each presenting unique technological requirements and challenges.

The infrastructure is a composite of radio access and backhauling networks, predominantly reliant on wireless links, while the core network is sustained by optical links. Integral to this infrastructure are subsystems such as RF and mm-Waves Front-End Modules, which are incorporated into active phased array and massive MIMO antennas, multiband point-to-point radios, and high-speed optical modules. The capacity of these wireless links is contingent upon system gain and propagation conditions, dictating stringent specifications for antenna gains, transmitter output power, and

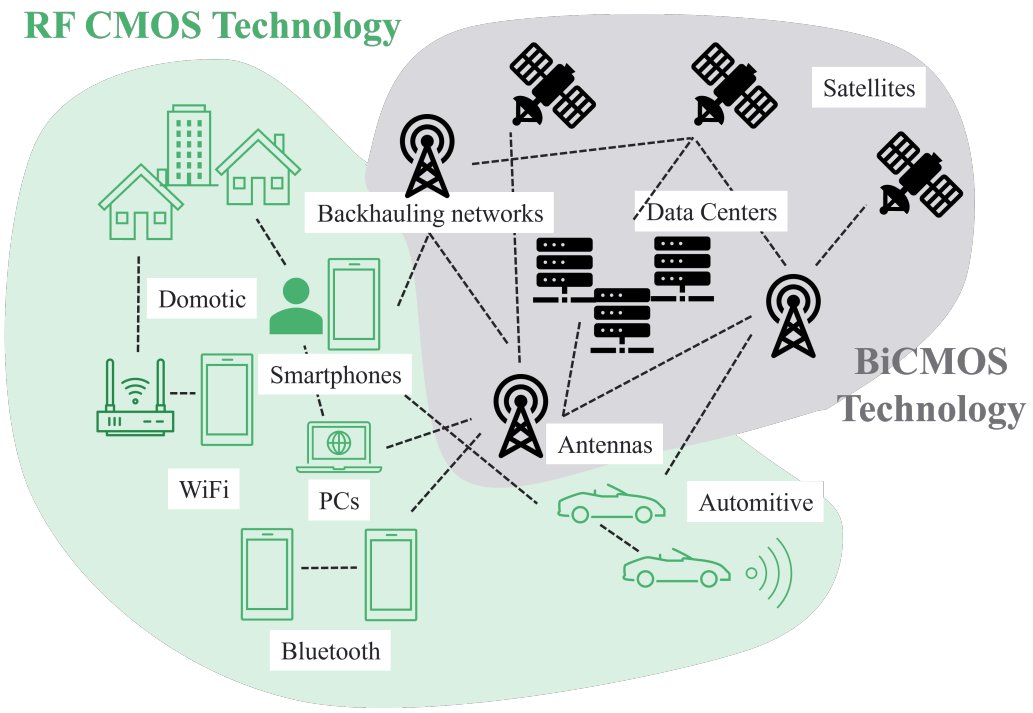


Fig. 1.14.: The various applications for RF CMOS and BiCMOS devices are reported. As can be seen, RF CMOS technology is more relevant for mobile and user-friendly devices, while BiCMOS technology is generally used more for applications in antennas, data centers, and satellites.

receiver noise figures. BiCMOS technology, particularly Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs), is identified as the optimal choice for infrastructure applications. This technology synergizes the strengths of CMOS logic, high-performance SiGe HBTs, and RF passives, creating a robust solution for high power handling and efficiency. SiGe HBTs exhibit high breakdown voltages, essential for operations requiring significant power handling. While power amplifiers in both SiGe and CMOS technologies demonstrate comparable performance, SiGe has a slight edge in terms of power saturation, especially in the 20-40 GHz range. Additionally, SiGe Power Amplifiers (PAs) marginally outperform CMOS-SOI PAs in terms of average efficiency, and SiGe Low Noise Amplifiers (LNAs) can achieve superior gain across a broad frequency spectrum [72, 73, 71, 49].

The user terminal segment faces the challenge of accommodating an expanding array of frequency bands within the constrained footprint of smartphone Front-End Modules (FEMs). The selection of silicon technology for these FEMs is critical and is influenced by the frequency spectrum required for the connectivity standard in question. Currently, CMOS technology, enhanced by RF Silicon-On-Insulator (SOI) evolution, is the preferred choice for user terminals. This technology facilitates the

development of cost-effective, high-performance LNAs and switches, with a vast array of devices available for creating highly integrated systems at minimal cost. The role of CMOS technology in mm-Waves applications has evolved significantly since its initial consideration for RF applications in the early 1990s. The new millennium brought forth aggressive dimensional scaling, which led to higher unity current-gain cut-off frequencies and maximum oscillation frequencies. Over the past decade and a half, Silicon-on-Insulator (SOI) has replaced standard bulk CMOS technology, guaranteeing performance improvements such as reduced leakage currents and capacitive parasites, while maintaining compatibility with existing development and production lines [74, 75]. RF-SOI has garnered substantial research attention due to its application in large volume markets requiring cost-effective single-chip transceivers. The first SOI modules for RF applications, notably integrated switches, achieved market dominance for handsets by 2012. The success of these modules is attributed to the substrate's RF performance, which offers low insertion loss, high isolation, and excellent linearity at a low cost. The discovery of parasitic surface conduction (PSC) beneath the buried oxide (BOx) and the subsequent introduction of a polysilicon trap-rich layer have significantly reduced signal distortion and improved linearity [76]. Advancements in SOI technology have led to the development of 45 nm PD-SOI nodes and sub-30 nm FD-SOI nodes, with cutoff and oscillation frequencies in the 300-400 GHz range. These nodes have enabled the integration of key RF circuit elements, including LNAs and PAs, and the commercial availability of high-performance CMOS RF functions. Despite lower carrier mobility compared to III-V materials, silicon MOSFETs have become competitive in high-frequency applications through the application of strain to enhance mobility [76]. Partially Depleted (PD) SOI transistors with a channel length of 90 or 130 nm, combined with a High-Resistivity (HR) trap-rich SOI substrate, have become the mainstream technology for RF ICs. The advent of 5G and subsequent generations of mobile communication systems necessitates higher cut-off frequencies, improved linearity, and reduced power consumption, all of which are addressed by these advanced SOI technologies.

FD vs PD SOI

In the realm of SOI device fabrication, the process typically commences with a silicon wafer, which is layered with a buried oxide (BOx). Atop this structure, one can engineer two varieties of transistors: fully depleted (FD) and partially depleted (PD) variants, differentiated by the silicon layer's thickness above the BOx (Fig. 1.15) [77]. The Shallow Trench Isolation (STI), in conjunction with the BOx, forms

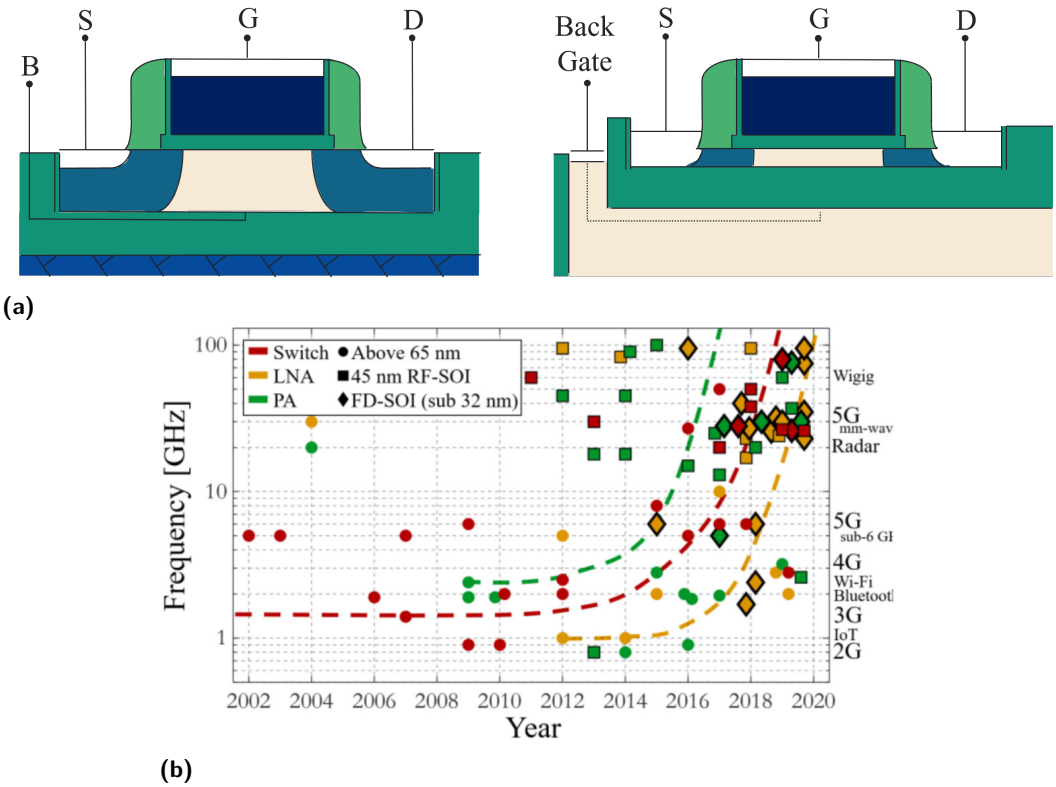


Fig. 1.15.: a)A PDSOI and FDSOI device are schematically represented in the figure. The main difference between the two devices is the thickness of the SOI: for the PDSOI it is a few tens of nanometers, while for the FDSOI it is a few nanometers. Additionally, for the PDSOI, a Trap Rich layer is present below the BOx to reduce parasitic currents and improve RF linearity. On the other hand, the FDSOI has a back gate that increases the electrostatic control of the channel and thus the static performance (subthreshold, leakage, transconductance...). b) The performance trends of the two devices for various RF applications are compared in the graph [76].

an isolated well for Field-Effect Transistors (FETs), which is crucial for minimizing capacitive effects in millimeter-wave operations.

In PDSOI technology, the layer of silicon on insulator is thicker than the channel's depletion region, allowing for the formation of a body contact to manage voltage and facilitate charge removal. FDSOI devices share similarities with PDSOI but are distinguished by a thinner silicon layer, which results in the full depletion of the body's mobile charges, thus heightening the importance of threshold voltage management.

PDSOI emerged as the initial technology due to the relative ease of producing thicker high-quality silicon layers. It offered significant benefits over traditional bulk CMOS by using both BOx and STI to achieve complete device isolation from the substrate,

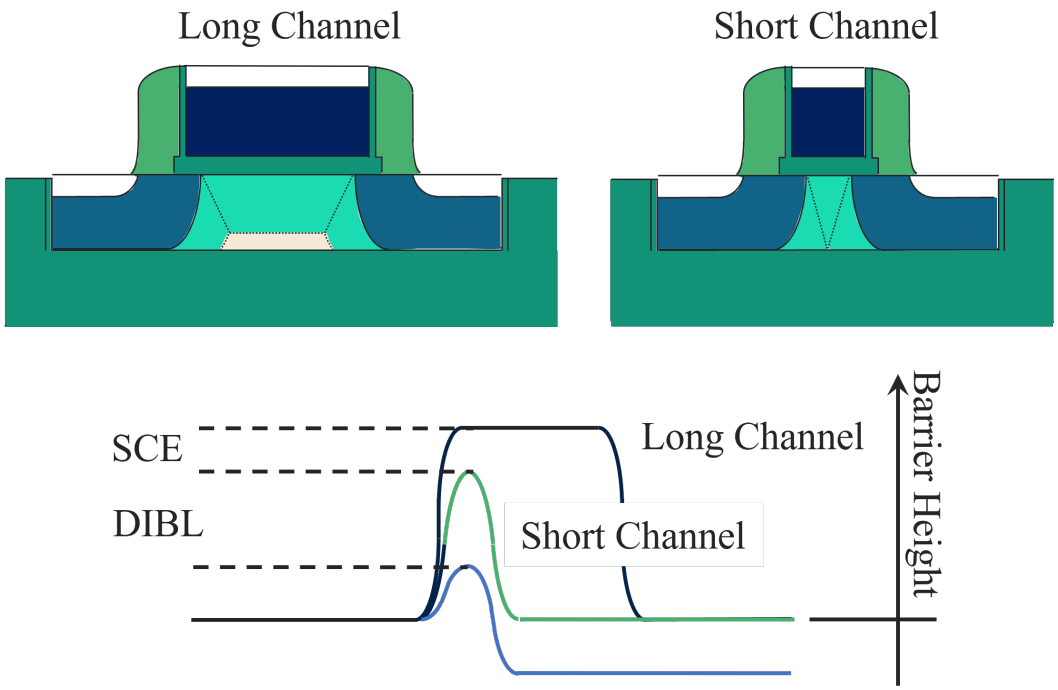


Fig. 1.16.: The Short-Channel Effect (SCE) and the Drain-Induced Barrier Lowering (DIBL) are represented here. In the case of bulk or PDSOI transistors, where the silicon is not completely depleted, the reduction of the channel length leads to less electrostatic control by the gate. This is because, for short channels, the drain and source junctions contribute more to the depletion of the channel rather than the gate. This generates a lowering of the barrier potential between the two junctions, reducing the threshold voltage and increasing the leakage between the two contacts. Additionally, when a positive voltage is applied to the drain, its depletion region is further extended, amplifying this effect (DIBL).

substantially reducing parasitic capacitances. However, PDSOI is not without its drawbacks, such as the "Short-channel effect", which arises when the gate length is reduced, diminishing the gate's control over the depletion zone and thereby lowering the threshold voltage (Fig. 1.16) [77, 78].

Another issue is Drain-Induced Barrier Lowering (DIBL), a phenomenon where the threshold voltage (V_{th}) decreases due to charge sharing between the gate and the drain junctions. Additionally, SOI MOSFETs in a floating-body state can exhibit the "kink effect," a distinctive anomaly in the output characteristics of n-channel transistors caused by impact ionization near the drain at high voltages [79].

These challenges have rendered PDSOI less suitable for analog applications, paving the way for FDSOI to claim a stake in the market. FDSOI devices, with their constant state of full depletion, are nearly immune to short-channel effects and DIBL. The reduced electric field near the drain also curtails electron-hole pair

generation, thus avoiding the kink effect. Despite FDSOI's higher transconductance and frequency performance parameters, PDSOI remains the preferred choice for millimeter-Waves applications. FDSOI's thinner silicon layer can lead to self-heating, RF performance degradation, and lower breakdown voltages, which are not ideal for power amplifiers and RF switches. PDSOI's Trap Rich Polysilicon layer beneath the BOx enhances device linearity by mitigating Parasitic Surface Conduction (PSC) [76]. Integration challenges between advanced FDSOI nodes and trap-rich substrates arise due to the complexity of defining back-gate contacts beneath the BOx. Current FDSOI-based Integrated Circuits (ICs) start with an SOI substrate featuring a standard resistivity handle. At high frequencies, thin dielectric layers become capacitive, allowing device fields to penetrate the substrate, causing losses and affecting parasitic couplings. Despite ongoing research to address these issues, PDSOI remains advantageous for its linearity benefits. Presently, the market offers 300 mm-diameter SOI trap-rich wafers for cutting-edge PDSOI nodes, integral to the Front-End Modules of contemporary smartphones. Consequently, enhancing PDSOI performance remains a pertinent objective.

1.4.3 ST PDSOI technology: CMOS65SOIMMW

One of the first PDSOI technology by ST was the so called CMOS65SOIFEM, which provided devices for several applications with gate length as short as 60 nm. In order to address the demand for a more cutting-edge technology, ST developed from a mature 40-nm bulk FEOL technology its CMOS65SOIMMW, reaching 40-nm devices fabricated on a 300-mm Trap-Rich SOI substrate (75 nm SOI / 200 nm BOx). This technology offers the possibility to implement RF switches, Low Noise Amplifiers, Power Amplifiers, and digital components in the same chip, thus providing an extremely complete and competitive platform on the market (Tab. 1.1).

For LNAs and PAs, NMOS and PMOS transistors are fabricated with a thin gate oxide (13 Å EOT, "GO1") with both low and standard V_{th} options, whereas devices with thick oxide (50 Å EOT, "GO2") are provided for RF switches and IO designs (Fig. 1.17). Boosters of electron mobility like high tensile Contact Etch Stop Layer (CESL) and Stress Memorization Technique (SMT) [80] are also employed. Pocket implantations are performed in GO1 transistors for limiting Short Channel Effects. Regarding contact and BEOL, it is based for cost aspect reason on 65-nm design rules. 5 or 7 copper Metal Layers (ML) with respectively 1 or 2 thick copper levels are proposed. Finally, both Body Contact and Floating Body devices are fabricated (Fig. 1.18).

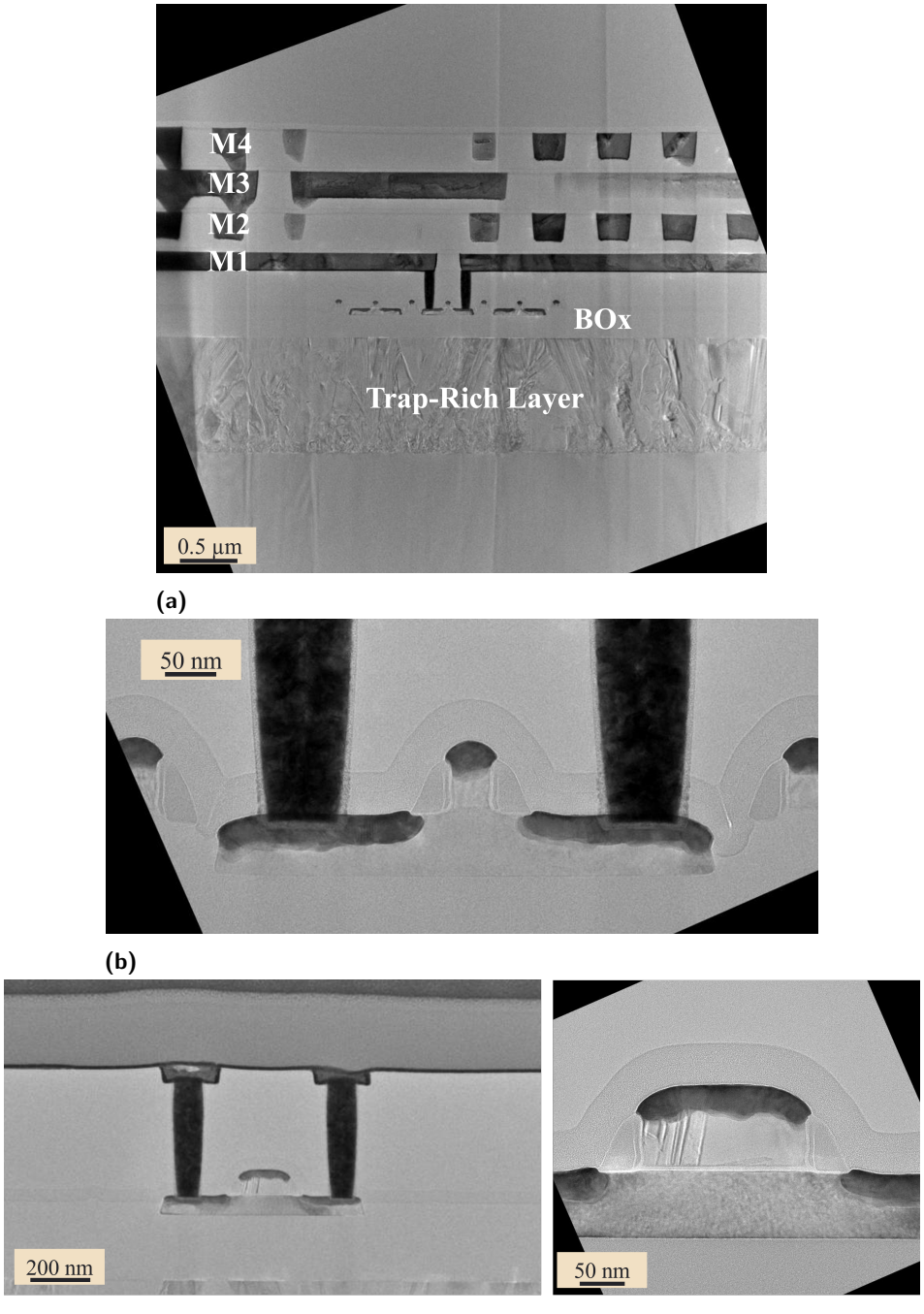


Fig. 1.17.: The reported TEM images show some characteristics of the CMOS65SOIMMW technology. In a), the presence of the Trap-Rich layer below the BOx is highlighted, which eliminates the generation of parasitic currents and thus increases the linearity of the devices. In b) and c) a GO1 and GO2 device used in LNA circuits and RF switches, respectively, are reported. For GO1, the minimum size of this type of device is 40 nm, while for the GO2 RF switch it is 0.1 µm.

Tab. 1.1.: The table lists the devices offered by the CMOS65SOIMMW technology. Among the various points on the list, it is noted that the transistors with LNA applications are of type GO1, thus with a gate oxide of 13 Å EOT, while the transistors for switch and PA are of type GO2, with a thicker oxide reaching 50 Å EOT

Technology device offer	
1V GO1 transistors	• Floating Body / Body Contacted NMOS (LVT/SVT) • Floating Body PMOS
2.5V GO2 transistors	• NMOS and PMOS Body contacted • RF Switch Body Contacted
Diodes	Gated and non-gated for ESD
Resistors	Silicided and non silicided Poly
Capacitors	• OTP based on GO1 • RF MOM • Poly/Well GO2
Inductors	Single-ended and differential for 5 and 7 ML
Transmission lines	CPW for 5 and 7 ML

At the start of this thesis, NMOS GO1 with voltage gain above 8 and 15 for transistor length of 40 and 60 nm were demonstrated, with f_T/f_{MAX} of 250/350 GHz for transistor length of 40 nm. Regarding RF switches performance, devices with $R_{ON}C_{OFF}$ of 79 fs and 85 fs can be provided at $L_G = 0.1$ µm and 0.12 µm and Poly-Pitch of 0.92 µm, respectively, with RFV_{max} values of 2.4 V and 3.2 V [9, 12].

The CMOS65SOIMMW technology demonstrates performance metrics that enable it to compete effectively with other semiconductor technologies currently available on the market and utilized in contemporary devices. Specifically, this includes 65-nm technologies from leading manufacturers such as GlobalFoundries, TSMC, UMC, and TowerJazz. The comparative capabilities in terms of f_t/f_{max} and $R_{ON}C_{OFF}/RFV_{max}$ for transistor devices from these manufacturers are illustrated in Fig. 1.19.

As reported in Fig. 1.19a, STMicroelectronics, GlobalFoundries [81, 62], and UMC [82] report comparable performance levels for Low Noise Amplifier (LNA) devices, with f_T/f_{MAX} values approximately in the range of 250/350 GHz. This consistency highlights the competitive nature of these technologies in high-frequency applications.

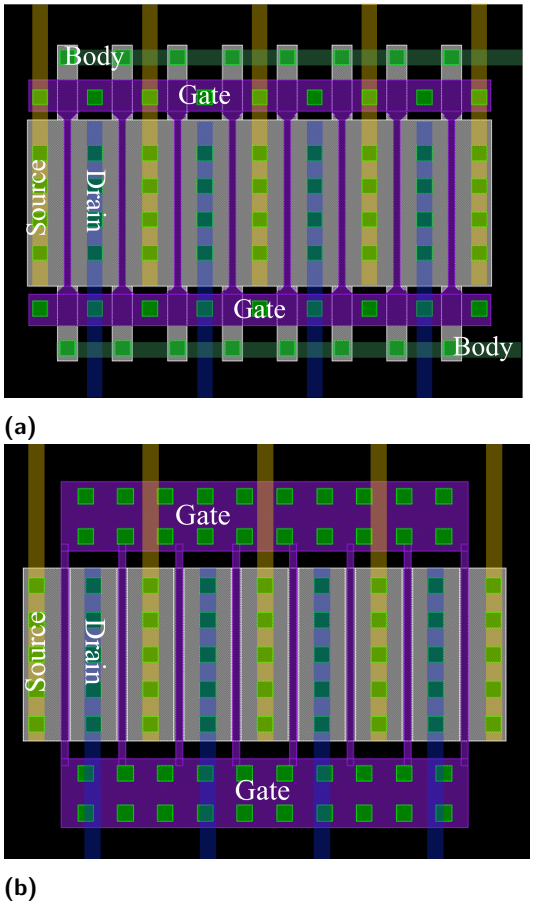
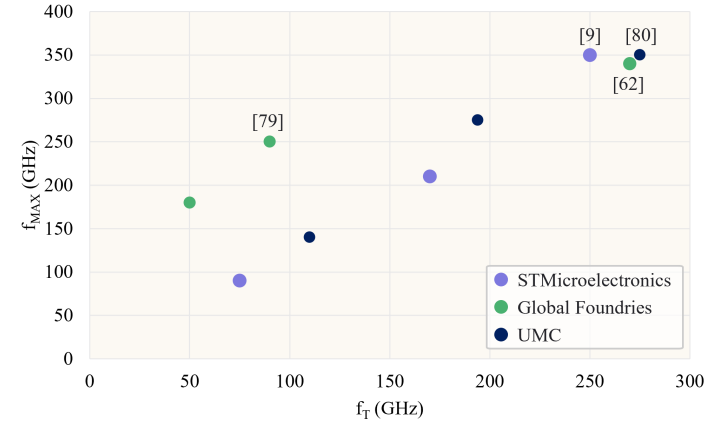
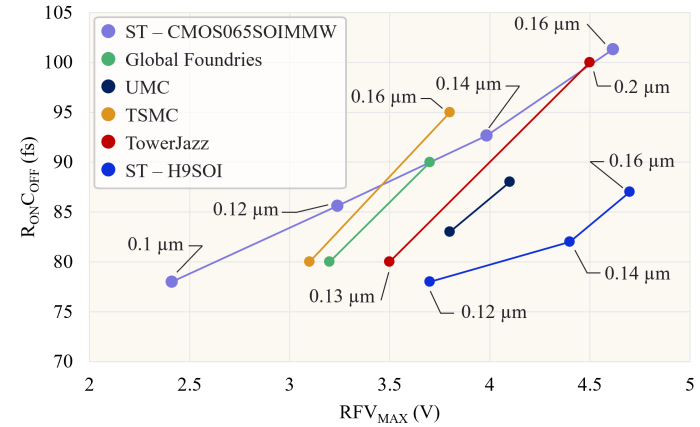


Fig. 1.18.: In figure, a) Body Contact (BC) and b) Floating Body (FB) configurations of the CMOS65SOIMMW RF structure are reported. The main difference between the two types of configuration is the presence of a body contact in the BC device. This contact allows for the control of the body potential and thus the extraction of charges that can be generated by impact of hot carriers. However, this contact has the drawback of generating an additional parasitic capacitive contribution with the gate, which limits the device's performance, as reported in Fig. 1.4.

The landscape for RF switch devices is more varied, as reported in Fig. 1.19b [81, 83, 84, 82]. The power handling capabilities of these devices can result in the provision of transistors with different channel lengths, tailored to meet specific customer requirements. This variability underscores the importance of flexibility in design and application-specific optimization. The current state-of-the-art for RF switch applications is represented by another technology from STMicroelectronics, known as H9SOI. Unlike CMOS65SOIMMW, H9SOI integrates only switch devices on 200-mm wafers. This technology achieves impressive $R_{\mathrm{ON}}C_{\mathrm{OFF}}/RFV_{\mathrm{max}}$ values of 78 fs / 3.7 V for devices with a gate length (L_{G}) of 0.12 µm [85]. These metrics underscore H9SOI's advanced capabilities and its suitability for high-performance RF switch applications.



(a)



(b)

Fig. 1.19.: The performances of CMOS65SOIMMW transistors for a) LNA and b) RF switch are compared with those published by other semiconductor companies. It is immediately noticeable that there is less competition for LNA devices, while for switch applications the market offers a wide range of choices in terms of performance and size. In both cases, the CMOS65SOIMMW technology proves to be highly competitive with the others.

Hence, the CMOS65SOIMMW technology stands as a robust competitor in the semiconductor market, particularly when benchmarked against other 65-nm technologies. Its performance metrics in both LNA and RF switch applications highlight its potential for integration into advanced communication systems.

1.4.4 Thesis objectives and organization

To maintain competitive performance in both types of applications, continuous development is essential. As discussed in previous chapters, RF figures of merit are closely linked to the characteristics of the devices. Specifically, f_T and R_{ON} are

directly influenced by transconductance and, consequently, the electron mobility of the devices. In contrast, f_{MAX} and C_{OFF} are, among other devices' properties, affected by parasitic characteristics such as C_{GD} and C_{GS} capacitances.

This thesis focuses on optimizing both electron mobility and parasitic capacitances through modifications to the SOI substrate. Three distinct projects were undertaken, which, while initially independent, have the potential to be integrated into a cohesive solution. These projects are named ThinSOI, Strained SOI, and Channel Orientation.

The ThinSOI project (cf. Chapter 2) investigates the impact of reducing the SOI layer thickness, which is typically 75 nm in standard devices. The objective is to explore how a thinner SOI layer affects the parasitic capacitances associated with the substrate, with the expectation of improving performance, particularly for RF switch devices.

The Strained SOI and Channel Orientation projects (cf. Chapter 3 and Chapter 4, respectively) delve into the field of "strain engineering", which examines the relationships between mechanical stress in a semiconductor material and the resulting deformation of its band structure, thereby altering its electrical properties. Introducing tensile stress within the silicon crystal structure can increase electron mobility by reducing intervalley scattering and/or modifying the effective mobility of the electrons. The theoretical foundations of strain engineering are detailed in the dedicated appendix (cf. Chapter B). The Strained SOI project developed a novel stressor method capable of introducing significant stress within the silicon channel, far more effectively than current "local" and "global" stressor techniques. This method involves forming a stress-inducing layer within the SOI, beneath the transistor device. The Channel Orientation project investigates how electron mobility (and thus device performance) varies along different crystalline directions, specifically <100> and <110> orientations.

The subsequent chapters present and discuss the results obtained from these three projects. Each project employed a comprehensive approach to semiconductor technology development, encompassing:

- Experimental Design: modifying the fabrication process to explore different parameters.
- Computational Modeling: utilizing computational tools to provide theoretical support for observed changes and to predict further improvements.

- Device Characterization: conducting both physical and electrical characterization to obtain empirical data on the structural and performance impacts.

While this manuscript may not offer the whimsical reading experience of "Alice in Wonderland," I hope it serves as a White Rabbit, leading to new discoveries or deeper insights into RF SOI technology.

References

[1] A. Gupta et al. “A Survey of 5G Network: Architecture and emerging technologies”. In: *IEEE Access* 3 (2015), pp. 1206–1232.

[2] M. Giordano et al. “A Tutorial on Beam Management for 3GPP NR at mmWave Frequency”. In: *IEEE Comunications Surveys and Tutorials* 21 (2019), pp. 173–196.

[3] T.S. Rappaport et al. “Milllimter Wave communications for 5G cellular: It will work!” In: *IEEE Access* 1 (2013), pp. 335–349.

[4] S. Voinigescu. *High-Frequency Integrated Circuits*. Cambridge University Press, 2013.

[5] P. Eloranta et al. “A multimode transmitter in 0.13 µm CMOS using direct-digital RF modulator”. In: *IEEE JSSC* 42 (2007), pp. 2774–2784.

[6] F.M. Colebrooke. “Homodyne”. In: *Wireless World and Radio Review* 13 (1924), pp. 645–648.

[7] P.D.L. Beasley et al. “Solving the problems of a single antenna frequency modulated CW radar”. In: *Proc. IEEE Radar Conference* (1990), pp. 91–395.

[8] H.T. Friis. “Noise Figures of Radio Receivers”. In: *IEEE RFIC Virtual Journal* 32 (1944), pp. 419–422.

[9] S. Crémer et al. “40-nm RFSOI technology exhibiting 90fs $R_{ON}C_{OFF}$ and f_T/f_{MAX} of 250 GHz/350 GHz targeting sub-6 GHz and mmW 5G applications”. In: *IEEE 53rd European Solid-State Device Research Conference (ESSDERC)* (2023).

[10] J. Singh et al. “14-nm FinFET Technology for Analog and RF Applications”. In: *IEEE Transactions On Electron Devices* (2018), pp. 31–37.

[11] M. Micovic et al. “High Frequency GaN HEMTs for RF MMIC Applications”. In: *2016 IEEE International Electron Devices Meeting (IEDM)* (2016), pp. 3.3.1–3.3.4.

[12] P. Chevalier et al. “PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications”. In: *2020 IEEE International Electron Devices Meeting (IEDM)* (2020), pp. 34.4.1–34.4.4.

[13] C.R. Bolognesi et al. “III-V GaAs and INP HBT devices for 4G and 5G wireless applications”. In: *2018 China Semiconductor Technology International Conference (CSTIC)* (2018), pp. 1–4.

[14] S. Makioka et al. “Super Self-Aligned GaAs RF Switch IC with 0.25 dB Extremely Low Insertion Loss for Mobile Communication Systems”. In: *IEEE Trans. Electron Devices* 48 (2001), pp. 1510–1514.

[15] D. Kelly et al. “The State-of-the-Art of Silicon-on-Sapphire CMOS RF Switches”. In: *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)* (2005).

[16] F. Gianesello et al. “Advanced 200-mm RF SOI Technology exhibiting 78 fs $R_{ON}C_{OFF}$ and 3.7 V breakdown voltage targeting sub 6 GHz 5G FEM”. In: *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)* (2022), pp. 191–194.

[17] F. Gustrau. *RF and Microwave Engineering: Fundamentals of Wireless Communications*. J. Wiley and Sons, 2012.

[18] B. Martineau. “65nm CMOSSOI potentialities for millimeterwave wireless applications”. PhD thesis. Université des sciences et technologies de Lille, 2008.

[19] N. Woldhoff. “Caractérisations et modélisations des technologies CMOS et BiCMOS de dernières générations jusque 220 GHz”. PhD thesis. Université des sciences et technologies de Lille, 2009.

[20] G. Dambrine. “What are the limiting parameters of deep-submicron MOSFETs for high frequency applications?” In: *Electron Device Letters, IEEE* (2003), pp. 189–191.

[21] R. Valentin. “Influence of gate offset spacer width on SOI MOSFETs HF properties”. In: *Silicon Monolithic Integrated Circuits in RF Systems* (2006), pp. 18–20.

[22] S. J. Mason. “Power Gain in Feedback Amplifiers”. In: *Res. Lab. of Electronics, Mass. Inst. Tech., Cambridge, Mass., Tech. Rept. No. 257* (1953).

[23] S. J. Mason. “Power Gain in Feedback Amplifiers”. In: *J. Appl. Physics* (1956), pp. 1025–1027.

[24] T. Parenty. “Etude et perspective des transistors à hétérostructures AlInAs/-GaInAs de lonfeur de frille inéfriere à 100 nm et conception de circuits integers en bande G”. PhD thesis. Université des sciences et technologies de Lille, 2003.

[25] G. Hiblot et al. “Refined conformal mapping model for MOSFET parasitic capacitances based on elliptic integrals”. In: *IEEE Transactions on Electron Devices* (2015), pp. 972–979.

[26] O. Oezdamar et al. “Linearity Trade-offs in High-Voltage RF Switches for Antenna Tuning Applications”. In: *2020 IEEE Asia-Pacific Microwave Conference* (2020), pp. 896–898.

[27] O. Oezdamar et al. “Linearity Analysis of High-Voltage RF Switches for Antenna Tuning Applications”. In: *IEEE Transactions on Microwave Theory and Techniques* (2022), pp. 14–23.

[28] C. Li et al. “5G mm-Wave Front-End-Module Design with Advanced SOI Process”. In: *2017 IEEE 12th International Conference on ASIC* (2017), pp. 1017–1020.

[29] M. Jaffe et al. “Improvements in SOI Technology for RF Switches”. In: *2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2015), pp. 30–32.

[30] A. Rathi et al. “Large Signal RF Reliability of 45-nm RFSOI Power Amplifier Cell for Wi-Fi6 Applications”. In: *2021 IEEE International Reliability Physics Symposium* (2021), pp. 1–6.

[31] F. Gianesello et al. “Highly linear and sub 120 fs Ron x Coff 130 nm RF SOI Technology Targeting 5G Carrier Aggregation RF Switches and FEM SOC”. In: *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2016), pp. 9–12.

[32] A. Léon et al. “RF Power-Handling Performance for Direct Actuation of Germanium Telluride Switches”. In: *RF Power-Handling Performance for Direct Actuation of Germanium Telluride Switches* (2020), pp. 60–73.

[33] N. El-Hinnawy et al. “Switch Stacking for OFF-State Power Handling Improvements in PCM RF Switches”. In: *2021 IEEE MTT-S International Microwave Symposium* (2021), pp. 60–73.

[34] F. Khan et al. “mmWave mobile broadband (MMB): Unleashing the 3–300GHz spectrum”. In: *34th IEEE Sarnoff Symposium* (2011), pp. 1–6.

[35] FCC Online Table Of Frequency Allocations. “https://transition.fcc.gov/oet/spectrum/table/fcctable.pdf”. In: (2022).

[36] Cisco. “Cisco Annual Internet Report (2018–2023) White Paper”. In: (2020).

[37] Ericsson. “Ericsson Mobility Report”. In: *Business Review 2024* (2024).

[38] C.E. Shannon. “A Mathematical Theory of Communication”. In: *The Bell System Technical Journal* 27 (1948), 379–423 623–656.

[39] M. Cheffena. “Industrial wireless communications over the millimeter wave spectrum: opportunities and challenges”. In: *IEEE Communications Magazine* 54 (2016), pp. 66–72.

[40] S. Rangan et al. “Millimeter-wave cellular wireless networks: potentials and challenges”. In: *Proceedings of the IEEE* 102 (2014), pp. 366–385.

[41] Z. Pi et al. “An introduction to millimeter-wave mobile broadband systems”. In: *IEEE Communications Magazine* 49 (2011), pp. 101–107.

[42] D. Bojic et al. “Advanced wireless and optical technologies for small-cell mobile backhaul with dynamic software-defined management”. In: *IEEE Communication Magazine* 51 (2013), pp. 86–93.

[43] R. Taori et al. “Point-to-multipoint in-band mm-wave backhaul for 5G networks”. In: *IEEE Communication Magazine* 53 (2015), pp. 195–201.

[44] GSMA. “5G Spectrum, GSMA Public Policy Position”. In: (2021).

[45] YOLE. “5G mMTC and IoT Platforms – Technology and Market Trends 2021”. In: (2021).

[46] S.K. Rao et al. *Impact of 5G Technologies on Industry 4.0*. 2018, pp. 145–159.

[47] K.E. Georgiou et al. “5G Use in Healthcare: The Future is Present”. In: *Journal of the Society of Laparoscopic and Robotic Surgeons* 25 (2021).

[48] M.A.I. Mozumder. “Overview: Technology Roadmap of the Future Trend of Metaverse based on IoT, Blockchain, AI Technique, and Medical Domain Metaverse Activity”. In: *24th International Conference on Advanced Communication Technology (ICACT)* (2022), pp. 256–261.

[49] A.M. Niknejad et al. *Introduction to mm-Wave Silicon Devices, Circuits, and Systems*. Springer, 2008.

[50] B.D. Van Veen et al. “Beamforming: A Versatile Approach to Spatial Filtering”. In: *IEEE ASSP Magazine* 5 (1988), pp. 4–24.

[51] R. Sun et al. “A millimeter-wave automotive radar with high angular resolution for identification of closely spaced on-road obstacles”. In: *Scientific Reports* (2023).

[52] Y. Shiratori et al. “Ultra-high Speed InP/GaAsSb-based Type-II Double-heterojunction Bipolar Transistors and Transfer Technology onto SiC Substrate”. In: *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)* (2020), pp. 1–4.

[53] A. M. Arabhavi et al. “InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With fMAX = 1.2 THz”. In: *IEEE Transactions on Electron Devices* (2022), pp. 2122–2129.

[54] D. C. Ruiz et al. “New GaInAs/InAs/InP Composite Channels for mm-Wave Low-Noise InP HEMTs”. In: *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium* (2019), pp. 1–4.

[55] Y. Tang et al. “Ultrahigh-Speed GaN High-Electron-Mobility Transistors With fT/fmax of 454/444 GHz”. In: *IEEE Electron Device Letters* (2015), pp. 549–551.

[56] K. Shinohara et al. “Self-aligned-gate GaN-HEMTs with heavily-doped n+-GaN ohmic contacts to 2DEG”. In: *2012 International Electron Devices Meeting* (2012), pp. 27.2.1–27.2.4.

[57] D. Han et al. “Low-Noise Microwave Performance of 30 nm GaInAs MOS-HEMTs: Comparison to Low-Noise HEMTs”. In: *IEEE Electron Device Letters* (2020), pp. 1320–1323.

[58] B. Heinemann et al. “SiGe HBT technology with fT/fmax of 300GHz/500GHz and 2.0 ps CML gate delay”. In: *2010 International Electron Devices Meeting* (2010), pp. 30.5.1–30.5.4.

[59] J. Pekarik et al. “SiGe HBTs with fT/fMAX = 375/510GHz Integrated in 45nm PDSOI CMOS”. In: *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium* (2021), pp. 1–4.

[60] O. M. Kane et al. “22nm Ultra-Thin Body and Buried Oxide FDSOI RF Noise Performance”. In: *2019 IEEE Radio Frequency Integrated Circuits Symposium* (2019), pp. 35–38.

[61] S. Callender et al. “FinFET for mm Wave - Technology and Circuit Design Challenges”. In: *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium* (2018), pp. 168–173.

[62] S. H. Jain et al. “Novel mmWave NMOS Device for High Pout mmWave Power Amplifiers in 45RFSOI”. In: *2021 - IEEE 51st European Solid-State Device Research Conference* (2021), pp. 199–202.

[63] KA. Kar-Roy et al. “Recent developments using TowerJazz SiGe BiCMOS platform for mmWave and THz applications”. In: *Proceedings of the SPIE* (2013).

[64] R.A. Murphy. “Surface-oriented Schottky barrier diodes for millimeter and submillimeter wave applications”. In: *Proceedings of 1978 IEEE International Electron Devices Meeting* (1978), pp. 124–128.

[65] A. Chu et al. “31 GHz monolithic GaAs mixer/preamplifier circuit for receiver applications”. In: *IEEE Trans. Electron Devices* 28 (1981), pp. 149–154.

[66] P.M. Roodaki et al. “A survey of millimeter-wave technologies”. In: *Proceedings of 2011 International Conference on Electrical and Control Engineering* (2011), pp. 5726–5728.

[67] S.P. Voinigesku et al. “A comparison of Si CMOS, SiGe BiCMOS and InP HBT technologies for high-speed and millimeter-wave ICs”. In: *Proceedings of 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2004), pp. 111–114.

[68] J. Schellenberg et al. “Broadband 2 W GaN MMIC”. In: *Proceedings of 2013 IEEE MTT-S International Microwave Symposium Digest (IMS)* (2013), pp. 1–4.

[69] H. Wang et al. “MMICs in the millimeter-wave regime”. In: *IEEE Microw. Mag.* 1 (2009), pp. 99–117.

[70] Yole Group. “Ultra-Wideband Comparison 2024. Technology, Process and Cost Comparison Report”. In: (2024).

[71] H. Hashemi et al. *mm-Wave Silicon Power Amplifiers and Transmitters*. Cambridge Univeristy Press, 2015.

[72] E. Brezza. “Developmente and Evaluation of a New Si/SiGe Heterojunction Bipolar Transistor Architecture for a High-Performance and Low Cost 55 nm BiCMOS technology”. PhD thesis. Université des sciences et technologies de Lille, 2022.

[73] A. Gauthier. “Etude et développement d’une nouvelle architecture de transistor bipolaire à hétérojonction Si / SiGe compatible avec la technologie CMOS FD-SOI”. PhD thesis. Université des sciences et technologies de Lille, 2019.

[74] A. A. Abidi. “RF CMOS Comes of Age”. In: *IEEE Journal of Solid-State Circuits* (2004), pp. 549–561.

[75] N. Ishihara et al. “RF CMOS Integrated Circuit: History, Current Status and Future Prospects”. In: *IEICE Trans. Fundamentals* (2011), pp. 556–567.

[76] J. P. Raskin et al. “SOI technology pushes the limits of CMOS for RF applications”. In: *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2016), pp. 17–20.

[77] J. P. Colinge. *Silicon-On-Insulator Technology: Materials to VLSI, 3rd Edition*. th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2004.

[78] D. Tsoukalas et al. “Reduction of the Reverse Short Channel Effect in Thick SOI MOSFET’s”. In: *IEEE ELECTRON DEVICE LETTERS* (1997), pp. 90–92.

[79] J. P. Colinge. “Reduction of Kink Effect in Thin-Film SO1 MOSFET’s”. In: *IEEE ELECTRON DEVICE LETTERS* (1988), pp. 97–99.

[80] C. Ortolland et al. “Stress Memorization Technique—Fundamental Understanding and Low-Cost Integration for Advanced CMOS Technology Using a Nonselective Process”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (2009), pp. 1690–1697.

[81] P. A. Rabben. “RFSOI: Delivering Performance and Integration for the Next Generation of Mobile”. In: (2016).

[82] UMC Present. “RFSOI Technology”. In: (2019).

[83] “RFSOI + HR-Bulk SW Roadmap”. In: (2019).

[84] K. Lin. “RF-SOI Technology”. In: (2019).

[85] F. Gianesello et al. “Advanced 200-mm RF SOI technology exhibiting 78 fs RON x COFF and 3.7 V breakdown voltage targeting sub 6 GHz 5G FEM”. In: *IEEE Radio Frequency Integrated Circuits Symposium* (2022), pp. 191–194.

2

ThinSOI Project

The ThinSOI project aims to enhance the performance of CMOS65SOIMMW Partially-Depleted Silicon-on-Insulator (PDSOI) transistors [1, 2] by minimizing the parasitic capacitances associated with the substrate. This has been pursued by manufacturing devices on substrates with SOI thinner than the conventional 75 nm thickness. By decreasing the SOI thickness, we anticipate a reduction in capacitive elements linked to the substrate, specifically the junction capacitances (C_{BD} and C_{BS}) and the inner fringing capacitances, C_{IF}, which in turn reduce gate-to-drain/source capacitance, $C_{\mathrm{G\text{-}DS}}$. Since the Figure of Merits of RF switch devices are closely connected to parasitic capacitances, this reduction is expected to strongly enhance devices' performance. Within this chapter, we will present and examine the findings from the ThinSOI project for RF switch devices. The initial section focuses on the manufacturing process details, including the thinning process and silicide considerations. The discussion about the DC Parametric Tests (PTs) results follows, sheding light on the static behavior of devices and its variation with SOI thickness. The RF analysis will then be presented, discussing the effects of SOI thickness on high-frequency performance, as deduced from S-parameter measurements. This section will be the starting point for a deep discussion about the breakdown phenomena in RF switch devices, reported in the following paragraph. To conclude, we will offer a succinct summary and propose directions for future work, aiming to extend the project's scope for ongoing research and development of novel devices.

2.1 RF switch devices

2.1.1 Process

Within the scope of the ThinSOI project, research has been conducted on four different SOI substrate thicknesses: 75 nm, 55 nm, 45 nm, and 35 nm. The standard 75-nm and the 55-nm SOI wafers were sourced from Soitec, while the 45-nm and

35-nm SOI substrates were produced onsite at STMicroelectronics. The latter two were derived from standard 75-nm SOI wafers, which underwent a thinning process at the initial stages of the fabrication workflow. This process involved a series of controlled silicon oxidation steps, followed by targeted etching to remove the newly formed oxide layers, resulting in the desired thinner SOI substrates.

The fabrication of thin SOI substrates involved the use of both wet oxidation and Rapid Thermal Oxidation (RTO) with In Situ Steam Generation (ISSG) techniques. The primary distinctions between these methods lie in the thickness of oxide they can generate and their respective oxidation rates, with wet oxidation being significantly faster. Wet oxidation is typically employed for creating thick oxide layers, up to 30 nm. For thinner oxides, RTO becomes the preferred method, as the oxide thickness can be better controlled. The wet oxidation process exposes the wafer to an environment rich in water vapor within a reaction chamber, accelerating the oxidation process. Conversely, ISSG represents a form of wet oxidation where steam is produced directly adjacent to the wafer surface, which moderates the oxidation rate. In ISSG, hydrogen (H_2) acts as a catalyst, creating an O_2+H_2 atmosphere inside the chamber [3, 4, 5, 6]. Following oxide formation, a series of wet etching steps was implemented to remove the oxide. This etching process included: (1) immersing the wafer in a hydrofluoric acid (HF) solution, (2) applying a cleaning procedure using ammonia and hydrogen peroxide to remove larger oxide particles, (3) employing a nanospray technique with the same solution to cleanse the wafer of smaller oxide particles, and (4) using a hydrochloric acid (HCl) solution for removing metallic contaminants.

To reduce the standard substrate to 45 nm, (1) a first oxide of 40 nm was grown by wet oxidation, which was calibrated to consume 20 nm of silicon, followed by (2) an etching step with HF 3.3%, 33 s of cleaning process, 24 s of nanospray and 10 s in HCl bath. (3) A RTO ISSG process was then carried out to form 10 nm of silicon oxide, consuming 5 nm of silicon. This step consisted of a 110 s treatment at T = 900 °C, with a gas composed of 24.2 L of O_2 and 11.8 L of H_2 at 8 Torr. The oxide was then removed by means of (4) another etching step, like the previous one, with HF 3.3%, 21 s of cleaning process, 24 s of nanospray and 10 s in HCl bath. Step (3) and (4) were then repeated once again to consume the remaining 5 nm of silicon (Fig. 2.1).

The production of 35 nm SOI substrates required a less complex process, involving a single wet oxidation step followed by an etching step. Wet oxidation was calibrated to form an oxide of 80 nm, which consumes about 40 nm of silicon. To remove the

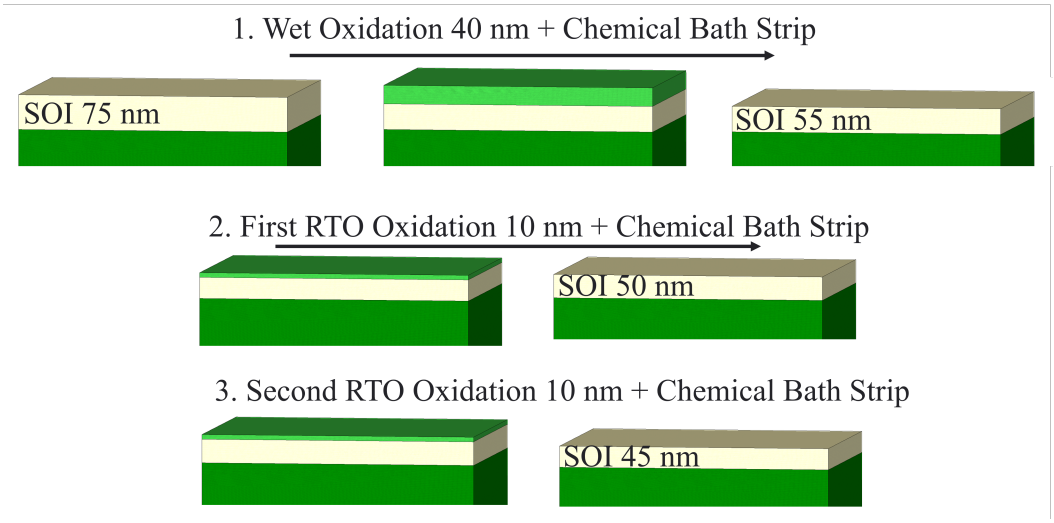


Fig. 2.1.: The thinning process for obtaining 45-nm SOI substrates starting from standard wafers is reported. A first wet oxidation step is conducted, which consumes 20 nm of silicon forming a 40-nm oxide. The oxide is then chemically removed. A RTO step follows, which forms an oxide of 10 nm, consuming 5 nm of SOI, that is stripped by another chemical bath. RTO and the last etching step are conducted once again, finally obtaining an SOI layer of 45 nm.

entire oxide, a HF 5% solution was used, together with a 30 s cleaning step, 24 s of nanospray, and 10 s of HCl bath.

To ascertain the precise SOI thickness following the thinning procedure, ellipsometry was utilized, which involved taking measurements on specially designed test structures on each die. Ellipsometry is an optical technique that can accurately gauge the thickness of layers on substrates to a few nanometers. It does so by analyzing how a light beam's polarization changes after it strikes and reflects off the sample. The resulting spectral data are interpreted using a substrate model to deduce the thickness of the layers.

For each thickness, two wafers were examined, with measurements taken at 16 distinct points on each wafer to assess the uniformity of the thinning process.

The resulting SOI thicknesses for the nominally 75-nm, 55-nm, 45-nm, and 35-nm substrates were measured to be (73.6 ± 0.2) nm, (53.7 ± 0.4) nm, (45.5 ± 0.4) nm, and (39.1 ± 0.3) nm, respectively. The thinning process for the 45-nm SOI successfully met the target thickness. However, the final thickness for the 35-nm SOI was found to be 4 nm more than anticipated, which may be attributed to the challenges in accurately calibrating the 80-nm wet oxidation. For future experiments, a multi-step process similar to that used for the 45-nm SOI is recommended. Nonetheless, the relative errors for the in-house produced thicknesses were on par with those of the

Tab. 2.1.: Split matrix of the implantations cocktails used. Less PWELL energy or a modified LDD dose were used for studying their impact on RF switch devices' performance at different t_{SOI}.

	Test conducted with:			
	STD Implants	**Less Energy PWELL**	**Double LDD Dose**	**Half LDD Dose**
	B 20 keV As 1e15 cm^{-2}	B 10 keV As 1e15 cm^{-2}	B 20 keV As 2e15 cm^{-2}	B 20 keV As 5e14 cm^{-2}
75-nm SOI	Yes			
55-nm SOI	Yes	Yes	Yes	
45-nm SOI	Yes	Yes		Yes
35-nm SOI	Yes	Yes		Yes

purchased substrates, indicating that the thinning processes used were effective in producing SOI substrates with satisfactory uniformity across the wafers.

Some samples have been treated with modified body (PWELL) and Lightly Doped Drain (LDD) implantations conditions, in order to study the doping profiles impact on RF switch devices' performance at different SOI thicknesses (t_{SOI}). As RF switches devices are NMOS transistors, the standard CMOS65SOIMMW fabrication process involves SOI to be doped with boron by means of two implantations with two different energies, resulting, after thermal treatment, in a flat doping profile. Boron is firstly implanted at 10 keV and 3.9e12 cm^{-2} of dose, and secondly at 20 keV and 5.6e12 cm^{-2}. For LDD, a 6 keV arsenic implantation with a dose of 1e15 cm^{-2} is normally employed. For some wafers, the energy of the second boron implantation was reduced to 10 keV, while for others arsenic dose was doubled to 2e15 cm^{-2} or halved to 5e14 cm^{-2}. The split matrix is reported in Tab. 2.1.

Additionally, silicidation needed to be modified for 35-nm SOI wafers. The conventional CMOS65SOIMMW procedure includes creating a 28 nm layer of silicon-enriched nickel (Ni(Pt)Si) to establish an ohmic contact between the silicon and metal layers. The process begins with the deposition of NiPt and a titanium nitride (TiN) layer, followed by a Rapid Thermal Process (RTP) at 265 °C for 60 seconds. This step initiates a solid-state reaction with the silicon, consuming part of the metal layer. Afterward, an etching process removes any metal that did not react. A second RTP at 390 °C for 30 seconds is then performed to create the desired less resistive crystalline silicide phase [7, 8].

Typically, for standard substrates, the silicide layer does not reach the buried oxide (BOx) layer below because the thickness of the Silicon-on-Insulator (t_{SOI}) is greater

than that of the silicide (t_{silicide}). However, with a starting thickness of 35 nm for SOI, the cumulative effects of oxidation, etching, and resin removal steps result in a t_{SOI} at the silicide formation step that is less than t_{silicide}. If the standard silicide method is applied, the solid-state reaction would completely consume the silicon layer between the surface and the BOx. Subsequently, nickel begins to diffuse sideways to sustain the reaction, potentially leading to the formation of silicide bridges across junctions and within the transistor channel (Fig. 2.2). This issue, commonly referred to as 'piping', can cause device failure upon application of voltage. In cases where the entire channel is silicided, it can even lead to the transistor's total failure due to a short circuit (Fig. 2.3).

To avoid piping, the SiNi thickness target was reduced from 28 nm to 18 nm by changing the conditions of the first RTP to 253 °C for 30 s. A first verification of the success of this new recipe was given by inline ellipsometry measurements, which reported the formation of a 17 nm silicide layer. EDX measurements conducted on these new samples reported a thickness of 20 nm and confirmed that no piping occured. Indeed, Fig. 2.4 show that Ni stops diffusing close to the spacers, without entering into the transistor's channel.

As previously mentioned, the silicon thickness is inadvertently reduced due to oxidation, etching, and resin stripping processes. It was essential to maintain strict control over the silicon's actual thickness until the completion of the production process. This control is crucial not only to avoid complications, such as the previously discussed silicide issue, but also to accurately interpret and link the electrical performance outcomes that will be observed.

Ellipsometry assessments conducted on SOI substrates with an initial thickness of 73.6 nm (the nominal 75-nm SOI) indicated a reduced final thickness of approximately 61 nm, reflecting a reduction of nearly 12 nm from the original SOI. For other substrates, it was not feasible to directly measure the SOI thickness through to

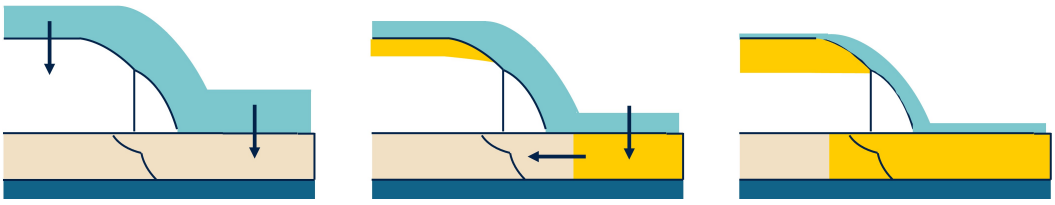


Fig. 2.2.: The piping process is schematically represented. Once the NiPt is deposited, the solid state reaction with silicon is activated by RTP, forming vertically the silicide Ni(Pt)Si. Given the limited thickness of the SOI and the amount of reagent still available, the reaction continues but horizontally, passing through the contact junction and arriving inside the channel.

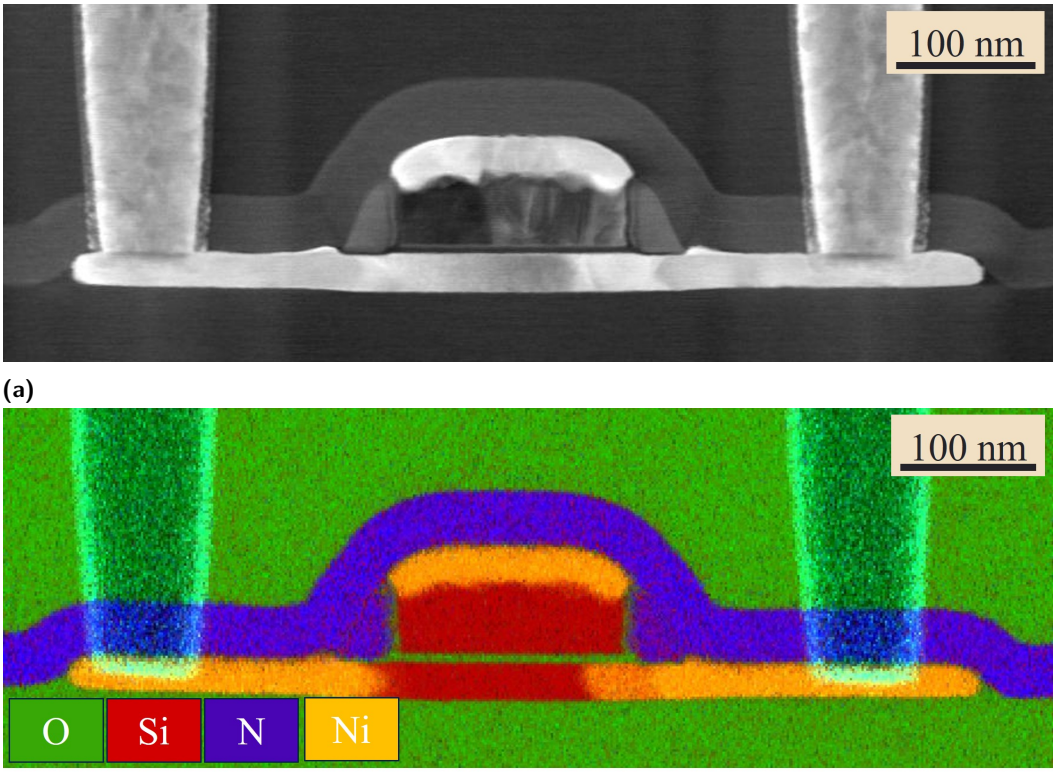
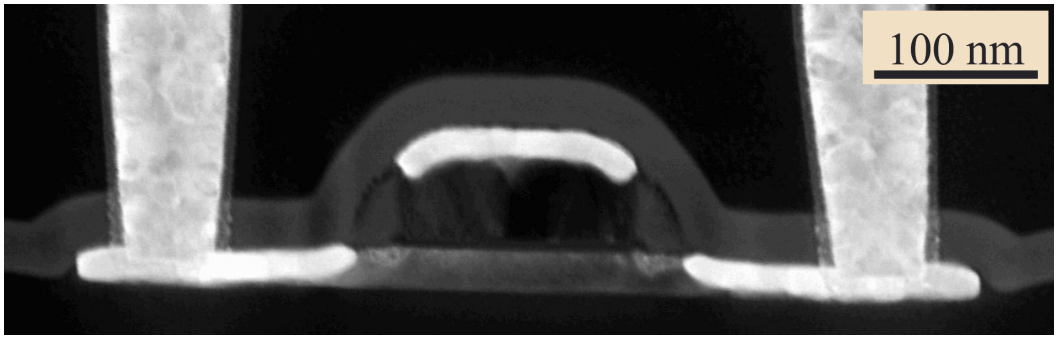
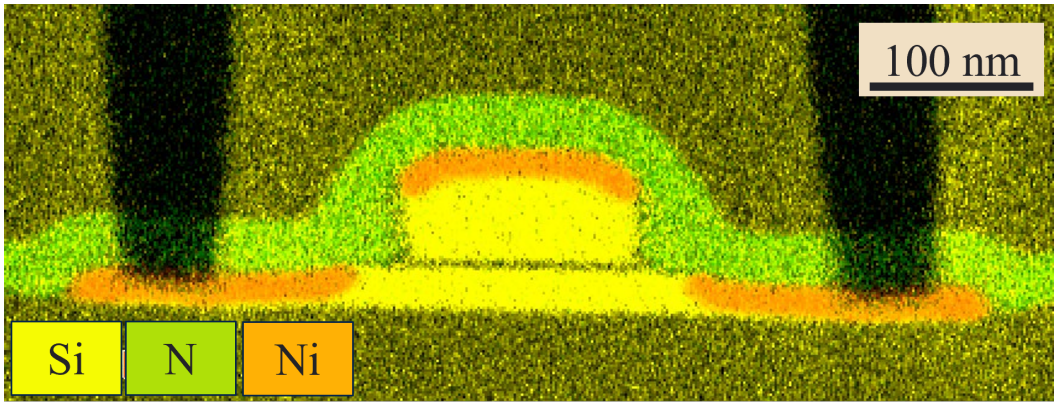


Fig. 2.3.: a) HAADF image of a 35-nm SOI device with $L_G = 0.18$ µm treated with the standard silicide recipe. Due to the non-optimization of the silicide thickness, piping occurs below the spacers. b) Visualization of the EDX signals for oxygen, silicon, nitrogen, and nickel, showing that piping is accentuated following the application of a positive voltage. Indeed, Ni is found inside the channel.



(a)



(b)

Fig. 2.4.: a) HAADF image of a 35-nm SOI device with $L_G = 0.18$ µm treated with the new silicide recipe. b) Visualization of the EDX signals for silicon, nitrogen, and nickel. The silicide is found only inside the junctions and did not exceed the position of the spacers, confirming the perfect optimization of the silicidation step.

the end of the process, as the models used to fit the ellipsometry data were not calibrated for such thin layers of SOI. Since the rate of silicon consumption is not anticipated to vary based on the thickness of the SOI, the subsequent sections will assume that the final thicknesses of the SOI for various substrates are equivalent to the initial thicknesses decreased by 12 nm.

2.1.2 Parametric Tests Analysis

Prior to delving into the RF characteristics of our devices, we offer an examination of how the variations in SOI thickness have influenced the static behavior of the devices. This analysis will outline the relationship between the thickness of the SOI (t_{SOI}) and certain parameters that are typically assessed during Parametric Tests (PTs). PTs are routinely performed in line with the fabrication process using probe cards that interact with test structures located at the periphery of each die. The values for each parameter discussed in this report represent the median of measurements taken from a minimum of five distinct devices. This preliminary analysis aims to shed light on the effects of SOI thickness on device performance and will serve as a foundation for the subsequent discussion of the RF findings.

To get a first insight into devices' behavior as a function of t_{SOI}, threshold voltage (V_{th}), On current (I_{DS}), and leakage current (I_{OFF}) have been measured for devices with different gate lengths. Threshold voltage has been extracted in linear regime conditions, that is $V_{\mathrm{DS}} = 0.1$ V, and probing V_{GS} until reaching $I_{\mathrm{DS}} = 100 \cdot W_{\mathrm{G}}/L_{\mathrm{G}}$ nA, with W_{G} and L_{G} being the gate width and length, respectively. I_{DS} was evaluated at $V_{\mathrm{DS}} = 0.1$ V and $V_{\mathrm{GS}} = 3.3$ V. I_{OFF} was obtained at $V_{\mathrm{DS}} = 2.5$ V and $V_{\mathrm{GS}} = 0$ V. Moreover, $R_{\mathrm{ON\text{-}DC}}$ was also extracted but only for devices with $L_{\mathrm{G}} = 0.18$ µm, at $V_{\mathrm{DS}} = 0.1$ V and $V_{\mathrm{GS}} = 2.5$ V. All measurements have been performed on devices with gate width (W_{G}) of 2.5 µm. The PT data of samples with different SOI thicknesses and standard implantations are reported in Fig. 2.5.

The threshold voltage graph (Fig. 2.5a) indicates that V_{th} is influenced by the thickness of the SOI, with thinner SOI layers leading to a decrease in V_{th} values. The most significant V_{th} shift observed is 0.4 V, occurring when the t_{SOI} is reduced to 35 nm and the gate length is 0.18 µm. Nonetheless, for devices with the same substrate but shorter channels, the difference in V_{th} is less pronounced. This is attributed to the diminished Short Channel Effect (SCE) in 35-nm SOI devices compared to those with 75-nm SOI, with respective V_{th} reductions of 0.15 V and 0.35 V. The lesser SCE in thinner SOI devices is beneficial for electrostatic control of the channel, a phenomenon that is well-documented in standard literature [9, 10, 11,

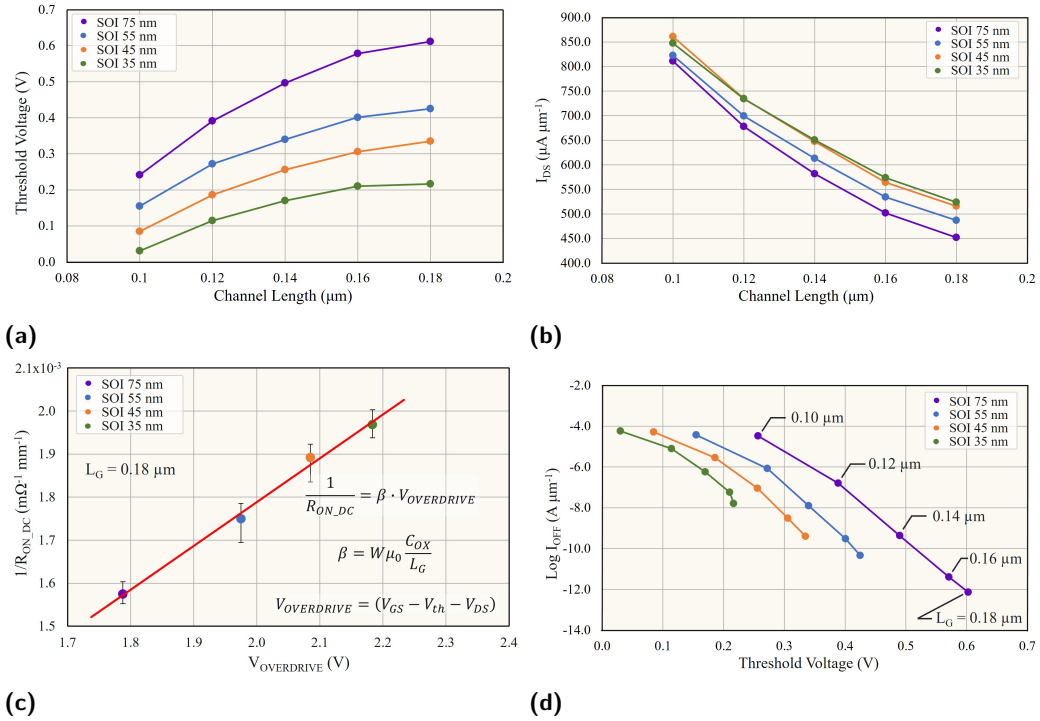


Fig. 2.5.: The most important PT results obtained for all SOI substrates studied are reported in figures. a) Threshold voltages as a function of channel length. The shift in V_{th} is clearly observable as well as the decrease of the roll-off phenomenon in thin SOI. b) ON current as a function of channel length. c) $1/R_{\mathrm{ON\text{-}DC}}$ vs $V_{\mathrm{OVERDRIVE}}$. The linear relationship between the two parameters confirms that the slight increase in current for thin SOI is due to the V_{th} shift. d) I_{OFF} as a function of V_{th}.

12, 13]. While the V_{th} shift can be a 'second order' concern for long-channel devices, such as those with $L_{\mathrm{G}} = 0.18$ um, it becomes a more critical issue for shorter-channel devices due to the shift approaching 0 V. Since threshold voltage determines key device properties like the On-resistance (R_{ON}) and breakdown voltage, maintaining control over V_{th} is crucial for the production of functional devices.

The observed decrease in V_{th} with thinner SOI is explained by the fact that maintaining the same implantation energy for the PWELL process results in boron being implanted into the BOx, which in turn lowers the doping concentration in the SOI. This hypothesis was validated through Technology Computer-Aided Design (TCAD) simulations using Sentaurus Synopsys [14], which demonstrated that with a reduced t_{SOI} and unoptimized implantation energies, the majority of the boron initially implanted no longer resides in the SOI. Post-thermal treatment, the activated doping concentration as simulated by TCAD showed a significant decrease of nearly 50%, dropping from 4.7e17 cm^{-3} in a 75-n SOI to 2.4e17 cm^{-3} in a 35-nm SOI (Fig. 2.6).

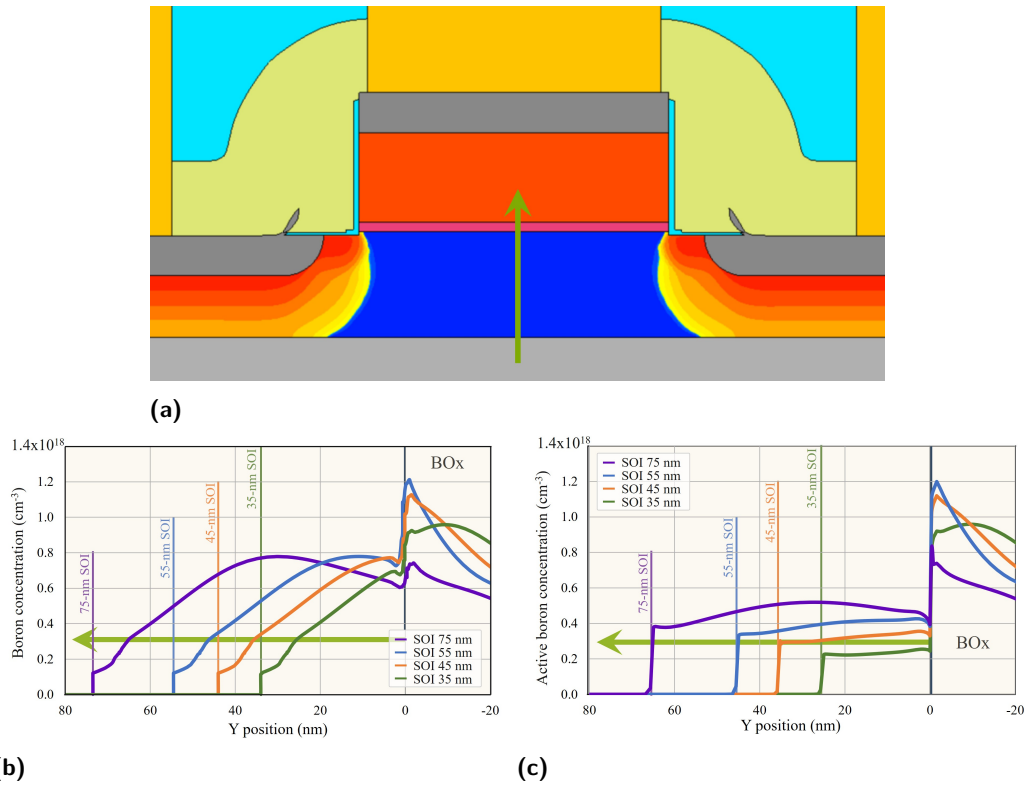
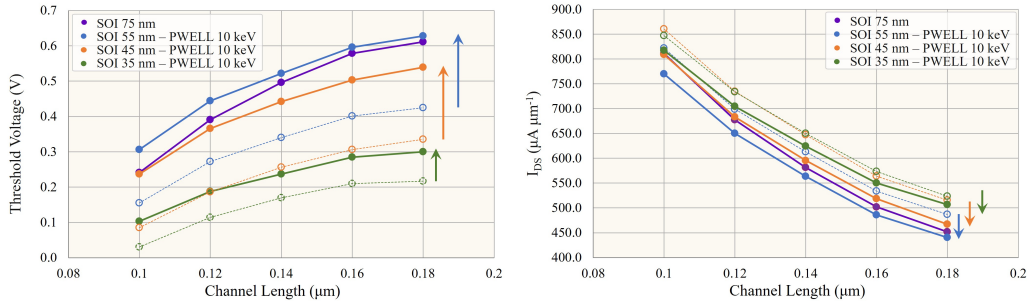


Fig. 2.6.: a) TCAD representation of a simulated RF switch device. The vertical arrow indicates the y-direction of the following two graphs. b) As-implanted boron profiles for the four SOI substrates studied. It can be seen that as t_{SOI} decreases, the boron is increasingly implanted inside the BOx. c) Concentration profiles of activated boron at the end of the process. The lower concentration obtained in thin SOI explains the drastic reduction of threshold voltage.

To solve this problem a lower implant energy can be used, reducing the implant depth. An implantation process using a 10 keV PWELL instead of the standard 20-keV implant has been experimented with across various SOI types, revealing that it is indeed possible to raise the threshold voltage to the initial value of the 75-nm SOI (Fig. 2.7a). In the case of the 55-nm SOI, the V_{th} was fully restored to its standard value. However, for the 45-nm and 35-nm SOI substrates, the V_{th} did not return to the standard levels, indicating that a further reduction in implantation energy might be necessary to achieve the desired V_{th}.

The I_{DS} and On-resistance (R_{ON}) are anticipated to be significantly influenced by changes in the threshold voltage (V_{th}), despite the bias conditions that are employed to lessen the impact of V_{th}. It has been observed that I_{DS} increases with the reduction of SOI thickness due to the corresponding decrease in V_{th} (Fig. 2.5b). Nevertheless, the variation in I_{DS} is not as pronounced as that in V_{th}: for example, when comparing a device with a standard substrate to a 35-nm SOI device with



(a) **(b)**

Fig. 2.7.: a) The new threshold voltage and b) ON-current curves obtained when employing a 10 keV PWELL implant are compared with the ones of the standard implantation shown in Fig. 2.5. An increase in V_{th} is always achieved but for the 35-nm SOI the values are still much lower than the standard ones.

a L_{G} of 0.18 µm, V_{th} decreases by 55%, while I_{DS} only increases by 16%. This discrepancy is likely because at a gate-source voltage (V_{GS}) of 3.3 V, the channels in both devices are nearly fully open, and the current is less dependent on the difference between V_{GS} and V_{th}. Instead, it is more significantly influenced by shunt resistances, which remain unchanged with varying SOI thickness. Furthermore, as the V_{th} difference diminishes with smaller L_{G} dimensions, I_{DS} also decreases, narrowing the gap between the Process-Of-Reference (POR, the standard 75-nm SOI) and thin SOI values.

When V_{th} is adjusted back to standard levels through a lower-energy PWELL implantation, the I_{DS} values of the POR are nearly fully restored. However, since the V_{th} for the 35-nm SOI was not completely returned to standard, the I_{DS} for this thickness also remains higher than the standard case (Fig. 2.7b).

$R_{\mathrm{ON\text{-}DC}}$ extracted at $V_{\mathrm{GS}} = 2.5$ V shows a more evident shift of its value when reducing t_{SOI} because V_{GS} is lower than the I_{DS} case, and hence V_{th} has a major influence on current (Fig. 2.5c). To verify that only the V_{th} variation was the cause for having reducing R_{ON} values when lowering t_{SOI}, the reciprocal of $R_{\mathrm{ON\text{-}DC}}$ has been studied as a function of $V_{\mathrm{OVERDRIVE}}$, defined as V_{GS}-V_{th}-V_{DS}, at different t_{SOI}. The linear relationship between the two parameters can be easily extracted from the current characteristic equation of a common MOSFET, which implies:

$$I_{\mathrm{DS}} = K\frac{W_{\mathrm{G}}}{L_{\mathrm{G}}}V_{\mathrm{OVERDRIVE}}V_{\mathrm{DS}} \tag{2.1}$$

With K being μC_{OX}, where μ is the electrons mobility and C_{OX} the oxide capacitance. The analysis conducted in Fig. 2.5c clearly reported that $1/R_{\mathrm{ON\text{-}DC}}$ depends linearly

on $V_{\text{OVERDRIVE}}$ and hence on V_{th}. This feature confirmed the fact that t_{SOI} does not impact directly the value of R_{ON} but its reduction comes from the down-shift of V_{th}, due to the decrease of doping concentration. Moreover, the linear relationship between the two parameters suggests that the reduced doping concentration did not impact electrons' mobility.

The On-resistance (R_{ON}) is influenced not only by the threshold voltage (V_{th}) but also by the dose of the Lightly Doped Drain (LDD) implant (Fig. 2.8). Under the given bias conditions, when comparing samples that have the same PWELL but different LDD doses, it has been observed that a 50% reduction in the arsenic dose results in a 3.4% increase in R_{ON}. Conversely, R_{ON} decreases by 2.3% when the arsenic dose is doubled. This occurs because the access resistance of the LDD region is directly related to the concentration of the LDD dose.

Finally, as expected, the decrease of V_{th} also impacts leakage current by increasing its value, in particular for long channel devices (Fig. 2.5d), passing from 10^{-12} A/µm for the POR SOI to 10^{-8} A/µm for 35-nm SOI. However, the worsening of the characteristic is almost completely suppressed for short channel devices most likely due to the improvement in electrostatic channel control.

C_{OFF} represents the capacitance between the drain and source when the transistor is in the Off state. It is calculated as the sum of the gate-to-drain/source capacitance ($C_{\text{G-DS}}$) and the body-to-drain/source capacitance ($C_{\text{B-DS}}$) divided by 4, as explained in Fig. 2.9. Low-frequency AC measurements performed during PTs allow for the identification of the two separate contributions to C_{OFF}, $C_{\text{G-DS}}$ and $C_{\text{B-DS}}$, which are indistinguishable in RF measurements.

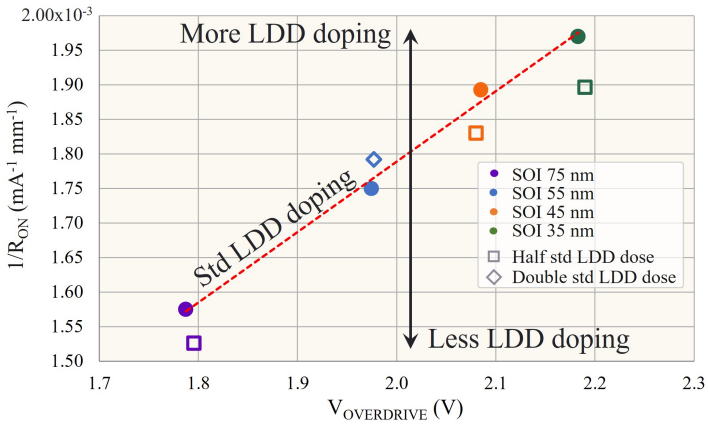
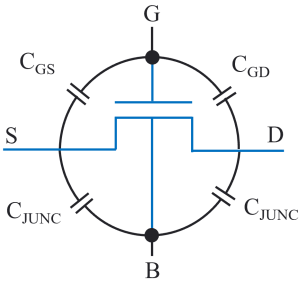


Fig. 2.8.: $1/R_{\text{ON-DC}}$ vs $V_{\text{OVERDRIVE}}$ for different LDD implantations. When the LDD dose is doubled (halved), $R_{\text{ON-DC}}$ decreases (increases) and hence $1/R_{\text{ON-DC}}$ increases (decreases).



$$C_{OFF} = \left(\frac{1}{\frac{1}{C_{GD}} + \frac{1}{C_{GS}}} \right) + \left(\frac{C_{JUNC}}{2} \right) = \frac{C_{GD}}{2} + \frac{C_{JUNC}}{2}$$

$$C_{GS} = C_{GD} = C_{G\text{-}DS} / 2$$

$$C_{JUNC} = C_{B\text{-}DS} / 2$$

$$\mathbf{C_{OFF} = \frac{C_{G\text{-}DS} + C_{B\text{-}DS}}{4}}$$

Fig. 2.9.: Circuit diagram of a transistor showing the capacitance contributions that form C_{OFF}. On the right the expression of C_{OFF} as a function of $C_{\mathrm{G\text{-}DS}}$ and $C_{\mathrm{B\text{-}DS}}$ has been derived.

Two measurements are required to obtain independently $C_{\mathrm{G\text{-}DS}}$ and $C_{\mathrm{B\text{-}DS}}$: for the former a voltage of 2.5 V is applied to the shorted drain and source terminals, while the body is grounded; for the latter, the same voltage is applied to drain and source but this time gate is grounded. The measurement frequency was set to 100 kHz, with an AC signal amplitude of 0.1 V. These capacitances were measured on large structures consisting of three parallel stacks, each with 888 gate fingers, and with a L_{G} of 0.18 µm and W_{G} of 2.5 µm, totaling to 6660 µm².

The findings for $C_{\mathrm{B\text{-}DS}}$ are not reported as the thinning of t_{SOI} did not show a significant effect on its value, which is very low in any case. Indeed, analysis of the $C_{\mathrm{B\text{-}DS}}$ versus V_{GS} curves and TCAD simulations confirmed that our RF switch devices on a 75-nm SOI substrate are already in a fully depleted state when 2.5 V is applied to the contacts. The application of an AC signal does not substantially alter the depletion region between source and drain and the body, resulting in a consistently low measured capacitance. Moreover, instrumental limitations and calibration issues cause $C_{\mathrm{B\text{-}DS}}$ to exhibit negative values in the order of a few femtofarads per millimeter (fF/mm), which have not physical meaning. The same reasoning applies to $C_{\mathrm{B\text{-}DS}}$ measurements on thinner SOI substrates. Therefore, a definitive assessment of t_{SOI}'s impact on $C_{\mathrm{B\text{-}DS}}$ is not feasible.

On the other hand, $C_{\mathrm{G\text{-}DS}}$ has been found to decrease with the reduction of SOI thickness by about 3%, 5%, and 7% for 55-nm, 45-nm, and 35-nm SOI, respectively, which in turn improved C_{OFF} of the same amount (Fig. 2.10a and d).

The total gate-drain capacitance is calculated as the sum of 3 parallel capacitances, that is $C_{\mathrm{G\text{-}DS}} = 2 \cdot (C_{\mathrm{IF}} + C_{\mathrm{OF}} + C_{\mathrm{OV}})$. In this equation, C_{IF} represents the inner fringing capacitance, C_{OF} denotes the outer fringing capacitance, and C_{OV} is the

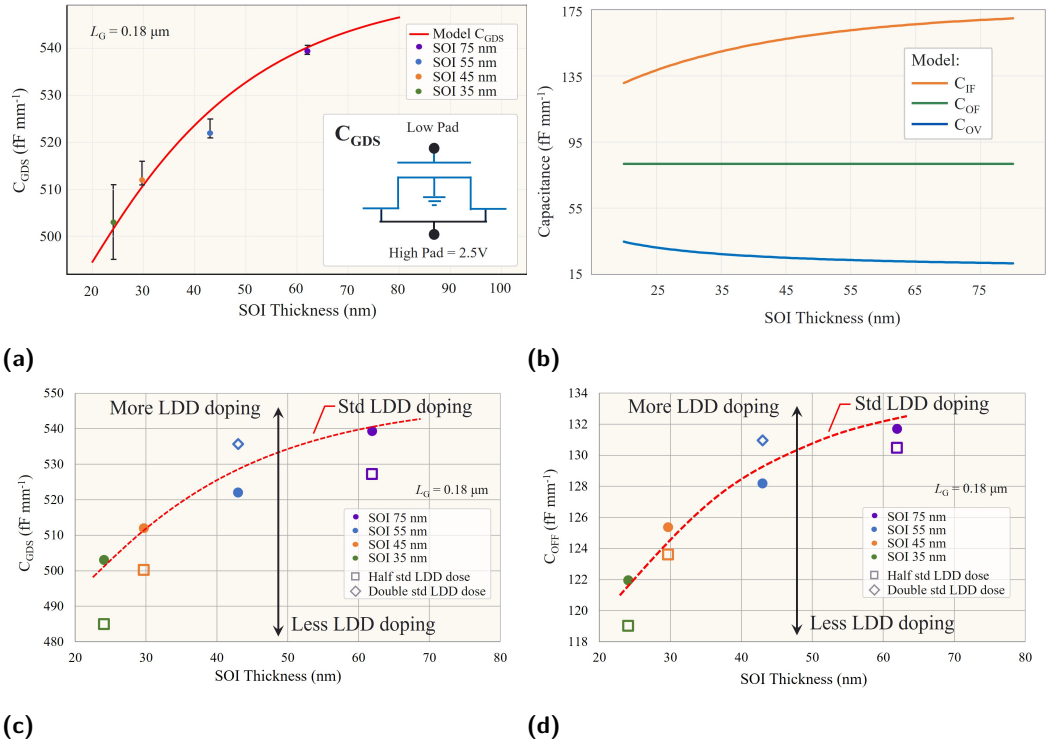


Fig. 2.10.: a) $C_{\text{G-DS}}$ as a function of t_{SOI} for devices with $L_{\text{G}} = 0.18$ µm. The model line in red is the sum of the three contributions C_{IF}, C_{OF}, and C_{OV}, whose profiles as a function of SOI thickness are reported in b). Through the reported model it was possible to trace the reduction of $C_{\text{G-DS}}$ back to the reduction of C_{IF}. c) $C_{\text{G-DS}}$ have been reported for different LDD doses. Their increase with increasing doping is given by an increase in C_{OV}. d) C_{OFF} as a function of t_{SOI} for std LDD doping and different LDD doses are reported.

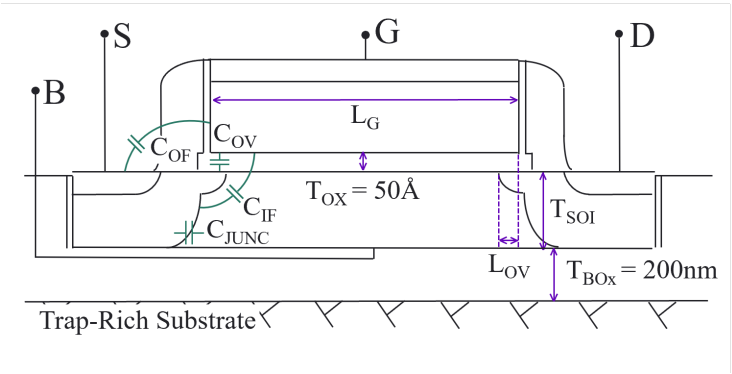


Fig. 2.11.: Schematic representation of an RF switch device showing the three components of $C_{\text{G-DS}}$. C_{OF} is an external component passing through the spacers while C_{IF} is internal to the device and the substrate and depends on t_{SOI}. Finally, C_{OV} depends on L_{OV}, that is the extension of the overlap of the LDD with the gate.

overlap capacitance, which results from the LDD region extending over the poly gate. The three contributions are well visualized in Fig. 2.11. We have utilized the capacitance model from Hiblot et al. [15], which describes the interaction between perpendicular electrodes, to mimic the experimental findings and to analyze how C_{IF}, C_{OF}, and C_{OV} change with variations in the thickness of the SOI. Our research indicates that a reduction in the inner fringing capacitance is the primary factor behind the observed decrease in $C_{\text{G-DS}}$, as reported in Fig. 2.10b). This reduction in C_{IF} can be attributed to its dependency on the depth of the junctions, which, in our technology, is equivalent to the t_{SOI} as the junctions span the entire SOI layer.

Originally, we assumed a constant C_{OV} in our calculations to emulate the pattern of $C_{\text{G-DS}}$, but this led to consistently lower results than what was experimentally observed. To align our calculations with the experimental data, it was necessary to adjust C_{OV} in response to reductions in t_{SOI}. The physical rationale behind this adjustment is that thinning the SOI layer reduces the concentration of PWELL dopants, leaving less p-type counter doping in the channel. Consequently, the n-type LDD region is able to extend further, resulting in an increased C_{OV}. Computationally, this extension of the LDD was quantified as an increase of 0.7 nm when transitioning from a 75-nm SOI to a 35-nm SOI, a change that is consistent with the altered doping concentration and the general dimensions of the devices.

Therefore, the overlap capacitance is also a significant factor in the parasitic capacitances of a device, which in turn affects the overall Off-state capacitance. Adjusting the amount of overlap between the LDD and the gate, such as by modifying the LDD dose, can control its value. The influence of the arsenic dose on both the $C_{\text{G-DS}}$ and C_{OFF} for varying thicknesses of the SOI is illustrated in Fig. 2.10c-d. A

reduction in the LDD dose by half leads to a decrease in $C_{\text{G-DS}}$ ranging from 12 to 18 fF/mm, suggesting a shrink of the LDD by 0.6 to 1 nm, depending on the t_{SOI} and consequently the PWELL concentration. This results in a C_{OFF} reduction of 1.8 to 3 fF/mm, which is approximately a 3% decrease. Conversely, doubling the LDD dose causes $C_{\text{G-DS}}$ to rise by 14 fF/mm due to a 0.7 nm increase in the LDD region, which in turn raises C_{OFF} by 3 fF/mm (a 3% increase). Therefore, decreasing the LDD dose could be an effective strategy to lower C_{OV} and improve C_{OFF}. However, it is important to note that the trend observed for C_{OFF} is the exact opposite of that for the on-resistance; as the LDD dose is reduced, R_{ON} increases. This necessitates a careful calibration of the LDD dose to balance C_{OFF} and R_{ON} and enhance the overall device performance.

In conclusion, our initial electrical analysis using parameter tests has shown that the thickness of the SOI significantly affects the static characteristics of our RF switch devices. A reduction in threshold voltage was observed in thin SOI wafers, likely due to non-optimized PWELL implantations performed with standard CMOS65SOIMMW energies, which allowed boron to penetrate the buried oxide (BOx) beneath the SOI, thus reducing the doping concentration. This shift in V_{th} led to a lower R_{ON} and a higher Off-state current, which, while potentially beneficial for $R_{\text{ON}}C_{\text{OFF}}$ performance, poses serious isolation challenges, particularly for devices with short channels. To address this, PWELL implantation energies must be tailored to the specific t_{SOI} substrate. We have shown that lowering the implantation energy by 10 keV can realign V_{th} to standard levels, thereby meeting the performance objectives for both R_{ON} and I_{OFF}. Moreover, the reduction in t_{SOI} has enhanced gate electrostatic control, as evidenced by a less pronounced V_{th} roll-off due to the Short Channel Effect in thin SOI samples compared to the standard 75-nm SOI.

One of the most notable benefits of thinning the SOI is observed in the analysis of parasitic capacitances, where a significant decrease in C_{OFF} has been documented. Devices fabricated on thin SOI substrates exhibit a reduced inner fringing contribution to $C_{\text{G-DS}}$, although C_{OV} experienced a slight increase, again due to the reduced PWELL doping concentration.

Lastly, it has been shown that both R_{ON} and C_{OFF} are affected by the arsenic dose in the LDD. A higher dose reduces R_{ON} but worsens parasitic capacitance due to an increase in overlap capacitance. Conversely, a lower LDD dose yields better parasitic capacitance performance, but at the cost of increased R_{ON} due to the deterioration of access resistances.

2.1.3 RF measurements

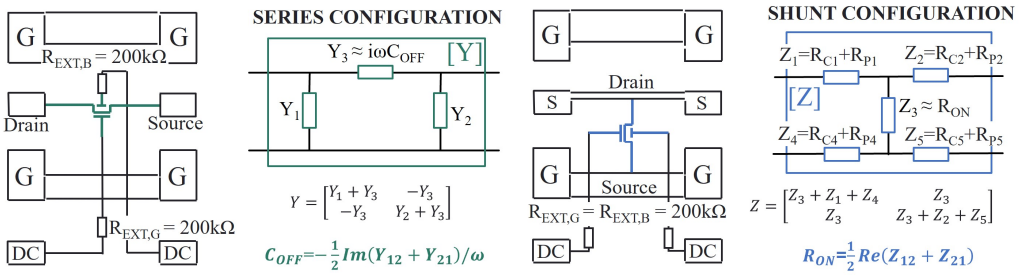
The essential parameters derived from MOS devices functioning as switches in RF applications include the On-resistance (R_{ON}), the Off-state capacitance (C_{OFF}), and the maximum RF voltage (RFV_{MAX}). The small-signal R_{ON} is determined using the device in a 'shunt' configuration, which allows for the intrinsic elimination of losses from pads and connections without the need for additional dummy structures. Similarly, the small-signal C_{OFF} is extracted from a device that is an identical replica of the Device Under Test (DUT) but configured in 'series'. This ensures consistency in the measurement conditions for C_{OFF} (Fig. 2.12).

The large-signal parameter, RFV_{MAX}, represents the input power voltage at which a significant increase in signal harmonics is observed. This parameter is typically assessed using the shunt DUT in its Off-state, as this setup is more indicative of the power handling capabilities of the switch under critical conditions.

It is important to note that all RF measurements undergo a de-embedding process to eliminate parasitic resistances and capacitances caused by metal layers and interconnections up to Metal 1.

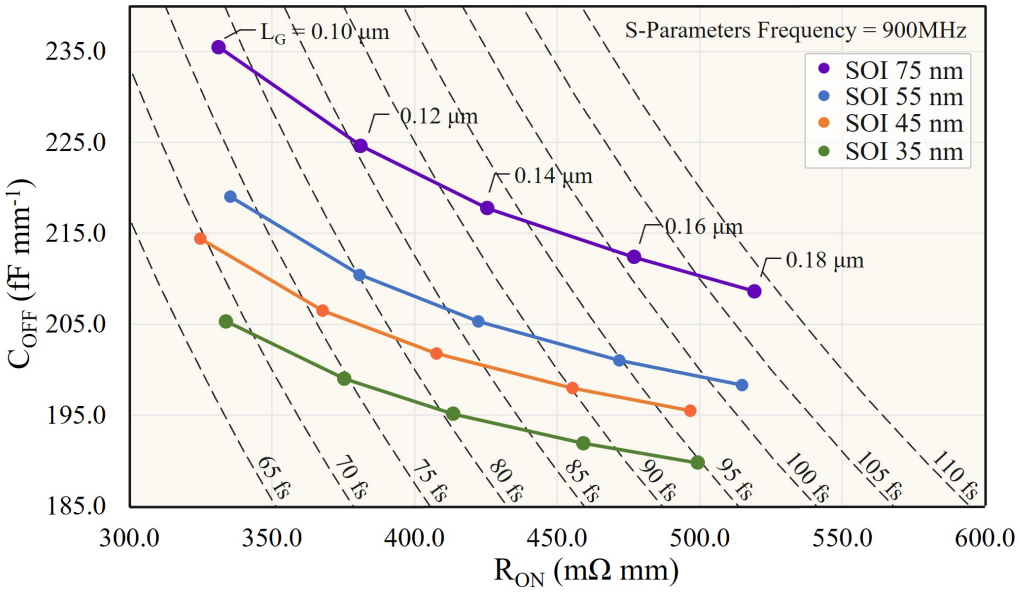
For the measurements of C_{OFF} and RFV_{MAX}, the gate-source voltage (V_{GS}) and the bulk-source voltage (V_{BS}) are set to -2.5 V to reflect Off-state conditions. In contrast, for R_{ON} measurements, V_{GS} and V_{BS} are set to +3.3 V to simulate On-state conditions.

Fig. 4.4 presents the results for a) C_{OFF} vs R_{ON} and b) $R_{ON}C_{OFF}$ vs RFV_{MAX} of devices fabricated with various SOI thicknesses and standard implantation processes. When compared to the baseline 75-nm SOI, the C_{OFF} exhibited enhancements of 5%, 7%, and 9% for devices with reduced t_{SOI} thicknesses of 55 nm, 45 nm, and 35 nm,

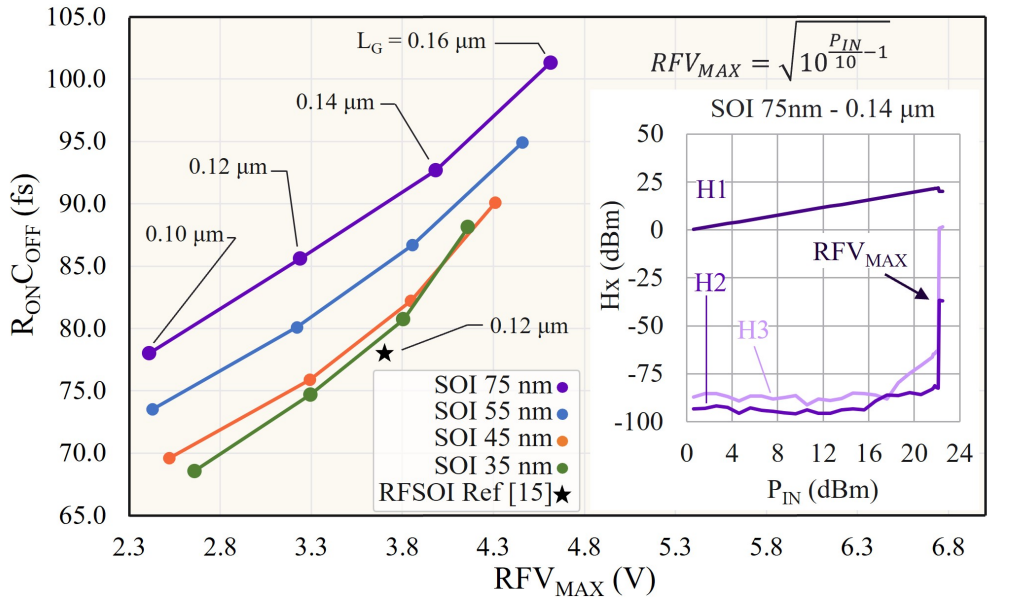


(a) **(b)**

Fig. 2.12.: Schematic representations of a device in a) series and b) shunt configuration are shown with the corresponding admittance and impedence matrix, employed to extract C_{OFF} and R_{ON}, respectively.



(a)



(b)

Fig. 2.13.: a) C_{OFF} vs R_{ON} and b) $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ vs RFV_{MAX} graphs for devices fabricated on all four SOI substrates and by employing the standard implantation recipes. A drastic reduction in C_{OFF} is obtained when reducing t_{SOI}, leading to the improvement of $R_{\mathrm{ON}}C_{\mathrm{OFF}}$. In b) the state-of-art value is also reported. Moreover, the definition of RFV_{MAX} is graphically represented as the P_{IN} value at which harmonics drastically increase.

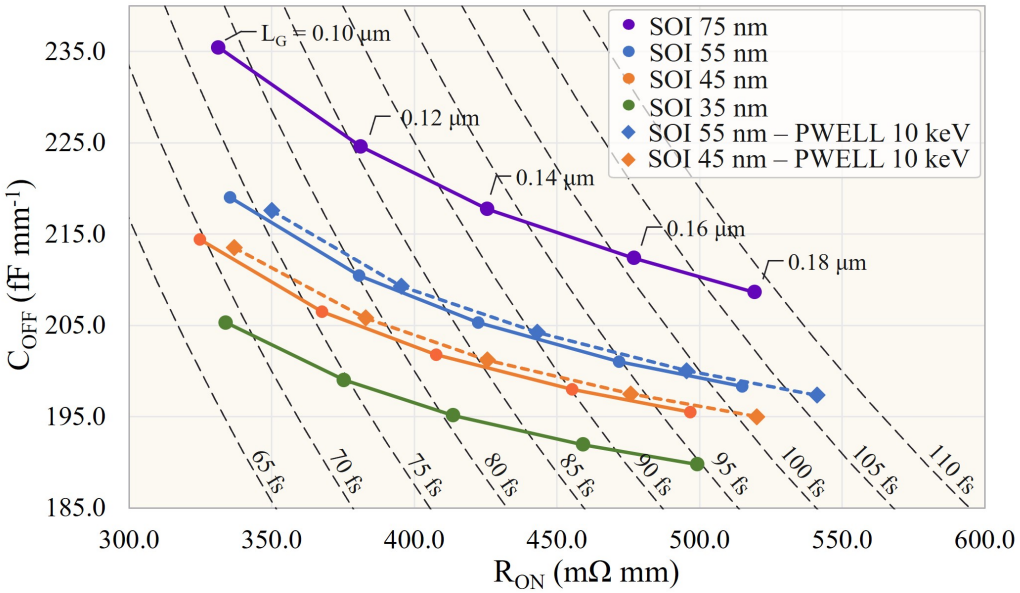
respectively. These improvements are primarily attributed to the decrease in the inner fringing capacitance, which is affected by the diminished depth of the junctions, as discussed in the preceding section. The R_{ON} has also been influenced by the thinner SOI layers, due to the associated reduction in threshold voltage; however, the variation in R_{ON} is less pronounced when compared to the Parametric Tests (PTs) values, as revealed by RF extraction methods. The most notable difference in V_{th}—and consequently in R_{ON}—is seen in devices with a gate length of 0.18 µm. For devices with shorter gate lengths, R_{ON} remains relatively stable.

Regarding the product $R_{\mathrm{ON}}C_{\mathrm{OFF}}$, the most favorable performance was observed in devices with a 35-nm SOI thickness, where there was a 14% improvement over the standard SOI thickness. This resulted in $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ values of 68 fs and 74.4 fs for devices with $L_{\mathrm{G}} = 0.10$ µm and 0.12 µm, respectively, which may be considered among the best published figures to date [16]. Nevertheless, it is important to consider the significance of power handling in the evaluation of RF switch devices. A balance between $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ and RFV_{MAX} must be maintained, as both parameters are critical for the overall benchmarking of these devices.

In devices with longer channel lengths ($L_{\mathrm{G}} > 0.12$ µm), a reduction in the thickness of the SOI leads to a decrease in the maximum RF voltage (RFV_{MAX}), as shown in Fig. 4.4b. The subsequent section will provide a more detailed explanation, but in essence, for long-channel devices, a thinner t_{SOI} results in an increase in the intrinsic body resistance ($R_{\mathrm{int,b}}$). This increase in resistance lowers the threshold for the body current of holes that activates the parasitic bipolar transistor, which in turn provokes the breakdown and hence the drastic increase in harmonics.

Conversely, devices with shorter channels benefit from enhanced electrostatic control due to the thinner SOI, which actually leads to an increase in RFV_{MAX}. Specifically, for the 35-nm SOI, there is a 10.5% increase in RFV_{MAX}. When examining devices with $L_{\mathrm{G}} = 0.10$ µm and 0.12 µm on a 35-nm SOI, the RFV_{MAX} reaches values of 2.7 V and 3.3 V, respectively. As it will be explained later, for these devices punch-through is also involved, which reduces when electrostatic control is improved.

Analyzing the relationship between $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ and RFV_{MAX}, it is evident that there is an enhancement in the performance of RF switches when the thickness of the SOI is reduced, especially for devices with short channel lengths. The improvement in $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ is directly related to the decrease in the inner fringing capacitance and consequently the $C_{\mathrm{G\text{-}DS}}$. Additionally, the power handling capabilities are also enhanced, as the breakdown in these devices is predominantly governed by electrostatic control. However, for devices with longer channels, while $R_{\mathrm{ON}}C_{\mathrm{OFF}}$



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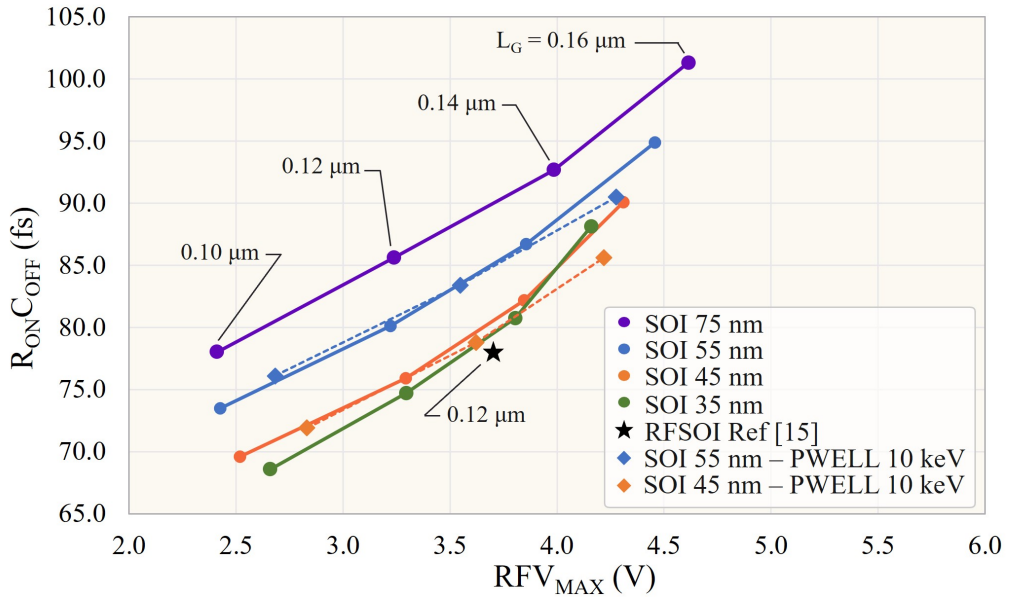


(b)

Fig. 2.14.: a) C_{OFF} vs R_{ON} and b) $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ vs RFV_{MAX} graphs for devices fabricated on all four SOI substrates and by employing a 10 keV PWELL implant step. The increase in doping inside the body also causes V_{th} to rise, consequently increasing the R_{ON} values. At the same time, RFV_{MAX} values increase due to the reduction of body resistance but only for long-channel devices.

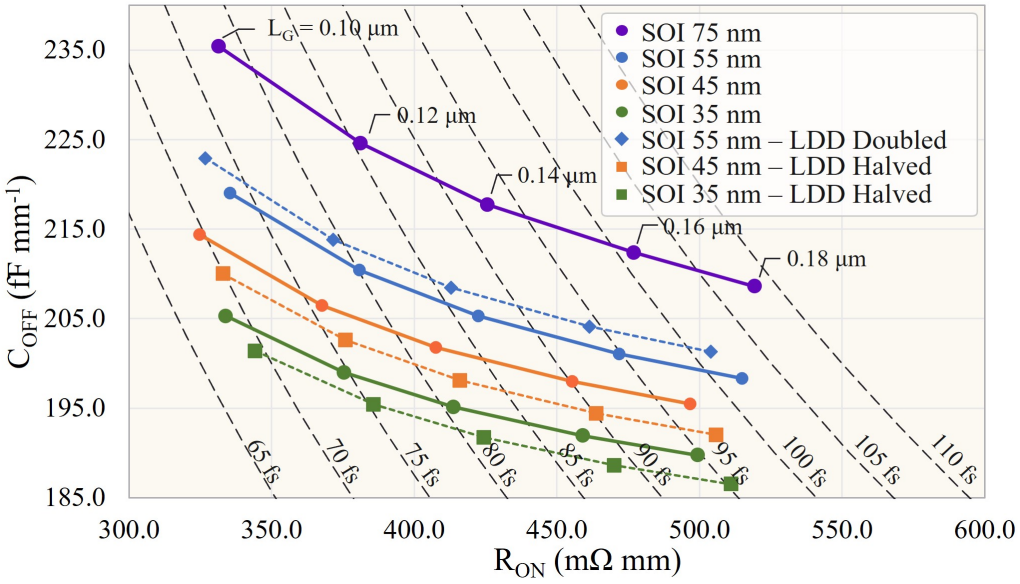
benefits from a reduction in t_{SOI}, RFV_{MAX} suffers due to breakdown being more influenced by the body resistance.

The effects of lowering the PWELL implantation energy are detailed in Fig. 2.14. As anticipated, R_{ON} is significantly increased due to the shift of the threshold voltage towards more standard values, and C_{OFF} sees a marginal improvement, likely because the increased counter p-type doping causes the n-type LDD to recede, thus reducing the overlap capacitance. When considering the $R_{\mathrm{ON}}C_{\mathrm{OFF}}$-$RFV_{\mathrm{MAX}}$ ratio, short channel devices follow a similar pattern to that observed with standard energy implantations, whereas long channel transistors experience a more pronounced improvement in RFV_{MAX} relative to the decrease in $R_{\mathrm{ON}}C_{\mathrm{OFF}}$, hence their performance are overall improved.

The same type of analysis was performed for different LDD doping conditions, as shown in Fig. 2.15. The trends identified in the parameter test analysis are also reflected in the RF measurements: doubling the arsenic dose in the LDD increases C_{OFF} while decreasing R_{ON}, leading to a net reduction in $R_{\mathrm{ON}}C_{\mathrm{OFF}}$. Conversely, halving the LDD dose enhances C_{OFF} but worsens RON, resulting in an overall increase in $R_{\mathrm{ON}}C_{\mathrm{OFF}}$. For long channel devices, reducing the LDD dose is advantageous as it slightly bolsters their power handling capacity. This improvement is due to the breakdown mechanism, which also involves the generation of minority carriers in the LDD, a process exaceR_{B}ated by the Gate Induced Drain Leakage (GIDL) effect. This effect is mitigated when a lower doping concentration is used, as will be further explained in the following section.

To summarize, the analysis of **S**-parameters and harmonic measurements, followed by the extraction of RF switch Figures of Merit, has shown enhanced performance in devices built on SOI substrates with a thinner SOI than what is typically used in CMOS65SOIMMW technology. For $R_{\mathrm{ON}}C_{\mathrm{OFF}}$, a trend emerges where its value improves progressively with thinner SOI layers. However, the behavior of RFV_{MAX} is more complex. A thinner t_{SOI} proves advantageous for short channel devices but detrimental to the power handling capabilities of long channel devices. The underlying reasons for these divergent trends are linked to the mechanisms that cause breakdown: Gate Induced Drain Leakage (GIDL) and parasitic bipolar activation in long channel devices, versus punch-through and parasitic bipolar activation in short channel devices. A comprehensive discussion on breakdown phenomena in RF switch devices will be presented in the subsequent section.

Moreover, both the reduction of PWELL implantation energy—which increases the p-type doping concentration—and the decrease in LDD arsenic dose have been shown to negatively impact the $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ value while enhancing RFV_{MAX}. This



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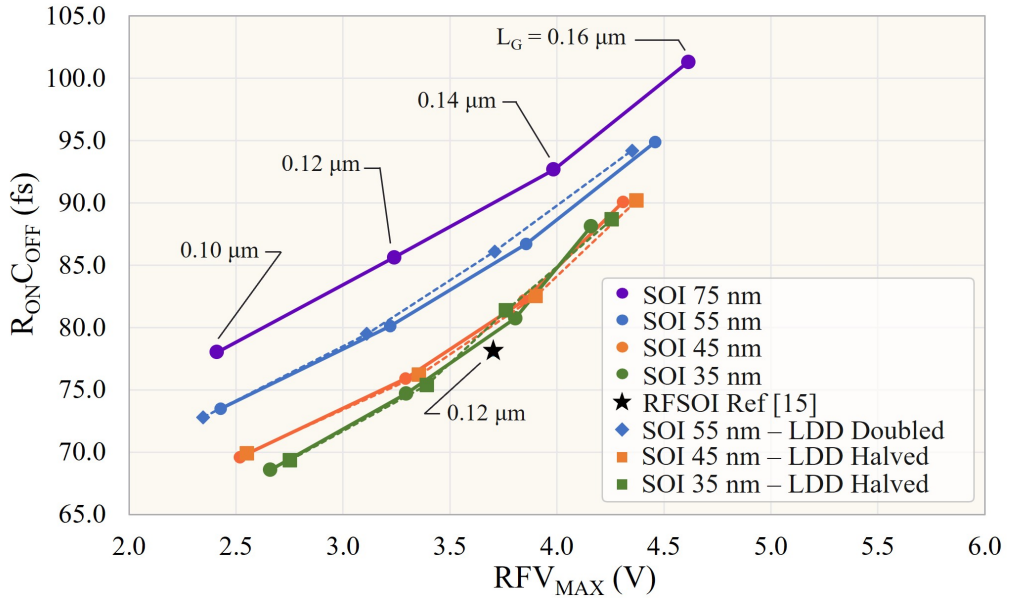


(b)

Fig. 2.15.: a) C_{OFF} vs R_{ON} and b) $R_{ON}C_{OFF}$ vs RFV_{MAX} graphs for devices fabricated on all four SOI substrates and by modifying the LDD implant dose. When the arsenic dose is doubled, C_{OFF} value slightly increases while maintenant an almost constant R_{ON}. The opposite trend occurs when the arsenic dose is halved, together with a small increase in RFV_{MAX}, due to the reduction of LDD overlap and hence of GIDL.

results in a consistent $R_{ON}C_{OFF}$-RFV_{MAX} ratio. However, for devices with L_G greater than 0.12 µm, this ratio actually decreases, as the improvement in power handling capability outpaces the degradation in $R_{ON}C_{OFF}$.

2.1.4 Breakdown Phenomena Analysis

To gain a clearer understanding of the contrasting behaviors in RFV_{MAX} between long and short channel devices with reduced t_{SOI}, it is necessary to examine the breakdown phenomena. Large-signal measurements, which are typically employed to determine RFV_{MAX}, did not yield significant insights. Consequently, we approached the issue from a DC perspective by studying the current flows in various devices prior to the onset of breakdown. This approach allowed us to identify the mechanisms responsible for DC breakdown and to recognize that certain mechanisms are more dominant in devices of specific sizes. It was subsequently found that the breakdown behavior in RF conditions is analogous to that in DC, with the addition of capacitive effects that are introduced by the high-frequency nature of the input signal, causing voltage fluctuations at different nodes within the device. The findings from this investigation are reported here.

DC breakdown measurements were performed on a range of devices by recording the current-voltage (I-V) characteristics as the drain current was varied under different gate voltage (V_{GS}) and bulk voltage (V_{BS}) conditions. During these measurements, we defined DCV_{MAX} as the maximum drain DC voltage that could be applied before a sharp increase in the drain current was observed. The forthcoming analysis will delve into the characteristics of both long and short channel devices, and it will be followed by an elucidation of the relationship between DC and RF breakdown phenomena.

Fig. 2.16a shows the DC I-V characteristics of the 75-nm SOI 0.16 µm device in Off-state conditions. A similar behavior is obtained for all devices with $L_G > 0.10$ µm. I-V curves are characterized by forcing a specific current value and measuring the corresponding V_{DS} value. Typically, a first smooth increase in drain current is observed, which depends on both V_{GS} and V_{BS}, followed by an exponential increase, which marks the device breakdown.

The inset of Fig. 2.16a illustrates that the initial current flow occurs between the drain and the body. For a constant gate voltage (V_{GS}), the magnitude of this current is influenced by the body voltage (V_{BS}), with an increase observed when a more negative V_{BS} is applied. Upon comparing data from multiple samples, it was noted that this segment of the current-voltage curves is also affected by the

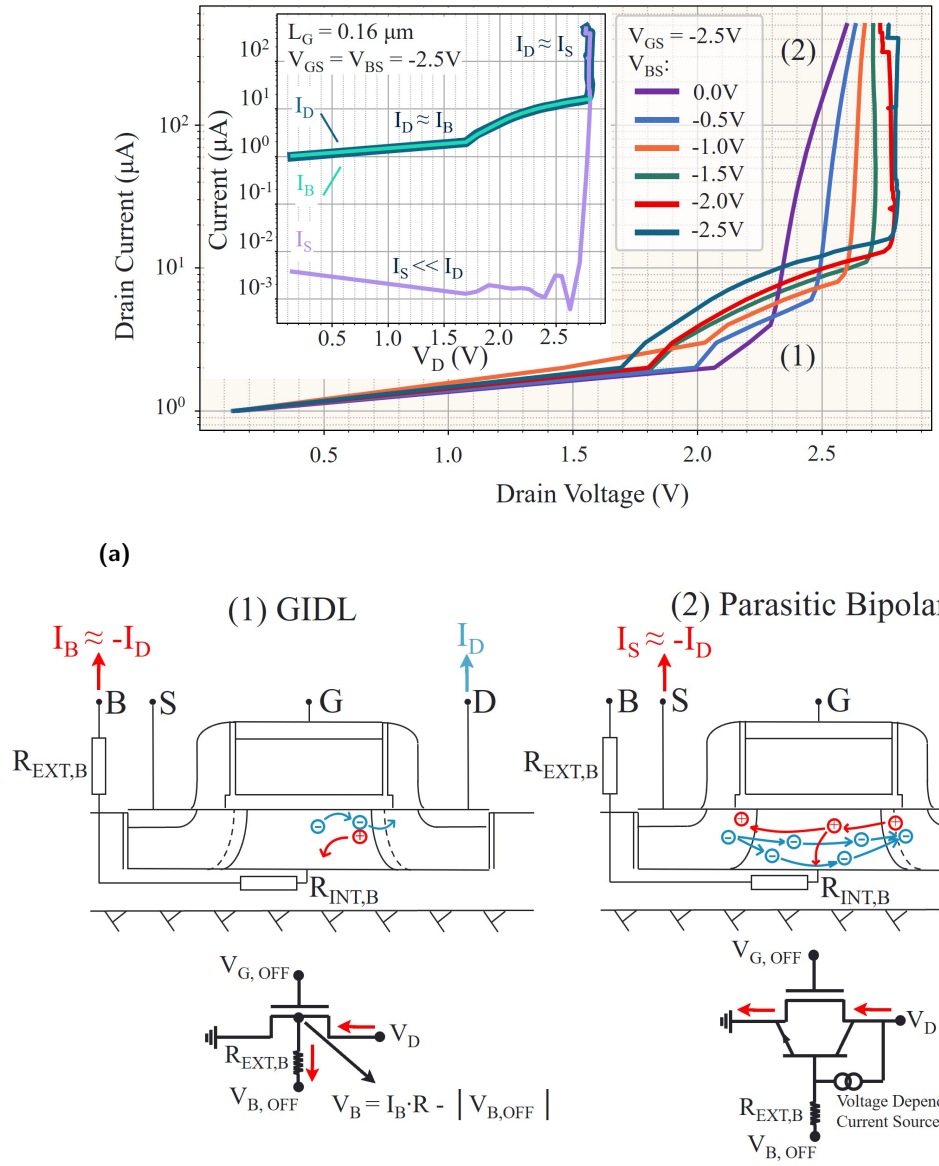


Fig. 2.16.: a) I-V characteristics of the 75-nm SOI 0.16 μm device in OFF-state conditions for V_{GS} and V_{BS} values specified in the legend. In insert, drain, source, and body currents are reported as a function of V_D showing that for these devices (1) GIDL and (2) parasitic bipolar opening are the two phenomena that occur. Indeed, initially current flows between drain and body, but at a certain V_D value I_S increases drastically and the circuit between source and drain is closed. In b) schematic views of how these two phenomena occur are represented.

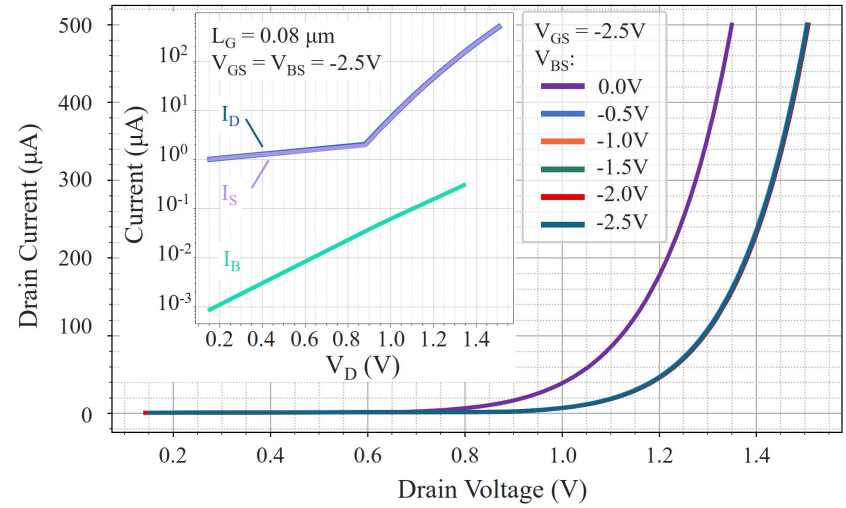
LDD arsenic dose. Specifically, a reduced arsenic dose leads to a lower current, whereas an increased dose results in a higher current. These observations point to Gate-Induced Drain Leakage (GIDL) as the source of the initial leakage current.

GIDL occurs due to the strong electric field at the drain junction of the MOSFET when a high negative gate bias is present. This negative gate bias causes the band structure of the pn junction to bend, facilitating the emission of minority carriers into the drain region beneath the gate through a Band-To-Band tunneling mechanism [17, 18]. The experimental results align with the understanding that a more heavily doped junction will more readily generate minority carriers. Once generated, electrons and holes are then swept towards the higher and the lowest potential, that is drain and body, respectively.

As the holes move toward the body contact, the internal body potential rises on account of the resistive path they encounter, which is the sum of the intrinsic body resistance ($R_{\mathrm{int,b}}$) and any external resistance ($R_{\mathrm{ext,b}}$) added to it (Fig. 2.16b). At this stage, the source current is minimal, but as the body potential approaches approximately +0.6 V, the source-body junction becomes forward-biased, and the parasitic NPN bipolar transistor is activated [19, 20, 21]. This results in the injection of electrons from the source (emitter) into the body (base) and their collection at the drain (collector), leading to a sharp increase in current as reflected in the I-V characteristics. The drain voltage (V_{DS}) at which this activation potential is reached is identified as DCV_{MAX}. Triggering of the bipolar transistor is characterized by the reduction of the measured V_{DS}, which leads to the "pull-back" signature of the I-V curve.

DCV_{MAX} is influenced by the t_{SOI} and the conditions of the PWELL implantation, similar to the dependency of RFV_{MAX} on these factors in long channel devices, as discussed in the previous section. The rationale behind this dependency is that breakdown is precipitated by the triggering of a parasitic bipolar transistor, which is reliant on the body resistance (R_{B}). R_{B} is affected by both the geometrical aspects, such as the SOI thickness, and the doping concentration.

In devices with a reduced t_{SOI}, $R_{\mathrm{int,b}}$ is believed to increase due to geometrical reasons, leading to a higher overall R_{B}. This means that a smaller current is required to elevate the body potential to the critical level of +0.6 V, thus necessitating a lower drain voltage (V_{DS}) to initiate the parasitic bipolar transistor. Conversely, when the PWELL implantation is performed with less energy, it results in a higher p-type doping concentration, which reduces $R_{\mathrm{int,b}}$ and therefore R_{B} as well. Consequently, a significantly larger current is necessary to raise the body potential to +0.6 V, which means that a higher V_{DS} is required for triggering the parasitic bipolar transistor.



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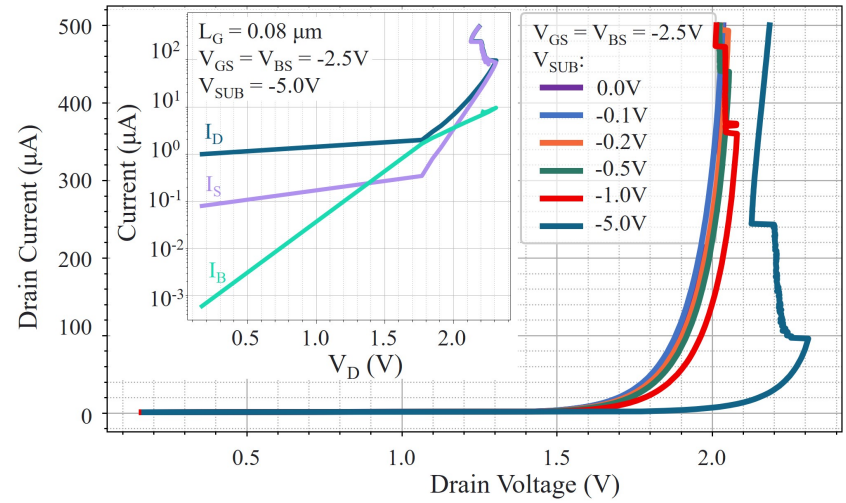


(b)

Fig. 2.17.: a) I-V characteristics of the 75-nm SOI 0.08 µm device in OFF-state conditions for V_{GS} and V_{BS} values specified in the legend. In insert, drain, source, and body currents are reported as a function of V_{DS} showing that for these devices (1) punch-through between source and drain occurs. b) For the same device, I-V characteristics while varying V_{SUB} are reported. At V_{SUB} = -5 V, GIDL and parasitic bipolar behaviors are restored.

In devices with a gate length (L_G) less than 0.1 µm, it has been observed that leakage current primarily flows between the drain and source even at low drain voltages, with the body current being relatively insignificant in comparison (Fig. 2.17a). These devices do not exhibit a sharp increase in drain current under any combination of V_{GS} and V_{BS} bias. Nevertheless, when a negative voltage is applied to the chuck contact of the probe station, simulating a back-biasing condition, the current-voltage (I-V) characteristics begin to mirror those seen in devices with L_G > 0.10 µm (Fig. 2.17b). For devices with L_G = 0.08 µm, the behavior typical of long-channel devices is reinstated at a back-bias, or substrate voltage, V_{SUB}, of -5 V, while for L_G = 0.06 µm (not illustrated here), a V_{SUB} of -30 V is required.

In these shorter-channel devices, a punch-through mechanism is identified, where electrons move directly from source to drain due to the reduced barrier potential in the body [22, 23, 24]. This reduction is a result of the significant overlap of the depletion regions from both junctions. As V_{DS} increases, the barrier potential further diminishes, leading to an increase in the drain-source current (I_{DS}). However, when a negative back-bias is applied, the barrier potential is reinstated, and the Gate-Induced Drain Leakage (GIDL)/NPN bipolar triggering mechanism becomes predominant again.

For devices with L_G = 0.10 µm, the OFF-state I-V characteristics resemble those of devices with L_G > 0.10 µm, but there is a gradual increase in source current even before the bipolar transistor is activated (Fig. 2.18). These devices represent

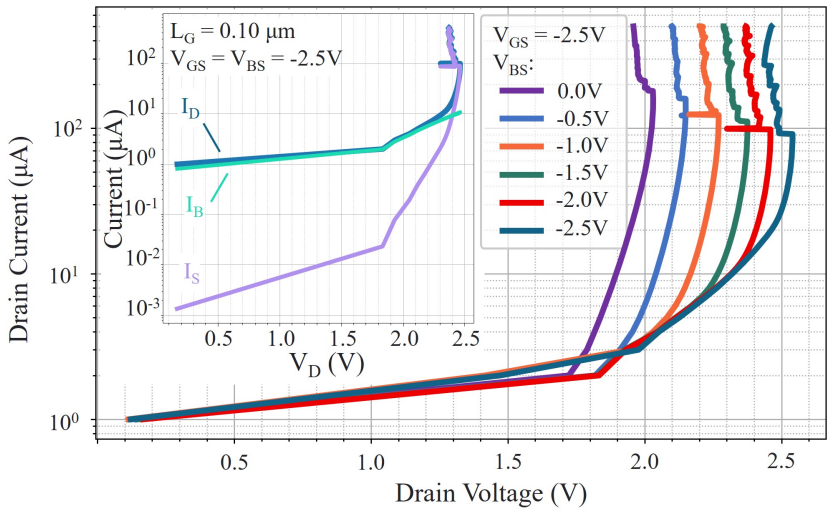


Fig. 2.18.: I-V characteristics of the 75-nm SOI 0.10 µm device in OFF-state conditions for V_{GS} and V_{BS} values specified in the legend. In these devices, a combination of GIDL, parasitic bipolar, and punch-through occurs, as reported in the insert.

an intermediate stage between the GIDL/NPN triggering and the punch-through mechanisms, with both competing to influence the breakdown event.

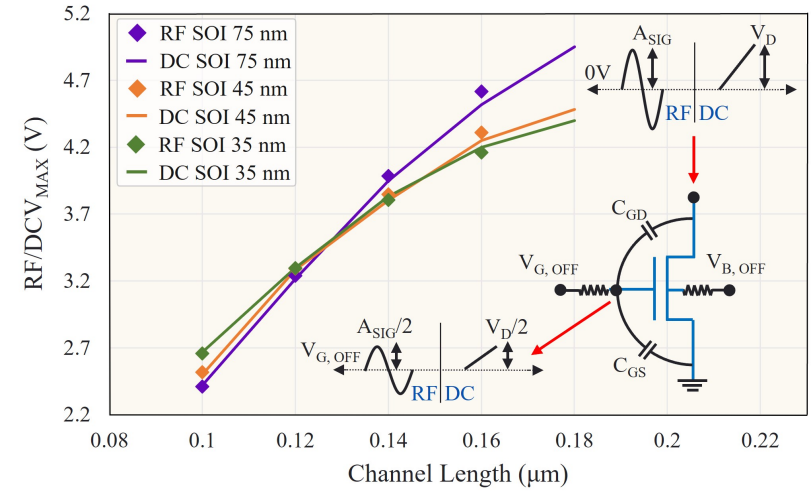
It is important to note that punch-through is associated with Short Channel Effects, which typically reduce the potential barrier between the source and drain [25]. However, as previously mentioned, devices with thin SOI layers have shown a reduction in SCE, meaning that the body barrier potential is less affected by the drain junction's depletion region, resulting in an increased barrier height. Consequently, punch-through is effectively suppressed, and the GIDL/NPN bipolar triggering mechanism prevails, leading to a higher DCV_{MAX}.

The DC breakdown analysis described was conducted with V_{GS} and V_{BS} set to Off-state conditions. Although changes in t_{SOI} or implantation parameters affect DCV_{MAX} in a manner similar to RFV_{MAX}, the breakdown voltages measured in DC are lower than those obtained in large-signal RF tests. For instance, the RFV_{MAX} for a 0.16 µm device on 75-nm SOI is 4.6 V (Fig. 4.4), whereas the DCV_{MAX} does not exceed 2.8 V (Fig. 2.16a), indicating additional phenomena at play in RF conditions.

To accurately replicate the RF breakdown values, it is necessary to account for the 'floating gate effect' [26, 27, 28]. This effect arises from the high external gate resistance ($R_{\mathrm{ext,b}}$), which allows V_{GS} at the gate node to fluctuate instead of being fixed at -2.5 V when an RF signal is applied to the drain. Two capacitors, represented by the gate-to-drain and gate-to-source capacitances (C_{GD} and C_{GS}), form a capacitive voltage divider. Consequently, for an input signal amplitude (A_{SIG}), V_{GS} varies by $A_{\mathrm{SIG}}/2$.

To incorporate this effect into a DC I-V breakdown measurement, the initial Off-state conditions are set, and then both the drain and gate voltages are swept simultaneously to V_{DS} and $V_{\mathrm{DS}}/2$, respectively. Using this setup, Gate-Induced Drain Leakage (GIDL) is diminished due to the increased V_{GS}, which reduces the hole current through the body and postpones the triggering of the NPN bipolar transistor. Breakdown measurements employing this method have shown that DCV_{MAX} aligns precisely with RFV_{MAX} for all devices studied, confirming that the significant increase in harmonics is indeed caused by the activation of the parasitic bipolar transistor [29] (Fig. 2.19).

This finding is a significant breakthrough in the study of breakdown in RF switch devices, demonstrating that their power handling capacity is entirely dependent on electrostatic phenomena that can also be observed in DC conditions. GIDL, NPN bipolar triggering, and punch-through are the principal factors leading to the loss of



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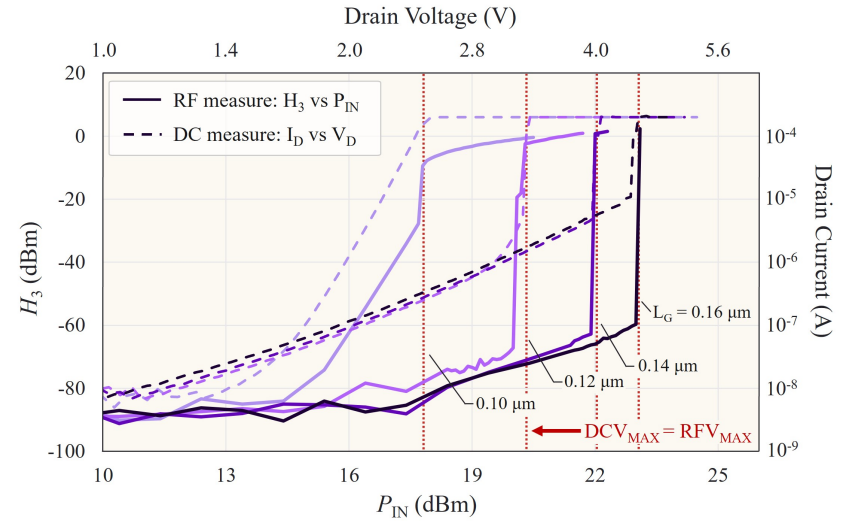


(b)

Fig. 2.19.: a) The data obtained by extracting RFV_{MAX} from the power measurement and by extracting DCV_{MAX} with the I-V measurement applying the floating gate effect are compared in the figure. The insert shows how this effect works: given the high resistance applied to the gate, a floating point is created which varies in value based on the input RF signal, precisely by $A_{\mathrm{SIG}}/2$ due to the presence of the capacitive divider C_{GD}-C_{GS} . To mimic this effect in DC, as the drain voltage varies, a change in gate voltage equal to $V_{\mathrm{DS}}/2$ must be applied. Figure b) shows the perfect correlation between the drastic increase of the H2 harmonic considered as the RFV_{MAX} point (solid line) and the drastic increase of the drain current, considered as the DCV_{MAX} point (dashed line).

linearity in the devices and ultimately causing the drastic increase in harmonics, thus determining RFV_{MAX} . These phenomena are influenced by numerous variables, including the device's size and geometry, doping profiles, and applied voltages. Moreover, the development of a method to study RFV_{MAX} using straightforward DC measurements is a crucial advancement for the future progression of these devices. It offers the ability to test this characteristic during the processing phase, thereby allowing for the rapid and effective evaluation of the impact of process flow changes on the power-handling capabilities.

In conclusion, RFV_{MAX} is linked to three leakage phenomena (GIDL, parasitic bipolar, and punc- through), and hence its value can be increased by (1) reducing GIDL and body current, (2) reducing body resistance R_{B}, and (3) improving electrostatic control.

2.1.5 Summary of Results and Prospects

The Thin SOI project aimed to investigate the impact of reducing the thickness of the SOI layer on the performance of transistor devices for RF switch applications. This evaluation focused on analyzing the changes in the $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ product and power handling through the RFV_{MAX} parameter.

By modifying the manufacturing process, we successfully introduced SOI thinning steps to reduce the standard thickness from 75 nm to 45 nm and 35 nm. This adaptation required adjustments, particularly in the formation of the silicide and the PWELL implantation energies, to prevent excessive reduction in doping concentration, which would adversely affect the threshold voltage and power handling capabilities.

The RF results demonstrated a significant reduction in parasitic capacitance C_{OFF} with decreasing t_{SOI} thickness, while maintaining similar R_{ON} values to standard samples. This reduction, attributed to decreased inner fringing capacitance between the gate contact and the source/drain junctions, led to a lower $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ product. Notably, record values of 68 fs and 74 fs were achieved for devices with $L_{\mathrm{G}} = 0.10$ µm and 0.12 µm on substrates with a nominal SOI of 35 nm, surpassing the previous state-of-the-art value of 78 fs for devices with a gate length of 0.12 µm fabricated with competing technology. However, the reduction in t_{SOI} thickness also resulted in decreased power handling, as indicated by the RFV_{MAX} value, but only for long-channel transistors ($L_{\mathrm{G}} > 0.12$ µm). This is due to increased intrinsic body resistance from reduced dopant concentration, leading to easier activation of the parasitic bipolar formed by the body/contact junctions. Conversely, for

short-channel devices ($L_G \leq 0.12$ µm), the t_{SOI} reduction was beneficial, enhancing RFV_{MAX} due to improved electrostatic control of the channel and reduced 'quasi' punch-through phenomena.

In summary, while reducing t_{SOI} consistently improved the $R_{ON}C_{OFF}$ product within the studied thickness range, the enhancement of RFV_{MAX} depended on the physical characteristics of the devices, particularly channel size. This observation stems from the complex nature of breakdown in RF switch devices, influenced by GIDL, parasitic bipolar activation, and punch-through phenomena. Improved control over these factors leads to increased RFV_{MAX} and power handling. For GIDL, optimizing the LDD to reduce gate overlap and silicon band bending is crucial. For parasitic bipolar and punch-through, optimizing body doping to reduce intrinsic resistance and increase the potential barrier between source and drain is essential.

The results presented provide a solid foundation for future studies aimed at exploring the limits of the Thin SOI approach in enhancing RF switch device performance, primarily through further SOI thickness reduction. While the current results show a progressive reduction in parasitic capacitance C_{IF}, it remains to be seen how far this improvement can continue. Additionally, the increase in RFV_{MAX} for short-channel devices with reduced t_{SOI} marks a significant breakthrough for RF switch applications, suggesting the feasibility of using transistors with reduced L_G without compromising power handling. Future research should focus on optimizing PWELL implantations for each new SOI thickness to potentially recover the electrostatic properties of standard devices even for small t_{SOI} and mitigate RFV_{MAX} degradation in long-channel devices due to increased body resistance. A proposed solution is the use of a highly doped thin layer at the interface with the BOx, potentially created through epitaxy, to effectively evacuate holes toward the body pad and delay parasitic bipolar activation. These proposals are not only feasible but also promise to bring a comprehensive conclusion to the work presented in this thesis.

References

[1] S. Crémer et al. "40-nm RFSOI technology exhibiting 90fs $R_{ON}C_{OFF}$ and f_T/f_{MAX} of 250 GHz/350 GHz targeting sub-6 GHz and mmW 5G applications". In: *IEEE 53rd European Solid-State Device Research Conference (ESSDERC)* (2023).

[2] P. Chevalier et al. "PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications". In: *2020 IEEE International Electron Devices Meeting (IEDM)* (2020), pp. 34.4.1–34.4.4.

[3] F. Rozé et al. “Oxidation kinetics of Si and SiGe by dry rapid thermal oxidation, in-situ steam generation oxidation and dry furnace oxidation”. In: *Journal of Applied Physics* (2017), pp. 245308.1–245308.10.

[4] B. E. Deal and A. S. Grove. “General Relationship for the Thermal Oxidation of Silicon”. In: *Journal of Applied Physics* (1963), pp. 3770–3778.

[5] M. Langenbuch et al. “In situ steam generation (ISSG) versus standard steam technology: impact on oxide reliability”. In: *Microelectronics Reliability* (2005), pp. 875–878.

[6] A. Ludsteck et al. “Growth model for thin oxides and oxide optimization”. In: *Journal of Applied Physics* (2004), pp. 2827–2831.

[7] I. Blum et al. “Diffusion and redistribution of boron in nickel silicides”. In: *Defect and Diffusion Forum* (2012), pp. 415–420.

[8] Y.L. Jiang et al. “Dopant Redistribution Induced by Ni Silicidation at 300°C”. In: *The Fourth International Workshop on Junction Technology, 2004. IWJT ’04* (2004), pp. 139–142.

[9] S. M. Sze. *Physics of Semiconductor Devices*. J. Wiley and Sons, 1981.

[10] J. P. Colinge. *Silicon-On-Insulator Technology: Materials to VLSI, 3rd Edition*. th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2004.

[11] D. Hisamoto et al. “A fully depleted lean-channel transistor (DELTA)-a novel vertical ultrathin SOI MOSFET”. In: *IEEE Electron Device Letters* (1990), pp. 36–38.

[12] K. K. Young. “Short-channel effect in fully depleted SOI MOSFETs”. In: *IEEE Transactions on Electron Devices* (1989), pp. 3399–402.

[13] S. R. Banna et al. “Threshold voltage model for deep-submicrometer fully depleted SOI MOSFET’s”. In: *IEEE Transactions on Electron Devices* (1995), pp. 1949–1955.

[14] 2020 Sentaurus Process/Device User Manual Synopsys. In: ().

[15] G. Hiblot et al. “Refined conformal mapping model for MOSFET parasitic capacitances based on elliptic integrals”. In: *IEEE Transactions on Electron Devices* (2015), pp. 972–979.

[16] F. Gianesello et al. “Advanced 200-mm RF SOI technology exhibiting 78 fs RON x COFF and 3.7 V breakdown voltage targeting sub 6 GHz 5G FEM”. In: *IEEE Radio Frequency Integrated Circuits Symposium* (2022), pp. 191–194.

[17] L. Huang et al. “Mechanism analysis of gate-induced drain leakage in off-state n-MOSFET”. In: *Microelectronics Reliability* (1998), pp. 1425–1431.

[18] R. Inagaki et al. “A GIDL-Current Model for Advanced MOSFET Technologies Implemented into HiSIM2”. In: *2007 International Conference on Communications, Circuits and Systems* (2007), pp. 1057–1061.

[19] W. Muller et al. “Short-Channel MOS Transistors in the Avalanche-Multiplication Regime”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (1982), pp. 1778–1784.

[20] E. Sun et al. “Breakdown mechanism in short-channel MOS transistor”. In: *1978 International Electron Devices Meeting* (1978), pp. 478–482.

[21] E. P. Ver Ploeg et al. “Parasitic Bipplar Gain in Fully Depleted n-Channel SO1 MOSFET’s”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (1994), pp. 970–977.

[22] B. Eitan et al. “Surface conduction in short-channel MOS devices as a limitation to VLSI scaling”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (1982), pp. 254–266.

[23] F.C. Hsu et al. “A Simple Punchthrough Model for Short-Channel MOSFET‘s”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (1983), pp. 1354–1359.

[24] J.J. Barnes et al. “Short-Channel MOSFET’S in the Punchthrough Current Mode”. In: *IEEE JOURNAL OF SOLID-STATE CIRCUITS* (1979), pp. 368–375.

[25] R. R. Troutman. “VLSI limitations from drain-induced barrier lowering”. In: *IEEE Journal of Solid-State Circuits* (1979), pp. 3383–3391.

[26] M. Ahn et al. “A High-Power CMOS Switch Using A Novel Adaptive Voltage Swing Distribution Method in Multistack FETs”. In: *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES* (2008), pp. 849–858.

[27] M. Ahn et al. “A Novel Multi-Stack Device Structure and its Analysis for High Power CMOS Switch Design”. In: *2007 IEEE/MTT-S International Microwave Symposium* (2007), pp. 1393–1396.

[28] M. Ahn et al. “A High Power CMOS Switch Using Substrate Body Switching in Multistack Structure”. In: *IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS* (2007), pp. 682–684.

[29] D. Im et al. “Characterization and optimization of partially depleted SOI MOSFETs for high power RF switch applications”. In: *Solid-State Electronics* (2013), pp. 94–98.

3

Strained SOI Project

Enhancing the transconductance of a transistor is a direct route to improve its performance in low-noise amplifier (LNA) applications. This is because the transconductance is closely linked to the transistor's cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}, cf. Appendix B). One effective way to increase transconductance is by improving carrier mobility. This can be achieved by deliberately introducing mechanical strain to the conductive channel. Such strain alters the semiconductor's band structure, affecting not just the band gap but also the population density of the bands and the carriers' effective mass. For NMOS transistors, applying tensile stress along the channel can significantly increase electron mobility. Specifically, a 1 % tensile strain along the <100> direction of the silicon lattice can result in a 40 % increase in mobility. This improvement rises to 70 % when the strain is oriented along the <110> direction and reaches 80% with biaxial strain [1, 2, 3, 4] (cf. Appendix B). Industrially, there are various established methods for enhancing transistor performance, broadly categorized into 'global stressor techniques' and 'local capping-film techniques'. Global stressor techniques involve using a buffer layer, like SiGe, beneath the silicon layer, which introduces uniform stress across the entire wafer. These techniques are highly effective; however, they impose the same stress—either tensile or compressive—on both NMOS and PMOS transistors, adversely affecting the performance of one of the two transistor types[5, 6, 7]. In contrast, local techniques, such as the Stress Memorization Technique (SMT) and Contact Etch Stop Layer (CESL), target specific devices for stress application [8, 9, 10, 11, 12, 13]. The downside is that these techniques are constrained by the physical geometry and mechanical strength of the materials, which limits the amount of stress that can be applied (cf. Chapter 4).

In light of these considerations, we have developed an innovative stressor technique that utilizes SiGe in a unique way to induce substantial stress in the NMOS transistors of our CMOS65SOIMMW technology. This method has been termed the 'Localized SiGe Stressor Technique'. The process unfolds as follows (Fig. 3.1):

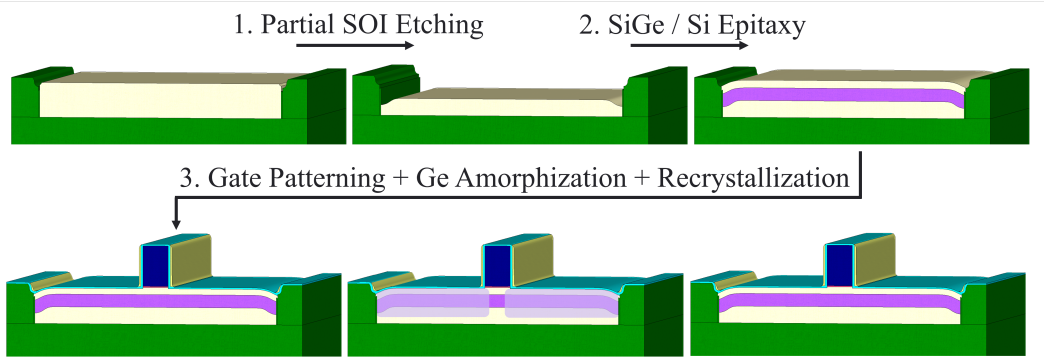


Fig. 3.1.: The process flow of the Localized SiGe Stressor Technique is schematically reported. It mainly consists on three steps: (1) SOI is partially etched after the STI brick for then (2) growing by epitaxy an SiGe / Si stack. At this point, SiGe is to consider pseudomorphic, as it assumes the lattice parameter of the SOI below, and hence compressively strained, while the top Si is completely relaxed. (3) After the gate patterning brick, Ge implantation is used to amorphize the SOI / SiGe / Si structure up to the SOI. In this way, SiGe is free to relax and stretches the silicon on top, thus introducing a tensile strain. A recrystallization step is then conducted to recover the initial crystal order.

1. After the Shallow Trench Isolation (STI) process, the Silicon-On-Insulator (SOI) is selectively and partially etched away in the active region of the NMOS devices.

2. Subsequently, a SiGe / Si bilayer is epitaxially grown at thicknesses sufficiently small so that no defect is expected to form, resulting in a layered structure of Buried Oxide (BOx) / Si / SiGe / Si. Initially, the SiGe layer is under compressive strain due to the difference in lattice parameters, while the Si layers above and below remain strain-free.

3. Following the gate structure formation, Ge ion implantation is employed to amorphize the Si / SiGe / Si configuration adjacent to the NMOS transistor's channel. This disrupts the crystalline structure's rigidity, allowing the SiGe layer to relax. This relaxation process imparts tensile strain to the upper Si layer. The amorphized regions are then recrystallized to restore the crystalline structure.

Achieving full relaxation of the SiGe layer is expected to result in a strain value ranging from 0.8 % to 1 %, depending on the germanium content. This could theoretically lead to a 40 % enhancement in mobility, transconductance, and cutoff frequency, all while not adversely affecting PMOS device performance [1]. Such an advancement would significantly bolster the overall capabilities of our CMOS65SOIMMW 40-nm Partially Depleted Silicon-On-Insulator (PDSOI) technology, which incorporates

Low Noise Amplifiers, Power Amplifiers, RF switches, and digital components on a single chip, offering a highly comprehensive and competitive solution [14, 15].

This chapter details the outcomes of the Strained SOI project. The majority of these outcomes pertain to process integration and computational analysis, as the project's primary aim was to incorporate this innovative technique into the standard CMOS65SOIMMW process—a challenging endeavor due to the multitude of parameters and processing steps that must be managed to yield functional devices. The initial section is devoted to introducing the preliminary short-loop tests, which served as a proof of concept for the technique and subsequent investigations into stress transfer from SiGe to Si. The methods used to fabricate the samples and the results of strain measurements will be discussed, along with computational models that provide a deeper understanding of the findings. In particular, it will be seen that the significant contribution of strain within the silicon channel is due to two coexisting phenomena: (1) the relaxation of the SiGe layer and (2) the formation of dislocations at the side of the channel. The second section addresses process challenges, such as germanium diffusion out of SiGe and lateral diffusion of source/drain (S/D) dopants, and demonstrates how these issues were resolved. The final part of the chapter presents the electrical data for the manufactured devices, divided in Parametric Test (PT) and Radio Frequency (RF) results, which necessitated the consideration of all the analyses and optimizations discussed earlier. To wrap up, a concise summary will be provided, along with suggestions for future research directions that aim to broaden the project's impact and support the continued development of innovative devices.

3.1 Proof of Concept Tests of the Localized SiGe Stressor Technique

Following the design of the Localized SiGe Stressor Technique, the next step was to verify that the idea worked effectively by introducing a high amount of strain within the silicon channel. To verify it, a first stress transfer test on a blanket wafer has been carried out.

For this experiment, dummy gates of polysilicon with a gate length (L_G) of 35 nm were constructed on a stack consisting of Buried Oxide (BOx) / 15 nm SOI / 50 nm SiGe with 20 % Ge content / 15 nm Si (Fig. 3.2). The sample preparation process began with a selective chemical etching of the standard SOI, followed by two epitaxial growth steps to form the SiGe and Si layers. An optimized process

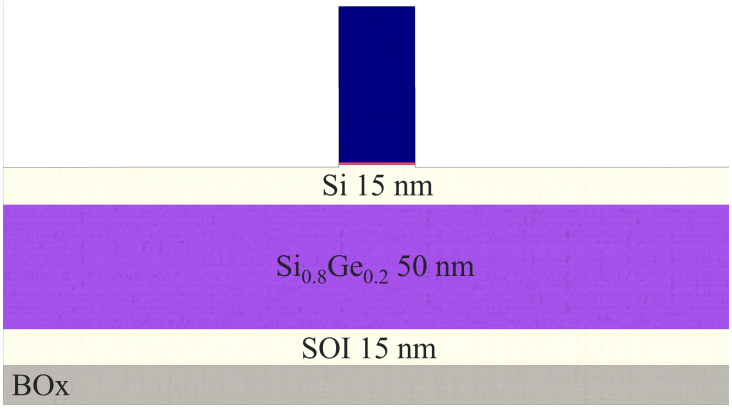


Fig. 3.2.: Schematic representation of the 15 nm SOI / 50 nm SiGe with 20 % Ge content / 15 nm Si structure on which the effectiveness of the Localized SiGe Stressor Technique was tested to induce high amounts of strain within the Si layer.

with a gas chemistry of SiH_2Cl_2 + GeH_4 + HCl was employed to grow the SiGe 20 % / Si stack preventing the relaxation of elastic strain and the emergence of surface undulations on the SiGe during temperature ramps. The resulting final stack composition was measured to be BOx / 18 nm SOI / 45 nm $Si_{0.8}Ge_{0.2}$ / 15 nm Si, which was sufficiently close to the intended specifications. The dummy gates were created using the standard CMOS65SOIMMW process. After their construction, we proceeded to amorphize the structure until inside the bottom Si layer through germanium ion implantation at energy of 50 keV and dose of 2e15 cm^{-2}. This step was followed by a recrystallization process, which involved heating the samples to 600 °C for 120 seconds. The optimal amorphization conditions were previously determined. Indeed, various Ge implant energies were tested on samples with the same stack of the first stress transfer test, aiming to achieve different amorphization depths. As reported by High-Resolution X-Ray Diffraction (HRXRD) analysis in Fig. 3.3, the crystal structure was found to be well-ordered after recrystallization when the amorphization extended into the bottom silicon layer rather than stopping within the SiGe layer. Additionally, a preliminary analysis of strain content obtained from the Reciprocal Space Maps (RSMs) showed that the SiGe layer was almost completely relaxed under these conditions (Fig. 3.3a).

To properly analyze the structure's strain profile of the proof-of-concept test following the amorphization and recrystallization steps we utilized Precession Electron Diffraction (PED) measurements. PED is an advanced technique for acquiring electron diffraction patterns within a Transmission Electron Microscope (TEM) [16] (Fig. 3.4). By comparing the diffraction pattern of an under-analysis structure with that of a non-strained silicon reference, one can extract the strain content carthography of the structure. PED has advantages over other electron diffraction methods

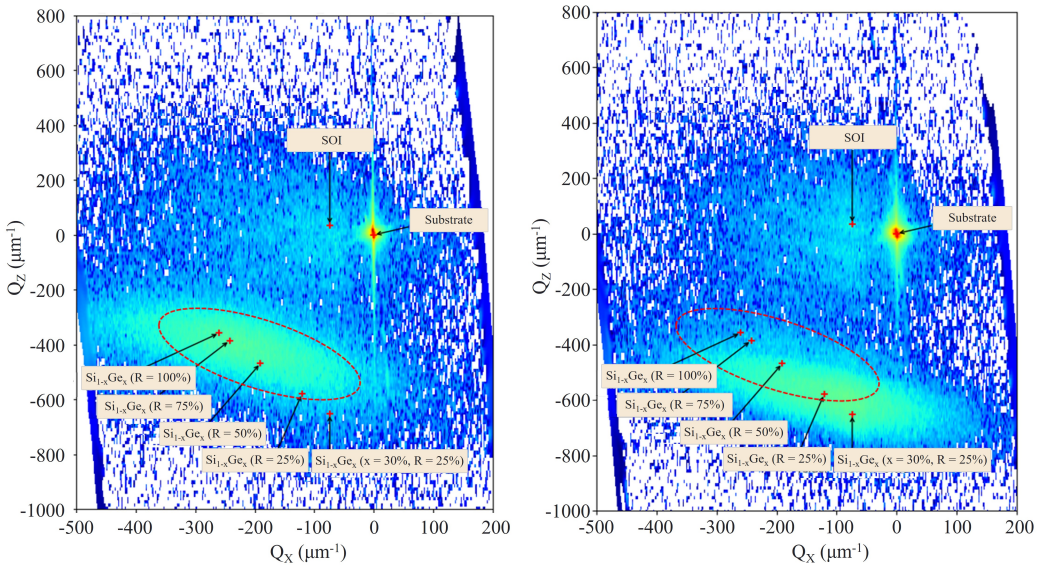


Fig. 3.3.: HRXRD characterization after the amorphization/recrystallization step conducted by means of two implant conditions: a) high implant energy for amorphizing up to the inside of SOI; b) low implant energy for amorphizing up to the inside of SiGe. In both graphs the substrate signal as well as the SOI signal are visible. The expected positions of the SiGe signal at different relaxation percentages are also reported. The comparison of the two images shows that a more relaxed SiGe can be obtained when amorphization occurs up to the SOI (a).

due to its increased sensitivity to minor experimental variations. The averaging effect of multiple incident beam directions means that the resulting patterns are less affected by small misalignments between the zone axis and the microscope's optic axis, preserving the symmetry of the zone axis in the patterns. Additionally, PED patterns are less influenced by the sample's thickness—a factor that can significantly affect standard electron diffraction patterns. Furthermore, PED offers the benefit of analyzing much smaller samples compared to X-ray diffraction, which typically requires single crystals to be at least approximately 5 µm in size. Hence, with electron-based methods like PED, it is possible to probe samples that are significantly smaller.

Therefore, PED is an effective tool for examining the strain within a structure by contrasting its diffraction pattern against that of a known reference, such as the silicon substrate beneath the BOx. By employing this method, we have been able to create a detailed map of the strain distribution within the SOI / SiGe / Si structure after undergoing the amorphization and recrystallization processes. This mapping includes the strain matrix elements ε_{xx} and ε_{yy}, that we denoted as the 'in-plane strain' and the 'out-of-plane strain', represented the strain parallel and

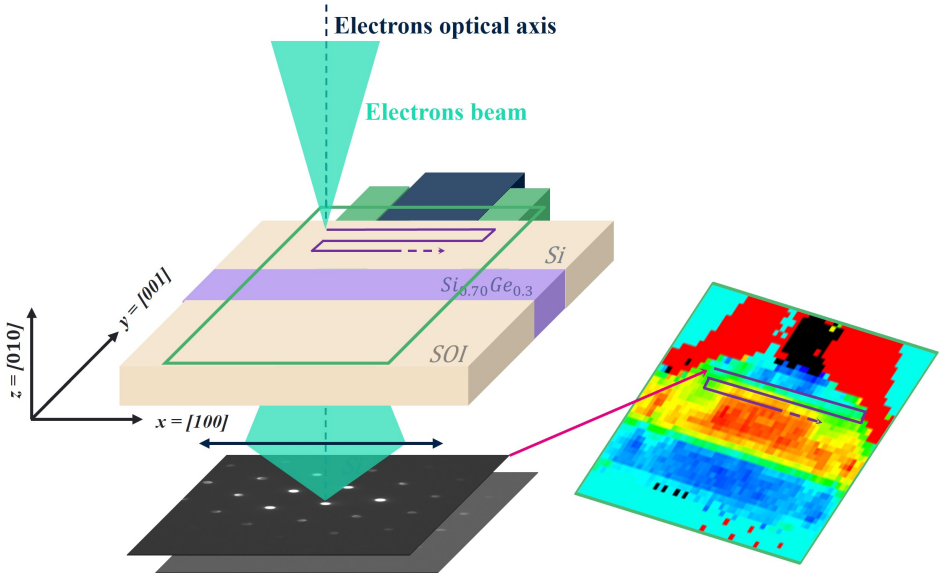


Fig. 3.4.: The operating principle of the PED measurement is schematically reported. The studied structure is scanned by an electron beam with a certain vertical and horizontal step. At each measurement point, the beam is made to precede around the optical axis and the resulting diffraction pattern is collected. The comparison of the pattern thus obtained with the diffraction measurement of a non-stressed reference sample results in a pixel with a certain strain value. The set of all pixels provides a complete cartography of the amount of strain inside the structure.

perpendicular to the channel orientation, respectively. The findings are illustrated in figure 3.5, which also presents the ε_{xx} and ε_{yy} values obtained along a vertical line under a dummy gate.

Within the SiGe layer, both the in-plane strain and the out-of-plane strain are observed to reach a nearly identical value of approximately 1.2 %, particularly near the interface between the top Si layer and the SiGe. This indicates that the lattice parameters of the SiGe cubic cell in both directions are almost equal. However, this also implies that the SiGe has not fully relaxed, as the measured strain values are below the theoretical 1.5 %, which is the expected value for a completely relaxed SiGe layer with a 20 % Ge content relative to the lattice parameter of the silicon reference [17]. Conversely, at the interface between SiGe and the SOI, ε_{xx} and ε_{yy} exhibit distinct behaviors: ε_{yy} increases while ε_{xx} diminishes, eventually aligning with the value found in the SOI. This suggests that the SiGe is still constrained by the lattice parameter of the underlying SOI. This behavior aligns with expectations, as elastic relaxation typically occurs where there are no constraints—in this case, at the edges of the structure where amorphization has taken place. In contrast, the area of the SOI beneath the dummy gate was not subjected to Ge implantation, and thus its mechanical properties remain unchanged. As a result, the SiGe layer in

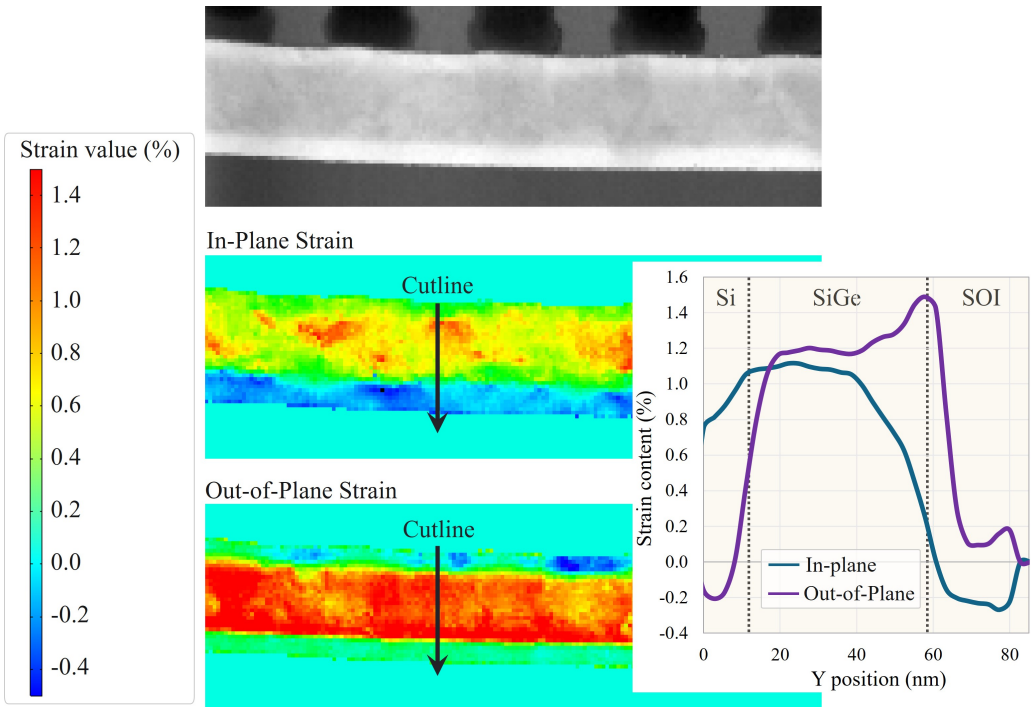


Fig. 3.5.: The PED result of the proof-of-concept test is here reported. From top to bottom, the High-Angle Annular Dark-Field (HAADF) image of the sample with dummy gates on blanket wafer and the in-plane and out-of-plane strain cartographies are shown, respectively. On the right, both strain profiles as a function of the vertical position are reported, obtained along the cutline highlighted.

this region cannot relax and is forced to retain the same lattice parameter as the SOI. The relaxation of the SiGe layer has effectively caused the tensile stretching of the overlying Si layer, as indicated by the PED measurements. At the interface between Si and SiGe, ε_{xx} shows a positive strain value of 1.0 %, which then slightly decreases to 0.8 % closer to the dummy gate, likely due to its restrictive influence. These observations provide evidence that this novel method has the potential to introduce a significant amount of strain into the silicon channel.

A more detailed examination of the PED data suggests that, in addition to the SiGe relaxation, other processes have occurred during the fabrication steps. Specifically, the presence of negative strain values for the out-of-plane and in-plane strains in the Si and SOI layers, respectively, cannot be solely attributed to elastic relaxation. This implies that there are additional factors at play influencing the strain distribution within the structure.

High-Resolution Transmission Electron Microscopy (HRTEM) images have shown the presence of stacking faults (SFs) on either side of the channel following the recrystallization process (Fig. 3.6). Recognizing that such defects can serve as

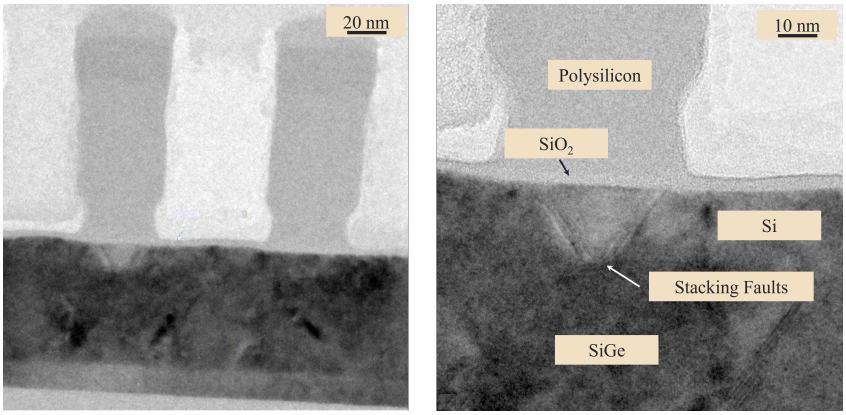


Fig. 3.6.: Partial HRTEM image of the proof-of-concept sample is shown (left) together with a zoom (right) detailing the area below the dummy gate. The images clearly show the presence of stacking faults.

sources of stress, generating both tensile and compressive stresses within an elastic material simultaneously, we have suspected that these defects might also play a role in the final strain values that were experimentally observed.

To test this hypothesis, an experiment was designed with the objective of creating stacking faults without causing SiGe relaxation. The initial step involved determining the specific conditions under which SFs form during the amorphization and recrystallization processes. A valuable resource for monitoring the formation of SFs and for computational replication is the fully atomistic model provided by Sentaurus Synopsys [18], which employs Lattice Kinetic Monte Carlo (LKMC) simulations. The LKMC method is a recognized technique for examining the Solid-Phase Epitaxy Regrowth (SPER) of a material during recrystallization, as it accounts for the influence of regrowth direction, dopant concentrations, and strain on the SPER velocity [19, 20, 21].

Initially, LKMC was utilized to replicate the SFs observed in the first short-loop test, confirming its capability to yield reliable results. The experimental structure was modeled in Sentaurus, and the same amorphization and recrystallization conditions used in the experiment were reproduced in the simulation. The lateral images in Fig. 3.7 show that the structure was actually fully amorphized up to the SOI layer due to the implantation energies used, which laterally extended the two amorphized zones on either side of the gate until they merged. However, a small unamorphized portion of the top Si layer beneath the gate was still present. To gain a clearer understanding of the recrystallization front movements, snapshots of the amorphous-crystalline interfaces were taken every 12 seconds and then superimposed onto a single image. This method produced the map shown in Fig. 3.7. At first, the main recrystallization

front is the horizontal one moving vertically towards device's surface. It was most likely this movement of the front that caused the SiGe to initially recrystallize with the crystalline parameter of silicon, and then secondly yield to elastic relaxation, thus acquiring an almost standard lattice parameter ($\varepsilon_{xx} \approx 1.5$ % in Fig. 3.5). However, at 60 seconds the recrystallization began to proceed in multiple directions as the vertical and horizontal fronts (coming from the small unamorphized portion of the top Si) converged. The recrystallization continued to advance towards the surface until full recrystallization was obtained after 120 seconds. According to Shen et al. [22], SFs are expected to form when the angle between the horizontal and vertical recrystallization fronts is less than 90 degrees. By observing Fig. 3.7, acute angles are spotted starting from $t = 60$ s where the vertical and horizontal fronts merge, possibly being two points where SFs could form. By comparing the simulation results (Fig. 3.7) to HRTEM observations (Fig. 3.6), these points are found to be located exactly where defects have been observed experimentally. This feature seems to prove that TCAD simulations successfully replicated the formation

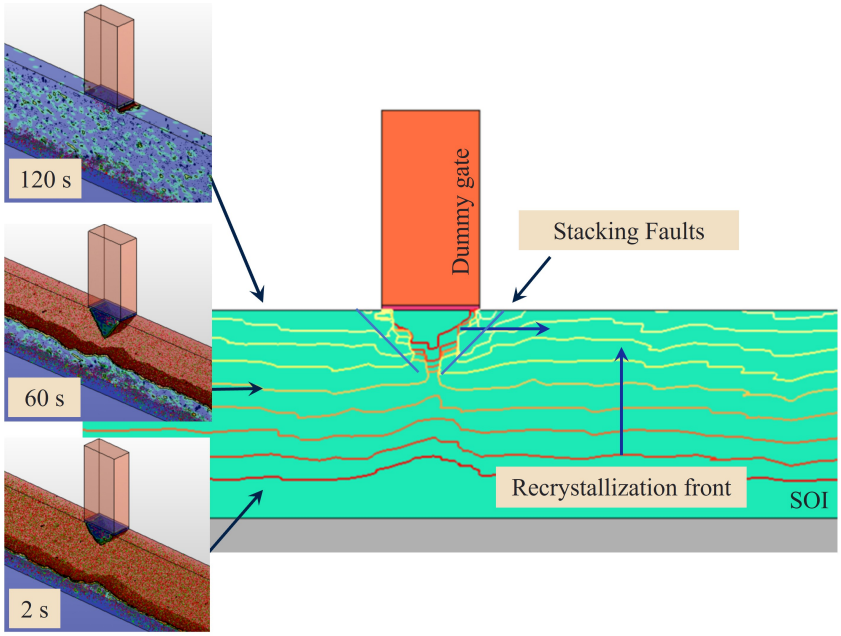


Fig. 3.7.: The results obtained from the LKMC simulations of the proof-of-concept sample are shown here. These simulations were intended to reproduce the SPER event in the samples after amorphization, as reported by the three snapshots at the top obtained at $t = 2$ s, 60 s, and 120 s, respectively. The superposition of the crystal-amorphous interface of the snapshots taken every 12 s provided the image on the right, with which it is possible to follow the movement of the recrystallization front. Initially only vertical, but once it reaches the crystalline seed below the gate it splits in two, moving towards the two opposite horizontal directions. The formation of the acute angle between the vertical and horizontal fronts determines a point of possible creation of stacking faults.

of SFs and to confirm the utility of TCAD for accurately reproducing experimental outcomes.

The previously validated model was subsequently applied to devise a method for creating SFs without triggering SiGe relaxation. The most effective strategy identified was the implementation of nitride spacers adjacent to the gate. This experiment also aimed to lay the groundwork for the fabrication of fully operational devices, which necessitated considering the STI and resulted in a reduction of the overall structure's final thickness. Consequently, Lattice Kinetic Monte Carlo simulations were performed on a modified trilayer structure, which comprised an SOI layer of 30 nm, a SiGe layer of 25 nm with 30 % Ge, and a top Si layer of 15 nm, culminating in a combined thickness of 70 nm. To achieve a complete vertical amorphization of the SiGe layer while only partially amorphizing the SOI, similar to the previous experiments, the energy for the Ge implantation was lowered by 20 keV while maintaining the same implantation dose. Nitride spacers with width of 40 nm, typically used in the CMOS65SOIMMW process prior to source/drain junction implantations, were introduced to prevent full amorphization of the SiGe. LKMC simulations were then carried out with the same recrystallization conditions as in the earlier tests. The position of the recrystallization fronts has been acquired each 12 seconds. The overlap of all snapshots provided the map reported in Fig. 3.8.

Since the two amorphized zones were kept distinct from each other, two separate multidirectional SPER events occurred on each side of the poly gate. Horizontal recrystallization fronts moved laterally in the <100> silicon direction, while the vertical recrystallization fronts advanced upwards towards the <001> silicon direction. Even though the recrystallization velocities in both directions are theoretically identical [19], the horizontal front was observed to progress more swiftly than the vertical one due to the presence of the spacers. This discrepancy in speed led to a decrease in the angle between the two fronts, resulting in a recrystallization pattern that mirrored the one seen in the previous LKMC simulation. This observation indicated that stacking faults could potentially be generated in this new structure as well.

To assess the influence of SFs on the final strain, it was crucial to minimize the relaxation of the SiGe layer. We validated this premise by rigorously evaluating the mechanical behavior of the structure post-amorphization, using COMSOL Multiphysics simulations [23]. In the COMSOL simulations, the amorphized regions were represented by inserting two blocks of amorphous silicon on either side of the gate. For this amorphous material, we assigned an isotropic Young's modulus and Poisson's ratio with values of 120 GPa and 0.27 [24], respectively. The outcomes

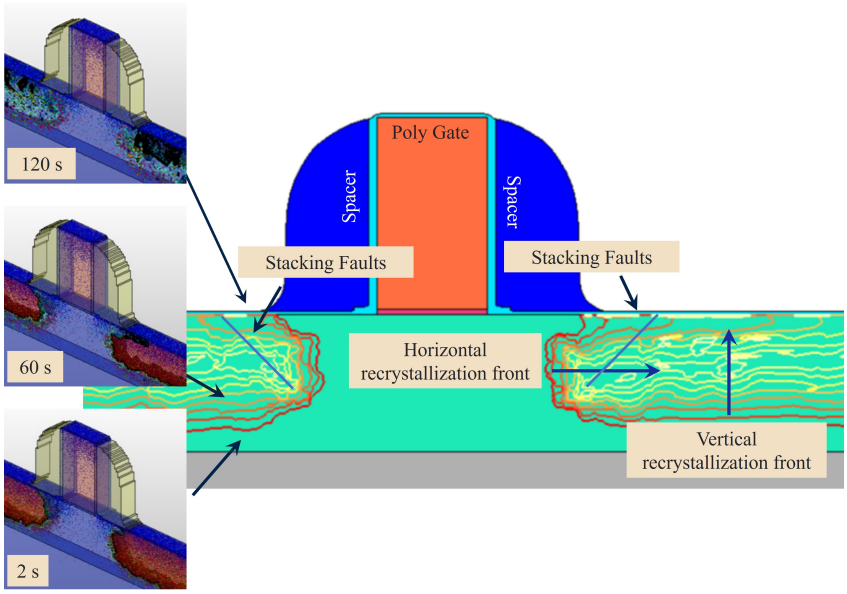


Fig. 3.8.: Similar to Fig. 3.7, the results of LKMC simulations for the new SiGe-relaxation-free test are reported. In this case, the aim was to study the SPER event following amorphization of a structure provided with spacers, that will be used to avoid the two amorphized zones on the sides of the gate to merge. The study provided the amorphization/recrystallization conditions necessary to obtain stacking faults, which are believed to form at the points below the spacers where the recrystallization fronts form acute angles.

from COMSOL simulation are reported in Fig. 3.9 and indicate a slight relaxation of the SiGe at the interfaces with the amorphous silicon, while the central part of the SiGe layer remained fully compressed. The strain values within the Si channel were approximately 0.05 %. These results confirmed that the selected conditions and structural design effectively prevented the relaxation of the SiGe layer, thereby nearly eliminating its contribution to the final strain in the Si channel. This ensures that the impact of SFs on the strain can be measured with minimal interference from SiGe relaxation.

After the experiment was meticulously planned through computational means, we proceeded to fabricate the new SOI / SiGe / Si structure. The same fabrication process previously described was utilized, with adjustments made to the growth durations to accommodate the altered thicknesses of the layers and to account for loading effects [25, 26, 27]. These effects are specific to patterned wafers, where the presence of oxide can lead to charge accumulation in the active well, consequently altering the growth rate compared to that on blanket wafers. The gate and spacers were then constructed in accordance with the established CMOS65SOIMMW process. The amorphization and subsequent recrystallization steps were carried out using the parameters determined from the simulations: a germanium implantation step with

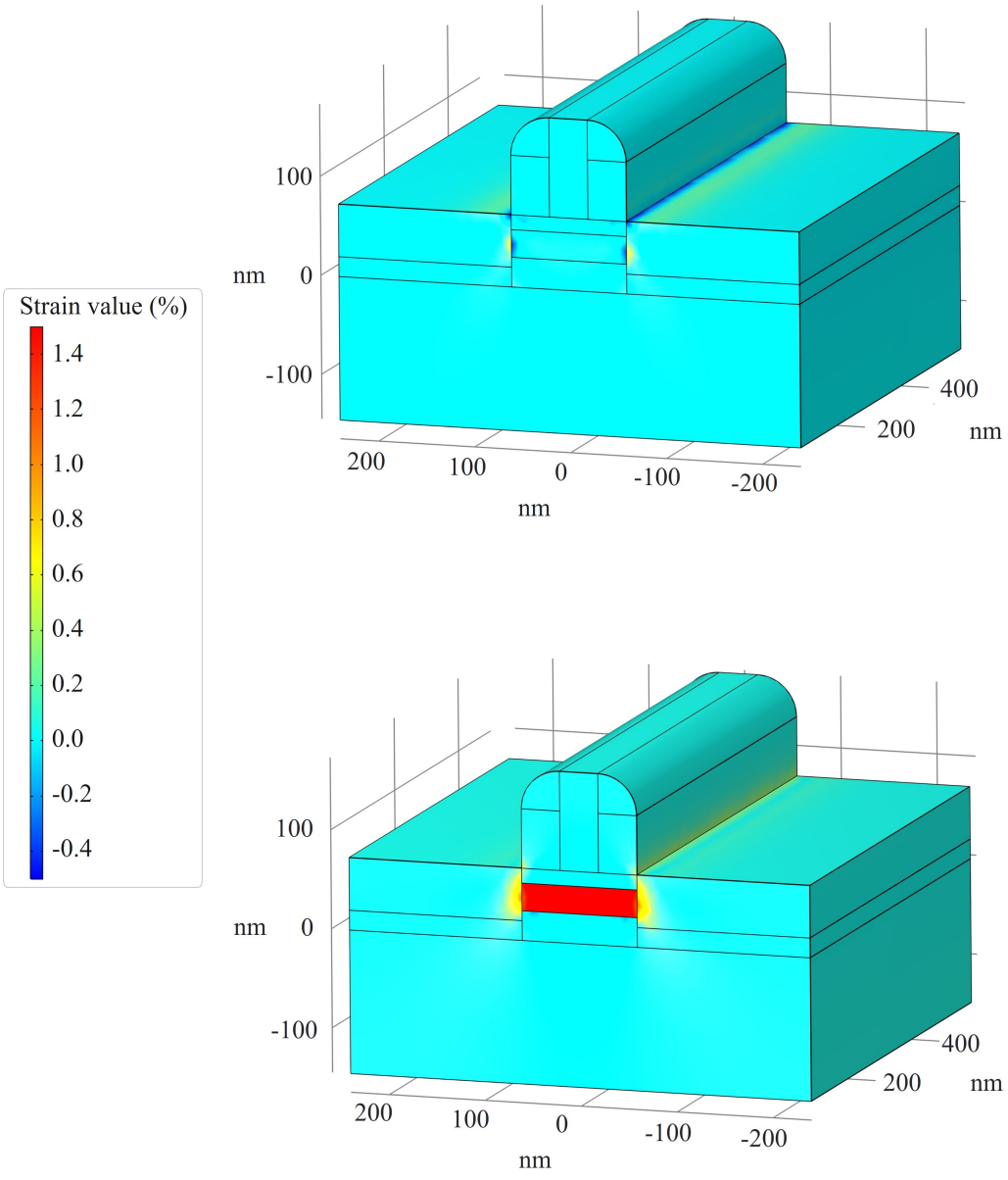


Fig. 3.9.: In-plain (top) and out-of-plane (bottom) strains of COMSOL simulations of SiGe relaxation in a spacers-equipped structure. The results show an almost complete lack of relaxation due to the distance between the two amorphized regions.

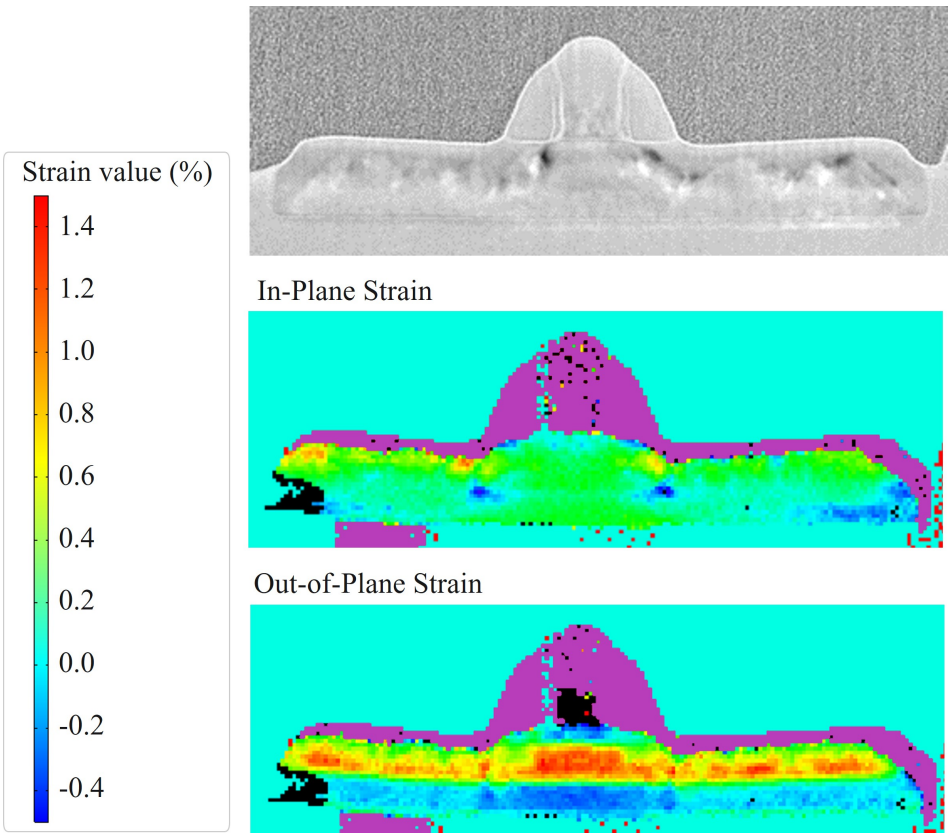


Fig. 3.10.: The PED result of the spacer experiment is here reported. From top to bottom, the HAADF image of the sample and the in-plane and out-of-plane strain cartographies are shown, respectively. the almost complete uniformity of the in-plane strain value close to 0 % confirms the lack of relaxation of the SiGe. At the same time, two spots with positive and negative strain are visible inside the trilayer structure and at the sides of the spacers, where stacking faults probably originated.

a dose of 2e15 cm^{-2} and an energy of 30 keV, followed by a thermal annealing at 600 °C for 120 seconds to ensure a proper recrystallization. To gather strain data, PED measurements were performed once again. Results are reported in Fig. 3.10.

The strain maps indicate that the in-plane strain remains relatively uniform throughout the structure, suggesting that there has been no significant change in the average strain content. The fact that ε_{xx} still globally assumes values greater than 0 % is due to two possible factors: the first is the relaxation of the lamella in the direction perpendicular to the image due to its reduced thickness, which could cause a global change in the strain within the sample; the second is an imperfect identification of the no-strain point (0 %) due to suboptimal calibration of the measuring instrument or of the algorithm used during data extraction. Additionally, the out-of-plane strain exhibits positive values within the SiGe layer, which is attributed to the vertical

distortion resulting from its pseudomorphic phase. This confirms that the SiGe layer did not undergo relaxation during the amorphization and recrystallization process. Nonetheless, two notable spots were identified on either side of the gate, aligned with the spacers, where both positive and negative strains are observed above and below, respectively, a hypothetical horizontal line. The positive strain reached peak values of up to 1.5 %, while the negative strain reached values as low as -0.5 %.

Subsequent HRTEM analysis was performed to investigate the characteristics of these spots, which revealed the presence of stacking faults (Fig. 3.11). For each spot, two dislocations on the (0 -2 2) plane were detected, confirming their role as the source of strain within the structure. As outlined by Nobarro [28] such lattice defects can indeed generate a certain amount of strain.

To mirror the experimental findings, Sentaurus simulation was conducted, incorporating two dislocations with their cores positioned where the horizontal and vertical recrystallization fronts were expected to produce stacking faults. In Sentaurus, the strain and stress contributions of dislocations are calculated using the Airy stress functions [28]:

$$\sigma_{xx} = -\frac{Eb}{4\pi(1-\upsilon^2)}\frac{y(3x^2+y^2)}{(x^2+y^2)^2} \tag{3.1}$$

$$\sigma_{yy} = -\frac{Eb}{4\pi(1-\upsilon^2)}\frac{y(x^2-y^2)}{(x^2+y^2)^2} \tag{3.2}$$

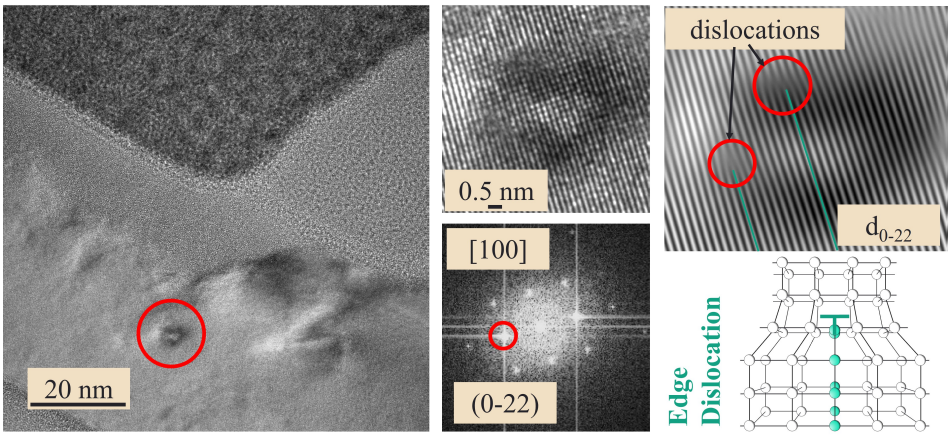


Fig. 3.11.: The left image, showing a detail of the HRTEM analysis of the spot to the left of the gate that showed positive and negative in-plane strain, identifies the presence of defects (highlighted in the figure by the red circle). Through Fourier transform it was possible to limit the observation to the crystalline planes (0 -2 2) of the silicon, generating the right image where two edge dislocations are highlighted in green. An edge dislocation is also represented schematically.

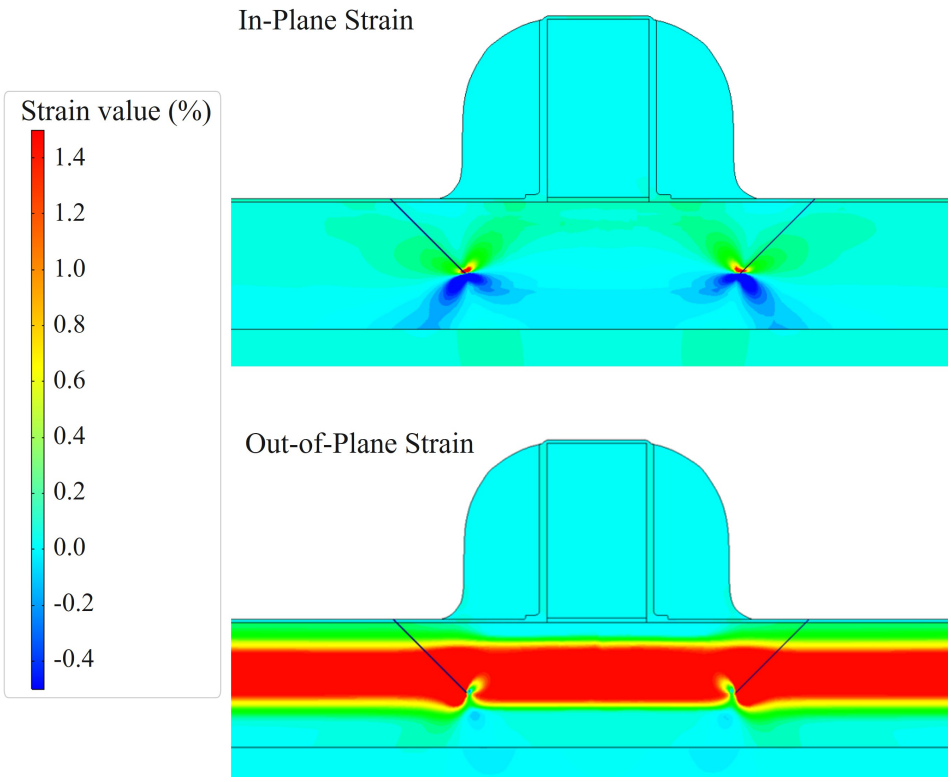


Fig. 3.12.: The in-plane (top) and out-of-plane (bottom) strains of the TCAD simulations with edge dislocations are reported. The results show very similar cartographies to those obtained with the PED measurements, demonstrating an almost perfect agreement between simulation and experiment.

where σ_{xx} and σ_{yy} are the in-plane and out-of-plane (parallel and perpendicular to the surface) stress contents, respectively, E is the Young's modulus, υ the Poisson ration, b the Burger's vector, and x, y the coordinates of the measuring location. Sentaurus simulations reveal that a positive (tensile) stress is observed at the upper part of each dislocation, where the missing half plane is located, whereas a negative (compressive) stress is obtained in the lower part (Fig. 3.12). The side-by-side evaluation of the experimental strain maps and those generated by simulation indicates a strong correlation between the positions of the dislocations and the strain they induce, with both datasets showing nearly identical results, confirming that SFs can induce quite important amounts of strain. These features suggest that in the first stress transfer test, the high in-plane strain levels obtained in the Si-top layer could have been obtained not only for the relaxation of SiGe, which actually was found to be partial, but also due to the presence of SFs.

The results reported in this section underscore two pivotal outcomes for the Strained SOI project. First and foremost, we have verified that the Localized SiGe Stres-

sor Technique can introduce high amount of strain in the channel when the two amorphized regions are close to each other. In fact, when the two are separated, as in the second test where spacers were introduced, SiGe struggles to relax and therefore to induce tensile strain within the Si-top layer, particularly in the center of the device. It is therefore believed that this technique is functional only for short-channel devices, leaving the initial amount of strain in long-channel devices almost completely unchanged. Moreover, we identified two different phenomena that coexist for the introduction of strain in the channel: (1) by inducing SiGe to relax by means of partial amorphization of the SOI / SiGe / Si structure and (2) by creating dislocations at the sides of the channel. The final strain value is expected to be modulated by varying the parameters of the trilayer structure, such as adjusting the germanium concentration in the SiGe layer and the thicknesses of the layers. Indeed, increasing the Ge content within the SiGe results in a larger lattice parameter for the fully relaxed crystal, leading to greater stretching of the Si-top layer. However, it is important to note that there is a maximum Ge content limit for a given SiGe thickness [29, 30, 31]. Exceeding this limit causes the crystal to relax non-elastically, resulting in fractures. Additionally, it is believed that a thinner silicon top layer induces more strain in the channel's inversion zone. This was evidenced by the first test, which showed a decrease in strain when moving from the SiGe / Si interface to the dummy gate. Further studies will be necessary to clarify these relationships. Moreover, final strain could be also be modified by strategically altering the positions of the dislocations. By bringing them closer to the channel, their impact on the strain will be greater, without introducing any electrical conduction problems due to the uniformity of the crystal lattice. Indeed, the dislocation cores were found to be located far from the Si-top layer. Finally, a second important outcome is given by the fact that the findings confirm the efficacy of TCAD and COMSOL simulations as predictive tools for dislocation formation and for quantifying their strain contribution, and for SiGe relaxation. The validation of both suites as reliable resources opens up further possibilities for precise engineering of strain in Silicon-On-Insulator structures to optimize device characteristics.

3.2 Integration of the Localized SiGe Stressor Technique

The initial step in applying the Localized SiGe Stressor Technique involved verifying its functionality and understanding how stress is transferred from SiGe to the Si channel. The subsequent step focused on adapting the standard process to effectively

integrate the stressor method. This adaptation required addressing issues related to the thermal budgets used during the process, which impact the stability of the structure.

In the following sections, we will present the results about the studies concerning the diffusion of Ge beyond the SiGe layer and the uncontrolled diffusion within the SiGe of species forming the source/drain junctions. These findings will be incorporated into the manufacturing process to produce functional strained-SOI devices, which will be showcased at the end of this paragraph.

3.2.1 Structural stability and Ge diffusion

To maximize the effectiveness of the Localized SiGe Stressor Technique, it is essential to maintain structural stability throughout the fabrication process. This involves preventing relaxation of the SiGe layer before the amorphization step and minimizing the diffusion of Ge. This latter phenomenon could reduce the inherent compressive strain in the as-grown SiGe layer, thereby diminishing the stress that can be transferred to Si channels. Consequently, it is crucial to assess and manage the effects that thermal budgets may have on the stability of the SOI / SiGe / Si stack.

Previously conducted tests demonstrated that only after the gate oxide formation the stability of the stack was impacted, because of the most critical temperature steps of the entire CMOS65SOIMMW fabrication flow. Gate oxide formation occurs in two steps: the first one conducted below 970 °C is used to oxidize silicon, while the second one, the so-called Post-Nitridation Anneal (PNA), is normally conducted at 1100 °C to induce the absorption of nitrogen atoms in the formed oxide, enhancing the dielectric constant.

To investigate the impact of gate oxide formation, we treated two stacks composed of BOx / SOI 6 nm / SiGe 20 nm with 20 % of Ge / Si-top 18 nm with two different gate oxide processes: one that included both oxidation and PNA steps, and another that omitted the PNA step. To assess the extent of SiGe relaxation and Ge out-diffusion, we conducted Reciprocal Space Maps (RSMs) around the asymmetrical (113) X-Ray diffraction order and ω-2θ scans around the symmetrical (004) XRD order, respectively, both before and after the thermal treatments.

In the (113) RSMs, SiGe relaxation is indicated by a shift in the SiGe layer's Q_{x} coordinate to a value lower than that of the SOI substrate, and an increase in the Q_{z} coordinate, which would bring it closer to that of the substrate compared to its position immediately after epitaxy. The RSMs for both gate oxide processes

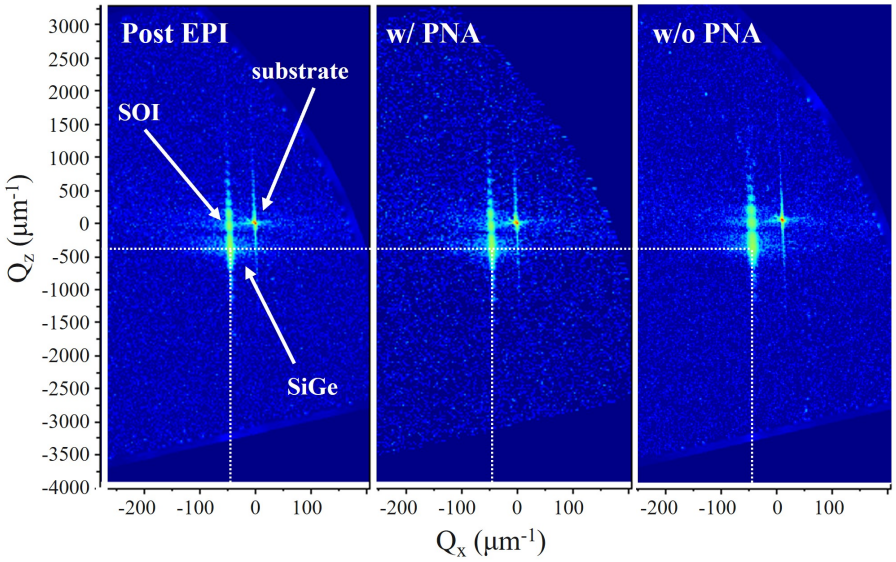
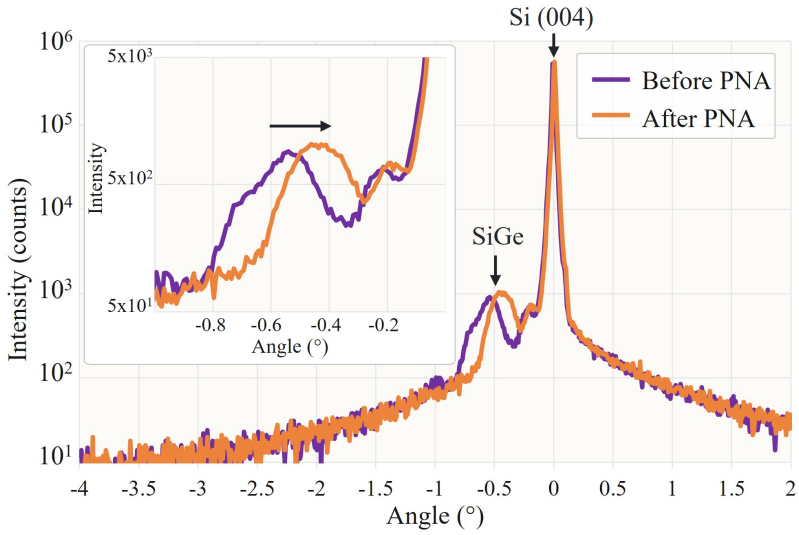


Fig. 3.13.: Reciprocal Space Maps close to the (113) XRD order of the structure as-grown ("Post EPI") and after gate oxide processes with ("w/ PNA") and without PNA ("w/o PNA"). The reciprocal lattice coordinates of SiGe peak did not change whatever the configuration, meaning that SiGe did not relax.

(illustrated in Fig. 3.13) showed that the Q_x coordinate of the SiGe layer remained aligned with that of the SOI substrate, and there were no significant shifts in the SiGe signal along the Q_z direction compared to its position immediately following epitaxy. This indicates that the SiGe layer did not undergo relaxation and that the internal compressive strain was successfully retained in both processes.

However, when analyzing the ω-2θ XRD profiles (Fig. 3.14a), a discernible angular shift of the SiGe peak towards the Si peak was observed in the sample that underwent the PNA. As depicted in Fig. 3.14b, the XRD profile of the SOI / SiGe / Si stack before the PNA step could be accurately modeled using a discrete three-layer structure, consisting of the SOI, SiGe, and Si-top layers. Post-PNA, a more complex five-layer model became necessary to describe the structure due to the introduction of SiGe interlayers, caused by Ge diffusion, with intermediate Ge content. The analysis revealed that the maximum germanium concentration in the SiGe layer decreased from an initial 19.9 % to 16.5 % after PNA. Additionally, the total thickness of the SiGe layers, which is the cumulative thickness of all SiGe layers, expanded from the original 20 nm to 27.8 nm.

To simulate the experimental findings, we employed an inter-diffusion model within the Sentaurus Process software suite. This model posits that the movement of silicon and germanium atoms is facilitated by point defects, predominantly vacancies and



(a)

before PNA			after PNA		
layer	Ge (%)	th (nm)	layer	Ge (%)	th (nm)
Si		17.0	Si		12.4
			SiGe	9.5	4.0
SiGe	19.9	20.0	SiGe	16.5	17.9
			SiGe	11.1	5.9
Si		5.7	Si		1.4

(b)

Fig. 3.14.: a) HRXRD measurements around the (004) XRD order before and after the gate oxide process with standard PNA step are reported. In insert, the zoom showing the angular shift of the SiGe layer peak is provided, which reports that a modification of the Ge content profile in the structure occured. b) Fit results are given in the table for both measurements. The table shows the Ge content and thickness values for each layer identified by the analysis of the two HRXRD measurements. Before PNA, the diffraction profile can be described by a three-layer model. After the use of PNA, a five-layer model is necessary to reproduce the experimental data, highlighting the Ge diffusion outside the SiGe.

interstitials, and that the diffusivity of these atoms is increased by the presence of internal strain. The governing equations of the model are detailed in [32, 33]:

$$\frac{d}{dt}C_{\mathrm{Ge,Si}} = \nabla \cdot (D_{\mathrm{inter}} \nabla C_{\mathrm{Ge,Si}}) - \nabla \cdot (D_{\mathrm{inter}} C_{\mathrm{Ge,Si}} (1 - x_{\mathrm{MOLE}}) \frac{\Delta V}{k_B T} \nabla P) \tag{3.3}$$

$$D_{\mathrm{inter}} = D^{V}_{\mathrm{inter}} D_{VF} \frac{C_V}{C*_{\mathrm{V(intrinsic)}}} + D^{I}_{\mathrm{inter}} D_{IF} \frac{C_I}{C*_{\mathrm{I(intrinsic)}}} \tag{3.4}$$

where C_{Ge} (or C_{Si}) is the concentration of Ge (or Si) atoms in SiGe, k_B is the Boltzmann constant, T the temperature in kelvin, ΔV is a parameter with volume dimensions, and P is the pressure; C_V and C_I are the concentrations of vacancies and interstitials; C_V^* intrinsic and C_I^* intrinsic are the equilibrium concentrations of vacancies and interstitials in the intrinsic materials; D^V_{inter} and D^I_{inter} are the interdiffusion coefficients in undoped and unstrained SiGe for vacancy and interstitial mechanisms; finally, D_{VF} and D_{IF} are the coefficients that take into account the modification of diffusivity of vacancies and interstitials in strained SiGe, as a function of pressure. To conduct the simulations, the standard values listed in the Sentaurus manual [18] have been used for all parameters.

When only the oxidation step was considered, no Ge diffusion was observed, as experimentally. However, for the scenario involving PNA, the model was able to quite accurately replicate the broadened width of the SiGe layer following the thermal treatment, as shown in Fig 3.15a. The small difference between the two dataset is due to the fact that while HRXRD analysis gives average values of Ge content and thickness, TCAD simulations provide a continuous Ge profile.

Using our model, we also projected the effects of a reduced-temperature PNA on the structural stability, indicating that lowering the annealing temperature by 75 °C could effectively restrain the migration of germanium atoms from the SiGe layer, as reported in Fig. 3.15b. The simulation predicted that the initial germanium mole fraction (0.20) would be entirely conserved, while the final thickness of the

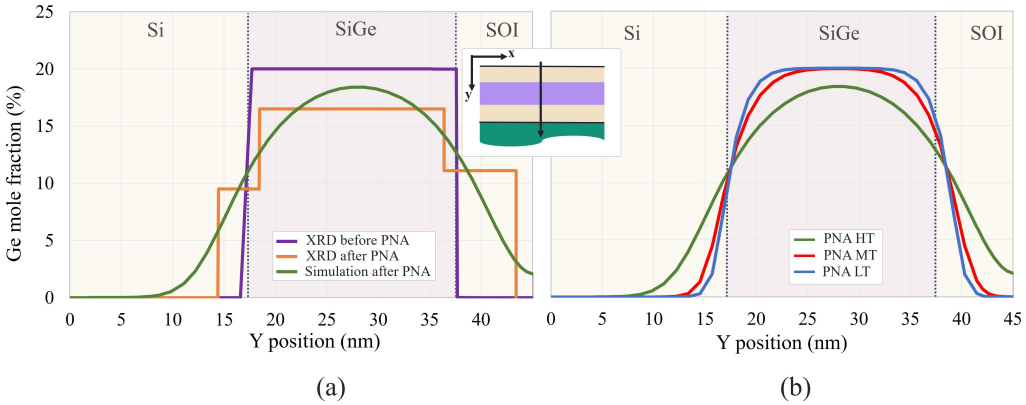
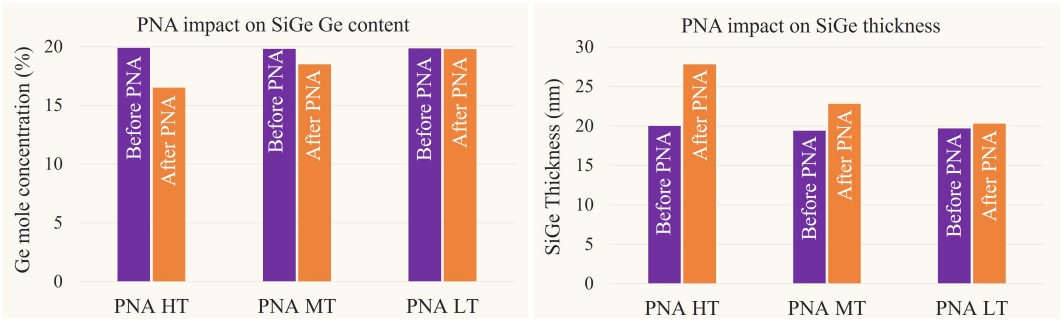


Fig. 3.15.: a) The XRD analysis results in Fig. 3.14 for Ge content are reported together with the post-PNA profile simulated in Sentaurus, showing a good agreement between simulation and experiment. b) The Ge profiles reported are the results of simulations performed by testing three different PNA temperatures (HT = 1100 °C, MT = 1050 °C, LT = 1025 °C). It can be seen that as the temperature is lowered, the diffusion of Ge outside the SiGe decreases, keeping the Ge concentration and the SiGe thickness almost identical to the pre-PNA case.



(a) **(b)**

Fig. 3.16.: Comparison of a) Ge contents and b) SiGe thicknesses before and after the PNA step at different temperatures (HT = 1100 °C, MT = 1050 °C, LT = 1025 °C). The plots show that the initial properties of the SiGe layer are almost completely preserved when PNA temperature is decreased by 75 °C.

SiGe layer (evaluated as the segment between the two points at which Ge content becomes 0 %) would be 30 % less than that resulting from a standard PNA at a temperature 75 °C higher.

To validate these computational insights, experimental trials were carried out. The HRXRD findings post-processing confirmed a diminished germanium diffusion at the lower temperature: the thickness of the processed SiGe layer was reduced by 26 %, and the peak germanium content was slightly lowered to 0.19 (Fig. 3.16a-b). These results underscore the accuracy of our model in managing and maintaining the structural integrity of the SOI / SiGe / Si stack. They also highlight the necessity to adjust the CMOS65SOIMMW fabrication process to ensure the production of high-performance devices. A low-temperature PNA has indeed been adopted in the process for the fabrication of the devices that will then be electrically characterized. The only possible risk that could arise from using a PNA at a lower temperature is that of reducing the nitrogen absorption of the gate oxide, thereby lowering its dielectric constant. A possible variation in the threshold voltage and gate leakage is therefore expected.

3.2.2 Source/Drain n-type dopants lateral diffusion in SiGe

For the successful fabrication of functional devices, precise formation of the source/drain junctions is essential. The implantation conditions and thermal treatments for S/D formation in the standard CMOS65SOIMMW process are designed with the diffusion properties of dopants in silicon in mind, to prevent excessive diffusion that could lead to device shortening. However, the integration of a SiGe layer within the SOI substrate introduces a significant challenge in controlling dopant diffusion, as even a

small incorporation of Ge into the Si lattice can dramatically increase dopant diffusivity. Initial testing using standard implant conditions and Spike annealing at 1000 °C post S/D implantation for dopant activation resulted in complete short-channel formation between source and drain for devices with short channels, rendering them unable to be electrostatically controlled. This issue did not arise in longer transistors due to the greater distance between the junctions.

To confirm that the observed leakage was caused by the over-diffusion of n-type dopants into the SiGe layer, Electron Energy Loss Spectroscopy (EELS) analysis was performed to pinpoint the dopants' locations post-Spike anneal. EELS was chosen over Energy-Dispersive X-ray Spectroscopy (EDX) because the latter could not adequately detect dopants like phosphorus and arsenic within the channel, owing to its higher detection limits. EELS, by contrast, can identify even trace amounts of dopants by analyzing the energy lost through inelastic electron collisions within the sample [34].

Comparing the energy loss profiles in the SiGe layer of devices with short and long channels, we detected a doublet in the first peak of Si in the short channel devices (indicated by dark arrows in the Fig. 3.17), suggesting the presence of additional species, likely As or P [35, 36, 37], though it was not possible to discern between them.

To further substantiate this hypothesis, TCAD simulations were carried out (Fig. 3.18). The simulations using standard Spike anneal conditions showed that phos-

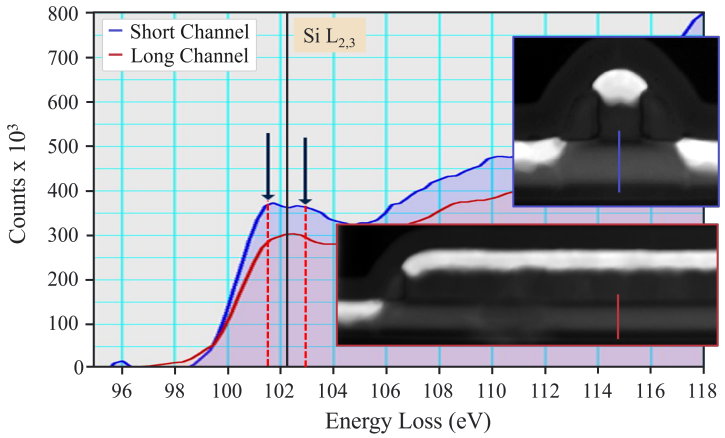


Fig. 3.17.: Comparison of EELS profiles obtained at the center of short- and long-channel strained-SOI devices. The two signal peaks detected in the short-hannel case close to the silicon $L_{2,3}$ signal indicate the presence of a different chemical environment than the long-channel case. This could be caused by the uncontrolled diffusion inside the SiGe of phosphorus or arsenic used for the source/drain junctions.

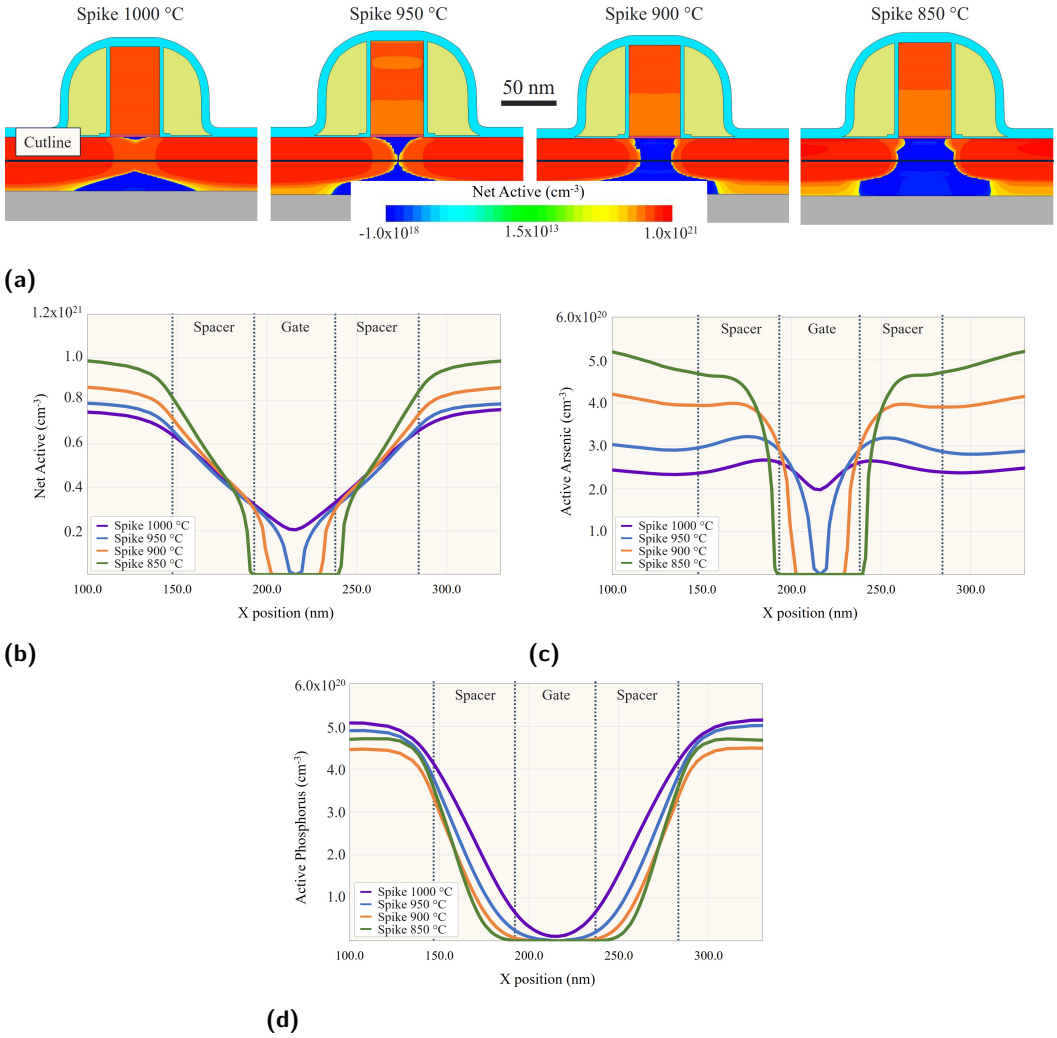


Fig. 3.18.: a) TCAD simulations at different Spike temperatures, reporting different extent of source/drain dopant diffusion. Reducing temperature leads also to the reduction of dopants diffusion and activation in the polysilicon, as reported by the variation of the Net Active. The plots report the simulated horizontal profiles inside the SiGe of the b) net active, c) active arsenic, and d) active phosphorus at different temperatures.

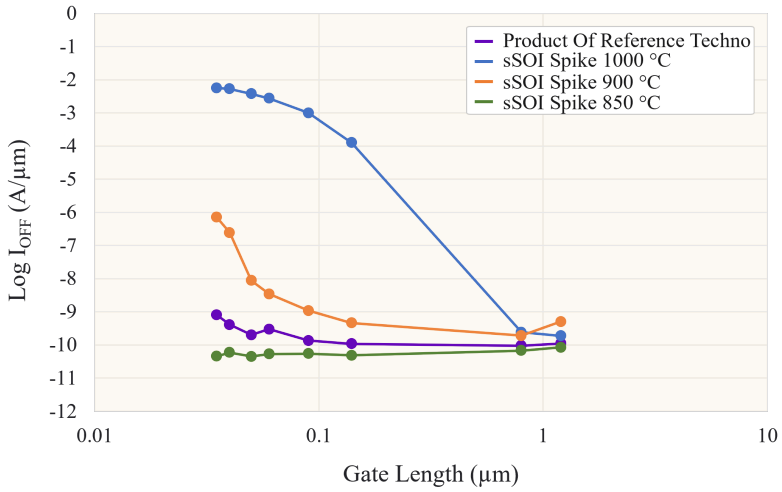


Fig. 3.19.: The figure shows the parametric tests data of the I_{OFF} for different gate lengths of the strained-SOI devices treated with different Spike temperatures.

phorus diffuses aggressively into SiGe, with its diffusivity being enhanced by the presence of Ge compared to its diffusion in pure silicon. Arsenic was also observed to diffuse into SiGe, albeit to a lesser extent. The results from Sentaurus simulations confirmed that the diffusion of n-type dopants needs to be carefully optimized to circumvent issues of over-diffusion.

A direct method to curtail the diffusion of dopants is to lower the annealing temperature used during the process. TCAD simulations indicated that a reduction to 900 °C or 850 °C could be effective. To assess the accuracy of the Sentaurus simulations, experimental trials were conducted at these two temperatures. The leakage current for both sets of samples was measured using Parametric Tests (Fig. 3.19). The best results was obtained when employing a Spike anneal at 850 °C, as If_{OFF} in strained-SOI samples (sSOI) is similar to the values of the technology Product of Reference (POR). At 900 °C, dopants still diffuse into SiGe consequently leading to an Off current of about 10^{-6} A/µm for short-channel devices. However, given the fact that this value could be considered as satisfactorily low, we decided to proceed with a Spike at 900 °C for the production of devices. This choice aims to maximize dopant activation in both the active silicon and the polysilicon gate, ensuring optimal device performance by achieving low resistance and minimizing the possible phenomenon of polysilicon gate depletion.

3.2.3 Sample Fabrication

The studies and corresponding results reported in the previous paragraphs have been crucial for the integration of the Localized SiGe Stressor Technique within the CMOS65SOIMMW process and the subsequent functionality of the devices. In the manufacturing process, reported in Fig. 3.20, the PNA temperature was reduced from 1100 °C to 1025 °C, and the Spike temperature post source/drain implantation was limited to 900 °C instead of 1000 °C. An example of a strained-SOI device manufactured under these conditions is shown in Fig. 3.21. The image demonstrates a geometry very similar to that of the so-called silicon-reference devices despite the presence of the trilayer stack and the process modifications.

As reported in Fig. 3.20, in addition to these main changes (highlighted in green), which were applied to all manufactured samples, some devices underwent further process modifications aimed at optimizing the stress transfer from SiGe to the Si channel and avoiding phenomena that are difficult to study and foresee computationally, such as the poly-depletion phenomenon. For the former, some samples were treated with a tilted Ge implantation to extend the amorphized area and further relax the SiGe, theoretically increasing the strain in the silicon channel. For the latter, as explained in the following section, we attempted to improve doping activation in the polysilicon gate. Specifically, some samples were subjected to Nano Second

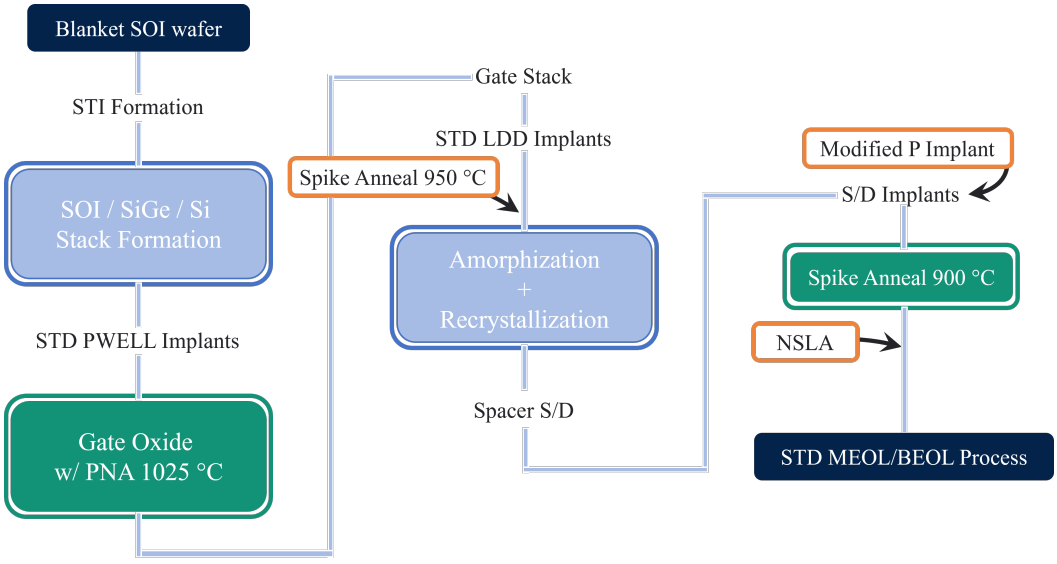
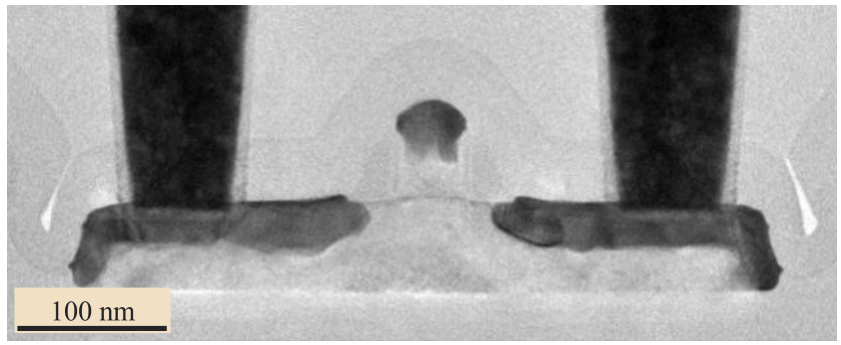
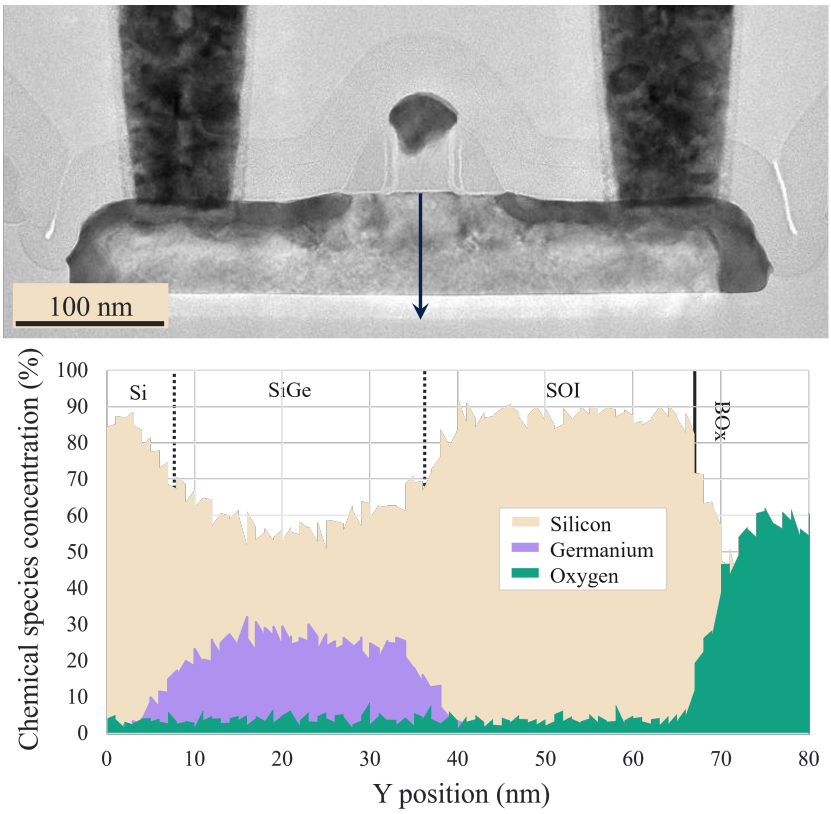


Fig. 3.20.: The complete manufacturing process of the Strained SOI project is reported. The steps added to the standard process are highlighted in light blue. The steps already present in the CMOS65SOIMMW flow but which have been modified are reported in green. Finally, the additional steps tested only on some samples are highlighted in orange.



(a)



(b)

Fig. 3.21.: a) SEM image of a silicon reference device treated with the strained SOI process. b) SEM image of a complete strained-SOI device and EDX profiles of the Si, Ge and O signals.

Laser Anneal (NSLA) after the deposition of the nitride Contact Etch Stop Layer (CESL), using energy levels of either 300 mJ/cm² or 325 mJ/cm². These limited energy levels were selected based on short-loop tests that revealed the formation defects atop the nitride layer at an energy higher than 350 mJ/cm², likely due to the onset of polysilicon melting. Additionally, some devices underwent a phosphorus implantation step with either an energy increased by 10 keV or an energy increased by 5 keV plus a doubled dosage. The rationale behind these modifications was to position the dopants closer to the gate oxide without causing diffusion, thereby increasing the concentration of activated dopants near the silicon channel. The aspect of a strained-SOI sample obtained by employing the fabrication process just described is reported in Fig. 3.21 where it is compared to the one of a silicon reference device of the same process lot.

The electrical results obtained are reported in the following sections, first presenting the electrostatic characteristics of the devices and then their RF performance.

3.3 Electrical Characterization

The devices obtained through the manufacturing process described in the previous section were subsequently electrically characterized. The results obtained will be reported hereby. The electrostatic data will be presented first. The primary goal of this initial analysis is to highlight the effects of process modifications and the implementation of this novel stressor technique on devices' electrostatic behavior. The insights gained will serve as a foundation for a more detailed discussion of RF performance outcomes that will be presented in the second paragraph.

3.3.1 Parametric Tests and DC Results

Similar to the previous project, we will examine how the processing techniques used for integrating the Localized SiGe Stressor Technique have impacted the static characteristics of LNA devices. This analysis will encompass both standard Parametric Tests (PTs) and DC measurement results for devices with varying gate lengths, focusing particularly on short-channel devices with a gate length (L_G) of 40 nm. Key parameters of interest for these devices are:

- Threshold Voltage (V_{th})
- Drain Current-Gate Voltage Transfer Characteristic (I_{DS}-V_{GS})

- Transconductance (G_{m})
- Gate-to-Channel Capacitance (C_{GG})
- Junction Capacitance (C_{JUNC})

V_{th} has been determined in linear regime, using drain-source voltages (V_{DS}) of 50 mV and varying the gate-source voltage (V_{GS}) until the drain current (I_{DS}) reaches a specific value calculated as $I_{\mathrm{DS}} = 40 \cdot W_{\mathrm{G}}/L_{\mathrm{G}}$ nA, with W_{G} and L_{G} being the gate width and length, respectively. I_{DS}-V_{GS} curves have been acquired first in Parametric Tests and then by conducting DC measurements, sweeping V_{GS} from 0 V to 2.5 V. C_{GG} measurements were carried out by connecting the drain, source, and body contacts to 0 V and varying the gate potential from -2 V to +2 V. For C_{JUNC}, a bias between -2.5 V and +0.5 V was applied at both source and drain while keeping the body contact at 0 V and grounding the gate. These measurements were taken at a frequency of 100 kHz with an AC signal amplitude of 0.1 V. C_{GG} and C_{JUNC} were limited to devices with $L_{\mathrm{G}} = 1.2$ µm and $L_{\mathrm{G}} = 40$ nm, respectively.

First, a comparison between the technology Process-of-Reference (POR) devices and the silicon reference (SR) devices of the Strained SOI project is proposed to analyze the impact that process modifications had on standard electrical characteristics without stress contributions. These SR samples have been fabricated by following the process depicted in Fig 3.20 but without the SOI / SiGe / Si structure. Secondly, the characteristics of the strained-SOI wafers will be reported, highlighting the effect of employing this new stressor methodology on performance.

As shown in Tab. 3.1, as silicon reference (SR) we selected a SOI sample which underwent a PNA at 1025 °C and a 950 °C Spike anneal after the Lightly-Doped-Drain (LDD) implantations. LDD is commonly used to reduce the electric field at the drain side, avoiding failures. The 950 °C Spike was employed with the aim of ensuring nearly standard LDD activation, approaching the efficiency of the standard Spike at 1000 °C after the n-type source/drain implantations. SR samples were treated with a 600 °C anneal step before the source/drain implantations, in order to evaluate the impact of this thermal budget on doping profiles and devices characteristics. The phosphorus implant energy for the source/drain junctions formation was increased by 10 keV, aimed to increase doping in the polysilicon gate near the oxide interface to avoid poly-depletion, as the same implantation is used for both source/drain and poly-gate doping. Finally, the Spike anneal after S/D was reduced to 900 °C. Due to the numerous changes, another silicon reference sample, SR2, will help in analyzing the modifications obtained, which differs from

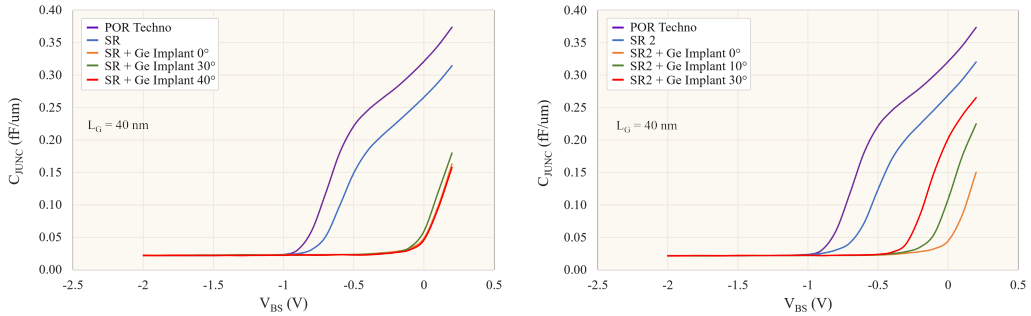
Tab. 3.1.: The modifications applied to the process are summarized here for both SR and SR2.

	POR	**Silicon Reference**	**Silicon Reference 2**
PNA	1100 °C	1025 °C	1025 °C
Recrystallization	No	2 min 600 °C	2 min 600 °C
Spike after LDD	No	950 °C	No
NSD P implant	15 keV 3e13 cm^{-2}	25 keV 3e13 cm^{-2}	15 keV 3e13 cm^{-2}
Spike anneal	1000 °C	900 °C	900 °C

the standard process only for the temperature-reduced PNA, the amorphization step, and the 900 °C Spike anneal after the source/drain implantation.

A first fundamental feature for the functionality of a transistor device is the correct formation of junctions. By comparing the junction capacitance curves of the POR and SR samples (Fig. 3.22a), both exhibit a similar trend, confirming that the source/drain junctions have been correctly formed. As the body voltage becomes more negative, the curves show a smooth decrease due to the extension of the junction depletion regions, followed by a drastic reduction between -0.5 V and -1 V, after which the capacitance value remains constant regardless of the applied voltage. This occurs because the source and drain depletion regions extend completely over the body, eventually fully depleting the device. At this point, any modification of the body-contact potential has no effect.

The fact that full depletion occurs at higher voltages in the silicon reference device is linked to the larger extension of the depletion regions compared to the POR sample. Since the source/drain sheet resistances showed a decrease in value for the silicon



(a) **(b)**

Fig. 3.22.: Comparison of C_{JUNC} curves between a POR device and the a) SR and b) SR2 ones. Cases with Ge implantation are also reported. Although with different trends, the curves generally show typical behaviors of POR junctions.

reference sample (passing from 22.5 Ω, for POR, to 15 Ω, for SR), it is believed that there is higher n-type dopant activation in this sample. This increased activation could also have extended the junctions' depletion regions, causing full depletion to occur at higher voltages.

The junction capacitance of SR2 shows a characteristics very similar to that of the SR, but with full depletion occurring at higher V_{BS}. Since source/drain sheet resistance is the same between SR and SR2 (for SR2 being 14.5 Ω), the most likely explanation is that the anneal conditions achieved less activation of the dopants in the body.

Some samples of the SRs were also treated with an amorphization step before the recrystallization anneal, under different conditions. For the SR-like samples, Ge implantation energy was set at 25 keV, also testing different angles: 0°, 30°, and 40°. For the SR2-type samples, Ge implantation was performed at 30 keV with three different tilt angles: 0°, 10°, and 30°. Their junction capacitance characteristics are also reported in Fig. 3.22a-b. For both cases, the 0° tilt amorphization causes full depletion to occur already at $V_{BS} = 0$ V. For SR, increasing the tilt angle has no impact on the curves, while for SR2 it causes full depletion to shift towards the standard values. Since the S/D sheet resistance does not change with Ge implantation (15 Ω), we assume that n-type doping activation is not the cause of this shift. It is most likely due to the extension of the two junctions. We hypothesize that the recrystallization conditions employed did not perfectly recover the fully crystalline phase of the two amorphized regions or created some defects, such as interstitials and vacancies, which enhanced doping diffusion [35, 36, 37]. Indeed, TCAD simulations report a no complete recovery of the crystal order when the Ge implantation is tilted. However, no clear evidence has been obtained to date of doping diffusion due to amorphization, as the leakage currents do not seem to be impacted by it, which, on the contrary, should increase with the enhancement of lateral diffusion. A more detailed study is required to understand these features and control the impact of amorphization and recrystallization on junction formation.

To ensure the functionality of the devices, the process flow must also guarantee adequate doping of the gate, particularly near the interfacial oxide. This is typically achieved using a 1000 °C Spike anneal, which allows dopants to diffuse vertically towards the oxide and become activated. However, both diffusion and activation are limited when the temperature is reduced to 900 °C. Dopant activation in polysilicon can be studied by analyzing threshold voltage (V_{th}) and gate-to-channel capacitance (C_{GG}) characteristics, as illustrated in Fig. 3.23 where these properties are compared for both SR samples relative to the technology POR.

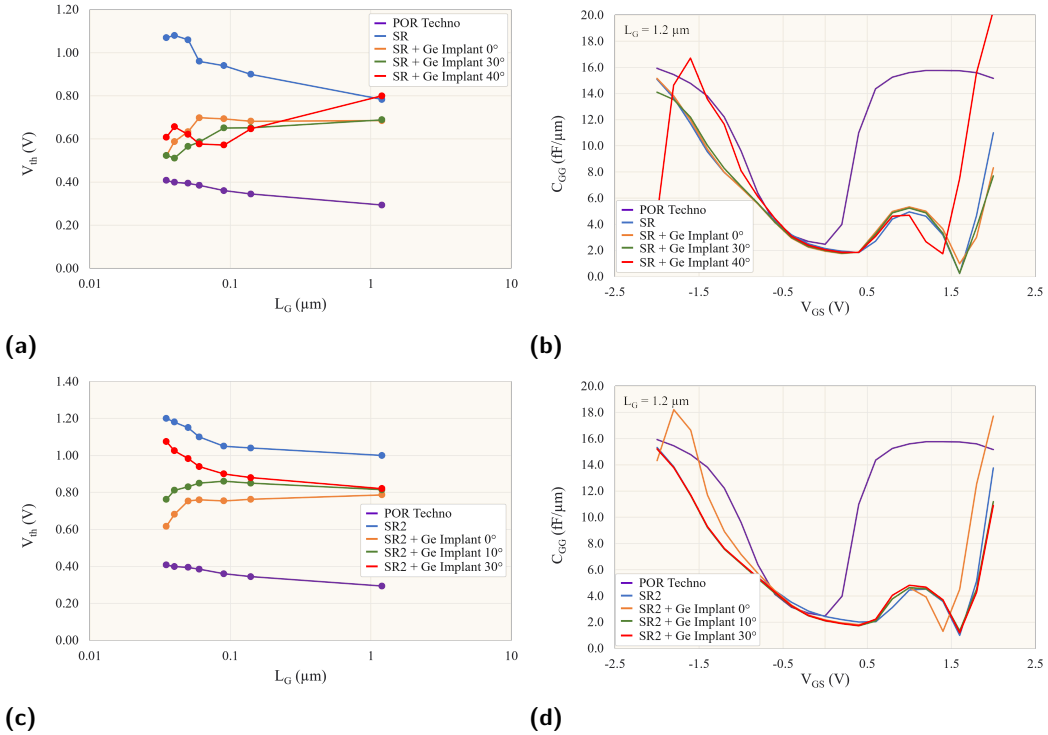


Fig. 3.23.: Threshold voltage values, for different gate lengths, and C_{GG}-vs-V_{GS} curves, measured for devices with $L_G = 1.2$ µm, are reported in a-b) for SR, and c-d) for SR2. The results are compared to POR values. For both silicon references, data show a drastic increase in V_{th}. As demonstrated by the C_{GG} curves, this behavior appears to be due to the poly depletion phenomenon, due to the low concentration levels of active doping inside the poly gates.

The V_{th} values extracted for the silicon references are significantly higher compared to the technology POR, reaching +0.5 V and +0.7 V for SR and SR2, respectively, without Ge implantation. This is likely due to reduced diffusion and activation of dopants in polysilicon compared to the standard case, leading to the so-called poly-depletion effect [38, 39, 40, 41]. This phenomenon occurs in low-doped poly-gates when a potential is applied to induce the inversion of the transistor channel. For NMOS devices with n-type doped polysilicon gates, the gate is biased with a positive voltage, attracting negative charges from the poly-gate and creating a positive depletion region at the interface with the gate oxide. This region is normally negligible for standard doped gates. However, as doping concentration decreases, the depletion region in the polysilicon extends, requiring a higher gate voltage to generate the same potential difference between gate contact and channel.

Poly-depletion is particularly evident in the C_{GG} characteristics at positive V_{GS}. In the POR case, once strong inversion is reached at 1.0 V, the C_{GG} value remains almost constant at higher V_{GS} values. Conversely, for the two silicon references, although C_{GG} starts to increase around 0.5 V, once V_{GS} reaches 1 V, the value drops as poly-depletion begins to extend. Moreover, at $V_{GS} = 1.5$ V, C_{GG} drastically increases as the hyper-low doped polysilicon probably induces poly-inversion. This is a severe issue for our devices and will obviously impact all other characteristics, as we will discuss later.

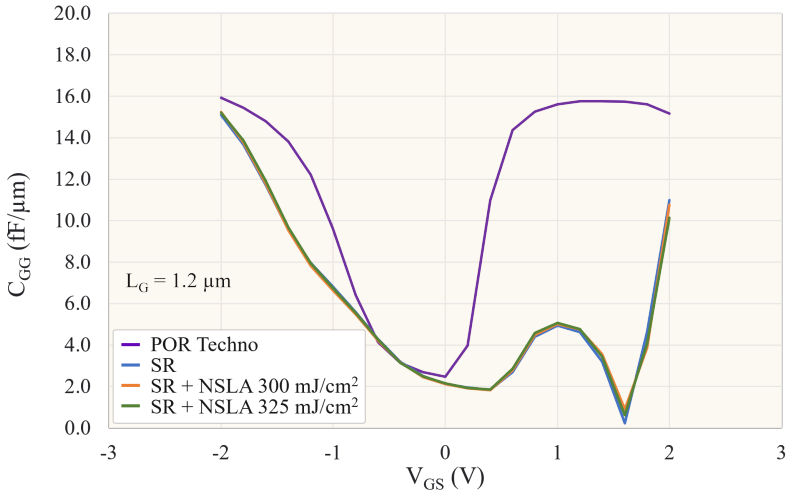


Fig. 3.24.: In the figure the C_{GG} curves of the POR sample and those of the silicon references with and without NSLA treatment are reported. The plot shows no influence of the NSLA on the characteristics of the devices, probably due to the reduced insolation energy used.

The deeper S/D implantation performed in SR does not substantially solve the problem, and the use of Nano Second Laser Anneal (NSLA) shows no positive impacts (Fig. 3.24). The simplest and most applicable suggested solution is to perform a pre-doping implant followed by a thermal anneal before polysilicon patterning. This approach allows the use of high anneal temperatures to properly diffuse and activate dopants all over the polysilicon without affecting the active silicon, as source/drain junctions have not yet been formed. This solution will be tested in a future process flow after the publication of this thesis.

Although the issue of poly-depletion has not been resolved and will affect device characteristics, a thorough analysis of the static behavior as a function of the process flow is still necessary to gain a deeper understanding of the DC and RF results. As shown, the V_{th} for samples without Ge implantation is high. However, the threshold voltage decreases when an amorphization step is introduced. Since the V_{th} roll-off is not affected by this, the decrease to lower values is most likely due to the modification of grain sizes in the polysilicon, which increases dopant diffusivity towards the interfacial oxide [42, 43, 44]. Nevertheless, C_{GG} is only slightly influenced by this change (Fig. 3.23b,d).

The I_{D}-V_{G} characteristics of the technology POR and the two SRs are shown in Fig. 3.25. As expected, the On current is drastically reduced due to the poly-depletion effect [38, 39, 40]. Poly-depletion increases the effective oxide thickness, thereby reducing C_{OX}, which significantly degrades I_{DS}. For the same reason, the subthreshold slope decreases, resulting in leakage current values below V_{GS}-V_{th} compared to the POR device. The On current is slightly higher in the SR2 case. This behavior is not been clarified yet, as S/D sheet resistance is the same for the two samples. Moreover, as the 950 °C anneal treatment after the LDD implantation was employed in SR, it was expected to have a better access resistance hence a higher current, but results show the opposite trend. Further investigation will be conducted.

Overall, the characteristics of the silicon references indicate that the modified process flow significantly impacted the doping profile in the polysilicon gate due to the reduced Spike temperature after the S/D implantation. Consequently, poly-depletion occurs, even with the use of a modified S/D implant recipe and NSLA, which drastically limits the On current of the devices. The Ge implantations appeared to mitigate this issue slightly, as evidenced by lower V_{th} and higher On current. Additionally, the LDDs and source/drain junctions seem to be well-formed, as indicated by C_{JUNC} and sheet resistance measurements. However, the source/drain junctions appear to be affected by the amorphization step, as impurities left by

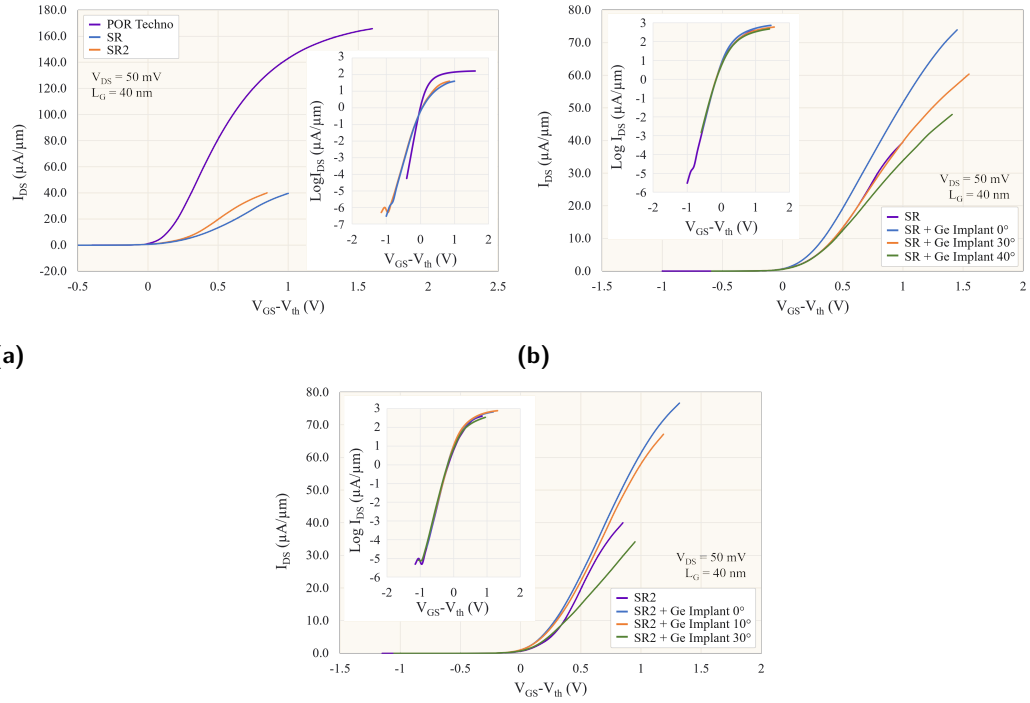


Fig. 3.25.: I_{DS}-$V_{OVERDRIVE}$ curves for silicon references are reported. a) Comparison of SR and SR2 with the POR device. b) Comparison of the characteristics for SR devices without and with Ge implant. c) Comparison of the characteristics for SR2 devices without and with Ge implant. At equal $V_{OVERDRIVE}$, the plots show a drastic reduction of current in silicon reference devices, probably due to the identified poly depletion phenomenon. The current level is also influences by the Ge implantation, obtaining maximim values for implantations without tilt.

the recrystallization process could have potentially altered the S/D doping profiles significantly.

Having identified the effects of the new process on silicon devices, we can now analyze how the new stress method influences their characteristics. Threshold voltage characteristics and C_{GG} curves are presented in Fig. 3.26a-b. As expected, poly-depletion is clearly observable even in the strained-SOI samples (sSOI), as indicated by the drop in C_{GG} around $V_{GS} = 1$ V, which in turn results in an extremely high V_{th}. The presence of a SiGe layer within the SOI does not appear to have significantly impacted the activation of p-type dopants, as V_{th} values are found to be almost identical to those of the SR, particularly for samples treated with the amorphization step.

No junction capacitance measurements were acquired for the strained-SOI sample without Ge amorphization (Fig. 3.26c). However, the C_{JUNC} of amorphized samples

exhibits the typical trend of S/D SOI junctions, indicating correct formation. Nevertheless, the decrease marking the onset of full depletion is smoother than in the silicon reference case, likely due to a less abrupt pn junction as the SiGe induced lateral dopant diffusion.

The I_{DS}-V_{GS} curves for both the SR and strained-SOI samples are shown in Fig. 3.27, including a comparison between amorphized and non-amorphized samples. If the amorphization step is not included in the process, meaning the SiGe did not have the opportunity to relax, sheet resistance worsens in the strained-SOI sample, resulting in a lower On current compared to the silicon reference. As demonstrated by sheet resistance measurements, this is because the S/D resistance of strained-SOI devices is higher (21 Ω with respect to 15 Ω of SR), likely due to lower n-type dopant activation in the SiGe. However, when amorphization is added to the process flow, the On current at $V_{OVERDRIVE}$ = 1.0 V (defined as $V_{OVERDRIVE} = V_{GS}$ - V_{th}) increases by 38 % for the silicon reference and 157 % for the strained-SOI sample. Under these bias conditions, a low electric field regime is established in the device where mobility is limited by phonon scattering. Since S/D sheet resistance did not

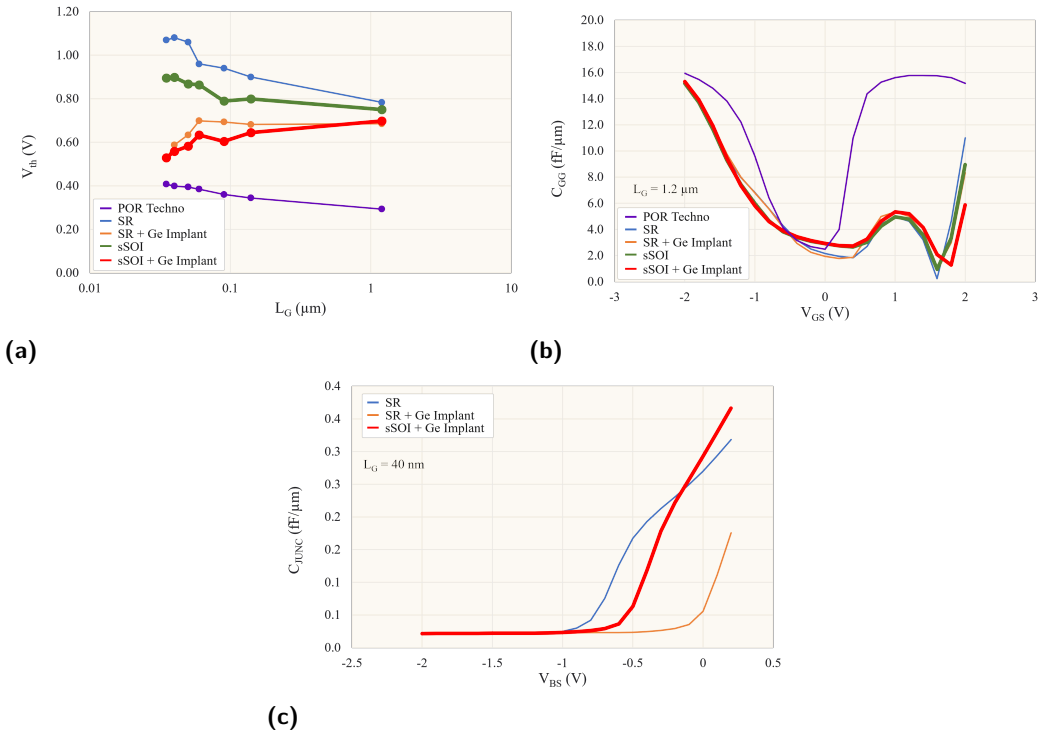
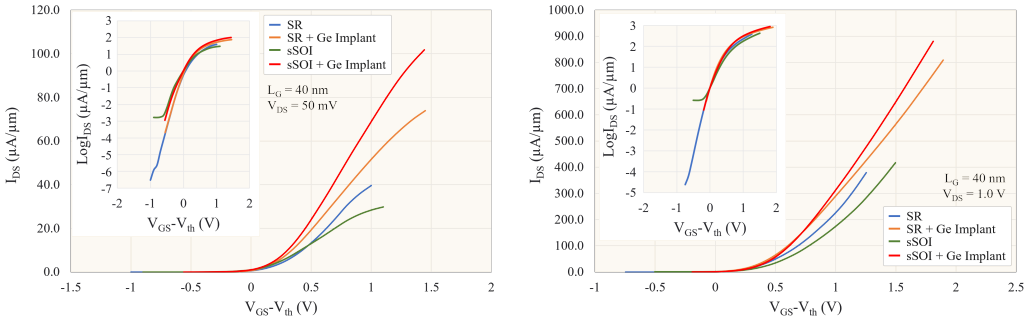


Fig. 3.26.: a) Threshold voltage, b) C_{GG}, and c) C_{JUNC} of the strained-SOI devices without and with Ge implantation are compared with the POR and SR devices. In general the measured characteristics are similar to those obtained for the silicon reference.



(a) **(b)**

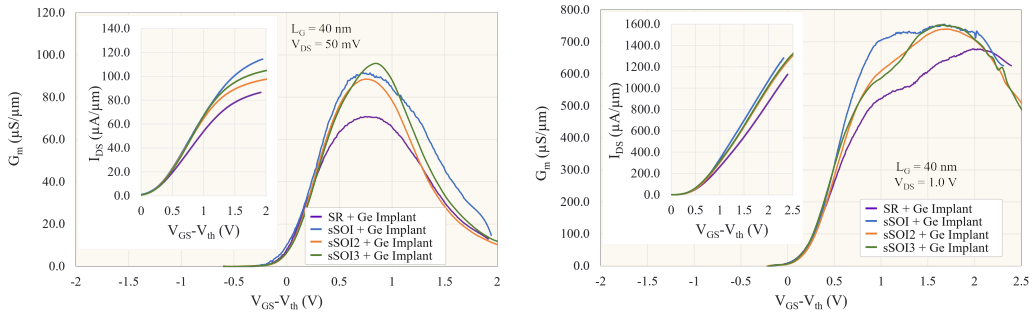
Fig. 3.27.: I_{DS}-$V_{OVERDRIVE}$ curves of the strained-SOI devices without and with Ge implantation are compared to those of SR devices in a) linear (V_{DS} = 50 mV) and b) saturation regime (V_{DS} = 1.0 V). For both conditions, the current increase that occurs in the case with the Ge implant is much greater in the sSOI devices than in SR ones, possibly due to an increase in electrons mobility.

change with the addition of the amorphization step, this improvement could be an early indication of enhanced electron mobility. A similar improvement is also observed in the saturation regime, with current at $V_{OVERDRIVE}$ = 1.0 V increasing by 12.5 % for the silicon reference and 85 % for the strained-SOI sample. In the latter case, the boost is less significant than in the previous regime, likely due to other factors such as interfacial roughness, access resistances, and saturation velocity.

PT measurements did not allow for a correct evaluation of the transconductance (G_m) of each sample due to the maximum V_{GS} value set. To study G_m, DC measurements were conducted by collecting I_{DS}-V_{GS} in both the linear and saturation regimes for all gate lengths, sweeping the gate voltage from 0 V to 2.5 V. Transconductance was then extracted as the derivative of the current-voltage curves. Other strained-SOI samples have been fabricated in addition to the one already reported, each of which underwent a specific process change in terms of thermal treatments and implantations. The splits performed are summerized in Tab. 3.2. The results for 40-nm devices are shown in Fig. 3.28.

Tab. 3.2.: Split matrix of the strained-SOI samples studied. Only the modifications not common for all samples are reported.

	SR	**sSOI**	**sSOI2**	**sSOI3**
Spike after LDD	950 °C	950 °C	No	950 °C
NSD P implant	25 keV 3e13 cm^{-2}	25 keV 3e13 cm^{-2}	25 keV 3e13 cm^{-2}	20 keV 6e13 cm^{-2}

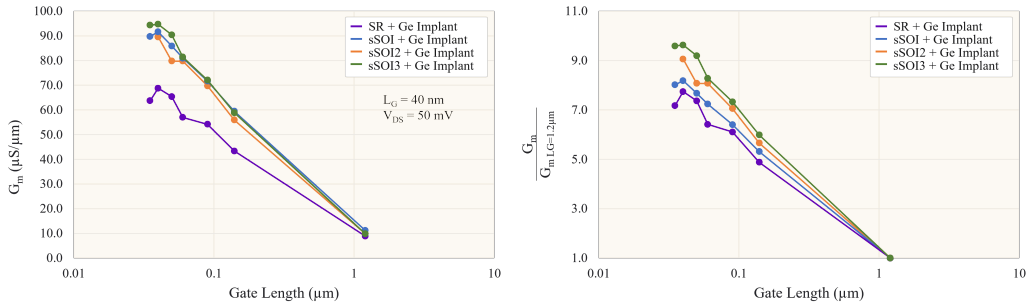


(a) **(b)**

Fig. 3.28.: G_m-vs-$V_{OVERDRIVE}$ characteristics of the strained-SOI devices with Ge implant are compared with that of the SR in a) linear and b) saturation regime. In both cases, the transconductance is higher for the sSOI samples.

In the linear regime, G_m is shown to assume higher values when the stressor technique is employed, increasing by 30 %. A similar improvement is observed in the saturation regime, although it strongly depends on the applied bias. G_m directly depends on electron mobility, which is usually extracted using methods such as the Y-function [45] and the CV-split methodology [46]. These procedures require the evaluation of charge density in the channel in the inversion regime via capacitance-voltage measurements. However, the presence of strong poly-depletion in our devices prevents this, making electron mobility extraction via DC methods impossible. Moreover, these extraction methods also require relatively long-channel devices. Since the stressor technique is most effective for short-channel devices, as SiGe relaxes the most when almost fully amorphized, analyzing long-channel devices would yield mobility values that do not align with those observed in the 40-nm devices. However, a preliminary evaluation of the presence of strain and the resulting enhancement of mobility can be done by studying G_m at different gate lengths, as it is expected to increase more when L_G is reduced for strained-SOI devices. The maximum G_m as a function of L_G is shown in Fig. 3.29a. The results indicate that strained-SOI devices consistently have higher transconductance values than their silicon reference counterparts. Even when compared to the 1.2 µm values, Gm in devices with the SiGe stressor technique is higher than in the silicon-only sample (Fig. 3.29b). These features do not constitute definitive proof of the presence of strain within the devices or the effectiveness of the stressor method. However, they clearly show that transconductance is always better in devices where the SiGe layer is present.

To summarize, from the comparison of PT, AC, and DC data of the POR, reference samples, and those with SiGe, it emerged that the modifications made to the standard process have significantly degraded the performance of the devices due to the evident



(a) **(b)**

Fig. 3.29.: a) The maximum G_m values at each gate length for the strained-SOI devices are compared to the values of the silicon reference. b) The values reported in a) have been divided by the G_m value extracted at long channel (L_G = 1.2 µm). The transconductance characteristic appears to be always higher in the sSOI samples rather than in the SR.

phenomenon of poly-depletion caused by poor dopant activation in the poly-gate. Despite this, all tested devices were functional, demonstrating that the integration of a SiGe layer within the SOI is feasible. Considering the limitations of the process used, which still requires further optimizations, NMOS transistors with SiGe, when treated with an amorphization step, exhibit higher current and transconductance values compared to their silicon-only counterparts, although the access resistance is higher. Additionally, the transconductance increases more significantly as the channel length decreases. However, as previously mentioned, a direct analysis of mobility is not possible for these samples using the characterization data presented so far. It will be necessary to analyze the RF data in detail. Through the extraction of S-parameters, it is possible to make a precise evaluation of channel resistance (and hence of electrons mobility) isolating it from other factors such as access resistance. RF results will be reported in the next section and will provide a clear idea of the effectiveness of the Localized SiGe Stressor Technique for improving device performance.

3.3.2 RF Results

The data presented in the previous section indicated that, despite a significant decrease in performance compared to POR devices, the use of the Localized SiGe Stressor Technique appears to have enhanced the electrostatic properties of the devices relative to the silicon reference, in particular transconductance. To determine whether there has been an increase in electrons' mobility due to stress contribution, an RF analysis was conducted. This analysis involved measuring the S parameters

of devices with varying channel lengths and subsequently processing them through Bracale analysis [47] to extract the small-signal circuit elements, specifically using data between 10 and 20 GHz.

As previously mentioned, it is challenging to determine in DC whether an increase in device current is due to a reduction in channel resistance (hence an enhancement in electrons mobility) or access resistance. Therefore, the observed increase in G_{m} cannot be directly attributed to an increase in mobility. The RF analysis enabled the separation of the three contributions R_{ON}, R_{D}, and R_{S} for different values of L_{G}, that is the channel resistance and the drain and source access resistances, respectively. Their evaluation has been conducted in cold-FET conditions, that is at $V_{\mathrm{D}} = 0$ V, while V_{G} was set at high values to induce strong inversion in the channel. In this way, the impact of stress on low-field mobility should be visible. The results are reported in Fig 3.30. The values of R_{D} and R_{S} seem not to change with L_{G}, which was expected as they should not depend on channel dimensions. R_{D} values are approximately 1.5 Ω and 1.0 Ω for SR and sSOI samples, respectively, while for R_{S} 1.3 Ω and 0.8 Ω were found for SR and sSOI. This feature shows an opposite

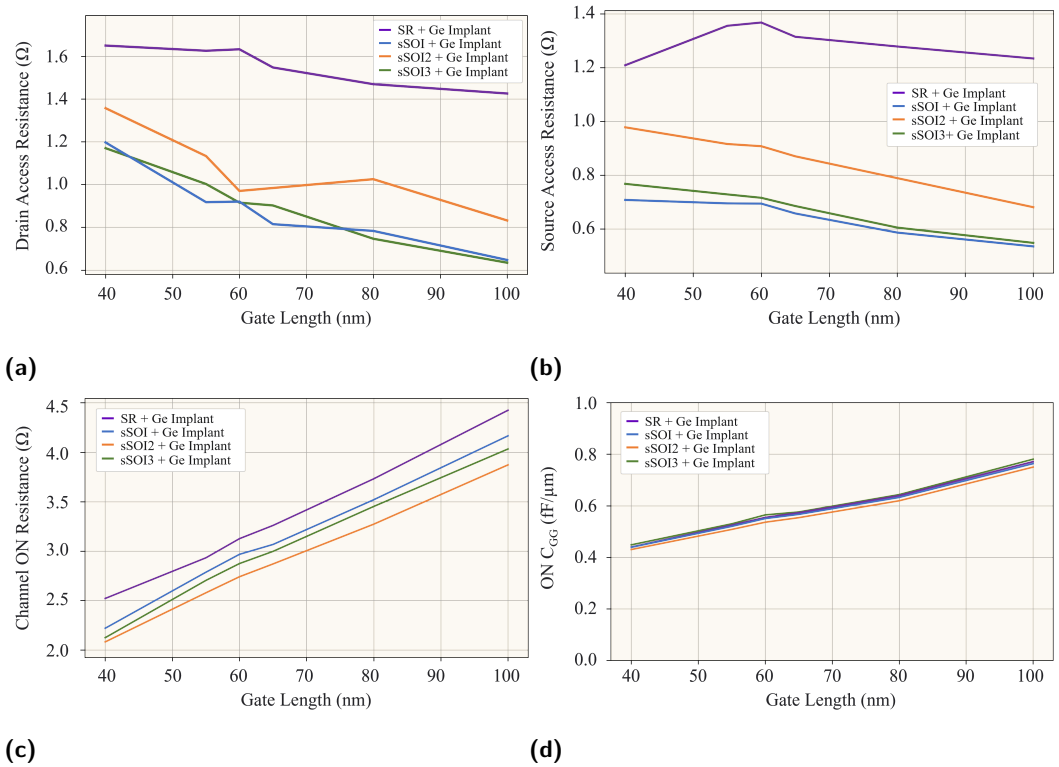


Fig. 3.30.: The elements a) R_{D}, b) R_{S}, c) R_{ON}, and d) C_{GG} of the small-signal circuit extracted by employing the Bracale method are reported as a function of gate length, for both SR and sSOI samples. The extraction was conducted in cold-FET conditions to consider the impact of stress on low-field electrons' mobility.

behavior of what reported in PT as it was shown that S/D sheet resistances were higher for the strained-SOI case. However for the RF analysis, R_D and R_S take also into account the lateral resistances of contacts and LDDs and as we reported an enhanced dopants diffusion due to SiGe we believe that the reduced resistance in sSOI is likely due to the longer extension of LDDs and S/D junctions in these devices.

The channel resistance R_{ON} was obtained as the reciprocal of the conductance G_{DS}. The graph of R_{ON} as a function of L_G shows a general decrease in its value as the channel narrows for all samples. The SR sample consistently shows slightly higher values (about +0.2 Ω).

Despite this result, when comparing the maximum transconductance values in saturation mode, this slight variation in the trend as a function of L_G disappears, and the SR and strained-SOI curves are almost parallel (Fig. 3.31a). Moreover, the substantial increase in transconductance observed in DC is no longer as pronounced in the RF case, and therefore the values of f_T and f_{MAX} derived from it are very similar between the SR case and the strained-SOI case (Fig. 3.31b-c).

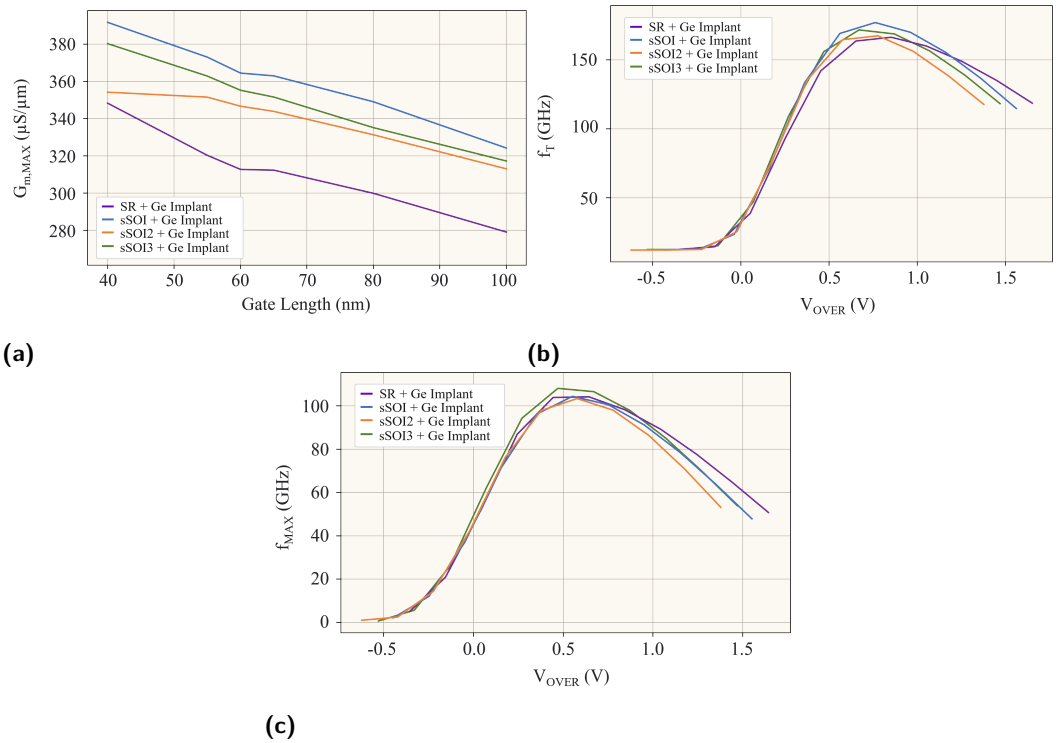


Fig. 3.31.: a) $G_{m,MAX}$ extracted in saturation regime (V_D = 1.0 V) are reported as a function of gate length. In b) and c) the extracted f_T and f_{MAX} at f = 28 GHz as a function of V_{OVER} are shown, respectively. Performance seem to be only slightly impacted by the Localized SiGe Stressor Technique.

The RF data appears to indicate a general equivalence in performance between the two types of samples, suggesting that only a small amount of stress was introduced into the strained-SOI device channel. These conclusions differ significantly from those obtained in the previous section, as the DC and RF characteristics seem to diverge considerably. Notably, the maximum transconductance values obtained in RF are almost 300 S/m and 150 S/m lower than those obtained in DC for the strained-SOI and SR samples, respectively. The reason for this reduction is unclear at the moment, but it is hypothesized that the different test structures used may have influenced the contribution of poly depletion and the new stressor method.

Accurate and unequivocal determination of whether stress has been successfully introduced into the Si channel via the Localized SiGe Stressor Method can only be achieved through PED analysis of the samples. This measurement is essential for both the test structures used in DC studies and the Devices-Under-Test (DUTs) employed in RF studies. Comparing these two sets of measurements could elucidate the significant differences observed between the two data sets, particularly explaining the discrepancies between the G_{m} data obtained in DC and at high frequencies. Additionally, for future iterations of the project, addressing the poly depletion effect is crucial, as it currently limits the potential performance of the devices and complicates the analysis of results.

3.3.3 Summary of Results and Prospects

The basic idea that led to the experimentation of the Strained SOI project was to increase the performance of NMOS devices in CMOS65SOIMMW technology by improving electron mobility through the massive introduction of strain within the Si channel. To achieve this, a commonly known approach known to be 'global', which involves using SiGe beneath the silicon, was modified to become 'local', using it only for individual NMOS devices, thus obtaining what we called the Localized SiGe Stressor Technique. This technique is based on the concept of relaxing a compressed SiGe layer buried in the SOI to induce tensile stress in the overlying silicon, where the transistor channel will be created. However, the effectiveness of this technique has only been demonstrated preliminarily and partially.

In this chapter, an in-depth study was initially reported on how stress transfer occurs from SiGe to the overlying Si following partial amorphization and recrystallization of the SOI / SiGe / Si trilayer structure. The proof-of-concept test conducted on blanket wafers reported significant success, showing ε_{xx} values within the Si-top around 1 %. The importance of this achievement lies in the fact that if this value were

introduced into complete RF devices, performance would undergo a drastic increase, given the theoretical 40 % increase in electron mobility. However, the concept of relaxing the initially compressed SiGe layer alone was not sufficient to interpret the data obtained for this first test, highlighting that other stress phenomena were at play. The application of specific software for studying stress and process steps (Sentaurus sProcess and Comsol Multiphysics) and simultaneously experimenting and physically characterizing samples made it possible to identify a second stress mechanism, given by the presence of dislocations on both sides of the channel, formed during the recrystallization of the amorphized zone. These dislocations do not seem to impact device performance since the missing plane causing a lattice mismatch is oriented towards the BOx and not towards the Si-top where the channel formation occurs. Perfect control of both stress mechanisms, (1) SiGe relaxation and (2) dislocations, would result in a considerable stress contribution within the device, ideally even greater than that obtained for the proof-of-concept test.

While the demonstration of the Localized SiGe Stressor Technique's functionality immediately showed positive and encouraging results, integrating this method within CMOS65SOIMMW proved quite complex. The reason does not lie so much in the type of steps used, which are canonical in semiconductor technology, but rather in adapting the process flow to a SiGe layer within the SOI. Two main problems encountered were reported: the diffusion of Ge outside the SiGe and the diffusion of n-type dopants used for the source/drain junctions into the SiGe layer. Again, the dual approach of experimentation and computational modeling proved successful in explaining the observed phenomena and resolving them. It was demonstrated that a targeted reduction in PNA temperature and Spike post-implantation S/D temperature could resolve the encountered issues while keeping the devices functional.

Despite everything, it was not possible to predict that a slight reduction in the thermal budget used could have a significant and fundamental impact on dopant activation within the poly gate, resulting in the phenomenon of poly depletion. This lack of foresight was due, as previously mentioned, to the computational models' inability to predict the behavior of dopants within polysilicon, given its complex composition and morphology. Highlighted by the measured C_{GG} curves, poly depletion severely limited the performance of the studied devices. The analysis of electrostatic characteristics showed a tremendous decrease in currents compared to POR devices, due to the "virtual" increase in the C_{OX} parameter. Consequently, transconductance and RF figures of merit $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ were also significantly degraded. However, the use of the Localized SiGe Stressor Technique resulted in a notable increase in G_{m} compared to the silicon reference, with a DC measurement increase

of over 30 %. This improvement was not observed in the RF analysis, neither in the G_{m} parameter nor in R_{ON}, that is the effective channel resistance excluding extrinsic contributions such as access resistances. Due to the complexity of data analysis, particularly because of the poly depletion phenomenon, it was not possible to clearly ascertain the presence or absence of stress within the device channels. To obtain a precise and irrefutable answer, PED measurements will be necessary on both DC devices and RF test structures to have clear proof of the strain contribution within the DUTs. This way, we will be able to understand the effectiveness of the presented stressor method and whether there are efficiency dependencies related to the type of structure on which it is implemented.

A comprehensive conclusion of the Strained SOI project requires an additional fabrication iteration, resolving the poly depletion issue. This is possible through the introduction of a poly-silicon doping step followed by a high-temperature Spike anneal before the patterning and gate formation phase. The devices thus obtained would be considered fully functional and free of any issues that could impact their real characteristics and performance. If the PED measures and this latest iteration yield concretely positive results, the Localized SiGe Stressor Technique will be verified as an effective method to enhance the performance of CMOS65SOIMMW devices.

References

[1] K. Uchida et al. “Stress engineering in (100) and (110) nMOSFETs”. In: *2008 9th International Conference on Solid-State and Integrated-Circuit Technology* (2008), pp. 109–112.

[2] F. Gàmiz et al. “Combined effect of mechanical stressors and channel orientation on mobility in FDSOI n and p MOSFETs”. In: *2012 IEEE International SOI Conference (SOI)* (2012), pp. 1–2.

[3] E. Ungersboeck et al. “Electron Inversion Layer Mobility Enhancement by Uniaxial Stress on (001) and (110) Oriented MOSFETs”. In: *2006 International Conference on Simulation of Semiconductor Processes and Devices* (2006), pp. 43–46.

[4] C. D. Young et al. “Critical Discussion on (100) and (110) orientation dependent transport: nMOS Planar and FinFET”. In: *2011 Symposium on VLSI Technology - Digest of Technical Papers* (2011), pp. 18–19.

[5] R. Berthelon et al. “Mechanical simulations of BOX creep for strained FD-SOI”. In: *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon* (2017), pp. 91–94.

[6] C. Sun et al. “Strained Silicon-on-Insulator Platform for Cointegration of Logic and RF—Part I: Implant-Induced Strain Relaxation”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (2021), pp. 1425–1431.

[7] D. Chanemougame et al. “Performance boost of scaled Si PMOS through Novel SiGe Stressor for HP CMOS”. In: *Digest of Technical Papers. 2005 Symposium on VLSI Technology, 2005* (2005), pp. 10.1.1–10.1.4.

[8] C. Ortolland et al. “Stress Memorization Technique—Fundamental Understanding and Low-Cost Integration for Advanced CMOS Technology Using a Nonselective Process”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (2009), pp. 1690–1697.

[9] S. M. Pandey et al. “Mechanism of Stress Memorization Technique (SMT) and Method to Maximize Its Effect”. In: *IEEE ELECTRON DEVICE LETTERS* (2011), pp. 467–469.

[10] K. Y. Lim et al. “Novel Stress-Memorization-Technology (SMT) for High Electron Mobility Enhancement of Gate Last High-k/Metal Gate Devices”. In: *2010 International Electron Devices Meeting* (2010), pp. 10.1.1–10.1.4.

[11] T. Ghani et al. “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors”. In: *IEEE International Electron Devices Meeting 2003* (2003), pp. 11.6.1–11.6.3.

[12] C. Gallon et al. “Mechanical and Electrical Analysis of Strained Liner Effect in 35nm Fully Depleted Silicon-on-Insulator Devices with Ultra Thin Silicon Channels”. In: *Japanese Journal of Applied Physics* (2006), pp. 3058–3063.

[13] K. Mistry et al. “Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology”. In: *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004* (2004), pp. 50–51.

[14] S. Crémer et al. “40-nm RFSOI technology exhibiting 90fs $R_{ON}C_{OFF}$ and f_T/f_{MAX} of 250 GHz/350 GHz targeting sub-6 GHz and mmW 5G applications”. In: *IEEE 53rd European Solid-State Device Research Conference (ESSDERC)* (2023).

[15] P. Chevalier et al. “PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications”. In: *2020 IEEE International Electron Devices Meeting (IEDM)* (2020), pp. 34.4.1–34.4.4.

[16] M.P. Vigouroux et al. “Strain mapping at the nanoscale using precession electron diffraction in transmission electron microscope with off axis camera”. In: *Appl. Phys. Lett.* (2014).

[17] C. Kittel. *Introduction to solid state physics, 7th edition*. J. Wiley and Sons, 1996.

[18] 2020 Sentaurus Process/Device User Manual Synopsys. In: ().

[19] G.L. Olson et al. “Kinetics of solid phase crystallization in amorphous silicon”. In: *Materials Science Reports* (1988), pp. 1–77.

[20] B. Sklenard. “Physical modeling of junction processing in FDSOI devices for 20 nm node and below”. PhD thesis. Micro and nanotechnologies/Microelectronics, Université de Grenoble, 2014.

[21] I. Martin-Bragado et al. “Atomistic modeling of epitaxial growth of semiconductor materials”. In: *Materials Science in Semiconductor Processing* (2016), pp. 223–229.

[22] T. M. Shen et al. “Molecular Dynamic Simulation Study of Stress Memorization in Si Dislocations”. In: *Int. Electron Devices Meet.* (2012), pp. 30.1.1–20.1.4.

[23] Sweden COMSOL Multiphysics® v. 6.1. www.comsol.com. COMSOL AB Stockholm. In: ().

[24] M. Szabadi et al. “Elastic and mechanical properties of ion-implanted silicon determined by surface-acoustic-wave spectrometry”. In: *PHYSICAL REVIEW B* (1998), pp. 8941–8948.

[25] J. Hallstedt et al. “Methods to reduce the loading effect in selective and non-selective epitaxial growth of sigec layers”. In: *Materials Science and Engineering B* (2004), pp. 122–126.

[26] R. Loo et al. “Successful Selective Epitaxial Si1-xGex Deposition Process for HBT-BiCMOS and High Mobility Heterojunction pMOS Applications”. In: *Journal of The Electrochemical Society* (2003), G638.

[27] C. Fellous et al. “Thermal and chemical loading effects in non selective Si/SiGe epitaxy”. In: *Materials Science and Engineering B89* (2002), pp. 323–327.

[28] F. R. N. Nabarro. “Mathematical theory of stationary dislocations”. In: *Advances in Physics* (1952), pp. 269–394.

[29] J. H. Van Der Merwe. “Crystal Interfaces. Part I. Semi-Infinite Crystals”. In: *J. Appl. Phys.* (1963), pp. 117–122.

[30] T. Tsukamoto et al. “Increasing the critical thickness of SiGe layers on Si substrates using sputter epitaxy method”. In: *Journal of Crystal Growth* (2022), p. 126900.

[31] D. J. Paul. “Si/SiGe heterostructures: from material and physics to devices and circuits”. In: *Semiconductor Science and Technology* (2004), R75.

[32] P. Castrillo et al. “Physical modeling and implementation scheme of native defect diffusion and interdiffusion in SiGe heterostructures for atomistic process simulation”. In: *J. Appl. Phys* (2011), p. 103502.

[33] C. Zechner et al. “Silicon germanium interdiffusion in SiGe device fabrication: A calibrated TCAD model”. In: *Mater. Sci. Semicond. Process.* (2016), pp. 230–234.

[34] H. Mullejans et al. “Electron energy-loss spectroscopy (EELS); comparison with X-ray analysis”. In: *JOURNAL DE PHYSIQUE IV* (1993), pp. 2083–2092.

[35] S. Eguchi et al. “On the mechanism of ion-implanted As diffusion in relaxed SiGe”. In: *Applied Surface Science* (2004), pp. 59–62.

[36] S. Eguchi et al. “Comparison of arsenic and phosphorus diffusion behavior in silicon–germanium alloys”. In: *APPLIED PHYSICS LETTERS* (2002), pp. 1743–1745.

[37] A. A. Sharma et al. “Empirical process model for arsenic diffusion in Si1-xGex alloys”. In: *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology* (2010), pp. 956–959.

[38] E. H. Nicollian et al. *MOS (Metal Oxide Semiconductor) Physics and Technology*. J. Wiley and Sons, 1982.

[39] S. M. Sze. *Physics of Semiconductor Devices*. J. Wiley and Sons, 1981.

[40] N. D. Arora et al. “Modeling the Poly silicon Depletion Effect and Its Impact on Submicrometer CMOS Circuit Performance”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (1995), pp. 935–943.

[41] H. Watanabe. “Depletion Layer of Gate Poly-Si”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (2005), pp. 2265–2271.

[42] H. Puchner et al. “An advanced model for dopant diffusion in polysilicon”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (1995), pp. 1750–1755.

[43] S. Jones et al. “Modeling dopant diffusion in polysilicon”. In: *Proc. Simulation of Semiconductor Devices and Processes* (1988), pp. 441–447.

[44] H. Puchner et al. “Dynamic grain-growth and static clustering effects on dopant diffusion in polysilicon”. In: *Proceedings of International Workshop on Numerical Modeling of processes and Devices for Integrated Circuits* (1994), pp. 109–112.

[45] N. Subramanian et al. “Parameter extraction of nano-scale MOSFETs using modified Y function method”. In: *2010 Proceedings of the European Solid State Device Research Conference* (2010), pp. 309–312.

[46] K. Romanjek et al. “Improved split C-V method for effective mobility extraction in sub-0.1-um Si MOSFETs”. In: *IEEE Electron Device Letters* (2004), pp. 583–585.

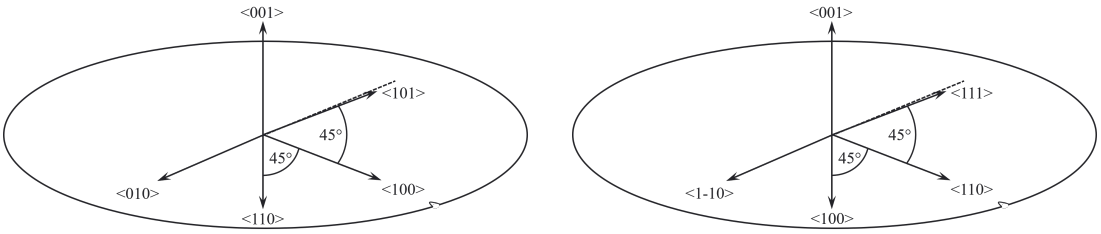
[47] A. Bracale et al. “A New Approach for SOI Devices Small-Signal Parameters Extraction”. In: *Analog Integrated Circuits and Signal Processing* (2000), pp. 157–169.

4

Channel Orientation Project

Similar to the Strained SOI project, the Channel Orientation project aims to enhance transconductance to improve the figure of merits f_T and f_{MAX} of LNA devices, with a focus on carrier mobility. PMOS devices exhibit better performance when aligned along the <100> silicon crystal direction due to the intrinsically higher holes mobility compared to the commonly used <110> direction. In contrast, NMOS device electron mobility is normally independent of the crystal direction due to the symmetry of the silicon crystal, which has six equivalent valleys in conduction band along the (100), (110), and (111) planes. However, when stress is applied, this degeneracy is broken, making electron mobility dependent on the crystal direction [1, 2, 3, 4, 5] (cf. Appendix B). Numerous studies in literature have explored the relationship between induced stress and electron mobility in the inversion layer, particularly under three conditions: uniaxial stress along the <100> or <110> directions, and biaxial stress [6, 7, 8, 9]. In all cases, electron mobility improves under tensile (positive) stress. For the first and third condition, mobility enhancement is due to valley repopulation, which increases electron density in the conduction bands. For the second condition, both valley repopulation and a reduction in electron effective mass contribute to improve mobility [10].

In the CMOS65SOIMMW technology, all devices are fabricated with their channels oriented along the <100> silicon crystal direction [11, 12]. Historically, no stressor techniques were used, making the <100> orientation a straightforward choice to enhance PMOS performance without affecting NMOS devices. Recently, Stress Memorization Technique (SMT) and Contact-Etch Stop Layer (CESL) [13, 14, 15, 16, 17, 18] have been standardized due to their apparent improvements in NMOS performance. SMT involves depositing a nitride layer with intrinsic stress of 500 MPa after the source/drain (S/D) implantation step. The subsequent Spike anneal at 1000 °C expands the polysilicon, which remains positively stressed due to the constrained nitride layer. Some of this stress is transferred to the underlying silicon. CESL directly induces tensile stress in silicon by depositing a nitride layer processed



(a) (b)

Fig. 4.1.: The substrates used for fabricating devices along the a) <100> and b) <110> silicon crystal direction are schematically represented.

by UV light for removing Si-H bonds and obtaining an intrinsic stress of 1.5 GPa, which stretches the silicon lattice underneath.

At the start of this thesis, no comprehensive study had been conducted to verify the presence of stress in the SOI after applying SMT and CESL, nor had the nature of the stress (uniaxial or biaxial) been determined. The Channel Orientation project aims to study the impact of channel orientation on device performance when stressor techniques are employed. To this end, both standard devices with channels oriented along the <100> crystal direction and NMOS transistors oriented along the <110> crystal direction were fabricated, the latter using SOI substrates with the notch aligned along <110> (Fig. 4.1). Some samples were fabricated without SMT or with a less stressed CESL to isolate their contributions to device performance. Aside from the substrate, the standard CMOS65SOIMMW fabrication process was followed. To achieve our goals, parametric tests, DC, and RF data were collected for several samples. These results will be presented and analyzed, supported by mechanical and electrical simulations conducted using Synopsys Sentaurus [19] and COMSOL Multiphysics [20]. These simulations have proven essential in explaining the results and substantiating the hypotheses. They will also be used to propose potential future developments of the study initiated here.

4.1 Electrical Characterization

As for the previous projects, an overview of PT and DC measurements is purchased, for giving an insight into devices' electrostatic behaviors, before moving to the analysis of RF data. In following, the samples fabricated on standard substrate will be reported as POR, that is Process-Of-Reference, while the ones on the rotated wafers, that is with the channel aligned to the <110> silicon crystal direction, are denoted as NewRot.

The main PT values, that is threshold voltage (V_{th}), On current (I_{DS}), and Off current (I_{OFF}), are reported in Fig 4.2. An initial analysis of the data reveals that transitioning from a <100> channel orientation to a <110> channel orientation does not significantly alter the device characteristics. For both channel orientations, the threshold voltage exhibits the typical gradual increase with the decrease of gate length (L_{G}), indicative of the roll-up effect due to the pocket, followed by the roll-off associated with the Short Channel Effect [21, 22]. The roll-up effect appears slightly more pronounced in the NewRot case, likely due to differences in the profiles of the p-type dopants (boron and indium) used in pocket formation, likely due to differences in channeling during implantations [23, 24]. The On currents, which increase with the decrease of L_{G} due to reduced channel resistance, are higher for the NewRot case. However, the different V_{th} values between the POR and NewRot cases should be taken into account. Additionally, I_{OFF} does not vary with the change in orientation.

The On-state currents were further characterized through DC measurements of I_{DS}-V_{GS} curves, with the data reported as a function of the overdrive voltage, $V_{\mathrm{OVERDRIVE}}$, to account for different threshold voltages. The resulting data, shown in Fig. 4.3, indicate that the change in crystalline orientation has no effect on the currents. Analyzing the transconductance curves derived from the I_{DS}-V_{GS} measurements also shows no impact on this property. Therefore, it can be concluded that for the NMOS samples studied, changing the channel orientation does not induce any electrostatic modification, despite the presence of stressors. Any minor differences observed are attributed to variations in dopant profiles.

This conclusion suggests that there is negligible or no stress contribution within the SOI, which prevents the expected mobility increase in the <110> direction. This assertion was verified through measurements conducted on samples without SMT or with CESL with reduced stress. The I_{DS}-V_{GS} and transconductance (G_{m}) data shown in Fig. 4.3 surprisingly indicate that, taking into account a slight variation in V_{th}, for both types of channels, the absence of one of the two stressors does not substantially change the characteristics of the devices, supporting the idea of limited stress presence within the channel.

Another verification of this hypothesis was obtained by analyzing the RF data of the POR and NewRot devices, which allow for the extraction and individual study of each component of the transistors and the determination of the values of the two figures of merit, f_{T} and f_{MAX}. These data were obtained from small-signal measurements of the **S**-parameters performed on devices in floating body configuration, at various drain and gate voltages, in a frequency range between 100 MHz and 40 GHz. The

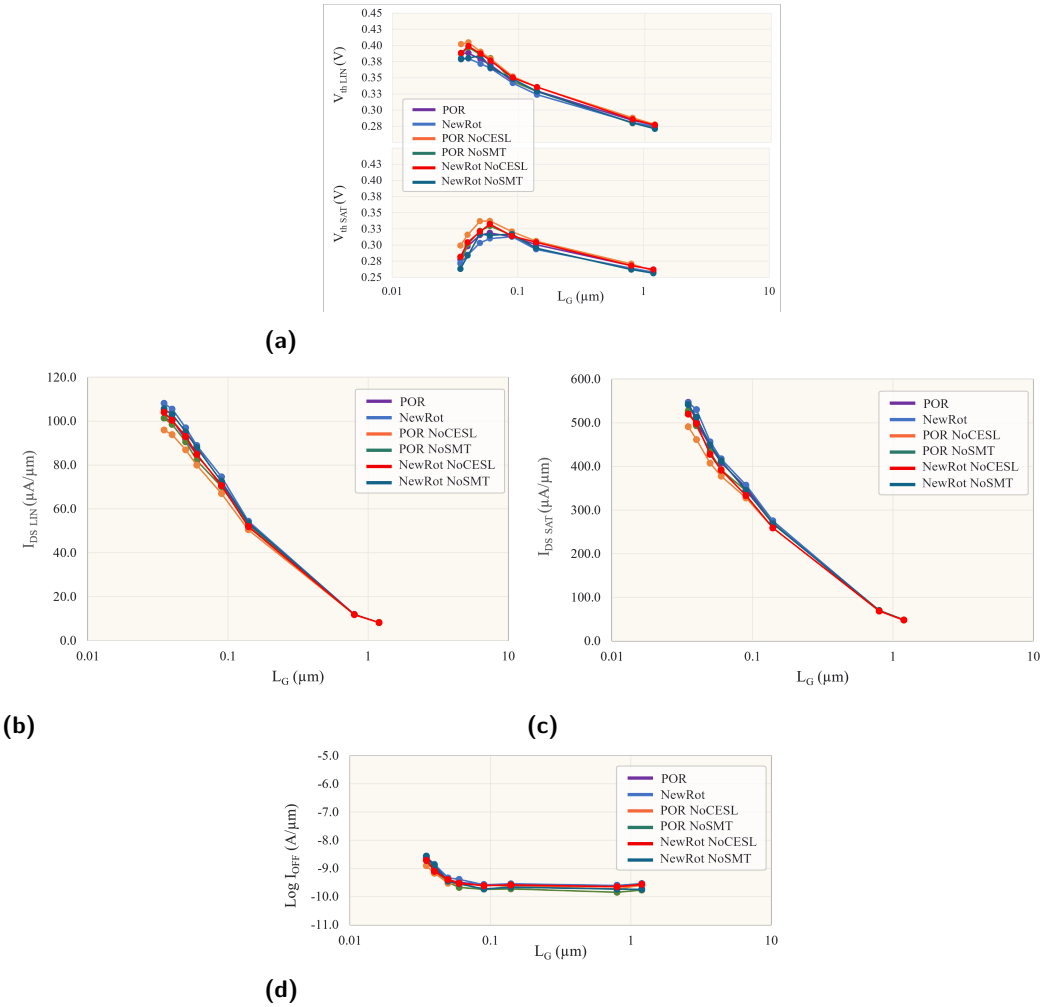


Fig. 4.2.: Results of the parametric tests conducted on standard and NewRot devices at different channel lengths. a) V_{th} vs L_{G} graph for both linear ($V_{\mathrm{DS}} = 50$ mV) and saturation ($V_{\mathrm{DS}} = 1.0$ V) regimes. b) I_{DS} vs L_{G} in linear and c) saturation conditions. d) Leakage current meaured at $V_{\mathrm{DS}} = 1.0$ V and $V_{\mathrm{GS}} = 0$ V. The results show that changing channel orientation and removing stressor methods do not change substantially PT characteristics.

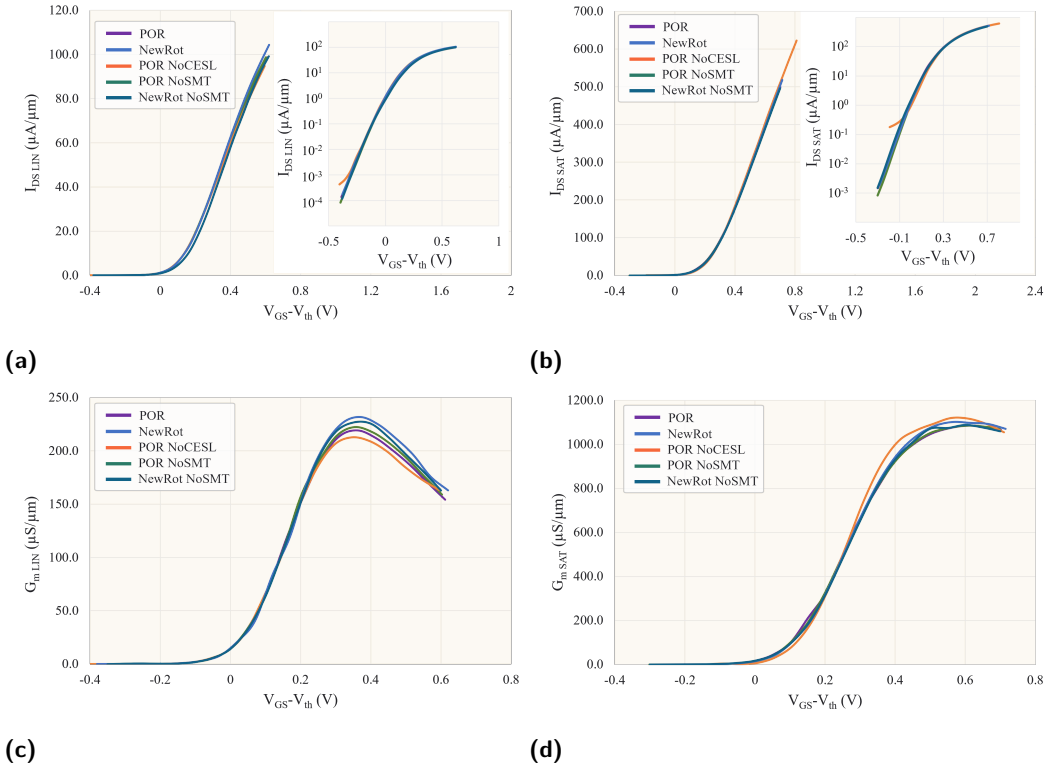


Fig. 4.3.: DC measurements conducted on short channel devices (L_G = 40 nm) on standard and NewRot substrate. a-b) I_{DS}-$V_{OVERDRIVE}$ curves in linear and saturation regime, respectively, with semilog graph as insert. c-d) Corresponding G_m-$V_{OVERDRIVE}$ curves of the overlying I_{DS}-V_{GS} graphs. DC data show a small improvement in G_m when passing from the <100> to the <110> channel orientation.

S-parameters thus obtained were subsequently reprocessed by applying Bracale analysis [25], which makes it possible to extract the elements of the small-signal circuit, starting from the extrinsic elements such as drain and gate pad capacitances (C_{PD} and C_{PG}), contact resistances (gate resistance R_G, drain resistance R_D, source resistance R_S), and inductances (gate inductance L_G, drain inductance L_D, source inductance L_S), to the intrinsic ones such as channel capacitance C_{GG} and G_m (cf. Appendix A). From their extraction, it is then possible to calculate the values of f_T and f_{MAX}. Any increase in mobility for the <110> direction should manifest as an increase in the value of G_m, which, unlike the DC case, is now completely isolated from resistive contributions almost entirely eliminating the erroneous evaluation of its magnitude, and hence impacting the value of f_T and f_{MAX}.

The results obtained for the NMOS transistors that include both stressors are shown in Fig. 4.4 and 4.5. The RF analysis was limited to these two devices (POR and NewRot) since the elimination of SMT and the reduction of the intrinsic CESL

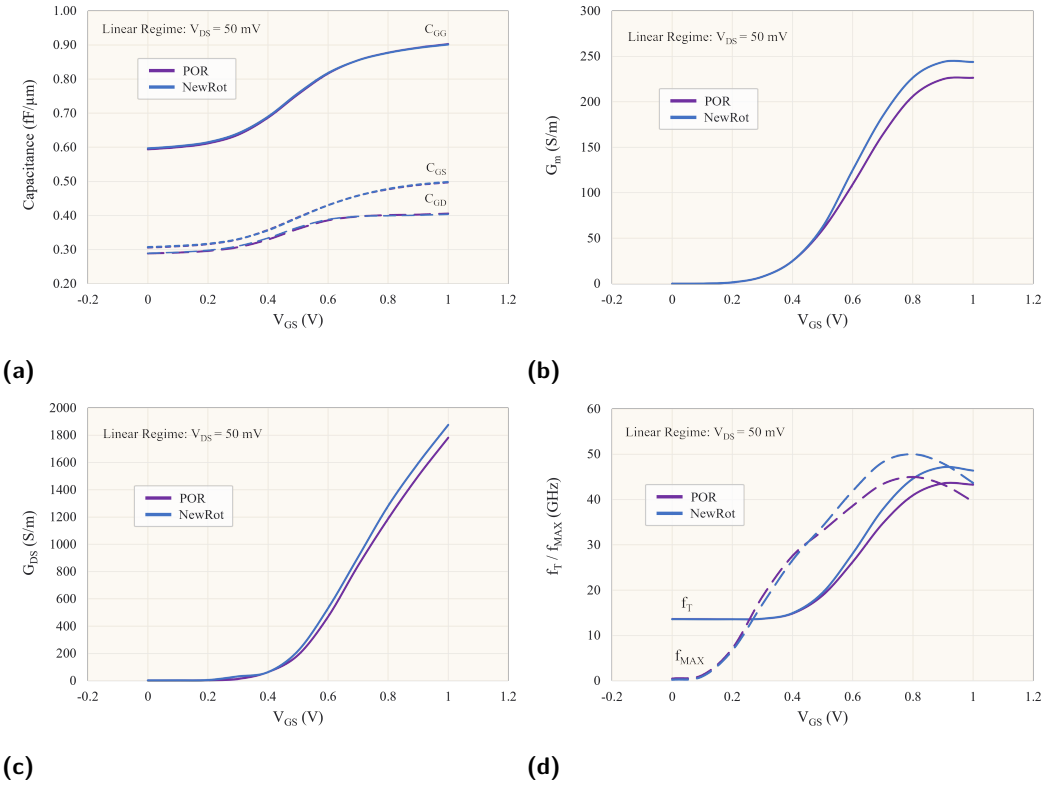


Fig. 4.4.: The RF data extracted from the **S**-parameters analysis at $f = 28$ GHz in low-field regime ($V_{DS} = 50$ mV) are here reported for both POR and NewRot devices. a) C_{GG}, C_{GD}, and C_{GS} curves as a function of the applied V_{GS}. b) G_m-V_{GS} curve. c) G_{DS}-V_{GS} curve. d) RF FOMs f_T (solid lines) and f_{MAX} (dashed lines). In these conditions, a small increase in both G_m and G_{DS} is spotted, with the consequent increase in f_T and f_{MAX} of a few GHz.

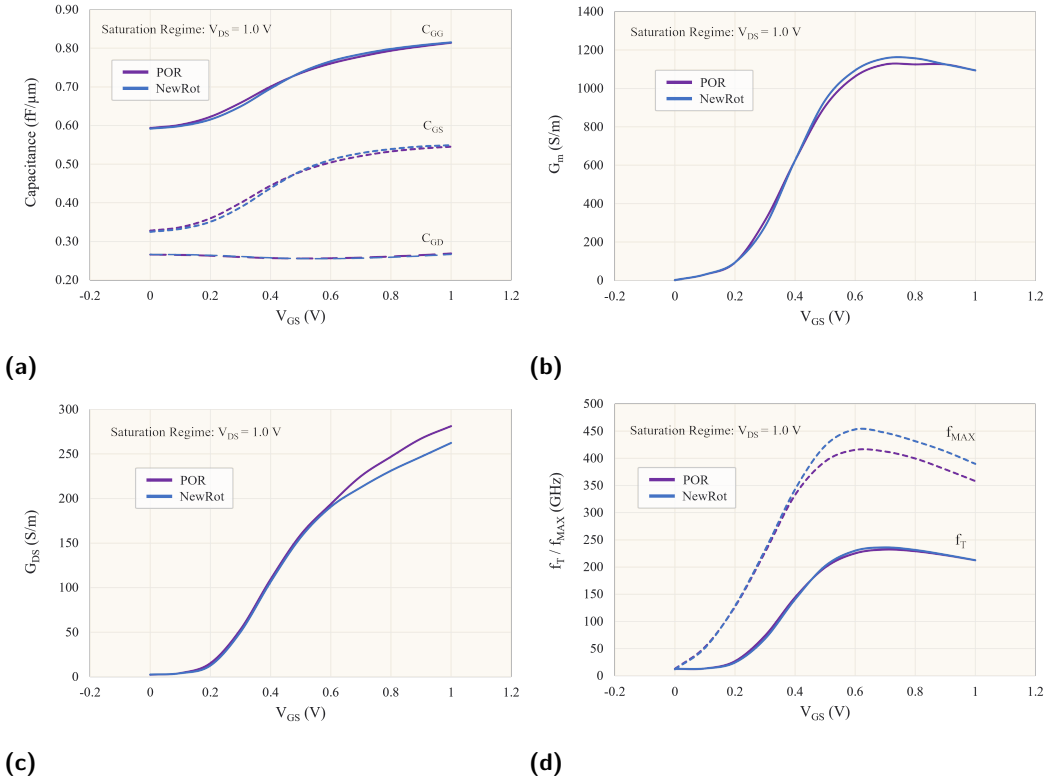


Fig. 4.5.: The RF data extracted from the S parameters analysis at $f = 28$ GHz in saturation regime ($V_{DS} = 1.0$ V) are here reported for both POR and NewRot devices. a) C_{GG}, C_{GD}, and C_{GS} curves as a function of the applied V_{GS}. b) G_m-V_{GS} curve. c) G_{DS}-V_{GS} curve. d) RF FOMs f_T (solid lines) and f_{MAX} (dashed lines). While G_m was found to assume the same values no matter which channel orientation is considered, G_{DS} slightly decreases in NewRot sample, reducing the value of f_{MAX}.

stress from 1.5 GPa to 800 MPa provided electrical results identical to the process standards. The RF data show that in saturation regime similar results of what had already been observed in the electrostatic case are obtained, whereas some differences exist in the linear regime. In the latter case, at $f = 28$ GHz G_{m} passes from 226 S/m to 243 S/m, hence showing an increase of about 16 %, which is also transposed to the f_{T} value. However at $V_{\mathrm{DS}} = 1.0$ V and $f = 28$ GHz, the maximum value for G_{m} was found to assume almost the same value for both POR and NewRot samples, that is 1125 S/m and 1156 S/m respectively. Hence, since C_{GG} did not change when moving from <100> to <110>, the maximum f_{T} did not increased and assume the value of 230 GHz. Only f_{MAX} shows a small improvement of about 6 % moving from 320 GHz to 340 GHz, in particular due to the reduction in conductance, G_{DS}. This change seems hardly related to a variation in the electrons mobility due to the change in channel orientation and it is most likely due to the modification of dopants profiles spotted already in electrostatic measurements.

The collected electrical data have therefore unequivocally shown that for the studied devices, the change in channel orientation did not yield any significant improvement in performance, whether in DC or RF. It is therefore necessary to ask why this modification did not produce the expected results, whether due to a limited amount of stress within the structure or some other effects that has not been observed so far. To answer this question, we used computational models to reproduce the electrical characteristics of the devices and study the transfer of stress from the stressors to silicon. The next section will focus on this topic.

4.2 Simulations Results

To better interpret the results obtained from the electrical analysis, a computational study was conducted in two steps. The first step involved reproducing the fabrication process and the electrical characteristics of the studied devices through TCAD simulations performed in Synopsys Sentaurus. This allowed for the verification of their dependence on channel orientation, the presence of stress, doping profiles, and device geometry. Subsequently, a more in-depth study was conducted on how stress is applied to the structure and in which amount, through mechanical simulations using the COMSOL Multiphysics suite, whose reliability had already been verified at the nanometric level in the previous chapter.

The simulations carried out in Sentaurus were conducted with the 2022.03 version. Although many of the parameters related to material properties are already calibrated by default, such as dopant diffusion models, their activation, and charge carrier

mobility, a calibration of the manufacturing process was necessary to account for some peculiarities of our devices. This calibration was conducted considering the POR devices of all the projects reported in this thesis, in order to have a larger number of samples and increase the accuracy of the simulations. As suggested by the Sentaurus sDevice manual [19], the calibration was carried out as follows: first by reproducing the capacitance-voltage (CV) characteristic of long-channel devices, identifying some characteristics of the gate stack such as the permittivity of the gate oxide, the dopant concentration within the polysilicon, and at the same time, validating the dopant profile within the body (PWELL). Secondly, we focused on verifying the activation of pocket dopants by reproducing the roll-up and roll-off phenomena of the threshold voltage. Finally, the I_{DS}-V_{GS} curves were considered, evaluating a modification of the mobility models used as well as the saturation velocity and the presence of parasitic resistances.

All process simulations were carried out by activating the *AdvancedCalibration* option [19], which includes the diffusion and activation models of dopants listed in Table 4.1. The implantation steps were reproduced through analytical simulations. This choice was made to speed up calculation times, as the comparison between analytical and Monte Carlo simulations did not identify any substantial changes in dopant profiles in the studied devices. Finally, the diffusion steps were performed by simulating the temperature profiles of each thermal treatment above 550 °C. For electrical simulations, the most common models for calculating mobility, recombi-

Tab. 4.1.: Sentaurus models employed during both fabrication process and electrical characteristics simulations.

Simulation Type	Phenomenon	Model
Fabrication Process	Dopants Diffusion	Charged Pair
	Diffusion at Si/oxide interface	Three Phase Segregation (B, As, P)
		Segregation (In)
	Dopants Activation	Transient
Electrical Characteristics	Band Gap Calculation	eQuantumPotential
	Mobility	Enormal
		HighFieldSaturation
		eMultivalley
		eSubband
	Mobility Strain-Dependence	DeformationPotential
		DOS

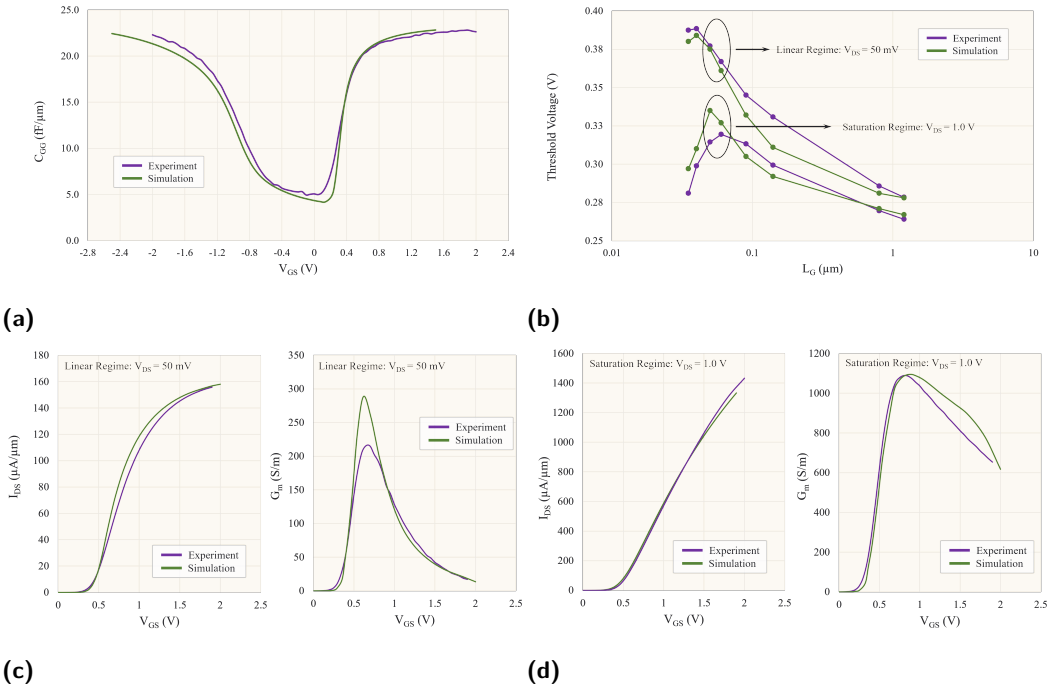


Fig. 4.6.: The comparison between the experimental (in purple) and the calibrated simulation (in green) characteristics is here reported for POR devices. a) Channel capacitance curves as a function of V_{GS}. b) V_{th}-vs-L_G in both linear and saturation regime. c) I_{DS} and G_m curves a function of V_{GS} in linear regime. d) I_{DS} and G_m curves a function of V_{GS} in saturation regime. The graphs show that all characteristics have been well reproduced computationnaly even if G_m in linear regime assumes higher values than what reported experimentally.

nation effects, and saturation velocity were considered and are also listed in Table 4.1.

The experimental CV curve was compared with the simulated ones for which a corrective factor of 1.1 was applied to the boron dose implanted for the PWELL doping (Fig. 4.6a). These curves were obtained considering a doping of 6e20 cm^{-3} within the polysilicon of the gate and an electric susceptibility of 4.24 eV, while the dielectric constant of the oxide was set to 6.0 due to the presence of nitrogen, which raises the value above the standard 3.8 of SiO_2. To reproduce the V_{th}-vs-L_G curves (Fig. 4.6b) the doses of boron and indium used for the pockets have also been modified. For boron, a factor of 1.1 was used again, while for indium it was necessary to significantly reduce the concentration by applying a factor of 0.2.

It should be clarified that these corrections are not real, in the sense that the quantity physically implanted during production is the one formally declared by the recipe used. These corrections mostly aim to phenomenologically consider the possibility that the activation processes of dopants in silicon are different from the models used.

Factors such as the quality of the silicon crystal or the formation of clusters and thus deactivation mechanisms of the dopants are not rigorously considered during simulations, resulting in doping profiles that do not align with experimental ones. That said, it is asserted that an in-depth study of the manufacturing process can certainly lead to an optimal calibration of all the phenomena affecting the dopants, but it was not possible to do so in this thesis due to the limited number of samples produced. Therefore, for all the simulations reported from here on, it was not possible to refine the model parameters, and we limited ourselves to considering these individual corrective factors for each implantation.

Finally, we compared the experimental I_{DS}-V_{GS} curves with the simulated ones (Fig. 4.6c-d). For this last study, no parameters were modified since the data sets were already sufficiently aligned. However, when calculating transconductance as the first derivative of I_{DS}-V_{GS}, Sentaurus fails in reproducing its maximum value in linear regime, while it works quite well in saturation regime. Comparing the simulated results with those obtained experimentally, we can affirm that we have achieved a good degree of reproducibility.

The model calibrated in this way has been used to reproduce the experimental data of devices aligned along the crystallographic direction <110>. The results are shown in Fig. 4.7. The V_{th} values obtained for different gate lengths are quite similar to the experimental one for both linear and saturation regime. The I_{DS}-V_{GS} curves are well reproduced computationally is the case V_{DS} = 1.0 V (Fig. 4.7c), but in linear conditions (Fig. 4.7b) simulations fail in reproducing the experimental observations. Indeed, if experimentally the NewRot sample was found to have a sightly higher current with respect to the POR one, computationally the result is the opposite, even if the difference between the two curves is minimal. Furthermore, in both cases, the simulated sub-threshold slope is steeper than the experimental ones, most likely because of the presence of defects at the silicon-gate oxide interface that have not been reproduced. In general, we can state that the simulations carried out resulted in electrical characteristics similar to the data collected during the DC measurements. However, as will be explained later in this chapter, the slight misalignment between experimental data and simulations is due to the fact that a simple 2D model is not sufficient to best describe the contribution of stress within a 3D structure, and therefore it is not possible to effectively study its effect on mobility.

It should be noted that in the model used the process steps related to the formation of stressors have also been included. The analysis of the structure at the end of the Front-End of Line process reports a total absence of positive stress in the channel

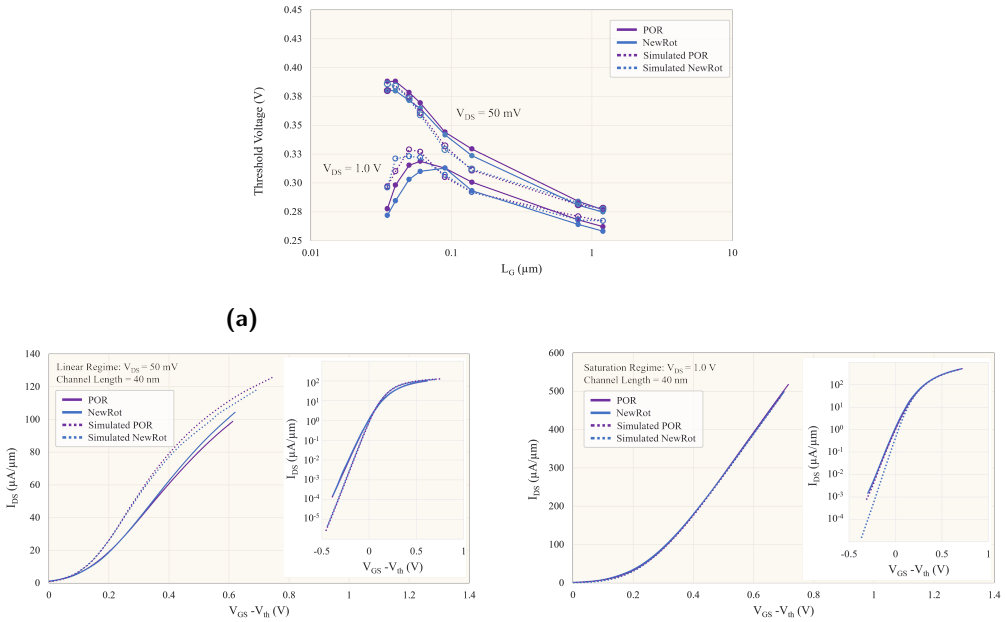


Fig. 4.7.: Experimental and simulated characteristics of the NewRot samples (in blue) are compared to those of the standard ones (in purple). a) V_{th}-vs-L_{G} in both linear and saturation regime. b) $I_{\mathrm{DS}}V_{\mathrm{OVERDRIVE}}$ curves in linear and c) saturation regime for devices with L_{G} of 40 nm. Even if the computational results are in good agreement with the experimental ones, the impact of channel orientation on I_{DS} has not been well reproduced. This behavior is explained further in the chapter.

direction, and indeed a small negative contribution was observed. It is therefore clear that the lack of observed changes in the electrical characteristics related to electron mobility is due to the absence of a strong stress contribution despite the presence of stressors.

This lack of stress is already quite evident when observing the simulated structure shortly after the deposition of the CESL (Fig. 4.8). Indeed, even if a certain limited amount of positive stress along the x-direction (σ_{xx}) is present within the channel (amounting to about 150 MPa) once the nitride layer with an intrinsic tensile stress of 1.5 GPa is deposited, this component disappears when the CESL is etched for the creation of contacts. These simulations, however, should be considered simplifications of what actually happens in a device since they were conducted with a 2D approach and the contacts are not defined as trenches but rather as holes in the CESL. This concept is visualized through Fig. 4.9 that shows the geometry of a CMOS65SOIMMW device with $L_{\mathrm{G}} = 40$ nm.

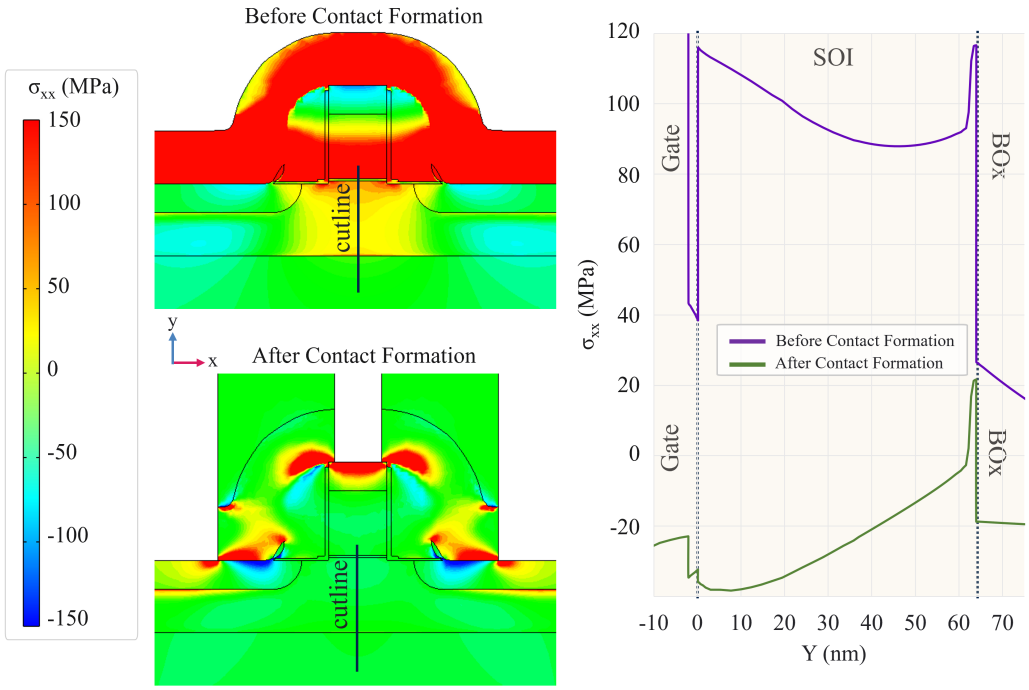


Fig. 4.8.: The effect of CESL on the amount of stress inside the structure was simulated by 2D TCAD simulations. In the left images the stress along the x-axis is shown (top) after CESL deposition and before contact opening and (bottom) after contact formation. On the right, the graph reports the value of σ_{xx} along the cutline shown in the figure before and after the etching process for the formation of contacts. If the stress input via CESL is already very low initially, it disappears completely once the contacts are formed.

So, if it is true that the formation of contacts completely eliminates the tensile stress contribution of the CESL, it is also true that this does not occur along the entire channel but only at specific points. To effectively study the distribution of stress during the formation of contacts, the use of COMSOL is essential if one wants to mechanically study the structure with a 3D approach. Given the invariance of the experimental data with and without SMT and the computational difficulty in reproducing the behavior of polysilicon due to numerous factors that limit the reproduction of thermal effects (one of which is the size of the crystalline grains), in the next discussion only the presence and role of the CESL have been thoroughly investigated.

The COMSOL simulations were carried out considering only a portion of W_G = 500 nm compared to the entire device' width, applying relaxation constraints to all four sides of the structure to reproduce the presence of the Shallow Trench Isolation. The mechanical behavior of the CESL was reproduced by applying the isotropic properties of amorphous SiN, with a Young's modulus of 250 GPa and a Poisson

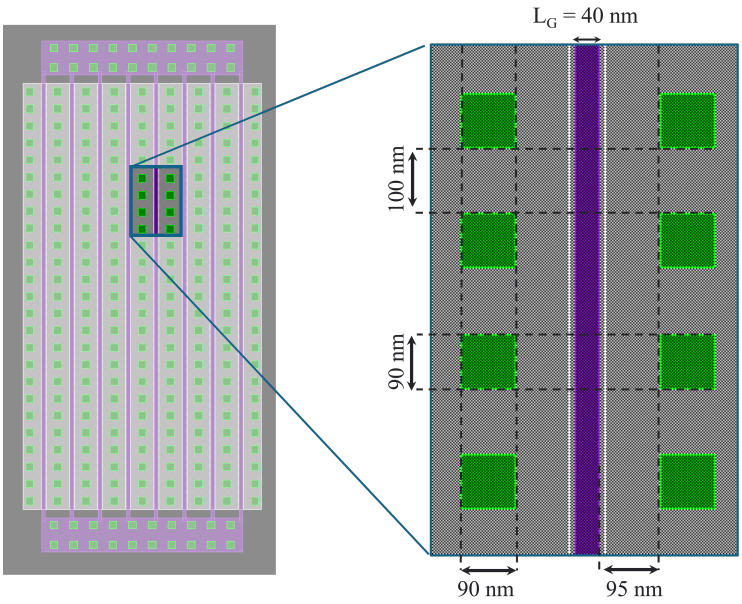


Fig. 4.9.: The simplified CAD design of a typical RF test structure is reported here. The active region is shown in grey, while the polysilicon and contacts are highlighted in purple and green, respectively. As can be seen, the contacts are not formed by patterning a continuous trench, but rather by opening equally spaced holes.

ratio of 0.23 [26]. The underlying silicon was instead applied with the matrix of the cubic crystal elastic elements [27]. To reproduce the effect of the contacts, some areas of the CESL were removed, with dimensions of 90x90 nm^2 and spaced by 100 nm, as in the case of the fabricated structure. Finally, an initial uniform stress of 1.5 GPa was applied to the CESL in all three directions x, y, z. The results of the studied structure are shown in Fig. 4.10-4.11.

The mechanical simulation reports that for the study of stress content the structure can be divided into two portions parallel to the x-y plane (Fig. 4.11). A first one where the entire CESL has been kept (in figure the "NoContact Region") and a second one where the contacts have been created (the "InContact Region"). The former shows results similar to those obtained in TCAD before the formation of the holes. In this case, the stress along the x-axis within the channel reaches values around 110 MPa and then decreases slightly as it approaches the SOI/BOx interface. For the other portion, within the SOI a tensile stress results below the gate that does not exceed 100 MPa, from the channel to the interface with the BOx. As demonstrated in Sentaurus (Fig. 4.8), after creating holes for contact formation, the CESL is free to relax without constraints, thereby reducing the stress applied to the underlying silicon. Notably, there is a difference in results between the etched CESL in 3D and 2D approaches. In the 3D case, a certain level of positive stress is maintained,

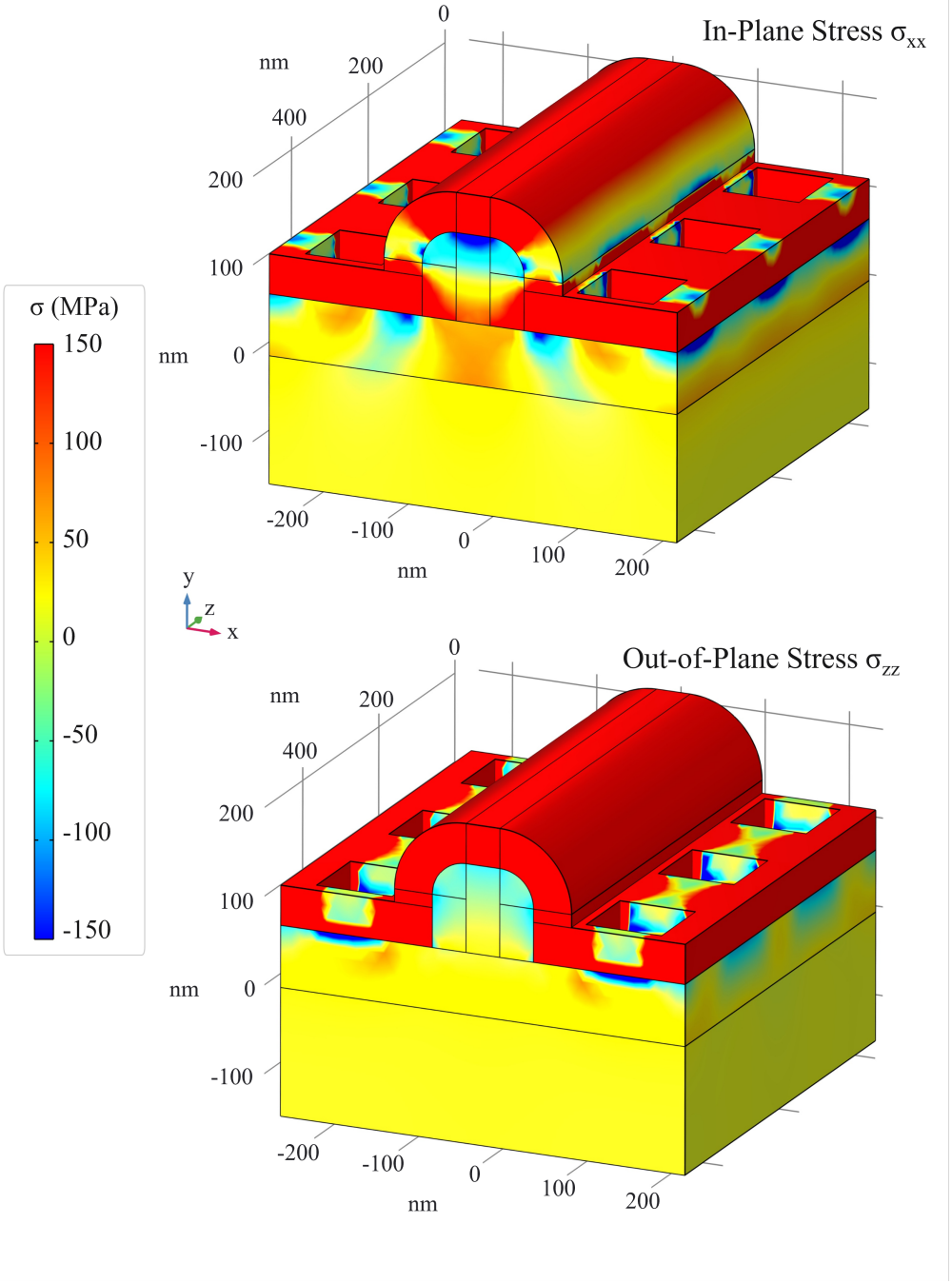


Fig. 4.10.: The stress contribution of the CESL was studied through 3D COMSOL simulations. On the top, the structure shows the in-plane stress, i.e. along the x-direction, while on the bottom, the structure shows the out-of-plane stress, i.e. along the z-direction. If on one hand the stress along the z-axis is almost completely zero, on the other, the in-plane stress assumes positive values despite the etching of the CESL for contact formation.

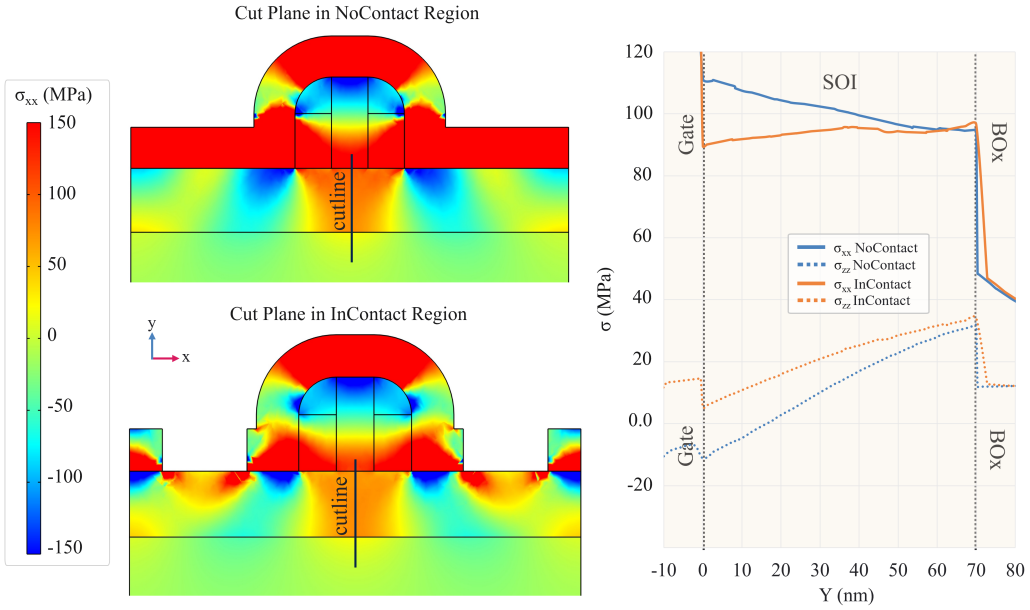


Fig. 4.11.: The COMSOL result for σ_{xx} is studied here by forming two slices, one within a region of the structure with intact CESL (NoContact, in blue) and the other for a region with etched CESL (InContact, in orange). The graph on the right reports for both cases σ_{xx} and σ_{zz} obtained along the highlighted cutline. A reduction of σ_{xx} occurs when the CESL is partially etched for the formation of the contacts. This stress assumes extremely low values even keeping the SiN layer intact, not exceeding 0.11 GPa which is equivalent to approximately 0.1 % of strain in the silicon.

whereas in the Sentaurus simulation, this positive stress is completely lost, and a degree of negative stress appears. It is believed that this negative stress contributes to the misalignment of the electrical characteristics between Sentaurus simulations and real cases in the linear regime. However, as shown by COMSOL simulations, this negative stress is merely an artifact. Ultimately, the almost complete absence of positive stress within the structure is confirmed. Finally, along the z-axis of our structure (the direction perpendicular to the channel and the front view of the device), almost no trace of stress was found, beyond a slight compressive contribution of the order of 10 MPa.

The results thus obtained answer both initial questions: firstly, the CESL contributes only uniaxially to the stress within the transistor structure, that is, along the direction of the channel. It is not possible to obtain biaxial stress, with the second axis in the direction perpendicular to the channel and parallel to the SOI/gate oxide interface most likely because of the presence of the gate structure that does not allow the transfer of stress from the CESL to the silicon. Secondly, although the presence of tensile stress is confirmed within the channel and in the direction parallel to it, its

value is very limited compared to what would be expected from the application of a stressor with 1.5 GPa of intrinsic stress. This fact is due both to the presence of etched areas of the CESL that allow a relaxation of the stressor and to the geometry and mechanical properties of the materials used that limit the transfer of stress towards the channel. By converting the stress within the silicon into strain, values around 0.1 % are obtained, which are too small to observe an increase in mobility by varying the channel orientation from <100> to <110>. As reported in [1], a substantial appreciation between these two orientations can be achieved starting from values around 0.45 % of uniaxial strain (almost 400 MPa in silicon). We therefore hypothesize that this is the most suitable explanation to interpret the obtained electrical data.

The COMSOL model developed in this study has been further refined to explore potential strategies for enhancing the effectiveness of the CESL, thereby achieving a tangible increase in electron mobility. Various options were considered, including increasing the CESL's intrinsic stress, its thickness and its elastic constant. If we take intrinsic stress content as an example (Fig. 4.12), it must be increased to at least 6 GPa to achieve a stress value of at least 400 MPa within silicon. Reaching such a high stress level within a SiN layer is challenging due to the risk of material fractures, and other strategies are similarly difficult to implement. We believe

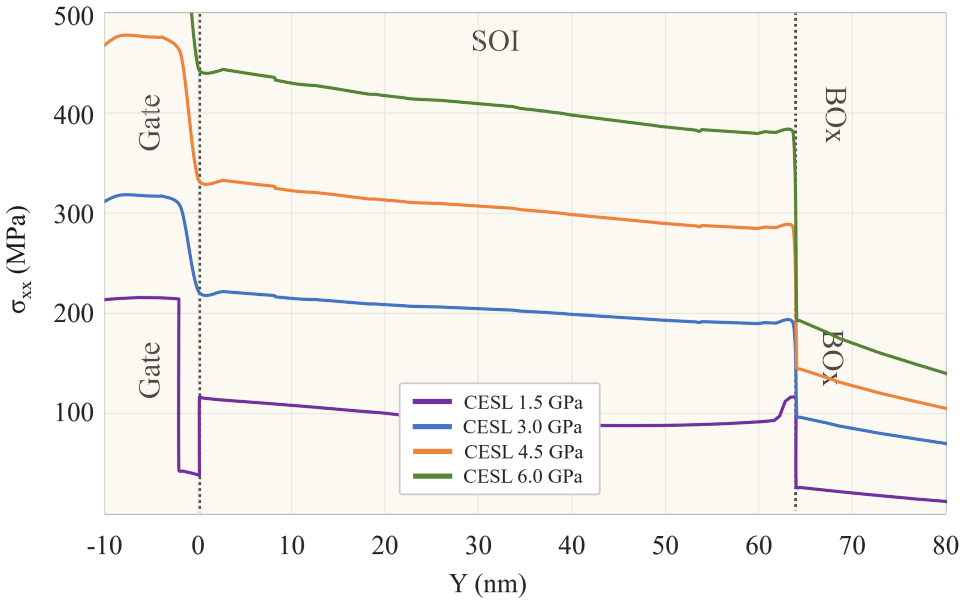


Fig. 4.12.: COMSOL simulations have been conducted with different intrinsic stress in CESL. The σ_{xx} profiles obtained underneath the gate, for portions of the structure where CESL has not been etch, are reported

that the most feasible method is to increase the thickness of the CESL. However, simulations have not shown a significant increase in stress within the SOI using this approach. If these findings will be validated through experimental studies on similar devices, the results presented in this thesis would once again underscore the limited effectiveness of local stressors in significantly boosting the performance of NMOS devices.

4.2.1 Summary of Results and Prospects

The Channel Orientation project aimed to investigate the impact of changing the direction of the NMOS device channel on transistor performance. The fundamental concept was to leverage the higher electron mobility along the <110> direction of silicon under stress, achieved through the use of CESL and SMT. However, a comparison of the DC and RF electrical characteristics of devices with two different orientations did not reveal a significant change in transconductance and RF figures of merit. Additionally, the absence of the SMT or the reduction of stress in the CESL did not negatively impact device performance, which remained nearly identical.

Electrical and process simulations using Sentaurus and COMSOL provided insights into these results. The use of local stressors, which rely on the deposition of intrinsically stressed layers to induce stress in silicon, appears to be less effective than anticipated, even if both stressor techniques have been widely used in CMOS 40-nm (CESL and SMT) and CMOS 65-nm (CESL only) technologies. Specifically, in the case of CESL, it was found that only 10 % of the stress present in the nitride layer is transferred to the underlying silicon. This was demonstrated through both 2D and 3D simulations, showing that for a nitride with 1.5 GPa, the stress within the transistors is uniaxial and only 100 MPa. This value further decreases following the partial etching of the layer for the formation of contacts. The resulting stress translates to a strain of 0.1 % in silicon, which is insufficient to induce a difference in mobility between the <100> and <110> directions. To achieve significant differences and enhance device performance, a strain of at least 0.4 % (equivalent to approximately 400 MPa) is required. Achieving such a value with CESL is challenging. COMSOL simulations indicated the necessity of using layers with thicknesses greater than 100 nm or with intrinsic stress of at least 4 GPa.

These conclusions, however, are currently hypothetical. A definitive conclusion of the project necessitates a precise analysis of the stress within the studied structures, for instance, through PED measurements, to verify the accuracy of the simulations. Additionally, a new iteration of experiments and measurements on fabricated devices,

varying aspects of CESL and SMT (such as thickness and stress), would allow the collection of further data to conclusively assess the effectiveness of these methods. Finally, it is proposed to re-examine the effect of channel orientation using more effective stressor methods.

References

[1] K. Uchida et al. “Stress engineering in (100) and (110) nMOSFETs”. In: *2008 9th International Conference on Solid-State and Integrated-Circuit Technology* (2008), pp. 109–112.

[2] E. Ungersboeck et al. “Electron Inversion Layer Mobility Enhancement by Uniaxial Stress on (001) and (110) Oriented MOSFETs”. In: *2006 International Conference on Simulation of Semiconductor Processes and Devices* (2006), pp. 43–46.

[3] K. Uchida et al. “Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime”. In: *IEEE InternationalElectron Devices Meeting* (2005), pp. 129–132.

[4] V. Sverdlov et al. “Effects of shear strain on the conduction band in silicon: An efficient two-band kp theory”. In: *ESSDERC 2007 - 37th European Solid State Device Research Conference* (2007), pp. 386–389.

[5] H. Irie et al. “In-Plane Mobility Anisotropy and Universality Under Uni-axial Strains in n- and p-MOS Inversion Layers on (l00), (110), and (111) Si”. In: *EDM Technical Digest. IEEE International Electron Devices Meeting* (2004), pp. 225–228.

[6] S. Flachowsky et al. “Mobility and strain effects for <100> and <110> oriented silicon and SiGe transistor channels”. In: *13th International Conference on Ultimate Integration on Silicon (ULIS)* (2012), pp. 5–8.

[7] W. Jiang et al. “Study of electron mobility on silicon with different crystalline orientations”. In: *13th International Conference on Ultimate Integration on Silicon (ULIS)* (2012), pp. 1–3.

[8] T. Matsumoto et al. “Novel SOI wafer engineering using low stress and high mobility CMOSFET with -channel for embedded RF/analog applications”. In: *Digest. International Electron Devices Meeting* (2002), pp. 663–666.

[9] P. Yang et al. “Effects of switching from <110> to <100> channel orientation and tensile stress on n-channel and p-channel metal–oxide-semiconductor transistors”. In: *Solid-State Electronics* (2010), pp. 461–474.

[10] V. Sverdlov. *Strain Effects on the Conduction Band of Silicon. In: Strain-Induced Effects in Advanced MOSFETs*. Springer, 2010, pp. 105–122.

[11] S. Crémer et al. “40-nm RFSOI technology exhibiting 90fs $R_{ON}C_{OFF}$ and f_T/f_{MAX} of 250 GHz/350 GHz targeting sub-6 GHz and mmW 5G applications”. In: *IEEE 53rd European Solid-State Device Research Conference (ESSDERC)* (2023).

[12] P. Chevalier et al. “PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications”. In: *2020 IEEE International Electron Devices Meeting (IEDM)* (2020), pp. 34.4.1–34.4.4.

[13] C. Ortolland et al. “Stress Memorization Technique—Fundamental Understanding and Low-Cost Integration for Advanced CMOS Technology Using a Nonselective Process”. In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* (2009), pp. 1690–1697.

[14] S. M. Pandey et al. “Mechanism of Stress Memorization Technique (SMT) and Method to Maximize Its Effect”. In: *IEEE ELECTRON DEVICE LETTERS* (2011), pp. 467–469.

[15] K. Y. Lim et al. “Novel Stress-Memorization-Technology (SMT) for High Electron Mobility Enhancement of Gate Last High-k/Metal Gate Devices”. In: *2010 International Electron Devices Meeting* (2010), pp. 10.1.1–10.1.4.

[16] T. Ghani et al. “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors”. In: *IEEE International Electron Devices Meeting 2003* (2003), pp. 11.6.1–11.6.3.

[17] C. Gallon et al. “Mechanical and Electrical Analysis of Strained Liner Effect in 35nm Fully Depleted Silicon-on-Insulator Devices with Ultra Thin Silicon Channels”. In: *Japanese Journal of Applied Physics* (2006), pp. 3058–3063.

[18] K. Mistry et al. “Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology”. In: *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004* (2004), pp. 50–51.

[19] 2020 Sentaurus Process/Device User Manual Synopsys. In: ().

[20] Sweden COMSOL Multiphysics® v. 6.1. www.comsol.com. COMSOL AB Stockholm. In: ().

[21] J. P. Colinge. *Silicon-On-Insulator Technology: Materials to VLSI, 3rd Edition*. th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2004.

[22] S. M. Sze. *Physics of Semiconductor Devices*. J. Wiley and Sons, 1981.

[23] V. Raineri et al. "Channeling implants in silicon crystals". In: *Materials Chemistry and Physics* (1994), pp. 105–130.

[24] A. La Ferla et al. "Axial channeling of boron ions into silicon". In: *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms* (1992), pp. 339–344.

[25] A. Bracale et al. "A New Approach for SOI Devices Small-Signal Parameters Extraction". In: *Analog Integrated Circuits and Signal Processing* (2000), pp. 157–169.

[26] Y.C. Chiou et al. "The effect of Young's modulus of contact-etch-stop layer (CESL) stressor on the strained-Si MOSFET". In: *Phys. Status Solidi A* (2012), pp. 1950–1953.

[27] J.J. Wortman et al. "Young's Modulus, Shear Modulus, and Poisson's Ratio in Silicon and Germanium". In: *Journal of Applied Physics* (1964), pp. 153–156.

5

Conclusions and Future Prospectives

The objective of this work was to study the impact that certain modifications applied to the SOI substrate have on the performance of PDSOI NMOS transistors for RF applications in Low-Noise Amplifiers (LNAs) and switches. This study was conducted on devices from the STMicroelectronics CMOS65SOIMMW technology, but the resulting considerations can also be extended and applied to other Partially-Depleted technologies. Three research areas were identified to improve the standard performance of the technology, characterized by f_T/f_{MAX} of 250/350 GHz for NMOS GO1 devices with $L_G = 40$ nm and $R_{ON}C_{OFF}/RFV_{max}$ of 85 fs / 3.2 V for NMOS GO2 devices with $L_G = 0.12$ µm. These areas were named ThinSOI project, Strained SOI, and Channel Orientation.

With the ThinSOI project (cf. Chapter 2), the aim was to study the impact that a thinning of the SOI has on the parasitic capacitances related to the substrate and therefore on the performance of the devices, given the close relationship between these two properties. The work carried out focused on NMOS devices for RF switch applications. It was demonstrated that a progressive reduction in the thickness of the SOI (t_{SOI}) proportionally reduces the so-called inner-fringing parasitic capacitance C_{IF}, in turn reducing C_{OFF} and therefore the $R_{ON}C_{OFF}$ product, which is considered one of the figures of merit for such devices. The best results obtained in terms of $R_{ON}C_{OFF}$ were measured for devices fabricated on 35-nm SOI substrates, achieving values of 68 fs and 74 fs for transistors with $L_G = 0.10$ µm and 0.12 µm, respectively, improving the performance of standard devices on 75 nm SOI by 14 %. For the same devices, RFV_{max} values of 2.7 V and 3.3 V were obtained, constituting a slight improvement over the reference values. In the context of the ThinSOI project, a study was also conducted on how device breakdown occurs, demonstrating that the phenomena attributable to breakdown are Gate-Induced Drain Leakage, triggering of the parasitic bipolar, and punch-through between drain and source. Additionally, the applicability of a method for measuring the RFV_{max} characteristic quickly and reliably on a DC bench was also demonstrated. The ThinSOI project

demonstrated the effectiveness of reducing the thickness of the SOI to increase the performance of RF switch devices. The study also showed that further improvements are possible. Among the various topics planned for the continuation of the project is the fabrication of devices on SOI with a thickness of less than 35 nm, anticipating a reduction in $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ and an increase in RFV_{max}, further improving performance. Additionally, optimization of some characteristics of the fabrication process, such as the implantations used to define the Lightly-Doped-Drain (LDD) and the body (PWELL), is necessary.

The Strained SOI project (cf. Chapter 3) has focused on the topic of strain engineering, which is the branch of semiconductors that studies the relationship between material strain and the electrical properties of devices. An attempt was made to implement a new stressor method to introduce large amounts of strain within the transistor channel for LNA, which involves the use of a SiGe layer within the SOI, dubbed the "Localized SiGe Stressor Technique". To date, the study conducted has only reported partial results. By means of physical analysis, the Localized SiGe Stressor Technique has been demonstrated to be functional for introducing strain in the channel. Indeed, Precession Electron Diffraction measurements reported strain values equal to 0.8 %, which theoretically should ensure an increase of about 50 % in mobility and figures of merit $f_{\mathrm{T}}/f_{\mathrm{MAX}}$. However, the effectiveness at the electrical level of the increase in mobility and thus the performance of the devices has not been observed due to the numerous difficulties related to integration into the manufacturing process. While some issues have been successfully resolved, including the diffusion of Ge outside the SiGe layer and the excessive diffusion within the SiGe by the species forming the source/drain junctions, the latest fabricated and studied samples are affected by a significant problem of poly-depletion, which greatly limits the electrical characteristics of the devices. $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ values of 170/120 GHz have been measured for devices with and without the Localized SiGe Stressor Technique, well below the standard reference values of the CMOS65SOIMMW technology. Therefore, a further modification of the manufacturing process focused on resolving the poly-depletion is necessary. For this purpose, a strategy has already been identified, based on the so-called predoping of polysilicon. The idea is to dope the polysilicon and activate the dopants through anneal once deposited on the wafer and before the formation of the gates. This process, already well known and used in other technologies, should completely resolve the poly-depletion and thus provide fully functional devices. Only at this point will we be able to verify the effectiveness of the presented stressor method.

Always tied to the theme of strain engineering, the Channel Orientation project (cf. Chapter 4) centers its design on the 45° rotation of the silicon substrate, fabricating

devices with a channel no longer aligned with the <100> crystallographic direction of silicon but with the <110> direction. The hypothetical presence of tensile strain within the NMOS devices of the CMOS65SOIMMW technology, resulting from the use of Stress Memorization Technique (SMT) and intrinsically stressed Contact Etch Stop Layer (CESL), allowed for the prediction of performance improvements of these devices when transitioning from one orientation to the other, as described by theory (cf. Appendix B). However, the characterization and comparison of the electrical properties of the two types of samples did not report any improvement. A more extensive study, which included the electrical characterization of devices without SMT or with less stressed CESL and the use of 2D and 3D computational models, resulted in the finding that the two stressor methods were inefficient in introducing significant amounts of strain within the channel. This conclusion, which still needs to be directly verified through physical analysis, could explain the lack of improvement in electrical mobility and RF performance when transitioning to the <110> orientation. To observe a performance increase, some strategies have been conceived through the application of computational models. Among the various prospects for future studies is the increase in the thickness and intrinsic tension of the CESL, which should enhance the strain within the channel. Additionally, an in-depth study on SMT will be necessary to fully understand its stress mechanism and make it more effective.

In conclusion, this thesis reports observations and results from three very different studies in the ways they sought to improve the performance of NMOS PDSOI devices in CMOS65SOIMMW technology, for LNA and RF switch applications. While the ThinSOI project has proven to be effective from the outset, the Strained SOI and Channel Orientation projects have not yet demonstrated the same impact. However, many research avenues remain open from which future work can take shape, continuing the development of the RFSOI field.

A

Small-signal equivalent circuit and the lumped elements extraction

To determine the RF FoMs, **S**-parameters extraction is required. **S**-parameters, or scattering parameters, are the elements of the **S**-matrix obtained when studying the two-port network based on the transmission and reflection of power waves. **S**-parameters are a convinient way of studying an RF component as they permit the extraction of **Z**- and **Y**-parameters at the same time, which at contrary require measurements on open or short circuited port, respectively [1, 2]. From **S**-parameters measurements one can extract all the characteristics of a transistor (capacitances, resistances, transconductance...), analyzing completely the RF device. Doing that means extracting the lumped elements of the so called small signal equivalent circuit of a component.

The small-signal equivalent circuit (SSEC) is an electrical model that represents a transistor device using lumped elements such as resistances, capacitances, and inductances. As the name suggests, this model is applicable only in cases where small signals are applied, thus generating exclusively linear phenomena. A typical

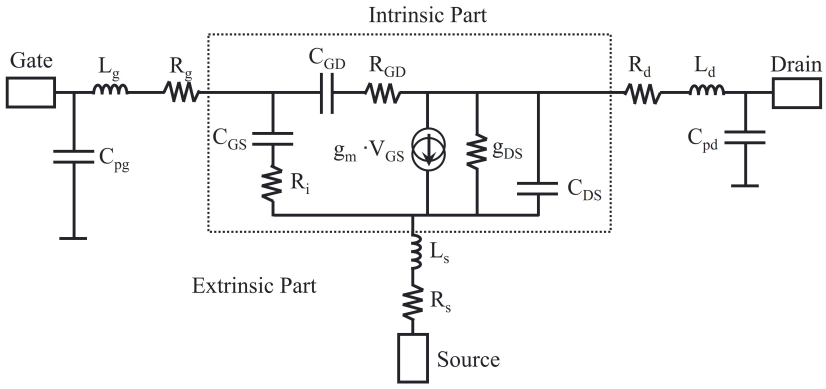


Fig. A.1.: Electrical schematic of the small signal equivalent circuit of an SOI transistor.

SSEC for a transistor is shown in Fig. A.1. This model, reported by Bracale et al. [3], will be used to extract the elements of the transistors analyzed in this thesis.

This SSEC can be divided into two parts: intrinsic and extrinsic. The intrinsic part corresponds to the active area under the gate, where the transistor effect occurs. This includes the gate-to-source and gate-to-drain capacitances, C_{GS} and C_{GD}, and a current source $g_{\mathrm{m}}V_{\mathrm{GSi}}$, which considers the transistor effect, with g_{m} being the transconductance of the device. Moreover, since MOSFETs are not ideal current sources, it is necessary to add a drain conductance g_{DS}.

The extrinsic part is associated with the parasitic elements present in the access areas between the intrinsic part and the metallic contacts that connect the transistor to the rest of the circuit. These elements are considered independent of biasing. The access resistances R_{d} and R_{s} have two main origins: the metallic parts of the access lines and the contact resistances between the metal and the source/drain junctions. The resistance R_{g} is mainly due to the resistance of the silicide deposited on the gate. The inductances L_{g}, L_{d}, and L_{s} represent the reactive effect of the transistor connections. Finally, the capacitances C_{pg} and C_{pd}, called pad capacitances, are due to the metallic connections of the transistor. Finally, the capacitance C_{DS} models the proximity coupling between the drain and source wells through the BOx (Buried Oxide) beneath the SOI (Silicon-On-Insulator). This coupling becomes more significant with the reduction of the gate length (L_{G}).

The determination of the elements of the equivalent circuit in Fig. A.1 is done step by step according to a deembedding methodology, which consists of first determining the extrinsic elements and then progressively approaching the intrinsic area [4, 5].

Firstly, the extraction of the C_{pg} and C_{pd} plot capacitances is obtained by nullifying the channel conductivity. To do this, a cold polarization measurement is performed, applying a V_{DS} voltage of 0 V and a V_{GS} voltage much lower than the threshold voltage. The equivalent circuit under these polarization conditions becomes the one represented in the figure. When $V_{\mathrm{DS}} = 0$ V, the gate charge is equally distributed between the drain and source due to the symmetry of the structure, thus $C_{\mathrm{GS}} = C_{\mathrm{GD}} = C_{\mathrm{B}}$. These capacities vary with the channel width W_{G}, while C_{pg} and C_{pd} are considered constant. The $\mathbf{Y}$-parameters of the equivalent circuit are therefore:

$$\begin{aligned} Imag(Y_{11}) &= \omega(C_{\mathrm{pg}} + 2C_{\mathrm{B}}(W_{\mathrm{G}})) \\ Imag(Y_{12}) &= -\omega C_{\mathrm{B}}(W_{\mathrm{G}}) \\ Imag(Y_{22}) &= \omega(C_{\mathrm{pd}} + C_{\mathrm{B}}(W_{\mathrm{G}}) + C_{\mathrm{DS}}(W_{\mathrm{G}})) \end{aligned} \tag{A.1}$$

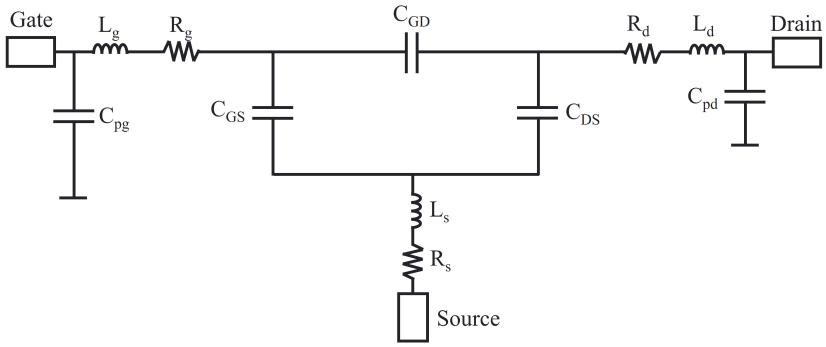


Fig. A.2.: Equivalent schematic of the MOSFET biased at $V_{\mathrm{DS}} = 0$ V and $V_{\mathrm{GS}} < V_{\mathrm{th}}$ with the C_{DS} capacitance that considers the capacitive effect between source and drain through the BOx below the SOI.

If C_{DS} is not considered in the system, the formulas easily provide the expressions for C_{pg} and C_{pd}, that is

$$C_{\mathrm{pg}} = \frac{Imag(Y_{11}+2Y_{12})}{\omega} \qquad and \qquad C_{\mathrm{pd}} = \frac{Imag(Y_{22}+2Y_{12})}{\omega} \tag{A.2}$$

The access resistances are determined using a direct extraction method with cold polarization proposed by Bracale. The equivalent diagram is shown in Fig. A.2.

The expression of the **Z**-parameters of this scheme allows access to the value of the access resistances.

$$\begin{gathered} Real(Z_{11} - Z_{12}) = R_{\mathrm{d}} + f(V_{\mathrm{GS}})/2 \\ Real(Z_{22} - Z_{12}) = R_{\mathrm{g}} + f(V_{\mathrm{GS}}) \\ Real(Z_{12}) = R_{\mathrm{s}} + f(V_{\mathrm{GS}}) \end{gathered} \tag{A.3}$$

Where $f(V_{\mathrm{GS}})$ is given by the physics of the MOSFET transistor in cold biasing:

$$f(V_{\mathrm{GS}}) = \frac{1}{g_{\mathrm{DS}}}\Big|_{V_{\mathrm{DS}}=0V} \qquad \text{and} \qquad \frac{1}{g_{\mathrm{DS}}}\Big|_{V_{\mathrm{DS}}=0V} = \frac{\mu W_{\mathrm{G}} C_{\mathrm{OX}}}{L_{\mathrm{G}}}(V_{\mathrm{GS}} - V_{\mathrm{th}}) \tag{A.4}$$

The resistances R_{g}, R_{d}, R_{s} are the intercepts obtained from a simple regression of $1/(V_{\mathrm{GS}}\text{-}V_{\mathrm{th}})$.

The imaginary part of the **Z**-parameters is given as:

$$Imag(Z_{22}-Z_{12}) = L_{\mathrm{d}} + \frac{C_{\mathrm{GS}}+2C_{\mathrm{DS}}}{4K^2}\frac{1}{(V_{\mathrm{GS}}-V_{\mathrm{th}})^2}$$

$$Imag(Z_{12}) = L_{\mathrm{s}} + \frac{C_{\mathrm{GS}}+2C_{\mathrm{DS}}}{4K^2}\frac{1}{(V_{\mathrm{GS}}-V_{\mathrm{th}})^2} \tag{A.5}$$

$$Imag(Z_{11}-Z_{12}) = L_{\mathrm{g}} + \frac{C_{\mathrm{DS}}(C_{\mathrm{GS}}+2C_{\mathrm{DS}})}{4C_{\mathrm{GS}}K^2}\frac{1}{(V_{\mathrm{GS}}-V_{\mathrm{th}})^2} - \frac{1}{2C_{\mathrm{GS}}\omega^2}$$

Where $K = (\mu W_{\mathrm{G}} C_{\mathrm{OX}})/L_{\mathrm{G}}$ Therefore, L_{d} and L_{s} are obtained with the intercept of the plot of the corresponding imaginary part of the parameter **Z** vs $(1/(V_{\mathrm{GS}}\text{-}V_{\mathrm{th}}))^2$. For the L_{g} case, two steps are necessary: i) a linear regression of Imag(Z_{11}-Z_{12}) vs ${W_{\mathrm{G}}}^2$ is required for different V_{GS} values and ii) a new linear regression for each intercept of step i) vs $(1/(V_{\mathrm{GS}}\text{-}V_{\mathrm{th}}))^2$. The intercept of the second step will give the corresponding value of R_{G}.

As the final step, all that remains is the extraction of the intrinsic elements of the small-signal model. These elements are determined from the expression of the $\mathrm{Y_{INT}}$-matrix:

$$g_{\mathrm{m}} = \left|(Y_{\mathrm{INT21}} - Y_{\mathrm{INT12}})\left(1 + j\frac{Real(Y_{\mathrm{INT11}}) + Real(Y_{\mathrm{INT12}})}{Imag(Y_{\mathrm{INT11}}) + Imag(Y_{\mathrm{INT12}})}\right)\right| \tag{A.6}$$

$$g_{\mathrm{DS}} = Real(Y_{\mathrm{INT22}}) + Real(Y_{\mathrm{INT12}}) \tag{A.7}$$

$$C_{\mathrm{GS}} = \frac{Imag(Y_{\mathrm{INT11}}) + Imag(Y_{\mathrm{INT12}})}{\omega}\left(1 + \left(\frac{Real(Y_{\mathrm{INT11}}) + Real(Y_{\mathrm{INT12}})}{Imag(Y_{\mathrm{INT11}}) + Imag(Y_{\mathrm{INT12}})}\right)^2\right) \tag{A.8}$$

$$C_{\mathrm{GD}} = -\frac{Imag(Y_{\mathrm{INT12}})}{\omega}\left(1 + \left(\frac{Real(Y_{\mathrm{INT12}})}{Imag(Y_{\mathrm{INT12}})}\right)^2\right) \tag{A.9}$$

$$C_{\mathrm{DS}} = \frac{Imag(Y_{\mathrm{INT22}}) + Imag(Y_{\mathrm{INT12}})}{\omega} \tag{A.10}$$

$$R_{\mathrm{i}} = \frac{1}{C_{\mathrm{GS}}\omega}\frac{Real(Y_{\mathrm{INT11}}) + Real(Y_{\mathrm{INT12}})}{Imag(Y_{\mathrm{INT11}}) + Imag(Y_{\mathrm{INT12}})} \tag{A.11}$$

$$R_{\mathrm{GD}} = \frac{1}{C_{\mathrm{GD}}\omega} \frac{Real(Y_{\mathrm{INT12}})}{Imag(Y_{\mathrm{INT12}})} \tag{A.12}$$

The combined use of **S**-parameter measurements and small-signal analysis provides a robust methodology for the characterization, design, and optimization of RF devices. This approach ensures accuracy, efficiency, and high performance in advanced communication and electronic systems. As will be demonstrated in the following chapters, this type of analysis has been extensively applied to conduct an in-depth study of the effects of various process modifications on the characteristics of the devices under investigation, with a particular focus on the LNA devices within the Strained-SOI and Channel Orientation project.

B

Strain Engineering

Applying a force to the surface of any solid results in its deformation, which can alter some of the material's properties. For semiconductors, crystal deformation affects the band structure, thereby modifying the electrical properties, particularly the mobility of charge carriers. In silicon, the types of stress—and consequently strain—that are of most interest to researchers and engineers are uniaxial <100>, uniaxial <110>, and biaxial. This interest stems from the fact that the silicon crystal orientations most commonly used in device fabrication are <100> and <110>. The following sections present the theory linking mechanical deformation to changes in electrical properties, with a focus on how the conduction band and electron mobility in NMOS devices are affected.

The deformation potential theory, developed by Bardeen and Shockley [1] and later generalized by Herring and Vogt [2], describes the influence of strain on the band structure. According to this theory, energy is expressed as a Taylor series in powers of lattice strain, truncated after the terms linear in strain. This approach relates the shifts in energy bands to small deformations of the crystal, as

$$\Delta E(\mathbf{k}) = \sum_{ij} D_{ij}^{(\mathbf{k})} \varepsilon_{ij} \tag{B.1}$$

The band shift is directly proportional to the strain, with the proportionality coefficients D_{ij} forming a second-rank tensor known as the deformation potential tensor. This tensor is a characteristic of a specific non-degenerate band at a chosen point $\mathbf{k}$. Being symmetric, the tensor has only six independent components. In cubic semiconductors, this number is further reduced to three.

Hence, using the linear deformation potential theory, the shift of the conduction band minima under stress in silicon and germanium can be determined. In silicon, the linear energy shift for one of the six degenerate valleys (i = 1, 2, ..., 6) is given by the following expression:

$$\Delta E_c^{(i)} = D_d^{\Delta} Tr(\hat{\varepsilon}) + D_u^{\Delta} \mathbf{a}_i^{\mathbf{T}} \hat{\varepsilon} \mathbf{a}_i \tag{B.2}$$

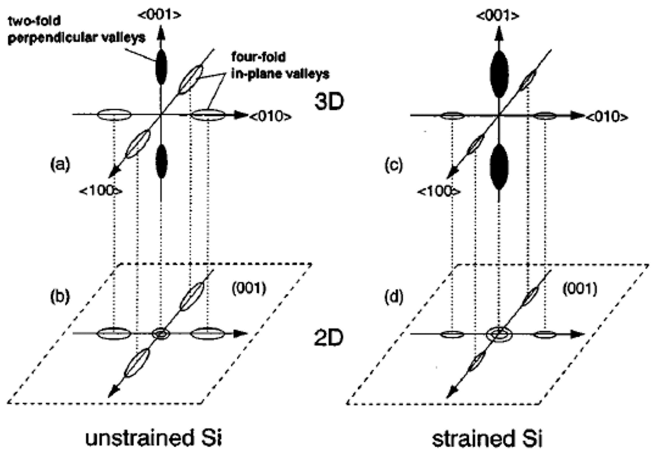


Fig. B.1.: Figure from [5]. Schematic view of the sixfold valley of the minimum of the conduction band in unstrained Si (on the left) and biaxial strained Si (on the right). When the biaxial strain is applied the valleys splits into two groups. In the two-fold valley perpendicular to the plane phonon interscattering decreases and they become more populated.

Where D_{d} and D_{u} denote the dilation and uniaxial deformation potentials, respectively, and $\mathbf{a}_i$ is a unit vector parallel to the $\mathbf{k}_0$ vector determining the minimum position of the valley i.

Using the aforementioned relations, the valley splitting due to stress in any direction can be determined once the strain tensor is known. Uniaxial <100> or biaxial tensile strain cause the sixfold degenerate valleys in unstrained silicon to split into two groups, as illustrated in Fig. B.1. For the former, the group with lower energy is fourfold degenerate, while for the latter, the group with lower energy is twofold degenerate, with the transverse mass parallel to the interface. This leads to [3, 4]

- the suppression of intervalley scattering, resulting from the energy splitting between the twofold and fourfold valleys.
- the decrease in the averaged conductivity mass due to the preferential electron population in the lower-energy valleys, which have a lighter conductivity mass compared to the higher-energy valleys.

A similar discussion can be done for deformation along the <110> silicon direction, even if in this case the uniaxial stress produces an off-diagonal element in the strain tensor, resulting in a shear distortion of the crystal. Under shear deformation, significant changes in the band structure occur. Specifically, due to non-zero values of the shear deformation potential D_{ij}, the degeneracy between the two lowest

conduction bands at the X-points of the Brillouin zone along the [001] axis is lifted. Consequently, for non-zero values of shear stress, an additional energy splitting between the two conduction bands appears at the X-point. This splitting substantially modifies the effective masses in the valleys along the [001] direction, making them functions of the shear stress value.

The $k \cdot p$ theory is a well-established method for analytically describing the band structure [6, 7, 8, 9]. It accurately reproduces the band structure at energies below 0.5 eV, which is sufficient for describing the subband structure and transport properties of advanced MOSFETs. To obtain analytical expressions for energy dispersion within the $k \cdot p$ theory, the [001] direction is considered. Other pairs of valleys can be analyzed similarly. In relaxed silicon, the two conduction bands Δ_1 (i=1) and Δ_2' (i=2) become degenerate exactly at the X-points. Since the minimum of the conduction band is only $k_0 = 0.15 \cdot \frac{2\pi}{a}$ away from the X-point, the dispersion around the minimum is well described by degenerate perturbation theory built at the X-point, which includes only these two bands. The diagonal elements H_{ii} of the Hamiltonian of the strained crystal at the X-point are

$$H_{ii}^0(\mathbf{k}) = (-1)^{i-1}\frac{\hbar}{m_0}k_z p + \frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2 k_x^2}{2m_t} + \frac{\hbar^2 k_y^2}{2m_t} + \delta E_c \tag{B.3}$$

Where i = 1,2, m_0 is the free electron mass, m_t is the transversal and m_l the longitudinal effective mass. In this Hamiltonian, the last term is linked to the presence of the strain-induced shift of both valleys:

$$\delta E_c = D_d(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + D_u\varepsilon_{zz} \tag{B.4}$$

The coupling between the two bands is described by the off-diagonal terms including shear strain [7]:

$$H_{ij}(k) = H_{ij}^0 - D\varepsilon_{xy} \tag{B.5}$$

Where D = 14 eV denotes the shear deformation potential, and

$$H_{12}^0(\mathbf{k}) = \frac{\hbar^2 k_x k_y}{M} \tag{B.6}$$

The parameter M can be determined using $\mathbf{k} \cdot \mathbf{p}$ perturbation theory, finally having $M = \frac{m_t}{1-m_t/m_0}$. By applying degenerate perturbation theory, one can derive the

following dispersion relations for the [001] valleys, incorporating the shear strain component for the two lowest conduction bands:

$$E(\mathbf{k}) = \frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2(k_x^2 + k_y^2)}{2m_t} + \delta E_c \pm \sqrt{\left(\frac{\hbar}{m_0} k_z p\right)^2 + \left(D\varepsilon_{xy} - \frac{\hbar^2 k_x k_y}{M}\right)^2} \tag{B.7}$$

The previous formula indicates that shear strain (ε_{xy}) removes the degeneracy between the conduction bands of the two [001] valleys at the X-point by creating a gap:

$$\delta E_{X[001]} \varepsilon_{xy} = 2D \left|\varepsilon_{xy}\right| \tag{B.8}$$

which is linear in shear strain. As in the previous case, here too a split of the conduction band determines a reduction of the intervalley split and therefore a repopulation of the valleys, increasing the mobility of the electrons.

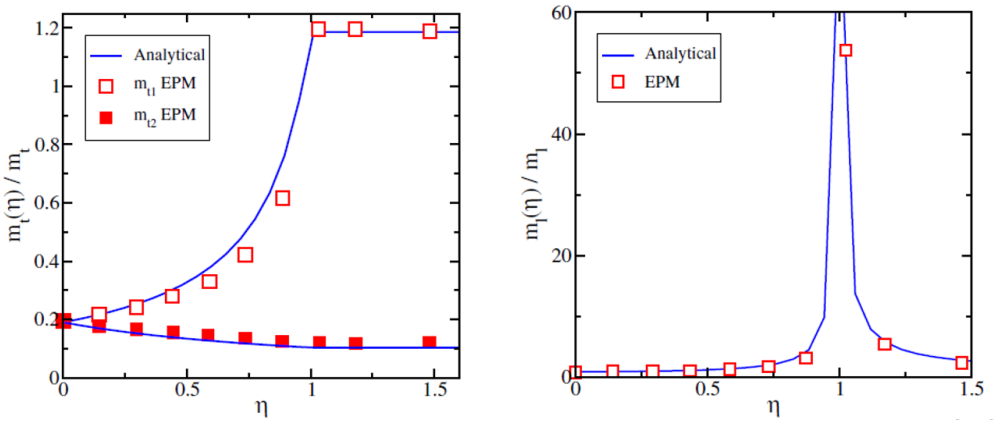
Additionally, a shear strain component ε_{xy} modifies the effective masses of the [001] valleys. By evaluating the second derivatives of equation (1.7), one obtain two distinct branches for the effective masses across (m_{t1}) and along (m_{t2}) the stress direction [8, 9]:

$$\begin{aligned} \frac{m_{t1}(\eta)}{m_t} &= \begin{cases} (1 - \eta\frac{m_t}{M})^{-1} & |\eta| < 1 \\ (1 - sgn(\eta)\frac{m_t}{M})^{-1} & |\eta| > 1 \end{cases} \\ \frac{m_{t2}(\eta)}{m_t} &= \begin{cases} (1 + \eta\frac{m_t}{M})^{-1} & |\eta| < 1 \\ (1 + sgn(\eta)\frac{m_t}{M})^{-1} & |\eta| > 1 \end{cases} \end{aligned} \tag{B.9}$$

Here, $sgn(\eta)$ denotes the sign function of η, that is

$$\eta = \frac{2D\varepsilon_{xy}}{\Delta} \tag{B.10}$$

a dimensionless strain, with $\Delta = 0.53$ eV, that becomes 1 when the strain ε_{xy} makes the minimum of the band coinciding with the X-point. In Fig. B.2a, the analytical expressions for the transverse masses (1.9) are compared with the masses obtained from empirical pseudopotential method (EPM) calculations, showing good agreement between the two data sets. It can be observed that as m_{t1} increases, the effective mass parallel to the direction of the stress decreases, leading to a reduction in the total mass m_c, defined as:



(a) (b)

Fig. B.2.: Figure from [8]. a) The effective transversal masses across (m_{t1}) and along (m_{t2}) the stress direction and b) the effective longitudinal mass (m_l) are reported as a function of the dimensional strain η.

$$m_c = \frac{3}{\left(\frac{1}{m_l} + \frac{1}{m_{t1}} + \frac{1}{m_{t2}}\right)} \tag{B.11}$$

The dependence of m_l on shear strain η can be found analogously [8, 9]:

$$\frac{m_l(\eta)}{m_l} = \begin{cases} (1-\eta^2)^{-1} & |\eta| < 1 \\ (1-1/|\eta|)^{-1} & |\eta| > 1 \end{cases} \tag{B.12}$$

The longitudinal mass becomes infinite, when the valley minimum touches the X-point (Fig. B.2b).

In general, the combined effect of the energy gap and the change in effective masses generates a variation in electron mobility as shown in the figure below. In particular, it is the mobility parallel to the direction of the stress that determines a greater increase.

It is therefore possible to compare the effects of the three strain contributions, as shown in the Fig. B.3. From the image, it is clear how a positive strain improves electron mobility in every case, but the variation among the three cases is significant. For low strain levels, the most effective type results to be the biaxial one. However both biaxial and uniaxial <100> tend to saturate towards a strain value of 0.5 %. On the contrary, the uniaxial <110> case benefits from the reduction of degeneracy, and therefore from less intervalley scattering, but also from a lower effective mass,

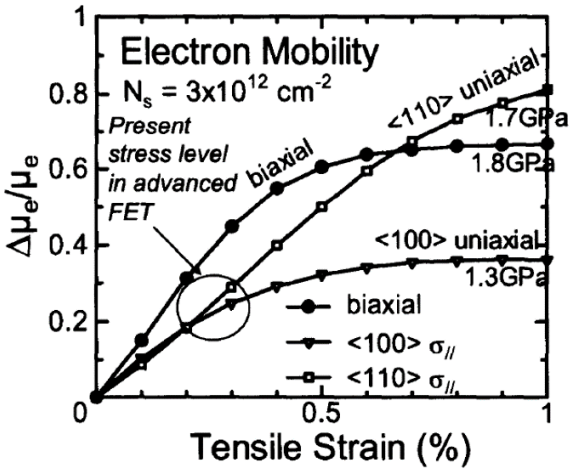


Fig. B.3.: Figure from [10]. The enhancement in electrons' mobility is compared for the three types of strain studied. At low strain level the most beneficial is the biaxial strain, while for high amount of strain, the uniwial <110> results to be the most efficient.

and for this reason, mobility improves and is not subject to any saturation, at least up to strain values of 1.0 %.

References

[1] J. Bardeen and W. Shockley. "Deformation potentials and mobilities in non-polar crystals". In: *Phys. Rev.* (1950), pp. 72–80.

[2] C. Herring et al. "Transport and deformation-potential theory for many-valley semiconductors with anisotropic scattering". In: *Phys. Rev.* (1956), pp. 944–961.

[3] M. V. Fischetti et al. "On the enhanced electron mobility in strained-silicon inversion layers". In: *J. Appl. Phys.* (2002), pp. 7320–7324.

[4] M. V. Fischetti et al. "Monte Carlo simulation of electron transport in Si: The first 20 years". In: *26th European Solid State DEvice Research Conference* (1996), pp. 813–820.

[5] S. I. Takagi et al. "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors". In: *J. Appl. Phys* (1996), pp. 1567–1577.

[6] G. L. Bir et al. *Symmetry and Strain-Induced Effects in Semiconductors*. 1974.

[7] J. C. Hensel et al. "Cyclotron resonance in uniaxially stressed silicon". In: *Phys. Rev.* (1965), A225–A238.

[8] V. Sverdlov et al. “Effects of shear strain on the conduction band in silicon: An efficient two-band kp theory”. In: *ESSDERC 2007 - 37th European Solid State Device Research Conference* (2007), pp. 386–389.

[9] E. Ungersboeck et al. “The effect of general strain on band structure and electron mobility of silicon”. In: *IEEE Trans. Electron Devices* (2007), pp. 2183–2190.

[10] K. Uchida et al. “Stress engineering in (100) and (110) nMOSFETs”. In: *2008 9th International Conference on Solid-State and Integrated-Circuit Technology* (2008), pp. 109–112.

Résumé

La technologie RF CMOS, initialement utilisée pour le Bluetooth et le GPS dans les années 1990, est désormais cruciale pour les réseaux cellulaires dans les smartphones, les PC et les modems WiFi. La transition du 4G au 5G a entraîné la nécessité d'améliorations continues des transistors utilisés dans les modules RF Front End, et le développement du 6G nécessite désormais des LNAs et des commutateurs rentables et performants capables de fonctionner dans la gamme de fréquences des ondes millimétriques. L'objectif principal de cette thèse est d'améliorer les indicateurs de performance clés des dispositifs STMicroelectronics CMOS65SOIMMW PDSOI, ce qui signifie réduire $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ tout en maintenant des valeurs RFV_{max} élevées pour les transistors de commutation et augmenter f_{T} et f_{MAX} pour les transistors LNA. Cela implique de réduire les capacités parasites et d'améliorer la mobilité des électrons par des modifications du substrat SOI. Trois projets ont été entrepris pour atteindre ces objectifs : ThinSOI, Strained SOI et Channel Orientation. Le projet ThinSOI étudie l'impact de la réduction de l'épaisseur de la couche SOI, typiquement de 75 nm, pour améliorer les capacités parasites et la performance des commutateurs RF. Le projet Strained SOI vise à améliorer la mobilité des électrons grâce à l'ingénierie des contraintes en intégrant une nouvelle méthode de tenseur à base de SiGe qui introduit une contrainte de traction significative dans le canal de silicium. Le projet Channel Orientation examine les variations de la mobilité des électrons selon différentes directions cristallines (<100> et <110>). Pour chaque projet, une approche globale a été employée, impliquant la conception d'expériences pour modifier les processus de fabrication et donc les caractéristiques des dispositifs, la modélisation computationnelle pour soutenir et prédire les améliorations et aider à la compréhension des phénomènes physiques et électriques, et la caractérisation des dispositifs pour recueillir des données empiriques.

Abstract

RF CMOS technology, initially used for Bluetooth and GPS in the 1990s, is now crucial for cellular networking in smartphones, PCs, and WiFi modems. The transition from 4G to 5G has driven the need for continuous improvements of the transistors employed in the RF Front End Modules, and now 6G development

requires cost-effective and high-performance LNAs and switches capable of working in the mm-Waves frequencies range. The primary objective of this thesis is to improve key performance metrics of the STMicroelectronics CMOS65SOIMMW PDSOI devices, which means reducing $R_{\mathrm{ON}}C_{\mathrm{OFF}}$ while keeping how RFV_{max} values for switches transistors and increasing f_{T} and f_{MAX} for LNA transistors. This involves reducing parasitic capacitances and enhancing electron mobility by means of modifications of the SOI substrate. Three projects were undertaken to address these objectives: ThinSOI, Strained SOI, and Channel Orientation. The ThinSOI project investigates the impact of reducing the SOI layer thickness, typically 75 nm, to improve parasitic capacitances and RF switch performance. The Strained SOI project aims to enhance electron mobility through strain engineering by integrating a novel SiGe-based stressor method that introduces significant tensile stress within the silicon channel. The Channel Orientation project examines electron mobility variations along different crystalline directions (<100> and <110>). For each project, a comprehensive approach was employed which involved the design of experiments to modify fabrication processes and hence devices characteristics, computational modeling to support and predict improvements and help in the understanding of physical and electrical phenomena, and device characterization to gather empirical data.

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