THESE

Présentée à l'Université de Lille

École Doctorale Sciences de l'Ingénierie et des Systèmes ED-ENGSYS

Pour obtenir le grade de :

DOCTEUR DE L'UNIVERSITE

Spécialité : **Électronique, Microélectronique, Nanoélectronique et Micro-Ondes**

Par

François GRANDPIERRON

Design, fabrication and simulation of next generation robust GaN HEMTs for millimeter wave applications

Conception, fabrication et simulation de HEMTs GaN robustes de prochaine génération pour les applications millimétriques

Soutenance le 17 décembre 2024 devant la Commission d'examen :

Mme. Nadine COLLAERT (Professeur, Vrije Universiteit Brussel)	Rapporteur
M. Jean-Pierre RASKIN (Professeur, UC Louvain)	Rapporteur
M. Didier THERON (DR CNRS, IEMN)	Président de Jury
M. César RODA NEVE (Program manager, SOITEC)	Examinateur
M. Jean-Marc TANGUY (Ingénieur, DGA)	Examinateur
M. Didier FLORIOT (Technical director, Thales)	Invité
M. Farid MEDJDOUB (Chercheur CNRS, IEMN)	Directeur de Thèse

Acknowledgements

Ce travail a été réalisé au sein du groupe WIND, à l'Institut d'Électronique, de Microélectronique et de Nanotechnologie (IEMN) de la Faculté des Sciences et Technologies de l'Université de Lille.

Je tiens à exprimer ma profonde gratitude à mon directeur de thèse, **Dr. Farid Medjdoub**, pour m'avoir offert l'opportunité de mener à bien ce projet et pour la confiance qu'il m'a témoignée tout au long de ces trois années. Son encadrement de grande qualité, sa disponibilité constante, ses conseils avisés et son enthousiasme ont été des éléments déterminants dans ma progression. Je lui suis infiniment reconnaissant pour son expertise et sa passion pour la recherche, qui m'ont permis d'évoluer avec sérénité.

Je remercie chaleureusement **M. Didier Théron**, Directeur de recherche au CNRS, pour avoir accepté de présider cette commission d'examen. J'adresse également mes sincères remerciements à **M. Jean-Pierre Raskin**, professeur à l'Université Catholique de Louvain, et à **Mme Nadine Collaert**, professeur à la Vrije Universiteit Brussel, pour l'honneur qu'ils m'ont fait en rapportant ce travail. Mes remerciements vont aussi à **M. Jean-Marc Tanguy**, ingénieur à la DGA, **M. Didier Floriot**, directeur technique chez Thales, et **M. César Roda-Neve**, program manager chez SOITEC, pour le temps et l'attention qu'ils ont consacrés à l'évaluation de ce travail. Je tiens également à remercier l'ensemble des partenaires et financeurs – SOITEC, SweGaN, ESA, CE, DGA, UMS et C2N – avec qui j'ai eu l'honneur de collaborer dans le cadre de plusieurs projets.

Ces années de doctorat ont été marquées par un environnement de travail exceptionnel, tant sur le plan scientifique qu'humain. À ce titre, je remercie chaleureusement l'ensemble du personnel de la salle blanche pour leur temps et leur aide, ainsi que toutes les personnes impliquées dans la centrale de caractérisation. Je souhaite tout particulièrement remercier **Etienne Okada** pour sa disponibilité, son professionnalisme en caractérisation (et en simulation !) ainsi que sa bonne humeur communicative. Merci à **Timothey Bertrand**, **Saliha Ouendi**, **Pascal Tilmant**, **Marc Dewitte**, **Carlos Moncasi Luque**, **James Elegbe**, **Laurent Fuger** et **Christophe Boyaval** pour leur expertise et leur aide en salle blanche.

Je tiens également à exprimer ma gratitude à l'ensemble du groupe WIND, sans qui ce travail n'aurait pas été possible. Merci à **Kathia Harrouche** pour son accueil, sa patience, sa gentillesse et sa capacité à transmettre son savoir en salle blanche ; à **Élodie Carneiro** pour son aide précieuse en salle blanche, sa gentillesse et son efficacité (même très tôt le matin !) ; à **Lyes Ben Hammou** pour son soutien en caractérisation et sa disponibilité sans faille ; à **Youssef Hamdaoui** pour son aide précieuse et sa bonne humeur quotidienne ; à **Jash Meta** pour ses conseils avisés et les superbes moments partagés ; à **Srisaran Venkatachalam** et **Ajay Shanbhag** pour leur aide dans les projets de simulation et leur bienveillance. Enfin, merci à **Abdelkhalek Sefssafi**, **Manoj Kumar Yadav**, **Tom Micottis**, **Adrien Bidaud** et **Idriss Abid** pour leur grande sympathie au sein du groupe.

Je n'oublie pas mes parents ainsi que mon frère, qui m'ont soutenu tout au long de mes études et de cette thèse. Je remercie également mes plus proches amis – **Glenn**, **Mathieu**, **Margaux**, **Marc**, **Paul**, **Laure** et **Juliette** – pour leur soutien indéfectible, tant durant cette période de travail qu'au quotidien. Enfin, je remercie infiniment **Mélanie** pour son soutien inestimable et pour l'aventure que nous avons vécue, chacun à travers nos thèses respectives. Le plus dur est derrière nous ; il nous reste, ensemble, à poursuivre notre belle aventure.

Abstract

In recent years, significant progress has been achieved with GaN high electron mobility transistors (HEMTs) in advancing the next generation of 5G networks, radar systems, and satellite communications. However, to further enhance power amplification and high-frequency operation (>30 GHz), innovative architectures have been developed. These designs feature reengineered structures, including sub-150 nm gate lengths, thinner barrier layers, or optimized epitaxial layers. Several research groups have demonstrated impressive results, achieving high power-added efficiency (PAE > 50%) with substantial high output power (P_{OUT} > 3 W/mm), across frequency ranges from the Ka-band (30 GHz) to the W-band (94 GHz). Despite these advancements, the reliability of short devices remains a significant challenge due to high electric field, self-heating, and electron trapping effects. This research integrates device fabrication, structural and electrical characterizations, and TCAD simulations to provide cutting-edge insights in this field. One of the most promising technologies, the graded AlGaN channel HEMT has been explored through advanced simulations to better understand its unique properties. Furthermore, an optimized buffer architecture using an AlGaN back barrier and an ultra-thin AlN barrier has enabled state-of-the-art power performance at 40 GHz in fabricated devices. Finally, a novel buffer-free architecture featuring an ultra-thin AlGaN barrier has also been investigated, showing promising results that may rival existing technologies. Short-term reliability tests have been conducted to identify key shortcomings and guide future development.

Résumé

Ces dernières années, des avancées significatives ont été réalisées avec les transistors à haute mobilité électronique en GaN (HEMTs) contribuant à l'évolution de la prochaine génération de réseaux 5G, de systèmes radar et de communications par satellite. Cependant, pour améliorer davantage l'amplification de puissance et les performances à haute fréquence (>30 GHz), de nouvelles architectures ont été développées. Ces conceptions se caractérisent pardes structures repensées avec des longueurs de grille inférieures à 150 nm, des couches barrières réduites ou des couches épitaxiales optimisées. Plusieurs groupes de recherche ont obtenu des résultats remarquables, alliant un rendement en puissance ajoutée élevée (PAE > 50%) à une puissance de sortie élevée (P_{OUT} > 3 W/mm), couvrant des plages de fréquences allant de la bande Ka (30 GHz) à la bande W (94 GHz). Malgré ces progrès, la fiabilité des dispositifs de faibles dimensions reste un défi majeur en raison du champ électrique élevé, de l'auto-échauffement et des effets de piégeage. Cette recherche associe la fabrication et la caractérisation de dispositifs avec des simulations TCAD pour fournir des informations clés dans ce domaine. L'une des technologies les plus prometteuses, le HEMT à canal AlGaN gradué, a été analysée à travers des simulations pour mieux comprendre ce qui en fait une solution unique. De plus, grâce à une architecture de buffer optimisée reposant sur l'insertion d'une couche barrière sous le canal en AlGaN et une barrière ultra-mince en AlN, des performances en puissance à l'état de l'art à 40 GHz ont été atteintes sur les composants fabriqués. Enfin, une nouvelle architecture sans buffer dotée d'une barrière ultra-mince en AlGaN a également été étudiée, montrant des résultats prometteurs qui pourraient rivaliser avec les technologies existantes. La fiabilité à court terme de ces structures a été évaluée afin d'identifier les principaux points faibles et d'orienter les futurs développements.

Table of contents

General introduction

Our society is becoming heavily dependent on electronic devices, which represent a fundamental part of our social infrastructure. However, as concerns about global warming intensify, solutions to reduce our carbon footprint are imperative. To this purpose, considerable effort is being devoted to the development of renewable energies, which has led to increased demand for new power systems. One of the main advances in this field is the replacement of traditional electrical systems with wide-bandgap (WBG) semiconductors, which offer higher efficiency, greater thermal dissipation, and improved performance compared to traditional silicon-based semiconductors.

Due to their low cost and worldwide availability, silicon (Si)-based devices have mainly met the global demand of the microelectronics industry. Silicon-based devices, such as Insulated-Gate Bipolar Transistors (IGBTs) and super-junction Metal-Oxide Field-Effect Transistors (MOSFETs), play a key role in modern electronics as essential components of energy-efficient systems. These devices are an integral part of our daily lives but are reaching their physical limits when it comes to providing the output power required by new technologies, particularly at high frequencies.

III-V semiconductors such as gallium arsenide (GaAs), indium phosphide (InP) or WBG gallium nitride (GaN) have made significant progress in the semiconductor field, offering higher power density, high-frequency converters and faster switching speeds than Si-based devices. Thanks to their superior physical properties, III-V devices such as InP Heterojunction Bipolar Transistors (HBTs) or GaAs High Electron Mobility Transistors (HEMTs) have been favored for the creation of monolithic microwave integrated circuits (MMICs). However, power amplifiers based on InP or GaAs face saturated power level constraints due to their low drain bias operation linked to their low breakdown voltage. To satisfy the requirements of high-power, high-frequency circuits, GaN has emerged as a robust and promising material to replace existing technologies. It offers superior electrical properties, mechanical robustness and the ability to operate at higher temperatures, setting it apart from other semiconductors. One of the key figures of merit of RF GaN devices is power added efficiency (PAE), which defines the energy efficiency of amplifiers and must be maximized as much as possible.

In addition, sufficient output power (P_{OUT}) and improved linearity are essential for GaN technologies. To date, several innovations have demonstrated outstanding performance in the millimeter-wave bands (30-300 GHz). However, widespread adoption of these technologies is still limited by challenges such as trapping effects and device reliability, particularly for devices with short gate lengths.

This work is part of three projects: the AID (Agence Innovation Défense)-CNRS GREAT project, the AGAMI-EURIGAMI project (funded by the CEE under the European Defense Fund), and a contract with the European Space Agency (ESA). It is specifically supported by UMS with two epitaxial suppliers: SOITEC and SweGaN. The overall objective of these projects is to develop a robust GaN HEMT technology on silicon carbide (SiC) substrates for power amplification up to the W-band (94 GHz) for future telecommunication systems, space and military applications. Several objectives have been set to advance and improve high-frequency GaN technologies: **The technology must be robust and capable of withstanding an operating voltage greater than or equal to V_{DS} = 20V. The aim is to simultaneously combine high output power density (P_{OUT} > 3.5 W/mm), power added efficiency (PAE > 55%) while showing strong reliability in sub-150 nm GaN HEMTs**. This thesis work covers the following topics: fabrication and characterization of GaN-based HEMTs for millimeter-wave applications, supported by device simulations. **Figure 1** illustrated the main activities carried out in this frame.

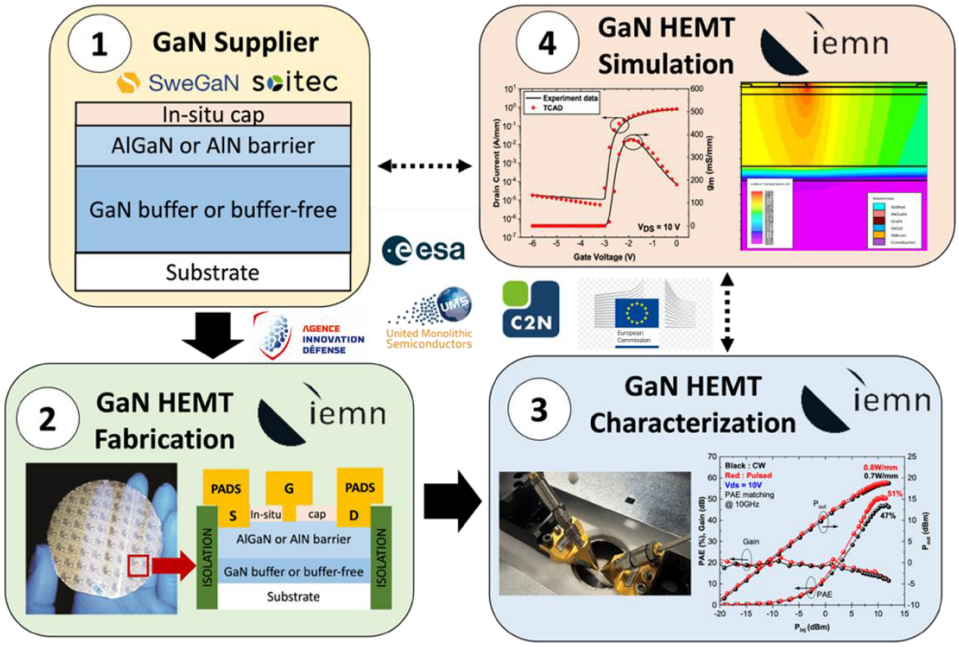


Figure 1. Diagram showing the main activities involved during this work.

This thesis work is organized as follows:

- **STEP 1:** The GaN heterostructures were grown and delivered by the companies SOITEC and SweGaN. We defined the epilayer stacks.

- **STEP 2:** The fabrication of GaN HEMTs is performed using IEMN cleanroom facilities **(50% of the total time)**.

- **STEP 3:** Electrical characterization of GaN HEMTs, including DC, DC pulsed, small-signal, large-signal and reliability measurements, is also carried out at IEMN laboratory **(15% of total time)**.

- **STEP 4:** TCAD simulations were conducted to understand physical phenomena behind the electrical characterizations. Today, GaN simulations are increasingly used to support manufacturers' technology development. A European Space Agency (ESA) project based on TCAD simulation has also been completed in order to investigate the most promising mmW technologies for space applications **(35% of total time)**.

This manuscript is divided into three main chapters:

Chapter 1 introduces GaN HEMT technology and its role in millimeter-wave applications. The overview covers the properties of GaN material and highlights its advantages over other semiconductors. It details the structural elements of GaN HEMTs and the strategies for achieving high performance in the millimeter-wave bands. The chapter examines the characteristics and challenges of GaN HEMTs. It concludes with the current status and progress of GaN technologies in millimeter-wave bands.

Chapter 2 presents the simulation work realized during this thesis, the software used and the methodology developed. We will present the framework of the ESA project and its objectives, as well as the results obtained in this frame. The main technology studied in this project is the graded AlGaN channel HEMT developed by Hughes Research Laboratories (HRL, USA). This technology was chosen for its outstanding performance up to W-band, combined with an excellent linearity.

Chapter 3 details the design optimization, the related fabrication process and subsequent electrical characterization of GaN HEMTs. This research focuses on two distinct GaN structures, both designed for millimeter-wave applications. The objectives are to improve their (power, linearity, PAE) performance and reliability. The first structures study the effects of incorporating carbon into an AlGaN back barrier of AlN/GaN HEMTs. The aim is to understand how carbon doping affects the overall device performance. The next structures explore the characteristics of buffer-free Al-rich AlGaN/GaN HEMTs. This study aims to understand the potential benefits and challenges of the absence of buffer layers in these advanced GaN HEMTs.

This manuscript ends with a conclusion and a presentation of the outlooks of this work.

Chapter 1: GaN-based HEMT technology – Overview

I. Millimeter-wave applications and market trend

In recent years, GaN technology has become key in the millimeter-wave (mmW) bands for multiple applications, thanks to its exceptional material properties. Millimeter waves cover the frequency spectrum from 30 GHz to 300 GHz, between microwaves and infrared (IR) waves. Their wavelengths (λ) range from 1 to 10 mm. **Figure 1.1** shows the entire electromagnetic spectrum, focusing on the bands (Ka to W) of interest within this thesis [1].

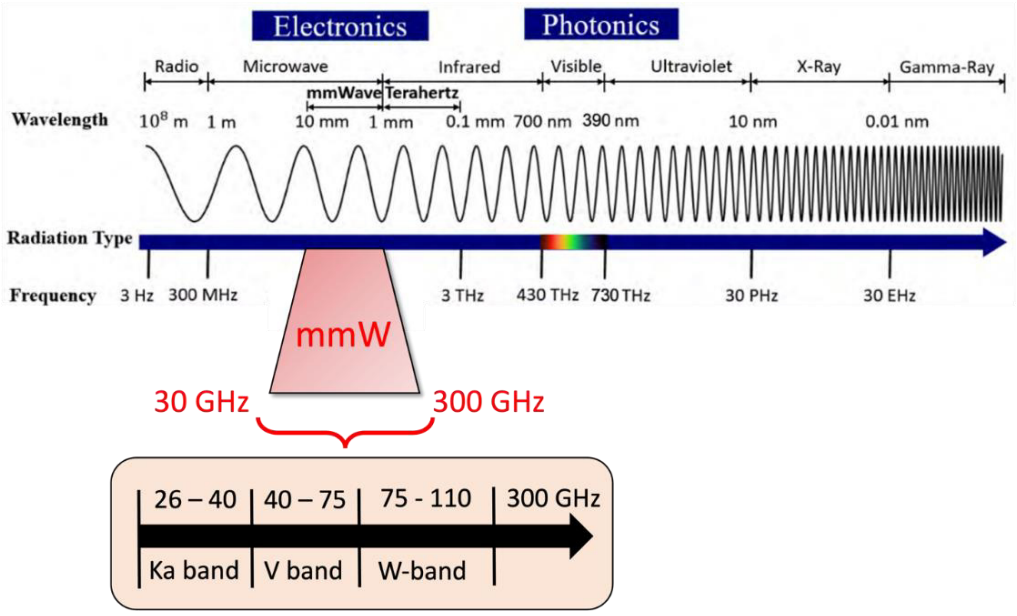


Figure 1.1. Electromagnetic spectrum in frequency and wavelength [1].

Owing to short wavelengths, feeder systems can integrate large antenna arrays into compact physical dimensions. This allows a higher density of antenna elements without increasing antenna size, resulting in narrower beams at mmW frequencies as compared to microwave frequencies. This feature improves the precision and efficiency of high-frequency signal transmission, making mmW technology ideal for advanced communication systems. Microwave monolithic integrated circuits (MMICs) based on III-V semiconductors have become essential to satisfy the millimeter-wave market. MMICs based on InP and GaAs deliver excellent efficiency but rather limited output power due to their low-bias operation, below V_{DS} = 10V, leading to the development of wide bandgap GaN-based MMICs [2-4].

In this context, GaN devices are particularly valuable for mmW applications due to their high electron mobility (~1500 cm2/V.s), high saturation velocity ($2.5.10^7$ cm/s) and remarkable thermal stability. In addition, their high breakdown field (3.3 MV/cm) makes them suitable for applications requiring robust performance under harsh conditions, such as in aerospace, military and defense applications where high power and high temperatures are needed. **Figure 1.2** shows the main sectors where GaN RF devices are typically used.

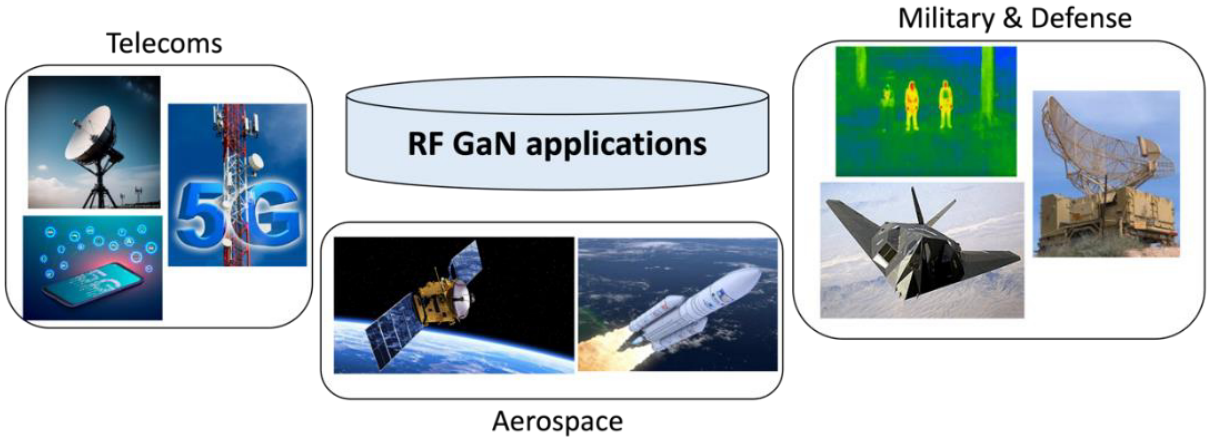


Figure 1.2. Major sectors using RF GaN technology.

In telecommunications, GaN technology significantly improves base stations by enabling both high-power density and high-frequency performance, which is crucial for the development of 5G infrastructures. As macrocells and microcells move from remote radio heads (RRHs) to active antenna systems (AASs), the growing demand for massive MIMO requires more power amplifier (PA) units per base station. GaN's superior efficiency and broadband capability at frequencies above 3 GHz, compared to Laterally Diffused Metal Oxide Semiconductor (LDMOS), offer substantial advantages and opportunities for GaN in this field.

For defense and military applications, GaN remains the cornerstone of many applications such as radar, electronic warfare and communication systems. Systems based on traveling wave tubes (TWTs) are gradually being replaced by GaN technology to enhance national security. GaN improves radar systems by offering better resolution and extended detection ranges for larger surveillance areas. GaN amplifiers are also a game-changer for jamming systems that disrupt enemy communications, and for electronic countermeasures that protect military forces, underlining their strategic importance [5, 6].

For space and satellite communications, GaN's high resistance to radiation makes it an ideal material. It supports communications systems in extreme environmental conditions beyond the Earth's atmosphere, as in satellite transponders, power amplifiers and DC-DC converters. GaN amplifiers are essential for transmitting clear signals over long distances, which is crucial for geostationary and low-earth orbit systems providing services such as high-speed internet and weather forecasting [7].

GaN technology has now been adopted in many parts of the world, thanks to major investments by industry and governments. Its development has grown steadily over the years, particularly in America, Europe and Asia. **Figure 1.3.a** shows some of the main players in GaN technology for high-frequency applications. According to Yole Group [8] and reports from Mordor intelligence [9], the RF GaN market is set for substantial growth, with its value estimated to rise from $1.7 billion in 2024 to $4.03 billion in 2029. One of the fastest-growing sectors is telecommunications, where RF GaN devices are expected to contribute nearly 45% of the total market, exceeding $1.3 billion by 2028 due to the explosive development of 5G infrastructures **(Figure 1.3.b)**.

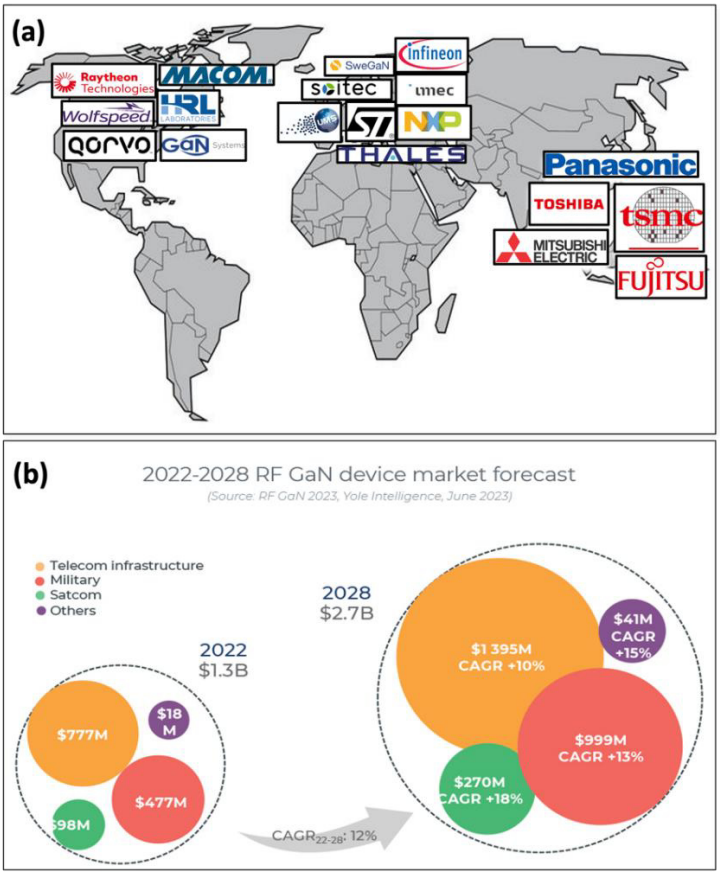


Figure 1.3. (a) RF GaN players and (b) 2022-2028 RF GaN device market forecast [9].

II. GaN material and properties

II.1. GaN crystal structure

III-V semiconductors such as aluminum nitride (AlN), gallium nitride (GaN) and indium nitride (InN) crystallize in three main structures: rock salt, wurtzite (hexagonal) and zinc-blende (cubic). The rock salt structure is not currently used in electronic devices due to its lack of relevant properties. The zinc-blende structure is a thermodynamically metastable polytype of GaN, favored in device applications due to its smaller bandgap and higher carrier mobility. However, at room temperature and atmospheric pressure, the wurtzite form is the thermodynamically stable phase for nitride semiconductors. In this structure, bonding within GaN is predominantly covalent, with each Ga atom forming tetrahedral bonds with four N atoms **(Figure 1.4)**.

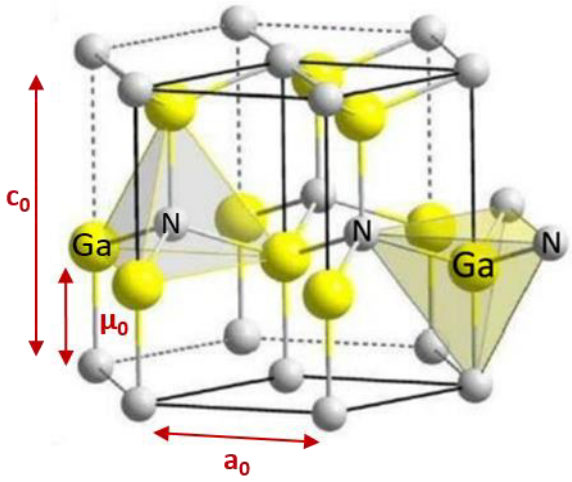


Figure 1.4. GaN wurtzite crystal structure.

The wurtzite form of GaN has a hexagonal crystal structure, with the axial direction of the hexagonal column known as the c-axis. Due to the higher electronegativity of nitrogen compared to gallium, Ga and N atoms exhibit cationic (+) and anionic (-) characteristics respectively, resulting in spontaneous polarization along the crystal orientation [0001]. The wurtzite structure lacks inversion symmetry, which induces two distinct polarities: Ga-face [0001] and N-face [000$\bar{1}$]. For the Ga-face polarity, the N-Ga bond is oriented from the substrate to the surface, starting with the growth of N atoms and ending with a Ga surface, and vice versa for the N-face polarity **(Figure 1.5)**.

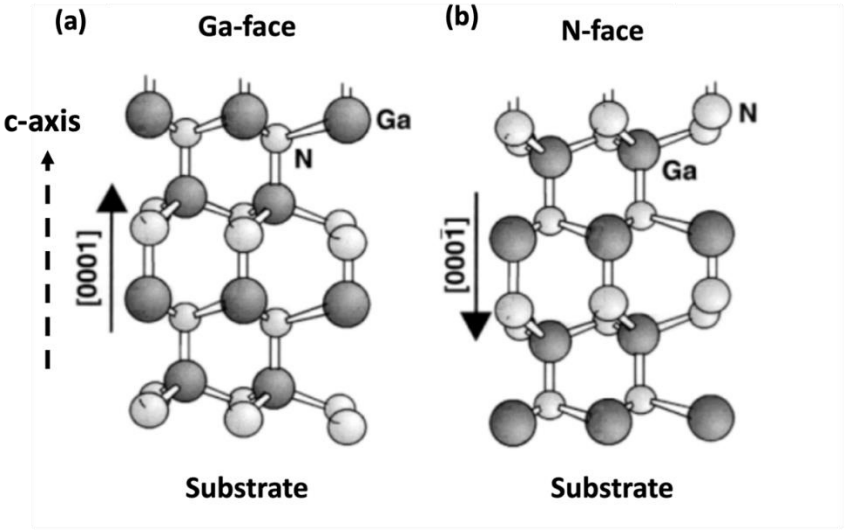


Figure 1.5. Hexagonal wurtzite crystal GaN, Ga-face (a) and N-face (b) [10].

The two faces have distinct chemical properties: The N-face is chemically active, enabling wet chemical etching of materials, which often results in rough surface morphology. The Ga-face is chemically more inert, resulting in a smoother surface morphology. In addition, the Ga-face more readily incorporates acceptors, while the N-face more readily incorporates donors. The Ga-polarity is the most widely used orientation for device manufacture, due to its ease of growth and high quality. The N-polarity, on the other hand, is more difficult to produce, but is gaining in popularity within the scientific and industrial communities.

Several dimensions characterize the crystal lattice parameters of the wurtzite form. These include the basal hexagonal edge length (a_0), the hexagonal lattice cell height (c_0) and the anion-cation length of the bond parallel to c_0 (μ_0). **Table 1.1** gives an overview of lattice constants for III-nitride wurtzite compounds [11, 12]. The ideal lattice constant ratio for a wurtzite structure is $c_0/a_0 = 1.633$. Among III-nitride semiconductors, GaN is the closest to this ideal ratio, compared with InN and AlN.

Table 1.1. Lattice constants for AlN, GaN and InN at room temperature.

Lattice constants	AlN	GaN	InN
a_0 (Å) [11]	3.112	3.189	3.540
c_0 (Å) [11]	4.982	5.185	5.705
c_0/a_0 [12]	1.6190	1.6336	1.6270
μ_0 [11]	0.380	0.376	0.377

Deviations from this ideal ratio (as μ_0 increases and the c_0/a_0 ratio decreases) result in a less ideal crystal structure. This increase in non-ideality enhances spontaneous polarization (P_{SP}) within the material, influencing the electronic properties of devices based on these materials. For example, the AlN crystal has a c0/a0 ratio of 1.619 with a P_{SP} of -0.081 C/m^2, while GaN has a higher ratio and a lower P_{SP} of -0.029 C/m^2 [11].

II.2. Polarization effects

III-N wurtzite crystal structures such as GaN, InN and AlN grown along [0001] exhibit polarization effects. Due to the absence of inversion symmetry in orientation and anion-cation bonds, these materials induce negative spontaneous polarization (P_{SP}) along the c-axis. In addition, deformation and mechanical stress during growth, caused by lattice mismatch, result in piezoelectric polarization (P_{PE}) and, consequently, an electric field. The total polarization (P_T) of III-N materials is defined by the sum of the two polarizations [12]:

$$P_T = P_{SP} + P_{PE} \qquad (1)$$

The growth of an AlGaN/GaN heterostructure along the c-axis features different energy gaps between AlGaN and GaN, creating an energy discontinuity at the interface. In addition, there is a lattice mismatch between the two materials ($a_0^{GaN} > a_0^{AlGaN}$), which generates tensile stress on the AlGaN layer to compensate for it. Thus, in an AlGaN/GaN heterostructure strained by the Ga-face, a piezoelectric polarization effect will be induced along the growth direction, given by [12]:

$$P_{PE} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \qquad (2)$$

With:

- e_{33} and e_{31}, the piezoelectric coefficients of the material.
- $\epsilon_z = \frac{(c-c_0)}{c_0}$, the strain along the c-axis.
- $\epsilon_x = \epsilon_y = \frac{(a-a_0)}{a_0}$, the in-plane strain assumed to be isotropic.
- a and c the lattice constants of the strained layer.

The following equation (3) gives the lattice constants of hexagonal GaN [12]:

$$\frac{(c-c_0)}{c_0} = -2\,\frac{C_{13}}{C_{33}}\frac{a-a_0}{a_0} \qquad (3)$$

Where C_{13} and C_{33} are elastic constants and by combining (2) and (3), the P_{PE} in the c-axis direction can be expressed as [12]:

$$P_{PE} = 2\,\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad (4)$$

Since $\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) < 0$ for AlGaN over the entire composition range, P_{PE} is negative for tensile strain and positive for compression-strained barriers. Consequently, the AlGaN/GaN heterostructure with AlGaN under tensile strain, P_{PE} will be negative and parallel to P_{SP} pointing towards the substrate [12-14] as shown in **Figure 1.6.a**.

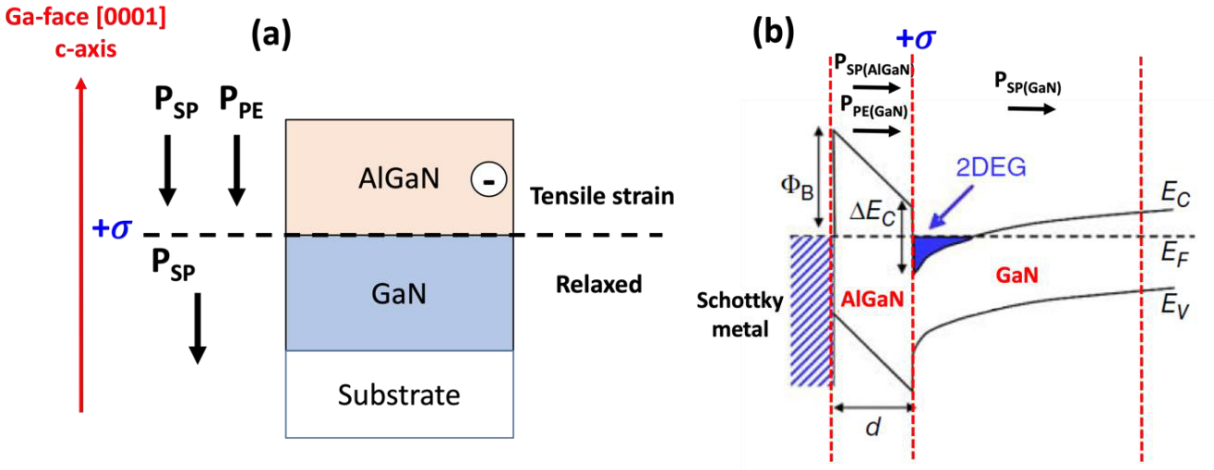


Figure 1.6. (a) Spontaneous and piezoelectric polarization in Ga-face for an AlGaN/GaN heterostructure subject to tensile strain, leading to positive polarization-induced sheet charge density σ. (b) Band diagram of an AlGaN/GaN heterostructure with formation of an electron well (2DEG) below the Fermi level [15].

The charge density induced by the total polarization in space is defined as follows:

$$\sigma_p = -\nabla P \qquad (5)$$

A polarization-induced charge density is associated with a polarization gradient in space, which in turn depends on the aluminum composition [12]:

$$|\sigma_{(x)}| = | [P_{SP}(Al_xGa_{1-x}N) + P_{PE}(Al_xGa_{1-x}N) - P_{SP}(GaN)] | \qquad (6)$$

For Ga-polar AlGaN/GaN heterostructure, the polarization-induced sheet charge is positive ($+\sigma$). Consequently, to balance this positive charge, free electrons are attracted, forming a Two-Dimensional Electron Gas (2DEG), as illustrated in **Figure 1.6.b**.

The maximum sheet carrier density of 2DEG (N_S) can be expressed by the following equation [12]:

$$n_s(x) = \frac{+\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{de^2}\right)[e\phi_b(x) + E_F(x) - \Delta E_c(x)] \qquad (7)$$

Where:

- d, the thickness of the AlGaN barrier layer.
- $e\phi_b(x)$, the height of the metal Schottky barrier.
- $\epsilon(x)$, the relative dielectric constant of AlGaN.
- $E_F(x)$, the fermi level with respect to the GaN conduction band energy.
- $\Delta E_c(x)$, the conduction band offset at the AlGaN/GaN interface.

In an AlGaN/GaN heterostructure, the 2DEG typically has a carrier density (n_S) of about 1.2×10^{13} cm^{-2} with electron mobility (μ) up to 2000 $cm^2/V.s$ [16, 17]. The sheet carrier concentration is influenced by several parameters, such as alloy composition and barrier layer thickness.

II.3. GaN properties and comparison with other semiconductors

GaN has been identified as a promising solution for meeting the combination of high-power and high-frequency requirements. Thanks to its excellent properties, in particular its energy gap three times greater than that of InP, GaAs and Si, GaN enables high operating voltage due to its larger breakdown field. Another interesting feature of GaN is its high saturated electron velocity (V_{sat}), which enables high current density at high voltage **(Table 1.2)**. Furthermore, GaN has a much higher thermal conductivity than GaAs and InP, which is a key factor directly related to power dissipation in the device.

Table 1.2. Characteristics of widely used semiconductor materials [18-22].

Material	Si	SiC	GaAs	InP	GaN
Mobility μ ($cm^2/V.s$)	[1100-1500*]	[400-1000*]	[6000*-8500**]	[5400*-10000**]	[1000*-2000**]
Bandgap E_g (eV)	1.1	3.2	1.4	1.3	3.4
Thermal conductivity λ (W/cm.K)	1.5	3.7	0.46	0.7	1.3
Critical eletric field E_c (mV/cm)	0.3	3.0	0.4	0.5	3.3
Saturation velocity v_{sat} (10^7cm/s)	1.0	2.0	1.2	1.5	2.5

*Bulk mobility and depending on material quality, **2DEG

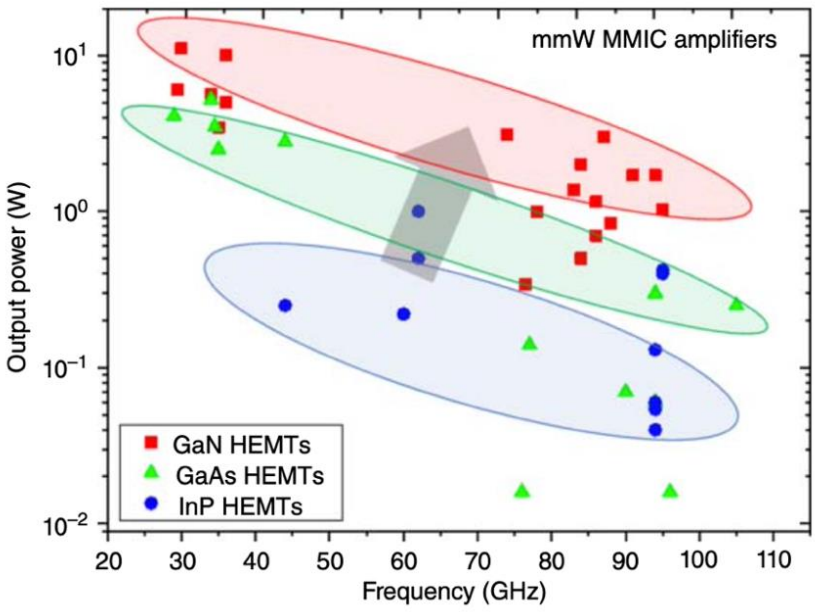


Figure 1.7. Output power of MMIC amplifiers based on GaN, GaAs and InP HEMTs [15].

For ultra-short devices operating at millimeter-wave frequencies, GaN-based heterostructures grown on SiC substrate are preferred due to both the intrinsic properties of GaN and the thermal conductivity of SiC. This facilitates the heat generated by self-heating to be properly dissipated and increases output power density capabilities at high frequencies. Moreover, GaN-based materials offer greater temperature stability and are inherently resistant to radiation due to their wide bandgap and strong covalent bonds, making them ideal for space environments [23]. **Figure 1.7** shows a comparison of the output powers obtained for GaN-, GaAs- and InP-based MMIC amplifiers reported in the literature, highlighting the superiority of GaN HEMTs [15].

To better evaluate the performance of semiconductor-based devices, two figures of merit (FOMs) have been proposed: The Johnson's Figure of Merit (JFoM) and the Baliga's Figure of Merit (BFoM). The JFoM is used to measure the ability of a semiconductor material to operate at both high frequencies and high-power levels:

$$\mathrm{JFoM} = \left(\frac{\mathrm{V_{sat}E_c}}{2\pi}\right)^2 \qquad (8)$$

With:

- E_C, the critical electric field
- V_{sat}, the electron saturation velocity

The BFoM evaluates the device's voltage withstand capability and its resistive losses:

$$\mathrm{BFoM} = \varepsilon\mu\mathrm{E_C^3} \qquad (9)$$

With**:**

- ε, the relative permittivity
- μ, the electron mobility
- E_C, the critical electric field

Table 1.3 summarizes the main figures of merit for various WBG semiconductors, normalized to Si as a reference. GaN's potential is undeniable, as it offers an excellent balance between high power and high frequency capabilities.

Table 1.3. Main figures of merit for WBG semiconductors normalized to Si [24, 25].

	Si [24]	GaAs [24]	InP [25]	4H-SiC [24]	GaN [24]
JFoM	1	11	16	410	790
BFoM	1	28	10	290	910

GaN and SiC show FOM values in similar proportions, which demonstrates significant advantages over conventional semiconductors. This points to the potential benefits of combining these two materials to develop advanced PA MMICs [26-28].

III. GaN-based HEMT structure

Figure 1.8 shows a typical GaN-based HEMT structure, composed of several layers. The substrate, generally made of silicon, silicon carbide or sapphire, provides mechanical support and influences heat dissipation. On top, a nucleation layer (AlN) is typically deposited to manage lattice mismatch and ensure high-quality epitaxial growth. this is followed by buffer layers is added to further manage the strain, reduce defects and dislocation density in tha active layers. The channel layer (GaN) is where the 2DEG is formed at the interface with the barrier layer, which induces a strong polarization field that creates and confines the 2DEG at the heterojunction. Finally, a cap layer, which can be GaN or SiN, is used to protect the underlying layers and optimize surface properties to enhance the device performance.

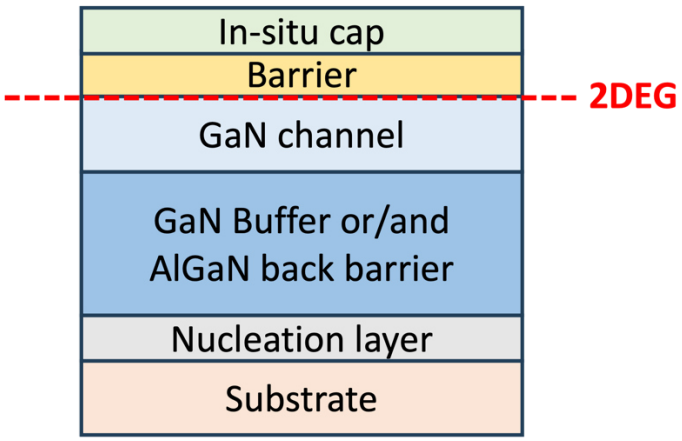


Figure 1.8. Typical Ga-polar HEMT epitaxy.

III.1. Growth techniques

Nowadays, two different techniques are commonly used to grow GaN HEMT epitaxies: Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE). Depending on the growth technique, layer uniformity and quality will be influenced by growth parameters such as temperature, pressure, and gas flow inside the chamber [29-31].

MBE is an ultra-high vacuum growth technique based on reactions between molecular, atomic or ionized beams of thermal energy from the constituent elements on a heated substrate. Renowned for its precision, the MBE technique offers atomic-level control, resulting in high-purity layers with low defect densities and minimal deformation. The result is extremely sharp interfaces. The main advantages of this technique are its slow growth rate and low growth temperature, typically between 600°C and 900°C [32, 33]. However, its slow growth rate and high operating costs due to the need for ultra-high vacuum conditions, makes this technique difficult to implement in an industrial scale.

MOCVD involves the thermal decomposition of ammonia (NH3) with organometallic compounds on the surface of a heated substrate. Commonly used organometallic compounds, such as trimethylgallium (TMGa), trimethylaluminum (TMAl) and trimethylindium (TMIn), are used to introduce Group III elements [34, 35]. These compounds are delivered to the reaction chamber via a carrier gas such as hydrogen (H_2) or nitrogen (N_2). This technique is less expensive than MBE. The typical growth rate is a few micrometers per hour, which is about twice as fast as MBE. As a result, MOCVD is the main method used in the GaN industry, as it effectively combines low cost with the production of high-quality material [36].

In this thesis work, Ga-polar epitaxy layers were produced by MOCVD, which were supplied by SOITEC and SweGaN companies.

III.2 Substrate choice

The choice of substrate for GaN HEMTs is crucial, as it directly influences the performance and cost of the final device. Selection depends on the specific demands of the intended application, including available size, lattice offset, thermal conductivity and coefficient of thermal expansion (CTE) [37].

Table 1.4 shows a comparison between the different substrates usually used for GaN growth. Bulk GaN substrates are not yet available in large wafers, which limits their application and expansion.

Table 1.4. Comparison of substrates suitable for GaN HEMTs [38].

	Si	SiC	GaN Bulk	Sapphire
Thermal conductivity (W/cm.K)	1.5	4.9	2.0	0.35
Thermal expansion coefficient ($\times 10^{-6}$ K^{-1})	2.6	4.4	5.5	7.5
Thermal expansion coefficient mismatch GaN (%)	52.7	18.9	0	36.4
Lattice mismatch with GaN (%)	17	3.5	0	14
Cost	Very low	High	Very high	Medium
Size (mm)	300	200	100	150

The sapphire substrate is semi-insulating by nature and can withstand high growth temperatures. It is relatively cost-effective and readily available, making it an attractive option for GaN RF HEMTs. However, the lattice mismatch between GaN and sapphire can lead to significant defect dislocations in epitaxial layers. In addition, sapphire has a relatively low thermal conductivity (0.35 W/cm.K) compared with other substrates such as silicon (1.5 W/cm.K) or silicon carbide (4.9 W/cm.K), resulting in poor heat dissipation [39].

Silicon is the most popular substrate due to its low cost and wide availability. Increasingly, research and development is focused on GaN-on-silicon HEMTs as a solution, particularly for low-frequency applications [40, 41]. However, silicon has a significant lattice mismatch with GaN, which can lead to defects during growth. In addition, silicon's low thermal conductivity translates into higher thermal resistance, which has an impact on device performance.

Silicon carbide (SiC) has established itself as the preferred substrate for high-frequency applications due to its low lattice mismatch with GaN and its superior thermal conductivity compared with other materials. Its ability to dissipate heat makes it indispensable in applications requiring robust thermal management. As a result, SiC-based GaN HEMTs offer excellent performance in the millimeter-wave range [42-44]. However, the main limitations of SiC are its high cost and the limited availability of large wafer size.

III.3. AlN nucleation layer

This layer is essential for the growth of high-quality GaN layers. Its role is to reduce the lattice mismatch between GaN and substrate, thus minimizing defects and thermal stresses, and facilitating subsequent growth of the buffer layer [45]. The quality and thickness of the AlN nucleation layer influence the thermal resistance (TBR), which has an impact on the device's operating temperature due to self-heating. By optimizing the nucleation layer, the TBR at the GaN/SiC interface can be reduced [46]. In fact, it was demonstrated that switching from standard to hot-wall MOCVD technology resulted in a 25% reduction in TBR, which translated into a 10% drop in operating temperature. [47].

III.4. Buffer design for millimeter waves

The buffer layer plays an important role in GaN-based HEMTs, and its design has a considerable impact on device performance. Thick and undoped, it typically reduces dislocations reaching the channel, providing a smoother surface for barrier layer growth. These buffers exhibit n-type conductivity due to unintentional impurities introduced during the growth process. This results in parasitic conduction paths and high leakage currents, degrading the device isolation. Consequently, for devices with short gate lengths, undoped buffers are insufficient to confine electrons in the channel and induce short-channel effects. To mitigate short channel effects, it is essential to reduce the distance between the gate and the channel by maintaining an L_G/a ratio greater than 15 (L_G is the gate length and a the gate-to-channel distance) [48]. The configuration of the buffer layer plays an essential role in this process. A well-designed buffer layer, such as one incorporating high-resistivity materials, ensures effective electron confinement under a high electric field [49]. Various methods have been reported in the literature to make the buffer layer more resistive. Carbon (C) or iron (Fe) doping is a popular method for increasing the resistivity of the GaN buffer layer. However, excessive incorporation of these dopants can lead to significant current collapse [50].

- <u>Fe-doped and C-doped GaN buffer:</u>

Fe doping is an effective approach to improving the resistivity of the GaN buffer layer. Incorporating Fe atoms introduces deep acceptor states that prevent parasitic conduction paths.

This improves device isolation, breakdown voltage and increases the safe operating bias voltage [51-53]. However, iron doping has drawbacks such as current collapse and memory effects that prevent abrupt doping profiles [54, 55]. C-doped GaN buffers offer significantly higher resistivity with a much sharper profile than Fe-doped GaN. For short devices offering high performance under strong drain bias, C-doped buffers are essential for improving breakdown voltage and device robustness [56, 57]. Nevertheless, with high carbon concentrations, GaN becomes p-type and is isolated from the channel by a PN junction. As a result, under strong drain bias, electrons can be trapped in the p-type region, forming a back-polarized PN junction, leading to a strong current collapse [58]. C-doping introduces deep traps by substituting carbon atoms for nitrogen (C_N) or gallium (C_Ga), thereby modifying the material properties. When carbon replaces nitrogen in the GaN lattice, it acts as an acceptor, with an ionization energy of 0.9 eV [59, 60].

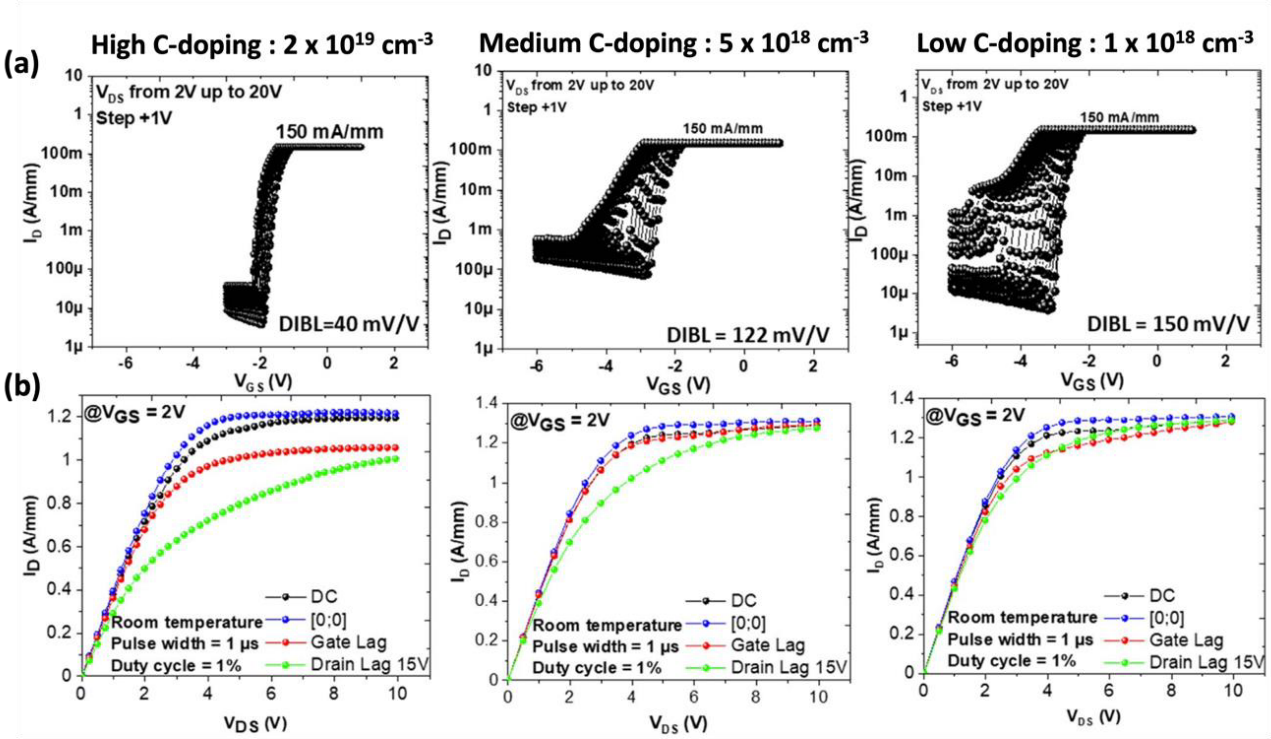


Figure 1.9. (a) Transfer characteristics up to V_{DS} = 20V and (b) DC-pulsed up to V_{DS} = 15V for a 100nm GaN channel with different C-doping (L_G = 100nm) [61].

Recently, our research group reported that the carbon content of the buffer layer and its proximity to the GaN channel has a direct impact on transistor performance [61]. At 100 nm from the 2DEG, a high carbon concentration significantly improves electron confinement and reduces leakage current, but conversely increases current collapse **(Figure 1.9)**.

It is therefore important to carefully optimize the carbon concentration and distance to the 2DEG in order to tune the electron confinement / current collapse trade-off.

- AlGaN back barrier:

Another solution for improving electron confinement is to use an AlGaN back barrier. This introduces a high-potential barrier that prevents electrons paths within the structure by repelling them through a back-polarization mechanism. Numerous studies have demonstrated that the insertion of a back barrier improves the electron confinement, reduces the drain leakage current and mitigates current collapse [62-64]. It is also possible to combine the AlGaN back barrier with carbon doping in the GaN buffer to strike the right balance between electron confinement and trapping effects [65, 66]. In particular, we have achieved state-of-the-art large signal performance at 40 GHz with such a buffer combination, yielding a PAE of 66.5% at V_{DS} = 20V [65]. However, the aluminum content of the back barrier must be adjusted to ensure effective back polarization. Growing an AlGaN back barrier with a high aluminum content poses several challenges. A high aluminum composition can lead to increased deformation and a greater density of defects within the structure, reducing the quality of the active layers [67]. In addition, the use of an AlGaN back barrier with a high aluminum content can have an impact on heat dissipation inside the structure. It has been shown that as the Al content increases, the thermal conductivity of AlGaN decreases, which can affect the device's ability to dissipate heat efficiently **(Figure 1.10)** [68].

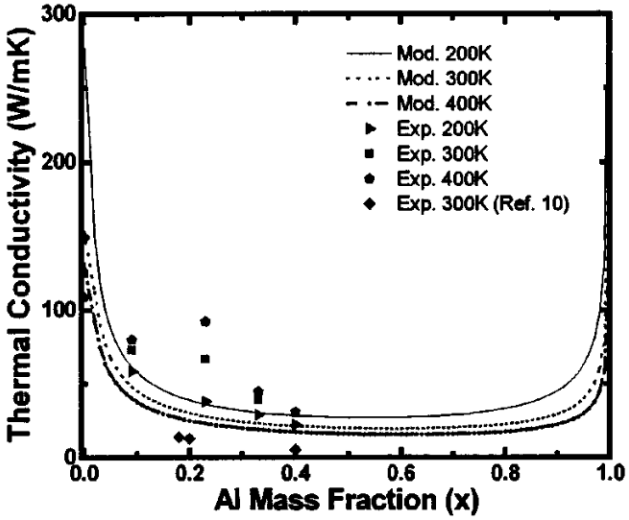


Figure 1.10. Thermal conductivity as a function of the Al mass fraction x for $Al_xGa_{1-x}N$ alloy system at 200, 300, and 400 K [68].

- Buffer-free technology:

Recently, the development of buffer-free GaN HEMTs (SweGaN) has attracted interest in the field of semiconductor technology. This design uses an AlN nucleation layer as a back barrier, produced by hot-wall MOCVD under specific conditions. The use of a high-quality AlN nucleation layer provides greater structural integrity with fewer dislocations compared to conventional GaN buffer structures, as shown in **Figure 1.11**. Limited research has been conducted on buffer-free HEMTs; however, some studies have reported remarkable robustness and competitive performance metrics.

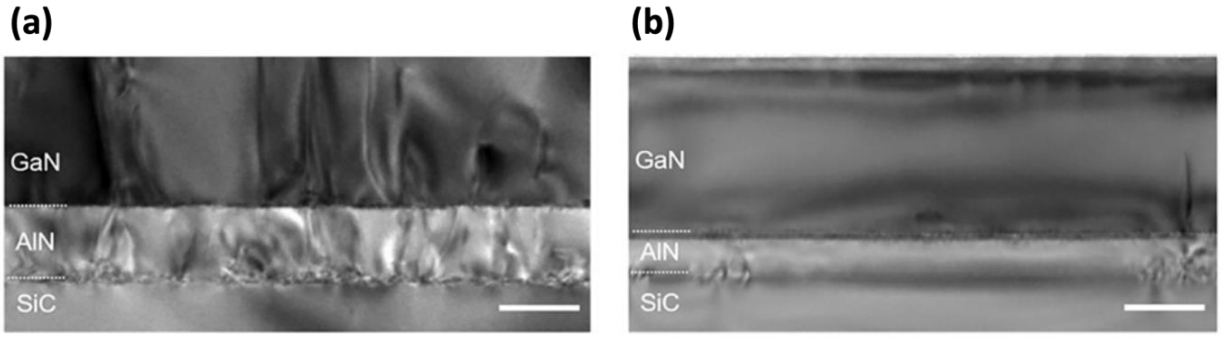


Figure 1.11. (a) TEM images of "standard" MOCVD growth GaN/AlN//SiC and (b) "hot-wall MOCVD growth GaN/AlN/SiC [69].

For example, SweGaN demonstrated lateral and vertical breakdown voltages over 1500 V for ultrathin AlGaN/GaN HEMTs grown on SiC, using a 200 nm thick GaN channel with a 60 nm thick AlN NL as a back barrier [69]. Comparisons between a buffer-free GaN HEMT and a conventional Fe-doped thick buffer revealed competitive output power levels and efficiency at 3 GHz [70]. In another recent study, promising RF performance was reported at 30 GHz, with an output power of 2 W/mm and a PAE of 53% at V_{DS} = 15V [71]. Improvements in heat dissipation were also noted in this design, as heat transfers more efficiently to the substrate without additional thermal barrier from the thick buffer layers. Thermal imaging revealed a reduction of about 30% in surface temperature in the buffer-free devices compared to the conventional Fe-doped buffer devices **(Figure 1.12)** [72].

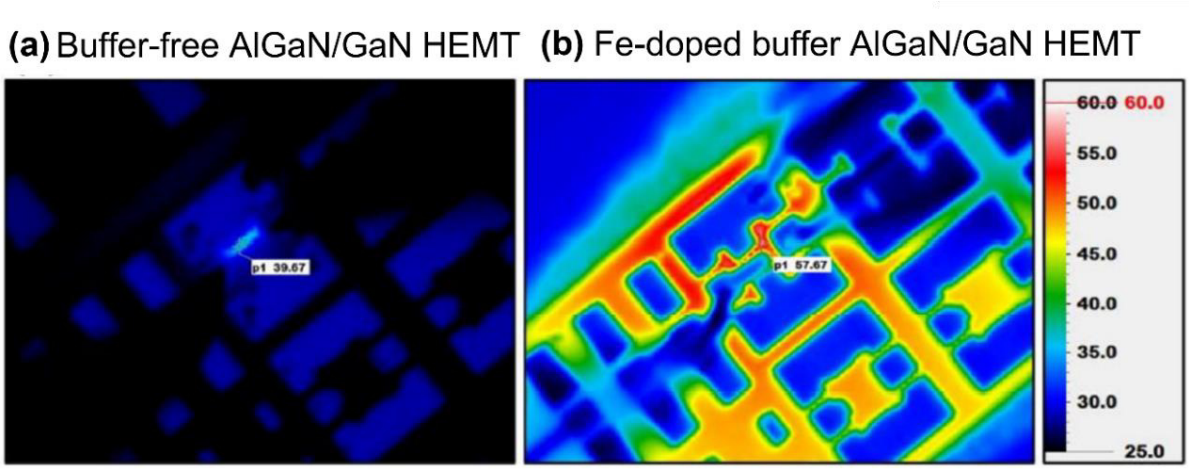


Figure 1.12. Thermal image measurements of buffer-free (a) and thick Fe-doped buffer (b) AlGaN/GaN HEMTs.

However, the proximity of the 2DEG to the substrate and the AlN nucleation layer may induce trapping effects due to doping agents such as vanadium, requiring further research to fully understand this new architecture.

In this thesis work, we will study two different types of buffer designs, both intended to the use of short gate length devices (100 nm) for millimeter-wave applications. The first architecture grown by SOITEC, combines a C-doped GaN buffer layer with a C-doped AlGaN back barrier on a SiC substrate. The second design involves the use of an AlN nucleation layer as a back barrier without any buffer layer, known as "QuanFINE" and developed by SweGaN.

III.4. GaN channel

The GaN channel is the active layer of the HEMT heterostructure. It is generally undoped to allow high electron transport and avoid trapping near the 2DEG. The thickness of the GaN channel is crucial as it has a direct impact on the device robustness and performance. A thicker GaN channel can improve the electron density and reduce trapping. However, for scaled devices with short gate lengths, a thinner GaN channel is needed to control short-channel effects such as drain-induced barrier lowering (DIBL). High DIBL can induce threshold voltage shifts and increase leakage currents. This trade-off is essential to obtain reliable, high-performance devices suitable for high-frequency applications.

One design that differs from the conventional GaN channel is the graded AlGaN channel HEMT developed by Hughes Research Laboratories (HRL, USA). This design is unique since it incorporates a gradient of AlGaN (ranging from 0% to 10% Al content) between the barrier and the GaN channel. This approach has demonstrated state-of-the-art power performance up to the W-band [73]. Further details on this architecture will be provided in chapter 2.

III.5. Barrier and in-situ cap layer

The choice of the barrier layer is essential for optimum performance in GaN HEMTs. Barrier thickness and composition will impact mechanical deformation and piezoelectric polarization, which directly influence the mobility (μ) and carrier density (N_S) of the 2DEG. Several barrier options are available, all based on III-nitride semiconductors, including ternary and quaternary alloys such as AlGaN, AlN, InAlGaN or InAlN.

- AlGaN barriers

The use of an AlGaN barrier is the most widely adopted and developed technology for GaN-based HEMTs. Typical AlGaN barriers have an aluminum composition of between 20 and 35%, and thicknesses ranging from 14 to 30 nm. Depending on the configuration of the AlGaN barrier, a sheet carrier density of between 5×10^{12} cm^{-2} and 1.2×10^{13} cm^{-2} can be achieved, with an electron mobility that can be above 2000 $cm^2/V.s$. A low aluminum content and a thin barrier reduce the density of 2DEG, while a high aluminum composition with a thick barrier increases the lattice mismatch with GaN. Despite excellent Ka-band power performance [74], it is difficult to further improve AlGaN/GaN HEMTs, as the barrier scale reaches theoretical limits in terms of thickness and carrier density combination for higher-frequency applications. To enhance the frequency performances, it is mandatory to shrink the gate length while maintaining an L_G/a aspect ratio greater than 15 to mitigate short-channel effects [48]. Consequently, reducing the barrier thickness is an effective approach to maintaining this ratio. However, in AlGaN/GaN devices, the channel's sheet carrier density drops for a barrier thickness below 20 nm, impacting the performance [75, 76]. This issue necessitates the development of new material barriers to maintain high performance.

- InAlN and InAlGaN barriers

Recently, the exploration of new barrier such as InAlN and InAlGaN for GaN-based HEMTs has intensified. These barriers have the advantage of being lattice-matched to GaN when the indium (In) concentration is 17% [77]. In addition, spontaneous polarization at the InAlN and InAlGaN/GaN interfaces induces a much higher electron density due to a stronger polarization field than conventional AlGaN barriers, improving the overall device performance. InAlN barriers have demonstrated very high 2DEG properties, with electron densities up to 2.6×10^{13} cm^{-2} [78] and electron mobility in excess of 1000 $cm^2/V.s$, as well as exceptional thermal stability up to 1000°C [79]. Scaling devices while benefiting from short gate lengths (100 nm and below) requires growing InAlN barrier layers thinner than 10 nm. This results in a high L_G/a ratio, making this barrier attractive for millimeter-wave applications [80, 81]. For example, using a 9.8 nm InAlN barrier in GaN HEMTs, an output power density of 5.8 W/mm with an associated PAE of 43.6% has been reported at 35 GHz [82]. InAlGaN barriers also exhibit superior 2DEG properties to conventional AlGaN barriers, thanks to a remarkable electron mobility exceeding 1600 $cm^2/V.s$ while maintaining an electron density of 1.8×10^{13} cm^{-2} [83, 84]. An impressive result was obtained at 96 GHz with an InAlGaN/GaN HEMT, delivering an output power density of 3 W/mm with a gate length of 80 nm [85]. Despite these excellent performances, the reliability of these barriers has yet to be demonstrated, which remains the main challenge. Moreover, comprehensive studies on the long-term stability and diffusion behavior of indium in InAlN or InAlGaN barrier layers are still required.

- AlN barriers

The ultrathin AlN/GaN system has emerged as a promising candidate for high-power millimeter-wave applications due to its ability to significantly scale-down the barrier thickness while benefiting from strong polarization effects. 2DEG density can reach an electron mobility of around 1000 $cm^2/V.s$ with a high electron density of over 2×10^{13} cm^{-2} [36, 86]. However, high-quality AlN barriers can be tricky to grow due to the large lattice mismatch between AlN and GaN. Excessive deformation can lead to increased defect density in the barrier, which can impact on 2DEG properties and device robustness [87]. Despite these difficulties, significant power performance has been achieved at 40 GHz with ultrathin AlN barrier layers [44, 62, 88]. This highlights the potential of ultrathin AlN barriers for high-frequency applications.

- In-situ cap layer

The final layer is a passivation layer, typically sub-10 nm, made of GaN or SiN. Its role is to protect the barrier layers from contamination, oxidation and surface leakage current. In addition, passivation layers are necessary to reduce trapping effects by passivating the surface charges, which may also improves electron mobility by reducing surface scattering of electrons [89, 90].

III.6. GaN HEMTs studied in this work

With the aim of further pushing the limits of conventional GaN HEMTs for high mmW performance, two different structures were investigated in this work (**Figure 1.13**).

- The first structure, grown by SOITEC, consists of an ultrathin AlN barrier, a GaN channel, a C-doped AlGaN back barrier and a C-doped GaN buffer on a SiC substrate. The structure is covered by an in-situ SiN cap.
- The second structure, grown by SweGaN, is an ultra-thin HEMT with a total epi-thickness of less than 250 nm on semi-insulating SiC substrate. It consists of a thin Al-rich AlGaN barrier, a GaN channel and an AlN nucleation layer acting as a back barrier. The structure is covered with a hybrid in-situ cap of GaN/SiN.

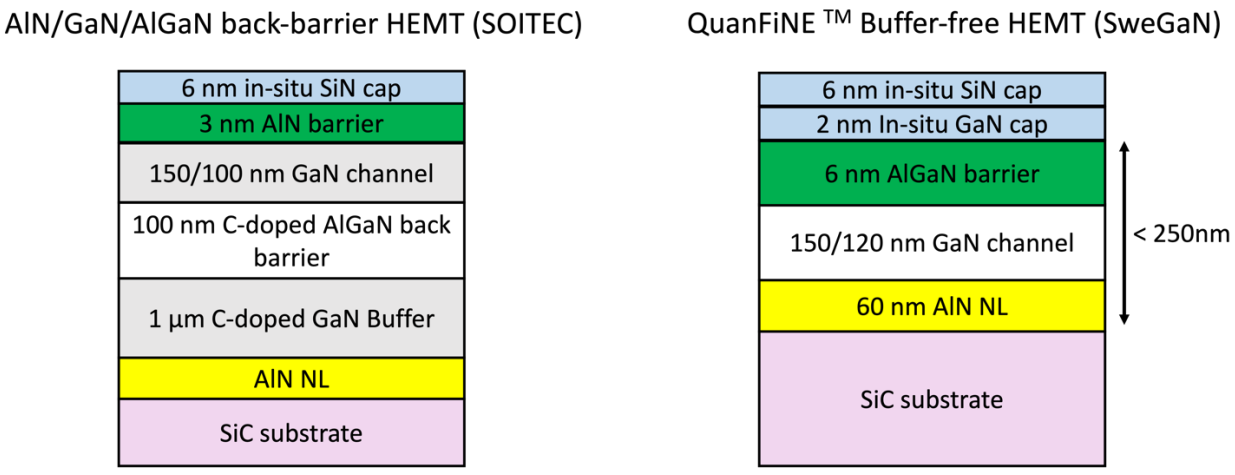


Figure 1.13. AlN/GaN HEMT epitaxy from SOITEC (left) and AlGaN/GaN Buffer-free HEMT epitaxy from SweGaN (right).

IV. Device downscaling and key features for performance enhancement

IV.1. T-shaped gate

To improve the performance of GaN HEMTs, an effective optimization approach is required. This involves competitive design of the epitaxial layer to control the electron transport properties, and engineering of transistor geometrical elements during fabrication, such as gate module or ohmic contacts. As device dimensions expand to the nanoscale, it is essential to shrink gate lengths to reduce electron transit times. However, a corresponding reduction in barrier thickness is required, while improving RF characteristics. F_t and F_{max} determine the maximum speed and frequency range over which the device can operate efficiently. Maximum transconductance (G_M) with short gate lengths and reduced parasitic elements further increases F_t/F_{max}. Therefore, a T-shaped gate effectively reduces these parasitic elements. Improving F_{max} requires a gate foot height (H_{GF}) greater than 100 nm, which is essential for better electric field distribution and lower parasitic capacitances and resistances [91-93]. The key principle for improving F_t is to reduce the gate length while maintaining a high aspect ratio L_G/a combined with a high carrier density in the 2DEG [48].

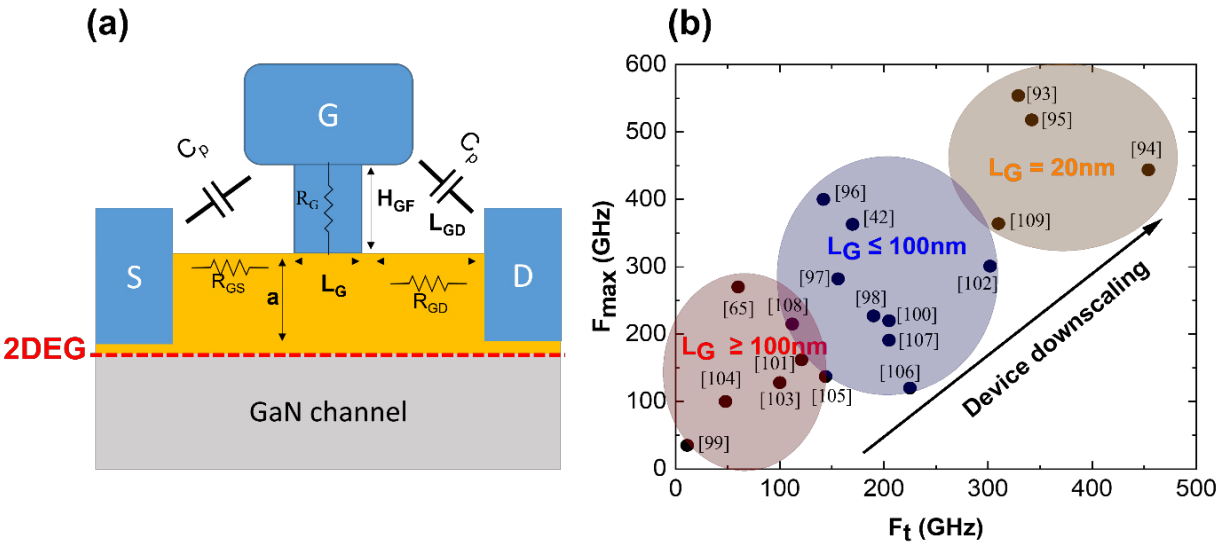


Figure 1.14. (a) Cross-section of T-gate GaN HEMT. (b) F_{max} as a function of F_t according to L_G with different T-gate optimizations [42, 65, 93-109].

Figure 1.14.a presents a cross-sectional view of a GaN HEMT, showing the parasitic elements of the T-gate design. Reducing the source-drain distance also increases F_t/F_{max} by lowering the on-resistance and improving the maximum drain current. However, this reduction has also an impact on breakdown voltage, as a higher electric field will be confined into a smaller area. **Figure 1.14.b** provides a benchmark of F_{max} as a function of F_t according to L_G through several approaches intended to reduce parasitic elements. These approaches include T-gate optimization, self-aligned gate processes, n^+ GaN ohmic contact regrowth and vertical scale epitaxy. The most remarkable results for F_t and F_{max} to date are 454 GHz and 582 GHz respectively, using a 20nm gate length [93, 94].

IV.2. Advanced ohmic contacts

To achieve high RF performance with aggressive device scaling, it is necessary to reduce the contact resistance (R_C), as it has a significant impact on parasitic resistances. Typically, partial etching of the barrier layer is performed to get as close as possible to the 2DEG without damaging the GaN channel. In general, contact resistance values of less than 0.5 Ω.mm are required to optimize device performance up to Ka-band and even lower at higher frequencies. To accomplish this, several factors must be carefully considered during the manufacturing process. These include the composition and thickness of the metal stack, the annealing temperature and the etching parameters or surface treatments applied. The Ti/Al/Ni/Au metal stack is widely used for GaN HEMTs due to its well-established fabrication process and reliable performance. However, achieving low contact resistances with this stack generally requires an annealing temperature above 800°C. This high temperature facilitates the formation of an alloy that provides good ohmic contact by reducing the Schottky barrier height and increasing carrier tunneling [110]. To reduce the contact resistances with Ti/Al/Ni/Au metal stacks, it is essential not only to limit the metal's lateral diffusion and the surface roughness that occurs during high temperature annealing, but also the thickness of each metal layer [111, 112].

Alternative metal stacks have also been explored, incorporating other elements such as Molybdenum (Mo) or Tantalum (Ta). These options offer excellent ohmic contact while enabling lower annealing temperatures. **Figure 1.15** shows different contact resistances obtained as a function of annealing temperature for different barrier layers and metal stacks used.

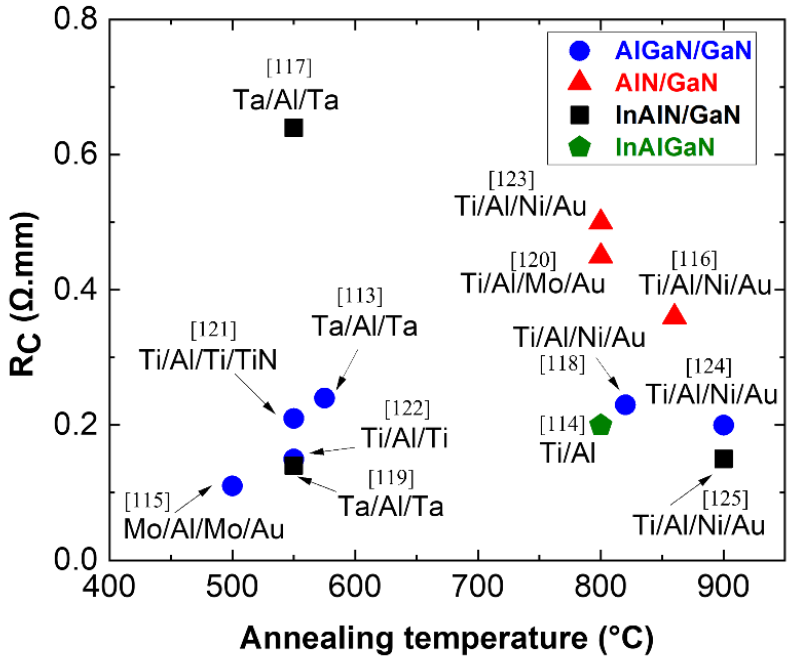


Figure 1.15. R_C versus annealing temperature for different barrier layer on GaN [113-125].

While recessed ohmic contacts can achieve contact resistances often below 0.5 Ω-mm, the use of regrown n^+ GaN layers can further reduce parasitic resistances to less than 0.1 Ω-mm [93, 95, 97, 108, 126]. This approach involves regrowing a highly doped n^+ GaN layer, which allows direct contact with the 2DEG, facilitating the electron transport across the metal-semiconductor interface. This advanced technique is crucial to unlock the ultra-low resistances required for high-frequency devices. However, currently, ohmic contact regrowth is mainly achieved by MBE technology, thereby making it less suitable for large-scale foundry processes.

V. Characteristics and challenges of RF GaN HEMTs

In this section, we present the main features used to study GaN-based HEMTs fabricated during this thesis work. Challenges are also discussed, as well as the state of the art. GaN HEMTs can be characterized through different electrical measurements, including DC and small-signal measurements, large-signal performances (load pull), linearity and short-term reliability tests. The IEMN laboratory has comprehensive facilities for evaluating transistor performance, covering key performance measurements except for linearity tests, which is currently under development at 40 GHz.

V.1. DC characteristics

A HEMT is a type of heterojunction field effect transistor. It works by modulating the conductance between two ohmic contacts, the Source (S) and the Drain (D), through the electrostatic influence of a metallic control electrode known as Gate (G). The gate is defined by its length (L_G) and width (W) and acts as a controller that adjusts the current flowing through the GaN channel **(Figure 1.16)**.

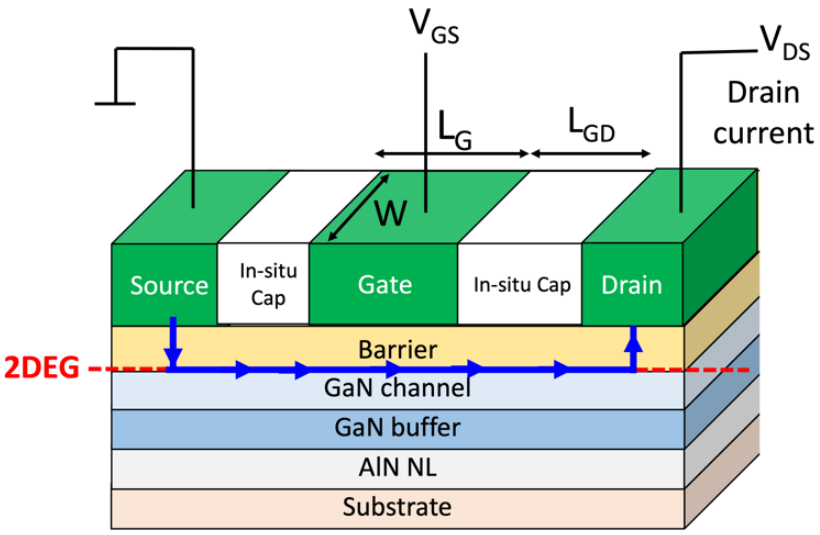


Figure 1.16. Operating principle of a HEMT, where current flows from the source to the drain contact inside the channel.

Beyond assessing on and off current, DC characteristics are used to detect undesirable effects that can cause electrical anomalies such as short channel effects, poor robustness, and leakage currents. In ON-state, GaN HEMTs must be able to deliver high maximum drain current density ($I_{D\ max}$) and high maximum transconductance (G_M) while maintaining low OFF-state leakage current. **Figure 1.17** shows typical DC characteristics I_DV_G and I_DV_D where we can extract several parameters such as:

- **$I_{D\ max}$** : the maximum drain current that the transistor can deliver in ON state.
- **$I_{D\ leakage}$** : the drain leakage current of the transistor in OFF state.
- **V_{TH}** : the threshold voltage of the transistor, corresponding to the transistor's transition from the OFF-state to the ON-state.
- **$G_{M\ max}$** : the maximum extrinsic transconductance, which is expressed by the following equation:

$$G_M = \left(\frac{\delta I_{DS}}{\delta V_{GS}}\right) V_{DS\,=\,Cste} \qquad (10)$$

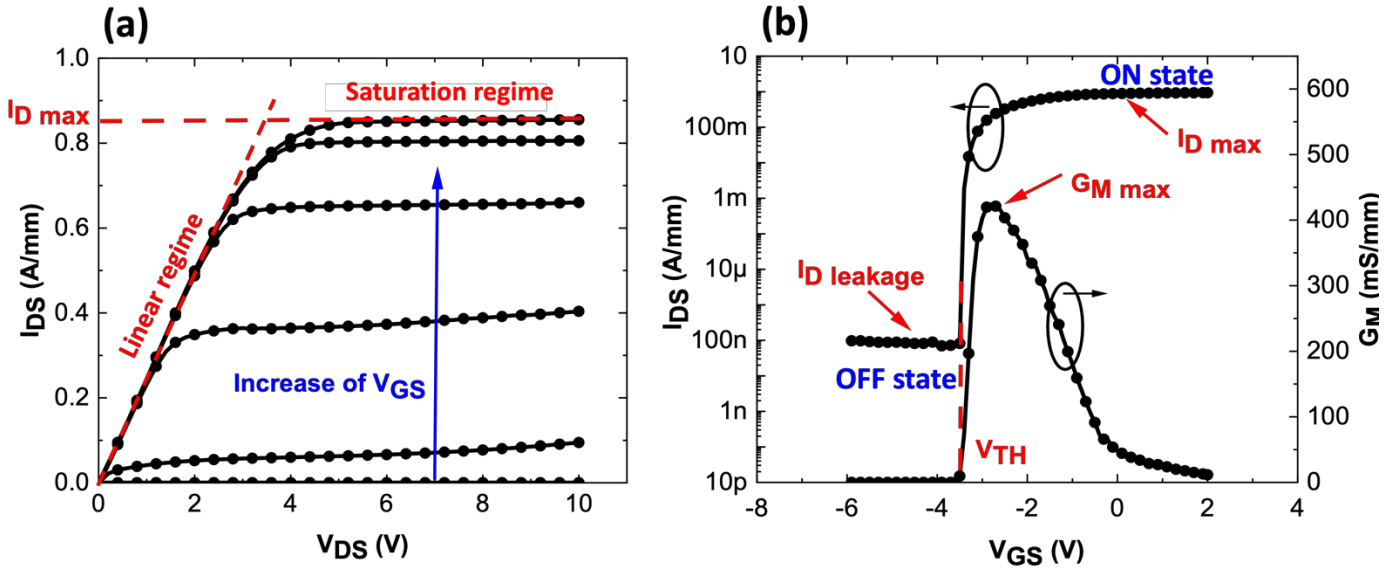


Figure 1.17. (a) Typical $I_D(V_{DS})$ and (b) I_D-$G_M(V_{GS})$ characteristics of a GaN HEMT.

Figure 1.17.a illustrates the $I_D(V_{DS})$ output characteristics of a HEMT, showing two distinct operational regimes: the linear regime, where the drain current (I_D) is proportional to the drain voltage (V_{DS}), and the saturation regime, where the drain current becomes independent on the drain voltage. The maximum drain current ($I_{D\ max}$) is determined from the saturation region. **Figure 1.17.b** presents the standard $I_D(V_{GS})$ characteristic from which the ON and OFF state drain currents are extracted. A high I_{ON}/I_{OFF} ratio with low leakage current is essential for optimum transistor performance. The threshold voltage is generally extrapolated graphically using the tangent extrapolation method, allowing for instance the evaluation of the Schottky contact and the gate length scaling quality. This graph displays three distinct operating zones:

- **$V_{GS} > V_{TH}$**: The carrier density in the channel increases with the drain current as a function of the gate voltage, reaching an optimum V_{GS} for which the transconductance is maximized.
- **$V_{GS} < V_{TH}$**: The channel becomes fully depleted, indicating the transistor is switched off.
- **Beyond $G_{M\ max}$**: the transconductance decreases as the channel opens, mainly due to self-heating and the decrease of electron mobility/velocity.

Another important parameter for assessing the device performances is the Drain Induced Barrier Lowering (DIBL), a short channel effect characterized by a negative shift in threshold voltage and an increase in the leakage current at high drain voltage. This is a very efficient and quick test to evaluate the material quality and / or the epi-design architecture under high electric field. The DIBL value reflects the electron confinement within the 2DEG and should be as low as possible. A high DIBL indicates a less robust device with a poor electron confinement. It is expressed by the following equation:

$$\mathrm{DIBL} = \frac{\Delta V_{TH}}{\Delta V_{DS}} \qquad (11)$$

The way to measure it is as follows : the drain current is limited to a specified compliance (150 mA/mm for instance) to avoid excessive self-heating during multiple $I_D(V_{GS})$ sweeps with V_{DS} ranging from 2V to 20V (or more). **Figure 1.18.a** displays an example of a transistor with DIBL showing an excellent electron confinement while maintaining low leakage currents. In contrast, **Figure 1.18.b** illustrates a component with poor DIBL, exhibiting insufficient electron confinement and an associated increase in leakage currents.

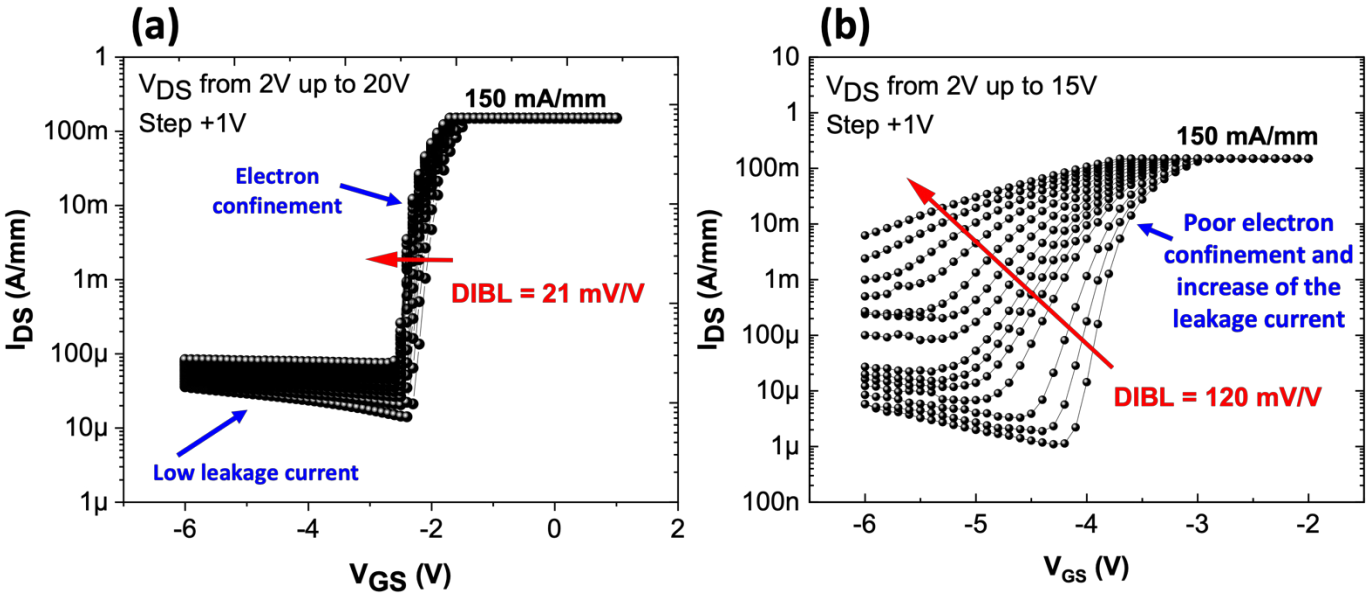


Figure 1.18. (a) An example of HEMTs with an excellent DIBL and (b) poor DIBL.

V.2. Small signal characteristics

The linear or equivalent small-signal model of GaN HEMT is presented in **Figure 1.19**. This model consists of two types of parameters: intrinsic and extrinsic elements. The extrinsic parameters correspond to the parasitic elements from the access lines and metallization, including pad capacitances (C_{PG}, C_{PD}, C_{PGD}), pad inductances (L_G, L_D, L_S), and gate and access resistances (R_G, R_D, R_S). The intrinsic parameters include gate-to-source, gate-to-drain, and drain-to-source capacitances (C_{GS}, C_{GD}, C_{DS}), as well as the drain-to-source resistance (R_{DS}), which are bias dependent.

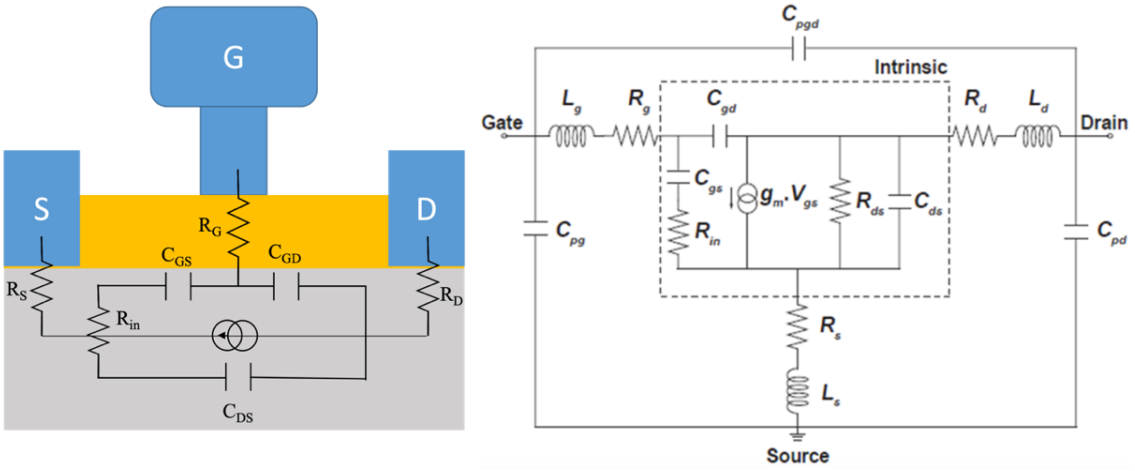


Figure 1.19. Small signal equivalent circuit model of GaN HEMTs.

The RF performance of GaN HEMTs is usually tested by means of two small-signal figures of merit: the current gain cutoff frequency (F_t) and the maximum oscillation frequency (F_{max}). To access them, the optimal gate bias (V_{GS}) is set at the point of maximum transconductance ($G_{M\,max}$), while the drain voltage (V_{DS}) is increased to evaluate the maximum oscillation frequency (F_{max}) of the transistor. To extract F_t and F_{max} the current gain H_{21} and the unilateral power gain (U) are calculated from S-parameter measurements via the following equations:

$$H_{21} = \frac{-S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \quad (12)$$

$$U = \frac{1}{2}\frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\frac{S_{21}}{S_{12}} - \mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)} \quad (13)$$

The transition frequency, also known as the cutoff frequency (Ft), is the frequency at which the current gain H_{21} equals 0 dB. This frequency depends on the transconductance and the intrinsic characteristics of the transistor's equivalent circuit model:

$$F_t = \frac{G_M}{2\pi(C_{GS}+C_{GD})} \qquad (14)$$

Where G_M, C_{GS}, C_{GD} represent the transconductance, gate-to-source capacitance and gate-to-drain capacitance, respectively.

F_{max} is a crucial figure of merit for assessing the potential of transistors in high-frequency power applications. It is defined as the frequency at which the unilateral power gain (U) drops to 0 dB. F_{max} is expressed by the following equation:

$$F_{max} = \frac{Ft}{2(R_G+R_{DS})^{\frac{1}{2}}} \qquad (15)$$

With R_G is the gate resistance and R_{DS} is the drain-to-source resistance.

F_t and F_{max} are determined by an extrapolation method using a slope of -20 dB/decade. **Figure 1.20** shows an example of F_t/F_{max} extraction from the H_{21} and U plots.

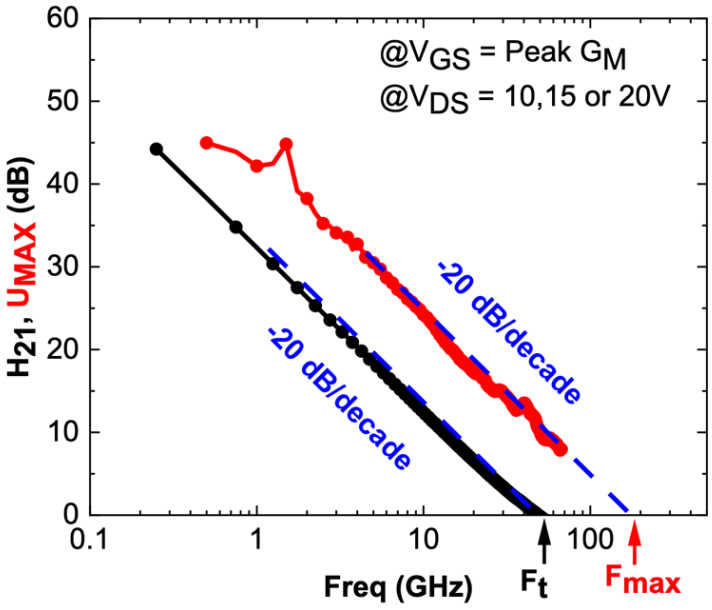


Figure 1.20. Example of U_{max} and H_{21} plots used for determining F_t and F_{max}.

V.3. DC-pulsed characteristics

Trapping effects are one of the major challenges in GaN HEMTs, as traps contribute to memory effects and can cause performance, reliability issues and failure mechanisms. Traps arise from defects or impurities that capture and release electrons, causing fluctuations in electron density, leading to current collapse and increased channel resistance. For high-frequency applications, trapping and detrapping can reduce the performances of the device by affecting the dynamic on-resistance and related current density. Moreover, these effects can be thermally activated, becoming more pronounced with increased temperature, thereby exacerbating GaN HEMT degradation. To quantify and analyze trapping effects, pulsed I-V measurements are performed using different quiescent bias points. This approach enables to understand how these parasitic effects influence the transistor performance. traps are generally classified into two types: "Gate Lag" (GL) and "Drain Lag" (DL). Gate Lag refers to electron trapping near the gate, while Drain Lag is related the overall space charge region between the gate and drain within the structure, including surface and buffer layers.

Pulsed I-V measurements are performed by pulsing the gate and drain from the quiescent bias points (V_{GQ}; V_{DQ}), corresponding to a fixed trapping time during the off-state period (t_{OFF}). The drain current is then measured during the on-state period (t_{ON}) of the pulse. The on-state duration (pulse width) is reduced to 1 µs, while the off-state duration is extended to 99 µs. This configuration limits self-heating and allows to highlight on the trapping effect with a reduced impact of self-heating. The ratio between pulse width and period is known as the duty cycle, which corresponds to 1%. **Figure 1.21** features an example of pulsed $I_D(V_{DS})$ characteristics for devices with low current collapse **(Figure 1.21.a)** and high current collapse **(Figure 1.21.b).** A specific DC pulsed protocol, based on DC characteristics, is established for several bias points to identify trapping effects:

- **Cold Point**: (V_{GQ}; V_{DQ}) = (0V; 0V), which corresponds to a measurement where self-heating effects are excluded, and electron trapping negligible.
- **Gate Lag**: (V_{GQ}; V_{DQ}) = (< V_{TH}; 0V), which highlights the electron trapping under the gate region.
- **Drain Lag**: (V_{GQ}; V_{DQ}) = (< V_{TH}; ([10V,15V,20V…]), which shows the electron trapping under the gate-to-drain region.

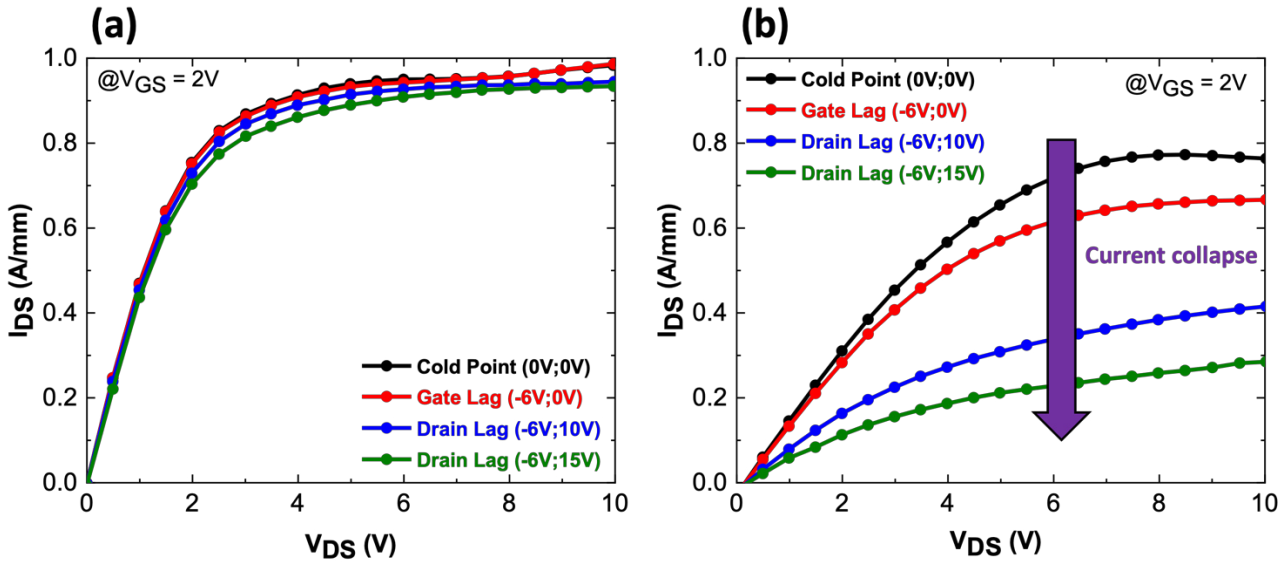


Figure 1.21. (a) An example of DC pulsed showing low (a) and high (b) current collapse.

V.4. Large signal characteristics

GaN devices must be able to provide high gain, high power-added efficiency (PAE), and high output power density (P_{OUT}). To evaluate these characteristics, load pull measurements are conducted at the frequency of interest. These measurements can be made using two distinct excitation modes: Continuous Wave (CW) and pulsed mode. CW load pull involves continuous bias of the transistor with a constant RF signal, resulting in steady-state operation and continuous heat generation. In contrast, pulsed mode applies the RF signal and bias in pulses, allowing intermittent cooling periods. This lowers the average junction temperatures and improves performance by reducing the thermal budget. Additionally, pulsed mode mitigates trapping phenomena by allowing periods of zero bias between pulses.

The following equations are used to evaluate RF performance at a specific frequency:

$$PAE = \frac{P_{OUT} - P_{abs}}{P_{DC}} \qquad (16)$$

Where PAE is the power added efficiency, P_{OUT} is the output power density (W), P_{DC} is the dissipated DC power density and P_{abs} is the power absorbed at the input of the device (W). PAE is a key measure for evaluating the heat management of a device. A high PAE indicates that the device efficiently converts DC power into RF power, minimizing energy loss as heat.

The operating mode of a transistor determines the bias class. As shown in **Figure 1.22**, various bias classes exist (A, AB, B…), with the deep class AB being the most common for telecommunication. In class AB, the quiescent drain current is set to an optimal value that balances linearity and efficiency.

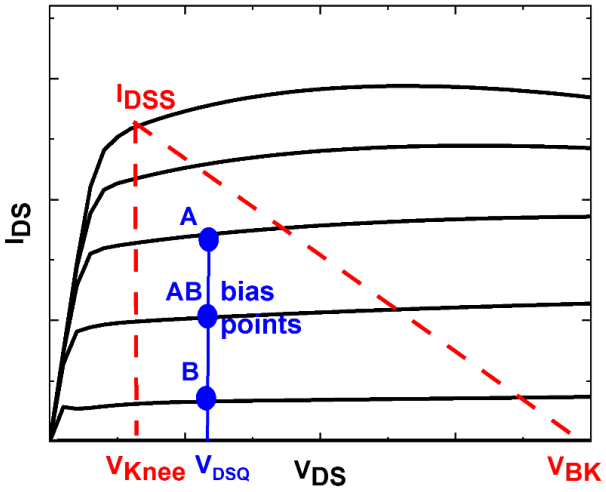


Figure 1.22. I-V characteristics illustrating three distinct bias points (Class A, AB, B).

- $P_{OUT} = \frac{V_{DSQ} - V_{knee} \times I_{DSS}}{4}$ (17)

With V_{DSQ}, the quiescent drain-source voltage bias, V_{knee}, the knee voltage of the transistor's I-V curve and I_{DSS}, the saturated current density. A high breakdown voltage allows for high quiescent drain-source voltage operation, thereby increasing the output power density (P_{OUT}).

Equation (18) expresses the power gain (G_p), a key performance indicator of transistors that defines their ability to amplify an RF signal. High gain contributes to high power density and improves PAE, which in turn improves the overall device performance.

- $G_p = \frac{P_{OUT}}{P_{abs}}$ (18)

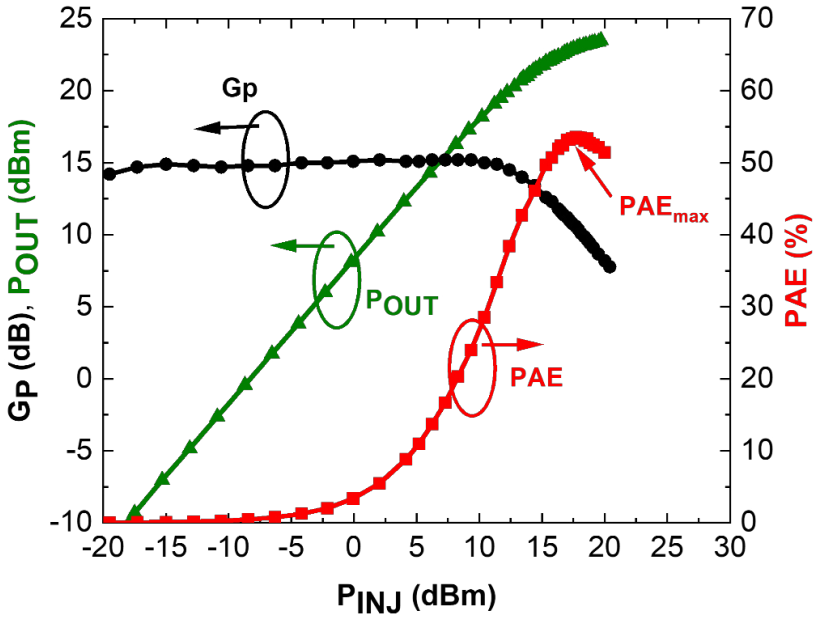


Figure 1.23. An example of large signal characteristics showing the PAE, P_{OUT} and G_P.

Figure 1.23 shows an example of large signal characteristics measured at a given frequency. The major factors limiting PAE and P_{OUT} in GaN HEMTs are the DC to RF dispersion and thermal effects. DC to RF dispersion, often referred to as current collapse, is caused by electron trapping and leads to reduced performances. Additionally, self-heating occurs at high drain voltages, which has a significant impact on PAE by reducing the electron mobility. Effective thermal management and mitigation of electron trapping are essential to maintain high PAE and output power density.

V.5. GaN HEMTs reliability

Reliability is defined as the ability of a component to perform a required function or mission successfully, without failure or degradation over a specific period. This is particularly important for systems that cannot be maintained during operation, such as satellites and military equipment. The reliability of the final product is highly dependent on the design of the device, the material quality and the fabrication process. Numerous studies have demonstrated that GaN devices offer a unique combination of power and efficiency superior to other technologies. However, there are currently not commercially available GaN foundry processes above 40 GHz with proven long-term reliability.

For GaN HEMTs with short gate lengths (<150 nm), reliability becomes a major issue due to high electric field peaks and high junction temperatures (T_J) that result from the reduced device dimensions. RF devices are subject to a variety of failure mechanisms that affect their reliability. One of the most common is the degradation at the gate edge, which can occur in both the OFF and ON states. High electric field induces hot carrier injection, where high-energy electrons are trapped in dielectrics or on the surface and interfaces below the gate. This can lead to degradation such as, threshold voltage shifts, increased gate leakage current, higher dynamic on-resistance and a drop in output current [127-129]. Trapping activation or reactivation represents another failure mechanism in GaN HEMTs.

This issue arises from defects or impurities within the semiconductor, materials, leading to traps that capture charge carriers. These traps become more prominent under high electric field and elevated junction temperature, significantly degrading the RF performance of the device. Effective junction temperature management is crucial, as devices typically operate at high power densities and generate substantial heat. A high junction temperature can also induce metal-metal interdiffusion, degradation of the ohmic contact and gate metal, as well as delamination of the passivation. **Figure 1.24** summarizes the main mechanisms identified as leading to reliability issues for GaN HEMTs.

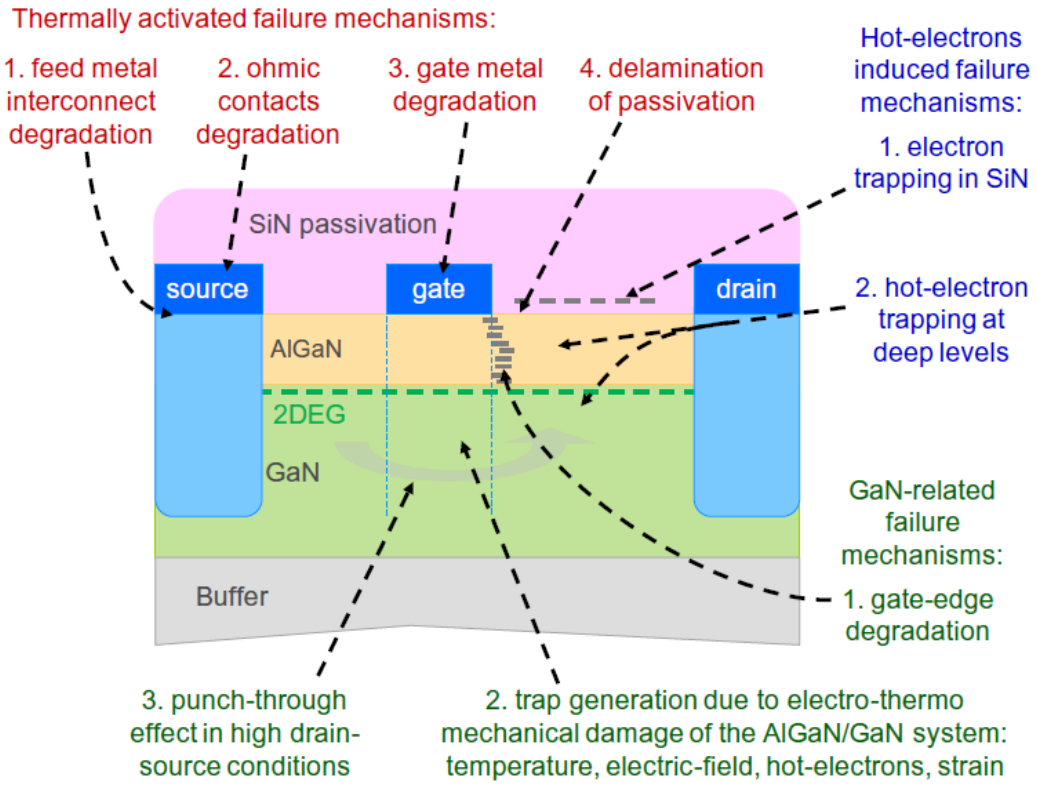


Figure 1.24. Failure mechanisms identified in GaN HEMTs [130].

Two types of tests can be carried out to evaluate the longevity of GaN HEMTs: short-term and long-term reliability tests. Short-term reliability tests are designed to quickly identify potential early-life failures and provide immediate feedback on material quality and device design. These tests typically last from a few hours to a few days and simulate accelerated operating conditions to expose immediate weaknesses. These are DC or large signal tests performed directly on wafer, conducted at various temperature. DC robustness tests are carried out in off-state, semi-on state or on-state conditions. The drain voltage is gradually increased until device breakdown, with continuous monitoring of gate and drain currents to detect failure mechanisms [131]. Similarly, RF robustness tests are conducted by monitoring the device under large signal conditions for several hours at different temperature [132]. However, short-term reliability tests do not provide comprehensive information on long-term degradation kinetics, activation energy, or mean time to failure (MTTF). Consequently, long-term reliability tests are needed to validate the overall reliability of GaN HEMTs before they can be installed on production lines. These tests are represented by the "bathtub" curve, which is divided into three distinct regions, as illustrated in **Figure 1.25.**

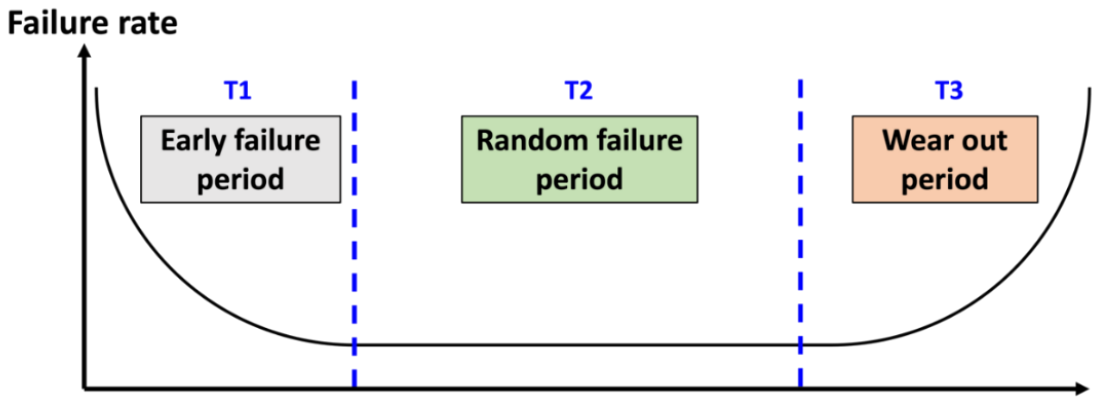


Figure 1.25. Typical bathtub behavior for long-term reliability.

- **Early Failure Period (T1)** : This initial phase is characterized by a high failure rate due to manufacturing defects or early-life weaknesses. Failures are most likely to occur during this period and are often detected through short-term reliability tests or burn-in processes.

- **Random Failure Period (T2)** : After initial failures, the devices enter a stable phase with a low and constant failure rate. This period represents the most reliable phase of the device's life when failures occur randomly. For highly reliable devices, this period should be as long as possible, with a minimal and constant failure rate.
- **Wear-Out Period (T3)** : In the final phase, the failure rate rises sharply as the device approaches the end of its operational life. This increase is due to the gradual degradation of materials and components over time, leading to the inevitable wear-out and final device failure.

Long-term reliability tests, such as High Temperature Operating Life (HTOL), accelerate the aging process of devices by exposing them to high temperatures and electrical stress. This approach helps predict lifespan and identify potential failure mechanisms. HTOL tests can be also carried out under DC and RF conditions. In the case of RF HTOL, an RF signal from the load pull is applied with the device biased in class A or AB. The input power is set at a specific frequency corresponding to the device's peak PAE under high chuck temperatures. The aim of this test is to reach a T_J of around 150°C, which will accelerate the device's lifespan. During the test, key parameters such as PAE, output power (P_{OUT}), and gate leakage current are monitored for any significant changes. This test extends over thousands of hours and requires robust packaging to effectively manage self-heating, which can be complex to set up in a laboratory. However, in this thesis work, short-term HTOL tests were carried out on wafers over several hours to provide an initial indication of the reliability of the studied structures.

V.6. GaN HEMTs linearity

GaN devices are initially evaluated using single-tone power measurements for large signal performances. Nevertheless, the adoption of GaN into communication systems such as 5G network using complex modulation schemes requires additional device evaluation to demonstrate their usefulness in these systems. Indeed, at high frequencies and high data rates, the implementation of circuit level techniques increases system complexity and cost. Therefore, high linearity in GaN devices is crucial to minimize the signal distortion and ensure high-quality signal transmission. Intrinsically, linear devices and circuits reduce the need for pre-distortion, filtering, and the interfering effects of out-of-band signals.

Device linearity is linked to device design and the non-linearity of the transconductance, resistive and capacitive elements of the devices [133, 134]. GaN HEMTs have demonstrated superior RF performance in the millimeter-wave range, but at high frequencies, linearity remains limited, mainly due to self-heating, DC/RF dispersion and the rather abrupt drop in transconductance in on-state conditions.

Many figures of merit are used to evaluate the linearity of GaN power amplifier such as the adjacent channel power ratio (ACPR), The Input Gain Compression Point (P_1dB), The Input Third Order Intercept Point (IIP_3), the Output Third-Order Intercept Point (OIP_3) to DC power consumption ratio (OIP_3/P_{DC}) and the carrier to third-order inter-modulation ratio (C/IM_3). The most reported in the literature for GaN HEMTs are IIP_3, $OIP3/P_{DC}$, and C/IM_3.

- **IIP_3** represents the hypothetical input power level at which the third-order intermodulation component (IM_3) equals the fundamental output power (P_0), serving as a key indicator of the device's linearity and its ability to handle high input power with minimal distortion (**Figure 1.26**).
- **OIP_3/P_{DC}** combines the device's linearity at the output stage and its energy efficiency. It is calculated by dividing the output third-order intercept point (OIP_3), the hypothetical output power level (where $P_0 = IM_3$) by the DC power consumption (P_{DC}). A high OIP_3/P_{DC} ratio means that the device not only maintains good linearity, but also operates efficiently.

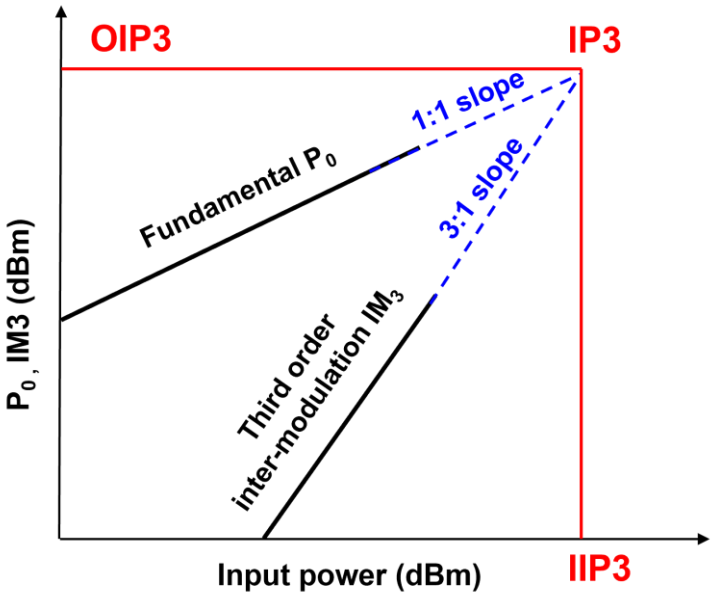


Figure 1.26. Input third order Intercept (IIP3) and output third order intercept point (OIP3).

- **C/IM3 ratio** is an essential measure of linearity that corresponds to the ratio between the power of the fundamental carrier signal and the power of the third-order intermodulation products (IM_3), which are undesirable signals generated due to nonlinearities in the amplifier.

While IIP_3 provides information on linearity on a singular point, the C/I ratio provide data on IM_3 suppression at every input power level. A higher C/IM_3 ratio indicates better linearity, meaning the fundamental signal is much stronger that the distortion products.

VI. State-of-the-art GaN HEMT architecture for mmW applications

GaN-based devices have the potential to revolutionize the field of millimeter-wave solid-state power amplifiers (SSPAs), opening new applications that were previously unfeasible due to the limited output power of SSPAs and large size of traveling wave tube amplifiers (TWTAs). However, industrial RF GaN HEMTs are currently qualified only up to Ka band (30 GHz) using a 150nm gate length. Future telecommunication and earth observation applications will require high-performance GaN based SSPAs available up to the W-band. Nevertheless, reducing the gate length to reach higher frequencies requires a complete overhaul of fundamental epitaxial materials and device design. **Table 1.5** summarizes the specific requirements for sub-100nm gate length GaN-based HEMTs.

Table 1.5. Technical requirements for Ka/W-band GaN HEMTs.

Summary of the technical requirements that must be simultaneously achieved for mmW short GaN-based HEMTs with L_G < 100 nm
High electron confinement and high breakdown voltage
Low trapping effects (current collapse < 15%)
High current and power gain (e.g., F_t/F_{max} > 100/300 GHz)
High PAE (>55%) and P_{OUT} (>3.5 W/mm)
High linearity (C/IM_3 > 30dBc and linear G_M)
High reliability under high junction temperature (T_J = 250°C)

Researchers from diverse laboratories have showcased state-of-the-art performances in the millimeter-wave range using Ga or N-polar heterostructures. This final section aims to outline the most advanced GaN architectures reported in the literature, presenting cutting-edge innovations and breakthroughs in this field.

VI.1. InAlGaN/GaN HEMT from Fujitsu

Figure 1.27 illustrates the cross-section of Fujitsu's advanced InAlGaN/GaN HEMT technology (L_G = 80 nm) and incorporates some engineering aspects [85].

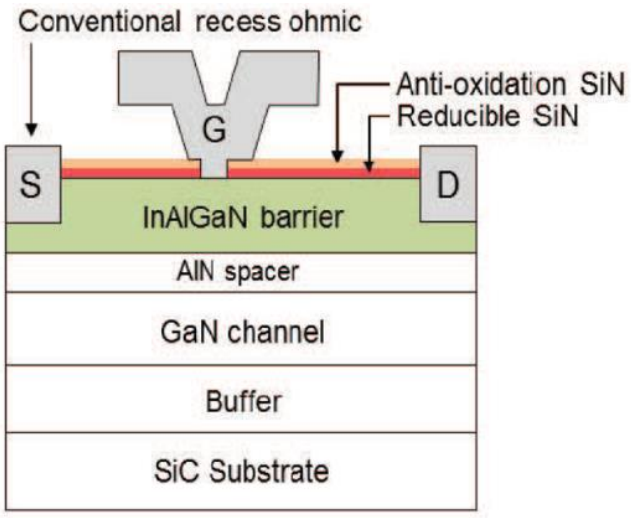


Figure 1.27. Schematic cross section of Fujitsu InAlGaN/GaN HEMTs.

To mitigate the current collapse, a double SiN passivation layer has been implemented and an overhanging Y-shaped gate design is adopted to reduce the electric field without compromising high-frequency performance. Load-pull measurements at 96 GHz indicate a high P_{OUT} of 3 W/mm at V_{DS} = 20V (**Figure 1.28.a**) [85]. However, an improved version of this structure has demonstrated high power operation across a broad frequency range from the S-band to the W-band. This enhancement incorporates regrown n^+ GaN contact layer to reduce contact resistance and an InGaN back barrier to minimize the off-state drain leakage current. A diamond heat spreader is also introduced to lower the thermal resistance and boost the output power density. The maximum pulsed P_{OUT} achieved for this InAlGaN/GaN device was 4.5 W/mm at V_{DS} = 25V (94 GHz) [135].

Nevertheless, no associated PAE have been reported with these output power. Basic reliability was also investigated by monitoring gate leakage (I_G) under pinch-off conditions at V_{DS} = 10V and T_J = 150°C. A slight increase of I_G was reported after 40 hours (**Figure 1.28.b**). Further reliability studies are needed to validate this technology, especially under severe conditions and no linearity has been reported for this technology to date.

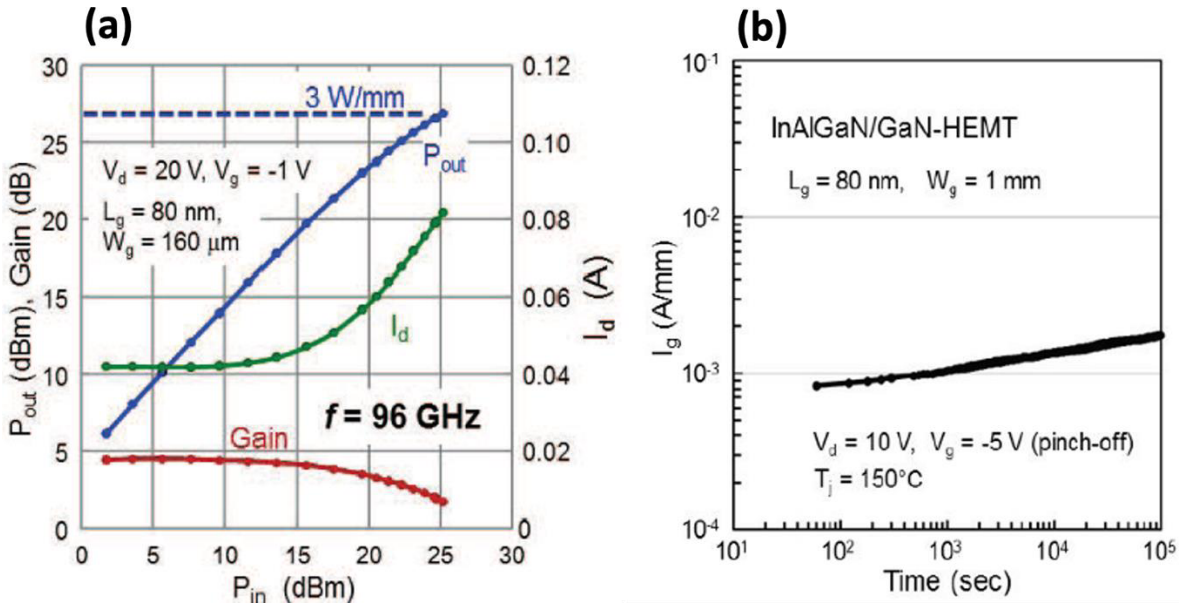


Figure 1.28. (a) RF power performances at 94 GHz and (b) I_G stress at T_J=150°C.

VI.2. N-polar GaN HEMT from UCSB

Recent developments in N-polar GaN devices at the University of California, Santa Barbara (UCSB), indicate significant potential for improving millimeter-wave power applications. UCSB's N-polar deep recess MIS-HEMT, featuring a 48 nm gate length achieved by ruthenium atomic layer deposition (ALD), has demonstrated a high-power gain of 8.1 dB at 94 GHz. A thick GaN cap layer is employed to manage DC and RF dispersion effectively and regrown n^+ GaN contacts are used to improve the maximum drain current. CW load-pull measurements at 94 GHz showed an output power of 6.2 W/mm with a PAE of 33.8% at V_{DS} = 18V (**Figure 1.29**) [136]. Moreover, the N-polar deep recess MIS-HEMT, initially developed for W-band power performance, has been adapted to support Ka-band performance. At 30 GHz, CW high-power performance has been reported with a PAE of 47.4% and an output power of 10.3 W/mm. Two-tone linearity tests under the same bias and matching conditions reveal an OIP_3/P_{DC} ratio greater than 6.7 dB. At 10 dB back-off from peak PAE, a C/I ratio above 37 dBc was obtained, but with a rather low associated PAE of 20% [137].

Lastly, for N-polar HEMT, a record PAE in W-band was recently achieved by adding a thin layer of titanium nitride (TiN) in the Schottky contact. The use of TiN/Ru stack as the Schottky gate metal resulted in a six-fold reduction in reverse-bias leakage current compared with Ru-only counterparts. At 94 GHz and V_{DS} = 12V, the N-polar HEMT achieved a PAE of 53.4%, with an associated P_{OUT} of 3.7 W/mm [138]. Despite state-of-the-art power performances the gate recess method presents challenges, particularly in terms of device reliability. Controlling this method is complex and often leads to degradation of the gate module. Consequently, the long-term reliability of UCSB's devices remains to be demonstrated.

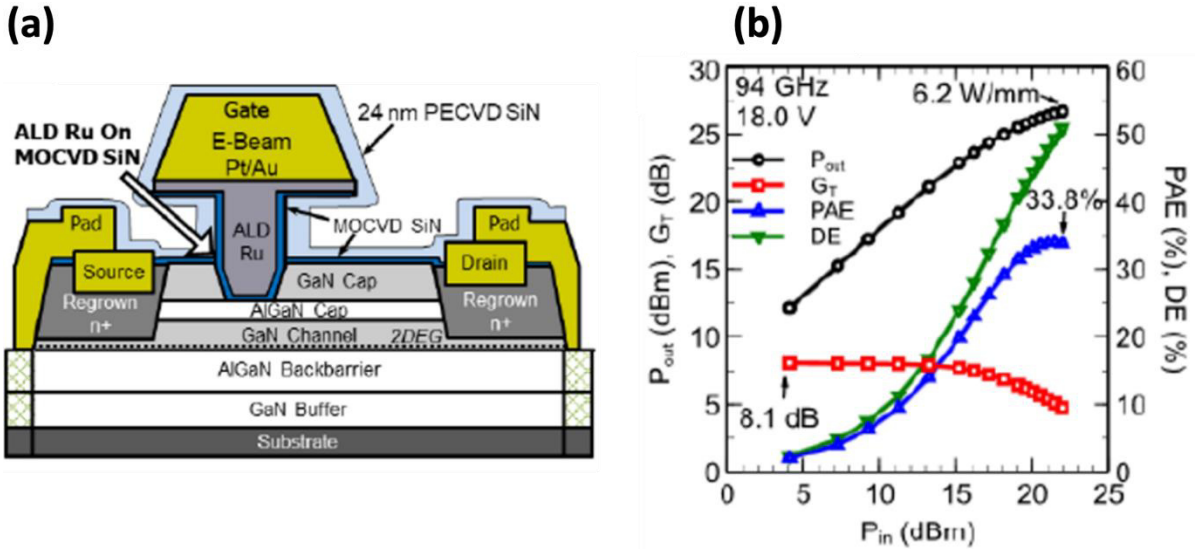


Figure 1.29. (a) Schematic cross-section of UCSB N-polar MIS-HEMT and (b) associated RF power performances at 94 GHz.

VI.3. Multi-channel SLCFET from Northrop Grumman

The Northrop Grumman's super-lattice castellated field-effect transistor (SLCFET) architecture uses a superlattice of stacked, nanoribbon-etched AlGaN/GaN heterostructures, controlled by a 100 nm T-gate that drives the stacked channels from the sidewalls **(Figure 1.30.a)**. This design achieves high carrier density and charge control, resulting in impressive performance. This architecture enables a very high drain current density of 4.8 A/mm. At 94 GHz, the SLCFET achieved the highest P_{OUT} of 10.87 W/mm to date with a PAE of 43%. [139] (**Figure 1.30.b**). Linearity measurements have been conducted up to 30 GHz and a OIP3/PDC ratio above 6 dB has been reported with a transconductance over a wide gate voltage range [140].

However, the complex design, which includes stacked AlGaN/GaN heterostructures and precise etching for nanoribbons and a three-dimensional castellated gate structure, makes the fabrication process more difficult and potentially less reliable than traditional HEMT structures. It is important to note that to date, high reliability with low trapping effects still need to be proven for this technology.

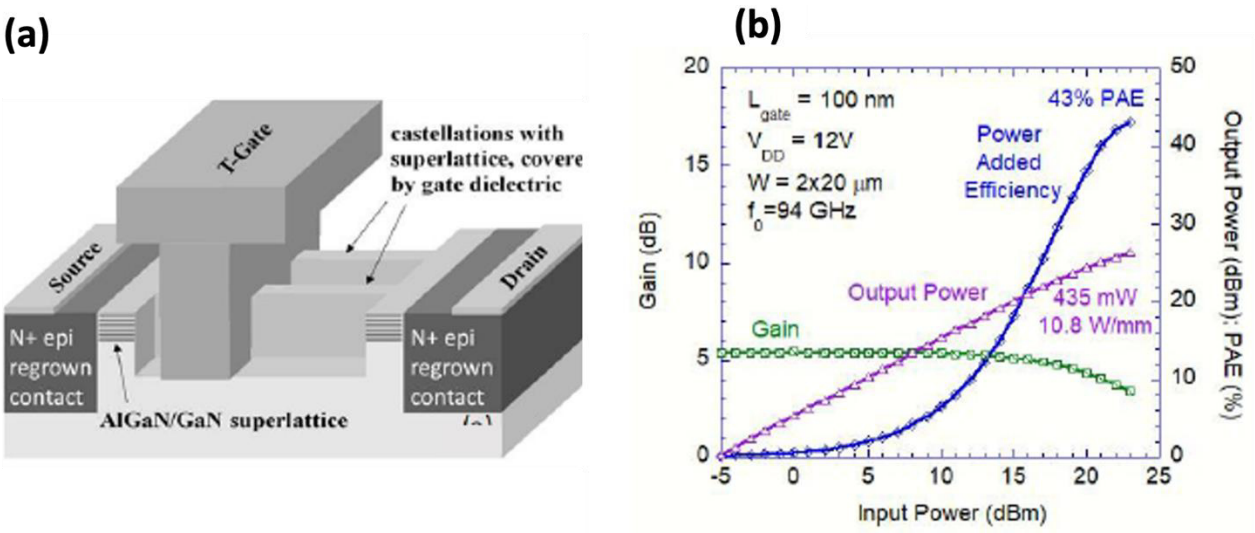


Figure 1.30. (a) Structure of SLCFET technology and (b) RF power performances at 94GHz.

VI.4. Graded AlGaN channel HEMT from HRL

The high-speed AlGaN/GaN graded channel (GC) HEMTs developed by HRL have demonstrated significant potential for high-frequency operation. The structure consists of a 60 nm T-gate, featuring a 6 nm AlGaN layer with an Al-composition gradient from 0% to 10% between the AlGaN barrier and the GaN channel (**Figure 1.31.a**). Large signal CW measurements at 30 GHz showed an impressive PAE of 75% with an output power of 2.1 W/mm at V_{DS} = 10V (**Figure 1.31.b**). At V_{DS} = 14 V and 18 V, the measured P_{OUT} increased to 3.0 W/mm and 3.5 W/mm, with peak PAE of 65 and 50%, respectively [141]. Furthermore, GC AlGaN/GaN HEMTs offer clear advantages over conventional AlGaN/GaN HEMTs, particularly by overcoming the device linearity. At 30 GHz, the graded channel demonstrated excellent linearity with a C/I ratio greater than 30 dBc while maintaining a PAE in excess of 50% [142]. An OIP_3/P_{DC} of 20 dB has also been measured, which is the highest value reported to date for a GaN HEMT [143]. Power performances at 94 GHz has been recently reported, showing a record PAE of 45% for Ga-polar HEMT with an associated output power of 2.1 W/mm at V_{DS} = 14V [73].

The graded AlGaN channel HEMT is the only technology that has demonstrated very high-power performances combined with excellent linearity in millimeter-waves range. However, high reliability under severe conditions has not been reported yet.

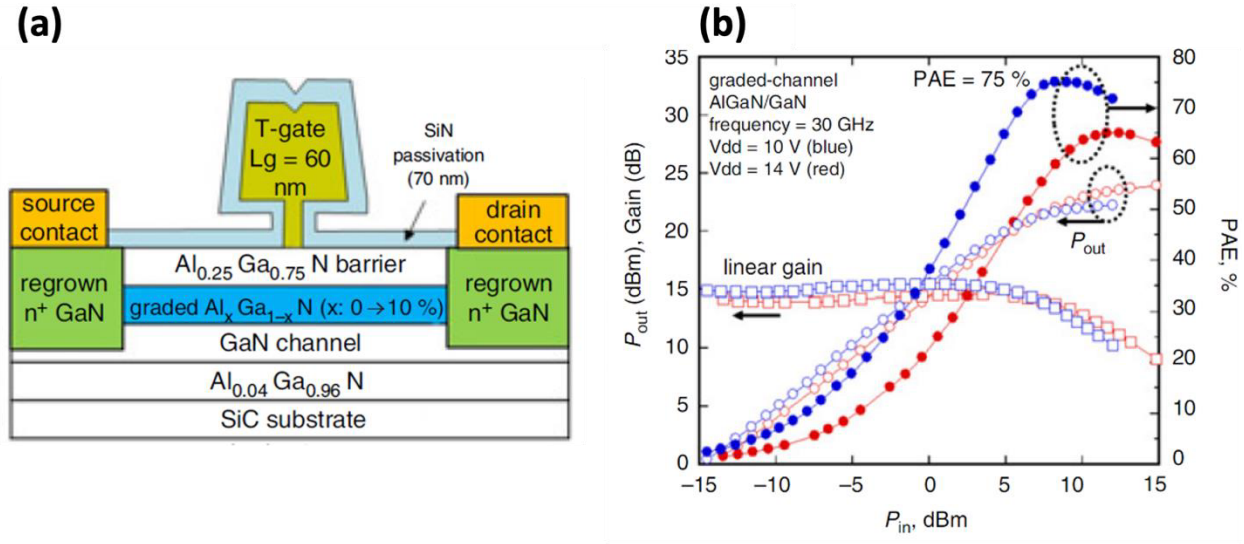


Figure 1.31. (a) Schematic cross-section of the GC AlGaN/GaN HEMT and (b) RF power performances at 30 GHz.

A simulation study has been carried out as part of this thesis to understand why this technology provides such high linearity while maintaining excellent power performance at high frequencies. In particular, we will examine the impact of the AlGaN gradient within the GaN channel on the overall characteristics of the transistor. Chapter II aims to present the objectives and results of this study.

VI.5. AlN/GaN HEMT from IEMN

This architecture is developed in our research group over the last decade. It has both advantages and challenges, which will be discussed below and in detail throughout the manuscript. **Figure 1.32** illustrates a cross-section of a 110 nm AlN/GaN HEMT along with the associated RF power performance. This structure incorporates a high-C doped GaN buffer (C = 2×10^{19} cm^{-3}) followed by a 100 nm GaN channel and a 3 nm AlN barrier layer. Large signal characterizations were carried out in Q-band and W-band. **Figure 1.32.b** reports CW/pulsed power performances at 40 GHz demonstrating a P_{OUT} of 4.3 W/m and 5.1 W/mm with an associated PAE of 58% and 73% at V_{DS} = 30V, respectively [88].

The difference of over 10 points in PAE between CW and pulsed mode is attributed to the high carbon concentration in the buffer with the 100 nm GaN channel. CW large signal characterization at 94 GHz was performed on the same devices, yielding a high output power of 4 W/mm with a PAE of 14.3% at V_{DS}=20V (**Figure 1.32.d**) [44].

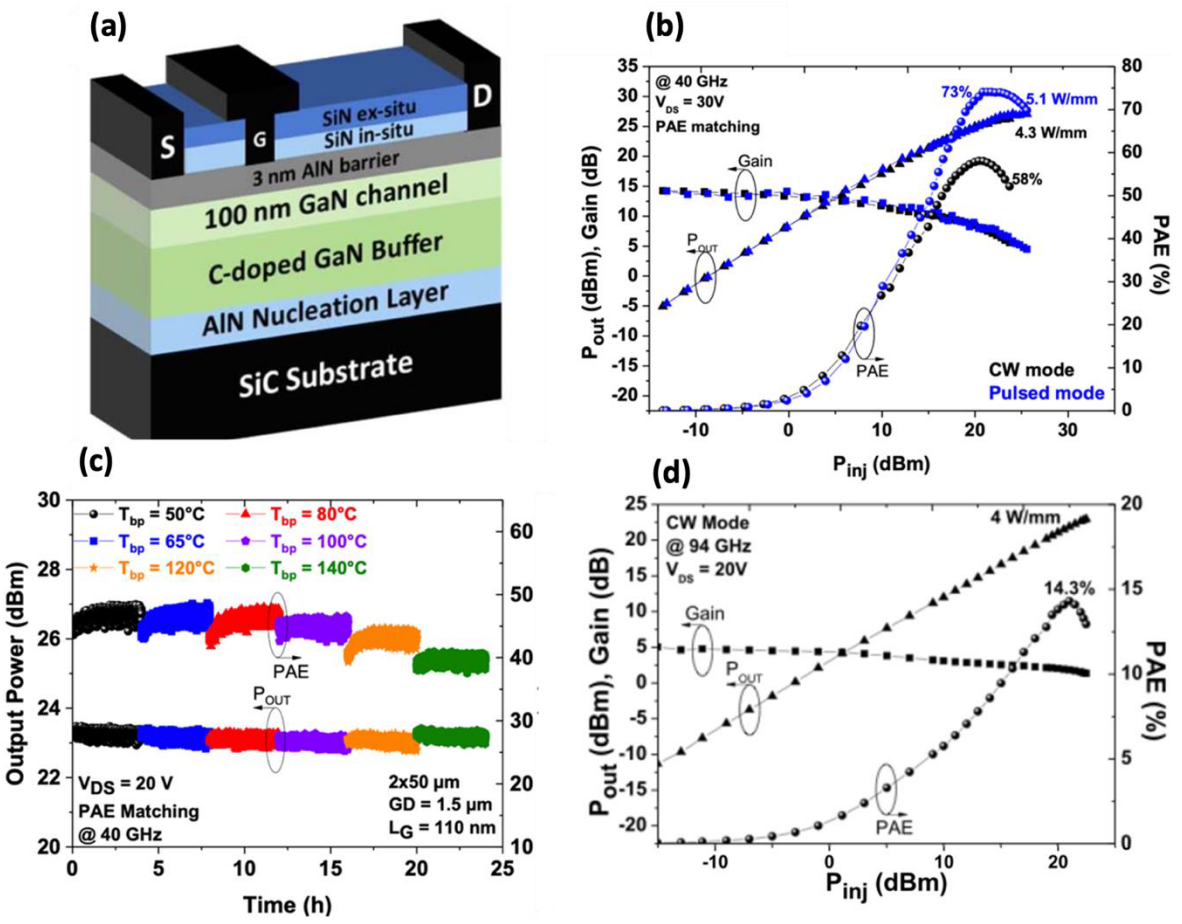


Figure 1.32. (a) AlN/GaN HEMT structure, (b) CW/pulsed power performances at 40 GHz, (c) RF stress for 24 hours at 140°C and (d) power performances at 94 GHz.

RF Short-term reliability assessment up to 140°C **(Figure 1.32.c)** revealed stable output power density and PAE over 24 hours at a drain voltage of V_{DS} = 20 in class AB, with no observed degradation in leakage current [132]. However, further reduction of trapping effects is still necessary to narrow the gap between CW and pulsed conditions and also improve the performance at 94 GHz. Moreover, reliability under high junction temperature needs to be validated at this stage, and linearity should be evaluated. To reduce the gap between CW/pulsed mode, the C-doping should be wisely tuned within the structure in order to reduce trapping effects while maintaining a robust technology.

As indicated in [61], it necessary to find the proper balance between the carbon concentration in the GaN buffer and its distance from the 2DEG to obtain a good electron confinement while avoiding high trapping. To address this concern, a thicker GaN channel of 150 nm was used together with a reduced carbon concentration down to 5×10^{18} cm^{-3}. To prevent drain leakage current and punch-through effect under high electric field, a thin AlGaN back barrier layer was introduced between the C-doped GaN buffer and the GaN channel **(Figure 1.33.a)**. The optimized heterostructure achieves a unique combination of high electron confinement and low trapping effects for gate lengths as short as 100 nm. Experimental results **(Figure 1.33.b)** demonstrated outstanding performance with a record PAE of 70% in pulsed mode and 66.5% in CW mode at 40 GHz with an associated P_{OUT} of 4.2 W/mm and 3.5 W/mm, respectively [65].

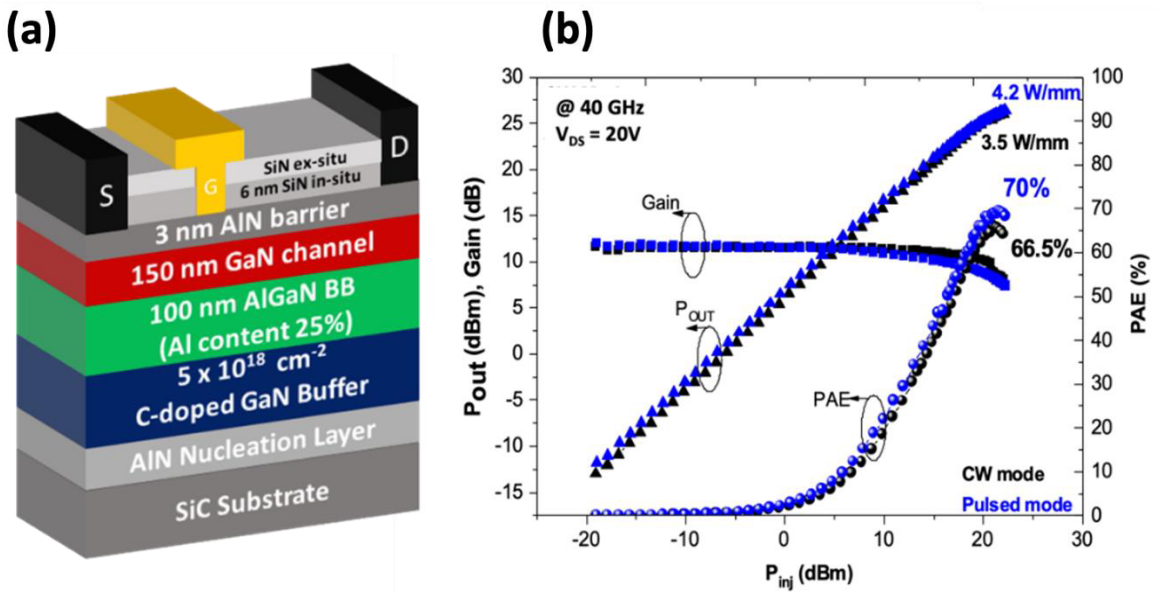


Figure 1.33. (a) AlN/GaN/AlGaN HEMT structure, (b) CW/pulsed power performances at 40 GHz, showing less than 5 point differences between CW and pulsed mode.

The AlN/GaN/AlGaN HEMT has demonstrated state of the art power performances up to Q-band without any degradation of the devices after load pull measurements. In the context of the project GREAT, this structure holds significant interest, particularly to the industrial partners SOITEC and UMS. Consequently, it is essential to primary validate this structure with reliability tests, such as HTOL. As part of this thesis work, short-term HTOL reliability tests have been completed. The AlN/GaN/AlGaN structure forms one of the cornerstones of this thesis (chapter 3).

VI.6. Review of state-of the art GaN HEMTs

Figure 1.34 displays a benchmark of short millimeter-wave GaN devices. In 2005, UCSB reported a record P_{OUT} of 10.5 W/mm at 40 GHz using conventional AlGaN/GaN HEMT technology with a gate length of 160 nm but with a relatively low PAE compared to what can be achieved today [74]. The need to downscale the device and shrink the gate length has led to the emergence of new architectures aimed at surpassing past the performance records of the past.

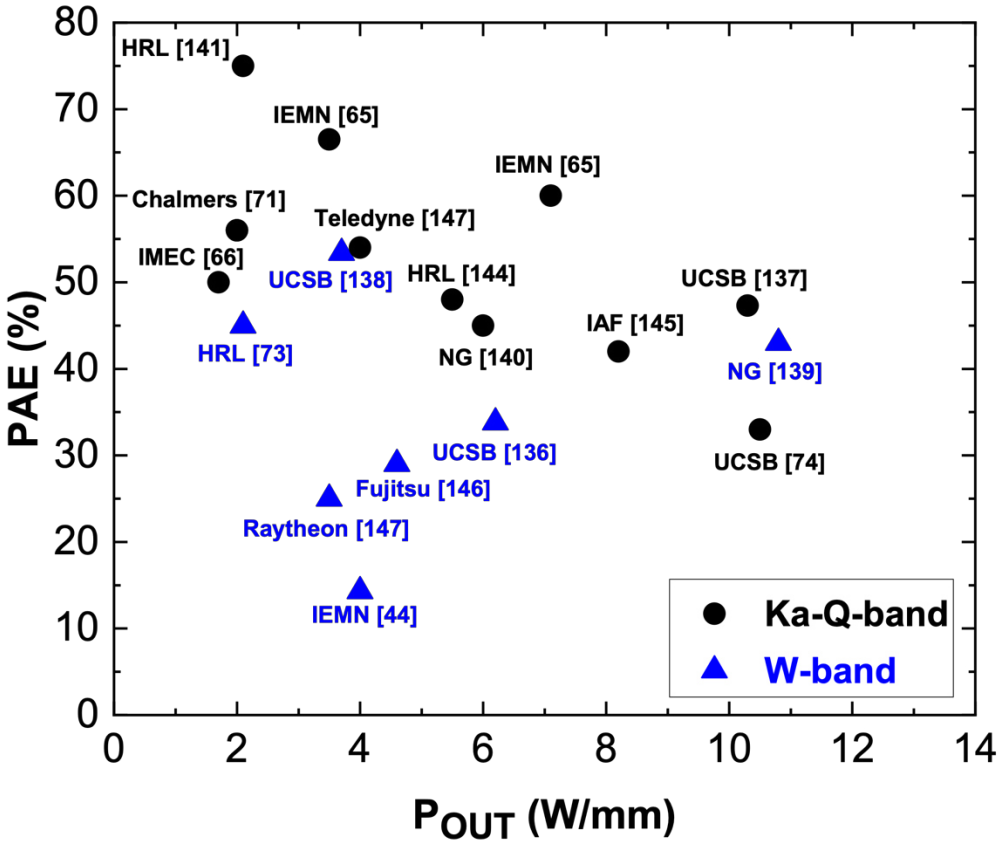


Figure 1.34. Benchmark of PAE as a function of P_{OUT} for mmW GaN HEMTs.

Recently, HRL laboratories developed AlGaN/GaN graded channel HEMTs with an output power density of 2.1 W/mm and a PAE of 75% at 30 GHz [141]. This design also demonstrated the best linearity to date while maintaining very high-power performance at 30 GHz [142, 143]. Measured W-band performance is also the highest reported to date for Ga-polar HEMTs, with a record PAE of 45% [73]. At 40GHz, IEMN laboratory demonstrated ultrathin AlN/GaN/AlGaN back barrier HEMTs achieving a PAE of 66.5% with an associated P_{OUT} of 3.4 W/mm [78].

Additionally, UCSB researchers have shown outstanding performance with N-polar HEMT technology achieving a PAE of 53.4% and a P_{OUT} to 3.7 W/mm at 94 GHz, the highest for N-polar HEMTs [138]. Northrop Grumman demonstrated a P_{OUT} record of 10.8 W/mm with the SLCFET technology at 94 GHz [139]. Finally, the IAF laboratory with ScAlN-based barrier GaN HEMTs [145] and the Teledyne laboratory with Si-doped AlGaN/GaN HEMTs [147] have also reported high power performance in the Ka-band. Each of these technologies demonstrates remarkable performance in the millimeter-wave range. However, none of them has yet demonstrated exceptional reliability, making this factor the highest technical priority for validation.

VII. Conclusion chapter 1

GaN-based devices have emerged as a key technology for millimeter-wave applications due to their outstanding material properties. Recent advancements in GaN device designs have significantly enhanced performance, including high power and high efficiency. These capabilities make GaN devices ideal for variety of millimeter-wave applications, including 5G, satellite communications, and military systems. However, no existing technology meets all mm-wave requirements simultaneously, such as high DC, RF, large signal, linearity, and reliability performances. GaN HEMT devices, especially those with short gate lengths (< 100 nm) face significant reliability challenges. Thermal management, particularly for small devices, and full control of surface and bulk traps are critical to ensuring the required device reliability. In this context, one of the main objectives of this thesis is the development of GaN HEMT devices capable to combine high power, high efficiency, and high reliability for operation in the millimeter-wave range.

References chapter 1

[1] T. S. Rappaport *et al.*, « Wireless Communications and Applications Above 100 GHz: Opportunities and Challenges for 6G and Beyond », *IEEE Access*, vol. 7, p. 78729-78757, 2019, doi: 10.1109/ACCESS.2019.2921522.

[2] H. J. Siweris *et al.*, « Low-cost GaAs pHEMT MMIC's for millimeter-wave sensor applications », *IEEE Trans. Microwave Theory Techn.*, vol. 46, n° 12, p. 2560-2567, déc. 1998, doi: 10.1109/22.739248.

[3] P. M. Smith, « InP-based HEMTs for microwave and millimeter-wave applications », in *Seventh International Conference on Indium Phosphide and Related Materials*, Hokkaido, Japan: IEEE, 1995, p. 68-72. doi: 10.1109/ICIPRM.1995.522078.

[4] C. F. Campbell, D. C. Dumka, M.-Y. Kao, et D. M. Fanning, « High Efficiency Ka-Band Power Amplifier MMIC Utilizing a High Voltage Dual Field Plate GaAs PHEMT Process », in *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Waikoloa, HI, USA: IEEE, oct. 2011, p. 1-4. doi: 10.1109/CSICS.2011.6062436.

[5] C. S. Whelan, « GaN Technology for Microwave and Millimeter Wave Applications », 2010.

[6] *GaN Power Amplifier - Design Solutions*, E-book, septembre 2019.

[7] P. Fayt, M. Fossion, P. Maynadier, et M. Notarianni, « Gan Transistor in Space Equipments: From Selection to Applications », *E3S Web Conf.*, vol. 16, p. 12002, 2017, doi: 10.1051/e3sconf/20171612002.

[8] « https://www.yolegroup.com/product/report/rf-gan-2023/ ».

[9] « https://www.mordorintelligence.com/industry-reports/rf-gan-market ».

[10] S. Li, « The atomic struture of inversion domains and grain boundaries in wurtzite semonconductors: an investigation by atomistic modelling and high resolution transmission electron microscopy ».

[11] F. Bernardini, V. Fiorentini, et D. Vanderbilt, « Spontaneous polarization and piezoelectric constants of III-V nitrides », *Phys. Rev. B*, vol. 56, nº 16, p. R10024-R10027, oct. 1997, doi: 10.1103/PhysRevB.56.R10024.

[12] O. Ambacher *et al.*, « Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures », *Journal of Applied Physics*, vol. 85, nº 6, p. 3222-3233, mars 1999, doi: 10.1063/1.369664.

[13] O. Ambacher *et al.*, « Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures », *J. Phys.: Condens. Matter*, vol. 14, nº 13, p. 3399-3434, avr. 2002, doi: 10.1088/0953-8984/14/13/302.

[14] O. Ambacher *et al.*, « Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures », *Journal of Applied Physics*, vol. 87, nº 1, p. 334-344, janv. 2000, doi: 10.1063/1.371866.

[15] E. F. Roccaforte et M. Leszczynski, « Nitride Semiconductor Technology ».

[16] X. Xu *et al.*, « Wafer-level MOCVD growth of AlGaN/GaN-on-Si HEMT structures with ultra-high room temperature 2DEG mobility », *AIP Advances*, vol. 6, nº 11, p. 115016, nov. 2016, doi: 10.1063/1.4967816.

[17] Y. Zhang *et al.*, « High-Temperature-Recessed Millimeter-Wave AlGaN/GaN HEMTs With 42.8% Power-Added-Efficiency at 35 GHz », *IEEE Electron Device Lett.*, vol. 39, nº 5, p. 727-730, mai 2018, doi: 10.1109/LED.2018.2822259.

[18] S. Karmalkar, M. S. Shur, et R. Gaska, « GaN -BASED POWER HIGH ELECTRON MOBILITY TRANSISTORS », in *Wide Energy Bandgap Electronic Devices*, WORLD SCIENTIFIC, 2003, p. 173-216. doi: 10.1142/9789812796882_0003.

[19] T. Boles, « GaN-on-Silicon – Present capabilities and future directions », présenté à 8TH INTERNATIONAL CONFERENCE ON LOW DIMENSIONAL STRUCTURES AND DEVICES (LDSD 2016), Mayan Riviera, Mexico, 2018, p. 020001. doi: 10.1063/1.5024484.

[20] B. R. Bennett, T. Suemitsu, N. Waldron, et J. A. Del Alamo, « Growth of InP high electron mobility transistor structures with Te doping », *Journal of Crystal Growth*, vol. 278, nº 1-4, p. 596-599, mai 2005, doi: 10.1016/j.jcrysgro.2004.12.070.

[21] D. W. Runton, B. Trabert, J. B. Shealy, et R. Vetury, « History of GaN: High-Power RF Gallium Nitride (GaN) from Infancy to Manufacturable Process and Beyond », *IEEE Microwave*, vol. 14, nº 3, p. 82-93, mai 2013, doi: 10.1109/MMM.2013.2240853.

[22] B. Ozpineci, « WIDE BANDGAP SEMICONDUCTORS FOR UTILITY APPLICATIONS ».

[23] T. Satoh, K. Osawa, et A. Nitta, « GaN HEMT for Space Applications », in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, San Diego, CA: IEEE, oct. 2018, p. 136-139. doi: 10.1109/BCICTS.2018.8551070.

[24] L. M. Porter et R. F. Davis, « A critical review of ohmic and rectifying contacts for silicon carbide », *Materials Science and Engineering: B*, vol. 34, nº 2-3, p. 83-105, nov. 1995, doi: 10.1016/0921-5107(95)01276-1.

[25] H. Jain, S. Rajawat, et P. Agrawal, « Comparision of wide band gap semiconductors for power electronics applications », in *2008 International Conference on Recent Advances in Microwave Theory and Applications*, Jaipur, Rajasthan, India: IEEE, nov. 2008, p. 878-881. doi: 10.1109/AMTA.2008.4763184.

[26] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, et W. L. Pribble, « A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs », *IEEE Trans. Microwave Theory Techn.*, vol. 60, nº 6, p. 1764-1783, juin 2012, doi: 10.1109/TMTT.2012.2187535.

[27] M. R. Duffy, G. Lasser, G. Nevett, M. Roberg, et Z. Popovic, « A Three-Stage 18.5–24-GHz GaN-on-SiC 4 W 40% Efficient MMIC PA », *IEEE J. Solid-State Circuits*, vol. 54, nº 9, p. 2402-2410, sept. 2019, doi: 10.1109/JSSC.2019.2924087.

[28] B. Schmukler *et al.*, « A High Efficiency, Ka-Band, GaN-on-SiC MMIC with Low Compression », in *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Nashville, TN, USA: IEEE, nov. 2019, p. 1-4. doi: 10.1109/BCICTS45179.2019.8972749.

[29] Y. Zhang *et al.*, « Charge control and mobility in AlGaNÕGaN transistors: Experimental and theoretical studies », *J. Appl. Phys.*, vol. 87, nº 11, 2000.

[30] J. Ligl *et al.*, « Metalorganic chemical vapor phase deposition of AlScN/GaN heterostructures », *Journal of Applied Physics*, vol. 127, nº 19, p. 195704, mai 2020, doi: 10.1063/5.0003095.

[31] A. E. Wickenden *et al.*, « The influence of OMVPE growth pressure on the morphology, compensation, and doping of GaN and related alloys », *Journal of Elec Materi*, vol. 29, nº 1, p. 21-26, janv. 2000, doi: 10.1007/s11664-000-0088-2.

[32] C. R. Abernathy, J. D. MacKenzie, et S. M. Donovan, « Growth of group III nitrides by metalorganic molecular beam epitaxy », *Journal of Crystal Growth*, vol. 178, nº 1-2, p. 74-86, juin 1997, doi: 10.1016/S0022-0248(97)00074-2.

[33] H. Tang, S. Rolfe, F. Semond, J. A. Bardwell, et J. M. Baribeau, « Mechanisms of ammonia—MBE growth of GaN on SiC for transport devices », *Journal of Crystal Growth*, vol. 311, nº 7, p. 2091-2095, mars 2009, doi: 10.1016/j.jcrysgro.2008.10.052.

[34] S. Barbara, « MOCVD Growth Technologies for Applications in AlGaN/GaN High Electron Mobility Transistors ».

[35] S. Hu, S. Liu, Z. Zhang, H. Yan, Z. Gan, et H. Fang, « A novel MOCVD reactor for growth of high-quality GaN-related LED layers », *Journal of Crystal Growth*, vol. 415, p. 72-77, avr. 2015, doi: 10.1016/j.jcrysgro.2014.12.038.

[36] B. Godejohann *et al.*, « AlN/GaN HEMTs grown by MBE and MOCVD: Impact of Al distribution », *Physica Status Solidi (b)*, vol. 254, nº 8, p. 1600715, août 2017, doi: 10.1002/pssb.201600715.

[37] L. Liu et J. H. Edgar, « Substrates for gallium nitride epitaxy », *Materials Science and Engineering: R: Reports*, vol. 37, nº 3, p. 61-127, avr. 2002, doi: 10.1016/S0927-796X(02)00008-6.

[38] K. Iniewski, « Devices, Circuits, and Systems », 2016.

[39] R. Cuerdo *et al.*, « High temperature behaviour of GaN HEMT devices on Si(111) and sapphire substrates », *Phys. Status Solidi (c)*, vol. 5, nº 6, p. 1971-1973, mai 2008, doi: 10.1002/pssc.200778555.

[40] F. Iucolano et T. Boles, « GaN-on-Si HEMTs for wireless base stations », *Materials Science in Semiconductor Processing*, vol. 98, p. 100-105, août 2019, doi: 10.1016/j.mssp.2019.03.032.

[41] S. Hoshi *et al.*, « 12.88 W/mm GaN High Electron Mobility Transistor on Silicon Substrate for High Voltage Operation », *Appl. Phys. Express*, vol. 2, p. 061001, juin 2009, doi: 10.1143/APEX.2.061001.

[42] J.-S. Moon *et al.*, « 360 GHz f_{MAX} Graded-Channel AlGaN/GaN HEMTs for mmW Low-Noise Applications », *IEEE Electron Device Lett.*, vol. 41, nº 8, p. 1173-1176, août 2020, doi: 10.1109/LED.2020.3005337.

[43] J. S. Moon *et al.*, « Gate-recessed AlGaN-GaN HEMTs for high-performance millimeter-wave applications », *IEEE Electron Device Lett.*, vol. 26, nº 6, p. 348-350, juin 2005, doi: 10.1109/LED.2005.848107.

[44] K. Harrouche, R. Kabouche, E. Okada, et F. Medjdoub, « High Performance and Highly Robust AlN/GaN HEMTs for Millimeter-Wave Operation », *IEEE J. Electron Devices Soc.*, vol. 7, p. 1145-1150, 2019, doi: 10.1109/JEDS.2019.2952314.

[45] J. J. Freedsman, A. Watanabe, Y. Yamaoka, T. Kubo, et T. Egawa, « Influence of AlN nucleation layer on vertical breakdown characteristics for GaN-on-Si », *Physica Status Solidi (a)*, vol. 213, nº 2, p. 424-428, févr. 2016, doi: 10.1002/pssa.201532601.

[46] J.-T. Chen *et al.*, « Low thermal resistance of a GaN-on-SiC transistor structure with improved structural properties at the interface », *Journal of Crystal Growth*, vol. 428, p. 54-58, oct. 2015, doi: 10.1016/j.jcrysgro.2015.07.021.

[47] G. J. Riedel *et al.*, « Reducing Thermal Resistance of AlGaN/GaN Electronic Devices Using Novel Nucleation Layers », *IEEE Electron Device Lett.*, vol. 30, nº 2, p. 103-106, févr. 2009, doi: 10.1109/LED.2008.2010340.

[48] G. H. Jessen *et al.*, « Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices », *IEEE Trans. Electron Devices*, vol. 54, nº 10, p. 2589-2597, oct. 2007, doi: 10.1109/TED.2007.904476.

[49] M. J. Uren *et al.*, « Punch-through in short-channel AlGaN/GaN HFETs », *IEEE Trans. Electron Devices*, vol. 53, nº 2, p. 395-398, févr. 2006, doi: 10.1109/TED.2005.862702.

[50] M. J. Uren, J. Moreke, et M. Kuball, « Buffer Design to Minimize Current Collapse in GaN/AlGaN HFETs », *IEEE Trans. Electron Devices*, vol. 59, nº 12, p. 3327-3333, déc. 2012, doi: 10.1109/TED.2012.2216535.

[51] K.-P. Chang, P.-J. Lin, R.-H. Horng, et D.-S. Wuu, « Growth characteristics of Fe-doped GaN epilayers on SiC (001) substrates and their effects on high breakdown voltage devices », *Materials Science in Semiconductor Processing*, vol. 119, p. 105228, nov. 2020, doi: 10.1016/j.mssp.2020.105228.

[52] F. Jia *et al.*, « The Influence of Fe Doping Tail in Unintentionally Doped GaN Layer on DC and RF Performance of AlGaN/GaN HEMTs », *IEEE Trans. Electron Devices*, vol. 68, nº 12, p. 6069-6075, déc. 2021, doi: 10.1109/TED.2021.3123113.

[53] V. Desmaris *et al.*, « Comparison of the DC and Microwave Performance of AlGaN/GaN HEMTs Grown on SiC by MOCVD With Fe-Doped or Unintentionally Doped GaN Buffer Layers », *IEEE Trans. Electron Devices*, vol. 53, nº 9, p. 2413-2417, sept. 2006, doi: 10.1109/TED.2006.880825.

[54] M. Meneghini *et al.*, « Buffer Traps in Fe-Doped AlGaN/GaN HEMTs: Investigation of the Physical Properties Based on Pulsed and Transient Measurements », *IEEE Trans. Electron Devices*, vol. 61, nº 12, p. 4070-4077, déc. 2014, doi: 10.1109/TED.2014.2364855.

[55] S. Heikman, S. Keller, S. P. DenBaars, et U. K. Mishra, « Growth of Fe doped semi-insulating GaN by metalorganic chemical vapor deposition », *Applied Physics Letters*, vol. 81, nº 3, p. 439-441, juill. 2002, doi: 10.1063/1.1490396.

[56] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Wurfl, et G. Trankle, « AlGaN/GaN/GaN:C Back-Barrier HFETs With Breakdown Voltage of Over 1 kV and Low $R_{\scriptscriptstyle{\rm ON}} \times A$ », *IEEE Trans. Electron Devices*, vol. 57, nº 11, p. 3050-3058, nov. 2010, doi: 10.1109/TED.2010.2069566.

[57] R. Kabouche *et al.*, « Comparison of C-Doped AlN/GaN HEMTs and AlN/GaN/AlGaN Double Heterostructure for mmW Applications », in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid: IEEE, sept. 2018, p. 5-8. doi: 10.23919/EuMIC.2018.8539962.

[58] J. Bergsten *et al.*, « Electron Trapping in Extended Defects in Microwave AlGaN/GaN HEMTs With Carbon-Doped Buffers », *IEEE Trans. Electron Devices*, vol. 65, nº 6, p. 2446-2453, juin 2018, doi: 10.1109/TED.2018.2828410.

[59] J. L. Lyons, A. Janotti, et C. G. Van De Walle, « Carbon impurities and the yellow luminescence in GaN », *Applied Physics Letters*, vol. 97, nº 15, p. 152108, oct. 2010, doi: 10.1063/1.3492841.

[60] J. L. Lyons, A. Janotti, et C. G. Van De Walle, « Effects of carbon on the electrical and optical properties of InN, GaN, and AlN », *Phys. Rev. B*, vol. 89, nº 3, p. 035204, janv. 2014, doi: 10.1103/PhysRevB.89.035204.

[61] K. Harrouche, S. Venkatachalam, F. Grandpierron, E. Okada, et F. Medjdoub, « Impact of undoped channel thickness and carbon concentration on AlN/GaN-on-SiC HEMT performances », *Appl. Phys. Express*, vol. 15, nº 11, p. 116504, nov. 2022, doi: 10.35848/1882-0786/ac9c46.

[62] F. Medjdoub, M. Zegaoui, B. Grimbert, N. Rolland, et P.-A. Rolland, « Effects of AlGaN Back Barrier on AlN/GaN-on-Silicon High-Electron-Mobility Transistors », *Appl. Phys. Express*, vol. 4, nº 12, p. 124101, nov. 2011, doi: 10.1143/APEX.4.124101.

[63] A. Shanbhag, F. Grandpierron, K. Harrouche, et F. Medjdoub, « Physical Insights of thin AlGaN Back Barrier for millimeter-wave high voltage AlN/GaN on SiC HEMTs ».

[64] D. S. Lee, X. Gao, S. Guo, et T. Palacios, « InAlN/GaN HEMTs With AlGaN Back Barriers », *IEEE Electron Device Lett.*, vol. 32, nº 5, p. 617-619, mai 2011, doi: 10.1109/LED.2011.2111352.

[65] K. Harrouche, S. Venkatachalam, L. Ben-Hammou, F. Grandpierron, E. Okada, et F. Medjdoub, « Low Trapping Effects and High Electron Confinement in Short AlN/GaN-On-SiC HEMTs by Means of a Thin AlGaN Back Barrier », *Micromachines*, vol. 14, nº 2, p. 291, janv. 2023, doi: 10.3390/mi14020291.

[66] R. ElKashlan *et al.*, « A Composite AlGaN/cGaN Back Barrier for mm-Wave GaN-on-Si HEMTs », in *ESSDERC 2023 - IEEE 53rd European Solid-State Device Research*

Conference (ESSDERC), Lisbon, Portugal: IEEE, sept. 2023, p. 152-155. doi: 10.1109/ESSDERC59256.2023.10268539.

[67] L. He *et al.*, « The influence of Al composition in AlGaN back barrier layer on leakage current and dynamic R_{ON} characteristics of AlGaN/GaN HEMTs: Influence of Al composition on characteristics of AlGaN/GaN HEMTs », *Phys. Status Solidi A*, vol. 214, nº 8, p. 1600824, août 2017, doi: 10.1002/pssa.201600824.

[68] W. Liu et A. A. Balandin, « Thermal conduction in AlxGa1−xN alloys and thin films », *Journal of Applied Physics*, vol. 97, nº 7, p. 073710, avr. 2005, doi: 10.1063/1.1868876.

[69] J.-T. Chen *et al.*, « A GaN–SiC hybrid material for high-frequency and power electronics », *Applied Physics Letters*, vol. 113, nº 4, p. 041605, juill. 2018, doi: 10.1063/1.5042049.

[70] D.-Y. Chen *et al.*, « Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors », *IEEE Electron Device Lett.*, vol. 41, nº 6, p. 828-831, juin 2020, doi: 10.1109/LED.2020.2988074.

[71] D.-Y. Chen *et al.*, « Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High Breakdown Buffer-Free AlGaN/GaN Heterostructures », *Physica Status Solidi (a)*, vol. 220, nº 16, p. 2200496, août 2023, doi: 10.1002/pssa.202200496.

[72] C.-R. Huang *et al.*, « Thermally stable radio frequency power and noise behaviors of AlGaN/GaN high electron mobility transistor without voltage-blocking buffer layer design », *Journal of Vacuum Science & Technology B*, vol. 42, nº 4, p. 043201, juill. 2024, doi: 10.1116/6.0003551.

[73] J.-S. Moon *et al.*, « *W* -Band Graded-Channel GaN HEMTs With Record 45% Power-Added-Efficiency at 94 GHz », *IEEE Microw. Wireless Tech. Lett.*, vol. 33, nº 2, p. 161-164, févr. 2023, doi: 10.1109/LMWC.2022.3207978.

[74] T. Palacios *et al.*, « High-power AlGaN/GaN HEMTs for Ka-band applications », *IEEE Electron Device Lett.*, vol. 26, nº 11, p. 781-783, nov. 2005, doi: 10.1109/LED.2005.857701.

[75] V. Tilak *et al.*, « Influence of barrier thickness on the high-power performance of AlGaN/GaN HEMTs », *IEEE Electron Device Lett.*, vol. 22, nº 11, p. 504-506, nov. 2001, doi: 10.1109/55.962644.

[76] M. Higashiwaki et T. Matsui, « Barrier Thickness Dependence of Electrical Properties and DC Device Characteristics of AlGaN/GaN Heterostructure Field-Effect Transistors Grown by Plasma-Assisted Molecular-Beam Epitaxy », *Jpn. J. Appl. Phys.*, vol. 43, nº 9A, p. L1147, sept. 2004, doi: 10.1143/JJAP.43.L1147.

[77] J. Kuzmik, « Power electronics on InAlN/(In)GaN: Prospect for a record performance », *IEEE Electron Device Lett.*, vol. 22, nº 11, p. 510-512, nov. 2001, doi: 10.1109/55.962646.

[78] M. Gonschorek, J.-F. Carlin, E. Feltin, M. A. Py, et N. Grandjean, « High electron mobility lattice-matched AlInN⁄GaN field-effect transistor heterostructures », *Applied Physics Letters*, vol. 89, nº 6, p. 062106, août 2006, doi: 10.1063/1.2335390.

[79] F. Medjdoub *et al.*, « Can InAlN/GaN be an alternative to high power / high temperature AlGaN/GaN devices? », in *2006 International Electron Devices Meeting*, San Francisco, CA: IEEE, déc. 2006, p. 1-4. doi: 10.1109/IEDM.2006.346935.

[80] Y. Yue *et al.*, « Ultrascaled InAlN/GaN High Electron Mobility Transistors with Cutoff Frequency of 400 GHz », *Jpn. J. Appl. Phys.*, vol. 52, nº 8S, p. 08JN14, août 2013, doi: 10.7567/JJAP.52.08JN14.

[81] D. S. Lee, X. Gao, S. Guo, D. Kopp, P. Fay, et T. Palacios, « 300-GHz InAlN/GaN HEMTs With InGaN Back Barrier », *IEEE Electron Device Lett.*, vol. 32, nº 11, p. 1525-1527, nov. 2011, doi: 10.1109/LED.2011.2164613.

[82] A. Crespo *et al.*, « High-Power Ka-Band Performance of AlInN/GaN HEMT With 9.8-nm-Thin Barrier », *IEEE Electron Device Lett.*, vol. 31, nº 1, p. 2-4, janv. 2010, doi: 10.1109/LED.2009.2034875.

[83] N. Ketteniss *et al.*, « Study on quaternary AlInGaN/GaN HFETs grown on sapphire substrates », *Semicond. Sci. Technol.*, vol. 25, nº 7, p. 075013, juill. 2010, doi: 10.1088/0268-1242/25/7/075013.

[84] R. Wang *et al.*, « Quaternary Barrier InAlGaN HEMTs With $f_{T}/f_{\max}$ of 230/300 GHz », *IEEE Electron Device Lett.*, vol. 34, nº 3, p. 378-380, mars 2013, doi: 10.1109/LED.2013.2238503.

[85] K. Makiyama *et al.*, « Collapse-free high power InAlGaN/GaN-HEMT with 3 W/mm at 96 GHz », in *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, USA: IEEE, déc. 2015, p. 9.1.1-9.1.4. doi: 10.1109/IEDM.2015.7409659.

[86] F. A. Faria, K. Nomoto, Z. Hu, S. Rouvimov, H. (Grace) Xing, et D. Jena, « Low temperature AlN growth by MBE and its application in HEMTs », *Journal of Crystal Growth*, vol. 425, p. 133-137, sept. 2015, doi: 10.1016/j.jcrysgro.2015.03.039.

[87] S. M. Hubbard, D. Pavlidis, V. Valiaev, et A. Eisenbach, « Metal-organic vapor phase epitaxy growth and characterization of AlN/GaN heterostructures », *Journal of Elec Materi*, vol. 31, nº 5, p. 395-401, mai 2002, doi: 10.1007/s11664-002-0090-y.

[88] K. Harrouche, R. Kabouche, E. Okada, et F. Medjdoub, « High Power AlN/GaN HEMTs with record power-added-efficiency >70% at 40 GHz », in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA: IEEE, août 2020, p. 285-288. doi: 10.1109/IMS30576.2020.9223971.

[89] H. Sun *et al.*, « Investigation of the Trap States and V_{TH} Instability in LPCVD Si_3N_4/AlGaN/GaN MIS-HEMTs with an *In-Situ* Si_3N_4 Interfacial Layer », *IEEE Trans. Electron Devices*, vol. 66, nº 8, p. 3290-3295, août 2019, doi: 10.1109/TED.2019.2919246.

[90] Y. Xia *et al.*, « Effects of the cap layer on the properties of AlN barrier HEMT grown on 6-inch Si(111) substrate », *Mater. Res. Express*, vol. 7, nº 6, p. 065902, juin 2020, doi: 10.1088/2053-1591/ab96f5.

[91] J. W. Chung, W. E. Hoke, E. M. Chumbes, et T. Palacios, « AlGaN/GaN HEMT With 300-GHz $f_{\max}$ », *IEEE Electron Device Lett.*, vol. 31, nº 3, p. 195-197, mars 2010, doi: 10.1109/LED.2009.2038935.

[92] T. Palacios *et al.*, « Optimization of AlGaN/GaN HEMTs for high frequency operation », *Physica Status Solidi (a)*, vol. 203, nº 7, p. 1845-1850, mai 2006, doi: 10.1002/pssa.200565384.

[93] K. Shinohara *et al.*, « Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications », *IEEE Trans. Electron Devices*, vol. 60, nº 10, p. 2982-2996, oct. 2013, doi: 10.1109/TED.2013.2268160.

[94] Y. Tang *et al.*, « Ultrahigh-Speed GaN High-Electron-Mobility Transistors With $f_{T}/f_{\mathrm {max}}$ of 454/444 GHz », *IEEE Electron Device Lett.*, vol. 36, nº 6, p. 549-551, juin 2015, doi: 10.1109/LED.2015.2421311.

[95] K. Shinohara *et al.*, « Self-aligned-gate GaN-HEMTs with heavily-doped n+-GaN ohmic contacts to 2DEG », in *2012 International Electron Devices Meeting*, San Francisco, CA, USA: IEEE, déc. 2012, p. 27.2.1-27.2.4. doi: 10.1109/IEDM.2012.6479113.

[96] D. Denninghoff, J. Lu, M. Laurent, E. Ahmadi, S. Keller, et U. K. Mishra, « N-polar GaN/InAlN MIS-HEMT with 400-GHz ƒmax », in *70th Device Research Conference*, University Park, PA, USA: IEEE, juin 2012, p. 151-152. doi: 10.1109/DRC.2012.6256939.

[97] I. Milosavljevic *et al.*, « Vertically scaled GaN/AlN DH-HEMTs with regrown n+GaN ohmic contacts by MBE », in *68th Device Research Conference*, Notre Dame, IN, USA: IEEE, juin 2010, p. 159-160. doi: 10.1109/DRC.2010.5551886.

[98] M. Higashiwaki, T. Mimura, et T. Matsui, « AlGaN/GaN Heterostructure Field-Effect Transistors on 4H-SiC Substrates with Current-Gain Cutoff Frequency of 190 GHz », *Appl. Phys. Expr.*, vol. 1, p. 021103, févr. 2008, doi: 10.1143/APEX.1.021103.

[99] M. Asif Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burm, et M. S. Shur, « Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor », *Applied Physics Letters*, vol. 65, nº 9, p. 1121-1123, août 1994, doi: 10.1063/1.112116.

[100] S. Tirelli *et al.*, « Fully Passivated AlInN/GaN HEMTs With $f_{\rm T}/f_{\rm MAX}$ of 205/220 GHz », *IEEE Electron Device Lett.*, vol. 32, nº 10, p. 1364-1366, oct. 2011, doi: 10.1109/LED.2011.2162087.

[101] V. Kumar *et al.*, « AlGaN/GaN HEMTs on SiC with f/sub T/ of over 120 GHz », *IEEE Electron Device Lett.*, vol. 23, nº 8, p. 455-457, août 2002, doi: 10.1109/LED.2002.801303.

[102] M. L. Schuette *et al.*, « Gate-recessed integrated E/D GaN HEMT technology with f_T/f_{max} >300 GHz », *IEEE Electron Device Lett.*, vol. 34, nº 6, p. 741-743, juin 2013, doi: 10.1109/LED.2013.2257657.

[103] Y. Durmus, D. Yilmaz, A. Toprak, A. B. Turhan, O. A. Sen, et E. Ozbay, « AlGaN/GaN HEMT with fT:100GHz and fmax:128GHz », in *2015 10th European Microwave Integrated Circuits Conference (EuMIC)*, Paris, France: IEEE, sept. 2015, p. 199-202. doi: 10.1109/EuMIC.2015.7345103.

[104] V. G. Mokerov *et al.*, « AlGaN/GaN-HEMTs with a breakdown voltage higher than 100 V and maximum oscillation frequency f max as high as 100 GHz », *Semiconductors*, vol. 43, nº 4, p. 537-543, avr. 2009, doi: 10.1134/S1063782609040253.

[105] Haifeng Sun *et al.*, « 100-nm-Gate (Al,In)N/GaN HEMTs Grown on SiC With ${F}_{ \rm T} = \hbox{144}\ \hbox{GHz}$ », *IEEE Electron Device Lett.*, vol. 31, nº 4, p. 293-295, avr. 2010, doi: 10.1109/LED.2009.2039845.

[106] J. W. Chung, Tae-Woo Kim, et T. Palacios, « Advanced gate technologies for state-of-the-art fT in AlGaN/GaN HEMTs », in *2010 International Electron Devices Meeting*, San Francisco, CA, USA: IEEE, déc. 2010, p. 30.2.1-30.2.4. doi: 10.1109/IEDM.2010.5703449.

[107] Haifeng Sun *et al.*, « 205-GHz (Al,In)N/GaN HEMTs », *IEEE Electron Device Lett.*, vol. 31, nº 9, p. 957-959, sept. 2010, doi: 10.1109/LED.2010.2055826.

[108] A. L. Corrion *et al.*, « Enhancement-Mode AlN/GaN/AlGaN DHFET With 700-mS/mm g_{m} and 112-GHz f_{T} », *IEEE Electron Device Lett.*, vol. 31, nº 10, p. 1116-1118, oct. 2010, doi: 10.1109/LED.2010.2058845.

[109] K. Shinohara *et al.*, « Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency », in *2011 International Electron Devices Meeting*, Washington, DC, USA: IEEE, déc. 2011, p. 19.1.1-19.1.4. doi: 10.1109/IEDM.2011.6131582.

[110] G. Greco, F. Iucolano, et F. Roccaforte, « Ohmic contacts to Gallium Nitride materials », *Applied Surface Science*, vol. 383, p. 324-345, oct. 2016, doi: 10.1016/j.apsusc.2016.04.016.

[111] R. Gong *et al.*, « Analysis of surface roughness in Ti/Al/Ni/Au Ohmic contact to AlGaN/GaN high electron mobility transistors », *Applied Physics Letters*, vol. 97, nº 6, p. 062115, août 2010, doi: 10.1063/1.3479928.

[112] X. Kong, K. Wei, G. Liu, et X. Liu, « Role of Ti/Al relative thickness in the formation mechanism of Ti/Al/Ni/Au Ohmic contacts to AlGaN/GaN heterostructures », *J. Phys. D: Appl. Phys.*, vol. 45, nº 26, p. 265101, juill. 2012, doi: 10.1088/0022-3727/45/26/265101.

[113] Y.-K. Lin *et al.*, « A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs », *Semicond. Sci. Technol.*, vol. 33, nº 9, p. 095019, sept. 2018, doi: 10.1088/1361-6641/aad7a8.

[114] S. Riedmüller, C. Steinmann, J. Grünenpütt, F. Scholz, et H. Blanck, « Improvement of Ohmic Contact for InAlGaN/AlN/GaN HEMTs with Recess Etching », *Physica Status Solidi (a)*, vol. 215, nº 8, p. 1700456, avr. 2018, doi: 10.1002/pssa.201700456.

[115] A. Basu, F. M. Mohammed, S. Guo, B. Peres, et I. Adesida, « Mo⁄Al⁄Mo⁄Au Ohmic contact scheme for AlxGa1−xN⁄GaN high electron mobility transistors annealed at 500 °C », *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing,*

Measurement, and Phenomena, vol. 24, nº 2, p. L16-L18, mars 2006, doi: 10.1116/1.2178365.

[116] H. G. Xing, D. Deen, Y. Cao, T. Zimmermann, P. Fay, et D. Jena, « MBE-Grown Ultra-shallow AlN/GaN HFET Technology », *ECS Trans.*, vol. 11, nº 5, p. 233-237, sept. 2007, doi: 10.1149/1.2783877.

[117] A. Malmros *et al.*, « Evaluation of an InAlN/AlN/GaN HEMT with Ta-based ohmic contacts and PECVD SiN passivation », *Phys. Status Solidi C*, vol. 11, nº 3-4, p. 924-927, févr. 2014, doi: 10.1002/pssc.201300320.

[118] T.-H. Jaing *et al.*, « Sinx-Assisted Tin Formation at Interface for Algan/Gan High Electron Mobility Transistors of High-Performance Ti/Al/Ni/Au Ohmic Contacts », 2023. doi: 10.2139/ssrn.4560651.

[119] J. Bergsten *et al.*, « Low resistive Au-free, Ta-based, recessed ohmic contacts to InAlN/AlN/GaN heterostructures », *Semicond. Sci. Technol.*, vol. 30, nº 10, p. 105034, oct. 2015, doi: 10.1088/0268-1242/30/10/105034.

[120] L. Wang, I. Adesida, A. M. Dabiran, A. M. Wowchak, et P. P. Chow, « Ti/Al/Mo/Au Ohmic contacts to all-binary AlN/GaN high electron mobility transistors », *Applied Physics Letters*, vol. 93, nº 3, p. 032109, juill. 2008, doi: 10.1063/1.2964204.

[121] J. Zhang *et al.*, « Ultralow-Contact-Resistance Au-Free Ohmic Contacts With Low Annealing Temperature on AlGaN/GaN Heterostructures », *IEEE Electron Device Lett.*, vol. 39, nº 6, p. 847-850, juin 2018, doi: 10.1109/LED.2018.2822659.

[122] D.-Y. Chen, A. R. Persson, V. Darakchieva, P. O. Å. Persson, J.-T. Chen, et N. Rorsman, « Structural investigation of ultra-low resistance deeply recessed sidewall ohmic contacts for AlGaN/GaN HEMTs based on Ti/Al/Ti-metallization », *Semicond. Sci. Technol.*, vol. 38, nº 10, p. 105006, oct. 2023, doi: 10.1088/1361-6641/acf396.

[123] D. A. Deen, D. F. Storm, D. S. Katzer, D. J. Meyer, et S. C. Binari, « Dependence of ohmic contact resistance on barrier thickness of AlN/GaN HEMT structures », *Solid-State Electronics*, vol. 54, nº 6, p. 613-615, juin 2010, doi: 10.1016/j.sse.2009.11.012.

[124] B. Jacobs, M. C. J. C. M. Kramer, E. J. Geluk, et F. Karouta, « Optimisation of the Ti/Al/Ni/Au ohmic contact on AlGaN/GaN FET structures », *Journal of Crystal Growth*, vol. 241, nº 1-2, p. 15-18, mai 2002, doi: 10.1016/S0022-0248(02)00920-X.

[125] N. Sarazin *et al.*, « AlInN/AlN/GaN HEMT Technology on SiC With 10-W/mm and 50% PAE at 10 GHz », *IEEE Electron Device Lett.*, vol. 31, nº 1, p. 11-13, janv. 2010, doi: 10.1109/LED.2009.2035145.

[126] J. Guo *et al.*, « MBE-Regrown Ohmics in InAlN HEMTs With a Regrowth Interface Resistance of 0.05 $\Omega\cdot\hbox{mm}$ », *IEEE Electron Device Lett.*, vol. 33, nº 4, p. 525-527, avr. 2012, doi: 10.1109/LED.2012.2186116.

[127] G. Meneghesso *et al.*, « Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives », *IEEE Trans. Device Mater. Relib.*, vol. 8, nº 2, p. 332-343, juin 2008, doi: 10.1109/TDMR.2008.923743.

[128] J. A. Del Alamo et J. Joh, « GaN HEMT reliability », *Microelectronics Reliability*, vol. 49, nº 9-11, p. 1200-1206, sept. 2009, doi: 10.1016/j.microrel.2009.07.003.

[129] M. Meneghini, A. Stocco, R. Silvestri, G. Meneghesso, et E. Zanoni, « Degradation of AlGaN/GaN high electron mobility transistors related to hot electrons », *Applied Physics Letters*, vol. 100, nº 23, p. 233508, juin 2012, doi: 10.1063/1.4723848.

[130] G. Meneghesso *et al.*, « Degradation of AlGaN/GaN HEMT devices: Role of reverse-bias and hot electron stress », *Microelectronic Engineering*, vol. 109, p. 257-261, sept. 2013, doi: 10.1016/j.mee.2013.03.017.

[131] Zhan. Gao *et al.*, « Short Term Reliability and Robustness of ultra-thin barrier, 110 nrn-gate AlN/GaN HEMTs », in *2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Singapore: IEEE, juill. 2020, p. 1-6. doi: 10.1109/IPFA49335.2020.9260793.

[132] R. Kabouche, K. Harrouche, E. Okada, et F. Medjdoub, « Short-term reliability of high performance Q-band AlN/GaN HEMTs », in *2020 IEEE International Reliability Physics Symposium (IRPS)*, Dallas, TX, USA: IEEE, avr. 2020, p. 1-6. doi: 10.1109/IRPS45951.2020.9129322.

[133] I. Khalil, E. Bahat-Treidel, F. Schnieder, et J. Wurfl, « Improving the Linearity of GaN HEMTs by Optimizing Epitaxial Structure », *IEEE Trans. Electron Devices*, vol. 56, nº 3, p. 361-364, mars 2009, doi: 10.1109/TED.2008.2011849.

[134] J. Vidkj, « Linearity Assessment of GaN Technology ».

[135] J. Kotani *et al.*, « Recent advancement of GaN HEMT with InAlGaN barrier layer and future prospects of A1N-based electron devices », in *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA: IEEE, déc. 2018, p. 30.4.1-30.4.4. doi: 10.1109/IEDM.2018.8614519.

[136] W. Liu *et al.*, « 6.2 W/Mm and Record 33.8% PAE at 94 GHz From N-Polar GaN Deep Recess MIS-HEMTs With ALD Ru Gates », *IEEE Microw. Wireless Compon. Lett.*, vol. 31, nº 6, p. 748-751, juin 2021, doi: 10.1109/LMWC.2021.3067228.

[137] B. Romanczyk *et al.*, « Evaluation of linearity at 30 GHz for N-polar GaN deep recess transistors with 10.3 W/mm of output power and 47.4% PAE », *Applied Physics Letters*, vol. 119, nº 7, p. 072105, août 2021, doi: 10.1063/5.0058587.

[138] H. Collins *et al.*, « N-Polar Deep Recess GaN HEMT With a TiN Schottky Gate Contact Demonstrating 53.4% PAE and 3.7 W/mm Associated P$_{\mathrm{out}}$ at 94 GHz », *IEEE Microw. Wireless Tech. Lett.*, p. 1-4, 2024, doi: 10.1109/LMWT.2024.3402558.

[139] R. S. Howell, B. Novak, T. Vasen, P. Shea, J. Chang, et S. Afroz, « GaN SLCFET Technology for Next Generation mmW Systems, Demonstrating P_{out} of 10.87 W/mm With 43% PAE at 94 GHz », *IEEE Microw. Wireless Tech. Lett.*, vol. 33, nº 6, p. 839-842, juin 2023, doi: 10.1109/LMWT.2023.3271862.

[140] J. Chang *et al.*, « The Super-Lattice Castellated Field-Effect Transistor: A High-Power, High-Performance RF Amplifier », *IEEE Electron Device Lett.*, vol. 40, nº 7, p. 1048-1051, juill. 2019, doi: 10.1109/LED.2019.2917285.

[141] J. S. Moon *et al.*, « High-speed graded-channel AlGaN/GaN HEMTs with power added efficiency >70% at 30 GHz », *Electron. lett.*, vol. 56, nº 13, p. 678-680, juin 2020, doi: 10.1049/el.2020.0281.

[142] J. Moon *et al.*, « Novel High-speed Linear GaN Technology with High Efficiency », in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA: IEEE, juin 2019, p. 1130-1132. doi: 10.1109/MWSYM.2019.8700832.

[143] J. Moon *et al.*, « Highly-Linear and Efficient mm-Wave GaN HEMT Technology », 2022.

[144] J.-S. Moon *et al.*, « Power Scaling of Graded-Channel GaN HEMTs With Mini-Field-Plate T-gate and 156 GHz f_T », *IEEE Electron Device Lett.*, vol. 42, nº 6, p. 796-799, juin 2021, doi: 10.1109/LED.2021.3075926.

[145] S. Krause, I. Streicher, P. Waltereit, L. Kirste, P. Brückner and S. Leone, "AlScN/GaN HEMTs Grown by Metal-Organic Chemical Vapor Deposition With 8.4 W/mm Output Power and 48 % Power-Added Efficiency at 30 GHz," in IEEE Electron Device Letters, vol. 44, no. 1, pp. 17-20, Jan. 2023, doi: 10.1109/LED.2022.3220877

[146] Yusuke Kumazaki et al 2024 Appl. Phys. Express 17 086504 DOI 10.35848/1882-0786/ad68c2

[147] F. Medjdoub et al., "Emerging GaN Technologies for Next-Generation Millimeter-Wave Applications," in IEEE Microwave Magazine, vol. 25, no. 10, pp. 18-37, Oct. 2024, doi: 10.1109/MMM.2024.3428188

Chapter 2: Graded AlGaN channel HEMT – A simulation study

I. Introduction

I.1. Context of the study

GaN technology is seen as a disruptive technology for space applications due to its superior performances. For RF applications, the benefit for space is tremendous as solid-state GaN transistors (SSPAs) allow replacement of bulky TWT amplifiers for high output power applications ranging from P to Ka-band (12 - 30GHz). However, RF industrial GaN HEMTs are currently qualified only up 30 GHz using a gate length down to 150 nm. Future Telecommunication and Earth Observation applications will require high performance GaN based SSPAs to also be available in Q, V and W-band frequencies.

As presented previously, several GaN device architectures have achieved outstanding performance up to W-band. However, proven reliability under harsh conditions still limits their use in space applications. Moreover, for mobile wireless, satcom and radar applications, device linearity (i.e., the device's ability to handle large signals without intermodulation distortion) is critical. Current GaN devices deployed in wireless base stations make extensive use of digital predistortion techniques to achieve sufficient linearity, but this is very computationally intensive (thereby power consuming) and therefore does not scale well with the increasing data rates and bandwidths of 5G and beyond. A transistor with excellent initial linearity is highly advantageous for space applications as it reduces the need for predistortion equipment.

In this frame, the European Space Agency (ESA), launched several research programs to evaluate and study promising technologies that can offer both high performance and linearity. These programs aim to implement and optimize Technology Computer-Aided Design (TCAD) simulations for a better understanding of device physics and to guide technological choices before starting the fabrication process. The objective of this study was to support ESA in its choices towards the most suitable GaN technologies to be investigated for future space applications. Principal target is to design a technology that could combine high P_{OUT}, PAE and linearity in the millimeter-wave range while fulfilling the space reliability requirements.

Among all the existing technologies, the graded AlGaN channel HEMT was chosen because of its unique combination of high performance and superior linearity. However, this technology is currently developed by HRL in USA. A simulation workflow has been established, covering both the device and the circuit level to investigate this device configuration system. The challenge was to reproduce as close as possible the behavior of the graded AlGaN channel not only the DC and small signal performances but also the large signal and linearity characteristics; the aim being to compare with conventional AlGaN/GaN HEMTs in order to highlight its benefits and further understanding the device physics.

I.2. Source of non-linearity and improvement methods

The non-linearity of power amplifiers is generally defined by intermodulation distortion (IMD). It can be pointed out that the intermodulation distortion products are generated at different frequencies when a two-tone test is applied to a non-linear device. While second order terms and harmonics are easy to filter, third-order intermodulation (IMD_3) products occurring at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ close to the fundamental frequency (carrier) are difficult to filter which cause in-band interference (IM3) in the receiver **(Figure 2.1)**.

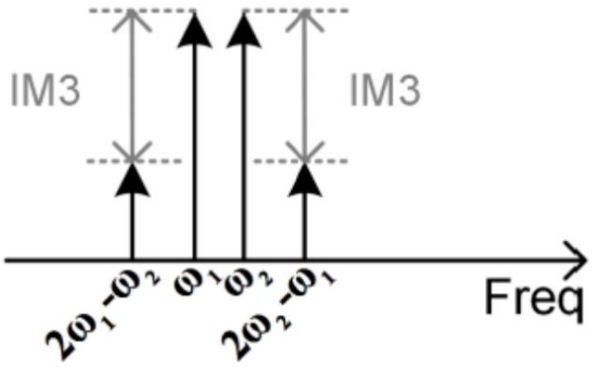


Figure 2.1. Third-order intermodulation distortion

The main cause of nonlinearity in GaN HEMT at high frequencies comes from the transconductance (G_M), the output conductance (g_{DS}), the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}) [1, 2]. However, the main concern remains the sharp drop in G_M after reaching its peak at open channel [2, 3]. This phenomenon is mainly due to the reduced electron velocity from hot phonon scattering at high carrier density [4, 5] and the increased in non-linear source and drain resistance [6, 7].

Self-heating and trapping effects are also responsible of G_M roll-off and are not negligeable [8, 9]. Since several years, few designs have been proposed to improve the G_M flatness such as nanowire channel HEMTs [10] or Buried Dual Gates Field Effect Transistors (BRIDGE FETs) [11]. The concept of these technologies is to bury dual gates in HEMT structure to form lateral Schottky contacts with the 2DEG. The drain current is then controlled solely by modulating the width of the 2DEG while maintaining the sheet electron density constant, which results in a much flatter transconductance. FinFET architectures can also improve G_M flatness by connecting several FETs in parallel, leading to a 3D structure that allows better control of the charge carriers from the channel [12, 13]. Nevertheless, these technologies have weaknesses. Their designs are complex to build and involve additional gate metal, which generates increased external parasitic capacitances affecting the small signal performances. Thus, in this case, there is a strong trade-off between improving the device linearity and degrading the RF performances.

Another way to improve the G_M flatness without reducing the device performance is to optimize the epitaxy design. Conventional GaN channel can be replaced by graded AlGaN channel structures. Since AlGaN has polarization properties, a linear gradient of Al composition in the AlGaN layer allows carriers to propagate in the channel rather than being confined at the interface of the heterostructure. This concept is not recent and has been used to develop polarization-graded FETs (PolFETs). In this configuration, the channel is graded from GaN to AlGaN, allowing a new electron distribution along the gradient, which generates a three-dimensional electron gas (3DEG) [14-19]. In this way, at open channel, the depletion width will decrease but the volumetric charge density is unchanged. Therefore, the electron saturation velocity remains stable, and the G_M flatness improved.

The graded channel HEMT concept is notably used by HRL. This technology will be studied in detail by simulation and presented in the following sections. It can be pointed out that we had to build up a workflow from scratch in this frame, learn how to use multiple software considering the advantages and limitations of the different models. This was a difficult and time-consuming process, but essential to mimicking the device characteristics as good as possible.

II. Methodology and models

II.1. Overview of the simulation workflow

The purpose is to compare simulation results with experimental data (large signal and linearity) in order to validate the proposed methodology. The final objective is to provide some physical insights on the architecture of the graded AlGaN channel HEMT and to compare with conventional AlGaN/GaN HEMTs. The simulation workflow involves three levels: device-level simulation **(Level 1)**, compact modeling **(Level 2)**, and circuit-level simulation **(Level 3)**. A short note on the three levels is given below **(Figure 2.2)**.

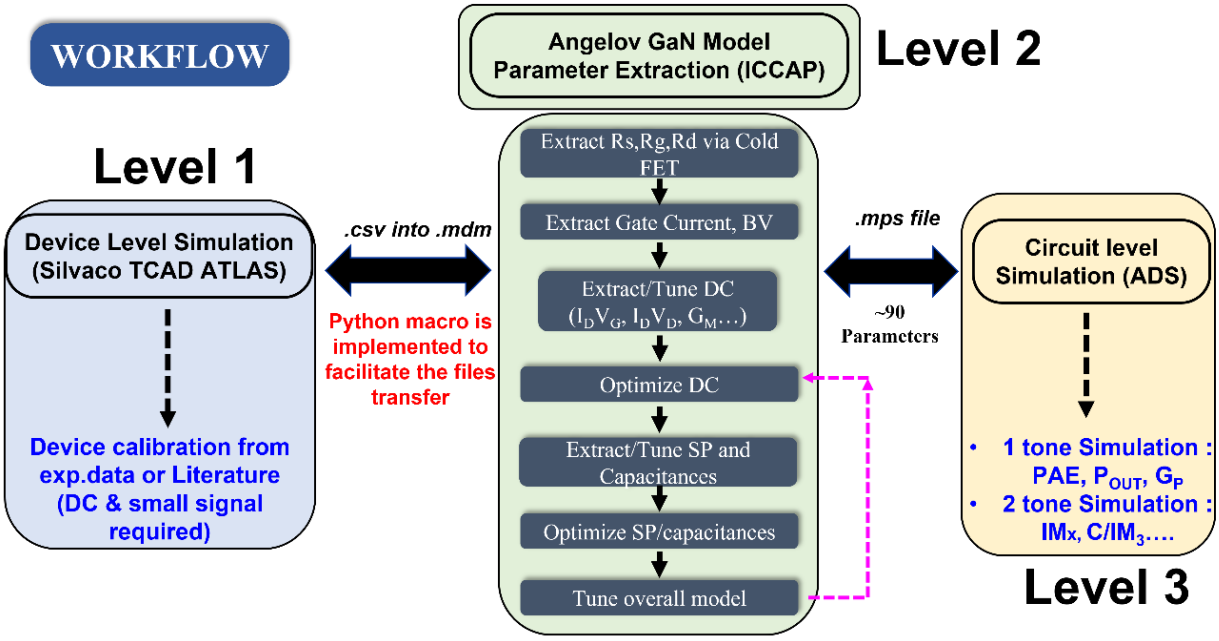


Figure 2.2. The flowchart showing three different levels involved in the simulation workflow.

Level 1 is a device-level TCAD simulation performed using SILVACO ATLAS 2D simulator. It involves the design of vertical structure, especially the epitaxial layers composition and thicknesses, followed by transistor design such as geometry, source and drain terminals (ohmic contacts), gate length and its position between source and drain. The user can also define different trapping or thermal models to study specific effects or phenomena that occur in a device. However, including too many models simultaneously often results in excessive simulation time, and above all severe convergence issues. For our current simulations, we have included both thermal and trapping effects.

Moreover, at the barrier/channel interface, the 2DEG can be simulated via physics-based models. The 2DEG properties, such as electron mobility (μ), carrier concentration (N_s), and saturation velocity (v_{sat}), could be either defined or generated via in-built physical models. Calibration of D.C and R.F characteristics against the experimental results is necessary. To validate the calibration of simulated device, the most critical parameters such as transconductance (G_M), cut-off frequency (F_t) and maximum oscillation frequency (F_{max}), are compared to the respective experimental values. All data exported by ATLAS are in .cvs format.

Level 2 involves generation of a compact and non-linear transistor model for TCAD SILVACO data. The extraction of compact model parameters is performed using the commercially available software ICCAP 2022 (Keysight Technologies). To generate large signal and linearity performances, it is necessary to inject a model at the circuit level. Level 2 acts as a platform between level 1 and level 3 to incorporate the transistor parameters generated in SILVACO into a physical model, which is then injected into level 3. For that, the Angelov model, a well-established mathematical model dedicated to GaN HEMTs was chosen. The model allows assessing the performances at high frequencies, typically up to 20 GHz or beyond. The model parameter extraction includes several steps and requires multiple iterations. The main challenge here is to fit as accurately as possible SILVACO data with the Angelov model. After satisfactory fitting, the model parameters are exported as *".mps"* file which can be readable by the circuit-level simulator ADS (level 3).

Level 3 is a circuit-level simulation using Advanced System Design (ADS, Keysight Technologies). The compact non-linear model from ICCAP is imported as a custom- made GaN HEMT, acting as the device under test (DUT) for harmonic balance simulations to predict large signal and linearity characteristics at the frequency of interest.

Data Management: The output from level 1 simulation delivers a significant amount of data files, therefore, a good data management is essential. Data transfer from SILVACO ATLAS (level 1) to ICCAP (level 2) is not a common practice, because no commercial built-in tool is available to transfer data file types from *".csv"* to *".mdm*". Manual transfer of files would be time-consuming and may lead to human errors. Hence, a macro (open-source python code) has been developed to accurately transfer the data files.

II.2. Choice of the model

As listed in **Table 2.1**, different types of transistor models such as physics-, virtual source-, empirical, or artificial neural network (ANN)-based models are available [20]. Usually, physics-based models such as ASM-HEMT require detailed information about the transistor and include a large number of parameters that can be difficult to manage. However, impressive results have recently been reported, particularly for modeling large signal characteristics at high-frequency (>10 GHz) [21-23]. ANN-based models do not provide direct physical insights and requires a significant amount of high-quality data to train the neurons.

Table 2.1. A survey of models available for GaN HEMTs.

Model	Year	Model Type	Max. Freq.	Notes
Curtice (RCA Labs)	1980	Empirical	20 GHz (LS)	Developed for GaAs FET, not suitable for GaN
Dambrine-Cappy (Lille Univ)	1988	Empirical	5 GHz (SS)	Not suitable for large signal and high frequencies
EE-HEMT (Keysight)	1998	Empirical	10 GHz (LS)	May not accurate at higher frequencies
Angelov GaN (Chalmers Univ)	2008	Empirical	20-30 GHz (LS)	May not accurate at higher frequencies
MVSG (MIT)	2013	Physics-based	<10 GHz (LS)	Technology-dependent
DynaFET (Keysight)	2014	Artificial Neural Network (ANN) based	<10 GHz (LS)	A black-box behavioral model, needs more data to train ANN
ASM-HEMT (Berkeley,IIT-K)	2015	Virtual source	10-30-94* GHz (LS)	Technology-dependent

*Only 1 publication reported to date at 94 GHz [19]

Empirical models such as Curtice, EE-HEMT or Angelov model are widely used for modeling transistors and are established in the industry for over 10 years [24]. The Angelov model, also known as the Chalmers model, is a well-known empirical model developed by *Iltcho Angelov* at Chalmers University. Originally designed for GaAs MESFETS and HEMTs [25], it has been substantially improved [26, 27] and extended for GaN HEMTs [28]. However, the Angelov model is non-speculative since it is not physics based and suffer to provide physical insights. The model scalability is also not trivial, especially at high frequency and large bias operation. Any change in process or device geometry requires re-adjustments of the model, which is time-consuming for users. Nevertheless, the model is reasonably easy to use and allows to study large signal and linearity characteristics up to 20-30 GHz.

In fact, it offers a good balance between the amount of prior information and the number of parameters required to build it. A toolkit is also directly available in ICCAP software for extracting and optimizing the model parameters.

II.3. Choice of HRL reference devices for design the structure in TCAD

J.S. Moon et al., have reported several papers on the performance of their graded AlGaN channel HEMTs [29-35]. Unfortunately, all structural details required for reverse engineering has not been reported in a single publication. Moreover, it is difficult to find one paper reporting general view of DC, small signal, large signal and linearity characteristics all together. Therefore, to replicate the HRL results, we decided to combine two articles that report approximately the same performance while providing enough structural details to build the graded AlGaN channel HEMT in ATLAS SILVACO [34, 35]. **Table 2.2** summarized the main information available on these two papers.

Table 2.2. Summary of GC technology detail derived from [34, 35]

REF	Structure (Epi-layers composition & Thickness)	Available characteristics/data								
		L_G (nm)	V_{TH} (V)	G_M (mS/mm) @V_{DS} = 5V	G_M Curve	$I_{D\ MAX}$ (A/mm) V_{GS} = 0 V V_{DS} = 5 V	F_T/F_{MAX} (GHz)	Loadpull @V_{DS} = 14 V 30 GHz	Linearity @V_{DS} = 14 V 30 GHz	Device width
[34]	No	50	-2.9	520	Yes	1.0	Not reported	Gain = 14 dB PAE = 65% P_{OUT} = 3 W/mm	C/IM3 = -17dBc and -30 dBc at 6 dB output power back-off	2*37.5 µm
[35]	Yes	60	-3.3	540	No	1.0	156/300	Gain = 15 dB PAE = 61% P_{OUT} = 3.4 W/mm	Not reported	2*37.5 µm

III. Workflow validation and model calibrations

III.1. ATLAS SILVACO simulation (level 1)

ATLAS is one of many products developed by SILVACO international. The software is a physical based simulator which predict the electrical characteristics of semiconductor devices through a designed structure and at specified bias conditions. ATLAS has been popular since many years, helping industry and academic research to investigate and visualize physical phenomena that are difficult or impossible to measure. It is then possible to obtain trends in the behavior of electrical devices, thus orienting industrial choices but also reducing the number of experiments and therefore R&D costs.

In this frame, GaN HEMTs can be represented on a two-dimensional grid with meshing parameters. At every mesh intersection, the program simulates carrier transport by means of differential equations derived from Maxwell's laws, Poisson's equations, continuity and drift-diffusion transport equations [36]. To enhance accuracy, the program incorporates the appropriate physics via numerical procedures. ATLAS attempts to find solutions to carrier parameters such as current through electrodes, electron concentrations, and electric fields throughout the device. ATLAS sets up the equations with an initial guess for parameter values then iterates through parameters to resolve discrepancies. It can alternatively use a decoupled (GUMMEL) or coupled (NEWTON) approach to achieve an acceptable correspondence of values. When convergence on acceptable values does not occur, the program automatically reduces the iteration step size. ATLAS generates the initial guess for parameter values by solving a zero-bias condition in the device. Finally, the simulator is a controlled tool that needs instructions in a specific order to correctly simulate a component. There are five groups of instructions, which must be given in order to avoid errors or incorrect results **(Figure 2.3)**.

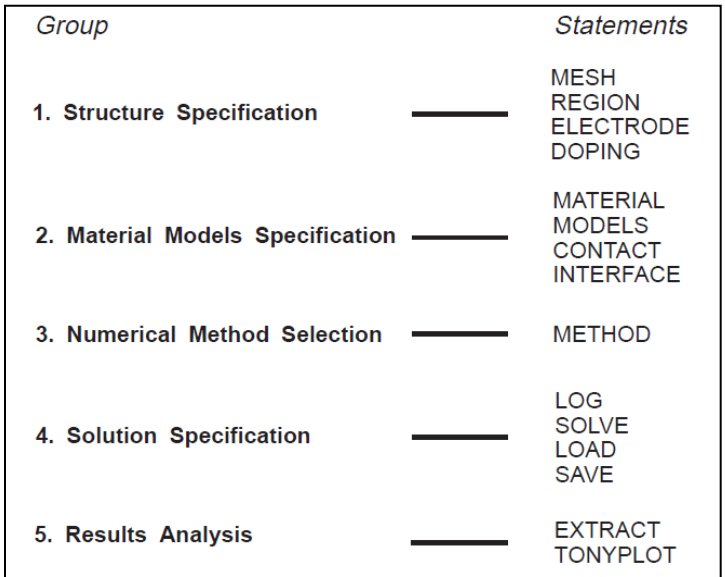


Figure 2.3. Structure design in ATLAS [36].

III.1.a. Inputs for calibration and structure design

- Epitaxial stack:

Figure 2.4.a shows the AlGaN/GaN graded channel HEMT as provided in the HRL publication [35] and its structure replicated in ATLAS. In SILVACO, each layer from the epitaxial stack is described as a region with its material properties. As shown in **Figure 2.4.b**, only the active regions are modelled, the SiC substrate/nucleation layer are excluded. The active regions consist in 1µm $Al_{0.04}GaN$ buffer, 20nm thick GaN channel layer, 6nm thick linearly graded AlGaN channel layer with an Al composition ranging from 0% to 10%, as reported in [30]. The barrier layer is 15 nm thick $Al_{0.25}GaN$ with a SiN cap. The n^+ regrown GaN regions are used and place underneath the source and drain electrodes with a doping concentration of $4\times10^{20}/cm^3$ to achieved low contact resistances. **Figure 2.4.c** shows another view of the structure along an y-cutline from the gate to the buffer layer showing the aluminum composition of the layers, especially the linear profile of the graded AlGaN channel.

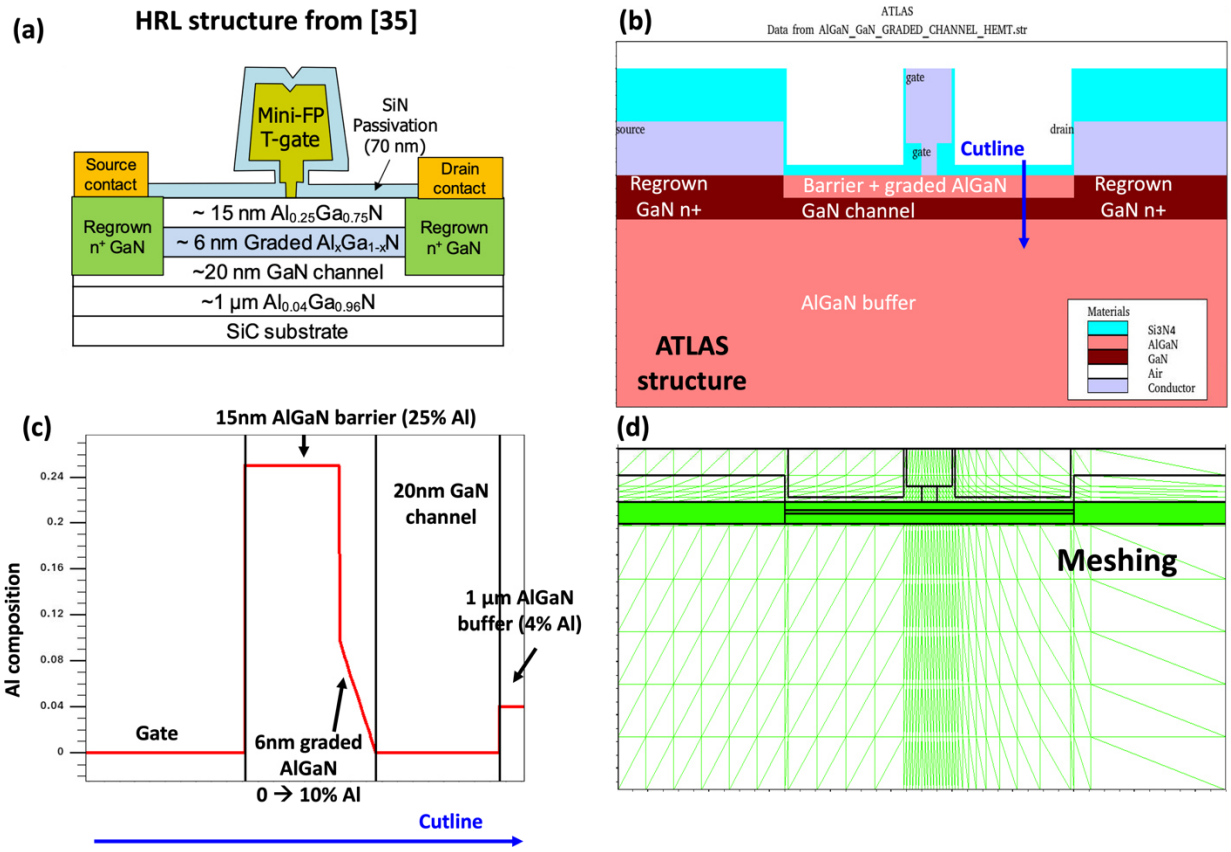


Figure 2.4. (a) Graded AlGaN channel from HRL, (b) corresponding structure designed in ATLAS, (c) y-cutline under the gate to the buffer layer showing Al-profiles for different layers and (d) meshing used in simulations.

- Meshing:

For numerical finite 2D modeling, the mesh of the regions must be specified in x and y directions. The result can be highly dependent on the meshing. Generally, mesh spacing is denser in active regions such as the channel (2DEG) and below the gate, while it is coarse in other regions. We used a minimum mesh spacing of 0.001 μm in active regions and 0.1 μm in non-critical regions. Although a denser meshing leads to more accurate results, it also increases simulation times considerably. A poorly defined mesh led to convergence issues and affect the calibration results. **Figure 2.4.d** presents the meshing used for the graded AlGaN channel HEMT.

- Material properties:

By default, ATLAS [36] considers AlGaN layer as a Wurtzite material, which is characterized by two components namely, spontaneous and piezoelectric polarization. Using the build-in polarization model, the AlGaN barrier region automatically sets the positive charge at the bottom and the negative charge at the top. The strain in the region is calculated from the lattice mismatch with the adjacent regions using the *"calc.strain"* statement. Using the statement *"polar.scale",* the magnitude of the total charge can be defined to achieve a carrier concentration (N_S) in the range of 9.0-9.5×10^{12}/cm^2 in the 2DEG, as desired for HRL's device. The 2DEG mobility (μ) was set to 1500 cm^2/Vs. For the AlGaN graded channel, a linear Al grading profile is defined by fixing the boundaries of the composition from 0% to 10%.

- Electrodes:

As seen in **Figure 2.4.b**, all three electrodes source, gate and drain are represented as a conductor (purple color). However, source and drain electrodes are defined as ohmic contacts, whereas the gate electrode as a Schottky contact, defined by its work function of 5.25 eV, typical value for Ni/Au. The gate resistance was fixed to 300 Ω.μm according to the information available in [35]. For the source and drain contacts, it is possible to specify external resistances (in Ω.μm) at the contact terminals. We used source and drain resistances of 160 Ω.μm and 280 Ω.μm, respectively. It is worthy to mention that we simulate a single finger gate of 50 nm length, which is then numerically normalized, equivalent to multiple fingers i.e., 2×37.5 μm. The gate length was fixed to 50 nm and positioned at equidistance 0.5 μm between the source and drain contacts.

- Physical Models:

We used the default model from ATLAS with the values for peak electron velocity and electron mobility adjusted for AlGaN/GaN structures. The models specified are the following: Shockley-Read-Hall recombination with fixed carrier lifetimes (SRH), Fermi-Dirac (FERMI) statistics and a parallel field mobility (FLDMOB) model. For fixing the electron mobility, we have used a composition and temperature dependent low field model (Farahmand Modified Caughey Thomas - FMCT), especially developed for nitride materials [36-38].

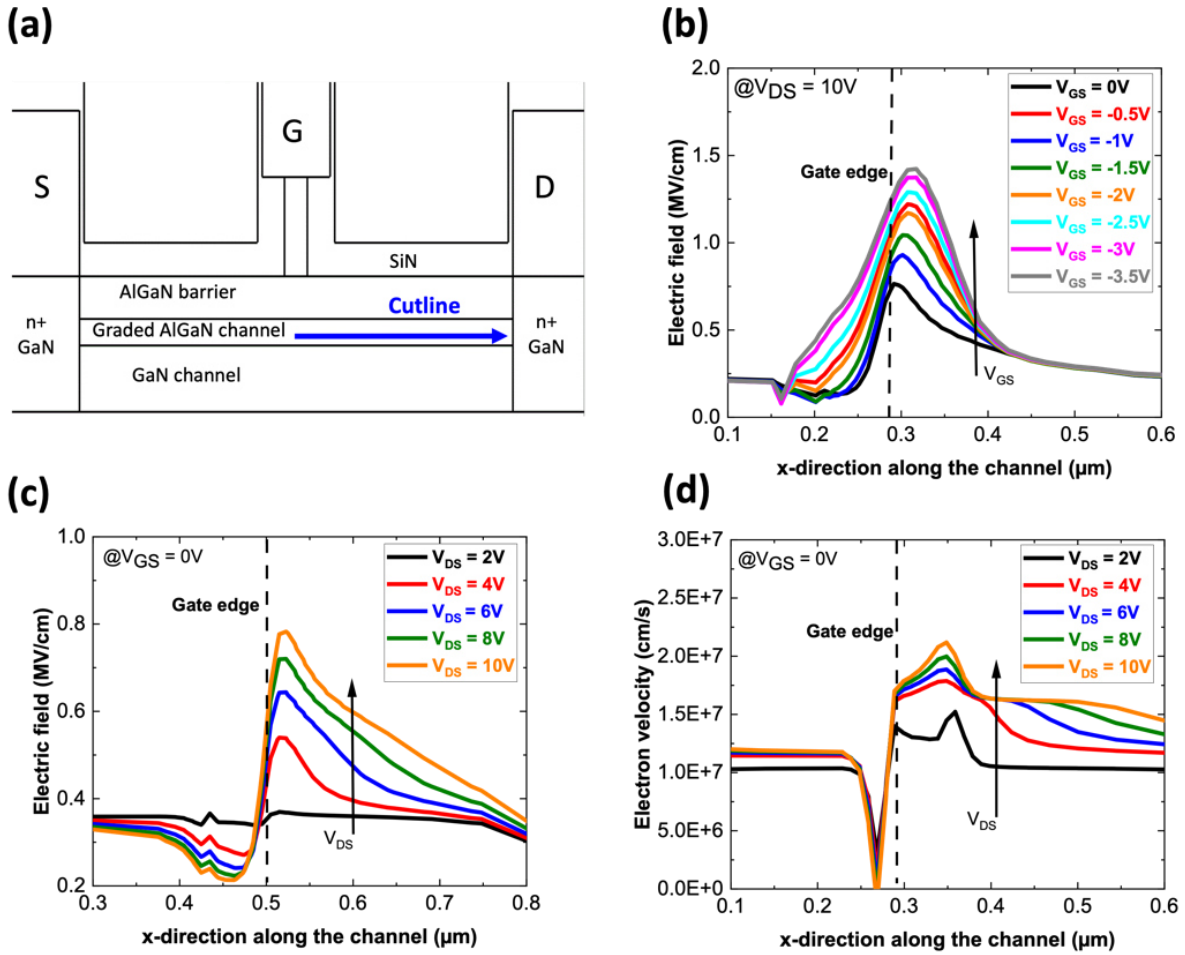


Figure 2.5. (a) Cutline along the graded AlGaN channel HEMT showing the electric field (b, c) and the electron velocity (d) for different bias conditions.

To ensure that the model and the generated structure align with physical ranges for AlGaN/GaN HEMT, electric field and electron velocity at different bias conditions were extracted. **Figure 2.5** shows snapshots from TCAD simulation corresponding to the electric field and the channel velocity.

These snapshots are taken along a cutline from the gate to the drain edge below the gate through the channel **(Figure 2.5.a)**. As expected, in open channel conditions, the electric field increases with V_{DS}, with a peak located under the gate edge **(Figure 2.6.c)**. Similarly, the electron velocity tends to saturate at high voltage **(Figure 2.5.d)**. Finally, at V_{DS} constant, the electric field along the channel increases as we switch from ON to OFF state **(Figure 2.5.b)**.

III.1.b. DC and RF small signal characteristics

Figure 2.6.a shows the transconductance (G_M) and transfer (I_DV_G) characteristics of the structure shown in **Figure 2.4**. Threshold voltage (V_{TH}), maximum linear G_M and the maximum current of the simulated device are very close to the HRL's device. Such characteristics verifies that the TCAD model developed in this study provides a close approximation of the experimental device [34]. For RF small signal characteristics, S-parameter simulations were performed in the frequency range of 1 GHz – 150 GHz in the same condition than HRL, i.e., V_{DS} = 5V at peak G_M bias. The simulated F_T/F_{MAX} are 165/290 GHz in agreement with HRL's data of 156/308 GHz [35] (**Figure 2.6.b**). The simulated maximum stable/available gain (MSG/MAG) at 30GHz are also very close to the experimental data with a value of 14.9 dB against 13.8 dB, respectively. **Table 2.3** summarizes the simulated results their comparison with HRL's experimental data.

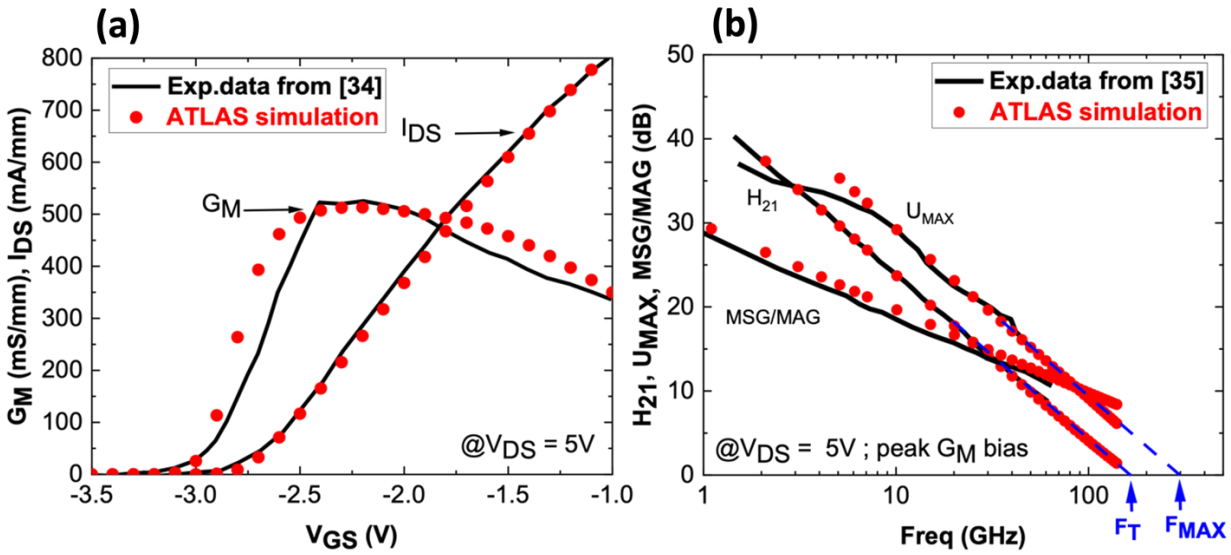


Figure 2.6. (a) Simulated DC and (b) RF small signal characteristics obtained with ATLAS SILVACO versus HRL's experimental data.

Table 2.3. Summary of simulated characteristics vs HRL's experimental data.

DATA	I_{DMAX} at V_{GS} = 0V (A/mm)	$G_{M\ MAX}$ (mS/mm)	Linear G_M	F_T/F_{MAX} (GHz)	MSG/MGA (dB)
TCAD	1.05	513	Yes	165/290	14.9
HRL exp.data	1.02 [34]	520 [34]	Yes [34]	156/308 [35]	13.8 [34]

III.2. Angelov GaN HEMT modelling with ICCAP (level 2)

The Angelov model is an empirical model based on measured experimental data and mathematical formulations based on equivalent circuit. The model was developed by focusing on the non-linear fit of the drain current and its derivatives. The central equations include those describing the drain current (I_{DS}), the gate current (I_{GS}) and non-linear capacitors (C_{GS}, C_{GD}, C_{DS}). The theory and mathematical expressions including the current equations, charge, and capacitance expressions are documented and can be found elsewhere [39, 40]. Recently, the Angelov model has been greatly improved and extended to include most of the specific GaN device related effects such as gate-leakage current, self-heating, DC to RF dispersion. For our simulations, trapping and thermal effects are not included as they are not simulated at the device level. It is also possible to modify the Angelov model directly by adding or simplifying parameters of the model to improve fitting between data [41-44].

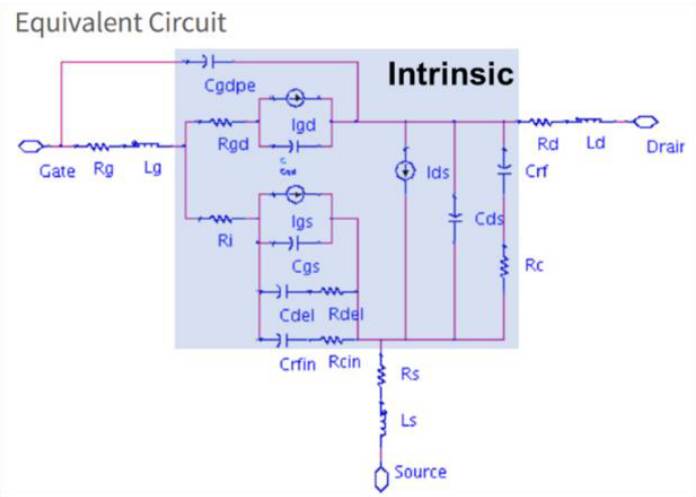


Figure 2.7. Large signal equivalent circuit of Angelov GaN model [45].

In our case, no changes were made to the model, we used it as available in ICCAP software. **Figure 2.7** shows the standard large signal equivalent circuit of Angelov GaN model. Typically, the extraction of model parameters is carried out with respect to D.C. and small signal RF measurements. After satisfactory overall fitting, the model can be used to simulate large signal and linearity performances at the circuit level in ADS. In this case, TCAD data from ATLAS have been used and directly implemented into the ICCAP model. To do this, we fed the Angelov model with a large amount of DC and RF small signal data from TCAD at different V_{DS} and V_{GS} polarizations.

III.2.a. Model parameters

Table 2.4 is a list of modes and parameters used in the Angelov GaN model [39, 45]**.** For proper operation of the model, the modes should be specified. For instance, self-heating is active only when SELFT mode = 1. For IDS current model, mode 0 corresponds to original, and 1 is a symmetric model. Similarly, for the capacitance model, mode 0 is linear, 1 is a bias-dependent capacitance, and 2 is a charge-based capacitance. In general, the bias-dependent capacitor models are known to be less robust, which leads to convergence issues. Charge-based models are normally more robust. In this work, the following model flags have been used: IDSMOD=1, IGMOD=1 and CAPMOD=2, NOIMOD=0, and SELFT=1. The Angelov GaN model consists of 87 parameters in total, which can be categorized into sub-groups as highlighted in the **Table 2.4**.

Table 2.4. Parameters of Angelov GaN model

	Parameter	**Explanation**	**Units**	**Nominal Default**
	Model modes			
	IDSMOD	Ids Current model mode (0-1) *0– original , 1- Symmetric*	None	0
	IGMOD	Gate diode model mode (0-1) *0-Igd/Igs model OFF; 1-Igd/Igs model ON*	None	0
	CAPMOD	Capacitance model mode (0-2) *0-linear ;1-bias dependent capacitance ;2- charge-based*	None	2
	NOIMOD	Noise model mode (0-1) *0 – Noise model OFF; 1- Noise mode ON*	None	1
	SELFT	Self-heating mode (0-1) *0 – self-heating OFF; 1 – self-heating ON*	None	0
	Current Ids parameters			
1	IPK0	Current for maximum transconductance Ipk	A	0.05
2	VPKS	Gate voltage Vpk for maximum Gm	V	-0.2

3	DVPKS	Delta gate voltage at peak Gm	V	0.2
4	P1	Polynomial coefficient P1 for channel current	V^{-1}	0.8
5	P2	Polynomial coefficient P2 for channel current	V^{-2}	0
6	P3	Polynomial coefficient P3 for channel current	V^{-3}	0
7	ALPHAR	Saturation parameter alpha r for knee region	V^{-1}	0.1
8	ALPHAR	Saturation parameter alpha s for saturation region	V^{-1}	1
9	VKN	Knee Voltage	V	4
10	LAMBDA	Channel length modulation parameter	None	0.001
11	LAMBDA1	Channel length modulation parameter	None	0
12	LVG	Coefficient for channel length modulation parameter	None	0
13	B1	Unsaturated coefficient B1 for P1	None	0.1
14	B2	Saturated coefficient B2 for P1	V^{-1}	4
	Breakdown Parameters			
15	LSB0	Soft breakdown model parameter	None	0
16	VTR	Soft breakdown model parameter	V	50
17	VSB2	Surface breakdown model parameter	V	0
18	EBD	Surface breakdown model parameter	V^{-1}	0.2
19	KBDGATE	Gate breakdown parameter	V	1
20	VBDGS	Gate Source breakdown voltage	V	10
21	VBDGD	Gate Drain breakdown voltage	V	100
22	PBDG	Gate breakdown exponent	V^{-1}	0.5
	Capacitance parameters			
23	CDS	Zero-bias drain-source junction capacitance	F	0
24	CGSPI	Gate-Source pinch-off capacitance	F	0
25	CGS0	Gate-Source capacitance parameter	F	0
26	CGDPI	Gate-Drain pinch-off capacitance	F	0
27	CGDPE	External Gate-Drain capacitance	F	0
28	CGD0	Gate-Drain capacitance parameter	F	0
29	P10	Polynomial coefficients for capacitances	None	0
30	P11			1
31	P20			0
32	P21			0.2
33	P30			0
34	P31			0.2
35	P40			0
36	P41			1
37	P111			0
38	P222			0
39	M	Coefficient for capacitance		0.5
40	IJ	Gate forward saturation current	A	0.00005
41	PG	Gate current parameter	None	15
42	NE	Gate p-n emission coefficient		1
43	VJG	Gate current parameter	V	0.7
44	RG	Gate ohmic resistane	ohm	1.05
45	RD	Drain ohmic resistance	ohm	1.05
46	RD2	Variable drain ohmic resistance	ohm	0
47	RI	Input resistance	ohm	1.05

48	RS	Source ohmic resistance	ohm	1.05
49	RGD	Gate resistance	ohm	1.05
50	LD	Drain ohmic inductance	H	0
51	LS	Source ohmic inductance	H	0
52	LG	Gate ohmic inductance	H	0
53	Tau	Device delay	s	0
	Frequency Dispersion Model parameters			
54	RCMIN	Minimum value of Rc	ohm	1000
55	RC	Resistance for frequency dependent output conductance	ohm	10000
56	CRF	Capacitance for frequency dependent output conductance	F	0
57	RCIN	Resistance for frequency dependent input conductance	ohm	100000
58	CRFIN	Capacitance for frequency dependent output conductance	F	0
59	RDEL	Resistance for frequency dependent input conductance	ohm	1000
60	CDEL	Capacitance for frequency dependent output conductance	F	0
61	KBGATE	Polynomial coefficient for frequency dependent input conductance	V^{-1}	0
	Self-Heating Model Parameters			
62	RTHERM	Thermal resistance	$K.W^{-1}$	10.001
63	CTHERM	Thermal capacitance	$Ws.K^{-1}$	0.0001
64	TCIPKO	Linear temperature coefficient for Ipk	K^{-1}	-0.002
65	TCP1	Linear temperature coefficient for P1	K^{-1}	-0.002
66	TCCGS0	Linear temperature coefficient for CGS0	K^{-1}	0.002
67	TCCGD0	Linear temperature coefficient for CGD0	K^{-1}	0.002
68	TCLSB0	Linear temperature coefficient for LSB0	K^{-1}	0
69	TCRC	Linear temperature coefficient for RC	K^{-1}	0
70	TCCRF	Linear temperature coefficient for CRF	K^{-1}	0
71	TCRS	Linear temperature coefficient for RS	K^{-1}	0.003
	Noise Model Parameters			
72	NOISER	Gate noise coefficient	None	0.5
73	NOISEP	Gate noise coefficient	None	0.5
74	NOISEC	Gate-drain noise coefficient	None	1
75	FNC	Noise corner frequency	Hz	0
76	KF	Flicker noise coefficient	None	0
77	AF	Flicker noise exponent	None	1
78	FFE	Flicker noise parameter	None	1
79	TG	Equivalent Temperature at Gate	°C	25
80	TD	Equivalent Temperature at Drain	°C	25
81	TD1	Variable Equivalent Temperature at Drain	°C	0.1
82	TMN	Noise fitting coefficient	None	1
83	KLF	Flicker noise exponent	None	1E14
84	FGR	Gate resistance frequency corner	Hz	60 k
85	NP	Flicker noise frequency exponent	None	0.3
86	LW	Effective gate noise width	mm	0.1
87	TNOM	Parameter for measurement Temperature	°C	25

III.2.b. Parameter extraction and data fitting

In this section, the major steps involved in the model parameter extraction and fitting are detailed. However, the entire data extraction, fitting procedure and how to use the ICCAP software can be found in the Keysight documentation [46-48].

1. **Cold FET**: The resistances (R_S, R_G, R_D) and inductances (L_S, L_G, L_D) were extracted from the real and imaginary parts of the Z-parameters transformed from S parameters of the TCAD simulated data. We have not implemented a specific value for inductances in TCAD (only resistances). So, it is found that the inductance is in the range of 1 pH (from the cold FET extraction). These values are used as starting points, which are further tuned during the fitting process. Typically, the bias conditions for Cold FET are: I_{GS} = 0.002 A and I_{DS} = -0.001 A. In this way, convergence problems in ATLAS were avoided.

2. **DC I_DV_G**: Extracting the drain current (I_{DS}) from the model is one of most important part to build the ultimate large signal model. As transconductance (G_M) fitting is undertaken, which is key for the linearity performances. The drain current is simulated in a wide range of biases sweeping both V_{GS} and V_{DS}. We simulated I_DV_G curves for at least 12 drain voltages: 4V to 15V with a step of 1V in the V_{GS} window of -4V (off-state) to 0V (fully open channel). It is important to feed the model with a wide range of values to ensure consistency. However, this makes it significantly more challenging to achieve a good fit systematically across the entire range. The parameters extracted using I_DV_G curves are IPK0, VPKS, DVPKS, P1, P2 and P3. In fact, the polynomial P1 is a ratio of transconductance (G_M) to the drain current (I_{DS}) at V_{GS} where G_M is maximum**.** Using *"Levenberg-Marquardt"* algorithm, the % absolute error is minimized and linear regression coefficient R^2 is maximized.

3. **DC I_DV_D:** The remaining current (I_{DS}) parameters are extracted from I_DV_D curves. For this, we simulated at least 9 I_DV_D curves for gate voltage V_{GS} ranging from -4.0 V to 0 V with a step of 0.5 V. Two regions can be identified: the knee region and the saturation region. It is important to evaluate the device fitting along a typical load-line, as we will discuss in the next section.

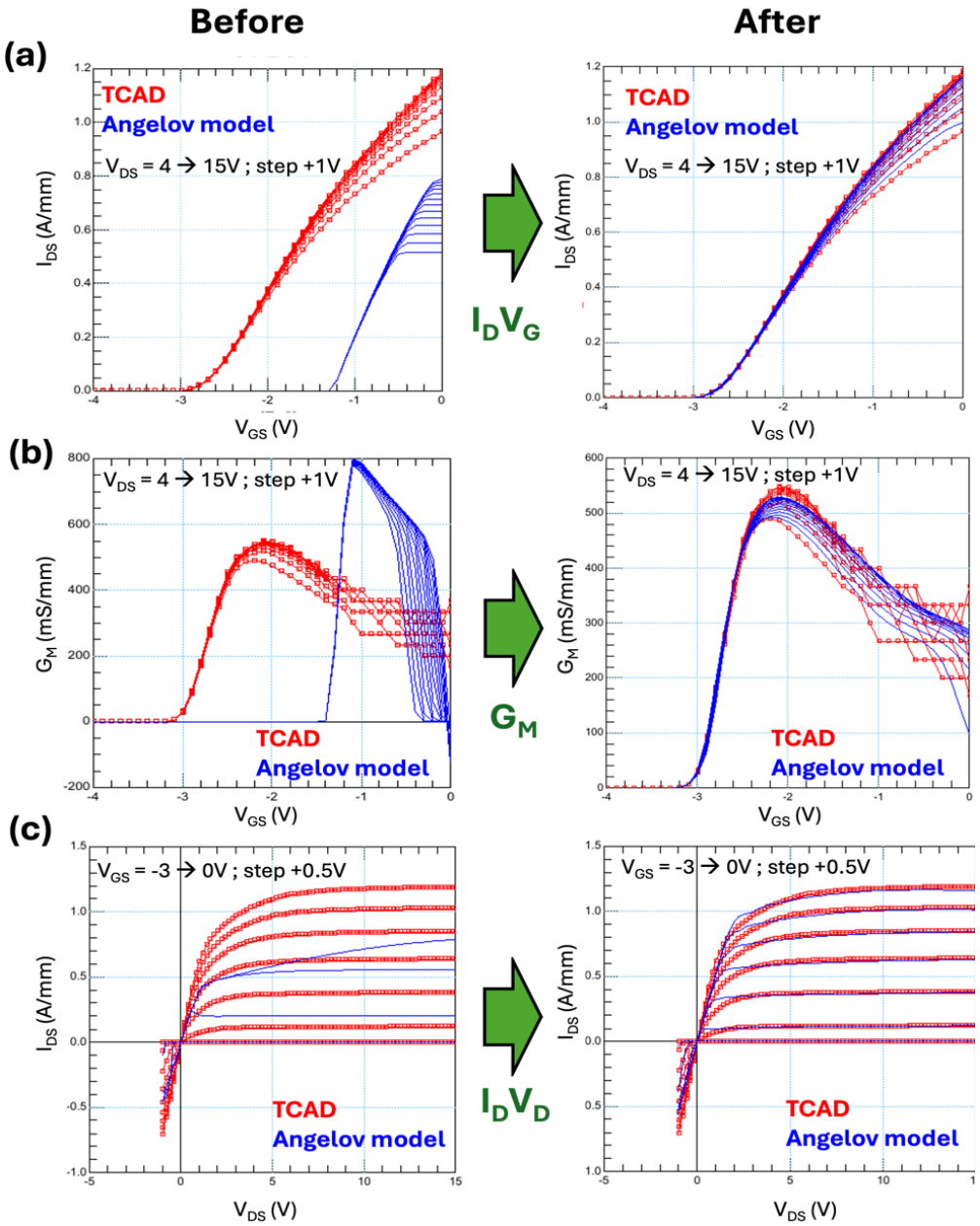


Figure 2.8. DC fitting of I_DV_G (a), G_M (b) and I_DV_D curves (c) before and after optimization of Angelov model with TCAD data.

Such a detailed analysis will also provide proper behavior of the model but can reveal how a qualitative fit along the entire load-line can be challenging. **Figure 2.8** presents the DC results for I_DV_G (a), G_M (b) and I_DV_D (c) between TCAD and the Angelov model for the graded AlGaN channel HEMT. Initially, the fitting is inadequate due to the lack of parameter tuning. However, after multiple iterations and careful optimizations, a qualitative fit is achieved across a broad range of V_{DS} and V_{GS} values. The model captures the electrical behavior of the device and gives a proper representation of the linear shape of the G_M.

4. **S-parameter fitting:** To extract the capacitances between the gate-source (C_{GS}), gate-drain (C_{GD}) and drain-source (C_{DS}), S-parameter ATLAS simulations were performed at several biases in the frequency range 100 MHz – 20 GHz, as detailed in **Table 2.5**.

Table 2.5. Bias conditions used for S-parameter ATLAS simulation to extract capacitances and RF parameters of the Angelov GaN model.

Bias conditions	**Angelov model's nomenclature**	**V_{GS} (V)**	**V_{DS} (V)**	**Freq**	**Remarks**
S parameters at V_{GS} & V_{DS} = 0V	S_0	0	0	100 MHz -20 GHz	Cold FET condition
S parameters for fixed V_{DS} = 0V & variable V_{GS} **Window 1**	A1	-5V to -1V	0	100 MHz -20 GHz	Pinch-off capacitances
S parameters for fixed V_{DS} = 0V & variable V_{GS} **Window 2**	A2	-6V to -3V	0	100 MHz -20 GHz	Off-state capacitances
S parameters for fixed V_{DS} = 0V & variable V_{GS} **Window 3**	A3	-2V to 0V	0	100 MHz -20 GHz	Open channel capacitances
S parameters for fixed V_{GS} = 0V & variable V_{DS}	$S\_V_{G0}\_V_D$	0 V	0 V – 15V	100 MHz -20 GHz	Open channel and high current
S parameters for fixed V_{GS} & variable V_{DS}	G_M_1	-2.2V	0 V – 15V	100 MHz -20 GHz	Biased where G_M is maximum
	G_M_2	-1.0V	0 V – 15V	100 MHz -20 GHz	Biased where current I_{DS} satured
	G_M_3	-2.7V	0 V – 15V	100 MHz -20 GHz	Biased near pinch-off voltage
S parameters for fixed frequency 1GHz, variable V_{GS} **(Window 1,2,3)** & variable V_{DS}	S_V_{D1}	-3.7V – -1.1V	5 V, 10 V, 15V	1 GHz	Pinch-off capacitances
	S_V_{D2}	-5.8V – -4.0V	5 V, 10 V, 15V	1 GHz	Off-state capacitances
	S_V_{D3}	-2.4V – 0.5V	5 V, 10 V, 15V	1 GHz	Open channel capacitances
	$S\_V_G\_V_D$	-3.8 V – 1.0 V	0V-15V	1 GHz	Open channel and high current
S parameters for fixed frequency 10GHz, variable V_{GS} & variable V_{DS}	$S_V_G_V_D$_FC2	-5 V – 0 V	0V-10V	10 GHz	Pinch-off capacitances

The best practice used as a typical routine is described here. At first, the capacitance parameters CGSPI, CGDPI, CDS, CGS0, CGD0, and their related polynomials P10, P11, P40 and P41, were extracted from the S parameter data available in "A1".

This is followed by fine tuning and optimization of the other parameters such as RC, RCMIN, CRF, RI, and RGD, which are frequency dependent. Similarly, remaining polynomials P20, P21, P30 and P31 were extracted from the data available in "S_VG0_VD". These two sets of fitting were iterated for several times, until a satisfactory fit is obtained. **Figure 2.9.a** shows the fitting of capacitances at 1GHz using data "A1", i.e., sweeping V_{GS} at V_{DS} = 0 V, whereas **Figure 2.9.b** shows the same capacitances using "A1" at V_{DS} = 10V. This last is not in the original data base of Angelov Model. We added this bias condition to the model as the large signal and linearity characteristics has been reported up to V_{DS} = 10V.

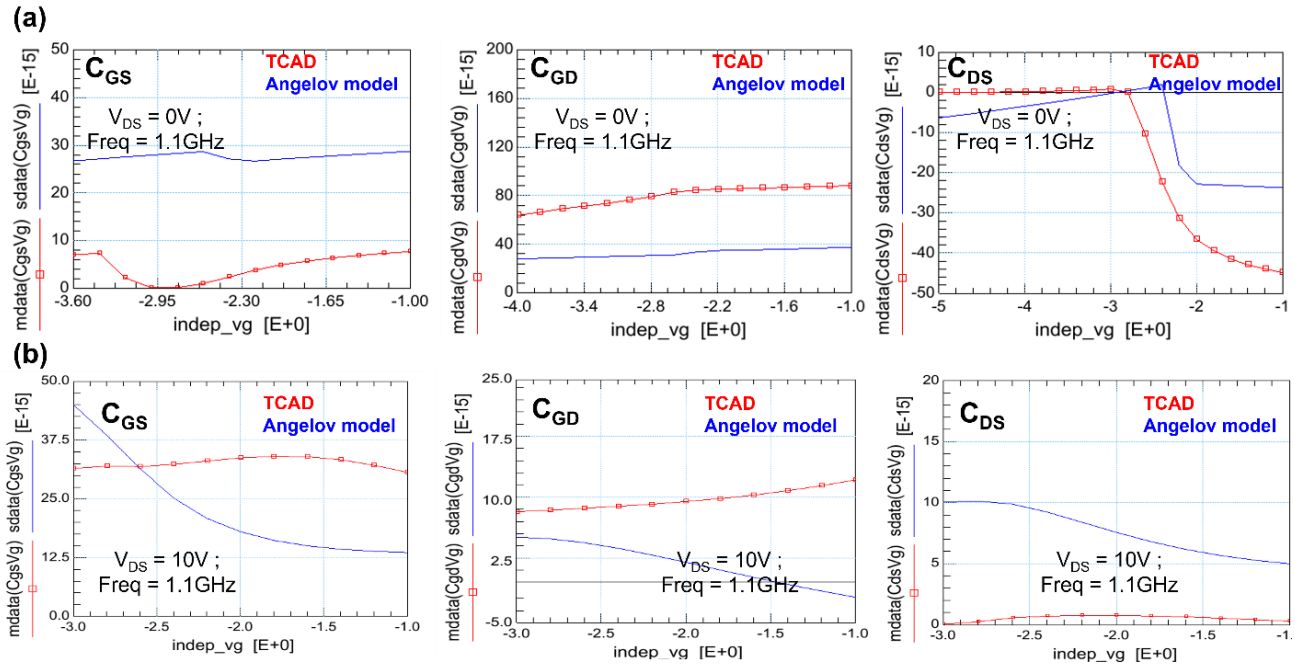


Figure 2.9. (a) Snapshot of C_{GS}, C_{GD} and C_{DS} versus V_{GS} at V_{DS} = 0V and (b) V_{DS} = 10V, ("A1" window), extracted from ICCAP software.

Figure 2.10 shows the capacitance fitting when biased at V_{GS} = -2.7 V, near the pinch-off voltage for V_{DS} = 0V to 15V ("G_M_3" in the **Table 2.5**). Although, there are discrepancies in the capacitances between TCAD and Angelov GaN model, the fitting can be further improved by changing the model equations or by implementing more data such as temperature or pulsed simulations. Another way to improve the fitting is to try new parameter combinations, but this requires numerous iterations that are time-consuming and may not improve anything

It maybe also possible to reduce the range of V_{DS} and V_{GS} to give less freedom to the model during the optimization phases but this would be less realistic from device physics point of view.

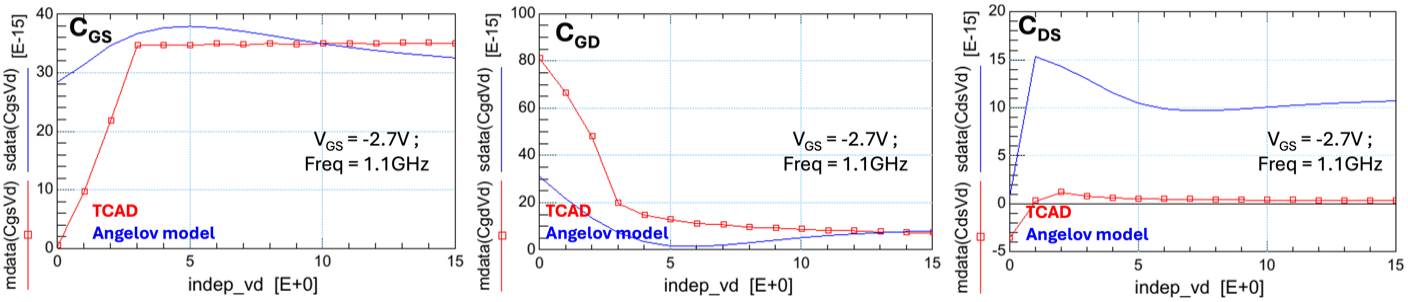


Figure 2.10. Snapshot of C_{GS}, C_{GD} and C_{DS} at V_{GS} = -2.7V (G_M_3 window) for V_{DS} = 0V to 15V, extracted from ICCAP software.

III.2.c. Data fitting along the load-line

To assess the achieved fitting from the Angelov GaN model over a wide range of bias conditions, an arbitrary load-line has been formed on I_DV_{DS} characteristics as shown in **Figure 2.11.a**. The load-line goes from the knee voltage at high current region (V_{GS} = 0 V) to high drain voltages (V_{DS} = 15V) and low current region, typically down to off-state (V_{GS} = -3V). The principal intermodulation parameters, the transconductance G_M **(Figure 2.11.b)** and its higher order derivatives $G_{M'}$, $G_{M''}$ **(Figure 2.11.c, d)** of the Angelov model and TCAD data are very close along the load-line. Such results indicate that the model properly reproduces the HRL's device. Similar to the transconductance, the capacitances were extracted from S-parameters at various bias conditions along the load-line **(see Figure 2.12)**. As noted above, the capacitances can show a poor matching for some points on the load-line, particularly for C_{DS}, suggesting that the scalability of the model with wide polarization points is not easy to manage. Nevertheless, in our case, a single bias point is used to reproduce the large signal and linearity characteristics reported by HRL [34], which is V_{DS} = 14V in deep class AB.

For this study, the fitting was considered to be satisfactory enough to reproduce the performance of HRL's graded AlGaN channel. At this stage, we export the Angelov model to ADS to simulate large signal and linearity characteristics.

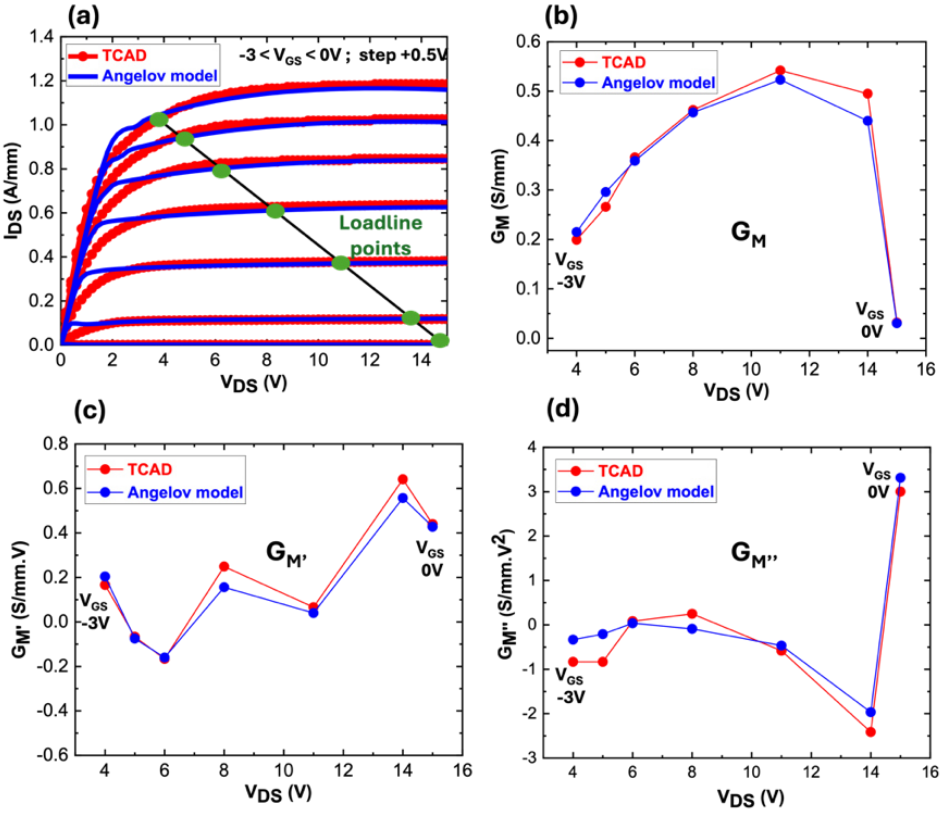


Figure 2.11. Transconductance G_M and its higher order derivatives along the DC load-line.

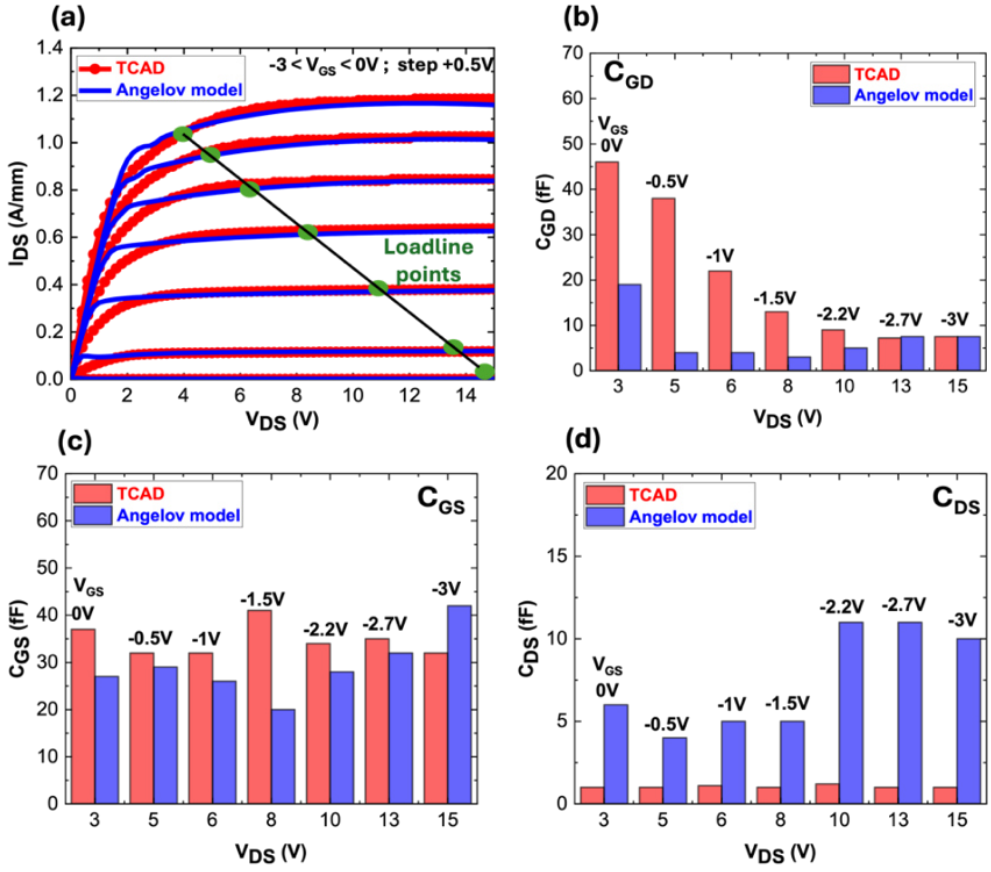


Figure 2.12. Capacitances C_{GD} (a), C_{GS} (b) and C_{DS} (c) along the DC load-line.

III.3. Circuit level simulation in ADS (level 3)

To predict the large-signal and linearity performances at 30 GHz, a harmonic balance simulation is implemented in the commercial software, Advanced Design Systems (ADS), Keysight Technologies. Harmonic Balance (HB) simulation calculates the magnitude and phase of voltages or currents in a potentially nonlinear circuit. It allows simulation of circuits with multiple input frequencies, for e.g, two-tone linearity analysis and other inter-modulation frequencies. Generally, the HB method involves iterations. First, an assumption is made for a given sinusoidal excitation having a steady-state solution, which is then approximated to satisfactory accuracy by means of a finite Fourier series. The circuit elements and the parameters of the HB simulation for large-signal and linearity are discussed in the following sections.

III.3.a. One-tone large signal performances @30GHz

Figure 2.13 shows the snapshot of the circuit diagram used for active load pull analysis. The circuit has been designed as simple as possible without the addition of resistors or extended capacitors, which are normally present experimentally. The transistor (device under test) is a compact FET model imported from ICCAP with the final list of Angelov model parameters.

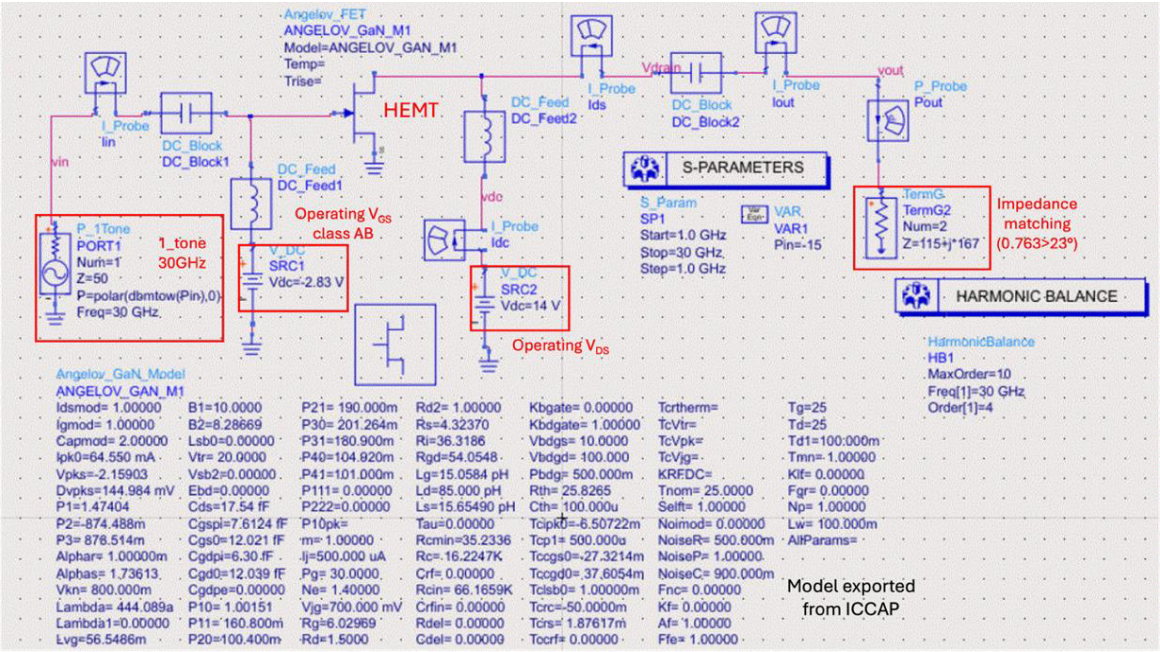


Figure 2.13. Circuit diagram of large signal characteristics at 30GHz.

The transistor is biased through DC sources: SRC1 as gate bias, SRC2 as drain bias and the source terminal is grounded. For this simulation, the operating V_{GS} and V_{DS} are -2.83 V and 14 V, respectively. It is worth noting that the operating V_{GS} is selected based on output current I_{DS} corresponding to the operating class of the transistor, i.e, deep class AB which allows maximizing the PAE performance.

PORT1 acts as an input terminal with a single tone (fixed input frequency) at 30 GHz. We did not change the input impedance and considered 50 ohms, as used in our load-pull test bench at IEMN. This source provides sinusoidal frequency at a specified power, for e.g., P_{in} = -10 dBm, which will be converted to Watts with the dbmtow function and degrees of phase. The A.C. voltage and current flowing out from the input source terminal are labeled, as V_{in} and I_{in}. On the right side of the circuit, the port "TermG" is the output terminal with load impedance Z = 115 +j167, corresponding to the reflection coefficient of 0.763<23°, which is close to the HRL's experimental impedance, 0.76<28°, as reported in [34]. The complex A.C. voltage and current delivered to the output terminal are labeled, as V_{out} and I_{out}. The DC blocks were introduced to avoid unintentional signals altering the device under test. The S-parameter simulations were set up in the frequency range 1 GHz to 30 GHz with a step size of 1 GHz. This allows estimating the power absorbed (from magnitude of S_{11}), which is then involved in the calculation of PAE. On the other hand, the harmonic balance simulation was set up, so that the fundamental frequency is 30 GHz with the Order [1] = 4.

The index [1] shows that only one fundamental frequency is being considered (30 GHz in our case). Order [1] = 4 specifies the number of harmonic frequencies to be calculated for the first frequency, in this case, the harmonics are at 30, 60, 90, and 120 GHz. To determine the optimum order for the simulation, a minimum order is set and then gradually increased in the steps of 1 or 2 harmonics. When the solution does not evolve anymore, the optimum order is reached [49]. The solver for HB simulation is set as robust, Krylov method [50]. The output such as I_{DS} at the operating class, P_{in} (W), P_{dc} (W), P_{abs} (W and dBm) are shown in **Figure 2.14**. The formulas shown in blue are in accordance with the ADS equation styles.

Figure 2.15 shows the output of S-parameter simulation, particularly S_{11}. Here, we can see the magnitude of S_{11} at 30 GHz which is of our interest and to be used in the formula of power absorbed **(Figure 2.14.d)**. This value accounts for the reflected power, thus significantly contributing to the calculation of gain and PAE.

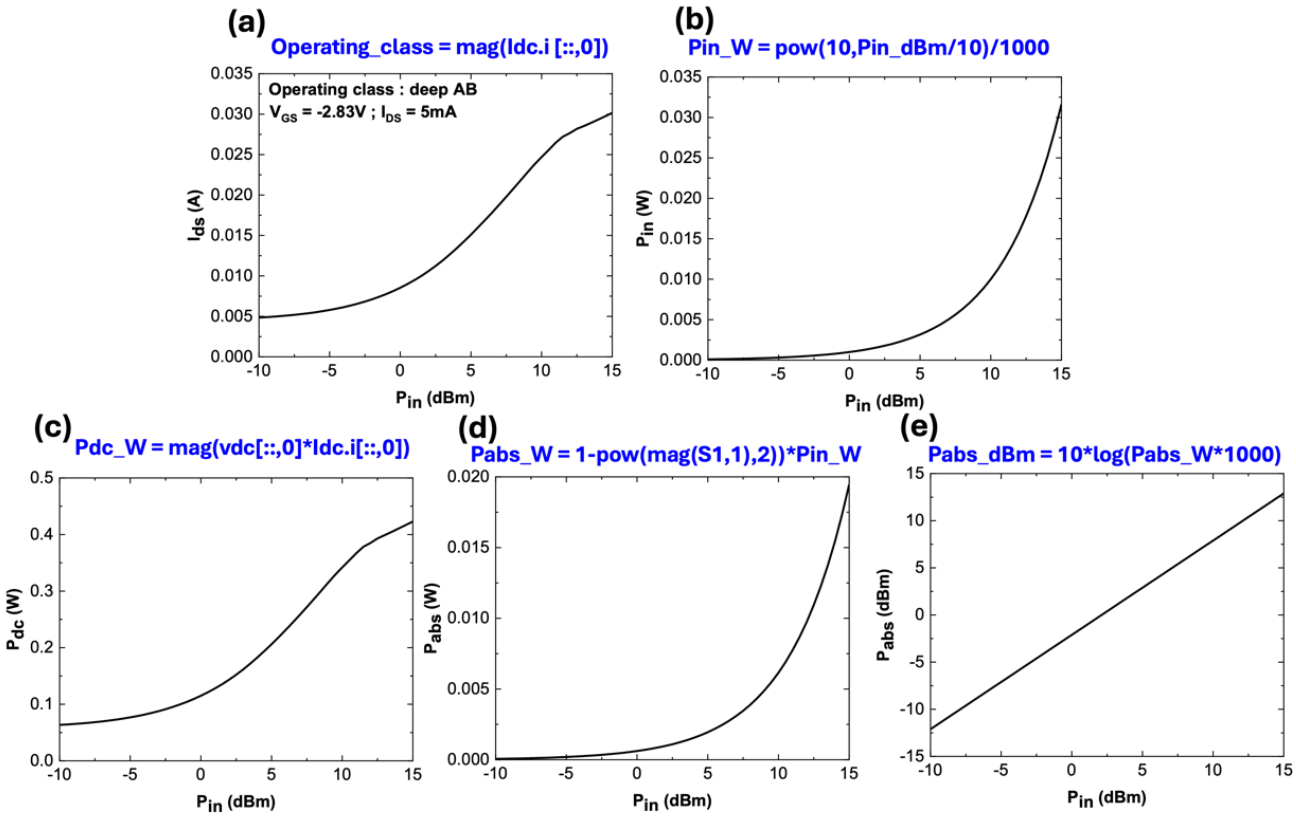


Figure 2.14. Current and output power of harmonic balance simulation for P_{in} from -10 to +15 dBm: (a) I_{DS} at the operating class, i.e., deep AB, (b) P_{in} in Watts vs P_{in} in dBm (unit conversion), (c) P_{dc} in Watts, (d) P_{abs} in Watts, and (e) P_{abs} in dBm.

freq	S(1,1)
1.000 GHz	1.019 / -2.356
2.000 GHz	1.038 / -4.825
3.000 GHz	1.056 / -7.412
4.000 GHz	1.073 / -10.122
5.000 GHz	1.089 / -12.958
6.000 GHz	1.103 / -15.922
7.000 GHz	1.115 / -19.013
8.000 GHz	1.125 / -22.228
9.000 GHz	1.132 / -25.560
10.00 GHz	1.136 / -28.999
11.00 GHz	1.136 / -32.531
12.00 GHz	1.132 / -36.139
13.00 GHz	1.124 / -39.801
14.00 GHz	1.111 / -43.492
15.00 GHz	1.094 / -47.185
16.00 GHz	1.073 / -50.852
17.00 GHz	1.048 / -54.465
18.00 GHz	1.019 / -57.997
19.00 GHz	0.988 / -61.424
20.00 GHz	0.954 / -64.723
21.00 GHz	0.918 / -67.878
22.00 GHz	0.882 / -70.875
23.00 GHz	0.845 / -73.704
24.00 GHz	0.807 / -76.360
25.00 GHz	0.771 / -78.839
26.00 GHz	0.735 / -81.141
27.00 GHz	0.700 / -83.268
28.00 GHz	0.666 / -85.226
29.00 GHz	0.633 / -87.018
30.00 GHz	0.602 / -88.652

Value of S(1,1) used in the Pabs_W formula

Figure 2.15. Reflected signal S11 from S parameter simulation for the optimized output impedance (0.763>23°).

The output power is calculated from the V_{out} and conjugate of I_{out} for the fundamental frequency 30 GHz (**Figure 2.16.a** (in Watts) and **Figure 2.16.b** (in dBm). The P_{OUT} at maximum PAE is estimated to be 3.30 W/mm at V_{DS} = 14 V, which is close to the values reported by HRL (3.0 W/mm). The gain and maximum power added efficiency were 15.2 dB (c) and 65%, (d) respectively, versus 14 dB and 65% for HRL experimental data [34]. The comparison of ADS simulation results and HRL's data are shown in **Figure 2.17**. Simulated large-signal performances at 30 GHz are in good agreement with the experimental data.

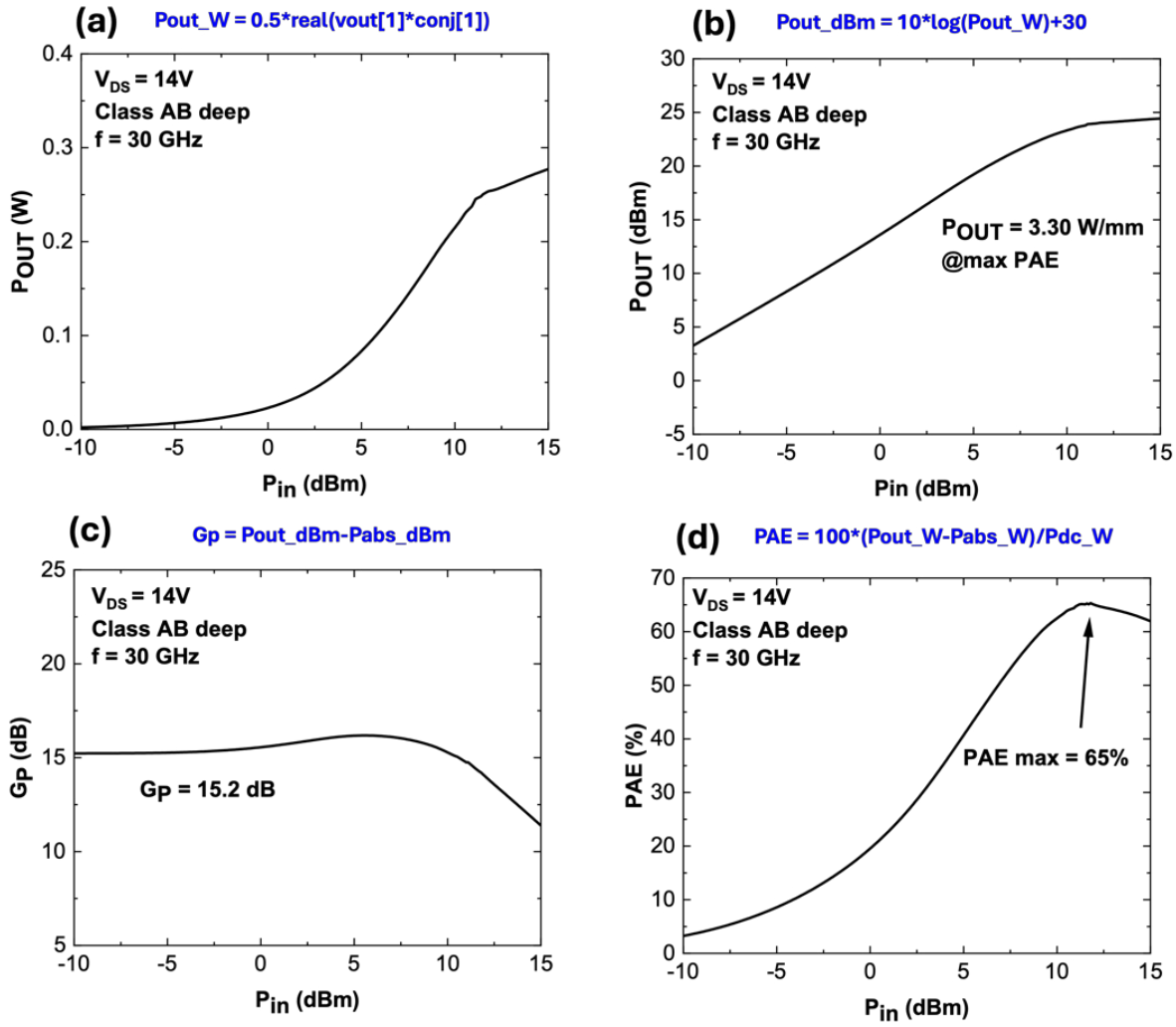


Figure 2.16. Output power calculated for fundamental frequency (30 GHz) from the complex V_{out} and conjugate of I_{out}. (a) Pout in Watts, (b) Pout in dBm, (c) Gain in dB and (d) PAE (%) (impedance matching I = 0.763>23°).

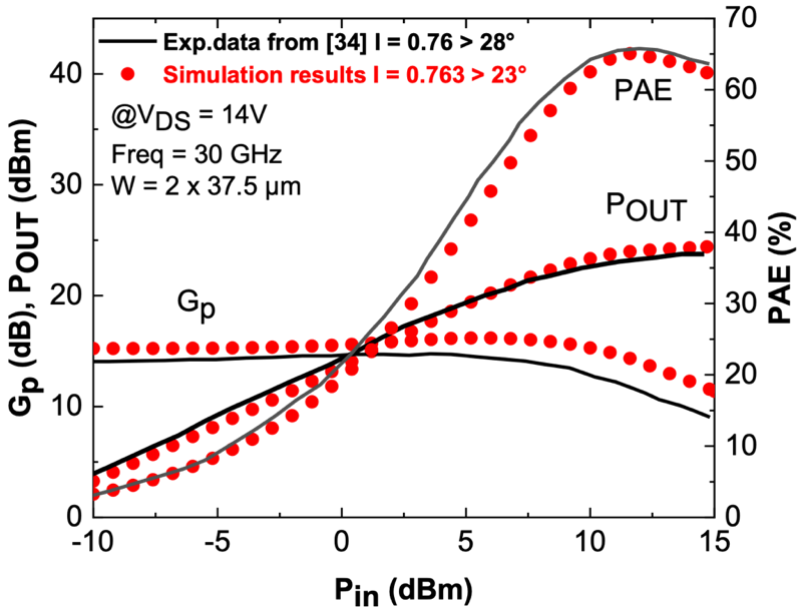


Figure 2.17. Comparison of large-signal performance from HRL data with large signal simulation using the optimum impedance matching.

III.3.b. Two-tone linearity performances @30GHz

The circuit diagram used to simulate two-tone linearity performances is shown in **Figure 2.18**. We can see many commonalities between the circuit of large signal load pull and linearity simulation. The device under test is the same transistor defined as Angelov GaN model used for large signal simulation. The bias condition (V_{GS} and V_{DS}), and impedance matching are same as the one-tone simulation. As can be noticed the difference lies at the input port, two RF signals with frequencies Freq1 and Freq2 are injected with a spacing of 10 MHz with a center frequency being at 30 GHz. Similarly, two frequencies have been set at the harmonic balance simulation setting. The mixing of two-tone frequencies was noticed for a single Pin of -10dBm. The resulting mixing frequencies are shown in **Figure 2.19.a**. In 2-tone simulation, the fundamental frequency corresponds to 30 GHz minus/plus the 10 MHz spacing (29.99000 GHz and 30.01000 GHz). These 2 frequencies have been considered to calculate the first order. Their respective index **(Figure 2.19.a)** is 4 and 5 (highlighted in black). For the third-order inter-modulation (IM_3), it corresponds to the frequency of 30.03000 GHz. Its index is 6 (highlighted in red). **Figure 2.19.b** shows the power delivered by the fundamental frequency, third-order inter-modulation and the linearity figure-of-merit namely C/IM_3.

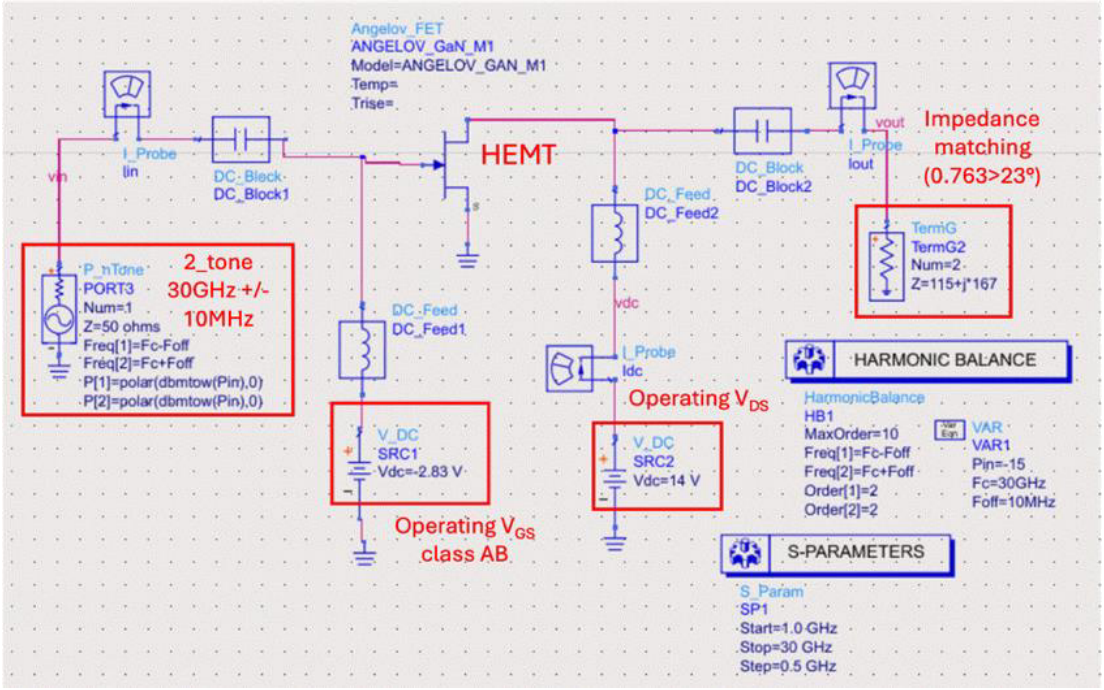
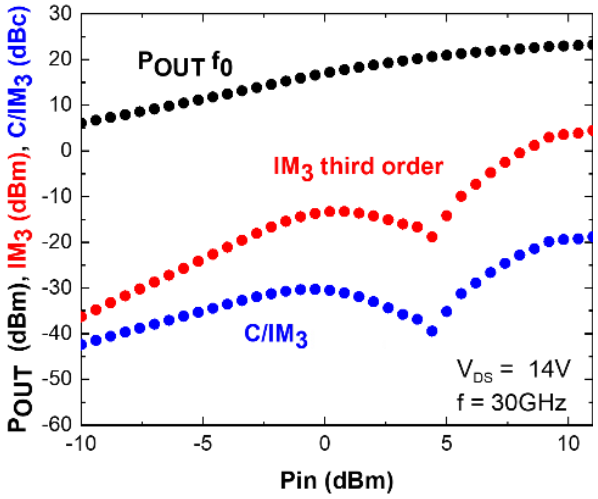


Figure 2.18. Circuit diagram used in ADS for two-tone linearity intermodulation analysis.

(a)

	freq	Mix(1)	
Pin=-10.000000			
	0.0000000 Hz		0
	20.00000 MHz		-1
	40.00000 MHz		-2
	29.97000 GHz		2
IM_1	29.99000 GHz	[4]	1
	30.01000 GHz	[5]	0
IM_3	30.03000 GHz	[6]	-1
	59.98000 GHz		2
	60.00000 GHz		1
	60.02000 GHz		0
	89.99000 GHz		2
	90.01000 GHz		1
	120.0000 GHz		2

(b)



$P_{OUT}(f_0) = (0.5*real(vout[4]*conj(Iout.i[4]))+(0.5*real(vout[5]*conj(Iout.i[5]))$

$IM_3 = 0.5*real(vout[6]*conj(Iout.i[6]))$

$-C/IM_3 = -(10*log(P_{out}/IM_3))$

Figure 2.19. (a) Table of mixing frequencies (b) fundamental, third-order inter-modulation and C/IM₃ ratio.

Figure 2.20 is a comparison of the linearity simulation with HRL's experimental data [34]. The simulation results are quite close to the HRL's experimental results. HRL reported that at 6 dB output power backed-off from maximum PAE, C/I was greater than 30 dBc with an associated PAE of 50%. In our simulation, at 6 dB output power backed-off from peak PAE, we also achieved C/I = -30dBc with an associated PAE of 46%, which is underestimated but consistent with their experimental results.

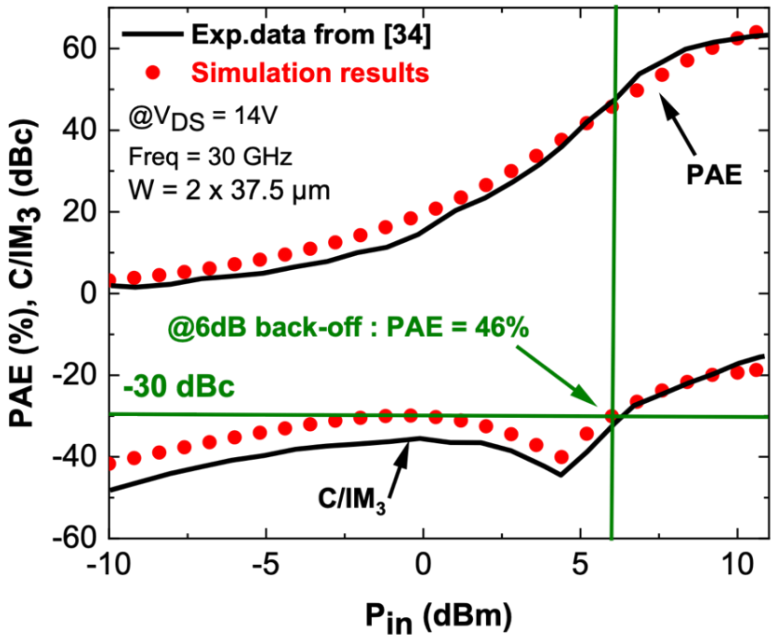


Figure 2.20. Comparison between HRL linearity results and 2-tone ADS simulation.

This high C/I ratio indicates that the interference is significantly weaker than the carrier signal, which is ideal for maintaining signal quality and integrity. One of the major challenges is to obtain a high C/I ratio while still achieving excellent RF performances. Generally, it is possible to obtain a correct C/I ratio at the expense of power performance, as we will see in the next section. This first part enabled us to validate the workflow developed to study the graded AlGaN channel HEMT. Despite difficulties of obtaining a proper matching between the Angelov model and TCAD simulations, the main characteristics of the graded channel have been reproduced. It is worth noticing that this represents the first successful simulation of both large signal and linearity characteristics for a GaN HEMTs with short dimensions. The next section of this chapter will provide a comparative performance analysis (at device and circuit level) of graded channel to standard AlGaN/GaN HEMTs. The aim is to provide insights into the benefits of the graded technology.

IV. Graded channel versus AlGaN/GaN HEMT

IV.1. Device-level comparison with TCAD SILVACO

To study the impact of the AlGaN graded channel, we decided to compare it to a conventional AlGaN/GaN HEMT. We then investigated their performances with TCAD SILVACO (level 1) as well as in terms of linearity and large signal in ADS (level 3). Therefore, similar structures in ATLAS with and without graded AlGaN channel have been generated **(Figure 2.21)**. The graded channel structure being the same as the one described in the previous section.

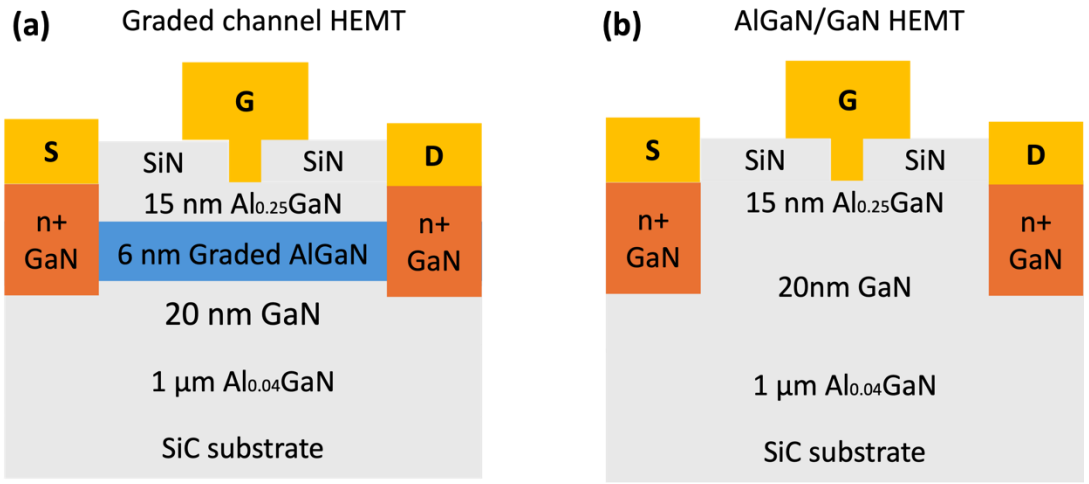


Figure 2.21. (a) Graded AlGaN channel (REF) and (b) GaN channel HEMT structures.

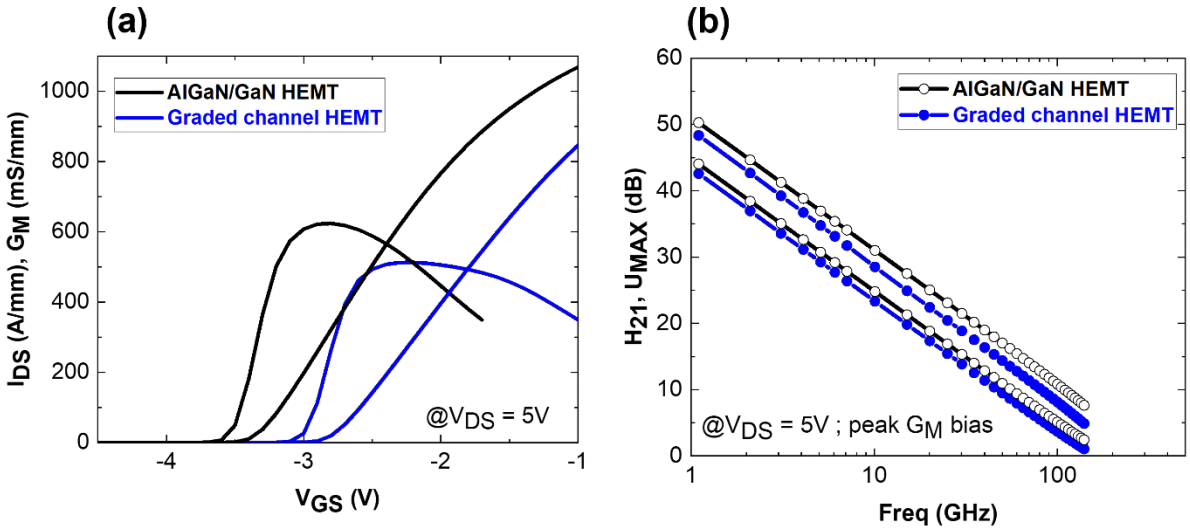


Figure 2.22. (a) DC and (b) RF small signal characteristics comparison for graded channel and GaN channel HEMTs.

Both HEMTs have the same parameters and designs, except the N_s value that was adjusted as the graded part was removed. The value is larger for the conventional GaN channel HEMT ($1.5\times10^{13}/cm^{-2}$) because the 2DEG is generated at the heterojunction between the AlGaN barrier and the GaN channel. So, the piezoelectric effects are thus stronger without the graded channel. DC characteristics (I_DV_G, G_M) and RF small signal (F_T, F_{MAX}) for both structures are presented in the **Figure 2.22**. Standard AlGaN/GaN HEMT delivers higher DC and small signal characteristics compared to the graded AlGaN channel HEMT, owing to a higher 2DEG carrier density. **Table 2.6** summarizes the main characteristics of these two structures.

Table 2.6. Summary of DC and RF small signal performances between graded channel and GaN channel HEMT simulated in ATLAS.

Characteristics	Graded channel HEMT	AlGaN/GaN HEMT
N_S	$9.0\times10^{12}/cm^{-2}$	$1.5\times10^{13}/cm^{-2}$
Idmax @V_{GS} = -1V	850 mA/mm	1070 mA/mm
Peak G_M	513 mS/mm	630 mS/mm
Linear G_M	High	Low
F_T/F_{MAX}	165/290 GHz	180/360 GHz

At first sight, the standard AlGaN/GaN HEMT appears to be a better choice than the graded AlGaN channel HEMT. However, we can see that a major difference lies in the G_M shape. The G_M for the graded channel HEMT exhibits flatness over a wide V_{GS} range, whereas the AlGaN/GaN HEMT shows a G_M with a greater peak but an abrupt collapse. This suggests more intermodulation distortion, which will lead to a degradation in the device linearity. To better compare them, we have aligned G_M and its derivatives $G_{M'}$ and $G_{M''}$ to compensate the shift in the threshold voltage that results from the different 2DEG properties **(Figure 2.23)**. From **Figure 2.23.a**, we can apply a simple calculation of difference in the $G_{M\ peak}$ and the G_M at a voltage range of 1V for both structures. The parameter can define a "roll-off" factor. For the graded AlGaN channel, the difference is equal to 93 mS/mm (18% decrease) whereas for the standard AlGaN/GaN HEMT, the difference is 245 mS/mm (39% decrease).

This confirms the better flatness of G_M for the graded channel HEMT. This improved linearity is also reflected on $G_{M'}$ and $G_{M''}$. In fact, the amplitudes of the derivatives are smaller for the graded channel, as shown in **Figure 2.23.b, c**, suggesting less impact of intermodulation distortions. To investigate further the graded AlGaN channel and its impact on the device characteristics, we have extracted from ATLAS, the electron distribution along the channel for both devices **(Figure 2.24)**.

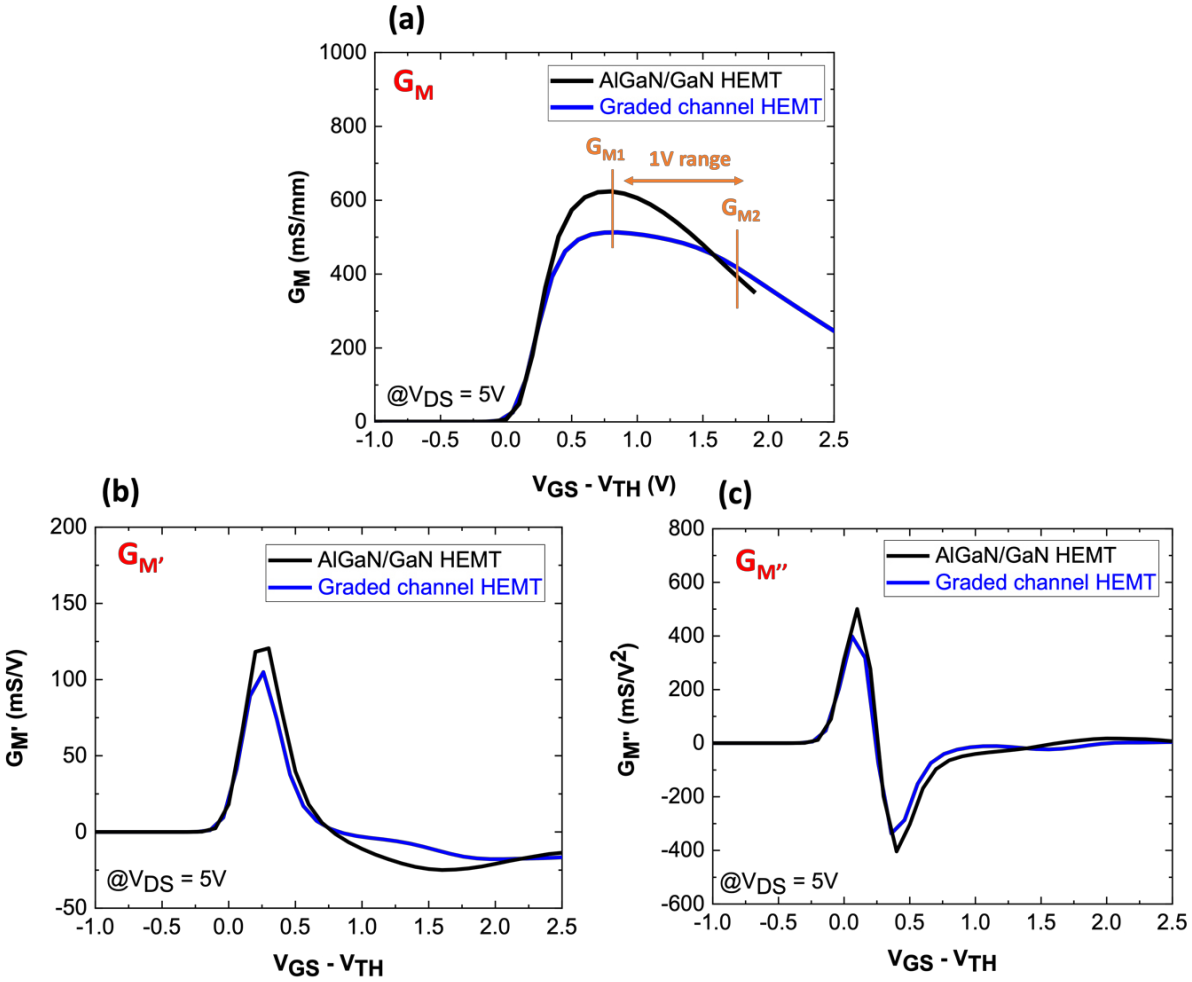


Figure 2.23. Comparison of (a) G_M, (b) $G_{M'}$ and (c) $G_{M''}$ for both simulated structures.

It can be noticed that the electron distribution at the interface between the barrier/graded channel **(Figure 2.24.a)** and the barrier/GaN channel **(Figure 2.24.b)** is quite different. Indeed, for the AlGaN/GaN HEMT, a standard distribution at the heterojunction is observed with the formation of a sharp 2DEG at the interface between these two layers. In contrast, for the graded AlGaN channel, a spread of the electron concentration inside the graded layer can be observed.

This polarization gradient gives rise to a three-dimensional electron (3DEG) 'slab' instead of standard well-confined 2DEG observed for an AlGaN/GaN heterostructure. To study the impact of this 3DEG, the lateral electric field has been extracted at peak G_M bias and V_{DS} = 10V along the channel for both structures (**Figure 2.25)**.

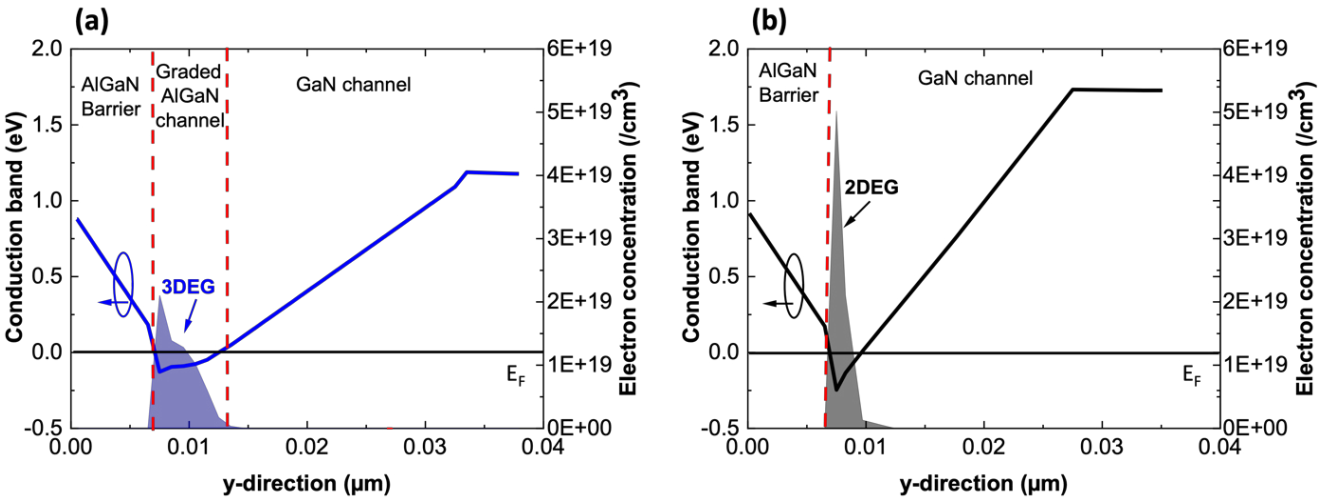


Figure 2.24. Electron distribution and conduction band diagram of graded channel (a) and GaN channel HEMT (b), extracted from ATLAS.

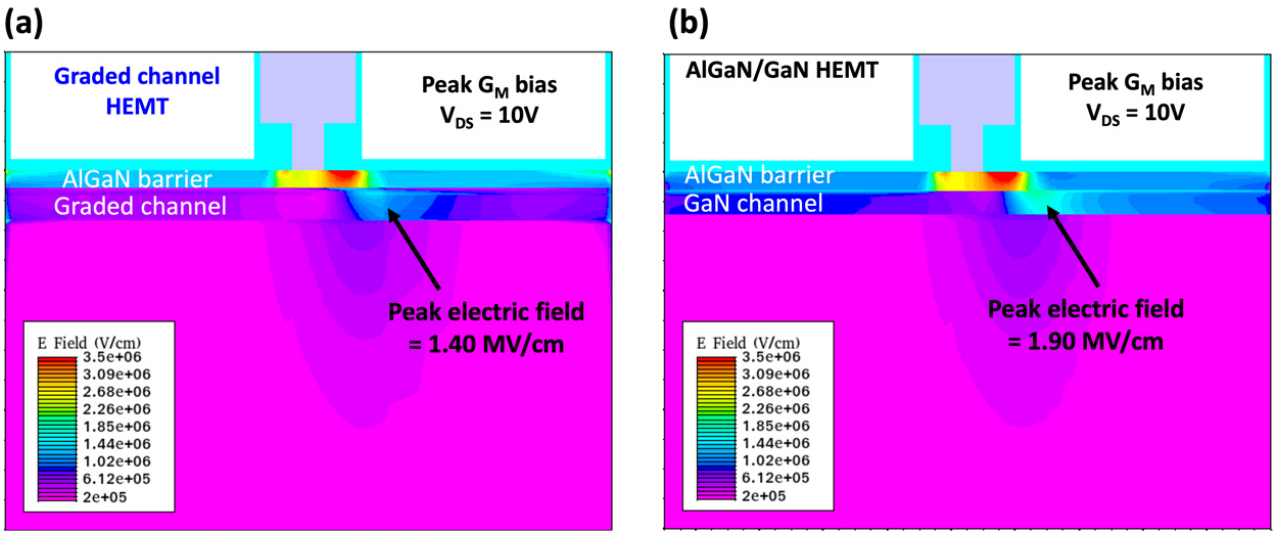


Figure 2.25. Electric field distribution for graded channel (a) and GaN channel HEMT (b), extracted from ATLAS.

From TCAD simulations, it appears that the electric field peak of the graded AlGaN channel **(Figure 2.25.a)** is lower than the standard GaN channel **(Figure 2.25.b)**. The peak electric field in the AlGaN channel is equal to 1.40 MV/cm against 1.90 MV/cm for the GaN channel HEMT. We also extracted the electric field profiles using a cutline along the channel. **Figure 2.26** shows that the graded channel allows a 25% reduction in peak field, which is consistent with previous report [35, 51].

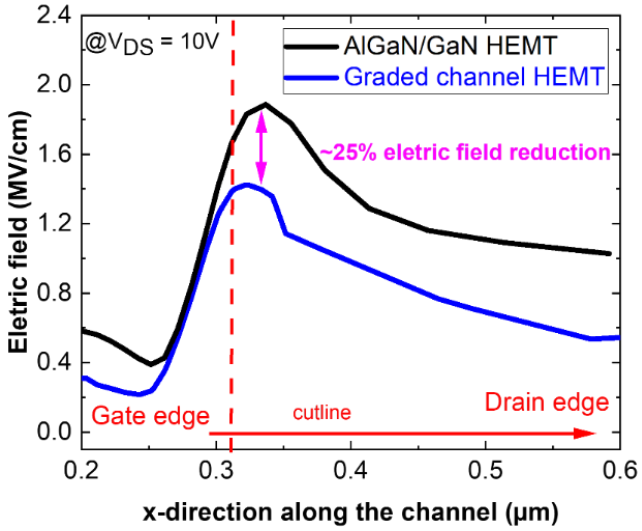


Figure 2.26. Electric field profiles along the channel between AlGaN/GaN and graded channel HEMT, extracted from ATLAS.

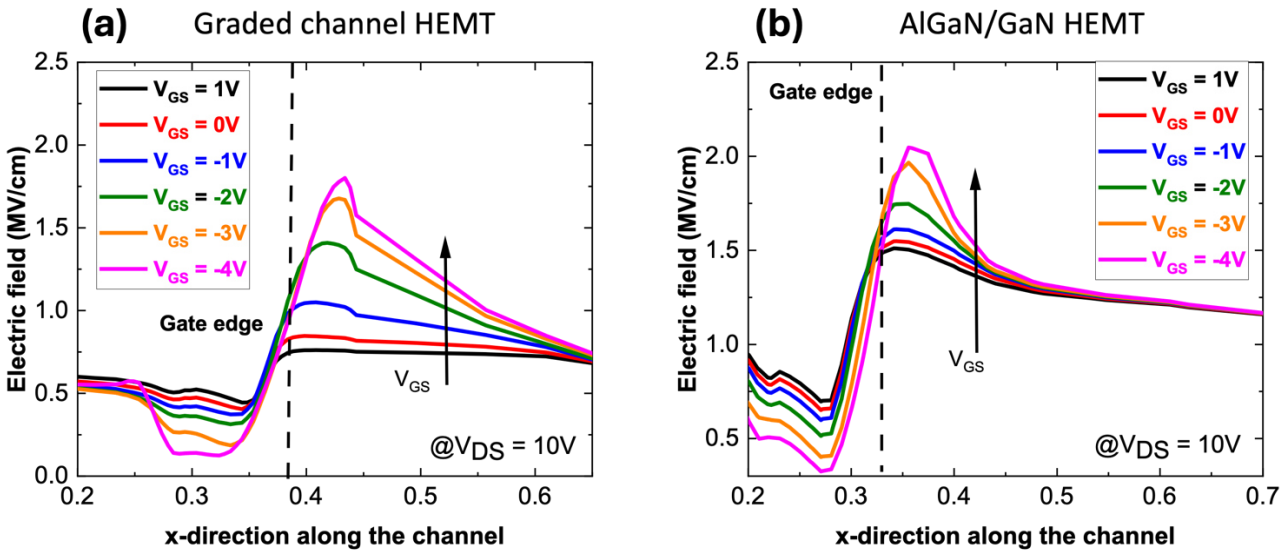


Figure 2.27. Electric field along the channel for (a) graded channel and (b) AlGaN/GaN HEMT, extracted from ATLAS at V_{DS} = 10V and V_{GS} ranging from -4V to +1V.

Moreover, the electric field is not only lower at peak G_M bias within the channel but also over the whole gate voltage range from V_{GS} = -4V until +1V, as shown in **Figure 2.27**. This also suggests that this reduction of the peak electric field also enables higher breakdown voltage for the graded channel technology.

These superior results can be attributed to the 3DEG distribution along the channel and therefore, inserting an AlGaN gradient allows for a reduction of the electric field at the gate edge towards the drain, contributing to a flatter transconductance. In terms of RF small signal performances, the cut-off frequency (F_T) was also extracted from S-parameters simulations at various V_{GS} for both devices. As shown in **Figure 2.23.a**, the graded channel has a more linear transconductance, enabling to maintain high F_T values over a wider V_{GS} range (**Figure 2.28.a**). In contrast, the standard AlGaN/GaN device achieves a slightly higher peak F_T at peak Gm but undergoes significant drop afterward. This behavior is attributed to the ability of the graded channel to handle greater electron velocity saturation compared with the conventional AlGaN/GaN structure. Specifically, the channel velocity has been extracted from TCAD simulations for both structures.

Figure 2.28.b indicates that the graded channel is less affected by the saturation velocity limitation caused by hot phonon scattering. This is due to its 3DEG configuration, resulting in a more linear G_M response.

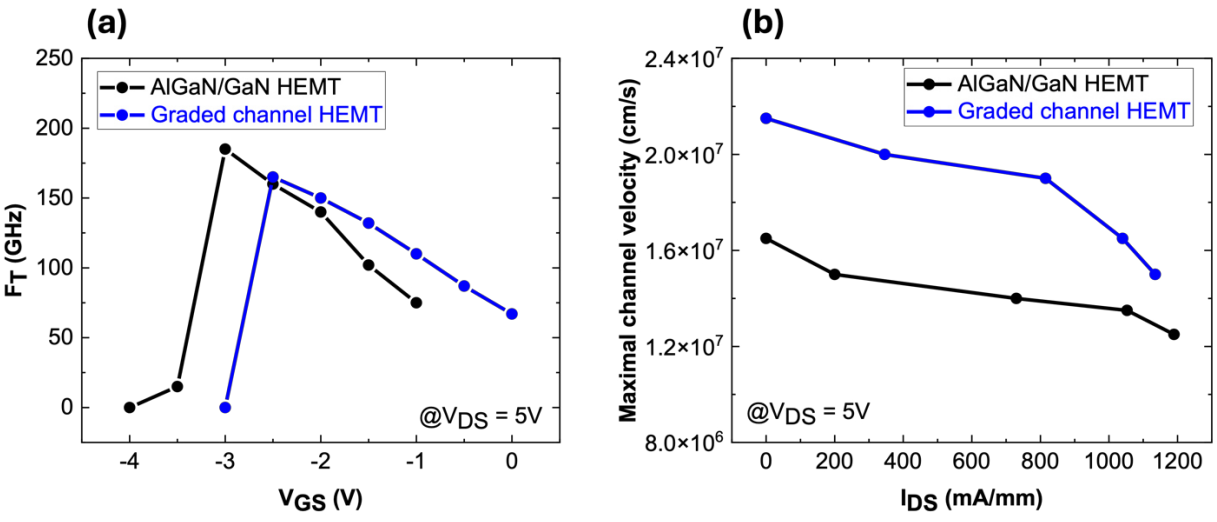


Figure 2.28. (a) Simulated F_T comparison between standard AlGaN/GaN and graded channel HEMT at V_{DS} = 5V for different V_{GS}, (b) extracted channel velocity at different current level.

In this first comparative section, we have seen that the AlGaN/GaN HEMT delivers superior DC and small signal performances than the graded channel HEMT. However, it appears that the graded channel yield in a 3DEG configuration, inducing a reduced electric field while maintaining a high electron velocity, thus improving G_M flatness and increasing device's linearity. The next section will focus on the comparison of these two structures at the circuit level to compare their linearity performances.

IV.2. Large signal and linearity performances

IV.2.a. ICCAP modelling and data fitting

As shown in the workflow description, we used the Angelov model based on data from ATLAS SILVACO to simulate the AlGaN/GaN HEMT at the circuit level. **Figure 2.29** shows the DC characteristics from TCAD (red color) with the associated Angelov model fitting (blue color). By tuning the Angelov model, a proper fit is achieved for the whole DC characteristics.

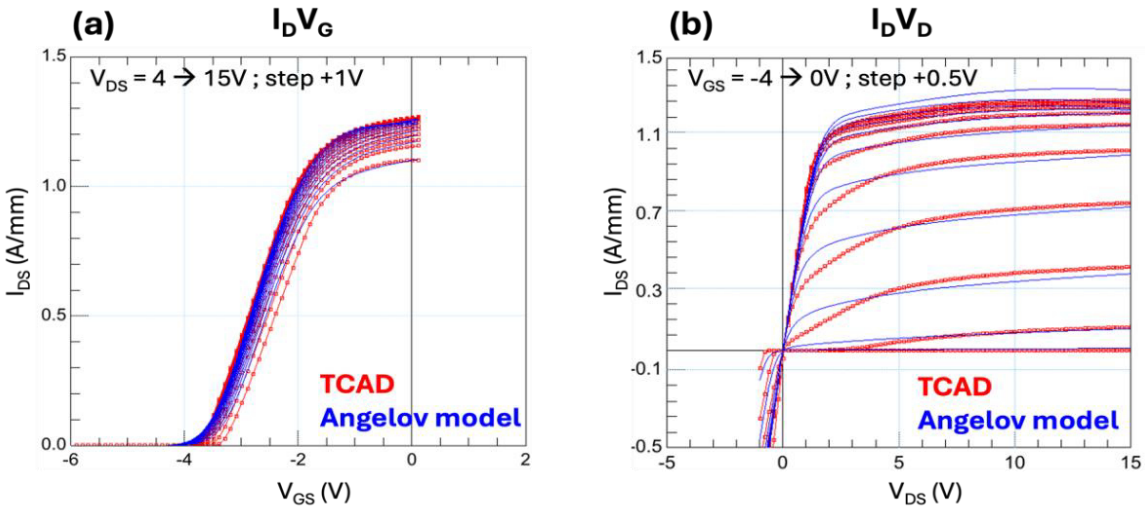


Figure 2.29. DC fitting between Angelov model and TCAD data.

Figure 2.30.a shows some fitting of capacitances using data "A1" window, i.e., sweeping V_{GS} at V_{DS} = 10V, whereas **Figure 2.30.b** displays the same capacitances using "G_M_3" window, sweeping V_{DS} at V_{GS} = -3.2V (near pinch-off). As seen with the graded channel, a perfect fit was not achieved for capacitances but can probably be improved by trying other parameter combinations within the Angelov model. However, it can be pointed out that this empirical tuning would be time consuming.

Therefore, in this framework, the overall fitting was considered satisfactory enough to perform the AlGaN/GaN HEMT structure comparison. The purpose is to investigate whether we can access information about the structure at the circuit level and compare its performance with the graded channel HEMT.

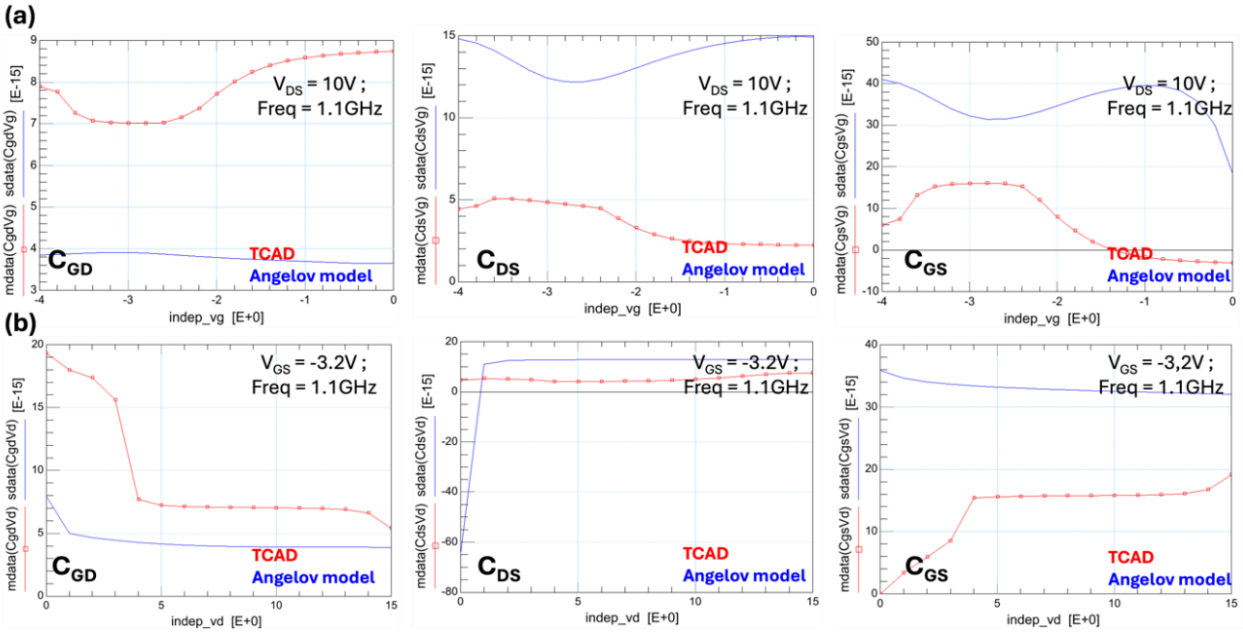


Figure 2.30. (a) Snapshot of C_{GS}, C_{GD} and C_{DS} versus V_{GS} at V_{DS} = 10V ("A1" window) and (b) at V_{GS} = -3.2V for V_{DS} = 0V to 15V ("G_M_3" window), extracted from ICCAP software.

IV.2.b. Large signal and linearity characteristics @30GHz

In this last part, large signal and linearity performances at the circuit level of both structures are compared. Large signal simulations were performed under the same voltage conditions (V_{DS} = 14V, deep class AB) and with the same load-pull circuit implemented previously in ADS. **Figure 2.31** shows the power performance comparison of the graded channel and the AlGaN/GaN HEMT at 30 GHz. By tuning the output impedance matching, we can see that the AlGaN/GaN HEMT also delivers excellent performances with a max PAE of 68.5%, owing to a high gain due to a higher G_M and RF small signal characteristics. We can see that the obtained P_{OUT} is comparable (3.2 W/mm) to the graded channel HEMT (3.3 W/mm). The slight discrepancy is mainly due to the impedance matching used and/or the data fitting with the Angelov model.

Indeed, we chose to take the same matching impedance than the graded channel for a fair comparison. From RF power performance point of view, the standard AlGaN/GaN HEMT offers similar or even better performance than the graded channel HEMT. However, this should be balanced with the linearity performances that must also be considered. For the linearity comparison, the same 2-tone circuit in ADS was used as previously. **Figure 2.32** shows a comparison of the linearity performances from the graded channel and standard AlGaN/GaN HEMT.

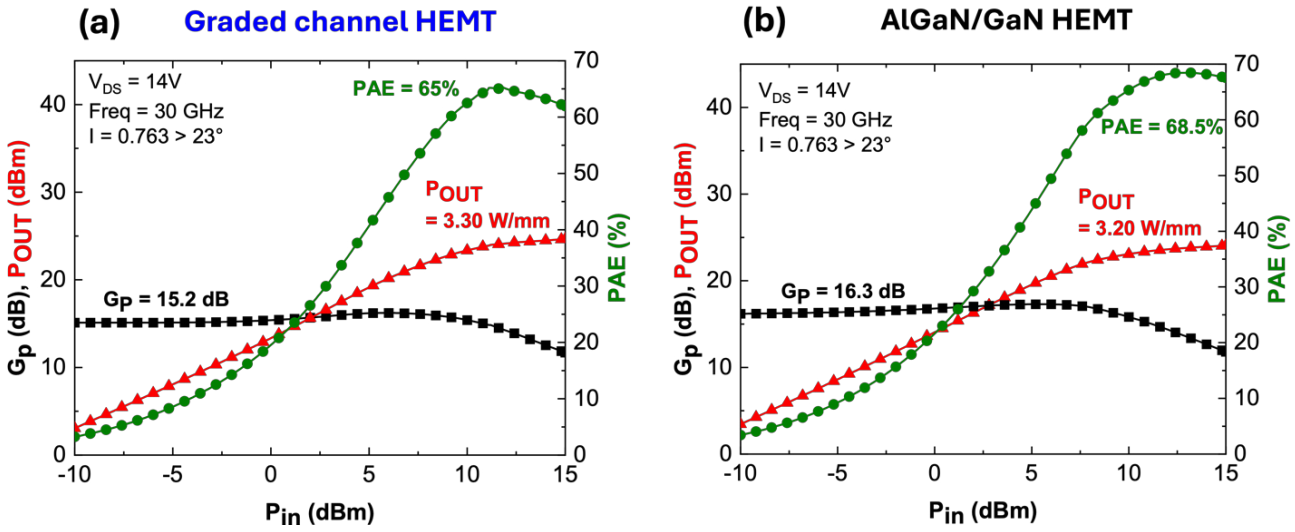


Figure 2.31. Large signal performances simulated at 30 GHz for the graded channel (a) and standard AlGaN/GaN HEMT (b).

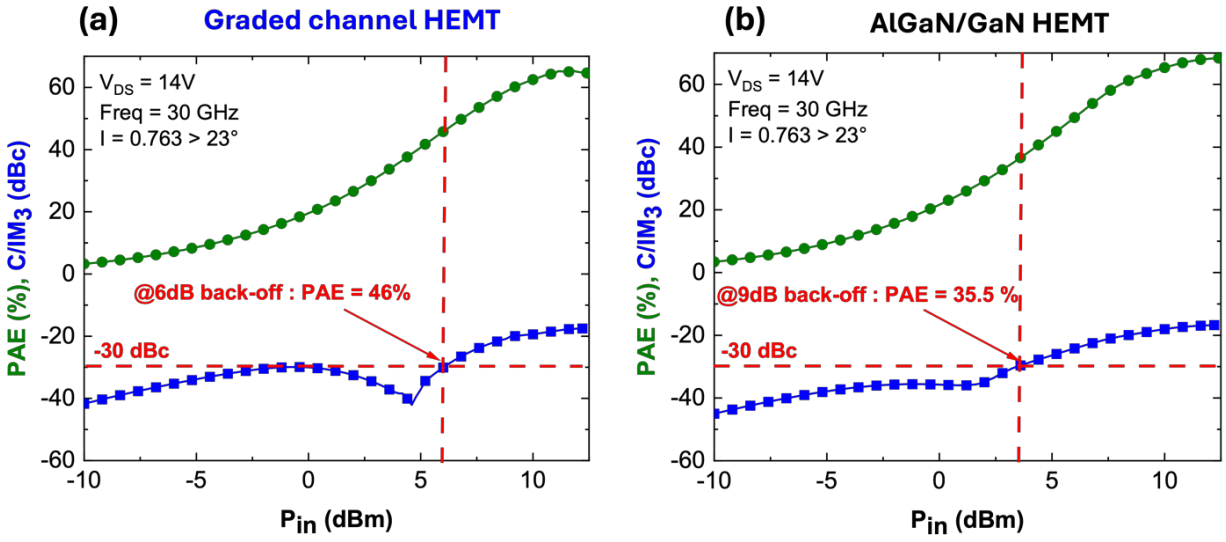


Figure 2.32. Linearity performances simulated at 30 GHz for the graded channel (a) and standard AlGaN/GaN HEMT (b).

At maximum PAE (P_{in} = 12 dBm), the graded AlGaN channel (**Figure 2.32.a**) has a C/I ratio of 17.5 dBc whereas the standard AlGaN/GaN HEMT (**Figure 2.32.b**) has a lower C/I ratio with 16.5 dBc showing a degraded linearity. Moreover, if we focus on the linear regime operation of the transistor at C/I = 30dBc, it can be observed that at 6dB output power backed-off (from peak PAE), the graded AlGaN channel achieved C/I = 30dBc with an associated PAE equal to 46%. On the other hand, the AlGaN/GaN HEMT reaches C/I = 30dBc at 9dB output power backed- off with an associated PAE of 35.5%. Therefore, it is necessary to back-off significantly further from the peak PAE to achieve a good linearity which then deteriorates the associated PAE (by more than 10 points difference). Thus, for many applications, graded AlGaN channel technology offers clear advantages over conventional AlGaN/GaN HEMTs by reducing intermodulation distortion for power amplifiers while delivering superior power-added-efficiency.

V. Conclusion chapter 2

For high frequency beyond 30 GHz, the graded AlGaN channel HEMT is an attractive solution to overcome the trade-off between high linearity and high power-added-efficiency. In-depth understanding requires advanced device simulation as well as device development to reveal its potential. Thus, we developed a workflow using multiple software with the aim of addressing the whole figure of merits at the device and circuit level.

Therefore, large-signal and linearity performances of promising graded channel based HEMTs from HRL's device architecture have been reproduced by hybrid simulation method that involves three different levels, starting from ATLAS (SILVACO), compact transistor modeling (Angelov GaN Model, ICCAP) and circuit level simulation (ADS). By using harmonic balance method and matching load impedance, the output power, gain, power added efficiency, C/IM3 were found to be comparable with the HRL's experimental data. Thus, this three-level simulation approach is suitable to reproduce experimental results for a specific bias condition and could open more opportunities to study variations in the epitaxial layers or device architecture. For instance, level 1 is particularly adapted to study phenomena at the epitaxial level that do not involve non-linear electrical phenomena. However, it is important to point out that the scalability of the model is difficult to achieve, which remains one of the main limitations. For instance, optimization and data fitting required a considerable number of iterations (more than one hundred needed to fit the parameters).

The large signal and linearity results presented in this study have been achieved for a specific bias condition and would require a complete tuning of the full workflow with other configurations. Nevertheless, large signal performance and linearity of the graded AlGaN channel HEMT could be compared to a standard AlGaN/GaN HEMT based on state-of-the-art HRL's performance. TCAD DC and RF small signal characteristics were investigated. The electric field and the channel velocity under different conditions were extracted for both structures. We observed that the insertion of a graded channel decreases the electric field peak at the gate edge and improves the electron velocity. In turn, the formation of a 3DEG enables to spread the electric field (such as field plate but without the parasitic induced capacitance increase drawback) and achieve flat G_M, enhancing the linearity performance. Then, we used harmonic balance simulations to compare the two technologies. Under the same simulation conditions, it was shown that the standard AlGaN/GaN device can reach comparable or even higher PAE. However, the linearity is degraded because of the need for more back-off to reach a linear regime, directly affecting the associated PAE. As shown in this chapter, GaN-based simulation can now provide a deeper understanding of complex physical phenomena and support new technology development.

References chapter 2

[1] E. R. Srinidhi et G. Kompa, « Investigation of IMD3 in GaN HEMT based on extended volterra series analysis », in 2007 European Microwave Integrated Circuit Conference, Munich, Germany: IEEE, oct. 2007, p. 52-55. doi: 10.1109/EMICC.2007.4412645.

[2] C. Du et al., « A review on GaN HEMTs: nonlinear mechanisms and improvement methods », J. Semicond., vol. 44, nº 12, p. 121801, déc. 2023, doi: 10.1088/1674-4926/44/12/121801.

[3] A. Tarakji et al., « Large-signal linearity in III-N MOSDHFETs », IEEE Electron Device Lett., vol. 24, nº 6, p. 369-371, juin 2003, doi: 10.1109/LED.2003.813355.

[4] J. B. Khurgin, S. Bajaj, et S. Rajan, « Elastic scattering by hot electrons and apparent lifetime of longitudinal optical phonons in gallium nitride », Applied Physics Letters, vol. 107, nº 26, p. 262101, déc. 2015, doi: 10.1063/1.4938745.

[5] C. H. Oxley, M. J. Uren, A. Coates, et D. G. Hayes, « On the temperature and carrier density dependence of electron saturation velocity in an AlGaN/GaN HEMT », IEEE Trans. Electron Devices, vol. 53, nº 3, p. 565-567, mars 2006, doi: 10.1109/TED.2005.863540.

[6] T. Palacios et al., « Influence of the Dynamic Access Resistance in the$g_m$andf_TLinearity of AlGaN/GaN HEMTs », IEEE Trans. Electron Devices, vol. 52, nº 10, p. 2117-2123, oct. 2005, doi: 10.1109/TED.2005.856180.

[7] C.-H. Chen et al., « The causes of GaN HEMT bell-shaped transconductance degradation », Solid-State Electronics, vol. 126, p. 115-124, déc. 2016, doi: 10.1016/j.sse.2016.09.005.

[8] J. Du et al., « Study on transconductance non-linearity of AlGaN/GaN HEMTs considering acceptor-like traps in barrier layer under the gate », Solid-State Electronics, vol. 115, p. 60-64, janv. 2016, doi: 10.1016/j.sse.2015.10.008.

[9] G. Meneghesso et al., « Trapping phenomena in AlGaN/GaN HEMTs: a study based on pulsed and transient measurements », Semicond. Sci. Technol., vol. 28, nº 7, p. 074021, juill. 2013, doi: 10.1088/0268-1242/28/7/074021.

[10] D. S. Lee et al., « Nanowire Channel InAlN/GaN HEMTs With High Linearity of $g_{\rm m}$ and $f_{\rm T}$ », IEEE Electron Device Lett., vol. 34, nº 8, p. 969-971, août 2013, doi: 10.1109/LED.2013.2261913.

[11] K. Shinohara et al., « GaN-Based Field-Effect Transistors With Laterally Gated Two-Dimensional Electron Gas », IEEE Electron Device Lett., vol. 39, nº 3, p. 417-420, mars 2018, doi: 10.1109/LED.2018.2797940.

[12] W. Choi, V. Balasubramanian, P. M. Asbeck, et S. A. Dayeh, « Linearity by Synthesis: An Intrinsically Linear AlGaN/GaN-on-Si Transistor with OIP3/(F-1)P $_{DC}$ of 10.1 at 30 GHz », in 2020 Device Research Conference (DRC), Columbus, OH, USA: IEEE, juin 2020, p. 1-2. doi: 10.1109/DRC50226.2020.9135184.

[13] P. Wang et al., « Influence of Fin-Like Configuration Parameters on the Linearity of AlGaN/GaN HEMTs », IEEE Trans. Electron Devices, vol. 68, nº 4, p. 1563-1569, avr. 2021, doi: 10.1109/TED.2021.3062561.

[14] P. Sung Park, D. N. Nath, S. Krishnamoorthy, et S. Rajan, « Electron gas dimensionality engineering in AlGaN/GaN high electron mobility transistors using polarization », Applied Physics Letters, vol. 100, nº 6, p. 063507, févr. 2012, doi: 10.1063/1.3685483.

[15] S. H. Sohel et al., « Linearity Improvement With AlGaN Polarization- Graded Field Effect Transistors With Low Pressure Chemical Vapor Deposition Grown SiN $_x$ Passivation », IEEE Electron Device Lett., vol. 41, nº 1, p. 19-22, janv. 2020, doi: 10.1109/LED.2019.2951655.

[16] S. H. Sohel, S. Bajaj, T. Razzak, D. J. Meyer, et S. Rajan, « Design of Graded AlGaN Channel Transistors for Improved Large-Signal Linearity ».

[17] S. Rajan, S. P. DenBaars, U. K. Mishra, H. (Grace) Xing, et D. Jena, « Electron mobility in graded AlGaN alloys », Applied Physics Letters, vol. 88, nº 4, p. 042103, janv. 2006, doi: 10.1063/1.2165190.

[18] D. Jena et al., « Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys », Applied Physics Letters, vol. 81, nº 23, p. 4395-4397, déc. 2002, doi: 10.1063/1.1526161.

[19] S. Bajaj et al., « Graded AlGaN Channel Transistors for Improved Current and Power Gain Linearity », IEEE Trans. Electron Devices, vol. 64, nº 8, p. 3114-3119, août 2017, doi: 10.1109/TED.2017.2713784.

[20] H. Luo, W. Hu, et Y. Guo, « On large-signal modeling of GaN HEMTs: past, development and future », Chip, vol. 2, nº 3, p. 100052, sept. 2023, doi: 10.1016/j.chip.2023.100052.

[21] N. C. Miller et al., « An ASM-HEMT for Large-Signal Modeling of GaN HEMTs in High-Temperature Applications », IEEE J. Electron Devices Soc., vol. 11, p. 531-538, 2023, doi: 10.1109/JEDS.2023.3320580.

[22] P. Beleniotis, C. Zervos, S. Krause, S. Chevtchenko, D. Ritter, et M. Rudolph, « Investigation of Traps Impact on PAE and Linearity of AlGaN/GaN HEMTs Relying on a Combined TCAD–Compact Model Approach », IEEE Trans. Electron Devices, vol. 71, nº 6, p. 3582-3589, juin 2024, doi: 10.1109/TED.2024.3388386.

[23] N. C. Miller, M. Elliott, R. Gilbert, E. Arkun, et D. J. Denninghoff, « Surmounting W-band Scalar Load-Pull Limitations Using the ASM-HEMT Model for Millimeter-Wave GaN HEMT Technology Large-Signal Assessment », in 2022 99th ARFTG Microwave Measurement Conference (ARFTG), Denver, CO, USA: IEEE, juin 2022, p. 1-4. doi: 10.1109/ARFTG54656.2022.9896585.

[24] W. Grabinski, B. Nauwelaers, et D. Schreurs, Éd., Transistor level modeling for analog/RF IC design. Dordrecht: Springer, 2006.

[25] I. Angelov, H. Zirath, et N. Rosman, « A new empirical nonlinear model for HEMT and MESFET devices », IEEE Trans. Microwave Theory Techn., vol. 40, nº 12, p. 2258-2266, déc. 1992, doi: 10.1109/22.179888.

[26] I. Angelov, L. Bengtsson, et M. Garcia, « Extensions of the Chalmers nonlinear HEMT and MESFET model », IEEE Trans. Microwave Theory Techn., vol. 44, nº 10, p. 1664-1674, oct. 1996, doi: 10.1109/22.538957.

[27] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, et H. Zirath, « An Empirical Table-Based FET Model », IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, vol. 47, nº 12, 1999.

[28] I. Angelov et al., « Large-signal modelling and comparison of AlGaN/GaN HEMTs and SiC MESFETs », in 2006 Asia-Pacific Microwave Conference, Yokohama, Japan: IEEE, déc. 2006, p. 279-282. doi: 10.1109/APMC.2006.4429422.

[29] J.-S. Moon et al., « 360 GHz f_{MAX} Graded-Channel AlGaN/GaN HEMTs for mmW Low-Noise Applications », IEEE Electron Device Lett., vol. 41, nº 8, p. 1173-1176, août 2020, doi: 10.1109/LED.2020.3005337.

[30] J. S. Moon et al., « High-speed graded-channel AlGaN/GaN HEMTs with power added efficiency >70% at 30 GHz », Electron. lett., vol. 56, nº 13, p. 678-680, juin 2020, doi: 10.1049/el.2020.0281.

[31] J. Moon et al., « Highly-Linear and Efficient mm-Wave GaN HEMT Technology », 2022.

[32] J. Moon et al., « Ultra-Linear and High-Efficiency GaN Technology for 5G and Beyond », in 2022 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), Las Vegas, NV, USA: IEEE, janv. 2022, p. 5-7. doi: 10.1109/PAWR53092.2022.9719870.

[33] J.-S. Moon et al., « W -Band Graded-Channel GaN HEMTs With Record 45% Power-Added-Efficiency at 94 GHz », IEEE Microw. Wireless Tech. Lett., vol. 33, nº 2, p. 161-164, févr. 2023, doi: 10.1109/LMWC.2022.3207978.

[34] J. Moon et al., « Novel High-speed Linear GaN Technology with High Efficiency », in 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA: IEEE, juin 2019, p. 1130-1132. doi: 10.1109/MWSYM.2019.8700832.

[35] J.-S. Moon et al., « Power Scaling of Graded-Channel GaN HEMTs With Mini-Field-Plate T-gate and 156 GHz f_T », IEEE Electron Device Lett., vol. 42, nº 6, p. 796-799, juin 2021, doi: 10.1109/LED.2021.3075926.

[36] P. H. Drive et S. Clara, « DEVICE SIMULATION SOFTWARE ».

[37] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, et K. F. Brennan, « Electron transport characteristics of GaN for high temperature device modeling », Journal of Applied Physics, vol. 83, nº 9, p. 4777-4781, mai 1998, doi: 10.1063/1.367269.

[38] M. Farahmand et al., « Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries », IEEE Trans. Electron Devices, vol. 48, nº 3, p. 535-542, mars 2001, doi: 10.1109/16.906448.

[39] « ADS 2009, Nonlinear Devices », 2009.

[40] R. Tinti, « Dr. Ilcho Angelov Associate Professor Microwave Electronics Lab Department of Microtechnology and Nanoscience Chalmers University Goteborg Sweden ».

[41] Z. Zhao et al., « High Precision Model by Error Compensation Method based on the Angelov Model », in 2019 16th China International Forum on Solid State Lighting & 2019 International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS), Shenzhen, China: IEEE, nov. 2019, p. 63-66. doi: 10.1109/SSLChinaIFWS49075.2019.9019772.

[42] C. Wang et al., « An Electrothermal Model for Empirical Large- Signal Modeling of AlGaN/GaN HEMTs Including Self-Heating and Ambient Temperature Effects », IEEE Trans. Microwave Theory Techn., vol. 62, nº 12, p. 2878-2887, déc. 2014, doi: 10.1109/TMTT.2014.2364821.

[43] H. Luo, H. Zhang, W. Hu, et Y. Guo, « A simplification method for capacitance models in AlGaN / GaN high electron mobility transistors under large drain voltage using channel analysis », Int J RF Microw Comput Aided Eng, vol. 31, nº 1, janv. 2021, doi: 10.1002/mmce.22489.

[44] S. Emekar et al., « Modified angelov model for an exploratory GaN-HEMT technology with short, few-fingered gates », in 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Kamakura: IEEE, sept. 2017, p. 117-120. doi: 10.23919/SISPAD.2017.8085278.

[45] « Keysight Knowledge Center, “Appendix A - Parameters ». [En ligne]. Disponible sur: https://iccap.2023/doc/angelov/Appendix_A_-_Angelov GaN_Parameters_and_Equivalent_circuit.htlm

[46] « Keysight Knowledge Center, “Appendix B - Extraction flow ». [En ligne]. Disponible sur: http://iccap.2023/doc/angelov/Appendix_B_-_Parameter-Extraction_functions.html

[47] « Keysight documentation - ICCAP - Using the tool ».

[48] « Keysight documentation - ICCAP - Example Flow of Angelov-GaN Toolkit ».

[49] S. Long, « Harmonic Balance Simulation on ADS ».

[50] « Agilent Technologies: Harmonic Balance for Large Signal AC and S-parameter Simulation ».

[51] N. Venkatesan, J.-S. Moon, et P. Fay, « Electric Field Engineering in Graded-Channel GaN-Based HEMTs », in 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA: IEEE, déc. 2021, p. 1-4. doi: 10.1109/BCICTS50416.2021.9682456.

Chapter 3: Towards ultrathin Al-rich barrier layer devices: Study of AlGaN and AlN/GaN HEMTs for millimeter-wave applications

I. Introduction

As presented in the previous sections, considerable efforts are being made to improve GaN technology in millimeter-wave range. By shrinking the gate length down to 100 nm and below along with epitaxy and process engineering, attractive performances have been achieved. However, at these frequencies, the combination of high efficiency and output power density with proven reliability is still limited by thermal management, gate degradation, trapping effects, or the degradation of the electron confinement. **Figure 3.1** recalls some major challenges, ranging from the epitaxial structure to device fabrication which need to be addressed to unlock next generation RF GaN devices. In this chapter, we investigated two different types of structures from the following suppliers: SOITEC and SweGaN. The main objective of these studies is to provide insights on next generation GaN technology for millimeter-wave applications. The technology must be able to operate up to V_{DS} = 20V with a high PAE and a suitable P_{OUT} while demonstrating promising reliability. For that, we will present first the processing steps involved in the fabrication of these GaN HEMTs.

The chapter will be then divided into two sub-sections. The first involves the study of HEMTs fabricated on layers supplied by SOITEC. In brief, these devices correspond to AlN/GaN transistors with a carbon doped AlGaN back-barrier. We will review the background of this technology in our research group and the results achieved during this PhD work. The impact of carbon in the AlGaN back barrier is investigated as well supported by TCAD simulations. The second part concerns the fabrication of GaN HEMTs supplied by SweGaN. The study focuses on QuanFINE®, so called AlGaN/GaN buffer-free HEMTs.

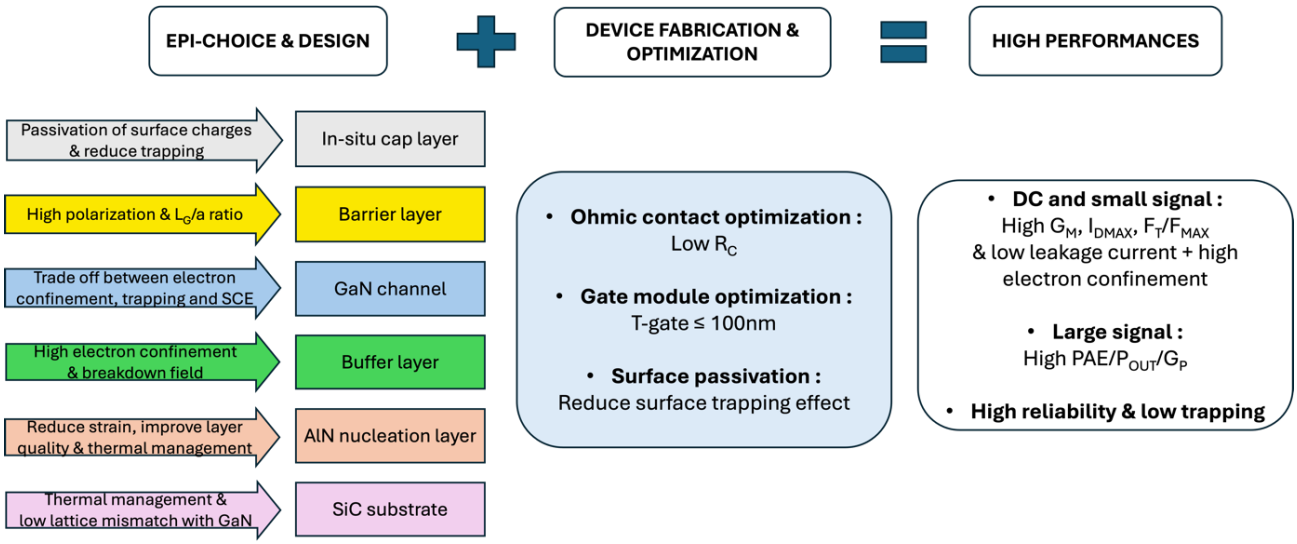


Figure 3.1. Schematic process from epitaxy to device showing the requirements to achieve high RF performances.

II. Process fabrication

II.1. Mask layout

Figure 3.2 shows the complete schematic design of the so-called "GaN FAST" mask layout used in this work. This layout consists of three steps of e-beam lithography (alignment marks, ohmic contacts and gate module) and two optical photolithography (isolation and pads) steps. E-beam lithography is needed for the high resolution of the critical patterns, such as the short gate lengths. However, it can be pointed out this technique is time consuming.

The “GaN FAST” mask includes a variety of process control monitor patterns (PCMs), and different transistor designs. At the bottom of the mask, there are several PCMs that are used to evaluate the electrical parameters of the epitaxial structure and to control the process quality. For instance, TLM patterns are implemented to measure the ohmic contact resistances. Hall patterns are used to assess the 2DEG characteristics such as the electron mobility, density and sheet resistance of the heterostructure whereas circular diodes are used to evaluate the Schottky gate contact. Device isolation is verified by measuring the leakage current flowing through two isolated contacts with various spacing.

Additionally, transmission lines are available to evaluate the RF losses of the epitaxial structure. At the top of the mask, there are eight columns of transistors, offering three different gate width: 2×25 µm, 2×50 µm and 2×100 µm. In each column, four HEMTs, containing two gate fingers with L_G ranging from 500 nm to 100 nm. L_{GD} varies between 0.5 µm, 1.5 µm and 2.5 µm, while L_{GS} remains constant at 0.5 µm. It is important to note that in this mask we made the choice to have several gate lengths in order to better understand the processing and epi-design dependence on the electrical performances.

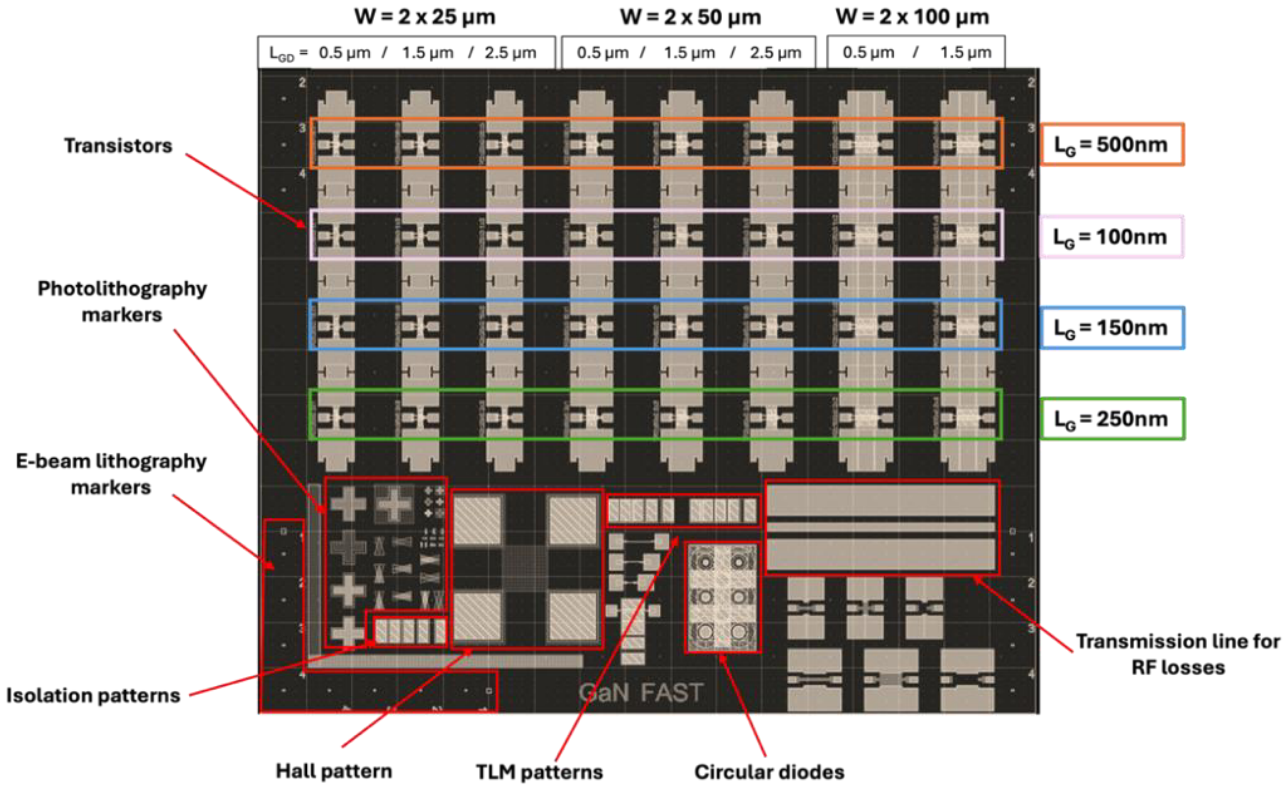


Figure 3.2. Single cell layout mask "GaN FAST" for e-beam GaN HEMT fabrication replicating across the samples.

II.2. Fabrication steps

The transistors were fabricated using the IEMN's clean room facilities. Although the structures investigated are quite different, the process is relatively similar. However, specific adjustments are made with respect to the epi-stack. The process flow is illustrated in **Figure 3.3**. We will describe each step in more detail in the following sections. It is important to note that before starting, the received wafers are diced into 2.5 cm × 2.5 cm coupons.

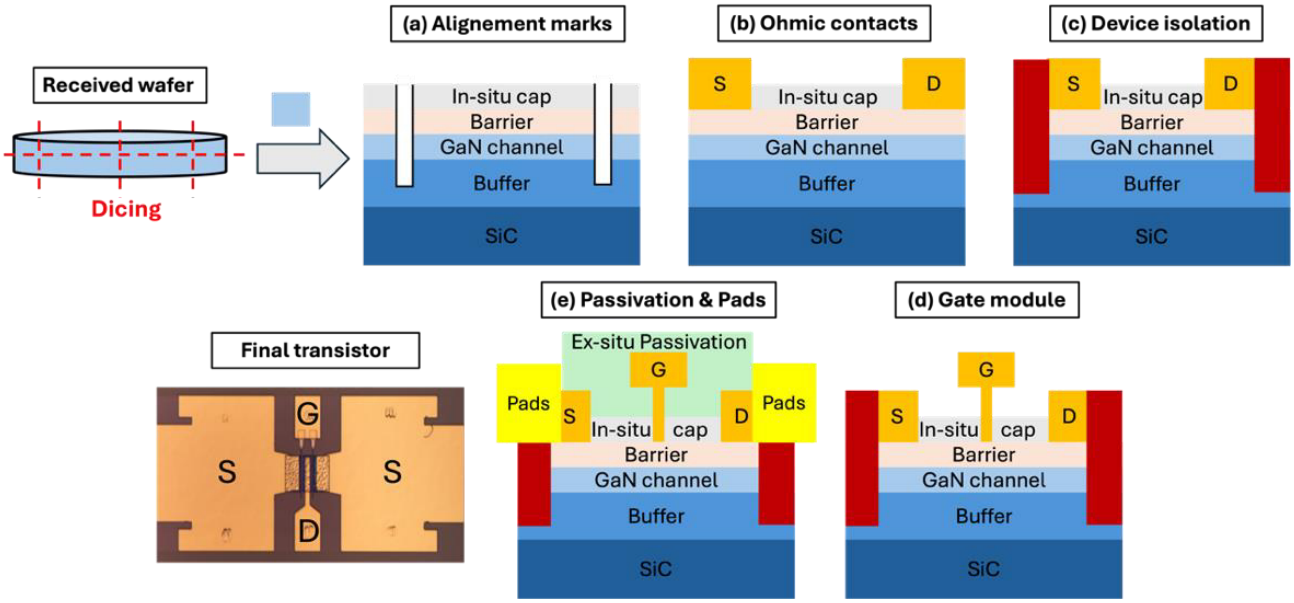


Figure 3.3. (a-e) E-beam process flow performed during this thesis-work.

II.2.a. Alignment marks

Mark patterns are mandatory to accurately align the different fabrication steps. The first mark set are used as reference for subsequent patterns. The marks can be either etched or metallized. In our case, etched marks are used to prevent poor surface roughness of the metal and delamination after the ohmic contact annealing step. **Figure 3.4** details the alignment mark fabrication.

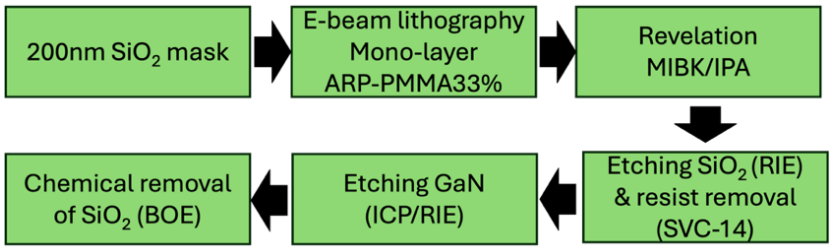


Figure 3.4. Main process flow for alignment marks.

The process begins with the deposition of 200nm of SiO2 by Plasma-Enhanced Chemical Vapor Deposition (PECVD), which serves as a sacrificial layer to protect the sample. Then, a single layer of e-beam resist (ARP PMMA 33%) is applied.

After pattern revelation, the SiO_2 mask is etched by reactive ion etching (RIE) with SF_6 plasma. The proper etching of SiO2 is controlled with a profilometer and the resist is removed with an SVC-14 solution. Then, Inductively Coupled Plasma (ICP) based on Cl_2/Ar plasma is used to etch the marks to a depth of 350-400 nm, ensuring sufficient contrast for subsequent writing levels. The final patterns are controlled using SEM analysis, as shown in **Figure 3.5**. Finally, the remaining SiO_2 is removed through a HF-based solution (BOE 7:1).

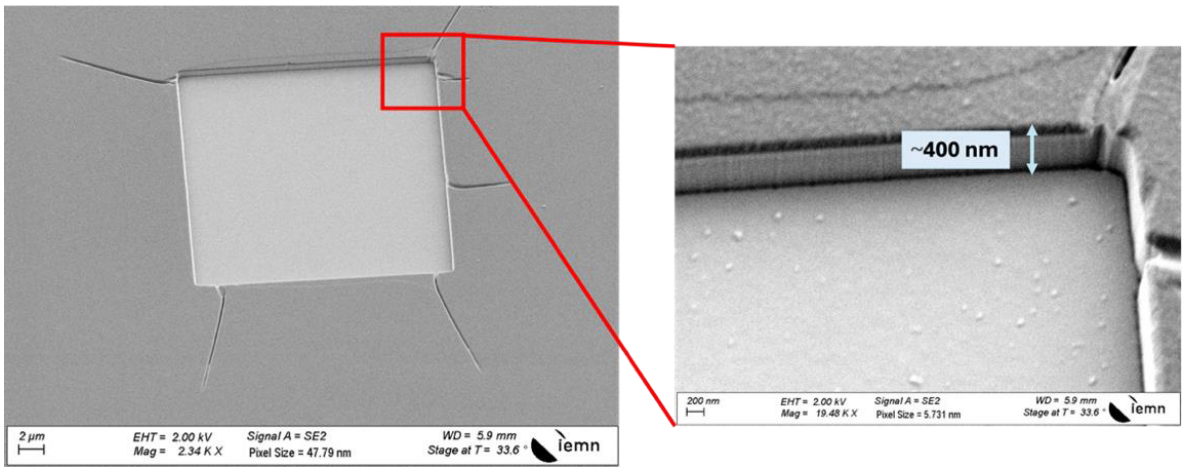


Figure 3.5. Tilted SEM image of an alignment mark.

II.2.b. Ohmic contacts

The second step involves the fabrication of ohmic contacts targeting the lowest possible contact resistances (R_C). A low contact resistance ensures maximum drain current, low on-resistance, high transconductance and consequently high frequency performance Ft/Fmax. However, achieving low R_C on GaN-based materials can be difficult due to the wide bandgap, which naturally favors Schottky-type contacts. Several factors influence the optimum contact value, such as the work function, the thickness and composition of the metal stack, the annealing temperature and time, the barrier layer thickness or the surface treatments [1-6]. Limiting the lateral diffusion of metal by getting sharp edge acuity and rather smooth surface morphology are also crucial to prevent additional parasitic capacitances, short circuits. **Figure 3.6** shows the key steps in the fabrication of ohmic contacts.

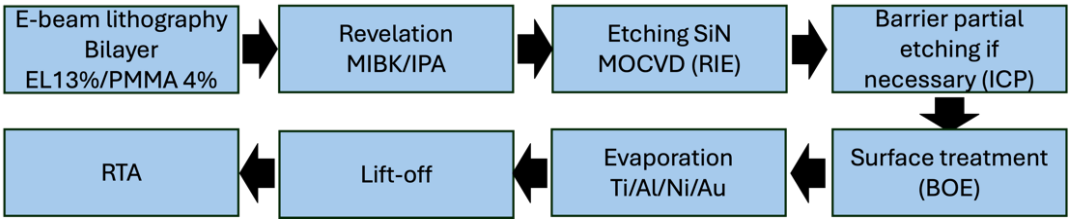


Figure 3.6. Main process flow for ohmic contacts.

The process begins with e-beam lithography using an EL13%/PMMA4% bilayer. After development, the in-situ MOCVD SiN cap layer is etched by RIE using SF_6 plasma. All the structures studied in this work include indeed an in-situ SiN cap, which is locally etched below the contacts. If the SiN cap is not properly etched, contacting the 2DEG becomes difficult, leading to significantly increased contact resistances. Additionally, after RTA, uncontrolled lateral etching can cause metal diffusion towards the SiN interface. To address this, the SiN is deliberately laterally over-etched to ensure that the SiN sidewalls are separated from the metal stack by at least 100 nm. **Figure 3.7** shows an SEM image of an ohmic contact post-annealing. The image demonstrates controlled lateral etching with good surface morphology, precise edge definition, and no lateral diffusion of the metal. Conversely, if the SiN MOCVD is completely laterally etched, the active area between the two contacts is unprotected and thus subjected to contaminations or trapping. **Figure 3.8** presents two examples of undesired SiN over-etching resulting in an unprotected active surface (a) and lateral diffusion of the metal after annealing (b).

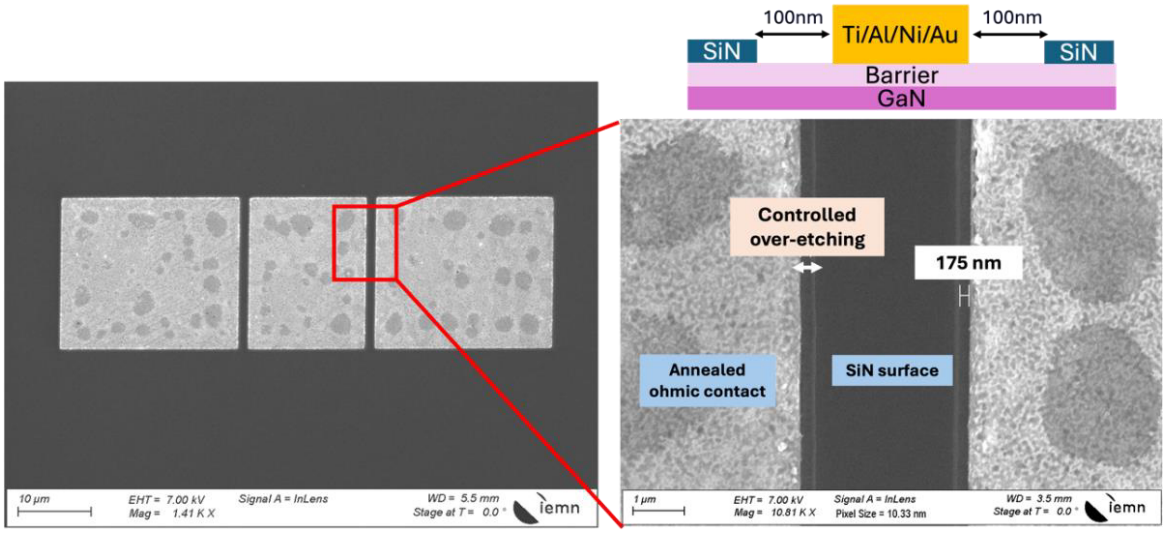


Figure 3.7. SEM image of ohmic contact after annealing with a zoom showing controlled SiN etching.

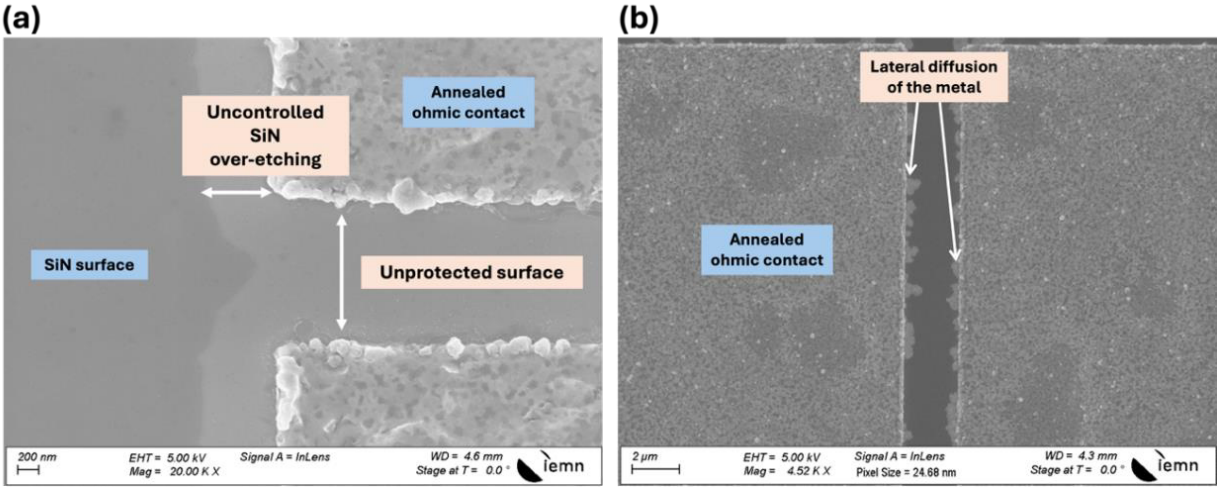


Figure 3.8. (a) SEM image showing an uncontrolled SiN over-etching between two contacts and (b) SEM image illustrating a lateral diffusion of the metal post-annealing.

Subsequently, partial etching or surface treatment of the barrier (depending on the barrier thickness) is performed using BCl_3/SF_6 plasma to reduce the distance between the metal and the 2DEG. A chemical deoxidation with BOE solution is added prior to the metallization step to prevent the formation of a native oxide after the ICP etching step. Evaporation of Ti/Al/Ni/Au stack (12/200/40/100nm) is then carried out, which has been optimized previously within our group. Titanium (Ti) acts as an adhesion layer and reacts with GaN during rapid thermal annealing (RTA) to form a TiN alloy at the metal/semiconductor interface. This alloy induces nitrogen vacancies in the barrier layer, which acts as shallow donors, increasing carrier injection into the 2DEG and enhancing the channel conductivity [4, 7-10]. The deposition of an aluminum (Al) layer forms a Ti-Al alloy which reduces the reactivity between Ti and GaN [5, 11, 12]. This reduction limits the formation of voids at the interface caused by gallium migration, which would otherwise increase the contact resistance. To prevent the diffusion of gold (Au) into the Al/Ti layers, which could compromise the contact, a layer of nickel (Ni) is deposited. The entire metal stack is capped with a layer of gold, known for its excellent electrical interconnection properties, to ensure uniform current distribution and to prevent oxidation of the metal stack. Finally, after lift-off, a rapid thermal annealing (RTA) process is performed, inducing alloy formation, thus lowering the contact resistance [2, 13, 14]. The quality of ohmic contacts can be evaluated using Transmission Line Method (TLM) patterns, as shown in **Figure 3.9.a**.

These patterns consist of rectangular metal contacts with varying spacings of 2µm (d_0), 5µm (d_1), 10µm (d_2) and 20µm (d_3). W is the width of the contact and L the contact length. I-V measurements are then performed with two-probes, sweeping the voltage from -10V to +10V. **Figure 3.9.b** shows the current density measured between two contacts with a spacing of 2 µm. The black curve displays a non-ohmic behavior, characterized by an inflexion point while the blue curve exhibits an ohmic behavior. In addition, four-probe measurements can be used to determine the contact resistance (R_C). In this method, the total resistance is measured between two adjacent contacts, with current flowing through the semiconductor from one contact to another. The total resistance R_T of a metal-semiconductor contact is the sum of the resistances associated with each distance, as given by:

$$R_T = 2\,\frac{R_c}{W} + \frac{R_{sheet}}{W} \times d \qquad (19)$$

with R_C as the contact resistance and R_{sheet} as the sheet resistance of the semiconductor.

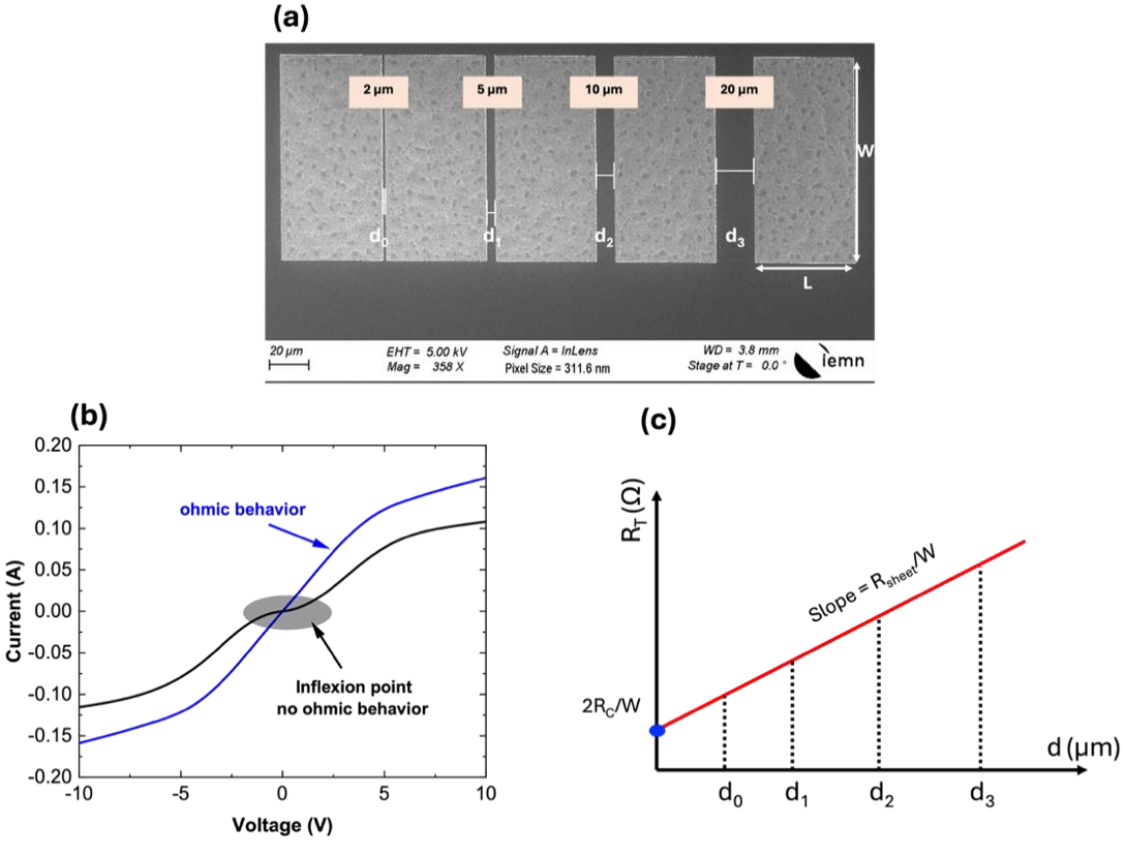


Figure 3.9. (a) SEM image of TLM patterns, (b) example of ohmic and non-ohmic characteristics and (c) total resistance as a function of contact spacing d.

Contact resistance can then be extracted with a linear regression analysis of total resistance versus contact spacing (dx), as shown in **Figure 3.9.c**. The slope of the linear fit gives R_{sheet}, while the y-intercept provides R_C.

In this thesis work, two different barriers are studied, both with Al-rich and ultra-thin sub-10 nm thickness. The first one is an AlN barrier (from SOITEC), while the second one is an AlGaN barrier (from SweGaN). For the AlN structures, the ohmic contacts are formed directly on top of the barrier layer after the SiN cap etching, without additional recess of the barrier, as illustrated in **Figure 3.10.a**. The R_C is directly dependent on the annealing temperature that we tuned to reduce the contact resistance as much as possible. (**Figure 3.10.b**). The lowest value obtained is 0.35 Ω.mm with an RTA at 850°C.

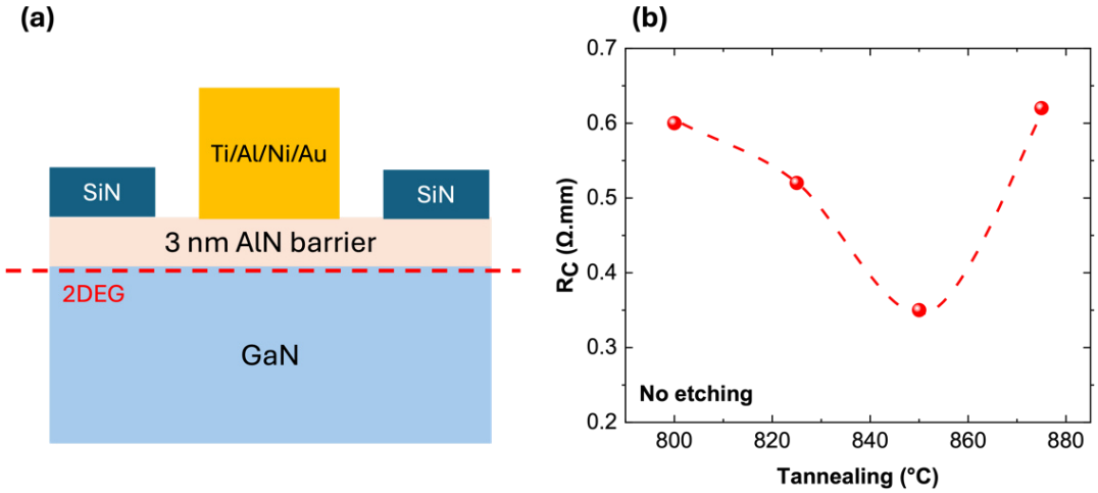


Figure 3.10. (a) Schematic of non-recessed Ti/Al/Ni/Au ohmic contacts on ultra-thin AlN barrier and (b) evolution of R_C as a function of annealing temperature.

For the AlGaN structures, an additional treatment is added after the SiN etching. To reduce the resistance of the ohmic contacts, partial recess of the barrier is performed prior to metallization using a BCl_3/SF_6 plasma. This etch step is necessary to bring the metal stack closer to the 2DEG conduction channel without degrading the GaN layer (**Figure 3.11.a)**. For this purpose, different etching rates for the AlGaN barrier were tested. **Figure 3.11.b** shows the evolution of the R_C as a function of etching time with an RTA fixed at 850°C. The best R_C achieved is 0.43 Ω.mm. Further etching and temperature adjustments are still required to reduce R_C to 0.3 Ω.mm. However, the contact quality is sufficient for the study.

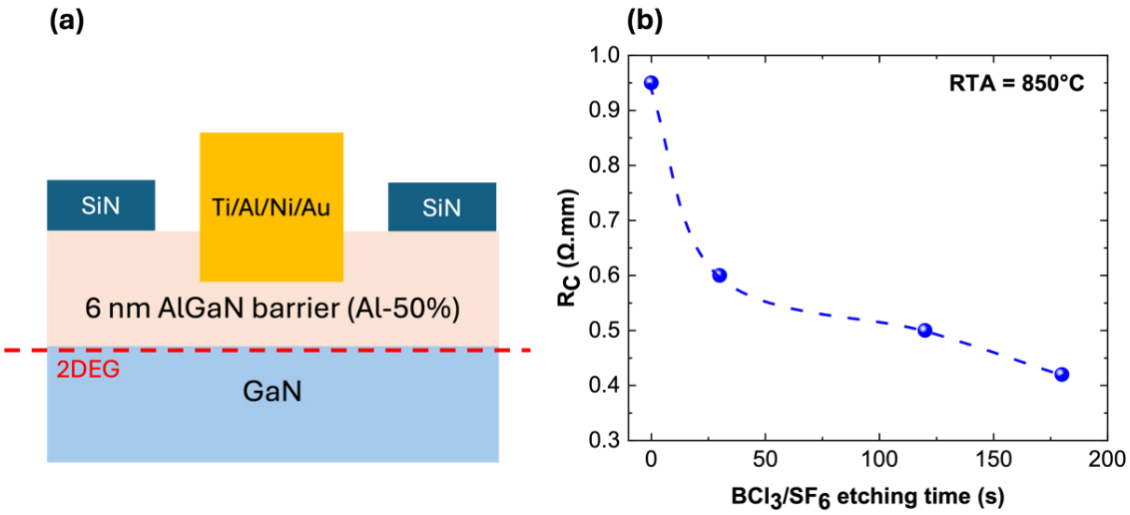


Figure 3.11. (a) Partial-recess of Ti/Al/Ni/Au ohmic contacts on ultra-thin AlGaN barrier and (b) contact resistance R_C as function of BCl_3/SF_6 etching time (RTA = 850°C).

II.2.c. Device isolation

Device isolation is an important step, as it precisely defines the active area of each transistor, providing an optimal path for electrons between source and drain contacts. The process should isolate efficiently, minimizing leakage currents between neighboring transistors. The boundary is established by isolating the 2DEG and the underlying region, typically a few hundred nanometers. The isolation can be performed through two main methods: deep etching using ICP (mesa) or ion implantation using species such as Argon, Nitrogen, Helium, or Oxygen. In our case, N^+ implantation (w/o post-annealing) was used with energy and implantation doses properly optimized in the past. The crystalline structure is thereby broken, and the semiconductor becomes amorphous, preventing parasitic conduction. **Figure 3.12** shows the key steps for device isolation.

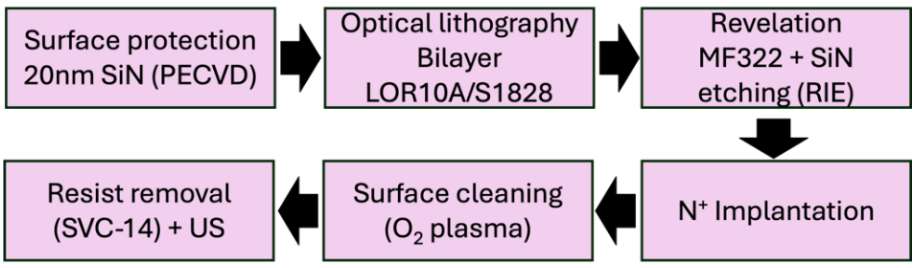


Figure 3.12. Main process flow for device isolation.

First, a SiN layer (20 nm) is deposited by PECVD to protect the surface as initial passivation to reduce the surface leakage and trapping effects. We used optical photolithography with an S1828/LOR10A bilayer. This step does not require the precision of e-beam writing as the patterns and related distances are rather large. It can be performed with a hard mask saving time and cost. After patterning, the SiN PECVD is etched by RIE and N+ implantation is performed to isolate the contacts. Three doses with different energies are used: (1) 20 KeV - 0.25×10^{14} at/cm^2, (2) 50 KeV - 1×10^{14} at/cm^2, (3) 100 KeV - 1.5×10^{14} at/cm^2. Then, O_2 plasma, resist removal and ultrasonic treatment are used to clean the surface before starting the gate fabrication. The proper implantation is verified by measuring the current flowing between isolated patterns. The isolation step also allows Hall effect measurements to assess the 2DEG properties such as R_{sheet}, electron mobility and density, using Van der Pauw patterns. **Figure 3.13** shows a SEM image of an ohmic contact after isolation, as well as a typical I-V measurement up to 200V between two isolated patterns (5µm spacing) showing very low leakage current.

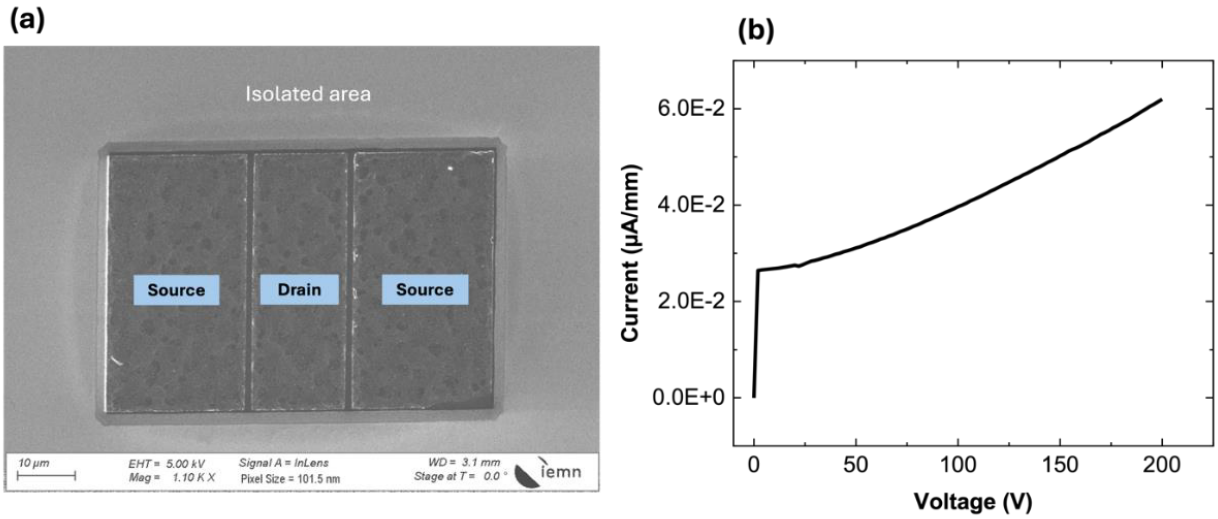


Figure 3.13. (a) Ohmic contacts after isolation and (b) IV measurement between two isolated patterns.

II.2.d. Gate Schottky module

The gate fabrication represents the most critical step in the overall process. To achieve high-frequency performance, it is imperative to reduce the gate length (100 nm or below) to maximize device's performance.

The T-shaped gate footprint is defined by electron-beam lithography to reduce both gate resistance and parasitic capacitance, especially when using a shorter gate length. **Figure 3.14** presents the key steps involved in the gate fabrication.

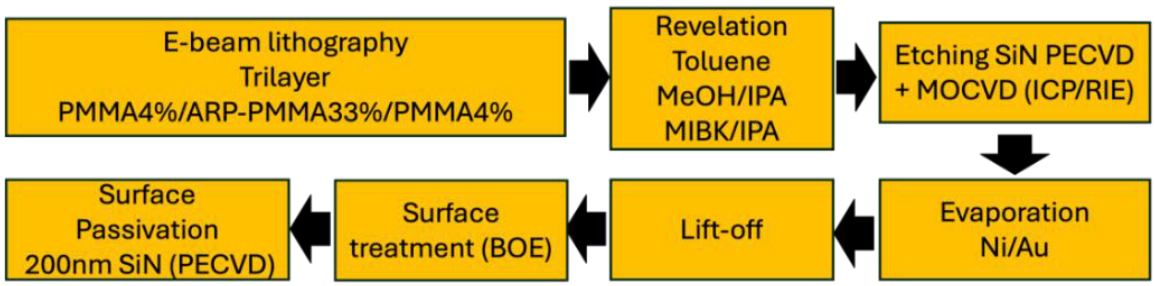


Figure 3.14. Main process flow for gate module fabrication.

The process begins with e-beam lithography using a three-layer PMMA resist. After development, the SiN PECVD and MOCVD layers are etched to define the gate foot. This step is critical to avoid impurities at the gate/barrier interface while maintaining short gate lengths. That is why an anisotropic SiN etching was develop using a highly selective ICP-RIE process with SF_6 plasma. It is important to note that the etching rate is highly sensitive to external factors, such as the cleanliness of the chamber, its preconditioning, and the type / size of substrate used. In order to prevent excessive etching of the resist mask and the SiN MOCVD layer as well as avoiding damages of the barrier layer, we used a low-power RIE etching process. This approach reduces physical etching and favors chemical etching, which is less damaging and limits undesired Fluorine implantation into the barrier layer. In addition, an etch cycle was implemented to achieve uniform etching as the intrinsic temperature is well controlled in this case as opposed to continuous etching. However, with a thick SiN MOCVD layer (6 nm), the increased number of cycles leads to lateral over-etching of the PECVD SiN and the resist that have a substantially different etching rate. **Figure 3.15.a** shows a top SEM view of the pattern after the tri-layer resist development, revealing a 70 nm opening. After four etching cycles, the etched SiN MOCVD dimension expanded to 105 nm, exceeding the original resist pattern opening (**Figure 3.15.b**). Consequently, it is important to systematically optimize the etching cycle number with respect to the SiN thickness of the structure in order to achieve the desired gate dimensions.

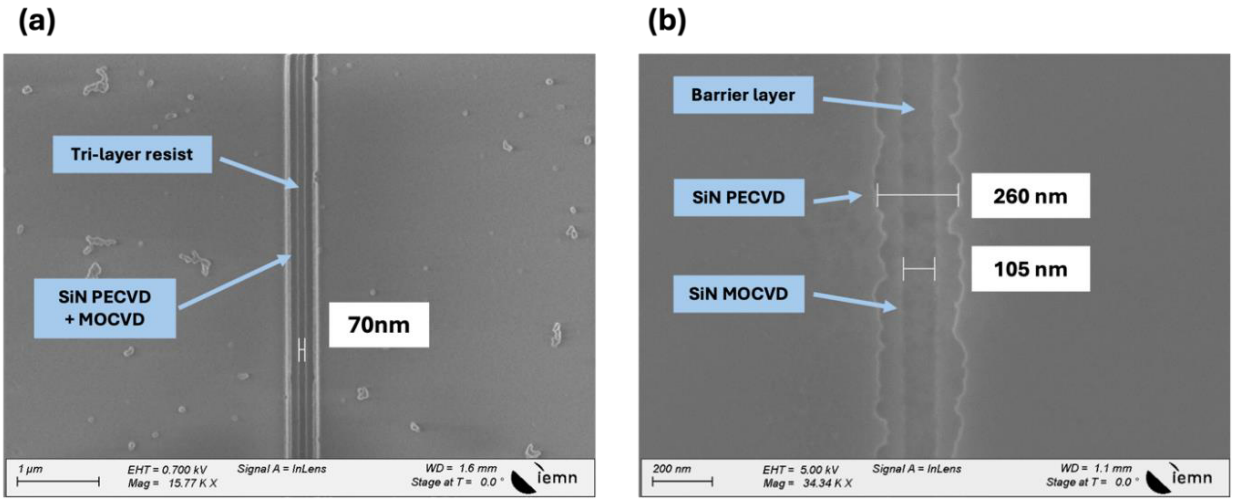


Figure 3.15. (a) Top-view SEM image of the tri-layer resist pattern opening and (b) SiN MOCVD and PECVD etching.

After etching, gate Schottky contacts are formed using Ni/Au (20/400 nm) metal stack by evaporation and T-shape gates are obtained by lift-off. Ni is used for its good bonding properties and ensures a reasonable Schottky barrier height, when deposited on the semiconductor barrier, while Au improves the electrical contact. **Figure 3.16** summarizes the critical steps corresponding to the gate fabrication.

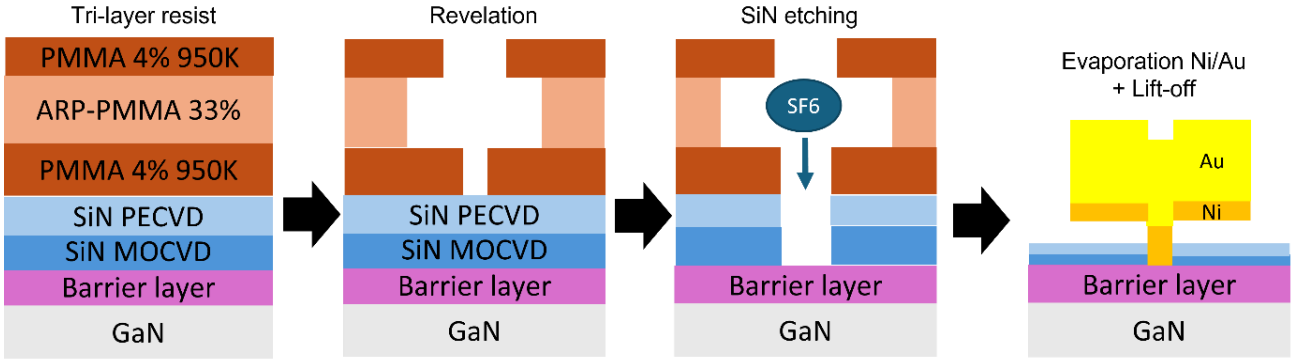


Figure 3.16. Schematic of critical steps of the gate fabrication.

In our e-beam mask, we chose to use several gate lengths to study their impact on device performance. **Figure 3.17** presents SEM images of a transistor at the end of gate fabrication (a), tilted images of all available gate lengths ranging from 100 nm to 500 nm (b-e), and a related FIB cross-section of a 100 nm gate length (f).

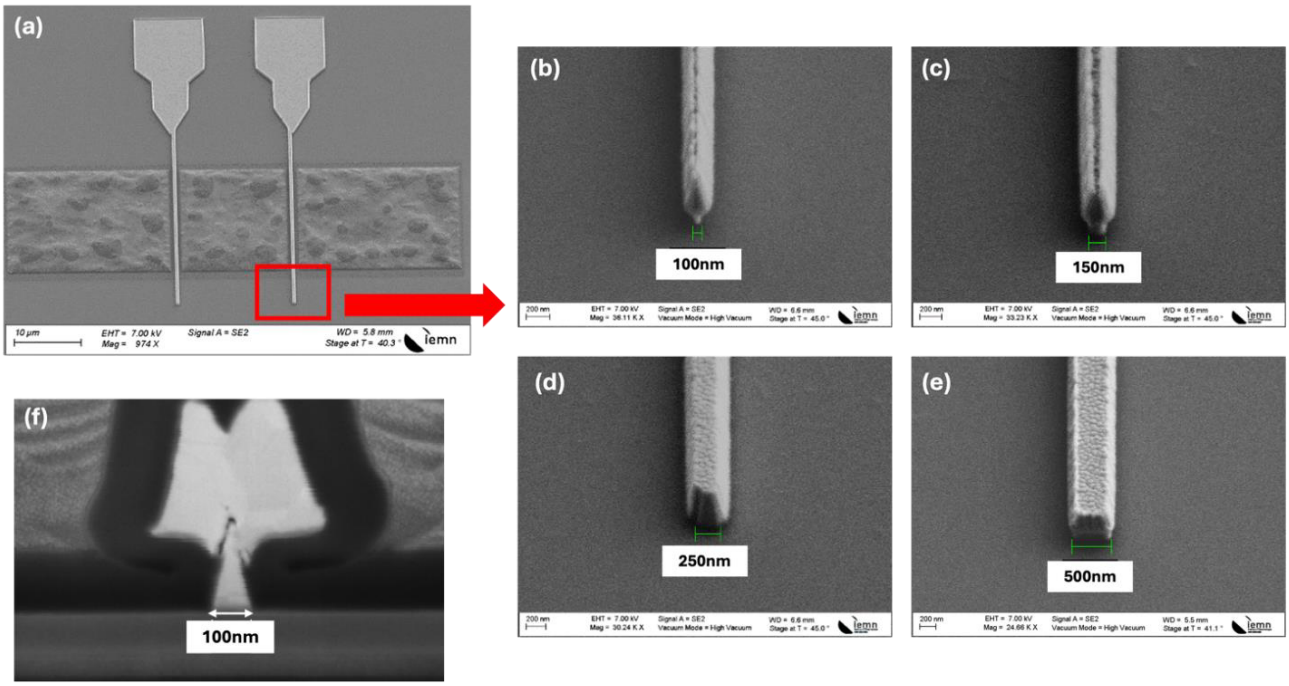


Figure 3.17. (a) SEM image of a transistor after gate fabrication, (b-e) tilted SEM images of gate lengths ranging from 100 nm to 500 nm and (f) corresponding FIB cross-section image of 100 nm gate length.

The process concludes with chemical surface deoxidation (BOE), followed by a final passivation with 200 nm thick SiN deposited by PECVD. The primary role of this passivation is to further mitigate surface states and related trapping effects that may arise from surface dangling atomic bonds, surface growth defects, or plasma-induced damage during processing. It also protects the transistor from external contaminants. The quality of Schottky contacts is evaluated through electrical characterization of circular diodes (**Figure 3.18.a**). Characteristics of 54 µm-diameter diodes with AlN and AlGaN barrier layer are presented in **Figure 3.18.b**. When a positive voltage is applied to the diode (forward bias), the metal/semiconductor Schottky barrier decreases, leading to an exponential increase in current starting from a threshold voltage that corresponds to the barrier height. The threshold voltage for the AlGaN/GaN structures (~+0.9V) is typically lower than that of AlN/GaN structures (~+1.5V), which is attributed to the lower Schottky barrier height with the AlGaN barrier layer.

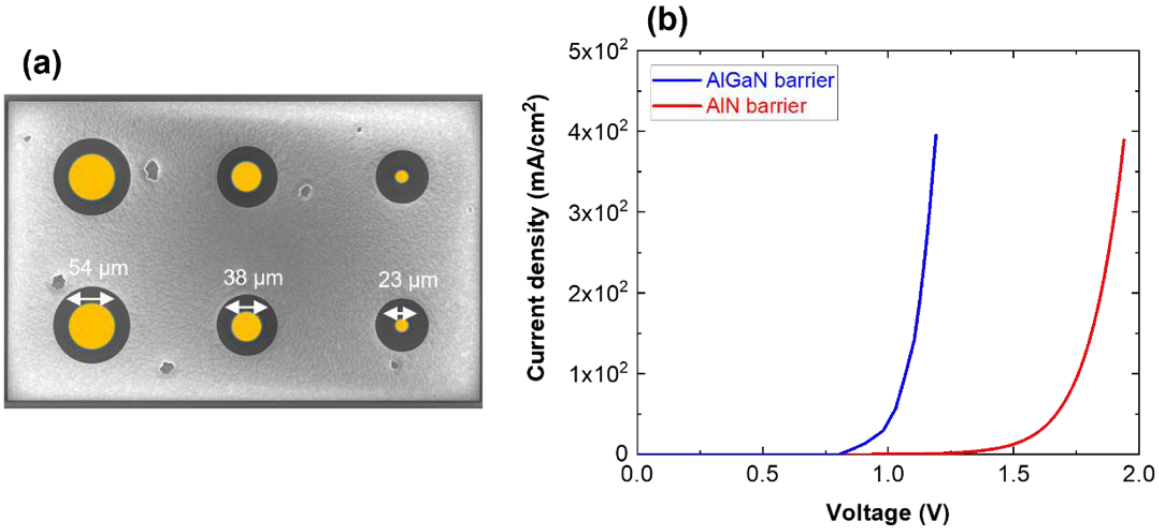


Figure 3.18. (a) SEM image of circular diodes and (b) electrical characteristics of forward-diodes (54 µm diameter) for AlGaN and AlN barriers.

II.2.e. PADS fabrication

The final step in the process is to include the pads, which enable electrical characterization of the device by providing access to the three terminals (gate, source and drain). Optical lithography with ARP53:20 resist is used with a hard mask similar to the isolation step. Afterwards, the SiN PECVD passivation layer is etched by RIE using SF_6 plasma to connect the terminals to the previous metal levels. A Ti/Au metal stack (100/400 nm) is then evaporated, followed by a lift-off process. **Figure 3.19.a** shows the process flow for pads fabrication, while **Figure 3.19.b** an SEM image of the final transistor after lift-off.

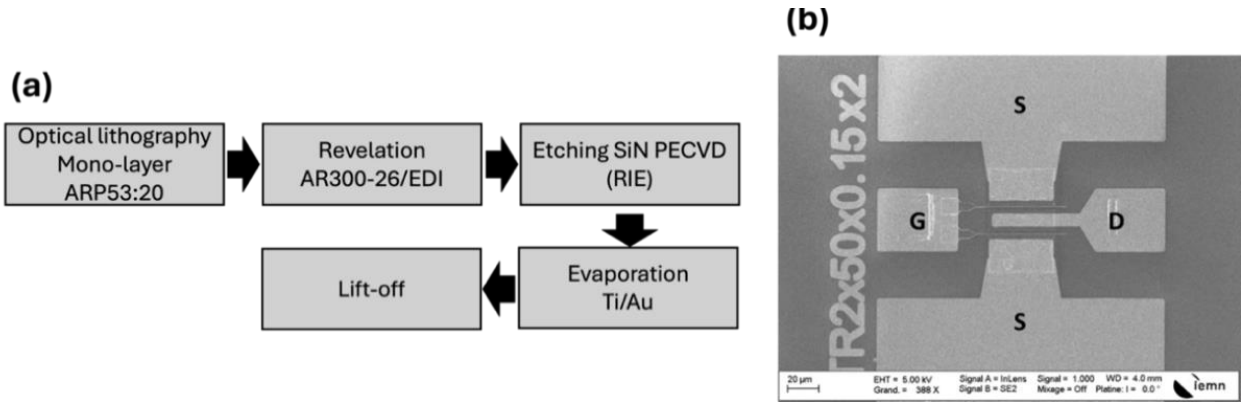


Figure 3.19. (a) Process flow for pads fabrication, (b) SEM image of a 2×50 µm transistor after pads metallization.

III. AlN/GaN/AlGaN back barrier HEMTs

III.1. Introduction and technology background

As discussed in Chapter I, section VI.5, high C-doped AlN/GaN HEMT structures enabled to achieve promising performances at 40 GHz. However, the high carbon concentration (2×10^{19} cm^{-3}) in the GaN buffer with 100 nm GaN channel thickness induced trapping effects, resulting in a rather large gap in performances between CW and pulsed mode. For short sub-150 nm gate length GaN devices, reducing or moving the carbon away from the 2DEG with a thicker GaN channel to mitigate trapping is not a good solution as it will impact the electron confinement and thus increase the drain leakage current. Therefore, to address this challenge, the insertion of a thin AlGaN back barrier between the GaN channel and the C-doped GaN buffer has emerged as a potential solution to reduce trapping effects while maintaining excellent electron confinement. It is important to note that the C-doped AlN-based HEMTs (w/o AlGaN back barrier) have been extensively developed in our research group during the PhD thesis of Kathia Harrouche: "*Design and fabrication of GaN-based field effect power transistors up to W-band, 2021*" [15] **Figure 3.19** summarizes the advantages/disadvantages of the C-doped AlN/GaN HEMTs and the remaining challenges of the AlN/GaN/AlGaN back barrier HEMTs.

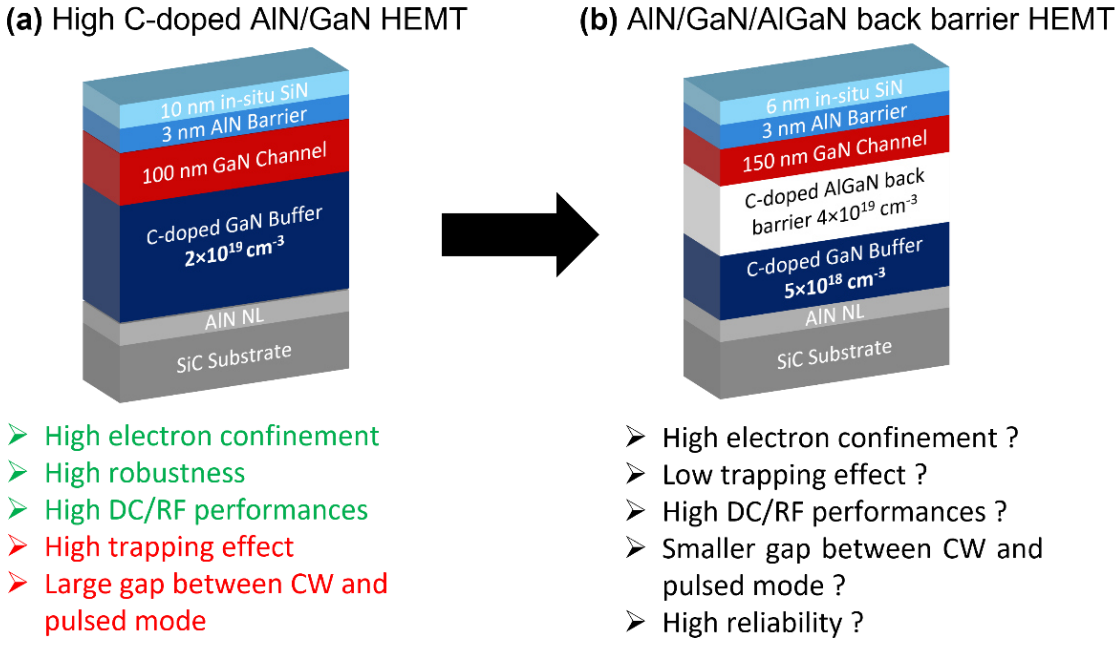


Figure 3.19. Challenges and key features of (a) C-doped AlN/GaN and (b) AlN/GaN/AlGaN back barrier HEMTs.

The AlGaN back barrier structure consists of a 1 µm C-doped (5×10^{18} cm^{-3}) GaN buffer layer, followed by a 100 nm thick, highly C-doped (5×10^{19} cm^{-3}) AlGaN layer, a 150 nm thick undoped GaN channel with an ultra-thin 3 nm thick AlN barrier layer, capped with a 6 nm thick SiN layer. The main concern for this structure was to determine the optimum Al content in the back barrier to provide a sufficient back polarization, ensuring a proper electron confinement under high electric field, a low leakage current, and preventing short-channel effects in sub-150 nm devices. The second point of interest was to examine whether a high carbon concentration within the AlGaN back barrier is a source of trapping effects within the heterostructure.

III.2. Impact of the Al-content in the AlGaN back barrier

To carry out this study, 3 structures were grown by MOCVD with an Al-content in the AlGaN back barrier ranging from 10% to 25%. **Figure 3.20** presents the structures with their associated 2DEG properties, which are quite similar for all structures with an electron mobility (µ) between 870 to 975 $cm^2/V.s$ and an electron density (n_S) of 2.1-2.3×10^{13} cm^{-2}. To investigate the impact of the Al-content on these structures, an e-beam process has been applied using various gate lengths. **Figure 3.21** presents the DC (DIBL, I_DV_D) and DC-pulsed characteristics of 2×50 µm transistors with L_G = 250 nm (red), 100 nm (blue) and L_{GD} = 0.5 µm.

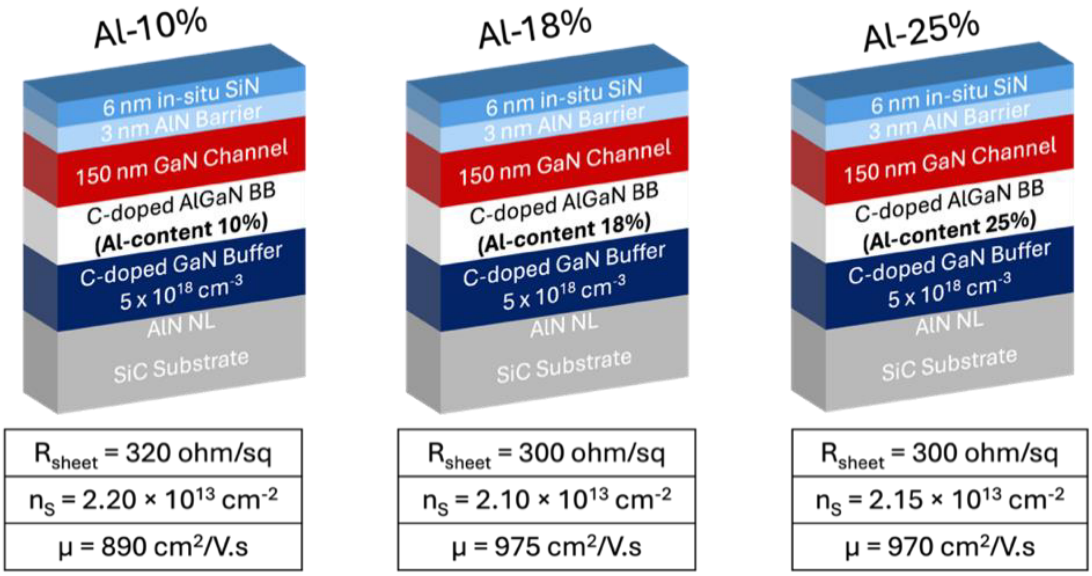


Figure 3.20. Structures under studied with Al-content ranging from 10% to 25%

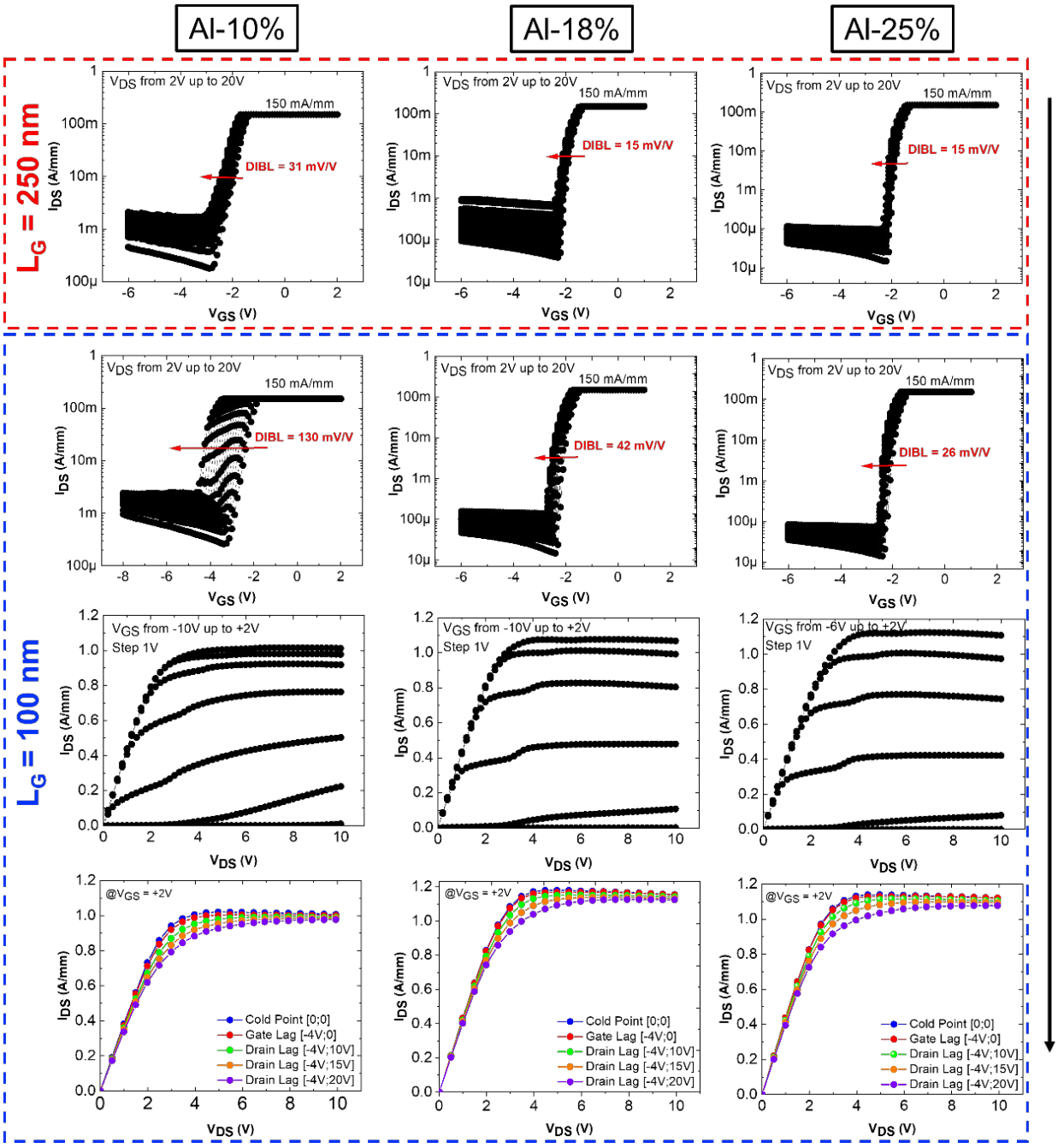


Figure 3.21. IV characteristics of AlGaN back-barrier HEMTs with 10% to 25% Al-content.

When using 250 nm gate length devices (red color), an excellent electron confinement is extracted for all three structures. However, to achieve optimal high-frequency performance, shorter gate lengths are required. When the gate length is reduced to 100 nm (blue color), a significant degradation in electron confinement and increased of drain leakage current is observed for the Al-10% structure along with a device degradation under higher bias (V_{DS} > 15 V).

This indicates that low Al-content (< 10%) within the AlGaN back barrier is inadequate to increase the conduction band offset between the AlGaN/GaN layer. In this case, the low Al% based back-barrier does not ensure proper electron confinement under high electric field, compromising the robustness of these devices. In contrast, the Al-18% and Al-25% provides excellent DIBL with a low leakage current up to V_{DS} = 20V, resulting from a strong back-polarization and high energy barrier at the interface. The trapping effects are minimal for all structures, regardless of the Al% in the AlGaN back barrier (around 15% of current collapse at V_{DS} = 20V). This is attributed to the moderate carbon doping in the buffer layer, which is located far enough from the 2DEG (250 nm) and thus minimizing its impact on device dynamic performances. Moreover, due to a higher bandgap than GaN, the AlGaN back barrier prevents electrons from being injected into the GaN buffer. Finally, it is important to notice that the high concentration of carbon in the AlGaN back barrier did not induce significant trapping effects. This suggests that: carbon compensation in the AlGaN layer may not generate trapping activation as seen in GaN layers; a large portion of the carbon in the AlGaN back barrier compensates the second 2DEG at the AlGaN back-barrier / GaN buffer interface as we will see later in this chapter. **Figure 3.22** summarizes the DIBL as a function of gate lengths for the four structures. Due to their poor electrical characteristics, the Al-10% structure was excluded from further study.

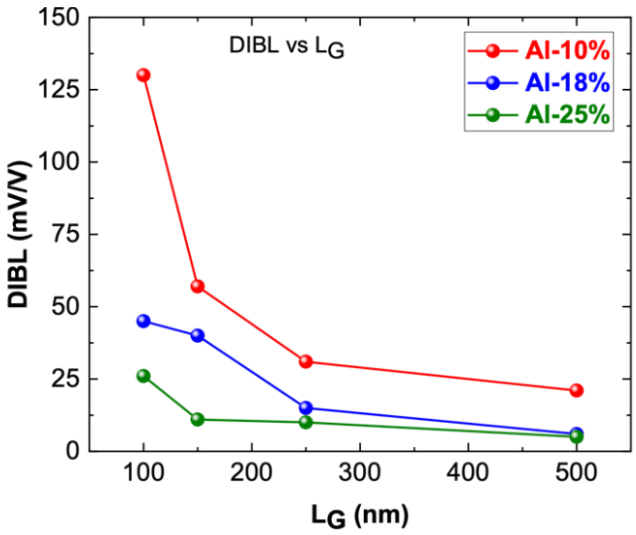


Figure 3.22. DIBL as a function of L_G for devices with 10% to 25% Al-content.

For short devices, the Al-25% structure offers the best balance in terms of electron confinement (DIBL = 26 mV/V), maximum current density (1.1 A/mm at V_{GS} = +2V).

The measured extrinsic G_M is around 400 mS/mm and has a linear shape (comparable to HRL's graded channel HEMT). This shape indicates promising linearity performances for this structure. Linearity measurements are planned in the future, with a current development of a two-tone bench in our research group (Lyes Ben-Hammou's PhD thesis).

S-parameter measurements were performed up to 67 GHz, showing cut-off frequencies F_T / F_{MAX} of 60 GHz / 270 GHz at V_{DS} = 20V. In addition, a high-power gain of 15 dB at 40 GHz is also achieved. **Figure 3.23** summarizes the DC and small signal characteristics of the Al-25% structure. The Al-18% structure delivers comparable performance but with a slightly degraded electron confinement (DIBL = 42 mV/V) and higher drain leakage current.

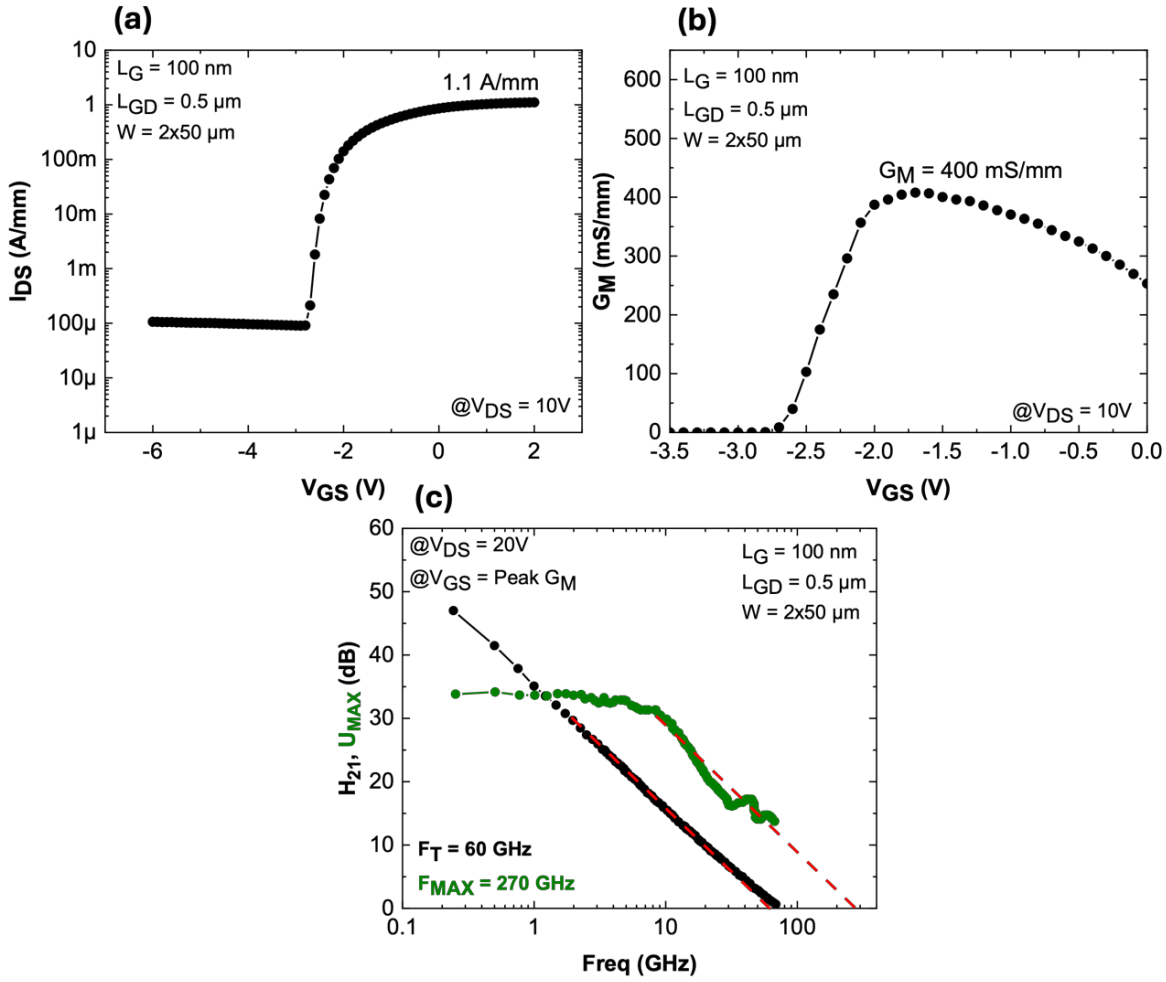


Figure 3.23. (a) I_DV_G, (b) G_M and (c) F_t/F_{max} at V_{DS} = 20V for Al-25% structure of 2×50 µm transistors with L_G = 100 nm and L_{GD} = 0.5 µm.

III.3. Large signal characterization at 40 GHz

III.3.a. Power performance of the Al-18% structure

In order to further compare the Al-18% and Al-25% structures, load pull measurements have been performed. Large-signal measurements were carried out on a PNA-X network analyzer (N5245A-NVNA) allowing load-pull on-wafer characterizations at 40 GHz in CW and pulsed mode. **Figure 3.24** shows CW performances (PAE matching, class AB : 100 mA/mm) of a 2×50 µm transistor with L_G = 100 nm and L_{GD} = 0.5 µm up to V_{DS} = 20V.

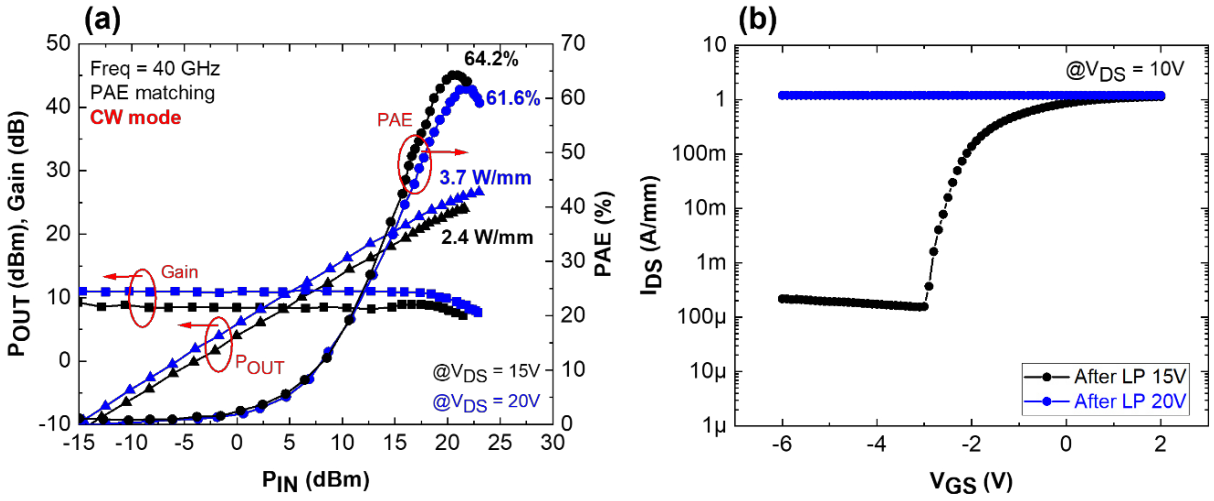


Figure 3.24. (a) CW large signal performance at 40 GHz up to V_{DS} = 20V of the Al-18% structure. (b) I_DV_G characteristics after load-pull sweeps (L_G = 100 nm, L_{GD} = 0.5 µm).

A high PAE of 64.2% at V_{DS} = 15V is achieved with an associated P_{OUT} of 2.4 W/mm. At V_{DS} = 20V, the PAE remains above 60% with an increase of the output power at 3.7 W/mm. However, after multiple sweeps at V_{DS} = 20V, we observed a severe degradation of the leakage current resulting in complete degradation of devices. Power performance measurements under pulsed mode were performed as well. **Figure 3.25** shows an improved PAE/P_{OUT} combination but the gap with CW performance is not significant (about 5 points for PAE). This is mainly due to the quite low electron trapping effects within the structure. At V_{DS} = 15/20V, PAE was 68.6% (P_{OUT} = 2.6 W/mm) and 61.6% (P_{OUT} = 4.5 W/mm), respectively. Despite excellent RF performances, we also observed a severe degradation of the devices after several sweeps at V_{DS} = 20V.

The degradation in pulsed mode shows that the origin is more related to the electric field than the junction temperature. Therefore, for the 18%-Al structure, the bias limitation appears to be around V_{DS} = 15V, which indicates that the Al-content is not high enough in the AlGaN back barrier to properly operate at higher drain bias.

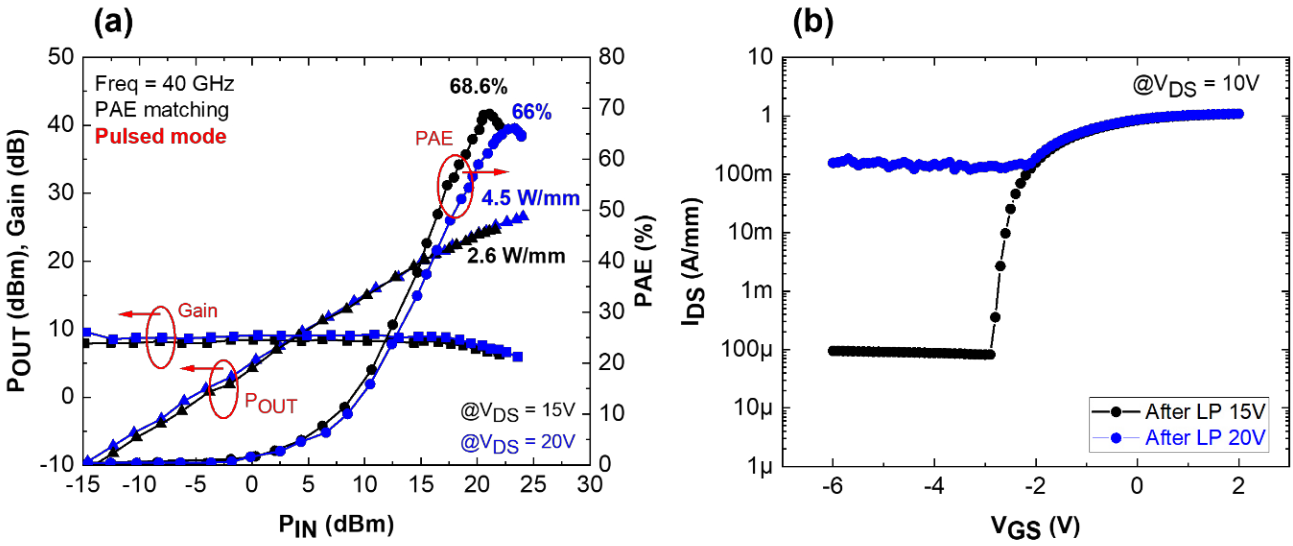


Figure 3.25. (a) Pulsed large signal performances at 40 GHz up to V_{DS} = 20V of the Al-18% structure. (b) I_DV_G characteristics after load-pull sweeps (L_G = 100 nm, L_{GD} = 0.5 µm).

III.3.b. Power performance of the Al-25% structure

Figure 3.26 presents CW performance of a 2×50 µm transistor with L_G = 100 nm and L_{GD} = 0.5 µm up to V_{DS} = 25 V. The measured optimum PAE is 67% and 66.5% at V_{DS} = 15 and 20V with an output power of 2.5 and 3.5 W/mm, respectively. This represents one of the highest PAE achieved at 40 GHz under high power density (> 3 W/mm). Moreover, in contrast with the Al-18% structure, no degradation of the device was observed at V_{DS} = 20 V, which constituted an improvement. This is attributed to the higher Al-content into the back barrier, enabling better electron confinement and lower leakage current. As a result, the device has been pushed at higher drain bias. At V_{DS} = 25 V, PAE was 57.5% with an associated P_{OUT} of 4.8 W/mm. However, at this bias, the device was degraded due to strong electric field and the short transistor design.

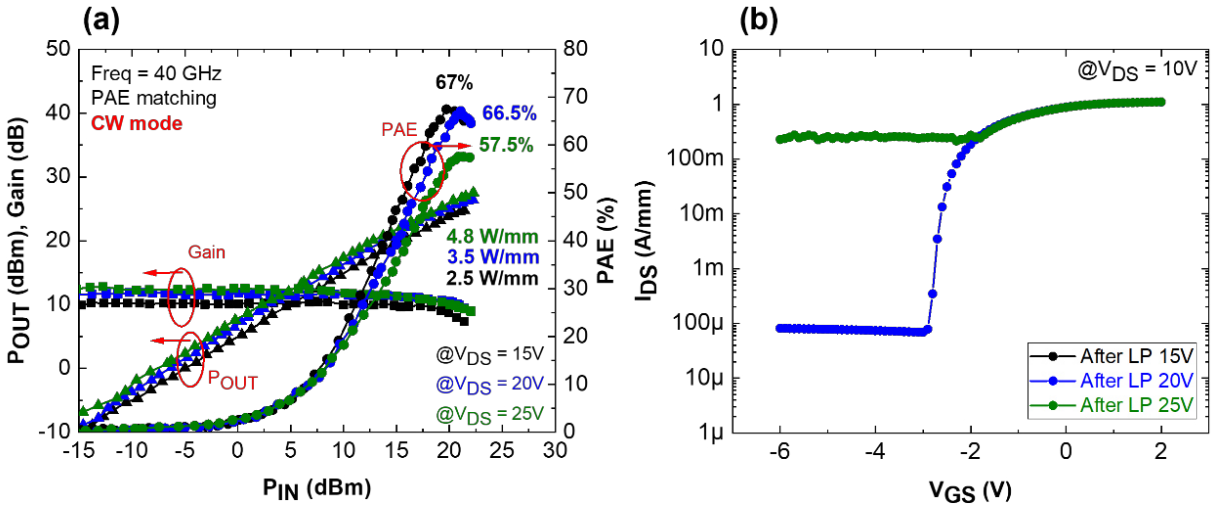


Figure 3.26. (a) CW large signal performances at 40 GHz up to V_{DS} = 25V of the Al-25% structure. (b) I_DV_G characteristics after load-pull sweeps (L_G = 100 nm, L_{GD} = 0.5 µm).

Figure 3.27 displays the results obtained in pulsed mode. A record PAE of 74% and 70% was reached at V_{DS} = 15 and 20V, respectively. Notably, the gap between CW/pulsed mode is also greatly reduced (less than 5 points at V_{DS} = 20V) compared with the highly C-doped AlN/GaN structure (over 10 points difference, [15]). The device could also be biased up to V_{DS} = 25V without degradation and the PAE was 65% with an associated P_{OUT} of 6.0 W/mm. At V_{DS} = 30V, the output power was very high (7.1 W/mm) and the PAE was still impressive (58.5%), but the components were degraded after measurements.

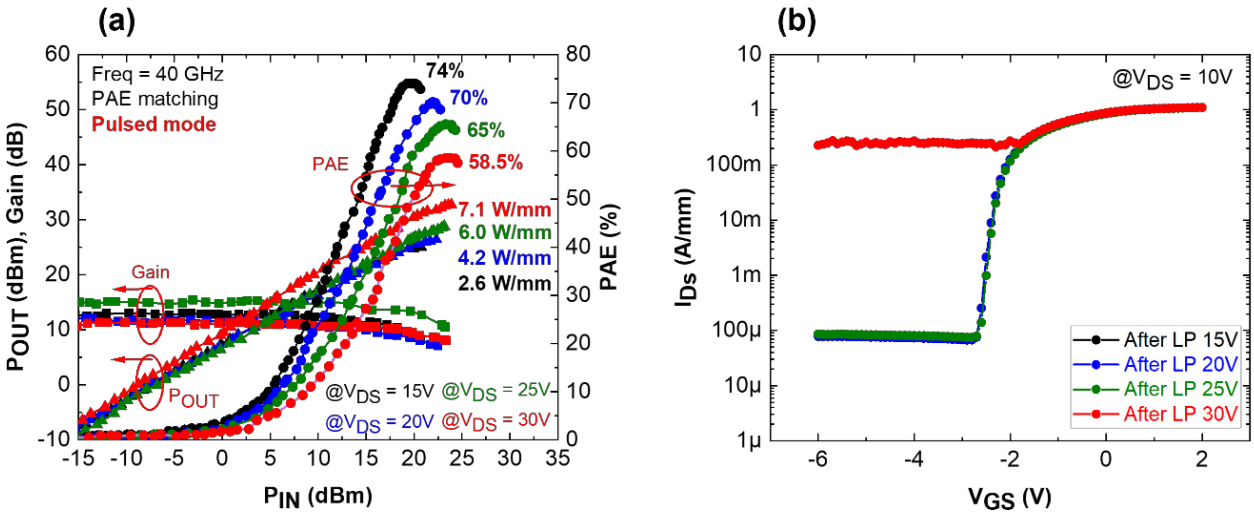


Figure 3.27. (a) Pulsed large signal performances at 40 GHz up to V_{DS} = 30V of the Al-25% structure. (b) I_DV_G characteristics after load-pull sweeps (L_G = 100 nm, L_{GD} = 0.5 µm).

Figure 3.28 compares and summarizes the power performances of both AlGaN back-barrier structures. Although the Al-18% structure shows very good results, it does not appear robust enough for operation up to V_{DS} = 20V. Severe degradation of the devices has been observed after multiple load-pull sweeps, which points towards the insufficient Al-content in the AlGaN back barrier. In contrast, the Al-25% structure showed no degradation up to V_{DS} = 20V, indicating that this Al-content is suitable with state-of-the-art large signal power performances at 40 GHz for Ga-polar HEMTs.

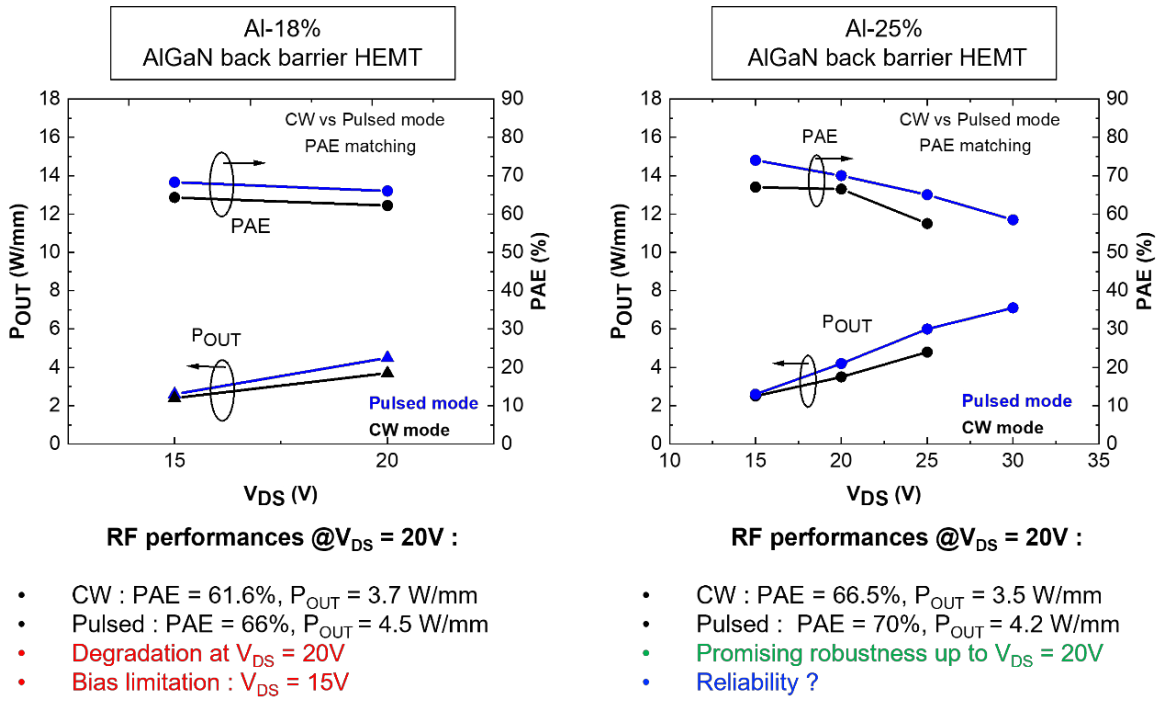


Figure 3.28. Summary of power performances between Al-18% and Al-25% AlGaN back barrier HEMTs at 40 GHz.

For the remainder of the study, the Al-18% structure is excluded due to the limited robustness at V_{DS} = 20V. The Al-25% structure demonstrates all the required characteristics for future Ka-band applications. This structure features indeed a major improvement in terms of trapping reduction thanks to the insertion of an AlGaN back barrier layer compared with the C-doped AlN/GaN HEMTs while maintaining a promising robustness. However, further investigations including short-term reliability assessments and structural analysis are required to validate and gain deeper insights into this technology.

III.4. Structural analysis of the Al-25% structure

To better understand the achieved outstanding electrical characteristics, structural characterization of the AlN/GaN/AlGaN back barrier (Al-25%) HEMTs was carried out using high-resolution transmission electron microscopy (HRTEM). Thin lamella required for TEM analysis were prepared at IEMN using focused ion beam (FIB) technique. Then, samples were sent to C2N laboratory for detailed analysis. Moreover, Secondary-Ion Mass Spectrometry (SIMS) has been also performed. Unprocessed samples were sent to *Eurofins EAG* Laboratories to further explore the composition and impurities of the structure. A key challenge in fabricating high-performance devices remains the undesired background defects or levels in AlGaN or GaN crystals. Finally, in our case, controlling both Al-content and carbon doping into the AlGaN back barrier is also essential for optimum performances. Secondary ion mass spectrometry (SIMS) was carried out to verify and control the carbon concentration as well as impurities such as oxygen (**Figure 3.30**). For instance, oxygen has been identified in GaN layers as a source of unintentional n-type conductivity [16, 17]. In our case, we observed low oxygen concentration along the structure, showing minimal level of impurities.

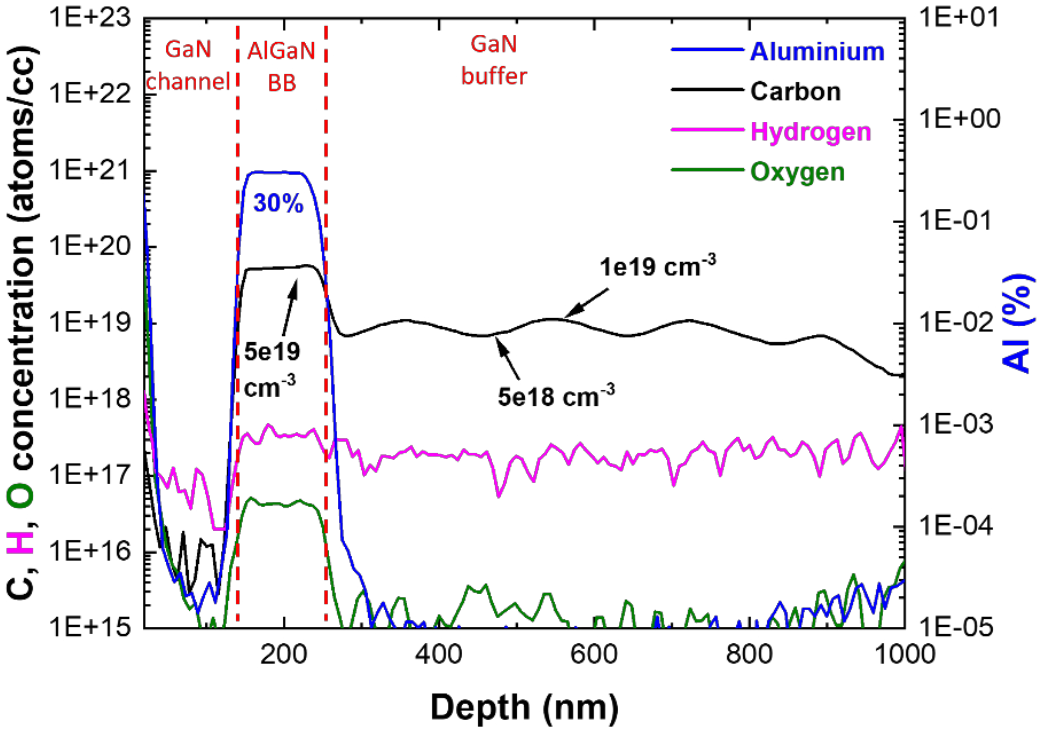


Figure 3.30. SIMS analysis of the AlN/GaN/AlGaN back barrier structure.

The Al-content within the AlGaN back barrier is estimated to be 30%, in agreement with the EDX analysis. The average carbon concentration in the GaN buffer is approximately 7×10^{18} cm^{-3} which is consistent with the targeting value. A significant carbon concentration of 5×10^{19} cm^{-3} is observed in the AlGaN back barrier with 1×10^{19} cm^{-3} at the back barrier/GaN buffer interface. The impact of the carbon concentration in the AlGaN back barrier will be studied in more detail in this chapter.

III.5. Short-term high temperature operating life test at 40 GHz

As presented before, the AlGaN back barrier structure enabled to achieve state of the art power performance at 40 GHz, without noticeable degradation up to V_{DS} = 20V. However, this structure needs to be evaluated in terms of reliability. On-wafer short-term high temperature operating life (HTOL) tests offer initial insight into device degradation or failure, providing feedback for material quality or process adjustments prior to long-term reliability of packaged devices. This evaluation involves RF robustness test under severe conditions for few hours using a high junction temperature (Tj = 250°C). In our case, these tests are carried out directly on wafer with our load-pull setup, without any device packaging. To reach a high junction temperature, specific bias conditions (V_{DS}, I_{DS}) are combined with a high chuck temperature (T_{chuck}) with respect to the transistor design.

The estimation of the exact junction temperature of a device is not trivial. This can be performed by Raman spectroscopy or Finite Element Analysis (FEA) simulations which are not available at IEMN laboratory [18-21]. However, as part of the project GREAT, the industrial partner United Monolithic Semiconductors (UMS) has established the conditions required to reach Tj = 250°C but for the C-doped AlN/GaN HEMT without AlGaN back barrier. These are the following conditions:

W = 2×50 µm / L_G = 150 nm / L_{GD} = 1.5 µm / V_{DS} = 20V / I_{DS} = 225 mA/mm and T_{chuck} = 150°C

It should be reminded that the high Al% in the AlGaN back barrier structure is around 30%, which is not beneficial for efficient heat dissipation. Consequently, the conditions given by UMS yield in T_J certainly well-above 250°C.

Figure 3.31 shows the short-term HTOL test carried out under these conditions during 8 hours on the AlGaN back barrier HEMTs. Measurements are performed under large signal conditions at 40 GHz.

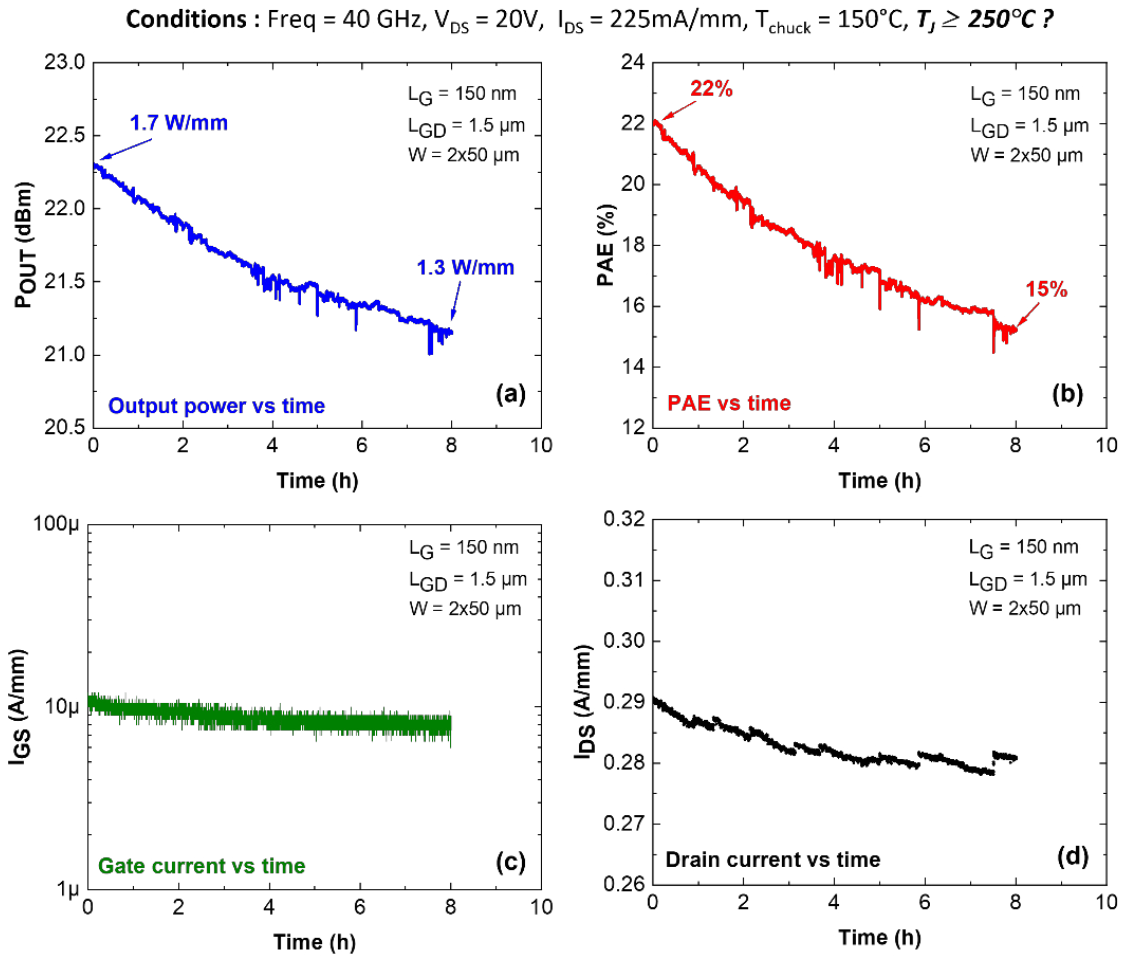


Figure 3.31. HTOL test for 8 hours monitoring (a) P_{OUT}, (b) PAE, (c) I_{GS} and (d) I_{DS} vs time.

The maximum PAE is only 22% with an associated P_{OUT} of 1.7 W/mm. This expected decrease (compared to previous load pull results at room temperature) is attributed to self-heating and thermal impacts, reducing the electron mobility at high temperature, which directly affects the gain and, therefore the PAE. Furthermore, transistors with L_{GD} = 1.5 µm have slightly lower power gain as compared to L_{GD} = 0.5 µm and finally measurements are not performed under class AB (100 mA/mm vs 225 mA/mm for HTOL). Nevertheless, under these conditions, a severe drop in PAE/P_{OUT}/I_{DS} over 8 hours is observed, indicating a poor reliability over extended periods. However, no degradation of gate leakage current was noticed during the test. **Figure 3.32** presents the IV-curves before and after the 8h of HTOL stress.

The DC characteristics remained particularly similar to those observed before the test, despite the significant drop in performance (**Figure 3.32.a and b**). These measurements were performed directly after the HTOL test. However, a notable difference in electron trapping is clearly observed, particularly in terms of drain lag, reflected by a significant current collapse increase from 13% before stress to 30% after stress (**Figure 3.32.c**).

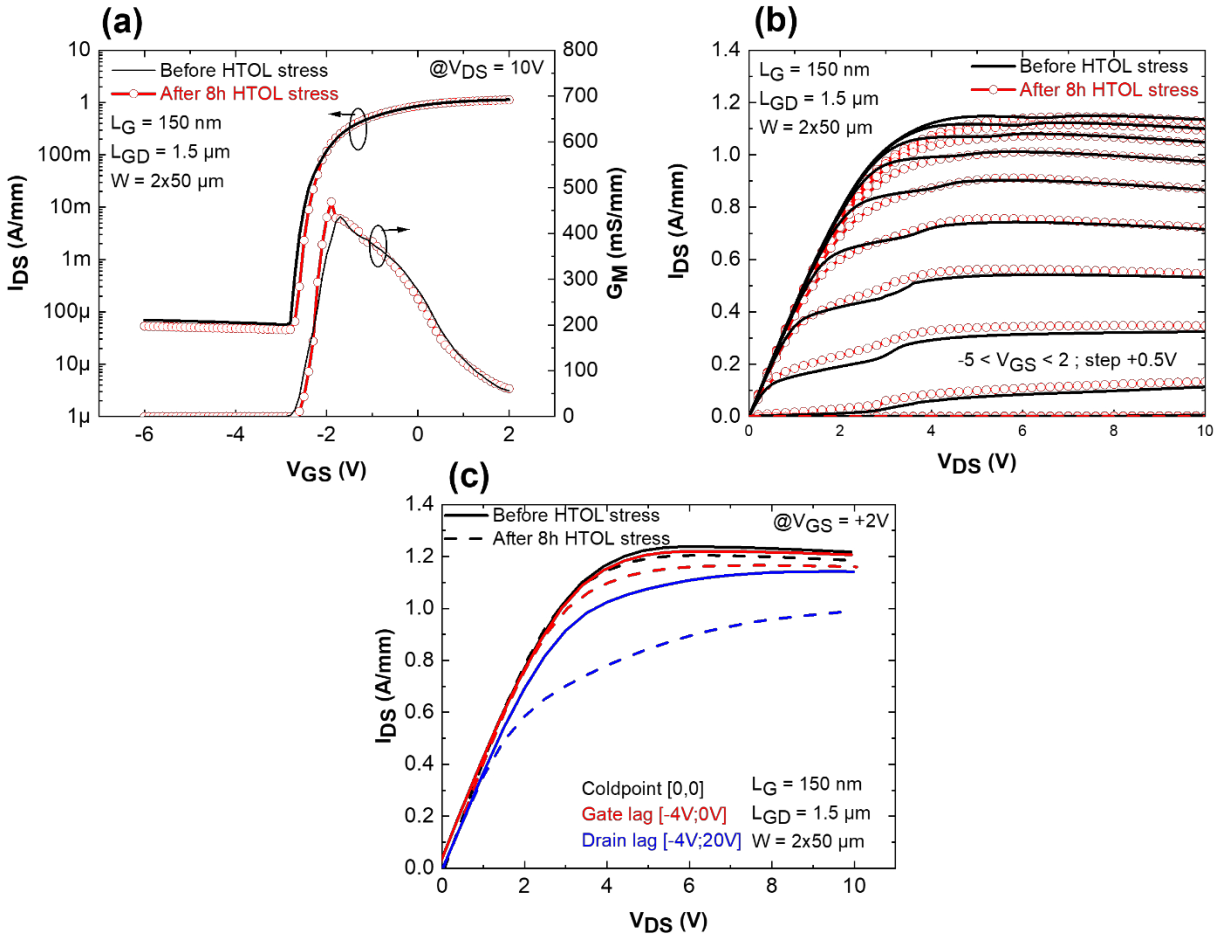


Figure 3.32. I_DV_G (a), I_DV_D (b) and DC-pulsed (c) characteristics before and after 8 hours of HTOL stress.

Currently, the increase in trapping effects cannot be directly linked to the performance drop during HTOL stress and may represent a distinct phenomenon. Two hypotheses are proposed to explain this increase: the first one involves the activation of deep carbon traps under high junction temperature. The second one concerns a physical degradation near the peak electric field, such as the passivation layer, the barrier layer or the gate metal, which may activate surface traps.

The second hypothesis was investigated by means of HRTEM analysis on devices subjected to 8 hours of HTOL stress, which was compared with an unstressed control transistor (**Figure 3.33**).

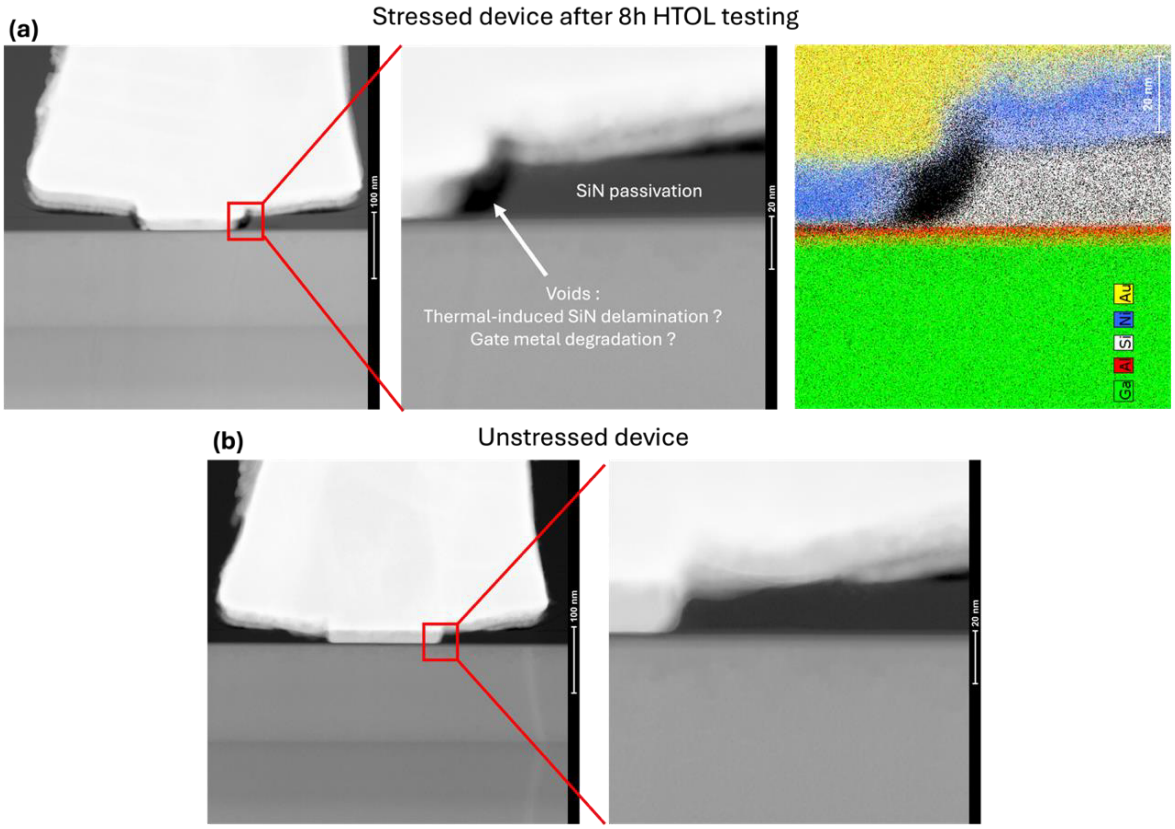


Figure 3.33. STEM image comparison between stressed (a) and unstressed device (b) in the gate region.

For the stressed device, a noticeable modification of the SiN passivation layer in the the gate foot vicinity was observed. Voids were formed at the Ni/SiN interface (**Figure 3.33.a**), which were not present prior to the electrical stress (**Figure 3.33.b**). According to the literature, for extended periods of HTOL stress, these defects can create pathways for Au alloy diffusion all the way down to the barrier layer [22-25]. This degradation can lead to a shift in threshold voltage, output current drop as well as increase of gate leakage current. These observations could largely explain the increase in trapping due to hot electron injection in the SiN layer occurring under high electric field and high junction temperature. However, the activation of deep carbon traps in the structure during stress cannot be entirely ruled out. As mentioned, the junction temperature is estimated to at least 250°C or most probably higher.

However, if the junction temperature is underestimated, the conditions used before may be too severe. We therefore carried out another HTOL test with a reduced chuck temperature. This test allows to reduce the junction temperature and determine the device's Safe Operating Area (SOA). **Figure 3.34** presents the HTOL test carried out for 8 hours under the same conditions but with T_{chuck} sets at 100°C.

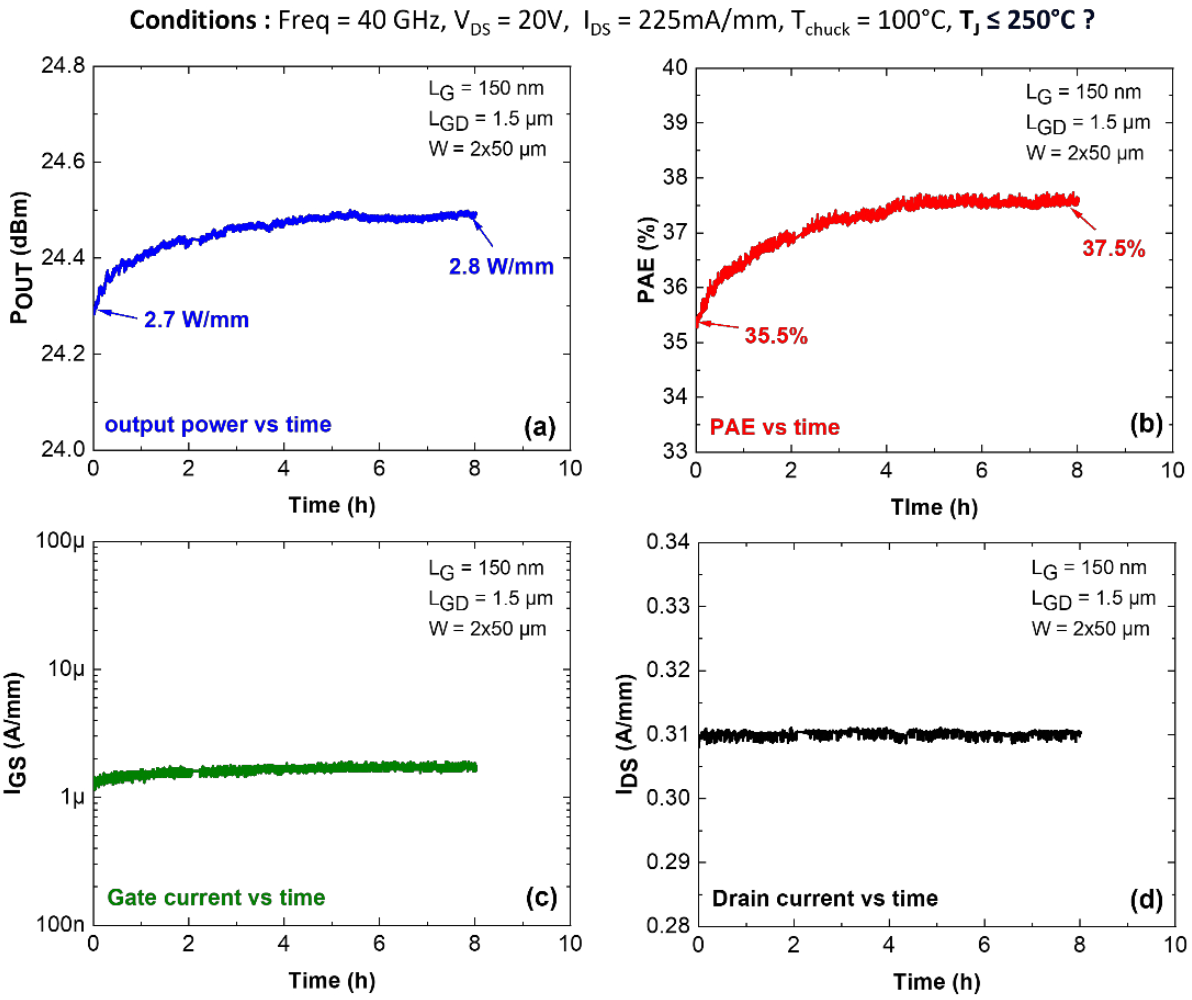


Figure 3.34. HTOL test for 8 hours monitoring (a) P_{OUT}, (b) PAE, (c) I_{GS} and (d) I_{DS} vs time.

The device's behavior differs considerably from the one observed at T_{chuck} = 150°C. Power performances are much better due to the lower junction temperature, which has less impact on electron mobility. More importantly, power performances remained remarkably stable during the 8h HTOL stress, confirming the direct impact of a reduced junction temperature in the channel. This result is promising for long-term reliability. However, proper measurements of the junction temperature enabling fine tuning of Tj (e.g. T_{chuck}) will be needed to better define the SOA of this technology.

Figure 3.35 presents the IV-characteristics before and after 8h of HTOL stress. The DC characteristics remained consistent as compared to those observed before the stress, with no significant changes in leakage current, and maximum drain current (**Figure 3.35.a and b**). However, a slight difference was observed in the trapping behavior with a current collapse only increasing from 11% to 16% after stress and had no impact on the device performances. (**Figure 3.35.c**). This is much lower than the HTOL test performed at T_{chuck} = 150°C.

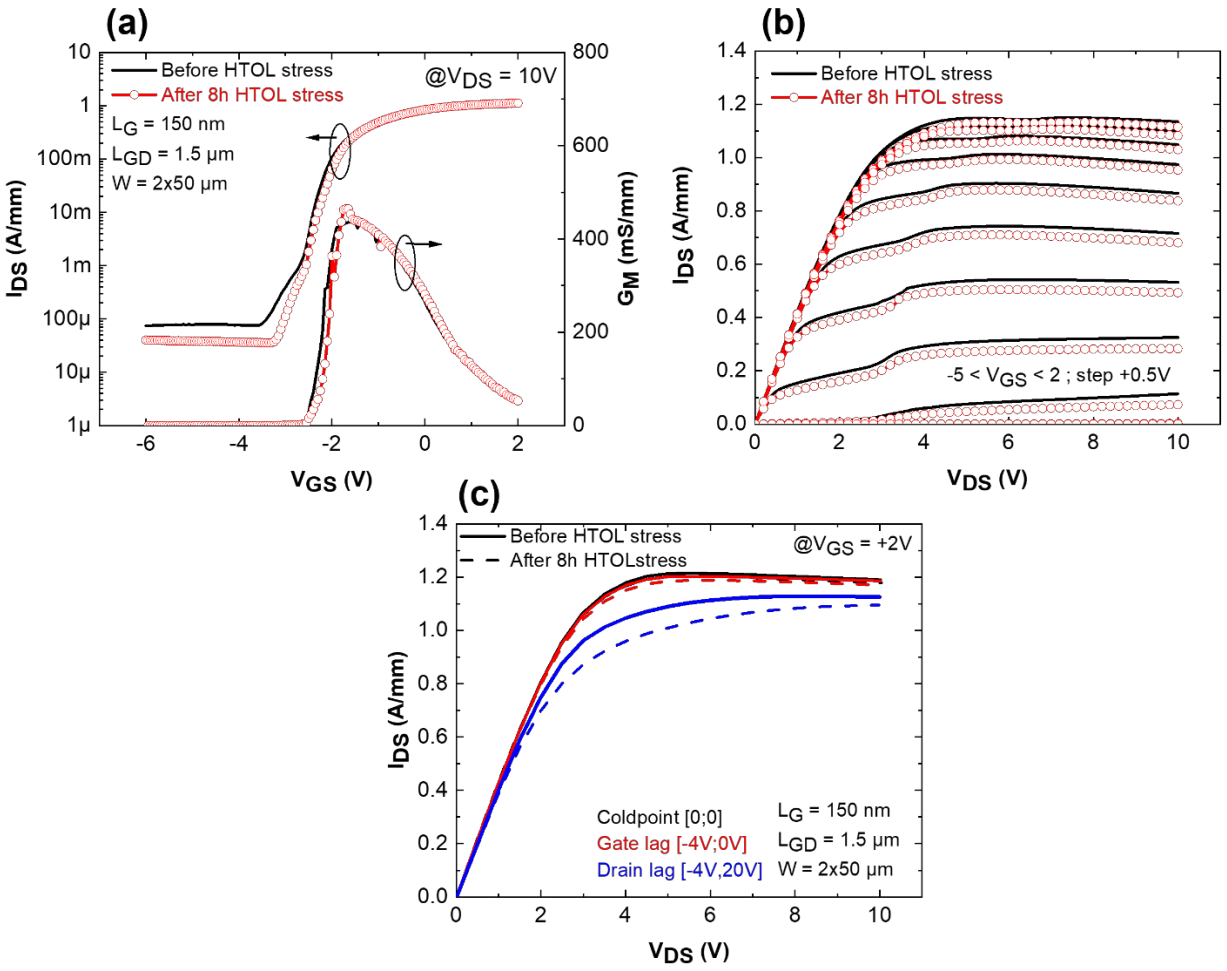


Figure 3.35. I_DV_G (a), I_DV_D (b) and DC-pulsed characteristics (c) before and after 8 hours of HTOL stress.

To correlate this slight increase in trapping with surface degradation, we also conducted an HRTEM analysis on this device (**Figure 3.36**). We observed the same type of voids, but less pronounced at the Ni/SiN interface compared with those shown at T_{chuck} = 150°C.

This indicates that the resulting voids subsequent to the electrical test scales with the junction temperature and most probably are time dependent. It seems that that the stress time under such conditions does not degrade the surface enough to induce significant current collapse. A longer stress time may result in larger voids, increased trapping effects leading to a drop of RF power performance. Processing efforts are required to adjust the gate module (gate shape, nature of passivation and metal stack) in order to avoid such a degradation under high junction temperature.

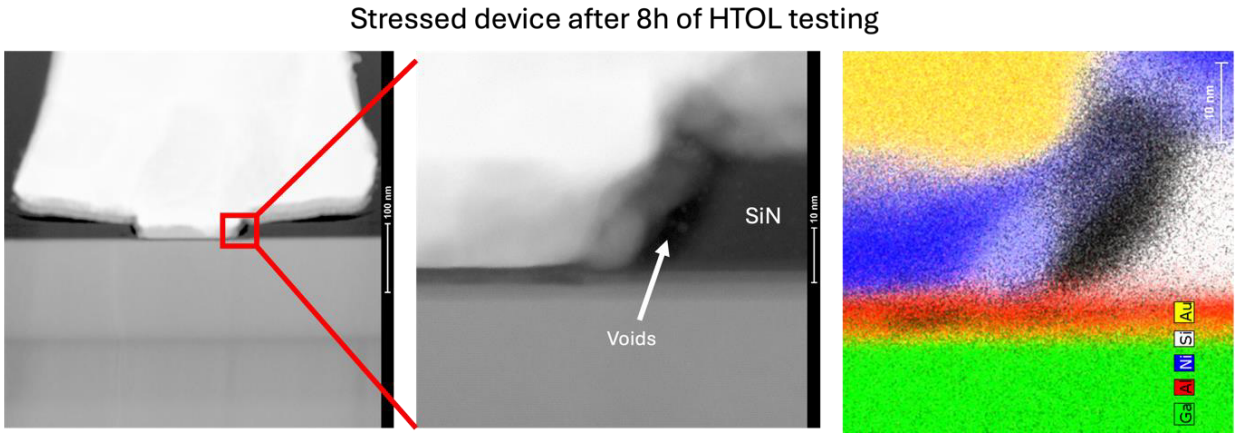


Figure 3.36. STEM images of the stressed device in the gate region.

III.6. Impact of carbon doping in the AlGaN back barrier

III.6.a. Presentation of the studied structures

As shown with the SIMS analysis, the AlGaN back barrier is heavily doped with carbon. In this section, we examine its impact on the device's electrical characteristics using two structures **(Figure 3.37**). 2DEG properties are identical for both structures, with an electron density of 2.2×10^{13} cm^{-2} and an associated electron mobility of 800 $cm^2/V.s$.

- **Structure A** features a highly carbon-doped AlGaN back barrier layer, similar to the structure presented in the previous section. The only difference is the thickness of the GaN channel, which has been reduced from 150 nm to 100 nm. This change was made to confine electrons in case the absence of carbon in the AlGaN back barrier (structure B) degraded the device's electrical characteristics.
- **Structure B** is identical to structure A, except that the AlGaN back barrier is undoped.

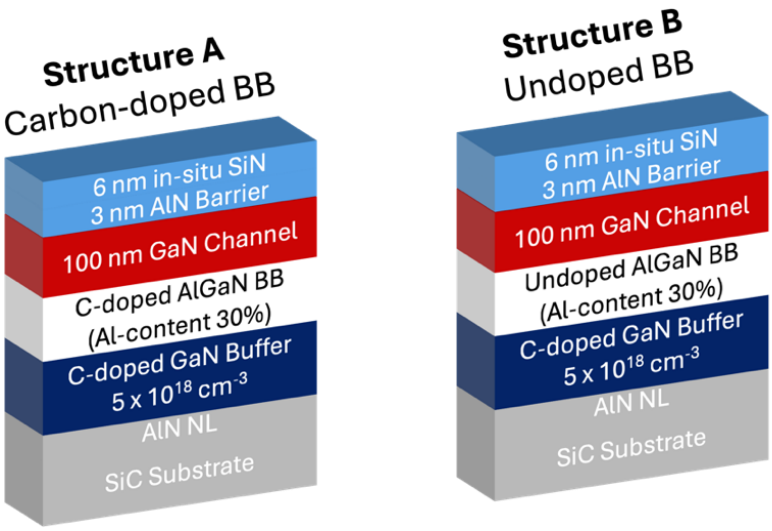


Figure 3.37. High C-doped (left) and Undoped (right) AlGaN back barrier structures.

Figure 3.38 presents a SIMS comparison of the structures. The Al-content in the back barrier is 30%. The only difference is that in structure B, the Al-content is more gradually distributed than in structure A. The carbon concentration in the AlGaN back barrier for structure A is 4×10^{19} cm^{-3}. It is also important to note that the carbon concentration is also high at the back barrier/C-GaN buffer interface ($1\times10^{19}cm^{-3}$). For structure B, the carbon concentration is 5×10^{16} cm^{-3} (considered undoped) and 5×10^{17} cm^{-3} at the AlGaN BB / GaN interface.

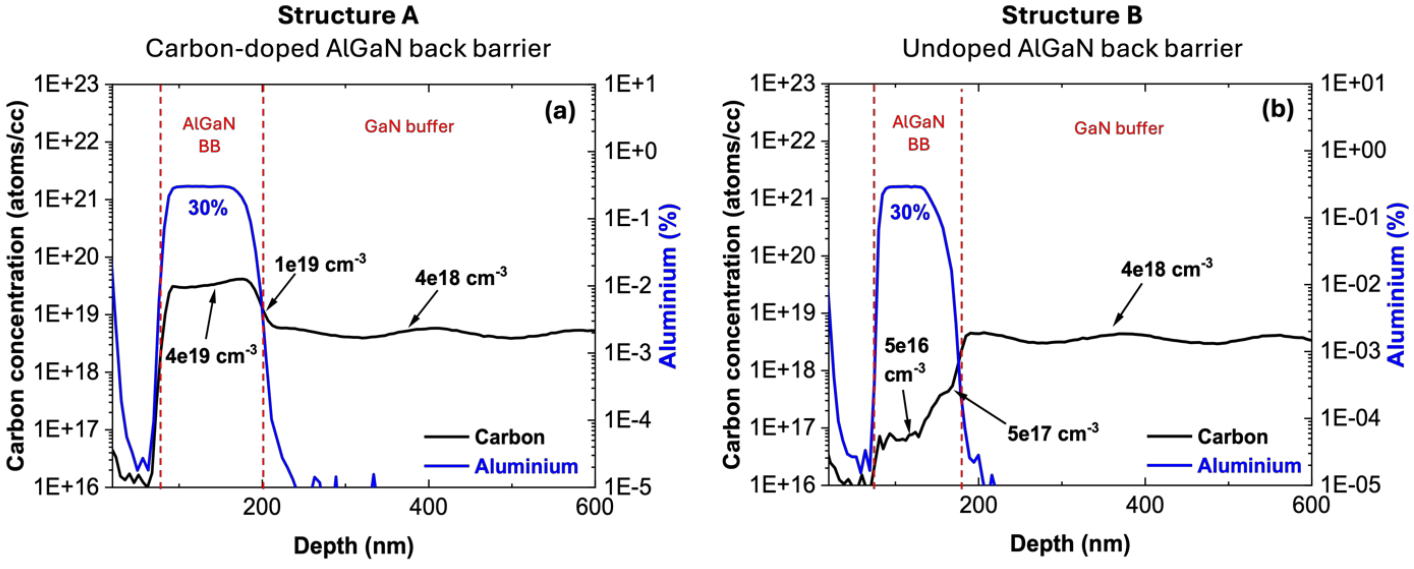


Figure 3.38. SIMS comparison between structure A and B.

III.6.b. Electrical characteristics of highly doped versus undoped back barrier

DC measurements were performed on both structures. **Figure 3.39** presents a comparison of DIBL, I_DV_G, G_M, and DC-pulsed characteristics of 2×25 µm transistors with L_G = 500 nm (red), 100 nm (blue) and L_{GD} = 0.5 µm.

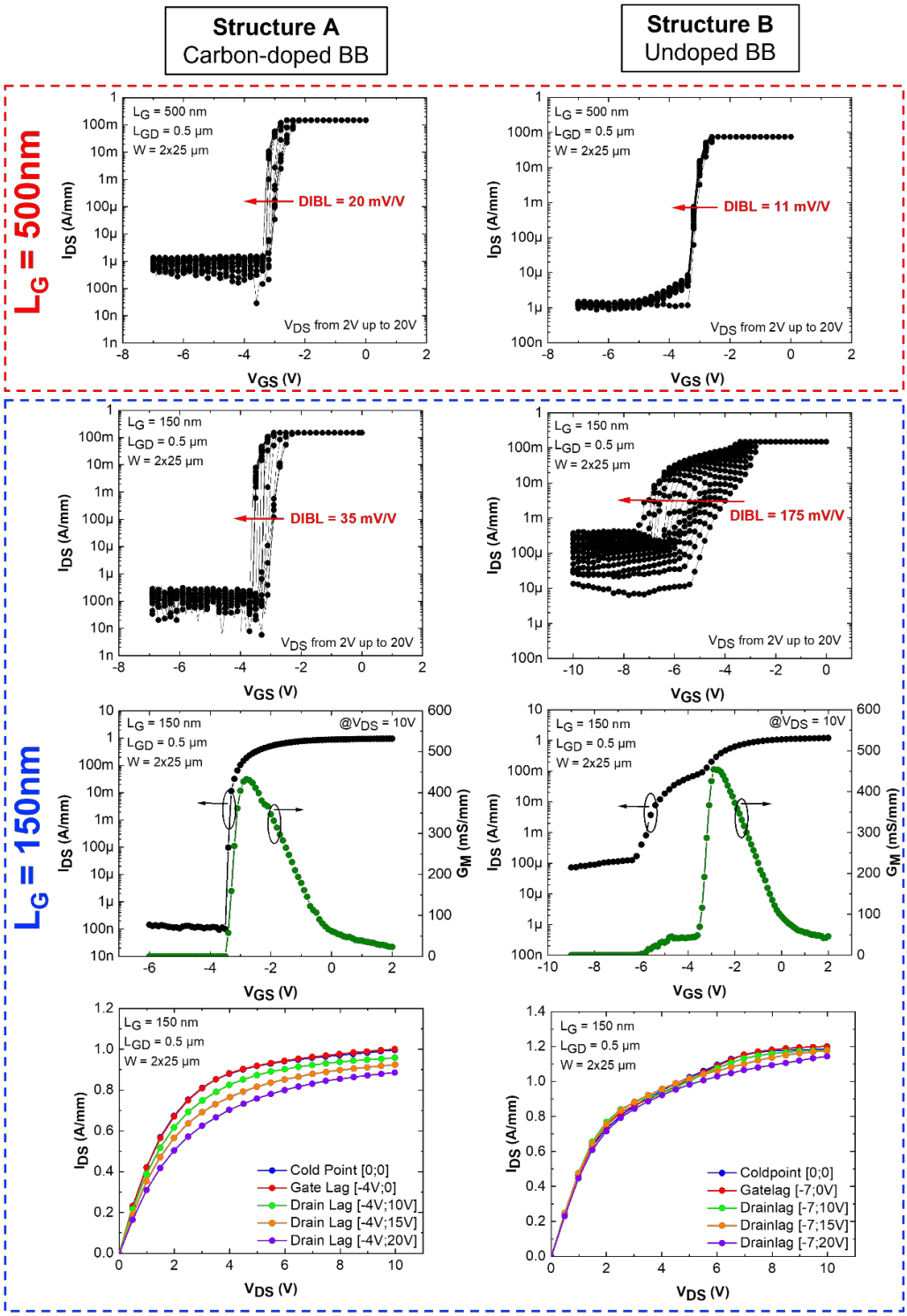


Figure 3.39. IV characteristics comparison structures A and B.

For large gate lengths (L_G = 500 nm), we observed low leakage current and excellent electron confinement for both structures. At first sight, the absence of carbon doping in the AlGaN back barrier does not appear to create any electrical issues. However, when the gate length was reduced down to 150 nm, clear differences were found. Structure B (undoped) failed to confine electrons under high electric field, resulting in poor electron confinement (DIBL = 175 mV/V) and high leakage currents up to V_{DS} = 20V. In contrast, the highly carbon-doped structure exhibited very low leakage currents (below 10 uA/mm), along with excellent electron confinement (DIBL = 35 mV/V). The maximum current for both structures is around 1 A/mm, with a comparable transconductance of 450 mS/mm. In terms of electron trapping, the undoped back barrier delivers low current collapse. In contrast, structure A shows a current collapse of around 20% at V_{DS} = 20V. This is consistent with the high carbon concentration in the AlGaN back barrier near the 2DEG when using a 100 nm thick GaN channel, as compared to the previous 150 nm thick GaN channel structure.

In addition, the IV curves of the undoped structure do not show proper pinch-off. Unexpectedly, a second threshold voltage was identified, indicating the presence of a parasitic conduction. This severe parasitic conduction may suggest the existence of a 2nd 2DEG at the interface between the AlGaN back barrier and the GaN buffer. To investigate this possibility, capacitance-voltage (C-V) characterizations were carried out on both structures (**Figure 3.40**) [26]. Measurements were performed on circular Schottky diodes with a 54 µm diameter, using a frequency of 1 MHz and a reverse voltage sweep up to -40 V to ensure complete 2DEG depletion. We observed that the carbon-doped structure shows a single sharp peak, corresponding to the 2DEG between the Al-rich barrier and the GaN channel. In contrast, the undoped structure shows two distinct peaks. The first corresponds to the 2DEG, while the second one (much weaker) indicates the presence of another electron well in the structure. This observation confirms that the absence of carbon compensation leads to the formation of a 2nd 2DEG at the AlGaN back barrier/GaN buffer interface. Consequently, carbon doping in the back barrier plays a crucial role in the electrical characteristics of the device.

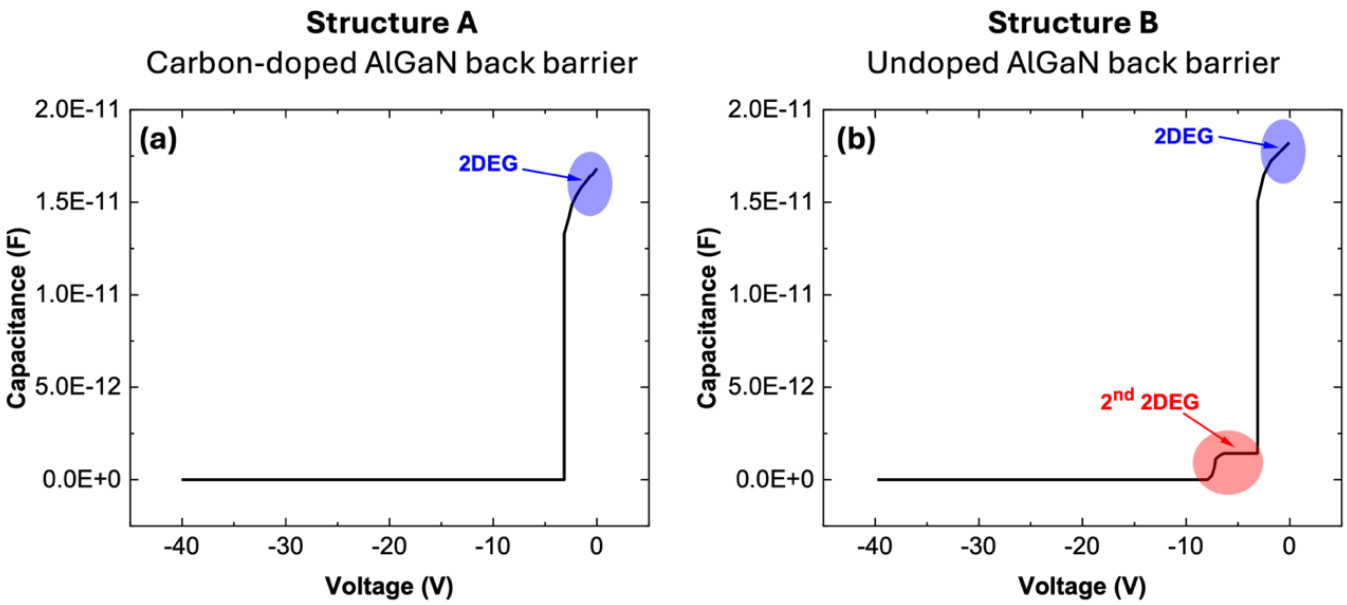


Figure 3.40. Capacitance-Voltage (C-V) profile comparison between structure A and B.

III.6.c. TCAD simulation and physical insights of C-doped back barrier

The influence of C-doping within the AlGaN back barrier and its effect on the second 2DEG have been investigated using TCAD simulation. **Figure 3.41.a** shows the structure reproduced in ATLAS SILVACO. The GaN channel and AlGaN back barrier layers are both 100 nm thick, while the GaN buffer is 1 µm. The gate length is 150 nm, and the gate-drain distance is 0.5 µm. For carbon doping, acceptor traps with an energy level of 0.9 eV below the conduction band (rather than E_V + 0.9 eV [27, 28]) were introduced in the AlGaN back barrier and the GaN buffer layer [29]. The Al-content in the back barrier was set to 30%, as shown in (**Figure 3.41.b**). **Figure 3.41.c** shows the IV-fitting between the experimental data and the TCAD simulation for the C-doped AlGaN back barrier structure. For calibration, we used physical models similar to those described in Chapter II but adjusted for the AlGaN back barrier structure.

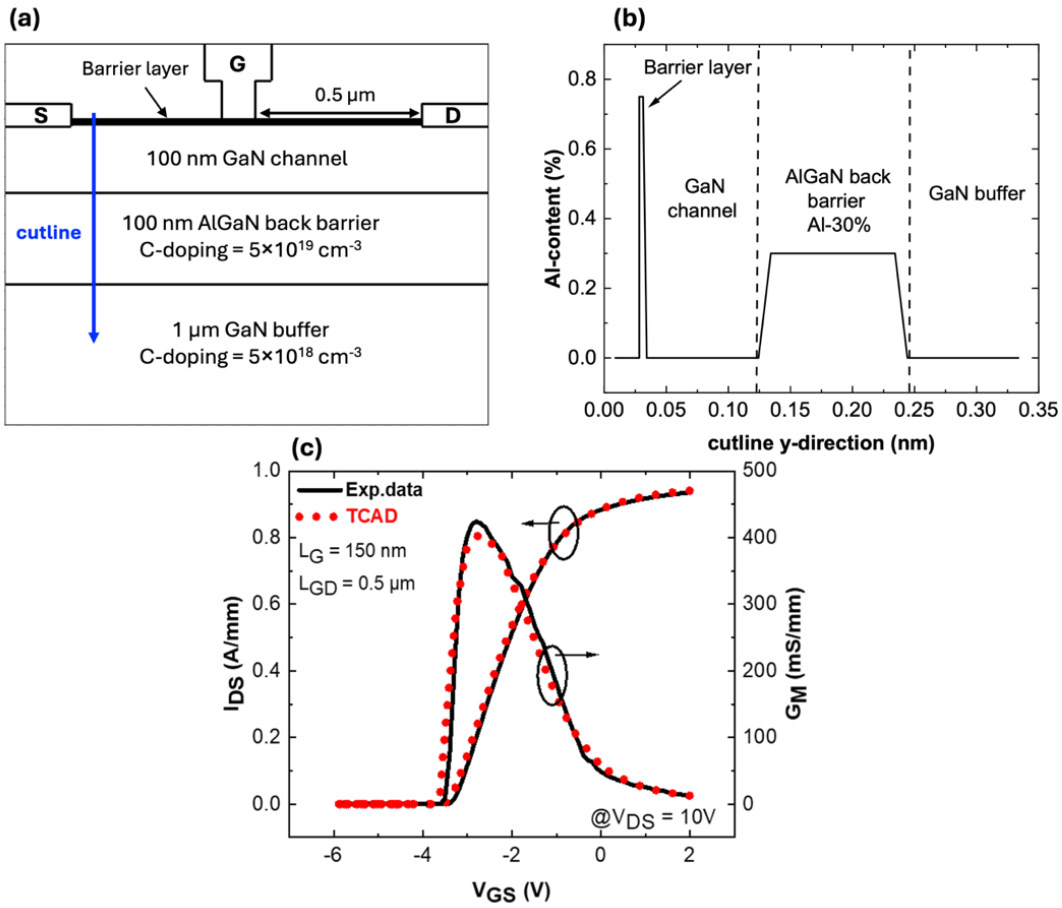


Figure 3.41. (a) TCAD device structure, (b) Al-profile in the structure and (c) exp. data vs TCAD calibration for the high-C doped AlGaN back barrier HEMT.

To investigate the impact of carbon doping, we varied the carbon concentration within the back-barrier as follows:

- AlGaN back barrier C-doping = 5×10^{19} cm^{-3}
- AlGaN back barrier C-doping = 5×10^{18} cm^{-3}
- AlGaN back barrier C-doping = 1×10^{18} cm^{-3}
- AlGaN back barrier C-doping = 5×10^{17} cm^{-3}
- AlGaN back barrier Undoped = 1×10^{17} cm^{-3}

Figure 3.42 illustrates the simulated conduction band diagrams for all cases. For a C-doping of 5×10^{19} cm^{-3} (black), the conduction band looks quite standard with a slight discontinuity at the AlGaN back barrier / GaN buffer interface.

However, when the doping concentration is reduced, the discontinuity at the back-barrier and GaN buffer interface becomes more and more pronounced. The conduction band tends to reach the Fermi level (E_F), suggesting the formation of an electron-well for a C-doping below 5×10^{18} cm^{-3} (red).

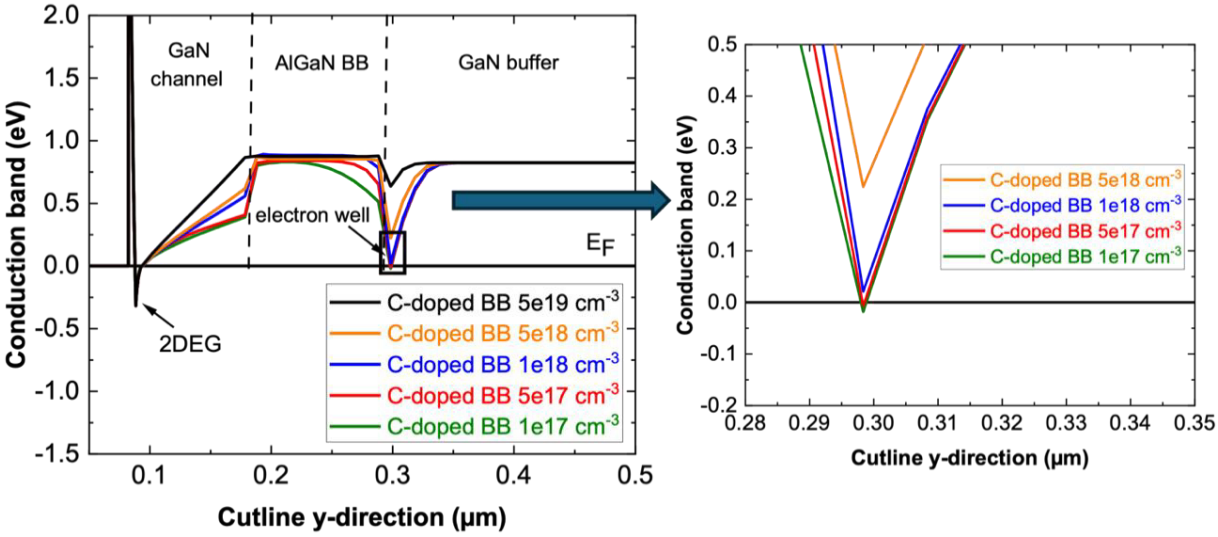


Figure 3.42. Simulated conduction band diagrams as a function of C-doping in the AlGaN back barrier

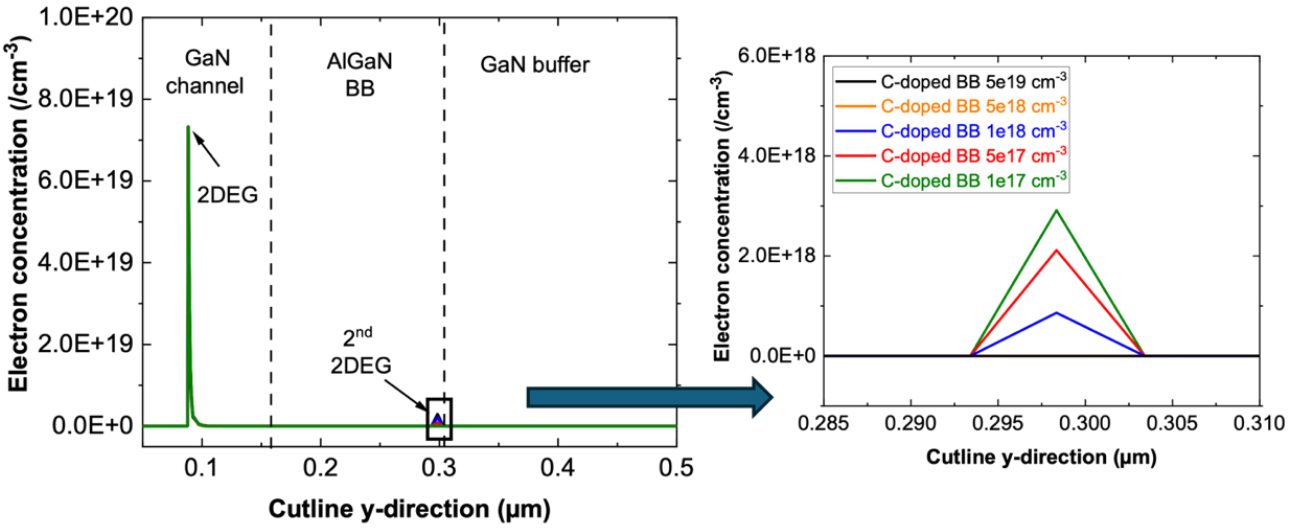


Figure 3.43. Extracted electron concentration as a function of C-doping in the AlGaN BB.

Figure 3.43 displays the extracted electron concentration for all structures. As expected, reducing the carbon concentration in the AlGaN back barrier leads to an increase in the electron density at the interface, showing the presence of a second 2DEG. At lower carbon doping levels, such as 5×10^{17} cm^{-3}, these concentrations are too weak to compensate for this 2DEG. As a result, the conduction band falls below the Fermi level. However, for C-doping above 1×10^{18} cm^{-3}, the carbon concentration can be high enough to balance the parasitic additional 2DEG.

To further verify that the 2nd 2DEG is annihilated at a specific carbon concentration level, DIBL characteristics were simulated (**Figure 3.44**). For high C-doped AlGaN back-barrier, strong electron confinement was achieved, confirming a full compensation of the 2DEG (consistent with experimental data). For a C-doping down to 1×10^{18} cm^{-3}, the DIBL remained excellent, indicating that high carbon doping > 1×10^{19} cm^{-3} is not necessarily required. For a doping concentration below 1×10^{18} cm^{-3}, a severe degradation in DIBL was observed due to the presence of the 2nd 2DEG. However, future experimental studies should focus on structures with intermediate carbon doping (mid-10^{18} cm^{-3}) to fully confirm these simulations.

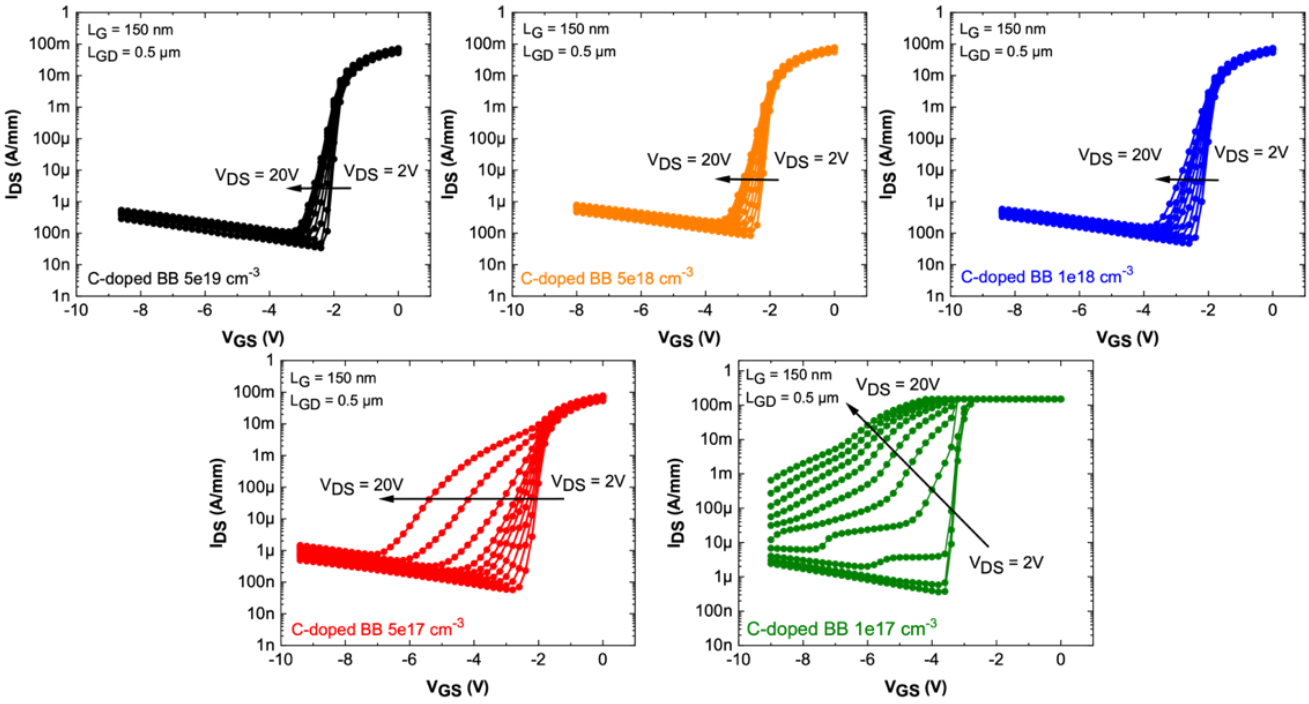


Figure 3.44. Simulated DIBL characteristics as a function of C-doping in the AlGaN back barrier of 2×25 µm transistors with L_G = 150 nm and L_{GD} = 0.5 µm.

To better understand the impact of carbon doping into the back barrier, we compared the electric field distribution and the current distribution between the high C-doped and undoped AlGaN BB structures at V_{GS} = -6V (pinch-off conditions) and V_{DS} = 20V (**Figure 3.45**). Without carbon compensation, the electric field extends down to the buffer layer due to the 2nd 2DEG. Moreover, the current distribution shows severe punch-through with a pronounced leakage path between the channel and the buffer induce by the undoped AlGaN back barrier. In contrast, for the C-doped, the electric field was confined into the GaN channel and the AlGaN back barrier and no punch-through is observed.

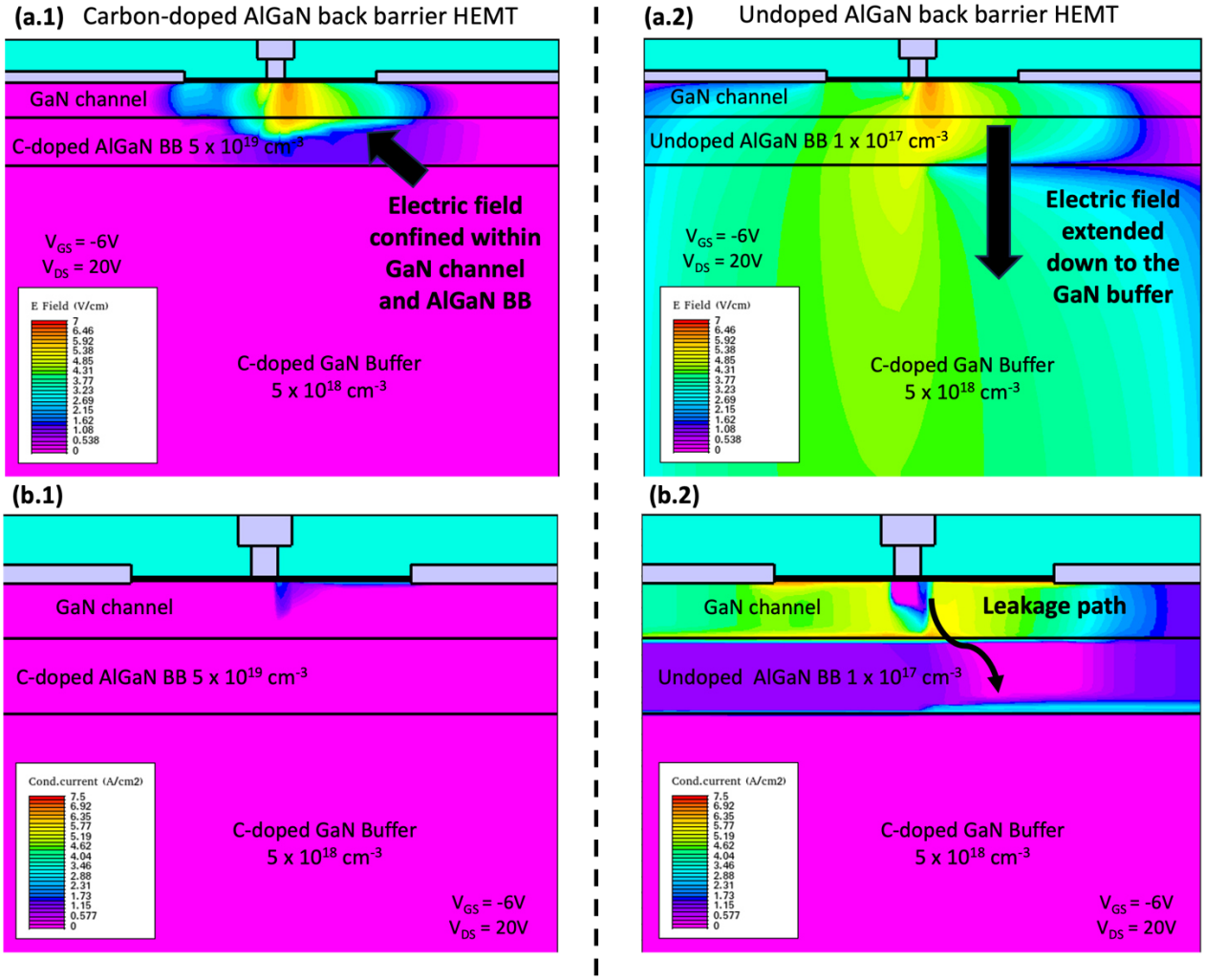


Figure 3.45. Electric field (a.1-a.2) and current distribution (b.1-b.2) profiles for the C-doped (left) and undoped (right) AlGaN back barrier structures at V_{GS} = -6V and V_{DS} = 20V (L_G = 150 nm and L_{GD} = 0.5 µm).

III.6.d. Other C-doped AlGaN back barrier trials

As part of a medium carbon-doped optimization in the AlGaN back barrier layer, two additional structures (VAR1 and VAR2) were tested with the aim of achieving a carbon concentration within the mid-10^{18} cm^{-3}. **Figure 3.46** presents the structures along with their SIMS and C-V measurements. VAR1 has a higher carbon concentration (1×10^{17} cm^{-3} and 9.5×10^{17} cm^{-3} at the interface) than the undoped BB structure but still fails to neutralize the 2DEG. For VAR2, the concentration was further increased to 1.5×10^{18} cm^{-3} at the interface. However, the carbon concentration in the back barrier remained too low (4×10^{17} cm^{-3}) to fully compensate for the 2DEG. However, an improvement has been achieved for VAR2. Indeed, the 2nd 2DEG appears to be less pronounced compared with VAR1, showing that carbon compensation has been partially effective. Precise control of carbon doping in the back barrier, while maintaining a sufficiently high Al-content during growth remains a challenge. Further iterations are still required to achieve the desired carbon concentration to further improve these types of devices.

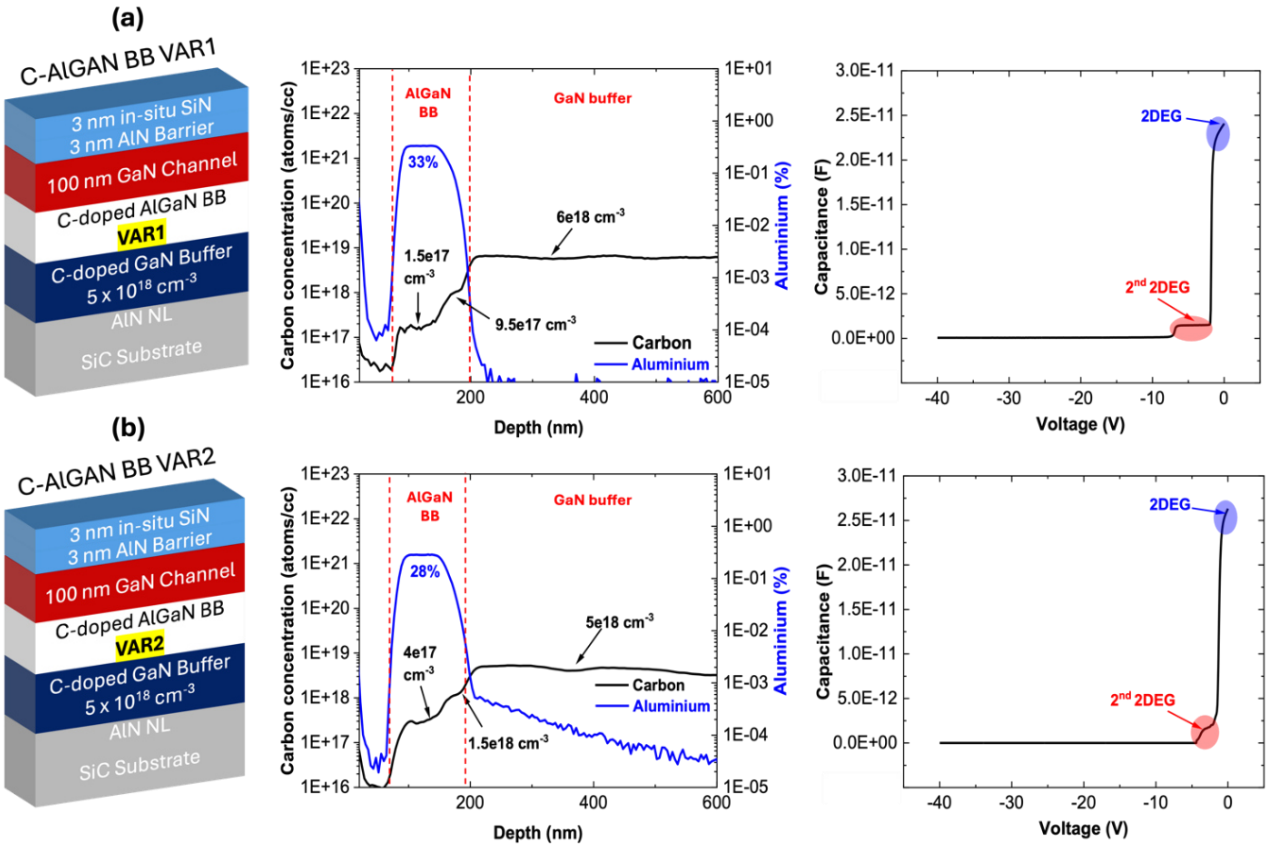


Figure 3.46. SIMS characterization and C-V measurements of VAR1 (a) and VAR2 (b)

IV. AlGaN/GaN buffer-free HEMT

IV.1. Introduction

The aim of this investigation is to evaluate the performance of AlGaN/GaN buffer-free HEMTs for mmW applications. Two structures were grown on semi-insulating SiC substrates by hot-wall MOCVD from the company SweGaN, producing a high-quality AlN nucleation layer with few dislocations/defects that allows direct growth of a GaN channel without transition layers [30] (**Figure 3.47**). The epitaxies consist of a 60 nm AlN nucleation layer, followed by a 150 nm (structure A) or 120 nm (structure B) thick GaN channel. An ultra-thin 6 nm Al-rich barrier layer with 50% Al-content, and a GaN/SiN hybrid cap layer are deposited on top. The total thickness of the epitaxies (excluding the substrate) is less than 250 nm. The absence of buffer layers is expected to significantly improve the thermal dissipation, as heat will be transferred directly to the substrate, which is advantageous for short gate length devices that induce a high electric field. However, the proximity to the substrate/AlN NL with the 2DEG may introduce drawbacks, such as trapping effects, as dopant species may be present in these regions. For this initial study, the ohmic contacts were not fully optimized, yielding contact resistance R_C values of 0.65 Ω.mm. These structures generate an electron mobility of 1350 $cm^2/V.s$ along with a 2DEG density of 1.3×10^{13} cm^{-2} and a sheet resistance (R_{sh}) of 340 ohm/sq.

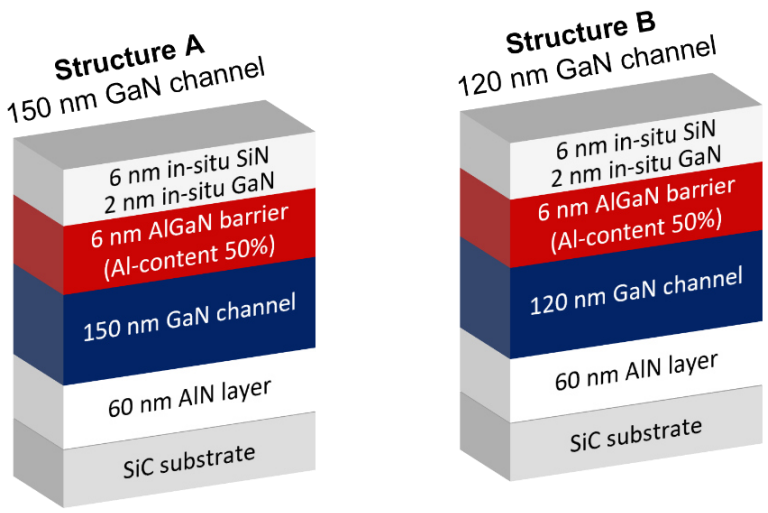


Figure 3.47. AlGaN/GaN buffer-free studied structures.

IV.2. DC and small signal characteristics

Figure 3.48 shows the IV-characteristics carried out on 2×50 µm transistors with L_G = 100 nm and L_{GD} = 0.5 µm. Both structures deliver a maximum drain current density of 0.85-0.9 A/mm (V_{GS} = +2V) with a leakage current below 100 µA/mm and a transconductance of around 330 mS/mm at V_{DS} = 10V. These values are limited by the high contact resistances (R_C = 0.65 Ω.mm). However, new attempts are planned with a reduced R_C, which should result in a maximum current density greater than 1 A/mm and a G_M above 400 mS/mm. DC-pulsed measurements reveal a current collapse of around 25% at V_{DS} = 20V. The electron trapping can be attributed to surface states as the passivation may need to be optimized and/or to the proximity with the nucleation/substrate region, where impurities / defects may be present.

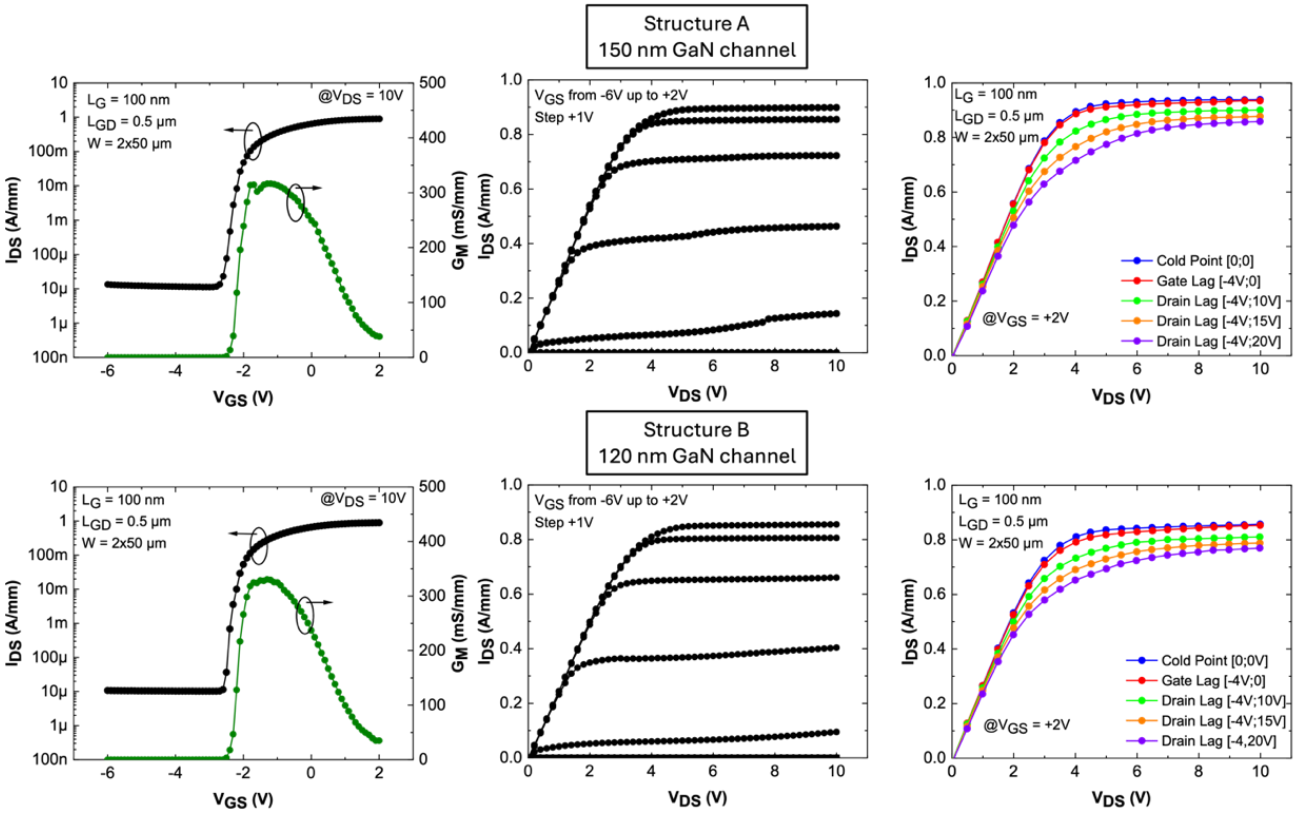


Figure 3.48. DC and DC-pulsed characteristics between structure A (top) and B (bottom) of 2×50 µm transistors with L_G = 100 nm and L_{GD} = 0.5 µm.

In order to assess the electron confinement, DIBL measurements have been performed. We observed no degradation of the leakage current up to V_{DS} = 20V with an excellent electron confinement owing to the AlN nucleation layer which remarkably acts as a back barrier (**Figure 3.49.a**).

The only difference was a slight improvement in electron confinement for the structure B (**Figure 3.49.b)** which is attributed to the thinner GaN channel. **Figure 3.49.c** summarizes the DIBL for gate length ranging from 500 nm down to 100 nm for both structures.

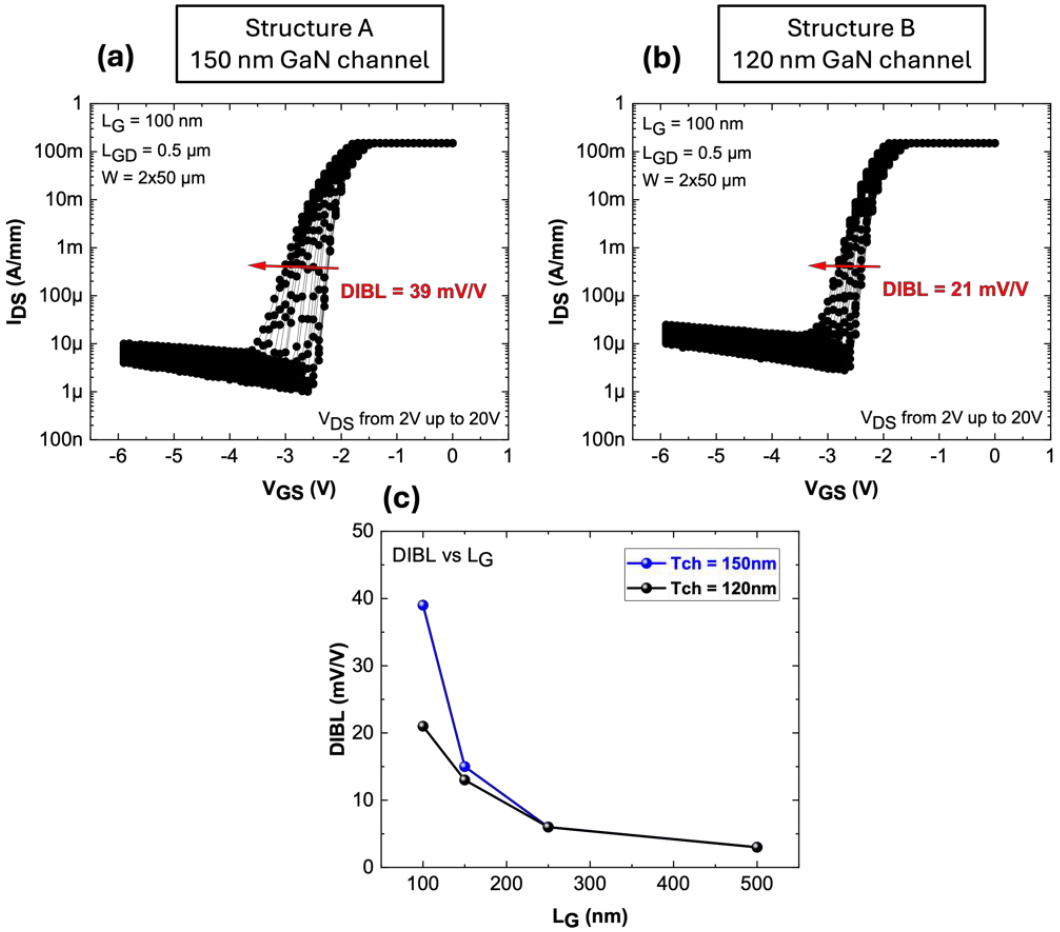


Figure 3.49. DIBL characteristics of 2×50 µm transistors with L_G = 100 nm and L_{GD} = 0.5 µm for structure A (a), structure B (b) and DIBL vs L_G (c).

Small-signal characteristics were measured, showing an F_T/F_{MAX} around 73 GHz / 290 GHz at V_{DS} = 20V. Devices also demonstrated a high-power gain of 18.5 dB at 40 GHz despite the rather high contact resistances. Both structures exhibit identical 2DEG properties, maximum drain current density, and transconductance, leading to similar performance, as presented in **Figure 3.50**.

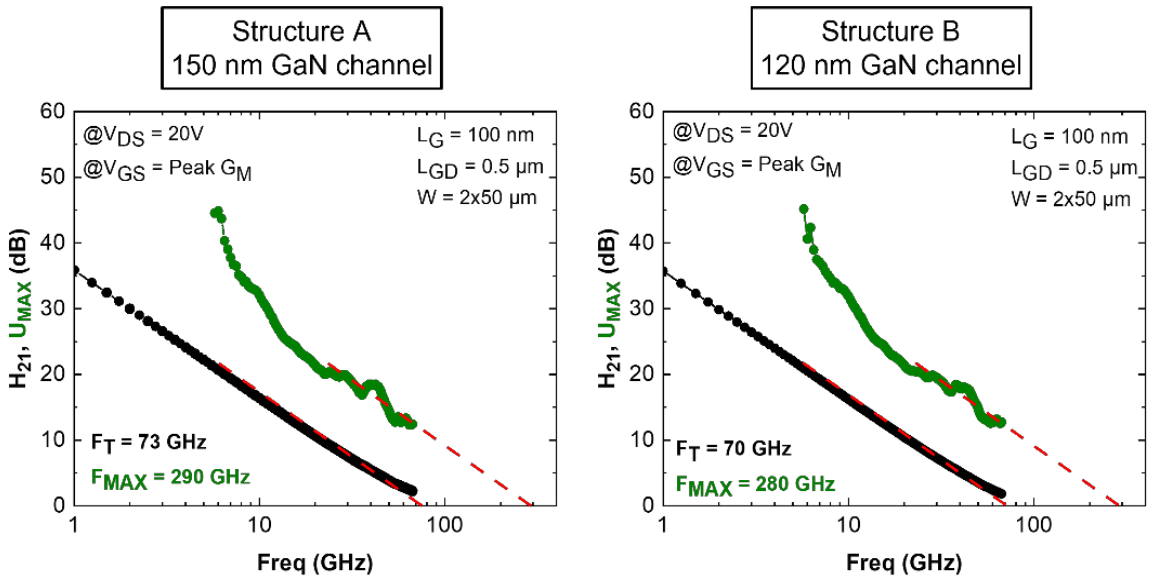


Figure 3.50. Small signal performance for structure A (left) and B (right) of 2×50 µm transistors with L_G = 100 nm and L_{GD} = 0.5 µm

IV.3. Structural characterization

IV.3.a. High Resolution Transmission Electron microscopy (HRTEM)

High-resolution transmission electron microscopy (HRTEM) and energy-dispersive X-ray spectroscopy (EDX) were performed to gain deeper insights into the AlGaN/GaN buffer-free structure. **Figure 3.51.a** presents a STEM image of structure A (150 nm GaN channel) while **Figure 3.51.b** displays a zoom at the gate/AlGaN barrier interface. We observed that few nanometers (1-2 nm) of the SiN MOCVD cap remained between the GaN cap and the gate metal, indicating that the etching process is not fully optimized. Further etch tuning needs to be conducted with an increased number of SF_6 etch cycles to suppress this interface and study its impact. **Figure 3.51.c** presents the EDX mapping of the Al-rich AlGaN barrier layer. The total thickness of the barrier is 7 nm, with a maximum Al content of 57% (slightly higher than expected). The barrier is divided into two distinct regions: an AlGaN transition layer of approximately 4.5 nm, ranging from 0 to 50%, and an Al-rich layer of 2.5 nm, extending from 50 to 57%. This type of transition has been studied and reported [31, 32]. It has been shown that for thin Al-rich AlGaN (or AlN) barriers, an AlGaN transition is typically formed due to the high growth temperature in the MOCVD process.

This configuration may also suggest that electrons are distributed across the transition rather than being confined to an abrupt interface.

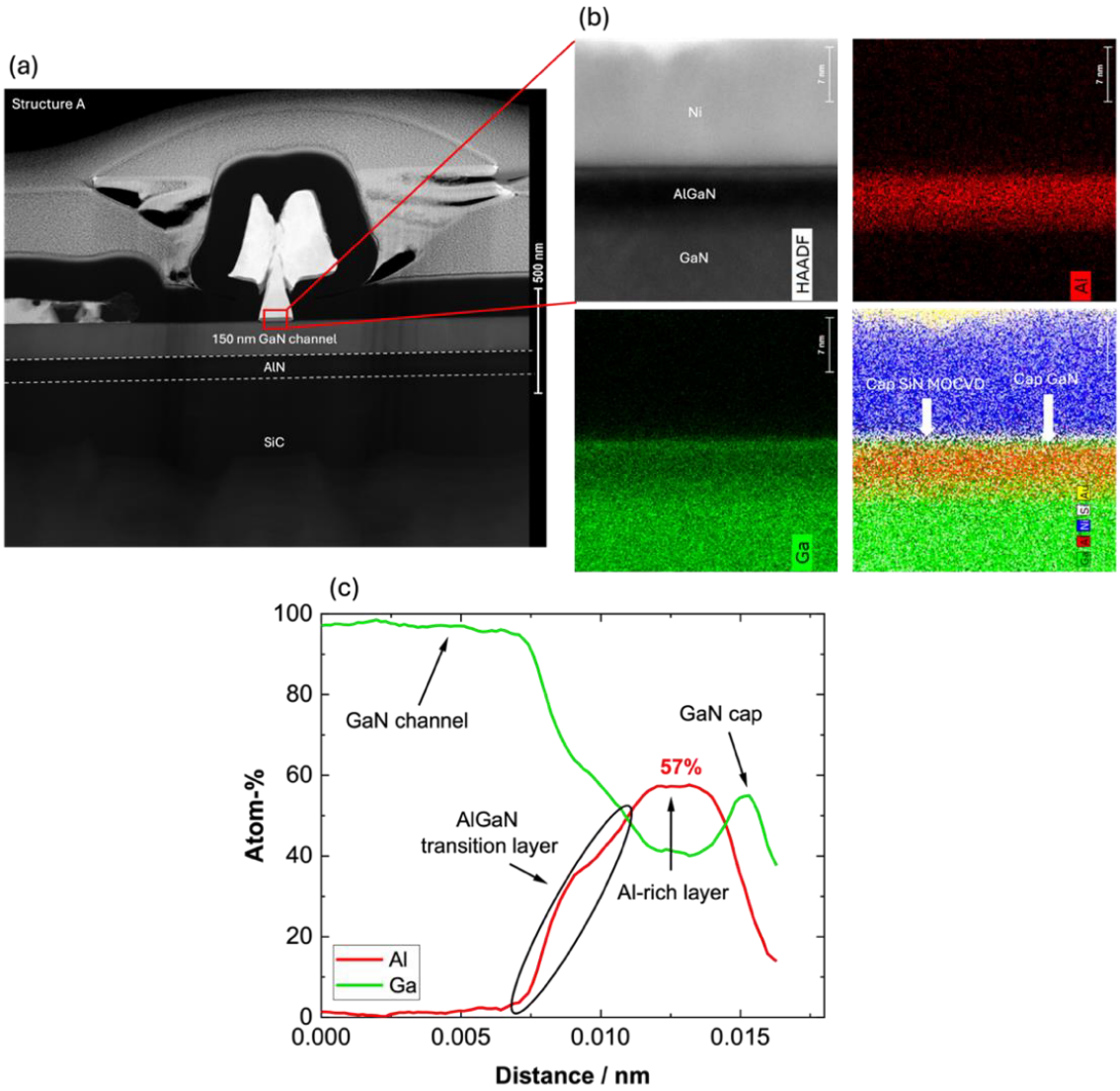


Figure 3.51. (a) STEM image of structure A, (b) zoom at the gate/barrier interface and (c) EDX mapping of the barrier region with Al and Ga-distribution.

IV.3.b. Secondary-Ion Mass Spectrometry (SIMS)

SIMS characterization was performed to detect any impurities incorporated during growth (**Figure 3.52**). For both epitaxial stacks, we detected very low concentrations of carbon, hydrogen, and oxygen in the GaN layer, indicating excellent control of the growth process. However, we noticed that oxygen is present at the GaN/AlN interface layer.

These impurities may be close enough to the GaN channel to cause trapping effects, which could explain the current collapse. It is important to note that other impurities (e.g., Vanadium dopants) or intrinsic point defects could also be present in the AlN layer or the SiC substrate [33-35].

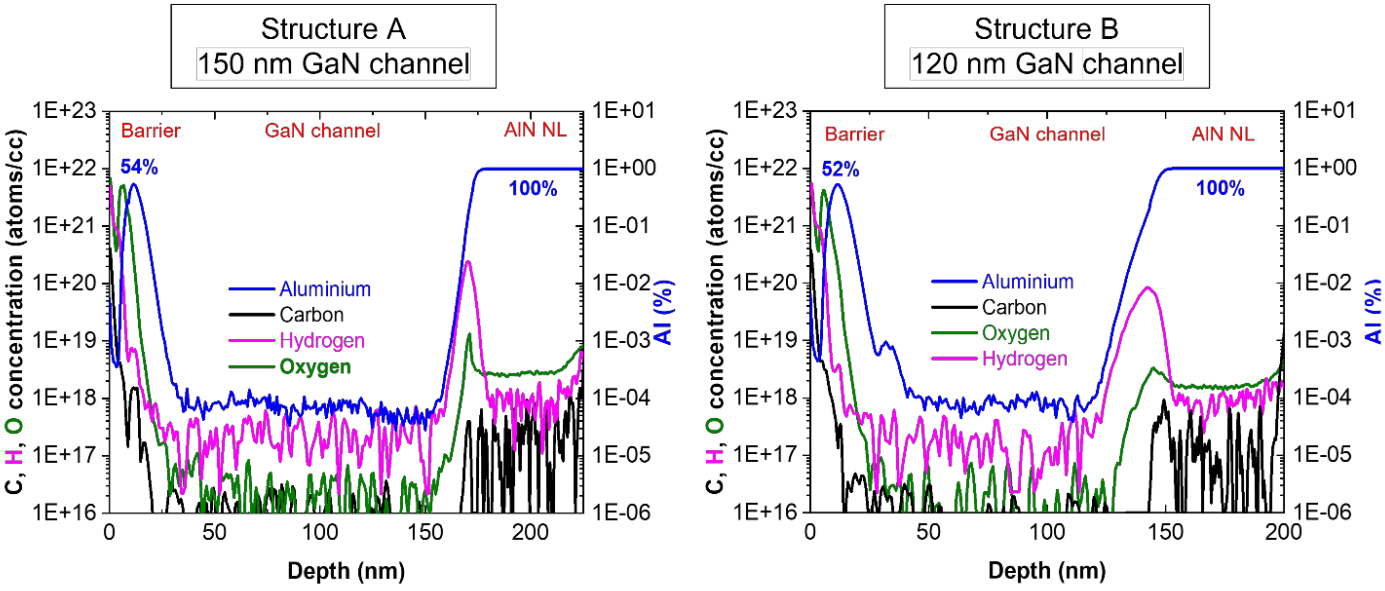


Figure 3.52. SIMS comparison between structure A (left) and B (right).

IV.4. Large signal characterization at 40 GHz

IV.4.a. Performances of 150 nm GaN channel (structure A) HEMTs

Figure 3.53 shows the CW and pulsed power performance (PAE matching, class AB 100 mA/mm) of 2×50 µm transistors with L_G = 100 nm and L_{GD} = 0.5 µm. In CW and at V_{DS} = 10V, a PAE of 50% is achieved, with a saturated power density of 1.25 W/mm (**Figure 3.56.a**). In pulsed mode, the PAE increases to 56.5% with a corresponding P_{OUT} of 1.30 W/mm. The higher pulsed PAE is expected from the reduction of trapping effects. At V_{DS} = 20V (CW), PAE was 44.5% with a P_{OUT} of 2.4 W/mm, while in pulsed mode, the PAE increases to 50%, and the P_{OUT} reaches 2.60 W/mm (**Figure 3.53.b**). Additionally, IV-characteristics after load-pull measurements (**Figure 3.53.c**) indicate no degradation in leakage current up to V_{DS} = 20V.

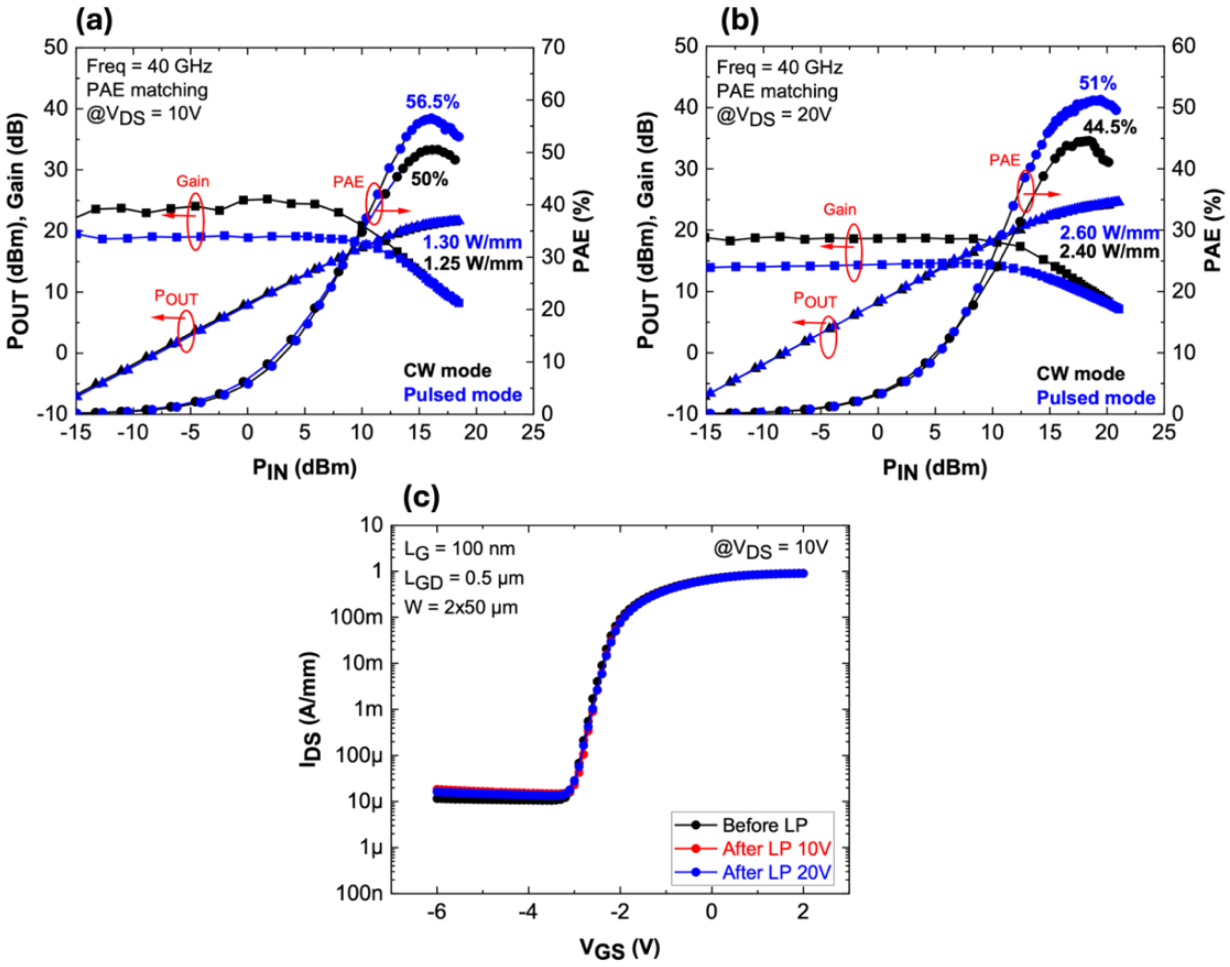


Figure 3.53. CW and pulsed power performance of structure A at (a) V_{DS} = 10V, (b) 20V and (c) $I_D V_G$ before/after load pull sweeps (L_G = 100 nm and L_{GD} = 0.5 µm).

IV.4.b. Performance of 120 nm GaN channel (structure B) HEMTs

Similarly, the power performance of structure B was evaluated using the same transistor design, resulting in comparable results. At V_{DS} = 10V (**Figure 3.54.a**), the PAE was 48.2% in CW and 55% in pulsed mode, with an output power of 1.25 W/mm and 1.20 W/mm, respectively. At V_{DS} = 20V (**Figure 3.54.b**), the measured PAE was 43.5% in CW and 47% in pulsed mode, with corresponding P_{OUT} of 2.10 W/mm and 2.35 W/mm, respectively. To assess the robustness at higher bias, several sweeps were performed at V_{DS} = 30V (**Figure 3.54.c**). The PAE was 36% and the output power 3.6 W/mm. No significant degradation of the transistor was observed, except for a slight increase in leakage current, induced by the high electric field associated with the short gate length (**Figure 3.54.d**).

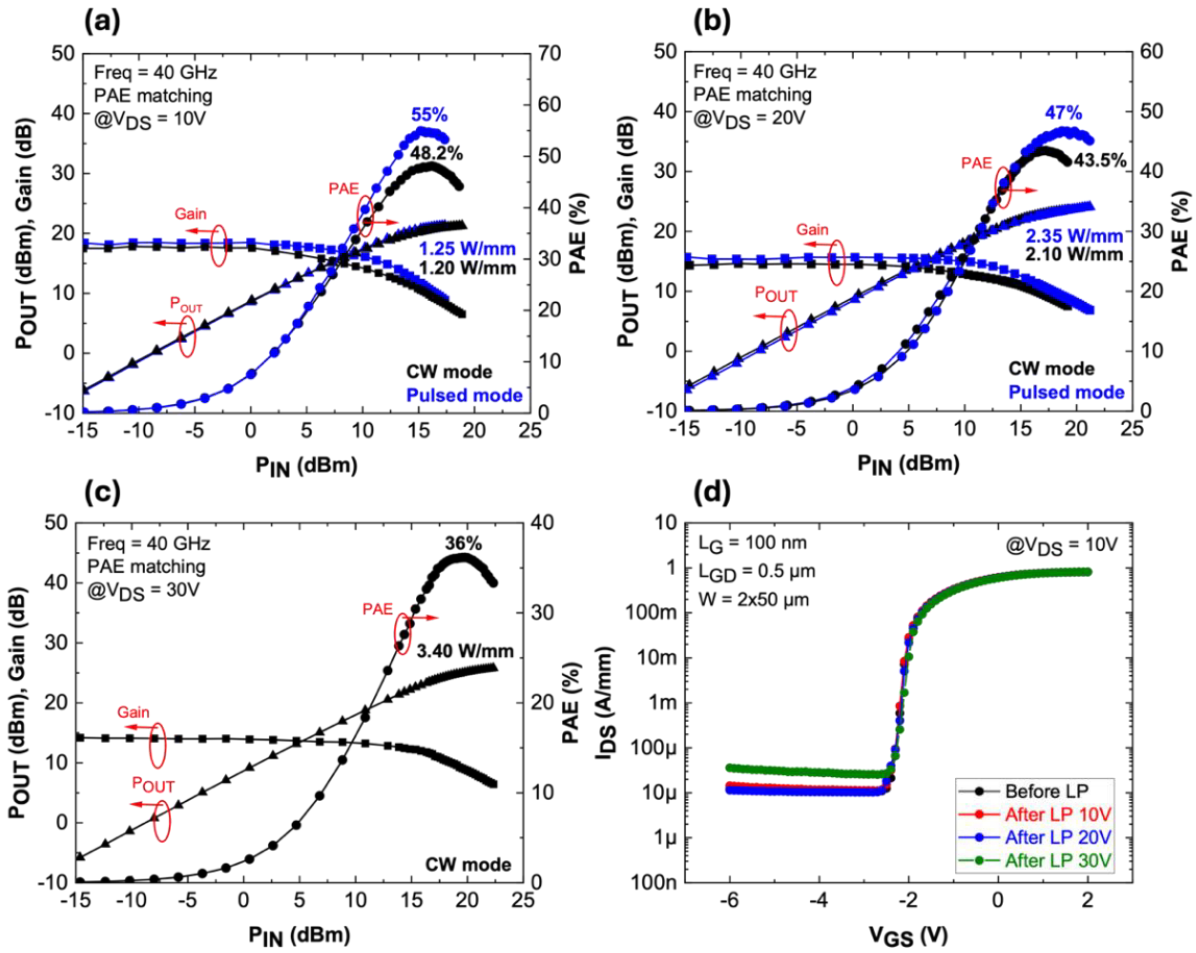


Figure 3.54. CW and pulsed power performance of structure B at (a) V_{DS} = 10V, (b) 20V, (c) 30V and (d) I_DV_G before/after (L_G = 100 nm and L_{GD} = 0.5 µm).

Despite the rather conservative power performance due to high contact resistances, these results highlight the potential of AlGaN/GaN buffer-free HEMTs for future high-frequency applications. Further efforts will focus on reducing contact resistances to fully unlock the potentialities of this technology. Moreover, short-term reliability of these structures also needs to be evaluated, which will be the subject of the next section.

IV.5. Short-term high temperature operating life test at 40 GHz

An initial reliability assessment was carried out by performing on-wafer, short-term HTOL tests without device packaging. However, the exact conditions to fix T_J = 250°C for this structure were unknown. As a starting point, we used the same conditions that were applied to the AlGaN back-barrier structure described previously: Freq = 40 GHz, V_{DS} = 20V, I_D = 225 mA/mm and T_{chuck} = 150°C.

It is important to recall that for buffer-free HEMTs, the thermal dissipation is improved due to the absence of thick buffer layers. Consequently, these conditions may not be sufficient to achieve a junction temperature of 250°C. Prior to the test, load pull measurements were carried out under these conditions to detect any early failures in both structures. **Figure 3.55** displays the IV characteristics before and after load pull sweeps performed on 2×50 µm transistors with L_G = 150 nm and L_{GD} = 1.5 µm.

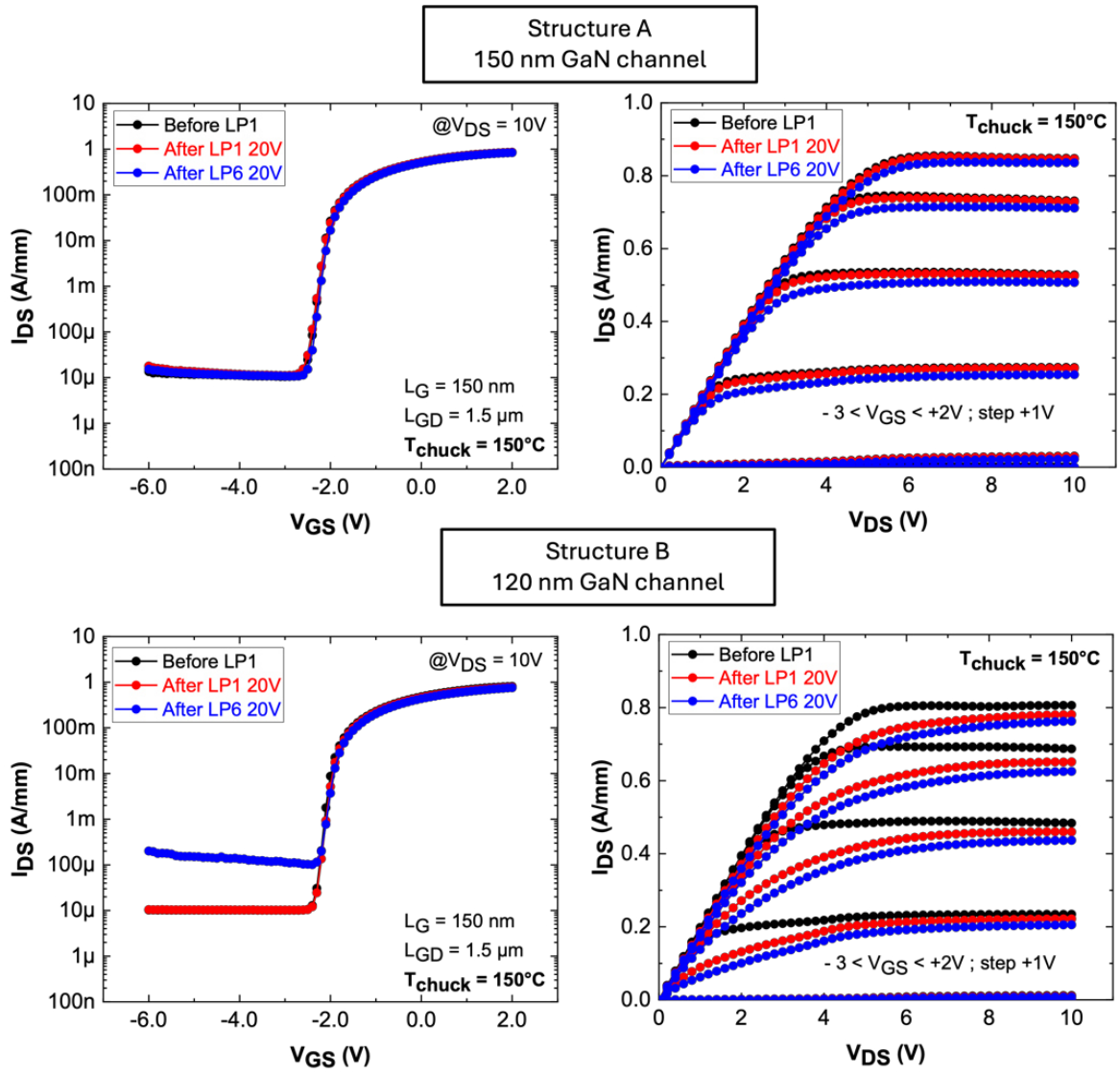


Figure 3.55. IV characteristics before/after load-pull sweeps under V_{DS} = 20V, I_{DS} = 225 mA/mm and T_{chuck} = 150°C for structure A (top) and B (bottom).

Structure B (120 nm GaN channel) exhibited a significant degradation after several load-pull sweeps, including an increase in leakage current and degraded R_{ON}. This was unexpected, given that structure B offers an even better electron confinement than structure A and showed no signs of degradation up to V_{DS} = 30V (**Figure 3.54**).

The reasons for this deterioration are still under investigation, but one possible explanation could be related to epitaxy. With a 120 nm GaN channel, the 2DEG can be too close to the nucleation layer, and defects can be thermally activated under these conditions, leading to the observed degradation. Structure A showed no degradation under the same conditions, so the short-term HTOL test was performed on this structure. **Figure 3.57** shows the P_{OUT}, PAE, I_{GS} and I_D monitoring as a function of time for 7.5-hours HTOL conducted on 2×50 µm transistors with L_G = 125 nm and L_{GD} = 1.5 µm (Structure A). The PAE, P_{OUT} and I_{GS} remained constant across the entire test with only a slight decrease in I_D, which suggests promising long-term reliability.

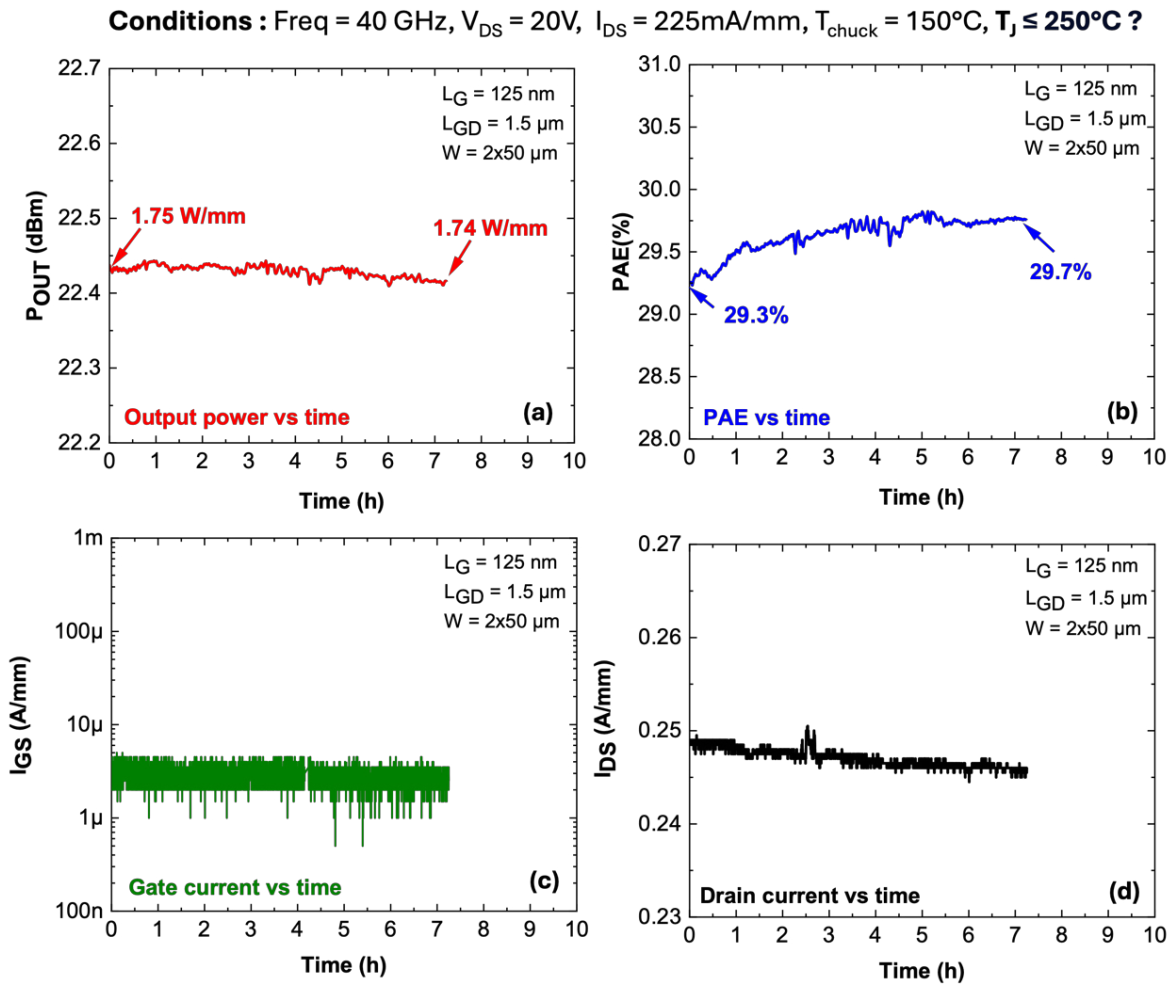


Figure 3.57. HTOL test for 7.5 hours monitoring (a) P_{OUT}, (b) PAE, (c) I_{GS} and (d) I_{DS} vs time.

Figure 3.58 presents the I-V characteristics before and after the 7.5-hours HTOL test. We observed that the leakage current did not deteriorate. However, we identified a positive threshold voltage shift of +0.5V (**Figure 3.58.a**).

The ON resistance remained unchanged, with the same maximum current density at V_{GS} = +2V. Nevertheless, at lower V_{GS}, the current density decreases, which is linked to the V_{TH} shift. (**Figure 3.58.b**). A positive shift in the threshold voltage introduces stability issues for a device. In fact, this change results in a decrease in the bias current, which in turn leads to a change in the operating class. With regards to electron trapping, a slight increase in drain lag at V_{DS} = 20V was observed (**Figure 3.58.c**).

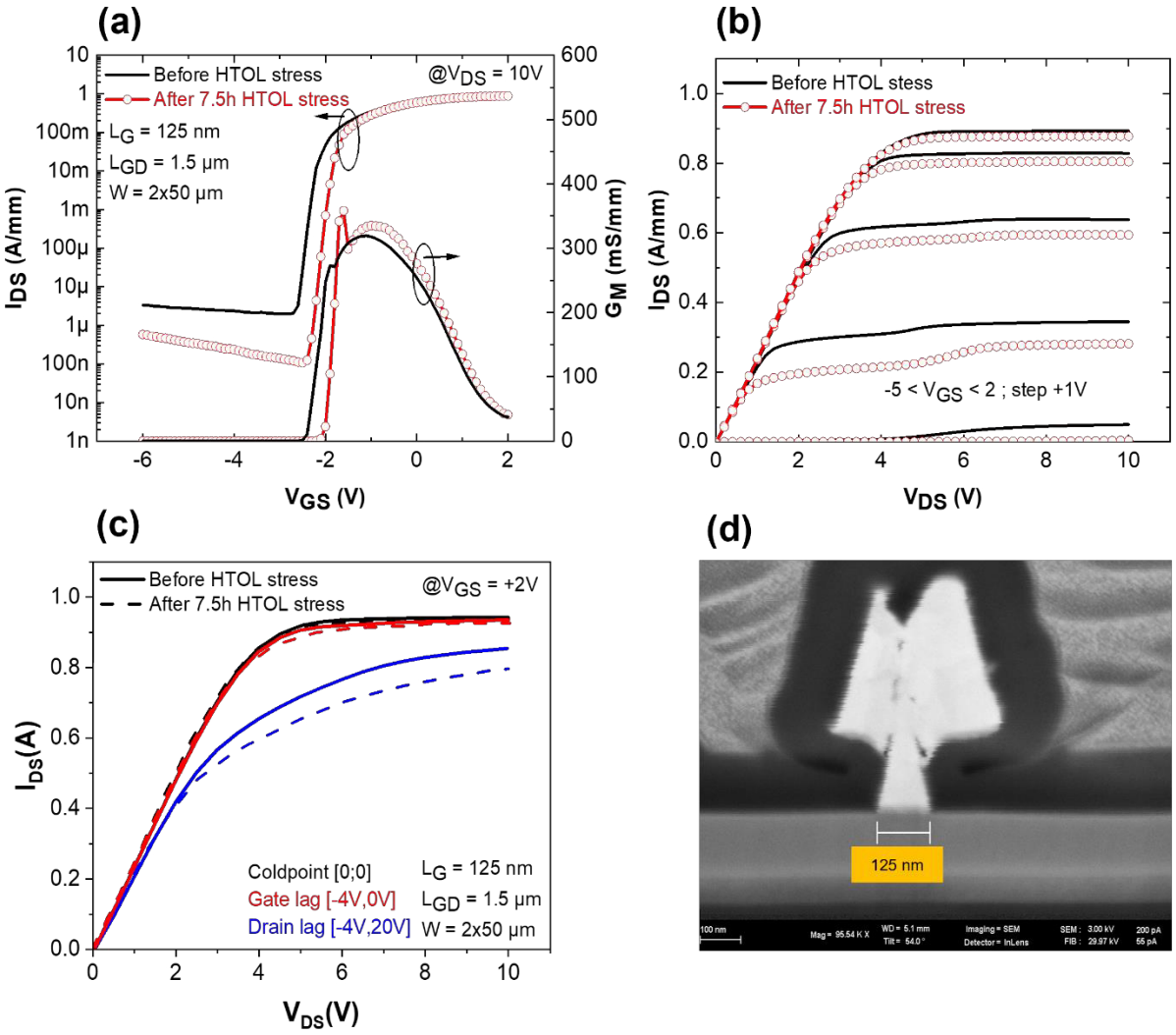


Figure 3.58. I_DV_G (a), I_DV_D (b) and DC-pulsed (c) characteristics before and after 7.5 hours of HTOL test.

To further investigate the impact of this stress, HRTEM and EDX characterizations of the device post-stress were carried out. **Figure 3.59** shows HAADF and EDX images of the gate region. We noticed a significant degradation at both gate edges down to the AlGaN barrier layer. Pitlike or void defects appeared to a depth of approximately 4 nm into the barrier layer, indicating substantial damages.

Moreover, we observed Au diffusion thought the SiN sidewalls, with some Ga atoms intermixing that damages the AlGaN barrier layer. This physical degradation was unexpected, given that we did not observe major electrical degradation during the stress test. However, during a prolonged period of stress (several hundreds of hours), these defects may lead to device failure. Such material degradation has been reported in the literature [36-40]. Indeed, pits or cracks can be caused by the reverse piezoelectric effect of the AlGaN layer, crystallographic defects or electrochemical reactions at the surface with oxygen, which will modify the metal/semiconductor interface. The deterioration of the barrier layer can be linked to the positive shift of V_{TH}, the slight increase in trapping, and the slight drop in drain current during the stress. These phenomena are driven by the high electric field at the gate edge and thermally amplified by the high junction temperature.

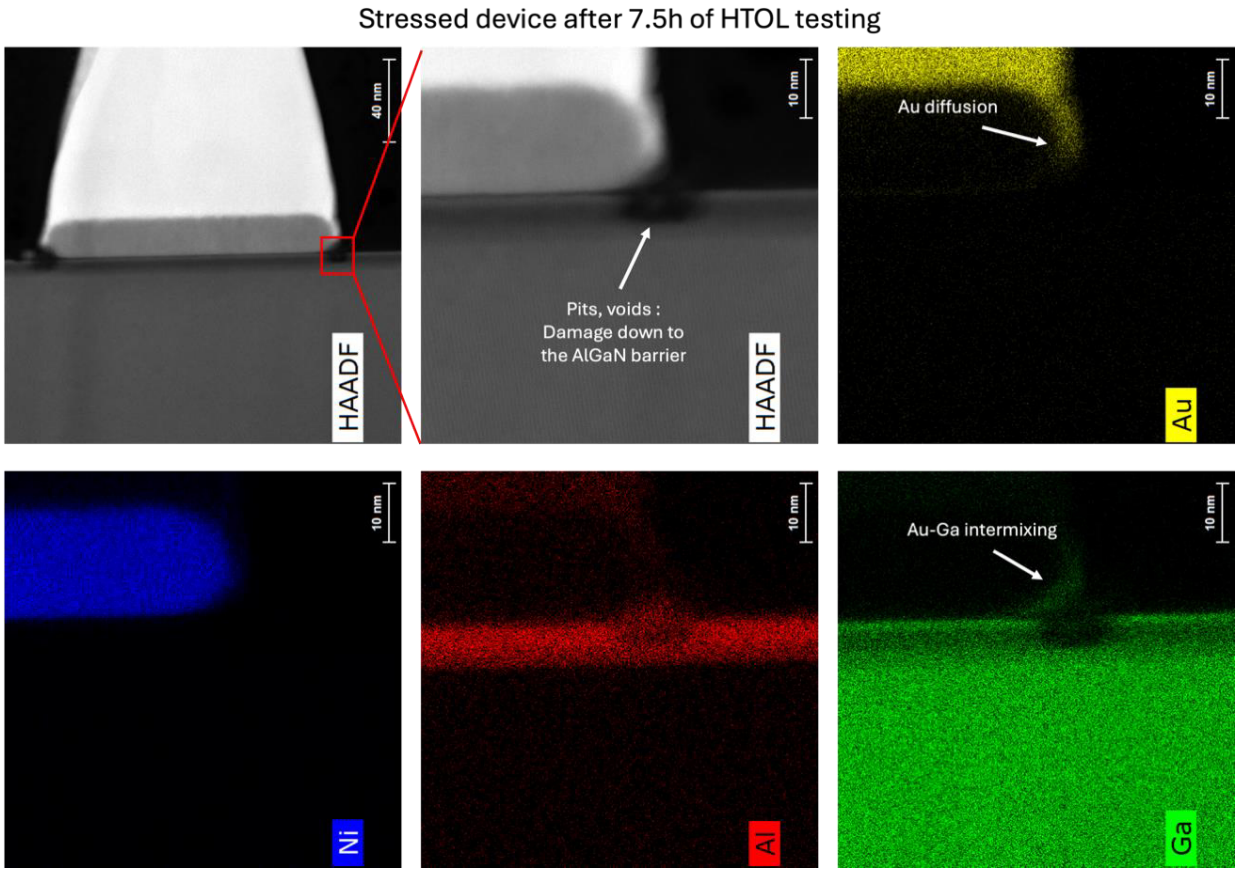


Figure 3.59. STEM and EDX images in the gate region after 7.5 hours HTOL stress.

Since we did not have the exact conditions required to fix T_J = 250°C, those used previously might yield in lower-than-expected T_j knowing that the thermal dissipation is certainly higher for the buffer-free heterostructure.

Therefore, to increase the junction temperature of to explore the device's robustness limits, we performed another HTOL test, but with T_{chuck} set at 180°C. **Figure 3.60** displays the results of 8-hours HTOL testing. Under these conditions, we observed a different device behavior compared to the previous test performed at T_{chuck} = 150°C. The PAE and P_{OUT} decreased linearly, the gate leakage current increased with a sudden jump at the end of the test, and we noted a significant decrease in the drain current I_D. This suggests that these conditions result in a critical junction temperature exceeding the limits of these devices. Nevertheless, it will be essential to assess the junction temperature of this structure in order to validate these results.

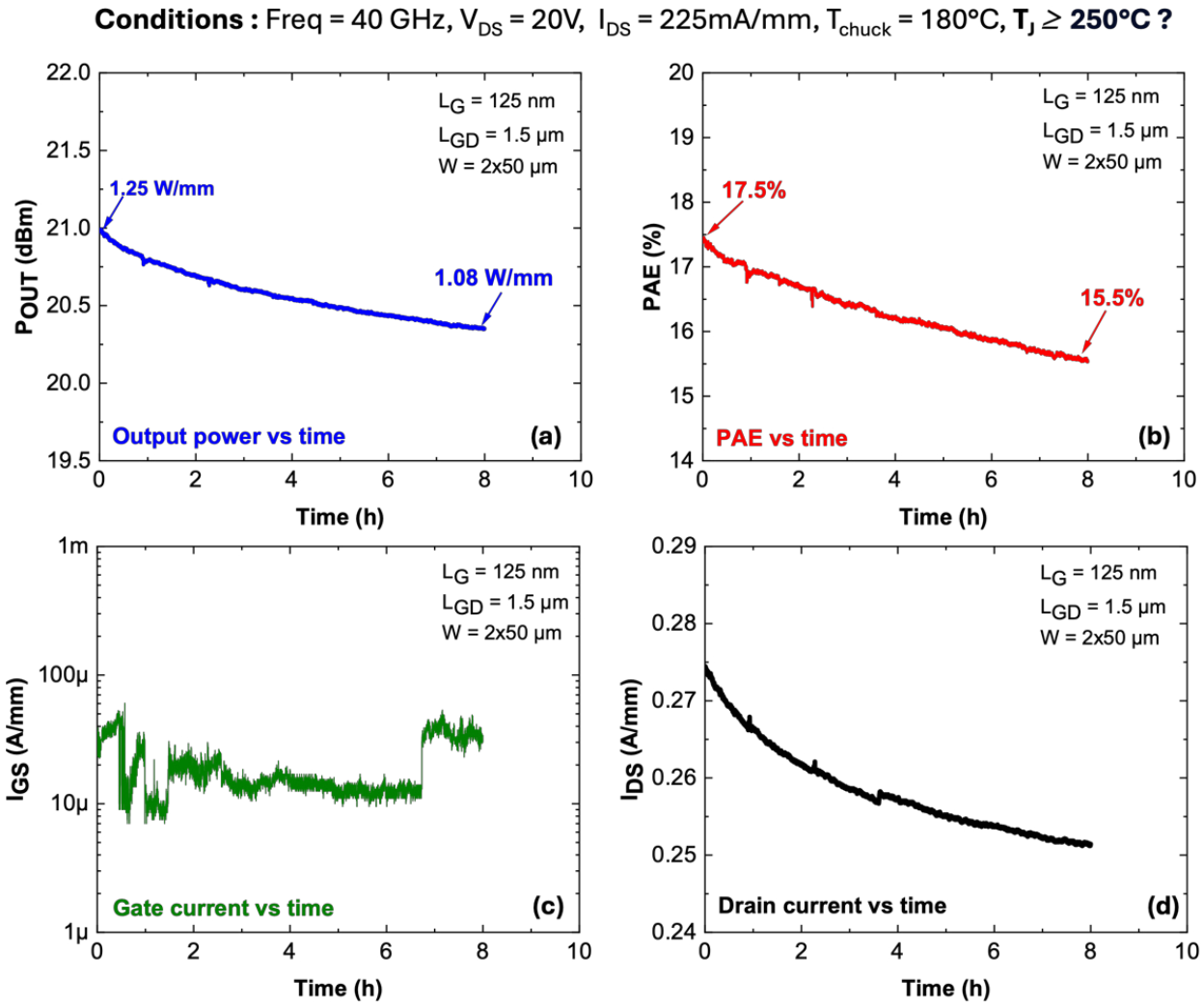


Figure 3.60. HTOL test for 8 hours monitoring (a) P_{OUT}, (b) PAE, (c) I_{GS} and (d) I_D vs time.

Figure 3.61 shows the IV characteristics before and after the 8-hours HTOL test. As in the previous test, we found a positive shift in V_{TH}, but this time accompanied by an increase in leakage current.

In addition, R_{ON} is slightly degraded, with a decrease in maximum drain current density. Under these conditions, a significant increase in current collapse at V_{DS} = 20V was noted compared to the initial DC-pulsed characteristics. These electrical degradations suggest that the high junction temperature may be the cause of the gate metal and barrier layer deterioration.

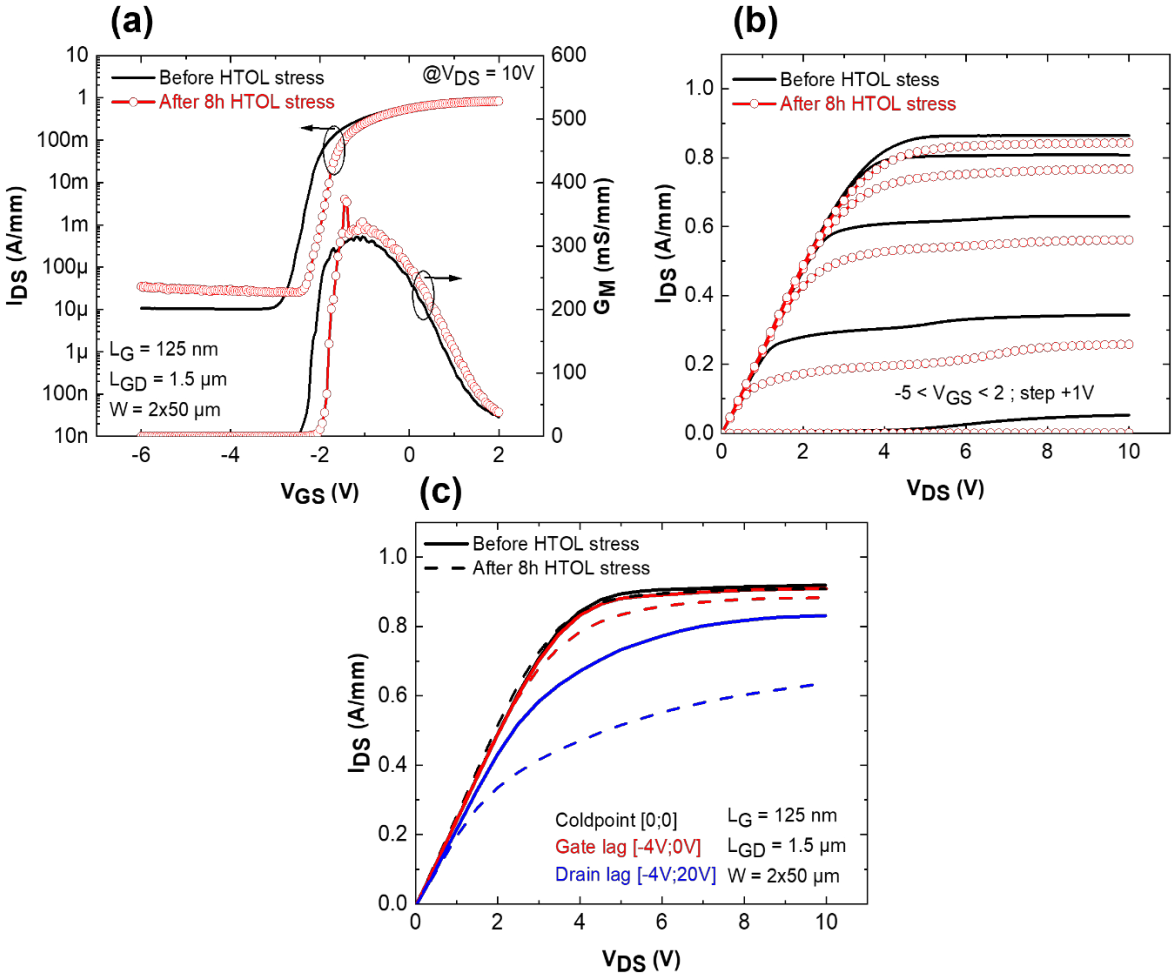


Figure 3.61. I_DV_G (a), I_DV_D (b) and DC-pulsed (c) characteristics before and after 8 hours of HTOL test.

With the aim of correlating the decrease of DC and power characteristics with the gate module and barrier layer degradation, we also performed HRTEM analysis on the device subjected to the HTOL stress test (**Figure 3.62**). We observed the same type of degradation as in the previous stress test, but more pronounced. In fact, there is a more significant Au diffusion, which spreads further laterally down to the gate foot. The formation of an Au-Ga alloy is also more pronounced, and the barrier layer is damaged with noticeable voids. We can therefore deduce that the drop in performance during the HTOL test is linked to these degradations, which are strongly exacerbated by the junction temperature and the high electric field.

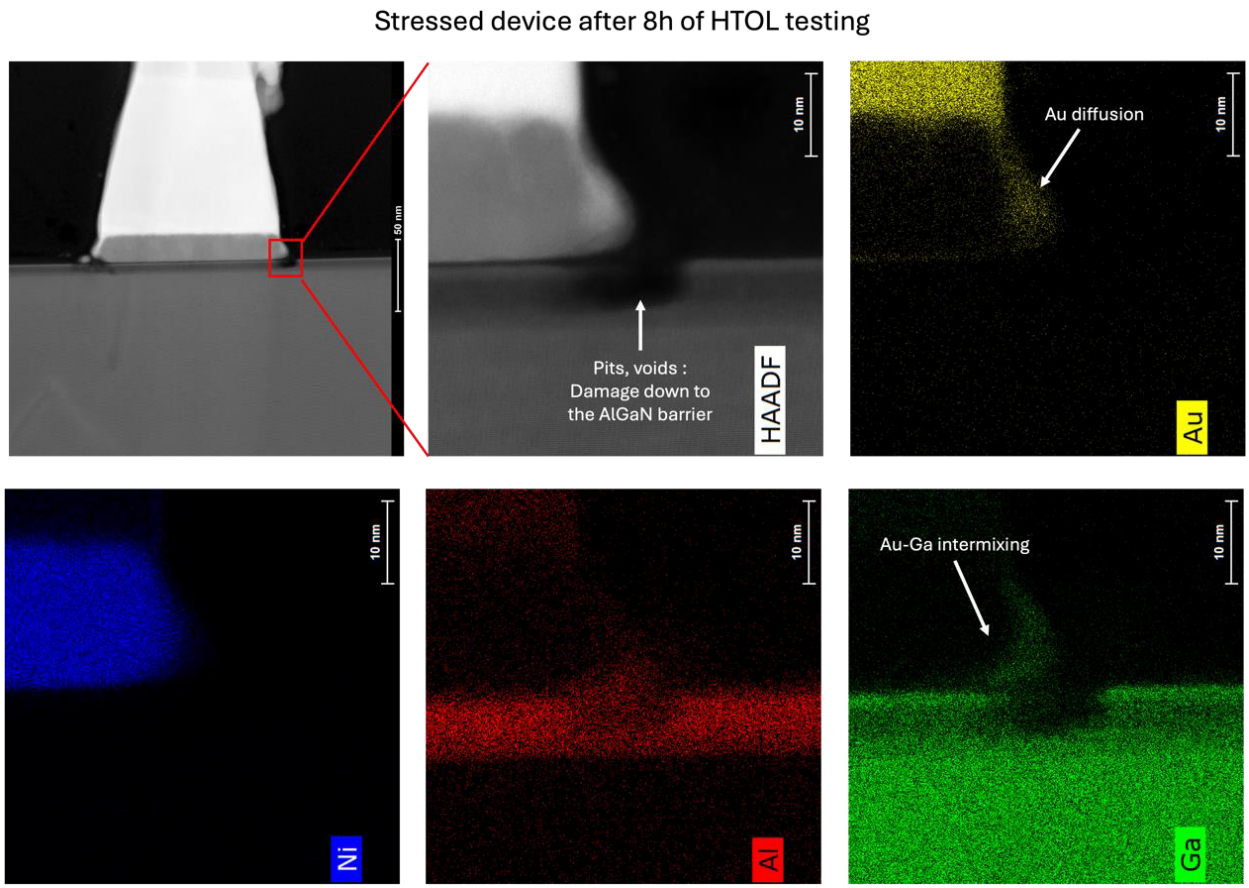


Figure 3.62. STEM and EDX images in the gate region after 8 hours HTOL stress

It is important to emphasize the fact that we did not detect exactly the same type of degradation in AlGaN/GaN buffer-free HEMTs (Au diffusion and barrier damage) as in AlGaN back-barrier HEMTs (SiN delamination and Ni degradation). Although the structures studied in this chapter are completely different and sourced from different suppliers, they share a common fabrication process (with some minor adjustments based on the heterostructures). The degradations strongly indicate a failure of the gate module or passivation layer induced by a high electric field and high junction temperatures. It is therefore crucial to consider ways to minimize or prevent these effects to improve the reliability. For instance, some studies have focused on optimizing the gate module by adjusting the foot height or gate shape to better control the electric field compare with conventional T-gate, especially in short gate-length devices [41-43]. Other studies propose to change the metal composition of the gate contact, using other alloys such as iridium [41, 44, 45] or TiN [46, 47] instead of nickel to prevent gold diffusion. Finally, post gate annealing may also improve metal stability and prevent its degradation, thus improving the overall device reliability [41, 48, 49]. However, it is essential to ensure that optimizations for reliability are not made at the expense of device performance.

V. Conclusion chapter 3

The demonstration of high performance at high-frequency for GaN technologies is linked not only to advanced epitaxy, but also to the fabrication process, especially of the device reliability figure of merit is considered. This chapter begins with an overview of the mask set and fabrication steps used in this work. To enhance the device performance, optimizing ohmic and gate contacts is essential. Reducing the contact resistances is crucial to improve the maximum current density, which requires careful engineering. At the same time, the fabrication of the gate module for high-frequency operation is the subject of critical development. It is important to ensure an appropriate and reliable design that delivers excellent RF performances, while reducing parasitic elements and control the electric field, especially with short gate length devices. This chapter continues with the study of AlN/GaN/AlGaN back-barrier HEMTs. Inserting a carbon-doped AlGaN back barrier with optimized Al-content effectively prevents short-channel effects, reduces trapping, and ensures excellent electron confinement with short gate length transistors. Despite a high carbon concentration ($> 1\times10^{19}$ cm^{-3}) in the AlGaN back barrier, rather low electron trapping effects are observed resulting in state-of-the-art Q-band power performance. However, a drastic reduction in carbon concentration in this layer led to the formation of a second 2DEG at the back barrier/GaN buffer interface, which severely compromised the device performance. TCAD simulations indicate that excessive carbon doping is not necessarily required to address this problem but achieving controlled carbon concentration in the mid-10^{18} cm^{-3} during growth remains a challenge.

An initial reliability study of the structure was performed using short-term HTOL test. The AlGaN back-barrier structure is highly sensitive to the conditions applied at a given junction temperature, which must be accurately measured. HRTEM analyses revealed more failures related to processing, which are accelerated under high electric field and high junction temperatures, rather than issues with the epitaxy itself. This chapter is completed with a study of buffer-free AlGaN/GaN HEMTs. It has been demonstrated that buffer-free devices can be a competitive alternative for future millimeter-wave applications. Excellent electron confinement without any doping compensation, low leakage current, and promising power performance at 40 GHz have been presented. However, further investigations are still needed with optimized ohmic contacts to fully evaluate their potentialities.

Initial short-term reliability measurements also show promising results for these structures, reflecting the improved thermal dissipation. Nevertheless, the junction temperature must be also assessed accurately under the given conditions. Finally, HRTEM also revealed some fabrication-related failures. Careful optimization of the gate module should be explored in the future to improve the overall device reliability.

References chapter 3

[1] A. C. Schmitz, A. T. Ping, M. A. Khan, Q. Chen, J. W. Yang, et I. Adesida, « Metal contacts to n-type GaN », *Journal of Elec Materi*, vol. 27, nº 4, p. 255-260, avr. 1998, doi: 10.1007/s11664-998-0396-5.

[2] L. Song *et al.*, « Influence factors and temperature reliability of ohmic contact on AlGaN/GaN HEMTs », *AIP Advances*, vol. 8, nº 3, p. 035213, mars 2018, doi: 10.1063/1.5024803.

[3] B. Benakaprasad, A. M. Eblabla, X. Li, K. G. Crawford, et K. Elgaid, « Optimization of Ohmic Contact for AlGaN/GaN HEMT on Low-Resistivity Silicon », *IEEE Trans. Electron Devices*, vol. 67, nº 3, p. 863-868, mars 2020, doi: 10.1109/TED.2020.2968186.

[4] M. W. Fay *et al.*, « Structural and electrical characterization of AuPdAlTi ohmic contacts to AlGaN⁄GaN with varying Ti content », *Journal of Applied Physics*, vol. 96, nº 10, p. 5588-5595, nov. 2004, doi: 10.1063/1.1796514.

[5] S. S. Mahajan, A. Dhaul, R. Laishram, S. Kapoor, S. Vinayak, et B. K. Sehgal, « Micro-structural evaluation of Ti/Al/Ni/Au ohmic contacts with different Ti/Al thicknesses in AlGaN/GaN HEMTs », *Materials Science and Engineering: B*, vol. 183, p. 47-53, avr. 2014, doi: 10.1016/j.mseb.2013.12.005.

[6] M. Meer, A. Rawat, K. Takhar, S. Ganguly, et D. Saha, « Interface dynamics in ohmic contact optimization on AlGaN/GaN heterostructure by the formation of TiN », *Microelectronic Engineering*, vol. 219, p. 111144, janv. 2020, doi: 10.1016/j.mee.2019.111144.

[7] C. J. Lu, A. V. Davydov, D. Josell, et L. A. Bendersky, « Interfacial reactions of TiÕn-GaN contacts at elevated temperature », *J. Appl. Phys.*, vol. 94, nº 1, 2003.

[8] S. Ruvimov *et al.*, « Microstructure of Ti/Al and Ti/Al/Ni/Au Ohmic contacts for *n* -GaN », *Applied Physics Letters*, vol. 69, nº 11, p. 1556-1558, sept. 1996, doi: 10.1063/1.117060.

[9] B. Van Daele *et al.*, « Mechanism for Ohmic contact formation on Si3N4 passivated AlGaN⁄GaN high-electron-mobility transistors », *Applied Physics Letters*, vol. 89, nº 20, p. 201908, nov. 2006, doi: 10.1063/1.2388889.

[10] Z. Fan, S. N. Mohammad, W. Kim, Ö. Aktas, A. E. Botchkarev, et H. Morkoç, « Very low resistance multilayer Ohmic contact to *n* -GaN », *Applied Physics Letters*, vol. 68, nº 12, p. 1672-1674, mars 1996, doi: 10.1063/1.115901.

[11] B. Van Daele, G. Van Tendeloo, W. Ruythooren, J. Derluyn, M. R. Leys, et M. Germain, « The role of Al on Ohmic contact formation on n-type GaN and AlGaN/GaN », *Applied Physics Letters*, vol. 87, nº 6, p. 061905, août 2005, doi: 10.1063/1.2008361.

[12] X. Kong, K. Wei, G. Liu, et X. Liu, « Role of Ti/Al relative thickness in the formation mechanism of Ti/Al/Ni/Au Ohmic contacts to AlGaN/GaN heterostructures », *J. Phys. D: Appl. Phys.*, vol. 45, nº 26, p. 265101, juill. 2012, doi: 10.1088/0022-3727/45/26/265101.

[13] Q. Feng, L.-M. Li, Y. Hao, J.-Y. Ni, et J.-C. Zhang, « The improvement of ohmic contact of Ti/Al/Ni/Au to AlGaN/GaN HEMT by multi-step annealing method », *Solid-State Electronics*, vol. 53, nº 9, p. 955-958, sept. 2009, doi: 10.1016/j.sse.2009.06.002.

[14] Y. Zhu, W. Cao, Y. Fan, Y. Deng, et C. Xu, « Effects of rapid thermal annealing on ohmic contact of AlGaN/GaN HEMTs », *J. Semicond.*, vol. 35, nº 2, p. 026004, févr. 2014, doi: 10.1088/1674-4926/35/2/026004.

[15] K. Harrouche, « Design and fabrication of GaN-based field effect power transistors up to W-band », Lille, 2021.

[16] M. Murthy, J. A. Freitas, J. Kim, E. R. Glaser, et D. Storm, « Residual impurities in GaN substrates and epitaxial layers grown by various techniques », *Journal of Crystal Growth*, vol. 305, nº 2, p. 393-398, juill. 2007, doi: 10.1016/j.jcrysgro.2007.03.029.

[17] C. G. van de Walle, C. Stampfl, et J. Neugebauer, « Theory of Doping and Defects in III-V Nitrides », *Journal of Crystal Growth*, vol. 189-190, p. 505-510, juin 1998, doi: 10.1016/S0022-0248(98)00340-6.

[18] J. A. Carter, J. Acord, D. Hoffmann, A. Trageser, et C. Pagel, « Thermal factors influencing the reliability of GaN HEMTs », in *2012 28th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)*, San Jose, CA, USA: IEEE, mars 2012, p. 182-188. doi: 10.1109/STHERM.2012.6188847.

[19] L. Baczkowski *et al.*, « Thermal Characterization Using Optical Methods of AlGaN/GaN HEMTs on SiC Substrate in RF Operating Conditions », *IEEE Trans. Electron Devices*, vol. 62, nº 12, p. 3992-3998, déc. 2015, doi: 10.1109/TED.2015.2493204.

[20] M. Kuball *et al.*, « Measurement of temperature in active high-power AlGaN/GaN HFETs using Raman spectroscopy », *IEEE Electron Device Lett.*, vol. 23, nº 1, p. 7-9, janv. 2002, doi: 10.1109/55.974795.

[21] R. J. T. Simms, J. W. Pomeroy, M. J. Uren, T. Martin, et M. Kuball, « Channel Temperature Determination in High-Power AlGaN/GaN HFETs Using Electrical Methods and Raman Spectroscopy », *IEEE Trans. Electron Devices*, vol. 55, nº 2, p. 478-482, févr. 2008, doi: 10.1109/TED.2007.913005.

[22] M. Dammann *et al.*, « Reliability of 100 nm AlGaN/GaN HEMTs for mm-wave applications », *Microelectronics Reliability*, vol. 76-77, p. 292-297, sept. 2017, doi: 10.1016/j.microrel.2017.07.008.

[23] H. Jung *et al.*, « Reliability behavior of GaN HEMTs related to Au diffusion at the Schottky interface », *Phys. Status Solidi (c)*, vol. 6, nº S2, juin 2009, doi: 10.1002/pssc.200880819.

[24] M. Dammann *et al.*, « Degradation of 0.25 µm GaN HEMTs under high temperature stress test », *Microelectronics Reliability*, vol. 55, nº 9-10, p. 1667-1671, août 2015, doi: 10.1016/j.microrel.2015.06.042.

[25] Y. Q. Chen *et al.*, « Degradation mechanism of AlGaN/GaN HEMTs during high temperature operation stress », *Semicond. Sci. Technol.*, vol. 33, nº 1, p. 015019, janv. 2018, doi: 10.1088/1361-6641/aa9d71.

[26] P. Blood, « Capacitance-voltage profiling and the characterisation of III-V semiconductors using electrolyte barriers », *Semicond. Sci. Technol.*, vol. 1, nº 1, p. 7-27, juill. 1986, doi: 10.1088/0268-1242/1/1/002.

[27] M. J. Uren *et al.*, « Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths », *IEEE Electron Device Lett.*, vol. 35, nº 3, p. 327-329, mars 2014, doi: 10.1109/LED.2013.2297626.

[28] M. J. Uren et M. Kuball, « Impact of carbon in the buffer on power switching GaN-on-Si and RF GaN-on-SiC HEMTs », *Jpn. J. Appl. Phys.*, vol. 60, nº SB, p. SB0802, mai 2021, doi: 10.35848/1347-4065/abdb82.

[29] M. J. Uren *et al.*, « "Leaky Dielectric" Model for the Suppression of Dynamic R_{ON} in Carbon-Doped AlGaN/GaN HEMTs », *IEEE Trans. Electron Devices*, vol. 64, nº 7, p. 2826-2834, juill. 2017, doi: 10.1109/TED.2017.2706090.

[30] J. Lu *et al.*, « Transmorphic epitaxial growth of AlN nucleation layers on SiC substrates for high-breakdown thin GaN transistors », *Applied Physics Letters*, vol. 115, nº 22, p. 221601, nov. 2019, doi: 10.1063/1.5123374.

[31] B. Godejohann *et al.*, « AlN/GaN HEMTs grown by MBE and MOCVD: Impact of Al distribution », *Physica Status Solidi (b)*, vol. 254, nº 8, p. 1600715, août 2017, doi: 10.1002/pssb.201600715.

[32] A. Papamichail *et al.*, « Impact of Al profile in high-Al content AlGaN/GaN HEMTs on the 2DEG properties », *Applied Physics Letters*, vol. 125, nº 12, p. 123505, sept. 2024, doi: 10.1063/5.0218911.

[33] G. Zhan *et al.*, « Transconductance Overshoot, a New Trap-Related Effect in AlGaN/GaN HEMTs », *IEEE Trans. Electron Devices*, vol. 70, nº 6, p. 3005-3010, juin 2023, doi: 10.1109/TED.2023.3270134.

[34] J. R. Jenny *et al.*, « High-purity semi-insulating 4H-SiC grown by the seeded-sublimation method », *Journal of Elec Materi*, vol. 31, nº 5, p. 366-369, mai 2002, doi: 10.1007/s11664-002-0084-9.

[35] M. E. Zvanut, V. V. Konovalov, H. Wang, W. C. Mitchel, W. D. Mitchell, et G. Landis, « Defect levels and types of point defects in high-purity and vanadium-doped semi-insulating 4H–SiC », *Journal of Applied Physics*, vol. 96, nº 10, p. 5484-5489, nov. 2004, doi: 10.1063/1.1797547.

[36] U. Chowdhury *et al.*, « TEM Observation of Crack- and Pit-Shaped Defects in Electrically Degraded GaN HEMTs », *IEEE Electron Device Lett.*, vol. 29, nº 10, p. 1098-1100, oct. 2008, doi: 10.1109/LED.2008.2003073.

[37] L. Li, J. Joh, J. A. Del Alamo, et C. V. Thompson, « Spatial distribution of structural degradation under high-power stress in AlGaN/GaN high electron mobility transistors », *Applied Physics Letters*, vol. 100, nº 17, p. 172109, avr. 2012, doi: 10.1063/1.4707163.

[38] D. Marcon *et al.*, « Reliability of AlGaN/GaN HEMTs: Permanent leakage current increase and output current drop », in *Proceedings of the 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Suzhou, China: IEEE, juill. 2013, p. 249-254. doi: 10.1109/IPFA.2013.6599162.

[39] F. Gao, S. C. Tan, J. A. Del Alamo, C. V. Thompson, et T. Palacios, « Impact of Water-Assisted Electrochemical Reactions on the OFF-State Degradation of AlGaN/GaN HEMTs », *IEEE Trans. Electron Devices*, vol. 61, nº 2, p. 437-444, févr. 2014, doi: 10.1109/TED.2013.2293114.

[40] E. Zanoni *et al.*, « Failure Physics and Reliability of GaN-Based HEMTs for Microwave and Millimeter-Wave Applications: A Review of Consolidated Data and Recent Results », *Physica Status Solidi (a)*, vol. 219, nº 24, p. 2100722, déc. 2022, doi: 10.1002/pssa.202100722.

[41] P. F. Magnier, « Étude de la fiabilité des filières 0.15 µm GaN sur SiC Caractérisation et analyse des effets parasites et des mécanismes de dégradation ».

[42] J. Möreke, M. Ťapajna, M. J. Uren, Y. Pei, U. K. Mishra, et M. Kuball, « Effects of gate shaping and consequent process changes on AlGaN/GaN HEMT reliability », *Physica Status Solidi (a)*, vol. 209, nº 12, p. 2646-2652, déc. 2012, doi: 10.1002/pssa.201228395.

[43] S. D. Burnham *et al.*, « Reliability of T-gate AlGaN/GaN HEMTs », *Phys. Status Solidi C*, vol. 8, nº 7-8, p. 2399-2403, juill. 2011, doi: 10.1002/pssc.201000916.

[44] R. Lossy, H. Blanck, et J. Würfl, « Reliability studies on GaN HEMTs with sputtered Iridium gate module », *Microelectron. Reliab.*, vol. 52, nº 9-10, p. 2144-2148, sept. 2012, doi: 10.1016/j.microrel.2012.06.154.

[45] R. Lossy, H. Blanck, et J. Würfl, « 10.3 Sputtered Iridium Gate Module for GaN HEMT with Stress Engineering and High Reliability », 2014.

[46] D. I. Shahin *et al.*, « Electrical and Thermal Stability of ALD-Deposited TiN Transition Metal Nitride Schottky Gates for AlGaN/GaN HEMTs », *ECS J. Solid State Sci. Technol.*, vol. 5, nº 7, p. Q204-Q207, 2016, doi: 10.1149/2.0211607jss.

[47] D. I. Shahin *et al.*, « Reliability Assessment of Thermally-Stable Gate Materials for AlGaN/GaN HEMTs », 2016.

[48] C. Chen *et al.*, « Effect of the post-gate annealing on the gate reliability of AlGaN/GaN HEMTs », *J. Semicond.*, vol. 42, nº 9, p. 092802, sept. 2021, doi: 10.1088/1674-4926/42/9/092802.

[49] S. Singhal *et al.*, « Reliability of large periphery GaN-on-Si HFETs », *Microelectronics Reliability*, vol. 46, nº 8, p. 1247-1253, août 2006, doi: 10.1016/j.microrel.2006.02.009.

General conclusion

In an increasingly connected world, the interest in millimeter-wave frequencies continues to expand due to their reduced wavelengths and wide frequency bands, enabling more compact components with improved efficiency. However, several challenges remain to be addressed before these technologies can be fully utilized. High-frequency devices must deliver high efficiency and power density while maintaining strong reliability. GaN-based transistors have emerged as a highly promising candidate in this frame. The primary objective of this PhD thesis was to investigate advanced GaN HEMT architectures for next-generation mmWave applications, through device fabrication and TCAD simulation.

Chapter 1 presents the unique properties of GaN that are compared to those from other commonly used semiconductors. GaN exceptional properties such as its high bandgap, high electron velocity and critical electric field make it an ideal candidate for future RF applications. Then, GaN-based HEMTs have been described with a focus on specific device design targeting mmW applications. Each layer of the epi-stack must be carefully optimized, as it has a significant impact on device performance. Device fabrication and process optimization also play a critical role, as it will determine the overall efficiency and robustness, particularly under high electric field and high junction temperature. In recent years, several advancements have been achieved, and many academics and industrials have reported outstanding power performance up to the W band. The main challenges now facing the community, on top of the combination of output power density and power-added-efficiency are : the improvement of the device linearity and reliability along with reduced trapping effects. There are currently no commercially available high power (> 3 W/mm) GaN foundry processes above 40 GHz with proven long-term reliability. The chapter concludes with a review of the latest GaN technologies aiming for millimeter-wave range.

Chapter 2 is dedicated to the study of graded AlGaN channel HEMT from HRL laboratory using TCAD simulations. This technology is of great interest because of its unique combination of high linearity with high power-added-efficiency. A powerful and complex simulation workflow has been developed in this frame. Three distinct levels are used: device-level simulation (1), compact modeling (2), and circuit-level simulation (3).

The main challenge was to reproduce as close as possible the device's behavior, including large signal and linearity characteristics, and to compare with conventional AlGaN/GaN HEMTs in order to further understand the benefits and physical phenomena involved in this technology. Thanks to its unique and optimized epi-design, graded AlGaN channel HEMTs enable electrons to spread along the graded layer, forming a 3DEG configuration that improves the electron channel velocity and thus allowing for flat transconductance. In fact, this particular electron distribution reduces the peak electric field without additional gate metal capacitances. As a result, the device can operate in a linear regime while maintaining high RF power performance (PAE > 65%). These results also demonstrate that TCAD simulation is becoming a more and more powerful tool supporting the understanding of complex GaN HEMT architectures as seen for Silicon-based technologies.

In Chapter 3, the electrical and structural characterizations of two different structures have been investigated. The fabrication process used in this thesis-work is first described. The chapter continues with a study of AlN/GaN/AlGaN back barrier HEMTs. We demonstrated that the insertion of a thin C-doped AlGaN layer offers an excellent compromise for reducing trapping effects while maintaining excellent electron confinement with short gate lengths. State-of-the-art power performance at 40 GHz was achieved with a PAE above 65% and an associated P_{OUT} of 3.5 W/mm at V_{DS} = 20V. Subsequently, initial short-term reliability measurements were conducted. It was found that this AlGaN back barrier based devices are sensitive to the junction temperature (Tj). Structural characterizations after short-term HTOL tests under high Tj revealed a degradation of the gate module, pointing out the need to optimize the fabrication process. Finally, a study of the impact of carbon in the back barrier was conducted. Completely removing carbon in the AlGaN back barrier proved not to be a viable option, as it severely degraded the device performance and induced a second 2DEG. TCAD simulations demonstrated that high levels of carbon doping is not required, but a sufficiently high concentration (> 1×10^{18} cm^{-3}) is necessary to compensate for the electrons at the back barrier/buffer interface. This chapter concludes with a study of AlGaN/GaN buffer-free HEMTs. Excellent electron confinement and low leakage current were achieved with short gate lengths. Due to the high-quality AlN nucleation layer acting as a back barrier, this technology could be fully competitive with existing thick-buffer designs.

Encouraging power performance at 40 GHz was observed, with a PAE of around 50% and an associated P_{OUT} of 2.6 W/mm at V_{DS} = 20V. Further efforts are still needed to reduce trapping and better understand this technology. Initial short-term reliability measurements also showed promising results, reflecting improved thermal dissipation. However, HRTEM revealed severe gate metal degradation, and optimizing the gate module remains one of the major challenges for improving device reliability.

Outlooks and future work

As presented in Chapter 2, a simulation methodology covering both device and circuit levels has been developed. Within this framework, several improvements and new topics can be explored. It would be beneficial to modify and implement new parameters in ATLAS or in the Angelov model to better assess the scalability or data fitting of the entire workflow. For instance, trapping or thermal effects could be integrated. As part of the development of a two-tone linearity bench at the IEMN laboratory, the workflow could initially be applied to our own structures, such as the AlN/GaN/AlGaN back barrier HEMT to evaluate linearity performance. TCAD thermal or aging stress simulations can also be carried out on the AlGaN back barrier and on buffer-free structures to determine their respective drawbacks or advantages. Finally, the impact of carbon in the AlGaN back barrier needs further study, and TCAD could provide additional insights (**Figure 1**).

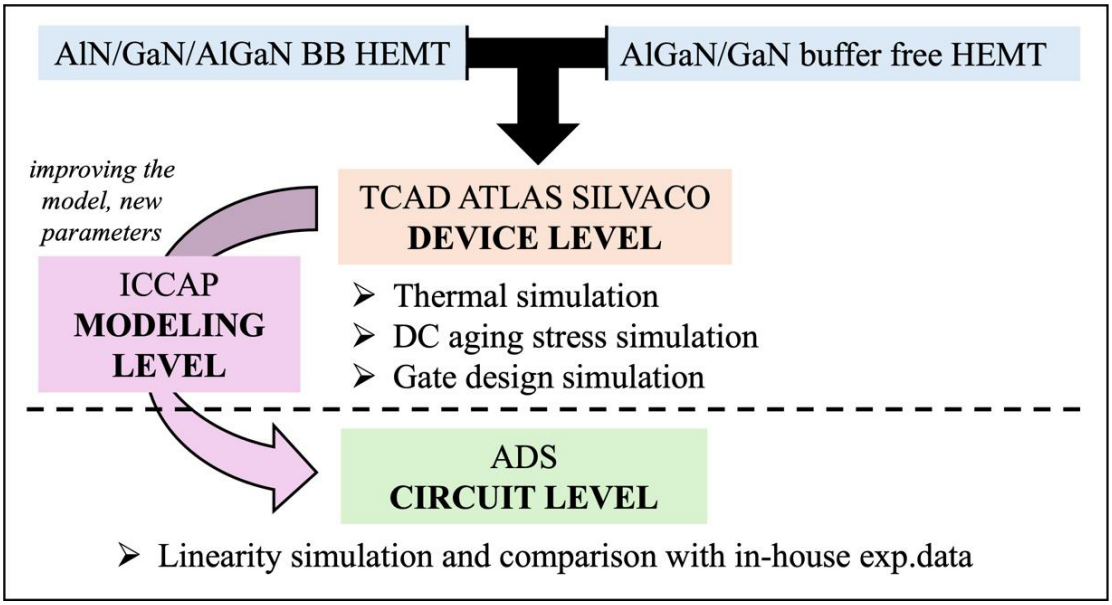


Figure 1. Roadmap for device simulations.

As discussed in Chapter 3, the AlN/GaN/AlGaN back barrier structure offers promising performance for future mmW applications. However, it is essential to measure the junction temperature under the given conditions to validate the results. This should be performed in a near future with the support of partners. Additionally, careful optimization of the gate module (shape, foot height, and/or metal changes) must be implemented in order to limit or prevent the observed degradation after HTOL stress and thus enables operation under higher junction temperature. Regarding the carbon doping in the AlGaN back barrier, its impact on trapping phenomena remains largely unknown and has been rarely studied by the scientific community. Transient drain current measurements (DCT), as well as temperature measurements, are currently being conducted in our research group to better understand its impact. To support this study, two new structures have been designed with SOITEC and are undergoing development. The first one is an AlN/GaN/C-doped AlGaN back barrier structure with 250 nm thick GaN channel. The second one features a hybrid C-doped/undoped AlGaN back barrier with thinner GaN channel (**Figure 2**). These new heterostructures should enable us to further explain the impact of carbon within the AlGaN layer with respect to trapping and electron confinement with short gate lengths.

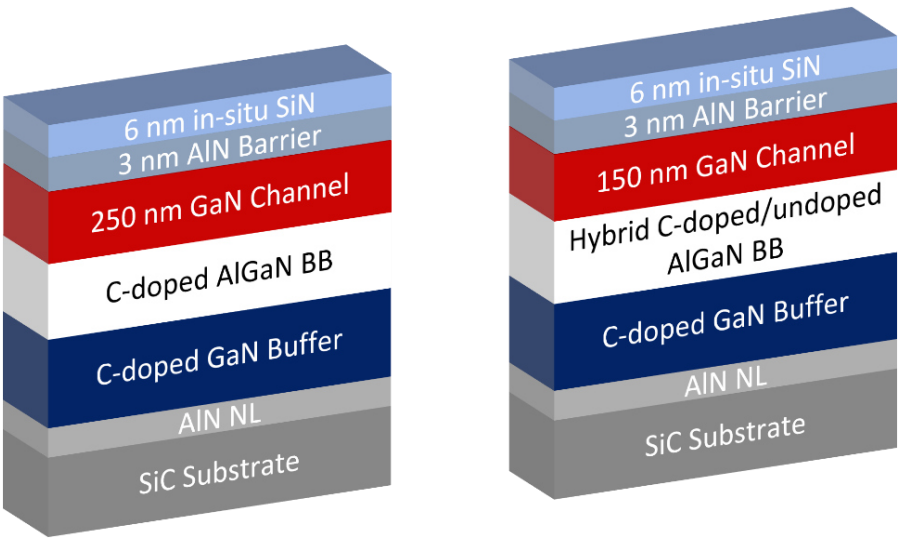


Figure 2. Planned variations of the AlN/GaN/AlGaN back barrier structure.

In chapter 3, we also presented AlGaN/GaN buffer-free HEMTs with encouraging results despite the non-optimized contact resistances. The next step is to reduce the contact resistances below 0.4 Ω.mm and reevaluate the power performances at 40 GHz. Additionally, promising results in terms of reliability have also emerged.

However, the junction temperature under the test conditions must be also measured. Through HRTEM analysis, we again observed severe degradation of the gate module after short-term HTOL test. Efforts are required to optimized the gate module and prevent such damages. With the aim of better understanding this epi-design approach, two new structures have been defined, and will be grown by the partner SweGaN (**Figure 3**). The first one is identical to the 150 nm GaN channel except for the GaN/SiN hybrid cap that has been replaced by a SiN cap. This structure will allow to study the impact of the in-situ cap, particularly on surface trapping. The second one is also identical but with the insertion of an AlGaN back barrier layer sandwiched between the GaN channel and the AlN nucleation layer. This structure could be highly attractive, with potential improvements in term of trapping while maintaining optimum electron confinement with short gate lenghts.

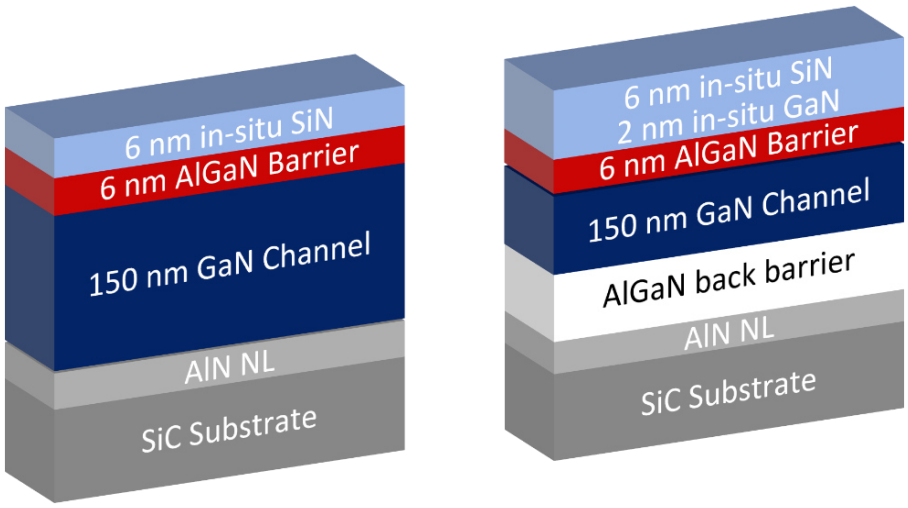


Figure 3. Planned variations of the AlGaN/GaN buffer-free structure.

Publications and contributions

• Journals:

- **François Grandpierron**, Elodie Carneiro, Lyes Ben-Hammou, Jeong-sun Moon and Farid Medjdoub, *Understanding and quantifying the benefit of graded AlGaN channel HEMTs,* Micromachines,2024,15(11), 1356.

- Ajay Shanbhag, **Francois Grandpierron**, Kathia Harrouche, Farid Medjdoub, *Physical Insights of thin AlGaN Back Barrier for millimeter-wave high voltage AlN/GaN on SiC HEMTs,* Applied Physics Letters, 2023, 123 (4), pp.142102.

- Kathia Harrouche, Srisaran Venkatachalam, Lyes Ben-Hammou, **François Grandpierron**, Etienne Okada and Farid Medjdoub, *Low Trapping Effects and High Electron Confinement in Short AlN/GaN-On-SiC HEMTs by Means of a Thin AlGaN Back Barrier,* Micromachines, 2023,14,291.

- Kathia Harrouche, Srisaran Venkatachalam, **Francois Grandpierron**, Etienne Okada, and Farid Medjdoub, *Impact of undoped channel thickness and carbon concentration on AlN/GaN on SiC HEMT performances,* Applied Physics Express 15, 116504, 2022

• International conferences:

- International Workshop on Nitride Semiconductors (IWN) 2024 (November 3-8) at Honolulu (USA), *High temperature operating life test assessment of buffer-free GaN-on-SiC HEMTs for millimeter wave applications,* **François Grandpierron**, Elodie Carneiro Lyes Ben-Hammou, Ding Yuan Chen, Jr-Tai Chen and Farid Medjdoub

- The next Millimeter-Wave breakthrough coming up with advanced AlN/GaN transistors. GaN Marathon, Jun 2024, Verone, Italy. *The next Millimeter-Wave breakthrough coming up with advanced AlN/GaN transistors*, L. Ben-Hammou**, Francois Grandpierron**, Kathia Harrouche, F Medjdoub.

- 7th Workshop on Compound Semiconductor Devices and Integrated Circuits, May 2024, Heraklion, Greece, *Investigation of the origin of deep levels in Carbon-doped AlN/GaN/AlGaN HEMTs,* L. Ben Hammou, **Francois Grandpierron**, Elodie Carneiro, Katir Ziouche, Etienne Okada

- Workshop Wocsdice Exmatec 2024 (May 19-23) at Heraklion (Greece): *Impact of carbon-doped AlGaN back barrier in AlN/GaN/AlGaN HEMTs,* **François Grandpierron**, Lyes Ben-Hammou, Elodie Carneiro, Marianne Germain, Jan Strate and Farid Medjdoub

- 14th International Conference on Nitride Semiconductors (ICNS-14), Nov 2023, Nagoya, Japan, *Epi-design optimization in AlN/GaN HEMTs for superior drain bias operation and reduced trapping effects*, Kathia Harrouche, Lyes Ben-Hammou, **François Grandpierron**, Ajay Shanbhag, Etienne Okada

- 46th Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE 2023), May 2023, Palerme (Italie), *Pushing Q-band power performances by means of buffer engineering in AlN-GaN HEMTs*, Kathia Harrouche, **François Grandpierron**, Lyes Ben-Hammou, Etienne Okada, F Medjdoub

- International Workshop on Nitride Semiconductors, IWN 2022, Oct 2022, Berlin, Germany, *Combining low trapping effects and high electron confinement in sub-100 nm AlN/GaN HEMTs under high electric field*, S Venkatachalam, Kathia Harrouche, **François Grandpierron**, Stefan Degroote, Marianne Germain

- 8th International Conference on Antennas and Electromagnetic Systems, AES 2022, May 2022, Marrakesh, Morocco, *Status and progress of millimeter-wave GaN transistors for next generation high-power radar systems*, Kathia Harrouche, Sri Saran Vankatachalam, Elodie Carneiro, **François Grandpierron**, F Medjdoub

- **Other contributions:**

As part of the development of SmartGaN, an emerging substrate produced by SOITEC for next-generation high-voltage power applications, I applied my expertise in TCAD simulation to evaluate a novel concept leveraging SmartCut technology (commonly used for SOI substrates). This concept involves transferring a high-quality, thin GaN layer onto high thermal conductivity PolySiC or Silicon using a bonding layer. The target markets for this innovation include 600V and 1200V applications.

Within this framework, our research group is responsible for exploring the potential of these engineered substrates by theoretically assessing their impact on various lateral and vertical power device designs. The initial set of simulations led to the generation of two patents by SOITEC, for which I am a co-inventor.

- **Patent 1 :** *Substrat intermédiaire pour la fabrication d'un substrat pour transistor a haute mobilité d'électrons,* Thierry Boudet (SOITEC), **François Grandpierron** (CNRS) and Farid Medjdoub (CNRS),

- **Patent 2 :** *Design of vertical SmartGaN substrate for power electronics (in progress),* Thierry Boudet (SOITEC), **François Grandpierron** (CNRS) and Farid Medjdoub (CNRS).