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Analyse du comportement de commutation des transistors GaN-HEMTs dans les convertisseurs de puissance en tenant compte de la variation de Vth et de la configuration du driver de grille

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Switching behaviour analysis of GaN-HEMTs in power converters considering Vth shift and gate driver configuration

by

Xuyang Lu

A thesis submitted in partial fulfilment of the University's requirements for the Degree of Doctor of Philosophy

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Keywords: GaN power transistors, threshold voltage measurement, semiconductor transistors modelling, switching behaviour, circuit parasitic parameters.

Mots clés : GaN transistor de puissance, mesure de tension de seuil, modélisation des transistors semi-conducteurs, comportement de commutation, paramètres parasites du circuit.

Switching behaviour analysis of GaN-HEMTs in power converters considering Vth shift and gate driver configuration

Abstract

This thesis investigates the influence of threshold voltage (V_{th}) shift and gate driver's output capacitance on the switching behaviour of gallium nitride high electron mobility transistors (GaN-HEMTs). Understanding these factors is crucial for accurate device modelling and switching performance estimation before employing the GaN-HEMTs in power converters. The first chapter of the thesis introduces the origin and characterisation methods of the V_{th} shift phenomenon in GaN-HEMTs. In the second chapter, an in-situ V_{th} measurement method is proposed to characterise the V_{th} shift phenomenon under soft-switching conditions in both single- and multi-pulse modes. The third chapter studies the impact of V_{th} shift on the switching behaviour of the transistors through theoretical analysis, demonstrated by simulation and experimental validation. In the final chapter, the influence of the gate driver's output capacitance on the switching behaviour of GaN-HEMTs is investigated in two common gate configurations: single and split outputs. Equivalent circuits for both configurations are presented to illustrate their effect on transistors driving performance. The results clearly show that both the positive V_{th} shift and the output capacitance in the split output gate driver can slow down the turn-on commutation speed of GaN-HEMTs.

Keywords: GaN power transistors, threshold voltage measurement, semiconductor transistors modelling, switching behaviour, circuit parasitic parameters.

Analyse du comportement de commutation des transistors GaN-HEMTs dans les convertisseurs de puissance en tenant compte de la variation de Vth et de la configuration du driver de grille

Résumé

Cette thèse s'intéresse à l'influence de la variation de la tension de seuil (V_{th}) et de la capacité de sortie du driver de grille sur le comportement en commutation des transistors à haute mobilité d'électrons en nitrure de gallium (GaN-HEMTs). Comprendre ces facteurs est crucial pour une modélisation précise des dispositifs et pour une bonne estimation des performances en commutation avant d'employer les GaN-HEMTs dans les convertisseurs de puissance. La première partie de la thèse présente l'origine et les méthodes de caractérisation du phénomène de variation de V_{th} dans les GaN-HEMTs. Dans le deuxième chapitre, une méthode de mesure in-situ de V_{th} est proposée pour caractériser le phénomène de variation de V_{th} dans des conditions de commutation douce, en modes mono-impulsion et multi-impulsion. Le troisième chapitre étudie l'impact de la variation de V_{th} sur le comportement en commutation à travers une analyse théorique, démontrée par simulation et par validation expérimentale. Dans la dernière partie, l'influence de la capacité de sortie du driver de grille sur le comportement en commutation des GaN-HEMTs est examinée dans deux configurations de grille courantes : sortie unique et sortie séparée. Des circuits équivalents pour les deux configurations sont présentés pour illustrer leur effet sur les performances de commande rapprochée des transistors. Les résultats montrent qu'aussi bien l'augmentation de V_{th} que la capacité de sortie du driver de grille à sorties séparées peuvent ralentir la vitesse de commutation à la mise en conduction des GaN-HEMTs.

Mots clés : GaN transistor de puissance, mesure de tension de seuil, modélisation des transistors semi-conducteurs, comportement de commutation, paramètres parasites du circuit.

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Acronyms

Symbols

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Introduction

Electrification is essential in enabling the integration of renewable energy sources and reducing the carbon emission. This transition necessitates the widespread deployment of power converters, which can support the electrification of transportation and industrial sectors. The emergence of gallium nitride (GaN) semiconductor devices has elevated the operation frequency of power converters to unprecedented levels due to the fast commutation characteristics of new transistors. Although GaN transistors can significantly enhance the efficiency and power density of the power converters, they also introduce additional challenges, including device reliability concerns, high sensitivity of parasitic parameters, and electromagnetic compatibility (EMC) issues. Addressing these challenges requires a deep understanding of the trapping effect in GaN transistors, such as the related dynamic on-state resistance (R_{on}) and threshold voltage (V_{th}) shift phenomenon, and their influence on the switching performance of GaN devices. Additionally, the influence of circuit parasitic parameters on the application of GaN transistors should be carefully considered due to the high commutation speed of GaN transistors.

This thesis explores three research challenges derived from the GaN high electron mobility transistors (GaN-HEMTs) technology. The first one relates to the characterisation of the voltage bias induced V_{th} shift phenomenon based on a customised circuit. The second one investigates the influence of V_{th} shift on the switching behaviour of transistors, following the conclusion of the first challenge. Finally, the influence of gate driver configuration on the switching commutation of GaN-HEMTs is studied based on two regular gate loop topologies. This thesis comprises by four chapters.

The first chapter is dedicated to introducing the origins of the trapping effect and the high sensitivity of GaN-HEMTs to parasitic parameters, stemming from the material properties and device structure. It also reviews the state-of-the-art research on the dynamic R_{on} and V_{th} shift phenomena found in commercial GaN-HEMTs, highlighting the necessity for further characterisation of the voltage bias induced V_{th} shift phenomenon and its impact on switching behaviour. Subsequently, the significantly reduced inter-electrode capacitance of GaN-HEMTs is illustrated, emphasising the importance of considering the gate driver's output capacitance when driving the GaN-HEMTs.

The second chapter describes an half-bridge based in-situ V_{th} shift measurement method, enabling the characterisation of the off-state drain-to-source voltage (V_{ds}) induced V_{th} shift for both Schottky-type and Ohmic-type p-GaN gate HEMTs. The V_{ds}

bias induced V_{th} shift phenomenon under various bias amplitudes and durations is characterised in the single pulse mode test. Subsequently, the recovery behaviour of the shifted V_{th} after an extended high-voltage single-pulse bias is evaluated using the same setup, showing an hours level recovery time constant for the Schottky-type GaN-HEMTs, and this time constant is validated by the semiconductor curve tracer based test. Additionally, the influence of recovery time, duty cycle and switching frequency on the steady-state V_{th} is evaluated for these two types of device in the continuous mode test. The significant positive V_{th} shift and the prolonged recovery time suggests the potential impact of V_{th} shift phenomenon on subsequent switching commutations after the voltage bias.

In the third chapter, the influence of V_{th} shift on the switching behaviour of GaN-HEMTs is demonstrated. At first, the relationship between the transfer characteristics and switching transition is analysed to theoretically assess the impact of V_{th} shift on the switching commutation. Subsequently, an H-bridge based double-pulse test (DPT) is employed to capture the $I-V$ characteristics of GaN-HEMTs, incorporating the V_{ds} bias induced V_{th} shift phenomenon. Subsequently, GaN-HEMT models incorporating these $I-V$ characteristics were developed and imported into simulations to investigate how the V_{th} shift influences the switching behaviour of GaN-HEMTs. Finally, a DPT-based experiment is performed to further validate the theoretical analysis and simulation.

In the last chapter, the focus shifts to the output capacitance (C_{oss}) of metal oxide semiconductor field effect transistors (MOSFETs) inside the gate driver. Its impact on the switching behaviour of GaN-HEMTs is investigated based on two commonly used gate driver output topologies: single and split configurations. The equivalent circuits of these two gate configurations are proposed to analyse the influence of gate driver C_{oss} on the charging and discharging process of GaN-HEMTs, indicating that this C_{oss} could slow down the charging process of GaN-HEMTs in the split output gate configuration, this phenomenon is defined as the split output gate configuration (SPOGC) effect in this study. Subsequently, hard-switching simulation setups, with these two gate configurations, are constructed to evaluate the influence of SPOGC effect on the switching behaviour. Finally, the corresponding DPTs are conducted to validate this influence on the switching behaviour of GaN-HEMTs.

Chapter 1

GaN transistors state-of-the art review

Outline of the current chapter

1.1 Research context

It has been more than 70 years since the invention of the first silicon (Si)-based transistor. During this time period, researchers and engineers have diligently worked to enhance Si-based transistors, pushing the devices' performance to the limits of the Si material [1]. The limitation of conductivity and breakdown voltage of Si-based transistors have posed an obstacle to further enhancing the efficiency of the electrical energy conversion. In the past ten years, wide band-gap (WBG) semiconductors, silicon carbide (SiC) and gallium nitride (GaN), have become key candidates to deliver higher efficiency for energy conversion and contribute to meeting the net-zero goals for carbon emissions.

With the notable development of digital economy, the massive amounts of data create a surge energy demand, posing a new challenge for power supplies in data centres. Moreover, the rapid development of artificial intelligence (AI) could push the energy consumption to the next level. The utilisation of WBG semiconductor transistors comes in anticipation to address this challenge. For example, the replacement of Si-based

power supplies with GaN-based power supplies in the data centers worldwide from 2015 to 2021 could save 21^3 TWh of energy and reduce 10^6 Mt of CO_2 [2].

Furthermore, the requirement of sustainability imposes a new set of rules for reducing the carbon footprint of power converters due to environmental considerations. It demands considering the environmental impact throughout the entire lifecycle of power converters, including reduced carbon emissions during fabrication, longer estimated lifetimes, and recyclability [3]. The utilisation of the GaN power transistors could enhance sustainability from various aspects, as illustrated the next subsection.

1.1.1 Energy conversion efficiency

Improving the efficiency of power converters is a significant challenge, as it contributes to reducing losses during the energy conversion. The main losses of power converters come from the transistors, which are primarily categorised into conduction losses and switching losses [4]. The simplified operation conditions of an ideal switch and a transistor (hard-switching) are depicted in Fig. 1.1. For the ideal switch, the current and voltage commutations occur instantaneously, resulting in zero switching losses. During the conduction state, there is no voltage drop across the switch due to the zero on-state resistance R_{on}, leading to no conduction losses. However, for real transistors, it takes time for the commutation of voltage and current, resulting in switching losses. The non-zero R_{on} produces conduction losses during the on-state transistor functioning. Therefore, power transistors with fast commutation speed and low R_{on} are expected to be implemented in the high-efficiency power converters. Compared to the conventional Si devices, GaN power transistors have garnered increasing attention due to their characteristics, which more closely resemble the ideal switches. An example illustrative supporting the GaN transistor technology is the 900 W three-phase inverter, where under full load its efficiency have been improved from 98.2 % to 99.3 % by replacing the Si insulated gate bipolar transistors (IGBTs) with gallium nitride high electron mobility transistors (GaN-HEMTs) [5]. Moreover, a GaN-based 2.5 kW totem-pole power factor correction (PFC) with 99 % peak efficiency is reported in [6].

1.1.2 Power density and sustainability

High power density is another key objective in the power converter design, and it is defined as the amount of power per unit volume. The power density of power converters is mainly determined by the passive devices, such as transformers, capacitors and heat sinks. The volume of inductors or capacitors in power converter applications is mainly determined by the operating frequency, and it could be significantly reduced by increasing the frequency. However, the switching losses of power transistors become more prominent at higher operation frequencies. Therefore, it is highly recommended to use GaN transistors in high-frequency due to their fast switching speed, which results in lower switching losses compared to other power transistors. For example, in a GaN-based 1 MHz inductor-inductor-capacitor (LLC) resonant DC-DC converter, the size of transformer can be reduced 6 times compared to the Si transistor based 1 kHz design,

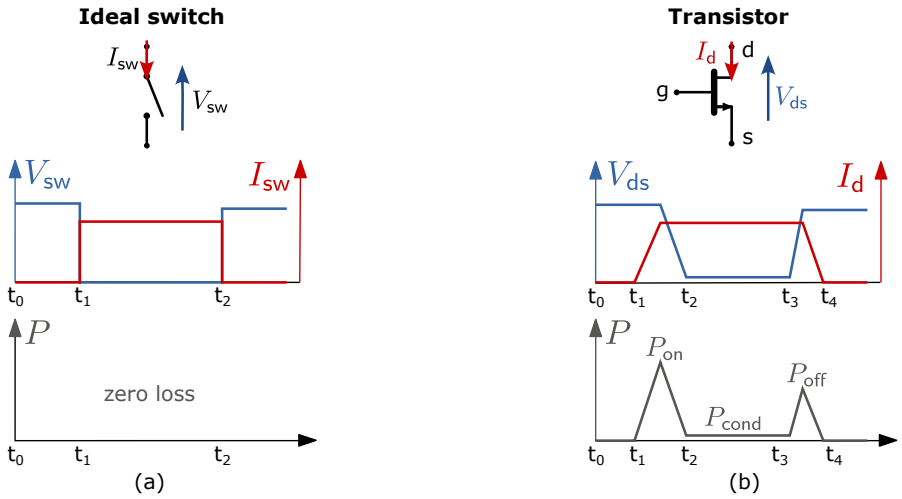


Figure 1.1: Schematic of operation conditions and switching waveforms of (a) an ideal switch and (b) a transistor.

and the power density can reach up to 8.5 W cm^{-3} [7]. Moreover, the low R_{on} contributes to decreasing the overall conduction losses, thereby reducing the size of the heat sink.

High power density contributes to improving space efficiency and reducing costs. More importantly, sustainability and the low carbon footprint of power converters can significantly benefit from it by requiring fewer materials and energy during fabrication. Therefore, GaN power transistors show significant advantages for achieving high efficiency and high power density converters, which in turn contribute to the sustainability of power conversion systems [8].

However, GaN-HEMTs exhibit unique characteristics, such as the dynamic R_{on} and threshold voltage V_{th}[1] shift phenomena, combined with a high sensitivity to parasitic parameters. These characteristics hinder further increases in the efficiency and power density of GaN-based power converters. Moreover, most driving technologies and evaluation standards for GaN-HEMTs are inherited from Si-based technology. To fully release the superior performance of GaN-HEMTs in power converters, it is necessary to understand and characterise these special features and evaluate their influence on device applications.

1.2 GaN material and power transistors

The typical characteristics of GaN power transistors will be reviewed in this section, starting from their material properties, followed by the structure and operation mechanisms of GaN-HEMTs, and concluding with the overview of the commercialised GaN-HEMTs and vertical power devices under development.

[1] Refers to the minimum gate-to-source voltage that can turn the transistor to on-state.

1.2.1 Material properties comparison of Si, SiC and GaN

The performance of power transistors initially originate from the material properties. The material parameters of Si, SiC and GaN are compared in Table 1.1. The GaN material has a wide band gap (E_g), which means more energy is required to excite the valence electrons to the conduction band compared to the other two counterparts. Therefore, GaN transistors can work at high operating temperature. A good example supporting the GaN stability at high temperatures is reported in [9], where the basic $I-V$ characteristics of an enhancement-mode GaN-HEMT is characterised under 500 °C in NASA Glenn Extreme Environment Rig to simulate the Venus environment, the device only showing a minor degradation after 10 days of continuous operation. Additionally, GaN has a very high critical electric field (E_{crit}), meaning that shorter drift region can be achieved for the same breakdown voltage. The relative high E_{crit} combining with the lateral structure of GaN-HEMT reduces the size of the device. The E_{crit} possesses a power-law dependence on the band gap, expressed as $E_{crit} \propto E_g^{2.3}$ [10]. Therefore, the GaN material fits the technological profile for fabricating high-temperature and high-voltage power transistors.

Material parameters	Unit	Si	4H-SiC *	GaN
Band gap (E_g)	eV	1.12	3.23	3.4
Critical electric field (E_{crit})	MV/cm	0.3	2.5	3.3
Relative dielectric permittivity (ϵ_r)		11.7	10	8.9
Electron mobility (μ)	$cm^2/(V{\cdot}s)$	1440	950	2000 (2DEG) **
Electron saturation velocity (v_s)	$10^7 cm/s$	1	2	2.4
Thermal conductivity (κ_{th})	W/(m·K)	1.3	3.7	2.5

* 4H-SiC is one of the major polytypes of SiC crystalline structure.
** The electron mobility of 1400 $cm^2/(V{\cdot}s)$ is reported for bulk GaN materials in [11]. The 2DEG will be further explained in section 1.2.2.2.

Table 1.1: Comparison of the material properties of Si, SiC, and GaN [11], [12].

The GaN material exhibits the lowest relative dielectric permittivity (ϵ_r), as shown in Table 1.1, which contributes to achieving smaller inter-electrode capacitances for power transistors. The small inter-electrode capacitance is one of the main reasons why GaN power transistors can achieve ultra-fast switching speeds, effectively reducing switching losses. To be noted that the electron mobility (μ) increases the conductivity of semiconductors, and the μ of GaN materials is higher when compared to SiC and it contributes as well to reducing the conduction losses of GaN transistors. Since a single parameter is not relevant for a thorough comparison on material properties, several figure of merit (FOM) are proposed to further asses their performance as discussed below.

On the one hand, the high speed performance of high frequency transistors can be

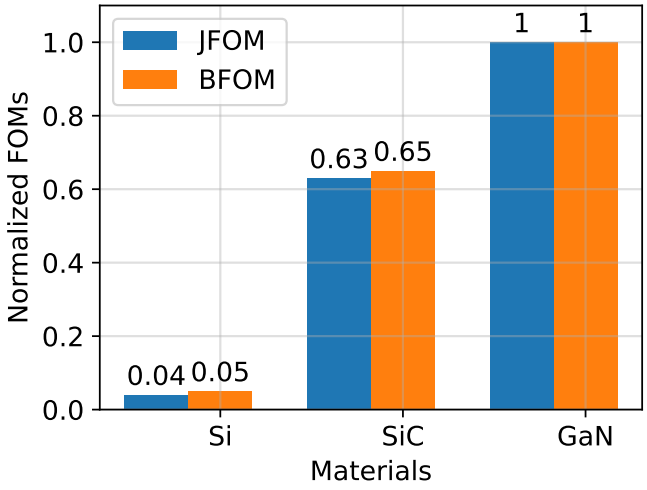


Figure 1.2: Normalised JFOM and BFOM of Si and SiC to GaN (materials' data is from Table 1.1).

described by the Johnson figure of merit (JFOM) that is defined as [11]:

$$JFOM = \frac{v_s \cdot E_{crit}}{2\pi} = f_{t,max} \cdot V_{ds,max} \tag{1.1}$$

where $f_{t,max}$ and $V_{ds,max}$ represent the maximum transient frequency and drain-to-source voltage respectively.

On the other hand, the Baliga figure of merit (BFOM) is used to evaluate the conduction losses for power semiconductors from the material perspective [13]. It is based on the assumption that the power losses solely originate from the R_{on} of power transistors, expressed as:

$$BFOM = \mu \cdot \epsilon_r \cdot E_{crit}^3 \tag{1.2}$$

In a p-n junction, the R_{on} of the n-type semiconductor region is inversely proportional to the BFOM [10], therefore, high BFOM is helps to reduce the conduction losses.

The normalised JFOM and BFOM of materials from Table 1.1 are compared in Fig. 1.2, highlighting the advantages of using GaN transistors for high frequency, high voltage, and low losses over Si and SiC transistors.

1.2.2 Basic structure and operating principle of power GaN-HEMTs

Beyond the material properties, however, the performance of GaN transistors is also highly dependent on the device structures. The HEMT structure is regarded as the most developed and established technology for GaN power transistors. This subsection will introduce the transistor with this structure from basic physics operating principle to the latest commercialised devices.

Materials	Band gap (eV)	Lattice constant a (Å)	Lattice constant c (Å)
AlN	6.1	3.11	4.98
GaN	3.4	3.19	5.19

Table 1.2: Band gap and lattice constant of AlN and GaN materials [15].

1.2.2.1 Polarisation effect

The polarisation effect of GaN includes spontaneous polarisation (P_{sp}) and piezoelectric polarisation (P_{pe}). GaN possesses a Wurtzite crystal structure, similar to the majority of group III-Nitride semiconductors. This structure is non-centrosymmetric, which means it lacks a center of symmetry, resulting in a spontaneous polarisation effect intrinsically. Furthermore, if the lattice experiences strain, the deformation will induce a displacement of atoms within the lattice, resulting in the generation of an electric field, this is called piezoelectric polarisation property [14]. The polarisation effect is fundamental to the conducting channel of GaN-HEMTs, as discussed below.

1.2.2.2 AlGaN/GaN heterojunction and 2DEG channel

The heterojunction is a semiconductor junction composed of two different semiconductor materials. These two materials possess relative big band gap discontinuity to form the potential barrier, necessary for device operation. Meanwhile, the lattice mismatch of these two materials must be small to reduce the interface defect and distortion. The band gap and lattice constant of aluminium nitride (AlN) and GaN are shown in Table 1.2. The $Al_xGa_{1-x}N$ is the resulting alloy of AlN and GaN. It inherits the polarisation effect, while its band gap and lattice constant fall in between those of AlN and GaN by changing the mole fraction x. The AlGaN is a suitable material to form the heterojunction with GaN due to the big band gap discontinuity and small lattice mismatch.

When AlGaN is grown on the top of GaN (Ga-face[2]), the AlGaN is in tensile strain due to the relative smaller lattice constant compared to GaN. In this special case, the spontaneous and piezoelectric polarisation of AlGaN are in the same direction, leading to the generation of positive polarisation charge ($+\sigma$) in the heterojunction interface, as shown in Fig. 1.3(a). The $+\sigma$ is attracting electrons to form the 2-dimentional electron gas (2DEG) in GaN side [16]. Note that both AlGaN and GaN are unintentionally doped (UID), and these electrons are mainly from the donor energy states on the surface of AlGaN [17]. If the AlGaN layer is sufficient thick, the Fermi level (E_f) can reach the donor state (E_d) and the electrons can be stimulated to the conduction band (E_c), leaving the positive surface charge as showed in Fig. 1.3(b). Under the electric field induced by the AlGaN polarisation, these stimulated electrons will move toward GaN layer, forming the 2DEG.

[2]The Ga-face refers to the externally exposed surface of GaN crystals composed of gallium atoms in the GaN lattice.

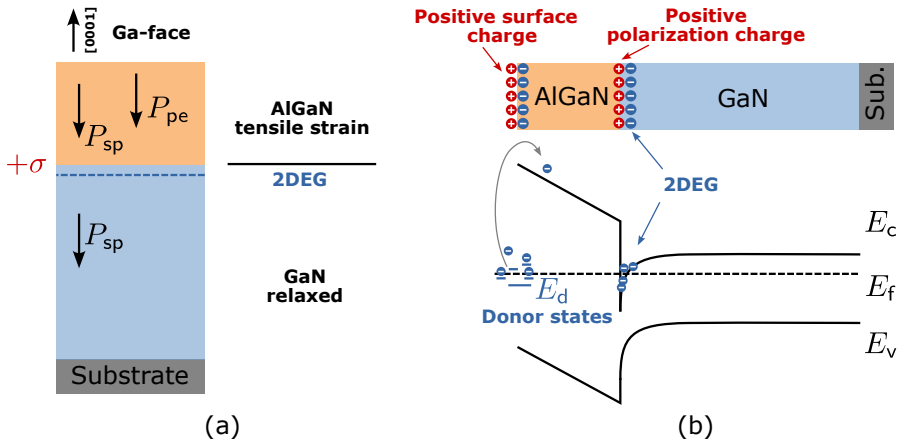


Figure 1.3: Formation of 2DEG in AlGaN/GaN heterojunction (a) polarisation of AlGaN on Ga-face GaN (b) generation of positive surface charge and the electrons in 2DEG from the surface donor states.

In the 2DEG, the electrons have a quantised energy level in one direction (perpendicular to the heterojunction interface), and they can move freely in the other two directions. Moreover, the origin of these electrons in the 2DEG is from AlGaN layer but they are moving in GaN layer, translating that the electrons in 2DEG have less influence from impurity scattering (donor impurity atoms in AlGaN layer) [18]. This is the reason why the electron mobility in 2DEG is extremely high. As mentioned earlier, the electron mobility of GaN in AlGaN/GaN heterojunction can be up to 2000 $cm^2/(V{\cdot}s)$, which is much higher than that in the intrinsic material (1400 $cm^2/(V{\cdot}s)$) [11], [12]. The AlGaN/GaN heterojunction is the fundamental structure of GaN-HEMTs, and the high electron mobility of the 2DEG channel results in the small on-state resistance R_{on}, contributing to the low conduction losses of GaN-HEMTs.

1.2.2.3 Structures and technologies of power GaN-HEMTs

The basic structure of GaN-HEMTs is depicted in Fig.1.4. As discussed above, the 2DEG is naturally formed by the AlGaN/GaN heterojunction without applying external gate voltage (V_g). When a voltage is applied to the drain (D) and source (S) terminals, current will flow through the 2DEG channel. Therefore, GaN-HEMTs naturally are depletion-mode (normally-on) devices. When a negative voltage is applied to the gate (G), the 2DEG will be depleted, allowing the transistor to withstand high voltage in the drain side. The function and necessity of the GaN buffer layer, passivation region, and field plate, which are critical for power devices, will be discussed below.

Si substrate is one of the promising candidates for growing the GaN epitaxial layers due to its reduced costs and maximized yield. However, there are primarily two challenges to be addressed to achieve high-quality GaN layers [10]:

- GaN and Si exhibit approximately a 17 % lattice mismatch [19], and the induced

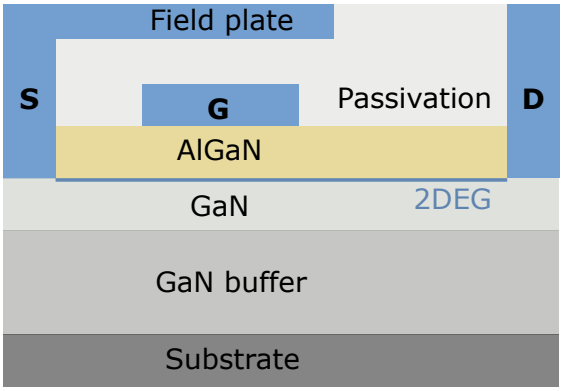


Figure 1.4: Schematic of the power GaN-HEMTs structure (depletion-mode).

strain can propagate through the GaN layer, introducing some defects that can affect the quality and performance of the 2DEG, such as the dynamic R_{on} effect.

- The significant difference of thermal expansion coefficients between GaN ($5.59 \times 10^{-6} K^{-1}$) [20] and Si ($2.6 \times 10^{-6} K^{-1}$) could introduce cracks in the GaN layer during the cooling-stage of epitaxial growth.

To deal with the lattice and thermal expansion mismatches, it is essential to introduce a buffer layer between the Si substrate and GaN layer. An AlN nucleation layer is typically grown on the Si substrate as an initiating layer for GaN epitaxial, as shown in Fig. 1.5. A commonly reported GaN buffer is composed by several layers of $Al_xGa_{1-x}N$ with gradually decreased mole fraction x (AlN, when x = 1; GaN, when x = 0), to mitigate the lattice and thermal mismatch, as displayed in Fig. 1.5(a). Another type of buffer layer consists of several thin AlN/GaN pairs, known as the superlattice, as shown in Fig. 1.5(b). Higher breakdown voltages and fewer defects are reported in this superlattice buffer compared to the step-graded AlGaN buffer. [21], [22].

An additional function of the buffer layer is to increase the isolation between 2DEG and substrate, as the UID GaN is intrinsically n-type semiconductor with a relatively low resistance. It can introduce non-negligible leakage current during off-state that is undesirable for power devices. To increase the resistivity between UID GaN and substrate, the carbon (C) doped GaN and buffer layers are utilised. The C dopant can introduce deep acceptor impurities to compensate the donor states [23]. The schematic of these two popular buffers of power GaN-HEMTs with C-doped GaN layer are shown in Fig. 1.5. Note that the quality of 2DEG channel and the dynamic performance of power GaN-HEMTs are highly dependent on the buffer layer, which is proprietary information for GaN vendors.

The AlGaN/GaN heterojunction ends up with the surface passivation layer in GaN-HEMTs as shown in Fig. 1.4, which is typically made of silicon nitride (SiN) material. The passivation layer is used to reduce the oxidation and defects of the AlGaN layer. It has been mentioned previously that the electrons of 2DEG originate from the surface donor

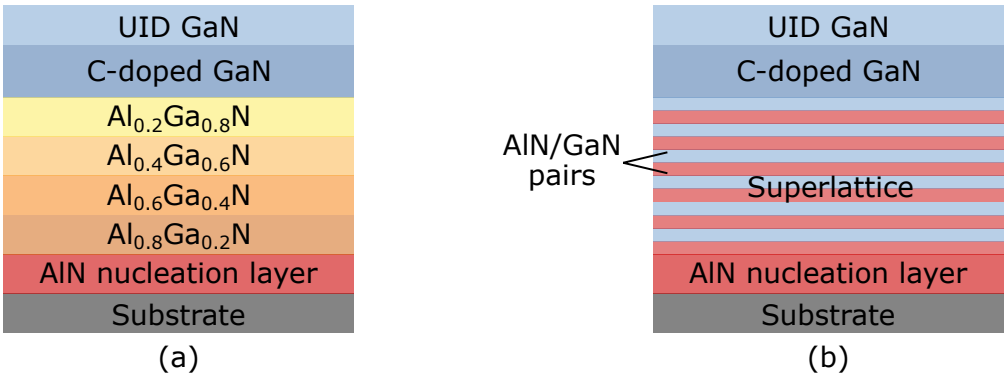


Figure 1.5: Schematic of buffers for power GaN-HEMTs with C-doped GaN layer (a) step-graded buffer (b) superlattice buffer [22].

states of AlGaN layer. However, some surface states also have the ability to capture electrons. The captured electrons on AlGaN surface accumulate together, which behaves like a "virtual gate" in gate to drain access region. The "virtual gate" effect can reduce the conductivity of the 2DEG, causing more conduction losses of the GaN-HEMTs, even depleting the channel [24], [25]. This phenomenon is also known as the current collapse and the passivation layer contributes to mitigate this "virtual gate" effect by reducing the density of surface states on AlGaN layer.

The GaN-HEMTs are lateral devices, meaning the electric field distribution during the off-state is non-uniform, experiencing a high peak at the gate edge close to the drain side. This electric field's peak limits the device breakdown voltage. Therefore, the field plate is fabricated on the source terminal to alleviate the peak of electric field, especially for the gate to source access region as shown in Fig. 1.4. There are several different field plate designs to smooth the electric field peak, such as single field plate, multiple field plates and slant field plate [10], [26]. A practical implemented GaN-HEMT example with a breakdown voltage up to 1200 V is reported by adopting three field plates structure [27]. To be noted that the $C-V$ characteristics of the power GaN-HEMTs are highly related to the field plate design [28].

1.2.2.4 Enhancement-mode GaN-HEMTs technologies

In power electronics applications, enhancement-mode (normally-off) transistors are more popular for the compatibility and safety reasons. There are several techniques that can achieve the enhancement-mode transistors based on the basic structure of GaN-HEMTs:

- **Cascode structure:** this configuration consists of a depletion-mode GaN-HEMT and an enhancement-mode Si-based metal oxide semiconductor field effect transistors (MOSFETs), where the connection is shown in Fig. 1.6. This cascode structure

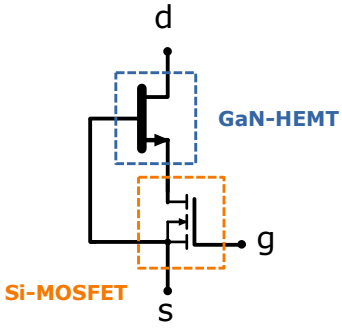


Figure 1.6: Cascode structure for the normally-off GaN transistors composed by a normally-on GaN-HEMT and Si-MOSFET.

is controlled by the Si-MOSFET, so that the device V_{th} is the same as Si-MOSFET. The advantages of the cascode structure are the relative high V_{th} and good compatibility for Si-MOSFET driver. Moreover, the cascode structure supports the increase of rated voltage for power GaN transistors, as the high off-state voltage can be shared by these two transistors (1.2 kV rated voltage can be achieved by the cascode structure developed by Transphorm [29]). However, the increased parasitic inductance resulting from connections and expanded packaging can severely impact the device switching transition performance [30].

- **Fluorine ion treated HEMTs:** the positive V_{th} can be achieved by implanting the fluorine ions into AlGaN layer under the gate metal, as the fluorine ions are negative charged and able to change the surface potential of AlGaN, depleting the 2DEG channel [31].

- **Recessed gate metal insulator semiconductor (MIS) HEMTs:** the AlGaN barrier under the gate can be partly or fully etched to achieve a relative high V_{th} and low gate leakage current. The V_{th} is proportional to the recessed AlGaN thickness [32], while a dielectric layer is mandatory after the etching process to ensure the isolation between gate node and 2DEG channel. Therefore, the V_{th} and electron mobility of the 2DEG are closely related to the selection of dielectric materials and the etching process [10].

- **p-GaN gate HEMTs:** the p-type GaN (or AlGaN) are grown on the AlGaN barrier under the gate stack, which can lift up the energy band diagram of the AlGaN/-GaN heterojunction and deplete the 2DEG channel without external gate voltage, resulting the normally-off behaviour. The schematic of this operation principle is shown in Fig. 1.7 [33]. After applying the positive gate voltage the depleted 2DEG channel can be fully recovered. However, it is challenging to achieve a high quality p-type GaN as the UID GaN is a n-type semiconductor. To address this issue, magnesium (Mg) is widely used, as a p-type dopant for GaN or AlGaN. However, the ionisation energy of Mg is relatively high, therefore, it is difficult to achieve a high concentration of holes with low Mg doping level. Nevertheless, a

high Mg doping level could introduce more defects in the p-GaN layer, affecting the electrical or thermal performance of this transistor. In addition to having sufficient hole concentration in p-GaN, the thin thickness and low Al content in the AlGaN layer are crucial factors in increasing the V_{th} of p-GaN gate HEMTs [34].

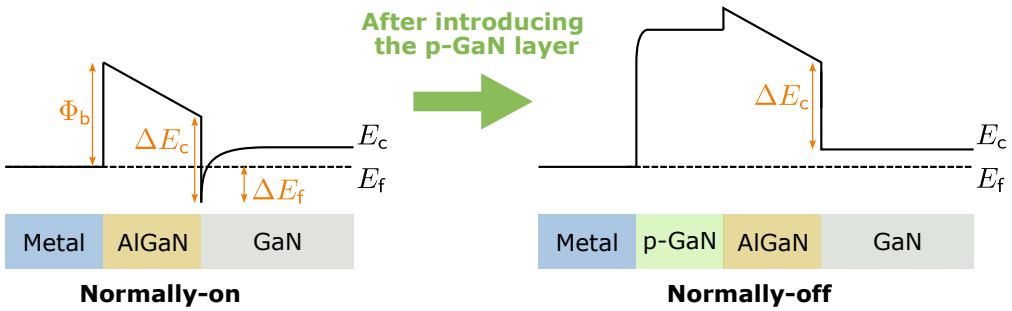


Figure 1.7: The operation principle of p-GaN layer to achieve the normally-off device. Note that the normally-on structure and band diagram is the same as that in Fig. 1.3.

1.2.3 p-GaN gate HEMTs

The p-GaN gate stack is considered as the most mature technology to achieve the normally-off GaN-HEMTs, in consequence, the commercially available discrete (distinct from cascode) enhancement-mode GaN-HEMTs adhere to this technology. Two commercialised p-GaN gate HEMTs, with Schottky- and Ohmic-type gate contacts will be introduced in this subsection.

1.2.3.1 Schottky-type p-GaN gate HEMTs

It is natural for a Schottky-type contact to form between p-GaN and a single-metal electrode, because of the wide energy band gap and big electron affinity of GaN material [10]. Additionally, the p-GaN/AlGaN/GaN heterostructure can form a PIN junction, as the p-GaN and UID GaN are respectively p-type and n-type semiconductors and the AlGaN is depleted as an intrinsic region due to the polarization effect. This PIN junction is in forward bias when the positive gate voltage V_g is applied to turn on the device. The structure and equivalent circuit of the gate stack of the Schottky-type GaN-HEMTs is shown in Fig. 1.8 (a). As mentioned above, this device is easy to drive, similar as driving a Si-MOSFET. However, the gate stack is not strictly insulated as with MOSFETs. The gate leakage current can flow through this PIN junction to the 2DEG channel during on-state, and the leakage current is mainly limited by the reverse biased Schottky junction. However, a relative high V_{gs} voltage in an extended bias duration could degrade the Schottky junction, leading to more than approximately two orders of

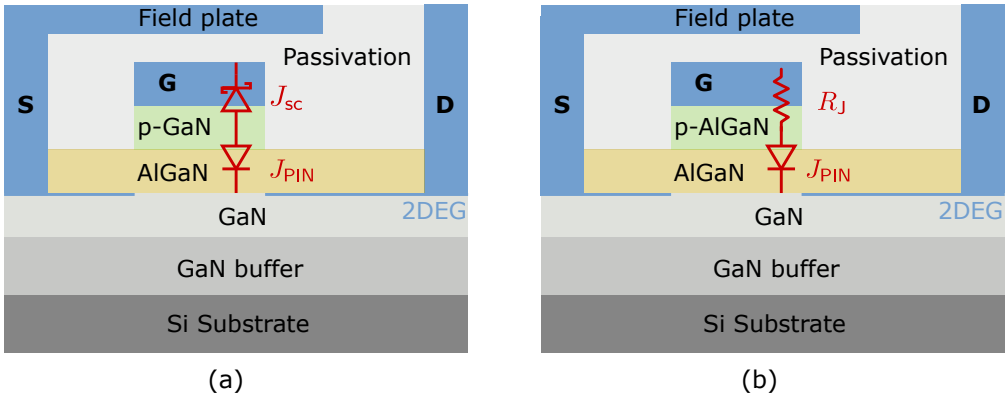


Figure 1.8: The structure and equivalent circuit of gate stack of (a) Schottky-type p-GaN gate HEMTs where the p-GaN layer is floated by two back-to-back diodes and (b) Ohmic-type p-AlGaN gate where the p-AlGaN layer is not floating. Note that the p-AlGaN is adopted as p-GaN in the first generation of gate injection transistors (GITs).

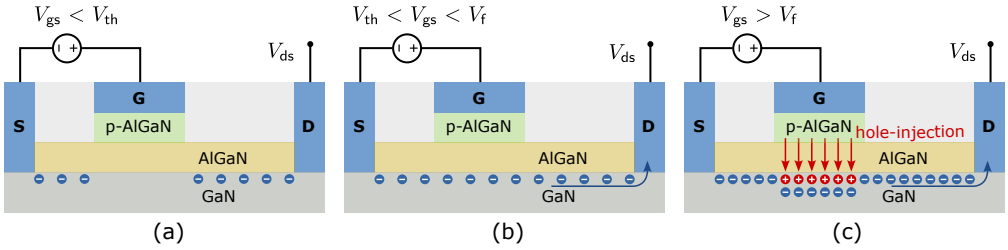


Figure 1.9: The schematic of operation principle of GITs (a) in off-state (b) on-state (c) the on-state with channel modulation function to increase channel conductivity [36].

magnitude gate leakage current under 6 V of V_{gs} bias compared to the fresh device, but the Schottky junction is still functional [35]. This is one of the reasons why no more than 6 V of V_g is recommended by GaN-HEMT manufacturers using this device architecture. Moreover, high electric field on the p-GaN or AlGaN layers can lead to the V_{th} shift phenomenon, which will be discussed in details in Section 1.3.

1.2.3.2 Ohmic-type p-GaN gate HEMTs (GITs)

To further increase the conductivity of 2DEG channel, the gate injection transistor (GITs) are proposed in [36], where the Ohmic-type contact between p-GaN and gate metal is adopted. It should be noted that the p-AlGaN layer is adopted, functioning as the p-GaN layer, in the first generation of the GITs, as shown in Fig. 1.8(b). Thanks to the Ohmic contact, the gate stack has higher V_g over-driving capability compared to the Schottky-type device.

The operation principle of Ohmic-type GITs is similar to the Schottky-type GaN-HEMTs. But the Ohmic-type GITs also enable a channel modulation function that can

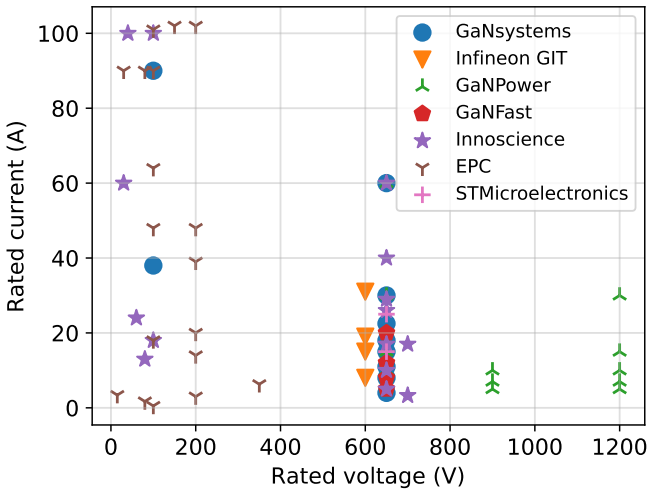


Figure 1.10: Distribution of rated voltage and current of a selection from the currently commercialised p-GaN gate HEMTs.

reduce the R_{on} of the transistors. The operation principle is shown in Fig. 1.9. When V_{gs} is less than V_{th}, the 2DEG channel is depleted by the p-GaN layer. When V_{gs} is higher than V_{th} but lower than the forward conduction voltage of the PIN junction (V_f), the 2DEG channel is formed, and electrons can move from source to drain, same as Schottky-type devices. However, if increasing the V_{gs} until it exceeds V_f, the PIN junction will forward conduct and holes can be injected to the 2DEG channel (the electrons injected to gate can be suppressed by the AlGaN/GaN barrier), as depicted in Fig. 1.9 (c). The injected holes can attract an equivalent amount of electrons from the source to conserve charge neutrality in the channel. Under positive V_{ds} bias, the attracted electrons drift toward the drain side, while the injected holes hold position around the gate due to their much lower mobility. In this way, the conductivity of the 2DEG channel gets improved.

The channel modulation function requires a continuous gate current (around 10 mA [37]) to maintain the hole injection, therefore, the GITs are known as current drive devices. Hence, the gate loop configuration can be more complicated and the driving losses can be more prominent than the Schottky-type GaN-HEMTs.

1.2.3.3 Power rating of commercialised p-GaN gate HEMTs

Mainstream GaN transistor vendors and their devices are summarised in Fig. 1.10 in terms of the distribution of rated voltage and current.[3] To be noted that all the listed GaN-HEMTs are discrete devices, which distinguishes them from power integrated circuits (ICs). The main rated voltage for p-GaN gate HEMTs is up to 650 V. However, Innoscience has released a 700 V rated voltage device, and GaNPower has developed a

[3]Data is sourced from the official websites of vendors at 25 °C. For simplicity, not all products are listed from one manufacturer; The listed products are for demonstrating the rated voltage and current ranges.

1.2 kV rated voltage engineering sample in 2024. For the devices under 200 V, the rated current can be up to 100 A. The maximum rated power is up to 39 kW for all commercialised p-GaN gate HEMTs. Combined with its superior high-frequency performance, power GaN-HEMTs are currently mainly used in fast chargers for consumer electronics, telecom, and data centers. It is anticipated that the applications in electrical vehicles or hybrid electrical vehicles (EVs/HEVs) and industrial will be the primary driver until 2030 for this specific market [38].

Moreover, all of the presented devices from Fig. 1.10 have adopted the Schottky-type p-GaN gate, except for the Infineon GIT, which uses the Ohmic-type p-GaN gate. For consistency, the Infineon GITs will be referred as Ohmic-type devices and other p-GaN gate HEMTs as Schottky-type GaN-HEMTs in the following of this work.

1.2.4 Vertical GaN power transistors

In addition to the commercialised lateral GaN-HEMTs, vertical GaN power devices are also under development, aiming to increase the breakdown voltage, current capability and solve the trapping effect issue of GaN-HEMTs [10]. In this subsection, the vertical GaN power transistors will be introduced by compared to the lateral GaN-HEMTs.

1.2.4.1 Drawbacks of lateral GaN-HEMTs

The drawbacks of GaN-HEMTs are mainly attributed to its technology responsible for lateral structures:

- The performance of GaN-HEMTs is sensitive to the surface traps and defects, because the current flow takes place close to the device surface [39]. These effects, along with the dynamic R_{on} and current collapse phenomena, will be discussed in detail in section 1.3.

- The breakdown voltage is limited by the length of gate-to-drain region [40], as illustrated in Fig. 1.4. Therefore, increasing the breakdown voltage is constrained by the lateral size of the device, and the R_{on} would be increased correspondingly. Moreover, the inhomogeneous distribution of electric field in the lateral device further limits the device breakdown voltage [41].

- GaN-HEMTs are naturally normally-on devices. Although the p-GaN technique can elevate the V_{th} to a positive value, the reliability issues associated with the gate stack and low V_{th} have a constant impact on the application usage of the device [42], [43], [44].

- GaN-HEMTs have a reduced avalanche capability due to the lacking of inherent p-n junction between source and drain (no drift region). Therefore, the holes generated during the impact ionisation and multiplication are limited, resulting in low avalanche capability. The reverse breakdown occurs when the reverse voltage exceeds the over-voltage limitation, rather than through avalanche energy [45],

[46]. Therefore, higher critical breakdown voltage of GaN-HEMTs is required when compared to the MOSFETs.

1.2.4.2 Characteristics of vertical GaN power transistor

Vertical structure GaN power transistors normally adopt the junction field-effect transistors (JFETs) [47], [48] or MOSFETs structure [49], which show significant potential in addressing the aforementioned issues. Firstly, surface states have less impact on device performance, as the electric field is mostly well distributed within the GaN layer, and so is the conducting current. Overall, the breakdown voltage of vertical devices is determined by the thickness of GaN drift region, and increasing the epitaxy thickness has negligible impact on the device size, compared with the lateral devices. Hence, vertical GaN transistors with 1.2 kV above breakdown voltage and low R_{on} have been successfully manufactured as reported in [48], [50]. Recently, the secrete GaN JEFT is starting to be commercialised by NexGen Power Systems with the maximum power rating in 1.2 kV and 35 A. Importantly, V_{th} above 3.5 V in GaN trench MOSFET is reported [49], showing the advantages of vertical GaN devices. Additionally, the vertical GaN transistors could have higher over-voltage ruggedness due to their improved avalanche ability compared to the lateral GaN-HEMTs. However, the body diode may become necessary again in the vertical GaN power transistors. Correspondingly, the channel conductivity of the vertical GaN transistors may be reduced due to the lacking of a 2DEG channel. Moreover, the tens of mA gate leakage current in the GaN-JFETs may not be negligible [51].

1.2.4.3 Challenges in vertical GaN devices

The superior performance of the above presented vertical devices is achieved by fabricating on bulk GaN substrates using the homo-epitaxy technique providing reduced lattice or coefficient of thermal expansion (CTE) mismatch. However, GaN substrates are extremely expensive, and the wafer diameter is typically limited to 2 inch [52], [53], making large-scale and long-term production hardly feasible. These expensive substrates are currently only used for fabricating specific devices, such as GaN laser diodes. Additionally, the growth process of bulk GaN crystals requires extreme conditions, such as temperatures above 2200 °C and nitrogen pressures exceeding 6 GPa [53]. Consequently, the GaN on foreign substrates like Si or SiC vertical devices are under development as the alternative to the GaN substrate based devices. In [54], a GaN-on-Si vertical MOSFETs is fabricated showing 645 V of breakdown voltage. However, significant challenges remain in improving device's performance by reducing its defects caused by the lattice and CTE mismatch.

In general, despite the significant potential of vertical GaN power transistors in achieving higher breakdown voltage, current capability and reliability, they address only a specific market due to the high cost of GaN substrates and the fabrication process.

1.2.4.4 Comparison between lateral and vertical GaN transistors

One the one hand, the maximum voltage and current ratings of commercially available lateral (from GaNPower) and vertical (from NexGen Power Systems) GaN power transistors are both limited to 1.2 kV and 35 A. However, vertical GaN devices demonstrate greater potential for higher breakdown voltage and current capability compared to their lateral counterparts. On the other hand, lateral GaN transistors may be more desirable for high-efficiency power conversion, owing to their low conductivity 2DEG channel and low inter-electrode capacitance.

1.2.5 Type of GaN transistors used in this study

It is necessary to mention the used GaN transistors in this study, as several GaN transistors with different technologies are introduced. In this study, power p-GaN gate HEMTs, to distinguish them from radio frequency (RF) GaN-HEMTs, are selected. Specifically, the 650 V GaN-HEMTs from GaN systems and 600 V GITs from Infineon are adopted as the samples for the Schottky- and Ohmic-type GaN-HEMTs, respectively. The performance variations between them could provide valuable information in transistor selection for GaN-based power converters, since these two technologies are mature and the vendors focus on a specialised market share. In the following text, GaN-HEMTs will represent both devices in general. When comparing between these two devices, the Schottky-type GaN-HEMTs will be used to distinguish from the GITs.

1.3 Trapping effect and parametric shift of GaN-HEMTs

GaN-HEMTs have received an increased interest in power electronics applications due to their low power losses and high frequency operation ability. However, they suffer from the parametric shift phenomena when subjected to voltage or hard-switching stresses, primarily manifesting as dynamic R_{on} and V_{th} shift for power devices [55], [56], [57]. These phenomena are mainly attributed to the trapping effect.

1.3.1 Trapping effect

The trapping effect refers to carriers being captured by traps in semiconductor devices under external stresses, such as an electric field. These traps originate from defects or interface states in GaN-HEMTs, which will be discussed further below.

1.3.1.1 Origin and locations of traps in GaN-HEMTs

From a material perspective, GaN, as an alloy of a III-V compound semiconductor, contain intrinsic defects such as atomic dislocations. Additionally, to achieve the p-GaN layer in the gate stack, acceptor impurities are mostly introduced by using the Mg-dopant, which mainly introduces shallow level acceptor traps in p-GaN or AlGaN layers [58]. For power devices, the C-doped GaN buffer is adopted to improve the breakdown

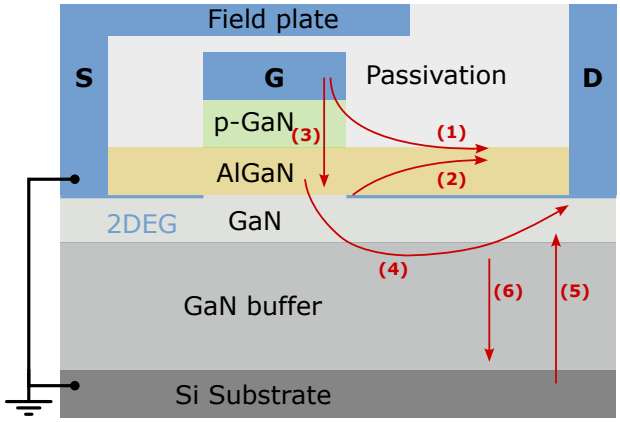


Figure 1.11: Carrier trapping paths under different stresses in GaN-HEMTs.

voltage and resistivity between drain and source, which can result in deep level acceptor or donor traps (mainly acceptor traps) [59]. Except the above mentioned impurity-related defects, various acceptor or donor traps exist in the interface of AlGaN/GaN or buffer layer because of the lattice mismatch as discussed in Section 1.2.

1.3.1.2 Leakage paths under different voltage stresses

The trapping mechanism occurs when carriers encounter traps, making the carrier leakage path essential for the occurrence of the trapping effect. Several leakage paths form when GaN-HEMTs are subjected to different stresses, accelerating the occurrence of trapping effect, influencing the device performance by affecting the normal electric field distribution in the device. The schematic of these leakage paths is depicted in Fig. 1.11.

(1) Gate-to-drain leakage path in passivation layer or AlGaN surface. When the device is subjected to off-state V_{ds} bias, gate leakage electrons can cross the passivation layer or migrate through surface traps of AlGaN. This path can be alleviated by, such as, a well designed field plate and applying passivation optimization techniques specific for power devices [25]. Note that electrons or holes can cross the AlGaN barrier in gate stack under high V_{ds} bias by the trap-assisted tunneling [60], [61], contributing to the gate-to-drain leakage current.

(2) Gate-to-drain region inside AlGaN layer or surface. In hard-switching transition, electrons in the 2DEG channel can be accelerated by the electric field, and the electrons can achieve sufficient kinetic energy (known as hot electrons) to overcome the barrier of AlGaN and partly get trapped inside AlGaN layer or in the surface states[62], [63].

(3) From gate metal to 2DEG through the p-GaN and AlGaN layers. As discussed in subsection 1.2.3, the gate stack of GaN-HEMT is not strictly insulated and

non-negligible gate leakage current forms when the gate terminal is subjected to positive V_{gs} bias [64], [65].

(4) Gate-to-drain region in the buffer layer. When the device undertakes high off-state voltage or hard-switching stresses, electrons can cross the buffer layer from gate to the drain side, forming a leakage path [10].

(5) From substrate to drain in buffer layer. As the substrate is connected to source inside power GaN-HEMTs, the high voltage drop is also shared by the buffer layer, therefore, enabling the existence of a measurable leakage current during high V_{ds} bias [35], [66]. The leakage path in the buffer is complex due to the introduction of C-dopant and defects related to different buffer structures and fabricating processes.

(6) From drain toward substrate in buffer layer. This leakage path is similar to path (5), but the direction is reversed as this path refers to hole trapping (emitting trapped electrons). This is due to the existence of donor traps in GaN buffer [60], [67].

It can be summarised that electron trapping mainly occurs when the device is subjected to V_{ds}, V_{gs} biases, or hard-switching stress. The locations are primarily distributed in the gate-to-drain region (in buffer layer) and the gate stack area. Trapped electrons in the gate-to-drain region can partly deplete the 2DEG channel, increasing the R_{on} or decreasing the maximum transconductance (g_m) of the device [68], [69], [70]. The V_{th} of device can be shifted positively, if electron trapping occurs in the gate stack [64], [65]. The parametric shift can be recovered gradually once the external stresses are removed. Moreover, the donor traps can also capture holes in some conditions, which could mitigate the effect caused by electron trapping in nearby.

1.3.2 Dynamic on-state resistance

The dynamic R_{on} effect is arguably the most well-known negative phenomenon in GaN-HEMTs, as it can increase the conduction losses of the device, leading to additional errors in efficiency evaluation and cooling design of power converter applications. As discussed in last subsection, it is mainly caused by the trapped electrons in gate-to-drain region inside the buffer layer. The electron trapping can be induced by the off-state V_{ds} bias or hard-switching stress, therefore, it is important to characterise the dynamic R_{on} effect before implementing the device inside power converters' design.

1.3.2.1 Characterisation methods

There are mainly two types of methods used to characterise the the dynamic R_{on} effect. One technique is based on the semiconductor curve tracer instruments (such as the B1505A from Keysight Technologies), the other one is based on the analysis of a customised circuit. The former is mostly utilised to investigate the long term voltage

bias (DC) induced dynamic R_{on} effect as the R_{on} is basically extracted from the Ohmic region of measured $I-V$ output characteristics. The main drawbacks of the curve tracer based methods can be mentioned as below:

- The measurement response time (t_m) in curve tracer is long, relating to the time period from the removal of the V_{ds} bias to the R_{on} measurement transient, as shown in Fig. 1.12(a). The dynamic R_{on} can recover once the V_{ds} bias is removed due to the de-trapping effect, and different orders of de-trapping time constants are reported, ranging from 1 µs to 10 s. [56], [71], [72]. Therefore, long t_m could underestimate the dynamic R_{on} effect, as the increased R_{on} is partially recovered during the t_m period.
- The minimum pulse widths, $^{dV_{ds}}/_{dt}$, $^{dI_d}/_{dt}$, and t_m are relatively large, making it unsuitable for characterisation of the dynamic R_{on} in high-frequency and continuous mode operation conditions.
- The power limitation force the measurements to be conducted on a low power interval, making it unsuitable for evaluating the influence of hard-switching stress (high V_{ds} and high I_d exist simultaneously) on dynamic R_{on} [73].

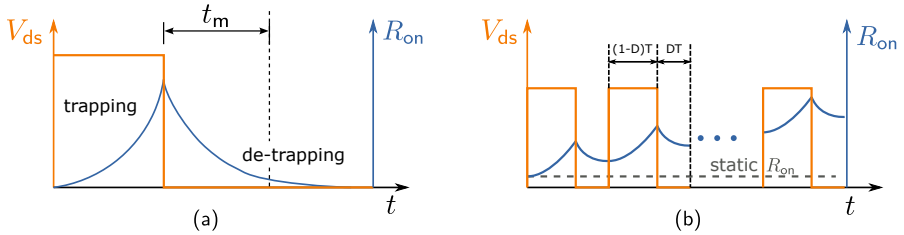


Figure 1.12: Schematic of R_{on} (a) measurement response time in dynamic R_{on} characterisation (b) dynamic R_{on} in continuous mode.

To address these issues, customised circuit based measurement methods have been proposed and will be mainly reviewed in this work. The customised circuits enable to emulate the voltage bias or hard-switching transitions similar to the conditions experienced by devices operating in power converters. In these techniques, the R_{on} is typically obtained by measuring the on-state V_{ds} and I_d of GaN-HEMTs. A clamping circuit is required to clamp the several hundred volts off-state V_{ds} to just several volts, allowing accurate measurement of the on-state V_{ds} using 12- or 8-bit digital oscilloscopes [74], [75]. It should be noted that the t_m in these methods generally depends on the stabilisation time of the clamping circuits. A short t_m is essential for dynamic R_{on} characterisation in high-frequency continuous mode conditions. Various clamping circuits with t_m in the order of tens of nanoseconds are able to characterise dynamic R_{on} in multi-MHz switching frequency as reported in [71], [72], [75], [76].

In the customised circuit based dynamic R_{on} characterisation, there are mainly two test conditions:

- **Single pulse mode:** the device under test (DUT) is subjected to a single-pulse test. By controlling the duration and amplitude of the V_{ds} bias, the relation between V_{ds} bias and dynamic R_{on} can be inferred in soft-switching. The influence of hot electrons on dynamic R_{on} can be evaluated by achieving a hard-switching condition [75]. The pulse mode is suitable for investigating the time resolved trapping and de-trapping phenomenon.

- **Continuous pulse mode:** the DUT operates continuously, similar to its functioning in power converters. In this mode, the dynamic R_{on} is influenced by the trapping and de-trapping mechanisms when the DUT is in off-state and on-state, respectively. The actual R_{on} is dependent on the accumulation of trapping and de-trapping mechanisms as depicted in Fig. 1.12(b). In addition to the trapping effect, the continuous mode will result in an increase of the junction temperature (T_j). Since the static R_{on} is directly related to the T_j, the manifestation of the dynamic R_{on} is linked to the rise of temperature rather than the trapping effect only. In other words, the increased R_{on} in continuous mode can be overrated due to the temperature increasing resulted from device operation. Hence, the control of self-heating is significant for accurate dynamic R_{on} characterisation.

1.3.2.2 Distribution of dynamic R_{on} for commercialised GaN-HEMTs

The reported dynamic R_{on} of commercial GaN transistors are summarised in Table 1.3. The data from both 650 V GaN-HEMTs and 600 V GITs is compared for double-pulse and respective continuous mode. It should be noted that the bias time and t_m are not standardised across data collected from various publications, even though they significantly influence the measured R_{on}. Therefore, the highest dynamic R_{on} from each test condition collected to provide a comparison based general overview.

In pulse mode, an approximately 1.5 times increase in R_{on} is reported under soft-switching for GaN-HEMTs, and the GITs show a slightly higher R_{on} for the same conditions. In hard-switching, the measured R_{on} is similar to that produced by soft-switching, however, two important points should be mentioned:

- The dynamic R_{on} of GaN-HEMTs increases dramatically once the load current exceeds 10 A, result that could be attributed to the hot electrons related trapping effect[4], which can happen during the hard-switching transition [75]. Also, a similar phenomenon is reported in [56] for the wafer level test.

- The dynamic R_{on} of GITs in hard-switching is significantly lower when compared to that resulted from soft-switching, effect explainable by the hole-injection mechanism provided by a hybrid p-GaN drain structure (PD-structure) as depicted in Fig. 1.13. According to [77], the hole-injection mechanism in the PD-structure is more likely to occur during hard-switching commutation. This PD-structure, proposed in [79], aims to suppress the dynamic R_{on} increase caused by electron

[4]The hot electrons refer to the electrons with high kinetic energy (accelerated by the high electric field), so that they can be captured in the GaN buffer or AlGaN layer.

Devices	Test condition	Type of switching	Power level	Normalised R_{on}
GaN-HEMTs	Pulse mode	Soft	400 V/10 A	1.62 [77]
	Pulse mode	Hard	400 V/10 A	1.63 [77]
	Pulse mode	Soft	400 V/8 A	1.2 [78]
	Pulse mode	Hard	400 V/25 A	7.1 [75]
	Pulse mode	Hard	400 V/10 A	1.2 [75]
	Pulse mode	Soft	200 V/2 A	1.5 [72]
	200 kHz	Soft	400 V/20 mA	1.45 [76]
	200 kHz	Soft	150 V/20 mA	1.78 [76]
	500 kHz	Soft	400 V/1 A	1.65 [71]
	1 MHz	Soft	400 V/15 A	1.82 [77]
	1 MHz	Hard	400 V/10 A	1.62 [77]
	1 MHz	Soft	200 V/2 A	1.74 [72]
	2 MHz	Soft	400 V/1 A	1.99 [71]
	5 MHz	Soft	400 V/1 A	1.81 [71]
GITs	Pulse mode	Soft	400 V/10 A	1.68 [77]
	Pulse mode	Hard	400 V/10 A	1.18 [77]
	Pulse mode	Soft	400 V/8 A	1.28 [78]
	Pulse mode	Soft	200 V/2 A	2.02 [72]
	1 MHz	Soft	400 V/5 A	1.99 [77]
	1 MHz	Hard	400 V/5 A	1.65 [77]

* The dynamic R_{on} are normalised by using static R_{on} at 25 °C. In [71], the dynamic R_{on} is normalised with the static R_{on} at the same T_c, as the T_c can ramp up to 80 °C under 5 MHz switching.

Table 1.3: Summary of normalised dynamic R_{on} of commercial GaN-HEMTs characterised by customised circuits.

trapping in the gate-to-drain access region and buffer layer. This device is called HD-GITs as well, which structure and hole-injection mechanism are depicted in Fig. 1.13. It should be noted that the GITs tested in this study feature the PD structure.

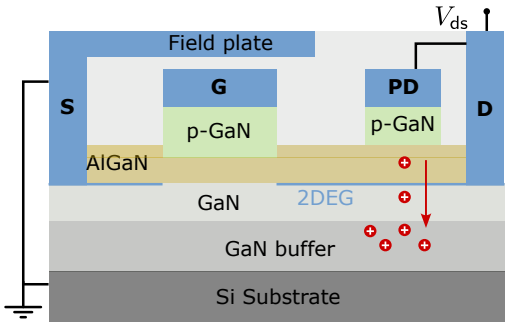


Figure 1.13: Schematic of the structure of HD-GITs and hole-injection mechanism from the PD-structure.

In the soft-switching of continuous mode, the dynamic R_{on} generally remains within the same range as that observed in pulse mode, typically less than twice of the static R_{on}. As previously discussed, the control of T_j is important but it cannot be directly measured. Hence, the case temperature (T_c) is monitored to estimate the T_j by exploiting the RC thermal model provided by the manufacturers' datasheet. In [72], [76], low load current is adopted to introduce less self-heating mitigating the influence of temperature. In [71], the measured dynamic R_{on} is normalised with the static R_{on} in the same case temperature. In this way, the temperature increased R_{on} can be compensated. In [71], the measured dynamic R_{on} initially increases and then slightly lowers down as the switching frequency rise. This behaviour can be explained by the decreased de-trapping time constant in high temperature, which is supported by several works [35], [80], [81]. The dynamic R_{on} in continuous mode is influenced by the accumulation of trapped electrons, which also depends on the history of trapping and de-trapping processes [55], as depicted in Fig. 1.12(b). A small de-trapping time constant helps to reduce the measured dynamic R_{on}. In hard-switching, the situation becomes more complicated due to the involvement of hot electrons related trapping and the impact ionisation generated holes [56], [82], [83]. These two mechanisms overlap, adding complexity to the overall behaviour study of dynamic R_{on}.

Generally, the impact of hard-switching stress on the dynamic R_{on} of Schottky-type GaN-HEMTs and GITs deserves further investigation, as hot electron trapping, impact ionisation, and hole-injection mechanisms (only for GITs) may coexist during the hard-switching transition. These phenomena observed during hard-switching could provide useful information about the device's degradation mechanism and life-time estimation [28], [84]. The relationship between the time constant of trapping and de-trapping with temperature is also an important aspect in dynamic R_{on} study. In high-frequency continuous mode, the dynamic R_{on} results from the accumulation of trapping and

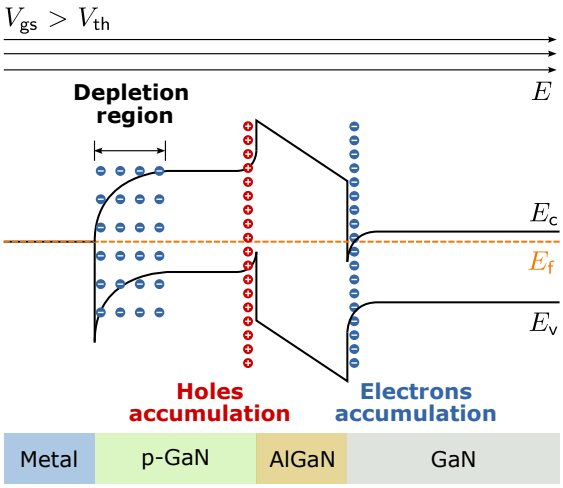


Figure 1.14: Depletion of p-GaN layer and carriers distribution in the gate stack of GaN-HEMTs when $V_{gs} > V_{th}$.

de-trapping effects, while the corresponding time constant can determine the final R_{on} under different switching frequencies and duty cycles.

1.3.3 Threshold voltage shift

The V_{th} shift phenomenon is more complex than the dynamic R_{on} phenomenon due to the complex gate structure, various types of traps and different carrier accumulation mechanisms present in GaN-HEMTs. The V_{th} shift has a critical impact on device application. For example, in the half-bridge configuration, a negative V_{th} shift could lead to the false turn-on phenomenon that can contribute to additional losses and even device breakdown [43], as the V_{th} of GaN-HEMTs is relative low with typically around 1.5 V. Therefore, it is essential to understand and characterise the V_{th} shift before placing the device in a specific application. A good practice will be to understand how GaN-HEMTs are turned on from carriers perspective before discussing the V_{th} shift phenomenon.

1.3.3.1 Turn-on mechanism of GaN-HEMTs

The V_{th} for the enhancement-mode GaN-HEMTs is lifted to a positive interval by introducing a p-GaN layer. As depicted in Fig. 1.14, when a positive voltage (higher than V_{th}) is applied to the gate, the Schottky contact is in reverse bias and the p-GaN layer is depleted. The depleted holes will be accumulated at the interface of p-GaN/AlGaN under the electric field, attracting electrons to form the 2DEG channel. In other words, it is the positive voltage potential in p-GaN layer that is responsible for device turn-on. Therefore, the carriers accumulated in the gate stack area can change the V_{th} by influencing the voltage potential in p-GaN layer.

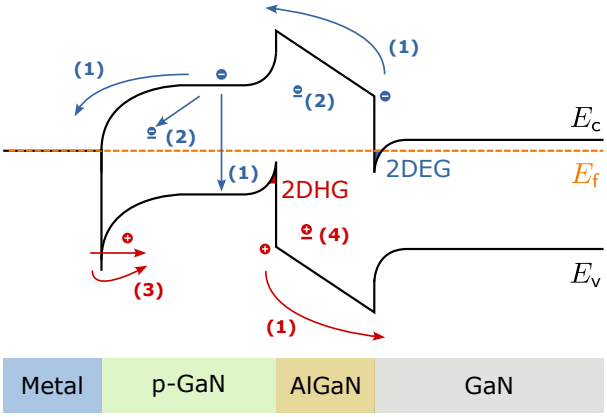


Figure 1.15: Main mechanisms related to the V_{th} shift under V_{gs} bias of Schottky-type GaN-HEMTs.

Moreover, the p-GaN layer is floating, sandwiched between two "back-to-back" diodes: the Schottky junction of metal/p-GaN and the PIN junction of p-GaN/AlGaN/GaN [64], [85], as depicted in Fig. 1.8 (a). Because of this floating property, the accumulated carriers in the p-GaN layer cannot get compensated immediately after removing the voltage bias, so that the remaining carriers can influence the voltage potential of the p-GaN layer, causing V_{th} shift phenomenon. **To summarise**, the potential of the p-GaN layer is sensitive to external voltage biases, hence, a V_{th} shift can be caused not only by the V_{ds} bias but also by the V_{gs} bias and even hard-switching stress.

1.3.3.2 Mechanisms related to the V_{gs} bias induced V_{th} shift

Both positive and negative V_{th} shifts are reported under the V_{gs} bias, phenomena that can be explained by the carriers accumulation in the gate stack. In Fig. 1.14, the ideal turn on mechanism is illustrated without considering transport carriers and trapping. However, these mechanisms occur in the real functioning, which influences the potential of p-GaN layer. The carriers transport and trapping mechanisms of Schottky-type GaN-HEMTs are depicted in Fig. 1.15, to reveal the mechanism of V_{gs} bias induced V_{th} shift.

(1) By increasing the V_{gs}, the p-GaN layer get continuously charged. Once the p-GaN potential is higher than the forward conduction voltage of the PIN junction, the electrons from the 2DEG can be injected into the p-GaN layer through the AlGaN barrier [64], [86], [87]. These electrons can recombine with holes in the p-GaN layer or be emitted through the gate contact. Meanwhile, holes can be injected into the 2DEG channel [64], [88]. Thus, the holes in the p-GaN layer suffer a partly depletion (called hole-deficiency), requiring a higher V_{gs} to turn on the device, which leads to a positive V_{th} shift.

(2) During the electron injection from 2DEG to p-GaN layer, the electrons can also be

captured by the acceptor traps (Mg-dopant related) in the p-GaN, AlGaN layers or the P-GaN/AlGaN interface [58], [65], [89], [90]. These trapped electrons can further reduce the potential of p-GaN layer, causing a positive V_{th} shift.

(3) When the V_{gs} is higher (normally above 5 V [88], [89], [91]), the Schottky barrier becomes thinner. Hence, more holes can be injected into the p-GaN layer by tunneling or due thermionic emission [64], [88], replenishing the depleted holes (alleviating the hole-deficiency) and increasing the p-GaN potential. Therefore, the positive V_{th} shift can be compensated. Under long-time V_{gs} bias (higher than tens of millisecond [88], [89]), it could result in a negative V_{th} shift.

(4) The injected holes can also get trapped in the AlGaN layer under a high and long-time of V_{gs} bias, the corresponding donor traps may be related to the nitrogen-vacancy of AlGaN layer [86], [88], [92]. The trapped holes enable to attract the electrons under the gate stack, leading to negative V_{th} shift.

It should be noted that the metal/p-GaN contact of GITs is Ohmic-type. Under the V_{gs} bias, enough holes can be injected to the p-GaN layer, preventing the hole-deficiency phenomenon, as discussed in Fig. 1.9. Therefore, a positive V_{gs} bias may not lead to positive V_{th} shift for GITs, and a negative V_{th} shift is more likely to occur due to the hole-injection from gate contact. This inference is verified through TCAD simulation in [64] and by experiment in [88], [91].

The above discussion is summarised in Table 1.4. The holes can be depleted and cannot be replenished due to the floating p-GaN layer of GaN-HEMTs, the process potentially leading to a positive V_{th} shift. This hole deficiency can be alleviated by the hole-injection mechanism under high V_{gs} bias, aimed to induce a negative V_{th} shift. Overall, other mechanisms such as electron trapping in the p-GaN or AlGaN layer or hole trapping in the AlGaN layer can respectively induce as a positive or negative V_{th} shift. From all the phenomena mentioned, the electron trapping might be the dominant one due to the high concentration of acceptor traps involved [60], [94]. [58], [93].

Mechanisms	GaN-HEMTs	GITs
Hole-deficiency in p-GaN layer	Low V_{gs} bias	✗
Hole injection	High V_{gs} bias	✓
Electron trapping	✓	✓
Hole trapping	✓	✓
V_{th} shift	Positive / Negative	Negative

Table 1.4: Summary of the V_{gs} induced V_{th} shift mechanisms for Schottky-type GaN-HEMTs and GITs.

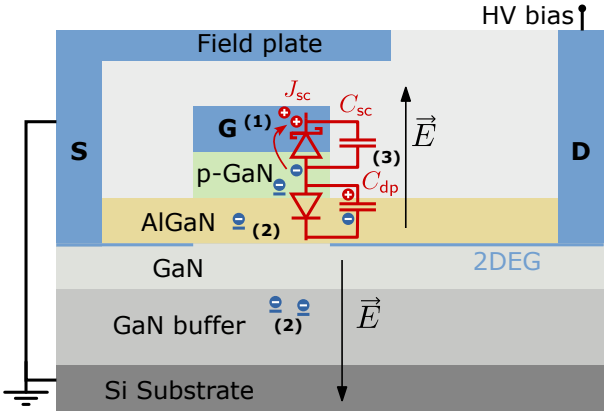


Figure 1.16: Mechanisms of off-state high V_{ds} voltage bias induced V_{th} shift: (1) Hole-deficiency in p-GaN layer. (2) Electron trapping in p-GaN/AlGaN heterojunction or GaN buffer layer. (3) p-GaN potential is elevated by V_{ds} due to the in series C_{sc} and C_{dp}.

1.3.3.3 Characterisation method for the V_{gs} bias induced V_{th} shift

The V_{gs} bias induced V_{th} shift is typically characterised by the "measure-stress-measure" sequence using a curve tracer [65], [87], [89], [94]. In this method, the transfer characteristics are periodically measured by sweeping the V_{gs} from 0 to 6 V in several second (called measure stage), while a constant V_{gs} bias (in different voltage or stress time and called stress stage) is applied between each measurement period to investigate its influence on V_{th} shift. It should be noted that the DUT under this measurement sequence operates differently compared to a real application conditions where the applied V_{gs} rises and falls between 0 and 6 V in tens of nanosecond. Moreover, the time interval between "stress" and "measure" can reach up to several second [89], delay that makes this method unsuitable for the monitoring of V_{th} shift with fast recovery time constant. In [88], [91], customised circuits with faster t_m are proposed to address the delayed measurement issue.

It should be noted that the duration of the V_{gs} bias could be a more notable parameter acting on the V_{th} than the amplitude of V_{gs} from a device application point of view. Because the commercial GaN-HEMTs are recommended to be driven by a V_{gs} of 6 V, limiting the device exploitation range. In contrast, both the duration and amplitude of V_{ds} bias vary significantly in power converter applications, highlighting the need for further investigation into the corresponding V_{th} shift.

1.3.3.4 Mechanisms related to the V_{ds} bias induced V_{th} shift

Several mechanisms are responsible for the V_{ds} bias induced V_{th} shift of GaN-HEMTs due to the floating p-GaN layer discussed in Fig. 1.8(a) and to various traps in the gate stack. The three mechanisms are illustrated in Fig. 1.16 while the explanation about the involved processes is provided as follows:

(1) The gate stack of GaN-HEMTs is composed with two "back-to-back" diodes. When the device experiences an off-state V_{ds} bias, the PIN junction (p-GaN/AlGaN/GaN) works in reverse bias and the electrons in p-GaN are accumulated at the interface of p-GaN/AlGaN. Simultaneously, holes in p-GaN are emitted out of the gate stack through the forward biased Schottky junction (J_{sc}). However these holes cannot return to the p-GaN layer immediately after the V_{ds} bias is removed, since the J_{sc} is in reverse bias. These unrestored holes can cause a hole-deficiency in the p-GaN layer, this phenomenon leading to positive V_{th} shift [64], [85], [95].

(2) As a leakage path from the gate to the drain terminal exists in Fig. 1.11, when the device undertakes high V_{ds} bias, and the leakage current could result in the electron trapping on the gate stack. As well, the acceptor traps in the buffer layer underneath the gate stack can capture electrons under high V_{ds} bias, therefore, reducing the electron density under the gate. Overall, these trapped electrons can induce a positive V_{th} shift as discussed in [35], [96].

(3) The Schottky and PIN junctions' equivalent capacitors C_{sc} and C_{dp} are in series configuration as shown in Fig. 1.16. In this state, the p-GaN potential can be elevated under the V_{ds} bias, meaning that less V_{gs} is required to turn-on the device, this process inducing a negative V_{th} shift. The mechanism is reported as the "Gate/Drain Coupled Barrier Lowering (GDCBL) effect" in [73], [97]. To be noted that the potential of p-GaN layer cannot be elevated indefinitely along with the increasing of V_{ds}, because the p-GaN potential will be clamped once the J_{sc} gets in conduction mode, and the capacitive coupling between C_{dp} and C_{sc} becomes smaller when V_{ds} increases.

Similarly, the p-GaN layer of GITs is not floating as mentioned in Fig. 1.8(b), thus, it does not have the hole deficiency or the GDCBL effect. Electron trapping in the gate stack and buffer layer can occur under the off-state V_{ds} bias state. However, once the device is turned on, the hole injection through the gate stack may compensate for the trapped electrons.

1.3.3.5 Characterisation method for the V_{ds} bias induced V_{th} shift

As a fundamental characterisation equipment for semiconductor devices, the curve tracer can be employed to characterise and analyse the mechanisms of V_{ds} bias induced V_{th} shift as mentioned in [35], [73], [85], [96]. However, the relatively long measurement response time t_m makes it difficult to capture the V_{th} shift with a fast recovery time constant. For example, a t_m up to seconds range between high voltage stress and low voltage measurement period is reported in [35]. This method is not suitable for characterising the V_{th} shift in high-frequency continuous mode, due to the long t_m. Additionally, the influence of V_{gs} bias cannot be fully excluded, as the transfer characteristics requires to be measured in this method to obtain the V_{th}, where the V_{gs} bias is necessary for transfer characteristics measurement.

Several custom circuit-based methods are proposed to characterise the V_{ds} biased induced V_{th} shift. In [98], a half-bridge with a current source-based measurement circuit is proposed to evaluate the V_{ds} bias induced V_{th} shift: A constant current provided by the current source flows through the DUT during the V_{th} measurement stage, and the V_{th} shift is obtained by comparing the measured V_{th} before and after the V_{ds} bias. Moreover, this method allows for the observation of the time-resolved V_{th} recovery effect. However, the t_m of this circuit is not mentioned, and its ability to characterise the V_{th} shift in continuous mode is not reported.

In [99], a bootstrap circuit is proposed to measure the V_{ds} bias induced V_{th} shift, based on the third-quadrant conducting characteristics of GaN-HEMTs. A fast t_m (60 ns) is reported for this circuit and it is able to measure the V_{ds} bias induced V_{th} in continuous mode up to 2 MHz. However, this method requires an active source included clamping circuit, complicating the measurement setup. Moreover, a specific power loop is required, which is not compatible with the standard half-bridge.

In [100], [101], [102], a V_{th} extraction method based on hard-switching waveforms is reported, where the measured V_{gs} and I_d are used to plot the transfer characteristics while the V_{th} can be determined. This method enables to characterise the V_{th} shift during hard-switching, but a big gate resistor R_g is required to slow down the switching waveforms to eliminate the influence of parasitic parameters and probe propagation delays. However, the big R_g is not accounted for the normal operation case for GaN-HEMTs.

In [103], a half-bridge circuit with a capacitor in series inside the power loop is proposed to measure the V_{ds} bias related V_{th} shift. One side of the capacitor is connected to the source terminal of the low-side DUT, and the other side is connected to the ground. The V_{ds} bias is applied to the DUT when the high-side device is in on-state. Then, the DUT is turned on, and the current charges the capacitor, increasing the potential of the source terminal of the DUT. When the V_{gs} drops below the V_{th}, the DUT turns off, and the V_{gs} is clamped to the V_{th}. However, the V_{ds} bias is always present during the V_{th} measurement stage, and the measured V_{th} is the result of off-state V_{ds} bias and hot-electrons stress. Additionally, the V_{th} recovery behaviour might be underestimated in this method, as the V_{ds} bias still exists during the V_{th} measurement stage. Whereas, the measurement performance under high V_{ds} bias (400 V) and continuous mode are not discussed.

The advantages and disadvantages of above V_{th} instability characterisation methods are summarised in Table 1.5. It can be concluded that a V_{th} shift measurement method with a fast measurement response time is essential for characterising the V_{th} shift in continuous mode. Additionally, it is important that the measurement method can be half-bridge compatible and easy to implement: a half-bridge compatible method not only facilitates in-situ measurement (characterising the V_{th} in actual power converter applications) but also makes it more accessible for power electronics engineers to evaluate the V_{th} shift for GaN-HEMTs.

characterisation methods	Advantages	Disadvantages
[35], [73], [85], [96]	Automatic measurement	Long measurement response time; Long pulse width; V_{gs} bias not excluded
[98]	Short pulse width	No continuous mode
[99]	Fast measurement response; Continuous mode	Complicated clamping circuit
[100], [101], [102]	Able to evaluate V_{th} shift during hard-switching	Large R_g required
[103]	Short pulse width; No clamping circuit	No continuous mode; Low voltage only test; Not typical switching condition

Table 1.5: Summary of the characterisation methods for V_{ds} bias induced V_{th} shift.

1.3.3.6 Two types of V_{ds} bias induced V_{th} shift

The maximum reported value for the V_{ds} bias induced V_{th} shifts are compared in Fig. 1.17, where the data is from the studies in Table 1.5. To be noted that the V_{ds} bias time and measurement response time in these studies are not the same, so the results can only indicate the general level of the shifted V_{th}. Moreover, the rated and bias voltages of the investigated devices are different, so the V_{ds} bias is normalised to the corresponding rated voltage to show the bias amplitude. As shown in Fig. 1.17, different levels of positive V_{th} shift under V_{ds} bias are compared for commercial GaN-HEMTs. The variation could be related to the varying V_{ds} bias time, strength or different trap mechanisms.

Interestingly, opposite V_{th} shifts are reported for the same device in [73] and [99], as the negative shift being an unusual effect. The Schottky-type GaN-HEMTs typically exhibit a positive V_{th} shift under V_{ds} bias. Therefore, it is necessary to critically analyse their measurement setups and methods. For a clear comparison, two studies [35], [73] using the same curve tracer (B1505A) to characterise the similar Schottky-type GaN-HEMTs (GS66502 and GS66504) are examined. When the V_{th} is measured by a curve tracer, the transfer characteristics are tested at first by increasing the V_{gs} pulse with constant V_{ds} bias, afterward the V_{th} can be extracted from the measured transfer characteristics, as shown in Fig.1.18. In Fig.1.18(a), the transfer characteristics are measured under low V_{ds} (typically 1 V to limit the on-state current), while a high V_{ds} voltage is applied between each measurement pulses as the V_{ds} bias. It should be noted that the high V_{ds} bias is applied when the device is in the off-state, which is the typical

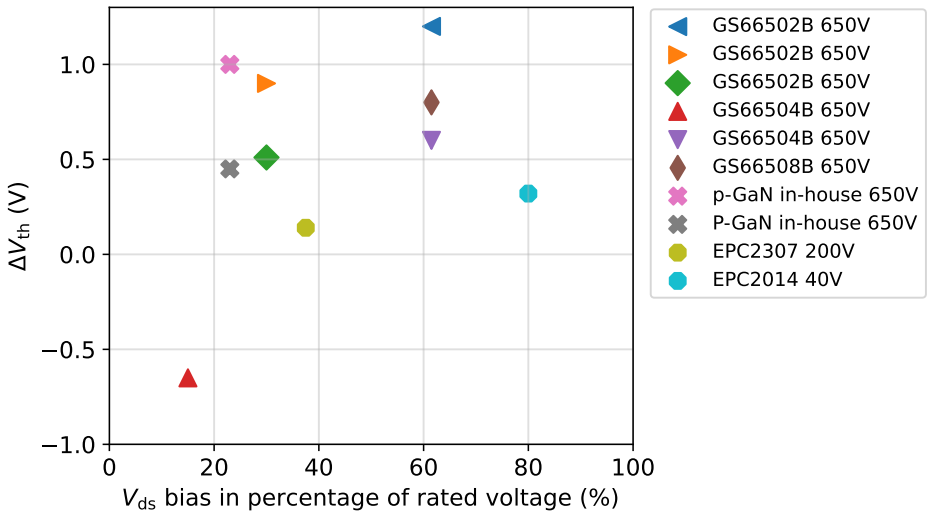


Figure 1.17: The maximum reported V_{ds} bias induced V_{th} shifts in Table 1.5.

condition when discussing V_{ds} bias induced V_{th} shift, and a positive V_{th} shift is reported [85], [96], [99]. However, in Fig.1.18(b) the transfer characteristics are tested under high V_{ds}, here, the high V_{ds} does not refer to the off-state V_{ds} bias but to a semi-on state. Consequently, the V_{th} shift mechanisms differ, explaining why opposite V_{th} shifts are observed for similar devices. In this condition, the V_{ds} is limited to 100 V, and the measurement pulse width is kept very short to avoid high on-state current.

Classifying the V_{ds} bias is important, as the timing of the V_{ds} bias appearance differs when the device operates in power converters. For example, when the device is in the off-state, the V_{ds} bias is similar to that illustrated in Fig. 1.18(a), but when the device is in functioning a hard-switching transition (semi-on-state), the V_{ds} bias in Fig. 1.18(b) occurs. In the semi-on-state, hot electron related trapping [56] and impact ionisation [83] are reported, where these two mechanisms could influence the electron trapping state in the GaN-HEMTs as well. These two types of V_{ds} biases can cause opposite V_{th} shift, therefore, they are classified as I-type and II-type V_{ds} bias in this work, as illustrated in Table. 1.6. Opposite V_{th} shift is reported under these two types of V_{ds} bias due to the activation of different shift mechanisms.

Consequently, the test conditions and the corresponding mechanisms must be clarified before investigating the V_{ds} bias induced V_{th} shift. These observations strongly advocate the necessity of in-situ V_{th} measurement for the GaN-HEMTs based power converter designs.

1.3.3.7 Influence of V_{th} shift on device application

The V_{th} of GaN-HEMTs is raised to a positive interval, but it remains relatively low compared to the Si-MOSFETs. Hence, the negative V_{th} shift could be detrimental to the device, as it can result in the false turn-on phenomenon [43]. The false turn-on can

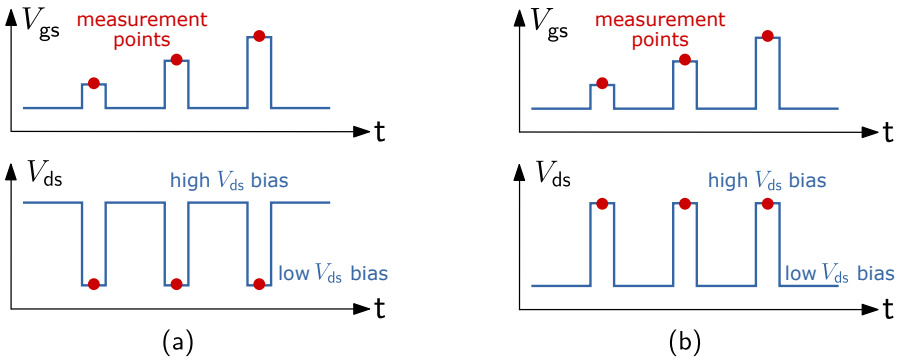


Figure 1.18: Measurement sequence of V_{ds} induced V_{th} shift using curve tracer (a) in study [35] (positive V_{th} shift) and (b) in study [73], where the channel current is limited to 1 mA under high V_{ds} bias to mitigate device self-heating (negative V_{th} shift).

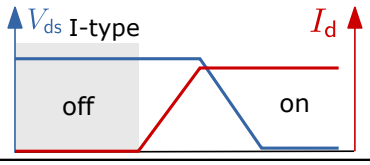
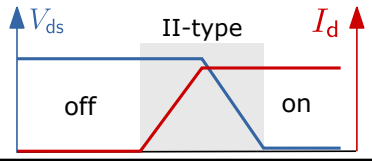
V_{ds} bias	I-type V_{ds} bias	II-type V_{ds} bias
V_{th} shift	positive[35], [85], [96], [98], [99], [104], [105]	negative[43], [73], [97], [101]
Mechanisms illustrated in Fig. 1.16	(1) Hole-deficiency in p-GaN layer [64], [85], [95]; (2) Electron trapping in AlGaN layer and GaN buffer[35], [96]	(3) p-GaN potential is elevated by V_{ds}[73], [97]
Device state switching commutation	off-state	semi-on-state
Switching waveforms		

Table 1.6: Two types of V_{ds} bias related V_{th} shift.

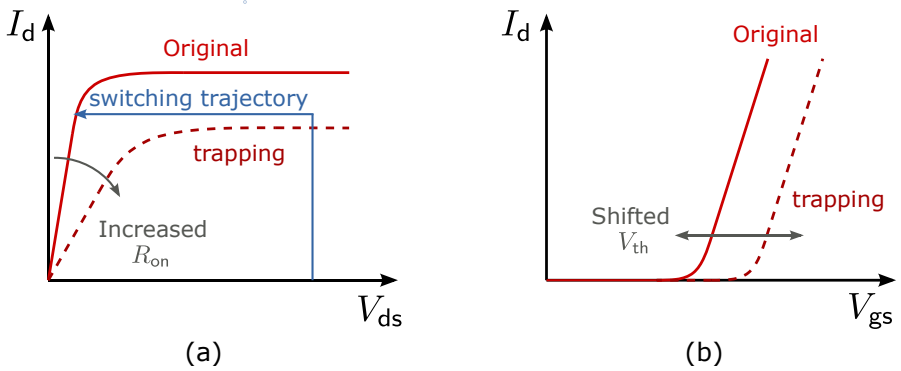


Figure 1.19: Trapping effect in (a) output characteristics and (b) transfer characteristics.

cause not only an increase in switching losses but also device failure in some conditions, therefore, including the GaN-based device in power application designs becoming a very challenging task.

The V_{th} is used as a temperature sensitive electrical parameter (TSEP) to measure the T_j of Si-IGBTs [106], [107] or SiC-MOSFETs [108], [109], however, it is challenging to adopt this method for GaN-HEMTs due to the voltage bias induced V_{th} shift. Therefore, it is helpful to determinate if the V_{th} of GaN-HEMTs can be a TSEP by characterising their voltage bias induced V_{th} shift phenomenon.

The influence of trapping effect on device's $I-V$ characteristics can be depicted in Fig. 1.19, where the increased dynamic R_{on} is expressed as the reduced slope in the Ohmic region of output characteristics, while the positive shifted V_{th} can be shown as the shift of the transfer characteristics. Moreover, since the transfer characteristics are closely related to the device switching transition, the V_{th} shift may influence the device's switching behaviour. This aspect has been less investigated in the literature, but it is crucial for GaN-HEMTs, as the devices primarily operate on high-frequency conditions, where the switching losses and the electromagnetic interference (EMI) emissions are significant. The slow down on switching commutation is reported after the V_{ds} bias and it is attributed to the positive V_{th} shift but without providing a demonstration [98], [104], [105]. The V_{ds} bias induced trapping effect can also influence the $C-V$ characteristics of GaN-HEMTs [110], which in turn can significantly impact the device's switching behaviour. Therefore, it cannot be directly inferred that the slowed switching speed is solely due to the positively shifted V_{th}. **To summarise**, it is important to investigate and demonstrate the influence of V_{th} shift on device switching behaviour.

1.3.4 V_{th} shift issues investigated in this work

As discussed previously, the dynamic R_{on} can be linked to the V_{ds} bias induced trapping effect. Various studies document and popularise it to the research community whereas, the voltage bias induced V_{th} shift and its impact on device application remain still hidden to the large audience. This work focuses on several voltage bias induced V_{th} shift

unanswered questions summarised as follows:

- In-situ V_{th} characterisation considering the actual device operation condition in power converters. Opposite V_{th} shifts have been reported for the same device under different type of V_{ds} bias. The complicated V_{th} shift related mechanisms indicates that it is essential to evaluate the V_{th} shift with carefully considering the device operation conditions, such as pure off-state bias (I-type V_{ds} bias) and hard-switching transition (II-type V_{ds} bias). Moreover, the switching speed of GaN-HEMTs is so fast that the static test results from curve tracer cannot reflect the actual device characteristics during the switching transition. Consequently, the in-situ V_{th} characterisation method is necessary to reveal the actual V_{th} when device operating in power converters.

- Evaluating the V_{th} shift phenomenon of GITs under the V_{ds} bias. From the operation mechanism of GITs, the p-GaN layer forms an Ohmic-contact with the gate metal and the hole-injection mechanism through the Ohmic gate contributes to release the trapped electrons in gate stack. Also, the hole-injection from the PD-structure might neutralise the trapped electron under V_{ds} bias, but there is no experimental demonstration (Only the decreased R_{on} in experiment is reported in [77]). The above mechanisms indicate an alleviated positive or even negative V_{th} shift for GITs under the voltage bias. However, the V_{th} shift phenomenon of the GITs is less characterised from the literature. One research implementing the curve tracer based test method announces that the GITs device have a stable V_{th} under V_{ds} bias because of the non-floating p-GaN layer [73]. And same conclusion is drawn under the pure V_{gs} bias in [91]. However, the V_{th} shift phenomenon under continuous V_{ds} bias, combined with a fast measurement response time t_m, remains to be evaluated.

- If and how the V_{th} shift can influence the switching behaviour of GaN-HEMTs. Since the $I-V$ characteristics determine the steady-state point of the transistors, the V_{th} shift may influence the switching behaviour of GaN-HEMTs. This requires further investigation because the switching behaviour is closely related to switching losses and EMI issues, which are significant for GaN-HEMTs applications.

The in-situ V_{th} shift measurement for Schottky-type GaN-HEMTs and GITs will be discussed in detail in Chapter 2 and the influence of V_{th} shift on device's switching behaviours will be discussed in Chapter 3.

1.4 Impact of parasitic parameters on GaN-HEMTs application

There are several challenges to overcome for driving the GaN-HEMTs efficiently to fully unleash their performance on fast switching and reduced power losses. For example, the ultra-fast switching can induce high-frequency oscillations, resulting in severe EMI. Additionally, special attentions should be given to avoid the false turn-on issue during

the switching commutation, since the fast commutation speed can induce voltage spikes on its low V_{th}.

1.4.1 Small inter-electrode capacitance and fast switching speed

The low switching losses of GaN-HEMTs and their sensitivity to parasitic parameters are both determined by the small inter-electrode capacitance.

1.4.1.1 Origin of small inter-electrode capacitance in GaN-HEMTs

Thanks to the low relative dielectric permittivity ϵ_r, the inter-electrode capacitance of GaN-HEMTs can be much smaller in size as compared with the same designs implemented on different materials. Relative high E_{crit} of GaN contributes to reducing the length of drain-to-gate access region, therefore the overall size of the GaN-HEMTs can be reduced, resulting in small parasitic capacitances. Additionally, as shown in Fig. 1.4, the lateral structure enables the gate, source and drain terminals to be on the same plane, contributing to the delivery of reduced gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}) [111].

1.4.1.2 Inter-electrode capacitance comparison between MOSFETs and GaN-HEMTs

Table 1.7 compares the inter-electrode capacitances[5] of some Si- and SiC-MOSFETs with two GaN-HEMTs at similar power level. It can be seen that the input capacitance (C_{iss}) of GaN-HEMTs is approximately ten times smaller than that of Si-MOSFETs, this difference enabling the fast charge and discharge of the gate capacitance with small driving losses. Also, GaN-HEMTs have the smallest reverse capacitance (C_{rss}), fact that helps to alleviate the Miller effect during hard-switching transition, also increasing the switching speed. Although, due to the structure of lateral devices, the output capacitance (C_{oss}) of GaN-HEMTs is not significantly smaller compared to Si- or SiC-MOSFETs [47], the generally smaller inter-electrode capacitance still enables ultra-fast switching speeds for GaN-HEMTs.

1.4.1.3 Fast switching speed of GaN-HEMTs

The switching transition times of GS66508P and SCT2120AF are compared in [74], where a double-pulse test (DPT) with an inductive load is implemented to obtain the hard-switching waveforms. The current transition times during turn-on (from 10 % to 90 % of peak current) at 10 A of target I_d are 8 ns for the SiC-MOSFET and 5 ns for the GaN-HEMTs, while the voltage transition times during turn-off (from 10 % to 90 % of DC voltage) are 16 ns and 6 ns at 300 V of V_{ds}, respectively. These measurement results show the ultra-fast switching capability of GaN-HEMTs while advocating the importance of inter-electrode capacitance on device switching behaviour. Moreover, the ultra-fast switching speed of GaN-HEMTs makes parasitic parameters non-negligible. For

[5] Refers to the parasitic capacitors between gate, drain and source terminals of transistors.

Devices	Model	V_{ds} (V) / I_d (A)	C_{iss} (pF)	C_{rss} (pF)	C_{oss} (pF)
Si-MOSFET	SiHG22N65E	650 / 22	2415	10.5	59
SiC-MOSFET	C3M0120065D	650 / 22	640	1.2	45
SiC-MOSFET	SCT2120AF	650 / 30	1200	13	90
GaN-HEMT	GS66506T	650 / 22.5	185	0.7	49
GaN-HEMT	GS66508P	650 / 30	242	1.5	65

* Data in this table is from the manufacturer datasheet.
** The C_{iss}, C_{rss} and C_{oss} are measured under $V_{gs} = 0\,V$, $V_{ds} = 400\,V$.

Table 1.7: Comparison of inter-electrode capacitance of Si- and SiC-MOSFETs and GaN-HEMTs.

example, a dI_d/dt of 2 A/ns can induce a 2 V voltage drop across a parasitic inductance of 1 nH, and a 40 V/ns dV_{ds}/dt can lead to 4 A displacement current through 100 pF parasitic capacitance. Hence, it is important, when designing the PCB layout and routing, for GaN-HEMTs to minimize the parasitic inductance and/or capacitance, especially for the gate and power loops.

1.4.2 Influence of parasitic parameters on GaN-HEMTs switching behaviour

As discussed in the last subsection, circuit parasitic parameters can induce notable current and voltage spikes during switching. These induced voltages or currents can superimpose on the main switching waveforms, influencing the device's commutation behaviour and EMI emissions. Increased losses, severe overshoot even oscillation instabilities are attributed to the parasitic circuit parameters in GaN-HEMTs application.

1.4.2.1 Parasitic inductance in the half-bridge circuit

To comprehensively illustrate the influence of parasitic inductance on device switching behaviour, the lumped parasitic inductance present in a half-bridge configuration is depicted in Fig. 1.20. The power loop parasitic inductance (L_d) primarily originates from the PCB trace looped through the power device towards the C_{DC} and the pin connections of the power device's package. The L_g^H and L_g^L are the gate loop parasitic inductance (L_g) from the high-side and low-side respectively. And the L_{cs}^H and L_{cs}^L represent the corresponding common-source inductance (L_{cs}), which is the inductance shared by the power loop and gate loop.

During current commutation, the large dI_d/dt can induce a voltage drop across L_d, leading to severe overshoot on the measured V_{ds} of the low-side device during turn-off commutation. Moreover, the dI_d/dt can be decreased by L_d due to the increased inductive reactance, as reported in [112], [113], [114]. A big L_g could slow down the charging/discharging speed of C_{iss} of the device, decreasing the commutation

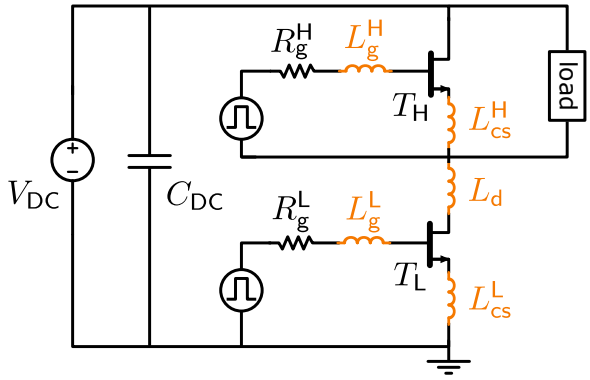


Figure 1.20: Lumped parasitic inductance in the half-bridge.

speed during the commutation [114], while L_g and C_{iss} can resonate, leading to severe oscillation in V_{ds}. To be noted that the influence of L_g^H on the low-side device can be neglected, and vice versa [112].

The common-source inductance primarily originates from the connection of the source terminal inside the device package, also shared by the power and gate loops. Although the L_{cs} of GaN-HEMTs is reduced to several hundred pico-henries (pH) by the use of surface mount technology (SMT), its impact on device switching commutation is still important. This is because the dI_d/dt (from the power loop) is very high, and the induced voltage can obstruct the charging and discharging process in the gate loop. The phenomenon is depicted in Fig. 1.21, where the low-side transistor is assumed as a current source with three inter-electrode capacitances. During the turn-off transition, the dI_d/dt can induce negative voltage drop on the L_{cs} and this voltage can charge the C_{iss} of GaN-HEMTs. However, the $C_{iss} = C_{gs} + C_{gd}$ occurs in discharging process during turn-off transition, so the L_{cs} can slowdown the turn-off commutation speed (same negative feedback effect for the turn-on transition). This phenomenon is broadly reported for SiC-MOSFETs as well in [112], [113], [114]. To be noted that even with the adoption of a Kelvin connection, the L_{cs} cannot be fully eliminated.

An experimental switching waveform a GaN-HEMT (GS66502B) is shown in Fig. 1.22, where the ultra-fast commutation in approximately 10 ns is displayed but with severe current and voltage oscillations, also know as switching ringing. More severe phenomena induced by parasitic inductance and other parameters will be discussed in the following sections.

1.4.2.2 False turn-on and gate instability phenomenon

As discussed in the last subsection, parasitic inductance can induce notable voltage overshoot during the fast switching commutation of GaN-HEMTs. This voltage overshoot can resonate between the parasitic inductance and the inter-electrode capacitance, resulting in significant current and voltage oscillations. High-frequency oscillations in the power loop can cause severe EMI issues, while oscillations in the gate loop are more

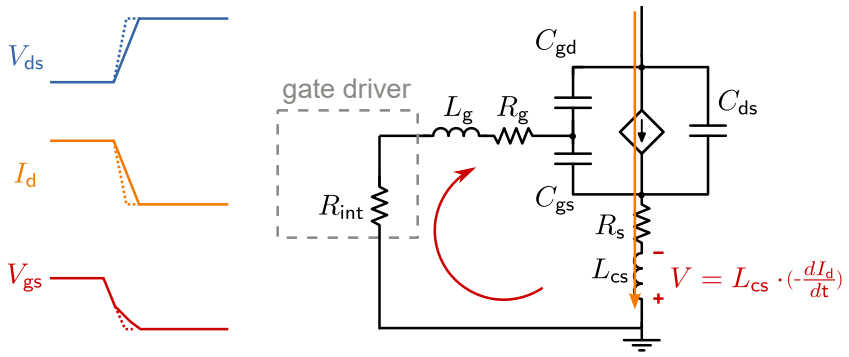


Figure 1.21: Influence of L_{cs} on the switching commutation speed (dashed line represent the switching waveform without L_{cs}).

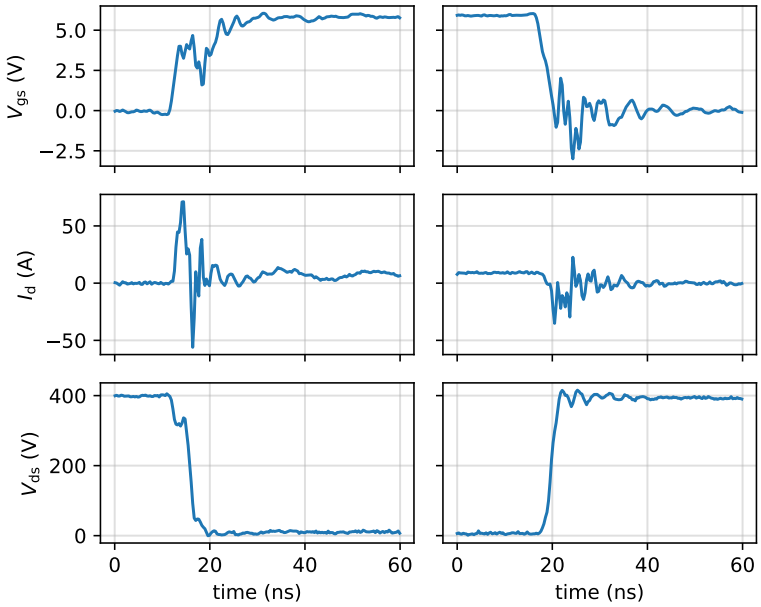
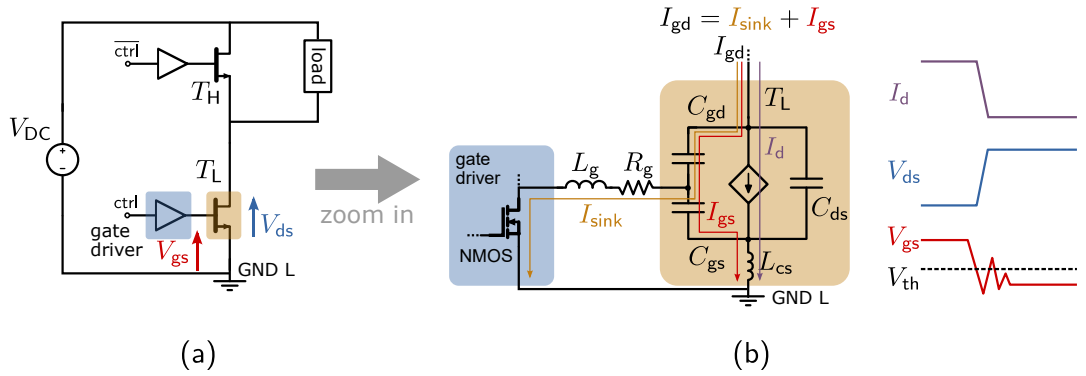


Figure 1.22: Measured turn-on and turn-off switching waveforms of a GaN-HEMT from a double-pulse test with 400 V of DC voltage and 5 A of load current.



(a) (b)

Figure 1.23: The schematics of (a) half-bridge circuit and (b) principle of GaN-HEMTs' false turn-on phenomenon.

critical for switching commutation. Because the V_{th} of GaN-HEMTs is already very low (typically 1.5 V) and the negative V_{th} shift may occur in this condition [43], the gate loop voltage oscillations can easily reach the V_{th} and turn on the device, leading to the so called false turn-on phenomenon.

For example, as shown in Fig. 1.23(a), the high-side (T_H) and low-side device (T_L) operate complementarily in the half-bridge circuit. During the turn-off transition of T_L, the $C_{oss} = C_{ds} + C_{gd}$ of T_L will get charged by the load current. Simultaneously, the C_{gd} is being discharged, forming the discharging current I_{gd}. More exactly, one part of I_{gd} is sunk by the on-state n-channel MOSFET (NMOS) in gate driver, which is noted as I_{sink}. The I_{sink} can induce voltage drop on L_g and R_g that can increase the voltage drop on C_{gs}. The other part of I_{gd} can further charge the C_{gs}, forming the I_{gs}, as shown in Fig. 1.23(b). Hence, both I_{sink} and I_{gs} tend to increase the V_{gs} during turn-off transient, whereas the induced voltage drop on L_{cs} can also rise the V_{gs}. These induced voltages could further resonate with C_{iss}, therefore forcing the V_{gs} oscillation to exceed the V_{th} after the turn-off transition, leading to the false turn-on phenomenon. Just after a small dead time, the T_H will be turned on and this can cause the cross conduction of the two transistors, leading to high power losses or even the device's short circuit failure. Symmetrically, the T_H transistor is also affected by this phenomenon.

More detrimentally, the V_{gs} oscillation can becomes gradually divergent in some conditions, where the V_{gs} oscillation can turn on and off the GaN-HEMTs with a very high frequency. This phenomenon is called "gate instability phenomenon" [42]. The gate instability issue is highly related to the parasitic parameters in the gate loop and the V_{th} shift of GaN-HEMTs. On top of induced additional losses it can cause the failure of the gate stack since the absolute maximum gate rating voltage is from -10 V to 7 V for the Schottky-type GaN-HEMTs [115].

1.4.3 Parasitic parameters considered in this work

The switching behaviour of GaN-HEMTs is very sensitive to the circuit parasitic parameters, therefore, special attentions should be drawn to avoid the oscillations caused by the gate loop parasitic inductance L_g and common-source inductance L_{cs}. Moreover, the C_{iss} of GaN-HEMTs is extremely small compared to that in Si-MOSFETs for devices with the same power level. Hence, the charging and discharging process of the C_{iss} could be extremely sensitive to the parasitic parameters in the whole gate loop, including the parasitic parameters inside the gate driver. The impact of L_g on the device switching transition is widely investigated in [112], [113], [114], while the influence of parasitic parameters inside the gate driver, for example the C_{oss} of NMOS in Fig. 1.23(b), is not commonly investigated in the literature. This matter might have been overlooked for Si- or SiC-MOSFETs because their C_{iss} is on nano-farads (nF) scale, the value is much higher than the C_{oss} of MOSFETs in the gate driver. However, this C_{oss} may becomes important, when the gate driver is used to drive the power GaN-HEMTs with several hundred pico-farad level of C_{iss}. Its impact on the switching behaviour of GaN-HEMTs will be discussed in detail in Chapter 4.

1.5 Summary of findings

The basic operating principle and fast switching characteristics of power GaN-HEMTs have been illustrated. Subsequently, the application challenges of GaN-HEMTs in terms of dynamic R_{on}, V_{th} shift, and sensitivity to parasitic parameters are reviewed, covering the underlying physical mechanisms and their impact on power converters. Consequently, several questions arise that warrant research attention:

- An in-situ and half-bridge compatible V_{th} measurement method is required to characterise the off-state (I-type) V_{ds} bias induced V_{th} in both single pulse and continuous mode. It should be noted that the impact of II-type V_{ds} bias (hard-switching) is excluded in this method to obtain the pure relation between off-state V_{ds} bias and V_{th} shift. The influence of II-type V_{ds} bias on the V_{th} shift will be partly discussed in Chapter 3. The objective of this measurement method is to reveal the actual V_{th} when device operating similar as in power converter regime (soft-switching operation). Moreover, the structure and operation principle of GITs indicate different V_{th} shift mechanisms. The measurement method and characterisation result will be discussed in Chapter 2.

- The V_{th} shift may influence the device switching behaviour by shifting the transfer characteristics, this phenomenon is crucial for GaN-HEMTs as the device mainly operates in high-frequency. This hypothesis will be addressed in Chapter 3.

- The ultra-fast commutation speed of GaN-HEMTs makes its switching behaviour sensitive to the circuit parasitic parameters. In the gate loop, these parasitic parameters could influence the charging and discharging process of the C_{iss} of

GaN-HEMTs. Due to the significantly reduced C_{iss} value of GaN-HEMTs compared to their Si-MOSFET counterparts, the gate driver's output capacitance may influence the charging and discharging process of GaN-HEMTs, leading to the various switching behaviours. This issue requires detailed investigation and will be explored in Chapter 4.

Chapter 2

Characterisation of off-state V_{ds} bias induced V_{th} shift

Outline of the current chapter

The V_{th} shift of GaN-HEMTs is coupled with several parameters such as V_{gs} bias, different types of V_{ds} bias, and temperature. It is essential to decouple these parameters to investigate the impact of a single parameter on the V_{th} shift. The off-state (I-type) V_{ds} bias is a typical state of GaN-HEMTs when they operate in power converters, this V_{ds} bias induced V_{th} shift could influence the following operation of the transistors. Therefore, it is essential to investigate the off-state V_{ds} bias induced V_{th} shift, which can provide valuable information for the V_{th} estimation of GaN-HEMTs. This chapter aims to investigate the off-state V_{ds} bias on the V_{th} shift for both Schottky-type GaN-HEMTs and GITs, as different V_{th} shift related mechanisms could occur under the off-state voltage stress for these two type of devices. The characterisation of the off-state V_{ds} bias induced V_{th} shift is achieved by proposing an in-situ V_{th} measurement method. This method enables the measurement of the relationship between V_{ds} bias duration (and strength) and the resulting V_{th} shift, as well as the V_{th} recovery behaviour of the shifted V_{th}. Additionally, this method allows for measuring the dynamic behaviour of V_{th} for GaN-HEMTs when they are continuously operating in soft-switching conditions. This chapter will begin by introducing the measurement principles of the proposed method, followed by the presentation of V_{th} shift measurement results from both single and continuous mode tests for both Schottky-type GaN-HEMTs and GITs. Finally, the chapter will conclude with a discussion of the findings and the limitations of this measurement method, highlighting areas for future work.

2.1 Half-bridge based V_{th} shift measurement method

The customised circuit-based measurement methods for the V_{ds} bias induced V_{th} shift are reported in [98], [99], [101], [103]. These methods either require specific circuits that are not compatible with the standard half-bridge configuration, cannot exclude the influence of hard-switching, or do not support continuous test modes, as discussed in section 1.3.3.5. To address these issues, a V_{th} shift measurement method utilise a standard half-bridge, designed for straightforward implementation and to facilitate an in-situ measurement. The underlying principles of this method, along with the experiment setup, will be detailed below.

2.1.1 Third quadrant characteristics of GaN-HEMTs

The V_{th} measurement principle in this method utilises the third quadrant characteristics of GaN-HEMTs. Due to their "quasi-symmetrical" structure, as illustrated in Fig. 1.4, GaN-HEMTs can be turned on by applying a positive voltage to either gate-to-source or gate-to-drain nodes (inter-electrode capacitances C_{gs} or C_{gd}). This unique feature

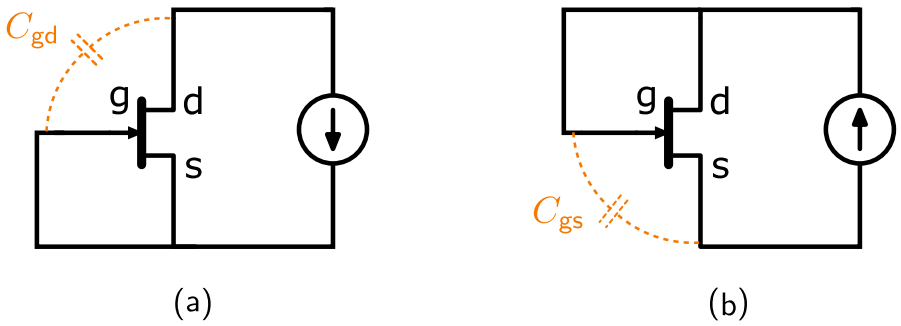


Figure 2.1: The conducting mechanisms of the GaN-HEMTs in (a) reverse and (b) forward.

enables effective V_{th} measurement within the proposed method. Fig. 2.1(a) illustrates how the third quadrant characteristics are utilised in the V_{th} measurement. When the gate-to-source nodes of a GaN-HEMT are shorted, a current source can be used to charge the device's C_{gd}. As the C_{gd} charges to V_{th}, the 2DEG channel of the GaN-HEMTs is formed and the device can conduct in reverse, allowing for the measurement of V_{th} under specific conditions. It should be noted that the third quadrant conduction mechanism of GaN-HEMTs differs from that of MOSFETs. In MOSFETs, current flows through the body diode in reverse conduction, whereas in GaN-HEMTs, the current flows through the main channel. The third quadrant characteristics of GaN-HEMTs is also utilised as a freewheeling diode in power converters. As a comparison, Fig. 2.1(b) shows the forward conducting characteristics of GaN-HEMTs, where the device conducts once the C_{gs} is charged to V_{th} as the MOSFETs.

If the V_{th} of C_{gs} (V_{th}^{gs}) and C_{gd} (V_{th}^{gd}) are identical, the measured V_{th}^{gd} can represent the V_{th} of GaN-HEMTs and the V_{th} shift phenomenon can be measured using V_{th}^{gd}. However, they might be not always identical due to the non-strictly symmetrical structure as shown in Fig. 1.4, where the length of gate-to-source access region is shorter than that in gate-to-drain region. Therefore, it is necessary to verify the symmetry of V_{th} for GaN-HEMTs. Two commercialised Schottky-type GaN-HEMTs (GS-065-030-2-L, 650 V/30 A) and GIT (IGOT60R070D1, 600 V/31 A) are used as the DUTs in this investigation. Their reverse conducting characteristics ($I_d - V_{gd}$) and transfer characteristics ($I_d - V_{gs}$) are measured by the semiconductor curve tracer B1505A from Keysight, as shown in Fig. 2.2, where the reverse conducting characteristics (dashed line) and the transfer characteristics (solid line) of these two devices show high similarity.

Therefore, the measured V_{th}^{gd} can be considered equivalent to V_{th}^{gs} when investigating the V_{th} shift phenomenon. This principle is adopted as well in [91], [99] to study the V_{th} shift of GaN-HEMTs.

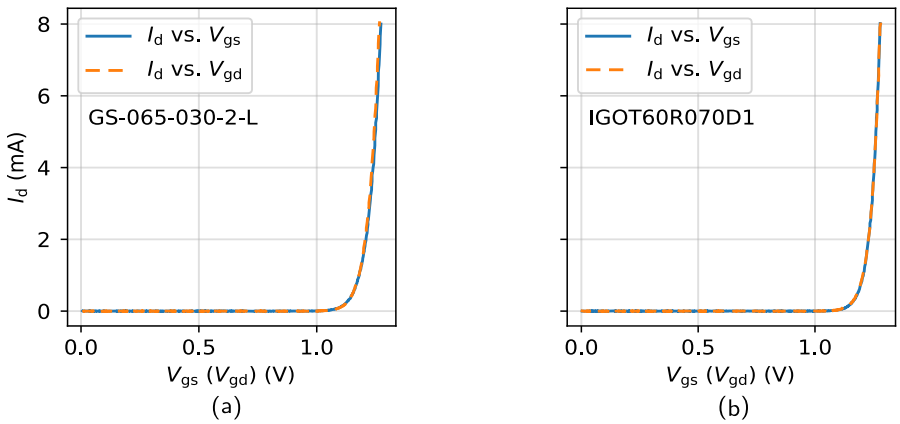


Figure 2.2: The reverse conducting characteristics ($I_d - V_{gd}$) and transfer characteristics ($I_d - V_{gs}$) of (a) the Schottky-type GaN-HEMTs (GS-065-030-2-L) and (b) GITs (IGOT60R070D1).

2.1.2 Measurement schematic and principle

A standard half-bridge configuration with an RL load is adopted to characterise the off-state V_{ds} bias induced V_{th} shift. The schematic and measurement principle are shown in Fig. 2.3, where the V_{DC} and C represent the power supply and DC capacitor of the half-bridge, respectively. The symbols T_H and T_L denote the high-side and low-side transistors, with their control signals labeled as V_g^H and V_g^L. Basically, there are three stages in this measurement:

(1) Initially, the T_H is in off-state and the source-to-gate terminals of T_L (DUT) are shorted to ensure the off-state as well. Since the DUT is in parallel with the RL load, the V_{DC} bias is undertook by the T_H and the V_{ds} bias of DUT can be considered as zero.

(2) When the T_H is turned to on-state, from t_0 to t_1, the high V_{DC} bias is subjected to the drain side of DUT, as shown in Fig. 2.3(a). In this condition, the off-state V_{ds} bias is applied to the DUT and the bias amplitude and time duration can be respectively adjusted by the V_{DC} voltage and the on-state time of T_H, and this period is defined as V_{ds} bias stage. In the meantime, the RL load will be charged and the charging speed and saturated current is depended on the resistance and inductance of the load. The key signals in this stage are depicted in Fig. 2.3(c).

(3) When the T_H is turned to off-state, from t_1 to t_2, the V_{ds} bias in the DUT will be removed. Afterward, the current in the RL load will charge the C_{gd} of the DUT and flow through the DUT based on the third quadrant characteristics, while the V_{gd} (equal to V_{sd}) of the DUT will be clamped to the V_{th} at its corresponding channel's current (I_{ch}). Once the DUT is in reverse conduction, the measured load current I_L equals to the I_{ch} of the device, and the corresponding V_{th} can

be obtained by measuring V_{sd}, which is defined as V_{th} measurement stage and shown in Fig. 2.3(c). In this stage, the V_{th} of DUT after the off-state V_{ds} bias can be measured. Furthermore, the V_{ds} bias and V_{th} measurement stage can be repeated to evaluate the variation of V_{th} when the device is operating in continuous mode.

2.1.2.1 Voltage clamping circuit

To implement this V_{th} shift characterisation method, the V_{ds} and I_L should be measured. However, the V_{ds} varies from several hundred volts during the V_{ds} bias stage to less than 2 V (reverse on-state V_{ds}) during the V_{th} measurement stage. Therefore, it is impossible to acquire an accurate reverse on-state V_{ds} using several hundred volts range in a digital oscilloscope with an 8-bit or even 12-bit analog to digital converter (ADC). A clamping circuit is essential to fix the off-state V_{ds} to a low value during the bias stage, so that the reverse on-state V_{ds} can be measured accurately using a small voltage range. Same challenge has been reported when the dynamic R_{on} of GaN-HEMTs is characterised, several clamping circuits being reported in [72], [75], [77], [78], [116]. The clamping circuit proposed in [72] is adopted in this work to characterise the V_{ds} biased induced V_{th} shift, and it is composed of a Schottky diode, a Zener diode and a normally-on Si-MOSFET. The reasons for adopting this clamping circuit are:

- This clamping circuit is able to measure the reverse on-state voltage V_{sd}, which can be assumed as the V_{th} when device operates in the third quadrant.
- Only three components are required to achieve this clamping circuit and it does not require an extra power supply to operate, showing a good half-bridge compatibility.
- The measurement response time from off-state bias to on-state measurement stage is short, which contributes to the characterisation of the V_{th} shift in high frequency continuous mode.

The schematic of the half-bridge with the clamping circuit is shown in Fig. 2.4, where the voltage drop on the Zener diode (Z_1) and Schottky diode (S_1) is the clamped V_{ds} voltage (V_{dsm}). The working principle of the clamping circuit is illustrated bellow:

- When the DUT is subjected to a high off-state V_{ds} bias, the junction capacitance of Z_1 will get charged through the on-state M_1. Once the V_{dsm} (equal to $V_{s'g'}$) exceeds the $-V_{th}$ of M_1, the M_1 will be turned off and the C_{oss} of M_1 will undertake the high V_{DC}, so the V_{dsm} will be clamped at $-V_{th}$ of M_1.
- During the reverse turn-on transient of the DUT, the C_{oss} of DUT and M_1 and the junction capacitance of Z_1 will discharge, leading to the decreasing of V_{dsm}. Once the $V_{s'g'}$ of M_1 is lower than its $-V_{th}$, and the M_1 will be turned to on again. Simultaneously, the I_L will charge the junction capacitance of S_1 and the C_{gd} of DUT, until S_1 is in reverse bias and DUT is in reverse on-state.

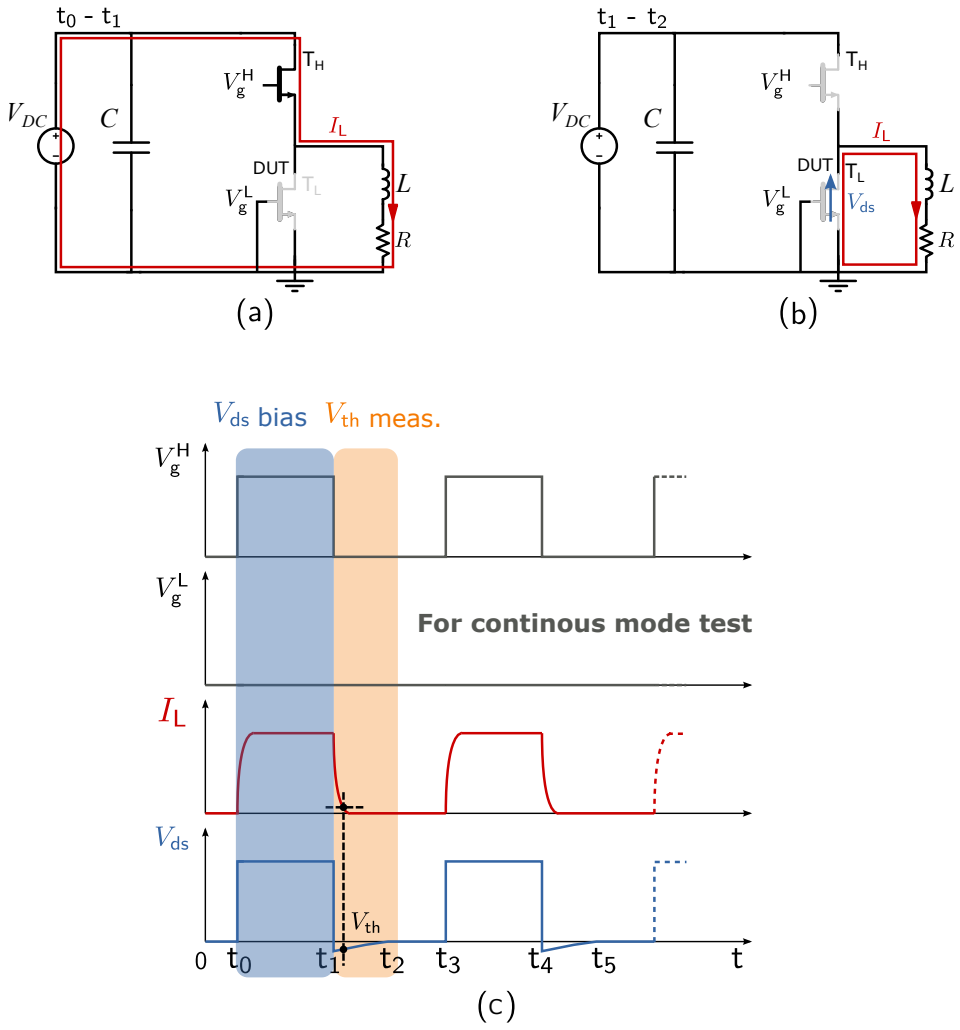


Figure 2.3: The schematic of the half-bridge based in-situ V_{th} measurement method in (a) V_{ds} bias stage and (b) V_{th} measurement stage. (c) The control sequence of the essential parameters in the measurement and the interpolation method for extracting V_{th}.

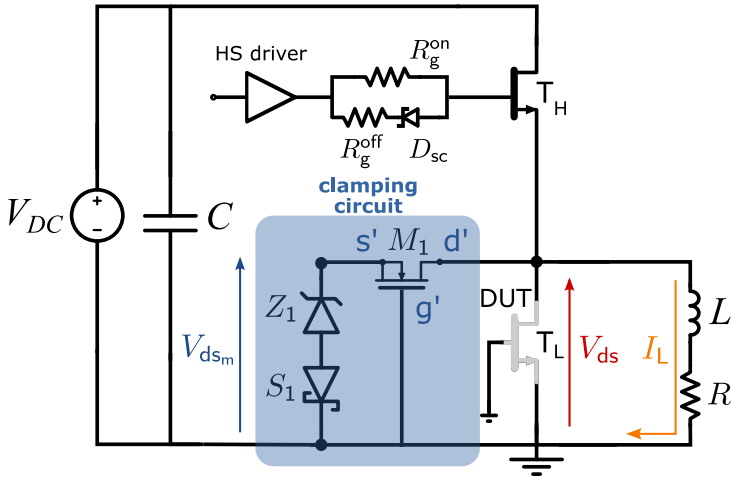


Figure 2.4: The schematic of the half-bridge with RL load and the clamping circuit for in-situ V_{th} shift measurement.

- When the DUT is in reverse on-state, the I_L is equal to I_{ch}. Moreover, the S_1 is in reverse bias and V_{dsm} is equal to V_{ds} as the leakage current flowing through M_1 is very small because of these two diodes, making the voltage drop on M_1 negligible. Therefore, the reverse on-state V_{ds} can be measured properly using this clamping circuit.

The selection of these three components are critical to the performance of the clamping circuit. There are few conditions to achieve to ensure a correct functioning for the clamping voltage:

- For M_1, the V_{th} should be relatively small to ensure a small voltage swing of V_{dsm}. And the rated breakdown voltage should be in the same level of DUT. For Z_1, the Zener voltage should be higher than the $-V_{th}$ of M_1 to ensure the M_1 can be turned off. For S_1, the breakdown voltage cannot be lower than the reverse V_{ds} of DUT and the leakage current should be small to ensure nearly all of the current is flow through the DUT.

- To achieve a good dynamic performance of the clamping circuit, the C_{oss} of all these three components should be as small as possible, especially for M_1 since it will be discharged with the DUT from several hundred volts to 0 during the turn-off transition of T_H. Small C_{oss} of M_1 contributes to achieve a fast V_{dsm} measurement response time.

Based on the above requirements, in this study, the BSP135H6433XTMA1 (600 V) is adopted as M_1 and the BZG05C3V3 (3.3 V) and SD0603S040S0R2 (40 V) are respectively adopted as the Z_1 and S_1.

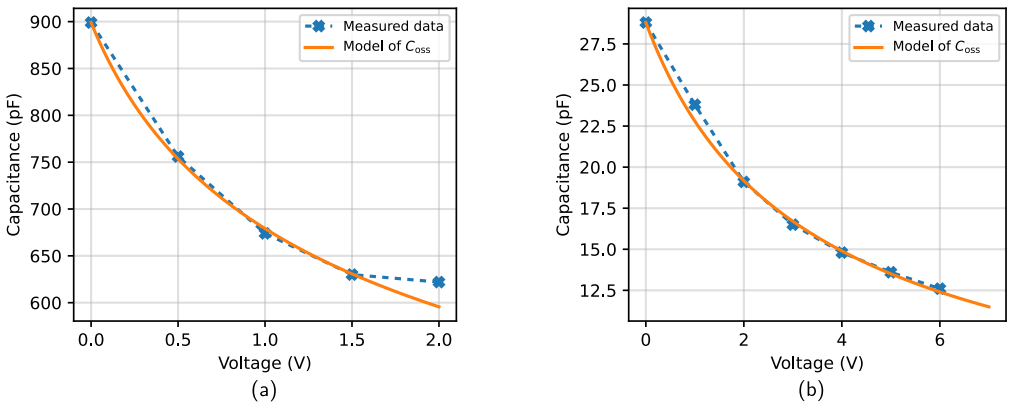


Figure 2.5: The measured and modelled non-linear C_{oss} of (a) Zener diode (BZG05C3V3) and (b) Schottky diode (SD0603S040S0R2).

$V_{DC} = 200\,\text{V}$	$R_g^{on} = 10\,\Omega$	$R_g^{off} = 3.3\,\Omega$	$L = 78\,\mu\text{H}$	$R = 220\,\Omega$

Table 2.1: Simulation parameters in Fig. 2.4.

2.1.2.2 Simulation analysis of the measurement principle

A simulation is implemented in SPICE (Simulation Program with Integrated Circuit Emphasis) environment to verify the measurement principle and the performance of clamping circuit, where the schematic is the same as presented in Fig. 2.4. The SPICE model of GS-065-030-2-L provided by the manufacturer is adopted as the T_H and DUT. For the clamping circuit, the manufacturer model of BSP135H6433XTMA1 is adopted as the M_1. Additionally, the output charge Q_{oss} of DUT and M_1 are compared by the DC sweeping simulation from 0 to 200 V. The Q_{oss} of M_1 and DUT are found to be 2.3 nC and 48.8 nC, respectively, indicating that M_1 has a minimal influence on the commutation of the DUT, which is in line with the component selection requirements as discussed above. The customised diode models for Z_1 and S_1 are constructed, with the modeled non-linear C_{oss} of BZG05C3V3 and SD0603S040S0R2 based on the measurement results from the impedance analyzer, as shown in Fig. 2.5. Other key parameters for this simulation are listed in Table 2.1.

The simulation waveforms of the DUT and clamping voltage V_{dsm} are shown in Fig. 2.6. When the off-state V_{ds} bias is applied to the DUT, the V_{dsm} is clamped to $-V_{th}$ of M_1 (approximately 1.6 V). During the reverse turn-on process of DUT, the V_{dsm} decreases toward to a negative value, simultaneously, the C_{oss} of DUT is discharging as shown in the discharging current I_{coss}. This commutation time determines the measurement response time of V_{th} in this method. Once the commutation is completed and the DUT is in reverse on-state conduction, the device channel current I_{ch} will be equal to I_L, therefore, I_{ch} can be replaced by the measured I_L. In this condition, the corresponding reverse voltage drop on the DUT V_{sd} represents the V_{th} of the DUT. For

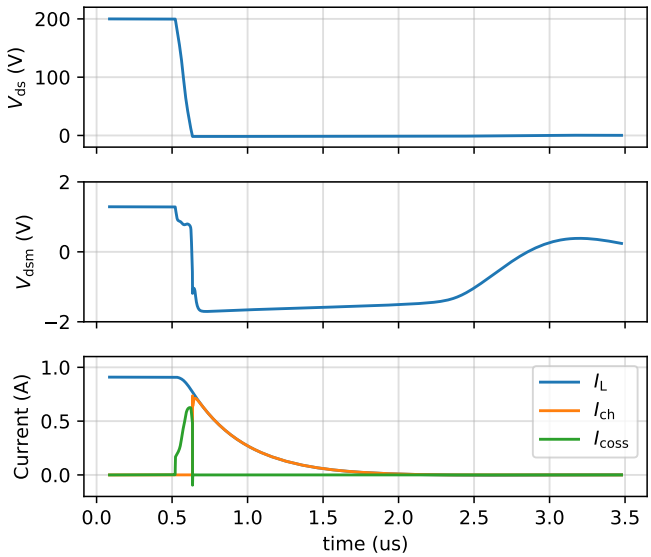


Figure 2.6: Simulation result of the half-bridge and RL load based V_{th} measurement with the schematic and simulation parameters respectively shown in Fig. 2.4 and Table. 2.1.

example, when the I_L drops to 10 mA, the corresponding $|V_{dsm}|$ is 1.52 V, and this value is the same as V_{th} of the DUT model obtained by the DC sweeping simulation.

The selection of the RL load is significant in this method because a big time constant can increase the V_{th} measurement response time. For example, it can take a long time for I_L to decrease to a mA level when use a large RL load. A too big power resistor is also not a good choice, as a small I_L can increase the commutation time of the DUT, thereby increasing the measurement response time of V_{th} as well. Additionally, the power rating of the resistor should be considered as the high V_{ds} bias can be applied to it for several hundred seconds in the single pulse test.

2.1.3 Experiment setup

A standard half-bridge configuration with the clamping circuit is presented in Fig. 2.7, where the important corresponding components in Fig. 2.4 are marked. The T_H and T_L are controlled complementarily by one pulse-width modulation (PWM) signal, as in a general half-bridge. For the V_{th} shift characterisation, the gate control loop of T_L (DUT) is disconnected, and the gate-to-source connectors of T_L are shorted. This ensures that the DUT is not controlled by the PWM signal and the DUT is always in off-state, so that the measured V_{sd} equals to the V_{gd} of DUT. These minor modifications to a standard half-bridge show the ease of implementation of this in-situ V_{th} shift characterisation method, which is one of the main advantages compared to the methods reported in the literature. Additionally, another similar half-bridge with the IGOT60R070D1 as the T_H and T_L is employed to investigate the V_{th} shift phenomenon of GITs devices. The

schematic and function of these two boards are the same, and the only difference is the design of driving circuitry because the GITs are current-driven devices.

The V_{ds} is measured by a 1 MHz passive probe. A 800 MHz galvanically isolated probe with a ±5 V range tip is adopted to accurately measure the V_{dsm}. Note that a sufficient preheating is performed before the measurement, aiming to avoid the influence of temperature drifting of the probe. A 120 MHz Hall-effect current probe with 1 mA measurement resolution is used to measure the I_L. It should be noted that the I_d measured by the current shunt (presented in Fig. 2.7(a)) is not adopted because the shunt resistor could bring common-mode noise from the ground of oscilloscope, influencing the current measurement accuracy especially under a low value of current.

2.2 Single pulse mode test

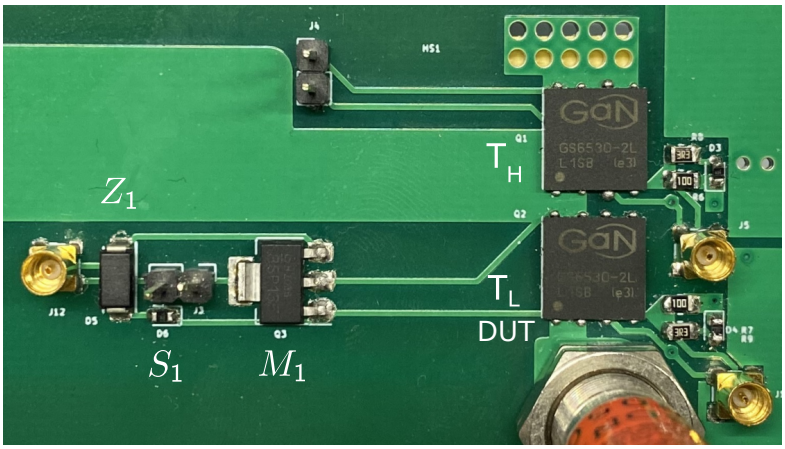
The measured V_{th} shift after the single pulse V_{ds} bias are discussed in this section. The objective is to investigate the relation between off-state V_{ds} bias (strength and duration) and the shifted V_{th} for both Schottky-type GaN-HEMTs and GITs. Furthermore, the recovery behaviour of the shifted V_{th} will be evaluated for these two types of devices.

2.2.1 Off-state V_{ds} bias induced V_{th} shift

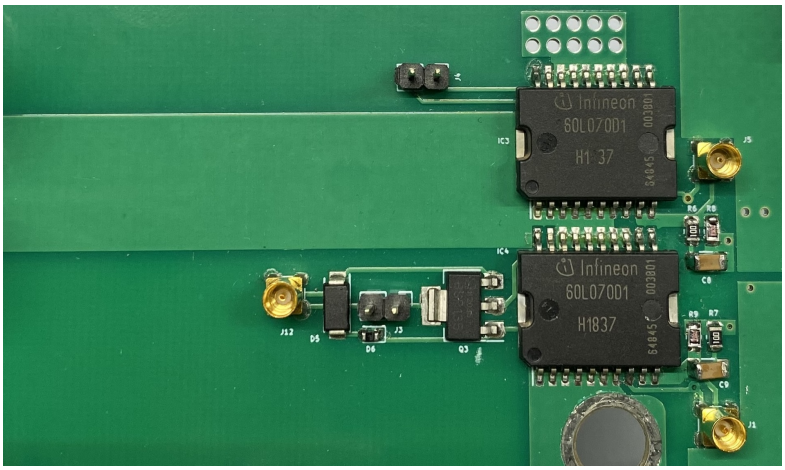
The off-state V_{ds} bias induced V_{th} shift will be evaluated in this subsection in terms of V_{ds} bias time and voltage. Moreover, the measurement uncertainty of the proposed measurement setup will be discussed to ensure a convening test result.

2.2.1.1 Measured switching waveforms and positive V_{th} shift

In the single pulse test, the same RL load used in the previous simulation is applied, with $R = 220\,\Omega$ and $L = 78\,\mu H$. The measured switching waveforms for GS-065-030-2-L under 200 V of V_{ds} bias are shown in Fig. 2.8(a), which is similar to the simulation results in Fig. 2.6. The measured V_{dsm}, when the DUT is in reverse conduction, becomes more and more negative with the increasing of off-state Vds bias duration, while the measured I_L remains unchanged. This phenomenon indicates that the increased off-state V_{ds} bias time (under 200 V) can result in a positive V_{th} shift. To show this relation clearly, the measured $|V_{dsm}|$ and I_L in the grey region of Fig. 2.8(a) are plotted to respectively represent the V_{gd} and I_{ch}. This V_{gd} and I_{ch} characteristics are similar to the device "transfer characteristics", which are depicted in Fig. 2.8(b), where a notable positive shift can be observed with the increasing of bias duration. Note that the probe de-skew between the current and voltage probe is addressed based on the propagation time indicated in the datasheet, though it is not a significant parameter influencing the measurement result.



(a)



(b)

Figure 2.7: The experiment boards of the standard half-bridge and the clamping circuit with (a) GS-065-030-2-L (Schottky-type GaN-HEMTs) (b) IGOT60R070D1 (GITs) as the T_H and T_L.

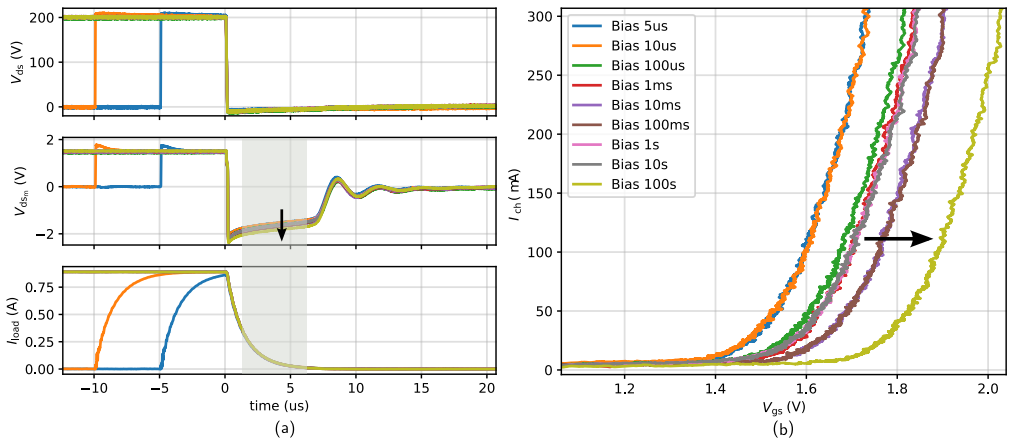


Figure 2.8: Measurement results for GS-065-030-2-L (a) switching waveforms under the 200 V of V_{ds} bias for different bias time. (b) $I_{ch} - V_{gd}$ characteristics (transfer characteristics) from the measurement results of V_{dsm} and I_{load} between 1 µs to 6 µs (grey region).

2.2.1.2 Measurement uncertainty evaluation

The above measurement shows the off-state V_{ds} bias induced positive V_{th} shift. However, the measurement uncertainty of this method should be evaluated to accurately quantify the shifted V_{th}.

At first, a SiC power diode (C4D40120D) is used as a DUT to replace the low-side GaN-HEMT in the half-bridge and the same test for in Fig. 2.8 is repeated. The objective is to demonstrate that the positive V_{th} shift is due to the GaN-HEMTs itself instead of the measurement setup. The switching waveforms and the relation of anode-to-cathode voltage V_{ad} and I_{ch} are respectively shown in Fig. 2.9(a) and (b). The V_{th} (or knee voltage) of the SiC diode at $I_{ch} = 20\,\text{mA}$ remains nearly unchanged with only around 0.03 V measurement uncertainty, which may be attributed to the probe offset. The measurement uncertainty is also evaluated by applying different V_{ds} to the C4D40120D for 10 µs. The measured switching waveforms and corresponding $I_{ch} - V_{ac}$ characteristics are displayed in Fig. 2.10, where it shows around 0.06 V measurement uncertainty when the V_{ds} varies from 50 V to 400 V. Consequently, the measured V_{th} shift exceeding 0.06 V can be attributed to the devices themselves in this measurement configuration. The observed approximately 0.3 V of V_{th} shift of GaN-HEMT is significant compared to the measurement uncertainty.

To properly quantify the V_{th} shift phenomenon of GaN-HEMTs, the original V_{th} (without any external high voltage bias, such as V_{ds} and V_{gs}) of the device should be measured as a reference. However, the curve tracer B1505A used in this experiment is not able to measure the V_{th} when the I_{ch} is higher than 8 mA, due to the power limitation of the high voltage source measurement unit (HVSMU). Therefore, a simple steady-state V_{th} measurement circuit is designed to measure the original V_{th} at higher I_{ch}, as the schematic depicted in Fig. 2.11. In this circuit, an adjustable voltage source is placed in series with a 100 Ω resistor (significantly higher than the R_{on} of the DUTs) to function as

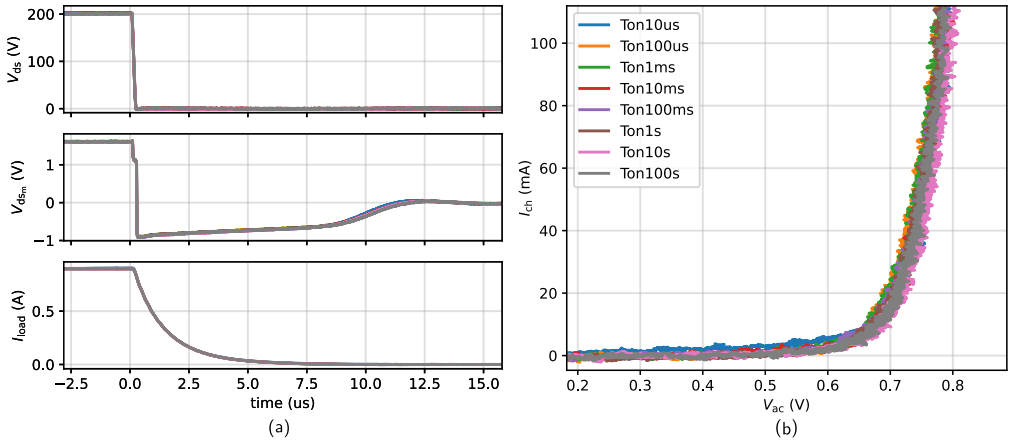


Figure 2.9: Measurement results for the SiC power diode C4D40120D (a) switching waveforms after the 200 V of V_{ds} bias for different bias time. (b) $I_{ch} - V_{ac}$ characteristics from the measurement results of V_{dsm} and I_{load} between 3 µs to 6 µs.

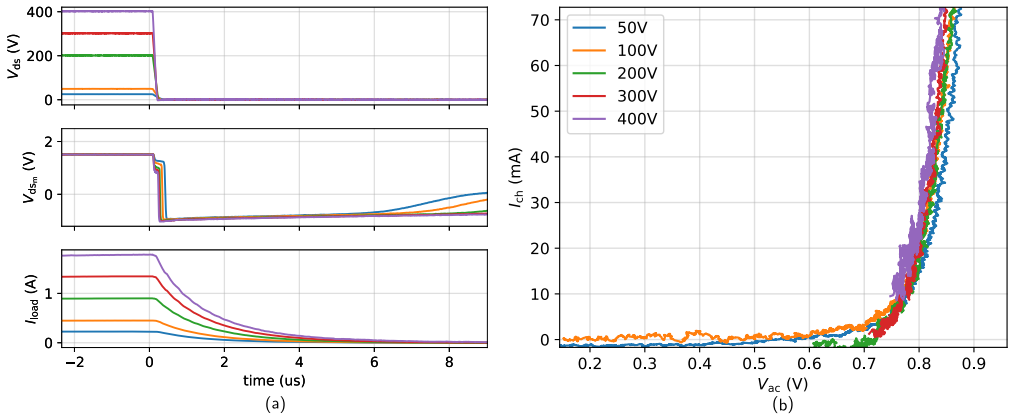


Figure 2.10: Measurement results for the SiC power diode C4D40120D (a) switching waveforms after the 10 µs of V_{ds} bias for different bias amplitudes. (b) $I_{ch} - V_{ac}$ characteristics from the measurement results of V_{dsm} and I_{load}.

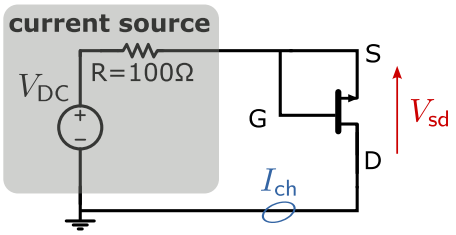


Figure 2.11: The schematic of the original V_{th} measurement circuit, where the V_{sd} can be assured as the V_{th} of GaN-HEMTs at corresponding I_d.

I_{ch}	V_{th} (GS-065-030-2-L)	V_{th} (IGOT60R070D1)
5 mA	1.30 V	1.25 V
20 mA	1.38 V	1.32 V
50 mA	1.53 V	1.35 V
80 mA	1.58 V	1.38 V
100 mA	1.59 V	1.39 V
140 mA	1.60 V	1.40 V

Table 2.2: Measured original V_{th} at different I_{ch} for Schottky-type GaN-HEMTs and GITs.

an adjustable current source for charging the C_{gd} of the DUTs. The C_{gs} is shorted while charging the C_{gd} to measure the V_{th}^{gd}. Once the C_{gd} is charged to the V_{th}^{gd}, the current will flow through the device channel and will be measured by the Hall effect current probe TCP0030A. The voltage drop across the DUT, V_{sd}, is then measured as the V_{th} at the corresponding channel current. By increasing the V_{DC}, the V_{th} at higher channel current can be measured.

The original V_{th} of GS-065-030-2-L and IGOT60R070D1 at different I_{ch} are displayed in Table 2.2. It should be noted that the original V_{th} measured by this steady-state method agrees with the measurement results from the curve tracer when $I_{ch} < 8$ mA, which supports the accuracy of this steady-state method. These two measured original V_{th} will be used as references for the following V_{th} shift evaluation for the Schottky- and Ohmic-type GaN-HEMTs, as the same device samples will be utilised.

To summarise, the measurement uncertainty of the proposed method is evaluated and the original V_{th} at different I_{ch} of the selected GaN-HEMTs are obtained. Based on these results, the relationship between the V_{ds} bias duration and the shifted V_{th} under different V_{ds} bias strength can be fully quantified. It is necessary to quantify the V_{ds} bias induced V_{th} shift phenomenon before applying the GaN-HEMTs to the power converters, as this phenomenon could influence the devices' performance as discussed in subsection 1.3.3.7.

2.2.1.3 V_{th} shift quantification

Schottky-type GaN-HEMTs

The V_{th} shift phenomenon of GS-065-030-2-L is firstly quantified. Taking the result from Fig. 2.8 as an example, at I_{ch} = 20 mA, the V_{th} increases from 1.43 V to 1.76 V with V_{ds} bias time increasing from 5 µs to 100 s. It results in a 0.33 V of positive V_{th} shift. To evaluate the influence of V_{ds} bias amplitude on the V_{th} shift, the measured V_{th} at I_{ch} = 20 mA under different V_{ds} bias are compared in Fig. 2.12(a), where the original V_{th} (1.38 V) baseline is chosen from the Table 2.2 when I_{ch} = 20 mA. After 5 µs or 10 µs of V_{ds} bias, the V_{th} does not show a clear shift, but it is generally slightly higher than the original V_{th}. This could be related to the hole-deficiency induced V_{th} shift that is not time-dependent [35], [85], as discussed in the mechanism (1) in section 1.3.3.4. Basically, the V_{th} shows a positive shift with an increasing of bias time under different V_{ds} biases, which agrees with the widely reported off-state V_{ds} bias induced V_{th} shift [35], [98], [99].

It should be noted that the positive V_{th} shift has a dropping stage when the bias time is close to 1 s, afterward, it still shows an increase behaviour. This V_{th} dropping is more pronounced when the V_{ds} bias exceeds 200 V. The reduction of the positive V_{th} shift under V_{ds} bias has not been reported in the studies listed in Table 1.5. This finding benefits from the "full map" of shifted V_{th} under different V_{ds} bias durations and amplitudes as in Fig. 2.12(a). Similar "full map" is created in [35] but the V_{th} dropping phenomenon is presented, which could be attributed to the curve tracer based measurement method, where the measurement response time between the high voltage bias and V_{th} is much longer than this proposed method, and a positive V_{gs} bias is introduced to measure the V_{th}. These conditions may obscure the V_{th} reduction phenomenon, further emphasising the importance of the in-situ V_{th} shift measurement method. To physics, the V_{th} reduction could be linked to the ionisation of donor-like traps (hole trapping) in the AlGaN/GaN interface or the GaN buffer layer [60], [65], [86]. It should be noted that the hole-trapping effect is not reported in the studies listed in Table 1.5, which may because the V_{th} reduction phenomenon was not observed in those studies. This measurement results support that the measured V_{th} is the competition result of the electron and hole trappings in the GaN-HEMTs.

Moreover, the measured ΔV_{th} from 5 µs to 100 s is not increasing with the rising of V_{ds} bias voltage, as shown in Fig. 2.12(b). Similar non-monotonic behaviour is reported in [76], [117], [118], [119] for the dynamic R_{on} of Schottky-type GaN-HEMTs after a long time of off-state V_{ds} bias, and in [120] for the V_{th} shift of 100 V rated Schottky-type GaN-HEMTs. These non-monotonic behaviours of dynamic R_{on} is explained by the high V_{ds} bias induced impact ionisation mechanism, where the hole-electron pair can be generated [82], [83]. After the impact ionisation, the generated electrons are drifted to the drain side under the high electric filed, and the left holes are injected to AlGaN or GaN buffer layers to mitigate the electron trapping effect [119], [120]. However, the impact ionisation primarily occurs when the device is under critical off-state voltage or high-voltage hard-switching stress, which cannot explain the ΔV_{th} dropping under 200 V or 300 V of V_{ds} bias for the 650 V rated Schottky-type GaN-HEMTs. This is the reason

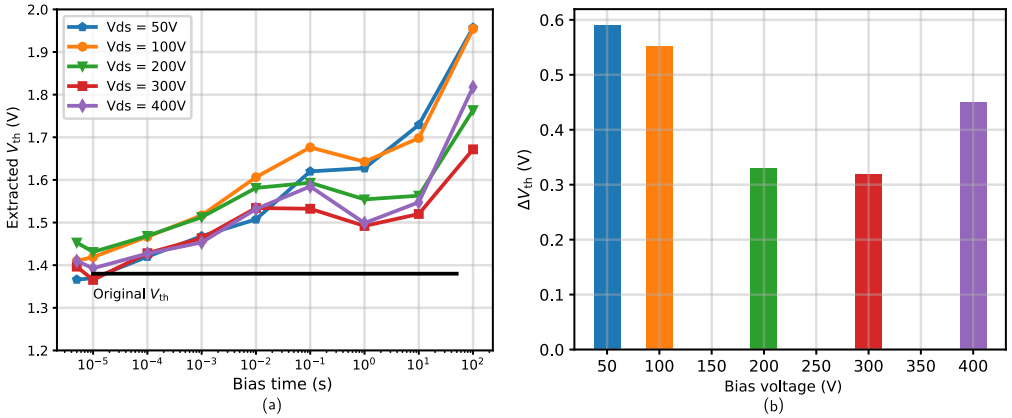


Figure 2.12: Measured V_{th} for GS-065-030-2-L (a) at I_{ch} = 20 mA after different off-state V_{ds} bias amplitudes and time (the original V_{th} is measured by the steady-state method as shown in Table 2.2) (b) measured ΔV_{th} from 100 s to 5 µs after different V_{ds} bias amplitudes.

why the impact ionisation is not mentioned in section 1.3.3.4, also, the relationship between the impact ionisation and V_{th} shift is not widely reported.

Since the RL load values are kept the same in these experiments, the saturated load current is higher with the V_{ds} bias voltage increasing, which may influence the measured V_{th} shift and result in the non-monotonic behaviours. To ensure the V_{th} variations are mainly caused by the V_{ds} bias, the influence from different load current should be evaluated.

On the one hand, the measurement response time t_m varies at different saturated load currents. Higher load current requires a longer time dropping to specific I_{ch}, as shown in Fig. 2.13. In this figure, the DUT is subjected to the off-state V_{ds} bias, increasing from 50 V to 400 V, for 10 µs. The saturated I_{load} increases with the V_{ds} bias since the RL load remains unchanged. If the measured V_{th} at I_{ch} = 20 mA are compared, the Δt_m can reach up to around 4.5 µs from 50 V to 400 V, as depicted in Fig. 2.13(b). If the recovery time constant of shifted V_{th} is in microsecond range, the 4.5 µs of Δt_m may mitigate the positive V_{th} shift. For example, when comparing the V_{th} shift phenomenon under 50 V and 400 V, the shifted V_{th} under 400 V may be recovered a bit before comparing them at I_{ch} = 20 mA. An approximately 30 µs recovery time constant for the V_{ds} bias induced V_{th} shift is reported for a 2 µs of V_{ds} bias in [121]. However, the recovery time constant could become longer when the V_{ds} bias time is extended. For the same series of Schottky-type GaN-HEMTs from GaNsystems, millisecond and second-range time constants are reported after the 60 s above of V_{ds} bias in [98], [121], [122]. Consequently, the Δt_m should not significantly influence the measured V_{th} under different V_{ds} bias, especially when the V_{ds} bias time is extended. This perspective will be verified in Fig. 2.16 later.

On the other hand, the increased load current will result in higher channel current I_{ch} flowing through the DUT, as shown in Fig. 2.13(a), although the value is limited

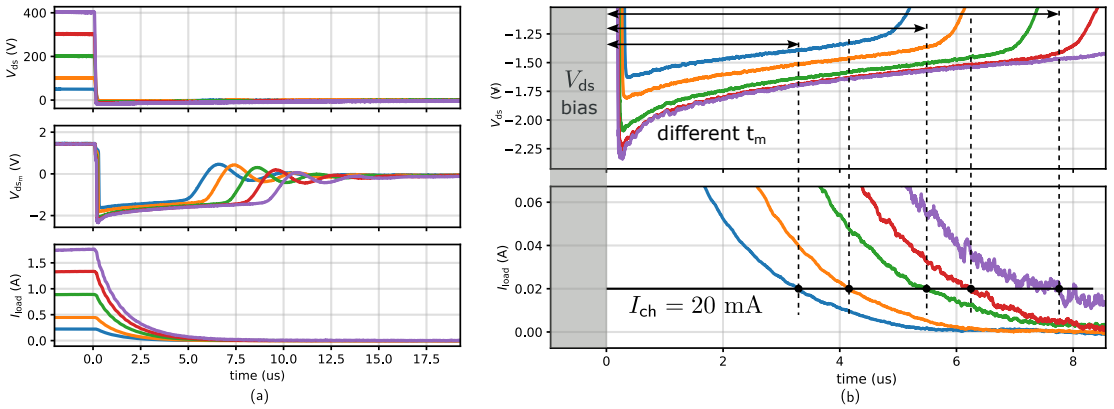


Figure 2.13: Measured switching waveforms after 10 µs of different V_{ds} bias (a) whole switching waveforms (b) zoomed in waveforms to show the variation of measurement response (V_{th} recovery) time under different V_{DC}.

less than 2 A in this measurement. However, the I_{ch} may not cause V_{th} shift, based on the V_{th} shift mechanisms and reported works [10], [84], [123]. To further verify the influence of I_{ch} on V_{th} shift, another RL load composed of a 1.5 Ω resistor and a 30 µH inductor is used to evaluate the V_{th} under a 5 V V_{ds} bias. The large time constant of this load allows for achieving different I_{ch} by adjusting the V_{ds} bias time, before the load current get saturated. This low value of V_{ds} bias is expected to cause no V_{th} shift. Hence, the influence of I_{ch} on the V_{th} shift can be evaluated. The switching waveform and the measured $I_{ch} - V_{gd}$ characteristics are shown in Fig. 2.14. The bias durations for these two tests are set to 10 µs and 30 µs, respectively. The longer bias time results in nearly twice the I_{ch}, but it does not cause a V_{th} shift. Therefore, the influence of different I_{ch} caused by different V_{ds} biases on V_{th} shift can be excluded.

The relationship between the bias amplitudes and durations of V_{ds} and shifted V_{th} is characterised for the Schottky-type GaN-HEMTs, where the influence of different t_m and load current on the measured V_{th} is discussed, validating relevance between the proposed method and results.

GITs

Same V_{ds} bias induced V_{th} shift characterisation process is adopted to evaluate the V_{th} shift phenomenon of the IGOT60R07D1 device, using the half-bridge as shown in Fig. 2.7(b). To exclude any influence from the measurement setup, a SiC power diode C4D40120D is firstly characterised using the GITs based half-bridge, and the results agree well with those in Fig. 2.9 and Fig. 2.10. The off-state V_{ds} bias induced V_{th} shift of IGOT60R07D1 are displayed in Fig. 2.15, where the positive V_{th} remains stable before the bias duration exceeding 100 ms. The V_{th} shows a noticeable drop when the bias duration is higher than this value. Afterward, the V_{th} stabilises with the increasing of bias duration, exhibiting a slight negative shift compared to its original value. Moreover,

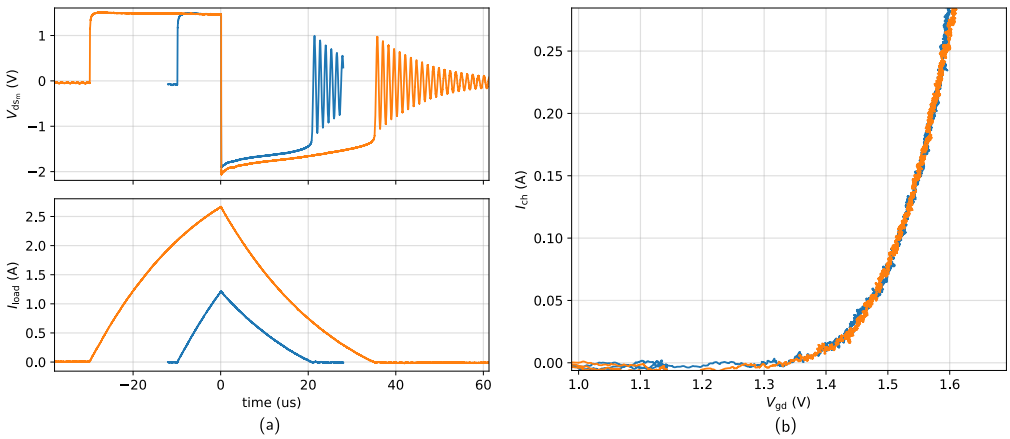


Figure 2.14: Measurement results for GS-065-030-2-L (a) switching waveforms under the 5 V of V_{ds} bias with a load of 1.5 Ω resistor and a 30 µH inductor. (b) $I_{ch} - V_{gd}$ characteristics from the measurement results of V_{dsm} and I_{load}.

the ΔV_{th} measured from 100 s to 5 µs are depicted in Fig. 2.15(b), which shows that the V_{th} shifts negatively with the V_{ds} bias amplitude increasing. Additionally, the shifted V_{th} does not present a strong relation with the V_{ds} bias amplitude, once V_{ds} exceeds 50 V.

To the best knowledge of the author, the V_{th} shift behaviour of GITs under the different amplitudes and durations of off-state V_{ds} bias is firstly reported in this work. It also results in a lack of references to evaluate the measured results, unfortunately. However, this result supports the hole-injection mechanism caused by the PD-structure of GITs [124], as discussed in Fig. 1.13. The hole-injection mechanism may be more easy to be triggered under high V_{ds} bias and the injected holes are attracted to the gate stack to release the trapped electrons in AlGaN/GaN interface or GaN buffer, especially when the bias time is extended. This can well explain the observed results in Fig. 2.15(a), where the V_{th} decreases with the increasing of bias duration and amplitude. Additionally, the less increased dynamic R_{on} under high V_{ds} bias for GITs are reported in [77], which supports the hole-injection induced de-trapping effect.

It should be noted that there is around 0.25 V of positive ΔV_{th}, comparing to the original V_{th} of IGOT60R07D1, when the V_{ds} bias time is shorter than 1 s. This is different with the GS-065-030-2-L device that the V_{th} increases from the original V_{th}. It may indicate that the electron trapping related positive V_{th} still exist in GITs, which has a less 5 µs of trapping time constant. And the V_{th} represents a notable negative V_{th} shift when the V_{ds} bias time is longer than 1 s, which indicates that the hole-injection mechanism might occur after a relative long bias time. It is interesting to be observe that the V_{th} is finally getting saturated at around the original V_{th}.

Except the distinct V_{th} shift direction of Schottky-type GaN-HEMTs and GITs devices, the measured $I_{ch} - V_{gd}$ characteristics under different V_{ds} bias time are quite different. The measured $I_{ch} - V_{gd}$ under 5 µs to 100 s of 400 V bias are compared in Fig. 2.16, where

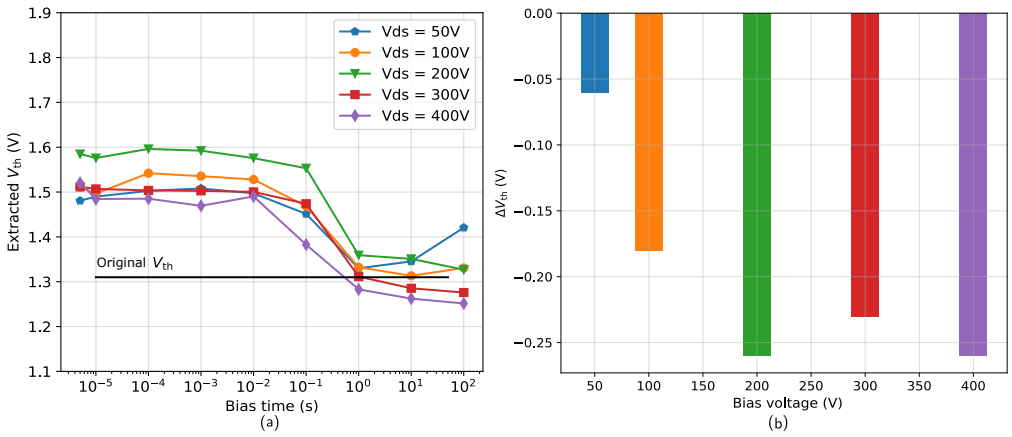


Figure 2.15: Measured V_{th} of IGOT60R07D1 (a) at I_{ch} = 20 mA after different off-state V_{ds} bias amplitudes and time (the original V_{th} is measured by the steady-state method as shown in Table 2.2). (b) measured ΔV_{th} from 100 s to 5 µs after different V_{ds} bias amplitudes.

the slope of Schottky-type GaN-HEMTs remains constant (each $I_{ch} - V_{gd}$ curve are in parallel), while the GIT shows a increased slope with the increasing of bias duration. If considering the $I_{ch} - V_{gd}$ characteristics of GIT as its transfer characteristics, the increased slope can be attributed to the increased g_m. The decreased g_m of GaN-HEMTs induced by the electron trapping under gate stack or access region are reported in [68], [69], [70]. Therefore, the decreased V_{th} and increased maximum transconductance g_m could be attributed to the hole-injection from the PD-structure of GIT as discussed in Fig. 1.9. This hole injection mechanism contributes to releasing trapped electrons in the access region or gate stack [77]. Moreover, the measured $I_{ch} - V_{gd}$ of GIT did not show a clear variation of g_m under less than 200 V, this phenomenon that may be due to the relative weak hole-injection under low V_{ds} bias.

To summarise, in the single pulse test, the Schottky-type GaN-HEMTs exhibit a positive V_{th} shift with the bias time increasing from 5 µs to 100 s, while the GIT show a negative V_{th} shift behaviour. Additionally, both positive and negative shifts in V_{th} (ΔV_{th}) do not exhibit a consistent increase with the rising of bias voltage amplitude. Two main novelty findings under the extended V_{ds} bias duration are observed. Note that another samples of GS-065-030-2-L and IGOT60R07D1 are tested in the same conditions, which shows similar V_{th} shift behaviours.

- The Schottky-type GaN-HEMTs present a V_{th} dropping stage when the V_{ds} bias time approaches 1 s, which becomes more prominent with increasing the V_{ds} bias amplitude.
- The g_m of Schottky-type GaN-HEMTs remain constant with increasing of the bias time under all V_{ds} bias amplitudes, while the g_m of GIT increased under long time of bias time once the V_{ds} bias voltage is higher than 200 V.

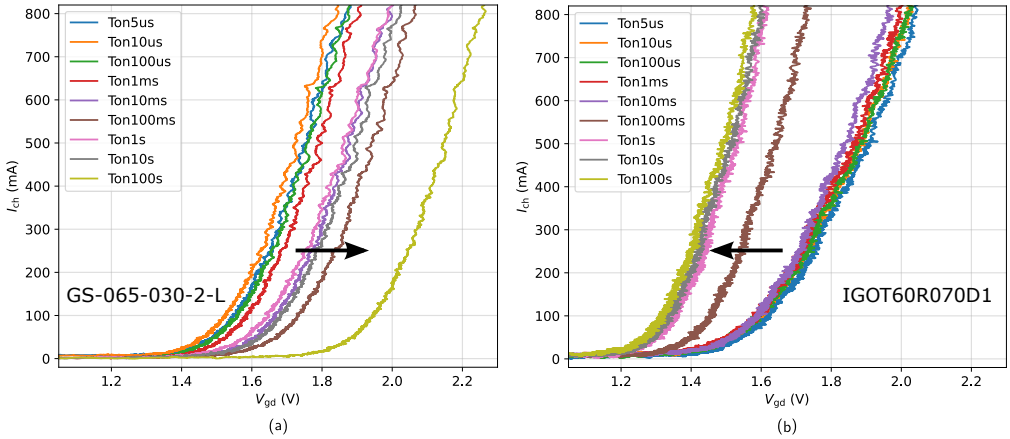


Figure 2.16: Measured $I_{ch} - V_{gd}$ characteristics under 400 V of V_{ds} bias with various of bias time for (a) Schottky-type GaN-HEMTs (b) GITs device.

Until now, the influence of V_{ds} bias (trapping) on the V_{th} shift has been studied. However, the shifted V_{th} is recoverable once the V_{ds} bias is removed (de-trapping), which plays a crucial role in the actual V_{th} when the device operates in power converters. Therefore, it is essential to investigate the recovery behaviour of the shifted V_{th} after the extended V_{ds} bias conditions.

2.2.2 Recovery behaviour of the shifted V_{th} for GaN-HEMTs

2.2.2.1 Proposed measurement method for V_{th} recovery

It is necessary to evaluate the recovery behaviour of the shifted V_{th} to further understand the V_{th} shift phenomenon. In the literature, the recovery behaviour of the shifted V_{th} can be measured by extending the time window of the V_{th} shift measurement [98], [99], [103], however, the long-time of recovery behaviour cannot be measured using this method due to the limitation of data length. In [35], a curve tracer is used to measure the V_{th} recovery behaviour by performing basic transfer characteristic measurements following a specified duration of V_{ds} bias, however, it is not suitable for the customised circuit based V_{th} shift characterisation method.

The recovery behaviour of the shifted V_{th} can be conveniently measured in this proposed method by just applying another low V_{ds} pulse after an extended time of the high V_{ds} bias. The schematic of the measurement sequence is shown in Fig. 2.17. The DUT is primarily biased under high V_{ds} for a specific time and then the shifted V_{th} is measured between t_1 and t_2, which is the same as previous single pulse test. After a predetermined interval, a low and brief V_{ds} bias is applied to the DUT to repeat the V_{th} measurement, as shown between t_3 and t_5. The purpose of this low and short V_{ds} pulse is to minimize the impact of V_{ds} bias induced V_{th} shift. Additionally, the short V_{ds} pulse can be repeated after a longer recovery time to obtain the further recovery behaviour. By comparing the two measured V_{th}, the recovered V_{th} can be obtained. But it should

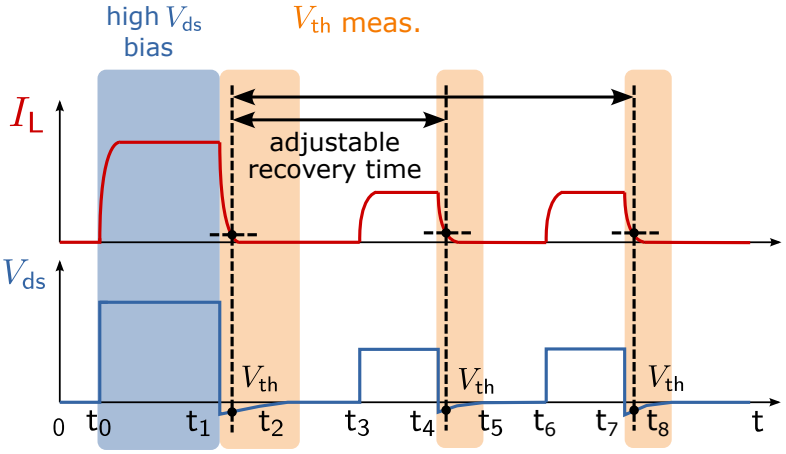


Figure 2.17: Schematic of the measurement sequence for V_{th} recovery phenomenon.

be noted that, due to the equipment limitation, the adjustable time between these two pulse is controlled manually, which can only ensure the minute-level accuracy. With the help of programmable DC power supply and function generator, the millisecond- or even microsecond-level of accuracy can be achieved. Hence, a minimum of 1 min recovery time is adopted in this work to evaluate the V_{th} recovery behaviour after 100 s of V_{ds} bias.

2.2.2.2 Recovery behaviour evaluation

The measured switching waveforms with a low V_{ds} pulse of 10 µs and 20 V (after 100 s of 100 V V_{ds} bias) are displayed in Fig.2.18(a) for the GS-065-030-2-L, where the recovery time increases from 1 min to approximately 30 hours. The recovery of the V_{th} can be observed from the V_{dsm} waveform. Moreover, the measured $I_{ch} - V_{gd}$ after different recovery time are depicted in Fig.2.18(b) to clearly show the recovery behaviour of the shifted V_{th}. The results show the recovery behaviour with time constants on the order of minutes to hours, where the relatively fast recovery occurs within approximately 1 h, while full recovery takes significantly longer.

To further characterise the recovery behaviour, similar tests are repeated under different V_{ds} bias amplitudes. The V_{th} at I_{ch} = 20 mA are extracted to quantify the recovery of the V_{th}. Moreover, the recovery of the V_{th} is compared to the shifted V_{th} to have a full map of V_{th} shift phenomenon for the GS-065-030-2-L, as plotted in Fig. 2.19. The left side shows the positive shifted V_{th} with increasing bias time, and the right side presents the measured V_{th} with an increase of the recovery time from 1 min to 24 h after the 100 s of high V_{ds} bias.

Generally, the shifted V_{th} recovers towards the original V_{th} together with the rising recovery time. However, the recovery behaviours are distinct when the amplitude of the previous V_{ds} bias is different. For the shifted V_{th} induced by 50 V or 100 V of V_{ds}, it will slowly recover to the original V_{th} somewhat logarithmically. In contrast, when the

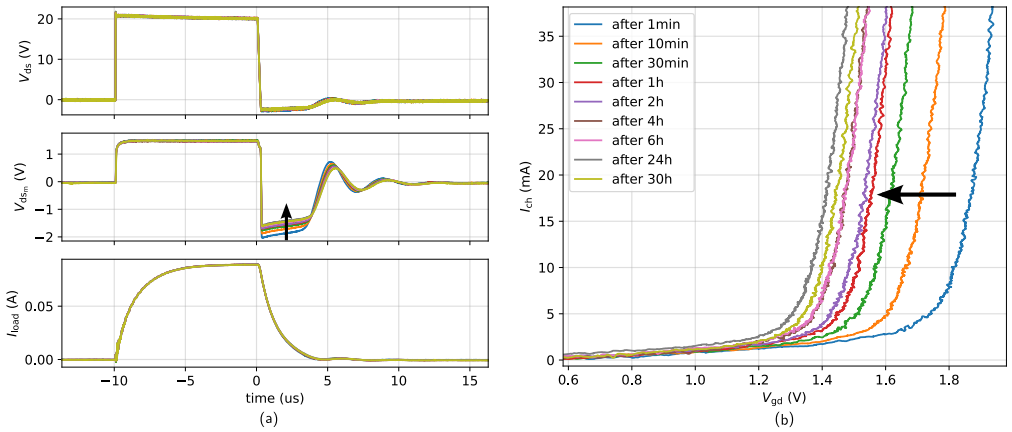


Figure 2.18: Measurement results of the V_{th} recovery behaviour for GS-065-030-2-L (a) switching waveforms under the 20 V of V_{ds} bias after the 100 s of 100 V single pulse and the recover time varies from 1 min to 30 h (b) $I_{ch} - V_{gd}$ characteristics from the measurement results of V_{dsm} and I_{load}.

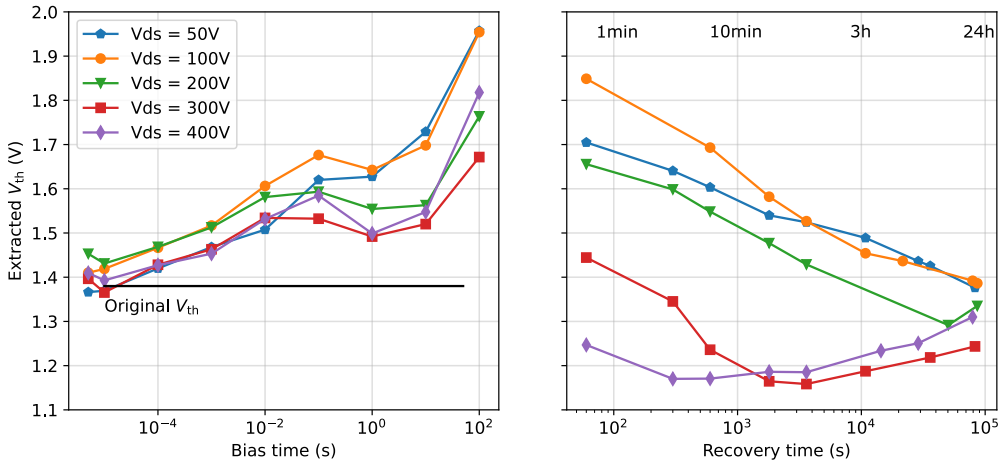


Figure 2.19: Measured V_{th} shift and recovery behaviour of GS-065-030-2-L at I_{ch} = 20 mA. The recovery behaviour is measured after the 100 s of high V_{ds} bias using the same method in Fig.2.18 and the recovery time varies from 1 min to 24 h.

previous V_{ds} bias is 300 V or higher, the shifted V_{th} will recover rapidly to a negative value (over-recovery) compared to the original V_{th}. After approximately 1 h, it shifts to the most negative value and then gradually recovers to the original V_{th}. To be noted that it can take around 72 h to fully recover to the original V_{th}, though it is not plotted in Fig. 2.19. The recovery of the 200 V V_{ds} bias induced V_{th} seems to be a transition state between the two cases, since both the logarithmic recovery behaviour and a small negative V_{th} shift are observed. It should be noted that the hour-level recovery time constant and the over-recovery effect after the prolonged and high V_{ds} bias for the Schottky-type GaN-HEMTs are the new findings compared to the literature.

This rapid and negative V_{th} recovery following the 300 V V_{ds} bias suggests the emergence of a new mechanism during the prolonged duration and high amplitude V_{ds} bias. This mechanism may also be responsible for the mitigated positive V_{th} shift observed during the bias stage. The donor-like traps related hole-trapping mechanism in the p-GaN/AlGaN/GaN heterojunction may be responsible for these phenomena [60], [65], [86]. Indeed, the V_{th} shift phenomenon of GaN-HEMTs primarily involves the competition between electron trapping and hole trapping in the gate stack, hole trapping could result in negative V_{th} shift. This mechanism could explain the mitigation of the positive V_{th} shift and the quick recovery observed in Fig. 2.19. Additionally, the trapping and de-trapping time of holes could be much larger comparing to the electrons [60], [125], [126], due to the significantly low hole mobility (< 10 cm^2/V·s) [127]. This could explain the over-recovery of the shifted V_{th}, as the hole trapping compensates the electron trapping induced positive V_{th} shift, and the trapped holes require much longer time to be released compared to the trapped electrons, leading to a negative V_{th} shift in the recovery stage. The V_{th} over-recovery phenomenon is also observed after the device undertaking 100 s and 7 V of V_{gs} bias as described in [127].

Interestingly, both of the V_{th} dropping in Fig. 2.19(a) and V_{th} over-recovery phenomenon in Fig. 2.19(b) become pronounced when the V_{ds} bias exceeds 200 V. Physically, these effects could be linked to the hole trapping, which compensates for the electron trapping (corresponding to the reduced V_{th}) and exhibits a longer recovery time constant (corresponding to the long recovery time). Both phenomena suggest that the hole trapping mechanism becomes active and shows measurable parameter shift of Schottky-type GaN-HEMTs under prolonged duration and high V_{ds} bias.

For the IGOT60R070D1 (GIT), the same recovery rest is implemented. However, the measured V_{th} after 1 min of the recovery time is nearly the same as the original V_{th} with approximately 30 mV of variation, which indicates that the shifted V_{th} can get recovered in 1 min. This is reasonable since the shifted V_{th} under extended V_{ds} bias is already limited as shown in Fig. 2.15(a). This agrees with the hypothesis that microsecond-level recovery time constant is dominant in GIT devices after the extended time of V_{ds} bias, as discussed in Fig. 2.16.

The observed recovery behavior of the Schottky-type device is novel, with limited references available for validating these findings. To further rule out potential influences from the proposed measurement method (for example, the reverse conducted load current), an additional measurement technique with comparable V_{ds} bias stress and

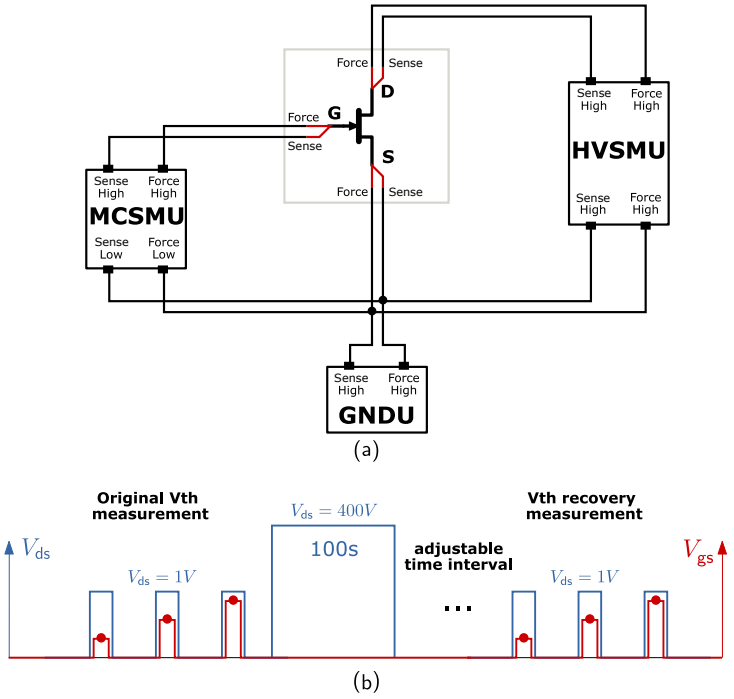


Figure 2.20: Schematic of (a) device connection in curve tracer and (b) the measurement sequence when using curve tracer to characterise the V_{th} recovery behaviour.

recovery time is required for cross-referencing.

2.2.2.3 Recovery behaviour verification by curve tracer

To further verify the V_{th} recovery behaviour of Schottky-type GaN-HEMTs after the extended time of V_{ds} bias and exclude the influence of reverse I_{ch} in the half-bridge based test, the curve tracer (B1505A) is employed to perform a similar test for the same DUT. It should be noted that the DUT is removed from the proposed test board and connected to the curve tracer to ensure the same DUT. The device connection and the measurement sequence set in the curve tracer are shown in Fig. 2.20. The high voltage source/measure unit (HVSMU) is used to provide the V_{ds} stress on the DUT and measure the I_d. The voltage and current can go up to 1.5 kV and 8 mA simultaneously in pulse-mode. The medium current source/measure unit (MCSMU) is used to provide the V_{gs} bias during the transfer characteristics measurement for V_{th}. The ground unit (GNDU) is connected to the source of the DUT and these two SMUs to provide ground reference.

To characterise the V_{th} recovery behaviour, the measurement and stress sequence are set as illustrated in Fig. 2.20(b). Before the extended time and high V_{ds} is applied on the DUT, the transfer characteristics are measured and the original V_{th} is extracted from the measured transfer characteristics. Afterward, the 400 V of V_{ds} bias is applied

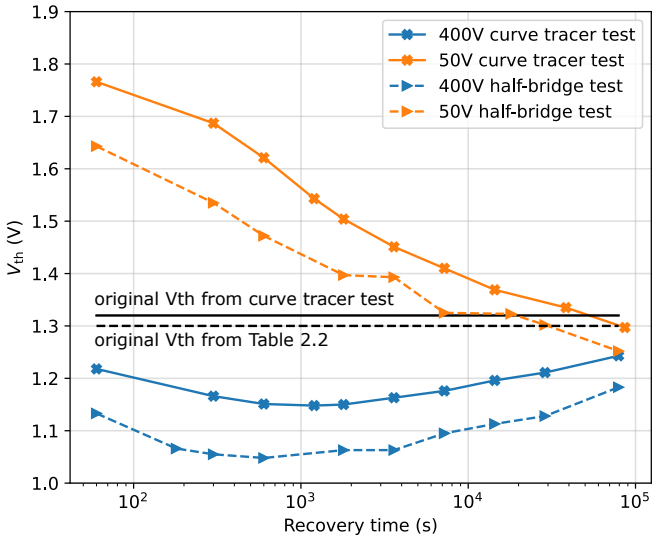


Figure 2.21: Comparison of V_{th} recovery behaviour at I_{ch} = 5 mA between curve tracer test and half-bridge based test for the same DUT sample.

on the DUT for 100 s as the bias stage. After an adjustable time interval (recovery time), the transfer characteristics will be measured again to obtain the recovered V_{th}. This measurement process is implemented for the same DUT as the half-bridge based test for 50 V and 400 V of V_{ds} bias, respectively. The relation between the recovered V_{th} and recovery time from these two kind of tests are compared Fig. 2.21. To be noted that, due to the current limitation of HVSMU, the V_{th} at I_{ch} = 5 mA from these two tests is adopted for comparison.

As illustrated in the figure, the over-recovery behaviour after 100 s and 400 V of V_{ds} bias still exists in the curve tracer based test, while it doesn't appear when the V_{ds} bias is 50 V. The V_{th} recovery behaviour shows the same trend in both curve tracer and half-bridge based test, validating the correctness of proposed half-bridge based test [1]. This also suggests that the over-recovery is solely due to the off-state V_{ds} bias as opposed to the reverse conducted load current in the half-bridge based test. Additionally, the V_{th} recovery behaviour of other GS-065-030-2-L and GS66502B devices are characterised by using the curve tracer, showing the same V_{th} recovery trend, suggesting the universality of this long-time and negative V_{th} recovery behaviour of Schottky-type GaN-HEMTs. Moreover, it should be noted that there is an offset between the results from curve tracer and half-bridge for the same DUT, offset that exists also on the original V_{th} test. This offset may come from the different measurement mechanisms of these two methods. For example, in the curve tracer test, the DUT is subjected to the V_{gs} bias (even small) during the transfer characteristics measurement and this small V_{gs} bias could lead to

[1] The curve tracer based method can only implment the proper V_{th} recovery measurement. Due to the limitation of the pulse-width and measurement response time, it is impossible to measure the V_{th} shift behaviour right after several microsecond of V_{ds} bias as discussed in section 1.3.3.5.

positive V_{th} shift for Schottky-type GaN-HEMTs [65], [88], [90]. On the other hand, this offset may be partly attributed to the measurement uncertainty of the half-bridge test, which can be caused by the probe offset or the perturbation induced by the EMI as the clamping circuit is not fully shielded. In conclusion, the extended duration and high V_{ds} bias could result in the over-recovery of the shifted V_{th}.

2.2.3 Summary of the single pulse test

In the experiments presented above, we have assessed the V_{th} shifts induced by single pulse of V_{ds} bias, for both Schottky-type GaN-HEMTs and GITs. The main findings can be summarised as following:

- The V_{th} of Schottky-type GaN-HEMTs and GITs show a positive and negative V_{th} shifts respectively with increasing the V_{ds} bias time, particularly after extending the bias time to seconds. The result of Schottky-type GaN-HEMTs agrees with the literature while the result of GITs is less reported in the literature.
- The ΔV_{th} shift in Schottky-type GaN-HEMTs is generally larger than that in GITs. However, the ΔV_{th} shift does not show an increase with the rising of V_{ds} bias amplitude for either type of devices.
- The recovery time constant of Schottky-type GaN-HEMTs after a 100 s of applied V_{ds} bias is longer than that of GITs. For Schottky-type GaN-HEMTs, minute- to hour-level time constants are observed, with full recovery taking approximately 3 days. In contrast, the shifted V_{th} of GITs can recover within 1 min. Moreover, an increased g_m is observed with increasing the bias time for GITs when the V_{ds} bias is higher than 200 V, which may indicate the existence of the microsecond-level time constant for V_{th} recovery.
- A reduction in positive V_{th} and an over-recovery of V_{th} are observed in Schottky-type GaN-HEMTs following a V_{ds} bias voltage exceeding 200 V applied for an extended duration (around or exceeding 100 s). These effects indicate the activation of a hole trapping mechanism under this stress condition, which is rarely reported in the literature.

The single pulse test aims to investigate the relationship between bias time or strength and the V_{th} shift. However, the results may not be representative of continuous operation. The time constants of the V_{ds} bias induced trapping and recovery of the shifted V_{th} (de-trapping) are critical to predicting the actual V_{th} when the device operates continuously in the PWM power converters. To further evaluate the real-time V_{th} of these two devices, the continuous mode test will be discussed in the following section.

2.3 Continuous mode test

In this section, the V_{th} shift phenomenon will be evaluated when the GaN-HEMTs undertake multi-pulses of V_{ds} bias in continuous mode, emulating converter-like operations.

Several test scenarios are implemented to investigate the influence of V_{ds} bias voltage, switching frequency, and duty-cycle on the real-time V_{th} for these two types of GaN transistors.

2.3.1 V_{th} measurement principle in continuous mode

The V_{th} measurement principle is the same as that in single pulse, as shown in Fig. 2.3, where the device is subjected to V_{ds} bias when the T_H is in on-state, and the V_{th} can be extracted at specific load current when the T_H is in off-state. The continuous mode test can be easily implemented by controlling the T_H with a PWM signal, meanwhile, the experiment setup remains the same as the single pulse test. In this condition, the DUT operates as a freewheeling diode in a buck converter, where the V_{ds} bias subjected to the DUT corresponds to the device under soft-switching condition. Therefore, the actual V_{th} when device operates continuously can be obtained. This also exhibits the convenience and good half-bridge compatibility of this in-situ V_{th} measurement method. For example, the measured switching waveforms and extracted V_{th} of GS-065-030-2-L in continuous mode are displayed in Fig. 2.22 to illustrate the V_{th} measurement principle. The V_{th} can be extracted using the same interpolation method as discussed in Fig. 2.3(c) and the first 80 cycles of V_{th} at $I_{ch} = 20\,\text{mA}$ are depicted in Fig. 2.22(b), clearly exhibiting a rising behaviour of the V_{th} with the increasing of switching cycles. It also shows the V_{th} accumulation effect due to the competition of trapping and de-trapping mechanisms inside the device. To be noted the I_{ch} of the DUT is controlled less than 200 mA and the total operating time for the first 80 cycles is less than 1 ms, so the influence of temperature can be neglected. To further evaluate the V_{th} shift in continuous operation mode, the influence of the recovery time constant, duty-cycle and switching frequency on the steady-state V_{th} for different devices are illustrated below.

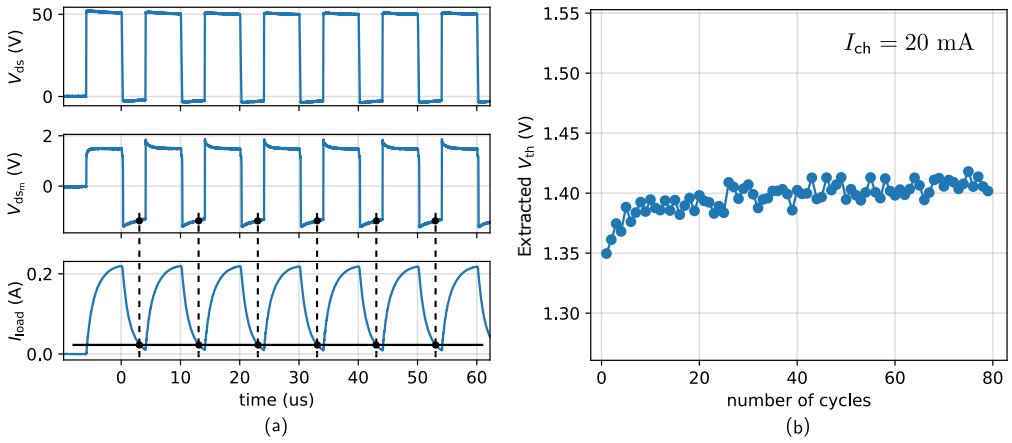


Figure 2.22: V_{th} measurement principle in continuous mode for GS-065-030-2-L (a) measured switching waveforms at $V_{dc} = 50\,\text{V}$, $f = 100\,\text{kHz}$, $D = 0.4$ (b) extracted V_{th} at $I_{ch} = 20\,\text{mA}$ from the first 80 switching cycles.

2.3.2 Measurement result of V_{th} in steady-state

The real-time V_{th} when the GS-065-030-2-L and IGOT60R07D1 operate continuously is characterised in this subsection. The different time constant of trapping and de-trapping can be estimated by adjusting the duty cycle and frequency of the PWM signal.

2.3.2.1 Influence of recovery time on the V_{th}

As shown in Fig. 2.22, the V_{th} shows a gradually rising trend, eventually reaching a saturation value due to the balance of trapping and de-trapping mechanisms, known as the steady-state V_{th}. The recovery time is critical for the actual steady-state V_{th} in continuous operation. To further evaluate this perspective, the steady-state V_{th} is measured with constant 1 µs of V_{ds} bias time under different frequency. This approach allows us to determine the effect of recovery time on the steady-state V_{th}.

For the DUTs used in this test, the V_{th} can saturate within 2 min of operation. Therefore, to exclude the influence of temperature on the measured V_{th}, the T_j should be controlled and evaluated during the 2 min test window. The load current I_{load} should be limited to reduce the ΔT_j of the DUT, so the V_{ds} bias is limited to 50 V in this investigation. Moreover, a thermocouple is used to monitor the T_c of the DUT during the measurement. The T_j can be evaluated by considering the dissipated power of the DUTs and the junction-to-case thermal resistance ($R_{\theta jc}$) provided by the datasheet as shown in equation 2.1 [55].

$$T_j = T_c + R_{\theta jc} \cdot P \tag{2.1}$$

Since the DUT operates under soft-switching and the I_{load} is limited to less than 200 mA with 220 Ω of power resistor and 78 µH of inductor, the variation between T_j and T_c is less than 1 °C in this case. The ΔT_c is less than 5 °C with 2 min of operation in 500 kHz, so the influence of temperature on the measurement result can be excluded.

The measured steady-state switching waveforms and extracted V_{th} of GS-065-030-2-L after 2 min of operation is displayed in Fig. 2.23, where the V_{th} at I_{ch} = 90 mA is selected because the minimum I_{ch} is around 90 mA when f = 500 kHz. In this measurement, the frequency increases from 1 Hz to 500 kHz, which means the recovery time decreases from 1 s to 1 µs in each switching cycle. When the frequency is less than 100 Hz, the steady-state V_{th} remains the same as the original V_{th}. It indicates that the 1 µs V_{ds} bias induced V_{th} shift has a less than 10 ms of time constant. The steady-state V_{th} increases notably once the frequency is higher than 1 kHz, and the 500 kHz can lead to around 30 % positive V_{th} shift comparing to that in 100 Hz. Moreover, the rise of the curve in Fig. 2.23(b) represents a two-level slope with 10 kHz as the dividing point. It may indicate the existence of two level time constant for V_{th} recovery, which are in the range of from 10 ms to 100 µs and from 100 µs to 1 µs. To exclude the influence of the measurement method, the same test is repeated by replacing the GaN-HEMTs with a SiC power diode and the steady-state V_{th} does not change with switching frequency, only a 20 mV of variation can be observed and it could be attributed to the measurement uncertainty, as shown in Fig. 2.24. Additionally, the V_{th} characterisation results from the single pulse test under 50 V of V_{ds} bias are plotted in Fig. 2.23(b), it shows that the

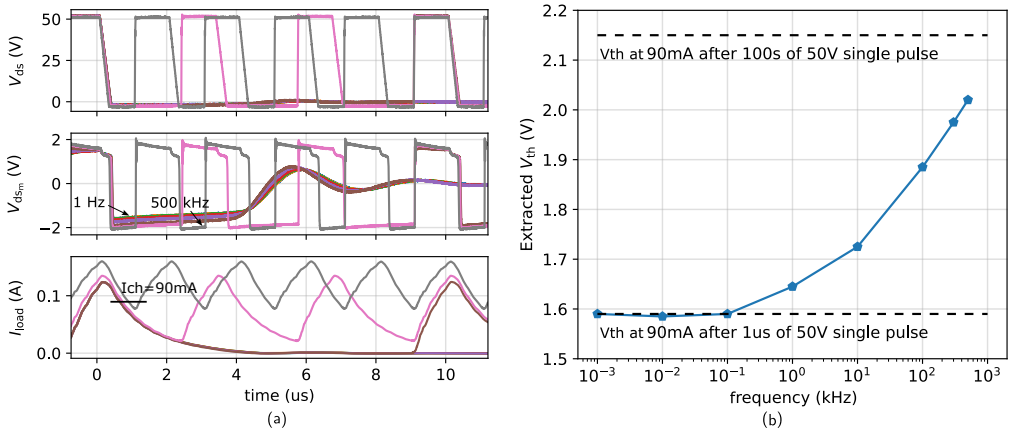


Figure 2.23: Influence of the recovery time on the steady-state V_{th} with 1 µs of bias time in each switching cycle for GS-065-030-2-L under V_{ds} = 50 V (a) measured switching waveforms (b) extracted V_{th} at I_{ch} = 90 mA versus operating frequency.

steady-state V_{th} is in the range of shifted V_{th} of single pulse test. A perspective may be obtained that the long time of single pulse V_{ds} bias (50 V) can induce a saturated ΔV_{th} and the steady-state V_{th} will be in the range of this maximum ΔV_{th}.

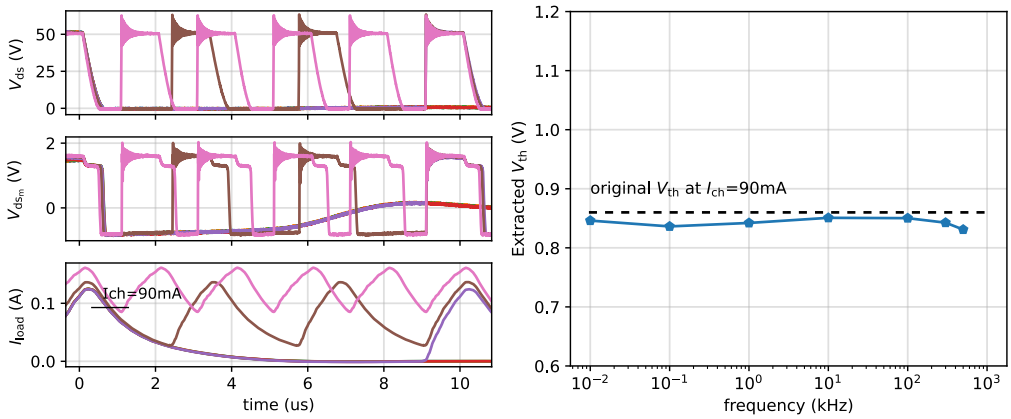


Figure 2.24: Influence of the recovery time on the steady-state V_{th} with 1 µs of bias time in each switching cycle for SiC power diode C4D40120D under V_{ds} = 50 V (a) measured switching waveforms (b) extracted V_{th} at I_{ch} = 90 mA versus operating frequency.

To further verify this perspective, similar test from 100 Hz to 1 MHz with 500 ns of bias time under 50 V was conducted. The steady-state V_{th} is still in the range of maximum ΔV_{th} from single pulse test, as shown in Fig. 2.25. The frequency axis is constrained by the V_{ds} pulse width. At 1 MHz, the stress and recovery phases each occupy 50 % of the cycle, reaching the limitation.

Same test is implemented for the IGOT60R07D1 as presented in Fig. 2.26 to evaluate the influence of recovery time of the GITs. The switching frequency increases from 10 Hz

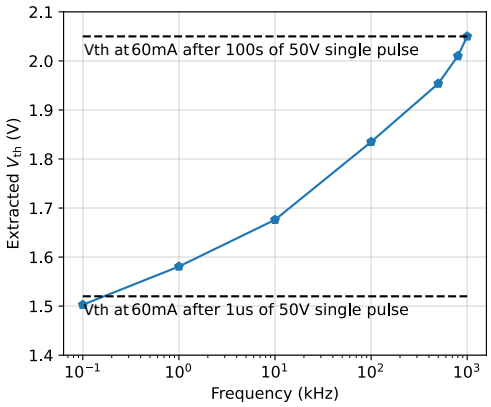


Figure 2.25: Extracted steady-state V_{th} at I_{ch} = 60 mA versus operating frequency with 500 ns of bias time in each switching cycle for GS-065-030-2-L.

to 500 kHz with 1 us of V_{ds} bias time in each switching cycle, however, the steady-state V_{th} does not indicate straightforward V_{th} variation. The less than 80 mV decreasing in V_{th} is within the same level of measurement uncertainty as that when evaluating the SiC power diode. Therefore, it can be concluded that the recovery time of the 1 us of V_{ds} bias (50 V) is less than 1 us or this V_{ds} bias will not induce notable V_{th} shift in the steady-state.

The influence of recovery time (no-stress time) on the steady-state V_{th} of GaN-HEMTs is evaluated, showing a significant impact on the V_{th} of Schottky-type GaN-HEMTs as a relative long de-trapping time constant. While, the its impact on the GITs is less noticeable. However, these test conditions are not practical from device application point of view, since the duty-cycle of T_H can be small to 0.00001 when the frequency is 10 Hz in above test scenarios. Hence, the steady-state V_{th} of GaN-HEMTs will be evaluated further in more practical conditions, where the duty-cycle is in the range of 0.1 to 0.7.

2.3.2.2 Influence of duty-cycle on the V_{th}

More practical duty-cycle range, from 0.1 to 0.7, is selected to evaluate its influence on the steady-state V_{th} of GaN-HEMTs with 100 kHz of operation frequency. Same RL load (R = 220 Ω, L = 78 µH) and V_{ds} = 50 V are adopted to inhibit the increase of T_j. In this operation, the increase of T_c in 2 min is less than 3 °C. The measured switching waveforms and extracted steady-state V_{th} at I_{ch} = 90 mA of GS-065-030-2-L are displayed in Fig. 2.27. The steady-state V_{th} does not show significant variation with the increase of duty-cycle. The slightly increase of V_{th} might be related to the measurement uncertainty.

Same test is implemented for IGOT60R07D1 and the results are shown in Fig. 2.28. An approximately 0.1 V of V_{th} decreasing is observed when the duty-cycle rises from 0.1 to 0.3 and then the V_{th} stabilises. This fact might be related to the V_{th} measurement

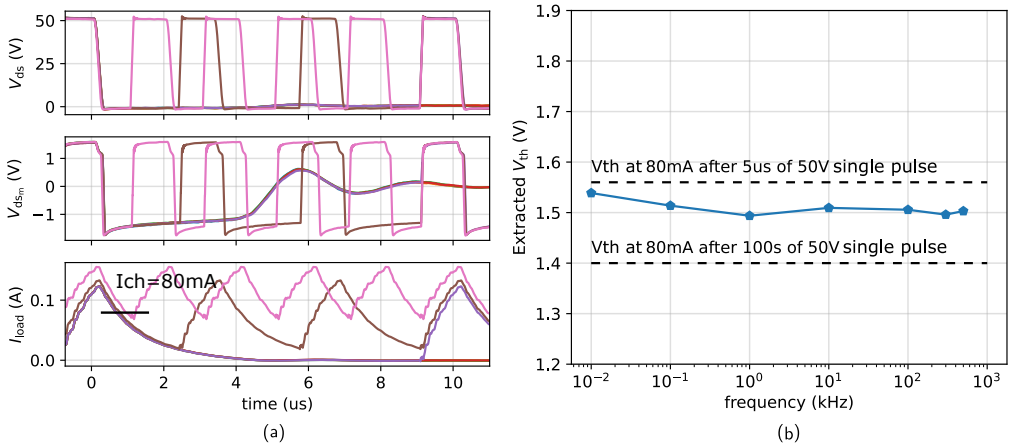


Figure 2.26: Influence of the recovery time on the steady-state V_{th} with 1 µs of bias time in each switching cycle for IGOT60R07D1 under V_{ds} = 50 V (a) measured switching waveforms (b) extracted V_{th} at I_{ch} = 80 mA versus operating frequency.

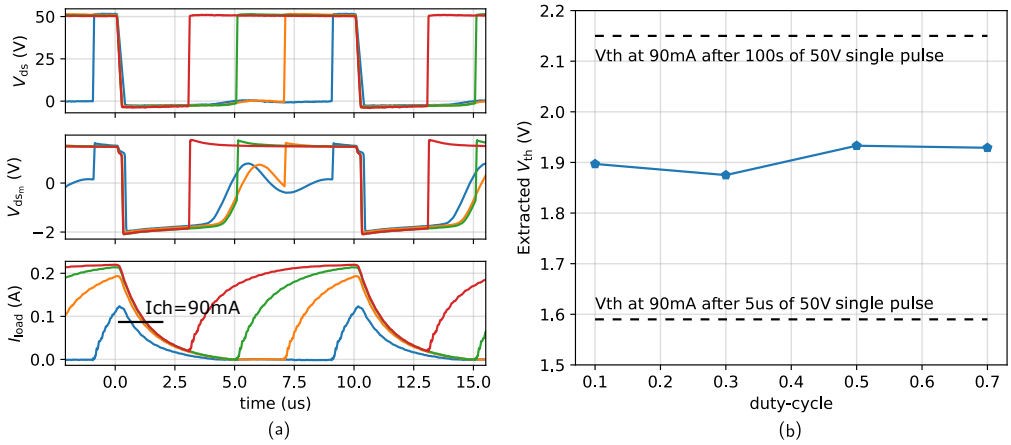


Figure 2.27: Influence of duty-cycle on the steady-state V_{th} of GS-065-030-2-L under V_{ds} = 50 V and f = 100 kHz (a) measured switching waveforms with duty-cycle range from 0.1 to 0.7 (b) extracted V_{th} at I_{ch} = 90 mA versus duty-cycle.

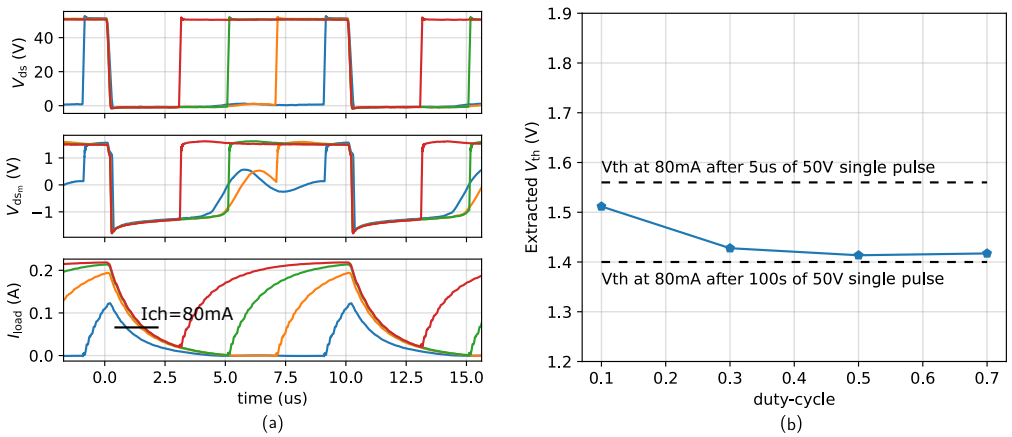


Figure 2.28: Influence of duty-cycle on the steady-state V_{th} of IGOT60R07D1 under $V_{ds} = 50\,V$ and $f = 100\,kHz$ (a) measured switching waveforms with duty-cycle range from 0.1 to 0.7 (b) extracted V_{th} at $I_{ch} = 80\,mA$ versus duty-cycle.

time variation, as shown in Fig. 2.28(a), where the V_{th} in 0.1 of duty-cycle is measured at around 1 µs and the V_{th} in other duty-cycle is measured at around 2 µs. This 1 µs variation may be responsible for the 0.1 V V_{th} dropping. For the Schottky-type GaN-HEMTs, this time variation is still present, but the influence on measured V_{th} is much smaller than that for the GIT device.

In general, the influence of duty-cycle on the steady-state V_{th} is not significant as shown in above tests. This fact may be due to the relative small variation in the duty-cycle. However, the time to reach the steady-state V_{th} may vary with different duty-cycle, which will be discussed in the future work. However, in actual device application, the operation frequency may have more significant impact on the steady-state V_{th}, which will be discussed in the following.

2.3.2.3 Influence of switching frequency on the V_{th}

To evaluate the influence of switching frequency on the steady-state V_{th}, similar experiments are implemented as illustrated in Fig. 2.27 and Fig. 2.28. The difference is that the duty-cycle of the PWM signal is set to 0.5 and the frequency rises from 10 Hz to 500 kHz. The results for the GS-065-030-2-L are displayed in Fig. 2.29, where the steady-state V_{th} exhibits approximately a 0.2 V positive shift as the frequency increases. This positive V_{th} shift primarily occurs when the switching frequency rises from 100 Hz to 10 kHz, beyond this point, it gradually reaches saturation. This result disagrees with the conclusion from [99] that the V_{th} of Schottky-type GaN-HEMTs is independent from switching frequency. This conclusion may be due to the limited pulses applied in testing presented in [99], as the whole measurement time window is only 200 µs, when the V_{th} shift phenomenon is not saturated, while our measurement time window is 2 min. Moreover, during the 2 min test, a shift of V_{dsm} can be observed with the increasing of testing time, supporting the hypothesis that the V_{th} shift phenomenon requires longer

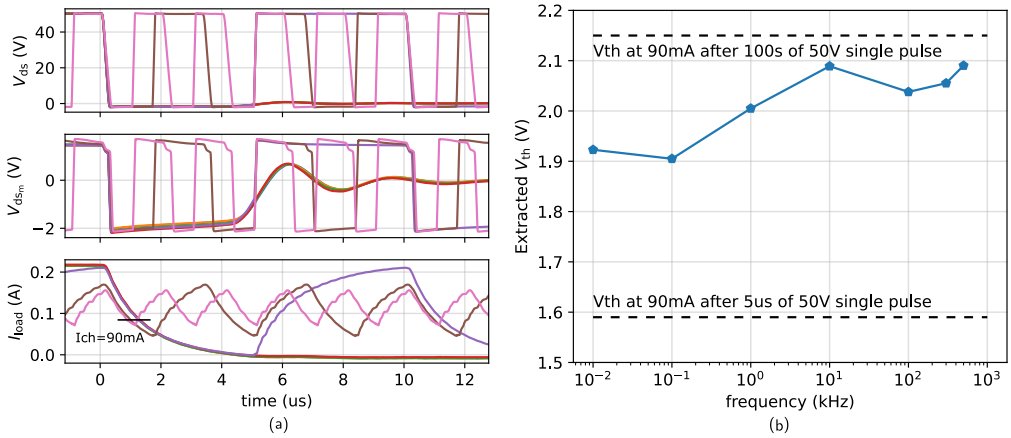


Figure 2.29: Influence of switching frequency on the steady-state V_{th} of GS-065-030-2-L under 50 V of V_{ds} bias and 0.5 of duty-cycle (a) measured switching waveforms with switching frequency increasing from 10 Hz to 500 kHz (b) extracted V_{th} at I_{ch} = 90 mA versus switching frequency.

time to get saturated. The following measurement results in this subsection can support this perspective as well.

The measurement results of IGOT60R07D1 are depicted in Fig. 2.30, where the V_{th} remains nearly constant with the increasing of operation frequency, presenting a variation not higher than 50 mV. It should be noted that the V_{th} of IGOT60R07D1 at I_{ch} = 80 mA remains at 1.5 V with a less than 100 mV variation in all previous tests, this V_{th} level exhibits the stability of the GIT devices.

The V_{ds} voltage in above tests is limited to 50 V to reduce the load current and to exclude the influence of temperature, however, this voltage is relatively low for a 600 V level of power GaN-HEMTs. Under higher V_{ds} bias amplitude, other trapping related mechanisms could occur, such as the donor-like traps related hole trapping and the hole-injection for GITs, these mechanisms that can neutralise the influence of the trapped electrons as discussed in section 2.2, therefore, it is required to evaluate the V_{th} variation under higher V_{ds} voltage. To properly control the increase of T_j, a larger power resistor (860 Ω) is used to limit the I_{ch} of DUTs. Correspondingly, an increased inductor (325 µH) is adopted to ensure the time constant of this RL load close to the previous RL load configuration. Indeed, a too large RL time constant can increase the measurement response time t_t^m in this method, as discussed in Fig. 2.13.

The steady-state V_{th} of these two devices tested under 2 min of 400 V V_{ds} bias operation are evaluated by using a large RL load, where the switching frequency increases from 10 Hz to 500 kHz same as the test under 50 V. The results of GS-065-030-2-L are displayed in Fig. 2.31. It should be noted that the maximum ΔT_c can go up to around 30 °C when the frequency is 500 kHz, which can be attributed to higher average I_{ch} through the DUTs. Since the influence of temperature cannot be fully eliminated in current measurement conditions, the measured T_c by the thermocouple is indicated in

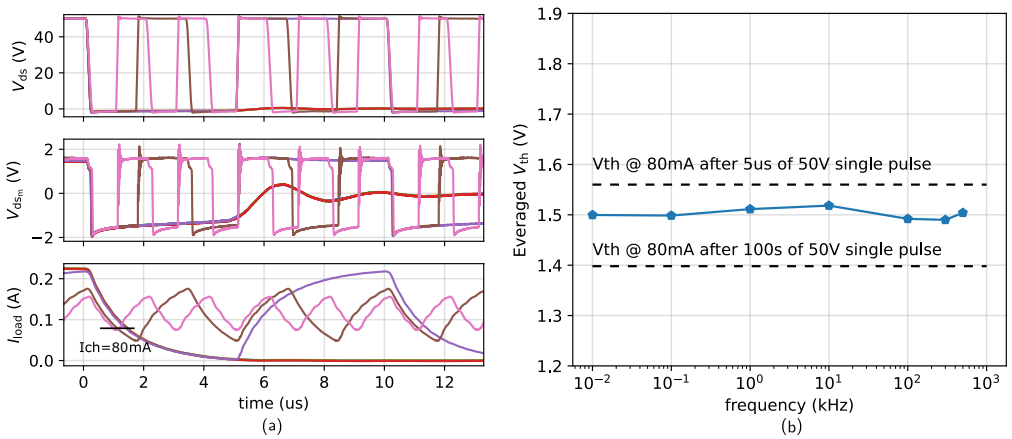


Figure 2.30: Influence of switching frequency on the steady-state V_{th} of IGOT60R07D1 under 50 V of V_{ds} bias and 0.5 of duty-cycle (a) measured switching waveforms with switching frequency increasing from 10 Hz to 500 kHz (b) extracted V_{th} at I_{ch} = 80 mA versus switching frequency.

the steady-state V_{th} as shown in Fig. 2.31(b). Similar to the 50 V test, the V_{th} exhibits a rising trend with the rise of the switching frequency while the maximum ΔV_{th} is around 0.2 V. Although the measured T_c in 500 kHz is around 30 °C higher than that for 10 Hz, the increasing behaviour of V_{th} does not show significant variation when compared to the test under 50 V. Moreover, the original V_{th} of the commercial Schottky-type GaN-HEMTs (same series with the used DUT) is approximately independent on the temperature as reported in [35]. The high temperature could speed up the de-trapping of electrons [35], [80], [81], so the V_{th} may decrease with the increasing of temperature, however, this phenomenon is not reflected in the results. It may indicate the 30 °C of ΔT_c cannot cause notable influence on the V_{th} shift.

The results from IGOT60R07D1 test are shown in Fig. 2.32, where the steady-state V_{th} initially rises and then falls with the frequency increasing. However, the V_{th} variation is not critical, and the ΔV_{th} remains within the range of 0.2 V.

It should be noted that the steady-state V_{th} shown in Fig. 2.31(b) and Fig. 2.32(b) is not in the range of ΔV_{th} measured from the single pulse test. The steady-state value could be attributed to the different measurement response time t_m between the steady-state and single pulse test. For example, when the I_{ch} = 140 mA, the t_m for steady-state V_{th} is around 1 µs, whereas the t_m in the single pulse test is approximately 3.8 µs because of the higher load current (small RL load) as shown in Fig. 2.13. If the microsecond-level V_{th} recovery time constant is presented, the 2.8 µs of Δt_m could cause measurement error. In other words, the measured V_{th} at 3.8 µs have recovered more than that measured at 1 µs. This can explain why the measured steady-state V_{th} is higher than when measured by the single pulse. Also, the offset between the steady-state V_{th} and single pulse result is larger for GITs, this may be explained by the existence of microsecond or nanosecond-level of recovery time constant in GITs, as mentioned in Fig. 2.16. This different t_m

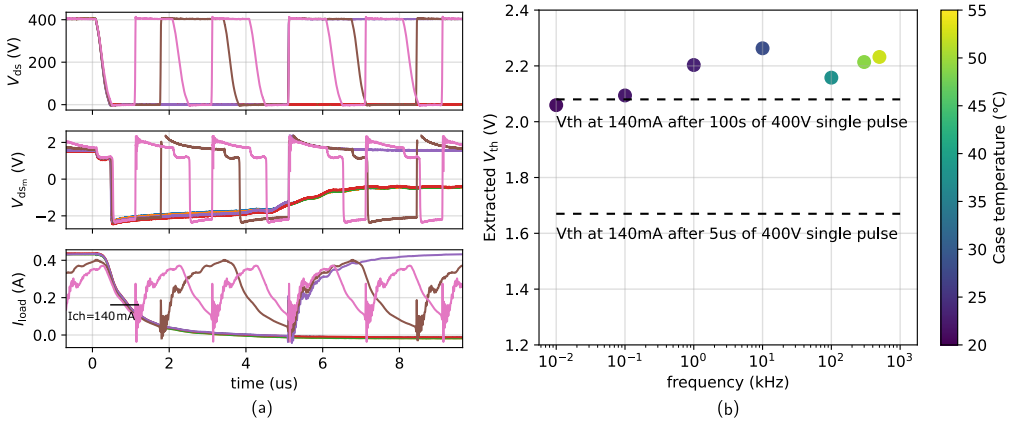


Figure 2.31: Influence of switching frequency on the steady-state V_{th} of GS-065-030-2-L under 400 V of V_{ds} bias and 0.5 of duty-cycle (a) measured switching waveforms with switching frequency increase from 10 Hz to 500 kHz (b) extracted V_{th} at I_{ch} = 140 mA versus switching frequency with different T_c.

produced measurement error is the drawback of this proposed V_{th} shift characterisation method, when microsecond-level and faster V_{th} recovery time constant present. Specific RL load should be selected to make sure the V_{th} is measured with same recovery time and I_{ch} when comparing the V_{th} shift under different V_{ds}. However, this drawback will not influence the measurement accuracy under different bias time or switching frequency, since the t_m remains unchanged in those tests.

To determine the V_{th} accumulation effect of GaN-HEMTs in the continuous operation, the V_{th} from the first 950 switching cycles and the steady-state are measured. A practical operation condition is selected to show the generalisation of this phenomenon, with V_{dc} set to 400 V and a switching frequency of 100 kHz with 0.5 of duty-cycle. The RL load is the same as the previous 400 V test. The measurement switching waveforms and the extracted V_{th} for GS-065-030-2-L and IGOT60R07D1 are respectively shown in Fig. 2.33. These two GaN-HEMTs exhibit distinct V_{th} shift behaviours under the same test condition. The Schottky-type GaN-HEMTs show a positive V_{th} shift with the increasing of switching cycles, especially in the first 50 cycles. The fast V_{th} shift in the first 50 cycles may indicate a mechanism with fast time constant. For example, the floating p-GaN layer related hole-deficiency mechanism can cause a positive V_{th} shift with fast time constant for the Schottky-type GaN-HEMTs as reported in [35], [85]. It also should be noted that the duration of the first 950 switching cycles is taking only 10 ms, in which the T_j does not increase significantly, so the influence of temperature on the V_{th} in this fist 950 cycles can be excluded. There is around 0.45 V positive ΔV_{th} compared between the first switching cycle and the steady-state. Similar positive V_{th} shift and saturation behaviour in continuous mode is also reported in [101]. The GIT shows a negative V_{th} shift and get saturated with further increasing the switching cycles. The negative ΔV_{th} is around 0.3 V when compared between the first cycle and steady-state. The GIT does not show the quick V_{th} shift as the Schottky-type GaN-HEMTs,

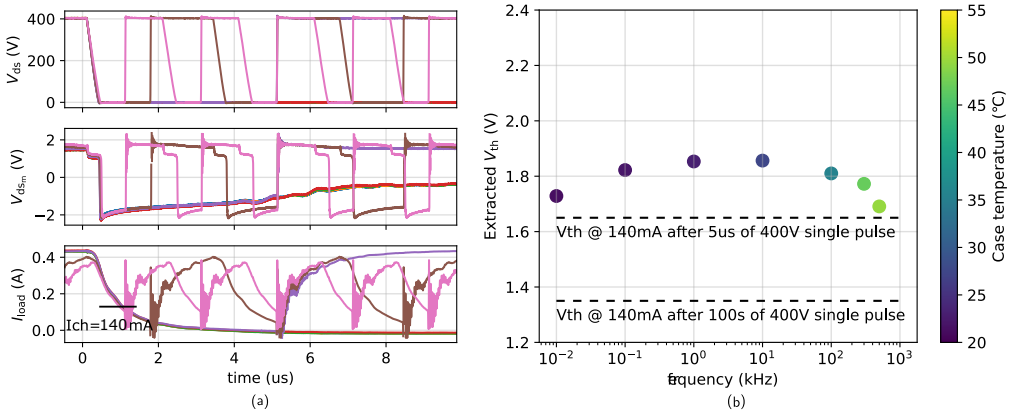


Figure 2.32: Influence of switching frequency on the steady-state V_{th} of IGOT60R07D1 under 400 V of V_{ds} bias and 0.5 of duty-cycle (a) measured switching waveforms with switching frequency increase from 10 Hz to 500 kHz (b) extracted V_{th} at I_{ch} = 140 mA versus switching frequency with different T_c.

which can be explained by the Ohmic-type contact between the p-GaN layer and gate metal, where the p-GaN layer is not floating and the hole-deficiency is not present as discussed in the Fig. 1.8 and [73], [97].

2.3.3 Summary of the continuous mode test

The V_{th} shift phenomenon in continuous mode is evaluated for the GS-065-030-2-L and IGOT60R07D1 devices. The findings can be summarised as following:

- The steady-state V_{th} is dependent on the time constant of electron trapping and de-trapping mechanisms. The V_{th} of Schottky-type GaN-HEMTs increases significantly with reducing the V_{th} recovery time, while the V_{th} of GIT remains more stable in the same test conditions. This phenomenon indicates that the GIT device may have a faster (microsecond or less) de-trapping time constant than the Schottky-type GaN-HEMTs.
- When it operates in several hundred kHz, the change of duty-cycle does not influence the steady-state V_{th} notably on any of these two devices.
- When the duty-cycle is constant, the steady-state V_{th} of Schottky-type GaN-HEMTs exhibit a slightly positive V_{th} shift with the increasing of switching frequency, while the V_{th} of GIT remains more stable. The relative stable V_{th} of GIT may be attributed to the Ohmic-type gate contact and hole-injection mechanism from the PD-structure.
- The dynamic V_{th} at the beginning of the switching cycles is evaluated under a high voltage operation condition for the 600 V level power GaN-HEMTs, showing that the Schottky-type GaN-HEMTs present a positive V_{th} shift with increasing

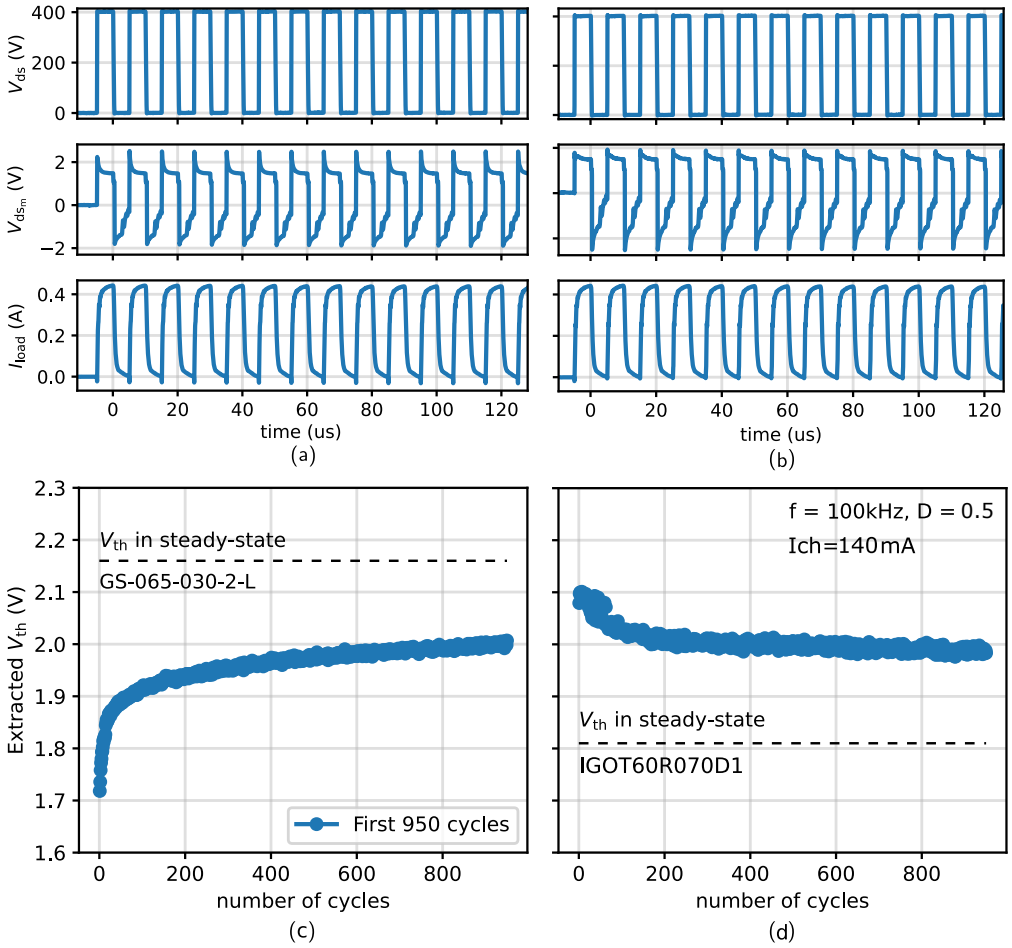


Figure 2.33: Dynamic V_{th} shift effect under 400 V of V_{ds}: measured switching waveforms from the first several switching cycles (a) GS-065-030-2-L (b) IGOT60R07D1. Comparison of the V_{th} at I_{ch} = 140 mA from the first 950 switching cycles and the steady-state (c) GS-065-030-2-L (d) IGOT60R07D1.

switching cycles, while the GIT shows a negative V_{th} shift. This variation indicates the existence of different V_{th} shift related mechanisms. However, it should be noted, even the GIT show a negative V_{th} shift with increasing the switching cycles, the steady-state V_{th} is higher than the corresponding original V_{th}. It could be related to the partial activation of the hole-injection mechanism during this multi-pulse continuous test.

2.4 Conclusion and discussion

2.4.1 V_{th} shift variation in single pulse and continuous test

In the single mode test, the Schottky-type GaN-HEMTs and GITs respectively show a significant positive and slightly negative V_{th} shift after the extended V_{ds} bias, when compared to the original V_{th}. Specifically, the ΔV_{th} of these two devices after 100 s of 400 V bias are respectively 0.44 V and -0.06 V, compared to the original V_{th}. This shifted V_{th} of Schottky-type GaN-HEMTs requires several tens of hours to get fully recovered, while the GITs show a faster recovery speed (less than 1 min). In the continuous mode test, the steady-state V_{th} of both the GaN-HEMTs and GITs presents a positive V_{th} compared to the original V_{th} under 400 V of V_{ds} bias, with 0.56 V for GaN-HEMTs and 0.4 V for GITs, although the V_{th} of GITs shows a reduced trend with the increasing of operation cycles as shown in Fig. 2.33.

The positive ΔV_{th} in the steady-state are higher when compared to that from the single pulse. For the Schottky-type GaN-HEMTs, the higher ΔV_{th} in continuous mode can be explained by the weak or absent hole-assisted de-trapping mechanism. In the extended time single pulse test, high V_{ds} bias could induce a strong electric field that may ionise the donor-like traps in the gate stack, generating holes to neutralise the trapped electrons, leading to lower positive V_{th} shift as discussed in section 2.2.1. However, in continuous mode testing, this mechanism may not occur or may become very weak. This explanation is supported when comparing the recovery behaviour of V_{th} after 100 s of 400 V single V_{ds} pulse and 2 min of continuous mode test under 400 V, as shown in Fig. 2.34. After the extended time of single pulse, the V_{th} shows an over-recovery phenomenon when compared with the original V_{th} as discussed in Fig. 2.21, and this phenomenon is attributed to the hole trapping mechanism. While the over-recovery does not appear after 2 min of continuous mode test, the recovery behaviour is similar to that observed after the 50 V single pulse test, where the hole trapping effect may not occur under such a low V_{ds} bias. Due to the difficulty of evidencing the hole trapping mechanism inside the device, the above analysis is just a hypothesis. However, the new findings about the different recovery behaviour of shifted V_{th} can confirm that the V_{th} shift related mechanisms differ on the extended single pulse test and the continuous mode test. This demonstrates the necessity of evaluating V_{th} shift in converter-like operation mode, as V_{th} measurements from single pulse tests cannot represent V_{th} in continuous operation. Considering the complex mechanisms related to V_{th} shift and the vastly different application scenarios of GaN-HEMTs, the in-situ V_{th} measurement is critical to evaluate the V_{th} of GaN-HEMTs in power converters.

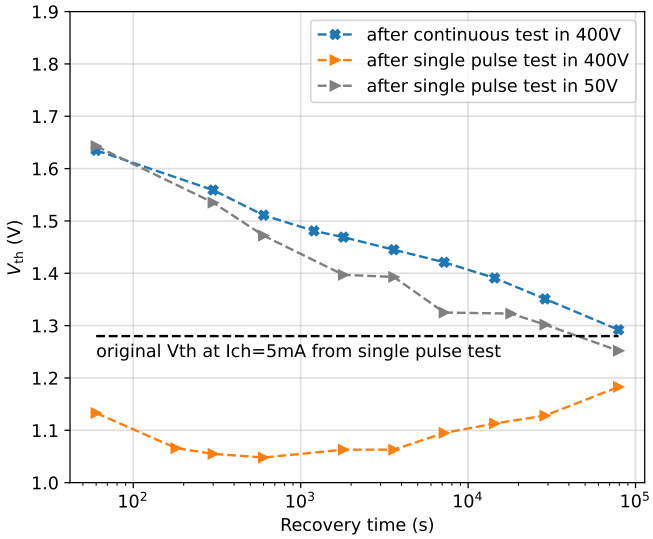


Figure 2.34: Recovery behaviours of shifted V_{th} for GS-065-030-2-L after 100 s of single pulse V_{ds} bias under 50 V and 400 V and 2 min of continuous mode test with $f = 100$ kHz and $D = 0.5$ under 400 V.

To provide guidance for applying GaN-HEMTs in power converter applications, it is important to discuss the short-term V_{ds} bias induced V_{th} shift, as the devices are controlled by short pulses PWM signals. For the Schottky-type device, as displayed in Fig. 2.12, a single V_{ds} bias (5 us) will not induce notable V_{th} shift, but the continuous V_{ds} bias (1 us) with 1 kHz above frequency can cause significantly positive V_{th} shift as shown in Fig. 2.23. For the Ohmic-type device, the short-term V_{ds} bias could cause positive V_{th} shift in both single and continuous ($V_{ds} = 400$ V) modes but the amplitude remains low compared to the Schottky-type device, as shown in Fig. 2.15 and Fig. 2.32 respectively.

2.4.2 Limitation and future work

To compare the V_{th} shift phenomenon under various V_{ds} bias amplitudes, it is necessary to keep identical V_{th} measurement time t_m, as shown in Fig. 2.13(b). In other words, the measured V_{th} should have same recovery time after different V_{ds} bias amplitudes. Additionally, it is convenient to quantify the shifted V_{th} when comparing it at the same I_{ch}. Therefore, when comparing the V_{th} shift under various V_{ds} amplitudes, different RL load should be selected to ensure that the V_{th} is measured under the same I_{ch} and with same t_m. The increased t_m under higher V_{ds} bias amplitude underestimated the shifted V_{th} when compared to the V_{th} under low V_{ds} bias and faster t_m, especially when a microsecond-level recovery time constant exists. Selecting the proper RL load for each operating condition increases the complexity of this method when comparing the V_{th} shift at different V_{ds} voltage amplitudes. Moreover, a relatively low load current

should be maintained to mitigate the rise of t_j under high voltage and continuous mode operation, further complicating the selection of the RL load. An adjustable RL load could be considered to solve this issues while ensuring compatibility with this proposed method.

For the V_{th} recovery measurement, as discussed in Fig. 2.17, the adjustable recovery time is manually controlled in this work. This approach does not guarantee precise control over the recovery time, nor does it allow for reducing the recovery time to the millisecond or microsecond level. The programmable control for the high voltage power supply and function generator can be adopted to further evaluating the recovery behaviour of V_{th} with an accurate controlling of recovery time, which would be the further work of this characterisation.

2.4.3 Influence of the shifted V_{th} on device performance

Based on the characterisation result from the single pulse testing, it can be concluded that the extended time of single pulse V_{ds} bias can induce a significantly positive V_{th} shift for the Schottky-type GaN-HEMTs and the shifted V_{th} requires several days to fully recover. Moreover, the long duration of V_{ds} bias (300 V above) could result in a negative V_{th} comparing to the original V_{th} of the device, which increases the risk of false-turn on [43] or gate instability [42] issues for the Schottky-type GaN-HEMTs. The long time recovery behaviour should be highlighted when characterising the V_{th} or other related parameters for Schottky-type GaN-HEMTs, because a transistor can experience long term V_{ds} bias when the converter belongs to a standby mode. Therefore, it is necessary to make sure that the V_{th} is in a original or saturated shift conditions, when characterising the V_{th} related parameters.

The V_{th} of these two types of devices shows a positive V_{th} shift under continuous V_{ds} bias conditions, while the shifted V_{th} of GIT is lower than that for the Schottky-type GaN-HEMTs. The positive shifted V_{th} could increase the reverse conduction loss when device operates as a freewheeling diode or during the dead-time in power converter applications. Additionally, the positive shifted V_{th} could manifest as an increase of the R_{on} of the GaN-HEMTs when the gate voltage is not sufficient (less than 5 V) for the Schottky-type GaN-HEMTs [57], [128]. Consequently, the positive V_{th} could increase the total losses and reduce the efficiency of the GaN-based power converters.

The positive V_{th} shift may influence the switching behaviours of GaN-HEMTs [95], [98], [104], [105], but lacking of theoretical analysis and demonstration. While this perspective is important, as it could influence the switching losses and EMC issues of the GaN-HEMTs, the influence of V_{th} shift on the switching behaviour of GaN-HEMTs will be discussed in the next chapter.

Chapter 3

Influence of V_{th} shift on the switching behaviour

Outline of the current chapter

The influence of V_{th} shift phenomenon on the switching behaviour of GaN-HEMTs will be discussed in this chapter. Initially, the phenomenon of different voltage biases induced V_{th} shift in the double-pulse test (DPT) is discussed to explore whether the shifted V_{th} can affect the switching behaviour of the device under test (DUT). Moreover, an H-bridge based DPT is introduced to control the initial V_{ds} bias to decouple the different voltage bias induced V_{th} shifts. Subsequently, the influence of V_{th} shift on the device commutation is analysed theoretically. To demonstrate the influence of V_{th} shift on the switching behaviour of GaN-HEMTs, the high-voltage and high current (HVHC) $I-V$ characteristics are presented, afterward, these $I-V$ characteristics are imported to the model of GaN-HEMTs. In this way, the GaN-HEMT models can include the V_{th} shift phenomenon, and its influence on the device switching behaviour can be demonstrated by simulation. Finally, the experiments are implemented to validate the theoretical analysis and simulation result.

3.1 V_{th} shift phenomenon in double-pulse test

In this section, the different voltage biases in the conventional DPT are discussed. Afterward, the potential influence of varying V_{ds} biases on the switching behaviour of GaN-HEMTs in DPT is analysed. Finally, an H-bridge based DPT is introduced to decouple the influence of the two types of V_{ds} biases, as classified in section 1.3.3.6, on the switching behaviour of GaN-HEMTs. It should be noted that the I-type V_{ds} bias induced V_{th} shift is studied in chapter 2, which corresponds to the soft-switching. However, in the hard-switching, investigated using the DPT, the II-type V_{ds} bias is involved and it will be developed later. It is therefore necessary to decouple these two types of V_{ds} biases, as well as to analyse and model the V_{th} shift phenomenon arising from each V_{ds} bias type.

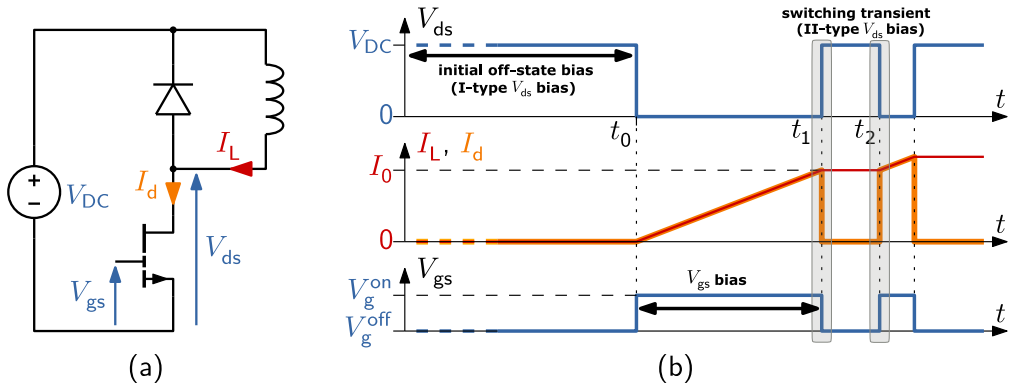


Figure 3.1: Conventional double-pulse test (DPT) (a) schematics and (b) corresponding switching waveforms including different types of voltage biases.

3.1.1 Various voltage biases in conventional DPT

3.1.1.1 Introduction of conventional DPT

The DPT is a typical experimental method that enables the evaluation of the hard-switching behaviour for power transistors under different voltage and current levels [129]. The DPT can be conveniently implemented using a switching cell with an inductor load, with the schematic and typical switching waveforms depicted in Fig. 3.1. The low-side transistor is the device under test (DUT) and the high-side device operates as a freewheeling diode after the DUT switches from on- to off-state. Initially, the DUT is in off-state and subjected to the V_{DC} voltage bias. Once the DUT is turned on, the load inductor is charged and I_d starts to increase, as shown in Fig. 3.1(b) from t_0 to t_1. In this stage, the I_d follows by the equation:

$$I_d = I_L = V_{DC}\frac{t_1 - t_0}{L} \tag{3.1}$$

Therefore, by adjusting V_{DC} and time interval between t_0 and t_1, the hard-switching behaviour of DUT at different voltage and current can be evaluated, where the turn-on and turn-off transition are respectively shown at t_2 and t_1. To be noted that the load current I_L will freewheel through the high-side diode when the DUT is in off-state between t_1 and t_2. If the time interval $[t_1, t_2]$ is small enough, with a large load inductor, the I_L could remains nearly unchanged in this period, making the device turn-on and -off at the same I_d value.

3.1.1.2 Different voltage biases induced V_{th} shift in DPT

It is essential to discuss the different voltage biases in detail when a GaN-HEMT is adopted as the DUT in the DPT, because each voltage bias has the potential to induce V_{th} shift. As discussed in Table 1.6, V_{ds} biases can be classified into two types depending on whether V_{ds} overlaps with I_d. Correspondingly, in Fig. 3.1(b), the DUT is shown

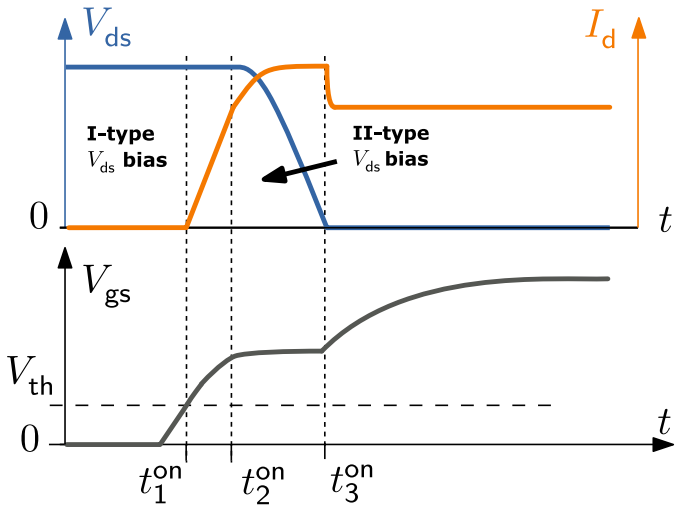


Figure 3.2: II-type V_{ds} bias in the turn-on switching waveform from the DPT.

subjected to the I-type V_{ds} bias when the device is in off-state, in two time intervals [0, t_0] and [t_1, t_2]. The V_{ds} bias during the hard-switching transition t_1 and t_2 is assumed as the II-type V_{ds} bias, because the I_d rises or falls under high V_{ds}, resulting in different stress for the DUT. Additionally, when the DUT is in on-state between t_0 and t_1, the device is subjected to the 6 V of V_{gs} bias and this bias might influence the device's V_{th} as well.

3.1.1.3 Two types of V_{ds} bias during turn-on commutation

The DPT is primarily employed to evaluate the switching behaviour of the power transistors, for GaN-HEMTs, the various voltage biases in the DPT may influence the measured switching behaviour, due to the voltage bias induced V_{th} shift. When investigating the influence of V_{th} shift on the switching behaviour of GaN-HEMTs, it is necessary to discuss the II-type V_{ds} bias in detail. Because this type of V_{ds} bias appears during the switching transition, and the induced V_{th} shift could directly influence the switching transition of the GaN-HEMTs, for example, it is the V_{th} that determines when the I_d starts to rise in the turn-on transition. Specifically, a typical turn-on waveform in hard-switching is depicted in Fig. 3.2. Before t_1^{on}, the device is in off-state and subjected to the I-type V_{ds} bias. After t_1^{on}, V_{gs} exceeds V_{th} and I_d starts to rise. However, during the current rising stage V_{ds} maintains a high voltage close to V_{DC}. This high V_{ds} could induce a negative V_{th} shift as reported in [73], [97]. Moreover, the hot electron related trapping mechanism could occur under this II-type V_{ds} bias due to the overlap between high V_{ds} and I_d, further influencing the V_{th} in hard-switching. These two types of V_{ds} bias may cause various V_{th} shift behaviour due to the different related mechanisms. Therefore, it is necessary to distinguish them and study their influence on switching behaviour respectively.

The initial I-type V_{ds} bias in the conventional DPT should be specially noted as well,

since the induced V_{th} shift could influence the following switching transition, due to the long recovery time of the shifted V_{th}. As shown in Fig. 3.1, the I-type V_{ds} bias is applied to the DUT once the DPT is in standby mode. In this state, the V_{DC} is adjusted to a high value, but the test is still on hold, and the corresponding switching waveform is shown in Fig. 3.1(b) before t_0. This I-type V_{ds} may persist from several seconds to minutes and cause a positive V_{th} shift, more importantly, this shifted V_{th} requires a long time to get recovered as discussed in Section 2.2. Therefore, the initial I-type V_{ds} bias induced V_{th} shift could influence the following test result from DPT, and the initial I-type V_{ds} bias must be controlled to accurately evaluate the switching behaviour of GaN-HEMTs in DPT.

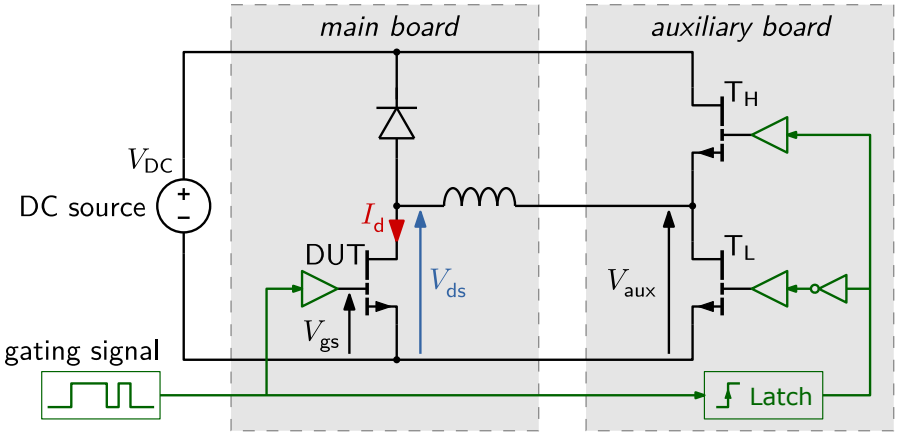
To summarise, the initial I-type V_{ds} bias could influence the switching behaviour when GaN-HEMTs are tested in DPT, as the shifted V_{th} cannot be fully recovered before the switching transition. The switching behaviour could also be influenced by the II-type V_{ds} bias due to the instantaneous shift in V_{th} during the switching transition. Moreover, these two types of V_{ds} bias may cause opposite V_{th} shift and both influence the switching behaviour of GaN-HEMTs in DPT. It is essential to decouple these two types V_{ds} bias in DPT and investigate their impact on the switching behaviour.

3.1.2 Introduction of H-bridge based DPT

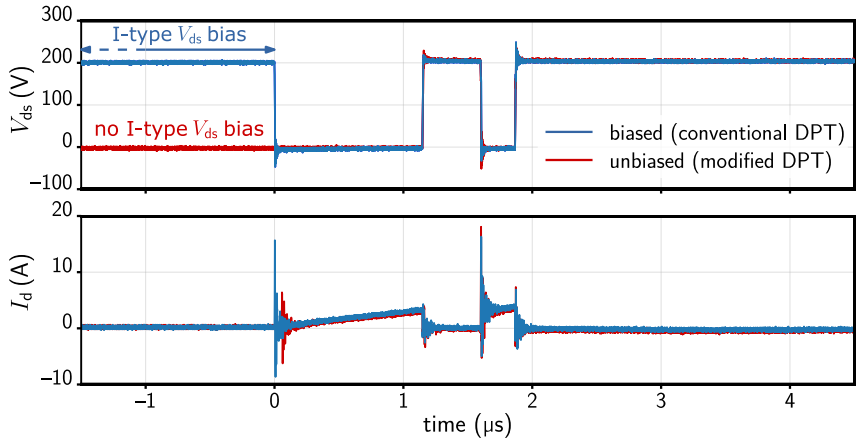
To evaluate the V_{th} shift phenomenon of GaN-HEMTs in DPT, the initial I-type V_{ds} bias should be controlled. Some circuits are proposed to control the initial V_{ds} bias when evaluating the dynamic R_{on} of GaN-HEMTs as reported in [78], [130], [131]. In this work, an H-bridge based DPT proposed in [42] is adopted to investigate the influence of the initial V_{ds} bias induced V_{th} shift on switching behaviour. The H-bridge based DPT not only enables the control of the initial I-type V_{ds} bias but also could sustain a conventional DPT.

The schematic and corresponding waveforms are displayed in Fig. 3.3, where the H-bridge is composed of a main board and an auxiliary board. The main board is similar to the conventional DPT half-bridge, with the high-side device operating as a freewheeling diode. The auxiliary board is a half-bridge with a D-type flip-flop in the gate loop, and T_H and T_L operate complementary. The two boards are controlled by a single signal to operate synchronously, where two operation modes can be achieved:

- **Modified DPT:** when the DPT is in standby mode, the DUT is in off-state controlled by the gate signal, simultaneously, the T_H and T_L in auxiliary board are in off- and on-state respectively. In this condition, the $V_{ds} = V_{aux} = 0\,V$, the DUT is not subjected to the initial I-type V_{ds} bias as opposed to the conventional DPT. Once the DUT is turned on by the gate signal, the T_H and T_L will be respectively turned on and off, simultaneously, the rise edge of gate signal will trigger the D-type flip-flop and the state of T_H and T_L will be locked. Afterward, the DUT can be tested as in the conventional DPT.
- **Conventional DPT:** to achieve the conventional DPT directly using this set up, a rise edge of gate signal can be transfered to the H-bridge when $V_{DC} = 0\,V$. In this



(a)



(b)

Figure 3.3: H-bridge based DPT (a) schematic of the circuit composed by a main board and an auxiliary board that utilised to control the initial I-type V_{ds} bias (b) switching waveforms of the conventional and modified DPT.

way, the T_H and T_L can be respectively locked to on and off state before starting the test, and the H-bridge DPT will operate same as the conventional DPT.

The corresponding switching waveforms of modified and conventional DPT through this H-bridge are depicted in Fig. 3.3(b), clearly showing the variation of the initial V_{ds} bias before starting the test and the consistency of the subsequent waveforms. To be noted that the DPT with and without the initial I-type V_{ds} bias are respectively named as biased and unbiased DPT in the following of this work.

By implementing the H-bridge based DPT, the initial I-type V_{ds} bias in the conventional DPT can be controlled, moreover, the influence of the I-type V_{ds} on the switching behaviour of GaN-HEMTs can be evaluated.

3.2 Switching behaviour analysis considering the V_{th} shift

In this section, the influence of V_{th} shift on the switching behaviour of Schottky-type GaN-HEMTs will be theoretically analysed. It should be noted that the theoretical analysis is mainly based on our previous work in [132]. A simple model of the switching cell as displayed in Fig. 3.4 is utilised to analyse the typical hard-switching transition. The switching voltage and current are respectively represented by V_{DC} and I_0. The low-side transistor is modelled by a voltage-controlled current source I_{ch} and three inter-electrode capacitances drain-to-source capacitance (C_{ds}), C_{gd} and C_{gs}, similarly, the freewheeling diode is modeled by a voltage-controlled current source I_{ak} with a junction capacitor C_j in parallel. The gate driver is modeled by an adjustable voltage source controlling the transistor through the gate resistor R_g, where the on and off gate voltages are named as V_g^{on} and V_g^{off} respectively. To be noted that the parasitic capacitances of the diode and transistor are considered linear in this section, and the parasitic inductances from the power loop (L_d), gate loop (L_g) and shared by these two loops (common-source inductance L_s) are neglected to simplify the switching analysis.

Two conditions, based on the presence of the Miller plateau, will be primarily discussed, corresponding to slow and ultra-fast switching commutation of GaN-HEMTs, respectively. Afterward, the expected influence of V_{th} shift phenomenon on the switching behaviour will be analysed in a more general condition.

3.2.1 Slow switching condition with Miller plateau

Based on the switching cell and the hypotheses presented in Fig. 3.4, the typical slowed down turn-on and turn-off switching waveforms of the low-side power transistor are respectively displayed in Fig. 3.5(a) and (b), where the Miller plateau is clearly presented with the V_{pl}^{on} and V_{pl}^{off} respectively at turn-on and turn-off. Since the commutation mostly occurs in the current saturation region of the output characteristics of the transistor, the switching behaviour can be conveniently analysed in the $I_{ch} - V_{gs}$ plane. This plane represents the transfer characteristics under high V_{ds} saturation region as depicted in Fig. 3.5(c). In this plane, the operation point of the device moves along the device $I - V$ characteristics, which corresponds to the commutation process of the transistor.

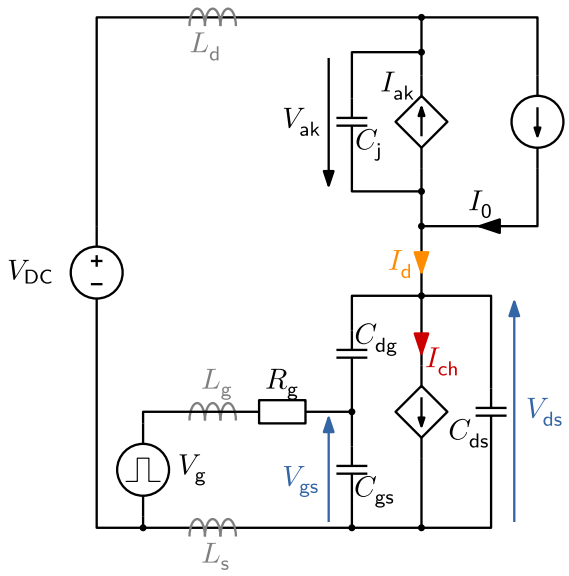


Figure 3.4: Schematic of the switching cell for hard-switching transition analysis.

- **At turn-on:** the current transition starts with the rising of V_{gs} (exceeding V_{th}) until the (V_{gs}, I_{ch}) operating point reaches point A (V_0, I_0). This process corresponds to the switching waveform in time domain from t_1^{on} to t_2^{on} in Fig. 3.5(a). Afterward, the diode is in reverse bias (zero I_{ak}) and V_{gs} reaches the plateau voltage (V_{pl}) between t_2^{on} and t_3^{on}, corresponding to point B in Fig. 3.5(c), where V_{ds} drops due to the $I_{ch} > I_0$ resulting in the discharging of the transistor's output capacitance $(C_{ds} + C_{dg})$ and charging of the diode's junction capacitance C_j. Finally, the device conducts with low V_{ds} and the transfer characteristic is no longer relevant to the switching commutation.

- **At turn-off:** the voltage transition starts around point A when $I_{ch} < I_0$, therefore, the output capacitance of the low-side transistor gets charged. Afterward, the plateau voltage V_{pl}^{off} is reached at point C, corresponding to the switching process from t_1^{off} to t_2^{off} in Fig. 3.5(b). Once the diode becomes conducting at t_2^{off}, the current of the transistor drops to zero with decreasing V_{gs}.

The current transition can be obviously linked to the transfer characteristics according to the basic model:

$$I_{ch} = g_m(V_{gs} - V_{th}) \quad , \quad V_{gs} > V_{th} \tag{3.2}$$

The voltage transition, however, requires more analysis focusing on the plateau voltage. At the Miller plateau, constant V_{gs} implies that V_{dg} and V_{ds} have the same time derivatives, such that:

$$\frac{V_g - V_{gs}}{R_g} = -C_{dg}\frac{dV_{ds}}{dt} \tag{3.3}$$

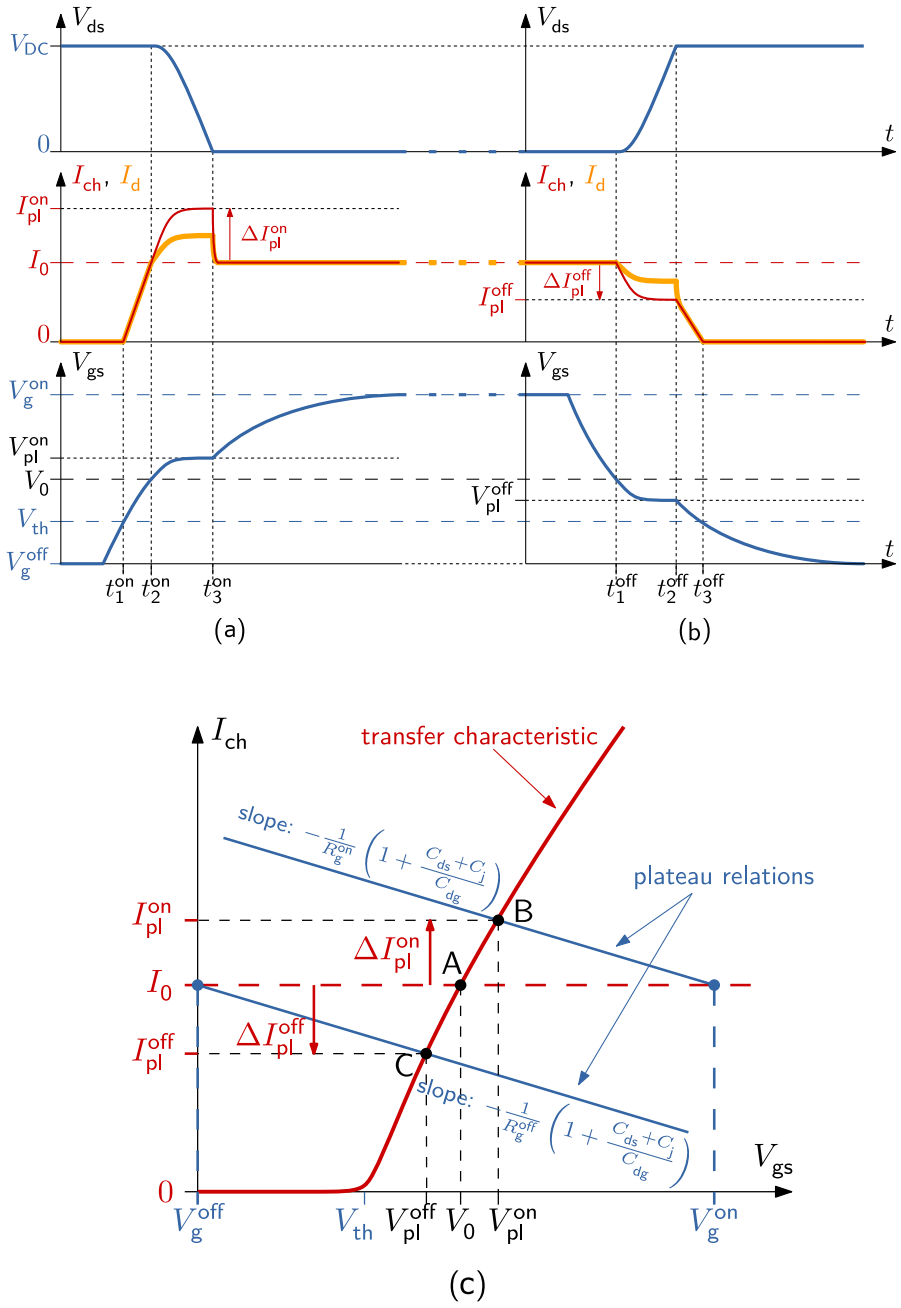


Figure 3.5: Simplified hard-switching transition from the switching cell in slow commutation condition (a) turn-on switching waveform (b) turn-off switching waveform (c) transfer characteristics with the Miller plateau relation.

In addition, voltage variations are linked to the charge or discharge of the output capacitances ($C_{dg} + C_{ds}$) by $I_{ch} - I_d$, where I_d is the drain current:

$$\frac{dV_{ds}}{dt} = \frac{I_d - I_{ch}}{C_{dg} + C_{ds}} \tag{3.4}$$

Since the power loop parasitic inductances (L_d and L_s) are omitted, V_{ds} and V_{ak} also have the same time derivatives, which yields:

$$I_d = I_0 - C_j \frac{dV_{ak}}{dt} = I_0 - C_j \frac{dV_{ds}}{dt} \tag{3.5}$$

Combining eqs. (3.3) to (3.5), an equation linking the I_{ch} and V_{gs} during the Miller plateau is obtained:

$$I_{ch} = I_0 - \frac{V_{gs} - V_g}{R_g}\left(1 + \frac{C_{ds} + C_j}{C_{dg}}\right) \tag{3.6}$$

This "Miller plateau relation" is plotted as straight lines in Fig. 3.5(c), passing through points (V_g^{on}, I_0) at turn-on (respectively, (V_g^{off}, I_0) at turn-off) with a negative slope that depends on the gate resistance (R_g^{on} or R_g^{off} respectively, if different) and inter-electrode capacitances of the power devices. To be noted that C_j equals $C_{ds} + C_{dg}$, if an identical GaN-HEMT with reverse-conducting is used as the diode. Therefore, the operating points at the Miller plateau (point B (V_{pl}^{on}, I_{pl}^{on}) at turn-on and C ($V_{pl}^{off}, I_{pl}^{off}$) at turn-off) are obtained at the intersections of the Miller plateau relations with the transfer characteristics.

Furthermore, the difference ΔI_{ch} between channel and load currents is a key parameter for the voltage transition speed since (3.4) and (3.5) yield:

$$\frac{dV_{ds}}{dt} = \frac{I_0 - I_{ch}}{C_{dg} + C_{ds} + C_j} = \frac{-\Delta I_{ch}}{C_{dg} + C_{ds} + C_j} \tag{3.7}$$

Its value at points B and C is represented in Fig. 3.5(c) as ΔI_{pl}^{on} and ΔI_{pl}^{off}, respectively. Calculating the intersection of the plateau relation line with the transfer characteristics using eq. (3.2), the voltage transition at the plateau can then be expressed as a function of V_{th}:

$$-\frac{dV_{ds}}{dt} = \frac{g_m(V_g - V_{th}) - I_0}{g_m R_g C_{dg} + C_{ds} + C_{dg} + C_j} = f(V_{th}) \tag{3.8}$$

This equation shows how the V_{th} shift phenomenon can influence the voltage transition in the slow-switching condition. Interestingly, it can be easily verified that turn-on transition gets slower due to negative df/dV_{th}.

Finally, the drain current can be related to the channel current from eqs. (3.5) and (3.7) by:

$$\frac{I_d - I_0}{\Delta I_{ch}} = \frac{C_j}{C_{dg} + C_{ds} + C_j} \tag{3.9}$$

which equals 1/2 if the diode is adopted by an identical GaN-HEMT (still considering the linear inter-electrode capacitances). For this reason, the curve of I_d in Fig. 3.5(a) and (b) has half of the deviation of I_{ch} to I_0 during the voltage transitions.

To summarise, in the slow switching with Miller plateau, the voltage transition speed can be reduced by a positive shift of V_{th} and vice versa.

3.2.2 Fast switching condition without Miller plateau

The above analysis should be completed by considering the ultra-fast commutation speed of the GaN-HEMTs that the Miller plateau voltage may not have enough time to be attained [133]. This effect can be displayed on the $I_{ch} - V_{gs}$ plane in Fig. 3.5(c), where the slopes of the Miller plateau relation lines increase when a high C_{ds}/C_{dg} ratio of device and a small value of R_g are used. In this fast switching condition, the crossing points between the Miller plateau relation lines with the transfer characteristics will move away as shown in Fig. 3.6(a).

- **At turn-on:** both current and voltage transitions are similar to those in previous slow switching condition, except that the "target" ΔI_{pl}^{on} is now much larger at point B. Consequently, as I_{ch} keeps increasing much beyond point A, the V_{ds} voltage falls more and more rapidly and eventually reaches its final on-state value before the pseudo steady state is reached. Thus, point B is not fully attained and the waveforms in Fig. 3.6(b) do not have time to be stabilised in the time interval $[t_2^{on}, t_3^{on}]$ (The dotted lines after t_3^{on} show how they would have stabilised otherwise).

- **At turn-off:** the switching transition is more impacted by the new slopes in Fig. 3.6(a), because the intersection of the Miller plateau relation line and the transfer characteristics is now at point D with zero channel current. Should the transconductance curve remain straight below V_{th} gate voltage, extending to negative I_{ch}, then the "target" pseudo steady state for the voltage transition would be at point C with a large negative ΔI_{pl}^{off}. For the corresponding switching waveform, the channel current will rapidly drop to zero when voltage transition starts as shown in Fig. 3.6(c). Thus, current transition is already finished in the channel at time t_2^{off} in Fig. 3.6(c) (The dotted lines after t_2^{off} show how V_{gs} and I_{ch} would have stabilised if current could become negative at point C). However, t_2^{off} is only the beginning of the voltage transition: afterwards drain voltage rises up to V_{DC} in the $[t_2^{off}, t_3^{off}]$ interval, under $\Delta I_{ch} = -I_0$ in eq. (3.7). Thus, the drain current alone is merely charging the output capacitance of the transistor, resulting in a turn-off voltage rising speed that only depends on the load current I_0. Similar behaviour has been reported for various transistor technologies [74], [134], usually associated with the switching transition in low current. It suggests that V_{th} shift phenomenon would not influence the turn-off commutation once the channel stops conducting in the fast switching condition.

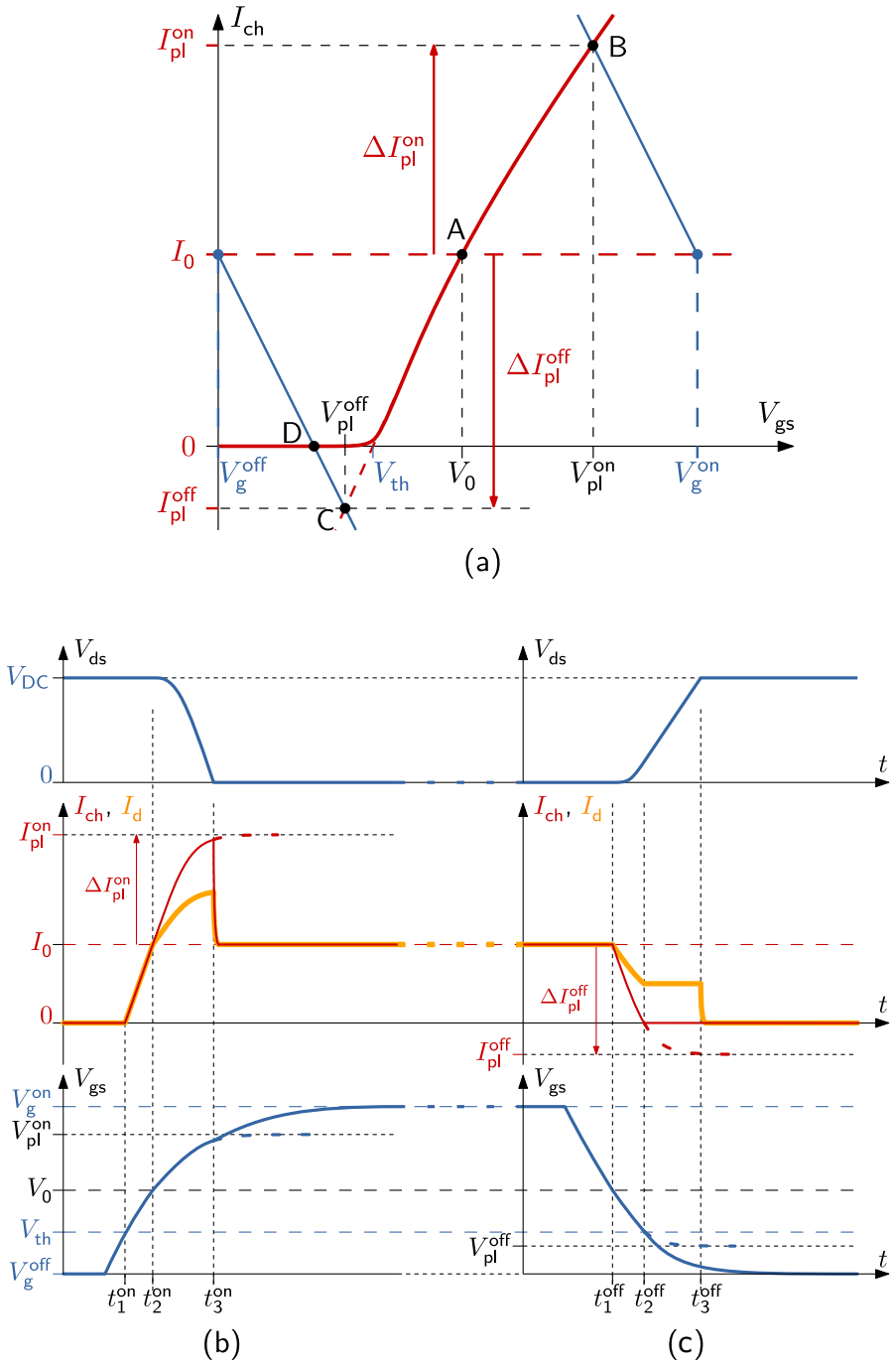


Figure 3.6: Simplified hard-switching from the switching cell in fast commutation condition (a) turn-on switching waveform (b) turn-off switching waveform (c) transfer characteristics with the Miller plateau relation.

To summarise, in the fast switching without Miller plateau, the turn-off switching transition may be not influenced by the V_{th} shift due to the channel current could drop to zero at the beginning of V_{ds} transition, especially in a low current switching.

3.2.3 Influence of V_{th} shift on the switching behaviour for Schottky-type GaN-HEMTs

The analysis in Fig. 3.6 can be combined with the result of I-type V_{ds} bias induced positive V_{th} shift observed in Section 2.2 to investigate its impact on the switching behaviour. It should be noted that the Schottky-type GaN-HEMTs are mainly focused on this chapter due to the pronounced positive V_{th} shift and voltage-driven characteristics[1]. Fig. 3.7 presents simple piecewise linear transfer characteristics defined by the V_{th} and g_m of the device according to eq. (3.2). Depending on if the transfer characteristics are influenced by the I-type V_{ds} bias, corresponding to the two test conditions in the H-bridge based DPT, two curves are considered:

- **Unbiased** represents that the GaN-HEMT is not subjected to the initial I-type V_{ds} bias in the H-bridge based DPT. The corresponding transfer characteristics (solid line in Fig. 3.7) would be obtained when the device has zero initial V_{ds} bias. Thus, the corresponding threshold voltage are identified with a "0" superscript: V_{th}^{0}.
- **Biased** represents that the GaN-HEMT incurred initial I-type V_{ds} bias induced positive V_{th} shift, by the V_{DC} before t_0 in the conventional mode DPT. The corresponding curve (dashed line in Fig. 3.7) is determined by V_{th}^{E}, including the E bias superscript indication.

In addition, the Miller plateau relation lines are also plotted, similar to the fast switching condition in Fig. 3.6(a), and the crossing points A^0, B^0, C^0 for the unbiased curve and A^E, B^E, C^E for the biased case are defined.

The parameters used for Fig. 3.7 are based on the device GS66502B (650 V/7.5 A) from GaN Systems, where the unbiased V_{th}^{0} is approximated by the transfer characteristics from datasheet, while the biased V_{th}^{E} is set in Table 3.1, with considering the positive shifted V_{th} value from our measurements and supported by literature [35], [85], [95], [96], [98], [105]. Also, the Table 3.1 provides the on/off gate voltages, switched current, gate resistance (identical for both on and off states), and device capacitance values approximated from the datasheet at a 200 V drain voltage, which are used to plot the Miller plateau relation lines.

- **At turn-on:** the current transition could be slowed in biased condition since the rising span of V_{gs} from $(V_{th}^{E}, 0)$ to point A^E is much closer to its final value V_g^{on} than that in the unbiased condition, as displayed in Fig. 3.7. To be noted, this V_{gs}

[1]The negative V_{th} shift of GITs under the I-type V_{ds} bias is not significant, but more importantly, the GITs are current-driven devices, where a specific RC circuit is recommended in the gate loop, leading to different commutation analysis compared to above theoretical analysis. This regime will be discussed later in this chapter.

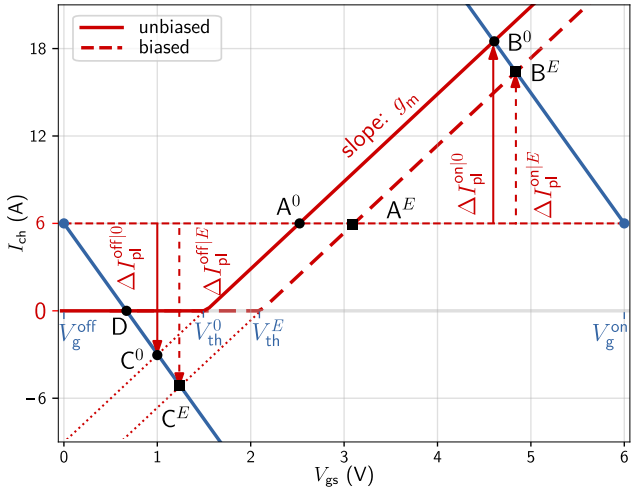


Figure 3.7: Transfer characteristics in unbiased and biased modes considering Miller plateau relation.

$V_{th}^0 = 1.5\,V$	$V_g^{on} = 6\,V$	$I_0 = 6\,A$	$R_g = 15\,\Omega$	$C_j = 20.3\,pF$
$V_{th}^E = 2.1\,V$	$V_g^{off} = 0\,V$	$g_m = 6\,S$	$C_{dg} = 0.3\,pF$	$C_{ds} = 20\,pF$

Table 3.1: Parameter values for plotting Fig. 3.7.

rising span is in charge of the current transition of the transistor, which means the current rising stage in the biased condition will take a longer time due to the RC charging characteristics of the V_{gs} (the charging of C_{gs} through R_g is an RC process). Afterwards, the voltage transition can be linked to ΔI_{ch} as mentioned in eq. (3.7). Fig. 3.7 reveals that the "target" values in biased ($\Delta I_{pl}^{on|E}$) and unbiased ($\Delta I_{pl}^{on|0}$) conditions are different, as the transfer characteristics are shifted by the V_{th}. Therefore, ΔI_{ch} rises slower in biased state (from A^E towards B^E) than in unbiased one (from A^0 towards B^0), resulting in a slower voltage transition as well, due to the eq. (3.7).

- **At turn-off:** as mentioned in section 3.2.2, the voltage transition is primarily associated with a fast current transition of I_{ch} that reaches zero rapidly when the operating point moves from point A towards point C in Fig. 3.7, bifurcating at $(V_{th}, 0)$ towards point D. Consequently, the turn-off transition can be much less influenced by the V_{th} shift as it was at turn-on, because it is obviously that C^0 and C^E in Fig. 3.7 cannot be reached in ultra-fast switching as they are non-physical. Afterwards, V_{ds} voltage keeps rising since the drain current is charging the output capacitance of the transistor, as discussed in Fig. 3.6(c). Since the turn-off transition is then independent on the transfer characteristics, it might be concluded that the V_{th} shift does not influence the turn-off switching transition,

especially in a fast switching with a relative low load current.

However, if the turn-off switching transition happens with a relative high load current or slow commutation speed, the V_{th} shift could influence the switching behaviour as the C^0 and C^E would be reached in the first quadrant of $I_{ch} - V_{gs}$ plane. Specifically, the current transition in biased mode should be faster than the unbiased one, because of the closer V_{gs} span to V_g^{on} and the RC discharging characteristics of V_{gs}. Also, the voltage transition in biased mode would be faster as well, due to the larger $\Delta I_{pl}^{off|E}$ and eq. (3.7).

Overall, the I-type V_{ds} bias induced positive V_{th} shift could slow down the turn-on switching commutation speed by decreasing the dV_{ds}/dt and dI_d/dt, while the turn-off switching transition may not be influenced by the V_{th} shift, especially in the fast switching with low load current. This will be verified in section 3.5.3, but additional analysis is provided beforehand. Moreover, the device V_{th} is also dependent on the II-type V_{ds} bias in hard-switching. Therefore, only the transfer characteristics under high V_{ds} saturation region can be used to predict the hard-switching transition, as the switching commutation mainly occurs in high V_{ds} saturation region.

To verify the influence of these two types of V_{ds} bias induced V_{th} shift on the switching behaviour of GaN-HEMTs, a method to obtain and model the transfer characteristics under different high V_{ds} is required.

3.3 High-voltage and high-current output characteristics

To demonstrate the influence of V_{th} shift on the switching behaviour of GaN-HEMTs as analysed in the last section, a simulation method is preferred initially, since the influence of extra parameters can be excluded, such as the $C - V$ characteristics. Therefore, it is necessary to construct a device model including the V_{th} shift phenomenon for the simulation. For this reason, the high-voltage and high-current (HVHC) output characteristics considering the V_{th} shift phenomenon will be introduced and characterised, this $I - V$ characteristics being further modeled and imported to a simulation program with integrated circuit emphasis (SPICE) model to demonstrate the influence of V_{th} shift on the switching behaviour of GaN-HEMTs. Additionally, the influence of other factors, such as the circuit parasitic parameters and V_{gs} bias induced V_{th} shift, on the measured HVHC $I - V$ characteristics will be evaluated.

3.3.1 Introduction of the HVHC output characteristics

A V_{th} shift extraction method based on the switching waveform from DPT will be discussed in this section. As shown in Fig. 3.1, there are various voltage biases in the DPT that could influence the switching behaviour of GaN-HEMTs by the V_{th} shift, based on this assumption, the switching waveform from DPT could include information about the V_{th} shift as well. Therefore, it is possible to investigate the V_{th} shift phenomenon

through analysing the switching waveform of the DPT, and by controlling different voltage biases.

The V_{th} extraction method through the switching waveform can be achieved by constructing the HVHC output characteristics, where the V_{th} is included in this $I-V$ characteristics.

As implied by the name, the HVHC output characteristics exhibit a high V_{ds} saturation region and a high I_d region, reaching the rated voltage and current levels, therefore, providing more switching related information than the typical $I-V$ output characteristics. For example, some mechanisms occur only under high V_{ds} voltage, such as the trapping effect or the GDCBL effect [73], [97] that can be included in the HVHC output characteristics. In other words, the II-type V_{ds} bias induced V_{th} shift can be included in the HVHC output characteristics. The V_{ds} saturation region in the typical output characteristics is only limited to several volts [115], related to the power limitations of the semiconductor curve tracer. However, output characteristics measured under such a low V_{ds} range may not accurately reflect the actual I-V characteristics when the power GaN-HEMTs operate at several hundred volts. As supported by the previous switching behaviour analysis, in Fig. 3.5(a), the switching commutation primarily happens under high V_{ds} saturation region and the transfer characteristics in Fig. 3.5(c) refer to the $I_d - V_{gs}$ relation under high V_{ds} saturation region as well. Consequently, it is necessary to utilise the HVHC output characteristics when predicting the switching behaviour of GaN-HEMTs.

The HVHC output characteristics measurement method through the switching waveform of DPT are reported in [135], [136] for the SiC-MOSFETs, where a large gate resistor R_g is used to slowdown the turn-on switching waveform of the DUT to improve the measurement accuracy, and the corresponding V_{ds} and I_d are measured when the V_{gs} reaches the Miller plateau voltage V_{pl}. By repeating the test with different V_{DC} and load currents, the relation between V_{ds} and I_d at different V_{gs} (V_{ds} and I_d are measured when $V_{gs} = V_{pl}$) can be obtained. To be noted that the V_{pl} under different V_{DC} is different because of the short channel effect of SiC-MOSFETs, which mechanism differs from the mechanism in power GaN-HEMTs [73]. Nevertheless, a large gate resistor is still proposed to use to facilitate data acquisition through slowed turn-on commutation. However, a new interpolation method is proposed to obtain the HVHC output characteristics, requiring fewer experimental scenarios than the method in [135], [136]. Additionally, considering the coexistence of two types of V_{ds} biases in GaN-HEMTs, a new DPT experimental configuration is necessary as discussed blow.

3.3.2 Proposed measurement method for the HVHC output characteristics

The switching waveform from conventional DPT is not suitable for constructing the HVHC output characteristics for GaN-HEMTs, since both I- and II-type V_{ds} bias induced V_{th} shift could be included in the HVHC output characteristics. To evaluate the influence of V_{th} shift phenomenon on the switching behaviour, these two types of V_{ds} bias induced V_{th} shift should be decoupled, therefore, the H-bridge based DPT in Fig. 3.3 can be adopted to decouple the V_{th} shift induced by these two types of V_{ds} bias.

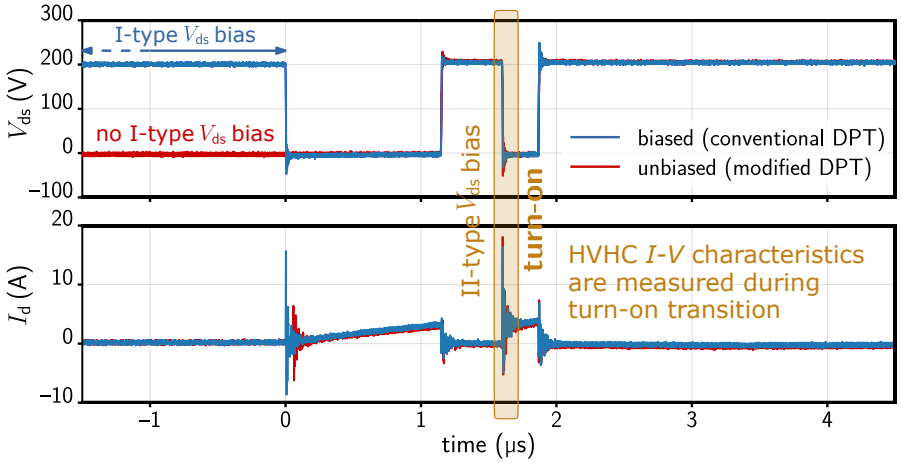


Figure 3.8: HVHC output characteristics extraction through the turn-on switching waveforms form the H-bridge based DPT.

As shown in Fig. 3.8, the HVHC output characteristics of GaN-HEMTs can be extracted from both biased and unbiased turn-on switching waveforms, allowing for the comparison of HVHC output characteristics with and without the influence of I-type V_{ds} bias. To be noted that the II-type V_{ds} bias induced V_{th} is always included in the HVHC output characteristics as it is extracted from the switching waveform with V_{ds}.

3.3.2.1 Experiment setup

The H-bridge based DPT discussed in Fig. 3.3 is implemented to control the influence of the initial I-type V_{ds} bias, where the H-bridge experimental board is displayed in Fig. 3.9. The main board is primarily used to implement the DPT and measure the typical switching waveform, while the auxiliary board is used to control the initial I-type V_{ds} bias. The DC+ and DC- connectors from these two boards are respectively connected together to compose the H-bridge, and the inductor load is connected in between of these two middle point connectors. The same gate signal is used to control these two boards for synchronisation, as discussed in Fig. 3.3(a). The GS66502B (650 V/7.5 A) is adopted as the power transistors (including the DUT) in this H-bridge. The V_{gs} is measured by a 500 MHz passive probe (P5050B) and the V_{ds} is measured by a 200 MHz high voltage differential probe (THDP0200). To reduce the measurement noise for current, a 120 MHz Hall effect probe (TCP0030A) is adopted to measure the I_d compared to the current shunt. In this work, a new HVHC output characteristics measurement method based on the turn-on switching waveforms is proposed [100]. In this method, a 1 kΩ turn-on gate resistor R_g^{on} is used to slow down the turn-on commutation speed.

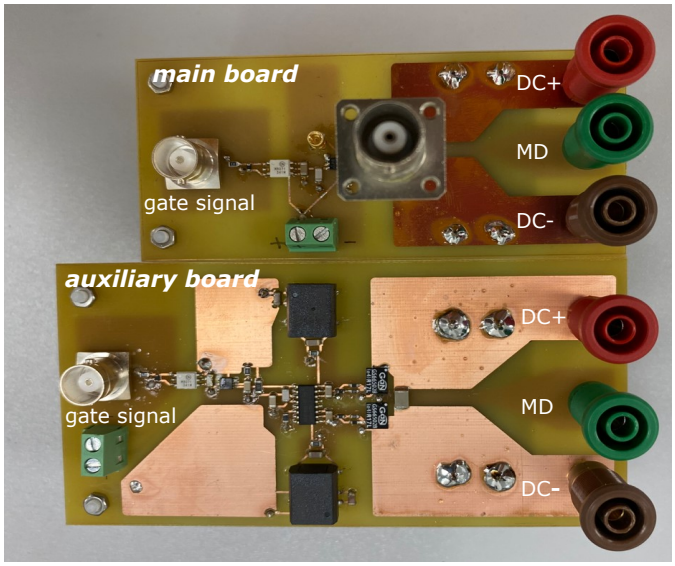


Figure 3.9: Experiment board for the H-bridge based DPT, where the main board is used to measure the typical switching waveforms of DPT and the auxiliary board is used to control the initial I-type V_{ds} bias.

3.3.2.2 Measurement result

In the experiment, the V_{DC} is set to 200 V that limits the V_{ds} range of the HVHC output characteristics. Under 200 V of V_{DC}, different drain current I_d can be achieved by adjusting the time interval between t_0 and t_1 to control the increasing of load current as shown in Fig. 3.1. In this way, the turn-on switching waveforms at 200 V of V_{ds} and various I_d can be obtained, these switching waveforms can be further used to construct the HVHC output characteristics.

Fig. 3.10 represents how the HVHC output characteristics are extracted through a set of slowed down turn-on switching waveforms using the proposed method in this work. For example, a line representing $V_{gs} = 1.8\,V$ is used to interpolate the V_{gs} switching waveforms to get four intersections as shown in Fig. 3.10(a). The corresponding I_d and V_{ds} can be obtained and plotted in the $I_d - V_{ds}$ plane with the same V_{gs} as shown in Fig. 3.10(b). By repeating this interpolation over a range of V_{gs}, the full curve of the HVHC output characteristics can be obtained. From this process, it can be clearly observed that the influence of II-type V_{ds} bias is included in the HVHC output characteristics as the data points are extracted under different high V_{ds} biases as shown in Fig. 3.10(a). In other words, the HVHC output characteristics include the complete relationship between V_{gs}, V_{ds} and I_d during the switching commutation.

It should be noted that the 1 kΩ of R_g^{on} is used to slow down the turn-on switching transition, which is not a practical application case for GaN-HEMTs. The V_{th} characteristics of the device in this slowed hard-switching transient might be different with that in fast switching, due to the higher possibility of hot electrons trapping[56] or impact

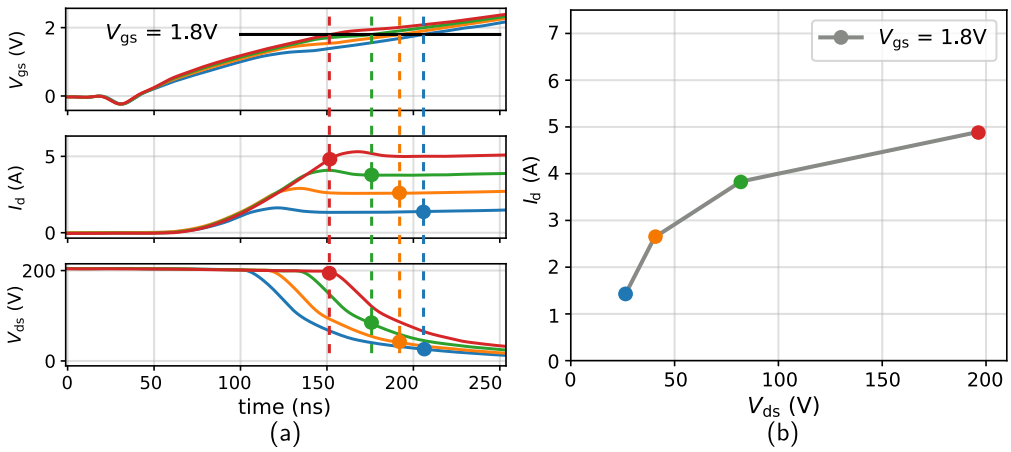


Figure 3.10: The extraction method for HVHC output characteristics using interpolating (a) a set of slowed turn-on switching waveforms with different I_d (b) extracted HVHC output characteristics when $V_{gs} = 1.8\,V$.

ionisation[83]. Moreover, the dynamic R_{on} phenomenon of the device might become serious due to this slowed down switching transient [56], [75], which could increase the conduction losses of the device. However, the objective of this work is to highlight the influence of different types of V_{ds} biases on the V_{th} and demonstrate the impact of V_{th} shift on switching behaviours. In fast switching, circuit parasitic inductance[135] and probe impedance[137] will all make it impossible to draw the conclusion if any difference observed, which will be investigated in future work.

3.3.3 Error analysis for the measured HVHC output characteristics

Even if a large R_g^{on} is used to slow down the turn-on switching commutation, the influence of the probe delay and circuit parasitic parameters on the constructed HVHC output characteristics should be evaluated. Moreover, the junction temperature T_j of the DUT during the switching commutation should be evaluated due to the extended overlap between V_{ds} and I_d by the large R_g^{on}. Additionally, the influence of different V_{gs} biases in the DPT on the measured HVHC output characteristics requires discussion.

3.3.3.1 Influence of probe propagation delay

Proper extraction of HVHC output characteristics in Fig. 3.10(b) requires accurate synchronisation of the oscilloscope-acquired signals. However, voltage and current probes involve propagation delays that are attributed to the different measurement and signal conversion techniques [137], [138], potentially disrupting the time alignment of the measured signals. Since the HVHC output characteristics are extracted through the turn-on switching transition, although slowed by the large R_g^{on}, the propagation delay induced by different probes could mislead the correct corresponding relation

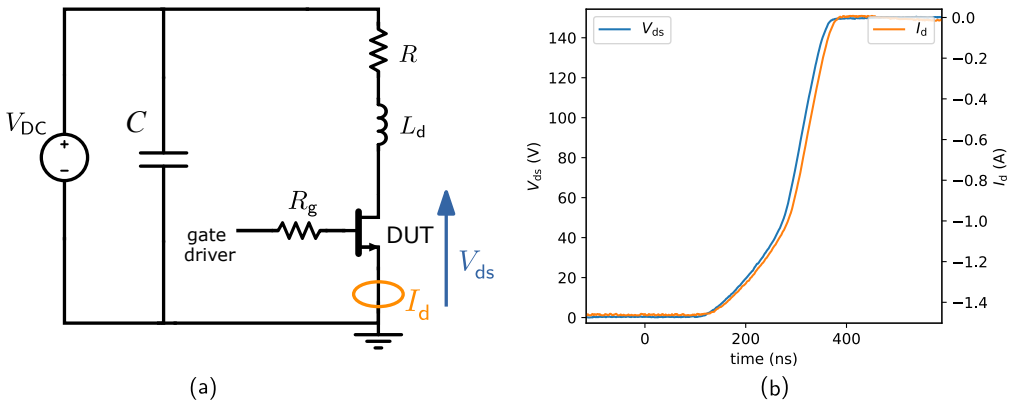


Figure 3.11: Power resistor based probe de-skew method (a) schematic modified on the half-bridge of DPT (b) measured V_{ds} and I_d for $I-V$ alignment.

of measured switching waveforms, further influencing the resulted HVHC output characteristics.

Several methods are reported to de-skew the probe delay, including the post processing method based on the known I-V relations [139], [140] and commercial test fixture based method [141]. In this work, a method similar to [118] is adopted. The schematic is shown in Fig. 3.11, where the high-side device in a half-bridge configuration is replaced by a power resistor. The DUT is controlled by a single pulse, and the V_{ds} and I_d in the turn-on commutation are measured as shown in Fig. 3.11(b). Due to the characteristics of the power resistor load, the switching waveforms of V_{ds} and I_d should be in phase. The time off-set between V_{ds} and I_d in Fig. 3.11(b) can be attributed to the probe delay. To be noted that a 1 kΩ R_g is used to slow down the commutation speed to emulate the DPT. Moreover, the influence of parasitic L_d can be reduced due to the slow commutation. Following these conditions, 30 nH of L_d can only induce approximately 278 ps of time off-set, by converting the rise time (t_r) to equivalent frequency using equation $t_r = 1/(f * \pi)$ [118], so that the L_d induced delay can be neglected. By using different probes to measure the V_{ds}, the relative delay of the probes can be derived.

The relative propagation delay between the used probes is displayed in Fig. 3.12. These delays will be de-skewed for the DPT results when constructing the HVHC output characteristics.

3.3.3.2 Influence of parasitic circuit parameters

The output characteristics represent the relationship between channel current I_{ch} and the voltage on the intrinsic gate-to-source capacitance V_{Cgs}, however, due to the existence of parasitic circuit parameters in the device package, such as parasitic inductance and resistance, these two signals cannot be directly measured with the probes. Fig. 3.13 shows the distribution of parasitic parameters inside the device package and the variation between measured V_{gs}, V_{ld} and I_{ch} and V_{Cgs}. Consequently, the influence of these parasitic parameters should be discussed and compensated to obtain the channel current

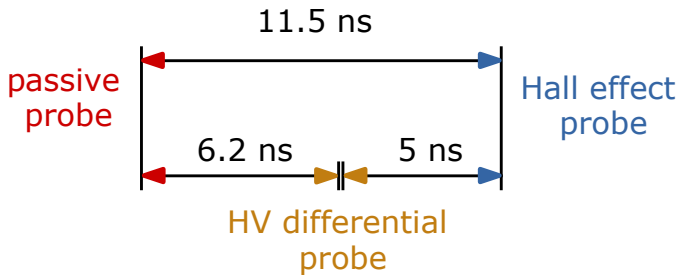


Figure 3.12: Relative propagation delay between the used probes for V_{gs}, V_{ds} and I_d measurement when $R_g = 1\,k\Omega$

I_{ch} and intrinsic V_{Cgs} for constructing the HVHC output characteristics, based on the following process.

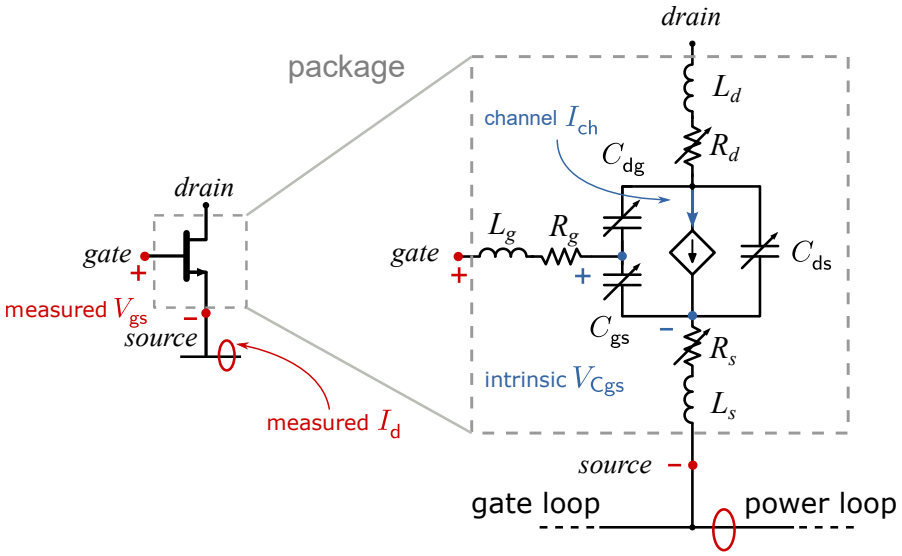


Figure 3.13: Schematic for the variation between the measured V_{gs}, I_d and intrinsic V_{Cgs} and I_{ch} of GaN-HEMTs due to the parasitic parameters in the device package.

During the turn-on transition, the output capacitance $C_{oss} = C_{gd} + C_{ds}$ of the GaN-HEMTs will discharge and the corresponding I_{Coss} current cannot be measured by the current probe but it contributes the variation between I_{ch} and I_d. Therefore, I_{Coss} should be calculated to compensate the measured I_d as eq. (3.10):

$$I_{ch} = I_d - I_{Coss} = I_d - C_{oss}\frac{dV_{ds}}{dt} \tag{3.10}$$

However, the C_{oss} of GaN-HEMTs is a non-linear capacitance, highly depending on the V_{ds} voltage. To calculate the I_{Coss} accurately, the model of C_{oss} for GS66502B reported

n	a_n	b_n	c_n	d_n	e_n	f_n	g_n	h_n	i_n	j_n
1	100^{-12}	60.85^{-12}	1.405	1.5	14.93^{-12}	0.9169	5	3.933^{-12}	0.07737	-35
2	103.5^{-12}	9.43^{-12}	0.030	-118.9	11.49^{-12}	0.7	-47.34	20^{-12}	0.06603	-51.22

Table 3.2: Parameters used in equation (3.11).

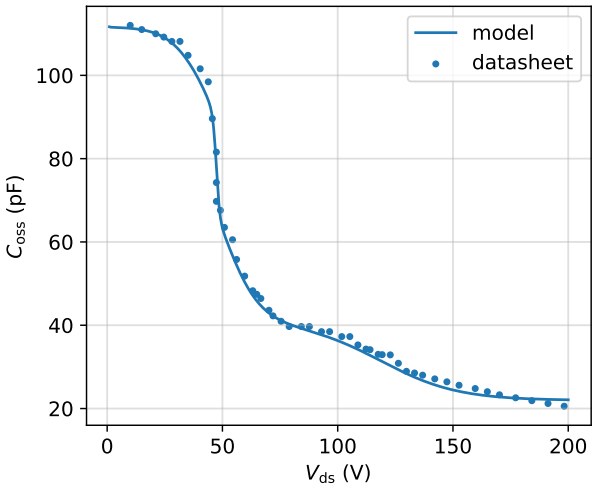


Figure 3.14: Comparison of the C_{oss} of GS66502B between model and datasheet

in [142], [143] is used, as shown in eq. (3.11):

$$C_{gd} = a_1 - b_1(1+\tanh(c_1(V_{gd}+d_1))) + e_1(1+\tanh(f_1(V_{gd}+g_1))) - h_1(1+\tanh(i_1(V_{gd}+j_1))) \tag{3.11a}$$

$$C_{ds} = a_2 - b_2(1+\tanh(c_2(V_{ds}+d_2))) - e_2(1+\tanh(f_2(V_{ds}+g_2))) - h_2(1+\tanh(i_2(V_{ds}+j_2))) \tag{3.11b}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{3.11c}$$

where the parameters used in eq. (3.11) are displayed in Table 3.2. To be noted that V_{gs} is assumed as zero when evaluating the relation between C_{oss} and V_{ds}. The comparison of C_{oss} between the model and datasheet is shown in Fig. 3.14.

As displayed in Fig. 3.13, the measured V_{gs} includes the voltage drop on the L_g, L_s, R_g and R_s, in addition to the intrinsic voltage on C_{gs}. To obtain the V_{Cgs}, the voltage drop induced by the parasitic parameters should be eliminated or compensated. By utilising a large R_g^{on}, the influence of parasitic inductance can be neglected, due to the low dI_d/dt and several hundred pico-henries of parasitic L_s [142]. As for the voltage drop on the internal R_g, it is dependent on the gate leakage current I_g during Miller plateau

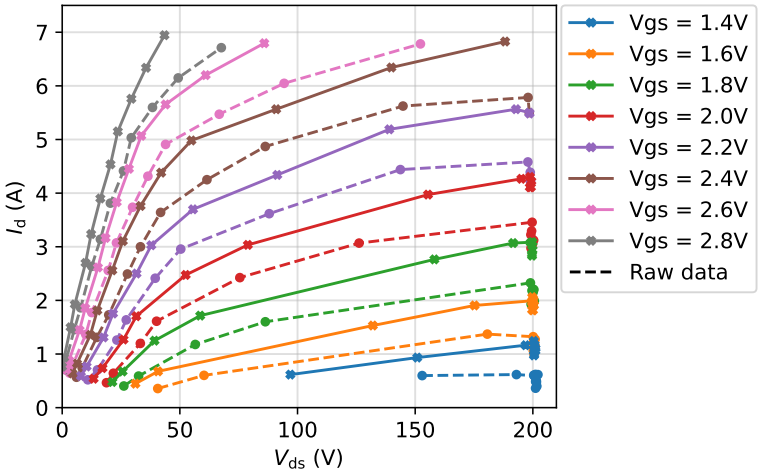


Figure 3.15: Comparison of HVHC output characteristics constructed from raw measured data from biased DPT (dashed curves) and those obtained after compensating for probe propagation delay and parasitic parameters (solid curves).

that can be calculated by eq. (3.12):

$$I_g = \frac{V_g - V_{pl}}{R_g^{on}} \tag{3.12}$$

where the gate voltage V_g and the Miller plateau voltage V_{pl} are respectively considered as 6 V and 1.5 V (based on measurement), and the R_g^{on} is 1 kΩ, resulting in I_g of approximately 4.5 mA. According to the manufacturer's device model, the internal R_g is 225 mΩ. Therefore, the voltage drop on the internal R_g is approximately 1 mV, this value can also be neglected. Hence, the difference between measured V_{gs} and intrinsic V_{Cgs} is mainly dependent on the voltage drop on R_s and can be compensated based on equation eq. (3.13):

$$V_{Cgs} = V_{gs} - I_d R_s \tag{3.13}$$

where R_s is considered to be constant (14.3 mΩ) due to the extreme low temperature sensitivity with 0.1 mΩ/K based on the measurement result described in [142]. Consequently, the error caused by the circuit's parasitic parameters is evaluated and compensated.

The measured HVHC output characteristics with and without the compensation of probe propagation delay and parasitic parameters are compared in Fig. 3.15, where the variation caused by these two factors can be clearly observed.

3.3.3.3 Influence of junction temperature

During the DPT, the junction temperature T_j of the DUT should be evaluated in the turn-on transition since the commutation time is extended by the large R_g^{on}, as shown

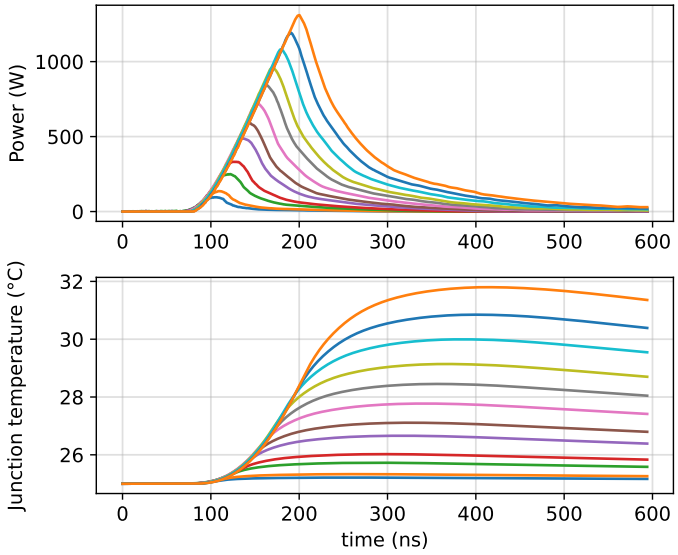


Figure 3.16: Power and estimated T_j during the turn-on transition for the HVHC output characteristics construction.

in Fig. 3.10(a). An RC thermal model of GS66502B, provided by the datasheet [115], is adopted to estimate the T_j during the turn-on transition. The power waveform of the DUT calculated by using the measured V_{ds} and I_d of is imported to the RC thermal model to obtain the transient T_j. Fig. 3.16 shows the turn-on power waveforms at different I_d and the corresponding T_J. The maximum T_j is less than 32 °C, when assuming the ambient temperature is 25 °C. It should be noted that the increasing of T_J value in other stages of the DUT sequence can be neglected, except for the turn-on transition [100].

Based on the waveforms of T_j in Fig. 3.16, the T_j at different time transients in the DPT can be determined, therefore, its corresponding value in the HVHC output characteristics can be obtained. The HVHC output characteristics extracted with the distribution of T_j through the biased DPT switching waveforms (corresponding to Fig. 3.16) is displayed on Fig. 3.17. It can be seen that the high temperature points are mainly distributed in the high current and middle voltage region, this region corresponding to the time period after the high V_{ds} and high I_d hard switching. However, since the maximum ΔT_j is less than 7 °C, the influence of T_j on the HVHC output characteristics can be neglected in this test.

3.3.3.4 Influence of various V_{gs} biases

It should be outlined that the HVHC output characteristics are extracted through a set of switching waveforms with different load current in the DPT, and different load current is achieved by adjusting different V_{gs} bias time. Therefore, the various V_{gs} bias may influence V_{th} of the HVHC output characteristics. In this test, the V_{gs} bias is adjusted from 150 ns to 2750 ns to increase the load current from around 0.5 A to 7 A.

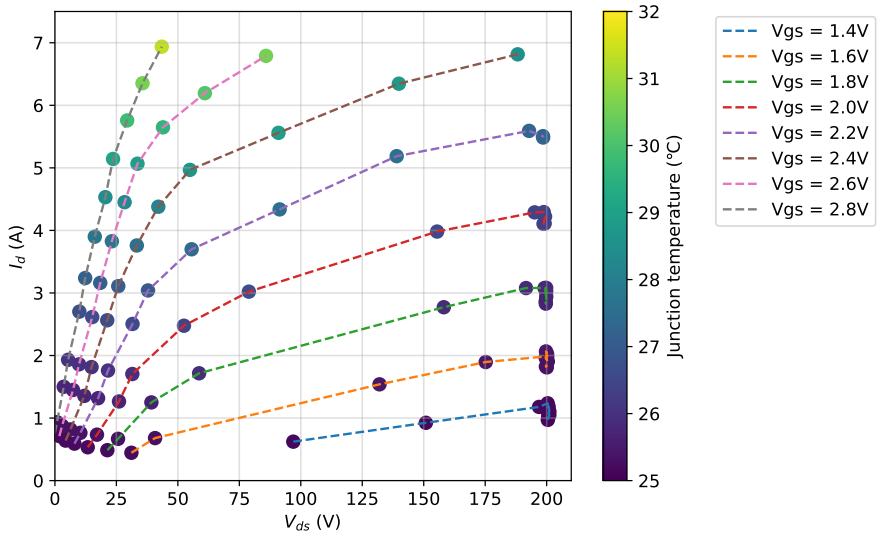


Figure 3.17: HVHC output characteristics extracted with the distribution of T_j through the biased DPT switching waveforms.

The turn-on switching waveforms of V_{gs} and I_d with these two V_{gs} bias time acting on the biased and unbiased DPT are respectively plotted to evaluate the influence of V_{gs} bias time on the V_{th} shift. To be noted that the influence of parasitic parameters are compensated, same as the HVHC output characteristics, to ensure that the I_d and V_{gs} can represent the channel current I_{ch} and intrinsic V_{cgs}. Fig. 3.18 shows the transfer characteristics plotted by the I_d and V_{gs}, with I_d in log scale to highlight the V_{th} variation. It can be seen that V_{gs} bias time has more notable influence on the unbiased test, with around 0.2 V of positive V_{th} shift from 150 ns to 2750 ns, while in the biased mode the V_{th} variation is less than 0.1 V. The small V_{th} shift in biased mode may indicate that the electron trapping in the gate stack is relatively saturated because of the long time initial off-state V_{ds} bias. Currently, the influence of V_{gs} bias time on the measured HVHC I-V characteristics cannot be fully eliminated, and addressing this issue requires a more complicated H-bridge DPT setup. Taking in account the relatively insignificant influence, especially in the biased mode, while the primary objective of the HVHC output characteristics is to demonstrate the influence of V_{th} shift on the switching behaviour of GaN-HEMTs, this V_{th} variation is considered acceptable in this study.

To summarise, the influence of the probe delay and parasitic circuit parameters on the HVHC output characteristics should be carefully considered, even when a large R_g^{on} is used to slow down the turn-on commutation speed. However, the T_j will not rise significantly in this test. The influence of various V_{gs} bias time on the V_{th} shift can be accepted, due to its relative small value (less than 0.2 V).

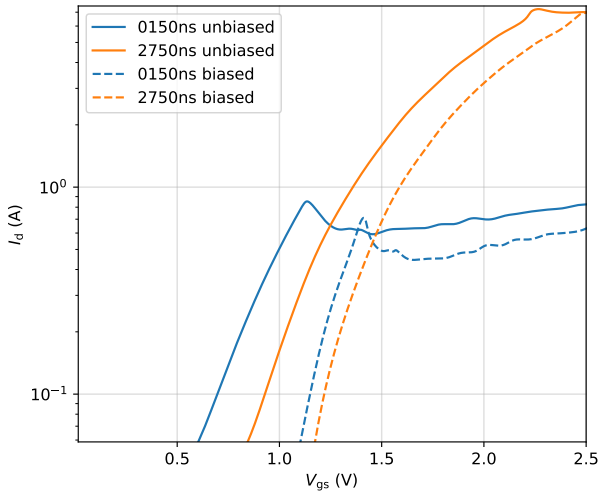


Figure 3.18: Influence of V_{gs} bias time on the extracted transfer characteristics.

3.3.4 V_{ds} bias induced V_{th} shift in the HVHC output characteristics

The HVHC output characteristics can be constructed by interpolating a set of slow turn-on switching waveforms from the DPT, including the II-type V_{ds} bias induced V_{th} shift. Therefore, depending on if the switching waveforms are from the biased DPT, the HVHC output characteristics with and without the influence of initial I-type V_{ds} bias can be obtained. In this test, one minute of initial I-type V_{ds} bias is applied in biased mode DPT to produce a saturated positive V_{th} shift [35], [99], [101], as the V_{ds} induced V_{th} instability is time dependent.

The HVHC output characteristics of GS66502B are shown in Fig. 3.19(a), where they are depicted as biased and unbiased HVHC output characteristics, represented by dashed and solid lines, respectively. The differentiation depends on whether the HVHC output characteristics are extracted from the switching waveforms of biased mode DPT. Moreover, to clearly show the V_{th} shift phenomenon, the transfer characteristics at different high V_{ds} can be obtained by interpolating at different V_{ds} values on the HVHC output characteristics as shown in Fig. 3.19(b). In this way, these two types of V_{ds} bias induced V_{th} shifts can be observed.

By comparing the solid and dashed curves in the transfer characteristics, the I-type V_{ds} bias induced positive V_{th} shift can be noted, where the approximately 0.5 V of ΔV_{th} is in the same order of magnitude as reported in [35], [99]. Moreover, all the transfer characteristics shift negatively with V_{ds} increasing from 50 V to 200 V, which could be related to the II-type V_{ds} bias during turn-on transient. The mechanism may be attributed to the elevated potential of p-GaN layer under high V_{ds} bias as discussed in [73], [97]. To be noted that this negative transfer characteristics shift is also reported for power SiC-MOSFETs [135], [144], but it is attributed to the drain induced barrier lowering (DIBL) effect for vertical power MOSFETs. For the lateral power GaN-HEMTs,

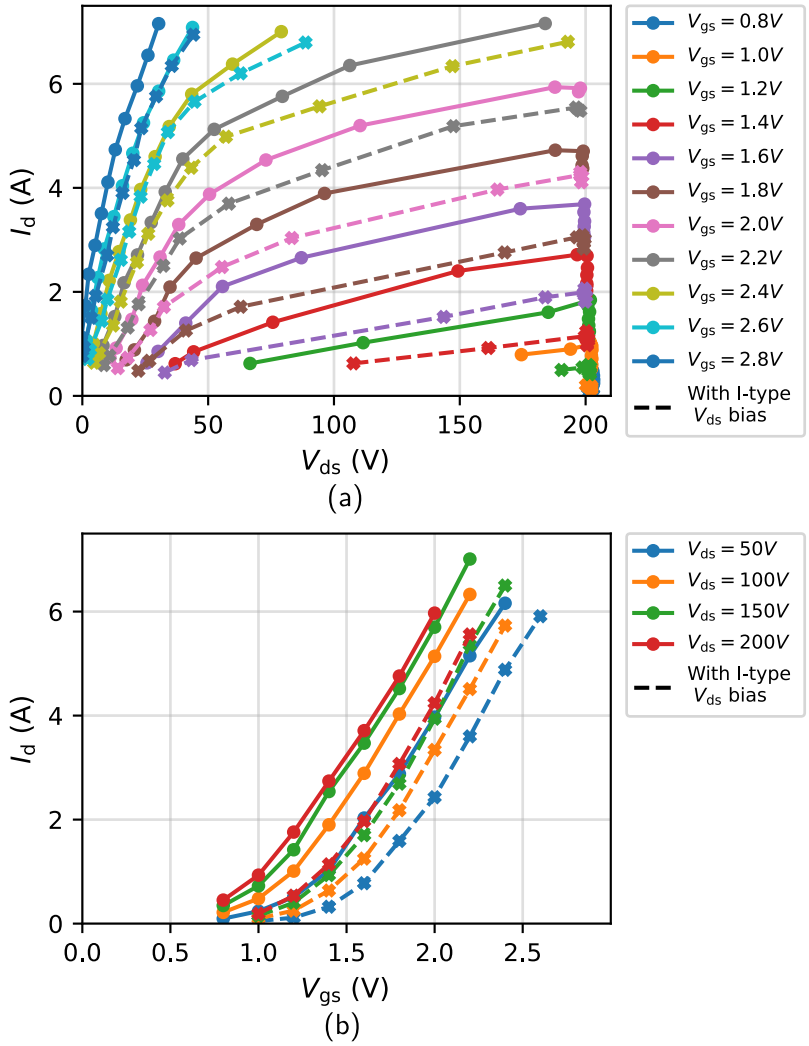


Figure 3.19: The HVHC I–V characteristics with (biased) and without (unbiased) the influence of I-type V_{ds} bias (a) output characteristics and (b) transfer characteristics under different V_{ds} (dynamic transfer characteristics). Here, the transfer characteristics are obtained by interpolating at different V_{ds} on the output characteristics. The I-type V_{ds} bias induced positive V_{th} shift can be obtained by comparing the dashed and solid curves. The II-type V_{ds} bias induced negative V_{th} shift are shown with V_{ds} increasing from 50 V to 200 V in both types of curves.

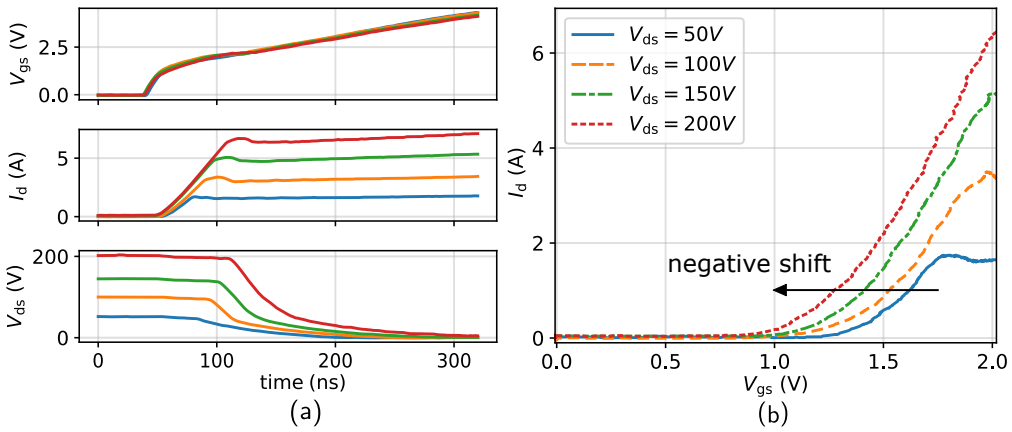


Figure 3.20: Measured (a) turn-on switching waveforms under different II-type V_{ds} bias from unbiased mode DPT and (b) negative V_{th} shift with the increase of II-type V_{ds} bias.

the DIBL effect is limited, due to the relative long length of gate-to-drain region [145], [146].

To further investigate this negative V_{th} shift, the unbiased DPT is implemented under different V_{DC}, where the influence of initial I-type V_{ds} bias is eliminated, and the turn-on time of DUT is set to 1 us to exclude the influence of varying V_{gs} bias time. The turn-on switching waveforms are shown in Fig. 3.20(a), where the I_d starts to rise earlier and faster under higher II-type V_{ds} bias, indicating the small V_{th} under high V_{ds} bias. Correspondingly, the transfer characteristics under different V_{ds} are plotted using the I_d and V_{gs} switching waveforms, as shown in Fig. 3.20(b). Approximately $-0.4\,\mathrm{V}$ of ΔV_{th} can be observed with V_{ds} increase from 50 V to 200 V, and this value is in agreement with the negative ΔV_{th} in Fig. 3.19(b). It should be noted that this II-type V_{ds} bias induced negative V_{th} can be easily overlooked by curve tracer based device characterisation methods, as the transfer characteristics are typically measured below 10 V of V_{ds}[115], [147], [148]. However, since the device normally operates under several hundred volts, neglecting this shift may impact the prediction of device switching behaviour.

The V_{th} shift phenomenon induced by the two types of V_{ds} bias are characterised using the above discussed method. To be noted that both the biased and unbiased HVHC output characteristics in Fig. 3.19(a) include II-type V_{ds} bias induced negative V_{th}, since they both consider the complete relation between V_{ds}, V_{gs} and I_d during high voltage hard-switching. While only the biased HVHC output characteristics include the I-type V_{ds} bias induced positive V_{th} shift, these biased and unbiased HVHC output characteristics can be further modeled to validate the impact of V_{th} shift on the switching behaviour of GaN-HEMTs.

3.3.5 Evaluation of the V_{gs} bias induced V_{th} shift

The influence of V_{gs} bias on the measured HVHC output characteristics was analysed and subsequently neglected in the previous section. However, the H-bridge based DPT

setup provides a new method to evaluate the V_{gs} bias induced V_{th} shift, where the impact of V_{gs} bias duration is directly reflected in the switching waveforms of GaN-HEMTs within this configuration.

3.3.5.1 Measurement principle

The H-bridge based DPT can not only characterise the V_{ds} bias induced V_{th} shift but also evaluate the V_{gs} bias induced V_{th} shift. As mentioned in Fig. 3.1(b), the positive V_{gs} bias during the on-state of the DUT contributes to the V_{th} value during the turn-on transition, consequently, the influence of V_{gs} bias on the V_{th} shift can be evaluated by adjusting the V_{gs} bias time. Thanks to the H-bridge based DPT, the influence of initial V_{ds} bias on the V_{th} shift can be eliminated when solely investigating the influence of V_{gs} bias.

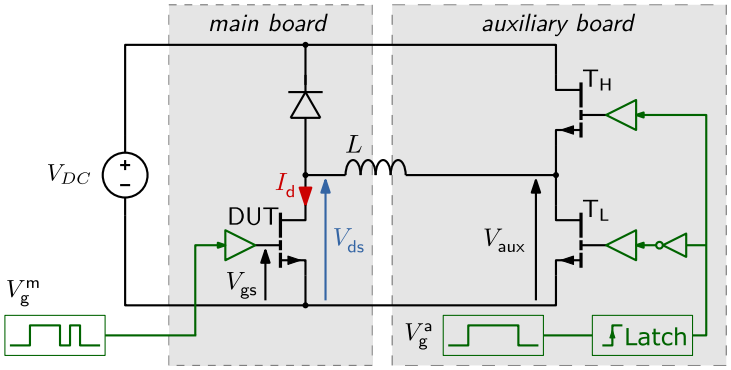
To adjust the V_{gs} bias time of DUT while maintaining the same load current, the H-bridge based DPT should be controlled separately by two gate signals. The schematic and the control sequence are displayed in Fig. 3.21, where the main board is controlled by a double pulse signal V_g^m and the auxiliary board is controlled by a single pulse signal V_g^a. Initially, both of the T_H and DUT are in off-state, and the initial I-type V_{ds} bias of DUT is eliminated as discussed above. The load current would increase only when both T_H and DUT are in on-state, requiring both V_g^m and V_g^a are in high level as the highlighted time interval $[t_1, t_2]$ in Fig. 3.21. Consequently, the extra positive V_{gs} bias time can be obtained by extending the width of first pulse of V_g^m when the V_g^a is in low level. The V_{th} can be extracted from the slowed down turn-on switching waveforms as depicted in Fig. 3.20.

3.3.5.2 Measurement result

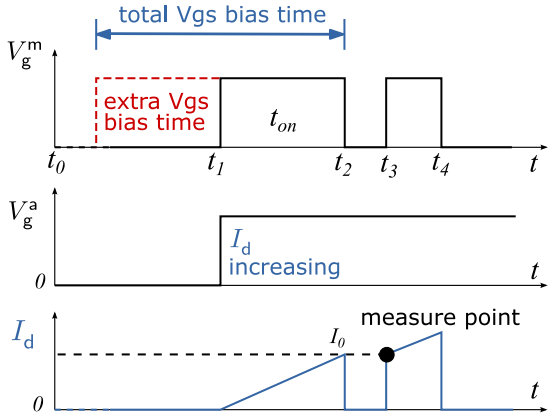
Based on the measurement principle discussed above, the influence of extra V_{gs} bias time from 1 µs to 300 s is evaluated. The measurement is implemented when $V_{DC} = 200\,\text{V}$, $L = 80\,\mu\text{H}$ and the current rising time $t_{on} = 2\,\mu\text{s}$, and the load current is 5 A as resulted from eq. 3.14.

$$\Delta I = \frac{V_{DC} \cdot \Delta t}{L} \tag{3.14}$$

The transfer characteristics based on the turn-on switching waveforms with different extra V_{gs} bias time are displayed in Fig. 3.22(a), where the V_{gs} bias amplitude is set for 6 V as recommended by the datasheet. The compensation of the probe propagation delay and the influence of parasitic parameters are addressed as discussed in section 3.3.3. To further evaluate the relation between V_{gs} bias time and the V_{th} value, V_{th} when $I_d = 10\,\text{mA}$ is extracted and plotted in Fig. 3.22(b). V_{th} represents a strong non-linear shift behaviour with the increasing of V_{gs} bias time, where V_{th} increases along with the extending of V_{gs} bias time before 100 µs. Afterward, the V_{th} starts to decrease and gets close to saturation value. This V_{gs} bias induced V_{th} shift trend is also reported in literature [88]. The positive V_{th} shift after the short time V_{gs} bias can be attributed to the hole-deficiency mechanisms [64], [65], [86], while the negative V_{th} shift after a long time



(a)



(b)

Figure 3.21: Schematic of the (a) circuit and (b) control sequence of the H-bridge based DPT to investigate the influence of V_{gs} bias time on the V_{th} shift.

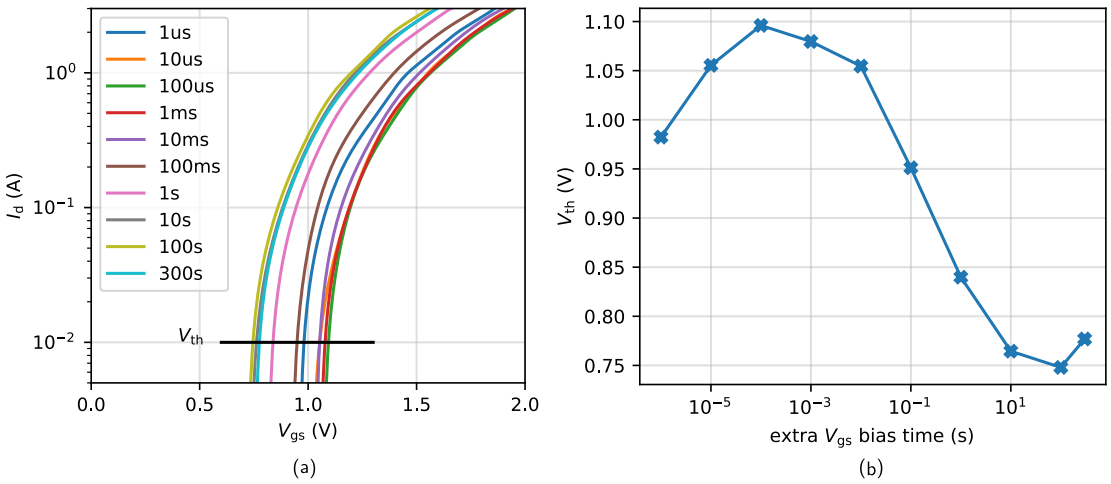


Figure 3.22: Measurement result of V_{gs} bias induced V_{th} shift using the H-bridge based DPT at V_{DC} = 200 V(a) transfer characteristics extracted from the turn-on switching waveforms (b) extra V_{gs} bias time versus V_{th}.

of V_{gs} bias could be related to the hole-injection mechanisms [64], [90], as respectively discussed in the mechanisms (1)(2) and (3)(4) in section 1.3.3.2.

It should be noted that the measured V_{th} could differ from the original V_{th} of the device, even though the V_{gs} bias time is short enough, because there are other voltage biases that could influence the V_{th}. To be specific, the different voltage biases during the V_{th} shift evaluation in Fig. 3.21(a) are depicted in Fig. 3.23, where the V_{th} is extracted during t_3 under the II-type V_{ds} bias. Before the measurement, the I-type V_{ds} bias also present, even if it remains in 500 ns interval from t_2 to t_3 and constant during the test. However, this short V_{ds} bias may not induce notable V_{th} shift as discussed in section 2.2.

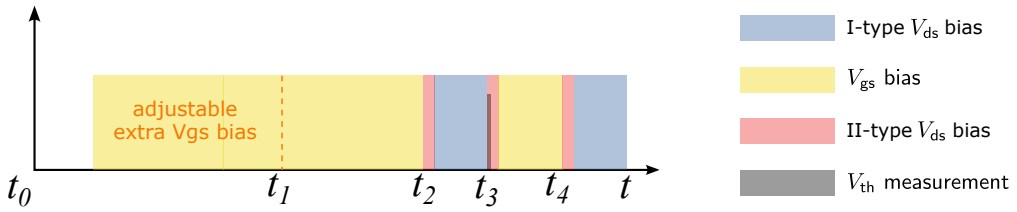


Figure 3.23: Different voltage biases during the V_{gs} bias induced V_{th} evaluation using the H-bridge based DPT.

The influence of V_{gs} bias time on the V_{th} shift under different II-type V_{ds} biases are also investigated using the same method as presented in Fig. 3.22. To maintain the same load current, a different load inductor L is adopted for various V_{DC} as shown in Table 3.3. The extra V_{gs} bias time increases from 1 µs to 300 s as displayed in Fig. 3.24, where the V_{th} is extracted at I_d = 10 mA. Under different V_{DC}, the relation between the V_{gs} bias time and the V_{th} shift remains unchanged, however, they have a negative off-set with the

V_{DC}	t_{on}	L
200 V	2 µs	80 µH
100 V	2 µs	40 µH
50 V	2 µs	20 µH

Table 3.3: Experiment parameters used in Fig. 3.24.

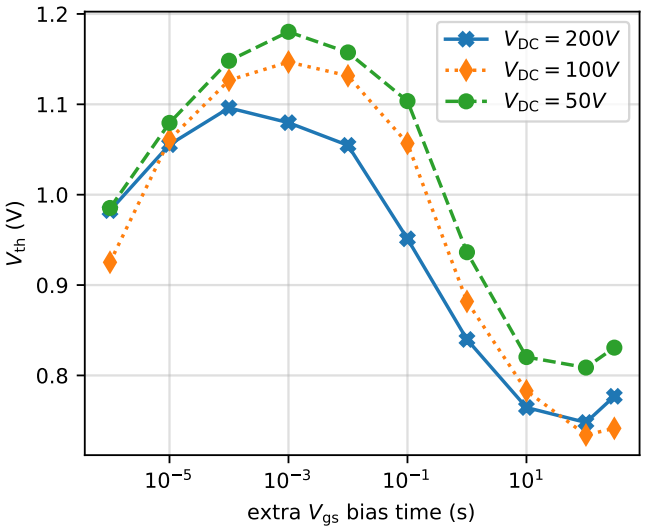


Figure 3.24: Measurement result of V_{th} shift induced by different V_{gs} bias time (from 1 µs to 300 s) under different V_{DC}.

increasing of V_{DC}. This negative off-set can be attributed to the II-type V_{ds} bias induced negative V_{th} shift as discussed in Fig. 3.20.

Thanks to the H-bridge based DPT, some voltage biases can be controlled to investigate the influence of V_{ds} or V_{gs} on the V_{th} shift of GaN-HEMTs, although they cannot be completely eliminated. More importantly, the influence of voltage bias induced V_{th} shift on the actual switching transition can be directly obtained in the DPT. To the best of the author's knowledge, this work is among the first to consider different trapping effect-related biases in the DPT, as shown in Fig. 3.23. Furthermore, the measured V_{th} shift indicates that each stress type could impact the final switching waveforms of the GaN-HEMTs. However, some parameters cannot be fully eliminated experimentally. To further demonstrate the influence of V_{th} shift on the switching behaviour, the simulation method will be employed in the next section.

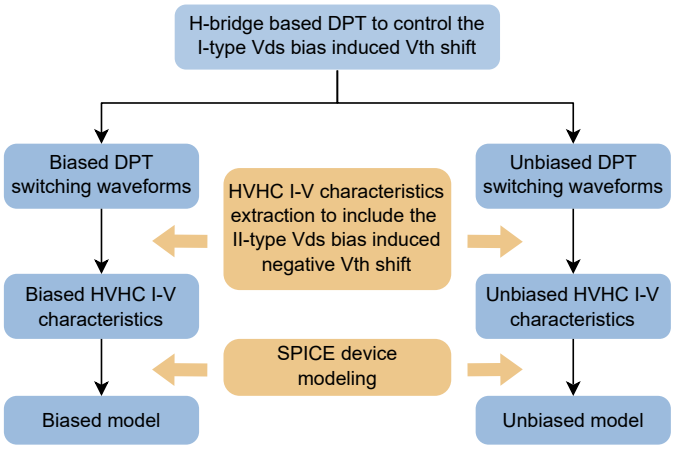


Figure 3.25: Modelling process of the SPICE models and the inclusion relationship of each model to different V_{ds} bias induced V_{th} shift.

3.4 SPICE device modelling considering V_{ds} bias induced V_{th} shift

The measured HVHC output characteristics will be modelled and then imported to the SPICE models to evaluate the influence of V_{th} shift on the switching behaviour of GaN-HEMTs. Initially, it is necessary to clarify the modelling process and the V_{th} shifts induced by different V_{ds} biases in each model. As displayed in Fig. 3.25, two SPICE models with and without the influence of initial I-type V_{ds} bias induced V_{th} shift will be proposed and the influence on the switching behaviour can be evaluated by comparing the simulation results of these two models. Additionally, since the II-type V_{ds} bias induced negative V_{th} shift is included in the HVHC output characteristics, its impact on switching behaviour can be evaluated by comparing against the manufacturer model.

3.4.1 Modelling of HVHC output characteristics

Behaviour models considering the obtained HVHC output characteristics are constructed in this subsection. In the conventional behaviour modelling, empirical equations are adopted to fit measured $I-V$ characteristics as reported in [135], [149], [150]. However, it is time-consuming and complicated to propose appropriate equations and search a global solution for tens of optimised parameters using the non-linear regression methods. More importantly, most of the output characteristics models proposed for HEMTs and MOSFETs assumes I_d becoming saturated after V_{ds} above 5 V or 10 V [115], [148], like for the manufacturer model [115], the relative low saturation V_{ds} means that these models are not compatible with the inclusion of the II-type V_{ds} bias induced V_{th} shift. Considering that the power transistors mainly operate under several hundred volts of V_{ds} and that switching occurs in high V_{ds} region, the models of output characteristics with low V_{ds} saturation may not be suitable to predict device switching behaviour.

model	a	b	c	d	e	f	g	h	i	j
biased	-3.722	-0.141	3.244	-9.241	-0.561	2.576	-1.730^{-3}	-0.221	0.456	0.078
unbiased	2.427	0.133	9.130	-7.523	-0.516	2.706	0.025	0.144	-0.623	-0.019

Table 3.4: Parameters used in equation 3.15 for biased and unbiased Angelov model.

Therefore, proposed modelling in this work considers full V_{ds} range based on acquired data presented in Section 3.3.4.

3.4.1.1 Curve fitting based modelling method

Some $I-V$ characteristics models compatible to the high V_{ds} saturation region (the dynamic transfer characteristics as shown in Fig. 3.19(b)) are proposed in [135], [144], [151], [152] for WBG devices. In this work, the adapted Angelov equations for $I-V$ characteristics proposed in [152] are utilised to fit the measured HVHC $I-V$ characteristics and the derived models are named as Angelov models, as shown in eq. 3.15:

$$I_{ch} = (a - 25 \cdot b) \cdot (1 + g \cdot V_{ds}) \cdot (I_{ch1} + I_{ch2}) \tag{3.15a}$$

$$I_{ch1} = \ln(1 + \exp(c \cdot V_{gs} - (d - 25 \cdot e)))^f \tag{3.15b}$$

$$I_{ch2} = -\ln(1 + \exp(c \cdot V_{gs} - (d - 25 \cdot e) - h \cdot (V_{ds})^i \cdot \tanh(j \cdot V_{ds})))^f \tag{3.15c}$$

A conventional optimisation method using the "SLSQP" algorithm is employed to fit the HVHC $I-V$ characteristics for obtaining the biased and unbiased models. The comparison of the fitted model and the measured HVHC output characteristics is depicted in Fig. 3.26, where the Angelov model exhibits a good compatibility with high saturated V_{ds}, allowing for a desirable fitting result for the HVHC $I-V$ characteristics. The fitted parameters for biased and unbiased models are listed in Table 3.4. To show the advantages of the high saturated V_{ds} model, the $I-V$ characteristics from the manufacturer model [115] are adopted to fit the biased HVHC $I-V$ characteristics using the same optimisation method and the results are depicted in Fig. 3.27, where the fitting result is impractical due to the low saturated V_{ds} of the model. However, the Angelov model also exhibits some undesirable fitting results, particularly in the high-current and high-voltage region under biased condition and the low-current and high-voltage region under unbiased condition. These undesirable fittings may influence the switching behaviour of the SPICE models when considering these HVHC $I-V$ characteristics, which will be discussed below.

3.4.1.2 Proposed neural network based modelling method

Artificial intelligence (AI) technology is developing rapidly in power electronics, and the AI's neural network counts as a strong ability for the non-linear behaviour modelling, therefore, a neural network based modelling method is proposed to improve the fitting

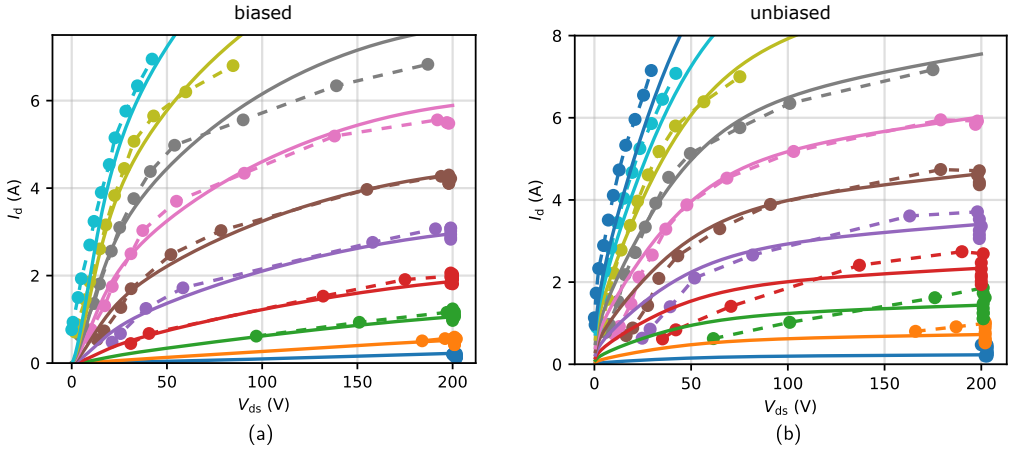


Figure 3.26: Comparison of measured HVHC output characteristics (dashed curves) and fitted Angelov model (solid curves) in (a) biased and (b) unbiased conditions.

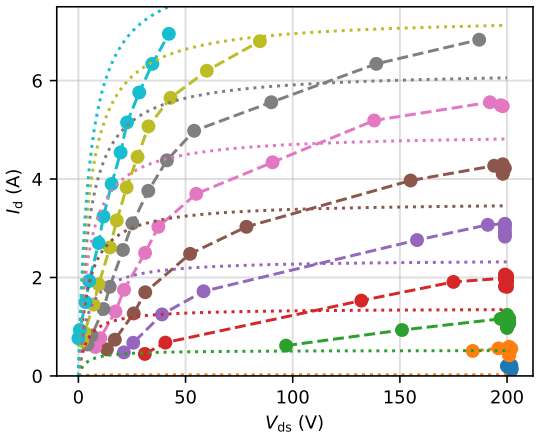


Figure 3.27: Comparison of the biased HVHC output characteristics (dashed curves) and fitted manufacturer model (dotted curves).

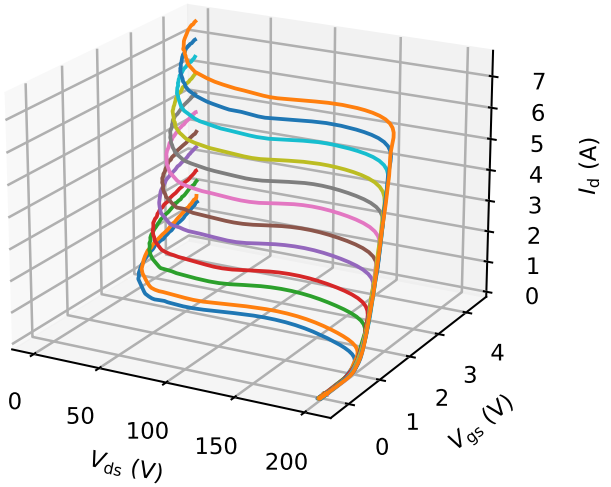


Figure 3.28: 3D switching trajectories of the slowed down turn-on commutation under 200 V of V_{DC} with 12 different width for the 1st DPT pulse form the biased DPT.

results of Angelov model. In this proposed method, the dedicated equations are not required and the fitting process is more convenient compared to the conventional optimisation based fitting method [136], [153].

Beneficial from the strong data-driven ability of neural network, the whole sets of measured turn-on switching waveforms for extracting the HVHC $I-V$ characteristics can be utilised for modelling. For example, the 3D switching trajectories extracted through the set of turn-on switching waveforms, including all the V_{gs}, V_{ds} and I_d information during turn-on transition as shown in Fig. 3.28, can be directly employed to train the neural network model.

A multilayer perceptron (MLP) neural network is adopted to model the HVHC $I-V$ characteristics due to the desirable ability of non-linear behaviour fitting. More importantly, the MLP neural network can be written as equations, which can be directly executed in the SPICE simulation environment. A 3-layer neural network with 2 neurons as the input layer (for V_{gs} and V_{ds} respectively), 6 neurons as the hidden layer, and 1 neuron as output layer (for I_d) is employed, considering the simplicity of the model in SPICE environment. The model is expressed as eq. 3.16:

$$I_d = \tanh(\mathbf{I} \times \mathbf{W_1}^T + \mathbf{B_1}^T) \times \mathbf{W_2} + b \tag{3.16}$$

where $\mathbf{I} = (V_{gs} \;\; V_{ds})$ is the input vector, $\mathbf{W_1}$, $\mathbf{B_1}$ and $\mathbf{W_2}$ are parameter matrices and b is a single bias parameter.

$$\mathbf{W_1^b} = \begin{pmatrix} -0.991 & -0.149 \\ 4.664 & -0.638 \\ -0.648 & -1.119 \\ -5.860 & -0.970 \\ -2.800 & 0.935 \\ -0.509 & -1.240 \end{pmatrix}, \mathbf{B_1^b} = \begin{pmatrix} 1.234 \\ -1.764 \\ 2.166 \\ 1.427 \\ -1.255 \\ 1.541 \end{pmatrix}, \mathbf{W_2^b} = \begin{pmatrix} -1.442 \\ 1.756 \\ -2.362 \\ -4.284 \\ 2.844 \\ 2.033 \end{pmatrix}, \mathrm{b^b} = -3.926 \tag{3.17}$$

$$\mathbf{W_1^u} = \begin{pmatrix} -1.121 & 0.164 \\ 1.255 & 0.229 \\ -0.861 & -1.013 \\ 0.524 & -1.257 \\ -0.820 & -1.195 \\ -0.833 & 0.669 \end{pmatrix}, \mathbf{B_1^u} = \begin{pmatrix} -0.117 \\ -1.413 \\ 1.919 \\ 0.401 \\ 1.320 \\ 1.407 \end{pmatrix}, \mathbf{W_2^u} = \begin{pmatrix} 0.163 \\ 1.259 \\ -1.670 \\ -0.889 \\ 1.417 \\ -0.939 \end{pmatrix}, \mathrm{b^u} = -0.460 \tag{3.18}$$

By feeding the data of the 3D switching trajectories from biased and unbiased DPT to the neural network, the biased and unbiased HVHC $I-V$ characteristics models can be obtained, these models are named as the neural network models in this work. Parameters of the biased and unbiased neural network models are shown in eq. 3.17 and eq. 3.18 respectively, where superscript "b" and "u" represent biased and unbiased respectively. The HVHC $I-V$ characteristics models constructed by neural network and Angelov equations are compared to the measurement results in Fig. 3.29. It can be seen that the neural network models show better fitting results compared to the Angelov model, especially in the high V_{ds} region. This fact can be attributed to the greater generalisation of neural network models. In other words, the neural network is a purely data-driven model, free from the behavioural limitations of the empirical equations in the conventional fitting methods. It should be noted that the neural network model can exhibit some incorrect points around the coordinate origin due to the insufficient constrains from its equations. The modification equations proposed in [136] are adopted to correct these points in this study, however, these points does not influence the analysed switching behaviour in HVHC region.

More importantly, the neural network based modelling represents a new method to obtain the HVHC $I-V$ characteristics, making unnecessary the interpolation method shown in Fig. 3.10. Broadly speaking, the neural network provides a tool to conveniently model the strong non-linear behaviour.

3.4.2 Construction of the device SPICE model

Considering the objective demonstrating the influence of the V_{th} shift on the switching behaviour of GaN-HEMTs, the SPICE model is employed due to its accurate prediction of switching behaviour and fast simulation speed. The SPICE model of the power transistor is basically composed by a voltage-controlled current source ($I-V$ characteristics), three

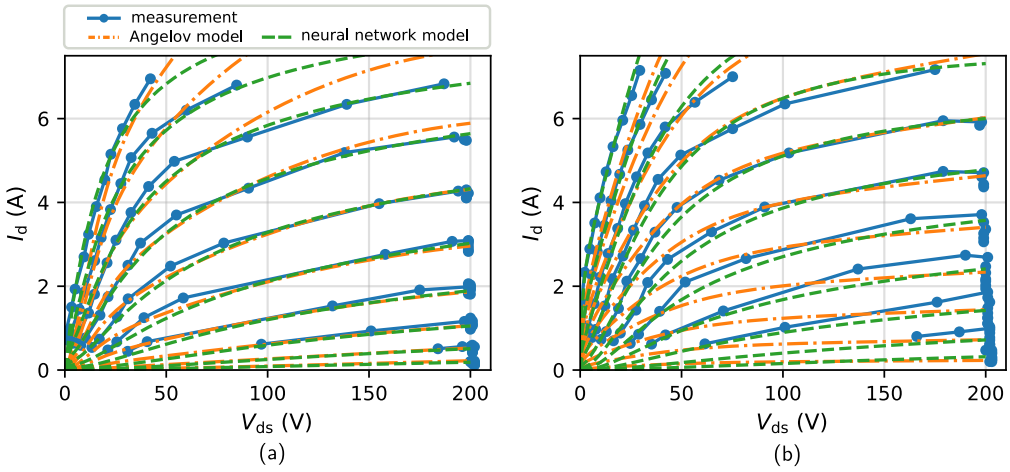


Figure 3.29: Comparison of HVHC $I-V$ characteristics between experiment measurement and constructed models (neural network and Angelov models) in (a) biased and (b) unbiased conditions.

non-linear capacitances ($C-V$ characteristics) and parasitic parameters as depicted in Fig. 3.13. The proposed SPICE models are modified based on the manufacturer's model of GS66502B [115], in which the original I–V characteristics equations are replaced by the constructed HVHC I–V characteristics models in Fig. 3.29. Other parts, such as the C–V characteristics and the parasitics parameters remain unchanged, to exclude the impact of these parameters. In this way, the variation in the switching behaviour of the models is solely dependent on the differences in their $I-V$ characteristics. This is the reason why SPICE models are adopted to demonstrate the influence of V_{th} shift on device switching behaviour, as it is challenging to decouple the influence of I–V and C–V characteristics in experiments. Moreover, the switching behaviour is also dependent on the device C–V characteristics, and the C–V characteristics could be also impacted by the V_{ds} bias induced trapping effect in GaN buffer layer [110].

Based on whether the HVHC $I-V$ characteristics are extracted from biased DPT, the SPICE models are classified into biased and unbiased models. Additionally, according to the modeling method of the $I-V$ characteristics, the obtained models are further divided into Angelov models and neural network models. The classification results in a total of four proposed SPICE models. Including the manufacturer model, they are summarised in Table 3.5 along with their inclusion of different V_{ds} biases.

3.5 Simulation and experiment validation

3.5.1 Model calibration in slow switching

All SPICE behaviour models are applied to the DPT simulation, with the same schematic as Fig. 3.1(a), to replace the freewheeling diode and DUT. Their turn-on simulation

models	I-type V_{ds} bias	II-type V_{ds} bias
Neural network biased model	✓	✓
Neural network unbiased model	✗	✓
Angelov biased model	✓	✓
Angelov unbiased model	✗	✓
Manufacturer model	✗	✗

Table 3.5: All SPICE models and their inclusion of different types of V_{ds} bias.

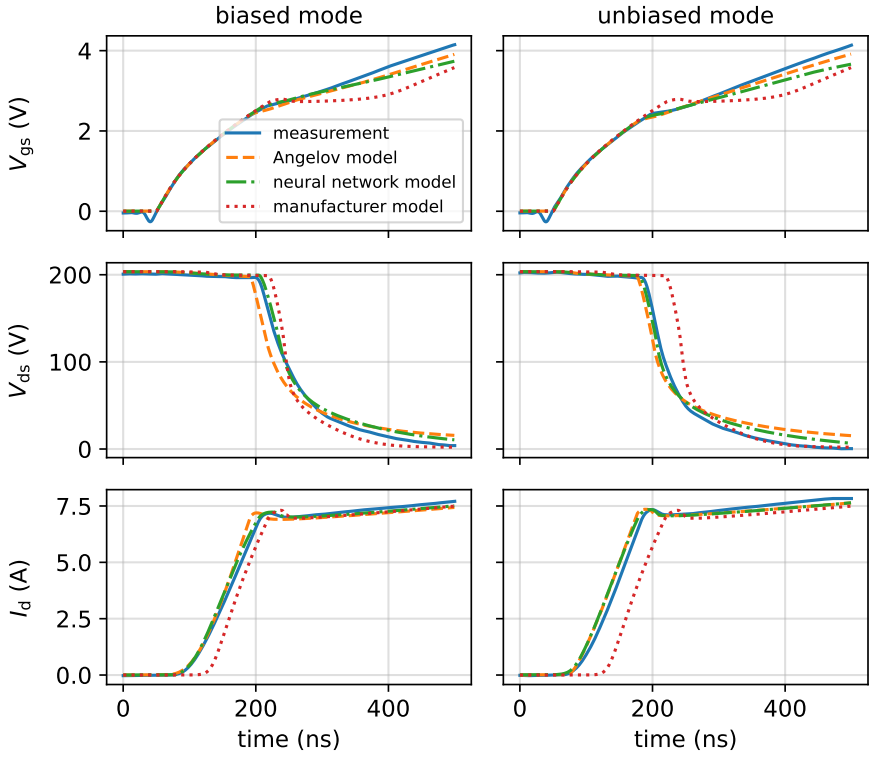


Figure 3.30: Comparison of turn-on switching waveforms (with 1 kΩ R_g^{on}) from biased and unbiased DPT with simulation results of biased and unbiased SPICE models.

Turn-on switching waveforms	dV_{ds}/dt (V/ns)	dI_d/dt (A/us)	E_{on} (uJ)
Measurement result biased	-1.40	63.64	142.88
Measurement result unbiased	-1.75	70.45	126.86
Neural network model biased	-1.24	65.02	159.71
Neural network model unbiased	-1.34	71.20	141.15
Angelov model biased	-1.15	73.54	139.36
Angelov model unbiased	-1.12	74.53	145.74
Manufacturer model	-2.38	78.65	114.49

Table 3.6: dV_{ds}/dt, dI_d/dt and switching losses during turn-on transition from measurement and model simulation results in Fig. 3.30.

waveforms are compared to the biased and unbiased DPT measurement results at $I_d = 7$ A, which are depicted in Fig. 3.30. The result of manufacturer model is compared as a reference. As shown in Fig. 3.30, the Miller plateau appears in V_{gs} waveforms as the large R_g^{on} is used, and it is tilted in the results of both measurement and simulation models that the HVHC $I - V$ characteristics are considered. This tilted Miller plateau could be attributed to the II-type V_{ds} bias induced negative V_{th} shift. Because transfer characteristics shift positively with V_{ds} decreasing as shown in Fig. 3.19(b), therefore, a higher V_{gs} is required to maintain the same I_d in V_{ds} dropping stage. This can also be observed from Fig. 3.5(c), where shifted transfer characteristics would pull point B farther to the right, increasing plateau voltage. By contrast, a flat Miller plateau is exhibited by the manufacturer model, as the transfer characteristics remain constant under different V_{ds} bias, meaning the II-type V_{ds} bias induced V_{th} shift is overlooked. This tilted Miller plateau is also observed in [144] for SiC-MOSFETs and in [95] for GaN-HEMTs. However, in Fig. 3.30, both neural network and Angelov model show slow voltage dropping speed when V_{ds} is under around 30 V, especially in unbiased models, which may be attributed to the undesirable fitting in low V_{ds} Ohmic region in HVHC I–V characteristics.

To quantify the influence of positive V_{th} shift on the switching behaviour of GaN-HEMTs, the dV_{ds}/dt, dI_d/dt and turn-on switching losses (E_{on}) of simulation and experiment waveforms in Fig. 3.30 are calculated in Table 3.6. By comparing experimental results, the absolute values of dV_{ds}/dt and dI_d/dt in biased mode are reduced, leading to 12.6 % higher switching losses, which is attributed to the I-type V_{ds} induced positive V_{th} shift and in accordance with the analysis in section 3.2.3. In simulation results, the neural network models can reproduce this trend, and the switching losses are increased 13.2 % from unbiased to biased model. However, the Angelov models could not show this phenomenon effectively, which could be ascribed to the undesirable fitting results in the high I_d and high V_{ds} region of HVHC I–V characteristics in Fig. 3.29(a). To further evaluate the performance of proposed models, the absolute difference of dV_{ds}/dt, dI_d/dt and

| Model–Measurement |	dV_{ds}/dt (V/ns)	dI_d/dt (A/us)	E_{on} (uJ)
Neural network model biased	0.16	1.38	16.83
Neural network model unbiased	0.41	0.75	14.29
Angelov model biased	0.25	9.90	3.52
Angelov model unbiased	0.63	4.08	18.88
Manufacture model biased	0.98	15.01	28.39
Manufacture model unbiased	0.63	8.20	12.37

Table 3.7: Comparison of the absolute difference of dV_{ds}/dt, dI_d/dt and E_{on} between models and measurement results in Table 3.6.

E_{on} between simulation and experiment results in Table 3.6 are compared in Table 3.7. The neural network models show the best agreement with measurement results in terms of dV_{ds}/dt and dI_d/dt. This also shows the potential advantage of neural network in non-linear fitting.

However, the preceding characterisation and model evaluation for Fig. 3.30 was with 1 kΩ of R_g, which does not reflect the actual use of GaN-HEMTs. Therefore, it is necessary to evaluate the influence of this V_{th} shift on the fast switching commutation.

3.5.2 Model prediction in fast switching

The neural network models are employed to further verify the impact of V_{th} shift on device switching waveforms in fast switching conditions. In the simulation, 20 Ω of R_g^{on} and 2 Ω of R_g^{off} are adopted, and 10 nH of L_g and 6 nH of L_d are considered, where these values are in the range of reported or recommanded values [111], [154]. The simulation waveforms of V_{ds}, I_d and I_{ch} are shown in Fig. 3.31. At turn-on, the absolute value of dV_{ds}/dt, dI_d/dt, and current overshoot towards ΔI_{pl}^{on} are larger in unbiased mode, as analysed in Fig. 3.7. At turn-off, the commutation waveforms are almost identical in these two models. This is because, in such a fast turn-off commutation with low load current, the I_{ch} drops to zero when V_{ds} starts to increase, meaning the current transition is finished in the channel, afterward, the V_{ds} increasing process is independent of transfer characteristics. These results verify the hypothesis proposed in section 3.2.3 that I-type of V_{ds} induced positive V_{th} shift can slow down the turn-on commutation speed, while the turn-off process is not affected due to the I_{ch} drops to zero quickly.

To evaluate the impact of II-type V_{ds} bias induced negative V_{th} shift on switching waveforms, the unbiased neural network model is utilised for DPT simulation at different V_{DC}, and the manufacturer model is used as a reference. To clearly show the impact, the parasitic inductances are neglected. The simulation results are depicted in Fig. 3.32. At turn-on, the I_d rises earlier and faster under higher V_{ds} bias, due to the negatively shifted transfer characteristics induced by the higher II-type V_{ds} bias. This trend is also observed in the measured turn-on switching waveforms in Fig. 3.20(a). By contrast, the

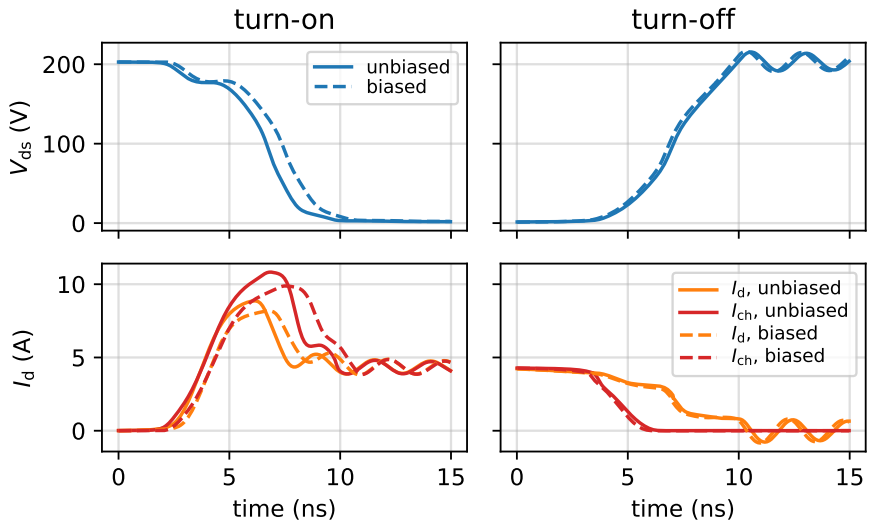


Figure 3.31: Comparison of turn-on and turn-off simulation switching waveforms of biased and unbiased neural network models. In turn-on transient, the $^{dV_{ds}}/_{dt}$, $^{dI_d}/_{dt}$ and current overshoot of biased model are decreased.

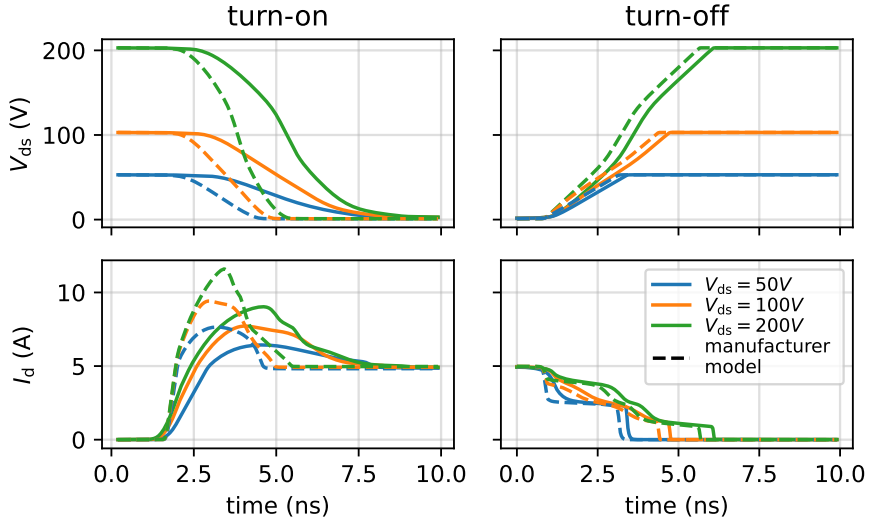


Figure 3.32: Turn-on and turn-off simulation waveforms at different V_{ds} from unbiased neural network model. In turn-on transient, $^{dI_d}/_{dt}$ and current overshoot of neural-network model are increased with V_{ds} voltage increasing.

waveform of rising I_d from manufacturer model remains unchanged at different V_{ds} bias, due to its constant transfer characteristics. At turn-off, the I_d commutation speed is not affected by the shifted transfer characteristics, because I_{ch} drops to zero quickly as mentioned above. Both of the specific switching behaviours in turn-on and turn-off agree with the analysis in section 3.2.3.

3.5.3 Experiment validation

The impact of V_{th} shift on the switching behaviour of the Schottky-type GaN-HEMTs is analysed theoretically and demonstrated through simulation. As well, the decreased dV_{ds}/dt and dI_d/dt caused by the positive V_{th} shift are quantified experimentally in Table 3.6 for the slow switching conditions. However, considering the 600 V level rated voltage and the ultra-fast commutation speed of GaN-HEMTs, the influence of V_{th} shift on the switching behaviour under more practical switching conditions (400 V of V_{DC} with small R_{on}) requires to be validated experimentally. Additionally, the existence of these influences on GITs deserves to be investigated, given their different V_{th} shift behaviour and driving methods compared to Schottky-type GaN-HEMTs.

3.5.3.1 Schottky-type GaN-HEMTs

The H-bridge DPT is implemented under 400 V of V_{DC} with 20 Ω of R_g^{on} and 2 Ω of R_g^{off}, which are typical application conditions for the GaN-HEMTs. The turn-on and turn-off switching waveforms in biased and unbiased DPT are shown in Fig 3.33, where V_{ds} is measured by a 400 MHz high voltage passive probe (PPE4KV) and I_d is measured by a 1.2 GHz current shunt (SDN-015). V_{ds} and I_d in biased mode show the decreased dV_{ds}/dt (10.8 %) and dI_d/dt (13.2 %), leading to a 13.4 % increased E_{on}. The switching waveforms show less peak overshoot compared to the unbiased mode in turn-on transition, while the turn-off commutation does not show this variation. To be noted that this comparison experiment is repeated under different V_{DC} and with several different samples of GS66502B, and a similar phenomenon can be observed. All of these experimental results show the consistency with the previous theoretical analysis and simulation. Similar effect in turn-on switching waveforms for the Schottky-type GaN-HEMTs are also reported in [98], [104].

3.5.3.2 GITs

To further evaluate the influence of initial I-type V_{ds} bias on the switching behaviour of GITs, the similar biased and unbiased tests are implemented for the IGOT60R07D1 device. Two standard half-bridges, shown in Fig. 2.7, are configured as an H-bridge, where the high-side and low-side devices operate complementary on each bridge. The schematics and the control sequence are displayed in Fig. 3.34, where these two half-bridges are controlled separately and the switching waveforms of low-side GIT are monitored. The initial I-type V_{ds} bias time can be adjusted by extending the overlap time of V_g^1 and V_g^2 from t' to t_1 as shown in Fig. 3.34(b). It should be noted that the

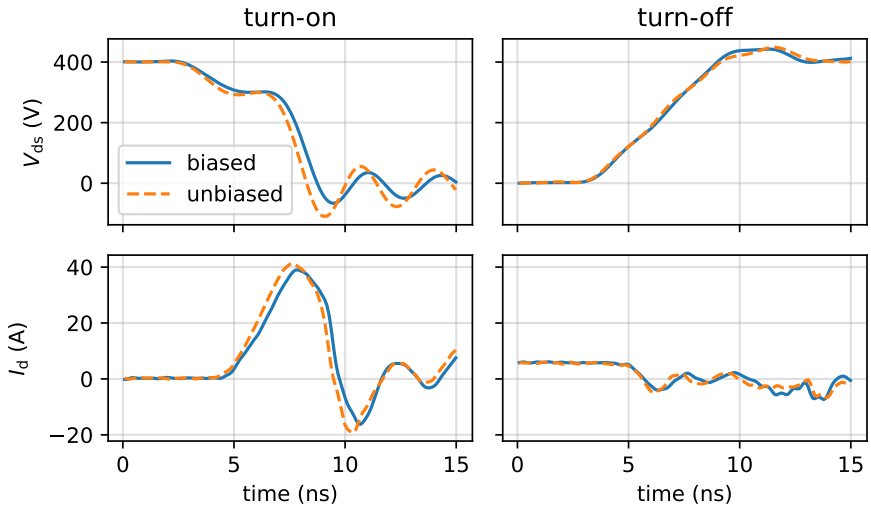


Figure 3.33: Experimental turn-on and turn-off switching waveforms from the H-bridge based DPT in fast switching condition with 400 V of V_{DC}.

initial V_{ds} bias is not fully eliminated compared to the one in Fig. 3.8 that is using for the Schottky-type GaN-HEMTs. This residual initial V_{ds} bias helps induce the positive V_{th} shift as shown in Fig. 2.15 compared to the extended initial V_{ds} bias, which potentially amplifies the V_{th} variations between biased and unbiased conditions for GITs and results in noticeable variations in the switching waveforms.

In this test, the switching waveforms with 1 µs and 100 s of initial V_{ds} bias time are respectively represent the unbiased and biased test, as shown in Fig 3.35. It should be noted that 1 µs and 100 s of I-type V_{ds} bias can respectively cause positive and negative V_{th} shift based on the characterisation result in Fig. 2.15, therefore, the influence of V_{th} shift on the switching behaviour of GIT could be obtained in this H-bridge based DPT.

The turn-on and turn-off switching waveforms with 10 Ω of R_g under 400 V of V_{DC} are depicted in Fig. 3.36. Based on the previous analysis, the dV_{ds}/dt and dI_d/dt of turn-on switching waveform in biased mode should be larger because of the negative V_{th} shift, however, this effect doesn't occur for the GITs. Moreover, the turn-off switching transition exhibits variations, because of the relative slow commutation speed and high load current of GITs, where the channel current cannot drop to zero fast. However, variation of dV_{ds}/dt and dI_d/dt doesn't follow the previous conclusion in section 3.2.3 that positive V_{th} could increase the turn-off commutation speed. Two reasons could explain the observed phenomenon. The shifted V_{th} of GIT can get recovered before the switching commutation, as supported by the fast recovery phenomenon described in section 2.2.2. Moreover, the driving method for GITs is different with the Schottky-type GaN-HEMTs, therefore, the Miller relation derived in section 3.2 can be changed for GITs, as they are current-driven devices.

The schematic of the gate configuration for driving the GITs is displayed in Fig. 3.37,

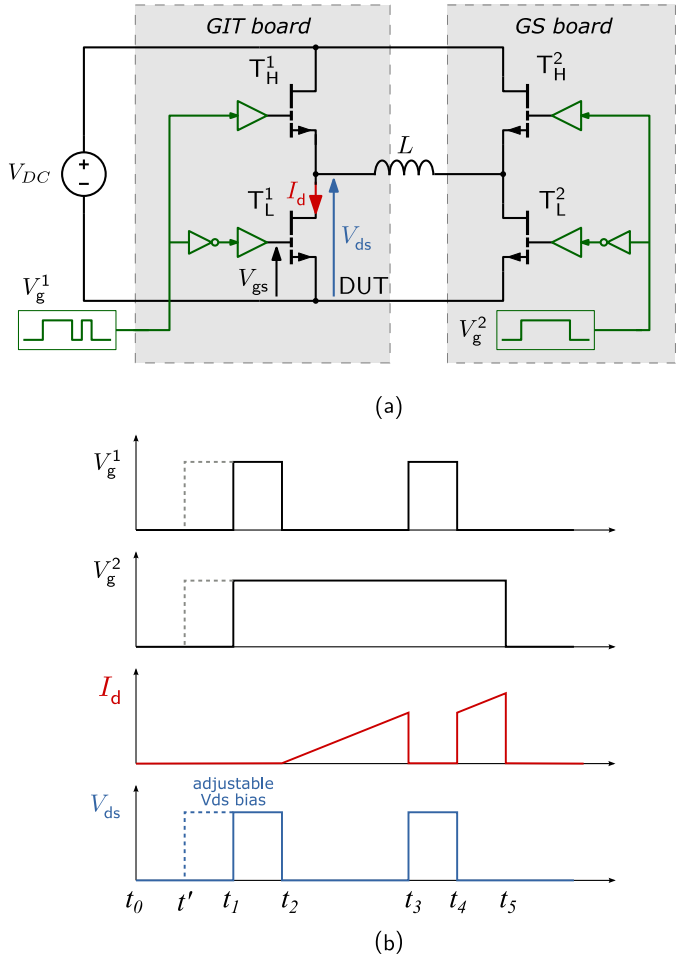


Figure 3.34: Schematic of the experiment setup for the biased and unbiased tests of GIT (a) circuit and (b) control sequence.

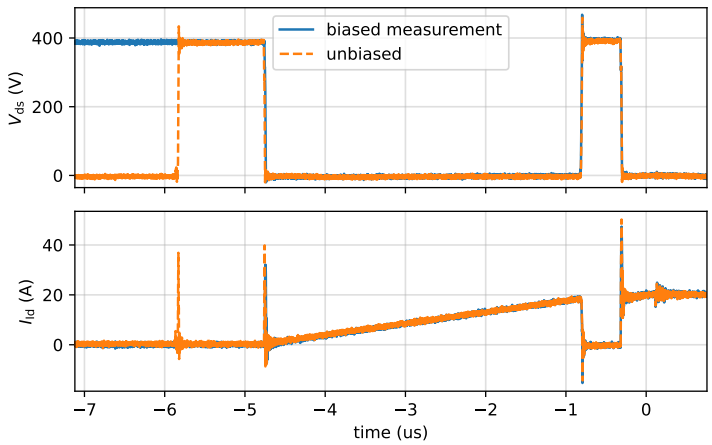


Figure 3.35: Measured biased and unbiased switching waveforms for GITs.

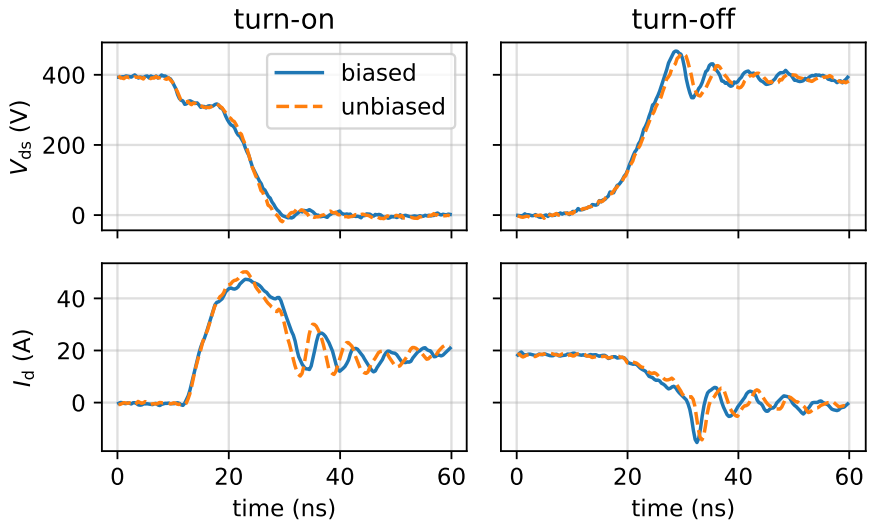


Figure 3.36: Biased and unbiased switching waveforms for GITs in turn-on and turn-off switching transition.

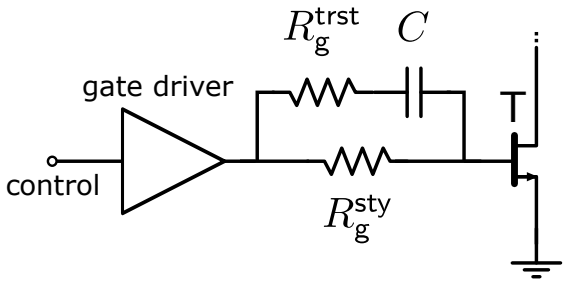


Figure 3.37: Schematic of gate configuration for driving the GITs.

where a relative large gate resistor R_g^{sty} (several hundred Ω) is used to provide a mA level gate leakage for maintaining the hole-injection mechanism of the GITs. To achieve a fast switching commutation, an RC configuration (several Ω of R_g^{trst} and several nF of C are connected in series) is required to drive the device, where bigger transient current can flow through the RC structure to charge or discharge the input capacitance of GITs more quickly. This gate configuration could influence the Miller plateau relation derived in section 3.2, moreover, the non-isolated gate stack of GITs can further complicate the analysis. Consequently, for future work, it is essential to evaluate the recovery time-constant of the shifted V_{th} and investigate the special gate stack and driving method for the GITs.

3.6 Conclusion and discussion

In this chapter, different voltage biases (two types of V_{ds} bias and V_{gs} bias) in the DPT are discussed and evaluated using the H-bridge based DPT. The two types of V_{ds} bias induced V_{th} shift are decoupled by analysing the extracted HVHC $I-V$ characteristics, representing an original contribution of this work. Afterward, a neural network based HVHC $I-V$ characteristics modelling method is proposed to accurately model V_{th} shift phenomenon of the Schottky-type GaN-HEMTs. Finally, the influence of V_{th} shift on the switching waveforms of Schottky-type GaN-HEMTs is analysed theoretically and demonstrated using simulation and experimental work, marking another contribution to this study.

The results indicate that the off-state V_{ds} bias before turn-on commutation (initial I-type V_{ds} bias) can cause positive V_{th} shift, while the V_{ds} bias during turn-on transient (II-type V_{ds} bias) can lead to negative V_{th} shift. Moreover, the short time of 6 V V_{gs} bias can cause the positive V_{th} shift and the negative V_{th} shift appears once the bias time is longer than 1 s. Based on the switching commutation analysis, the positive V_{th} shift could reduce the turn-on dV_{ds}/dt, dI_d/dt, increasing the switching losses. The reason is that the V_{gs} rising span from V_{th} to the plateau voltage is closer to V_g^{on} after positive V_{th} shift. As a result, the current commutation becomes longer due to the RC charging characteristics of V_{gs}. Moreover, the change in channel current ΔI_{ch} becomes smaller, which is positively related to dV_{ds}/dt based on the deduction in section 3.2.1. Meanwhile,

the turn-off transition remains essentially unchanged because the channel current drops to zero rapidly before the above mechanisms occur. However, if the turn-off switching transition is not very fast and with a relative high load current, where the channel current cannot drop to zero at the beginning of turn-off transition, the positive V_{th} shift might increase the turn-off commutation speed. Moreover, the tilted Miller plateau of GaN-HEMTs in slow switching condition can be attributed to the II-type V_{ds} bias induced negative V_{th} shift. The results suggest that the HVHC $I-V$ characteristics that include the V_{th} shift phenomenon are indispensable for accurate turn-on switching behaviour modeling and losses estimation. Moreover, the actual $I-V$ characteristics are influenced by various factors, including voltage biases, hot electrons, temperatures, etc., when the device operates in real power converters. Consequently, the characterisation method to obtain the multi-parameter coupled $I-V$ characteristics is essential, which would improve the accuracy for switching behaviour modelling for GaN-HEMTs.

As for the influence of V_{th} shift on the switching behaviour of GITs, the conclusion may be different with the Schottky-type GaN-HEMTs. Indeed, the GITs are current driving devices with the special non-isolated gate stack (Ohmic-type gate) and they also require an extra RC structure for fast turn-on and turn-off, resulting in a different switching transition analysis as Fig. 3.7, for example, the "Miller plateau relation" could be changed. Additionally, the I-type V_{ds} bias induced V_{th} shift in GITs may get recovered very quickly as discussed in Chapter 2. Consequently, the influence of V_{th} shift on the switching behaviour of GITs requires further investigation.

The influence of these two types of V_{ds} bias on the HVHC I-V characteristics of Schottky-type GaN-HEMTs has been investigated and modeled, revealing a significant impact on the switching of GaN-HEMTs. However, the switching behaviour of GaN-HEMTs is also strongly influenced by the gate driver stage, particularly in the output configurations, which will be the focus of the next chapter.

Chapter 4

Influence of the gate driver configuration on the switching behaviour

Outline of the current chapter

In this chapter, the influence of output capacitance of the gate driver on the switching waveforms of GaN-HEMTs will be discussed, with a primary focus on the two common gate loop topologies in GaN-HEMTs driving: single and split configurations. The chapter begins by introducing these two gate configurations and comparing the value of the output capacitance of gate driver and input capacitance of GaN-HEMTs to evidence the potential influence of the gate driver's output capacitance on the charging process of GaN-HEMTs. Following this, the equivalent circuits for both configurations are presented to analyse this phenomenon theoretically. Additionally, hard-switching simulations are conducted to investigate how the gate driver's output capacitance affects the switching behaviour of GaN-HEMTs across different configurations, taking into account the parasitic inductances in the gate loop. Afterward, a double pulse test (DPT) based hard-switching experiment is conducted to further verify these effects, demonstrating that the output capacitance in the split output gate driver can slow down the turn-on commutation speed of GaN-HEMTs. The potential influence of this effect on the GaN-based power converter and the future work are discussed at the end of this chapter.

4.1 Single and split gate output configurations

Due to the fast commutation speed of GaN-HEMTs, their switching behaviour is sensitive to the circuit parasitic parameters, especially to the gate loop parasitic inductance L_g. This is because the L_g induced voltage spike can exceed the V_{th} of GaN-HEMTs (typically 1.5 V) during the turn-off transition, leading to the false turn-on phenomenon. Furthermore, the L_g can oscillate with the parasitic capacitances in the gate loop causing the gate instability issue during turn-off transition as discussed in section 1.4.2.2. These issues can give rise to additional switching losses or even device breakdown, therefore, special attention should be paid in the gate loop to eliminate the gate oscillations.

To solve above issues, a negative V_{gs} can be applied to turn off the device to avoid the voltage spike exceeding the V_{th}. However, this is undesirable for GaN-HEMTs, as a negative V_{gs} can increase the reverse on-state voltage drop of GaN-HEMTs based

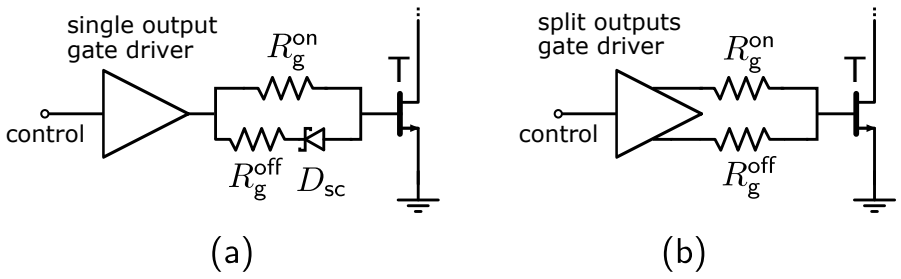


Figure 4.1: Schematic of single output (a) and split output (b) gate configurations.

on their third quadrant characteristics, leading to higher dead time losses [75], [119]. Some active gate driving techniques are proposed to provide adaptive gate voltage to solve the false turn-on issue and optimise the switching commutation behaviour [155], [156], however, the additional losses and reliability concern of the active driver add new challenges for circuit design.

4.1.1 Split output gate configurations

The key to solve the false turn-on issue lies in reducing the impedance of the turn-off loop. In the gate loop design, a small R_g^{off} is typically recommended to achieve a low turn-off impedance, and a relative large R_g^{on} is used to slowdown the turn-on commutation to avoid the high current overshoot or severe EMI, as shown in Fig. 4.1(a) [111]. To achieve this configuration, a Schottky diode is necessary to separate the turn-on and turn-off loops. However, this Schottky diode can introduce an approximate 0.3 V or even more positive voltage drop on the C_{gs} during turn-off transition, and this voltage drop can increase the V_{gs} during turn-off transition, leading to a high risk of false turn-on phenomenon, and it is non-negligible for GaN-HEMTs as the V_{th} is typically only 1.5 V. Therefore, a split output gate driver is recommended [157], [158], where there are two separate output channels for the turn-on and turn-off transitions, as shown in Fig. 4.1(b). In this configuration, the Schottky diode is not required and the voltage drop on it can be eliminated [155]. Furthermore, the gate circuitry can be designed more compact to further reduce the L_g, so this split output gate driver is widely adopted by the integrated GaN-based power modules [159].

However, the influence of these two types of gate driver topologies on the switching behaviour of GaN-HEMTs is less discussed, although it is of high interests for high-efficiency gate driver selection and compact GaN-based power module design.

4.1.2 Driving of GaN-HEMTs using single and split gate configurations

4.1.2.1 Driving process in turn-on and turn-off

During the commutation of GaN-HEMTs, it is the voltage across C_{gs} that turns-on and -off the devices, and the V_{gs} is generally sourced and sunk by the gate driver. Specifically, this process is achieved by complementarily switching the N-channel MOSFETs (NMOS)

and P-channel MOSFETs (PMOS) of a push-pull configuration in the gate driver as displayed in Fig. 4.2, where the source and sink loop are respectively shown as the red and blue solid arrow lines. During the turn-on transition, the PMOS in the gate driver is turned to on-state to allow the gate voltage V_g to charge the C_{gs}. Simultaneously, the NMOS is in off-state, and its output capacitance C_{oss} also gets charged by the V_g as highlighted by the red dashed arrow line in Fig. 4.2. The off-state of NMOS provides a possibility that the charging speed of C_{gs} of GaN-HEMTs can be slowed down by the charging process of the output capacitance of NMOS (C_{oss}^{NMOS}), since the gate charging current is diverted by the C_{oss}^{NMOS}. Similarly, the discharging speed of GaN-HEMTs' C_{gs} can also be decreased by the charging process of the output capacitance of PMOS (C_{oss}^{PMOS}). Therefore, the turn-on and turn-off transitions could be influenced by the output capacitance of gate driver, specifically the C_{oss}^{NMOS} or C_{oss}^{PMOS} within the gate driver, where the two configurations of single- and split-output drivers can make a difference. Additionally, there is no in-depth study in the literature about this regard, which is the main knowledge gap addressed by this chapter.

4.1.2.2 C_{oss} of gate driver's MOSFETs and C_{iss} of GaN-HEMTs

The impact of the C_{oss} of MOSFETs in the gate driver can usually be neglected when driving Si or SiC power MOSFETs, since the value of C_{iss} for power MOSFETs can be up to several nano-farad [160]. This value is far larger than the C_{oss} of the gate driver's MOSFETs [157]. However, the C_{iss} of power GaN-HEMTs is significantly reduced compared to that of Si or SiC MOSFETs at the same power level, as compared in Table 1.7. Moreover, input capacitance value of various power GaN-HEMTs (C_{iss}^{GaN}) is listed in Table 4.1 and the C_{oss} of low power Si-MOSFETs is collected in Table 4.2 for comparison, showing the same level of capacitances. It should be noted that the Si-MOSFETs in Table 4.2 are selected based on the V_{ds} and I_d values that are in the same range as maximum supply voltage (V_{DD}), sink current (I_{sink}) and source current (I_{source}) of the commercial gate drivers for GaN-HEMTs. To support this comparison, the maximum V_{DD}, I_{sink} and I_{source} of the commercial gate drivers for GaN-HEMTs are listed in Table 4.3. It also should be noted that the I_d in Table 4.2 represents the continuous current, while the I_{sink} and I_{source} in Table 4.3 represent the pulsed current. As the pulsed current is around 3 to 4 times higher than the continuous current, the power level of Si-MOSFETs in Table 4.2 can be considered equivalent to that for the commercial gate driver in Table 4.3. Moreover, the C_{oss}^{NMOS} in the LM5114 and 1EDN7511B gate drivers have been measured in this work, where the measurement process will be discussed in section. 4.2.1.1, and the results align with the C_{oss} range shown in Table 4.2. Additionally, some C_{oss} of the low power MOSFETs are even larger than the C_{iss}^{GaN}, which could significantly influence the charging or discharging process of GaN-HEMTs when driven by these type of gate drivers. The potential influence will be analysed in detail below.

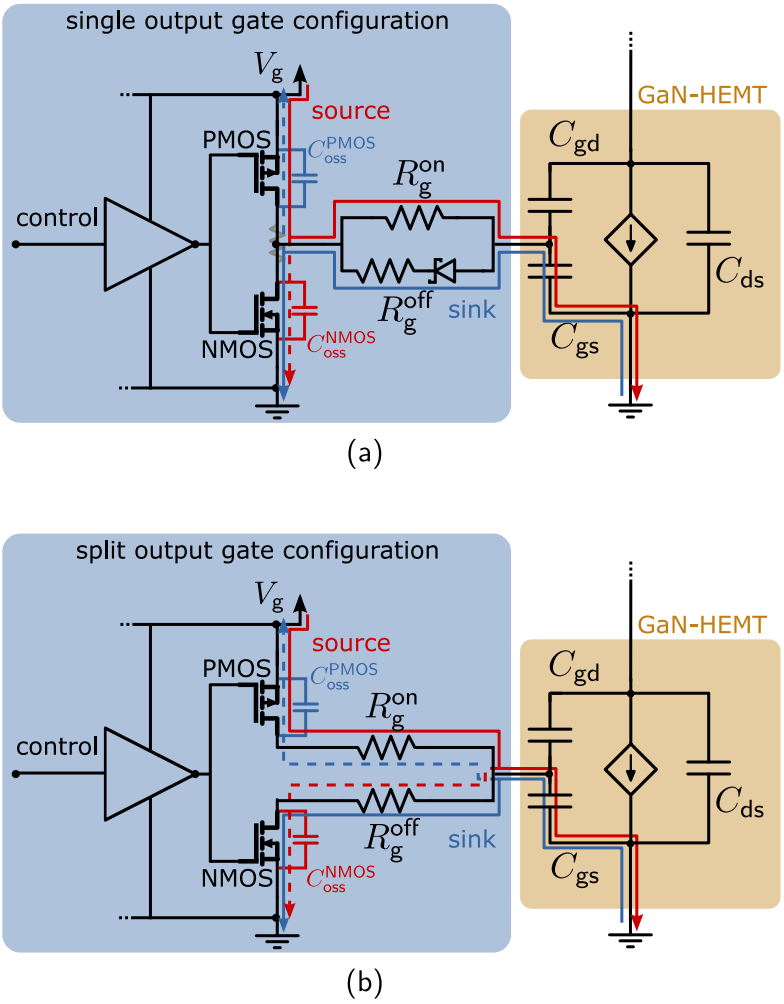


Figure 4.2: Turn-on and turn-off (source and sink) loop of (a) single and (b) split output gate configurations for GaN-HEMTs driving.

Devices	Model	V_{ds} (V) / I_d (A)	C_{iss} (pF)
GaN-HEMTs	GS66502B	650 / 7.5	60
	GS-065-018-6-LR	700 / 23	132
	GS66508B/T	650 / 30	240
	IGLR60R340D1	600 / 8	88
	IGLR60R260D1	600 / 10	110
	INN700D350B	700 / 6	50
	SGT120R65AL	650 / 15	125

* Data in this table is from the manufacturer datasheet.
** C_{iss} is measured when V_{DS} is 400 V and V_{GS} is 0 V.

Table 4.1: C_{iss} of commercial power GaN-HEMTs.

Devices	Model	V_{ds} (V) / I_d (A)	C_{oss} (pF)
N-Chanel Si-MOSFETs	Si1050X	8 / 1.34	190
	CSD13381F4	12 / 2.1	47
	CSD13201W10	12 / 1.6	245
	PMXB40UNE	12 / 3.2	107
P-Chanel Si-MOSFETs	Si1499DH	-8 / -1.6	220
	RZF020P01	-12 / -2	75
	CSD13201W10	-12 / -1.6	73
	DMP1200UFR4	-12 / -2	131

* Data in this table is from the manufacturer datasheet.
** C_{oss} is measured under half of rated V_{DS} voltage and 0 V of V_{GS}.

Table 4.2: C_{oss} of commercial low power Si-MOSFETs.

Model	Max. V_{DD} (V)	I_{sink}(A) / I_{source} (A)	Output
LM5114	12.6	7.6 / 1.3	Split
UCC27511	18	8 / 4	Split
UCC27512	18	8 / 4	Single
1EDN7511B	10	8 / 4	Split
1EDN7512B	10	8 / 4	Single

* Data in this table is from the manufacturer datasheet.

Table 4.3: Commercial low-side gate drivers for power GaN-HEMTs.

4.1.3 Driving variation using single and split gate configurations

It has been found that the C_{oss} in the gate driver's MOSFETs could influence the charging and discharging process of the C_{iss} of GaN-HEMTs due to the similar capacitance value. However, when the GaN-HEMTs are respectively driven by the single and split output gate drivers, the impact could be different.

4.1.3.1 Equivalent circuits for the single and split output gate configurations

To analyse the driving variation, the equivalent circuits of the charging process for GaN-HEMTs using the single and split output gate configurations are depicted in Fig. 4.3. When GaN-HEMTs are driven by the single output gate configuration, with L_g neglected at first, the equivalent circuit can be considered as a single RC circuit, as displayed in Fig. 4.3(a). Here, the charging loop of C_{oss}^{NMOS} inside the gate driver is neglected, because it gets charged extremely fast when compared to the charging process of C_{iss}^{GaN}. Specifically, the corresponding charging time constants for C_{oss}^{NMOS} and C_{iss}^{GaN} are respectively $R_{para}C_{oss}^{NMOS}$ and $R_g^{on}C_{iss}^{GaN}$, where R_{para} is the parasitic resistance in the gate driver between C_{oss}^{PMOS} and C_{oss}^{NMOS} as highlighted as a grey resistor in Fig. 4.2(a), and it is far smaller than R_g^{on}. Therefore, the charging process of GaN-HEMTs using the single output gate configuration can be seen as a single RC charging process. By contrast, the split output gate configuration can be regarded as a two-stage cascade RC circuit, where the R_g^{off} and C_{oss}^{NMOS} are included as a branch and this branch is connected to the output of the first-stage $R_g^{on}C_{iss}^{GaN}$, as depicted in Fig. 4.3(b). In the cascade RC circuit, The time constant of R_g^{off} and C_{oss}^{NMOS} can be comparable to that of R_g^{on} and C_{iss}^{GaN}. In this cascade RC topology, C_{iss}^{GaN} and C_{oss}^{NMOS} will be charged to V_g at the same time, interacting with each other during the charging process. Therefore, the charging process of C_{iss}^{GaN} can be influenced by the charging of C_{oss}^{NMOS}, when the split output gate configuration is adopted.

4.1.3.2 Influence of C_{oss}^{NMOS} on the charging process of C_{iss}^{GaN} in split output configuration (SPOGC effect)

When GaN-HEMTs are driven by different gate configurations, the charging behaviour of C_{iss}^{GaN} could be different. To investigate the influence of C_{oss}^{NMOS} on the charging process of C_{iss}^{GaN}, when using different gate configurations, the simulation using the schematics in Fig. 4.3 can be implemented. For simplification, C_{oss}^{NMOS} is considered as linear, and the parasitic inductance L_g is neglected. A single pulse voltage source V_g with 10 ns of rise time (t_r^g) is used to emulate the output voltage from the gate driver during the turn-on transition. The value of t_r^g is selected based on the datasheet of a commercial gate driver [157]. The value of C_{oss}^{NMOS} sweeps from 0 to 240 pF in steps of 60 pF and these values are in the same range of the C_{oss}^{NMOS} in commercial gate drivers based on the values listed in Table 4.2. Other simulation parameters are listed in Table 4.4. The simulation waveforms of voltage on C_{iss}^{GaN} in these two configurations, V_{single} and V_{split}, are displayed in Fig. 4.4(a). The rising speed of V_{split} is reduced with the increasing

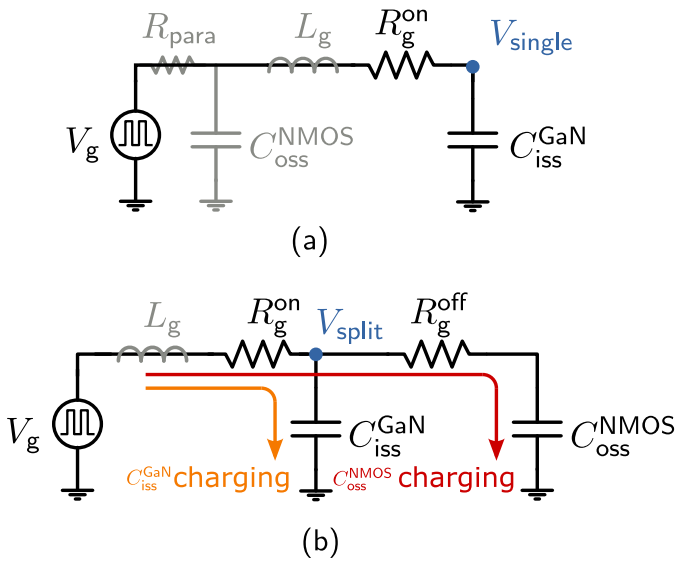


Figure 4.3: Equivalent circuit of the charging process for GaN-HEMTs using (a) single and (b) split output gate configurations.

of C_{oss}^{NMOS}, while the V_{single} remains unchanged. To quantify this differentiation, the rise time of V_{single} and V_{split} from 0 to 3.6 V (63 % of V_g) are respectively defined as t_r^{single} and t_r^{split}, afterward, the relative change rate of t_r^{single} and t_r^{split} ($\Delta t_r^{spt-sgl}$) can be calculated using eq. 4.1:

$$\Delta t_r^{spt-sgl} = \frac{t_r^{split} - t_r^{single}}{t_r^{single}} \times 100\,\% \tag{4.1}$$

The calculated $\Delta t_r^{spt-sgl}$ under different C_{oss}^{NMOS} is displayed in Fig. 4.4(b), showing that the rising speed of V_{split} is slower than the V_{single} and this variation becomes prominent with the increasing of C_{oss}^{NMOS}.

This variation can be explained by the extended time constant of the cascade RC topology in the split output gate configuration, in which the values of C_{oss}^{NMOS} and R_g^{off} play significant roles. On the one hand, the increased C_{oss}^{NMOS} enlarges the time constant of the second RC stage, leading to a large overall time constant for the entire RC topology. On the other hand, the small R_g^{off} is critical in this process. For instance, if the R_g^{off} is far larger than R_g^{on}, the influence of $R_g^{off}C_{oss}^{NMOS}$ branch on the charging process of C_{iss}^{GaN} would be minimal. In this case, the $R_g^{on}C_{iss}^{GaN}$ would essentially charge according to its own normal time constant. Meanwhile, the $R_g^{off}C_{oss}^{NMOS}$ would charge slowly without pronounced influence on the voltage across C_{iss}^{GaN}. When the R_g^{off} is much smaller than the R_g^{on}, the C_{iss}^{GaN} and C_{oss}^{NMOS} behave as if they are in parallel, and the charging time constant of C_{iss}^{GaN} approximates $R_g^{on}(C_{iss}^{GaN}+C_{oss}^{NMOS})$, resulting in reduced charging speed

$R_g^{on} = 20\,\Omega$	$R_g^{off} = 2\,\Omega$	$R_{para} = 1\,m\Omega$	$C_{iss}^{GaN} = 60\,pF$	$V_g = 6\,V$	$L_g = 0\,H$	$t_r^g = 10\,ns$

Table 4.4: Simulation parameters for investigating the influence of C_{oss}^{NMOS} on the charging process of C_{iss}^{GaN} in Fig. 4.4.

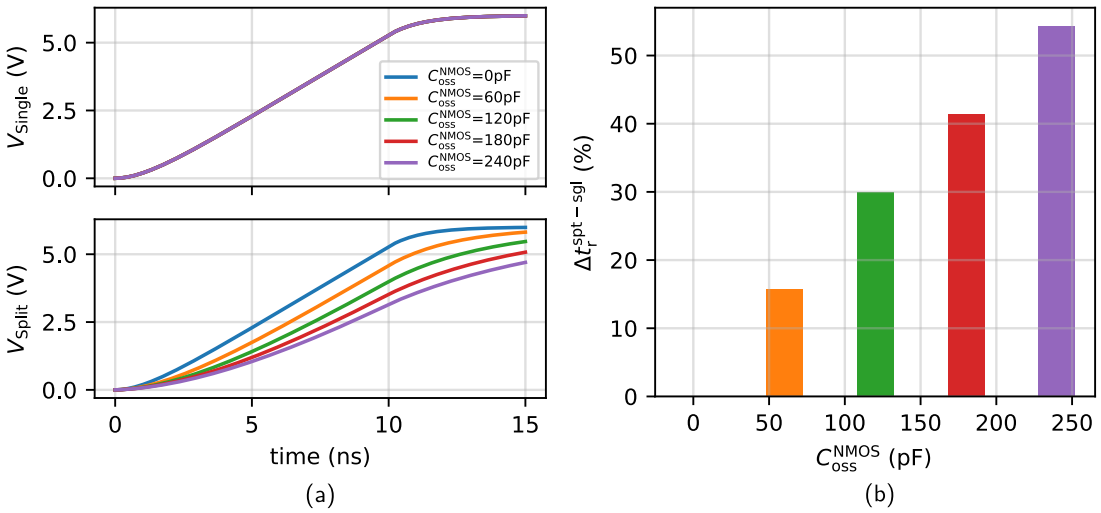


Figure 4.4: Simulation result of (a) charging waveforms of C_{iss}^{GaN} in single and split output configurations with various C_{oss}^{NMOS} and (b) calculated $\Delta t_r^{spt-sgl}$.

of C_{iss}^{GaN}. In fact, configurations of smaller R_g^{off} and larger C_{oss}^{NMOS}, compared to the R_g^{on} and C_{iss}^{GaN}, could enlarge this charging variation, which will be discussed in detail in the following section. Interestingly, the comparable value of C_{oss}^{NMOS} in the gate driver to C_{iss}^{GaN} and the recommended small R_g^{off} in GaN-HEMT applications satisfy configurations analysed here. As for the single output topology, the increased C_{oss}^{NMOS} could not affect the charging process of C_{iss}^{GaN} as the charging process is equivalent to a single RC, due to the extreme small R_{para}. Therefore, the charging speed of C_{iss}^{GaN} in split output gate configuration will be slowed down by increasing the C_{oss}^{NMOS} in the gate driver.

For conciseness, the influence of C_{oss}^{NMOS} on the charging process of C_{iss}^{GaN} in the split output gate configuration is defined as split output gate configuration (SPOGC) effect further in this study. This effect can be quantified by $\Delta t_r^{spt-sgl}$, and the larger $\Delta t_r^{spt-sgl}$ the more significant SPOGC effect. Investigating this effect is meaningful since the commutation speed and switching behaviour of GaN-HEMTs are significantly dependent on the charging and discharging time of C_{iss}^{GaN}, and the switching commutation is directly related to the switching losses estimation and EMI evaluation of the devices.

4.1.4 Influence of gate circuit parameters on the SPOGC effect

The magnitude of SPOGC effect can vary, depending on the specific value of the gate circuit parameters, such as t_r^g, R_g and L_g. The influence of these parameters on the

Power transistors	Gate driver model	t_r^g (ns)	V_{DD} (V)	Load C_L (pF)
Si-MOSFETs, GaN-HEMTs	UCC27511	16	4.5	1800
	LM5114	10	4.5	1000
	1EDN7511B	6.5	12	1800
	Si827X	10.5	15	200
GaN-HEMTs	NCP51820	2	15	330
	LMG1025Q	0.65	5	220
	TPS7H60x5	3	5	1000

* Data in this table is from the manufacturer datasheet.

Table 4.5: Comparison of the rise time of commercial gate drivers (for Si-MOSFETs and GaN-HEMTs) under different test conditions.

SPOGC effect will be discussed below.

4.1.4.1 Influence of t_r^g on SPOGC effect

The influence of gate driver's rise time t_r^g on the SPOGC effect could be significant, because t_r^g is approximately in the same range of commutation time as power GaN-HEMTs. For example, the t_r^g of commercial gate driver are approximately 10 ns, and the turn-on time of GaN-HEMTs can also fit this range as shown in Fig. 3.33. For this reason, the rising edge of the output voltage pulse from gate driver cannot be simply considered a step excitation for GaN-HEMTs. In contrast, this is acceptable for Si-MOSFETs, as their turn-on commutation time can last several hundred nanoseconds. The 10 ns of t_r^g from gate driver is more like a ramp excitation during the driving of GaN-HEMTs. Therefore, t_r^g could be one of the factors influencing the SPOGC effect and further influencing the switching behaviour of GaN-HEMTs.

Interestingly, the rise time t_r^g of newly released gate drivers for GaN-HEMTs has been significantly reduced, which may further reduce the commutation time or trigger other effect on the switching behaviour of GaN-HEMTs. In Table 4.5, the t_r^g of various gate drivers for Si-MOSFETs and GaN-HEMTs are compared, and the output voltage V_{DD} and load capacitor C_L during the test are listed as well. It should be noted that the classification is based on the recommendations provided in the datasheet of these gate drivers. The t_r^g of gate drivers dedicated to GaN-HEMTs (as recommended in the datasheet and application note [158], [161]) is noticeably reduced compared to that of gate drivers for Si-MOSFETs. Therefore, it is necessary to analyse the influence of t_r^g on the SPOGC effect.

To investigate the influence of t_r^g, the simulation for Fig. 4.4 is repeated but with t_r^g set to 2 ns, while other parameters remain unchanged. This setting is used to emulate the turn-on charging process of GaN-HEMTs driven by the fast gate driver. The simulation waveforms of V_{single} and V_{split} are displayed in Fig. 4.5(a), where the charging speed

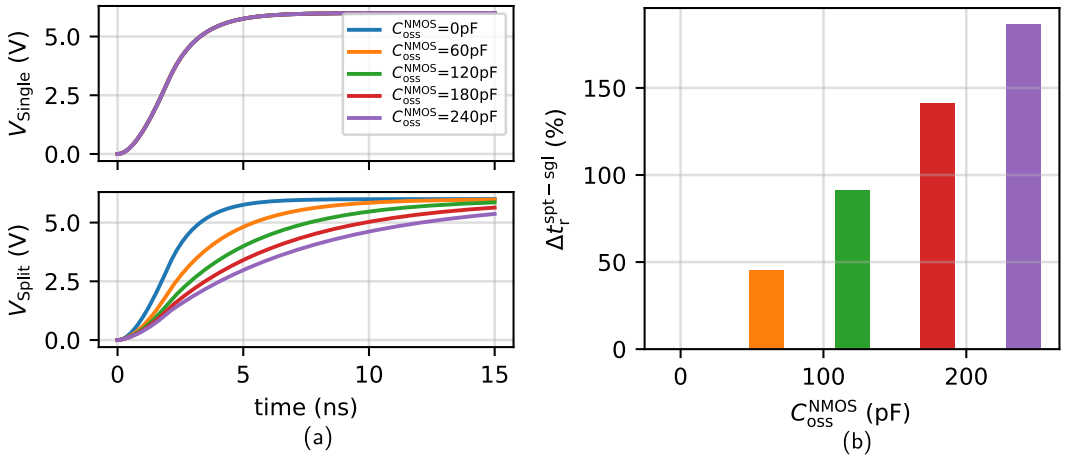


Figure 4.5: Simulation result of (a) charging waveforms of C_{iss}^{GaN} in single and split output configurations with various C_{oss}^{NMOS} and (b) calculated $\Delta t_r^{spt-sgl}$ with t_r^g=2 ns.

$C_{oss}^{NMOS} = 120\,pF$	$R_{para} = 1\,m\Omega$	$C_{lss}^{GaN} = 60\,pF$	$V_g = 6\,V$	$L_g = 0\,H$	$t_r^g = 2\,ns$

Table 4.6: Simulation parameters for investigating the influence of R_g on the SPOGC effect in Fig. 4.6.

of C_{iss}^{GaN} in these two configurations are much faster compared to that using 10 ns of t_r^g. Moreover, the $\Delta t_r^{spt-sgl}$ is significantly increased with 2 ns of t_r^g, as displayed in Fig. 4.5(b), indicating a more severe SPOGC effect driven by the gate driver with small t_r^g.

The above simulation shows that a small t_r can enhance the SPOGC effect compared to a large t_r with other parameters remaining the same. This is because a large t_r (low speed source) could alleviate the effect of R_g^{on} or R_g^{off} in the transient. Specifically, when the RC topology is subjected to a ramp excitation with a time constant greater than that of the RC, the capacitor voltage simply follows the ramp with an offset determined by the value of resistor, where the charging speed of capacitor depends more on the charging source. To further evaluate the circuit parameters on the SPOGC effect, the influence of R_g^{on} and R_g^{off} should be discussed below.

4.1.4.2 Influence of R_g on SPOGC effect

The simulation for Fig. 4.3 is further implemented by increasing the R_g^{off} from 2 Ω to 20 Ω with R_g^{on} = 20 Ω. Other simulation parameters are displayed in Table 4.6. $\Delta t_r^{spt-sgl}$ decreases with the increasing of R_g^{off}, as shown in Fig. 4.6(a), indicating a reduction in the SPOGC effect. This reduction represents that the relative small R_g^{off} tends to enhance the SPOGC effect, as it effectively makes C_{oss}^{NMOS} paralleled to C_{iss}^{GaN}.

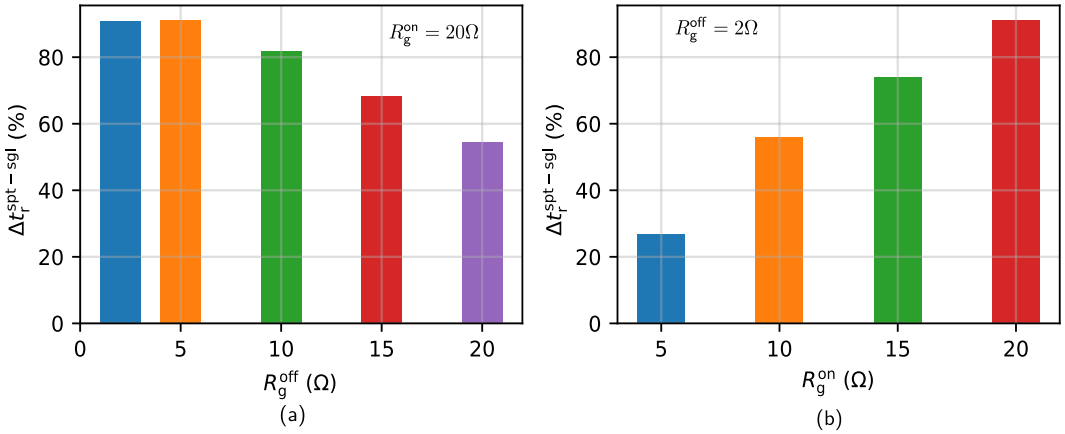


Figure 4.6: Relative change rate of rise time (a) with different R_g^{off} at $R_g^{on} = 20\Omega$ and (b) different R_g^{on} at $R_g^{off} = 2\Omega$.

To gain further insight into this phenomenon, the charging current and charges of C_{oss}^{NMOS} and C_{iss}^{GaN} are calculated in these two configurations, where R_g^{off} is respectively set to 2 Ω and 200 Ω with $R_g^{on} = 20\,\Omega$, as shown in Fig. 4.7. Other simulation parameters remain the same as those in Table 4.6. In the case of $R_g^{off} = 2\,\Omega$, the rising speed of voltage across C_{iss}^{GaN} (V_{iss}^{GaN}) has been notably reduced in the split output configuration, representing a severe SPOGC effect. This occurs because the charging of C_{oss}^{NMOS} affects the charging process of C_{iss}^{GaN}, which is supported by the even higher charging current and charges in the C_{oss}^{NMOS} compared to the C_{iss}^{GaN}. However, when $R_g^{off} = 200\,\Omega$, the charging process of C_{iss}^{GaN} is less impacted by the C_{oss}^{NMOS}, supported by significantly reduced charging current and charges for C_{oss}^{NMOS}. Moreover, the charging current and charges of C_{iss}^{GaN} when $R_g^{off} = 200\,\Omega$ are smaller than those when $R_g^{off} = 2\,\Omega$, showing a reduced SPOGC effect. These simulation results align with the analysis in section 4.1.3.2.

Furthermore, the influence of R_g^{on} is investigated by increasing it from 5 Ω to 20 Ω with $R_g^{off} = 2\,\Omega$, and the $\Delta t_r^{spt-sgl}$ becomes larger with higher R_g^{on}, as shown in Fig. 4.6(b). This is because that the charging processes of both C_{iss}^{GaN} and C_{oss}^{NMOS} are reduced with the rising of R_g^{on}, which masks the effect of the increased time constant from the $R_g^{off} C_{oss}^{NMOS}$ branch on the overall RC topology. In other word, the relative value of R_g^{off} is reduced by increasing the R_g^{on}, which makes the parallel effect of C_{oss}^{NMOS} more effective.

It should be noted that the trend shown in Fig. 4.6 still exists when $t_r^g = 10\,\text{ns}$ but it is somewhat less pronounced, which support the analysis in Section 4.1.4.1.

4.1.4.3 Influence of L_g on SPOGC effect

The gate loop parasitic inductance L_g could also influence the SPOGC effect, particularly when t_r^g is small. During the charging process of C_{iss}^{GaN}, most of the initial voltage change is applied across the L_g, causing the gate current to be smoothed by the inductive response. However, the lumped L_g in Fig. 4.3 may not influence the SPOGC effect

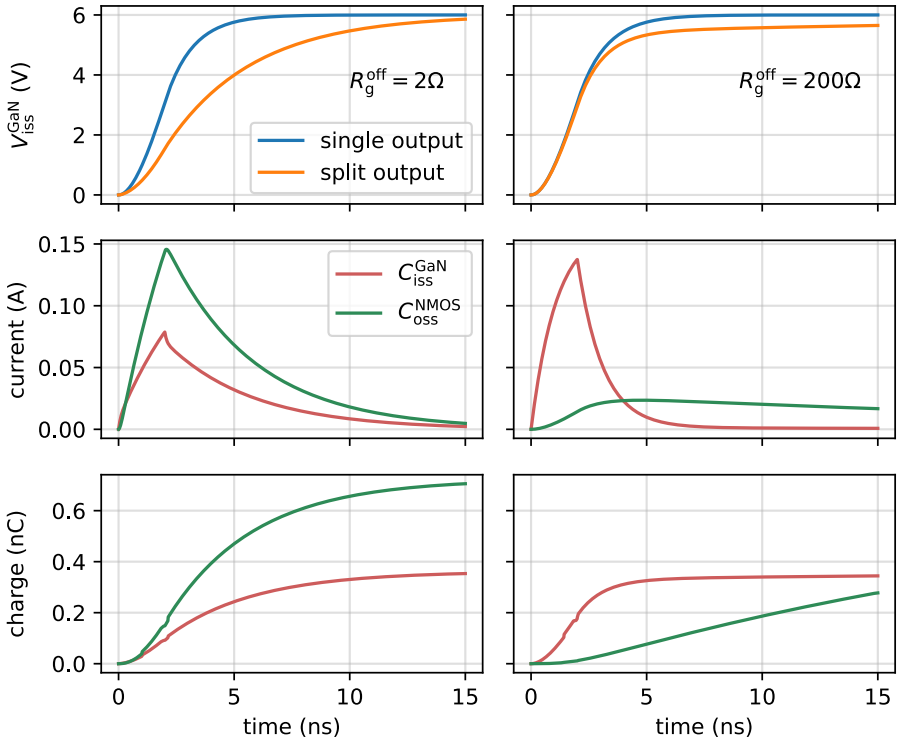


Figure 4.7: Mechanism of R_g^{off} influence on the SPOGC effect with the switching waveform of V_{iss}^{GaN} in single and split output configurations, as well as the charging current and charge in C_{iss}^{GaN} and C_{oss}^{NMOS}.

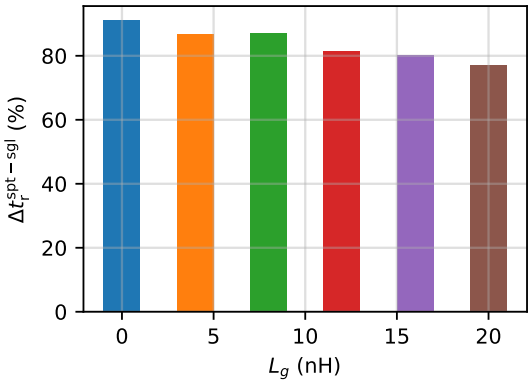


Figure 4.8: Simulation result of $\Delta t_r^{spt-sgl}$ with lumped L_g increasing from 0 nH to 20 nH.

significantly, because the lumped L_g is shared by the charging loop of C_{iss}^{GaN} and C_{oss}^{NMOS}, which may not influence the charging balance of these two loops. This hypothesis can be supported by sweeping the lumped L_g from 0 nH to 20 nH in the simulation with the configuration of Fig. 4.3, where $R_g^{on} = 20\,\Omega$ and $R_g^{off} = 2\,\Omega$ and another parameters remain the same as Table 4.6. The simulation result of $\Delta t_r^{spt-sgl}$ is shown in Fig. 4.8 and the small variation of $\Delta t_r^{spt-sgl}$ indicates the lumped L_g has very limited influence on the SPOGC effect, even though the range of L_g variation is much smaller than 20 nH in a well-designed gate loop.

However, the actual L_g in the gate circuitry is not lumped as in Fig. 4.3 but unevenly distributed in the turn-on and turn-off loops. Thus, the influence of distributed L_g on the SPOGC effect should be discussed and the cascade RC circuit with considering the distributed L_g in turn-on and turn-off loops is employed to evaluate this effect as shown in Fig. 4.9(b), where L_g^{on} and L_g^{off} respectively corresponds to the L_g of source and sink loop in Fig. 4.2. By contrast, the equivalent charging circuit of single output topology remains unchanged as in Fig. 4.9(a).

In the simulation, the L_g^{off} is varied from 2 nH to 10 nH in step of 2 nH with L_g^{on} fixed at 5 nH and other simulation parameters are listed in Table 4.7. As the simulation results shown in Fig. 4.10(b), the $\Delta t_r^{spt-sgl}$ does not change monotonically with increasing L_g^{off}, although a reduced trend is presented after L_g^{off} exceeding 4 nH. The influence of distributed L_g on the SPOGC effect is complicated, because the introduced L_g^{on} and L_g^{off} could cause severe oscillation during the charging process of C_{iss}^{GaN} as shown in Fig. 4.10(a). Moreover, the actual C_{iss}^{GaN} and C_{oss}^{NMOS} are non-linear capacitances, and there also exist mutual inductive coupling between the gate and power loop, leading to more complicated value of L_g. Therefore, the impact of L_g on SPOGC effect in various circuits can differ, especially in fast switching commutation.

To summarise, the SPOGC effect becomes more pronounced with the increasing of C_{oss}^{NMOS}, reducing of R_g^{off}, which can extend the charging process of C_{iss}^{GaN} in the split output gate configurations. Moreover, a small t_r^g in the gate driver could enhance the

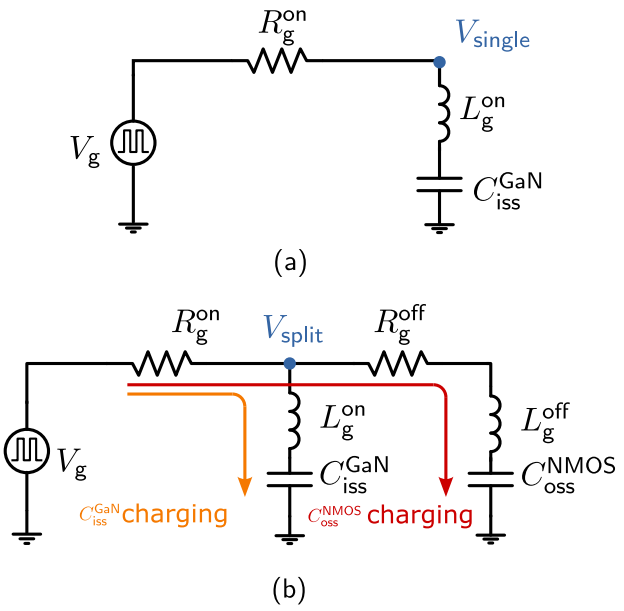


Figure 4.9: Equivalent charging circuit of (a) single and (b) split output gate configuration considering a distributed L_g

$R_g^{on} = 20\,\Omega$	$R_g^{off} = 2\,\Omega$	$C_{iss}^{GaN} = 60\,pF$	$C_{oss}^{NMOS} = 120\,pF$
$L_g^{on} = 5\,nH$	$t_r^g = 2\,ns$	$V_g = 6\,V$	

Table 4.7: Simulation parameters of investigating the influence of L_g^{off} on the SPOGC effect in Fig. 4.10

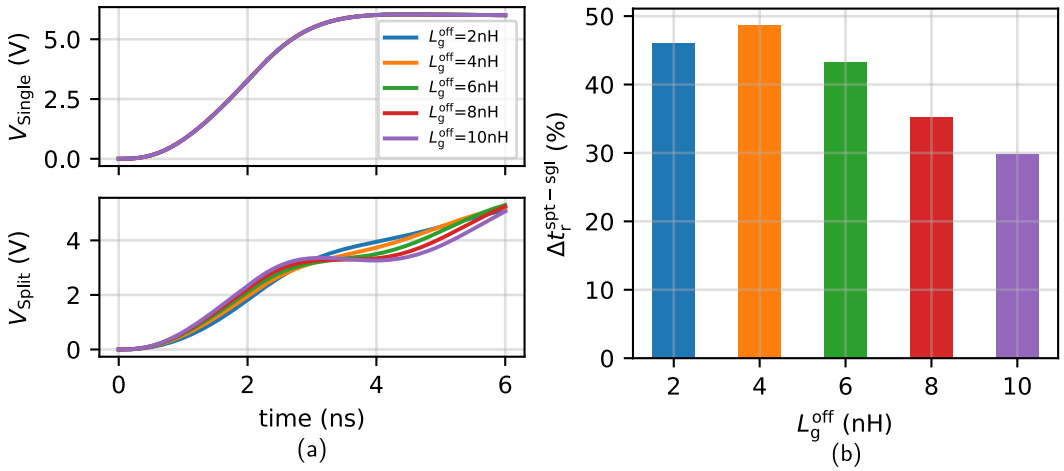


Figure 4.10: Simulation result of (a) charging waveforms of C_{iss}^{GaN} in single and split output configurations with considering different L_g^{off} and (b) calculated $\Delta t_r^{spt-sgl}$.

SPOGC effect as well. However, when considering the distributed L_g, the LC resonance-induced fluctuations complicate the charging process of C_{iss}^{GaN}.

To thoroughly assess the impact of the SPOGC effect on the switching behaviour of GaN-HEMTs, it is essential to consider the actual parasitic parameters in the gate circuitry and the non-linear capacitances. Therefore, a switching behaviour simulation with considering an actual GaN-HEMT model and parasitic circuit parameters is recommended, followed by experimental validation to further verify the influence, which will be discussed in the following part.

4.2 SPICE simulation of SPOGC effect on switching behaviours

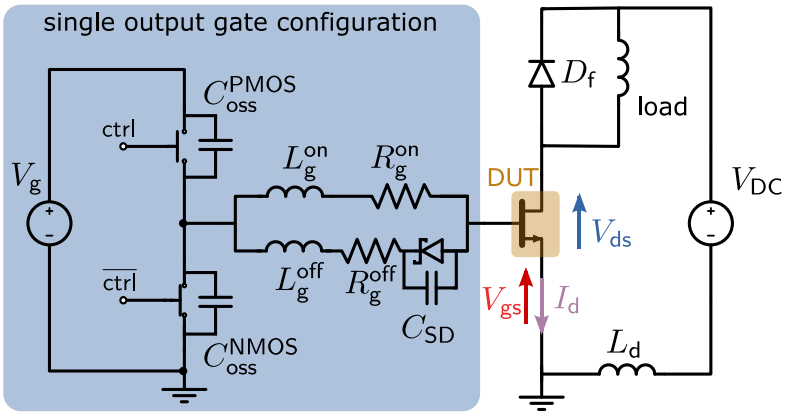
It is of practical significance to investigate the impact of SPOGC effect on GaN-HEMTs switching behaviours, considering the proper circuit parasitic parameters, such as the non-linear characteristics of C_{iss}^{GaN} and C_{oss}^{NMOS}, as well as the parasitic inductance in the gate (L_g) and power loop L_d. Therefore, a half-bridge based hard-switching simulation emulating the double-pulse test is implemented, where the low-side GaN-HEMT (as the DUT) is respectively driven by the single and split output gate configurations as shown in Fig. 4.11. The high-side device functions as a freewheeling diode (D_f) that can be achieved by shorting the gate and source of a GaN-HEMT. To be noted that only the turn-on process is investigated, since the phenomenon in turn-off is similar as analysed in Fig. 4.2. The GS66502B SPICE model provided by manufacturer is used as the high-side and low-side power transistors in this simulation. The two gate drivers with single and split output topology are modelled by ideal switches in parallel with capacitors, performing as the C_{oss}^{NMOS} and C_{oss}^{PMOS}, and the whole ensemble functions as a push-pull gate driver. The reason for using ideal switches with capacitors instead of MOSFET models in the gate driver is that it facilitates adjustment of the C_{oss} value of the gate driver MOSFETs. Specifically, the C_{oss} will be modelled as a non-linear capacitance in this section.

4.2.1 Circuit parasitic parameters extraction for SPICE simulation

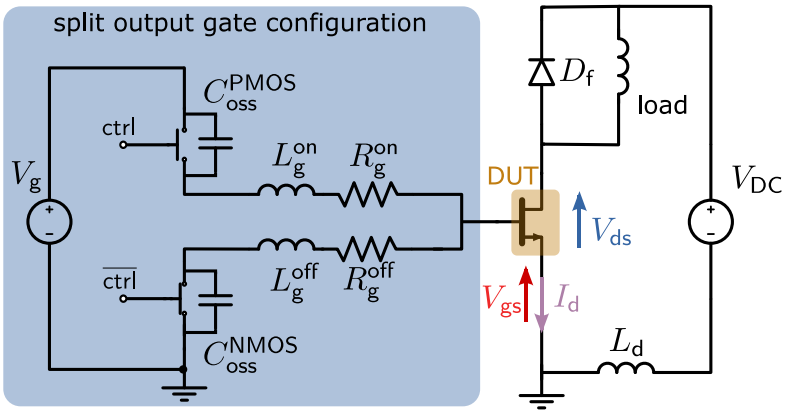
To accurately assess the SPOGC effect on the switching behaviour of GaN-HEMTs, it is crucial to extract the circuit parasitic parameters and incorporate them into the SPICE simulation. In this subsection, the parasitic parameters extraction of a half-bridge circuit (for double-pulse test) will be illustrated using the measurement and electromagnetic (EM) simulation methods.

4.2.1.1 C_{oss} of gate driver extraction using impedance analyzer

To determine the non-linear C_{oss} of the N-channel MOSFETs inside the gate driver, a impedance analyzer (4294A) is employed. A measurement board is required to ensure the gate driver state remains the same as that during turning on. For example, the source output is high and sink output is open. A 6 V voltage is required as well to supply the V_{DD} of gate driver during the measurement to avoid triggering the under



(a)



(b)

Figure 4.11: Schematic of the customised single (a) and split output (b) gate configurations of half-bridges for the switching behaviour simulation in SPICE.

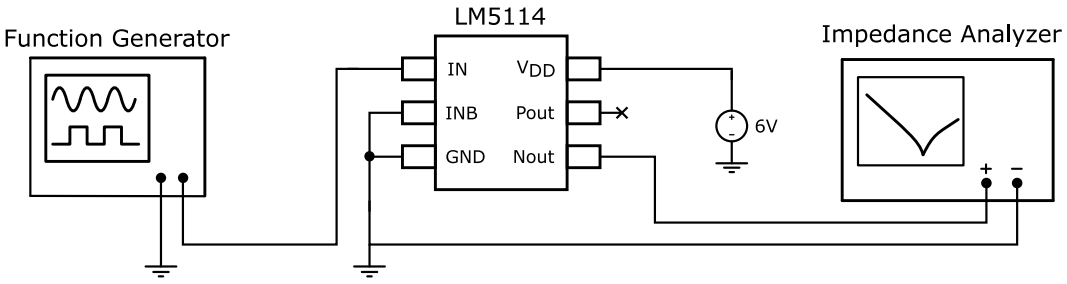


Figure 4.12: Schematic of the measurement method for the C_{oss}^{NMOS} in the gate driver LM5114.

voltage lockout (UVLO) function. Additionally, the DC bias function in the impedance analyzer is utilised to provide voltage bias on the C_{oss}^{NMOS} of the gate driver to measure its voltage-dependent non-linear capacitance. The schematic of the measurement setup for the LM5114 [157] is shown in Fig. 4.12, based on the structure of the gate driver provided by the datasheet, the impedance between the "Nout" and "GND" pins can be measured as the C_{oss}^{NMOS}. The measurement setup and measurement board for gate driver is displayed in Fig. 4.13.

When the pins of the gate driver are connected and supplied as mentioned above, the measured impedance can be seen as the C_{oss}^{NMOS} of the gate driver. The measured impedance under different V_{DC} bias provided by the impedance analyzer is shown in Fig. 4.14, where the $-90\,\text{deg}$ phase confirms a capacitive behaviour of the results. The capacitance under different V_{DC} bias is calculated based on the measured impedance from 1 MHz to 10 MHz, and the $C-V$ characteristics is drawn in Fig. 4.15, showing a typical inverse voltage behaviour.

The C_{oss}^{NMOS} of LM5114 can reach up to 140 pF under zero voltage bias, which is comparable to the C_{iss}^{GaN} as listed in Table 4.1. Additionally, the gate driver 1EDN7511B is tested using this method, showing a 118 pF C_{oss}^{NMOS} in the same conditions. The measured values of C_{oss}^{NMOS} from different gate drivers supports that this is not an isolated case.

To consider this $C-V$ characteristics of C_{oss}^{NMOS} of the gate driver in the SPICE simulation, the non-linear capacitor model is adopted to fit the measured $C-V$ characteristics, as shown in eq. 4.2:

$$C(V) = \frac{C_0}{(1+\frac{V}{V_0})^m} \tag{4.2}$$

where the C_0, V_0 and m are parameters to be fitted. The fitting result is displayed in Fig. 4.15. Afterward, the obtained model is used as the C_{oss}^{NMOS} of the gate driver in the SPICE simulation. To be noted that the capacitor has to be converted to charges in the SPICE environment and the corresponding equation will be displayed in Fig. 4.22. The value of C_{oss}^{PMOS} is set to 60 pF, although it will not influence the charging process of C_{iss}^{GaN}.

In addition, the non-linear junction capacitance of Schottky diode (C_{SD}) in the single

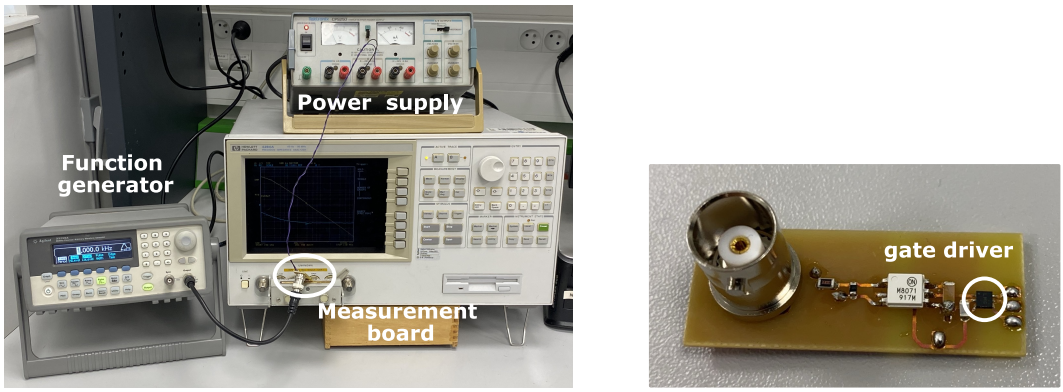


Figure 4.13: Measurement setup and measurement board for the C_{oss}^{NMOS} in the gate driver.

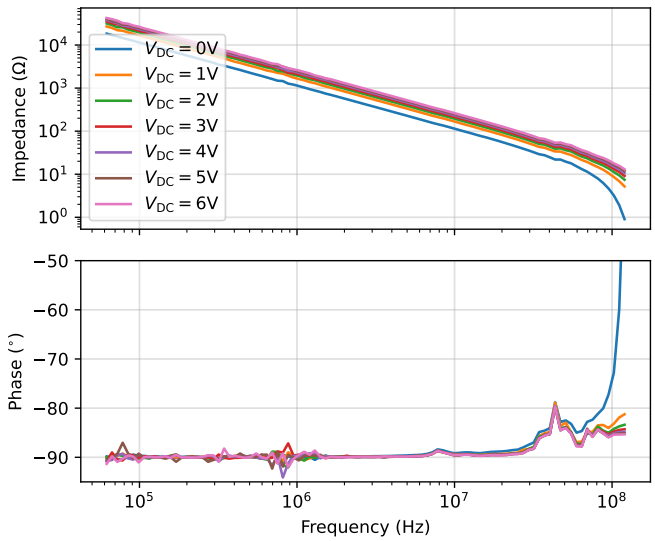


Figure 4.14: Measured impedance of the gate driver LM5114 using impedance analyzer.

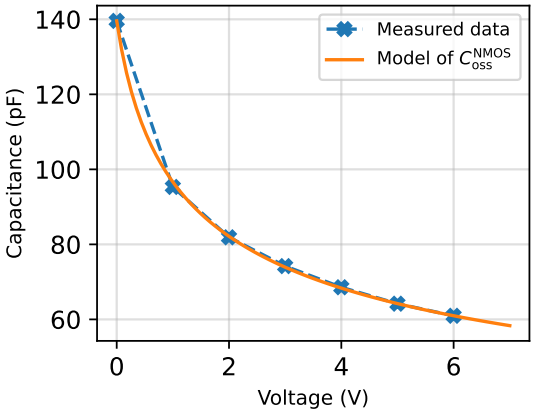


Figure 4.15: Measurement and modelling results of C_{oss}^{NMOS} in LM5114 gate driver.

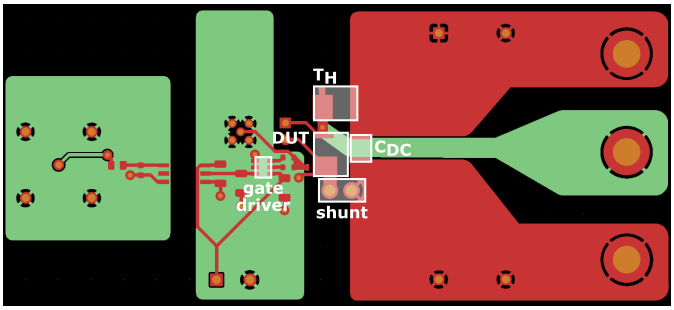
output gate configuration is measured and modelled using the same method as C_{oss}^{NMOS} of LM5114, since this C_{SD} could also influence the switching charging process of C_{iss}^{GaN} and the simulation results from single output topology will be compared to those from the split output topology. At turn-on transient, the charge of C_{SD} can allow part of the rising edge of gate driver output current flowing through the R_g^{off} branch for a short time, accelerating the charging speed of C_{iss}^{GaN}. However, the Schottky diode is not required in the split output configuration, which means that the impedance of turn-off loop in split output configuration is higher than the single output configuration for the rising edge from gate driver, when the L_g^{off} and R_g^{off} are the same in these two configurations. Therefore, the C_{SD} can amplify the switching behaviour variation caused by the SPOGC effect when comparing these two gate configurations.

By measuring and incorporating these important non-linear capacitances from both gate configurations into the SPICE simulation, the accuracy of switching behaviour analysis can be improved. Additionally, the value of parasitic inductance in the gate and power loops is critical for accurately evaluating the impact of the SPOGC effect on the switching behaviour of GaN-HEMTs. The extraction process will be detailed below.

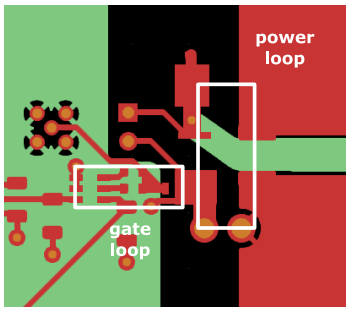
4.2.1.2 Parasitic inductance extraction for power and gate loops of half-bridge

Although it is beneficial to obtain the actual L_g in turn-on and turn-off loops, accurate measurement for L_g^{on} and L_g^{off} is challenging due to their extremely low value (a few nH) and the complex measurement calibration process. Therefore, extracting the parasitic inductance using the electromagnetic (EM) simulation software is widely adopted. In this work, the Advanced Design System (ADS) software from Keysight is employed to extract the parasitic inductance of power loop L_d and gate loop L_g based on the PCB layout.

The PCB layout of the half-bridge (main board) in Fig. 3.9 is utilised to extract the parasitic inductances. The PCB trace and main components are displayed in Fig. 4.16(a),



(a)



(b)

Figure 4.16: PCB layout of the half-bridge (presented previously in Fig. 3.9) with highlighted (a) main components and (b) power and gate loops.

where the gate and source of T_H are shorted to represent a freewheeling diode. The power loop consists of the PCB trace circulated by the T_H and DUT, current shunt, and DC decoupling capacitor C_{DC}. The gate loop is composed from the output of the gate driver, R_g, the source of the DUT, and the GND of the gate driver, as shown in Fig. 4.16(b).

Parasitic inductance extraction for gate loop

The PCB design file (Gerber) can be imported to the ADS to implement the EM simulation, after this, an EM model of the gate loop PCB trace can be obtained. This model can be further utilised in S-parameter simulation to extract the gate loop parasitic inductance L_g [154].

In the EM simulation, the substrate is defined as a two-layer PCB, with 35 µm of copper on both the top and bottom layers and a 1.6 mm FR4 dielectric layer. The top and bottom layers are connected through vias, which are also defined in the substrate. The substrate and 3D momentum model of the gate loop are displayed in Fig. 4.17, where the turn-off loop is depicted through the R_g^{off} (turn-on loop is through the R_g^{on}). The momentum RF simulator is adopted for the EM simulation with sweeping frequency from 1 kHz to 1 GHz, afterward, an EM model of the gate loop is obtained.

To extract the L_g, this obtained EM model can be utilised for a S-parameter simula-

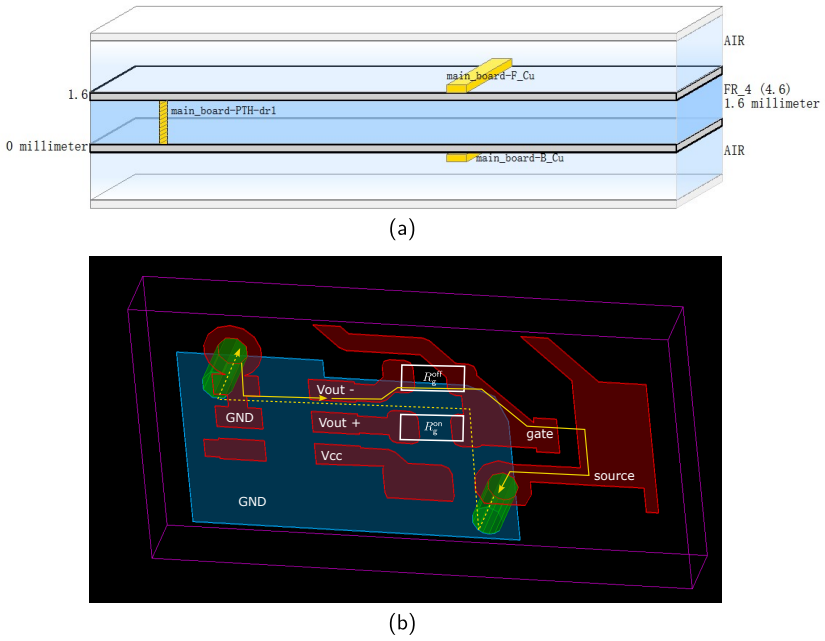


Figure 4.17: Setup of the EM momentum simulation in ADS (a) substrate (b) 3D model of the gate loop layout with turn-off loop highlighted.

tion. The two-layer PCB can be basically assumed as a 2-port network. To conveniently extract the parasitic inductance, it can be converted to a 1-port network by shorting one port, where the schematic of the connection is depicted in Fig. 4.18.

After the S-parameter simulation, the input impedance (Z_{in}) can be calculated by eq. 4.3:

$$Z_{\text{in}} = Z_0 \cdot \frac{1 + S_{11}}{1 - S_{11}} \tag{4.3}$$

where Z_0 is the reference impedance of the system (normally 50 Ω) and S_{11} is the reflection coefficient of the 1-port network. In ADS, this calculation can be directly achieved by calling the Z_{in} function. The parasitic inductance can be calculated by eq. 4.4:

$$L_{\text{para}} = \frac{\text{Im}(Z_{\text{in}})}{2\pi f} \tag{4.4}$$

L_{g}^{on} and $L_{\text{g}}^{\text{off}}$ (identified to those in Fig. 4.11) can be extracted using this method, and their values versus frequency are displayed in Fig. 4.19, where $L_{\text{g}}^{\text{off}}$ is higher than L_{g}^{on} due to the relative large loop as displayed in Fig. 4.18. Based on the commutation time of GaN-HEMTs in Fig. 3.33, an equivalent frequency f_{eq} can be considered to extract the inductance value, as:

$$f_{\text{eq}} = \frac{1}{\pi t_{\text{r}}} \tag{4.5}$$

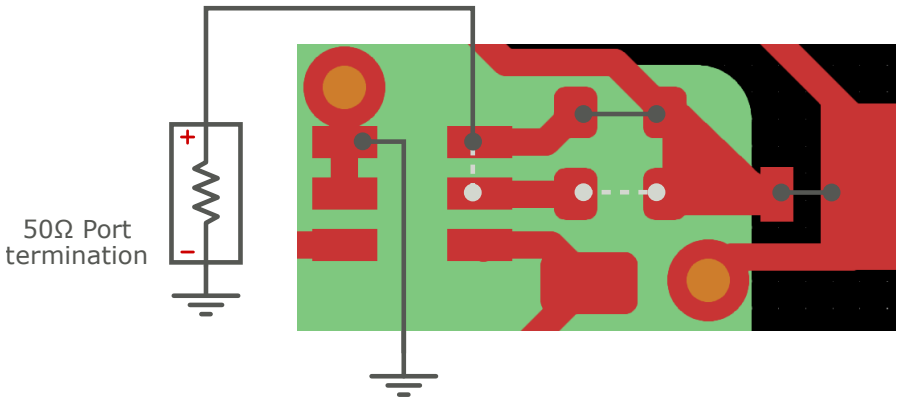


Figure 4.18: Connection of gate loop layout for L_g^{off} extraction (light grey colour for L_g^{on}) using S-parameter simulation (1-port network).

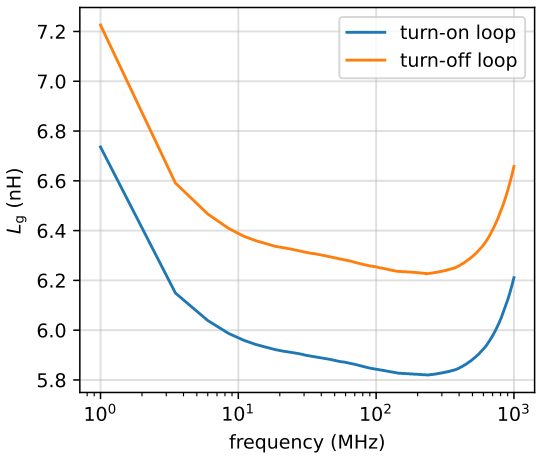


Figure 4.19: Extracted L_g^{on} and L_g^{off} using S-parameter simulation in ADS.

$R_g^{on} = 330\,\Omega$	$R_g^{off} = 2\,\Omega$	$L_g^{on} = 5.9\,nH$	$L_g^{off} = 6.3\,nH$
$V_{DC} = 100\,V$	$t_r = 2\,ns$	$L_d = 7\,nH$	

Table 4.8: SPICE simulation parameters for the DPT based hard-switching in slow switching.

and the equivalent frequency can take values from 60 MHz to 80 MHz. Therefore, the parasitic inductances at 80 MHz are collected with $L_g^{on} = 5.9\,nH$ and $L_g^{off} = 6.3\,nH$.

Parasitic inductance extraction for power loop

A similar process can be repeated to extract the power loop parasitic inductance L_d, except the substrate setup in the EM momentum simulation. As displayed in Fig. 4.16(b), the power loop consists of a single-layer PCB trace. Therefore, the substrate should be adjusted as shown in Fig. 4.20, where a 35 µm of copper on the FR4 dielectric is set as the conductor layer (main_board−F_Cu). To consider this conductor layer as the single-layer PCB trace, a 1 cm of AIR layer is added on the top of the bottom layer (conductor as well) to isolate its electromagnetic field influence on the top side copper layer [154].

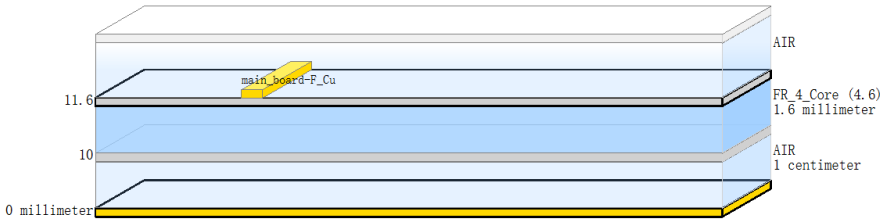


Figure 4.20: Substrate setup for the power loop in the EM momentum simulation.

After the EM simulation, the obtained model of power loop trace can be used for the S-parameter simulation and the L_d can be extracted using the same process as discussed above. The extracted L_d is displayed in Fig. 4.21, where $L_d = 7.0\,nH$ at 80 MHz.

4.2.2 SPICE simulation results

The hard-switching simulation based on the schematics in Fig. 4.11 are adopted to evaluate the influence of SPOGC effect on the switching behaviour of GaN-HEMTs by comparing the switching waveforms of DUTs driven by the single and split output gate configurations. The essential parasitic circuit parameters extracted in section 4.2.1 are incorporated in the simulation. The whole circuit and related parameters are displayed in Fig. 4.22.

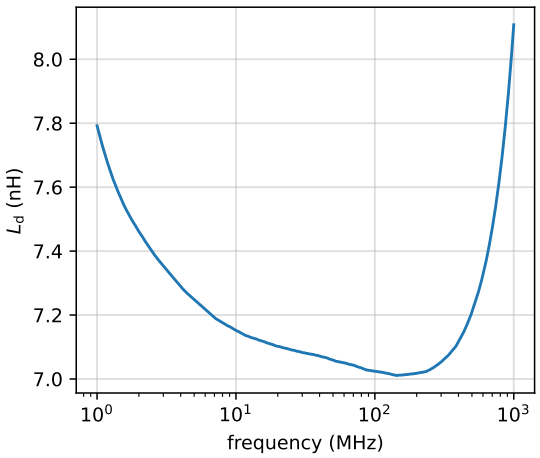


Figure 4.21: Extracted L_d using S-parameter simulation in ADS.

4.2.2.1 Slow switching condition

To understand how the switching waveforms are influenced by the SPOGC effect, a large R_g^{on} is used to reduce the turn-on commutation speed at first, where the influence of parasitic inductance can be eliminated, making the analysis more straightforward. The simulation parameters are listed in Table 4.8 and the simulation results are displayed in Fig. 4.23, where the turn-on switching transition driven by the split output gate configuration is extended compared to that driven by the single output gate configuration. This switching variation can be explained by the V_{gs} switching waveform that is affected by the SPOGC effect, where the C_{oss}^{NMOS} charging process diverts current from the C_{iss}^{GaN} charging loop, when using the split output gate configuration, leading a slow V_{gs} rise compared to the single output configuration. Importantly, the variation of V_{gs} between the threshold voltage V_{th} and plateau voltage V_{pl} can influence the commutation behaviour of I_d and V_{ds}. By noting the V_{th} and V_{pl} of the SG66502B in the V_{gs} waveform and highlighting these two time intervals in Fig. 4.23, the extended rise time of the V_{gs} can be observed in the split output gate configuration, by comparing the width of the blue (single) and orange (split) areas. The time interval from V_{th} to V_{pl} determines the rising time of I_d, therefore, the commutation time of I_d in split output waveform is extended, leading to the decreased dI_d/dt from 0.75 A/ns in single output to 0.56 A/ns in split output. Moreover, the reduced ΔV_{ds} in the split output configuration in the highlighted areas can be observed, from 6.6 V to 5.0 V, which is also due to the decreased dI_d/dt.

4.2.2.2 Fast switching condition

Evaluating the SPOGC effect under fast switching conditions is crucial, as the influence of parasitic circuit parameters becomes more pronounced, and fast switching is a typical operating condition for GaN-HEMTs. The above simulation is reimplemented

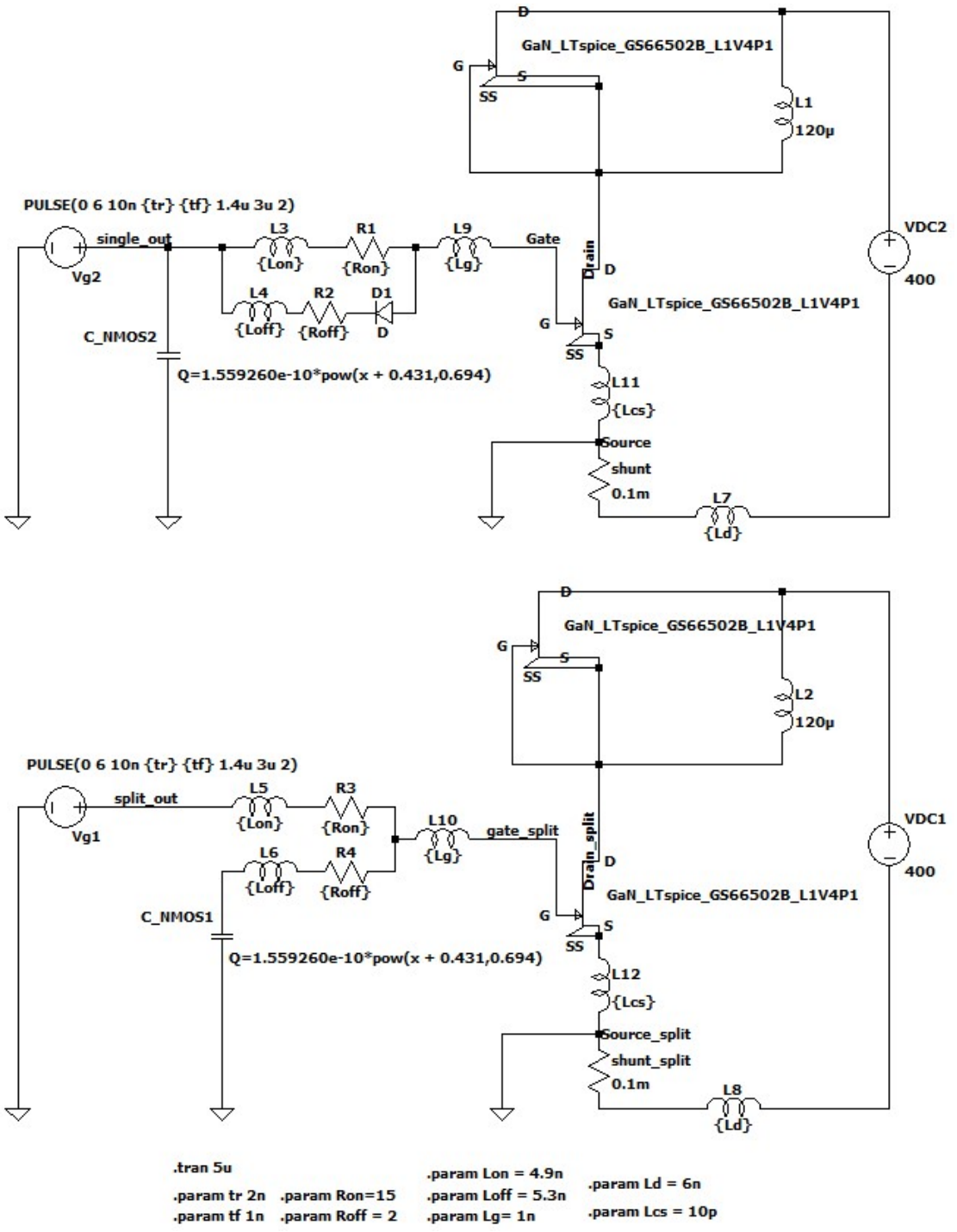


Figure 4.22: Schematic and Simulation Parameters Setup in LTspice for Single- and Split-output Gate Driver Based Hard-switching

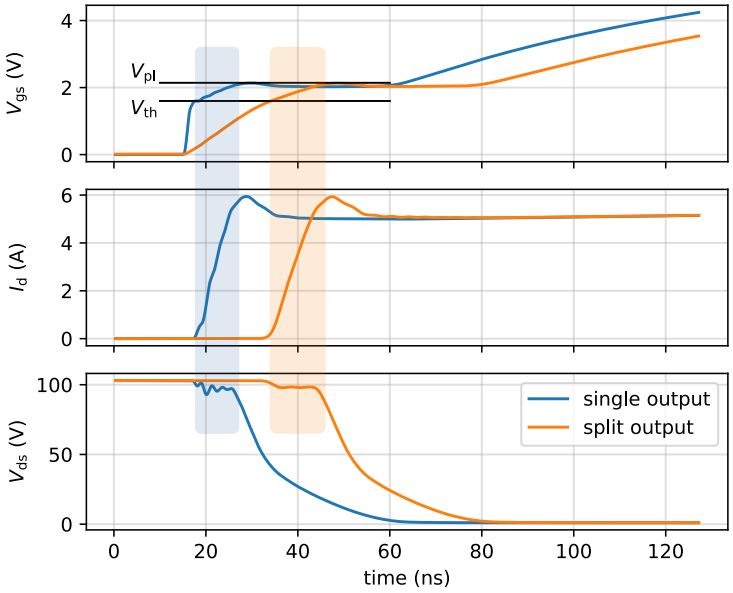


Figure 4.23: Turn-on simulation waveforms of the GaN-HEMTs driven by the single and split output gate configurations in slow switching condition.

by adjusting the R_g^{on} from 330 Ω to 15 Ω and increasing the V_{DC} from 100 V to 400 V, corresponding to a more practical switching commutation for GaN-HEMTs, other simulation parameters remain the same as in Table 4.8. The simulation results are shown in Fig. 4.24, where the turn-on switching waveforms driven by the split output configuration are extended. Due to the prolonged V_{gs} rise time from V_{th} to V_{pl} in the split output topology, the rising stage of I_d is extended, simultaneously, the V_{ds} reduce slowly because of the reduced dI_d/dt. This effect is similar to what occurs under slow switching conditions, indicating the influence of SPOGC effect on the switching waveforms a common phenomenon.

To assess the impact of slowed-down commutation on turn-on losses, turn-on switching power (P_{on}) and turn-on switching energy (E_{on}) are calculated based on the I_d and V_{ds} waveforms from the split output gate configuration simulation, revealing an approximately 6.5 % increase in E_{on} compared to the single output configuration.

The simulation results suggest that the split output gate configuration could slow down the turn-on commutation speed of the GaN-HEMTs due to the SPOGC effect, leading to higher turn-on losses. This effect is primarily attributed to the V_{gs} variation that is determined by the charging speed of C_{iss}^{GaN} in different gate configurations. However, to further demonstrate the existence of SPOGC effect and its influence on the switching behaviours of GaN-HEMTs, the experimental verification is necessary.

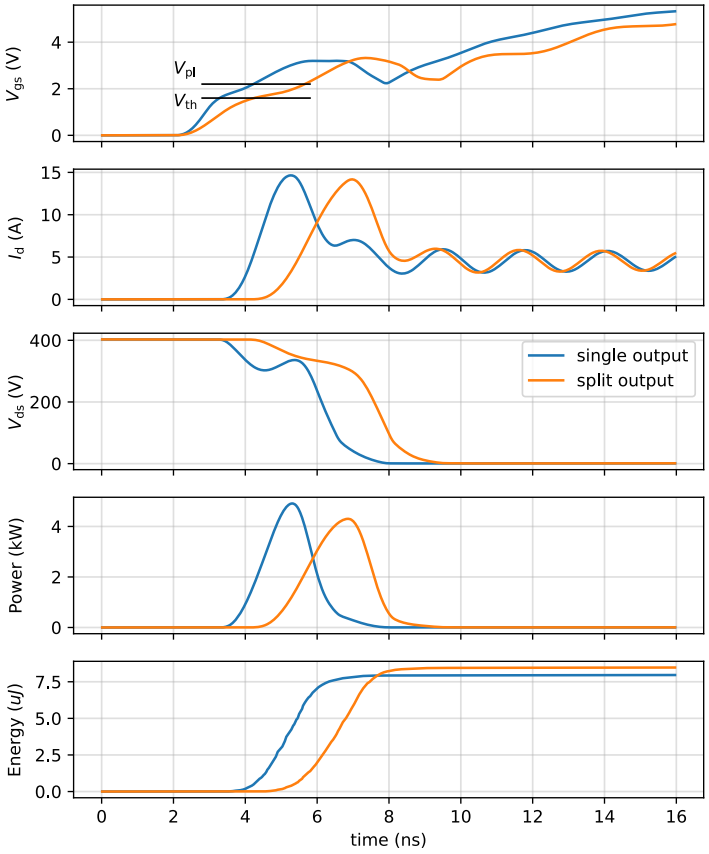


Figure 4.24: SPICE simulation waveforms of the GaN-HEMTs driven by the single and split output gate configurations in turn-on commutation.

4.3 Experimental validation

In this section, the influence of SPOGC effect on the switching behaviour of GaN-HEMTs is experimentally validated. The objective is to demonstrate the existence of this effect in the real application of GaN-HEMTs.

4.3.1 Experiment setup

The half-bridge based DPT with the same schematic in Fig. 4.11 is employed to evaluate the hard-switching transition of GaN-HEMTs driven by gate drivers with different output topologies, where GS66502B is adopted as the power transistors, and the LM5114 gate drive is adopted. The PCB layout with the essential components are also displayed in Fig. 4.16.

4.3.1.1 Gate driver modification

To demonstrate the impact of different gate driver output topologies on the switching waveforms of GaN-HEMTs, two gate drivers with identical electrical characteristics but different output topologies (single and split) are required. However, finding such gate drivers is challenging. Additionally, the pin distributions of single and split output gate driver packages do not match, making it difficult to drive the GaN-HEMTs with the same circuit parasitic parameters, such as L_g, when using two different gate drivers.

To address this issue, the "Nout" and "Pout" pins of LM5114, as shown in Fig. 4.12, are connected together to function as a single output gate driver. The rising edge of output voltage of "Pout" pin from the original (split) and modified (single) LM5114 are compared in Fig. 4.25, where the gate driver's operating voltage (V_{DD}) is set to 6 V, with C_{iss}^{GaN} of GS66502B as the load capacitor. As displayed, the rising edge of the output voltage before and after the modification remains nearly identical. It should be noted that the rise time of gate driver t_r^g is around 2 ns, supporting the simulation setting adopted in section 4.2.2. This approach allows for the evaluation of the influence of the gate driver output topology on the switching behaviour of GaN-HEMTs, while minimizing the impact of varying electrical characteristics between different gate drivers. For the single output gate circuitry, only a Schottky diode is required to be added in the turn-off loop as shown in Fig. 4.1. Consequently, all electrical characteristics of the single and split output gate drivers, as well as the circuit parasitic parameters in both gate configurations, are matched as similar as possible.

4.3.1.2 Eliminating the influence of V_{ds} bias induced V_{th} shift

The conventional DPT is adopted for the experimental validation in hard-switching. However, the long-term V_{ds} bias present in the conventional DPT can cause a positive V_{th} shift, which could affect the switching behaviour of GaN-HEMTs, as discussed in Chapter 3. To mitigate this influence, the DUT is biased for 2 minutes under the DC voltage (V_{DC}) before starting the test in both single and split output gate configurations.

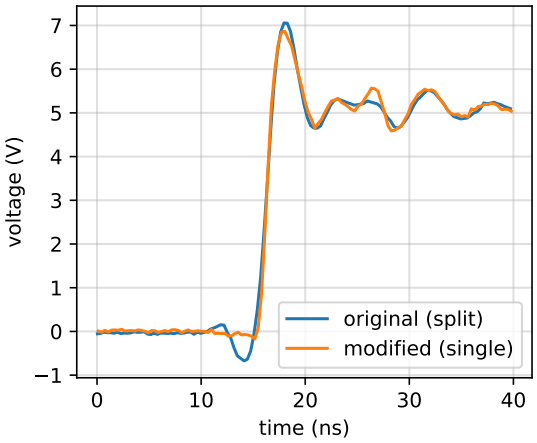


Figure 4.25: Comparison of the rising edge of output voltage of "Pout" pin from the original (split) and modified (single) LM5114 with the C_{iss} of GS66502B as the load.

This ensures that the V_{th} of the DUT is saturated and remains consistent across all test conditions, therefore, the influence of V_{th} shift on the switching behaviours can be neglected in the following tests.

4.3.2 Measurement results

The measured switching waveforms of the GS66502B are presented in this subsection to validate the previous simulation analyses about how the SPOGC effect influence the switching behaviour of GaN-HEMTs. Additionally, both slow and fast switching conditions are tested to demonstrate the generality of this phenomenon.

4.3.2.1 Slow switching condition

The R_g^{on} and R_g^{off} are respectively set as 330 Ω and 2 Ω for the slow switching condition, and the V_{DC} is set as 100 V. These parameters are the same as for the simulation presented on Fig. 4.23. Due to the ultra-fast switching speed of GaN-HEMTs (mainly for the fast switching condition measurement below), high bandwidth probes are required to measure the switching waveforms. The V_{gs} and V_{ds} are respectively measured by the 500 MHz (TIVH05) and 1 GHz (TIVP1) galvanically-isolated probe from Tektronix, and a 1.2 GHz current shunt (SSDN-015) is used to measure the fast switching transition of I_d. The switching waveforms are displayed in Fig. 4.26, where the rising time of V_{gs} is clearly extended by the split output gate configurations. Consequently, the I_d in the split output configuration begins to rise later than in the single output, as it takes longer for the C_{iss}^{GaN} to charge to the V_{th} value. Additionally, the rising slope of I_d in the split output is reduced due to the extended time period between V_{th} and the plateau voltage V_{pl}, where the dI_d/dt reduced from 0.33 A/ns to 0.27 A/ns showing a 18.2 % reduction. This reduction in the dI_d/dt also mitigates the corresponding drop in V_{ds}. The experimental

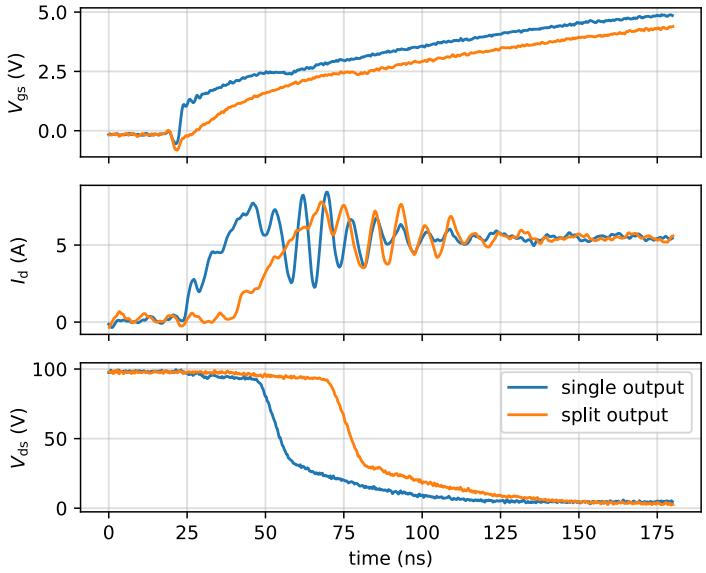


Figure 4.26: Comparison of measured turn-on switching waveforms of GaN-HEMTs driven by the single and split output gate configurations in slow switching with R_g^{on} = 330 Ω and R_g^{off} = 2 Ω.

results align well with the previous simulations, confirming the impact of the SPOGC effect on the turn-on switching transitions under slow switching conditions.

4.3.2.2 Fast switching condition

It is essential to evaluate the influence of SPOGC effect during the fast switching condition, since the SPOGC effect is very sensitive to the parasitic circuit parameters in the fast switching transition. Additionally, the fast switching is a typical characteristic of GaN-HEMTs and assenting the existence of SPOGC effect in this condition is valuable for applying the devices in high-frequency power converters.

To achieve a practical application scenario for the 650 V GaN-HEMTs in power converters, R_g^{on} is reduced to 15 Ω, and V_{DC} is increased to 400 V. Other circuit parameters and measurement probes are remained the same as the slow switching test. The measured turn-on switching waveforms are displayed in Fig. 4.27, where the switching waveforms driven by the split output configuration are still slowed down by the SPOGC effect as presented in the simulation and slow switching experiment. This result indicates that the influence of SPOGC effect on the switching behaviour of GaN-HEMTs still exist, although with a severe impact of parasitic circuit parameters in the fast switching condition. To further evaluate the influence of SPOGC effect on the switching losses, the switching power and energy are calculated. The GaN-HEMTs driven by the split output gate configuration shows an approximately 5.1 % of increased E_{on} when compared to the value for the single output gate drivers. Additionally, the $^{dI_d}/_{dt}$ of the first current

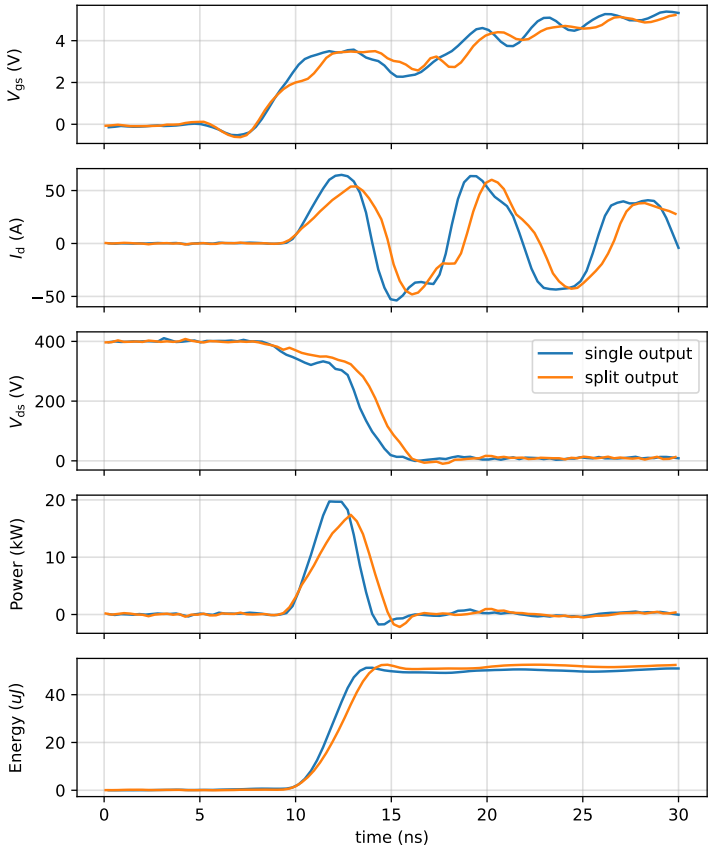


Figure 4.27: Comparison of measured turn-on switching waveforms and calculated turn-on losses of GaN-HEMTs driven by the single and split output gate configurations using LM5114 in fast switching with $R_g^{on} = 15\,\Omega$ and $R_g^{off} = 2\,\Omega$.

overshoot is calculated, showing 29.67 A/ns in the single output configuration, which is reduced to 15.66 A/ns in the split output configuration. This represents a 47.2 % reduction in $^{dI_d}/_{dt}$, attributed to the SPOGC effect. It also should be noted that similar comparison tests under different V_{ds} from 100 V to 400 V are implemented as well, showing the same phenomenon. Therefore, the EMI generated by the GaN-HEMTs might be reduced when they are driven by the split output gate configuration.

To demonstrate the universality of the SPOGC effect, the gate driver LM5114 is replaced by the 1EDN7511 from Infineon to drive the same GS66502B device, with remaining other experiment parameters the same. To be noted these two gate drivers have the same package and footprint. The C_{oss}^{NMOS} of 1EDN7511 was measured using the same method and the value under zero voltage bias is 118 pF, as mentioned in section 4.2.1.1. The turn-on switching waveforms is displayed in Fig. 4.28, which showing the similar effect as that driven by the LM5114.

By comparing the measured switching waveforms under slow and fast switching

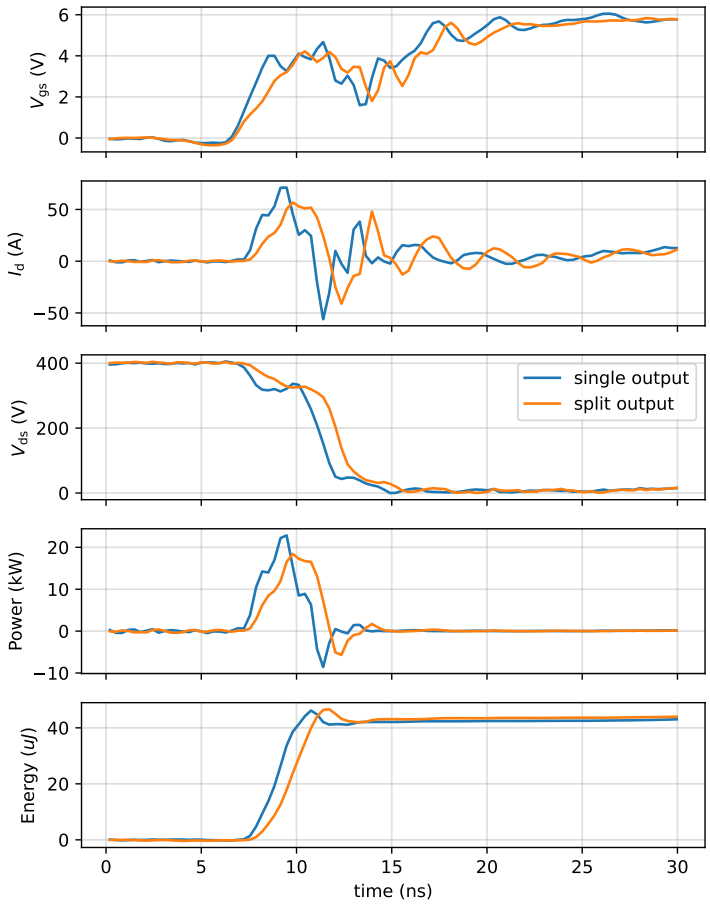


Figure 4.28: Comparison of measured turn-on switching waveforms and calculated turn-on losses of GaN-HEMTs driven by the single and split output gate configurations using 1EDN7511 in fast switching with $R_g^{on} = 15\,\Omega$ and $R_g^{off} = 2\,\Omega$.

conditions, slight variations in the V_{gs} are observed, although the split output configuration slows down the V_{gs} in both cases. In slow switching, the variation between V_{gs} in the single and split output configurations appears as long as V_{gs} begins to rise. In contrast, during fast switching, the variation only becomes noticeable after V_{gs} approximately exceeds V_{th}, at which point I_d rises almost simultaneously in both configurations. Also, this phenomenon does not appear in the fast switching simulation. This variation could be attributed to the simplified parasitic inductance model of L_g and the neglected common source inductance L_{cs} and mutual inductive coupling effect, these inductances could further resonate with the parasitic capacitances in the gate loop, making the charging process of V_{gs} more complicated.

To summarise, the split output gate configuration can slow down the turn-on commutation speed of GaN-HEMTs due to the relative large C_{oss}^{NMOS}, particularly affecting the V_{gs} and I_d waveforms, whether under fast or slow switching conditions. This reduction in commutation speed can lead to higher switching losses, though it may also result in lower EMI. The trade-off should be carefully considered in the design of GaN-based power converters. Furthermore, the value of C_{oss}^{NMOS} and effects similar to the SPOGC effect are not mentioned in the gate driver datasheets—at least for the gate drivers examined in this work. This study suggests that the output capacitance of gate drivers, particularly when using the split output configuration, should be considered as an important parameter for GaN-HEMTs application.

4.4 Discussion and conclusion

In this work, the driving performance of the single and split output gate drivers for power GaN-HEMTs is investigated via simulation and experimentation. It was demonstrated that the output capacitance of the n-type MOSFET (C_{oss}^{NMOS}) in the split output gate driver can slow down the turn-on commutation speed of GaN-HEMTs compared to that in the single output gate driver. This occurs because the C_{oss}^{NMOS} in the split output gate driver can divert the charging current from the input capacitance of the GaN-HEMTs (C_{iss}^{GaN}), leading to a slower charging speed of C_{iss}^{GaN}, this effect is defined as the SPOGC effect in this study. This effect is prevalent in any split output gate drivers but it is not as pronounced when driving the Si-MOSFETs, as the input capacitance of power MOSFETs (C_{iss}^{MOS}) is significantly larger than the C_{oss}^{NMOS} in the gate driver. Consequently, the charging process of C_{iss}^{MOS} is not substantially affected by the C_{oss} of gate driver, leading to the SPOGC effect being largely overlooked when driving the power Si-MOSFETs. However, due to the reduced C_{iss} values encountered in power GaN-HEMTs, the SPOGC effect becomes more noticeable because the values of C_{iss}^{GaN} and C_{oss}^{NMOS} are comparable. Simulation analysis indicates that the impedance ratio of the C_{iss}^{GaN} and C_{oss}^{NMOS} charging loops in the split output configuration is the primary determinant of the extent of the SPOGC effect. However, the parasitic inductance in the gate loop L_g could resonate with these capacitances, making the charging process of C_{iss}^{GaN} more complicated.

Moreover, the SPOGC effect should be accounted for the accurate switching be-

haviour modelling, neglecting the influence of C_{oss}^{NMOS} could lead to mismatched switching waveforms especially for the V_{gs}.

The SPOGC effect can slow down the commutation speed of GaN-HEMTs, especially for the V_{gs} and I_d waveforms, resulting an increased turn-on losses and reduced dI_d/dt. This effect has been demonstrated using the DPT based hard-switching experiment in both slow and fast switching. The influence of SPOGC effect on the switching behaviour should be considered when designing the GaN-based power converters, as the split output gate driver is widely adopted to achieve a compact gate loop (the Schottky diode is not required when using this gate driver) and avoid the false-turn on phenomenon of GaN-HEMTs.

Additionally, the SPOGC effect warrants greater attention from gate driver manufacturers and should be highlighted in their datasheet. For instance, providing the values of C_{oss}^{NMOS} and C_{oss}^{PMOS} in split output gate drivers would help engineers to assess the impact of the SPOGC effect when designing GaN-based power converters. This information would be valuable for optimising designs and ensuring reliable performance in power converter applications.

Conclusion and perspectives

To address the challenges of reliability and high efficiency in GaN-based power converters, this thesis conducted an in-depth investigation into the V_{th} shift phenomenon and the switching behaviour of GaN-HEMTs. Additionally, the influence of gate driver output capacitance on the switching transition of GaN-HEMTs has been discussed. The research reveals that Schottky-type GaN-HEMTs exhibit a significant positive V_{th} shift after the V_{ds} bias, and both this positive V_{th} shift and gate driver output capacitance could slow down the turn-on commutation speed of GaN-HEMTs in the half-bridge circuit based applications.

Based on the state-of-the-art research requirements for power GaN-HEMTs, chapter 1 showed that it is essential to characterise the V_{ds} bias induced V_{th} shift phenomenon and investigate its impact on the switching behaviour. Moreover, special attention should be given to the parasitic parameters in the entire gate loop when analysing the switching performance of GaN-HEMTs, as these parameters could significantly influence device operation.

In the second chapter, the off-state V_{ds} bias induced V_{th} shift phenomenon has been characterised for both Schottky-type GaN-HEMTs and GITs based on a proposed half-bridge compatible in-situ V_{th} shift measurement method. The single pulse test result shows that the Schottky-type GaN-HEMTs exhibit a significantly positive V_{th} shift after an extended bias time, while the V_{th} of GITs shows a slightly negative V_{th} shift. A V_{th} dropping phenomenon is observed for the Schottky-type device under approximately 1 s of 200 V above V_{ds} bias, which is not reported in the literature. Additionally, the shifted V_{th} of Schottky-type device requires several tens of hours to fully recover, while the GITs show a fast recovery of less than one minute. Moreover, an over-recovery phenomenon is observed in the Schottky-type device following an extended high-voltage single-pulse V_{ds} bias. The new findings of the V_{th} dropping and over-recovery phenomena are attributed to the hole trapping under the extended time and high amplitude of V_{ds} bias. In the continuous mode test, the V_{th} of Schottky-type GaN-HEMTs and GITs respectively exhibits an increasing and decreasing trend, as the number of operating cycles increases, eventually reaching stabilisation in a steady state, which represents the outcome of the interplay between trapping and de-trapping mechanisms. The steady state V_{th} of GaN-HEMTs is influenced by several factors, including switching frequency, duty cycle, and voltage bias amplitude. It should be noted that the over-recovery phenomenon not occurs after the continuous mode test under the same V_{ds} bias amplitude and

duration for the same Schottky-type device. This variation indicates the presence of distinct mechanisms related to the V_{th} shift and highlights the necessity of conducting both single and continuous modes of testing. To sum up, the V_{th} shift phenomenon of the Schottky-type GaN-HEMTs is significant, where the maximum ΔV_{th} reaches to approximately 0.8 V (considering the over-recovery phenomenon) for the same sample. Under the same condition, the maximum ΔV_{th} of GITs is relative low in around 0.4 V. To the best knowledge of the author, this is the first characterisation of off-state V_{ds} bias induced V_{th} shift for GITs using both single- and multi-pulse tests, benefiting from the proposed straightforward V_{th} measurement method. However, to evaluate the V_{th} shift phenomenon of GaN-HEMTs in multi-megahertz, the measurement response time t_m of the proposed method requires to be reduced further, whereas the channel current of the DUT should be limited to control the junction temperature T_j. Future work will be performed on the adjustable RL load to address above mentioned limitations.

In the third chapter, the impact of V_{th} shift on the switching behaviour of GaN-HEMTs has been investigated. By employing the H-bridge based double-pulse test setup and utilising the high-voltage and high-current $I-V$ characteristics, two types of V_{ds} bias induced V_{th} shift are revealed. Subsequently, the impact of V_{th} shift on the switching behaviour is demonstrated followed by the process of theoretical analysis, simulation and experimental validation. The result shows that the I-type V_{ds} bias induced positive V_{th} shift can slow down the turn-on commutation speed of GaN-HEMTs, leading to higher turn-on switching energy and reduced dI_d/dt and dV_{ds}/dt. Meanwhile, the II-type V_{ds} bias induced negative V_{th} shift could influence the switching behaviour as well, especially for the V_{gs} waveforms. The turn-off switching transition is independent of the V_{th} shift if the channel current drops to zero rapidly before the mechanisms mentioned above occur. However, the positive V_{th} shift could accelerate the turn-off transition in the slow commutation condition. The influence of V_{th} shift on the switching behaviour of Schottky-type GaN-HEMTs is demonstrated and evaluated, however, its impact on the GITs is different.

In the last chapter, the impact of the gate driver output capacitance on the switching behaviour of GaN-HEMTs has been examined, focusing on the single and split output gate configurations. In the split output gate configuration the output capacitance gate driver can divert the charging current of C_{iss} in GaN-HEMTs, resulting in a slower charging speed of C_{iss}. This influence is defined as the SPOGC effect in this study, and it does not occur in the single output gate configuration. The current diversion can slow the rise of V_{gs} and extend the commutation times of V_{ds} and I_d when GaN-HEMTs are driven by split output gate drivers. Both simulation and experimental methods are used to validate the influence of SPOGC effect on the switching behaviour of GaN-HEMTs, employing both slow and fast commutation test conditions. It should be noted that this phenomenon is often overlooked when driving power MOSFETs, as the C_{iss} of power MOSFETs is several orders of magnitude larger than the gate driver's C_{oss}. However, this effect becomes significant in the accurate evaluation and modeling of switching waveforms for GaN-HEMTs due to their significantly reduced C_{iss}. Moreover, the value and effect of the gate driver output capacitance are not mentioned in the datasheet,

although, they are important to assess the commutation behaviour of GaN-HEMTs. The study in this chapter showed that the switching behaviour of GaN-HEMTs is very sensitive to the circuit parasitic parameters. Additionally, the distributed parasitic inductance in these loops, along with the mutual inductive coupling effect, can influence the SPOGC effect under fast commutation conditions. Moreover, the rise time of the gate driver for GaN-HEMTs becomes shorter, making the parasitic inductance's role more significant. Consequently, future work will focus on the SPOGC effect considering the faster commutation speed and more complex inductive effects

In conclusion, the lateral structure and unique material properties of GaN-HEMTs result in low losses and high-frequency application capabilities. However, these characteristics are susceptible to the V_{th} shift phenomenon and show sensitivity to parasitic parameters, both of which can significantly impact the switching behaviour of GaN-HEMTs. These phenomena are not pronounced in Si- or SiC-MOSFETs, and most of the characterisation and driving techniques for GaN-HEMTs are inherited from MOSFETs, leaving knowledge gaps similar to those discussed in this work. Consequently, to further release the high-frequency and low losses of GaN-HEMTs, these regimes deserve more attentions in research and development of GaN-based power converters. Additionally, the trapping effect related parameter shift phenomenon could provide important informations in terms of the device reliability and life-time estimation, which can be a future research direction of this work.

Publications

(1) X. Lu, A. Videt, S. Faramehr, K. Li, V. Marsic, P. Igic and N. Idir, "Impact of V_{th} Instability of Schottky-Type p-GaN Gate HEMTs on Switching Behaviors," in IEEE Transactions on Power Electronics, vol. 39, no. 9, pp. 11625-11636, Sept. 2024, doi: 10.1109/TPEL.2024.3405320.

(2) X. Lu, A. Videt, N. Idir, V. Marsic, P. Igic and S. Faramehr, "Investigation on Single and Split Output Gate Configurations Influence on the GaN-HEMTs Switching Behaviours," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-9.

(3) X. Lu, A. Videt, K. Li, S. Faramehr, P. Igic and N. Idir, "Influence of Current Collapse due to V_{ds} Bias Effect on GaN-HEMTs $I_d - V_{ds}$ Characteristics in Saturation Region," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-9.

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