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Epitaxial growth and near-field characterization of InSb nanostructures for advanced electron devices

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Croissance épitaxiale et caractérisation champ-proche de nanostructures d'InSb pour composants électroniques avancés

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Expliquer toute la nature est une tâche trop ardue pour un seul homme ou une seule époque. Il est plus sage de faire peu en étant sûr de soi et laisser le reste à ceux qui viendront après, que présumer de tout sans être sûr de rien.

Isaac Newton

Rien dans la vie n'est à craindre, tout doit être compris. C'est maintenant le moment de comprendre davantage, afin de craindre moins.

Marie Curie

Epitaxial growth and near-field characterization of InSb nanostructures for advanced electron devices

Abstract

At the dawn of the quantum era, which promises radically new ways of processing information, III-V semiconductors — and InSb in particular — stand out as one of the most promising material for this transition. With high electron mobility, strong spin-orbit interaction, and small effective mass, InSb exhibits ideal properties for quantum applications such as Majorana-based devices, while also offering opportunities in high-performance nanoelectronics beyond quantum computing. However, the deployment to functional devices has been hampered by the strong lattice-mismatch of InSb to conventional III-V substrates, making the growth of defect-free nanostructures challenging. This thesis investigates the **Selective Area Growth (SAG)** of InSb nanostructures on both lattice-matched and highly mismatched substrates using **Molecular Beam Epitaxy (MBE)**. To enable the carrier density modulation required for quantum devices, InSb was also integrated within gated heterostructures incorporating semiconducting barriers.

This thesis work dealt with the InSb growth on lattice-matched CdTe substrates at the beginning, but technological limitations constrained the quality and scalability of the InSb nanostructures. The study then shifted to GaAs $(111)_B$ substrates, where growth optimization yielded high crystal quality thin films and planar nanostructures with low defect density, as confirmed by cross-sectional **Scanning Transmission Electron Microscopy (STEM)** and **Scanning Tunneling Microscopy (STM)**.
Following the optimized growth on GaAs $(111)_B$, high quality InSb thin-films and in-plane **nanowires (NWs)** were produced on low roughness GaInP buffer layers grown on GaAs under carefully optimized conditions. Through a structural and a morphological study, we then discussed the minor differences observed with the growth of InSb nanostructures on GaAs substrates. The final part of the thesis focused on electrical transport studies of the InSb/GaInP/GaAs:n+ heterostructure combining Hall measurements, **Transfer Length Method (TLM)**, and **Four-Probe Scanning Tunneling Microscopy (4P-STM)**. An effective charge density modulation inside the InSb nanostructures as well as a record-high electron mobility for InSb thin films grown on III-V mismatched substrate were demonstrated. A last comprehensive **Scanning Tunneling Spectroscopy (STS)** study revealed that precise control of surface integrity is essential to fully exploit the potential of these nanostructures.

Altogether, this work establishes a scalable route to high-quality InSb nanostructures, advancing both quantum device development and high-performance III–V nanoelectronics.

Keywords: InSb, III-V Heterostructures, Nanowires, Quantum transport, Selective Area Growth, Molecular Beam Epitaxy, Multiple-tip Scanning Tunneling Microscopy, Transport measurements

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Croissance épitaxiale et caractérisation champ-proche de nanostructures d'InSb pour composants électroniques avancés

Résumé

À l'aube de l'ère quantique, qui promet des modes de traitement de l'information radicalement nouveaux, les semi-conducteurs III-V — et en particulier l'antimoniure d'indium (InSb) — apparaissent comme des materiaux prometteurs pour contribuer à cette transition. Grâce à sa mobilité électronique élevée, son fort couplage spin-orbite et sa faible masse effective, l'InSb possède les propriétés idéales pour des applications quantiques telles que les dispositifs à base de fermions de Majorana, tout en ouvrant la voie à des applications innovantes en nanoélectronique haute performance au-delà du calcul quantique. Cependant, la mise en oeuvre de tels dispositifs fonctionnels reste freinée par le fort désaccord de maille entre l'InSb et les substrats III-V conventionnels, qui rend difficile une croissance de nanostructures exemptes de défauts. Cette thèse explore la croissance sélective de nanostructures d'InSb sur des substrats à maille accordée et fortement désaccordée, en utilisant l'épitaxie par jets moléculaires. Afin de permettre la modulation de densité de porteurs nécessaire aux dispositifs quantiques, l'InSb a également été intégré dans des hétérostructures comportant des barrières de potentiel semi-conductrices.

L'étude a porté dans un premier temps sur la croissance de l'InSb sur des substrats de tellure de cadmium (CdTe) accordés en maille, mais des limitations technologiques ont limité la qualité et la production de nanostructures d'InSb. La suite de l'étude s'est alors orientée vers l'utilisation de substrats d'arseniure de gallium (GaAs) orientés selon la direction $(111)_B$, où l'optimisation des paramètres de croissance a permis d'obtenir des couches minces et des nanostructures planaires de haute qualité cristalline avec une faible densité de défauts, confirmées par des analyses en microscopie électronique en transmission ainsi qu'en microscopie à effet tunnel.
À la suite de l'optimisation de la croissance d'InSb sur GaAs $(111)_B$, des couches minces et des nanofils d'InSb de haute qualité ont été réalisés sur des couches tampons de phosphure de gallium-indium à faible rugosité, elle-même épitaxiée sur substrat GaAs dans des conditions optimisées. Une étude structurale et morphologique a permis de discuter les différences mineures observées par rapport à la croissance des nanostructures d'InSb directement sur GaAs. La dernière partie de la thèse a été consacrée à l'étude des propriétés de transport électrique de l'hétérostructure InSb/GaInP/GaAs dopé n, en combinant des mesures de Hall, la méthode des longueurs de transfert et la microscopie à effet tunnel à quatre pointes. Une modulation efficace de la densité de porteurs à l'intérieur des nanostructures d'InSb, ainsi qu'une mobilité électronique record pour des couches minces d'InSb épitaxiées directement sur substrats III-V désaccordés, ont été démontrées. Enfin, une étude par spectroscopie à effet tunnel a révélé que le contrôle précis de l'état de surface est essentiel pour exploiter pleinement le potentiel de ces nanostructures.

Dans l'ensemble, ce travail établit une base fondamentale vers la production de nanostructures d'InSb de haute qualité, utile à la fois pour le développement de dispositifs quantiques et la nanoéléctronique III-V haute performance.

Mots clés : InSb, Hétérostructures III-V, Nanofils, Transport quantique, Croissance Sélective, Epitaxie par Jets Moléculaires, Microscopie à effet tunnel à pointes multiples, Transport électronique

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Introduction

Over the past five decades, exponential improvements in silicon **Complementary Metal Oxide Semiconductor (CMOS)** technology have underpinned modern information processing, following Moore's law.[1] This scaling trajectory has slowed down in recent years, as miniaturization faces power density, variability and interconnects bottlenecks. Device innovations such as **Gate All Around Field-Effect-Transistor (GAAFET)** at the 3 nm node partially mitigated these issues,[2,3,4,5] but fundamental scaling challenges persist, underscoring the need for alternatives to conventional transistor-based computing.

One disruptive paradigm is quantum computing, which exploits uniquely quantum mechanics phenomena such as superposition and entanglement, embodied in basic units called "qubits".[6,7] Unlike classical bits, qubits can encode processed information in fundamentally new ways, opening the possibility to tackle problems in cryptography, chemistry and optimization that are intractable for classical machines.[8,9] Among the various material platforms explored, one-dimensional semiconductor **NWs** have emerged as highly promising building blocks not only for quantum devices but also for advanced electronics thanks to their natural two-dimensional carrier confinement.[10,11,12]

Based on their outstanding transport properties, especially their high electron mobility, some of the III-V semiconductors were rapidly considered as potential candidates for the fabrication of quantum devices. Namely, InAs and InSb both exhibit very low effective electron mass and strong spin-orbit coupling, but InSb stands out due to its higher electron mobility and stronger coupling, making it particularly suitable for Majorana-based devices.[13,14,15,16]

The emergence of reliable **nanowire (NW)**-based quantum devices has not yet been possible so far, because their fabrication presents either a scalability or a structural quality issue. The **NWs** have been mainly vertically grown using the **Vapor-Liquid-Solid (VLS)** method that yields high crystalline quality **NWs** but suffers from poor scalability, as each wire must be transferred individually on a host substrate.[17] In contrast, **Selective Area Growth (SAG)** offers wafer-scale integration by defining **NWs** within geometrical apertures patterned on a dielectric mask,[18,19] though its larger contact area with the substrate makes it prone to crystal defects, especially in InSb. The second major hurdle in quantum device fabrication is the accurate control of the charge density inside the **NWs**, which is essential for maintaining and manipulating their quantum states. To achieve this, **NWs** must be integrated into gated heterostructures that allow electrostatic tuning.

While early efforts relied on **Metal-Organic Chemical Vapor Deposition (MOCVD)** for the **SAG** of in-plane **NWs**, this approach suffered from limitations in structural quality. At **Institute of Electronic, Microelectronic and Nanotechnologies (IEMN)**, the EPIPHY group has instead developed extensive expertise over the years through the fabrication of III-V **NWs**

using **Molecular Beam Epitaxy (MBE)**, which offers superior crystalline control. In particular, the introduction of an **Atomic Hydrogen (H_{AT})** flux was shown to be critical for obtaining GaSb in-plane **NWs** with high selectivity.[20] Building on this, functional devices such as InGaAs **NW**-based **Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET)** and tunnel diodes were later demonstrated using the same process.[21] More recently, in the doctoral work of Wijden Khelifi, InAs and InSb nanostructures were investigated leading to the successful growth of core-shell InAs/GaSb in-plane nanostructures on InP (111), with significantly enhanced transport properties compared to their unprotected InAs **NWs**.[22]

Altogether, this expertise represents a solid foundation that will serve the interests of this project. In that regard, this thesis work aims at the elaboration of high quality in-plane InSb **NWs** using H_{AT}-assisted **Selective Area Molecular Beam Epitaxy (SAMBE)**. It also intends to characterize their electronic transport. To maximize the InSb structural quality, growth investigations on the CdTe lattice-matched substrate will be done, but as described later in this thesis, will face issues with the etching of CdTe. In answer to the fabrication of gated heterostructures, InSb growth experiments will be performed on highly-mismatched n-doped GaAs substrates as we ambition to introduce either an AlGaAs or a GaInP layer in between, to act as a potential barrier and allow the modulation of the charge density inside InSb through applying a bias on the substrate.

This thesis is hence divided in 6 chapters. After introducing the fabrication of quantum devices and their associated challenges, the chapter 1 will reveal how low effective electron mass III-V semiconductors such as InSb are ideal candidates for the realization of advanced electronic devices. Then, the various epitaxial growth integration pathways will be detailed while outlining the advantages of **SAG** using **MBE** over other techniques for the production of nanostructures. The final section will review the different InSb devices originating from a growth on both lattice-matched and highly mismatched substrates before reporting their transport properties.

Chapter 2 will present first the **MBE** system used for the III-V semiconductors growth as well as the patterning processes in the context of H_{AT}-assisted **SAG** to fabricate the nanostructures. The main morphological, structural and electrical characterization techniques considered in this thesis are then detailed.

The third chapter deals with the epitaxial growth of InSb on CdTe (001) and (111) substrates. The optimized growth conditions to get a smooth InSb layer are determined through variations of the key experimental parameters, *i.e.* the growth temperature, the Sb/In ratio and the H_{AT} exposure. Hall measurements, **X-Ray Diffraction (XRD)** and **Atomic Force Microscopy (AFM)** will be used to determine the preferred CdTe substrate orientation to achieve low roughness InSb layers. The chapter will also adress challenges specific to **SAG** on CdTe substrates, such as surface etching, and propose the use of protective capping layers to mitigate this issue.

Chapter 4 extends the growth study to highly mismatched GaAs $(111)_B$ substrates. Building on previous work on InSb/InP nanostructures,[22] we will examine the growth of InSb thin films and **NWs** under similar conditions and evaluate their structural quality through **Scanning Transmission Electron Microscopy (STEM)** cross-sectional analysis as well as **Scanning Tunneling Microscopy (STM)** characterization.

The chapter 5 will investigate the integration of InSb nanostructures into heterostructures with a semiconducting barrier. While the first section will demonstrate that a low roughness GaInP thin film can be grown on GaAs $(111)_B$ substrate, the second one will reveal that using specific deoxidation sequence and adjusted growth conditions, smooth InSb layers and nanostructures on top can be produced. Then, the structural quality of the InSb **NWs** on GaInP/GaAs will be evaluated through a **STEM** study to compare with the growth directly performed on GaAs $(111)_B$.

The last chapter will be dedicated to the transport properties of InSb nanostructures grown on GaInP/GaAs $(111)_B$:n+ substrates. Electrical measurements — including Hall effect, **Transfer Length Method (TLM)** and **Four Probe Scanning Tunneling Microscopy (4P-STM)** — will be used to evaluate carrier density control, resistivity, and electron mobility. The impact of growth conditions, crystallographic orientation, and aperture geometry on transport performance will be analyzed. The last section will use **Scanning Tunnelling Spectroscopy (STS)** to study the surface-states of the InSb $(111)_B$ surface, which covers the top facets of the InSb **NWs**.

Chapter 1

State of the art and PhD work objectives

1.1 Introduction

This chapter starts by introducing quantum devices through the Majorana example, based on one-dimensional nanostructures. After reviewing the challenges associated to these devices, the most appealing candidate for the realization of such applications, InSb, will be detailed. The various integration pathways to grow nanostructures will be presented in a second time for both two and one-dimensional nanostructures. In the final section, a literature study is conducted to report the actual state-of-the-art transport properties of InSb-based devices, which will help us refining our objectives for this thesis work.

1.2 Nanostructures for quantum devices

Along with the endless quest for smaller, faster and more reliable electronic devices, the nanotechnology era emerged. The concept of this field is to optimize and tailor devices properties through their miniaturization at the nanoscale. Over the years, significant progess in existing designs like **Field-Effect-Transistor (FET)**, solar cells, sensors or lasers were achieved to boost their performances. To do so, nanotechnology takes advantage of a phenomenon described at the early-age of semi-conductors called the quantum confinement effect. A nanostructure will experience confinement when one of its dimensions becomes comparable to the De Broglie wavelength described by

$$\lambda_{DB} = \frac{\hbar}{\sqrt{2m_e * k_B T}} \tag{1.1}$$

where m_e* is the effective electron mass, $\hbar$ the reduced Planck constant, k_B the Boltzmann constant and T the temperature.[23]

Therefore, all of the nanostructure properties including band structures, will be modified in comparison to the bulk. Knowing that, several classes of nanostructures were established. First, **Quantum Well (QW)**, where carriers motion remains free in the plane (2D) and gets restricted in the thickness (usually labelled z-axis). Then, **NWs** have only a one dimensional (1D) propagation, along their length. Eventually, **Quantum Dots (QDs)**, for which the carriers are

constrained in all 3 dimensions (0D). The **Density of States (DOS)** per volume $D^{(i)}(E)$ (where $i = 0, 1, 2$ or 3) is then progressively modified with quantum confinment as depicted in Figure 1.1.

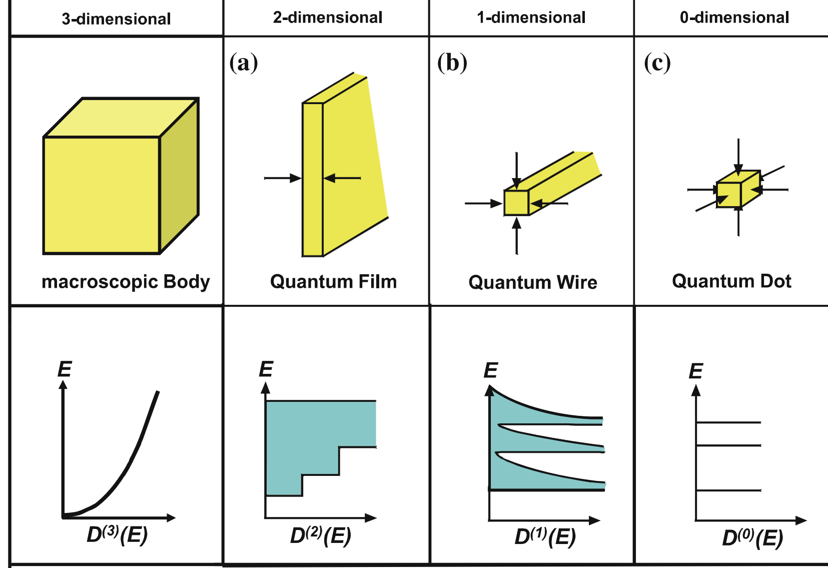


Figure 1.1: Schematic of the **DOS** depending on the nanostructure dimension. Extracted from[24].

In the bulk case (3D), the energy levels form a continuous band. Moving on to **NWs**, the energy band will turn into peaks and end up fully discrete as spike-like in **QDs** (0D). The **DOS** per volume L^i in real space will be in the form of either

$$D^{(3)}(E)dE = \frac{1}{(2\pi)^2}\frac{m}{\hbar^3}\sqrt{2mE}\mathrm{d}E \tag{1.2}$$

$$D^{(2)}(E)dE = \frac{2\pi k \mathrm{d}k}{(2\pi)^2} = \frac{m}{2\pi\hbar^2}\mathrm{d}E \tag{1.3}$$

$$D^{(1)}(E)dE = \frac{1}{2\pi}\mathrm{d}k = \frac{m}{2\pi\hbar}\frac{1}{\sqrt{2mE}}\mathrm{d}E \tag{1.4}$$

for respectively bulk, quantum wells and **NWs**.

These spacial restrictions will not only affect the **DOS**, but electronic levels occupancy, carrier density, mobility and also optical properties. Briefly, this structure design engineering enlarged the capabilites to tune device properties.

1.2.1 1D based quantum devices

With the rush towards quantum computing development for about a decade, the device complexity further stepped up. However, the quantum systems are exposed to quantum decoherence. For instance, electrons interacting with their environment via electromagnetic forces can easily lose their quantum properties.[25,26] This fragility remains a major obstacle to build reliable quantum processors. To address it, robust platforms are needed, and Majorana quasi-particles offer a promising solution thanks to their intrinsic topological protection.

1.2.1.1 Principle of Majorana fermions devices

First predicted in 1937 by Ettore Majorana, these eponymous particles shook up entire condensed matter physics at this time.[27] Indeed, Majorana fermions are particles that are their own anti-particles, visualized mathematically through

$$\psi = \psi^{\dagger} \tag{1.5}$$

where ψ is the quantum field spin operator (the mathematical tool encoding particles creation and annihilation) and $\psi^{\dagger}$ the Hermitian conjugate (complex conjugate and transpose).[28,29]

Because of this properties, Majorana fermions could be used for quantum operation due to their fault-tolerant character. In other words, they are not subject to quantum decoherence as regular fermions do due to their charged status.

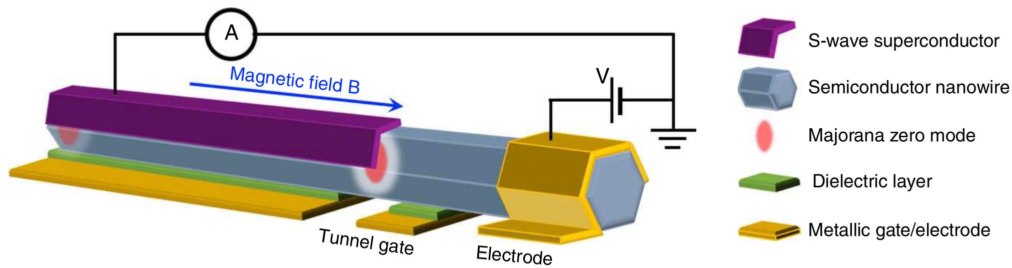


Figure 1.2: Schematic of a **NW**-based Majorana device, adapted for tunneling spectroscopy measurement. A **NW** is coupled to a s-wave superconductor from which Majorana zero mode would emerge at both ends of the **NW** if all conditions are gathered. For that, two gates are needed to perform the measurement: a gate for electro-chemical potential tuning and a tunneling gate to account for various tunnel barrier transmission values. Extracted from[11].

Putting the mathematical details aside because it is beyond the scope of this work, the prediction of Majorana fermions triggered a limitless race in looking for the device that could integrate it for real.[30,31,32]

1.2.1.2 NW-based devices

NW-based quantum devices were put into the spotlight over the last decade for being the perfect host for the famous Majorana fermions devices.[33] This design consists in a semiconductor-superconductor quantum wire as presented in Figure 1.2 that caught much attention in recent years.[34,35,36] In this setup, the Majorana fermions are predicted to emerge as quasi-particles at both ends of the hybrid **NW**, nowadays labeled **Majorana Zero Mode (MZM)**.

Three main ingredients were called out to achieve **MZM** in this design:

- A strong **Spin Orbit Coupling (SOC)** semiconductor to allow splitted spin states and spin-momentum locking.
- A high-quality (s-wave) superconductor-semiconductor interface to ensure particle-hole symmetry via proximity effect.
- A magnetic field $\vec{B}$ parallel to the **NW** to break time-reversal symmetry and create a topological phase.

The **MZM**s exist at the end of the region where superconductor-semiconductor are overlapping because the structure is in a topological phase (*i.e.* protected against impurities and defects).

Superconductivity has a central role in understanding how **MZM** can emerge in this setup. Discovered experimentally in 1911 by Onnes, this property was solely explained through the **BCS** theory in 1957 by J.Bardeen, L.Cooper and J.Schrieffer. It occurs when the resistivity of a material drops to zero below a critical temperature T_c, allowing a current to flow within the material without energy dissipation. At the microscopic scale, the **BCS** theory explains this phenomenon by the formation of Cooper pairs that consists in the coupling of two opposite spin and momentum electrons to form a bound state.[37] Together, they exhibit an integer total spin value (0 or 1) allowing them to occupy the same quantum state.

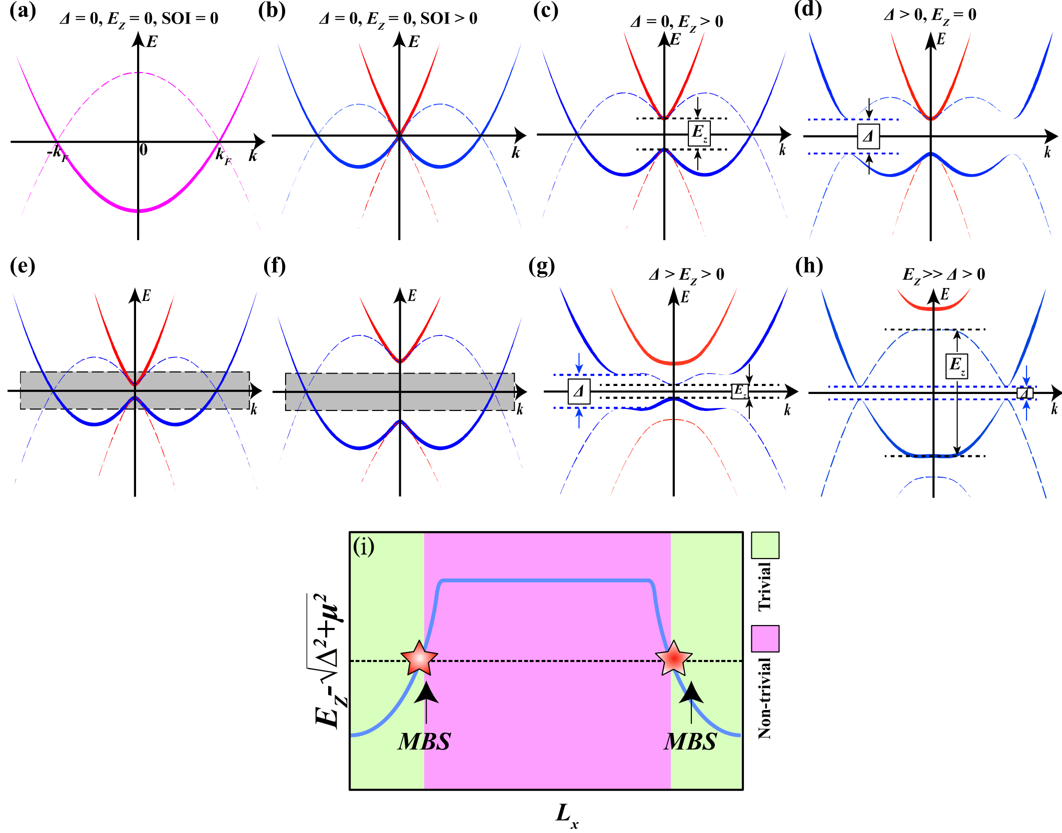


Figure 1.3: Energy dispersion relation plots in the case of a **NW**-based quantum device. Electron bands are materialized by solid lines. Hole-like bands correspond to dash lines. (a) Case of a regular semiconductor **NW** with no **SOC**. (b) For a high **SOC**, spin bands splitting occurs. (c) In the presence of an additional magnetic field $\vec{B}$ a Zeeman gap is opened E_z. (d) Schematic of the superconducting energy gap in a superconductor **NW** with no $\vec{B}$ field. (e-f) Two "helical" phases for different E_z values. This corresponds to a semiconducting **NW** with strong spin orbit interaction coupled to a s-wave superconductor. In (f) the grey region corresponds to a spinless environment. (g) Trivial superconducting phase, when the $\vec{B}$ field does not exceed critical value, meaning $\Delta > E_z$. (h) Topological superconducting phase where $\Delta < E_z$. (i) Schematic graph of Majorana bound states created at both ends of the **NW**. Adapted from[38].

Looking now at Figure 1.3, the **MZM** emergence within a **NW**-based design can be explained step-by-step using the three aforementioned ingredients. The energy dispersion diagram of a regular semiconducting **NW** with no **Spin Orbit Interaction (SOI)** is shown in Figure 1.3a as a reminder. First, for a high **SOC** 1D semiconducting **NW**, splitting of the two electronic spin

bands occurs as depicted in Figure 1.3b. Now, with an applied external magnetic field, a Zeeman splitting induced gap E_z is opened up for $k = 0$ and forms a spinless region at the Fermi level E_F called the helical phase. When adding a superconductor on top, a superconducting gap Δ is now induced through the **NW** due to the proximity effect (Figure 1.3d). Indeed, the Cooper pairs formed leak into the semiconductor allowing its electrons to pair as well. The final step is obtained for the condition

$$|\tilde{B}| > \sqrt{\Delta^2 + \mu^2} \tag{1.6}$$

where μ is the chemical potential, $\tilde{B} = g\mu_B B$ the Zeeman field with g the landé g-factor, $\mu_B = e\hbar/2m_e$ the Bohr magneton.[28]

If the condition of Equation 1.6 is not satisfied, *i.e.* the Zeeman gap E_z is lower than Δ the superconducting gap, the **NW** will remain in the trivial superconducting state as per Figures 1.3e and g. This is justified through opposite spin electrons still being able to form Cooper pairs. Otherwise, for stronger magnetic field $\vec{B}$ beyond the critical value, the Zeeman gap E_z is large enough to push one spin band to higher energy. The gap vanishes and reopens to form the topological superconducting phase (Figures 1.3f and h). Because only one spin species is now found near the Fermi level, there is no more opposite spin species to pair with, leaving behind a p-wave pairing. Thanks to the gap closure and reopening, **Time Reversal Symmetry (TRS)** is broken and a **MZM** emerges through a Majorana bound states pair at each ends of the superconducting **NW** (Figure 1.3i). The **MZM**s being then topologically protected through particle-hole symmetry.

Several techniques are now developed to evidence these **MZM**s among which the trendy **Zero Bias Anomaly (ZBA)** keyword became ubiquitous in the literature. It is simply resulting from **Zero-Bias Conductance Peak (ZBCP)** measurement (Figure 1.4). In that case, the transmission spectrum of the **NW** (differential conductance $dG = dI/dV$) is evaluated as a function of the gate voltage ($\mathbf{V}_G$).[36] For such experiments, a careful control of the **NW** quantum device is needed. This control is generally achieved through the use of multiple gates at very low temperature (few mK) making the whole system very sensitive to any external fluctuations.

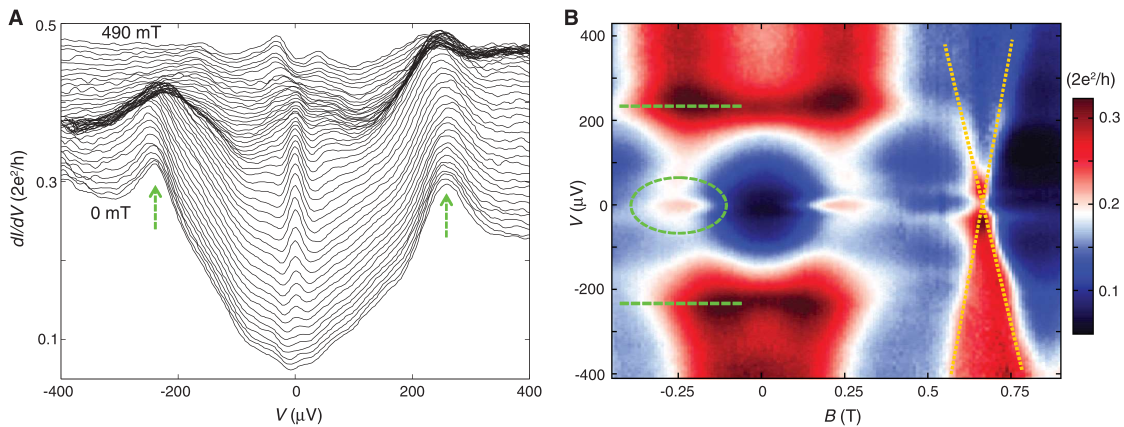


Figure 1.4: Example of **ZBCP** measurement through magnetic field dependent tunneling spectroscopy. A) Various dI/dV curves for different B fields. B) The exctracted color plot of dI/dV depending on the applied voltage V and magnetic field $\vec{B}$. The green-dashed oval represents the Zero Bias Peak and dotted lines indicate the gap edges as per arrows in A). Extracted from[16].

In the literature, several **NW**-based device designs were tested, using for most high **SOC** semiconductors such as InAs or InSb, and Al or Nb-based materials for superconductors.[15,39,40,41]

In spite of all efforts so far, the collected results still remain far from the ideal quantized value peak of $G(0) = 2e^2/h$ for perfectly transparent Majorana modes. As imaged in Figure 1.4a only a small fraction of $G(0)$ is captured, thus prohibiting the confirmation of their existence. Nevertheless, this valuable knowledge is still reinforcing the common interest in the quest of quantum computing.

1.2.1.3 Devices based on 2DEG with top gates defining 1D channel

A considerable amount of studies explored also the potential of Majorana devices based on **Two-Dimensional Electron Gas (2DEG)** instead of **NWs**. Through accurate design of the structure, a quasi 1D channel can be defined. Among the suggested architectures, two options were investigated theoretically and experimentally to confirm their convenience for such quantum applications.

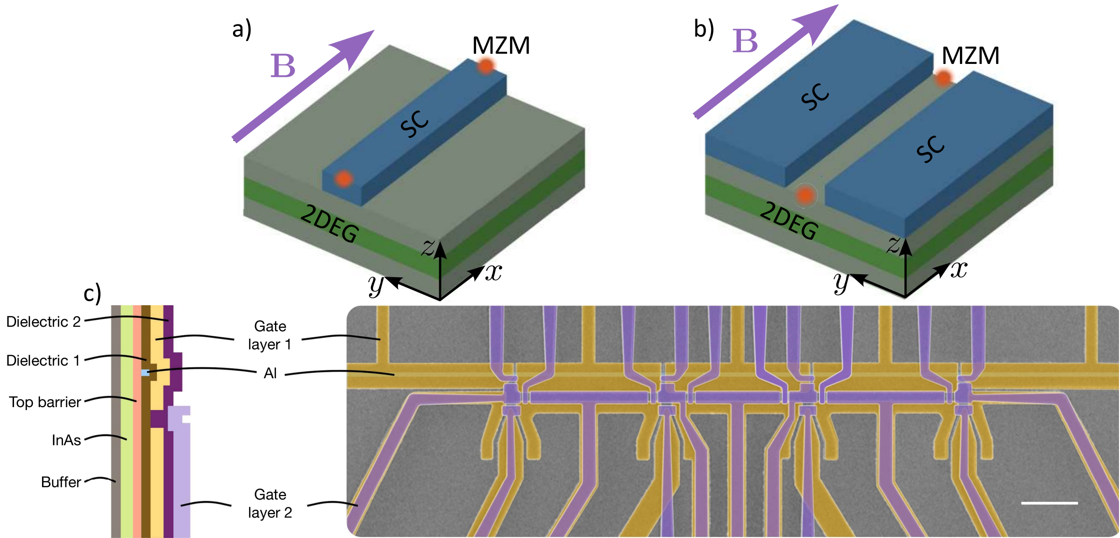


Figure 1.5: Schematics of the different Majorana devices based on **2DEG**, a) the "S-stripe" design, where only a semiconductor narrow stripe covers the surface. b) The "N-stripe" geometry which is inverted. In both cases **MZM** are predicted to appear at both ends of the stripe forming a quasi 1D channel. The light green represents top and bottom barrier layers respectively, to confine the **2DEG** in a **QW**. Extracted from[42]. c) The cross-section and top view schematic of the Majorana 1 device from Microsoft. Extracted from[43]. The design is more complex with **QDs** and dual dielectric and gate layers. Scale bar on the image is 1 µm.

As depicted in Figure 1.5a, the first setup called "S-stripe" consists in depositing a narrow 1D superconducting cover strip on top of a **2DEG**. A negatively biased gate is in charge of depleting the exposed **2DEG** to induce a similar situation than for the **NW**-based device with **MZM** emerging at the stripe ends.[42] The second design called "N-stripe" has a similar but inverted structure. The superconductor covers the **2DEG** surface except along a narrow 1D stripe as pictured in Figure 1.5b. In such structures, the **MZM**s are emerging from the Andreev bound states formed thanks to Andreev reflections at both superconductor-semiconductor interfaces that constructively interfere.[44,45,46]

Microsoft claimed very recently achieving Majorana fermions devices with another kind of architecture through the recent press release of Majorana 1 device.[43] As presented in Figure 1.5c, the superconducting topological **NW** is formed in a similar way to "S-stripe" structures using an

InAs **2DEG** and an Al superconductor. However, to fabricate such device, the design was further complicated with multiple **QDs** and gates to accurately control and tune the potential along the nanostructure.[47,48] Nevertheless, due to the extreme actual complexity of fabricating the device and sensing **MZM** properly, there remains considerable efforts before implementing it in the daily-life nanostructured components.

1.2.2 Ballistic transport in quantum devices

One implicit condition for the **MZM**s to emerge within such quantum device is that the semi-conducting **NW** must be in the ballistic transport regime. As established for a long time, any disorder in the material triggers scattering from impurities, phonons or electrons. Consequently, this effect can be responsible for topological phase destruction as well as increased decoherence.

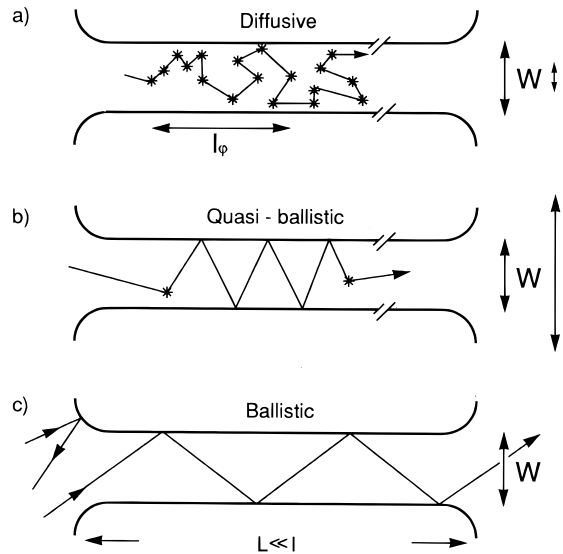


Figure 1.6: Schematics of the three transport regimes with electron trajectories: a) Diffusive ($l < W, L$), b) quasi-ballistic ($W < l < L$) and c) Ballistic ($W, L < l$). Scattering from impurities is represented by *. Extracted from[49].

Ballistic transport occurs when electrons are flowing through the device without scattering (= collision). Figure 1.6 shows the three main regimes existing in conducting materials that will depend on the mean free path of electrons ($l = v_f \tau$) with regards to the conductor dimensions (W and L for the width and length).[49] This parameter describes the average distance between two collisions with v_f the electron velocity and τ the scattering time:

- $l < W, L$ represents the diffusive transport (Figure 1.6a), most commonly seen in bulk materials at **Room Temperature (RT)**. With scattering, electron energy and momentum can change (elastic or inelastic).
- $W < l < L$ determines the quasi-ballistic transport (Figure 1.6b) where the carriers have an existing but low probability of collision.
- $W, L < l$ stands for ballistic regime where conductance does not depend anymore on the length of the conductor (Figure 1.6c).

The characteristic of the ballistic transport can be explained through the use of Landauer's formalism in a two terminal biased quantum wire. The current is expressed by

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} \mathrm{T}(E)M(E)(f_1(E) - f_2(E)) \tag{1.7}$$

where $\mathrm{T}(E)$ is the transmission energy, $M(E)$ the number of conductive channels at energy E and $f_i(E)$ the Fermi function of each contact.[50,51]

Only electrons in between the source and drain quasi Fermi energy (depicted by F^+ and F^- in Figure 1.7a can carry the current. As such, the number of contributing electrons will be in the corresponding k-states included between k_D and k_S.[52] For a one-dimensional system each k-state is separated by $\frac{2\pi}{L}$ with two electrons per k-state. Equation 1.7 can be reorganized into

$$I = \frac{2q}{h}\int_{k_D}^{k_S} \mathrm{T}(E)M(E)\mathrm{d}k\frac{\mathrm{d}E}{\mathrm{d}k} \tag{1.8}$$

In the case of a ballistic regime (no collision), the transmission energy $\mathrm{T} = 1$. Then, by switching to energy variable and integrating, it yields for a single channel ($M = 1$)

$$I = \frac{2q}{h}(\mu_S - \mu_D) \leftrightarrow I = \frac{2q^2}{h}V_{DS} \tag{1.9}$$

where $V_{DS} = -(\mu_D - \mu_S)/q$.

As $G = I/V$, the quantization of ballistic conductance (and resistance) is well highlighted. For a number M of conductive channels

$$G = \frac{2e^2}{h}M(E_F) \leftrightarrow G = \frac{M(E_F)}{12.9\ \mathrm{k\Omega}} \tag{1.10}$$

leading to the well-known conductance plateaus (Figure 1.7b) with every step corresponding to a new conducting channel that contributes to current flow through the device.[50]

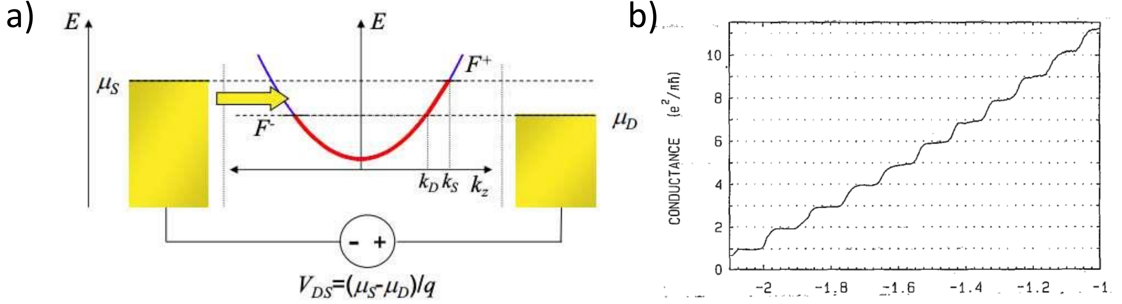


Figure 1.7: . a) Schematic of a two terminal contacted quantum wire under applied bias with an energy versus k-space diagram. Extracted from[52]. b) Conductance plateau shown from Quantum Point Contact measurement of an AlGaAs/GaAs **2DEG**. Extracted from[53].

Measurements at very low temperature (<4 K through Helium cooling) such as **quantum point contact (QPC)**, **4P-STM** or other probing techniques on nanodevices are used to evidence such transport regime.

Eventually, to resonate with the previously explained Majorana devices, the ballistic regime must predominate in such nanostructures to ensure transport properties are robust and exhibit

minimal scattering. Therefore, devices with a high electron mobility and large mean free path values will be generally associated with such ballistic transport. Table 1.1 summarizes the highest state-of-the-art reported values depending on the structure type and material system in order to quantify this ballistic transport aspect.

Type	Material	μ (cm^2.V^{-1}.s^{-1})	n (cm^{-2}/(cm^{-3})	l (µm)*	T (K)	Ref
2DEG	GaAs/AlGaAs	57×10^6	1.55×10^{11}	370*	0.3	56
	GaAs/AlGaAs	44×10^6	2×10^{11}	325*	0.3	57
	GaAs/AlGaAs	35×10^6	3×10^{11}	316*	0.36	58
	InAs/AlGaSb	0.65×10^6	3.81×10^{11}	6.63*	0.5	59
	InSb/InAlSb	0.35×10^6	4.9×10^{11}	4.031*	1.3	54
	InSb/InAlSb	0.2×10^6	2×10^{11}	1.47*	1.8	60
	InAs/InGaAs	0.12×10^6	9×10^{11}	1.88*	0.01	61
NWs	InSb	0.035×10^6	1×10^{17}	0.26	4.2	62
	InSb	0.025×10^6	–	0.1	4	63
	InAsSb	0.016×10^6	–	–	10	64

Table 1.1: State of the art mobilities and mean free path length. Mean free-path with * are calculated using following expression:[54,55] $l_e = \sqrt{2\pi\hbar^2 n_e \mu^2/e^2}$

While the **2DEG** AlGaAs/GaAs devices exhibit an electron mobility higher than several tens of millions of cm^2.V^{-1}.s^{-1} thanks to ultra pure materials (AlGaAs and GaAs) growth with minimal defects, InAs or InSb-based **2DEG** immediately ranges down to electron mobilities of several hundreds of cm^2.V^{-1}.s^{-1}. Oppositely, the lower electron mobility evidenced in InAs or InSb-based **2DEG** results from an increased defect density coupled to surface states scattering the carriers. In these **2DEG**-based devices, the mean free path can range from sub-micrometric values to tens of microns.

Switching now to **NWs** devices, the electron mobility drops further with best values around 35 000 cm^2.V^{-1}.s^{-1} at **Low Temperature (LT)** (4.2 K) in the case of InSb **NWs FET**s. Because electrons are confined in one dimension, the scattering sensitivity increases which reduces their mean free path significantly.

To conclude, this Table 1.1 will serve in the following of the work as a point of reference with regards to the expected mobility values in thoroughly optimized cases. Keeping in mind that any defects will be detrimental for the transport properties, the highest mobilities and mean free path values will solely be achieved through finding optimized growth pathways.

1.3 InSb for quantum devices

1.3.1 InSb properties

As mentioned in the previous section, indium antimonide (InSb) is proven to be the ideal candidate for quantum devices applications together with indium arsenide (InAs). Already used for mid infrared detectors,[65] InSb is deemed to be the most valuable of the III-V semiconductors family owing to its exceptional electronic bulk properties.

Looking at the values registered in Table 1.2, both III-V semiconductors exhibit bulk properties far more appealing than silicon (Si) with regards to **MZM** investigation. Their very low electron effective mass (m_e^*) coupled to large electron mobility (μ_e) and Landé g-factor (g) ensures

	a (Å)	E_g(300 K) (eV)	$m_e^*(m_o)$	μ_e (300 K) ($cm^2.V^{-1}.s^{-1}$)	g
InSb	6.479	0.17	0.014	77000	51
InAs	6.058	0.35	0.022	33000	12.5
Si	5.431	1.12	0.98	1400	2

Table 1.2: Comparison of the lattice constant and basic electronic parameters between InSb and InAs with Si[66,67,68,69].

a high **SOI** necessary to meet the stringent quantum conditions. Though InSb excels even more than InAs bulk properties, the lack of a lattice matched semi-insulating substrate still exposes it to potential growth defects, through a metamorphic growth, altering the transport properties.

While III-nitrides (AlN, GaN,...) crystallize in a **Wurzite (WZ)** structure, most of the III-V (InSb, InAs, GaAs, InP, GaP, ...) exhibit a **Zinc-Blende (ZB)** structure which consists in two interpenetrating **Face-Centered Cubic (FCC)** lattices as illustrated in Figure 1.8.

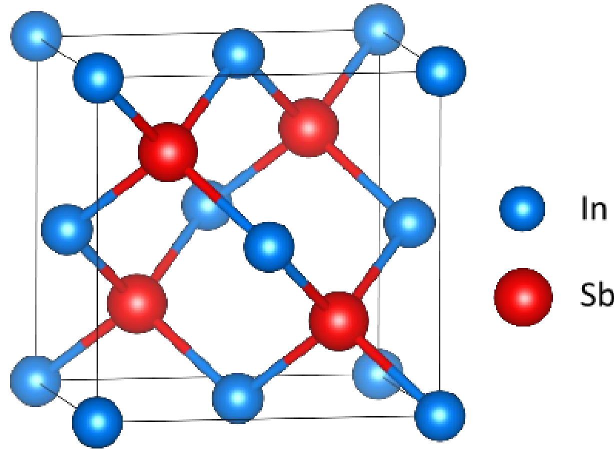


Figure 1.8: Structure of the InSb unit cell.

The cations from group III-element, here In, form the first **FCC** lattice. The group V-elements, like Sb, are shifted by (1/4, 1/4, 1/4) in the cell, occupying the interstitial tetrahedral positions and forming the second sub-lattice. Therefore, each atom is tetrahedrally coordinated to four nearest neighbors ensuring strong covalent bonds. For wafer cutting, three main crystallographic orientations are commonly used. The (100) plane forms square-like lattices making it the preferred wafer-cut. (110) plane gives diamond-like atom organization and (111) is defined by hexagonal atoms arrangement.[70] For **ZB** crystals, the principal cleavage plane is parallel to (110) due to the absence of electrostatic forces between the planes because of an equal number of III and V atoms.[71]

1.3.2 InSb heteroepitaxial growth

Because of its low energy band gap of 0.17 eV as shown in Table 1.2, its growth on InSb substrates is not considered as the high conductivity of the substrate prevents proper device insulation. Cheaper purchased substrates with semi-insulating possibilities such as GaAs or InP will be consequently preferred for the epitaxial growth of InSb.

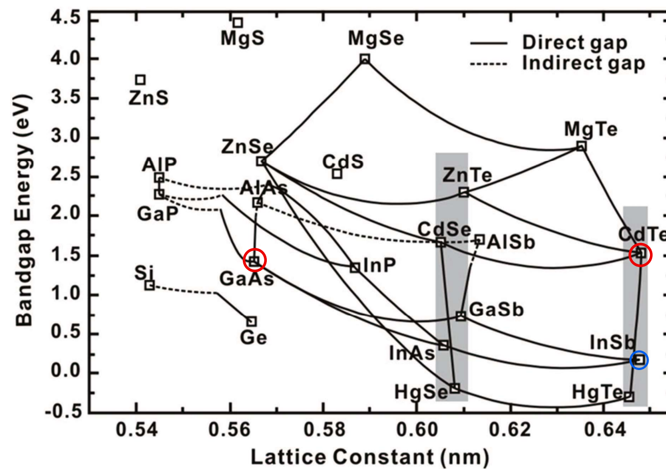


Figure 1.9: Bandgap energy of semiconductors versus lattice constant. Adapted from[72].

As shown on Figure 1.9, the major downside of InSb stands on its difficult integration on other III-V substrates. InSb has the largest lattice constant (6.48 Å) of this family of materials. It causes immediately an important lattice mismatch with any other types of III-V substrates. The lattice mismatch or misfit is expressed by

$$f = \frac{a_S - a_L}{a_S} \tag{1.11}$$

where a_S is the substrate lattice constant and a_L the one from the layer grown on top.[73] Depending on the value of f (in %), different scenarios may happen for thin film growth on a mismatched substrate.

For $0 < f < 2$ % the growth remains coherent but some strain can be created. With higher values of $f \approx 3 - 4$ % the strain accumulates until a critical thickness h_c for which misfit dislocations (plastic deformation) will be created to relax the strain in the growing layer (Figure 1.10a).[74,75] The value of h_c for these misfit rates already drops down to few nanometers. Beyond $f > 4$ %, the interface is not coherent anymore, with almost immediate (one to few monolayers) plastic relaxation through an array of misfit dislocations at the interface to evacuate maximal stresses.[76]

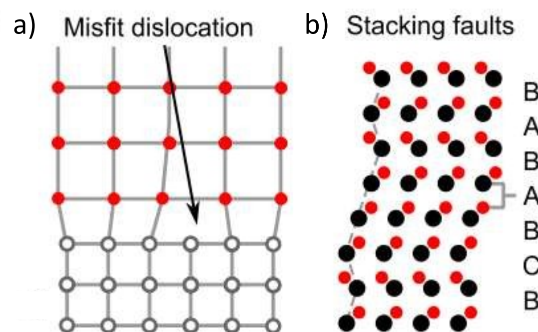


Figure 1.10: Representation of different types of defects, here in the case of III-V growth on a mismatched substrate. a) Misfit dislocation arising from high misfit to relax strain plastically. b) Stacking faults within the III-V layer. Adapted from[77].

Not only dislocations (1D line defects) but other types of defects may emerge from misfit accomodation such as **Stacking Fault (SF)**, as shown in Figure 1.10b. A **SF** is a 2D planar defect that results from a change in the stacking sequence of atomic planes.

Using Equation 1.11, the misfits between InSb and standard III-V substrates can be estimated. Very large rates are found with InSb on InP situated at 10.4 % and InSb on GaAs even further with 14.6 %. Nevertheless, a potential alternative to get smoother InSb films is to use a CdTe substrate (part of the II-VI family) for epitaxial growth. Its lattice constant of 6.4825 Å (Figure 1.9) offers almost a perfect lattice matching (f = 0.054 %) with InSb.[78] CdTe has a comparable band gap (E_g=1.5 eV) than the III-V substrates candidates GaAs and InP. By using undoped CdTe substrates it could offer the possibility to grow high quality InSb on an insulating substrate. However, the heterovalent junction formed InSb/CdTe is accompanied with a charge imbalance that may create interfacial states trapping carriers or dopants. They also exhibit a different thermal stability which may complicate growth parameter optimization and abrupt interface formation.[79]

1.4 Integration pathways

1.4.1 Growth regimes

To fabricate sophisticated quantum devices and take advantage of the outstanding InSb bulk transport properties, it is necessary to achieve the highest growth quality possible. This is where epitaxy comes into play, allowing to grow crystalline thin layers. In this process, the single crystal substrate orientation is transferred to the growing layers.[80] For epitaxial growth of a layer from the same material than the wafer, this is called homoepitaxy. When the two differs, the term heteroepitaxy is employed (InSb on GaAs for instance).

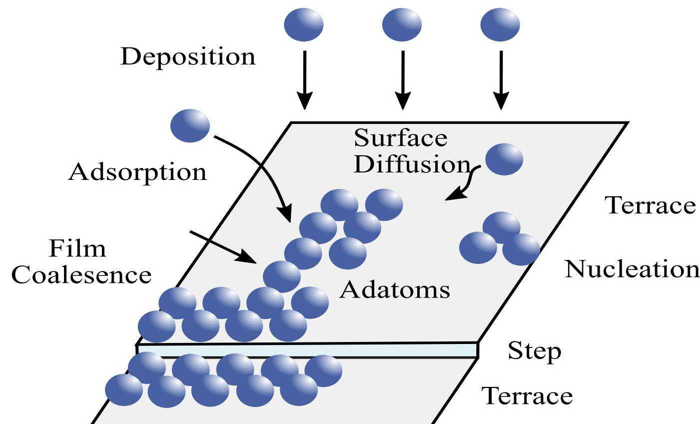


Figure 1.11: Scheme of the different mechanisms in epitaxy namely adsorption, diffusion, incorporation and nucleation. Extracted from[81].

During epitaxy, different mechanisms interplay as depicted in Figure 1.11. Usually, an atom is firstly adsorbed on the surface before incorporation. Driven by the free energy minimization of the system, the atom will diffuse on the surface until the most appropriate incorporation site (energetically speaking) is found. Then, the adatoms form nucleation sites, that will help in film coalescence. In the context of III-V semiconductors, group III-elements are adsorbed first due to their lower volatility before group V-elements arrives for bonding.

Three main growth regimes are taking place in epitaxy, all can be roughly related to surface energy consideration as imaged in Figure 1.12.

- The **Frank-van der Merwe (FM)** regime referring to the ideal case where 2D layer by layer growth is occurring because of $\gamma_s > \gamma_f + \gamma_{fs}$, known as perfect substrate wetting.
- The **Volmer-Weber (VW)** regime where the growing layer is formed by islands, due to a stronger attraction between atoms than the once towards substrate via $\gamma_s < \gamma_f + \gamma_{fs}$
- The intermediate regime **Stranski-Krastanov (SK)** known as layer-plus-island where the first monolayers follow a layer-by-layer growth until a critical thickness after which islands are formed. This regime is often explained through strain accumulation in heteroepitaxy.

$\gamma_s, \gamma_f, \gamma_{fs}$ are respectively standing for substrate, growing film and film-substrate interface surface energies.[82,83]

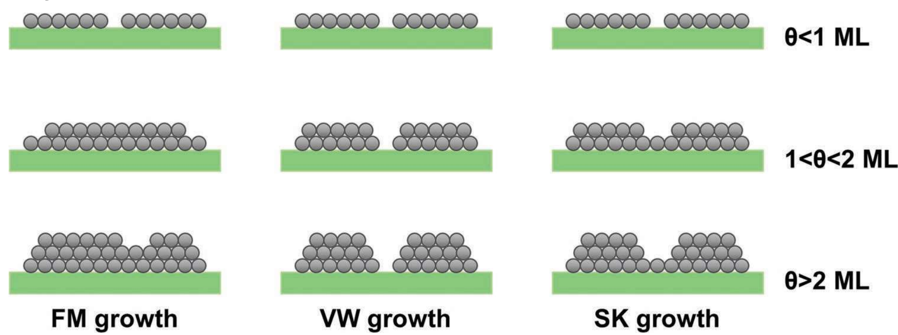


Figure 1.12: From left to right: the three different growth regimes Frank-van der Merwe (**FM**) layer-by-layer, Volmer-Weber (**VW**) island growth and Stranski-Krastanov (**SK**) layer-plus-island. θ refers to the monolayer coverage of the substrate. Extracted from[84].

1.4.2 Growth techniques and crystal defects

Several growth techniques established since the middle of the XXth century can be used to fabricate high quality crystalline layers. Each of these methods contributed in the development of more advanced devices, although their applications can differ.

MOCVD settled as a reference growth technique for mass production of optoelectronics devices (**Light Emitting Diode (LED)**, solar cells, lasers, ...) thanks to its versatility and high growth quality of multilayered structures. Metalorganic precursors are introduced into the reactor and decomposed onto the heated substrate to form an epitaxial layer. The good uniformity, low pressure (usually 50 – 150 Torr) and growth rate in the range of several micrometers per hour offered by **MOCVD** all account for its scalability, thus preferred for large scale volume production.[85]

Less favored for large-scale production due to its lower growth accuracy, **Hybrid Vapor Phase Epitaxy (HVPE)** still found a role in the high-power application field. This technique is based on hydrides species reaction with metal elements for III-V/II-VI growth (GaAs, GaP, ZnSe, ZnTe) or chlorides species in the case of III-nitrides (GaN essentially). As **HVPE** operates at higher pressures up to 1 atmosphere and larger growth rate (1 – 5µm/min),[86,87] it performs at growing thick layers or bulk crystal substrates. Although being a powerful technique, these experimental conditions are less in line with the required low residual doping of epitaxial layers for quantum devices fabrication.

In contrast to these techniques, the last method of growth, **MBE** adopts a nuanced position. This technique allows to produce extremely high-quality thin films with atomic layer precision thanks to favorable experimental conditions. Indeed, **MBE** operates under high-vacuum environment typically in the $10^{-8} - 10^{-12}$ Torr and at very low growth rates less than a nanometer per minute (0.1 – 1 nm/min), meaning as low as 0.01 **Monolayer (ML)**/s. Also, higher growth rates up to a micrometer per hour (1 µm/h), *i.e.* 1 **ML**/s can also be set. In both cases, the growth rate can be manipulated with a remarkable accuracy through the calibration of elemental beam fluxes for each species.[88,89] The whole system offers not only critical thickness control but also layer composition through doping for instance. Thus, **MBE** gathers all the crucial conditions to guarantee high electronic properties for consistent quantum devices fabrication.

Nonetheless, independently of all the presented growth techniques a variety of crystal defects can be formed during the layer epitaxy. While the lattice mismatch will be responsible for a considerable amount of these defects such as misfit dislocation (1D) as presented in the previous section 1.3.2, the crystal orientation of the substrate will also further influence defect formation. Indeed, adatom mobility, surface reconstruction, surface energies and strain relaxation processes will be different if the epitaxial growth takes place on (001) or (111) substrates.

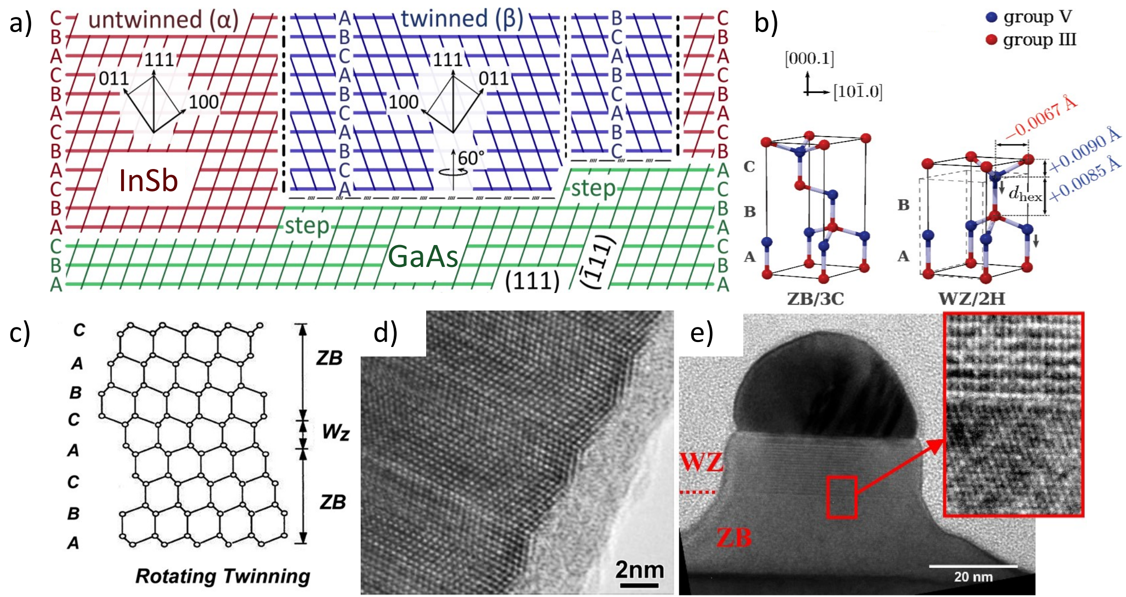


Figure 1.13: a) Schematic of a possible InSb on GaAs $(111)_B$ cross section showing twinning at the interface. Normal stacking (ABC) is shown in red (untwinned α), twinned regions in blue (β) where stacking sequence is mirrored (CBA). Extracted from[90]. b) Scheme of the InSb **ZB** and hexagonal **WZ** structure. d_{hex} represents the bond length in the hexagonal unit. Comparison with normal cubic lattice is in dashed lines. Extracted from[91]. c) Model showing twinning inside a **NW**. A small **WZ** region (CAC) results from the twin plane. d) **STEM** image of an InAs (111) **NWs** displaying the "zig-zag" twinned structure with coexistence of **ZB** and **WZ** segments. Extracted from[92]. e) **Transmission Electronic Microscopy (TEM)** image of a GaAs (111) **NWs** exhibiting an abrupt transition from **ZB** to **WZ** structure. Inset shows a zoom-in on the interfacial region. Extracted from[93].

Especially in the case of III-V growth on (111) substrates, "twinning" has been evidenced inevitably.[92] As shown in Figures 1.13a and c, a twin corresponds to a planar defect where two regions are mirrored by suddenly changing the stacking order of layer of atoms. For example

the stacking sequence ABCABCABC changes into ABCACBACB in usual **ZB** structure for III-V materials. The plane disrupting this ideal stacking sequence is called a twin plane.[94,95]

Unfortunately, due to the closely packed nature and the symmetry of the (111) surface, only a slight position shift of atoms from the regular stacking is needed to create a twin boundary making it a low-cost energetic process. As a matter of fact, Gottschalk *et al.* proved quantitatively on several III-V semiconductors that the (111) **SF** energy (*i.e.* the energy to have a (111) twin boundary) was correlated with the frequency of (111) twin formation. Authors demonstrated that such energy barrier is lower with higher ionicity of the bonds (47 meV/atom for GaAs, 43 meV/atom for InSb and 17 meV/atom for InP).[96]

In this view, especially in the case of III-V **NWs**, twinning was observed to induce a transition of the **ZB** crystal to the hexagonal **WZ** structure due to the low energetic barriers (Figure 1.13b). Such a change was evidenced in GaAs **NWs** and investigated by Glas *et al.* In their study, they highlighted a **ZB** to **WZ** structure transition characterized by a difference in lateral facets. While the **ZB** exhibits triangular bases with tilted lateral facets, the hexagonal **WZ** polytype presents vertical facets as shown in Figure 1.13e. Through modeling, they demonstrated that the growth conditions (temperature and vapor pressure controlling supersaturation) were directly responsible for stabilizing the **WZ** structure during the remaining **NW** growth.[93] Eventually, a high density of twinning plane was also observed in InAs **NWs**. As depicted in Figures 1.13c and d through a “zig-zag” shape, such finding supports the energetically favorable coexistence of **ZB** and **WZ** structures within (111) oriented III-V semiconductors.[92]

Thanks to the preserved lattice continuity across the twin plane (just mirrored), twinning is less detrimental than dislocations regarding the semiconductor transport properties. Nevertheless, because it still remains a (2D) planar crystal defect, extensive efforts will be made through controlled growth to try reducing twinning density especially when using (111) oriented substrates.

1.4.3 Two Dimensional InSb integration

Due to its large lattice constant, the integration of InSb on III-V substrates remains delicate as a highly mismatched growth will be too detrimental for transport properties. Therefore, many efforts were done so far trying to cope with this disadvantage and produce high quality InSb layers for advanced optoelectronic applications. In the mean time, the InSb growth on lattice matched CdTe substrate also received some attention to assess potential outcome from this unique III-V/II-VI combination.

1.4.3.1 Growth on InP mismatched substrate

Among the extensive studies conducted on the heteroepitaxial growth of InSb on InP substrates,[97] previous works from the EPIPHY team highlighted the impact of the substrate crystallographic orientation on the InSb growth regime in this highly mismatched system.[22,98] To do so, the growth of 10 nm-thick InSb thin film was done on (100) and (111) oriented InP substrates. Under similar growth conditions that consisted in: **Growth rate (V_G)** = 0.05 **ML**/s, high Sb/In ratio (120), **Growth temperature (T_G)** ∼390 – 405 °C, the two samples exhibited a drastic difference in the InSb film morphology.

The InSb growth on InP (100) in Figure 1.14a displayed elongated islands along the [110] direction with a thickness 10 times higher than the nominal value. As the InSb islands formed {111} side facets in these growth conditions, it suggested their surface energy is minimized. Looking at Figure 1.14b, the InSb growth on InP $(111)_B$ substrates confirmed the surface energy minimization along this (111) orientation, as a quasi-2D growth mode was achieved where InSb

covered about 90% of the surface. Under **XRD**, the InSb film appeared to be 95% relaxed only after 10 nm as depicted in Figure 1.14c.

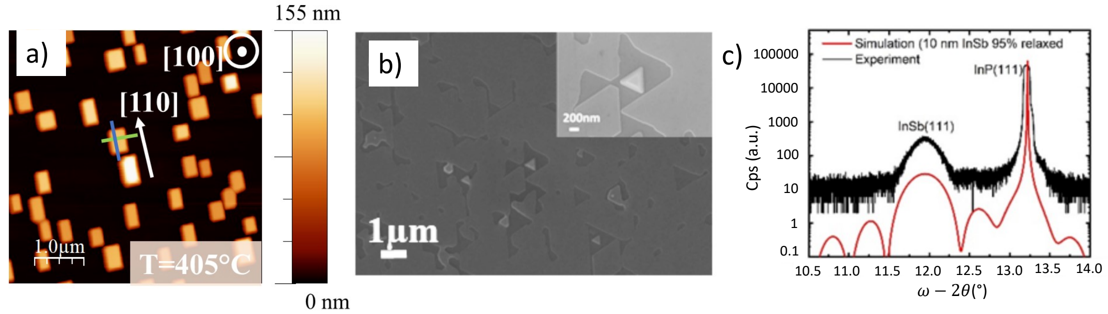


Figure 1.14: a) **AFM** image of a 10 nm-thick InSb film on InP (100) substrate. b) **SEM** image of a 10 nm-thick InSb film on InP $(111)_B$ substrate. The inset shows a magnified view focusing on a hillock. c) **XRD** spectra of the same sample from b). Extracted from[22].

Based on these observations, the low surface energy of (111)-oriented III-V substrates appeared to promote the smooth growth of InSb films in spite of the high lattice mismatch. In this regard, this observation supports the choice of a $(111)_B$ oriented GaAs substrates in the remaining of this work to aim at achieving smooth InSb thin films. For the **SAG** of nanostructures, the impact of induced defects from lattice mismatch on the electronic properties will potentially be limited. Indeed, with a proper aspect ratio of the dielectric mask, the dislocation density can be reduced.

1.4.3.2 Growth on GaAs highly mismatched substrate

A plethora of studies concentrated their efforts in accommodating and optimizing the InSb growth on GaAs substrates. In order to counteract the usual 3D **VW** regime when grown on (001) GaAs substrate, Debnath *et al.* used a low temperature InSb seed layer to produce high quality layers. The seed layer was first deposited at lower temperature (300 °C) before heating up for the remaining of the growth at 380 °C without growth interruption. With this two-step process, an electron mobility ∼53000 $cm^2.V^{-1}.s^{-1}$ at **RT** for a 2 μm thick InSb film was obtained.[99]

While the growth of InSb on GaAs (001) substrate was mainly following a 3D islands **VW** regime after only 2 **ML**s on (001) substrate, the use of (111) type substrate was shown to modify completely surface kinetics, favoring film flatness in this case.[100] Kanisawa *et al.*[101] demonstrated this effect by transitioning from a (001) to $(111)_A$ GaAs substrate in optimized growth conditions ($\mathbf{V_G}$ = 0.1 nm/s) to produce smooth 2D InSb layers. The film was grown using a two-step process (3 nm at 310 – 325 °C, then 97 nm at 380 – 395 °C) under a V/III ratio close to unity. The resulting 100 nm InSb film exhibits reduced roughness and enhanced transport properties with room temperature Hall mobility of about 4500 $cm^2.V^{-1}.s^{-1}$.

Nevertheless, the use of a strain-relaxing $Al_xIn_{1-x}Sb$ buffer layer proved to be the most efficient way to produce high quality InSb layers on GaAs. Due to its larger band gap, it also helps confining electrons into InSb. For sufficiently low values of x, the metamorphic layer will avoid the InSb channel relaxation. R.M. Biefeld and J.D. Phillips demonstrated that using an $Al_{0.12}In_{0.88}Sb$ thick buffer layer on GaAs substrate, they optimized the trade-off between bandgap and lattice mismatch. As a result, they could measured a **RT** electron mobility as high as 40 000 $cm^2.V^{-1}.s^{-1}$ for a 0.55 μm-thick InSb layer.[102]

As described in Figure 1.15, more complex **QW** heterostructures were imagined using this AlInSb buffer layer. For instance, an upper barrier with doping plane or even with metallic top gate was added, to aim at tuning transport properties. In these recent works, electron mobility of more than 240 000 and 350 000 $cm^2.V^{-1}.s^{-1}$ at **LT** were obtained.[103,104] The room temperature value converged around 50 000 $cm^2.V^{-1}.s^{-1}$.[104]

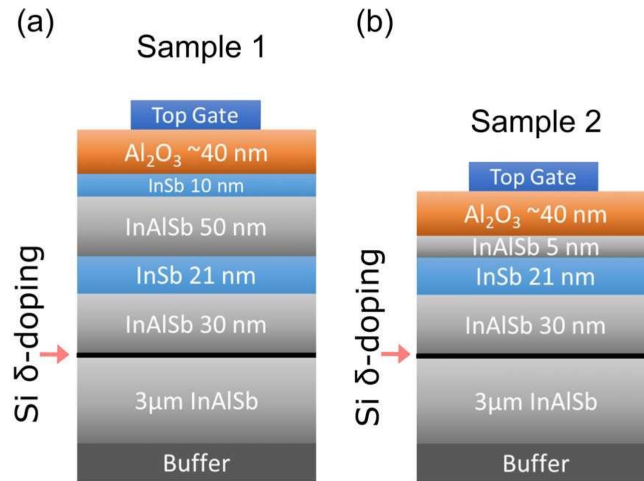


Figure 1.15: (a) Structure example of the an **QW**s. Extracted from[103]

1.4.3.3 Growth on lattice-matched CdTe substrate

Due to the larger commercial availability of InSb substrates, numerous studies were applied to CdTe epitaxial growth on InSb substrates (mainly (001) orientation), either in thin film or multilayered structures.[105,106,107,108] Although they have almost perfect lattice matching, several downsides were evidenced through this material combination in later works.

Inter-diffusion problems have been identified between the two compounds. At the interface, an In_2Te_3 layer was observed through Auger depth profiles within the structures. This inter-diffusion phenomenon is deemed to arise from growth parameters such as the beam fluxes (favoring a stoichiometric imbalance), the growth temperature or even the growth rate. Authors pinpointed that for $\mathbf{T_G}$ > 300 °C significant inter-mixing occurs. Increasing the growth rate or beam fluxes (Cd overpressure for CdTe growth) is the only way to mitigate this effect. A convenient growth temperature range was defined for roughly 175 °C < $\mathbf{T_G}$ < 275 °C in order to limit such phenomenon.[107,108,109,110] Among the few studies that investigated InSb grown on CdTe (001)[109] and (111) substrates,[110] similar interdiffusion problems at higher growth temperatures were evidenced.

The thermal incompatibility between the two materials is the second drawback of this system. While CdTe is confortable in low temperatures below 300 °C, InSb growth is preferential above 350 °C. As a matter of fact, this compels researchers to find an optimal trade-off to achieve good structural and electrical properties in such heterostructures.

Nevertheless, recent studies pursued in the possible InSb integration through lattice-matching CdTe layers in **QW**s heterostructures. A group of scientists from Shanghai University (J. Li, Y. Zhang, C. Thang *et al.*) dedicated several studies on the growth of InSb/CdTe heterostructures on GaAs (111) substrates by **MBE**. They made use of the CdTe as a buffer layer to limit the

induced defects within its thickness and grow high quality InSb film on top. Using a 1.2 µm thick CdTe buffer, they could achieve electrically active InSb (low mobility μ of 300 cm²/V.s at **RT**). In contrast, InSb was found to be insulating in the case of InSb/GaAs structure for a similar 10 nm InSb layer.[111] Based on their optimized growth conditions, complementary studies were done on **QW** structures (Figure 1.16).

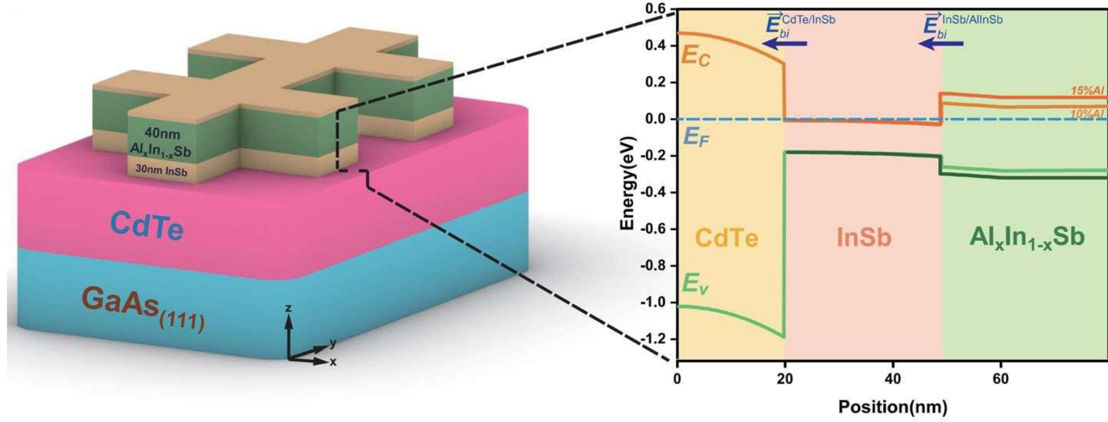


Figure 1.16: Schematic of the heterostructure in the form of Hall bar device, with corresponding simulated band diagram of the **QW**. The stack is as following: InSb (2 nm)/$Al_xIn_{1-x}Sb$ (40 nm)/InSb (30 nm)/CdTe (400 nm)/GaAs heterostructures. Extracted from[112].

An asymmetric **QW** was built with an $Al_xIn_{1-x}Sb$ barrier on top of InSb layer to focus on possible **SOC** properties. For optimized Al content (x = 15 %), they reached a mobility of 4400 $cm^2.V^{-1}.s^{-1}$ at 1.5 K with carrier concentration of 5.2×10^{12} cm^{-2}. On another hand, thanks to this design, they could achieve very high Rashba coefficient values of 0.23 eV.Å (at 1.5 K) from the magneto-conductance curves.[112] The Rashba effect arises in systems where asymmetric built-in potential is found. This **QW** structure demonstrates it because the inversion symmetry is broken thus causing energy bands to split in the presence of an electric field. The coefficient α_R defines how strong **SOC** is, in the system. Last but not least, the same group showed effective control of the Rashba effect using a **FET** device with similarities in the structure (thicker CdTe buffer layer of 1.2 µm, no $Al_xIn_{1-x}Sb$ layer). Through gate voltage modulation, a clear ON/OFF state (10^4 change in the current value) and tuning of the Rashba coefficient from 0.47 to 0.73 eV.Å was observed.[113]

Despite the exposed inter-diffusion phenomenon, if abrupt InSb/CdTe interfaces are grown within properly engineered devices, this system predicted to exhibit topological insulation properties can pave the way towards advanced quantum application.[114]

1.4.4 One Dimensional InSb Integration

1.4.4.1 InSb NWs Growth techniques

In order to achieve advanced mesoscopic devices for quantum computing applications like the **MZM** devices described in section 1.2.1, low dimensions nanostructures (1D or 0D) remain the core component for that. As specified, semiconductor **NWs** (1D) were extensively studied. Therefore, a perfect control of every growth parameter is crucial to realize **NWs** with quantum-compatible electronic properties. As of today, three different approaches are commonly defined as the reference techniques for the growth of **NWs**.

Vapor Liquid Solid
The first technique called **VLS** was discovered by R.S Wagner and W. C. Ellis in 1964. Through the synthesis of Si whiskers using a gold catalyst droplet, this bottom-up approach has since became the main fabrication technique for **NW** epitaxial growth.[115]

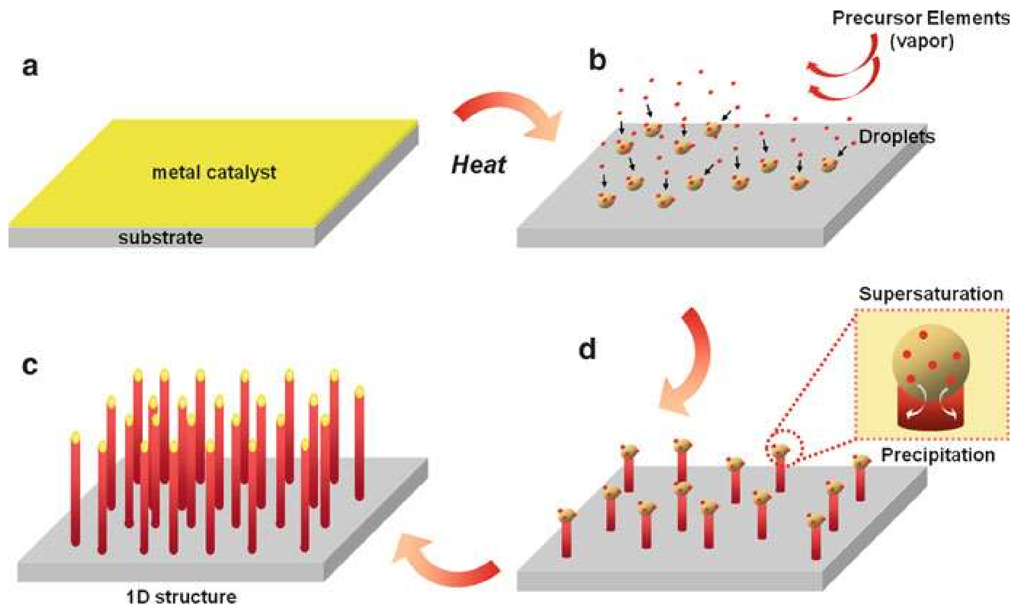


Figure 1.17: Schematic of the various steps for the **VLS** growth mechanism of a **NW**. a) the metallic catalyst is deposited on the substrate. b) Upon heating above the eutectic melting point of the metallic catalyst, droplets are formed. d) Under continuous precursors exposure, catalyst supersaturation is reached which enables crystallization of the excess semiconducting atoms at the interface. c) End of the **NW** growth. Extracted from[17].

The **VLS** relies upon the reaction between a metal catalyst and precursors in vapor phase to grow the **NW** (Figure 1.17). At first, only Au or Ni catalysts were used, while nowadays even III-elements like Ga or In are also possible. The substrate is heated to a temperature beyond the metallic droplet eutectic melting point. It forms a liquid alloy with the semiconductor precursor and act as a seed for the **NW** growth. Following continuous exposure to the precursors, the liquid catalyst becomes supersaturated. The excess semiconducting atoms will then travel to the liquid-solid interface and crystallize initiating the vertical **NW** growth.[116]

Several key aspects of **VLS** can be mentioned from the numerous studies done throughout the years. The angle of the grown **NWs** with regards to the substrate depends on different factors. First, the substrate orientation, which affects minimization of the total system free energy. Then, the contact angle of the catalyst droplet with the surface. Eventually, surface diffusion kinetics also play a role about the **NWs** verticality. Altogether, these parameters affect the tilting angle of the grown **NWs**.[117,118]

Vertical NW growth using VLS
Because the contact area with the substrate is reduced, the vertical growth of InSb **NWs** by **VLS** remains the primary technique to produce these 1D nanostructures. Either a direct growth on InSb or other III-V substrate is possible. Although in the latter case the mismatch will induce defects, the surface area remains small ensuring high structural quality over **NWs** length. Over the years, the possibilities offered by **VLS** growth multiplied. At first, homoepitaxy on unmasked

substrate[119] was used to produce randomly distributed **NWs** on the surface. Nowadays, core-shell **NWs** heteroepitaxy on patterned substrate can be grown with accurate control.[120] In such examples, hole arrays are defined via e-beam lithography to control gold catalyst and **NWs** diameter. On top of the enhanced localization, vertical heterostructures were built such as InSb/InAs examples.[62,121,122,123,124] Through carefully optimizing the growth conditions, especially V/III ratio, a variety of different InSb **NWs** shapes can be obtained from vertical to nanocrosses as shown in Figures 1.18a and b.

G. Badawy *et al.* attempted to achieve an all-in-one vertical heterostructure. They realized semiconductor-superconductor **NWs** based on core InSb/shell CdTe with Al or Pb superconductor overgrowth.[125,126] The shell thickness is controlled to ensure a tunneling barrier and proper proximity effect with the superconducting layer. This latter deposition was made possible through the complex use of "shadow" deposition, defined by exposing the vertical **NWs** to a beam flux but with a specific angle of incidence (Figures 1.18c, d, e and f).

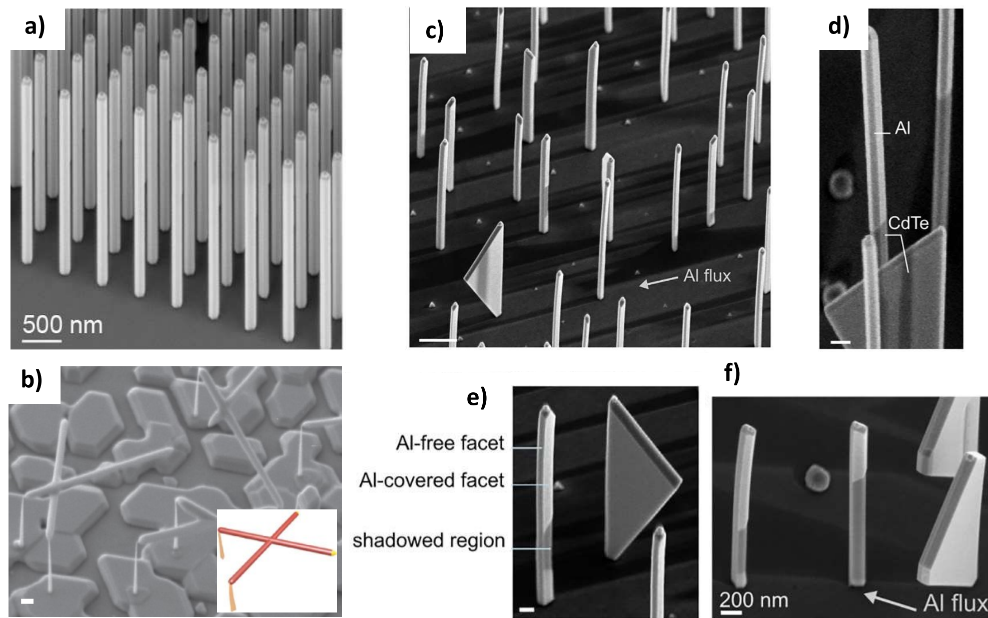


Figure 1.18: **SEM** images of a) Stemless InSb **NWs**.[121] b) InSb nanocrosses grown on InP (111)/InAs stems (scale bar: 200 nm).[127] **SEM** image of core-shell InSb/CdTe **NW** after selective deposition of Al via shadowing c) (scale bar: 1 µm). Al covered and free regions d) visible yielding either narrow e) or wide f) superconducting/normal junction(scale bar: 200 nm).[126]

In the same line, Khan *et al.* explored superconducting β-Sn deposition on various III-V vertical **NWs**. In the case of InSb and InAsSb, a mixture of both semi-metallic α-Sn and superconducting β-Sn was obtained. α-Sn region was attributed to its quasi-identical cubic crystal structure with InSb. On the other hand, the β-Sn domains seemed to nucleate from defective sites and expand with increasing thickness.[128]

In spite of the numerous perks of **VLS**, this self-assembled growth technique lacks of scalability. As a matter of fact, it is not possible to process several **NWs** in parallel, as each of them need first to be transferred on a host substrate. Eventually, many questions regarding metal contamination from the droplet within the **NW** were raised. Nevertheless, with careful control of growth conditions and micro-manipulation, the **VLS** remains the main considered technique in growing high epitaxial quality **NWs** for quantum testing.

Selective Area Growth

Together with the development of lithography and etching techniques within patterning processes, **SAG** emerged slowly in the late 1970's.[129] In contrast with **VLS**, the position and the shape of the nanostructures can be controlled with a high precision for **SAG**. To do so, a dielectric mask usually made out of oxide (SiO_2 historically) is deposited on the substrate surface. Then, this latter is patterned to design structures of various shapes and orientations. **SAG** rapidly gained success by tailoring the properties of the semiconducting layers due to the variation in shapes, crystallographic orientation or composition.[18]

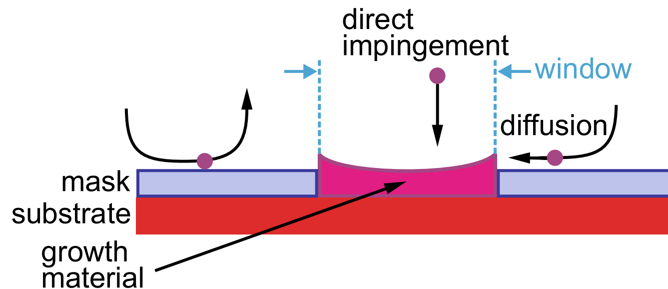


Figure 1.19: Schematic of selective area growth. Under proper conditions, growth only occurs in the window of the mask. Material is supplied from both the species direct impingement or through the surface diffusion of particles. Extracted from[130].

Because only a patterned substrate is needed, various epitaxial techniques are compatible with **SAG**. Suppression of parasitic growth on the mask is favored when adatoms have a low sticking coefficient on the mask and a large diffusion length.[130,131] As the metalorganic precursors in **MOCVD** have a lower sticking coefficient than molecular beam species, the former technique is more efficient in reaching high selectivity. But, by carefully tuning the growth conditions, **MBE** can be used for **SAG** while avoiding poly-crystalline growth on the mask. As depicted in Figure 1.19, in favorable experimental conditions, material growth occurs only inside the aperture, supplied either through the direct impingement of the species or via the adatoms that diffused on the mask surface. To get a high selectivity, *i.e.* epitaxial growth only on the semiconductor surface, the growth conditions must be optimized to ensure the reevaporation of impinging atoms on the mask or their diffusion towards the apertures.

In the case of III-V **SAG** using a dielectric mask, selectivity is driven by the desorption of the adatoms on the mask surface. Oppositely, through the use of a patterned graphene mask, the III-element surface diffusion length was found to govern.[132] Based on these experimental observations, many studies focused their work on kinetic models and simulations to extract the criteria for perfect selectivity.[133,134,135] Logically, they emphasized on the growth and design parameters dependency of the selectivity window. For instance, Cachaza *et al.* observed a different growth behavior depending on the width of **NWs**. While no growth occured at all for a 45 nm-wide **NW**, a smooth growth in the case of a 150 nm-wide **NW** was obtained. They highlighted that such change in design affected the overall kinetics to transition into different regimes (source, sink, balance,...).[136] Consequently, any deviation in the growth or design parameters significantly impacts selectivity. Therefore, a rigorous control of the entire process parameters is of utmost importance to achieve **SAG**.

By chance, few years back, Aseev *et al.* proposed a study on both GaAs and InAs **SAG** to construct a selectivity map. This useful tool indicates the suitable parameters range (growth temperature and rate) to reach high selectivity.

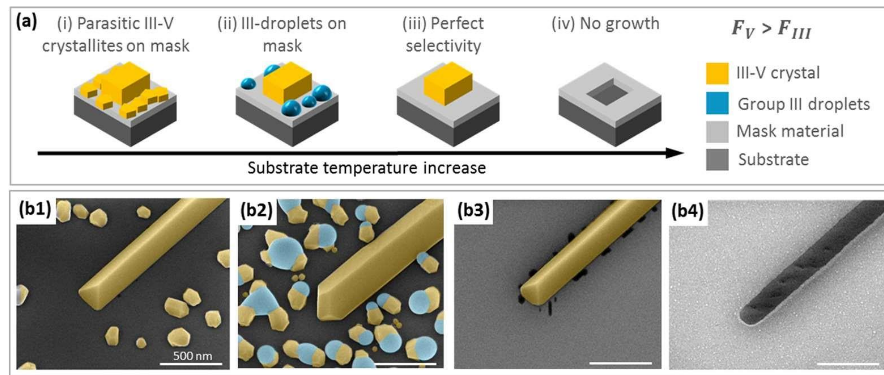


Figure 1.20: a) Schematic of the III-V growth modes in **SAG** depending on substrate temperature. GaAs growth at substrate temperature of b1) 610 °C with As flux during cooling b2) 600 °C with As decreasing flux during cooling b3) 630 °C allowing selective growth b4) 690 °C where evaporation during growth occurs. Extracted from[19].

As illustrated in Figure 1.20, for the convenient growth temperature and beam fluxes range, perfect selectivity can be achieved. In addition to that, they also recalled that the selectivity window could be extended through the use of a $\mathbf{H_{AT}}$ flux during **SAG**. Indeed, such reactive species prevent crystallites nucleation on the mask (via formation of volatile compounds with element-III droplets on the mask).[137] Altogether, these advices helped significantly any **SAG** to find the suitable set of parameters to achieve high selectivity.[138]

Previous work conducted by the EPIPHY group confirmed the extension of the selectivity window through $\mathbf{H_{AT}}$ plasma during growth.[139,140] In this regard, we will focus on attempting $\mathbf{H_{AT}}$-assisted **SAG** by **MBE** of InSb in-plane **NWs** growth on the aforementioned substrates: CdTe and GaAs. Selectivity map will be adapted (growth and design parameters) to cope with possible hindrance coming from layer-substrate combination.

In-plane InSb NWs through SAG

As a response to the aforementioned **VLS** limitations, direct in-plane **NW** growth through **SAG** using **MBE** has a chance to solve these problems. Due to the larger surface contact area with the substrate that is more prone to defects, fewer studies were done.

The growth of in-plane InSb **NWs** on mismatched substrates through **SAG** was demonstrated several years ago by the EPIPHY group at **IEMN**. There, the growth of a 600nm $Al_{0.8}Ga_{0.2}Sb$ buffer layer was done on a GaAs (001) substrate to accommodate most of the lattice mismatch. After a SiO_2 masking process and apertures opening, InSb $\mathbf{H_{AT}}$-assisted **SAG** by **MBE** was performed yielding a nanostructure free of threading defects.[139]

The following year, Aseev *et al.* ingeniously used a trick to mix the **VLS** and **SAG** method.[141] As in the former technique, they used a metal catalyst, this time being directly an In droplet (instead of the usual gold droplet). Within a patterned mask as in **SAG**, they could grow directly in-plane nanostructure through what they called the "metal-sown-epitaxy" technique. Complex networks with excellent morphology could be achieved with this. During conventional **SAG** of InSb on III-V mismatched substrates (here InP), apertures are poorly filled. Indeed, depending on the growth temperature, a trade-off between optimal selectivity and nucleation conditions must be found. But with this method, the In droplet firstly deposited acts as a group-III reservoir for subsequent InSb growth. After the droplet is deposited, only Sb flux is supplied to start nucleation. Then, both In and Sb are supplied after raising substrate temperature to grow high quality InSb **NWs** (Figures 1.21a, b, c and d).

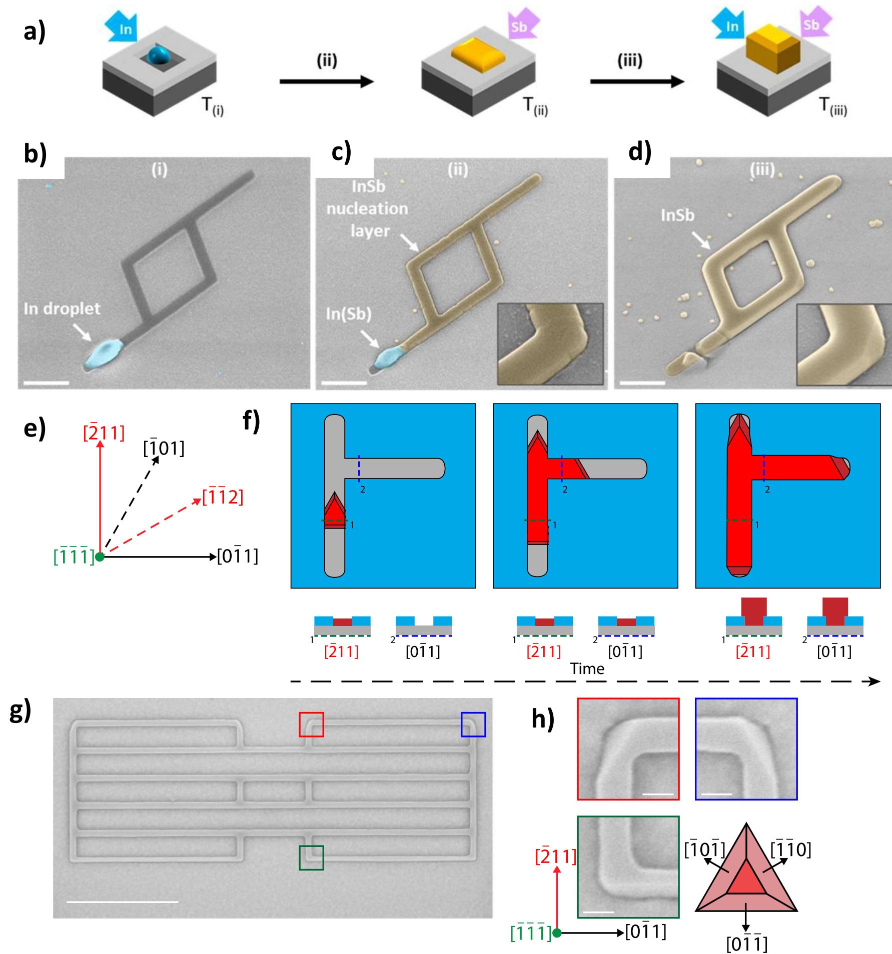


Figure 1.21: a) Schematic of the metal sown **SAG** of InSb nanostructures. b) **SEM** images of the different growth steps for a nanoring structure. Indium droplet is deposited inside the aperture. c) Sb is supplied for InSb nucleation layer. d) Both In and Sb are then supplied to pursue the **SAG** (scale bar: 500 nm). Adapted from[141]. e) The favorable growth directions for in-plane **NWs** growth on $(111)_B$ type substrate. f) Schematic of InSb in-plane **NWs** via **SAG** on an InP $(111)_B$ substrate at different time of the growth. Below each panels a cross-section scheme shows the InSb **NWs** height relative to the 20 nm thick Si_3N_4 mask (light blue). g) Resulting in-plane InSb **NWs** grown on InP $(111)_B$ in controlled conditions (Scale bar: 1 µm). h) Zoom-in on the colored squares in g) showing the corners of the nanostructure with a scheme illustrating the stable facets formed (Scale bar: 50 nm). Extracted from[142].

Recently, Op het Veld *et al.* proposed another approach through **MOCVD** to grow high-quality in-plane InSb **NWs**.[142] In order to discard the possible threading defects induced by lattice relaxation, they promoted the use of (111) substrates. Instead, strain relaxation is only restricted at the interface. To minimize the defects induced from nuclei merging, the authors increased the V/III ratio to large values (> 30000) in order to obtain a single nucleation point. In such growth conditions, interconnected **NW** networks are achieved consistently with a narrow diameter of 60 nm and several microns lengths (Figures 1.21e, f, g, h).

Template Assisted Selective Epitaxy
Last but not least, a recent technique is still relevant to be mentioned, as it promotes an interesting approach to ease III-V **NWs** integration on Si substrates. This technique called **Template Assisted Selective Epitaxy (TASE)** was demonstrated by H.Schmid *et al.* at IBM[143] and refers to the growth of III-V **NWs** assisted through a Si seed in a designed template. As shown in Figure 1.22, the template is prepared through several process steps and could be even combined with direct superconductor deposition upfront (here TiN).

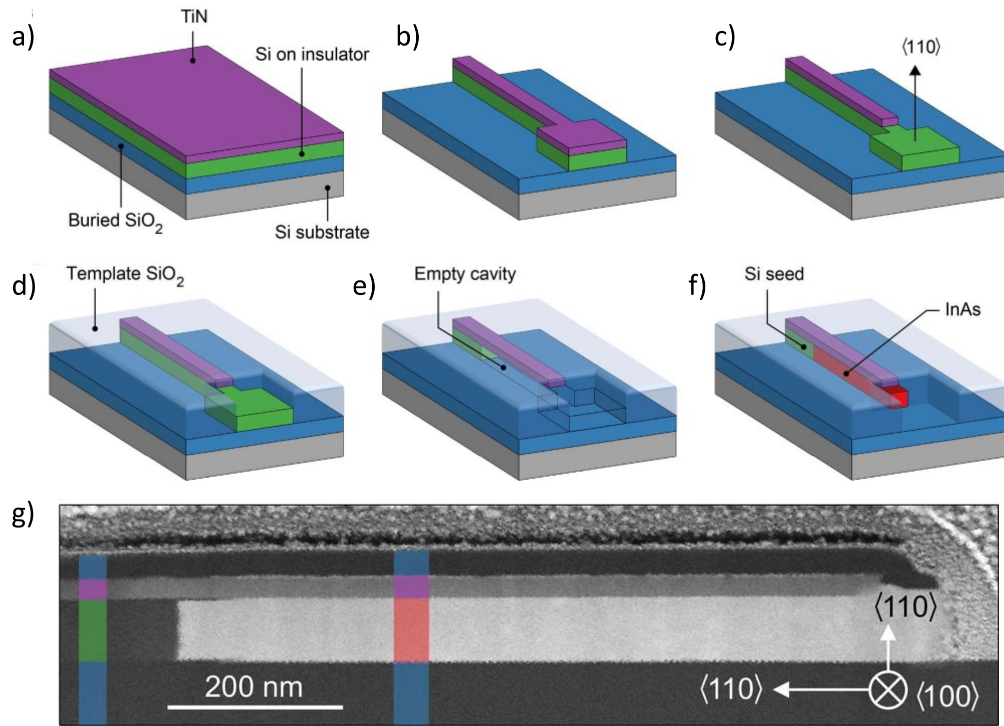


Figure 1.22: a) The silicon-on-insulator wafer is covered with a 20 nm-thick TiN film. b) Patterning of the structure is performed, here in the form of a **NW** with a square end. c) Etching of the TiN layer on the **NW** end. d) 40 nm-thick SiO_2 deposition followed by selective etch to expose a Si square. e) The cavity in the SiO_2/TiN template is formed through selective etching of the Si layer. f) InAs **NW** growth guided by the Si seed and template. g) **STEM** image of the device in a longitudinal cut (along the axis of the **NW** growth). The colored boxes refer to the different layers in f). Adapted from[144].

Starting from the TiN/silicon-on-insulator wafer (a buried SiO_2 layer separating a thin Si layer from the Si substrate), the structure is first patterned (Figures 1.22a and b). In a second time, the TiN is etched selectively before SiO_2 is deposited then etched as well (Figures 1.22c and d). To form the cavity, the Si is also etched back to leave only a small seed region that will promote the III-V **NW** growth, InAs by **MOCVD** in this case (Figures 1.22e and f). This method allows to get a high control over **NWs** shapes and defect filtering via template sidewalls and geometry. Additionally, this techniques offers a direct back-gate control thanks to the insulating SiO_2 layer and a direct scalability towards 3D and monolithic integration on Si.[144] Despite the possibility to build complex networks and ballistic devices as well, the studies so far concentrated their efforts on InAs **NWs** via **TASE**, leaving behind InSb or any extension of this process towards other substrates than Si.

1.5 InSb-based devices

With respect to InSb quantum-compatible device development, each of the very many studies strove to further enhance transport properties through increased electron mobility for instance. Whether the devices are **2DEG** or **NWs**-based, extensive efforts were made to probe their electrical properties resulting from growth or design improvements. Therefore, this section proposes a detailed review of the various InSb-based devices to determine the scope of this work in light of the current state of the art.

1.5.1 2DEG-based InSb devices

As indicated in Table 1.1, large electron mobilities were achieved through InSb **QW** structures. Both designs relied on the use of an AlInSb buffer to minimize strain in the InSb **QW** and accommodate the mismatch from GaAs (001) substrate. However, the overall InSb **QW** structure differed with a double-sided-δ doped layer proposed by Lehner *et al.*[54] (Figure 1.23a), while the second adopted an asymmetric Si-δ doping plane[60] (Figure 1.24a).

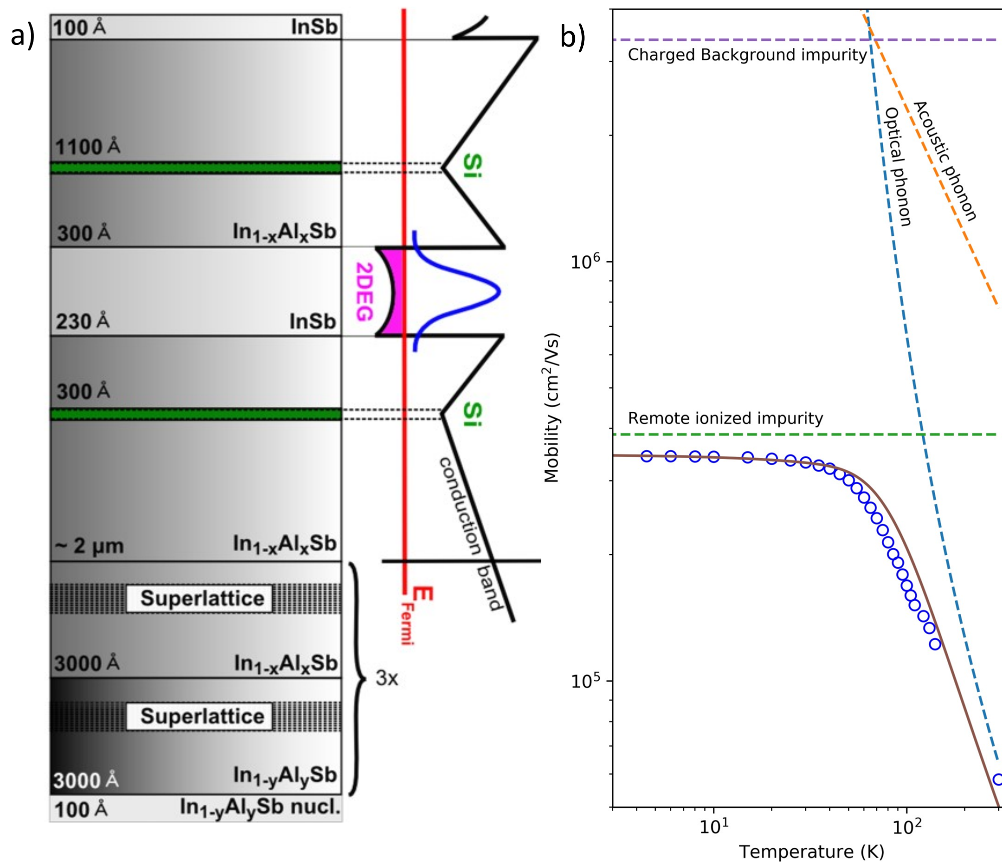


Figure 1.23: a) double-sided-δ doped **QW** structure. Aside of the scheme, the band diagram with first order wave function is added. b) Temperature-dependent mobility plot for the highest mobility sample. Open circles is the experimental data, fit is in solid line. Dashed lines correspond to the simulated mobilities limited by the different scattering mechanisms. Extracted from[54].

In the former case, an electron mobility as large as 349 000 cm^2.V^{-1}.s^{-1} for a carrier density of 4.90×10^{11} cm^{-2} at 1.3 K is obtained for such symmetrically doped 23 nm-thick InSb **QW** with a 30 nm spacer after growth optimization. Through a reduced dislocation density using a GaSb instead of AlSb first intermediate buffer, the minimal disorder allowed to extend the electron mean free path up to 4.031 µm. Because this value is larger than the average distance between threading dislocations, their impact is negligible on the InSb **QW** transport properties. Despite such improvement, the temperature-dependent mobility chart in Figure 1.23b demonstrates that the remote ionized impurity scattering is the limiting factor. At **RT**, the optical phonon scattering (lattice vibration) comes into play, drastically reducing the mobility to 58 000 cm^2.V^{-1}.s^{-1} at an electron density of 1.04×10^{12} cm^{-2}.

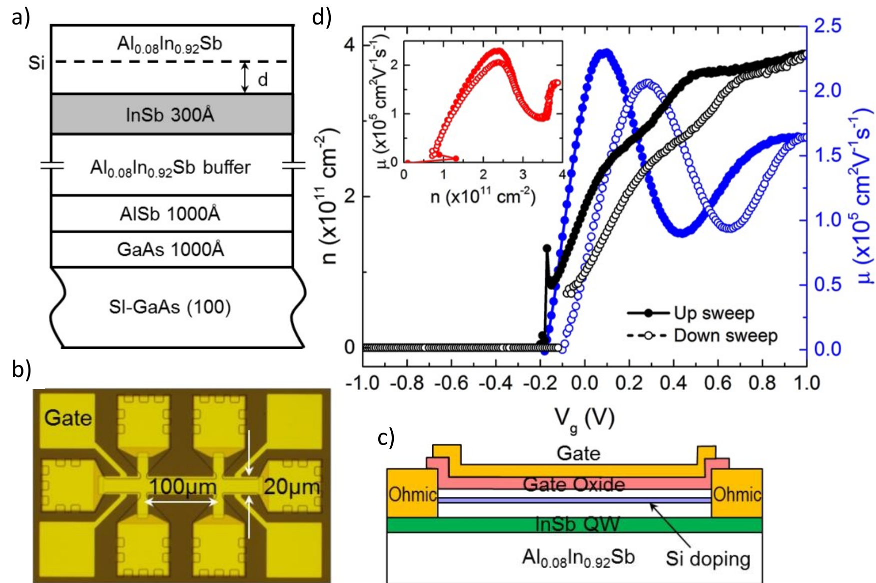


Figure 1.24: a) Schematic of the asymetric InSb **QW** heterostructure. b) Example of the gated Hall-bar device with the cross-section sketch in c). d) Carrier density and electron mobility as a function of gate bias under $\vec{B}$ = 0.1 T. Inset corresponds to electron mobility vs. carrier density plot. Extracted from[60].

In the asymmetrical InSb **QW**, Yi *et al.* fabricated Hall-bar devices as illustrated by Figures 1.24b and c. At a temperature of 1.8 K, authors confirmed an electron mobility exceeding 200 000 cm^2.V^{-1}.s^{-1} with a peak value around 230 000 cm^2.V^{-1}.s^{-1} for low positive gate voltage. While the device exhibits proper channel pinch-off for small negative gate voltage $V_G \approx$ -0.17 V, a surprising behavior is observed in the positive gate voltage range (Figure 1.24d). After electron mobility peaks at around V_G = 0.1 V, a decrease in its value is observed with a corresponding change in the carrier density versus gate voltage slope. This effect is consistently explained through the population of a lower mobility channel in the δ doping layer.

1.5.2 VLS based InSb devices

As mentioned in the previous section 1.4.4.1, the grown vertical **NWs** need to be transferred onto a host substrate in order to fabricate **NWs**-based **FET** devices. For most cases, a SiO_2 covered doped Si substrate is used to host the **NW**. Designs can differ but generally include Ti/Au metal contacts and either a top or back-gate (using p-type Si substrate) to build the **NWs-FET** devices (Figures 1.25a, b, c and d). Because of their high aspect ratio and smaller mismatched induced

defective area, the electron mobility is usually over 10 000 $cm^2.V^{-1}.s^{-1}$ at cryogenic temperature, depending on the dimensions. Reported values at **LT** (4 K), with several references from section 1.4.4.1, are as follow:

- 20 000 < μ < 35 000 $cm^2.V^{-1}.s^{-1}$ with $n = 1 \times 10^{17}$ cm^{-3} and mean free path of 260 nm for a 100 nm-wide InSb **NW** is reported by Plissard *et al.* from six devices[62] (Figure 1.25b).
- Core-shell CdTe/InSb **NW**-**FET** devices from Badawy *et al.* exhibited an electron mobility of μ = 21 500, 26 000, 14 000 and 17 000 $cm^2.V^{-1}.s^{-1}$ for channel lengths of 1, 2, 3 and 5 µm respectively. Values were extracted from I versus V_{BG} pinch-off curves on several 120 nm **NWs** diameter[125] (Figure 1.25d).
- Another study of the same authors on the stemless InSb **NWs** (Figure 1.21e) revealed average electron mobility μ = 44 000 $cm^2.V^{-1}.s^{-1}$ from 15 **FET** devices. The **NW** diameter ranges from 130 to 190 nm and source-drain separation between 1-2 µm. For largest separation, output characteristic curves of quantized conductance G showed well-defined e^2/h plateaus under $\vec{B} > 5$ T (Figure 1.25e).[121]
- Gül *et al.* obtained an average electron mobility of 24 000 $cm^2.V^{-1}.s^{-1}$ from around 10 devices with InSb **NWs** diameter of approximately 100 nm. In the work, they also pinpointed the very high impact of surface adsorption on the actual transport properties.[63]

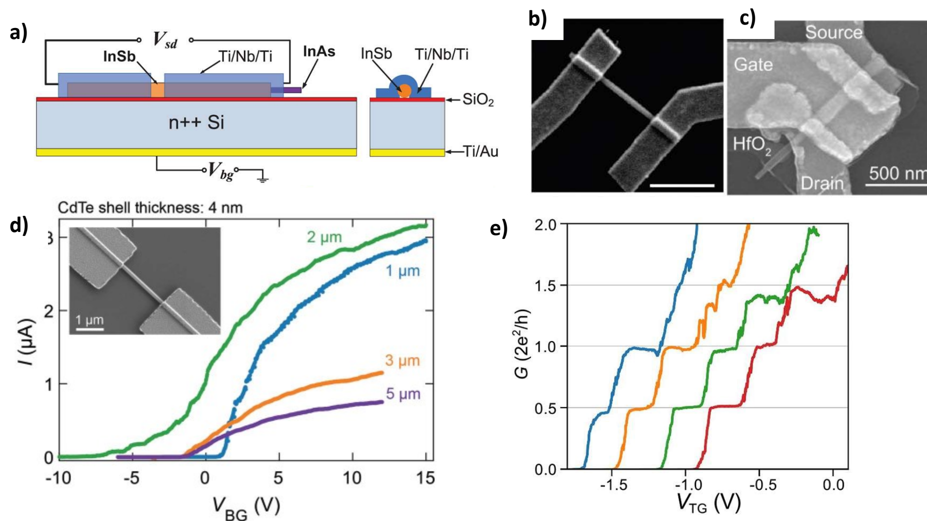


Figure 1.25: Various **NW FET** devices designs for transport measurement from[41] in a), [62] in b) and [123] in c). d) **LT** pinch-off current vs back-gate voltage curves of core-shell InSb/CdTe **NW** transferred onto a SiO2/p-doped Si substrate. The different curves in these **FET** devices refer for various channel lengths. Extracted from[125]. e) **QPC** versus top gate votalge of the device showing e^2/h quantized plateaus at 6 K. Extracted from[121].

In spite of the reduced electron mobilities in **NWs**-**FET** devices due to the increased surface scattering, undeniable excellent transport properties can still be achieved through **VLS** grown **NWs**. Moreover, the report of the **NWs** is usually done onto an insulating layer grown at the surface of a doped host substrate, enabling a back-gate effect. Nevertheless, this report of the **NWs** onto a host substrate accounts for a scalability problem. Even though lots of progress were made in micro-manipulation, this results in **NW** uniqueness, preventing reproducible and scalable devices production.

1.5.3 In-plane InSb-based devices

As discussed earlier, the **SAG** of in-plane InSb **NWs** eases the fabrication of scalable devices. Even though a greater disorder (*i.e.* increased defect density) resulting in lower electron mobility is induced during fabrication, the few studies conducted have still demonstrated interesting transport properties that could be further enhanced over time. Coming back onto the InSb **FET** devices built using an AlGaSb mismatch accomodating layer (Figure 1.26a), a proper channel pinching with an ON/OFF current ratio of 10^4 at 77 K for a 3 µm channel length was observed (Figure 1.26b). The **FET** mobility variation for low temperatures highlighted the importance of surface impurities and native oxide layer that degrade transport properties significantly.[139]

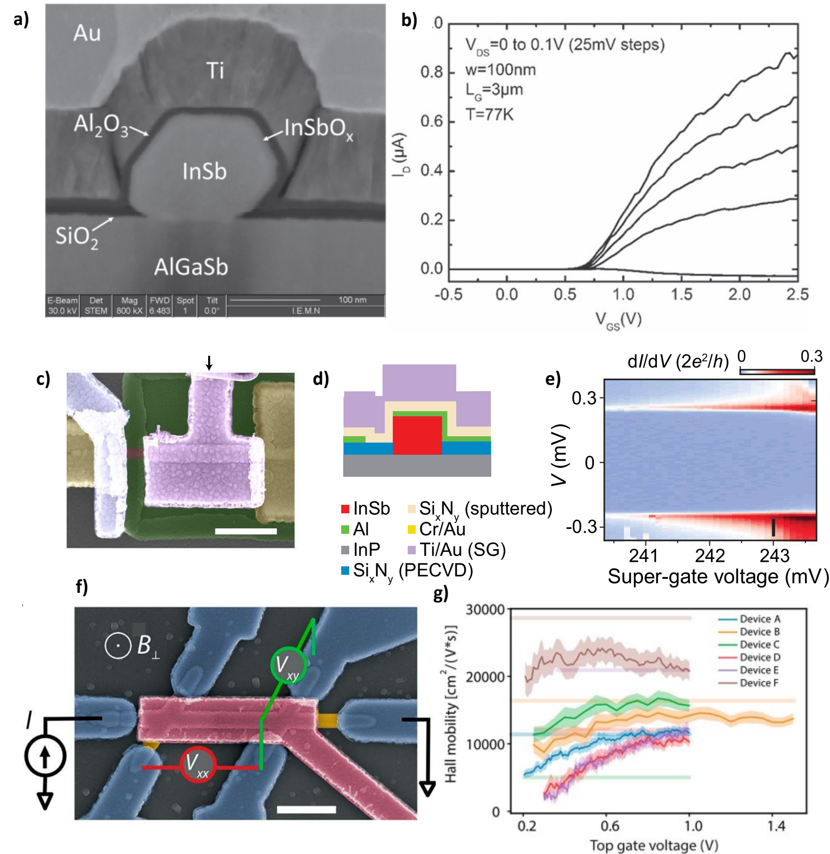


Figure 1.26: a) Cross-section **FIB-STEM** image of the InSb **NW-MOSFET** from a 100 nm aperture width. b) Drain current versus gate voltage of the fabricated **NW-MOSFET** at 77 K for a gate length of 3 µm. Extracted from[139]. c) False-colored **SEM** image of a semiconductor-superconductor **NW** device with d) a schematic cross-section view. e) Differential conductance (dI/dV) versus bias voltage and super-gate voltage. A superconducting gap of ~250 µeV is observed. Extracted from[142]. f) False-colored **SEM** image of an in-plane Hall bar structure for transport measurement. Cr/Au contacts are in blue, gate electrode in red separated from the InSb **NW** in yellow through a sputtered SiNx dielectric (invisible) (scale bar: 1 µm). g) Hall mobility vs top gate voltage of each devices. Extracted from[141].

As presented in the previous section 1.4.4.1, through their single nucleation point technique by **MOCVD**, Op het Veld *et al.* could generate complex in-plane InSb **NWs** networks and build devices with different shapes. In this regard, an Al superconducting layer was deposited

and etched selectively (Figures 1.26c and d). From the measurements, a superconducting gap (~250 µeV) was evidenced together with a phase coherent length of 9 µm through other types of designed InSb nano-devices (Figure 1.26e)).[142] The large value reported means electron coherence is preserved without any defect scattering over long distances. This striking progress is an important asset for hybrid **NWs**-based superconducting devices for topological quantum computing.

Using the metal-sown epitaxy technique, Aseev et al managed to build various in-plane InSb devices like Hall-bar directly after growth (Figure 1.26f). In such structures, the Hall mobility was observed as high as 20 000 $cm^2.V^{-1}.s^{-1}$ for these devices at 20 mK. In the case of InSb **NW**-**FET** devices an averaged value of 19 000 $cm^2.V^{-1}.s^{-1}$ at 20 mK is obtained out of 16 devices (Figure 1.26g).[141]

Throughout this chapter, the importance of controlling the charge density inside the nanostructure has been mentioned repeatedly. Possible through the field-effect, any of the transport properties experiments need such control to properly determine the device characteristics. In the context of Majorana-based devices, this gating architecture becomes crucial to tune the carrier density and transit into the topological superconducting phase.

1.5.4 Semi-conducting barrier

Based on the **SAG** scalability, a full heterostructure can be grown from different material layers. Firstly, the **SAG** onto a semi-insulating substrate like GaAs or CdTe would need to be mastered to produce smooth InSb **NWs**. In a second time, the possibility to enable back-gate electrostatic control of the nanostructures without the need to report them onto a host substrate would satisfy the remaining challenges. Therefore, we aim in this work at developing in-plane InSb **NWs** including a possibility of back-gating to tune the charge density inside the nanostructures. However, we are motivated to use a semiconductor barrier replacing the conventional oxide. To grow this heterostructure, a higher band-gap material with lattice parameter ranging from GaAs to InSb is needed. Such condition must be fulfilled to maximize the layer quality and mitigate additional defects formation. Knowing these restrictions, three possible candidates stand out as either $Al_{0.8}Ga_{0.2}As$, $Ga_{0.51}In_{0.49}P$ and CdTe (Figure 1.27).

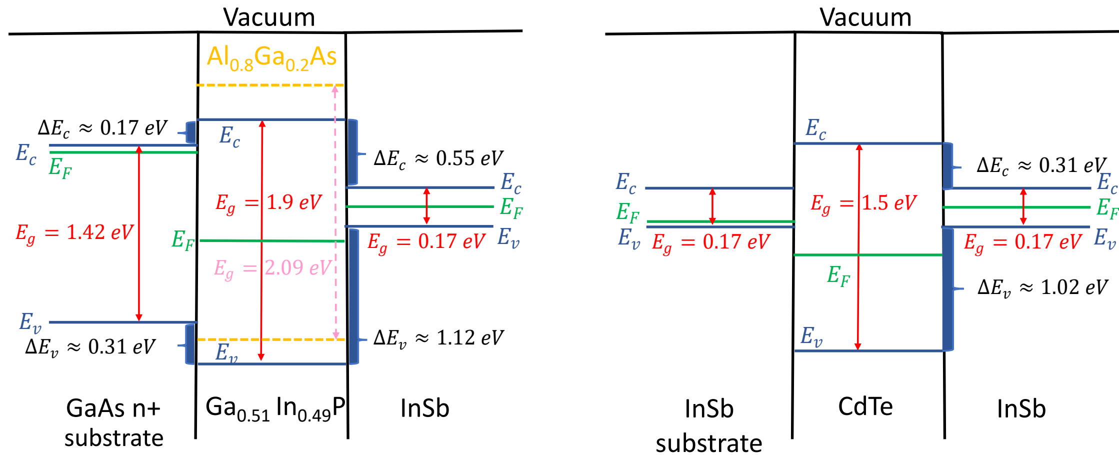


Figure 1.27: Schematic band diagram (flat-band) of the heterostructure showing band offsets with left) the two III-V semiconductor barrier candidates and right) the II-VI (CdTe) barrier. E_g, E_F, E_c, E_v stands for the band gap energy, the Fermi Level, the conduction band minimum and the valence band maximum respectively. ΔE_c or ΔE_v offset values are both estimated and extracted from[66,68,145,146,147].

In the latter case, the heterostructure InSb substrate/CdTe barrier/InSb **NWs** would also fulfill these restrictions. However, due to equipment limitations (**MBE** reactor not equipped for CdTe growth), the growth of CdTe on InSb substrate is investigated at CEA-LETI as part of this ANR project Inspiring. In this work, this system will be studied through the epitaxial growth of InSb on CdTe substrates. Regarding the III-V ternary candidates, both of them are lattice matched to GaAs for the correct composition and exhibit a band gap of 2.09 eV and 1.9 eV respectively. As depicted in Figure 1.27 , the larger conduction band offset of $Al_{0.8}Ga_{0.2}As$ with regards to GaAs and InSb would ensure a stronger carrier confinement than $Ga_{0.51}In_{0.49}P$. As a matter of fact a better gate control can be achieved together with reduced leakage current. Both materials exhibit similar range of dielectric constant (between 11 – 13). Nevertheless, both III-V compounds will need to undergo growth optimization as interface quality with InSb will strongly impact device performance and charge density control.

1.6 Thesis objectives

Throughout this chapter, the actual stakes associated to the quantum computing integration were pictured via the ambitious example of Majorana devices. The core of such system relies preferably on a semiconducting **NW** with high mobility, strong **SOI** and low electron effective mass. Using the best candidate material InSb, we summarized how it can fulfill this role.

Its quantum-appealing properties as well as the lattice mismatch accommodation were detailed in the first place. Next, we stepped into the epitaxial processes description to grow one-dimensional nanostructures (**NWs**). Among the various possibilities, **SAG** coupled to **MBE** exhibits the most convenient way to enable in-plane **NWs** growth in controlled conditions. Then, state-of-the-art studies showed how the transport properties strongly rely on the **NW** crystalline quality. The whole resulting from growth conditions and heterostructure interfaces. In the same context, device fabrication through the contact and gates deposition contribute as well to the limitation in performances.

Therefore, numerous objectives are present in this thesis. At first, we plan to investigate the **MBE** growth of InSb thin films on both lattice-matched CdTe and mismatched GaAs substrates. Extensive efforts will be done to understand and mitigate the challenges coming from either InSb/CdTe or InSb/GaAs combination. For InSb/CdTe, intermixing and thermal compatibility will be carefully addressed. In the case of InSb/GaAs, minimization of the defects propagation will be attempted. From the 2D layers understandings, InSb in-plane **NWs** through **SAG** by **MBE** will be then studied.

Extensive structural characterization will be conducted on the various InSb structures (thin films and **NWs**). Using **Low Temperature Scanning Tunneling Microscopy (LT-STM)**, surface reconstructions studies and spectroscopic measurements of the electronic states will be performed. Additionally, **STEM** cross-sectional analysis will be conducted to help getting the full picture of growth conditions and mismatch accommodation impact on transport properties.

In answer to the required gate control for quantum devices, charge density tuning inside InSb **NWs** will be explored through **MBE** growth of back-gated heterostructures. A semiconductor barrier of either AlGaAs or GaInP will be grown on GaAs $(111)_B$ substrate. A first part will assess the device feasibility for 2D thin films before aiming for in-plane carrier density modulated InSb **NWs**. The electronic transport properties of these **NWs** will be studied through Hall, **TLM** and **4P-STM** measurements to determine the electron mobility, sheet resistance and prove their effective carrier density modulation. Eventually, an **STM** study to investigate the possibility to remove the native oxide layer prior **4P-STM** based transport measurements will be performed.

Chapter 2

Experimental techniques

2.1 Introduction

This chapter is dedicated to the presentation of the growth and characterization techniques used in this work. In the first section, we detail the **MBE** system in which all samples were grown. As we consider **SAG** for the fabrication of nanostructures, the different process steps for substrate patterning are presented (Chiara Crivello performed the **Atomic Layer Deposition (ALD)** deposition and Yves Deblock the e-beam lithography). In a second time, after providing a theoretical background, the **LT-STM** and **4P-STM** machines that we used to analyze the various samples are described. The remaining structural, morphological and electrical characterization techniques (**AFM**, **XRD**, **TLM**, Hall effect) will be reviewed from both a theoretical and practical point of view. On top of the "routine" analysis performed throughout this thesis, all the aforementioned experimental techniques were used in a completely autonomous way unless the **MBE** machine that requires an extensive handling experience, where Christophe Coignon, **MBE** engineer intervened. Resulting from a collaboration in the scope of the "PROCOPE" project, the **STEM** images presented in the following of this work were acquired at **Jülich Forschungszentrum***, for which i participated as well, and the **Focused Ion Beam (FIB)** lamellae preparation was executed by Qianqian Lan and David Troadec (**IEMN**) respectively. Regarding the structural **X-Ray Photoelectron Spectroscopy (XPS)** analysis conducted in the next chapter, this latter was performed in-house by Xavier Wallart.

2.2 Molecular Beam Epitaxy

2.2.1 General presentation of the growth system

Discovered in the late 1960s', **MBE** proficiently stood out as the reference growth technique for very high purity and crystalline thin films deposition. At first used for compound semiconductors growth, **MBE** nowadays allows processing a wide variety of oxides, metals and ceramics as well. The essence of the epitaxial relationship lies in the reaction of molecular or atomic beams impinging a heated crystalline substrate under **Ultra-high vacuum (UHV)** conditions as schematized in Figure 2.1. This pure environment is mandatory to guarantee very low contamination and suppression of particles collision during their travel from the sources to the sample surface.

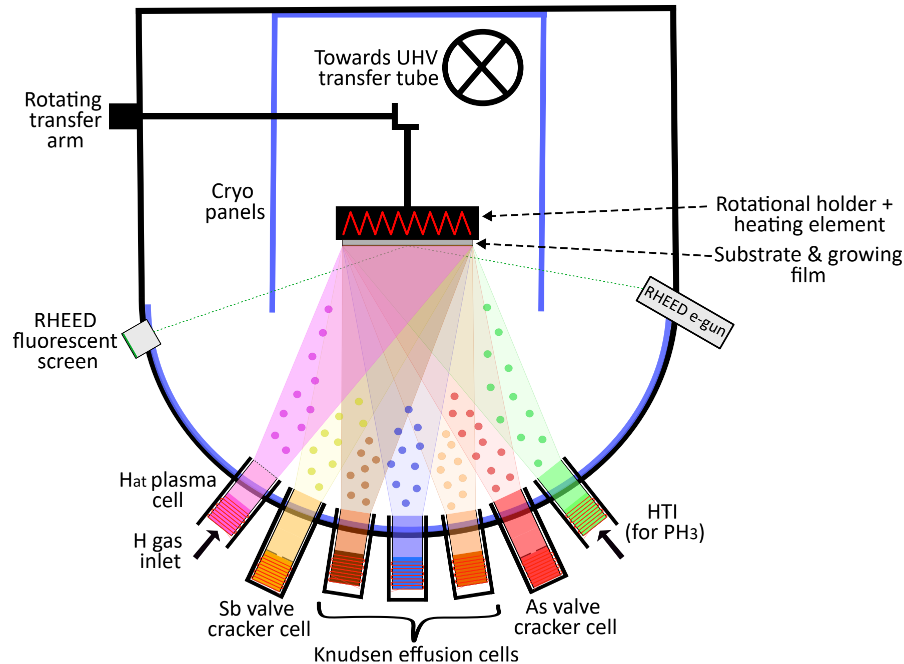


Figure 2.1: Scheme of a **MBE** reactor, with a design adjusted to the model used in this work, having different types of cells.

In addition to the relatively low growth temperatures employed in **MBE**, the low growth rate (as low as 0.01 ML/s) contributes also to the unique precision of this technique. Altogether, it ensures that the epitaxial film can exhibit a remarkable control over composition, uniformity, doping and atomically sharp crystalline interfaces. Undoubtedly, with the growing interest and development of this technique over the years, **MBE** played a key role in fabricating the emerging quantum nanostructures such as **QW**s, superlattices, **2DEG** or periodic heterostructures that are now very demanding with regards to bandgap engineering and electronic properties.

2.2.2 Riber C21 reactor

The **MBE** reactor used for all growths in this work is part of a larger system, gathering another reactor dedicated to Van der Waals epitaxy for **Two-dimensional Transition Metal Dichalcogenide (TMDC)** materials (WSe_2, $HfSe_2$, $TaSe_2$, etc...) followed by a **XPS** chamber as a chemical surface analysis tool. The different chambers are connected through an **UHV** tube placed perpendicularly all along and divided in several sections that are isolated via gate valves. The samples are carried from one end to the other using a cart of eight slots.

Prior entering the **MBE** chamber (Riber C21-TM), the sample undergoes a 12 h bake out at 100 °C followed by a 90 min outgassing at 200 °C for GaAs and 150 °C for CdTe wafer pieces to ensure proper **UHV** transfer. GaAs 2-inch wafers are manufactured by Axiotron (AxT) ($-0.5° \leq$ (111) misorientation $\leq 0.5°$) and Wafer Technology (WT) ($-0.1° \leq$ (111) misorientation $\leq 0.1°$). CdTe (001) and $Cd_{0.97}Zn_{0.03}Te$ (111) 40 x 40 mm square-wafers were provided by the **CEA LETI**. In the following of this work, despite $Cd_{0.97}Zn_{0.03}Te$ (111) has a small Zn content, we will report to it for simplicity as "CdTe (111)". For most epitaxial growths, 1/6 of 2-inch GaAs wafers or small CdTe pieces are cleaved and glued with indium onto a 2-inch Si unpolished carrier wafer. Then, the Si-carrier is mounted onto a molybdenum (Mo) plate. When growing on 2-inch wafers,

direct mounting can be done on the Mo plate. Inside the **MBE** chamber, the base pressure is kept as low as 1×10^{-10} Torr thanks to a combination of an ionic pump and a cryogenic pump as well as liquid nitrogen cooled (77 K) panels. As presented in Figure 2.2, the C21 reactor, dedicated to III-V semiconductor growth is equipped with various types of cells.

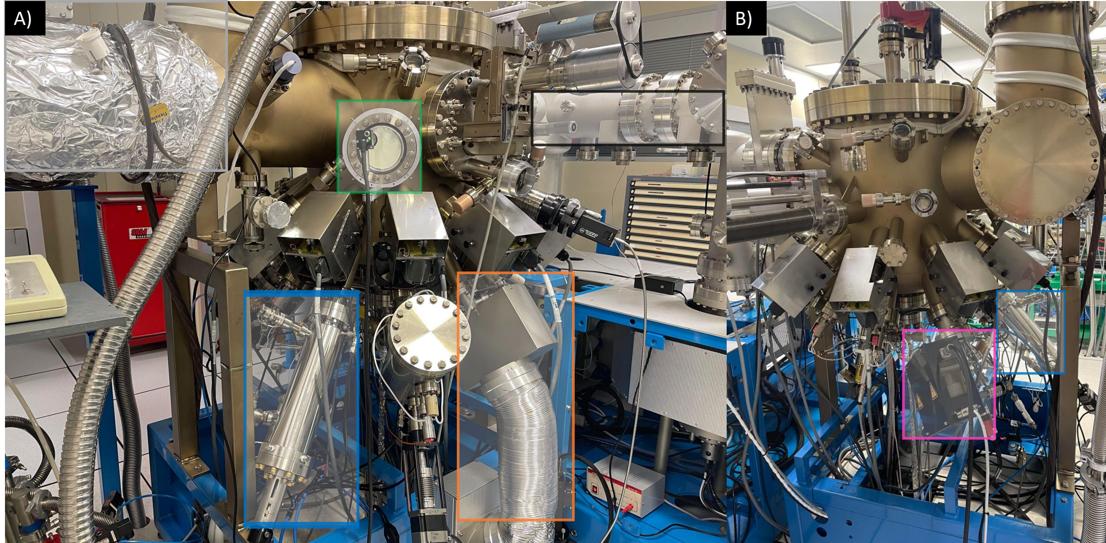


Figure 2.2: A) Frontside and B) Backside of the C21 reactor. Color boxes highlight specific components of the machine: The ion pumping unit (grey box), the RHEED fluorescent screen (green box), the high temperature injector for AsH_3 or PH_3 (orange box), the connection to the main UHV tube (black box), the RF $\mathbf{H_{AT}}$ plasma cell (pink box) and the Sb cracker (blue box).

Conventional Knudsen effusion cells are used for group III-elements (Ga, In, Al) while valve cracker cells evaporate group V-elements (As_4 and Sb_2).[148] Moreover, a **High Temperature Gas Injector (HTI)** can provide AsH_3 or PH_3 cracking. Doping elements can be found in an effusion cell (Si, Be, Te) or incorporated from a CBr_4 line if carbon doping is desired. Eventually, a hydrogen plasma cell is also mounted to be able to perform substrate deoxidation and enhance the growth selectivity during **SAG**.[149,150] The plasma cell is based on a 600 W RF excitation coil at 13.56 MHz that allows to dissociate molecular hydrogen (nominal flow rate of 3 **standard cubic centimetres per minute (sccm)**) to atomic reactive species with the generated discharge. A H_2/Ar (2 %) mix is used to ensure the ignition and stability of the $\mathbf{H_{AT}}$ plasma.

MBE is based on the three temperatures principle which states that the substrate temperature must be found between the evaporation temperature of group III and group V-element. Respecting this condition $T_{III} > T_S > T_V$ through a fine tuning of each elemental flux ensures the growth of stoichiometric III-V thin layers.[88,151,152] In this view, the group III deposition rate will dictate overall growth rate. The condensed atoms on the surface are waiting for group V atoms that can only incorporate in their presence to build the complete monolayer. This explains why the V/III ratio is often larger than unity allowing an excess of group V-element.

The control of fluxes is obtained via a careful calibration of the temperature of each effusion cells. While standard effusion cells are used for group III-element evaporation, valve crackers are used for As and Sb evaporation. These latter enable low residual partial pressures of As and Sb in the chamber while allowing a quick control of As and Sb flux during the growth by adjusting the valve position. Typical cracking temperatures are 900 °C for the Sb cell to ensure the dissociation of Sb_4 molecules into Sb_2 and Sb species and 600 °C for the As cell (in this case

As_4 molecules are evaporated). Phosphine (PH_3) is cracked at 850 °C via the **HTI** to obtain a P_2 flux. To ensure uniform growth conditions over the sample surface, the substrate holder in the central area of the chamber is rotating during epitaxy. The beam fluxes directed towards the substrate surface are coming from the tilted evaporation cells.

Growth temperature can be monitored via three possible ways: first, a thermocouple located at the backside of the sample holder; then, a pyrometer measuring the black-body radiation of the substrate surface; eventually, with a BandIT system measuring the absorption spectrum for 2-inch substrates. As the former solution depends of the type, thickness and back-side roughness of the substrate, the pyrometer temperature is considered closer to the real temperature of the surface. This temperature is defined as the growth temperature in the following. The pyrometer is calibrated by observing the melting of a small piece of InSb substrate at 525 °C. In this work, the BandIT was solely used for growth on 2-inch wafers as the III-V substrates are transparent at the pyrometer wavelength. Indeed, when samples are glued on Si carrier with indium, the pyrometer probes in reality the direct radiation coming from the In surface used to glue the sample. Because the BandiT requires a good knowledge of the absorption spectra of the substrate,[153] its use was restricted to growth on 2-inch substrates only.

2.2.3 Reflection High-Energy Electron Diffraction

As in most of the **MBE** systems, the C21 reactor is equipped with a **Reflective High Energy Electron Diffraction (RHEED)** unit, which enables a real-time in situ epitaxial growth control on a fluorescent screen (green box in Figure 2.2). **RHEED** is a powerful characterization technique to obtain real-time information about the morphology, crystal quality and surface reconstruction of the growing layer. An electron beam is generated with an electron gun, focused onto the sample surface with a grazing incidence small angle θ. The beam is diffracted by the crystal lattice creating a diffraction pattern instantaneously imaged on a fluorescent screen. The **RHEED** pattern corresponds to the intersection of the Ewald's sphere and the surface of the reciprocal lattice (Figure 2.3a).

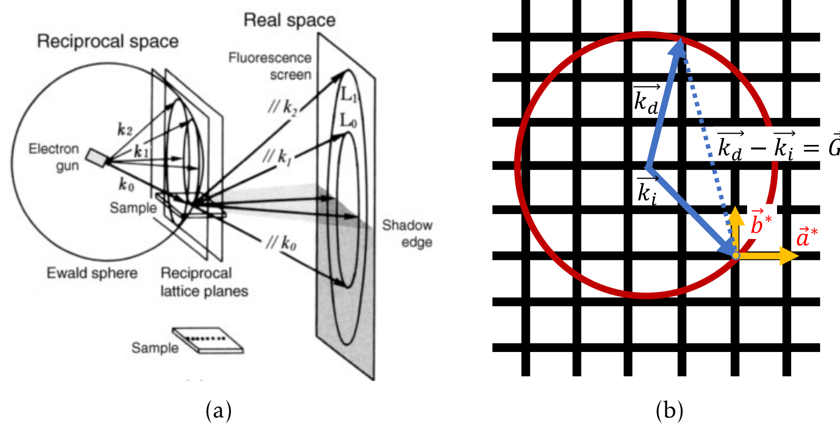


Figure 2.3: (a) Scheme of the RHEED unit and working principle extracted from[154]. (b) Schematic of Ewald's sphere with constructive interference condition.

The wavevectors k_i and k_d of the incident and diffracted beams will have the same magnitude with $|\vec{k_i}| = |\vec{k_d}| = 2\pi/\lambda$, where λ is the De Broglie wavelength directly evaluated from the **RHEED** e-gun accelerating voltage. The Ewald's sphere is then obtained by drawing the vectors from the same origin than $\vec{k_i}$, with a radius of its magnitude.[154] The diffracted spots that intersect

the perimeter of Ewald's sphere will then be part of the **RHEED** surface reconstruction pattern when the condition $|\vec{k_i} - \vec{k_d}| = |\Delta\vec{k}| = |\vec{G}|$ is satisfied, where $\vec{G} = h\vec{a^*} + k\vec{b^*} + l\vec{c^*}$ is a reciprocal lattice vector[155] (Figure 2.3b). Therefore, it is possible to follow during the whole growth process a large quantity of information. The deoxidization state, the strain induced from lattice mismatch, the size of the grains, the surface roughness, the growth regime transition and the atomic arrangement on the surface can all be extracted from **RHEED**.

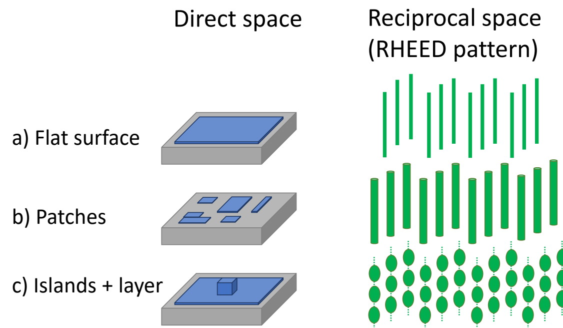


Figure 2.4: Examples of different **RHEED** patterns according to the growing morphologies.

As depicted in Figure 2.4, any change in the **RHEED** streak will reflect a change in epitaxial growth. Wider streaks depict the presence of several domains on the growing surface, while modulation along their vertical length witnesses of a stepped surface. Last but no least, the appearance of spots on the **RHEED** generally reflects a relaxation of stresses, which can be elastic (via surface deformation) or plastic. As a side remark, circular rings visible on the **RHEED** demonstrates a lack of selectivity for **SAG** samples due to parasitic nucleation on the oxide mask.

To conclude this section, the **RHEED** contributes to a well-calibrated epitaxial growth via the flux calibration of each element using the **RHEED** intensity oscillation method. To do so, the specular spot intensity is monitored along a layer-by-layer growth performed in specifically known conditions. During the growth of a monolayer, the surface state will change from stepped to smooth leading to an intensity variation on the specular spot along the full monolayer completion growth process (see Figure 2.5). From the total number of oscillations, the number of grown monolayers is deduced then allowing the extraction of the elemental flux in monolayer per second (**ML**/s).

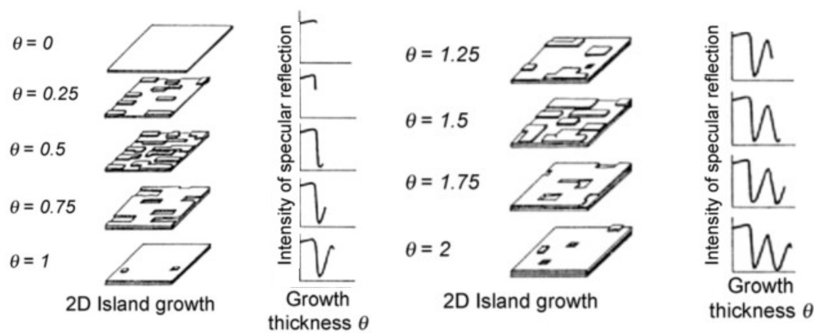


Figure 2.5: Schematic representation of 2D-island growth with the associated **RHEED** specular spot intensity oscillated. Adapted from[154].

However, this growth rate is specific to the surface orientation because of the density of atoms per monolayer being dependent of the crystal direction for cubic materials. As an example, we

take a similar growth rate of 0.5 nm/s for InSb grown on a (001) and (111) substrate. Hence, the growth rate will be 0.77 **ML**/s for (001) (as $d_{001} = a/\sqrt{1} = a$) and 1.33 **ML**/s on (111) (from $d_{111} = a/\sqrt{1^2 + 1^2 + 1^2} = a/\sqrt{3}$). In this work, the indium flux is calibrated with the measurement of the growth rate of InAs on an InAs (001) substrate under As-rich conditions to guarantee a **FM** layer-by-layer growth regime. For As flux calibration, the growth rate is set by In temperature, and As flux is progressively reduced down to the critical flux for which the growth rate starts to decrease. A similar method is used for calibrating Sb flux through GaSb homoepitaxy.

2.2.4 Mask preparation process

In this section, the fabrication of the dielectric mask required for **SAG** is detailed step by step. For this work, two types of wafers are used: 40 x 40 mm square-shaped CdTe (001) and (111) wafers and 2-inch GaAs $(111)_B$ wafers (n-type ≈ 3×10^{18} cm^{-3}, p-type ≈ 1×10^{19} cm^{-3}). GaAs substrates are either bare or covered with a III-V semiconducting barrier (AlGaAs or GaInP) epitaxially grown on top. Two types of masking processes were developed. The original mask, labeled A was established some time ago during Maria Fahed's PhD work as part of EPIPHY group.[140] Then, another type of process (mask B) has been developed more recently during Claire Rondeau-Body's master-degree project.[156] As shown in Figure 2.6, mask A is based on a single SiO_2 dielectric layer, while the second mask B introduced a thin Al_2O_3 layer below the SiO_2 layer. Thanks to the double-dielectric layer (Al_2O_3/SiO_2) design, narrower and sharper aperture trenches can be achieved.

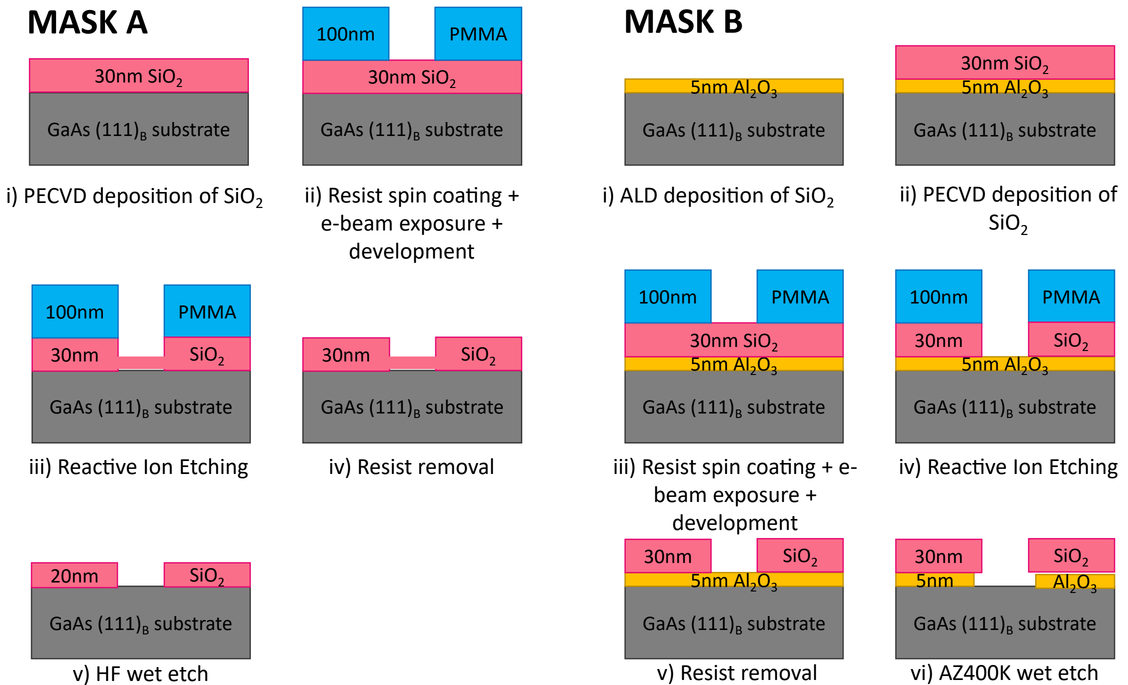


Figure 2.6: All masking process steps for the design of both masks.

2.2.4.1 Dielectric deposition and Spin coating

For mask A, a 30 nm SiO_2 layer is firstly deposited by **Plasma-enhanced Chemical Vapor Deposition (PECVD)** at 300 °C for GaAs substrates in an Oxford Plasma Lab80 Plus machine

(5% SiH_4/N_2 150 sccm, N_2O 700 sccm, P = 1000 mT, RF power = 20 W, t = 27 s). In the case of CdTe substrates, SiO_2 was deposited at 250 °C with the same other parameters.

Spin coating is performed in the second step (after the oxide) with a 100 nm PMMA 3 % 495 K photoresist. First, an adherence enhancing layer (HMDS) is coated on the substrate prior to the photoresist. Once PMMA is coated on the sample, it is annealed at 180 °C for 10 min to evaporate the solvent before geometric patterns are defined in the photoresist by e-beam lithography. The different mask layouts were designed using the Layout Editor Software.

Regarding the mask B process, the first step consists in the deposition of the 5 nm Al_2O_3 layer by **ALD** at 200 °C. The recipe is based on the repetition of the **ALD** cycle 45 times. A cycle is structured in 4 steps: the substrate is respectively exposed to 0.1 s of TMA (Trimethylaluminum $Al(CH_3)_3$), F = 150 sccm, 4 s of N_2 purge, 0.1 s of H_2O (F = 200 sccm) and 6 s of N_2 purge. After the 5 nm Al_2O_3 layer, the 30 nm SiO_2 layer deposition and resist spin coating are performed the same way as for mask A before the sample undergoes irradiation from e-beam lithography.

2.2.4.2 Die layout

Six different types of mask layout were used in this work with each having specific patterns to match with the characterization technique employed for post-growth analysis. The cell size is a square of 3.2 mm x 3.2 mm. Cells are spaced by 200 µm before repeating the die. The mask layout classification can be found in appendix A following with their respective patterns. In the following chapters, the mask labels as referred in appendix A will be used to identify the specific layout patterned on the sample for both the growth and subsequent characterization. For all masks, the nanostructures crystal orientation is known thanks to proper mask alignment with wafer flats (e.g an “IEMN” structure oriented parallel to the wafer flat). All other orientations can then be deduced at any time.

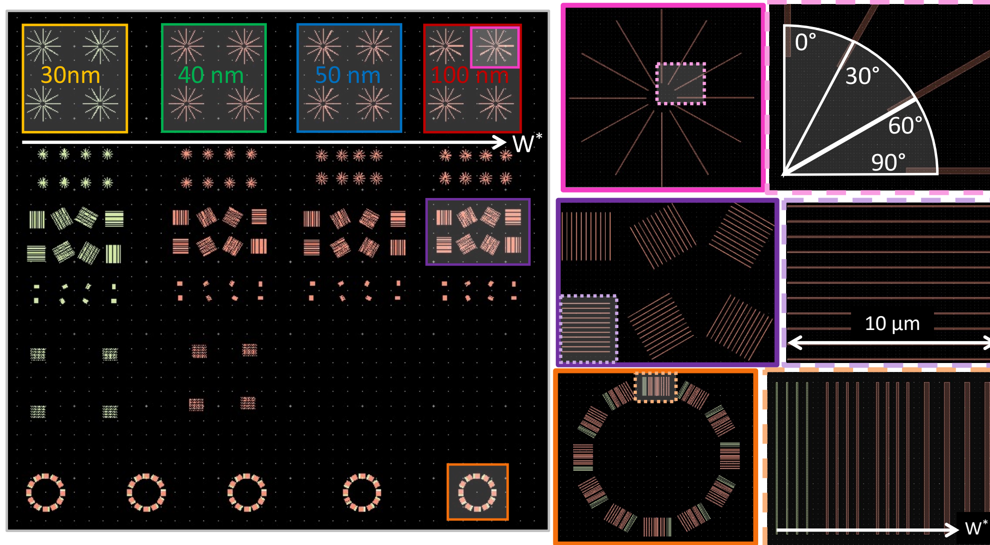


Figure 2.7: Example of mask “3” used for **Four Point Probe (4PP)** experiments. Structures with different aperture widths w, varying from 30 nm to 100 nm are repeated. Insets: Zooms on the different nanostructure shapes.

To illustrate the different interesting geometric shapes in this work, Figure 2.7 presents as an example the nano-patterns on the mask “3” used for **4PP** transport measurements. Among the patterns, a “sun-shape” structure is designed as shown in the pink box. Here, 10 µm long

apertures are patterned and repeated clockwise every 30° (see the zoom-in on the pink box). This "sun-shape" is duplicated 4 times to form a sub-group. From Figure 2.7, sub-groups of increasing aperture width can be seen along with the white arrow such as 30 nm in the yellow box, 40 nm in the green box, 50 nm in the blue box and 100 nm in the red box.

The second type of "sun-shape" structure is highlighted in the orange box. The angular variation is the same (every 30°) but the various aperture widths are organized inside arrays. Within an array, the same logic is followed. This time being stacked by sets of four, the apertures will increase in width from the left to the right (zoom-in on the orange box): 30, 40, 50 and 100 nm-wide aperture. The purple box shows a set of 11 apertures from 0 to 90 ° every 30 ° especially created to perform **4PP** measurements on **NWs**, directly correlated with growth orientation. All of these structures are of high importance to evidence crystallographic orientation growth dependency as well as aperture width effect.

2.2.4.3 E-beam lithography and development

For e-beam exposure, the dose needs to be optimized for every aperture width to be sharp and undergo smooth development avoiding resist residues. For this work, on mask A process ("single dielectric mask"), a dose of 420 C/cm^2 is used. For mask B process (Figure 2.7), all structures $\geq$ 30 nm are obtained with the same dose. For the mask layout "3, 4 and 5", the narrowest structures (light yellow) width is decreased to 20 nm and a dose of 680 C/cm^2 is used to overexpose them and reach $\sim$35 nm of width after development.

After exposure, the sample is developed in a **Methyl Isobutyl Ketone (MIBK)-Isopropanol (IPA)** solution (1:2 dilution rate) for 1 min, then put into an **IPA** ultrasonic bath for 30 s and dried with nitrogen pistol. After development, openings down to the SiO_2 layer are achieved in the 100 nm thick resist film.

2.2.4.4 Apertures opening via Reactive Ion Etching

As shown in Figure 2.6 **Reactive Ion Etching (RIE)** is performed following the development of the resist after e-beam lithography to open the trenches down to few nms of SiO_2 (for mask A process) or to land onto the Al_2O_3 etch stopping layer (for mask B process). The etch is done inside an OXFORD Plasmalab 80 tool chamber. A first 6 s O_2 plasma (20 sccm, RF power 50 W, pressure 50 mT) is used to clean the potential resist residues from the development inside the resist aperture trenches. Next, the reactive plasma step takes place to etch the oxide layer, using a CF_4 (20 **sccm**)/CHF_3 (20 **sccm**)/Ar (10**sccm**) plasma for 60 s (RF power 100 W, pressure 50 mT) in the case of mask A process. For mask B process, a reactive plasma of CF_4 (40 sccm)/CHF_3 (40 sccm) for 60 s (RF power 180 W, pressure 50 mT) is used.

Thereafter, for both masks (A and B) the resist layer removal step is conducted by putting the sample into a SVC-14 remover bath, on a heating plate at 70°C for 1h at least, followed by subsequent acetone rinse (15 s) and ultrasonic bath for 2 min before finishing with a last **IPA** bath for 2 min. The sample is then going back into **RIE** for a final mask surface cleaning using the same oxygen plasma recipe for 30 s this time (O_2 plasma, 20 **sccm**, RF power 50 W, pressure 50 mT). At this stage, the apertures are defined and the sample is almost ready to be introduced into the **MBE** chamber. A last wet etch step is needed to fully open the trench and control apertures.

2.2.5 Mask apertures control: role of dielectric layer design

With the original SiO_2 mask design, an HF 1% bath is used to dip the patterned sample and fully etch the remaining thin layer inside the aperture (~35 s). However, as HF treatment acts as an isotropic etching agent upon SiO_2, the overall oxide surface is also etched with the same etch rate, leading to a decrease in the trench depth and an enlargement of the aperture width. For a 30 nm film, at the end of this process, the remaining SiO_2 thickness is between 10 and 20 nm. This is still convenient to grow InSb **NW** with relatively good containment in the lateral direction until the mask surface is reached. However, because of the isotropic etch that enlarged the aperture width, the narrowest achievable value is around 65 nm instead of 40 nm-wide nominal aperture planned on the mask layout.

As a matter of fact, the aim for getting a sharper border near the aperture, as well as vertical deeper trenches motivated the development of this new mask design B. The introduced 5 nm-thick Al_2O_3 layer beneath the 30 nm-thick SiO_2 layer helped in meeting these requirements. Because of the gas species used during the **RIE** step, the etch is selective to land on the Al_2O_3 surface (the etch rate of this material is very low compared to the recipe time making it indirectly "selective"). Then, the subsequent wet etch treatment was also adapted to be HF-free by switching to an AZ400K resist stripper bath for 15 s. The double dielectric layer enables for a vertical deeper, sharper and narrower trench controlled down to around 35 nm (for the overexposed 20 nm nominal aperture width) as shown in Figure 2.8a. This significant reduction in the width of the nanostructures gives the opportunity of growing and probing potentially narrower **NWs**.

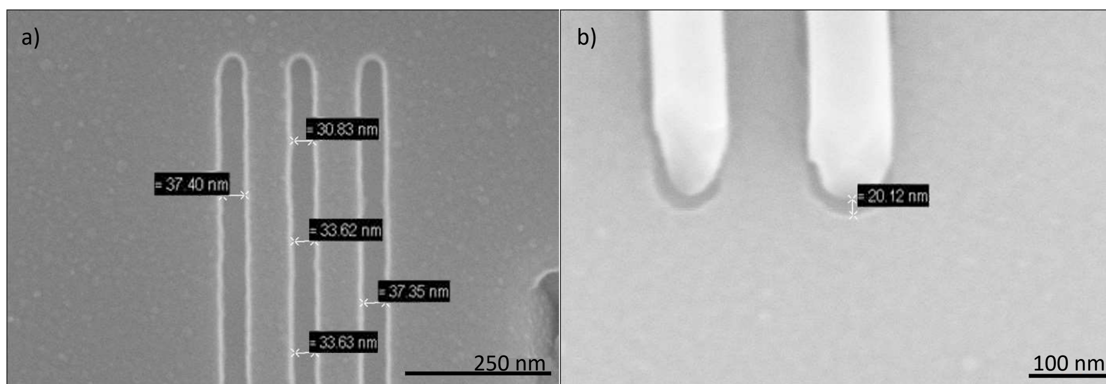


Figure 2.8: a) **SEM** image of the overexposed 20 nm-wide **NWs** patterns after the new masking process. b) **SEM** image of an InAs **SAG** on GaSb/GaAs substrate with SiO_2 layer wet-etched to show the AZ400K under-etching of the Al_2O_3 layer. Extracted from[156].

Although this new mask design B improved the control of the nanostructure sizes, two drawbacks were also evidenced in a later time. Because the AZ400K stripper does not react with SiO_2, the etching of the Al_2O_3 layer causes a lateral "under-etching" as seen on Figure 2.8b and also visible after growth through **STEM** cross-section profiles. The second drawback observed is an important decrease of the selectivity rate during **SAG** (increase in parasitic nucleation on mask) in spite of the $\mathbf{H_{AT}}$ plasma used. This inconvenience, potentially affecting the growth regime was assigned to the mask roughness. Indeed, later tests revealed later that the HF treatment for mask A process is acting as a smoothing agent on the oxide surface preventing important parasitic nucleation.

To prove such point, a 50 nm-thick SiO_2 layer was grown at 300 °C on an InP (100) substrate using the regular **PECVD** recipe for mask A and B process. A piece of the wafer was then

wet-etched in an HF 1% solution for 30s leaving 22 nm of SiO_2 remaining (confirmed through ellipsometry measurement). As shown in Figure 2.9a the HF-etched surface **Root-Mean Square (RMS)** roughness is sub-nm (0.98 nm) while the bare SiO_2 surface in Figure 2.9b, the as-deposited 50 nm-thick SiO_2 layer is rougher (2.33 nm **RMS** roughness).

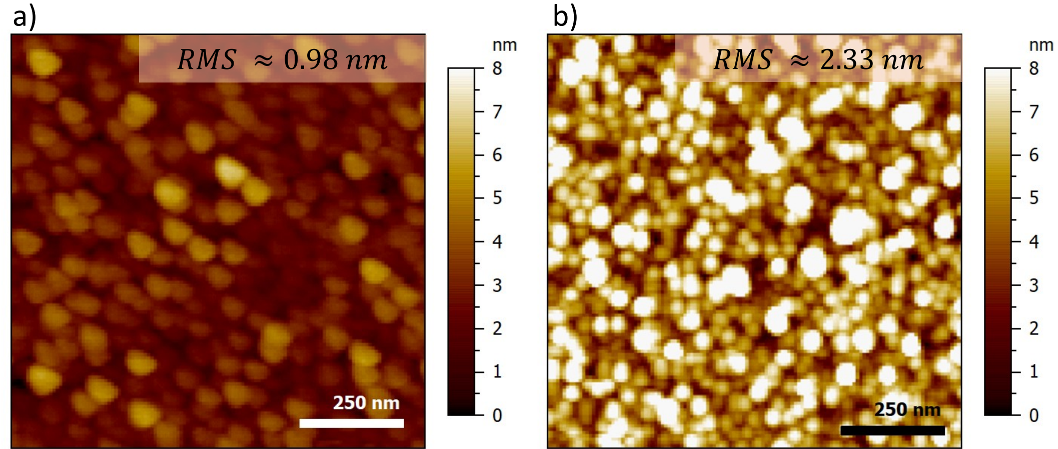


Figure 2.9: 50 nm-thick SiO_2 layer deposited onto an InP (100) substrate for HF 1% wet-etch experiment. In a), the surface is dipped in HF 1% for 30s, etching SiO_2 down to 22 nm-thick, as measured by ellipsometry. In b), the surface of the as-deposited SiO_2 layer with no HF treatment is rougher.

To fix this issue, the SiO_2 **PECVD** thickness was increased to 50 nm and followed by a rapid HF 1 % wet etch to reach a 30 nm thickness value (checked by ellipsometry) before the resist spin coating step. Because this impact was noticed late in the work, all presented samples were fabricated without using the modified **PECVD** SiO_2 thickness.

2.2.6 Selective Area Growth

After all masking process steps, the sample is introduced under vaccuum for the subsequent **SAG** in the **MBE** reactor. Outgassing at 200 °C for GaAs and 150 °C for CdTe substrates for 1 h 30 is done prior to the introduction of the sample inside the growth chamber. As the **SAG** samples are covered by the dielectric amorphous mask on most of the surface, no in-situ **RHEED** monitoring can be done this way. As a matter of fact, the deoxidation process is tracked using a bare GaAs or CdTe substrate (without any mask) that is also glued in the central area of the Si carrier to monitor the **RHEED** during the growth as seen in Figure 2.10.

In the case of InSb **SAG** on GaInP/GaAs $(111)_B$ substrate, a bare GaAs substrate is mostly used because it offers a time and cost effective solution. Growing a GaInP 2D layer on GaAs substrate takes a certain time and cost from the materials and machine usage. For **SAG** samples, the same deoxidation recipe developed for the 2D InSb growth is run in this case, ensuring that the mask apertures will be properly cleaned. All deoxidation process parameters will be further detailed in the next chapters.

To achieve the highest selectivity as possible, an accurate control of the growth conditions is needed. As specified in the section 1.4.4.1 of chapter 1, the suitable selectivity window for each combination (InSb/CdTe, InSb/GaAs, InSb/SC barrier) must be found. The $\mathbf{H_{AT}}$ plasma is added during the whole time of **SAG** to widen the selectivity window.[138,150]

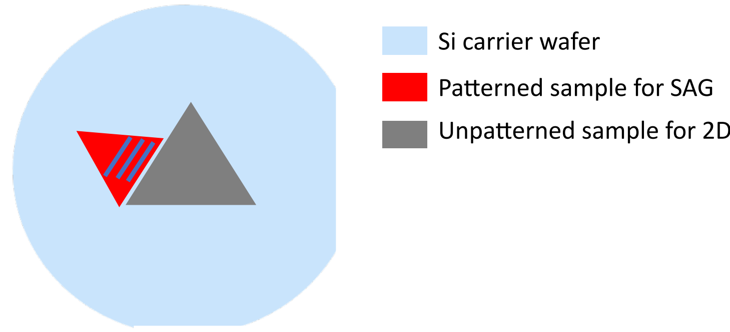


Figure 2.10: Schematic of the sample arrangement for the **SAG** experiment. An unpatterned substrate in the center corresponds to the 2D sample that allows to track the **RHEED** during **SAG**. Conversely, the patterned sample for InSb nanostructures growth (shown by the blue bars) is glued next to the center.

2.3 Scanning Tunneling Microscopy

2.3.1 Introduction

Invented in 1981 at IBM Zürich by Binnig G. and Rohrer H. this surface analysis technique revolutionized our vision of the matter at the nanoscale and contributed to the advent of the nanotechnology era.[157,158] **STM** not only pushed topographic images of surfaces down to individual atoms and molecules, but it gave the possibility to trigger reactions and probe electronic events from conductive samples.

To do so, the **STS** mode can be used to investigate the electronic states of sample surfaces. Taking advantage of the wave-particule duality described by De Broglie. L, **STM** does not obey anymore to classical but quantum mechanics law with the tunneling effect as the core principle behind. Given the major milestone achieved by the creation of such a technique, their invention was rewarded by a Nobel-Prize shortly after, in 1986.

2.3.2 Electron tunneling effect

In classical mechanics, when an electron is facing a thin potential barrier separating two electrodes with an energy lower than the barrier height, the electron cannot travel across the barrier. Now, assuming the wave-particle duality of electron, based on quantum mechanics, this crossing probability is not anymore equal to zero. This involves that when a voltage is applied between the two electrodes, the resulting tunneling current will exist and varies exponentially with the electrodes separation d. The wave function of the electron, described in each region by the quantum mechanics, accurately demonstrates this phenomenon.

The scenario depicted in Figure 2.11 represents how tunneling current occurs. An electron of energy E moving in a potential $U(z)$ encounters a barrier in the central region (II) where $U(z) = U_0$. For this example, we set $U(z) = 0$ (regions I and III). Because the electron follows quantum mechanics, its energy satisfies the (one-dimension in this case) Schrödinger equation[159,160]

$$-\frac{\hbar^2}{2m}\frac{\partial^2}{\partial z^2}\psi(z) + U(z)\psi(z) = E\psi(z) \tag{2.1}$$

where $\hbar$ is the reduced Planck constant and m is the electron mass.

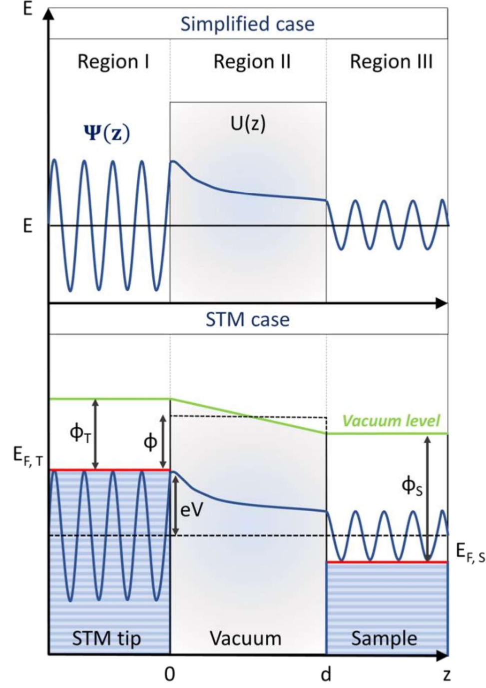


Figure 2.11: Schematic diagram of the tunneling effect using the simplified one-dimensional barrier example. Bottom part shows the same scenario applied to the **STM** working principle. Here, the barrier height on each region is defined by their work function (relative to the vacuum level) Φ. Extracted from[161].

Because at the side regions (I and III), $U = 0$, the solutions for these regions are

$$\psi_I(z) = Ae^{ik_1 z} + Be^{-ik_1 z} \tag{2.2}$$

$$\psi_{III}(z) = Fe^{ik_1 z} \tag{2.3}$$

where $k_1 = \sqrt{2mE}/\hbar$ and A, B, F are coefficients. In region I, as the electron can also be reflected, and thus move in the opposite direction, a second term exists. For region III, following the same logic, the election is only transmitted without any reflection, yielding a single 'z-positive' direction term. In the central region II where the potential is non-zero and equal to U_0, the solution corresponds to the sum of evanescent waves

$$\psi_{II}(z) = Ce^{ik_2 z} + De^{-ik_2 z} \tag{2.4}$$

with this time $k_2 = \sqrt{2m(U_0 - E)}/\hbar$, C and D are coefficients. The transmission coefficient is expressed by the ratio of the transmitted to the incident flux, which after solving the systems of Equations 2.2, 2.3 and 2.4 gives

$$T = \frac{|F|^2}{|A|^2} \tag{2.5}$$

$$T = \frac{1}{1 + \frac{U_0^2 \sinh^2(k_2 d)}{4E(U_0 - E)}} \tag{2.6}$$

It is often assumed that $k_2 d > 1$ simplifying the transmission rate to

$$T \approx \frac{16E(U_0 - E)}{U_0^2} e^{-2k_2 d} \tag{2.7}$$

From Equation 2.7, the electron transmission across the potential barrier depends exponentially on the distance d, the electrodes separation. In the **STM** system, the first electrode is a sharp metallic tip, made up from tungsten W in this work, and the other one is the semi-conductive sample to be studied. The potential barrier is represented by the vacuum barrier between the two parts. Under **UHV**, this is simply the tip apex to sample surface separation. Figure 2.12 showcases this tunneling effect translated to the **STM** system, depending on the applied bias voltage between the sample and the tip.

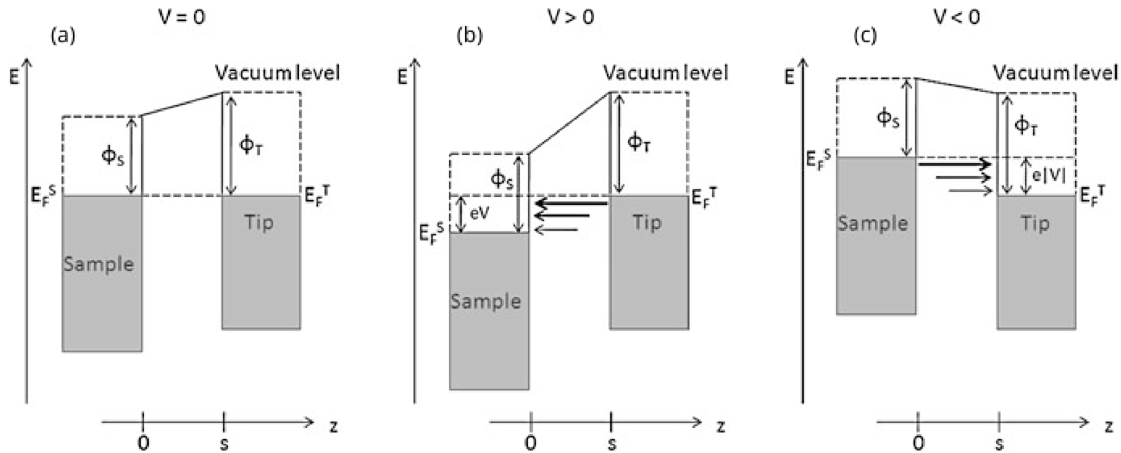


Figure 2.12: a) Tip-sample equilibrium conditions with no applied bias. Fermi levels are aligned. A potential barrier is created with regards to the work function of each materials. b) With a positive bias applied on the sample, electrons tunnel from the tip to the sample as $E_{F,S}$ is lowered by $-eV$ from $E_{F,T}$. c) At negative sample bias, the electrons tunnel from the sample to the tip. Thicker and longer arrows indicate an exponentially increasing tunneling probability for electrons to tunnel through the barrier. Extracted from[162].

The barrier height Φ is defined by the average of the tip and sample work function, thus directly linked to the vacuum and the Fermi level of tip $E_{F,T}$ and sample $E_{F,S}$.

In Figure 2.12a when no bias is applied, electrons are allowed to tunnel either from the sample to the tip or vice-versa, but overall, no tunneling current flows. Now, by applying a bias on the sample with respect to the grounded tip, two situations can be distinguished. In the case of Figure 2.12b, when $V > 0$ $E_{F,S}$ is shifted down by $-eV$ (with V the actual applied voltage), electrons tunnel from the tip occupied states to the sample unoccupied states. Comparatively, when $V < 0$, electron tunneling occurs from the sample to the tip (Figure 2.12c).

In order to raster scan the tip on the sample surface and get a stable tunneling current, a sample-tip distance in the range of a nanometer is needed. The measurement can be performed either in what is called the "fixed height (z)" mode or the "constant current (I)" mode. The former makes no use of the feedback loop on the z piezo to keep a fixed sample-tip distance d and measures the current variations regarding the bias as illustrated in Fig. 2.13. This mode allows to collect information on the **DOS**, but cannot be used over large areas without degrading

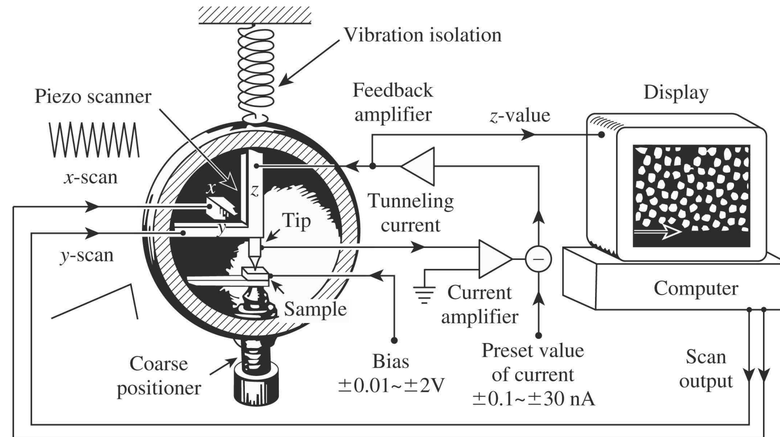


Figure 2.13: **STM** apparatus scheme. A tunneling current is obtained by applying a bias between the sample and the tip. The piezoelectric motors control the movement of the tip in all directions. A feedback system allows to enter either constant current (I) or height (z) mode if activated or not. The entire system is isolated against vibration to guarantee stable conditions.Extracted from[163].

the **STM** tip. For the second mode, the feedback loop on the z piezo is used to constantly adjust the tip-sample distance and keep the tunneling current constant, usually between 10 to 50 pA. Consequently, the topography of the sample can be accurately reproduced by the tip scanning, making it the standard imaging mode.

2.3.3 Scanning Tunneling Spectroscopy (STS)

As a complementary technique to the atomic scale imaging offered by **STM**, the spectroscopic mode further extends the tool capabilities by investigating the sample electronic structure. **STS** provides direct information about the sample **Local Density of States (LDOS)** as well as the band gap energy for semiconducting samples. Starting from the Tersoff and Hamann model, which considers a spherical tip apex with a s-type wave function, a simplified version of tunneling current can be expressed as[164]

$$I \propto \int_0^{eV} \rho_S(E)\rho_T(E-eV)T(E,eV)dE \tag{2.8}$$

with ρ_S and ρ_T being the **DOS** of the sample and tip respectively. Because the tip is metallic (W), its **DOS** is assumed constant around the Fermi level. Therefore, it can eliminate its energy dependency from the integral, turning Equation 2.8 into[165]

$$I \propto \int_0^{eV} \rho_S(E)T(E,eV)dE \tag{2.9}$$

The resulting current equation shows now that it represents the integral over the sample **DOS** up to the energy eV. Using the Figure 2.14a, the interest of **STS** is clearly evidenced. If we take now the derivative of the current (Equation 2.9), the differential conductance will give $dI/dV \propto \rho_S(E_F - eV)$ for small bias ranges. In other words, the **DOS** of the sample at energy eV will be directly evaluated.

In this example structure, an InGaAs **NW** chain that consists in alternating **QDs** and bridges **(BRs)** was studied as part of the training session on the **LT-STM** (Figures 2.14b and c). With the collection of dI/dV spectrum, it gives access to the local electronic states. The different energy levels can be clearly resolved in the form of these discrete quantized peaks as E_{eQD1}, E_{eQD2} or E_{eBR1}. On the BR1 curve, the second and third lower energy levels can even be evidenced for higher values of the sample voltage.

In the case of a larger bias range, the transmission probability must be taken into account. However, to cancel out its effect, the actual **normalized differential**, *i.e.* $(dI/dV)/(I/V)$, can be considered to determine the **LDOS** in the sample area below the tip. In practice, to achieve such extensive information, the **STM** is used in constant height (z) mode, without raster scanning the surface. The tip is kept immobile above the area of interest to perform the spectroscopic measurement. The bias voltage is swept, while the resulting tunneling current is measured. Typically, the setpoint (tunneling) current is also increased to several hundreds of pA up to a nA for closer interactions with the surface.

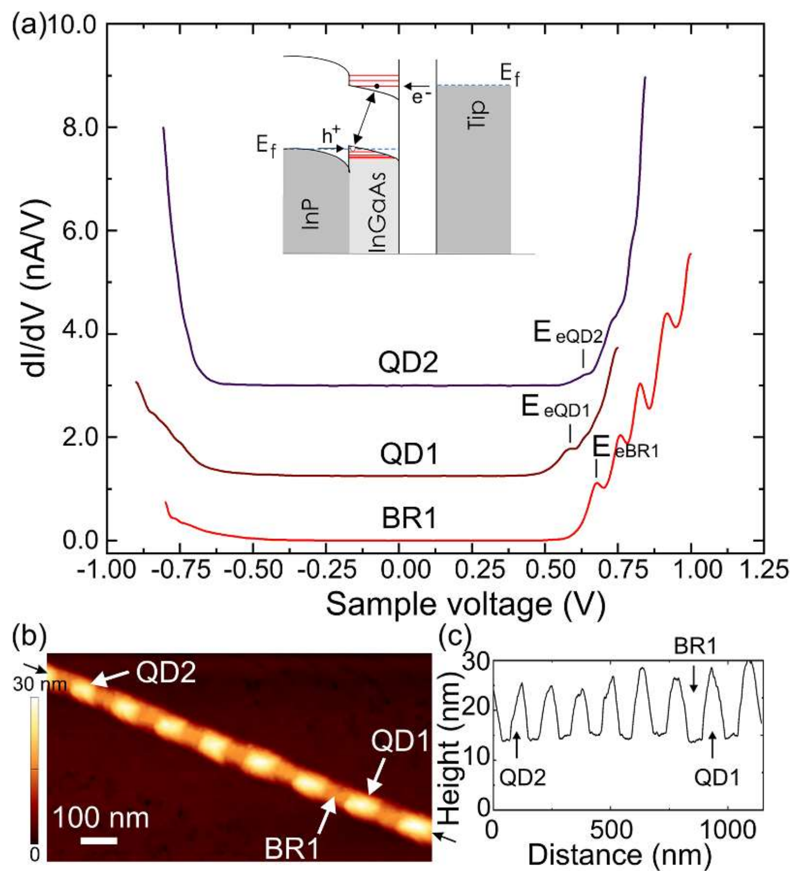


Figure 2.14: **STS** spectra example of an InGaAs **NW** chain with thickness modulation along its length forming **QDs** on InP (100) substrate. (a) Three dI/dV spectra measured on two **QDs** (QD1, QD2) or bridge (BR1) showing several quantized states in the conduction band. E_e stands for the lowest energy conduction band states. Inset: Band diagram of the junction. At positive bias an electron is injected from the tip at Fermi level into InGaAs and recombines immediately with a hole from InP valence band. (b) Topographic **STM** image (c) **STM** height profile acquired along the chain of **QDs**. Online publication available[166].

2.3.4 Omicron Low-Temperature STM

As part of this work, the **LT-STM** from the physics group of **IEMN** located at the **Institut Supérieur d'Electronique et du Numérique (ISEN-JUNIA)** was used for all the **STM** and **STS** measurements. Developed by Omicron GmbH, the system is divided into three chambers isolated from each other through gate valves. The introduction chamber (green box in Figure 2.15) is found next to the preparation chamber (yellow box). It allows the tip and sample transfer from air to the vacuum environment. The preparation chamber hosts an ion gun unit, a mass spectrometer and a Raman system. The third chamber is the analysis chamber (blue box) where cleaned spare tips and samples can be stored in a 6-slots carousel aside of the main measuring area.

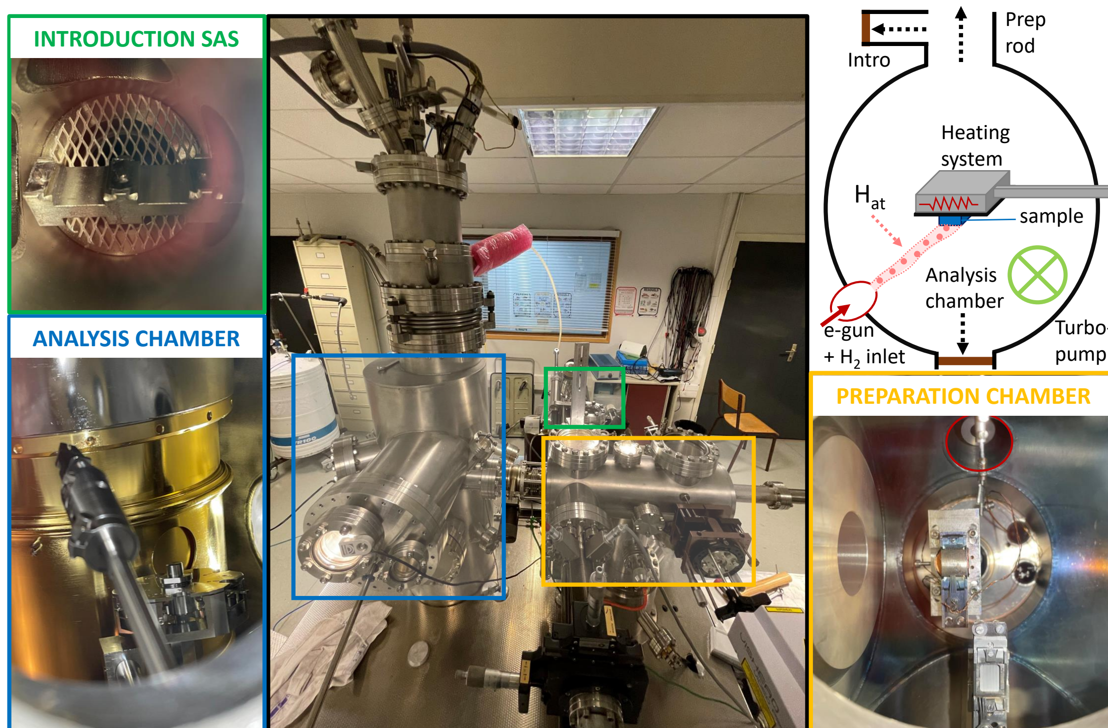


Figure 2.15: The Omicron **LT-STM** system, with insets bordered by different colors to highlight each parts of the setup. An extra schematic in the top right corner depicts how deoxidization of the sample is performed within the preparation chamber using a flux of $\mathbf{H_{AT}}$ injected from an ion-gun, the sample being maintained at high temperature on the manipulator stage.

To maintain the whole system under **UHV**, different pumping tools are used. The introduction chamber reaches a pressure as low as 10^{-8} Torr using a turbomolecular pump while the preparation and analysis chamber pressures are kept in the low 10^{-10} Torr range (even 10^{-11} Torr for the analysis) with the help of an ionic pump and **Titanium Sublimation Pumps (TSPs)**.

Because cryogenic temperatures of the system are needed to achieve the best resolution, the **STM** is equipped with a double cryostat unit. A larger cryostat surrounding the analysis chamber acting as a shield for the inner smaller one allows to keep the chamber cooled down. Depending on the temperature needed, either liquid helium (5 K) or nitrogen (77 K) can be filled in the cryostats, though for this work all results were collected at 77 K.

Aiming to have an ideal single-atom sharp apex for convenient tunneling spectroscopy, the tips are prepared via a reliable electro-chemical etching process of the W wire. The wire is dipped at the desired length inside a sodium hydroxide (NaOH) solution and a DC voltage is applied between the anode (the wire) and the cathode (placed in the bath as well). The electro-chemical reaction is then driven at the interface with the solution, the meniscus, where etching rate is higher in this region. As the part of the wire deeper in the solution etches slower, the necking shape of the tip is obtained. When the etched part of the wire at the meniscus is thin enough, the lower part falls off under the gravity leaving a sharp apex on the W tip.

The sample and the tips are both fixed on their respective carrier plate. Following their introduction under **UHV**, the loadlock is outgassed for several hours at 120 °C to get rid of any residual water inside. Transfer rods allow then to carry the specimen through the preparation and analysis chamber. Annealing of the tip is performed by Joule effect heating from the mechanical contact of the W wire, away from the apex, with a tantalum sheet to remove any oxides that may have reacted on the tip apex. The heating is monitored using the electric current based on the pressure, once the wire becomes orange as seen from a visible naked eye looking through a viewport. When the pressure drops back to the standard value, the tip is then 'flashed' (rapid increase of the current to heat the tip to a high temperature), up to a bright yellow color and cooled quickly to make sure the contaminants are removed. The flashing process also allows the tip apex to crystallize in order to ensure optimal conditions for stable scanning. This step is repeated 5 times while monitoring the pressure at all time to remain in a clean environment.

To remove surface oxides from the studied surfaces of InSb (111) the samples are heated to 340 °C for 1 h 30. Then, $\mathbf{H_{AT}}$ is sputtered using the ion gun (accelerating voltage of 1.5 kV) for 1 h 30, while maintaining the temperature of the sample at 340 °C (top right corner of Figure 2.15). Once deoxidization is done and pressure back in the low 10^{-10} Torr, the sample is ready for transfer to the analysis chamber.

The tip must be mounted first inside the analysis chamber. To do so, the tip holding plate is placed using the wobblestick (blue box in Figure 2.15) in the measuring chamber. Then, through the use of a CCD camera installed on a lateral viewport, the tip unit is moved using the piezoelectronic stepper motor to come and pick it up from the holder. Once the tip is caught magnetically and properly mounted, the unit is lowered completely and tip holding plate is placed back into the carousel.

For the transfer of the sample, it is first collected via the main transfer rod in the preparation chamber. Then, the gate valve to the analysis chamber is opened and the sample is placed in one of the carousel free slots. As per the blue box from Figure 2.15, the sample is then picked up through the wobblestick which can move freely in x,y,z direction. The sample is flipped to have surface pointing down and placed in the chamber.

With both the tip and the sample mounted, the scanning can start. Both shields are closed to ensure the thermal and vibrationnal stability at 77 K. Coarse approach of the tip is done using the stepper motor and the CCD camera to place it few microns above the sample once the tip mirror reflection from the surface is seen. Eventually, the tunneling approach is automatically done using the built-in function developed on the Nanonis controller (Specs GmbH).

2.3.5 Omicron Four-Probe STM

Fabricated by Omicron as well, the so called "Nanoprobe", a **Four Probe Scanning Tunneling Microscope** (**4P-STM**) further extends the characterization capabilities of the **multi-physics characterization platform (PCMP-PCP)** at IEMN. Figure 2.16 displays all the main constituting elements of the Nanoprobe. An introduction chamber allows to store up to 6 samples or tips under **UHV**. The preparation chamber gathers also 6 storage positions and includes a central translating manipulator combined to a direct current heating unit for sample preparation. Close to the manipulator a combined gas injection input, a filament and a tantalum sheet are found for the surface and tip preparations. The same process described in the previous section 2.3.4 was used for tip preparation.

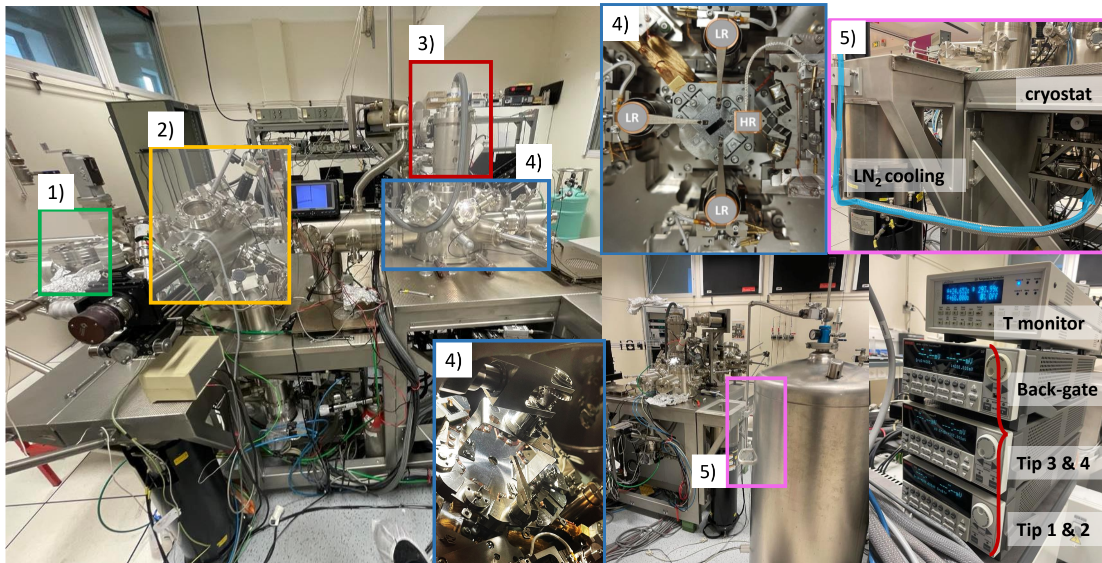


Figure 2.16: Photographs of the Omicron Nanoprobe system. 1) Introduction chamber (green box), 2) preparation chamber (yellow box), 3) **SEM** column (red box) and 4) analysis chamber (blue box) are present. 4) At the top, an aerial view of the **4P-STM** stage design, showing all 4 tips piezo units (adapted from[161], p.69). 4) At the bottom, the 10-slots carousel to store tips and samples is shown. 5) The cooling line system to the cryostat underneath the sample stage to perform **LT** measurements. Below, the Keithleys sourcemeters used for back-gated experiments (later explained in section 2.3.6.1) are shown.

On the other hand of the chamber a perpendicular transfer rod ensures that the sample and tips are moved to the analysis chamber. In this chamber, an optimized design allows to gather the measurement stage consisting of a **Scanning Electronic Microscope (SEM)** column located above, four piezoelectric units, rotated each of them by 90 degrees, and a 10-slots carousel. Among the four scanners, one has a compact design for holding tight a higher resolution (HR) probe, recognizable by the shorter tip length. Every unit (including the stage) is movable using a command controller for coarse positioning. The accurate movement of the tips towards a nanostructure is achieved thanks to the combination of the **SEM** navigation for localization and the tip displacement via low amplitude piezo drives through the Nanonis software.

For **LT** experiments, the Nanoprobe makes use of a liquid He/liquid N_2 flow cryostat to cool the sample down to 50 K at lowest. In the framework of this thesis, only liquid N_2 cooling was done, allowing to reach a sample temperature as low as 113 K, because the cryostat is thermally connected to the stage by a copper braid. This latter ensures a good mechanical decoupling

from the chamber. Because the stage only is cooled down, important tips thermalization time is needed to ensure a good electrical contact. Even after several hours, risks of tips damage, contact issues and so noisy measurements do exist in such thermal configuration.

2.3.6 Resistance measurements

To evaluate the nanostructure **Four Probe resistance (R_{4P})**, the tips are first brought close to the nanostructure under the operation of the **SEM**. Then, each tip is being contacted with a combination of manual manipulation and the auto-approach function of the Nanoprobe in the **STM** mode. The control system lowers the tip automatically on the surface with a Z-increment until a tunneling current is found. In usual conditions, a small voltage is applied on the tip (~100 mV) and a setpoint current is defined (100 pA). The tip contact is then done by manually disabling the Z-motor control, to let the tip drift and pushing it carefully down until a stable electrical contact is guaranteed. The **SEM** electron beam is blanked not to interfere with the sample transport measurement.

Two Keithley 2636B sourcemeters command the tips to collect $\mathbf{R_{4P}}$ after the tips are disconnected from the Nanonis control system thanks to the use of automatic switch boxes from the Omicron amplifiers. Conventionally, a **Two Probe resistance (R_{2P})** measurement for each probe configurations is performed to determine the associated contact resistances, traducing the contact quality.

The advantage of the four-probe configuration over two-probe lies in the suppression of the contact resistance in the collected data. In **4PP** measurement, two probes are configured to inject/collect a current and two extra probes are assigned to evaluate the voltage drop across the distance, which allows to get the nanostructure resistance just like Ohm's law ($U = RI$) by dividing the potential drop with the measured current.

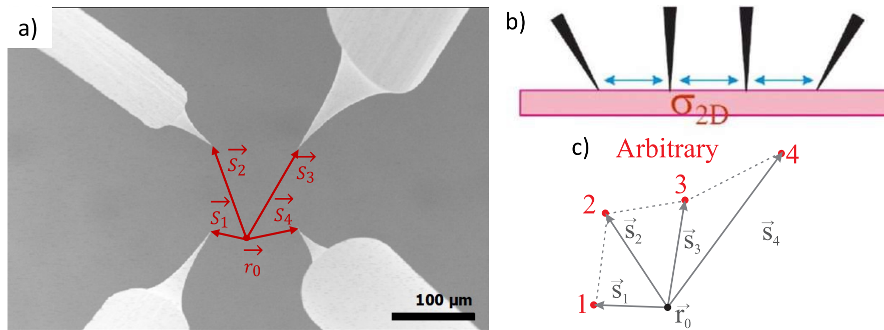


Figure 2.17: a) **SEM** image of the four probes with an arbitrary arrangement. b) Schematic of the 2D surface conductivity σ_s in the case of a **2DEG** with probe separation. c) Scheme of the arbitrary configuration for a resistance measurement on a **2DEG** showing probe separation. Extracted from[167].

The relationship for $\mathbf{R_{4P}}$ will depend on the nanostructure and the probe separation, for which in this study, the measurement on a 2D pad can be approximated with the equation given for a **2DEG** in arbitrary arrangement as shown in Figure 2.17

$$R_{4P}^{2D} = \frac{1}{2\pi\sigma_s}\left|\ln\frac{s_{13}s_{24}}{s_{23}s_{14}}\right| \tag{2.10}$$

where s_{ij} represents the probe separation between tips i and j and σ_s represents the surface conductivity.[167,168,169]

For the most studied structure, **NWs**, because the probes are on the same line, and only one tip is moving the equation becomes linearly dependant on the distance to simply be[170]

$$R_{4P}^{NW} = \frac{\rho d}{S} \tag{2.11}$$

with d corresponding to the two inner probe separation distance, ρ being the resistivity and S the cross-sectional area of the **NW**.

The Figure 2.18 shows an example of **4PP** resistance measurement that i performed using the **4P-STM** on 30 nm-thick HgTe in-plane **NWs** grown on a CdTe (001) substrate by **SAG** at CEA-LETI by Nicolas Chaize and Philippe Ballet in the frame of the ANR Inspiring project. In this case, the **NW** is ingeniously designed with lateral connections to larger pads that are easing the probe landing. With such design, the distance separation is exactly known from the lateral connections distance as in Figure 2.18a. In this example, the current is injected at the source and extracted by the drain. The voltage drop measured between V_1 and V_2 allows the calculation of the **NW** $\mathbf{R_{4P}}$. Several **NWs** of two different crystal orientations were probed at both **LT** and **RT**.

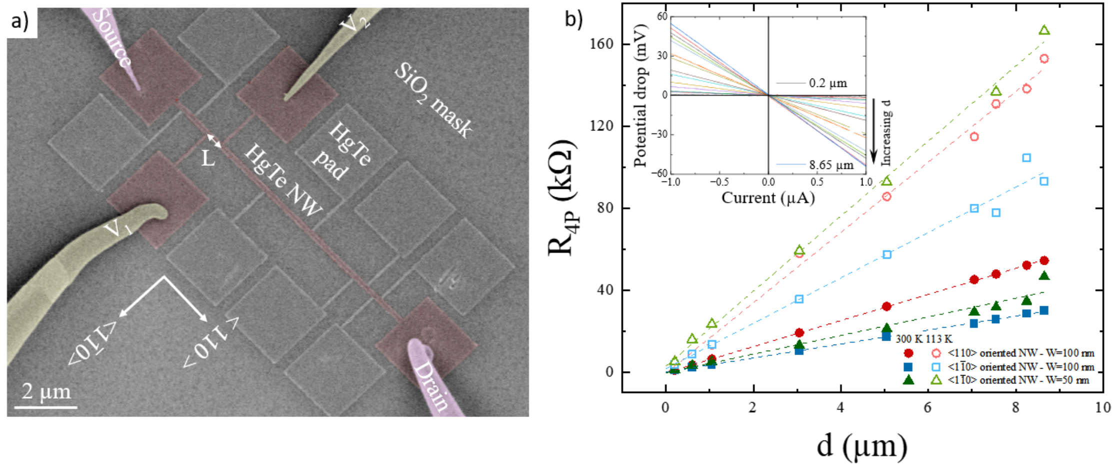


Figure 2.18: a) **SEM** image of a 30 nm-thick HgTe **NW** with lateral pads during **4PP** resistance measurements. The current is injected via the source and extracted by the drain while the voltage drop is measured between V_1 and V_2. The distance separation d between the potential probes is indicated. The **NW** was grown by the CEA-LETI. b) $\mathbf{R_{4P}}$ versus distance separation d collected at **LT** and **RT** for **NWs** of different crystal orientation. Inset: An example of the voltage drop between the inner probes as a function of injected current for increasing distance separation d (online publication available[171]).

The $\mathbf{R_{4P}}$ values all exhibit a linear trend as a function of the distance separation d which is consistent with a diffusive transport in these **NWs**. Significant variation in the resistance (thus conductivity, as $\sigma = (d/R_{4P})/(t.W)$) values between both orientations can be seen from the curves in Figure 2.18b. Such results correlate well with their cross-sectional analysis that showed a lower structural disorder for the $[1\bar{1}0]$ orientation, hence a lower $\mathbf{R_{4P}}$.[171]

2.3.6.1 Back-gated experiments

In order to further extend the possibilities of transport measurements and offers additional parameters extraction, the system configuration was adjusted to explore back-gated experiments. A third Keithley 2636B sourcemeter is added to control the voltage applied on the gate (Figure 2.16), *i.e.* at the back of the conductive sample. The sample is switched from ground to short and

the output directly connected to the new sourcemeter. Due to equipment related purpose, the automatic switchboxes are disconnected and replaced with older manual switchboxes achieving the same function.

The transport measurements are then commanded through Python scripts using the Spyder software. Two types of scripts (either adapted for **4PP** or **Two Point Probe (2PP)** configuration) are used for these measurements, to estimate key transport parameters such as the conductance G, the electron mobility μ or the carrier density n.

$$G = \frac{I_D}{\Delta V} \qquad \mu_{4p} = \left(\frac{D}{C_i W}\right) \cdot \frac{\partial G}{\partial V_g} \qquad n = \frac{d}{R_{4p} S q \mu_{4p}} \tag{2.12}$$

The Figure 2.19a represents a schematic of the back-gated circuit in the case of in-plane InSb **NW** heterostructures with a semiconductor barrier. A voltage difference is applied between the back of the sample and the source which conveys the back-gate voltage information. Then, as for usual **4PP** measurement, the voltage drop, $\Delta V = V_2 - V_1$, is evaluated between the two inner probes. Current is injected by the source and extracted by the drain.

The first script called "Output characteristics" collects $I_D = f(V_{DS})$ for various fixed values of **Gate-to-source Voltage ($\mathbf{V_{GS}}$)**, for which an example of measured curves is displayed in Figure 2.19b. The second script "Transfer curves" makes a loop on $\mathbf{V_{GS}}$ for various fixed values of V_{DS} corresponding to regular tests on **MOSFET** devices.

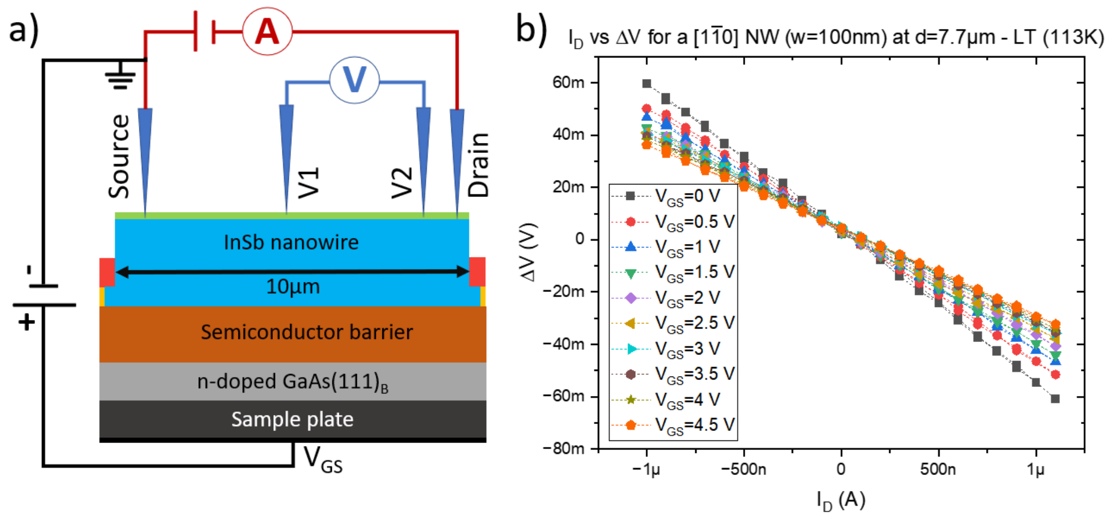


Figure 2.19: a) Simplified scheme of the back-gated **4PP** experiments for one of the analyzed heterostructure. A voltage is applied at the back of the sample relative the source. b) Example of a set of $I(V)$ curves measured at a fixed distance d between the potential probes and different gate voltages using the Output characteristics script.

2.4 Atomic Force Microscopy

Inspired by **STM**, **AFM** emerged not even a decade later by the same inventors.[172] This technique allowed to extend nanometric scale probing to non-conductive samples. In **AFM**, the tip is fixed on a flexible cantilever, acting as a spring, to interact with the surface of the sample, by mean of forces measurement and not tunneling current like in **STM**.

As visible on Figure 2.20a, when the tip is far away from the surface, interaction forces are negligible. As the tip-sample distance gets smaller, an attractive force (negative) is occurring before rapidly switching to a strong repulsive force for even smaller distances. To detect the variation of the forces, a laser beam focused on the cantilever end is reflected towards a segmented photodetector . From the deflection of the laser, the force is measured and adjusted with respect to a reference, thanks to a feedback loop electronic unit. During operation, the deflection of the spring-like cantilever is also translated from electrical signal into a useful topographical image.[173]

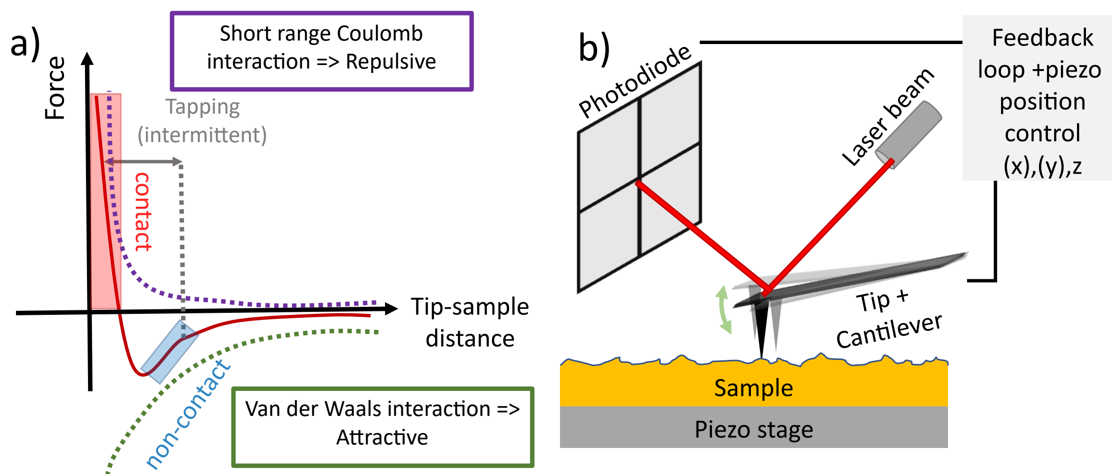


Figure 2.20: a) Schematic force-distance graph representing the various tip-sample interactions. b) **AFM** working principle with main components during tapping mode scanning.

AFM can be used in three different modes each of them depending on the interaction mode: contact, tapping, non-contact. Because contact mode can induce damages on the sample (repulsive force region), the tapping mode was preferred for all characterizations in this work.

In such mode, the cantilever is driven to vibrate close to its resonance frequency. When approaching the surface, the oscillation amplitude varies because of the change of the tip-sample interaction, which are mostly caused by Van der Waals or electrostatic forces. This amplitude change is referred as the detection signal. This one should be kept constant with the help of the feedback loop and piezo-system (Figure 2.20b) to monitor, in simple words, the probe height position.[174]

Located in the **PCMP-PCP** of **IEMN**, the **AFM** model Dimension 3100 from Bruker, with standard vertical and lateral resolutions of 0.1 nm and 10 nm respectively, was used for this thesis work. To limit as much as possible tip geometry effects on the resulting topographical images, **NCHV-A** probes supplied by Bruker were used. Their sharpness corresponds to a radius curvature at the apex of 10 nm or less. The resulting data consists in three different reconstructed images: a topographic, an amplitude (error correlated) and a phase image providing extra information on adhesive or composition variation on the surface.

2.5 X-Ray Diffraction

To assess the crystalline quality of all MBE-grown 2D films, the non-destructive characterization technique **XRD** was used. An incident X-Ray beam gets elastically scattered by the crystal lattice

structure of the sample and is then collected by a crystal analyzer. In usual operation, a raster scan on θ_B, the incident angle between the X-Ray beam and the surface of the sample is made, such that constructive interference will occur when the Bragg's law is satisfied

$$n\lambda = 2d_{hkl} \sin\theta_B \tag{2.13}$$

where λ is the X-Ray wavelength. In other words, for all sets of d_{hkl} planes characteristic of the crystalline sample, an intensity peak is visible on the resulting graph.[175]

Many derivative modes emerged from X-Ray techniques to further extend the extracted information such as grazing-incidence (**GIXRD**) for in-plane misorientation quantification, triple axis (**T-XRD**) for mismatch relaxation or even reflectivity (**XRR**) for film density and roughness analysis.

The X'Pert MRD model from Panalytical available in the **IEMN** III-V cleanroom, was used to achieve the structural characterization for thin films in the conventional mode. The system includes a Cu-Kα (λ = 1.54 Å) X-ray source. As seen on Figure 2.21, all incident angles can be varied independently ω, 2θ, χ, φ. Small range variations on ω and φ are necessary to find the optimum intensity of the diffraction peak. Larger scans on 2θ are then started as the routine analysis for our purpose. Using the built-in machine software, immediate check on the crystal quality as well as layer composition and relaxation can be done by fitting experimental data.

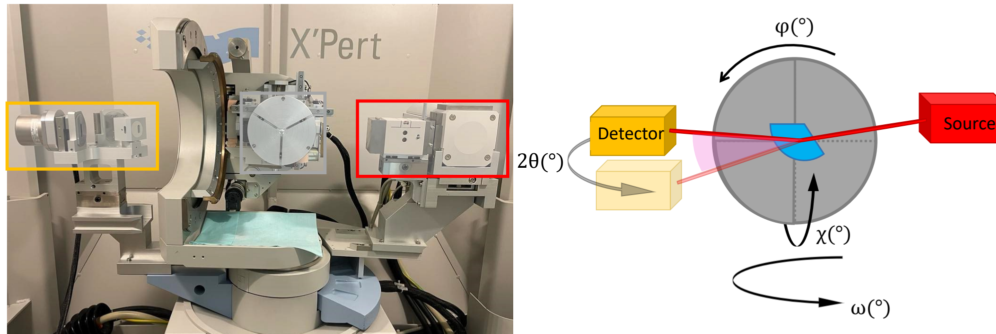


Figure 2.21: Photograph of the X'Pert MRD appartus, with associated schematic of the tool design. The detector (yellow box) rotates either together with the whole stage in ω angle or seperately during scan to cover a define 2θ angle range. The fixed X-ray source can be either equipped with an attenuator or not.

2.6 Electrical Characterization

2.6.1 Transfer length Method

Because the contact resistance R_c dictates in many ways heterojunctions performances (**MOSFET**, **High Electron Mobility Transistor (HEMT)**, solar cells,...) its proper determination does matter to understand how efficient the device can operate. A high R_c reduces the drive current, the switching speed, and increases power dissipation incident angle, directly affecting lifetime and reliability of the device.

To estimate the contact resistance R_c between the metal and the semiconductor or any other conductive material, we relied on the **TLM**. As schematized in Figure 2.22, the structure consists in an array of evaporated metal electrodes with known dimensions L and W with various spacing d on top of the layer of interest. This array is isolated from other devices by etching mesas down to the semiconductor barrier. By measuring $I-V$ characteristics for all different distances, the

resistance is expressed by

$$R_{TLM}(d) = 2R_c + \frac{R_{sh}}{W}d \tag{2.14}$$

where R_{sh} is the sheet resistance of the layer. Plotting then $R_{TLM} = f(d)$, the linear dependency with distance allows to extract R_c from y-axis intercept and deduce R_{sh} from the slope of the curve.[176,177]

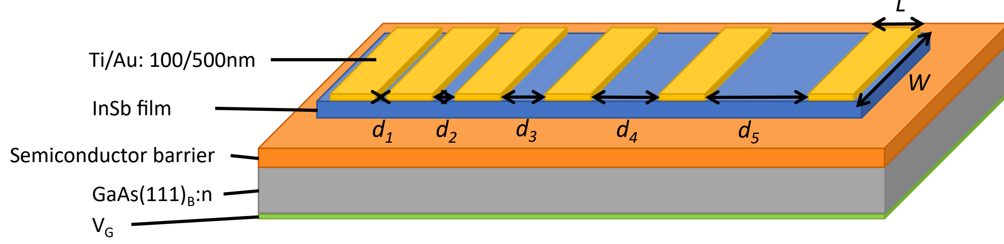


Figure 2.22: Schematic of a typical structure for **TLM** analysis.

Within the **Hyperfrequency Optical and Photonics Characterization (HOPC)** platform of IEMN, a four-probe bench was used for these experiments. The measurements were operated by Keithleys sourcemeters via the input parameters set on the IC-CAP software interface.

By approximating larger distance **TLM** structures as semi-infinite **2DEG**, it is possible to approach further electronic devices testing. One of the objectives in this work being focused on charge carrier density modulation, the system can be switched to the proper configuration for back-gated experiments. Such tests were then conducted on InSb heterojunctions on doped substrate to now collect $I_D = f(\mathbf{V_{GS}})$ transfer curves in order to extract the electron mobility µ, define the gate voltage leak-free region and determine the threshold voltage V_{th} or the carrier density n for instance.

2.6.2 Hall effect

For comparison and complementary purposes, Hall effect measurements were performed as well on InSb thin films. Discovered in the late XIXth century, this technique helps determining electronic transport properties via the generation of a voltage perpendicular to both a current flow and an applied magnetic field in a (semi-)conducting material. Because of the magnetic field, a Lorentz force is experienced by the moving charge carriers, pushing them to one side of the plate, which results in a voltage difference, called the Hall voltage V_H.[178,179]

$$V_H = \frac{IB}{qnd} \tag{2.15}$$

where I is the applied current, B the magnetic field, q the elementary charge for an electron 1.6 $\times 10^{-19}$ C, n the carrier concentration and d the thickness of the film.

The Hall coefficient R_H can then be deduced to describe the conduction type (a "+" sign means p-type semiconductor whereas a "−" sign is for n-type)

$$R_H = \frac{V_H d}{IB} = \frac{1}{qn} \tag{2.16}$$

The sheet resistance is then obtained from $R_{sh} = R_H/\mu = 1/nq\mu$. Experiments were done on a HL5500 Hall machine located in the **IEMN** III-V cleanroom. A permanent magnetic field equivalent to 0.32 T was applied. The measurements can be either performed at **RT** or **LT** (77 K),

by directly pouring liquid N_2 on the sample. Van der Pauw structures presented in Figure 2.23 were designed on the sample to allow for Hall effect measurements.

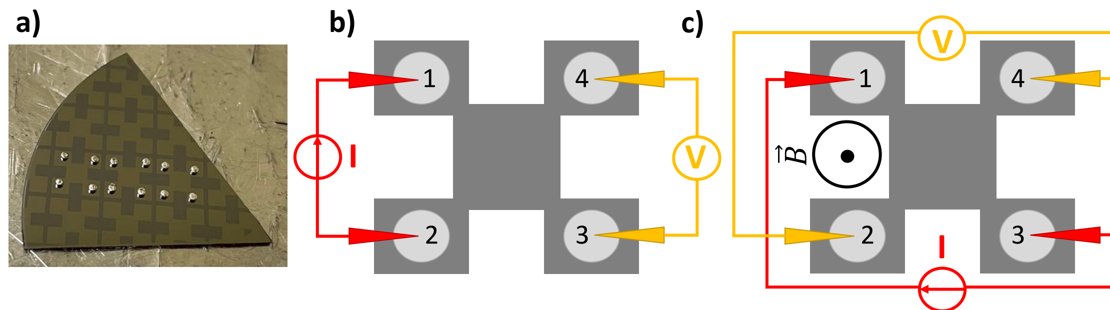


Figure 2.23: a) Example of a sample with Van der Pauw structures contacted with indium balls. b) Schematic of the resistance measurement to extract R_{sh}. c) Hall measurement in the presence of a magnetic filed $\vec{B}$ to collect the remaining electronic transport properties

To fabricate such structures, the **MBE** grown **Two-Dimmensional (2D)** InSb thin films were spin-coated with an AZ 1518 photoresist before undergoing UV light exposure through a chromium mask. Subsequent development was done in a MIF 726 solution for 20 s. Next, the heterostructures were etched in a $HF/H_2O_2/H_2O$ (1:1:200) solution and the remaining resist was removed in an acetone solution for 30 s. As a last step, the structures were topped with indium balls to ensure an Ohmic contact. The preparation of indium balls included a deoxidization step (dip in HNO_3 solution for 1 min then heating at 100 °C for 30 min) followed by an annealing step at 200 °C once the In balls were placed on the mesas to let In diffuse into the InSb films.

2.7 Additional characterization techniques

Throughout the entire masking process steps (after development, **RIE**, before chamber introduction, after **MBE** growth and oxide mask removal) an Ultra 55 Gemini **SEM** from Zeiss was used to monitor the sample preparation and qualify the nanostructures. The typical acceleration voltage was 10 kV for as-grown samples while the voltage was reduced below 1 kV to avoid damages on the resist-covered samples. The in-lens mode was preferred for easy high-resolution imaging.

Further microscopic characterization were done using a **High-Angle Annular Dark-Field (HAADF)-STEM** TFS 300 (FEI Titan) from Thermofisher as part of collaborative work with **Jülich Forschungszentrum*** to acquire cross-section **STEM** images. The objective here being the study of atomic interfaces, crystalline organization with lattice-mismatch induced defects, **NWs** morphologies and composition. For such deep analysis, **FIB** preparation of very thin lamellaes were done by ion milling. In this work, lamellaes were either prepared in-house at **IEMN** thanks to David Troadec or at **Jülich Forschungszentrum*** by Qianqian Lan.

For the control of the oxide mask thickness as well as the studies of the etching rate, an ellipsometer AutoSE model from Jobin Ivon HORIBA was used as a double check up technique to ensure correct sample masking preparation. The thickness is estimated from models fitting the experimental data in the built-in DeltaPsi2 software.

Last but not least, most part of the raw data like **AFM**, **STEM** images or even **STS** curves were processed using Mountains software from Digital Surf that allows multiple characterization data treatment. For any other raw files, Origin software was used to process experimental datasets.

Chapter 3

MBE growth of InSb thin films and in-plane NWs on CdTe substrate

3.1 Introduction

To benefit from the outstanding electron transport properties in InSb, it is necessary to achieve high quality thin films and nanostructures on a semi-insulating substrate or at least on an insulating layer. Given the very low lattice mismatch, the growth of InSb on a CdTe substrate is considered as the best option to limit the creation of crystal defects that could deteriorate the transport properties.

In this regard, this chapter will present the InSb growth on CdTe. At first, the growth of 2D epitaxial InSb thin films on CdTe (001) and (111) surfaces will be described. Then, based on the results obtained from these experiments, **SAG** of InSb nanostructures on CdTe will be studied. Throughout this chapter, several characterization techniques will be used to qualify and analyze the growth experiments, namely **AFM**, **XRD**, **XPS** (performed thanks to X.Wallart from EPIPHY team), **SEM** and Hall effect measurements.

3.2 InSb thin films on nearly lattice-matched CdTe substrates

Although the lattice constants of InSb and CdTe are almost identical (f = 0.046 %), a careful optimization of the growth conditions is needed to limit the intermixing at the interface between CdTe and InSb, which could favor the formation of an In_2Te_3 compound.[107,110] For that purpose, a thermal trade-off, as highlighted in chapter 1 section 1.4.3.3, must be found.

3.2.1 InSb thin films on CdTe (001) substrates

The first growth experiments were conducted on a (001)-oriented CdTe substrate investigating the InSb crystal quality by means of surface morphology analysis (**AFM**), surface chemical composition (**XPS**), crystal relaxation (**XRD**) and transport properties (Hall measurements).

3.2.1.1 Substrate deoxidation

Prior to the InSb growth, the CdTe wafers supplied by the CEA-LETI were introduced under **UHV** and outgassed at 150 °C for 1 h 30 before being transferred into the **MBE** chamber. The CdTe substrate deoxidation was performed to obtain a clean and well-ordered surface for the InSb nucleation. As the reactor was not equipped with II or VI element sources, no CdTe buffer layers could be grown after the removal of the native oxide layer and InSb has to be grown directly on the deoxidized CdTe substrate. It is thus primarily important to get a smooth surface after oxide removal.

The CdTe (001) substrates were deoxidized with a $\mathbf{H_{AT}}$ flux at 100 °C for 1 min. The **RHEED** already started to appear after this step. Then, the substrate temperature was further increased to 310 °C with a 10 °C/min heating ramp. As imaged in Figure 3.1, a clean (2 × 1) **RHEED** pattern is observed as reported in the literature.[109]

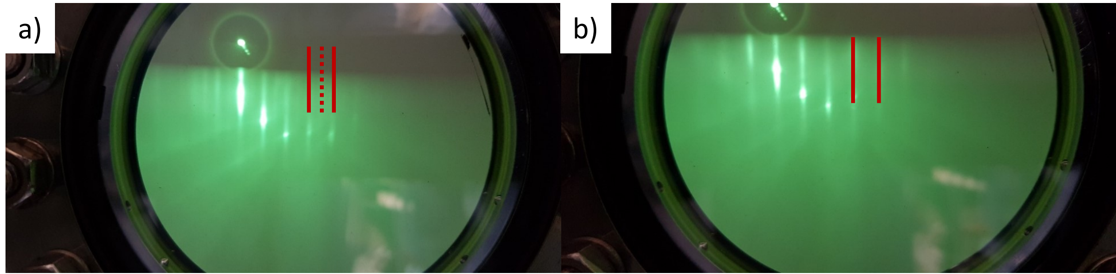


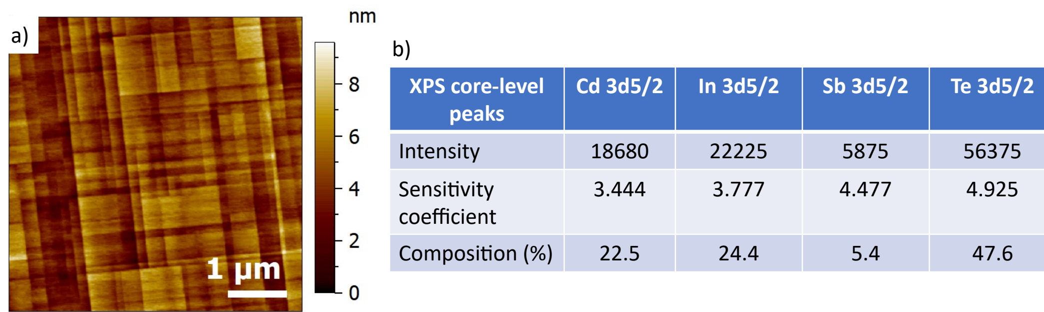
Figure 3.1: (2×1) **RHEED** pattern of the CdTe (001) surface after deoxidation with a a) two-fold periodicity (shown by the red dashed line) and b) the singular periodicity for a 90° rotation (no streak visible between the red lines).

3.2.1.2 Influence of the growth rate and temperature on InSb morphology

Two samples were prepared with different conditions to rapidly assess the effect of both the growth rate and temperature on the InSb film. Both samples were grown without $\mathbf{H_{AT}}$. Regarding the labeling convention of the samples, we decided to choose "IC..." to simply refer to InSb growth on CdTe. For the other systems considered in the next chapters, a similar convention system is adopted.

The first sample **IC1** was grown in a two-step process. First, 10 **ML**s of InSb were deposited at $\mathbf{T_G}$ = 320 °C. Then, the substrate was further heated up to 370 °C where the remaining 50 nm of InSb were grown. A low growth rate of 0.1 **ML**/s was used. The Sb/In ratio was set to 4 during the first 10 **ML**s of InSb and then increased to 10 for the subsequent 50 nm of InSb.

From the Figure 3.2a, the InSb morphology exhibits a 2D growth behavior with a relatively flat surface consisting of well defined atomic terraces. To further analyze the surface state of the InSb layer, **XPS** survey and core-levels spectra (available in Annex B, Figure B.1 and B.2) were collected directly after the epitaxial growth. As summarized in the table of Figure 3.2b, the **XPS** study revealed a degraded composition on the InSb surface, with a strong presence of Cd and Te at the expense of Sb, which is not present on the surface in great amount (in atomic %: Cd $3d_{5/2}$ = 22.5, In $3d_{5/2}$ = 24.4, Sb $3d_{5/2}$ = 5.4, Te $3d_{5/2}$ = 47.6). This result highlights the strong diffusion of Cd and Te through the InSb layer. As mentioned in the literature, the growth temperature of 370 °C for **IC1** was too high and favored the inter-diffusion of the species through the InSb layer, possibly also forming In_2Te_3 compound.[108,109,110,180] Based on these findings, we decided to lower the growth temperature of the InSb layer to avoid as much as possible the inter-diffusion of Cd and Te species.[181]



XPS core-level peaks	Cd 3d5/2	In 3d5/2	Sb 3d5/2	Te 3d5/2
Intensity	18680	22225	5875	56375
Sensitivity coefficient	3.444	3.777	4.477	4.925
Composition (%)	22.5	24.4	5.4	47.6

Figure 3.2: a) **AFM** image of sample **IC1** grown using the two-step process b) Summary table of the **XPS** analysis showing the composition on the surface of the sample **IC1**.

Therefore, the second sample **IC2** was grown at 320 °C. The Sb/In ratio was decreased to 1.5 while a moderate $\mathbf{V_G}$ = 0.5 **ML**/s was used. These modifications in the other growth parameters were done to evaluate how the morphology could change. As depicted in the topographic **AFM** image of Figure 3.3a, the InSb surface consists of hillocks, visible on the surface with a density of 5.2×10^{7} cm^{-2}.

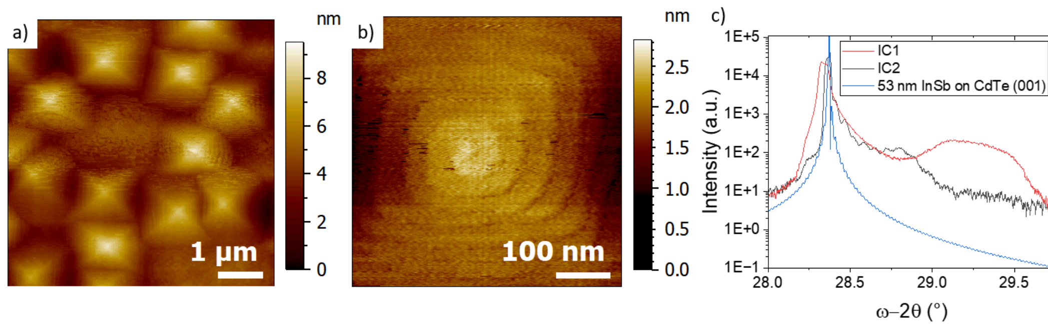


Figure 3.3: **AFM** images of sample **IC2** at a) large scale and b) small scale. c) **XRD** curve of samples **IC1** and **IC2** together with a simulated curve for a 53 nm-thick InSb film on CdTe (001).

At large scale, with a low resolution, they appear with a pyramidal shape. At small scale (Figure 3.3b), a clear spiral shape is guessed, indicating that each of these hillocks correspond to the step-flow growth from a screw dislocation core.[182,183]

Comparing now the **XRD** curves of the two samples **IC1** and **IC2** shown in Figure 3.3c, a clear difference is observed. The sample **IC1** exhibits a rather large diffraction peak, as well as a significant "bump" around 29.2°. This latter is a direct proof of the strong inter-diffusion of Cd and Te that occurred in the structure when InSb is grown at higher temperatures ($\mathbf{T_G}$ = 370 °C). Conversely, the sample **IC2** grown at lower temperature (320 °C) displays a narrower diffraction peak, which matches well the simulation for a 53 nm InSb film on CdTe. Though reduced, the inter-diffusion phenomenon might still have occurred as an enlarged area is visible on the spectra around 28.8°.

3.2.1.3 Hall effect measurements

To assess the transport properties of the InSb layer on CdTe (001), Hall effect measurements were performed on sample **IC2** after the definition of Van der Pauw Devices using optical lithography and chemical etching as explained in chapter 2 section 2.6.2. The results at both 300 K and 77 K are gathered in Table 3.1 below.

Temperature (K)	R_{sheet} ($\Omega/\square$)	n (10^{12} cm^{-2})	μ (cm^2.V^{-1}.s^{-1})
300	207	-7.78	3870
77	216	-7.6	3800

Table 3.1: Hall effect measurements at 300 K and 77 K of sample **IC2**, 53 nm InSb on CdTe (001) ($\mathbf{T_G}$ = 320 °C, $\mathbf{V_G}$ = 0.5 **ML**/s, V/III = 1.5).

At **RT**, the sample exhibits an electron mobility of 3870 cm^2.V^{-1}.s^{-1}. The negative carrier concentration indicates a n-type conductivity that suggests background doping due to the intermixing-induced defects, as the growth temperature above 300 °C enables Te diffusion.

At **LT** (77 K), almost no variation in the transport properties is seen. The mobility remains at 3800 cm^2.V^{-1}.s^{-1}, which interestingly highlights that the phonon scattering is not the dominant transport mechanism (in this case a higher mobility would be thus expected for **LT**). The transport limited by dislocations only occurs when their density is very high.[104] However, in this case, the important residual doping due to the Te diffusion or the heterovalent InSb/CdTe interface increases both the probability of interaction with ionized donors and scattering by the interface defects.

While a lower growth rate improves the structural quality of the InSb layer, the increased growth temperature favors detrimental inter-diffusion between InSb and CdTe which also impacts the transport properties as described in the previous section. In this regard, a lower growth temperature will be kept for later tests and the option to grow InSb on CdTe (111) substrates was explored more thoroughly.

3.2.2 InSb thin films on CdTe (111) substrates

3.2.2.1 Substrate deoxidation

Because the CdTe substrate cannot withstand high growth temperatures without a Cd flux exposure, the deoxidation process needs to be adjusted accordingly to obtain favorable surfaces for the growth of InSb. For the study on CdTe (111) substrates, two different deoxidation sequences were tested:

- The first recipe, called **DC1**, consisted in 1 min of $\mathbf{H_{AT}}$ plasma exposure at 75 °C. Then, the substrate was heated up to 320 °C and stabilized for InSb growth. The **RHEED** after deoxidation resulted in a (1×1) spotty **RHEED** pattern indicating a certain surface roughness.

- The optimized recipe, labelled **DC2** used the same first step of $\mathbf{H_{AT}}$ plasma exposure at 75 °C. However, it adopted thereafter a gentler heating ramp with adjusted P.I.D values. This was justified to avoid brutal temperature spikes due to power jolts of the controller. Then, above 300 °C, the Sb beam flux (set to 1 **ML**/s) was opened and closed manually to inject 2-3 **ML**s in order to sustain a sharper (1×1) **RHEED** (Figure 3.4a). This operation is repeated 3 – 4 times to preserve the CdTe surface until the temperature for InSb epitaxial growth was reached.

Although the **RHEED** pointed to a rough surface for sample **DC1**, no **AFM** analysis of the CdTe surface using the recipe **DC1** was done unfortunately. In contrast, the surface morphology prepared using the second deoxidation recipe **DC2** is shown in Figure 3.4b.

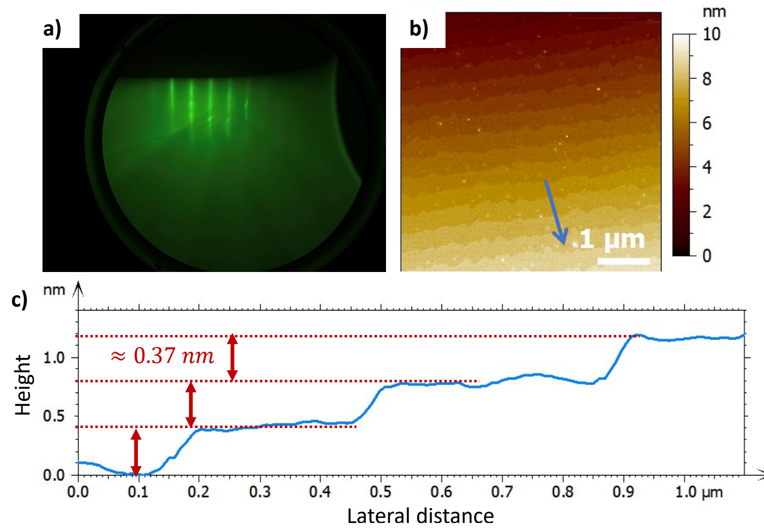


Figure 3.4: a) (1 × 1) **RHEED** reconstruction observed for the CdTe (111) surface. The pattern is streaky meaning the prepared surface is flat. b) **AFM** image of the CdTe (111) surface after the deoxidation sequence 2 (**DC2**) performed in the **MBE** system. The atomic terraces are clearly visible and their width is around 350 nm. c) Scan profile acquired along the downpointing blue arrow in a).

Based on the **AFM** image, the surface exhibits smooth atomic terraces. The **RMS** roughness of a terrace is lower than 0.15 nm which could contribute to proper InSb nucleation. The atomic height of a terrace measured with the **AFM** corresponds to the theoretical monolayer thickness of CdTe (111), $a_{CdTe}\sqrt{3}/3 = 0.374$ nm.

3.2.2.2 Growth conditions

Several samples were prepared using an iterative approach for the growth of the InSb layer. The growth parameters were empirically adjusted based on the previous sample morphology outcome. All conditions are summarized in Table 3.2.

Sample	**IC3**	**IC4**	**IC5**	**IC6**	**IC7**	**IC8**
V_G (ML/s)	0.05	0.05	0.05	0.05	0.05	0.05
Sb/In ratio	136	136	20	20	20	20
T_G (°C)	300	300	310	310	300	300
$t_{nominal}$ (nm)	30	50	2	5	30	30
H_{AT}	✗	✗	✗	✗	✗	✓
Deoxidation sequence	**DC1**	**DC1**	**DC1**	**DC2**	**DC2**	**DC2**

Table 3.2: InSb on CdTe (111) 2D sample growth conditions.

For all samples the growth rate was decreased to 0.05 **ML**/s with respect to the growth performed on the CdTe (001) substrate, in order to maximize the crystalline quality and uniformity of the InSb layer. Furthermore, we started with a high Sb/In ratio (136) based on previous observation of an InSb smooth growth on InP (111) substrates as described in Chapter 1 section 1.4.3.1.[22,98]

Regarding the different samples, the effects of the V/III ratio, the growth duration and the use of a $\mathbf{H_{AT}}$ flux exposure during epitaxy were studied throughout, **IC3**, **IC4**, **IC7** and **IC8**. The initial nucleation of the InSb film was studied with samples **IC5** and **IC6** which involved reduced InSb thicknesses of 2 and 5 nm respectively. The growth temperature was kept mainly at 300 °C and always below 330 °C to limit the inter-diffusion processes between InSb and CdTe. As a $\mathbf{H_{AT}}$ flux produced by a RF-plasma cell could be used to widen the selectivity window for **SAG** (RF power 600 W, H_2 98 %, Ar 2 %, total flux of 3 sccm), its influence on the growth of InSb thin films was also investigated.

3.2.3 Morphology of the InSb layers on CdTe (111) substrates

3.2.3.1 Influence of a high V/III ratio

As seen in Figure 3.5a, the high V/III ratio used for sample **IC3** causes the formation of isolated three-dimensional (3D) islands on a smooth background. These triangular islands cover around 40 % of the surface with a density of 7×10^{6} cm^{-2}, preventing the growth of a continuous film.

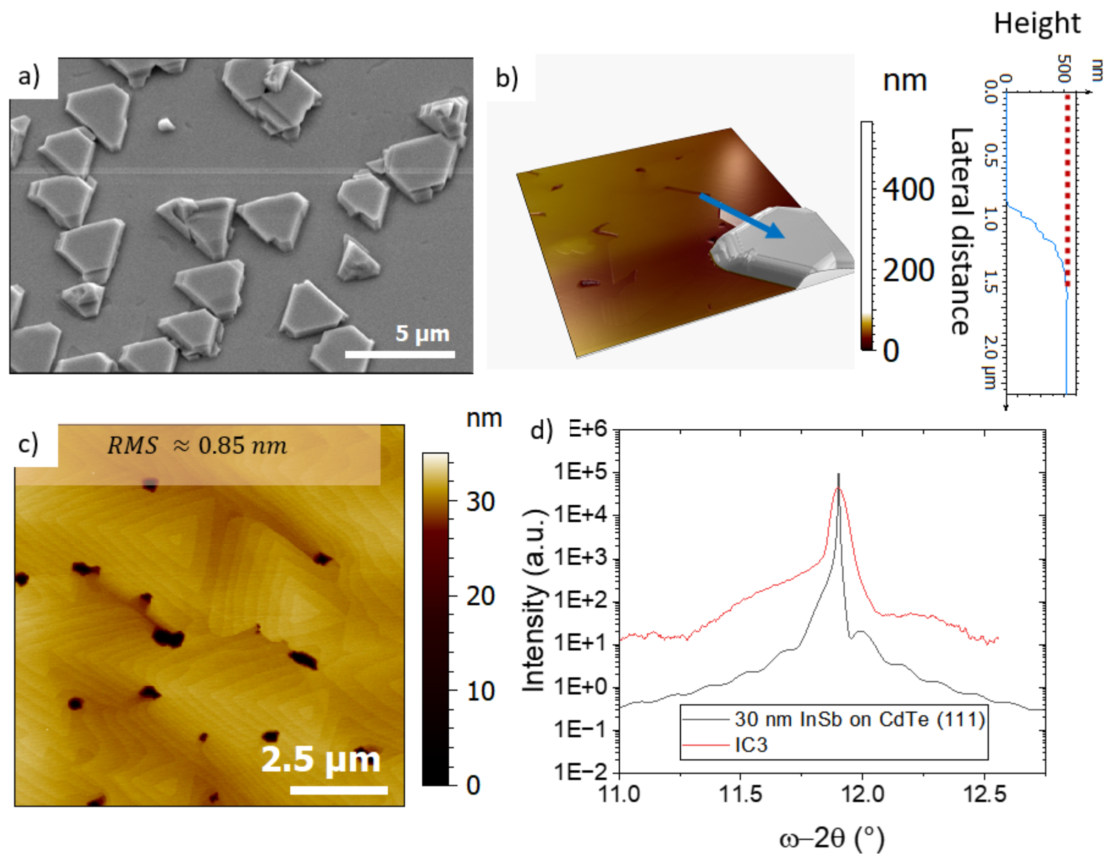


Figure 3.5: a) **SEM** image of the InSb/CdTe sample **IC3**. b) **AFM** image in 3D view showing an InSb island. The corresponding line profile is found on the right side. The island is 500 nm higher than the background. c) **AFM** image of the InSb surface in an island-free region. The **RMS** roughness does not take into account the nanoholes on the surface. d) **XRD** spectra of sample **IC3** with a simulation for a 30 nm-thick InSb film on CdTe (111) substrate represented by the black curve.

Despite the existence of these islands, the analysis of the **XRD** curves in Figure 3.5d reveals a relatively good quality of the InSb film when the InSb on CdTe growth temperature is kept below 330 °C. Indeed, compared to the growth performed with CdTe (001) substrate, the inter-diffusion of the Cd and Te species seems reduced as the shape of the spectrum matches well with the simulated curve.

Such a result is consistent with the **AFM** image acquired in an "island-free" area of the sample shown in Figure 3.5c. The surface consists of triangular shaped atomic terraces together with random unfilled areas. The coverage rate of the surface exceeds 98 % (excluding the unfilled areas) and accounts for the streaky (2×2) **RHEED** pattern observed during the whole growth of the InSb layer. The terrace width ranges between 250 and 300 nm. Upon checking the depth of the nanoholes, we find an average value of 30 nm matching exactly with the nominal thickness of the sample.

Focusing again on the triangular islands, their height reaches a mean value around 500 nm compared to the background as observed in Figure 3.5b. Because the Sb is largely in excess, we believe that this morphology results from Sb crystallites included in the InSb film.

The second experiement dealt with a longer growth time (sample **IC4**). Although the smoother contrast in Figure 3.6a compared to the one observed for sample **IC3** (Figure 3.5a) indicates a smaller island height, a similar morphology was obtained. The surface coverage of these hillocks goes up to 65 %. The **RHEED** showed a milky (1×1) reconstruction and supported such a morphology.

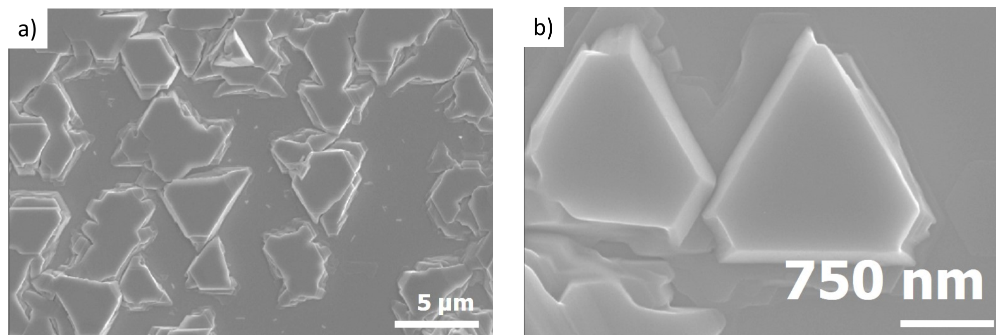


Figure 3.6: a) **SEM** image of the sample **IC4**. b) Magnified **SEM** image of two triangular islands.

Based on the morphology found for both samples, we believe that the over-excess of Sb is too detrimental at $\mathbf{T_G}$ = 300 °C. Because of the high Sb flux, this led to a Sb crystallization which comes up in the form of 3D islands.

3.2.3.2 Observation of the InSb nucleation

Before considering the **SAG** of InSb on CdTe (111), it is still interesting to study how InSb nucleation occurs on the CdTe surface. In this regard, samples **IC5** and **IC6**, involving smaller InSb thicknesses, were fabricated. Aware of the detrimental influence of a high Sb flux, the V/III ratio was drastically reduced (from 136 to 20). Figure 3.7 shows the AFM images of both samples.

At low coverage rate of InSb corresponding to a thickness of 2 nm (sample **IC5**), the morphology of the CdTe substrate is preserved as shown in Figure 3.7a). A lot of small islands have nucleated on the terraces, covering 7% of the surface. The nuclei are small enough so that the change of contrast induced by the step height is still visible.

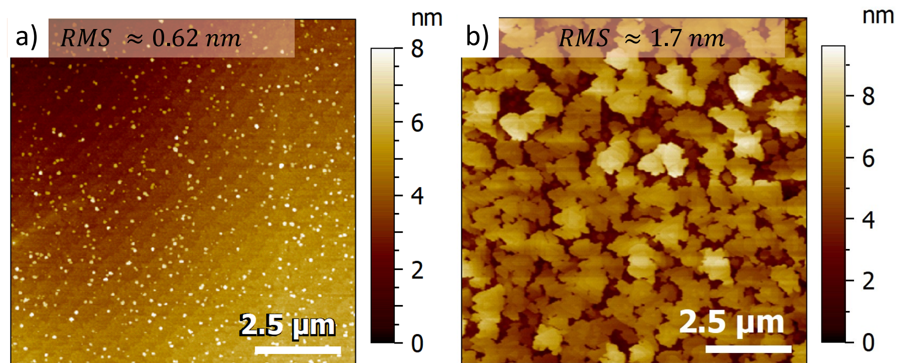


Figure 3.7: a) **AFM** image of sample **IC5** for a 2 nm InSb nucleation test. b) **AFM** image of sample **IC6** for a 5 nm InSb nucleation test.

For sample **IC6**, the morphology of the surface has changed. Irregular patches have replaced the periodic alignment of the terraces. The surface coverage reaches more than 80 % if we assume that the darkest region corresponds to the CdTe substrate. In this latter sample, the **RMS** roughness value gets higher than for sample **IC5** (1.7 nm vs 0.62 nm) due to larger regions coalescing with several unfilled areas in between.

3.2.3.3 Influence of a low V/III ratio and a flux of H_{AT} during growth

As no sign of Sb clustering was detected, we kept the V/III ratio to 20, meaning that the Sb flux was decreased from 6.8 to 1 **ML**/s for sample **IC7** in comparison with samples **IC3**. The InSb nominal thickness was set to 30 nm.

The InSb surface of sample **IC7** as shown in Figure 3.8a fully covers the CdTe substrate with no visible holes in the surface. The morphology consists of triangular concentric terraces of distributed widths between 100 and 350 nm. The **RMS** roughness value at a 10 µm × 10 µm scan size reduces to 0.54 nm with respect to sample **IC3**.

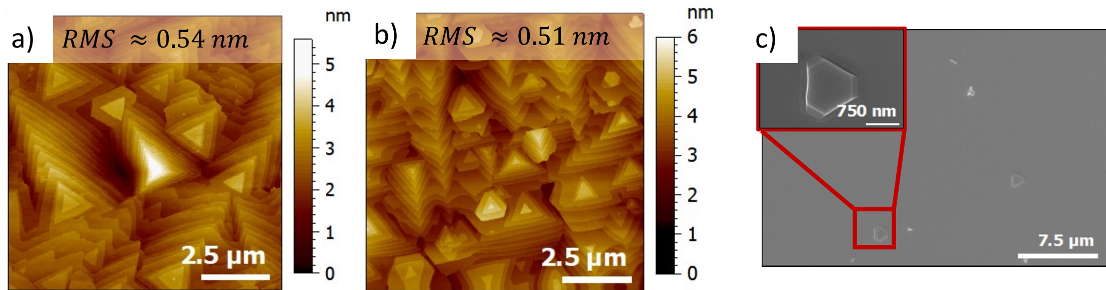


Figure 3.8: a) **AFM** image of the sample **IC7** in optimized V/III ratio conditions. b) **AFM** image of the sample **IC8**, with H_{AT} addition during growth. c) **SEM** image of sample **IC8** with a magnified view on a protrusion.

We note that for sample **IC8**, a H_{AT} flux exposure was added during the growth. The aim was to study the potential impact on the InSb morphology because H_{AT} enhances selectivity in the case of **SAG**. The comparison of Figures 3.8a and b indicates that the morphology remains similar with no impact on the general shape of the terraces. This result is consistent with an almost unchanged **RMS** roughness value between both samples. The formation of a smooth surface is confirmed through **SEM** images at larger scale for sample **IC8** as per Figure 3.8c.

Because of the reduced V/III ratio, the triangular islands seen on samples **IC3** and **IC4** are rare, covering less than 1 % of the surface. They are attributed to Sb clusters coming from the possibly still too high V/III ratio (Sb excess).

3.2.3.4 Hall effect measurements

In order to evaluate the transport properties of the InSb layer grown on the CdTe (111) substrate, Hall effect measurements were performed on sample **IC7**. Van der Pauw devices were defined using the process described in chapter 2 section 2.6.2. Table 3.3 presents the results at 300 K and 77 K for sample **IC7**. It also includes the data measured with sample **IC2** grown on CdTe (001) as well as the results from literature of InSb on CdTe (111) for comparison.

Sample	Temperature (K)	R_{sh} (Ω/□)	n (10^{12} cm^{-2})	μ (cm^2.V^{-1}.s^{-1})
IC7	300	642	-2.73	3560
IC7	77	818	-2.46	3100
Ref[111]	300	-	∼ -6	1000
Ref[112]	1.5	-	∼ -5.2	4400
IC2	300	207	-7.78	3870
IC2	77	216	-7.6	3800

Table 3.3: Hall effect measurements at 300 K and 77 K of sample **IC7**, 30 nm InSb on CdTe (111) ($\mathbf{T_G}$ = 300 °C, $\mathbf{V_G}$ = 0.05 **ML**/s, V/III = 20) and comparison with the data from sample **IC2**, 50 nm InSb on CdTe (001) ($\mathbf{T_G}$ = 320 °C, $\mathbf{V_G}$ = 0.5 **ML**/s, V/III = 1.5) as well as data reported in the literature[111,112].

At **RT** (300 K), sample **IC7** exhibits a carrier density of -2.73×10^{12} cm^{-2} which is approximately three times lower than the one from sample **IC2**. The electron mobility of sample **IC7** equals 3560 cm^2.V^{-1}.s^{-1} at 300 K. This charge density and mobility values aligns well with the ones reported in the literature despite the heterostructures are not fully comparable (∼1000 cm^2.V^{-1}.s^{-1} and -6×10^{12} cm^{-2} at 300 K for a 50 nm-thick InSb layer on a 1.2 µm-thick CdTe buffer on GaAs $(111)_B$ substrate[111] while a mobility of 4400 cm^2.V^{-1}.s^{-1} and a charge density of -5.2×10^{12} cm^{-2} were measured at 1.5 K for an $Al_{0.15}In_{0.85}Sb$ (40 nm)/InSb (30 nm)/CdTe (400 nm) **QW** on GaAs $(111)_B$ substrate[112]).

Despite the reduction in the InSb thickness compared to the sample **IC2** that would lead to a decrease in mobility (due to stronger surface and interface scattering), the sample **IC7** maintains a similar mobility value. With a similar thickness than **IC2** (e.g 50 nm of InSb as well), one could expect an improvement of the mobility thanks to the reduced roughness of the film. The increase in the sheet resistance to 642 Ω/□ is explained easily by the reduced mobility and carrier density using the formula:

$$R_{sh} = \frac{1}{q \cdot n \cdot \mu \cdot} \tag{3.1}$$

The small decrease (10 %) in the charge density obtained at **LT** (77 K) does not follow the usual variation of an intrinsic semiconductor as a function of the temperature. Hence, we can try to evaluate the importance of the doping type. The equation of the concentration of electrons in the conduction band for a n-type semiconductor is given by

$$n = N_c \exp\left[-(E_c - E_F)/kT\right] \tag{3.2}$$

where the density of states N_c is expressed by

$$N_c = 2\left(\frac{2 \times \pi \times m_e^* \times k \times T}{h^2}\right)^{3/2} \quad (3.3)$$

with m_e^* is the effective electron mass.

Based on equation 3.2 and the temperature dependence of $N_c \propto T^{3/2}$, we calculate the position of the Fermi level from the measured sheet densities. Doing the ratio $n_{77\ K}/n_{300\ K}$ we obtain the expression

$$\frac{n_{77\ K}}{n_{300\ K}} = \frac{N_c(77\ K)}{N_c(300\ K)} \times \exp\left[\left(\frac{E_F - E_C}{k}\right)\left(\frac{1}{77} - \frac{1}{300}\right)\right] \quad (3.4)$$

where

$$\frac{N_c(77\ K)}{N_c(300\ K)} = \left(\frac{77}{300}\right)^{3/2} \quad (3.5)$$

As all other parameters are known, we can isolate $E_F - E_C$ (using $k = 8.617 \times 10^{-5}$ eV/K) to get $E_F - E_C = 17.3$ meV. Knowing that kT value at 77 K equals to 6.65 meV, a quasi-degenerate regime happens, which confirms the small variation in the sheet density from lowering the temperature as the conduction band is already filled up due to the high doping here.

Conclusion

Although there is still room for further optimization, the growth conditions used for sample **IC8** led to a relatively smooth 2D InSb thin film. Both gentler deoxidation process (**DC2**) and lower V/III ratio have a positive combined effect on the InSb growth. The nucleation experiments pointed out that a rapid coverage of the surface is observed with around 80 % for only 5nm of InSb on CdTe (111). The transport properties evaluated from Hall effect measurements on Van der Pauw devices highlighted an improvement in the layer quality when InSb was grown under these optimized conditions on CdTe (111). It is explained by a lower defect density and limited Cd/Te interdiffusion. We believe it to be worth for sample **IC8** as well. Therefore, from the low roughness and hillocks density in thicker films, the **IC8**-like growth conditions ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ < 330 °C, low V/III ratio) act as a good starting point to transition towards in-plane InSb **NWs** on CdTe by **SAG**.

3.3 SAG of InSb on CdTe (111)

SAG was performed with mask A process , consisting of a 30 nm-thick SiO_2 layer that was patterned to form different nanostructure geometries. With this single layer dielectric mask, the apertures were fully etched down to the CdTe (111) substrate surface using a HF 1 % wet etch for around 40 s before the sample introduction under **UHV** and into the **MBE** reactor. Hence, as shown in chapter 2 section 2.2.5, the remaining SiO_2 mask thickness was ~15 – 20 nm with rounded aperture edges (not vertically sharp). The mask layout is referenced in Figure A.1 of appendix A under the label "Mask 1".

Figure A.1a shows an overview of the different nanostructures and geometric shapes that were patterned for the structural study of the nanostructures and their electronic transport properties. Figures A.1b and c emphasize on specific patterns which were useful to assess the structural quality of the nanostructures, respectively from in-plane observations or cross-sectional analysis with **STEM**. The most interesting designs that will be essential in investigating the growth morphology are presented in Figure A.1d and e.

First, a "sun-shape" structure (Figure A.1d) corresponds to **NWs** that are duplicated every 10° to form a 360° pattern. Such a pattern helps assessing the crystal orientation dependency of

the nanostructures. The **NWs** length is 10 µm and the aperture width is 100 nm (in some cases, also a pattern with 50 nm-wide opening is designed).

The second structure shown in Figure A.1e corresponds to patterns for **FIB** lamella preparation. They consist of an array of **NWs** with different aperture widths (3, 2, 1 µm, 500, 200, 100, 50 nm). The pitch between the **NWs** is equal to 1 µm for all apertures except the two narrowest ones (100 and 50 nm) where it is decreased to 500 nm. Thanks to this modulation of the aperture width, the influence of the lateral confinement will be investigated on the **NW** morphology. The length of the **NWs** is set to 10 µm.

3.3.1 Selection of the growth conditions

Starting from the favorable conditions for a smooth InSb 2D growth, *i.e.* low $\mathbf{V_G}$ = 0.05 **ML**/s, low V/III ratio around 20, $\mathbf{T_G}$ < 330 °C, several InSb **SAG** samples were grown with the conditions reported in Table 3.4. For the **SAG** samples, the naming convention is adapted by adding a "S" before the material combination, hence **SIC** refers to the **SAG** of InSb on CdTe substrates. As mentioned in the chapter 2 section 2.2.6, a CdTe bare (111) substrate is glued in the central area of the Si carrer to track the **RHEED** during InSb **SAG**.

Sample	SIC1	SIC2	SIC3	SIC4
$\mathbf{V_G}$ (ML/s)	0.05	0.05	0.05	0.05
Sb/In ratio	20	20	20	10
$\mathbf{T_G}$ (°C)	310	310	300	330
$t_{nominal}$ (nm)	2	5	30	30
$\mathbf{H_{AT}}$	✗	✗	✓	✓
Other				$\mathbf{H_{AT}}$ added after 5 nm of InSb

Table 3.4: Growth conditions for the **SAG** of InSb nanostructures on CdTe (111).

Table 3.4 illustrates the four different samples presented in this section. Nucleation tests were performed for samples **SIC1** and **SIC2** while much thicker InSb nanostructures were grown on sample **SIC3**. A two-step growth process was adopted for sample **SIC4** where the $\mathbf{H_{AT}}$ was only activated when the growth of the InSb layer reached a thickness of 5 nm.

3.3.1.1 InSb nucleation inside NWs apertures

Understanding the InSb nucleation inside the mask apertures in the context of **SAG** is essential to get a good control over the growth of the whole nanostructures. It provides information such as the growth mode (2D wetting layer or 3D islands), the interface quality and the selectivity rate (parasitic nucleation on the mask). Therefore, we started this study with samples **SIC1** and **SIC2**. Figure 3.9 and Figure 3.10 depict **SEM** and **AFM** images of the nucleation experiments performed for both samples. For sample **SIC1**, corresponding to the deposition of 2 nm of InSb on CdTe (111) ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 310 °C, V/III ratio = 20), the apertures created to grow the **NWs** appear dark in the **SEM** image of Figure 3.9a. Interestingly, they are surrounded by an area with a wiggled edge, which appears slightly darker than the SiO_2 surface. We attribute this area to HF wet under etching of the CdTe native oxide near the aperture edges.

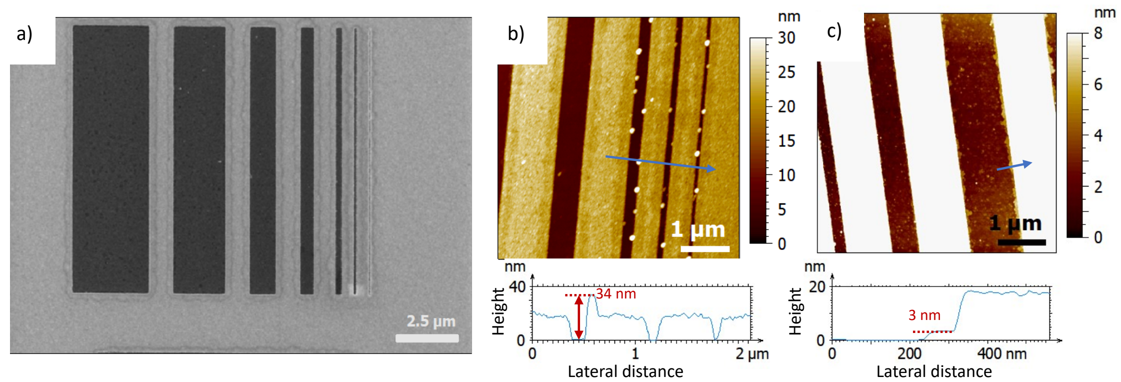


Figure 3.9: a) **SEM** image of sample **SIC1** showing **NWs** of different aperture widths. From left to the right, the theoretical width corresponds to 3, 2, 1 µm, 500, 200, 100, 50 nm. The pitch is equal to 1 µm for the largest apertures and to 500 nm for the last two apertures with a width of 100 and 50 nm. b) **AFM** image of sample **SIC1** at a smaller scale. The line profile plotted at the bottom was acquired along the blue arrow. c) **AFM** image of sample **SIC1** where the contrast has been enhanced to highlight the background of a larger aperture. The line profile plotted at the bottom was acquired along the blue arrow.

The comparison with the **AFM** image (Figure 3.9b) supports this hypothesis, as a narrow strip is visible along the edge of the dark apertures. The observation of the **AFM** image shows bright clusters in the narrower apertures. They are much higher than the ones observed for the 2D growth in Figure 3.7a. They are also higher than the thickness of the SiO_2 mask, which is about 17 nm based on the **AFM** profile. We believe that they predominantly appear in the narrower apertures because of the stronger lateral confinement, which promotes a 3D growth mode instead of a 2D growth mode. In the wider apertures, small islands with a height of 3 nm (considering the lowest data point in the center of aperture is the CdTe surface) can be observed by adjusting the color scale bar of the **AFM** image, as shown in Figure 3.9c. They nucleate at the edges of the apertures, because the dielectric mask prevents the adatoms from further diffusion.

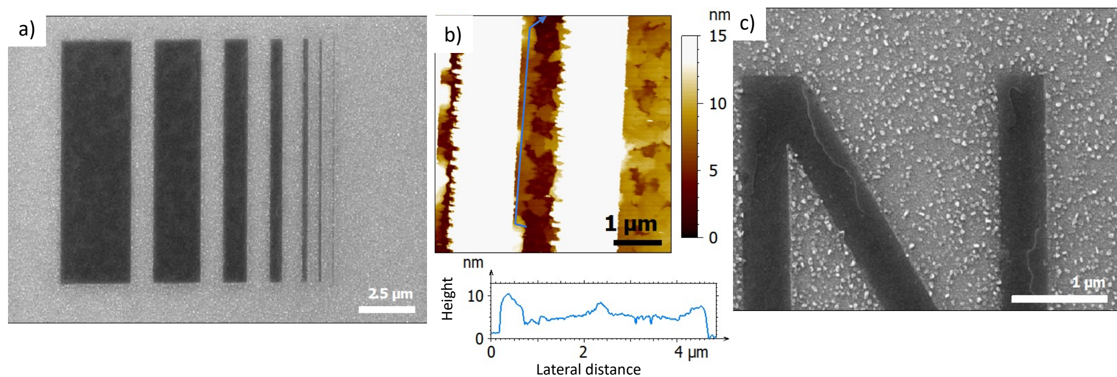


Figure 3.10: a) **SEM** image of sample **SIC2**. b) **AFM** image with an enhanced contrast to observe islands in the aperture. The line profile plotted at the bottom was acquired along the blue arrow. c) **SEM** image of the “N” from “IEMN” structure showing off both the InSb 2D smooth nucleation starting from the aperture edges and the parasitic nucleation on mask.

When 5 nm of InSb are deposited, corresponding to sample **SIC2**, the dark apertures do not show any new features in the **SEM** image, but the surface of the SiO_2 appear grainy (Figure 3.10a). At smaller scale, the growth mode as observed through **AFM** in Figure 3.10b remains

similar to the previous sample with InSb nucleating from the aperture edges. The measurement of their height variation with **AFM** yields 9 nm, a value which matches well with the expected 5 nm InSb thickness and the coverage rate of the surface. In this growth regime, the nuclei from both sides of the aperture expand before merging in the central area to form a smooth film.

The major difference between sample **SIC1** and **SIC2** arises from the change of the SiO_2 surface. The important parasitic nucleation visible on the **SEM** images of sample **SIC2** (Figure 3.10c) is due to a poor selectivity for the growth in this temperature range with no $\mathbf{H_{AT}}$ flux.

3.3.1.2 $\mathbf{H_{AT}}$-assisted SAG of InSb on CdTe

As flat and smooth InSb islands were observed on the CdTe surface in the case of 2D thin films on sample **IC8**, the **SAG** sample **SIC3** was fabricated using the same optimized growth conditions with a $\mathbf{H_{AT}}$ plasma addition during the whole growth to mitigate the formation of clusters on the mask. The InSb thickness was set to 30 nm in order to assess the structural quality of the various nanostructures. From the observation of Figure 3.11a, a significant parasitic nucleation on the mask is still evidenced. Although the $\mathbf{H_{AT}}$ flux addition during growth helped decreasing this phenomenon, the growth temperature is too low to ensure a sufficiently high In/Sb desorption from the mask. Additionally, the high Sb/In ratio favors the formation of not only clusters but also chunks which might predominantly consists of Sb.

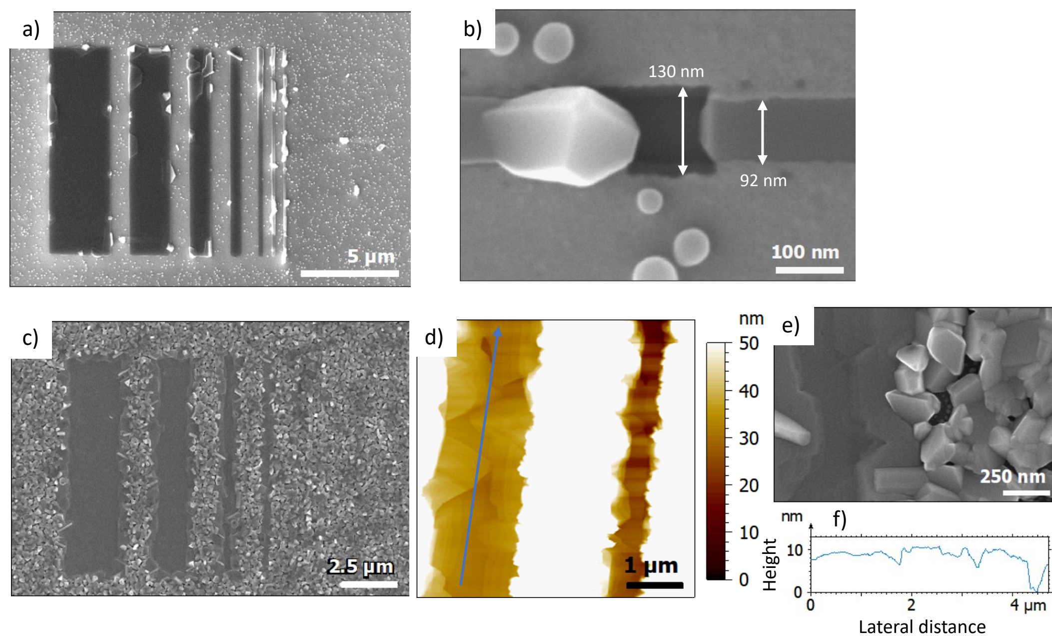


Figure 3.11: a) **SEM** image of sample **SIC3** obtained after an InSb deposition of 30 nm on CdTe (111). b) Zoomed-in **SEM** image of a partially filled aperture, designed with a 50 nm width, illustrating the influence of the $\mathbf{H_{AT}}$ flux exposure on a CdTe opening. The highlighted distances show the respective etching. This is visible through the dark contrast lines near each aperture edge in the central part of the image. The HF wet etch step enlarged the aperture up to 92 nm. c) **SEM** image of sample **SIC4** grown in two-steps. Important nucleation on the dielectric mask is visible. d) **AFM** image of sample **SIC4** with an enhanced contrast to highlight InSb islands in an aperture. The blue arrow corresponds to the line profile shown in f). e) **SEM** image of the edge of a wide aperture filled with InSb (left side of the picture) and parasitic nucleation on the mask (right side of the picture).

Regarding the InSb **NWs**, a different morphology is visible according to their width. The larger apertures seems filled with a quite smooth InSb layer exhibiting a few clusters on the edges. In the narrowest apertures (100 and 50 nm), these clusters results in very rough **NWs**.

At smaller scale, in the 50 nm-wide aperture (nominal value but rather 90 nm after masking process) depicted in Figure 3.11b, a mix between, both deep holes, with a mask under-etching of about 20 nm on each side and completely filled areas are observed in the mask opening. This means that the $\mathbf{H_{AT}}$ plasma exposure of the CdTe surface at 300 °C has resulted in the etching of the substrate in the opening and subsequent or concurrent InSb growth has occured to fill some part of the aperture. Depending on the $\mathbf{H_{AT}}$ plasma efficiency and substrate temperature such an etching of CdTe has been reported[184,185] and seems prohibitive for InSb **SAG**.

Therefore, an extra test experiment was conducted using a two-step growth process to counteract the etching of the CdTe (111) substrate during the $\mathbf{H_{AT}}$-assisted **SAG** of InSb. Sample **SIC4** was prepared as per the conditions reported in Table 3.4. In the first step, InSb was grown without any $\mathbf{H_{AT}}$ plasma during the first 5 nm to prevent the etching of CdTe. Because InSb wets uniformly the surface and coalesces rapidly as observed for sample **SIC3**, the CdTe substrate was supposed to be protected against $\mathbf{H_{AT}}$ for the remaining of the growth. Then, the $\mathbf{H_{AT}}$ plasma was activated for the remaining deposition of 25 nm of InSb without growth interruption.

As illustrated in Figure 3.11c, even though the CdTe etch is avoided, the two-step growth process does not improve the quality of the sample. While the InSb layer is smooth far from the edges of the aperture as shown in the **AFM** and **SEM** images of Figures 3.11d and e respectively, the absence of $\mathbf{H_{AT}}$ flux at the beginning of the growth leads to a full parasitic growth on the mask. In both images, the terraces appear higher along the edge of the apertures than in their middle, indicating that the growth nucleates at the aperture edges. The height profile measured with **AFM** indicates a mean value around 10 nm but with some downhills.

Consequently, the observed etching effect of the CdTe substrate under a $\mathbf{H_{AT}}$ flux exposure during InSb **SAG** seriously hinders the possibility to achieve smooth and high quality nanostructures on CdTe. Without any $\mathbf{H_{AT}}$ flux, the direct **SAG** of InSb on CdTe seems not feasible in a range of temperature limiting the inter-diffusion between the CdTe and InSb, as a large polycrystalline parasitic nucleation is seen on the mask. Therefore, a passivation layer preventing CdTe to be etched by $\mathbf{H_{AT}}$ has to be developed.

3.3.2 Growth of a GaSb 2D protective layer on CdTe

Among the available options on the **MBE** reactor, GaSb could be used as a potential protective layer on the CdTe substrate. The lattice mismatch between GaSb and InSb or CdTe is about 6 %, which is less extreme than with other III-V binary compounds like GaAs (14.6 %) or InP (10.4 %) but still high to induce defects like dislocations when the critical relaxation thickness is reached. The usual growth temperature for GaSb, around 500 °C, is higher than the one for InSb. In order to preserve the CdTe thermal stability and enlarge the critical relaxation thickness of GaSb, we will stick to the lower growth temperature established in our previous experiment *i.e.* below 340 °C. In this regard, two GaSb unmasked samples were first grown in order to check their surface morphology and possible use as an efficient capping layer protecting CdTe from $\mathbf{H_{AT}}$ etching. Their growth conditions are summarized in Table 3.5.

For this study, the CdTe substrates were prepared using the deoxidation sequence **DC2** as described in section 3.2.2.1. Moreover, no $\mathbf{H_{AT}}$ flux was added during the GaSb growth to prevent the etching of the CdTe substrate. All growth parameters were explicitly varied between the two experiments to confirm that no drastic changes are induced onto the GaSb thin film morphology.

Sample	**GC1**	**GC2**
$\mathbf{V_G}$ (*ML/s*)	0.7	0.2
Sb/Ga ratio	1.5	2.5
$\mathbf{T_G}$ (°C)	320	340
$t_{nominal}$ (nm)	5	10
Deoxidation sequence	**DC2**	**DC2**

Table 3.5: GaSb on CdTe (111) 2D sample growth conditions.

The GaSb surface of the first sample **GC1** presented in Figure 3.12a (5 nm-thick GaSb layer grown at $\mathbf{V_G}$ = 0.7 **ML**/s and $\mathbf{T_G}$ = 320 °C, Sb/Ga = 1.5) exhibits a granular aspect although atomic terraces of the underlying CdTe substrate are guessed. The **RMS** roughness remains low with a sub-nm value of 0.83 nm. At smaller scale, the GaSb film nucleated in small grains of random shapes that seldom merged, covering 90 % of the surface (Figure 3.12b). From the height profile, the mean value of the height variations lies around 5 nm. This result suggests a strain-driven growth mode.

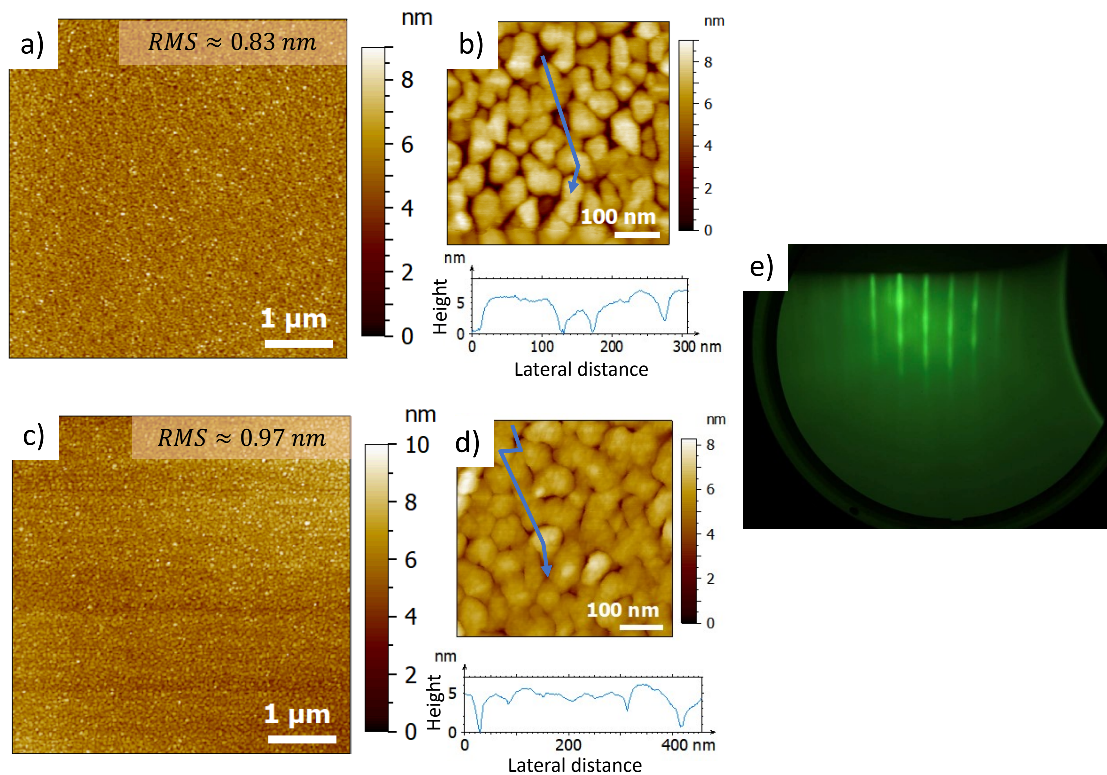


Figure 3.12: a) **AFM** image of sample **GC1**. b) Zoomed-in **AFM** image at 1 µm scale of sample **GC1** with a corresponding line profile indicated by the blue arrow. c) **AFM** image of sample **GC2**. d) Zoomed-in **AFM** image at 1 µm scale. The line profile below is extracted at the position of the blue arrow. e) (1 × 1) spotty **RHEED** at the end of the GaSb growth on CdTe.

The second sample **GC2** (10 nm of GaSb on CdTe at a lower $\mathbf{V_G}$ of 0.2 **ML**/s and higher $\mathbf{T_G}$) displays a similar morphology (Figure 3.12c). This confirms the negligible impact of a change of the growth parameters towards the GaSb layer morphology. As the thickness increased, the **RMS** roughness became slightly higher (0.97 nm). Based on the **AFM** image at smaller scale seen in Figure 3.12d, the layer covers more than 98 % of the surface leaving only few shallow holes behind.

For both samples, the **RHEED** consisted in a very spotty (1×1) reconstruction that refined along the growth to end up as a less spotty (1×1) **RHEED** with modulated streaks (Figure 3.12e). It indicates a multi-stepped surface,[154] which is consistent with the observed morphology. In the background, two faint intermediate streaks can be seen, which suggests a (3×3) Ga-stabilized surface.[186]

3.3.3 InSb SAG on GaSb/CdTe

Before transitioning to the **SAG** of InSb on GaSb/CdTe, an experiment in the form of a 2D InSb thin film on GaSb on CdTe was done (but not shown), which comforted us that the GaSb could be a solution for the InSb **SAG**. For this sample **IGC**, the CdTe substrate underwent the deoxidation sequence **DC2** and the GaSb growth made use of the same parameters as in sample **GC1** ($\mathbf{V_G}$ = 0.7 **ML**/s, $\mathbf{T_G}$ = 320 °C, Sb/Ga = 1.5, thickness of 5 nm). A subsequent 100 nm-thick InSb layer was grown on top of the GaSb layer at a low growth rate ($\mathbf{V_G}$ = 0.05 **ML**/s), Sb/In ratio (10) and similar growth temperature ($\mathbf{T_G}$ = 320 °C). During the growth, a streaky (2×2) **RHEED** was obtained for about 30 – 40 nm of InSb, but then suddenly collapsed into a milky (2×2) before changing into a weak (1×1) reconstruction. This degradation is probably linked to a difficult control of the temperature along the growth (increased infrared absorption in the thick InSb layer). Nevertheless, the streaky (2×2) **RHEED** obtained in the first stage convinced us that the GaSb could be a solution to protect the CdTe substrate while not interfering with the InSb morphology during **SAG**.

For the **SAG** sample (**SIGC**), a 5 nm-thick GaSb layer was grown on a new piece of CdTe (111) substrate in the same conditions as in sample **GC1** ($\mathbf{V_G}$ = 0.7 **ML**/s, Sb/Ga = 1.5, $\mathbf{T_G}$ = 320 °C). The GaSb layer was then patterned to define apertures for nanostructures. For this experiment, the mask B process was used (Al_2O_3/SiO_2 dielectric mask) because the HF wet-etch step in the mask A process (SiO_2 only) etches the GaSb. Moreover, the mask B process also allows to keep narrow and vertical apertures. At this point, we speculated that the geometrical confinement imposed by **SAG** help to limit the impact of the strain and defects, what should promote a smoother growth in the apertures. Because on the **SAG** sample, the GaSb surface is found in the aperture, the deoxidation sequence was done using a GaSb (001) substrate in the center of the Si carrier to track the **RHEED** correctly. The $\mathbf{H_{AT}}$ exposure was used since the beginning of the growth and kept active up to ∼300 °C. At this temperature, the **RHEED** started to appear. Then, the substrate temperature was further increased towards $\mathbf{T_G}$ under Sb overpressure without $\mathbf{H_{AT}}$. Once the temperature was stabilized, a 50 nm-thick InSb layer was then selectively deposited under $\mathbf{H_{AT}}$ exposure with the following conditions: $\mathbf{V_G}$ = 0.05 **ML**/s,$\mathbf{T_G}$ = 360 °C, Sb/In = 10.

Figure 3.13 shows two **SEM** images of the sample after growth, focusing on patterns consisting of crossed arrows and **IEMN** structures. A halo surrounding each structure is clearly seen, signature of the etching of the CdTe surface. This effect is quite strong in Figure 3.13b, where the InSb layer seems to have grown from the edges and the sub-etched regions underneath the masked GaSb layer (see the letter "E").

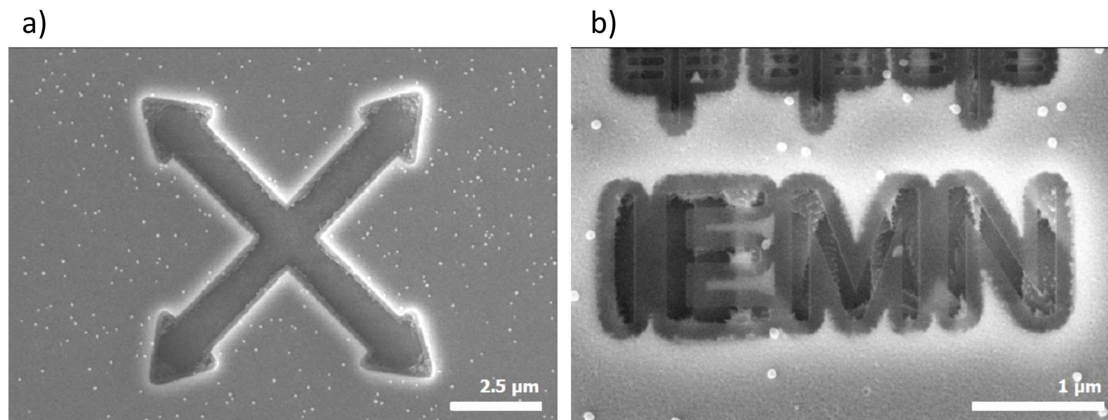


Figure 3.13: **SEM** images of sample **SIGC**, corresponding to the **SAG** of 50 nm-thick InSb nanostructures on 5 nm-thick GaSb layer grown on CdTe (111): a) crossed arrows and b) IEMN letters. The first pattern is localized in the mask “4” from Figure A.4b in appendix A. The **IEMN** structure can be found in Figure A.1b.

Despite the enhanced selectivity provided by the $\mathbf{H_{AT}}$ flux exposure, the granular morphology of the thin GaSb cap layer may result in a porosity of the GaSb layer and an insufficient protection of the CdTe surface to the $\mathbf{H_{AT}}$ flux exposure. Also, the thinning of the GaSb layer from the oxidation-desoxidation steps during the mask processing may lead to this $\mathbf{H_{AT}}$ etching of the exposed CdTe surface.

3.4 Conclusion

Throughout this chapter, the epitaxial growth of InSb thin films and nanostructures on CdTe (111) was detailed. The first section dedicated to 2D growth highlighted that a smooth InSb film with low **RMS** roughness can be grown under optimized conditions ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ < 330 °C, low V/III ratio) on CdTe (111) substrates. Nevertheless, to limit the inter-diffusion of Cd and Te species throughout the InSb layer that also alters the overall transport properties, a low growth temperature must be kept.

In the context of **SAG**, although the relatively weak lattice mismatch of the two compounds propelled this system as a potential association for growing high quality InSb nanostructures, the **SEM** observations after **SAG** revealed major issues arising from the etching of the CdTe substrate by the $\mathbf{H_{AT}}$ exposure, required to get a satisfactory selectivity for the InSb growth. The tentative use of a thin GaSb pseudomorphic layer on CdTe to prevent this etching effect was unfortunately unsuccessful, because of the porosity of the GaSb layer . This latter is probably related to the granular texture of the layer and its degradation during the mask fabrication process. Because of these limitations, that we were not able to mitigate, we decided to focus the work on the **SAG** of InSb nanostructures on GaAs substrates in the following chapters.

Chapter 4

MBE growth of InSb thin films and in-plane NWs on GaAs $(111)_B$ substrate

4.1 Introduction

Based on the mitigated results from the **MBE** growth of InSb on CdTe, which highlighted inter-diffusion problems as well as etching of the CdTe substrate by the **H_{AT}** plasma during **SAG**, we decided to investigate the heteroepitaxy of InSb on III-V mismatched substrate.

As mentioned in chapter 1 section 1.4.3.1, satisfying results were obtained for InSb epitaxial growth on InP (111) substrates in previous works from EPIPHY team.[22,98] In this work, as we have the ambition to introduce an efficient potential barrier between the substrate and the InSb layer, the growth on GaAs $(111)_B$ substrates is a straightforward choice as it offers either AlGaAs or GaInP as lattice-matched potential barrier options.

Consequently, this chapter focuses on the **MBE** growth of InSb thin films and in-plane **NWs** on GaAs $(111)_B$ substrates. This study is divided into three sections. Following the same approach as the one used in the previous chapter, the InSb thin film growth is first investigated. In order to analyze the surface reconstruction after oxide desorption, a **STM** study conducted on an InSb thin film on GaAs $(111)_B$ is detailed in the second section. The last section is dedicated to the **SAG** of in-plane InSb **NWs** on GaAs $(111)_B$.

Throughout this chapter, various characterization techniques are used to understand the mechanisms responsible for the InSb growth morphology on GaAs $(111)_B$ in both thin films and in-plane **NWs**. It includes a **STEM** study performed on InSb in-plane **NWs** to investigate the interface with the GaAs substrate and the possible lattice-mismatch induced defects. This latter study was realized thanks to a collaboration with the **Jülich Forschungszentrum** within the “PROCOPE” project.

4.2 InSb thin films on mismatched GaAs $(111)_B$ substrates

Due to the important lattice mismatch between InSb and GaAs (f = 14.6 %), the InSb growth on GaAs must be optimized in order to achieve high quality thin-films and nanostructures. Based

on the previous work related to the InSb growth on an InP $(111)_B$ substrate, it was observed that a large Sb flux helps minimizing the energy of the top InSb (111) surface[22] as well as the interface energy between InSb and InP and promotes the spreading of InSb on the mismatched substrate. Consequently, we investigate the use of a GaAs $(111)_B$ substrate with similar growth conditions to promote a rapid coverage of the surface and avoid an undesired 3D nucleation. However, the growth conditions require further tuning to favor the In diffusion on the substrate surface in order to minimize the density of InSb nuclei and quicken their lateral extent.

4.2.1 Which preparation for the GaAs surface ?

Prior to the growth of InSb, the GaAs $(111)_B$ wafers were introduced under **UHV** and outgassed at 200 °C for 1 h 30 before being loaded into the **MBE** chamber. The n-doped GaAs (111) substrates were supplied by Axiotron (AxT) ($-0.5° \leq$ (111) misorientation $\leq 0.5°$, $n = 2.5 \times 10^{18}/\text{cm}^3$) and Wafer Technology (WT) ($-0.1° \leq$ (111) misorientation $\leq 0.1°$ $n = 2.5 - 4 \times 10^{18}/\text{cm}^3$) and the name of the supplier will be mentioned for every experiments. Depending on the GaAs initial surface roughness, the energy at the interface between InSb and GaAs will be different, affecting the growth regime.

Usually, buffer layers are appreciated for producing a lower surface roughness than the one found on raw deoxidized substrates. In this regard, we investigated through **AFM** the GaAs surface state of two samples, the first one being a GaAs $(111)_B$ substrate deoxidized with a $\mathbf{H_{AT}}$ flux exposure while the second consists of a 50 nm-thick GaAs buffer grown on GaAs $(111)_B$.

For the GaAs deoxidation, the substrate (supplied by AxT) was first heated up to 360 °C. Then, the substrate was exposed to a $\mathbf{H_{AT}}$ flux while being further heated up to 440 °C under an As_4 pressure. The $\mathbf{H_{AT}}$ flux was then stopped and the temperature was increased to 570 °C under a larger As_4 pressure until the $(\sqrt{19} \times \sqrt{19})$ **RHEED** reconstruction was clearly seen.[187,188,189] The 50 nm-thick GaAs buffer was grown at $\mathbf{T_G}$ = 510 °C with $\mathbf{V_G}$ = 0.1 **ML**/s and V/III ratio = 10 after the substrate was properly deoxidized using the above mentioned procedure.

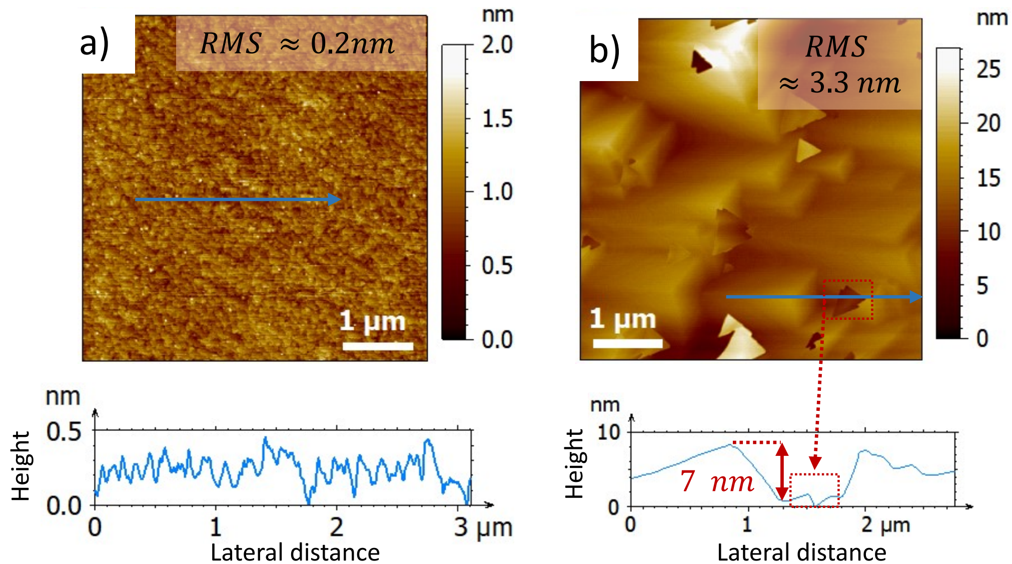


Figure 4.1: a) **AFM** image of the as-deoxidized GaAs substrate. A low **RMS** roughness is confirmed through the line profile. b) **AFM** image of the surface of the GaAs 50 nm-thick buffer layer. The profile crosses an elongated pyramid and an etch pit.

Looking at Figure 4.1a, the surface of the $\mathbf{H_{AT}}$-deoxidized GaAs $(111)_B$ substrate clearly shows atomic terraces with erratic edges. The morphology remains smooth with an overall **RMS** roughness of 0.2 nm at a 5 µm × 5 µm scale.

Conversely, as depicted in Figure 4.1b, the GaAs buffer surface shows a crowded elongated pyramidal morphology with additional triangular features randomly distributed. These latter are distinguished into two categories with the first gathering all triangular features "above" the surface and the other one "below" the main background. As illustrated by the height profile, the vertical base-to-summit separation of an elongated pyramid is 7 nm. The depression of a triangular feature is 1.6 nm. All these height variations contribute to a rough surface with a **RMS** roughness of 3.3 nm. The triangular shaped holes are assigned to be etch pits coming from Ga droplets[190] while the triangular hillocks are probably resulting from twin defects as their 180° misorientation with respect to the elongated pyramids suggests.

This pyramidal morphology of the GaAs buffer is in agreement with similar observations of GaAs $(111)_B$ substrates in the literature for similar growth conditions (low $\mathbf{V_G}$ and $\mathbf{T_G} \sim$ 500 °C).[191,192]

4.2.2 Growth conditions for the InSb film

All InSb growth experiments conducted on the GaAs $(111)_B$ substrates are gathered in Table 4.1. The samples are labelled with the same logic as in chapter 3 with **IG** standing for "InSb on GaAs".

Sample	**IG1**	**IG2**	**IG3**	**IG4**	**IG5**	**IG6**	**IG7**	**IG8**
$\mathbf{V_G}$ (*ML/s*)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
Sb/In ratio	136	136	136	136	136	136	136	136
$\mathbf{T_G}$ (°C)	380	380	390	380	385	390	400	390
$t_{nominal}$ (nm)	20	30	30	50	30	50	50	100
Supplier	AxT	AxT	AxT	AxT	AxT	AxT	AxT	AxT
buffer GaAs	✓	✗	✗	✗	✗	✗	✗	✗
(3×3) GaAs **RHEED** observation	✗	✗	✗	✗	✓	✓	✓	✓

Table 4.1: InSb on GaAs $(111)_B$ 2D sample growth conditions.

Regarding the GaAs substrate deoxidation, the same recipe as described in section 4.2.1 was used to obtain the clear $(\sqrt{19}\times\sqrt{19})$ **RHEED** reconstruction at 570 °C under a larger As_4 pressure. The substrate temperature was then lowered down to the corresponding growth temperature for InSb under a decreasing As_4 pressure, which is completely stopped below 400 °C. During this intermediate step (after GaAs deoxidation and before starting InSb growth), the GaAs **RHEED** reconstruction changed from the $(\sqrt{19}\times\sqrt{19})$ to either a (3×3) or a (2×2) surface reconstruction, as indicated in Table 4.1. For all experiments, a low growth rate was also used to promote the diffusion of the In adatoms towards energetically stable sites and to be in **SAG**-compatible conditions. A $\mathbf{H_{AT}}$ flux was also added during the InSb growth for all samples. Moreover, the Sb/In ratio was kept as high as possible, here 136, to reach a rapid coalescence of the InSb film as observed on InP (111) substrates. The higher growth temperature compared to InSb on CdTe (380 °C vs 300 °C) combined to the $\mathbf{H_{AT}}$ flux ensures a sufficient re-evaporation of the Sb species and avoid the formation of Sb crystallite as found in the previous chapter.

4.2.3 Influence of the growth parameters on the InSb film morphology

4.2.3.1 Influence of a GaAs buffer layer

To investigate the impact of the initial GaAs surface roughness on the nucleation of InSb, the sample **IG1** consisting of a 20 nm InSb layer grown on top of a 50 nm-thick GaAs layer (grown using the same conditions as for the GaAs buffer layer of section 4.2.1) is compared with a 30 nm-thick InSb layer grown with similar conditions but on a buffer-free GaAs $(111)_B$ substrate just after deoxidation (sample **IG2**).

As depicted in Figure 4.2a, the InSb film grown on the GaAs buffer layer consists of islands with heights ranging between 50 and 150 nm compared to the background. The observation of islands is consistent with a spotty (2×2) **RHEED** that was observed during the InSb growth. If we assume that the areas between the islands are depleted in InSb, then the surface coverage is relatively low as it reaches only about 33 %.

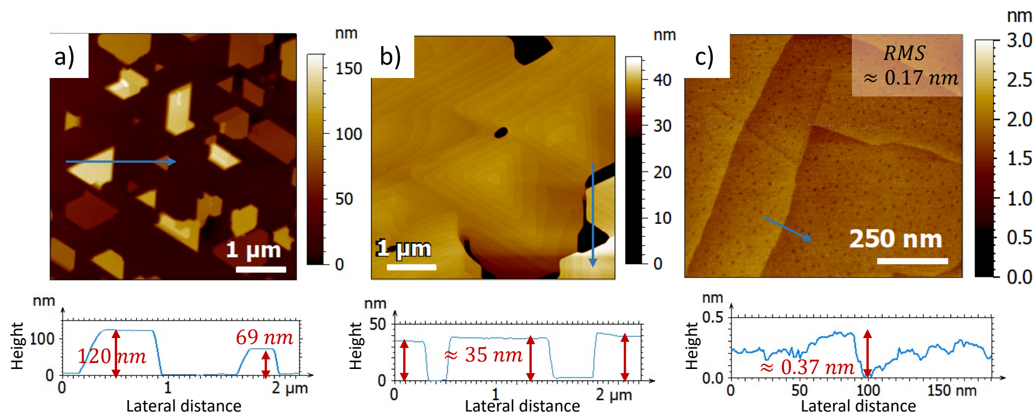


Figure 4.2: a) **AFM** image of the sample **IG1** with a line profile acquired at the position of the blue arrow. b) **AFM** image of the sample **IG2**. The height profile shown below, was acquired along the path defined by the blue arrow. c) **AFM** image at lower scale of the sample **IG2** showing the atomic terraces in a hole-free region.

For the sample **IG2** shown in Figure 4.2b, the InSb layer reveals to be smooth with few unfilled areas covering more than 93 % of the surface after a 30 nm-thick film. If we assume that the bottom of the holes consists of the GaAs substrate, the height profile yields an InSb thickness around 35 nm, which is close to the nominal value. When looking at smaller scale in a region with no holes, the atomic terraces are visible on the surface (Figure 4.2c). For both samples, the unfilled areas arise from the lattice mismatch between InSb and GaAs that also triggers the formation of 3D islands.

Comparing the InSb growth on the two different GaAs surfaces, the flatness obtained at low scale (**RMS** roughness of 0.17 nm) for the sample **IG2** added to the higher coverage of InSb on the just deoxidized GaAs surface outperforms the results obtained for InSb grown on a buffered GaAs substrate. Also, the morphology of sample **IG2** is similar to the one found for InSb on InP $(111)_B$ grown under high V/III ratio.

Based on such observations, the InSb thin film morphology appears to be strongly correlated with the underlying GaAs surface morphology. A rough initial GaAs surface favors the formation of dispersed and high InSb islands, delaying the coalescence of the InSb film, while a smooth GaAs surface promotes the spreading of InSb on GaAs. Consequently, the deoxidization of GaAs substrates under $\mathbf{H_{AT}}$ was kept as the main surface preparation technique as it produces a lower roughness template to favor a smooth growth of the InSb films.

4.2.3.2 Influence of a higher growth temperature

The next experiments were performed with growth conditions deduced from the optimization studies carried out for the InSb growth on InP (111),[22] requiring a moderate growth temperature and a large Sb overpressure (~390 °C and Sb/In = 136). Figure 4.3 gathers **AFM** and **SEM** images of the sample **IG3**. This latter was grown at slightly higher growth temperature (390 °C) than **IG2** (presented in section 4.2.3.1) to assess the growth sensitivity in this range of temperatures.

Despite the formation of a smooth film, a small fraction of the surface show islands probably originating from twin defects on Figure 4.3a and b.

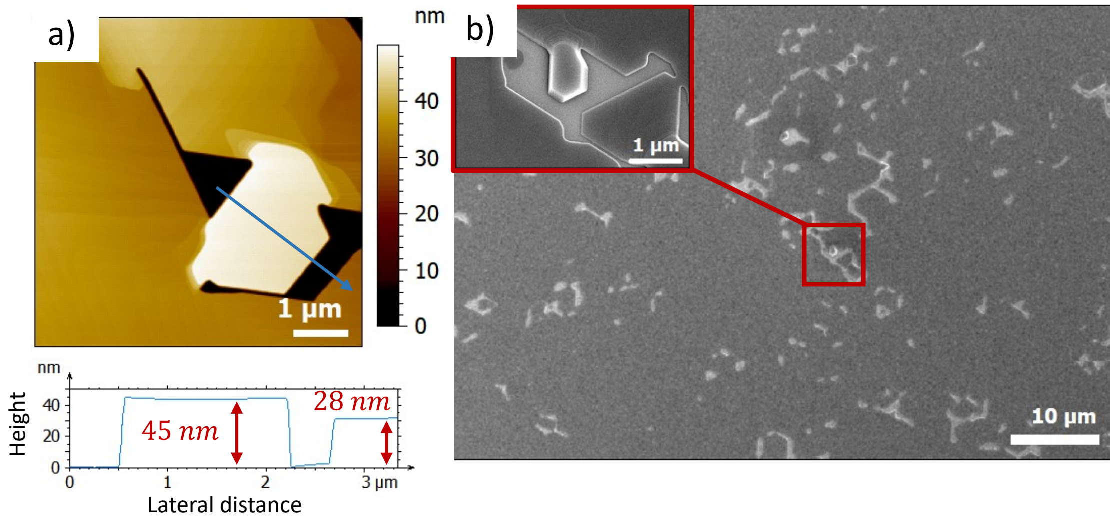


Figure 4.3: a) **AFM** image of sample **IG3**. The stepheight profile below was acquired across the island as indicated by the blue arrow b) **SEM** image of sample **IG3**. Inset: zoom of an InSb island surrounded by voids in the layer.

The inset of the **SEM** image in Figure 4.3b shows a bright contrast for the region encircling partly the island, which differs from the dark contrast observed on the InSb film. Based on this change of contrast, we assign this bright region to the GaAs surface. Hence, the presence of these defects limits the coalescence of the InSb film. This may be due to the formation cost of grain boundaries between differently oriented domains. If we assume that the bottom of the holes surrounding the island seen in Figure 4.3a consists of the GaAs substrate, then the height profile yields an InSb thickness of 45 nm. Such a difference is usually explained because the accumulation of material on the island results from its depletion in the surrounding.[191] The rest of the InSb layer matches the expected 30 nm thickness with a height of 28 nm as seen in the height profile of Figure 4.3a. More importantly, the overall coverage rate of the surface reaches 93 %. Through **XRD** measurements (Figure 4.4), the experimental curve matches well with a 30 nm-thick InSb layer on GaAs $(111)_B$ relaxed at 98 %, which supports the rapid coalescence of the film observed on **IG3** in these growth conditions.

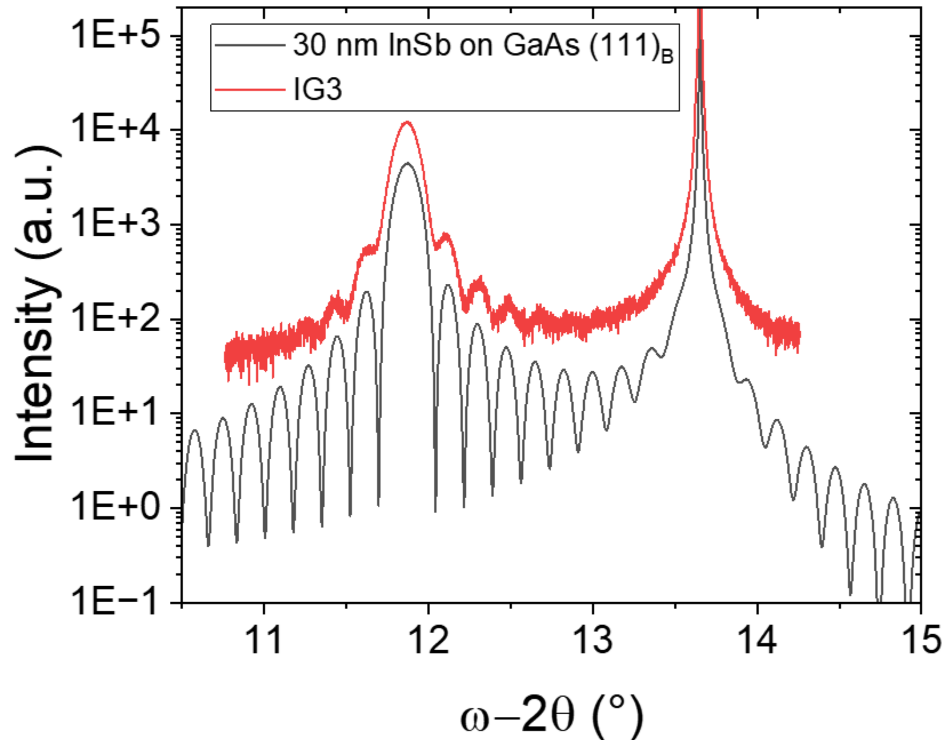


Figure 4.4: a) **XRD** curve of sample **IG3** and a simulation of 30 nm of InSb on GaAs $(111)_B$.

4.2.3.3 Influence of the film thickness

To end this study about the influence of the growth parameters, the effect of the InSb film thickness was investigated in order to determine if a full coverage of the surface was achievable. Referring to Table 4.1, sample **IG4** was grown using similar conditions than sample **IG2** (as no significant difference is observed for $\mathbf{T_G}$ = 380 °C instead of 390 °C and the difference is probably lower than the accuracy of the temperature measurement) but with a nominal film thickness of 50 nm instead of 30 nm.

Looking at Figure 4.5a, the surface morphology of the 50 nm-thick InSb layer (sample **IG4**) is identical to the one of the 30 nm thick layer (sample **IG2**), displayed in Figure 4.2b. The surface reveals a succession of atomic terraces consisting of triangular edges with rounded apexes. Some unfilled areas are still visible on the surface. The height profile over a hole shows a 56 nm-deep trench. The measurement of such a profile is consistent with the increase of the nominal thickness. It also agrees with the slight increase of the layer thickness due to incomplete coverage, which implies a higher deposition on the areas covering the substrate. The surface coverage rate of 97 % remains comparable to the 30 nm-thick sample **IG2**, demonstrating that for this range of thicknesses, there is no significant impact. In order to reach the full surface coverage (100 %), we can imagine that the InSb thickness must reach several hundreds of nanometers.

4.2.3.4 Influence of the GaAs surface reconstruction on the InSb thin film surface coverage

The graph in Figure 4.5b summarizes the surface coverage rate observed with **AFM** for all the samples prepared for this study. Although the main growth parameters were not so much different, we can see that, four samples show a surface coverage rate below 90%: **IG5**, **IG6**, **IG7**,

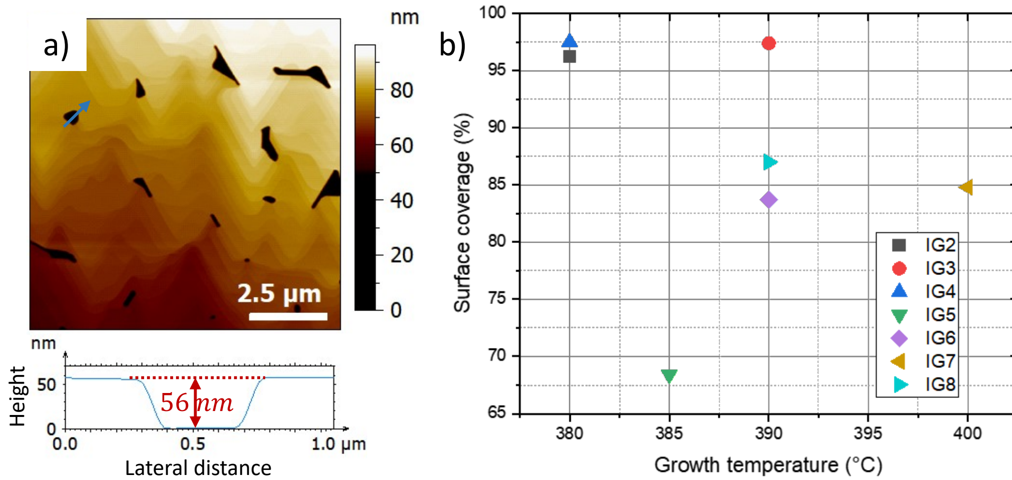


Figure 4.5: a) **AFM** image of sample **IG4**. Height profile across a nano-hole represented by the blue arrow. b) Scatter plot of the surface coverage rate versus $\mathbf{T_G}$ for different **IG** samples.

IG8. These samples were grown on deoxidized substrates and as demonstrated in the previous section, the differences in their thickness does not account for such a lower surface coverage rate.

With further investigations, these four samples with a lower surface coverage only differ from the other ones by the presence of a (3×3) reconstruction after the GaAs substrate deoxidation observed by **RHEED**. Only a few articles mentioned such surface reconstruction in the literature. While Thornton *et al.*[188] observed some elements (trimers) of a (3×3) periodicity through a **STM** analysis on GaAs $(111)_B$ substrates after annealing at 500 °C, Mac Rae *et al.*[193] reported a (3×3) pattern using **Low Energy Electron Diffraction (LEED)** on GaAs $(111)_B$ surfaces. Moriarty *et al.* deposited Sb on a GaAs $(111)_B$ (2×2) reconstructed surface, followed by an annealing between 300 and 525 °C, which resulted in local arrangements of Sb trimers in a (1×3) reconstruction.

Thanks to these experimental observations, a schematic surface reconstruction diagram of GaAs $(111)_B$ is presented in Figure 4.6, which helps further understanding the InSb coverage issue. As mentioned previously, the last step of the GaAs deoxidation consists in an annealing step under an As flux (usually around 4 – 5 **ML**/s) until a sharp $(\sqrt{19} \times \sqrt{19})$ reconstruction becomes visible (usually for 530 °C $< T_{sub} <$ 570 °C).[196,197]

In the case of samples **IG5**, **IG6**, **IG7**, **IG8**, the (3×3) reconstruction was witnessed when the temperature was lowered to $\mathbf{T_G}$ before the growth of the InSb layer. In other words, this means that after the $(\sqrt{19} \times \sqrt{19})$ was observed and while the temperature decreased, the As_4 flux was reduced, which resulted in the transition to the (3×3) reconstruction at intermediate temperature. Although further experiments would be required to determine if the occurrence of a (3×3) reconstruction on GaAs is really linked to a certain residual Sb pressure in the chamber from previous growths, these observations prove that the substrate preparation conditions strongly impact the growth regime of the subsequent InSb layer.

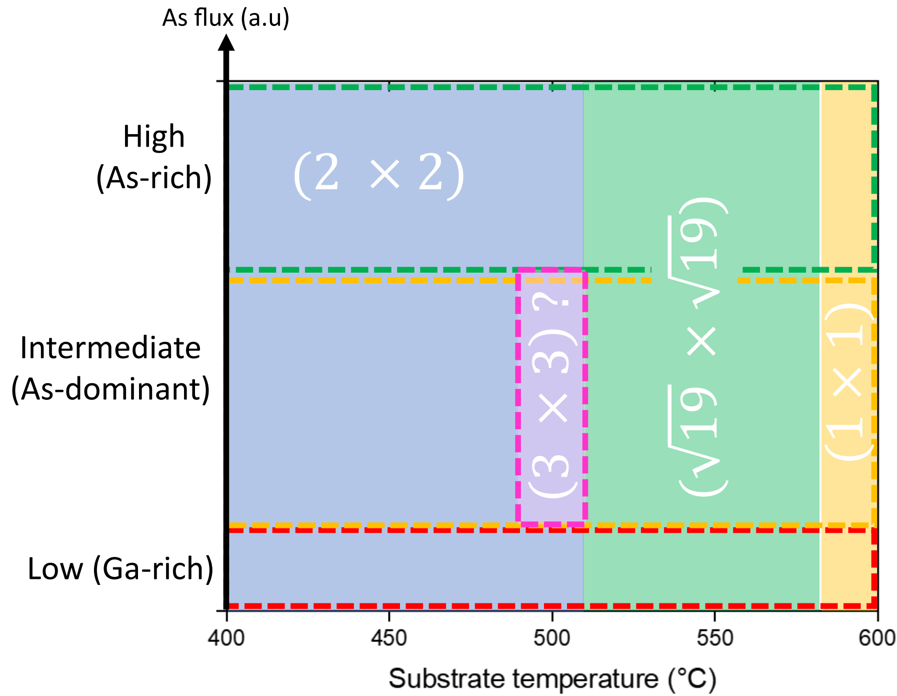


Figure 4.6: Schematic surface reconstruction diagram of the GaAs $(111)_B$ substrates from both experimental and theoretical works.[189,194,195,196]

Conclusion
To conclude this section, the optimized growth conditions for the growth of smooth InSb thin films on GaAs $(111)_B$ were established. Large excess of group V-element (V/III ratio = 136) as well as low growth rate (0.05 **ML**/s) and growth temperature in the 380 – 400 °C range are needed to get a rapid coalescence of the film with only few nanoholes. On top of that, the importance of the underlying surface roughness (and even reconstruction) was underlined in this section, as this parameter strongly influenced the resulting growth of the InSb layer. These results are promising for a smooth transition towards the **SAG** of InSb in-plane **NWs** on GaAs $(111)_B$, as the impact of the observed nanoholes are expected to disappear in the case of **SAG** where the mask apertures limit the growth area to few micrometers.

4.3 STM and STS analysis of InSb 2D heterostructures

As the **SAG** of InSb **NWs** in the previous chapter was performed with a dielectric mask thickness of 30 nm, it is interesting to assess the structure of the InSb (111) surface for a similar layer thickness. Among the three samples having this thickness, **IG2**, **IG3** and **IG5**, we decided to examine in more details sample **IG5**, with the hope to get further insight into the physical reasons causing a partial coverage of the GaAs substrate by the InSb layer. We start this section with a review of the surface reconstructions already observed by **STM** in the literature, before the experimental investigation of sample **IG5** surface, once the native oxide has been removed.

4.3.1 Surface reconstructions of the InSb (111) surface

Through the literature, several studies focused on the surface reconstruction of InSb (111) thin films.[198,199,200,201,202,203] Among the observed reconstructions, two cases were most commonly reported. The first one refers to the Sb-stabilized top surface represented by a (2×2) reconstruction, matching with the **RHEED** observed during the InSb growth. Oppositely, in the case of In-stabilized (Sb-poor) surfaces, the adatoms reorganize into a (3×3) reconstruction. Both reconstructions are illustrated in Figure 4.7.

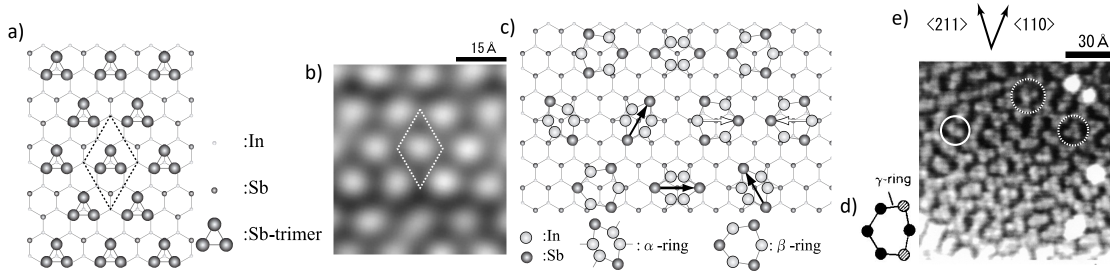


Figure 4.7: a) InSb (111) (2×2) surface reconstruction model. b) A corresponding **STM** image of the InSb (2×2) reconstruction (sample bias V = 1 V, $I_{setpoint}$ = 100 pA). c) Model of the InSb (111) (3×3) surface reconstruction showing both the α and β hexamers. α-rings corresponds to In_4Sb_2 elliptic structure and β-rings exhibit a balanced In_3Sb_3 trigonal structure. d) Schematic of the γ-ring conformation that also consists in In_4Sb_2 hexamers . Extracted from[203]. e) **STM** image of an InSb (111) (3×3) reconstruction with α-rings represented in solid white circle and β rings in dotted line circles (sample bias V = -1.2 V, $I_{setpoint}$ = 100 pA). Extracted from[200].

The (2×2) reconstruction (Figure 4.7a) is characterized by the formation of Sb trimers which are resolved through a single protrusion in the **STM** image (Figure 4.7b), whatever the bias applied to the sample.[199] As to the (3×3) reconstruction, the unit structure adopts several atomic arrangements, all of them consisting of hexamer rings shown in Figures 4.7c and d. The first type, labelled α, presents a higher number of In atoms (4) compared to Sb atoms (2). Hence, this hexamer develops an elliptic conformation that can normally be resolved through two distinct spheres under **STM** scanning (Figure 4.7e). The second one, labeled γ (Figure 4.7d), shows the same proportion of In and Sb atoms, but their arrangement differs. In the hexamer ring, one In atom has substituted to a Sb atom, behaving as an antisite. The third type of rings, β, show a balanced composition between In and Sb atoms (3 of each), allowing a more regular hexagonal arrangement. Specifically, it is distinguished in **STM** by three closely stacked spheres in a triangular fashion (Figure 4.7e). We note that, in the majority of the **STM** works, the α and β rings are visible in the occupied state images and appear as a single protrusions in the empty state images.[204] We note also that bright protrusions were also observed but not identified so far.

When the Sb concentration at the surface is further reduced, a new surface reconstruction develops, though rarely observed. A (3×1) reconstruction was observed by Björkvist *et al.* under specific conditions.[205] This surface reconstruction was obtained after annealing at very high temperature (750 K), close to the melting point of InSb. At these elevated temperature, Sb desorbs quantitatively, leaving the surface uncompensated from this loss. When characterized with **STM**, the (3×1) reconstruction exhibits missing rows of Sb for the first meta-stable structure, while the second one also has an In missing row in the surface double layer.

4.3.2 InSb on GaAs $(111)_B$ surface reconstruction

Sample **IG5** corresponds to 30 nm-thick InSb grown on GaAs $(111)_B$ ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 385 °C, Sb/In = 136). A p-type GaAs substrate (1.5×10^{19} cm^{-3}) was used, because such a high level of doping ensures a steady transfer of charge carriers from the occupied states and into the empty states of the semiconductors in **STM** at 77 K, in particular for heterostructures.[206]

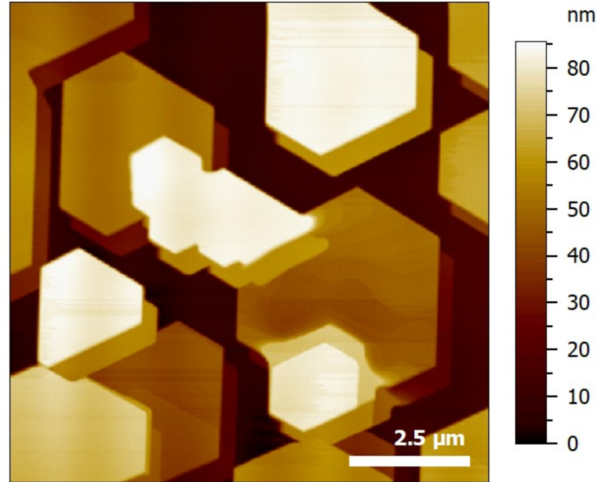


Figure 4.8: **AFM** image of sample **IG5** consisting of a 30 nm-thick InSb layer on GaAs $(111)_B$ ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 385 °C, Sb/In = 136). The **AFM** tip apex was double during scanning, creating this false-stepped structure near the islands edges.

We recall that for sample **IG5**, the surface coverage was found lower than usual with a coverage rate around 70% for InSb on GaAs $(111)_B$ (see Figure 4.8). The morphology resulted in InSb 3D islands with a height reaching 80 – 90 nm at most. This growth behavior is attributed to fluctuations caused by the deoxidation of the GaAs substrate, as a (3×3) **RHEED** was observed prior the InSb growth. Nevertheless, for **STM** experiments, the islands are large enough to avoid any tip crash due to steep terraces.

After the transfer of the sample from the **MBE** to the **LT-STM**, it was outgassed for twelve hours at 120 °C to get rid of residual water. Sample deoxidation was then conducted as detailed in Chapter 2 section 2.3.4 using the ion gun for $\mathbf{H_{AT}}$ exposure. The surface free energy of the InSb {111} surfaces being lower than the {100} surface, the desorption of native oxides requires higher temperatures.[207] As reported in the literature, the use of a $\mathbf{H_{AT}}$ flux during the deoxidation process allows to obtain properly reconstructed surface for an annealing temperature of 350 °C and 60 min of exposure. With further increase in the annealing temperature to 400 °C, decomposition of the InSb (with Sb desorption) may happen which imposes us to consider lower temperatures to avoid this risk.[208,209]

In this regard, a first attempt was done at 300 °C for 1 h 30 without $\mathbf{H_{AT}}$ followed by another 1 h 30 with $\mathbf{H_{AT}}$. This process resulted in a poorly deoxidized surface. The tunneling current was not stable, leading to a low resolution of the surface. Hence, a second attempt was done by increasing the temperature up to 340 °C and exposing the sample to $\mathbf{H_{AT}}$ for 1 h 30 followed by an annealing of 1 h 30 at the same temperature without $\mathbf{H_{AT}}$. Following the second attempt, the tunneling current was much more stable and allowed the acquisition of atomically resolved **STM** images.

We note that an uncertainty of 10 °C exists between the measured temperatures with the thermocouple of the manipulator and the true one of the GaAs substrate. Also, the backside of the sample had still some indium left from the **MBE** growth. Therefore, the mechanical contact with the sample plate was not homogeneous and could account for small local deviations in the temperature.

4.3.3 Atomic surface quality of InSb/GaAs $(111)_B$

As depicted in Figure 4.9a, large-scale **STM** images of the InSb surface shows atomically flat terraces consisting of two layers. For each layer, the magnified **STM** view in the bottom inset reveals the existence of bright protrusions, signature of a reconstructed surface. Based on the height profile aquired across two adjacent layers, both layers are separated by an atomic-step height corresponding to an InSb (111) monolayer ($a\sqrt{3}/3$ = 0.374 nm). Therefore, the pits are not deep, but their presence departs from the absence of pits on the oxidized InSb surface imaged with **AFM** (Figures 4.3, 4.5 and 4.8). We attribute this slight change of the surface morphology to the desorption of the native oxide layer with $\mathbf{H_{AT}}$ which involves the loss of Sb and In species from the surface. This result is consistent with previous **STM** studies performed on the InSb (001) surface and on the sidewalls of deoxidized InAs **NWs** grown by the **VLS** mechanism.[210,211,212,213] The hydrogen cleaning is successful to desorb the oxide species. However the temperature of 340 °C, slightly above the congruent evaporation temperature of InSb, leads to the preferential evaporation of Sb, which might result in an atomic rearrangement at the surface and the formation of pits of one monolayer depth.

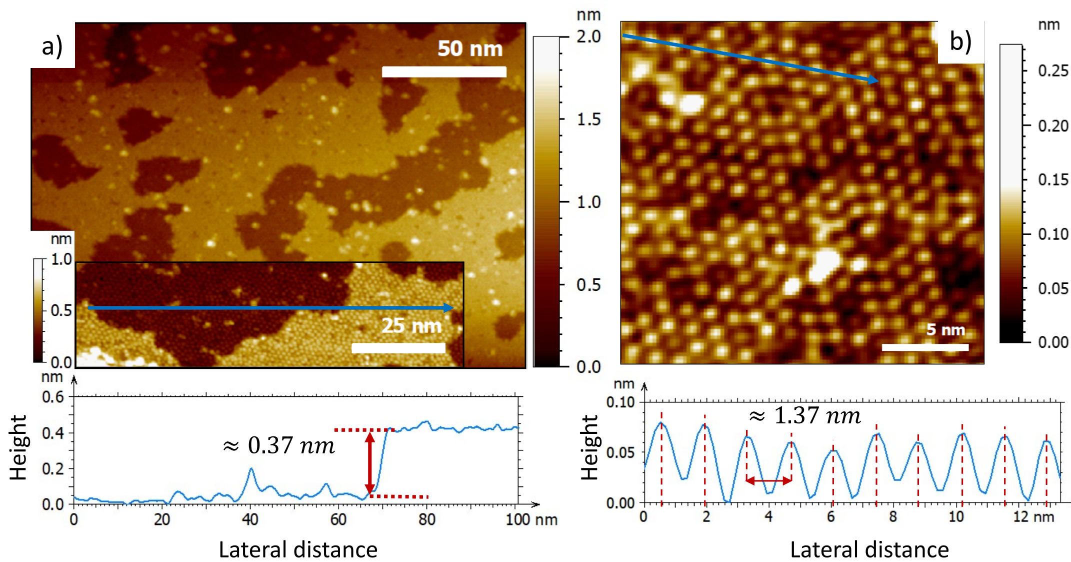


Figure 4.9: a) **STM** image of 30 nm InSb on GaAs $(111)_B$ (sample bias V = -2 V, $I_{setpoint}$ = 10 pA). Inset: Zoom-in (neighboring area) with a stepheight profile along the blue arrow (sample bias V = -2 V, $I_{setpoint}$ = 50 pA). b) Atomically-resolved **STM** image of the InSb (111) (3×3) surface reconstruction. Blue arrow shows the surface periodicity as indicated below in the line profile (sample bias V = -2 V, $I_{setpoint}$ = 10 pA).

To further elaborate on this hypothesis, a smaller area of the surface was observed (Figure 4.9b. At first glance, the InSb surface shows a relatively ordered reconstruction. Still, several defects ("darker areas") and disordered regions are visible here and there. Checking the periodicity of the bright protrusion, either through the profile (blue arrow) or the analysis of the **Fast-Fourier**

Transform (FFT) image, the measurement yields a lattice with a periodicity of 1.37 nm, which matches the (3×3) InSb reconstruction ($3a/\sqrt{2} = 1.374$ nm). Hence, the InSb surface preparation to remove the native oxide clearly turned the (2×2) Sb-rich surface obtained during **MBE** into a (3×3) In-rich reconstruction, as a result of the Sb desorption forcing the InSb surface to adopt a reconstruction involving a smaller amount of Sb atoms.

Further observation of the InSb surface on another area of the sample revealed new interesting features. The first features appear as faint trimers, spread between the bright protrusions. Some of them are highlighted by the blue rectangle of Figure 4.10a. They show two orientations and look similar to the ones observed in section 4.3.1. We assign these trigonal features to β-rings from the InSb (3×3) reconstruction which are consistent with similar observation from Inada *et al.*[200], as highlighted in Figure 4.7e (dotted circles). The β-rings have an equal number of group III and V atoms, yielding In_3Sb_3 clusters.

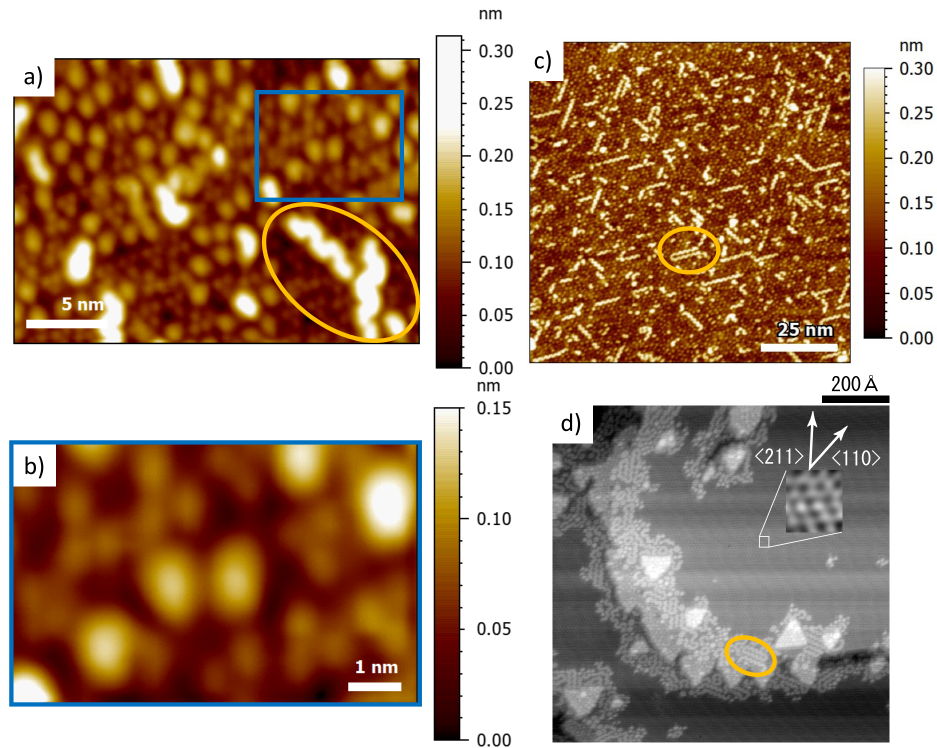


Figure 4.10: a) High-resolution **STM** image showing off the various features (In-chains in the yellow ellipse, β-rings in the blue box) (sample bias V = -2 V, $I_{setpoint}$ = 50 pA). b) Zoom-in from the blue rectangle in a), the trigonal structure of the β-rings are visible. c) **STM** image collected in another region of the sample (sample bias V = -2 V, $I_{setpoint}$ = 50 pA). The yellow ellipse shows an In-chain. d) **STM** image of the InSb (111) (2×2) surface after depositing 0.2 **ML** of In at 200 °C (sample bias V = -2 V, $I_{setpoint}$ = 100 pA) for comparison.[200] In-chains are highlighted in the yellow ellipse.

The filled state images of Figure 4.10 allows to probe the three Sb atoms in each cluster. They appear with a lower contrast than the single protrusion and depending on the tip can be more or less resolved. For example, in Figure 4.10b, darkers protrusions are visible and we believe that they correspond to Sb trimers. We note that their concentration varies depending on the area which is scanned. Based on the more or less well resolved observation of the trimers,

we speculate that the bright protrusions, which show the highest concentration in Figure 4.9b, correspond to In and Sb clusters with two or a single Sb atom, signature again of the desorption of Sb atoms from the surface during the preparation. As mentioned above, the α rings contain two Sb atoms. As these atoms are positioned diametrically opposite each other in the cluster, they should be individually resolved in the occupied state images of Figure 4.10a, which is not the case. Therefore, we suspect the rings to be made of a γ structure. For this structure, highlighted in Figure 4.7d, an In atom has substituted a Sb atom. As mentioned above, this In atom behaves as an antisite, which might cause a change of the **LDOS** close to the Fermi level. It could account for the observation of a single protrusion in the cluster at both positive and negative bias.[198] The high concentration of γ-rings, signature of a lower amount of Sb atoms with respect to the β-rings, agrees with a significant desorption of the Sb atoms during the deoxidation of the surface.

The second main features, which are not visible in Figure 4.9, but seen in other areas of the same sample, correspond to "zig-zag"-like chains, consisting of very bright protrusions topping the InSb surface. These chains are clearly seen in Figures 4.10a and c. They show three orientations, which are aligned with the $[\bar{1}10]$, $[\bar{1}01]$ and $[0\bar{1}1]$ symmetry axis of the InSb (111) plane. Based on the work of Inada *et al.*[200], where the authors deposited up to 0.7 **ML** of In at 200 °C on the InSb (111) (2×2) surface and noticed such In segments after 0.2 **ML** deposition (see Figure 4.10d), we attribute the zig-zag chains to the self-assembly of In adatoms. In the context of our study, the occurrence of In-chains attests again the preferential Sb desorption from the surface, which can be strong in some areas of the wafer and might lead to the ordered arrangement of the In atoms on the surface.

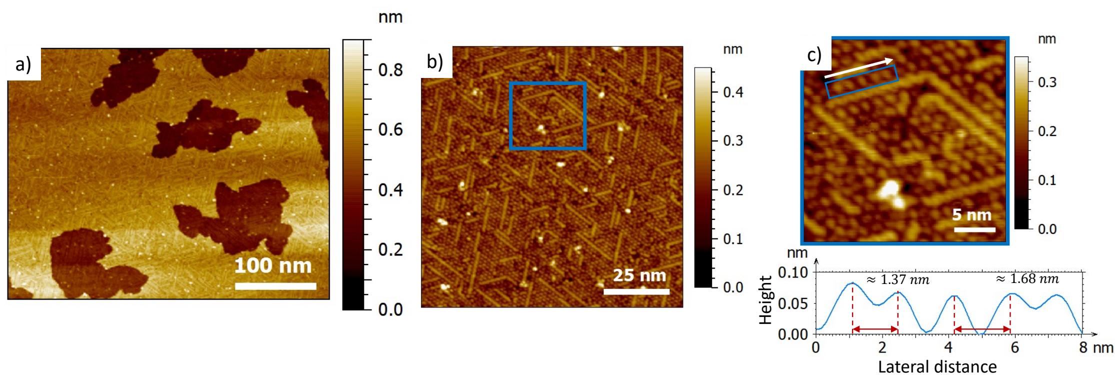


Figure 4.11: a) **STM** image of the sample in the edge area (sample bias V = 2 V, $I_{setpoint}$ = 5 pA). b) **STM** image at smaller scale showing off the InSb (111) (3×3) surface reconstruction as well as disordered regions and defects (darker areas) (sample bias V = 2 V, $I_{setpoint}$ = 5 pA). c) Zoom-in on the blue rectangle from b) highlighting a deviation of the (3×3) periodicity in the line scan profile below.

Finally, Figure 4.11 shows **STM** images obtained at the edge of the sample. The surface reconstruction also presents atomically-high pits in the top InSb layer (Figure 4.11a). At smaller scale, In-chains longer than the ones seen in Figure 4.10 are visible with a higher density (Figure 4.11b). A new type of defect is also detected as highlighted in the blue squared region in Figure 4.11c. The line profile acquired along the axis of the rectangle shows a clear local disruption in the periodicity: the usual value of 1.37 nm for the (3×3) reconstruction is here increased to 1.68 nm. This interval suggests that the second layer is also affected by the shortage of Sb atoms due to their preferential desorption.

To end this section, this comparison of the structures observed in the middle of the sample and at the edge highlights the influence of the temperature on the sample preparation. Here, the increased length of In-chains and the increase in their density as well as the higher disorder in the arrangement of bright protrusions suggest a much larger Sb desorption from the surface. This observation stays consistent with the increased annealing temperature on the edge of the sample which arises from the clamping setup. At this location, the temperature is locally higher than in the central area that is away from this point of contact (but no clear ΔT could be estimated). A higher temperature causes a more pronounced loss of Sb which leads to a stronger defects-induced local disorder.

Conclusion

To conclude this section, a structural analysis using **STM** was performed on a 30 nm-thick InSb thin film on GaAs $(111)_B$. The InSb surface reconstruction corresponds to a (3×3) periodicity which was different from the Sb-rich (2×2) **RHEED** observed during InSb growth. This change was deduced to arise from the sample preparation process for **STM** that led to important Sb desorption. The loss of Sb will automatically lead to a higher disorder on the surface that results from the induced defects. Consequently, the electronic states of the surface will be impacted, so as the transport properties that are affected by surface states. Hence, a careful control in the oxide desorption process or a capping layer is needed to guarantee the InSb surface integrity and maximize the electron transport inside the layer.

4.4 InSb NWs on GaAs $(111)_B$

In this final section, the **SAG** of InSb on GaAs $(111)_B$ is detailed. The 2D growth of InSb on GaAs $(111)_B$ presented in the first section has produced smooth InSb surfaces with a low density of nanoholes (coverage rate of 97 %) when the thickness of the InSb layer was 30 nm. Due to the important lattice mismatch between both materials (f = 14.6 %), the rapid plastic relaxation of the InSb layer under optimized growth conditions allowed to relieve the strain and avoided the formation of a high density of 3D islands. Starting from the same growth conditions, *i.e.* a low $\mathbf{V_G}$ of 0.05 **ML**/s, a high Sb/In ratio (136) and $\mathbf{T_G}$ in the 380 – 400 °C range, in-plane InSb **NWs** were prepared by **SAG**. Again, different growth conditions were selected and are referred in Table 4.2.

Sample	**SIG1**	**SIG2***	**SIG3***	**SIG4***
$\mathbf{V_G}$ (ML/s)	0.05	0.05	0.05	0.05
Sb/In ratio	136	136	136	136
$\mathbf{T_G}$ (°C)	380	380	390	390
$t_{nominal}$ (nm)	30	50	50	100
Mask layout	2	3	3	3
Supplier	AxT	AxT	AxT	AxT

Table 4.2: **SAG** conditions for the deposition of InSb on patterned GaAs $(111)_B$ substrates. When the label is indicated with a *, it means the mask B process was used, which consists of an Al_2O_3/SiO_2 double dielectric layer. The details of the mask layout are found in appendix A.

Sample **SIG1** was fabricated using mask A process, with a single layer of SiO_2 (30 nm), while all the remaining ones were patterned with the mask B process, consisting of a stack of Al_2O_3 (5 nm)/SiO_2 (30 nm) as detailed in Chapter 2 section 2.2.4. This mainly impacts the depth of the patterns (about 35 nm for mask B against 15 nm for mask A), the lateral profile of the pattern (straight for mask B and rounded for mask A) and the minimum pattern width achievable. Moreover, two different mask layouts (geometrical shapes and nanostructures) were employed and further detailed in the appendix A. A $\mathbf{H_{AT}}$ flux generated by the RF plasma cell was used for all samples during the **SAG** to enhance selectivity.[19,137]

Various nanostructures were designed, depending on the mask layout, to assess the impact of crystal orientation, aperture width and pitch size. For example, considering Figure A.2a the layout comprises various geometries such as **NWs**, nanocrosses, nanogrids or sun-shapes. The arrays of **NWs** are of particular interest. As depicted in Figure A.2b, they consist of **NWs** with different aperture widths grouped by sets of four **NWs**. From the widest to the narrowest groups, the width corresponds to: 1 µm, 500, 200, 100, 50 nm for a total of 20 **NWs** per array. The pitch size varies accordingly: 1 µm, 500, 300, 400, 450 nm (from the widest to the narrowest **NWs**). The length of all the **NWs** is 20 µm. The arrays are duplicated from 0 to 90° every 30° to assess the impact of the crystallographic orientation as well.

The second important geometry refers to the sun-shape structure. Visible at magnified view in Figure A.1d, it consists of a 10 µm-long **NW** duplicated every 10° to form a 360° sun-shape and cover different crystallographic orientations. On this mask, this sun-shape is reproduced for three different apertures widths. From top to bottom: 500, 200, 100 nm.

Moving onto the mask layout 3 of Figure A.3a fewer and new geometries were designed. In Figures A.3d and e, the patterns consist of **NWs** duplicated this time every 30° to complete a 360° rotation. The **NWs** length is 10 µm and the aperture width ranges from 30 nm (at most left in Figure A.3b) to 100 nm (at most right, presented in Figure A.3d).

The second version of the sun-shape illustrated in Figure A.3e and f consists this time of an array of 16 **NWs** of various aperture widths grouped by sets of 4 **NWs**. From left to the right the aperture width corresponds to a nominal value of: 30, 40, 50, 100 nm. This array is then duplicated every 30° to form a 360° sun-shape covering the different crystallographic orientations.

Eventually, the last considered structure is simply an array of 11 **NWs** with a length of 10 µm. Their aperture width also varies depending on their position on the mask layout as seen in Figure A.3b. The magnified view in Figure A.3c highlights the array of 100 nm-wide **NWs**. This structure is duplicated from 0 to 90° every 30° as well.

4.4.1 Morphological study

Not only the selectivity but also the **NWs** morphology are evaluated through this study. For that purpose, we use the various geometrical shapes with different aperture widths, pitches and crystallographic orientations designed on the two mask layouts as described in the previous section 4.4.

Sample **SIG1** was grown in the low temperature range (380 °C) of the aforementioned optimized growth conditions listed in Table 4.2. Figure 4.12a shows a large-scale **SEM** view of the layout cell. All the patterns appear darker than the dielectric mask. The sun-shape structure and **NWs** highlighted in the color boxes are the most useful designs to rapidly evaluate the morphology.

As shown in Figure 4.12b, the 500 nm-wide sun-shape illustrates the formation of smooth planar **NWs** that grew inside the openings. The absence of nucleation on the mask is the sign

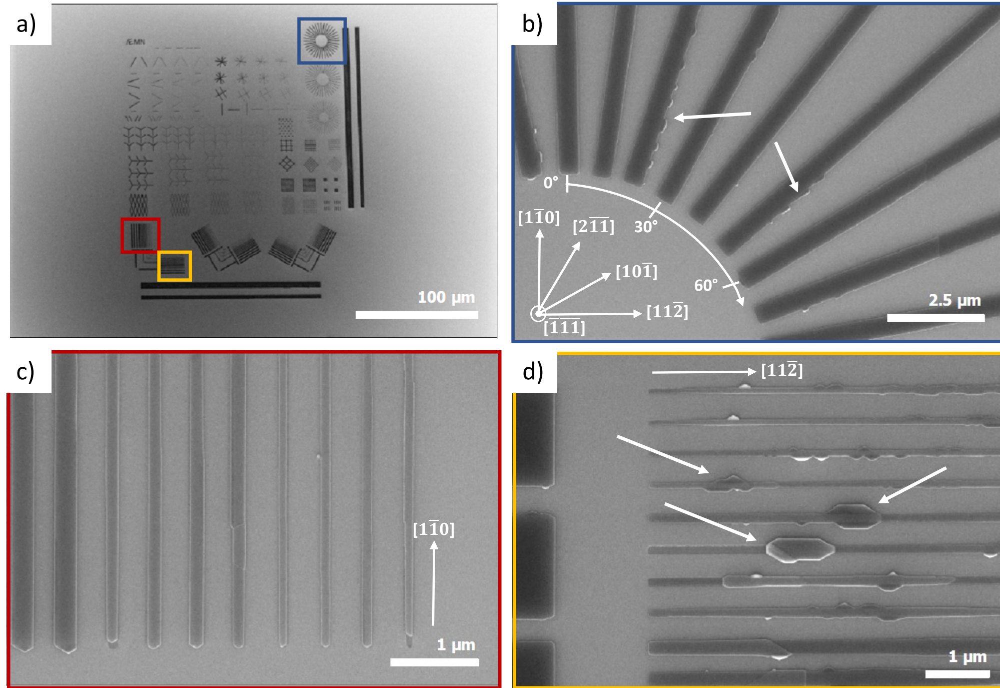


Figure 4.12: **SEM** images of sample **SIG1**, corresponding to the **SAG** of 30 nm-thick InSb nanostructures on GaAs $(111)_B$. a) Large scale view of the mask layout with different geometric patterns. The sun-shape in the blue box and two-differently oriented **NWs** array in the red and yellow boxes are highlighted. b) Zoomed-in view on the sun-shape pattern seen in the blue box in a). The nominal aperture width is 500 nm and the pattern is repeated every 10° clockwise to assess the impact of the crystal orientation. c) $[1\bar{1}0]$-oriented **NWs** of different nominal width (grouped by four). From left to right widths of 200, 100 and 50 nm. d) Similar pattern oriented along the $[11\bar{2}]$ direction. Aperture widths of 50, 100 and 200 nm shown from top to bottom.

of a high selectivity for the growth. From the closer examination of the **NW** edges, which sometimes exhibit zigzag and appear bright, we notice that the roughness of the **NW** edges varies with the in-plane orientation of the apertures. The edges are rather straight along the two main crystallographic orientation $[1\bar{1}0]$ and $[11\bar{2}]$ as well as their equivalent directions which are found every 60° (because of the six-fold rotational symmetry of the **ZB** (111) surface). In contrast, between these main directions, the edges of the **NWs** are less straight and exhibit a lateral overgrowth on the mask as pointed out by the white arrows. This is a direct consequence of the low energy facets that cannot form easily along these directions.[214] As reported by Lee *et al.*[215] on InAs in-plane **NWs** on InP $(111)_B$ substrates, the <$11\bar{2}$> **NWs** have two vertical $\{1\bar{1}0\}$ facets while <$1\bar{1}0$> **NWs** usually generates a vertical $\{11\bar{2}\}$ facet and a slanted $\{\bar{1}00\}$ facet.

The **NWs** presented in Figure 4.12c are all smooth independently of the different aperture widths. As they were grown along the $[1\bar{1}0]$ direction, this result is consistent with the one observed for the sun-shape pattern. We note a similar contrast for all the **NWs**, signature of a good homogeneity in their morphology. This result is in contrast with the $[11\bar{2}]$-oriented **NWs** observed in Figure 4.12d. Although their edges were found similar to the $[1\bar{1}0]$-oriented **NWs** in the sun-shape pattern with large apertures, it is clear that their growth inside narrow apertures gives rise to a lower uniformity, with either lateral overgrowth or clipping along the **NWs**.

4.4.1.1 Influence of the growth temperature,thickness and mask design

For samples **SIG2**, **SIG3** and **SIG4**, the mask layout 3 was used. It included the design of patterns for cross-sectional **STEM** analysis, that required **FIB** lamellae preparation. Figure 4.13 shows **SEM** images of InSb nanostructures obtained for the three samples. As referred in the Table 4.2, the growth conditions were slightly modified between the samples: a change of 10 °C of $\mathbf{T_G}$ was tested (sample **SIG2**) or the InSb nominal thickness was increased from 50 to 100 nm (sample **SIG4**). We first consider the sun-shape pattern of Figure 4.13. In this pattern, each **NWs** array is then duplicated and rotated every 30° to assess the impact of the crystallographic orientation as well.

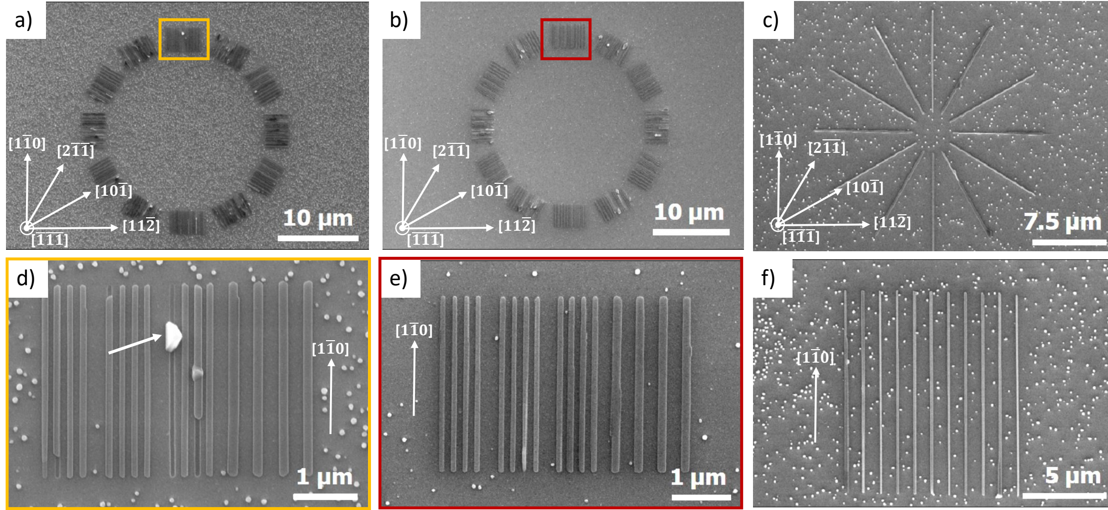


Figure 4.13: **SEM** image of sun-shape patterns designed on sample a) **SIG2**, b) **SIG3** and c) **SIG4**. This dense type of sun-shape consists of an array of 3-µm long **NWs** divided into 4 sets of different apertures widths (from left to right to 30, 40, 50 and 100 nm). d) and e) Zoomed-in view of the yellow and red rectangles in a) and b) illustrating the 3 µm-long **NWs** array of various aperture widths. f) Array of 10 µm-long [1$\bar{1}$0]-oriented **NWs** with a width of 100 nm grown on sample **SIG4**.

At first, a clear difference in the selectivity rate is seen when switching to the mask B process (Al_2O_3/SiO_2 bi-layer) for sample **SIG2** which exhibits significant parasitic nucleation (Figure 4.13a) compared to the sample **SIG1** that uses mask A with SiO_2 only (Figure 4.12c). By increasing the growth temperature in sample **SIG3**, the selectivity slightly increases as seen in Figure 4.13b. Nevertheless, the decrease in selectivity observed using the mask B indicates a narrowing of the selectivity window in terms of growth temperatures. The thermal resistance (R_{th}) of both masks can be evaluated through the simple equation

$$R_{th} = \frac{t}{k} \tag{4.1}$$

where t is the thickness of the dielectric layer and k is the thermal conductivity (SiO_2: 1.06 $W.m^{-1}.K^{-1}$ and Al_2O_3 1.25 $W.m^{-1}.K^{-1}$ at 300 K[216,217,218]). Assuming a thickness of 15 nm for the SiO_2 in mask A and 30 nm of SiO_2 on top of 5 nm of Al_2O_3 for mask B, we get a $R_B/R_A \approx 2.28$. Then, we can evaluate the temperature drop ΔT caused by the change in thermal resistance from mask A to mask B process through the equation below

$$\Delta T = (R_B - R_A) \times \phi \tag{4.2}$$

where the radiative heat flow is expressed as $\phi = \sigma \times \epsilon \times T^4$ (σ the Stefan-Boltzmann constant equals 5.6704×10^{-8} W.m^{-2}.K^{-4}, ϵ the emissivity of the material set to 0.7 in our experiments for GaAs substrates and T the growth temperature of 390 °C). After calculation, the temperature drop ΔT equals 1.4×10^{-4} K which means no impact should be expected on the selectivity due to the thermal resistance change for mask B.

In this regard, we suggest that the increased roughness of the SiO_2 layer on top of Al_2O_3 without any HF treatment (chapter 2 Section 2.2.5) in the mask B process is responsible of the higher nucleation probability on the mask, hence reducing the selectivity.

Now comparing **SIG3** with **SIG4**, a higher density of clusters on the SiO_2 surface between the **NWs** is seen for the last sample. It corresponds to a thicker InSb layer (100 nm vs. 50 nm). This increased nucleation on the mask is simply due to the longer **SAG** time. Still, in comparison with sample **SIG1**, observed in Figure 4.12, the selectivity obtained with the mask B process here is degraded, which confirms that the mask roughness can deeply influence the growth kinetics.

With regard to the crystallographic orientation dependency, the $[1\bar{1}0]$-oriented **NWs** shown in Figures 4.13d and e are smooth. Although they overgrow slightly on the mask, as seen in Figure 4.13d, in most cases their shape remains straight. Conversely, the $[11\bar{2}]$-oriented **NWs** generally present a more significant lateral overgrowth. Even though not illustrated at a smaller scale, the horizontal $[11\bar{2}]$-oriented **NWs** in Figures 4.13a and b predominantly appear either disrupted or with random lateral overgrowth on the mask making their top facet not flat anymore. This phenomenon is visible on all the duplicated arrays of the same $<11\bar{2}>$ family (every 60°), which supports the fact that a better morphology is found for $[1\bar{1}0]$-oriented **NWs**.

Nevertheless, as highlighted in Figure 4.13d, in some cases for the $[1\bar{1}0]$ **NWs**, a single 3D InSb island can be observed with no growth in the remaining part of the aperture while the neighbouring openings are completely filled with smooth **NWs**. Even though this event was rarely observed, this example suggests that an underlying defect in the aperture, or a local variation of the surface roughness prevents the InSb 2D growth mode to take place.

The best accomplishment in this section is visualized in Figure 4.13f where 10 µm-long $[1\bar{1}0]$ in-plane InSb **NWs** on GaAs $(111)_B$ were achieved with a high structural quality and without any disruption, albeit to a smaller selectivity.

4.4.2 STEM cross-sectional analysis

To get a deeper insight into the InSb growth in the aperture and investigate the **NW** morphology as well as the interface with the GaAs substrate, a **FIB** lamella was prepared from sample **SIG3**. $[0\bar{1}1]$-oriented **NWs** were cut along the $[\bar{2}11]$ direction to image their cross section with **STEM**. In addition, an **Energy-dispersive X-ray Spectroscopy (EDX)** analysis was performed to establish a compositional study of the **NWs**. As presented in Figure 4.14a, two **NWs** of different nominal aperture widths of 100 nm (Figure 4.14b) and 50 nm (Figure 4.14c) respectively have been investigated.

At first glance, both **NWs** exhibit a flat top surface with good lateral confinement guided by the vertical dielectric sidewalls from mask B. No significant mask overgrowth is observed, though a small variation of the width along the growth axis. For the 100 nm aperture in Figure 4.14b, the **NW** width near the interface varies from 147 nm (line profile 1) to 139 nm (line profile 2) before increasing again to 155 nm once InSb reaches the mask surface (line profile 3). In the case of the 50 nm-wide aperture, the same trend is visible with the following evolution of the **NW** width (from line profile 1, 2 and 3 respectively): it starts from 92 nm, narrows up to 86 nm and then increases to 99 nm. Based on these values, the real aperture width turns out to be significantly larger than the nominal value (~140 nm vs. 100 nm and ~90 nm vs. 50 nm). This

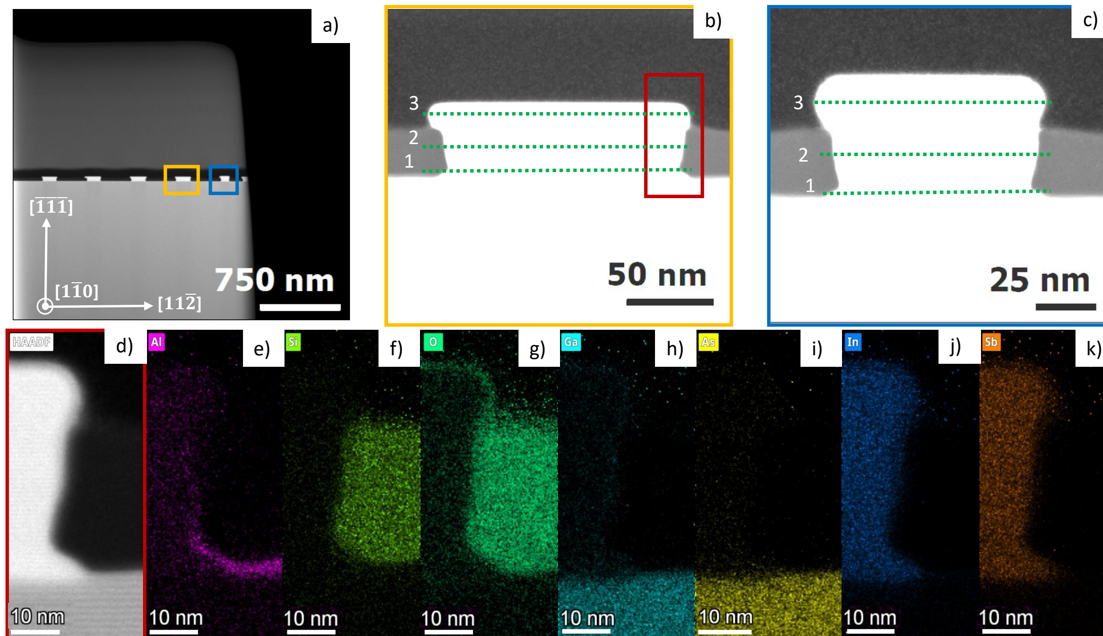


Figure 4.14: **STEM** images of sample **SIG3** at a) large scale, b) and c) smaller scales performed onto a 100 nm wide **NW** and a 50 nm wide **NW**. The contrast was adjusted such that the Al_2O_3/SiO_2 mask surface is visible (light grey contrasted). The green lines labeled 1, 2, 3 correspond to line profiles evaluating the experimental width of the **NWs** at different vertical positions. d) **HAADF**-**STEM** image of the **NW** edge as per the red box in b). Related **EDX** maps of the different chemical element with e) Al (purple) f) Si (light green), g) O (green), h) Ga (light blue), i) As (yellow), j) In (blue) and k) Sb (orange).

variation is probably a result of a too large e-beam dose. Indeed, the distance between the **NWs** may have an impact on the real received dose during exposure. With a short separation, the actual dose, due to the small pitch between the pattern, would be larger than the set value.

A new effect, caused by the introduction of the Al_2O_3 layer in mask B is revealed: an underetching of the Al_2O_3 layer occurred and led to the wider InSb basis seen in the **STEM** image. This result is supported by the Al map acquired with **EDX** spectroscopy which also suggests that the Al_2O_3 had been lifted up near the **NW** edges (Figure 4.14d). This small recess in the mask arises from the AZ400K wet etch. In contrast, the SiO_2 sidewalls are rather vertical (Figures 4.14f and g). The examination of the O-content profile also shows a residual oxidation of the InSb **NW** from air exposure in the emerging part. Eventually, a quite abrupt chemical interface between the GaAs substrate and InSb can be deduced from Figures 4.14h, i, j and k.

Focusing on the interface region of the wider **NW** (Figure 4.15a), the high resolution image reveals the presence of planar defects (Figure 4.15b). The first type of defects is observed above the interface, which is defined by the contrast change from dark (GaAs) to bright (InSb). These defects correspond to **SF**s in the InSb layer (pointed by red arrows in Figure 4.15b). Although a change of the lattice orientation is observed in the **STEM** image when the **SF**s occur, the **SF**s are better resolved in the inverse **FFT** obtained from the filtered **FFT** image through the horizontal dark lines which propagate across the width of the **NW** (Figure 4.15d). No other **SF**s are observed along the remaining upper part of the **NW**. This is interesting to notice that the few **SF**s are lying just above the mismatched interface and are connected laterally to the sidewalls in the narrowest part of the mask opening.

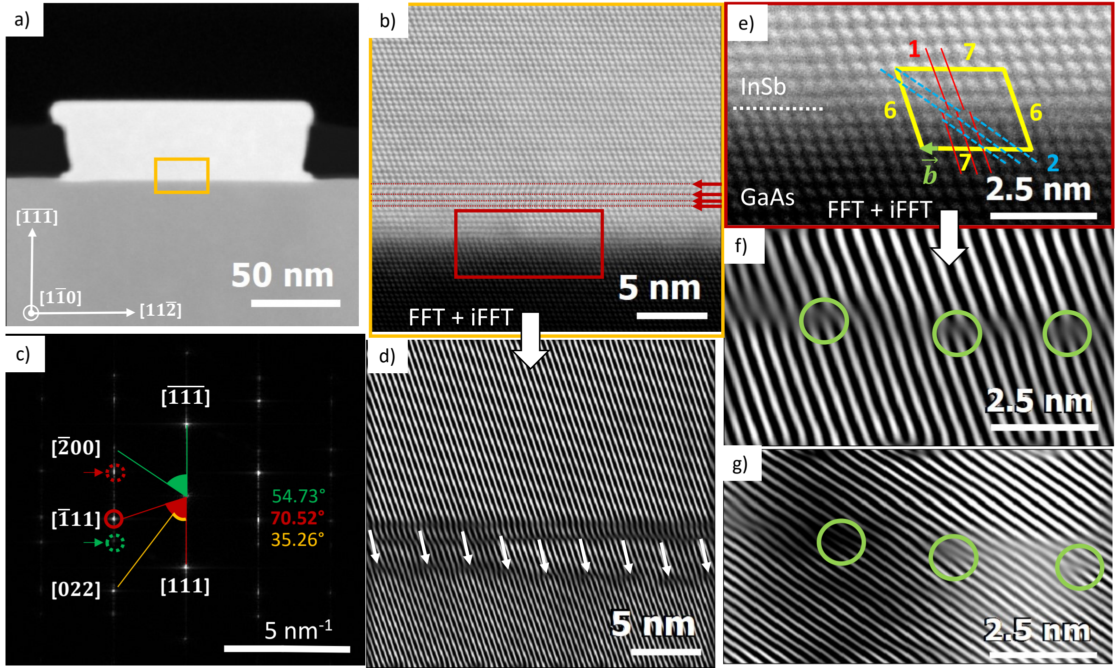


Figure 4.15: **STEM** images of sample **SIG3**. a) Large view on a 100 nm-wide InSb **NW**. b) Magnified view of the central region highlighted in yellow in a). Red-dotted lines and arrows show **SF**s. c) **FFT** of an InSb region from b). The angles between the main crystallographic directions are reported for information. The dotted red and green circles corresponds to the **SF**s "mirrored" contribution. d) Inverse-**FFT** image of b) after a g = $[\bar{1}11]$ filtering of the **FFT** image. White arrows show the periodic **MD** network while twinned regions appear dark contrasted. e) InSb/GaAs interfacial region from the red box in b). The yellow lines help determining the Burgers vector. The red and blue lines shows the atomic columns along two different filtering planes. f) Inverse-**FFT** of the **FFT** image of e) after a g = $[\bar{1}11]$ filtering that corresponds to the red lines "1" in e). g) Inverse-**FFT** of the **FFT** image of e) after a g = [022] filtering which refers to the blue lines "2" in e). The green circles highlight dislocations at the InSb/GaAs interface.

Regarding the InSb/GaAs interface, as anticipated from the large lattice mismatch (f = 14.6 %), a clear **Misfit Dislocation (MD)** network can be seen in Figure 4.15d at the positions pointed by the white arrows. To outline it, the **FFT** image of Figure 4.15b, which is shown in Figure 4.15c is filtered for specific g-vectors. From the $[\bar{1}11]$ net planes filtered image (Figure 4.15d), the dislocations show a 2.9 nm periodicity along $[11\bar{2}]$. This is consistent with the 2.7 nm expected value using the formula from Babkevich *et al.*[219]:

$$D = \frac{\sqrt{3} a_{InSb} a_{GaAs}}{\sqrt{8}(a_{InSb} - a_{GaAs})} \tag{4.3}$$

At smaller scale in the interfacial region from Figure 4.15e, the Burger circuit drawn through the yellow lines does not form a closed loop, confirming the existence of the dislocations. Depending on the net plane used for filtering, different atomic columns will be considered in the image which results in a different tilt angle but the same dislocations are observed. Nevertheless, the difference in the periodicity (2.9 nm vs. 2.7 nm) observed confirms that a residual stress is still present, which cannot be elastically relaxed due to the mask sidewalls in the apertures. Hence, the resulting **SF**s in the InSb layer can originate from the residual plastic relaxation of

the mismatch.

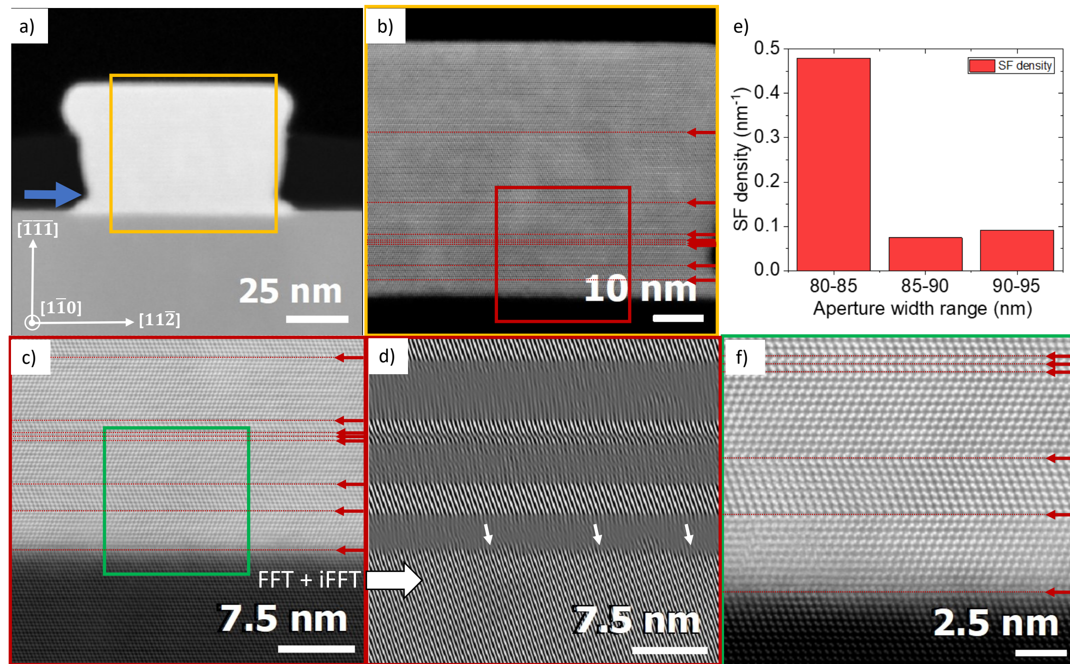


Figure 4.16: **STEM** images of sample **SIG3**. a) Large view on the 50 nm-wide **NW**. The blue arrow points towards the bottleneck region. b) Lower scale image of the central region in yellow box from a). Red-dotted lines and arrows show **SF**s. c) Further scaling down near the interface region obtained from the red box in b). d) Reconstructed surface by g=[$\bar{1}$11] **FFT** filtering and **iFFT**. White arrows show the periodic **MD** network while twinned regions appear dark contrasted. e) Graph of the **SF** density per unit of length according to the aperture width (set by ranges). f) Zoom on the inferfacial region from the green box in c).

For the narrower **NW** seen in Figure 4.16a (50 nm nominal width), the **SF** density appears to be denser a bit further from the mismatched interface as evidenced through the successive zoomed-in views shown in Figures 4.16b, c and f (marked by the red arrows). At the interface with GaAs, the first InSb atomic plane immediately forms a twin. The layer then remains stable on successive atomic planes before another twin changes the stacking back again. In the upper part of Figure 4.16f, successive **SF**s are observed every InSb atomic layer. Looking at the lower part of Figure 4.16b, these successive **SF**s are located near the bottleneck region (pointed by the blue arrow in Figure 4.16a), where the aperture width is the narrowest. These observations are consistent with a similar behavior for the wider **NW** as seen in Figure 4.15b. Additionally, if we consider the last **SF** located at the uppermost region of the **NW** in Figure 4.16b, this defect also aligns well with the SiO_2 mask surface, where the sidewalls of the **NW** change and get no longer confined inside the aperture.

By calculating the average **SF** density per unit of length according to the aperture width for this **NW**, it is clearly seen that a higher density is found for the lower aperture width (Figure 4.16e), that is to say, in the bottleneck region where the sidewalls angle varies quickly. The local strain accumulated from this geometrical confinement seems immediately relieved through a **SF**, which has a low-energetic cost for the <111> close-packed plane family. From these observations, we thus believe that the **SF** density is correlated with the sidewalls of the **NW** and more precisely to their abrupt angle variation.

With regards to lattice-mismatch accommodation, a periodic **MD** network is found at the InSb/GaAs interface for this narrower **NW** as well. Some dislocations are pointed out by the white arrows in Figure 4.16d. Although we have an intermediate **SF** just above the interface that blurs the **FFT**-filtered image, a mean dislocation spacing can be estimated as well, which is consistent with the value determined for the wider **NW**. Then, by comparing the mean spacing between two fringes inside the InSb layer to the mean spacing inside GaAs, the difference gives a lattice mismatch of 13.6 % which would corresponds to a 93 % relaxation of the InSb layer. This suggests that, thanks to the **MD** network at the interface, most of the mismatch is already accommodated after the first twinned region inside InSb, which allows to get a smooth subsequent growth of the **NW**.

4.5 Conclusion

Throughout this chapter, the successful growth of both smooth InSb thin films and in-plane **NWs** on GaAs $(111)_B$ substrates was achieved under optimized growth conditions ($\mathbf{T_G}$ around 390 °C, $\mathbf{V_G}$ = 0.05 **ML**/s, Sb/In = 136). The quality of the InSb thin films depends on the GaAs surface roughness after deoxidation that affects In and Sb diffusion lengths.

Through the **STM** analysis of InSb (111) surfaces, a (3×3) reconstruction was observed which arises from the sample preparation process that led to important Sb desorption. These observations highlight the importance of controlling the surface state of the InSb nanostructures as it will degrade their transport properties. To maximize the electron transport and ensure the integrity of the layer, a careful control of the InSb surface or a passivation layer is needed.

The InSb in-plane **NWs** grown on GaAs $(111)_B$ exhibited a crystallographic orientation dependency where larger lateral overgrowth and coalescence issues were observed for $[11\bar{2}]$-oriented **NWs**, while this phenomenon was rarely evidenced for $[1\bar{1}0]$-oriented ones. In both cases, the large Sb/In ratio, low growth rate and higher growth temperature (~390 °C) help to get a rapid coalescence of the InSb layer. Through a **STEM** cross-sectional analysis, a periodic **MD** network is observed at the InSb/GaAs interface, that arises from the extreme lattice mismatch (f = 14.6 %). This **MD** network allows a quasi-full relaxation of the InSb layer (93 %), which can grow smoothly under the optimized conditions. Eventually, twinning is also observed along the thickness of the InSb **NWs** but the density of **SF**s seems to be correlated with the aperture sidewalls.

In summary, the successful growth of InSb in-plane **NWs** on GaAs $(111)_B$ with lengths up to 10 µm is promising as it shows that despite a large lattice-mismatch, a smooth morphology can be obtained. Nevertheless, knowing the existence of defects at the interface through the **MD** network, the electron transport properties may probably be affected. Now, in our quest to tune the conductance of the in-plane **NWs**, the addition of a semiconducting potential barrier between the GaAs substrate and InSb can be contemplated. Therefore, the next chapter will be devoted to the investigation of the semiconducting potential barrier thin film growth and the subsequent InSb **SAG** on top of this layer.

Chapter 5

MBE growth of InSb thin films and in-plane NWs on a doped GaAs $(111)_B$ substrate with a semiconducting barrier

5.1 Introduction

As proposed in Chapter 1, the introduction of a potential barrier between GaAs and InSb could enable an electrostatic modulation of the charge carrier density in the InSb layer by applying a bias on the doped GaAs substrate. The choice of the material for the potential barrier is guided by the band offsets and the lattice mismatch with the substrate in order to limit the strain relaxation mechanisms involved in the epitaxial process.

The Chapter 4 showed that InSb thin films and in-plane **NWs** can be achieved on mismatched GaAs $(111)_B$ substrate with a smooth morphology and high structural quality under specific growth conditions. From this result, we considered the two different III-V semiconductors that can be lattice matched to GaAs while exhibiting both conduction and valence band offsets with GaAs: $Al_{0.8}Ga_{0.2}As$ and $Ga_{0.51}In_{0.49}P$. While the former can offer a large conduction band offset with GaAs for $x = 0.8$, the latter exhibits a larger valence band offset but a conduction band offset limited to about 170 meV. One key parameter for the final choice is their ability to be grown on GaAs (111) substrates with a low surface roughness, as seen in the previous chapter, that it is critical to achieve a smooth InSb growth.

This chapter is thus divided in three sections. First, the **MBE** thin film growth of $Al_{0.8}Ga_{0.2}As$ and $Ga_{0.51}In_{0.49}P$ on GaAs $(111)_B$ will be investigated after reviewing the literature for these materials. Then, the subsequent InSb thin film growth on the potential barrier yielding the smoothest morphology will be discussed. The third section will deal with the InSb **SAG** experiments of the full stack InSb/semi-conducting barrier/GaAs $(111)_B$.

5.2 Semiconducting barrier growth on GaAs $(111)_B$ substrates

5.2.1 $Al_{0.8}Ga_{0.2}As$ thin film growth on GaAs $(111)_B$

Literature review

The epitaxial growth of $Al_xGa_{1-x}As$/GaAs on GaAs (001) is perfectly mastered for several decades with extremely high electron mobility exceeding several tenths of millions $cm^2.V^{-1}.s^{-1}$ at **LT** thanks to a very low interface roughness.[56] Yet, AlGaAs grown on (111) GaAs substrates exhibits much rougher surfaces composed of pyramidal hillocks and twin defects.[220,221,222,223] While a large part of the AlGaAs thin films demonstrated a very rough surface, a mirror-like surface was achieved in specific growth conditions. Only a large increase in the growth temperature close to 900 °C via **Metal-Organic Vapor Phase Epitaxy (MOVPE)** or intentional misorientation from (111) orientation (2° off) helped in smoothing the surface.[222] Upon further studies, the formation of rough AlGaAs surfaces on GaAs $(111)_B$ was assigned to the short migration length of Al adatoms.[221] A viable option dwelt in **Migration Enhanced Epitaxy (MEE)**. As employed by Imamoto *et al.*, this technique allowed to grow smooth (low Al content) $Al_{0.2}Ga_{0.8}As$ epi-layer at low temperatures in the range of 400 – 500°C. In **MEE**, group III and V-elements are deposited alternatively to react and form the layer. Typically, deposition times of 1 and 3 seconds were used for III and V-elements respectively. Over cycling, this technique promotes the migration of the adatoms on the surface. As a result, for an $Al_{0.3}Ga_{0.7}As$-GaAs single **QW**, a 50 times higher photo-luminescence was obtained compared to similar structures grown on (001) substrate.[224]

For an on-axis (111) substrate, a high growth temperature (> 650 °C) coupled to a low V/III ratio is recommended as the resulting morphology was found to be extremely sensitive to As-surfaces.[225,226,227] As a matter of fact, these As-stabilized surfaces are deemed to affect Ga incorporation. In such conditions, a lower **RMS** roughness of the AlGaAs thin film on GaAs $(111)_B$ was obtained when the As pressure was reduced. Controversially, the growth of AlGaAs on GaAs $(111)_A$ showed opposite behavior, with a smoother film under high As pressure.[228]

Eventually, for high Al-content AlGaAs, higher growth temperatures are needed to counteract the small Al adatoms surface migration length that promotes twin defects appearance.[221] Yet, this adds up to the extreme sensitivity of the GaAs $(111)_B$ surface, which will reach its thermal stability limits, especially if low As pressures are expected.

Growth conditions

As AlGaAs remains nearly-lattice matched to GaAs across the whole composition range (a_{AlAs} = 5.6611 Å, *i.e.* f = 0.13 %), this ternary III-V semiconductor proved to be useful for **HEMT** and RF or high-power electronics applications.[229,230] To aim for an efficient blocking of the electrons with the $Al_xGa_{1-x}As$, we choose a high Al-content of $x = 0.8$ as the conduction band offset with GaAs is ∼0.55 eV. However, for such a composition, the thin film develops a strong predisposition to oxidation. Therefore, all the $Al_{0.8}Ga_{0.2}As$ layers grown in this work require a cap to prevent strong oxidation in air during post-growth characterization such as **AFM**. All the necessary information regarding the growth conditions are summarized in Table 5.1. Keeping the same logic, these samples are labelled **AG** referring to “AlGaAs on GaAs”. As explained in chapter 4 section 4.2.3.1, we initially believed that a smoother surface could be achieved with the use of a GaAs buffer (Figure 5.1). This GaAs buffer probably does not exhibit the same morphology as the one presented in the previous chapter (section 4.2.1) because it was grown at higher $\mathbf{T_G}$. Unfortunately, no **AFM** study was conducted on the buffered substrate, but supplementary experiments were done on as-deoxidized GaAs substrate for comparison.

Sample	**AG1**	**AG2**	**AG3**	**AG4**	**AG5**
AlGaAs $\mathbf{V_G}$ (**ML**/s)	0.5	0.5	0.5	0.5	0.5
AlGaAs V/III ratio	2	8.7	8.7	10	10
AlGaAs $\mathbf{T_G}$ (°C)	690	690	630	580	620
AlGaAs $t_{nominal}$ (nm)	100	100	100	100	100
GaAs cap $\mathbf{V_G}$ (**ML**/s)	0.3	0.3	0.3	0.5	0.5
GaAs cap V/III ratio	3.33	14.5	14.5	10	10
GaAs cap $\mathbf{T_G}$ (°C)	630	630	610	580	620
GaAs buffer $\mathbf{V_G}$ (**ML**/s)	0.3	0.3	0.3	✗	✗
GaAs buffer V/III ratio	3.33	6	6	✗	✗
GaAs buffer $\mathbf{T_G}$ (°C)	630	630	610	✗	✗
GaAs buffer $t_{nominal}$ (nm)	20	20	20	✗	✗
GaAs wafer supplier	AxT	AxT	AxT	WT	WT

Table 5.1: AlGaAs on GaAs $(111)_B$ samples growth conditions.

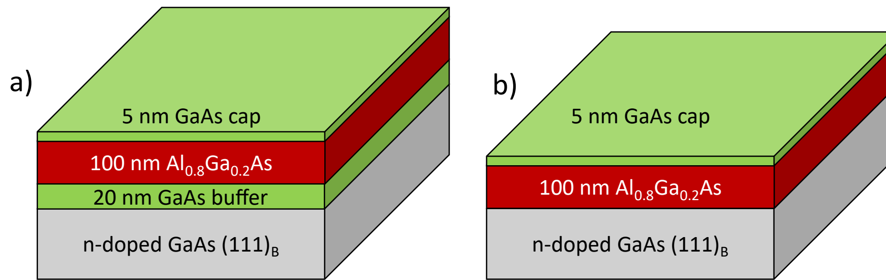


Figure 5.1: Schematics of the $Al_{0.8}Ga_{0.2}As$ structure grown on GaAs $(111)_B$ substrates with a) a 20 nm GaAs buffer layer and a 5 nm GaAs cap and b) without the GaAs buffer layer.

To protect all samples from oxidation in air and perform proper **AFM** characterization, the $Al_{0.8}Ga_{0.2}As$ thin films were covered by a 5 nm-thick GaAs cap. The cap growth conditions are also gathered in Table 5.1.

5.2.1.1 Influence of the V/III ratio

From the state of the art growth for an AlGaAs layer on a GaAs $(111)_B$ substrate, a rather low As/Ga ratio (3.33) was used for the buffer growth of the first sample **AG1**. In this case, a 20 nm-thick GaAs buffer layer was grown at a temperature of 630 °C prior to AlGaAs epitaxy. In these conditions, a $(\sqrt{19} \times \sqrt{19})$ **RHEED** pattern, which is characteristic of a GaAs surface reconstruction with As-vacancy, is observed.[197] The $Al_{0.8}Ga_{0.2}As$ layer was further grown at 690 °C with a V/III ratio of 2 to promote Al diffusion. To protect the sensitive AlGaAs layer from oxidation a 5 nm GaAs capping layer grown at 630 °C was added on top.

In these conditions, as shown in Figure 5.2a the layer exhibits a rough puzzled surface sprinkled by deep trenches over the whole area. Their depth extends up to 40 nm compared to the top surface. At smaller scale, some triangular etch pits are also observed (Figure 5.2b).

For the growth of the second sample, we increased the general As flux, resulting in a higher

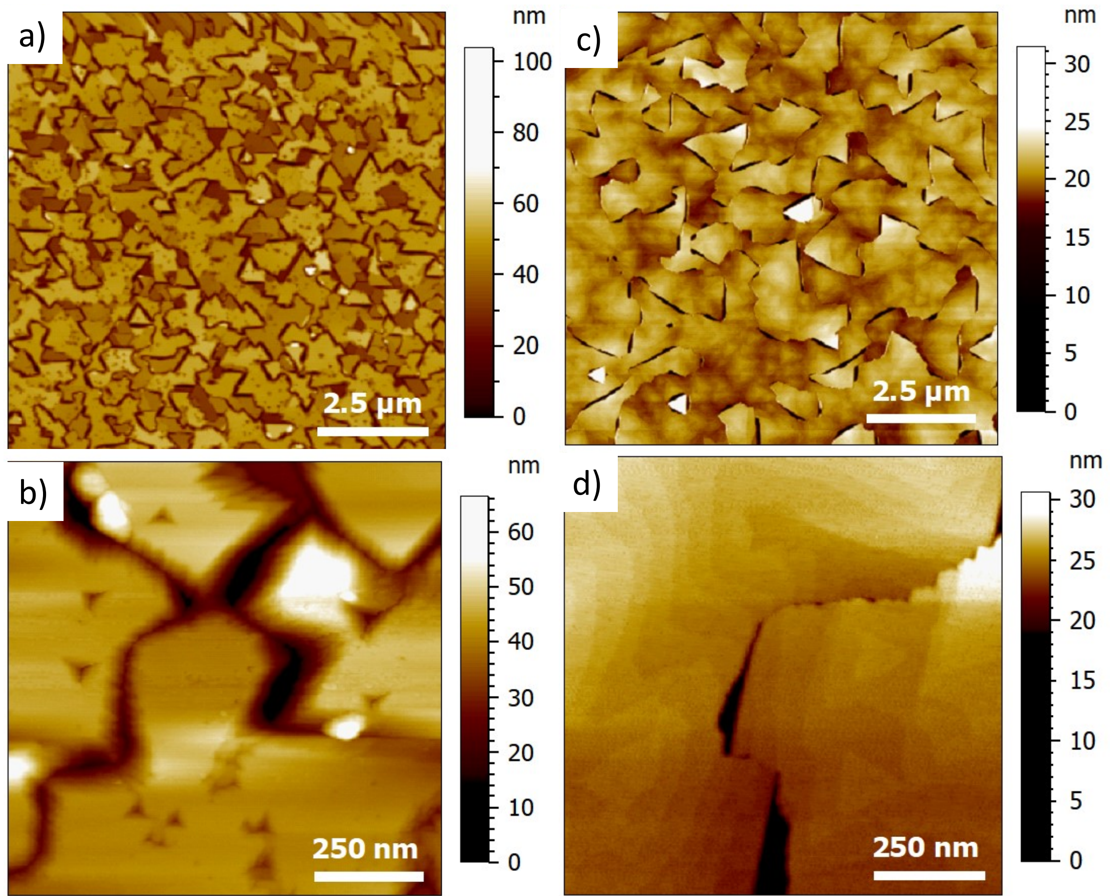


Figure 5.2: a) **AFM** image of sample **AG1**. b) Magnified view with a lateral scan size of 1 µm. c) **AFM** image of sample **AG2**. d) Magnified view with a lateral scan size of 1 µm.

V/III ratio for these different epilayers (the GaAs buffer, the $Al_{0.8}Ga_{0.2}As$ layer and the GaAs cap). By increasing the V/III ratio to 8, the $Al_{0.8}Ga_{0.2}As$ morphology of sample **AG2** shows significant differences (Figure 5.2c). The density of trenches is reduced, with no visible etch pits as well. The sample **AG2** exhibits a lower surface roughness (1.78 nm at 10 µm x 10 µm scale vs 9.94 nm for sample **AG1**) which is partially induced by atomic terraces observed at smaller scale (Figure 5.2d). Moreover, the trench depth is smaller, ranging now between 10 – 15 nm. This indicates a positive impact of a larger V/III ratio on the surface morphology.

5.2.1.2 Influence of the growth temperature (T_G)

In order to reduce the As desorption rate from GaAs and AlGaAs surfaces, a lower growth temperature was used for sample **AG3** (Table 5.1). $\mathbf{T_G}$ was set to 630 °C, while comparable growth rate and V/III ratio to the previous experiments were used.

Figure 5.3 displays **AFM** images at large and small scales of the sample **AG3** as well as an example of height profile across a trench. Unfortunately, the morphology exhibits some similarities with the one of sample **AG1**. The trenches are still visible but are now shallower with a depth of 5 nm only. Etch pits are seen here and there in the magnified view of Figure 5.3b. Finally, the atomic terraces are clearly observed and appear to be wider than the ones seen on

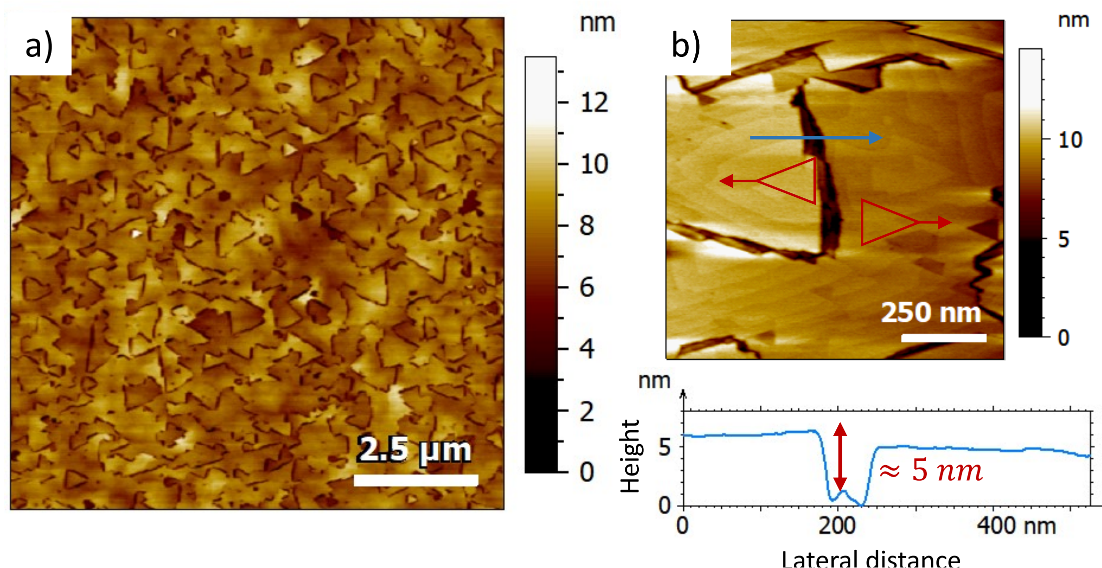


Figure 5.3: a) **AFM** image of sample **AG3**. b) Zoom in at 1 µm scan size with a height profile across a trench outlined by the blue arrow. The red triangles and pointing arrow illustrate the different domain orientation from both sides of a trench.

sample **AG2**. Moreover, the terrace orientation on the different grain clearly changes, as guided by the red triangles pointing in different directions. From one side of the trench to the other, a 180° rotation is seen. Thus, the trench seems to originate from the grain boundary associated with twin domains formed at the initial nucleation of the film. Thanks to a reduction of the growth temperature, the overall **RMS** roughness is improved (1.16 nm). The slower diffusion of III-element adatoms may favor a uniform nucleation and a decrease of the As desorption. Nevertheless, the presence of trenches still hinders the growth of a smooth InSb film on top.

5.2.1.3 Impact of GaAs buffer layer

Taking into account the results from chapter 4 section 4.2.3.1 and the roughness resulting from the GaAs buffer layer growth, the direct growth of $Al_{0.8}Ga_{0.2}As$ on a buffer-free GaAs substrate was also considered (Figure 5.1b). A high V/III ratio of 10 and lower $\mathbf{T_G}$ of 580 °C and 620 °C were used for sample **AG4** and **AG5** respectively (Table 5.1).

The Figure 5.4 shows the morphology of the $Al_{0.8}Ga_{0.2}As$ layer grown on buffer-free GaAs $(111)_B$ substrates. The surfaces in Figures 5.4a and b reveal a different morphology from the previous experiments. Here, no trenches are visible even though the overall **RMS** roughness remains above one nanometer (1.4 nm) due to the grainy texture of the film. Because the growth temperature is much lower (580 °C), adatom diffusion is strongly limited, increasing the density of nucleation sites and giving rise to the observed degree of roughness.[221]

Regarding the sample **AG5** grown at $\mathbf{T_G}$ = 620 °C in Figures 5.4c and d, a morphology similar to the one of sample **AG3** is observed. A high density of trenches with some etch pits is visible in this case as well. Their depth also ranges between 5 – 6 nm, demonstrating that the GaAs buffer layer does not much impact the final morphology. Although the strong sensitivity of $Al_{0.8}Ga_{0.2}As$ to the growth conditions is demonstrated, we could not obtain satisfying results so far on GaAs $(111)_B$ substrates.

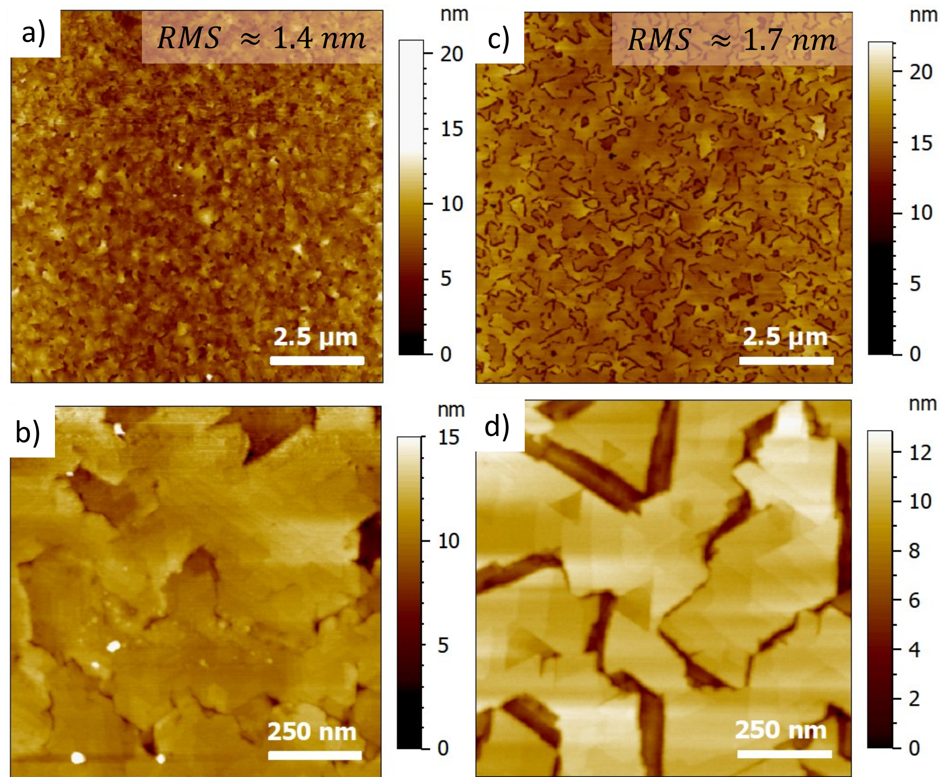


Figure 5.4: a) **AFM** image of sample **AG4** grown on GaAs $(111)_B$. b) Zoom at 1 µm scan size c) **AFM** image of sample **AG5** grown on GaAs $(111)_B$. d) Zoom at 1 µm scan size.

Conclusion
Throughout this section, several experiments were conducted to optimize the morphology of $Al_{0.8}Ga_{0.2}As$ on GaAs (111) substrates. Growth conditions combining a high $\mathbf{T_G}$ and low As/III ratio result in a surface morphology exhibiting deep trenches and etch pits. By increasing the As/III ratio and reducing the growth temperature, the morphology evolved into a smoother surface with shallow trenches (5 nm) but their density is still too high. By comparing the direct growth of AlGaAs layers on GaAs substrates with similar layers grown on a 20 nm-thick GaAs buffer, we conclude that the main origin of the roughness is due to the AlGaAs layer itself. In short, an unsatisfactory high surface roughness $Al_{0.8}Ga_{0.2}As$ layer was consistently obtained, preventing its use as a good seed layer for InSb growth. Therefore, this limitation calls for an alternative.

5.2.2 $Ga_{0.51}In_{0.49}P$ thin film growth

Literature review

Similar to AlGaAs, the growth of GaInP on GaAs (111) is quite complex. Martinez *et al.* studied the GaInP growth on various GaAs substrates such as (001), $(111)_A$ and $(111)_B$. Because their surface dangling bonds differ, meaning a change in surface reconstruction, the growth mechanisms are drastically different.[231] Using **MOCVD** and a growth temperature of 600 °C, the GaInP layer shows a specular surface for (001) and $(111)_A$ substrates. In contrast, its growth

on $(111)_B$ substrates exhibits an island morphology. The islands are predicted to be Ga-rich due to growth rate fluctuations. These variations are attributed to the difference of the diffusion length between Ga and In species on the surface.[232]

In the case of GaInP growth on GaAs $(111)_B$, an intentional misorientation from the exact $(111)_B$ orientation was also prescribed to promote a step-flow growth. As proposed by Morita *et al.*, the step edges from the offcut help regulating the adatom incorporation along the steps.[233] Conversely, the absence of step edges inevitably gives rise to an island nucleation, hence roughening the surface. On such exactly oriented $(111)_B$ surfaces, the absence of step makes the nucleation sites very sensitive to the underlying surface. In the growing layer, twin defects are easily formed because the formation energy of a twin is low.

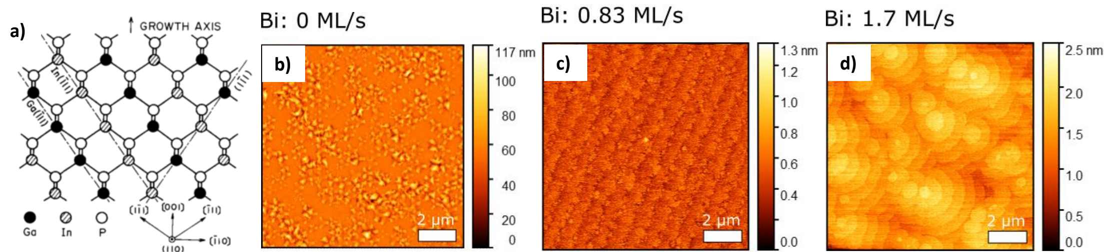


Figure 5.5: a) Schematic structure of the CuPt ordering from layered Ga and In atom $(\bar{1}11)$ planes for a GaInP growth on (001) substrate. Extracted from[234]. **AFM** images of $Al_{0.3}Ga_{0.7}As$ / GaAs $(111)_A$ layers grown for different Bi fluxes: b) Without any Bi, the surface exhibits protrusion, c) under 0.83 **ML**/s of Bi, the surface becomes atomically flat with visible rough terraces. d) For higher flux of Bi, 1.7 **ML**/s the **RMS** roughness increases slightly, though the surface remains smooth the terraces become rounded. Extracted from[235].

Last but not least, some studies focused on the use of surfactant-mediated GaInP growth on (001) oriented substrates. Along this direction, GaInP exhibits CuPt-type ordering superlattices in the equivalent <111> directions. Ga and In atoms are arranged in a layered structure as depicted through Figure 5.5a. Intensive efforts were done to suppress, control or benefit from this ordering that involves band gap reduction, polarized photoluminescence and induced strain.[236,237,238] Many surfactants were investigated to alter the order parameter such as Te, Si, Zn, Sb, Bi and As through different mechanisms involved in the growth kinetics.[239,240]

Particularly Sb and Bi were found to efficiently suppress ordering. They were further found to smooth the surface morphology. G.B.Stringfellow's group highlighted that a low concentration of surfactant was needed to induce changes: a Sb/P ratio in the vapor phase not exceeding 4×10^{-4} efficiently eliminates the phosphorus dimers on the surface that are needed for CuPt ordering.[241] Higher concentration led to a change of the surface reconstruction that cancelled the benefits of the surfactant.

In the case of Bi, more pronounced changes were evidenced in comparison with Sb for similar vapor concentrations.[239] A smooth surface involving a sequence of atomic-high terraces was obtained for a Bi/III_v[1] ratio of 1.65×10^{-2}. Attributed to impact group III incorporation kinetics on step edges, Bi also revealed to be beneficial in smoothing GaAs and $Al_{0.3}Ga_{0.7}As$ $(111)_A$ surfaces up to fluxes of 1.7 **ML**/s[235] (Figures 5.5b, c, d). This promising approach needs nonetheless further investigation on other III-V (111)-type substrates and epilayers.

[1] the v refers to the vapor phase flux of the III element

Growth conditions

The epitaxial growth of $Ga_{0.51}In_{0.49}P$ on GaAs was investigated as a result of the complex optimization of $Al_{0.8}Ga_{0.2}As$ surfaces. Because this III-V ternary compound does not contain any Al, the starting growth temperature is reduced, matching better the thermal stability of a GaAs substrate. Here, no GaAs buffer was grown for any of the samples because a higher roughness was obtained, when such a buffer was used, as explained in chapter 4 section 4.2.3.1. Instead, we decided to grow GaInP on buffer-free (as-deoxidized) GaAs $(111)_B$ substrates. For all samples, no $\mathbf{H_{AT}}$ flux was added during the epitaxial growth. The set of constant growth parameters used during the first experiments was defined as: low $\mathbf{V_G}$ = 0.2 **ML**/s, high V/III ratio of 50 (P flux of ≈10 **ML**/s), $\mathbf{T_G}$ = 520 °C and a GaInP thickness of 100 nm. Table 5.2 gathers the different growth conditions used in this study.

Sample	**GG1**	**GG2**	**GG3**	**GG4**	**GG5**	**GG6**	**GG7**
$\mathbf{V_G}$ (**ML**/s)	0.2	0.2	0.2	0.2	0.1	0.2	0.4
V/III ratio	50	50	50	50	50	50	50
$\mathbf{T_G}$ (°C)	520	520	530	550	520	520	520
$t_{nominal}$ (nm)	100	100	100	100	100	100	100
GaAs wafer supplier	AxT	AxT	AxT	WT	WT	WT	WT

Table 5.2: GaInP on GaAs $(111)_B$ 2D samples growth conditions.

5.2.2.1 Influence of the growth temperature

We started by investigating the impact of the growth temperature. The first samples **GG1** and **GG2** were both grown at $\mathbf{T_G}$ = 520 °C. These samples correspond to the GaInP growth on 2-inches GaAs wafers, that were used for subsequent InSb thin film growth and **SAG** experiments. As imaged in Figures 5.6a and b, despite the same growth conditions were used, sample **GG1** exhibits a lower **RMS** roughness than sample **GG2**. The rounded atomic terraces visible in sample **GG1** are due to a residual Sb content in the **MBE** chamber despite the shutter was closed, because the sample was grown during an epitaxy campaign where the Sb evaporator was at 570 °C and the cracker cell at 900 °C. Conversely, sample **GG2** was grown during a Sb-free campaign, meaning the Sb evaporator temperature was set to 350 °C and the cracker cell at 700 °C. Because such an effect was observed on the morphology of sample **GG1**, the Sb-surfactant effect will be investigated more thoroughly in following of this work.

Visible in Figures 5.6b and c, the surface of the GaInP layer (sample **GG2**) significantly differs from the morphology observed with the $Al_{0.8}Ga_{0.2}As$ films. Instead of trenches, the morphology of GaInP consists in a bunching of elongated pyramids similar to the GaAs buffer morphology in chapter 4 section 4.2.1. The **RMS** surface roughness of sample **GG2** at 10 µm scan size remains higher than 1 nm (2.35 nm exactly) due to the terrace-step structure. The terrace width ranges between 35 – 75 nm. By slightly increasing the growth temperature (sample **GG3**), the surface morphology remains similar even though more faceted pyramids appeared (Figure 5.6d). The atomic terrace width increases to 100 nm (not shown), this result being attributed to an increased diffusion length. Overall, the surface **RMS** roughness heightened gently up to 3.03 nm. With further increase in the temperature, the growth regime totally switched towards a 3D islanding mode as depicted in Figure 5.6e.

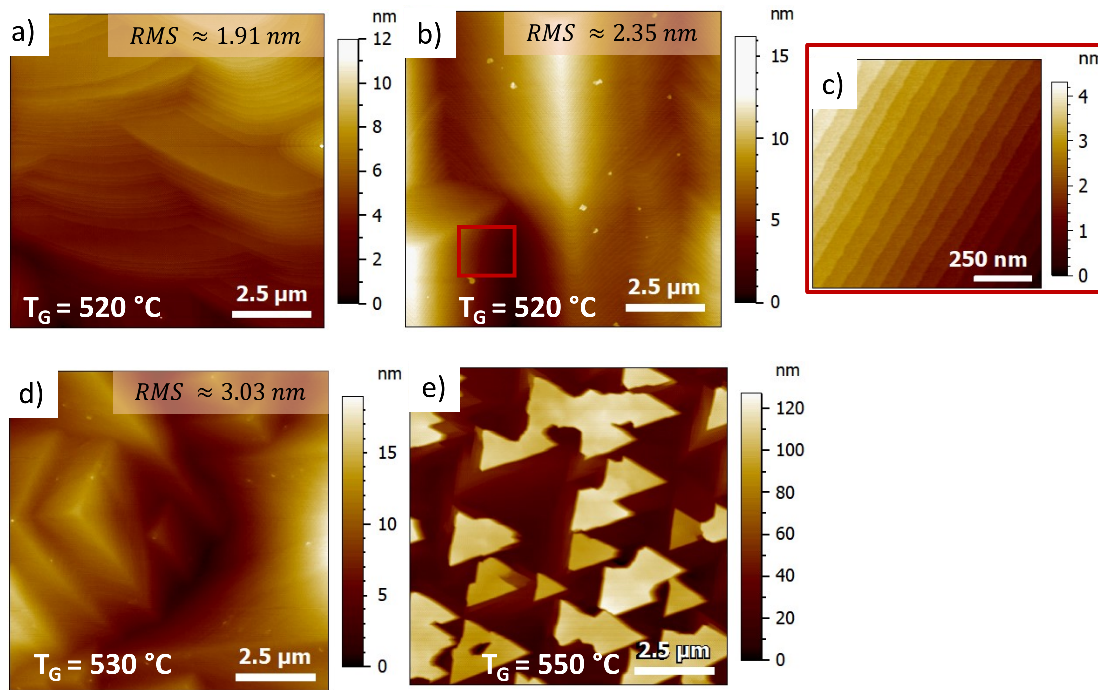


Figure 5.6: a) **AFM** image of sample **GG1**. b) **AFM** image of sample **GG2**. c) Zoom-in at 1 µm scan size on an elongated pyramid of sample **GG2**. d) **AFM** image of sample **GG3**. $\mathbf{T_G}$ = 530 °C. e) **AFM** image of sample **GG4** grown at 550 °C.

In this **AFM** image, the surface shows islands that are higher than 60 nm. At such temperature, the adatoms start to migrate over long distances enhancing island nucleation. On top of that, the group III desorption was also increased, which can cause fluctuations in the local composition.

5.2.2.2 Influence of the growth rate

To further investigate the influence of the growth parameters on the GaInP layer morphology, variation of the growth rate was considered. Referring to Table 5.2, three $\mathbf{V_G}$ values are compared: 0.1, 0.2 and 0.4 **ML**/s corresponding to samples **GG5**, **GG6** and **GG7** respectively.

As displayed in Figure 5.7, minimal changes of the morphology are visible and step-flow growth regime remains for all three samples. For a lower value of $\mathbf{V_G}$ (sample **GG5**), the surface presents a larger number of elongated pyramids visible on the scan. At smaller scale in 5.7b, the atomic terraces are mainly regular although some of them reveals a larger width up to 200 nm.

For the sample **GG6** (Figures 5.7c and d) grown at 0.2 **ML**/s, a lower **RMS** roughness (1.06 nm) than sample **GG5** is found as a result of a lower amount of elongated pyramids on the surface. Nevertheless, the atomic terraces at smaller scale follow the same trend than in sample **GG5**. Moreover, the **RMS** roughness value of **GG6** is also lower than the one of **GG2** while both samples were grown in similar conditions and imaged at the same scale. As we used a GaAs wafer supplied by WT, having a different constraint on the miscut orientation with respect to the (111) direction (±0.1° for **GG6** instead of ±0.5° for **GG2**), we suspect that the substrate misorientation could play a role on the final surface roughness as reported in different studies.[221,242,243] A careful measurement of the substrate properties would then be needed to control this parameter.

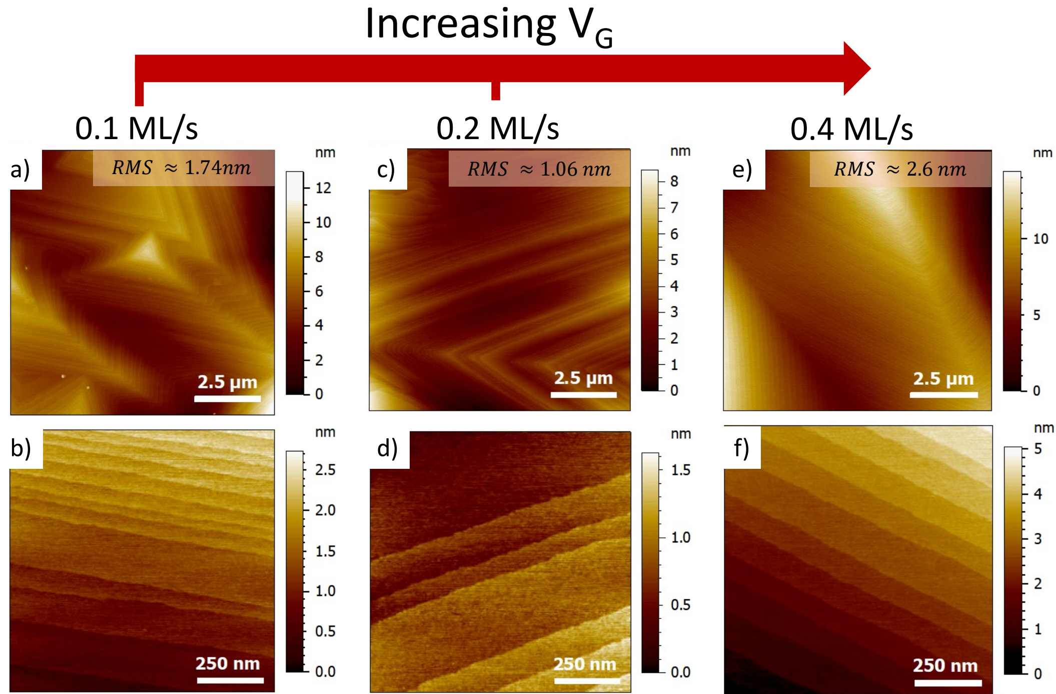


Figure 5.7: a) **AFM** image of sample **GG5** under reduced $\mathbf{V_G}$ (0.1 **ML**/s). b) zoom at 1 µm scan size c) **AFM** image of sample **GG6** grown at $\mathbf{V_G}$ = 0.2 **ML**/s. d) zoom at 1 µm scan size . e) **AFM** image of sample **GG7** deposited at higher $\mathbf{V_G}$ = 0.4 **ML**/s f) zoom at 1 µm scan size.

The last sample **GG7**, grown at higher growth rate (0.4 **ML**/s) exhibits the largest **RMS** roughness of the three samples of this study. The morphology at large scale (Figure 5.7e) resembles to the one of sample **GG2**. At smaller scale in Figure 5.7f, the atomic terraces here are more regular as observed as well in sample **GG2**, which suggests that the growth rate does not play a significant role in this range of values. In this regard, we decided to continue with the standard value of $\mathbf{V_G}$ = 0.2 **ML**/s for the following GaInP growth experiments.

5.2.2.3 Effect of the Sb surfactant

Driven by the studies praising the beneficial effect of a surfactant mediated growth for GaInP and the observed morphology of sample **GG1**, the use of an Sb flux during epitaxy was investigated in several ways. Table 5.3 summarizes all the growth conditions. The samples follow a **GSG** label standing for "GaInP-Sb surfactant on GaAs".

Three 50 nm-thick GaInP samples were fabricated to investigate the addition of Sb during growth. All other parameters are similar to the optimized conditions found so far, *i.e.* $\mathbf{T_G}$ = 520 °C, $\mathbf{V_G}$ = 0.2 **ML**/s, V/III = 50. **GSG1** was grown with a direct Sb flux of 0.03 **ML**/s added during the GaInP layer growth. While the Sb/P ratio must be low, the added Sb flux cannot be further reduced in our **MBE** system due to valve control accuracy of the cell. The second sample was grown without any Sb flux during growth but was mounted onto a sample holder previously used for the growth of Sb containing layers. Hence, the plate is covered with condensed Sb from previous growths (as it can be deduced from its light grey color). Nevertheless, the exact amount of Sb condensed on the plate cannot be determined accurately which leaves the Sb flux parameter as unknown here.

Sample	GSG1	GSG2	GSG3
$\mathbf{V_G}$ (ML/s)	0.2	0.2	0.2
P/III ratio	50	50	50
$\mathbf{T_G}$ (°C)	520	520	520
$t_{nominal}$ (nm)	50	50	50
$\mathbf{H_{AT}}$	✓	✓	✓
Sb flux	≈0.03 **ML**/s	Sb-packed sample holder	✗

Table 5.3: Growth conditions of GaInP on GaAs $(111)_B$ with Sb surfactant.

Thirdly, for **GSG3**, the GaInP layer is grown on a substrate holder free from Sb condensation, but following an epitaxial growth campaign of antimonide compounds. Therefore, residual Sb inside the **MBE** chamber probably acted as a surfactant for this sample **GSG3**.

Figure 5.8 compares the **AFM** images of the three samples. As mentioned in the literature, a drastic change in the layer morphology can be seen with the addition of the Sb surfactant. All three surfaces do not display the regular elongated pyramids but instead circular flattened protrusions with various density.

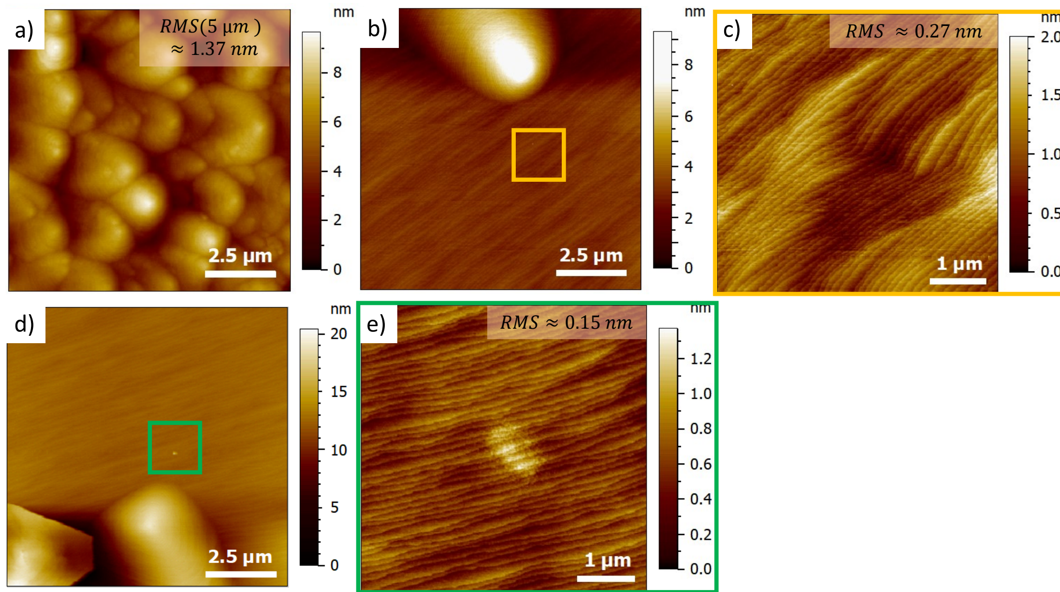


Figure 5.8: a) **AFM** image of sample **GSG1**. b) **AFM** image of sample **GSG2**. c) Zoom at smaller scale of sample **GSG2**. d) **AFM** image of sample **GSG3**. e) Zoom at smaller scale of sample **GSG3**.

In the case of sample **GSG1**, the addition of an Sb flux during the growth triggered a transition in the **RHEED** from a (1×1) to a (2×2) surface reconstruction. In Figure 5.8a, the surface consists of entangled circular pyramids of various sizes that results in a bumpy morphology, although the **RMS** roughness at 5 µm remains relatively low (1.37 nm). While the advised Sb/P ratio from the literature[241] should not exceed $4{\times}10^{-4}$, in the present case the value was more lying in the 10^{-3} range.

The second sample depicted in Figure 5.8b exhibits a flattened surface with a single protrusion with a height of 7 nm relative to the smooth background. These protrusions may arise from In droplets. At smaller scan size (Figure 5.8c) away from the protrusion, the **RMS** roughness reaches a very low value (0.27 nm). Although the exact amount of Sb is not known, the significantly smoother morphology can be attributed to a lower rate of Sb adsorbed on the surface. During this growth, the GaInP **RHEED** remained (1×1), corresponding to the usual surface reconstruction in P-rich atmosphere.

The last sample **GSG3** presents a similar morphology than for **GSG2** (Figure 5.8d). The atomic terraces revealed at smaller scale in Figure 5.8e are less rounded than for sample **GSG2**. Nevertheless, the probably residual Sb inside the chamber is responsible of this effect as their shape differs from the regular atomic terraces observed in the previous samples (albeit a thicker GaInP film). At larger scale, no new defects are seen, traducing the low defect density and promoting the smoothness of this GaInP film.

In summary, the benefits of adding an Sb flux during the growth of GaInP on GaAs $(111)_B$ substrates remains complex. The exact quantity of Sb needs to be carefully controlled to yield a smoothing effect. Indeed, for excessive Sb flux, the GaInP morphology becomes wavy and develops circular protrusions. Despite some protrusions are still visible, the use of a low Sb flux during GaInP growth keeps the surface **RMS** roughness relatively low as in sample **GSG3**. Nevertheless, further characterization is needed to assess the potential Sb incorporation into the GaInP layer.

5.2.2.4 XRD analysis of the GaInP samples

The influence of the growth conditions (discussed in the previous sections) on the ternary composition of the GaInP layer through **XRD** is investigated herein. In order to minimize the lattice mismatch with GaAs and avoid strain induced defects, the right $Ga_{0.51}In_{0.49}P$ composition is required. Figure 5.9 gathers the **XRD** $\omega - 2\theta$ scans along the $[\bar{1}\bar{1}\bar{1}]$ direction of all the studied samples.

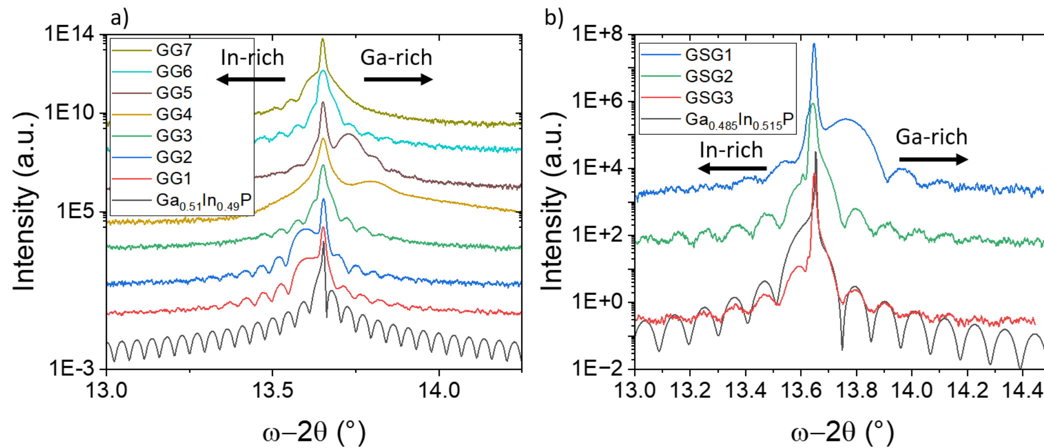


Figure 5.9: a) **XRD** curves of all studied GaInP samples. The bottom curve simulates a 100 nm-thick $Ga_{0.51}In_{0.49}P$ layer on GaAs $(111)_B$. Curves are aligned horizontally on the substrate peak and are vertically shifted for clarity purposes. b) **XRD** curves of all studied Sb-surfactant mediated GaInP samples. The bottom black curve corresponds to the simulated fit of sample **GSG3** giving a 42 nm-thick $Ga_{0.485}In_{0.515}P$ layer on GaAs $(111)_B$.

Each curve is aligned on the substrate peak and shifted to higher intensity for clarity purposes. In Figure 5.9a, the bottom curve (grey), corresponds to a simulated spectrum assuming a 100 nm-thick $Ga_{0.51}In_{0.49}P$ layer on GaAs $(111)_B$. Among the various curves, the samples can immediately be divided into two categories. The first one corresponds to samples showing the Pendellösung fringes, which are the periodic oscillations seen aside of the main diffraction peak. The Pendellösung effect arises from coherent interference between X-rays reflected from different interfaces within a crystal or thin film.[244] The observation of Pendellösung fringes indicates a sharp interface with the substrate and a smooth film surface. The second category corresponds to samples not showing any of these oscillations. The absence of Pendellösung fringes could be attributed to rough surfaces and interfaces as well as the presence of crystal defects in the layer. This is the case for the sample **GG4** which showed a defective and very rough surface. While **GG5** and **GG7** exhibited a relatively smooth surface (Figures 5.7a and e), the Pendellösung fringes are very damped.

By comparing the reference spectrum (in grey at the bottom of Figure 5.9a) with regards to all other spectra, variations in the composition of the GaInP layer can be noticed from one sample to the other (**GG1**: $Ga_{0.487}In_{0.513}P$, **GG2**: $Ga_{0.478}In_{0.522}P$, **GG3**: $Ga_{0.502}In_{0.498}P$, **GG4**: $Ga_{0.605}In_{0.395}P$, **GG5**: $Ga_{0.567}In_{0.433}P$, **GG6**: $Ga_{0.525}In_{0.475}P$, **GG7**: $Ga_{0.493}In_{0.507}P$).

The usual optimized recipe found for sample **GG1** and **GG2** that produced high quality layers appears to be In-rich, *i.e.* slightly compressively strained (bump on the left-side). In contrast, sample **GG6** that was grown with identical parameters has a GaInP composition closer to the expected values. Because of the low growth rate used in these experiments, it is possible that the elemental fluxes calibration is not accurate enough to avoid such composition variations.

Based on this **XRD** analysis, the effect of the growth temperature on the composition is clearly confirmed with a transition from In-rich in **GG2** to a more lattice matched layer in **GG3** and ending up with a Ga-rich composition in **GG4**. This result corroborates well with the increased In desorption at higher temperatures, that is directly reflected in the altered composition. In this case, the In flux should be increased to sustain the optimal GaInP composition and possibly obtain even smoother layers. With regards to the growth rate effect, the sample **GG5** grown at $\mathbf{V_G}$ = 0.1 **ML**/s also shows a Ga-rich composition (bump on the right-side).

For the influence of the Sb-surfactant, the first three samples show differences in the **XRD** scans presented in Figure 5.9b. When the sample is grown on the As-rich sample holder (**GSG3**) or the Sb-rich one (**GSG2**), a slight In-rich composition is seen corresponding here to $Ga_{0.485}In_{0.515}P$. In contrast, when Sb was added during the GaInP growth (**GSG1**), causing the **RHEED** pattern to change into a (2×2) reconstruction, a direct shift to a Ga-rich alloy occurs. The obtained $Ga_{0.536}In_{0.464}P$ layer confirms that no Sb has been incorporated in the layer. If this was the case, the GaInP composition would have been shifted towards In-rich composition. The observed behavior suggests that Sb reduces instead the In incorporation rate within the GaInP layer.

5.2.2.5 Influence of the wafer-edge on the film morphology

To finish up this section, a persistent effect was noticed for almost all GaInP growths. When the film morphology was bad or resulted in highly protruding elongated pyramids, the sample was coming out with a hazy surface visible with naked eye. This aspect was caused by the high density of pyramids on the surface which suppresses the usual mirror-like aspect of the wafer surface. However, in every of these samples with textured surfaces, the wafer rounded edges were smooth on at least several hundreds of micrometers from the edges (visible by naked eye). Under optical microscopes, the surface on the edges appeared featureless (Figures 5.10a and b).

After investigations, the difference between the central region (pyramid crowded = hazy

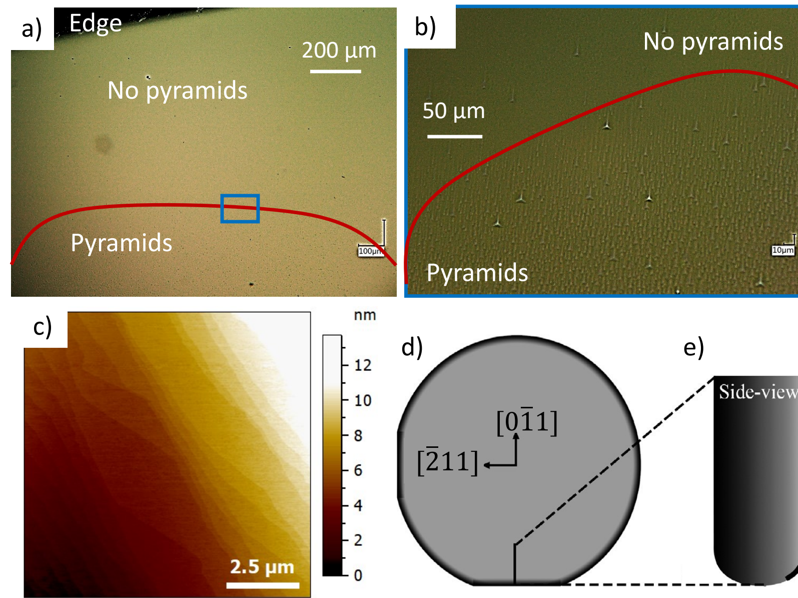


Figure 5.10: a) Optical microscope image of the rounded edge region. b) Zoom on the transition between the smooth and pyramid crowded region from blue rectangle in a). c) **AFM** image of sample **GG3** on the edge of the sample in a mirror-like region. d) Schematic of a 2-inches GaAs (111) wafer showing edge-bowing effect due to polishing. e) Side view of the line profile in d) where the edge bowing reveals the misorientation in this area. Adapted from[245].

aspect) and the wafer edge is attributed to the bowing at wafer-edge.[246] As depicted in Figures 5.10d and e, the wafers present a certain bowing that results from polishing. From the side view, this corresponds to a significant misorientation at this scale. As shown in Figure 5.10c, for sample **GG3**, a perfectly smooth surface consisting of atomic terraces is visible in this region. Here, no elongated pyramids are seen but a specular surface. This confirms the impact of misorientation from the (111) axis to produce specular surfaces.

Conclusion

Throughout this section, the GaInP growth was thoroughly investigated. The obtained films revealed a trenchless surface, composed mainly of elongated pyramids with ordered atomic terraces. The Sb-surfactant effect was studied through several epitaxial growth conditions. Despite a remarkable smoothing effect attributed to lower surface energies when a slight amount of Sb is used, the exact control of the introduced quantity remains complex. Additionally, the Sb exposure of the GaInP layer impacts the In incorporation rate in the growing layer affecting the final composition.

The GaInP layer composition was also evaluated and showed significant variation among the studied samples. In the end, the samples **GG1**, **GG2** and **GG6** all resulted in optimized GaInP growth as they exhibited a low **RMS** surface roughness without trenches. Such morphology was achieved under optimized growth conditions *i.e.* $\mathbf{T_G}$ = 520 °C, $\mathbf{V_G}$ = 0.2 **ML**/s, V/III = 50, which revealed to correspond to a GaInP with a slightly In-rich composition for **GG1** and **GG2**. Based on these results, the GaInP is clearly the best choice for obtaining a smooth InSb layer grown on top and act as a potential barrier for the modulation of charge carriers in the heterostructures.

5.3 InSb thin films on GaInP/GaAs$(111)_B$ heterostructures

5.3.1 Growth conditions

The results discussed in the previous section highlighted that under optimized growth conditions, GaInP on a GaAs $(111)_B$ substrate exhibits a smoother and trenchless morphology than AlGaAs on a GaAs $(111)_B$ substrate. Hence, the growth of InSb on GaInP/GaAs $(111)_B$ heterostructures (Figure 5.11) is investigated in order to enable a modulation of the charge density in InSb with a bias applied to the substrate.

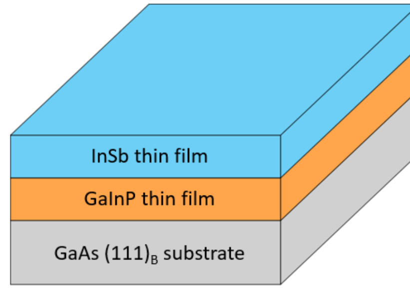


Figure 5.11: Scheme of the InSb/GaInP/GaAs 2D heterostructure.

Sample	**IGG1**	**IGG2**	**IGG3***	**IGG4***	**IGG5***	**IGG6***	**IGG7***	**IGG8***
$\mathbf{V}_{\mathbf{G}\,GaInP}$ (ML/s)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
V/III ratio	50	50	50	50	50	50	50	50
$\mathbf{T_G}$ (°C)	520	520	520	520	520	520	520	520
t_{GaInP} (nm)	45	45	100	100	100	100	100	100
$\mathbf{V}_{\mathbf{G}\,InSb}$ (ML/s)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
V/III ratio	136	136	136	136	136	136	136	136
$\mathbf{T_G}$ (°C)	390	375	385	385	350	365	385	430
t_{InSb} (nm)	20	20	100	100	20	20	20	20
$\mathbf{H_{AT}}$	✓	✓	✗	✗	✓	✓	✓	✓
Surface preparation	5 nm GaAs interf.	(1×1) **RHEED** GaInP	desox PH_3	desox As	desox As	desox As	desox As	desox As

Table 5.4: Growth conditions for different InSb thin films on GaInP/GaAs $(111)_B$ heterostructures.. The samples with a * indicates that a piece of GaInP/GaAs from **GG1** was used as substrate and deoxidized for the subsequent InSb growth.

Table 5.4 details all the experiments for the growth of InSb on GaInP/GaAs $(111)_B$ heterostructures. The label here follows an "**IGG**" naming convention according to "InSb on GaInP on GaAs". For samples **IGG1** and **IGG2**, the growth took place in a single run, meaning the GaAs substrate was deoxidized first, then a GaInP layer was grown at its respective $\mathbf{T_G}$ (Table 5.4) and finally the temperature was decreased to a suitable value ($\mathbf{T_G}$ of InSb in Table 5.4) to grow the InSb layer on top.

For samples **IGG3** to **IGG8**, the InSb growth was done on a piece of GaInP/GaAs $(111)_B$ heterostructures coming from sample **GG1**. In this case, as the GaInP surface was exposed to air, after its introduction in the **MBE** reactor for InSb epitaxy, the GaInP surface was deoxidized firstly. In that regard, the last row of Table 5.4 mentions the V-element (either P or As) used during the GaInP surface deoxidation.

Based on the preceding optimization works on both InSb on GaAs (in chapter 4) and GaInP on GaAs (in section 5.2.2), most of the growth parameters are already determined. As detailed in Table 5.4, for GaInP growth the usual optimized conditions $\mathbf{V_G}$ = 0.2 **ML**/s, V/III = 50, $\mathbf{T_G}$ = 520 °C are used because they favored the growth of layers with a lower **RMS** roughness.

Regarding the InSb growth parameters, the optimized conditions, which favored a rapid coalescence of the film as evidenced during the experiments on GaAs $(111)_B$ from Chapter 4 section 4.2.3, are used, *i.e.* a high V/III ratio of 136, a low $\mathbf{V_G}$ of 0.05 **ML**/s and a growth temperature around ∼390 °C. The $\mathbf{H_{AT}}$ indication in Table 5.4 represents the atomic hydrogen flux added during the growth of the InSb layer.

5.3.2 Deoxidation of GaAs and GaInP/GaAs surfaces

For all GaAs $(111)_B$ substrates, the same deoxidation process as described in chapter 4 section 4.2.1 is used. As indicated in Table 5.4, this oxide desorption method concerns the samples **IGG1** and **IGG2**.

Regarding the (**GG1**) GaInP/GaAs $(111)_B$ substrates used for samples **IGG3** to **IGG8**, the deoxidation process was a bit modified. The first recipe, valid for sample **IGG3**, consisted in heating the substrate up to 360 °C. Then, it was exposed to $\mathbf{H_{AT}}$ for 1 min up to 380 °C under a low P flux. Afterwards, the $\mathbf{H_{AT}}$ exposure was stopped and the sample was annealed under an increased P flux up to 440 °C. The substrate temperature was then decreased and stabilized to the proper $\mathbf{T_G}$ value for the subsequent InSb growth (P flux stopped below 400 °C). Unfortunately, no **AFM** was performed on a deoxidized GaInP surface under P flux but the sharp (1×1) **RHEED** pattern indicated a quite smooth surface.

For all remaining samples (**IGG4** to **IGG8**), the same recipe was used, but the P flux was replaced with an As flux to stabilize the GaInP surface. The substrate was first heated up to 360 °C. Then, a $\mathbf{H_{AT}}$ flux and As overpressure was added while heating further up to 380°C. Finally, the $\mathbf{H_{AT}}$ flux was stopped and the substrate was annealed up to 460 °C under an increased As overpressure giving either a (1×1) or faint (2×2) **RHEED** reconstruction. Once the deoxidation was finished and the substrate temperature decreased below 400 °C for InSb growth, the As flux exposure was stopped.

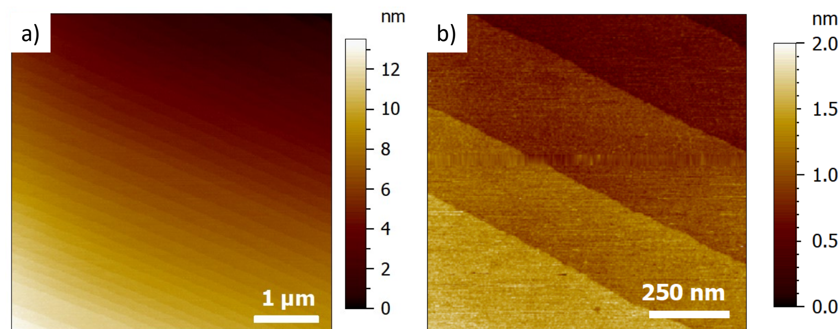


Figure 5.12: **AFM** images of **GG1** after deoxidation under As atmosphere at a) large scale and b) lower scale.

As seen in Figure 5.12, the GaInP surface of sample **GG1** after deoxidation under an As flux shows that the integrity of the atomic terraces is preserved. The morphology is similar to the one observed just after the **MBE** growth of **GG1** (Figure 5.6a). No $\mathbf{H_{AT}}$ etching is observed, hence validating this method to prepare the GaInP surface.

5.3.3 Morphology and structural study of the InSb film as a function of the growth parameters

5.3.3.1 Direct growth of InSb on GaInP

The first experiment with sample **IGG1** aimed at growing an InSb layer under the same conditions than the optimized results obtained on GaAs as seen in Table 5.4. To anticipate a possible interplay between InSb and GaInP, a 5 nm-thin GaAs layer was grown on top of the 45 nm-thick GaInP layer prior to the growth of InSb. To obtain such an intermediate GaAs layer, a P-As commutation was first done for 5 sec. After the growth of the GaAs layer, the As flux was decreased to 0 when the targeted growth temperature was reached. Then, the subsequent InSb growth took place. Comparatively, sample **IGG2** was elaborated in similar conditions (albeit a slightly lower growth temperature still in a convenient range) and without any GaAs layer in-between GaInP and InSb.

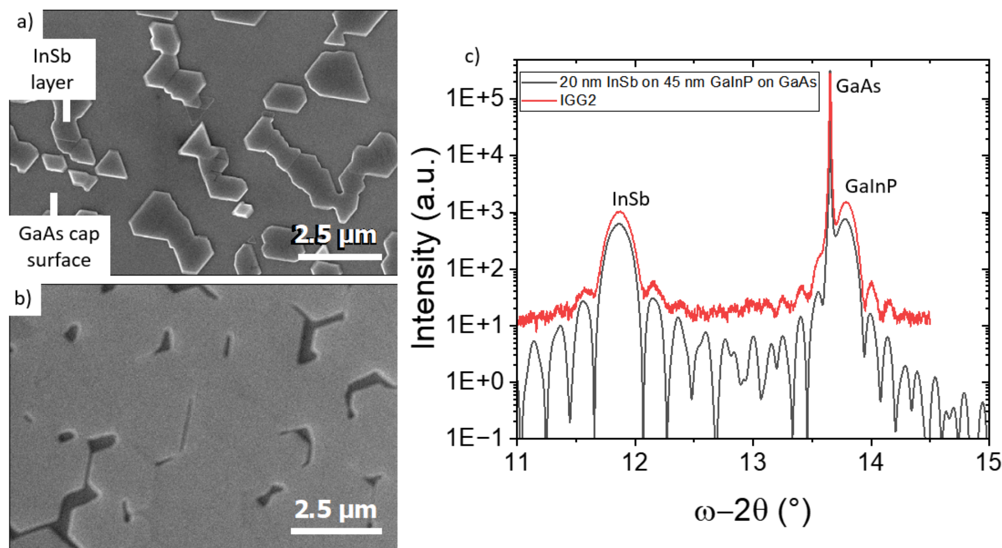


Figure 5.13: a) **SEM** image of **IGG1** b) **SEM** image of **IGG2**. c) Experimental and fitted **XRD** curves of sample **IGG2**.

Figure 5.13 shows **SEM** images of sample **IGG1** and **IGG2** surfaces as well as an **XRD** scan to assess the InSb film relaxation. The sample **IGG1** exhibits a morphology consisting of 3D InSb islands if we assume that the gray contrast in the background corresponds to the GaAs cap surface. Due to the 3D growth regime, the coverage of the surface is quite low (33 %) (Figure 5.13a). In contrast, for sample **IGG2** (Figure 5.13b) the InSb 20 nm-thick film wets uniformly the GaInP surface resulting in a smooth film with a low density of holes (95 % surface coverage). This striking difference between **IGG1** and **IGG2** suggests that the 5 nm-thin GaAs buffer layer on top of GaInP hinders the 2D growth of the InSb layer as previously observed for InSb/GaAs samples in chapter 4.

Looking into the **XRD** scan of sample **IGG2** in Figure 5.13c, the three layers can be clearly identified. The broad peaks correspond to the epitaxially grown 20 nm-thick InSb and 45 nm-thick GaInP while the GaAs $(111)_B$ substrate yields the sharp peak. From fitting the experimental data, the InSb layer is assumed to be 97 % relaxed for a thickness of 22 nm, meaning the InSb transitions rapidly into a smooth growth regime as confirmed in Figure 5.13b. Furthermore, the Pendellösung fringes visible on the **XRD** scan are not frequently observed on relaxed films, which further demonstrates the low interfacial roughness between the layers (InSb/GaInP and GaInP/GaAs) and their high crystalline quality.

5.3.3.2 Influence of the V-element overpressure used for the GaInP deoxidation

In this section, the InSb epitaxial growth on deoxidized GaInP thin films (grown beforehand on GaAs $(111)_B$) was investigated using either a P or As overpressure. As a reminder, the GaInP/GaAs substrates originates from the sample **GG1**.

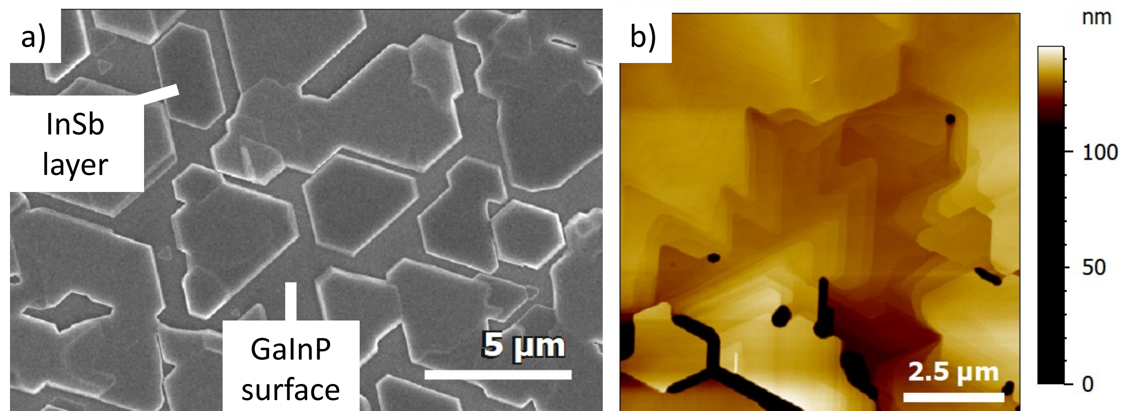


Figure 5.14: a) **SEM** image of **IGG3**. b) **AFM** image of **IGG4**.

The sample **IGG3** was deoxidized using a P flux (from the cracking of PH_3 in the **HTI** cell) to stabilize the GaInP surface in a P atmosphere before the growth of InSb as explained in the section 5.3.2. Sample **IGG4** made use of the deoxidation recipe using As before the growth of InSb, as described in the previous section 5.3.2 as well.

Figure 5.14a and b shows a **SEM** and an **AFM** image of samples **IGG3** and **IGG4** respectively. In the former case of sample **IGG3**, the 100 nm InSb layer grown on a GaInP surface deoxidized under P flux was not fully coalesced. The InSb 3D islands exhibit sharp faceted edges. Assuming again that the gray contrast between the 3D islands reflects the GaInP surface, the InSb coverage rate reaches 78% of the surface.

In contrast, the islands formed in sample **IGG4**, after the deposition of a 100 nm-thick InSb layer on a GaInP surface deoxidized under an As flux, rapidly merged into a smoother film with a small quantity of residual nanoholes. Due to the larger spreading of the InSb layer obtained on the As-deoxidized GaInP surface, the coverage rate reaches 97%. Overall, the general surface indicates a smoother aspect with no hillocks or strong height variations, suggesting that the As-surface preparation promotes the spreading of the InSb islands. Based on these observations, we can formulate two hypotheses explaining this difference relying upon the reduction of the interface energy: either it is due to a rougher interface after P-assisted deoxidation or to a reduced cost of the interfacial **MD** network between InSb and GaInP when an As flux is used during GaInP deoxidation, both hypotheses being potentially linked.

5.3.3.3 Influence of the growth temperature

In this part, we investigate the impact of the growth temperature on the InSb thin film morphology. For this study, we used samples **IGG5**, **IGG6**, **IGG7**, **IGG8** composed of a 20 nm-thick InSb film deposited on a GaInP/GaAs pseudo-substrate at 350, 365, 385 and 430 °C respectively (referenced in Table 5.4). We note that the GaInP/GaAs substrates were all deoxidized using the As-based surface preparation detailed previously. Figures 5.15a, b, c, and d present the **AFM** images of sample **IGG5**, **IGG6**, **IGG7** and **IGG8** respectively.

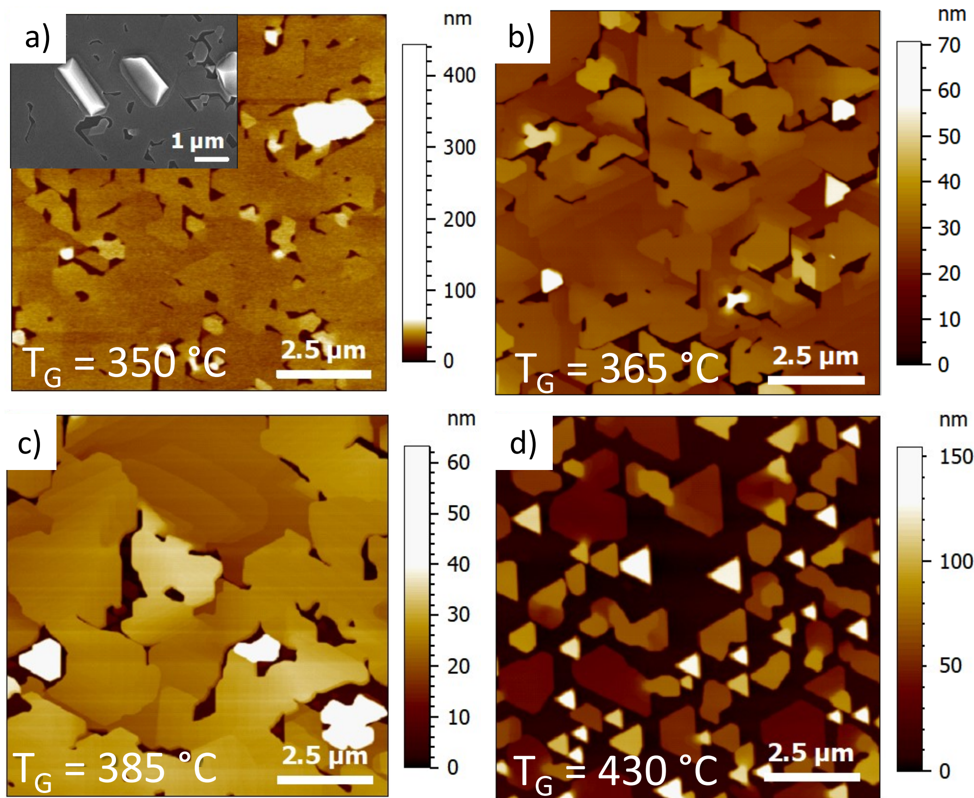


Figure 5.15: a) **AFM** image of sample **IGG5** grown at $\mathbf{T_G}$ = 350 °C. Inset: **SEM** image of **IGG5**. b) **AFM** image of sample **IGG6** grown at $\mathbf{T_G}$ = 365 °C. c) **AFM** image of sample **IGG7** grown at $\mathbf{T_G}$ = 385 °C. d) **AFM** image of sample **IGG8** grown at $\mathbf{T_G}$ = 430 °C.

Despite few unfilled areas and hillocks, the surface of **IGG5** in Figure 5.15a is rather smooth, covering 94 % of the surface. Nevertheless, at this temperature (350 °C), new defects appear, which are possibly Sb clusters visible as bright contrasted features above the InSb surface. The Sb chunk seen in the **AFM** image (white feature) of Figure 5.15a is around 400 nm high. The large Sb flux and the limited Sb desorption at such low growth temperature favors Sb clustering.

With increasing $\mathbf{T_G}$, the Sb clustering is suppressed as displayed for samples **IGG6** and **IGG7** in Figures 5.15b and c. Their surface shows a similar morphology, but without the occurence of Sb defects as high as the ones observed for **IGG5**.

Eventually, the last sample **IGG8** grown at 430 °C, contrasts with the other samples (Figure 5.15d). At elevated growth temperature, the InSb film shows a reduced coalescence on the surface (52 % coverage rate). The layer instead forms smaller but higher 3D islands up to 150 nm. The increased indium adatom mobility at high temperature is probably at the origin of the

reduction of the island density. The larger desorption rate of Sb at high temperature may also result in the reduction of the InSb (111) surface energy despite large Sb overpressure promoting 3D instead of 2D islands.

Conclusion

Through the different experiments performed in this section, key directions to grow smooth InSb thin films on a GaInP/GaAs pseudo-substrate were identified. Using optimized growth conditions for the GaInP buffer, the direct growth of InSb leads to a 95 % coverage of the surface and almost a full relaxation of the InSb layer (97 %) after a 22 nm-thick deposition from fitting the **XRD** experimental curve (sample **IGG2**). When the growth is performed after air exposure of the GaInP/GaAs pseudo-substrates, we have shown that a deoxidation under As flux results in a smoother morphology of the InSb film than using a P flux. In this case, an InSb thin film with a rather low density of nanoholes and hillocks has been obtained (**IGG4**), allowing one to consider the fabrication of bottom gated InSb/GaInP/GaAs nanostructures by **SAG**.

5.4 SAG of InSb NWs on GaInP/GaAs $(111)_B$

To realize in-plane InSb **NWs** prone to a charge carrier modulation, two possible options can be considered. As presented in Figure 5.16a, the first architecture relies on a dual-**SAG** where both III-V semiconductors are deposited during the same growth run on a patterned GaAs $(111)_B$ substrate. GaInP **NWs** are selectively grown first before the deposition of the InSb **NWs** on top. Such an option would enable the growth of InSb without any contact with the dielectric mask.

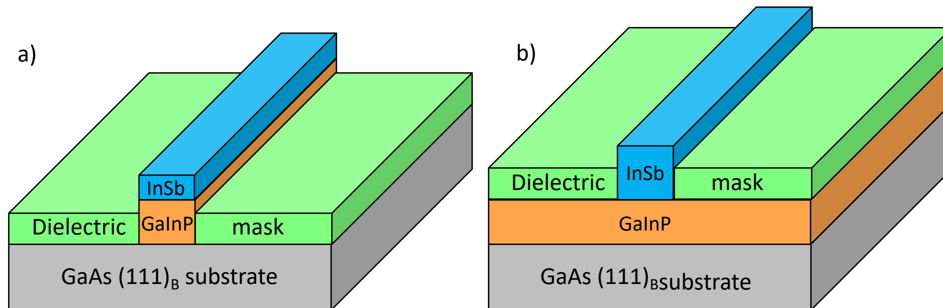


Figure 5.16: Schematics of the two pathways to grow in-plane InSb **NWs** on GaInP/GaAs $(111)_B$. a) The dual-**SAG** where both GaInP and InSb are grown by **SAG**. b) **SAG** of InSb on a 2D GaInP layer.

The second option implies that the GaInP layer is grown on GaAs before the mask fabrication to enable the **SAG** of InSb **NWs** within the mask apertures (Figure 5.16b). Nevertheless, this architecture could impact the roughness of the GaInP surface in the apertures through the mask fabrication process. As a reminder, the optimized growth conditions for 2D thin films, as detailed in the previous section, form the basis of our work. In the case of InSb, it corresponds to a low $\mathbf{V_G}$ of 0.05 **ML**/s, a high Sb/In ratio (136) and a $\mathbf{T_G}$ value in the 380 – 400 °C range. For GaInP, the following conditions are considered to be ideal in this work: $\mathbf{V_G}$ = 0.2 **ML**/s, V/III ratio of 50, a $\mathbf{T_G}$ value in the 510 – 520 °C range. Yet, these growth conditions will be subjected to change in case the obtained selectivity or morphology is not satisfying.

5.4.1 GaInP NWs on GaAs $(111)_B$

Before tackling the dual-**SAG**, it is important to certify that the lattice-matched GaInP **SAG** on GaAs $(111)_B$ produces smooth in-plane **NWs** with a high structural quality. The sample **SGG** was thus prepared using the same conditions than **GSG3** sample grown on a bare GaAs substrate: $\mathbf{V_G}$ = 0.2 **ML**/s, $\mathbf{T_G}$ = 520 °C, V/III ratio of 50, which resulted in a low surface roughness. For this experiment, the mask A process consisting of a single dielectric layer (SiO_2) was used for the mask fabrication.

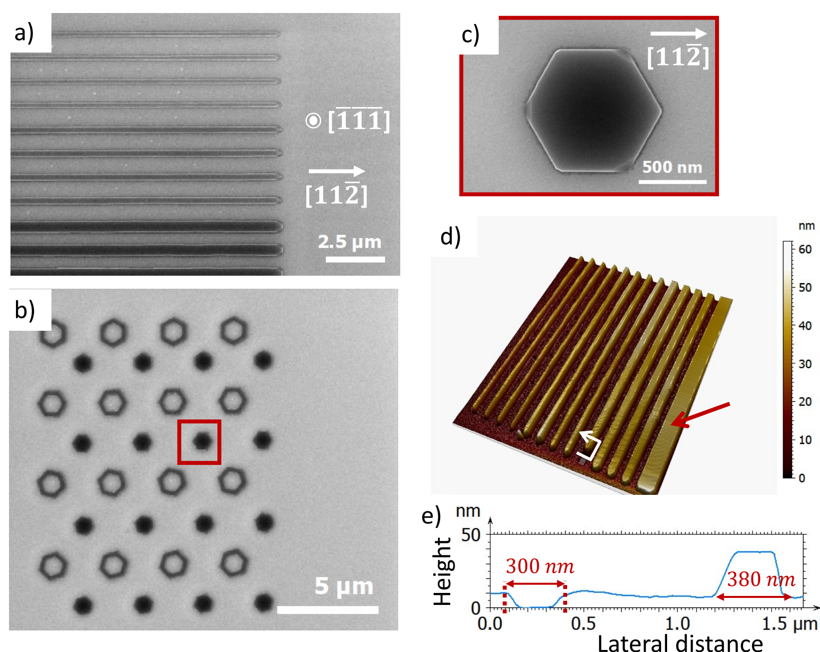


Figure 5.17: a) **SEM** image of [11$\bar{2}$]-oriented GaInP in-plane **NWs** on GaAs $(111)_B$ from sample **SGG**. From top to bottom, the **NWs** have different aperture widths (by set of four **NWs**): 50, 100, 200 nm. b) **SEM** image of hexagonal-shaped GaInP nanostructures grown on GaAs $(111)_B$ substrate. c) **SEM** image of a single hexagonal structure from the red colored box in b). d) **AFM** 3D image of similar structures. The red arrow points towards the GaInP terraces visible on the **NW**. e) Height profile corresponding to the white linepath in d).

Figure 5.17 shows **SEM** and **AFM** images of the 50 nm-thick in-plane GaInP **NWs** on GaAs $(111)_B$ substrate. At first, a high selectivity is noticed with no parasitic nucleation on the SiO_2 mask. The GaInP **NWs** displayed in the **SEM** image of Figures 5.17a, b and c exhibit a smooth morphology over the various aperture widths and shapes. They are all straight and faceted on their long sidewalls and ends as evidenced by the brighter contrast. Figure 5.17d shows the **AFM** 3D view of similar **NWs**. On the widest **NWs**, steps are visible on the top facets, when the reader magnifies the image. The observation of such steps indicates that a step-flow growth happens in these conditions. The white arrow represents a linepath going across both a 200 nm-wide aperture (in an area where no growth occured) and the GaInP **NW** whose height is around 40 nm. As evaluated from the height profile in Figure 5.17e), the SiO_2 aperture is significantly enlarged up to 300 nm compared to a nominal value of 200 nm. This is attributed to both the HF wet etching and the increased e-beam dose due to the proximity of the other patterns. For this experiment, the sample was probably slightly over-etched before introduction into **UHV** as only 10 nm of SiO_2 remains according to the **AFM** profile. We can thus deduce that GaInP overpasses

the thickness of the mask with a lateral growth of ~40 nm over each side of the aperture. Based on the results of this experiment, the subsequent InSb **SAG** on in-plane GaInP **NWs** on GaAs $(111)_B$ can now be considered for the full heterostructure.

5.4.2 InSb/GaInP NWs on GaAs $(111)_B$

In this study, GaInP was first deposited in the mask aperture with a thickness of 45 nm, *i.e.* higher than the height of the dielectric mask. Therefore, we expect that the growth of InSb will not be laterally confined by the dielectric. The sample **SISGG** was grown in the following conditions for GaInP: $\mathbf{V_G}$ = 0.2 **ML**/s, V/III ratio = 50, $\mathbf{T_G}$ = 520 °C and InSb: $\mathbf{V_G}$ = 0.05 **ML**/s, V/III ratio = 136, $\mathbf{T_G}$ = 375 °C. The thickness of the InSb layer is 20 nm. For this experiment, the $\mathbf{H_{AT}}$ plasma was added during the growth and we noted that after the GaInP growth, a (2×2) **RHEED**, associated with a Sb-rich surface was observed on the bare maskless substrate (simultaneously grown). Furthermore, the mask A process was used for this sample, which corresponds to a SiO_2 mask only.

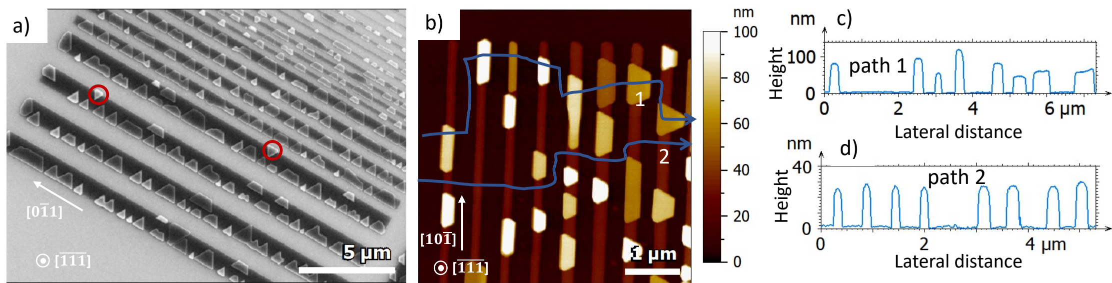


Figure 5.18: a) **SEM** image of [0$\bar{1}$1]-oriented **NWs** with different aperture widths in sample **SISGG**. The red circles highlights twinned InSb islands. b) **AFM** image of sample **SISGG** on [10$\bar{1}$]-oriented **NWs**. The blue line paths correspond to height profiles in c) for the InSb islands in line 1 and d) GaInP **NWs** in line 2 respectively.

As imaged in Figure 5.18a, the InSb layer forms 3D islands on the **SAG** patterns whatever their width is (structures detailed in Annex A, Figure A.2). In Figures 5.18c and d, two height profiles are defined in the **AFM** image to estimate the difference between InSb and GaInP: the path 1 crosses InSb islands while the path 2 goes through GaInP **NWs** only. From these profiles, the InSb 3D islands height ranges between 44 and 118 nm higher than the SiO_2 mask. Conversely, the GaInP **NWs** are around 25 nm higher than the mask surface, which agrees well with the 45 nm nominal layer thickness and the 20 nm thickness of the mask after HF etching. In terms of lateral dimensions, in the narrowest apertures (50 nm nominal width), the GaInP **NWs** mean width is about 180 nm while the InSb islands on top are as large as 290 nm. In the apertures with a 100 nm nominal width, the GaInP and InSb are about 270 and 480 nm-wide respectively (mean values). The discrepancy with respect to the nominal width of the apertures is partially due to the enlargement induced by HF wet etching but also the larger e-beam dose due to proximity effects. Hence, the lateral growth over the mask for both GaInP and InSb is eased, consistently with the observations of GaInP **NWs** from section 5.4.1 and InSb **NWs** cross-sections in the chapter 4 section 4.4.2.

Eventually, the **SEM** image in Figure 5.18a provides additional information regarding the InSb 3D islands growth. From the larger openings, we can see that most of the islands nucleate from one side of the GaInP patterns with a characteristic triangular shape. A few 180° rotated InSb islands nucleating from the other side facet of the GaInP **NWs** are also visible (red circles in Figure 5.18a), giving the impression that the orientation of the twin domains could be related to

the initial orientation of the GaInP surface. These observations supports the fact that the initial surface roughness of the GaInP layer has a strong impact on the InSb growth mode.

To conclude upon this dual-**SAG** experiment, neither the slightly lower growth temperature nor the possibly Sb-rich GaInP surface could be held responsible for the 3D islands growth mode obtained for InSb on GaInP **SAG** patterns. The preferential nucleation of InSb on the side facets of GaInP rather confirms that an initial flat (111) GaInP or GaAs surface is required to achieve the 2D growth mode observed in section 5.3.3.3. In the following, we will thus try to keep the GaInP surface as smooth as possible by fabricating the mask on a GaInP/GaAs pseudo-substrate.

5.4.3 InSb NWs on 2D GaInP on GaAs

For this section, as schematized in Figure 5.16b, the InSb **SAG** on patterned GaInP/GaAs pseudo-substrates is investigated. In this configuration, InSb nanostructures are initially confined inside the mask aperture. A part of 100 nm GaInP/GaAs $(111)_B$ **GG1** and **GG2** samples (surface morphology presented in Figure 5.6) have been used for the patterned substrates preparation. The remaining part of **GG1** was kept unpatterned for **RHEED** monitoring purposes, simultaneously with InSb **SAG**. When it is the case, it is mentioned in the last raw of Table 5.5 that summarizes all the growth conditions for this study. Otherwise, this means a GaAs $(111)_B$ substrate was used for **RHEED** monitoring. All samples are grown under a $\mathbf{H_{AT}}$ exposure during **SAG**.

Sample	**SIGG1**	**SIGG2**	**SIGG3***	**SIGG4***	**SIGG5***	**SIGG6***
GaInP 2D layer ref.	**GG1**	**GG1**	**GG2**	**GG2**	**GG2**	**GG2**
$\mathbf{V}_{\mathbf{G}\,InSb}$ (ML/s)	0.05	0.05	0.05	0.05	0.05	0.05
V/III ratio	136	136	136	136	136	136
$\mathbf{T_G}$ (°C)	385	365	380	390	400	390
$t_{nominal}$ (nm)	20	20	50	50	50	100
Reference 2D sample for **RHEED**	**GG1**	**GG1**	GaAs $(111)_B$	GaAs $(111)_B$	GaAs $(111)_B$	GaAs $(111)_B$

Table 5.5: Growth conditions for the **SAG** of InSb on GaInP/GaAs patterned substrates. Samples with * were grown using the mask B process *i.e.* Al_2O_3/SiO_2 dielectric mask whereas mask A process was used for the other samples.

5.4.3.1 Influence of the growth temperature

The first sample **SIGG1** was grown in the conditions optimized for the **SAG** of InSb on patterned GaAs substrate ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 385 °C, V/III ratio of 136). Figure 5.19a) presents the resulting morphology obtained for the growth inside $[1\bar{1}0]$-oriented patterns with different aperture widths. As expected, a quite good selectivity is reached in these growth conditions with almost no nucleation on the mask.

Independently from the aperture width, a 3D island growth regime is observed. The different contrasts in the **SEM** images help to identify uncovered GaInP surface (darker areas) and InSb islands with different shapes. Inside apertures larger than 500 nm (four openings at most left), two types of InSb islands can be found. The brighter ones correspond to pyramidal islands with

a triangular shape. An **AFM** scan on one of these islands reveals a height of about 160 nm and a shape composed of a small {111} top facet delimited by two {100} facets as well as a narrow high-index {311} facet that forms a 30° angle with the base plane (Figure 5.19b). In contrast to the islands observed for **SISGG** in Figure 5.18a, their nucleation site does not occur at the edge of the aperture only. Regarding the darker islands, they seem lower and more spread with an enlarged top (111) surface.

Inside the narrowest apertures below 500 nm (three apertures at most right of the Figure 5.19a), both types of islands remain but the geometrical confinement of the growth enlarges the shape of the InSb islands along the main aperture axis. However, these segments are not sufficiently long to fill the full aperture area.

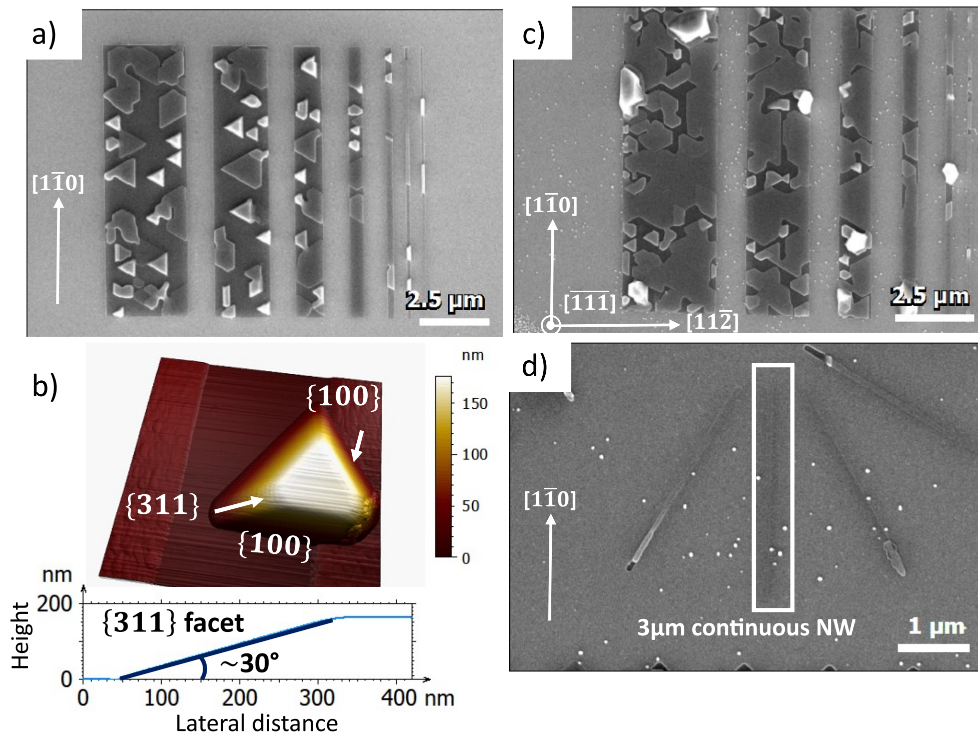


Figure 5.19: a) **SEM** image of InSb [1$\bar{1}$0]-oriented **NWs** arrays on sample **SIGG1**. b) **AFM** image (3D view) of sample **SIGG1** highlighting a typical triangular InSb island. White arrows point to the two types of observed facets: the {311} facet being determined from the height profile below. c) **SEM** image of InSb [1$\bar{1}$0]-oriented **NWs** arrays on sample **SIGG2**. d) **SEM** 3 µm-long apertures in sample **SIGG2**.

For sample **SIGG2** (Figure 5.19c), the growth at reduced $\mathbf{T_G}$ (365 °C) increases the spreading of InSb and the coalescence of 2D islands while decreasing the density of 3D islands. For the narrowest apertures, InSb almost completely covers the GaInP surface with only a very few clusters or clipping along the 10 µm-long openings. The wider **NWs** have fewer islands (bright contrasted features) and the coalescence of the InSb layer increased also with a reduced density of unfilled areas. For areas where shorter apertures were designed (Figure 5.19d), the **NWs** are mostly continuous up to 3 µm. Although still satisfactory, this improvement of the InSb film morphology with the reduction of the growth temperature also leads to a slight degradation of the selectivity as some very small clusters can be observed on the SiO_2 mask on Figures 5.19c) and d.

In conclusion, we found a slightly different growth temperature optimizing the 2D nucleation of InSb on patterned GaInP/GaAs substrate with respect to the growth on a mask-less GaInP/GaAs or a patterned GaAs $(111)_B$ wafer. The difference of 20 °C between the two kind of samples is close to the precision limit that we could expect with the pyrometer measurement. Furthermore, the temperature being estimated from the infrared emission of the surface of the reference sample during the growth, the change of emissivity between a GaInP and a GaAs surface may also have an impact on this measurement and explain the small deviation.

5.4.3.2 InSb growth inside a deeper dielectric mask

In order to increase the nominal thickness of InSb while limiting lateral overgrowth, we used the mask B process (Al_2O_3/SiO_2 double dielectric layer) to get deeper apertures, although we have shown in the previous chapter that it yields to a decrease of the selectivity. Based on the promising results from sample **SIGG2**, the InSb film thickness is increased to 50 nm to compare the growth morphology above the mask surface. As the reference sample from which the temperature is estimated is no more a GaInP/GaAs pseudo substrate but a bare GaAs substrate, we explored a range of temperature between 380 °C and 400 °C. We note that the underlying GaInP surface corresponds to sample **GG2**. The reason for the change of GaInP/GaAs substrate only comes from the fact that sample **GG1** was entirely consumed and no more parts were left to do these **SAG** experiments.

Figure 5.20 presents arrays of **NWs** with different orientations and magnifications of the **SEM** images for the three samples with a 50 nm InSb thickness, namely **SIGG3**, **SIGG4** and **SIGG5**. Consistent with the results obtained in the previous chapter for the **SAG** of InSb nanostructures on GaAs $(111)_B$ the selectivity rate greatly decreased, especially for the sample **SIGG3** grown at 380 °C (see Figure 5.20a). This could be attributed to a combination of three phenomena: (i) the increased thickness of the InSb film with respect to previous experiments, (ii) the use of a GaAs substrate as a reference sample for the temperature measurement and (iii) the mask process change, as we have shown in chapter 2 section 2.2.5 that the roughness of the SiO_2 layer without HF chemical etching seriously impacts the selectivity.

Despite the selectivity decreased, the in-plane growth of the InSb **NWs** improves with a larger success rate of smooth and continuous **NWs** as displayed in Figures 5.20d. Most of the **NWs** grew with high structural quality independently of the aperture width. From Figure 5.20g that depicts a sun-shape of 3 µm-long **NWs** having all the same aperture width, a clear crystallographic orientation dependence is visible. The <11$\bar{2}$>-oriented ones, which correspond to **NWs** making an angle of $n\pi/3$ ($n \in \mathbb{N}$) with respect to the horizontal axis, are more defective. Some apertures are filled with islands having a rhombus shape much larger than the aperture size. When the apertures are fully filled with InSb, the **NWs** show different contrasts along their length which are caused by segments of different heights. Conversely, the <1$\bar{1}$0>-oriented **NWs** show a higher quality and look also thinner.

In order to improve the selectivity, the growth temperature was raised. Samples **SIGG4** and **SIGG5** were respectively grown at 390 and 400 °C (Figures 5.20b and c). The comparison of the number of bright clusters seen on the dielectric mask between samples **SIGG3**, **SIGG4** and **SIGG5** clearly shows the benefit of a higher temperature: an increase in $\mathbf{T_G}$ helps re-evaporating the adatoms on the dielectric mask. The structural quality of the **NWs** for all three samples is similar as an identical yield is obtained for [0$\bar{1}$1]-oriented **NWs** (11 are "smooth" out of 16) as well as a limited lateral overgrowth (for the 100 nm-wide apertures, the mean width is ∼150 nm) when the structures in Figures 5.20d, e and f are compared. Moreover, a dependency on their orientation is again observed, indicating that a change of growth temperature in sample **SIGG4**

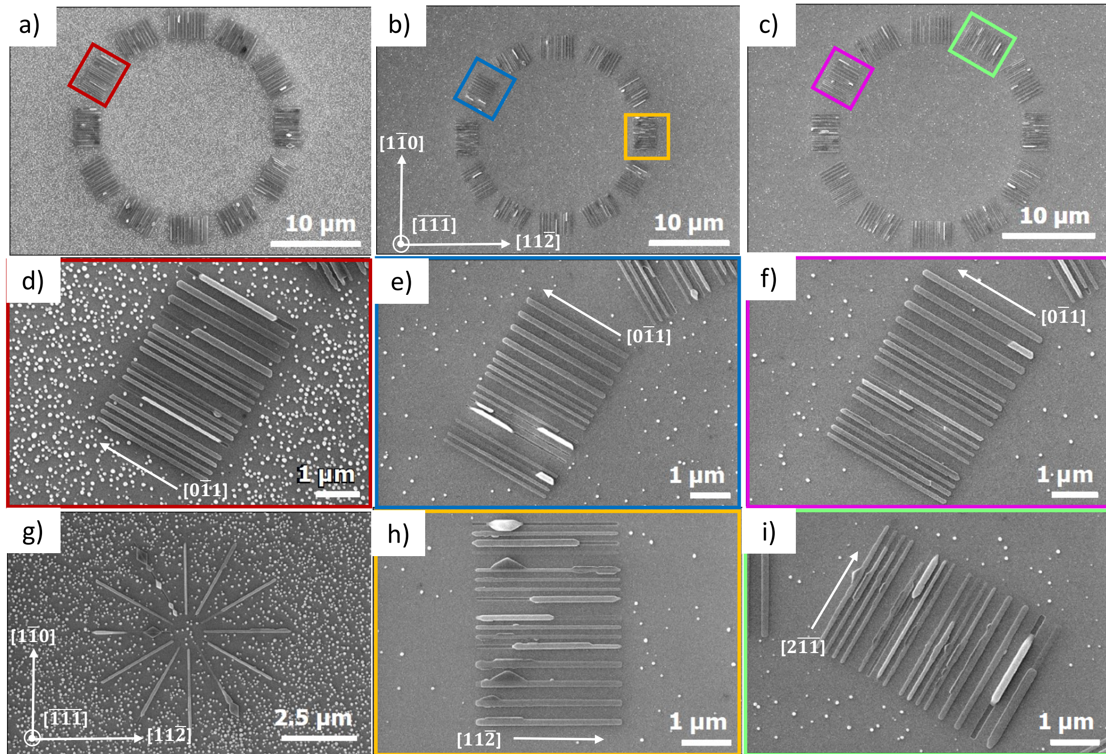


Figure 5.20: **SEM** images of the second sun-shape version in a) sample **SIGG3**, b) **SIGG4**, c) **SIGG5**. d) 3 µm-long in-plane InSb **NWs** array from the red box in a). Aperture widths are 30, 40, 50 and 100 nm from the bottom to the top (for each aperture there is a set of four **NWs**). e) **NWs** array seen in the blue box in b) for sample **SIGG4**. f) **NWs** array magnified from the pink box in c) for sample **SIGG5**. g) 3 µm-long in-plane InSb **NWs** in a sun-shape from sample **SIGG3**. h) 3 µm-long in-plane InSb **NWs** array from the yellow box in b). i) **NWs** array from the green box in c) for sample **SIGG5**.

or **SIGG5** does not modify the result obtained for sample **SIGG3**: $[0\bar{1}1]$-oriented **NWs** are straight and continuous (Figure 5.20e) whereas the $[11\bar{2}]$ apertures have a lower success rate to give a uniform segment. These **NWs** usually face larger lateral overgrowth (Figure 5.20h).

Similar conclusions can be drawn for sample **SIGG5** when the Figure 5.20f) and i) are compared for $<11\bar{2}>$ and $<1\bar{1}0>$-oriented **NWs** respectively. We note that these observations are consistent with the results obtained in the chapter 4 (section 4.4.2) for InSb in-plane **NWs** on GaAs $(111)_B$, where the $<11\bar{2}>$-oriented **NWs** showed a larger lateral overgrowth than the $<1\bar{1}0>$-oriented **NWs**. This result indicates the following generality: the introduction of a GaInP intermediate layer does not affect the InSb growth regime compared to its growth on GaAs $(111)_B$.

Eventually, looking at Figure 5.21a and b, the major achievement of this work is observed: 10 µm-long in-plane InSb **NWs** on a GaInP/GaAs $(111)_B$ substrate are obtained without any disruption. We note that the optimal growth conditions require a higher $\mathbf{T_G}$ in comparison with the samples grown with mask A process (**SIGG1**, **SIGG2**). As already mentioned in chapter 4 this difference of growth temperature is due to the higher roughness of the SiO_2 layer as a result of mask process B that requires a stronger heating to obtain a similar selectivity.[247]

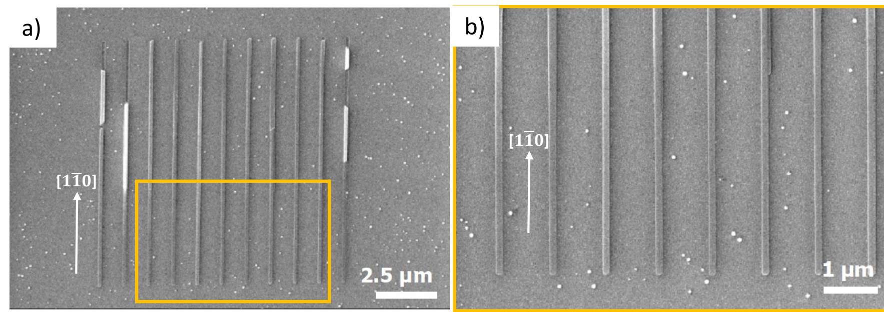


Figure 5.21: a) **SEM** image of an array of [1$\bar{1}$0]-oriented **NWs** that are 10 µm-long in sample **SIGG4**. b) Magnified view on the **NWs** from the yellow box in a).

5.4.3.3 Evolution of the NW morphology for a larger InSb thickness

The last experiment, through sample **SIGG6**, focuses on the influence of the film thickness on the InSb **NW** morphology. In this case, the InSb nominal thickness is significantly larger than the mask depth (100 nm with respect to 35 nm). As seen in Figure 5.22a the InSb **NWs** of the sun-shape array are mostly smooth except for the <11$\bar{2}$>-oriented **NWs** which appear more frequently disrupted or largely overgrown on the mask surface. The selectivity remains satisfactory and identical to the one of sample **SIGG4** and **SIGG5** in spite of the increased InSb thickness (100 nm vs 50 nm).

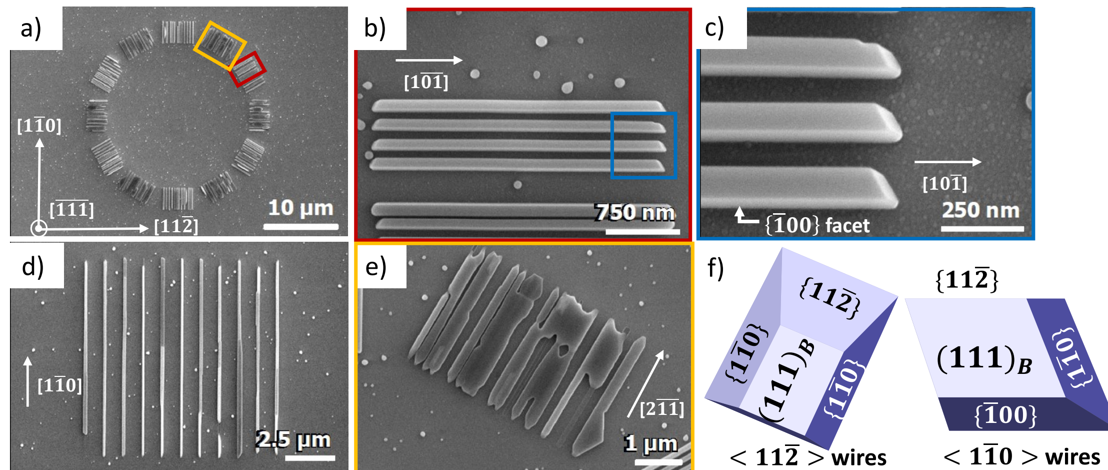


Figure 5.22: a) **SEM** image of **NWs** grown in the second sun-shape version of sample **SIGG6**. b) Rotated **SEM** image of [10$\bar{1}$]-oriented **NWs** from the redbox in a). The **NWs** nominal aperture width is 30 nm. c) Further zoom from the blue box in b). The clear trapezoidal geometry of the in-plane InSb **NWs** is visible with well defined facets. d) **SEM** image of [1$\bar{1}$0]-oriented 10 µm-long **NWs** (nominal aperture width 30 nm). e) **SEM** image of [2$\bar{1}\bar{1}$]-oriented **NWs** from the yellow box in a). f) Schematic representation of two differently oriented **NWs** grown on a $(111)_B$ substrate. Reproduced from[215].

Focusing onto [10$\bar{1}$]-oriented **NWs** visible in the Figures 5.22b and c, an asymmetric trapezoidal section can be seen, which was less easily observable in previous samples **SIGG4** and **SIGG5**. Here, the thicker region formed out of the mask surface is able to develop low energy facets. From Figure 5.22f, this geometry is well defined with a {$\bar{1}$00} slanted facet on one side and a vertical {11$\bar{2}$} facet on the other for <1$\bar{1}$0> **NWs**. The lateral overgrowth remains acceptable as

the average **NW** width is ~120 nm, knowing that the 30 nm nominal aperture already enlarged after the patterning process. For <11$\bar{2}$>-oriented **NWs**, we confirm as well the observation of two vertical {1$\bar{1}$0} facets forming here a rectangular section (visible on the **NW** at most right in Figure 5.22e) as schematized in Figure 5.22f. Additionally, along this [2$\bar{1}\bar{1}$] orientation, the **NWs** exhibit a significant lateral overgrowth leading in this case to the merging of few **NWs** over the SiO_2 mask surface.

Lastly, Figure 5.22d shows that the high success rate for the fabrication of continuous **NWs** is not limited to short aperture lengths. Even for a length of 10 µm, the increase of the InSb thickness, leads to the formation of high quality **NWs** along the [1$\bar{1}$0] direction with similar lateral overgrowth (for the smooth **NWs**) than the 3 µm-long apertures in Figure 5.22b.

5.4.4 Scanning transmission electron microscopy of the InSb NWs

5.4.4.1 Transverse cross-sectional analysis

While the lateral facets of the **NWs** are imaged with **SEM** when their thickness is 100 nm (sample **SIGG6**), a growth corresponding to a thickness of 50 nm makes the identification of their cross-section with **SEM** more difficult (sample **SIGG4**). Therefore a cross-sectional study of the **NW** is preferred. Figure 5.23a shows a **SEM** image of another sun-shape structure grown on sample **SIGG4**. The **STEM** lamella was cut along the [11$\bar{2}$] direction across an array of [1$\bar{1}$0]-oriented **NWs** that includes both smooth **NWs** and 3D islands. The large scale **STEM** image of this cross-section is shown in Figure 5.23b. It highlights different morphologies of InSb in-plane **NWs** grown on the GaInP/GaAs heterostructure.

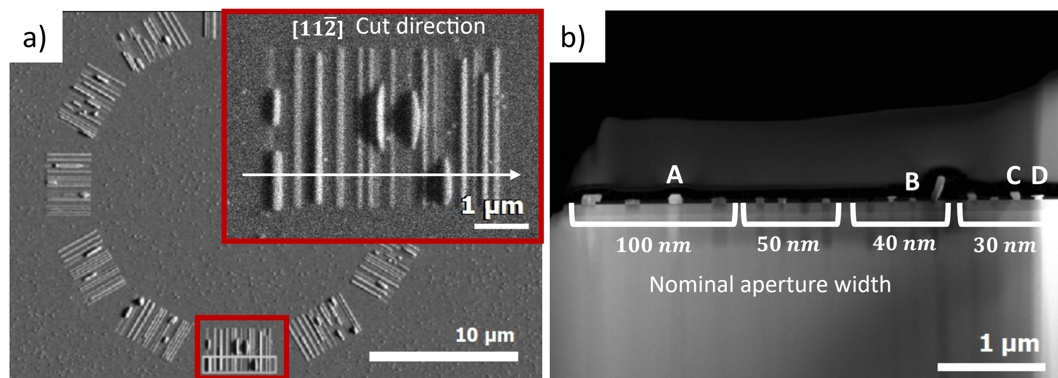


Figure 5.23: a) **SEM** image of **NWs** grown in the second sun-shape version on sample **SIGG4**. Inset: Higher magnification **SEM** image showing the cut direction of the lamella. b) Large **STEM** view of the lamella. The label A, B, C, D refer to a selection of **NWs** with specific cross-sectional shapes. The zone axis is [1$\bar{1}$0].

We start the study of the structural quality of the heterostructure with the observation of high-resolution **HAADF**-**STEM** images acquired at the GaInP/GaAs interface on this sample. In Figure 5.24, the GaInP and GaAs layers appear dark and bright respectively. Based on the sharp change of the contrast seen between both layers, the interface takes place over one atomic layer. It is therefore abrupt. By performing a [$\bar{1}$11]-filtered **FFT** and then an inverse **FFT** image at the position of the interface, no dislocation is seen. In our case, although the 2D GaInP layer grown from sample **GG2** was found to be slightly In-rich from the **XRD** analysis described in section 5.2.2.4, the very low lattice-mismatch induced by this In enrichment does not cause the formation of defects at the interface or in the GaInP layer.

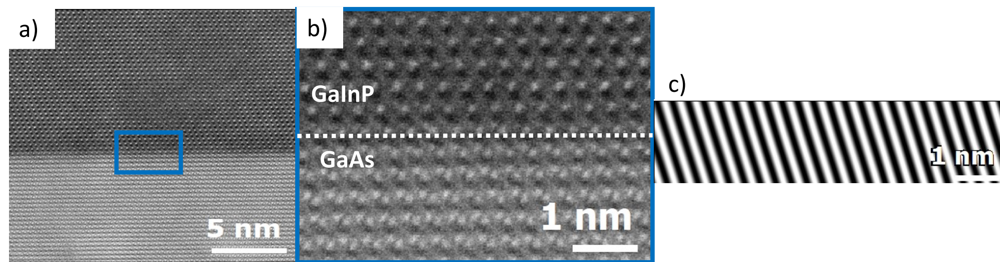


Figure 5.24: a) **STEM** image of the GaInP/GaAs interface, b) magnified view of the blue box in a) showing the atomically abrupt interface. c) $[\bar{1}11]$-**FFT** filtered and inverse **FFT** image of the GaInP/GaAs interface.

Now that we confirmed the high interface quality between GaInP and GaAs, we can go back onto the InSb in-plane **NWs** discussion. Figure 5.25 shows higher magnification **STEM** images of the different **NWs** morphologies. When the InSb is selectively grown on a GaInP surface, significant changes in the morphology are observed for several **NWs**, which highlights a different behavior compared to the InSb **SAG** directly on GaAs $(111)_B$ substrates (chapter 4, section 4.4.2). As shown in Figure 5.25, while smooth **NWs** with a flat top surface are still obtained (labeled B), some of the **NWs** display instead either well-defined facets, 3D growth regime or lateral overgrowth once the mask surface level is reached. Nevertheless, it is important to mention that the nominal aperture width does not seem to impact the growth regime as the different types of **NWs** can be found along the varying aperture widths (Figure 5.23b).

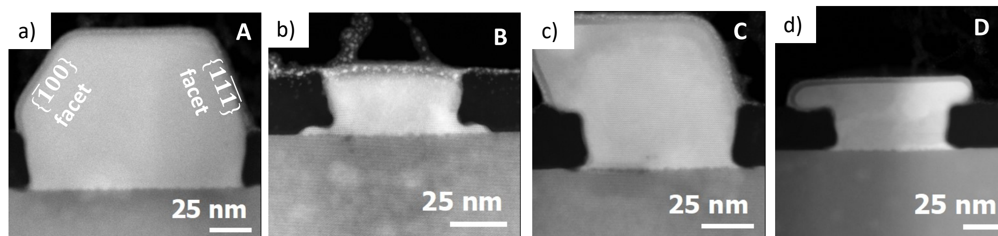


Figure 5.25: **STEM** images of a a) faceted 100 nm-wide **NW**, b) 40 nm-wide smooth **NW** with no lateral overgrowth and a flat top surface, c) 30 nm-wide **NW** that presents 3D growth, facets and lateral overgrowth on the mask and d) 30 nm-wide **NW** with lateral overgrowth.

InSb crystal quality among the different NWs morphologies

Focusing on the smooth **NW** (labeled B) in Figure 5.26a, a periodic **MD** network is formed at the InSb/GaInP interface due to the important lattice mismatch between InSb and GaInP (f = 14.6 %, similar to the one of the InSb/GaAs system). The position of the **MDs** are highlighted for instance in the $[\bar{1}11]$-filtered **FFT** and inverse **FFT** image of Figure 5.26a by the yellow circles. The **MDs** are repeated with a mean spacing of 2.7 nm along the $[11\bar{2}]$ direction consistent with the one found at the InSb/GaAs interface.[100] While some **SFs** near the InSb/GaInP interface are observed, which is consistent with similar observations for InSb **NWs** on GaAs (chapter 4), the InSb/GaInP interface appears to be rougher in this system. Yet, away from the interfacial region, the heart of the InSb **NW** is free from planar defects as shown in Figure 5.26c, for another smooth **NW** (50 nm-wide aperture). Near the surface of the **NW**, planar defects are evidenced as in Figure 5.26b, but the presence of InSb native oxide coupled to the **FIB** preparation process are deemed to be correlated to their formation because it was consistently observed for all **NWs** in this lamella.

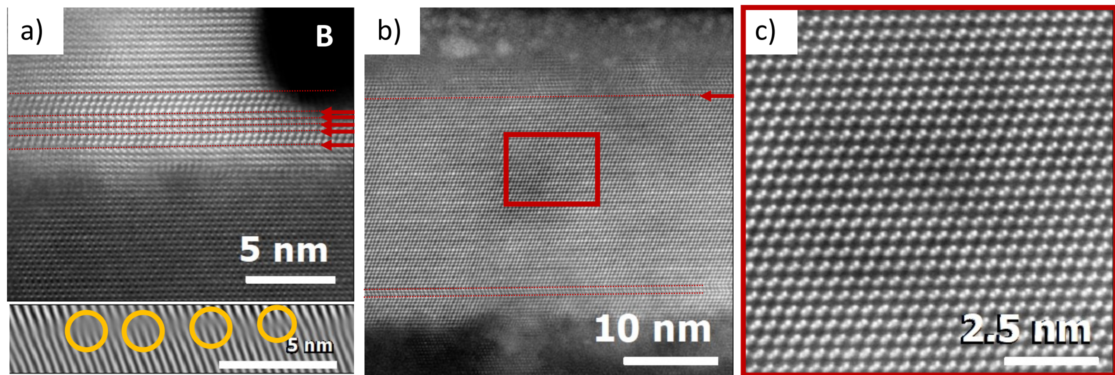


Figure 5.26: a) **STEM** image of the 40 nm-wide smooth **NW** "B", where red arrows are showing **SF**s in the InSb layer. Below is a [$\bar{1}$11]-**FFT** filtered and inverse **FFT** image of the InSb/GaInP interface showing the **MD** network (yellow circles). b) Low magnification **STEM** image of another smooth **NW**, with a 50 nm nominal aperture width, to show the interfacial region as well as the sub-surface area. c) Higher magnification **STEM** image of the central area of the smooth **NW** from b) (red rectangle box).

For the InSb **NWs** displaying a different morphology, the cross-sectional analysis revealed also the presence of a **MD** network at the interface as well as **SF**s (Figures 5.27a and b). While the density of **SF**s appeared to vary along the **NW** thickness, supplementary crystalline defects were observed. As shown in Figure 5.27, both the faceted **NW** and the one with lateral overgrowth (C and D) exhibit an isolated dislocation along the ($\bar{1}\bar{1}\bar{1}$) plane. While in the former case, it is caused by the intersection of complex twins which propagate through the InSb layer, no surrounding additional defects are found for the latter **NW** in Figure 5.27b. In this regard, we believe these emerging crystal defects may affect the final morphology of the **NWs**.

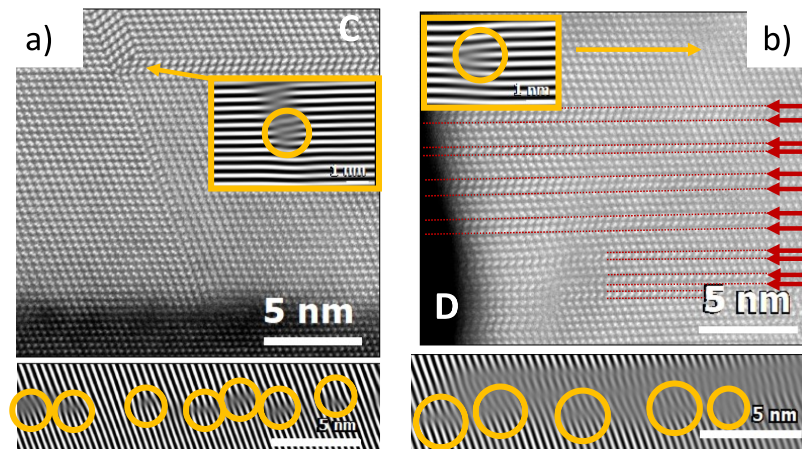


Figure 5.27: **STEM** images of: a) The 30 nm-wide **NW** (C) and b) The 30 nm-wide **NW** with the morphology D. On all images, red arrows are showing **SF**s in the InSb layer. In the **STEM** images b) a dislocation is seen at the intersection of a complex twin in the inset ([$\bar{1}\bar{1}\bar{1}$]-**FFT** filtered and inverse **FFT** image). The inset of **STEM** image b) shows an isolated dislocation ([$\bar{1}\bar{1}\bar{1}$]-**FFT** filtered and inverse **FFT** image). Below all **STEM** images, is a [$\bar{1}$11]-**FFT** filtered and inverse **FFT** image of the InSb/GaInP interface showing the **MD** network (yellow circles) is shown.

The impact of the mask process on the formation of defects was also assessed through a **STEM** cross-sectional analysis (available in appendix C) on a lamella prepared from sample **SIGG2** that made use of mask A process (SiO_2 only). Despite smooth and more faceted (3D-like) **NWs** were investigated, as shown in Figures C.1c and d, similar **MD** networks were observed as well as **SF**s in both cases. Several **NWs** exhibited a 180° rotation of the InSb crystal at the InSb/GaInP interface which persists until the top InSb surface as observed in Figure C.1f and C.2c. While such phenomenon clearly affects the type of facets formed, thus the nanostructures shape, it seems not correlated to the growth regime nor to the mask process as this was observed as well in smooth **NWs** (Figure C.1e and Figure C.2b).

5.4.4.2 Longitudinal cross-sectional analysis

Following the **STEM** analysis performed across the width of the **NWs**, a lamella was prepared by cutting the **NW** longitudinally for a 20 µm-long, 50 nm-wide $[1\bar{1}0]$-oriented **NW** grown on sample **SIGG2**. In the **SEM** image of 5.28a, the selected **NW** is protected and the protective shell gives a much larger width than the ones seen for its neighbors. We choose a **NW** exhibiting disruptions and islands to investigate their origin. Hence, the lamella on Figure 5.28b shows isolated regions corresponding to different InSb segments.

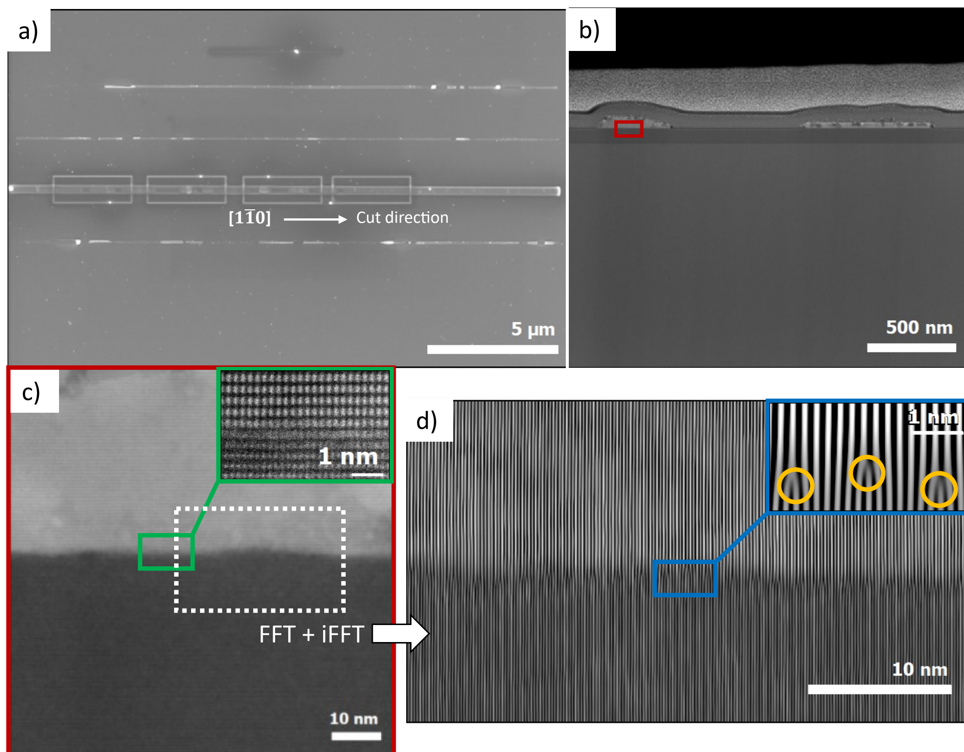


Figure 5.28: a) **SEM** image of a 20 µm-long InSb **NW** in sample **SIGG2** during **FIB** lamella preparation, b) large scale **STEM** image of the $[1\bar{1}0]$-oriented **NW** cut along its length. The zone axis is $[11\bar{2}]$. c) Zoom at smaller scale from the red box in b). Inset in the green box shows a magnified view allowing the visualization of atomic planes along this $[11\bar{2}]$ zone axis. d) $[1\bar{1}0]$ filtered **FFT** and reconstructed image of the white dotted box in c). The periodic **MD** array is evidenced at the interface. The blue box inset shows a magnified view of the regularly spaced dislocations (yellow circles).

Focusing on the InSb/GaInP interface in Figure 5.28c, the **STEM** image reveals a quite important roughness along the interface. Looking at the magnified view of the interface in the green box (inset), the atoms arrangement of this $[11\bar{2}]$ zone axis can be distinguished. In this crystal orientation, the **SF**s cannot be observed as the $[1\bar{1}0]$ horizontal direction is a mirror plane (while the $[11\bar{2}]$ direction was not for the lamellae cut along the width).

From the white dotted box in Figure 5.28c, the **MD** network at the interface between InSb and GaInP can be revealed using a $[1\bar{1}0]$ filtered **FFT** and inverse-**FFT** image (Figure 5.28d). From the magnified image in the blue inset, the regular dislocation spacing equals 1.5 nm along the $[1\bar{1}0]$ direction. This reduced spacing is consistent with the denser atomic stacking, which enhances the projected dislocation density in this viewing direction.

5.4.4.3 Impact of the substrate on the NW structural quality

Based on all the **SEM** and **STEM** investigations of the InSb **NWs** grown either on the GaAs $(111)_B$ substrate or on the GaInP/GaAs $(111)_B$, it is possible to determine the influence of the substrate on the **NW** structural quality.

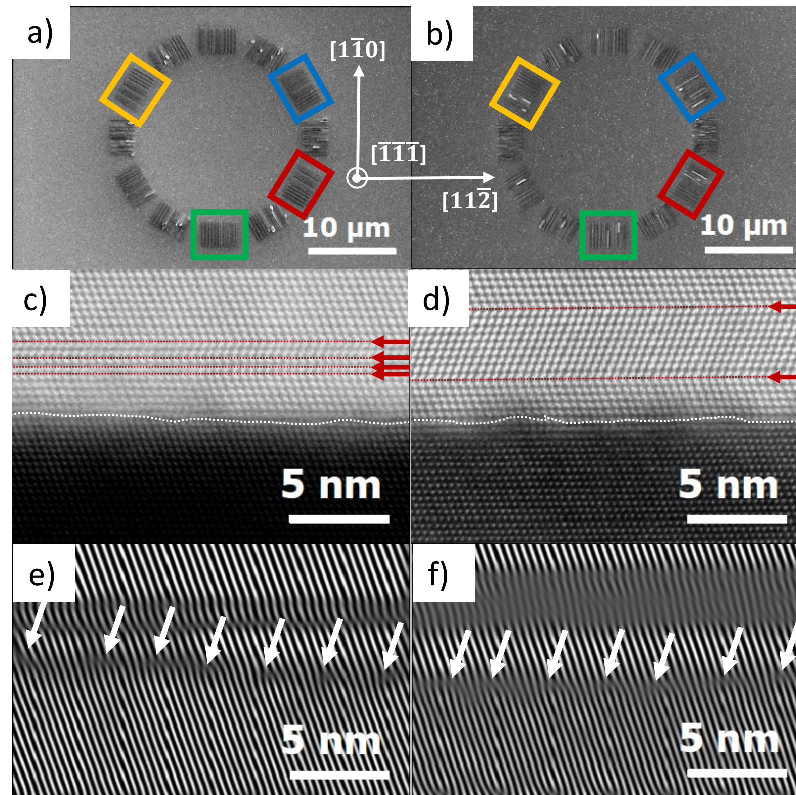


Figure 5.29: **SEM** image of a sun-shape structure from a) sample **SIG3** and b) sample **SIGG4** . The color boxes highlights the difference in the InSb **NWs** growth morphology along the main crystallographic orientation family <1$\bar{1}$0>. c) **STEM** image of the 100 nm wide InSb **NW** on GaAs with **SF**s indicated by the red arrows. d) **STEM** image of the faceted 100 nm wide **NW** A with **SF**s indicated by the red arrows. The white dotted line suggests the interface between the two materials. e) $[\bar{1}11]$-**FFT** filtered and inverse **FFT** image of the InSb/GaAs interface highlighting the periodic **MD** network. f) $[\bar{1}11]$-**FFT** filtered and inverse **FFT** image of the InSb/GaInP interface highlighting the periodic **MD** network.

Figure 5.29a and b presents two sun-shape structures acquired for sample **SIG3** and **SIGG4** that were fabricated together during the same **MBE** growth run (both samples were glued on the Si carrier). As a reminder, the growth conditions are the following: $\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 390 °C, V/III ratio of 136; the nominal thickness of the InSb **NW** being 50 nm.

Here we focus on the **NWs** showing the highest quality, *i.e.* the ones grown along the <1$\bar{1}$0> direction. The success rate of their growth can be evaluated by counting the amount of smooth and continuous **NWs**, in the sun-shape patterns of Figure 5.29a) and b), compared to the "defective" **NWs**, which appear disrupted, with 3D islands or thicker than the nominal thickness, signature of a brighter contrast in the **SEM** image. The success rate reaches 99 % for these 3 µm-long InSb **NWs** grown on GaAs subtrate and drops to 82 % for the ones grown on a GaInP/GaAs substrate.

Then comparison of the dislocations observed at both interfaces in the **STEM** images of Figures 5.29e and f does not give any indication as both systems exhibit a periodic **MD** network of similar spacing. In contrast, the interface abruptness seems to account for the higher success rate when the growth occurs on GaAs $(111)_B$. Indeed, the comparison of Figures 5.29c and d shows that the InSb/GaInP interface does not appear as abrupt as the InSb/GaAs one. The InSb/GaInP interface presents some intermediate contrasted areas. Additionally, it was observed that some parts were already made of InSb (the two distinct atoms) while the neighboring part on the same atomic layer consisted of GaInP. As previously observed in chapter 4 section 4.2.3.1 and 4.2.3.4 or even in the section 5.3.3.2 of this chapter, the morphology of the InSb layer is sensitive upon the surface roughness of the underlying substrate, which is consistent with the result of this paragraph.

Conclusion

Throughout this section, the **SAG** of InSb on GaInP/GaAs heterostructures was explored. While the **SAG** of GaInP **NWs** on GaAs $(111)_B$ turned out to give good results with the growth of smooth and continuous **NWs** in the apertures, the subsequent **SAG** of InSb **NWs** on top of these GaInP **NWs** did not give satisfying results. Indeed, the InSb nucleated as 3D triangular islands on the edges of the GaInP **NWs** without coalescing into a continuous layer.

Conversely, when the InSb **SAG** was performed on patterned 2D GaInP/GaAs heterostructures using the deeper dielectric mask B process (Al_2O_3/SiO_2), a promising outcome is achieved with the growth of 10 µm-long InSb **NWs** even though the selectivity cannot meet the one obtained on a mask consisting of SiO_2 only.

A general lateral overgrowth as well as a crystallographic orientation dependency were consistently observed through the different characterization techniques (**AFM**, **SEM**, **STEM**): [1$\bar{1}$0]-oriented **NWs** are found to be more continuous and uniformly shaped, corroborating the observations of the InSb **NWs** grown on GaAs $(111)_B$ from chapter 4.

The different defects at the InSb/GaInP interface were investigated through **STEM** structural analysis. While a similar **MD** network to the one found for InSb **NWs** on GaAs was observed, additional dislocations and twin domains were also noticed in the faceted, 3D or laterally overgrowing InSb **NWs**, which may account for this change of growth morphology compared to smooth **NWs**. Then, we considered the interfacial roughness as another possible root cause for the occurrence of these defects. From the comparison of the success rate to obtain InSb **NWs** with smooth top facets on GaInP or GaAs surfaces, we noticed a difference in the abruptness of this interface based on the **STEM** analysis. In summary, the GaInP roughness is deemed to be responsible for the lower success rate in achieving smooth InSb **NWs**. Nevertheless, the success rate remains higher than 80 %, meaning a high number of smooth and exploitable **NWs** are present on the grown samples to conduct transport measurements conveniently.

5.5 Conclusion

In this chapter, major accomplishments were achieved. The first section focused on the thin film growth of $Al_{0.8}Ga_{0.2}As$ and $Ga_{0.51}In_{0.49}P$ on GaAs $(111)_B$ to get an insulating barrier before the growth of InSb. We demonstrated that with the latter, a lower **RMS** roughness can be obtained while the former results in the formation of a large density of cracks and trenches in the layer. To improve further the smoothness of the surface, the introduction of Sb as a surfactant during the growth of $Ga_{0.51}In_{0.49}P$ was studied. However, tuning the exact amount of Sb to get a beneficial effect was tricky with our set-up.

In a second time, the subsequent InSb thin film growth on GaInP/GaAs substrates was investigated. A quite smooth morphology is obtained with few unfilled areas under similar growth conditions than the optimized one for InSb on GaAs $(111)_B$ substrates. These experiments stressed the importance of the underlying surface roughness and preparation on the growth mode of the InSb layer. Indeed, starting InSb growth on a GaInP surface deoxidized under an As flux gave better results than with a P flux.

While the **SAG** of in-plane GaInP nanostructures on a patterned GaAs $(111)_B$ substrate provides very good results, the subsequent growth of InSb forms 3D triangular islands that nucleates from the edges of the GaInP **NWs**.

Growing InSb nanostructures from a patterned GaInP/GaAs $(111)_B$ pseudo-substrate revealed to be much more efficient. Using a deeper dielectric mask and adjusting the growth conditions, continuous in-plane InSb **NWs** as long as 10 µm could be achieved with a quite good yield. Similar to InSb on GaAs $(111)_B$ (see chapter 4 section 4.4.2), the cross-sectional **STEM** analysis revealed that, although most of the high lattice mismatch between GaInP and InSb is accommodated via the formation of a **MD** network at the interface, **SF** and twin domains are also observed along the growth direction.

The structural defect density appeared to vary among the investigated **NWs** with various morphologies. The aperture width revealed not to favor any growth mode as the different types of **NWs** were evidenced for all aperture widths. We rather emphasized on the roughness at the InSb/GaInP interface producing a less atomically abrupt transition than the InSb/GaAs one. Overall, most of the InSb **NWs** grown on GaInP/GaAs (111) still exhibited a smooth morphology along the preferred $[1\bar{1}0]$ orientation while keeping a high success rate (82 %) for a length of 3 µm.

In summary, the successful growth of smooth 10 µm-long in-plane InSb **NWs** on GaInP/GaAs $(111)_B$ substrate was demonstrated, opening the door to transport measurements with the possibility to tune the charge density in the **NW** by biasing the substrate.

Chapter 6

Transport measurements in InSb/GaInP/GaAs $(111)_B$ heterostructures

6.1 Introduction

In the previous chapter, we were able to grow InSb thin films and nanostructures on GaInP/GaAs $(111)_B$ heterostructures with good structural quality. Because the band gap of GaInP/GaAs is a type I heterostructure with the band gap of GaInP larger than the one of GaAs, the GaInP layer could act as a potential barrier. This brings us to the final objectives of this work: Is the electronic quality of the InSb layer good enough to achieve an efficient conduction and can we modulate this conduction as the InSb layer is separated from the GaAs gate by the GaInP barrier ?

To answer these questions, the final chapter will be divided into three main sections. First, Hall measurements will be performed on the 2D InSb thin films which were grown on the GaInP/GaAs $(111)_B$ heterostructures. On the same sample, **TLM** devices will be fabricated to test the charge carrier modulation inside the InSb 2D thin films. A back-gate voltage will be applied on the n-doped GaAs substrate to evaluate its effect on the transport properties of the device.

Then, the second section will focus on the study of transport properties of in-plane InSb nanostructures by **SAG** on the GaInP/GaAs $(111)_B$ heterostructures. To perform such experiments, a **4P-STM** will be used, as this instrument allows a direct access to single **NW**, without any processing of the nanostructures. Furthermore, the arbitrary positioning of the 4 probes along a single **NW** offers the advantage to probe multiple locations while it avoids expensive processes for the fabrication of electrodes. At first, the electrical conduction of InSb **NWs** with oxidized sidewalls will be investigated. Then, a voltage will be applied to the back of the n-doped GaAs substrate to evaluate the possible modulation of the charge carriers inside the InSb **NWs**.

As the **4P-STM** experiments are performed in **UHV**, the surface of the InSb **NWs** can be controlled. Because its impact on the scattering effects becomes important with **NWs**, the last section of this chapter will deal with **STM** and **STS** studies of 2D Insb thin films grown on the GaInP/GaAs heterostructures to determine the surface reconstruction and defects after the

desorption of their native oxide. Such a study is a prerequisite before investigating the transport properties of InSb **NWs** with clean and well-ordered sidewalls by **4P-STM**.

6.2 Transport properties of 2D InSb thin films on GaInP/GaAs heterostructures

6.2.1 Hall measurements

Before considering the possible modulation of the charge carriers inside the InSb layer, it is important to first assess the electrical conduction of this layer. Consequently, Hall experiments were performed on a piece of sample **IGG4** that was patterned with Van der Pauw microstructures as explained in chapter 2 section 2.6.2, which consist of a 470 µm square central region, with four 900 µm × 900 µm pads at each corner, connected via 50 µm-wide, 25 µm-long arms (see in appendix A Figure A.6a and c in the red and yellow boxes). After photoresist patterns definition and a short in-situ argon etching inside the metal evaporation chamber to remove the InSb native oxide, Ti/Au contacts were deposited. InSb mesas down to the GaInP surface were then realized by wet etching with the same solution described in chapter 2 section 2.6.2. We recall here that sample **IGG7** showed the best film morphology in the previous chapter and that **IGG4** differs from **IGG7** by a larger thickness only. Sample **IGG4** consists of a 100 nm-thick InSb layer on a GaInP/GaAs:n+ $(111)_B$ heterostructure. The growth conditions are found in chapter 5 section 5.3.1. The GaInP/GaAs heterostructure used for the growth of sample **IGG4** came from sample **GG1**.

The resulting InSb film morphology (**IGG4**) was shown in Figure 5.14b and exhibits a smooth surface with relaxed islands that coalesced rapidly to cover more than 97 % of the GaInP surface. Table 6.1 summarizes the main parameters determined from the Hall measurements at 300 K.

Sample	T (K)	R_{sh} ($\Omega/\square$)	n (10^{12} cm^{-2})	μ (cm^2.V^{-1}.s^{-1})
IGG4	300	930	-0.6	11000

Table 6.1: Hall effect measurements at 300 K of sample **IGG4**, 100 nm InSb-thick on GaInP/GaAs $(111)_B$ heterostructure. Growth parameter for InSb: $\mathbf{T_G}$ = 385 °C, $\mathbf{V_G}$ = 0.05 **ML**/s, V/III = 136 and for GaInP (**GG1** sample): $\mathbf{T_G}$ = 520 °C, $\mathbf{V_G}$ = 0.2 **ML**/s, V/III = 50.

A sheet resistance equal to 930 $\Omega/\square$ was found. A low carrier density (n) was measured with a value of -0.6×10^{12} cm^{-2} which suggests a very low background doping. Based on these values, the electron mobility reaches 11000 cm^2.V^{-1}.s^{-1}. This value can appear as rather low compared with the literature, which reports electron mobility of 40000 cm^2.V^{-1}.s^{-1} at 300 K for InSb layers. But these results were obtained by using either an $In_{1-x}Al_xSb$ buffer layer or a much thicker InSb layer (>1 µm) on GaAs.[102,248] Taking into account the incomplete coalescence of the layer, the mobility value seems reasonnable. It is even higher than the one measured by Kanisawa *et al.* with a value of ~4500 cm^2.V^{-1}.s^{-1} and a carrier density of ~0.5×10^{12} cm^{-2} at 300 K for a 100 nm-thick InSb layer grown on a GaAs $(111)_A$ substrate by **MBE**.[101]

In the context of this work, we find interesting to compare these results to the one found for the InSb/CdTe thin films corresponding to sample **IC7** and measured at 300 K in Chapter 3 section 3.2.3.4. As a reminder, the reported values from Hall measurements for this sample were R_{sh} = 642 $\Omega/\square$, n = -2.73 ×10^{12} cm^{-2} and μ = 3560 cm^2.V^{-1}.s^{-1}.

Although the InSb was grown on highly mismatched GaInP, sample **IGG4** shows a three-fold higher mobility which is surprising at first sight. This result can be attributed to several factors. The growth of a thicker InSb layer, 100 nm instead of 30 nm, helps to reduce the

deleterious influence of interface and surface scattering. Secondly, the effect of high lattice mismatch between InSb and GaInP is attenuated thanks to the formation of a regular array of misfit dislocations at the interface, which limits the threading dislocation density as well as the roughness of the surface.

Moreover, the higher carrier density for InSb on CdTe sample points to the existence of residual donors, which was strongly supported by the intermixing observed through the **XPS** analysis in chapter 3 section 3.2.1.2 for sample **IC2** (in this case, the carrier density n is even higher, reaching 7.78×10^{12} cm^{-2}). These residual donors act as ionized scattering centers, which impacts the mobility significantly.

Low Temperature measurements

Unfortunately, the low residual doping of the InSb layer at 77 K led to non-ohmic contacts, which prevented us to measure the electron mobility at low temperature on these Van der Pauw devices.

6.2.2 TLM measurements

To validate the previous transport measurements and determine if the charge carriers density inside the InSb layer could be modulated, some **TLM** structures were also patterned on sample **IGG4**. As described in chapter 2 section 2.6.1, these experiments are key to measure the contact resistance between the InSb layer and electrodes as well as the resistance of the layer independently.

The **TLM** structures are outlined in Figure A.6b in appendix A and consist of 50 µm-wide and 94 µm-long rectangular pads separated by various distances d: 5, 10, 15, 20, 50 µm. The structures are patterned on the sample within the same process than for the previous Van der Pauw device fabrication. The isolation of the InSb mesas resulted in a resistance between two neighboring electrodes higher than 10 MΩ (Figure 6.1b). The same Ti/Au metal stack was deposited on the back-side of the GaAs:n+ substrate after protecting the top surface with photoresist.

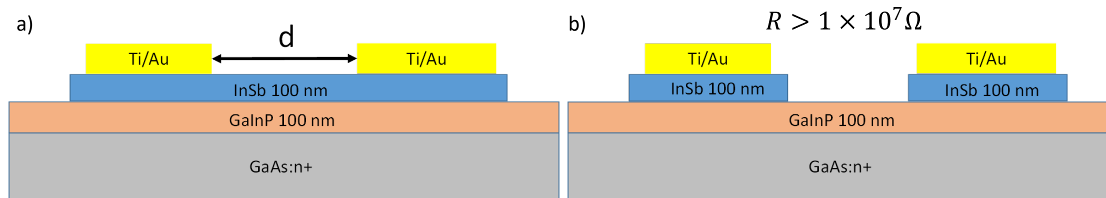


Figure 6.1: Schematic of the **TLM** device on sample **IGG4** showing a) a measurement at distance d and b) the mesas etched down to the GaInP surface to isolate each **TLM** array.

To conduct the experiments once the device was ready, a four-probe bench from the **HOPC** platform at IEMN was used. The data collection was managed through Keithleys sourcemeters and the input parameters were set on the IC-CAP software interface once all probes were manually contacted. All **TLM** measurements were done at 300 K.

6.2.2.1 Evaluation of the operating range of the heterostructure

Before considering the data collection for the different distances, we evaluated the operating range of the heterostructure. In other words, as we have a semiconducting GaInP barrier, it is

important to define the gate voltage range for which the system is not leaking. To do so, a bias voltage was applied between a top metal electrode and the back-contact deposited on the GaAs $(111)_B$:n+ substrate, as illustrated in Figure 6.2a. The current was measured as a function of the bias voltage applied on the back contact.

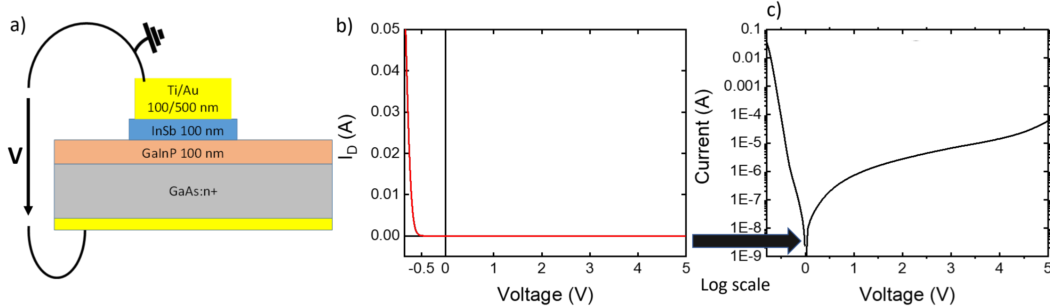


Figure 6.2: a) Schematic of the **TLM** device for the leakage testing configuration. b) Current-voltage characteristic of vertical devices fabricated with sample **IGG4** plotted with a vertical linear scale in b) or logarithmic vertical scale in c).

As shown in Figure 6.2b, the device operates within a low leakage regime in the -0.5 – 5 V range. When switching to the logarithmic scale of Figure 6.2c, the leakage is smaller than 0.1 mA from -0.5 V and up to 5 V at positive voltages.

6.2.2.2 Determining the contact resistance and sheet resistance of the layer (R_c, R_{sh})

To further characterize the operating parameters of the InSb/GaInP/GaAs heterostructure, the determination of both the contact and sheet resistance of the layer is important. As defined in the chapter 2 section 2.6.1, we first acquired, with the **TLM** device, the I-V characteristics between top contacts curves from -0.5 V to 0.5 V for all inter-electrode distances d with a floating substrate as shown in Figure 6.3.

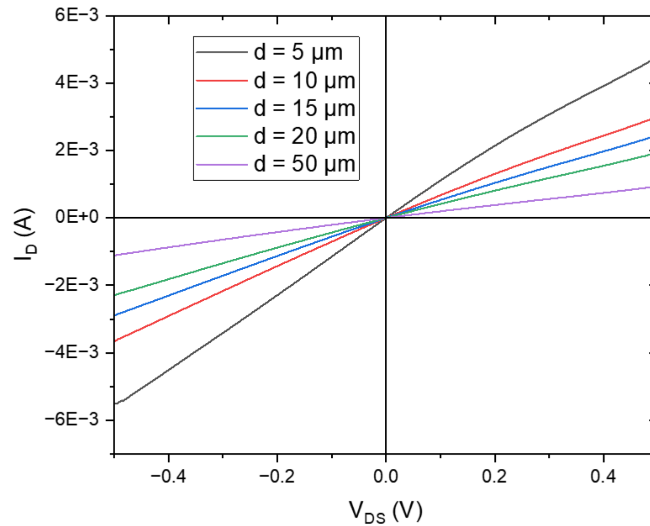


Figure 6.3: I_D vs V_{DS} curves for all distances d with no applied gate voltage. The **TLM** resistance (R_{TLM}) can be extracted from the slope of these linear curves.

From the linear dependency, the slope allows to extract the **TLM** resistance (R_{TLM}). Then, using the equation 2.14 (recalled in Figure 6.4a), the contact resistance (R_c) is given by the y-intercept of the curve and the sheet resistance (R_{sh}) can be deduced from the interpolated slope, knowing the width W of the channel. From Figure 6.4a, we extract a contact resistance R_c of 17.7 ± 1 Ω and a layer sheet resistance R_{sh} of 874 ± 8 Ω/□ (W = 94 µm). This latter value agrees reasonably well with the sheet resistance determined from Hall measurements (930 Ω/□).

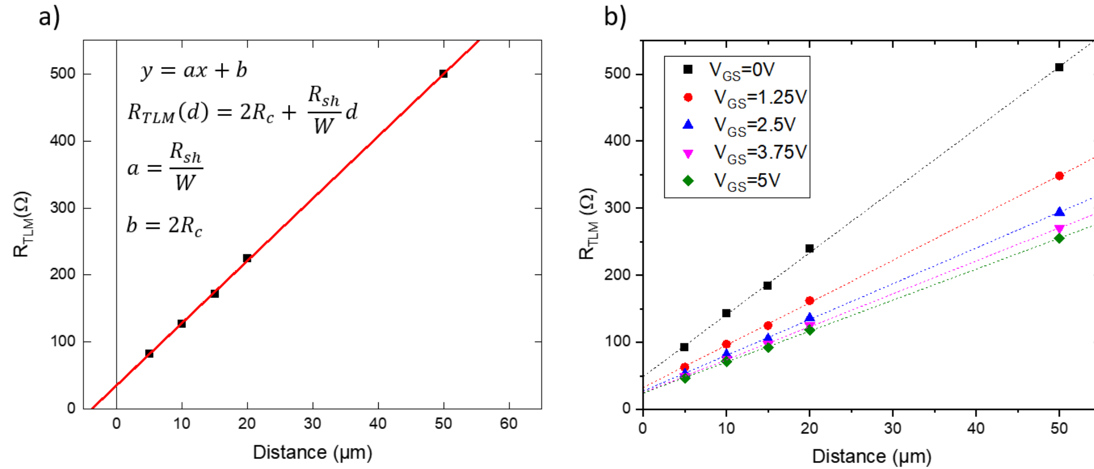


Figure 6.4: **TLM** resistance (R_{TLM}) as a function of the distance d a) with a floating back-gate and b) for various values of back gate voltage $\mathbf{V_{GS}}$. These curves allow the extraction of both the contact and sheet resistance (R_c and R_{sh}).

As highlighted in Figure 6.4b, where R_{TLM} is plotted against d for various substrate bias, the slope of the curve changes. The variation of R_{sh} is listed in Table 6.2 below.

Substrate bias voltage (V)	0	1.25	2.5	3.75	5
R_{sh} (Ω/□)	870	595	502	462	435

Table 6.2: Sheet resistance extracted from R_{TLM} versus **TLM** distance for various substrate bias voltages.

A variation of the substrate bias voltage from 0 to 5 V causes a decrease of the sheet resistance by 50 % which represents a proof of the successful modulation of the charge carrier density inside the InSb layer. Regarding R_c, the y-intercepts of the curves are different depending on the substrate bias voltage value as the area under the contacts is also enriched.

6.2.2.3 Extraction of the electron mobility

Using the **TLM** devices, the electron mobility of the heterostructure can also be extracted thanks to the operating gate voltage. To do so, we focus on the widest device at a distance d = 50 µm. As depicted in Figure 6.5a, the drain current (I_D) was measured as a function of the back-gate to source voltage ($\mathbf{V_{GS}}$) for various drain to source voltages (V_{DS}), such a graph being called a "Transfer curve".

For all curves collected at different V_{DS} values in Figure 6.5b, the current I_D increases accordingly with $\mathbf{V_{GS}}$, which is a second proof that more electrons are present in the channel. The third confirmation is the upward scaling of I_D with increasing V_{DS} that witnesses the modulation of the channel resistance through back-gate-controlled charge density. At 300 K, the full depletion is not obtained (incomplete pinching) due to the large thermal activation

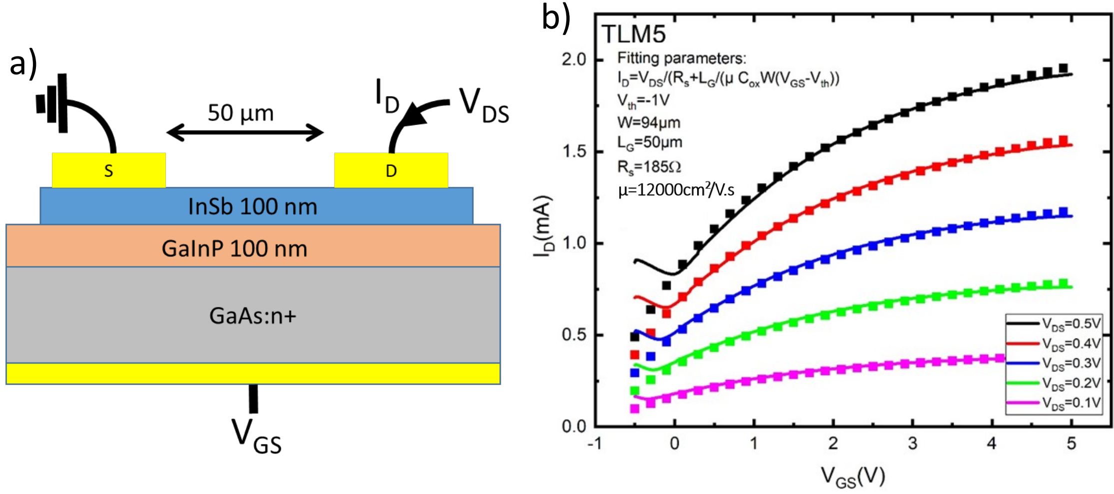


Figure 6.5: a) Schematic of the back-gated experiments on the widest **TLM** b) Drain current curve as a function of the gate to source voltage applied on the GaAs substrate of sample **IGG4** for various drain-source voltages.

of carriers, but a significant modulation of the charge carrier is observed. Furthermore, the device shows an ambipolar behavior, as the current increases at negative back-gate voltages. This property is representative of a hole conduction due to the narrow band gap of InSb. This phenomenon is coming from the large density of thermally activated holes at **RT**, but also the from the ones generated by electric field-assisted band to band electron tunneling from the channel to the drain region under the effect of V_{DS} voltage.[139,249,250] The negative $\mathbf{V_{GS}}$ pulls the energy bands of the channel upwards, creating a narrow tunneling barrier at the channel-drain junction that enables the ambipolarity of the device.

From these transfer curves, the device can be modeled with a n-type **MOSFET**. To take into account the series resistance (R_S) that arises from the contacts (equivalent to $2R_c$), the drain current can be expressed by

$$I_D = V_{DS}\left(R_S + \frac{L_G}{\mu_{FE} C_{ox} W (V_{GS} - V_{th})}\right)^{-1} \tag{6.1}$$

where L_G is the channel length (50 µm), W the channel width (94 µm), C_{ox} the capacitance of the GaInP barrier, V_{th} the threshold voltage and μ_{FE} the field effect mobility.[63]

The capacitance C_{ox} for GaInP is expressed by $C_{ox} = \varepsilon_0\varepsilon_r/t_{ox}$, where ε_0 is the vacuum permittivity ($\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm), ε_r the relative dielectric constant of the GaInP layer ($\varepsilon_r = 9.61 - 0.5x = 9.36$ F/cm for $x = 0.5$ the Ga content[251]) and t_{ox} the thickness of the potential barrier (100 nm). Converting the whole in F/cm^2 to meet the mobility standard unit, $C_{ox} = 8.274 \times 10^{-8}$ F/cm^2.

Using Equation 6.1, each I_D curve is fitted to extract the mobility. Because the full depletion is not obtained at 300 K, the **Threshold Voltage** (V_{th}) and the series resistance were fitted in the model with constant values of -1 V and 185 Ω respectively. This latter value implies a contacts resistance which is higher than the one deduced from **TLM** measurements with floating back-gate. This could be due to the accumulation of charges near the bottom interface of the InSb layer for positive back-gate voltages. As highlighted in the Figure 6.5b, for all curves we obtain an electron mobility of ~12000 cm^2.V^{-1}.s^{-1} which is consistent with the Hall measurements at 300 K reported earlier in this chapter (μ = 11000 cm^2.V^{-1}.s^{-1}, n_s = -0.6×10^{12} cm^{-2}). This result

once again represents the highest electron mobility achieved for an InSb thin film grown on mismatched substrates without any accommodating buffer layers, outperforming the previous data from literature[101] of ~4500 $cm^2.V^{-1}.s^{-1}$.

Conclusion

Throughout this section, the transport properties of the InSb thin films on GaInP/GaAs $(111)_B$ substrates were investigated by performing Hall and gate-dependent **TLM** measurements. For both techniques, an electron mobility higher than 10000 $cm^2.V^{-1}.s^{-1}$ was measured: 11000 $cm^2.V^{-1}.s^{-1}$ for Hall and 12000 $cm^2.V^{-1}.s^{-1}$ for **TLM** measurements respectively, yielding a record electron mobility for InSb 2D thin films grown directly on a highly mismatched substrate without accommodating buffer layers. The low charge density n of -0.6×10^{12} cm^{-2} indicates low background doping. The presence of a **MD** network at the InSb/GaInP interface does not seem to result neither in a large density of interface traps nor in a large density of donor defects that could seriously degrade the transport properties in the InSb layer at 300 K.

In the second part, the back-gated **TLM** measurements indicated that the InSb/GaInP/GaAs stack enables a modulation of charge carrier density inside the InSb layer with the doped GaAs substrate bias. The devices exhibited a quite good control with no leak to the gate over the -0.5 V < $\mathbf{V_{GS}}$ < 5 V voltage range.

6.3 4P-STM transport measurements of in-plane InSb nanostructures on GaInP/GaAs substrates

After showing that the use of an InSb/GaInP/GaAs:n+ stack enables a back-gate control of the conduction in the InSb channel for thin films, we investigate in this part the possibility to get a similar command for in-plane nanostructures. In this regard, **4P-STM** measurements were performed on two samples: 1) **SIGG6** which corresponds to the **SAG** of 100 nm-thick InSb on a GaInP/GaAs substrate, 2) **SIGG3** which corresponds to the **SAG** of 50 nm-thick InSb on a GaInP/GaAs substrate (see chapter 5 section 5.4.3 for growth conditions).

As explained in chapter 2, the **4P-STM** measurements consists in contacting a nanostructure with 4 **STM** tips. Because the positioning of the probes on the nanostructures is risky for the probes, despite a supervision with the **SEM**, we usually etch the dielectric mask to make sure that the approach in the tunneling mode can also be made safely on the surface of the substrate. However, we realized that the removal of the SiO_2 dielectric layer by HF dip can result in InSb etching catalyzed when metallic markers are present on the surface.

Therefore, all the **4P-STM** measurements were performed with the dielectric mask maintained intact between the nanostructures. Nevertheless, the thickness of InSb nanostructures is sufficient to overpass the mask surface, which makes the tip landing on the nanostructures safe.

As no capping layer was deposited after the growth of the InSb nanostructures and the **4P-STM** is not equipped with an ion gun for $\mathbf{H_{AT}}$ exposure, the nanostructures were left covered with their native oxide. Only an annealing step of 120 °C was performed for a few hours in order to desorb the water molecules following the introduction of the samples in **UHV**. The electric contact was then made by piercing this thin oxide layer with the **STM** tungsten tips.

Tip positioning error

While this **4P-STM** technique enables a direct electrical contact with a nanostructure using freely movable tungsten tips, there exists an uncertainty with regards to the exact position of the contact. Indeed, the tip has a finite radius which can shadow the contact point in the **SEM** image.

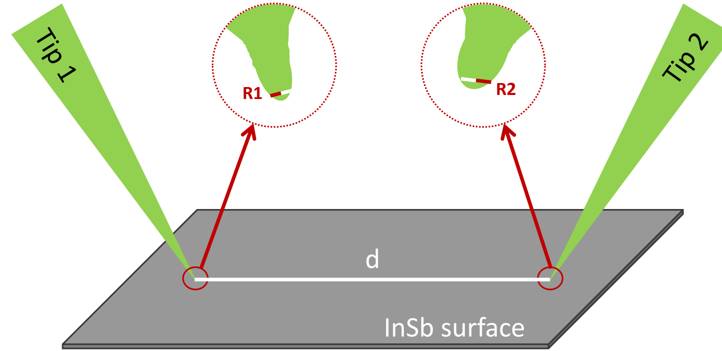


Figure 6.6: Schematic of the distance d between two tips. If we consider d at the center of each tip, the actual uncertainty about the position is taken into account by adding their radius into the measure (R1 and R2).

In general, we consider that the tip center is in contact with the surface, however as seen in Figure 6.6, we need to account for the total tip radius. If we consider d the inner distance between the center of the two tips, the real distance may be significantly larger or shorter depending on the tips radius. The real distance d_{real} that takes into account this deviation in the form of error bars is expressed as $d_{real} = d \pm (R_1 + R_2)$. In this work, whenever we present a parameter as a function of the probe distance, the tip positioning error will be indicated.

6.3.1 Charge carrier modulation in InSb nanoplatelets

In an attempt to quickly evaluate the electronic quality of the **SAG** of InSb nanostructures, we first considered the nanoplatelet depicted in appendix A Figure A.5b (through the red rectangles) and Figure 6.7a. They belong to sample **SIGG6** where the InSb thickness deposited in the apertures is 100 nm. They are 2 µm-wide by 3 µm-long and have a geometry which should yield transport properties closer to a **2DEG** than a one-dimensional system.

The tunneling approach of the tips relies on the standard approach of a **STM** tip thanks to the coarse motor and the scanner of each tip. It is performed automatically through the built-in function implemented in the Nanonis software. A setpoint of 100 pA was set and a small voltage (typically -100 mV) was applied to the tip, so that the InSb surface is detected in the tunneling regime without crashing the **STM** tip. Once the tunneling approach was done, the tip was gently pushed down until the current of the preamplifiers saturates (at 333 nA in high gain conditions) to ensure a steady electrical contact. Such a method to create an electrical contact was repeated for the other **STM** tips. Experiments with two tips and four tips in contact with the surface of a nanoplatelet were performed. For the latter one, as seen in the schematic structure of Figure 6.9a, a linear arrangement of the **STM** tips was achieved along the longest axis of the nanoplatelet. The outer tips, which were placed close to the border of the nanoplatelet, were used to inject and collect the current, while the inner ones measured the potential drop. To position the inner tips, one was kept fixed at a small distance from the source tip while the second inner tip is displaced at various distances for each measurement.

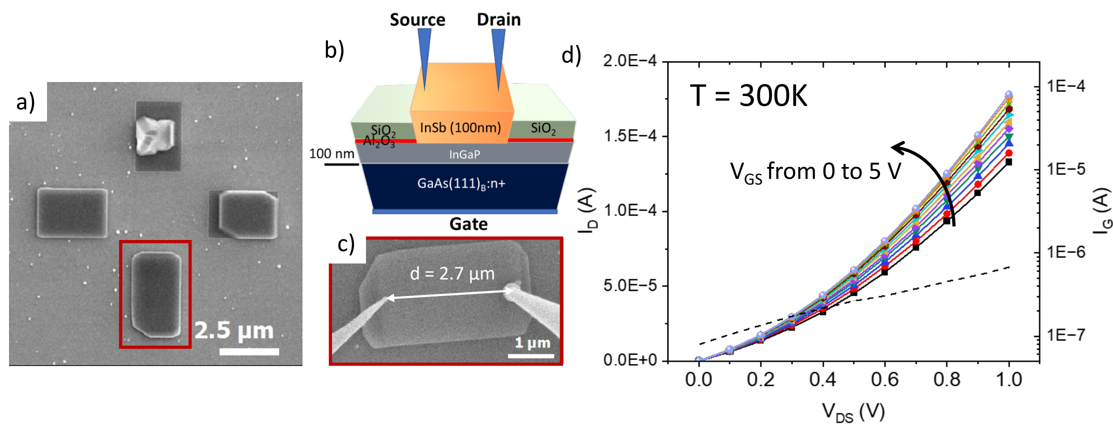


Figure 6.7: a) **SEM** image of the nanoplatelets of sample **SIGG6** b) Schematic of the **2PP** measurement configuration. c) **2PP** measurements at a distance $d = 2.7$ µm. d) Drain current curve at 300 K as a function of the drain-source voltage for various gate voltages. On the right y-axis, the gate current is shown for $\mathbf{V_{GS}} = 5$ V.

6.3.1.1 2PP measurements

The first data collection was done through **2PP** measurements. For the Output characteristics script, that corresponds to $I_D = f(V_{DS})$, the drain-to-source voltage was swept from -1 V to 1 V twice (forward and backward sweep) and the resulting drain current I_D was measured. For each V_{DS} sweep, the gate voltage was changed by gradual steps from 0 to 5 V. Figures 6.7b and c illustrates schematically and through in-situ **SEM** imaging, the **2PP** measurement configuration. The tip distance is set to 2.70 ± 0.25 µm.

From the Output characteristic curve in Figure 6.7d, the modulation of the charge density inside the InSb nanoplatelet is visible as the current increases accordingly with higher $\mathbf{V_{GS}}$ values for a fixed V_{DS}. This observed modulation is valid as the gate current for $\mathbf{V_{GS}} = 5$ V remains much lower (in the $8{\times}10^{-7}$ A) than the measured drain current, meaning this is not due to leakage from the gate. However, the current-voltage characteristic is not linear, which originates from the Schottky contacts formed between the tungsten tips and the InSb surface. If we compare the resistance of the InSb thin film (Figure 6.4b) with the resistance measured for the nanoplatelet at the same V_{DS} and $\mathbf{V_{GS}}$, we find an increase of the total resistance by a factor of 10. Assuming a resistivity of InSb similar between both systems would give a contact resistance higher on the nanoplatelet, which is consistent with the presence of the native oxide left on the nanostructure. Moreover, the local point-contact in this **4P-STM** method yields obviously a higher resistance than a metallic pad used for the **TLM** measurements.

Further experiments were conducted on the same InSb nanoplatelet at **LT** (113 K). As explained in chapter 2, because the microscope does not reside in a cryostat and can only cool the sample, while the tips are held at **RT**, an important thermalization time is needed before getting a convenient contact. Even then, the risk of tip damage exists due to stronger thermal drift, higher contact resistances and enhanced noise of the measurements. To get a successful measurement, we usually started cooling down the sample the evening before the measurements while keeping the tips 50 µm away from the surface. After this overnight cooling, the tips were thermalized, allowing a steady tunneling approach of the **STM** tips and a longer time without disruption of the electrical contact.

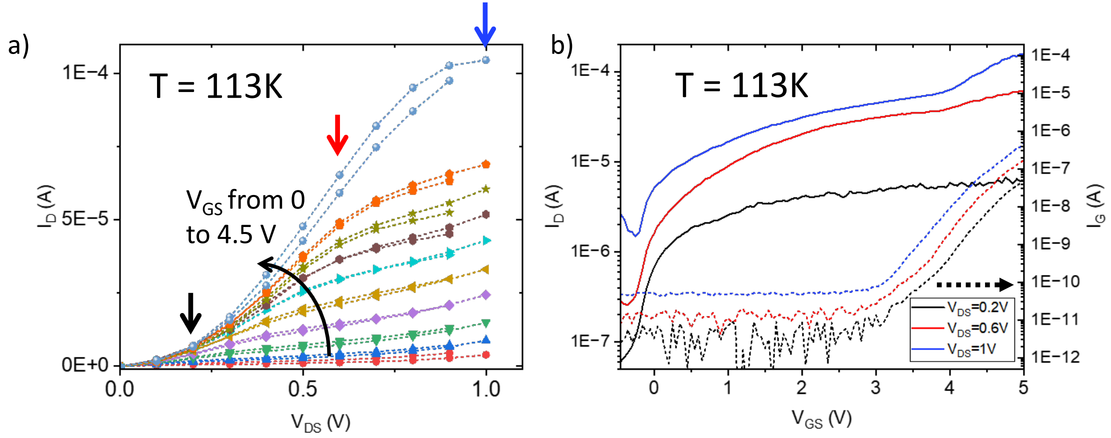


Figure 6.8: a) Drain current curve at 113 K as a function of the drain-source voltage for various gate voltages. b) Transfer curve (I_D versus $\mathbf{V_{GS}}$) for various drain-source voltages. Each curve corresponds to the vertical line-cut indicated by the colored arrows in a).

Figures 6.8a and b present the output characteristics and transfer curves respectively for the InSb nanoplatelet at 113 K. The gate modulation of the conductance of the InSb channel is visible through an increase in the current with both V_{DS} and $\mathbf{V_{GS}}$. Compared with the **RT** experiment at 300 K, the temperature drop causes a decrease of the current from 1.75×10^{-4} A to 1.05×10^{-4} A at maximum $\mathbf{V_G}$ = 4.5 V and V_{DS} = 1 V, which agrees with a reduced concentration of the free charge carriers and an increase of the contact resistances.

The transfer curves ($I_D = f(\mathbf{V_{GS}})$) from Figure 6.8b provides further information on the transport inside the heterostructure. First, it showcases the efficient gate switching of the InSb channel at **LT**. For V_{DS} = 0.6 V, an increase in the current by a factor 120 is seen for $\mathbf{V_{GS}}$ from -0.5 to 3 V. Secondly, the ambipolar behavior of the InSb heterostructure is again evidenced through the sudden increase of the current at low negative gate voltages. As the contribution of thermally activated holes can be neglected at 113 K, this means that this phenomenon is mainly due to band to band tunneling effect. Indeed, the impact of the drain to source voltage on the negative part of the characteristics evidences the role of the longitudinal electric field in the ambipolar current.

Yet, the shift in the corresponding $\mathbf{V_{GS}}$ value of this minimal current can be attributed to **Drain Induced Barrier Lowering (DIBL)**. This phenomenon occurs for high enough V_{DS} values. In such conditions, the generated electric field from the drain will further extend into the channel, hence reducing the potential barrier at the source that makes it easier for the electrons to flow (hence a lower threshold voltage to turn off the **MOSFET**).[252,253]

Although being still two orders of magnitude under the drain current, the gate current I_G (right axis and dotted color lines) shows a sharp increase by almost a factor 10000 when $\mathbf{V_{GS}}$ is increased from 3 to 5 V. This is a clear evidence of gate leakage due to tunneling or field-assisted injection through the GaInP barrier. Eventually, for larger V_{DS} values, for instance V_{DS} = 1 V, a clear increase in the drain current starting at $\mathbf{V_{GS}}$ = 4 V is seen, which comes from the impact ionization phenomena. Under larger drain-source polarization, the generated electric field increases in the channel near the drain, which accelerates the electrons that collide with the atoms in the lattice. These latters are hence ionized, creating additional electron-hole pairs. The gate current thus increases due to the larger thermal energy of electrons flowing in InSb resulting from impact ionization. These electrons hence flow more easily over the GaInP barrier to the

substrate.[254] In this regard, the gate current was monitored at all time during the acquisition of the electrical measurements to remain under controlled-leakage conditions.

6.3.1.2 4PP measurements

To get insight into the resistivity of the InSb nanoplatelet and avoid the contribution of the contact resistance, **4PP** measurements were run at **RT** (300 K). The same experiments, adapted to the four-probe configuration, were performed. For these experiments, the current is swept forward and backward from -50 to 50 µA. The voltage drop ΔV corresponds to the difference of potential measured between the inner tips labeled V_2 and V_1. The inner probe distance was set at 1.2 ± 0.2 µm and the conductance was measured for various applied gate voltages, from -0.5 to 4.5 V by steps of 0.5 V.

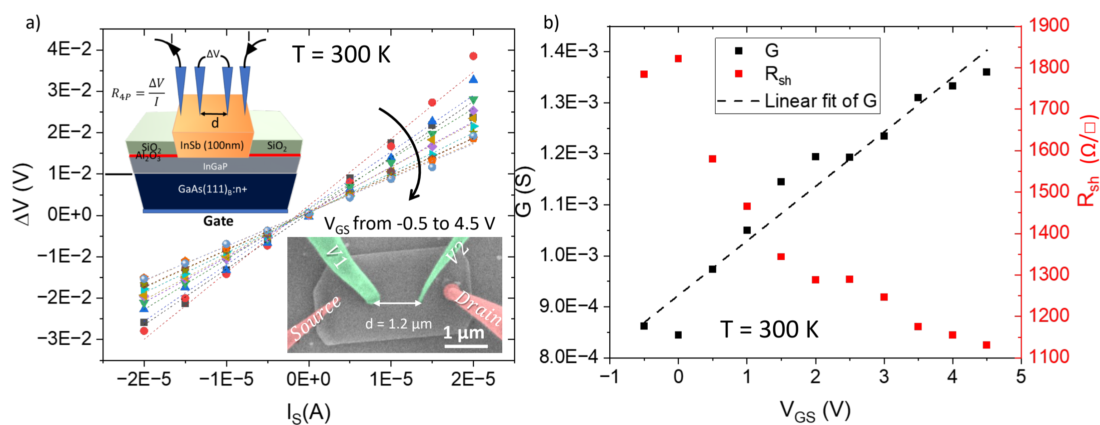


Figure 6.9: a) $I-V$ curves from the **4PP** measurements on the nanoplatelets for various gate voltage values at 300 K. Insets: schematic of the **4PP** measurement configuration on the InSb/GaInP/GaAs heterostructure and false-colored **SEM** image of the measurement at the inner tip distance d = 1.2 µm. b) Conductance and sheet resistance variations as a function of the back-gate voltage at 300 K extracted from the **4PP** measurements.

As shown in Figure 6.9a the $I-V$ curves are this time linear because of the absence of contact resistance in the measurement as long as the tips are in contact with the InSb surface. From the slope of the curves, the $\mathbf{R_{4P}}$ can be extracted (simply through $\mathbf{R_{4P}} = \Delta V/I$). Compared to the **2PP** measurements, the resistance is roughly ten times smaller. This result supports the conclusion of a significant contribution of the contact resistance when the electrodes consist of **STM** tips. By taking the inverse of $\mathbf{R_{4P}}$, the intrinsic conductance G is calculated. As highlighted in Figure 6.9b, the quasi-linear increase of G with $\mathbf{V_{GS}}$ shows the efficient modulation of the charge density inside the InSb nanoplatelet.

To compare the resistivity of the InSb nanoplatelet with the one of the InSb thin film, we assume that the sheet resistance of the nanoplatelet is given by $R_{sh} = \mathbf{R_{4P}} \times W/d$. For comparable values of $\mathbf{V_{GS}}$, 0 V and 2.5 V, the sheet resistance of the InSb thin film were 870 Ω/□ and 502 Ω/□ versus 1822 Ω/□ and 1288 Ω/□ for the nanoplatelet. Albeit slightly higher, the sheet resistance shows the same order of magnitude. We believe that the discrepancies arise from the correction factor which must be applied to the **4PP** measurements.[169] While the **TLM** structures have metallic pads that cover the whole width of the structure, the **4P-STM** tips are only injecting current and probing voltage at a single point of the 2D nanoplatelets. The field distribution

hence varies spatially, accounting for a deviation of the sheet resistance.

To conclude, the sheet resistance obtained from the **4P-STM** performed on the nanoplatelet agrees with the values found for the InSb thin film from **TLM** and Hall measurements, suggesting similar transport properties between both systems. However, thanks to their limited dimensions with **SAG**, they are free from nanoholes in the layer.

6.3.2 Transport properties of bottom-gated InSb NWs

The **NWs** grown by **SAG** were finally investigated. We restricted the study to two main crystallographic orientations, namely $<1\bar{1}0>$ and $<11\bar{2}>$. In the context of **4P-STM**, the measurements were performed on 10 µm-long **NWs** designed within arrays of different equivalent orientations as presented in Figure 6.10a and appendix A, Figure A.3c.

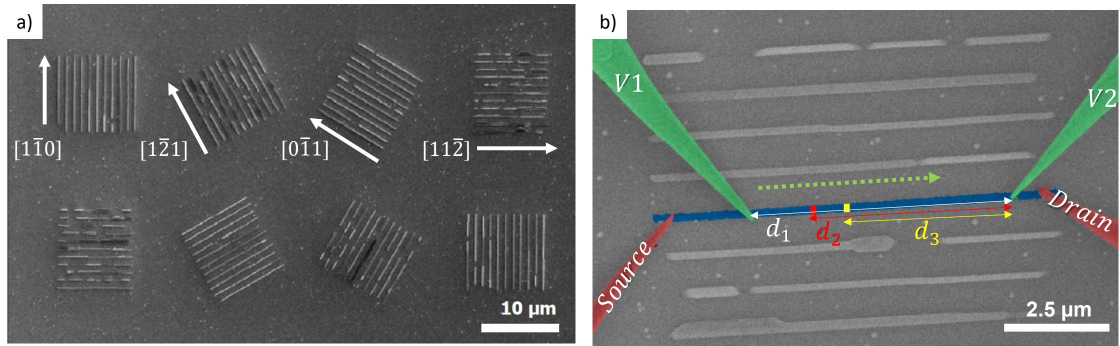


Figure 6.10: a) **SEM** image of **NW** arrays with different orientations studied in the context of **4PP** measurements. b) False-colored **SEM** image illustrating how a **4PP** measurement takes place on a **NW**. After all tips are contacted, only V_1 is moved (green-dashed arrow) to collect the data at various probe distances d_1, d_2, d_3

Figure 6.10b illustrates a **NW** in contact with 4 **STM** tips. In this configuration, only one of the four probes is moved along the **NW** to measure the electrical characteristics as a function of the separation d between the inner tips. Such a method reduces the probability to crash the **STM** tips and degrade the surface of the **NW** because the data acquisition is performed step-wise from the largest tip separation to the shortest one. From the linear $I-V$ curves obtained from the **4PP** measurements, the **NW** resistance was extracted for each distance at different gate voltages.

In the context of **LT** (113 K) measurements, in spite of the precautions taken for the sample cooling, the contact for all four tips needs to be regularly checked as a temperature difference can still exist between the tips and the sample leading to the drift of the tips and their disengagement from the surface. As such, the probability of degrading the **NW** surface increases.

6.3.2.1 Effect of the aperture width on the NW resistivity

The critical effect of the aperture width on the transport properties was first investigated with sample **SIGG6**. For this purpose, **4PP** measurements were performed on two [0$\bar{1}$1]-oriented **NWs** with a significant difference in their respective theoretical aperture width: 40 nm and 100 nm. The experimental width determined from the **SEM** images revealed a width much larger for both **NWs**: 165 nm and 245 nm for the 40 nm and 100 nm nominal aperture width respectively, indicating an overgrowth of the **NWs**, once the thickness of the deposited InSb is higher than the height of the dielectric bilayer.

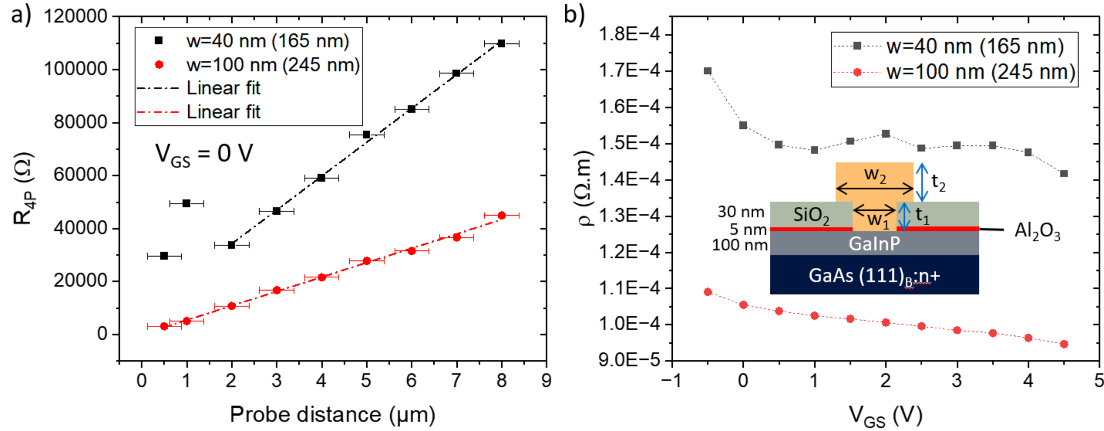


Figure 6.11: a) $\mathbf{R_{4P}}$ vs probe distance for the two $[0\bar{1}1]$ **NWs** of different width at 300 K and $\mathbf{V_{GS}}$ = 0 V. b) Resistivity curve as a function of $\mathbf{V_{GS}}$ showing the gate modulation efficiency. Inset: Schematic of the heterostructure showing how the section of the **NW** is used for calculation.

As shown in Figure 6.11a, the $\mathbf{R_{4P}}$ is consistently higher in the case of the narrower **NW** for all probe distances. For the wider **NW**, all the values of $\mathbf{R_{4P}}$ fall on the same line, which agrees with a resistance proportional to the **NW** length. For the narrower **NW**, the same behavior is observed, although the values measured for the smaller probe distances deviate from the linear fit obtained for the rest of the values. This deviation can be attributed to a damage of the **NW** surface when the two potential probes become close. From the linear fit of the $\mathbf{R_{4P}}$, we can evaluate the **NW** resistivity based on the measured dimensions of the nanostructures using the common equation

$$\rho = \frac{\mathbf{R_{4P}} \times S}{d} \tag{6.2}$$

where S is the cross section area of the **NW**.

For the calculation, $\mathbf{R_{4P}}/d$ is given by the slope of the fitting line and the section of the **NW** is split into two terms: $S = W_1 \times t_1 + W_2 \times t_2$ (inset schematic of Figure 6.11b). The first term corresponds to the InSb thickness inside the aperture where we chose to use the theoretical aperture width (40 or 100 nm). The second term represents the InSb part of the **NW** that grew outside the mask and expanded laterally. As a result, the narrower **NW** section is: $S = 40 \times 10^{-9} \times 35 \times 10^{-9} + 165 \times 10^{-9} \times 65 \times 10^{-9} = 1.21 \times 10^{-14}$ m^2. For the wider **NW** (100 nm), $S = 1.94 \times 10^{-14}$ m^2.

The comparison of the resistivity yields a larger resistivity by a factor of 1.5 for the narrower **NW**. By repeating the **4PP** measurements at different $\mathbf{V_{GS}}$ (Figure 6.11b), a similar trend is observed. We attribute it to the increased surface-to-volume ratio. Eventually, the resistivity decreases along with $\mathbf{V_{GS}}$. Slightly similar back-gate control efficiencies are obtained for both **NW** dimensions (about -16 % of resistivity between -0.5 V and 4.5 V).

6.3.2.2 Effect of the NW nominal thickness

In this section, we compare two $[0\bar{1}1]$-oriented **NWs** of different nominal InSb thicknesses: 50 and 100 nm-thick. Both **NWs** have a nominal aperture width of 100 nm. Figures 6.12a and b present the extracted $\mathbf{R_{4P}}$ as a function of the probe distance for the 100 nm-thick (sample **SIGG5**) and 50 nm-thick (sample **SIGG2**) InSb **NW** respectively.

Taking into account the lateral overgrowth as well as the increase in the InSb thickness,

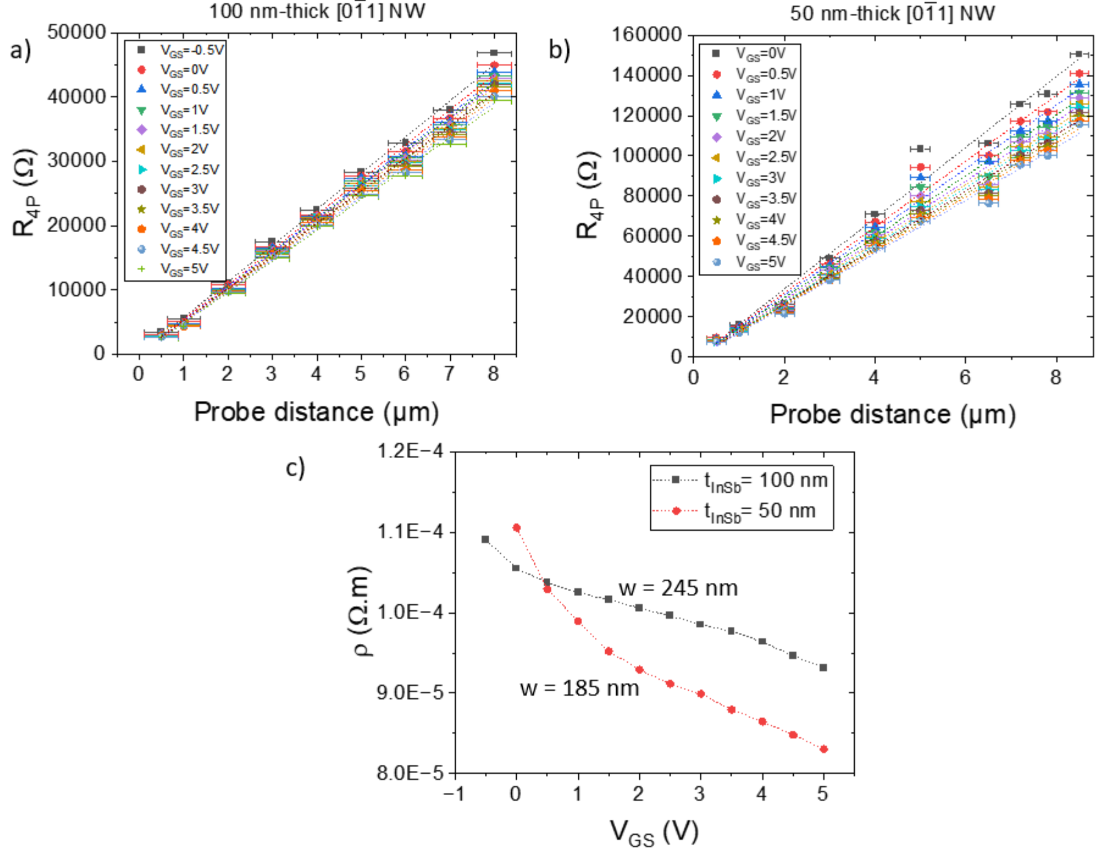


Figure 6.12: a) $\mathbf{R_{4P}}$ vs probe distance for the 100 nm-thick [0$\bar{1}$1]-oriented InSb **NW** (sample **SIGG6**). b) Four probe resistance versus probe distance for the 50 nm-thick [0$\bar{1}$1]-oriented InSb **NW** from sample **SIGG2**. c) Resistivity curves as a function of $\mathbf{V_{GS}}$ for the 50 nm-thick and 100 nm-thick InSb **NW**. The experimental width measured through the top view **SEM** images are indicated for each **NW**.

a geometric factor of 3.1 is obtained from the ratio between the two **NWs** sections: $S_{50\ nm} = 6.27 \times 10^{-15}$ m^2 and $S_{100\ nm} = 1.94 \times 10^{-14}$ m^2. The measured $\mathbf{R_{4P}}$ is consistent with these geometrical differences as a a three-fold increase is observed for the thinner **NW**: for $\mathbf{V_{GS}} = 0$, at $d = 1$ μm the $\mathbf{R_{4P}}$ equals around 15000 Ω versus 5000 Ω for the 50 and 100 nm-thick InSb **NWs** respectively. For larger tip separations, the same behavior is found with 150000 Ω for the 50 nm-thick InSb **NW** and 50000 Ω for the 100 nm-thick **NW**.

Comparing the resistivity as a function of $\mathbf{V_{GS}}$ in Figure 6.12c, the modulation of the charge density inside the InSb **NWs** is noticed from the decreasing trend of the curves. Nevertheless, a more efficient gate modulation is evidenced for the thinner InSb **NW** (50 nm) with a decrease of about 25 % of the resistivity (for $\mathbf{V_{GS}}$ in the 0 – 5 V range) in contrast with a 14 % decrease for the thicker **NW** (100 nm). Indeed, in a thinner channel the gate electric field penetrates more uniformly inside the core of the InSb **NWs** as the characteristic length ($\lambda = \sqrt{(\varepsilon_{InSb}/\varepsilon_{GaInP}) t_{InSb} t_{GaInP}}$) is directly linked to the channel potential by $\phi(x) \propto e^{-x/\lambda}$. With smaller values of λ, *i.e.* smaller values of t_{InSb}, in similar systems (same permittivity and barrier thickness), the drain field decays quickly near the junctions with the channel, hence leading to an enhanced gate control.[255]

6.3.2.3 Effect of the growth orientation on the NW resistivity

This section deals with the influence of the crystallographic **NW** orientation on the resistivity. Because the number of **NWs** per array with a high quality morphology was limited (aperture fully filled with a constant lateral overgrowth over the whole **NW** length), only a few **NWs** could be probed and their transport properties compared for $[1\bar{1}0]$, $[1\bar{2}1]$ and $[0\bar{1}1]$ orientations. The data were collected using the output characteristic script ($I_D = f(V_{DS})$), where the current was swept from -1 to 1 µA. Figure 6.13a shows the extracted $\mathbf{R_{4P}}$ for three differently oriented 100 nm-wide **NWs** as a function of the probe distance.

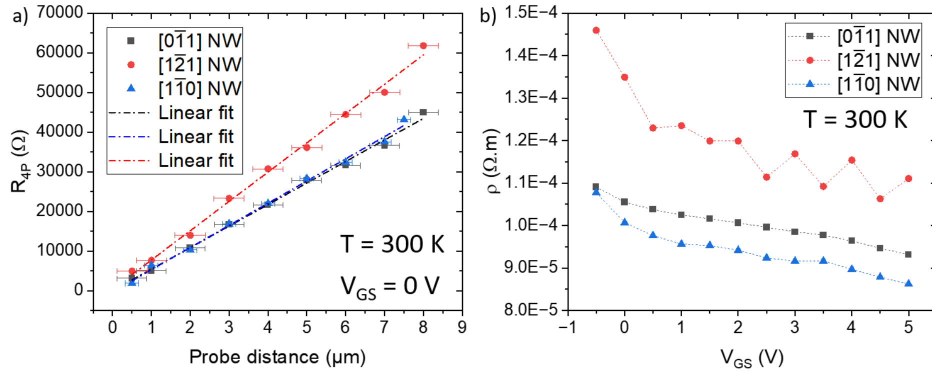


Figure 6.13: a) $\mathbf{R_{4P}}$ vs probe distances for three different **NW** orientations at 300 K and $\mathbf{V_G}$ = 0 V. b) Deduced resistivity (ρ) as a function of the gate voltage for the three different **NWs** at 300 K.

For all three **NWs**, a linear evolution of $\mathbf{R_{4P}}$ with the inner probe distance is evidenced in agreement with similar behavior reported in the literature.[169,256] While quasi-similar results are found for the $[1\bar{1}0]$ and $[0\bar{1}1]$-oriented **NWs** which makes sense as they are two equivalent orientations, the $[1\bar{2}1]$-oriented **NW** exhibits a steeper slope with $\mathbf{R_{4P}}$ reaching a maximum of 61800 Ω for d = 8 µm.

When their resistivity is compared, as seen in Figure 6.13b, this difference between the two main crystallographic orientations is confirmed. As the three **NWs** measured showed the same experimental width of 230 nm, we cannot correlate the slight change of resistivity to geometrical difference. However, the nature of the facets that emerge above the mask may result in different surface Fermi level pining or scattering phenomena.

Regarding the modulation of the charge carrier density inside the Insb **NWs**, quite a difference is observed depending on the **NW** orientation. For $\mathbf{V_{GS}}$ varying from 0 to 5 V, the resistivity decreases of: 15 % for the $[0\bar{1}1]$-oriented **NW**, 20 % for the $[1\bar{1}0]$ one and 25 % for the $[1\bar{2}1]$ orientation. This is mainly due to a more efficient depletion of the carriers for negative gate voltage for the latter orientation and could indicate different energy levels for the surface states of the involved facets.

Based on the sheet carrier density measured on the 2D InSb/GaInP/GaAs heterostructure through Hall effect in section 6.2.1, we assume a sheet electron density (n_{2D}) of 0.6×10^{12} cm^{-2} in the InSb **NWs** at **RT**, whatever their orientation is. Using the resistivity calculated from the $\mathbf{R_{4P}}$ measurements and the following equation

$$\mu = \frac{t}{n_{2D} \times q \times \rho} \tag{6.3}$$

where t is the nominal InSb thickness and q the electric charge (1.6×10^{-19} C), we can evaluate the electron mobility inside the 100 nm wide InSb **NWs**. As the cross-section shape of the **NWs**

is not rectangular, the above equation only gives a rough estimation, but yet interesting, of the electron mobility. For the $<1\bar{1}0>$-oriented **NWs** the electron mobility would be about 10000 $cm^2.V^{-1}.s^{-1}$ and 7800 $cm^2.V^{-1}.s^{-1}$ for the $<11\bar{2}>$-oriented ones. Such values corroborate well with the previous values reported through Hall and **TLM** measurements. For such a mobility, we could estimate a mean free path of around 127 nm at **RT** for $<1\bar{1}0>$-oriented **NWs** and 98 nm for $<11\bar{2}>$-oriented ones according to equation 6.4

$$l_e = \frac{\hbar\sqrt{2\times\pi\times n_{2D}}}{q}\mu \tag{6.4}$$

Nevertheless, the native oxide on the surface of the **NWs** probably degrades the transport properties. Measurements on oxide-free **NWs** at cryogenic temperatures may result in a significant improvement of the electron transport properties.

6.3.2.4 LT transport measurements on InSb NWs

To further assess the transport properties of the in-plane InSb **NWs** on GaInP/GaAs (111)*B*, we performed additional measurements on the same **NWs** (except for the $[1\bar{2}1]$ orientation) at **LT** (113 K). As specified in the previous section, in this temperature range, the risk of both tip and **NW** degradation increased. On top of that, the contacting process was repeated in some cases to ensure the reliability of the measurements.

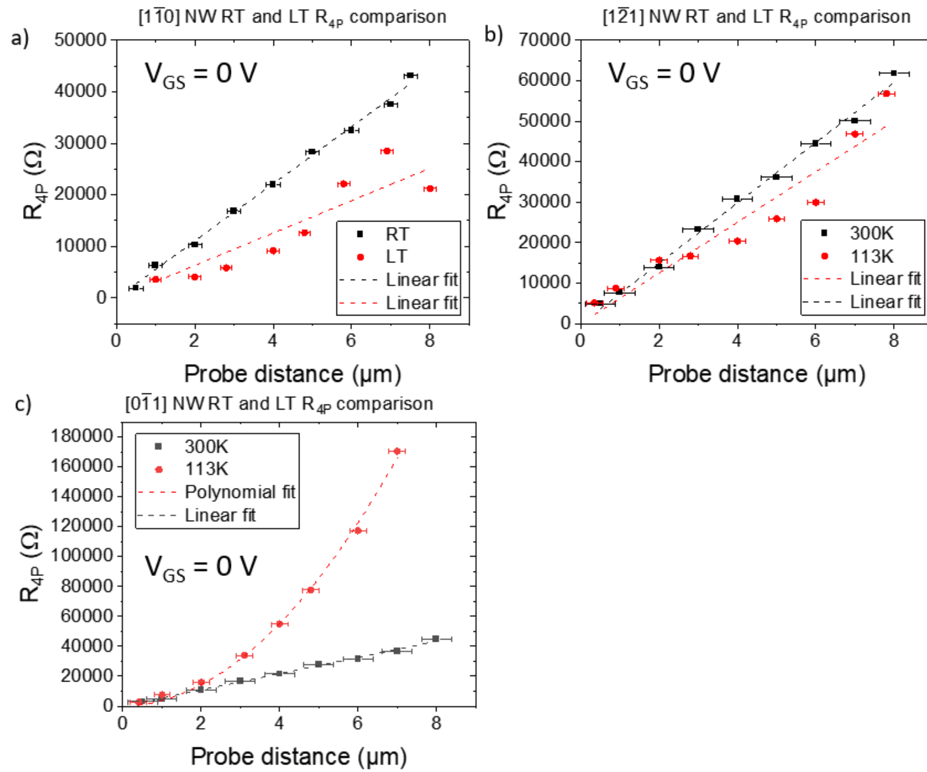


Figure 6.14: $\mathbf{R_{4P}}$ vs probe distance curves at **LT** for a) $[1\bar{1}0]$, b) $[1\bar{2}1]$, c) $[0\bar{1}1]$-oriented **NWs** with $\mathbf{V_G}$ = 0 V. To serve for comparison, the data collected at **RT** is added on the graphs. In the case of $[1\bar{2}1]$ a different **NW** was measured at **LT**.

Figures 6.14a, b and c gather the $\mathbf{R_{4P}}$ measurements at $\mathbf{V_{GS}}$ = 0 and **LT** for all three studied orientations $[1\bar{1}0]$, $[0\bar{1}1]$ and $[1\bar{2}1]$ respectively. In order to emphasize the evolution of the $\mathbf{R_{4P}}$, the curves collected at 300 K are added for comparison.

When looking at the variation of $\mathbf{R_{4P}}$ between **RT** and **LT** for the $[1\bar{1}0]$-oriented **NW** in Figure 6.14a, a significant decrease is observed, reaching more than 50 % for d = 8 µm. This marked difference can be understood as a reduced phonon scattering and thus an increase of the electron mobility at **LT**. If we assume the same electron density as the one measured at **RT**, *i.e.* n_{2D} = $0.6{\times}10^{12}$ cm^{-2}, we can roughly estimate the minimal value of the electron mobility at **LT** using equation 6.3. Extracting the resistivity from the $\mathbf{R_{4P}}$ curve in Figure 6.14a at $\mathbf{V_{GS}}$ = 0 V, we obtain a value of $6.21{\times}10^{-5}$ Ω.m that gives a minimal electron mobility of ~16800 cm^2.V^{-1}.s^{-1} for the $[1\bar{1}0]$-oriented **NW**. As the electron density resulting from thermal activation is lower at **LT**, the increase in the electron mobility should even be more pronounced than what can be expected from the reduced resistance.

Although a different **NW** (experimental width = 220 nm) was measured at **LT** for the $[1\bar{2}1]$ orientation (Figure 6.14b), it is still interesting to make the comparison assuming that the $\mathbf{R_{4P}}$ value at **RT** would be similar to the original **NW**. When cooling down from 300 K to 113 K, the $\mathbf{R_{4P}}$ shows a decrease around 17 % for the largest probe distance. This decrease is consistent with the one found for the $[1\bar{1}0]$-oriented **NW**, signature again of a reduced phonon scattering. However, the smaller magnitude of the decrease may suggest that an additional scattering mechanism dominates phonon scattering for the $[1\bar{2}1]$-oriented **NW** at **LT**, for example scattering by the surface states on the different facets of the **NWs**. When evaluating the electron mobility using the same method as for the $[1\bar{1}0]$-oriented **NW**, we obtain around 9600 cm^2.V^{-1}.s^{-1} for this $[1\bar{2}1]$-oriented **NW** (with an extracted resistivity of $1.1{\times}10^{-4}$ Ω.m).

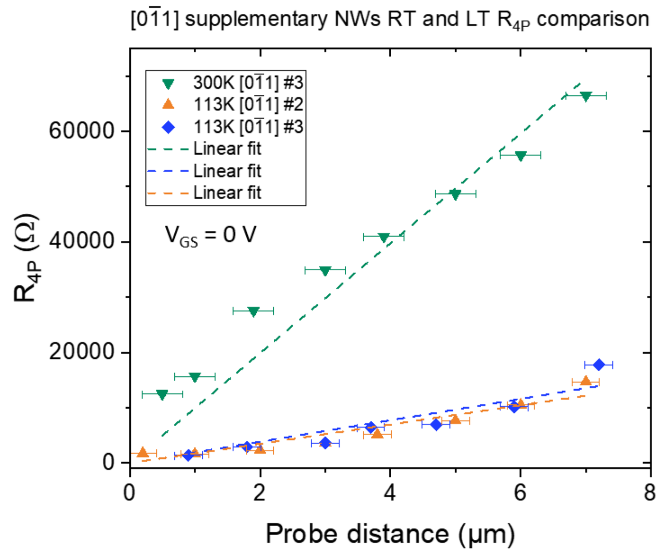


Figure 6.15: $\mathbf{R_{4P}}$ vs probe distance curves at **LT** for additional $[0\bar{1}1]$-oriented **NWs** with $\mathbf{V_{GS}}$ = 0 V. To serve for comparison, the data collected at **RT** is added on the graphs.

For the last orientation $[0\bar{1}1]$, a surprising behavior is evidenced when the same **NW** is measured at 113 K after a previous measurement at 300 K (red curve in Figure 6.14c). The $\mathbf{R_{4P}}$ exhibits a large increase with now a quadratic dependency upon the probe distance. In the **SEM** images (not shown), very light scratches that resulted from the **RT** measurements were visible on the **NW** which we believe are responsible of the sudden change in $\mathbf{R_{4P}}$ variation. Because of

the damage of this **NW**, two additional **NWs** were measured at 113 K and one of them at 300 K thereafter. As seen from the Figure 6.15, these two **NWs** exhibits almost a similar $\mathbf{R_{4P}}$ at 113 K that is 75 % lower than the value at 300 K for d = 7 µm, which confirms the trend observed so far for all **NWs**. Regarding the electron mobility, using the same estimation method with equation 6.3, we can estimate the minimal value of the electron mobility at low temperature (113 K). After calculation, we obtain ~7300 $cm^2.V^{-1}.s^{-1}$ at 300 K (with $\rho = 1.4\times10^{-4}$ Ω.m) and ~22500 $cm^2.V^{-1}.s^{-1}$ at low temperature (113 K) (with $\rho = 4.5\times10^{-5}$ Ω.m) for the $[0\bar{1}1]$-oriented **NW** respectively.

6.3.2.5 Impact of discontinuity on the transport properties

So far, continuous **NWs** have been investigated. But, as shown in the previous chapter, a number of **NWs** consists of several continuous or discontinuous InSb segments. Here, we focus on a **NW** that presented two continuous segments, visible as a change of height variation along the **NW** length.

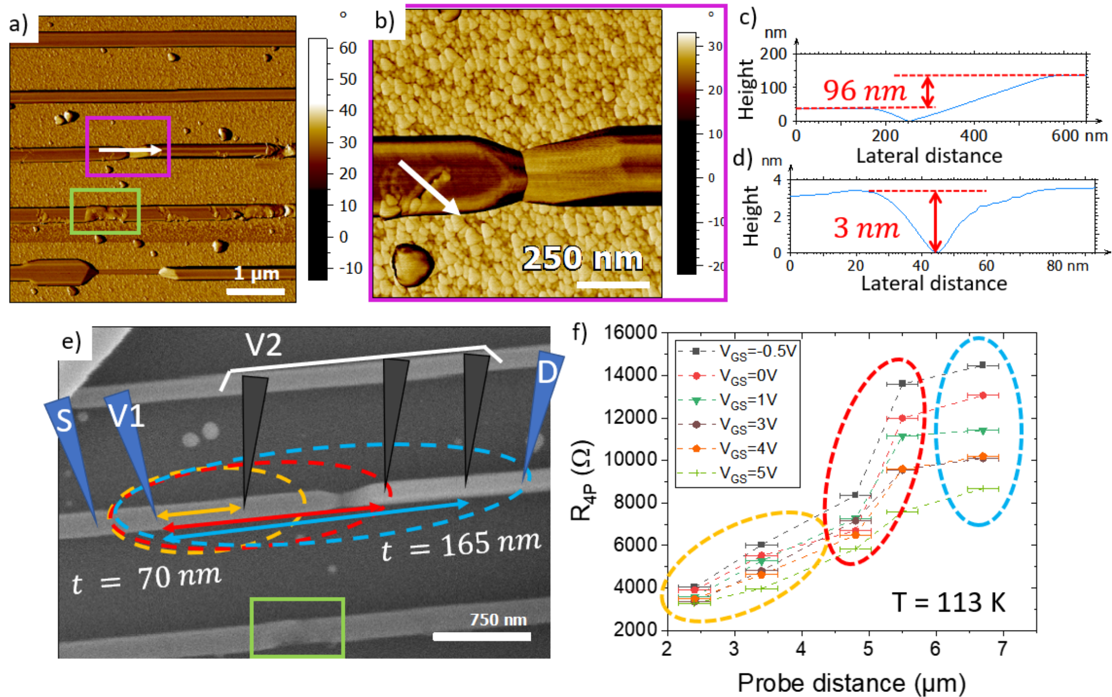


Figure 6.16: a) phase **AFM** image of the $[\bar{1}10]$-oriented **NWs** revealing damages induced by tip contacting. The green rectangle corresponds to the same area depicted in the **SEM** image of e). b) Lower scale phase **AFM** image of the pink rectangle in a). The height variation is clearly seen between the two regions. c) Height profile across the junction of the two InSb segments indicated by the white arrow in a). d) Height profile across the scratch in b) showing a 3 nm deep penetration was done. e) **SEM** image of the **NW** with height variation. The four tips are schematizing the **4PP** measurement configuration. Only V_2 is moving. The yellow region represents the shortest distances. Red region gathers the data point collected when V_2 is placed just before and after the height variation. Blue region corresponds to the largest distance. The green rectangle indicate damages done on an additional **NW** through previous **4PP** measurement. f) $\mathbf{R_{4P}}$ curves vs probe distance for various $\mathbf{V_{GS}}$ at 113 K on the **NW** highlighted in e).

As shown in Figures 6.16a and b, the $[1\bar{1}0]$-oriented **NW** exhibits a region where the InSb thickness decreases strongly then increases at a higher value than the nominal thickness of 100 nm. Figure 6.16c shows clearly that the right segment is 96 nm above the left segment which was verified to be 100 nm high compared to the GaInP surface. Hence, the right segment reaches almost a thickness of 200 nm. We attribute this transition to the coalescence of two nucleation sites with two different types of islands as seen in Figure C.1a on the **NW** at most left of the **SEM** image. The **NW** resistance was measured for several probe distances before and after the constriction to assess its impact on the transport properties (V_2 moving only). The data was acquired at **LT** (113 K).

From the $\mathbf{R_{4P}}$ curve in Figure 6.16f, three different domains can be established. The yellow section represents the smaller distance where V_1 and V_2 were contacted on the thinner part of the **NW** on the left side of Figure 6.16e. The red region gathers the probe distances just before and after the height variation. Eventually, the blue region represents the largest distance when V_2 is placed further on the thicker part of the **NW** (right side of Figure 6.16e). For small distances (yellow region) on the thinner part of the **NW**, the $\mathbf{R_{4P}}$ remains low with moderate gate modulation efficiency because the small distance between the probe causes a small potential drop. When probing the resistance across the constriction area (red region), a clear jump in the $\mathbf{R_{4P}}$ value is observed. This increase results from the potential barrier induced by the constriction. In the blue region, we retrieve a smaller slope and a better gate switching efficiency. Through increased gate voltages, an interesting behavior is revealed on this **NW** as the impact of the thickness variation on the $\mathbf{R_{4P}}$ value is reduced for larger values. When $\mathbf{V_{GS}}$ is set at -0.5 V, in the depletion mode, the resistance jump equals 62 % of its initial value while for $\mathbf{V_G}$ = 5 V, in the accumulation mode, only a 30 % increase of the resistance is observed after crossing the constriction. This behavior is attributed to the accumulation of electrons near the bottom interface of the channel, reducing the impact of the **NW** thickness variation (Figure 6.16f).

6.3.2.6 Probe invasiveness on the transport properties

The quadratic behavior of the $\mathbf{R_{4P}}$ at 113 K for the original $[0\bar{1}1]$-oriented **NW** stressed the importance of preserving their integrity and limit as much as possible the induced defects on the **NW** from the tip contacting processes. The mechanical impact of the probe was characterized in the **AFM** phase image. For example, a $[0\bar{1}1]$-oriented **NW** that was unintentionally degraded at **LT** shows a damaged region in the green rectangle in Figure 6.16a. This damage looks way more severe than what is just visible in the **SEM** image of Figure 6.16e. Moreover, focusing on the same **NW** away from the green rectangle, several scratches are seen along the whole length of the **NW**. A magnified view of a scratch induced by a potential probe is highlighted in Figure 6.16b. Acquiring the height profile across this scratch shows a 3 nm deep impact in Figure 6.16d, meaning that the native oxide was certainly pierced despite a lot of care to avoid high contact pressure by the tip.

Therefore, we investigated, the impact of these defects on the transport measurements. As depicted in Figure 6.17a, we repeated measurements at 300 K on the original $[0\bar{1}1]$-oriented **NW** following the data acquisition performed at 113 K. All the damages that resulted from these **RT** (lower left inset) and **LT** (top right inset) experiments are shown in Figure 6.17a.

The transport measurements are repeated in both the conventional configuration (V_1 is moving to shortest probe distance, V_2 kept fixed) called “RT-bis” from the Figure 6.17b and the reverse configuration (V_2 moving, V_1 fixed) labeled “RT-bis-reverse”. At $\mathbf{V_{GS}}$ = 0 V, a clear increase of about 25 % in the slope of $\mathbf{R_{4P}}$ is observed for this second phase of measurements at **RT**, confirming the negative impact of the defects created on the transport properties. Irreversible structural damages were caused by the tips on the InSb **NW** (scratching, plastic deformation,

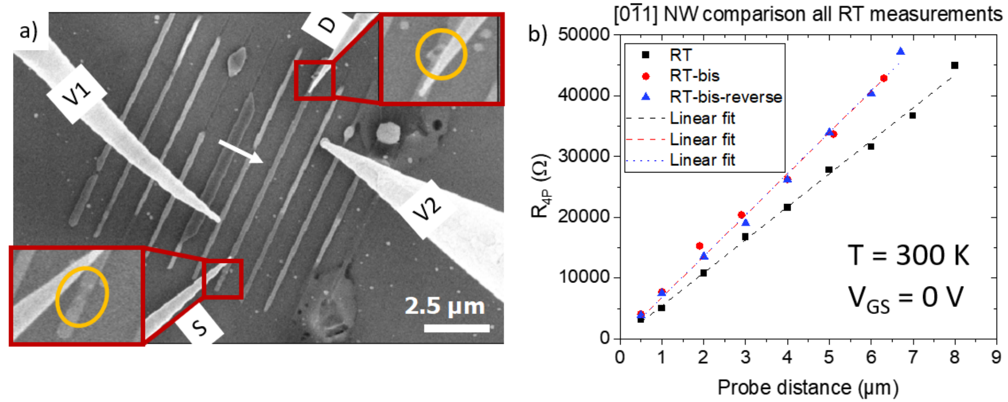


Figure 6.17: a) **SEM** image of the second measurements at **RT** on the $[0\bar{1}1]$ **NW** after damages induced from tip contacting. The **NW** of interest is pointed by the white arrow. In the bottom left red rectangle, the damage from the first **RT** measurement is seen. In the upper right corner, a magnified view reveals the damage caused at the end of the **LT** measurement. b) $\mathbf{R_{4P}}$ vs probe distance comparison for both measurements at 300 K and $\mathbf{V_G}$ = 0 V.

local disruption or even melting and vaporization). These introduced defects most probably act as localized scattering centers or local potential barriers both contributing to a reduced carrier mobility and higher resistance.

Moreover, the effect of the tip contact pressure, especially at **LT** (113 K), was studied through a simple experiment on a 100 nm-wide $[\bar{1}01]$-oriented **NW** where no previous measurements were performed. For the first acquisition of data, the normal contacting method was used for all of the four probes as mentioned in section 6.3.1, *i.e.* the tips are gently pushed down until the pre-amplifiers saturate in current. Then, for the second measurement, we intentionally pushed the V_1 probe by 20 nm further down onto the **NW** surface to get a stronger contact pressure and performed the transport measurement, as schematized in Figure 6.18a.

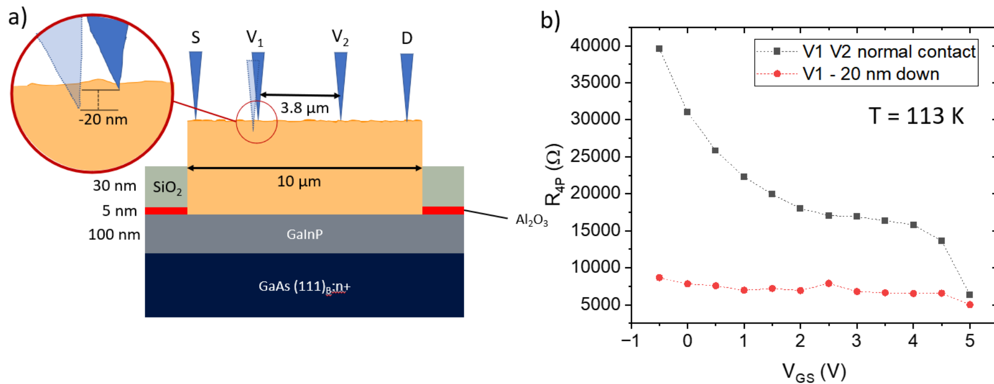


Figure 6.18: a) Schematic of the tip contact pressure experiment in the **4PP** configuration. A first set of data is acquired using the normal contacting method. Then, only the tip V_1 is pushed down for 20 nm to get a stronger contact. The inset shows a magnified view of the difference between the two contacts. The second contact of the probe V_1 is laterally shifted for clarity purpose. b) $\mathbf{R_{4P}}$ vs $\mathbf{V_{GS}}$ for the two different tip contact pressures. Inset: Schematic of the **4PP** measurement that illustrates how tips affect the potential distribution along the **NW**.

The extracted $\mathbf{R_{4P}}$ as a function of $\mathbf{V_{GS}}$ shown in Figure 6.18b reveals significant variations in the modulation behavior and the overall value of $\mathbf{R_{4P}}$ depending on the contact pressure on V_1. In the case of the usual normal contact, the $\mathbf{R_{4P}}$ exhibits a reduction of 80 % in its value along the $\mathbf{V_{GS}}$ voltage range (-0.5 to 5 V) which is a consistent behavior with the different **NWs** measured so far.

Conversely, when the contact pressure on the probe V_1 increases, the resulting $\mathbf{R_{4P}}$ value drops significantly and the gate command efficiency is degraded. This suggests that the tips are impacting the electric field distribution along the **NW**. When the tip penetration depth is increased, it can locally screen the gate electric field and introduce a local potential barrier, hence affecting the current flow as well as the gate control. This invasiveness of the **4P-STM** tips was well described by Aprojanz *et al.* which was found to strongly impact the $\mathbf{R_{4P}}$ extracted from **4PP** measurements on the graphene nanoribbons sidewalls when pressing.[257]

Conclusion

Through this section, **4P-STM** transport measurements were performed on in-plane InSb nanoplatelets and **NWs** on GaInP/GaAs:n+ substrates. The former nanostructures confirmed the efficient gate command when a voltage is applied on the backside of the doped substrate. At **LT** (113 K), the gate switching efficiency is improved and the current is increased by a factor 120 when $\mathbf{V_{GS}}$ switches from -0.5 V to +3 V. Moreover, an ambipolar behavior of the device related to the narrow band gap of InSb is evidenced consistently with **TLM** measurements on large scale devices. In the **4PP** configuration, the measured sheet resistance R_{sh} is also in good agreement with the values determined by Hall and **TLM** measurements. Some differences are deemed to arise from the field distribution change induced by the **STM** tips which are local contacts instead of uniform lateral metallic pads that covers the whole width of the structure in **TLM** devices.

In the case of in-plane **NWs**, various parameters were investigated to analyze their impact on the InSb transport properties. The first two studies upon the effect of the **NW** aperture width or the InSb nominal thickness revealed marked changes upon the transport efficiency. As a matter of fact, the narrower **NW** exhibits a higher resistivity due to the geometrical confinement that increases the surface-to-volume ratio and the larger scattering of electrons facets roughness and surface states. Similarly, for a thinner **NW** (50 nm vs 100 nm), the $\mathbf{R_{4P}}$ is also found higher for the same reason. Nevertheless, the modulation of the charge carriers is improved and becomes more sensitive as a result of the enhanced gate electric field penetration.

As anticipated from the morphological differences observed in **SEM** in the section 5.4.3.2 of chapter 5, a higher resistivity is found for the $[1\bar{2}1]$-oriented **NW** compared to the $[0\bar{1}1]$ or $[1\bar{1}0]$-oriented one which can be related to an increased defect density inside the $[1\bar{2}1]$-oriented nanostructure. At **LT** (113 K), a decrease in the $\mathbf{R_{4P}}$ value is observed on undamaged **NWs** for all orientations which suggests a strong increase of the mobility while the carrier density shrinks. Through a simple estimation method, a rough minimal value of the electron mobility at **LT** was given, reaching more than 22000 $cm^2.V^{-1}.s^{-1}$ for $[0\bar{1}1]$-oriented **NWs**.

The complexity to probe ballistic properties does not only rely on cryogenic temperature but also on the integrity of the **NW**, their surface state, and the tips invasiveness. Through the different studies of the impact of the defects on the transport properties, we showed that the tip contacting process induces damage on the surface of the **NWs** that are directly responsible for an increased $\mathbf{R_{4P}}$. Depending on the contact pressure, the contact resistance also changes and the tips can impact the electric field distribution along the **NW**.

6.4 STM and STS analysis of InSb thin films on GaInP/GaAs substrates

As the native oxide layer and surface states of the InSb **NWs** can be a serious source of electron mobility degradation, for this last section, we aim at establishing a reliable preparation process for the desorption of the InSb native oxide. This would benefit for a future measurement of the transport properties on a clean and well-ordered **NW** surface. The second interest in this study is the investigation of the surface reconstruction of InSb on GaInP/GaAs substrate by **STM**. Thirdly, an **STS** study will also be performed to probe the **LDOS** on the InSb reconstructed surface.

We first focused on the surface of thin-films, as **STM** images can be acquired anywhere on the sample, in contrast to **NWs** which are more difficult to localize with the tip in the **LT-STM** because of the presence of the dielectric mask between the nanostructures. The prepared sample consists of a 30 nm-thick InSb layer (grown under the following conditions: $\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 385 °C, V/III ratio = 136) on a 20 nm-thick GaInP layer (grown at $\mathbf{V_G}$ = 0.2 **ML**/s, $\mathbf{T_G}$ = 520 °C, V/III ratio = 50) on GaAs $(111)_B$ p-type substrate (1.5×10^{19} cm^{-3}). The GaInP layer thickness is voluntarily reduced to ensure tunneling through the substrate. During InSb growth a streaky (2×2) **RHEED** was observed.

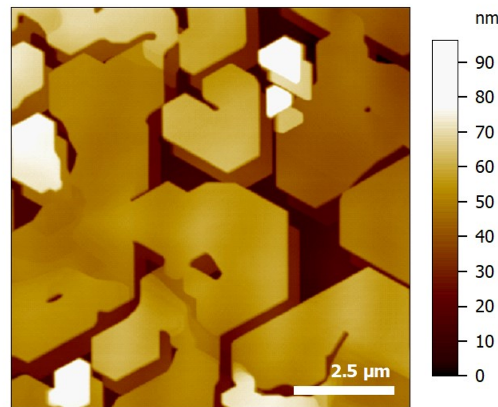


Figure 6.19: **AFM** image of a 30 nm-thick InSb layer grown on a GaInP/GaAs sample ($\mathbf{V_G}$ = 0.05 **ML**/s, $\mathbf{T_G}$ = 385 °C, Sb/In = 136). The GaInP layer has a thickness of 20 nm and was grown with the following conditions: $\mathbf{V_G}$ = 0.2 **ML**/s, $\mathbf{T_G}$ = 520 °C, V/III ratio = 50. The **AFM** tip apex was double during scanning, creating this false-stepped structure near the islands edges.

As seen from Figure 6.19, the surface coverage was found to be slightly lower than the one previously observed for **IGG4** in chapter 5 section 5.3.3.2 with only 86 % of coverage rate, despite the use of similar optimized growth conditions. The surface roughness of the thinner GaInP layer could be incriminated in this case. The morphology of the sample revealed 2D and 3D InSb islands with some of them up to 90 nm in height compared to the GaInP background. Nevertheless, the 2D islands are sufficiently large to enable **STM** experiment safely.

6.4.1 InSb on GaInP on GaAs $(111)_B$ surface reconstruction

The preparation steps of this InSb surface were identical to the one described for the InSb/GaAs surface in chapter 4, section 4.3.2. After outgassing the sample for 12 hours at 120 °C in the

loadlock following the introduction under **UHV**, the sample was transferred in the preparation chamber and deoxidized using a thermal annealing combined with a $\mathbf{H_{AT}}$ exposure thanks to an ion gun (described in chapter 2). The first step consisted of an annealing step for 1 h 30 without $\mathbf{H_{AT}}$ followed by another cycle of 1 h 30 under $\mathbf{H_{AT}}$ exposure. Unfortunately, unstable tunneling conditions revealed a poorly deoxidized surface. Hence, a second step was performed for which the annealing temperature was increased up to 340 °C and the sample exposed to $\mathbf{H_{AT}}$ for 1 h 30. Then, the $\mathbf{H_{AT}}$ flux was stopped and the annealing was maintained at the same temperature for 1 h 30. After that process, a stable tunneling current was obtained giving rise to high resolution **STM** images. The deoxidized InSb (111) surface on GaInP / GaAs $(111)_B$ shown in Figure 6.20a contrasts with the former holey surface of the InSb thin film on GaAs $(111)_B$ in chapter 4, Figure 4.9a.

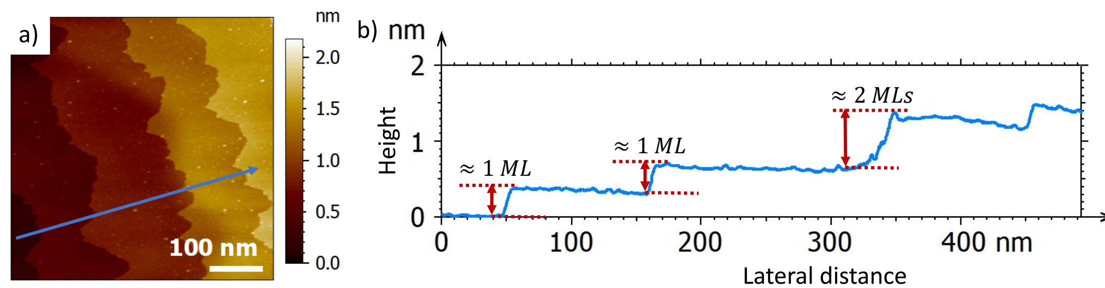


Figure 6.20: a) **STM** image of the 30 nm-thick InSb layer grown on a 20 nm-thick GaInP on GaAs $(111)_B$ sample. The **STM** image was acquired in the central area of the sample (bias V = -1 V, $I_{setpoint}$ = 50 pA). b) Stepheight profile acquired along the blue arrow in a) illustrating the monolayer and bi-layer atomic terraces. The variation of contrast observed on individual terraces is caused by non-linearity effects of the **STM** scanner.

Instead, the surface reveals terraces with no pit. When the step height is measured across several terraces in Figure 4.9b, there is a coexistence between monolayer and bi-layer steps. The observation of well-defined terraces indicates a reduced Sb desorption and the absence of In diffusion during the deoxidation process. As the appearance of vacancy islands, observed in chapter 4, Figure 4.9a was attributed to the stoichiometric Langmuir evaporation of both group III and V atoms (agreeing with similar observations on InAs **NWs** surface[210]), the difference in the surface morphology between both samples might be caused by the temperature of the sample during the preparation. It was probably slightly lower than for the previous sample, although the thermocouple on the manipulator pointed to the same temperature of 340 °C.

Because the change of morphology can involve different atomic structures, high resolution **STM** images were also recorded. Figure 6.21a depicts a 10 nm x 10 nm **STM** image of the InSb $(111)_B$ surface. As a matter of fact, the surface reconstruction is consistent with what was observed and speculated already in chapter 4 section 4.3.2 that is to say the preferential Sb desorption from the surface due to the high temperature annealing leading to the In-rich (3×3) surface reconstruction. The (3×3) periodicity is confirmed through the **FFT** visualization in Figure 6.21b, where the inverse of the spacing between the neighboring spots matches well with the theoretical value of 1.374 nm or through a line profile from the reconstructed surface in Figure 6.21c. In addition to the bright protrusions, features with a fainter contrast are also observed, as highlighted in the white rectangle of Figure 6.21a. It shows a ternary symmetry, consistent with a trimer, suggesting the formation of β-rings at a small concentration. Such an analysis is supported by Figure 6.22a, which shows the InSb surface with the (3×3) reconstruction with a small concentration of dark sites at a larger scale. Also, we note the absence of In-chains, indicating that the sample has not been heated as high as the InSb/GaAs sample.

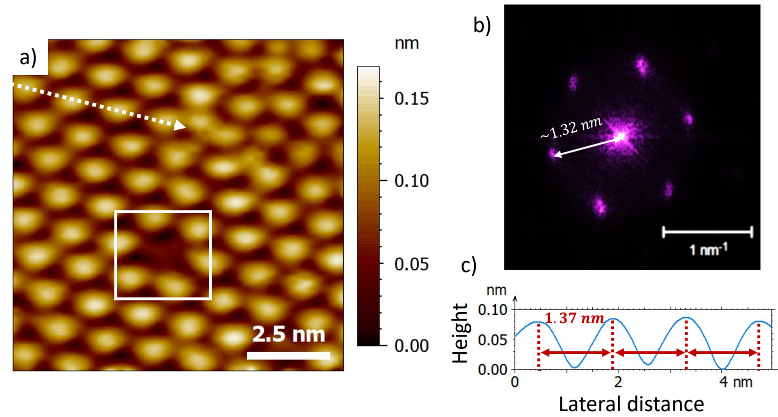


Figure 6.21: a) High resolution **STM** image of the 30 nm-thick InSb layer grown on a 20 nm-thick GaInP on GaAs $(111)_B$ substrate and acquired in the central left area of the sample (sample bias V = -1 V, $I_{setpoint}$ = 50 pA). b) **FFT** spectrum of a larger view **STM** image showing the (3×3) periodicity. c) Line profile taken along the white arrow in a) showing the (3×3) periodicity.

6.4.2 Tunneling spectroscopy of the InSb surface grown on the GaInP/GaAs $(111)_B$ heterostructure

To further probe the electronic structure of this InSb (3×3) reconstructed surface, **STS** was performed at 77 K using a variable tip-sample separation.[258] To increase the transmission probability of the tunneling junction and better resolve the band edge of InSb, a Z-spectroscopy script was implemented to move the tip towards the InSb surface by 400 pm during the negative bias sweep and then retract the tip by the same distance during the positive bias sweep. The setpoint current was 500 pA.

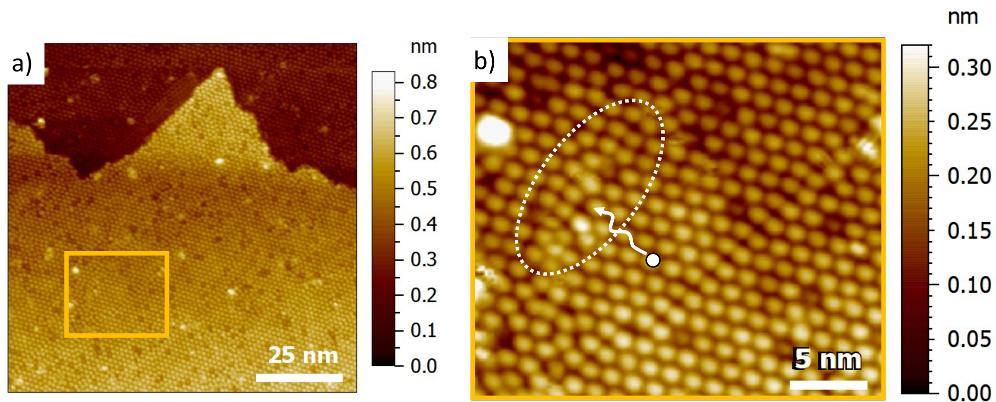


Figure 6.22: a) **STM** image of the InSb $(111)_B$ surface grown on the GaInP/GaAs heterostructure (sample bias V = -1 V, $I_{setpoint}$ = 50 pA). b) Zoom to highlight the lack of long-range periodicity. The white arrow indicates the thermal drift from the starting position during overnight Z-spectroscopy data collection. The white dotted ellipse represent the resulting area after thermal drift over the night.

As illustrated in Figure 6.22b, local defective sites can be seen such as a twin boundary crossing diagonally the image, missing atoms or disordered regions. For the following spectroscopic analysis, the “Z-**STS**” (called this way because it combines usual **STS** with a Z-height variation during the spectroscopy) was started at the location defined by the white spot in Figure 6.22b

and lasted 18 hours (overnight script). Over such long scanning time, inevitable thermal drift occurred which will serve for our discussions. The white arrow indicates the guessed thermal drift direction with the dotted circle surrounding defective locations which were visited upon the drift of the scanner.

Among all scans, the most representative results are presented in Figure 6.23. At first, the **STM** tip was positioned in an ordered region, on a bright protrusion surrounded by other bright protrusions giving rise to the (3×3) structure (white circle). The first observation that can be done in Figure 6.23a is the existence of a small region where the differential conductance is close to zero. This region is narrower than the value of 0.23 eV for the band gap of InSb at 77 K.

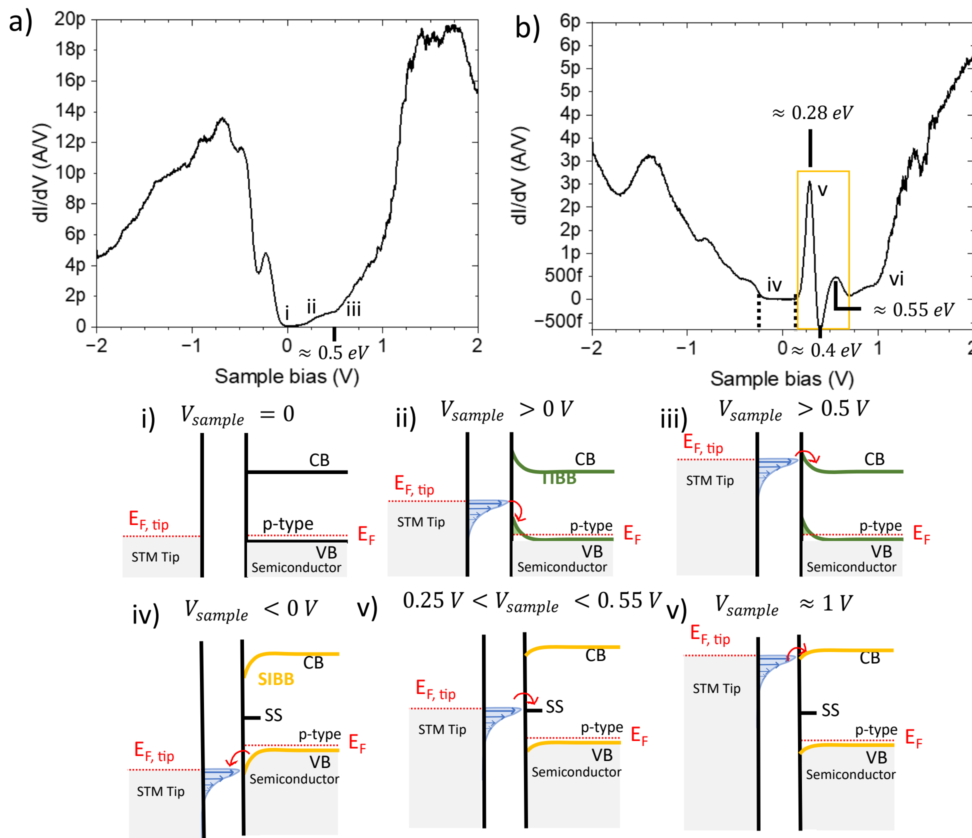


Figure 6.23: a) dI/dV spectra acquired through Z-**STS** at 77 K on an "ordered" region of the InSb (111) (3×3) surface. b) dI/dV spectra acquired through Z-**STS** at 77 K on a "defective" region of the InSb (111) (3×3) surface. Schematic energy diagrams: i) with no sample bias; ii) with a small positive sample bias inducing a **Tip Induced Band Bending (TIBB)** that increases slightly the probed current; iii) with larger positive bias, the Fermi level of the tip aligns with the conduction band. iv) At negative sample bias, the positively charged (+) surface state in the band gap provokes a downward band bending that shifts the valence band edge away from the Fermi level (0 V). v) With increasing sample bias, a negative differential resistance is observed in b) due to the the tip Fermi level resonating with the surface state at maximum tunneling probability. vi) For $V_{sample}\approx1$ V, the tip Fermi level aligns with the conduction band. The tunneling probability (exponential decay) is shown in blue between the **STM** tip and semiconductor sides. Larger blue arrows mean a higher tunneling probability is found.

Based on the position of the Fermi level (0 V) with respect to the edges of the zero-conductance region, E_F is almost pinned at the top of the valence band (Figure 6.23a and on the corresponding diagram i) on the well-ordered InSb (3×3) reconstructed surface, consistent with Dong *et al.*[198]. Because the InSb and GaInP layers were not intentionally doped, the tip causes a small band bending at positive bias. Therefore, when the sample bias is increased, as shown on the diagram ii. in Figure 6.23, the **TIBB** allows empty valence band (**VB**) states to contribute to the current. With further increase in the sample bias, the tip Fermi level becomes aligned with the conduction band (**CB**) states of the InSb layer (diagram iii. of Figure 6.23a). These states account for the tail of the signal observed up to the onset, around +0.5 V, hiding the true edge of the conduction band.

Now, looking at Figure 6.23b), significant changes are observed in the differential conductance dI/dV curve. The first evidence is the shift of the valence band edge away from the Fermi level near -0.25 V, which is correlated with the presence of a localized surface state (**SS**). Despite the exact location of the measurement is unknown due to the thermal drift, it is clear that the underlying surface is defective (as highlighted in the dotted circle from Figure 6.22b). We believe this defect to be positively charged (+), as in such case, a downward band bending is caused by **Surface Induced Band Bending (SIBB)**, which explains the shift of the valence band edge towards more negative value as shown in the schematic diagram iv. of Figure 6.23b.

Secondly, at the right of the Fermi level, a clear and strong **Negative Differential resistance (NDR)** is observed. Indeed, with further increase in the sample bias, the Fermi level of the tip aligns and resonates with the surface state energy level (located in the bandgap) at the maximum of the tunneling probability, causing this strong increase in the current as schematized through the diagram v. of Figure 6.23b. The **NDR** as well as the positively charged defect that creates this surface state are consistent with other works that reported such behavior, for example when an isolated Si dangling bond state was probed at the passivated surface of the Si $(111)_B$ $(\sqrt{3} \times \sqrt{3})$ surface.[259,260,261] Eventually, with further increase in the sample bias, the tip Fermi level reaches the conduction band states allowing for the current to increase again ~1 V as observed in Figure 6.23b and shown in the diagram vi. To conclude on the nature of the defect, this latter remains nonetheless complex to assume as the surface presents some disordered regions, but the observed (3×3) reconstruction so far points out to a Sb desorption that may favor Sb vacancies (donors). This would also be consistent with the positively charged defect accounting for the strong shift of the valence band edge with respect to E_F.

Conclusion

To conclude this section, the structural and spectroscopic analysis of a 30 nm-thick InSb thin film on 20 nm-thick GaInP on GaAs $(111)_B$ using **STM** and **STS** demonstrated both some differences and similarities with the InSb surface when it is directly grown on GaAs $(111)_B$. While the reconstruction of the surface is similar with a (3×3) periodicity consisting of mainly γ-rings (In_4Sb_2 clusters), the InSb surface is not holey as in the case of InSb on GaAs (chapter 4, Figure 4.9a). It demonstrates how essential is the control of the sample temperature during the desorption of the native oxide.

With regards to the spectroscopic analysis, a clear evidence of a localized state in the band gap of InSb via the measurement of a **NDR** was observed in a disordered defective region. Although we were able to identify the nature of the defect, such localized energy level may act as surface traps. As the **STM** image revealed that the InSb surface is not perfectly ordered, we expect a significant concentration of such defects, which can considerably impact the transport properties of the InSb layer. Therefore, the surface preparation process is of utmost priority to prevent important scattering in the InSb layer.

6.5 Conclusion

In summary, this chapter demonstrated the efficiency of the InSb/GaInP/GaAs:n+ heterostructure for enabling a back-gate control of in-plane InSb nanostructure conduction. The transport properties investigated in several ways (Hall, **TLM**, **4P-STM**) highlighted a consistent electron mobility exceeding 10000 $cm^2.V^{-1}.s^{-1}$ at 300 K, either in the case of 2D thin films or in-plane **NWs**. This value overpasses the previously reported values for a highly mismatched InSb thin film with similar thickness.[101] The **LT** (113 K) **4P-STM** measurements suggested an enhancement of the transport properties. Nonetheless, we also highlighted tip contacting damages and invasiveness that can disturb the reliability of the collected data if cares are not taken. As the electron transport properties are probably still limited by the presence of a native oxide layer at the surface of InSb, we investigated the possibility to deoxidize InSb with an annealing under a $\mathbf{H_{AT}}$ flux produced by an ion-gun in a **STM** preparation chamber. The observation of a (3×3) reconstructed surface free from In-chains as well as the spectroscopic measurement that could be performed with the **LT-STM** confirmed the efficiency of the deoxidization process, that could be contemplated for the electrical characterization of oxide-free InSb **NW** in the **4P-STM** set-up.

Conclusion

This thesis project, which was devoted to the epitaxial growth and near-field characterization of InSb nanostructures, delivered promising results as well as valuable understandings for their possible integration into advanced electronic devices. After reviewing the applications, fabrication methods, and transport properties of InSb reported in the literature (chapter 1), the various growth and characterisation techniques employed in this study were described in detail (chapter 2). In order to achieve the defined objectives of producing high-quality InSb nanostructures and integrating them into a back-gated heterostructure to modulate their charge density, the research was divided into four main areas. In chapter 3, the epitaxial growth of InSb thin films and nanostructures on the lattice-matched substrate CdTe was investigated. In chapter 4, the focus shifted to the epitaxial growth of InSb on a highly mismatched substrate, GaAs. Eventually, chapter 5 investigated the epitaxial growth of InSb thin films and nanostructures on a semiconductor barrier lattice-matched to GaAs substrates before chapter 6 evaluated their transport properties and charge density modulation by applying a bias on the doped GaAs substrate.

Starting with InSb growth on a CdTe (001) substrate at temperatures above 350 °C, we observed strong interdiffusion of Cd and Te species throughout the InSb layer. This, combined with the InSb defective morphology, forced us to shift the growth to a CdTe (111) substrate, while decreasing the temperature to avoid intermixing. Therefore, when the growth temperature and V/III ratio were kept low (below 330 °C and 20, respectively), smooth InSb thin films with sub-nanometer **RMS** roughness could be grown on CdTe (111) substrates with reduced Cd and Te interdiffusion. However, in the context of **SAG**, the use of $\mathbf{H_{AT}}$ exposure to enhance selectivity and avoid parasitic nucleation on the mask resulted in significant etching of the CdTe substrate. To protect the CdTe surface, a thin GaSb capping layer was grown on the CdTe substrate. Nevertheless, a similar result was observed with a CdTe etching occurring through the GaSb layer, questioning the growth of high-quality InSb nanostructures on CdTe substrates.

Given the complexity of optimizing the InSb growth on the only CdTe lattice-matched substrate, we adopted another approach with the growth of InSb on lattice-mismatched substrates, in this work, GaAs. Based on prior studies from the EPIPHY team about the InSb growth on InP (111) substrates, we showed in chapter 4 that smooth InSb thin films and nanostructures could also be achieved on GaAs $(111)_B$ substrates under optimized growth conditions: $\mathbf{T_G} \approx 390$ °C, $\mathbf{V_G} = 0.05$ **ML**/s and Sb/In ratio of 136. With the help of numerous characterization techniques, a clear sensitivity of InSb upon the underlying GaAs surface roughness was evidenced. When the InSb thin film was grown on either a GaAs buffer layer or a (3×3) reconstructed (Ga-rich) GaAs deoxidized surface (obtained at intermediate temperature ∼500 °C), it resulted in a layer consisting of 3D islands with a poor surface coverage rate. Conversely, on (2×2) (As-stabilized)

GaAs reconstructed surface, the InSb coalesced rapidly, as instant plastic relaxation happens due to the high lattice mismatch with GaAs, to form a smooth layer with very few holes.

Exploiting this promising morphology from the thin films experiments, the **SAG** InSb on GaAs $(111)_B$ resulted in a smooth growth with continuous in-plane **NWs** up to 10 µm-long. A cross-sectional **STEM** analysis highlighted the presence of a periodic **MD** network, confined at the InSb/GaAs interface, which ensures a quasi-full relaxation. The resulting InSb in-plane **NWs** showed off some twinned region (arising from **SF**s) near the interface, although these planar defects are probably correlated to the aperture sidewalls. Away from this region, no further defects were found in most of the InSb **NWs** exhibiting a planar morphology, but a lateral overgrowth developed once the mask surface is reached. This latter phenomenon was more pronounced for $[11\bar{2}]$-oriented **NWs** whereas $[1\bar{1}0]$-oriented **NWs** did not showcase such problems but remained straight and continuous.

Eventually, **STM** investigations of the InSb (111) 2D surface revealed a change from the (2×2) reconstruction after growth to a (3×3) disordered surface induced by the desorption of the native oxide after the air exposure of the sample. Such a modification of the surface structure could have an influence on the conductivity of the **NWs**.

Following these results, chapter 5 explored the epitaxial growth of two candidates for the semi-conducting barrier, $Al_{0.8}Ga_{0.2}As$ and $Ga_{0.51}In_{0.49}P$ on lattice-matched GaAs $(111)_B$ substrate. We showed that the growth of $Ga_{0.51}In_{0.49}P$ produced a low **RMS** roughness layer, while the $Al_{0.8}Ga_{0.2}As$ layer exhibited a large density of trenches, responsible for an increased roughness. An attempt to further improve the smoothness of the GaInP layer was done by introducing Sb as a surfactant, but the amount of Sb to get a beneficial effect was hardly controllable.

In a second time, the subsequent growth of InSb on GaInP on GaAs $(111)_B$ reasserted the impact of the underlying surface roughness on the InSb structural and morphological properties. Notably, the V-element overpressure used for GaInP deoxidation revealed that using an As overpressure rather than a P one produced a smooth InSb layer with few holes. Furthermore, a study of the growth temperature indicated that Sb clustering or 3D InSb islands growth were avoided when similar temperature ranges to those employed for InSb on GaAs were used (380 – 400 °C).

The transition towards **SAG** of InSb on GaInP/GaAs pseudo-substrates rapidly dismissed the dual-**SAG** option, as the growth of InSb on top of the GaInP **NWs** only followed a 3D islands growth regime with a larger nucleation density at the edges of the GaInP **NWs**. In contrast, when the InSb was grown under optimized conditions inside apertures defined on patterned GaInP surfaces, especially when the deeper dielectric mask B (Al_2O_3/SiO_2) was used, up to 10 µm-long in-plane InSb **NWs** were achieved. Consistently with the results of chapter 4, the crystal quality of in-plane InSb **NWs** exhibited an orientation dependency with sharper and faceted $[1\bar{1}0]$-oriented **NWs** compared to $[11\bar{2}]$-oriented ones. The lateral overgrowth was resolved through the **STEM** cross-sectional analysis as well as the same periodic **MD** network at the InSb/GaInP interface. We presumed that the roughness at the InSb/GaInP interface compared to the more abrupt InSb/GaAs interface is responsible for the slight decrease in the success rate of continuous and long **NWs**.

The final chapter closed up this project with the assessment of the transport properties inside InSb/GaInP/GaAs heterostructures. For both InSb thin films and in-plane nanostructures, an electron mobility exceeding 10000 $cm^2.V^{-1}.s^{-1}$ at **RT** was consistently observed through the several characterization techniques used, such as Hall, **TLM** or **4P-STM** measurements. This result outperformed the previously reported value in the literature of 4500 $cm^2.V^{-1}.s^{-1}$ for

similar InSb thickness on GaAs (111) substrate, which highlighted the improvements of the Insb structural quality on highly mismatched substrates. This major achievement was topped up with the demonstration of an efficient modulation of the charge density inside the InSb nanostructures by applying a back-gate voltage on the n-doped GaAs substrate. Throughout the **4P-STM** study, the measurements at **LT** (113 K) stressed the invasiveness of the **STM** tips as well as the importance of the surface integrity of the **NWs** to reach higher mobilities.

Moreover, the last section of the chapter attempted to provide a controlled deoxidation process of the InSb surface after annealing under a $\mathbf{H_{AT}}$ produced by an ion gun. Nevertheless, the **STM** study showed the complexity of this process without any Sb overpressure to reconstruct a growth-like surface, as a (3×3) reconstruction was observed similar to InSb thin film on GaAs in chapter 4. Lastly, the **STS** study performed on such surface supplanted the importance of a passivated surface to maximize the transport properties, as localized surface states were probed on the (3×3) reconstructed InSb surface, which act as carrier traps.

Looking forward, the numerous progresses made from this thesis provide a solid foundation regarding high quality InSb nanostructures on mismatched substrates with a gate-tuning capability. The structural improvements and the electron mobility observed at **RT** are sufficiently promising to pursue the optimization efforts and evidence the ballistic transport within these nanostructures. Achieving this milestone requires low-temperature transport measurements on **NWs** with atomically clean and well-ordered sidewalls.

A key step toward functional devices involves the fabrication of nanostructures with reliable metallic contacts. This necessitates addressing the challenge of the native oxide on InSb surfaces, which can significantly degrade contact transparency. A first route could be a sulfur passivation of the InSb surface, as this treatment proved to be efficient in both producing a chemical (preventing rapid oxidation in air) and electrical passivation (eliminating the surface induced states in the band gap). While wet chemical passivation through $(NH_4)_2S_x$ solution is the most common and effective way to passivate III-V surfaces,[262,263] a sulfurization in vapor phase through either H_2S or molecular sulfur evaporation can also be performed[264,265] prior to the dielectric and metal top gate deposition. The second possibility explored more recently, is the use of a CdTe shell on the InSb **NW**, which could not only act as a protective surface passivation layer, but also as a tunnel barrier between a superconductor and InSb.[125,266] In the context of the ANR Inspiring project, the CdTe passivation on InSb nanostructures grown at **IEMN** was initiated by CEA-LETI. Considering the effective passivation of the InSb surfaces, including subsequent dielectric deposition and usual top metal contacts (Ti/Au), transport measurements at cryogenic temperatures under variable magnetic field could pave the way to probe ballistic transport inside InSb nanostructures.

Beyond semiconductor gating, the integration of superconducting shells (Al, Sn or Nb with a respective critical temperature of 1.2, 3.7 and 9.3 K) epitaxially grown on InSb nanostructures represents the next technological breakthrough. As stated in chapter 1, these hybrid devices are of particular interest for the emergence of Majorana bound states and topological quantum computing. However, the realization of such epitaxies is nontrivial, as it requires to grow the superconductor at very low temperatures while exhibiting an abrupt interface with the semiconductor, which cannot be mitigated through ex-situ deposition. Indeed, (Ar) ion milling or oxide removal techniques are too agressive for the **NW** surface.[267] Yet, several pioneering studies have demonstrated recently in-situ epitaxy of superconductors on III-V **NWs**. However, they also highlighted a problem of vertical **NWs** bending due to differences in thermal expansion coefficients or strain in the crystal structure.[268] The interface quality between the III-V **NW** and the superconductor also revealed to be defective with an array of dislocations in some

cases.[269] Over the last years, the "shadow deposition" has enabled remarkable progresses in the fabrication of these hybrid systems. Using a combination of shadow walls and tilted metal beam fluxes,[270] the superconductor can be grown in-situ on the III-V **NWs** with a uniform thickness and abrupt interface, exhibiting quantum compatible properties after complete device fabrication, as reported by Pendharkar *et al.*[271]. Moreover, this recent technique being not only compatible with **VLS** grown vertical **NWs**, but also with in-plane **NWs** grown by **SAG**, could open the door to an universal platform for scalable semiconductor-superconductor **NWs** fabrication.[272] Despite the numerous remaining challenges, all of these different possibilities further account for the versatility of InSb in answering challenges dictated by the quantum computing quest.

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Appendix A

Mask layouts

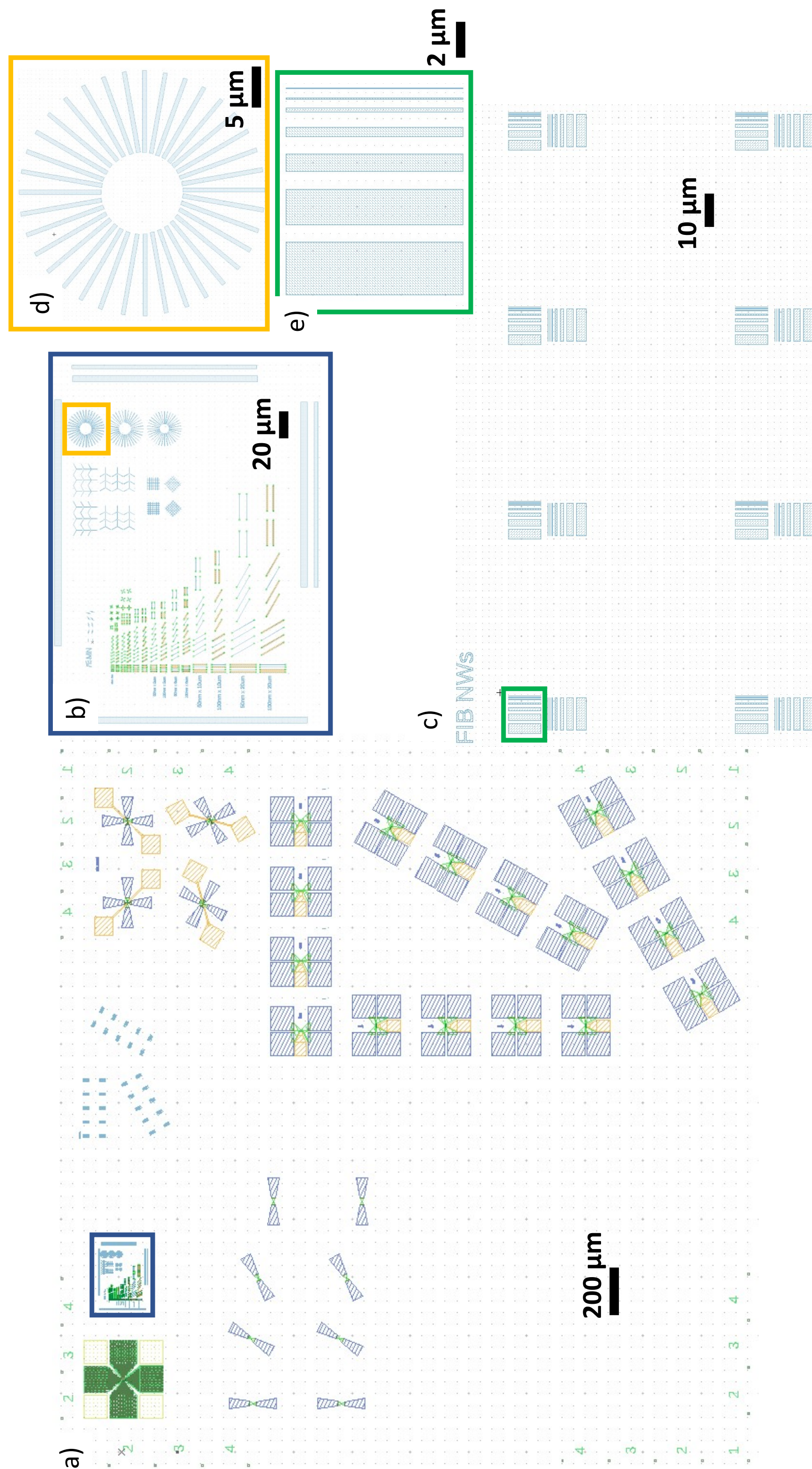

Figure A.1: Mask 1 used for the **SAG** of InSb on CdTe (111) substrates.

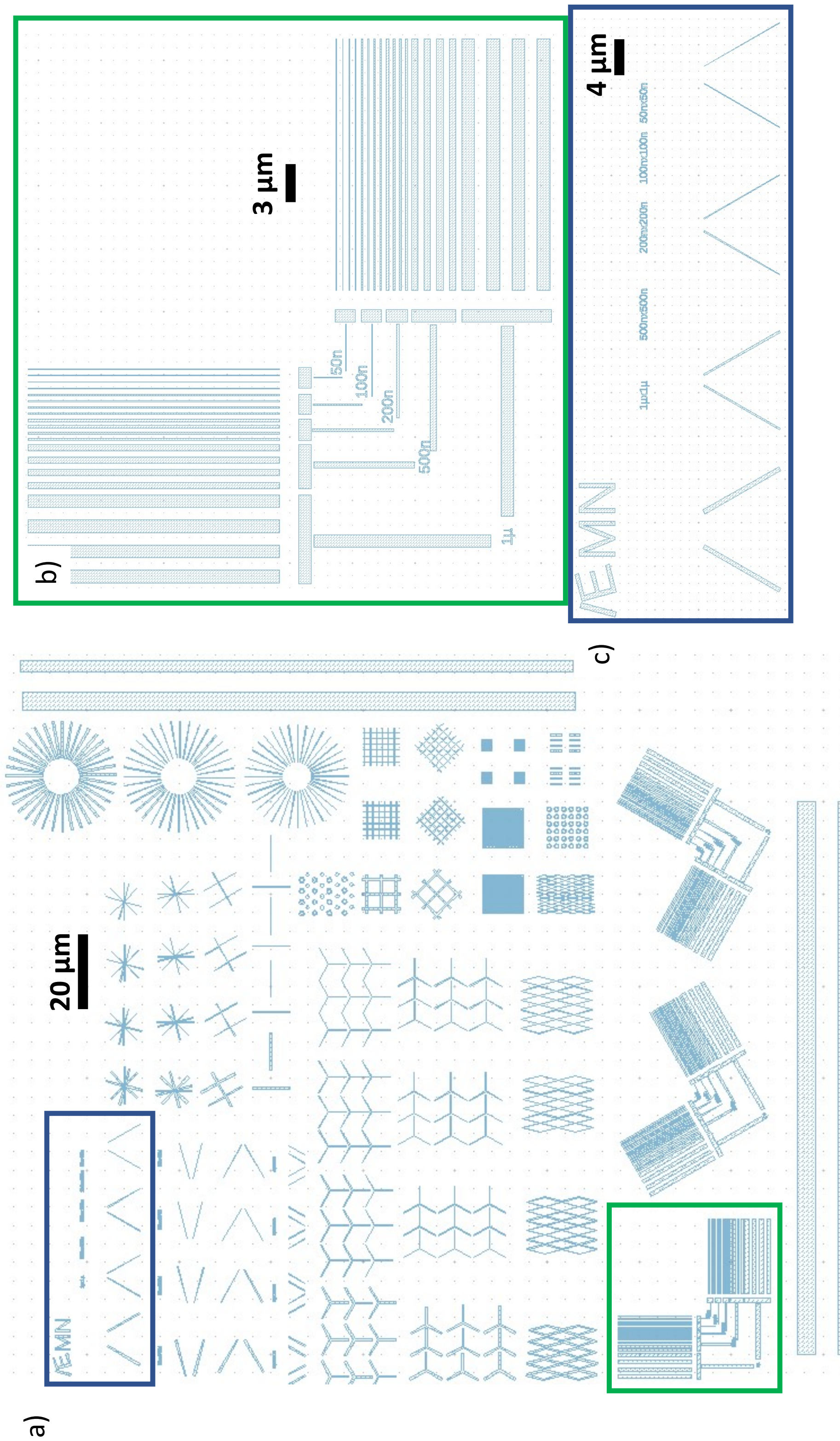

Figure A.2: Mask 2 gathering different nanostructures to assess the geometric shape, aperture width, crystallographic orientation impacts on the InSb morphology.

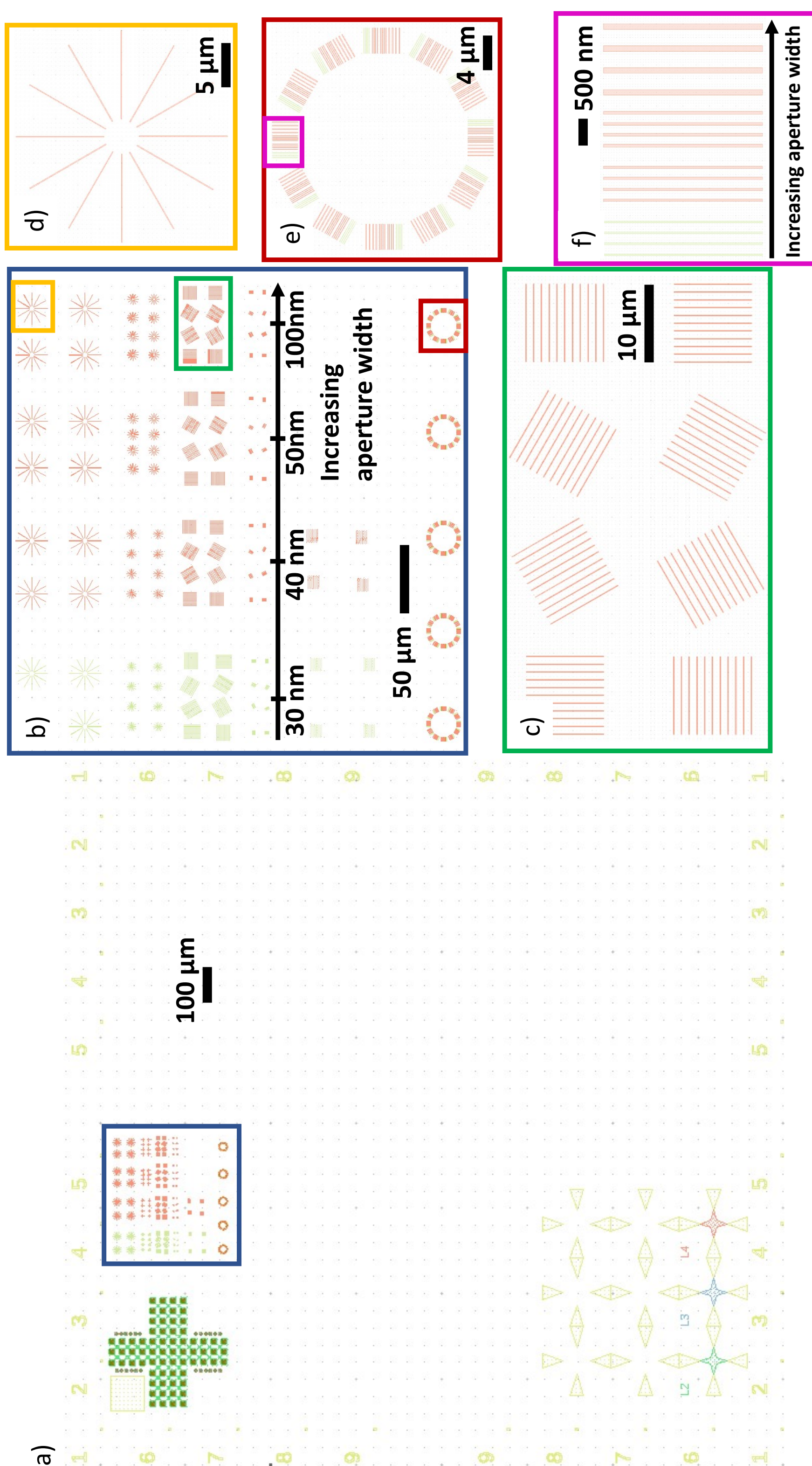

Figure A.3: Mask 3 for **4P-STM** transport measurements but also gathers various nanostructures to assess the crystallographic orientation impact on the InSb morphology.

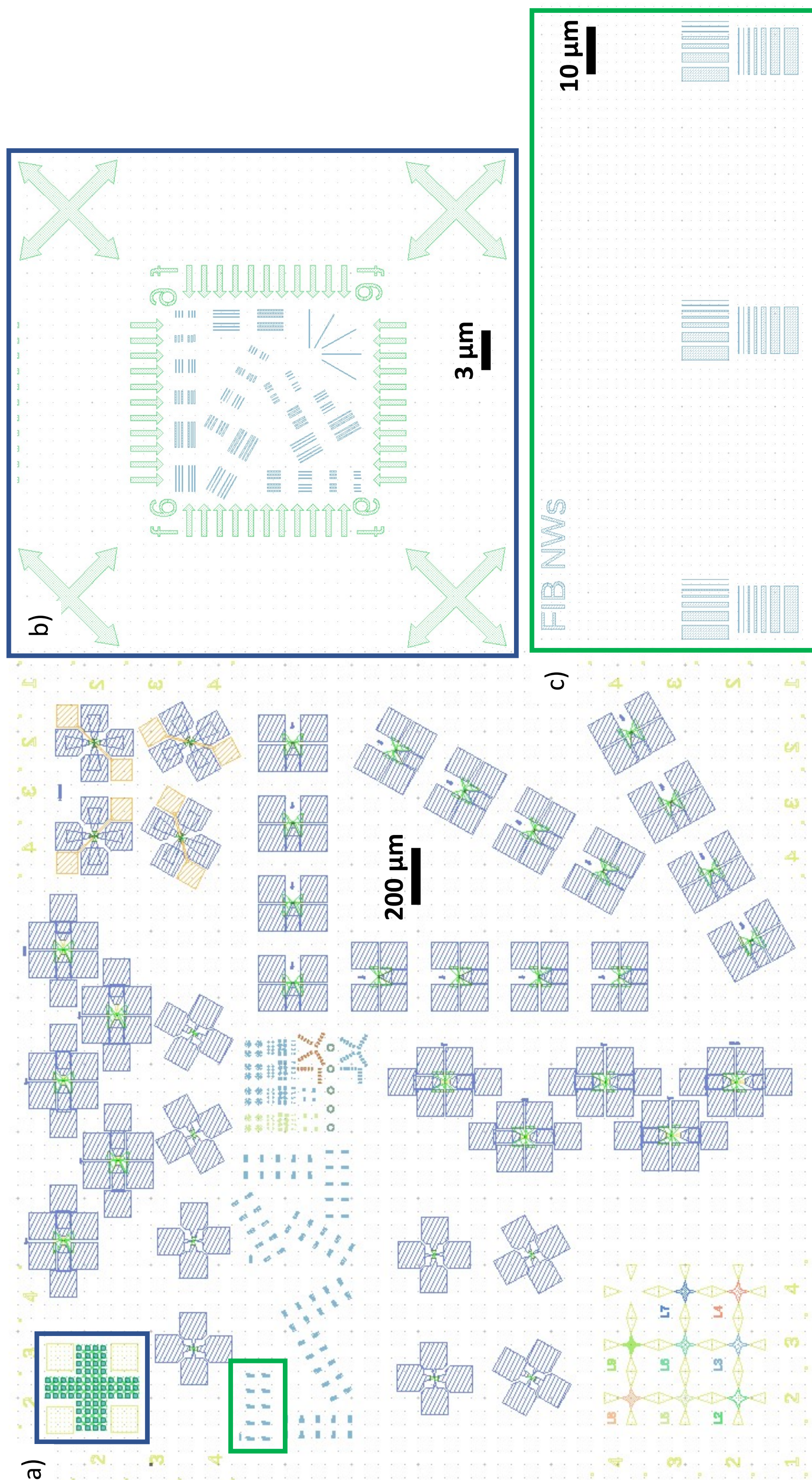

Figure A.4: Mask 4 gathering different types of devices that can be used for (cryogenic) transport measurements.

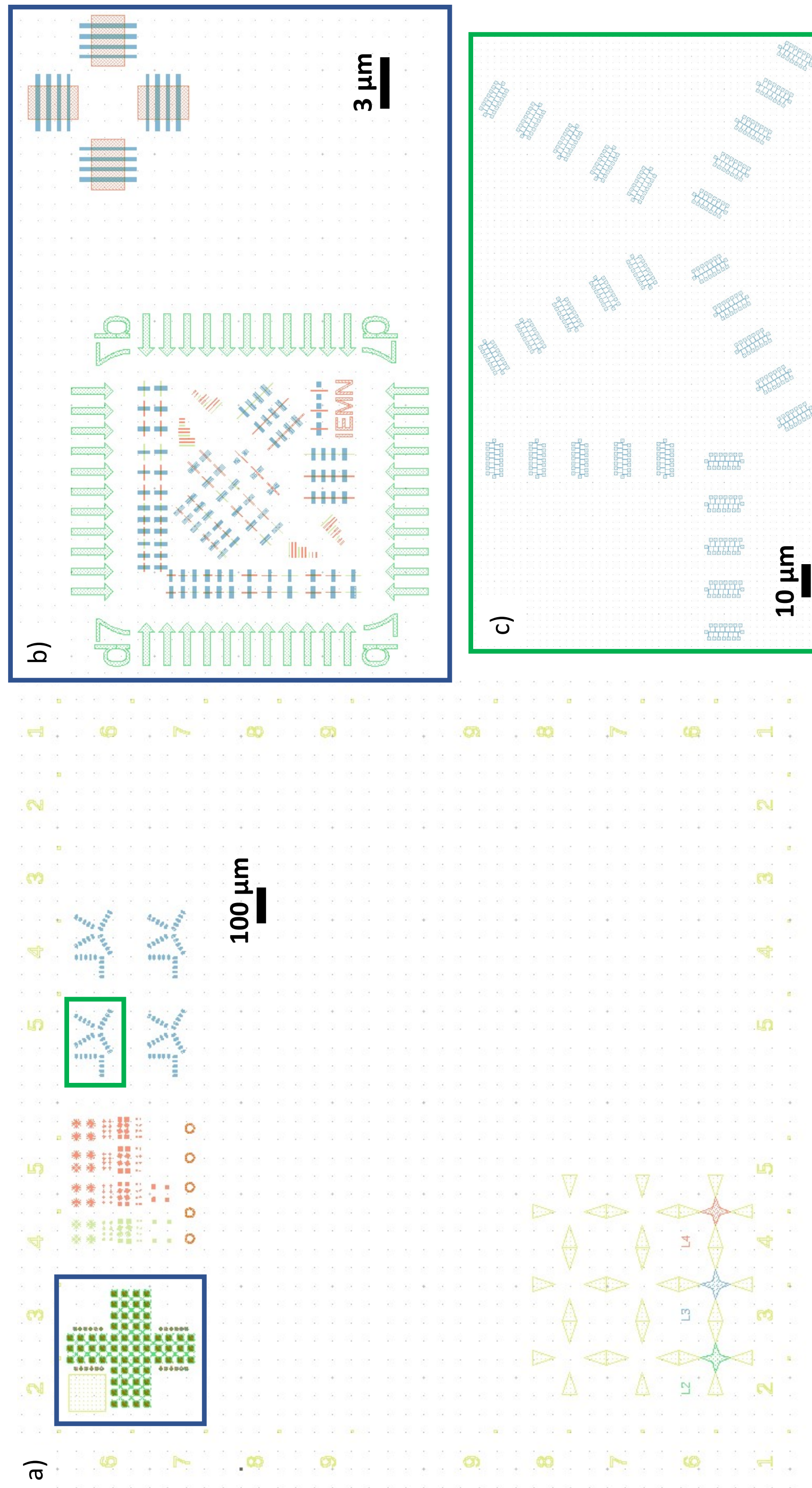

Figure A.5: Mask 5 used for the **SAG** of InSb on GaSb/CdTe (111) substrates.

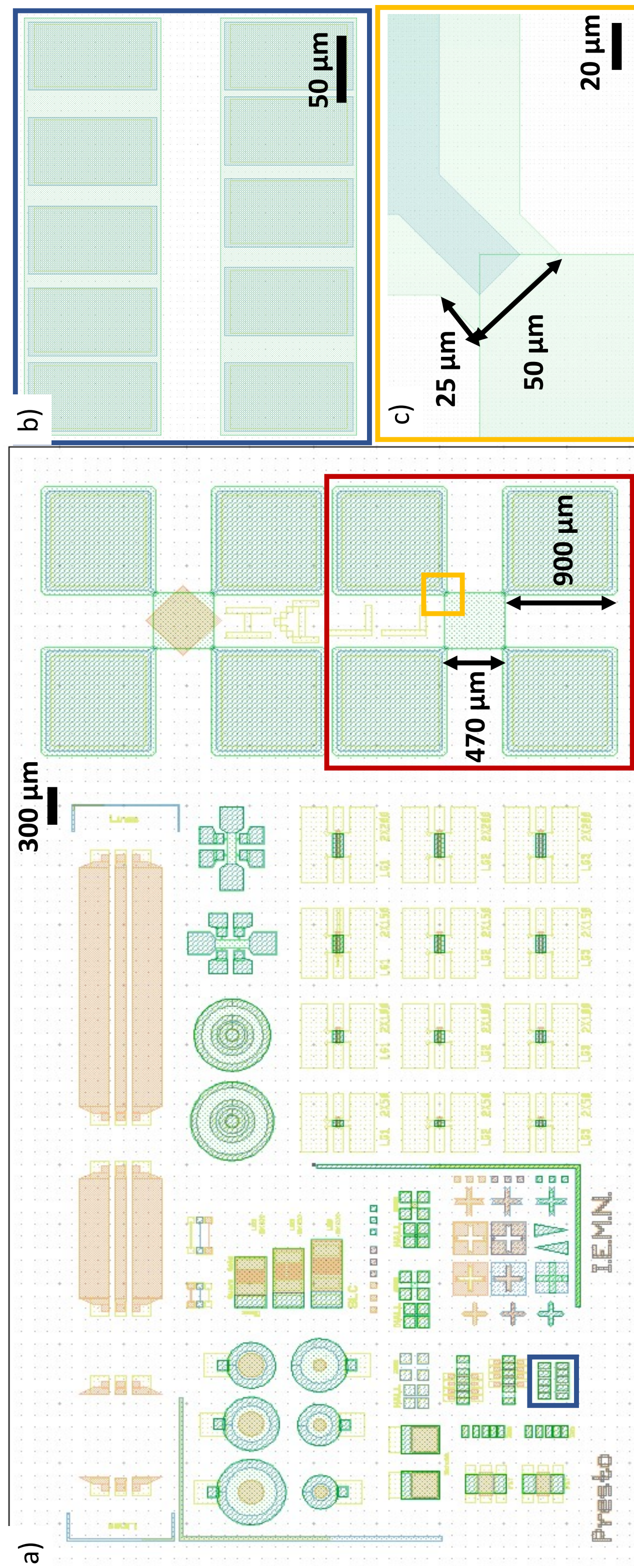

Figure A.6: Mask 6 used for Hall effect and TLM measurements.

Appendix B

XPS quantitative analysis

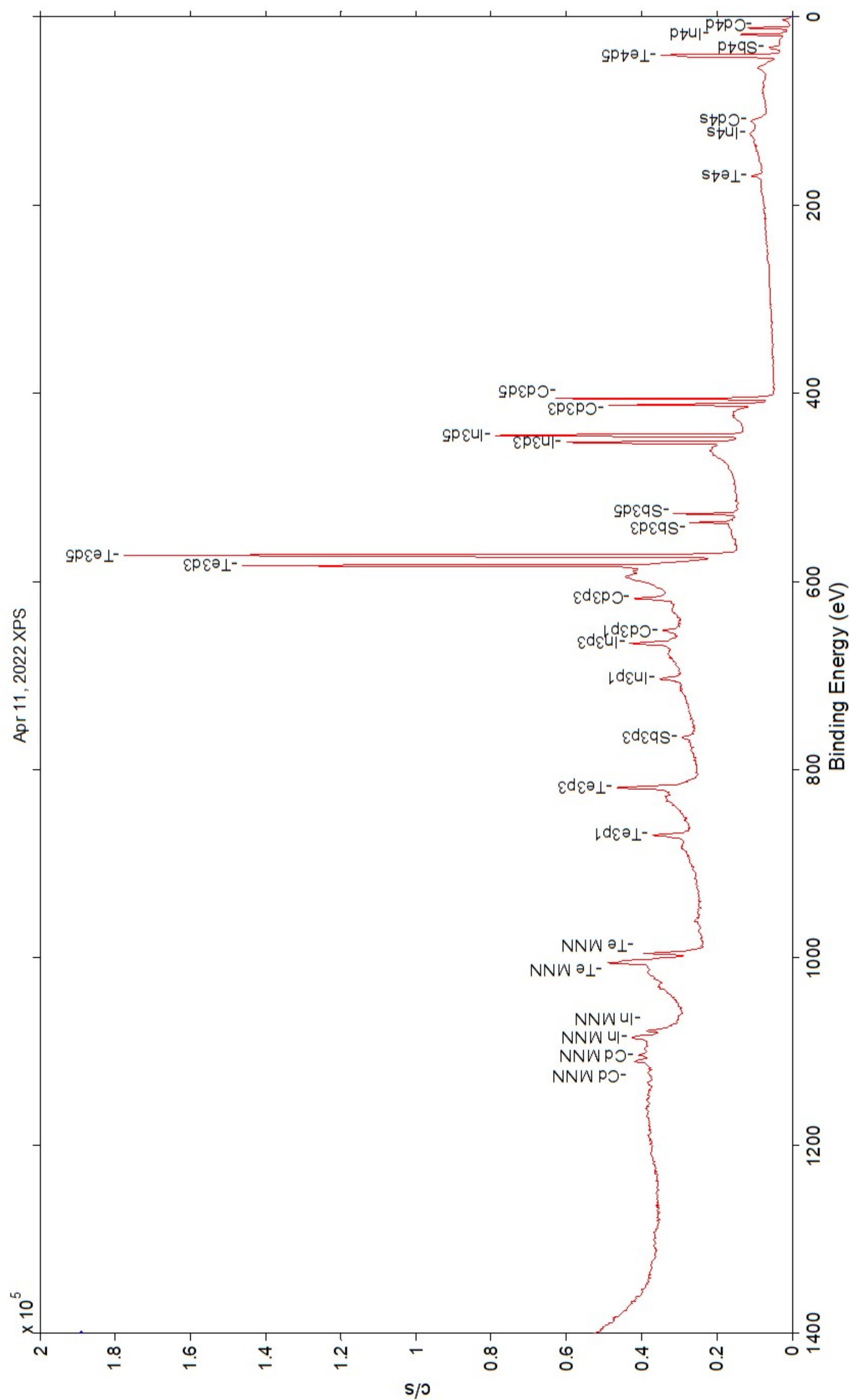

Figure B.1: **XPS** survey spectrum of sample **IC1**, 50 nm-thick InSb on CdTe (100) grown using a two step process (10 **MLs** of InSb at 320 °C followed by 50 nm at 370 °C).

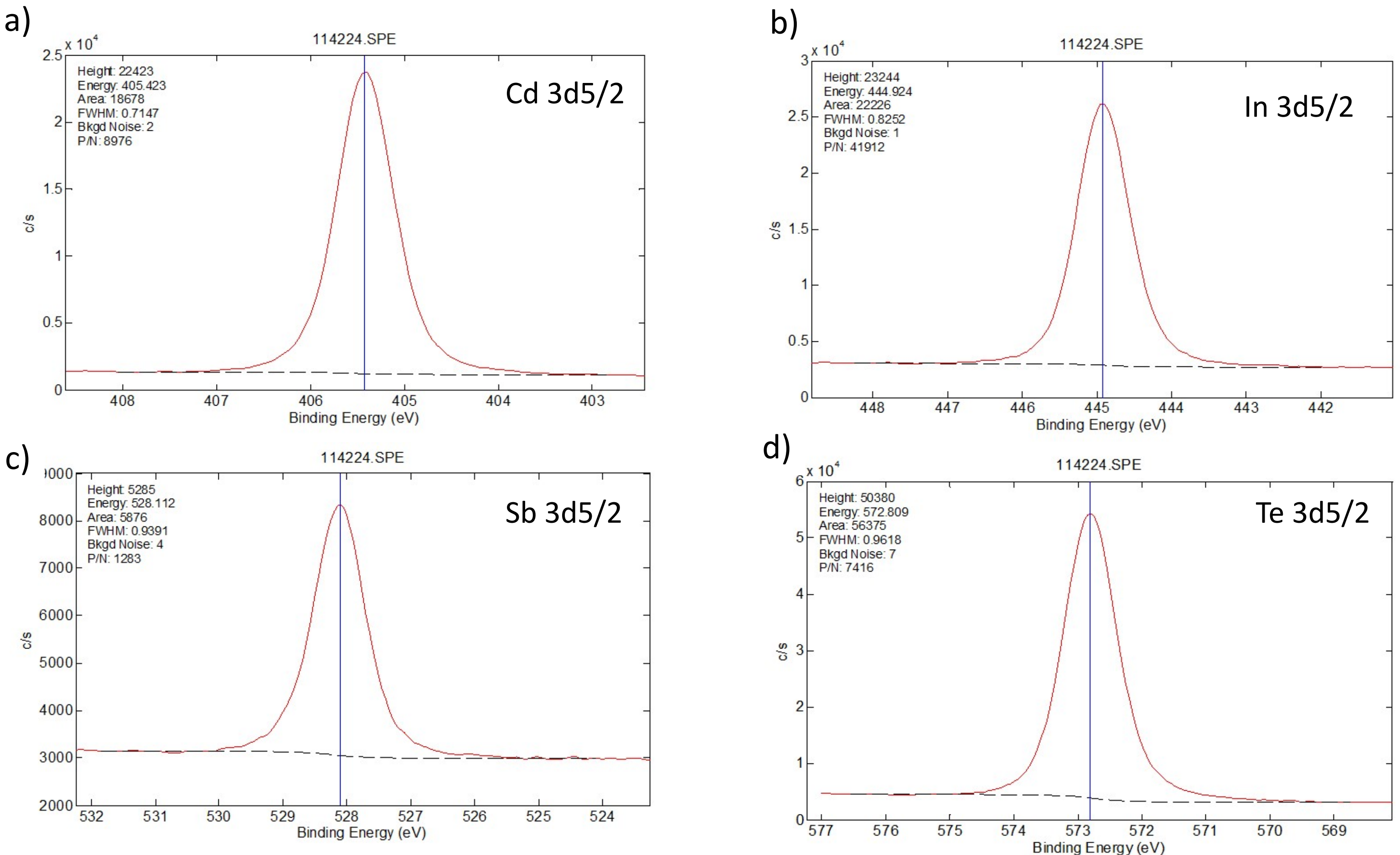

Figure B.2: **XPS** spectra of a) Cd $3d_{5/2}$, b) In $3d_{5/2}$, c) Sb $3d_{5/2}$, d) Te $3d_{5/2}$ core levels for sample **IC1**, 50 nm-thick InSb on CdTe (100) grown using a two step process (10 **ML**s of InSb at 320 °C followed by 50 nm at 370 °C) .

Appendix C

Additional STEM images for InSb NWs cross-sectional analysis

While sample **SIGG6** was obtained from the mask B process, which involves the use of a dielectric bilayer, a second lamella was also prepared from sample **SIGG2**, obtained with the mask A process, to assess the impact of the dielectric mask on the defect formation. Before preparing this lamella, the sample underwent a HF wet etch to fully remove the oxide mask, as a few residues were visible in between the **NWs** in the **SEM** image of Figure C.1a.

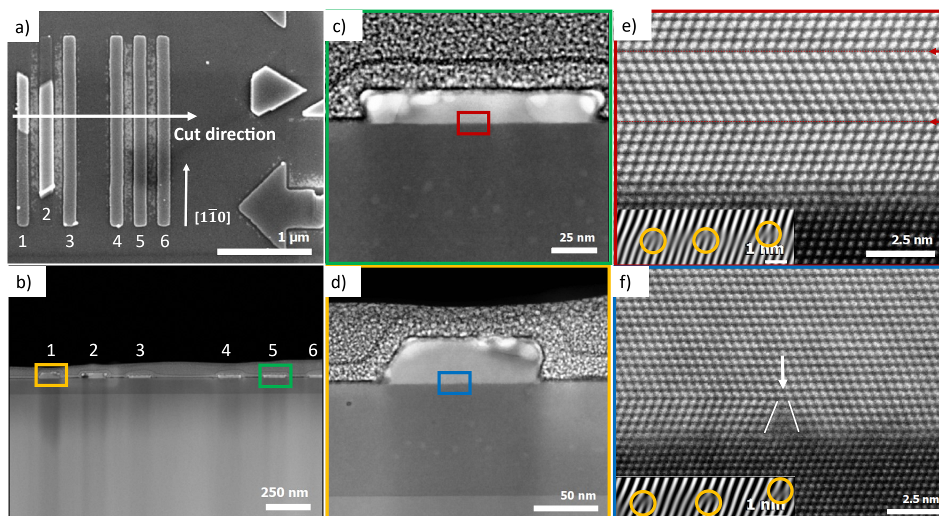

Figure C.1: a) **SEM** image of a [1$\bar{1}$0]-oriented 100 nm-wide **NW** array from sample **SIGG2**. b) Larger scale **STEM** image of the InSb **NWs**. The zone axis is [1$\bar{1}$0]. c) **TEM** image of a smooth **NW** from the green box in b). d) **STEM** image of a **NW** with a thicker grown region from the yellox box in b). e) Zoom at smaller scale from the red box in c). A twinned region separated by **SFs** is delimited by the red arrows. The inset shows a [$\bar{2}$00] filtered **FFT** and inverse **FFT** image of the formed **MD** network at the InSb/GaInP interface (yellow circles). f) Zoom at smaller scale from the blue box in d). No **SFs** along the thickness are observed but a complex twin between the white sticks is pointed out by the white arrow.[273] The inset shows a **MD** network (yellow circles).

Moreover, due to the **FIB** preparation step (that uses a carbon protective cap layer), the surface of the InSb **NWs** was further damaged as seen in Figures C.1c and d through the strong contrast variations near the surface of the **NW** and on its edges.

An array of six [$1\bar{1}0$]-oriented InSb **NWs** (2 µm-long and 100 nm-wide) were analyzed, which are all resolved in the cross-section view of Figure C.1b. Two types of InSb **NW** morphology are observed. The first type corresponds to **NWs** which fill the aperture and show the nominal thickness (Figure C.1c), whereas the second type concerns discontinuous **NWs**, which have a larger height than the nominal thickness (Figure C.1d). In the **SEM** image of Figure C.1a, they show a bright contrast.

In the high-resolution **STEM** image acquired in the central region of the first type of **NW** (Figure C.1e), the InSb layer presents a periodic **MD** network at the InSb/GaInP interface (inset showing a [$\bar{2}00$]-filtered **FFT** and inverse-**FFT** image) as well as two **SF**s separating a mirrored region. We can notice in this case than despite the twin region, the remaining part of the **NW** follows the same stacking orientation as the substrate.

Regarding the second type of **NW**, except in a short area near the interface where the **MD** can be clearly identified, the high-resolution **STEM** image of the thicker part at the most left of the **NW** indicates a 180° rotation of the InSb crystal at the InSb/GaInP interface (Figure C.1f). As pointed by the two white sticks and arrow, the region at the left is mirrored only after 5 to 6 monolayers while the right side is directly twinned at the InSb/GaInP interface. Except these interface defects, no other ones were found in the **NW** volume as shown in Figure C.2c.

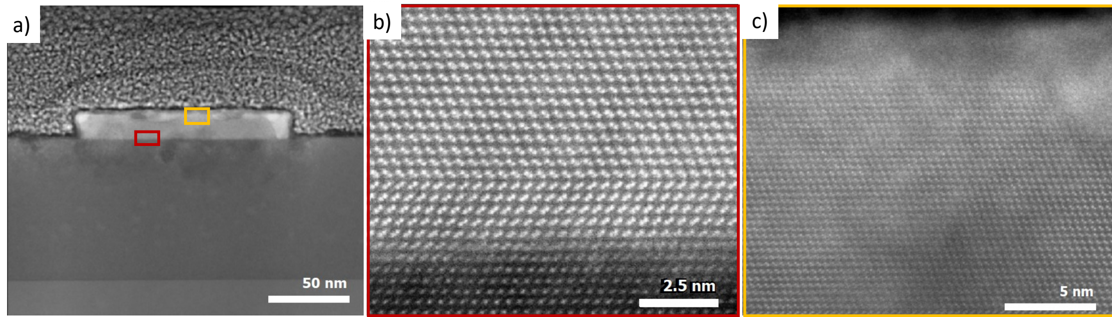

Figure C.2: a) **STEM** images of a) the **NW** "4" from the lamella of sample **SIGG2**, b) the interfacial region from the red box in a), c) the upper region of the **NW**. The zone axis is [$1\bar{1}0$].

All other investigated **NWs** on this sample follow the same trend, *i.e.* only a single twinned region along their volume with an interfacial **MD** network. Therefore, the zoo of defects and their occurrence are similar to the ones observed in sample **SIGG4** (Figures 5.26 and 5.27).

Appendix D

List of Communications and Publications

Communications

- Clément Barbot, Christophe Coinon, Xavier Wallart, Bruno Grandidier, Ludovic Desplanque — *Selective Area Growth of in-plane $In_{0.5}Ga_{0.5}P$ nanowires on GaAs $(111)_B$ substrate by molecular beam epitaxy* — 21st European Workshop on Molecular Beam Epitaxy, EuroMBE 2023, Apr 2023, Madrid, Spain hal-04475475v1
- Clément Barbot, Wijden Khelifi, Christophe Coinon, Pierre Capiod, Yves Deblock, ..., Ludovic Desplanque — *In-plane InAs and InSb nanowires grown by selective area MBE* — Journées Nationales Nanofils Semiconducteurs (J2N) 2024, C2N, Jun 2024, Palaiseau, France hal-04660092v1
- Clément Barbot, Christophe Coinon, Etienne Okada, Louis Thomas, Maxime Berthe, Bruno Grandidier, Ludovic Desplanque — *Modulation-Doped InSb Thin Film And Selective Area Grown In-Plane Nanowires on GaAs $(111)_B$ Substrates* — ICMBE2024, Sep 2024, Matsue, Japan hal-04936794v1 → **Oustanding Student Oral Presentation Award (certificate)**
- Clément Barbot, Christophe Coinon, Maxime Berthe, Yves Deblock, Qianqian Lan, ..., Ludovic Desplanque — *Bottom gated in-plane selective area grown InSb NWs on GaAs$(111)_B$* — EuroMBE 2025 Conference, CRHEA, Mar 2025, Auron, France hal-05019799v1

Publications

- Barbot C., Rondeau-Body C., Coinon C., Deblock Y., Tilmant P., Vaurette F., ..., Desplanque L., Grandidier B. (2024). InGaAs quantum dot chains grown by twofold selective area molecular beam epitaxy. Nanotechnology, 35(39), 395302.
- Khelifi W., Capiod P., Barbot C., Coinon C., Deblock Y., Santos C. N., ..., Grandidier B., Desplanque L. (2025). Selective area molecular beam epitaxy of InSb on InP (111) B: from thin films to quantum nanostructures. Nanotechnology, 36(12), 125301.
- Chaize N., Baudry X., Jouneau P. H., Gautier E., Rouvière J. L., Deblock Y., Barbot C., ..., Ballet P. (2024). Selective area epitaxy of in-plane HgTe nanostructures on CdTe (001) substrate. Nanotechnology, 35(50), 505602.

Acronyms

Numbers | A | C | D | E | F | G | H | I | L | M | N | P | Q | R | S | T | U | V | W | X | Z

Numbers

2D Two-Dimmensional. 61
2DEG Two-Dimensional Electron Gas. 10
2PP Two Point Probe. 57
4PP Four Point Probe. 44
4P-STM Four Probe Scanning Tunneling Microscopy. 3

A

AFM Atomic Force Microscopy. 2
ALD Atomic Layer Deposition. 37

C

CMOS Complementary Metal Oxide Semiconductor. 1

D

DIBL Drain Induced Barrier Lowering. 148
DOS Density of States. 6

E

EDX Energy-dispersive X-ray Spectroscopy. 98

F

FCC Face-Centered Cubic. 14
FET Field-Effect-Transistor. 5
FFT Fast-Fourrier Transform. 91
FIB Focused Ion Beam. 32
FM Frank-van der Merwe. 17

G

GAAFET Gate All Around Field-Effect-Transistor. 1

H

H_{AT} Atomic Hydrogen. 2
HAADF High-Angle Annular Dark-Field. 61
HEMT High Electron Mobility Transistor. 59
HOPC Hyperfrequency Optical and Photonics Characterization. 60
HTI High Temperature Gas Injector. 39
HVPE Hybrid Vapor Phase Epitaxy. 17

I

IEMN Institute of Electronic, Microelectronic and Nanotechnologies. 1
IPA Isopropanol. 44

L

LDOS Local Density of States. 50
LED Light Emitting Diode. 17
LEED Low Energy Electron Diffraction. 86
LT Low Temperature. 54
LT-STM Low Temperature Scanning Tunneling Microscopy. 34

M

MBE Molecular Beam Epitaxy. 2
MD Misfit Dislocation. 100
MEE Migration Enhanced Epitaxy. 104
MIBK Methyl Isobutyl Ketone. 44
ML Monolayer. 17
MOCVD Metal-Organic Chemical Vapor Deposition. 1, 27
MOSFET Metal-Oxide-Semiconductor Field-Effect-Transistor. 2
MZM Majorana Zero Mode. 7

N

NDR Negative Differential resistance. 165
NW nanowire. 123
NWs nanowires. 1

P

PCMP-PCP multi-physics characterization platform. 53
PECVD Plasma-enhanced Chemical Vapor Deposition. 43

Q

QDs Quantum Dots. 6
QPC quantum point contact. 12
QW Quantum Well. 5

R

R_{4P} Four Probe resistance. 55
RHEED Reflective High Energy Electron Diffraction. 40

RIE Reactive Ion Etching. 44
RMS Root-Mean Square. 46
RT Room Temperature. 11

S

SAE Selective Area Epitaxy. 34
SAG Selective Area Growth. 1
SAMBE Selective Area Molecular Beam Epitaxy. 2
sccm standard cubic centimetres per minute. 39
SEM Scanning Electronic Microscope. 20
SF Stacking Fault. 16
SIBB Surface Induced Band Bending. 165
SK Stranski-Krastanov. 17
SOC Spin Orbit Coupling. 7
SOI Spin Orbit Interaction. 8
STEM Scanning Transmission Electron Microscopy. 2
STM Scanning Tunneling Microscopy. 2
STS Scanning Tunnelling Spectroscopy. 3

T

T_G Growth temperature. 19
TASE Template Assisted Selective Epitaxy. 28
TEM Transmission Electronic Microscopy. 18
TIBB Tip Induced Band Bending. 163
TLM Transfer Length Method. 3
TRS Time Reversal Symmetry. 9

U

UHV Ultra-high vacuum. 35

V

V_G Growth rate. 19
V_{GS} Gate-to-source Voltage. 57
VLS Vapor-Liquid-Solid. 1
VW Volmer-Weber. 17

W

WZ Wurzite. 18

X

XPS X-Ray Photoelectron Spectroscopy. 37
XRD X-Ray Diffraction. 2

Z

ZB Zinc-Blende. 14
ZBA Zero Bias Anomaly. 9
ZBCP Zero-Bias Conductance Peak. 9

Epitaxial growth and near-field characterization of InSb nanostructures for advanced electron devices

Abstract

At the dawn of the quantum era, which promises radically new ways of processing information, III-V semiconductors — and InSb in particular — stand out as one of the most promising material for this transition. With high electron mobility, strong spin-orbit interaction, and small effective mass, InSb exhibits ideal properties for quantum applications such as Majorana-based devices, while also offering opportunities in high-performance nanoelectronics beyond quantum computing. However, the deployment to functional devices has been hampered by the strong lattice-mismatch of InSb to conventional III-V substrates, making the growth of defect-free nanostructures challenging. This thesis investigates the **Selective Area Growth (SAG)** of InSb nanostructures on both lattice-matched and highly mismatched substrates using **Molecular Beam Epitaxy (MBE)**. To enable the carrier density modulation required for quantum devices, InSb was also integrated within gated heterostructures incorporating semiconducting barriers.

This thesis work dealt with the InSb growth on lattice-matched CdTe substrates at the beginning, but technological limitations constrained the quality and scalability of the InSb nanostructures. The study then shifted to GaAs $(111)_B$ substrates, where growth optimization yielded high crystal quality thin films and planar nanostructures with low defect density, as confirmed by cross-sectional **Scanning Transmission Electron Microscopy (STEM)** and **Scanning Tunneling Microscopy (STM)**.
Following the optimized growth on GaAs $(111)_B$, high quality InSb thin-films and in-plane **nanowires (NWs)** were produced on low roughness GaInP buffer layers grown on GaAs under carefully optimized conditions. Through a structural and a morphological study, we then discussed the minor differences observed with the growth of InSb nanostructures on GaAs substrates. The final part of the thesis focused on electrical transport studies of the InSb/GaInP/GaAs:n+ heterostructure combining Hall measurements, **Transfer Length Method (TLM)**, and **Four-Probe Scanning Tunneling Microscopy (4P-STM)**. An effective charge density modulation inside the InSb nanostructures as well as a record-high electron mobility for InSb thin films grown on III-V mismatched substrate were demonstrated. A last comprehensive **Scanning Tunneling Spectroscopy (STS)** study revealed that precise control of surface integrity is essential to fully exploit the potential of these nanostructures.

Altogether, this work establishes a scalable route to high-quality InSb nanostructures, advancing both quantum device development and high-performance III–V nanoelectronics.

Keywords: InSb, III-V Heterostructures, Nanowires, Quantum transport, Selective Area Growth, Molecular Beam Epitaxy, Multiple-tip Scanning Tunneling Microscopy, Transport measurements

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CROISSANCE ÉPITAXIALE ET CARACTÉRISATION CHAMP-PROCHE DE NANOSTRUCTURES D'INSB POUR COMPOSANTS ÉLECTRONIQUES AVANCÉS

Résumé

À l'aube de l'ère quantique, qui promet des modes de traitement de l'information radicalement nouveaux, les semi-conducteurs III-V — et en particulier l'antimoniure d'indium (InSb) — apparaissent comme des materiaux prometteurs pour contribuer à cette transition. Grâce à sa mobilité électronique élevée, son fort couplage spin-orbite et sa faible masse effective, l'InSb possède les propriétés idéales pour des applications quantiques telles que les dispositifs à base de fermions de Majorana, tout en ouvrant la voie à des applications innovantes en nanoélectronique haute performance au-delà du calcul quantique. Cependant, la mise en oeuvre de tels dispositifs fonctionnels reste freinée par le fort désaccord de maille entre l'InSb et les substrats III-V conventionnels, qui rend difficile une croissance de nanostructures exemptes de défauts. Cette thèse explore la croissance sélective de nanostructures d'InSb sur des substrats à maille accordée et fortement désaccordée, en utilisant l'épitaxie par jets moléculaires. Afin de permettre la modulation de densité de porteurs nécessaire aux dispositifs quantiques, l'InSb a également été intégré dans des hétérostructures comportant des barrières de potentiel semi-conductrices.

L'étude a porté dans un premier temps sur la croissance de l'InSb sur des substrats de tellure de cadmium (CdTe) accordés en maille, mais des limitations technologiques ont limité la qualité et la production de nanostructures d'InSb. La suite de l'étude s'est alors orientée vers l'utilisation de substrats d'arseniure de gallium (GaAs) orientés selon la direction $(111)_B$, où l'optimisation des paramètres de croissance a permis d'obtenir des couches minces et des nanostructures planaires de haute qualité cristalline avec une faible densité de défauts, confirmées par des analyses en microscopie électronique en transmission ainsi qu'en microscopie à effet tunnel.
À la suite de l'optimisation de la croissance d'InSb sur GaAs $(111)_B$, des couches minces et des nanofils d'InSb de haute qualité ont été réalisés sur des couches tampons de phosphure de gallium-indium à faible rugosité, elle-même épitaxiée sur substrat GaAs dans des conditions optimisées. Une étude structurale et morphologique a permis de discuter les différences mineures observées par rapport à la croissance des nanostructures d'InSb directement sur GaAs. La dernière partie de la thèse a été consacrée à l'étude des propriétés de transport électrique de l'hétérostructure InSb/GaInP/GaAs dopé n, en combinant des mesures de Hall, la méthode des longueurs de transfert et la microscopie à effet tunnel à quatre pointes. Une modulation efficace de la densité de porteurs à l'intérieur des nanostructures d'InSb, ainsi qu'une mobilité électronique record pour des couches minces d'InSb épitaxiées directement sur substrats III-V désaccordés, ont été démontrées. Enfin, une étude par spectroscopie à effet tunnel a révélé que le contrôle précis de l'état de surface est essentiel pour exploiter pleinement le potentiel de ces nanostructures.

Dans l'ensemble, ce travail établit une base fondamentale vers la production de nanostructures d'InSb de haute qualité, utile à la fois pour le développement de dispositifs quantiques et la nanoéléctronique III-V haute performance.

Mots clés : InSb, Hétérostructures III-V, Nanofils, Transport quantique, Croissance Sélective, Epitaxie par Jets Moléculaires, Microscopie à effet tunnel à pointes multiples, Transport électronique