Université de Lille

Thèse de doctorat

Optimisation of manufacturing processes for the development of power transistors using GaN technology

Optimisation des procédés de fabrication pour le développement de transistors de puissance en GaN

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Abstract

This thesis investigates the design and optimization of gallium nitride (GaN) power transistors, focusing on lateral high-electron-mobility transistors (HEMTs) and vertical trench MOSFETs (V-T-MOSFETs). The objective is to achieve robust and reliable operation in the 600–1200 V class while maintaining high efficiency and fast switching.

As demand for electrical energy and power-conversion density continues to grow, conventional silicon devices are reaching their physical and performance limits. Wide bandgap semiconductors provide a path forward. Among them, GaN combines a high critical electric field and high electron mobility with device architectures that enable compact, high-frequency, and energy-efficient converters.

Chapter 1 establishes the context by retracing the evolution of power transistors from BJTs and MOSFETs to IGBTs and wide bandgap devices, and by benchmarking the intrinsic properties of Si, SiC, and GaN. This analysis highlights GaN's advantages in breakdown field, carrier mobility, and frequency capability, and reviews the state of the art in both lateral and vertical device families.

Chapter 2 focuses on the optimization of lateral GaN HEMTs. Using a combination of TCAD simulations and prototype fabrication, the influence of key design parameters such as buffer carbon concentration and back-barrier composition is investigated. Particular emphasis is placed on GaN HEMTs on sapphire substrates, which are optimized in view of an innovative vertical integration pathway based on the exfoliation technique that is studied by simulation. Experimental characterization validates the simulated trends and provides design guidelines to mitigate trapping and improve dynamic performance.

Chapter 3 addresses the development of vertical GaN architectures, presenting the design, fabrication, and characterization of GaN V-T-MOSFETs on silicon. Edge-termination techniques including fluorine implantation and p-GaN regrowth are evaluated through simulation. A complete fabrication flow for a vertical GaN-on-Si transistor is developed, and the resulting devices are electrically benchmarked to highlight both their potential and their current limitations.

Chapter 4 explores future optimization strategies for vertical GaN devices, including low-damage trench etching, corner rounding, and gate-dielectric engineering to suppress electric-field crowding and

interface trapping. Methods to improve device ruggedness, such as p-shielded gates and slanted p-body designs, are also discussed. These approaches point toward the requirements for reliable, high-voltage GaN transistors in automotive, renewable energy, and grid applications.

Keywords: Power devices; Gallium Nitride (GaN); HEMT; Vertical trench MOSFET (V-T-MOSFET); Process optimization; Back barrier; Edge termination.

Résumé

Cette thèse porte sur la conception et l'optimisation de transistors de puissance en nitrure de gallium (GaN), en se concentrant sur les transistors latéraux à haute mobilité électronique (HEMT) et les MOSFETs verticaux à tranchée (V-T-MOSFETs). L'objectif est d'obtenir un fonctionnement robuste et fiable dans la gamme de tension 600–1200 V, tout en conservant un rendement élevé et une commutation rapide.

Alors que la demande en énergie électrique et en densité de conversion de puissance ne cesse d'augmenter, les dispositifs conventionnels en silicium atteignent leurs limites physiques et de performance. Les semi-conducteurs à large bande interdite offrent une voie prometteuse. Parmi eux, le GaN combine un champ électrique critique élevé et une forte mobilité électronique avec des architectures de dispositifs permettant des convertisseurs compacts, à haute fréquence et à haut rendement énergétique.

Le chapitre 1 établit le contexte en retraçant l'évolution des transistors de puissance, des BJTs et MOSFETs aux IGBTs et aux dispositifs à large bande interdite, et en comparant les propriétés intrinsèques du Si, du SiC et du GaN. Cette analyse met en évidence les avantages du GaN en termes de champ de claquage, de mobilité des porteurs et de capacité en fréquence, et passe en revue l'état de l'art des dispositifs latéraux et verticaux.

Le chapitre 2 est consacré à l'optimisation des HEMTs GaN latéraux. À l'aide d'une combinaison de simulations TCAD et de fabrication de prototypes, l'influence de paramètres clés de conception tels que la concentration en carbone du buffer et la composition de la barrière arrière (back-barrier) est étudiée. Un accent particulier est mis sur les HEMTs GaN sur substrats saphir, optimisés en vue d'une voie innovante d'intégration verticale basée sur une technique d'exfoliation étudiée par simulation. La caractérisation expérimentale valide les tendances simulées et fournit des règles de conception visant à limiter les effets de piégeage et à améliorer les performances dynamiques.

Le chapitre 3 traite du développement d'architectures GaN verticales, en présentant la conception, la fabrication et la caractérisation de V-T-MOSFETs GaN sur silicium. Des techniques de terminai-

son de bord, incluant l'implantation de fluor et la repousse de p-GaN, sont évaluées par simulation. Un procédé complet de fabrication d'un transistor vertical GaN-sur-Si est développé, et les dispositifs obtenus sont caractérisés électriquement afin de mettre en évidence à la fois leur potentiel et leurs limitations actuelles.

Le chapitre 4 explore des stratégies d'optimisation futures pour les dispositifs GaN verticaux, notamment la gravure de tranchées à faible endommagement, l'arrondi des angles et l'ingénierie du diélectrique de grille afin de réduire la concentration du champ électrique et le piégeage aux interfaces. Des méthodes visant à améliorer la robustesse des dispositifs, telles que les grilles protégées par p-GaN et les conceptions de corps p inclinés, sont également discutées. Ces approches mettent en lumière les exigences nécessaires à la réalisation de transistors GaN haute tension fiables pour les applications automobiles, les énergies renouvelables et les réseaux électriques.

Mots-clés : Dispositifs de puissance ; Nitrure de gallium (GaN) ; HEMT ; MOSFET vertical à tranchée (V-T-MOSFET) ; Optimisation des procédés ; Barrière arrière ; Terminaison de bord.

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General Introduction

The global demand for electricity has been rising steadily over the past decades (Fig. 1, from [1]), driven by rapid industrialization, urbanization, and the growing adoption of digital technologies. According to the International Energy Agency (IEA), worldwide electricity consumption is projected to increase by approximately 50% by 2050, with developing countries contributing the majority of this growth [1]. This escalating demand places immense pressure on the power generation, transmission, and distribution infrastructure, highlighting the critical importance of using electrical energy efficiently. Energy efficiency is not only an economic concern but also an environmental one, as improving efficiency reduces the carbon footprint associated with electricity production, particularly when fossil fuels still dominate the energy mix.

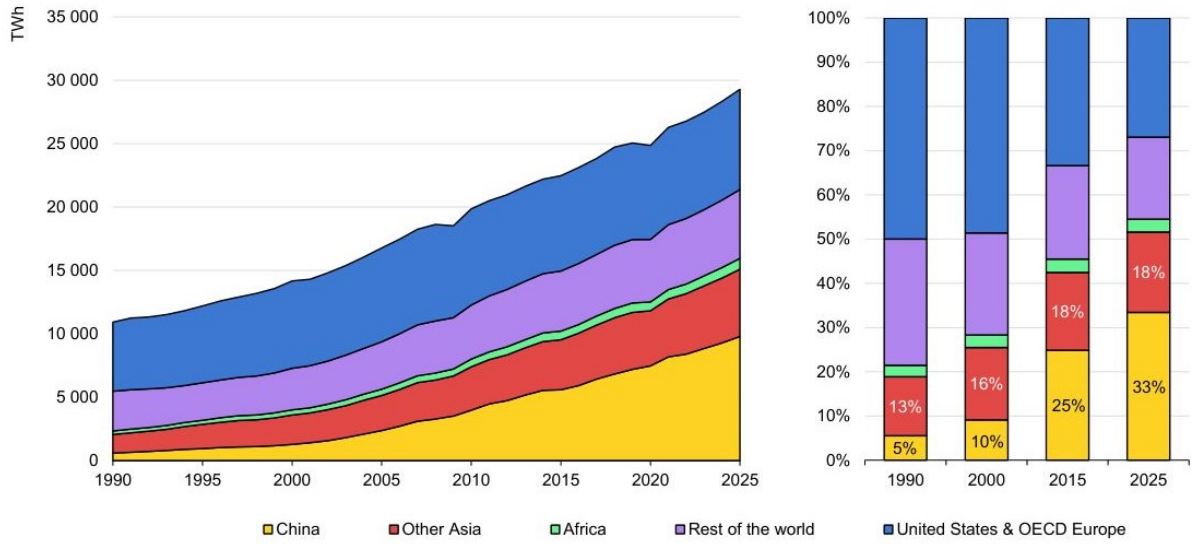


Figure 1: Evolution of the global electricity demand by region (left) and regional shares (right) from 1990 to 2025

Power electronic converters play a central role in modern electrical systems by controlling, conditioning, and regulating the flow of electrical energy. Their primary functions include converting alternating current (AC) to direct current (DC), DC to AC, or transforming voltage and frequency levels to match

specific application requirements. AC-DC converters, commonly known as rectifiers, are essential in applications such as battery charging, DC-powered electronics, and renewable energy systems like solar photovoltaic (PV) installations. DC-AC converters, or inverters, enable the integration of DC energy sources, such as batteries or PV panels, into the AC power grid and are critical for electric vehicles, uninterruptible power supplies (UPS), and distributed generation [2]. Additionally, DC-DC converters are widely used to adjust voltage levels for electronics, power supplies, and motor drives, while AC-AC converters facilitate frequency conversion for variable-speed motors and grid interconnection applications.

Despite their indispensability, power converters are a significant source of energy loss in electrical systems (see equation 1). Losses arise from conduction through semiconductors, switching transitions, leakage currents, and parasitic effects in passive components such as inductors and capacitors. Among these contributors, semiconductor transistors are the most influential, as their intrinsic properties directly affect conduction and switching losses. Improving the efficiency of these devices is therefore critical: even a small improvement of a few percentage points in converter efficiency can yield substantial reductions in global electricity consumption, resulting in significant cost savings and environmental benefits. In data centers, for instance, power conversion losses can account for 10–20% of total energy use, highlighting the need for high-performance semiconductor solutions.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} \tag{1}$$

- η is the conversion efficiency,
- P_{in},P_{out} and P_{loss} are the input, output, and loss power, respectively.

Equation 1: Equation for power conversion efficiency

Historically, silicon-based devices such as MOSFETs and IGBTs have been employed for power conversion, owing to their mature fabrication technology, mechanical robustness, and relatively low cost [3]. Silicon MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are widely used in low-voltage applications, while IGBTs (Insulated Gate Bipolar Transistors) dominate medium- and high-voltage systems due to their ability to handle high currents and voltages. However, silicon devices are approaching fundamental physical limits that restrict their performance. Conduction losses increase with voltage and current, and switching losses rise sharply at higher frequencies, limiting the potential for compact, high-efficiency designs. Additionally, the relatively low electron mobility and critical electric field of silicon restrict the maximum achievable switching speed and breakdown voltage. These limitations are particularly problematic in modern applications that demand high-frequency operation and compact, lightweight converters, such as electric vehicles, aerospace systems, and renewable energy inverters.

To overcome the inherent limitations of silicon, research has increasingly focused on wide-bandgap (WBG) materials, which exhibit superior electrical properties. Two WBG materials have emerged as leading candidates for next-generation power transistors: silicon carbide (SiC) and gallium nitride (GaN). SiC MOSFETs are characterized by high breakdown voltage, low on-resistance, and the ability to operate at elevated temperatures, making them particularly suitable for high-voltage, high-power applications such as grid-tied converters, industrial motor drives, and traction inverters. Nevertheless, SiC devices remain relatively expensive due to the high cost of substrates, complex epitaxial growth, and lower production yields compared to silicon. This high cost limits the widespread adoption of SiC in applications where cost sensitivity is critical, such as consumer electronics or low- to medium-voltage converters.

Gallium nitride, in contrast, offers remarkable advantages for power conversion, particularly for applications below $650\,\mathrm{V}$. GaN-based high-electron-mobility transistors (HEMTs) exhibit extremely high electron mobility, low gate and output capacitances, and minimal conduction losses. These properties enable very high switching speeds, allowing power converters to operate at frequencies several times higher than conventional silicon MOSFET-based systems, thereby reducing the size and weight of passive components such as inductors and capacitors. GaN-on-silicon (GaN-on-Si) HEMTs combine the superior electrical performance of GaN with the cost advantages of silicon substrates, enabling larger-scale production at a lower cost than SiC.

Research into GaN HEMTs continues to focus on extending the voltage range of these devices, which is currently limited compared to SiC MOSFETs, without compromising switching speed or efficiency. Success in these areas could broaden the applicability of GaN HEMTs to higher-voltage systems, further challenging the dominance of SiC devices.

Despite the promise of GaN HEMTs, alternative transistor architectures remain under exploration for high-voltage power conversion. One such approach is vertical trench MOSFETs, typically implemented on silicon. In this configuration, the current flows vertically through the device, allowing higher breakdown voltages without excessive increases in on-resistance. While vertical trench MOSFETs are not as mature as GaN HEMTs or conventional Si devices, they represent a potential pathway toward efficient, high-voltage power conversion using established silicon technology. Their development underscores the ongoing effort to improve device performance through innovative structures.

This thesis addresses two primary objectives.

First, to improve the performance and robustness of GaN HEMTs, aiming to extend their applicability to the $1200\,\mathrm{V}$ range. To fabricate these devices, we optimized HEMTs on sapphire, with the goal of subsequently transferring them by exfoliation onto a more thermally conductive substrate suitable for high-power applications. To this end, we used device simulations to evaluate the effects of the bonding

methods and the buffer/back-barrier choices, and we fabricated HEMTs to experimentally assess these configurations. This exfoliation approach is also applicable to vertical device fabrication.

Second, to establish and optimize the fabrication process for fully vertical GaN-on-Si trench MOSFETs. This architecture offers advantages over lateral devices, and vertical devices are the mainstream structure in power electronics (with lateral GaN HEMTs as the notable exception). Quasi-vertical and fully vertical MOSFETs were fabricated using the first iteration of this process, and simulations were conducted to identify steps for performance improvement.

This work was carried out as part of the VertiGo (Vertical GaN for High Voltage) project, initiated by the French Agence Nationale de la Recherche (project ANR-22-PEEL-2022) under the PEPR Électronique program. The project aims to develop processes for fabricating vertical GaN transistors, from epitaxy to packaging, through the coordinated efforts of several French laboratories (see Fig. 2).



Figure 2: Map of the laboratories associated with the VertiGo project and logo of the ANR and PEPR Électronique.

My research is presented in four chapters:

Chapter 1 presents the evolution of electricity management throughout history with a focus on the different types of transistors used for power conversion. Their operating principles and limitations for power management are discussed.

Chapter 2 covers the optimization of HEMTs for $1200\,\mathrm{V}$ applications. The epitaxies processed were on sapphire, with the objective of reporting them on SiC. It introduces the Silvaco TCAD environment and the simulated structures used to evaluate bonding solutions and to optimize buffer engineering and back-barrier variations. Guided by the simulation results, four epitaxial stacks were selected, and the

corresponding layers (on sapphire) were processed at IEMN. The process and electrical characterizations are presented.

Chapter 3 presents the optimization of the fabrication process for GaN vertical trench MOSFETs. It explains why this architecture was chosen for the VertiGo project and outlines the advantages of processing GaN-on-Si epitaxial stacks. After describing the baseline IEMN process, I fabricated GaN-on-Si quasi-vertical transistors and introduced targeted process variations to improve device performance. I also performed TCAD simulations to evaluate several edge-termination options. Finally, a first fully vertical trench MOSFET (V-T-MOSFET) was fabricated and characterized.

Chapter 4 outlines process and design directions to raise breakdown voltage while lowering on-state resistance in vertical trench GaN MOSFETs. On the process side, it focuses on gate fabrication optimization. On the device side, it introduces field- and current-management features, namely the p-shield and current spreading layer solutions, together with robust edge termination (p-GaN guard rings). The chapter also discusses exploratory superjunction concepts for ultimate scaling and evaluates p-type auxiliary materials (e.g., p-InGaN and NiO) to overcome limitations of Mg-doped GaN.

Chapter 1

From Silicon to Wide-Bandgap: The Evolution of Power Electronics

Power electronics is at the heart of modern society. Every time electrical energy is converted, from high-voltage transmission lines feeding cities to the compact chargers powering our smartphones, semiconductor devices perform the task of switching and controlling current and voltage. The history of power electronics is not merely a chronology of inventions; it is a narrative of technological responses to societal demands. Each new device emerged in answer to pressing needs: more efficient energy use, higher switching frequency, greater voltage and current handling, reduced system cost, and enhanced reliability. Understanding this progression is essential to grasp today's challenges, particularly the transition to wide bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN).

This chapter retraces the major steps in the evolution of semiconductor power devices, from the first controllable rectifiers of the mid-twentieth century to the silicon era of BJTs, MOSFETs, and IGBTs, to the wide bandgap revolution. The emphasis is not only on describing these devices but also on analyzing their impact, their limitations, and the motivations they created for subsequent innovations. This analytical perspective provides the foundation for understanding why lateral GaN devices are constrained, why reliability issues such as trapping phenomena remain central, and why vertical GaN architectures represent a promising direction for the future. The chapter concludes with the state of the art in recent GaN transistor technologies and an overview of the current R&D landscape and market status.

1.1 The evolution of power transistors throughout history

The evolution of electrical components has been closely tied to advances in our understanding of electricity, first in general principles and later, more specifically, in semiconductor physics during the modern era of electronics. The performance and design of these components have also been strongly influenced by developments in manufacturing technologies. This section explores the progression of electrical power management with regard to this evolution.

1.1.1 The beginnings of electricity: production, management, and use

The earliest observations of electricity were triboelectric phenomena: certain materials, when rubbed, could attract light objects. Aristotle (4th century BCE) and Pliny the Elder (1st century CE) noted that the Greek philosopher Thales of Miletus (c. 624–546 BCE) had observed this property in amber [4, 5]. His writings were lost, and the first publication that clearly described the effect is William Gilbert's *De Magnete* (1600 - [4–6]). In this work, Gilbert studied materials such as amber, glass, sulfur, and diamond, and coined the term *electricus* ("similar to amber" in Latin), derived from the Greek word for amber, $\eta\lambda\varepsilon\kappa\tau\rho o\nu$ (*electron*). At the beginning of the 17th century, however, no practical application of the *electricus* force was known.

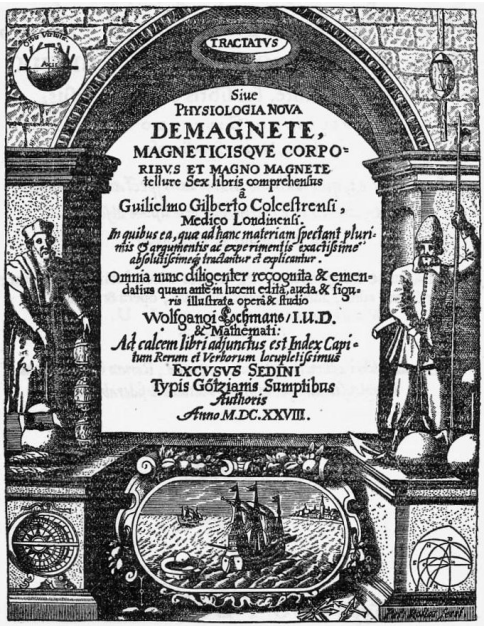


Figure 1.1: Cover of the treatise "De Magnete" from W.Gilbert - edition 1628

The first purpose-built electricity generator (c. 1672) is generally attributed to Otto von Guericke, who mounted a sulfur globe on an axle so that it could be rubbed by hand or with a leather pad to produce static electricity [4]. Despite this breakthrough, the invention did not lead to widespread use of electricity.

Nevertheless, notable developments followed, such as Francis Hauksbee's gas-discharge lamp (1705) and Pieter van Musschenbroek's Leyden jar, the first capacitor (1745).

A decisive step was taken with Alessandro Volta's electrochemical battery (1800), soon followed by Michael Faraday's invention of electromagnetic generators (1831). These laid the groundwork for the first large-scale application of electricity: Samuel Morse's telegraph system (1844), which remained in use for more than a century. The growing demand for electricity culminated in the construction of the first commercial power station in New York City in 1882, marking the beginning of urban electrification in the United States and Europe.

To manage this newly produced electricity, key components introduced during the 19th and early 20th centuries included [4, 5]:

- **Induction coil**, invented in 1836 by Nicholas Callan
- **Resistors**, theorized by Georg Simon Ohm in 1827 but widely implemented from the 1890s
- **Vacuum tube diode**, patented in 1904 by John Ambrose Fleming, based on thermionic emission
- **Semiconductor diodes**, theoretically described in a 1901 patent (granted 1904) by Jagadish Chandra Bose, who outlined their rectifying behavior,
- **Cat's whisker diodes**, patented in 1906 by Greenleaf Whittier Pickard, employing galena (PbS) crystals. They were widely used for radio detectors, although their conduction mechanism was not yet fully understood.

These innovations paved the way for technologies such as the incandescent light bulb (commercialized by Thomas Edison in 1879), radio (1895, by Guglielmo Marconi), and television (1927, by Philo Farnsworth), all of which accelerated the electrification of society in the first half of the 20th century. Before the advent of semiconductor devices, however, electronics relied primarily on vacuum tubes and electromechanical switches. These components were bulky, fragile, and inefficient: vacuum tubes, for instance, often exhibited energy losses exceeding 50% due to cathode heating.

The introduction of semiconductor diodes marked a major breakthrough, significantly reducing size, cost, and reliability issues. Still, early power-conversion systems based on semiconductors remained relatively inefficient by modern standards. The most transformative advance in electronic power management came with the invention of the transistor, which could amplify current and enabled much more complex, compact, and efficient circuits.

1.1.2 1947 - 1966: The point-contact transistor

Despite advances in solid-state physics between the 1920s and 1940s, semiconductor physics was still partly empirical when the first transistor was made, as several semiconductor-related phenomena were not fully understood. Band theory began in 1928 with Bloch, and developed through the 1930s; the drift-diffusion and continuity equations (Eq. 1.1 and 1.2) were already applied to charges in semiconductors in the 1930s and 1940s. However, many material parameters remained unclear, such as carrier lifetime and bulk/surface trap states. After a series of experiments, a team at Bell Laboratories in New Jersey, including John Bardeen and Walter Brattain, under the direction of William Shockley, developed the first point-contact transistor (using germanium) in 1947 [7, 8].

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + G_n - R_n \tag{1.1}$$

$$J_n = q\mu_n nE + qD_n \nabla n \tag{1.2}$$

- n, D_n and μ_n are the electron concentration, diffusion coefficient and mobility, respectively
- J_n is the electron current density
- G_n and R_n are the generation and recombination rate respectively
- q is the elementary charge
- E is the electric field

Equation 1.1 and 1.2: Continuity and drift-diffusion equations for electrons in a semiconductor [9]

It consists of a small block of germanium with two closely spaced metal wires (emitter and collector) placed in contact with its surface. A third terminal is connected to the opposite side of the germanium block and serves as the base (Fig. 1.2). When a small current is applied to the emitter, it injects charge carriers (electrons or holes) into the semiconductor. These carriers diffuse through the germanium and reach the collector region, where they contribute to a much larger current flow—thus achieving amplification. The base current influences the conductivity of the region between the emitter and collector, effectively controlling the collector current.

Point contact transistors were unsuitable for power conversion as they were extremely fragile. They could not withstand high current or high voltage, had low gain, and overheated easily, which further degraded performance. They were therefore optimized for high frequency (tens of MHz) and small

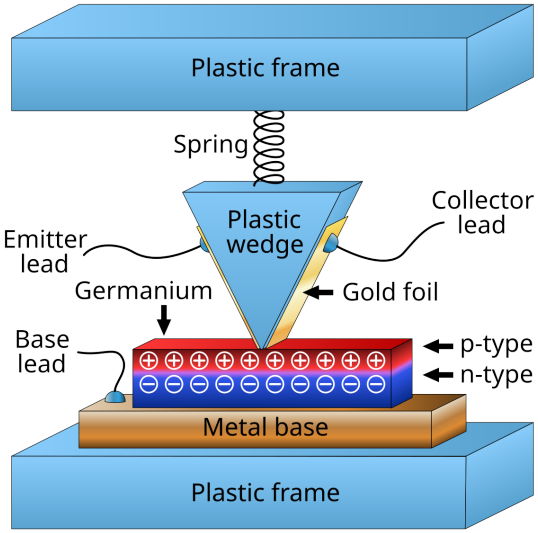


Figure 1.2: Schematic of the first transistor ever made : the germanium contact-point transistor (1948)

signal operation. Commercialization of point-contact transistors began in 1952 [10], but they remained in limited production until 1966, when they were quickly replaced by the next generation.

1.1.3 1948 - today: The Bipolar Junction Transistor (BJT)

A key milestone in modern semiconductors was the first engineered p–n junction. Russell Ohl (Bell Labs) first observed rectification in silicon in 1939, caused by naturally occurring inhomogeneous impurities forming a junction [11]. To better understand the role of impurities, teams from Bell Labs and Purdue developed methods in the early 1940s to intentionally insert dopant atoms into germanium by adding dopant species directly into the melt prior to crystal formation. The physical principles of n- and p-type conduction were clarified by Shockley's model (1949), which explained the depletion region and current transport [12], building on the experimental work of Bardeen and Brattain.

- **P-type doping:** acceptors (e.g., In or Ga in Ge) have one fewer valence electron than the host; their incorporation creates a missing electron (a hole, h^+). Electrons thermally hop to fill the vacancy, leaving a new hole. The acceptor becomes negatively ionized (A^-) and hole transport enables p-type conduction.
- **N-type doping:** donors (e.g., Sb or As in Ge) have one more valence electron than the host; the extra electron is weakly bound and can be thermally excited into the conduction band, leaving a positively ionized donor (D^+). These free electrons enable n-type conduction.

Mastering doping increased the intrinsic conductivity (Eq. 1.3) in heavily doped semiconductors, the

electron (or hole) concentration approximately equals the donor (or acceptor) density and, crucially, enabled engineered p–n junctions.

$$\sigma = q(n \cdot \mu_n + p \cdot \mu_p) \tag{1.3}$$

- σ is the electrical conductivity,
- n and p are the electron and hole concentrations respectively,
- μ_n and μ_p are their respective mobility.

Equation 1.3 Intrinsic conductivity of a semiconductor [9].

After growth, bringing p- and n-type regions into contact forms a p–n junction. Electrons from the n side diffuse to the p side and recombine with holes, leaving behind ionized dopants and establishing a space-charge region. The resulting internal electric field opposes further diffusion. Equilibrium is reached when drift (due to the built-in field) balances diffusion.

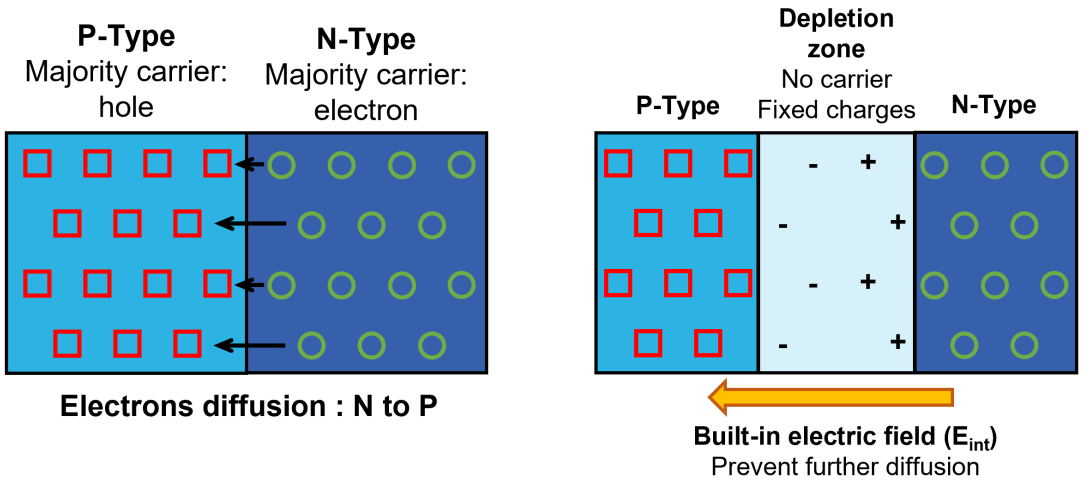


Figure 1.3: Schematic of a PN junction before (left) and after (right) equilibrium

$$\nabla \cdot E = \frac{\rho}{\varepsilon} \tag{1.4}$$

- E is the electric field,
- ρ is the space charge density,
- ε is the permittivity of the semiconductor.

Equation 1.4: Gauss's law [9].

Shockley's team proposed the Bipolar Junction Transistor (BJT) in 1948 [12]. The first BJT was fabricated in 1951 [13, 14] thanks to two major advancements: the zone refining purification method developed by W.G.Pfann [15], and the adaptation (by G.K.Teal [16, 17])of the Czochralski (initially used for metal, since 1918) to Ge to produce very pure and high quality Ge crystals.

BJTs rely on two asymmetric p–n junctions, offering better performance and manufacturability than point-contact devices. Early BJTs used planar N^+PN or P^+NP stacks with terminals on the emitter (heavily doped), base (thin, lightly doped), and collector (Fig. 1.4).

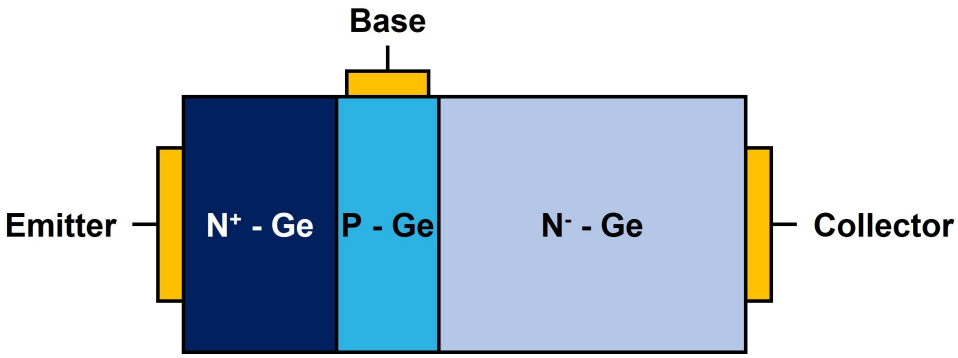


Figure 1.4: Schematic of a Bipolar Junction Transistor

BJTs are used in three main modes (example: N^+PN transistor).

In active mode, the base-emitter junction (N^+P) is forward biased (typically $V_{\mathrm{BE}} \simeq 0.7$ V in Si devices) allowing electrons from the emitter region to diffuse into the base. The emitter is heavily n-doped to enhance this diffusion. After arriving in the p-type base, these electrons may recombine with holes before reaching the collector. To aid carrier transport, the base is made very thin and lightly doped, and the base-collector junction (PN) is reverse biased ($V_{\mathrm{BC}} < 0$, typically between -0.1 and -0.7 V): the internal electric field of the p-n junction expands into the base and accelerates electrons toward the collector. Some emitter-injected carriers recombine in the base; to maintain charge neutrality, holes are supplied from the base electrode, creating a base current. The aim of this mode is current amplification: the gain factor, β, is the ratio of collector current to base current sustaining operation ($I_{\mathrm{C}} = \beta \cdot I_{\mathrm{B}}$). Typical β values range from 20 to 200.

For switching operation, saturation mode is used. The base-emitter junction is forward biased ($V_{\mathrm{BE}} \simeq$ 0.7 V) and the base-collector junction is also forward biased ($V_{\mathrm{BC}} > 0$, typically 0.1-0.3 V). This increases recombination and base current and reduces gain, but lowers the overall voltage V_{CE} since $V_{\mathrm{CE}} = V_{\mathrm{BE}} - V_{\mathrm{BC}}$. The reduced V_{CE} decreases energy loss per switching event (see below), which is why saturation was favored for power conversion.

In cutoff mode, both junctions are reverse biased, preventing current flow.

Early attempts to build high-power germanium BJTs quickly met limitations due to germanium's prop-

erties: only moderate current and voltage could be handled, and thermal stability was poor (properties degrade rapidly as temperature increases). As a result, voltages rarely exceeded 100 V, and current handling was limited to a few amperes [18].



Figure 1.5: Advertisement flyer from General Electric from 1956 for silicon power BJT.

Germanium was initially used because it is easier to melt and form pure single crystals compared with other semiconductors (low melting point, weaker bonding, high impurity intolerance and only one stable phase). In the early 1950s, the Czochralski crystal-growth and zone-refinement methods were adapted to silicon [17], enabling purification of silicon crystals. Consequently, the first Si BJT was fabricated in 1954 at Bell Labs. Silicon BJTs for power conversion were quickly produced (Fig. 1.5) and a vertical structure was adopted as early as the late 1950s / early 1960s [19], to maximize power density. Thanks to silicon's superior thermal conductivity, higher voltage tolerance, and greater stability, these transistors could operate at several hundred volts and conduct tens of amperes (see Table 1.1). Performance continued to improve with advances in epitaxial growth, packaging, and other manufacturing technologies. Silicon BJTs found early applications in DC-DC converters, solid-state power supplies, and motor controllers, and were widely adopted during the 1960s and 1970s in industrial automation, mainframe computers, aerospace, and military systems.

Despite the performance gains over the pre-transistor era, power converters based on silicon BJTs typically achieved 65–70% efficiency in the 1960s, improving to 80–85% by the late 1970s (from datasheet

Era	V_{CE} (V)	Current (A)	Switching Freq. (kHz)	Max. Power (W)	Model No.
1955 - 1959	65	5	n.s.	85	Ge 2N451 [20, 21]
1960 - 1965	60	15	n.s.	115	2N3055 [22, 23]
1966 - 1970	140	16	n.s.	150	2N3773 [24, 25]
1971 - 1975	450	15	~ 10	175	BUX48A [26]
1976 - 1980	700	5	~ 10	125	BU508 [27]
1981 - 1985	125 - 450	50 - 5	~ 50 ~ 30	250 - 83	BUV20 [28] BUT11A [29]

Table 1.1: Evolution of Si Power BJTs.

calculations). This was mainly due to three types of transistor losses.

$$P_{\text{cond}} = V_{\text{CE}} \cdot I_{\text{C}} \cdot D \tag{1.5}$$

- P_{cond} is the conduction loss,
- V_{CE} is the voltage between emitter and collector,
- I_{C} is the collector current,
- D is the duty cycle of the transistor = % of time spent on-state for each sweep

Equations 1.5: Conduction loss in BJTs [9].

Conduction loss is a consequence of the Joule effect in steady-state operation: current flowing through a resistive path generates heat. BJTs do not exhibit a well-defined on-resistance; instead, V_{BE} changes logarithmically with current density. If I_{C} is multiplied by 10, V_{BE} increases by only about 0.06 V for Si BJTs, and V_{BC} increases by an even smaller value. Therefore, when scaling up current, $V_{\text{CE(sat)}}$ increases only slightly (tens of mV), implying P_{cond} scales roughly linearly with (I_{C}). Moreover, the heat generated increases carrier injection, raising I_{C} further and potentially leading to thermal runaway.

$$P_{\text{drive}} = V_{\text{BE}} \cdot I_{\text{B}} \cdot D + Q_{\text{S}} \cdot V_{\text{BE}} \cdot f \tag{1.6}$$

- P_{drive} is the drive loss,
- V_{BE} and I_{B} are the base-emitter voltage and base current, respectively,
- D is the duty cycle of the transistor: % of time spent in fully on-state for each sweep.

Equation 1.6: Drive loss in BJTs [9].

To operate a BJT, the base electrode must inject holes into the base region to sustain electron injection from the emitter and compensate for recombination. This creates a base current, and the

associated drive loss corresponds to the power supplied to keep the BJT in conduction. This power becomes substantial at high current since I_{B} is proportional to I_{C} ($I_{\mathrm{B}} = I_{\mathrm{C}}/\beta$, where β is the current gain). During turn-off, a large amount of stored charge (holes) remains in the base and collector regions due to their relatively long lifetime. If not actively removed, these carriers slow turn-off and increase the drive required in the next cycle. To accelerate charge removal, a negative base-emitter voltage is applied, forcing a negative base current and extracting stored holes through the base contact. This speeds up the decay of the collector current. The extra energy associated with this active turn-off is approximately $Q_{\mathrm{S}} \cdot V_{\mathrm{BE}} \cdot f$, where Q_{S} is the stored charge. This term is often classified as part of the switching loss, though it can also be viewed as an additional component of the base-drive loss.

$$P_{\mathrm{sw}} \simeq \frac{1}{2} \cdot V_{\mathrm{CE}} \cdot I_{\mathrm{C}} \cdot (t_{\mathrm{on}} + t_{\mathrm{off}}) \cdot f \tag{1.7}$$

- $P_{_{\mathrm{sw}}}$ is the switching loss,
- I_{C} is the collector current,
- Q_{S} is the stored charge in the base when the BJT is turned off,
- V_{CE} is the voltage across the transistor and f its switching frequency,
- t_{on} and t_{off} are its turn-on and turn-off times respectively.

Equation 1.7: Switching loss in a BJTs [9].

The expression for P_{cond} is valid for constant I_{C} (steady-state transistor). During transitions (OFF $\rightarrow$ ON and ON $\rightarrow$ OFF), this cannot be applied over the switching intervals (t_{on} for OFF $\rightarrow$ ON and t_{off} for ON $\rightarrow$ OFF). Consequently, the Joule loss must be calculated by integrating the instantaneous product $V_{\mathrm{CE}}(t) \cdot I_{\mathrm{C}}(t)$, over the switching periods. For analytical simplicity, this integral is often approximated geometrically as a triangle, leading to Eq. 1.7.

In summary, BJT efficiency was limited mainly because BJTs are minority-carrier, current-driven devices. Minority carriers have long lifetimes, so they must be removed from the base at each switching cycle, drastically increasing switching losses and limiting maximum switching frequency. Furthermore, the output current being proportional to the drive current imposes a significant drive-power cost. For these reasons, BJTs were largely replaced in high-power systems by MOSFETs, which offer faster switching, lower gate-drive losses, and better thermal performance. The transition began in the mid-1970s, and MOSFETs became dominant in the 1980s, although some BJTs are still produced today for niche applications.

1.1.4 1969 - today: the Vertical MOSFET

To overcome BJT limitations, researchers designed a voltage-driven, majority-carrier device: the metal-oxide-semiconductor field-effect transistor (MOSFET). This became possible thanks to the maturation of two key processing techniques in the 1950s: photolithography, enabling precise patterning of complex devices [30], and thermal oxidation of silicon, producing high-quality SiO_2 passivation layers [31].

Photolithography defines patterns on a semiconductor by selectively protecting areas with a light-sensitive resist. The process typically involves three steps: spin-coating a UV-sensitive resist on the wafer; exposing the resist through a mask so that selected areas are chemically modified; and developing the resist to remove the soluble regions (for a positive resist, the exposed areas dissolve; for a negative resist, the unexposed areas dissolve). The minimum feature size is limited by diffraction to roughly 0.4–1× the light wavelength, which in early systems allowed features of tens of µm, much smaller than the hundreds of µm typical for BJTs.

The thermal oxidation of Si into SiO_2 was greatly improved by Mohamed Atalla (Bell Labs) in 1958–1959, who developed a process to grow uniform, low-leakage, passivating oxide layers. By the early 1950s, the role of bulk traps in carrier recombination was described by Shockley-Read-Hall (SRH) theory (1952–1953; see Eq. 1.8, [32, 33]), but the nature of surface traps was not yet known. Nevertheless, the effects of surface defects were empirically observed and effectively mitigated by Atalla's oxide passivation method.

$$U = \frac{n \cdot p - n_i^2}{\tau_p \left(n + n_1\right) + \tau_n \left(p + p_1\right)} \tag{1.8}$$

$$n_1 = N_c \cdot \exp\left(-\frac{E_c - E_t}{k_B T}\right) \tag{1.9}$$

$$p_1 = N_v \cdot \exp\left(-\frac{E_t - E_v}{k_B T}\right) \tag{1.10}$$

- U is the recombination rate,
- n, p are the electron and hole concentrations,
- n_i is the intrinsic carrier concentration,
- τ_n, τ_p are the electron and hole lifetimes,
- E_t is the trap energy level,
- E_c, E_v are the conduction and valence band energies,
- N_c, N_v are the effective densities of states,

- k_B is Boltzmann's constant, and T the absolute temperature.

Equation 1.8 to 1.10 Equations for the SRH (bulk) trap-assisted recombination of electrons [9].

Using these breakthroughs, J.Hoerni developed the planar process in 1959 [34]: by alternating Si oxidation, photolithography, and etching of unprotected SiO_2 (using HF solutions), smaller planar devices could be fabricated [35]. Applied at wafer scale, this enabled mass production with reproducible performance. The process was first used to improve BJTs, but was quickly exploited by M. Attala and D. Kahng to produce the first MOSFET in 1960 (planar device; Fig. 1.6 - [36, 37]).

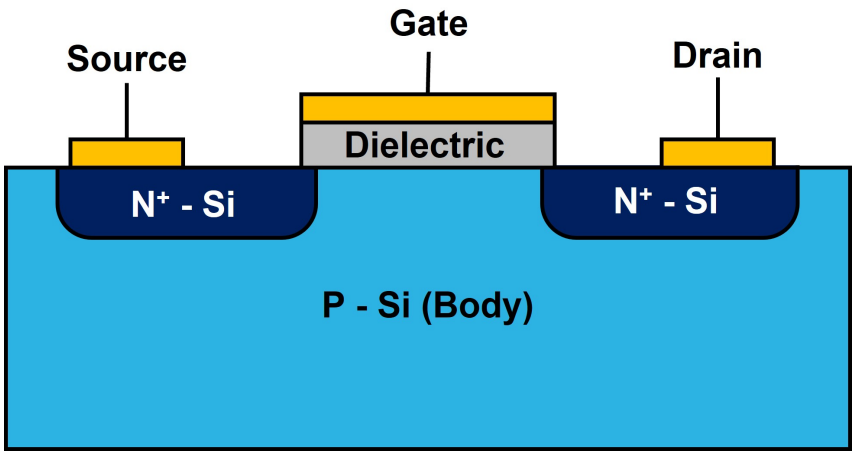


Figure 1.6: Schematic of a planar Si MOSFET

This transistor is a voltage-controlled device that regulates current flow between two terminals: the source and the drain, via a voltage applied to a third terminal, the gate. The gate electrode is electrically insulated from the semiconductor by a thin oxide layer, initially silicon dioxide but also other dielectrics (Al_2O_3, HfO_2,...).

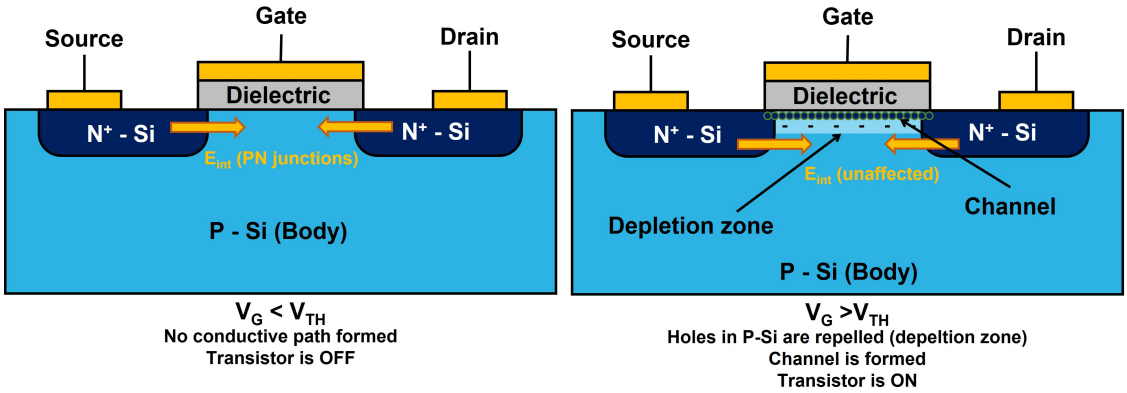


Figure 1.7: Channel formation in a planar n-channel MOSFET

When no voltage is applied to the gate, the internal electric field of the PN junction between n-Si

and the p-body prevents electrons from flowing from source to drain: the device is OFF. When the gate voltage (V_{G}) increases, an electric field appears and repels holes inside the p-Si, creating a depletion zone with negatively charged acceptors. When V_{G} reaches the threshold voltage (V_{TH}), electrons near the dielectric are promoted into the conduction band of the depleted p-Si and accumulate at the dielectric / p-Si interface, creating a conductive two-dimensional electron sheet called the channel (or inversion layer; Fig. 1.7). The channel creates a conductive path between source and drain (if $V_{\mathrm{DS}} \neq 0$), turning the device ON.

This phenomenon results from band bending induced by the gate electric field. If the conduction-band energy level (E_{C}) is above the Fermi level of p-Si, the occupancy is nearly zero (Eq. 1.11).The gate field bends the valence and conduction bands downward (toward more negative energy), adding a term $-q \cdot \psi(x)$ corresponding to the local electrostatic potential generated by the gate field. This term decreases with distance from the oxide; therefore, band bending is greatest at the oxide / p-Si interface. When V_{G} reaches V_{TH}, E_{C} approaches E_{F} and the electron population near the oxide grows exponentially (Eq.1.11): the channel forms.

$$f(E) = \frac{1}{1 + e^{\frac{E - E_{\mathrm{F}}}{k \cdot T}}} \tag{1.11}$$

- $f(E)$ and E are the occupancy probability and the energy level of the state,
- E_{F} is the Fermi level energy,
- k and T are the Boltzmann constant and temperature respectively.

Equation 1.11: Occupancy probability for a state with an energy level E [9].

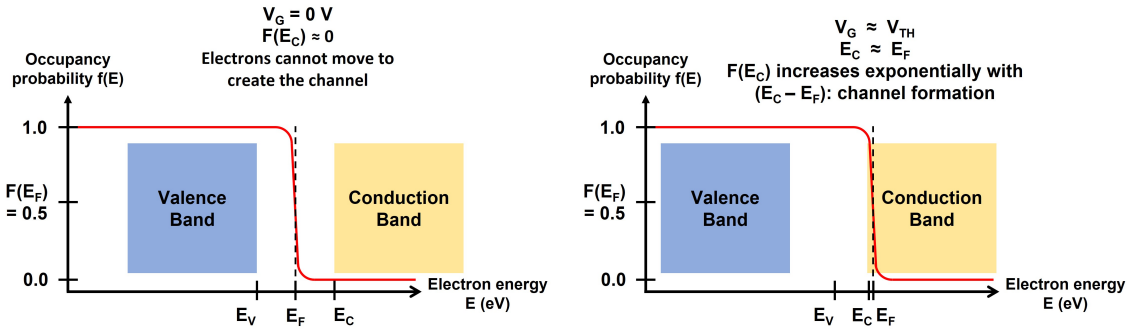


Figure 1.8: Gate induced band bending in P-Si.

MOSFET operation is divided into three regions: cutoff, linear (ohmic), and saturation. In cutoff, the gate voltage is below threshold, and the device is off. For fixed $V_{\mathrm{G}} > V_{\mathrm{TH}}$, in the linear region ($V_{\mathrm{DS}} \ll V_{\mathrm{G}} - V_{\mathrm{TH}}$), the device behaves like a variable resistor, with current increasing proportionally

to V_{DS} ($I_{\mathrm{DS}} = V_{\mathrm{DS}}/R_{\mathrm{DS(on)}}$). In saturation ($V_{\mathrm{DS}} \geq V_{\mathrm{G}} - V_{\mathrm{TH}}$), the MOSFET is fully on and the current becomes weakly dependent on V_{DS}, being controlled primarily by V_{G}($I_{\mathrm{DS}} \propto (V_{\mathrm{G}} - V_{\mathrm{TH}})^2$).

Nevertheless, planar MOSFETs were not used for power conversion in the 1960s. Despite higher switching frequency than BJTs, they could carry only small currents (a few mA) and block low voltages (tens of volts) [38]. They were used mostly for logic and memory until the invention of the vertical MOSFET in 1969.

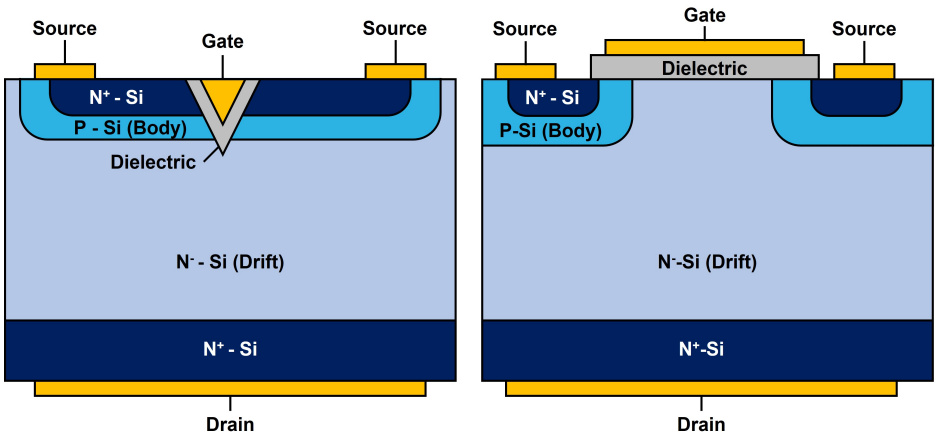


Figure 1.9: Schematics of a Si V-groove MOSFET (left) and D-MOSFET (right)

Through the 60s, many manufacturing processes improved (photolithography, SiO_2 passivation...) which leads to the fabrication of the first vertical MOSFET, the V-groove MOSFET (see Fig. 1.9), in 1969 by the Hitachi company. To enhance voltage blocking capability, a drift (lowly doped n-type $N_{\mathrm{D}} < 1\times10^{17}\,\mathrm{cm}^{-3}$) layer was added between the P-body and the drain region. In the off-state, the electric field is maximal at the P-body / drift layer interface and depends on both the voltage applied (V_{DS}) and the doping of the drift layer ($E_{\mathrm{MAX}} \simeq \sqrt{q \cdot N_{\mathrm{D}} \cdot V_{\mathrm{DS}}/(2 \cdot \varepsilon)}$, from a 1D depletion approximation). Thus, the critical electric field is reached at higher voltage if N_{D} is lower. In V-groove MOSFETs, electrons cross the p-Si vertically via a channel on the sidewalls of a V-shaped trench. These devices were functional, but limited by the V-notch (field crowding, reduced doping control), restricting voltage handling to tens of volts [39]. They were used for low-voltage (¡ 100 V), moderate-current (1 - 5 A) conversion until replaced by a more efficient design, the double-diffused MOSFET (D-MOSFET; Fig. 1.9).

The first D-MOSFET was also presented in 1969 by a team from the Electrotechnical Laboratory in Japan [40]. More complex to fabricate than V-groove MOSFETs, they reached the market in the mid-1970s, and quickly replaced BJTs for low-to medium- current and voltage power conversion. Today, Si MOSFETs can withstand up to 1700 V [41], conduct hundreds of amperes [42] or switch at hundreds of MHz [43]. Because they are voltage-driven, D-MOSFETs offered many advantages over BJTs but also few drawbacks.

$$P_{\text{cond}} = I^2 \cdot R_{\text{DS(on)}} \tag{1.12}$$

- P_{cond} is the conduction loss, I is the output current,
- $R_{\text{DS(on)}}$ is the on-state resistance of the MOSFET,
- V is the voltage across the transistor.

Equation 1.12: Conduction loss in MOSFETs [9].

At low current, $I^2 \cdot R_{\text{DS(on)}}$ is often much smaller than $V_{CE,sat} \cdot I$ for BJTs, giving MOSFETs lower conduction loss. At high current, quadratic scaling limits their use. High-voltage blocking is challenging: $R_{\text{DS(on)}}$ increases strongly with breakdown voltage, since a thicker, lower-doped drift region is needed. However, for low or medium current, low $R_{\text{DS(on)}}$ can be achieved, leading to lower conduction loss than in BJTs.

The switching-loss expression for D-MOSFETs is also Eq. 1.7, since no unique $R_{\text{DS(on)}}$ applies during transitions. Owing to rapid channel formation, turn-on and turn-off times are much shorter, usually tens of nanoseconds, compared to hundreds for BJTs, leading to significantly lower switching loss. This improvement allowed efficient operation at frequencies an order of magnitude higher than BJTs (up to several 100 kHz in the 1970s–1980s [44]).

$$P_{\text{gate}} = Q_{\text{G}} \cdot V_{\text{GS}} \cdot f \tag{1.13}$$

- P_{gate} is the gate drive loss,
- V_{GS} and Q_{G} the gate voltage and charge, respectively,
- f is the switching frequency of the transistor

Equation 1.13: Gate drive loss in a MOSFET [9].

The gate-drive loss (P_{gate}) is analogous to the base-drive loss of BJTs: it is the power to operate the gate. Because the MOSFET gate is insulated by an oxide, there is no steady gate current. Instead, P_{gate} corresponds to the energy to charge/discharge Q_{G} to form/deplete the channel. This loss is significantly smaller than the drive loss of BJTs.

$$P_{\text{Coss}} = Q_{\text{Coss}} \cdot V_{\text{DS}} \cdot f \tag{1.14}$$

- P_{Coss} and Q_{Coss} are the output capacitance loss and output charge, respectively,

- V_{DS} is the drain voltage,
- f is the switching frequency of the transistor

Equation 1.14: Capacitive switching loss [9].

This is analogous to P_{gate}: charges (Q_{Coss}) move when the device turns on/off. Because V_{DS} is not zero when turning off (only the gate is depleted), the drain electrode withdraws electrons from the drain/drift region. These charges must be re-injected at turn-on, hence P_{Coss}. This loss depends on drift-region properties (the drain is almost not depleted) and becomes important at high frequency or high voltage. This loss also exists in BJTs but is negligible compared with other terms.

In conclusion, MOSFET efficiency is generally higher than that of BJTs thanks to significantly reduced switching and gate-drive losses. Thus, by the late 1970s, D-MOSFETs had replaced BJTs in low- and medium-voltage conversion, while BJTs remained preferred in high-voltage, high-current ($>$500 V, $>$20 A) domains until the introduction of the IGBT.

1.1.5 1983 – Today: The IGBT

The first theoretical concept of the IGBT dates to the late 1970s [45], but the first device was fabricated in 1983 by General Electric [46]. The emergence of IGBTs in the early 1980s was enabled by advances in silicon processing. While the first prototypes (1982–83) relied mainly on planar diffusion, ion implantation, and epitaxial growth, more advanced techniques soon became decisive. Low-pressure CVD [47], already industrial by the 1970s, provided high-quality epitaxial drift layers, while reactive ion etching (RIE; late 1970s [48]) and inductively coupled plasma RIE (ICP-RIE; late 1980s [49]) enabled trench gates and precise junction terminations. Without these breakthroughs, the high-performance IGBTs of the late 1980s–1990s could not have been realized. IGBTs were widely adopted by the late 1980s and early 1990s.

The objective of the IGBT is to combine an n-channel MOSFET with a PNP BJT to obtain a voltage-driven, mixed-carrier (majority and minority) device. This is achieved by forming an N^+/P/N^-/P^+ stack (Fig. 1.10). The N^+ region is the source (emitter), the P layer is the body region, the N^- layer is the drift region, and the P^+ layer is the injection layer. In this stack, the MOS gate covers the P-body and forms a MOSFET using the source, body, and drift regions.

Two BJT-like structures can be identified: an NPN transistor formed by Source (N^+)/Body (P)/Drift (N^-), which is parasitic; and a PNP transistor formed by Body (P)/Drift (N^-)/Injection layer (P^+), which is the intended conduction path. The parasitic NPN is suppressed by short-circuiting the source and body via the emitter electrode, enforcing $V_{\mathrm{BS}} = 0$ V since the electrode is usually grounded.

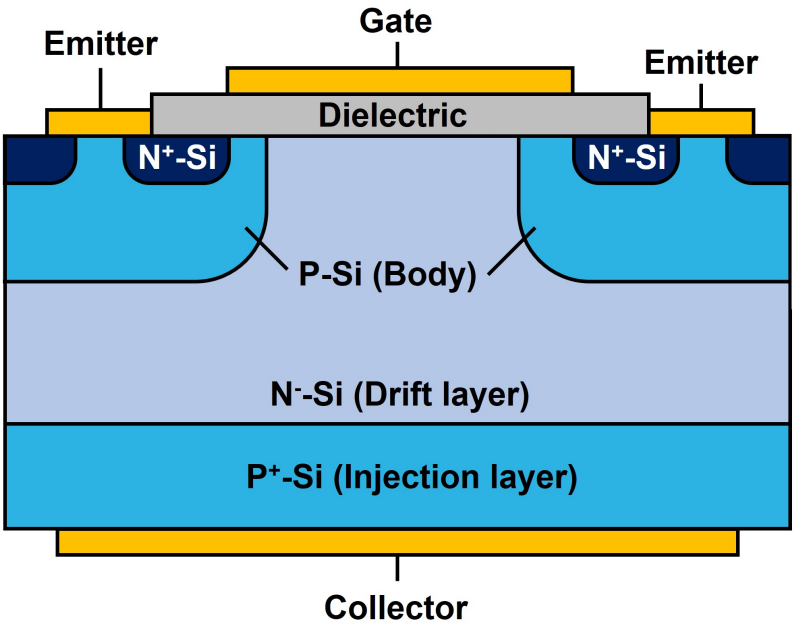


Figure 1.10: Schematic of an IGBT

When the gate voltage exceeds threshold, a channel forms at the surface of the P-body below the gate dielectric (see Section 1.1.4). Once the channel is formed and a collector-emitter voltage (V_{CE}) is applied, the potential distribution imposes the following:

- electrons flow from the source through the channel into the drift region and are accelerated toward the collector, with a small fraction recombining in the P^+ injection layer;
- the Body–Drift PN junction allows a small diffusion of holes from the P-body into the drift (below the channel, where holes are over-concentrated);
- and the Injection-layer–Drift PN junction is forward-biased, causing the injection layer to supply a large number of holes into the drift region.

Owing to the massive injection of holes and electrons into the drift region, it becomes highly conductive (plasma or conductivity modulation; see Eq. 1.3), drastically reducing device resistance. This allows very high currents to flow with minimal conduction loss and permits the use of a thick drift layer to maximize blocking voltage without a significant resistance penalty. These are the main advantages of IGBTs. However, due to their operating principle, IGBTs share a drawback with BJTs: minority carriers (holes) remain in the drift region after turn-off. Moreover, these carriers cannot be actively swept away as in BJTs because the drift region is isolated, leading to slower switching (tens of kHz) compared with BJTs.

Overall, IGBTs exhibit low conduction loss ($P_{\mathrm{cond}} = V_{\mathrm{CE}}(I_{\mathrm{C}}) \cdot I_{\mathrm{C}}$, with $V_{\mathrm{CE}}(I_{\mathrm{C}}) < R_{\mathrm{DS(on)}} \cdot I_{\mathrm{C}}$ at high current) and low gate-drive loss (Eq. 1.13), but high switching loss (Eq. 1.7) caused by the long turn-off time ($t_{\mathrm{off}} \simeq$ recombination time of holes injected into the drift). For these reasons, IGBTs are very efficient in high-current, low-frequency applications [50].

Today, the overwhelming majority of power converters use Si power MOSFETs and IGBTs due to their low cost and efficiency. Nevertheless, new options emerged in the 2000s owing to the superior properties of novel semiconductor materials.

1.1.6 1999 - today: SiC power MOSFETs

As early as 1989, researchers began to point out the physical limits of silicon for power applications and sought figures of merit to identify better materials. B.J.Baliga proposed a figure of merit for power devices (Baliga's FOM, BFOM=$\varepsilon\mu_n E_{\mathrm{C}}^3$) in 1989 [51], and identified SiC and diamond as potential replacements for silicon. In general, five intrinsic properties are required for a semiconductor to perform well in power conversion:

- **a wide bandgap $\mathbf{E_g}$ (**eV**)**, which correlates with higher critical field $\mathrm{E}_C(\propto \mathrm{E}_g^{2-2.5})$, reduced leakage ($I_{leak} \propto e^{-E_g/kT}$), and higher-temperature operation;
- **a high critical electric field $\mathbf{E_C}$ (**$\mathrm{MV\,cm^{-1}}$**)**, which enables thinner blocking layers and lower resistance;
- **high electron and hole mobilities $\boldsymbol{\mu_e}$ and $\boldsymbol{\mu_h}$ (**$\mathrm{cm^2\,V^{-1}\,s^{-1}}$**)**, which reduce channel resistance and speed channel dynamics (lower t_{on} and switching losses, Eq. 1.7);
- **a high electron saturation velocity $\mathbf{v_{sat,e}}$ (**$\mathrm{cm\,s^{-1}}$**)**, which limits I_{sat} at high fields ($\mathrm{I}_{\mathrm{sat}} \lesssim q \cdot n \cdot A \cdot v_{\mathrm{sat}}$, with A the active area);
- **and a high thermal conductivity $\boldsymbol{\kappa}$ (**$\mathrm{W\,cm^{-1}\,K^{-1}}$**)** to remove heat and prevent local overheating and thermal runaway.

Compared against these metrics, silicon is not ideal for high-performance power electronics: it has a small bandgap (1.1 eV), low critical field ($0.3\,\mathrm{MV\,cm^{-1}}$), modest thermal conductivity ($1.5\,\mathrm{W\,cm^{-1}\,K^{-1}}$) and moderate electron saturation velocity ($1 \times 10^7\,\mathrm{cm\,s^{-1}}$). Consequently, many materials came under investigation in the 1990s-2000s as potential replacements for Si, including silicon carbide (SiC), gallium nitride (GaN), aluminum nitride (AlN), gallium oxide ($\mathrm{Ga_2O_3}$), and diamond ($\mathrm{C}_{diamond}$).

SiC was the first material to replace silicon in power applications. It is a group-IV semiconductor with over 200 polytypes, though four are commonly used in the literature: 3C-SiC (cubic), 15R-SiC

(rhombohedral), and 6H-SiC and 4H-SiC (both hexagonal). For power applications, 4H-SiC is dominant (6H-SiC is used in niche cases) due to superior properties: a high critical field ($\sim 3.0\,\mathrm{MV\,cm^{-1}}$), good electron mobility ($\sim 1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$), and excellent thermal conductivity (up to $\sim 4.9\,\mathrm{W\,cm^{-1}\,K^{-1}}$).

The first method to produce SiC dates to 1891 (patented 1893) by E.G.Acheson, yielding impure powder/lumps [52]. These impurities nonetheless enabled early radio detectors [53]. A major advance came with attempts to produce bulk SiC substrates by sublimation: a method was patented in 1954 by Jan Anthony Lely [54]; production was improved in 1960 (D.R.Hamilton [55]) and 1968 (V.P.Novikov and V.I.Ionov [56]) but substrates remained defect-ridden, delaying commercial power devices for decades. The first 4H-SiC vertical power MOSFET was reported in 1999 by Yano et al. [57]. The first industrial SiC MOSFETs for power applications were presented by ROHM in December 2010 (600 V class - [58]) and by Cree (renamed Wolfspeed in 2021 [59, 60]) in January 2011 (1200 V class). Today (2025), SiC MOSFETs are commonly used in the 1200 - 3300 V range [61, 62] for fast switching, and research is ongoing to push breakdown to $\sim 10\,\mathrm{kV}$ [63].

Nevertheless, due to its production method (sublimation at 2000 - 2400 °C), which requires large energy, and its challenging dicing (Mohs hardness 9.2), bulk SiC substrates remain expensive, and production is growing more slowly than demand [64]. This is a major drawback since SiC devices are produced using homoepitaxy (SiC cannot be grown on silicon due to large lattice and thermal-expansion mismatches). To address this issue, another material with similar or superior properties has attracted intense research in recent years : gallium nitride.

2009 - today: GaN power HEMTs

After SiC, GaN became the third material to be deployed in power applications. It presents several advantages over SiC: a higher breakdown electric field ($\sim 3.4\,\mathrm{MV\,cm^{-1}}$) and higher electron mobility ($\sim 1400\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in undoped material), though it suffers from lower thermal conductivity (up to $\sim 2.3\,\mathrm{W\,cm^{-1}\,K^{-1}}$ for high-purity bulk GaN). A key advantage over SiC is its smaller lattice parameter, which allows growth on silicon substrates (with buffer layers to compensate strain), enabling high-volume, cost-effective fabrication in standard silicon fabs and leveraging CMOS infrastructure. Gallium nitride is a III-V semiconductor with two main polytypes: zinc blende (cubic) and wurtzite (hexagonal; Fig. 1.11 [65]). The cubic phase is metastable and a research topic; currently only wurtzite GaN (stable) is used.

The first fabrication of GaN dates to 1969 by Maruska and Tietjen at RCA Laboratories using hydride vapor phase epitaxy (HVPE) [66]. Early material, like early SiC, exhibited high defect density, and researchers struggled to implement p-type doping. These issues were solved in the late 1980s / early

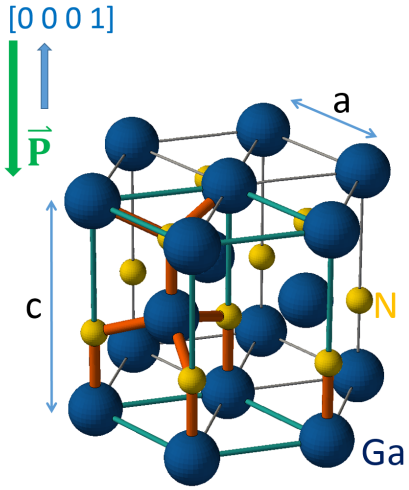


Figure 1.11: Wurtzite GaN lattice

1990s with the work of S.Nakamura, H.Amano, and I.Akasaki, who developed Mg p-type doping for GaN [67, 68] and optimized epitaxy, especially buffer layers on sapphire [69, 70]. This led to GaN's first mass-market application: the blue LED (1994; [71]). With high-quality GaN growth came another application (early 2000s): the high-electron-mobility transistor (HEMT). The first power HEMTs were made in the mid-1990s [72], but GaN-on-Si power HEMTs reached the market in 2009 (Efficient Power Conversion; [73]).

Property	**Si**	**4H-SiC**	**GaN**
Bandgap (eV)	1.12	3.26	3.43
Lattice parameter (Å)	(<111> plan) 3.840	3.073	3.189
Breakdown Electric Field ($\mathrm{MV\,cm^{-1}}$)	0.3	3.0	3.3
Electron Mobility ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	1400	800 - 1000	900 - 1500
Hole Mobility ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	450	115	150 - 200
Electron Saturation Velocity ($10^7\,\mathrm{cm\,s^{-1}}$)	1.0	2.0	2.5
Hole Saturation Velocity ($10^7\,\mathrm{cm\,s^{-1}}$)	0.8	1.5	1.5
Thermal Conductivity ($\mathrm{W\,cm^{-1}\,K^{-1}}$)	1.5	4.9	1.3
Piezoelectric constant e_{33} ($\mathrm{C\,m^{-2}}$) Piezoelectric constant e_{31} ($\mathrm{C\,m^{-2}}$)	0 0	0.67 -0.22	0.73 -0.49

Table 1.2: Comparison of the main properties of Si, 4H-SiC and GaN

These structures leverage the piezoelectric property of GaN (Tab. 1.2 and Eq. 1.8 to Eq. 1.12 - [74]) and AlGaN. Spontaneous polarization arises from the non-centrosymmetric wurtzite lattice (aligned Ga–N dipoles), this implies partial charge ($+\delta$ on Ga and $-\delta$ on the N atom), inducing a dipole moment for each bond ($p_{bond} = |\delta| \cdot d$, where d is the dipole displacement vector from $-\delta$ to $+\delta$). The polarization of GaN corresponds to sum of all dipoles per volume, and the dipoles along the c-axis do not cancel, but instead add up, leading to a net spontaneous polarization (Eq. 1.15). This dipoles (and the polar-

ization) can be strengthened by applying a strain on GaN (Eq. 1.17 and 1.18), leading to a piezoelectric polarization (Eq. 1.16) cumulative to the spontaneous one (Eq. 1.19).

$$P_{\mathrm{sp}} \approx -0.029\mathrm{C/m}^2 \tag{1.15}$$

$$P_{\mathrm{pz}} = 2e_{31}\,\varepsilon_{xx} + e_{33}\,\varepsilon_{zz} \tag{1.16}$$

$$\varepsilon_{xx} = \frac{a_{sub} - a_0}{a_0} \tag{1.17}$$

$$\varepsilon_{zz} = -2\frac{C_{13}}{C_{33}}\,\varepsilon_{xx} \tag{1.18}$$

$$P_{\mathrm{tot}} = P_{\mathrm{sp}} + P_{\mathrm{pz}} \tag{1.19}$$

- P_{sp}, P_{pz} and P_{tot} are the spontaneous, piezoelectric and total polarization, respectively,
- e_{31} and e_{33} are the piezoelectric coefficients,
- ε_{xx} and ε_{zz} are the in-plane and out-of-plane strain respectively,
- a_{sub} and a_0 are the substrate and relaxed material lattice parameters respectively,
- C_{13} and C_{33} are the elastic stiffness coefficients.

Equations 1.15 to 1.19: Equations of the c-axis polarization of GaN. Off axis polarization is usually negligible in GaN HEMT

When a strained AlGaN layer is deposited on GaN, the total polarization in AlGaN (spontaneous + piezoelectric) is larger than in the underlying GaN. The resulting polarization discontinuity creates a sheet of positive bound charge at the interface, which generates an electric field that bends the GaN conduction band downward. Where the conduction band dips below the Fermi level, electrons accumulate (sourced from the bulk, surface states, or contacts) and are confined in a triangular quantum well (Fig. 1.12), forming a two-dimensional electron gas (2DEG) with sheet density $N_{\mathrm{S}} \simeq 1 \times 10^{13}\,\mathrm{cm}^{-2}$ and mobility around $2000\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$. This makes the HEMT well suited for fast-switching applications. Moreover, the 2DEG properties (mobility and sheet charge) can be tuned by the Al content or the AlGaN thickness.

GaN power HEMTs are often grown on silicon substrates for cost reasons and comprise at minimum four layers: a transition layer (since GaN cannot be grown directly on Si), a semi-insulating layer to prevent leakage toward the substrate, an unintentionally doped (UID) GaN layer hosting the 2DEG, and an AlGaN barrier layer to create the 2DEG (Fig. 1.13). A passivation layer is usually deposited on top to mitigate adverse surface-defect effects.

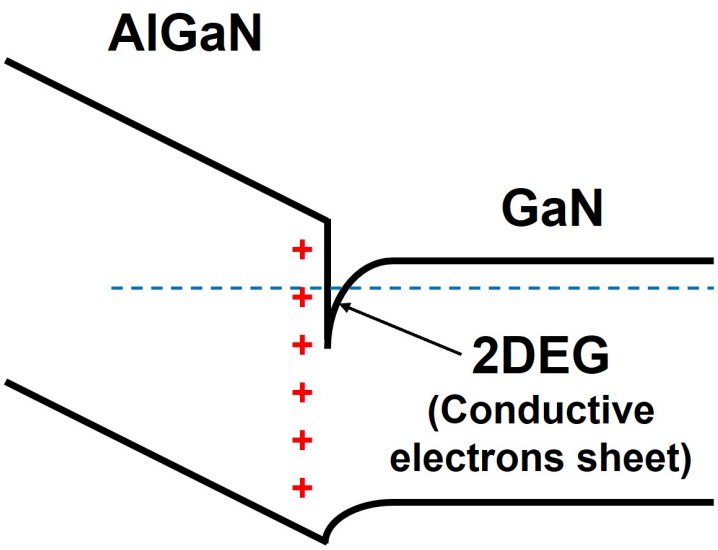


Figure 1.12: Schematics of a GaN-on-Si HEMT

GaN HEMTs exhibit shorter turn-on and turn-off times and lower Q_{G} and Q_{Coss} than SiC MOSFETs, reducing switching losses and enabling operation into the MHz range (versus hundreds of kHz typical for SiC in comparable power classes [75]). They are therefore more energy-efficient at a given power level, generate less heat, and allow smaller passive components, enabling compact, lightweight power systems.

Nevertheless, HEMTs have a major disadvantage compared with SiC MOSFETs: they are normally-on (conducting at V_{G} = 0 V) when using a Schottky-gate or MIS-gate. These HEMTs are called depletion-mode (or simply d-mode) HEMTs. For fail-safe operation and better compatibility with standard logic and gate drivers, a normally-off transistor is preferable. Such HEMTs exist, enhancement mode (e-mode) HEMTs, but they require additional process steps, such as recessed gates (demanding precise etching that can damage the surface) or accurate p-GaN growth and etching. These drawbacks did not prevent HEMTs from becoming dominant in medium-voltage applications.

High voltage scaling is, however, more problematic than with SiC, despite a few companies offering 900 V and 1200 V-class HEMTs [76]. Several challenges remain:

- thermal management (heat is generated close to the surface and must be evacuated);
- breakdown voltage scaling with device length (gate-to-drain distance), which increases footprint and cost;
- trapping in the structure, which increases dynamic resistance and causes current collapse;
- achieving a normally-off state, which usually requires complex processing;

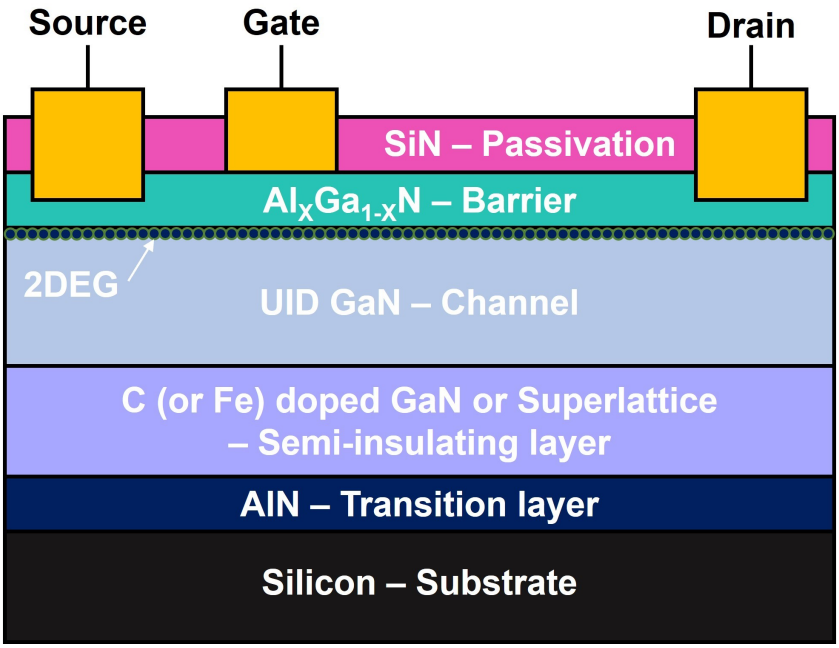


Figure 1.13: Schematics of a GaN-on-Si HEMT

- and improving epitaxy quality on silicon to reduce dislocations and leakage

In conclusion, GaN HEMTs combine exceptional switching performance with compelling integration pathways, but their wider adoption in high-power, high-voltage domains is constrained by field management, trapping phenomena, and normally-off implementation. To provide the necessary background for this thesis, the following section reviews the state of the art in GaN power transistors across both commercial and experimental domains. It covers lateral and vertical device families, novel gate and buffer concepts, and selected performance demonstrations that illustrate the opportunities and challenges of GaN as a power semiconductor. This survey establishes the context for the experimental work presented in Chapter 2.

1.1.7 Trapping phenomena and reliability as the central bottleneck

While material figures of merit and device topology largely determine the theoretical limits of power transistors, it is the interaction between high electric fields, defects, and carrier dynamics that most often dictates their practical performance and lifetime. In gallium nitride, this interaction manifests through charge trapping at surfaces, interfaces, and within the buffer, producing a characteristic set of degradations: dynamic on-resistance increase, current collapse, threshold-voltage shift, gate lag and drain lag that directly impact converter efficiency, thermal design, and reliability margins. As GaN transitions from medium-voltage fast switching toward higher blocking voltages and harsher operating conditions, these trapping-related effects become the primary bottleneck to wider industrial deployment.

Traps in GaN power devices can be categorized by location and by time constant. Surface states at the passivated access regions (particularly near the gate–drain edge) and interface states at the AlGaN/GaN heterojunction interact strongly with the two-dimensional electron gas (2DEG). In the volume, intentional deep levels introduced for buffer isolation (e.g., carbon) coexist with unintentional point defects and dislocation-related states. Depending on their capture cross-sections and energetic position, traps exhibit fast or slow dynamics. Fast traps exchange charge on microsecond to millisecond scales and are typically probed by pulsed I–V; slow traps respond over seconds to hours and dominate long-term drifts and bias-temperature instabilities. The SRH framework introduced earlier (Eq. 1.8-1.10) provides a convenient description: capture and emission rates set the instantaneous occupancy, while the local band bending and carrier concentrations, both field-dependent, control the net recombination or storage of charge.

Under high electric field in the off-state, electrons are injected into surface or buffer traps by field-assisted mechanisms. When the device is subsequently driven on, the trapped negative charge screens the 2DEG, locally depleting the channel and raising the apparent on-resistance. This is the microscopic origin of dynamic $R_{\mathrm{DS(on}}$ and current collapse observed after high-voltage stress. The effect is strongest near the gate-field plate edge, where the lateral field peaks, and in access regions where surface potential is most sensitive to trapped charge. A complementary manifestation is gate lag and drain lag: when a step-in gate or drain bias is applied, the drain current recovers only after traps re-emit carriers, producing a transient deficit that encodes the trap spectrum. Because capture and emission are thermally activated, both the magnitude and the recovery time of these lags depend on temperature; Arrhenius analysis of time constants thus reveals the energetic depth of the dominant states.

Buffer engineering for vertical isolation introduces an additional, intrinsically conflicting constraint. Carbon doping in the GaN buffer is highly effective at suppressing leakage to the substrate, but it also creates deep acceptor levels that act as electron traps. During high-field off-state stress, these centers capture electrons and become negatively charged, which elevates the electric field in adjacent regions and can bend the conduction band upward at the channel, again increasing dynamic resistance. In extreme cases, space-charge buildup in the buffer redistributes the internal field, lowering the effective breakdown voltage or shifting the device into regimes where hot-carrier effects and impact ionization accelerate degradation. Thus, the very strategy used to achieve low leakage compromises dynamic performance and reliability, unless the buffer and field-management design (field plates, terminations, cap layers) are co-optimized.

Reliability in GaN power devices is therefore inseparable from trapping. Classical metrics such as time-dependent dielectric breakdown (TDDB) of the gate stack, bias-temperature instability (BTI), and

hot-carrier injection (HCI) remain relevant, but they are now coupled to polarization-induced fields and to the heterostructure electrostatics. In MIS-gate HEMTs, for instance, the oxide/AlGaN interface quality governs threshold-voltage stability; positive or negative bias temperature stress produces reproducible V_{TH} shifts that reflect the net trapping in the oxide and at the interface. In Schottky-gate devices, barrier-height modulation by trapped charge and localized field crowding near the gate edge control gate leakage and long-term drift. Because real converters combine high dv/dt, high di/dt, and repetitive off-state over-voltage (freewheel recovery, ringing), the dynamic component of these phenomena, not their static I–V surrogates, ultimately determines usable switching frequency, conduction losses, and safe-operating-area margins.

Characterization methodologies have evolved to isolate and quantify these effects. Pulsed I–V measurements with carefully chosen quiescent biases separate channel transport from self-heating and reveal dynamic $R_{\mathrm{DS(on)}}$ as a function of prior stress. Gate- and drain-lag protocols monitor the transient drain current following abrupt bias steps, building a time-constant spectrum that can be analyzed against SRH kinetics. Double-pulse tests under realistic load replicate converter stress and expose collapse during hard switching. To probe the buffer, drain-current transient (DCT) and deep-level transient spectroscopy variants resolve emission kinetics from deep centers. Temperature-dependent measurements distinguish trap families by activation energy, and isothermal bias stress tracks V_{TH} drift and recovery pathways. In each case, the link between a measured macroscopic symptom (current deficit, resistance increase, threshold shift) and a microscopic mechanism (specific trap location, depth, and capture cross-section) is made through controlled electrostatics and, where applicable, calibrated TCAD.

Mitigation strategies follow directly from this picture. High-quality surface passivation suppresses surface states and stabilizes the access-region potential; field-plate engineering redistributes the lateral electric field to reduce peak fields at the gate edge and along the drain access. In the gate stack, high-κ dielectrics with low interface-state density and robust processing minimize oxide charging and V_{TH} drift. In the buffer, reduced or compensated carbon incorporation, alternative deep-level schemes, and superlattice interlayers can retain vertical isolation while lowering trap density and charge storage. Cap layers and gentle plasma treatments tune surface Fermi-level pinning without generating additional damage. At the circuit level, snubber networks and optimized layouts reduce overshoot and ringing, limiting the high-field stress that seeds trapping during operation. Each of these measures improves a piece of the puzzle; only their co-optimization delivers sustained dynamic performance.

Crucially, emphasizing traps and reliability clarifies the architectural trade-off between lateral and vertical GaN. In lateral HEMTs, the blocking field is largely lateral and concentrated near the surface, exactly where trap densities and interface instabilities are most consequential. Surface and interface

traps therefore couple strongly into the channel electrostatics, and field-plate design becomes a delicate balance between breakdown, dynamic resistance, and switching loss. In vertical GaN devices, by contrast, the blocking region is placed in the bulk drift layer; the highest fields are distributed away from the surface, and the conduction path is less exposed to surface and access-region charging. While vertical architectures introduce their own challenges (thick, low-defect epitaxy; termination design; and substrate quality), they inherently decouple the dominant trapping sites from the active channel, offering a more stable platform for high-voltage switching and long-term reliability. Addressing trapping and reliability is thus a prerequisite for the industrial adoption of GaN beyond consumer and IT markets.

1.2 State-of-the-art for GaN power components

Thanks to their excellent switching speed and efficiency, GaN transistors are now widely used in the 650 V class. A few manufacturers have begun offering 1.2 kV devices [76], and active research continues to push performance further. This section reviews the most relevant publications on breakdown-voltage (BV) enhancement in lateral HEMTs and summarizes the status of emerging vertical GaN device architectures that could enter the power market in the coming years.

1.2.1 State-of-the-art for GaN power HEMT

Because most lateral GaN HEMTs are not avalanche-rated, converter designers must ensure that the worst-case peak drain voltage (including overshoot and ringing) remains $\sim$ 20–50% below the device's $V_{\mathrm{DS,max}}$. In practice, this headroom, rather than avalanche energy absorption, protects the device during transients. Consequently, a HEMT targeted at 1.2 kV applications should demonstrate a BV in the range of $\sim$ 1.5-1.8 kV to guarantee safe operation in realistic circuits.

A straightforward path to higher BV is to increase the gate–drain spacing; however, this also increases specific on-resistance $\mathrm{R_{on,sp}}$, device footprint, and switching losses via a larger Q_{Coss}. Current research therefore focuses on maximizing BV while minimizing $\mathrm{R_{on,sp}}$, ideally approaching the material-limited trade-off. The figure below plots $R_{\mathrm{on,sp}}$ versus breakdown voltage for a broad set of HEMTs and substrates/technologies, compiled from [77–103]

The legend indicates the substrates used for GaN epitaxial growth and whether the transistor is normally-on (D-mode) or normally-off (E-mode). The black lines correspond to the theoretical conduction limit for the indicated materials ($R^{\mathrm{min}}_{\mathrm{on,sp}} = 4 \cdot V^2_{\mathrm{BR}} / \varepsilon_s \cdot \mu_s \cdot E^3_c$) and are useful as a first-order benchmark. It is important to note that the specific resistance $R_{\mathrm{on,sp}}$ is typically measured at 25 ℃ under static conditions and therefore does not represent the effective resistance under switching. In operation, the relevant

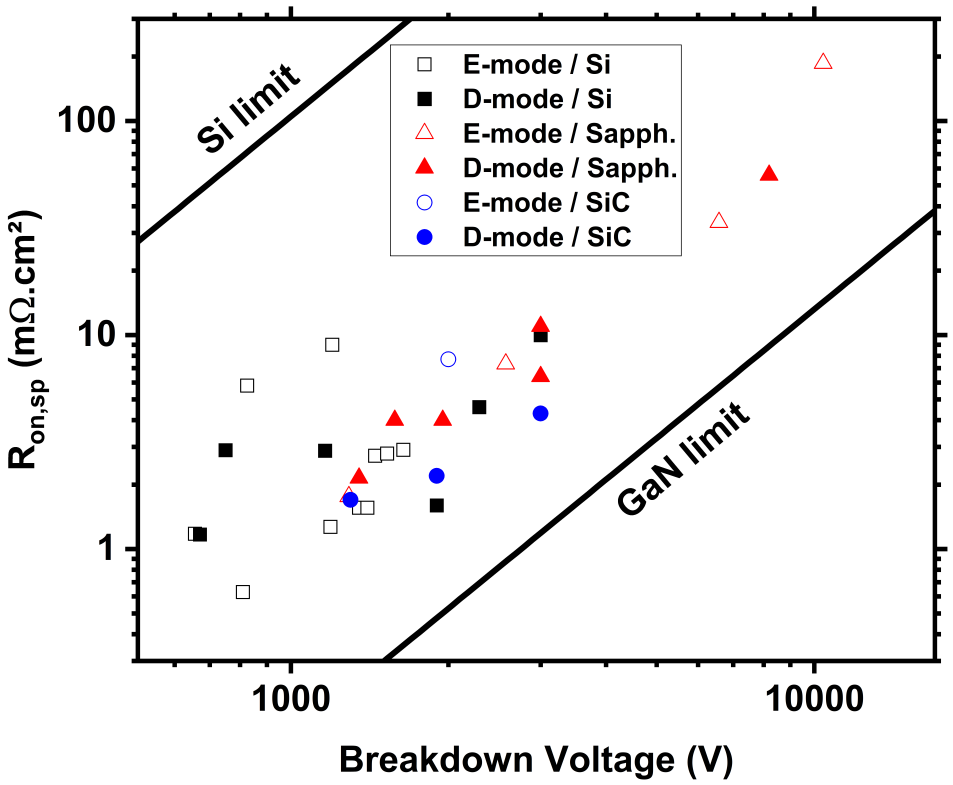


Figure 1.14: Breakdown voltage / specific on-resistance trade-off state-of-the-art of lateral GaN HEMTs for power applications

metric is the dynamic specific resistance: ($R^{\mathrm{dyn}}_{\mathrm{on,sp}} = R_{\mathrm{on,sp}} \cdot K^{\mathrm{dyn}}$ where K^{dyn} is the collapse factor ($\geqslant$ 1)). K^{dyn} depends on trapping (surface/interface/buffer), on the stress conditions (V_{DS}, V_{GS}), frequency, temperature, and the applied waveform. Because many academic reports omit K^{dyn}, a device that appears close to the conduction limit in static testing may still suffer significant current collapse under hard-switching.

In the 1.2–1.5 kV window, lateral GaN HEMTs can match SiC on static conduction metrics, but several factors still favor SiC MOSFETs in real converters: limited avalanche/short-circuit capability in many GaN processes, trapping-induced $R^{\mathrm{dyn}}_{\mathrm{on,sp}}$ larger output and reverse-recovery-like capacitive charges at high BV, and overall maturity/qualification in automotive and traction standards. These constraints motivate, in parallel with lateral HEMT optimization, the exploration of vertical GaN transistors for the multi-kilovolt regime.

1.2.2 Promising structures

Compared with lateral GaN HEMTs, vertical GaN power devices offer:

- **BV scaling with thickness:** the blocking region is the drift layer, so breakdown voltage scales

primarily with drift-layer thickness and doping, without increasing lateral footprint (aside from termination).

- **Better thermal path:** conduction losses are distributed through the bulk drift and can be extracted via a thinned, metalized backside, reducing thermal resistance compared with surface-constrained lateral devices.
- **Potential avalanche capability:** when the structure includes a p–n junction (e.g., MOSFET/JFET), devices can be designed and qualified for avalanche (architecture and process dependent).

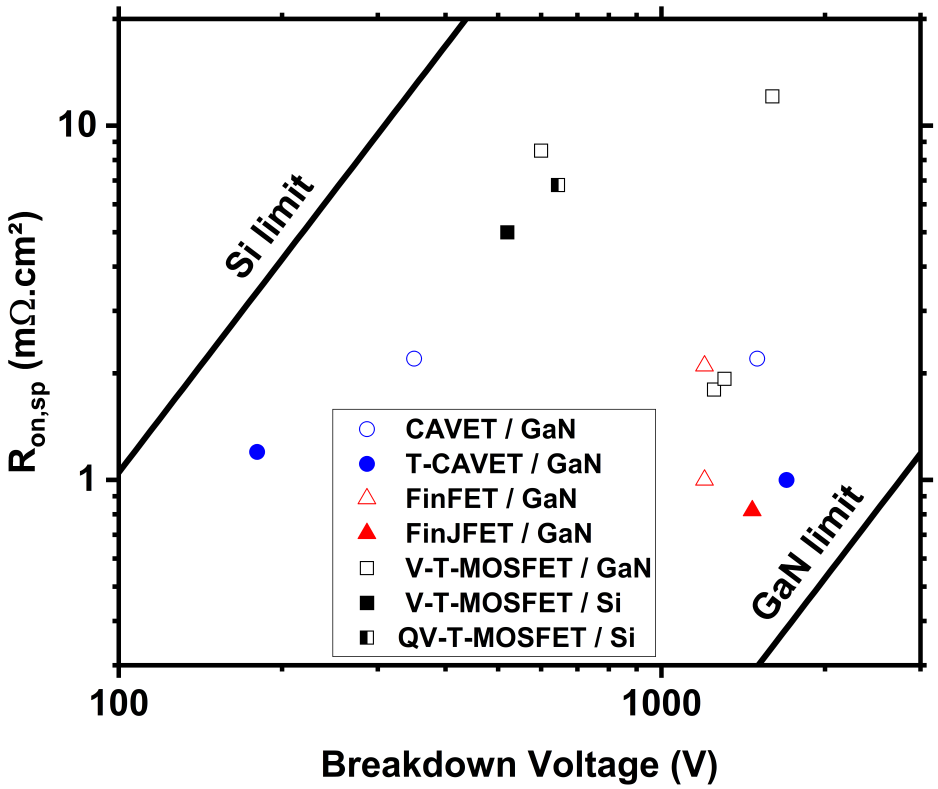


Figure 1.15: Breakdown voltage / specific on-resistance trade-off state-of-the-art of vertical GaN transistors for power applications

Several laboratories pursue vertical GaN transistors such as the Current Aperture Vertical Electron Transistor (CAVET), the Fin Field-Effect Transistor (FinFET), and the Vertical Trench MOSFET (V-T-MOSFET). Their most promising device performances are presented on Figure 1.15 (data from [104–115]). Many record results use GaN-on-GaN substrates due to their low defect density, low-leakage thick drift layers, and straightforward backside contact. However, GaN-on-GaN wafers are costly and historically smaller (4 in; 6 in is emerging [116, 117]), whereas GaN-on-Si enables lower cost and larger diameter at the expense of buffer-related challenges.

To push these structures towards the 1200 V class, key roadblocks include:

- **CAVET:** requires multiple regrowth steps that introduce interface traps (dynamic R_{on}, V_{TH} drift). As a HEMT-type channel, it lacks an intrinsic body diode; avalanche robustness is not inherent and is rarely specified.
- **FinFET:** per-fin current is limited; large devices need many fins, increasing series/interconnect resistance, Q_g, and layout/thermal complexity. Sidewall oxide/interface quality governs mobility and dispersion.
- **V-T-MOSFET:** gate-oxide reliability at trench sidewalls/corners and termination design are critical. On GaN-on-Si, thick low-leakage drift layers are hard to achieve due to stress/bow, which has limited demonstrated BV. In addition, process flows need GaN-specific optimization (not all SiC MOSFET techniques transfer directly).

Commercial vertical GaN today is exemplified by GaN-on-GaN JFETs (e.g., fin-channel eJFETs), not MOS FinFETs. GaN-on-Si FinFETs are being developed primarily for RF applications. Further materials and process maturity (buffer engineering on Si, sidewall/oxide quality, termination, qualification for avalanche/SC) is needed to reach cost- and reliability-friendly manufacturing for 1.2 kV power. While GaN-on-GaN is not ”prohibited”, its wafer cost and diameter currently limit widespread adoption; successful development on Si would address cost and could make vertical GaN a compelling alternative to SiC MOSFETs.

1.3 Applications and market for GaN transistors

Gallium Nitride (GaN) power transistors are increasingly used in modern power electronics due to their high efficiency, fast switching speed, and ability to operate at higher voltages and temperatures compared to traditional silicon-based transistors. One of the most prominent applications of GaN transistors is in power supply systems (or as converters, as a part of a supply system), particularly in data centers, telecommunications infrastructure, and consumer electronics. These devices allow for smaller, lighter, and more energy-efficient power adapters and converters, making them ideal for fast chargers used in smartphones, laptops, and electric vehicles (EVs). GaN’s high-frequency capabilities also reduce the size of passive components like inductors and capacitors, enabling compact and lightweight system designs [118].

Beyond consumer and industrial power supplies, GaN transistors are also used in RF (radio frequency) applications, satellite communication, and radar systems, where their ability to handle high power levels at high frequencies is critical. In automotive and aerospace sectors, GaN devices improve the efficiency and power density of electric drivetrains, onboard chargers, and power distribution units.

Market (devices)	Voltage Range	Current Range	Switching Frequency
Consumer electronics (power supplies - TV, fast chargers)	Up to 650 V	Up to 10 A	100 kHz – 1 MHz
Computing and data centers (power supplies, power converters)	Up to 650 V	Up to 100 A	100 kHz – 500 kHz
EV (power supplies - on-board chargers, traction inverters, LiDAR system)	Up to 900 V	Up to 50 A	50 kHz – 250 kHz
Industry and robotics (power supplies, laser and motor drives)	Up to 600 V	Up to 50 A	100 kHz – 1 MHz
Solar energy (power inverters, power converters - batteries)	Up to 1000 V	Up to 100 A	20 kHz – 100 kHz
RF and Telecommunications (5G, RF power amplifiers)	Up to 100 V	$<$10 A	10 MHz – 100+ MHz
Aerospace and defense systems (radar and warfare system, power converters, pulse modulators)	Up to 600 V	Up to 50 A	100 kHz – 1 MHz

Table 1.3: Applications of GaN power transistors and their typical operating ranges

Additionally, renewable energy systems such as solar inverters and wind turbines benefit from GaN's low conduction and switching losses, which enhance energy harvesting and grid integration. These typical applications and their voltage, current and frequency range are listed in Table 1.3. Data were taken from [119–128]. As the demand for higher performance and energy efficiency grows, GaN power transistors continue to expand their role across a wide range of high-performance and energy-sensitive applications.

Funding for gallium nitride (GaN) research—spanning government, corporate, and venture capital—is rising sharply (Fig. 1.16), driven by a convergence of market demand and strategic urgency. Governments across the U.S., EU, India, and Asia-Pacific have committed significant public R&D resources, capacity-expansion, and commercialization support. In Europe, the ECSEL/Chips Joint Undertaking has launched multiple GaN initiatives, including GaN4AP (budget $\approx$ €64 million [129]) and ALL2GaN ($\approx$ €60 million [130]), along with space-focused projects such as ESGAN and SAGAN. India's Ministry of Electronics & IT funds the Gallium Nitride Ecosystem Enabling Centre & Incubator (GEECI) at IISc to develop a domestic GaN pilot line [131]. In the United States, the CHIPS and Science Act underpin semiconductor research while GlobalFoundries has announced $3 billion in R&D—specifically citing next-generation GaN—within a broader $16 billion U.S. investment plan [132]. Across Asia-Pacific, programmes such as Taiwan's NT$300 billion ($\approx$ $9 billion [133]) Chip-based Industrial Innovation Initiative include GaN as a strategic technology. Private investment is also accelerating: for example, Cambridge GaN Devices closed a $32 million Series C round in 2025 [134], and numerous other start-ups have attracted substantial venture funding worldwide, reflecting strong investor confidence in GaN's growth potential.

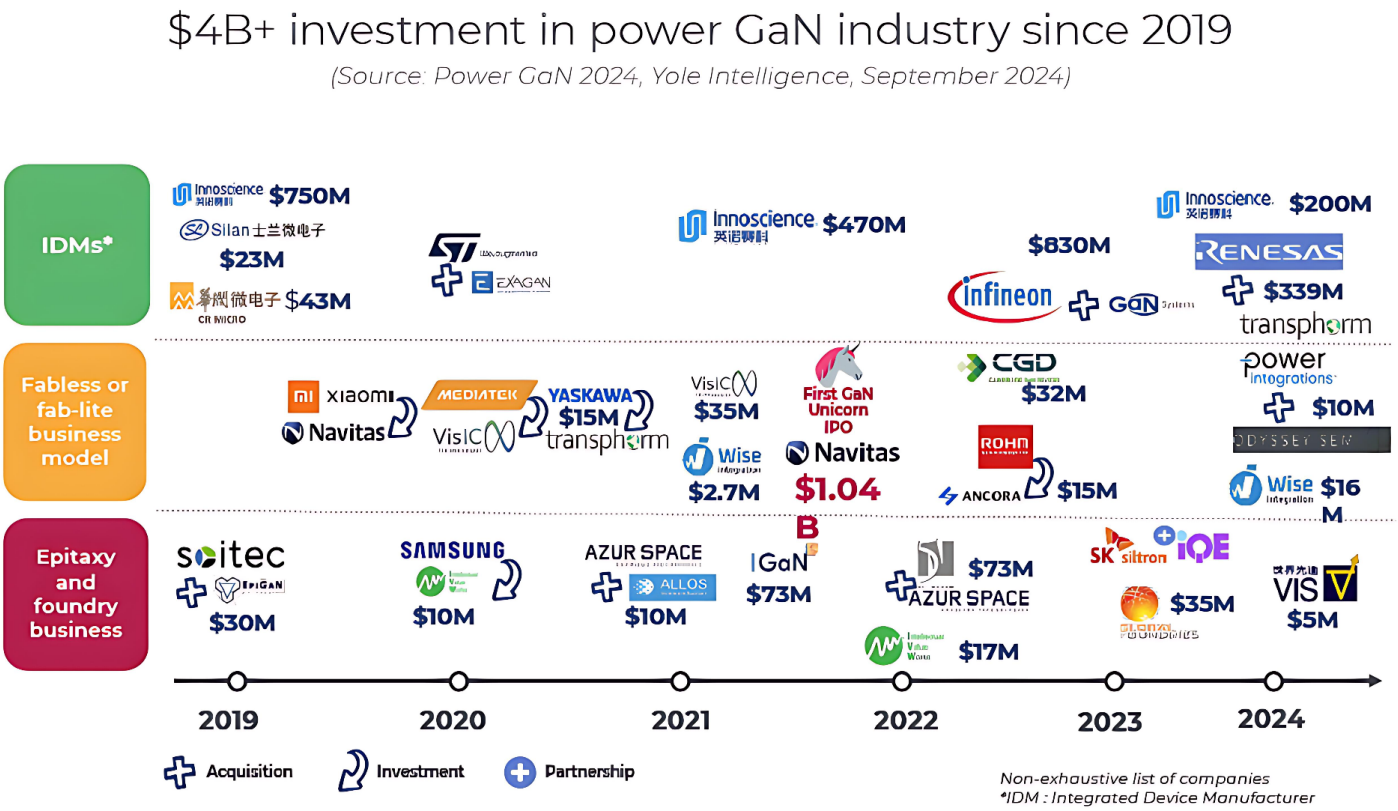


Figure 1.16: Recent investments in GaN research

The Gallium Nitride (GaN) power device market is on a rapid growth trajectory (Fig. 1.17). According to Yole Group's Power GaN 2024 report, the market was about $0.26 B in 2023 and is projected to reach approximately $2.01 B by 2029, implying a ∼41% compound annual growth rate (CAGR) over 2023–2029 [135]. Growth in 2024–2025 remains strong, driven by continued adoption in fast chargers and other consumer-power supplies, with expanding opportunities in data-center and telecom power.

As shown in Figure 1.17, consumer electronics remains the largest segment (∼$1,316 M by 2029; ∼38% CAGR), followed by automotive/mobility (∼$336 M; ∼79% CAGR). Telecom & infrastructure (∼$69 M; ∼60% CAGR), industrial–energy (∼$101 M; ∼35% CAGR), industrial (∼$73 M; ∼19% CAGR), defense & aerospace (∼$66 M; ∼50% CAGR), and others (∼$52 M; ∼57% CAGR) also contribute to the overall expansion [135].

As adoption broadens from consumer to automotive, energy, and defense markets, GaN is evolving from a niche technology into a mainstream enabler of energy-efficient systems. However, for higher-voltage classes (>900 V) and mission-critical domains (EV traction, aerospace, grid), the key bottlenecks remain reliability and trapping phenomena. These challenges, rather than intrinsic performance limits, will determine the pace of GaN's penetration in the multi-kilovolt range, making them the central focus of this thesis.

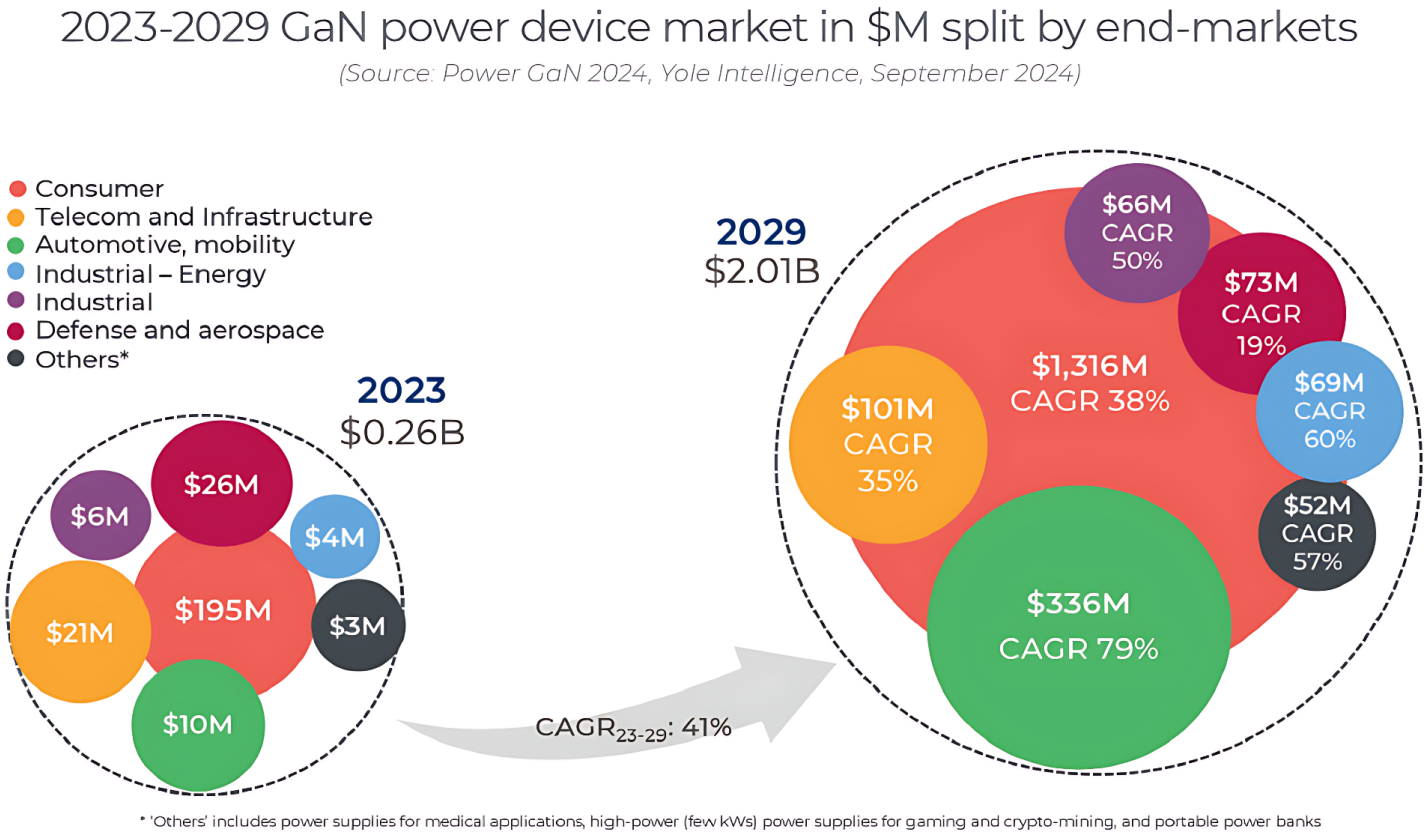


Figure 1.17: GaN power device market overview and forecast (source: Yole Group, Power GaN 2024).

Why Vertical GaN ?

Although lateral GaN HEMTs have successfully entered the 650 V class and are expanding toward 900–1200 V, their architecture intrinsically limits further scalability. In contrast, vertical GaN transistors address several critical challenges and open a path toward true high-voltage applications. The main advantages are:

- Breakdown scalability: In vertical devices, the drift region thickness and doping determine the breakdown voltage. This allows BV to scale into the multi-kilovolt range (>5–10 kV) without proportionally increasing the lateral footprint. Such scaling is essential for traction inverters, grid converters, and other high-voltage domains.
- Thermal path: Vertical conduction spreads heat through the bulk drift layer into the substrate, enabling efficient heat extraction via a thinned, metalized backside. This architecture provides a more favorable thermal resistance compared to lateral HEMTs, where heat is concentrated near the surface and must be dissipated laterally.
- Trap immunity: Because the highest electric fields are confined in the bulk drift region rather than

near the surface, vertical devices are intrinsically less sensitive to surface and interface traps. This reduces dynamic Ron degradation, current collapse, and threshold-voltage instabilities—issues that remain the primary reliability bottlenecks in lateral HEMTs.

- Industrial need: While lateral GaN addresses fast-switching at 650 V, vertical GaN is required to compete with SiC MOSFETs in the 1200–3300 V range that dominates EV traction, renewable energy, and grid-scale power conversion. Achieving reliable, cost-effective vertical GaN devices would allow GaN to complement and potentially displace SiC in these high-power markets.

Conclusion

This chapter traced the trajectory of power electronics from early rectifiers and vacuum tubes to silicon BJTs, MOSFETs, and IGBTs, and, finally, to wide-bandgap semiconductors. Each inflection point was driven by concrete application needs: higher efficiency, switching speed, voltage and current capability, thermal robustness, and manufacturability. Silicon devices established the foundations of modern conversion, yet their physical properties ultimately expose efficiency and frequency limits that constrain further system miniaturization.

Wide-bandgap materials address these limits at their root. SiC vertical MOSFETs have demonstrated how larger critical electric fields and superior thermal properties translate into practical high-voltage, high-efficiency operation. GaN extended the paradigm by enabling extremely fast switching via polarization-induced 2DEGs in lateral HEMTs, unlocking compact, MHz-class conversion at $\sim$ 650–1200 V. However, reliability rather than intrinsic figures of merit is the dominant barrier to broader GaN deployment at higher voltages.

On this basis, Chapter 2 focuses on the design, simulation, and experimental assessment of $\sim$ 1.2 kV-class lateral GaN HEMTs, with particular attention to buffer/back-barrier engineering. With the subsequent objective of reporting them onto a thermally favorable substrate such as AlN or ”dummy-grade” SiC, the processed epitaxies were optimized on sapphire. Chapter 3 then turns to vertical GaN trench MOSFETs, outlining the device architecture and termination strategies, and reporting the first process developments toward robust high-voltage operation.

Chapter 2

Heterogeneously Integrated GaN HEMTs towards 1.2 kV Class

2.1 Introduction and Objectives

GaN HEMTs can be extended to the 1.2 kV regime if three architectural changes are made at once. Current limitations include:

- **Stress management in epitaxy:** The large lattice and thermal-expansion mismatch between GaN and Si requires thick (typically a few to several µm) buffer stacks (AlN nucleation, graded AlGaN, or AlN/GaN superlattices) to prevent cracking and reduce defect density. This adds MOCVD time and cost and can introduce wafer bow and increased trapping.
- **Limited heat removal on Si:** In lateral GaN-on-Si HEMTs the dominant heat path is downward through the Si substrate and package. Silicon's moderate thermal conductivity ($\approx 1.5\,\mathrm{W\,cm^{-1}\,K^{-1}}$) and package interfaces limit junction cooling. The top side contributes little due to thin passivation/metal layers and isolation constraints.
- **Short short-circuit withstand time (SCWT):** Often in the hundreds of ns to $\sim$1–2 µs range for many e-mode 650 V devices [136], versus a few µs for typical SiC/Si MOSFETs [137] and $>$10 µs for IGBTs [138]. Limited SCWT primarily arises from high short-circuit current (weak current saturation), localized heating at the gate/drain edge with finite transient thermal capacity, and gate-stack stress (electro-thermal degradation under high field and temperature).

The objective of this chapter is to present the optimization (simulation, fabrication and electrical characterization) of GaN HEMTs structure on sapphire and investigate (simulations) an approach addressing

these challenges at once: a spalling-based transfer of high-quality GaN-on-sapphire HEMT films onto a semi-insulating 4H-SiC carrier through bonding. A careful use of the bonding step to impose beneficial residual stress for mobility and threshold tuning; and a compact, intrinsic current limiter in the source access region that caps short-circuit current at a controlled multiple of the rated value while introducing only a modest conduction penalty. The quantitative objectives translate as follows: the transferred device should block more than 1.6 kV in off-state tests across a spread of gate–drain spacings to ensure that margin exists in the field-plated, packaged product. The target static on-resistance is approximately $40\,\mathrm{m\Omega}$ at 1.2 kV and tens of amperes, which is the territory occupied by commercially available silicon carbide transistors. The device should survive a hard short-circuit pulse of at least ten µs at the rated bus, with post-pulse parameter drift below 10%.

(1) Substrate transfer to a high-κ, insulating carrier. The starting point is a gallium nitride HEMT epitaxial stack grown on sapphire rather than on silicon. Sapphire is chosen for two reasons. It allows high electron mobility and a high quality interface in the channel while maintaining insulating behavior in the substrate, which simplifies off-state leakage models and device isolation. It also decouples the epitaxy from the thermal expansion mismatch with silicon wafers. The wafer is processed to the point where large area HEMTs can be defined. AlN ($\kappa \approx 2.8\,\mathrm{W\,cm^{-1}\,K^{-1}}$) was initially considered as the substrate, but a semi-insulating ("dummy-grade") SiC carrier ($\kappa \approx 4.9\,\mathrm{W\,cm^{-1}\,K^{-1}}$) was selected. Compared with Si, this carrier lowers thermal resistance and reduces self-heating during short circuit, supporting a longer SCWT. It also mitigates buffer-to-substrate leakage and raises the vertical breakdown limit that often constrains GaN-on-Si HEMTs [139, 140].

To transfer the epitaxy onto SiC, mechanical spalling (also called controlled spalling), a mechanical lift-off technique can be used. First demonstrated for kerf-less removal of thin crystalline layers from expensive Ge substrates in 2012 [141],enabling their reuse. The method consists of initiating and guiding a crack parallel to the wafer surface at a controlled depth, typically using a tensile-stressed metal "stressor" layer (often Ni) so that the device film is released intact. The spalled layer are then bonded to a new substrate and the metal tensor layer is removed (see Fig. 2.1). The approach was subsequently adapted to GaN-on-Si [142] and GaN-on-sapphire [143]. To improve crack initiation and control, a van der Waals (2D, weakly bonded) release interlayer is often inserted beneath the epitaxial stack, typically hexagonal BN [144] or graphene [145]. Recently, Snure et al. reported successful spalling of GaN from 4-inch sapphire substrates [146], supporting the feasibility of the project.

(2) Local source–gate access engineering. By intentionally reducing the 2DEG density in a short source–gate access segment (via light implantation or barrier thinning), the local sheet resistance increases (even if mobility improves slightly). With proper sizing, this creates a controlled injection bottle-

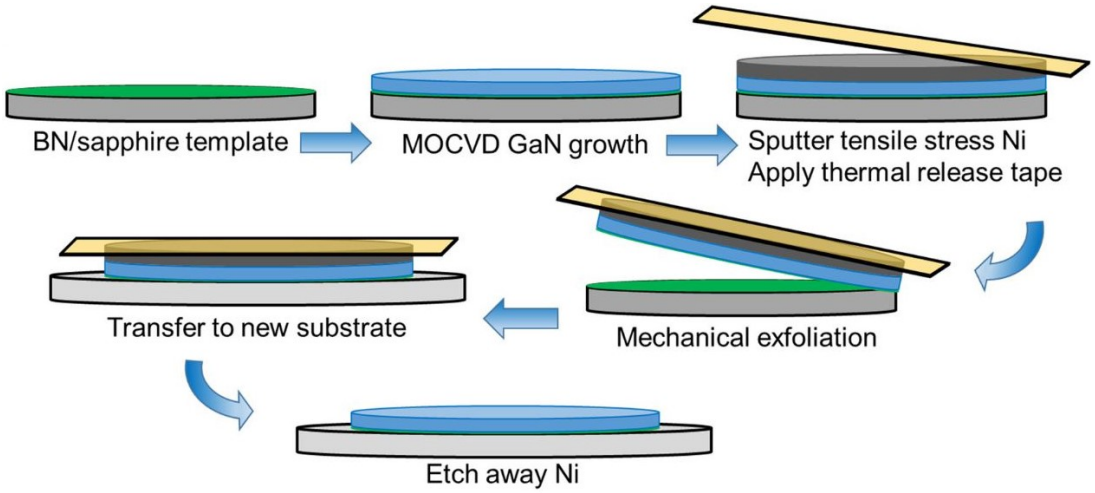


Figure 2.1: Schematics of the steps of controlled spalling

neck that clamps the short-circuit current (targeting $\sim$3–4$\times$ the rated current), curbing heating during a fault and thereby increasing SCWT. The trade-offs are a small increase in $R_{\mathrm{on,sp}}$ and some reduction of $I_{\mathrm{D,max}}$. The self-heating rate during the first µs of the fault is thereby reduced. Coupled with the superior thermal path into a more thermally favorable substrate, such as AlN or silicon carbide, this change in the time derivative of temperature is sufficient to cross the 10 µs threshold for survivability even if protection circuits act on a µs scale rather than in a few hundred ns.

In the following sections, we introduce the Silvaco Technology Computer-Aided Design (TCAD) environment used at the outset of the project. The goal was to anticipate the impact of transferring GaN HEMTs onto AlN substrates (substrate initially chosen at the start of the project, i.e. at the time of the simulations) with varying material quality and thermal conductivity on on-state performance, and to evaluate how alternative buffer configurations affect the off-state behavior. Based on these simulations, four device structures were selected for fabrication and testing at IEMN. After electrical characterization, additional simulations were carried out to refine the design, focusing on the role and composition of the back-barrier and on how the buffer carbon concentration influences the off-state behavior of the transistors. These simulations are presented together with the fabrication process and the electrical characterization of the HEMTs.

2.2 Preliminary work : TCAD simulations with Silvaco

It is possible to preview the behavior of electrical components with the help of dedicated TCAD software. The most widely used in the industry are Sentaurus and Silvaco. In this work, Silvaco software was used. Here, I will present the main features of this software, the physical models chosen to simulate

HEMTs and the results obtained for transistors reported on AlN or on sapphire with variations in their structures.

2.2.1 Structure design : meshing and doping

To predict the behavior of a component, Silvaco solves a set of 3 (by default) semiconductor physics equations: the carrier continuity equation (Eq. 1.1), the drift-diffusion law (Eq. 1.2) and Poisson's law (more accurate version of Gauss's law - see Eq. 1.4), by using a resolution algorithm. It calculates the electrostatic potential (ϕ), the electric field (E), the carrier densities (n and p), the current densities (J_{n} and J_{p}) and the electrodes current (I_{G}, I_{S} and I_{D}).

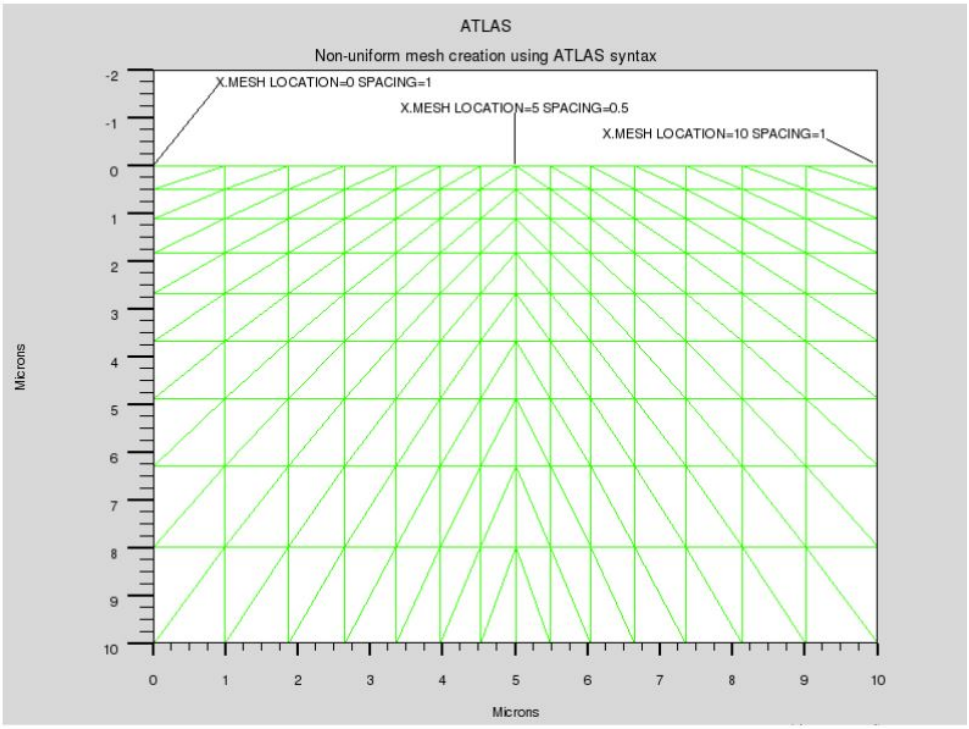


Figure 2.2: Example of a meshing with Silvaco

The aforementioned equations use scalar value (e.g. electron concentration) and vector (e.g. the electric field). However the software does not calculate these values on (or between) regularly spaced point(s) like an an orthonormal frame. A specific grid, called a meshing, must be defined for each structure to simulate.

To do so, the software needs a list of coordinates and spacing values along the X (and Y) axis. It will add a line perpendicular to the X (or Y) axis at each location and will fill the grid with lines separated by the spacing value (e.g., imposing a vertical line at x=0 µm with a spacing of 0.5 µm, it will add vertical lines at x=0.5 µm, x=1.0 µm, etc.). If the spacing values given are different between the imposed lines,

the spacing will gradually evolve between the locations. Figure 2.2 shows examples of a 10 x 10 µm mesh with imposed vertical lines at x=0, 5, and 10 µm with spacings of 1, 0.5, and 1 µm, respectively. The imposed horizontal lines are at y=0 µm and y=10 µm with spacings of 0.5 µm and 2 µm, respectively.

Silvaco creates one diagonal line in each rectangle thus formed and calculates scalar values at every line intersection and vectors along each line of the mesh. Increasing the number of lines leads to more accurate results (to a certain extent) but much longer calculation time. Also, the efficiency of the solving algorithm strongly depends on the meshing density : it is recommended to increase the number of points in areas where the values (electric field, current density,etc.) vary rapidly in order to ease resolution. In the upcoming results, meshing was optimized for each on-state and off-state simulation to obtain accurate results without sacrificing too much calculation time.

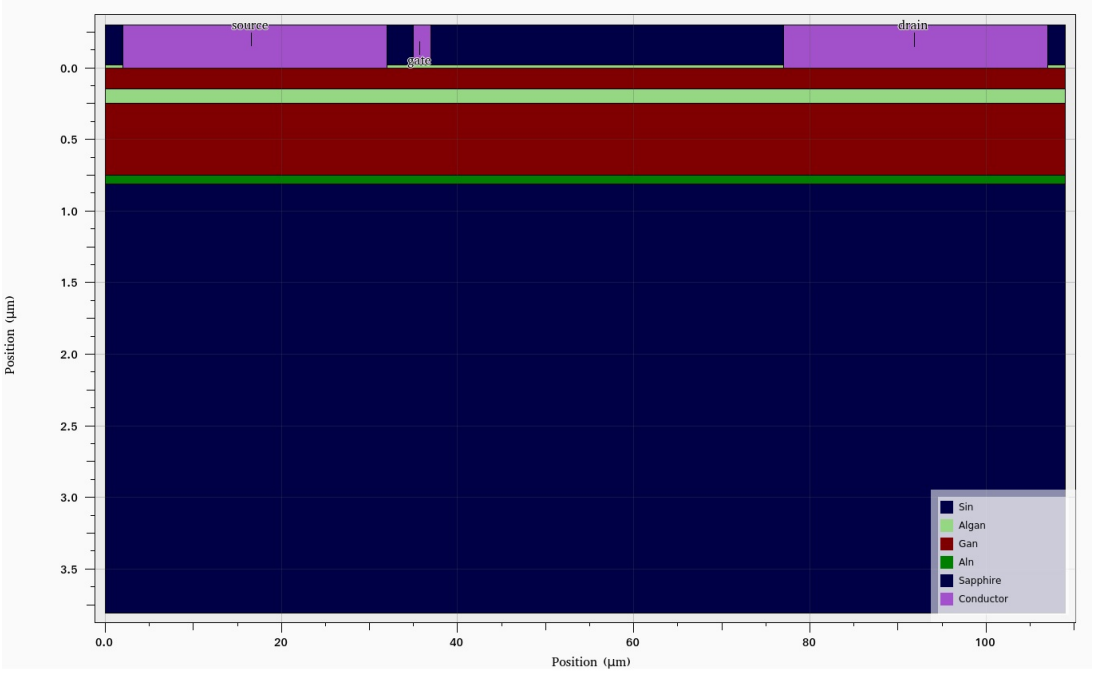


Figure 2.3: Example of a basic HEMT structure on sapphire (mesh is not displayed for a better readability)

After defining the mesh, each region must be specified by four vertices (forming either a trapezoidal or rectangular shape) together with the material from which it is composed. Most materials, including GaN and AlN, have their physical parameters (such as thermal conductivity, electron mobility, and bandgap) already included in the default Silvaco database. Nevertheless, it is possible to define a new material from scratch or to modify the parameters of existing ones.

By default, materials are undoped, and the doping of each region must be explicitly defined, including the doping type, concentration, dopant distribution, and related properties. If the dopant species act as recombination centers or traps, additional information must be provided, such as the energy level within

the bandgap and the degeneracy factor. These parameters are not available in the default database and must be specified for each structure.

Electrodes are defined in the same way as regions (by four vertices) except that, if the electrode material is absent from the default database, an electron affinity value may be assigned in place of the material.

Once the mesh, regions, doping profiles and electrodes have been defined, a basic structure is obtained and is ready for electrical simulation (Fig. 2.3). However, only a limited set of equations is used to compute solutions by default. To achieve more physically accurate results, it is essential to select and enable the appropriate physical models.

2.2.2 Physical models chosen

Silvaco offers many physical models that can be activated to take into account various physical phenomena, from light absorption to trap-assisted tunneling leakage. It is important to understand the physics occurring in the device to be simulated and to enable the closest corresponding models in Silvaco. Here, I will present the chosen model for the GaN HEMT.

Mobility

The mobility model enabled by default in Silvaco is very simple:

$$\mu_{\mathrm{n}} = \mu_{0,\mathrm{n}} \left(\frac{T}{300} \right)^{-T_{\mu,\mathrm{n}}} \tag{2.1}$$

- μ_{n} is the electron mobility,
- $\mu_{0,\mathrm{n}}$ is a definable parameter (1000 by default for electron and 500 for holes),
- $T_{\mu,\mathrm{n}}$ is a definable parameter (1.5 by default for both carriers),

Equation 2.1: Default model for electron mobility in Silvaco

It only takes into account the temperature, but not the electric field or the doping concentration. To replace this model, I used two complementary equations: the Albrecht equations and the Gansat model. They enable new calculations for mobility at low and high electric fields, respectively.

Their equations (Eqs. 2.2 and 2.3) include the doping and the electric field to provide a more accurate description of electron behavior. The low-field equation was established (by experimental data fitting) by Albrecht et al. specifically for GaN [147] whereas the Gansat model was developed for all nitrides

using Monte Carlo simulation [148] (another software tool, more oriented toward fundamental physics simulation).

$$\mu(N,T) = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N}{N_{\text{ref}}}\right)^{\alpha}} \left(\frac{T}{T_0}\right)^{\beta} \tag{2.2}$$

$$v(E) = \frac{\mu_0 E}{\left[1 + \left(\frac{\mu_0 E}{v_{\text{sat}}}\right)^{\beta}\right]^{1/\beta}} \tag{2.3}$$

- $\mu(N,T)$ is the carrier mobility, with T the temperature and N the associated doping concentration,
- $\mu_{\max}, \mu_{\min}, \alpha, \beta$ and T_0 are definable parameters,
- $v(E)$ and v_{sat} are the electron drift and saturation velocity, respectively,
- μ_0 is the low-field mobility and E the electric field,

Equation 2.2 and 2.3: simplified equations of the Albrecht and Gansat models in Silvaco

Activating these models does not slow down the convergence of the algorithm, so both were used for all simulations.

Polarization

To create a two-dimensional electron gas (2DEG) in a HEMT structure using Silvaco, several approaches are available. One option is to modify the interface between two layers to introduce a sheet of electrons and adjust the electron mobility in the channel layer. However, this method is not the most physically rigorous. Instead, Silvaco provides a dedicated model to calculate strain-induced polarization in wurtzite structures, based directly on the equations introduced in Chapter 1 (Eqs. 1.8 to 1.12). The lattice parameters of individual layers can be modified if necessary, although this is generally not required for GaN and AlGaN, since Silvaco provides reliable default values for these materials. A polarization coefficient is also available (with a default value of 1) and can be adjusted to fine-tune the 2DEG properties for better agreement with experimental data. Finally, by enabling the option to display interface charge, the formation of the 2DEG can be visualized within the Silvaco structure (see Fig. 2.4).

Carbon doping

In our HEMT structures, a carbon-doped GaN buffer is employed as a semi-insulating layer. Correctly defining the traps and their behavior is crucial to obtaining physically sound off-state simulations. The

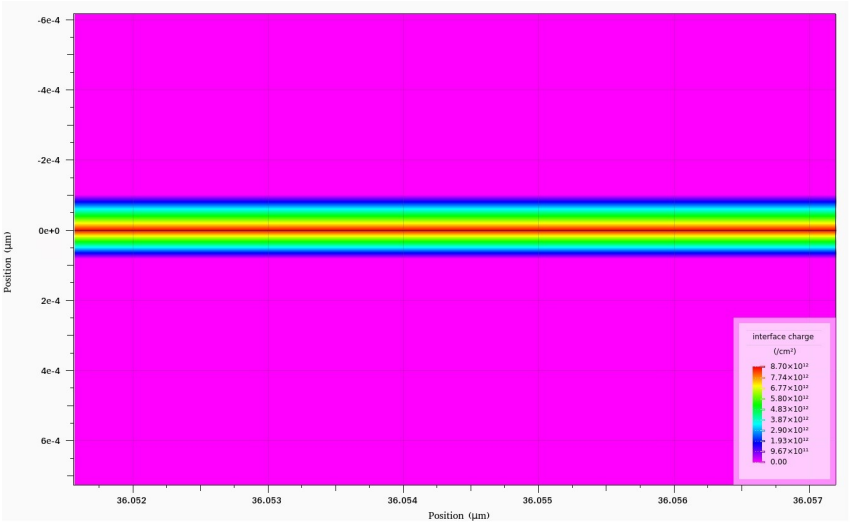


Figure 2.4: 2DEG observation on a Silvaco structure

insulating nature of carbon-doped GaN originates from acceptor traps created when carbon atoms substitute nitrogen atoms in the crystal lattice (C_N).

The reported energy level of these traps varies slightly in the literature, but the most widely accepted value is 0.9 eV above the valence band [149, 150] (i.e., 2.53 eV below the conduction band, given the GaN bandgap of 3.43 eV). This value was adopted in all simulations. These deep-level traps capture background donors naturally present in unintentionally doped GaN (due to residual impurities), thereby reducing its conductivity. Furthermore, because the acceptor level lies deep within the bandgap, it does not easily release holes into the valence band and therefore does not contribute to p-type conductivity, explaining the semi-insulating behavior of C-doped GaN.

However, introducing a high concentration of carbon also generates donor traps, which partly compensate the acceptor states [151]. Specifically, carbon can substitute gallium atoms in the lattice (C_{Ga}), forming donor states with energy levels around 0.2 eV below the conduction band minimum [149, 150]. In the present simulations, the donor state level was fixed at 0.2 eV below the conduction band (see Fig. 2.5).

During epitaxial growth, both types of traps form competitively, and their relative proportions depend on the specific growth conditions [152]. Several studies have attempted to quantify this ratio under standard MOCVD growth conditions, typically reporting C_{Ga} concentrations between 50% and 80% of the C_N concentration [153–155], with the proportion of C_{Ga} increasing as the total carbon concentration rises [153]. In the present simulations, the proportion of C_{Ga} was adjusted consistently with the total carbon doping level.

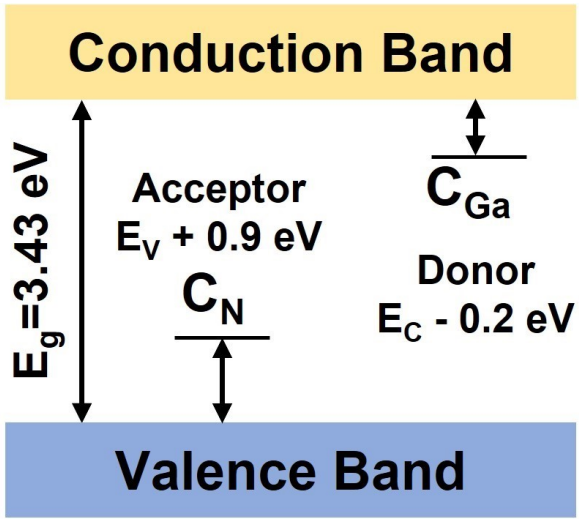


Figure 2.5: Schematic of the carbon-related acceptor and donor levels in the GaN bandgap

Leakage model

Several leakage mechanisms can occur in HEMTs, including buffer conduction (under very high vertical electric fields), gate leakage (dependent on gate technology), surface leakage (dependent on passivation), dislocation-related conduction (in high-defect-density epitaxies), and trap-assisted tunneling (TAT), among the most common [119, 140, 156].

In the following simulations, buffer conduction was neglected since the HEMT structures were grown on sapphire, an insulating substrate. Gate and surface leakage were also ignored, as they remain constant across structures fabricated using the same process. Moreover, enabling the corresponding Silvaco models for these mechanisms significantly reduces convergence speed and probability. Although the software includes a dislocation conduction model, known as the variable-range hopping (VHOP) model, it was not activated because the dislocation density in the structures was unknown. In addition, VHOP substantially slows convergence and often prevents successful resolution.

For the off-state simulations, only the trap-assisted tunneling model (TRAP.TUNNEL) was enabled, as TAT is considered the dominant leakage mechanism in our structures due to its dependence on the buffer. For the on-state simulations, the standard Shockley–Read–Hall (SRH) recombination model was activated.

$$R_{\mathrm{TAT}} = \frac{np - n_i^2}{\tau_p \left(n + n_1\, e^{-\frac{E_{\mathrm{trap}}}{kT}}\right) + \tau_n \left(p + p_1\, e^{-\frac{E_{\mathrm{trap}}}{kT}}\right)} \tag{2.4}$$

$$J_{\mathrm{TAT}} = q \int R_{\mathrm{TAT}}(x)\ \cdot dx \tag{2.5}$$

- R_{TAT} and J_{TAT} are the tunneling transition rate and current density, respectively,
- n, p and n_i are the electrons, holes and intrinsic carriers concentration, respectively
- τ_n and τ_p are the electron and holes lifetimes,
- E_{trap} is the difference between the trap energy level and the intrinsic Fermi level,
- n_1 and p_1 are the SRH equilibrium concentrations,
- k and T are the Boltzmann constant and temperature respectively,

Equation 2.4 and 2.5: Equations for the tunneling rate and current density in Silvaco (with the TRAP.TUNNEL model)

Since the model requires capture cross-section values (to calculate the carrier lifetimes τ_n and τ_p) for the defined traps, a value of $1 \times 10^{-15}\,\mathrm{cm}^2$ was adopted from the literature [154] for both carriers (electrons and holes) and for both trap types (C_N and C_{Ga}).

After selecting the models to be activated and defining all necessary parameters, two series of simulations were performed.

2.2.3 Simulations

Initial objective envisioned bonding onto AlN substrate. Accordingly, early in the project, a first series of simulations was carried out to evaluate different bonding solutions on AlN and their impact on the device performance. The reference structure for these simulations was taken from literature on high-power HEMTs [157]. Later, the decision was made to transfer the epitaxial structure onto SiC instead, while optimizing them on sapphire. Four different epitaxies (Fig. 2.14) were selected for an initial fabrication run (see Section 2.3) to asses the impact of the buffer and back barrier on the off-state behavior of HEMTs. Additional simulations were then performed based on experimental results, to better predict device behavior and potentially optimize these structures.

Reference structure

To assess the impact of individual parameters, a reference structure must first be defined, and its properties implemented in Silvaco as a baseline before varying any parameter. For this purpose, I reproduced the high-power GaN-on-Si HEMT described in a previous PhD thesis from our group [157] (see Fig. 2.6).

The reference epitaxy consisted of a step-graded, undoped AlGaN buffer to accommodate the silicon substrate. On top of this buffer, a semi-insulating C-doped GaN layer with a thickness of 2.6 µm and

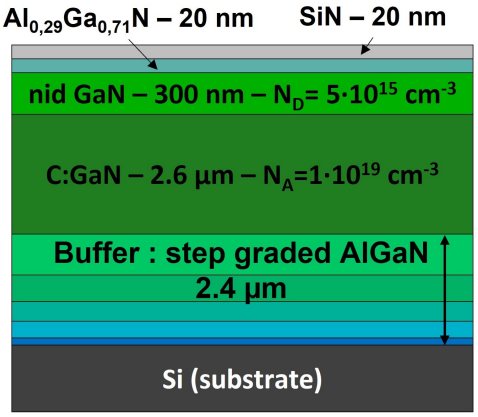


Figure 2.6: Epitaxy chosen for the reference structure

a carbon concentration of $1 \times 10^{19}\,\mathrm{cm}^{-3}$ was included. The channel consisted of a 300 nm GaN layer, while the barrier was a 20 nm AlGaN layer with 30% aluminum content. The gate-to-drain and gate-to-source distances were 15 µm and 5 µm, respectively, with a Schottky gate width of 1.5 µm. The results reported in the thesis were successfully reproduced (Fig. 2.7 - I_D-V_{GS} curves both showed threshold voltages V_{TH} at -14 V).

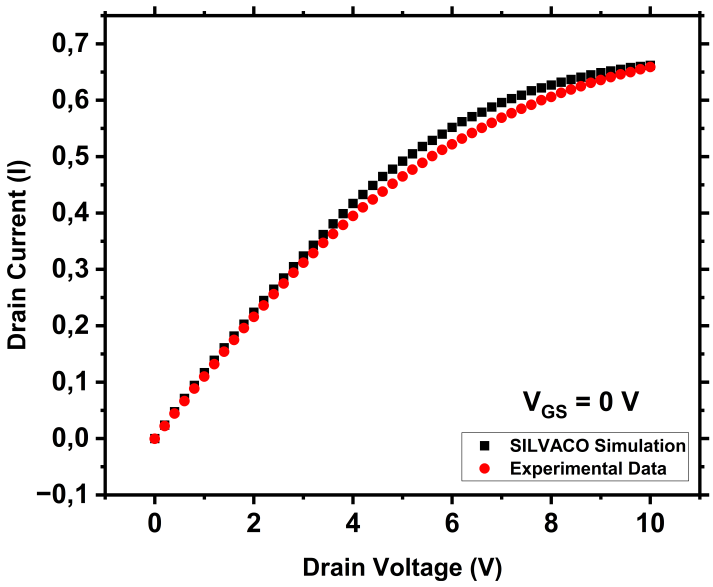


Figure 2.7: I_D-V_{DS} characteristics of the reference structure compared to the experimental data

Testing bonding solution

To transfer our GaN epitaxy onto a different substrate, a bonding method is required. Several approaches can be employed to attach an exfoliated epitaxy to a substrate, including metallic bonding (e.g., Au, Cu, eutectic), oxide bonding (SiO_2), or nitride bonding (SiN) [158].

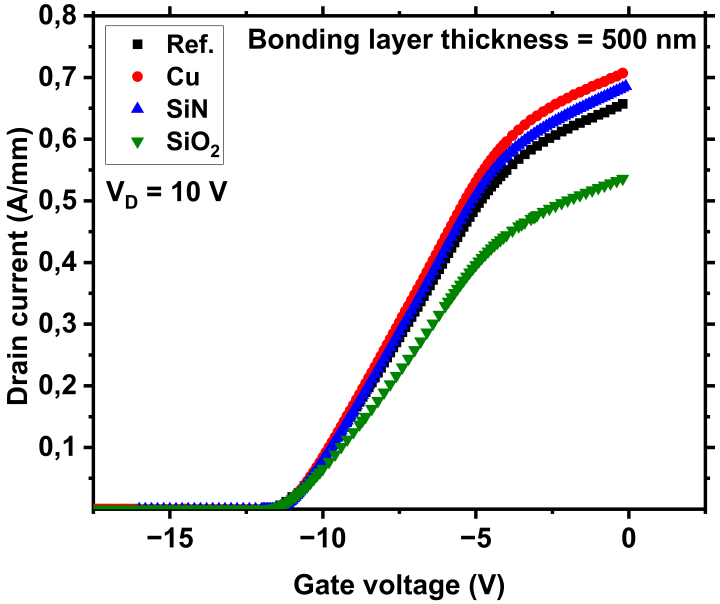


Figure 2.8: I_D-V_{GS} simulations for various bonding layer materials (thickness fixed at 500 nm)

I began my simulations by evaluating the impact of the bonding method on the hypothetical current gain of HEMTs bonded to an AlN substrate. For this purpose, a 500 µm bonding layer was inserted between the step-graded AlGaN buffer and the AlN substrate. Three bonding materials were tested: SiO_2, SiN, and Cu. The corresponding I_D-V_{GS} curves are shown in Figure 2.8

The results indicate a reduction in output current with the silicon dioxide bonding layer, decreasing from 0.657 to $0.536\,\mathrm{A\,mm^{-1}}$ (an 18% loss). A modest improvement of $\sim$ 4% was observed with the SiN layer, while the copper layer provided the largest benefit, with an output current increase of 8%.

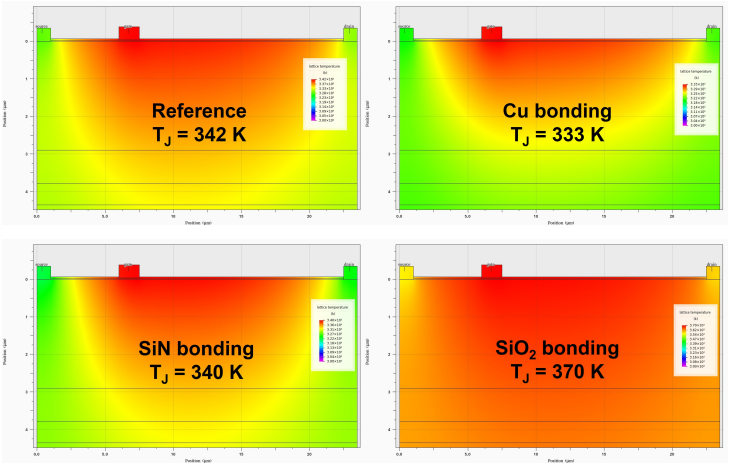


Figure 2.9: Device temperature at V_{DS} = 10 V for all bonding materials

These results can be attributed to the thermal conductivity and heat capacity of the bonding materials, which determine the efficiency of heat transfer to the AlN substrate. To validate this assumption, the drain

voltage was increased to 10 V and the junction temperature was monitored (see Fig. 2.9).

The recorded temperatures were consistent with the current values: a hotter 2DEG corresponds to a reduced drain current. To verify that the current reduction was primarily caused by self-heating, the reference structure was artificially heated to 370 K. The simulated ID–VGS curve at this temperature matched the curve obtained with the SiO_2 bonding layer, confirming the thermal origin of the effect.

Finally, the impact of bonding layer thickness was investigated. Additional simulations were carried out with SiO_2 bonding layers of 10, 50, and 100 nm. The corresponding results are presented in Figure 2.10.

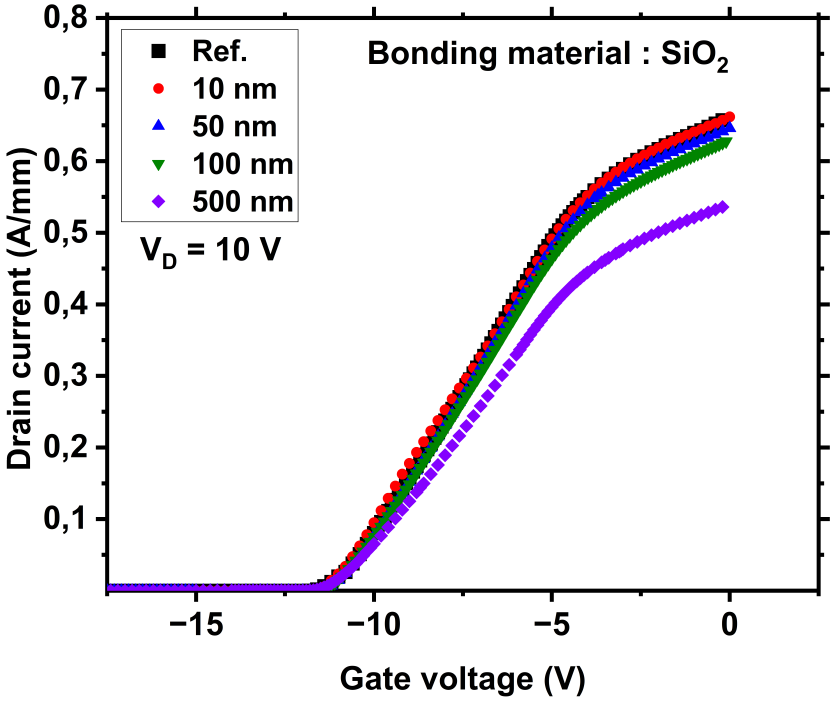


Figure 2.10: Simulation with a SiO_2 bonding layer of various thicknesses

It can be observed that the reduction in output current is significantly mitigated when the bonding layer is thinned. However, the current never fully recovers to the value obtained with the reference structure. This behavior is again correlated with the device temperature (see Fig. 2.11).

These results demonstrate that, in addition to the intrinsic properties of the bonding material, the thickness of the bonding layer plays a critical role in heat propagation toward the AlN substrate. Based on these simulations, the most suitable options for bonding our spalled epitaxies appear to be either a thin ($\leq$ 100 nm) SiN layer or a copper layer.

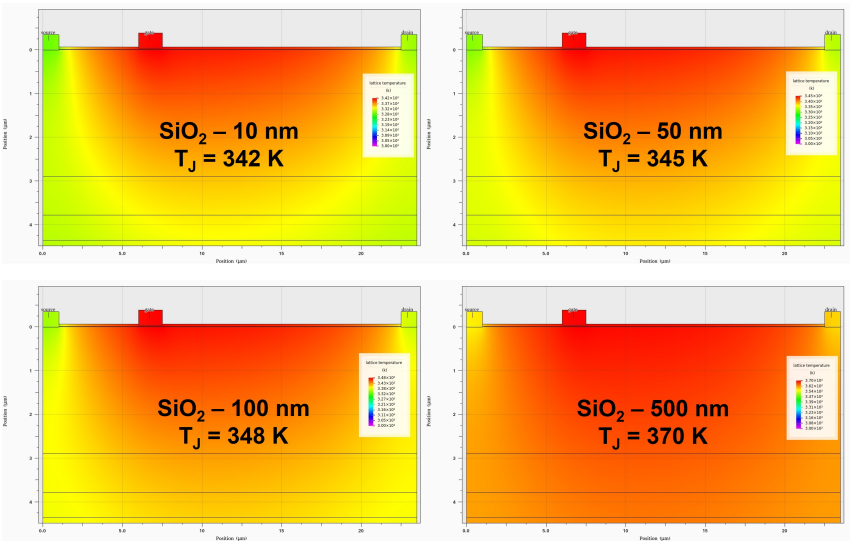


Figure 2.11: Device temperature at V_{DS} = 10 V for all SiO_2 thickness

Impact of the carbon doped GaN buffer configuration

Before selecting a definitive stack for the HEMTs, three different C-doped GaN semi-insulating buffers were simulated (with all other parameters kept identical) to evaluate their impact on off-state performance. Figure 2.12 illustrates the three buffer configurations tested: (i) a 1 µm carbon-doped GaN layer, (ii) a 2.5 µm carbon-doped GaN layer, and (iii) two 1 µm carbon-doped GaN layers separated by 0.5 µm of unintentionally doped (nid) GaN.

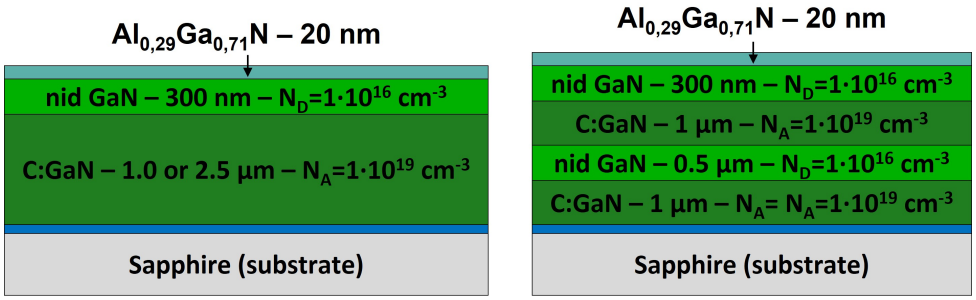


Figure 2.12: Schematics of the epitaxies tested with different buffers

As shown in Figure 2.13, the off-state simulations revealed that introducing a nid GaN layer increased buffer leakage and reduced the breakdown voltage. A slight improvement in breakdown voltage was observed when the C-doped layer thickness was increased; however, thickness did not appear to be a dominant factor in determining the breakdown voltage. Four epitaxial stacks were then defined for experimental validation with fabricated HEMTs (see Fig. 2.14). Structures A and B incorporate a thin (500 nm) highly carbon-doped GaN buffer with a carbon concentration of $1 \times 10^{19}\,\mathrm{cm}^{-3}$. Structures C and D, in contrast, employ a thicker (2.0 µm) bi-layer buffer consisting of a 1 µm moderately iron-doped

GaN layer ($1 \times 10^{18}\,\mathrm{cm}^{-3}$, with iron also acting as a semi-insulating dopant) beneath a 1 µm C-doped GaN layer with a reduced carbon concentration of $6 \times 10^{18}\,\mathrm{cm}^{-3}$).

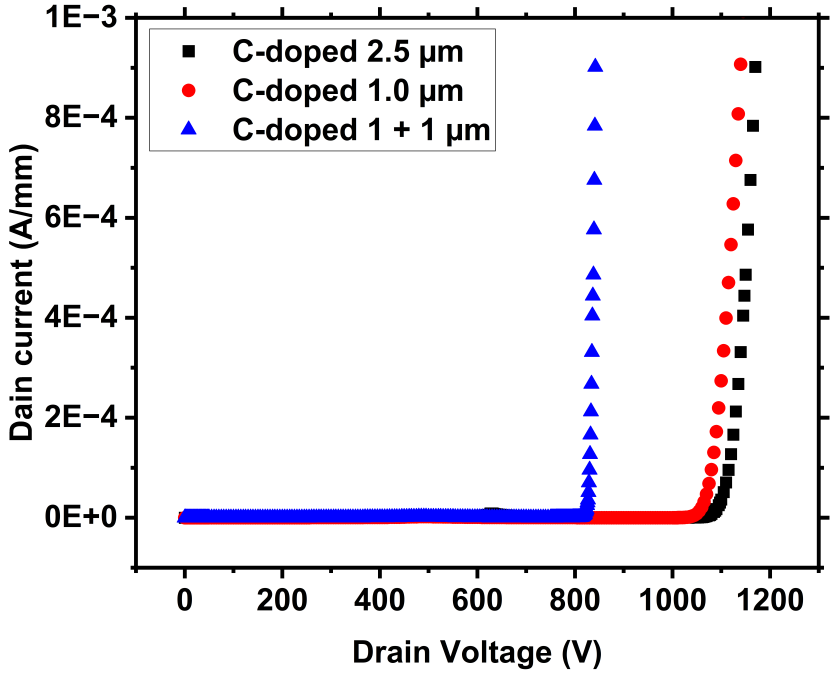


Figure 2.13: Breakdown voltage simulation of the structure shown in Figure 2.12

After this series of simulations, the decision was made to optimize our HEMTs epitaxy on sapphire, owing to the GaN superior quality, prior to reporting on AlN or dummy-grade SiC substrates. Consequently, the subsequent simulations were performed using GaN-on-sapphire stacks. To further enhance electron confinement in the top layer, a back barrier, implemented as a thin AlGaN layer, can be added above the semi-insulating buffer. Such back barriers have been investigated in the context of RF HEMTs [159, 160], but their impact on breakdown voltage has not been extensively studied, since this parameter is not critical for RF devices. To assess their effect on the off-state behavior of power HEMTs, a 100 nm back barrier with 6% aluminum content was introduced into structures A and C.

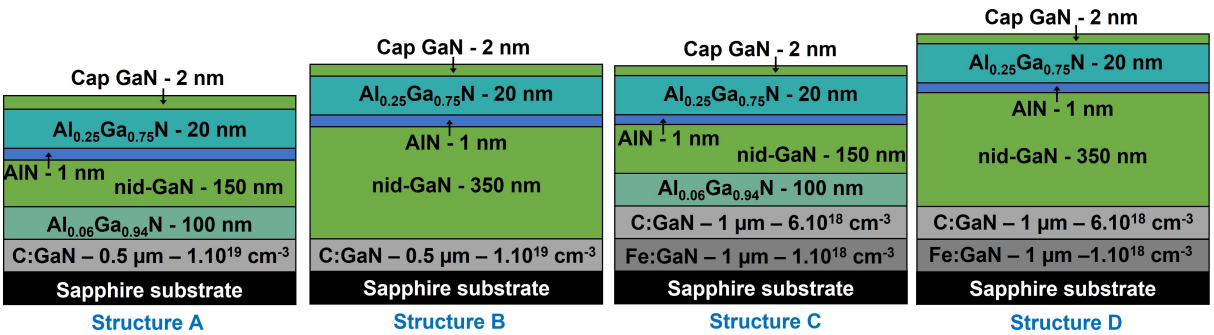


Figure 2.14: Schematics of the tested structures

Schematics of all tested structures are presented in Fig 2.14. HEMTs were then fabricated based on these epitaxial stacks (see Sections 2.3 and 2.4). The results obtained for structure A were used as a reference for a new series of simulations.

Impact of the carbon doping concentration in the semi-insulating GaN buffer

To better interpret the results obtained in Section 2.4and further optimize our HEMTs, two parameters were investigated: the carbon concentration in the buffer and the aluminum content in the back barrier. Structure A was reproduced in Silvaco, and the physical models were calibrated accordingly. The carbon concentration in the buffer was then varied from $1 \times 10^{17}\,\mathrm{cm}^{-3}$ to $1 \times 10^{19}\,\mathrm{cm}^{-3}$ (reference), while keeping the same back barrier for all cases. The breakdown simulation results are presented in Figure 2.15.

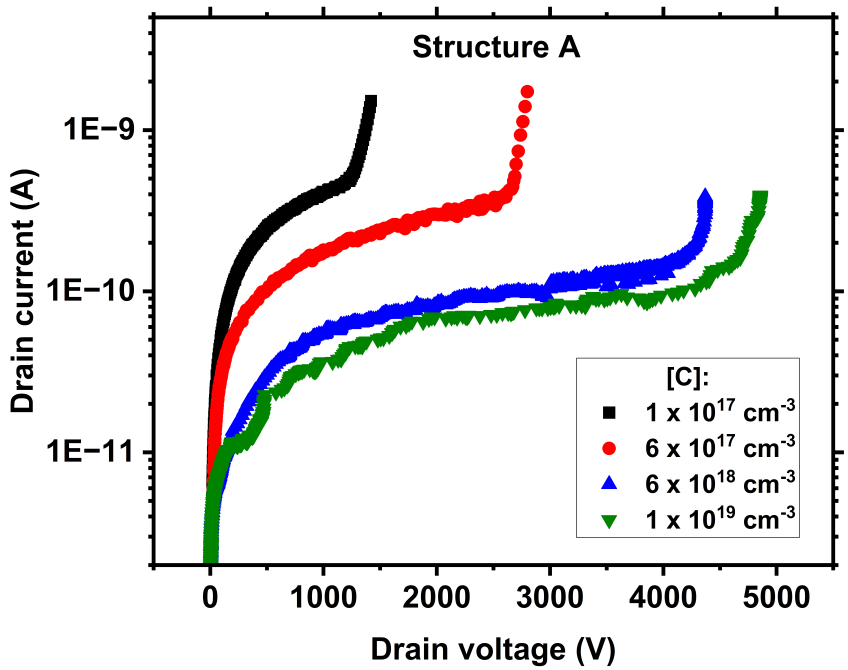


Figure 2.15: Breakdown simulation for various carbon concentrations in the buffer

Carbon atoms play two roles in these structures: (i) as acceptors, they capture electrons, reduce leakage, and help spread the electric field; (ii) they also foster leakage through trap-assisted tunneling. This trade-off was analyzed in the simulations, which showed that higher carbon concentrations lead to higher breakdown voltages, consistent with the literature [161]). A saturation effect was observed, however: increasing [C] beyond $5 \times 10^{18}\,\mathrm{cm}^{-3}$ yielded diminishing improvements in breakdown voltage. In addition, leakage decreased by one order of magnitude when the carbon concentration was increased by two orders of magnitude. Since higher C-doping also degrades material quality by increasing strain, a carbon concentration of approximately $5 \times 10^{18}\,\mathrm{cm}^{-3}$ appears optimal for power HEMTs.

To evaluate the impact of aluminum content in the back barrier, structure A was again used as the reference, with the aluminum mole fraction varied from 6% to 20%. The corresponding breakdown simulation results are shown in Figure 2.16.

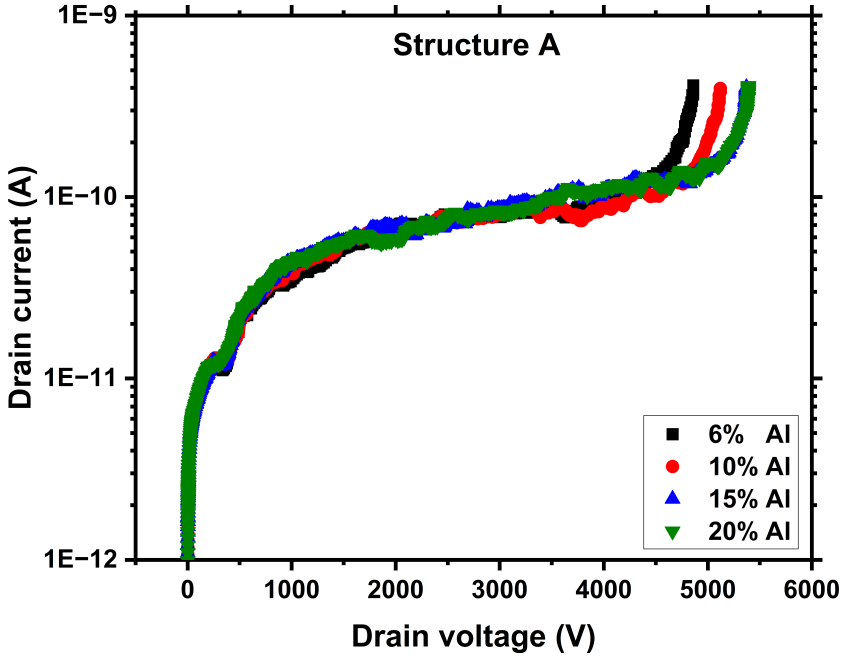


Figure 2.16: Breakdown simulations for various aluminum contents in the back barrier

Back barriers confine electrons in the upper layers due to their larger bandgap, which causes conduction band misalignment. However, their effect under high-voltage operation has rarely been studied. In our simulations, a small increase in breakdown voltage was observed with higher aluminum content, but this improvement quickly saturated. Overall, the aluminum concentration in the back barrier plays only a minor role in the off-state behavior of the HEMTs, while higher Al fractions complicate epitaxy growth and strain management.

2.3 Fabrication process of power HEMTs

In this section, I describe in detail the step-by-step process used to fabricate power HEMTs based on the previously discussed epitaxial structures. For each epitaxial stack, a quarter of a 4-inch wafer was processed.

2.3.1 Ohmic contact formation

Device fabrication begins with the deposition and annealing of ohmic contacts for the source and drain. For power devices, minimizing contact resistance is essential, as it directly contributes to the overall on-

state resistance (R_{on}) of the transistor (see Eq. 2.6). To reduce the contact resistance, the barrier layer was partially etched, allowing the metal stack to be deposited in close proximity to the 2DEG channel.

$$R_{\mathrm{on,sp}} = 2R_{\mathrm{c}} + R_{\mathrm{sh}} \cdot \left(L_{\mathrm{GS}} + W_{\mathrm{G}} + L_{\mathrm{GD}}\right) \tag{2.6}$$

- $R_{\mathrm{on,sp}}$ is specific on-state resistance of the HEMT (in $\Omega\,\mathrm{mm}^{-1}$),
- L_{GS} and L_{GD} are the gate to source and gate to drain distances respectively,
- W_{G} is the gate width.

Equation 2.6: Simplified equations for the $R_{\mathrm{on,sp}}$ of a HEMT

The fabrication sequence is as follows. To avoid depositing resist directly on the semiconductor surface, which could compromise passivation if the resist is not perfectly cleaned, a 20 nm SiO_2 layer was first deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. Photolithography was then performed using a lift-off resist, and the exposed areas were inspected under an optical microscope to verify alignment with the intended design (see Fig. 2.17).

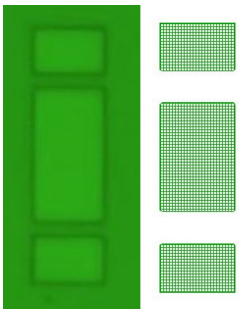


Figure 2.17: Left: optical observation of the ohmic contact photolithography. Right : theoretical design

The SiO_2 in the opened regions of the resist was etched using a diluted buffered oxide etchant (BOE) solution. Subsequently, the barrier layer was partially removed using inductively coupled plasma reactive ion etching (ICP-RIE) with a BCl_3 and Cl_2 gas mixture (ICP power : 200 W / RF power : 30 W).

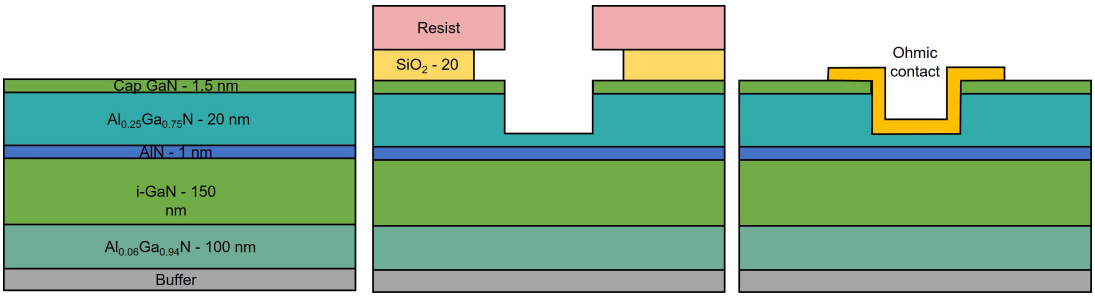


Figure 2.18: Schematics of the ohmic contact fabrication steps

The samples were then dipped for 15 s in pure BOE to remove the native Ga_2O_3 layer, which would otherwise increase the contact resistance. The chosen electrode metal stack was Ti/Al/Ni/Au (from bottom to top), a configuration widely adopted for GaN ohmic contacts in the literature for more than a decade. This stack was deposited by electron-beam evaporation under high vacuum ($1 \times 10^{-7}\,\mathrm{mbar}$). Following deposition, the resist was dissolved using SVC-14^{TM} solution, resulting in metal lift-off. The contacts were then annealed by rapid thermal annealing (RTA : 825℃ - 30 s). Finally, the protective SiO_2 layer was removed in pure BOE, completing the ohmic contact formation (see Fig. 2.19).

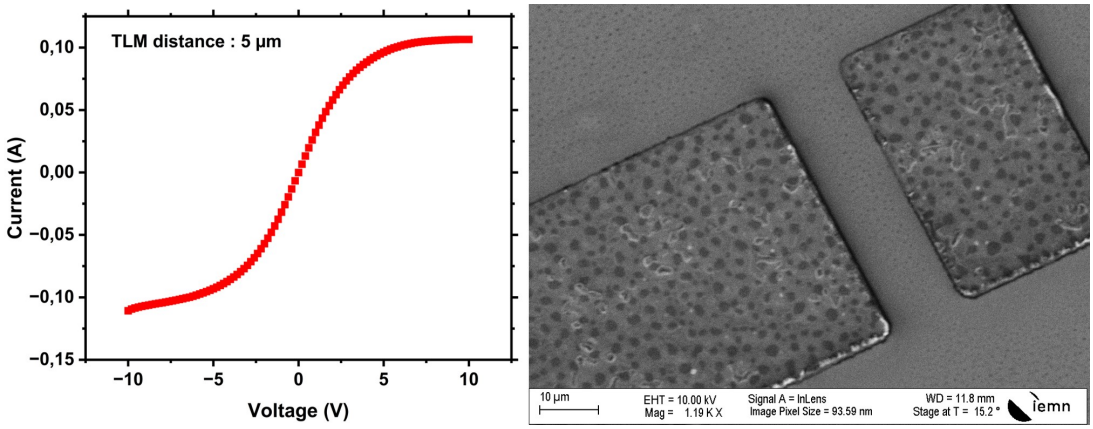


Figure 2.19: Left: I-V sweep between two TLMs. Right: SEM observation of annealed contacts

The ohmic nature of the contacts was verified by I–V sweeps between two transmission line method (TLM) structures, while surface cleanliness after annealing was assessed using scanning electron microscopy (SEM) (see Fig. 2.19).

2.3.2 Isolation etching

To define the geometry of the HEMTs and electrically isolate the contacts of each transistor, isolation trenches were etched to remove the 2DEG in non-active areas. The trench depth extended down to the buffer, thereby preventing any parasitic current flow outside the unetched regions.

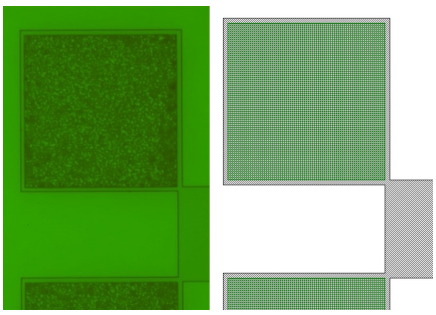


Figure 2.20: Left: optical observation of the isolation photolithography. Right : theoretical design

To achieve this, a 200 nm protective SiO_2 layer was first deposited at 300 °C by PECVD. Photolithography with a protective resist was then performed and inspected to verify alignment with the intended design (see Fig. 2.20).

The oxide layer was etched using reactive ion etching (RIE) with an SF_6 plasma (RF power : 150 W), chosen for its very high selectivity against GaN. The protective resist was subsequently stripped by oxygen plasma in the same RIE tool, followed by immersion in SVC-14^{TM}.

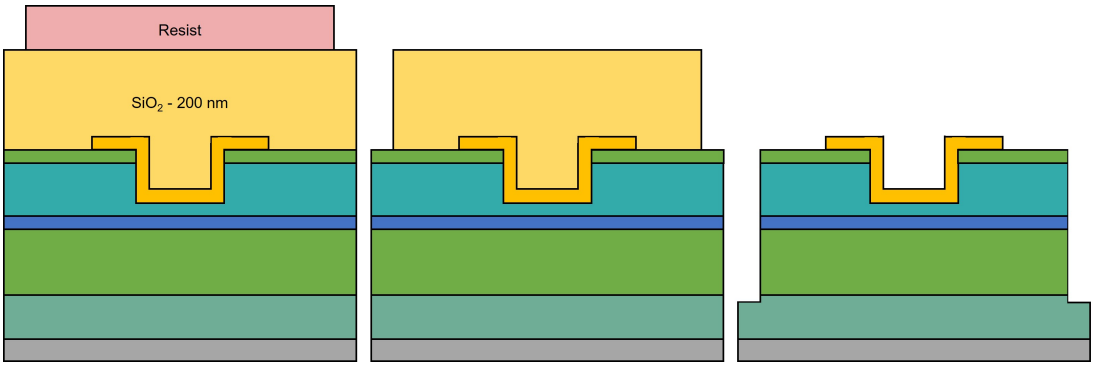


Figure 2.21: Schematics of the isolation etching process steps

Finally, the GaN and AlGaN layers were etched using inductively coupled plasma reactive ion etching (ICP-RIE) with a Cl_2/Ar gas mixture (ICP power : 100 W / RF power : 35 W), which provides a more physical etching mechanism. The residual SiO_2 protective layer was then dissolved in pure BOE, completing the formation of the isolation trench (see Fig. 2.21). For the processed structures, the trench depth was measured to be 500 $\pm$ 30 nm using a mechanical profilometer.

It is worth noting that an alternative approach to device isolation is ion implantation. In this method, the 2DEG is not physically removed but rather suppressed by defect introduction or carrier compensation using implanted ionic species (typically fluorine or nitrogen).

2.3.3 Gate deposition

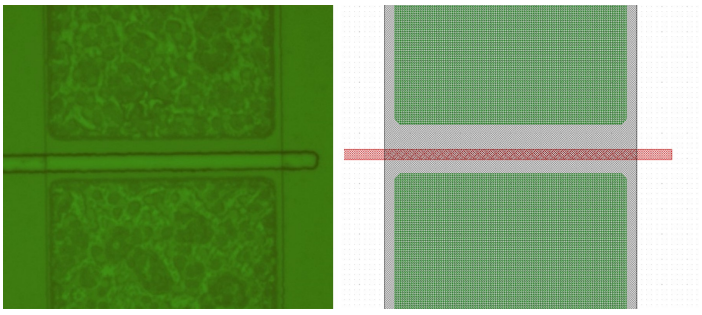


Figure 2.22: Left: optical observation of the gate photolithography. Right : theoretical design

Several gate technologies exist for HEMTs. The most common approaches are: (i) gate-on-insulator (MIS-HEMT), (ii) gate on p-GaN (e-mode HEMT, where the p-GaN layer can either be regrown by MBE or incorporated in the initial epitaxy and subsequently etched everywhere except beneath the gate), and (iii) Schottky contact gates. For this work, the simplest option was selected: the Schottky gate. The gate fabrication process closely resembles that of the ohmic contacts. A lift-off photolithography was performed (see Fig. 2.22) followed by deposition of the gate metal stack using electron-beam evaporation, after which the resist was stripped with SVC-14^{TM}.

Two key differences distinguish the gate process from ohmic contact formation. First, the metal stack must form a Schottky rather than an ohmic contact. For this purpose, a Ni/Au sequence (from bottom to top) was employed: Ni forms a Schottky contact with (Al)GaN, while Au provides high conductivity and prevents oxidation. Second, unlike ohmic contacts, the Schottky gate stack does not require post-deposition annealing.

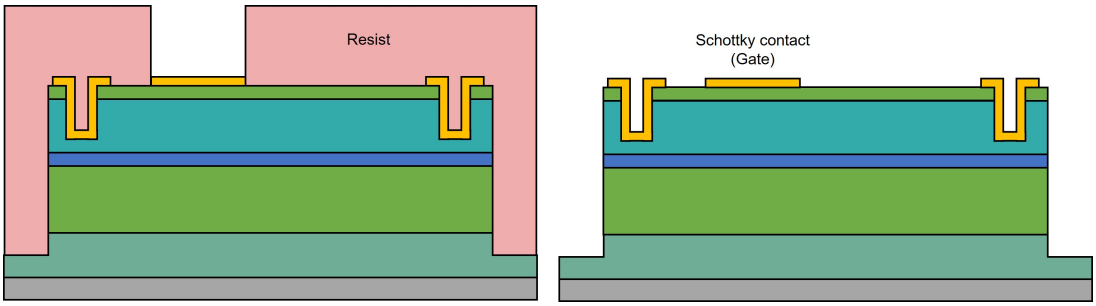


Figure 2.23: Schematics of the gate deposition steps

Because the precise placement of the gate contact is critical for HEMT operation, the fabricated gates were inspected after deposition by both optical microscopy and scanning electron microscopy (SEM) to ensure proper alignment and to confirm that no shorts occurred between the gate and source contacts (see Fig. 2.24).

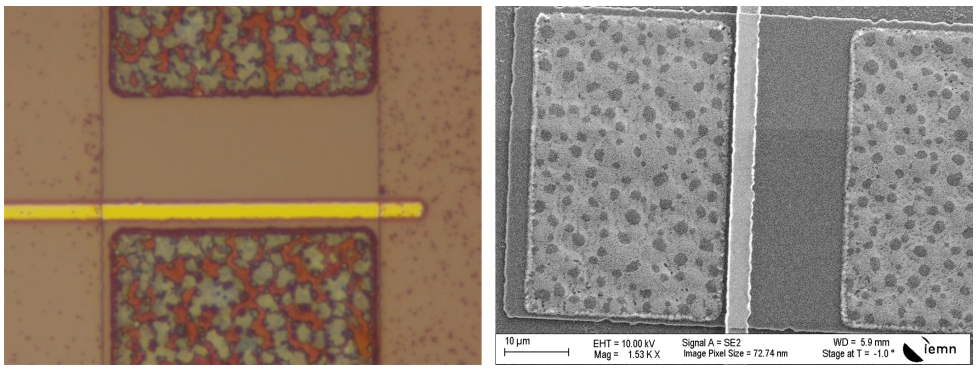


Figure 2.24: Observation of the gate after deposition. Left: optical microscope. Right: scanning electron microscope (SEM)

2.3.4 Passivation and pads deposition

To mitigate surface trapping, a passivation layer was deposited on the HEMTs: 150 nm of SiN by PECVD at 340 °C. As the name suggests, this layer passivates most of the electrically active surface states. For subsequent electrical characterization, the SiN deposited above the electrodes had to be removed on top of the pads. This was achieved through photolithography with a lift-off resist (see Fig. 2.25), followed by selective SiN etching by RIE using SF_6 plasma (RF power : 150 W).

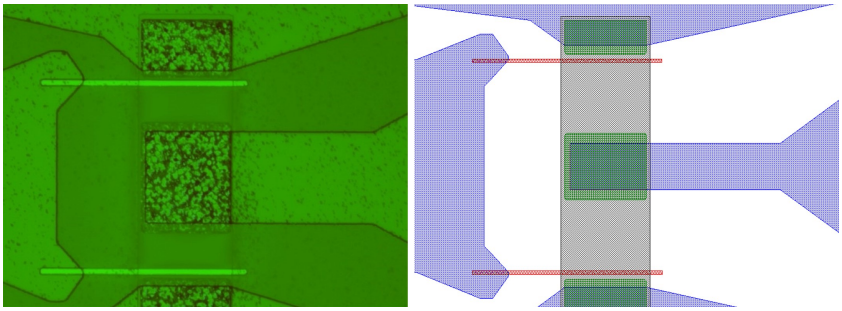


Figure 2.25: Left: optical observation of the pads photolithography. Right : theoretical design

The remaining lift-off resist was then reused for pad deposition. Since some measurement setups require large-area contacts, wide metallic pads were deposited on top of the existing source, gate, and drain electrodes (see Fig. 2.27).

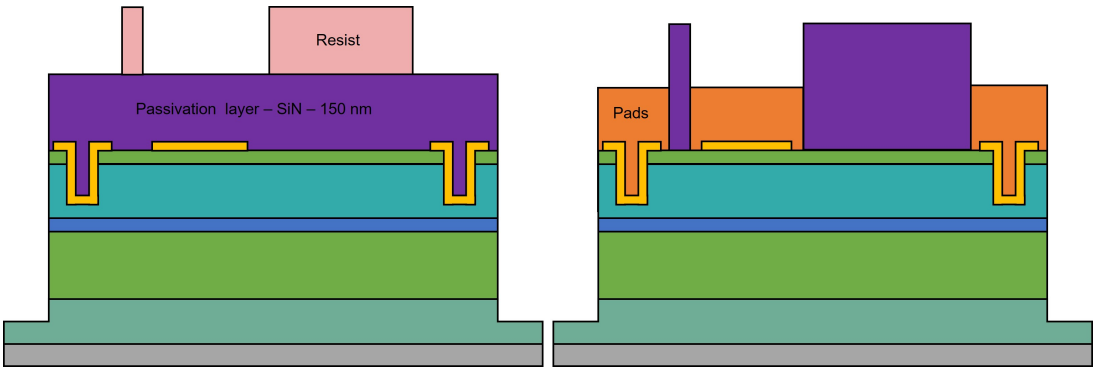


Figure 2.26: Schematics of the passivation layer and pads deposition steps

Because the pads directly contact metal, any conductive material could in principle be used. In this work, a Ti/Au stack was chosen: Ti for adhesion and Au for its high conductivity. The stack was deposited by electron-beam evaporation, and the resist was stripped with SVC-14^{TM}. Similar to the gate metallization, the pads did not require annealing.

Figure 2.27 presents a schematic top view of the fabricated HEMT:

- **Black:** active regions where the 2DEG remains (not removed during the isolation step).

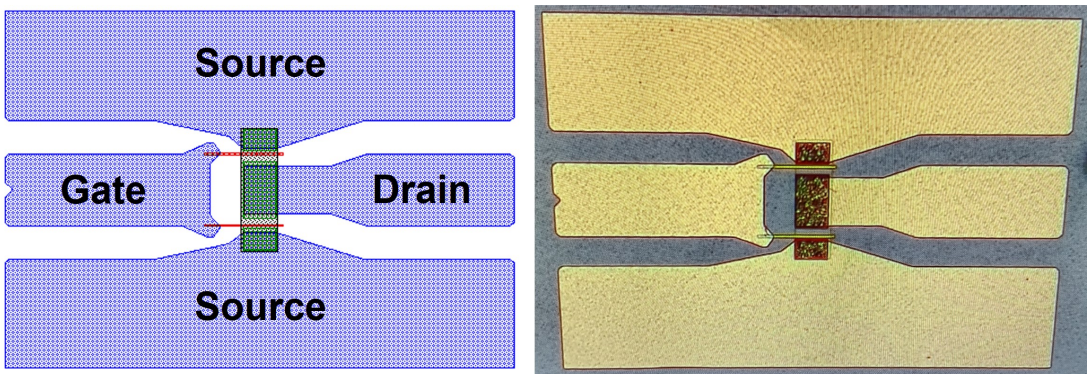


Figure 2.27: Schematic (left) and photo (right) of the fabricated HEMT at IEMN

- **Green:** ohmic contacts (drain in the center, sources on the edges). The gate–drain spacing varied from 2 to 40 µm.
- **Red:** gate contacts. The entire process employed UV-sensitive resist, resulting in 3 µm-wide gates.
- **Blue:** pad deposition areas.

Transistors with various gate–drain distances were electrically characterized in both on- and off-states. The results are presented in the following section.

2.4 Electrical characterizations

During the fabrication process, additional test structures were also implemented, such as Van der Pauw patterns and isolated contacts (see Fig. 2.28). Corresponding electrical results are presented in the following section.

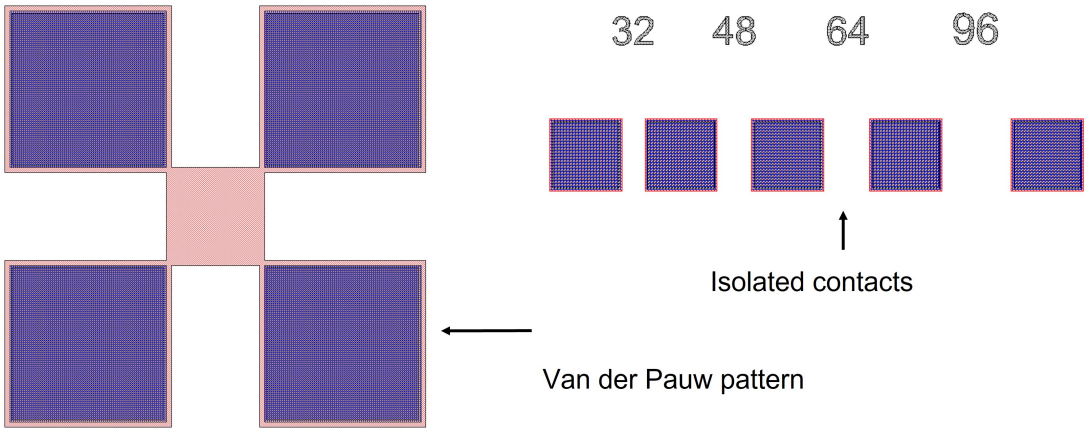


Figure 2.28: Schematic of representative test patterns used for electrical measurements, in addition to the HEMTs themselves. The numbers indicated above and between contacts correspond to the spacing between them (in µm).

2.4.1 Hall effect measurements

By using Van der Pauw patterns shown in Figure 2.28, it is possible to extract key properties of the 2DEG, namely the sheet resistance (R_{sh}), electron density (N_{S}) and electron mobility (μ_{e}) of the 2DEG. To determine R_{sh} a voltage is applied across pairs of the four terminals (labeled A, B, C, and D clockwise in the following equations), while the resulting current is measured to obtain the characteristic resistances (see Eqs. 2.7 to 2.8).

$$R_{\mathrm{AB,CD}} = \frac{V_{\mathrm{CD}}}{I_{\mathrm{[AB]}}} \tag{2.7}$$

$$R_{\mathrm{BC,DA}} = \frac{V_{\mathrm{DA}}}{I_{\mathrm{[BC]}}} \tag{2.8}$$

$$\exp\left(-\frac{\pi R_{\mathrm{AB,CD}}}{R_{\mathrm{sh}}}\right) + \exp\left(-\frac{\pi R_{\mathrm{BC,DA}}}{R_{\mathrm{sh}}}\right) = 1 \tag{2.9}$$

- $R_{\mathrm{AB,CD}}$ and $R_{\mathrm{BC,DA}}$ are characteristic resistances of the Van der Pauw shamrock,
- R_{sh} is the sheet resistance of the 2DEG.

Equations 2.7 to 2.9: Determination of R_{sh} using the Van der Pauw method

Extraction of the electron density requires a Hall effect measurement. A magnetic field $\vec{B}$ is applied perpendicular to the sample, and a current is injected along one diagonal (e.g., A $\rightarrow$ C for instance). Due to the Hall effect, a transverse voltage develops along the orthogonal diagonal (e.g., B $\rightarrow$ D). Measurement of this Hall voltage allows calculation of N_{S} (see Eq. 2.10).

$$N_{\mathrm{S}} = \frac{I \cdot B}{q \cdot V_{\mathrm{H}}} \tag{2.10}$$

$$\mu_{\mathrm{e}} = \frac{1}{q \cdot N_{\mathrm{S}} \cdot R_{\mathrm{sh}}} \tag{2.11}$$

- I and B are the current injected and magnetic field applied respectively,
- V_{H} and q are the induced Hall tension and elemental charge respectively.

Equations 2.10 and 2.11: Determination of N_{S} and μ_{e} using a Van der Pauw method

Finally, the electron mobility μ_{e} is derived from the measured values of R_{sh} and N_{S} (see Eq. 2.11). These measurements were performed at IEMN using a Hall effect measurement bench located in the cleanroom. The extracted 2DEG properties for the four fabricated structures are summarized in Tab. 2.1. Each reported value corresponds to the average of at least 5 measurements per sample.

Epitaxy	N_S (10^{12} cm^{-2})	μ_e (cm^2 V^{-1} s^{-1})	R_{sh} ($\Omega/\square$)
Structure A	8.3	1763	427
Structure B	8.9	1868	376
Structure C	9.4	1890	352
Structure D	10.2	1947	321

Table 2.1: 2DEG properties for each structure

The results indicate slightly degraded 2DEG properties for structures A and B, likely due to the thinner epitaxial layers, which increase strain and defect density. A modest degradation is also observed when a back barrier is introduced (A vs. B and C vs. D), probably for the same reason. Overall, however, all four structures exhibit rather comparable 2DEG properties.

2.4.2 DC characteristics

Both the on- and off-state characteristics of the fabricated transistors were measured using a high-voltage test bench. The setup consisted of a Keysight B1505A Power Device Analyzer equipped with a B1513C High Voltage Source/Monitor Unit, enabling measurements up to 3 kV, and complemented by a N1268A Ultra High Voltage Expander for measurements up to 10 kV. Electrical characterization began with the transfer characteristics, in order to verify proper device operation.

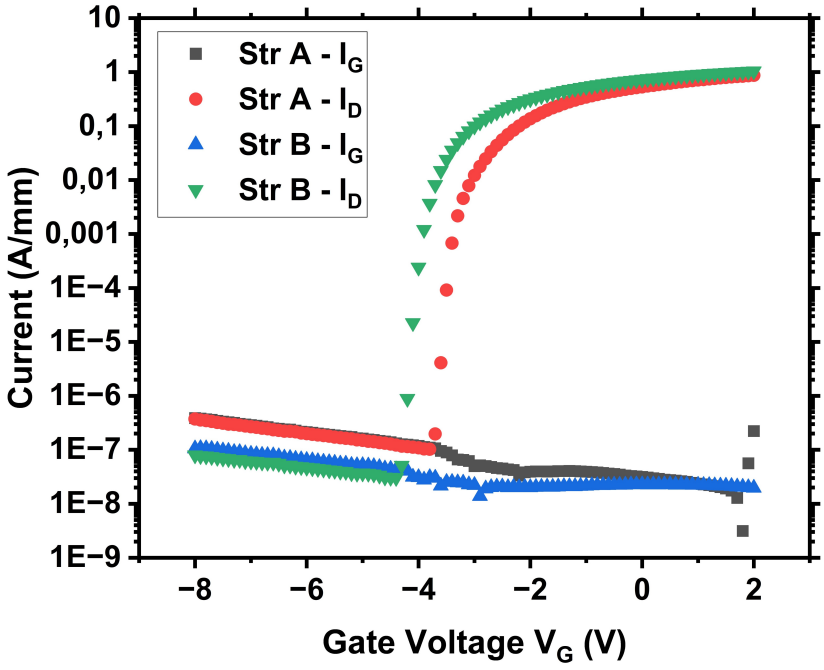


Figure 2.29: Drain current and gate leakage measured on structure A and B

For these measurements, a drain–source bias of 10 V was applied while the gate voltage was swept from –8 V to +2 V. Figure 2.29 presents representative transfer characteristics for HEMTs with

a gate–drain spacing of 10 µm, fabricated on structures A and B. Both devices exhibit comparable current densities of approximately $1\,\mathrm{A\,mm^{-1}}$, threshold voltages around –4 V, and very low gate leakage currents ($< 1\,\mu\mathrm{A\,mm^{-1}}$). Similar results were obtained across all structures, consistent with their nearly identical 2DEG properties.

2.4.3 Off-state performance: Buffer breakdown measurement

As highlighted by Cheng et al. [162], the behavior of carbon-doped GaN buffers grown on sapphire has received limited attention. Most prior studies focus on GaN-on-Si (for power devices) or GaN-on-SiC (for RF devices), whereas GaN-on-sapphire epitaxy has been used predominantly for optoelectronic applications. The following sections address this gap by examining the off-state performance of such buffers on an insulating substrate.

Isolated contacts, defined by etching the surface layers down to the buffer around them, were fabricated on each sample, with separation distances ranging from 5 to 96 µm. These structures enabled direct measurement of the breakdown voltage of the buffer layer. The corresponding results for both buffer types at each separation are presented in Figure 2.30.

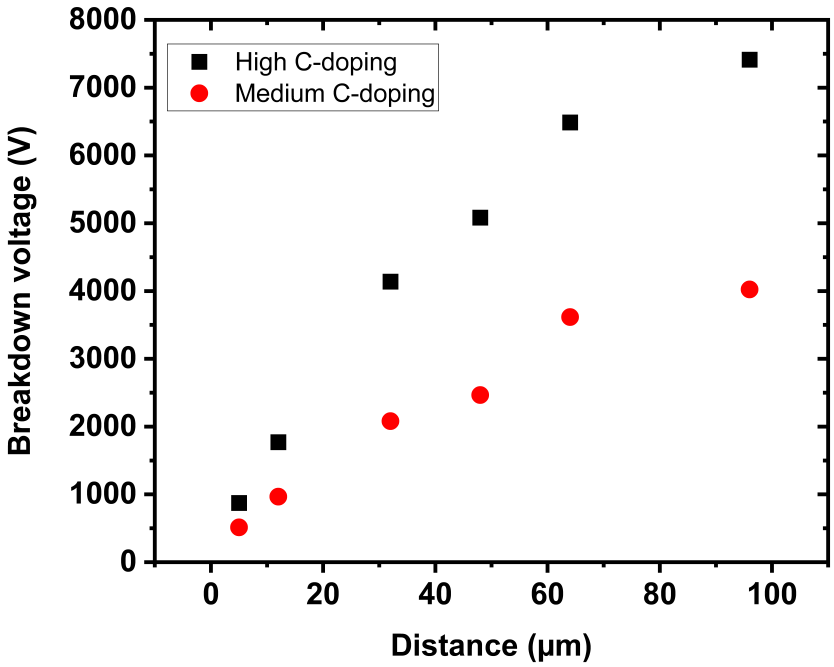


Figure 2.30: Typical buffer breakdown voltages as a function of contact spacing

Notably, the highly carbon-doped buffer demonstrated substantially enhanced voltage-handling capability, despite its reduced thickness. This observation indicates that the carbon concentration exerts a stronger influence on breakdown strength than buffer thickness, most likely due to improved compensa-

tion of deep traps and the suppression of leakage pathways.

2.4.4 HEMTs breakdown measurements

To evaluate whether the blocking performance of the buffer translates into improved device behavior, the breakdown voltage (BV) of the HEMTs was measured. The fabricated transistors had gate–drain (GD) spacings ranging from 2 to 40 µm. Measurements were carried out on devices with GD values of 10, 20, 30, and 40 µm. Figure 2.31 presents representative breakdown measurements for HEMTs with the largest GD for each structure, while Figure 2.32 shows the relationship between R_{on} and BV across all devices to assess overall performance. To ensure off-state conditions, the gate voltage was biased 5 V below the threshold voltage during all measurements.

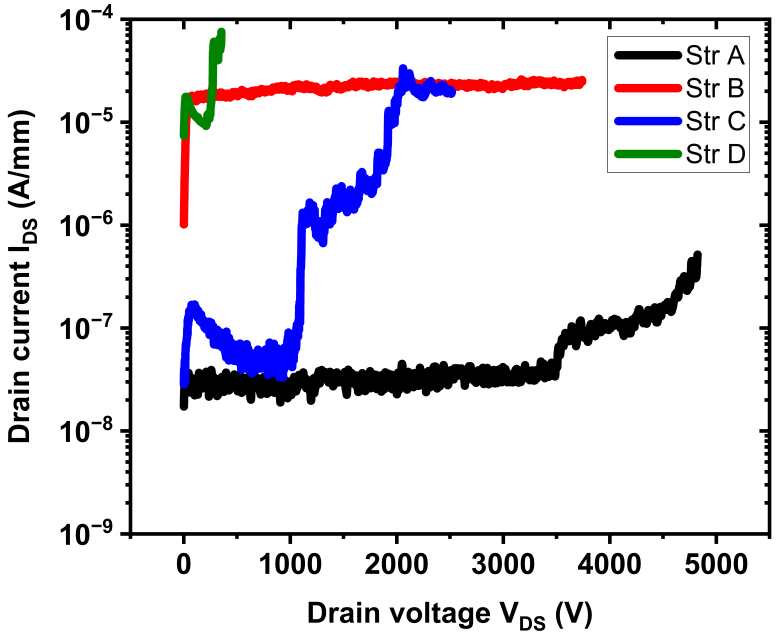


Figure 2.31: Typical breakdown voltages for HEMT with a gate to drain distance of 40 µm

As anticipated from the buffer-level breakdown analysis, devices incorporating highly carbon-doped buffers consistently exhibited higher breakdown voltages. In contrast, devices with lower carbon doping displayed increased off-state leakage currents and premature breakdown, consistent with weaker charge compensation in the buffer. The introduction of an AlGaN back barrier further enhanced BV while suppressing leakage, attributable to its role in improving 2DEG confinement and distributing the electric field more uniformly under high bias, as also reported for RF devices [163]. This enhanced confinement is critical for achieving higher blocking voltages. Importantly, all structures maintained low R_{on}, reflecting the favorable 2DEG transport properties Figure 2.32).

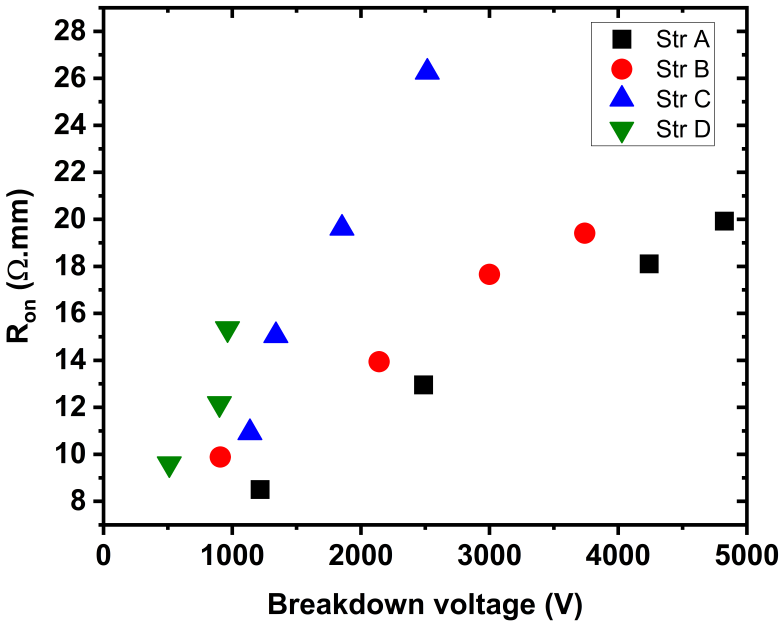


Figure 2.32: R_{on} vs breakdown voltage for our HEMTs (all GD)

The breakdown voltage scaled with GD as expected, with structures A and B (highly carbon-doped buffers) showing the best performance. A benchmark comparison is provided in Figure 2.33, placing our results in the context of the state of the art for GaN HEMTs on sapphire.

Our devices demonstrated state-of-the-art performance despite the absence of field plates or MIS gates. These promising results strongly support the continuation and further development of the exfoliation approach.

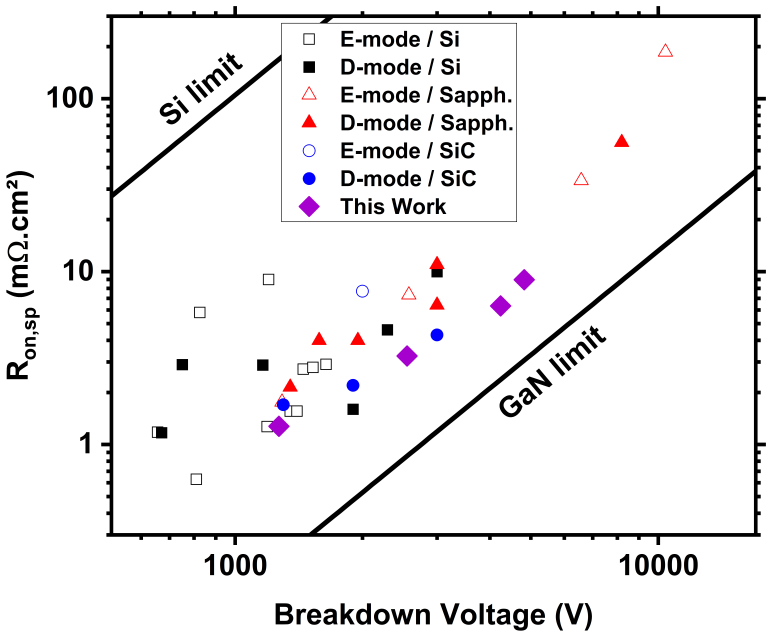


Figure 2.33: Benchmark $R_{\mathrm{on,sp}}$ vs breakdown voltage for GaN HEMT on sapphire

2.4.5 Pulsed DC measurements

Pulsed DC characterization was performed to evaluate trapping effects, both surface- and buffer-related occurring near the contacts. Two phenomena were investigated: gate lag and drain lag. To measure the gate lag, a fixed drain bias was applied while the device was maintained in the off-state for 100 µs by applying a gate voltage of –5 V, promoting electron trapping beneath the gate. The gate voltage was then abruptly switched to 2 V (on-state), and the drain current was recorded after 1 µs. By repeating this procedure at increasing drain biases, ID–VD curves were obtained (see Fig. 2.34). If electrons are trapped below the gate, they do not contribute to current conduction, and the measured drain current is reduced compared to standard DC measurements. The drain-lag experiment was performed in a similar way. The gate was held at 0 V (on-state), while a stressing drain voltage (10, 15, or 20 V) was applied for 100 µs to induce electron trapping beneath the drain. The drain bias was then switched to the measurement voltage, and the transient current was recorded.

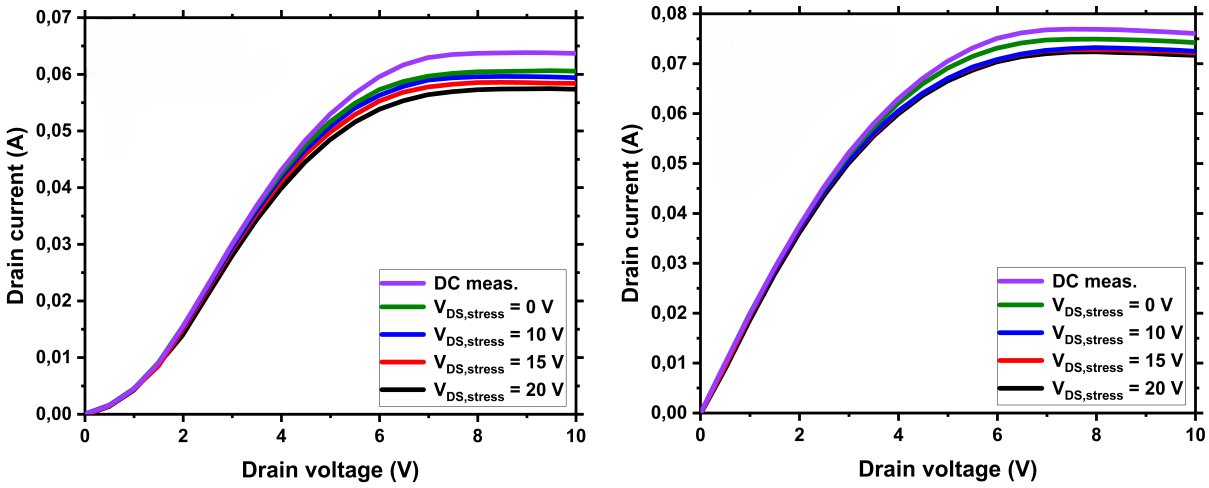


Figure 2.34: Pulsed DC measurements for structure A (left) and B (right)

Figure 2.34 reveals low gate lag and drain lag for both structures A and B, measured on HEMTs with a 5 µm gate–drain spacing. Only minimal current collapse was observed in all cases, indicating limited trapping effects.

2.4.6 Drain current transient (DCT) measurements

Drain current transient (DCT) measurements provide complementary insight to pulsed DC tests by directly monitoring the time evolution of the drain current following the release of trapped charge. Unlike pulsed DC, which compares static current levels before and after a stress condition, DCT captures the dynamics of trap emission and de-trapping, making it a powerful diagnostic for evaluating the kinetics of trapping mechanisms in HEMTs. In this experiment, electron trapping was induced by biasing the device

in a high-stress condition: a gate bias of –6 V (deep off-state) and a drain bias of 20 V were applied for 1 s to promote electron capture in surface and buffer traps. Immediately after, the biases were switched to –2 V at the gate and 5 V at the drain, and the temporal evolution of the drain current was recorded. The transient curves for structures A and B are shown in Figure 2.35.

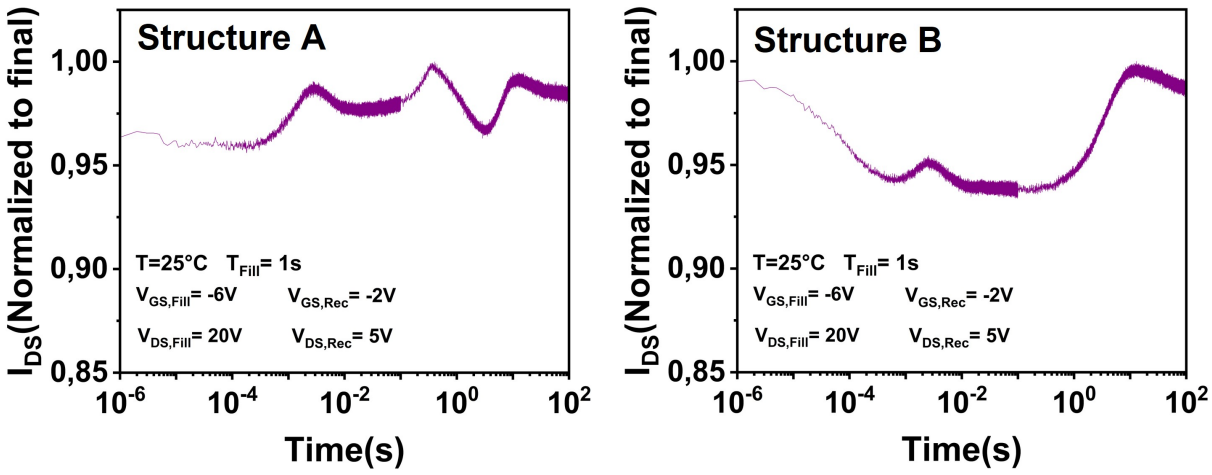


Figure 2.35: DCT measurements for structure A and B

The results reveal very limited trapping activity, with current collapse remaining below 5% in both structures. The recovery of the current occurs rapidly, without pronounced slow components, indicating the absence of deep or long-lived traps that would otherwise degrade dynamic performance. Together with the pulsed DC results, these measurements confirm that the optimized epitaxial design effectively suppresses both surface- and buffer-related trapping.

Conclusion

Using physics-based device simulations, epitaxial structures were designed and optimized to enable the fabrication of high-performance GaN-based power HEMTs on sapphire substrates. A carbon-doped GaN layer was employed as the semi-insulating buffer, and four different epitaxial stacks were proposed, grown, and processed at IEMN. HEMTs with varying gate–drain spacings were subsequently fabricated and characterized. The devices featured Schottky gates and did not rely on field plates or MIS gate technologies, thereby keeping the fabrication process simple and compatible with industrial constraints.

Electrical characterization confirmed the strong impact of buffer design on device performance. Structures A and B, which incorporated highly carbon-doped buffers, consistently outperformed their counterparts in terms of breakdown voltage and on-state resistance. The inclusion of an AlGaN back barrier was also shown to reduce leakage and improve blocking capability, highlighting its role in enhancing 2DEG confinement and electric field distribution. Together, these design choices resulted in

HEMTs delivering current densities around $1\,\mathrm{A\,mm^{-1}}$ at V_{DS} = 10 V, with low leakage currents and specific on-resistances among the best reported for GaN-on-sapphire technology.

Dynamic characterization, including pulsed DC and drain current transient (DCT) measurements, further demonstrated the robustness of the proposed structures. Both gate and drain lag effects were minimal, and current collapse remained below 5%, indicating effective suppression of surface and buffer trapping mechanisms. This dynamic stability is critical for ensuring device reliability under switching conditions. Nevertheless, the low trapping observed at moderate voltages must be further verified under high-voltage operation to fully assess device robustness for power switching applications.

Overall, the results place our HEMTs at the state of the art for GaN-on-sapphire devices, despite the absence of field plates or advanced gate technologies. These findings not only validate the proposed epitaxial design but also underscore the potential of sapphire-based GaN HEMTs for cost-effective, high-voltage power switching applications. The demonstrated performance provides a strong foundation for the exfoliation approach, with future work aiming at scaling, reliability testing, and integration into power electronic systems.

Chapter 3

Towards vertical MOSFET structures

While optimizing HEMTs is a promising route to extend GaN operation to the 1200 V range, alternative device concepts are also available. In power-conversion applications, vertical structures offer advantageous trade-offs and constitute the predominant architecture for high-power devices (Chapter 1).

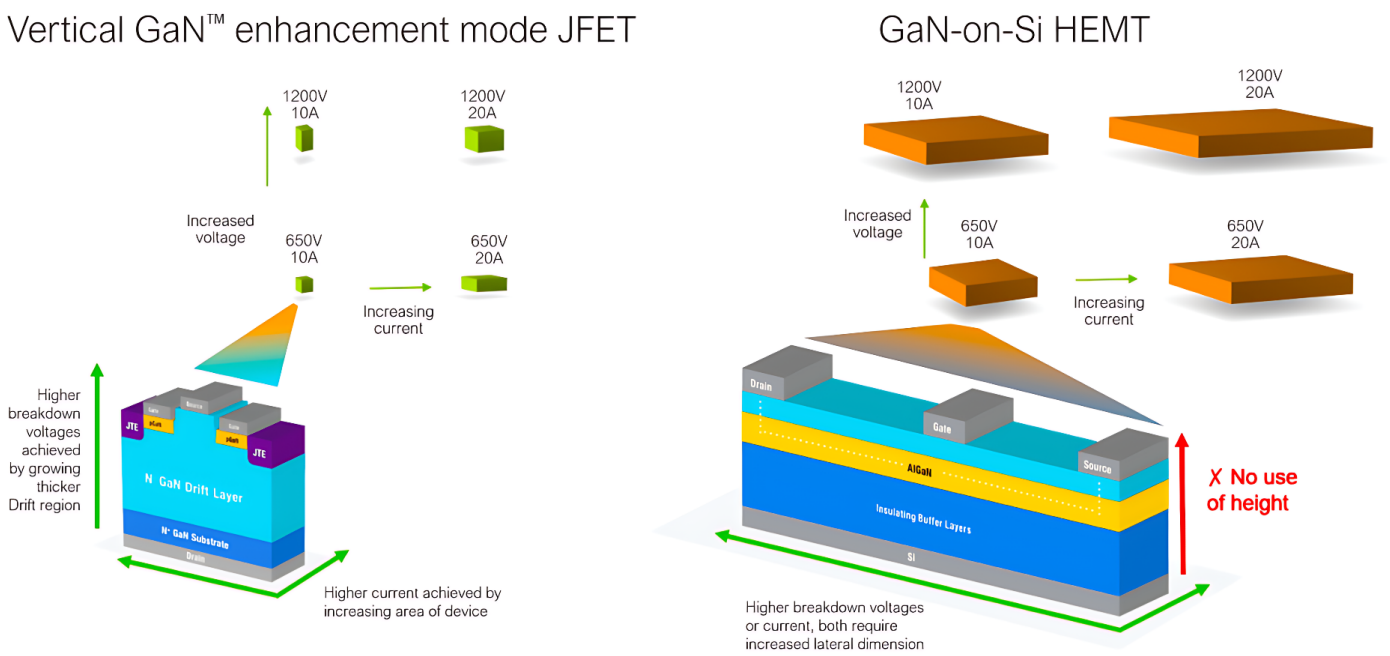


Figure 3.1: Sizing of vertical and lateral structures for power applications taken from [164]

The favorable aspects of GaN vertical trench MOSFETs (V-T-MOSFETs) include:

- **Current scaling with gate area.** In vertical cells, the conduction path scales with trench gate area rather than lateral width, enabling a smaller die at a given current rating and thus higher power density.

- **Breakdown set by thickness.** The blocking voltage is primarily determined by the vertical drift thickness and doping, so BV can be increased without enlarging the lateral footprint.
- **Backside metallization and vertical heat flow.** A low-resistance backside electrode provides a direct thermal path to the heat spreader; self-heating is mitigated compared with surface-hot lateral channels on GaN-on-Si HEMTs.
- **Bulk-centric heat generation.** The vertical current path distributes Joule heating in the bulk, away from surface access regions, easing thermal management at high current density.
- **Intrinsic avalanche path.** Properly designed vertical p–n structures can support controlled avalanche and wider safe operating area (SOA) than lateral HEMTs whose buffers and gates limit avalanche ruggedness.
- **Lower buffer-related trapping.** Vertical GaN devices do not require the highly carbon-doped buffer used on GaN-on-Si, reducing buffer trapping and dynamic-R_{on} effects.

Vertical GaN architectures may offer higher voltage blocking capability and a smaller footprint, but require significant research as they are immature compared to HEMTs. Several bottlenecks remain in the fabrication steps to replicate actual vertical structures (SiC MOSFETs for instance):

- **Achieving high p-type doping**. Mg is a relatively deep acceptor (around 0.15 eV above valence band [165, 166]) in GaN. After annealing the percentage of ionized acceptors is usually around 0.5 to 5%, up to to 8% with extreme activation methods (annealing above 1100℃ for several minutes by RTA [165]);
- **Ion implantation is challenging**. It causes severe lattice defects that are difficult to repair. Annealing above 1100℃ is required and protective layer [165] or extremely high pressure [167] is necessary to avoid GaN decomposition. Moreover, dopants diffuse poorly during activation, making it difficult to design doping profiles;
- **Lack of suitable thermal gate oxide**. Si and SiC use thermally grown SiO_2 for their gate, which offer great interface quality (Chapter 1). Ga_2O_3 cannot be used as gate dielectric due to its unsuitable properties: small conduction band offset with GaN (< 0.3 eV), prone to oxygen vacancies trap formation and tendency to form Ga-O-N inter-layer and a leaky stack overall.
- **Thick, high-quality GaN-on-Si epitaxies are still under development,** and devices may suffer from polarization-charge effects, wafer bow and high dislocation density.

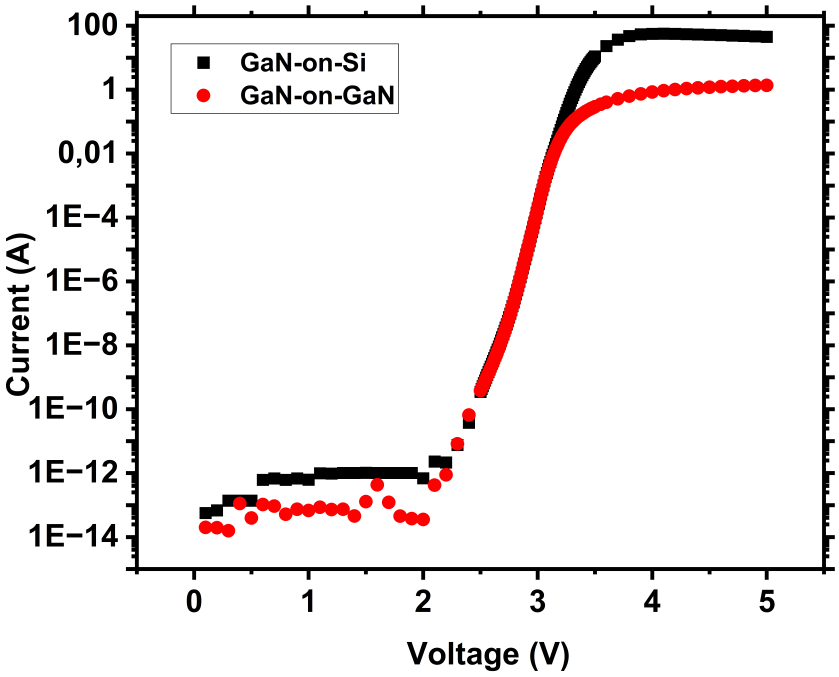


Figure 3.2: On-state current comparison for a GaN-on-GaN and GaN-on-Si PiN diodes

Figure 3.2 compares the forward characteristics of GaN-on-GaN and GaN-on-Si PiN diodes (reference structure taken from [168]), illustrating the potential of GaN-on-Si for high-current operation once epitaxial and processing issues are mitigated.

PiN diodes and V-T-MOSFETs have been fabricated in recent years with GaN-on-GaN epitaxies and displayed promising results [113, 169]. Transferring these processes on GaN-on-Si could improve the current output. Hamdaoui et al. demonstrated fully vertical gaN-on-Si GaN diodes with breakdown voltage over 1200 V, output current over 10 A, and avalanche capability [170, 171]. Vertical devices fabricated on bulk GaN do not require substrate thinning; instead, a backside electrode is deposited directly on the native substrate. However, the thick GaN substrate ($>$300 µm) acts as a poor thermal conductor, since the heat source lies far from the heat sink. By contrast, GaN-on-Si epitaxy enables substrate processing and deposition of a thick copper layer closer ($<$15 µm) to the active region, significantly improving heat extraction and allowing higher current operation (Fig. 3.2).

Reports on GaN-on-Si V-T-MOSFETs remain scarce [114, 172] and currently demonstrate breakdown voltage below 600 V. These devices must be improved through fabrication method enhancement.

The investigation and optimization presented in this chapter were carried out within the framework of the VertiGo project. The goal of this multi-partner initiative funded by the French Agence Nationale de la Recherche under the PEPR Électronique program is to establish a complete fabrication flow for vertical GaN devices capable of blocking kilovolt-class voltages while maintaining low specific on-resistance, thereby complementing the high-frequency domain already well served by lateral HEMTs.

The chapter begins with the baseline process flow for GaN-on-Si vertical MOSFETs developed at IEMN, covering trench formation, mesa etching, gate-dielectric deposition, and contact metallization. Simulations are presented to propose new edge-termination methods using fluorine implantation or p-GaN regrowth. Finally, electrical characterization of the fabricated quasi and fully vertical transistors demonstrates the potential of this architecture while clarifying its present limitations.

3.1 Fabrication process of a GaN-on-Si fully vertical trench MOSFET

Among publications reporting the fabrication of fully vertical p-i-n diodes [171, 173] or V-T-MOSFETs [114, 172] on GaN-on-Si epitaxial stacks, the silicon substrate is either fully removed after bonding the epilayers to a carrier substrate, or locally etched to expose the n^+ layer for backside contact formation. The process presented here adopts the second approach and follows Hamdaoui et al. [171], who demonstrated fully vertical p-i-n diodes with $\sim$1200 V breakdown and avalanche capability.

The GaN-on-Si epitaxial wafer used for device fabrication was provided by Siltronic and has the following specifications: 1300 µm thick, 6-inch Si substrate, 1.5 µm of buffer layer, a 700 nm n^+ drain layer (Si=$1 \times 10^{19}\,\mathrm{cm}^{-3}$), a 3500 nm n^- drift region (Si=$3 \times 10^{16}\,\mathrm{cm}^{-3}$), a 500 nm p-body (Mg=$2 \times 10^{19}\,\mathrm{cm}^{-3}$) and a 330 nm n^+ source layer (Si=$1 \times 10^{19}\,\mathrm{cm}^{-3}$). This stack was used to fabricate quasi- and fully-vertical device and had proven to procide competitive performance (see Sec. 3.3.1). Only a fragment of the wafer was processed for each sample. The fabrication starts after cleaning each piece for 2 min in acetone, then 2 min in isopropanol (IPA) and drying them with N_2 blow. The following steps are given for the reference sample.

3.1.1 Mesa and gate trench etching

The process begins with the etching of both the mesa and gate trench, using the same hard mask and same etching recipe for both. Firstly, a 1.1 µm SiO_2 layer was deposited at 300°C using PECVD. Photolithography was performed to define the mesa trench, and the silicon dioxide was etched using SF_6 plasma. The resist was removed using O_2 plasma, followed by 2 h immersion in SVC-14^{TM} at 70°C. Then, a 2.2 µm deep etching was done by ICP-RIE using Cl_2 and Ar. Another photolithography step was performed to define the gate trench. The SiO_2 was etched and the resist was removed using the same method. Finally, a 1.4 µm additional etching was performed by ICP-RIE (same Cl_2/Ar recipe). The SiO_2 remaining was dissolved by immersing the sample for 90s in pure buffered oxide etchant (BOE).

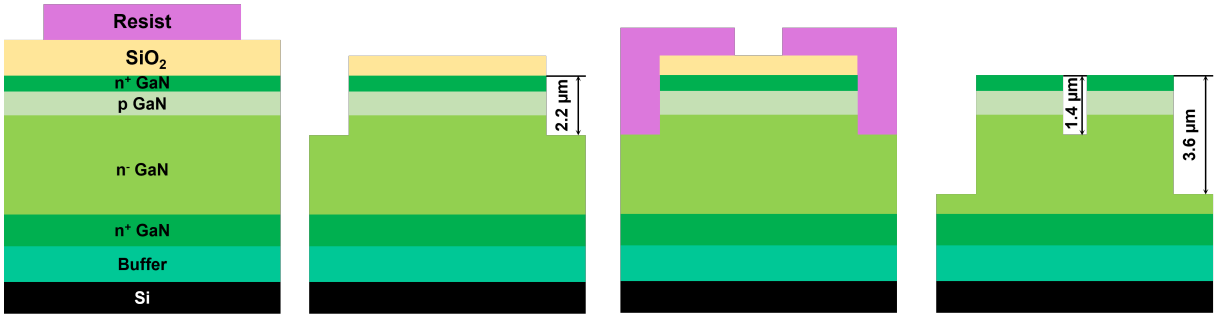


Figure 3.3: Main steps of the mesa and gate trench etching

At this stage, the sample has a 1.4 µm deep gate trench and a 3.6 µm deep mesa trench. Several inspection steps and measurements were performed after photolithography, etching, resist or SiO_2 removal to ensure proper process execution. Ultimately, the etching depths were measured using a mechanical profilometer.

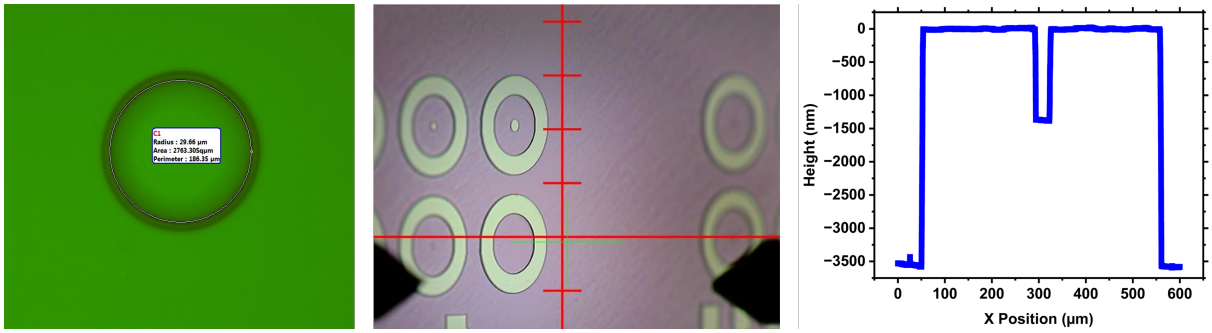


Figure 3.4: Sample observations during trench etching: (left) gate lithography under microscope, (middle) SiO_2 mask after second SF_6 etch and resist removal, (right) profilometer step measurement after oxide removal.

To achieve a reasonable etch rate ($\simeq 300\,\mathrm{nm\,min^{-1}}$) and near-vertical trench profiles ($\simeq 80°$), the process relied predominantly on Ar ion assistance, despite the associated increase in lattice damage. Further optimization of the gate trench etching was not pursued here, as gate fabrication optimization was the responsibility of another member of the VertiGo project (Valentin Ackermann [174]).

3.1.2 Contact formation

After the etching steps, the p-type dopants were activated by a 20 min anneal at 750 °C in N_2. Following a 2 min immersion in BOE, rinsing, and drying, the gate dielectric was deposited by PECVD: 100 nm of SiO_2 at 300 °C. Source contacts were defined by a lift-off photolithography process. The oxide above the contact openings was locally removed in BOE for 90 s, after which a Ti/Al/Ni/Au stack was deposited by electron-beam evaporation (same recipe as for HEMTs, see Sec. 2.3.1). After lift-off, the contacts were annealed for 10 min at 500 °C in air.

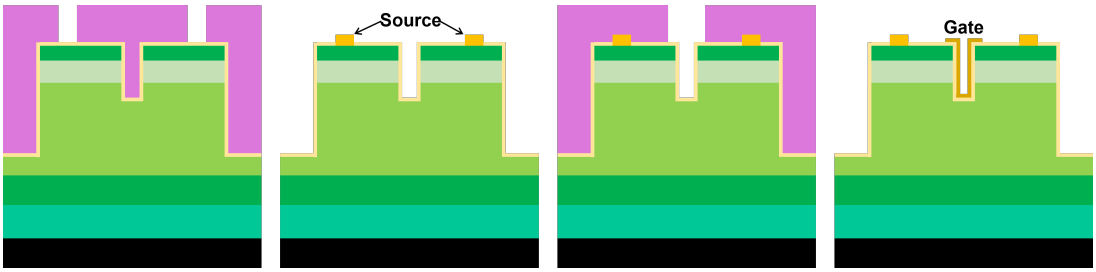


Figure 3.5: Main steps of the contact formation process.

Gate metallization followed the same sequence except that neither SiO_2 removal nor a contact anneal was performed. In this case the metal stack was Ni/Au. Inspection steps were carried out to verify alignment and feature dimensions (Fig. 3.6) and to confirm the ohmic behavior of the source contacts.

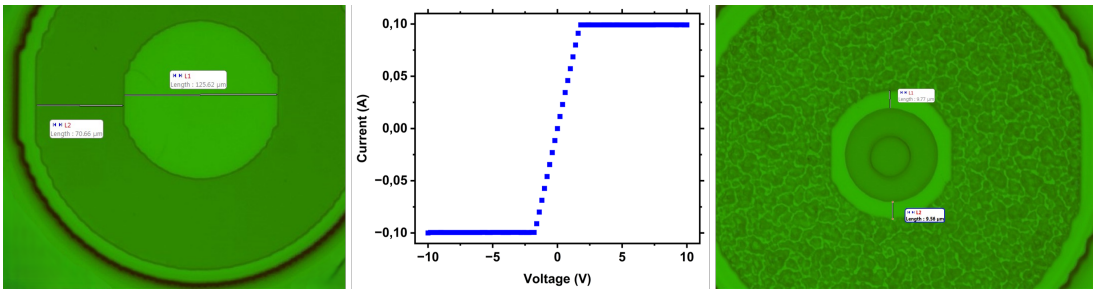


Figure 3.6: Optical inspection of the source (left) and gate (right) lithographies, and two-terminal measurement between TLM pads separated by 5 µm (center).

3.1.3 Backside processing

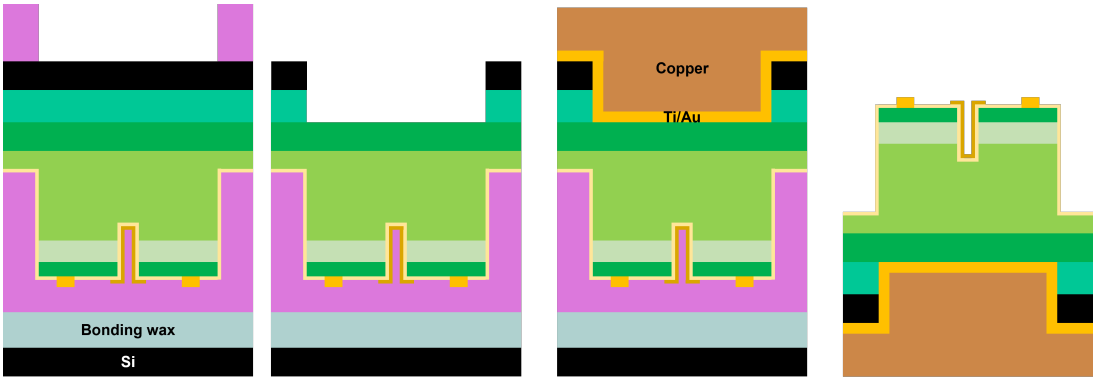


Figure 3.7: Main steps of the backside process

To process the Si substrate, a protective resist was applied to the front side and the sample was bonded to a Si carrier wafer with bonding wax. The substrate thickness was reduced to 300 µm by mechanical grinding, and a photolithography was performed to define the drain locations. Because there were no alignment marks on the backside, 2000 µm-diameter circles were patterned across the

sample to form the drain contact.

The remaining Si was etched using the Bosch (deep RIE) process [175, 176]. The buffer layer was then etched by ICP (Cl_2 plasma), after which the resist was stripped. Because GaN is spontaneously polarized along the c-axis (Chapter 1), the Ga- and N-polar faces exhibit different chemistries [177] (see Fig. 3.8 - [178]). The N-polar (back) face is more reactive; therefore the pre-metallization clean followed Ref. [179]: a 2 min immersion in HCl (37%) at 70 °C. A Ti/Au stack was then deposited to form an ohmic contact. Finally, a thick (> 100 µm) Cu layer was electroplated to act as a heat sink and to provide mechanical stability.

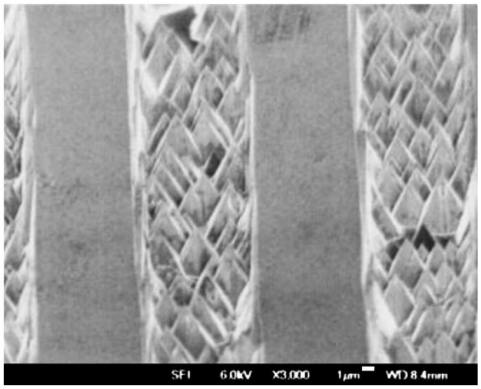


Figure 3.8: Observation of Ga- and N-polar GaN surfaces after etching in 2M KOH at 90℃ for 45 min

An electrochemical deposition (ECD) bench was built at IEMN and a Cu plating recipe was developed. The objective was to deposit a thick Cu layer to ensure mechanical stability and to form the drain contact. Test coupons consisted of Si fragments coated with a Ti/Au adhesion/seed stack. Unless stated otherwise, the $CuSO_4$ solution was held at 45°C with magnetic stirring at 200 rpm.

In the first trial, a constant (galvanostatic) current of 100 mA was applied for 2 h. The deposit was uniform and 18 µm thick (Fig. 3.9).

To increase the deposition rate, a second run used 100 mA for 30 min to create a smooth nucleation layer, followed by 200 mA for 90 min. The resulting thickness was 60 µm, but local Cu nodules (overgrowths) appeared, predominantly near the sample edges and more sparsely across the surface (Fig. 3.9), likely due to current crowding along field lines.

A third sample was plated at 100 mA for 4 h to test whether a thick layer could be obtained at the lower current. The deposit was 55 µm thick but strongly irregular, with numerous nodules (Fig. 3.9).

To mitigate nodule formation, the agitation was increased to 400 rpm and the deposition was interrupted every 30 min to check for overgrowths and, when present, to mechanically remove them. Sample 4 was processed as follows: 1 h at 100 mA / 30 min at 200 mA / nodule removal (NR) / 1 h at 100 mA / NR / 1 h at 200 mA / NR / 1 h at 100 mA / NR / 30 min at 100 mA / 30 min at 200 mA / NR.

The total deposition time was 5 h 30 min, yielding a thickness of 140 µm.

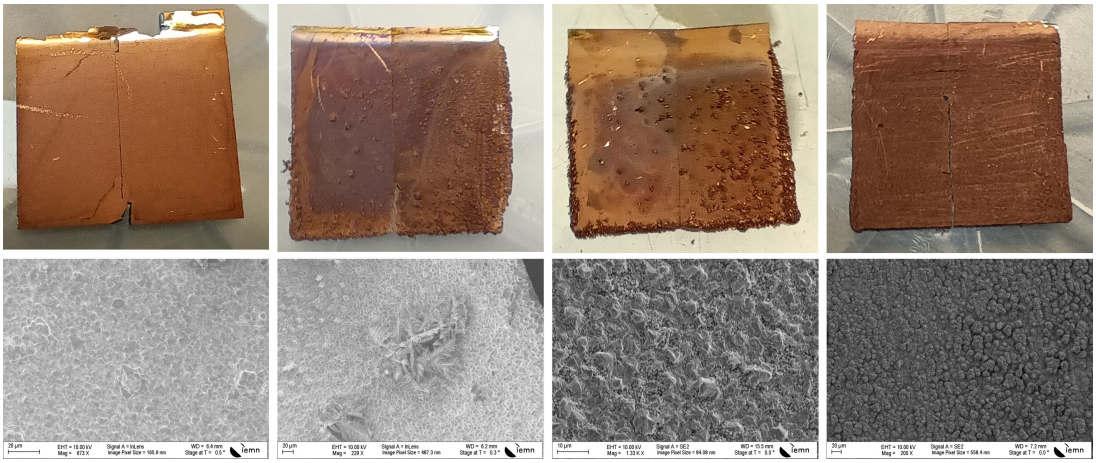


Figure 3.9: Macroscopic (top) and SEM (bottom) observation of sample 1 to 4 (from left to right)

Although the deposited thickness was acceptable, the macroscopic appearance was degraded by the mechanical nodule removal (visible scratch marks, Fig. 3.9). To investigate the effect of current density, a fifth sample was electroplated using a stepwise increase in current—0.25, 0.5, 0.75, and 1.5 A, each applied for 30 min, with an agitation set at 400 rpm. The resulting Cu surface was smooth but the thickness was non-uniform: approximately 100 µm near the electrical contact point and up to 160 µm at the opposite edge (Fig. 3.10).



Figure 3.10: Macroscopic observation of sample 5

Because the Cu layer primarily provides mechanical support, this thickness non-uniformity is not critical for device operation. To obtain a thicker deposit, a plating sequence consisting of 1 h at 0.5 A, 1 h at 1.0 A, and 1 h at 1.5 A was implemented, yielding a layer approximately 550 µm thick. This high-current recipe was therefore adopted for subsequent processing.

3.2 Process optimization with quasi-vertical trench MOSFETs

Before manufacturing fully vertical devices, different gate-dielectric and mesa-passivation processes were evaluated using quasi-vertical transistors. To avoid backside processing, the drain contact was

formed at the bottom of the mesa trench during the source-formation steps (shared photolithography, metal-stack deposition, and annealing). This contact reaches the bottom n^+ layer through the thin residual drift layer left at the trench bottom (Fig. 3.11).

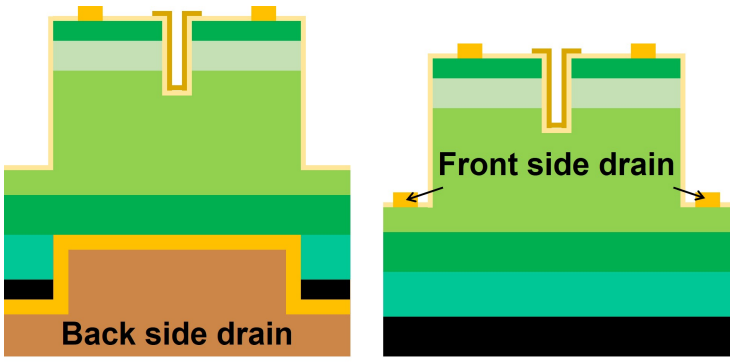


Figure 3.11: Schematic comparison of a fully vertical trench MOSFET (left) and a quasi-vertical trench MOSFET (right).

These devices are simpler and faster to fabricate because they do not require backside processing. Their electrical behavior differs slightly from that of fully vertical devices due to current crowding near the front side drain contact, which generally reduces the output current [114].

3.2.1 Impact of the oxide

A high-quality dielectric/GaN interface in the MOS stack is critical to ensure proper operation of trench MOSFETs [180]. Fixed charges and interface traps can affect the threshold voltage and electron mobility in the channel, and are detrimental to the dynamic on-resistance [174]. In our process, the dielectric was annealed together with the source contact (10 min at 500 °C). A reference process using 100 nm of SiO_2 (Sec. 3.1.2) was compared with a sample employing a SiO_2/Al_2O_3 bilayer: first, 50 nm of aluminum oxide was deposited by atomic layer deposition (ALD) at 300 °C, followed by 50 nm of SiO_2 deposited using the same PECVD recipe as the reference sample.

To assess the impact of interface quality on the device operation, five consecutive gate-voltage sweeps were performed at a fixed drain bias of 10 V. Since the threshold voltage was higher for the bilayer dielectric, the gate voltage was swept from 0 to 30 V, compared to 0–20 V for the single-layer reference (Fig. 3.12). A progressive increase in the threshold voltage was observed in the bilayer MOSFET, which is attributed to electron trapping at interface states. These traps could originate from oxygen or aluminum vacancies, or Al–O antisites, depending on the deposition and annealing conditions. A similar effect, though less pronounced, was observed for the single-layer dielectric.

Although aluminum oxide is generally reported to form a high-quality interface with GaN [181], the poor behavior of the bilayer MOS structure is likely due to traps located at the oxide/oxide interface.

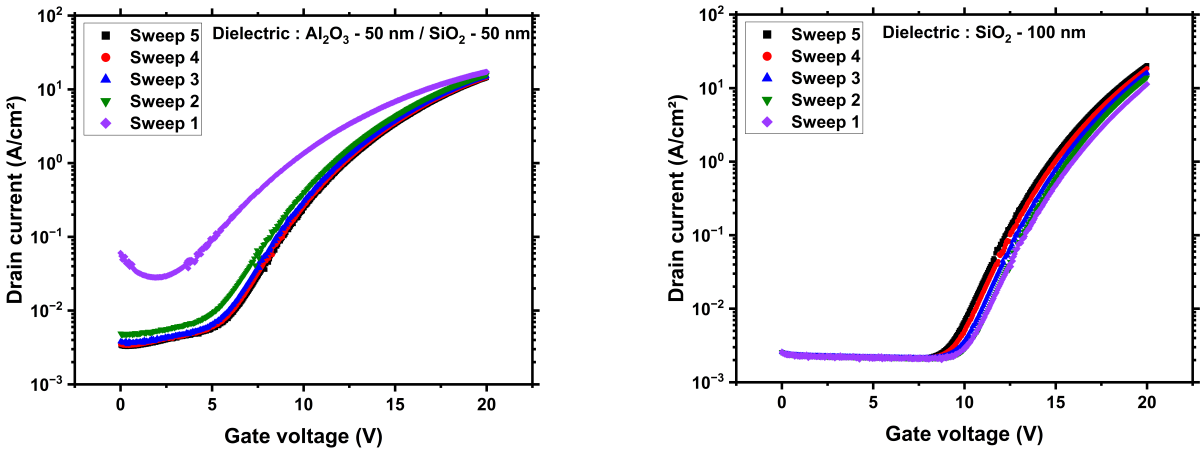


Figure 3.12: Consecutive I_D-V_G sweep on both samples

The SiO_2 deposited by PECVD is hydrogen- and hydroxyl-rich, which can generate border traps at the interface with Al_2O_3 [182, 183]. To mitigate this issue, the aluminum oxide layer should be densified or annealed prior to the deposition of the SiO_2 capping layer.

3.2.2 Improvement of the isolation method

The vertical anisotropic etching of GaN relies on the impact of Ar ions, which primarily remove material by physical sputtering. This process creates several types of damage at the etched surface, including lattice disorder, nitrogen vacancies, and a locally higher Ga concentration [184–187]. The damaged surface can act as a leakage pathway, since these defects behave as traps that promote trap-assisted tunneling.

To overcome this problem, two alternative isolation approaches are proposed: passivation of the etched surface using a p-GaN layer regrown by molecular beam epitaxy (MBE), and device isolation through fluorine implantation instead of mesa etching.

The upcoming simulations of quasi-vertical trench MOSFETs are done in comparison with a reference structure based on our epitaxy (Sec. 3.1), using mesa etching termination (MET) isolation method, and whose sidewalls are passivated by 100 nm of silicon dioxide and present an interface-trap state density of $1 \times 10^{13}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, following [188]. The trap-assisted tunneling (TAT) model was enabled to account for leakage, although due to convergence limitations it was only activated for drain voltages above 20 V. This reference showed a breakdown voltage of 335 V.

Mesa passivation using p-GaN regrowth

Because dry etching generates nitrogen vacancies (donor-type traps) that make the GaN surface more n-type, mesa sidewalls become potential leakage paths in vertical MOSFETs. Typically, the gate dielectric deposited in the trench also covers the mesa walls and provides some degree of passivation, but this is not necessarily sufficient or optimal to reduce leakage.

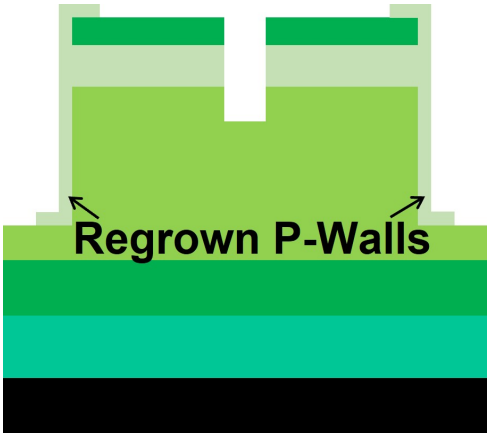


Figure 3.13: Schematic of the p-walls after their deposition and hard mask removal

A solution proposed here is to regrow a thin p-type GaN layer on the mesa walls using molecular beam epitaxy (MBE), forming a local p–n junction with the n-type drift region. This junction depletes the underlying GaN and prevents electrons from reaching the damaged sidewall, thereby suppressing leakage currents. Since MBE growth requires a temperature around 800 °C, the regrowth must be performed prior to contact formation to avoid multiple high-temperature annealing steps (Fig. 3.13).

To estimate the impact of this layer on the off-state behavior of our trench MOSFETs, two-dimensional simulations were performed using Silvaco TCAD. The regrown p-GaN layer thickness was fixed at 200 nm, and its acceptor concentration varied from $2 \times 10^{17}\,\mathrm{cm}^{-3}$ to $5 \times 10^{18}\,\mathrm{cm}^{-3}$, which are values typically achieved in MBE-grown p-GaN.

A reduction of the leakage current by approximately one order of magnitude and a 20% increase in breakdown voltage were observed (Fig. 3.14). It is important to note that the improvement saturates for acceptor concentrations above $5 \times 10^{17}\,\mathrm{cm}^{-3}$, indicating that further doping does not enhance the depletion or isolation effect.

Since tunneling currents cannot be directly visualized in Silvaco TCAD, Fig. 3.15 presents the simulated impact-ionization coefficient (which overlaps the regions of highest leakage current) at 330 V for both the reference structure and the one incorporating p-GaN walls doped at $5 \times 10^{17}\,\mathrm{cm}^{-3}$. With sufficiently high p-type doping, the depletion induced by the p-walls completely suppresses current leakage along the mesa.

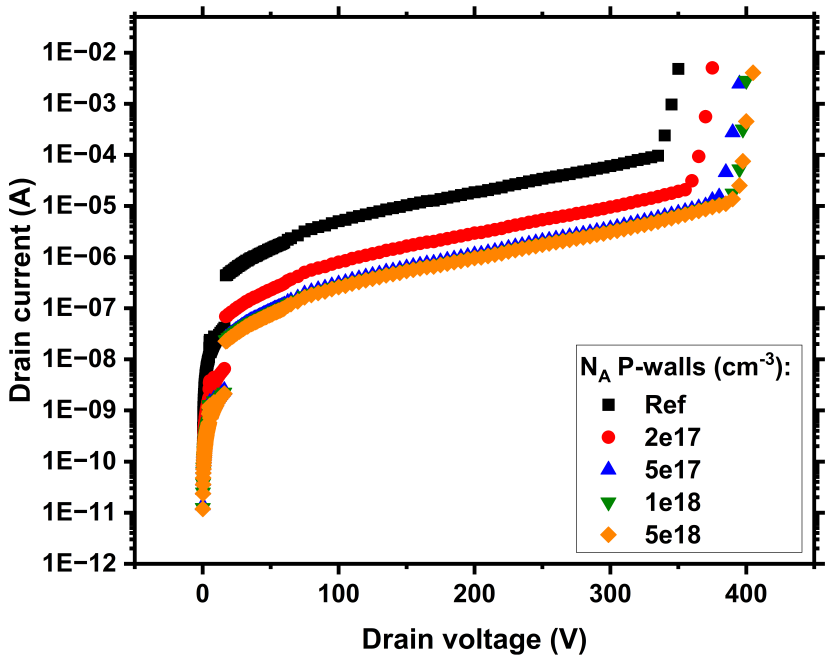


Figure 3.14: Simulations of MOSFETs with mesa passivated by different regrown p-walls

Moreover, a stronger impact ionization is observed along the mesa wall than in the bulk GaN for the reference device, explaining its earlier breakdown.

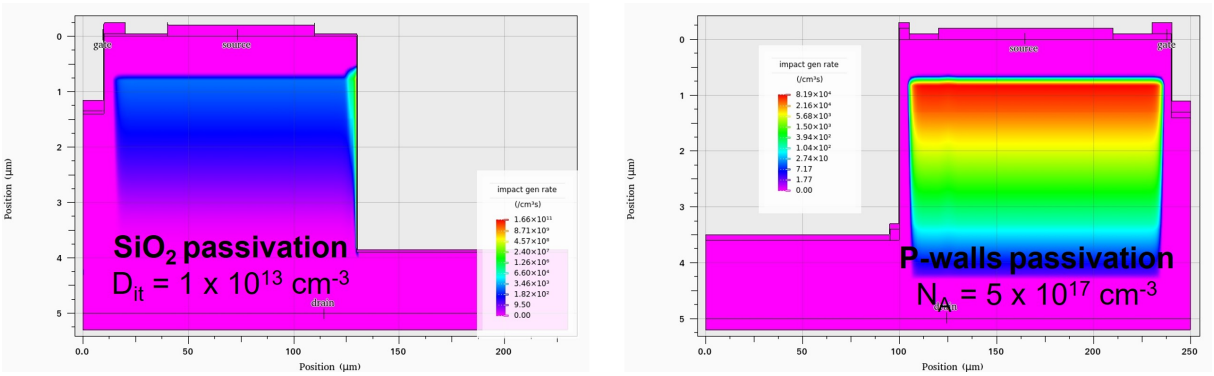


Figure 3.15: Impact ionization at 330 V for a MOSFET with SiO_2 (left) and P-walls passivation (right)

An attempt to fabricate these devices was made at the IEMN. After the etching steps (Sec. 3.1.1), a silicon dioxide hard mask was fabricated to ensure selective regrowth of the p-GaN layer along the mesa walls (Fig. 3.16). Three samples were prepared for 200 nm regrowth with targeted acceptor concentration of $2 \times 10^{17}\,\mathrm{cm}^{-3}$,$4 \times 10^{17}\,\mathrm{cm}^{-3}$ and $6 \times 10^{17}\,\mathrm{cm}^{-3}$.

The MBE regrowth exhibited uniform coverage on the top surface and at the trench bottom, whereas growth on the mesa sidewalls was strongly suppressed, resulting in the formation of small, faceted GaN crystallites. This was attributed to contamination of the mesa sidewalls during processing. A specific cleaning method prior to regrowth must be discussed with MBE experts and incorporated in our process.

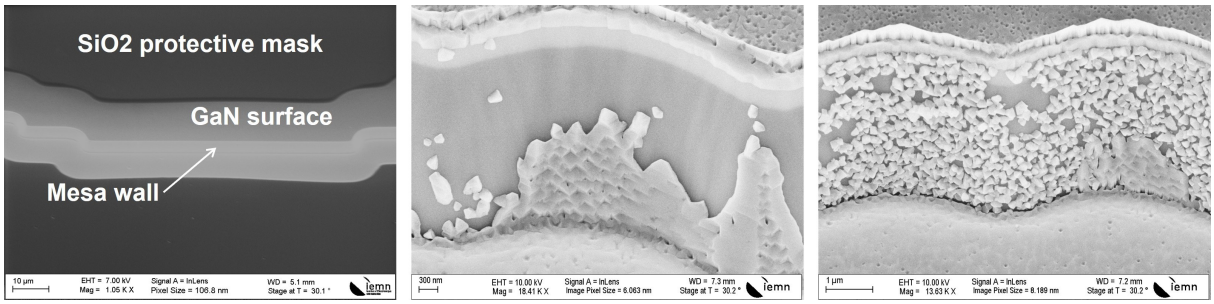


Figure 3.16: Observation of the mesa wall before (left) and after (middle, right) the MBE regrowth steps

The process was not finished on these samples.

Isolation by fluorine implantation

Another approach to mitigate sidewall leakage is to use ion implantation to isolate the devices, instead of relying on a long and potentially damaging mesa etch. Implanting fluorine ions (F^-) into GaN leads to the formation of Ga–F and V_N–F complexes, which act as deep acceptors located approximately 0.4–0.9 eV below the conduction band. These complexes render the implanted region semi-insulating. Isolation achieved in this way can effectively reduce leakage currents, as the induced damage is minimal and does not promote tunneling paths.

To evaluate the feasibility of fluorine implantation, simulations were performed using Silvaco TCAD. The software requires the implantation depth and spatial distribution as input parameters, which were obtained using the open-source simulation tool: Stopping and Range of Ions in Matter (SRIM).

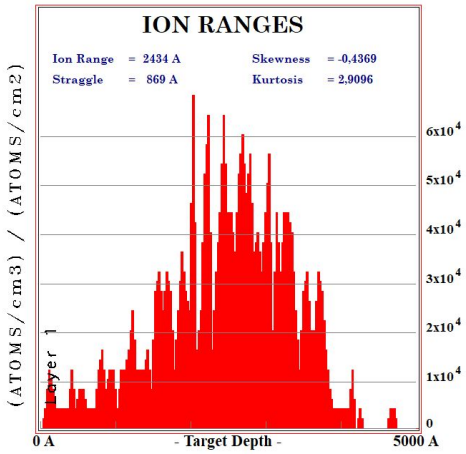


Figure 3.17: Example of a fluorine implantation profile generated using the SRIM software.

SRIM simulates the ballistic implantation of ions in a wide variety of materials. The user can select the ion energy (up to 10 GeV) and incidence angle (0–90°). After a specified number of ion impacts, the software provides statistical data and the resulting implantation depth profile. Figure 3.17 shows an

example of a fluorine implantation profile in GaN simulated by SRIM for 500 incident ions with an energy of 200 keV and an angle of 7°. The output corresponds to an ion volumetric density (cm^{-3}) normalized to the implantation dose (cm^{-2}).

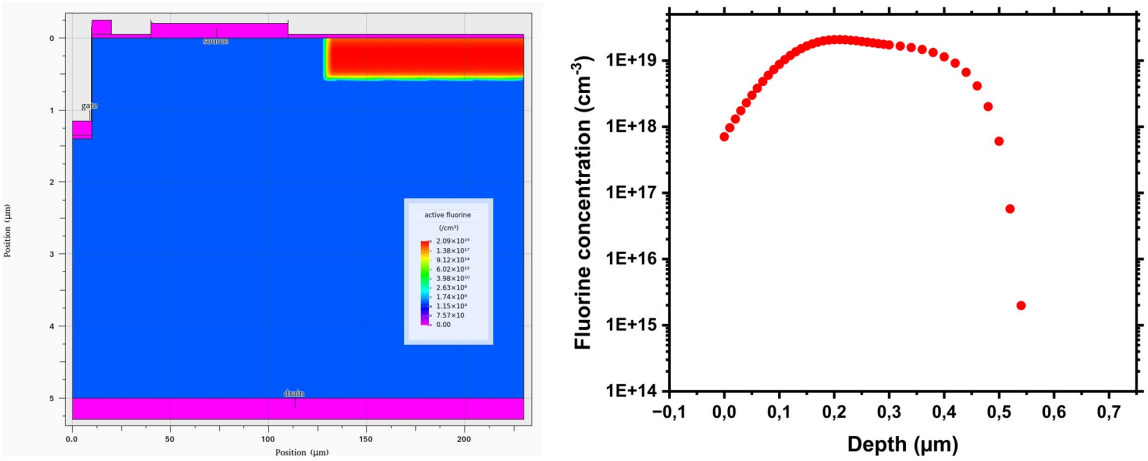


Figure 3.18: Fluorine implantation region (left) and simulated concentration profile (right) obtained using Silvaco TCAD.

To render the top 300 nm n^+ GaN layer semi-insulating, a triple-step implantation process was simulated: a first implantation at 200 keV with a dose of $4 \times 10^{14}\,\mathrm{cm}^{-2}$, a second at 140 keV with a dose of $2 \times 10^{14}\,\mathrm{cm}^{-2}$, and a final one at 80 keV with a dose of $1.2 \times 10^{14}\,\mathrm{cm}^{-2}$. The implanted region started 10 µm away from the source contact and extended laterally over 100 µm. This resulted in a fluorine concentration exceeding $5 \times 10^{17}\,\mathrm{cm}^{-3}$ within the first 500 nm of the epitaxial layer (Fig. 3.18).

Breakdown simulations were then performed on the device incorporating a fluorine-implanted termination (FIT). As shown in Fig. 3.19, the breakdown voltage increased by approximately +85%, while the leakage current decreased by almost two orders of magnitude. The simulated impact ionization coefficient confirms that the fluorine-implanted region effectively suppresses leakage in the drift layer.

These simulation results are consistent with recent experimental findings by Ma *et al.* [189], who fabricated fully vertical GaN-on-Si trench MOSFETs featuring either mesa or fluorine-implanted terminations. The reported breakdown voltages were 567 V and 1277 V, respectively (+125%), for a 7 µm-thick drift layer. This confirms that fluorine-implanted termination (FIT) is a promising technique for effective isolation and edge termination in vertical GaN power devices.

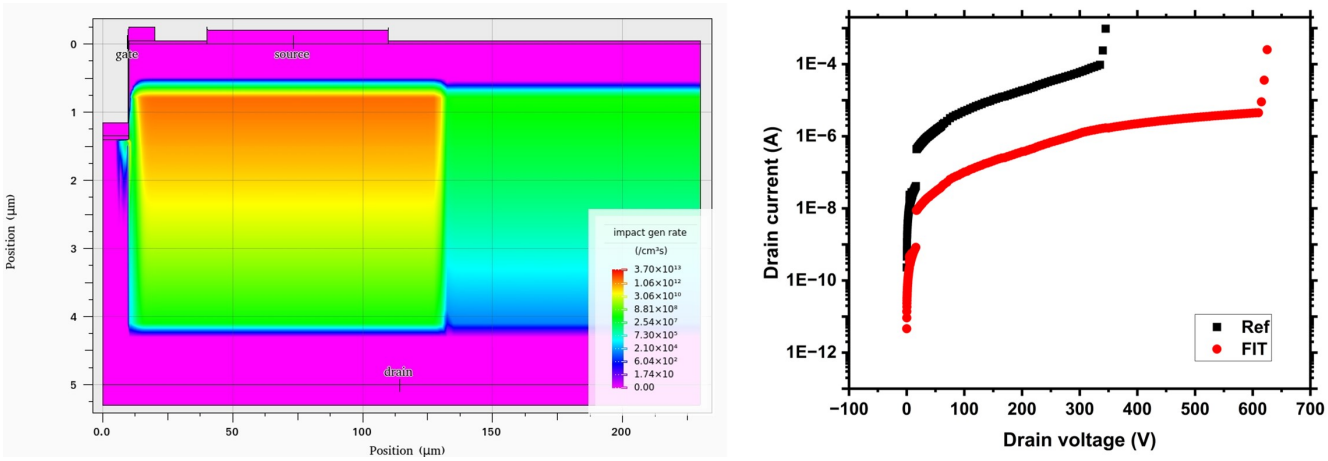


Figure 3.19: Breakdown simulation for the reference structure (mesa + SiO_2 passivation) and the fluorine-implanted termination (FIT).

3.3 Fabrication and measurement of quasi and fully vertical MOSFETs

Both quasi-vertical and fully vertical GaN-on-Si trench MOSFETs were fabricated. This section reports their electrical measurements.

3.3.1 Fabrication and measurement of quasi-vertical MOSFETs

Quasi-vertical trench MOSFETs were fabricated and electrically characterized at IEMN. A circular design was adopted: the smallest transistor has a gate trench diameter of 10 µm, gate contact diameter of 30 µm, gate-to-source and source-to-mesa distances of 10 µm, mesa trench width of 100 µm and drain contact width of 60 µm. Four other transistors were scaled by factors 1.5, 2, 3 and 4 (Fig. 3.20).

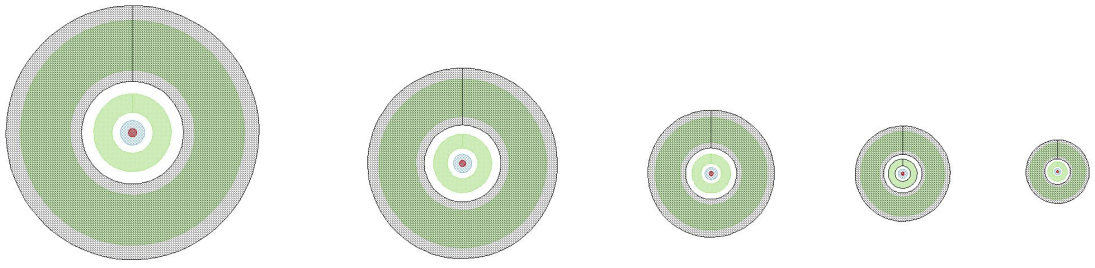
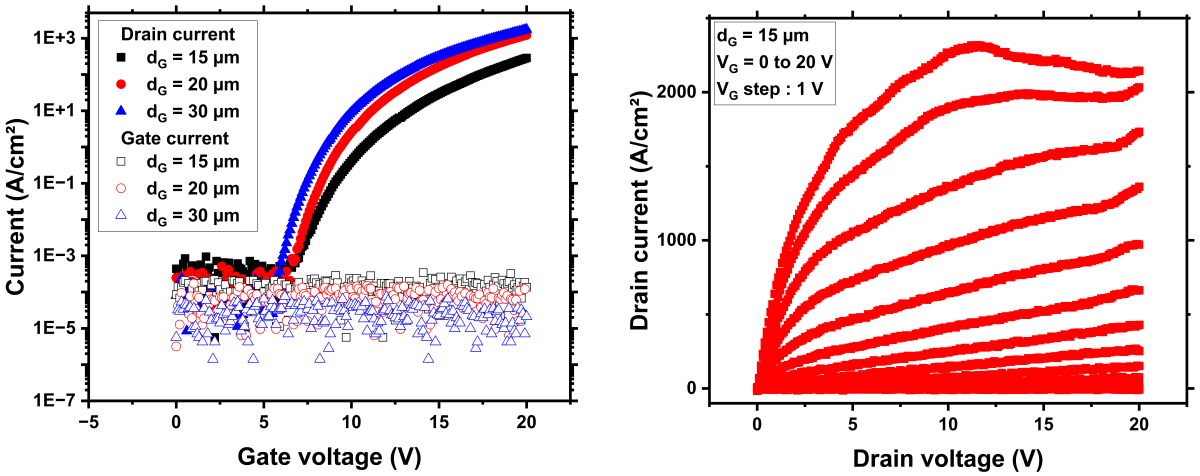


Figure 3.20: Schematics of the quasi-vertical MOSFETs

I_D–V_G measurements were performed on these transistors: V_D was fixed at 10 V and V_G was swept from 0 to 20 V. I_D–V_D measurements were performed by sweeping V_D from 0 to 20 V for fixed V_G values ranging from 0 to 20 V by step of 1 V. These on-state measurements are shown in Figure 3.21.

Our devices displayed a threshold voltage around 6 V (Fig. 3.21a) and the current scaled with the



(a) I_D-V_G curves for various gate diameters.

(b) I_D-V_D curves for a gate diameter of 15 µm.

Figure 3.21: On-state measurements of our quasi-vertical trench MOSFETs. Current normalized by the gate area.

gate surface as expected, with a maximal current density for the smallest gate, corresponding to $\simeq 2.3\,\mathrm{kA\,cm^{-2}}$ (Fig. 3.21b). The $R_{on,sp}$ extracted from the linear regime of I_D–V_D curves ranged from $1\,4$ to $1.7\,\mathrm{m\Omega\,cm^{-2}}$.

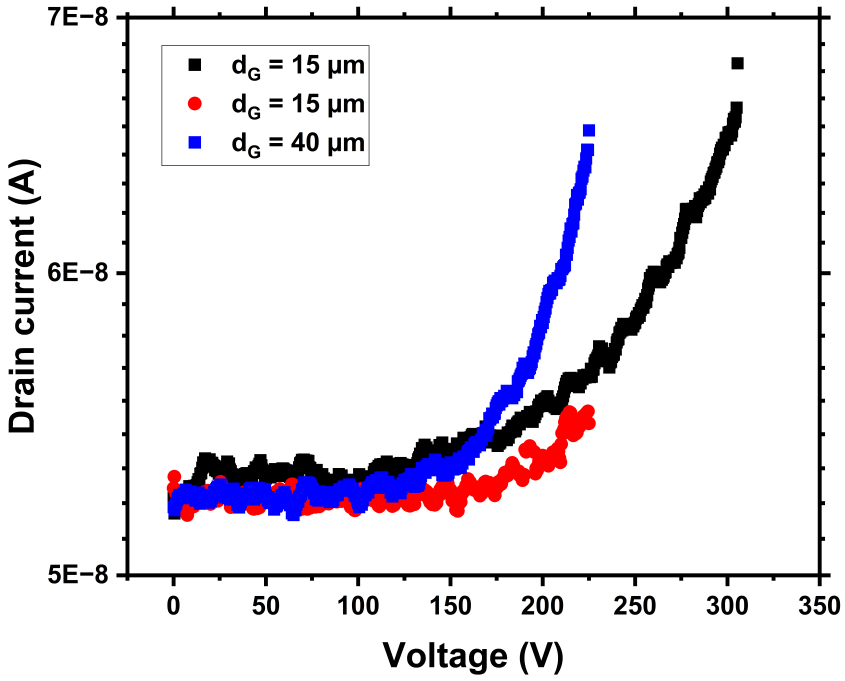


Figure 3.22: Breakdown characteristics of the quasi-vertical MOSFETs

Breakdown voltages were also measured and ranged from 220 to 305 V (Fig. 3.22). This is lower than the state-of-the-art for quasi-vertical GaN trench MOSFET on silicon[115]: 620 V for a 4 µm thick drift layer (Fig. 3.23), but could be improved by adding edge terminations. Our devices display higher

current density ($\simeq 1.3\,\mathrm{kA\,cm^{-2}}$) but a four times lower $R_{on,sp}$.

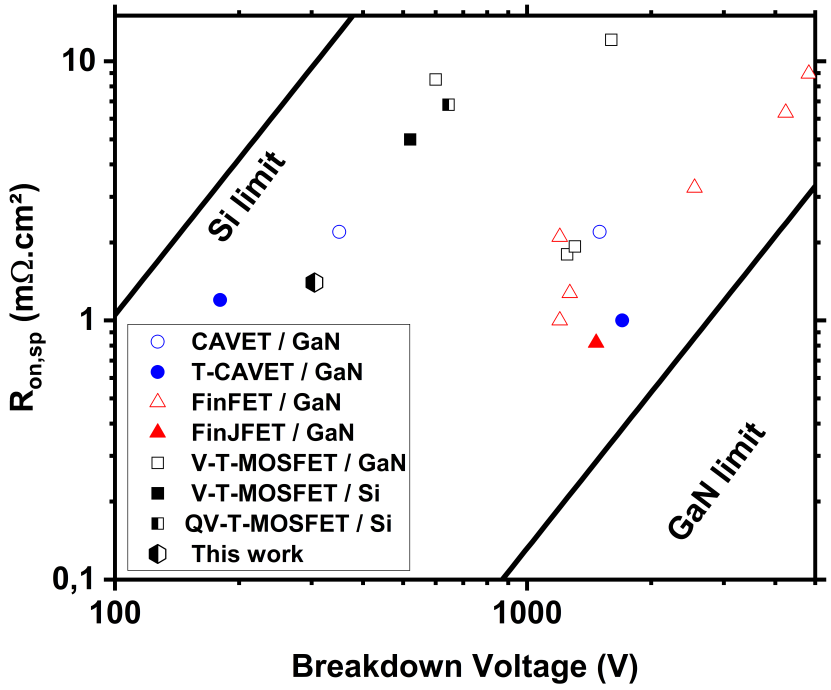


Figure 3.23: Breakdown characteristics of the quasi-vertical MOSFETs

3.3.2 Fabrication and measurement of fully vertical MOSFETs

Fully vertical trench MOSFETs were fabricated and electrically characterized at IEMN. A circular design was adopted, with gate trench diameters of 10, 20, 40, and 60 µm (Fig. 3.24). The gate-to-source and source-to-mesa distances were fixed at 20 µm. Gate contacts were designed 20 µm wider than the gate trenches, and the total transistor diameter was maintained at 300 µm.

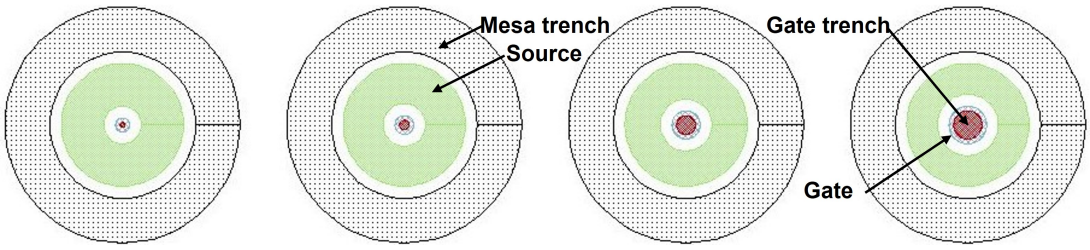
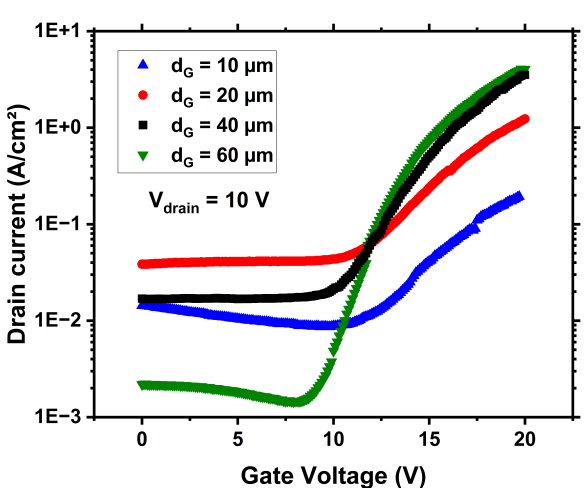


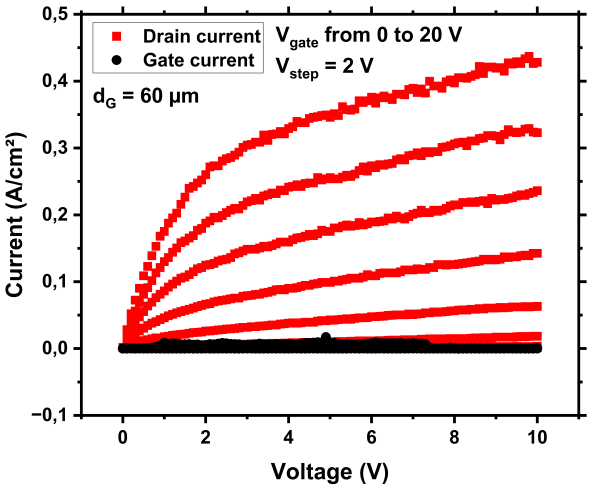
Figure 3.24: Schematics of the fully vertical MOSFETs

Threshold voltage was extracted from I_D–V_G sweeps performed at V_D = 10 V with V_G swept from 0 to 20 V (Fig. 3.25a). As expected [190], the drain current scales with gate area. The off-state drain leakage was on the order of $1\mathrm{e}-10$ to $1\times10^{-8}\,\mathrm{A}$, comparable to that of the quasi-vertical devices. The threshold voltage varied between 8 and 12 V across devices; this spread is likely due to variations in fixed charge

(Q_{f}) and interface-trap density (D_{it}) at the oxide/semiconductor interface.



(a) I_D-V_G curves for various gate diameters.



(b) I_D-V_D curves for a gate diameter of 60 µm.

Figure 3.25: On-state measurements of our fully vertical trench MOSFETs

Extra care was taken during source contact fabrication (including longer deoxidation and stronger agitation during cleaning). Transmission line method (TLM) measurements confirmed an ohmic, low-resistance contact (Fig. 3.27), with a specific contact resistivity of approximately $6 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$. This value alone cannot explain the very low output current (below 1 mA) observed in the devices.

The drain contact can play a non-negligible role in the total device resistance. The etched opening in the silicon substrate exhibits sidewalls with an angle of roughly 60° to the surface (Fig. 3.26). The Ti/Au adhesion/seed layer was deposited by electron-beam evaporation, which is a directional (non-conformal) process. Consequently, only a fraction of the target thickness (20 nm Ti and 100 nm Au on the horizontal surfaces) reaches the sidewalls; for a 60° slope this is on the order of $t \approx t_0 \cos 60^\circ \simeq 0.5\,t_0$, and shadowing can reduce it further. The sidewall film can therefore be very thin or even discontinuous.

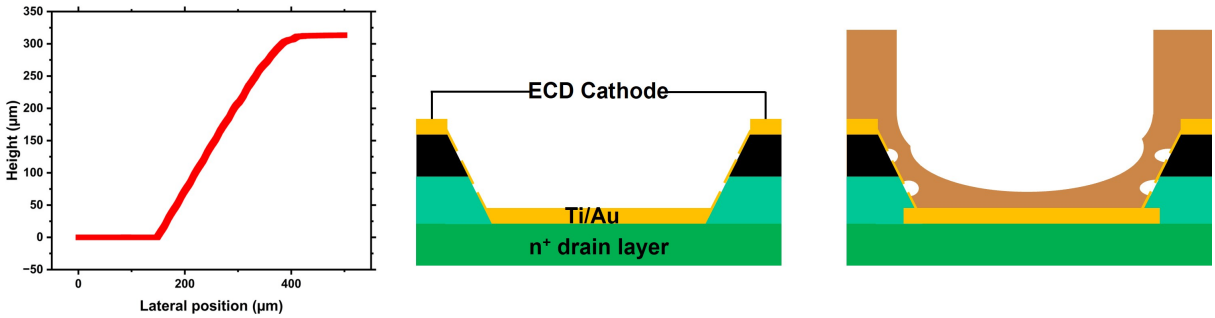


Figure 3.26: Step measurement of the etched wall (left) and schematic of the Ti/Au (middle) and copper layer deposited (right)

During subsequent copper electrodeposition, the cathodic connection is effectively made through this Ti/Au seed. Where the seed is resistive or discontinuous—particularly along the sidewalls and at

the trench bottom—the local current density is reduced (secondary/tertiary current distribution), leading to slower Cu growth, voids, and poor grain quality. The resulting non-uniform copper fill increases the drain-contact resistance and degrades overall device performance.

The I_D–V_D measurements for the largest gate (60 µm) exhibited a maximum drain current of $4\,\mathrm{A\,cm^{-2}}$, corresponding to a specific on-resistance $R_{on,sp}$ between $0.39\,\mathrm{a}$nd $0.93\,\Omega\,\mathrm{cm}^2$, likely caused by the drain contact.

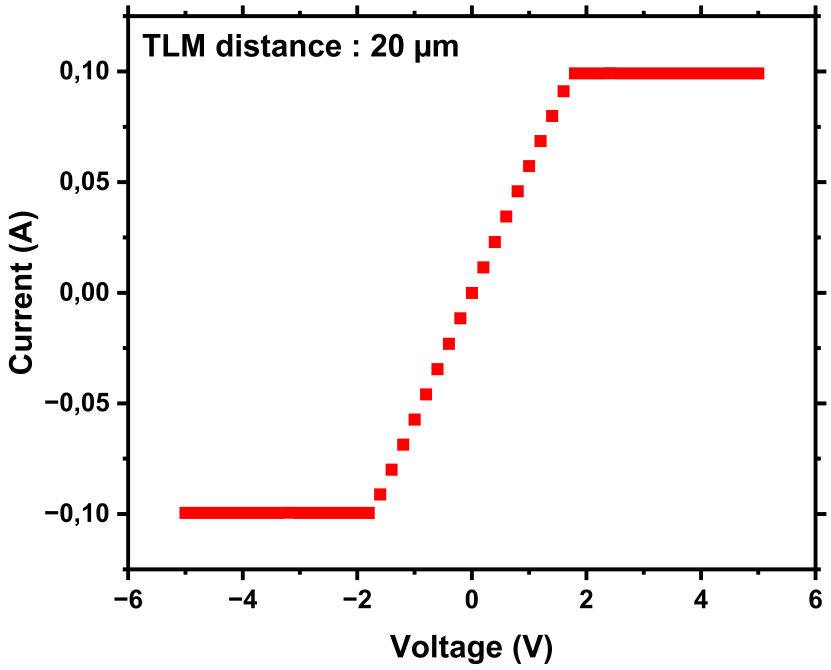


Figure 3.27: Two-terminal measurement between TLM pads separated by 20 µm

The gate leakage currents measured at V_G = 15 V ranged from $1 \times 10^{-8}\,$to $5 \times 10^{-7}\,\mathrm{A}$ across all devices, corresponding to a normalized leakage current of approximately $1 \times 10^{-4}\,\mathrm{A\,cm^{-2}}$. This level is consistent with that expected for non-optimized PECVD SiO_2 deposition, but could be reduced by optimized surface treatments and deposition conditions; down to $1\times10^{-8}\,\mathrm{A\,cm^{-2}}$ according to [191, 192].

The on-resistance R_{on}, extracted from the linear region (low V_D) of the I_D–V_D curves (Fig. 3.25b), varies strongly with the applied V_G. This behavior indicates a channel-limited R_{on} [193, 194]. It suggests a high interface trap density (D_{it}), significant fixed charge (Q_f), and damaged or rough sidewalls; reducing electron mobility and promoting trapping in the channel. These defects were not fully removed by the wet cleaning performed before dielectric deposition, nor by the subsequent dielectric/contact annealing (Sec. 3.1.2). The results indicate that the gate trench etching, surface damage recovery, and dielectric annealing steps require further optimization.

The measured breakdown voltages ranged from 210 to 280 V (independent from the gate size; see Fig. 3.28), consistent with those of the quasi-vertical devices fabricated using the same epitaxial

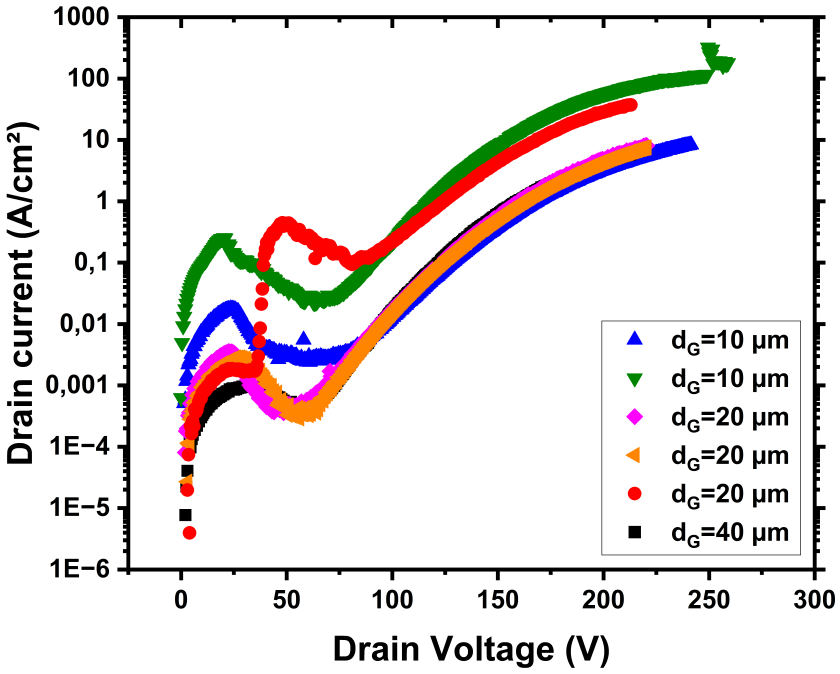


Figure 3.28: Examples of breakdown measurements

structure. Table 3.1 sums up the electrical characteristics measured on our quasi- and fully-vertical structures.

Parameter	Quasi-vertical	Fully vertical	Comment
V_{TH}	8 - 12 V	8 - 12 V	Similar threshold, confirms same p-body quality
$R_{on,sp}$	$\sim 1.4\,\mathrm{m\Omega\,cm^2}$	$\sim 400\,\mathrm{m\Omega\,cm^2}$	Increase due to series limitations
I_D^{max}	$\sim$ kA	$\sim$ A	Strongly reduced current
V_{BR}	$\simeq$ 250	$\simeq$ 250	Comparable breakdown strength

Table 3.1: Summary of quasi and fully vertical device comparison

Conclusion

This chapter established a complete process flow for GaN-on-Si vertical trench MOSFETs within the VertiGo PEPR project framework. Starting from an epitaxial stack optimized for high breakdown voltage, we developed and validated front-side patterning, trench etching, dielectric deposition, and metallization steps. Quasi-vertical structures were used as intermediate test vehicles to benchmark key process modules, particularly the gate dielectric and isolation schemes; before implementing the full backside sequence required for true vertical conduction.

The comparison between dielectric stacks revealed that PECVD SiO_2 alone offered better stability

than the SiO_2/Al_2O_3 bilayer, whose interface generated additional traps and threshold drift. Although Al_2O_3 generally forms high-quality GaN interfaces, hydrogen-rich SiO_2 on top of it produced "border traps" that increased positive fixed charge. Future work should investigate plasma-densified or annealed Al_2O_3 caps to maintain interface quality while enhancing field robustness.

Two complementary isolation strategies were explored. First, MBE p-GaN regrowth was proposed to passivate the mesa sidewalls by forming reverse-biased p–n junctions that laterally deplete the damaged GaN and suppress leakage. Simulations predicted a $\sim$ 20 % increase in breakdown voltage, but experimental regrowth suffered from poor sidewall nucleation due to surface contamination. Improved pre-MBE cleaning or in-situ plasma activation is therefore required.

Second, fluorine implantation (FIT) proved highly effective both in TCAD and experiments, increasing the breakdown voltage by about 85 % and reducing leakage by two orders of magnitude. The FIT process can be directly integrated into the vertical MOSFET flow without major modification, making it the most promising near-term isolation approach.

The fully vertical devices demonstrated correct gate control and stable breakdown around 250 V but exhibited limited drain current ($3\,\mathrm{A\,cm^{-2}}$ to $5\,\mathrm{A\,cm^{-2}}$). Since quasi-vertical devices fabricated from the same epitaxy and using the same etch sequence achieved much higher current density, the degradation was traced to backside process limitations. Non-conformal Ti/Au seed coverage inside deep Bosch-etched vias and the irregular morphology of the thick electroplated Cu layer likely introduced high series resistance and incomplete current spreading. These parasitic effects dominate the on-state behavior while leaving the vertical field distribution, and thus the breakdown voltage, largely unaffected.

The next development steps should focus on:

- **Backside metallization optimization** adopt conformal seed layers (e.g., Ti/TiN or sputtered W), employ pulsed-current Cu ECD, and perform in-situ surface activation before plating.
- **Dielectric and annealing improvements** replace air anneal by N_2 or forming-gas ambient to reduce oxide charge, and evaluate ALD SiO_2 or SiN caps.
- **Enhanced alignment control** implement stepper-based photolithography or self-aligned gate patterning to minimize overlap variation.
- **Thermal and electrical co-optimization** integrate the fitted parameters into TCAD to predict trade-offs between on-resistance, breakdown, and self-heating.

In summary, this work demonstrates **the technological feasibility of vertical GaN-on-Si trench MOSFETs** using an entirely in-house process at IEMN. All critical modules such as trench etch, gate

dielectric, isolation, and backside contact have been established and validated. The remaining performance gap is primarily technological rather than intrinsic to the vertical architecture. Once the backside metallization and dielectric processes are refined, the devices are expected to achieve kilovolt-class blocking voltages with sub-$10\,\mathrm{m\Omega\,cm^{-2}}$ specific on-resistance, thereby extending GaN-on-Si technology beyond lateral HEMTs into the high-power conversion domain.

Chapter 4

Outlook for V-T-MOSFETs

Vertical GaN trench MOSFETs (V-T-MOSFETs) promise kilovolt-class blocking with low specific on-resistance, but their fabrication toolbox remains less mature than that of Si and SiC. In particular, plasma damage during trench formation, interface traps in the MOS stack, and electric-field crowding at trench corners and device edges still limit reliability and performance. Moreover, the modest effectiveness of p-type doping in GaN constrains electrostatic design options that are routine in competing technologies.

This chapter proposes a set of process and design strategies to close that gap. The chapter is organized as follows. Section 4.1 optimizes gate fabrication, covering ICP–RIE trench etching, post-etch surface conditioning, and conformal dielectric stacks. Section 4.2 addresses field and current crowding, detailing the design, operation, and trade-offs of p-shield and current spreading layer (CSL) structures, and extends to guard rings and superjunction architectures for higher breakdown margin. The final section explores suitable p-type materials beyond GaN and their integration pathways to expand the design space of V-T-MOSFETs.

4.1 Gate fabrication optimization

This section details the optimization of gate formation in GaN trench MOSFETs, focusing on etching, surface conditioning, and dielectric deposition.

The gate trench defines the electrostatic control of the vertical MOSFET and must combine high anisotropy, smooth sidewalls, and minimal plasma damage. A high-quality metal–oxide–semiconductor (MOS) gate stack is critical to the operation and performance of MOSFETs. Accordingly, the gate process should be optimized to reduce the oxide/semiconductor interface defect density and mitigate electric-field crowding at trench corners, both of which strongly affect device behavior [194, 195]. Sharp

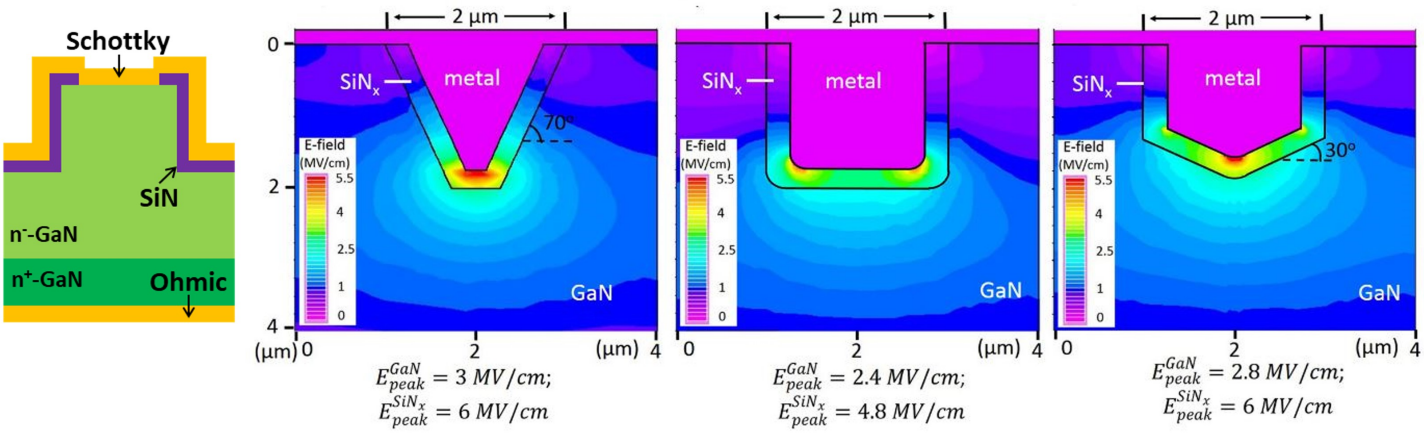


Figure 4.1: Schematic of the Schottky barrier diodes used for breakdown measurements (left) and simulated electric-field distribution at 600 V for three trench shapes with 250 nm PECVD SiN layer.

trench corners produce higher peak electric field than rounded corners at the same applied voltage (Fig. 4.1), which can trigger premature gate-induced breakdown. Zhang et al. [195] reported breakdown voltages of 150, 350, and 500 V in vertical Schottky diodes with different trench profiles, and showed that a flat-bottom trench with rounded corners minimizes the peak field and yields the highest breakdown voltage.

Additionally, traps in the MOS stack (interface and oxide/border states) can alter the threshold voltage, degrade channel mobility via Coulomb scattering, reduce the output current and the breakdown voltage, and increase $R_{\mathrm{on,sp}}$ [194]. Depending on their polarity and occupancy, these traps may shift V_{TH} either upward (e.g., acceptor-like traps filled with electrons) or downward (e.g., donor-like traps emptied under positive gate bias). Traps can also enable trap-assisted tunneling (TAT), further impacting conduction and reliability [196]. Therefore, minimizing trap density is essential to ensure proper operation of V-T-MOSFETs. Several options, discussed below, can be used to achieve a rounded-corner, low-trapping gate trench.

4.1.1 Trench gate etching improvement

The most common GaN dry-etch method is ICP–RIE, which proceeds predominantly via chlorine chemistry: Cl radicals form volatile $GaCl_x$ (e.g., $GaCl_3$), while nitrogen leaves as N_2 (or NCl_x under some conditions). The ICP coil sustains a plasma that produces a mixture of Cl radicals and Cl-bearing ions from Cl_2 gas, and an RF bias applied to the substrate electrode accelerates ions toward the chuck (see Fig. 4.2 - [197]).

$$GaN(s) + 3\ Cl\cdot(g) \rightarrow GaCl_3(g) + 1/2\ N_2(g) \tag{4.1}$$

Equation 4.1: chemical reaction between chlorine radicals and GaN (overall stoichiometry shown; actual surface pathways may involve intermediate GaCl and $GaCl_2$ species).

Increasing ICP coil power raises plasma density and the dissociation of gas molecules, boosting the fluxes of both Cl radicals and ions. This primarily increases the chemistry-limited component of the etch rate without, by itself, increasing ion energy at the surface. Increasing the applied RF bias increases ion energy and directionality. Higher RF bias generally increases etch rate and anisotropy, but also causes more lattice damage (a thicker altered layer), including nitrogen depletion, point-defect creation, and roughening, as well as greater mask erosion and redeposition [198].

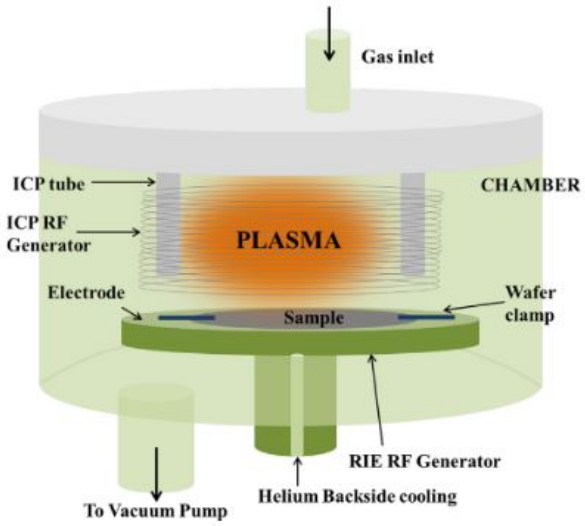


Figure 4.2: Schematic of an ICP-RIE reactor

Purely chemical (Cl_2-based) removal is slow. Inert assisting ions such as Ar or He can be added to the gas mix to enhance etching by breaking Ga–N bonds via physical impact and by promoting desorption of reaction products. Thus, GaN etching in ICP–RIE is typically ion-enhanced chemical etching rather than pure sputtering or purely chemical etching. The trade-off for the higher etch rate is the damage induced by these assisting ions.

In practice, to keep a low RF bias (< 100 V) and minimize damage while preserving anisotropy, a fraction of BCl_3 is often added in partial substitution for Cl_2. This reduces lateral etching: BCl_3 (and fragments such as BCl) are strong Lewis acids that bind O/H_2O, forming volatile boron oxychlorides. This removes native oxides and adsorbed water and suppresses Ga–O–Cl residues that can roughen or passivate the surface, leading to smoother sidewalls and less lateral attack at a given bias [199]. With suitable ratios and low pressure, B-containing species can also create an ultrathin sidewall-conditioning layer (and, with available N, BN-like terminations), which inhibit lateral etching [200]. The trade-off is a possible reduction in peak etch rate and lower selectivity to SiO_2 masks.

Two other parameters strongly influence the outcome. First, pressure: typical ICP pressures are a few to a few tens of mTorr. Lower pressure narrows the ion angular spread and improves anisotropy at a given bias, while higher pressure increases scattering, makes the process more neutral-driven (more isotropic), and can hinder by-product desorption. Second, chuck temperature: increasing substrate temperature accelerates chemical kinetics and product desorption, limits redeposition, and often allows a reduced RF bias for the same etch rate, thereby reducing damage.

Parameter (increase)	**Etch rate**	**Selectivity (SiO_2 mask)**	**Induced damage**	**Rationale**
ICP power	$\uparrow$	$\uparrow$ / $\approx$	$\approx$	$\uparrow$ radical & ion flux
RF bias power	$\uparrow$	$\downarrow$	$\uparrow\uparrow$	$\uparrow$ anisotropy, ion energy $\Rightarrow$ $\uparrow$ chemistry assistance, sputter/mask erosion
Pressure	$\downarrow$ / $\approx$	$\uparrow$ / $\approx$	$\downarrow$ (per ion)	$\downarrow$ mean free path, $\uparrow$ ion angular spread, $\downarrow$ anisotropy
Chuck temperature	$\uparrow$	$\uparrow$	$\downarrow$ (net)	$\uparrow$ volatility/desorption of $GaCl_x$, surface kinetics $\Rightarrow$ $\uparrow$ selectivity, $\downarrow$ damage (reduced bias for the same etching rate).

Legend: $\uparrow$ increase; $\downarrow$ decrease; $\approx$ minimal change. Trends are qualitative and tool-dependent.

Table 4.1: Qualitative impact of ICP–RIE parameters (excluding plasma composition) on GaN etching outcomes

Our current ICP–RIE recipe uses a Cl_2/Ar mixture with a flow ratio of 1:3 (Ar-rich), an ICP (source) power of 600 W and an RF (bias) power of 100 W, at a pressure of 8 mTorr and a chuck temperature of 17 $^\circ\mathrm{C}$. Under these conditions we obtain an etch rate of approximately $300\,\mathrm{nm\,min^{-1}}$ and mesa sidewall angles of 75–80°. This enables mesa fabrication in reasonable etch times; however, the high Ar fraction and the measured dc self-bias of $\sim$270 V indicate a sputter-assisted regime that is not optimal in terms of plasma-induced damage. A Cl_2/BCl_3 recipe (Cl_2-dominant with a small BCl_3 fraction) can deliver similar etch rate and anisotropy at lower RF bias—thereby reducing sidewall damage—albeit with reduced selectivity to SiO_2 masks [200]. This loss in selectivity could be regained by using higher temperature and lower pressure.

Another improvement for deep etching with Cl_2/BCl_3 is to use a Ni hard mask instead of the currently used SiO_2 mask. Khadar et al. [114] showed that a Ni mask leads to smoother gate sidewalls and nearly doubles the electron channel mobility compared with SiO_2. Nickel is more resistant to BCl_3 attack than SiO_2, reduces sputtering (which helps preserve smooth sidewalls), and, being metallic, dissipates heat and mitigates charging effects that can cause notching. The main drawbacks are a slightly more complex flow - since a thin Ti/Cr adhesion layer is typically required before Ni deposition - and potential metal redeposition (“fencing”), which calls for a brief post-etch clean to remove any Ni from the sidewalls (along with standard contamination control).

4.1.2 Post-etching treatment

After anisotropic ICP–RIE, the trench edge and sidewalls typically contain a thin altered layer (few to tens of nanometers) with defects and slight roughness. A mainstream approach in the literature to skim off this damaged material with minimal additional damage and to round sharp corners, is a short, isotropic wet step. In practice, some works employ hour-long immersions in hot alkaline solutions (e.g., KOH or TMAH at $60\,^{\circ}\mathrm{C}$ to $90\,^{\circ}\mathrm{C}$) on Ga-polar GaN to smooth edges and increase the radius of curvature without large changes in trench depth [114, 201–203]. However, once the post-etch altered layer is removed, alkaline etching becomes strongly crystallography- and defect- selective: on monocrystalline GaN, it preferentially attacks regions around threading dislocations and exposes low-index facets. Consequently, the etch time must be carefully limited to avoid pit growth and sidewall faceting [203, 204]. Figure 4.3 [205] shows the sidewalls of a GaN Multiple Quantum Wells (MQW) light emitting diode (LED), whose c-plane facets were exposed by TMAH exposure. Because the damaged-layer thickness is usually not known a priori and can vary with plasma conditions, this step is best implemented as short, calibrated dips with intermediate inspection (e.g., SEM/AFM or PL), rather than a single long soak.

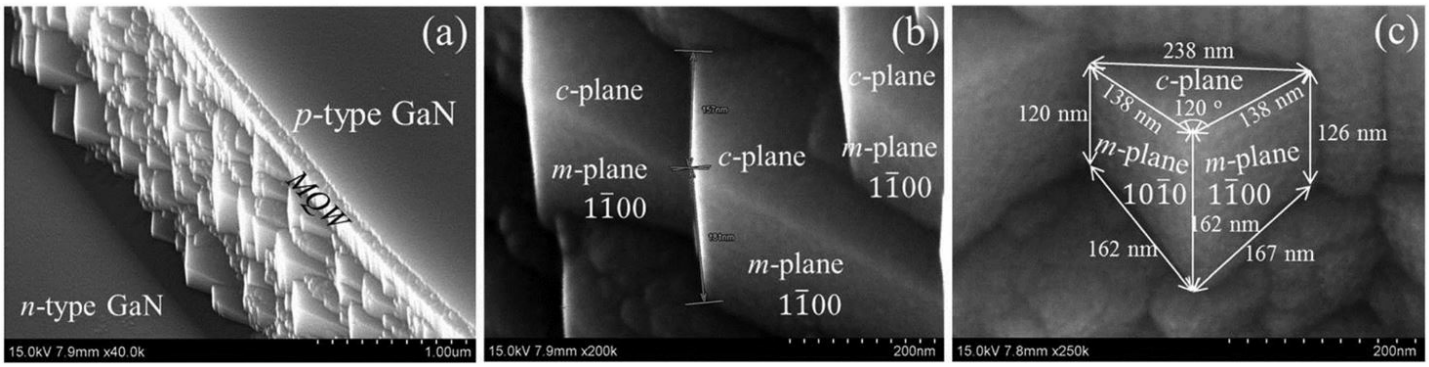


Figure 4.3: Exposed c-plane facet after TMAH etching on a GaN LED

A simpler alternative is a two-step, chemistry-limited surface “polish” cycle that repeats: gentle oxidation of the GaN surface to form a thin GaO_x layer, followed by oxide removal. Oxidation can be done with a brief downstream O_2 plasma, UV/ozone, or a dilute oxidizing wet soak (e.g., H_2O_2-containing mixture). The resulting GaO_x is then removed with an oxide-selective dip such as BOE (HF/NH_4F) or a dilute HCl rinse [206]. Each cycle removes only a few nanometers in an isotropic, damage-minimizing manner, effectively “resetting” the outermost surface and rounding the trench corner. This approach is compatible with most device flows and avoids ion damage; however, BOE will attack exposed SiO_2 (masks or gate dielectrics), so masking and timings must be planned accordingly.

Both methods affect the trench shape and must be well controlled to obtain rounded corners. To reduce damage without altering the trench shape, a low-energy, remote N_2 plasma exposure (or N_2/forming-

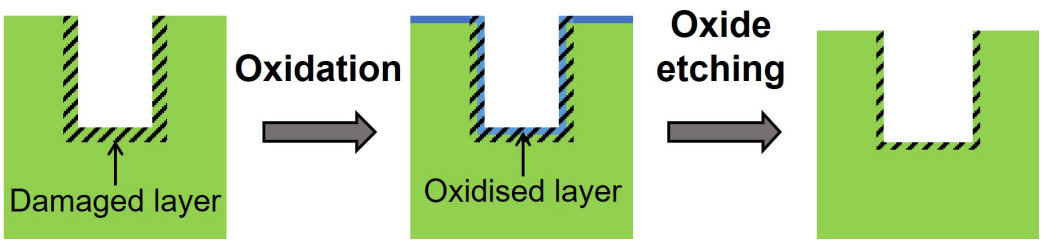


Figure 4.4: Schematics of the damage layer removal steps using oxidation and oxide etching

gas) can passivate dangling bonds, remove chlorine residues, and lightly nitridize the topmost surface, lowering surface-state density without adding sputter damage [207]. To keep it gentle, the plasma should be downstream/inductively generated with negligible substrate bias, short duration (tens of seconds to a few minutes), and low to moderate source power. A subsequent inert or forming-gas anneal (e.g., $350\,^{\circ}\mathrm{C}$ to $600\,^{\circ}\mathrm{C}$, a few minutes, tool- and stack-dependent) further heals shallow defects and desorbs weakly bound species. Together, this sequence reduces leakage and variability associated with the post-etch altered layer while preserving etched geometry. Care must be taken with temperature limits set by any nearby metals or dielectrics (e.g., PECVD SiN).

4.1.3 Dielectric deposition optimization

The gate dielectric is a critical component of the trench MOSFET, as it governs both the electrostatic coupling to the channel and the long-term device reliability. Because GaN cannot form a stable thermal oxide, the dielectric must be deposited ex situ with controlled interface chemistry. In this work, several materials and deposition techniques were considered, with attention to conformality, interface state density, and breakdown strength. A suitable gate dielectric must simultaneously provide:

- a **large conduction-band offset** to minimize electron tunneling,
- **low defect density** to limit charge trapping, and
- **excellent conformality** inside narrow trenches.

Among the materials in Fig. 4.5, the most widely used across microelectronics are SiO_2, SiN_x, HfO_2, and Al_2O_3. Other dielectrics have been explored in GaN MIS/HEMT structures [208–210], but often require careful interface engineering to avoid higher leakage and/or increased interface-trap density.

Depositing an oxide directly on etched GaN is sub-optimal because it tends to form Ga–O bonds and sub-oxides at the first monolayers, which act as interface traps (raising D_{it}) and can introduce fixed charge. A common remedy is to insert an ultrathin ($0.5\,\mathrm{nm}$ to $2.0\,\mathrm{nm}$) nitride-like interfacial layer (IL) before the main gate dielectric. Reported ILs include SiN_x [211], AlN [212, 213], and AlON (AlO_xN_y)

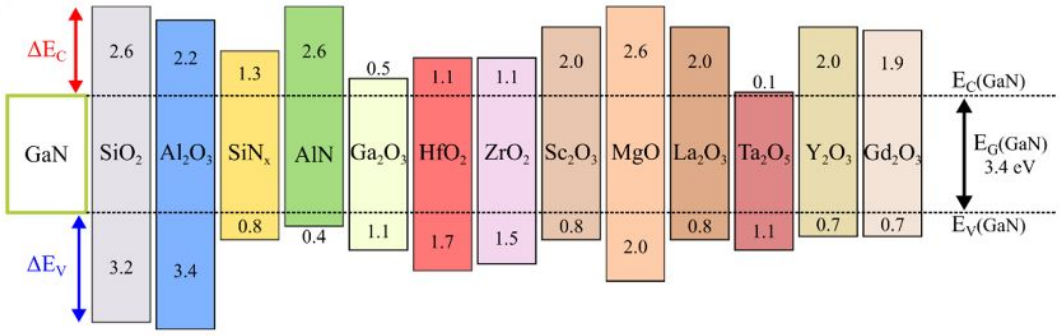


Figure 4.5: Schematic of the bandgap alignment of possible gate dielectrics with GaN

[214]. These interfacial layers suppress Ga–O formation and thereby reduce D_{it}; among them, optimized ultra-thin AlN generally yields the lowest interface trap densities when grown under gentle (remote/low-energy) conditions. The effective oxide thickness (EOT) and interface-trap density must be optimized together; typically $D_{\mathrm{it}} \simeq 1 \times 10^{12}\,\mathrm{cm}^2\,\mathrm{eV}^{-1}$ to $1 \times 10^{13}\,\mathrm{cm}^2\,\mathrm{eV}^{-1}$ is required to achieve stable threshold voltage below 15V. AlON offers nearly comparable D_{it} with a more forgiving process window, and SiN_x is typically less effective at the GaN channel interface but is robust and easy to deposit.

On top of the nitride IL, Al_2O_3 is usually favored over SiO_2 because its higher dielectric constant ($k \approx 8$–9) allows a thicker physical oxide at the same gate capacitance, thereby reducing peak electric field and gate leakage in the trench corners. If further electric-field reduction is needed, a very high k dielectric (HfO_2, k = 24 - 25) can be deposited on top of the Al_2O_3.

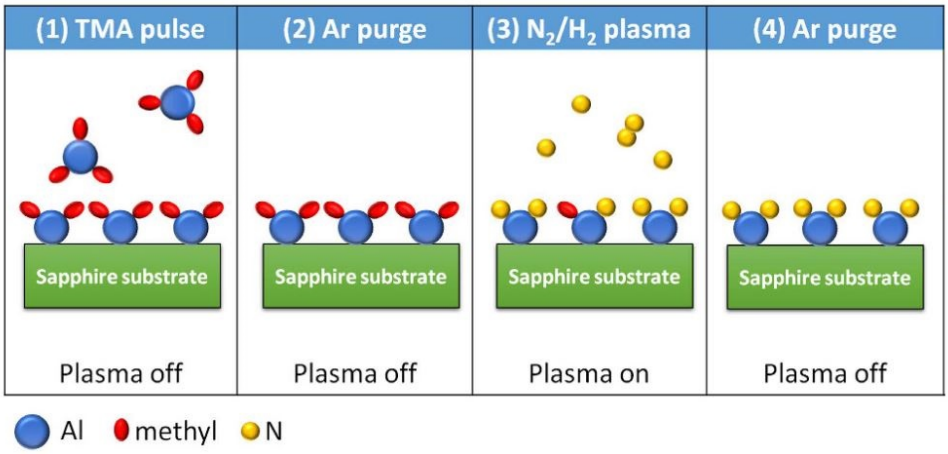


Figure 4.6: Schematic of ALD of AlN using trimethyl aluminum (TMA) and N_2/H_2 plasma

Deposition method and conditions also play a critical role in the trap density of the MOS stack. Atomic layer deposition (ALD - see Fig. 4.6) is the workhorse for deep trenches due to its self-limiting surface chemistry and excellent conformality. Thermal ALD Al_2O_3 (e.g., TMA/H_2O) at 150–300 $^{\circ}\mathrm{C}$ generally yields low roughness and good step coverage; however, H_2O-based cycles can incorporate hydrogen,

contributing to border traps that show up as positive-bias and temperature instability (PBTI) if pre-clean and post-anneal are not optimized. Using stronger oxidants (ozone) densifies the film and can reduce leakage, but may increase fixed charge or deep traps if the surface is not well prepared.

Plasma enhanced ALD (PEALD) enables lower temperature and can improve film density, yet plasma exposure near the interface risks generating defects; a remote plasma geometry and minimized ion energy are preferred for deposition on GaN.

PECVD dielectrics (SiN_x, SiO_2, AlN, AlON) offer high throughput and decent conformality at a low thermal budget, but typically contain higher hydrogen and exhibit more fixed charge/oxide/border traps than ALD analogues. They are therefore excellent for passivation, liners, and field plates; when used in a gate stack, a very thin ALD interfacial layer (e.g., Al_2O_3) can buffer the GaN interface and lower D_{it}.

LPCVD films (e.g., high-temperature SiN_x) are dense and robust but require higher thermal budgets that may conflict with metal stacks or dopant activation schedules.

Independent of the dielectric, surface preparation dominates interface quality. Effective flows combine an oxidize step (UV/ozone, mild O_2 plasma, or brief piranha) to form a thin GaO_x, a selective oxide strip (HF/BOE or dilute HCl) to remove the damaged/contaminated skin, and optionally a gentle nitridation (remote N_2/NH_3 plasma or ultrathin ALD AlN). This sequence lowers interface trap density (Dit), suppresses hysteresis, and reduces fixed charge drift. In trench geometries, rounded corners and a slightly thicker oxide at the trench bottom further reduce local field, which indirectly relaxes trap-driven stress (PBTI/NBTI) in the gate stack.

Dielectric / method	**Conformality (trench)**	**Trap tendencies (qual.)**
ALD Al_2O_3 (thermal)	Excellent	Low Dit with good prep; some border traps (H incorporation)
PEALD Al_2O_3 (remote)	Excellent	Low–moderate (depends on plasma exposure)
ALD HfO_2 (as cap)	Excellent	Higher trap sensitivity (PBTI) if directly on GaN
ALD/PEALD AlON	Very good	Often lower fixed charge vs pure Al_2O_3
PECVD SiN_x	Very good	Higher fixed charge / Dit if used as gate
PECVD SiO_2	Very good	Moderate traps; low k drives high E_{ox}

Table 4.2: Deposition options for GaN trench dielectrics and qualitative impact on traps.

A mild post-deposition anneal (PDA) in inert or forming gas (e.g., 300–500 $^{\circ}\mathrm{C}$, stack-dependent) helps drive out hydrogen, rearrange weak bonds, and reduce border traps. For high-k caps (HfO_2), a thin Al_2O_3 interlayer at the GaN interface plus a moderate PDA improves bias stability. Excessive anneal temperature can shift fixed charge or crystallize high-k films, so thermal budgets should be validated on

witness structures (C–V hysteresis, bias-temperature stress,...).

Ideally, low-damage anisotropic ICP-RIE etching followed by isotropic corner rounding, oxidative plasma treatment, and GaO_x removal with BOE should yield low-damage surfaces and a rounded-corner gate trench. Depositing an Al_2O_3 / AlN (IL) stack on top of that should lead to more efficient operation. By optimizing the gate fabrication to reduce traps and fixed charges, channel resistance will decrease, leading to better on-state performance: higher current, lower $R_{on,sp}$ and more stable V_{th}. The optimized MOS stack can also help reduce leakage and electric field peak, thus enhancing the gate-induced breakdown voltage of our devices.

4.2 Field and current crowding management

Beyond the critical gate-fabrication steps, additional strategies can further improve device performance. This section focuses on managing current flow and electric-field distribution throughout the structure to enhance both on and OFF-state behavior. The goals are to avoid localized hot spots by promoting uniform current spreading (mitigating rapid self-heating) and to minimize field crowding by keeping the electric field as uniform and as low as possible, thereby preventing premature breakdown. Two complementary structures are generally adopted: the **p-shield** and the **current spreading layer (CSL)**.

4.2.1 P-shield

In a trench MOSFET, the electric field tends to crowd at the trench bottom and corners, where the gate oxide is most vulnerable. A p-shield is a locally p-type region (typically tied to source) placed beneath the trench gate bottom and extending slightly under the sidewalls (Fig. 4.7). Its purpose is to electrostatically screen the gate from the drain-side field and to shape the depletion region so that the peak field shifts from the gate oxide into the drift region.

With the p-shield at (approximately) source potential, the p^+/n junction between the shield and the underlying n-type drift is reverse biased in the OFF-state. The resulting depletion region expands upward toward the trench bottom, intercepting field lines that would otherwise terminate on the gate electrode across the oxide. In Poisson's equation form, $\nabla\cdot(\varepsilon\nabla\phi) = -\rho(\phi, N_D, N_A)$: introducing a p-type pocket increases the local space charge ($\rho \approx -qN_A$ in depletion), which redistributes equipotentials and reduces the normal electric field E_{ox} in the oxide at the trench bottom/corners. For a given gate/drain bias, the p-shield thus lowers E_{ox} and moves the field maximum deeper into the semiconductor, increasing gate-dielectric reliability (lower gate-induced breakdown risk, improved time-dependent dielectric breakdown, TDDB, margin).

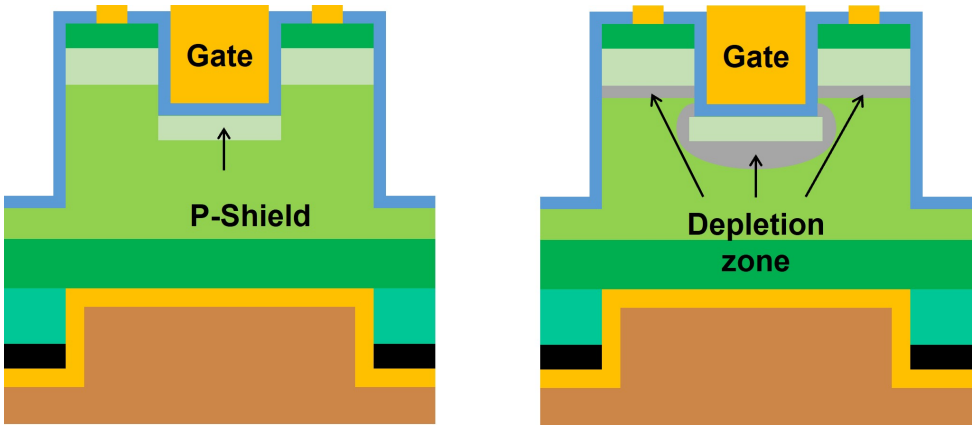


Figure 4.7: Schematic of a p-shield and the associated depletion region.

Because the p-shield is at source potential, it also acts as an electrostatic screen between the gate and drain. The effective gate–drain (Miller) capacitance C_{gd} is reduced: part of the gate fringing field that formerly coupled to the drain now couples to the shield (and hence to source). In a small-signal view, the capacitance network re-partitions such that C_{gd} decreases while C_{gs} (gate–shield/source) increases slightly. The net effect is reduced gate charge Q_{gd} and a shorter Miller plateau, improving switching speed and dv/dt robustness. In the time domain, this screening also mitigates drain-induced transient fields at the gate oxide, which helps suppress trap charging and dynamic R_{on} drift.

In the on-state, the p-shield is designed to be fully (or nearly fully) depleted so that it does not constrict the conduction throat under the trench. Co-optimization with the current-spreading layer (CSL, Sec. 4.2.2) and p-body spacing prevents excessive JFET-like pinch. If the p-shield is too deep or too highly doped, the neutral region shrinks in on-state, raising access/JFET resistance and increasing $R_{\mathrm{on,sp}}$. Thus, shield doping and depth are chosen to balance OFF-state field relief and on-state conductivity.

A low-impedance tie to source is the default because it fixes the shield potential, yielding predictable field lines and avoiding charge-storage effects. A floating shield can accumulate charge via traps or impact-generated carriers, causing history-dependent fields and variability in V_{TH} and R_{on}; it is generally avoided in power devices aimed at robust switching.

Key parameters are the shield depth and lateral extent under the gate bottom, the acceptor concentration N_A in the shield, and the shield-dielectric thickness (often slightly thicker than the gate oxide at the bottom). Increasing N_A or extending the shield enlarges the OFF-state depletion region and further reduces E_{ox} and C_{gd}, but pushes against on-state R_{on} and can add charge to C_{iss}. The practical target is a shield that is strongly depleted in OFF-state (for field control) yet offers minimal constriction in on-state. Rounded trench corners and, where feasible, a thicker bottom oxide (and/or a higher-k cap)

complement the p-shield by further lowering peak E_{ox}.

Simulations indicate that an acceptor density between $5 \times 10^{16}\,\mathrm{cm}^{-3}$ and $5 \times 10^{17}\,\mathrm{cm}^{-3}$ and a vertical separation of 100 - 200 nm below the gate dielectric provide optimal field balancing for 600 - 1200 V devices. Higher doping ($> 10^{18}\,\mathrm{cm}^{-3}$) can cause excessive depletion capacitance and increased gate charge, degrading switching speed. The lateral extent of the p-shield must exceed the gate width by at least 0.5 µm to avoid edge crowding at the trench corner.

Properly implemented, the p-shield improves OFF-state breakdown margin, reduces gate leakage and C_{gd}, stabilizes the gate stack against PBTI and transient charging, and enhances short-circuit/SOA robustness. P-shield fabrication may be challenging in GaN trench MOSFETs, as MBE p-GaN regrowth is complex on etched surfaces and requires specific cleaning prior to deposition. While p-shielded vertical SiC MOSFETs have been fabricated [215], GaN realizations remain mostly theoretical or at early demonstration stages [216–218].

4.2.2 Current spreading layer

In a vertical MOSFET, the conduction path from the inversion channel at the trench sidewall to the drift region is often constricted beneath the p-body regions (the “JFET region”; Fig. 4.8). A current-spreading layer (CSL) is a thin, lightly-to-moderately doped n-type layer embedded above the drift (typically just below the trench bottom and p-body) whose conductivity is higher than the drift region. The CSL provides a low-resistance lateral path that spreads current from adjacent cells before it turns vertical, thereby reducing access/JFET resistance and current crowding.

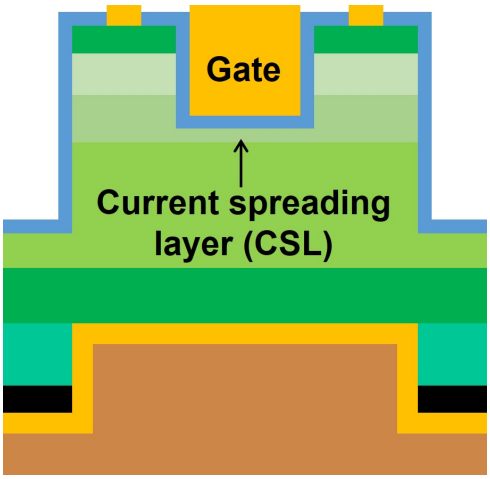


Figure 4.8: Schematic of a CSL in a vertical MOSFET.

In the OFF-state, the p-body/CSL/drift stack is reverse biased. The CSL is chosen so that it is fully depleted (or nearly so) at the rated drain voltage. Full depletion ensures that the CSL does not form a

leakage shunt, and that the blocking field is supported in the drift region as intended. Properly designed, the CSL smooths equipotentials under the trench bottom, reducing local field crowding next to the gate oxide and complementing p-shield action.

When the device is on, the channel injects electrons into the region beneath the trench. Without a CSL, the narrow "throat" between neighboring p-bodies behaves JFET-like: its depletion boundaries encroach into the conduction path, increasing series resistance. The CSL offers a lateral, higher-conductivity sheet that spreads current under multiple cells before it enters the vertical drift (Fig. 4.9). This reduces the peak current density and the voltage drop in the constricted throat, lowering the access/JFET component of $R_{\mathrm{on,sp}}$.

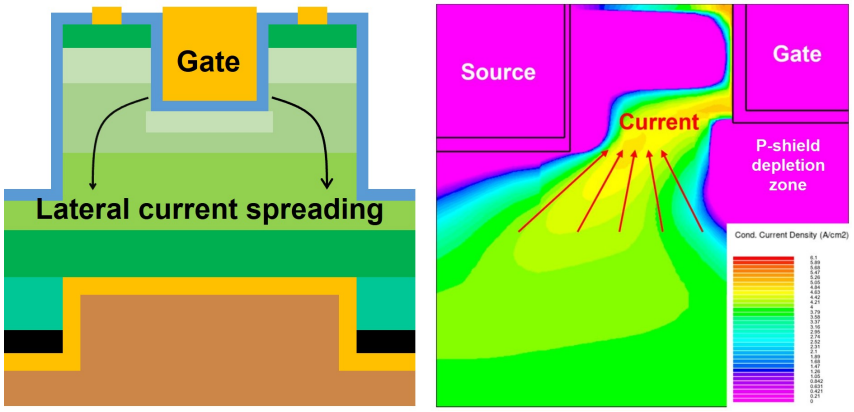


Figure 4.9: Schematic of a V-T-MOSFET with p-shield and CSL (left) and a SILVACO simulation showing lateral current spreading in the CSL (right), adapted from [219].

By relieving current constriction, the CSL reduces local self-heating and field hot spots at the trench bottom and p-body junction edges. This improves short-circuit robustness, mitigates trap charging near the sidewalls (benefiting dynamic R_{on}), and lowers the risk of premature punch-through under the gate. The CSL also works synergistically with a source-tied p-shield: the shield pulls field away from the oxide, while the CSL spreads current and flattens the potential near the trench floor.

Key parameters are the CSL thickness and donor concentration. Higher N_{CSL} and/or thicker t_{CSL} reduce $R_{\mathrm{on,sp}}$ by improving lateral spreading, but (i) make full depletion harder in the OFF-state (risking lower BV or earlier punch-through), and (ii) add charge near the channel, increasing C_{oss} and sometimes C_{gd}, which can raise switching losses. Practical designs target an n-type CSL with N_{CSL} on the order of 10^{16}–$10^{17}\,\mathrm{cm}^{-3}$ and tens to a few hundred of nanometers thickness, co-optimized with p-body depth/spacing, trench corner radius, and gate-oxide thickness so that the CSL depletes at BV yet provides low on-state sheet resistance.

The CSL is usually realized as an epitaxial layer between the channel/p-body region and the lower-doped vertical drift. Tight control of its thickness/doping uniformity is important for cell-to-cell consis-

tency. In GaN, polarization effects at heterointerfaces (e.g., if an AlGaN transition is used) can further assist or hinder depletion; maintaining a homogeneous n-GaN CSL avoids unintended 2DEG formation and keeps electrostatics predictable.

The adoption of such field-management layers will be crucial for the next generation of VertiGo devices, where target voltages exceed 1 kV and oxide fields must remain below $3\,\mathrm{MV\,cm^{-1}}$. Their proper design directly addresses the field crowding observed in Chapter 3 and paves the way for higher reliability and scalability.

4.2.3 p-GaN guard rings: concept, operation, and design

At the periphery of a vertical GaN device, the reverse-biased main p–n junction meets the surface with finite curvature. This geometric edge concentrates electric field and typically limits breakdown voltage (BV) below the parallel-plane value. A p-GaN guard ring (or a set of rings) places one or more auxiliary p-type regions concentric with the active junction near the die edge (Fig. 4.10). Under reverse bias, each ring forms its own reverse-biased p–n junction to the drift layer. The depletion region from each ring extends laterally into the drift and shares the potential drop with the main junction. As bias increases, neighboring depletion regions approach partial punch-through, producing a graded lateral potential and reducing the peak surface field at any single edge. The result is a higher BV and reduced sensitivity to local surface imperfections.

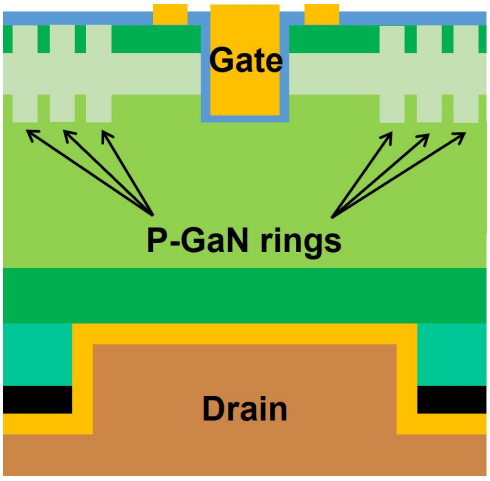


Figure 4.10: Schematic of a V-T-MOSFET with three p-GaN guard rings.

In a one-sided junction (lightly doped drift), the depletion width scales as $W \propto \sqrt{(V_{\mathrm{bi}} + V_R)/N_D}$. A guard ring positioned a distance s from the main junction begins to deplete the drift as V_R rises. Properly chosen spacing s and ring dose/depth ensure that, at the target BV, the depletion regions of adjacent junctions nearly meet (controlled punch-through). This creates a stepped potential distribution

from the active region to the scribe edge and lowers the maximum electric field $E_{\max}$ at the main edge. With multiple rings, the potential steps are finer and the field more uniform. Floating rings self-bias by capacitive coupling/leakage to intermediate potentials; source-tied rings clamp closer to 0 V and still help by enlarging depletion, but provide less potential grading per ring.

Because deep, well-activated p-implants in GaN are challenging, p-rings are commonly realized by patterned p-GaN regrowth (selective epitaxy) around the active area. Alternatives include shallow Mg implantation with high-temperature activation or hybrid approaches (e.g., deposited p-type oxides as auxiliary rings in specific structures). The rings are typically placed under high-quality passivation to suppress surface leakage and stabilize charges that influence ring self-bias.

Key design parameters include:

- **Ring doping:** typically, $N_A = 1 \times 10^{17}\,\mathrm{cm}^{-3}$ to $5 \times 10^{17}\,\mathrm{cm}^{-3}$.
- **Spacing:** 2 - 5 µm between adjacent rings.
- **Number of rings:** 2 - 4 for 600 V devices, increasing to 6 - 8 for $>$ 1 kV operation.

Simulations show that two rings can already lower the peak field by 30 %, while five rings approach the theoretical parallel-plane breakdown. The implanted fluorine termination (FIT) demonstrated in Chapter 3 can be interpreted as a simplified single-ring structure providing local charge compensation near the mesa edge. Guard-ring integration can be achieved by selective p-type implantation or by MBE regrowth through patterned SiO_2 masks.

Guard rings complement, but do not replace surface-field control from passivation and metal field plates. Fixed charge in the dielectric (e.g., negative charge in ALD Al_2O_3) shifts the effective potentials of floating rings. A source-tied field plate over thick dielectric further spreads surface equipotentials and can reduce the number of rings needed for a given BV target.

These rings must contact the drift layer; their trenches can therefore be etched with the gate-trench module (using a separate termination mask). Guard rings are already proven in vertical GaN PiN diodes [169, 220, 221] and Schottky diodes [222] and can be adapted to V-T-MOSFETs.

4.2.4 Superjunction MOSFET (SJ–MOSFET)

An alternative approach to field distribution is the superjunction (SJ) MOSFET concept, which replaces the uniformly doped n^- drift region with a periodic lattice of alternating n and p pillars that extend vertically through (most of) the drift thickness [223]. Under reverse bias, the depletion regions from adjacent p and n pillars expand laterally and mutually neutralize the space charge. When charge balance is satisfied, the electric field is redistributed nearly uniformly across the vertical thickness, allowing a

much higher breakdown voltage (BV) at a given drift thickness or a much higher drift doping at a given BV. In on-state, the current conducts primarily in the n pillars with a much higher donor concentration than a conventional n^- drift, dramatically reducing $R_{\mathrm{on,sp}}$.

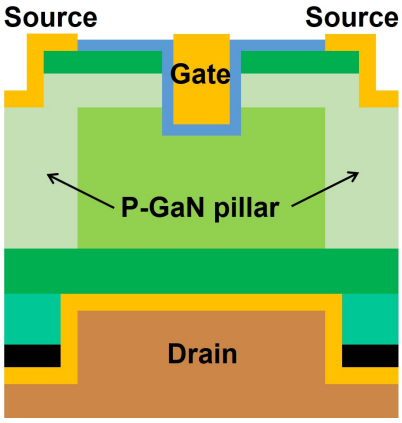


Figure 4.11: Schematic of a SJ-MOSFET.

In the blocking state, adjacent p/n pillars are reverse biased laterally. For a one-period unit cell of width $W = W_n + W_p$ (with W_n and W_p the pillar widths), the charge-balance condition is

$$Q_n \approx Q_p \quad \Leftrightarrow \quad N_D W_n \approx N_A W_p, \tag{4.2}$$

ignoring second-order effects from curvature and interface charge. When Eq. (4.2) holds, the lateral electric field between pillars becomes nearly linear, and the vertical field distribution approaches the parallel-plate limit set by the critical field E_{crit} of the semiconductor. As a result, the specific on–resistance–to–BV trade-off improves from conventional drift scaling to SJ scaling. Deviations from balance ($Q_n \neq Q_p$) cause residual space charge that reintroduces field peaking and lowers BV. In practice, the acceptable imbalance is only a few to $\sim$10% depending on geometry and surface charge.

With $V_G > V_{\mathrm{TH}}$, the inversion channel injects electrons into the n pillars. Because N_D in the n pillars can be an order of magnitude (or more) higher than in a conventional n^- drift of the same BV, the conduction cross-section has a much lower resistivity. For properly designed SJ cells, $R_{\mathrm{on,sp}}$ drops significantly compared with a uniform drift at identical BV.

Key geometric/electrostatic parameters are pillar widths W_n, W_p and pitch, pillar dopings N_D, N_A, pillar height (fill fraction of the drift), and corner curvature and passivation at the surface. Design proceeds by enforcing Eq. (4.2) (with margins for process variation), choosing pillar height to span the high-field region, and rounding corners to avoid local field crowding. Gate and termination features (p-shield, field plates, guard rings) remain relevant and are co-optimized with the SJ lattice.

Fabrication challenges

Implementing the SJ structure in GaN remains extremely challenging.

In silicon, SJ pillars are realized by multi-epitaxy or deep trench fill. In GaN, practical routes include:

- **Deep trench etch and selective regrowth:** etch vertical trenches into the drift and regrow p-GaN to form p pillars; the remaining GaN acts as n pillars (possibly followed by n-type compensation/doping).
- **Stacked epitaxy with pattern transfer:** sequential growth and etch-back to build alternating p/n regions.

GaN poses additional challenges: forming low-defect, high-activation p-GaN pillars (Mg activation, H removal, compensation), maintaining smooth, low-leakage pillar sidewalls (etch-damage control and post-etch repair), tight control of charge balance ($|Q_n - Q_p|/Q \lesssim$ a few percent), and thermal-budget compatibility with the trench gate dielectric. These factors make SJ in GaN a higher-risk, higher-complexity option than edge-only terminations like guard rings.

Benefits include orders-of-magnitude reduction in $R_{\mathrm{on,sp}}$ at a given BV compared with a uniform drift, a flatter electric field (higher BV margin for a given thickness), and potential die-size reduction at a target on-resistance. Trade-offs are: increased process complexity (multiple masks/epitaxy/regrowth), stringent charge-balance tolerance, possible increases in output/Miller capacitances ($C_{\mathrm{oss}}, C_{\mathrm{gd}}$) from the fine pillar geometry, and additional reliability validation (traps at p/n interfaces, dynamic R_{on} under switching).

Although early TCAD studies predict excellent figures of merit, experimental demonstrations have so far been limited to sub-600 V devices. For VertiGo devices, simpler approaches such as FIT edge termination combined with p-shield/CSL structures provide a more immediate path toward kilovolt-class performance. Nevertheless, the SJ framework defines the ultimate limit for vertical GaN power devices once epitaxial precision and dopant activation reach SiC-class maturity.

4.3 Suitable p-type material for process beyond GaN

Most of the previously discussed techniques rely on a p-GaN layer, and their design space is constrained by the low–to–moderate activated hole densities achievable with Mg-doped GaN. This section proposes approaches that enable higher effective p-type doping and thereby increase process and design flexibility.

Achieving efficient p-type doping in GaN remains a fundamental limitation for high-performance vertical MOSFETs. The high ionization energy of Mg acceptors ($\sim$ 0.15 eV above the valence band) restricts the activated hole concentration to $< 10^{18}\,\mathrm{cm}^{-3}$, even after high-temperature annealing. To overcome this intrinsic barrier, alternative materials with shallower acceptor levels and better valence-band alignment have been investigated as p-type auxiliary materials integrated with GaN.

4.3.1 p-type InGaN

Incorporation of indium in GaN reduces the acceptor ionization energy from $\sim$ 150 meV (GaN:Mg) to $\sim$ 40–60 meV for $In_{0.25}Ga_{0.75}N$:Mg (Fig. 4.12 - [224]), resulting in significantly higher activated hole densities [224]. For Mg concentrations around $5 \times 10^{19}\,\mathrm{cm}^{-3}$, typical hole densities of $2 \times 10^{18}\,\mathrm{cm}^{-3}$ to $7 \times 10^{18}\,\mathrm{cm}^{-3}$ are reported, representing a tenfold improvement over pure GaN. The enhanced activation is attributed to the upward shift of the valence band and local strain-induced modifications of the Mg–N bond length. In addition, the larger static dielectric constant of InGaN weakens the Coulomb binding of holes to Mg, further lowering the ionization energy in line with the hydrogenic impurity model [225].

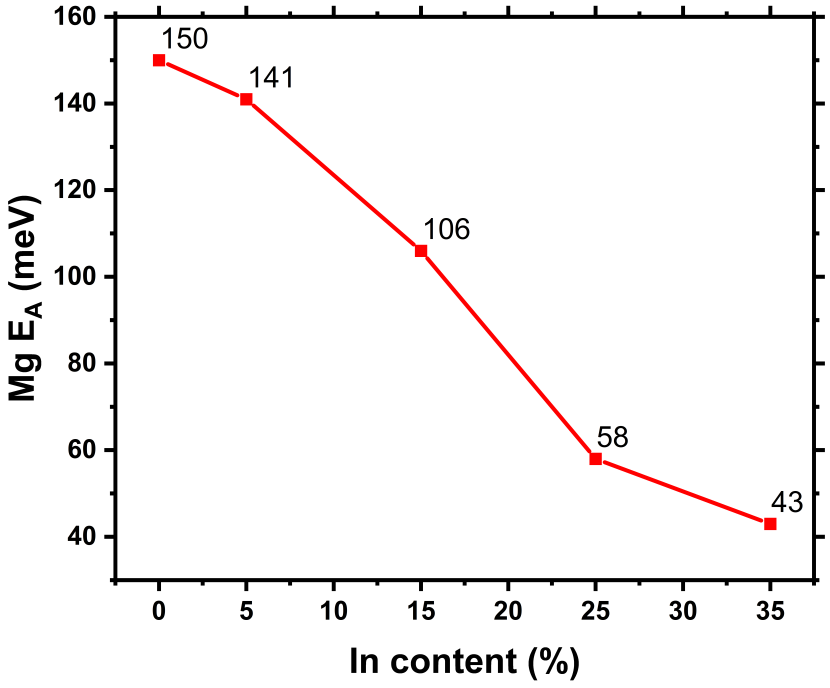


Figure 4.12: Mg activation energy as a function of In content in InGaN

Mg incorporation and post-growth activation also tend to be more effective in InGaN than in GaN. In particular, the binding energy of Mg–H complexes that form under hydrogen-containing growth conditions is reduced in In-containing layers, facilitating activation by thermal annealing. Taken together, these effects enable significantly higher effective hole concentrations in InGaN than in GaN at comparable Mg

doses, with reported room-temperature values up to $7.8 \times 10^{18}\,\mathrm{cm}^{-3}$ for 20% In [226].

These benefits come with trade-offs. Increasing In content reduces the material's critical electric field for avalanche/band-to-band breakdown due to the shrinking bandgap. For 20 - 25% In, bulk-like estimates place E_{crit} on the order of ~ 2.1–$2.4\,\mathrm{MV\,cm}^{-1}$ at $300\,\mathrm{K}$ (device-level values are often lower due to field crowding and defects). Consequently, while p-InGaN is attractive for achieving high activated acceptor densities (e.g., as a p-type cap or contact-assist layer), its use as a p-body in high-voltage structures can compromise breakdown voltage unless the peak electric field is engineered to reside in the GaN drift region rather than in the In-rich body.

Overall, InGaN offers a practical route toward improved hole conductivity without fundamentally altering the GaN epitaxial process. MBE growth of p-InGaN at 650–750 ℃ provides the best compromise between indium incorporation and Mg activation, making it a good candidate for the next VertiGo process iteration.

4.3.2 p-type NiO

Another candidate material for GaN passivation is nickel oxide. Nickel oxide (NiO) is an intrinsically p-type wide-bandgap oxide, whose conductivity originates from nickel vacancies (V_{Ni}) that act as acceptor defects. Under oxygen-rich growth conditions, a significant fraction of Ni atoms are oxidized to the 3+ state, generating holes in hybridized Ni 3d–O 2p orbitals. As a result, NiO can exhibit high hole concentrations, typically in the $1 \times 10^{18}\,\mathrm{cm}^{-3}$ to $1 \times 10^{20}\,\mathrm{cm}^{-3}$ range, even without extrinsic dopants, and can be further enhanced through Li doping (see Fig. 4.13).

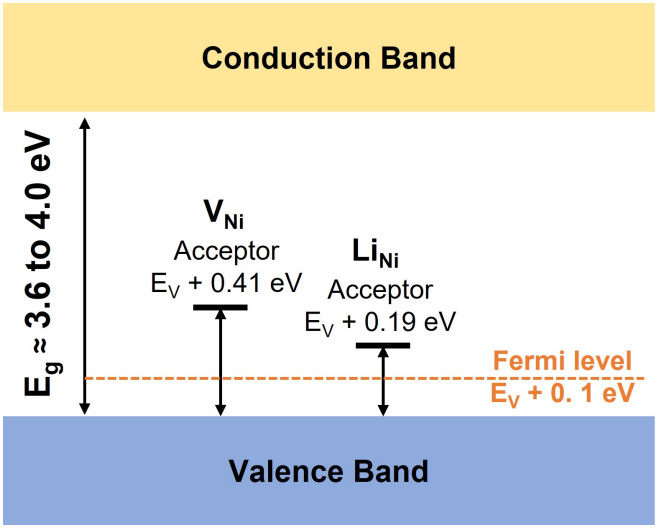


Figure 4.13: Mg activation energy as a function of In content in InGaN

When deposited on GaN, p-type NiO forms a hole-rich, high–work-function interface that effectively

suppresses electron accumulation and surface leakage, while providing good chemical stability and field screening. These properties make NiO an attractive passivation or field-modulation layer for GaN-based power devices, improving breakdown uniformity and dynamic performance without requiring optical transparency.

Deposition techniques such as reactive sputtering or pulsed-laser deposition enable conformal coverage and low defect density at temperatures compatible with the overall process (< 400 °C). However, thermal stability and interface-state control remain critical challenges; NiO tends to reduce to Ni under vacuum annealing or strong bias stress, potentially creating leakage paths. Further optimization of stoichiometry and post-deposition annealing is required to ensure reproducible, stable p-type behavior.

Conclusion

This chapter reviewed the **technological strategies** required to extend GaN-on-Si vertical MOSFETs toward kilovolt-class operation. Starting from the baseline process established in Chapter 3, it identified the key physical and material challenges: etch damage, dielectric quality, field crowding, and limited p-type conductivity; and surveyed the most promising solutions.

The proposed improvements can be summarized as follows:

- **Gate and surface engineering:** optimized Cl_2/BCl_3 ICP etching with controlled self-bias (~ 270 V) combined with oxidation–BOE or plasma-repair cycles to recover stoichiometric surfaces.
- **Dielectric optimization:** adoption of pure ALD Al_2O_3 or Al_2O_3/SiN_x bilayers with forming-gas annealing to minimize interface charge ($Q_f < 1 \times 10^{12}\,\mathrm{cm}^{-2}$).
- **Field-management layers:** integration of p-shield and CSL structures to reduce oxide fields below $3\,\mathrm{MV\,cm}^{-1}$ and enhance dynamic stability.
- **Edge termination:** use of fluorine implantation or multi-ring p-guard termination to achieve uniform potential distribution.
- **Advanced architectures:** exploration of superjunction principles for ultimate scaling, though presently limited by dopant activation control.
- **p-type materials:** evaluation of p-InGaN and NiO for improved hole conductivity and band alignment.

For near-term VertiGo developments, the most impactful combination will likely include:

- ALD Al_2O_3 gate dielectric

- fluorine-implanted termination (FIT)
- moderate-doping p-shield ($10^{17}\,\mathrm{cm}^{-3}$), and
- improved Cu backside contact uniformity.

These refinements are expected to raise breakdown voltages toward 1 kV while maintaining $R_{\mathrm{on,sp}} < 10\,\mathrm{m\Omega\,cm}^2$. In the longer term, incorporating p-InGaN or NiO layers could further enhance gate stability and enable normally-off vertical GaN devices.

General Conclusion

Chapter 1 established the context for high-efficiency power conversion by reviewing Si, SiC, and GaN technologies through standard figures of merit and by relating material properties (bandgap, critical field, mobility, thermal conductivity) to breakdown capability and $R_{on,sp}$. Beyond intrinsic limits, it identified design-level constraints that dominate in practice: electric-field crowding, charge trapping that inflates dynamic $R_{on,sp}^{dyn}$. Together, these considerations motivated vertical GaN architectures as a credible route to higher BV and lower conduction loss—conditional on low-damage etching, low-trap gate stacks, and robust terminations.

This thesis explored two complementary routes to push GaN power devices toward higher blocking voltage, lower loss, and improved reliability. First, lateral GaN HEMTs were studied with the objective of approaching the 1.2 kV class. TCAD guided buffer and back-barrier choices and highlighted the trade-offs between breakdown, leakage, and trapping. Fabricated HEMTs on sapphire confirmed the expected BV–spacing scaling and maintained low $R_{on,sp}$, benchmarking competitively against the literature and underscoring the importance of buffer charge management for dynamic behavior.

Second, a baseline GaN-on-Si vertical trench MOSFET flow was established. Quasi-vertical devices enabled process exploration, while the first fully vertical structures revealed the primary bottlenecks: conformal backside metallization and drain contact continuity. These limitations capped the apparent current density and inflated the extracted specific on-resistance, indicating that performance is presently limited by technology integration rather than by the vertical architecture itself. Once seed coverage, sidewall continuity, and dielectric interfaces are improved, the path to kilovolt-class blocking with sub-$10\,\mathrm{m\Omega\,cm^2}$ $R_{on,sp}$ appears realistic on GaN-on-Si.

Building on these findings, Chapter 4 mapped a pragmatic improvement plan. On the process side: low-damage, anisotropic ICP-RIE followed by gentle post-etch repair to control sidewall quality and trench rounding; and conformal gate stacks (ultrathin nitride interfacial layer plus ALD oxide) to reduce interface/border traps and bias-temperature drift. On the device side: p-shielding to lower oxide field and Miller coupling, a current-spreading layer (CSL) to relieve JFET/access resistance and hot spots,

robust edge terminations (p-GaN guard rings or FIT), and, longer-term, superjunction concepts when pillar charge balance and sidewall quality are under control. Together, these features target higher BV at a given geometry while containing the dynamic loss and variability that ultimately limit converter-level gains.

In summary, the lateral HEMT route delivered encouraging results and a clear buffer/field-management playbook; the vertical route established manufacturability and identified precisely what must be fixed for state-of-the-art performance. Near-term priorities are: (i) conformal backside/sidewall metallization, (ii) low-damage gate-trench etch with post-etch repair and controlled corner rounding, and (iii) co-optimization of p-shield/CSL/termination with a low-trap gate stack. Executing these steps should raise breakdown margin toward $\sim$ 1 kV while driving $R_{\mathrm{on,sp}} < 10\,\mathrm{m\Omega\,cm^2}$) on GaN-on-Si, opening a credible path from first demonstrations to robust, scalable vertical GaN power devices.

Further research is required to mature the manufacturing chain. The performance of GaN-on-sapphire HEMTs is promising for devices targeting the 1.2 kV class, but the bonding methods remain under active development. It is essential to verify that these steps do not degrade key device characteristics (BV, $R_{\mathrm{on,sp}}$, dynamic behavior) or long-term reliability, and to define process windows that are robust to wafer-level variability.

GaN-on-Si vertical devices also remain immature. The fabrication flow is likely to evolve in the near term, and further studies of device operation are needed on actual, fabricated trenched structures. Our process must be optimized to ensure effective p-GaN activation and properly executed contact anneals, while preserving the GaN/dielectric interface. Before that, we must develop an ALD recipe for a SiN interfacial layer and refine our current Al_2O_3 deposition recipe. We need to determine which oxidant (O_2/O_3 versus H_2O) yields lower D_{it} and higher current output, and whether a soft deposition step, at least for the first few nanometers, is required to avoid damaging the interfacial layer.

Additionally, we need to improve our ICP-etching recipe to enhance the gate shape and prevent gate-induced breakdown. A Cl_2/BCl_3 gas mix appears to be the best option; to ensure better etch rate and anisotropy, a small (to limit additional damage) proportion of Ar may be added. Post-etch, a gentle oxygen-plasma oxidation followed by BOE appears to be an effective approach to remove the damaged surface layer; however, its impact on trench geometry must be monitored.

In parallel, edge-termination techniques will be implemented. Fluorine implantation requires testing different doses and energies to ensure optimal ion distribution in GaN, as well as careful annealing to avoid further diffusion. MBE regrowth of p-GaN requires cleaning of the mesa sidewalls before deposition. Both ex-situ and in-situ solutions can be tested.

In the longer term, p-shield regrowth can be attempted by adding an additional etching step after the

gate etch. To ensure a shield wider than the gate trench, a protective mask covering the gate sidewalls and the sample surface will be needed, followed by an isotropic etch to widen the bottom of the trench. In an even longer timeframe, superjunction structure fabrication could be attempted once MBE regrowth of p-GaN is fully mastered.

Much of the available data concerns GaN-on-GaN epitaxy, simple MOS capacitors, or diodes. More fabrication of fully vertical trench MOSFETs is needed to provide valuable insight into their operation. In the long term, integrating p-type material is likely necessary to bring the architecture closer to industrial device practice and to improve overall maturity and efficiency. Moreover, this research is supported by advances in the development of thicker-drift, lower–dislocation-density, 6-inch GaN-on-Si epitaxial stacks [227, 228], which promise to further enhance the performance of vertical GaN devices. Ultimately, this work contributes to establishing a clear technological roadmap for scalable, high-voltage GaN power devices, bridging the gap between proof-of-concept demonstrations and manufacturable, reliable systems.

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Publications

1. **A. Bidaud**, L. Ben Hammou, A. Sefssafi, E. Okada, K. Ziouche, A. Paranjpe, and F. Medjdoub, “Buffer engineering to boost the blocking voltage of GaN high electron mobility transistors on sapphire,” presented at the 15th Int. Conf. on Nitride Semiconductors (ICNS-15), Malmö, Sweden, Jul. 2025.

2. N. Ignoumba-Ignoumba, C. Sonneville, **A. Bidaud**, P. Brosselard, E. Frayssinet, et al., “Physical and electrical characterizations of low n-doped MOCVD GaN-on-sapphire layers for power electronics applications,” Power Electronic Devices and Components, vol. 11, Art. no. 100100, 2025, doi: 10.1016/j.pedc.2025.100100.

3. N. Ignoumba-Ignoumba, C. Sonneville, **A. Bidaud**, M. El Amrani, T. Guillemin, et al., “Stress and doping analysis of low n-doped GaN layers grown on GaN, silicon and sapphire substrates by micro-Raman,” poster presented at ICNS-15, Malmö, Sweden, Jul. 2025. HAL Id: hal-05097968.

4. **A. Bidaud**, Y. Hamdaoui, K. Ziouche, and F. Medjdoub, “[Best poster award] Optimization of fully vertical GaN-on-silicon MOSFET for high-power energy conversion,” poster presented at C’NANO 2025, Paris, France, Mar. 2025. HAL Id: hal-05224675.

5. Y. Hamdaoui, S. Michler, **A. Bidaud**, K. Ziouche, and F. Medjdoub, “1200-V fully vertical GaN-on-silicon p-i-n diodes with avalanche capability and high on-state current above 10 A,” IEEE Transactions on Electron Devices, 2024, , vol. 11, pp.383-386, doi: 10.1109/TED.2024.3496440.

6. N. Ignoumba-Ignoumba, C. Sonneville, É. Frayssinet, **A. Bidaud**, F. Bartoli, et al., “Carrier density analysis in stressed n-doped GaN layers on sapphire,” presented at the GaN Marathon, Verona, Italy, Jun. 2024. HAL Id: hal-04639487

7. **A. Bidaud**, L. Ben Hammou, A. Sefssafi, E. Okada, K. Ziouche, A. Paranjpe, and F. Medjdoub, ”Back barrier integration for $>$4kV blocking in GaN HEMTs on sapphire without field plates”, Symposium de Génie Électrique, Toulouse, France, Jul 2025 . HAL Id: hal-05346045

8. **A. Bidaud**, A. Sefssafi, L. Ben Hammou, E. Okada, K. Ziouche, A. Paranjpe, and F. Medjdoub, “Record R_{ON} - BV Trade-Off and Scalable Heterogeneous Integration in Field-Plate-Free GaN-on-Sapphire HEMTs”, CS Mantech, Portland, USA, Oct 2025

To be submitted

1. **A. Bidaud**, L. Ben Hammou, A. Sefssafi, E. Okada, K. Ziouche, A. Paranjpe, and F. Medjdoub, ”Thermal and electrical optimization of GaN-on-sapphire HEMTs for 1.2 kV power applications through Bonding Layer and Buffer Engineering”, to be submitted to Applied Physics Letter (extended paper from ICNS conference), deadline Jan 2026