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Thermal optimization of RF commutators based on phase change material for 5G communications and beyond

Optimisation thermique des commutateurs RF basés sur les matériaux à changement de phase pour les communications 5G et au-delà

Soutenue le 15 décembre 2025 devant le Jury composé de :

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Dimensions:

L_{PCM}	PCM length
L_{RFgap}	RF_{gap} length
t_D or t_{Diel1}	Dielectric thickness
t_H	Heater thickness
t_{PCM}	PCM thickness
W_{PCM}	PCM width
W_h	Heater width
W_{space}	Width of the space separating branches of multi-branches heaters

Materials:

Al	Aluminium
AlCu	Aluminium-Copper alloy
AlN	Aluminium Nitride
Ge	Germanium
GeTe	Germanium Telluride
GST	Germanium–Antimony–Tellurium
Mo	Molybdenum
NiCr	Nickel-Chromium alloy
NiCrSi	Nickel-Chromium-Silicon alloy
Sb	Antimony
SbTe	Antimony Telluride
Si	Silicon
Si_3N_4	Silicon Nitride
SiO_2	Silicon Dioxide
Te	Tellure
TiN	Titanium Nitride
VO_2	Vanadium Dioxide
W	Tungsten

Measurement setups:

DUT	Device Under Test
GND	Ground
GSG	Ground-Signal-Ground
PCB	Printed Circuit Board
SOLT	Short-Load-Open-Thru
TRL	Thru-Reflect-Line
VNA	Virtual Network Analyzer
VSU	Voltage Source Unit

Microfabrication techniques:

CMP	Chemical Mechanical Planarization
CVD	Chemical Vapor Deposition

PECVD	Plasma-Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
RIE	Reactive Ion Etching

Performances:

C_{OFF}	OFF-state Capacitance
FOM	Figure-Of-Merit *(in this work, refers to the R_{ON} x C_{OFF} product)*
PH_{OFF}	OFF-state Power-Handling
PH_{ON}	ON-state Power-Handling
R_{ON}	ON-state Resistance
R_{OFF}	OFF-state Resistance

Technologies:

BEOL	Back-End-Of-Line
CMOS	Complementary Metal-Oxide-Semiconductor
FD-SOI	Fully Depleted Silicon-On-Insulator
MEMS	Micro Electromechanical System
PCM	Phase-Change Material
PD-SOI	Partially Depleted Silicon-On-Insulator
SOI	Silicon-On-Insulator

Telecommunications:

AMPS	Advanced Mobile Phone Systems
FR	Frequency Range
GSM	Global System for Mobile Communication
IoT	Internet of Things
RF	Radiofrequency
SMS	Short Message Service
ULTS	Universal Mobile Telecommunication System
URLLC	Ultra-Reliable Low-Latency Communications

Other:

DC	Direct Current
FEM	Finite Element Modeling
FIB-SEM	Focused Ion Beam - Scanning Electron Microscope
IR	Infrared
TEM	Transmission Electron Microscope

List of Symbols

Electrical Parameters:

$\boldsymbol{\rho_{rT}}$	Electrical resistivity at Room temperature *[Ω.cm]*
$\boldsymbol{\omega}$	Angular frequency *[rad.s^{-1}]*
$\boldsymbol{C}$	Capacitance [F]
$\boldsymbol{f}$	Signal frequency *[Hz]*
$\boldsymbol{I_{h(t)}}$	Current through the heater as a function of time (t) *[A]*
$\boldsymbol{P_{h(t)}}$	Heater power as a function of time (t) *[W]*
Pin	Input power *[dBm]*
Pout	Output power *[dBm]*
$\boldsymbol{R_g}$	Internal resistance of the generator *[Ω]*
$\boldsymbol{R_{h(t)}}$	Heater resistance as a function of time (t) *[Ω]*
$\boldsymbol{R_{rT}}$	Initial heater resistance at room temperature *[Ω]*
$\boldsymbol{U_c}$	Command voltage applied by the user to the generator *[V]*
$\boldsymbol{U_{h(t)}}$	Voltage at the heater terminals as a function of time (t) *[V]*
$\boldsymbol{Z_0}$	Line Reference Impedance *[Ω]*
$\boldsymbol{Z_C}$	Capacitive impedance *[Ω]*

Thermal Parameters:

$\boldsymbol{\alpha}$	Thermal diffusivity *[m^2.s^{-1}]*
$\boldsymbol{C_p}$	Specific heat Capacity *[J.kg^{-1}.K^{-1}]*
$\boldsymbol{k}$ **or** λ	Thermal conductivity *[W.m^{-1}.K^{-1}]*
$\boldsymbol{L_m}$	Latent heat of fusion *[J.m^{-3}]*
$\boldsymbol{Q}$	Heat Flux *[W.m^{-2}]*
$\boldsymbol{T}$	Temperature *[K]*
TBR	Thermal Boudary Resistance *[m^2.K.GW^{-1}]*
$\boldsymbol{TCR}$	Thermal Coefficient of Resistance *(dimensionless)*
Ta	Annealing temperature [K]
$\mathbf{T_{cryst}}$	Crystallization temperature *[K]*
$\boldsymbol{T_f}$	Final temperature *[K]*
Tf	Fictive temperature *[K]*
$\mathbf{T_{max}}$	Maximum temperature *[K]*
$\mathbf{T_{melt}}$	Melting temperature *[K]*
$\mathbf{T_{min}}$	Minimum temperature *[K]*
$\boldsymbol{T_r}$	Room temperature *[K]*
$\boldsymbol{\tau}$	Time constant representing the rate of temperature increase *[s]*

Phase-Field:

$\boldsymbol{\sigma}$	Electrical conudctivity *[S.m-1]*
$\boldsymbol{\sigma_a}$	Interfacial energy between two adjacent phases *[J]*
$\boldsymbol{d}$	Interatomic spacing *[Å]*
$\boldsymbol{f(\eta)}$	Local free energy potential *[J]*
$\boldsymbol{F(\eta)}$	Free energy functional *[J]*
$\boldsymbol{\Delta G}$	Free energy variation due to the phase transition of a small material portion *[J]*
$\boldsymbol{\Delta G^*}$	Energy barrier that must be overcome to form a stable nucleus *[J]*

$h'(\eta)$	Phase fraction change rate *[s-1]*
k_b	Boltzmann constant = 1.38e^{-23} *[J.K^{-1}]*
k_{th}	Thermal conductivity *[W.m^{-1}K^{-1}]*
L_η	Positive kinetic coefficient *[m^{4}J^{-1}s^{-1}]*
η	Order parameter *(dimensionless)*
N	Expected number of critical nuclei generated during a time step *(dimensionless)*
N_s	Number of potential nucleation sites per unit volume *(dimensionless)*
R_c	Critical nucleus radius *[Å]*
μ	Frequency of atoms attachement *[s^{-1}]*
V	Electric potential *[V]*
V_i	Crystal growth velocity *[m.s^{-1}]*
Z	Zeldovich factor *(dimensionless)*

Units:

Ω	Ohm
Å	Angstroms *(3e^{-10} m)*
dB	Decibel
dBm	Decibel-Milliwatt
fF	FemtoFarad *(10^{-15} Farad)*
fs	FemtoSecond *(10^{-15} second)*
Gbps	GigaBit Per Second *(10^9 bits/second)*
GHz	GigaHertz *(10^9 Hertz)*
GW	GigaWatt *(10^9 Watts)*
J	Joule
K	Kelvin *(Celsius temperature + 273.15)*
Kbps	KiloBit Per Second *(10^3 bits/second)*
MΩ	MegaOhm *(10^6 Ohms)*
Mbit	MegaBit *(10^6 Bits)*
Mbps	MegaBit Per Second *(10^6 bits/second)*
MHz	MegaHertz *(10^6 Hertz)*
nJ	NanoJoule *(10^{-9} Joule)*
nm	NanoMeter *(10^{-9} meter)*
ns	NanoSecond *(10^{-9} second)*
THz	TeraHertz *(10^{12} Hertz)*
μm	microMeter *(10^{-6} meter)*
μs	microSecond *(10^{-6} second)*
V	Volt
W	Watt

Other Parameters:

E	Energy *[J]*
L	Kapitza length *[m]*
ρ	Density of material *[kg.m^{-3}]*

Abstract

The exponential growth in global data exchange is placing increasing demands on high-performance communication technologies. Among emerging solutions, radio-frequency (RF) switches based on phase-change materials (PCMs), which modulate electrical conductivity via thermally induced phase transitions, show significant promise, especially for operation in higher-frequency bands that support faster data rates. To compete with established technologies, however, these devices must offer both robust power handling and excellent RF performance.

This thesis presents a comprehensive optimization strategy for PCM-based RF switches, grounded in finite element simulations to evaluate the impact of device geometry, material selection, and thermal actuation methods. New design approaches are proposed to enhance switching efficiency, primarily by increasing the volume of amorphized PCM in the OFF state, leading to reduced parasitic losses and improved thermal stability.

Fabricated and experimentally characterized devices exhibit substantial performance gains. The use of thermally conductive layers, together with tailored thermal management architectures, significantly improves heat dissipation and enables OFF-state power handling improvement of up to 5 dBm in series-configured switches. Furthermore, the implementation of multi-branch heating structures allows the switches to sustain power levels of up to 37 dBm in the OFF state and 35 dBm in the ON state. These enhancements are accompanied by a 20 % reduction in OFF-state parasitic capacitance, with no degradation in ON-state resistance, and a 16 % reduction in overall energy consumption.

In parallel, a Phase-Field modeling framework has been integrated into the simulation environment to track the microstructural evolution of the PCM during switching. This approach enables direct comparison between materials such as GST and GeTe, with GeTe demonstrating superior phase stability in the OFF state, highlighting its suitability for next-generation RF applications.

Keywords: RF Switch / Phase-Change Materials / thermoresistive heater / heat fluxes / GeTe (Germanium Telluride) / GST (Germanium-Antimony-Tellurium) / tungsten / parasitic capacities / power handling / finite elements modeling

Résumé

L'augmentation massive des échanges de données à l'échelle mondiale impose la conception de technologies de communication à haute performance. Les commutateurs radiofréquence (RF) à base de matériaux à changement de phase (PCM), dont la conductivité électrique est modulée par une transition de phase thermique, apparaissent comme une solution prometteuse, notamment dans le cadre d'exploitations de nouvelles bandes de fréquences plus élevées offrant des débits plus rapides. Toutefois, pour être compétitifs, ces dispositifs doivent offrir à la fois une excellente tenue en puissance et des performances RF optimales.

Ce travail de thèse propose une démarche d'optimisation de ces commutateurs, en s'appuyant sur des simulations par éléments finis pour analyser l'influence des paramètres géométriques, des matériaux utilisés et des stratégies de chauffage. De nouveaux designs sont proposés afin d'améliorer l'efficacité

de la commutation, notamment en augmentant la quantité de PCM amorphisé à l'état OFF, ce qui permet de réduire les pertes parasites et d'augmenter la stabilité thermique.

Les dispositifs issus de cette démarche présentent, après fabrication et caractérisation, des avancées notables. L'ajout de couches thermiquement conductrices et l'adoption d'architectures spécifiques ont permis d'optimiser l'évacuation de la chaleur, conduisant à une amélioration de la tenue en puissance à l'état OFF de 5 dBm pour des structures en série. Par ailleurs, l'implémentation de structures chauffantes multibranches a permis d'atteindre des tenues en puissance de 37 dBm à l'état OFF et de 35 dBm à l'état ON. Ces résultats s'accompagnent d'une diminution de 20 % des capacités parasites à l'état OFF, sans compromis sur la résistance à l'état ON, ainsi que d'une réduction de 16 % de la consommation énergétique.

Enfin, une modélisation basée sur la méthode « champ de phase » a été intégrée à l'environnement de simulation pour suivre l'évolution microstructurale du PCM lors de la commutation. Cette approche permet de comparer le comportement de matériaux comme le GST et le GeTe, ce dernier montrant une meilleure stabilité de phase à l'état OFF, et confirmant son intérêt pour les applications RF.

Mots clés : Commutateur RF / matériau à changement de phase (PCM) / chauffage thermorésistif / flux de chaleur / GeTe (Tellurure de Germanium) / GST (Germanium-Antimoine-Tellure) / tungstène / capacités parasites / tenue en puissance / simulations par méthode des éléments finis

General introduction

Transmitting information has always been a vital capability for human societies. From simple smoke signals and sound rhythms to telegraphs and telephones, humanity has continuously sought to overcome the limitations of distance and obstacles, striving to connect as many people as possible across the globe. The emergence of telephones, and subsequently widespread access to the Internet, has caused the volume of data to be transmitted worldwide to increase dramatically over the past decades. Meeting this growing demand requires constantly pushing the boundaries of information transmission capabilities, addressing the challenges of higher data rates, extended coverage, and improved signal quality. One critical component in this ecosystem is the radio-frequency switch (RF switch), which ensures the connection and transmission of signals between antennas and the transmitters and receivers integrated into modern devices.

Various types of RF switches are used to fulfill these requirements, with RF Micro-Electro-Mechanical Systems (RF-MEMS) and Silicon-on-Insulator (RF-SOI) CMOS technologies being among the most established. RF-MEMS devices provide excellent RF performance, with low insertion loss, strong isolation, and high linearity across a wide frequency range. However, their high actuation voltages, relatively slow switching speed, and limited reliability due to mechanical wear constrain their suitability for high-frequency applications such as 5G and beyond. RF-SOI CMOS switches, benefiting from mature fabrication processes, low power consumption, and high switching speed, have become the dominant industrial solution. Nevertheless, their performance deteriorates at millimeter-wave frequencies, limiting their applicability to next-generation communication systems.

As data rates continue to rise and mobile networks expand into higher frequency bands, maintaining good performance has become increasingly challenging. In this context, Phase-Change Materials (PCMs) have attracted growing interest. These materials exhibit a reversible change in resistivity under thermal control; a property first harnessed in non-volatile memory applications. Today, PCM is considered a promising candidate for RF switches, offering high isolation above 30 dB, low insertion loss below 0.5 dB, and the potential for energy-efficient operation due to its bistable nature. PCM-based devices also benefit from compact integration into very-large-scale integrated (VLSI) circuits and improved reliability, as the absence of mechanical components reduces sensitivity to wear and thermal aging, enabling operation in extreme environments such as automotive (on rough terrain), aerospace, or satellite systems.

Despite these advantages, several key performance metrics must be further optimized for PCM switches to reach commercial viability. The switching endurance —the number of ON-OFF cycles before performance degradation— must be increased to compete with established technologies. Parasitic capacitances in electrically actuated PCM switches must be minimized to improve the main Figure-of-Merit ($R_{ON} \times C_{OFF}$). Additionally, energy consumption can be reduced, and power-handling can be further enhanced, particularly in the OFF state and in the case of series-configured switches. The research presented in this manuscript aims to address these challenges, contributing to the advancement of PCM-based RF switches toward high-performance, reliable, and energy-efficient solutions.

The first chapter of this manuscript retraces the evolution of telecommunication systems —from primitive methods of information exchange to the advanced technologies used today. It provides an overview of the operating principles and typical performance metrics of MEMS, RF-SOI, and PCM switches, offering insights into the growing interest in PCM-based RF devices. According to the different actuation methods and materials presented, the resulting limitations are identified and

discussed. Following this, the typical fabrication process of PCM-based RF switches is presented, after which the role and function of each layer and material are detailed. This analysis establishes the link between material and structural characteristics, thermal behavior, and their impact on RF and power-handling performance. Overall, this first chapter provides a solid foundation for understanding the world of PCM RF switches and sets the stage for the performance improvements discussed in the subsequent sections.

The second chapter focuses on the methodology developed and employed throughout this work. It begins with the Finite Element Modeling (FEM) simulations, introducing the different models used during the PhD and their specific objectives. The material properties implemented in the simulations are listed, and the modeling strategies adopted to reproduce the key physical mechanisms governing PCM switch behavior are explained. These simulations serve primarily to analyze the thermal behavior of the devices under various conditions —such as variations in layer thicknesses, material properties, and voltage pulse profiles applied to the thermo-resistive element used for heat generation (called "heater"). The heating phase of the actuation pulse provides information on the energy required to trigger the phase transition, as well as on the temperatures reached within the different components, offering insight into their impact on the switch's reliability. Conversely, the cooling phase reveals the amorphization (changing of the PCM structure into a resistive state to block the signal during OFF-state) efficiency of the PCM. Subsequently, attention turns to experimental work. The measurement setups used for device actuation and characterization —including resistance, ON-state resistance, OFF-state capacitance, and power-handling— are described in detail, along with their operating principles. The protocols followed during measurements are then presented to facilitate comparison between simulation and experimental results. Finally, this chapter discusses the intrinsic limitations of FEM simulations in reproducing certain physical phenomena observed during measurements, highlighting potential sources of discrepancy between modeled and experimental data. With both the simulation and measurement methodologies established, the manuscript can then proceed to a detailed analysis of the electrical and thermal behavior of PCM-based RF switches.

The third chapter begins by addressing how to evaluate the amorphization efficiency in simulations. Since the capabilities of Finite Element Modeling (FEM) do not allow direct reproduction of the phase-change mechanism, an alternative approach is adopted. This method estimates the amorphized region by observing the cooling rate of the previously melted PCM. However, such an approach requires predefining which portion of the PCM is to be melted. To do so, an analysis is conducted to determine the optimal melted region —large enough to ensure reliable actuation if the model is transposed to fabricated devices, yet not too large to avoid melting PCM close to the RF electrodes, which act as excellent thermal conductors and would demand excessive energy to heat. Following this, the chapter presents optimizations related to the thickness of both the PCM and the heater. The heater must remain thin enough to maintain high electrical resistance and generate heat efficiently, yet sufficiently thick to ensure mechanical robustness and long-term reliability. Regarding the PCM, increasing its thickness provides a larger active volume for the crystalline (conductive) and amorphous (resistive) phases, but also slows down the cooling process, which can hinder amorphization efficiency. Furthermore, because the heater cannot be placed in direct contact with the PCM to prevent interference during signal transmission, a dielectric layer is introduced between them. An analysis is therefore performed to select the appropriate dielectric material, comparing high-thermal-conductivity materials —which favor faster cooling of the PCM— and low-thermal-conductivity materials —which promote heat retention during the heating phase. An extended study is then dedicated to the combined influence of two key geometric parameters: the RF_{gap} (i.e., the distance between the electrodes, which defines the amount of PCM available for amorphization) and the heater width. A wide range of dimensions is explored to characterize the thermal behavior of the switch and

to identify optimal trade-offs between efficient heating with minimal energy consumption, sufficient amorphous volume for strong OFF-state isolation, and reduced parasitic capacitance between the heater and the PCM. Finally, the chapter concludes with the optimization of the forming method —a process involving repeated actuation cycles to stabilize the performance of fabricated devices. This optimization improves the accuracy and repeatability of characterizations performed on switches which integrate the design enhancements developed in the following chapter.

The fourth chapter presents the main optimizations developed throughout the PhD. The first section focuses on achieving a more uniform temperature distribution within the heater, thereby preventing localized overheating that could compromise reliability and ensuring a more energy-efficient heat transfer to the PCM. These goals are achieved by adding a thermally conductive layer on top of the switch, which reduces the maximum heater temperature by up to one third for devices with short RF_{gap}. The analysis also reveals that this layer enhances heat dissipation during the PCM cooling phase, improving amorphization efficiency. Cooling is further accelerated by decreasing the distance between the PCM and the substrate, which acts as an efficient thermal sink. However, care is taken to avoid positioning the substrate too close to the PCM, as this would cause an exponential increase in energy consumption during the heating phase. The combined implementation of the thermally conductive layer and the reduced PCM–substrate spacing is validated experimentally, with fabricated devices exhibiting improvement in power-handling capability. An additional solution is explored in simulations, consisting of adding thermally conductive blocks on top of the switch, directly above the hottest PCM regions. The chapter then examines the influence of voltage pulse profile. Various pulse durations are tested to identify a trade-off between short pulses, which require less energy and limit heat diffusion within the switch, and longer pulses, which allow for gradual PCM heating and improved temperature control, reducing the risk of exceeding the melting threshold unnecessarily. Finally, an innovative heater design is introduced. By splitting the main conductive path into multiple branches, the temperature distribution within the PCM becomes more uniform, reducing temperature gradients and excess heating. The study focuses on two-branch (double-branch) heater configurations, with design guidelines established to optimize their thermal performance compared to conventional single-branch heaters. Measurements on fabricated devices confirm these improvements; double-branch heaters reduce energy consumption, accelerate PCM cooling, and increase OFF-state resistance. The enhanced amorphization efficiency also reduces parasitic capacitances, particularly in devices with wider heaters or PCM regions. Moreover, OFF-state power-handling also benefits from the more extensive amorphous volume.

The fifth chapter addresses the absence of phase-change physics in FEM simulations by introducing the Phase-Field Method (PFM). This method is described in detail, explaining how it enables the determination of the state of each point within the PCM based on the temporal evolution of temperature. In particular, the crystallization process is reproduced, including both the formation of crystalline clusters (nuclei) and their subsequent growth over time. Because the method depends on the intrinsic properties of the PCM, the crystallization dynamics naturally adapt to the specific material used. A comparative study between GeTe and GST materials highlights this feature: GST exhibits a nucleation-dominated crystallization behavior, whereas GeTe shows a growth-dominated one, both accurately reproduced during the cooling phase following amorphization pulses. Finally, the current limitations of the model are discussed, notably the significant computational resources required due to the extremely fine mesh refinement, which presently restricts simulations to two dimensions and limits the integration of additional physical phenomena within the switch.

Chapter 1
Evolution of communication technologies and the emergence of RF and PCM-based RF switches

The growing demand for high-performance wireless communications systems has driven significant interest in the development of radiofrequency (RF) switches capable of combining low insertion loss, high isolation, fast switching speed, and reliable power-handling. Among commercialized technologies, RF-MEMS devices, while offering good isolation and low insertion losses, have been limited by reliability issues, integration challenges, and long switching times. RF-SOI thus emerged as the dominant solution, providing a favorable compromise between RF performance and large-scale manufacturability. However, as new generations of cellular networks increasingly exploit higher frequency bands, the intrinsic limitations of RF-SOI open the need for alternatives approaches capable of breaking this barrier.

Among the emerging solutions, phase-change-material (PCM)-based RF switches are considered strong candidates for extending performance into high-frequency and high-power domains. In these devices, the electrical conductivity of a material bridging two electrodes is reversibly modified through thermally induced phase transitions. This bi-stable behavior, relying on transition between amorphous (highly resistive) and crystalline (highly conductive) states, enables sharp modulation of the electrical signal and supports competitive RF figures of merit, while also offering robust power-handling capability.

In this context, the present chapter first recalls the historical development of telecommunications and RF switch technologies. It then reviews the main families of RF switch technologies currently in use, with emphasis placed on their operating principles and comparative performance. The evolution of PCMs is subsequently traced from their original applications in data storage to their most recent use in RF switches. PCM-based switches are then analyzed in greater detail, with attention to the physical mechanisms underlying their phase transitions, the thermal and electrical properties of the materials involved, and the heating strategies required for actuation. Finally, the effects of structural geometry, material choices, and the shaping of voltage pulses used to generate Joule-effect-based thermal actuation are analyzed, thereby establishing the technological framework that motivates the investigations carried out in this work.

1.1 RF commutators

1.1.1 Evolution of telecommunication systems

Sharing information has always been essential for humanity's development. Throughout history, civilizations have devised various means of communication to overcome the challenge of distance. Both visual and audio methods have been employed for thousands of years. For instance, smoke signals were used by ancient populations and Indigenous American Tribes, while the semaphore system —using mechanically driven arms to form shapes— was developed in the 18th and 19th centuries [1]. However, the performance of these techniques depended heavily on external conditions such as line of sight and weather. Audio-based methods also played a significant role. Military drums, for example, conveyed different orders through specific rhythms, but these systems were restricted by their limited range. While short-range visual and audio signals are still in use today —such as traffic

lights or sirens— achieving global information exchange required communication technologies to move beyond human sensory and physical limitations.

The introduction of electricity in the early 19th century was a turning point for telecommunications. One of the first breakthroughs came from Samuel Morse, who invented the electric telegraph system, enabling message transmission at a rate of 10 bit/s [2]. By 1866, the first functional transatlantic cable was completed. A decade later, Alexander Graham Bell invented the telephone, which entered commercial use in the United States just two years later. The late 19th century saw the emergence of radio communications. In 1895, Guglielmo Marconi demonstrated the first wireless telegraph by transmitting a signal over 2 km, despite obstacles [3]. Radio technology advanced rapidly: broadcasting networks appeared around 1926, quickly gaining popularity until television emerged around 1950, taking a share of the shows initially diffused on radio That same year, coaxial cables were introduced, offering data transfer rates up to 100 Mbit/s, though suffering significant signal losses above 10 MHz [2]. Microwave links further pushed the frontier, raising the transmission frequency to 4 GHz and extending the distance between relays without compromising data rate. The limits of telecommunications were finally overcome with the arrival of the fiber optics between 1970 and 1980. The ultimate breakthrough came with the advent of fiber optics between 1970 and 1980. This technology drastically reduced signal transmission losses, which continued to improve over subsequent decades, as illustrated in Figure 1-1 extracted from [4].

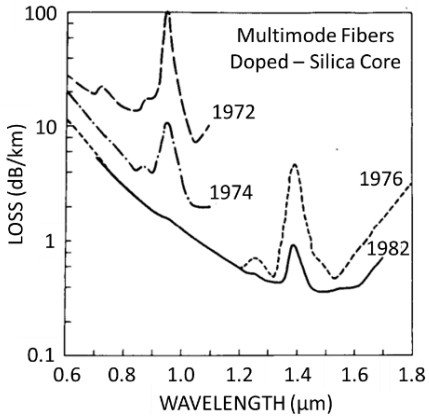


Figure 1-1: *Evolution of signal loss by wavelength between 1972 and 1982 [4].*

By the late 1970s, the emergence of mobile phones marked the beginning of the first generation of cellular networks, or 1G**.** The systems deployed under this generation, known as Advanced Mobile Phone Systems (AMPS), operated between 824 MHz and 894 MHz with a channel capacity of 30 kHz and a transmission rate of 2.4 kbps [5][6]. These networks supported only voice communication, although they were also capable of providing basic vehicle localization services [7]. The second generation (2G) appeared in the 1990s, distinguished primarily by the transition from analog to digital signal transmission. The introduction of the Global System for Mobile Communication (GSM) standard enabled not only voice calls but also text messaging (Short Message Service, SMS) and even image exchange [8]. Data transfer rates improved from an initial 9.6 kbps to about 40 kbps [9]. Frequency allocations expanded beyond those used by 1G, with the addition of the 1800 MHz and 1900 MHz bands [10][11]. The next leap came with the third generation (3G), formally known as the Universal Mobile Telecommunication System (UMTS). Offering data transfer rates between 144 kbps and 384 kbps [6][7], 3G networks enabled a wide range of new applications, including audio and video streaming, internet browsing, electronic wallets [12], health monitoring [12], and educational platforms for course and student management [13]. UMTS was initially deployed in the 2100 MHz band due to the wider channel bandwidth offered by this frequency, increasing the data transmission rate

in comparison with lower bands such as 900 MHz, which remained occupied by 2G services [14]. Over time, however, UMTS progressively extended into lower frequencies to improve coverage and reduce the number of required base stations [14]. Around 2010, the fourth generation (4G) was introduced, representing another major breakthrough. With data rates reaching 100 Mbps, 4G operated in multiple frequency bands, including 850 MHz, 900 MHZ, 1800 MHz and 2300 MHz [15]. Its key was the adoption of an all-IP architecture, which unified voice and data transmission within a single protocol and integrated both wired and wireless technologies [16]. This resulted in significantly improved media quality, faster data speeds, and more efficient network access for end users [5].

The fifth generation of telecommunication (5G) is the central focus of this work. Initially, 5G was conceived to address the exponential growth in global mobile data consumption. Figure 1-2 illustrates past and projected traffic trends [17][18]. As shown in Figure 1-2.(a) the 2018 edition already forecasted exponential growth, while the 2024 edition in Figure 1-2.(b) reveals that actual consumption has surpassed even these predictions. To meet such demands, three key challenges had to be overcome: achieving higher data rates, reducing latency, and extending network accessibility [19][20]. To address these requirements, 5G employs several innovations. First, network slicing enables dynamic allocation of resources to different applications according to their specific needs [21]. Second, at the transmission level, 5G builds upon existing 4G infrastructure, reusing established frequency bands while also exploiting higher ones to expand usable bandwidth and overall capacity. At present, two main frequency ranges are deployed: FR1 (sub-6 GHz) and FR2 (24 - 52 GHz, mmWave). FR1 is predominantly used in rural areas due to its wider coverage, albeit at lower data rates, whereas FR2 is favored in urban settings, where its reduced coverage is offset by significantly higher capacity and throughput [22]-[24]. The targeted performance metrics for 5G included a theoretical peak data rate of 20 Gbps (with a per-user rate of 100 Mbps), latency below 1 ms, and bandwidth usage of 100 MHz [25][26]. These improvements enable high-bandwidth applications such as virtual reality [27] and high-definition video streaming [28], as well as latency-sensitive services like autonomous driving [29], online gaming [30] and, more generally, Ultra-Reliable Low-Latency Communications (URLLC) [31] and the Internet of Things (IoT) [32].

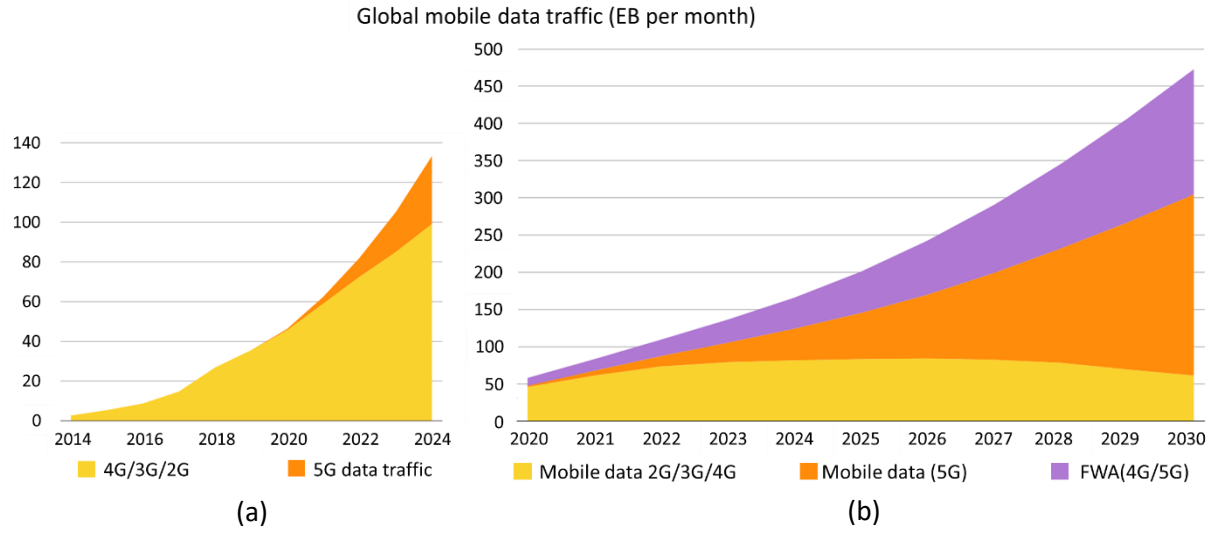


Figure 1-2: *Evolution of global mobile data traffic in exabytes (EB) per month, as reported by Ericsson: (a) November 2018 edition [17] and (b) November 2024 edition [18].*

In practice, 5G has demonstrated excellent data throughput, with 1 Gbps in real-world deployments and up to 10 Gbps under laboratory conditions [33]. Latency performance, while only approaching the 1 ms target in laboratory tests, still offers substantial improvements compared to 4G in operational

environments [34]. However, coverage and accessibility remain major challenges. In densely populated areas, the higher demand for data and the limited propagation of high-frequency signals necessitates a greater number of base stations. Without such expansion, coverage gaps result in significant signal losses [35]. This issue is compounded by the fact that 5G deployment has largely been implemented on top of existing 4G infrastructure, rather than through fully standalone networks. This strategy offers advantages such as cost-effectiveness, smoother technological transition, and dual connectivity [36]. Nevertheless, the reliance on pre-existing stations, combined with the high cost of constructing standalone 5G networks, limits deployment —especially in rural or peri-urban regions. As a result, populations outside major cities experience restricted access to high-frequency signals, exacerbating the digital divide.

To address the limitations of current deployments, 5G is progressively moving toward a new frequency range, FR3 —also referred to as the upper mid-band— which spans from 7 GHz to 24 GHz. This evolution, often termed "advanced 5G," is designed to provide a compromise between the high capacity of FR2 and the broader coverage of FR1 [37]. Although data rates and latency will be further improved, several challenges remain, including persistent coverage constraints, the high investment required for denser base station networks, and the limited availability of devices capable of supporting mmWave frequencies [38]. Looking ahead, FR3 is expected to play a central role in the deployment of sixth-generation networks (6G) [39]. This new standard will integrate a wide spectrum of frequencies, reusing both upper mid-band and mmWave bands for high-capacity communication while, for the first time, exploiting the terahertz (THz) range. THz bands promise ultra-high-speed links, though their extremely short propagation distances restrict their use to specific contexts such as indoor environments, device-to-device communication, or data center interconnects.

Table 1-1: *Evolution of telecommunications through the generations.*

Gen	Frequency band	Data transfer rate	Main new applications	Limitations
1G	[824 MHz - 894 MHz]	2.4 Kbps	Vocal communication	Quality
2G	[824 MHz - 894 MHz] [1800 MHz - 1900 MHz]	[9.6 Kbps - 40 Kbps]	Digital signals SMS Pictures exchange	Slow data transfer rate
3G	900 MHz 2100 MHz	[144 Kbps - 384 Kbps]	Audio & Video listening, Internet browsing	Still lacking in performances
4G	850 MHz, 900 MHZ, 1800 MHz, 2300 MHz	100 Mbps	All-IP architecture: better audio and video quality for medias and improved internet access	Although 5G delivers better performance than past generations, it still struggles to match the rapid rise in data demand.
5G	Sub 6 GHz, [24 GHz - 52 GHz] Aiming for [7 GHz - 24 GHz] (advanced 5G)	1 Gbps (real conditions) 10 Gbps (laboratory conditions)	Network slicing: IoT, low latency applications (Virtual reality, autonomous vehicles), data consuming applications (high-definition medias)	Cost for larger deployment for resources and coverage
6G	[7 GHz - 24 GHz], THz order	Aiming at 100 Gbps	All real time applications (remote healthcare, holographic communications…)	Cost for deployment, even more for zones outside cities

The performance targets for 6G include data transfer rates up to 100 Gbps and latencies below 1 ms [40]. The key obstacle remains the cost of deployment, as higher operating frequencies result in shorter coverage distances and, consequently, an increased need for base stations [41]. Compounding

this challenge is the relatively limited financial support allocated by the European Union for 6G-related research and innovation [42]. Despite these barriers, 6G is expected not only to enhance the capabilities of applications already enabled by 5G but also to introduce entirely new services, such as holographic communications.

A summary of the generational evolution of telecommunication systems is provided in Table 1-1. While the evolution of mobile network generations has primarily been driven by the demand for higher data rates, lower latency, and wider coverage, these advances also hinge on the ability to efficiently transmit and route signals. To understand the technological choices enabling these performance gains, it is necessary to turn to the key components responsible for signal transmission.

1.1.2 Signal transmission

Signal transmission lies at the heart of modern telecommunications systems. It relies on a complex chain of components designed to amplify, filter, direct, and isolate signals with minimal loss. Among these, RF switches play a central role in enabling flexible routing across the many frequency bands used in current and emerging networks.

At STMicroelectronics and CEA-LETI, research is actively focused on the development of new RF switches for a wide range of applications, particularly in the antenna domain. Figure 1-3 illustrates a typical front-end module designed for 4G telecommunications in the sub-6 GHz frequency range. This module integrates several essential elements: power amplifiers (1), filters (2), antennas (3), and RF switches (4).

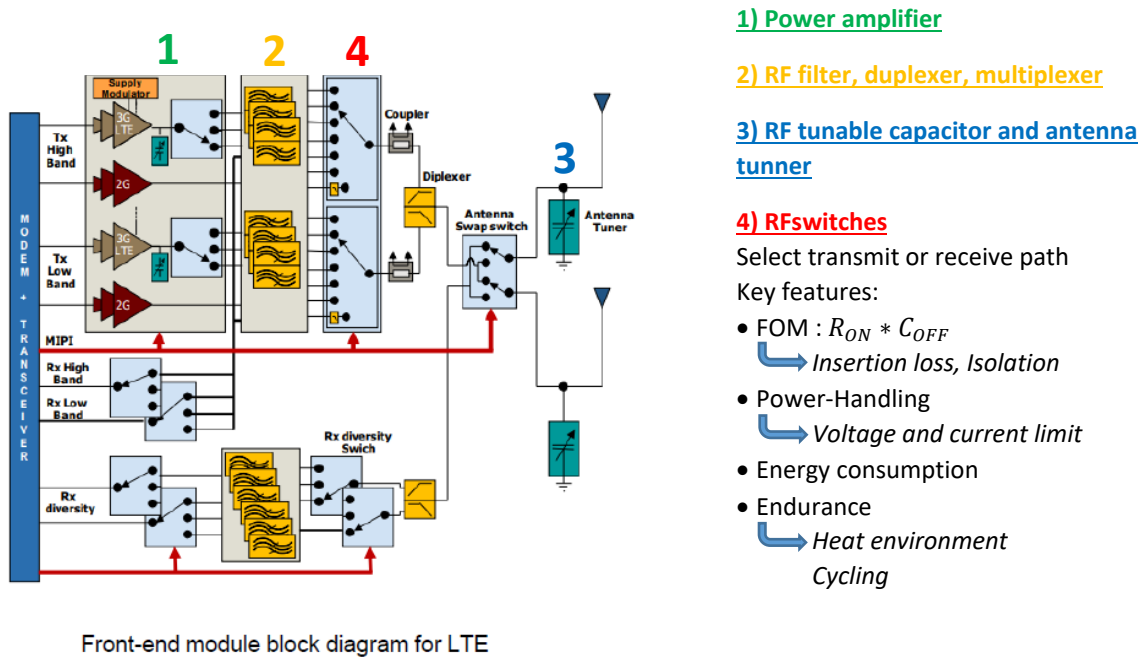


Figure 1-3*: Front end module of a 4G smartphone [43]. The right-side legend identifies its main components and underlines the key performance parameters of an RF switch.*

The switches are responsible for selecting transmission paths and routing signals, a function that becomes increasingly critical as modern smartphones operate across numerous frequency bands. The performance of RF switches is commonly assessed using multiple parameters. A primary metric is the Figure of Merit (FOM), defined as the product of the ON-state resistance (R_{ON}) and the OFF-state capacitance (C_{OFF}). This FOM quantifies the trade-off between conduction efficiency and isolation capability. In the ON state, current flows through a resistive channel, where low resistance is required

to minimize insertion losses. Conversely, in the OFF state, residual signal leakage occurs through a capacitive path, where low capacitance is desired to ensure strong isolation and suppress parasitic transmission. Additional performance indicators include power-handling in the ON-state (PH_{ON}) and in the OFF-state (PH_{OFF}), which specifies the maximum voltage or current the switch can sustain without degradation; power consumption, which must be minimized for energy-efficient operation; and endurance, often characterized by cycling, which measures the number of switching operations that can be performed before performance deteriorates.

An established technology for implementing RF switches is Micro-Electro-Mechanical Systems (MEMS). RF MEMS switches can be designed in several configurations and actuated through different mechanisms, including electrostatic, piezoelectric, thermal, or magnetic control. They may also be realized in series or shunt architectures, with either resistive or capacitive contacts [44]. Two examples of electrostatically actuated MEMS switches are shown in Figure 1-4 [45]. In the series resistive configuration, one segment of the transmission line is connected to a movable cantilever. The free end of the cantilever is suspended above the second segment of the line without direct contact. An electrode located beneath the cantilever —insulated by a dielectric to avoid short-circuiting— can be biased to generate an electrostatic force that pulls the cantilever downward. Once in contact with the second line segment, the switch enters its ON-state. This direct metal-to-metal contact ensures excellent RF performance, but it also reduces device reliability under repeated cycling. In the shunt capacitive configuration, the transmission line is initially uninterrupted, allowing the signal to propagate in the unactuated state. To switch the device OFF, a clamped–clamped membrane connected to ground is pulled downward by two electrodes (again insulated with a dielectric). This movement introduces a capacitive short circuit, effectively blocking the signal path. The dielectric layer between the membrane and electrodes plays a crucial role in extending the component's operational lifetime.

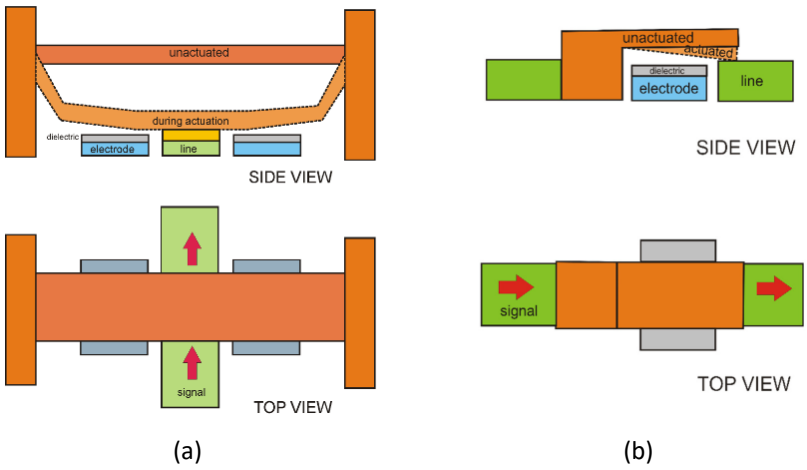


Figure 1-4: *(a) Capacitive and (b) resistive structures for RF MEMS switches [45].*

In terms of performance, capacitive MEMS structures are generally better suited for high-frequency applications compared with resistive counterparts, though their operational lifespan can be limited depending on the specific design and materials used [44]. Overall, MEMS switches offer low insertion loss, strong isolation, and excellent linearity, which minimizes signal distortion during transmission [46]. However, they also present challenges: high actuation voltages, relatively slow switching times, and comparatively large device sizes, which constrain their practicality for very high-frequency applications such as 5G, particularly in the mmWave range [44].

To overcome these limitations in commercial applications, the RF industry has widely adopted Silicon-On-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) switch. Its popularity stems from a combination of advantages: a low figure of merit ($R_{ON} \times C_{OFF}$) typically between 60 fs and 80 fs, high power-handling capability above 40 dBm, cost-effectiveness, and mature fabrication processes. Figure 1-5.a illustrates the basic principle of a CMOS switch. It consists of a source and a drain that share the same electrical polarity, separated by a silicon region with the opposite polarity. A gate electrode is positioned above this silicon layer. When a sufficient voltage is applied to the gate, it attracts charge carriers —electrons in p-type silicon or holes in n-type silicon— effectively transforming the silicon into the same type as the source and drain. This creates a conductive channel that allows current to flow between the source and drain, enabling signal transmission.

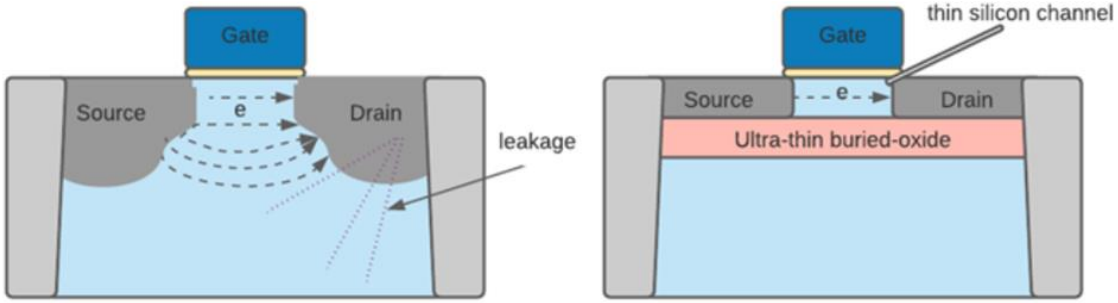


Figure 1-5: *(a) CMOS switch fabricated on a bulk silicon substrate. (b) RF-SOI CMOS switch with an oxyde layer on the substrate, enhancing isolation and RF performance [48].*

The RF-SOI CMOS switch, illustrated in Figure 1-5.b, is structurally similar to a standard CMOS switch but incorporates an additional buried dielectric layer beneath the conduction channel. This layer reduces current leakage and parasitic capacitances, thereby improving both switching speed and power efficiency. RF-SOI CMOS switches can be classified into two main types: Partially Depleted (PD-SOI) and Fully Depleted (FD-SOI). The distinction, illustrated in Figure 1-6, lies in the channel between the source and drain.

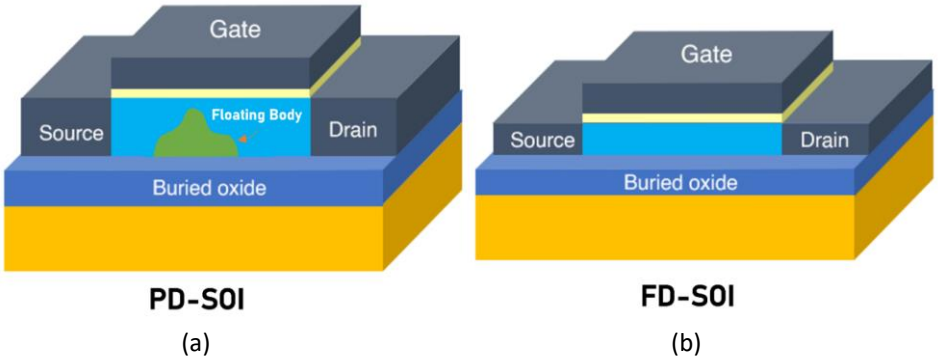


Figure 1-6: *(a) Partially Depleted SOI CMOS switch. (b) Fully Depleted SOI CMOS switch [47].*

A PD-SOI switch contains an undepleted region known as the “floating body,” which is unaffected by the gate potential. This induces current leakage and parasitic capacitances, making PD-SOI performance closer to that of bulk-silicon devices. In contrast, FD-SOI switches feature a fully depleted channel, providing superior performance and making them suitable for high-demand applications that require fast switching and low power consumption. In terms of performance, RF-SOI switches offer excellent isolation and low insertion loss. However, these advantages, along with power-handling capability, tend to diminish at frequencies above 6 GHz.

Typical performance characteristics for both RF MEMS and RF-SOI switches are summarized in Table 1-2. While RF-SOI switches offer high switching speed, low power consumption, and excellent isolation up to a few gigahertz, their performance begins to degrade at higher frequencies, and their power-handling is inherently limited by the device architecture.

Table 1-2: *Common parameters for RF MEMS and RF-SOI switches [44]-[47][49]-[51].*

	Actuation Voltage [V]	Cycling	Frequencies range	Insertion loss [dB]	Isolation [dB]	Power-handling [dBm]	R_{ON} x C_{OFF} [fs]	Switching speed [ns]
RF-MEMS	[3.6 - 90]	> 3B	[0 - 110 GHz]	[0.3 - 3]	[10 - >20]	[27 - 44]	[20 - 50]	[1000 - 300000]
RF-SOI	[(-3) - 3]	∞	[9 KHz - 220 GHz]	[<0.2 - 3]	[15 - 43]	27	[50 - 80]	[50 - 60]

These limitations have motivated the exploration of alternative switching technologies, including those based on emerging materials capable of offering enhanced performance, reduced size, and improved integration with modern semiconductor processes.

1.2 Phase-Change Materials-based RF switches

Among these emerging technologies, Phase-Change Material (PCM)-based RF switches have attracted significant attention. By exploiting the reversible transformation between conductive and insulating states in certain materials, PCM switches provide a novel mechanism for controlling signal paths in RF circuits. The development of PCM technology has a rich history, spanning from early observations of conductivity changes in molybdenum disulfide to modern high-performance RF applications.

1.2.1 History of PCM switches

The PCM principle traces back to the work of Alan Tower Waterman. While studying thermionic emissions, he observed conductivity variations in molybdenum disulfide (MoS_2). Further investigation revealed that the material could undergo a conductivity change under heating, electrical fields, or illumination, suggesting that its structure could be permanently altered [52]. PCM technology resurfaced during the early computer era, when there was interest in two-terminal non-volatile memories. Chalcogenides were among the materials explored for this purpose. In a seminal work by Stanford Ovshinsky in 1968, he demonstrated the long-term reversibility of PCM conductivity [53]. Daniel J. Shanefield later developed the first phase-change memory device based on this principle. Subsequent developments included R. G. Neale, D. L. Nelson, and Gordon E. Moore's 256-bit phase-change memory cells [54], which were not commercialized due to excessive size and power consumption. Roy R. Shanks and Craig Davis later created a 1024-bit PCM device with lower power requirements, but reliability issues still prevented commercialization. Advances in fabrication technology in the early 2000s enabled smaller PCM devices, reducing both device volume and the energy required for switching. Interest in PCM surged, leading to the first commercially available PCM memory device from BAE in 2006, followed by collaborations with Intel and STMicroelectronics. The application of PCM in RF switches began around 2010. Research teams at Carnegie Mellon University, the University of Waterloo, the University of Limoges, and Northrop Grumman and HRL Laboratories developed the first PCM-based RF switch structures, introducing the indirect heating principle [55][56]. Subsequent improvements allowed for monolithic integration of PCM switches, enabling easy incorporation into the Back-End-Of-the-Line (BEOL) of CMOS and other semiconductor processes. Despite these advances, research on PCM RF switches has declined, largely due to the substantial

investment required to enhance two critical performance metrics: power-handling and switching cycles.

Indeed, achieving the performance levels required to surpass RF-SOI switches demands a minimum power-handling of 36 dBm in both ON and OFF states, along with a maximum R_{ON} x C_{OFF} FOM between 30 fs and 40 fs. Additional parameters, such as switching speed, power consumption, and process compatibility, must also approach those of RF-SOI devices [51]. PCM-based RF switches generally provide sufficient PH_{ON}, but their OFF-state performance is limited by their intrinsic design, which will be detailed in the next sections. These limitations can be mitigated by stacking multiple PCM switches, although this strategy introduces additional parasitic capacitances that may affect overall performance [57]. Typical performance metrics for PCM RF switches are summarized in Table 1-3, and further explanations regarding the factors influencing each of these parameters are provided throughout the rest of this manuscript.

Table 1-3: *Common parameters for GeTe RF switches with electrical [51][55][58]-[65] and optical actuations [66]-[69].*

PCM RF switch	Cycling	Insertion loss [dB]	Isolation [dB]	Power-handling [dBm]	R_{ON} x C_{OFF} [fs]	Switching speed [ns]
Electrical actuation	1B	0.1 - 6	16 - 39	37	7 - 200	300 - 2000
Optical actuation	> 30K	0.6	20	37	26 - 45	30 - 6000

Currently, Tower Semiconductor is the only commercial foundry offering a process for PCM RF switches. They have successfully advanced PCM switch performance, delivering, in collaboration with Northrop Grumman, models approaching RF-SOI device levels, with an $R_{ON} \times C_{OFF}$ FOM as low as 12.5 fs and cycling endurance exceeding one billion operations [65]. However, recent publications from Taiwan Semiconductor Manufacturing Company suggest new developments in PCM-based RF switches [70][71], indicating that they may also be preparing a commercial offering in the near future.

Overall, while PCM RF switches have made significant progress and can now approach the performance of RF-SOI devices, their actual behavior and efficiency are strongly dependent on the choice of chalcogenide material and its structural properties. Understanding these material characteristics is therefore essential for optimizing switch design and operation.

1.2.2 PCM RF switches operation

To appreciate how PCM RF switches achieve their functionality, it is necessary to examine the materials at their core. These switches mostly utilize chalcogenide alloys from the GeSbTe ternary system (Germanium (Ge), Antimony (Sb), and Tellurium (Te)), whose composition and phase-change properties directly influence switching performance and stability. Figure 1-7 illustrates the characteristics of various combinations of these elements. As shown in Figure 1-7.a, compositions with higher Ge content exhibit higher crystallization temperatures. This trend is confirmed in Figure 1-7.c, which presents the structures of three materials; those richer in GeTe show elevated crystallization temperatures. Figure 1-7.b further demonstrates that a higher GeTe proportion enhances the phase stability of the material: amorphous regions require higher temperatures to crystallize, reducing the likelihood of unintentional structural changes over time. Conversely, Sb-rich compositions are preferred in applications demanding high switching speeds, such as memory devices that require rapid data writing.

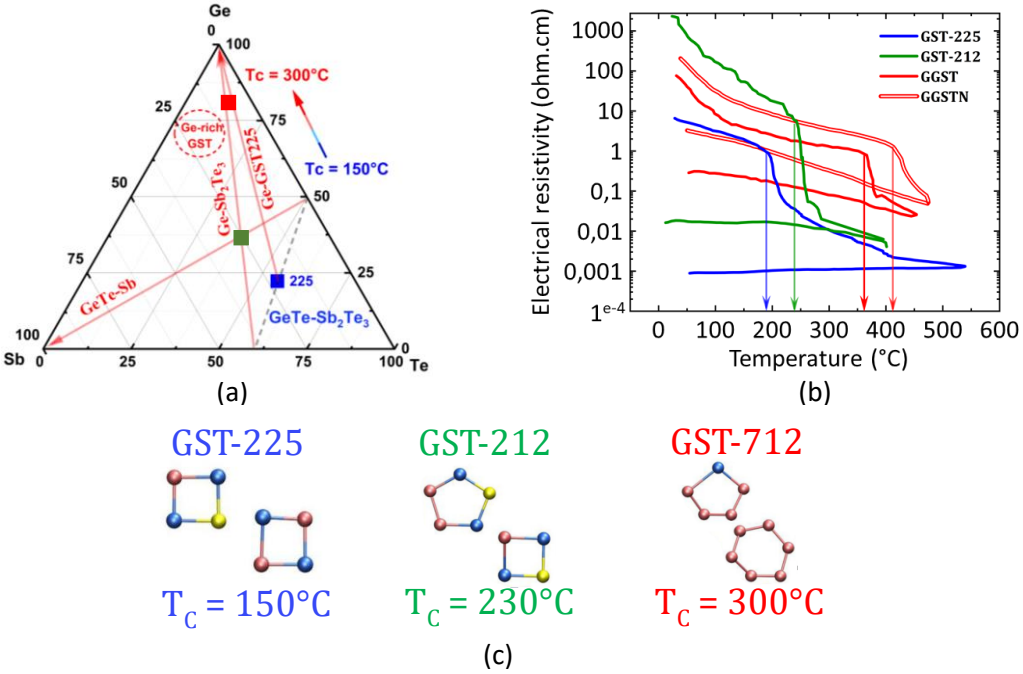


Figure 1-7: *Characteristics of different Ge-Sb-Te materials. (a) Ge-Sb-Te phase diagram showing compositional stability regions. (b) Resistivity versus temperature for various compositions. (c) Atomic structures of three representative materials, color-coded to match the diagram and resistivity graph, with their respective crystallization temperatures.*

When combined, these materials exhibit both an amorphous phase and at least one crystalline phase. The amorphous phase, illustrated on the right of Figure 1-8, is characterized by a disordered atomic structure and low electrical conductivity, effectively blocking the signal. In contrast, the crystalline phase, shown on the left of Figure 1-8 has an ordered atomic arrangement and high conductivity, allowing efficient signal transmission between electrodes.

The primary material investigated in this PhD work is GeTe, which is also the most commonly used for RF PCM switches. Its widespread adoption stems largely from its high R_{OFF}/R_{ON} ratio —on the order of 10^4— providing a clear distinction between the crystalline and amorphous phases. This characteristic ensures better isolation in the OFF-state compared to other PCMs based on similar compounds.

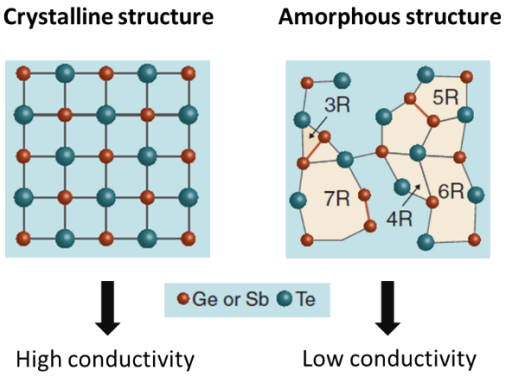


Figure 1-8: *Two main structural phases of a PCM. (left) Crystalline phase with high electrical conductivity, allowing signal transmission. (right) Amorphous phase with low electrical conductivity, blocking the signal [72].*

In contrast, GeSbTe (GST) is more frequently employed in memory applications due to its favorable balance of switching speed and stability. In memory devices, GST can achieve switching speeds below 1 ns, significantly enhancing data writing and reading performance [73]. Doped variations of GST, such

as Ge-rich GST or Sb-rich GST, further improve data retention thanks to higher crystallization temperatures and enhanced thermal stability [74][75]. While SbTe has also been explored as an RF PCM, its performance generally falls short compared to GeTe.

Another class of PCM is Vanadium Dioxide (VO_2), a transition metal oxide. Unlike chalcogenides, VO_2 undergoes a Mott transition, behaving as an insulator at room temperature and becoming metallic above 340 K. However, this material must be maintained above its transition temperature to remain conductive, which limits its bistability. Additionally, its relatively low transition temperature makes it susceptible to unintended property changes during operation. Table 1-4 summarizes the key performance characteristics of these four materials:

Table 1-4: *Performance comparison between GeTe [55][58][59][63][66][69], GST [59][76]-[78] , SbTe [58] and VO_2 [58][62][79]-[81].*

PCM	Thermal conductivity [$W.m^{-1}.K^{-1}$]	Crystallization temperature [K]	Melting temperature [K]
GeTe	0.3 - 2.2	470	998
GST	0.2 - 0.5	410 - 440	910
SbTe	-	420	-
VO_2	6	Semiconductor -> metallic: 340	-

During RF switch operation, the structural state of chalcogenide materials must be actively changed. This can be achieved through optical or electrical actuation, both of which generate the heat necessary for the phase transformation. The optical method, illustrated in Figure 1-9, employs an optical fiber connected to a pulsed laser source directed at the PCM. When illuminated, the PCM absorbs the light, causing its temperature to rise and triggering the phase change. Optical heating reduces parasitic capacitances that can occur with electrical actuation and ensures a more uniform temperature distribution across the PCM. Current research is focused on achieving high performance while using cost-effective laser sources, potentially making this approach practical for RF switch applications [67]

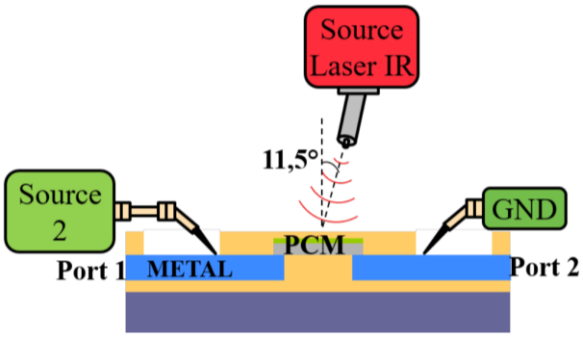


Figure 1-9: *Optical actuation of a PCM.*

The electrical method can be implemented in two ways: direct or indirect. In the direct approach, a voltage pulse is applied across the RF contacts themselves, inducing a Joule heating effect within the PCM to change its phase. This method is particularly advantageous for amorphization, as it avoids introducing additional metallic elements that would increase parasitic capacitances. However, it has the drawback that the RF and DC paths are not inherently decoupled, necessitating an extra decoupling circuit in the biasing network, which can introduce signal losses [82]. The electrical-indirect method, which is the approach adopted in this work, relies on a thermo-resistive metal element referred to as a heater, as illustrated in Figure 1-10.

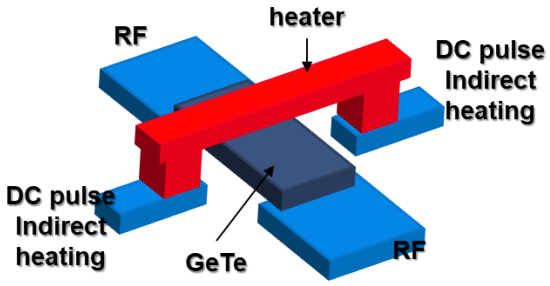


Figure 1-10: *3D view of the indirect actuation build.*

When a voltage pulse is applied to the heater, it behaves like a resistor, generating heat through the Joule effect. This heat is then transferred to the PCM, inducing the structural transformation. Depending on the desired phase, different types of pulses can be applied, as illustrated in Figure 1-11. To induce crystallization, a SET pulse is used. This pulse delivers sufficient heat to the PCM to reorganize its structure into the crystalline phase. Typically lasting on the order of 1 µs, the SET pulse switches the device into its ON state, enabling signal transmission between the RF electrodes.

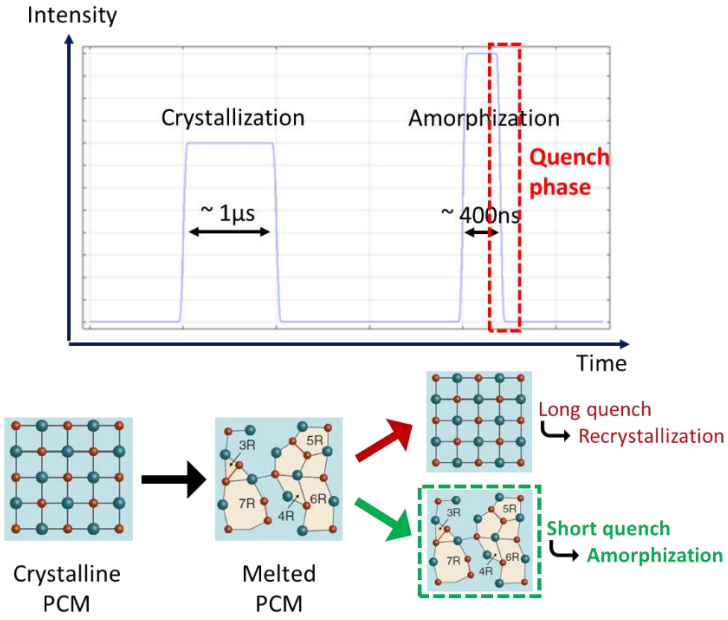


Figure 1-11: *Amorphization process for a PCM.*

In contrast, to amorphize a crystalline PCM, a stronger RESET pulse is applied to raise the PCM above its melting temperature. The critical step is then to rapidly cool the material to prevent spontaneous recrystallization, thereby stabilizing the disordered amorphous phase. During this quenching process, the PCM passes through the temperature range between crystallization and melting. If it remains within this range for too long, recrystallization can occur. For this reason, the RESET pulse must be short, ensuring that cooling is as rapid as possible. Extending the pulse duration would allow heat to diffuse into surrounding layers, elevating the local temperature during quenching and slowing the cooling process, ultimately reducing the effectiveness of amorphization.

Minimizing the quench duration is also essential for improving insulation and PH_{OFF}, as increasing the amorphous fraction of the PCM reduces the likelihood of unintended switching. Consequently, switch design must achieve a delicate balance: on the one hand, heat must be removed from the PCM as efficiently as possible during quenching; on the other, sufficient heating must still be delivered during the melting phase without incurring excessive energy consumption.

In summary, the operation of PCM RF switches relies heavily on the intrinsic properties of chalcogenide materials and their ability to reversibly switch between crystalline and amorphous states. However, to translate these material-level phenomena into practical and reliable RF devices, careful consideration must be given to the conception and design of the switch structure itself.

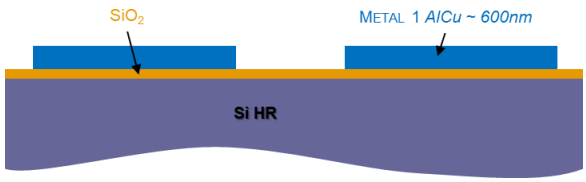
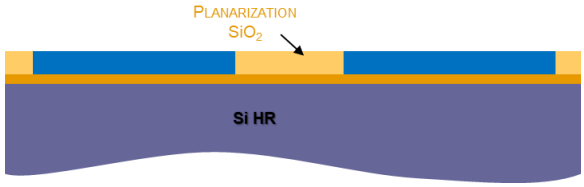
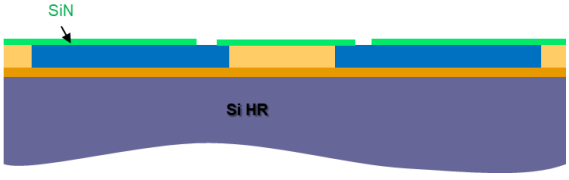
1.3 PCM-based RF switch conception

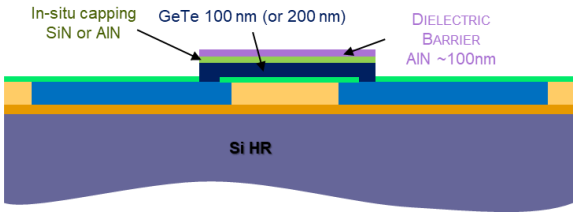
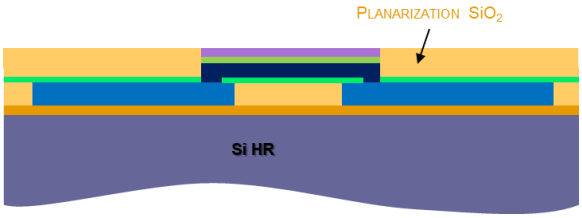
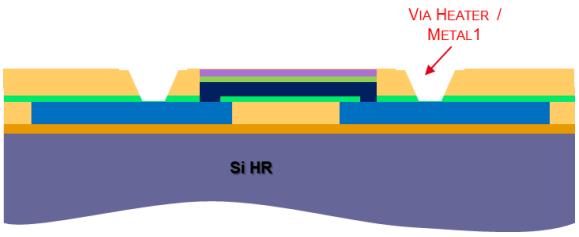
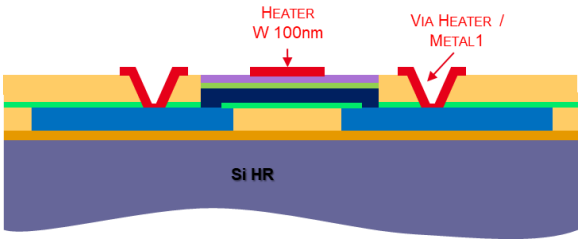
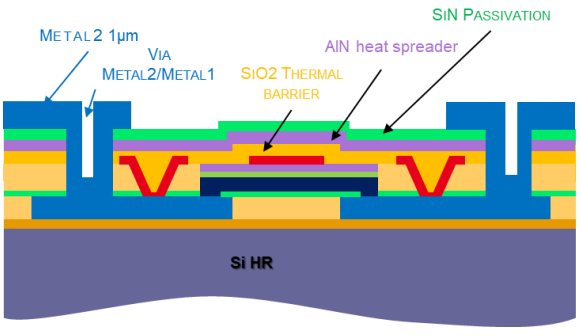
Building upon this understanding of PCM operation at the material level, the next step is to consider how these properties are integrated into complete device structures. This involves the conception of PCM-based RF switches, starting with the fabrication process that enables their realization.

1.3.1 Process flow overview

The fabrication process of the switches studied in this work was adapted from earlier developments reported in [83]. Building on that foundation, Table 1-5 outlines one of the processes employed in this thesis. This process served as the baseline for the subsequent variations used to fabricate the switches analyzed in Chapter 4.

Table 1-5: *Process flow for PCM-base RF switches with encapsulated PCM.*

STEP 1: Metal 1 Switches are fabricated on 200mm high-resistive silicon wafers (>5000 Ω.cm). A SiO_2 layer is deposited onto the substrate, with its thickness optimized either to leverage the substrate's thermal evacuation properties or, if made sufficiently thick, to emulate integration in the upper layer of the BEOL. Next, a first metal layer composed of AlCu, along with the corresponding adhesion layers and diffusion barriers, is deposited by PVD and patterned to form the RF and DC signal lines. The thickness of this metal layer is also optimized; thinner films enable easier patterning, while thicker ones reduce RF losses.	
STEP 2: SiO_2 A SiO_2 insulator is deposited by PECVD (Plasma-Enhanced Chemical Vapor Deposition) and subsequently planarized through CMP (Chemical Mechanical Planarization), preparing a smooth surface for PCM deposition.	
STEP 3: Dielectric 1 A thin dielectric layer (Si_3N_4) is deposited and patterned. This layer acts as a barrier between the SiO_2 and the PCM, preventing GeTe oxidation and mitigating void formation caused by outgassing from the underlying SiO_2.	

STEP 4: PCM and Dielectric 2 The PCM layer is deposited, followed by the in-situ deposition of a Si_3N_4 capping layer to prevent oxidation. Next, an AlN dielectric is deposited by PVD. AlN ensures electrical insulation between the PCM and the heater while maintaining good thermal conductivity. Its thickness must be carefully optimized: thin enough to promote heat transfer, but sufficiently thick to guarantee high electrical isolation. Patterning is then carried out by photolithography, Reactive Ion Etching (RIE), and stripping.	
STEP 5: SiO_2, Planarization Another SiO_2 layer is deposited via PECVD, and the surface is planarized with CMP to provide a flat surface for heater deposition.	
STEP 6: Vias opening Vias are opened using RIE down to Metal 1, creating electrical contact paths between the heater and the underlying metal.	
STEP 7: Heater The tungsten heater is deposited by PVD and patterned through dry etching.	
STEP 8: Dielectric 3 and Metal 2 The final capping stack is deposited. It consists of SiO_2 (PECVD), ensuring thermal confinement, followed by AlN (its role is detailed in Section 4.1), and a Si_3N_4 passivation layer that protects the device. Vias are then opened between Metal 1 and Metal 2 by patterning the dielectric stack, and a final metal layer is deposited by PVD. This Metal 2 layer provides additional routing flexibility, enabling circuit designs with line crossings between Metal 1 and Metal 2.	

While the fabrication process defines the sequence of steps required to realize a PCM-based RF switch, the overall device performance is equally determined by the way its different layers are arranged within the technological stack.

1.3.2 Typical design and conception of a PCM-based RF switch.

Understanding these structural arrangements is therefore essential, as the placement of each layer directly impacts heat transfer, switching efficiency, and reliability. **Erreur ! Source du renvoi introuvable.** illustrates the two principal technological stacks for a PCM-based RF switch. The distinction between these configurations lies in the relative positioning of the PCM and heater layers within the stack.

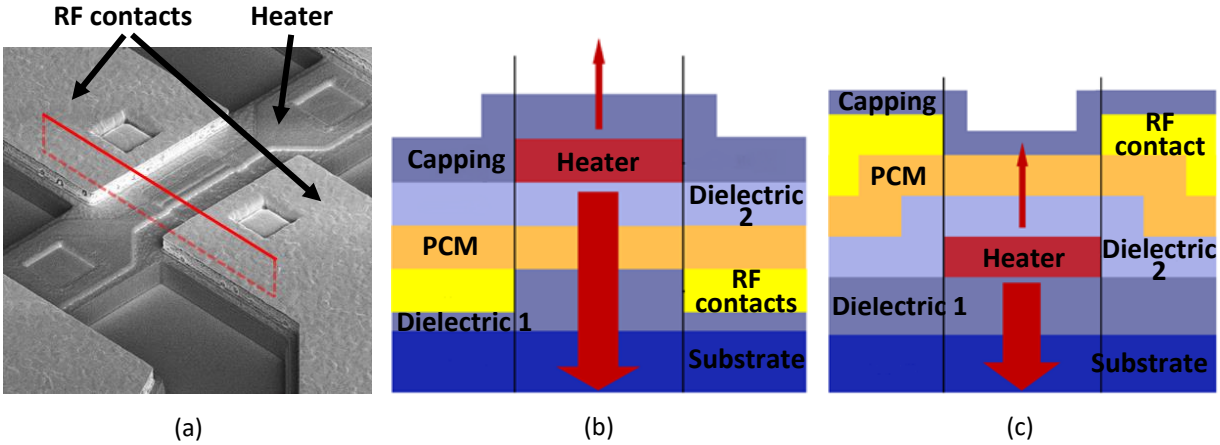
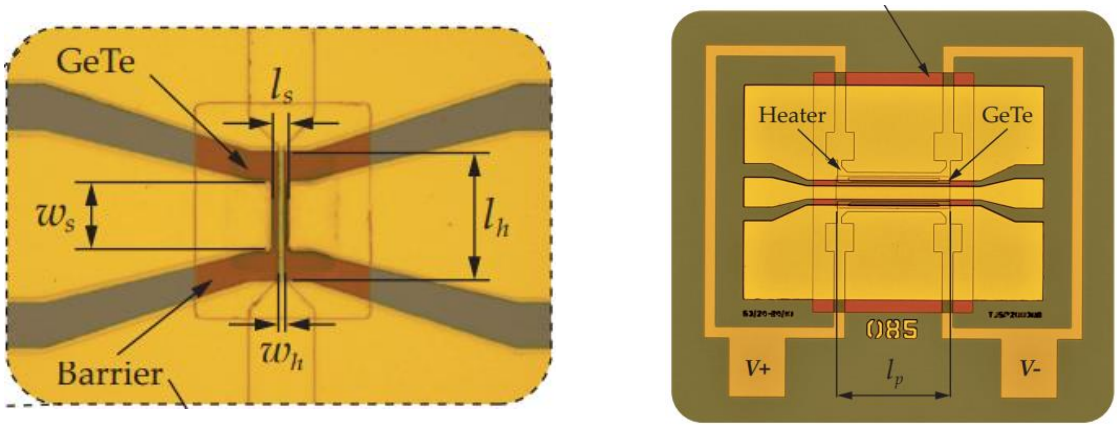


Figure 1-12: *(a) Top-view photograph of a PCM-based RF switch. The red rectangle indicates the cutting plane corresponding to the two schematics shown alongside. (b) Cross-sectional schematic of a Heater-on-Top architecture. The red arrows depict the heat flux generated by the heater: the majority flows downward into the PCM (large arrow), while a smaller portion escapes upward toward the device surface (small arrow). (c) Cross-sectional schematic of a PCM-on-Top architecture, where the PCM layer is placed closer to the substrate.*

The red arrows in **Erreur ! Source du renvoi introuvable.**.b and **Erreur ! Source du renvoi introuvable.**.c indicate the distribution of heat fluxes, showing that most of the thermal energy dissipates toward the substrate. In the first configuration (**Erreur ! Source du renvoi introuvable.**.b), the PCM is placed closer to the substrate. This arrangement facilitates the quench step, since heat can be evacuated more rapidly from the PCM. Additionally, a greater fraction of the heat generated by the heater contributes to raising the PCM temperature, as part of the flux is directed upward through the material. However, this advantage also comes with a drawback: the PCM, being in close proximity to the substrate, tends to lose heat more quickly, making the heating step less efficient. In the second configuration (**Erreur ! Source du renvoi introuvable.**.c), the heater is positioned closer to the substrate. This improves heat distribution within the heater, thereby reducing the risk of localized overheating, and it also enables faster cooling of the heater during the quench. On the downside, this design requires higher voltages during the heating phase to bring the PCM to its transition temperature, and the PCM itself cools less efficiently during quenching.

The Heater-on-Top structure shown in **Erreur ! Source du renvoi introuvable.**.b serves as the basis for the work presented in this thesis. This architecture provides several avenues for tuning the performance of the switch; however, such design efforts generally involve trade-offs rather than straightforward improvements, as enhancing one parameter often comes at the expense of another. The designs discussed thus far correspond to series configurations, as illustrated in Figure 1-13.a [72], where the PCM is positioned directly within the signal path. An alternative approach is the shunt configuration, shown in Figure 1-13.b, in which the PCM is placed in parallel with the signal line. In this case, the device operates differently: when the PCM is in its amorphous state, the RF signal propagates through the main path, while in the crystalline state, the PCM provides a short circuit to ground, diverting the signal away from the transmission line.



(a) (b)

Figure 1-13: *(a) Series configuration of a PCM-based RF switch, where the PCM is placed directly in the RF signal path. (b) Shunt configuration of a PCM-based RF switch, in which the PCM is connected in parallel to the signal line, providing a short circuit to ground in the crystalline state [72].*

While the choice of technological stack defines the overall architecture of the device, its ultimate performance is also determined by the precise geometry of each layer and the way thermal and electrical stimuli are applied during operation.

1.3.3 First order analysis of the impact of geometry and voltage pulse shape on performance.

To better understand these influences, it is useful to perform a first-order analysis of the device geometry and voltage pulse shaping, as both directly govern heating efficiency and quenching effectiveness in PCM-based RF switches. One of the central challenges in PCM switch design is achieving a suitable balance between heating efficiency and effective quenching during the amorphization process. Reaching the target temperature for crystallization or melting can be facilitated through several design choices, yet these often introduce constraints on how efficiently the material can be cooled during quenching.

Figure 1-14 presents the basic model used in this work. The key notations introduced are: the PCM length (L_{PCM}), the RF_{gap} length (L_{RFgap}) and the heater width (W_h). The yellow arrow indicates the trajectory of the RF signal when the switch is in the ON state. The heat flux directions during the quench step are also illustrated, with red arrows showing the main evacuation paths. The relative arrow sizes highlight the dominant thermal sinks, namely the substrate and the RF contacts Proper dimensioning of the switch is therefore a critical factor in defining its performance. Throughout this PhD work, the influence of various layer dimensions has been systematically studied through both simulations and experimental measurements, as further detailed in Chapter 3. For clarity, the key impacts of selected layers from the representative stack shown in Figure 1-14 will be summarized here.

1.3.3.1 Effect of the substrate

Starting from the bottom of the technological stack, the substrate plays a key role in determining amorphization efficiency through its distance from the PCM. Reducing this distance accelerates quenching, allowing the PCM to cool more rapidly below its recrystallization temperature and thereby increasing the amorphous fraction that can be achieved. However, this same proximity also causes faster heat dissipation during the heating step. As a result, the heater must generate more heat to reach the required PCM temperature, which in turn demands higher current, increases overall energy

consumption, and raises the maximum temperature inside the heater. Operating closer to its breakdown limit also subjects the heater to greater thermal stress, accelerating fatigue over repeated cycling. A trade-off in the PCM-substrate spacing must therefore be identified to enhance amorphization efficiency while mitigating adverse effects on energy consumption, heater reliability, and long-term device performance.

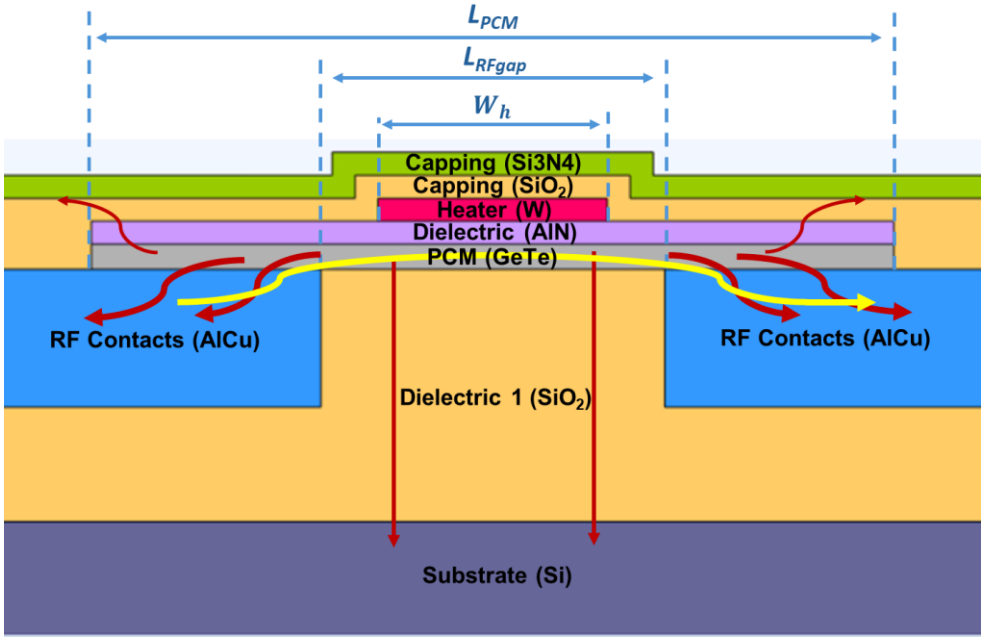


Figure 1-14: *Two-dimensional cross-section of the generic PCM-based RF switch studied in this work. The yellow arrow indicates the current path in the ON-state, while the red arrows represent heat flux directions during the quench step. Larger arrows correspond to more efficient evacuation paths toward the main thermal sinks.*

1.3.3.2 Effect of Dielectric 1

The next layer in the technological stack is the dielectric located between the substrate and the contacts, referred to as dielectric 1. Reducing its thickness brings the substrate closer to the PCM, which accelerates heat evacuation during the quench. However, maintaining a sufficient thickness is generally preferred, as it reduces the dependence of the switch's performance on the substrate's thermal properties. This ensures more stable behavior when the device is integrated into the upper layers of the CMOS back-end-of-line (BEOL). Dielectric 1 also serves to separate the two RF contacts, defining the RF_{gap}, which is one of the most critical design parameters of the switch. The amount of PCM that can undergo amorphization directly depends on the RF_{gap} length. A longer RF_{gap} makes it easier to heat the PCM center —since the contacts are further away— and enables the formation of a larger amorphous region. This improves OFF-state isolation and increases PH_{OFF} while decreasing C_{OFF}, provided the heater is properly designed to maximize amorphous length while minimizing parasitic capacitances. At the same time, a longer RF_{gap} increases the crystalline PCM length in the ON-state, which raises R_{ON} and degrades PH_{ON} [84]. In this work, priority is given to longer RF_{gap} to meet the challenge of achieving PH_{OFF} values above 36 dBm. Regarding the RF contacts themselves, their thickness is also significant: due to their good thermal conductivity, thicker contacts enhance heat evacuation during the quench step, further supporting efficient amorphization.

1.3.3.3 Effect of the PCM

The PCM itself plays a crucial role, particularly the portion located above the RF_{gap}. Its length influences the switch's performance in a manner closely linked to the RF_{gap} dimensions discussed previously.

Because the RF contacts are highly effective thermal sinks, PCM regions directly above or very close to the contacts often remain crystalline during amorphization, as the melting temperature is not reached in these areas. The PCM width significantly affects R_{on} and PH_{ON}. A wider PCM section reduces current density, lowering R_{on} and improving PH_{ON}. PCM thickness also impacts multiple performance factors. A thinner PCM layer switches faster, as less material must undergo the phase transition. However, this also increases R_{ON} value and insertion losses. Thinner PCM facilitates melting, allowing the formation of a longer amorphous region, which reduces C_{OFF} and enhances isolation. The impact on power-handling is nuanced: in the ON-state, a thinner PCM increases current density, lowering PH_{ON}, whereas in the OFF-state, the longer amorphous zone improves voltage tolerance, enhancing PH_{OFF}.

1.3.3.4 Effect of Dielectric 2

The dielectric layer above the PCM, often referred to as Dielectric 2 or the dielectric barrier, has a performance strongly dependent on its material properties. If the material is a good thermal conductor, heat generated by the heater tends to spread more horizontally toward the RF contacts rather than vertically into the PCM. This requires a higher voltage and greater energy consumption to sufficiently heat the PCM. On the other hand, during the quench, this improved lateral heat evacuation facilitates faster cooling of the PCM near the contacts, enhancing amorphization of the melted regions. Conversely, if the dielectric barrier is a poor thermal conductor, the heat from the heater is more effectively directed toward the PCM, making it easier to reach the desired phase-change temperature. However, this also slows the quench process by confining heat within the PCM, increasing the risk of unintended recrystallization instead of maintaining the amorphous state. Regardless of the material choice, the layer thickness must also be optimized. A thicker dielectric reduces parasitic capacitance between the heater and PCM, while a thinner layer improves heat transfer from the heater to the PCM, lowering the energy required for heating. Achieving the right balance between these factors is essential for reliable and efficient switch operation.

1.3.3.5 Effect of the heater

The dimensions of the heater play a key role in both the thermal and RF performance of the switch. In the ON-state, the heater size does not directly affect the R_{ON} value. This is because R_{ON}, typically measured at low frequency, depends on the amount of crystalline PCM; regardless of heater size, the PCM will be fully crystallized in the ON-state. However, insertion losses are influenced by parasitic capacitance between the heater and the crystalline PCM. A larger heater increases the interacting surface with the PCM, which increases the fraction of the signal that is short-circuited through this capacitance. The signal frequency further modulates this effect through the capacitive impedance:

$$Z_C = \frac{1}{j\omega C}$$

where Z_C is the impedance of the parasitic capacitance, C is its capacitance, and $\omega = 2\pi f$, with f being the signal frequency. As frequency increases, Z_C decreases, allowing more signal to bypass the PCM via the parasitic path, thereby increasing insertion losses. In terms of PH_{ON}, measurements at low frequency depend primarily on the crystalline PCM amount, similar to R_{ON}, and are thus largely unaffected by heater size. At higher frequencies, however, the parasitic capacitance could influence PH_{ON}, potentially modifying the effective power crossing the PCM, though this effect remains to be experimentally confirmed. Heater dimensions have a stronger influence in the OFF-state. A wider heater facilitates heating of the PCM edges, leading to a larger amorphized region. This improves both C_{OFF} and PH_{OFF} values. At the same time, more metal interacting with the crystalline PCM can slightly

increase parasitic effects, potentially affecting C_{OFF}. Consequently, careful sizing of the heater is crucial to achieve an optimal balance between efficient amorphization and minimal parasitic impact.

1.3.3.6 Effect of the capping

Finally, the top part of the switch, known as the capping, consists of various dielectric layers that cover the full length of the device. These layers are passive and primarily serve as a barrier against external contaminants. Because conduction and convection between the capping and the ambient air are much less effective than the conduction between the heater and the capping, the temperature of the capping largely follows that of the heater. As a result, the capping itself has a limited direct thermal impact on the switch's performance. It should be noted, however, that the capping does not fully represent the thermal dissipation occurring in the top part of the device. In practice, the interconnections built above the switch in the BEOL contain metallic features that act as heat spreaders. These metallic elements, rather than the capping dielectrics, are the components that significantly influence the thermal behavior of the upper portion of the switch.

1.3.3.7 Effect of the voltage pulse's shape

Another key factor in balancing the heating and quench steps is the shape of the voltage pulses applied to the heater. Shorter pulses enable faster switching and reduce mechanical and thermal stress on the materials, but they require higher voltages. Moreover, controlling the PCM temperature becomes more challenging, increasing the risk of exceeding the desired melting point. Longer pulses, on the other hand, are easier to manage and can promote larger amorphization of the PCM, as the heater has more time to transfer heat effectively. However, the extended heat diffusion also affects the surrounding layers of the switch, raising the overall temperature near the PCM. This higher local temperature can hinder efficient quenching, reducing the reliability of the amorphization process.

1.1.1.1 Summary

Table 1-6 provides an overview of how the dimensions of each layer, as well as the shape of the voltage pulse, influence the performance of the PCM-based RF switch.

Table 1-6 : *Summary of the impact of each layer's dimensions on the performance of the PCM-based RF switch.*

Layer / Parameter	Impact on Switch Performance
Substrate	Acts as an excellent thermal sink. A substrate closer to the PCM speeds up the quench, while a more distant substrate facilitates PCM heating.
Dielectric 1	Thermally isolating and sets the RF_{gap} between contacts. Longer RF_{gap} make it easier to heat the PCM center and extend the potential amorphous zone, improving isolation, PH_{OFF} and lowering C_{OFF} (if heater width is adapted). However, longer RF_{gap} also increase R_{ON}, reducing PH_{ON} value.
PCM	Larger PCMs increases R_{ON} and PH_{ON}. Thinner PCM layers produce longer amorphous regions, improving C_{OFF} and PH_{OFF}, but increase current density, reducing PH_{ON}.
Dielectric 2	• Thermally conductive: harder to heat PCM but speeds quench. • Thermally insulating: easier to heat PCM but slows quench. • Thickness: thicker layers reduce parasitic capacitance but make PCM heating harder.
Heater	At low frequency, dimensions do not affect R_{ON} and PH_{ON}. Larger heaters and higher signal frequencies increase insertion losses due to parasitic capacitance. Wider heaters increase amorphous PCM length, boosting PH_{OFF}. C_{OFF} is influenced by both the longer amorphous zone (reduces C_{OFF} and the larger heater-PCM interface (increases C_{OFF}).

Top capping	Thermally isolating; tends to follow heater temperature, limiting impact on switch behavior. Mainly serves as a passivation layer.
Voltage pulse	Short pulses improve switching speed and component reliability but require higher voltages. Long pulses are easier to control and allow more heat to reach PCM, but lengthen quench duration due to hotter surrounding layers.

In summary, the geometry of each layer and the shape of the voltage pulse play decisive roles in balancing heating and quenching efficiency, ultimately determining the overall performance of PCM-based RF switches. Yet, beyond geometrical considerations, the intrinsic properties of the materials composing each layer —particularly the heater— are equally critical.

1.3.4 Common materials used for the heater

For this reason, the following section examines the common materials employed for the thermo-resistive heater. Their thermal and electrical characteristics directly influence heat generation, distribution, and evacuation, making material selection a central step in PCM-based RF switch conception. As with the PCM analysis in Section 1.2.2, comparisons are made between candidate materials based on their intrinsic properties and resulting performance trade-offs. The heater must fulfill several requirements: it must generate sufficient Joule heating to induce a phase transition in the PCM, withstand repeated exposure to high temperatures (hence requiring a high melting point), and present a resistivity that is high enough to enhance heating efficiency without demanding excessive energy. Additional material properties are also critical:

- The electrical conductivity

- The Thermal Coefficient of Resistance (TCR): This coefficient represents the influence of temperature on the heater's resistivity. A positive TCR means that the resistivity of the material increases as the temperature rises, while a negative TCR means that the resistivity decreases with increasing temperature. The higher the TCR value, the stronger the effect of temperature on resistivity.

- The thermal diffusivity (α): This parameter represents how quickly heat propagates through a material; a higher diffusivity means the material heats up or cool down more rapidly. It is defined by the formula:

$$\alpha = \frac{\kappa}{\rho C_p} \tag{1}$$

  with:

  - The thermal conductivity (κ)

  - The density of the material (ρ): A higher density lowers the thermal diffusivity because the heat must travel more mass per unit volume.

  - The specific heat capacity (C_p): This represents the amount of energy required to raise the temperature of one unit mass of material by one degree Celsius. A high specific heat makes the material more resistant to temperature changes, while a low specific heat allows the material to heat up or cool down more quickly, thereby increasing the thermal diffusivity.

The material used throughout this PhD work is tungsten (W). With a melting point of about 3700 K, tungsten is the most thermally resistant option among common heater materials. Its resistivity at room temperature ranges from $5e^{-9}$ Ω.cm for thinner films to $5e^{-10}$ Ω.cm for thicker ones [85][86]. Although not the highest, this resistivity is balanced by its excellent thermal conductivity of 174 $W.m^{-1}.K^{-1}$ [87] which promotes homogeneous temperature distribution inside the heater and, by extension, in the PCM. Tungsten also exhibits a positive TCR of 0.0045 $°C^{-1}$ [88], a specific heat of 134 - 141 $J.Kg^{-1}.K^{-1}$ [89][90] and a density of 19.25 - 19.35 $g.cm^{-3}$ [90]. These values yield a thermal diffusivity of about 65.8 mm^2/s, consistent with reported values [91], placing tungsten as a material capable of both rapid heating and efficient cooling. Molybdenum (Mo) [92][93] offers similar characteristics, though slightly less favorable. Its resistivity is close to that of tungsten but its thermal conductivity (~140 $W.m^{-1}.K^{-1}$ [94][95]) and melting temperature (~2895 K [94][95]) are both somewhat lower. With a specific heat of 255 - 277 $J.Kg^{-1}.K^{-1}$ [89][96] and a density of 10.1 - 10.3 $g.cm^{-3}$ [96], Molybdenum reaches a thermal diffusivity of about 51.6 $m^2.s^{-1}$ [97]. This lower diffusivity translates into slower temperature variations compared to tungsten, yet still makes molybdenum a solid candidate for high-temperature PCM applications.

By contrast, nickel-chromium alloys (NiCr, NiCrSi) represent the opposite end of the spectrum. Their resistivity is significantly higher (10^{-4} Ω.cm [98]), which improves heat generation efficiency but at the cost of higher power consumption. This higher resistivity is advantageous with respect to parasitic capacitances. Consequently, the heater dimensions can be reduced, which in turn lowers the parasitic capacitance between the heater and the PCM [99]. Their thermal conductivity is much lower, around 12 $W.m^{-1}.K^{-1}$ [100], promoting highly localized heating but limiting lateral heat distribution. These alloys also have a much lower melting point, around 1670 K [101], which restricts their use in conjunction with high-melting-point PCMs such as GeTe. For NiCr, the TCR is 0.0004 per °C [88], while the specific heat lies between 380 and 500 $J.Kg^{-1}.K^{-1}$ [89][102], and the density is between 7.75 and 8.65 $g.cm^{-3}$ [102]. Together, these values result in a thermal diffusivity of only 3.32 $m^2.s^{-1}$, indicating very slow heating and cooling. This not only increases energy consumption but also lengthens the quench, reducing the efficiency of amorphization. The key thermal and electrical properties of the materials discussed for heater integration are summarized in Table 1-7.

Table 1-7: *Thermal conductivities and electrical resistivities of commonly used heater materials for PCM-based RF-switches.*

Material	Thermal conductivity [$W.m^{-1}.K^{-1}$]	Electrical resistivity [Ω.cm]	Melting temperature [K]	TCR	Specific heat [$J.Kg^{-1}.K^{-1}$]	Density [$kg.m^{-3}$]	Thermal diffusivity [$m^2.s^{-1}$]
Tungsten (W)	174	$5e^{-10}$	3700	0.0045	134 - 141	19250 - 19350	65.8
Molybdenum (Mo)	140	$5e^{10}$	2895	-	255 - 277	10100 - 10300	51.6
Nickel-Chromium(-Silicon) (NiCr (-Si))	12	10^{-4}	1670	0.0004	134 - 141	77500 - 86500	3.32

In conclusion, the choice of heater material represents a delicate compromise between thermal conductivity, electrical resistivity, melting temperature, and diffusivity. Refractory metals such as tungsten and molybdenum offer robustness and efficient heat distribution, making them suitable for high-temperature PCMs like GeTe. In contrast, alloys such as NiCr or NiCrSi provide higher resistivity and localized heating but suffer from lower thermal stability, which limits their use in demanding conditions. Ultimately, the heater material must be selected according to the target performance

requirements and the trade-offs acceptable for a given application into account the difficulties of finding good balances between the different performance parameters of the devices.

1.4 Conclusion on the chapter

In this chapter, the technological landscape of RF switches was reviewed, beginning with a historical overview of their development and extending to the analysis of RF-MEMS, RF-SOI, and PCM-based solutions. After recalling the main expectations for RF switches —low insertion loss, high isolation, fast switching speed, low power consumption, and robust power-handling— the inherent limitations of current technologies were underlined. In particular, the $R_{ON} \times C_{OFF}$ of RF-SOI switches, limited to about 50 ns, was identified as a critical barrier, motivating the exploration of alternative concepts.

Within this context, the specific advantages of PCM-based switches were outlined. Following a historical account of PCM development, the analysis addressed how material properties, device geometry, and heating strategies shape device performance. The contribution of each structural layer was detailed, together with the impact of voltage pulse shaping on switching dynamics. Finally, a comparison of heater materials further highlighted the contrast between tungsten, molybdenum, and NiCr alloys in terms of resistivity, thermal response, and robustness. From this review, the design choices retained in this work emerged clearly; a top-heater configuration combining GeTe as the PCM material with a tungsten heater, selected to balance efficient amorphization, high isolation, and limited parasitic effects while maintaining acceptable reliability. These considerations define the technological framework that supports the investigations carried out in this PhD.

The next chapter introduces the methodology adopted to pursue this study, covering the simulation strategies, measurement protocols, and experimental setups employed to characterize and optimize the behavior of PCM-based RF switches.

Chapter 2
Simulations and measurements methods

Chapter 2 presents a comprehensive study of the modeling and experimental characterization of PCM-based RF switches, forming the core methodology used to understand, predict, and improve their electrothermal and RF performance. The chapter follows a structured approach that combines numerical simulations and experimental validation in a continuous optimization loop.

Simulations, using multiple models adapted to different levels of abstraction and physical domains, enable the development of new designs aimed at enhancing component performance and reliability. These virtual studies guide the definition of key structural parameters, such as layers geometry and materials properties, and help predict critical behaviors including heating efficiency, quenching dynamics, and power consumption. Based on these results, new component generations are fabricated and experimentally characterized to extract quantitative data on switching dynamics, ON/OFF resistances, and RF performance. The outcomes of these measurements are then used to refine the simulation models, integrating real-world effects and imperfections observed during fabrication or cycling. This iterative workflow —alternating between simulation, fabrication, and characterization— forms a constant optimization loop that drives progressive performance improvement and deepens understanding of the underlying physical mechanisms.

The first part of the chapter focuses on the modeling strategy, detailing the progressive construction of the numerical models. Each level of modeling complexity allows for the evaluation of specific parameters, while ensuring physical consistency through calibrated material properties and boundary conditions.

The second part of the chapter presents the experimental characterization methods used to validate and complement the modeling results. Electrical and RF measurements protocols are presented to assess key performance indicators such as switching dynamics, insertion loss, and isolation, while power-handling measurements further extend this evaluation to high-power operating conditions. Together, these measurements provide a comprehensive view of the device's behavior under realistic operation.

Finally, the third part focuses on comparing simulation and measurement behaviors, identifying key discrepancies and their physical origins. This combined analysis bridges the gap between theoretical predictions and experimental observations, setting the stage for design optimization strategies.

Overall, this chapter establishes a unified methodological framework linking modeling, fabrication, and characterization. Through this integrated and iterative approach, it provides both theoretical insight and experimental validation essential to the advancement of PCM-based RF switch technology.

2.1 Finite element modeling

2.1.1 Starting point

This thesis builds upon previous work conducted by members of the research team supervising this PhD. In that study, two types of PCM-based RF switch models —previously introduced in Section 1.3.2— were converted into their thermally equivalent schematics, as shown in Figure 2-1. By applying several simplifying assumptions —treating air as a perfect insulator, considering the substrate

as an ideal thermostat, and neglecting lateral heat leakage— these schematics were further simplified into more analytically manageable forms.

In the Heater-on-Top configuration, the heat flux from the heater to the substrate crosses multiple intermediate layers, leading to significant thermal gradients at each interface that must be accurately represented in the model.

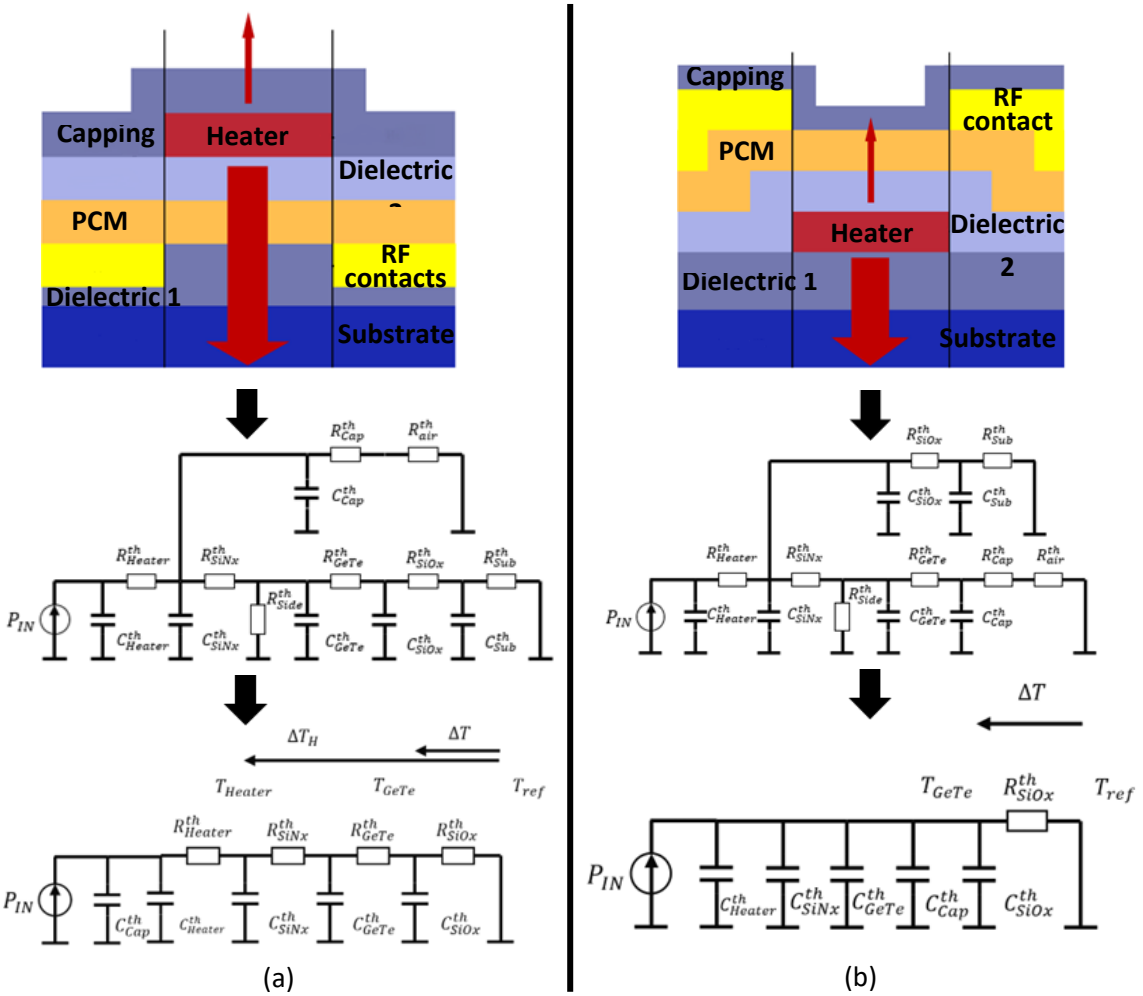


Figure 2-1: *(a) Heater-on-Top structure. (b) PCM-on-Top structure. The top panels illustrate the physical designs of the two configurations, the middle panels present their corresponding electrothermal representations, and the bottom panels show the simplified versions of these schematics.*

To capture these effects, electrothermal models were implemented in Matlab, and the power consumption, heating dynamics, and quenching behavior of both configurations were analyzed. The results confirmed the physical mechanisms described earlier and validated the differences between the two architectures highlighted in Section 1.3.2. This preliminary work concluded by emphasizing the importance of optimizing the layer dimensions to minimize power consumption, enhance PCM heating efficiency, and improve heat dissipation during the quenching phase —key factors for achieving better RF performance and power-handling capability.

While these electrothermal models provided valuable insights into the heating dynamics and power distribution of the switch, their simplified geometries and assumptions limit their ability to capture localized effects, such as temperature gradients across thin layers or the influence of 3D heat spreading. To accurately investigate these phenomena and refine the device design, a more detailed finite element representation is required.

2.1.2 Simplified 3D slice model - Slab

To address these limitations, a simplified 3D slice model —or slab— was developed using COMSOL Multiphysics® as illustrated in Figure 2-2. This model, representing a cross-section of the entire switch taken at the midpoint of its length, provides a controlled yet more realistic representation of the switch, with a 50 nm depth enabling the application of a voltage terminal on one side of the heater and a ground on the other —something not achievable in purely 2D simulations. Exploiting the model's symmetry, only one half is simulated, reducing computational effort.

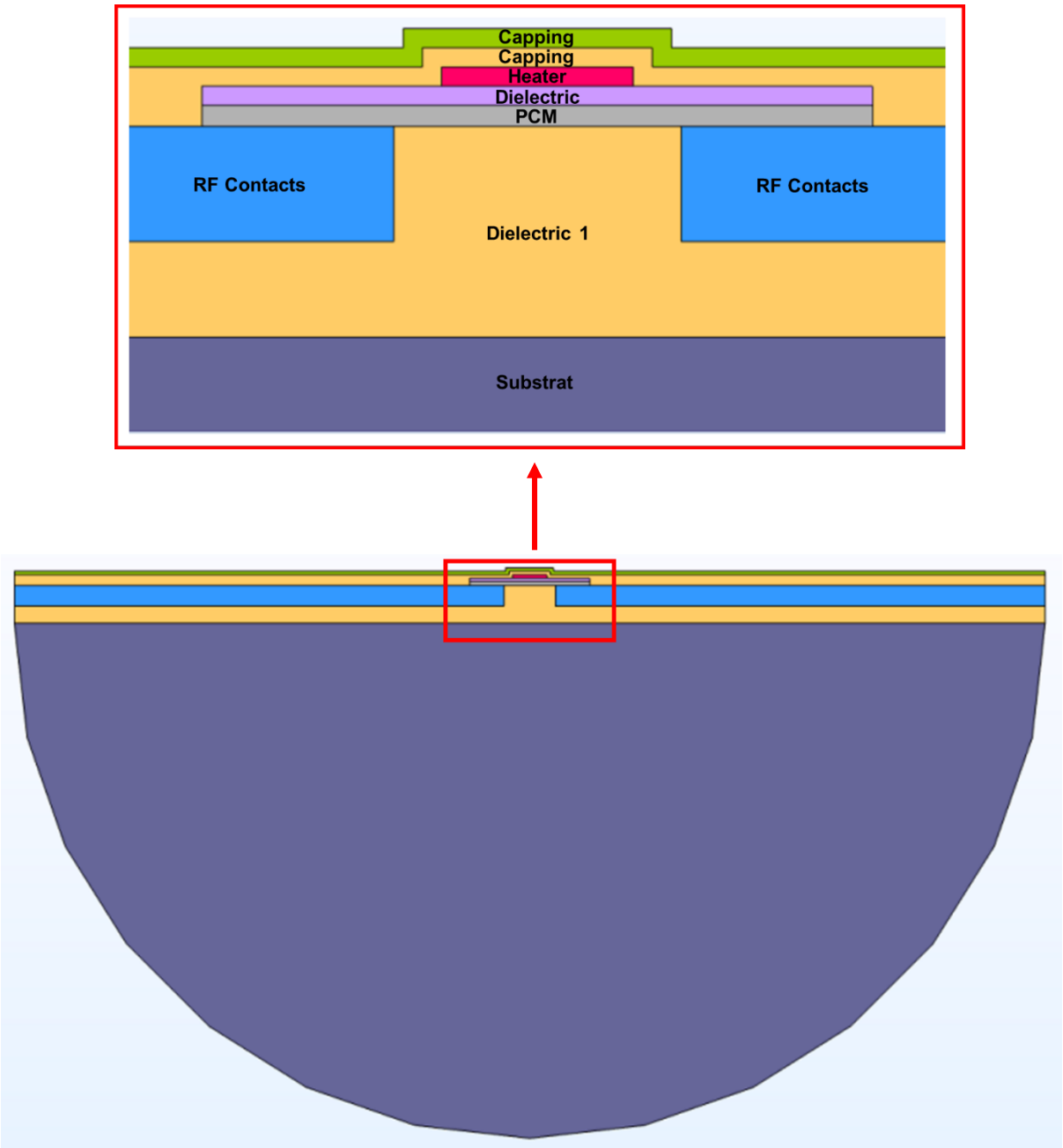


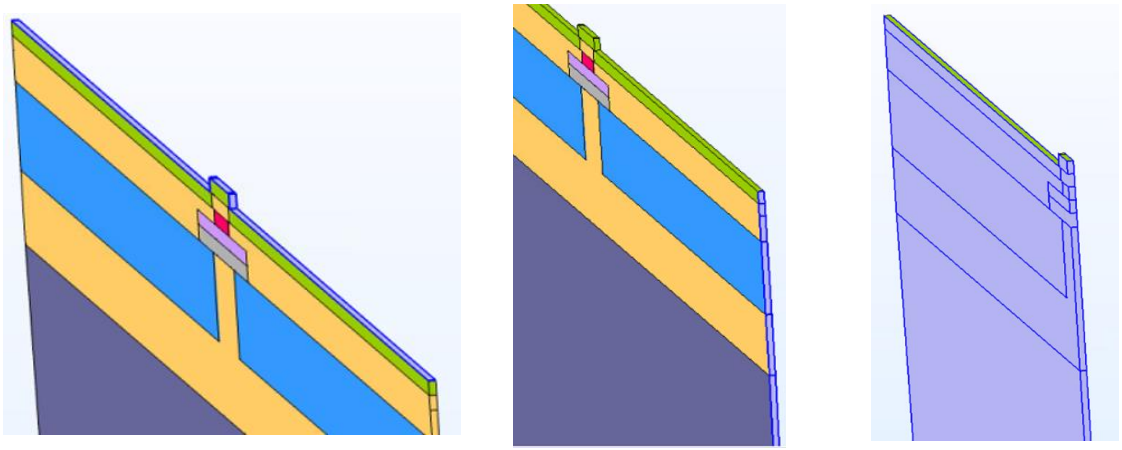
Figure 2-2: *Simplified 3D slice model.*

Regarding boundary conditions, a heat flux (Neumann condition) is first applied to the top surface of the switch (Figure 2-3.a). Its purpose is to define the rate of heat exchange between the switch and

the ambient air. This condition defines the rate of heat exchange between the switch and the ambient air, expressed by the equation:

$$Q = -k\left(\frac{dT}{dn}\right) \tag{2}$$

where Q is the heat flux [W.m^{-2}], $\left(\frac{dT}{dn}\right)$ the temperature gradient normal to the surface, and k the thermal conductivity of the top passivation layer. The negative sign indicates that heat flows from hotter to colder regions: a positive Q represents heat transfer from the ambient air to the switch, while a negative Q corresponds to heat leaving the switch toward the ambient.



(a) (b) (c)

Figure 2-3: *Heat transfer conditions applied in the model. The regions highlighted in blue indicate the locations of the respective boundary conditions; (a) convective heat transfert (Neumann condition), (b) fixed temperature (Dirichlet condition), and (c) symmetry condition applied to the plane dividing the model in half to account for the other half of the structure, as well as to the front and back faces to ensure periodicity.*

The second boundary condition is a fixed ambient temperature (Dirichlet condition) applied to the sides and bottom of the switch (Figure 2-3.b). As the ambient air itself is not modeled, the external faces are maintained at ambient temperature to simulate thermal contact with the surrounding environment. Care must be taken when applying this condition to avoid artificially constraining the internal thermal behavior of the switch.

The third boundary condition is a symmetry condition, applied to the front and back faces of the model as well as to the plane along which the model was halved (Figure 2-3.c). This ensures identical physical behavior across the 50 nm depth and effectively accounts for the missing half of the model without explicitly simulating it, thereby reducing computational resource requirements.

The substrate geometry is optimized in two ways. First, a cylindrical shape is adopted to reduce the number of mesh elements compared to a full rectangular block. Second, the substrate radius is adjusted to determine the minimum value beyond which the Dirichlet condition at its outer boundary no longer affects the thermal behavior of the switch. This is achieved by performing a parametric sweep on the substrate radius while monitoring the temperature at its outer edge. As shown in Figure 2-4, when the radius exceeds 15 µm, the substrate edge naturally stabilizes at ambient temperature, indicating that the Dirichlet condition no longer influences the thermal response of the switch.

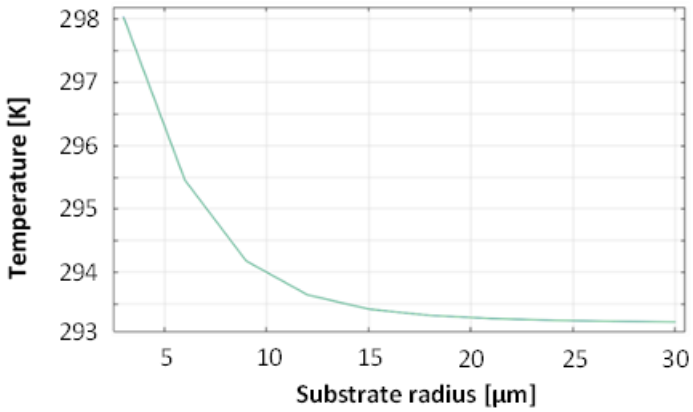


Figure 2-4: *Temperature at the substrate edge as a function of substrate radius.*

While the simplified slab model successfully capturs the essential thermal and electrical mechanisms of the switch, it remains limited in accurately representing edge effects, lateral heat spreading, and the influence of the complete geometry on power dissipation. These simplifications, though useful for preliminary understanding, could lead to deviations when compared with experimental data. To address these limitations and approach a configuration closer to the physical device, a complete three-dimensional model of the switch was developed.

2.1.3 Complete 3D model

Building upon the insights gained from the simplified 3D slab model, the next step involved constructing a full three-dimensional representation of the switch. This more comprehensive model incorporates all structural and material details —such as lateral extensions, contact geometries, and the complete stack of layers— to better reproduce the real device behavior and enable direct comparison with measurements. The resulting model, illustrated in Figure 2-5, is primarily designed to analyze the electrothermal behavior of the switch.

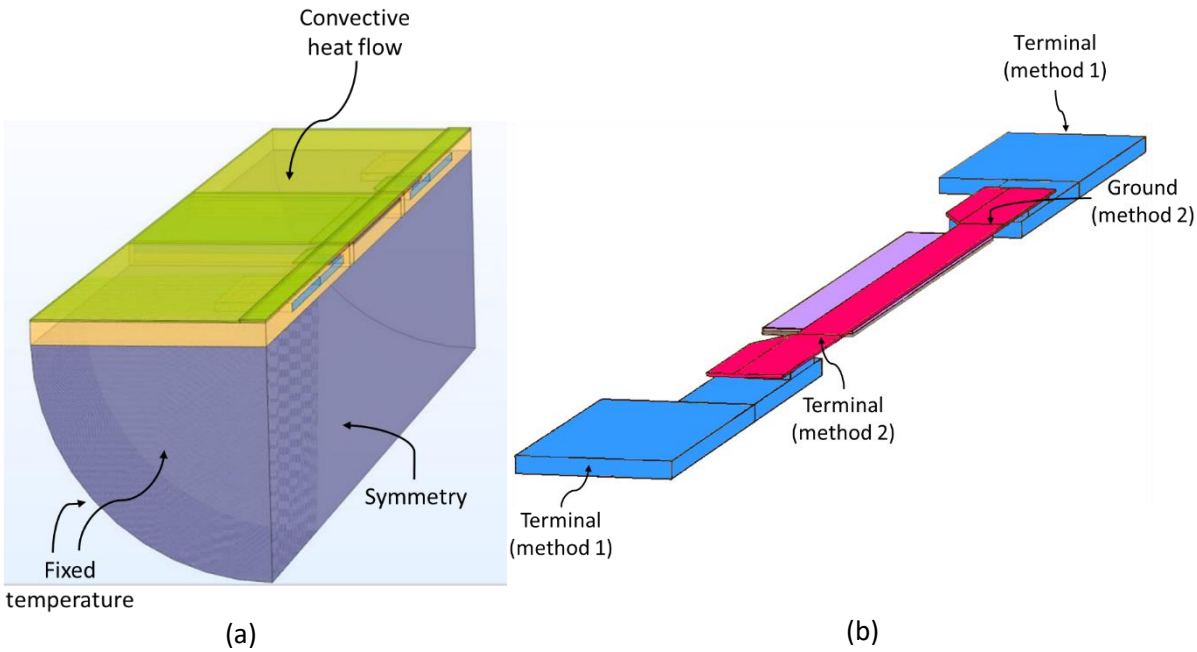


Figure 2-5: *(left) Half-view and (right) quarter-view of the 3D model representing the full length of the switch, with boundary conditions.*

At the beginning of the PhD, the voltage terminal and ground are positioned at the extremities of the contact pads (method 1 in Figure 2-5.b). They were later relocated to the edges of the heater to simplify the model and reduce electrical path complexity (method 2 in Figure 2-5.b). However, using a full 3D model introduces certain drawbacks. The most significant is the increased simulation time and the greater complexity of implementing design modifications, as each change —such as adding, removing, or adjusting a layer— requires careful adaptation of a larger number of elements, thereby increasing the number of geometrical parameters involved in the process.
With the full 3D model architecture defined and its electrothermal mechanisms implemented, the next step is to assign realistic material properties and boundary conditions to ensure physical accuracy. These parameters directly influence the simulated heating dynamics, power consumption, and thermal dissipation within the switch.

2.1.4 Physical parameters

2.1.4.1 Material properties

The physical parameters used in the simulations are selected based on experimental data, literature values, and in-house material characterizations. Particular attention is given to ensuring that the thermal and electrical properties of each layer accurately reflect the fabricated devices, thereby enabling meaningful comparison between simulated and measured results. The list of the thermal and electrical properties of the materials used for each layer is summarized in Table 2-1:

Table 2-1: *Thermal and electrical properties of materials used in simulations.*

Layer	Thermal conductivity [$W.m^{-1}.K^{-1}$]	Electrical resistivity [Ω.cm]	Specific heat [$J.Kg^{-1}.K^{-1}$]	Volumic mass [$kg.m^3$]
Si_3N_4	1.55	$2e^{14}$	700	3100
SiO_2	1.4	$2e^{14}$	730	2200
W	175	$3.08e^{-10}$ (at room temp)	132	17800
AlN	100	$1e^{9}$	740	3260
Cristalline GeTe	2.4 [103]	$8.7e^{-4}$	303	5770
Amorphous GeTe	0.29 [103]	6.67	303	5770
Cristalline GST	0.57 [103]	$8.7e^{-4}$	303	6140
Amorphous GST	0.19 [103]	6.67	303	6140
AlCu	238	$2.7e^{-6}$	900	2700
Si	130	$5e^{3}$	700	2329

Along with defining the material properties, another next step is to refine the physical parameters to maintain realistic operating conditions within the reduced 3D model.

2.1.4.2 Proportionnality of voltage

To achieve this, several adjustements are necessary. In particular, since the 3D model is reduced to a 50 nm slice, the voltage applied to the heater has to be scaled proportionally to the model's reduced dimensions to ensure consistent power density and thermal behavior.

2.1.4.3 Heater resistance

In addition to voltage scaling, the electrical resistance of the heater is carefully adjusted to match experimental measurements. This parameter directly influences the heat generation within the device and thus plays a key role in accurately reproducing the thermal response observed in real switches. The heater resistance, $R_{h(t)}$, varies with temperature, directly affecting the voltage across its

terminals. The heater temperature, $T_{h(t)}$, increases from the ambient temperature T_r to a final temperature T_f following an exponential temperature rise:

$$T_{h(t)} = T_r + \left(1 - e^{-\left(\frac{t}{\tau}\right)}\right) * \left(T_f - T_r\right) \quad (3)$$

Accordingly, the heater resistance, evolves over time as its temperature changes, following:

$$R_{h(t)} = R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (T_f - T_r))\right) \quad (4)$$

This temperature-dependent resistance influences the voltage across the heater, expressed as:

$$U_{h(t)} = 2 * U_c * \left(\frac{R_{h(t)}}{R_g + R_{h(t)}}\right) \quad (5)$$

With:

- $\boldsymbol{TCR}$**:** Thermal coefficient of resistance (1.35e^{-2} K^{-1} for tungsten)
- $\boldsymbol{U_{h(t)}}$**:** Voltage at the heater terminals as a function of time (t)
- $\boldsymbol{U_c}$**:** Command voltage applied by the user to the generator
- $\boldsymbol{R_{h(t)}}$**:** Heater resistance as a function of time (t)
- $\boldsymbol{R_{rT}}$**:** Initial heater resistance at room temperature
- $\boldsymbol{R_g}$**:** Internal resistance of the generator
- $\boldsymbol{T_{h(t)}}$**:** Heater temperature as a function of time (t)
- $\boldsymbol{T_f}$: Final temperature
- $\boldsymbol{T_r}$**:** Room temperature
- $\boldsymbol{\tau}$**:** Time constant representing the rate of temperature increase

It should be noted that in Equation (5) the generator voltage is multiplied by a factor of two. This reflects the behavior of real signal generators, which deliver twice the requested voltage to account for voltage division between the generator's internal 50 Ω resistance and the assumed 50 Ω load resistance.

During the initial phase of the PhD, this behavior was modeled using handwritten equations. However, these equations could only incorporate an average heater temperature at each time step, as it was not possible to account for the local temperature variations within the heater. To improve model accuracy, a virtual control circuit was later implemented in COMSOL Multiphysics®. This circuit includes a generator with a 50 Ω internal resistance (scaled proportionally for the simplified 3D slice model) connected between the heater terminal and ground, allowing direct control of the switch. Within this virtual circuit, the input voltage is manually doubled, since COMSOL does not automatically account for the generator's internal voltage division. The pulse waveform is also defined in this circuit. During simulations, the tungsten heater resistance evolves according to Equation (4). As a result, its resistance deviates from 50 Ω, leading to a dynamic voltage variation across the heater consistent with Equation (3). Additionally, a set of analytical equations is implemented in a "theoretical" module (separate from the virtual circuit) to predict the evolution of the heater's voltage and resistance as a function of a

user-defined temperature. This approach allows a direct comparison between theoretical predictions and simulated electrothermal behavior.

With the heater's electrical properties now consistent with the measured values, the model can reliably reproduce the heat generation mechanisms observed experimentally. This calibration establishes a solid foundation for assessing the device's overall electrothermal efficiency.

2.1.4.4 Calculating energy consumption

Building on this calibrated model, the next step involves quantifying the energy consumption during switching operations. This analysis provides direct insight into the power efficiency of the device and enables meaningful comparison between simulated and experimental results. The energy consumption can be evaluated using the following equations. The calculated energy corresponds to the power consumed by the heater to reach the melting temperature during the switching process:

$$I_{h(t)} = \frac{2 * U_c}{R_g + R_{h(t)}} \tag{6}$$

$$P_{h(t)} = {I^2}_{h(t)} * R_{h(t)} \tag{7}$$

$$E = \int_0^t P_{h(t)}.dt \tag{8}$$

With:

- $\boldsymbol{I_{h(t)}}$ Current through the heater as a function of time t
- $\boldsymbol{P_{h(t)}}$ **:** Heater power as a function of time t

By substituting Equation (7) into Equation (8), the energy can be expressed as:

$$E = \int_0^t {I^2}_{h(t)} * R_{h(t)}.dt \tag{9}$$

Then, substituting $I_{h(t)}$ from Equation (6):

$$E = \int_0^t \left(\frac{2 * U_c}{R_g + R_{h(t)}}\right)^2 * R_{h(t)}.dt \tag{10}$$

Finally, substituting $R_{h(t)}$ from Equation (4):

$$E = \int_0^t \left(\frac{2 * U_c}{R_g + R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (T_f - T_r)\right)}\right)^2 * R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (T_f - T_r)\right).dt \tag{11}$$

The parameters required to use these equations are determined either by the designer (U_c, R_g, T_r, t), from measurements (R_{rT}, TCR) or from simulation results (T_f, τ). The heater resistance at room temperature, R_{rT}, is calculated based on its geometrical dimensions and the material properties at T_r= 293.15 K:

$$R_{rT} = \rho_{rT} * \left(\frac{L_h}{W_h * t_h}\right) \quad (12)$$

where $\rho_{rT} = 30.77e^{-10}$ Ω.cm is the resistivity of tungsten at room temperature, and L_h, W_h and t_h are the heater length, width, and thickness, respectively. The time constant, τ, represents the time required for the heater to reach two-thirds of its total temperature rise during a pulse. It is obtained from reference temperature curves derived from simulations. As shown in Figure 2-6, which illustrates an example of the heater temperature rising over a 400 ns-wide pulse, the heater temperature increases from approximately 300 K to 1400 K during the pulse. This corresponds to a total temperature rise of 1100 K, and two-thirds of this rise —733 K— added to the initial temperature yields 1033 K. The heater reaches this temperature 137.5 ns after the start of the pulse, defining the characteristic time constant τ = 137.5 ns.

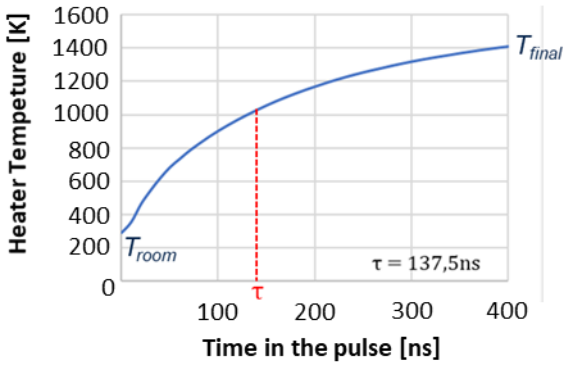


Figure 2-6: *Determination of the time constant τ, based on the heater temperature rise during a 400 ns-wide pulse.*

Additional simulations showed that τ varied by only a few nanoseconds. Replacing τ with other values within this range, or replacing the temperature reached in the heater with values between, for example, 1000 K and 3000 K in the energy formula, results in energy differences of only a few nanojoules. Given the minimal impact on the calculated energy, the temperature of 1400 K reached in the heater and its associated τ value were adopted for all subsequent energy calculations. This simplification significantly accelerates the estimation of energy consumption for both measurements and simulations, without compromising accuracy.

With all material parameters defined and the heater properly calibrated to reproduce realistic electrothermal behavior, the model now more accurately reflects the physical operation of the device during a switching pulse. However, to interpret its results meaningfully, it is essential to determine which portion of the phase-change material (PCM) actually undergoes transformation during operation.

2.1.5 Approximating the portion of the PCM affected by the phase change

The following section focuses on approximating the volume of PCM affected by the phase change. This step is crucial for correlating simulated temperature distributions with experimental switching behavior and for validating the model's predictive capability regarding the device's amorphization and crystallization dynamics. In practical applications, accurately determining the fraction of phase-change material (PCM) that becomes amorphous after a RESET pulse is challenging. Techniques such as Transmission Electron Microscopy (TEM) and electron diffraction are typically required to characterize the amorphized region within the PCM. Even with these methods, it is essential to consider the number of switching cycles, since the amorphized portion of the PCM evolves during the initial cycles before

reaching a stable configuration. This behavior is illustrated in Figure 2-7, which shows CEA switch samples observed at different cycling stages.

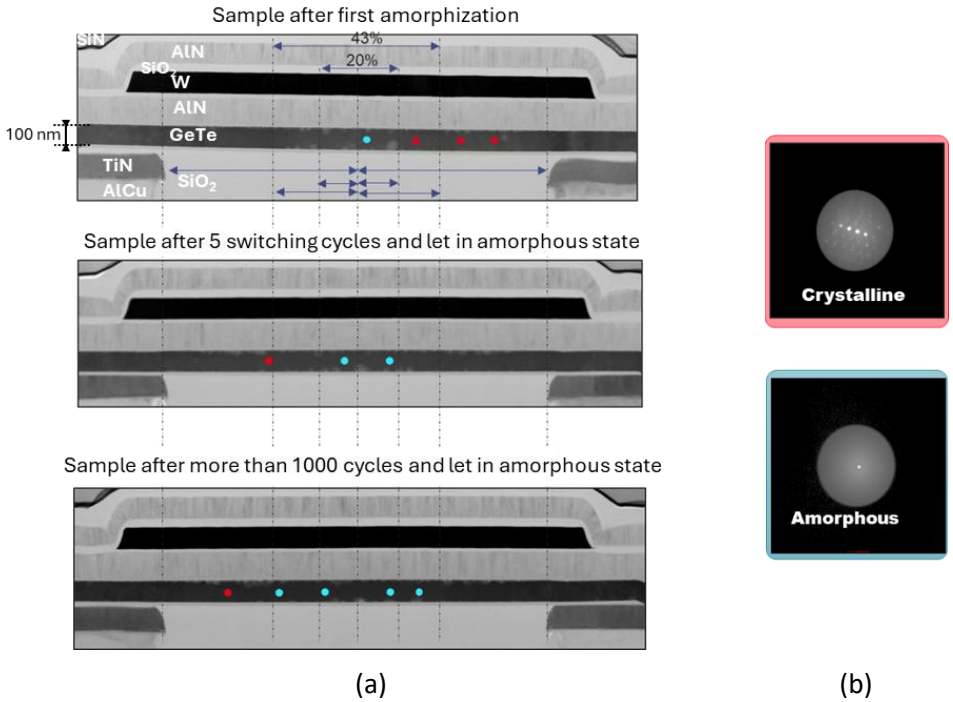


Figure 2-7: *(a) FIB–TEM cross-section showing the evolution of the amorphous region during cycling. The blue dots indicate amorphous PCM, while the red dots correspond to crystalline PCM. (b) Diffraction patterns collected from the regions marked in red and blue within the GeTe layer.*

In simulation, the objective is to ensure that the melting temperature is reached within a specific portion of the PCM. Although further details are provided in Section 3.1, it is important to define a realistic volume fraction of PCM expected to undergo phase change. In this work, the target is to melt approximately two-thirds of the PCM region located above the RF_{gap}. Consequently, in the simulations, the portion of PCM designated to reach the melting temperature is set to represent two-thirds of the total PCM volume, positioned at the center of the PCM layer, as illustrated in Figure 2-8.

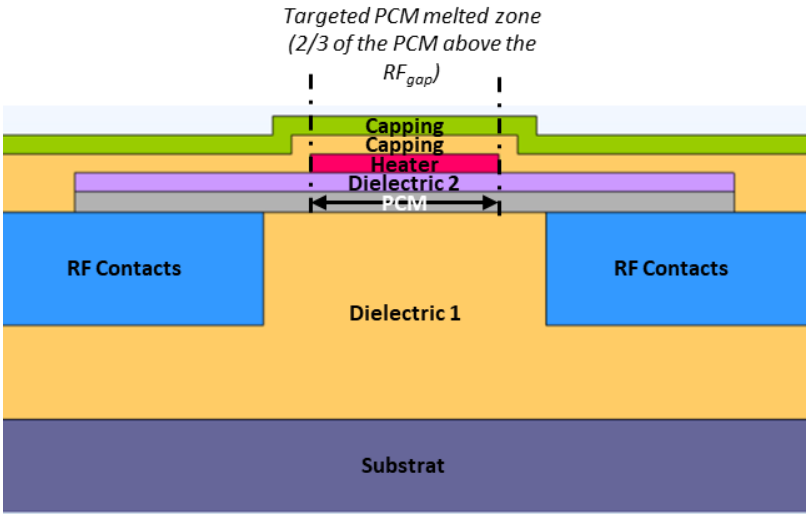


Figure 2-8: *Portion of the PCM expected to reach the melting temperature in each simulation.*

By defining a realistic portion of the PCM expected to undergo melting and re-solidification during a RESET pulse, the model establishes a consistent basis for evaluating thermal and structural behavior

under different electrical stimuli. This approximation enables a meaningful comparison between simulated and experimental results, ensuring that the modeled transformations correspond to physically observable switching events.

2.1.6 Simulation protocol

With the active PCM region identified, the next step involves establishing the simulation protocol to investigate its electrothermal behavior. This includes specifying the pulse characteristics and temperature monitoring methods employed to analyze the heating and quenching steps governing the phase-change process. Consistent with the previous section, each simulation is designed to melt approximately two-thirds of the PCM. To optimize the heater's energy consumption, a voltage sweep is applied, testing a range of pulse durations for each voltage level to determine the time required for the targeted portion of the PCM to reach its melting temperature. This approach enables a systematic comparison of the energy efficiency of different actuation pulse shapes that achieves the melting condition. Subsequently, the method was refined by maintaining a single pulse duration (except in studies focused on pulse-shape effects) while performing a voltage sweep. The optimal voltage is defined as the value at which two-thirds of the PCM reached the melting temperature. The next step focuses on estimating the portion of PCM that successfully undergoes amorphization. As previously mentioned, COMSOL Multiphysics® does not directly simulate phase-change behavior. Therefore, alternative temperature-based estimation methods were developed to assess the proportion of PCM undergoing amorphization, as illustrated in Figure 2-9. The first method involves monitoring the temperature evolution of the entire targeted PCM region. This allows observation of the cooling dynamics after heating, in particular:

- the minimum temperature (T_{min}) reached within the PCM at each time step
- the maximum temperature (T_{max}) at the same instants.

By defining a quenching time limit —the maximum time allowed for the PCM to cool below the crystallization temperature (T_{cryst}) before recrystallization occurs — it is possible to estimate, as shown in Figure 2-9.a:

- whether the PCM region is completed amorphized ($T_{max} < T_{cryst}$ after the quenching time limit),
- partially amorphized ($T_{min} < T_{cryst}$ but $T_{max} > T_{cryst}$), or
- not amorphized ($T_{min} > T_{cryst}$).

In the latter case, the difference between T_{min} and T_{cryst} at the end of the quenching period provides an indication of how close the PCM is to entering the amorphous state. However, this approach is limited by its coarse temporal resolution and by the fact that the points exhibiting T_{min} and T_{max} are not necessarily the same between two timesteps.

To overcome these limitations, a second method was implemented. Instead of evaluating the entire PCM region, the temperature is monitored along three horizontal lines —located at the bottom, middle, and top of the PCM layer— as shown in Figure 2-9.b for the bottom line. This is motivated by the observation that the top of the PCM, being closer to the heater, heats up more rapidly than the bottom. Conversely, the bottom region cools faster and is therefore more likely to retain an amorphous state. By tracking temperature evolution along these three lines over time, this approach provides more precise information on the vertical and lateral temperature distribution, and consequently, on the PCM's potential to amorphize within the selected quenching duration. Finally, a

third method is used to further clarify the analysis. Instead of line-based monitoring, temperature is recorded at specific key points within the PCM, as illustrated in the example shown in Figure 2-9.c. Since the top of the PCM typically reaches higher temperatures than the bottom, and the regions near the RF contacts cool more rapidly than the center, tracking these strategically selected points over time enables a localized and detailed understanding of the PCM's thermal and amorphization behavior.

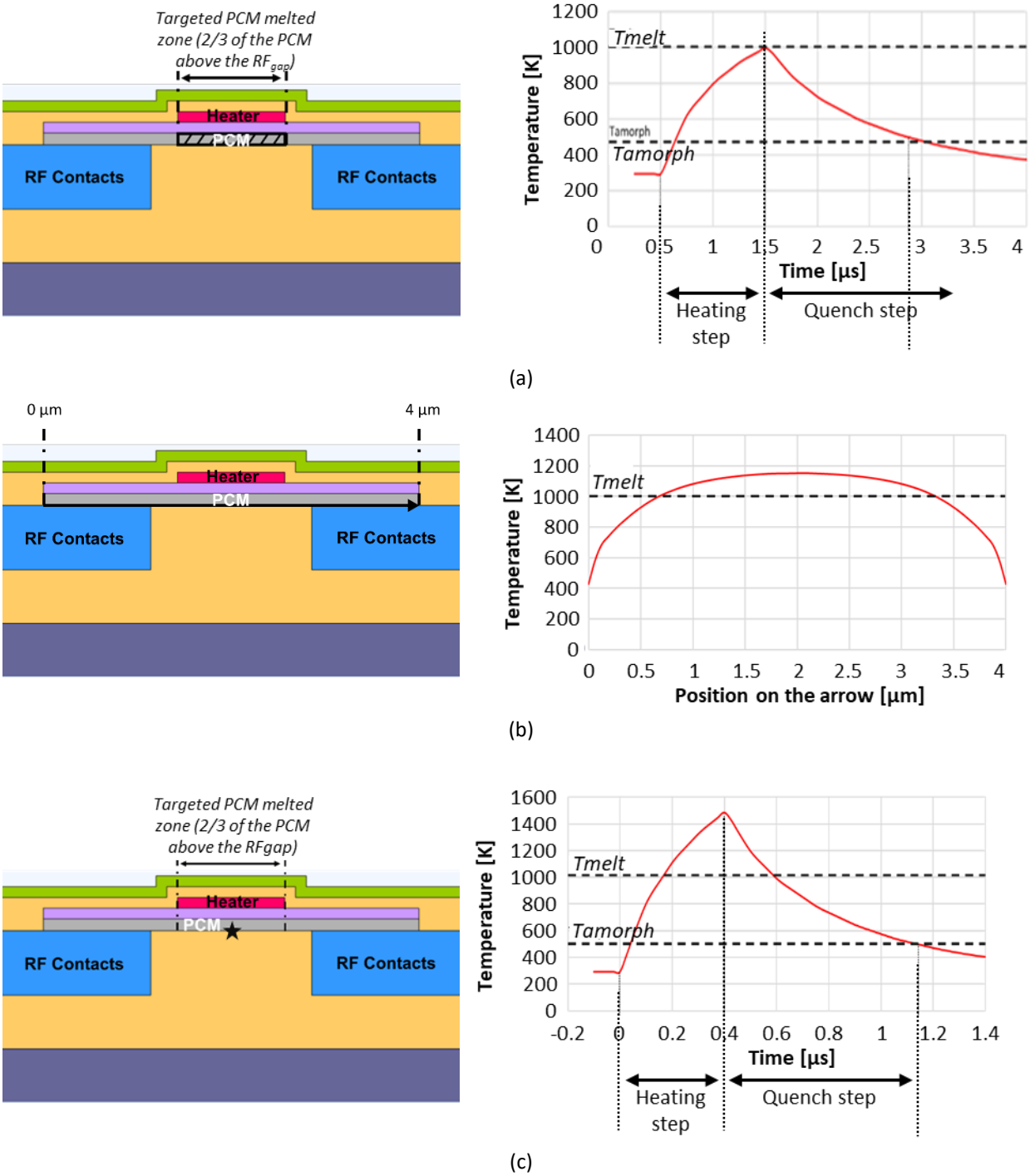


Figure 2-9: *Different methods for observing the temperature evolution within the PCM. (a) Monitoring of the minimum temperature in the PCM during a RESET pulse. (b) Temperature distribution along a line drawn at the bottom of the PCM, observed at the end of the heating phase, just before the onset of the quenching step. (c) Temperature evolution at a point located at the bottom of the PCM, at the midpoint of its length (defined by the dark star on the left-side schematic), during a RESET pulse.*

Through the stepwise development of the models —from thermally equivalent schematics to the full 3D structure with defined material properties and simulation protocols—, the electrothermal behavior of the PCM switch has been characterized numerically, providing a basis for comparison with real devices. To validate these results and probe the underlying physical phenomena, experimental characterization is necessary.

2.2 Characterization methods

The insights gained from these characterization methods complement the simulation results, providing a robust picture of the switch behavior. This combined knowledge enables the analysis of performance limitations, the impact of material and structural features, thereby guiding the design strategies and optimization approaches explored in the following sections.

2.2.1 Switching and switch resistance monitoring

The first type of electrical characterization performed in this work consistes of crystallizing and amorphizing the switches while simultaneously monitoring the resistances of both the heater and the RF path. The heater resistance serves as an indicator of the device's structural integrity. It is expected to remain relatively low —typically on the order of a few tens of ohms, depending on the heater length. If this resistance exhibits abnormal values (for instance, negative or exceeding 1000 Ω), it indicates a defective heater. In parallel, the resistance of the RF path provides information about the switching state: a low resistance (preferably below 20 Ω) corresponds to the ON-state, whereas a high resistance —typically about $10^4 \times R_{ON}$— corresponds to the OFF-state.

In the as-fabricated condition, the measured switches are initially conductive. The first step of the characterization process is therefore to amorphize them. This is achieved by applying a voltage sweep to the heater, initially ranging from 0 V to 10 V in 0.1 V increments. Based on preliminary results, this range was later optimized to start at 4 V in order to reduce the total measurement time and allow the characterization of a larger number of switches within a single session. Because switch performance typically evolves during the initial switching cycles, a "forming" procedure is employed during the first amorphization steps to obtain more representative results under realistic operating conditions. The forming process consists of applying a pulse train —i.e., a series of identical pulses— at each voltage step of the sweep. For example, ten consecutive pulses of 4 V are applied, followed by ten at 4.1 V, then ten at 4.2 V, and so on. An optimization of this forming protocol is presented in Section 3.6. Initially, a switch was considered amorphous when its resistance exceeded 1000 Ω. This criterion was later refined to align with the performance target of GeTe-based PCM switches, which is to achieve a resistance ratio on the order of 10^4 between the crystalline and amorphous states. Consequently, during measurements, the crystalline-state resistance (R_{ON}) is first determined, and the voltage sweep is continued until the measured resistance exceeded at least 10^4 x R_{ON}. Once the switch is successfully amorphized, RF performance and power-handling measurements are performed, or alternatively, a recrystallization (SET) step is attempted. Crystallization is achieved by applying another voltage sweep, starting from 0 V and using longer pulses. A switch is considered crystallized when its resistance falls below 100 Ω. Figure 2-10 shows the measurement setup used for these experiments. The setup consists of a printed circuit board (PCB) connected to four probes: two dedicated to the heater and two to the PCM. The PCB is interfaced with both a pulse generator and a parameter analyzer.

The pulse generator is used to apply voltage pulses to the heater, while the Voltage Source Unit 1 (VSU1) of the parameter analyzer is used to measure resistance by applying a small bias voltage of

20 mV, chosen to avoid influencing the behavior of the switch. VSU2 is used to control a relay that selects which resistance is being measured —either that of the heater or that of the PCM— according to the following configuration:

- A control voltage of 5 V enables the measurement of the heater resistance.
- A control voltage of 0 V enables the measurement of the PCM resistance.

The selection of the pulse amplitude and waveform applied by the pulse generator is managed through a dedicated Python script. An optimization study of the pulse duration is presented in Section 4.5.

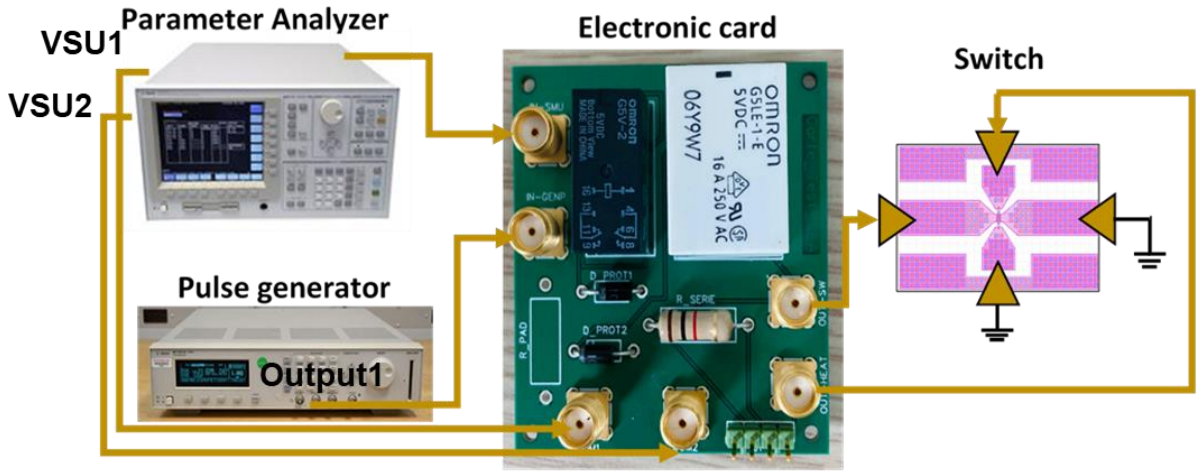


Figure 2-10: *Configuration of the switching measurement setup using CEA instrumentation. Monitoring the switching dynamics and resistance values provides critical insight into the electrothermal behavior of the PCM switches and establishes a baseline for device performance under controlled conditions. To complement this electrical characterization, it is also necessary to evaluate the switches' behavior in the RF domain.*

2.2.2 RF parameter extraction

RF parameter extraction reveals the frequency-dependent behavior of the switches, including characteristics such as insertion loss and isolation, complementing the electrical measurements and enabling a comprehensive assessment of device performance. As discussed in Section 1.1.2, two key metrics for evaluating switch performance are the ON-state resistance and the OFF-state capacitance at a given frequency. To determine these parameters, the S-parameters of the device must be extracted. These parameters describe the quality of signal transmission through a network. An example is illustrated in Figure 2-11, which presents a two-port network. Here, S11 represents the input return loss, S22 the output return loss, S12 the reverse gain, and S21 the forward gain.

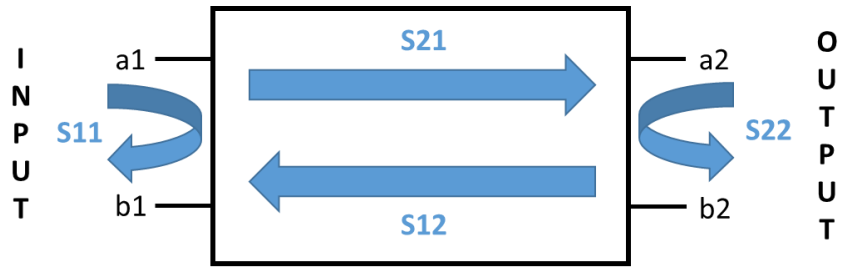


Figure 2-11: *Schematic of a two-port network illustrating the S-parameters: S11 (input return loss), S22 (output return loss), S12 (reverse gain), and S21 (forward gain).*

To obtain these S-parameters, the characterization setup shown in Figure 2-12 is used. It incorporates the elements detailed in the diagram of Figure 2-11. The measurements are performed on a semi-

automatic prober (PA300) equipped with a Vector Network Analyzer (VNA) —either an Anritsu 37369A (maximum frequency 40 GHz) or an Agilent N5230A (maximum frequency 20 GHz). The VNA delivers a −5 dBm (0.316 mW) signal to the Device Under Test (DUT) through Ground–Signal–Ground (GSG) RF Z probes (FormFactor) with a 150 µm pitch. Prior to measurement, a Short–Load–Open–Thru (SOLT) calibration is performed to eliminate distortions introduced by the test bench components (VNA, cables, probes, etc.). This calibration is carried out using a FormFactor CSR-8 calibration substrate, external to the wafer under test and provided by the manufacturer.

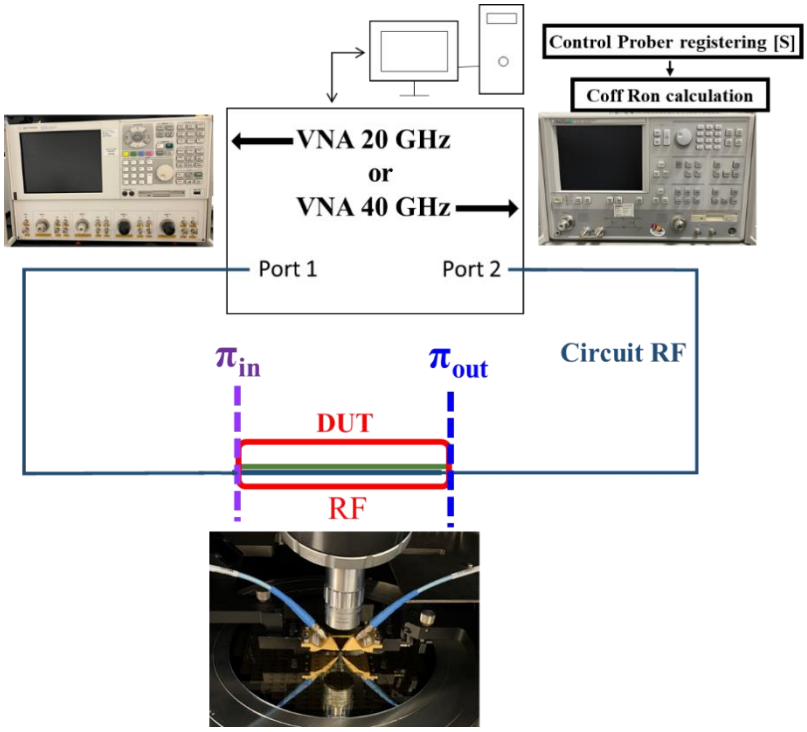


Figure 2-12: *Experimental setup for S-parameter measurement using CEA instrumentation, including a VNA, semi-automatic prober, and GSG RF probes.*

To perform the calibration, the Short, Open, Load and Thru standards are successively connected to each VNA port (port 1 and port 2 in Figure 2-12):

- Short: A short circuit first is applied, ideally reflecting the signal with a 180° phase shift. In practice, however, small parasitic inductances from the connectors and probes slightly alter this reflection. These effects are measured by the VNA and later compensated during calibration.

- Open: Next, an open circuit is connected. Ideally, it reflects the entire signal with no phase shift. In reality, parasitic capacitances exist between the open contacts, particularly at high frequencies (above 20 GHz). These capacitances are sensitive to probe positioning —if the probes are lifted slightly above the wafer, the capacitance decreases, which can even lead to negative correction values [104].

- Load: A 50 Ω load is then connected to absorb the signal completely, producing ideally no reflection. Real loads, however, introduce a small inductive component, which the VNA must also take into account during error correction

- Thru: Finally, a “Thru” connection is made to bridge both VNA ports. In theory, this allows the signal to pass through without loss or delay. In practice, a propagation delay occurs due to the finite length of the connection.

After all four standards are measured, the VNA uses these reference data to correct the system response. As a result, the extracted S-parameters represent only the behavior of the Device Under Test (DUT) between the two RF probes (π_{in} and π_{out} in Figure 2-12) excluding the effects of the measurement setup itself.

Once the S-parameters are extracted, they must be converted into R_{ON} and C_{OFF} values. To determine R_{ON}, a de-embedding step is required. In the ON-state, interconnections such as microstrips and contact pads introduce losses and phase shifts that must be removed. A reference “Thru” structure, in which the PCM is replaced by a metallic line, is therefore measured prior to the Device Under Test (DUT). The S21 parameter of the DUT is then measured, and the difference between the two allows isolating the intrinsic response of the switch. In practice, this means subtracting the S21 value of the Thru circuit from that of the DUT, resulting in an S21 that represents only the insertion loss of the switch itself, without fixture effects. The conversion from a linear value to decibels is expressed as:

$$S21_{dB} = 20log_{10}(|S21|) \tag{13}$$

The de-embedding can then be written as:

$$S21_{dB\_switch} = 20log_{10}(|S21_{DUT}|) - 20log_{10}(|S21_{Thru}|) \tag{14}$$

$$S21_{dB_{switch}} = 20log_{10}\left(\frac{|S21_{DUT}|}{|S21_{Thru}|}\right) \tag{15}$$

or, equivalently, in linear form:

$$|S21_{switch}| = 10^{\frac{S21_{dB\_switch}}{20}} = \frac{|S21_{DUT}|}{|S21_{Thru}|} \tag{16}$$

Considering the line reference impedance Z_0 and the ON-state resistance R_{ON}, $|S21_{switch}|$ can also be expressed as:

$$|S21_{switch}| = \frac{2 * Z_0}{(2 * Z_0) + R_{ON}} \tag{17}$$

Combining Equation (16) and Equation (17) gives the final formula to calculate R_{ON}:

$$\frac{|S21_{Thru}|}{|S21_{DUT}|} = \frac{(2 * Z_0) + R_{ON}}{2 * Z_0} \tag{18}$$

$$R_{ON} = 2 * Z_0 \left(\frac{|S21_{linear\_Thru}|}{|S21_{lienear\_DUT}|} - 1\right) \tag{19}$$

For more accurate high-frequency measurements, a Thru-Reflect-Line (TRL) de-embedding can be used to remove not only parasitic series resistances but also other unwanted effects. The C_{OFF} is determined directly from the measured S21 parameter, without de-embedding, using the following formula:

$$S21_{dB} = -10\, log_{10}\left(1 + \left(\frac{1}{(4\pi f C_{OFF} Z_0)^2}\right)\right) \tag{20}$$

which, after rearranging, gives:

$$10^{-\frac{S21_{dB}}{10}} = (1 + \left(\frac{1}{(4\pi f C_{OFF} Z_0)^2}\right)) \tag{21}$$

$$C_{OFF} = \frac{1}{4\pi f Z_0 \sqrt{10^{-\frac{S21_{dB}}{10}} - 1}} \tag{22}$$

Or, in linear form:

$$C_{OFF} = \frac{1}{4\pi f Z_0 \sqrt{\frac{1}{|S21|^2} - 1}} \tag{23}$$

Finally, probe movements along the wafer are automated using an internal CEA program that controls motion along the X, Y, and Z axes according to a predefined device map. The program automatically positions the probes on each DUT, initiates the measurement, records the results, and proceeds to the next device.

While RF parameter extraction characterizes frequency-dependent behavior such as insertion loss and isolation, it does not provide information on the switches' response under high-power conditions. Understanding how the device handles elevated RF power is therefore necessary to complete the performance assessment.

2.2.3 Power-handling measurements

To investigate power-handling capabilities, measurements are performed to determine the maximum RF power the switches can sustain without degradation or failure. These experiments complement the electrical and RF characterizations by revealing potential limitations under practical operating conditions. The power-handling measurements in both the ON and OFF states are carried out using the setup illustrated in Figure 2-13.

An RF source first generates a 915 MHz sinusoidal signal, which is then amplified by a power amplifier to deliver sufficient power to stress or even break the DUT during testing. To protect the amplifier, an attenuator limits the input power to a maximum of 10 dBm. The amplified signal is subsequently filtered through a bandpass filter, which isolates the fundamental frequency component and suppresses higher-order harmonics. A circulator then directs the filtered signal toward the DUT. The portion of the signal reflected by the DUT is redirected by the circulator to an attenuator, followed by a 50 Ω load, ensuring protection of the power amplifier from back reflections. Additional attenuators are inserted before and after the DUT to safeguard other components of the setup from multiple reflections, while also limiting the signal power received by the spectrum analyzer to a maximum of 30 dBm. The DUT is powered using two T-bias circuits placed on either side of the device. The first combines the DC bias with the RF signal at the DUT input, while the second separates the DC component at the output, allowing only the RF signal to be analyzed. A notch filter is positioned upstream of the spectrum analyzer to attenuate the signal level when necessary. This prevents the analyzer from generating its own harmonics, thereby ensuring that the harmonics observed correspond solely to those produced by the DUT.

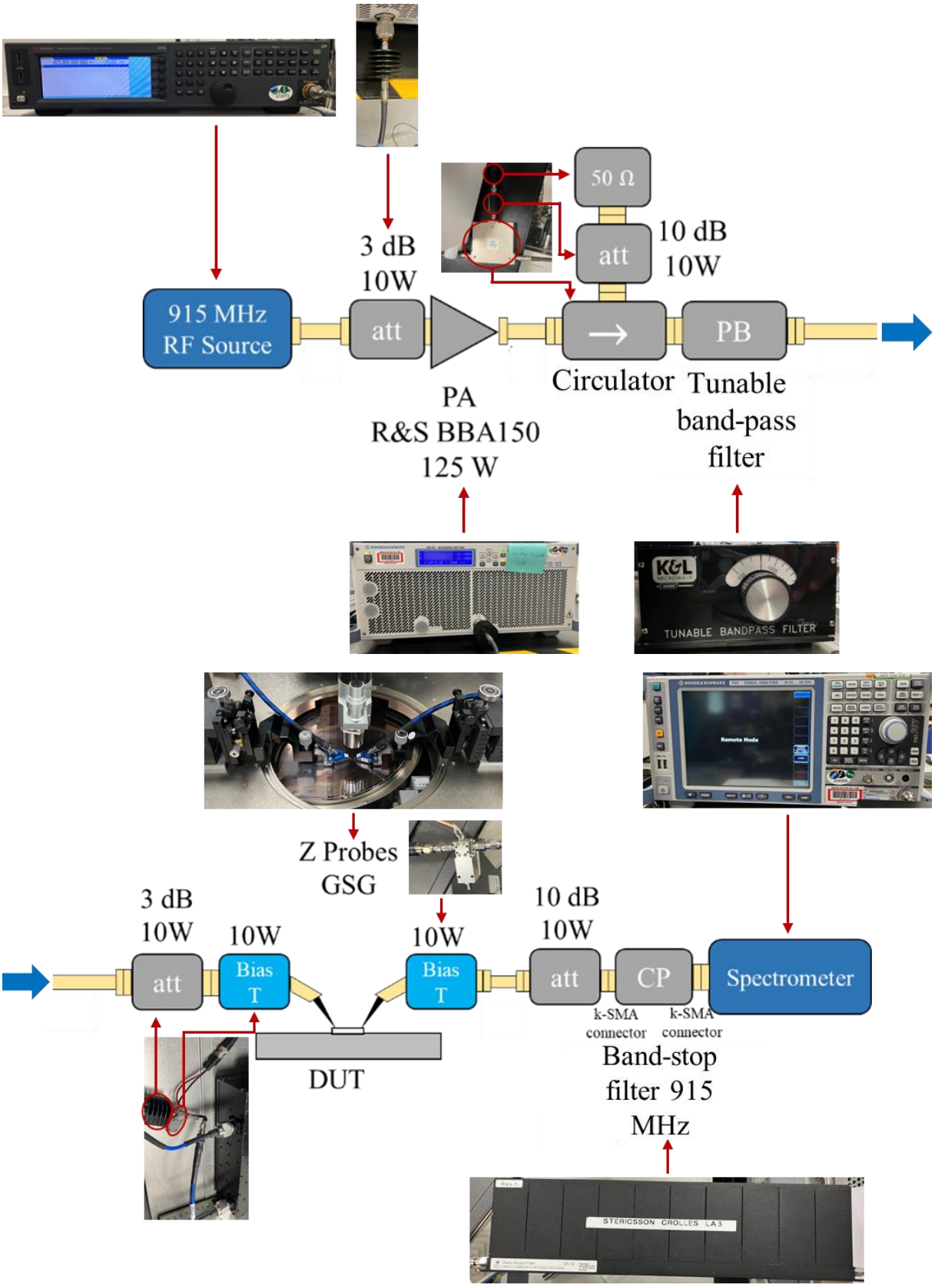


Figure 2-13: *Power-handling measurement setup comprising instruments from CEA, with some equipment provided by STMicroelectronics).*

During the measurement, a power sweep is applied to the DUT input, with each step lasting five seconds. The output power is monitored, and the fundamental, second, and third harmonics are recorded. Representative results are shown in Figure 2-14.

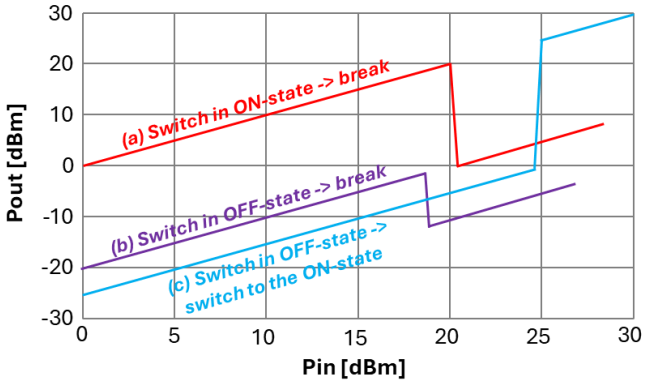


Figure 2-14: *Typical behaviors observed during for RF switch power-handling measurements.*

- Curve (a) corresponds to a switch in the ON-state, characterized by an output power equal to the input power at the beginning of the sweep. A sharp drop in output power is observed at a certain point, indicating a sudden increase in switch resistance and subsequent device breakdown.
- Curve (b) illustrates the OFF-state behavior, where the output power is initially lower than the input due to the high resistivity of the PCM. A sudden decrease in the output signal also marks the breakdown of the component.
- Curve (c) represents an OFF-state switch undergoing partial crystallization during the power sweep. In this case, the output power gradually increases until it reaches the input level, reflecting a transition toward the conductive state.

The combination of electrical switching, RF parameter extraction, and power-handling measurements provides a comprehensive experimental characterization of the PCM switches. These results establish a benchmark against which the accuracy and predictive capability of the simulations can be assessed.

2.3 Analysis of the comparison between simulation and measurement results

Building on the experimental data, the next step involves a detailed comparison between simulation predictions and measured device behavior. This analysis highlights important discrepancies, offering insight into the validity of the models and the physical phenomena influencing switch performance.

2.3.1 Thermal boundaries Resistances (TBR)

When heat propagates through a multilayer structure, additional thermal resistances arise at the interfaces between different materials. These thermal boundary resistances (TBRs) originate from several physical phenomena, including acoustic mismatch between materials —leading to phonon scattering— as well as surface roughness, which reduces the effective contact area between layers. Even in the case of perfectly flat and defect-free interfaces, a finite TBR remains. It can be defined by the following relation between the heat flux density Q and the temperature difference ΔT across the interface:

$$R_{th} = \frac{\Delta T}{Q} \tag{24}$$

As layer dimensions shrink, these interface resistances play an increasingly significant role in the overall thermal conductance, thereby limiting heat dissipation. At the beginning of this work, the impact of TBRs on the thermal behavior of the switch was investigated. Values of the different interfaces present in the design are collected from the literature and are summarized in Table 2-2. The black boxes correspond to material combinations that are not in direct contact within the switch structure.

Table 2-2: *TBR reported in the literature for the various interfaces between the switch layers.*

TBR Values	Capping (SiO_2)	Diel 2 (SiN)	PCM (GST)	RF contacts (Al)	Diel1 (SiO_2)	Substrate (Si)
Capping (SiO_2)		0.22 m^2·K/GW **[105]**				
Diel 2 (SiN)	0.22 m^2·K/GW **[105]**		15 m^2·K/GW **[106]**			
PCM (GST)		15 m^2·K/GW **[106]**		100-500 m^2·K/GW **[107]**	40 m^2·K/GW **[106]** + **[108]**	
RF contacts (Al)			100-500 m^2·K/GW **[107]**		6.29 m^2·K/GW **[109]**	
Diel1 (SiO_2)			40 m^2·K/GW **[106]** + **[108]**	6.29 m^2·K/GW **[109]**		0.4-3.5 m^2·K/GW **[110]**
Substrate (Si)					0.4-3.5 m^2·K/GW **[110]**	

From these data, several trends can be observed. Between low thermal conductivity dielectrics (e.g., SiO_2/Si_3N_4), the TBR is almost negligible, which is consistent with the weak heat flux and minimal temperature difference across such interfaces. In contrast, higher TBR values appear at the junctions between low-conductivity dielectrics and highly conductive layers, such as the interfaces between dielectric 1 and the RF contacts or between dielectric 1 and the substrate, both being excellent thermal conductors. The highest TBR is observed between the PCM and the RF contacts, resulting from the intense heat fluxes in this region, where a large amount of heat accumulated in the PCM during heating is rapidly drained through the contacts. The PCM/dielectric 1 interface also exhibits a notable TBR, since part of the heat stored in the PCM dissipates toward the substrate.

These values are then implemented in the finite element model to evaluate their influence on the switch's thermal behavior. The temperature continuity across interfaces is analyzed along a vertical line intersecting the different material boundaries in the 3D slice model, observed at the end of the heating phase of a pulse. Figure 2-15.a illustrates the temperature evolution across three specific interfaces:

- between the substrate and dielectric 1 (SiO_2) in Figure 2-15.a,
- between this dielectric and the PCM in Figure 2-15.b,
- between the PCM and the dielectric 2 (Si_3N_4) in Figure 2-15.c.

In each case, during the simulation, only the TBR of the interface analyzed is activated (green lines in the graphs of the right), and the evolution of the temperature along the observation line is compared with a simulation without the TBR activated (blue lines in the graphs). For the Si/SiO_2 interface (Figure 2-15.a), the temperature profiles obtained with and without the TBR applied are almost identical. This result is consistent with the very low TBR expected at this interface, as the temperature gradient across

Si and SiO_2 remains minimal. In contrast, Figure 2-15.b reveals a noticeable difference when the TBR is applied: the temperature in the PCM increases, while it decreases in the dielectric 1 layer.

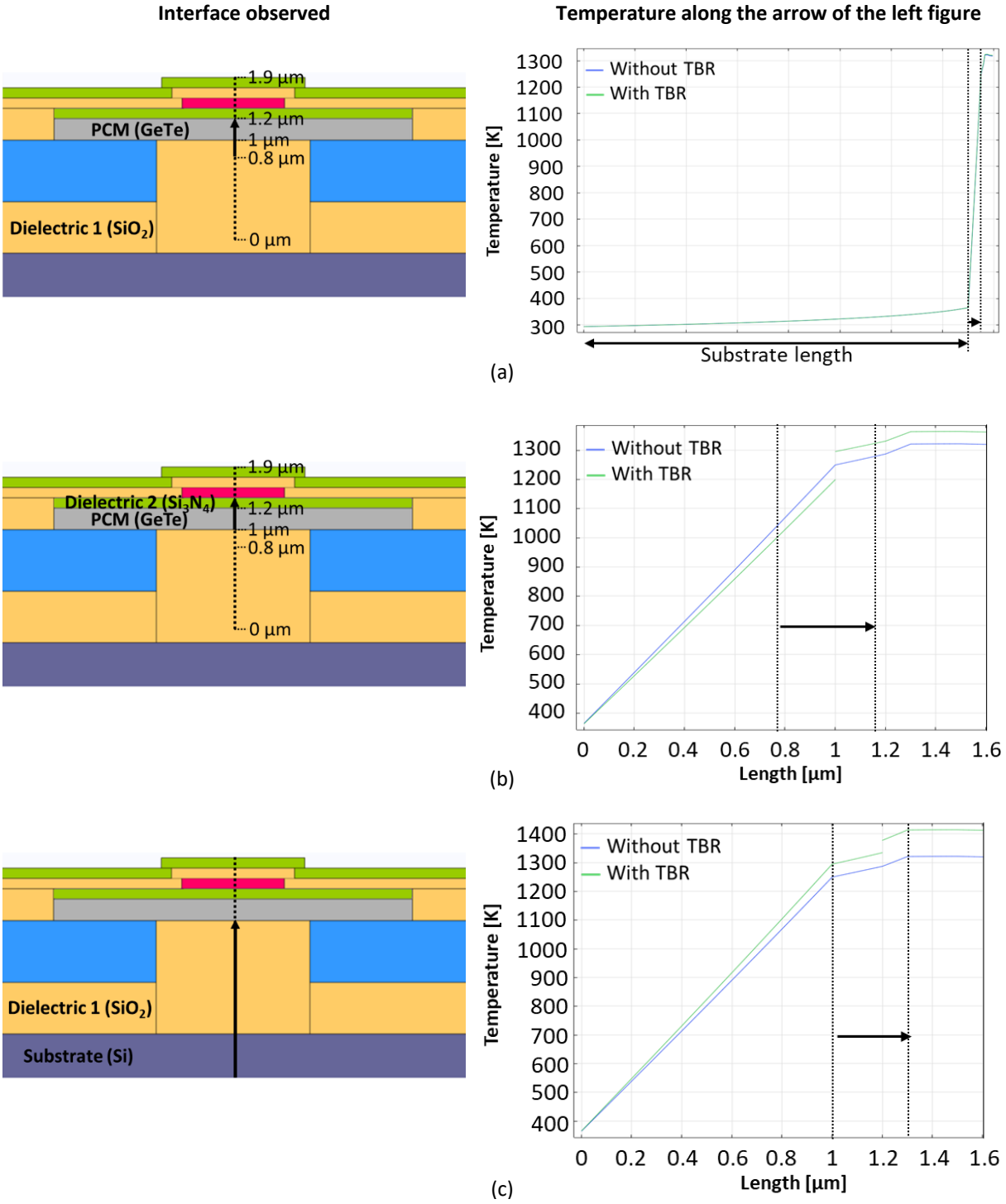


Figure 2-15: *Temperature evolution across the layers with TBRs applied at different interfaces, compared to a model without TBRs.*

The higher temperature in the PCM results from the reduced ability of heat to cross the interface due to the additional thermal resistance. Below the interface, the lower temperature arises because, as heat transfer across the interface becomes more limited, a portion of the heat is redirected and drained through the RF contacts instead. Consequently, less heat flows into dielectric 1, lowering its temperature. Finally, Figure 2-15.c, which concerns the interface between the PCM and the dielectric

above it, shows a temperature increase in both layers when the TBR is applied. As before, the higher temperature above the interface results from partial heat retention at the boundary. However, in this case, the temperature below the interface also rises, since no efficient heat dissipation paths exist in the upper dielectric 2 layer. As a result, the heat accumulated above the interface eventually crosses it entirely, leading to higher temperatures in the PCM compared to the simulation without TBR.To further assess the influence of the RF contacts on the temperature of dielectric 1 (seen in Figure 2-15.b), a 1D model was developed. This model represents the vertical stack of layers encountered along a line drawn through the center of the switch, from top to bottom, without including the RF contacts. As for the 3D slice model, the temperature evolution is observed at the end of the heating phase of a pulse, as illustrated in Figure 2-16.

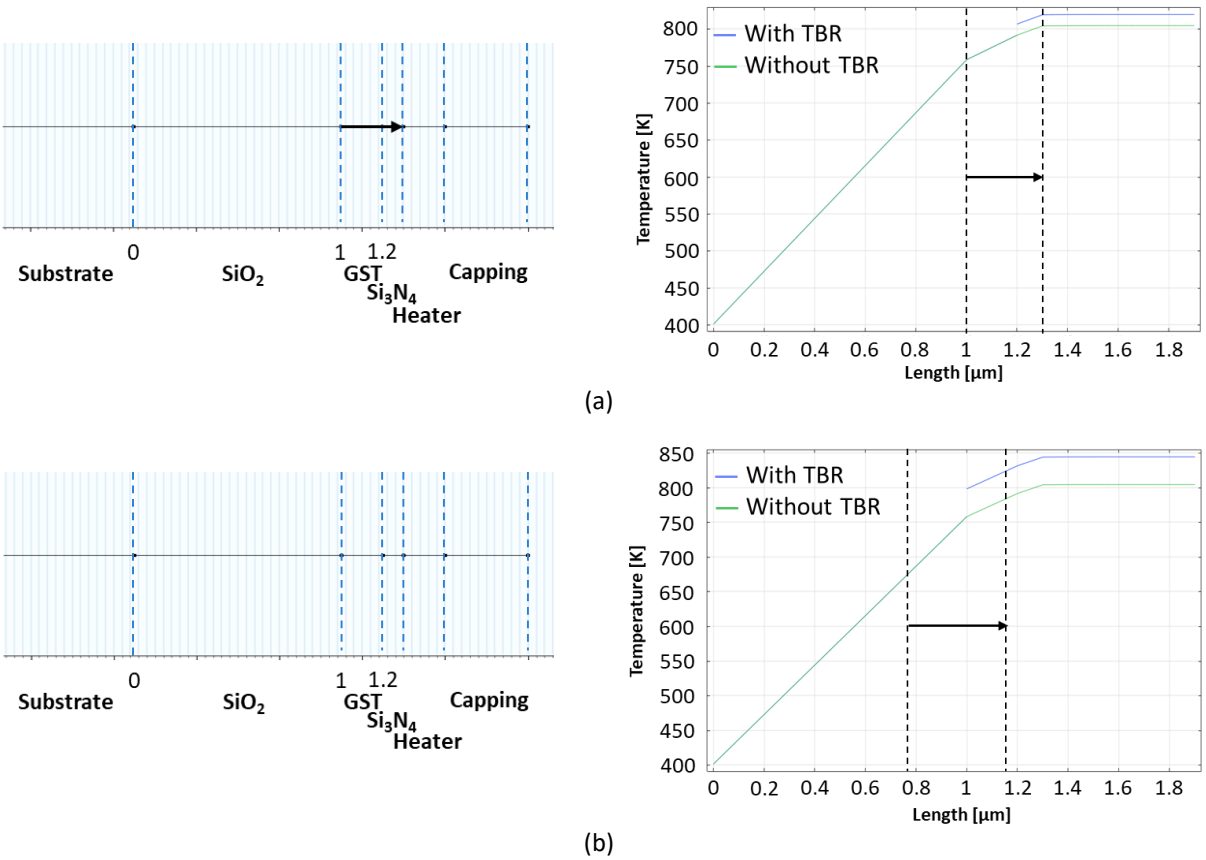


Figure 2-16: *Temperature evolution across the layers of a 1D model with TBRs applied at different interfaces, compared to a model without TBRs.*

In this case, no significant temperature difference is observed below the interface when comparing simulations with and without the TBR applied. Heat accumulation only appears above the interfaces. A useful way to assess whether the TBR between two materials is relevant for device design is to calculate the Kapitza length. This parameter represents the equivalent thickness of one of the two materials that would produce the same thermal resistance effect as the TBR itself. The Kapitza length can be determined using two approaches. The first method calculates it directly from the thermal boundary resistance R_{th} and the thermal conductivity λ of the material, following the relation:

$$L = \lambda R_{th} \tag{25}$$

where L as the Kapitza length. The second approach, illustrated in Figure 2-17, relies on analyzing the simulated temperature profiles. As shown in Figure 2-17.b, the temperature curve below the interface is extrapolated to meet the curve obtained above the interface when the TBR is applied. The upper

portion of the curve is then shifted to form a continuous profile. The horizontal displacement between the two curves corresponds to the thickness of the lower layer that would reproduce the TBR effect. For example, in Figure 2-17.c, an additional 100 nm of PCM would be required to emulate the TBR between the PCM and the dielectric above it in the simulated model. If the resulting Kapitza length is comparable to the dimensions of the device layers, its influence on heat transfer must not be neglected.

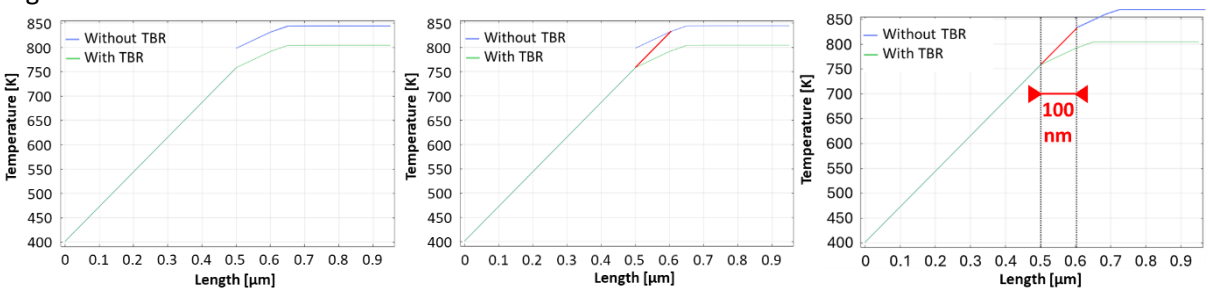


Figure 2-17: *Determination of the equivalent material thickness corresponding to the TBR at its adjacent interface.*

Though the analysis of the thermal behavior through the TBR evaluation provides key insights into the heat transport within the switch, understanding the thermal response alone is not sufficient. Material integrity and structural quality also play a crucial role in device performance and reliability.

2.3.2 Materials integrity

Consequently, the next step focuses on assessing the physical integrity of the switch materials. This includes examining defects, voids, and surface roughness that could impact both the electrothermal behavior and long-term reliability of the PCM switches. In simulations, each layer is assumed to have perfectly defined dimensions and uniform properties that remain unchanged throughout cycling. In practice, however, materials properties can be altered during fabrication and repeated device operation. Real device layers are not as ideally formed and their characteristics evolve with use. Cycling measurements are therefore required to quantify performance variations over time The devices investigated in this work were examined through several FIB-SEM cross-sectional images. An example is presented in Figure 2-18, comparing two deposition methods for the TiN/W heater: chemical vapor deposition (CVD) and physical vapor deposition (PVD). The CVD technique, which enables multidirectional deposition, provides significantly better conformity across the full heater thickness compared to PVD.

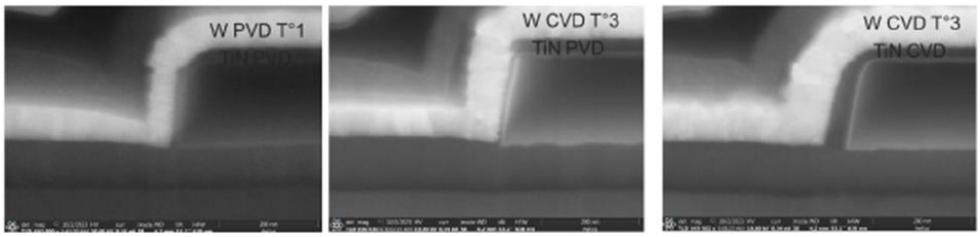
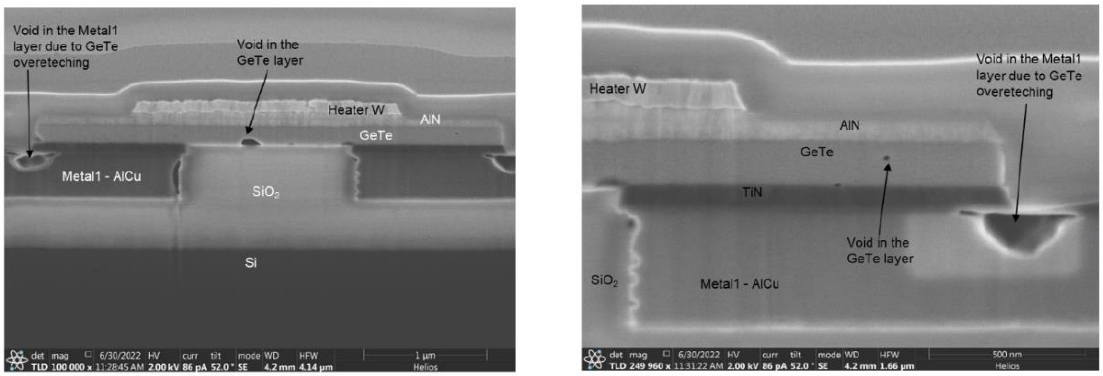


Figure 2-18: *FIB-SEM cross-sections of devices fabricated at CEA, comparing different metal heater variants.*

Another example is shown in Figure 2-19, where the observed layers deviate from the ideal flatness assumed in simulations. Some regions even exhibit process-induced damage, such as in the metal layer on the right-hand side of the image. Such imperfections can locally alter parameters like thermal boundary resistances (TBRs), which are partially dependent on surface roughness.



(a) (b)

Figure 2-19 : *(a) Overview and (b) enlarged FIB cross-section of a CEA-fabricated switch, showing surface roughness imperfections and void formation.*

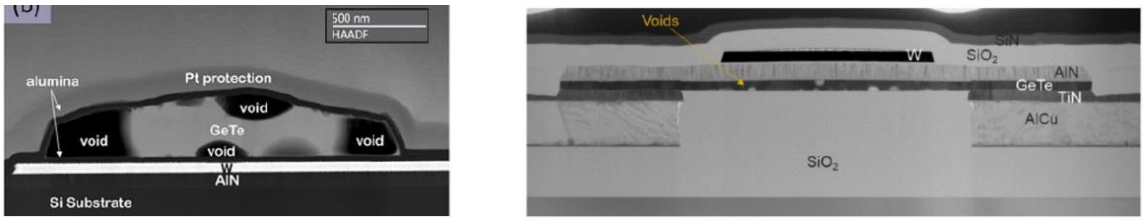
A particularly important observation concerns the modification of the internal composition of phase-change materials (PCMs) after cycling. These changes, visible across various PCM types, can arise from several mechanisms. One of them is elemental segregation, a process that may occur in directly heated PCMs through electromigration [112]. When the PCM is molten, electrostatic forces cause Ge and Sb atoms to become cations and migrate toward the cathode, while Te atoms, acting as anions, drift toward the anode. In the crystalline state, the opposite occurs: the flow of conductive charges drives Ge and Sb atoms toward the anode and Te atoms toward the cathode. Temperature increases can also promote atomic segregation [113]. The redistribution of atoms leads to void formation within the PCM, increasing porosity and reducing material reliability over time. This effect is more pronounced in Ge-rich PCMs, creating a design trade-off in memory applications: while a higher Ge content raises the crystallization temperature and improves data retention, it also enhances segregation and void formation.

The internal morphology of PCMs can also evolve through the dewetting effect, which results in the formation of voids at the interfaces between the PCM and adjacent layers. These voids reduce the effective contact area at the interfaces, thereby degrading energy transfer. Initially forming within the PCM during the first switching cycles, they tend to grow, merge, and migrate toward the material boundaries. When voids become sufficiently large, they can dominate the PCM's behavior. For instance, in the GeTe layer studied in [114], void growth and agglomeration at material boundaries — illustrated in Figure 2-20.a— significantly reduced the conduction path, leading to an increase in the amorphous-state resistance. The same study also reported that dewetting forces intensified PCM deformation during cycling, eventually causing rupture of the encapsulation layers and failure of the switches.

Additional mechanisms can also induce void formation, such as outgassing from SiO_2 layers. As described in [115], this phenomenon occurs during heating when gaseous species trapped in the SiO_2 accumulate at the interfaces with adjacent layers. Under pressure, these species can diffuse into the neighboring germanium materials. The effect becomes more pronounced at higher temperatures or under rapid heating. This outgassing behavior has been observed in TEM cross-sections of switches fabricated at CEA, as shown in Figure 2-20.b. Mitigation strategies include the introduction of a protective barrier between SiO_2 and the PCM or pre-degassing of SiO_2 layers prior to PCM deposition [115].

These material alterations —arising from fabrication imperfections and cumulative stress during cycling— are not represented in the simulation models developed in this work. Consequently, they

constitute a significant source of deviation between simulated predictions and the actual performance of the fabricated devices.



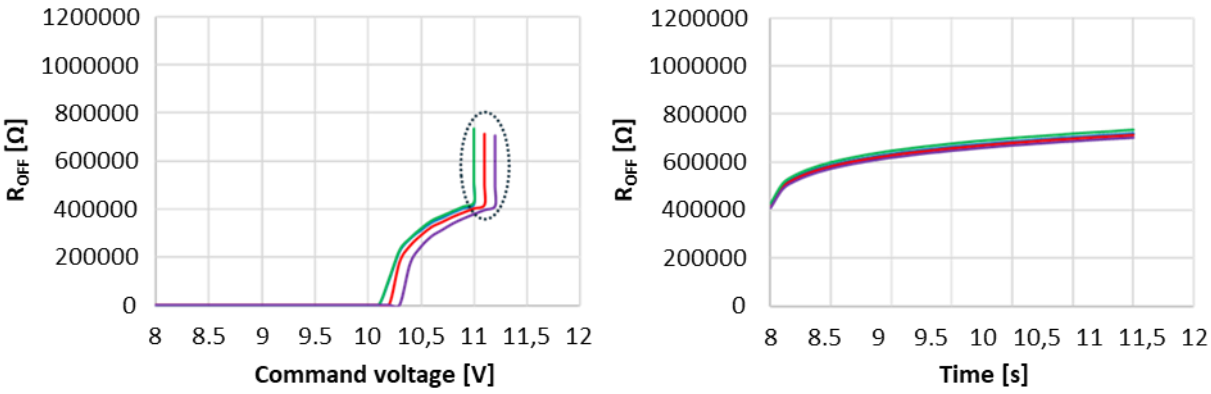
(a) (b)

Figure 2-20 : *(a) PCM layer exhibiting voids induced by the dewetting effect [114]. (b) CEA-fabricated switch showing PCM voids resulting from SiO_2 outgassing.*

While ensuring the structural quality of the PCM layers is crucial for accurate modeling, real devices may still exhibit time-dependent changes that cannot be captured by static material assessments alone. Understanding these dynamic effects is necessary to fully characterize switch behavior.

2.3.3 OFF-state resistance drift

One notable behavior of the switches is the drift of their OFF-state resistances over time. This phenomenon reflects gradual changes in the material's structural and thermal state, impacting device performance even under otherwise unchanged operating conditions. Once switched to the OFF state, a device exhibits a certain resistance value. For example, if the same switch is reused a week later for a crystallization attempt, its initial resistance is higher than in the previous measurement. This drift begins immediately after the amorphization step. Figure 2-21 illustrates this phenomenon for switches of the same design from different chips. Figure 2-21.a shows the resistance evolution during the voltage sweep applied by the generator.



(a) (b)

Figure 2-21: *(a) Evolution of the resistance of switches vs a sweep of voltages applied using amorphization pulses. For each case, the voltage sweep stopped once the switch reached 400 MΩ. The circle part of the curves represents an observation of the resistances during five minutes after the voltage sweep ended. (b) Different representation of the parts of the resistance curves circled in (a), this time showing the inertia of the resistances along the first five minutes (represented in the abscissa) following the voltage sweeps. The colors of the curves match the ones of the curves in (a).*

Once the resistances reached 400000 Ω, the voltage sweep was stopped, and the resistances were monitored for five minutes with a ten-second time step —represented as the vertical ends of the curves. Figure 2-21.b presents the same resistance evolution over the first five minutes following the end of the voltage sweep, plotted as a function of time. Both graphs confirm that all switches exhibit

a resistance drift immediately after the voltage sweep ends, with the resistance nearly doubling within the first five minutes. The time scale of this effect —occurring over days— far exceeds the microseconds required for the switches to cool to room temperature, ruling out further amorphization of the PCM as the cause.

A previous study [116] investigated the drift of the OFF-state resistance in RF phase-change material (PCM) switches over time. The authors demonstrate that this resistance variation is directly linked to the system's enthalpy and, therefore, to the structural relaxation (stabilization) of the PCM. By analyzing the enthalpy evolution of GeTe samples annealed for different durations, they introduce the concept of fictitious temperature (Tf), which reflects the structural state of the material: a higher Tf corresponds to a less relaxed structure. The results indicate that increasing the annealing time lowers Tf until it reaches the annealing temperature, signifying progressive structural stabilization. The resistance follows the same trend: when Tf > Ta (annealing temperature), resistivity increases over time (stabilization phase), whereas when Tf < Ta, resistivity decreases (rejunevation phase). A similar study on GST confirmed these findings and highlighted a "crossover" effect between different parts of the PCM during successive annealings, caused by the coexistence of fast rejuvenation and slow relaxation processes. This behavior underscores the critical role of structural relaxation in the time-dependent drift of R_{OFF} in RF PCM switches.

In the present work, resistance drift occurring over long periods is not included in simulations. For models following consecutive amorphization-crystallization steps, the absence of R_{OFF} drift between pulses contributes to discrepancies between simulated and measured device resistances.

2.4 Conclusion

This chapter established the methodological foundation used to study and optimize the electrothermal behavior of RF phase-change switches. By combining finite element modeling and experimental characterization approaches, it provided a coherent framework for understanding the physical mechanisms governing device operation and performance. The modeling work began with thermally equivalent schematics, which were progressively refined into simplified and full three-dimensional representations of the switch. These models enable a detailed analysis of heat distribution, energy consumption, and the extent of the PCM region affected by phase change. Through this stepwise approach, key design parameters —such as heater geometry, layer thicknesses, and material properties— were identified as major factors influencing switching efficiency and power-handling. The definition of physical parameters, including the proportional scaling of voltage and the precise evaluation of heater resistivity, ensures that simulations reproduce realistic operating conditions. Temperature-based estimation methods are also introduced to approximate the fraction of PCM undergoing amorphization, compensating for the absence of explicit phase-change modeling in COMSOL Multiphysics®. These methodological elements remain central to the modeling workflow employed throughout the next chapters.

The second part of the chapter presented the experimental characterization methods used to evaluate the electrical and RF performance of fabricated devices. These include the measurement setups, control systems, and acquisition protocols designed to assess switching dynamics, extract S-parameters, and evaluate power-handling capability. Together, these techniques form a comprehensive framework for investigating the relationships between electrical excitation, thermal response, and RF behavior in PCM-based switches.

The final section discussed several factors responsible for discrepancies between simulated and experimental observations, such as thermal boundary resistances, material imperfections, and long-term resistance drift. Accounting for these effects is essential to refine the models and achieve closer alignment with real device behavior.

Overall, this chapter defines a robust methodological loop in which modeling guides design improvements, and experimental characterization provides the feedback necessary for further refinement. Building on these methods, the next chapter applies the developed tools to the optimization of the PCM switch design. It focuses on three key aspects —layer dimensions, material selection, and voltage pulse shape— which together determine the thermal, electrical, and RF performance of the device. Using the simplified 3D sliced model introduced earlier as a baseline, the following analysis explores how these parameters influence energy efficiency, amorphization dynamics, and ultimately RF and power-handling behavior.

Chapter 3
Behaviors of PCM-based RF switches

When optimizing a PCM switch, three key parameters must be addressed: the layer dimensions, the material selection, and the shape of the voltage pulse applied to the heater. Optimizing these parameters is crucial to balance the switch's performance metrics, which include the maximum temperature reached in critical components (such as the heater), the energy consumed during actuation —calculated using the formula in (11)— , and the speed of the quenching phase. The latter directly determines the extent of PCM amorphization, thereby influencing both RF performance and power-handling capability. This chapter aims to characterize the overall behavior of the switch as its design parameters are varied, providing insights into the dimensional ranges, material choices, and voltage pulse shapes most likely to yield optimal performance. To establish a solid foundation for understanding device behavior, the first part of this chapter focuses on optimizing the PCM region targeted for melting in simulations. The second part examines the two most critical components —the PCM and the heater— by systematically varying their thicknesses and assessing the resulting effects on resource consumption, reliability, and quench speed. The third part explores various material and thickness combinations for the dielectric layer positioned between the PCM and the heater, while monitoring the same performance metrics. The fourth part then investigates combinations of heater width and RF_{gap} length over wide parameter ranges, revealing distinct thermal behaviors depending on the simulated configurations. Finally, the last part optimizes the forming method introduced in Section 2.2.1, improving measurement accuracy while avoiding unnecessary extensions of test duration.

All simulations presented in this chapter employ the simplified 3D sliced model described in Section 2.1.2. Figure 3-1 illustrates the reference design used throughout this study, and Table 3-1 summarizes the dimensions of all layers considered in the reference configuration.

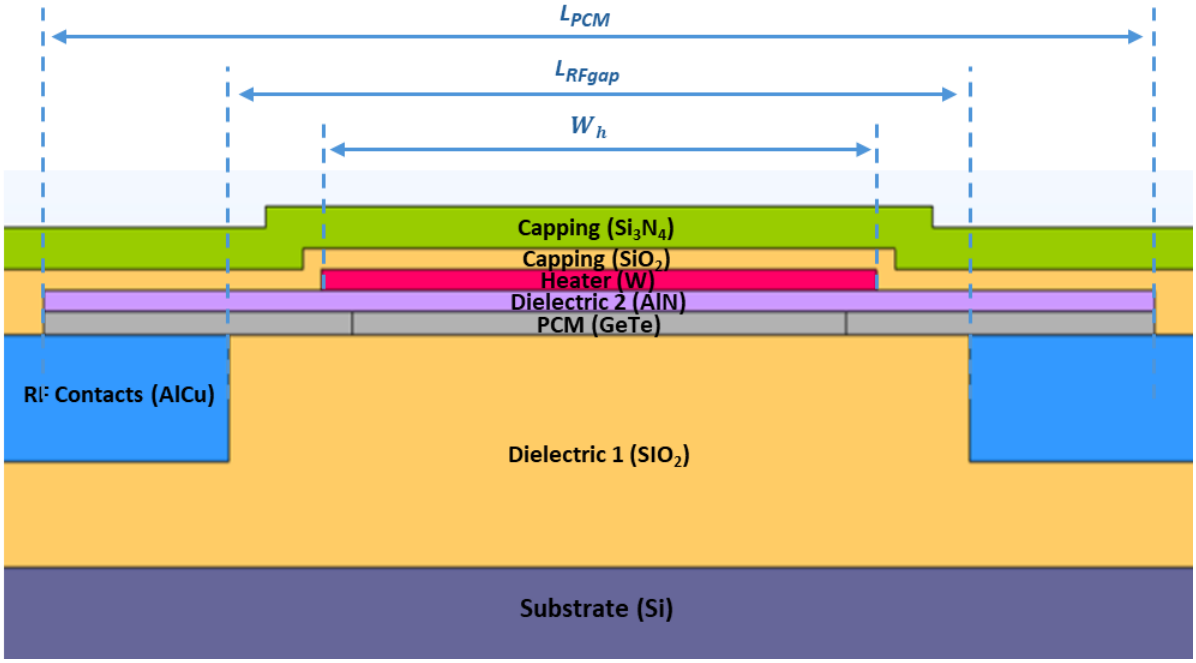


Figure 3-1 : *3D cross-sectional model employed in the simulations throughout this chapter.*

The analysis focuses specifically on the amorphization pulse, lasting 400 ns. To evaluate the quench duration, it is assumed that the quenching duration of a previously melted point in the PCM

corresponds to the time required for the material to cool from its melting temperature (998 K) down to below 500 K.

Table 3-1 : *Parameters of the different layers and materials used in the design of Figure 3-1.*

Layer	Width (length for the PCM) [µm]	Thickness [nm]
Capping (Si_3N_4)	30 (switch width)	**200**
Capping (SiO_2)	30 (switch width)	100
Heater (W)	3	100
Dielectric 2 (AlN)	4	100
PCM (GeTe)	6	110
RF_{gap} (SiO_2)	4	1100
RF contacts (AlCu)	13	600
Dielectric 1 (SiO_2)	30 (switch width)	500
Substrate (Si)	30 (switch width)	15000

The selection of these reference parameters results from the optimization and analysis detailed throughout the chapter. Accordingly, in each section, only the parameters under investigation differ from the baseline configuration shown in Figure 3-1.

3.1 Studied PCM zone

In fabricated devices, accurately determining which regions of the PCM have transitioned to the amorphous state and which remain crystalline is a challenging task. Transmission electron microscopy (TEM) is generally required to investigate the switching outcome; however, even with TEM, the amorphous regions often display irregular geometries, further complicated by phenomena such as void formation and elemental segregation. For this reason, simulations must begin with a clear definition of the target PCM region for amorphization. As is generally the case when switching a device to the OFF state, the objective is to maximize the amorphized volume of PCM, as this directly enhances both RF performance and power-handling capability.

Since the phase-change mechanism itself was not explicitly implemented in the simulations conducted for this study, the analysis relied on defining the portion of the PCM required to reach the melting temperature. Based on this assumption, the objective was twofold: (i) to achieve melting with minimal energy consumption, and (ii) to minimize the quench duration to maximize the chances of preventing recrystallization before the melted region fully cooled. To establish the target melt region, a series of simulations was performed across different PCM volumes. Figure 3-2 illustrates the various regions investigated.

Temperature evolution was tracked at four reference points within the PCM to estimate quench durations: P1 and P3 were positioned at the midpoint of the PCM length (top and bottom surfaces, respectively), while P2 and P4 were located at the extremities of the tested region (again at the top and bottom surfaces). In addition to quench durations, the simulations also computed key performance indicators: the energy consumed by the heater along the amorphization pulse, the applied voltage —defined once again as the value just sufficient to bring the defined PCM region to melt to its melting temperature— , and the peak temperature reached in the heater at the end of the heating step. A summary of all the results is provided in Table 3-2.

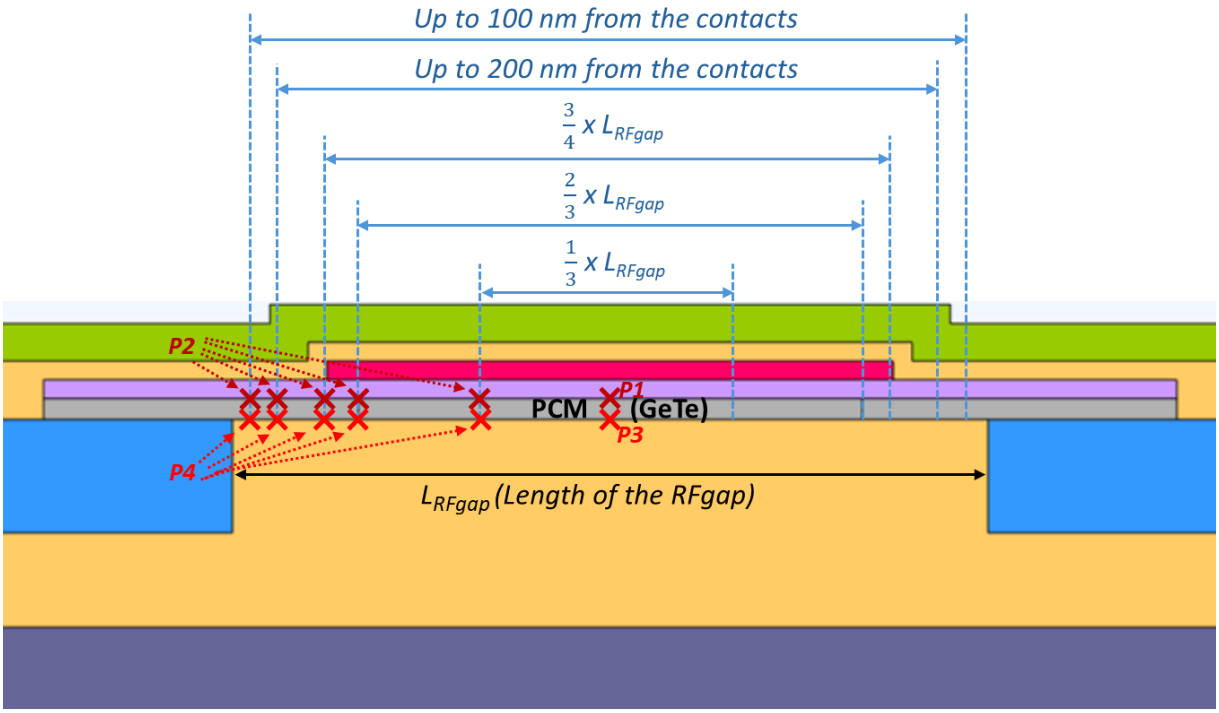


Figure 3-2: *Tested PCM region sizes and quench duration observation points used in Table 3-2.*

In the first simulation scenario, where the melted portion is defined as one-third of L_{RFgap} (second column in Table 3-2), quench durations are essentially identical at all observation points. This uniformity arises because the extremities of the melted region are sufficiently distant from the RF contacts, combined with the 4 µm RF_{gap} length. As a result, heat is distributed evenly throughout the melted PCM region, yielding consistent quench durations across all points.

Table 3-2 : *Switch performance evaluated for each of the PCM melted regions defined in Figure 3-2. The green-marked column corresponds to the reference configuration used throughout the other sections of this chapter.*

PCM studied zone	$(\frac{1}{3})$ x RF_{gap}	$(\frac{2}{3})$ x RF_{gap}	$(\frac{3}{4})$ x RF_{gap}	250 nm from RF contacts	100 nm from RF contacts
Voltage [V]	4.62	**4.94**	5.15	5.78	6.69
Energy [nJ]	166	**190**	**206**	**260**	**348**
Tmax heater [K]	1118	**1244**	1331	1611	2052
Quench duration PCM P1 [ns]	600	**700**	750	925	1125
Quench duration PCM P2 [ns]	600	**625**	675	775	925
Quench duration PCM P3 [ns]	600	**700**	775	925	1125
Quench duration PCM P4 [ns]	600	**625**	650	725	925

When the melted portion is increased to two-thirds of L_{RFgap} (third column in Table 3-2), differences in quench durations emerge between the center of the PCM and the extremities. In this configuration, the extremities are now close enough to the RF contacts so that heat is evacuated more efficiently from these points. Despite these local variations, the overall performance parameters remain comparable to the one-third L_{RFgap} case. However, doubling the potentially amorphized PCM volume provides a significant potential improvement in RF and power-handling (PH) performance, making the

two-thirds L_{RFgap} configuration a more favorable choice. Extending the melted portion to three-quarters of L_{RFgap} (fourth column in Table 3-2) results in slightly higher energy consumption, increased peak heater temperatures, and longer quench durations compared to the two-thirds case. However, these simulations are based on a 4 µm RF_{gap}. For switches with shorter RF_{gap}, such as 2 µm, a three-quarters L_{RFgap} melt region would leave only 500 nm of unmelted PCM, placing the extremities just 250 nm from the RF contacts. The next paragraph explains why proximity to the RF contacts poses challenges for switch performance.

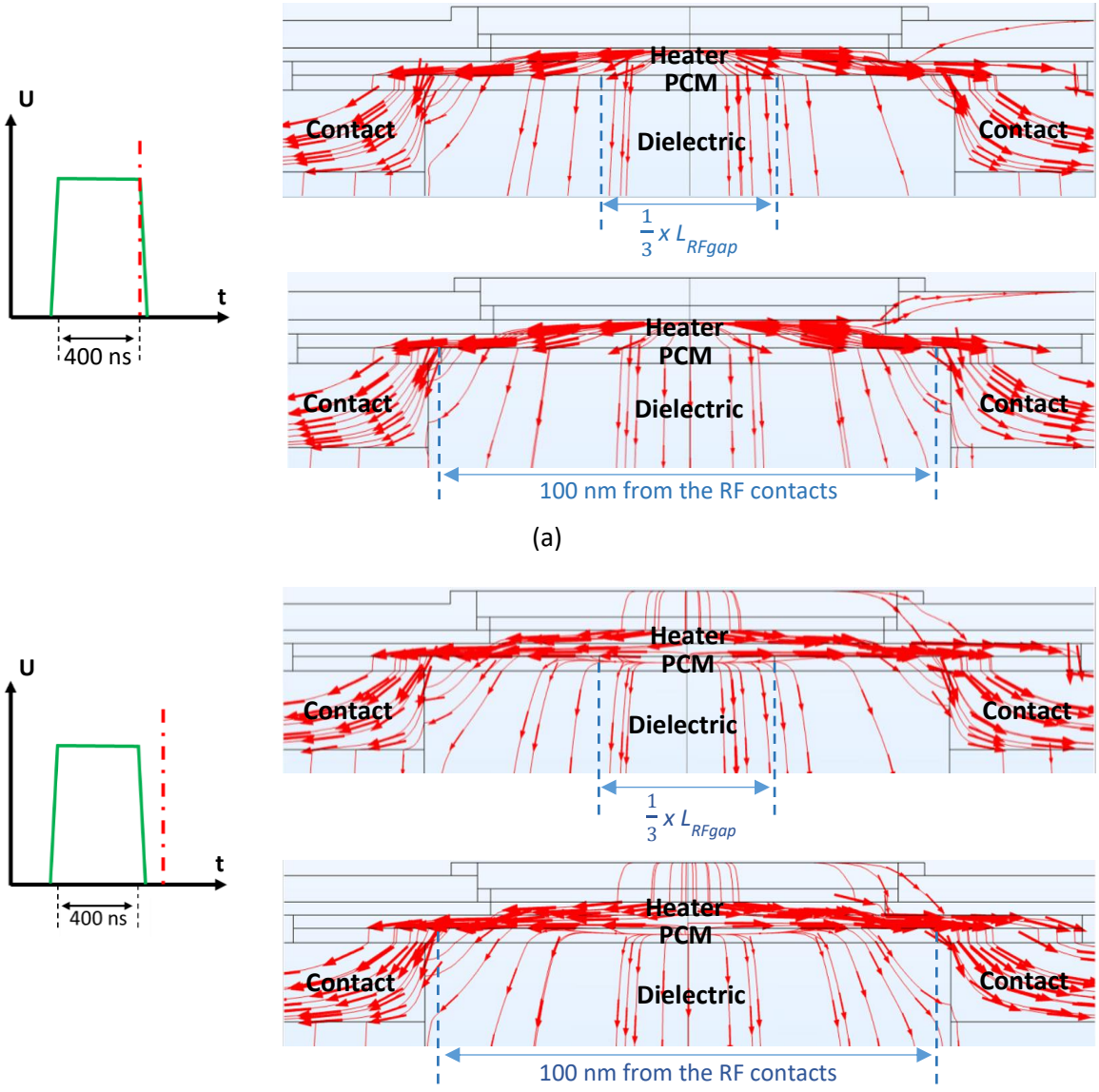


Figure 3-3: *Heat flux in short (defined as one-third of the RF_{gap}) and long (up to 100 nm from the RF contacts) melted PCM regions, shown (a) at the end of the heating phase and (b) during the quench phase. Arrow size is proportional to flux magnitude, while streamlines illustrate the continuity of heat paths. On the left, chronograms of the amorphization pulse are provided, with red vertical lines indicating the extraction time points for the results displayed on the right.*

Increasing the PCM portion size to within 250 nm (fifth column in Table 3-2) or 100 nm (sixth column in Table 3-2) of the RF contacts makes it difficult for the heater to deliver sufficient heat to fully melt the PCM. As the extremities of these portions approach the RF contacts, heat dissipation during the heating phase significantly increases, forcing the heater to compensate by providing significantly more

energy. Figure 3-3.a illustrates the difference between a short PCM portion and a long one in this regard. In the case of the short portion, heat is primarily directed toward the low thermal conductivity dielectric of the RF_{gap}, which helps retain heat within the PCM. By contrast, in the long portion scenario, part of the heat flux from the heater is conducted through the extremities of the PCM directly to the RF contacts, making it harder to retain heat in these regions.

The primary consequence of this increased heat evacuation is a marked increase in energy consumption, which runs counter to the goal of optimizing switch energy efficiency. The second consequence is a substantial increase in the peak temperature that the heater must reach to compensate, jeopardizing its structural integrity and reducing overall reliability. Furthermore, the heat accumulated at the center of the PCM also increases. For instance, Table 3-2 shows that points P1 and P3 reach temperatures of 2045 K and 1860 K, respectively, when the PCM portion is just 100 nm from the RF contacts, while the two-thirds L_{RFgap} configuration results in much lower temperatures at these points —1240 K and 1139 K. These higher temperatures lead to significantly longer quench durations for the PCM: at the center, because more heat must be dissipated, and at the extremities, because the elevated heat content from the center and surrounding layers impedes thermal evacuation. Figure 3-3.b illustrates how heat continues to flow from the heater to the extremities of the PCM zone during the quench in the case of a longer PCM portion targeted.
Based on these analyses, defining the melted PCM portion as two-thirds of the L_{RFgap} emerges as a suitable tradeoff, offering a substantial volume of potentially amorphous material while keeping energy consumption within acceptable limits and avoiding excessive strain on the heater or prolongation of the quench duration. With the melted PCM portion now optimized, attention turns to the influence of PCM thickness on the device's thermal behavior. This dimension plays a decisive role in determining the energy required for melting and the efficiency of heat dissipation during quenching.

3.2 PCM thickness

While the previous section focused on the impact of the melted PCM zone length on switch behavior, this section examines the effect of PCM thickness —denoted a t_{PCM}— on device performance. In the following set of simulations, t_{PCM} was systematically varied, and the resulting switch performances were evaluated. Figure 3-4 presents the different switch designs simulated, with the corresponding performance metrics summarized in Table 3-3.

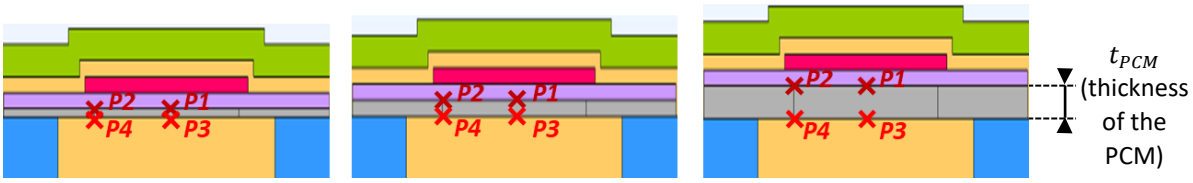


Figure 3-4 : *Model configurations with PCM thicknesses of (a) 50 nm, (b) 100 nm, and (c) 200 nm, showing observations points for the quench durations of Table 3-3. The definition of the PCM thickness (t_{PCM}) is shown in (c).*

Starting with a thin PCM layer (t_{PCM} = 50 nm), simulations show a rapid quench, with temperatures falling below the 500 K threshold defined to prevent recrystallization. Energy consumption is also low, measured at 183 nJ. Increasing the thickness to 100 nm results in longer quench durations —now inducing recrystallization— , which is expected, as a larger PCM volume requires more heat to be dissipated. To achieve melting, the heater must deliver additional thermal energy, achieved by raising the applied voltage. This results in a higher peak heater temperature during the pulse and increased

energy consumption. However, the thicker PCM also provides a larger volume of material, improving ON-state RF and power-handling (PH) performance and potentially improving overall FOM. Further increasing the thickness to 200 nm could, in principle, enhance these benefits, but quench durations rise again at all observation points, indicating that additional design adjustments would be necessary to manage thermal dissipation effectively and fully exploit the increased PCM volume.

Table 3-3 : *Switch performance for different PCM thicknesses, as illustrated in Figure 4. The green-marked column corresponds to the reference configuration used throughout the other sections of this chapter*.

PCM thickness [nm]	50	100	200
Voltage [V]	4.86	**4.92**	5.16
Energy [nJ]	183	**188**	207
Quench duration PCM P1 [ns]	475	**675**	875
Quench duration PCM P2 [ns]	425	**625**	825
Quench duration PCM P3 [ns]	425	**675**	900
Quench duration PCM P4 [ns]	425	**625**	800

Consequently, a PCM thickness of 100 nm emerges as a suitable compromise, offering a substantial amount of crystalline and amorphous volume while keeping the quench duration within acceptable limits. With this key layer dimension defined, attention now turns to the heater, the component directly responsible for initiating the phase transition.

3.3 Heater thickness

The heater's geometrical characteristics, particularly its thickness, strongly influence both the energy required to actuate the PCM and the device's overall efficiency. The heater must supply sufficient thermal energy to the PCM to ensure actuation while minimizing energy consumption and limiting parasitic capacitances in the OFF state between the heater and the crystalline PCM regions. This section examines the influence of heater thickness —denoted as t_h— on switch performance.

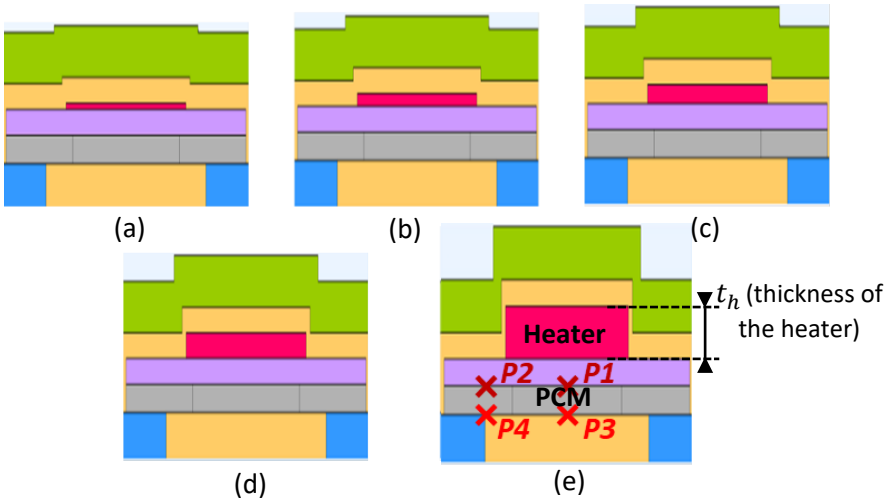


Figure 3-5 : *Design of the switch with a heater thickness of (a) 25 nm, (b) 50 nm, (c) 75 nm, (d) 100 nm, and (e) 200 nm. Observation points corresponding to performance metrics reported in Table 3-4, along with the definition of the dielectric thickness (t_h), are shown in (e).*

To evaluate this, a series of simulations was conducted with t_h varying from 25 nm to 200 nm. The resulting designs are shown in Figure 3-5, while the corresponding performances metrics are

summarized in Table 3-4. This table details energy consumption, applied voltage and the peak temperature reached in the heater. Interestingly, these parameters do not all follow the same trend. Energy consumption increases with heater thickness, while the maximum temperature reached in the heater decreases. As for applied voltage, an optimal value is observed around a thickness of 75 nm; increasing or decreasing the thickness from this point results in higher voltages being required.

Table 3-4 : *Voltages required to melt two-thirds of the PCM, associated energy consumption, maximum temperature reached in the heater, and quench durations at the four points defined in Figure 3-5. The green-marked column corresponds to the reference configuration used throughout the other sections of this chapter.*

Heater thickness [nm]	25	50	75	100	200
Voltage [V]	5.56	4.94	4.86	**4.94**	5.67
Energy [nJ]	183	185	187	**190**	205
Tmax heater [K]	1329	1286	1263	**1244**	1208
Quench duration PCM P1 [ns]	725	700	700	**700**	750
Quench duration PCM P2 [ns]	625	625	625	**625**	700
Quench duration PCM P3 [ns]	725	700	700	**700**	750
Quench duration PCM P4 [ns]	625	600	625	**625**	700

All of these trends are directly related to the evolution of the heater's resistance, which depends on its dimensions and its resistivity —denoted a ρ_{rT}. The expression for the heater's resistance at room temperature was defined in (12) as:

$$R_{rT} = \rho_{rT} * \left(\frac{L_h}{W_h * t_h}\right)$$

This formula indicates that the heater's resistance decreases as its thickness increases. It is noted that, for the same applied voltage, a thinner heater reaches a higher temperature than a thicker one. For instance, comparing heaters of 25 nm and 200 nm thickness —both requiring approximately the same voltage to melt two-thirds of the PCM overlapping the RF_{gap} — the 25 nm heater reaches a temperature roughly 120 K higher than the 200 nm heater. Likewise, under the same applied voltage, the 50 nm heater attains a temperature approximately 40 K higher than that of the 100 nm heater. Regarding energy consumption, its expression, also introduced in (11), is:

$$E = \int_0^t \left(\frac{2 * U_c}{R_g + R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right)} \right)^2 * R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right).dt$$

Where, for recall :

- $\boldsymbol{TCR}$**:** Thermal coefficient of resistance ($1.35*10^{-2}$ K^{-1} for tungsten)
- $\boldsymbol{U_c}$**:** Command voltage applied by the user to the generator
- $\boldsymbol{R_{rT}}$**:** Initial heater resistance at room temperature
- $\boldsymbol{R_g}$**:** Internal resistance of the generator
- $\boldsymbol{T_r}$**:** Room temperature
- $\boldsymbol{\tau}$**:** Time constant representing the rate of temperature increase

When the evolution of this integral is plotted for a fixed voltage —such as 5 V— the result appears as illustrated in Figure 3-6.

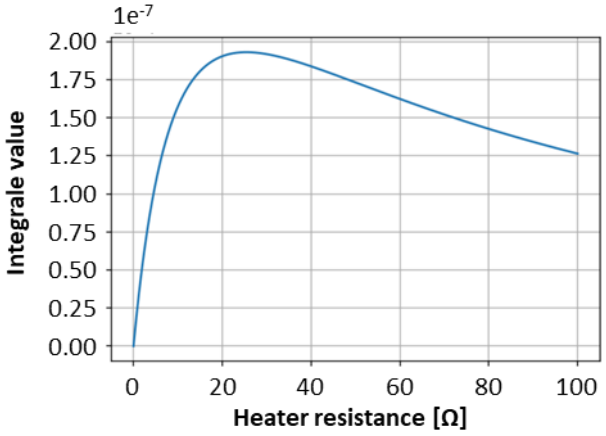


Figure 3-6 : *Evolution of energy consumption as heater resistance increases under a constant applied voltage.*

The graph shows that energy consumption initially increases for resistance values between 0 Ω and approximately 25 Ω, then starts to decrease as the resistance rises further. This trend arises because, when R_{rT} falls within the 0 Ω-25 Ω range, the expression:

$$R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right) \tag{26}$$

in the denominator of the energy consumption formula is dominated by the value of R_g, which is 50 Ω. When simplified, the formula becomes:

$$E = \int_0^t \left(\frac{2 * U_c}{R_g}\right)^2 * R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right).dt \tag{27}$$

Consequently, within this interval, the energy consumption rises as R_{rT} increases, due to its presence in the multiplicative term of the energy formula. Once R_{rT} exceeds 25 Ω, it begins to dominate over R_g, supported by the increasing thermal gradient. From this point, the simplified formula can be expressed as:

$$E = \int_0^t \left(\frac{2 * U_c}{R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right)}\right)^2 * R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right).dt \tag{28}$$

Which, when further simplified, gives:

$$E = \int_0^t \left(\frac{2 * U_c}{R_{rT} * \left(1 + TCR * ((1 - e^{-\left(\frac{t}{\tau}\right)}) * (t_h - T_r))\right)}\right).dt \tag{29}$$

From this point onward, the energy consumption continues to decrease as R_{rT} increases. The resistances of the various heaters analyzed in this section are summarized in Table 3-5. These values are calculated assuming a heater length of 19 µm, a width of 3 µm, and a room-temperature resistivity of tungsten of $3.07*10^{-10}$ Ω.cm.

Table 3-5*: Heater resistances corresponding to each design shown in Figure 3-5.*

Heater thickness [nm]	25	50	75	100	200
Resistance at room temperature [Ω]	77.95	38.97	25.98	**19.49**	9.74
Voltage [V]	5.56	4.94	4.86	**4.94**	5.67
Energy [nJ]	183	185	187	**190**	205

Starting with a 25 nm heater (183 nJ), increasing the thickness to 50 nm lowers the voltage needed to reach the PCM's melting point. However, this also causes a strong drop in room-temperature resistance. As shown in Figure 3-6, this shift toward lower resistances slightly increases the integrated energy, meaning that the resistance decrease has a greater effect than the modest voltage reduction. Consequently, the total energy consumption rises slightly. From 75 nm to 100 nm, the voltage begins to increase again, while resistance continues to fall. In this range, the change in resistance has less influence, so the rising voltage dominates, leading to a further increase in energy. This trend becomes clearer at 200 nm, where both the higher voltage and resistance behavior contribute to a continued rise in energy consumption. Simulations indicate that the applied voltage is minimal at a thickness of 75 nm. For thinner heaters (25–50 nm), the small volume and high resistance require higher voltages to produce sufficient heat, explaining their higher temperature. Beyond 75 nm, increasing thickness lowers resistance but enlarges the heater volume, reducing heating efficiency. Therefore, the voltage must increase again to maintain melting.

A 100 nm heater offers a good compromise: energy consumption remains close to that of 75 nm, but the larger volume and lower resistance improve reliability by reducing maximum temperature. Thicker heaters would demand higher voltages and generate more heat, slowing the quenching process (see Table 3-4). With the heater dimensions now defined, the next step addresses the interaction between the heater and the PCM. Because these two components cannot be in direct contact, the dielectric layer separating them becomes a key element in controlling both electrical isolation and thermal transfer efficiency.

3.4 Dielectric between PCM and heater

3.4.1 Material for dielectric between PCM and heater

A clear separation is required to prevent interference between the signal transmitted through the PCM and the current flowing in the heater. This electrical and functional isolation is achieved by introducing a dielectric layer between the two components. The choice of dielectric material strongly influences the thermal behavior of the switch. Using a dielectric with high thermal conductivity enables faster heat dissipation from the PCM during the quench phase, reducing the risk of recrystallization. However, during the heating phase, such materials also channel a considerable fraction of the heat generated by the heater toward the RF contacts, thereby reducing the thermal energy available for melting the PCM. Conversely, a dielectric with low thermal conductivity helps retain heat within the PCM during heating, improving energy transfer efficiency, but impedes heat evacuation during the quench, which increases the likelihood of recrystallization.

To assess which dielectric provides the most favorable balance of properties, simulations were carried out using aluminium nitride (AlN) as a high–thermal-conductivity option and silicon dioxide (SiO_2) as a low–thermal-conductivity counterpart. Figure 3-7.a presents the heat flux distributions immediately before the start of the quench phase. With AlN, most of the heat generated by the heater is conducted directly toward the RF contacts, bypassing much of the PCM. In contrast, with SiO_2, the majority of the

heat flows downward toward the silicon substrate, passing through the PCM along its path. For a dielectric thickness of 100 nm, this difference leads to a 60 nJ reduction in energy consumption when SiO_2 is used instead of AlN. Figure 3-7.b shows the situation 100 ns after the onset of the quench phase. The same tendencies remain: in the AlN configuration, heat is rapidly evacuated toward the RF contacts, while in the SiO_2 case, evacuation occurs primarily downward through the RF_{gap} dielectric. Because this RF_{gap} dielectric is also made of thermally insulating SiO_2, heat evacuation is significantly slower —resulting in a quench duration nearly twice as long as that observed with AlN.

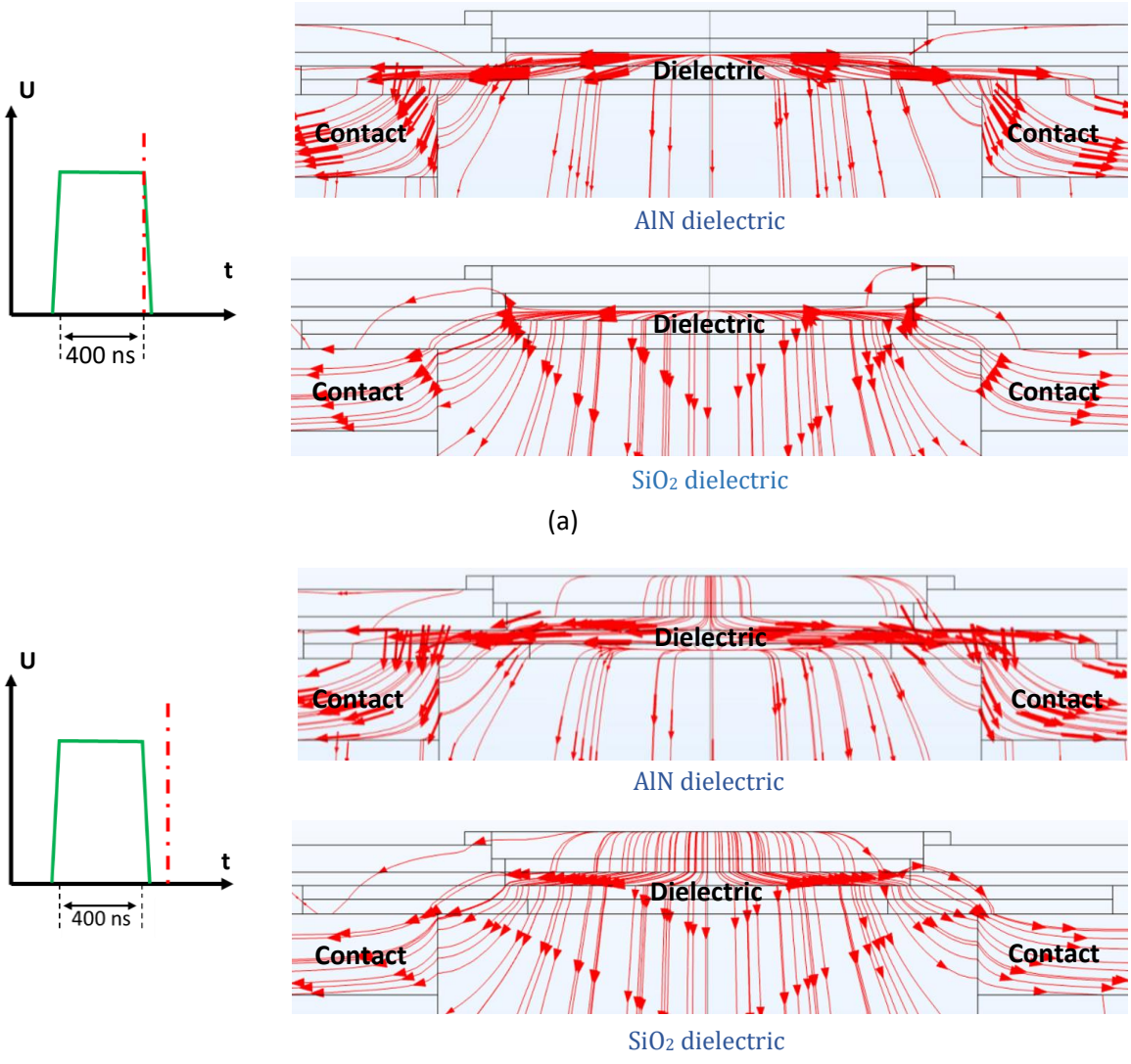


Figure 3-7: *Heat flux distribution in both short and long melted PCM regions, shown (a) at the end of the heating phase and (b) during the quenching phase. Arrow size is proportional to flux magnitude, while streamlines illustrate the continuity of heat paths. On the left, chronograms of the amorphization pulse are provided, with red vertical lines indicating the extraction time points for the results displayed on the right. AlN channels heat toward the RF contacts, facilitating its evacuation during the quench, whereas SiO_2 directs heat toward the PCM, ensuring its efficient heating*

Ultimately, AlN emerges as the more suitable dielectric for isolating the heater from the PCM. Although it entails a modest increase in energy consumption, it markedly accelerates the quench phase —a benefit that directly enhances both RF performance and power-handling (PH) capabilities.

3.4.2 Thickness of dielectric between PCM and heater

With the dielectric material now established, the next step is to determine the optimal thickness of the layer separating the heater from the PCM. The dielectric's width and length were fixed to match those of the PCM, while its thickness —denoted as t_D— was systematically varied between 25 nm and 300 nm, as illustrated in Figure 3-8. As in previous analyses, the following parameters were monitored: energy consumption, heater voltage, maximum heater temperature during the pulse, and quench durations at standard observation points within the PCM. The corresponding results are summarized in Table 3-6, which also includes a reference simulation batch using SiO_2 for comparison.

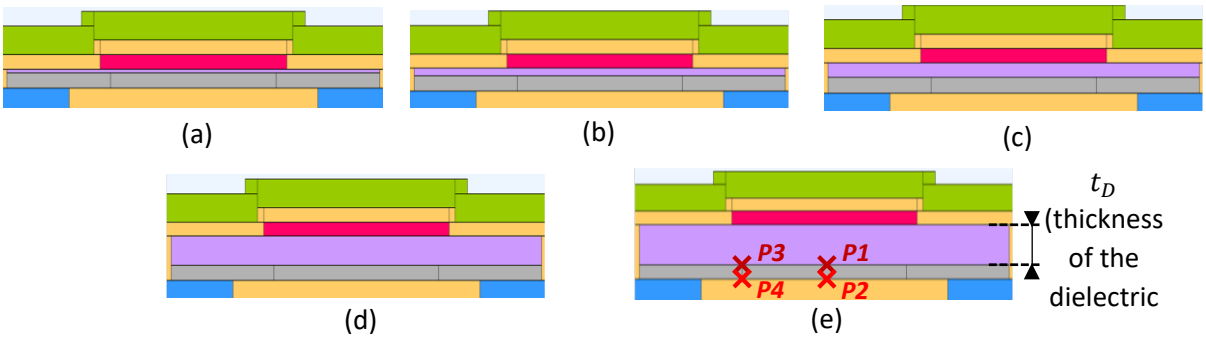


Figure 3-8: *Simulated switch designs with an AlN dielectric layer between the heater and the PCM, featuring layer thicknesses of (a) 25 nm, (b) 50 nm, (c) 100 nm, (d) 200 nm, and (e) 300 nm. Observation points corresponding to performance metrics reported in Table 6, along with the definition of the dielectric thickness (t_D variable), are shown in (e).*

A very thin AlN dielectric layer was found to exert little influence on switching behavior. At 25 nm, the configuration yields the lowest energy consumption, heater voltage, and maximum heater temperature, owing to efficient heat transfer across the thin layer. However, the quench duration is longer compared to thicker configurations, as less heat is removed from the PCM during this phase. Increasing t_D to 50 nm and then 100 nm reversed this trade-off: energy consumption rose, as more heat was diverted toward the RF contacts during heating, requiring greater input from the heater. On the other hand, the quench duration decreased, because the thicker dielectric promoted more effective heat removal from the PCM toward the RF contacts during cooling.

However, increasing t_D beyond 100 nm continues to raise energy consumption while offering little to no improvement in quenching performance. The most notable gains in heat evacuation from the PCM occur at the first thickness increments, where the AlN layer begins efficiently channeling heat from the PCM to the RF contacts. Beyond this point, the marginal impact on heat evacuation diminishes. Figure **3-9** illustrates the case of a 300 nm-thick AlN layer during the quenching phase: the heat flux from the PCM, directed toward the RF contacts through the AlN layer, remains concentrated near the interface between the PCM and the dielectric.

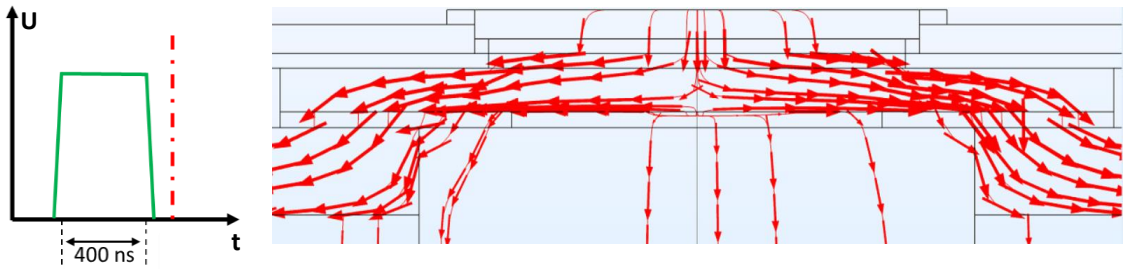


Figure 3-9: *Heat flux measured 100 nm into the quench phase for a switch featuring a 300 nm thick AlN layer between the heater and the PCM.*

This demonstrates that increasing the dielectric thickness mainly raises the heating demand —since a thicker dielectric extends the thermal path between the heater and the PCM, requiring higher voltage and energy— without enhancing heat extraction, as the heat still flows predominantly along the PCM–dielectric interface toward the RF contacts during the quench step. As a result, quenching speed does not benefit from the added thickness and can even deteriorate, since the excess heat disrupts the cooling of the PCM.

Table 3-6: *Switch performance with a dielectric layer between the heater and the PCM made of (a) AlN or (b) SiO_2, for various thicknesses. The green-marked column corresponds to the reference configuration used throughout the other sections of this chapter.*

AlN thickness [nm]	**25**	**50**	**100**	**200**	**300**
Voltage [V]	4.19	4.5	**4.94**	5.5	5.91
Energy [nJ]	136	157	**190**	235	272
Tmax heater [K]	1209	1226	**1244**	1249	1249
Quench duration PCM P1 [ns]	800	725	**700**	725	775
Quench duration PCM P2 [ns]	750	650	**625**	675	725
Quench duration PCM P3 [ns]	800	750	**700**	725	775
Quench duration PCM P4 [ns]	725	650	**625**	675	750

(a)

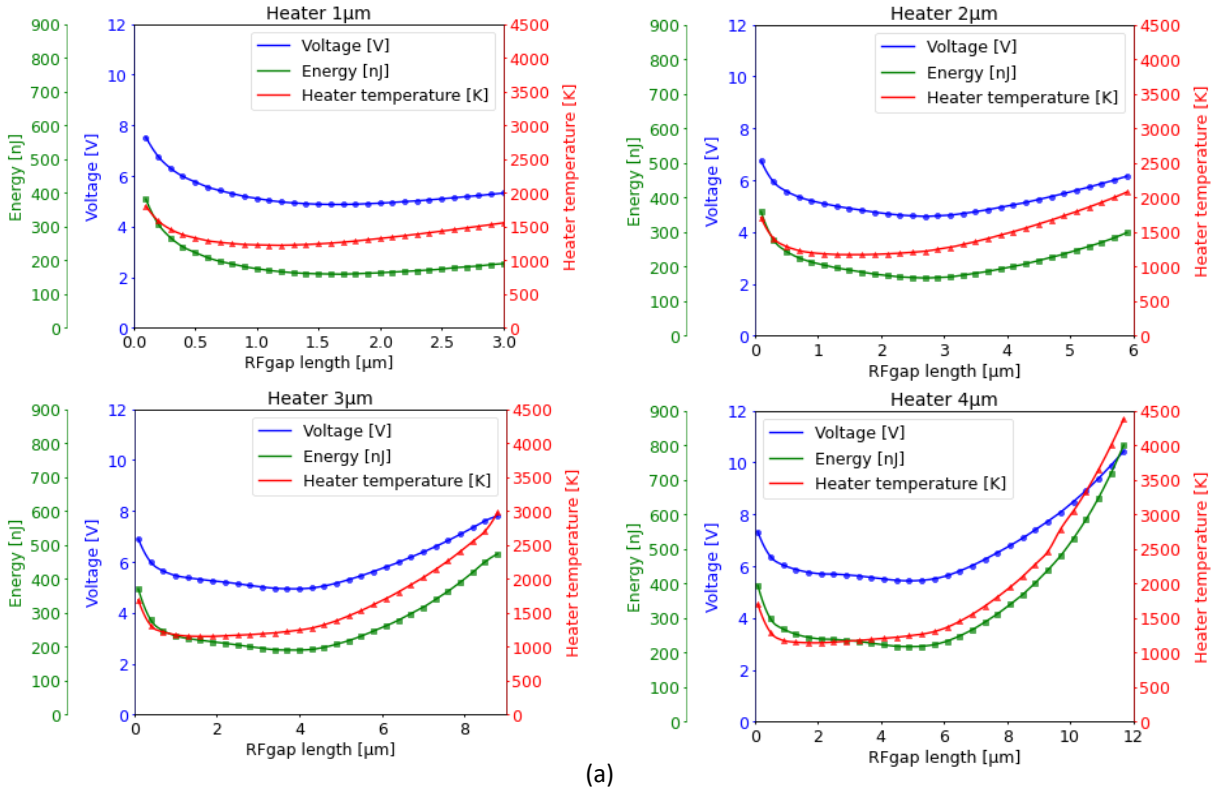
SiO_2 thickness [nm]	**25**	**50**	**100**	**200**	**300**
Voltage [V]	3.77	3.87	4.09	4.57	5.11
Energy [nJ]	111	116	130	162	203
Tmax heater [K]	1234	1294	1430	1743	2118
Quench duration PCM P1 [ns]	1125	1200	1325	1625	2125
Quench duration PCM P2 [ns]	1075	1125	1225	1450	1900
Quench duration PCM P3 [ns]	1100	1175	1300	1600	2100
Quench duration PCM P4 [ns]	1025	1075	1175	1400	1850

(b)

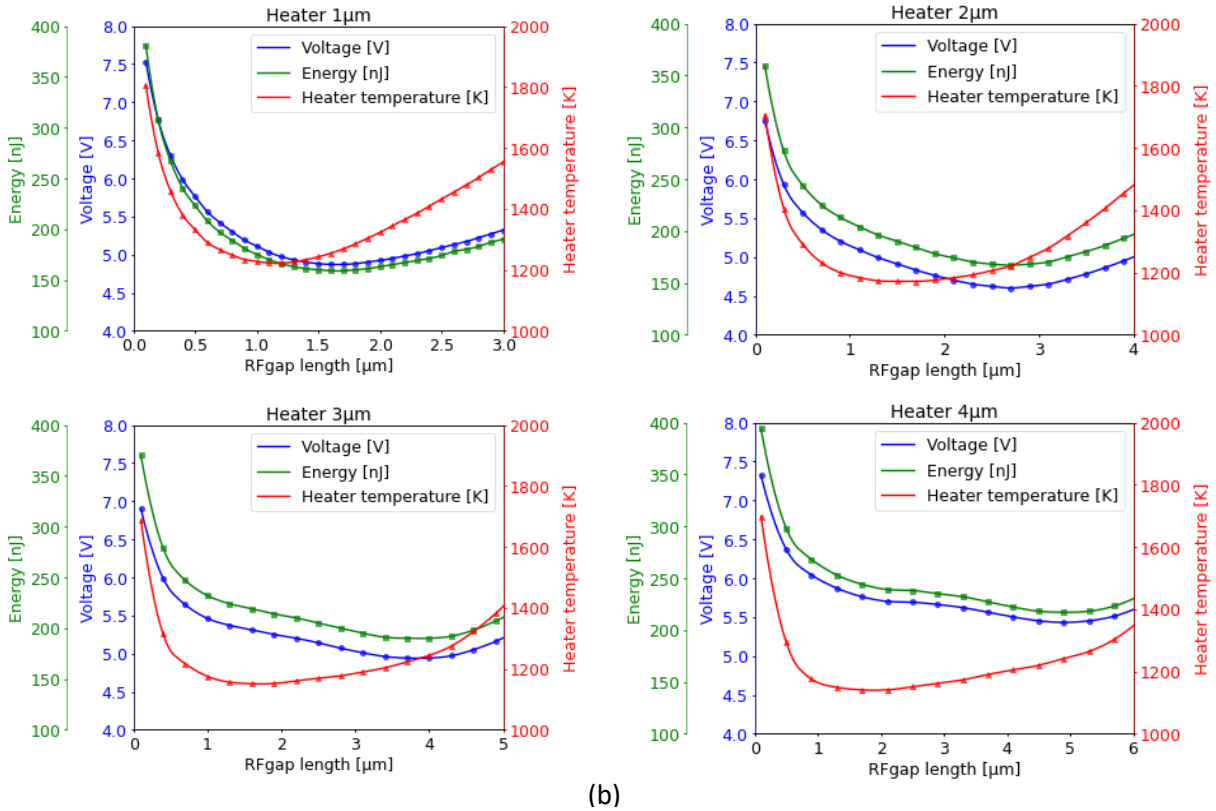
For SiO_2, Table 3-6 shows that the quench duration remains consistently long regardless of dielectric thickness. Moreover, increasing t_D leads to significantly higher heater temperatures, which can threaten device reliability. These findings further reinforce AlN as the more suitable dielectric between the heater and the PCM, with an optimal thickness of about 100 nm. However, if one wants to further reduce parasitic capacitances occurring between the heater and the PCM, further adjustments to the device's geometric parameters are required. Consequently, the next focus is on two critical dimensions —the RF_{gap} length and the heater width— which directly influence the thermal and electrical behavior of the switch.

3.5 RF_{gap} length and heater width

This section examines how the length of the RF_{gap} —which necessitates a corresponding adjustment of the PCM length— and the width of the heater govern the thermal behavior of the switch, with the ultimate aim of identifying the configuration that achieves the optimal balance among heating efficiency, energy consumption, and overall device performance.



(a)



(b)

Figure 3-10: *Voltages applied to the heater (blue), energy consumed (green), and maximum heater temperature (red) for switches with different heater widths, indicated in each graph title. In the first series of plots (a), the x-axis corresponds to all tested RF_{gap} lengths for the given heater width. In the second series (b), the x-axis extends up to RF_{gap} lengths equal to the heater width plus 2 µm.*

The heater width must be sufficient to deliver the heat required for PCM activation; however, an excessively wide heater results in unnecessary energy dissipation. Meanwhile, the RF_{gap} introduces a

more subtle trade-off. Short RF_{gap} bring the RF contacts closer together, which facilitates rapid heat evacuation during the quench phase, yet this configuration makes it more difficult to raise the PCM to its target temperature. Conversely, longer RF_{gap} enhance thermal confinement, allowing the PCM temperature to rise more readily and increasing the volume of material that can be amorphized. While this can improve RF performance and power-handling (PH) capability, it also entails higher energy consumption and slower heat evacuation.

To systematically investigate these effects, heaters with widths of 1 µm, 2 µm, 3 µm, and 4 µm were simulated. For each heater width, the RF_{gap} was varied from 0.1 µm up to three times the heater width, with step sizes selected to balance simulation resolution and computational cost:

- 1 µm heater → RF_{gap} from 0.1 µm to 3 µm in 0.1 µm increments
- 2 µm heater → RF_{gap} from 0.1 µm to 6 µm in 0.2 µm increments
- 3 µm heater → RF_{gap} from 0.1 µm to 9 µm in 0.3 µm increments
- 4 µm heater → RF_{gap} from 0.1 µm to 12 µm in 0.4 µm increments

These variable step sizes ensured that both simulation times and COMSOL file sizes remained manageable. For each configuration, the temperature distribution was recorded across the heater width and along the PCM length at three vertical positions: the top, middle, and bottom of the PCM layer. In all cases, the applied voltage was adjusted so that approximately two-thirds of the PCM reached its melting temperature.

Building on the investigation of heater widths and their impact on PCM activation, the thermal response of both the heater and PCM was next analyzed as a function of RF_{gap} length. Figure **3-10** summarizes these results, presenting, for each heater width, the applied voltages, corresponding energy consumption, and maximum heater temperatures. In Figure 3-10.a, all simulations are plotted together, covering the full range of RF_{gap} examined for each heater width. This comprehensive view particularly emphasizes the behavior of wider heaters when paired with very long RF_{gap}. However, this representation introduces an inherent bias: longer RF_{gap} naturally require more energy to melt the larger volume of PCM. To facilitate a fairer comparison, Figure 3-10.b adopts an alternative perspective, normalizing the horizontal axis to span the heater width plus 2 µm —that is, the heater itself with an additional 1 µm extension on either side.

The following sections detail how the switch's thermal behavior evolves with increasing RF_{gap} length, highlighting the differences across heater widths. This analysis further clarifies why a 3 µm-wide heater combined with a 4 µm-long RF_{gap} represents the most balanced design, optimizing the trade-offs among the switch's multiple performance metrics. To systematically capture thermal profiles along the RF_{gap}, three observation lines were defined within each model, as illustrated in Figure 3-11.

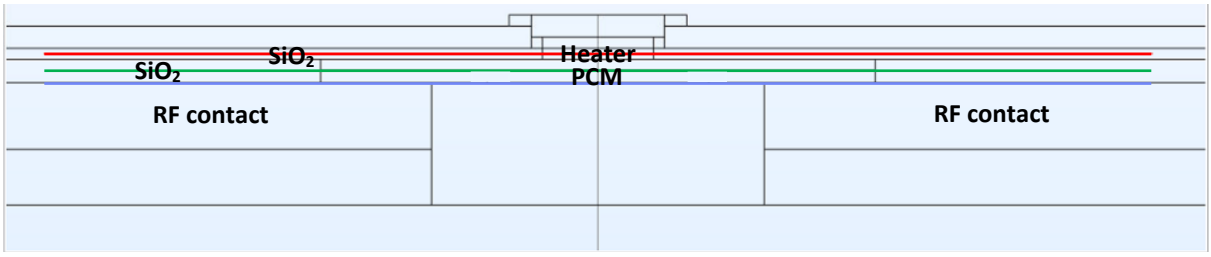


Figure 3-11 : *Observation lines used in the graphs of this section. The red line crosse the width of the heater, the green line crosses the length of the PCM at its top and the blue line crosses the length of the PCM at its bottom.*

One line runs across the heater width at mid-height (red), while the other two extend along the PCM length —one at the top surface (green) and the other at the bottom (blue). Because the 4 µm-wide

heater was simulated with RF_{gap} extending up to 12 µm, all observation lines were extended slightly beyond this range, independent of heater width, ensuring a consistent and comprehensive comparison of thermal behavior across all configurations.

Building on the examination of thermal behavior across different heater widths and RF_{gap}, attention is now directed to the scenario with the shortest RF_{gap}, 0.1 µm, for each heater. This configuration provides a clear view of the challenges associated with heat accumulation when the PCM region to be melted is extremely small and the RF contacts are in close proximity.

3.5.1 Shortest RF_{gap}

In this very short RF_{gap} scenario, the volume of PCM to be melted —approximately two-thirds of the PCM above the RF_{gap}— is considerably smaller than the heater width. Heat is evacuated almost instantaneously through the nearby RF contacts, which complicates the achievement of the PCM's melting temperature. Despite the small melt region, the heaters must attain elevated temperatures to provide sufficient energy. This requirement is reflected in the applied voltages, ranging from 7 V to 8 V, and in the corresponding energy consumption, which spans 350 nJ to 400 nJ, as reported in Figure **3-10**.

3.5.1.1 1 µm-wide heater

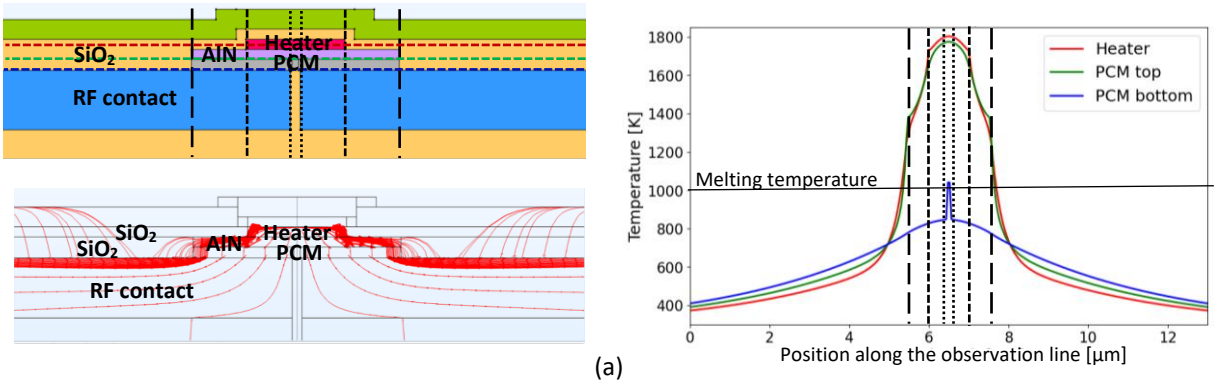
1.1.1.1.1 Bottom of the PCM

Focusing on the bottom of the 1 µm-wide heater, the blue curve in Figure 3-12.a, which traces the temperature along a line across the PCM base, reveals that the maximum temperature occurs at the center of the switch and gradually decreases toward the edges. Within this overall decline, three distinct behaviors can be discerned. First, from the PCM center to the edge of the RF_{gap}, the temperature drops sharply, forming a pronounced dome. This behavior arises because the central portion of the PCM —corresponding to two-thirds of the material that reaches its melting temperature and situated above the low-thermal-conductivity dielectric of the RF_{gap}— is located in close proximity to the RF_{gap} extremities, which are in direct contact with the highly thermally conductive RF contacts. The nearby contacts generate a strong temperature gradient over a short distance, with their thermal influence intensifying near the edges. This results in the steep dome observed at the PCM bottom above the RF_{gap}. Second, as the observation line traverses the PCM regions directly above the RF contacts, the full width of the line is subject to substantial heat extraction imposed by these contacts. Despite this intense thermal drainage, a dome-shaped profile persists, with the temperature declining more gradually near the RF_{gap} and more sharply toward the outer edges of the PCM.

The origin of the dome-shaped temperature profile can be understood by examining the directions of heat flux, as illustrated in Figure 3-12.a. In this figure, the largest arrows indicate the dominant paths of heat flow, while the lines trace the trajectories themselves. At the center of the heater, part of the generated heat spreads laterally toward the sides, whereas the remainder flows more vertically into the PCM. The relatively small arrows in the vertical direction indicate slower heat transport, which promotes accumulation in the central PCM region and thereby elevates its temperature.

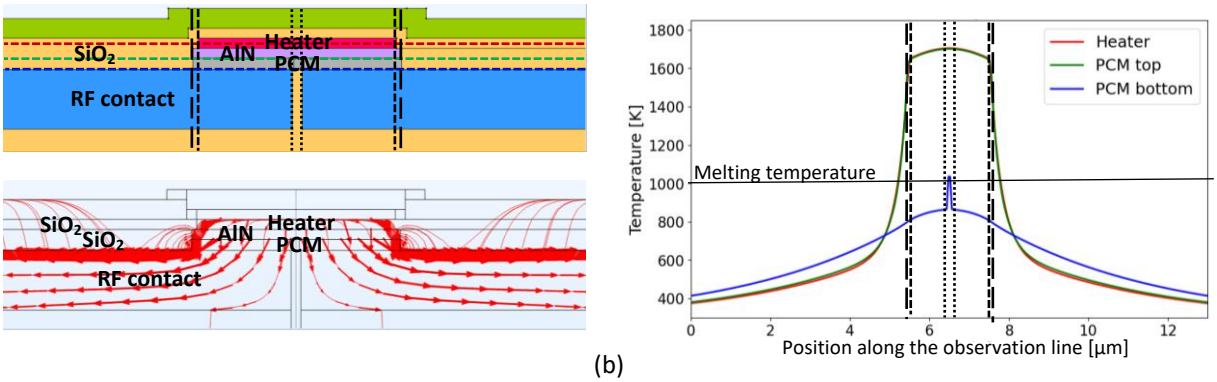
Heat flowing toward the heater edges, as well as heat generated at these extremities, follows the path of least thermal resistance, ultimately being evacuated horizontally through the RF contacts. This evacuation path is strongly influenced by the surrounding layers of the switch, starting with the SiO_2 layers. As thermal dielectrics, these layers act as insulating barriers that restrict vertical heat flow.

W_h = 1 µm ; L_{RFgap} = 0.1 µm



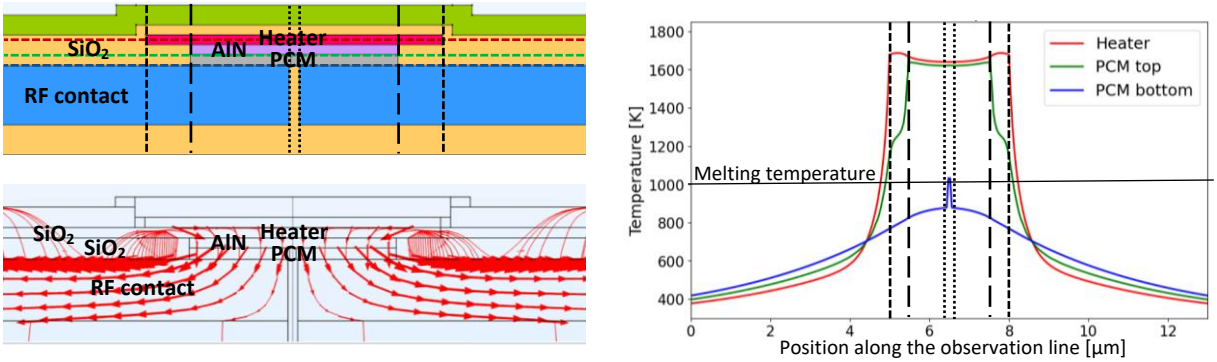
(a)

W_h = 2 µm ; L_{RFgap} = 0.1 µm



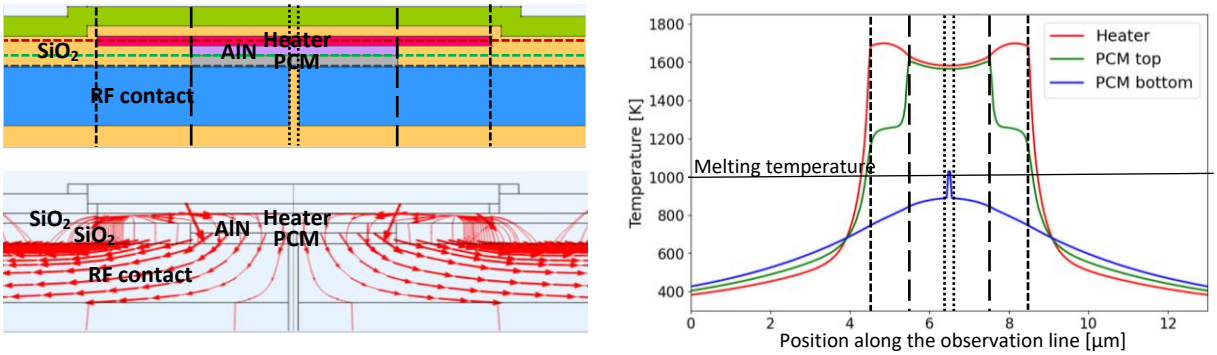
(b)

W_h = 3 µm ; L_{RFgap} = 0.1 µm



(c)

W_h = 4 µm ; L_{RFgap} = 0.1 µm



(d)

Figure 3-12 : *Temperature profiles along the observation lines defined in Figure 3-11 for switches with an RF_{gap} length of 1 µm and heater widths of (a) 1 µm, (b) 2 µm, (c) 3 µm, and (d) 4 µm. The right-hand plots display the temperatures recorded along the observation lines. Vertical black lines indicate the width and length of the different switch elements, with their positions referenced on the corresponding designs shown on the left. The heat fluxes illustrated in the schematics correspond to the same time point at which the temperature profiles were extracted.*

Consequently, heat at the heater edges is guided laterally along the SiO_2 boundaries, seeking the most horizontal route toward the RF contacts. To follow this path, heat first traverses the AlN layer, which, owing to its high thermal conductivity (100 W/(m·K)), efficiently channels heat toward the sides of the switch. Upon encountering additional SiO_2 layers, the majority of the heat continues through the PCM, still guided laterally by the SiO_2, while a small fraction briefly crosses the SiO_2 to reach the RF contacts. This partitioning occurs because the thermal conductivities of SiO_2 (1.4 W/(m·K)) and the underlying crystalline GeTe (2.4 W/(m·K)) are comparable. By contrast, beneath the heater, the highly conductive AlN layer dominates, directing heat primarily through itself rather than the surrounding SiO_2.
Finally, upon reaching the RF contacts, heat flows almost entirely horizontally toward the switch edges, as imposed by the Dirichlet conditions at the lateral extremities, completing its evacuation. This explains the dome shape observed at the bottom of the PCM above the RF contacts: regions near the center of the switch benefit from heat accumulation due to the slower vertical flux, whereas regions near the SiO_2 layers next to the PCM are closer to areas of rapid heat evacuation, producing the characteristic dome profile along the blue observation line. Beyond these central regions, the line follows the boundary between the RF contacts and the SiO_2 above them. In these sections, the temperature continues to decrease toward the sides of the switch, but the rate of decline progressively slows, reflecting the increasingly efficient heat evacuation at the PCM extremities.

3.5.1.1.1 Top of the PCM and mid-height of the heater

Now looking at the green and red observation lines of Figure 3-12.a respectively going through the top of the PCM and the middle of the height of the heater, the temperatures reached along them are way higher. The associated curves on the graph of the same figure show similar values and behaviors; this is because the top of the PCM shares a boundary with the AlN layer. Therefore, on the contrary to the bottom of the PCM which is almost totally (except from the very central part above the narrow RF_{gap}) in contact with the RF contacts and therefore has its heat directly drained, the top of the PCM is directly receiving the heat generated by the heater and transmitted by the AlN layer, almost replicating the same heat quantities and repartition.

Along these two curves, three distinct behaviors can be identified. First, a dome-shaped profile extends across the heater width. Within the heater, heat fluxes are strongest near the sides, causing the central region to reach higher temperatures, while heat is evacuated more rapidly as the lines approach the edges. Across the full width of the heater, temperatures at the top of the PCM are slightly lower than within the heater, reflecting the horizontal heat extraction from the heater toward the switch sides, which reduces the amount of heat transmitted upward to the PCM. Second, along the sections of the lines extending from the heater extremities to the edges of the AlN layer —crossing the SiO_2 layer for the red line and following the SiO_2-AlN boundary for the green line— the temperature continues to decrease. Initially, the drop is steep, then progressively slows toward the switch sides. Heat flux analysis indicates that in this zone, heat is evacuated from the heater edges toward the AlN extremities. Consequently, regions just beyond the heater exhibit rapid heat loss, explaining the steep initial temperature decline. Viewed from the opposite direction, starting near the switch sides, the lines initially encounter little heat, resulting in low temperatures; approaching the heater, the lines encounter the concentrated heat flowing from the heater edges, producing a sharp, nearly exponential temperature increase. Finally, comparing the green and red curves reveals that temperatures at the top PCM extremities exceed those of the corresponding SiO_2 regions. This is due to heat accumulation at the AlN extremities during evacuation, which partially blocks heat flow. The difference arises because heat is simultaneously drained through the SiO_2 layer (sampled by the red line) while accumulating above the top PCM (sampled by the green line).

The remaining portions of the green and red lines, extending from the AlN extremities toward the switch sides, exhibit similar behavior to that observed along the blue line at the PCM bottom. Heat is rapidly evacuated near the AlN extremities toward the RF contacts, and as the lines progress toward the switch edges, a small fraction of heat flows through the SiO_2 layer toward the top of the switch, slowing the temperature decrease in these regions. Across these zones, direct comparison of the curves indicates that the highest temperatures are observed in the blue line (PCM bottom), followed by the green line (PCM top), and finally the red line (heater mid-height). This ordering is consistent with expectations, as the boundary between the RF contacts and SiO_2 layer vertically captures heat from the surrounding SiO_2, influencing the thermal profile in this region.

3.5.1.2 Comparison with larger heaters

3.5.1.2.1 Bottom of the PCM

Extending the analysis from the 1 µm-wide heater to larger heater widths allows us to assess how heater size influences the thermal behavior at the PCM bottom. Across all heater widths, the temperature profiles along the blue observation lines exhibit qualitatively similar behaviors. This consistency arises because these lines are in direct contact with the RF contacts, which dominate heat extraction, thereby limiting the impact of heater width on the overall profile. Although the general trends remain unchanged, the absolute temperatures in regions between the RF_{gap} and the PCM extremities vary with heater width, with larger heaters producing higher temperatures in these areas. This occurs because the corresponding heat fluxes are directed toward the switch center, becoming more intense in the RF_{gap} region for larger heaters. Consequently, more heat is delivered to these zones, raising the local temperature without altering the overall shape of the temperature profile along the observation line.

3.5.1.2.2 Top of the PCM and mid-height of the heater

Building on the analysis of the PCM bottom for larger heaters, attention now shifts to the thermal behavior along the observation lines crossing the top of the PCM and the mid-height of the heater. Here, the impact of heater width becomes more pronounced. As heaters become wider, the dome-shaped temperature profile observed in narrower heaters gradually transforms into a well-like pattern. This change occurs because, while the heater width increases, the dimensions of the AlN layer and the PCM layer remain constant. In the case of the 2 µm-wide heater shown in Figure 3-12.b , its width nearly matches that of the AlN layer and the PCM layer, resulting in a slight dome in the temperature profile. Heat flux analysis shows more homogeneous heat evacuation than in the 1 µm heater scenario, with vertical heat transport at the heater center becoming more significant. Consequently, the overall direction of heat flux in the switch shifts toward the vertical: whereas in the 1 µm heater the heat largely flowed along the RF contact surfaces, in this wider heater case, heat penetrates more effectively toward the bottom of the RF contacts and the substrate. This enhances heating of the central PCM region, although the peak temperature at the center of the heater is slightly lower for wider heaters. Despite this, heat evacuation remains rapid at the heater extremities, preserving the dome-like shape observed in the graph. Moreover, because the heater width nearly equals the PCM length and the AlN width, the temperatures along the green observation line (crossing the top of the PCM) closely match those along the red line (crossing the heater at mid-height). This convergence is evident in the associated graph, where the red and green curves nearly overlap.

Then, looking at the 3 µm-wide heater case in Figure 3-12.c, the well shape starts appearing along both the heater's width and the top of the PCM's length. This time, the heater is wider than the AlN layer is, with the extremities of the heaters placed above the thermally isolating SiO_2 layer. Consequently, the heat is accumulating at the extremities of the heater. When looking at the heat fluxes, the

behaviors are quite different than the previous cases; the heat generated at the extremities can be seen being mostly drained by the AlN layer, flowing toward it and quickly entering it at its extremities in a more vertical way, while another small part in directly directed toward the RF contacts through the SiO_2 layer. As a result, the red curve in the associated graph shows tiny dome shapes at the extremities of the heater. Along the portions of the red observation line passing through the SiO_2, the temperature initially drops very rapidly before the rate of decrease slows toward the switch edges. This initial sharp decline is more pronounced than in the 1 µm heater scenario. In that case, the AlN layer beneath the adjacent SiO_2 facilitated horizontal heat spreading, moderating the temperature drop along the observation line. In contrast, for the 3 µm (and 4 µm) heaters, the SiO_2 regions next to the heater no longer overlie AlN. Consequently, heat is less able to spread horizontally and is directed more vertically toward the switch, producing a faster temperature decrease along the red observation line, as seen in Figure 3-12.c and Figure 3-12.d.

The most pronounced differences are observed along the green curve. In the segments corresponding to portions of the green observation line passing through the SiO_2 layers beneath portions of the heater, the temperature initially decreases rapidly nsear the AlN layer, then the rate of temperature drop slows progressively as the line extends toward the sides of the switch. The initial steep decline results from the proximity of the AlN layer, which generates a strong heat flux directed toward the RF contacts. As the observation line moves away from the AlN layer, its influence diminishes, and the heat supplied by the overlying heater begins to accumulate within the SiO_2, causing the temperature decrease to decelerate. The 4 µm-wide heater exhibits similar behavior to the 3 µm case, with all described effects amplified.

3.5.1.3 Conclusion on the shortest RF_{gap}

Taken together, the behaviors observed for heaters of increasing width confirm that very short RF_{gap} pose intrinsic challenges when the heater width is much larger that the RF_{gap} length. In every configuration, the PCM region struggles to reach its melting temperature because of the immediate and intense thermal drainage imposed by the nearby RF contacts. This constant heat extraction forces the application of relatively high voltages, as shown in Figure 3-10. Figure 3-13 again presents the evolution of voltage, energy consumption, and maximum heater temperature for the 1 µm- and 4 µm-wide heaters, with the data points corresponding to the shortest RF_{gap} highlighted by dotted rectangles.

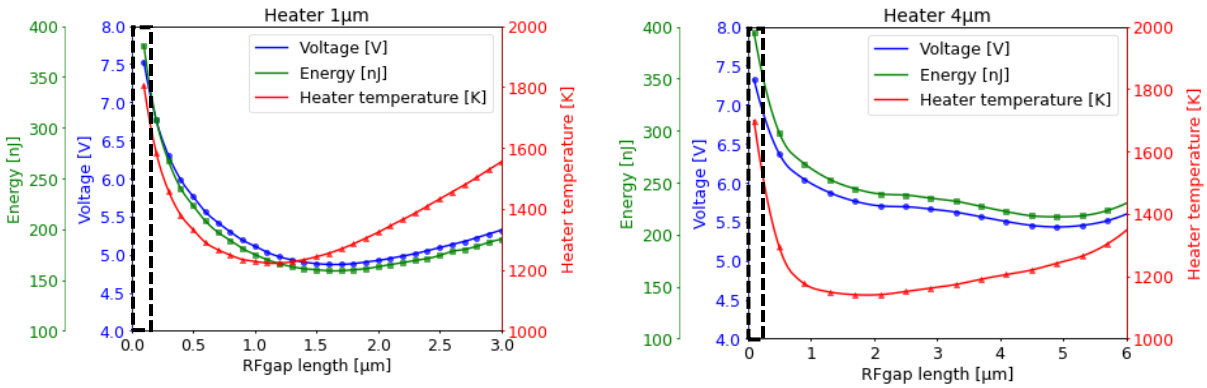


Figure 3-13 : *Voltages applied to the heater (blue), energy consumed (green), and maximum heater temperature (red) for switches with different heater widths, indicated in each graph title. The dotted black rectangles indicate the shortest RF_{gap}, studied in this section. The applied voltages and resulting energy consumptions are high to compensate for the rapid heat loss caused by the RF contacts being closely spaced, which quickly drain heat from the narrow PCM during the heating step.*

The 1 µm heater —covering only a small surface area and losing heat rapidly to the underlying AlN— requires 7.53 V and consumes 381 nJ, while the 4 µm heater —with its larger tungsten mass to heat— demands 7.32 V and consumes 394 nJ. These high voltage and energy requirements, combined with the elevated heater temperatures that threaten long-term reliability, make very short RF_{gap} a particularly unfavorable design choice, ultimately compromising the efficiency and robustness of the switches.
Having established these limitations, the study now turns to the effects of gradually lengthening the RF_{gap}. This progression sheds light on how extending the separation between RF contacts alters the PCM heating dynamics and the overall thermal balance of the device.

3.5.2 RF_{gap} lengthening and PCM maximum temperature increase

Having established that very short RF_{gap} impose severe thermal and reliability constraints across all heater widths, the analysis now turns to the effect of progressively lengthening the RF_{gap}. Starting from the shortest configurations, increasing the RF_{gap} initially raises the temperature at the center of the PCM bottom for all models, before leading to a slight decline once a certain RF_{gap} length is reached. This section explores the evolution of these distinct regimes, with Figure 3-14 illustrating each switch model at the RF_{gap} lengths corresponding to the end of these two phases.

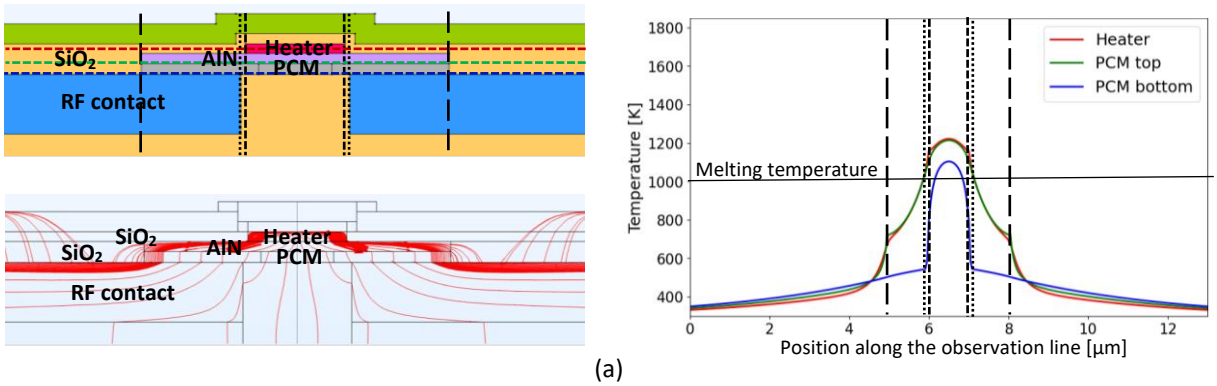
3.5.2.1 1 µm-wide heater

3.5.2.1.1 Bottom of the PCM

Following the general trend identified in the previous paragraph, attention now focuses on the 1 µm-wide heater to illustrate how the central PCM-bottom temperature evolves as the RF_{gap} is increased. In this model, the central temperature rises as the RF_{gap} lengthens up to ≈ 0.5 µm; beyond that point it begins to decline slightly, reaching the values reported at 1.1 µm in Figure 3-14.a. Two factors account for this behavior. First, even when the RF_{gap} is extended to 0.5 µm it remains relatively narrow, so the RF contacts continue to exert a strong influence on heat evacuation. The heater therefore must still supply substantial heat to offset this rapid drainage. Second, enlarging the melted region increases the contrast between the lateral portions —close to the RF contacts and only marginally reaching the melting point— and the central portion, which lies above the thermally isolating SiO_2 and accumulates heat more effectively. As a result, the center attains temperatures ≈ 10 % higher than in the 0.1 µm RF_{gap} case. The combination of sustained heat generation and faster central accumulation explains the initial rise in central PCM-bottom temperature.

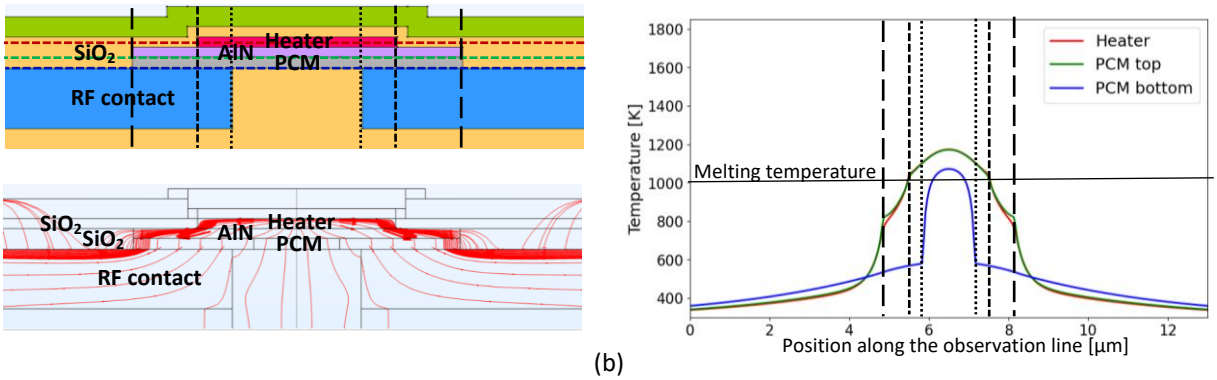
Beyond this point, up to an RF_{gap} of 1.1 µm, the central temperature begins to decrease slightly. At these lengths, the RF contacts are sufficiently spaced apart to reduce the amount of heat required to melt two-thirds of the PCM above the RF_{gap}. As a result, the heater operates at lower temperatures, leading to a modest reduction in central heat accumulation. Figure 3-14.a illustrates this situation for a 1 µm-wide heater with a 1.1 µm-long RF_{gap}: the central PCM bottom remains hotter than in the 0.1 µm case, but the trend has begun to reverse. Considering the entire PCM bottom across the RF_{gap}, not only the melted region, the temperature difference between the center and the RF_{gap} extremities becomes more pronounced than in the 0.1 µm configuration. The increased distance between the melted-zone boundaries and the RF_{gap} edges accentuates this contrast, producing a more visible thermal gradient along the blue observation line.

W_h = 1 µm ; L_{RFgap} = 1.1 µm



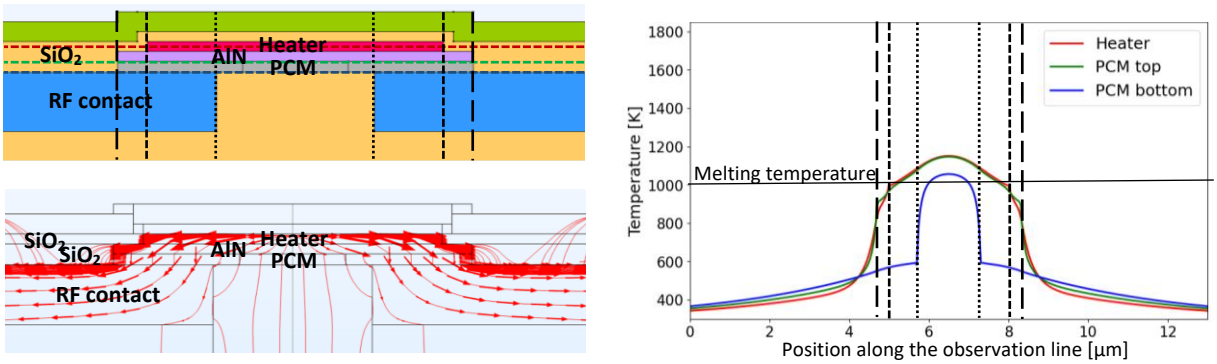
(a)

W_h = 2 µm ; L_{RFgap} = 1.3 µm



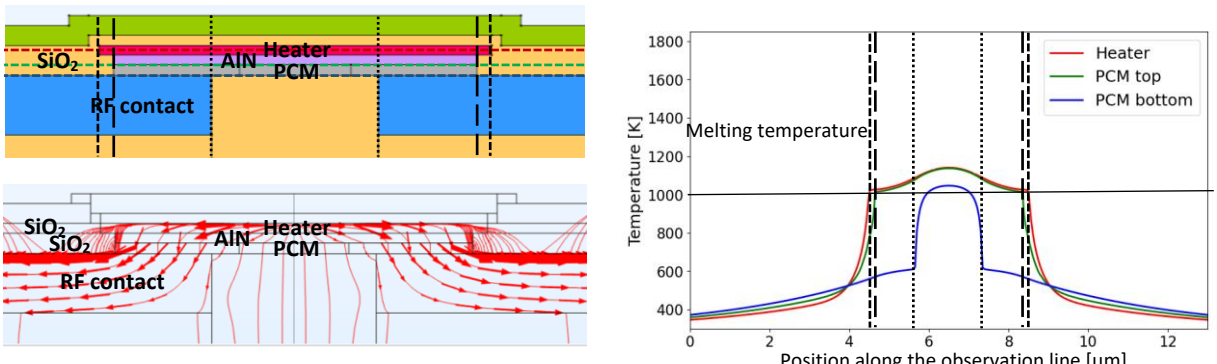
(b)

W_h = 3 µm ; L_{RFgap} = 1.6 µm



(c)

W_h = 4 µm ; L_{RFgap} = 1.7 µm



(d)

Figure 3-14 : *Temperature profiles along the observation lines defined in Figure 3-11, shown for switches with an RF_{gap} length at which the slight rise/decay phases of the PCM bottom temperature are completed, using heater widths of (a) 1 µm, (b) 2 µm, (c) 3 µm, and (d) 4 µm. The right-hand plots display the temperatures recorded along the observation lines. Vertical black lines indicate the width and length of the different switch elements, with their positions referenced on the corresponding designs shown on the left. The heat fluxes illustrated in the schematics correspond to the same time point at which the temperature profiles were extracted.*

Extending the analysis to the overall temperature profile along the blue observation line, the behavior remains closely aligned with that observed in the 0.1 µm RF_{gap} case. A pronounced dome shape appears above the RF_{gap}, followed by a smaller dome extending toward the PCM extremities; beyond these regions, the temperature continues to decline as the line approaches the switch edges, though with a progressively slower rate.

The underlying mechanisms are consistent with those described in the shortest RF_{gap} scenario: rapid drainage imposed by the RF contacts near the RF_{gap} edges, coupled with stronger heat accumulation in the central zone above the SiO_2. Correspondingly, the heat fluxes display the same patterns, with particularly strong lateral fluxes concentrated at the PCM extremities.

3.5.2.1.2 Top of the PCM and mid-height of the heater

Building on the observations made for the PCM bottom, the most significant changes with increasing RF_{gap} length are found in the heater temperatures themselves. Although heat generation must still remain substantial due to the proximity of the RF contacts, heating the PCM becomes considerably easier compared to the 0.1 µm RF_{gap} case. The extremities of the melt zone are now farther from the RF contacts, reducing the intensity of heat drainage, while the PCM center continues to benefit from efficient accumulation above the thermally isolating SiO_2. Consequently, the heater no longer needs to operate at such elevated levels to bring two-thirds of the PCM to its melting point. As a result, the maximum heater temperature decreases by roughly one-third, with the top of the PCM —closely following the heater behavior— showing a similar reduction

Regarding the temperature profiles along the red and green observation lines, their overall evolution remains similar to that of the 0.1 µm case. Heat fluxes are still directed laterally through the conductive layers before being channeled vertically, along the boundaries these layers share with SiO_2, into the underlying layers. However, one key difference emerges: in Figure 3-14.a, the green curve (top of the PCM) is now superimposed on the red curve (heater mid-height) across the heater width. In the 0.1 µm RF_{gap} scenario, the PCM in this region was positioned directly above the RF contacts, leading to stronger vertical drainage and a lower top-PCM temperature. In contrast, with the 1.1 µm RF_{gap}, this zone now lies entirely above SiO_2, allowing heat to accumulate more effectively and equalizing the temperatures between the heater mid-height and the PCM top.

3.5.2.2 Comparison with larger heaters

3.5.2.2.1 Bottom of the PCM

After examining the 1 µm-wide heater, it is instructive to compare its behavior with that of wider heaters. Among the key differences visible in Figure 3-14, the maximum temperature reached at the bottom of the PCM is systematically lower for larger heaters. This results from the fact that the RF_{gap} length at which the slight decline in PCM-bottom temperature ends shifts toward higher values as the heater width increases (a phenomenon analyzed in more detail in Section 3.5.4). Consequently, for wider heaters, this transition point occurs at longer RF_{gap}, which promotes heat accumulation in the PCM center. This effect can be clearly understood by examining the heat flux distributions in Figure **3-14**. In the case of narrow heaters, there is a stark contrast between the lateral fluxes evacuating heat through the RF contact surfaces and the much weaker vertical fluxes crossing the PCM bottom, with the latter being nearly negligible. By contrast, wider heaters exhibit more pronounced vertical fluxes through the PCM center, owing to the combination of longer RF_{gap} and a heater footprint that covers —or nearly covers— the entire PCM length. This configuration favors a more homogeneous heat distribution across the PCM.

As a result, the maximum temperature reached at the PCM bottom decreases with heater width. For instance, when comparing the respective RF_{gap} lengths that mark the end of the slight decline in PCM-bottom temperature, the 4 µm-wide heater reaches a maximum temperature about 5 % lower than that of the 1 µm-wide heater.

3.5.2.2.2 Top of the PCM and mid-height of the heater

Moving from the bottom of the PCM to the heater and the PCM top, the influence of heater width becomes even more apparent through the evolution of the heat fluxes. For the 3 µm and 4 µm-wide heaters with 0.1 µm-long RF_{gap}, heat fluxes were previously seen originating at the heater extremities and directed inward toward the switch center. By contrast, as shown in Figure 3-14.c and Figure 3-14.d, these wider heaters now exhibit fluxes that emerge from the heater center and spread outward toward the sides of the switch. This change makes it more difficult to heat the central region of the PCM bottom.

As already noted in Figure 3-12, the larger heaters display more homogeneous fluxes overall, which equalize the heat distribution inside the switch and reduce the temperature differences between its center and sides. This homogenization is reflected not only at the PCM bottom but also within the heaters and at the PCM tops, where noticeable temperature variations appear across the different switch models. For instance, the maximum temperature reached in these regions decreases by about 6.5 % for the 4 µm-wide heater compared to the 1 µm-wide case. Another striking difference highlighted in Figure 3-14 is that the 3 µm and 4 µm heaters no longer exhibit hotter extremities than centers. In line with the heat flux behavior described in the previous section (Section 3.5.2.2.1), heat is now evacuated more rapidly at the extremities than at the heater center. As a result, these larger heaters behave similarly to narrower ones: the central region must reach higher temperatures to ensure that sufficient heat is delivered to the PCM extremities. This behavior is clearly visible in the graphs of Figure 3-14.c and Figure 3-14.d, where the green curves (PCM top) nearly superpose the red ones (heater mid-height), particularly in the zones between the RF_{gap} and the PCM extremities.

In the 3 µm case, where the heater remains slightly narrower than the underlying AlN layer, the PCM top extremities reach slightly higher temperatures than the heater. As explained in the previous section, this effect arises from localized heat accumulation at the AlN extremities, where the evacuation flux encounters the adjacent SiO_2. Conversely, in the 4 µm case, where the heater slightly overhangs the AlN and extends above small portions of SiO_2, heat accumulates directly at the heater extremities. This configuration elevates the local temperature at these points, distinguishing the 4 µm heater behavior from that of the 3 µm one.

3.5.2.3 Conclusion

The initial increase in RF_{gap} length introduces a marked difference between the center of the PCM, which begins to accumulate heat more effectively and is less influenced by the RF contacts, and the extremities of the zones to be melted, which remain close to the RF contacts. This enhanced heat accumulation reduces the voltage required for effective PCM heating, as illustrated in Figure 3-10. Figure 3-15 again presents the evolution of voltage, energy consumption, and maximum heater temperature for the 1 µm- and 4 µm-wide heaters, with the data points corresponding to the RF_{gap} length studied in this section, highlighted by dotted rectangles. A 1 µm-wide heater paired with a 1.1 µm-long RF_{gap} sees its required voltage drop by one third compared to when it was paired with a 0.1 µm RF_{gap}, decreasing from 7.53 V to 5.03 V. The corresponding energy consumption decreases even more substantially, falling by 53.5 % from 381 nJ to 170 nJ. Similar trends are observed for wider heaters; for example, a 4 µm-wide heater combined with a 1.7 µm-long RF_{gap} requires only 5.76 V, compared to 7.32 V when paired with a 0.1 µm RF_{gap}, while its energy consumption drops from 394 nJ

to 244 nJ. Overall, this reduction in both voltage and energy lowers heater temperatures, thereby improving the reliability of the device.

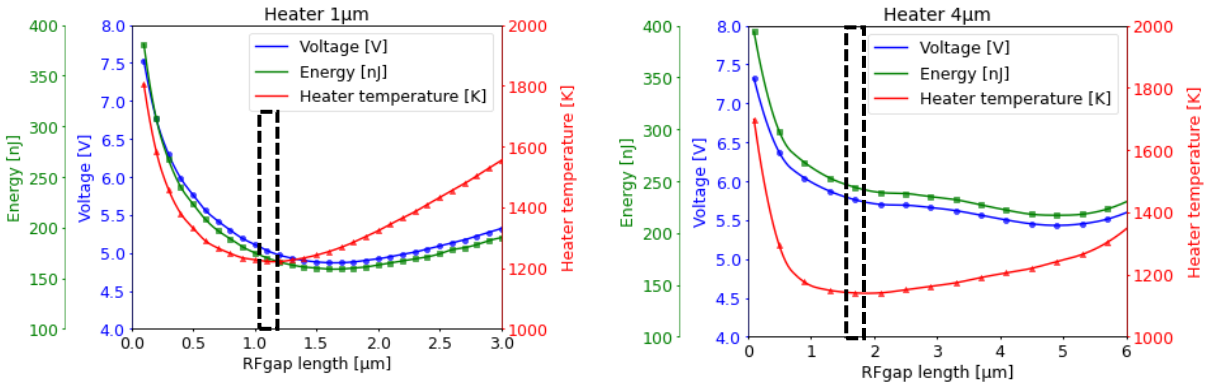


Figure 3-15 : *Voltages applied to the heater (blue), energy consumed (green), and maximum heater temperature (red) for switches with different heater widths, indicated in each graph title. The dotted black rectangles indicate the RF_{gap} lengths studied in this section. The maximum heater temperature decreases from the shortest RF_{gap} up to these points, then rises again to sufficiently heat the extremities of the lengthening PCM.*

Building on this understanding, attention now turns to the SiO_2 layers neighboring the widest heaters. As the RF_{gap} continues to increase, these regions exhibit a distinct change in their temperature evolution, marking the onset of a new phase in the device's thermal behavior.

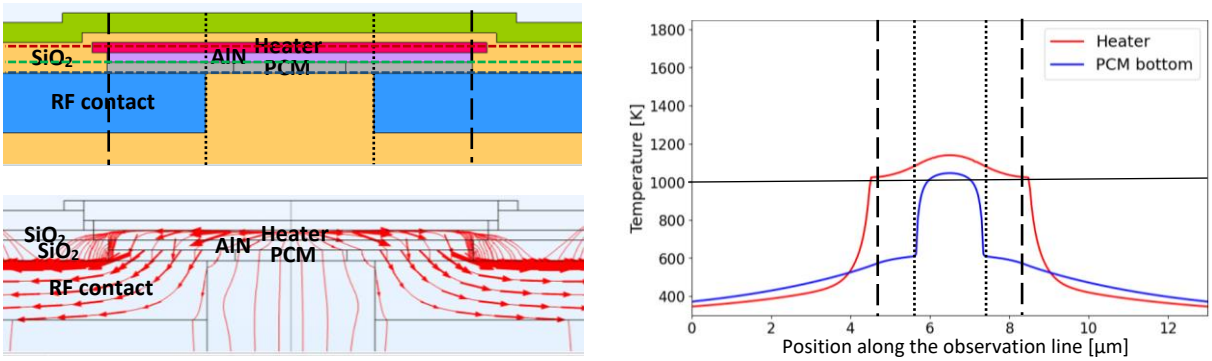
3.5.3 Emergence of dual-phase thermal behavior in SiO_2 regions with PCM and AlN dielectrics longer than heater's width.

Building on the trends identified in Section 3.5.2, where heater width and RF_{gap} length were shown to strongly affect heat flux distributions, an additional change appears when the RF_{gap} continues to lengthen in the cases of the 3 µm and 4 µm-wide heaters. This change is most clearly illustrated for the 4 µm heater in Figure 3-16. Up to an RF_{gap} length of 1.7 µm, the temperature evolution along the red observation line located in the SiO_2 regions exhibits a single, consistent behavior. As explained in Section 3.5.1.2.2, the absence of AlN underneath the SiO_2 adjacent to the heater forces the heat fluxes to evacuate vertically toward the RF contacts. In the corresponding graph for the 1.7 µm RF_{gap} (Figure 3-16.a), the red curve shows a steep temperature drop immediately at the heater outlet, followed by a progressively slower decline as the observation line extends toward the switch sides. However, at the next simulated RF_{gap} length of 2.1 µm, an important structural change occurs: the AlN and PCM layers become, respectively, wider and longer than the heater. In this configuration, the thermal behavior at the heater extremities changes markedly. As seen in Figure 3-16.b, part of the heat extracted from the heater edges now flows into the AlN extremities, while another part is drained through the adjacent SiO_2. This mixed pathway results in the temperatures near the heater edges remaining almost constant, as reflected in the red curve of the corresponding graph.

The heat fluxes at this RF_{gap} length confirms the transition. Heat is rapidly drained at the heater extremities, but most of it flows through the AlN, briefly crossing the short distance to its edges before being directed vertically into the RF contacts through the PCM. From this point onward, the temperature evolution in the SiO_2 regions splits into two distinct phases. The first phase occurs in the SiO_2 portions still located above AlN, where the red curve shows an initial sharp temperature drop due to vertical drainage into the AlN, followed by a slower decrease as the observation line advances toward the switch sides. The second phase begins when the observation line enters SiO_2 regions no longer supported by AlN; here, the temperature again decreases steeply at first, due to strong vertical

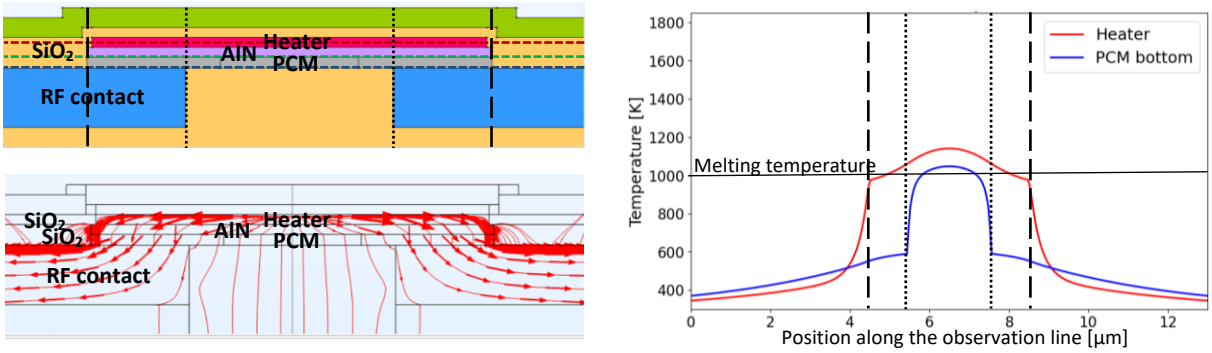
evacuation directly into the RF contacts, before gradually slowing as the line approaches the switch extremities and moves away from concentrated heat fluxes.

W_h = 4 µm ; L_{RFgap} = 1.7 µm



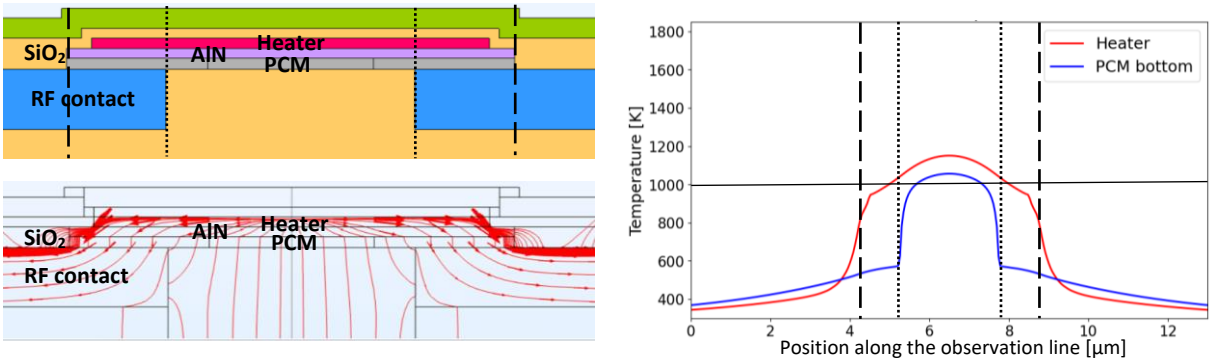
(a)

W_h = 4 µm ; L_{RFgap} = 2.1 µm



(b)

W_h = 4 µm ; L_{RFgap} = 2.5 µm



(c)

Figure 3-16 : *Temperature profiles along the red and blue observation lines defined in Figure 3-11 for the switch with a 4 µm-wide heater. RF_{gap} lengths were selected to highlight how temperature evolution changes with increasing RF_{gap} length. The right-hand plots display the temperatures recorded along the observation lines. Vertical black lines indicate the width and length of the different switch elements, with their positions referenced on the corresponding designs shown on the left. The heat fluxes illustrated in the schematics correspond to the same time point at which the temperature profiles were extracted.*

This separation between the two phases becomes even more visible at an RF_{gap} of 2.5 µm, where the AlN and PCM dimensions extend further beyond the heater width. At the same time, the heat fluxes within the RF contacts undergo a redistribution: they weaken in the vertical direction and concentrate

primarily near the surface, reflecting the increasingly horizontal entry of heat into the contacts and the reduced vertical penetration compared to shorter RF_{gap}.

Conclusion

As the RF_{gap} continues to lengthen, a new mechanism emerges in the switch with a 4 µm-wide heater. Because the PCM and AlN layers now extend beyond the heater's width, the thermal behavior in the adjacent SiO_2 regions changes significantly. The temperature evolution within these zones splits into two distinct phases, accompanied by a redirection of the heat fluxes. Whereas in shorter RF_{gap} the heat from the SiO_2 next to the heater flowed directly and vertically into the RF contacts, it must now cross both the AlN and PCM layers. This temporarily redirects part of the heat horizontally, delaying its evacuation. As a consequence, heat accumulation within the PCM is altered: the extremities of the melting zone progressively shift under the thermally isolating SiO_2, making them more difficult to heat than when they remained directly beneath the heater.

Recognizing these evolving heat pathways and their influence on temperature distributions provides the foundation for understanding why the PCM bottom temperature eventually rises again, and how this phenomenon links to the trends in applied voltage and energy consumption examined in the next section.

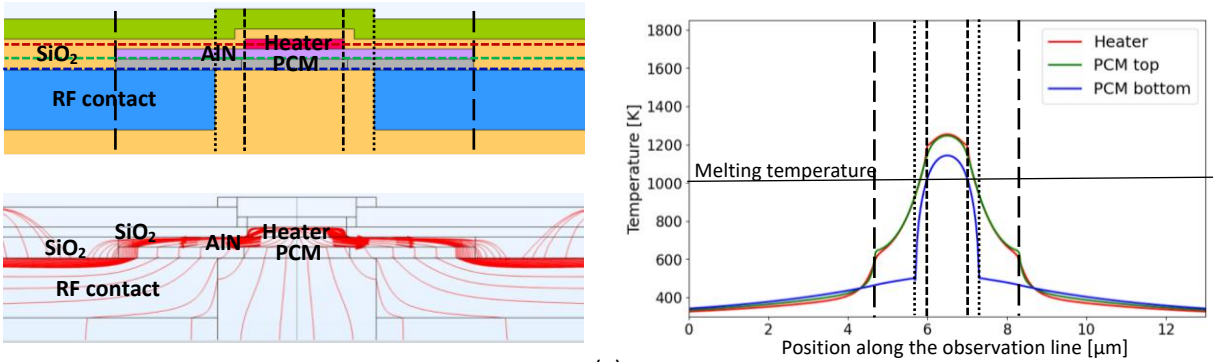
3.5.4 Change in the temperature evolution shape along the bottom of the PCM and impact of the tendencies of the voltage and energy consumption evolutions.

Building on the previous analysis of how the RF_{gap} length and heater width influence heat distribution, the focus now shifts to how these parameters affect the overall temperature profile along the bottom of the PCM. In particular, it is important to understand the evolution of the PCM bottom temperature once the slight decrease phase has concluded, and how this evolution drives the tendencies in voltage and energy consumption for different heater geometries. As discussed in Section 3.5.2.2.1, the RF_{gap} length at which the slight decrease in temperature at the center of the PCM bottom ends is higher for wider heaters. To understand this behavior, it is instructive to consider what happens when the RF_{gap} continues to increase beyond this point.

Once the slight temperature decrease phase concludes, further extending the RF_{gap} causes the temperature at the PCM bottom center to rise again. This increase occurs because the extremities of the zone to be melted move further away from the PCM center, where heat accumulation is most effective. At the same time, these extremities remain close to the RF contacts, which continue to extract heat efficiently, making it increasingly difficult for them to reach the melting temperature. As a result, the central PCM region must reach higher temperatures to compensate for insufficient heat at the extremities.

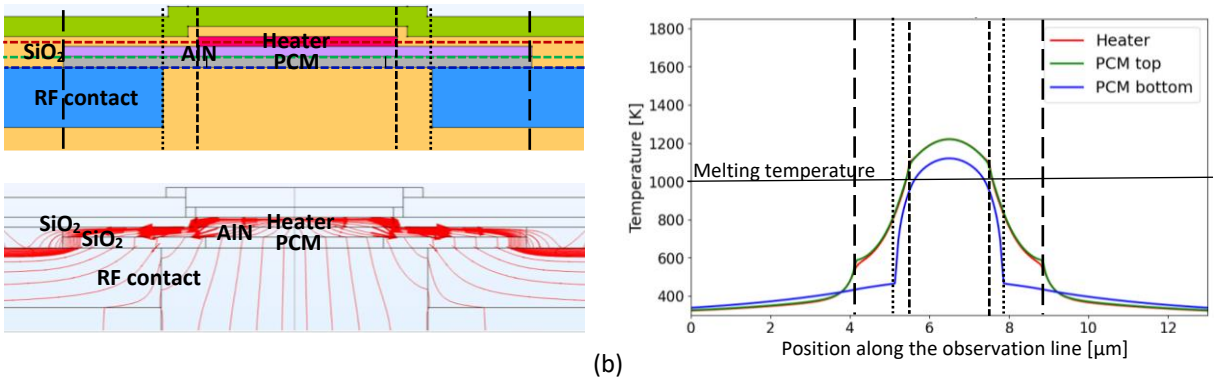
The RF_{gap} length at which this temperature increase begins (i.e., the point immediately following the slight temperature decrease) is larger for wider heaters. This is because wider heaters cover a greater portion of the PCM, allowing them to supply sufficient heat to the extremities of the melt zone over a longer RF_{gap}. In other words, at the RF_{gap} length where the 1 µm heater requires the center of the PCM to heat further, a 4 µm heater can still maintain adequate heat at the extremities without needing as much central temperature rise. This behavior directly influences the voltage and energy consumption trends: as the center of the PCM must reach higher temperatures, the applied voltage and energy input must increase correspondingly. Conversely, for wider heaters, the extended coverage mitigates this effect, delaying the onset of higher voltage and energy requirements as the RF_{gap} length grows.

W_h = 1 µm ; L_{RFgap} = 1.6 µm



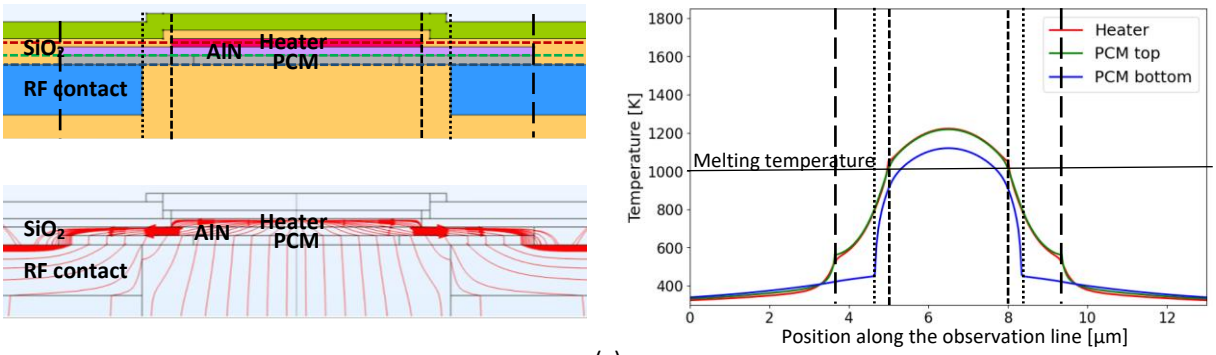
(a)

W_h = 2 µm ; L_{RFgap} = 2.7 µm



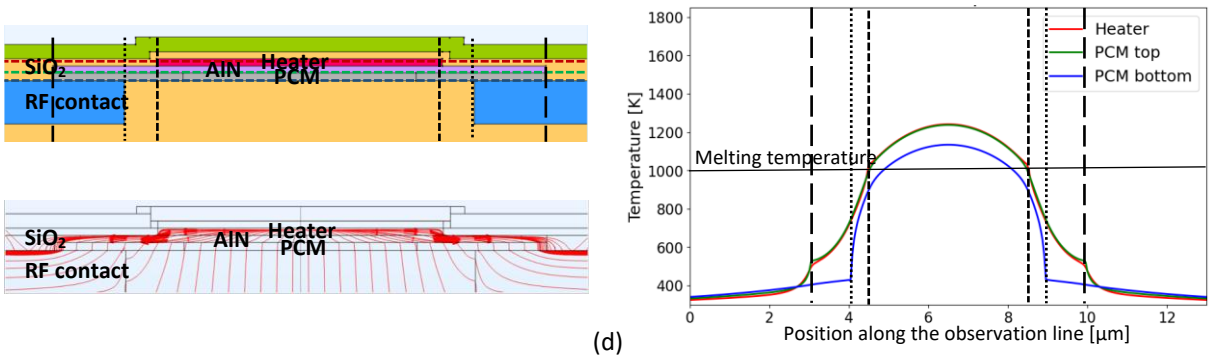
(b)

W_h = 3 µm ; L_{RFgap} = 3.7 µm



(c)

W_h = 4 µm ; L_{RFgap} = 4.9 µm



(d)

Figure 3-17 : *Temperature profiles along the observation lines defined in Figure 3-11 for switches with RF_{gap} lengths optimized for applied voltage and energy consumption, using heater widths of (a) 1 µm, (b) 2 µm, (c) 3 µm, and (d) 4 µm. The right-hand plots display the temperatures recorded along the observation lines. Vertical black lines indicate the width and length of the different switch elements, with their positions referenced on the corresponding designs shown on the left. The heat fluxes illustrated in the schematics correspond to the same time point at which the temperature profiles were extracted.*

Now, considering the mechanisms by which the temperature at the center of the PCM bottom can increase again along the RF_{gap} sweep, two distinct processes are at play. For the first few RF_{gap} lengths beyond 1.1 µm, the extremities of the melting zone reach the melting temperature by leveraging two factors. First, they still benefit from the heat accumulation facilitated by the increasing distance of the RF contacts. Second, the applied heater voltages continue to decrease, but very gradually, remaining nearly constant across these RF_{gap} lengths. This allows the heater itself to exploit the easier heat accumulation at the center of the switch, gradually raising its temperature as the RF_{gap} extends. However, at an RF_{gap} length of 1.6 µm, a notable change occurs. The temperatures observed along the blue observation line at the PCM bottom —specifically between the extremities of the heater and the edges of the RF_{gap}— approach those recorded along the red observation line in the corresponding SiO_2 regions next to the heater. This shift arises because, whereas previously these zones contained PCM with RF contacts beneath them, they now include PCM with a significant portion of SiO_2 from the RF_{gap} underneath. Consequently, in these sections of the blue observation line, heat begins to accumulate more effectively, causing the temperature to rise rapidly. During this phase, the SiO_2 located at the outlets of the heater still overlies the AlN, which continues to drain heat efficiently. As a result, the temperatures along the blue line in this region converge toward those along the red line, reflecting the combined effects of heat accumulation in the PCM and ongoing heat extraction from the heater by the AlN.

Figure 3-17.a illustrates the switch using a 1 µm-wide heater with an RF_{gap} of 1.6 µm. It is part of Figure 3-17 where the switches with wider heaters are also shown, along with the corresponding RF_{gap} at which the blue observation line begins to reach temperatures close to those of the heater in the same regions, as described previously. In general, this convergence occurs when the RF_{gap} length exceeds the heater width by approximately 0.6-0.9 µm. This finding confirms that, regardless of whether the PCM zone to be melted is longer or shorter than the heater width (longer for the 1 µm heater, shorter for the wider heaters), the key factor is the presence of SiO_2 beneath the sections of the blue observation line located between the heater extremities and the RF_{gap} edges. This SiO_2 layer allows heat to accumulate, raising the temperatures in these regions close to those of the SiO_2 adjacent to the heaters.

For the temperature at the PCM bottom to increase further as the RF_{gap} continues to lengthen, the SiO_2 regions next to the heater must also warm sufficiently to create “room” for heat accumulation. This is where the second mechanism responsible for the center PCM temperature rise comes into play: the applied heater voltages begin to increase, producing additional heat so that the PCM zones to be melted can reach their melting temperature. As the RF_{gap} length continues to grow, the extremities of the melting zone move progressively farther from the heaters, making them increasingly difficult to heat. Consequently, the voltages are raised in a slightly exponential manner to ensure that the SiO_2 adjacent to the heater reaches sufficiently high temperatures, allowing the PCM extremities to attain the melting temperature.

Conclusion

As the RF_{gap} length increases, two successive mechanisms drive the temperature rise at the bottom of the PCM. In the first stage, the wider spacing between the RF contacts gradually weakens their thermal influence on the PCM. Coupled with nearly constant heater voltages, this allows the PCM’s central region to accumulate heat more efficiently, supporting the melting of the target zone. At longer RF_{gap} lengths, however, the regions adjacent to the heater undergo a structural shift: instead of consisting of SiO_2 directly backed by the RF contacts, they now consist of SiO_2 underlain by the AlN layer. In this configuration, part of the heat is drained through the AlN and redirected into the PCM, which itself benefits from the heat accumulation made easier by the SiO_2 of the RF_{gap}. The interplay between this

drainage and accumulation causes the temperatures of these SiO_2-adjacent regions to converge with those at the PCM bottom. Once this convergence occurs, the melting zone of the PCM, now larger and with extremities further from the heater, requires additional thermal input. Heat accumulation alone no longer suffices, and the applied voltage must begin to rise again, bringing with it higher energy consumption and elevated heater temperatures. This turning point in the RF_{gap} sweep —where the PCM temperatures converge with those of the adjacent SiO_2— corresponds to the minimum in voltage and energy consumption: 4.87 V and 159 nJ for the 1 µm heater, 4.60 V and 167 nJ for the 2 µm heater, 4.94 V and 190 nJ for the 3 µm heater, and 5.43 V and 217 nJ for the 4 µm heater, as shown in Figure 3-18. Moreover, as heater width increases and covers the PCM more effectively, this convergence occurs at progressively larger RF_{gap} lengths, thereby extending the potential size of the amorphized PCM region.

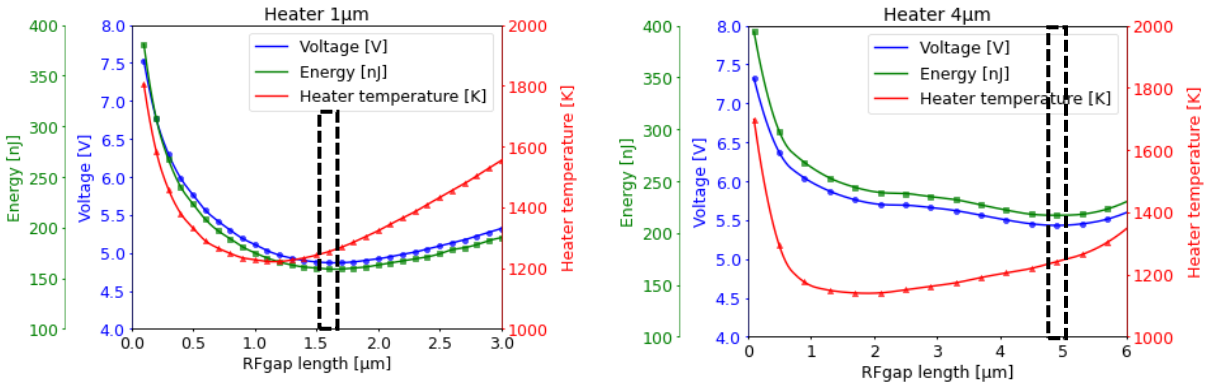


Figure 3-18 : *Voltages applied to the heater (blue), energy consumed (green), and maximum heater temperature (red) for switches with different heater widths, indicated in each graph title. The dotted black rectangles indicate the RF_{gap} lengths studied in this section. The voltages applied and energy consumption can be seen increasing again from these points to sufficiently heat the extremities of the PCM zone to melt.*

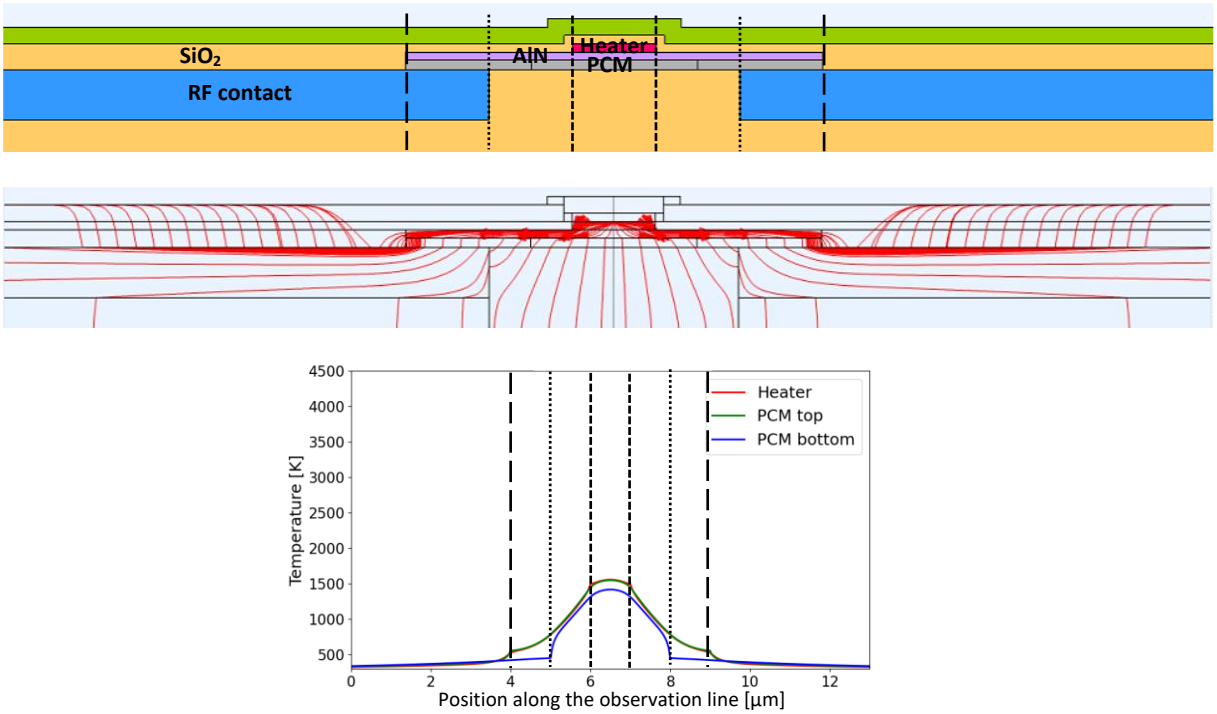
Taken together, these findings provide a clear understanding of how PCM heating dynamics respond to RF_{gap} length and heater width. This sets the stage for examining the end of the RF_{gap} length increase sweeps, where the interplay of extreme RF_{gap} lengths and heater configurations produces pronounced thermal effects throughout the switch, particularly in the PCM and heater components.

3.5.5 End of the RF_{gap} length increase sweep.

Building on the analysis of how the temperature along the bottom of the PCM evolves with increasing RF_{gap} lengths and the associated mechanisms influencing heat distribution, this final section examines the state of each of the four simulated switches at the maximum RF_{gap} length considered for each model. Starting with the switch using a 1 µm-wide heater, which concludes the sweep at a 3 µm-long RF_{gap}, Figure 3-19.a shows that the temperature along the blue observation line —covering the region between the heater extremities and the RF_{gap} extremities— now closely mirrors the temperature profile along the red line in the same zones. This indicates that the bottom of the PCM in these regions is no longer governed primarily by heat accumulation in the PCM itself but instead depends directly on the temperature within the adjacent SiO_2 layer next to the heater.

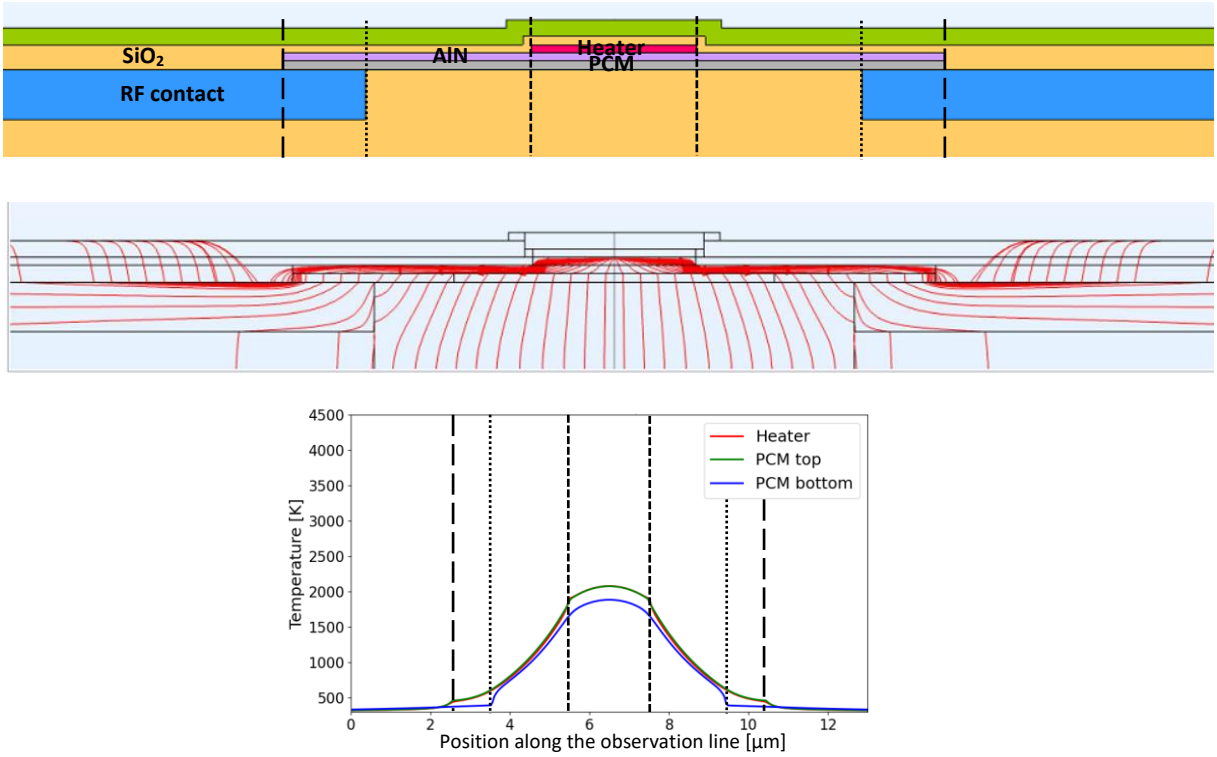
This behavior is consistent across the switches with wider heaters, as illustrated in Figure 3-19. In these cases, the blue curves in the corresponding graphs adopt the same shape as the red curves in the zones between the heater extremities and the RF_{gap} edges. Within these regions, the temperature decrease now occurs more gradually as the observation lines extend away from the heater toward the sides of the switch.

W_h = 1 µm ; L_{RFgap} = 3 µm



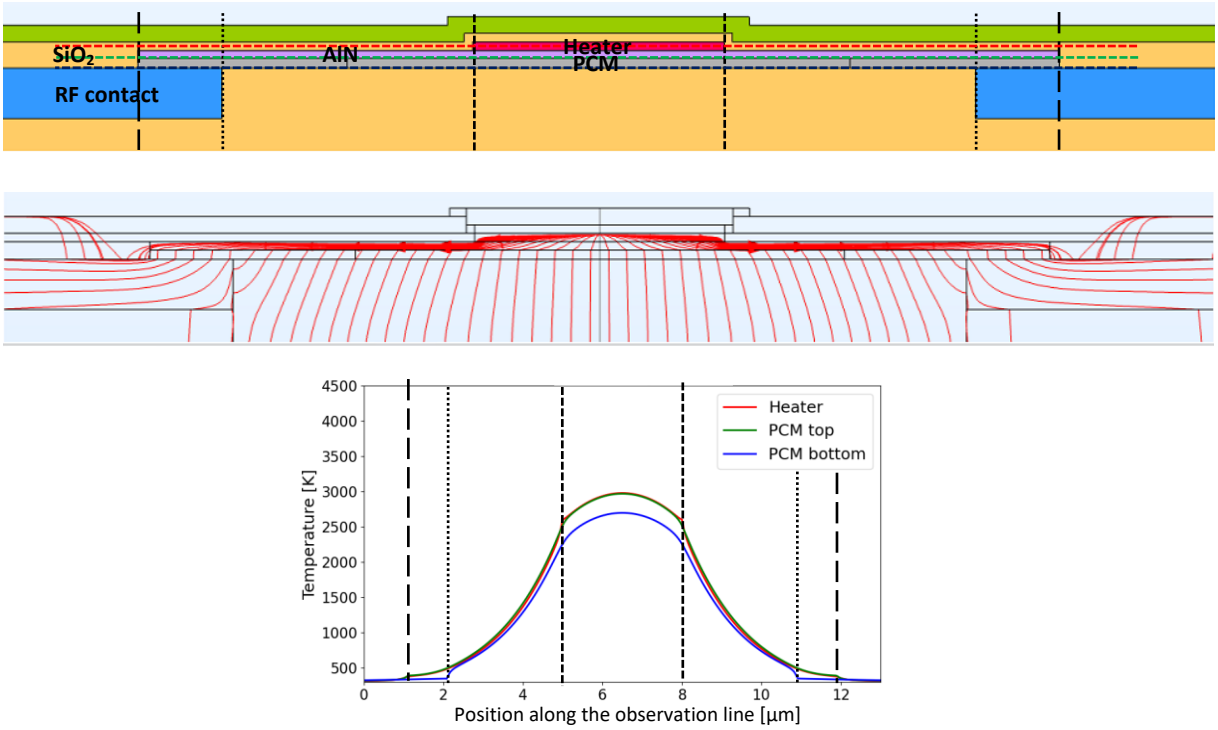
(a)

W_h = 2 µm ; L_{RFgap} = 6 µm



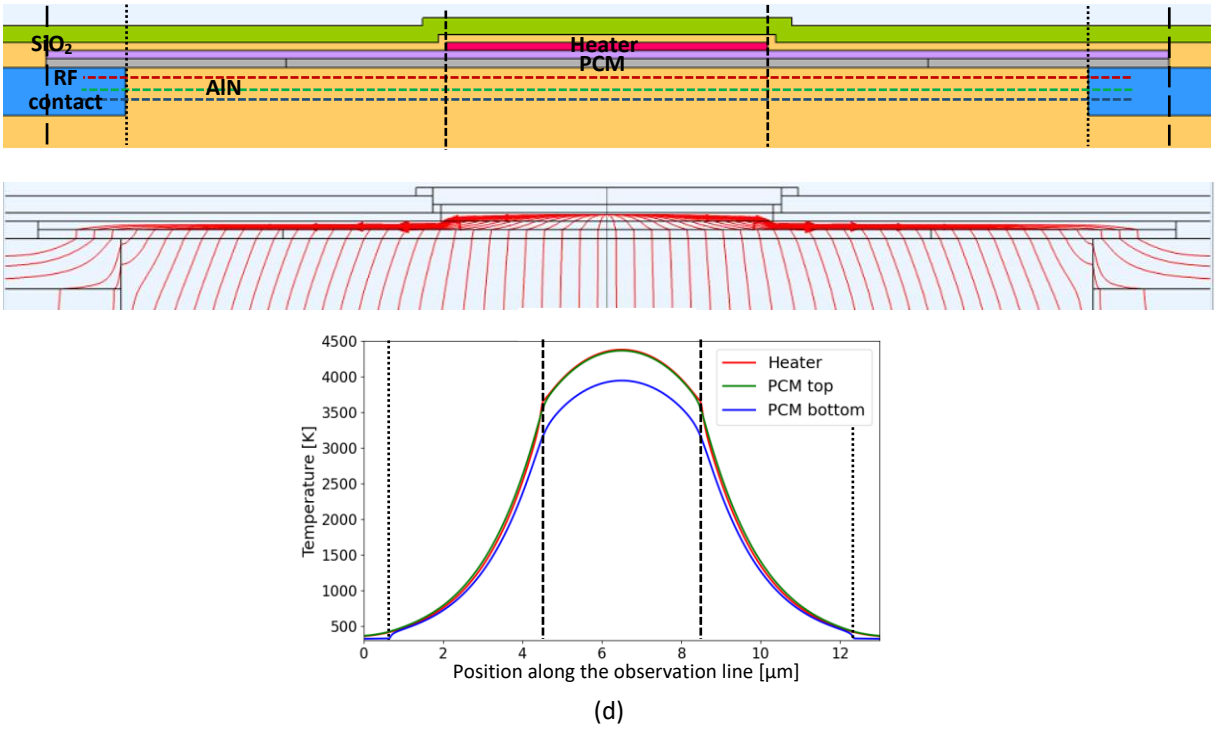
(b)

W_h = 3 µm ; L_{RFgap} = 9 µm



(c)

W_h = 4 µm ; L_{RFgap} = 12 µm



(d)

Figure 3-19: *Temperature profiles along the observation lines defined in Figure 3-11 for switches with the last RFgap length of the RF_{gap} length sweep they have been simulated with, using heaters with widths of (a) 1 µm, (b) 2 µm, (c) 3 µm, and (d) 4 µm. The right-hand plots display the temperatures recorded along the observation lines. Vertical black lines indicate the width and length of the different switch elements, with their positions referenced on the corresponding designs shown on the left. The heat fluxes illustrated in the schematics correspond to the same time point at which the temperature profiles were extracted.*

However, near the RF contacts, the previous behavior is maintained: heat is still extracted more rapidly, producing a sharper temperature drop until the contacts are reached, consistent with observations from the earlier sections. Regarding the heat flux, Figure 3-19.d shows that for the 4 µm-wide heater, with a final RF_{gap} length of 12 µm at the end of the sweep, the flux no longer extends to the extremities of the AlN and PCM layers. Upon reaching the RF contacts, the heat now enters them almost vertically. This change occurs because, as the flux travels through the PCM, it remains concentrated near the top of the PCM rather than following the top of the AlN layer as observed previously or for the other three switches. This behavior can be understood by comparing the relative strengths of the heat fluxes within the RF contacts versus those flowing through the RF_{gap} toward the substrate: the two are now comparable. Consequently, the influence of RF contact heat draining is significantly reduced, owing to the large distance between the PCM melting zone and the RF contacts due to the extended RF_{gap}. As the heat moves along the AlN layer toward the RF contacts, it is progressively drained by the substrate, gradually shifting the flux toward the bottom of the AlN layer. By the time the flux reaches the RF contacts, it is concentrated at their top and enters them directly in a vertical direction, as illustrated in the figure.

Finally, the temperatures reached at the end of the RF_{gap} length increase sweep are extremely high. Figure 3-20 shows that they range from 1553.3 K for the 1 µm-wide heater with a 3 µm RF_{gap} to 4378.1 K for the 4 µm-wide heater with a 4 µm RF_{gap}.

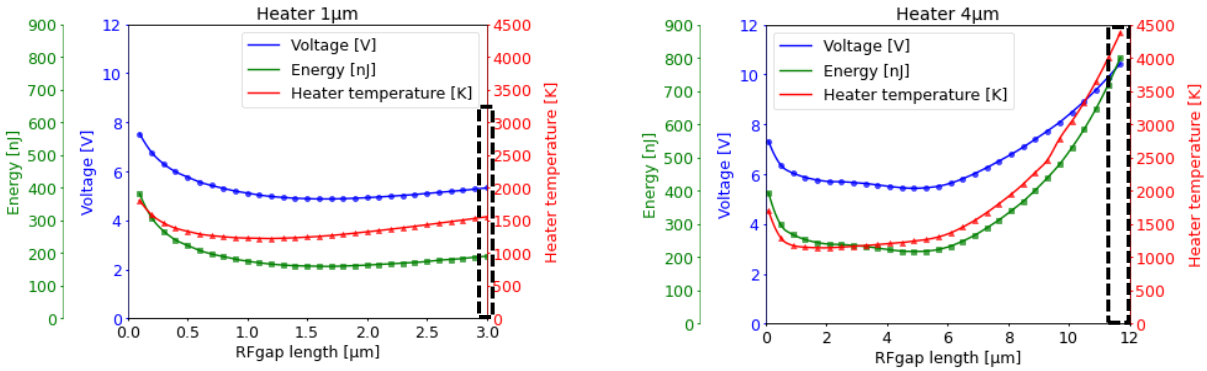


Figure 3-20 : *Voltages applied to the heater (blue), energy consumed (green), and maximum heater temperature (red) for switches with different heater widths, indicated in each graph title. The dotted black rectangles indicate the RF_{gap} lengths studied in this section. The voltages applied and energy consumption can be seen increasing again from these points to sufficiently heat the extremities of the PCM zone to melt.*

In the case of the larger heaters, such extreme temperatures pose a significant risk of damaging the heating element and reducing the overall reliability of the switch. For the bottom of the PCM, temperatures range from 1413.7 K for the 1 µm-wide heater switch to 3944 K for the 4 µm-wide heater switch. These elevated temperatures generate a substantial, unnecessary heat load that must be evacuated during the quench phase, extending the cooling time of the PCM and increasing the likelihood of recrystallization rather than proper amorphization.

Conclusion

The final RF_{gap} length of each sweep reveals how the thermal behavior of the switches ultimately stabilizes. Along the width axis —between the heaters and the RF contacts— the temperature profiles of the SiO_2 regions adjacent to the heater and of the PCM bottom converge, reaching similar values. From this point onward, any further temperature increase in the PCM melting zone depends mainly on the heat supplied by the heater to the neighboring SiO_2 regions. At this stage, the thermal draining effect of the substrate becomes comparable to that of the RF contacts. However, relying on very long RF_{gap}, while enabling the melting of a large PCM volume, introduces two major drawbacks. First, the

higher voltages and energy requirements (e.g., 10.43 V and 800 nJ for the 4 µm heater with a 12 µm RF_{gap} observed in Figure 3-10) drive the heaters to extreme temperatures, threatening their structural integrity. Second, the PCM itself also reaches excessive temperatures, adding large amounts of heat to dissipate during the quench phase. This prolongs cooling, reduces the likelihood of achieving amorphization, and ultimately cancels the benefit of melting a larger PCM region.

Building on the insights of all previous sections, the next one will provide a general conclusion for the entire study, identifying the optimal combination of RF_{gap} length and heater width that achieves a balanced trade-off between efficient PCM heating, energy consumption, and switch reliability.

3.5.6 General conclusions on the association of the RF_{gap} length and the heater's width

The analysis presented in this part of the chapter highlights the contrasting thermal behaviors of the switches depending on the various combinations of RF_{gap} length and heater width, with direct consequences on the maximum temperatures, applied voltages, and energy consumption.

Starting with the shortest tested RF_{gap} (0.1 µm), the results show severe heating issues. The strong thermal draining from the closely spaced RF contacts forces the heater to operate at high voltages, pushing its temperature far above that of the PCM. This compromises the device's reliability and induces excessive energy consumption. In addition, the tiny amount of potentially amorphized PCM would be insufficient to guarantee a robust OFF-state for switches. Together, these drawbacks rule out such short RF_{gap} for practical use. By contrast, the first increments in RF_{gap} length already bring notable improvements. As the RF contacts move further apart, heat accumulates more easily at the center of the PCM. This leads to a reduction in both the required voltage and the energy consumption, while also lowering the heater temperature and improving reliability. At the same time, the volume of amorphizable PCM increases, making these intermediate RF_{gap} far more attractive for integration in PCM-based RF switches.

A particularly important turning point occurs when the RF_{gap} length exceeds the heater width by about 0.6-0.9 µm. At this stage, the direction of the heat fluxes changes, and the temperature of the PCM sections located between the heater and the RF_{gap} extremities becomes governed by the temperatures in the adjacent SiO_2 regions. This configuration systematically corresponds to the lowest applied voltages and energy consumptions observed in the entire sweep, regardless of heater width. Combined with acceptable heater maximum temperatures (1220-1270 K depending on the design), these RF_{gap} emerge as highly promising candidates for optimized switch operation.

However, further lengthening the RF_{gap}, while increasing the amount of PCM that can be melted, comes at the cost of sharply rising resource requirements and higher operating temperatures in all layers of the device. This degrades heater reliability and prolongs the quench process, which in turn raises the risk of PCM recrystallization, undermining the advantage of having a larger melted volume. Thus, the optimal compromise is found by returning to the pivot point where the applied voltage reaches its minimum. This ensures a sufficiently long RF_{gap} for proper amorphization, while avoiding unnecessary energy penalties.

The final task is to determine which heater width should be selected among the four options considered. To this end, the operating requirements of each heater at its optimized RF_{gap} are first compared with the requirements that would arise if the same RF_{gap} length were paired with the other heater widths. The results of this comparative approach are summarized in Table 3-7.

Examining this comparison, two configurations clearly stand out among the four considered. The 2 µm-wide heater with its optimized 2.7 µm-long RF_{gap}, and the 3 µm-wide heater with its optimized 4 µm-

long RF_{gap}, share a common strength: in both cases, assigning another heater width while keeping the same RF_{gap} length systematically increases both required voltage and energy consumption. This observation rules out the 1 µm and 4 µm heaters. For example, in the last line of Table 3-7, choosing the 4 µm heater with its optimized 4.9 µm RF_{gap} would be less efficient than replacing it with the 3 µm heater, which not only lowers the requirements but also reduces parasitic capacitances with the crystalline PCM —thanks to the narrower heater and reduced metal interaction. Further optimization would then naturally bring the RF_{gap} back down to its 4 µm optimum. By contrast, the 2 µm and 3 µm heaters already represent the most efficient widths for their respective optimized RF_{gap} lengths.

Table 3-7: *The first column lists the tested heater widths and their corresponding RF_{gap} lengths that minimize the required voltage and energy consumption (provided as the blue-marked values). For these same RF_{gap} lengths, the voltage and energy consumption obtained with other heater widths are also provided. Green-marked values indicate the optimized heater width-RF_{gap} length combination for PH_{OFF}, selected as the reference for all subsequent simulations in this chapter.*

Heater under evaluation with its ideal RF_{gap} length	Operating requirements for the 1 µm-wide heater at the same RF_{gap} length	Operating requirements for the 2 µm-wide heater at the same RF_{gap} length	Operating requirements for the 3 µm-wide heater at the same RF_{gap} length	Operating requirements for the 4 µm-wide heater at the same RF_{gap} length
1 µm heater ***1.6 µm RF_{gap}***	4.87 V 159 nJ	4.83 V 184 nJ	5.31 V 219 nJ	5.76 V 244 nJ
2 µm heater ***2.7 µm RF_{gap}***	5.17 V 180 nJ	4.6 V 167 nJ	5.07 V 200 nJ	5.66 V 235 nJ
3 µm heater ***4 µm RF_{gap}***		5.04 V 200 nJ	**4.94 V** **190 nJ**	5.5 V 217 nJ
4 µm heater ***4.9 µm RF_{gap}***		5.48 V 236 nJ	5.16 V 207 nJ	5.43 V 217 nJ

The decision therefore comes down to these two options. The final choice is the 3 µm-wide heater with a 4 µm-long RF_{gap}, as it provides a larger volume of amorphizable PCM —offering potential improvements in RF and power-handling performance— while maintaining an acceptable difference in resource consumption compared to the 2 µm case. However, it should be noted that, to minimize the R_{ON} x C_{OFF} FOM, a 1 µm-wide heater combined with a 1.6 µm-long RF_{gap} may be more advantageous, depending on the amorphization efficiency. Reducing the heater width —and thus the amount of tungsten— decreases the parasitic capacitance between the heater and the crystalline PCM, while shortening the RF_{gap} lowers the ON-state resistance of the PCM. Conversely, a smaller RF_{gap} also reduces the volume of amorphous PCM, which can increase the fraction of crystalline PCM interacting with the heater and thereby enhance OFF-state parasitic capacitances.

More broadly, this analysis of heater width and RF_{gap} length associations illustrates the recurring challenge in optimizing PCM-based RF switches: finding the best compromise among a vast space of possible material choices, layouts, dimensions, and pulse designs, so as to balance thermal behavior, energy consumption, component reliability, and RF performance. Regarding the latter, measurements were performed on fabricated devices that incorporated the mechanisms described throughout this chapter. Before presenting the main advances achieved in PCM-based RF switches during this PhD, the next section provides further details on the forming method —introduced in Section 2.2.1— which underpinned the measurements leading to the optimizations discussed in Chapter 4 of this manuscript.

3.6 Forming

As a reminder, when performing a voltage sweep to determine the switching voltage, this method applies several consecutive voltage pulses to the heater —referred to as a pulse train— for each tested voltage before moving to the next. This approach provides a more realistic representation of the switch behavior, as it reproduces the cumulative heating and stress experienced under real operating conditions. It also improves the accuracy of the commutation voltage determination, reducing sensitivity to thermal and electrical fluctuations.

The purpose of this section is to establish the optimal number of pulses a pulse train should contain. To this end, commutation tests were carried out using pulses of identical shape and duration, but varying the number of pulses per train. The evaluation was performed under amorphization conditions, comparing both the voltages required to achieve commutation and the resistance values measured in devices once they successfully switched to the OFF-state.

Figure 3-21 illustrates the experimental procedure. Switches employing GeTeN as the PCM, with heaters 3 µm-wide and 20 µm-long and RF_{gap} of 4 µm, are tested on different chips across the same wafer.

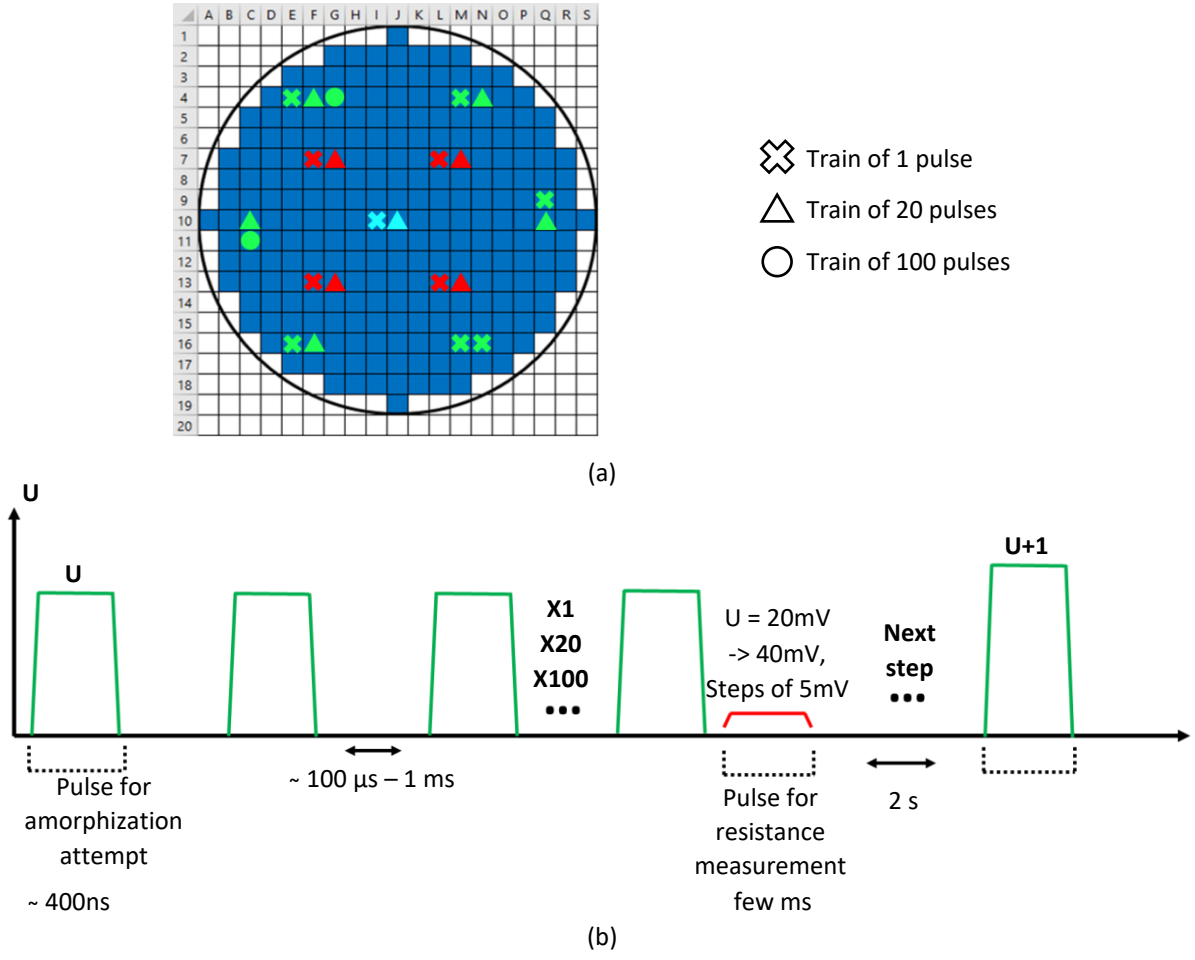
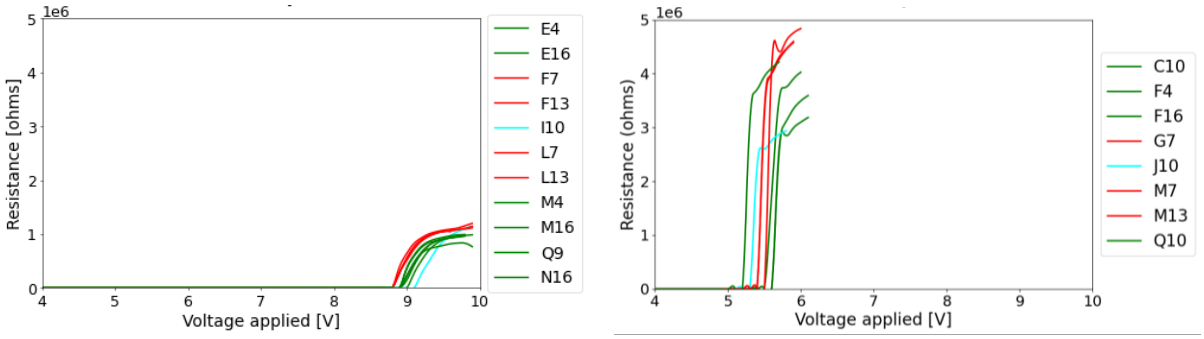


Figure 3-21 : *Protocol used for switch commutation. (a) Positions of the tested chips on the wafer, grouped by color according to their distance from the wafer center. These colors correspond to the curves reported in* **Figure 3-22**. *(b) Chronogram of the applied voltage pulses, showing the pulse duration, the interval between pulses within a pulse train, the interval between pulse trains, and the timing of resistance measurements —performed after each pulse train, just before advancing to the next voltage step in the sweep.*

Figure 3-21.a shows the distribution of the tested chips: some are subjected to pulse trains of 1 pulse, others to 20 pulses, and two chips to 100 pulses. Chips are selected across the wafer to account for potential variations in fabrication, such as differences in layer deposition accuracy that could affect the results. Figure 3-21.b presents a chronogram of the voltage pulse application. The voltage sweep ranges from 4 V to 20 V in 0.1 V increments.

After each tested voltage, a low-voltage pulse is applied to measure the switch resistance. Using a low voltage for resistance measurements prevents interference with the switch's behavior. Figure **3-22** presents the results of the resistance measurements. Each chip is color-coded according to its position on the wafer schematic in Figure 3-21.a. Figure 3-22.a shows the resistances obtained for switches commutated with pulse trains containing a single pulse, while Figure 3-22.b shows the resistances for switches commutated with pulse trains containing 20 pulses. Comparing the two graphs reveals two notable differences. First, switches subjected to pulse trains of 20 pulses achieve significantly higher resistance values. Those commutated with a single pulse per train reach resistances between 830 kΩ and 1.2 MΩ, whereas switches commutated with 20-pulse trains reach resistances ranging from 2.94 MΩ to 4.94 MΩ. Second, the voltage required to achieve commutation is considerably lower with 20-pulse trains, ranging from 5.3 V to 5.7 V, compared to 9.1 V to 9.6 V for single-pulse trains. Additional tests conducted with pulse trains of 100 pulses (not shown) produce performances similar to those obtained with 20-pulse trains.

Overall, these results indicate that pulse trains of 20 pulses represent the optimal choice for performing the forming method. Using fewer pulses per train reduces measurement accuracy, while increasing the number of pulses unnecessarily extends the measurement duration without improving accuracy.



(a) (b)

Figure 3-22 : *Resistances reached after the commutation toward the OFF-state of switches with RF_{gap} of 4 µm length and heaters of 3 µm width. Voltage sweeps from 4 V to 0 V are used, in steps of 0.1 V. Once the resistances reached at least 800 000 Ω, the voltage sweep went on for four more steps before stopping. The pulse trains are either made of (a) 1 pulse per voltage step or (b) 20 pulses per voltage step.*

These substantial differences highlight the importance of accounting for the realistic thermal and electrical behaviors described at the beginning of this section, ensuring that commutation experiments provide reliable guidance for switch design. Finally, this experiment also provides insight into fabrication quality variations across the wafer. Regardless of the number of pulses per train, switches located on chips near the wafer edges —represented in green in both the wafer schematic of Figure 3-21.a and the graphs of Figure 3-22— require higher voltages and achieve lower resistance values compared to switches situated near the center of the wafer, represented in red. These observations confirm that the fabrication process is not entirely uniform across the wafer, highlighting the importance of testing devices across multiple locations to account for these variations during experiments.

3.7 Chapter conclusion

This chapter has established the key parameters governing the optimization of PCM-based RF switches, focusing on layer dimensions, material selection, and the voltage-pulse methodology used during characterization. Each optimization lever has been analyzed to balance energy efficiency, switching performance, and device reliability.

First, the optimized PCM region targeted for melting was defined. The PCM volume must remain sufficiently large to ensure adequate amorphous material formation and performance improvement, yet small enough to limit resource consumption, reduce quench duration —thereby favoring amorphization over recrystallization— and control heater temperature for enhanced reliability. The analysis identified an optimal melt zone covering two-thirds of the PCM length above the RF_{gap}, centered along the PCM, with a PCM thickness of 100 nm. Next, optimization of the heater thickness demonstrated the need to balance thermal efficiency and structural integrity. Considering the heater's resistivity and its impact on energy consumption, a 100 nm- thick heater was selected as the most effective configuration. The choice of dielectric material proved equally critical. Among the materials investigated, AlN offered the best trade-off between heat transfer efficiency and thermal management during both heating and quenching. The optimal dielectric thickness was likewise determined to be 100 nm, providing efficient heat delivery to the PCM and rapid dissipation after switching.

The combined influence of heater width and RF_{gap} length was then assessed to achieve a balance between amorphizable PCM volume, heat flow efficiency, and device reliability. Two design sets were identified according to the desired performance objective:

- For PH_{OFF} optimization, a 3 µm-wide heater with a 4 µm-long RF_{gap}.
- For FOM optimization, a 1 µm-wide heater with a 1.6 µm-long RF_{gap}.

Finally, the voltage-pulse forming methodology was established to ensure measurement reproducibility and represent realistic operating conditions. A train of 20 pulses per voltage step was selected to achieve accurate characterization without excessive test duration.

With the design parameters now defined and justified, a coherent framework for device optimization has been established. This serves as a reliable reference for evaluating subsequent enhancements. The next chapter builds on this foundation, presenting the key optimizations achieved in this work for PCM-based RF switches through a combination of simulation results and electrical characterization.

Chapter 4
Design optimization

In the preceding chapter, the evaluation of PCM-based RF switches with short RF_{gap} highlighted intrinsic thermal challenges. The reduced distance between the RF contacts significantly enhances heat dissipation from the phase-change material (PCM) toward the electrodes, necessitating higher heater voltages to achieve the desired Joule heating. This increase in applied power, however, creates pronounced temperature gradients along the heater, leading to localized hot spots, particularly near the heater extremities where the surrounding SiO_2 dielectric exhibits low thermal conductivity. These hot spots not only jeopardize the structural integrity of the heater but also reduce the uniformity and controllability of PCM crystallization and amorphization.

To address these limitations, the present chapter explores several complementary strategies to improve thermal management and device performance. One key focus is the incorporation of a top AlN capping layer, chosen for its high thermal conductivity. This layer facilitates heat spreading, reducing peak temperatures and promoting a more uniform thermal profile across both the heater and the PCM. Coupled with careful optimization of the dielectric thickness beneath the RF contacts, this approach directly impacts quench dynamics, lowering the time required for the PCM to transition from its molten state to below the recrystallization temperature. Through simulations and experimental characterization, the effects of these structural modifications on ON- and OFF-state resistances, capacitances, and power-handling capabilities are quantified.

Another optimization considered in this chapter focuses on the control of the amorphization pulse itself. Pulse duration strongly influences the temperature reached within the heater, the energy consumed during switching, and the efficiency of PCM phase transition. Both full 3D and 3D slice models are employed to systematically investigate pulse width effects, revealing trade-offs between voltage requirements, maximum temperature, and quench duration. This analysis identifies an optimal pulse duration that balances efficient energy use with reliable, uniform PCM amorphization.

Finally, this chapter introduces a fundamental innovation in heater architecture: splitting the traditional single-branch heater into multiple branches. This multi-branches configuration is designed to homogenize temperature along the PCM, mitigate excess heating in central regions, and enhance both energy efficiency and device reliability. Detailed simulations of single-, double-, and triple-branche(s) designs provide insight into the optimal arrangement of heater coverage and spacing to achieve uniform amorphization while minimizing parasitic effects. Measurements on fabricated devices corroborate these findings, demonstrating improvements in OFF-state isolation, R_{ON} x C_{OFF} FOM, and power-handling capacity.

4.1 Addition of an AlN heat diffusion layer

4.1.1 Effect on the heat distribution in the heater – Simulation with complete 3D model

To mitigate hot-spot formation and promote a more uniform temperature profile, a modified switch architecture is proposed. In this design, a high–thermal-conductivity aluminium nitride (AlN) layer is integrated into the upper part of the switch, positioned between the SiO_2 and Si_3N_4 dielectric layers. Figure 4-1 illustrates this configuration: Figure 4-1.a presents a longitudinal view along the heater axis, while Figure 1.b shows a cross-sectional view along the heater width. In Figure 4-1.a, the red circles

indicate the locations of the previously identified hot spots —namely, the heater extremities confined within low-thermal-conductivity dielectrics.

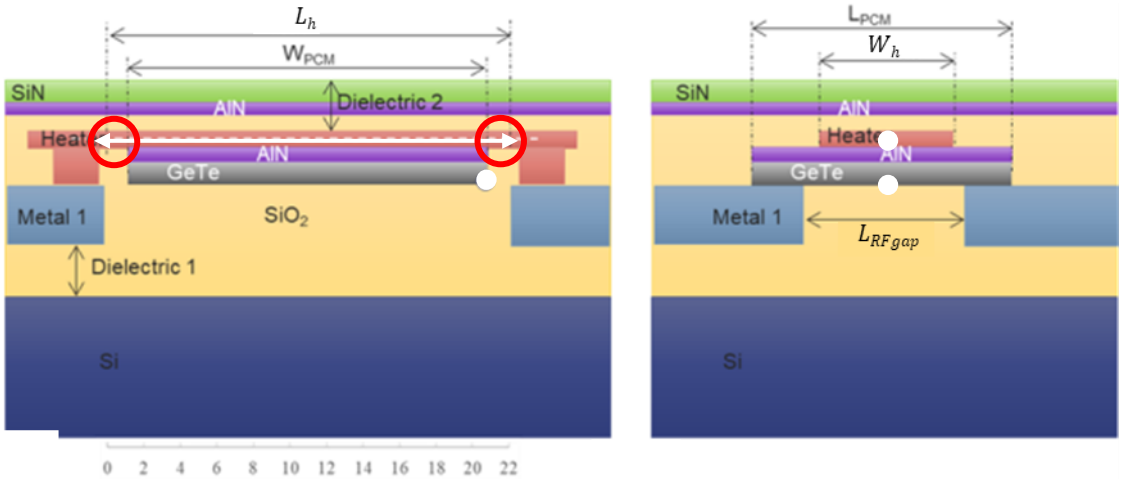


Figure 4-1: *(a) Schematic of the switch technological stack viewed along the heater length. The white line and white point indicate the observation locations used in the graphs of Figure 4-2 and Figure 4-4. Red circles mark the heater regions where heat accumulation occurs. The scale bar corresponds to that used in Figure 4-2. (b) Same stack viewed along the heater width. The white point circled in black in the heater corresponds to the white arrow in the longitudinal view. The white point in the PCM matches the same location in the other view.*

To evaluate the influence of the AlN layer on the heater's thermal distribution, the temperature along the white arrow shown in Figure 4-1 is computed for three different combinations of heater width and RF_{gap} length. Two of these configurations correspond to the most promising designs identified in the previous chapter: a 1 µm-wide heater with a 1.5 µm-long RF_{gap}, and a 3 µm-wide heater with a 4 µm-long RF_{gap}. The geometric parameters of all devices are summarized in Table 4-1. Temperatures are extracted at the end of the heating phase of a 400 ns amorphization pulse. For comparison, the same simulations are performed on the baseline design without the AlN top layer.

Table 4-1: *Dimensions of the studied devices, including PCM width (W_{PCM}), RF_{gap} length (L_{RFgap}) and heater width (W_h).*

Reference	W_{PCM}	L_{RFgap}	W_h
Device A	20 µm	1 µm	1 µm
Device B	20 µm	1.5 µm	1 µm
Device C	20 µm	4 µm	3 µm

Figure 4-2 presents the resulting temperature profiles. For Device B, which features a short RF_{gap}, the close proximity of the RF contacts enhances heat dissipation during the heating phase, thus requiring a significantly higher applied voltage. As a result, in the baseline configuration, the heat becomes strongly confined at the heater extremities, with local temperatures reaching up to 3000 K. Such extreme values drastically increase the risk of heater failure during switching operations; Figure 4-3 shows a microscope image of a heater extremity from a baseline device that fractured following an amorphization attempt. Introducing the AlN capping layer effectively absorbs and redistributes the excess heat from the heater extremities along the length of the switch, thereby improving temperature uniformity. The hot-spot temperature decreases from 3000 K to approximately 2000 K, significantly enhancing device reliability. For Device C, which features a larger RF_{gap}, the greater spacing between the RF contacts facilitates heat accumulation near the PCM center. In the baseline configuration, heat

also escapes through the metallic pads at the heater edges along its length, reversing the temperature gradient — making the heater center hotter than its extremities.

Nevertheless, incorporating the AlN top capping layer again promotes a more homogeneous temperature profile and reduces the maximum temperature reached within the heater.

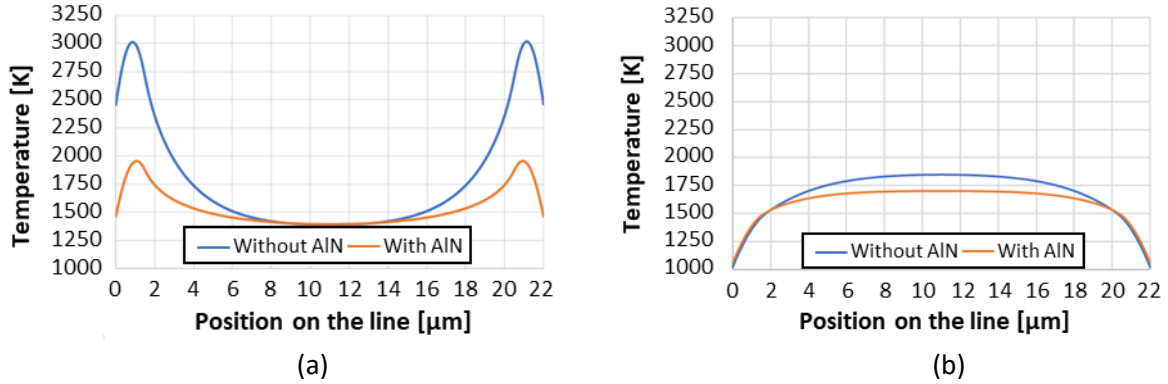


Figure 4-2: *(a) Temperature distribution along the white arrow defined in Figure 4-1 for (a) Device B and (b) Device C. Orange curves represent designs including the AlN layer, while blue curves correspond to the baseline designs without AlN.*

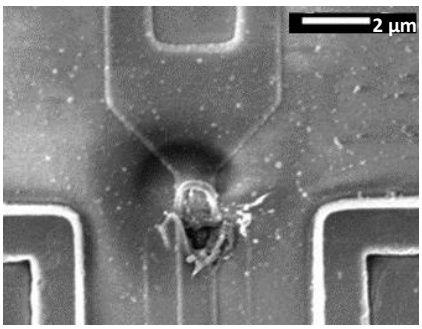


Figure 4-3: *Optical image of a heater extremity from a switch without the AlN top layer, showing fracture after an amorphization attempt.*

These initial simulations highlight how the addition of an AlN top capping layer effectively redistributes heat within the switch, reducing peak temperatures in the heater and improving the quench behavior of the PCM. These results underscore the potential of the AlN layer to enhance device reliability while guiding the design of subsequent simulations.

4.1.2 Effect on the quench duration – Simulation with 3D slice model

Additional simulations were conducted to highlight the benefits of integrating an AlN layer at the top of the switch for improving PCM cooling during the quench phase. In these simulations, the quench duration is defined as the duration required for at least one point within the PCM to cool from the melting temperature (1000 K) to below the recrystallization threshold (500 K). Figure 4-4 shows the temperature evolution during a 150 ns amorphization pulse for Device A (with a 1 µm-long RF_{gap}) and Device C (with a 4 µm-long RF_{gap}), taken at the white point in the PCM indicated in Figure 4-1. Then the AlN capping layer is introduced, the quench duration improves by approximately 50 ns for Device A and 75 ns for Device C compared to the baseline configuration. This improvement results from enhanced thermal dissipation provided by the AlN layer, which introduces an additional heat evacuation path. The voltage applied, energy required to melt two-thirds of the PCM, the maximum

heater temperature during the amorphization pulse, and the corresponding quench durations (defined as above) are summarized in Table 4-2 for both devices.

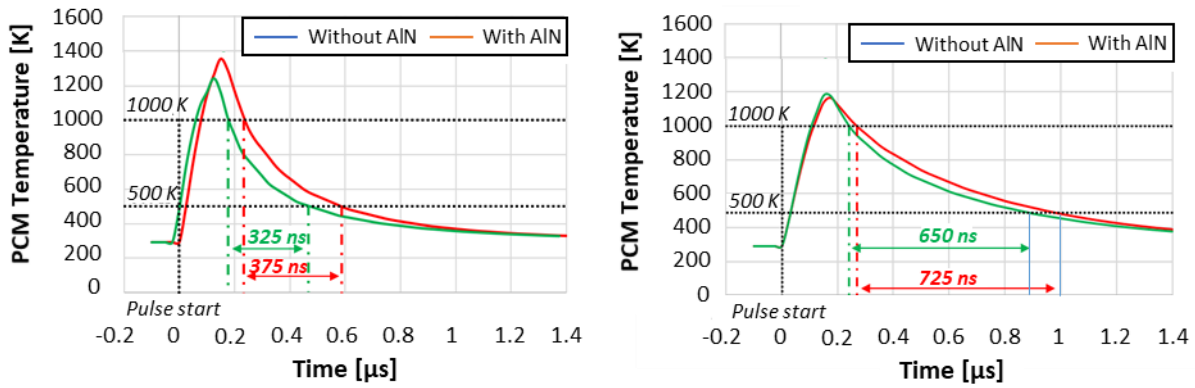


Figure 4-4: *Temperature evolution and quench duration at the white point defined in Figure 4-1 during a 150 ns amorphization pulse for (a) Device A and (b) Device C.*

Although incorporating the AlN layer increases the required voltage and overall energy consumption —owing to the enhanced heat dissipation— it also significantly reduces the maximum heater temperature, thereby improving device reliability.

Table 4-2: *Summary of voltage required to melt two-thirds of the PCM, heater energy consumption during the pulse, maximum heater temperature, and quench duration measured at the white point defined in Figure 4-1 for Devices A and C.*

	Device A		**Device C**	
AlN presence	No	Yes	No	Yes
RF_{gap} length [µm]	1µm	1µm	4µm	4µm
Applied voltage [V]	10.91	12.2	9	10.15
Consumed energy [nJ]	215	269	147	187
Heater max temperature [K]	2464	2183	1846	1702
Quench duration [ns]	375	325	725	650

These reductions in quench duration are achieved thanks to the AlN capping layer, which supplements the main thermal evacuation pathway through the RF contacts. Nevertheless, as shown in Figure 4-4 and Table 4-2, the quench duration remains relatively high for devices with larger RF_{gap}, where the central region of the PCM cools more slowly. Therefore, additional design strategies must be explored to further decrease the quench duration in such configurations.

4.2 Reduction of the PCM-substrate distance – Simulation with 3D slice modelling of an AlN heat diffusion layer

The next approach investigated to reduce the quench duration is to utilize the substrate as an efficient heat sink. Owing to its high thermal conductivity, bringing the substrate closer to the PCM layer accelerates cooling. To assess the impact of substrate proximity on the switch's thermal behavior, two thicknesses were varied in the simulations: the RF contacts thickness and the dielectric layer beneath them (dielectric 1). These thicknesses are defined in Figure 4-5, which presents the reference design used for the simulations: a top view in Figure 4-5.a shows only the heater, PCM, and RF_{gap}, while a

cross-sectional view in Figure 4-5.b depicts the entire stack. The RF contacts thickness is denoted as t_{RF} and the dielectric thickness below the RF contacts as t_{Diel1}. Table 4-3 summarizes the thicknesses tested. RF contacts thicknesses range from 100 nm to 600 nm, while the dielectric under the contacts is generally 50 nm. In two additional configurations, the RF contacts remain 600 nm thick, while the dielectric layer is increased to either 100 nm or 500 nm. For all simulations, the heater width is 3 µm and the RF_{gap} length is 4 µm. The table also reports the voltage required to melt two-thirds of the PCM volume within the RF_{gap}, the corresponding energy consumption, the maximum heater temperature at the end of a 400 ns amorphization pulse, and the quench duration (*Qduration*), defined in two ways:

- *Tmin* is the time required for the first point in the PCM to cool below the recrystallization temperature (500 K).
- *Tmax* is the time required for all points in the melted PCM region to cool below the recrystallization temperature.

The additional AlN layer studied in the previous section is included in all configurations.

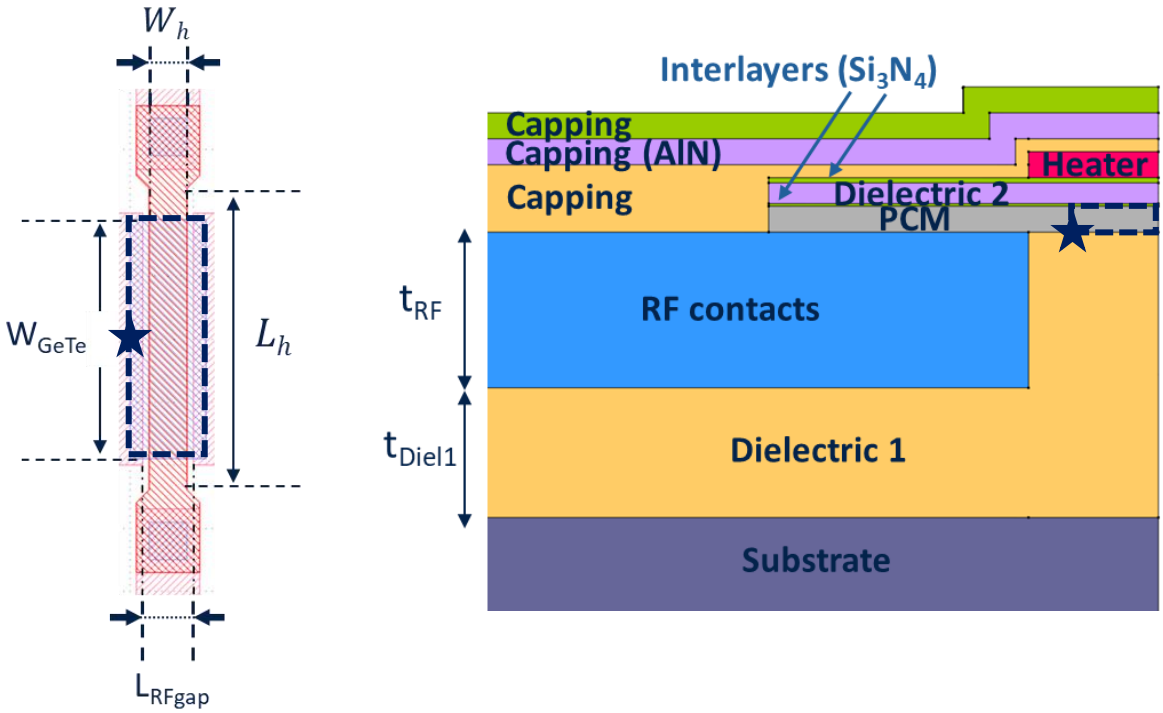


Figure 4-5: *(a) Top view of the switch design, showing a 19 µm-long heater (red striped element) with the associated PCM (blue striped element). The dark dotted rectangle indicates the two-thirds PCM region used to monitor the minimum and maximum temperatures for quench duration calculations reported in Table 4-3. The star marks the specific point in the PCM used to monitor temperature for the quench duration reported in Table 4-4. (b) Cross-sectional view of a switch configuration including the AlN top capping layer. The positions of the dark dotted rectangle and the star from (a) are also indicated.*

The results indicate that reducing the PCM-substrate distance clearly decreases the quench duration, as heat evacuates more efficiently through the substrate. This improvement enhances the amorphization efficiency of the switch. However, while heating parameters (voltage required to melt two-thirds of the PCM, associated heater energy consumption, and maximum heater temperature) remain nearly constant for larger PCM-substrate distances, they degrade exponentially when the distance becomes too small. Specifically, distances below 350 nm (corresponding to RF contacts thicknesses below 300 nm and a dielectric thickness of 50 nm) induce substantial increases in the required voltage, energy consumption, and maximum heater temperature. This behavior occurs

because further decreasing the PCM-substrate distance significantly increases the thermal conductance of the substrate heat evacuation path, necessitating high power to reach the melting temperature. Excessive heating can compromise the heater's integrity. An RF contacts thickness of 300 nm combined with a 50 nm SiO_2 dielectric layer represents a practical optimum, balancing quench performance and heater safety.

Table 4-3: *Voltages required to melt two-thirds of the PCM, corresponding energy consumption, maximum heater temperature, and quench durations for: at least one point in the PCM cooling below the recrystallization temperature (Qduration -> Tmin) and all points cooling below the recrystallization temperature (Qduration -> Tmax) in the dotted rectangle defined In Figure 4-5 for different combinations of RF contacts and dielectric 1 thicknesses.*

RF contacts thickness [nm]	**600**	**600**	**600**	**500**	**400**	**300**	**200**	**100**
Dielectric thickness [nm]	**500**	**100**	**50**	**50**	**50**	**50**	**50**	**50**
Energy [nJ]	206	207	212	219	231	**246**	291	411
Voltage [V]	7.16	7.18	7.26	7.38	7.59	**7.82**	8.5	10.1
$Tmax_{heater}$ [K]	1510	1530	1530	1553	1594	**1653**	1787	2110
Qduration -> Tmin [ns]	725	550	525	500	450	**375**	325	275
Qduration -> Tmax [ns]	825	650	625	600	575	**550**	525	525

Because the PCM minimum and maximum temperatures do not necessarily correspond to the same points in the PCM across different thicknesses, a complementary analysis was performed at a fixed observation point. This point, marked by a star in Figure 4-5.a and Figure 4-5.b, is located at mid-width of the PCM base and two-thirds along the RF_{gap} length from the center. The applied voltage is set to melt two-thirds of the PCM volume, ensuring that, at the end of the heating step, the PCM point with the lowest temperature reaches 1000 K. Notably, this observation point, although near the RF contacts (which serve as good heat evacuation spots), is not the closest to the metallic pads at the heater length extremities, which also contribute to heat dissipation. Consequently, the temperature at this point exceeds 1000 K at the end of the heating phase. Figure 4-6 presents the temperature evolution at this observation point during a 400 ns amorphization pulse, with the same performance parameters analyzed as in Table 4-3, across four combinations of RF contacts and dielectric thicknesses.

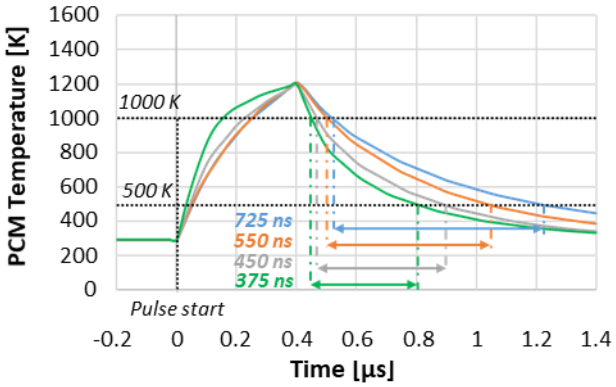


Figure 4-6: *Temperature evolution and quench duration at the PCM observation point marked by a star in Figure 4-5 during a 150 ns amorphization pulse.*

The results in Figure 4-6 confirm that reducing the PCM-substrate distance is an effective method to accelerate quenching, decreasing the quench duration from 725 ns to 375 ns. However, this strategy is constrained by its impact on other device performance metrics. Table 4-4 summarizes these

limitations. An RF contacts thickness of 300 nm paired with a 50 nm dielectric layer is again identified as an optimal configuration, achieving a 24 % reduction in quench duration compared to the baseline (600 nm RF contacts and 500 nm dielectric) while limiting adverse effects on other performance parameters.

Table 4-4: *Voltages required to melt two-thirds of the PCM, calculated energy consumption, maximum heater temperature, and quench duration measured at the PCM observation point marked by a star in Figure 4-5, for different combinations of RF contacts and dielectric 1 thicknesses.*

RF contacts thickness [nm]	**600**	**600**	**300**	**100**
Dielectric thickness [nm]	**500**	**100**	**50**	**50**
Energy [nJ]	206	207	246	411
Voltage [V]	7.16	7.18	7.82	10.1
$Tmax_{heater}$ [K]	1510	1530	1652	2110
Quench duration [ns]	725	550	450	375

These insights regarding quench duration and optimal distances between PCM and substrate provide a solid foundation for further device improvements, particularly when combined with additional layers to enhance thermal management.

4.3 Coupling the AlN top capping layer with the reduction of the PCM-substrate distance

Building on these findings, new devices incorporating an AlN top capping layer combined with reduced dielectric thickness under the RF contacts (100 nm) were fabricated and tested at CEA-LETI, to further enhance RF and power-handling performance. Figure 4-7.a presents the OFF-state power-handling measurements for devices in series configuration with (Lot gen2) and without (Lot gen1) the design enhancements, across different combinations of RF_{gap} length and heater width.

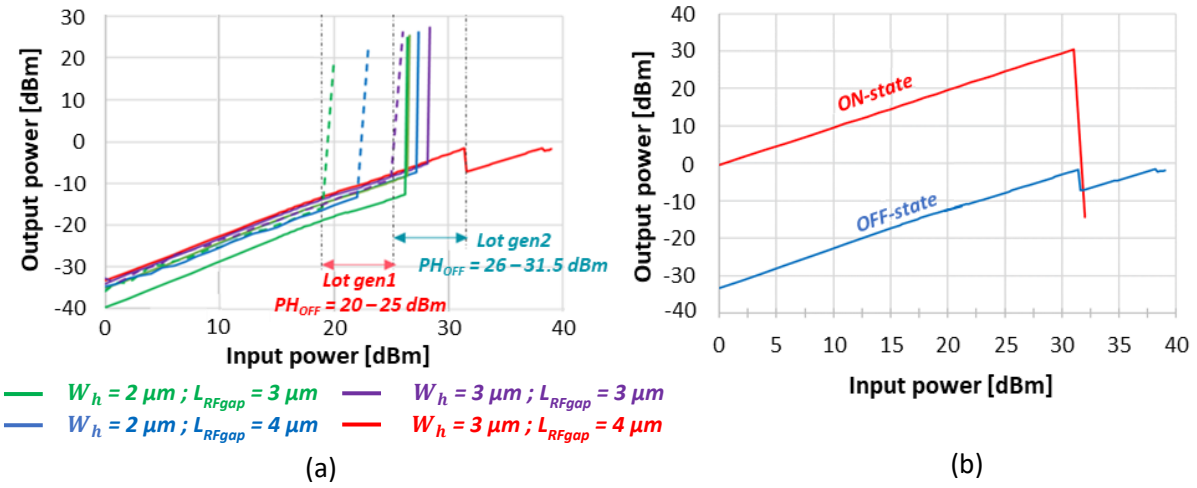


Figure 4-7: *(a) OFF-state power-handling for devices before (Lot gen1) and after (Lot gen2) implementing the AlN capping layer and reducing the dielectric thickness beneath the RF contacts to 100 nm. (b) Power-handling in both ON-state and OFF-state for the Gen2 device with an RF_{gap} length of 4 µm and a heater width of 3 µm.*

On average, the new devices exhibit a 6 dBm higher power-handling than the first lot. In particular, the device with the longest RF_{gap} and widest heater reached 31 dBm, and it is the only device that failed when the limit was reached. In contrast, other switches crystallized and transitioned to the ON-state.

The origin of this failure is illustrated Figure 4-7.b, which shows the ON-state power-handling for the same device, also measured at 31 dBm. Consequently, when the switch reaches its OFF-state power limit, it attempts to crystallize, but cannot transition to the ON-state because the ON-state power limit is simultaneously reached. The ON-state resistance (R_{on}) and OFF-state capacitance (C_{OFF}) were also characterized for the switch with the longest RF_{gap} and widest heater. As shown in Figure 4-8.a, up to 10 GHz, the insertion loss remains below 0.4 dB, corresponding to an R_{ON} value of 4.5 Ω, while the isolation exceeds 16 dB, corresponding to a C_{OFF} value of 25 fF. While the R_{on} meets the target, C_{OFF} was expected to reach 14 fF. This would have resulted in a FOM of 61 fs, but instead this value was 112 fs. Given that the targeted power-handling for series structures is 36 dBm, additional improvements are needed.

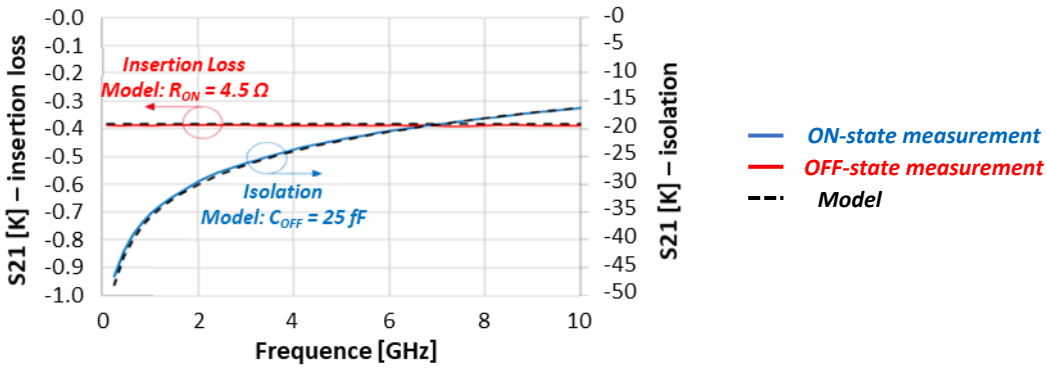


Figure 4-8: *ON-state resistance and OFF-state capacitance for the Gen2 device with an RF_{gap} length of 4 µm and a heater width of 3 µm.*

Nonetheless, achieving a 31 dBm power-handling in both ON and OFF states in series configuration represents a state-of-the-art performance for PCM-based RF switches. Table 4-5 compares this device's performance with other results reported in the literature, highlighting the improvements achieved through the combined design strategies.

Table 4-5: *Comparison of ON-state and OFF-state power-handling and R_{ON} x C_{OFF} FOM for various PCM-based RF switch designs reported in the literature, including different RF_{gap} lengths and PCM widths, alongside the performance achieved in this work.*

Reference	L_{RFgap} [µm]	W_{GeTe} [µm]	PH_{ON} [dBm]	PH_{OFF} [dBm]	FOM [fs]
[57]	1	10	27	23	10
[57]	1	10	27	34.5	50
[118]	3	10	39	26	35
[119]	4	90	37	29	93
This work	4	50	31	31.5	112

While the combination of an AlN capping layer with a reduced dielectric thickness under the RF contacts significantly improved power-handling and ON/OFF performance, alternative strategies for heat management were explored to further optimize temperature distribution and quench behavior.

4.4 Heat diffusion metal capping – Simulation with complete 3D model

One such approach involved adding a metallic aluminium (Al) top capping layer to the switch, leveraging its high thermal conductivity to diffuse heat more effectively within the heater and PCM. Figure 4-9 presents the first simulated designs incorporating this metal capping layer. All configurations share the same geometric parameters: an RF_{gap} length of 4 µm, a heater width of 3 µm, and a heater

length of 19 µm. They are compared to both the baseline configuration (without any top capping) and the configuration including the AlN top capping layer. In the metal-capped models, the Al layer extends laterally to cover the RF contacts, allowing efficient heat conduction toward the sides of the switch during the quench step.

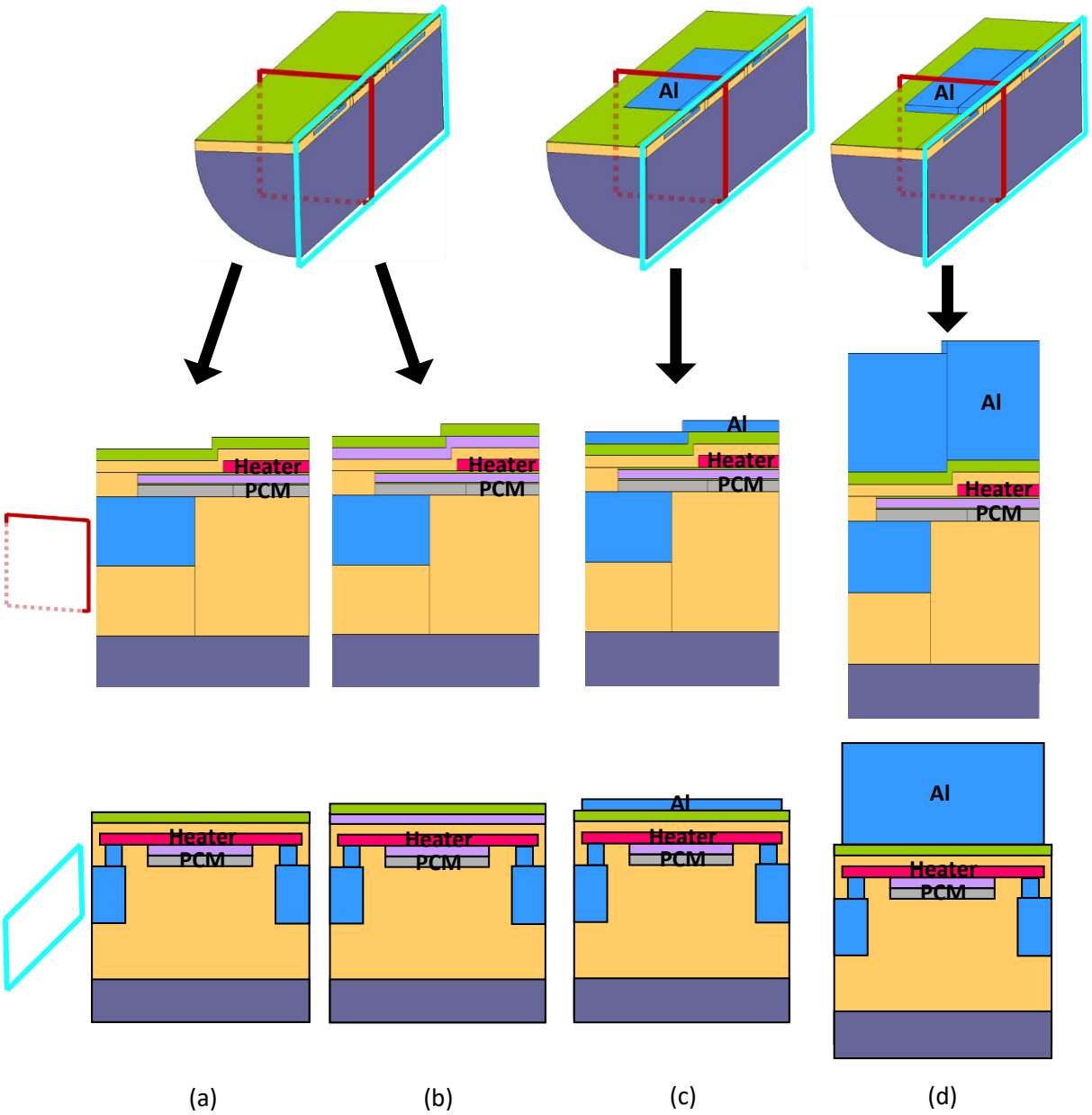


Figure 4-9: *Configurations of the simulated switches: (a) baseline configuration, (b) with a top AlN capping layer, (c) with a 100 nm-thick aluminium (Al) top capping layer covering the heater length, and (d) with a 1 µm-thick Al top capping layer covering the heater length. The top row shows complete 3D views of the switches (halved at mid-width). The middle row presents cross-sectional views along the width (cut at mid-length), and the bottom row shows cross-sectional views along the length (cut at mid-width).*

In this first study, two Al capping thicknesses were considered: 100 nm and 1 µm. For each configuration, the voltage required to melt two-thirds of the PCM and the time needed for the entire PCM region to cool from the melting temperature to below the recrystallization temperature were determined (Figure 4-10). The results show a clear improvement in the quenching behavior with the addition of a 100 nm-thick Al layer. Increasing the Al thickness to 1 µm further reduces the quench duration significantly; however, this comes at the cost of a marked increase in both the required

voltage and total energy consumption. This behavior stems from the enhanced thermal evacuation caused by the thicker metal, which cools the PCM faster but simultaneously demands higher power to achieve melting.

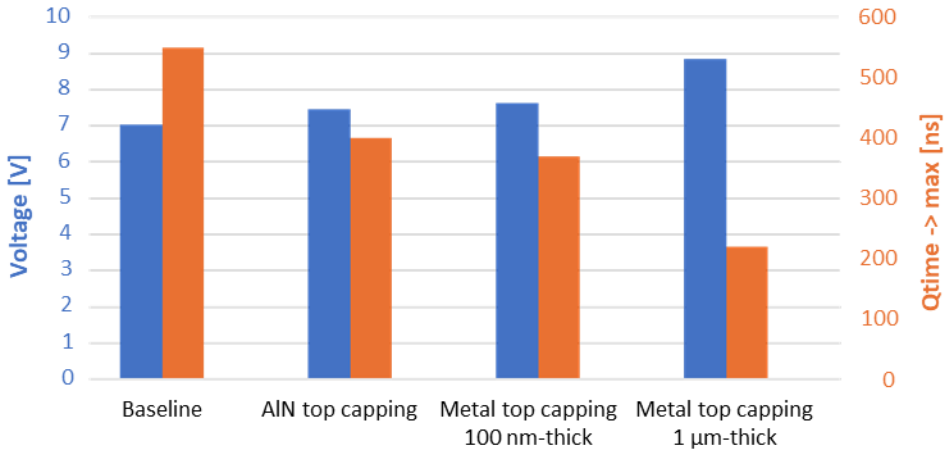


Figure 4-10: *Voltages required to melt two-thirds of the PCM and quench durations corresponding to the complete cooling of all PCM points from the melting temperature to below the recrystallization temperature, for each configuration presented in Figure 4-9.*

However, a critical issue arises when the Al layer extends across the entire width of the RF contacts. This configuration introduces parasitic capacitances between the metal capping and the underlying heater, which can degrade the switch's high-frequency RF performance. To mitigate these parasitic effects, the Al coverage area was reduced, resulting in new design variations illustrated in Figure 4-11. All new configurations employ a 1 µm-thick Al layer. The first design (Figure 4-11.b). features a metal strip covering the entire heater length. The second design (Figure 4-11.c) includes two separate Al blocks, each positioned at the extremities of the heater to cover its hot spots. The third design (Figure **4-11**.d also uses two Al blocks, but they are shifted slightly inward so as not to overlap the hot spots. For comparison, (Figure 4-11.a) shows the baseline configuration without any Al capping.

The impact of these different designs on the temperature distribution within the heater is shown in Figure 4-12. In all cases, the addition of Al reduces the maximum heater temperature relative to the baseline, as the metal facilitates lateral heat spreading. Between the two dual-block configurations, the design where the metal overlaps the heater's hot spots (Figure 4-12.c) shifts the peak temperature toward the heater center, but without significantly reducing its magnitude. This occurs because the enhanced heat dissipation at the extremities necessitates higher input energy to maintain sufficient PCM heating at the edges, leading to increased total energy consumption and central heat accumulation. Figure 4-13 summarizes the key thermal metrics —voltage required to melt two-thirds of the PCM and quench duration for complete cooling— for all configurations. Both designs with two separate Al blocks require lower actuation voltages than the continuous metal strip configuration, as the latter diffuses excessive heat away from the heater center. The configuration with two Al blocks that do not overlap the hot spots offers the lowest energy consumption and the shortest quench duration, confirming its superior thermal efficiency.

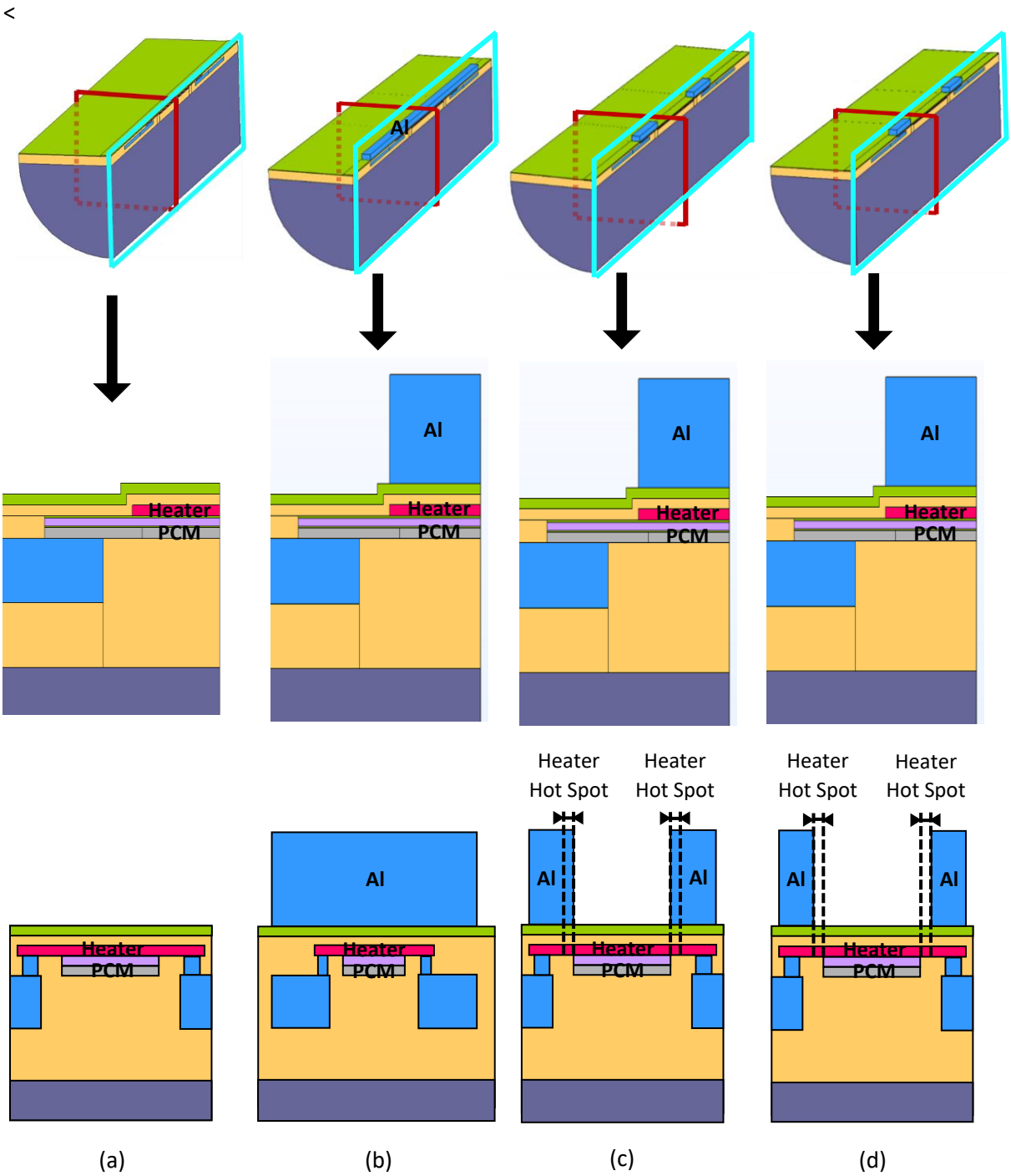


Figure 4-11 : *Configurations of the simulated switches: (a) baseline configuration, (b) with a 1 µm-thick Al top capping block covering the heater length and pads, (c) with two 1 µm-thick Al top capping blocks covering the heater extremities and overlapping the hot spots, and (d) with two 1 µm-thick Al top capping blocks covering the heater extremities without overlapping the hot spots. The top row shows complete 3D views of the switches (halved at mid-width). The middle row presents cross-sectional views along the width (cut at mid-length), and the bottom row shows cross-sectional views along the length (cut at mid-width).*

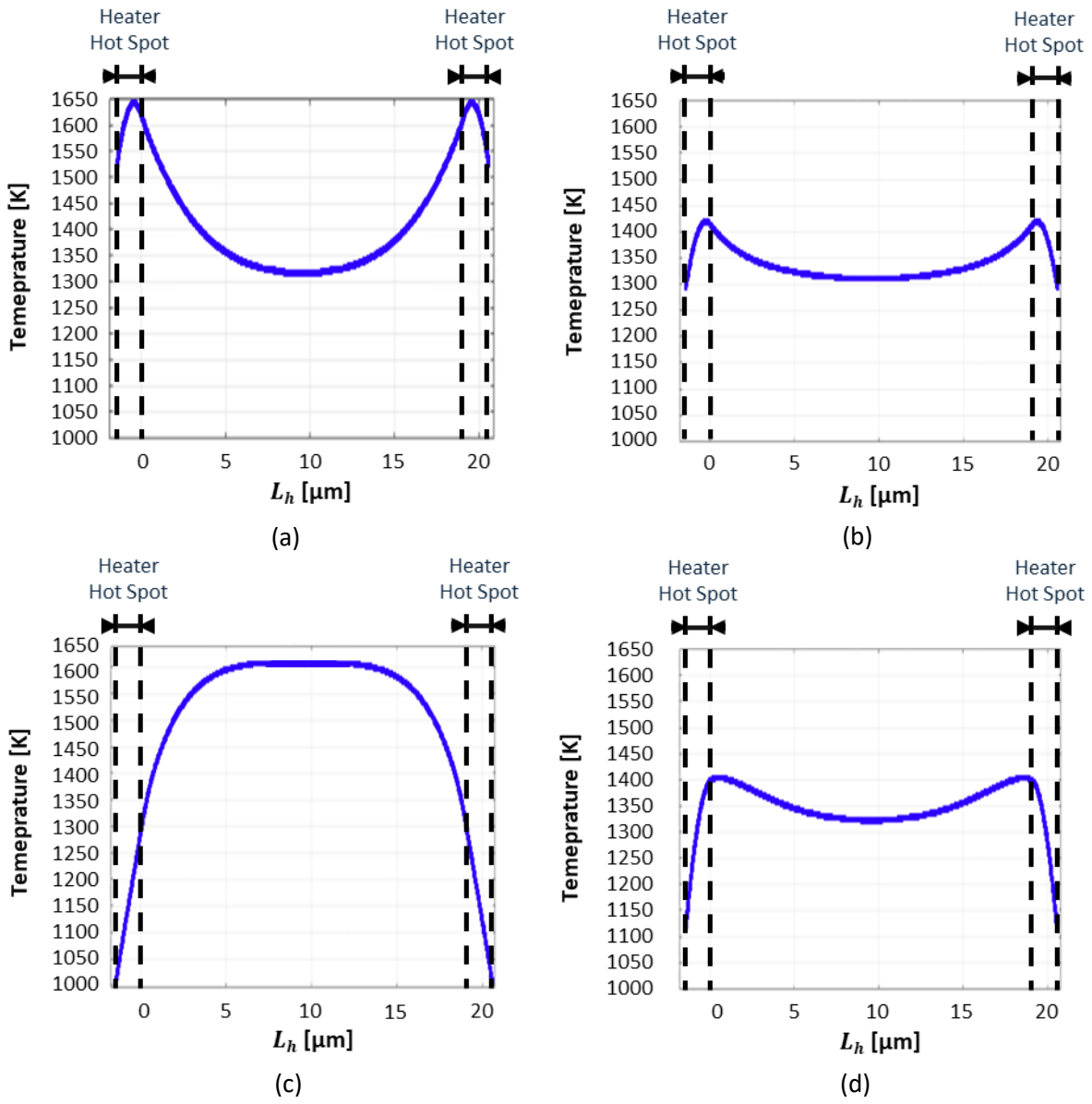


Figure 4-12: *Temperatures at the end of the heating step of a 400 ns-long amorphization pulse along the heater length defined by the white arrow in Figure 4-1, for the following configurations: (a) baseline, (b) with a 1 µm-thick Al top capping block covering the heater length and pads, (c) with two 1 µm-thick Al top capping blocks covering the heater extremities and overlapping the hot spots, and (d) with two 1 µm-thick Al top capping blocks covering the heater extremities without overlapping the hot spots.*

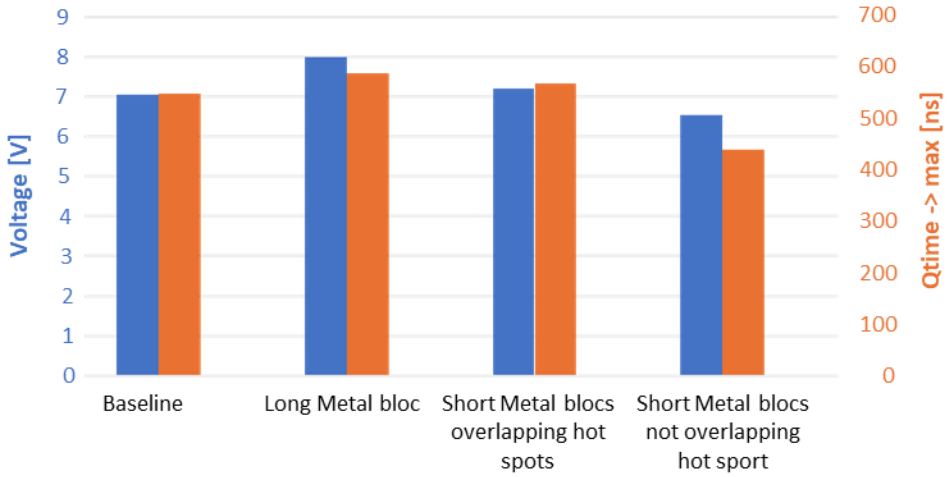


Figure 4-13: *Voltages required to melt two-thirds of the PCM and quench durations corresponding to the complete cooling of all PCM points from the melting temperature to below the recrystallization temperature, for the configurations presented in Figure 4-12.*

In conclusion, extending the Al capping across the entire heater length is unnecessary. The most effective configuration consists of two short Al blocks positioned near the heater extremities but not covering the hot spots. This design achieves a balanced heat distribution within the heater, reduces quench duration, minimizes energy consumption, and limits parasitic capacitance —ultimately improving both thermal and electrical performance of the switch.

4.5 Voltage pulse shapes – Simulation with complete 3D model and 3D slice model

Optimizing the electrical pulse parameters represents another key aspect in improving switching efficiency. In particular, the duration of the amorphization pulse strongly influences the thermal behavior of the PCM and, consequently, the performance and reliability of the switch. In general, the objective of an amorphization pulse is to melt and subsequently amorphize the largest possible fraction of the PCM. However, the outcome of this process depends critically on the pulse duration. A longer pulse allows finer control over the temperature evolution and requires a lower voltage to reach the melting temperature of the PCM. Yet, because heat has more time to diffuse into the surrounding layers, the entire device becomes hotter, leading to slower cooling during the quench phase. Conversely, a shorter pulse limits thermal diffusion into the rest of the stack and reduces the time available to reach the melting point. This requires a higher actuation voltage, resulting in steeper temperature gradients and potentially excessive heating of the heater region. Achieving complete PCM melting without overheating therefore becomes more challenging.

4.5.1 Simulations with a complete 3D model

To identify an optimal pulse duration, simulations were performed using several pulse lengths for two configurations: one including the AlN top capping layer and one without it. Both models feature an RF_{gap} length of 4 µm and a heater width of 3 µm. Figure 4-14 presents the voltages required to melt two-thirds of the PCM, the corresponding quench durations (time for the PCM to cool from the melting to the recrystallization temperature), and the energy consumed during each pulse. For the longest pulse duration (400 ns), the required voltage decreases, but both energy consumption and quench

duration increase —consistent with the expected effects of extended thermal diffusion within the switch. This trend is observed for both configurations, regardless of the presence of the AlN layer.

From these results, a 100 ns pulse initially appears to offer the best compromise: it consumes only slightly more energy than the 50 ns pulse while requiring a significantly lower voltage. However, to confirm this choice, it is essential to also consider the maximum temperature reached in the heater.

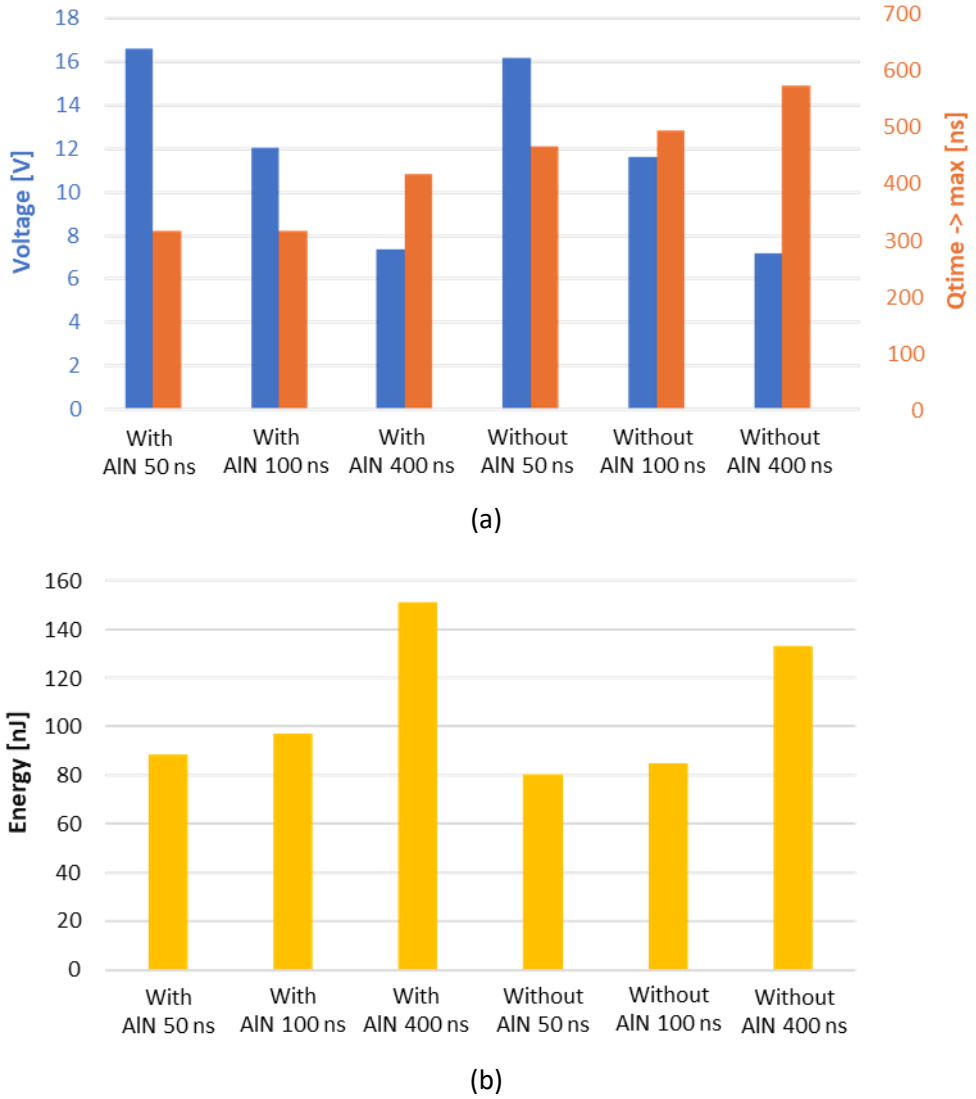


Figure 4-14: *(a) Voltages required to melt two-thirds of the PCM and quench durations for complete cooling of the PCM (all points) from the melting temperature to below the recrystallization temperature, shown for different amorphization pulse durations and for configurations with and without the AlN top capping layer. (b) Heater energy consumption during the pulse for the same configurations as in (a).*

Figure 4-15 compares the temperature distributions along the heater length at the end of the heating step for each pulse duration, for baseline configuration on the left panels and the configuration with AlN capping on the right panels. With a 50 ns pulse (Figure 4-15.a), the maximum temperature in the model without AlN capping reaches nearly the same level as that observed in devices with short RF_{gap} (as in Figure 4-2.a). In this regime, even the AlN layer is insufficient to substantially reduce the heater temperature. A 100 ns pulse (Figure 4-15.b) achieves temperatures below 2000 K, but only when the AlN capping layer is present.

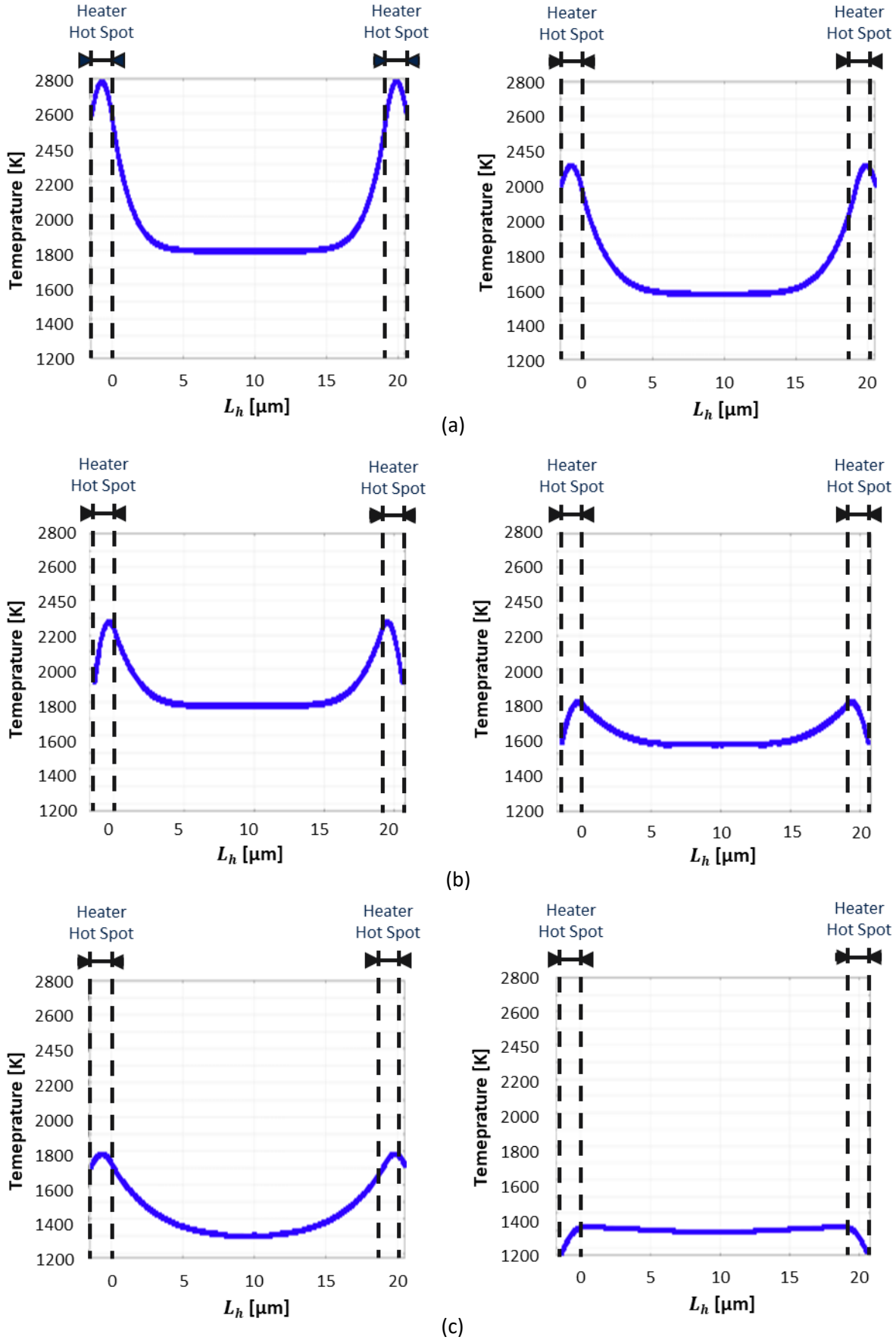


Figure 4-15: *Temperature profiles along the heater length defined by the white arrow in Figure 4-1 at the end of the heating step of amorphization pulses. The panels on the left correspond to the baseline configuration while the panels on the right show the AlN-capped configuration. The amorphization pulses durations are (a) 50 ns, (b) 100 ns, and (c) 400 ns.*

For the 400 ns pulse (Figure 4-15.c), the baseline configuration already exhibits temperatures below 2000 K, while adding the AlN capping further improves thermal uniformity along the heater. This makes the 400 ns pulse particularly attractive from a reliability standpoint.

However, in order to confirm this potential choice, another critical parameter must be considered: the temperature reached inside the heater.

4.5.2 Simulations with a 3D slice model

To refine the analysis and assist in the final selection of the optimal pulse duration, an extended simulation campaign was conducted using the 3D slice model (same as in Figure 4-5), for the design incorporating the AlN capping layer. The monitored zone corresponds to the two-thirds PCM region delimited by the black rectangle in Figure 4-5. In this case, the dielectric layer under the RF contacts was 50 nm-thick SiO_2. The performances corresponding to the tested pulse durations are presentd in Table 4-6.

The actuation voltage and maximum heater temperature both follow an exponential increase as the pulse duration decreases from 1000 ns to 25 ns, a trend that becomes particularly pronounced for durations shorter than 500 ns. When considering energy consumption and quench duration simultaneously, two potentially optimal pulse durations emerge: 100 ns and 500 ns. The 100 ns pulse provides an energy consumption approximately 8 % lower than that of the 500 ns pulse, whereas the 500 ns pulse yields a maximum heater temperature nearly 30 % lower. Given that the simulation time step is 25 ns, variations in quench duration below 100 ns are considered negligible.

Table 4-6 : *Voltages required to melt two-thirds of the PCM, associated energy consumption, maximum temperature reached in the heater, and quench durations corresponding to the cooling of at least one point (Qduration → Tmin) or all points (Qduration → Tmax) of the PCM from the melting temperature down to below the crystallization temperature, for different amorphization pulse durations.*

Pulse duration [ns]	**25**	**50**	**100**	**500**	**800**	**1000**
Energy [nJ]	250	219	**193**	**232**	292	336
Voltage [V]	25.75	17.55	**12.18**	**6.91**	6.33	6.15
$Tmax_{heater}$ [K]	4012	2888	**2108**	**1525**	1529	1537.3
Qduration -> Tmin [ns]	575	550	**550**	**525**	600	600
Qduration -> Tmax [ns]	825	800	**800**	**900**	1000	1050

A complementary analysis, similar to that presented in Table 4-4 and performed using the same model (with a 50 nm dielectric under the RF contacts), focused on the observation point defined by the white star in Figure 4-5. The results, presented in Table 4-7, again show that quench durations remain nearly constant for pulse lengths below 100 ns, confirming 100 ns as one of the two optimal durations. Increasing the pulse duration to 500 ns leads to an approximately 25 % longer quench duration.

Table 4-7 : *Voltages required to melt two-thirds of the PCM, associated energy consumption, maximum temperature reached in the heater, and quench duration measured at the point indicated by a star in Figure 4-5 for the same models and various amorphization pulse durations as in Table 4-6.*

Pulse duration [ns]	**25**	**50**	**100**	**500**	**800**	**1000**
Quench duration [ns]	675	675	**675**	850	925	950

Considering all performance indicators —energy consumption, maximum heater temperature, and quench behavior— a pulse duration of 100 ns emerges as the most balanced and efficient choice.

Importantly, this conclusion holds only when an AlN capping layer is implemented, as it effectively mitigates excessive temperature rise within the heater, ensuring both performance and reliability.

4.6 Multiple-branches heater architecture

4.6.1 Limits of the single-branch architecture and presentation of the solution

Having established the optimal pulse duration and the benefits of the AlN capping layer for thermal management, the next step is to investigate how modifications to the heater architecture itself can further enhance temperature homogenization, energy efficiency, and overall device performance. In conventional devices employing a single-branch heater (standard single-branch design), the temperature distribution along the longitudinal axis is not uniform. Because the extremities of the heater and PCM are located close to the RF contacts —highly efficient thermal conductors— these regions tend to dissipate heat more rapidly. As a result, heat accumulates preferentially in the central region of both the heater and the PCM. This effect becomes particularly pronounced in devices with long RF_{gap}, as illustrated in **Erreur ! Source du renvoi introuvable.**, where the maximum temperature is reached near the center of the PCM.

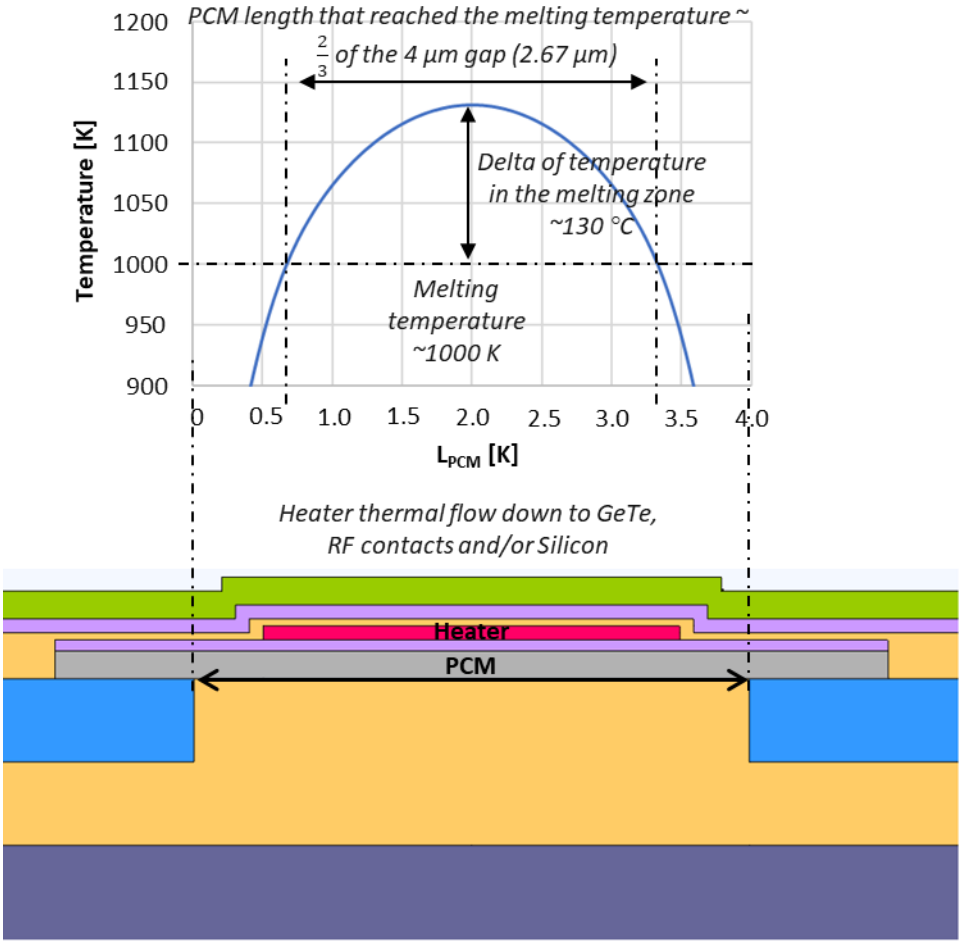
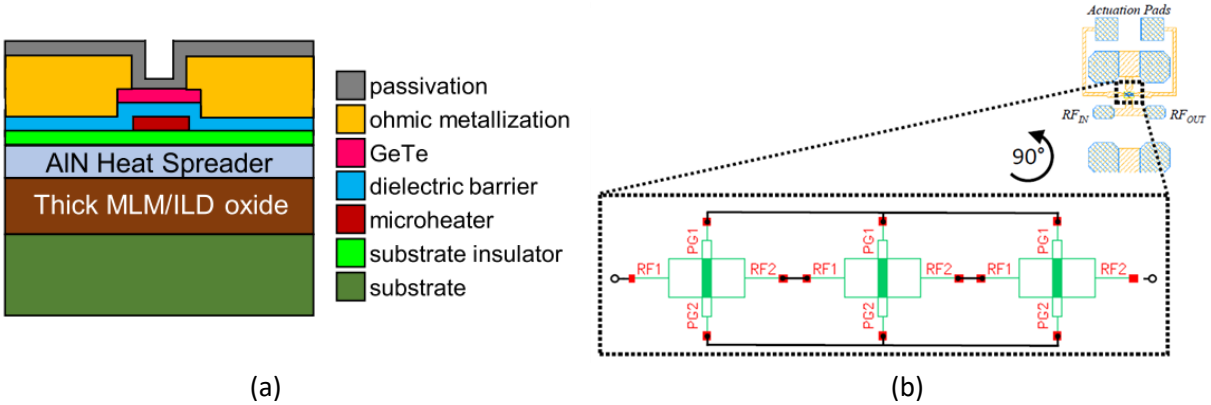


Figure 4-16: *(a) 3D views of a common heater architecture based on a single-branch heater (left) and another using double-branches heater (right). (b) Cut plans of switches using heaters with a single-branch (left) or with double-branches, supported by top view photography of a CEA-fabricated device using this new design (right).*

This thermal non-uniformity generates two major issues. First, the local overheating occurring in the central region increases the risk of degradation or even destruction of the materials, which negatively affects the reliability of the switch. Second, in order to raise the temperature of the PCM edges to the desired value, additional heat must be generated by the heater, leading to excessive heating in the center and unnecessary energy consumption. Moreover, the heater interacts with the crystalline part of the PCM, producing parasitic capacitances that degrade the RF performance of the device. This parasitic capacitance, which is proportional to the total length of the crystalline PCM, can increase the C_{OFF} value by a factor of two to four, thereby degrading the figure of merit (FOM) to the same extent. Together, these effects highlight the need to improve the amorphization efficiency and thermal management of the PCM region.

Several strategies have been proposed to improve temperature homogeneity within the switch, though each comes with its own limitations. The first one is the conventional bottom-heater structure described in Section 1.3.2, in which the heater is positioned beneath the PCM and close to the substrate. Owing to the substrate's high thermal conductivity, this configuration promotes a more uniform temperature distribution along the heater width and accelerates the quench phase. However, the constraints on dielectric thickness, combined with the need for a long RF_{gap} to ensure high power-handling, limit the applicability of this approach in the present work. A second solution, illustrated schematically in (Figure 4-17.a) and presented in [120] , consists of inserting an AlN layer between the heater and the underlying dielectric. The good thermal conductivity of AlN enables it to reproduce the heat-spreading effect of the substrate independently of dielectric thickness, ensuring more homogeneous temperatures within the heater. However, this configuration also channels heat toward the RF contacts, increasing thermal losses during the heating phase. While this property is advantageous during quenching, it reduces heating efficiency, requiring higher energy input to reach the PCM melting temperature. Consequently, the temperature uniformity achieved remains lower than in the architecture that will be introduced in this section. Nevertheless, a combination of both concepts could be envisioned as a potential hybrid solution. A third approach, shown in Figure 4-17.b and described in [57], divides the PCM into multiple independent cells separated by short gaps, each equipped with its own heater. This structure provides good local control over temperature and can enhance thermal uniformity. However, it introduces significant voltage distribution issues, as most of the actuation voltage tends to drop across the first cell. Solutions such as geometry optimization or capacitive compensation can mitigate this effect but increase the design complexity and often lead to performance degradation.



(a) (b)

Figure 4-17: *(a) Example of a common layout incorporating an AlN diffusion layer to mimic the substrate's thermal behavior. (b) Switch structure dividing the PCM into multiple sections, effectively equivalent to several switches connected in series.*

To overcome these limitations, a new heater architecture has been developed. The concept involves dividing the rectilinear portion of the heater into multiple parallel branches, all connected to the same extremity. In other words, these designs can be regarded as modified single-branch heaters from which one or more central sections have been removed. Figure 4-18.b presents an example of such a configuration, featuring a double-branches heater. Variants incorporating more than two branches can also be designed following the same principle.

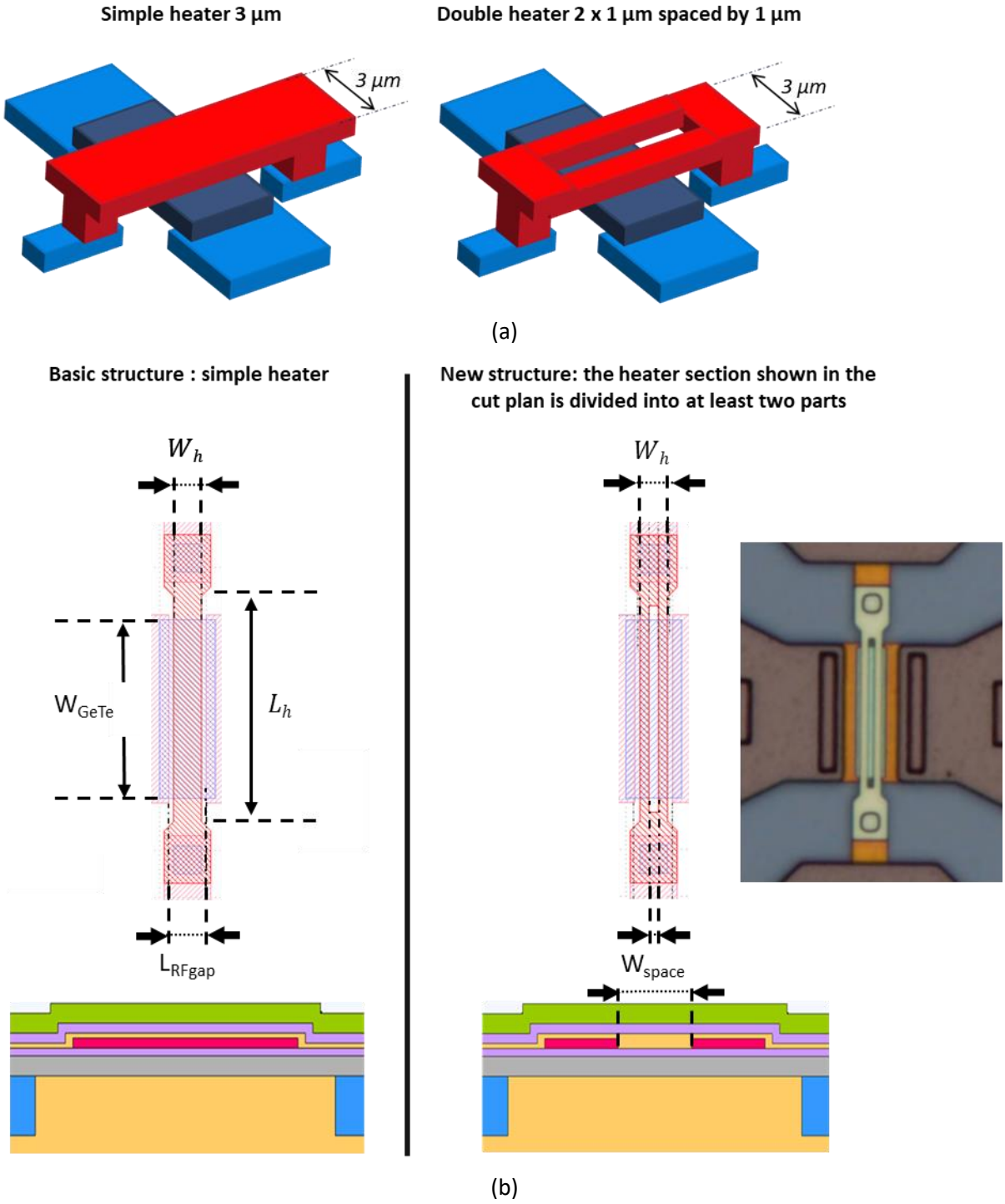


Figure 4-18: *(a) 3D views comparing a conventional single-branch heater (left) and a double-branches heater architecture (right). (b) Cut-plane views of switches using a single-branch heater (left) and a double-branch heater (right), accompanied by a top-view photograph of a CEA-fabricated device implementing the double-branch design.*

This new multi-branch heater architecture is expected to improve both thermal uniformity and energy efficiency by redistributing heat more evenly across the PCM. To validate these assumptions and quantify the thermal benefits of this design, detailed simulations were conducted using both double- and triple-branches configurations, as presented in the following section.

4.6.2 Temperature homogenization – Simulation with 3D slice model

Building on the observations made in the previous section, this part focuses on quantifying the temperature homogenization achieved through the multi-branch heater architecture. The first stage of this investigation was carried out using 3D slice models in COMSOL. A switch model using GeTe as the PCM and a 4 µm-long RF_{gap} was analyzed in three variants: a single-branch heater, a double-branches heater, and a triple-branches heater. Each design had the same overall coverage —the sum of the widths of all branches and the gaps between them— equal to 3 µm. These three models are illustrated in Figure 4-19.a.

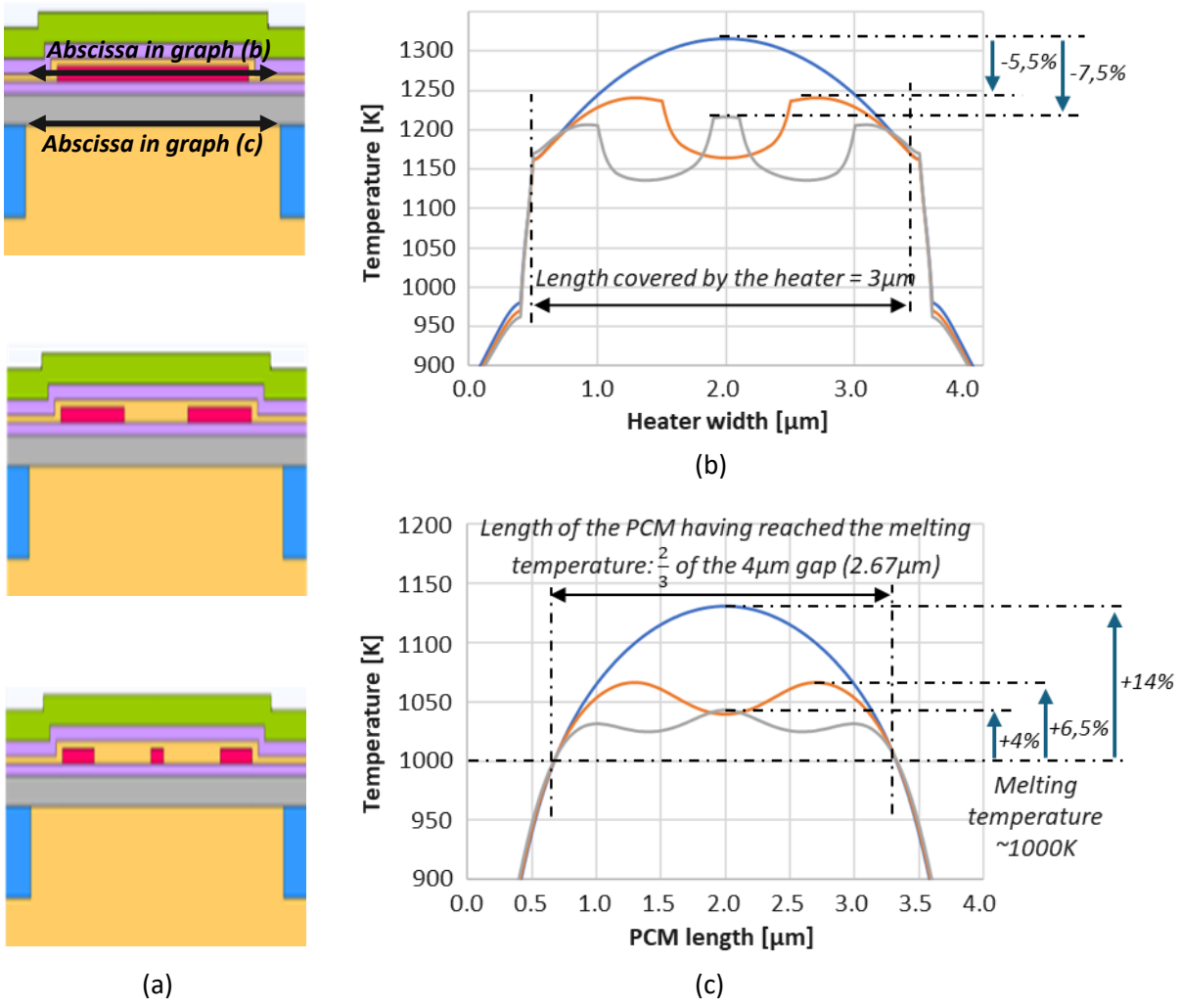


Figure 4-19: *(a) Layouts of switches employing heaters with one, two, or three branches. (b) Temperature distribution along the width of the heater defined by the top-left schematic, measured at the end of a 400 ns-long amorphization pulse. (c) Temperature distribution along the length of the PCM defined by the top-left schematic, measured at the end of a 400 ns-long amorphization pulse.*

A 400 ns-long amorphization pulse was applied to each configuration with the goal of delivering sufficient heat to melt two-thirds of the PCM above the RF_{gap}. Temperatures were measured just before the quench step, when the switches reached their maximum thermal load. Measurements were taken along a line at the mid-height of the heater spanning its width, and along a line at the base of the PCM extending over the RF_{gap} length. These readings were then superimposed in a common graph to compare temperature homogeneity across the three designs.

Figure 4-19.c shows the temperature profiles in the PCM. In the single-branch heater, the center of the PCM reached a maximum temperature of 1130 K, representing a 14 % excess over the melting point. By contrast, in the double-branches heater —designed with the same total coverage but with the central part removed— the temperature excess at the center was reduced. The maximum temperature was instead located under the two heater branches, exceeding the melting point by only 6.5 %. Finally, the triple-branch architecture further reduced the branch widths, introducing a smaller central branch to ensure sufficient heating of the PCM center. This design limited the temperature excess to 4 % above melting. These results demonstrate that splitting the heater into multiple branches effectively homogenizes temperature in critical regions of the switch.

Similar trends were observed within the heater itself, as shown in Figure 4-19.b. The difference between the maximum and minimum temperatures along the heater serves as a metric for thermal uniformity. The single-branch heater exhibited a temperature variation of 145 K, whereas the double-branches and triple-branches heaters reduced this difference to 70 K and 45 K, respectively. The maximum temperatures in the double-branches and triple-branches designs were therefore 5.5 % and 7.5 % lower than in the single-branch heater, which improves reliability by reducing the risk of heater damage. Further splitting the heater could continue to reduce temperature excesses and enhance PCM uniformity, but branch widths must remain compatible with fabrication constraints to ensure precision.

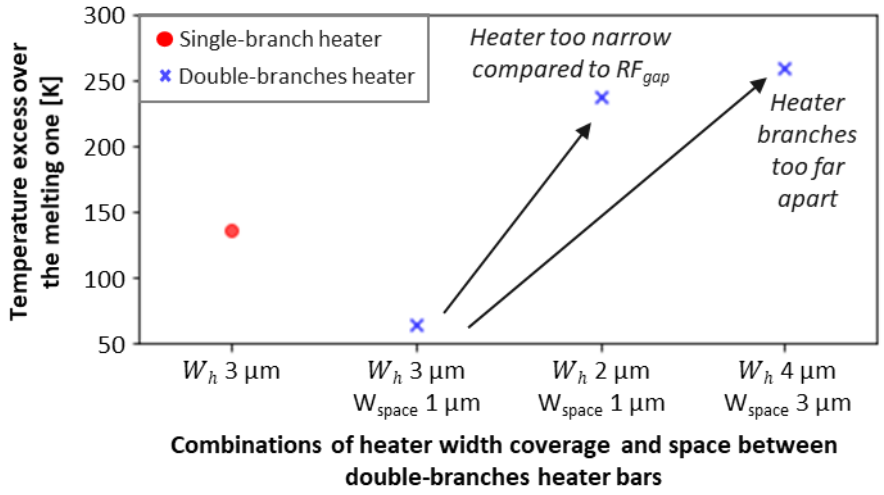


Figure 4-20 : *Temperature excess above the melting point (1000 K) observed at the base of the PCM for switches with various single-branch and double-branches heater designs.*

When designing a double-branches heater, careful attention must be paid to both the widths of the branches and the spacing between them. Sufficient separation is required to reduce temperature excesses in the central PCM region, but excessive spacing prevents adequate heating in these areas. To optimize these parameters, a study was conducted varying three factors: heater type (single-branch or double-branches), RF_{gap} length (1 µm to 4 µm in 0.5 µm steps), and the combined coverage of heaters and inter-branch spaces. Heater coverage was modeled at 1 µm, 2 µm, 3 µm, and 4 µm, with individual double-branch widths of 0.5 µm or 1 µm, yielding inter-branch gaps from 0.5 µm to 3 µm.

This produced heater-to-RF_{gap} coverage ratios from 25 % to 100 %, with all devices designed for a 4 µm RF_{gap}. Figure 4-20 summarizes the resulting temperature excesses above the melting point for selected designs. In these plots, « W_h » denotes the total heater coverage and « W_{space} » the spacing between branches, as illustrated schematically in Figure 4-18.b.

For a single-branch heater with 3 µm coverage, the maximum temperature exceeded melting by 135.2 K. Using a double-branches heater with two 1 µm-wide branches and the same total coverage, the excess was reduced to 64 K, owing to the removal of the central part of the heater and the corresponding reduction of heat accumulation in the PCM center. Reducing the coverage to 2 µm (two 0.5 µm-wide branches) increased the temperature excess to 237.5 K, as the limited coverage failed to adequately heat the edges of the targeted PCM zone. Conversely, when the coverage matched the RF_{gap} length (4 µm) but the inter-branch spacing was 3 µm, two narrow 0.5 µm branches were too far apart to efficiently heat the PCM center, producing hot spots at the PCM edges and a temperature excess of 259.2 K.

These findings confirm that multi-branch heaters significantly improve temperature uniformity and reduce thermal stress in both the PCM and the heater. However, achieving better thermal homogeneity must not come at the cost of excessive energy demand. Therefore, the next section explores how this architectural change impacts energy consumption, both through simulations and experimental validation.

4.6.3 Energy consumption – Simulation with 3D slice model + Measurements

Building on the structural and thermal analyses discussed earlier, this section focuses on evaluating the energy efficiency of the heater architectures. As a reminder, energy consumption is strongly dependent on the maximum temperature reached in the heater. By extension, it also depends on the temperature uniformity within the PCM: more efficient heat distribution reduces the amount of energy that must be generated by the heater to achieve the target melting conditions. Using the models analyzed in Section 4.6.2 and applying the calculation method described in Section 2.1.4.4, the energy consumption of various heater configurations was evaluated. Figure 4-21.a presents the simulated results for the same switches analyzed in Figure 4-20.

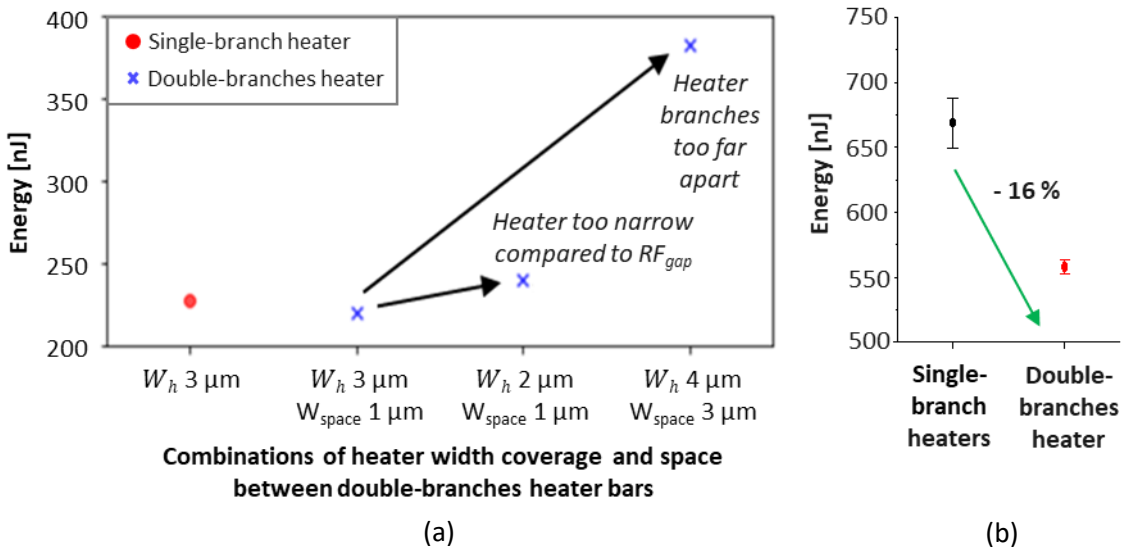


Figure 4-21: *(a) Simulated energy consumption for switches with different dimensions and heater architectures. (b) Measured energy consumption for fabricated devices with identical dimensions, comparing single-branch and double-branches heater architectures.*

The single-branch heater design required 228 nJ to melt two-thirds of the PCM. Introducing a double-branches heater reduced the energy consumption to 219 nJ, demonstrating the benefits of temperature homogenization. Reducing the total heater coverage to 2 µm increased consumption to 240 nJ, while widening the spacing between the double-branches significantly increased the required energy to 382 nJ. These trends highlight the importance of carefully balancing branch width and spacing to optimize energy efficiency.

To validate the simulations, energy consumption was also measured in fabricated devices. Figure **4-21**.b compares single-branch and double-branches heaters for devices with the same nominal dimensions: a 4 µm-long RF_{gap} and 3 µm heater coverage, with the double-branches heater featuring a 1 µm inter-branch spacing. Experimental results showed an average energy consumption of 670 nJ for single-branch devices, compared to 560 nJ for double-branches devices, corresponding to a 16 % reduction. These results confirm that the double-branch heater design not only improves temperature uniformity but also achieves measurable energy savings compared to the single-branch configuration.

Beyond energy efficiency, it is equally important to understand how these improvements affect the extent of PCM amorphization, which directly determines the switch's performance during operation. The following section addresses this aspect in detail.

4.6.4 Amount of PCM amorphized

Following the analysis of energy efficiency, attention is now directed toward understanding how heater geometry affects the extent of amorphization in the PCM layer. During the simulations described in the previous section, a particular behavior was observed in switches where the double-branches heater coverage matched the RF_{gap} length. In these configurations, the hottest regions of the PCM shifted toward its extremities, resulting in a larger melted zone than the initially targeted two-thirds of the PCM width. Motivated by this observation, the total width of melted PCM was evaluated for all models analyzed in the preceding simulations. Figure 4-22 presents the melted width for a selection of devices with 4 µm-long RF_{gap} and heater coverages close to or equal to the RF_{gap} length.

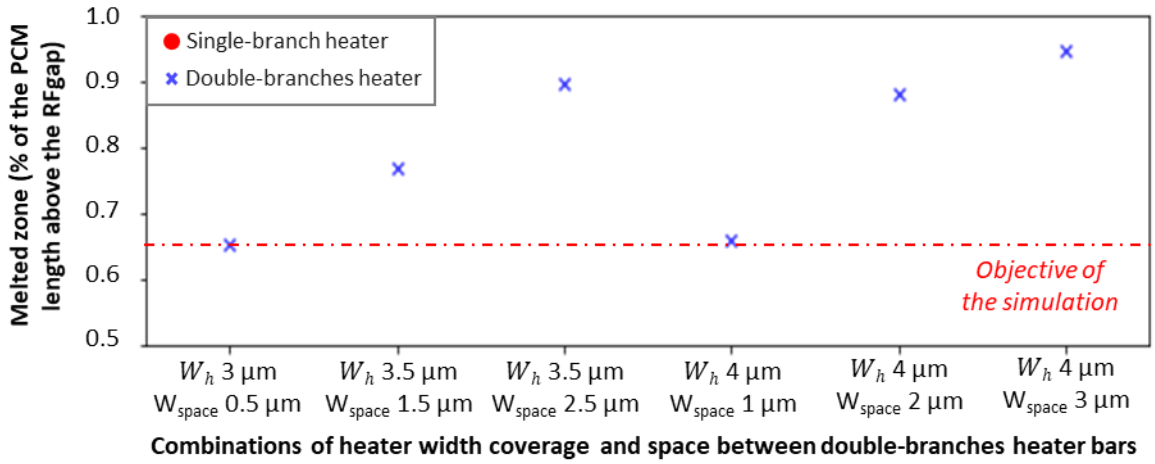


Figure 4-22: *Width of the PCM above the RF_{gap} that exceeds the melting temperature for various heater configurations, all corresponding to an RF_{gap} length of 4 µm.*

When the spacing between the two heater branches is small, the branches effectively cover the central region of the PCM. This central portion accumulates heat more quickly, reaching the melting temperature before the edges. As the spacing between branches increases, however, the extremities of the PCM become the hottest spots. At the end of the simulation, more than 66 % of the PCM above the RF_{gap} reaches the melting temperature. While this extended melting region can be advantageous

for switching, it also requires higher energy input. Figure 4-23 presents the calculated energy consumption for the same set of devices analyzed in Figure 4-22.

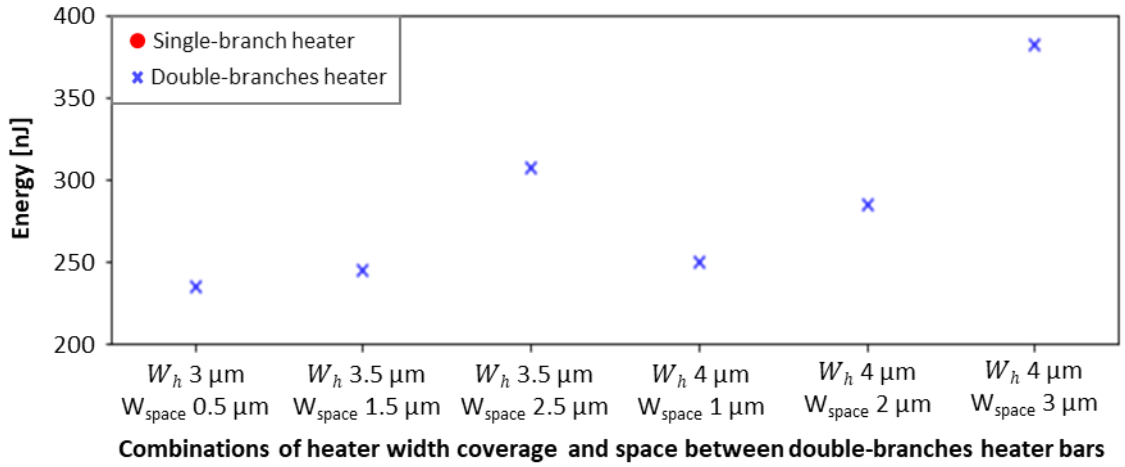


Figure 4-23: *Calculated energy consumption for different heater configurations, all corresponding to an RF_{gap} length of 4 µm.*

The results indicate that energy consumption increases exponentially as the spacing between branches grows. By analyzing these trends across all simulated models, a compromise can be defined between maximizing the melted PCM zone and minimizing energy consumption. Optimal configurations were identified for double-branches heaters with coverage of at least 80 % of the RF_{gap} and branch spacing of approximately 60 % of the total coverage. These designs allow up to 80 % of the PCM above the RF_{gap} to be melted while maintaining energy consumption below 250 nJ, demonstrating an effective balance between amorphization efficiency and energy efficiency.

These results make it possible to identify an optimal range of geometric parameters that balance heating efficiency, energy consumption, and the extent of PCM amorphization. To formalize these insights, the next section consolidates these findings into a set of design rules for optimizing the double-branch heater architecture.

4.6.5 Design rules

Based on the results presented in the previous sections, the next step involved formalizing these observations into concrete design principles. The analysis of temperature distribution, energy consumption, and the amount of amorphized PCM across all simulated models has enabled the establishment of design rules to optimize the efficiency of double-branches heaters. The primary objectives of these rules are:

- Minimize the energy required to bring a defined length of the PCM above the melting temperature.
- Achieve the most homogeneous temperature distribution within the PCM, with minimal overshoot beyond the melting temperature.

To meet these objectives, the following guidelines should be observed:

- Heater coverage: The total heater coverage should remain between the length of the PCM region targeted for melting and the length of the RF_{gap}. This ensures sufficient heating of both the central and lateral portions of the PCM, leading to more uniform temperatures and energy savings. Exceeding the RF_{gap} length would cause the heater to overlap the RF contacts, which

act as thermal sinks. In that case, part of the heat generated would be absorbed and lost, requiring additional energy to achieve the desired PCM temperature, thereby negating the efficiency advantages of a double-branches architecture and potentially creating hot spots at the extremities of the switch.

- Space between branches: The total length of the spaces separating the heater branches should remain below 50 % of the RF_{gap} length. This limitation prevents excessive temperature overshoot and ensures adequate heating of the PCM's central regions without increasing energy consumption unnecessarily.
- Space-to-coverage ratio: A ratio of approximately 60 % allows for a larger amorphized PCM region while maintaining acceptable energy requirements and temperature control.

By following these rules, the double-branch heater design provides a clear path toward improved energy efficiency and enhanced amorphization control. To confirm that these structural benefits also translate into superior electrical performance, the following section presents experimental measurements of S-parameters and OFF-state resistance.

4.6.6 S-Parameters and resistance in the OFF state - Measurements

To verify the electrical advantages of the optimized heater architecture, the following analyses compare the OFF-state resistance and S-parameters of fabricated devices incorporating either single- or double-branch heaters. Following the measurement procedures described in Section 2.2.1, the OFF-state resistances of fabricated devices with double-branches heaters were measured and compared to those of devices with single-branch heaters for the same sets of dimensions. The results indicate that the two-branch architecture enables the switches to reach higher R_{OFF} values. Figure 4-24 presents the R_{OFF} characterization for the same two groups of switches analyzed in Figure 4-21. Switches with double-branches heaters reached values above 10^6 Ω, whereas devices with single-branch heaters could not achieve this threshold.

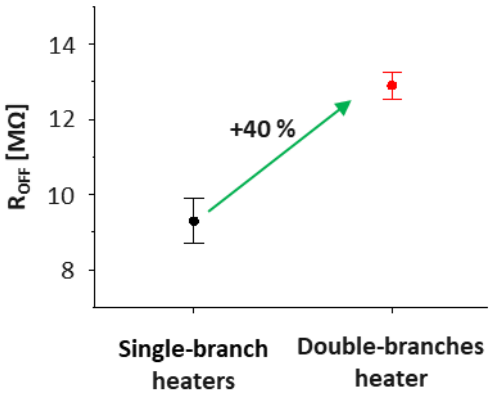


Figure 4-24: *Heater energy consumption measured for two sets of devices with identical designs, differing only in the type of heater. Multiple devices were tested for each heater type to ensure statistical consistency.*

The adoption of the double-branches heater architecture improved R_{OFF} by approximately 40 % which aligns with the temperature homogenization observed in Figure 4-19.b. The more uniform temperature distribution reduces heat excess, enabling the melting and quenching process to occur in a cooler environment. This accelerates the amorphization process, resulting in a larger portion of the PCM being amorphized, which in turn enhances the isolation and power-handling of the switches.

The next step involved characterization of the S-parameters to extract the R_{ON} and C_{OFF} values for both heater architectures, following the method described in Section 2.2.2. Devices with RF_{gap} lengths of

2 µm, 3 µm, and 4 µm were tested, with heater coverages of either 2 µm or 3 µm. For double-branches heaters, a 2 µm coverage corresponds to two 0.5 µm branches separated by a 1 µm space, while a 3 µm coverage corresponds to two 1 µm branches separated by 1 µm. The C_{OFF} was extracted at 5 GHz from devices after a single switching cycle, and the R_{ON} was extracted at 5 GHz from as-fabricated devices after de-embedding using a thru-line structure. Figure 4-25 summarizes R_{ON} and C_{OFF} for four sets of dimensions, comparing single-branch and double-branches heaters.

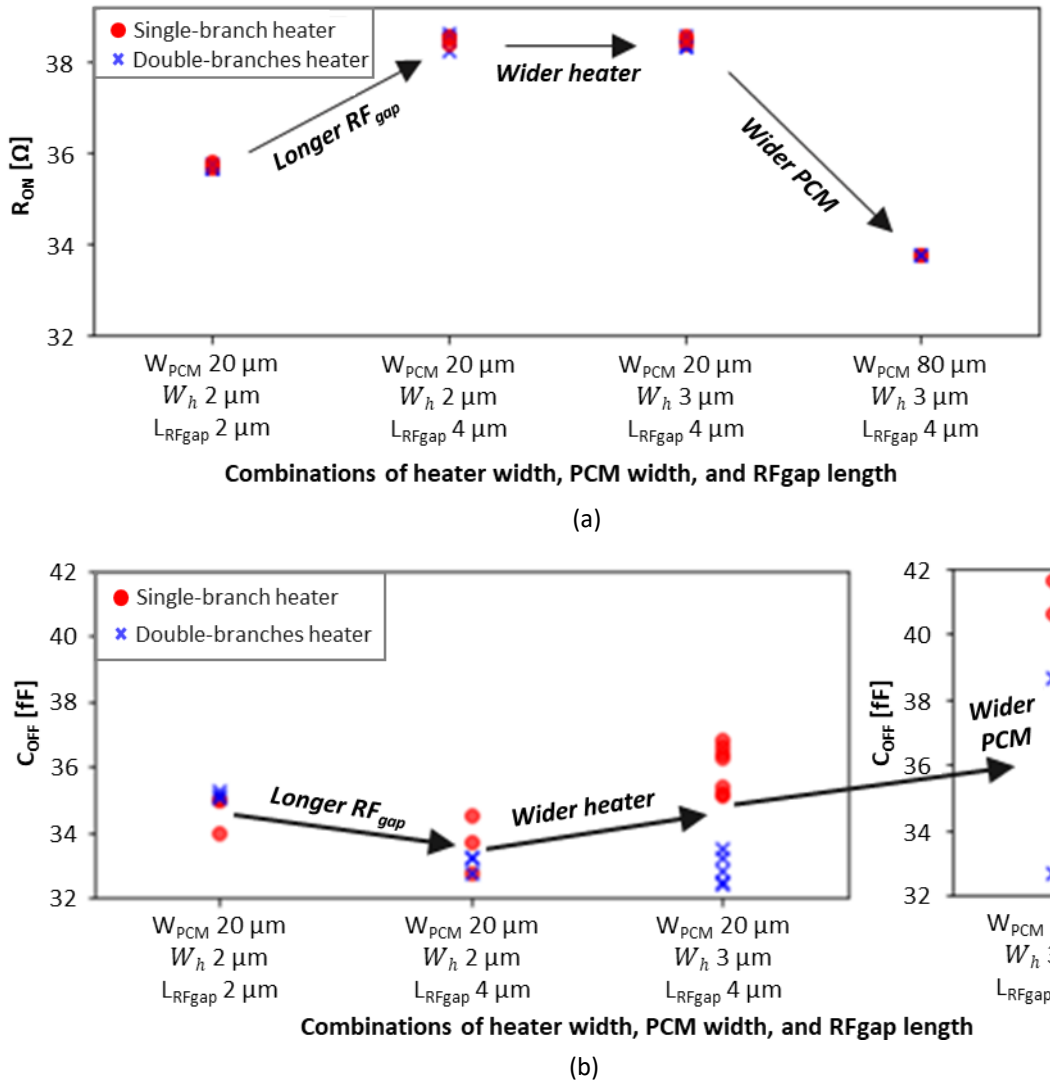


Figure 4-25 : *Influence of the heater architecture on switch performance for different sets of dimensions: (a) ON-state resistance and (b) OFF-state capacitance, comparing single-branch and double-branches heater designs.*

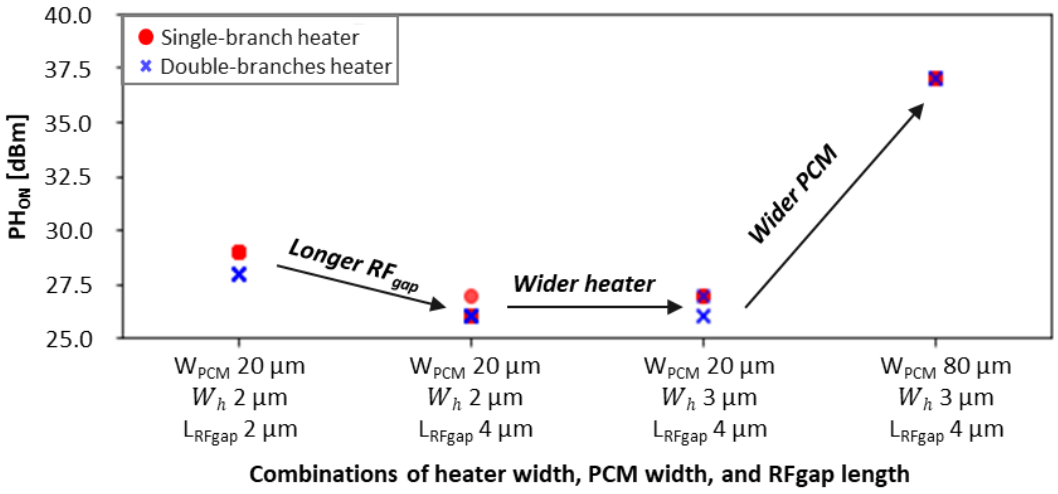
In the first design, with a 20 µm-wide PCM and a 2 µm heater coverage matching the RF_{gap} length, C_{OFF} values were approximately 11.5 fF for both architectures. The short RF_{gap} made it difficult for either heater to sufficiently heat the PCM extremities, explaining the similar performance. Extending the RF_{gap} to 4 µm resulted in lower C_{OFF} values of 10.4 fF, since a longer amorphized zone reduces parasitic capacitances by moving crystalline regions farther from the heater. Increasing the heater width to 3 µm introduced differences: the single-branch heater reached a minimum C_{OFF} of 11.6 fF, while the double-branches heater achieved 10.2 fF. The space between branches remained unchanged, confirming that the extra tungsten in the center of single-branch heaters does not contribute significantly to parasitic capacitance; instead, the improved amorphization from the double-branches

design is the main factor reducing C_{OFF}. Increasing the PCM width to 80 µm further widened the performance RF_{gap}, with the best single-branch device at 40.5 fF versus 32.7 fF for the best double-branches device, a 20 % improvement.

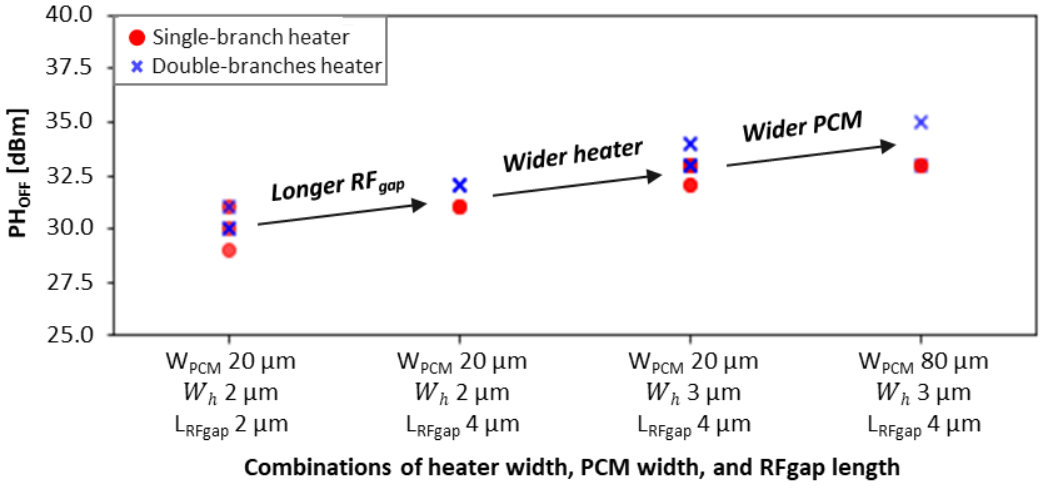
The R_{ON} values, as shown in Figure 4-25.a, are similar between single-branch and double-branches devices for each set of dimensions. This is expected because the ON-state resistance depends on the crystalline PCM, which is fully crystallized regardless of heater architecture. R_{ON} increases with longer RF_{gap} and decreases with wider PCM. Since the FOM depends on both C_{OFF} and R_{ON} values, it is evident that the double-branches design improves this key performance metric by lowering parasitic capacitance without negatively impacting ON-state resistance.

4.6.7 Power-handling in ON and OFF states - Measurements

After establishing the electrical benefits of the double-branch architecture, this section evaluates its impact on the power-handling performance of the switches in both ON and OFF states.



(a)



(b)

Figure 4-26 : *Influence of the heater architecture on the power-handling capabilities of PCM-based RF switches in (a) the ON-state and (b) the OFF-state, for different sets of dimensions.*

Measurements were performed on the same set of devices analyzed in the previous section. In the results presented in Figure 4-26, the PH_{OFF} values correspond to the devices used for C_{OFF} extraction, while the PH_{ON} values correspond to those used for R_{ON} extraction. For devices with a short RF_{gap} of 2 µm, the OFF-state power-handling is similar for both single-branch and double-branches heater designs. This is consistent with earlier observations, where differences between architectures are less pronounced with shorter RF_{gap}. Increasing the RF_{gap} enhances PH_{OFF} for both heater types because a larger PCM portion becomes available for amorphization. The double-branches heaters, by providing a more homogeneous temperature distribution, further improve the amount of amorphized PCM, thereby increasing PH_{OFF}. Additionally, wider heater coverage contributes to higher PH_{OFF} by supplying more heat to the PCM. Overall, the double-branches heater maintains an advantage over the single-branch design, with switches reaching 33 dBm. The highest PH_{OFF} recorded among all fabricated devices was 35 dBm, for a switch with a double-branches heater, an RF_{gap} of 4 µm, a 3 µm heater coverage (two 1 µm-wide branches), and a PCM width of 80 µm. In contrast, the ON-state power-handling behaves similarly to the R_{ON} parameter, depending only on the amount of crystalline PCM and remaining largely independent of heater design. As with R_{ON}, a longer RF_{gap} reduces PH_{ON} while a wider PCM increases it. Multiple devices were able to withstand the setup limit value of 37 dBm. Overall, these measurements confirm that using multi-branch heaters not only improves temperature homogenization and amorphization efficiency but also contributes to enhanced power-handling performance, particularly in the OFF-state.

4.7 Conclusion

Throughout this chapter, multiple factors influencing the performance of PCM-based RF switches have been systematically investigated, leading to tangible strategies for device improvement. The introduction of a top AlN capping layer emerged as a critical modification, enhancing thermal dissipation and homogenizing temperature distribution in both the heater and PCM. This improvement reduces localized hot spots, shortens quench durations, and ultimately enhances the reliability of the switches. Complementing this material optimization, reducing the dielectric thickness beneath the RF contacts brings the PCM closer to the substrate, accelerating heat removal during the quench phase and further contributing to improved thermal management. When these two optimizations are combined, the resulting devices exhibit a 6 dBm improvement in OFF-state power-handling, with certain switches achieving 31 dBm in both ON and OFF states for configurations featuring 4 µm-long RF_{gap} and 3 µm-wide heaters.

Beyond structural and material considerations, the analysis of amorphization pulse duration provided a deeper understanding of dynamic thermal behavior. Simulations indicate that a pulse duration of approximately 100 ns offers an optimal balance between energy consumption, maximum temperature control, and quench duration, ensuring efficient and uniform PCM phase transition.

A major advancement presented in this chapter is the introduction of multi-branch heater architectures. By splitting the heater into two or more branches, temperature homogenization across the PCM is significantly improved. This design reduces localized overheating, increases the effective length of the amorphized PCM region, and decreases parasitic capacitances, yielding a notable reduction in C_{OFF}. Measurements confirm that double-branch heater configurations enhance OFF-state isolation, improve the $R_{ON} \times C_{OFF}$ FOM, and contribute to higher power-handling capabilities, with some devices reaching up to 37 dBm in series structures. Additionally, the improved thermal uniformity and energy distribution in multi-branch designs translate directly into lower energy consumption and enhanced device reliability.

In conclusion, the integration of material, dimensional, pulse, and architectural optimizations forms a cohesive strategy to advance PCM-based RF switches. By systematically addressing heat management, energy efficiency, and temperature control, this chapter establishes design principles that enable robust, high-performance devices, paving the way for future developments in high-power RF applications.

Chapter 5
Phase-Field simulations

Simulating phase-change materials (PCMs) requires careful adaptation of their properties depending on the focus of the study. For crystallization studies, the amorphous properties of the PCM —such as GST or GeTe— are assigned, whereas for amorphization studies, the crystalline properties are used. While this approach allows the simulations to proceed, it imposes a fundamental limitation: the material retains the same set of properties throughout the simulation. For example, an initially crystalline GeTe maintains its crystalline characteristics even after undergoing an amorphization pulse. This limitation arises from the fact that conventional simulation tools, such as COMSOL, do not inherently reproduce the dynamic behavior of PCMs. The closest available mechanism is the definition of discrete material phases associated with temperature ranges —for instance, liquid water above 0 °C and solid water below 0 °C. As a result, when attempting to simulate PCM behavior, the material begins in the crystalline state at room temperature, adopts molten properties once heated above its melting point, but immediately reverts to the crystalline state as soon as the temperature falls below that threshold, rather than retaining amorphous properties.

To address this challenge, a two-dimensional Phase-Field model —building on frameworks developed for phase-change memories by Olga Cueto, Veronique Sousa, Gabriele Navarro, and Serge Blonkowski in [121]— is implemented to reproduce switching behavior more accurately. The model remains two-dimensional due to the substantial computational resources required by the extremely fine mesh necessary to capture nucleation and growth dynamics realistically. A consequence of this 2D configuration is that only a single device face is represented. Accordingly, the natural Joule heating effect —previously modeled with a terminal and a ground— must be replaced by a simplified heat source applied directly to the heater.

Building on this foundation, the chapter is organized as follows. Section 5.1 presents the theoretical framework of the Phase-Field model, detailing the two key mechanisms of PCM phase transitions: the growth of crystalline regions and the nucleation of new crystalline domains. Section 5.2 focuses on the application of this theory to our work, describing how the Phase-Field kinetics are coupled with finite-element thermal simulations to reproduce the amorphization and recrystallization processes in GeTe- and GST-based devices. This section also outlines the simulation process, including the alternation of nucleation and growth computations, and presents the results of the coupled simulations, highlighting differences in PCM behavior and their implications for device performance.

5.1 Theoretical analysis

To capture the dynamic behavior of PCMs during operation, their phase change is modeled in real time. The objective is to continuously adapt the properties of each point within the PCM according to its instantaneous state —molten, amorphous, or crystalline. To achieve this, a Phase-Field model is used, which reproduces two main phenomena: nucleation and growth. Nucleation refers to the formation of small crystalline regions, or nuclei, within the PCM. These nuclei form in areas where the temperature lies between the crystallization and melting temperatures. The growth process describes the time expansion of these nuclei, as well as the enlargement of any initially crystalline regions. To model nucleation and growth, the system identifies regions that exceed the melting temperature and assigns them amorphous properties. Upon cooling, these regions either crystallize —if the

temperature remains between the melting and crystallization points long enough— or retain their amorphous structure once they return to room temperature. The pathway followed depends primarily on two factors: the Phase-Field equations and the intrinsic properties of the PCM.

Within this framework, the model defines the representation of the phase state at each point in the PCM and its temporal evolution. This naturally leads to the first detailed mechanism: the growth of crystalline parts within the PCM.

5.1.1 Growth of PCM crystalline parts

To describe the phase state, the model assigns an order parameter η to each point of the PCM. Disordered, high-resistance structures (amorphous or molten) are represented by η = 0, while ordered, low-resistance crystalline structures correspond to η = 1. At the interface between two states, η takes values between 0 and 1, allowing for the modeling of a diffuse interface rather than a sharp boundary. This approach simplifies numerical computation while maintaining physical accuracy. The evolution of η is directly linked to the system's free energy, expressed as:

$$\frac{\partial \eta}{\partial t} = -L_\eta \left(\frac{\delta F}{\delta \eta}\right) \tag{30}$$

Here, L_η is a positive kinetic coefficient that determines the rate of system evolution. It depends on the crystal growth velocity V_i, the curvature radius of the nucleus interface R_c, (also reffered to as critical nucleus radius), and the energy gradient coefficient κ, according to:

$$L_\eta = \frac{V_i \, R_c}{\kappa} \tag{31}$$

A larger L_η indicates a faster phase change process, while the negative sign denotes energy dissipation. The crystal growth velocity V_i depends on the energy difference between the two phases, denoted ΔG, and is defined as:

$$V_i = d\mu \left(1 - e^{\frac{\Delta G d^3}{k_b T}}\right) \tag{32}$$

where μ is a temperature-dependent function representing the frequency of atomic attachment to a critical nucleus, d is the interatomic spacing, and k_b is the Boltzmann constant. The parameter ΔG denotes the volumetric Gibbs free energy difference between the crystalline and liquid phases and represents the thermodynamic driving force for crystallization. It depends on the thermal properties of the material —namely, the latent heat of fusion L_m and the melting temperature T_m— and is given by:

$$\Delta G = L_m \left(1 - \left(\frac{T}{T_m}\right)\right) \tag{33}$$

The free energy functional $F(\eta)$ is expressed as:

$$F(\eta) = \int_V \left(f(\eta) + \frac{\kappa}{2} \left| \nabla \eta \right|^2\right) dV \tag{34}$$

Here $f(\eta)$ represents the local free energy potential that describes the system in a homogeneous state ($\eta = 0$ or 1), while $\frac{\kappa}{2}|\nabla \eta|^2$ accounts for the interfacial energy when the system is non-homogeneous (0 < η < 1). The smoothing effect of the second term on $F(\eta)$ depends directly on the variation of η. Using variational calculus, Equation (34) yields:

$$\frac{\delta F(\eta)}{\delta \eta} = \frac{\partial f(\eta)}{\partial \eta} - \kappa \nabla^2 \eta \tag{35}$$

By combining (30) and (35), we obtain the Allen–Cahn equation, which governs the Phase-Field evolution during the crystal growth process:

$$\frac{\partial \eta}{\partial t} = -L_\eta \left(\frac{\partial f(\eta)}{\partial \eta} - \kappa \nabla^2 \eta \right) \tag{36}$$

In summary:

- $\boldsymbol{\frac{\partial \eta}{\partial t}}$ represents the temporal evolution of the phase change (i.e., how the local state η evolves).
- $\boldsymbol{L_\eta}$ determines the rate at which the system evolves toward a homogeneous state (η = 0 or 1).
- $\boldsymbol{\frac{\partial f(\eta)}{\partial \eta}}$ describes the change in free energy, typically modeled as a double-well potential containing two stable phases separated by an energy barrier, ensuring that η evolves toward one of the two stable states.
- $\boldsymbol{\kappa \nabla^2 \eta}$ represents the energy cost required to maintain a diffuse interface between phases, where a higher κ value produces a smoother interface.

Next, to evaluate the influence of the thermal properties of the PCM on the crystal growth mechanism, the heat equation is used:

$$\rho C_\rho \frac{\partial T}{\partial t} + \nabla\left(-k_{th}\overrightarrow{\nabla T}\right) = \sigma(\nabla V)^2 + L_m h'(\eta) \frac{\partial \eta}{\partial t} \tag{37}$$

The terms in this equation have the following meanings:

- $\boldsymbol{\rho C_\rho \frac{\partial T}{\partial t}}$ represents the rate of change of thermal energy with time. Here, ρ is the density of the PCM, and C_ρ is its specific heat (the amount of heat required to raise the temperature of a unit mass by 1 °C). In regions of the PCM that remain in steady state, this term can be neglected.
- $\boldsymbol{\nabla\left(-k_{th}\overrightarrow{\nabla T}\right)}$ describes heat diffusion within the material, governed by its thermal conductivity k_{th}. The negative sign simply indicates the direction of heat dissipation. In thin-film configurations, this term can often be neglected due to the limited temperature gradients across the material.
- $\boldsymbol{\sigma(\nabla V)^2}$ corresponds to the Joule heating effect, which occurs when an electrical current passes through the PCM. In this expression, σ is the electrical conductivity and V is the electric potential. Since the models considered here operate through indirect heating, this term is omitted.
- $\boldsymbol{L_m h'(\eta) \frac{\partial \eta}{\partial t}}$ accounts for the absorption or release of latent heat L_m defined as the thermal energy required to induce a phase change without changing temperature —for instance, ice absorbs heat at 0 °C to melt, while its temperature remains constant throughout the process. The function $h'(\eta)$represents the rate of change of the phase fraction; a higher value indicates that a larger portion of the PCM undergoes a phase transformation within a short time. In homogeneous PCM regions, this term can be neglected.

At the interfaces between two phases, the governing equation therefore becomes:

$$\rho C_\rho \frac{\partial T}{\partial t} + \nabla\left(-k_{th}\overrightarrow{\nabla T}\right) = L_m h'(\eta)\frac{\partial \eta}{\partial t} \tag{38}$$

Rearranging the terms yields the following expression for the evolution of the order parameter η:

$$\frac{\partial \eta}{\partial t} = \frac{\left(\rho C_\rho \frac{\partial T}{\partial t} + \nabla\left(-k_{th}\overrightarrow{\nabla T}\right)\right)}{L_m h'(\eta)} \tag{39}$$

Because the sign preceding k_{th} merely indicates whether heat is absorbed or dissipated, this expression shows that a higher thermal conductivity promotes a stronger evolution of the order parameter η. Consequently, PCMs with higher thermal conductivity exhibit faster nucleation and crystal growth. Conversely, a higher latent heat slows down the evolution of η, thereby reducing the growth rate of both nuclei and crystalline domains within the PCM.

In summary, the crystal growth mechanism describes how existing crystalline regions expand once the phase transition has begun. To fully capture the overall crystallization dynamics of PCMs, however, it is also necessary to consider how these crystalline regions first appear within the amorphous matrix.

5.1.2 Nucleation in the PCM

The second fundamental mechanism, nucleation, governs this initial formation of crystalline regions within the PCM. It is implemented using the nucleation rate equation, which defines the number of nuclei formed within a given volume per unit time. During this process, atoms and molecules form small aggregates of a new phase inside the material. These aggregates must reach a specific size — known as the critical radius— to become stable and capable of growing further over time. If their initial size is below this threshold, the clusters dissolve back into the original phase. The nucleation rate R is expressed as:

$$R = N_s Z \mu e^{\left(-\left(\frac{\Delta G^*}{k_b T}\right)\right)} \tag{40}$$

where:

- $\boldsymbol{N_s}$ is the number of potential nucleation sites per unit volume (in the model, this corresponds to the number of mesh elements).
- $\boldsymbol{Z}$ is the Zeldovich factor, representing the probability that a nucleus reaching the critical radius continues to grow rather than dissolve.
- $\boldsymbol{\mu}$ is the parameter defined in Equation (32), describing the frequency of atomic attachment.
- $\boldsymbol{\Delta G^*}$ is the energy barrier that must be overcome for a stable nucleus to form

For example, a nucleation rate of R = 1000 $m^{-3}.s^{-1}$ indicates that, on average, one thousand stable nuclei form in one cubic meter of material during one second. Similar to the Allen–Cahn equation governing crystal growth, the nucleation rate also depends on the thermal properties of the PCM through the nucleation energy barrier, defined as:

$$\Delta G^* = \frac{4\sigma_a^3}{27\Delta G^2} \tag{41}$$

where σ_a is the interfacial energy between two adjacent phases.

Using these relationships —while maintaining T between the melting temperature T_m and the crystallization temperature to allow nucleation— the influence of thermal properties on the nucleation rate can be determined. A higher L_m value increases the value of ΔG, which in turn decreases $\Delta G^*$and therefore enhances the nucleation rate. Similarly, lower temperatures or higher melting temperatures produce the same effect by increasing the $\frac{T}{T_m}$ ratio, thereby promoting the formation of stable nuclei within the PCM.

Together, the nucleation and crystal growth mechanisms form the theoretical foundation required to describe the complete phase-change process in PCMs. The interplay between these two phenomena determines the material's overall crystallization dynamics during heating and cooling cycles. Building on this theoretical framework, these kinetic relations have been implemented in our numerical models to reproduce realistic phase transitions in GeTe- and GST-based devices.

5.2 Application to PCM-based RF switches models

5.2.1 Coupling finite element simulation with the Phase-Field model

The implementation of these kinetic relations in a device-level simulation requires coupling the Phase-Field model with a finite-element thermal solver. By integrating nucleation and crystal growth dynamics with the local temperature distribution, the model can capture the material-specific recrystallization behaviors observed in PCMs. In this work, the primary PCM studied is GeTe, while GST has also been investigated for comparison. According to the literature, these two materials exhibit distinct recrystallization behaviors during the quenching phase of an amorphization step. GST primarily recrystallizes through nucleation rather than through the growth of the regions that remained crystalline after melting. In contrast, GeTe —owing to its higher thermal conductivity, latent heat of fusion, and melting temperature— exhibits a significantly higher crystal growth rate than GST [122]. Its recrystallization is therefore mainly driven by the growth of pre-existing crystalline regions. Consequently, when implementing the phase-change mechanisms in our COMSOL Multiphysics simulation models, it was essential to ensure that this difference in recrystallization behavior was accurately reproduced. This was achieved by adjusting the thermal properties, viscosities, and interfacial energies specific to each material.

To validate the equations used in the model, a Python script was developed to plot the nucleation rate (Equation (40)) and the crystal growth velocity (Equation (32)) for both materials using their characteristic parameters listed in Table 5-1.

Table 5-1: *Material parameters of GeTe and GST used in the phase-change simulations.*

Description	Symbol [unit]	GST	GeTe
Density	ρ [kg/m^3]	6150	5770
Interatomic distance	d [A]	3	3
Melting temperature	T_m [K]	880	997
Latent heat of melting	L_m [J/m^3]	1.1 10^9	1.36 10^9
Glass temperature	T_g [K]	353	373
Viscosity parameter a	a	4.2	4.9
Viscosity parameter b	b	2.4	2.7
Interface energy crystal/amorphous	$\frac{\kappa}{2}\lvert\nabla\eta\rvert^2$ [J/m^2]	0.1	0.13

The resulting plots are presented in Figure 5-1.

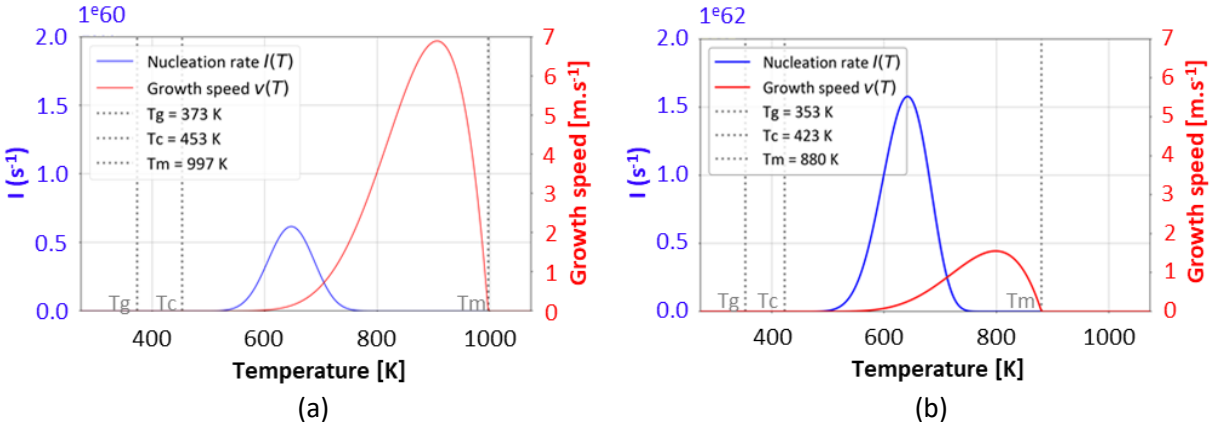


Figure 5-1: *Nucleation rate and crystal growth velocity as a function of temperature for (a) GeTe and (b) GST. The glass-transition temperature (Tg), crystallization temperature (Tc) and melting temperature (Tm) for each material are indicated below the horizontal axis.*

As expected, in these graphs, GST nucleation rate is higher than that of GeTe; meanwhile the crystal growth velocity is lower.

Regarding the implementation of the phase-change mechanisms in COMSOL, the main objective was to simulate the amorphization process of a PCM according to the following sequence:

- Begin with a fully crystalline PCM
- Apply heating until a significant portion of the PCM melts
- Allow the material to cool, so that the previously molten regions undergo partial recrystallization, leaving a portion of the PCM amorphous once it returns to room temperature. During this cooling phase, the recrystallization behavior of each PCM (either nucleation-driven for GST or growth-driven for GeTe) must be faithfully reproduced.

To accomplish this, the phase-change mechanism was implemented in COMSOL following the methodology proposed in [121] using two coupled components corresponding to the nucleation and crystal growth equations described in the theoretical analysis section. The first component, which models the entire switch in two dimensions, governs the amorphization pulse through a heat source applied to the heater. The power of this heat source is directly controlled by the pulse profile. When the pulse amplitude is zero, the switch remains at room temperature, meaning that the quenching phase occurs only during the descending ramp of the pulse. Because thermal inertia vanishes at the end of the ramp, the cooling (downward) ramp was set longer than the heating (upward) ramp to allow sufficient time for amorphization and recrystallization. The pulse power was tuned such that the molten regions of the PCM were comparable between GST and GeTe. For realistic thermal behavior, the central region of the PCM must be fully melted across its thickness, while the areas above the RF contacts —which act as efficient heat sinks— remain crystalline. The regions above the RF_{gap} but close to the contacts should melt only in their upper portion while remaining crystalline at the bottom. Any area that reaches the melting temperature adopts the properties of a high-resistivity amorphous phase. This first component also governs the nucleation process. The second component, which models only the PCM itself, handles the crystal growth mechanism. In this module, a finer mesh is employed due to the interatomic distance used in the Allen–Cahn equation, set to 1.1 nm. Consequently, the mesh elements have a size of approximately 1 nm^2.

This level of spatial refinement leads to high computational resource consumption. To mitigate this, a two-step simulation approach is adopted. The heating phase is computed using a stationary solver, while the quenching phase is simulated using a transient solver.

5.2.2 Simulation process

During the simulation, the two components are executed alternately, as illustrated in Figure 5-2.

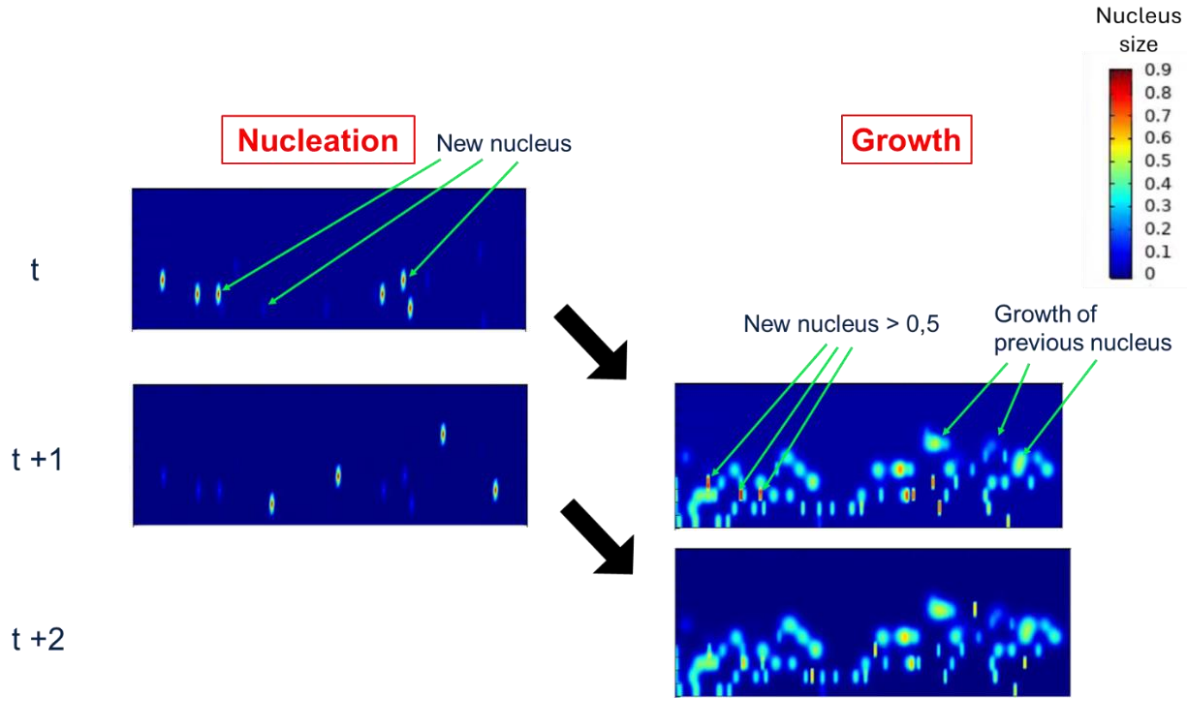


Figure 5-2: *Phase-change operation as implemented in the simulation models.*

In the first step, nuclei are generated within the PCM regions whose temperatures lie between the crystallization and melting temperatures. The natural variability in nucleus size observed experimentally is reproduced by assigning a random value between 0 and 1 to each nucleus. The expected number of critical nuclei generated during a given time step, denoted N, within a unit volume h, is defined by:

$$N(x, y, z) = R.dt.h^3 \quad (42)$$

where R represents the nucleation rate defined in Equation (40). At the following time step, nuclei associated with a random value of 0.5 or greater are considered to have reached the critical size and therefore continue to grow. In contrast, those with a value below 0.5 are regarded as subcritical and progressively dissolve back into the initial phase. The simulation then returns to the first component to perform a new nucleation cycle before proceeding to the next time step, repeating this sequence until the end of the amorphization pulse. Throughout this process, all PCM regions that transform into nuclei adopt the crystalline properties of the material.

With the nucleation and growth components operating in alternating time steps, the simulation captures the dynamic evolution of the PCM during an amorphization pulse. This framework makes it possible to observe how these mechanisms manifest in the spatial and temporal distributions of molten, amorphous, and crystalline regions within GeTe and GST.

5.2.3 Application to GeTe and GST

Using this approach, amorphization simulations were performed with GeTe and GST as the PCMs. The design of the 2D model employed for these simulations is shown in Figure 5-3, alongside a photograph of a fabricated device from which this design is derived. However, only half of the device was modeled to reduce computational resource consumption. Consequently, the temporal evolution of the PCM states during an amorphization pulse was examined within this half of the PCM. The specific observation region is indicated by the black rectangle in Figure 5-3.b.

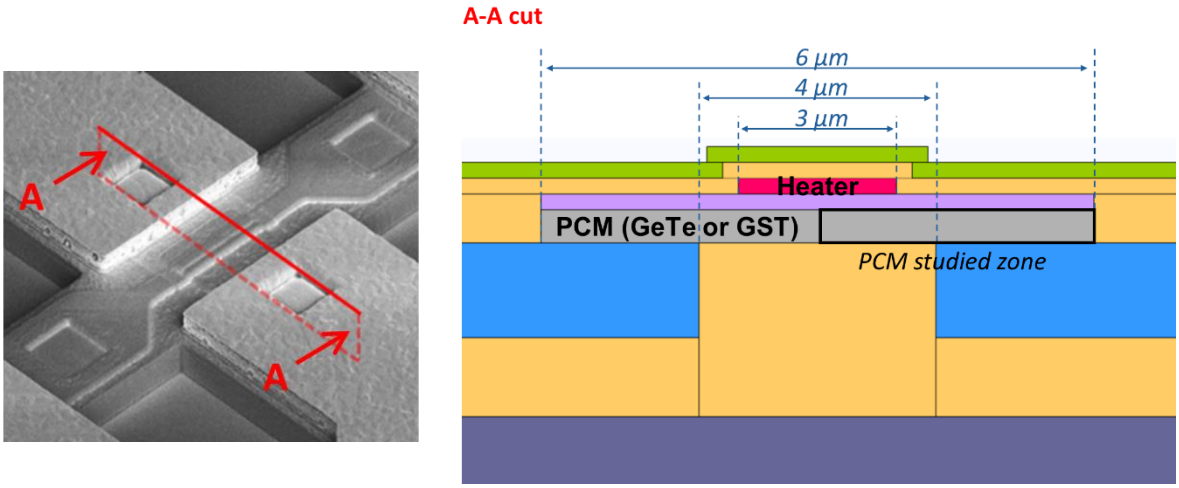


Figure 5-3: *(a) Photograph of a PCM RF switch with a red rectangle indicating the plane corresponding to the layout shown in (b).*

The evolution of the phases in GST and GeTe was monitored at different time steps during the quench phase, capturing both amorphization and recrystallization, as illustrated in Figure 5-4. The results begin shortly after the start of the quench phase. At this stage, both GeTe and GST contain molten regions where temperatures exceed 1000 K, amorphous regions corresponding to previously molten areas that have already cooled below the melting temperature, and crystalline regions located above the RF contacts. These contacts act as efficient heat sinks, preventing the PCM above them from reaching the melting temperature. The central region of both PCMs is fully molten and amorphized.

The simulations show that the molten regions of both PCMs gradually transform into amorphous phases over time, but the recrystallization mechanisms differ. GeTe initially undergoes recrystallization primarily through the growth of pre-existing crystalline parts located above the RF contacts, with minor nucleation appearing around the midpoint of the downward pulse ramp. In contrast, GST rapidly initiates nucleation, first at the interface between the crystalline region above the RF contacts and then progressively throughout all amorphous areas over time. A before/after quenching comparison presented in Figure 5-5 clearly demonstrates that GeTe and GST follow their expected recrystallization behaviors: GeTe is driven predominantly by the growth of initial crystalline parts with minimal nucleation, whereas GST recrystallizes mainly through nucleation, with almost no growth of pre-existing crystalline regions during quenching.

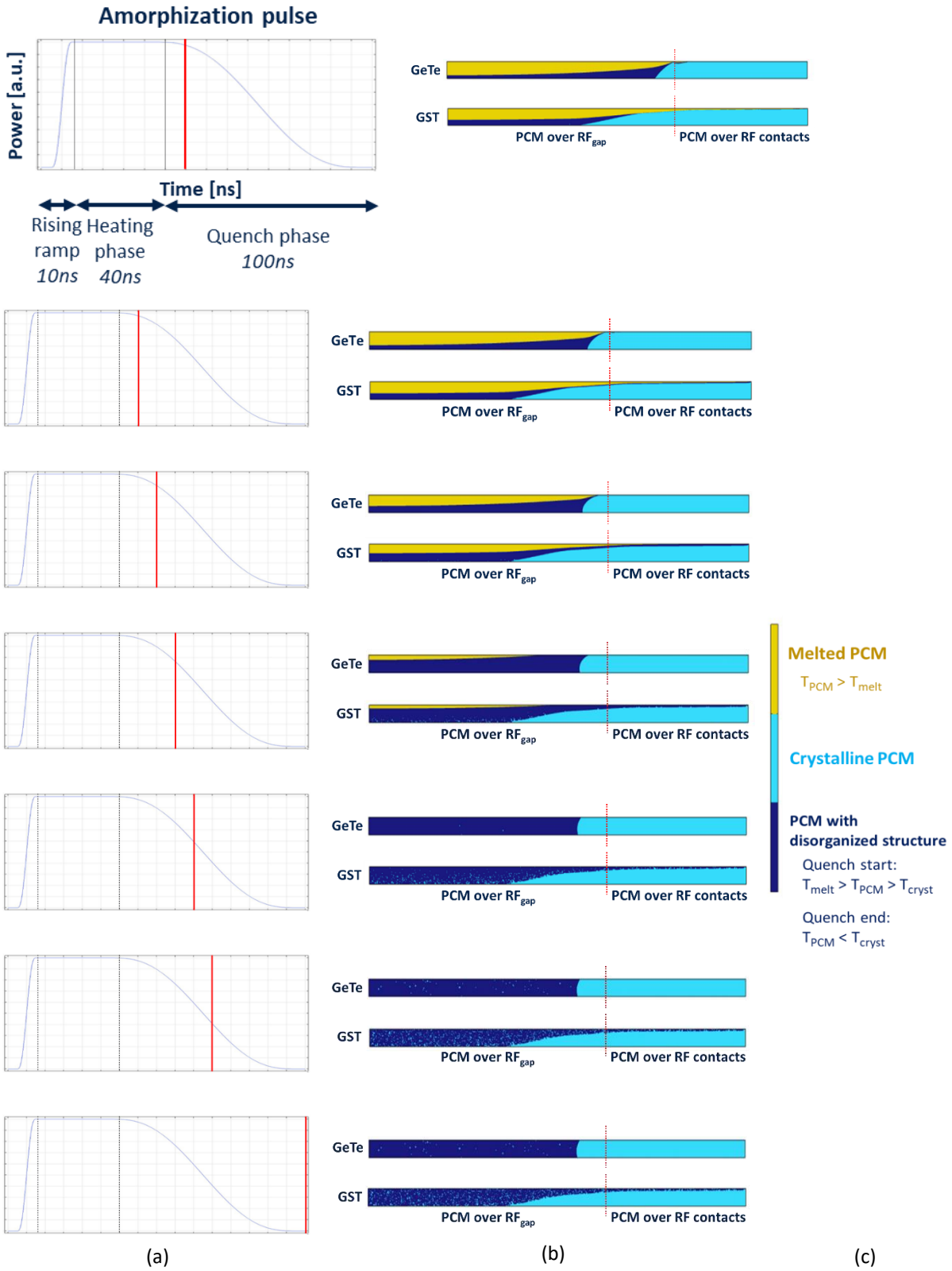


Figure 5-4: *Evolution of the phases of GST and GeTe during an amorphization pulse. The chronograms in (a) represent the heat source power applied over time. Red vertical lines indicate the time points at which the phase states of each material, shown in (b) are observed. The meaning of the colors in the images of (b) is detailed in the legend provided in (c).*

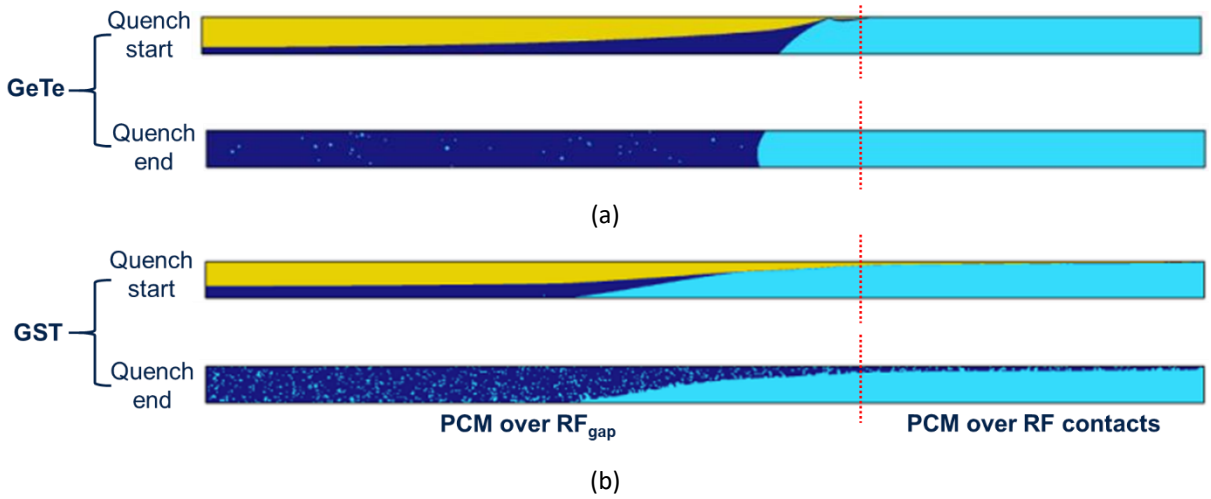


Figure 5-5: *Comparison of the states of the phases of each material between (a) the start of the quench step and (b) the end of the quench step.*

5.3 Conclusion

The implementation and validation of the Phase-Field model in COMSOL successfully demonstrates its ability to reproduce the complete sequence of phase-change phenomena in PCMs, from melting to amorphization and recrystallization. Through the coupling of the finite element simulation with the Phase-Field equations governing nucleation and growth, it was possible to dynamically capture the spatial and temporal evolution of crystalline, amorphous, and molten regions within the PCM during an amorphization pulse. The model accurately reflected the distinct recrystallization mechanisms of GeTe and GST —growth-dominated in GeTe and nucleation-driven in GST— thereby confirming the physical consistency of the approach with experimental and theoretical data reported in the literature. These results validate the robustness and versatility of the Phase-Field implementation in COMSOL for simulating realistic PCM behavior. Notably, GeTe exhibits a more stable amorphous region with fewer crystalline nuclei than GST, highlighting its superior isolation capability and potential for enhanced power-handling performance.

Despite these achievements, certain limitations remain. The high computational cost of the Phase-Field approach restricts simulation times and spatial dimensions. For instance, the downward ramp of the applied pulse was limited to 100 ns, whereas real quenching phases extend longer, allowing more extensive recrystallization. Extending the ramp duration would yield finer insights into nucleation and growth dynamics but would also increase simulation time and result storage by several tens of gigabytes. Future work could involve integrating the Phase-Field model within a full three-dimensional framework to account for the Joule effect and other 3D thermal and electrical phenomena, thereby further improving physical accuracy. However, such an enhancement would demand significantly greater computational resources.

General conclusion

This work focused on optimizing the thermal behavior of PCM-based RF switches for future generations of telecommunication systems. The objectives were to enhance power-handling in both ON and OFF states, minimize ON-state resistance and OFF-state capacitance, reduce energy consumption, and improve overall device reliability to increase endurance over repeated switching cycles. To this end, three simulation models —comprehensive 3D, 3D slab, and 2D— were developed. Experimental actuation was performed on fabricated devices while monitoring their resistance, and RF characterizations were conducted to extract key parameters and measure power-handling performance in both states.

In simulation, an optimal target zone for melting —corresponding to approximately two-thirds of the PCM volume located above the RF_{gap}— was defined for Finite Element Modeling (FEM) analyses. This target provides a sufficient amorphous portion in the OFF state to ensure good isolation while maintaining an adequate distance from the RF contacts, thereby minimizing the thermal energy required to induce melting.

The simulation tools were then employed to investigate several key parameters:

Materials

- **PCM:** The choice of PCM material is critical to ensure efficient phase transition during actuation and high performances during signal transmission. Germanium Telluride (GeTe) was selected for this work due to its high R_{OFF}/R_{ON} ratio (on the order of 10^4), which improves OFF-state isolation. GeTe also offers stable crystalline and amorphous phases, supported by a high crystallization temperature and a substantial RF_{gap} between crystallization and melting temperatures.

- **Heater:** Tungsten (W) was chosen as the heater material for its exceptionally high melting temperature (~3700 K), which greatly enhances reliability. Its excellent thermal conductivity (174 $W \cdot m^{-1} \cdot K^{-1}$) ensures efficient and uniform heat distribution.

- **Dielectric between PCM and heater:** The dielectric, which serves to prevent signal interference between the heater and the PCM, was chosen to be thermally conductive. This choice aims to facilitate efficient heat transfer toward the RF contacts during the PCM quenching phase, as these contacts act as excellent thermal sinks. Aluminum Nitride (AlN) was therefore selected as the dielectric material, as its high thermal conductivity promotes efficient heat evacuation toward the RF contacts —excellent thermal sinks— during the PCM quenching phase. Although this choice slightly increases energy consumption during the heating step, it enables a quench duration from half to three times faster than that obtained with a low-conductivity dielectric such as SiO_2, depending on the layer thickness.

Dimensions

- **PCM thickness:** The thickness of the PCM was set to approximately 100 nm to provide a sufficient volume for both crystalline and amorphous regions while limiting energy requirements and excessive heat retention, which would otherwise lengthen the quench phase and reduce amorphization efficiency.

- **Heater thickness**: The thickness of the heater was also established around 100 nm, balancing mechanical robustness and thermal efficiency —thick enough to ensure structural reliability and adequate heating power, but thin enough to reduce energy consumption.
- **Dielectric between PCM and heater**: The AlN dielectric layer was set to approximately 100 nm, providing a compromise between heating efficiency and quench dynamics. A thicker dielectric increases energy consumption due to a longer heat path, while an overly thin dielectric reduces the thermal conductivity benefits during quenching and enhances parasitic coupling between the heater and PCM.
- **RF_{gap} length and heater width:** The most challenging optimization involved balancing RF_{gap} length and heater width. Longer RF_{gap} allow for larger amorphous regions, improving isolation and OFF-state power-handling, but they also raise ON-state resistance and require wider heaters, which increase parasitic capacitance through the larger tungsten area. Conversely, shorter RF_{gap} reduce parasitic effects and ON-state resistance but require higher actuation power and result in hotter heaters, as the RF contacts lie closer to the PCM's central active region. Two configurations emerged as optimal:
    - A 3 µm-wide heater with a 4 µm-long RF_{gap}, which provides sufficient amorphization for good isolation and OFF-state power-handling with moderate energy consumption.
    - A 1 µm-wide heater with a 1.6 µm-long RF_{gap}, favoring reduced parasitic capacitance and ON-state resistance, thereby improving the $R_{ON} \times C_{OFF}$ FOM.

Building upon this baseline configuration, an optimization loop combining simulation and experimental results enabled the formulation of several design improvements, which are detailed in the following sections:

Addition of thermally conductive layers for temperature homogenization along the heater length

- **AlN top capping:** In devices with short RF_{gap}, the extremities of the heater lie in regions of low thermal conductivity, creating hot spots that compromise reliability. In this work, a heat-spreading AlN layer was added between the SiO_2 and Si_3N_4 top capping in the 3D simulation model. This layer actively redistributes heat along the heater's length. While its presence slightly increases energy consumption during the heating phase of the PCM —due to more efficient heat evacuation— it reduces the temperature at hot spots by up to one-third, significantly enhancing reliability. The improved temperature uniformity also accelerates quenching, as the AlN acts as a supplementary heat sink during the cooling step.
- **Al top blocs:** As part of this work, another solution was explored: the addition of 1 µm-thick aluminum blocks atop the switch, positioned above the heater extremities without covering the primary hot spots. In the 3D simulations, this approach reproduces similar benefits to the AlN capping, reducing hot-spot temperatures by approximately 15 %, and shortening quench duration by around 20 %.

Exploitation of heat sinks for heat evacuation acceleration

- **Reduction of PCM-substrate distance:** Throughout these studies, it was observed that devices with long RF_{gap} still exhibited extended quench durations despite the AlN capping addition. To accelerate cooling, the thermally conductive silicon substrate was brought closer to the PCM

by reducing the thickness of the RF contacts and the dielectric beneath them in the 3D slab model. In simulations, a 90 % reduction in dielectric thickness combined with a 50 % reduction of the RF contacts thickness results in a 40 % faster quench, although with a 22 % increase in energy consumption.

- **Combination of AlN top caping and reduced PCM-substrate distance:** As part of this work, series-structure devices were fabricated combining the AlN layer with 80 % reduction of the dielectric thickness beneath the RF contacts. Across varying heater widths and RF_{gap} lengths, the OFF-state power handling improves by an average of 6 dBm due to faster quenching, enabling more PCM above the RF_{gap} to transition to the amorphous state. Devices with a 3 µm-wide heater and a 4 µm-long RF_{gap} reach 31.5 dBm in both ON- and OFF-states —state-of-the-art results for series structures. RF performance remained high, with insertion loss below 0.4 dB and isolation above 16 dB. R_{ON} decreased to 4.5 Ω, while C_{OFF} increased to 25 fF, resulting in a FOM of 112 fs instead of the targeted 61 fs.

Splitting of the heater rectilign part for temperature homogenization along width

- **Temperature homogenization:** To reduce parasitic capacitances, a new heater design was proposed in this work: the rectilinear part of the heater was split into multiple branches. In 3D simulations, two- and three-branches heaters reduce peak temperature along the heater width by 5.5 % and 7.5 %, respectively. This also homogenizes the temperature along the PCM length, with peak temperatures dropping from 14 % above the target melting temperature for single-branch heaters to 6.5 % and 4 % for double- and triple-branches designs. Implementing a double-branch heater in fabricated devices with 3 µm-wide heaters and 4 µm-long RF_{gap} reduces energy consumption by 16 %, thanks to lower and more uniformly distributed PCM temperatures.

- **Design rules:** In this work, simulations of temperature uniformity, energy consumption, and melted PCM area were used to establish design rules for double-branch heaters, defining bar widths and spacing to minimize energy use while maximizing thermal uniformity and amorphization efficiency.

- **Improvement of resistance, capacitance and power-handling:** The double-branch architecture was implemented in fabricated devices to evaluate its impact on various performance aspects of the switch. The OFF-state resistance increases by 40 % for devices with 3 µm-wide heaters and 4 µm-long RF_{gap}, reflecting a larger amorphous PCM fraction enabled by a more energy-efficient actuation. This improved efficiency results from the reduction of unnecessary temperature excesses, which in turn accelerates the quenching process. While the ON-state resistance and power-handling remain unaffected by the heater design — depending solely on the amount of crystalline PCM, which corresponds to the entire PCM volume in the ON-state regardless of the heater configuration —, OFF-state performance improved, especially in devices with wide heaters and PCM where bigger amounts of PCM transitioned to the amorphous state. For devices with 3 µm-wide heaters, 4 µm-long RF_{gap}, and 80 µm-wide PCM, C_{OFF} dropped by 20 %, and PH_{OFF} reached the measurement limit of 37 dBm.

Implementation of phase-change mechanic in FEM simulations for accuracy improvement

A final improvement introduced in this work enhances the realism of FEM simulations, thereby increasing their overall accuracy. The phase-change mechanism, initially absent from the simulation

software used in this work, was incorporated into the 2D model through the implementation of the Phase-Field Method. By coupling the equations governing crystal nucleation and growth with an electrothermal model, the two stages of an amorphization pulse are successfully reproduced. GeTe and GST are successively employed in the model for comparison. Based on their respective thermal properties, the simulations accurately capture their distinct crystallization behaviors —growth-dominated for GeTe and nucleation-driven for GST. Furthermore, the results reveal that GeTe forms amorphous regions with fewer nuclei, indicating a more stable phase than GST and suggesting potentially improved OFF-state power-handling.

Overall, the results arising from this PhD bring the PCM based RF switch technology one step closer to matching the performances required for going beyond the most popular existing RF switches technologies capabilities. In the future, this type of switch is expected to be useful for high frequencies applications, like mm-wave for advanced 5G and 6G telecommunications, with isolation performance over 30 dB and insertion loss under <0.5 dB.

Perspectives

Addition of physics in simulations

As discussed in Section 2.3, certain physical effects remain absent from the simulation model, limiting its accuracy and preventing full alignment with the behavior of fabricated devices. Incorporating the thermal boundary resistance (TBR) into simulations would improve this accuracy. However, preliminary work on this approach indicates a substantial increase in computational resource consumption, primarily due to the laborious integration process. Future research should focus on developing more efficient methods to incorporate TBR, thereby bringing simulated results closer to the actual performance of fabricated devices.

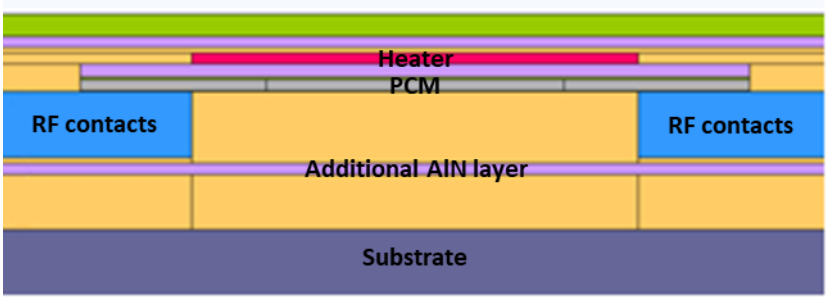
Another possible improvement is the implementation of a cycling system. By applying successive crystallization and amorphization pulses —either within a single unified model or by alternating between separate crystallization and amorphization simulations that each start from the other's final state— the model could reproduce the accumulation of heat during cycling. This effect, which significantly influences experimental measurements, would increase the realism and accuracy of the simulations, yielding results that better reflect actual device behavior.

Improvement of the material used as PCM

Section 2.3 also highlights several issues related to the phase-change material (PCM) itself. These include material degradation during microfabrication, as well as elemental segregation and void formation following repeated actuation cycles. Although mitigation strategies such as PCM encapsulation —to limit outgassing induced by the underlying SiO_2 layer— are already in use, further optimization of microfabrication processes and the development of additional protection strategies could enhance PCM integrity. Improving material quality in this way would directly benefit both thermal and electrical performance. In addition, studying the stoichiometry of the PCM could yield materials with higher conductivity, thereby reducing ON-state resistance and insertion losses in the transmitted signal.

Reproduction of substrate behavior through addition of AlN layer

Section 4.2 proposed exploiting the substrate's high thermal conductivity to accelerate heat evacuation during the quench phase by placing it closer to the PCM. However, this approach makes switch performance highly dependent on the substrate, restricting the ability to maintain these improvements once integrated into the back end of line (BEOL) of a CMOS process. A promising alternative would be to introduce an aluminum nitride (AlN) layer beneath the RF contacts to drain heat thus diminishing the reliance of the device operation over the proximity of the substrate. As illustrated in the schematic below, this additional AlN layer extends across the full width of the switch.



While this configuration may not reduce the quench duration as effectively as moving the substrate closer to the PCM, it could provide a significant advantage for device integration within the BEOL environment.

Device fabrication with Al top blocs

Section 4.4 introduced a new thermal homogenization design based on the addition of aluminum (Al) blocks positioned above the heater's extremities on the top side of the switch. Simulations indicate improved temperature uniformity, leading to enhanced amorphization efficiency and a shorter quench duration. These results, however, require confirmation through electrical characterization of fabricated devices incorporating these Al blocks.

Integration of Phase-Field model in 3D electrothermal models

Section 5.2 presented the coupling of a Phase-Field model with a 2D electrothermal simulation, enabling the reproduction of both amorphization and crystallization behaviors in PCMs. Nonetheless, significant limitations were identified, including prolonged computation times caused by the required mesh refinement. Future developments should aim to integrate the Phase-Field model into 3D electrothermal simulations, combining its precision with a full representation of the underlying physics —such as Joule heating induced by voltage pulses— while maintaining reasonable computational cost and resource consumption.

RF simulation model

In the current finite element method (FEM) simulations, the computation of RF performance remains limited. Consequently, this work primarily compares simulation and measurement results through thermal behavior metrics, such as energy consumption. To gain additional insight into RF performance during early design stages —prior to fabrication— supplementary RF simulations should complement this study. Such models could be developed using dedicated RF design software, for example Advanced Design System (ADS) from Keysight Technologies.

List of Conferences, publications and patent

Patents

Corentin Mercier, Stéphane Monfray, Alain Fleury, Bruno Reig, Jean-François Robillard, Emmanuel Dubois, 'PCM based RF-switches performances improvements with double heater design' (Patent application)

Articles

Corentin Mercier, Bruno Reig, Stéphane Monfray, Emmanuel Dubois, Alain Fleury, Ismaël Charlet, Jose Lugo-Alvarez, Clémence Hellion, Marjolaine Allain and Jean-François Robillard, 'Multiple Branches Heater Design for Improved Power Handling and OFF-state Capacitance in Phase Change Material-Based RF Switches', *IEEE Transactions on Electron Devices (TED)* (under review)

Oral contributions at conferences with proceedings:

EUMW, 22-27 September 2024, Paris

Corentin Mercier, Bruno Reig, S. Monfray, E. Dubois, A. Fleury, F. Gianesello, V. Puyal, I. Charlet, J. Lugo-Alvarez, C. Hellion, M. Allain, J. Denizart, J-F. Robillard, 'Optimization of the melt and quench behavior of phase-change RF switch to improve power handling', *2024 19th European Microwave Integrated Circuits Conference (EuMIC)*, 23-24 September 2024, doi: 10.23919/EuMIC61603.2024.10732309

JNM, 4-7 June 2024, Juan-Les-Pins

Corentin Mercier, Bruno Reig, Stéphane Monfray, Emmanuel Dubois, Alain Fleury, Frédéric Gianesello, Vincent Puyal, Ismaël Charlet, Jose Lugo-Alvarez, J.F. Robillard, 'Optimisation de la trempe et amélioration de la fiabilité de commutateurs à matériaux à changement de phase', *JNM2024 - 23ème Journées Nationales Microondes*, 4-7 June 2024, ⟨hal-04618653⟩

Oral contributions at conferences without proceedings

Multi-functionnal materials conference, 27-29 June 2023, Valenciennes
C. Mercier, A. Patil, J. Canosa, C. Jerez-Garcia, M. Brouillard, S. Monfray, A. Fleury, B. Reig, E. Dubois, P.-Y. Cresson, J-F. Robillard, 'GeTe thermal characterization with 3-omega and Raman thermometry methods'

Poster contributions at conferences

SISPAD, 24-26 September 2025, Grenoble

Corentin Mercier, J.F. Robillard, Emmanuel Dubois, Olga Cueto, Bruno Reig, Stéphane Monfray, Alain Fleury, 'Phase-field simulations for RF switches: highlighting the benefits of GeTe over GST', *SISPAD - International Conference on Simulation of Semiconductor Processes and Devices*, 24-26 September 2025, ⟨hal-05291420⟩

GDR Chalco 20-21 June 2022, Dijon

C. Mercier, G. Tardy, D. Gheysens, S. Monfray, A. Fleury, B. Reig, E. Dubois, J.-F. Robillard, 'Thermal design of PCM-RF Switches for 5G and beyond'

References:

[1] The evolution of Telecommunications: Connecting the World, Abel Nyambe Mushiba, February 2024, https://www.researchgate.net/publication/378498637_Title_The_Evolution_of_Telecommunications_Connecting_the_World

[2] Ivan Glesk, 'From Morse Code to Terabit Communications', *2010 Second Region 8 IEEE Conference on the History of Communications*, 03-05 November 2010, doi: 10.1109/HISTELCON.2010.5735303

[3] Gabriele Falciasecca; Barbara Valotti, 'Guglielmo Marconi: The pioneer of wireless communications', *2009 European Microwave Conference (EuMC)*, 29 September 2009 - 01 October 2009, doi: 10.23919/EUMC.2009.5296358

[4] Tingye Li, 'Advances in Optical Fiber Communications: An Historical Perspective', *IEEE Journal on Selected Areas in Communications*, Volume 1, Issue 3, Pages 356-372, April 1983, doi: 10.1109/JSAC.1983.1145944

[5] Varad Pawar; Anusha Chanda; Prapti Nag; Shreya Roy; Ankan Chatterjee; Sovan Bhattacharya, Dola Dinha, Chandan Bandyopaghyay, 'Evolution of 6G -- an In-depth Study on History of Spectrum Allocation', *2023 International Conference on Integrated Intelligence and Communication Systems (ICIICS)*, 24-25 November 2023, doi: 10.1109/ICIICS59993.2023.10421327

[6] Xichun Li; Abudulla Gani; Rosli Salleh; Omar Zakaria, 'The Future of Mobile Wireless Communication Networks', *2009 International Conference on Communication Software and Networks*, 27-28 February 2009, doi: 10.1109/ICCSN.2009.105

[7] G.D. Ott, 'Vehicle location in cellular mobile radio systems', *IEEE Transactions on Vehicular Technology*, Volume 26, Issue 1, February 1977, doi: 10.1109/T-VT.1977.23655

[8] Ewa Korzeniewska, Andrzej Krawczyk, '5G Technology as the Succesive Stage in the History of Wireless Telecommunication', *2019 IEEE International Conference on Modern Electrical and Energy Systems (MEES)*, 23-25 September 2019, doi: 10.1109/MEES.2019.8896516

[9] Purva Rajkotia, 'How 6G Can Transform The World and Technology', *IEEE standards associations*, 10 August 2022, https://standards.ieee.org/beyond-standards/how-6g-can-transform-the-world-and-technology/

[10] R. Magoon; A. Molnar; J. Zachan; G. Hatcher; W. Rhee, 'A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-n synthesizer', *IEEE Journal of Solid-State Circuits*, Volume 37, Issue 12, Pages 1710-1720, December 2002, doi: 10.1109/JSSC.2002.804356

[11] K. Yamamoto, T. Asada, S. Suzuki, T. Miura, A. Inoue, S. Miyakuni, J. Otsuji, R. Hattori, Y. Miyazaki, and T. Shimura, 'A GSM/EDGE dual-mode, 900/1800/1900-MHz triple-band HBT MMIC power amplifier module', *2002 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 03-04 June 2002, doi: 10.1109/RFIC.2002.1012041

[12] Kazuaki Yamauchi; Wenxi Chen; Daming Wei, 'An Intensive Survey of 3G Mobile Phone Technologies and Applications in Japan', *The Sixth IEEE International Conference on Computer and Information Technology (CIT'06)*, 20-22 September 2006, doi: 10.1109/CIT.2006.49

[13] Qian Shouyi; Mei Chengcai, '3G applications in colleges', *The 2010 International Conference on Apperceiving Computing and Intelligence Analysis Proceeding*, 17-19 December 2010, doi: 10.1109/ICACIA.2010.5709889

[14] Afzal Lodhi, Nishita Hathi, Yiannis Gkekas, Petrit Nahi, 'Coverage comparison of UMTS networks in 900 and 2100 MHz frequency bands', *2008 IET International Conference on Wireless, Mobile and Multimedia Networks*, 11-12 January 2008, doi: 10.1049/cp:20080136

[15] Yulianto La Elo; Fitri Yuli Zulkifli; Eko Tjipto Rahardjo , 'Design of wideband microstrip antenna with parasitic element for 4G/LTE application', *2017 15th International Conference on Quality in Research (QiR) : International Symposium on Electrical and Computer Engineering*, 24-27 July 2017, doi: 10.1109/QIR.2017.8168463

[16] Liljana M. Gavrilovska, Vladimir M. Atanasovski, 'Interoperability in Future Wireless CommunicationsSystems: A Roadmap to 4G', *Microwave Review*, June 2007, doi: https://www.researchgate.net/publication/228612436

[17] 'Ericsson Mobility Report November 2018', https://www.ericsson.com/4ac644/assets/local/reports-papers/mobility-report/documents/2018/ericsson-mobility-report-november-2018.pdf

[18] 'Ericsson Mobility Report November 2024', https://www.ericsson.com/4adb7e/assets/local/reports-papers/mobility-report/documents/2024/ericsson-mobility-report-november-2024.pdf

[19] George Tsoulos, Georgia Athanasiadou, Dimitra Zarbouti, George Nikitopoulos, Vassilis Tsoulos, Nikos Christopoulos, 'Empirical analysis of 5G deployments: A comparative assessment of network performance with 4G', *AEU - International Journal of Electronics and Communications*, Volume 186, November 2024, doi: 10.1016/j.aeue.2024.155479

[20] Nisha Panwar, Shantanu Sharma, Awadhesh Kumar Singh, 'A survey on 5G: The next generation of mobile communication', *Physical Communication*, Volume 18, Part 2, Pages 64-84, March 2016, doi: 10.1016/j.phycom.2015.10.006

[21] Shunliang Zhang, 'An Overview of Network Slicing for 5G', *IEEE Wireless Communications*, Volume 26, Issue 3, Pages 111-117, 11 April 2019, doi: 10.1109/MWC.2019.1800234

[22] Muhammad Zada, Izaz Ali Shah, Hyoungsuk Yoo, 'Integration of Sub-6-GHz and mm-Wave Bands With a Large Frequency Ratio for Future 5G MIMO Applications', *IEEE Access*, Volume 9, Pages 11241-11251, 12 January 2021, doi: 10.1109/ACCESS.2021.3051066

[23] Naser Al-Falahy, Omar Y.K. Alani, 'Millimetre wave frequency band as a candidate spectrum for 5G network architecture: A survey', *Physical Communication 32 (2019)*, Pages 120-144, November 2018, doi: https://doi.org/10.1016/j.phycom.2018.11.003

[24] Shahana Shamoon, Wu Yang Zhou, Farrukh Shahzad, Waqas Ali, Hafiz Subbyal, 'Integrated sub-6 GHz and millimeter wave band antenna array modules for 5G smartphone applications', *Int. J. Electron. Commun. (AEÜ) 161 (2023)*, 21 January 2023, doi: 10.1016/j.aeue.2023.154542

[25] ITU-R 'IMT Vision – Framework and overall objectives of the future development of IMT for 2020 and beyond', September 2015, https://www.itu.int/dms_pubrec/itu-r/rec/m/r-rec-m.2083-0-201509-i!!pdf-e.pdf

[26] Mansoor Shafi; Peter J. Smith; Peiying Zhu; Thomas Haustein; Andreas F. Molisch, 'Guest Editorial Deployment Issues and Performance Challenges for 5G, Part I', *IEEE Journal on Selected Areas in Communications*, Volume 35, Issue 6, Pages 1197-1200, 02 June 2017, doi: 10.1109/JSAC.2017.2690498

[27] Henry Mathews Kusuma; Vinod Kumar Shukla; Shaurya Gupta, 'Enabling VR/AR and Tactile through 5G Network', *2021 International Conference on Communication information and Computing Technology (ICCICT)*, 25-27 June 2021, doi: 10.1109/ICCICT50803.2021.9510181

[28] Laxmi Shrama; Abhishek Javali; Sudhir K. Routray, 'An Overview of High Speed Streaming in 5G', *2020 International Conference on Inventive Computation Technologies (ICICT)*, 26-28 February 2020, doi: 10.1109/ICICT48043.2020.9112489

[29] Saqib Hakak, Thippa Reddy Gadekallu, Praveen Kumar Reddy Maddikunta, Swarna Priya Ramu, Parimala M, Chamitha De Alwis, Madhusanka Liyanage 'Autonomous vehicles in 5G and beyond: A survey', *Vehicular Communications 39*, 5 December 2022, doi: 10.1016/j.vehcom.2022.100551

[30] Carlos Baena, Sergio Fortes, O. S. Peñaherrera-Pulla, Eduardo Baena, and Raquel Barco 'Gaming in the Cloud: 5G as the Pillar for Future Gaming Approaches', *IEEE Communications Magazine*, Volume 62, Issue 11, Pages 76-82, 13 May 2024, doi: 10.1109/MCOM.005.2300256

[31] S. Akhila; Hemavath, '5G Ultra-Reliable Low-Latency Communication: Use Cases, Concepts and Challenges', *2023 10th International Conference on Computing for Sustainable Global Development (INDIACom)*, 15-17 March 2023, https://ieeexplore.ieee.org/document/10112312

[32] Kinza Shafique; Bilal A. Khawaja; Farah Sabir; Sameer Qazi; Muhammad Mustaqim, 'Internet of Things (IoT) for Next-Generation Smart Systems: A Review of Current Challenges, Future Trends and Prospects for Emerging 5G-IoT Scenarios', *IEEE Access*, Volume 8, Pages 23022-23040, 28 January 2020, doi: 10.1109/ACCESS.2020.2970118

[33] Rucha Jichkar; Swati Paraskar; Rina Parteki; Manthan Ghosh; Trushna Deotale; Arfiya S Pathan, Shyam Bawankar, Laxman P.Thakare, '5g: An Emerging Technology And Its Advancement', *2023 11th International Conference on Emerging Trends in Engineering & Technology - Signal and Information Processing (ICETET - SIP)*, 28-29 April 2023, doi: 10.1109/ICETET-SIP58143.2023.10151530

[34] Omid Akbarzadeh; Hani Attar, 'Investigating The Effect of Latency in A 5G Infrastructure for Applications Requiring Ultra-Low Latency', *2022 International Engineering Conference on*

Electrical, Energy, and Artificial Intelligence (EICEEAI), 29 November 2022 - 01 December 2022, doi: 10.1109/EICEEAI56378.2022.10050470

[35] Pingping Lin; Jinyang Yu; Yuetian Zhou, 'Research on Spectrum Sharing Technology', *2023 IEEE International Symposium on Broadband Multimedia Systems and Broadcasting (BMSB)*, 14-16 June 2023, doi: 10.1109/BMSB58369.2023.10211171

[36] Mamta Agiwal, Hyeyeon Kwon, Seungkeun Park, Hu Jin, 'A Survey on 4G-5G Dual Connectivity: Road to 5G Implementation', *IEEE Access*, Volume 9, Pages 16193-16210, 18 January 2021, doi: 10.1109/ACCESS.2021.3052462

[37] Nora Meyne; Johannes Dommel; Thomas Kleine-Ostmann; Martin Kasparick, 'Comparison of Propagation Characteristics Between 5G Bands in a Reflective Industrial Environment', *2024 18th European Conference on Antennas and Propagation (EuCAP)*, 17-22 March 2024, doi: 10.23919/EuCAP60739.2024.10501391

[38] Rajiv baby, 'FR3 Frequency Range – New bands for 5G and 6G Networks, May 14, 2024', https://www.rfpage.com/fr3-frequency-range-5g/

[39] Seongjoon Kang; Marco Mezzavilla; Sundeep Rangan; Arjuna Madanayake; Satheesh Bojja Venkatakrishnan; Grégory Hellbourg, Monisha Ghosh, Hamed Rahmani, Aditya Dhananjay, 'Cellular Wireless Networks in the Upper Mid-Band', *IEEE Open Journal of the Communications Society*, Volume 5, Pages 2058-2075, 05 March 2024, doi: 10.1109/OJCOMS.2024.3373368

[40] Takehiro Nakamura, '5G Evolution and 6G', 2020 IEEE Symposium on VLSI Technology, 16-19 June 2020, doi: 10.1109/VLSITechnology18217.2020.9265094

[41] Gustav Wikström; Janne Peisa; Patrik Rugeland; Nicklas Johansson; Stefan Parkvall; Maksym Girnyk, Gunnar Mildh, Icaro Leonardo Da Silva, 'Challenges and Technologies for 6G', *2020 2nd 6G Wireless Summit (6G SUMMIT)*, 17-20 March 2020, doi: 10.1109/6GSUMMIT49458.2020.9083880

[42] Toon Norp; Prachi Sachdeva; Carles Anton; Konstantinos Trichias; Pooja Mohnani, '6G Research & Innovation Activities in Europe: An Overview of EU & Nationally funded Programmes', *2024 Joint European Conference on Networks and Communications & 6G Summit (EuCNC/6G Summit)*, 03-06 June 2024, doi: 10.1109/EuCNC/6GSummit60053.2024.10597076

[43] GlobalFoundries, 'Designing Next-Gen Cellular and Wi-Fi Switches Using RF SOI', *Technology*, May 2016

[44] Kurmendra, Saurabh Agarwal, 'MEMS Switch Realities: Addressing Challenges and Pioneering Solutions', *Micromachines 2024*, Volume 15, Issue 5, doi: 10.3390/mi15050556

[45] Viviana Mulloni, 'Instability and Drift Phenomena in Switching RF-MEMS Microsystems', *Actuators*, Volume 8, Issue 1, February 2019, doi: 10.3390/act8010015

[46] Li-Ya Ma; Norhayati Soin; Mohamad Hazwan Mohd Daut; Sharifah Fatmadiana Wan Muhamad Hatta, 'Comprehensive Study on RF-MEMS Switches Used for 5G Scenario', *IEEE Access*, Volume 7, Pages 107506-107522, 02 August 2019, doi: 10.1109/ACCESS.2019.2932800

[47] everythingRF, 'What is RF SOI', https://www.everythingrf.com/community/what-is-rf-soi

[48] Anysilicon, 'The Ultimate Guide: FDSOI', https://anysilicon.com/fdsoi/

[49] Nicolás Wainstein, Gina Adam, Eilam Yalon, Shahar Kvatinsky, 'Radiofrequency Switches Based on Emerging Resistive Memory Technologies - A Survey', *Proceedings of the IEEE*, Volume 109, Issue 1, Pages 77-95, January 2021, doi: 10.1109/JPROC.2020.3011953

[50] Tejinder Singh, Raafat R. Mansour 'Chalcogenide Phase-Change Material Germanium Telluride for Radio-Frequency Applications', *IEEE Nanotechnology Magazine*, Volume 16, Issue 3, Pages 26-41, June 2022, doi: 10.1109/MNANO.2022.3160772

[51] Nabil El-Hinnawy; Gregory Slovin; Kurt Moen; Chris Masse; David Howard, 'A Tale of Two Phases: An Overview of Phase-Change Material RF Switch Technology: Sub-20-fs RON*COFF RF Switch Technology for the Mm-Wave and 5G/6G Revolutions', *IEEE Microwave Magazine*, Volume 25, Issue 8, Pages 57-76, August 2024, doi: 10.1109/MMM.2024.3403288

[52] A. T. Waterman, 'The Electrical Conductivity of Molybdenite', *Physical Review Journals Archive,* Volume 21, Issue 5, 1 May 1923, doi: 10.1103/PhysRev.21.540

[53] Stanford R. Ovshinsky, 'Reversible Electrical Switching Phenomena in Disordered Structures', *Physical Review Letters*, Volume 21, Issue 20, 11 November 1968, doi**:** 10.1103/PhysRevLett.21.1450

[54] Neale, R. G., Nelson, D. L. and Moore, 'G. E.: Nonvolatile and reprogrammable, the read mostly memory is here', *Electronics*, Pages 56-60, September 30 1970, https://objective-analysis.com/wp-content/uploads/2022/12/Electronics-1970-Neale-Nelson-Moore.pdf

[55] Jeong-Sun Moon, Hwa-Chang Seo, Dustin Le, Helen Fung, Adele Schmitz, Thomas Oh, Samuel Kim, Kyung-Ah Son, and Baohua Yang, ' 10.6 THz Figure-of-Merit Phase-change RF Switches with Embedded Micro-heater', *2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF System*s, 26-28 January 2015, doi: 10.1109/SIRF.2015.7119879

[56] Nabil El-Hinnawy, Pavel Borodulin, Evan B. Jones, Brian P. Wagner, Matthew R. King, John S. Mason, Jr., James Bain, Jeyanandh Paramesh, T.E. Schlesinger, Robert S. Howell, Michael J. Lee, and Robert M. Young, '12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications', *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 19-22 October 2014, doi: 10.1109/CSICS.2014.6978522

[57] Nabil El-Hinnawy, Greg Slovin, Chris Masse, Paul Hurwitz, Jefferson Rose, David Howard 'Switch Stacking for OFF-State Power Handling Improvements in PCM RF Switches', *2021 IEEE MTT-S International Microwave Symposium (IMS)*, 07-25 June 2021, doi: 10.1109/IMS19712.2021.9574954

[58] Sheng Q, Libin Gao, Jiamei Wang, Hongwei Chen and Jihua Zhang, 'A Review on Material Selection Benchmarking in GeTe-Based RF Phase-Change Switches for Each Layer' *Micromachines 2024,* Volume 5, Issue 3, doi: 10.3390/mi15030380

[59] A.A. Burtsev, N.N. Eliseev, V.A. Mikhalevsky, A.V. Kiselev, V.V. Ionin, V.V. Grebenev, D.N. Karimov, A.A. Lotin, 'Physical properties' temperature dynamics of GeTe, Ge2Sb2Te5 and Ge2Sb2Se4Te1 phase change materials', *Materials Science in Semiconductor Processing,* Volume 153, January 2023, doi: 10.1016/j.mssp.2022.106907

[60] Pavel Borodulin; Nabil El-Hinnawy; Carlos R. Padilla; Andy Ezis; Matthew R. King; Daniel R. Johnson, Doyle T. Nichols, Robert M. Young, 'Recent advances in fabrication and characterization of GeTe-based phase-change RF switches and MMICs', *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 04-09 June 2017, doi: 10.1109/MWSYM.2017.8059098

[61] Shubing Li; Zhangchen Hou; Jianli Tang; Zhigao Hu, 'Design and Fabrication of Non-Volatile Direct Heating RF High-Speed Switch Matrix Based on GeTe Phase Change Material', *2023 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 13-15 November 2023, doi: 10.1109/IMWS-AMP57814.2023.10381058

[62] Alexandre Léon; Bruno Reig; Vincent Puyal; Etienne Perret; Philippe Ferrari; Florence Podevin, 'High Performance and Low Energy Consumption in Phase Change Material RF Switches', *2018 48th European Microwave Conference (EuMC)*, 23-27 September 2018, doi: 10.23919/EuMC.2018.8541622

[63] Alexandre Léon; Bruno Reig; Etienne Perret; Florence Podevin; Damien Saint-Patrice; Vincent Puyal, Jose Lugo-Alvarez, Philippe Ferrari, 'RF Power-Handling Performance for Direct Actuation of Germanium Telluride Switches', *IEEE Transactions on Microwave Theory and Techniques*, Volume 68, Issue 1, Pages 60-73, January 2020, doi: 10.1109/TMTT.2019.2946145

[64] Tejinder Singh; Raafat R. Mansour, 'Experimental Investigation of Performance, Reliability, and Cycle Endurance of Nonvolatile DC–67 GHz Phase-Change RF Switches', *IEEE Transactions on Microwave Theory and Techniques*, Volume 69, Issue 11, Pages 4697-4710, November 2021, doi: 10.1109/TMTT.2021.3105413

[65] Farooq Amin; Thomas Beglin; Nicholas Edwards; Nabil El-Hinnawy; Greg Slovin; David Howard, Doyle Nichols, Robert M. Young, 'Wideband SPDT and SP4T RF Switches using Phase-Change Material in a SiGe BiCMOS Process', *2021 IEEE MTT-S International Microwave Symposium (IMS)*, 07-25 June 2021, doi: 10.1109/IMS19712.2021.9574962

[66] I. Charlet, S. Guerber , A. Naoui, B. Charbonnier, C. Dupré , J. Lugo-Alvarez , C. Hellion, M. Allain, F. Podevin, E. Perret, B. Reig, 'Optical Actuation Performance of Phase-Change RF Switches', *IEEE Electron Device Letters*, Volume 45, Issue 3, Pages 500-503, March 2024, doi: 10.1109/LED.2023.3347800

[67] Ayoub Naoui, Ismael Charlet, Sylvain Guerber, Benoit Charbonnier, Cécilia Dupre, Jose Lugo, Clémence Hellion, Marjolaine Allain, Florence Podevin, Etienne Perret, Bruno Reig, 'Actionnement optique de commutateurs RF à base de PCM: comparaison des performances pour différentes tailles de GeTe', *JNM 2024 - 23èmes Journées Nationales Microondes*, June 2024, doi: cea-04754539

[68] Areski Ghalem; Cyril Guines; Damien Passerieux; Jean-Christophe Orlianges; Laure Huitema; Aurelian Crunteanu, 'Reversible, Fast Optical Switching of Phase Change Materials for Active Control of High-Frequency Functions', *2018 IEEE/MTT-S International Microwave Symposium – IMS*, 10-15 June 2018, doi: 10.1109/MWSYM.2018.8439247

[69] Aurelian Crunteanu; Laure Huitema; Jean-Christophe Orlianges; Cyril Guines; Damien Passerieux, 'Optical switching of GeTe phase change materials for high-frequency applications', *2017 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 20-22 September 2017, doi: 10.1109/IMWS-AMP.2017.8247379

[70] H.J. Li, K.P. Chang, C.E. Chen, W.T Hsieh, H.H. Kuo, C.C. Huang, H.C. Chen, Z.H. Ya, H.Y. Chen, J.D. Jin, S. H. Yang, Y.W. Ting, K.C. Tseng, K.C. Huang, Harry Chuang, 'A Novel Phase Change Material RF Switch with 16nm Technology to Achieve Low Voltage and Low Ron*Coff for mmWave', *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits),* 26 August 2024, doi: 10.1109/VLSITechnologyandCir46783.2024.10631337

[71] Yi-Ting Lin, Student Member, Ching-En Chen, Kuo-Pin Chang, Hung-Ju Li, Chang-Chih Huang, Yu-Wen Wang, Wei-Fang Chen, Han-Yu Chen, Chih-Ren Hsieh, Yu-Wei Ting, Kuo-Chin Huang, Harry Chuang and Zuo-Min Tsai, 'Broadband High-Performance SPDT Switch Based on Phase-Change-Material From DC to 200 GHz', *IEEE Microwave and Wireless Technology Letters*, Volume 35, Issue 6, Pages 730-733, June 2025, doi: 10.1109/LMWT.2025.3552771

[72] Tejinder Singh, Raafat R. Mansour, 'Characterization, Optimization, and Fabrication of Phase Change Material Germanium Telluride Based Miniaturized DC–67 GHz RF Switches', *IEEE Transactions on Microwave Theory and Techniques*, Volume 67, Issue 8, Pages 3237-3250, August 2019, doi: 10.1109/TMTT.2019.2926458

[73] D. Loke, T. H. Lee, W. J. Wang, L. P. Shi, R. Zhao, Y. C. Yeo, T. C. Chong, and S. R. Elliott, 'Breaking the Speed Limits of Phase-Change Memory', *Science*, Volume 336, Issue 6088, Pages 1566-1569, 22 Jun 2012, doi: 10.1126/science.1221561

[74] Neeru Bala, Bheem Khan, Kamaljit Singh, Palwinder Singh, Abhinav Pratap Singh and Anup Thakur, 'Recent advances in doped Ge2Sb2Te5 thin film based phase change memories', *Material Advances*, Issue 3, Pages 747-768, 2023, doi: 10.1039/D2MA01047J

[75] Pierre Noé, Christophe Vallée, Françoise Hippert, Frédéric Fillot and Jean-Yves Raty, 'Phase-change materials for non-volatile memory devices: from technological challenges to materials science issues', *Semiconductor Science and Technology*, Volume 33, Number 1, 2018, doi: 10.1088/1361-6641/aa7c25

[76] A. Crunteanu; A. Mennai; C. Guines; D. Passerieux; P. Blondy, 'Out-of-plane and inline RF switches based on Ge2Sb2Te5 phase-change material', *2014 IEEE MTT-S International Microwave Symposium (IMS2014*), 01-06 June 2014, doi: 10.1109/MWSYM.2014.6848417

[77] Amine Mennai; Annie Bessaudou; Françoise Cosset; Cyril Guines; Pierre Blondy; Aurelian Crunteanu, 'Bistable RF switches using Ge2Sb2Te5 phase change material', *2015 European Microwave Conference (EuMC)*, 07-10 September 2015, doi: 10.1109/EuMC.2015.7345920

[78] Changcheng Ma, Jing He, Jingjing Lu, Jie Zhu and Zuoqi Hu, 'Modeling of the Temperature Profiles and Thermoelectric Effects in Phase Change Memory Cells', *Applied Sciences,* Volume 8, Issue 8, July 2018, doi: 10.3390/app8081238

[79] M. Field, C. Hillman, P. Stupar, J. Hacker, Z. Griffith, K.-J. Lee, 'Vanadium dioxide phase change switches', *Proc. SPIE 9479, Open Architecture/Open Business Model Net-Centric Systems and Defense Transformation 2015,* 21 May 2015, doi: 10.1117/12.2179851

[80] M. N. Sadiq, M. Le Roy, A. Perennec, P. Laurent, N. Martin, D. Passerieux, A. Crunteanu, R. Boyer, F. Dumas-Bouchiat, M-B. Martin, L. Divay, Q. Levesque, G. Tanné, 'Design and Characterisation of VO2 Based Switches for Ultra-Fast Reconfigurable Devices', *2019 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 16-18 July 2019, doi: 10.1109/IMWS-AMP.2019.8880086

[81] A. Mennai; A. Bessaudou; F. Cosset; C. Guines; D. Passerieux; P. Blondy, 'High cut-off frequency RF switches integrating a metal-insulator transition material', *2015 IEEE MTT-S International Microwave Symposium*, 17-22 May 2015, doi: 10.1109/MWSYM.2015.7166910

[82] Muzhi Wang, Yonghyun Shim, Mina Rais-Zadeh, 'A Low-Loss Directly Heated Two-Port RF Phase Change Switch', *IEEE Electron Device* Letters, Volume 35, Issue 4, Pages 491-493, April 2014, doi: 10.1109/LED.2014.2303972

[83] A. Leon, 'Commutateurs RF à base de matériaux à changement d'état : conception, caractérisation et application', https://hal.science/tel-04607305v1

[84] Gregory Slovin, Min Xu, Rahul Singh, T. E. Schlesinger, Jeyanandh Paramesh, James A. Bain, 'Design Criteria in Sizing Phase-Change RF Switches', *IEEE transactions on microwave theory and techniques*, Volume 65, Issue 11, November 2017, doi: 10.1109/TMTT.2017.2759735

[85] M.C. Hugon, F. Varniere, B. Agius, M. Froment, C. Arena, J. Bessot, 'Stresses, microstructure and resistivity of thin tungsten films deposited by RF magnetron sputtering', *Applied Surface Science*, Volume 38, Issues 1-4, Pages 269-285, September 1989, doi: 10.1016/0169-4332(89)90548-5

[86] P. D. Desai, T. K. Chu, H. M. James, C. Y. Ho, 'Electrical Resistivity of Selected Elements', *Journal of Physical and Chemical Refererence*, Volume 13, Issue 4, Pages 1069-1096, October 1984, doi: 10.1063/1.555723

[87] Sang Hyun Lee, Su Yong Kwon, Hye Jeong Ham, 'Thermal conductivity of tungsten–copper composites', *Thermochimica Acta*, Volume 542, Pages 2-5, 20 August 2012, doi: 10.1016/j.tca.2012.03.022

[88] EEPOWER, 'Temperature Coefficient of Resistance', https://eepower.com/resistor-guide/resistor-fundamentals/temperature-coefficient-of-resistance/

[89] Engineers edge, 'Specific Heat Capacity of Metals table chart', https://www.engineersedge.com/materials/specific_heat_capacity_of_metals_13259.htm

[90] AZoMaterials, 'Tungsten', https://www.azom.com/properties.aspx?ArticleID=614

[91] Bruno Hay, Olivier Beaumont, Guillaume Failleau, Nolwenn Fleurence, Marc Grelard, Refat Razouk, Guillaume Davée, Jacques Hameury, 'Uncertainty Assessment for Very High Temperature Thermal Diffusivity Measurements on Molybdenum, Tungsten and Isotropic Graphite', *International Journal of Thermophysics*, Volume 23, Number 2, January 2022, doi: 10.1007/s10765-021-02926-6

[92] A. Hariri; A. Crunteanu; C. Guines; C. Hallepee; D. Passerieux; P. Blondy, 'Double-Port Double-Throw (DPDT) Switch Matrix Based on Phase Change Material (PCM)', *2018 48th European Microwave Conference (EuMC)*, 23-27 September 2018, doi: 10.23919/EuMC.2018.8541405

[93] N. Le Gall; I. Bettoumi; C. Hallepee; P. Blondy, 'Off-State Stability of Phase-Change Material RF-Switches', *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, 19-24 June 2022, doi: 10.1109/IMS37962.2022.9865537

[94] IMOA, 'Role of Molybdenum', https://www.imoa.info/molybdenum/molybdenum-properties.php

[95] PLANSEE, 'Molybdenum: Properties & uses', https://www.plansee.com/en/materials/molybdenum.html

[96] AZoMaterials, 'Molybdenum (Mo) - Properties, Applications', https://www.azom.com/properties.aspx?ArticleID=616

[97] Denis Rochais, H Le Houëdec, F. Enguehard, Julien Jumel, François Lepoutre, 'Microscale thermal characterization at temperatures up to 1000°C by photoreflectance microscopy. Application to the characterization of carbon fibres', *Journal of Physics D: Applied Physics*, Volume 38, Number 10, May 2005, doi: 10.1088/0022-3727/38/10/002

[98] Diaohao Zhai; Yongping Chen; Houming Zhai; Yi Liu, 'Fabrication and characterization of NiCr-based films with high resistivity and low temperature coefficient of resistance', *Nanotechnoly and precision engeneering,* Volume 6, Issue 2, 2023, doi: 10.1063/10.0017693

[99] European comission, 'Phase-Change Switch', https://ec.europa.eu/research/participants/documents/downloadPublic?documentIds=080166e5b5addac8&appId=PPGMS

[100] Robert M. Young; Nabil El-Hinnawy; Pavel Borodulin; Brian P. Wagner; Matthew R. King; Evan B. Jones; Robert S. Howell; Michael J. Lee, 'Thermal analysis of an indirectly heat pulsed non-volatile phase change material microwave switch', *Journal of Applied Physics*, Volume 116, Issue 5, 7 August 2014, doi: 10.1063/1.4891239

[101] RESISTALLOY, 'Nickel Chromium Alloy Physical And Mechanical Properties', https://www.resistalloytrading.co.uk/pages/nickelchromiumalloy

[102] AZoMaterials, 'Nickel Chrome Alloys - Properties and Applications', https://www.azom.com/properties.aspx?ArticleID=916

[103] Akash Patil, 'Thermal characterization of GeSbTe alloys by Raman thermometry for Phase-Change Memories' Micro and nanotechnologies/Microelectronics. Université de Lille, 2023. English. ⟨NNT : 2023ULILN037⟩. ⟨tel-04724070⟩

[104] CMC MICROSYSTEMS, 'Short-Open-Load-Thru (SOLT) Calibration ', https://account.cmc.ca/en/WhatWeOffer/Support/Documents/UserGuides/HiSpeedTestGuide/3_Techniques/Techniques_ChapterHolder/3_3_Calibration/3_3_3_1_SOLT.aspx

[105] S. W. Fong, A. Sood, L. Chen, N. Kumari, M. Asheghi, K. E. Goodson, G. A. Gibson, H.-S. P. Wong, 'Thermal conductivity measurement of amorphous dielectric multilayers for phase-change memory power reduction', *J. Appl. Phys. 120*, Issue 1, 7 July 2016, doi: 10.1063/1.4955165

[106] Luca Crespi, Andrea Ghetti, Mattia Boniardi, Andrea L. Lacaita, 'Electrical Conductivity Discontinuity at Melt in Phase Change Memory', *IEEE Electron Device Letters*, Volume 35, Issue 7, Page(s): 747 – 749, July 2014, doi: 10.1109/LED.2014.2320967

[107] Jean-Luc Battaglia, Vincent Schick, Andrzej Kusiak, Clément Rossignol, Claudia Wiemer, Alessio Lamperti, 'Identification of the temperature-dependent thermal boundary resistance at a metal-phase change material', *Inverse Problems in Science and Engineering*, Volume 20, Issue 7, Pages 941-950, 02 Dec 2011, doi: 10.1080/17415977.2011.637205

[108] Eilam Yalon, Sanchit Deshmukh, Miguel Muñoz Rojo, Feifei Lian, Christopher M. Neumann, Feng Xiong, Eric Pop, 'Spatially Resolved Thermometry of Resistive Memory Devices', Scientific Reports, 7, Article number 15360, 10 November 2017, doi: 10.1038/s41598-017-14498-3

[109] Heungdong Kwon, Christopher Perez, Woosung Park, Mehdi Asheghi, Kenneth E. Goodson, 'Thermal Characterization of Metal–Oxide Interfaces Using Time-Domain Thermoreflectance with Nanograting Transducers', *ACS Applied Materials & Interfaces*, Volume 13, Issue 48, 19, November 2021, doi: 10.1021/acsami.1c12422

[110] Koen Heijmans, Amar Deep Pathak, Pablo Solano-López, Domenico Giordano, Silvia Nedea, David Smeulders, 'Thermal Boundary Characteristics of Homo-/Heterogeneous Interfaces', Nanomaterials, 9(5), 663, 26 April 2019, doi: 10.3390/nano9050663

[111] Yiqi Yu, Marek Skowronski, 'Growth dominated crystallization of GeTe mushroom cells during partial SET operation', *J. Appl. Phys,* Volume 133, Issue 41, 24 January 2023, doi : 10.1063/5.0129023

[112] Tae-Youl Yang, Il-Mok Park, Byoung-Joon Kim, Young-Chang Joo, 'Atomic migration in molten and crystalline $Ge_2Sb_2Te_5$ under high electric field', *Appl. Phys. Lett*, Volume 95, Issue 3, 20 July 2009, doi: 10.1063/1.3184584

[113] Yung-Huei Lee, P.J. Liao, Vincent Hou, Dawei Heh, Chih-Hung Nien, Wen-Hsien Kuo, 'Composition Segregation of Ge-Rich GST and Its Effect on Reliability', *2021 IEEE International Reliability Physics Symposium (IRPS)*, 21-25 March 2021, doi: 10.1109/IRPS46558.2021.9405168

[114] Xinyi Fang, Mohammad Ayaz Masud, Gianluca Piazza, James Bain, 'Interface dewetting as a source of void formation and aggregation in phase change nanoscale actuators', *Appl. Phys. Lett.*, Volume 122, Issue 5, 30 January 2023, doi: 10.1063/5.0137456

[115] L. de los Santos Valladares, A. Bustamante Dominguez, J. Llandro, S. Holmes, O. Avalos Quispe, R. Langford, J. Albino Aguiar, C.H.W. Barnes, 'Surface morphology of amorphous germanium thin films following thermal outgassing of SiO2/Si substrates', *Applied Surface Science*, Volume 316, Pages 15-21, 15 October 2014, doi: 10.1016/j.apsusc.2014.07.073

[116] Julian Pries, Christian Stenz, Lisa Schäfer, Alexander Gutsche, Shuai Wei, Pierre Lucas, Matthias Wuttig, 'Resistance Drift Convergence and Inversion in Amorphous Phase Change Materials', *Advanced Functional Materials,* Volume 32, Issue 48, 25 September 2022, doi: 10.1002/adfm.202207194

[117] Robin Miquel, 'Simulation multi-échelle des mémoires PCM : du matériau au dispositif', Modélisation et simulation. Institut Polytechnique de Paris, 2023. Français. ⟨NNT : 2023IPPAX142⟩. ⟨tel-04470594⟩

[118] T. Singh and R. R. Mansour, 'Experimental Investigation of Performance, Reliability, and Cycle Endurance of Nonvolatile DC–67 GHz Phase-Change RF Switches', *IEEE Trans. Microw. Theory Tech.*, Volume 69, Issue 11, Pages 4697-4710, 1 September 2021. 2021, doi: 10.1109/TMTT.2021.3105413

[119] I. Charlet et al., 'RF Performance of Large Germanium Telluride Switches for Power Application', *in 2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, 18-19 September 2023, doi: 10.23919/EuMIC58042.2023.10288974

[120] N. El-Hinnawy *et al.*, 'Experimental Demonstration of AlN Heat Spreaders for the Monolithic Integration of Inline Phase-Change Switches', *IEEE Electron Device Letters*, Volume 39, Issue 4, Pages 610–613, 15 Fecbruary 2018, doi: 10.1109/LED.2018.2806383

[121] O. Cueto, V. Sousa, G. Navarro, and S. Blonkowski, 'Coupling the Phase-Field Method with an electrothermal solver to simulate phase change mechanisms in PCRAM cells', *2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Pages 301–304, September 2015, doi: 10.1109/SISPAD.2015.7292319.

[122] Y. Yu and M. Skowronski, 'Growth dominated crystallization of GeTe mushroom cells during partial SET operation', *Journal of Applied Physics*, vol. 133, no. 4, p. 044501, Jan. 2023, doi: 10.1063/5.0129023