UNIVERSITE DE LILLE 1 **N° d'ordre : 40600**

Ecole Doctorale Sciences Pour l'Ingénieur

THESE

En vue de l'obtention du grade de

DOCTEUR DE L'UNIVERSITE DE LILLE

Discipline : Micro et Nano technologies, Acoustique et Télécommunications

Emetteur à 60 GHz

avec des possibilités radio logicielle

Présentée et soutenue publiquement le 20 Septembre 2011

par Jonathan MULLER

Jury :

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Abstract

“60 GHz wireless transmitter with SDR capabilities”

By Jonathan Muller

“You see, wire telegraph is a kind of a very, very long cat. You pull the tail in New-York and the head is meowing in Los-Angeles. Do you understand this? And radio operates exactly the same way: you send signals here, they receive them there. The only difference is that there is no cat”

Albert Einstein.

Radio is everywhere. I guess everybody agree on this point. You use it everyday with your cellphone, your computer, your music player. As the technology growss-up the market is doing so. New applications show-up and the need of bandwidth become more and more necessary.

Recently the new deep sub-micron CMOS technologies have enabled the implementation of digital circuits for wireless communications, commonly called digital radio or software defined radio. This trend comes from the fact that standard analog/RF solutions are not viable anymore as they suffer from the degraded performances of the sub-micron devices.

Meanwhile recent development in wireless communication has enabled new applications while using more bandwidth. 60 GHz radio came up as the candidates for high-data-rate (10 Gb/sec), short-distance (1 to 10m), wireless telecommunication systems. The unlicensed 60GHz band offers a large bandwidth and enables new applications. Data links at 60GHz will enable data rates comparable to wired standards like gigabit Ethernet and High Definition Multimedia Interface (HDMI). The 60 GHz band is available from 57 GHz to 66 GHz and there are about 5 GHz of bandwidth common to Europe, Asia, Australia and North America.

New architectures are needed to cope with the limitations of these new CMOS processes, while taking advantage of the increasing speed and density of digital techniques. These techniques are used to process low bandwidth for wireless communication standards such Wifi and WiMax.

In this work, a transmitter architecture at 60 GHz with software defined radio capabilities has been studied. It is based on the combination of an interpolator and a DRFC (digital-to-RF converter), structure which combines a DAC and mixer in order to realize a direct conversion of the digital data stream to the RF frequency. The principal problem with a direct digital to RF translation is that spurs outside the signal band are transmitted and thus difficult to filter at the RF frequency. Images are thus up-converted without any filtering except from the zero order response of the DRFC. The combination of an interpolator and the DRFC will permit to realize a direct digital to RF conversion without polluting the adjacent channels.

The 60 GHz wireless standard IEEE 802.15.3c has been taken as a reference to study the proposed transmitter. This work is based on 4 radio channels of 2GHz in the 57 GHz – 65 GHz band. The output of the baseband digital signal processor is sampled at 2.5GS/s. Images at multiples of the initial sampling frequency are attenuated with an interpolator FIR filter working at 10 GS/s. After filtering and conversion to the analog domain, the first image appears with 20 dB attenuation at a 10 GHz offset. Therefore this image falls out of the standards frequency band, regardless of the channel used and can be eliminated by the RF band filters present in the systems. The architecture is therefore compatible with the standard's requirements.

A prototype of the 10GS/s interpolator has been implemented to prove the feasibility of the concept. Different optimizations at a system level and at a circuit level are mandatory to enable the 10 GS/s digital output. Static and dynamic logic are used to demonstrate such high data rates frequency.

The fabricated prototype transmitter IC demonstrates full functionality up to a 9.6 GHz and consumes 408mA (571mW) with a 1.4V supply voltage. The core area is 650 x 170 um^2.

Keywords: interpolator, digital transmitter, 60 GHz, software radio, RF, 65nm CMOS.

This thesis work has been performed in:

1st year: The Integrated Circuits Design Group /Microélectronique Silicium of the ISEN department of the Institut d'Electronique, de Microélectronique et de Nanotechnologies (IEMN), 41, bd Vauban, 59000 Lille, France.

2d year: The Berkeley Wireless Research Center (BWRC) in the group of Professor Ali Niknejad, 2108 Allston Way, Suite 200 Berkeley, CA 94704-1302.

3rd year: In STMicroelectronics, T&RD, 17 Rue des Martyrs, 38000 Grenoble Cedex 9, in the group of Didier Belod with Andreia Cathelin as supervisor.

Funding for this work has been given by STMicroelectronics and ANRT (association national de la recherche et de la technologie).

Résumé

“Emetteur sans fil à 60 GHz avec des possibilités radio logicielle”

Par Jonathan Muller

Les dernières technologies submicroniques ont permis le développement de circuits numériques pour les communications sans fil. Les architectures CMOS analogiques standards ont des difficultés à suivre la diminution de la tension d'alimentation et la diminution des performances des dispositifs, ce qui rend le développement d'émetteurs-récepteurs de plus en plus difficile. De plus l'utilisation de ces architectures CMOS standards analogique ne permet pas une approche multistandards (plusieurs chaines RF sont mises en place dans un téléphone).

En parallèle la demande de bande passante ne fait qu’augmenter. Le « 60 GHz », a émergé comme l'un des candidats les plus prometteurs pour le transfert sans fil haut-débit de données (10 Gb/sec) à courte distance (1 à 10m). L’utilisation de cette bande va donc permettre la création de nouvelles applications plus passionnantes les unes que les autres. De plus la bande est ouverte partout dans le monde, ce qui signifie qu’un plan de fréquence mondial peut être mis en place.

Ce travail de thèse propose de concilier le design radio avec une technologie CMOS submicronique pour un standard large bande contraignant comme celui proposé dans les systèmes 60 GHz.

Dans ce travail, une architecture d'émetteur numérique a été étudiée. Elle est basée sur la combinaison d'un interpolateur et d’un DRFC (convertisseur numérique-à-RF), structure qui combine un mélangeur et convertisseur numérique-analogique, afin de réaliser une conversion directe du flux de données numériques à la fréquence RF.

Le standard 60 GHz sans fil IEEE 802.15.3c a été pris comme référence pour étudier l'émetteur proposé. La modulation mise en œuvre est l’OFDM basée sur des sous-porteuses QPSK. Le spectre du flux de données numériques à la sortie du modulateur OFDM (échantillonné à 2,5 Géch/s) contient des répliques du signal provenant de l’échantillonnage. Ces images doivent être filtrées avant translation à la fréquence radio. L’interpolateur dans l'architecture de l’émetteur proposé réalise cette fonction de filtrage

et le DRFC la fonction de conversion numérique-analogique et translation directe à la fréquence radio. Le paragraphe suivant explique le concept plus en détail.

Comme expliqué précédemment, la sortie du modulateur OFDM est échantillonnée à 2.5 Géch/s. Les images aux multiples de la fréquence d'échantillonnage initial sont atténuées avec un interpolateur FIR fonctionnant à 10 Géch/s. Après filtrage et conversion dans le domaine analogique, la première image apparaît avec 20 dB d'atténuation à 10 GHz d'offset. Par conséquent, cette image se situe hors de la bande de fréquences définie dans le standard quel que soit le canal utilisé et peut être éliminée par les filtres de bande RF présents dans les systèmes. L'architecture est donc compatible avec les exigences de la norme.

Un prototype de l'interpolateur à 10 Géch/s a été mis en œuvre pour prouver la faisabilité du concept. Différentes optimisations au niveau du système et à un niveau du circuit sont obligatoires pour permettre le fonctionnement du circuit à 10 Géch/s. Des notions de logique statique et dynamique sont utilisées pour la construction du circuit à cette cadence.

Le prototype fabriqué est fonctionnel jusqu'à 9,6 GHz et consomme 408mA (571mW) avec une tension d'alimentation de 1.4V. La taille du cœur est de 650 x 170 um2.

Mots-clés: interpolateur, émetteur numérique, 60 GHz, radio logicielle, radio fréquence, 65nm CMOS.

Ce travail de thèse a été réalisé:

1ère année : Dans le département de conception de circuit à l'ISEN (dépendance de l'Institut d'Electronique, de Microélectronique et Nanotechnologies (IEMN)), 41, bd Vauban, 59000 Lille, France.

2ème année : Au Berkeley Wireless Research Center (BWRC) dans le groupe du Professeur Ali Niknejad, 2108 Allston Way, Suite 200 Berkeley, CA 94704-1302.

3ème année : Chez STMicroelectronics, T&RD, 17 Rue des Martyrs, 38000 Grenoble Cedex 9, dans le groupe de Didier Belod avec Andreia Cathelin en tant que responsable industriel.

Ce travail a été financé par STMicroelectronics et l'ANRT (association national de la recherche et de la technologie).

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Acronyms

ADC .....Analog to Digital Converter

BB.....Baseband
BER.....Bit Error Rate
BiCMOS.....Bipolar-CMOS
BPF .....Band Pass Filter
BPSK.....Binary Phase Shift Keying

CDMA.....Code Division Multiple Access
CMOS.....Complementary Metal Oxide Semiconductor
CMP .....Circuit Multi Project
CPL .....Complementary Pass Logic
CSD.....Canonical Signed Digit

DAC .....Digital to Analog Converter
DCS.....Digital Cellular Service
DRFC .....Digital-to-RF Converter
DSP.....Digital Signal Processor
DUT .....Device Under Test

ECMA .....European Computer Manufacturers Association
EDGE .....Enhanced Data rates for Global Evolution
ENOB.....Effective Number of Bits
ESD.....Electrostatic Discharge
EVM .....Error Vector Magnitude

FA.....Full Adder
FCC.....Federal Communications Commission
FIR.....Finite Impulse Response
FSK .....Frequency Shift Keying

GA .....Genetic Algorithm
GaAs.....Gallium Arsenic
GS/s .....Giga Samples per second
GSM .....Global System for mobile Communications

HD .....Hight Definition
HDMI.....High Definition Multimedia Interface
HRP .....hight Rate Protocol

I/Q.....In-phase/Quadrature
IC.....Integrated Circuits
IDFT.....Inverse Discrete Fourier Transform

IEEE .....Institute of Electrical and Electronics Engineers
IF .....Intermediate Frequency
IFFT .....Inverse Fast Fourier Transform
IIR.....Infinite Impulse Response
InP.....Indium Phosphide
IRFC.....Intermediate to Radio Frequency Converter

LC .....inductor and capacitor
LO.....Local Oscillator
LOS.....Light Off Site
LPF .....Low Pass Filter
LSB .....Least Significant Bit
LTE .....Long Term Evolution
LTI .....Linear Time Invariant

MAC.....Multiplexed Analogue Components
mmW.....milimeter Wave
MSB .....Most Significant Bit
MSK.....Minimum Shift Keying
NMOS .....Negative Metal Oxide Semi-conductor

NRZ .....Non Return to Zero

OFDM.....Orthogonal Frequency Division Multiplexing
OSR .....Oversampling Ratio

PA.....Power Amplifier
PAE.....Power Added Efficiency
PAPR .....Power to Average Peak Ratio
PCB.....Printed Circuit Board
PDN.....Pull Down Network
PHY .....Physical Layer
PLL.....Phase Lock Loop
PLS .....Post Layout Simulation
PMOS.....Positive Channel Metal Oxide Semiconductor
PUN.....Pull Up Network

QAM .....Quadrature Amplitude Modulation
QPSK.....Quadrature Phase Shift Keying

RC.....Resistance/Capacitance
RF.....Radio Frequency
RMS .....Route Min Square
RTL.....Resistor–Transistor Logic

SC.....Single Carrier
SDR .....Software Defined Radio

SFDR.....Spurious-Free Dynamic Range
Si .....Silicium
SiGe.....Silicium Germanium
SNR .....Signal to Noise Radio
SoC.....System on Chip

TD-SCDMA Time Division Synchronous Code Division Multiple Access
TG3C .....Task Group 3C (WPAN Millimeter Wave Alternative PHY)
TSPCFF .....True Single Phase Clock Flip-Flop

UMTS .....Universal Mobile Telecommunications System
UWB.....Ultra Wide Band

VCO.....Voltage Control Oscillator
VGA.....Video Graphics Array
VHDL.....Hardware Description Language
VHSIC.....Very-High-Speed Integrated Circuits

WCDMA....Wideband Code Division Multiple Access
WiMAX .....Worldwide Interoperability for Microwave Access
WLAN.....Wireless Local Area Network
WPAN .....Wireless Personal Area Network

Table of figures

1. CHAPTER BACKGROUND

The goal of this work is to implement a wireless 60 GHz transmitter with Software Defined Radio capabilities. This first chapter gives all the necessary background to understand the thematic of this work. First, a short introduction about the emergence of 60 GHz is explained. Then, as this work focuses on the transmitter part, a state-of-the art in transmitter architecture for different RF applications is presented, starting from an all analog transmitter and then going to an all digital transmitter where the concepts of SDR radio are presented.

In order to work with real specifications, the IEEE TG3C.15.3C standard has been selected. Some requirements for this standard can be found in annexe (60 GHZ IEEE TG3C.15.3C STANDARD) to clarify the architectural choices and to evaluate the performance of the transmitter.

1.1. INTRODUCTION

In the last years, the industry focused on the 1 – 10 GHz spectrum for different broadband applications such voice, data and multimedia. The interest in wireless communications becomes higher and higher everyday and new perspectives show-up because of this interest. In consequence, new solutions must be provided specifically in terms of data rate. Multimedia applications are hungry (multi gigabit per second) and following Shannon theory one way to increase the data rate is to increase the bandwidth. The UWB (ultra wide band) technology has been implemented specifically for this issue. But this technology that uses the 3 – 10 GHz spectrum must deal with a lot of interference (the 3-10 GHz spectrum is crowded with interferers: Bluetooth, Wifi, WiMax,…) and a limited data rate. A solution appeared in 2001 when the FCC (federal communications commission) released the 57-66 GHz band. 9 GHz of bandwidth, unlicensed, are available and ready to be used to enable new applications. [Niknejad08_1]

But the implementation of 60 GHz radios raises some questions, specifically on the technology to use. At the beginning the implementation of 60 GHz radios has been realized with expensive technologies based on III-V semiconductors (InP, GaAs) [Smulders07]. The progress in CMOS technology opened the way to the realization of 60 GHz radios in CMOS. At the same time the implementation of analog/RF transceivers become difficult considering the degraded performance of the devices.

New architectures are needed to cope in general with the limitations of these new CMOS processes, while taking advantage of the increasing speed and density of digital techniques. Fully digital architectures have been proposed for cellular communications. These architectures process small bandwidth for broadband wireless standards.

This thesis proposes the realization of a transmitter where SDR is predominant with a standard CMOS 65nm technology for a 60 GHz wireless standard.

This first chapter gives a quick overview of the state-of-the art in 60 GHz wireless communications. It is composed as follow: first a review of principles of communication with 60 GHz waves, then a state-of-the-art of standard CMOS radios is presented followed by a state-of-the art of CMOS digital radios.

1.2. 60 GHz WIRELESS COMMUNICATIONS

A table, a chair, a bowl of fruit and a violin; what else does a man need to be happy?

Albert Einstein

In this subsection the 60 GHz wireless communication system will be presented as the new unlicensed radio that will be able to supply data rates comparable to wired standards like the gigabit Ethernet and High Definition Multimedia Interface (HDMI). Advantages and drawbacks will be discussed. Finally a summary of the wireless applications well suited for 60 GHz will be presented.

1.2.1. Background

1.2.1.1. Unlicensed band

Background on the development of 60 GHz for commercial use is presented in [Baldwin07]. In 1995 the Federal Communication Commission (FCC) opened the 59-64 GHz band for non-government communications. This band was exploited long time ago for military applications but completely ignored for commercial applications [Wells10]. In 2001, the FCC finally proposed a continuous block of 9 GHz of spectrum between 57 and 66 GHz (Europe) for wireless communications and provided a worldwide overlap of 5 GHz band. The regulatory status is summarized in Figure 1-1.

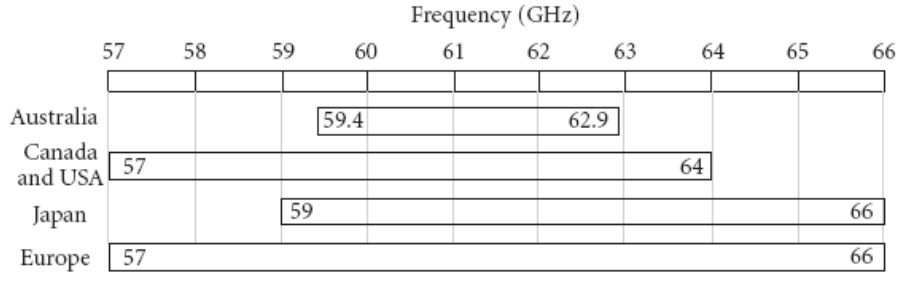

Figure 1-1: Worldwide available spectra around 60 GHz [Guo07]

Companies can benefit greatly by using this spectrum because it is unlicensed and therefore free. Other unlicensed bands exist but with less available bandwidth [KSchin98].

With such small bandwidth, wireless HDMI is not targetable. The need of 60 GHz is thus mandatory.

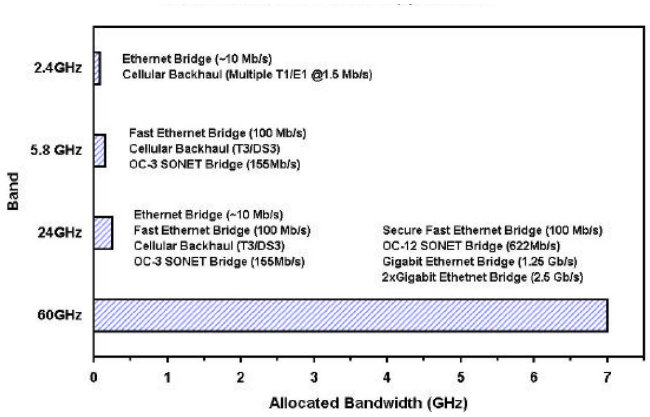

Figure 1-2: Unlicensed bands [KSchin98]

1.2.1.2. Nature of the 60 GHz wave

The 57-64 GHz band is located on the millimeter-wave band of the electromagnetic spectrum, where the wavelength varies from 10 millimeter to 1 millimeter.

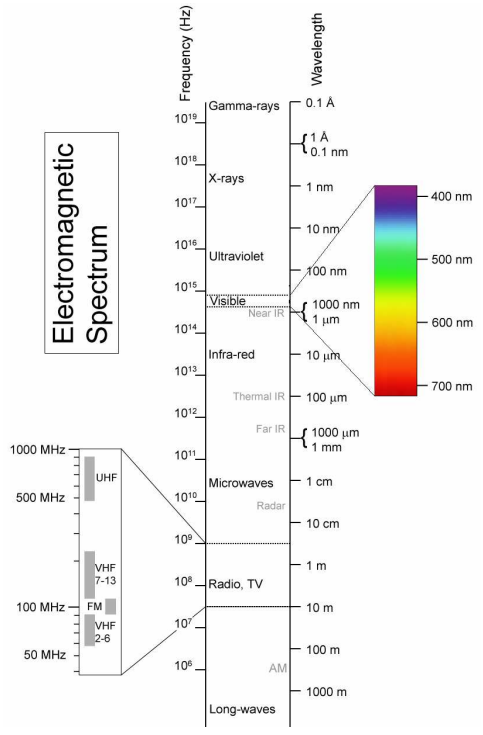

Figure 1-3: Spectrum [WikiSpectrum]

a. 0_2 absorption

A specific interest in this frequency band comes from a natural phenomenon that appears around 60 GHz: the oxygen molecule (0_2) absorbs energy around this frequency. This absorption causes high attenuation (10-15 dB/km) around 60 .The 60 GHz wave will therefore be attenuated over short distance and will not go far behind a targeted receiver.

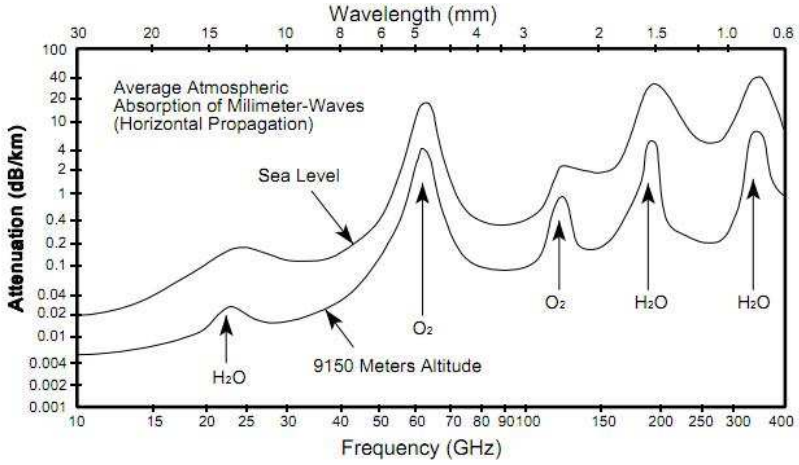

Figure 1-4: Peak absorption around 60 GHz causes by O_2 [HawaiEdu]

A consequence of O_2 absorption is the frequency reuse. As the transmitted signal from one specific transmitter is quickly attenuated, another transmitter can reuse the same frequency without interfere. Thus many links will be able to operate in a confined region [Robert07].

Another consequence of the O_2 absorption is that natural secure transmissions can be realized. As the wave is quickly attenuated, a short distance transmission can be realized without any encryption of the data [Guo07].

b. Antenna directivity

A benefit of using 60 GHz frequency is the size reduction and high integration of antenna. In order to realize efficient transmission, despite the high absorption phenomenon, the radio link at 60 GHz must use highly focused or higher gain antennas. In fact there is a fundamental relationship between the signal wavelength and the antenna size. The relationship states that as the frequency increases, the antenna becomes smaller to produce a required gain.

1.2.2. Applications and challenges

1.2.2.1. Point-to-point communication

There are various applications [Howarth05], [Robert07], [Zhu10]. The applications are mainly focused on high data rate transmission on a short distance. In Figure 1-5, different mobile or fix equipments can communicate over short distance with a data rate comparable to the wired Ethernet (1-10 Gb/s).

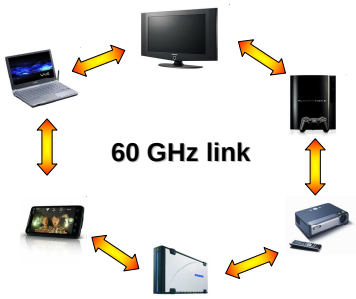

Figure 1-5: 60 GHz wireless applications

1.2.2.2. Broadband application (WLAN)

Using 60 GHz to realize long range communications seems not feasible (consequence of loss due to the 0_2 absorption). The question that arises is how to realize a WLAN based on 60 GHz communications? Can 60 GHz be used for intra-building communications? Standards like the IEEE 802.11n have already been developed with a data rates at hundreds of megabits per second [IEEE 802.11n]. Realize a WLAN based only on 60 GHz will take a considerable amount of effort (e.g.: it will be necessary to use 60 GHz repeaters for communications between rooms). A good compromise could be a hybrid 2.5/5/60 GHz WLAN solution. This solution uses lower frequencies for intra building transmission (IEEE 802.11n) and 60 GHz for short range transmission for high speed operations.

1.2.2.3. Challenges

Using 7 GHz of bandwidth around 60 GHz is very challenging in terms of RF design and implementation. The choice of the architecture and the technology (GaAs, InP, SiGe, Si) for radio implementation will have a major impact.

60GHz GaAs, InP and SiGe transceivers have already been implemented. These technologies benefit of superior gain and noise properties. Nevertheless, CMOS technology appears to be the appropriate candidate, as it provides low-costs and high integration compared to the others.

[Doan04] and [Doan05] put many efforts to highlight the different issues to the design of 60 GHz CMOS radios with advanced technology. Here are some points:

1. Parasitic elements: the parasitic elements of transistors must be well studied and understood. The parasitics contribute to reduce the frequency performance of transistors. As standard models do not fit at 60 GHz, new models must be studied and integrate all the parasitic effects. The most significant parasitics at 60 GHz are the series source, drain and gate resistances (R_S, R_D and R_G) and the resistive substrate network. The terminal inductances (L_S, L_D and L_G) model the delay effects caused by interconnections. The effects of parasitic on the device model have been covered by [Enz02].

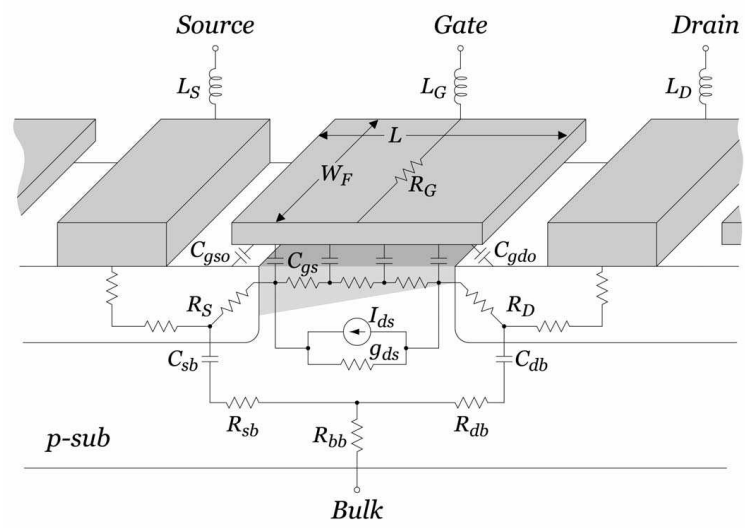

Figure 1-6: Model of one finger of NMOS transistor [Doan04]

- Special techniques of design: microwave techniques must be taken in account (e.g.: transmission line, impedance matching, electromagnetic simulations). [Niknejad07]

- Limitation of power: CMOS power amplifiers cannot provide the desired output power. Different choices are possible to cope with this limitation: power combining circuits, external power amplifier or beam-forming.

Research has been successful in recent years in CMOS Bulk technology in order to be able to offer 60 GHz radios [Niknejad10]. Different solutions of 60 GHz transmitters with either bipolar or CMOS technology are proposed in the next sections.

For further reading about 60 GHz CMOS radio development please refer to: [Niknejad08_2]

1.3. STATE OF THE ART IN TRANSMITTER ARCHITECTURES

State of the art transmitter architectures will be discussed in this following paragraph. The state of the art presents different architectures of transmitters. The first one presented is the standard analog transmitter. Last developments of this kind of transmitter for 60 GHz applications are presented. Then the concept of Software Defined Radio (SDR) is also presented. This type of transmitter has a digital architectural structure where the different parts of the standard analog transmitter are digitized. Examples of these transmitters are presented for frequencies ranging from 1 to 60 GHz.

1.3.1. Analog front end architecture

The goal of a transmitter is to translate a signal, which has been modulated in the baseband, to a certain frequency and amplify it before it is transmitted by the antenna. To reach this goal, analog transmitters are composed of three parts: The first one is the digital baseband that performs the signal modulation, the second one is the analog baseband where a DAC (digital to analog converter) performs the signal conversion and where a LPF (low pass filter) avoids aliasing, finally the third one is the RF front-end that realize the frequency translation and amplification of the signal. Depending on how one wants to realize the RF front-end two implementations exist, these called “homodyne structure” and the “heterodyne structure” and are shown in Figure 1-7 and Figure 1-21.

1.3.1.1. Homodyne structure

In a homodyne structure the frequency translation is done in one step directly to RF. The I/Q signals are first converted (digital-to-analog conversion) and filtered, then up-converted to the RF, filtered, amplified and filtered again before an emission is made on the antenna. This structure uses a single local oscillator (LO).

The homodyne architecture is illustrated in Figure 1-7.

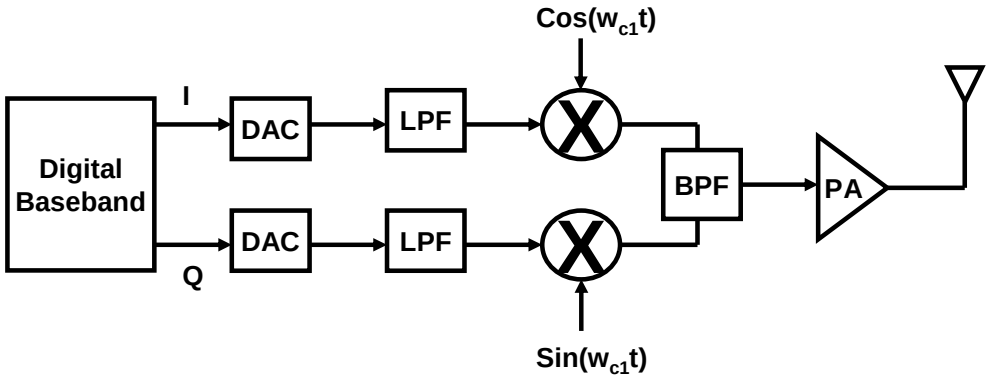

Figure 1-7: Homodyne structure

Advantages of this structure are the low power consumption (single LO and single frequency translator called a "Mixer") and the high integration. The drawback of this structure is called "Injection Pulling". As the power amplifier (PA) and the LO work at the same frequency a coupling effect exists. The output of the PA corrupts the VCO spectrum. The other negative point of this architecture is the LO generation directly at the RF frequency. The different parts that compose the transmitter are detailed in the following sub-sections.

a. Digital-to-analog converter

A lot of high speed DACs can be found in the literature. Here one example is presented. [Lin09] proposed a 12 bit 2.9 GS/s current steering DAC in a CMOS 65nm technology. It consumes 188 mW. The measured SFDR at 2.9 GS/s for an input signal of 650 MHz is 50 dB. In order to achieve a high operating frequency the segmented current steering architecture has been chosen.

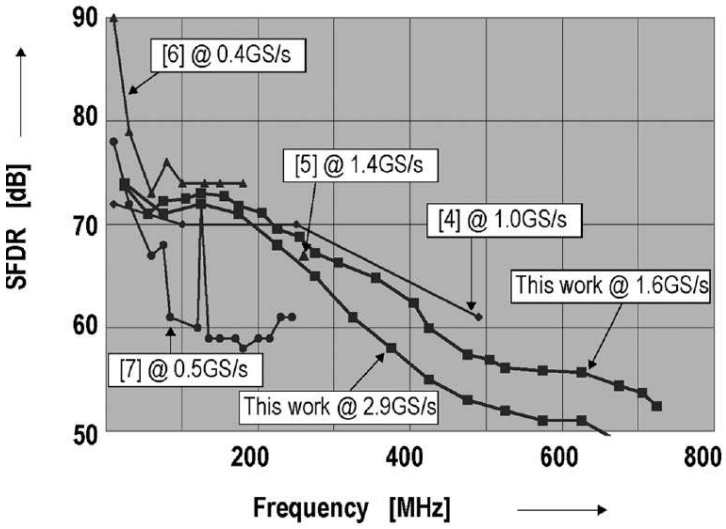

Figure 1-8: Measured SFDR vs input frequency from [Lin09]

b. Direct conversion mixer

[Lai07] reported the first millimetre wave double balanced up-conversion mixer. It works at 50 GHz. It has been designed in a CMOS 90nm technology and achieved 11dB conversion loss and a LO rejection of 26.5dB. It consumes 13.2 mW from 1.2 V. Baluns for single to differential and differential to single ended conversion have been integrated.

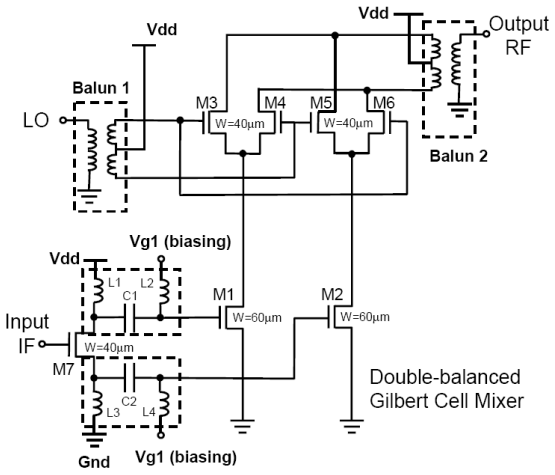

Figure 1-9: Direct conversion mixer proposed by [Lai07]

[Do07] proposed a solution with a 0.25um SiGe technology. An active balun is also implemented on chip to realize the single-differential and differential-single output conversion. At 0 dBm applied LO power the fully integrated upconversion micro mixer has a conversion gain of -6.5 dB and 0 dBm of input power under 1dB gain compression for an IF=5 GHz, a LO=55 GHz and a RF=60 GHz. It consumes 24mA with a 3.3 V supply voltage.

[Zhang08] proposed a direct conversion mixer based on a double-balanced mixer in a CMOS 130 nm technology. The mixer has a power conversion gain of better than 2 dB and an OP1dB of -5.6 dBm. The LO to RF isolation is better than 37 dB for LO frequencies from 57 GHz to 66 GHz. It consumes 24 mW.

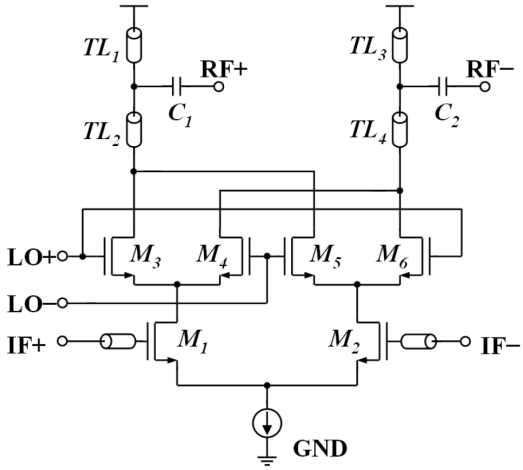

Figure 1-10: Double balanced mixer from [Zhang08]

c. LO generation

[Lee07] proposed a frequency synthesizer (58 to 60.4 GHz) in a 90 nm technology. A cross coupled structure with a LC tank and varactors is used to realize the VCO. The input reference clock is at 234.1 MHz. A 3rd order filter is integrated. The complete synthesizer consumes 80mW from 1.2V supply and occupies 0.95x1 mm^2. For 60.4 GHz the measured phase noise at 1 MHz offset is -85.1dBc/Hz.

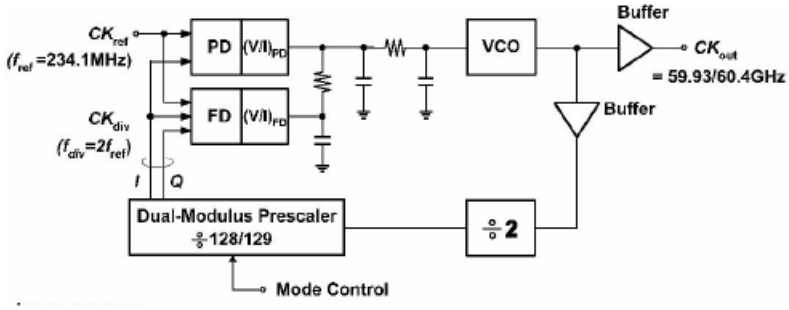

Figure 1-11: Synthesizer proposed by [Lee07]

A 60 GHz VCO (voltage control oscillator) has been introduced by [Gonzalez09]. Its central frequency is 56GHz and has a 17% tuning range. The oscillation frequency is tuned with differential varactors. It is able to address the full wireless HDMI band [WirelessHD]. The VCO is implemented in a 65nm bulk CMOS process and dissipates 15 mW from a 1.2 V

supply. The architecture of the VCO is depicted in Figure 1-12. The architecture is based on a NMOS cross-coupled pair and a LC tank.

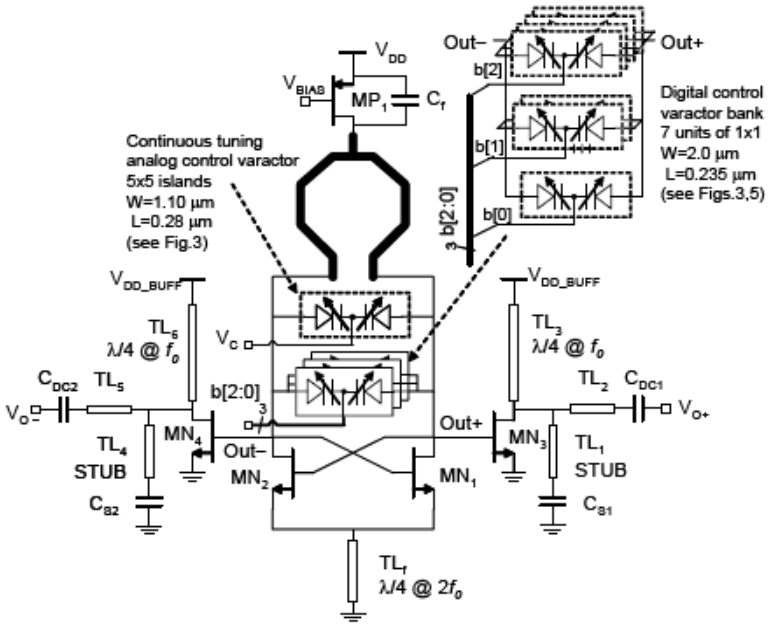

Figure 1-12: VCO proposed by [Gonzalez09]

Different solutions for PLLs have been proposed. A common idea to avoid the critical 60 GHz VCO and frequency pulling, is to use a VCO at a lower frequency combined with a doubler or tripler structure. The main advantage is that the LO generation is simplified and pulling largely reduced.

[Marcu09] proposed a PLL in a 90nm technology with a reference frequency at 117 MHz and an output at 60 GHz while using a push circuit. The VCO operates from a 0.7 V supply voltage and consumes 12 mA. Its tuning range is 4.4 GHz (59.6–64 GHz) at the push-push output. At a 10 MHz offset from the 60 GHz carrier, the phase noise is 112 dBc/Hz. This circuit has been integrated in a complete transceiver [Marcu09].

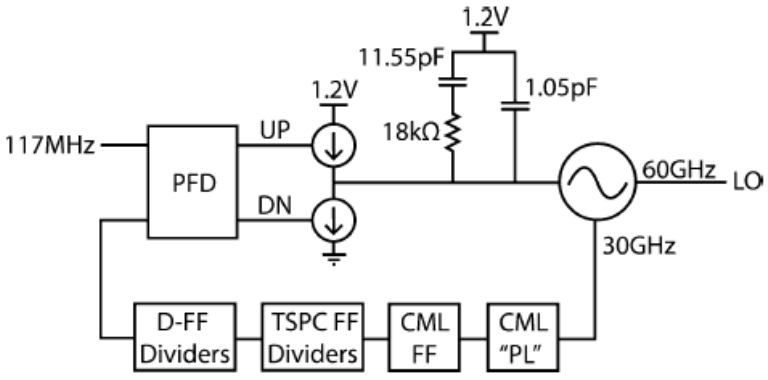

Figure 1-13: PLL at 60 GHz proposed by [Marcu09]

[Richard10] proposed the most advanced PLL for 60 GHz applications in a CMOS 65nm technology. The PLL is fully compliant with industrial standards such as IEEE 802.15.3c [IEEE09]. The PLL is composed of a push-push quadrature voltage controlled oscillator that delivers two 0°/90° LO signals around 20 GHz and a harmonic signal around 40 GHz. A 36 MHz clock is used a sreference. The PLL consumes 80mW. The analog part is supplied by 1.2V and the digital part supplied by 1.8V. The PLL occupies 1.6 x 1.9 mm^2. Its phase noise (20.88 GHz) is -100dB/Hz at 1 MHz offset and -126dBc/Hz at 10 MHz offset. The frequency synthesizer is depicted in Figure 1-14.

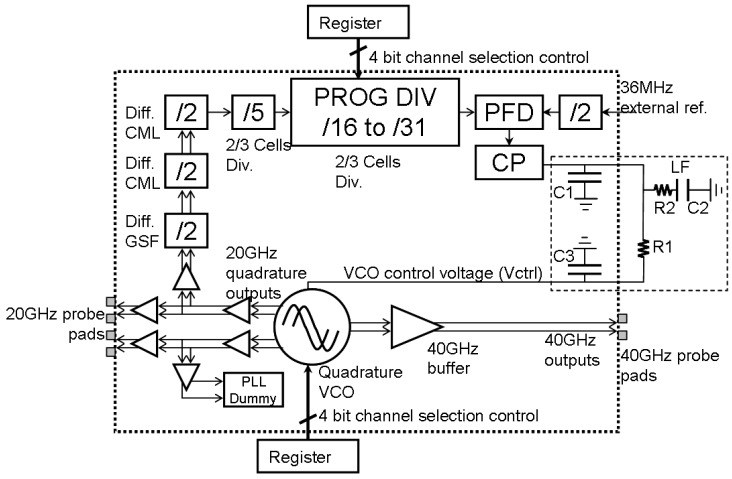

Figure 1-14: PLL architecture by [Richard10]

d. Power amplifier

[Pfeiffer06] reported a solution in a bipolar SiGe 130nm technology. The power amplifier is integrated with fully automatic level control. It achieves a power gain of 18 dB with output power of P-1dB and a PAE of 12.7 %. The PA is composed of two single stages in a push-pull amplifier topology. It consumes 63 mA on a 4V supply voltage.

[Heydari07] proposed a PA in a CMOS 90 nm technology. It is composed of two stages and has a measured power of gain of 9.8 dB. The 1 dB compression is equal to 6.7 dBm with a PAE of 20 %.

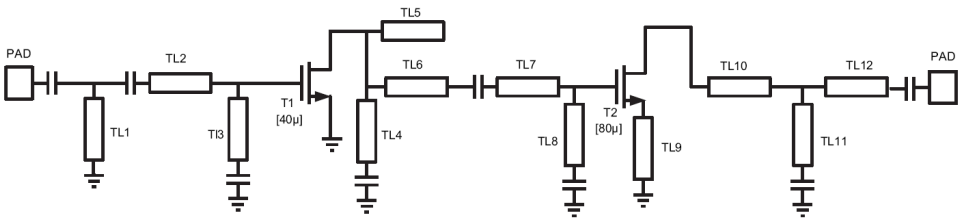

Figure 1-15: PA in CMOS 90nm technology by [Heydari07]

[Chowdhury08] demonstrated a transformer coupled two stages differential PA in a 90nm technology. By using transformer impedance matching and differential to single conversion can be performed. The PA operates from a 1V supply and achieves a 1dB compression point of 9 dBm and a saturated power of 12.3 dBm. The PAE is 32%.

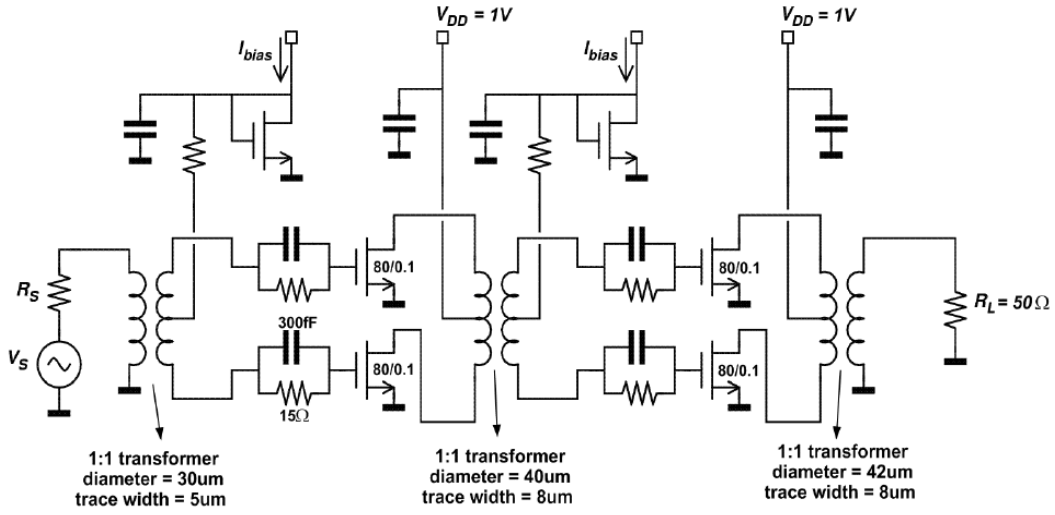

Figure 1-16: Transformer coupled two stages differential PA from [Chowdhury08]

[Siligaris09] proposed a PA in a 65nm CMOS SOI process. The PA is composed of two cascode stages. Input, output and inter stage matching networks are realized with coplanar wave guide transmission lines. The PA operates from 1.2V (going to 2.6V) and achieves a saturated output power of 10 dBm (going to 16.5dBm). The PAE is higher than 20 %.

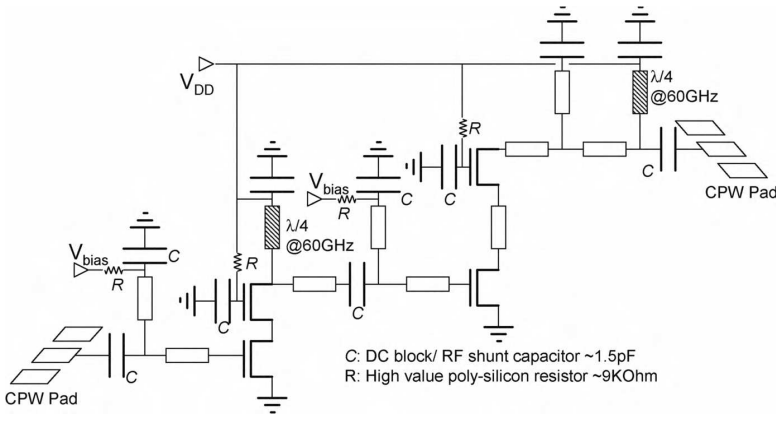

Figure 1-17: PA in 65nm CMOS SOI proposed by [Siligaris09]

[Martineau10] reported a PA for the 53-68 GHz band with a 8 way combiner in a standard 65nm CMOS technology. The PA has been designed to target the IEEE 802.15.3c wireless HD standard. OFDM signals are used in this standard, thus this PA had high

requirements on linearity. It operates at a 1.2V and achieves a saturated output power of 16.6 dBm. The PAE is 5%. The complete PA is composed of 8 differential PAs connected together with a zero degree power splitter at the input and a zero degree power combiner at the output.

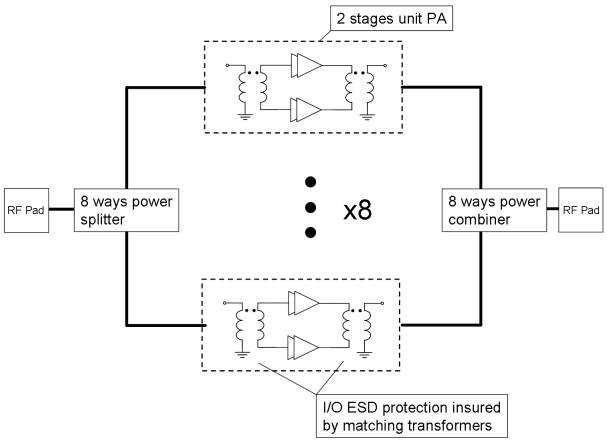

Figure 1-18 : PA with a 8 way combiner in 65nm CMOS technology by [Martineau10]

1.3.1.2. Homodyne transmitters at 60 GHz

[Wicks09] (Illustrated in Figure 1-19) proposed a direct-conversion in a 130 nm CMOS technology. The transmitter achieved a P_{sat} of 6.5 dBm. The transmitter has analog baseband I and Q differential inputs. These signals are amplified and filtered by variable gain amplifiers (VGA). The outputs of the VGAs are up-converted by a double balanced mixer. I and Q channels are combined by a power combiner. Finally the signal is amplified and filtered. The transmit part consumes 515mW. No information is given on the quality of the transmission: capacity, bit error rate (BER), etc.

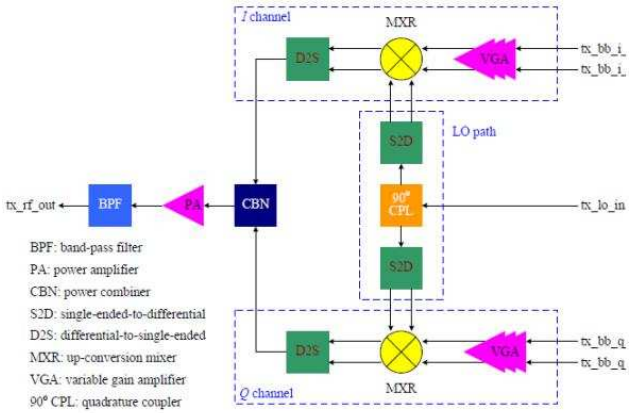

Figure 1-19: [Wicks09] transmitter architecture

[Lee10] proposes a low power solution by using an OOK modulation. It has been designed with a 90 nm CMOS technology and consumes 183 mW. The transmitter is composed of a 60 GHz VCO, an on-off keying modulator and a power amplifier. The input data stream directly modulates the 60 GHz clock before it is amplified by the PA. Antennas are integrated on chip (folded dipole antenna and patch array). A similar work has been realized by [Juntunen10] in a 90 nm technology for a power consumption of 156 mW.

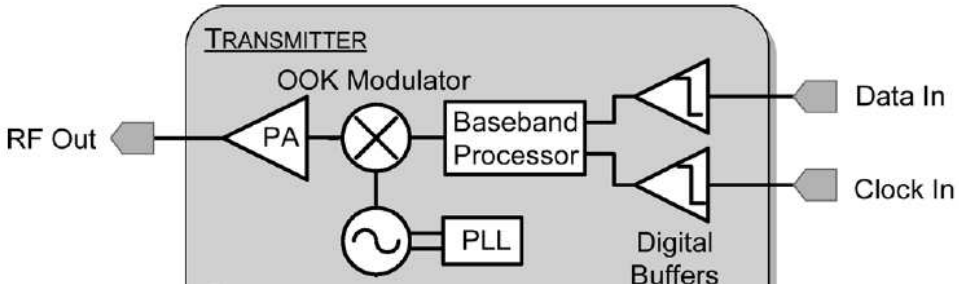

Figure 1-20: Direct modulator at 60 GHz by [Juntunen10]

[Okdada11] developed a solution with a 65nm CMOS technology compliant with the IEEE 802.15.3c for 16 QAM, 8 PSK, QPSK and BPSK modulations. It achieves a very high data rate from 8 Gb/s in QPSK mode to 11 Gb/s in 16 QAM mode. The power consumption is 186 mW. The transmitter is composed of a 4 stage PA, I/Q mixers and a quadrature oscillator. The PA output power is 9.5 dBm at 1dB compression and a PAE of 8.8 %. The architecture for the mixer is a standard double balanced Gilbert cell. A similar work has been presented by [Takayama10].

1.3.1.3. Heterodyne transmitters at 60 GHz

In this structure the frequency translation is done in two steps. The signal is first up-converted to an intermediate frequency, filtered, up-converted to the radio frequency, amplified and finally filtered again before emission on the antenna. This structure is illustrated in Figure 1-21.

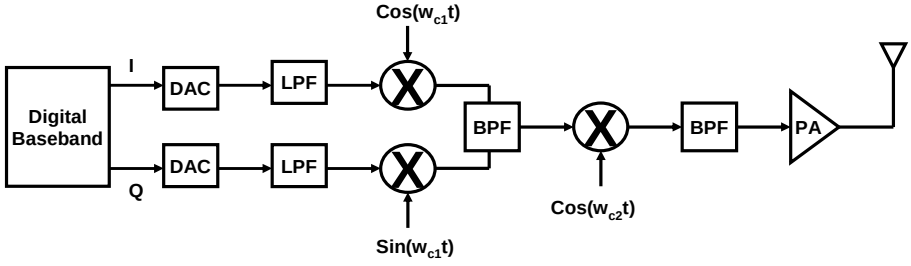

Figure 1-21: Heterodyne structure

As the frequency translation is done in two-stages, the filter design is easier. This also avoids couplings, as each stage operates a different frequency. The major drawback is that this architectural structure consumes more because it involves more elements: a synthesizer, a mixer and an additional filter. Moreover, the rejection of the image frequency must be taken into great consideration because these images can degrade the performance of the transmission. The choice of intermediate frequency then becomes a compromise between a high frequency synthesizer and a highly selective filter, which can require the use of an external filter.

[Reynolds07] proposes a solution with a SiGe BiCMOS 130nm technology. A complete transceiver has been realized with a very high level of integration and excellent RF performance. A multi-mode modulator is embedded in the IF up-conversion mixer. This provides a simpler way to generate an RF modulated waveform directly from a digital bit-stream in FSK, BPSK, MSK and other similar signalling schemes. The synthesizer is integrated. The output frequency range of the synthesizer is 15.3 to 18 GHz, which feeds a frequency tripler. Different tests have been done and a video system has been demonstrated, with an uncompressed wireless HDTV signal sent over a distance of 2.5m. The transmitter consumes 822mW. P.A. output power is 12 dBm.

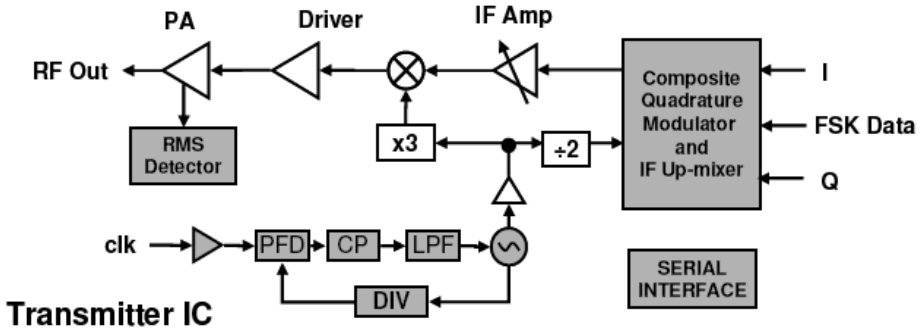

Figure 1-22: Heterodyne transmittere from [Reynolds07]

[Reynolds08] proposes a solution with a 65nm CMOS technology. It operates on a 1.2 V supply voltage and consumes 29 mW. The transmitter is composed of two mixers and a PA. The PA architecture is a single stage and single ended amplifier. It achieves a peak power gain of 5.5 dB, 1 dB compression point of 6 dBm and a saturated power of 9 dBm. The PAE is 8.5 %. The mixer is based on a standard Gilbert Cell.

See also [Pinel08] for standard heterodyne structure in a CMOS 90nm technology.

[Siligaris11] proposes a complete transceiver in a CMOS 65nm technology. The transmitter is composed of the analog baseband filters, the mixers and the quadrature LO generation and a PA. The proposed transceiver is fully compliant with the WirelessHD standard. It can perform both OFDM and single carrier modulations. The module occupies an area of 13.5×8.5mm². It consumes 1.357W in the transmit mode (357mW for the transmitter and 1W for the PA).

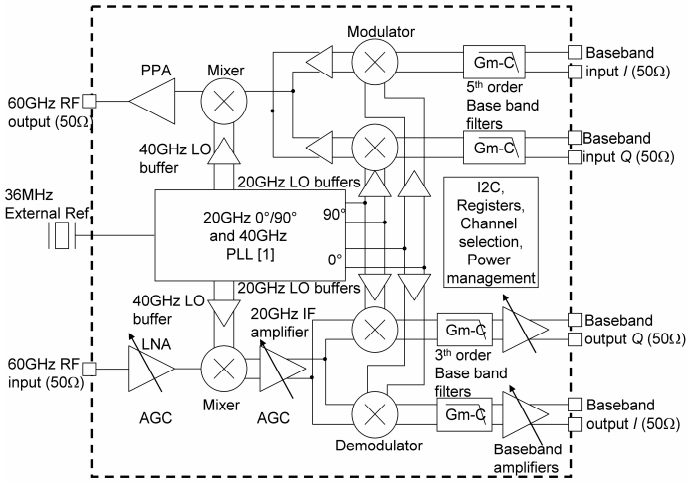

Figure 1-23: Heterodyne transmitter compliant with the WirelessHD standard by [Siligaris11]

1.3.2. Digital RF front end architecture

In this section the digital RF transmitter will be discussed. The structure presented previously, homodyne and heterodyne, are still valid here. In a digital RF stucture, the different components that compose the analog transmitter are digitized. This tends to digitize the analog/RF functions which come from a development which is called Software Defined Radio (SDR). In a first time, SDR is introduced, and then different possible implementations are presented.

1.3.2.1. Software Defined Radio

SDR refers to a multi-standard radio system where a single transceiver is able to be reconfigured to target different radio standards. SDR becomes more and more interesting, considering the number of different standards that a mobile phone must handle. Here is a list of the different standards available today in a mobile phone:

- 2G : GSM and DCS1800 (Europe), IS-95 (US)

- 3G: UMTS (Europe), CDMA2000 (US), TD-SCDMA (China)
- 4G: LTE, WiMAX
- Broadband access: Wifi
- Short-range: Bluetooth (today) and 60 GHz (tomorrow).

The ideal architecture able to manage all the standards is illustrated in Figure 1-24

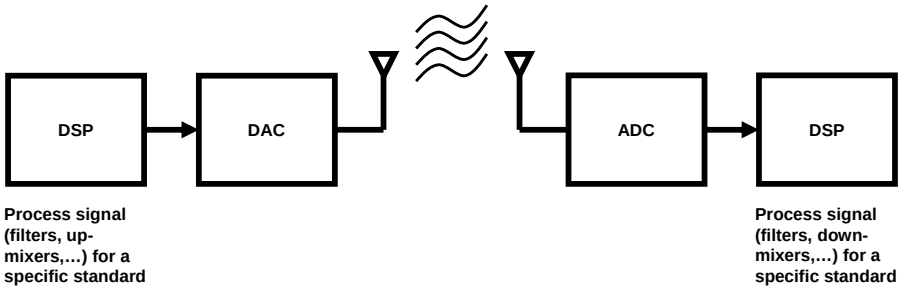

Figure 1-24: SDR universal architecture

This structure is multifunctional. On the transmission side, a digital signal processor (DSP), connected to a DAC, would be able to be reconfigured when one wants to use a specific standard. On the reception side, an ADC converts the signal that comes from the antenna and processes the ignal in the digital domain in order to recover the data sent by the emitter.

1.3.2.2. Digital RF implementation for broadband signals

[Eloranta08] proposed a direct-digital RF modulator in 0.13um CMOS for wide band multi-radio applications. This architecture is depicted in Figure 1-25.

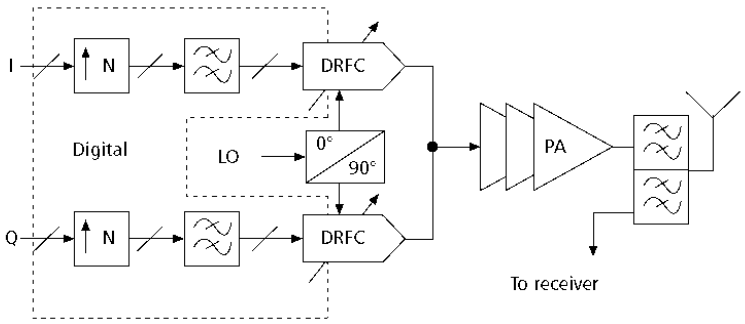

Figure 1-25: Direct-digital RF modulator [Eloranta05]

The multimode capacity of this architecture has been demonstrated with WCDMA, EDGE and WLAN requirements. The chip is implemented with standard 0.13um 1.2 V digital CMOS with a total silicon area of 4mm^2.

First, the digital baseband signal is up-sampled and then filtered by a cascade of basic Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters (interpolators). In a conventional analog architecture, the replicas of the sampled signal are filtered with an analog filter after the D/A conversion. As in the proposed architecture there is no analog baseband filters, the signal is up-sampled by a factor sufficiently large to guaranty after filtering that images are far away from the transmitter band. Filters are implemented as very simple FIR and IIR filters with 1 coefficient. Multiplications are implemented as shift operations.

Once the I/Q signals have been up-sampled and filtered, they are converted and translated to an RF frequency by a block called Digital-to-RF converter (DRFC). The D/A conversion and the frequency translation are done in the same block. This circuit is based on a conversion cell of a traditional current-steering DAC, but with the current source and switch pair transistors replaced by a double balanced mixer structure. Considering the large difference between the LO frequency and the data frequency, no synchronization has been implemented. The output signal is the sum of the different current from the different basic cell, as it is done in a traditional current steering DAC. The conversion cell is depicted in Figure 1-26.

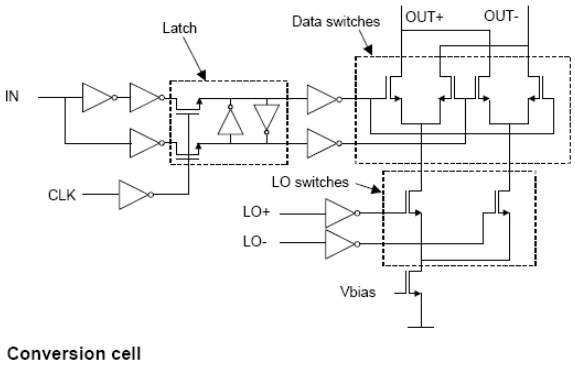

Figure 1-26: DRFC conversion cell

[Pozsgay08] uses a different approach. He proposes a Fully Digital 65nm CMOS Transmitter for the 2.4-to-2.7GHz WiFi/WiMAX bands using 5.4 GHz Delta-Sigma modulation and RF DACs. The architecture is depicted in Figure 1-27. Without going into details in the WiFi/WiMAX standard, one can understand the idea of this transmitter. First

the baseband signal is up-sampled and filtered by FIR and IIR filters (interpolators). The effect is to filter images that are created due to sampling and to push new images outside of the band in order to avoid aliasing between different channels. Then the filtered baseband signals pass through delta-sigma modulators with a high oversampling ratio (OSR) and a specific noise transfer function. The use of Delta-Sigma modulator decreases the number of bits of the DAC. Finally the RF DAC realizes the frequency translation and D/A conversion.

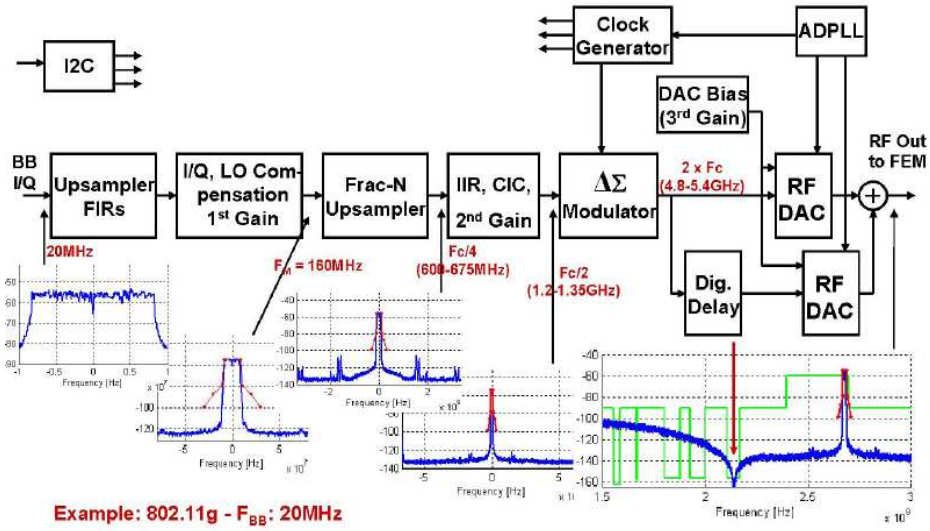

Figure 1-27: Fully digital CMOS transmitter [Postgay08]

The RF DAC architecture is presented in Figure 1-28

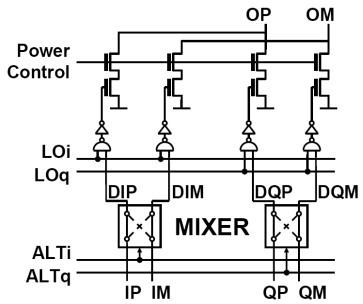

Figure 1-28: RF DAC

The I/Q BB signals, are translated by a digital mixer driven by ALTI and ALTQ signals, which are generated by division-by-2 from the PLL output. ALTI and ALTQ are shifted by 90° in order to realize the quadrature. The up-converted signals are then re-synchronized by the LOp/LOm PLL outputs by an AND gate. Figure 1-28 represents one cell of the RF DAC. As in a current steering DAC, segmentation has been done between

MSBs and LSBs which leads to RF DAC cell of different sizes or multiples of unitary RF DAC cell. The output current of the cell is set by the power control bias voltage.

1.3.2.3. 60 GHz transmitters with digital capabilities

Digital capabilities have been introduced in 60 GHz transmitters with the works of [Niknejad09] and [Tomkins09]. Both of them propose to translate digital data directly at 60 GHz with a DRFC which is a block that combines the digital-to-analog conversion and the RF translation.

A first interesting solution of homodyne architecture for a 60 GHz wireless transmitter with SDR capabilities has been proposed by [Niknejad09]. A complete transceiver has been designed in 90nm CMOS. Here we focus only on the transmission part. The transceiver is depicted in Figure 1-29.

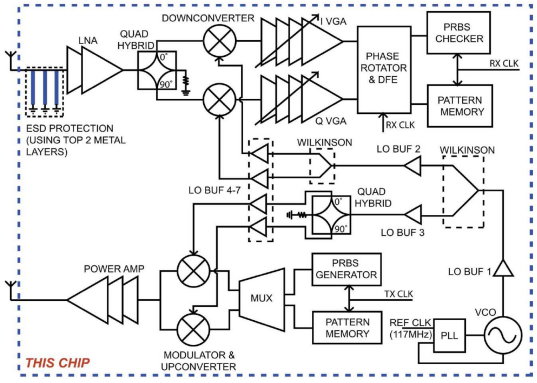

Figure 1-29: 60 GHz transceiver [Niknejad09]

The transmitter is composed of a digital baseband, a modulator – up-converter and a power amplifier. The modulation used is a single carrier QPSK. The modulator combines the DAC function and the mixer function. LO is generated by a PLL at 60 GHz. Due to the direct QPSK modulation of the RF carrier, the signal occupies a large bandwidth. The transmit part consumes, with a 1.2 V supply, 170 mW while transmitting 10 dBm. A data rate ofi 4Gb/s is achieved with a QPSK over 1m with less than 10^{-11} bit error rate (BER).

[Tomkins09] also proposes a direct conversions solution. This solution is realized with a 65nm technology. The system utilizes direct BPSK modulation at 60 GHz and does not include the power amplifier. The transmitter input accepts baseband digital non-return-to-zero (NRZ) data at rates beyond 6 Gb/s. NRZ data, produced off-chip, is applied to the BPSK modulator which directly modulates the 60 GHz transmitter The chip complete chip consumes 374 mW from 1.2 V which reduces to 232 mW for a 1.0 V supply. It occupies 1.28 x 0.81 mm^2. The 60 GHz LO signal is provided on chip.

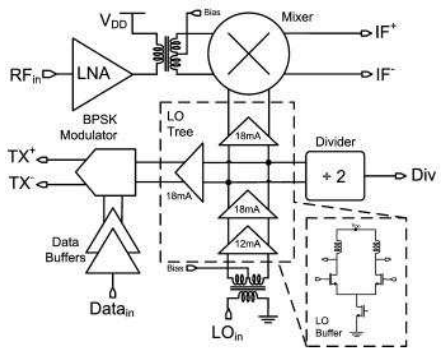

Figure 1-30: [Tomkins09] direct conversion architecture

1.4. CONCLUSION

An overview of 60 GHz applications and physical nature of mmW wave has been developed. Then both analog and digital transmitter architectures have been presented in order to understand the concepts that will be used in the proposed architecture in the next chapter.

Standard analog/RF architectures have been implemented in different technologies (III-V components and CMOS). High level of integration has been attained with architectures like [Marcu09] or [Sigiliaris11].

On the other hand, digital architecture have been developed for narrowband radio standard (UMTS, WiFi, WiMAX, …). These solutions take benefit of the technology scaling.

No fully digital implementations of 60 GHz wireless transmitter exist, however some architectures tend to integrate new functionalities that are normally used for narrowband architecture such the DRFC [Niknejad09].

The unsolved problem of direct modulation of the RF signal [Marcu09] is that the baseband digital images pollute the spectrum after conversion and translation. A filter should be implemented in the digital domain in order to attenuate the remaining images and target an industrial standard.

Based on these observations, the architecture targeted in this work is presented in Chapter 2.

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2. CHAPTER TRANSMITTER ARCHITECTURE

"Everything should be as simple as it is, but not simpler."

Albert Einstein

This chapter presents the targeted architecture which tends to digitize part of a wireless 60 GHz transmitter.

Two kinds of digital architectures are presented, homodyne and heterodyne. The homodyne architecture is based on a DRFC (digital-to-RF converter) in order to realize a direct conversion of the digital data stream to the RF frequency. The digital data stream at the baseband output needs to be oversampled and resulting replicas of the signal at multiples of the initial sampling frequency have to be filtered. The study of this interpolator is presented in detail in this chapter. In the digital heterodyne architecture, a digital IF is introduced in order to relax the local oscillator (LO) generation constraint. Choices are motivated and at the end the architecture that has been chosen is the homodyne one.

Then Matlab simulations of the baseband of the chosen architecture are presented. First the OFDM signal is constructed as a test vector for the interpolator simulations. A first interpolator architecture is presented. This architecture is based on cascaded FIR filters, two at 5 GHz and two at 10 GHz. The number of coefficients/filter has been reduced to a minimum following a dichotomy approach.

Finally this chapter focuses on how to simplify the interpolator while quantizing coefficients to powers of two. A GA (Genetic Algorithm) has been developed to optimize FIR filters with powers of two coefficients based on a frequency domain specification.

2.1. SIGNALS AND SYSTEMS THEORY

This section contains an introductory treatment of discrete-time signals and systems. Sampling theorem, finite impulse response (FIR) filters and interpolators are reviewed for a better understanding of the following sections.

2.1.1. Sampling

An analog signal (function) is periodically measured every T seconds (sampling). The result is the sampled function which can be calculated as the multiplication of the time signal and the Dirac sequence. In the frequency domain the signal is represented as a narrow band signal. Sampling in the time domain is represented as a Dirac sequence in the frequency domain. The sampled frequency function is the convolution of the frequency signal and the frequency Dirac train.

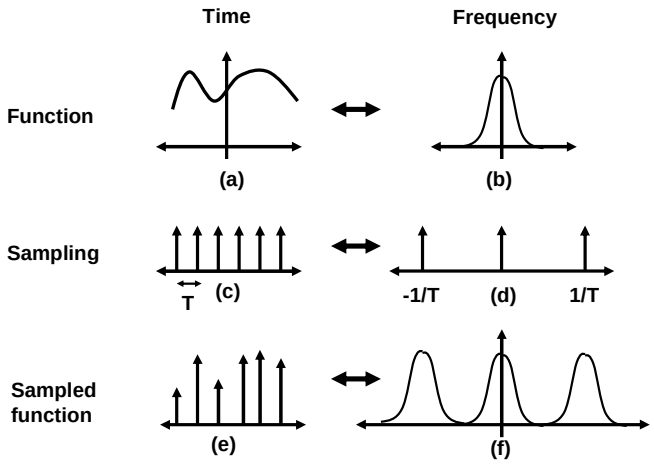


Figure 2-1 : Sampling in time/frequency domain

2.1.2. Up-sampling

The up-sampling process is used to increase the sampling rate of a signal. The up-sampling ratio is usually an integer, multiple of the original sampling frequency. Let us consider a discrete time signal s(k). Up sampling the signal is no more than adding zeros between each sample in s(k). In reality a sample and hold function is preferred which holds the value between each sample in s(k). The difference between “zero stuffing” and

sample and hold is notable. Zero stuffing does not change the spectrum of the signal, sample and hold attenuates images following a sinc function.

2.1.3. FIR filters

A digital filter realizes a function similar to an analog filter, but dealing with numbers. Digital filters offer many advantages over analog filters. They are programmable and reliable, free from component drift and matching errors and can be designed to have linear phase.

FIR (Finite Impulse Response) filters are a type of digital filter. Their impulse response is finite, means that the response settles to zero in a finite number of sample intervals. The linear time invariant (LTI) convolution of Eq 2-1 describes the general form of digital filters:

$$y(n) = \sum_m a_m x(n-m) \qquad \textbf{Eq 2-1}$$

The other type of digital filter is the IIR (infinite impulse response) filter and is not studied here. They contain feedbacks and have stability issues and moreover phase response is in general highly non-linear.

The FIR can be seen as an extension of a moving sum or as a weighted moving average. Where x(n) represents a collection of samples as $x=[x_0, x_1, x_2, \ldots, x_L]$ and a_m represents a set of coefficients $a=[a_0, a_1, a_2, \ldots, a_L]$. The impulse response of a FIR filter is the set of coefficients used in the FIR. The impulse, a '1' followed by '0' samples, is applied to a FIR filter, the output of the filter will be the set of coefficients, as the '1' sample moves past each coefficients in turn to form the output. This kind of filter is unconditionally stable. This property is obvious as described in Eq 2-1; the output is a linear combination of inputs (delayed). Moreover FIR filters can be designed to be linear phase by making the coefficient sequence symmetric.

FIR filters can be studied easily in the frequency domain. In the time domain, the output of the FIR is the convolution between the signal and the impulse response of the FIR. In the frequency domain, the convolution become a multiplication, thus the output of the FIR filter in the frequency domain is the multiplication of the signal and the FIR frequency response. An ideal low pass filter keeps all frequency components of a signal

below a designated cut-off frequency, w_c, and rejects all frequency components of a signal above w_c, according to:

$$H(f) = \begin{cases} 1, 0 \le w \le w_c \\ 0, w_c < w <= \pi \end{cases} \qquad \textbf{Eq 2-2}$$

As expressed in Eq 2-2, basically a low pass filter is a box in the frequency domain. The inverse Fourier transform of this frequency signal is a sinc function. In the time domain, the signal must be convoluted by the sinc function to realize a perfect low pass filter which is not possible because the FIR would have an infinite number of samples.

$$\sin c(t) = \frac{\sin(2.\pi.f.t)}{2.\pi.f.t} \qquad \textbf{Eq 2-3}$$

In reality the filter's response is characterized by different parameters (pass-band, transition band and stop-band) and for simplicity (do not deal with time domain) these parameters are studied in the frequency domain as shown in Figure 2-2.

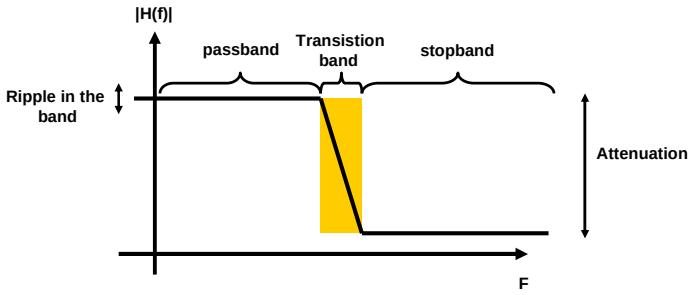


Figure 2-2 : Filters frequency specifications

The passband parameter is basically the bandwidth of filter where the signal should not be attenuated. The ripple is a parameter that specifies the tolerated amount of variations in the band. Obviously one wants this ripple as small as possible in order to do not add distortion in the band. The stopband is by contrast highly attenuated. The transition band is the transition between the passband and the stopband.

Finding the filter's length and coefficients is called filter design, based on the parameters as passband, stopband, … Once the frequency response is defined, one can transform the frequency response into a discrete time response through the inverse discrete Fourier transform. Coefficients of the filter are obtained by sampling the discrete time response.

For continuous time, one may use the Fourier transform or the Laplace transform. For discrete time signals and systems we generally use the "Z transform". The Z transform is a generalisation of Laplace's transform, meaning that magnitude and stability can be studied directly. The following paragraph gives an introduction to the Z transform. For advanced lecture in digital signal processing one may refer to [Orfanidis98]. The Z transform is defined as:

$$S(z) = \sum_{k=0}^{+\infty} s(kT).z^{-k} \qquad \textbf{Eq 2-4}$$

Where s(kT) are samples given at the sampling frequency 1/T. An interesting property is the time shift expressed as:

$$Z\{x(n-k)\} = z^{-k}x(z) \qquad \textbf{Eq 2-5}$$

z^{-k} is called a delay operator. Now the FIR transfer function in the Z domain of the equation Eq 2-1 can be expressed as:

$$H(z) = \sum_{i=0}^{N} a_i.z^{-i} \qquad \textbf{Eq 2-6}$$

Notice that replacing z by e^{jwT} in Eq 2-6 yields the frequency domain transfer function and so it is possible to compute magnitude and phase.

A specific study of the low pass filter FIR specifications needed in this work will be presented later in this chapter.

2.1.4. Interpolator

An interpolator is composed of an up-sampler and a FIR filter. The interpolated values added by the up-sampler are calculated by an FIR filter. This is illustrated in Figure 2-3 with a 4 time interpolator.

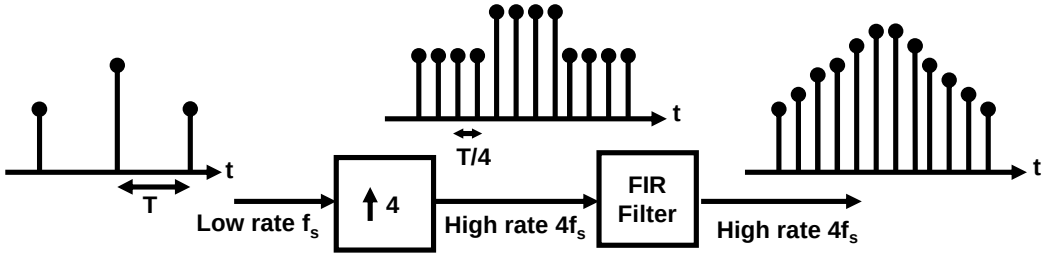


Figure 2-3: Interpolator (up-sampler & FIR filter) in time domain

The frequency response of this filter is shown in Figure 2-4.

The up-sampling creates a higher-rate signal whose spectrum is the same as the original over the original bandwidth, but because of the sample-hold function a sinc attenuation appears at the new sampling frequency. The low-pass filter eliminates the images up to the Nyquist frequency.

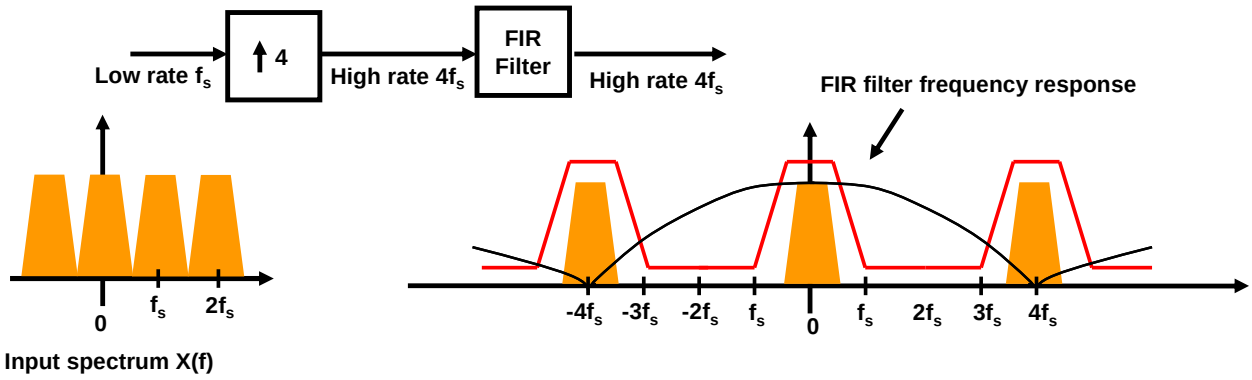


Figure 2-4: Interpolator (up-sampler & FIR filter) in frequency domain

2.2. GLOBAL TRANSMITTER ARCHITECTURE

Two architectures able to respond to the problematic of the thesis are presented. The first one is based on a homodyne structure and the second on the heterodyne structure. These architectures apply digital radio concepts applied to 60 GHz transmitters.

2.2.1. Homodyne structure

As shown in the previous chapter Homodyne structures can be used for analog or digital transmitters. The proposed Homodyne architecture is depicted in Figure 2-5. This architecture implements the Homodyne structure because the frequency translation to RF is done in one step. This architecture takes benefit of digital radio concepts by removing the analog baseband filter and replacing it by a digital equivalent.

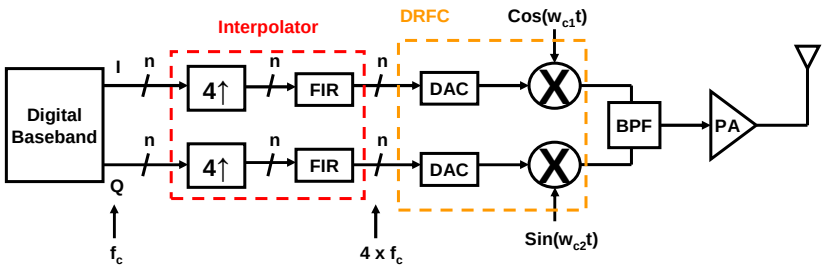


Figure 2-5: Homodyne transmitter with SDR capabilities

For the considered standard, the outputs of the digital signal processor have a sample rate of f_c=2.5 GS/s. At the present state of the art of technology, it seems feasible to oversample this signal at 10 Gs/s. Images of the original signal appear at multiples of the original sampling frequency. To meet the standard's spectrum mask requirements and avoid corruption of adjacent channels, filtering of images prior to conversion to the analog domain is necessary. After filtering and conversion to the analog domain, the first image appears at a 10GHz offset (see Figure 2-6). Therefore this image falls out of the standards frequency band, regardless of the channel used. The remaining images can be eliminated by the RF band filters present in the systems. The architecture is therefore compatible with the standard's requirements. However, stringent requirements are now placed on the digital interpolation filter (works at 10 GHz) and the DRFC (direct conversion to 60 GHz).

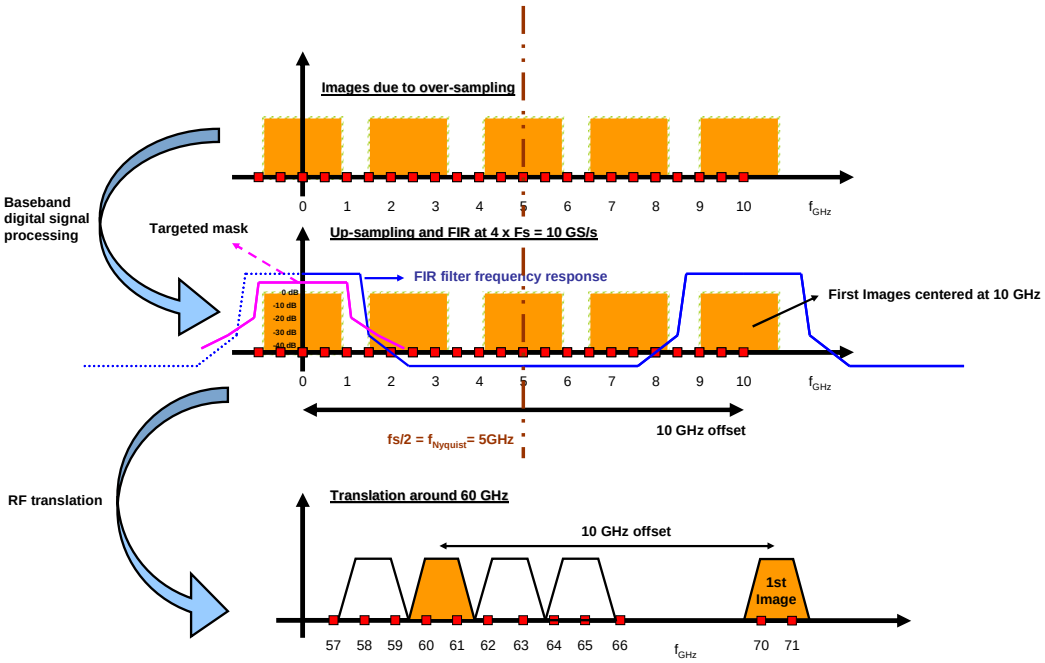


Figure 2-6: Digital signal processing applied in the transmitter

Till now the sampling process has been considered as a “perfect sampling”. Mathematically, sampling is represented as the multiplication of the signal by a Dirac sequence. One must consider that in reality images are attenuated following a sinc function (not shown on Figure 2-6) because of the replacement of the Dirac sequence by a pulse sequence. The attenuation provided by the sinc function at 9 GHz is – 19.36 dB. The other blocks in the chain (DRFC and PA) are naturally “narrowband” and will attenuate signals outside their bandwidth.

The necessary in-band SNR can be found with or without taking account of the over-sampling. To obtain an in-band SNR of 40 dB, 5.2 bits are necessary when taking in account the over-sampling. To obtain an in-band SNR of 40 dB without taking in account the over-sampling, 6.2 bits are necessary. The 4 time oversampling reduces the noise by 6 dB (1 bit).

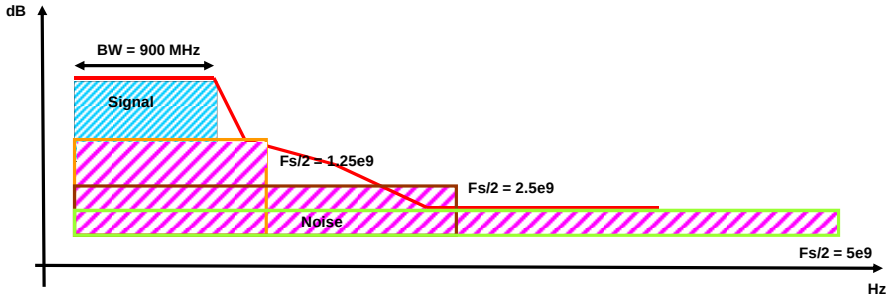


Figure 2-7: In-band SNR computation with and without oversampling by 4

Recall that OFDM signals suffer of high PAPR (10 dB is an average value) the number of bits must be increased by 1.95 which means that the input words are quantized on (5.2 + 1.9 bits) 7 bits.

The DRFC translates signals directly around 60 GHz. Special care must be taken with the LO generation. Four channels must be placed around 60 GHz. PLLs able to generate 60 GHz LO signals have been presented in the state-of-the art, see [Lee07], [Marcu09] and [Richard10].

Channel number	Channel center frequency
1	58.320 GHz
2	60.480 GHz
3	62.640 GHz
4	64.800 GHz

Table 2-1: Channel center frequencies for IEEE TG3C.15.3C in the case of the homodyne structure

The digital to RF converter has been presented previously in different works applied to digital radio for broadband mobile standards and for 60 GHz radio. Here specifications are quite different. A summary of the different constraints are presented in Table 2-2.

	Eloranta08	Poszgay08	Marcu09	Flament09	This Work
Bandwidth	4 MHz	20 MHz	-	1700 MHz	1700 MHz
Sampling frequency	300 MS/s	5,4 GS/s	5 GS/s	5 GS/s	10 GS/s
Number of bits	10	11	3	4	7

Table 2-2 : DRFC performances comparaison

The constraints applied to the DRFC in this work are different. Seven bits linearity is needed to target the signal-to-noise ratio (SNR) of 40 dB while the baseband part works at 10 GS/s. Clearly the architecture proposed by [Eloranta08] is not feasible for a direct conversion at 60 GHz because each conversion cell should work at 60 GHz. The architecture proposed by [Poszgay08] can't be used directly at 60 GHz, this would suppose that one is able to switch on and off a current source at 60 GHz which is not feasible. Architectures such [Marcu08] and [Flament09] are more suitable for a direct conversion at 60 GHz. The DAC part of these two last architectures does not work at 10 GS/s but state-of-the art literature proposes standard current steering DAC at high frequency till 12 GS/s in a standard CMOS technology [Savoj08].

2.2.2. Heterodyne structure

The Heterodyne structure is a variant of the Homodyne structure; it is presented in Figure 2-8.

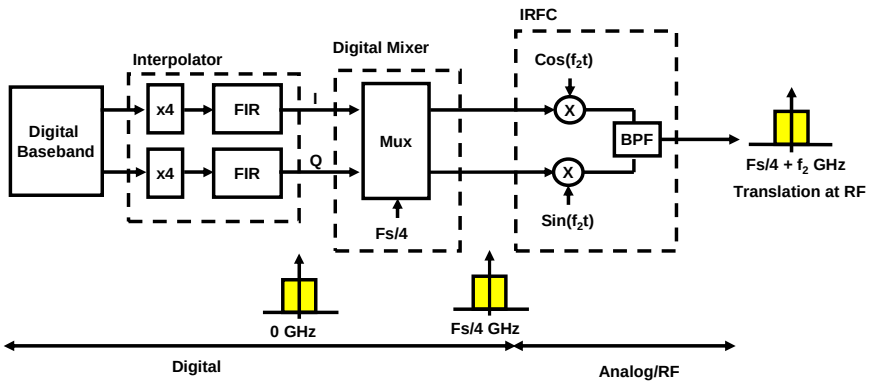


Figure 2-8: Heterodyne transmitter with SDR capabilities

Like in the previous architecture, the first part is the interpolator and is used to remove images. The signal is then passed in a digital mixer. The digital mixer is based on digital signal processing. No analog mixers are used in the digital IF mixer. It translates spectrum from DC to the IF frequency. This block is detailed in the next section. Finally the signal is converted and translated to the RF frequency by the intermediate frequency to RF converter (IRFC). This block is also detailed in next section.

2.2.2.1. Digital IF mixer

a. Quadrature digital modulator

The quadrature modulator performs a digital quadrature modulation to an IF carrier frequency. It allows the quadrature modulation to be performed in the digital domain with high precision and perfect I/Q channel matching.

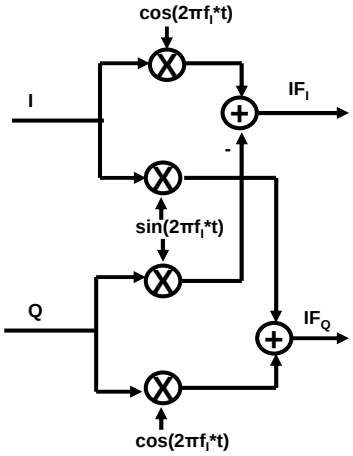


Figure 2-9: digital quadrature modulator

The output of IF_I and IF_Q are equal:

$$IF_I(n)=I(n)\cos(2\pi f_1 n)- Q(n)\sin(2\pi f_1 n) \quad \textbf{Eq 2-7}$$

$$IF_Q(n)=Q(n)\cos(2\pi f_1 n)+ I(n)\sin(2\pi f_1 n) \quad \textbf{Eq 2-8}$$

After manipulation one can show that on the IF_I path only the negative real component is present and that on the IF_Q path only the negative imaginary component is present. Considering that the digital modulator is directly followed by a quadrature analog mixer, the final output is composed of the negative component. By replacing the negator by a simple addition one can reconfigure the digital modulator to have the positive component.

About the implementation, by choosing the IF frequency equal to the sampling frequency divided by four, one can avoid using a true multiplier. The two mixing signals that form the real and imaginary parts of a complex Fs/4 oscillator used for frequency up-conversion (to obtain a quadrature version of a real bandpass signal originally centred at 0) are thus simplified. The real (in-phase) mixing sequence is $\cos(2\pi f_1 t)$ = 1,0,–1,0, etc. That mixing sequence's quadrature is $\sin(2\pi f_1 t)$ = 0, 1,0,-1, etc. The implementation here does not require any true multipliers or true adders, the sequence is chosen and combined with the help of multiplexers.

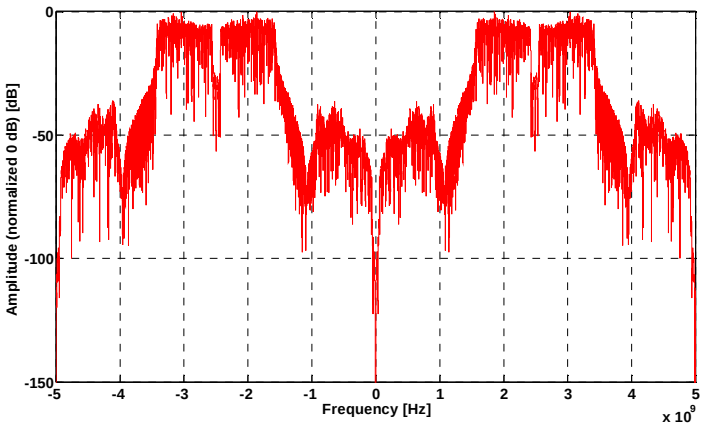


Figure 2-10: Frequency translation of the baseband signal around Fs/4

As the modulator can be programmed to use the lower or upper band the VCO frequency plan can be simplified. The VCO must generate 4 frequencies but in a narrower band. The LO generation needs to generate the following frequencies: 60.14 GHz and 62.3 GHz to target channel 3 and channel 4 with the upper band, and frequencies 60.82 GHz and 62.68 GHz to target the channel 1 and channel 2 with the lower band. This represents a slight improvement in terms of the VCO implementation.

Channel number	Channel center frequency (homodyne)	Channel center frequency (heterodyne)
1	58.320 GHz	60.820 GHz
2	60.480 GHz	62.680 GHz
3	62.640 GHz	60.140 GHz
4	64.800 GHz	62.300 GHz

Table 2-3: Channel center frequencies for IEEE TG3C.15.3C in the case of the homodyne and heterodyne structures

A global simulation has been realized as an example with f_{C2} 57.5 GHz. The channel is thus translated around 60 GHz. The result is depicted in Figure 2-11.

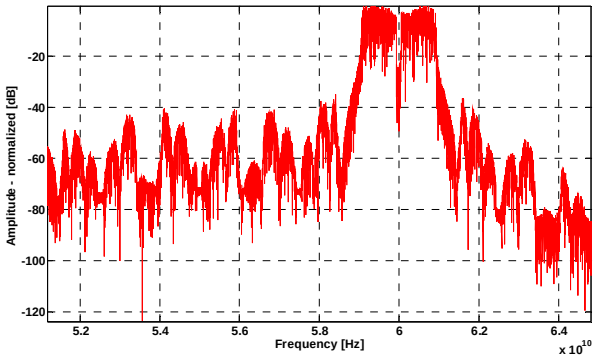


Figure 2-11: Frequency translation around Fs/4 + f_{C2}

b. Conclusion on digital frequency translation

Considering the sampling frequency used in this work (10 GHz) one can realize a translation around 2.5 GHz (Fs/4). With the state-of-the-art technology is hard to think about a digital translation to a higher frequency but with a more advanced technology, it might become possible.

2.2.2.2. Intermediate frequency to RF converter

As data were previously translated to an IF frequency, a different architecture of analog frequency translation can be presented: the IRFC (intermediate to RF frequency converter). In the architecture presented in Figure 2-12 the supplies of the DAC and the Mixer are now independent thanks to an integrated transformer. More headroom is therefore available for each block easing the design.

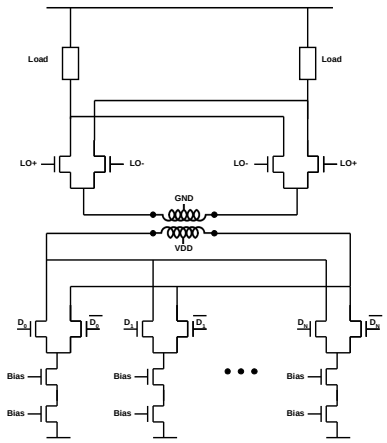


Figure 2-12: Intermediate to RF converter

Nevertheless a drawback appears because of the use of the transformer. Considering the bandwidth and the possible IF frequency (2.5 GHz), the transformer needs to be very wide band (low Q) and thus will add attenuation on the last sub-carriers and thus degrade the EVM. However, if the digital frequency in more advanced processes could be increase, the IF frequency could be moved to 5 GHz, making this concept more attractive.

2.2.3. Conclusion

Two architectures with SDR capabilities for a 60 GHz wireless transmitter have been proposed. Both use an interpolator at high frequency (10 GS/s).

The Homodyne structure is more compact and the use of this architecture will lead to a better power consumption and less silicon area compare to the heterodyne structure. The DRFC will be very challenging because of the high requirements (7 bits linearity for the DAC at 10 GS/s and direct translation around 60 GHz).

The Heterodyne structure exploits a digital mixer. State of the art technology limits the IF to 2,56Hz. IRFC could be used to increase the performance of the DAC. Local oscillator generation can also be relaxed. However, the effective bandwidth of the DAC part of the DRFC must be higher.

	Homodyne	Heterodyne
Digital functions	++	+++
Power consumption	+	-
Silicon area	+	--
L0 Generation	-	++
DAC linearity	-	+

Table 2-4: Summary of performance of Homodyne and Heterodyne structure

A choice must be made considering the performances of the architectures. Because of simplicity, the homodyne structure is chosen for this work.

2.3. MODEL OF THE DIGITAL TRANSMITTER

In this section a model of the digital part of the proposed transmitter, is presented. First a signal based on the IEEE TG3C.15.3C specification is constructed. The signal will be used as a test vector. Then based on the signal and the standard specification, the constraints on the interpolator are specified. Considering the frequency plan, it has been shown that the interpolator must work at 10 GS/s. This high frequency is hard to achieve with a state-of-the art technology. Thus different optimizations are presented in order to achieve the simplest but efficient hardware design.

The architecture considered for the rest of this work is the homodyne architecture presented in section 2.2.1 and depicted in Figure 2-13.

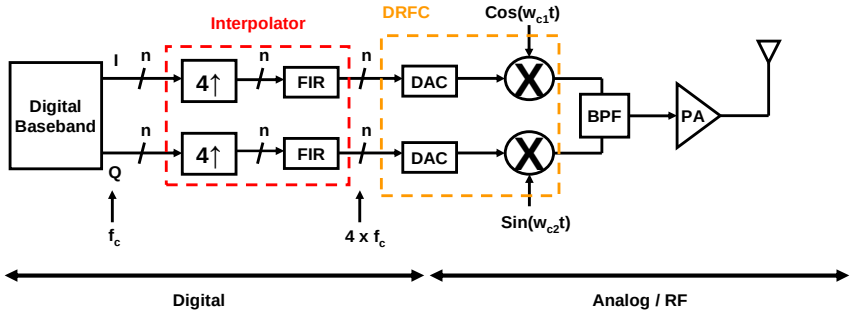


Figure 2-13: Proposed transmitter chain

This architecture introduced SDR concepts. This work focuses on the interpolator design. Specifically in this chapter the system study is presented. Matlab is used to realize the digital model.

2.3.1. Baseband processing

Here the baseband is based on the IEEE TG3C.15.3C standard. This study of the signal is important before any simulations. In this work the signal used is an OFDM signal. The signal is constructed with a simplified OFDM modulator depicted in Figure 2-14.

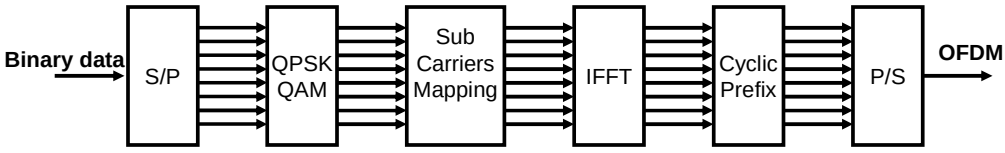


Figure 2-14: OFDM modulator simulated

Binary data are mapped into frequency domain QPSK symbols. These symbols are used as the inputs to an IFFT block that brings the signal into the time-domain. The IFFT takes in N symbols at a time where N is the number of subcarriers in the system. The IFFT block provides a simple way to modulate data onto N orthogonal subcarriers. The block of N output samples from the IFFT make up a single OFDM symbol. The length of the OFDM symbol is NT where T is the IFFT input symbol period. Each symbol is cyclically extended, thus the cyclic prefix is added at the beginning of the symbol. A typical value of 64 samples is used for the cyclic prefix.

The first step is to generate binary data and to map them on a QPSK modulator. The binary generation is done pseudo-randomly on 2 bits. Then sub-carriers are mapped following the standard's specifications, recalled in Table 2-5

Subcarriers type	Number of subcarriers	Logical subcarriers indexes
Null subcarriers	141	$[-256:-186] \cup [186:255]$
DC subcarriers	3	$-1, 0, 1$
Pilot subcarriers	16	$[-166:22:-12] \cup [12:22:166]$
Guard subcarriers	16	$[-185:-178] \cup [178:185]$
Data subcarriers	336	All others

Table 2-5: Sub-carriers allocation

Null sub-carriers, pilot sub-carriers and guard sub-carriers are set to 0. The IFFT is performed and the cyclic prefix is added. The result is presented in Figure 2-15. Finally the signal is serialized and the output frequency is defined at 2.5 GS/s. This basic OFDM signal will be used as a simulation base signal for the proposed transmitter.

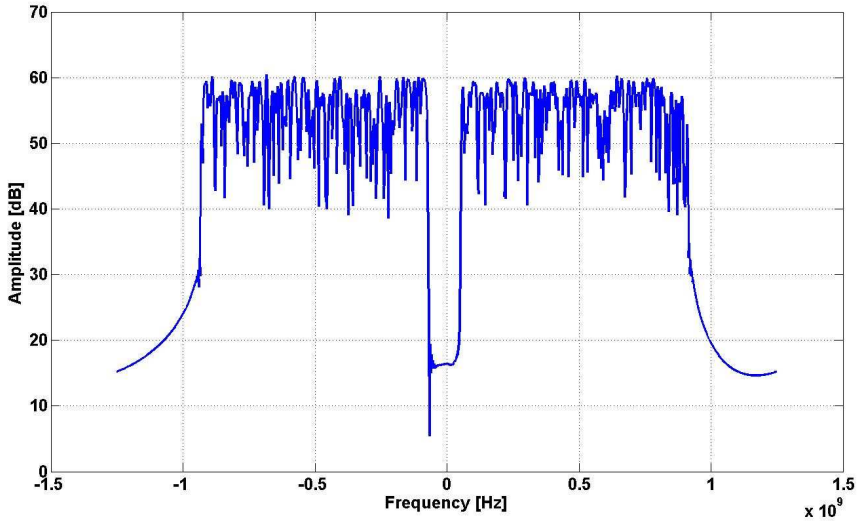


Figure 2-15: OFDM Signal simulated

2.3.2. Interpolator

As previously explained, the interpolator is composed of an up-sampler and a FIR filter, Figure 2-16. Simulations are performed to prove the feasibility of this block for the considered standard.

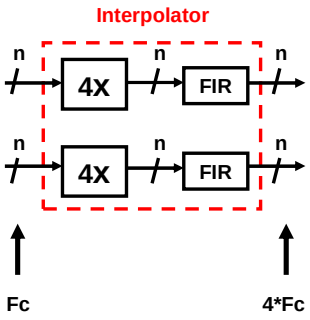


Figure 2-16: Interpolator (up-sampler + FIR filter)

The interpolator samples the input data at F_c = 2.5 GS/s and the output data are sampled at 10 GS/s. The FIR function is then realized at 10 GS/s. Images pollute the spectrum at every multiple of 2.5 GS/s. The first image is centred on 2.5 GHz and the second one is centred at 5 GHz shown in Figure 2-17 up-to $F_c/2$ = 5 GHz.

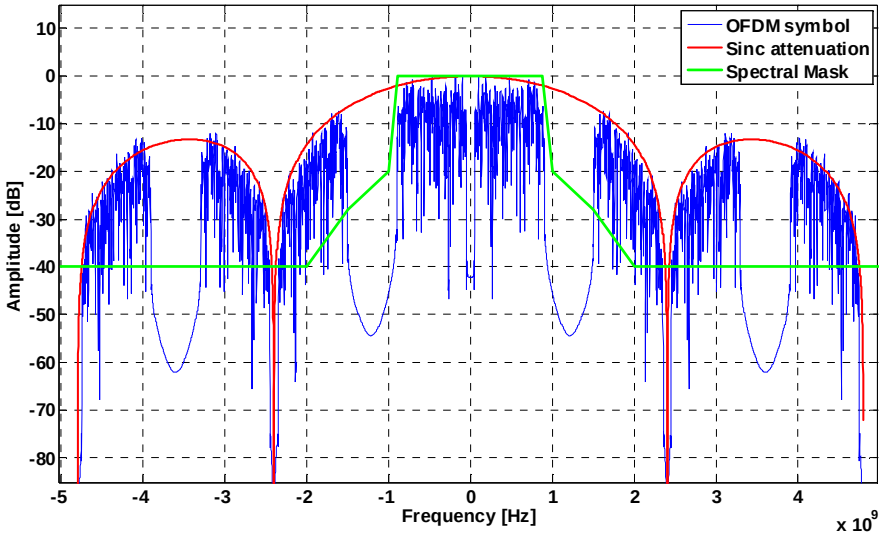


Figure 2-17: Signal sampled at 10 GS/s and images attenuated by a sinc function

The transmit spectrum mask is the power contained in a specified frequency bandwidth relative to the total carrier power. The interpolator frequency specifications appear naturally. An attenuation of 30 dB must be provided by the interpolator for the frequency range [1,5 GHz – 5 GHz].

2.3.2.1. Interpolator simulation

The order of the filter can be easily found with a signal processing CAD tool like Matlab. A first simulation has been performed and FIR filter of order 22 is sufficient to respect the spectrum mask.

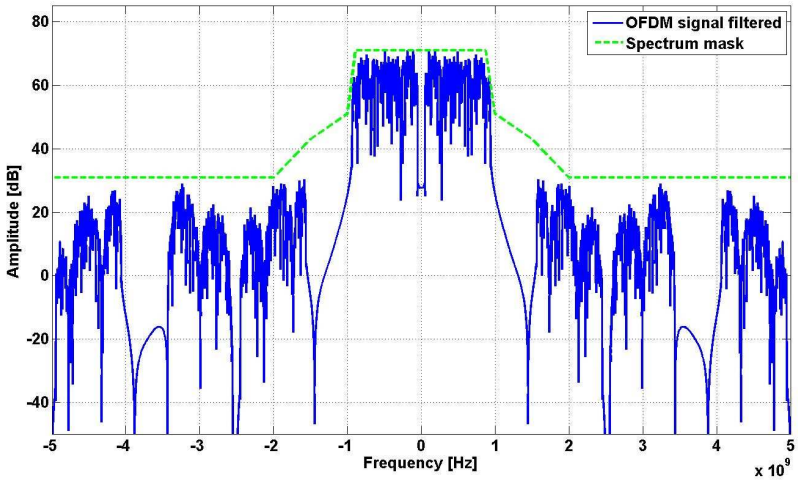


Figure 2-18: OFDM symbol filtered by an interpolator with 22 coefficients

Frequency specifications are presented in Figure 2-19:

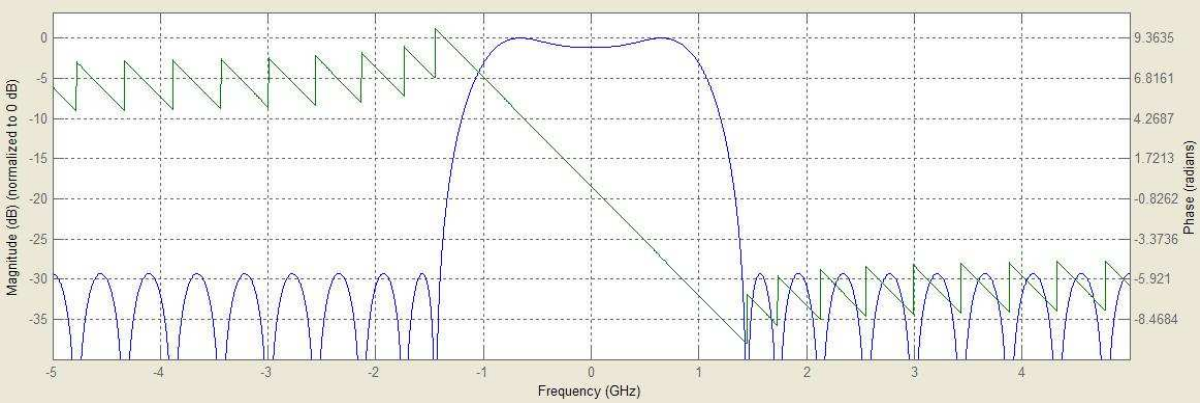


Figure 2-19: Frequency and Phase response of the 10 GHz Interpolator (22 coeff.)

A few comments can be made regarding this first simulation. The first one is obvious, the interpolator works at 10 GHz. Even with a state of the art technology, digital functions at 10 GHz are not simple to design and a 22 coefficients FIR filter is a complex function to design. Recall that an FIR needs MAC operations, means that multipliers at 10 GHz must be implemented which seems not practical in terms of design, area and power consumption.

The second one is about the frequency specifications of the interpolator. Here one can see that the phase is linear in the passband, which is a property of symmetric FIR filters. No control is done on the ripple in the passband. It is possible to reduce this ripple by increasing the number of coefficients at the cost of extra complexity and power consumption. This parameter must be well studied because ripple introduces distortion and increases the EVM.

Finally data are represented as real values and must be quantized on 7 bits (2's complement).

2.3.2.2. Comments on interpolators

The first question that arises to the reader is how can we achieve such high working frequency for a complex arithmetic function such an interpolator? Before going into the detail of the proposed solution in this thesis, it is interesting to have a look on the general solutions proposed at the state-of-the-art.

a. High speed 1bit-FIR filters

High speed FIR filters are used in high speed source-series-terminated (SST) transmitters. A SST driver is composed of a programmable FIR filter and a driver that realize a digital-to-analog conversion. The FIR filter has the role of an equalizer in this kind of transmitter. [Kossel08] proposes a SST driver in a 65nm technology able to provide a data rate of 8.5 Gb/s. The 4b input at quarter rate are multiplexed into two half rate streams. The half rate streams are retimed to the half rate clock. Then the FIR is implemented. The delayed tap has been realized with a data register and the polarity of the coefficients (+1, 0, -1).with the help of simple gates. Then these two streams are finally serialized to a single stream and retimed again before going into the driver slices. The architecture is depicted in Figure 2-20:

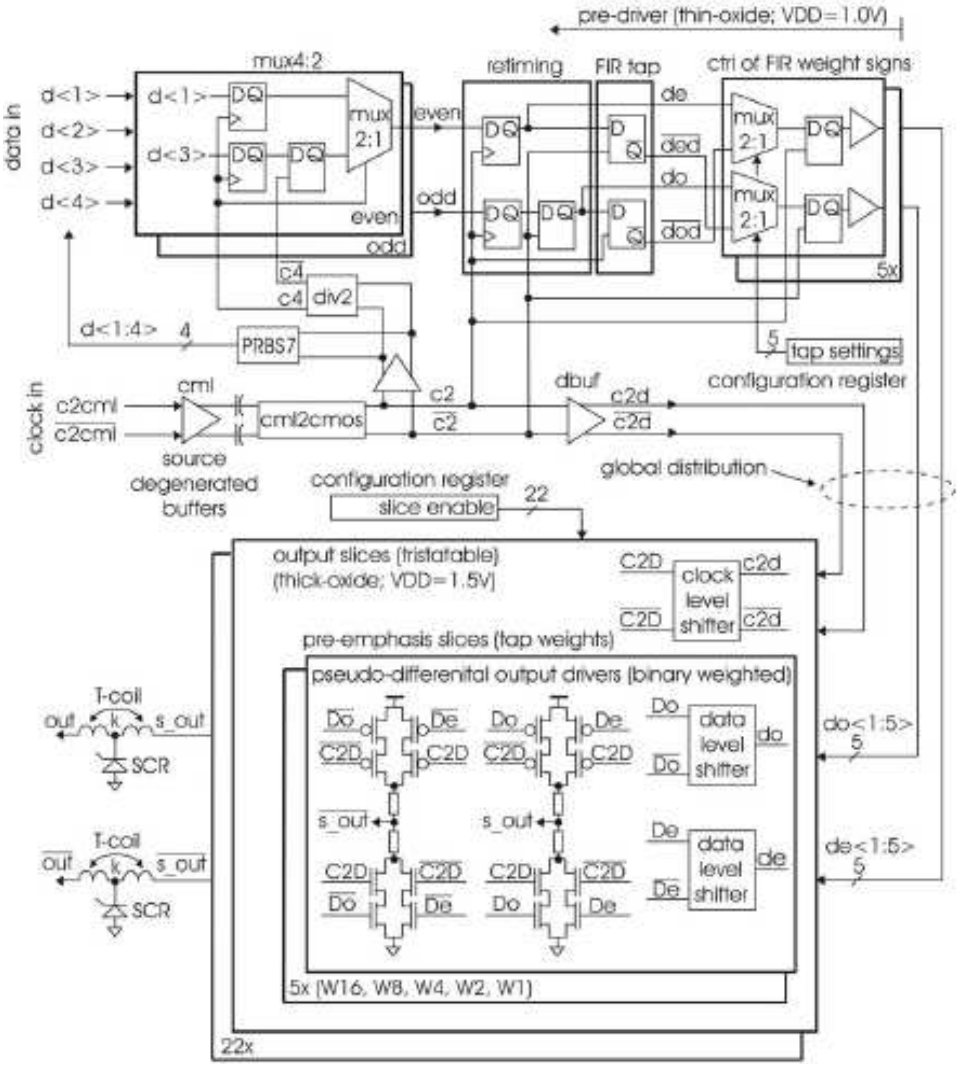


Figure 2-20: SST driver with FIR equalization filter

This kind of FIR filter can be summarized following the Figure 2-21.

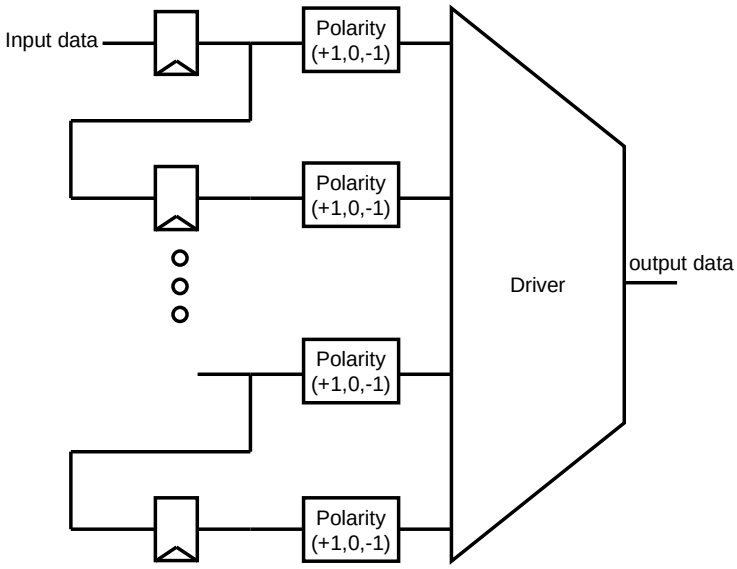


Figure 2-21: FIR filter implemented in SST driver

This kind of architectures [Menolfi05], [Menofli07], [Menolfi11] are really well suite for high speed I/O communications because they provide a very high output swing. The advantage of this architecture is that the transfer function of the FIR is highly programmable thanks to a feedback to the digital base band processor and that it can be easily couple to a DAC like driver.

b. Poly-phase filter

The interpolator is no more than a linear time invariant system. Parallel computing can be easily applied to these systems and is referred in the literature as poly-phase filter. It has been shown that the transfer function is a sum of delayed data multiplied by specific coefficients. In a poly-phase structure, the sum is decomposed in different sub-filters at a lower rate and then the output is recomposed with the help of a multiplexer. Let us take an example of a 12 tap FIR filter with an interpolation factor of 4. The coefficients are given by a_0 to a_{11}. In the straightforward way to realize an interpolator, the data are up-sampled by a factor of 4 and then the FIR filter is realized at 4 times the sampling rate (Figure 2-22). One can understand that depending of the frequencies involved realizing a interpolator can become really complex.

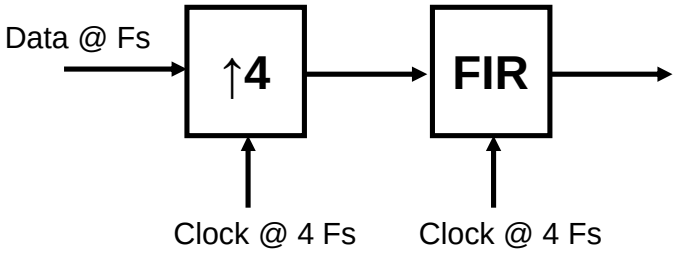


Figure 2-22: Straightforward interpolator realization

In the poly-phase approach, it is slightly different. If one interpolates by a factor L, you calculate L outputs for each input by using L different sub-filters that are derived from the original filter (Figure 2-23).

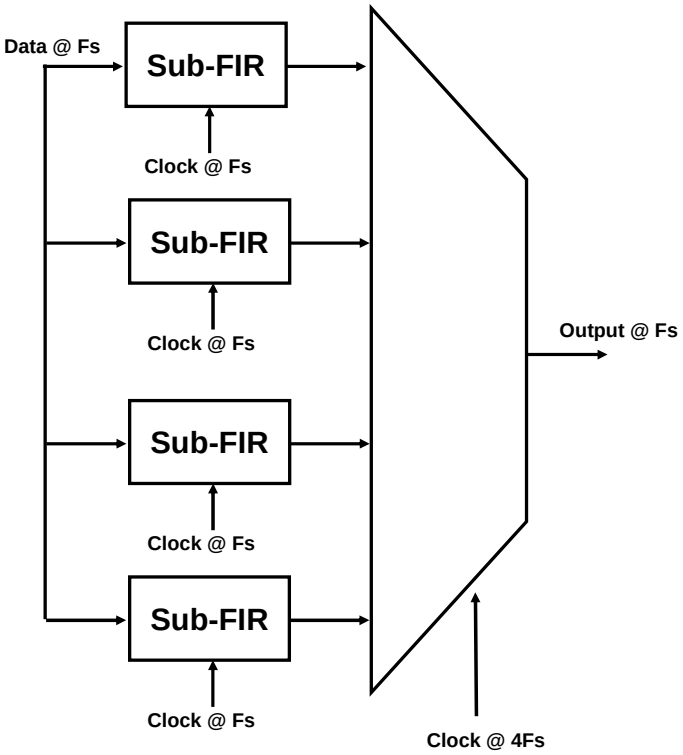


Figure 2-23: Polyphase interpolator realization

In order to show to the reader that the results are the same in the case of the straightforward and the poly-phase structure, let us compute the result of the poly-phase filter in the case of 12 coefficients and an interpolation factor of 4 (Table 2-6). By scrambling the data in a specific order, the result is that you are able to rearrange the output in the right order.

a0	**a1**	**a2**	**a3**	**a4**	**a5**	**a6**	**a7**	**a8**	**a9**	**a10**	**a11**	Result
x2	0	0	0	x1	0	0	0	x0	0	0	0	x2*a0+x1*a4+x0*a8
0	x2	0	0	0	x1	0	0	0	x0	0	0	x2*a1+x1*a5+x0*a9
0	0	x2	0	0	0	x1	0	0	0	x0	0	x2*a2+x1*a6+x0*a10
0	0	0	x2	0	0	0	x1	0	0	0	x0	x2*a3+x1*a7+x0*a11

Table 2-6 : Poly-phase computation of a 12 tap FIR with an interpolating factor of 4.

For sure here in this solution the design of the FIR has been simplified to 4 FIR of 3 coefficients per filter but stringent requirements have been put on the serializer. For further reading on poly-phase filters, the reader is invited to read [ProakisDSP].

The idea of working in parallel can be pushed further. [VanRoermund] proposes what it is called a flexible DAC. Recall that after the interpolator a digital-to-analog conversion must be performed. It is possible to push the parallel computing to the DAC. The multiplexer is then realized in the analog domain. In this case the requirements are pushed on the way that the different DAC will be summed meaning the clock of the mux and the mismatch between each path. Error on the clock (timing and duty cycle) and on the different path to recombine the output of each DAC, will lead to phase and amplitude distortion and thus will affect the ENOB. For further reading, please refer to [VanRoermund11] chapter 14: Flexible Digital-to-Analog conververt.

c. Conclusion

The SST driver has been proposed to realize a simple FIR structure. The advantage of the STT driver is that it can be couple easily with a DAC like driver. Also the transfer function of the FIR filter is highly programmable. The drawback of this architecture is the use of serializers. In the architecture proposed in this thesis, the sampling rate must be at 10GS/s.

The FIR design can be also simplified with the help of a poly-phase structure. But in this design high requirements are also put on the output serializer. The problem of the

serializer can be pushed to the DAC recombination. Even if the requirements on the serializer are pushed to the DAC, the analog multiplexer is not simple and each imperfection of timing and amplitude will degrade the overall ENOB. Another solution has been studied in this thesis and is presented in the next sections.

2.4. INTERPOLATOR MODEL

At this point the most important improvement would be to reduce the complexity of the interpolator while reducing the number of coefficients, while still having a good EVM. These two parameters are not compatible; if one reduces the number of coefficients considering a frequency specification, the ripple magnitude increases. This improvement is however necessary to reduce the design complexity.

The improvement is to split the interpolator in two different interpolators. Instead of one interpolator at 10 GHz, a separation is done with one interpolator at 5 GHz and one at 10 GHz. This first improvement leads to a reduction of the design complexity. The idea behind is that the first interpolator will attenuate partially or completely the first image [1.5 GHz – 2.5 GHz] up-to Nyquist frequency and the second interpolator will attenuate completely the first and the second image [2.5 GHz – 5 GHz] up-to Nyquist frequency, depicted in Figure 2-24.

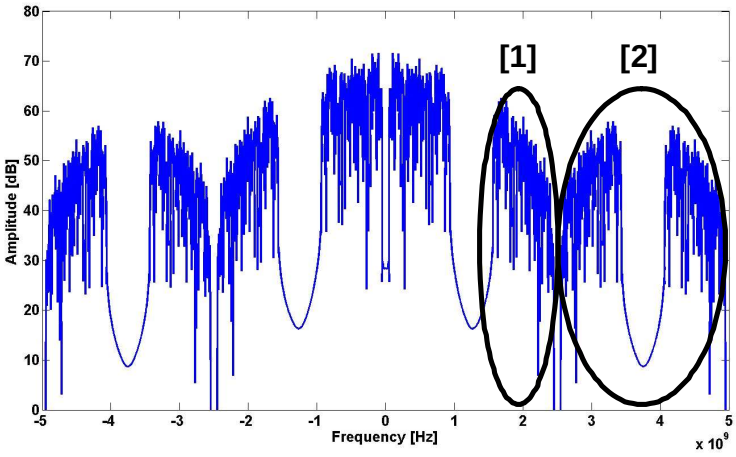


Figure 2-24: Differentiation of images to be attenuated

Figure 2-25 depicts the improvement strategy. As the last function works at 10 GHz remaining images still appear the multiples of 10 GHz.

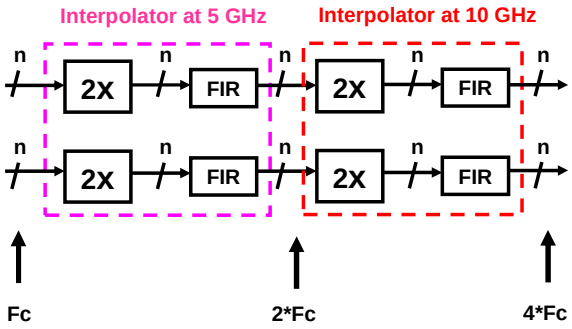
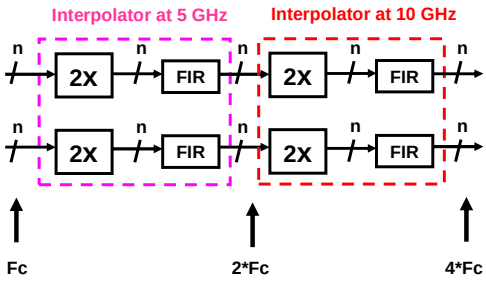


Figure 2-25: Interpolator improvement

Now a set of coefficients must be found for the first and second interpolator, while trying to reduce complexity. Parametric simulations can be done to find the number of coefficients but a dichotomous approach has been preferred. Starting from N coefficients, N/2 coefficients will be used in each interpolator.

Results are presented in Figure 2-26 and Figure 2-27. Notice that the first image [1] is not totally filtered after the first interpolator at 5 GS/s. This is not a problem as the second interpolator which works at 10 GS/s attenuates also the first image [1].



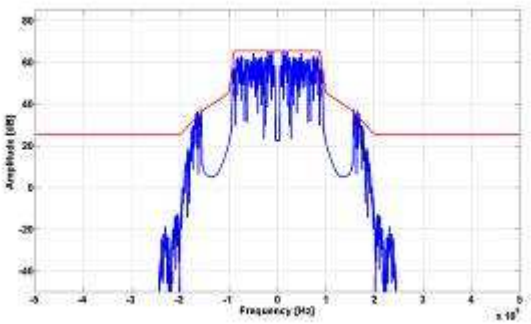


Figure 2-26: OFDM signal filtered after Interpolator at 5 GHz with 11 coeff.

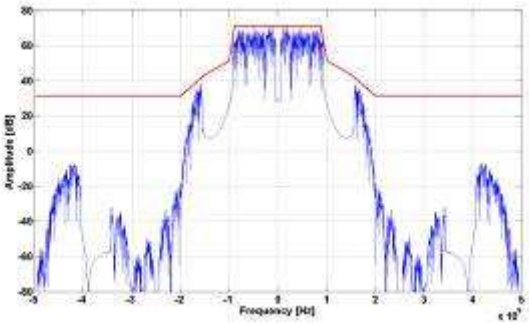


Figure 2-27: OFDM signal filtered after Interpolator at 10 GHz with 11 coeff.

An improvement has been reached, now an interpolator has to be designed at 10 GHz with half the coefficients. Same comments on the ripple can be done; in this synthesis no control on the pass-band ripple has been introduced.

At this point the dichotomous approach can be extended by following the scheme depicted in Figure 2-28. The next improvement (2d improvement) would be to divide the first interpolator at 5 GHz with 11 coefficients into two interpolators at 5 GHz with 5 or 6 coefficients and to divide the second interpolator at 10 GHz with 11 coefficients into two interpolators at 10 GHz with 5 or 6 coefficients.

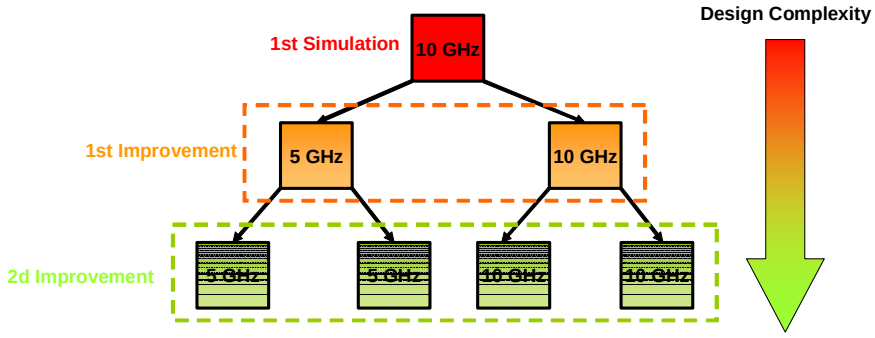
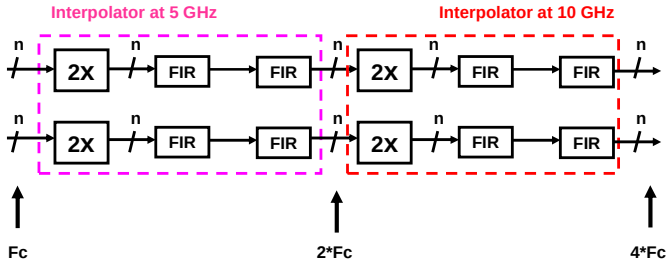


Figure 2-28: Improvements of the interpolator

Simulation results of the second improvement are depicted in Figure 2-29 and Figure 2-30.



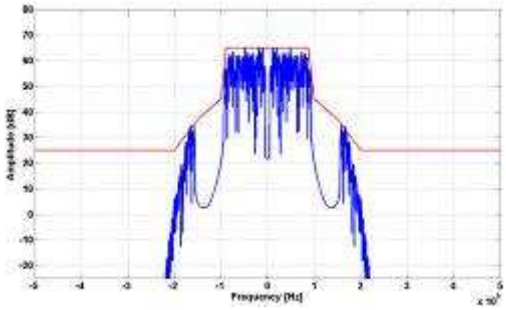


Figure 2-29 : OFDM signal filtered after Interpolator at 5 GHz with 2 FIR with 6 coeff.

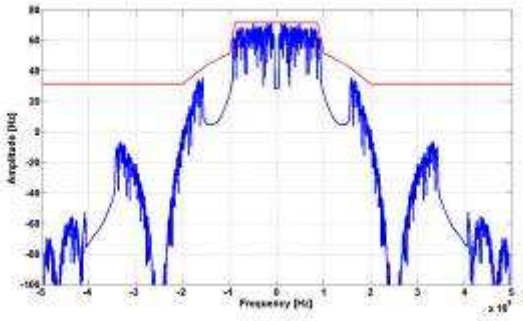


Figure 2-30 : OFDM signal filtered after Interpolator at 10 GHz with 2 FIR at 6 coeff.

With a low complexity arrangement of FIR filters (6 coefficients per filter) it is still possible to attenuate images of the OFDM signal. In the 5 GHz part, the same filter has been cascaded, as same as in the 10 GHz part. By cascading filters, the limit of the pass-band is attenuated, in this simulation the last sub-carrier is attenuated by 1.4 dB, see Figure 2-31.

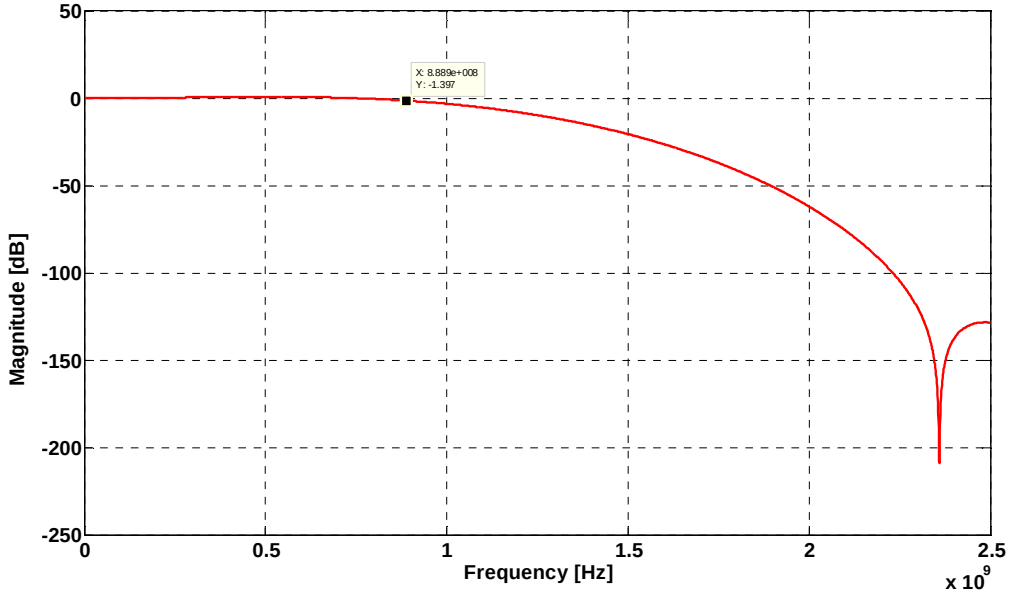


Figure 2-31: Global filter frequency response

This is the last improvement. The dichotomous approach cannot be pushed further. Now the problem of design complexity is solved another problem must be solved: the quantization of coefficients. Coefficients have been found but are still represented as real values, meaning that the FIRs need multipliers at 5 GHz and 10 GHz. An interesting solution to avoid standard multipliers is to represent coefficients in powers of two; the multiplication is thus transform into a shift operation.

Representing coefficients in powers of two means also changing the frequency specification of the filter. Special care must be taken and simulations, based on the previous study, must be done again. The architecture will be kept – 2 FIR at 5 GHz with 6 coefficients and 2 FIR at 10 GHz with 6 coefficients.

2.4.1. Interpolator with powers of two coefficients

A first approach is to quantize coefficients into the closest powers of two. Simulations have been realized and the transfer function has changed for the 5 GHz and 10 GHz filters. The transfer function has changed because the location of the zeros in the Z plane is modified. The result is high ripple in the band (> 4dB) shown in Figure 2-32 and insufficient attenuation outside the band, shown in Figure 2-33.

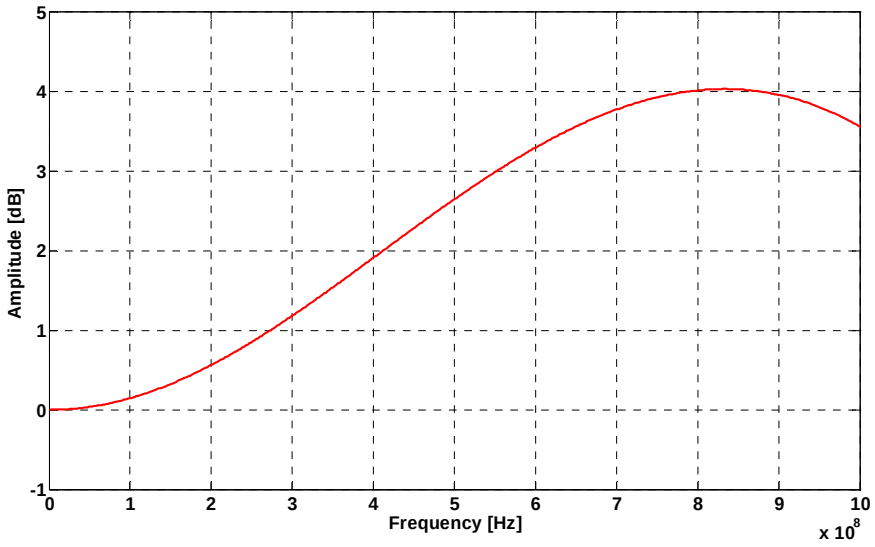


Figure 2-32: Ripple in pass-band due to direct quantization with powers of two coefficients

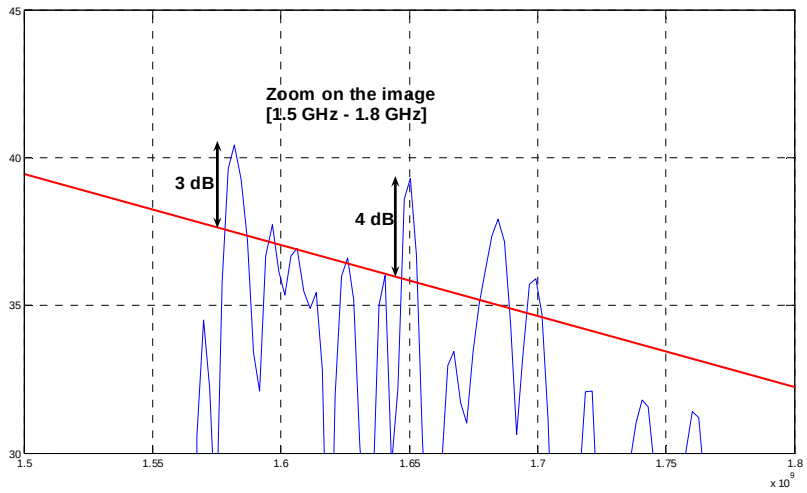


Figure 2-33: Insufficient stop-band attenuation due to direct quantization with powers of two coefficients

Till now ripple in the band and pass-band attenuation has not been taken in account. With real coefficients small ripple and small attenuation at the limit of the band has been noticed but in the case of quantized coefficients the ripple tends to increase. Indeed by quantizing coefficients, the zeros in the unity circle move and thus change the frequency response.

A solution is to approximate the real coefficients by a sum of powers of two coefficients. Thus each real coefficient is represented by a sum of powers of two (also called canonical signed digit - CSD) till the transfer function responds to the specifications. In this work this solution is not possible as the key point is to simplify the complexity of the digital circuit as much as possible.

The solution proposed in this work is to find a set of coefficients in the complete search space that is compliant with a number of user defined specifications. The advantage of this solution is that sum of powers of two do not have to be computed (like CSD) but appear naturally because of the convolution of the different cascaded FIR filters.

2.5. SEARCH ALGORITHMS

The goal of search algorithms is to find a specific solution in a complete search space. Parameters must be defined in order to differentiate a good filter from a bad filter. Considering a frequency specification for a filter and considering that filters will be cascaded, it would be interesting to find a set of filters with a small ripple in the band and large attenuation outside the band. Different strategies exist that enhance the performance of the search procedure over a fully random walk in the parameter space but first data encoding and fitness evaluation must be defined.

a. Data encoding

A FIR filter within N_C coefficients has the following form:

$$F(z) = \sum_{k=0}^{Nc-1} a_k z^{-k} = a_0 + a_1 z^{-1} + \ldots + a_{Nc-1} z^{-Nc-1} \qquad \textbf{Eq 2-9}$$

Taking advantage of the symmetry of the coefficients ($\forall k, a_k = a_{Nc-k-1}$), only half of the coefficients must be tuned; more precisely there are $Nmc = E\left[\frac{Nc+1}{2}\right]$ meaningful coefficients: $\{a_k, k \in \{0,...,Nmc\}\}$.

Each of those should now be chosen in a limited set of powers of two (further referred to as the "dynamic") defined as:

$$D = \{0\} \cup \{\pm 2^{-p}, p \in \{0,...,d-1\}\} \qquad \textbf{Eq 2-10}$$

The total is then $(\#D)^{Nmc}=(2d+1)^{Nmc}$ which represents the size of the space to be browsed. Finally, note that two proportional N_c-tuple of coefficients yield almost exactly the same filter and should not be represented twice; therefore, the largest is forced at +1 (the highest value in D) thus reducing search space size to $Nmc(2d+1)^{Nmc-1}$. Table 2-7 shows examples of typical values of the couple (Nmc,d) and the associated space size.

N_c \ D	7	10	13
7	13e3	37e3	79e3
12	4.6e6	25e6	86e6
19	380e9	7.9e12	76e12

Table 2-7 : Typical values of (N_C,d) with corresponding search space sizes.

b. Fitness evaluation

Among all possible solutions, one has to discriminate filters, therefore, two criteria are introduced (see figure):

1. F_1 represents the ripple inside the band, computed as the standard deviation of the dB gain in the range of frequencies [0, f_c] Hz (f_c cut off frequency).
2. F_2 measures the stopband attenuation, calculated as a sum of penalties over frequencies (greater than f_c) where the gain is greater than the targeted stop band attenuation.

Note that this definition of F_1 is independent of the actual value of the static gain.

Flat filters that are discriminated with low values of F_1 might appear of higher interest since cascades of duplicated identical filters tend to deteriorate the ripple in passband while improving attenuation elsewhere. However, since these two parameters have distinct impacts on the performances of the filter it would have been difficult to balance the one against the other. Therefore the fitness evaluation is under the form of a vector (F_1,F_2) and introduced multicriterion optimization in our research. This approach is conceptually harder to deal with, but has in practice limited impact on the complexity of the algorithms and is far more informative. [Carlos98] and [Cohon85].

c. Multicriterion optimization

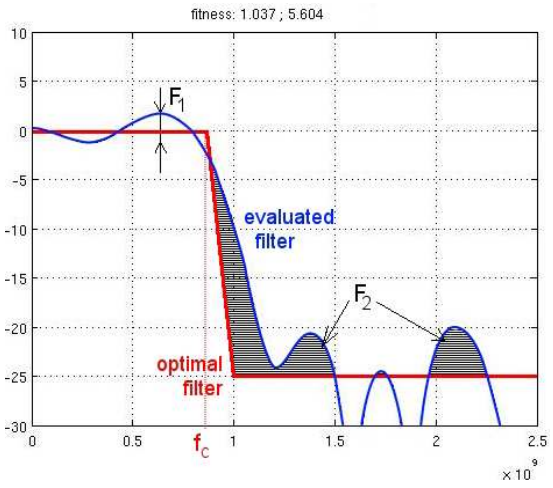
According to optimization field theory, a scalar "fitness function" is needed. When dealing with multicriteria optimization, this fitness function is a vector and sorting procedures against one dimension generally do not respect the other dimensions order. From a theoretical point of view, it is stated that the mathematical binary relation $\trianglelefteq$ specified below defines a "partial" order in the (F_1,F_2)-plane.

$$(F_1,F_2)\trianglelefteq(F_1',F_2') \Leftrightarrow \begin{cases} F_1 <= F_1' \\ F_2 <= F_2' \end{cases} \qquad \textbf{Eq 2-11}$$

Here are basic definitions:

It is stated that a solution (F_1,F_2) "dominates" solution (F_1',F_2'), and we write

$$(F_1,F_2) \triangleleft (F_1',F_2') \text{ if } \begin{cases} \forall i, F_i \leq F_i' \\ \exists i, F_i < F_i' \end{cases} \qquad \textbf{Eq 2-12}$$



2-34: Two fitness criteria of one possible filter

A solution (F_1,F_2) belonging to a set of feasible S is said to be "non-dominated with respect to S" if none of the solution in S dominates (F_1,F_2).

Finally, let S be a set of feasible solutions, the "Pareto front of S" is simply the subset of all non-dominated solutions in S. Figure 2-35 shows examples of domination/non-domination relations along with the pareto front of the given set of solution.

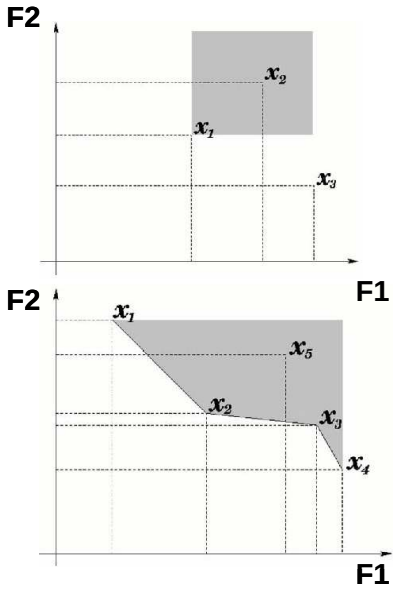


Figure 2-35: Domination/non-domination relations and Pareto front of set of solution in the (F_1,F_2)-plane

As seen before, the size of the set of feasible solutions increases exponentially with the number of coefficients and the allowed dynamic. Therefore, exhaustive enumeration of each solution – which nevertheless ensures the optimal filter to be found in a finite

time – quickly becomes out of the question. Many approaches have been developed to avoid such tedious work which often rely on a reordered enumeration of the solution set, which try to answer the question: “how to find a good strategy to partially explore the solution set on hand of already tested ones?” The answer mostly holds in a balance between a coarse exploration of the solutions set (“diversification”) and the fine optimization of the already encountered solutions (“intensifications”).

These techniques gather deterministic and stochastic optimization paradigms (the latter are known as “heuristic”) and benefit from a large experience of the computer science community but loose at least one of the two already mentioned main properties:

1. Optimality: (in the general case) the best found solution might not be the optimal one

2. Finite time algorithm: most heuristics only ensure an asymptotic convergence

The different approaches might be classified according to several criteria out of which a limited list is presented below. Some classical algorithms and ideas are then sorted:

- Continuous or discrete search space
- Deterministic or stochastic approach
- Diversifying or intensifying strategy
- Anytime algorithm or fixed amount of computation
- Need of an initial solution guess or not
- Whether or not the algorithm implements a selection mechanism
- Whether it deals with a single solution or a set of solutions
- Parallelizable or sequential strategy

A type of algorithm which is able to adder these points is the Genetic Algorithm. Besides the different advantages of genetic algorithms (GAs), their easy and pragmatic implementation and the a posteriori possibility to revise the above mentioned balance made them, in our opinion, the most suited tool for challenging this highly non-linear

problem. Moreover, the fact that a population of solutions is available at any time provides the user with a set of solutions which is somehow less frustrating than one "best-so-far" solution. Finally their ability to integrate other hybridizing heuristics (i.e. future work) legitimates their use in this particular task.

The main known drawbacks of Gas are their computational cost and, as they heavily rely on randomness, their lack of reproducibility.

d. Detailed description

Details of the main steps of the algorithm and the different peculiarities of the proposed implementation are described.

Genetic algorithms are population-based heuristics that simulate a Darwinian evolution process throughout several generations in order to achieve convergence of an initial random population of solutions towards an optimum of the response function hyper surface. The number of generations (Ngen) and the population size (Npop) are important parameters with regards to the GA success to find good solutions and to the available computational time. The following default values are assigned but these parameters are let as tunable parameter: Ngen = 500 and Npop = 100.

At each generation the given population evolves according to biologically inspired operators:

- Crossovers which allow recombining two individuals into two off-springs that share part of their parent's genome. This operator is believed to intensify the search by deriving profit of already encountered solutions. In technical words, this is done by one point crossovers with breaks occurring randomly. Crossovers happen between a random "pool" (on average 25% of the population) of fittest solutions but, among the "pool", individuals are randomly paired (this crossbreed strategy avoids premature convergences of the population).

- Some random modifications of the newborn's genome are then applied to simulate mutations that occur during recombination. The mutation frequency parameter is set of 5%.

- Finally completely random individuals immigrate to keep at hand a constant breeding-ground (and a constant population size).

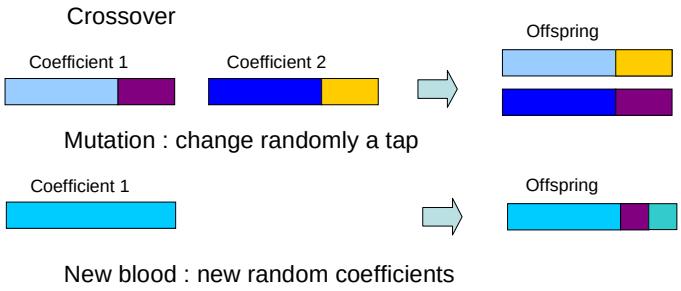


Figure 2-36: Evolution applied to filter's coefficients

The two last steps ensure the asymptotic convergence of GA towards an optimal solution. Only new individuals are then evaluated and the population is sorted according to the "distance to current Pareto front" criterion. Elitist selection is applied afterwards by freeing less fit inhabitants: only Pareto solutions are kept with a maximum keep ration of 50% of the entire population.

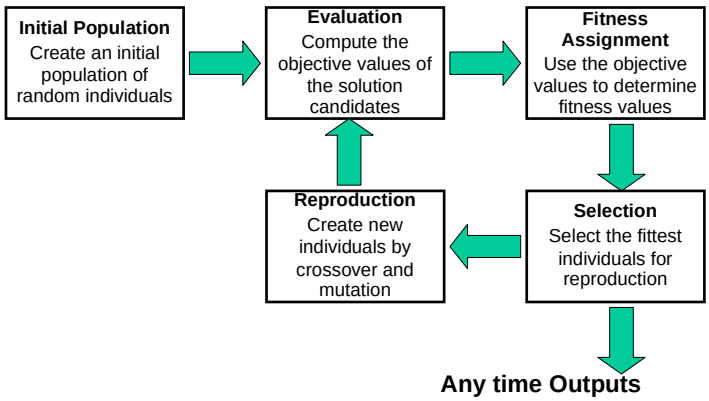


Figure 2-37 : Schematic representation of the GAFIR synthesis with GA algorithm (general case)

In order to test the algorithm, FIR filters with a large number of coefficients – as presented in the first simulation, have been generated by the GA. Table 2-8 presents the synthesis parameters:

Initial population	100
Generation	1000
Number of coefficients	22
Fs (sampling frequency)	10 GHz
CPU time on a laptop	~ 3 hours

Table 2-8: 22 coefficients FIR synthesis

Figure 2-38 shows the "Pareto front" with different solutions – good F_1 (low passband ripple), good F_2 (high stopband attenuation) and average F_1,F_2. Clearly only F_1 [a] and only F_2 [c] solutions are not acceptable; one does not achieve sufficient stopband attenuation while the other one adds a large ripple in the band. But the average solutions [b] are not sufficient to assure the complete attenuation of images.

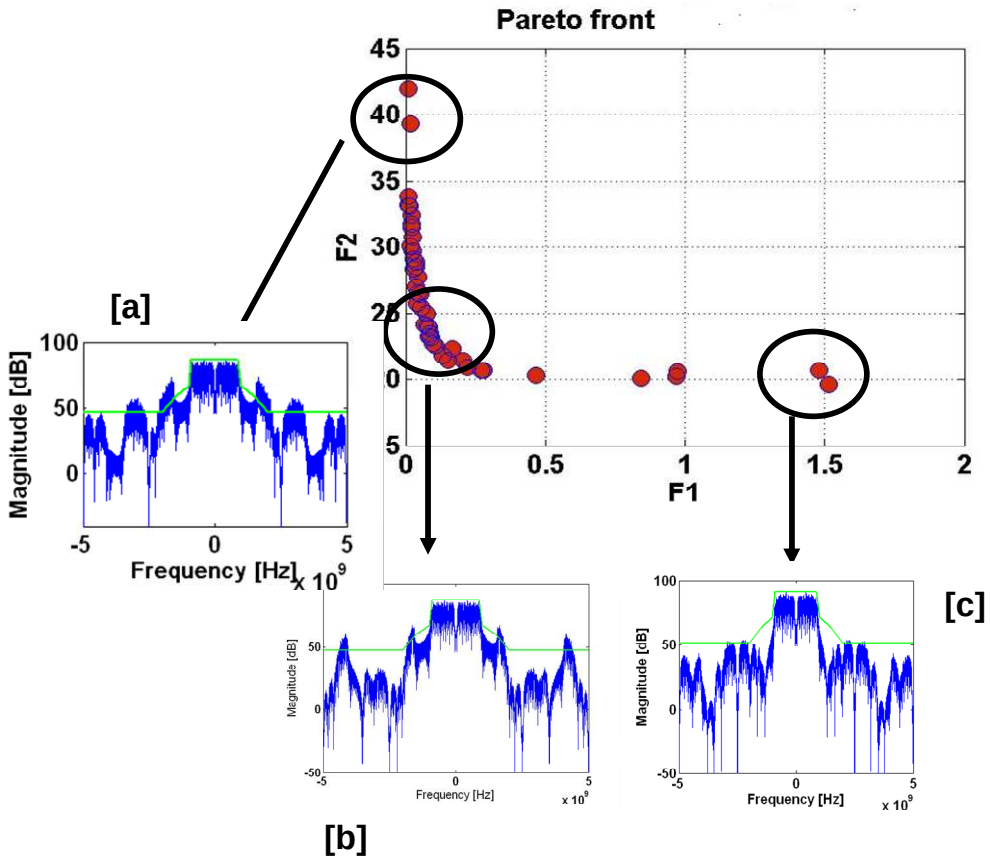


Figure 2-38: 22 coefficients synthesis result

This test was not concluding because 22 coefficients are no more sufficient to attenuate images without degrading the pass-band. Compared to 22 real coefficients (see first simulation) quantized filters have a loss of precision. One must take care of this loss and increase the number of quantized coefficients.

More over a synthesis has been performed to compare the brute force and a GA algorithm on 9 coefficients. This simulation has the goal to prove that the GA is able to find the best solution of the complete search space. Best solutions have been found by the GA and exhibit the Pareto front on Figure 2-39.

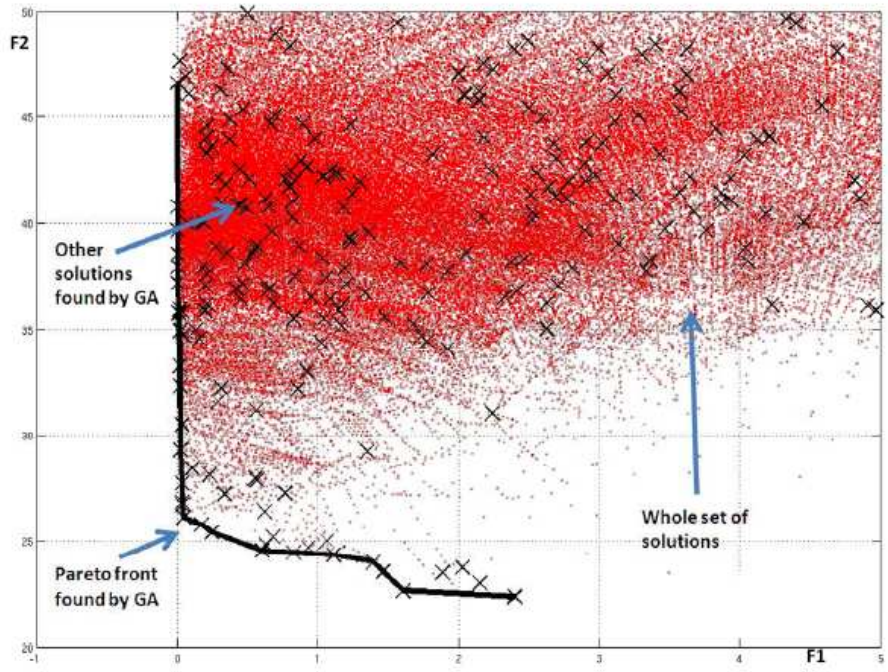


Figure 2-39: Comparison of GA solutions and brute force solutions for FIR with 9 coefficients

Now that it is sure that the GA finds the best set of coefficients in the full search space, a set of coefficients can be explored for this work.

2.6. INTERPOLATOR WITH POWERS OF TWO COEFFICIENTS REVISITED

The GA has been initially used to synthesize filters following the scheme defined in this work:

- 2 filters with 6 coefficients at 5 GHz
- 2 filters with 6 coefficients at 10 GHz

The generated filters respect the following constraints:

- The phase is linear => generation of symmetric coefficients
- Total ripple in the band is compliant with the EVM requirements => try to decrease the ripple in the band

- Images are sufficiently attenuated => be sure to have a margin between images and the spectral mask

- The design complexity has been reduced to its maximum => try to reduce the complexity of the filter at 10 GHz which is one important design challenge.

2.6.1. 5 GHz filter

For the 5 GHz filter, the dynamic has been set to 7, the number of coefficients to 6.

Initial population	100
Generations	1000
Dynamic	7 bits
Number of coefficients	6
Fs (sampling frequency)	5 GHz
CPU time on a laptop	~ 3 hours

Table 2-9: GA parameters for 5 GHz filters

The chosen solution is $[-2^{-4}\ 2^{-4}\ 2^{-1}\ 2^{-1}\ 2^{-4}\ -2^{-4}]$

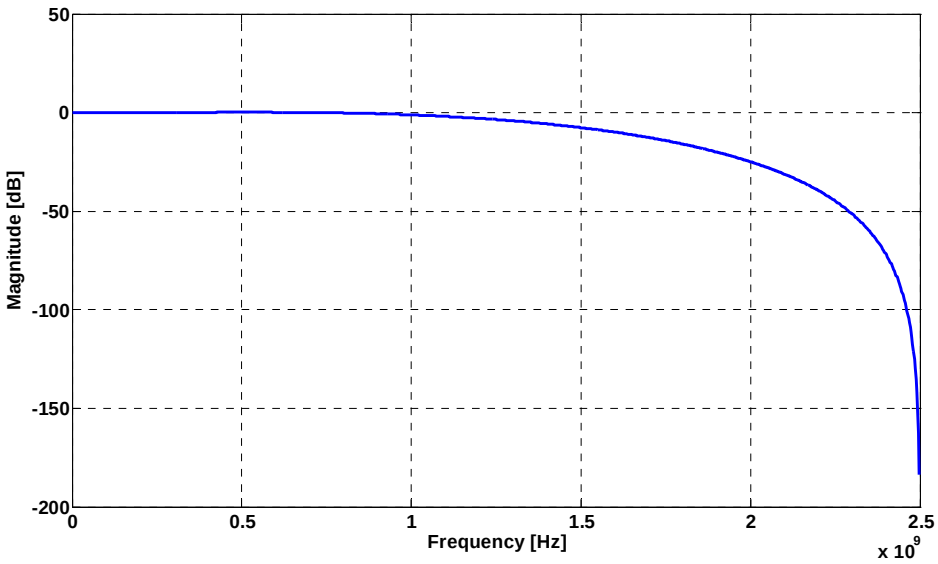


Figure 2-40: Transfer function (normalized) - 5 GHz FIR filter 6 coefficients

This filter will be cascaded with another filter with the same transfer function. Limit of the in-band attenuation of the cascaded transfer function is 1.3 dB.

2.6.2. 10 GHz filter

For the 10 GHz filter the same methodology has been applied and a solution is given in Figure 2-42.

Initial population	100
Generations	1000
Dynamic	7 bits
Number of coefficients	6-7
Fs (sampling frequency)	10 GHz
CPU time on a laptop	~ 3 hours

Table 2-10: GA parameters for 10 GHz filters

A set of filters has been found that meets the specifications; one possible solution is depicted in Figure 2-41 :

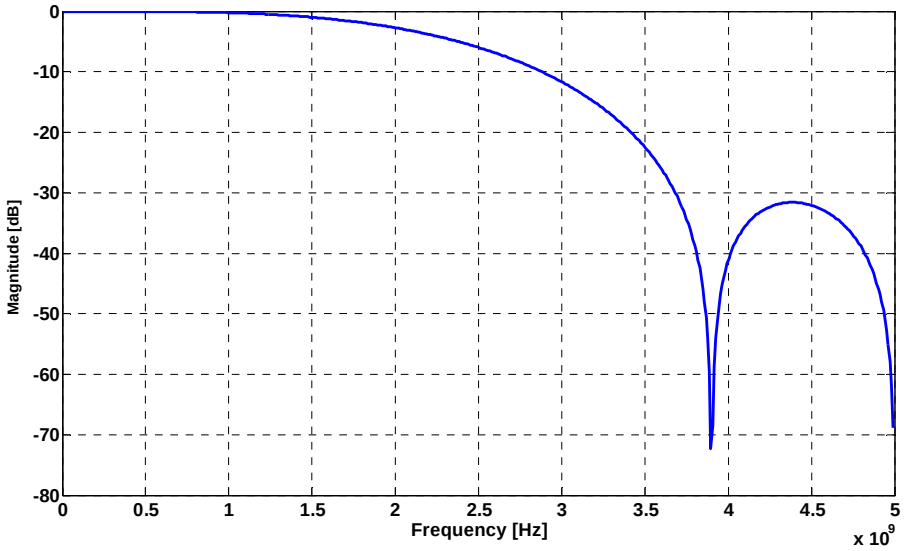


Figure 2-41: Transfer function (normalized) – 10 GHz filter 6 coefficients

Note that the number of coefficients has been increased to 7 coefficients. For the moment only even symmetry was used. It was interesting to see if better performance can be attained by adding odd symmetry which at the end is not remarkable.

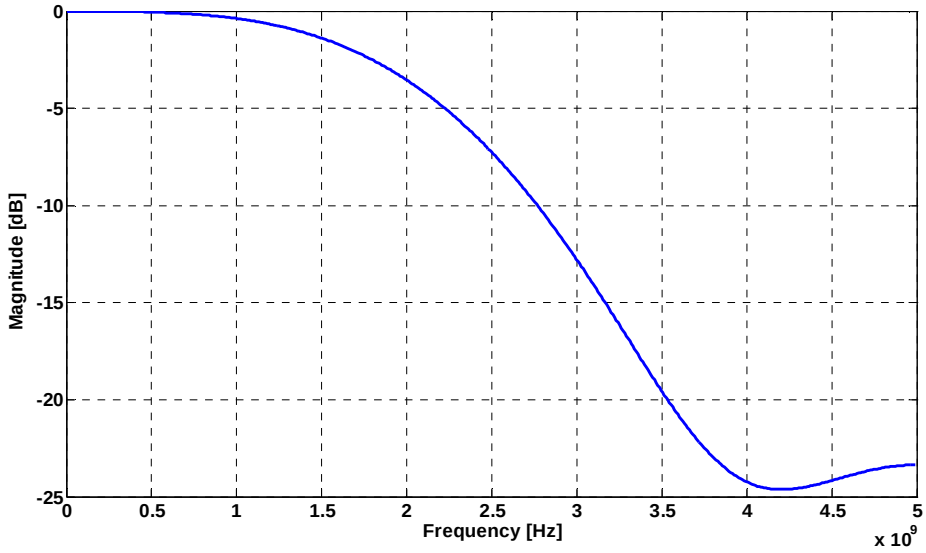


Figure 2-42: Transfer function (normalized) - 10 GHz FIR filter 7 coefficients

Table 2-11 summarizes the number of filters, coefficients and hardware complexity. A simulation has been performed with the following configuration:

- 2 filters at 5 GHz with 6 coefficients
- 2 filters at 10 GHz with 7 coefficients

	Number Coefficients	Coefficients	Adders
5 GHz (x2)	6	$\left[-2^{-4}2^{-4}2^{-1}2^{-1}2^{-4}-2^{-4}\right]$	5
10 GHz (x2)	6/7	$\left[-2^{-4}2^{-3}2^{-1}2^{-1}2^{-3}-2^{-4}\right]$ $\left[-2^{-5}2^{-6}2^{-2}2^{-1}2^{-2}2^{-6}-2^{-}\right.$	6/7

Table 2-11 : Interpolator configuration with powers of two (PO2) coefficients

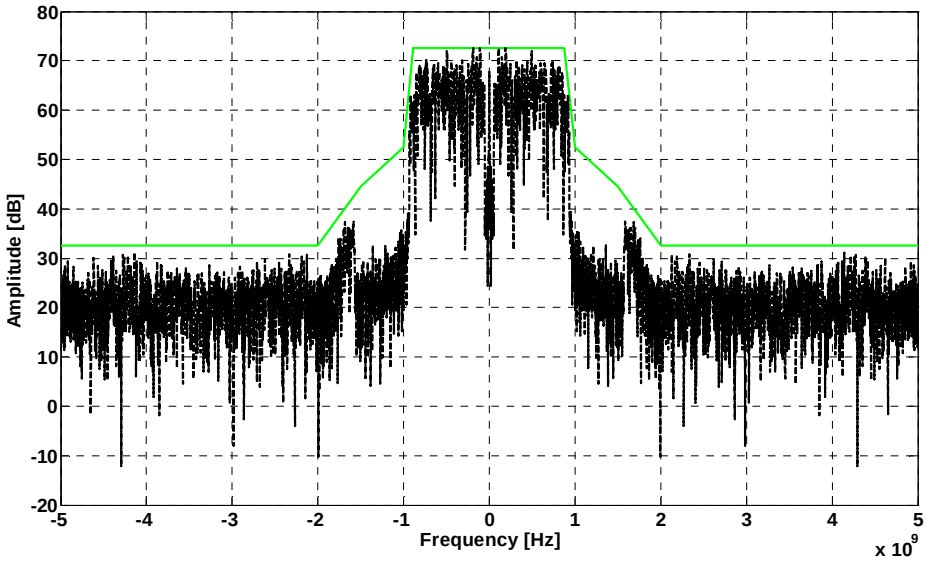


Figure 2-43: OFDM signal filtered with 2 filters at 5 GHz with 6 coefficients and 2 filters at 10 GHz with 6 coefficients.

It would be interesting to see if the complexity can be further reduced. It is unlikely that the 5 GHz filter can be changed as the margin between the mask and the first image is very small. The study has been performed for the 10 GHz filter and the number of coefficients has been reduced to 3 based on the coefficients found. New set of coefficients is presented - Table 2-12 - and represent the last improvement in this system study.

	Number Coefficients	Coefficients	Adders
5 GHz (x2)	6	$[-2^{-4}2^{-4}2^{-1}2^{-1}2^{-4}-2^{-4}]$	5
10 GHz (x2)	3	$[2^{-2}2^{-1}2^{-2}]$	2

Table 2-12 : Interpolator configuration with powers of two (PO2) coefficients used in this work

Adding the second filter at 10 GHz increases the order and so the attenuation at the limit of the band. The cost of this attenuation comes with the reduction of the design complexity at 10 GHz. This major drawback can be seen in Figure 2-44.

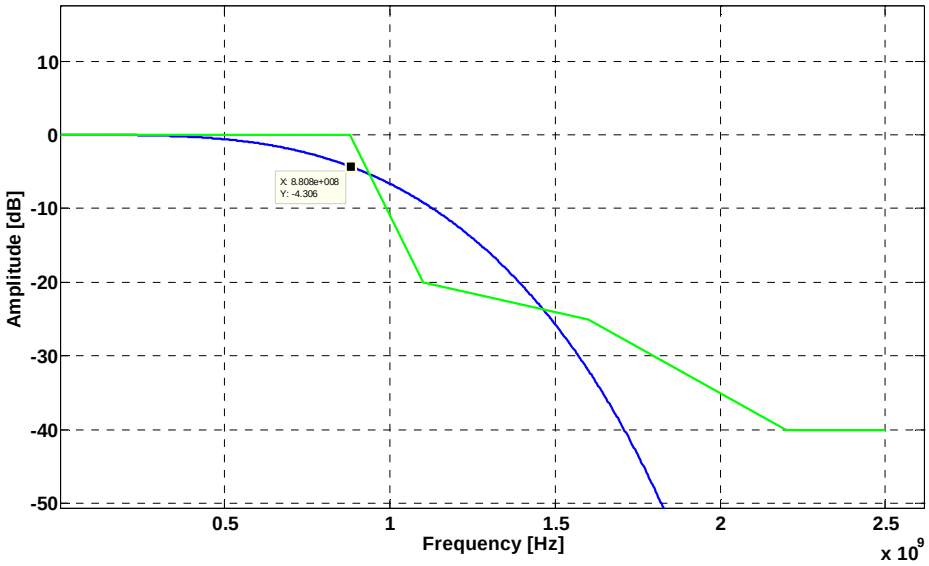


Figure 2-44: Global transfer function

Global simulation with the chosen coefficients has been performed and is given in Figure 2-45.

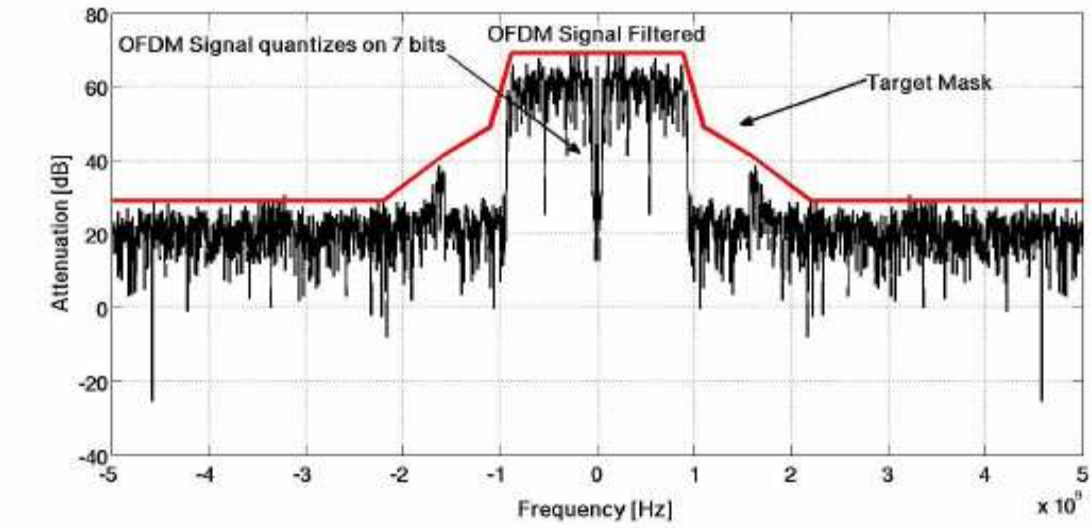


Figure 2-45: OFDM signal filtered with 2 filters at 5 GHz with 6 coefficients and 2 filters at 10 GHz with 3 coefficients

A last question must be discussed: what is the EVM? Is this filter configuration compliant with the standard? In order to answer this question some statements must be discussed:

- The EVM is dependant only on the magnitude error. Phase is linear and can be corrected by the equalization process in the receiver.

- The EVM is given in root mean square. The EVM can be calculated from the magnitude response of a system (linear scale).

The EVM is represented on the I/Q chart in Figure 2-46.

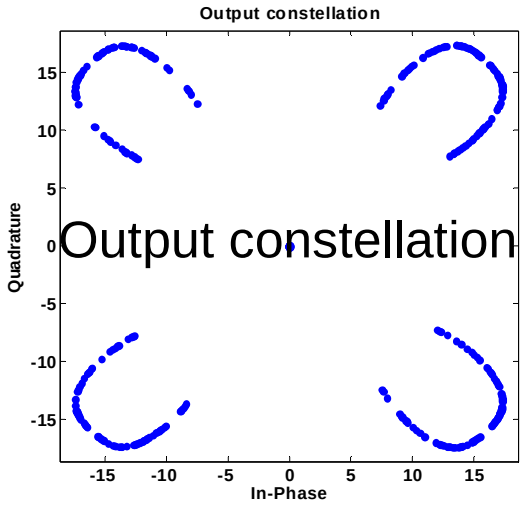


Figure 2-46: EVM simulation

The EVM is computed with the formula and the result is 17.83 % which is still compliant with the standard that required an EVM < 45 %. Note that 45 % is the EVM budget for a complete transmitter. This concludes the system analysis of the interpolator.

2.7. REFERENCE

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3. CHAPTER
INTERPOLATOR PHYSICAL DESIGN IN CMOS 65NM TECHNOLOGY

"Any intelligent fool can make things bigger and more complex... It takes a touch of genius - and a lot of courage to move in the opposite direction."

Albert Einstein

This chapter presents the design of the interpolator based on the system study presented in Chapter 2. The content is presented following a top – bottom view. First the global structure is presented. A transposed structure has been chosen. Then choices for the adder structure are motivated. With a maximum of 12 bit adder the pipelined ripple carry adder is chosen. Then a study at transistor level for different full adders and delays' structures are motivated considering the critical path of 100 ps. For the delay a fast dynamic flip-flop with a single phase clock is chosen. For the adders the CPL logic style is chosen.

A bit precise model realized with VHDL is presented. This model can be compared to the Matlab system. This model also confirms the system study.

Finally transistor design and layout are presented for the 5 GHz and 10 GHz FIR. The clock tree design is also taken in account.

A global simulation at transistor level is given in conclusion. Performances expected are also presented. The highest frequency achievable in simulation is 10 GHz on a 1.3 V supply voltage.

3.1. ELEMENTARY ARCHITECTURE

Considering the system study of Chapter 2 the interpolator is composed of 4 FIR filters. Obviously the critical path is the one where the clock period is the smallest. Here the critical path delay is 100 ps (10 GHz). This constraint is the most important one because it means that the digital logic must work at this specific frequency, which is not obvious with the actual technology. The choice of the FIR hardware structure and the digital logic that composes it determines the performance.

3.1.1. F.I.R. filters architecture

The FIR filter can be realized in several manners. Considering the frequency constraint the choice of the architecture is important. Two possible architectures are presented; other implementations are possible but are not covered in this work.

3.1.1.1. Direct structure

This structure is the direct application of the difference equation presented in chapter 2 and recall here (eq 1-1).

$$H(z) = \sum_{i=0}^{N} a_i . z^{-i} \qquad \textbf{Eq 3-1}$$

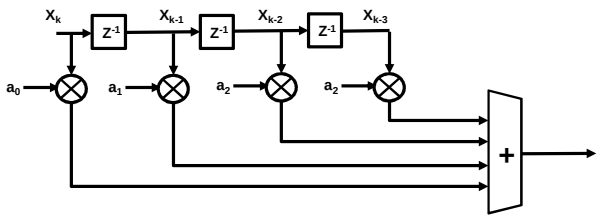


Figure 3-1: Direct Structure

The output is the sum of several weighted delayed inputs on n bits. The drawback of this architecture is the need for a single adder with a large number of inputs. This adder is in practice a cascade of 2 input adders, introducing an important over all delay.

3.1.1.2. Transposed structure

In the transposed structure the adders are spread over the filter. Instead of having one big adder structure that compute all the outputs (direct form), the adders are spread of over the structure in order to reduce the complexity of computation.

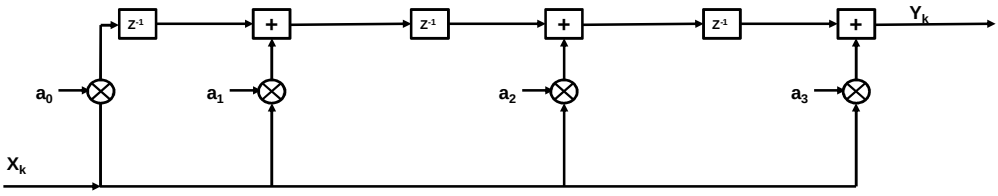


Figure 3-2: Direct Structure

As the multiplier is replaced by a shift operation, the two only components that compose the FIR are the adders and the delays.

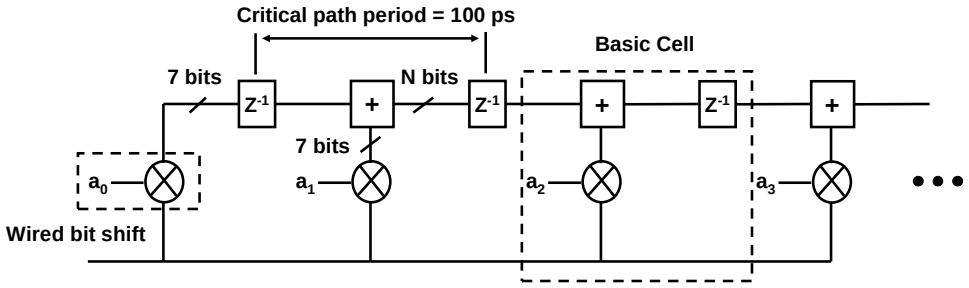


Figure 3-3: Basic cell and critical path

This transposed structure is chosen in this work.

In this structure the internal dynamic grows up from one stage to the another. A phenomenon of saturation (overflow) can appear and be propagated in the structure. Considering the coefficients found and the cascaded structure, a number of bits per filter must be defined in order to avoid the saturation effect. The number of bits/filter is studied in next sub-section.

It is also important to define the critical path in order to understand the limitations in the path. Refer to limitations come from the delays considering its T_{CQ} and T_{SETUP} time (that are correlated), from the adder considering its delay and from the quality of the clock – limited or not by the skew.

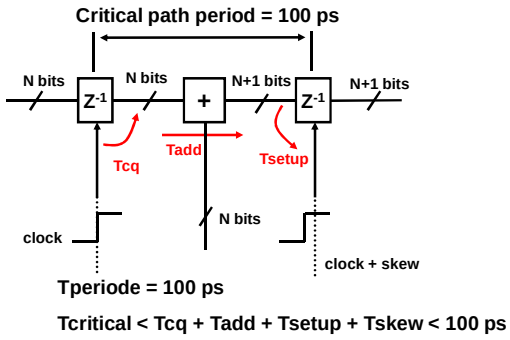


Figure 3-4: Critical path study in detail

Each component will be studied in the following section – adders and flip-flop – in order to find the best architecture in a set of possible implementations with characteristics compliant with the requirements.

3.1.1.3. Dynamic range in the interpolator

The question that must be answered is how many bits per filter must be used in order to avoid the saturation effect mentioned in the previous section?

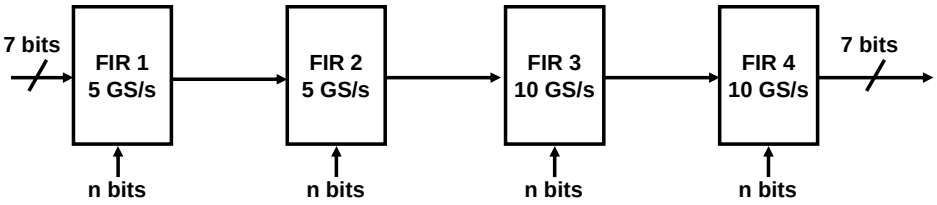


Figure 3-5: Dynamic range in the interpolator

In order to answer this question, the internal dynamic of each filter is studied following the coefficients and the signal used. Two methods are proposed. The first one is to realize the computation while continuously increasing the internal dynamic (from a filter to another) and truncate the output on 7 bits on the last stage (FIR4). The second is to increase the internal dynamic while truncating the output to 7 bits of each filter (FIR1 and FIR2 and FIR3 and FIR4). Both are presented.

a. Maximum dynamic with a continuous increase of the internal dynamic

For the 5 GS/s filter the coefficients are: $\left[-2^{-4}2^{-4}2^{-1}2^{-1}2^{-4}-2^{-4}\right]$. The convolution between the worst case input and the coefficients gives the number of bits to use in the structure to avoid saturation. Obviously the worst case is when the dynamic is the largest, here equal to 63. The convolution of $[-63,63,63,63,63,-63]$ and $\left[-2^{-4}2^{-4}2^{-1}2^{-1}2^{-4}-2^{-4}\right]$

is: $[7,-15,-63,0,118,157,118,0,-63,-15,7]$. Thus the maximum output value is: 251 (9 bits in 2's complement). This means that the size inside the FIR must be increased by 2. The same procedure can be used for the second FIR filter at 5 GS/s, its internal dynamic must be increased by 2. For the 10 GS/s FIR filters the same reasoning can be made. An increased of 2 bits per filter is needed, leading to the architecture presented in Figure 3-6.

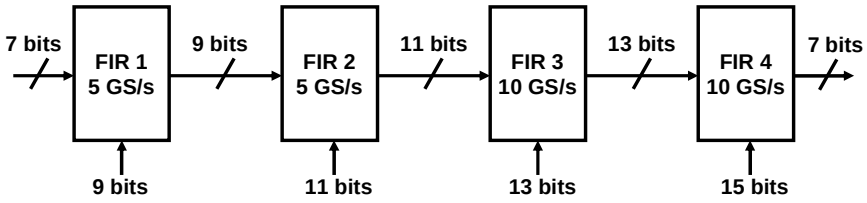


Figure 3-6: Internal dynamic adder for the 5GS/s and 10 GS/s FIR filters

b. Internal dynamic with a continuous increase of the internal dynamic while taking in account the signal

One important point must be underlined. The pattern $[-63,63,63,63,63,-63]$ is likely improbable as the signal is up-sampled by 2. System simulations have been performed on different OFDM signals and the number of bits must be increased up to 9 bits and 10 bits inside the 5GS/s architecture (FIR1 and FIR2) and to 11 bits and 12 bits inside the 10 GS/s architecture (FIR3 and FIR4). This slight improvement in terms of hardware complexity is depicted in Figure 3-7.

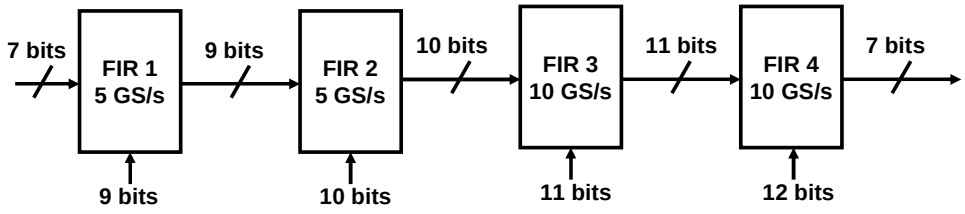


Figure 3-7: Internal dynamic for the 5GS/s FIR filters with OFDM simulation

c. Internal dynamic with a truncation at the output of each filter

The other solution is to increase the internal dynamic to avoid the saturation (like in Figure 3-7) and truncate the outputs to the initial dynamic (7 bits) for each filter. The advantage of this solution is that the internal dynamic of each filter tends to decrease and thus the hardware complexity. This solution is exhibited in Figure 3-8.

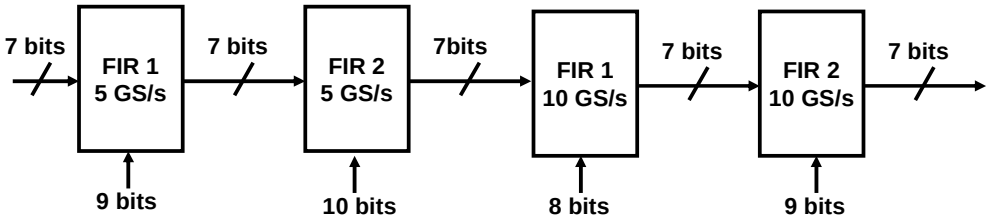


Figure 3-8: Internal dynamic with the truncated output

d. Chosen solution

The solution of Figure 3-6 requires too much hardware for improbable cases. Based on different OFDM symbols, the solutions proposed in Figure 3-7 and in Figure 3-8 are more interesting. In this work the method that has been investigated is the method presented where the dynamic increases continuously and the signal is truncated at the last stage (FIR4). The main reason is that the continuous truncation affects the global output precision. A loss of 2 LSB at the output can be noticed between the solution of Figure 3-7 and in Figure 3-8. Thus the global frequency response slightly changes. The frequency response to an impulse is presented in Figure 3-9. A better out of band attenuation is obtained in the case of a continuous increase of the dynamic.

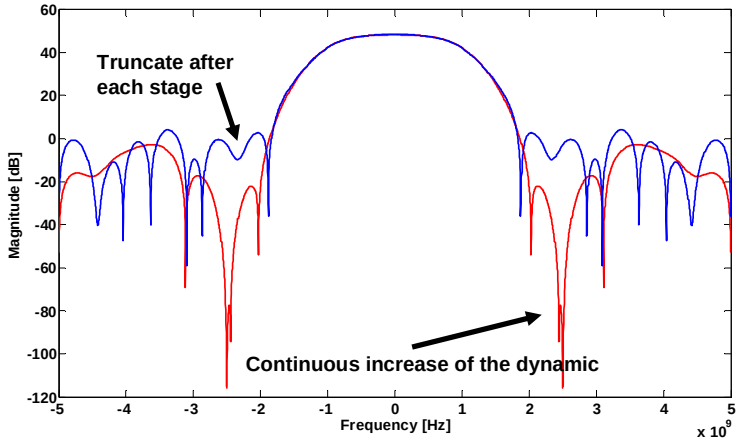


Figure 3-9: Frequency response of the FIR filter depending on the internal dynamic

3.1.2. Adder architecture

The adder is a component that has been largely studied in the past years. Here at the top level, the choice of the right adder for the targeted circuit is important. Speed is the key point but area, consumption and complexity must also be taken into account.

3.1.2.1. The binary adder definition

Table 3-1 shows the truth table of a binary full adder. A and B are the adder inputs, C_i the carry input, S the sum output and C_o the carry output.

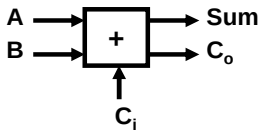


Figure 3-10: 1 bit binary adder

A	B	C_i	S	C_o	Carry Status
0	0	0	0	0	Delete
0	0	1	1	0	Delete
0	1	0	1	0	Propagate
0	1	1	0	1	Propagate
1	0	0	1	0	Propagate
1	0	1	0	1	Propagate
1	1	0	0	1	Generate
1	1	1	1	1	Generate

Table 3-1: Truth table for Full Adder

Boolean equations for S and C_o are:

$$S = A \oplus B \oplus C_i$$
$$= A\overline{B}\overline{C_i} + \overline{A}B\overline{C_i} + \overline{A}\overline{B}C_i + ABC_i \quad \textbf{Eq 3-2}$$

$$C_0 = AB + BC_i + AC_i \quad \textbf{Eq 3-3}$$

S and C_o can be defined as a function of the signals generate, delete and propagate. $G(Generate) = AB$, $D(Delete) = \overline{A}\overline{B}$ and $P(propagate) = A \oplus B$

Thus S and C_i can be rewritten as:

$$S = P \oplus C \quad \textbf{Eq 3-4}$$

$$C = G + PC \quad \textbf{Eq 3-5}$$

For details on the ripple adder please refer to [Rabaey]

3.1.2.2. The ripple carry adder

An N bit adder can be made by cascading N binary adder as presented in Figure 3-11

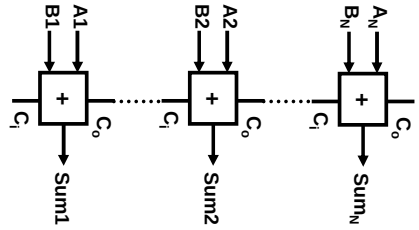


Figure 3-11: N bit adder

This architecture is called the ripple carry adder because the carry ripples from an adder to another one. To study the critical path, it is interesting to compute the delay of this structure and see that the delay is not constant and depends of the number of adders to pass through, which depends of the input signals. The worst case condition is when a carry is generated at the LSB (least significant bit) position and propagate up to the last adder. The delay is then proportional to the number of bits in the input words N and is approximated by:

$$t_{adder} = (N-1)t_{carry} + t_{sum} \qquad \textbf{Eq 3-6}$$

Where t_{carry} and t_{sum} represent the delay from C_i to C_o and Sum respectively.

This mean that the propagation delay of the ripple carry adder is linearly proportional to N. This delay becomes important when dealing with a large number of bits. From Eq 3-6 it is important to notice that when designing the full adder cell for a fast ripple carry adder it is more important to optimize delays for the carry than for the sum since the sum has less influence on the global adder delay.

3.1.2.3. Other adder style

For further reading the author invites you to read [Rabaey]

a. Carry skip adder

The idea is to skip the adders when there is carry propagation.

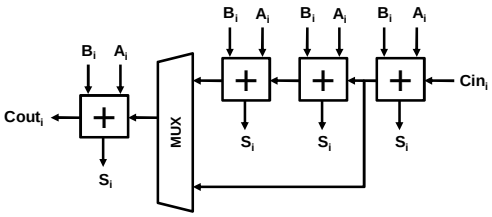


Figure 3-12: Carry skip adder

Carry-skip logic is added to each block to detect when the carry-in of the block can be passed directly to the next block. The carry propagation still exists but demands less computation.

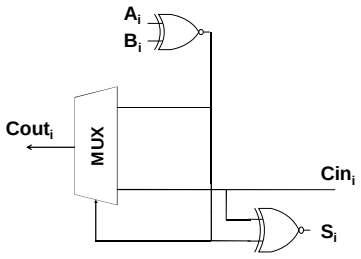


Figure 3-13: 1 bit Carry skip adder

This implementation needs a multiplexer to propagate the carry, which makes 32 transistors (28 + 4) for the static CMOS realization.

b. Carry look ahead adder

The idea is to compute the carry from the propagation terms. Each carry is computed with the precedent carry. We can compute the final carry with all the precedent carries. This architecture is very good for a large number of bits. For a small number of bits (< 16) this architecture does not show any improvements compare to the ripple carry adder.

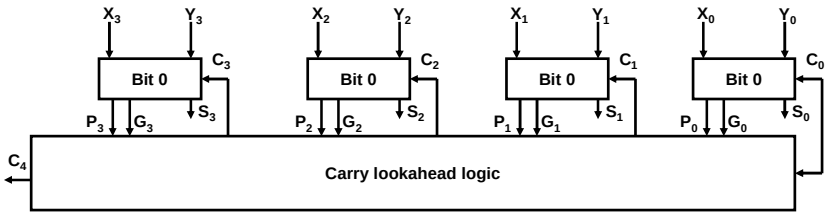


Figure 3-14 : 1 bit Carry look ahead adder

c. Carry Select adder

The idea behind the carry look ahead adder is to compute the actual addition in parallel with the two possible carries (1 and 0) and when the correct carry arrives from the previous stage, it selects the correct sum. Thus the carry select adder consists of two ripple carry adder and one multiplexer.

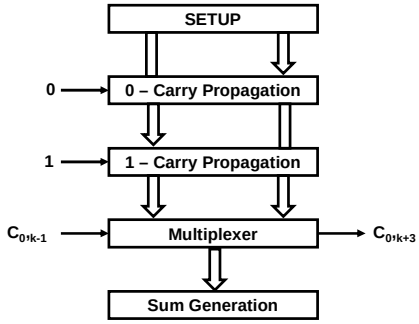


Figure 3-15: 4 bit carry select adder

The propagation delay is still linearly proportional to N because the block select signal that selects between the 0 and 1 still has to ripple through all stages by the multiplexer in the worst case.

d. Choice of the adder

Considering the size of the largest word in the structure (12 bits) the ripple carry adder is chosen. The main reason it is its simplicity of realization and design. The complexity added by the other architectures is not justified considering the small number of bits to process.

For further reading about adder architectures the reader can refer to [Rabaey].

3.2. CHOICE OF THE LOGIC

In this section the FA and the delay are studied at transistor level. Different architectures are presented. The final logic style is chosen based on simulations.

3.2.1. Full adder (FA logic style)

Once the global architecture of the interpolator and the adder structure has been defined two questions must be answered. 1) The first one is how to realize the basic cell which is the full adder and which transistor architecture must be used to reduce at the maximum the delay. 2) The second one is based on this study how many adders can be cascaded on one clock period. Here the reference clock frequency is 10 GHz as it is the critical frequency.

Many logic styles exist. Here only static logic is treated. The trade off between all of them is based on the speed, the power and the area. Considering the constraints of the design the speed is considered as the most important parameter. Two styles are commonly used: the complementary logic which is the most robust, must be sized and leads to large and thus slow gates and the pass transistor logic which is simple, fast, ratio-less but less robust.

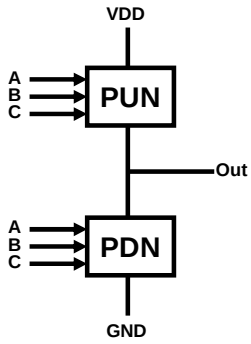


Figure 3-16: Complementary logic

Figure 3-17: Transistor pass logic

PUN and PDN in Figure 3-16 refer to pull up network (P transistors) and pull down network (N transistors).

3.2.1.1. Standard static CMOS full adder

The full adder is found from the Boolean expression and is represented in Figure 3-18:

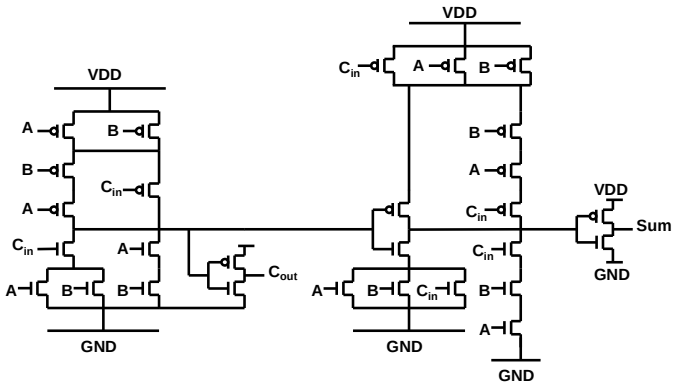


Figure 3-18: Direct implementation of the FA (28 Transistors)

A total of 28 transistors are used. A slight improvement can be made by using the Propagate/Generate/Delete signals to create a new topology Figure 3-19. In this architecture the carry out inverter is eliminated and the PUN and PDN are not dual anymore. This reduction in both areas and delay is a first step to accelerate the simple FA (full adder) architecture.

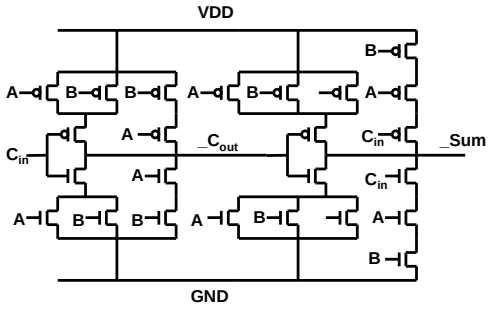


Figure 3-19: Mirror implementation of the FA (24 Transistors)

3.2.1.2. Transmission gate based adder

A full adder can be designed with transmission gates. The basic XOR function realized in the FA can be implementation with a multiplexer which is the basic function of transmission gates.

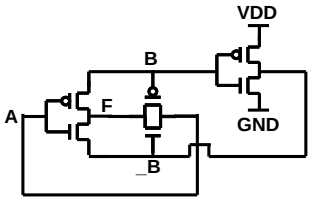


Figure 3-20: Transmission gate XOR

Figure 3-20 presents the basic XOR function realized with transmission gates. The output is $\overline{F} = (\overline{A}.B + A.\overline{B})$.

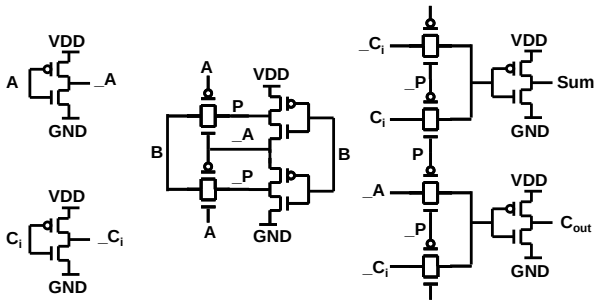


Figure 3-21: Transmission gate based full adder (24 Transistors)

This implementation (Figure 3-21) is no more considerated as complementary style logic. A full adder implementation based on the Propagate/Generate/Delete model is proposed in Figure 3-21 and uses 24 transistors. The propagate signal - A XOR B - is used to select the true or complementary value of the input carry as the new sum output. Based on the propagate signal, the output carry is either set to the input carry, or to one of inputs A or B. The main advantage of such an adder is that it has similar delays for both sum and carry outputs.

However the delays increase not linearly when pass gates are cascaded. This is important to underline when one deals with adders where cascades appear naturally. The approach to overcome this problem is to break the chain and insert buffers in order to restore the signal.

3.2.1.3. Pass transistor logic

Transmission gates have been used to realize a FA. Is it possible to reduce the XOR function while not using a transmission gate (NMOS and PMOS) but with only NMOS or PMOS. Obviously the reason for reducing the number of transistors is to lower the capacitance and thus reduce the delay.

A major problem when one wants to use pass transistors with only NMOS (or PMOS) transistors is the loss of complementary. NMOS transistor is effective to pass a 0, but is poor to pass a 1. When the pass transistor pulls a node to VDD, the output only charges to VDD - V_T. The fact is that the V_T will change because of the body effect thus the problem is getting worse. Considering the loss of a V_T at the output, another occurs, pass transistor gates cannot be cascaded by connection the output of a pass gate to the gate input of another pass transistor gate. The gate drive would be reduced to VDD - V_{TH1} - V_{TH2}.

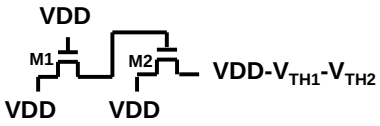


Figure 3-22: pass-transistor driving an other gate

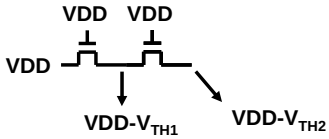


Figure 3-23: pass-transistor not driving an other gate

An inverter must be added at the output of the structure to recover the level in order to drive another gate. This logic style has an advantage to exhibit lower switching power but the disadvantage to have static power consumption – the output is a weak one thus PMOS of the subsequent CMOS inverter is not turned off completely.

A differential version of the pass transistor logic exists, called CPL in the literature. This kind of logic is used in general for high performance design. The basic idea behind CPL is to accept differential inputs and produce differential outputs. This kind of logic has interesting properties:

- Since the circuits are differential, complementary signals are always available and no extra inverters are needed.
- CPL belongs to the static logic style. The output is always connected to either VDD or GND.
- The same topology can be used for different gates, only inputs are permutated which leads to a very modular design.

The main drawbacks are that gates cannot be cascaded and the routing overhead of the complementary signals in the physical layout. Like single-ended pass transistor logic, differential pass transistor logic suffers from static power consumption and a reduced noise margin because of the drive to any high input to VDD - V_{TH}. A solution (that works for both single and differential pass gate logic style) exists to overcome this problem

which is the level restorer. The level restorer is (in the case of NMOS architecture) a single PMOS transistor put in a feedback path.

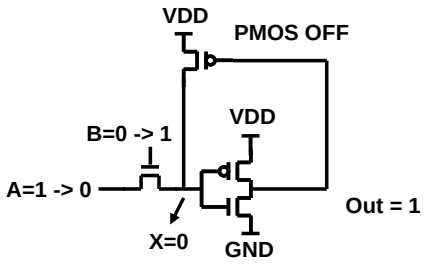


Figure 3-24: level restorer circuit (1)

If A is at 0 and B is at 1 the node X is charge to 0, the output inverter is at 1 and the state of the PMOS transistor is off. This is the normal operation for the transmission gate (Figure 3-24). Now the other operation for the transmission gate is when A switches from 0 to 1 (Figure 3-25). The node X is first charge to VDD - V_{TH}, which is enough to switch the output of the inverter to 0. Thus the PMOS is ON and drives the node X to VDD. This eliminates any static power dissipation in the inverter. Moreover no static current path exists through the level restorer and the pass transistor since the level restorer can be active only when A is at VDD.

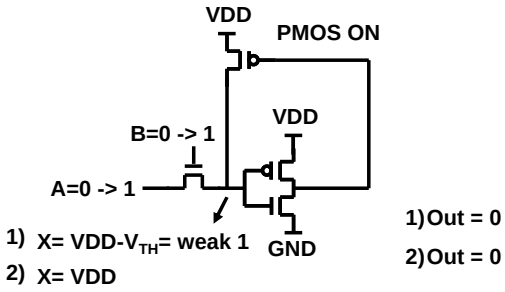


Figure 3-25: level restorer circuit (2)

While this solution eliminates the problem of static consumption another problem arises when the node X that has been set to 1 must be passed at 0. The pass transistor tries in one way to pull down the node X, while the level restorer tries to pull up the node X. In that specific case the pull down network must be stronger than the pull up network.

3.2.1.4. Adders simulation

The three different architectures have been designed and simulated after physical layout (PLS - post layout simulation) in different corners (typical, slow and fast) for maximum resistance and capacitance extraction over 1 V supply voltage.

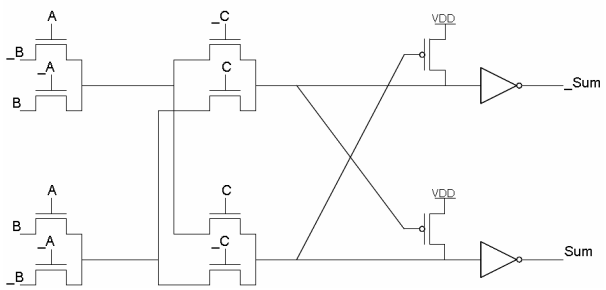
	CPL	TG	Combinational
Typical	40 ps	66 ps	50 ps
Fast	30 ps	46 ps	40 ps
Slow	49 ps	93 ps	66 ps

Table 3-2 : Benchmark of different adders

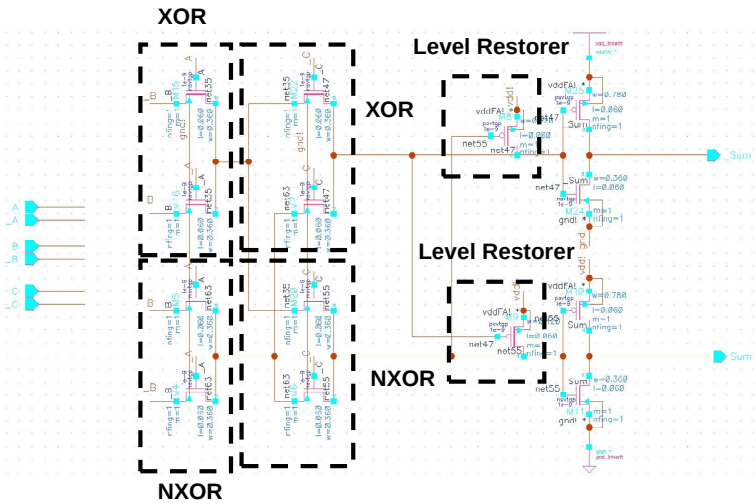
Considering the simulation results, CPL seems to be the right choice. The advantage of using CPL is that less than 30% of the clock period is used to compute a 1 bit addition. The drawbacks are the increased number of wires to route in the physical layout, the increased number of flip-flops (basically 2 times more) and the reduced noise margin.

3.2.1.5. CPL design

The CPL full adder is separated in two parts, a part that computes the SUM and the other that computes the CARRY OUT signal.



a)



b)

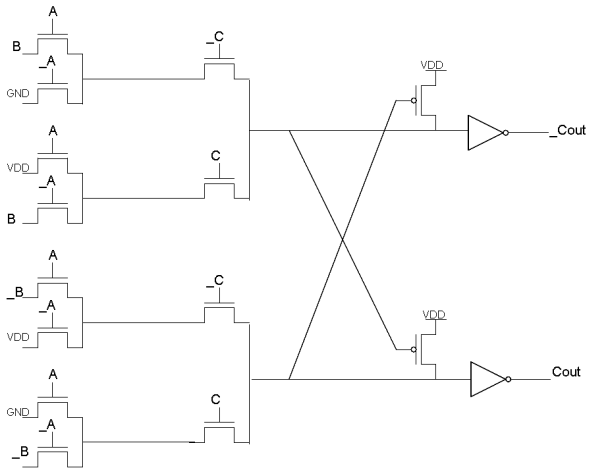
Figure 3-26: Sum CPL a) and b)

Both Sum and Carry parts have been designed to charge a flip-flop input capacitance. As CPL is a non-ratioed logic, all NMOS transistors have the same sized which is 3*Wmin/Lmin (with Wmin = 0.135u and Lmin = 0.065u). The level restorer has been designed considering the global size of the pull down network. Thus the size of the PMOS is Wmin/Lmin.

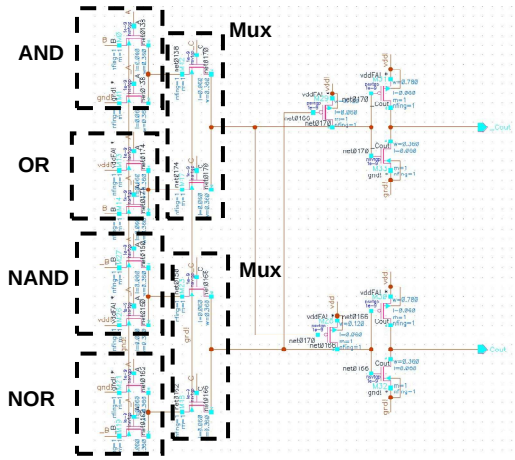
	W [um]	L [um]
NMOS	3*0.135	0.065
PMOS	0.135	0.065

Table 3-3 : Transistors size for the CPL full adder

The adder has been simulated in post-layout simulation with a 10 GS/s signal. The current consumption of the CPL adder is 48uA on 1 V nominal VDD.



a)



b)

Figure 3-27: Carry out CPL a) and b)

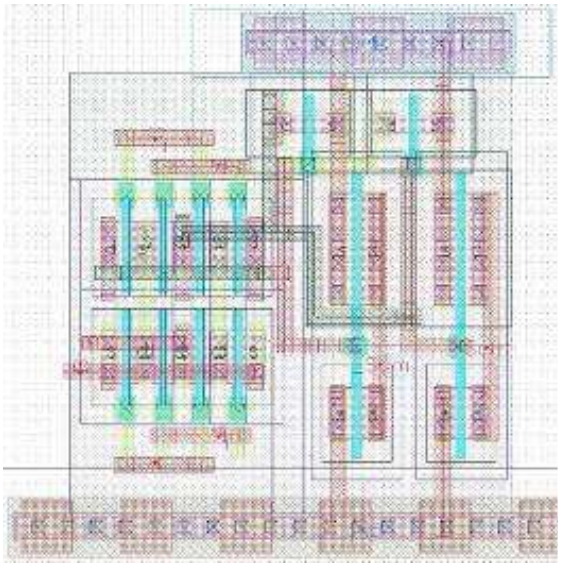


Figure 3-28: Sum CPL layout

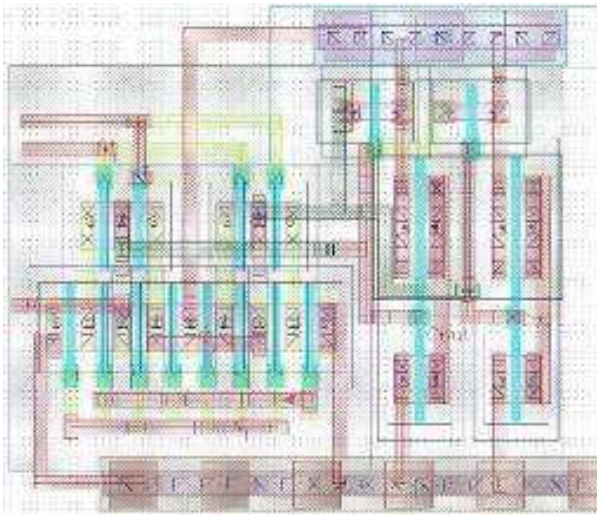


Figure 3-29: Carry out CPL layout

The layout sizes for the sum are 4.7 x 3.8 um^2 and for the carry are 4 x 4 um^2.

3.2.2. Delay (flip-flop)

Many architectures of flip-flops exist. One of the fastest is the True Single Phase Clock Flip-Flop (TSPCFF). It is able to work at several GHz. As stated in its name the TSPCFF uses only one clock phase. No inversion of the clock is needed.

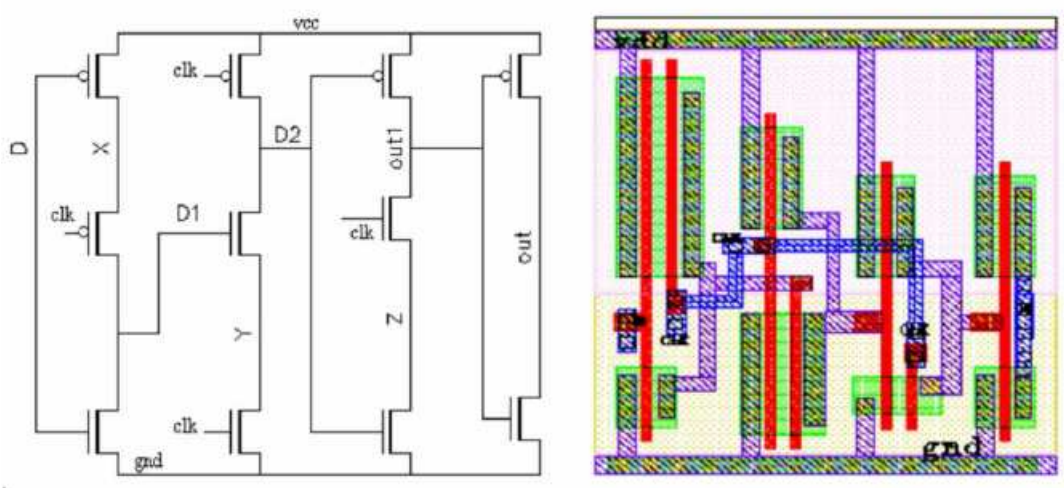


Figure 3-30: Schematic and layout of the TSPCFF

Figure 3-30 depictes the schematic and layout of the TSPCFF. The layout size is 5.4 x 4.5 um^2. The current consumption is 59 uA on a nominal 1V VDD.

Figure 3-31 describes the mechanism of operation. When the clock signal is low, D2 node is stuck at Vcc through the conducting PMOS. This phase is called “precharge”. Thus, out1 node is left high impedance and out node is its complementary. These latter nodes keep their preceding values (“hold” phase). D1 node is the complementary of D input.

When the clock signal goes high, then D2 becomes dependent on the D1 value. This is called “evaluation”. If D1 is low, then D2 does not change its precharge value. If D1 is high, then D2 node decharges through the NMOS transistors. The nodes out1 and out follow the D2 node as they are in an inverter configuration (“active” mode).

The register operation is very fast, but output edges rise and fall times and related propagation delays are different. A solution for equalizing the propagation delays for each transition is to adjust the out1 discharge time to the D2 discharge plus out1 charge times, by adjusting sizes of NMOS and PMOS transistors. In fact, out1 discharge must be slowed down whereas its charge must be fastened. This can be made by simulating the flip-flop to find the best optimization.

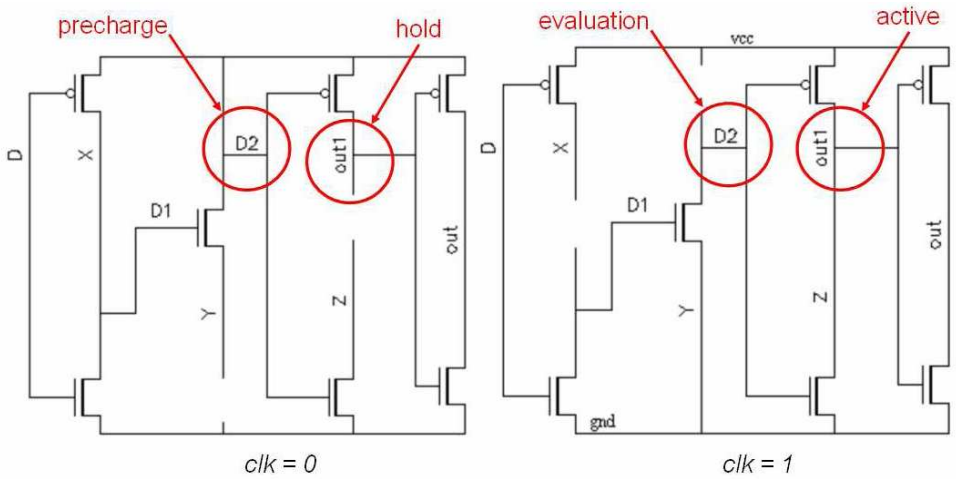


Figure 3-31: Mechanism inside the TSPCFF for clock low and clock high

In the study of a flip-flop one important parameter must be taken in account: the setup time (is the minimum amount of time the data signal should be held before the clock event so that the data are reliably sampled by the clock). This parameter is never studied alone because it is correlated to the clock-to-q (which is the time the flip-flop takes to change its output after the clock edge). This correlation can be understood easily by narrowing the time interval between the arrival of the data at the input and the clock edge.

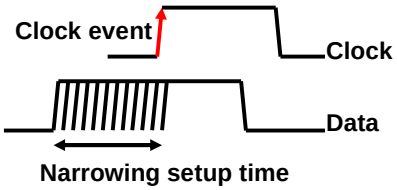


Figure 3-32: TCQ vs setup time simulation

This leads to a gradual degradation of the registers' delay. In simulation a couple – setup time, clock-to-q – can be computed. The result of this simulation is depicted in Figure 3-33. The 0 ps point correspond to the clock edge. The simulation has been performed with maximum resistance and capacitance extraction, at nominal supply voltage. The load is the CPL F.A.

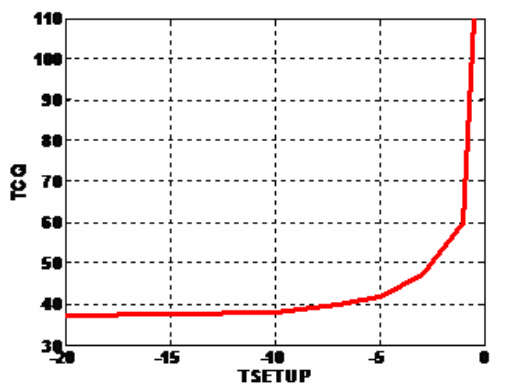


Figure 3-33: T_{CQ} vs T_{SETUP}

Figure 3-33 shows the degradation of the clock delay with the narrowing of the setup time. Close to 0 (clock event) the delay becomes really large (the data is not latched reliably). Far from the clock event the data is latched and the delay quasi constant.

A 5 ps (minimum) of T_{SETUP} for a 42 ps of T_{CQ} can be expected. This custom design takes benefit of driving the flip-flop close to its point of failure but with the best trade-off to expect a critical path under 100 ps.

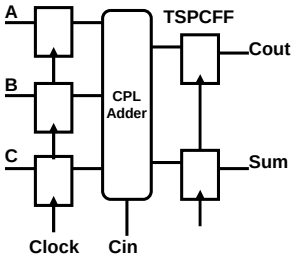
Finally the TSPCFF latch malfunctions when the slope of the clock is not sufficiently steep. A slow clock causes both NMOS and PMOS to be on, resulting in an undefined value and race conditions. This is an important remark and must be well studied in the clock tree design (see next section).

3.2.3. Critical path revisited

The full adder choice is the CPL and the flip-flop choice is the TSPCFF. In this sub-section, the critical path is revisited at transistor level. First the critical path at 10 GHz is presented and then the 5 GHz critical path.

3.2.3.1. 10 GHz critical path

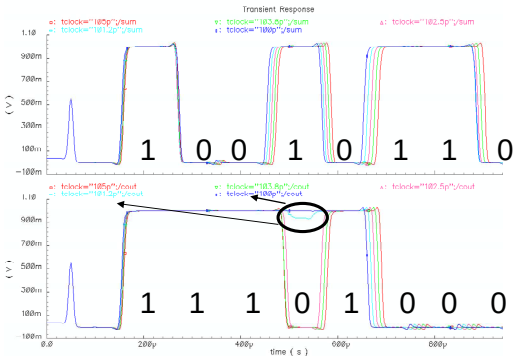
Now that the basic cells of the FIR have been designed, a global simulation of the critical path can be made. The simulation is performed with a clock at 10 GHz, with typical resistance and capacitance extraction, at a nominal temperature and a nominal supply voltage. No skew and jitter has been introduced. Buffers are introduced at the inputs and outputs are loaded with extra flip-flops.



(CMOS 65n)	Delay
TSPCFF	42ps
CPL Adder	48ps

Figure 3-34: Critical path at 10 GHz revisited

Results of the simulation are depicted in Figure 3-35. Inputs signals are generated to test all the possible patterns. The output carry and sum are compared to the truth table.



A	B	Ci	Co	S
1	1	1	1	1
0	1	1	1	0
1	0	1	1	0
0	0	1	0	1
1	1	0	1	0
0	1	0	0	1
1	0	0	0	1
0	0	0	0	0

Figure 3-35: Simulation of the critical path at 10 GHz

The post-layout simulation results show that the minimum valid critical path attained is 102 ps. The performance is layout dependant but here without going further in the physical layout, the main problem is that in the critical path a flip-flop must drive the inputs of the sum and carry blocks. That means that 6 flip-flops are used for the inputs (3 inputs and 3 complementary inputs) and 4 for the outputs (2 outputs and 2 complementary outputs). After physical layout, different wires and parasitic capacitances must be driven, which decreases the working frequency. Nevertheless the simulation passes when the supply voltage increases from 1V nominal to 1.1V.

A way to achieve a critical path under 100 ps with a nominal supply voltage of 1 V is to double the number of flip-flops. Now a flip-flop drives only one input while another one drives the complementary input. Drawbacks of this solution is that it increases the number of flip-flops in the chip, thus the power consumption and two different data paths exist for the same data which can lead to data dependency problems. That is why the first solution has been kept even if the critical path is not under the 100 ps but close.

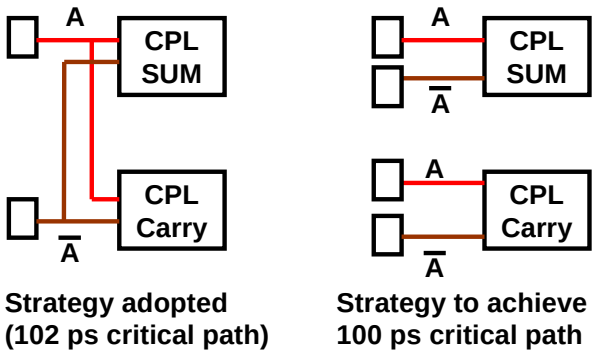


Figure 3-36: Different strategies to route signal to achieve a high working frequency

3.2.3.2. 5 GHz critical path

At 5 GHz the critical path must be under 200 ps. The last question is how many adders can fit inside the 200 ps period. The answer is 2 at the maximum, meaning that a pipeline of 2 can be used. The critical path at 5 GHz is depicted in Figure 3-37.

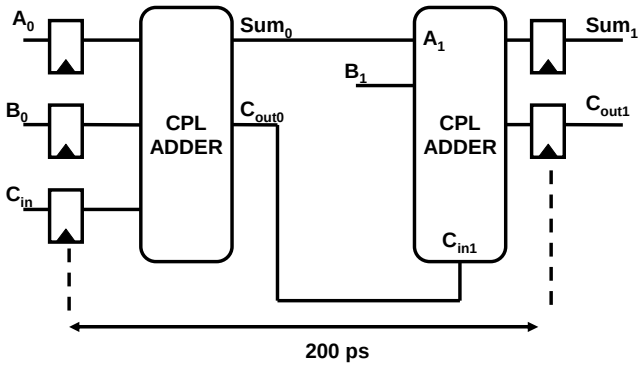


Figure 3-37: Critical path at 5 GHz revisited

3.3. VHDL MODEL OF THE INTERPOLATOR

Different important points to the design of the interpolator have been decided in the previous sections. The first one is the choice of the transposed structure. The second is the choice of the ripple carry adder. The third is the logic style and the choice of the CPL FA and TSPC flip-flop. The fourth is the use of a pipeline structure with a depth of 2 at 5 GHz and a depth of 1 at 10 GHz. Based on these informations a bit precise model can be constructed in order to validate the global architecture before going into the design.

3.3.1. 5 GHz FIR filter bit precise model

The first step is to delay the data in order to dispose of the delayed and shifted data at the right moment (clock event) in the filter. In other words the data multiplied by the coefficients must be provided in the structure. This operation is depicted in Figure 3-38 for the two first bits (bit0 and bit1). This structure must be extended 5 times in order to increase the internal word length up to 10 bits. The MSB (7^{th} bit) is extended internally in order to provide delayed values starting at the 4^{th} bit. At the output of the first 5 GHz filter delays must be added in order to provide the correct data to the second FIR filter. The second FIR filter is identical to the first one.

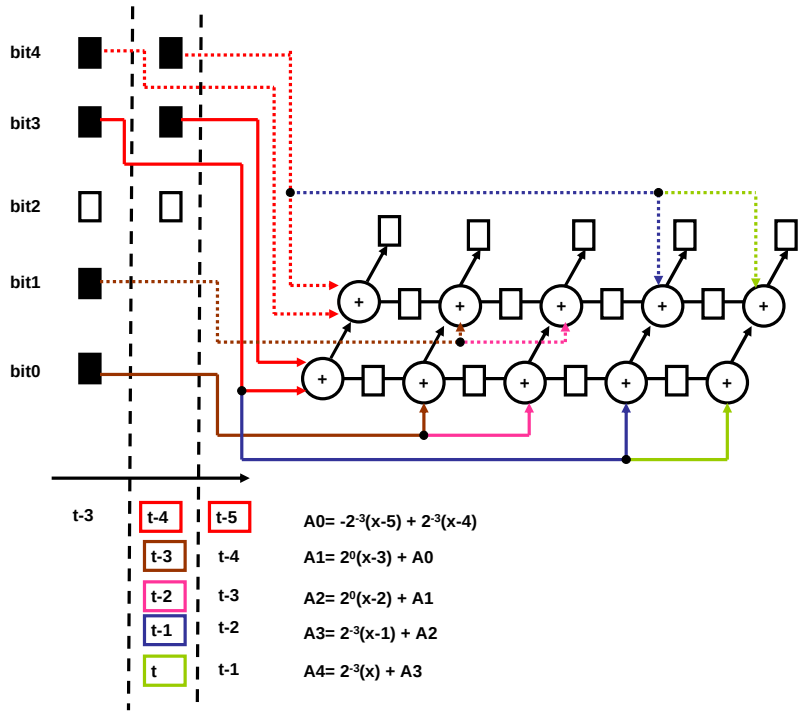


Figure 3-38: Basic cell for the 5 GHz filter

3.3.2. 10 GHz FIR filter model

The same methodology is applied to realize the 10 GHz filter. Before going in detail of the 10 GHz filter it is important to see that at the interface between the 5 GHz and 10 GHz filter, delays are introduced. This is needed in order to pass from a pipeline of 2, to a pipeline of 1. The operation is depicted in Figure 3-39 for the two first bits (bit0 and bit1). This basic structure must be extended to 11 bits and 12 bits, respectively for the first 10 GHz filter and second 10 GHz filter.

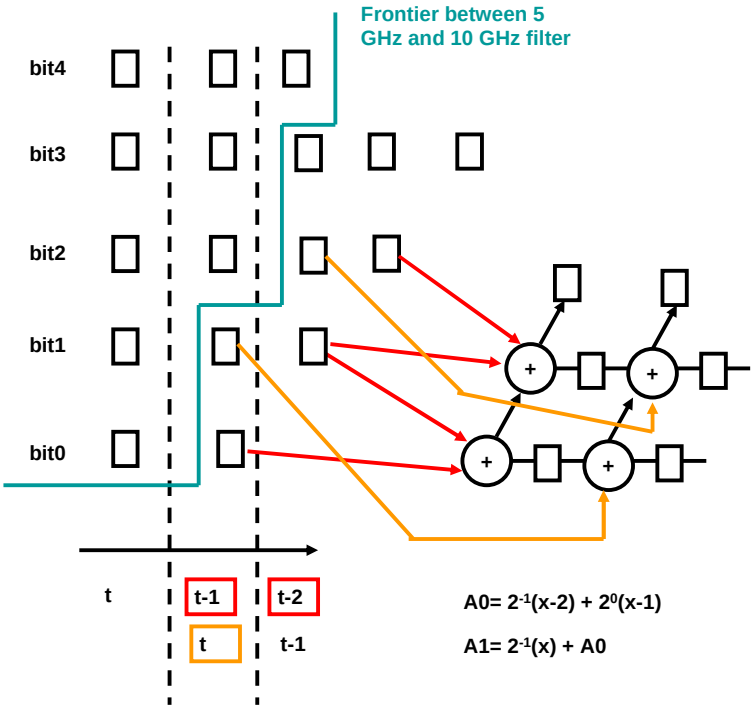


Figure 3-39: Basic cell for the 10 GHz filter

1.1.1. Complete FIR

The complete interpolator is depicted in Figure 3-40. For simplicity only one slice is represented. As explained previously, buffers are placed at the beginning of the structure to obtain the shifted data in the pipeline. Between the two FIRs at 5 GS/s, buffers are inserted in order to provide a latency to get the shifted data still in the pipeline. Buffers are also inserted between the 5 GS/s filter and the 10 GS/s filter. These buffers are necessary to pass from a pipeline of two to a pipeline of one. Between the two FIR at 10 GS/s, buffers are inserted to provide a latency to get the shifted data in the pipeline. Finally at the output of the last 10 GS/s filter, buffers are inserted in order to get the 7 bits outputs on the same clock event.

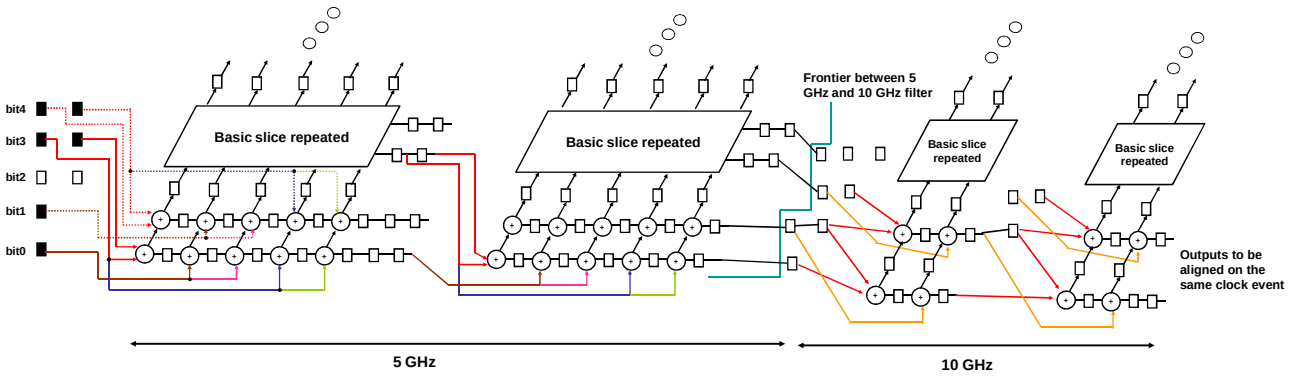


Figure 3-40: Complete interpolator structure on one slice

3.3.3. Simulation

In order to simulate the global architecture an OFDM symbol, previously generated and quantized in Matlab, is used. This is a good way to test the filter with VHDL and see the attenuation. The main problem is that this kind of simulation will not be practical at transistor level. In order to compare the 3 different simulations – Matlab, VHDL and transistors – a simplified pattern must be used.

Recall that FIR filters with fixed coefficients are linear time invariant system, the best pattern to compare the 3 systems is the impulse response (or equivalent: step response, sinusoidal response…). Table 3-4 shows the response to the impulse 63 in Matlab and in VHDL. The Matlab response has been rounded with the "fix" operator.

Matlab (fix)	-7 -23 -39 -37 0 92 224 354 440 440 354 224 92 0 -37 -39 -23 -7
VHDL	-7 -21 -38 -36 1 91 222 350 434 434 350 222 91 1 -36 -38 -21 -7

Table 3-4 : Impulse response of the interpolator Matlab vs VHDL

The difference between the two impulse responses can be easily understood. Matlab computes the impulse response with decimals while in the VDHL model decimals are ignored.

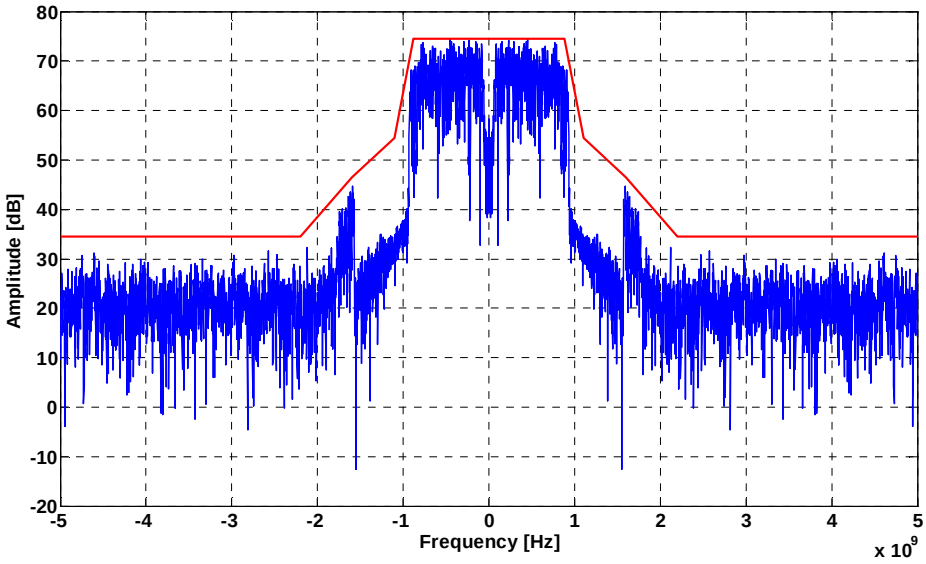


Figure 3-41: VHDL model response to a an OFDM symbol

3.4. TRANSISTOR LEVEL DESIGN OF THE INTERPOLATOR

This section is about the design at the transistor level of the interpolator. The interpolator is designed based on the VHDL model that defines the global architecture,. The basic cells used to realize the addition and delay operation are the CPL adder and the TSPC flip-flop, already demonstrated in post layout simulation in the previous section.

3.4.1. 5 GHz filter transistor level design

As seen previously in the VHDL model section, the design is very modular. It means that once a basic cell is designed, the filter is just an extended version of this cell on a certain number of stages specified by the internal word length of inside the filter. For the 5 GHz filters an extension to 10 bits is needed. Thus the basic cell presented in the previous section is repeated 5 times.

3.4.1.1. 5 GHz filter basic cell

The basic cell for the 5 GHz filter is depicted in Figure 3-42. The pipeline of two is made by inserting flip-flops after two consecutive adders.

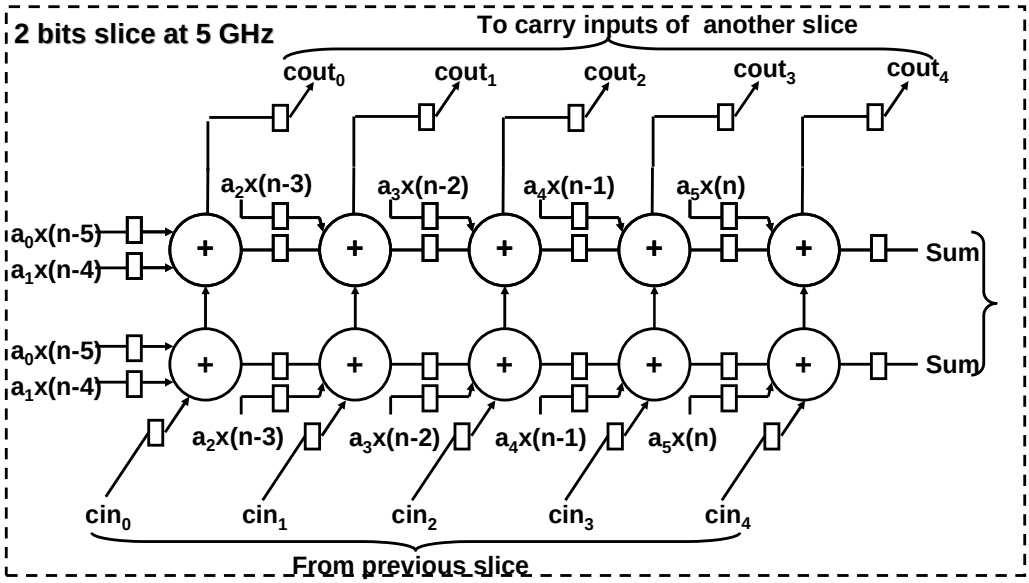


Figure 3-42: Transistor level of the basic cell for the 5 GHz filter

3.4.1.2. 5 GHz complete structure

The complete structure is a cascade of 5 elementary structures. The impulse response is still used to simulate the behaviour of the filter. Impulse response for one filter at 5 GHz is provided in a typical corner, on a nominal supply voltage of 1V, at 27°C, loaded by flip-flops. The impulse amplitude is 63 (0111111b).

Note on the simulator: the simulator chosen is Cadence Ultrasim. This choice must be noticed because the structure becomes very complex and the number of transistors will increase. Cadence Spectre becomes too slow to simulate such large structures.

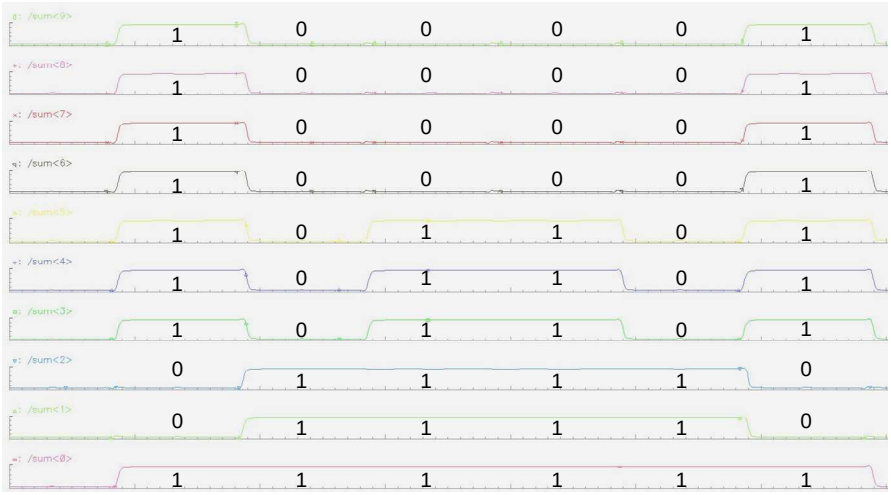


Figure 3-43: Impulse response simulated in Cadence for 1 FIR at 5 GHz

Matlab	-7.8 7.8 63 63 7.8 -7.8
VHDL	-7 7 63 63 7 -7
Ultrasim	-7 7 63 63 7 -7

Table 3-5 : Impulse response of a filter at 5 GHz Matlab vs VHDL vs Ultrasim

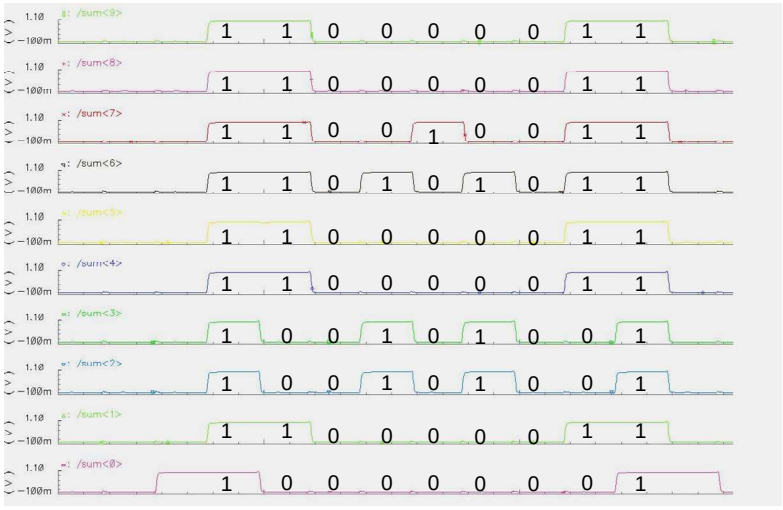


Figure 3-44: Impulse response simulated in Cadence for 2 FIR at 5 GHz

Matlab	0.875 -1.75 -14 0 76.125 129.5 76.1250 -14 -1.75 0.875
VHDL	1 -1 -14 0 76 128 76 0 -14 -1 1
Ultrasim	1 -1 -14 0 76 128 76 0 -14 -1 1

Table 3-6 : Impulse response of the two filters at 5 GHz Matlab vs VHDL vs Ultrasim

3.4.2. 10 GHz filter transistor level design

3.4.2.1. 10 GHz basic filter cell

The same methodology is used for the 10 GHz filter. A basic cell is designed and reused. The major differences compared to the 5 GHz filter are the number of coefficients and the pipeline depth. A pipeline of one is used for the 10 GHz filter.

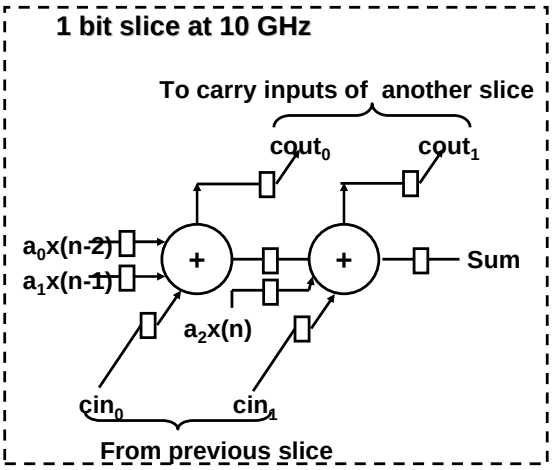


Figure 3-45: Transistor level of the basic cell for the 10 GHz filter

3.4.2.2. 10 GHz complete structure

For the first filter at 10 GHz, 11 cells are assembled and for the second filter, 12 cells are assembled. As previously shown, the 100 ps period can't be achieved in post layout simulation. In schematic simulation the 100 ps critical part can be achieved in a typical corner, at 27°C, loaded by flip-flops, on a supply voltage of 1.1V.

The impulse response is still used to simulate the behaviour of the filter. Impulse response for one filter at 10 GHz and two filters at 10 GHz is provided. The impulse is 63 (0111111b).

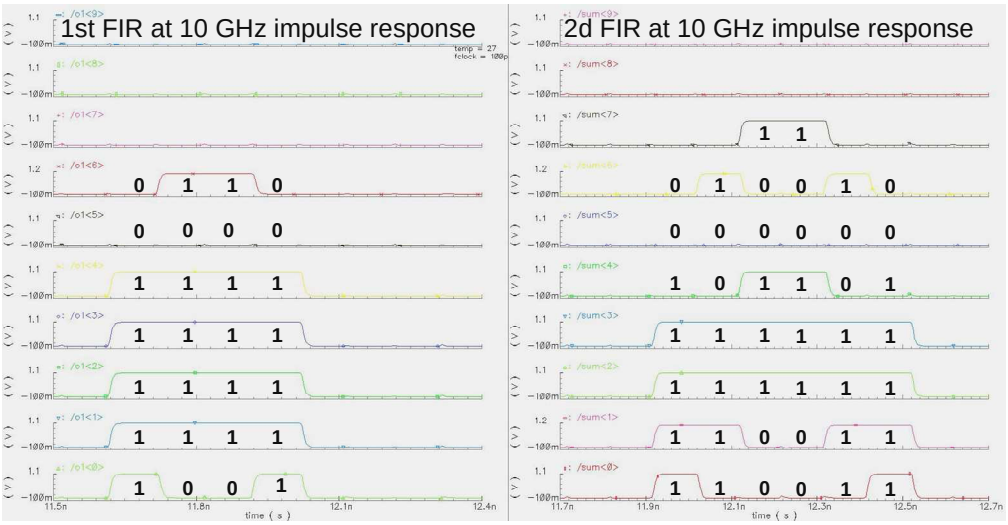


Figure 3-46: Impulse response simulated in Cadence for 1 and 2 FIR at 10 GHz

The impulse is sampled two times and the results are:

Matlab	31.5 94.5 94.5 31.5
VHDL	31 94 94 31
Ultrasim	31 94 94 31

Table 3-7 : Impulse response of one filter at 10 GHz Matlab vs VHDL vs Ultrasim

Matlab	15.75 78.75 157.5 157.5 78.75 15.75
VHDL	16 79 156 156 79 16
Ultrasim	16 79 156 156 79 16

Table 3-8 : Impulse response of two filters at 10 GHz Matlab vs VHDL vs Ultrasim

3.4.3. Clock tree design

The clock tree distribution problem is a trade-off between different parameters:

1) Large Chip Area
2) Non-uniform distribution of the flip-flops
3) All flip-flops need to get clock signals at the same time
4) Power budget
5) Clock routing

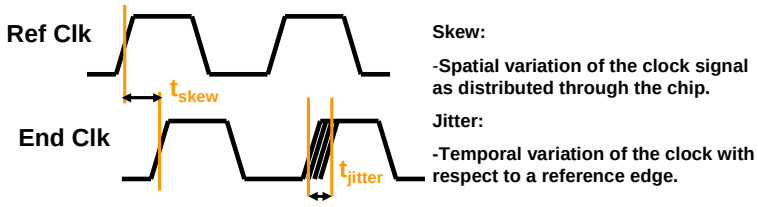


Figure 3-47: Skew and jitter definition

3.4.3.1. Review of some trees

Considering the high frequency targeted the choice of the clock tree is important. Obviously in this work the skew has to be reduced close to zero. Different architectures exist and are depicted in Figure 3-48.

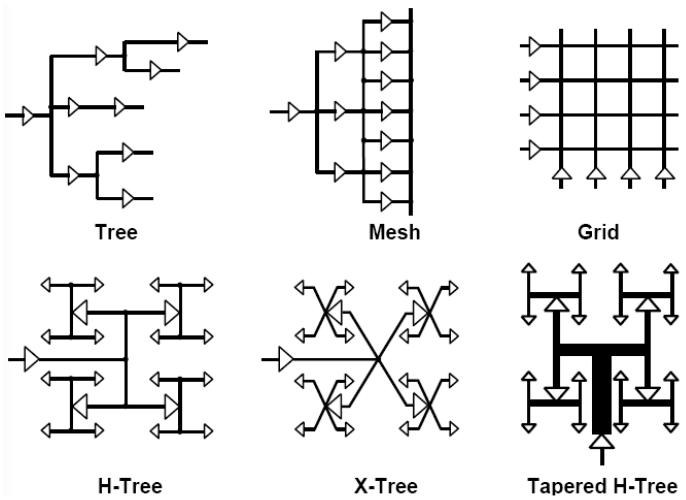


Figure 3-48: Clock tree architectures

1) The tree is the most common and general approach to clock distribution. It leads to an asymmetric structure and all paths must be balanced.

2) The buffered clock tree forms an n-ary tree. Buffers are inserted either at the clock source and/or along a clock path, forming a tree structure. Buffers have two functions: amplify the clock signals degraded by the distributed interconnect impedances and isolate the local clock nets from upstream load impedance.

3) The mesh is a hybrid buffered clock tree. Shunt paths further down the clock distribution network are placed to minimize the interconnect resistance within the clock tree. Skew can be close to zero.

4) A grid is realized with two kinds of metals and buffers are placed to drive in 2D the flip-flops. With the grid clock tree low skew is achievable. This structure suffers from a lot of excess interconnect and a large power dissipation.

5) H Tree is a solution to decrease skew while assuming a symmetric structure.

6) X Tree is a variant of H tree.

7) The tapered H-Tree is a variant of the H tree. The metal widths in H-tree structures are designed to progressively decrease as the signal propagates to lower levels of the hierarchy. This strategy minimizes reflections of the high-speed clock signals at the branching points.

3.4.3.2. Chosen clock tree

For our application the chosen architecture is a hybrid structure. The hybrid structure is the combination of the mesh structure and the grid structure in order to target a very low skew. The main drawback of these two architectures is the high power consumption. The chosen hybrid structure is depicted in Figure 3-49:

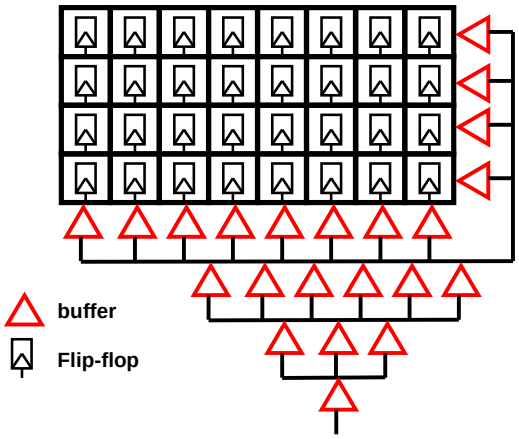


Figure 3-49: Hybrid clock tree – mesh and grid

3.4.3.3. 5 GHz and 10 GHz clock tree design

The design procedure is the same at 5 GHz and 10 GHz and can be summarized in the following points:

1. All nodes have capacitance and all branches have resistance
2. Fix the load (fan out) of each buffer
3. Compute the number of levels required
4. Position the buffers optimally (physical level)

One point to take care of is that all buffers must be balanced in order to keep a duty cycle as close as possible to 50%. Buffers have been designed by hand.

3.5. PHYSICAL LAYOUT LEVEL

In this section the physical layout of the interpolator is presented, starting from the basic slice up-to the global structure.

The technology used is a 65nm CMOS from STMicroelectronics with 7 metals layer (two upper levels are thick metal levels).

The physical layout of the interpolator must be separated in two parts: the 5 GHz filter and the 10 GHz filter. The same idea is used in the two cases: first layout and optimized a basic cell (bit slice) and then repeat it. For both filters the critical signal to drive is the carry. Physical layouts are shifted forward from slice to slice, thus direct carry connection from one block to the following are routed straight ahead. Internal bit slice connections are in metal 2 and metal 3. Carries are stacked metal 3 and metal 4. While the global capacitance is a little bit increased, the global resistance is decreased. The RC product is thus decreased and delay optimized for the carry signal.

For the clock signal metal 4 and 5 are used. The hybrid clock tree is based on a grid. Vertical connections are in metal 4 and horizontal connections in metal 5.

Metal six is used for VDD and metal seven for GND.

3.5.1. 5 GHz filter physical layout

First the basic 2 bits slice is realized (Figure 3-50). Long paths inherent to the physical layout have been taken into account in the physical design by introducing flip-flops at the beginning of each bit slice. Thus a flip-flop in the pipeline structure must drive only flip-flops and metal lines instead of long wires plus adder inputs.

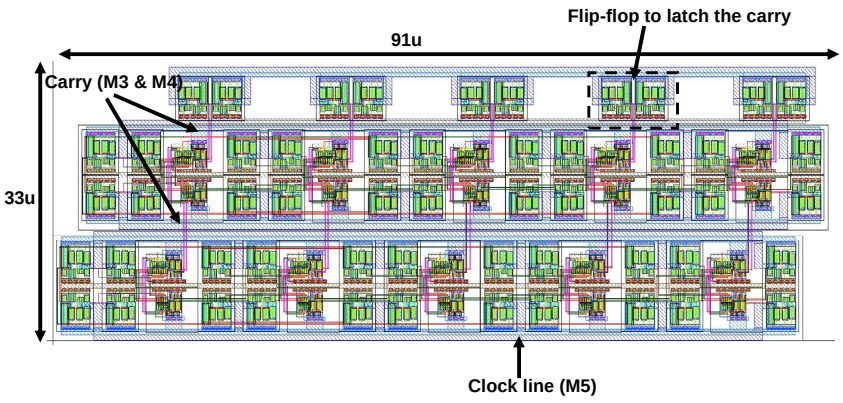


Figure 3-50: Layout of a basic cell at 5 GHz (2 stages)

The complete FIR filter at 5 GHz is composed of 5 times the basic cell and depicted in Figure 3-51.

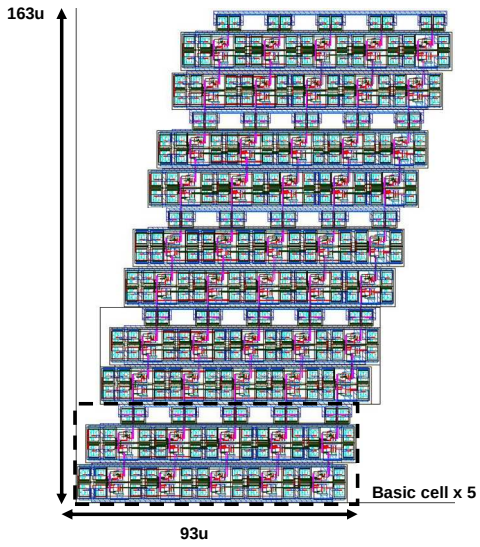


Figure 3-51: Layout of one FIR at 5 GHz

Assembly of the two 5 GHz filters is shown in Figure 3-52

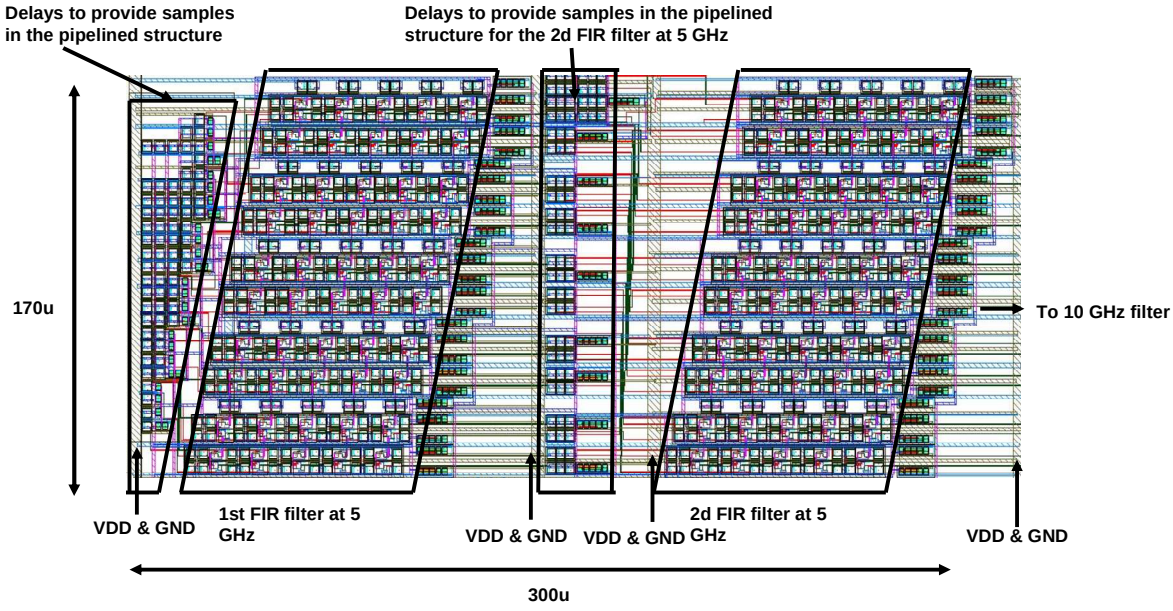


Figure 3-52: Layout of the complete FIR at 5 GHz

Large VDD and GND (12um) wires are routed in the structure to supply the different stages.

3.5.2. 10 GHz filter physical layout

For the 10 GHz the elementary structure is a 1 bit slice..

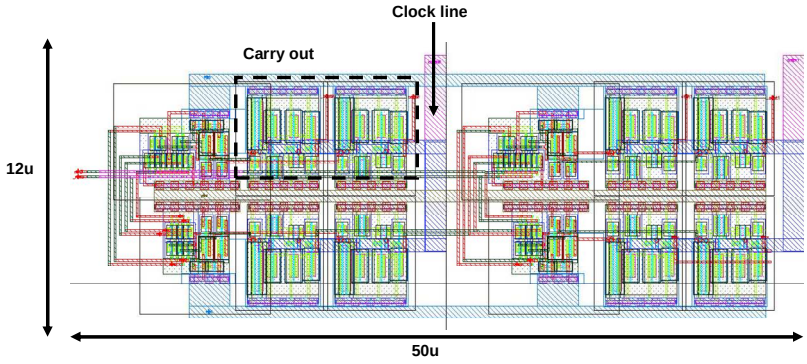


Figure 3-53: Layout of a basic cell at 10 GHz (1 stage)

The complete structure of one FIR filter at 10 GHz is depicted in Figure 3-54

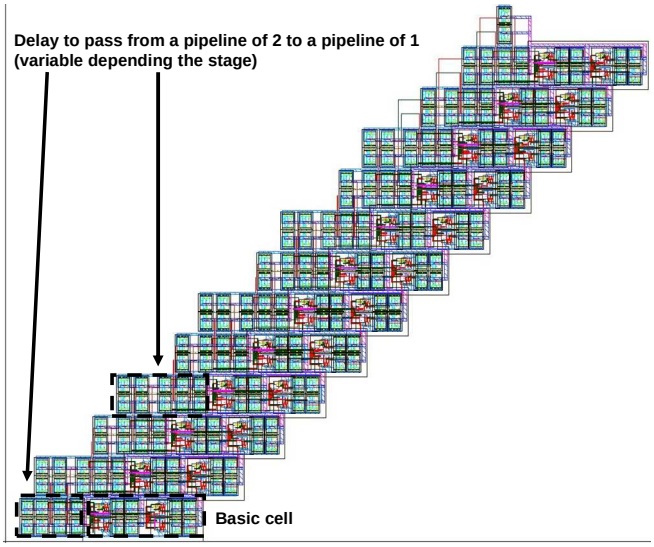


Figure 3-54: Layout of one FIR at 10 GHz

Finally the global structure is depicted in Figure 3-55

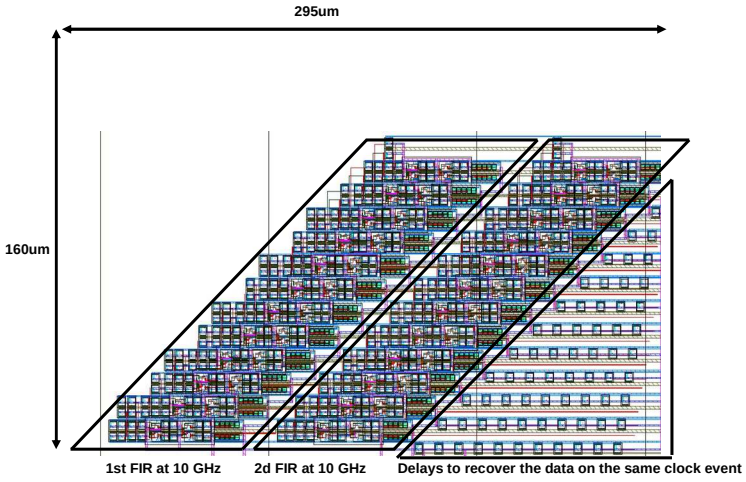


Figure 3-55: Layout of the complete FIR at 10 GHz

3.5.3. Clock tree physical layout

For the clock signal metals 4 and 5 are used. The hybrid clock tree is based on a grid. Metal 4 realized the vertical part of the grid and metal 5 realized the horizontal part of the grid.

Buffers are inserted along the right vertical grid and along the horizontal grid (Figure 3-49). This topology can avoid setup violations as the clock “flow” goes from right to left while the data “flow” goes from left to right.

In the clock tree another point to take care of is it the use of TSPC flip-flops in the interpolator. The point inherent of TSPC flip-flops is the steepness of the clock edge. To solve this problem the last stage buffers are inserted as close as possible to the TSPC flip-flops and a maximum of 12 TSPCFF are driven by a single buffer stage.

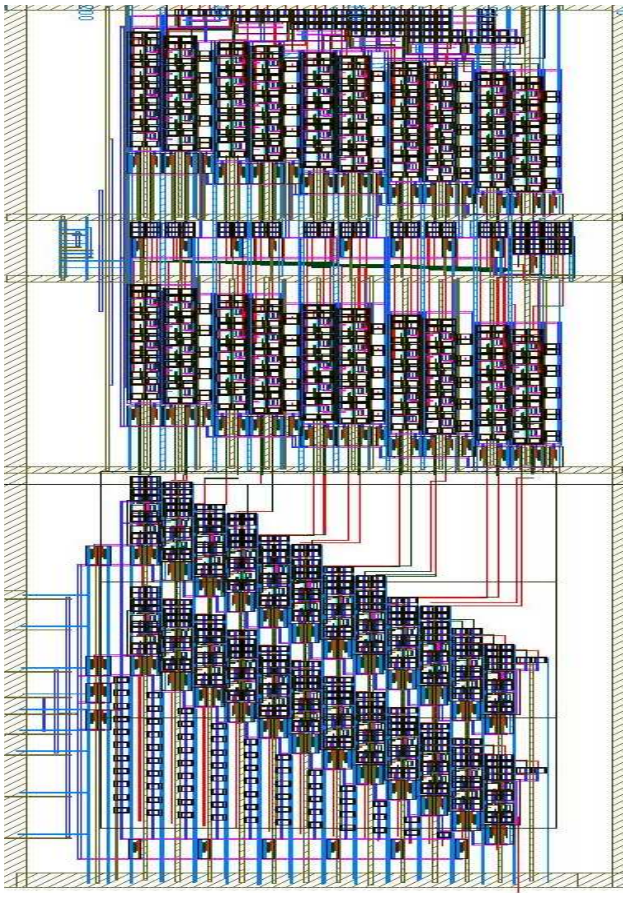


Figure 3-56: Layout of the interpolator (5 GHz & 10 GHz)

The core area is 650 x 170 um^2

3.6. GLOBAL SIMULATION

The global structure has been simulated in order to verify the transfer function (compared to the VHDL) and the timing. Simulations are also performed to see what the expected performances are, i.e.: find the maximum working frequency for a supply voltage. Supply voltage goes from 0.6V to 1.3V. Temperature is set to 27°C.

Supply Voltage [V]	Working Frequency [GHz]	Current consumption [mA]
0,6	2,5	30
0,7	3,5	50
0,8	5,128	83
0,825	5,5	94
0,85	5,7	100
0,9	6,3	122
0,95	7	139
1	7,8	163
1,05	8,4	190
1,11	8,849	217
1,13	9	240
1,19	9,5	265
1,22	9,8	281
1,3	10	307

Table 3-9 : Performance expected

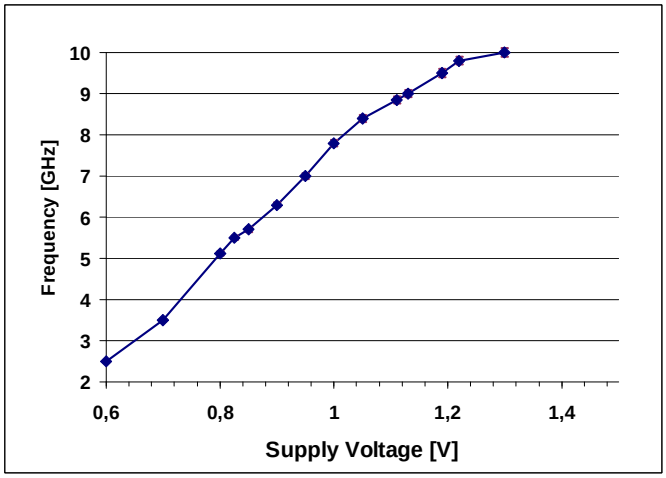


Figure 3-57: Frequency VS supply voltage

The characteristic tends to follow a linear law from 0.8 V to 1.2V considering an error of 5% for each value (see Figure 3-58)

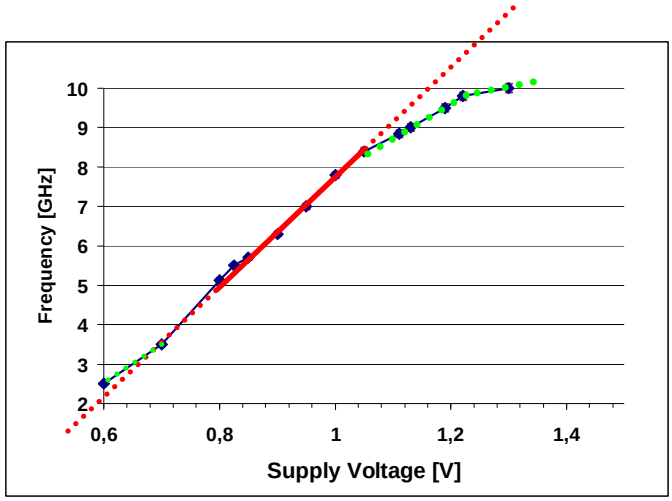


Figure 3-58 : Linear characteristic of the working frequency with a 5% error vs the supply voltage

Under 0.8V, a saturation tends to appear in the sense that as the supply decreases the CPL logic has more and more problems to regenerate the level and thus the maximum working frequency tends to “saturate”.

Above 1.1 V different problems appear. First the GP transistors are normally supplied with a tolerated nominal supply voltage of ±10%. The model of the GP transistors is valid from 0.9V to 1.1V.

The other point that can explain this saturation is the transconductance of the transistor. With the increase of the supply voltage, the V_{GS} also increases. At a certain point the current does not increase linearly with an increase of the V_{GS}.

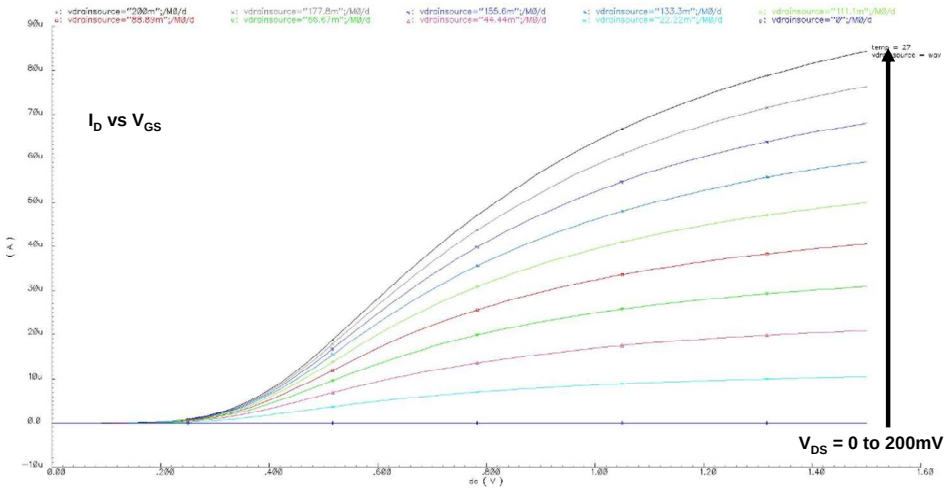


Figure 3-59: Parametric simulation I_D vs V_{GS} (V_{DS}=0 to 200mV)

This effect can be explained by the mobility reduction with the increase of the vertical electrical field. The mobility tends to decrease starting from a critical value of the electrical field.

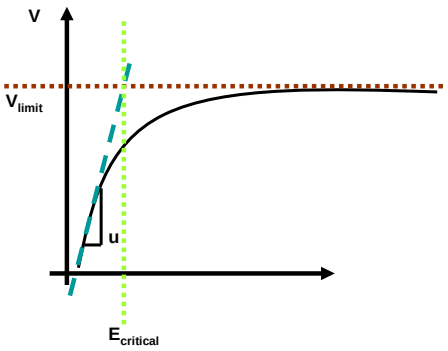


Figure 3-60: Speed of the carriers vs electrical field

Simulation of Figure 3-61 has been realized in a typical corner, at 27°C, with a clock period of 102 ps, on a 1.22V supply voltage. The impulse response is given in Table 3-10: For the extraction, considering the number of transistors, a global extract is not feasible. A solution to simulate the extracted view is to use the Ultrasim simulator with a hierarchical view (e.g.: extracted slices can be used with mixed-signal precision)

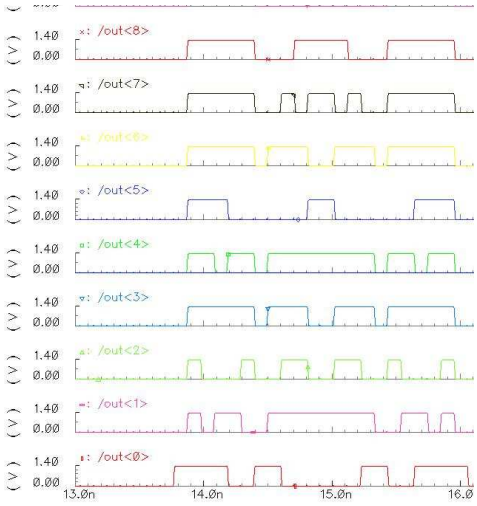


Figure 3-61: Simulation of the global structure at a schematic level with Fs=102 ps.

Matlab (fix)	0 -7 -23 -39 -37 0 92 224 354 440 440 354 224 92 0 -37 -39 -23 -7 0
VHDL	1 -7 -21 -38 -36 1 91 222 350 434 434 350 222 91 1 -36 -38 -21 -7 1
Ultrasim	1 -7 -21 -38 -36 1 91 222 350 434 434 350 222 91 1 -36 -38 -21 -7 1

Table 3-10 : Impulse response of the interpolator Matlab vs VHDL vs Ultrasim

3.7. CONCLUSION

The design of the interpolator has been presented. In order to achieve GS/s output samples, different high speed architectures have been introduced, starting at a system level with the choice of the transposed architecture with pipeline ripple carry adders, going into the design and physical layout of fast adders, fast flip-flops and low skew clock trees. Finally a global simulation of the interpolator for different supply voltage depicts in Figure 3-57 is presented.

The physical layout of the core has been presented. The core has been developed in STMicroelectronics CMOS 65nm technology. The core area is 650 x 166 um^2 and can achieve 10 GS/s with a supply voltage of 1.3 V. The power consumption expected at this frequency is 324 mA.

Implementation with CPL basically doubles the number of flip-flops and thus doubles the power consumption. Moreover to target the 10 GS/s output, a fine pipeline has been used. At the moment, the switching speed is the priority and theses choices validate specifically this priority. In a near future the access to a more advanced technology node, such the CMOS 32nm and further, will reduce the design complexity and the power consumption by using a non-differential logic style and a different pipeline depth.

Current consumption estimated	
CPL adder consumption (1V)	48 uA
TSPCFF consumption (1V)	59 uA
Interpolator (1.3V – 10 GHz)	324mA
Area	
Carry CPL area	4.7 x 3.8 um^2
Sum CPL area	4 x 4 um^2
TSPCFF area	5.4 x 4.5 um^2
5 GS/s slice area	91 x 13 um^2
10 GS/s slice area	50 x 12 um^2
5 GS/s FIR filter area	300 x 170 um^2
10 GS/s FIR filter area	295 x 170 um^2
Interpolator area	650 x 170 um^2

Table 3-11 : Summary of performances

4. CHAPTER
TEST METHODOLOGY AND MEASUREMENTS

"A person who never made a mistake never tried anything new."

Albert Einstein

This chapter presents the methodology that has been used to test the chip. The main problem is how to send data at a sample rate of 2.5 GS/s and get the interpolator temporal response at a sample rate of 10 GS/s.

Two solutions are presented. 1) The first one proposed was to use a 7 bits ADC at 2.5 GS/s to convert analog OFDM symbols into digital symbols that are fed into the interpolator. The interpolator outputs are converted with a 7 bits DAC at 10 GS/s. DAC output is checked with a spectrum analyser. This solution needs an analog OFDM generator, one ADC at 2.5 GS/s with an ENOB of 7 bits and one DAC at 10 GS/s with an ENOB of 7 bits. 2) The second solution proposed was to use memories in order to program test patterns that are fed at 2.5 GS/s into the interpolator and to read the interpolator time response to these patterns. A serial interface can be used to program input memory and read output memory at low speed (~KHz). A serializer is used to send data a low speed data rate (input memory) to a high speed data rate fed into the interpolator. A deserializer is used to send data from a high speed data rate (output of the interpolator) to a low speed data rate (write output memory).

Measurements have been performed. The circuit is able to operate at sampling frequencies of up to 9.6 GS/s. At 9.6 GS/s, the power consumption is 285mA on a 1.4V power supply.

4.1. TEST METHODOLOGY

This chapter presents the different test methodologies to test the high speed digital interpolator presented in the previous chapter. The main constraint is the speed. The question is how to provide 7 bits at 2.5 GS/s (input of the interpolator) and get 7 bits at 10 GS/s (output of the interpolator) and what are the measurements to realize (digital characterisation, output spectrum, etc.)? In order to answer this question two solutions are presented with different levels of difficulties.

4.1.1. ADC – Interpolator – DAC solution

The first solution proposed is to prove the functionality of the interpolator while verifying the output spectrum (image attenuation) for different input signals .The input signals can be sine waves at different frequencies (frequency characterization of the interpolator) or directly an OFDM signal (frequency characterization of the interpolator and characterization of other parameters such EVM, SNR,…).

A global schematic is depicted in Figure 4-1.

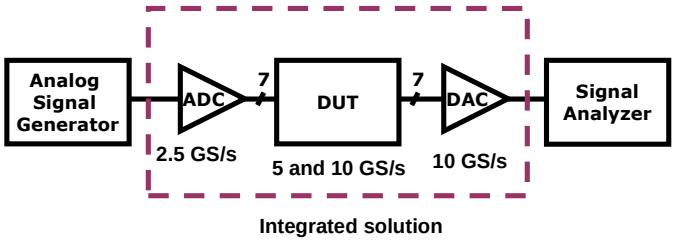


Figure 4-1: ADC - interpolator - DAC integrated test solution

The solution proposed in Figure 4-1 needs one ADC at 1.25 GS/s and one DAC at 10 GS/s. At this point both components have not been designed. The solution is to find these components as discrete blocks or on-chip blocks (Figure 4-2).

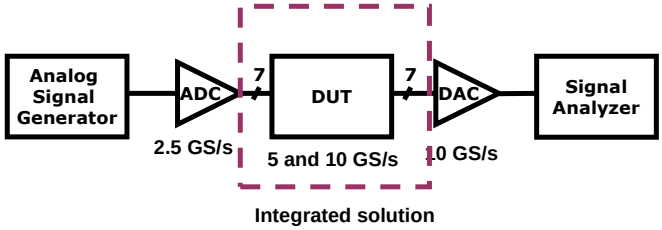


Figure 4-2 : ADC – interpolator – DAC with discrete components solution

4.1.1.1. ADCs or digital generator

a. ADC

E2V company proposes different solutions for high speed ADCs. Here is a summary of different ADCs able to satisfy the specifications (7 bits at 2.5 GS/s). The cost for one ADC is 100 dollars.

E2V solution EV10AS150
Fin : 2495 MHz / 8.3 bit (enob) @ 2.5 Gsps
Full scale analog input 500mVpp 100ohm differential
100 ohms differential clock input
Differential digital outputs, LVDS
EBGA (Enhanced Ball Grid Array)

Table 4-1: EV10AS150

E2V solution EV10AQ190
Fin : 1.2 GHz / 7.2 bit (enob) @ 2.5 GS/s
Full scale analog input 500mVpp 100ohm differential
2.5 GHz differential clock input
LVDS output format
EBGA (Enhanced Ball Grid Array)

Table 4-2: EV10AQ190

The basic architecture of the ADCs is depicted in Figure 4-3.

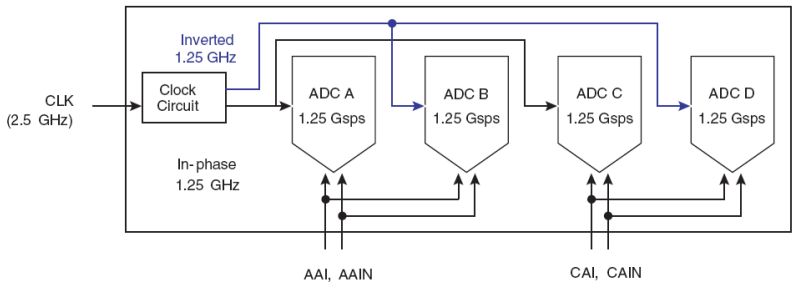


Figure 4-3 : ADC architecture

The architecture is able to provide an output up-to 5 GS/s while multiplexing the output of 4 ADCs at 1.25 GS/s. Here a 2.5 GS/s must be provided, meaning that 2 ADCs must be used. The output of the two ADCs will be interleaved on-chip. The package provided is EBGA (enhanced ball grid array) and it is composed of 380 pins.

At this time on-chip ADCs with the required sampling frequency and linearity were not available.

b. *Digital signal generator*

The ADC can be replaced by a digital signal generator that generates at 2.5 GS/s the different test patterns on 7 bits. The Tektronix DTG5334 is able to generate bits at this frequency.

Figure 4-4 : Digital data generator

The data generator is composed of a module (2 bits) that generates digital data up-to 3.35 Gb/s (DTGM30 module). Other modules can be inserted. The fact it is that a module costs 15000 dollars, which means that to generate the other 5 bits, 3 modules must be bought. It is an expensive solution. Moreover this solution needs to deal with a lot of cables and differential signals, which means that 14 pads must be provided to get the signal at 2.5 GS/s.

c. *DAC*

The maxtek advanced data converter module can be used. Designed in an IBM 180 nm Silicon Germanium (SiGe) BiCMOS process, this component enables high speed digital-to-analog conversion up-to 12.5 GS/s with 10 bits linearity. The basic architecture is depicted in Figure 4-5.

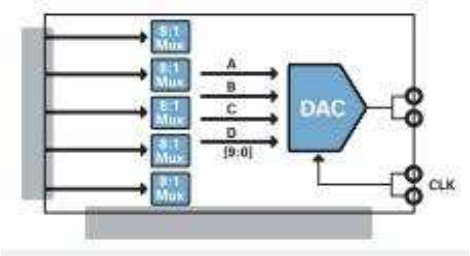


Figure 4-5 : DAC architecture

No others informations are provided on this component by the supplier. This was the only discrete DAC that was available and that was able to answer to the problematic.

No ip blocks were available with the required performances.

4.1.1.2. Conclusion

In the case of the solution with ADC: use discrete components to realize the test function is complex. First not all the components are available or not well described and their prices are expensive. This solution will lead to the design of a complex board where analog signal at 2.5 GS/s must be routed inside the chip and analog signal at 10 GS/s must be routed outside the chip. In the case of on-chip solutions it would have required a full custom design of ADCs and DACs.

In the case of the solution with the data signal generator, the routing overhead becomes important. It simplifies the design in one way but the price of components (modules) is still too high.

4.1.2. Memories – SerDes – serial interface

A solution to simplify the board designs and reduce the cost is to use a test system with input and output memories that can be written and read at low speed. In order to provide input data at a high speed to the interpolator and get the output data at a high speed from the interpolator, a serializer and a deserializer are used. The input and output memory can be synthesized from a VHDL RTL code but considering the high speed of the core the serializer and deserializer are custom designs and layouts.

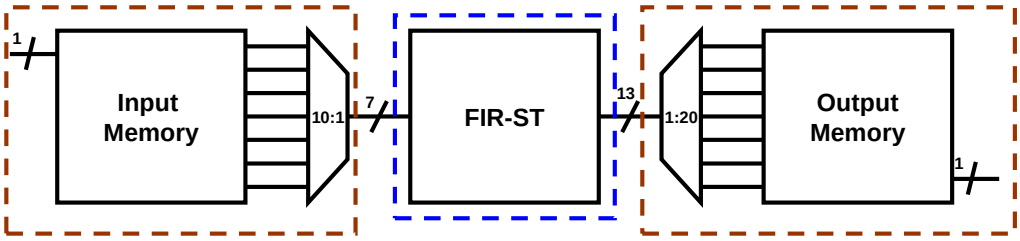


Figure 4-6 : Input/output memory test architecture

Each block will be studied in this section.

4.1.2.1. Input memory and serializer

The input memory is realized with flip-flops as a shift register. The size of the input memory is complex to define. First of all one must keep in mind that the output memory will be 2 times bigger than the input memory because of the oversampling ratio between

the input and the output. A symbol OFDM is composed of 512 (+ 64 cyclic prefix) points represented on 7 bits. This represents 3.5 K of memory. This is feasible but the output memory will represent 7 K of memory. The test structure will be bigger than the core itself and considering the price of the silicon area with a 65nm technology this is not a valuable solution. In order to test the core while keeping the input memory, the size of the input memory must be reduced. The core can be test with different kind of patterns (impulse response, step response, sine wave at different frequencies, random numbers …) and 1 K of memory will be sufficient.

The serializer serializes 10 bits in parallel at 500 MS/s to 1 bit stream at 5 GS/s. Recall that memories are synthesized blocks, 500 MHz is an achievable working frequency in a 65nm technology. The input memory is thus composed of 70 outputs (10 bits * 7 inputs) and to achieve the one 1 K memory the length of the memory is set to 15. The input memory is thus composed of 70 lines of 15 flip-flops.

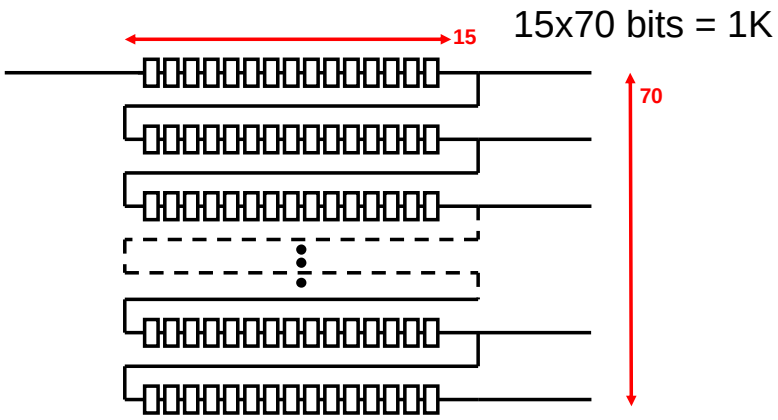


Figure 4-7 : input memory architecture

The input memory is connected to the serializer as shown in Figure 4-8

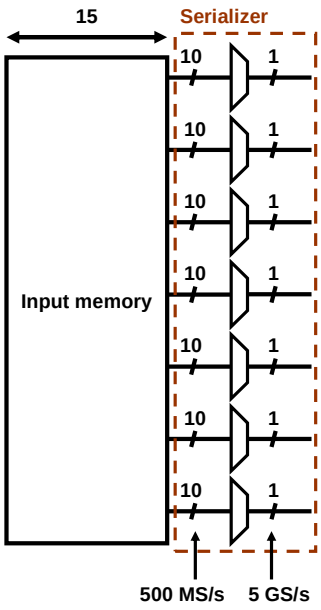


Figure 4-8 : input memory and serializer

It has been mentioned that the input memory architecture can be seen as a shift register. This means that the input memory is programmed (written) with 1 bit but read in parallel at the speed defined by the frequency ration between the serializer and memory working frequency. To simplify the board design the memory is programmed at a very low rate (KHz) and read at 500 MHz. The logic control to write/read the input memory will be presented later.

The serializer is a custom design. It accepts 10 bits at 500 MS/s and serializes them to a 1 bit stream at 5 GS/s. The internal structure is illustrated in Figure 4-9.

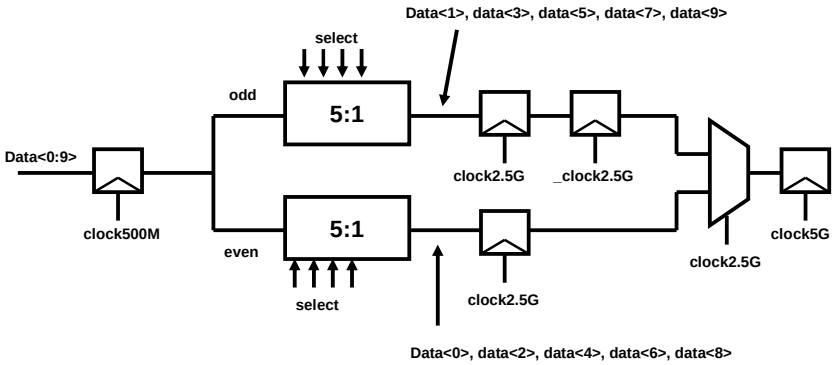


Figure 4-9 : One serializer 10 :1 architecture

The 10 bits are separated in odd and even data. The 5 odd bits at 500 MS/s are serialized to 1 bit stream at 2.5 GS/s and resynchronize by a 2.5 GHz clock. Finally a multiplexer serializes the two streams at 2.5 GS/s to one stream at 5 GS/s and resynchronizes them on the 5 GHz clock.

The 5:1 serializer is realised as depicted in Figure 4-10. The sel1, sel2, sel3 and sel4 signals are generated from the state machine that realized the division of the 5 GHz clock by 10.

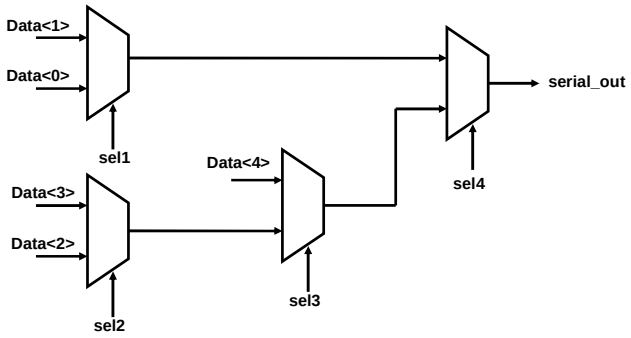


Figure 4-10: 5:1 serializer architecture

4.1.2.2. Output memory and deserializer

The same architecture can be implemented at the output. In order to verify the core function all the bits (12 bits output of the FIR4 at 10 GHz + 1 bit carry out) are written in the output memory. The scheme is the same but at the opposite a deserializer is used. From 1 bit at 10 GS/s, 20 bits are written in the output memory. The reason why now 1 bit is deserialize into 20 bits at 500 MS/s comes from the up-sampling ratio. At 10 GHz, if one wants to use the same 500 MHz clock, a division by 20 must be realized. Thus the same 500 MHz clock can be used for the serializer and deserializer.

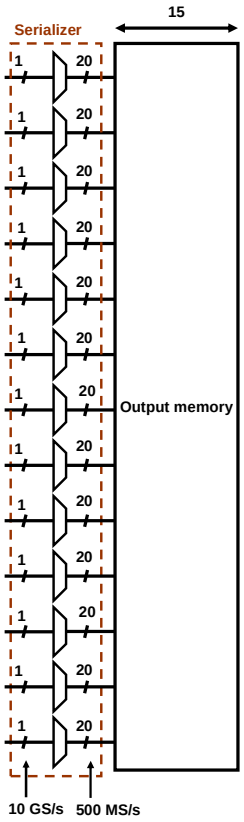


Figure 4-11 : output memory and serializer

The output memory is composed of 260 inputs (20 outputs * 13 bits) and the length of the memory is 15. The memory architecture is still a shift register. Data are written into the output memory at 500 MHz in parallel and read in series at ~KHz. The control logic will be presented later.

The deserializer takes 1 input at 10 GS/s and deserializes it to 20 bits at 500 MS/s. No clock division is realized in the deserializer. The 500 MHz clock provided to the deserializer is the same as the one in the serializer. As this clock is provided by the division

of the reference clock and synchronize by this latter, no synchronization problems can appear between the interpolator and deserializer.

The internal architecture of the deserializer is depicted in Figure 4-12.

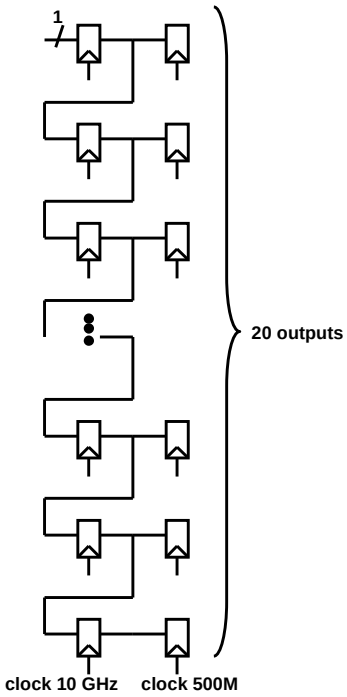


Figure 4-12: 1 :20 deserializer architecture

4.1.2.3. Serial interface and control logic

As mentioned previously the input memory and output memory are written and read at different frequencies. A serial interface has been designed in VHDL and synthesized to write the input memory and read the input memory. Control logic (state machine) manages the data path to change the clock and read and write signals.

a. Input memory controller

3 signals must be generated off chip to program the input memory. The 3 signals are an enable signal (enable), clock signal (clock_low) and the data (input).

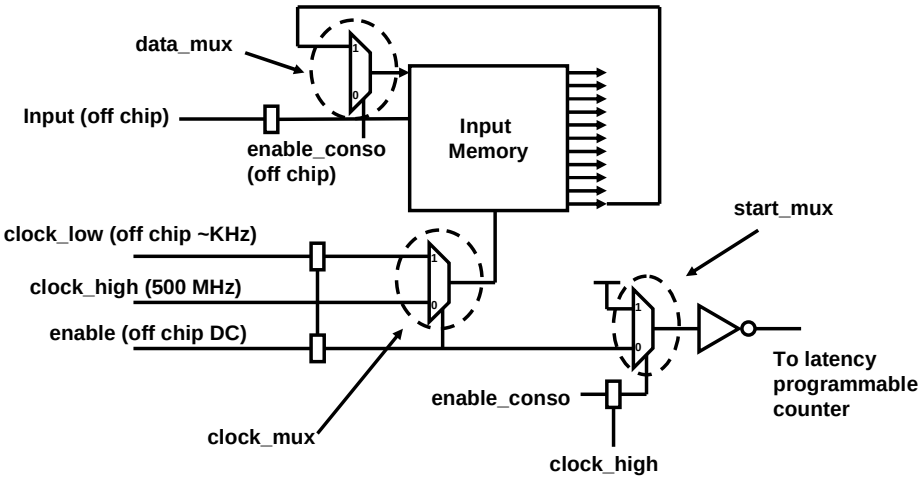


Figure 4-13 : input memory controler

As shown in Figure 4-13 depending on enable (0 or 1) the clock_mux lets pass clock_low or clock_high. This clock_mux is necessary to write the memory at a low speed (~KHz) and read it at full speed (500 MHz) in other words when enable is high the memory is set in the write mode and when enable is low the memory is set in the read mode.

The timing diagram below (Figure 4-14) shows how to program the input memory

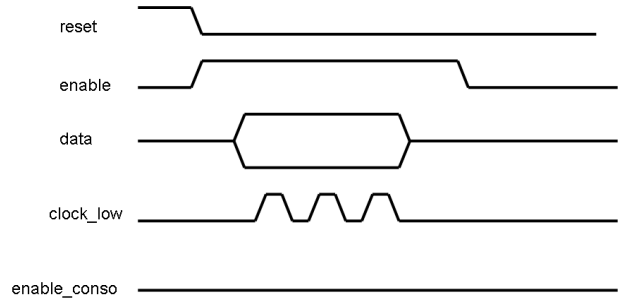


Figure 4-14 : Timing diagram to program the input memory

1050 clock events are generated and for each clock event a data is generated. 1050 corresponds to the depth of the input memory. Once enable goes low, the clock changes and data are read in parallel at 500 MHz.

Two other mux are used. The first one, data_mux, allows reading continuously the memory, this is mandatory to measure the power consumption. The second is the start_mux. When enable goes from high to low, this mux sends a bit start to another block, the latency counter. This block is explained in the next section.

The content of the input memory can be output. This possibility is to verify that the memory has been correctly programmed.

b. *Latency counter*

The latency counter is started with a start bit generated in the input memory controller. This start bit starts the counter (3 bits counter). The working frequency is 500 MHz.

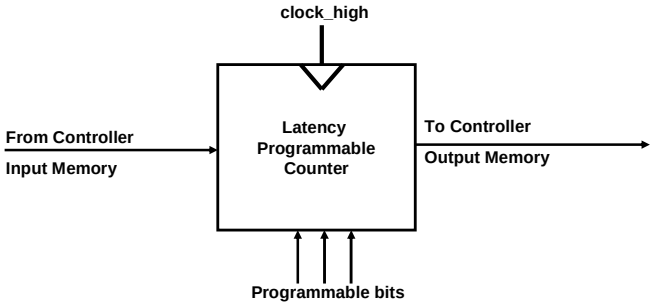


Figure 4-15 : Latency counter

This counter is used to compute the latency between the serializer – the interpolator – and the deserializer. It is necessary to recover the data after the deserializer with a programmable time frame. Another start bit is generated once the counter has finished counting in order to start the writing process inside the output memory.

c. *Output memory and output memory controller*

As mentioned previously the output memory is two times bigger than the input memory because of the oversampling ratio. The output memory must also be written and read at different speeds like the input memory. In the write mode, the data comes from the deserializer and must be written in parallel at 500 MHz. In the read mode, the data must be sent in series to the output. The output memory is illustrated in Figure 4-16.

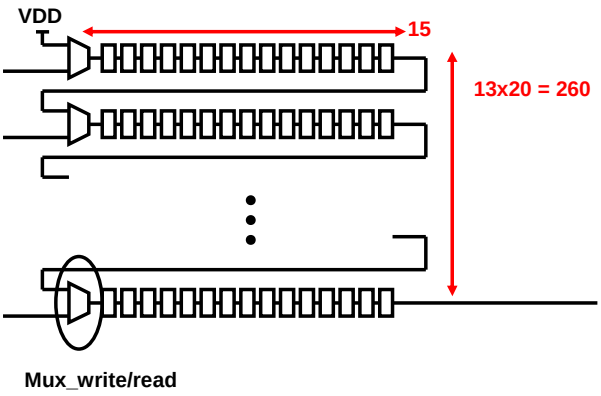


Figure 4-16 : Output memory

When mux_write/read is set to one the data can be written in parallel in the memory. When the mux is set to zero, the data are read in series.

The controller of the output memory is depicted in Figure 4-17.

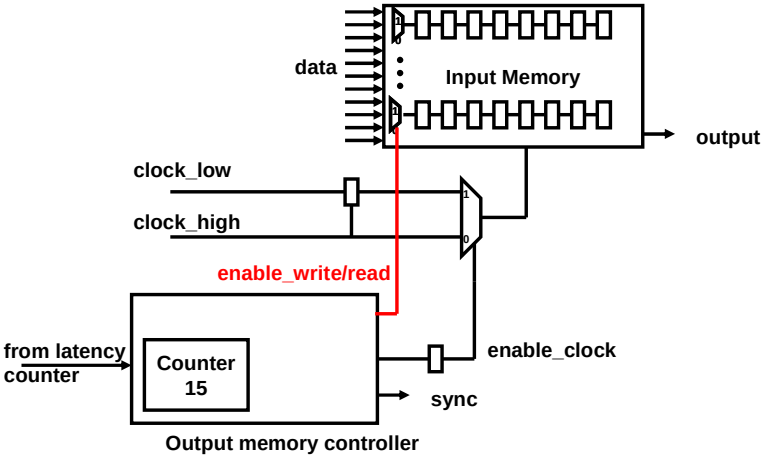


Figure 4-17 : Output memory controler

The controller is basically a counter. The latency counter gives a start signal to the output controller. When the output controller receives the start signal it puts the memory in the write mode (enable_write/read = '1' and enable_clock ='0'). In other words, the clock is the 500 MHz clock and data are written in parallel. Exactly 15 values are written in the output memory. Basically a counter counts to 15 while enabling 15 clock_high events. After the 15th clock_high event's, the output controller change the state from write to read and generates also a sync_signal (data ready to be read). In other words, clock_low is used and data are read in series.

d. Complete structure

The complete synthesised test structure is depicted in Figure 4-18. All the structure can be reset.

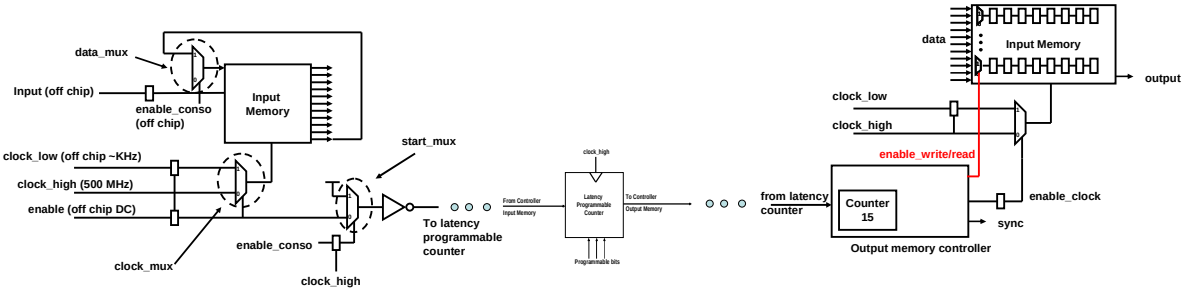


Figure 4-18 : Synthesized test structure

The integration of this test structure with the serializer/deserializer and the device under test is depicted in Figure 4-19

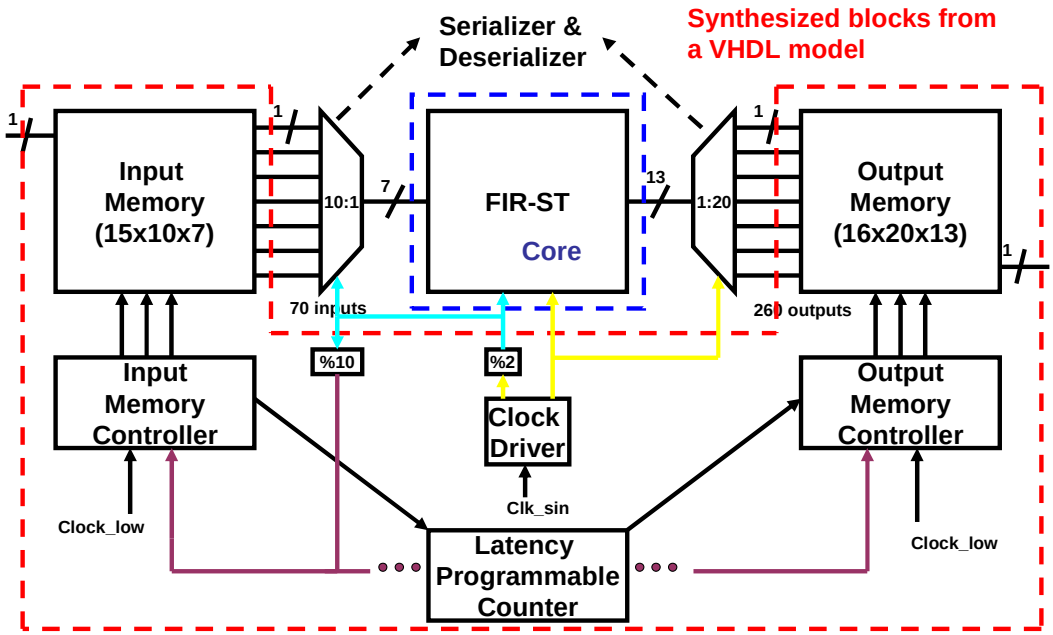


Figure 4-19: Global test structure

4.2. FIRST

In this section FIRST is presented. FIRST is a prototype designed in STMicroelectronics 65nm CMOS process. Its size is around 1500 x 900 um^2 and counts 48 pads.

4.2.1. FIRST Layout

FIRST is composed of the interpolator (core) and the test part presented in the previous section. A 1.5 nF decoupling capacitance has been integrated in order to reduce the ringing on the supply voltage. Transistors that composed FIRST are global purpose transistors with a nominal supply voltage of 1V. STMicroelectronics does not provide I/Os with GP option, thus the pads have been custom designed.

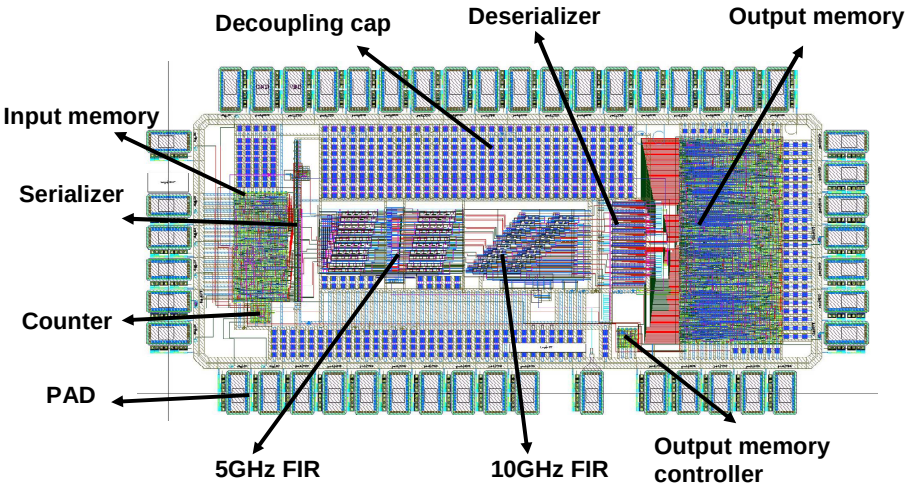


Figure 4-20 : FIRST physical layout

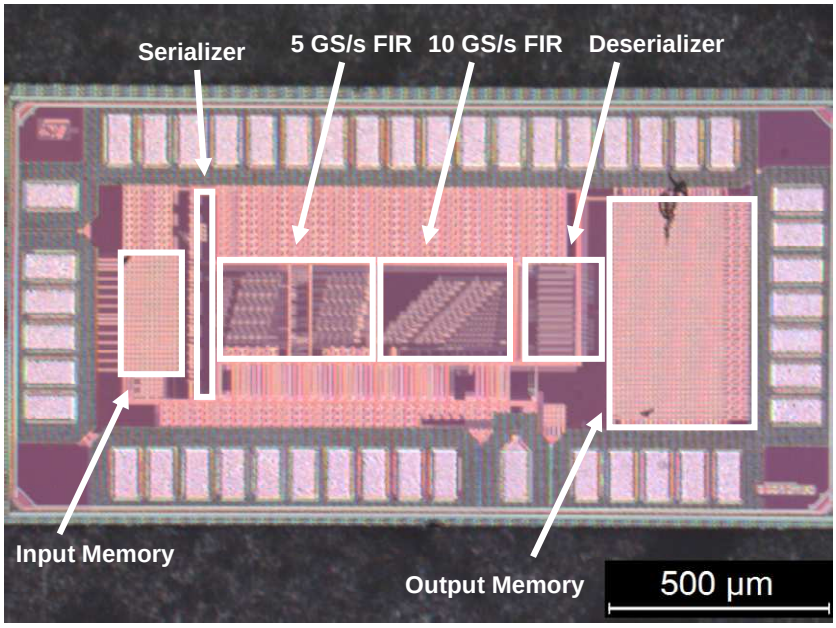


Figure 4-21: FIRST fabricated prototype

The layout is shown in Figure 4-20, the fabricated prototype in Figure 4-21 and is pad ring is composed as follow (Figure 4-22):

1) Top pads are supplies (VDD & GND) and one pad is used for the input data.

2) Right pads contain the output memory pad, the sync signal pad and supplies.

3) Bottom is composed of 2 configuration bits pad (for the counter), supplies and the high speed clock pad (10 GHz).

4) Left pads contain most of the signal pads (reset, enable, clock_low, enable_conso, out_memory and bit0).

The unused pads on the top and bottom are filled with GND/VDD

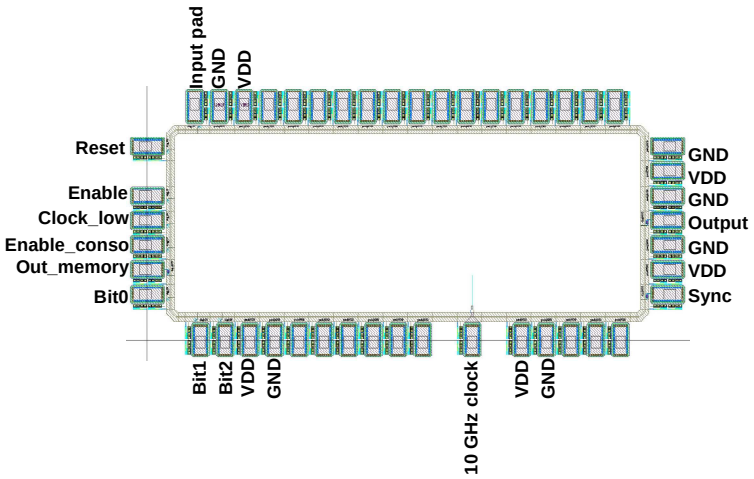


Figure 4-22: Pads ring

Considering the number of pads and the low complexity of the signal to generate, a chip on board solution is taken.

4.3. FIRST – MEASUREMENTS

In this section the results of FIRST are presented. In a first time the hardware used for the measurements will be described. A first prototype has been realized and measured. Because of a process error this first prototype did not give any relevant measurements. A second prototype has been fabricated, with the right process and validated up-to 9.6 GHz. The measurements of FIRST V2 will be described in detail.

4.3.1. Test hardware description

4.3.1.1. Measurement tools

As mentioned earlier the interpolator is a LTI system. To verify the core functionality at one specific frequency, input patterns must be programmed, pass through the interpolator and the output memory must be analysed. The test scheme is presented in Figure 4-23.

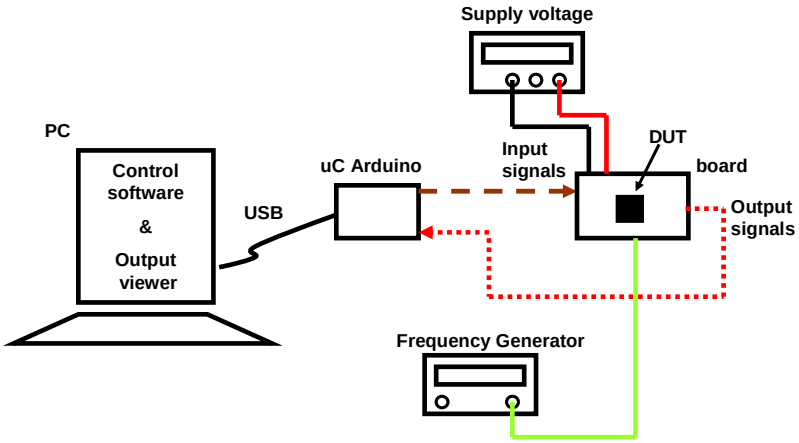


Figure 4-23: Test hardware to verify the core functionality

Patterns are shaped for the input memory by a Matlab script and written in a file. The content of the file is read by a program realized in Visual Basic. The software integrated the microcontroller library for data exchange.

Arduino is a microcontroller board based on the ATmega328. It has 14 digital input/output pins, a 16 MHz crystal oscillator, a USB connection, a power jack, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable to get started.

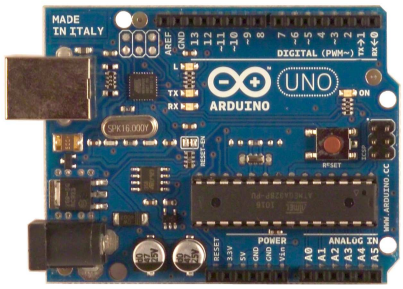


Figure 4-24: Microcontroller board

The Arduino is used for several tasks:

- Manage the communication protocol from the PC to the DUT. The Arduino integrates a USB-to-serial data converter.
- Manage the generation of the input signals (reset, input, clock_low, enable) and the recovery of the output data (output_mem and sync)

The Arduino works with a digital amplitude from 0V to 5V. The generated signal must be compatible with the chip where the digital amplitude goes from 0V to 1V. This conversion is realized with a daughter board connected to the Arduino (see photography).

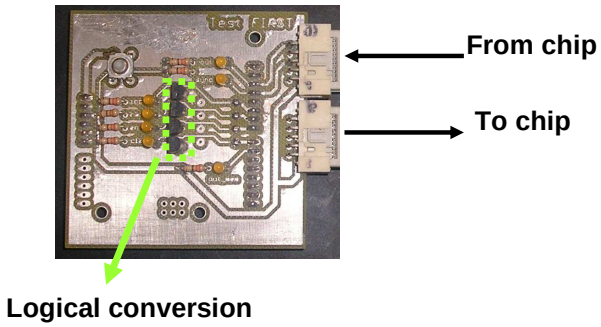


Figure 4-25 : Photography of the daughter board

The same problem appears at the outputs of the chip that go from 0V to 1V, they must be converted to 0V to 5V. The conversion is realized directly on the PCB. In both directions, the level conversion is realized with discrete bipolar components.

Once the output memory has been read, data are sent to the computer. The visual basic software shapes the data and plots them directly in a viewer. If the response seems correct, it is compared to the VHDL model.

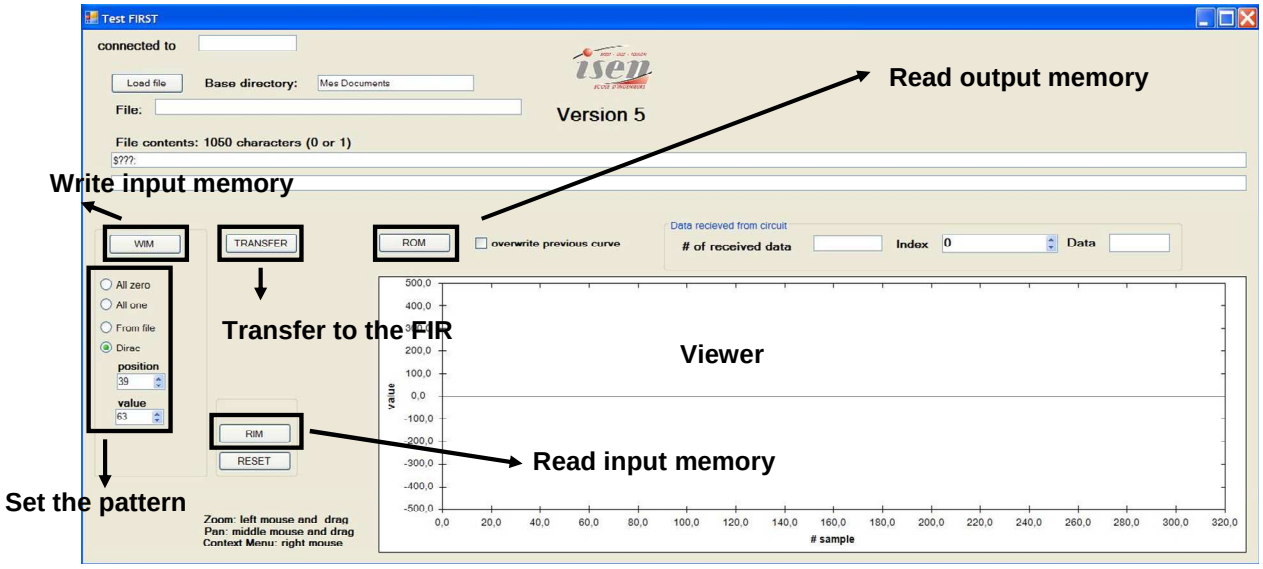


Figure 4-26: Software to test the core

The PCB, the substrate is a FR4, 2-layer, 840mm x 470mm PCB with state-of-the-art constraints on track width and isolation. Tracks on which the IC will be bonded are 75um wide and spaced by 100um from other tracks. The wire bonding operation did not give any difficulties. The main critical signal to route is the 10 GHz clock. This clock line has been matched to 50 ohms and terminated by two parallel resistors of 100 ohms. The configuration bits (enable_conso, bit0, bit1 and bit2) are set by jumpers. Connectors are used to provide input signals and output signals. The 1V to 5V conversion is realized at the

output of the chip with discrete bipolar transistors. Decoupling capacitances have been soldered as close as possible to the chip.

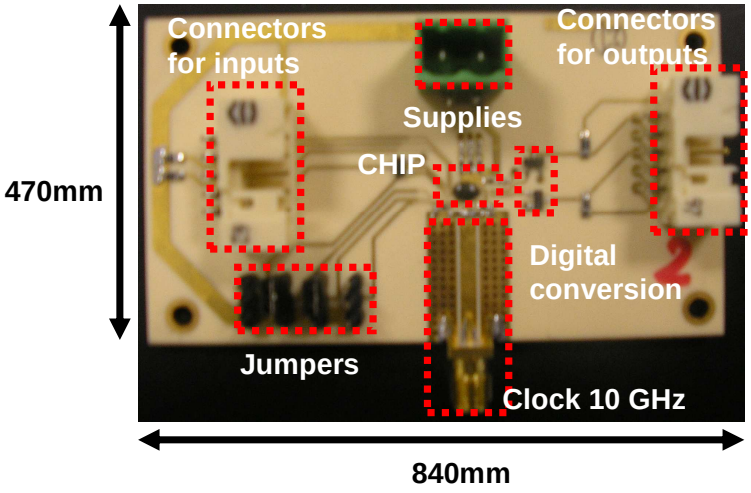


Figure 4-27: Photography of the board

4.3.2. Prototype

Two prototypes have been fabricated. The first one did not work because of an error in the process. The results presented here are the results of the second prototype.

4.3.2.1. Core functionality

To show the right functionality of the core, the impulse response has been chosen. The advantage of this method is that it is pretty easy to check the functionality while having a look at the temporal output response in the viewer integrated to the custom software.

The core has been measured at different frequencies starting at 500 MHz and for different supply voltages.

Clock @ 16 dBm	0,8	0,9	1	1,1	1,2	1,3	1,4	1,5
500M	14mA	17mA	20mA	22mA	25mA	29mA	32mA	36mA
1G	24mA	28mA	33mA	37mA	42mA	47mA	52mA	58mA
2G	45mA	52mA	59mA	67mA	75mA	84mA	93mA	104mA
3G	65mA	75mA	85mA	97mA	109mA	121mA	135mA	150mA
4G			111mA	126mA	142mA	160mA	178mA	198mA
5G					179mA	200mA	222mA	247mA
6G							264mA	293mA
7G							308mA	343mA
8G							349mA	390mA
9G							390mA	438mA
9G5							408mA	460mA
10G								
11G								

Clock @ 19 dBm

Table 4-3: Schmoo diagram

From Table 4-3 some conclusions can be given.

a. Working frequency

Regarding the working frequency, the interpolator does not work at 10 GHz but at the maximum at 9.5 GHz and not at the nominal supply voltage but at 1.4V. Indeed it works up-to 9.6 GHz but this last measurement was not repetitive. The interpolator works up-to 3 GHz at a reduced supply voltage of 0.8V. The working frequency can be compared to the expected performances found in Chapter 3 (see Figure 4-28).

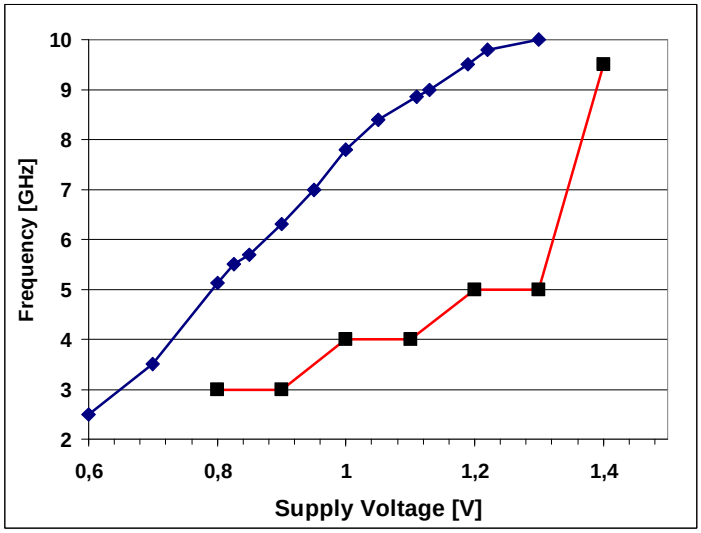


Figure 4-28 : Measurements (red line) and simulation (blue line) of the max working frequency

An increase of the supply voltage of 200mV, increases the maximum working frequency by 1 GHz. At the supply voltage of 1.4V all operating frequencies between 500 MHz and 9.6 GHz are valid.

First of all, the 9.6 GHz limit has never been passed. Extracted simulations have shown that the problem comes from the clock driver and the clock-tree. The clock driver shapes the input sine wave and provides the clock to the clock-tree. This one does not work at 10 GHz with a nominal supply voltage. It can work at 10 GHz by increasing the supply voltage up-to 1.3 V. Nevertheless the clock provided to the clock-tree is degraded and affects the global performance of the FIR. During measurements a good way to see if the clock tree does not provide a clock is to increase the working frequency while checking the power consumption. At a certain point when the clock tree will stop working the power consumption will fall dramatically. This effect has been noticed. Now the reason why the clock tree is not able to provide the clock is mainly because the clock is so fast that charge and discharge of input flip-flop capacitances is not anymore possible. Even if

the current is increased by increasing the supply voltage, this charge and discharge can't be made. Remind that TSPCFF are sensitive to the shape of the clock.

This first explanation is about the working frequency but does not respond to the question why the characteristic looks like a square characteristic? A test simulation with the clock shaper and the complete FIR has been made. With the clock shaper extracted and clock tree extracted, at the temperature of 85°C and in a slow corner, the frequency vs supply voltage looks like the measured frequency. A complete schmoo diagram cannot be provided because one simulation runs for 5 hours. This assumption has not been verified because no data has been provided about the process after the tape-out.

Finally the last point is about the variations of the supply voltage. Dynamic logic and CPL logic are sensitive to variations of the supply voltage. As the chip is wired bonded and huge current peaks flow into the wires, voltage variations must be expected. This effect has been simulated only with the equivalent numbers of flip-flops in the interpolator while assuming an ideal off-chip power supply.

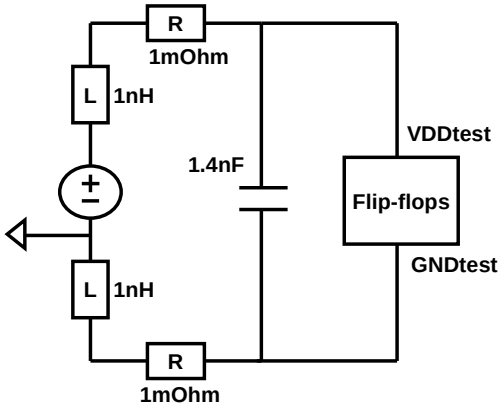


Figure 4-29: Simulation of the supply voltage variation

A DC loss and a voltage variation have been noticed depending on the working frequency. A loss of 80mV and a voltage variation of about 20mV have been noticed. This problem would need to be probe a further in order to develop techniques to be insensitive to these variations.

Finally as TSPCFF are used inside the chip, it is interesting to know the minimum working frequency of the chip. The chip is able to run at the minimum frequency of 161 MHz. This means that internally TSPCFF are clocked at the minimum at 8 MHz (clock division by 20).

b. *The power consumption*

Regarding the power consumption, Figure 4-30 and Figure 4-31 show the power consumption vs the working frequency at 1.4V and 1V. Both follow a linear trend as expected. The current consumption measured represents the current consumption of the entire chip. The core itself represents 70 % of the measured current consumption.

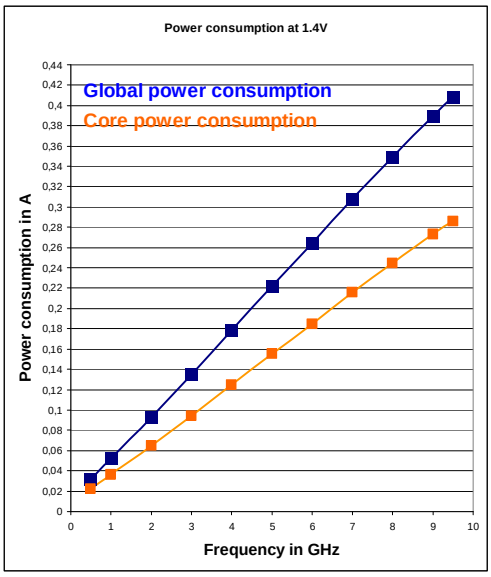


Figure 4-30: Power consumption vs Frequency at 1.4V

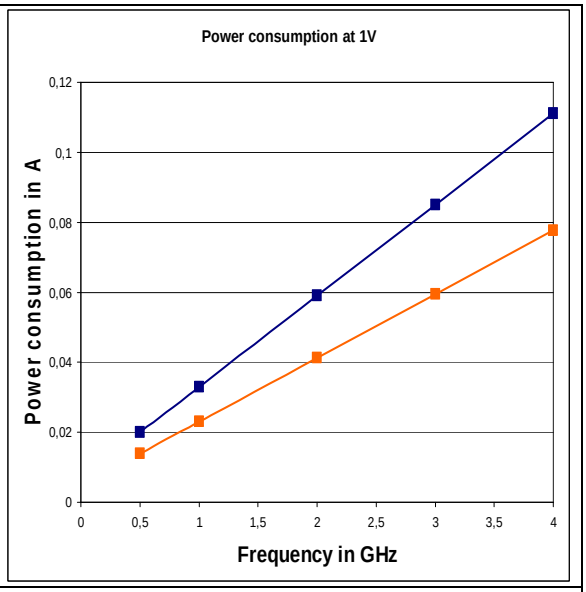


Figure 4-31: Power consumption vs Frequency at 1 V

At 9.6 GHz on a 1.4 supply voltage, the current consumption of the core is 285mA which represent a power consumption of 400 mW.

c. *Frequency response*

The input memory depth is sufficient to receive any kind of basic pattern. The impulse response has been one way to characterize the interpolator. In order to verify the frequency behaviour of the chip, the impulse response obtained is convoluted with OFDM symbols. Requirements are met and presented in Figure 4-32.

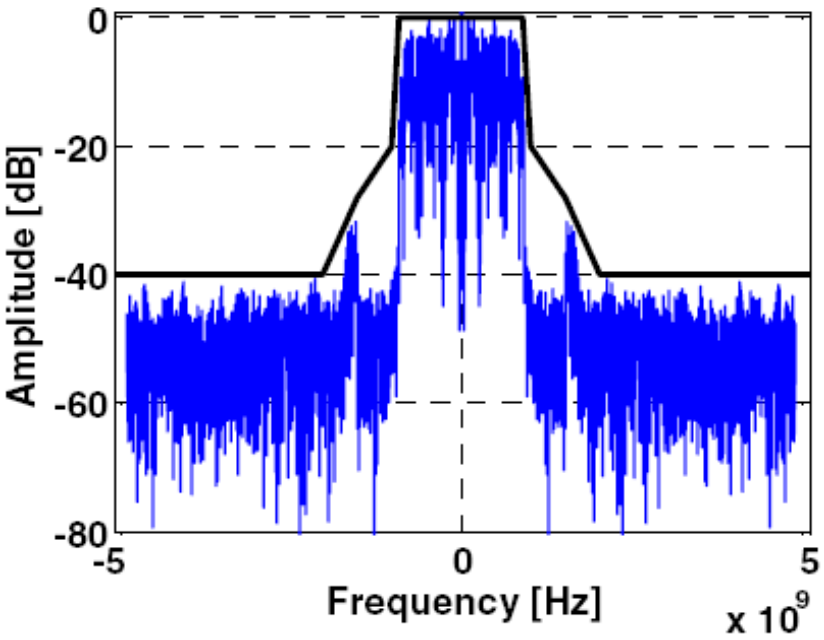
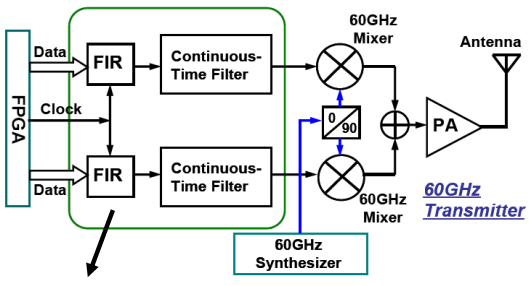


Figure 4-32: OFDM symbols filtered by convolution with measured coefficients. (the continuous line shows the filtering mask as derived from the IEEE 802.15.3c standard).

4.4. COMPARISON WITH SIMILAR WORKS

The closest comparison to the state of the art that can be performed is to a semi-digital FIR filter in a SiGe technology for a similar application described in [Ellinger10]. However, summing operations in [Ellinger10] are done in the analog domain; the circuit can therefore not be used in conjunction with a DRFC. Furthermore, the sampling frequency is lower as it targets single-carrier QPSK rather than OFDM modulations, and the spectrum mask is not fully met requiring additional analog filtering.

The architecture proposed by [Ellinger10] is depicted in Figure 4-33.



Work presented in [Ellinger10]

Figure 4-33 : 60 GHz direct conversion transmitter

The filter is composed of 17 taps. It filters images and converts the signal in the analog domain with the architecture illustrated in Figure 4-34. It has been realized in a 0.25 µm SiGe HBT technology, consumes 300mA with a supply voltage of 3.3V and the chip area is 1.6mm^2. The FIR works at the working frequency of 7 GHz.

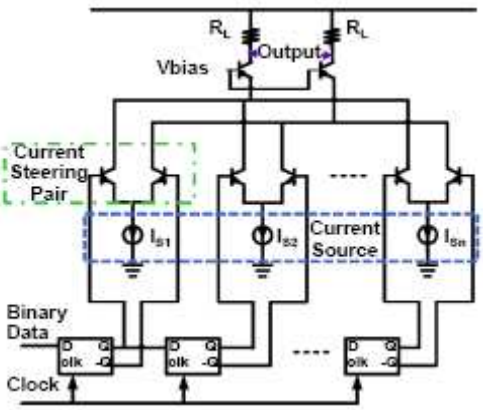


Figure 4-34: [Ellinger10] FIR architecture

The FIR topology consists of current steering differential pairs and DFlip-Flops. The output signal of the D-Flip-Flop can switch on and off the current steering differential pairs in each tap. The coefficients of the FIR filter are determined by the current source in each tap. The current mode outputs of the current steering pairs are summed together at the output.

The standard targeted is the ECMA standard with a relaxed spectrum mask (Figure 4-35).

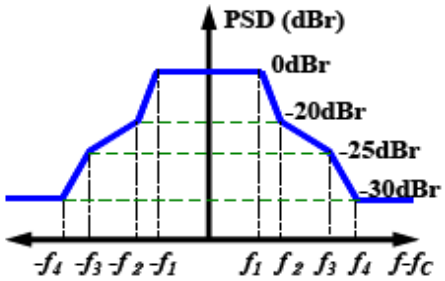


Figure 4-35: ECMA spectrum mask

Channel Bonding	Frequency(GHz)			
	f1	*f2*	*f3*	*f4*
Single Channel Transmission	1.05	1.08	1.5	2
Two Bonded Channels Transmission	2.1	2.16	3	4
Three Bonded Channels Transmission	3.15	3.24	4.5	6
Four Bonded Channels Transmission	4.2	4.32	6	8

Table 4-4: ECMA spectral requirements

Drawbacks of this work are:

- Sensitive to variations. The clock jitter causes inaccuracy of the FIR filter's response. Variations of the current sources cause also inaccuracies.
- Reduced requirements (ECMA standard)
- A high power consumption
- Design with an expensive technology

Advantage of this work is:

- Combine the FIR and DAC function

Table 4-5 summarizes the performances

	[Ellinger10]	This thesis
Technology	0.25um SiGE HBT	65nm CMOS STM
Fsample (GHz)	7	9.6
Number of taps	17	18
Attenuation (dB)	19 @ 2.2 GHz	40 @ 2.2 GHz
Power consumption (mW)	999	400 @ 1.4 V
Area	~0.8 mm2 (estimate)	0.1 mm2

Table 4-5: Performances summary

4.5. CONCLUSION

The test methodology for the interpolator has been presented. Different test cases have been studied, the one with on-chip input – output memories has been chosen.

A 65nm CMOS chip has been designed and fabricated in a STMicroelectronics process for demonstrating a key building block of the proposed 60 GHz wireless transmitter with SDR capabilities. A first chip has been fabricated but was not functional because of process errors. A second chip has been fabricated with the right process and has shown functionality up to 9.6 GHz. Measured performances fulfil requirements for the targeted standard. Performances in term of power consumption and working frequency are lower than expected in simulations but possible solutions to explain these problems

have been proposed. Nevertheless the designed chip settles the state-of-the-art in high speed digital design.

5. CHAPTER
PERSPECTIVES AND CONCLUSION

"If we knew what it was we were doing, it would not be called research, would it?"

Albert Einstein

This chapter gives some key points to probe further in the presented work. The first point presents a second test chip. This test chip has not been fabricated due to the lack of time. The second is focused on the different possible improvements with next generation technology.

A conclusion will be given to summing up the ideas presented in this document.

5.1. INTEGRATION OF THE FIR WITH A HIGH SPEED DAC.

The first idea before going to the realization of the FIR and the DRFC is to realize the integration of a FIR and high speed DAC. The standard baseband is composed of composed of an FIR and a DAC on I/Q.

The DAC is based on a current steering architecture. It accepts single ended inputs and provides differential outputs. It has an ENOB of 7.5 bits and works at 5 GS/s. Thus the working frequency of the FIR has been reduced by 2. The FIR working frequency is 2.5GS/s and 5GS/s. For a question of design reuse, the DAC has been provided by UC Berkeley has an IP block.

For test reasons ADCs have been used to generate digital signals from an analog generator. No input or output memories are used in this test chip. The ADC accepts differential inputs (DC = 225 mV and amplitude = 100 mV) and provides 9 bits converted on two outputs odd and even samples at half of its working frequency. The ADCs work at 1.25 GS/s with an ENOB of 9 bits. The architecture of the ADCs is a successive approximation.

The main difficulties of this test chip have been to:

1) Realize a synchronization of the two ADCs in order to assure that they start a conversion in the same time. A walking bit counter has been integrated with a control in order to start the ADCs in the same time

2) Interleave the output of each ADC in order to provide one stream at 1.25 GS/s to the FIR. The clock provided by the ADC is used to interleave odd and even samples.

3) Synchronize all the different blocks from a single clock provided off –chip.

The test chip has been realized in a 65nm technology from STMicroelectronics. Both LP and GP transistors are used. The nominal supply voltage for LP transistors is 1.2 V. Level shifters are used to realize up/down voltage conversion.

Characteristics of each block are summarized in Table 5-1

Block	Architecture	Size [um^2]	Sampling Frequency	ENOB
ADC	Successive approximation	610 x 472	1.25 GS/s	9
FIR	Interpolator	650 x 170	2.5 GS/s and 5 GS/s	7
DAC	Current steering	275 x 250	5 GS/s	7.5

Table 5-1 : Blocks characteristics

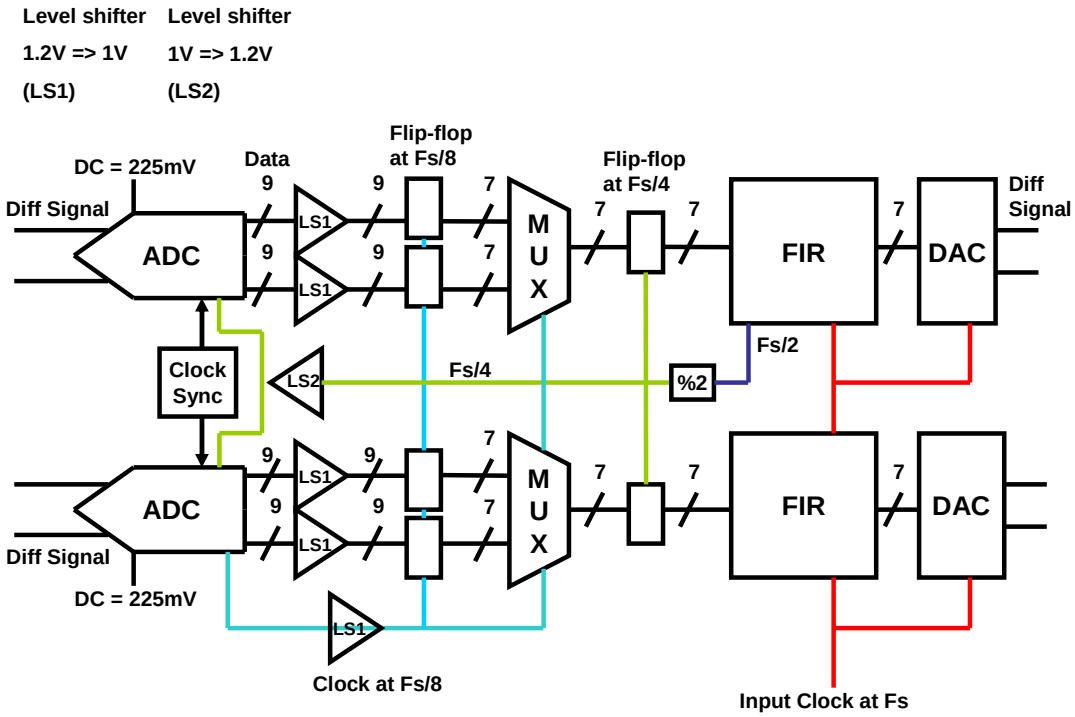


Figure 5-1: Baseband of the 60 GHz transmitter test chip

As illustrated in Figure 5-2, the test chip has been realized up-to the physical level. It has not been fabricated due to the lack of time once the first chip has been fully tested.

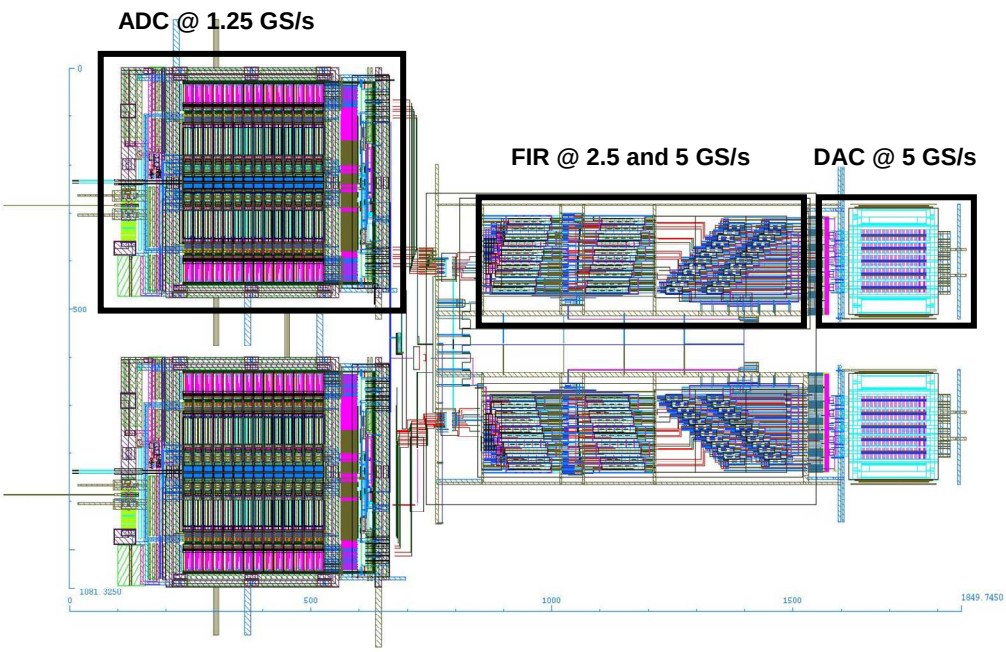


Figure 5-2: AC/DC physical layout view

5.2. TO PROBE FURTHER IN WIRELESS DIGITAL 60 GHZ TRANSMITTER

As it has been explained previously the 65nm technology has been pushed hardly to realize the interpolation function up-to 9.6 GHz. Different techniques enable this high working frequency but the power consumption has been neglected. In this part some key points are presented to reduce the actual power consumption of the interpolator function.

5.2.1.1. Complexity reduction

3 major changes can be applied to reduce the complexity of the interpolator and the power consumption:

a. Standard

The first one concerns about the standard. During these last 3 years the standard evolved and one of the major changes has been the reduction of the spectrum mask requirements.

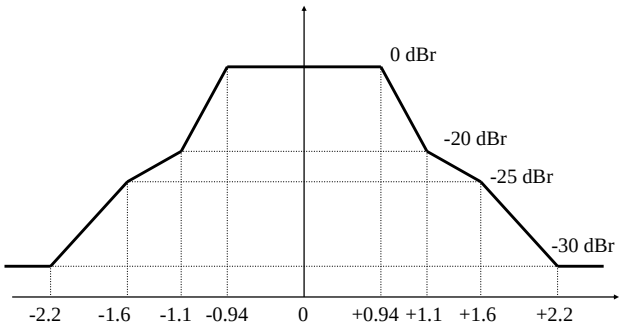


Figure 5-3: Actual spectrum mask [Spectrum10]

b. Interpolator specifications

As the standard changed, global specifications for the interpolator must also change. The modifications must appear at a system level where the FIR architecture must be simplified to avoid working at 10 GS/s.

c. Future technology nods

The 32 and 28 nm node are the next technology nodes. These technologies will allow on/off switching transistor at a higher frequency. The impact is remarkable in the sense that the design complexity will be reduced. In a first approximation the power consumption can be reduced by two because the use of CPL logic will not be necessary anymore. Significant reduction in complexity will be possible.

d. Conclusion

Considering the possible improvements a reduction of the design complexity and power consumption must be expected.

5.3. CONCLUSION

This document presented the study of a 60 GHz transmitter with software defined radio capabilities. The study started at a system level. The interpolator has been optimized in order to simplify the design. The design is based on different studies from the architectural level to the physical level. The interpolator has been designed based on this study. A mix of static and dynamic logic enable 10 GS/s data rate. A basic but clever solution to measure the interpolator has been presented. Results show that the bloc is able to run up-to 9.6 GS/s. Perspectives to this work have been presented.

5.4. REFERENCES

Web site:

[Spectrum10]:http://www.ecma-international.org/publications/files/ECMA-ST/ECMA-387.pdf

I. Annexe: 60 GHz IEEE TG3C.15.3C Standard

The 60 GHz IEEE TG3C.15.3C standard is presented in this annexe. First a review of the OFDM access is presented. Then specifications as the transmit mask, modulations and EVM, are given.

60 GHz IEEE TG3C.15.3C

In November 2007 the Working Group TG3C for Wireless Personal Area Networks (WPANs) gave a first merged document with the standardization for the 60 GHz frequency band. This draft defined a new millimetre wave (mmWave) based alternative physical layer (PHY) for the existing 802.15.3 Wireless Personal Area Network (WPAN) Standards 802.15.3-2003 and 802.15.3b-2005, and enhancements to Medium Access Control Layer (MAC) to enable operation at mmWave frequencies, with multi-Gbps throughput. Today this e and other competing standards are available.

The standard is composed of two transmission modes. Single carrier (SC) transmission modes are intended to cover various applications from low to high bit rate applications more suitable for power limited LOS environments and OFDM transmission modes more suitable for high bit rate transmissions over limited bandwidth and in non-LOS channels.

In this work SC transmission is not studying. OFDM transmission mode will be used as a reference [IEEE09]. Other standards exist and are not presented [WirelessHD], [ECMA09].

1. Survey of OFDM

In order to understand the signal involved, a survey of OFDM is presented [Richard99]. The basic principle of OFDM is to split a high-rate data stream into a number of lower rate streams that are transmitted simultaneously over a number of subcarriers. Because the symbol duration increases for the lower rate parallel subcarriers, the relative amount of dispersion in time caused by multiple paths delay is decreased. Inter symbol interference is significantly reduced by introducing a guard time in every OFDM symbol. In

the guard time, the OFDM symbol is extended (called Prefix Cyclic) to avoid inter carrier interference.

An OFDM signal consists of a sum of subcarriers that are modulated by using simple modulation scheme like PSK (phase shift keying), QAM (quadrature amplitude modulation). This basic representation is depicted in Figure 5-4

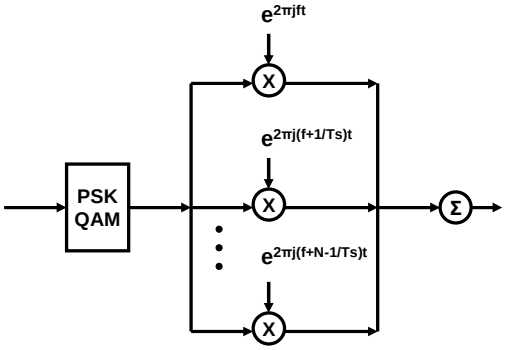


Figure 5-4: Basic construction of an OFDM Symbol

If I_k are the complex QPSK symbols, N is the number of subcarriers and T is the symbol duration, then one OFDM symbol starting at t=0 can be written as:

$$v(t) = \sum_{k=0}^{N-1} I_k e^{i2\pi kt/T}, 0 \le t \le T \qquad \text{Eq 5-1}$$

$$v(t) = 0\,,\ t < 0 \text{ or } t > T$$

The spacing between the different subcarriers of 1/T Hz makes them orthogonal between them.

The complex baseband OFDM signal is in fact nothing more than the inverse Fourier transform of N QPSK or QAM input symbols. The discrete time equivalent is the inverse discrete Fourier transform (IDFT), which is

$$v(n) = \frac{1}{N} \sum_{k=0}^{N_s} I_k . e^{2i\pi n \frac{k}{N}} \qquad \text{Eq 5-2}$$

where the time t is replaced by sample number n . In practice this transform can be implemented very efficiently by the inverse fast Fourier transform (IFFT). An N point IDFT requires a total of N^2 complex multiplications which are only phase rotations. There are also additions necessary to do an IFFT, but the hardware complexity of an adder is significantly lower than that of a multiplier or phase rotator. The IFFT drastically reduces the amount of calculations by exploiting the regularity of the operations in the IDFT.

A basic OFDM modulator is depicted in figure

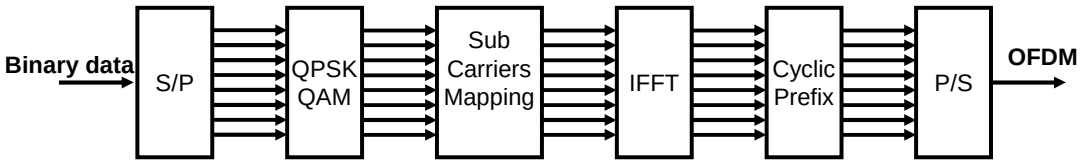


Figure 5-5: Basic OFDM modulator

First the binary signal is transformed from a series stream to a parallel stream. Then the data are mapped on a modulation as a QPSK or a16QAM. Sub-carriers are mapped (DC, Data, Pilots, Null). Then an IFFT is performed and a cyclic prefix is added. Finally a parallel to series conversion is done. The signal can now be transmitted by standard transmitting architectures.

2. HRP radio channel

The frequency plan used in the 60 GHz standard is presented in Figure 5-6. It is composed of four channels of 1728 MHz between 57.240 GHz and 65.880 GHz. The High-rate PHY (HRP) is a PHY that supports multi-Gb/s throughput. The HRP is optimized for the delivery of uncompressed high-definition video, other data can also be communicated using HRP.

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)	Roll-Off Factor
A1	57.240	58.320	59.400	1728	0.25
A2	59.400	60.480	61.560	1728	0.25
A3	61.560	62.640	63.720	1728	0.25
A4	63.720	64.800	65.880	1728	0.25

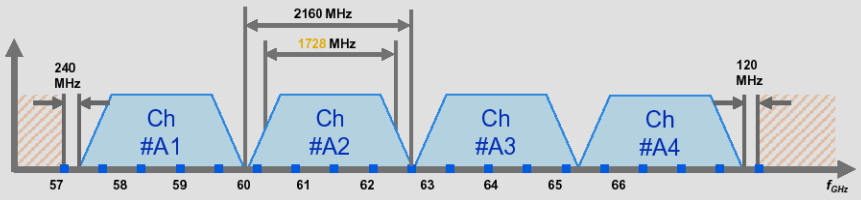


Figure 5-6: HRP radio channel plan

3. Spectrum mask

The spectrum shall adhere to the transmit spectrum mask shown in Figure 5-7. The spectrum mask guarantees that the devices do not interfere with each other. In Figure 5-7 one may also see how the subcarriers and null carriers are placed in the spectrum.

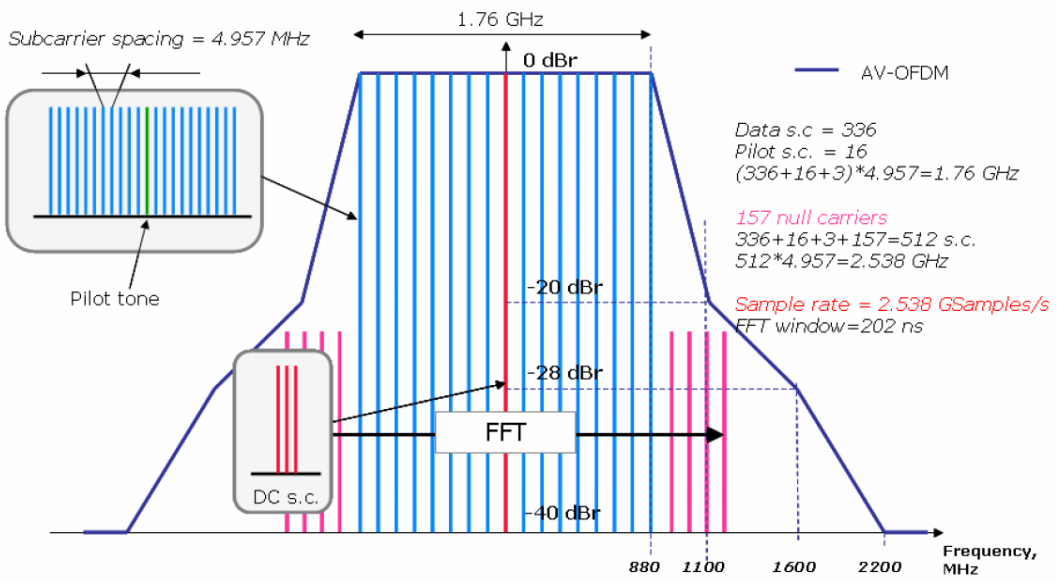


Figure 5-7: Tx mask

4. OFDM specification

The mapping of data and pilot subcarriers within an OFDM symbol is illustrated in Figure 5-8 [IEEE09]. The mapping is further summarized in Figure 5-9. As shown in Figure 5-8, there are 16 groups of subcarriers where each group consists of 21 data subcarriers and one pilot subcarrier. Finally a cyclic prefix is added. Typical value for cyclic prefix is 64.

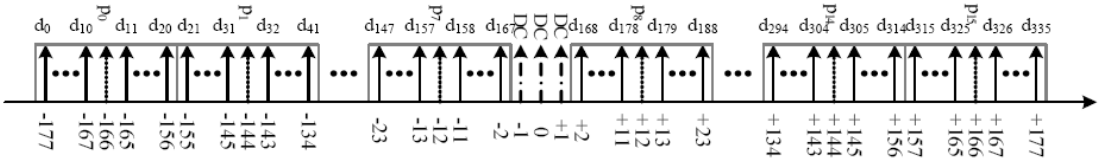


Figure 5-8: IFFT subcarriers frequency allocation

Subcarriers type	Number of subcarriers	Logical subcarriers indexes
Null subcarriers	141	[–256: – 186] ∪ [186:255]
DC subcarriers	3	–1, 0, 1
Pilot subcarriers	16	[– 166:22: – 12] ∪ [12:22:166]
Guard subcarriers	16	[– 185: – 178] ∪ [178:185]
Data subcarriers	336	All others

Figure 5-9: Subcarriers frequency allocation

Two different modulations can be applied on the data subcarriers. The first one is a simple QPSK. The constellation of a QPSK signal is depicted inFigure 5-10. The second one is a 16 QAM modulation. The constellation of the 16 QAM signal is depicted in Figure 5-11.

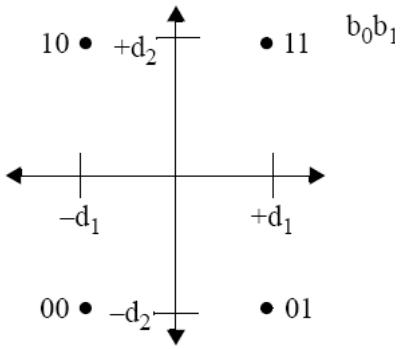


Figure 5-10: QPSK constellation

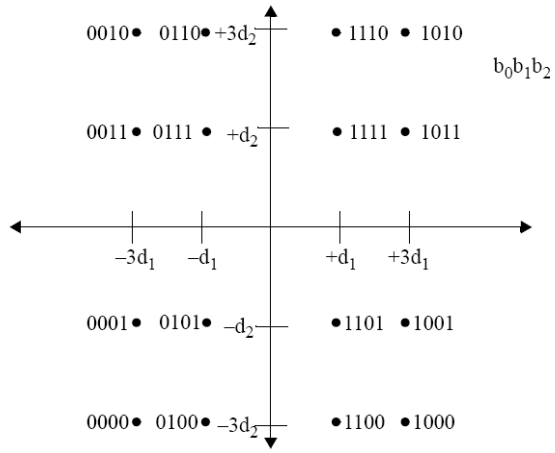


Figure 5-11: 16 QAM constellation

No specifications are given in the standard about the authorized ripple in the band. These specifications depend on the digital signal processing applied on the transmitter (pre-distortion) and receiver side (equalization).

5. Error Vector Magnitude specification

The error vector magnitude (EVM) is a vital quality measure for a transmission. A signal with an ideal constellation is created in the transmitting baseband. Following a set of imperfections in the transmitter implementation, the ideal location of the constellation changes. EVM is a measure of how far the points are from the ideal location.

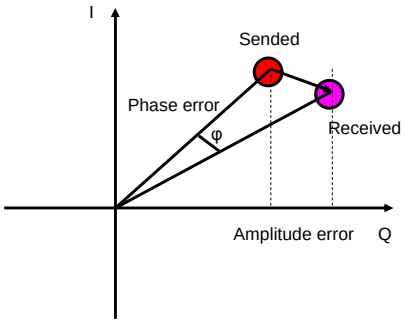


Figure 5-12: Error Vector Magnitude

In practice the EVM of a transmitter is measured by calculating the euclidean distance between the received symbol and the closest constellation point. The EVM is then the average RMS errors over a number of symbols. It is given by:

$$EVM_{rms} = \sqrt{\frac{\sum_{j=1}^{Ns}\left\{\sum_{k=1}^{Ndsc}\left[I_{jk} - I^{*}_{jk}\right]^{2} + \left[Q_{jk} - Q^{*}_{jk}\right]^{2}\right\}}{Pavg.Ns.Ndsc}} \qquad \text{Eq 5-3}$$

Ns = Number of symbols

Ndsc = Number of data sub-carriers

Pavg = Average power of the constellation

$\left[I_{jk} - I^{*}_{jk}\right]^{2}$ and $\left[Q_{jk} - Q^{*}_{jk}\right]^{2}$ = Is the complex coordinates of the jth measured symbol in the kth sub-carrier.

The EVM requirements are summarized in Table 2.

Mode	Modulation	Coding rate	Min output power	Max EVM
HRP0	QPSK	1/3	12 dBm	45 %
HRP1	QPSK	2/3	12 dBm	20 %
HRP2	16 QAM	2/3	12 dBm	9 %

Table 2: EVM requirements

References

[ECMA09]: http://www.ecma-international.org/ (online)

[IEEE09]: http://www.ieee802.org/11/Reports/tgad_update.htm (online)

[WirelessHD]:http://www.wirelesshd.org/pdfs/WirelessHD-Specification-Overview-v1.1May2010.pdf

II. Annexe: Study of the IEEE 802.15.3c with QAM

This part describes the filter synthesis for 16 QAM modulation used in the standard. Before going into details and simulations a fact must be established: A GA was not really necessary in section 2.6 considering the search space of 6 coefficient filters (means 3 coefficients to generate because of the symmetry). A simple brute force algorithm would have been able to find the best solution in such small space. But it is interesting to see the GA as a generalisation of a problem: find a set of powers of two coefficients that respect a filter frequency specification. The GA is able to synthesize FIR filters with a number of coefficients >> 9 coefficients where a brute force will take hours and hours. Till now OFDM based on QPSK has been used, in following sections it will be shown that the GA is necessary if one wants to synthesize FIR filters in order to use OFDM based on 16QAM modulation.

In the standard another modulation is also used with the OFDM access. The modulation is a 16 QAM. The architecture used for this study is presented in. This architecture is divided in two stages: the first one is composed of one filter that works at 5GS/s and the second part is composed of one filter that works at 10GS/s (corresponds to the first improvement presented in section2.4). The system has been studied to target the OFDM with a 16 QAM modulation and an EVM < 10% that is compliant with the standard. The number of coefficients per filter increased and the search space size as well making the use of an heuristic unavoidable.

This study has been realized in order to show that it is still possible for other modulations to use the system presented in this work. No implementation of the QAM architecture has been realized.

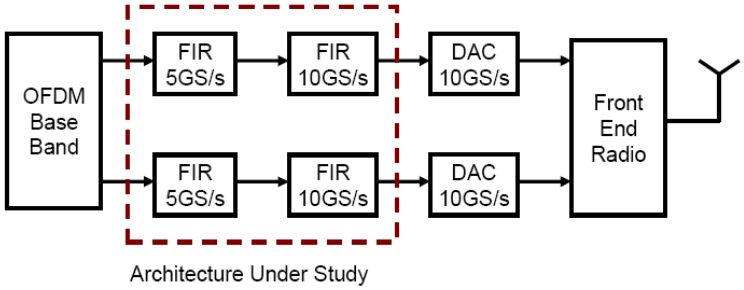


Figure 5-13: OFDM with 16 QAM architecture

A basic parametric simulation can be done to evaluate the number of coefficients per filter needed to target the EVM specification. Simulation results show that 15 coefficients for the filter that works at 5GS/s and 10 coefficients for the filter that works at 10GS/s are implemented to target the EVM. Coefficients are quantized as real numbers.

The magnitude response of this global filter is depicted in Figure 5-14. Filters are synthesized with real coefficients with Matlab. An odd number of coefficients is used to assure a linear phase. EVM is computed as an EVMmean. Considering a filter (linear time invariant system) the most important contribution to the EVM is the ripple in the band; group delay – in other words the linear phase is not an important parameter since can be easily corrected. Maximally flat filters are a solution for very low EVM thanks to their ripple close to 0 and their linear phase.

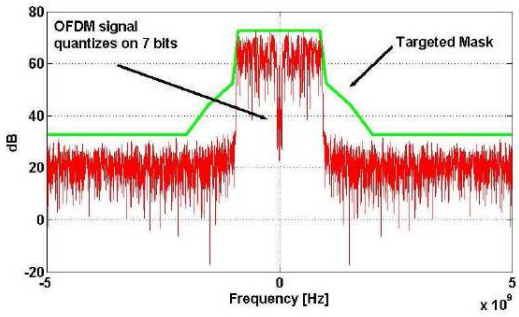


Figure 5-14: OFDM QAM16 symbol filtered by baseband filters with real coefficients

Here in Figure 5-14 the ripple in the band (linear) of the 5GS/s filter equals to 0.001 and the ripple in the band (linear) of the 10 GS/s filter is 0.007. The ripple of both is considerated as negligible and ensures a very good EVM. Phase shift introduced by the LTI system can be corrected at the equalization stage on the receiver side.

The goal of designing one stand alone filter is here challenged. We investigate a cascade like architecture for at least 2 reasons:

- This approach is similar to the divide and conquers heuristic since the GA first picks up most promising filter coefficients and secondly in this reduced search space, the best combination of filters is selected.

- Cascading FIR filters results in convolution of their coefficient vectors. It follows that sums of power-of-2 naturally appears in the global transfert function which is more promising since these sums of power-of-two more densively cover the real line.

The cost of the overall search is far smaller in this approach than would have been if the GA had to browse higher order filters with sum of powers-of-two coefficients. Systematic optimization of the combination of filters extracted from limited sets of solutions will be investigated in future works.

With regards to the number of real coefficients found in the filter requirement subsection, FIR filters have been synthesized by the GA with numbers of coefficients ranging from 10 to 19 at 5 GS/s and 10 GS/s filters. Such an increase of the search space from 10 to 19 tends to compensate the loss of precision in the transfer function because of powers of two discretization. Results are shown in Figure 5-15. Finally 16 coefficients for the filter at 5 GS/s and 13 coefficients for the filter at 10 GS/s were used with a global ripple of 0.01 (linear). The optimal filters have been overdesigned to assure a very low ripple in order to find only maximally flat filters thus a very low EVM. The EVMmean estimated is 1% which is completely compliant with OFDM access with 16QAM modulations. An OFDM symbol is applied to the FIR filter. The signal is quantized with 7bits. Images at 2.5GHz and 5GHz of the baseband signals have been completely filtered.

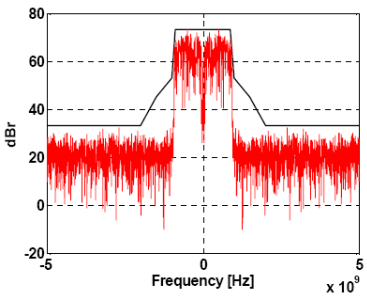


Figure 5-15: OFDM QAM16 symbol filtered by baseband filters with powers-of-two coefficients

RESUME EN FRANÇAIS

“Emetteur sans fil à 60 GHz avec des possibilités radio logicielle”

Par Jonathan Muller

Ce travail de recherche introduit une solution d’architecture radio numérique qui permet de remplacer les solutions standards analogique en tirant partie d’une technologie CMOS avancée.

Cette architecture se base sur deux blocs : un interpolateur numérique et un DRFC. Le DRFC est un bloc qui combine un convertisseur numérique-analogique et un mixer. Le signal provenant de la bande de base contient des images à tous les multiples de sa fréquence d’échantillonnage (cf. théorème de l’échantillonnage). Si ce signal est transmis directement à la fréquence radio par l’intermédiaire du DRFC, les images du signal vont polluer les canaux radio adjacents. Il convient donc de filtrer ces images en bande de base avant translation. Pour ce faire un interpolateur est mise en œuvre.

Cette thèse propose l’étude système ainsi que l’étude de réalisation de l’interpolateur. Un circuit prototype en 65nm CMOS a été développé pour démontrer le concept proposé. L’organisation de ce résumé est la suivante : dans une première partie la notion de radio logicielle est abordée. Un état de l’art succinct des architectures radio est effectué afin de bien comprendre les problèmes de développement des transmetteurs à l’heure actuelle. Dans une seconde partie, tenant compte des conclusions de l’état de l’art, une chaine radio est proposée pour un standard 60 GHz. Le standard 60 GHz choisi sera détaillé pour en comprendre les principales spécifications. L’étude système de cette chaine est proposée aussi dans la seconde partie. Une troisième partie aborde la notion de conception de circuits. L’interpolateur est étudié d’un point de vue électrique. Les contraintes importantes liées à la réalisation du bloc numérique à très haute cadence sont abordées et des solutions proposées. Cet interpolateur a été réalisé dans une technologie CMOS 65nm. Dans la quatrième partie les mesures de l’interpolateur sont présentées et

comparées à l'état de l'art dans la cinquième partie. Enfin des pistes à investiguer pour continuer ce travail sont proposées.

Ce résumé en français détaille, de façon concise et rapide le contenu de chaque chapitre en anglais, en mettant en avant les concepts proposés, les limitations rencontrées et comment elles ont été surmontées.

Chapitre 1

Durant ces dernières années, la plupart des efforts de l'industrie ont été porté sur les télécommunications utilisant la bande de 1-10 GHz pour des applications multimédias. L'intérêt pour les communications sans fil devient plus élevé de jours en jours et de nouvelles perspectives voient le jour. Afin de répondre à ces demandes, de nouvelles solutions doivent être fournies en particulier en termes de débit de données. En suivant la théorie de Shannon, une façon d'augmenter le débit de données est d'augmenter la bande passante. L'UWB (ultra large bande) a été mis en œuvre spécialement pour cela. Mais cette technologie qui utilise la bande 3 - 10 GHz du spectre doit pallier à un taux de données limité et à un grand nombre d'interférences. À ces fréquences, e spectre est bondé de brouilleurs: Bluetooth, Wifi, WiMax, etc. Une solution est apparue en 2001 lorsque la FCC (Federal Communications Commission) a publié la bande 57-66 GHz. 9 GHz de bande passante, sans licence, sont disponibles et prêts à être utilisés pour permettre de nouvelles applications. [Niknejad08_1].

Transmettre des ondes à 60 GHz n'est pas sans surprises. La bande 60 GHz se trouve dans la bande dite millimétrique en référence à la longueur d'onde (Figure 1-3). A cette fréquence, on trouve un pic d'absorption important (Figure 1-4). L'impact direct de cette absorption est que l'onde transmise sera rapidement atténuée. Néanmoins on peut y voir certains avantages. Par exemple, comme l'onde est fortement atténuée, une tierce personne ne pourra pas récupérer cette onde. La liaison est naturellement sécurisée.

La mise en œuvre, d'un point de vue électrique, d'émetteurs à 60 GHz soulève quelques questions. Traditionnellement, ces émetteurs ont été réalisés avec des technologies coûteuses à base de semi-conducteurs III-V (InP, GaAs) [Smulders07]. Les progrès rapides de la technologie CMOS ont ouvert la voie à la réalisation d'émetteur à 60 GHz. Malgré cela les architectures CMOS analogiques standards ont de plus en plus de difficultés à suivre les contraintes liées à la réduction de la technologie (la tension d'alimentation diminue ainsi que les performances du dispositif), ce qui rend le développement d'émetteurs-récepteurs SoC plus en plus difficile. Des solutions ont été proposées ces dernières années en technologie CMOS et SiGe [Reynolds07], [Wicks09], [Okdada11], [Siligaris11]. Ces solutions sont purement analogiques et suivent le design traditionnel d'une chaîne radio (Figure 1-7 et Figure 1-21).

De nouvelles architectures sont nécessaires pour s'affranchir des limites de ces nouvelles technologies. L'idée sous-jacente est d'obtenir une et une seule chaîne radio que configurable à souhait pour émettre selon différents standards. Des architectures numériques ont été proposées pour les communications des téléphones mobiles. Ces architectures sont dites bandes étroites car elles translatent de petites bandes passantes de l'ordre du MHz. Les travaux de [Eloranta08] et [Pozsgay08] sont des références dans ce domaine.

En ce qui concerne le « 60 GHz », des concepts de radio numérique ont été introduits par [Niknejad09] et [Tomkins09]. L'idée dans ces chaînes est de translater directement à la fréquence radio un signal provenant de la bande de base.

Cette thèse propose la réalisation d'un émetteur sans fil à 60 GHz où la radio numérique est prédominante avec une technologie standard CMOS 65nm.

Chapitre 2

Ce chapitre présente, au niveau système, une façon de numériser une chaîne d'émission standard à 60 GHz. Deux types d'architectures numériques sont présentées : une suivant la structure Homodyne (Figure 2-5) et l'autre suivant la structure Hétérodyne (Figure 2-8).

L'architecture Homodyne (Figure 2-5) est basée sur un DRFC (convertisseur numérique-à-RF) afin de réaliser une conversion directe du flux de données numériques à la fréquence RF. Cette structure a été étudiée par [Eloranta08] et [Pozsgay08]. Le DRFC combine en fait un convertisseur numérique-analogique et un mixer. Le flux de données numériques à la sortie en bande de base est un signal échantillonné à la fréquence de 2.5 GS/s (cf. standard chapitre 1). Suivant le théorème de l'échantillonnage, des images aux multiples de la fréquence d'échantillonnage du signal apparaissent. Si une conversion D/A et une translation directe de ce signal sont réalisées les images résultantes de l'échantillonnage pollueront le spectre et donc les canaux adjacents. D'après le standard nous disposons de 9 GHz libre autour de 60 GHz. Aussi après conversion nous devons garantir que le spectre n'est pas pollué sur cette bande en garantissant le masque spectral définit lui aussi dans le standard. Pour se faire les répliques doivent être filtrées. Le bloc qui réalise l'opération de sur-échantillonnage et de filtrage s'appelle un interpolateur. En fonctionnant à 10 GS/s et selon son gabarit, nous pouvons garantir qu'après conversion et translation, le masque spectral sera respecté et que la première image résultant du dernier échantillonnage se trouvera à 10 GHz d'offset et donc en dehors du plan de fréquence.

L'architecture Heterodyne (Figure 2-8) est basée sur un IRFC (intermediate-to-radio frequency converter). Le flux de données numérique provenant de la bande de base est filtré, comme dans la structure Homodyne, puis est translaté numériquement à une fréquence intermédiaire avant d'être translaté à nouveau par l'IRFC à la fréquence RF. Cette chaine d'émission intègre donc en plus un bloc numérique qui translate les données autour d'une fréquence IF (Figure 2-9). Les structures IRFC et DRFC fonctionnent sur le même principe, néanmoins dans le cas de l'architecture Heterodyne comme le signal est déjà translaté à une fréquence IF d'autres techniques de design peuvent être introduites. En l'occurrence une méthode de design radio (combinaison par transformateur) visant à augmenter les performances de ce dernier bloc est présentée dans la Figure 2-12.

L'étude de l'interpolateur est présentée en détail dans ce chapitre.

Tout d'abord un signal test est construit. Ce signal servira de signal d'entrée de l'interpolateur. Sa construction est basée sur le standard définit dans le chapitre 1. Une modulation de type OFDM QPSK est choisie. 512 sous-porteuses sont utilisées dont 336 pour les signaux modulés en QPSK. Des simulations Matlab valident sa construction (Figure 2-15). Ce symbole est quantifié sur 7 bits qui est le nombre de bit nécessaire pour respecter le SNR de 40 dB défini par le standard.

Ensuite une première étude système du FIR est proposée. L'idée est d'estimer la complexité de l'interpolateur. Un premier FIR avec des coefficients réels est proposé. (Figure 2-18). Ce filtre devra fonctionner à 10 GS/s et atténuera les fréquences du DC à $F_S/2$ (5 GHz).

Afin de simplifier le design de l'interpolateur, une seconde étude tente de réduire la complexité du filtre, en termes de fréquence de fonctionnement et du nombre de coefficients, par une approche dichotomique. L'idée sous-jacente est la suivante : à partir d'un filtre à 10 GHz à N coefficients, pouvons-nous construire une fonction de filtrage identique à deux filtres, l'un fonctionnant à 5 GHz sur N/2 coefficients et l'autre à 10 GHz sur N/2 coefficients ? Rien n'empêche de diviser le processus de filtrage en deux plans de fréquence, 5 GHz et 10 GHz, vu que les images du signal apparaissent entre 1.5 GHz et 5 GHz. La conclusion de cette étude est qu'il est possible de réduire la complexité du bloc de départ de 22 coefficients à 10 GHz par 4 filtres cascadés de tailles réduites dont 2 fonctionnent à 5 GHz sur 6 coefficients et les 2 autres à 10 GHz sur 3 coefficients. Les coefficients à 5 GHz et 10 GHz sont voulus identiques pour une simplification de design.

	Number Coefficients	Coefficients	Adders
5 GHz (x2)	6	$\left[-2^{-4}2^{-4}2^{-1}2^{-1}2^{-4}-2^{-4}\right]$	5
10 GHz (x2)	3	$\left[2^{-2}2^{-1}2^{-2}\right]$	2

Tableau : Récapitulation de l'interpolateur.

L'interpolateur est composé de filtres en cascade. Deux filtres à 5 GHz sont utilisés, avec 6 coefficients et deux filtres à 10 GHz avec 3 coefficients.

Les coefficients sont quantifiés en puissance de deux. Ceci représente déjà une simplification dans le sens ou le multiplieur standard est remplacé par une opération de

décalage de bit. Ces coefficients ont été trouvés par un algorithme génétique. L'algorithme permet de trouver des coefficients quantifiés en puissance de deux pour filtres FIR a partir d'une spécification fréquentielle.

Chapitre 3

Ce chapitre présente la conception de l'interpolateur basée sur l'étude du système présenté dans le chapitre 2. L'approche de design employé est une approche dite top-down. D'abord le niveau architectural est étudié. Ensuite on arrive au niveau transistor avec différentes techniques de design et enfin au niveau physique avec le layout. La technologie utilisée est une technologie CMOS 65nm.

L'interpolateur pour le moment est une boite noire. Cette boite noire réalise une fonction de filtrage à partir de différentes fonctions de transfères convoluées entre elles. Nous savons aussi du chapitre 2 que le nombre de bit qui rentre dans cette boite noire est 7, ce qui correspond aussi au nombre de bit disponible à sa sortie. Et nous savons enfin que les blocs doivent fonctionner à la fréquence de 5 GHz et de 10 GHz.

Un filtre FIR est composé d'additionneurs et de flip-flops. Rappelons que les multiplieurs sont présents mais sous forme de décalages de bit.

Pour la structure de l'additionneur, l'additionneur à propagation de retenue a été choisi. D'autres structures d'additionneurs ont été étudiées mais le gain en vitesse n'est pas remarquable considérant le faible nombre de bit à traiter. La structure à propagation de retenue est simple à mettre en œuvre et considérant la contrainte de vitesse, simple à pipeliner. (Figure 3-11)

Au niveau transistor l'additionneur CPL a été choisi. Un benchmark entre différents additionneurs a été réalisé et c'est celui-ci qui offre les meilleures performances en termes de vitesse. (Figure 3-26 et Figure 3-27)

Pour la partie flip-flop. Une architecture dynamique a été choisie. Le TSPCFF est connu pour sa rapidité. Il offre l'avantage de ne travailler que sur une seule phase de l'horloge. (Figure 3-30)

Afin de répondre aux contraintes de vitesse de 10 GS/s, un pipeline de niveau 1 a été choisi. Cela signifie que le chemin critique se trouve être un flip-flop, suivi d'un additionneur, suivi d'un flip-flop. En terme de délais, on retrouve le délai du flip-flop, suivi du délai de l'additionneur, suivi d'un délai minimum ou la data doit être présente devant le flip-flop (setup time). La somme de ces délais doit être inférieur à la fréquence d'horloge maximum, c'est-à-dire, 100 pico-seconde. Ce chemin critique a été étudié à

différents niveaux. De la même manière pour la partie à 5 GHz, un pipeline de deux est défini. Ces deux briques de bases, pipeline 1 et pipeline 2 sont présentées dans la Figure 3-38 et la Figure 3-39.

A partir de ces deux cellules de base nous pouvons construire le FIR. Un model VHDL a été réalisé afin d'étudier la structure choisie à un niveau de précision du bit. Le filtre est construit selon la Figure 3-40. Des simulations de spectres de chaque bloc valident son fonctionnement à différentes températures et tensions d'alimentations. La génération d'horloge est aussi étudiée. Afin de limiter le décalage temporel une structure en grille est choisie. La sortie des buffers est reliée à la sortie des autres buffers. Ainsi il n'existe pas de chemins différents pour l'horloge et le décalage temporel de celle-ci est limité. (Figure 3-49)

Le layout est construit de la même manière. Les cellules de base, pipeline 1 et pipeline 2, sont étudiées en simulation post-layout pour tenir compte des capacités parasites. (Figure 3-50 etFigure 3-52) Le layout de l'interpolateur complet est présenté dans la Figure 3-56

Enfin une simulation globale valide l'interpolateur jusqu'à la fréquence de 10 GHz sous une tension d'alimentation de 1.3V. Ce résultat est présenté dans la Figure 3-61.

Chapitre 4

Ce chapitre présente la méthodologie utilisée pour tester le FIR ainsi que les résultats de mesure.

Le bloc désigné accepte en entrée des données à 2.5 GS/s et sort des données à 10 GS/s. Aucuns appareils à un niveau numérique n'accepte de recevoir une telle fréquence. Le test à haute cadence est donc une étape à solutionner afin de pouvoir tester le bloc.

La solution de test parfaite serait de pouvoir générer des symboles OFDM à partir d'un générateur externe, puis de les convertir, les traiter via le FIR et reconvertir ces symboles au niveau analogique pour étudier le comportement du FIR. Une étude a été réalisée pour voir si cette solution était réalisable avec des composants en boîtier que l'on pourrait souder sur une plaque de test. Des ADC fonctionnent à cette cadence mais augmentent la complexité de réalisation de la carte de test aussi. Il ne semble pas y avoir de solutions pour le DAC. Une autre solution serait faisable, générer le symbole OFDM de manière numérique a la fréquence de 2.5 GS/s via un générateur. Ce type de générateur existe mais à un prix très conséquent. Cette solution n'a donc pas été retenue.

Pour la mesure du circuit une solution très peu coûteuse et très simple de réalisation du point de vue carte de test a été choisie. Cette solution fait appel a une mémoire d'entrée que l on programme comme on le souhaite, avec différents vecteurs de test et une mémoire de sortie qui récupère la réponse du FIR aux vecteurs de test d'entrée. La mémoire d'entrée doit fournir 7 bits à 5 GS/s. Afin de simplifier le processus de test, la mémoire d'entrée est programmée en série a basse cadence (~KHz). Le FIR acceptant en entrée 7 bits à 5 GS/s un « serializer » est utilisé afin d'effectuer une transformation parallèle - série pour amener les bits de la mémoire d'entrée à la fréquence de 5 GS/s. Pour se faire 7 serializers 10->1 sont utilises. Pour la sortie le problème est inverse. Le FIR donne 7 bits à 10 GS/s. Pour que ceux-ci puissent être écrits dans la mémoire de sortie une conversion série – parallèle est effectuée. Un deserializer 1->20 est utilisé. Le facteur 20 vient du sur-échantillonnage interne du FIR.

Le schéma global de test choisi est présenté dans la Figure 4-19. On retrouve bien la mémoire d'entrée et de sortie. On trouve aussi le serialiser et le deserializer et l'ensemble des circuits de contrôle qui permettent l'écriture et la lecture des mémoires d'entrée et de sortie.

Le circuit global avec la partie test est présenté dans la Figure 4-20 et le circuit fabrique est présenté dans la Figure 4-21.

Une carte de test a aussi été fabriquée. Sa conception a été très simplifiée car les signaux mis en jeux sont à très faible cadence. Le seul soin particulier a été pris pour le signal haute cadence, l'horloge a 10 GS/s.

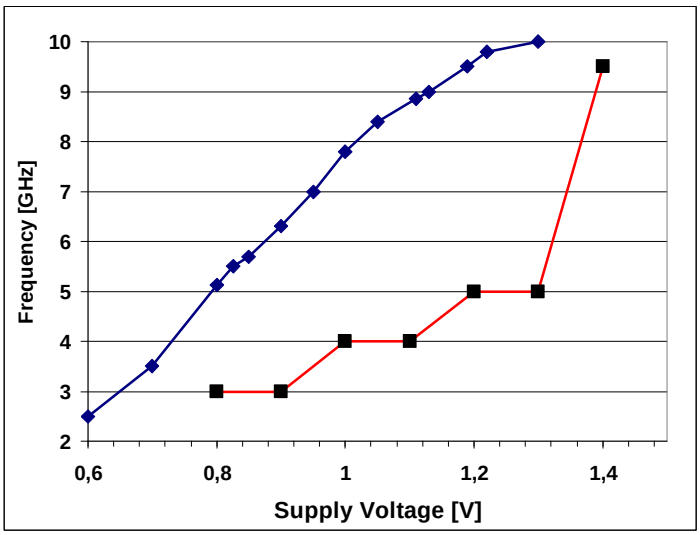
La mesure du circuit a donc été réalisée. Le vecteur de test est une impulsion car la réponse à impulsion caractérise entièrement le système linéaire qu'est le FIR. Il est commun de mesurer la fréquence maximale de fonctionnement à une tension d'alimentation donnée. Ce type de digramme est nommé « diagramme de Schmoo ».

Clock @ 16 dBm	0,8	0,9	1	1,1	1,2	1,3	1,4	1,5
500M	14mA	17mA	20mA	22mA	25mA	29mA	32mA	36mA
1G	24mA	28mA	33mA	37mA	42mA	47mA	52mA	58mA
2G	45mA	52mA	59mA	67mA	75mA	84mA	93mA	104mA
3G	65mA	75mA	85mA	97mA	109mA	121mA	135mA	150mA
4G			111mA	126mA	142mA	160mA	178mA	198mA
5G					179mA	200mA	222mA	247mA
6G							264mA	293mA
7G							308mA	343mA
8G							349mA	390mA
9G							390mA	438mA
9G5							408mA	460mA
10G								
11G								

Clock @ 19 dBm

Tableau : Mesure du circuit FIRST. Pour différentes tensions d'alimentation le circuit est mesuré jusqu' à sa fréquence maximale de fonctionnement. La consommation du circuit est rapportée pour les différents points.

Le circuit fonctionne jusqu'à la fréquence de 9.6 GS/s à une tension d'alimentation de 1.4V alors qu'il était conçu pour fonctionner à 10 GS/s sous 1V. Différentes pistes peuvent être avancées pour expliquer cette différence de fonctionnement. Les caractéristiques en simulation et en mesure sont reportées dans la figure ci-dessous.



Cette figure présente la fréquence de fonctionnement maximum pour une tension d'alimentation donnée, en simulation – courbe bleue et en mesure – courbe rouge.

La courbe bleue en simulation est assez linéaire mais on peut remarquer une tendance à se stabiliser à partir de 1.2V. En d'autres termes, la fréquence de fonctionnement n'évolue plus linéairement avec une augmentation de la tension d'alimentation. Ceci s'explique simplement par la transconductance du transistor. On peut remarquer nettement cet effet dans la Figure 3-59.

La courbe rouge en mesure n'évolue pas avec la même pente. On remarquera nettement une partie qui évolue de manière linéaire (0.8V - 1.2V) et un décrochage a partir de 1.3V. Différentes pistes peuvent expliquer cette réponse mais la plus avancée aujourd'hui vient d'une défaillance de la génération d'horloge. En simulation il a été remarqué que le driver d'horloge d'entrée ne peut fonctionner à 10 GHz qu'a une tension d'alimentation de 1.3 V. Ensuite il semblerait que l'arbre d'horloge ne soit pas à même de fournir une horloge à haute fréquence suffisamment propre au FIR. On peut donc avancer comme première explication que la génération d'horloge serait à revoir. Ensuite le TSPCFF et la logique CPL sont très sensibles aux variations d'alimentation. Aussi on peut penser que des variations d'alimentation causées par le circuit RLC d'accès changent la caractéristique du circuit.

Il est important de pouvoir comparer ces résultats à d'autres travaux. La comparaison la plus proche à l'état de l'art peut être faite avec un filtre semi-numérique dans une technologie SiGe réalisé pour une application similaire. Cette architecture est décrite dans [Ellinger10]. La majeure différence est que cette architecture est semi-digital car la sommation du FIR est faite dans le domaine analogique, ce circuit ne peut donc pas

être mis en place avec une structure tel le DRFC. Les inconvénients majeurs de ce circuit comparé au notre sont les suivants:

- Il est sensible aux variations d'horloge dans le sens où le jitter va changer la réponse fréquentielle du filtre.

- Ses spécifications sont plus simples, le circuit fonctionne pour un masque spectral relâché et une modulation type QPSK.

- Une grande consommation, ce circuit consomme près de 1W

- Ce circuit est réalisé dans une technologie plus coûteuse.

Le tableau ci-dessous synthétise les performances du circuit proposé par [Ellinger10] et compare ces performances par rapport aux mesures de notre circuit.

	[Ellinger10]	This thesis
Technology	0.25um SiGE HBT	65nm CMOS STM
Fsample (GHz)	7	9.6
Number of taps	17	18
Attenuation (dB)	19 @ 2.2 GHz	40 @ 2.2 GHz
Power consumption (mW)	999	400 @ 1.4 V
Area	~0.8 mm2 (estimate)	0.1 mm2

Ce tableau compare les performances des travaux de [Ellinger10] et les notre.

Chapitre 5

Ce chapitre 5 est la conclusion du document mais aussi le moment de présenter certaines perspectives.

La perspective la plus probable est la réalisation du baseband d'un émetteur avec l'intégration du FIR et d'un DAC. Une ip DAC a été fournie par le BWRC. Ce DAC fonctionne jusque 5 GS/s. Aussi les FIR sont utilisés à une fréquence réduite. Ce système va néanmoins permettre de valider l'architecture proposée jusqu'au mixer. Pour des raisons de test, des ADC à approximation successive sont utilisés afin de générer un signal numérique depuis un générateur externe. L'idée est bien entendu de fournir des symboles OFDM puis de les numériser pour les passer à travers le FIR et DAC. L'ADC est une ip fournie par STMicroelectronics. Cette architecture a été mise en œuvre jusqu'au layout mais pas fabriquée.

Les caractéristiques des blocs sont présentées dans le tableau ci-dessous:

Block	Architecture	Size [um^2]	Sampling Frequency	ENOB	Power
ADC	Successive approximation	610 x 472	1.25 GS/s	9	
FIR	Interpolator	650 x 170	2.5 GS/s and 5 GS/s	7	100 mA
DAC	Current steering	275 x 250	5 GS/s	7.5	

Ce tableau présente les caractéristiques des différents blocs mis en œuvre pour la réalisation du baseband complet d'un émetteur à 60 GHz

Le système complet (nommé AC/DC) est présenté dans la figure ci-dessous ainsi que la layout associé. Il se compose en I/Q d'un ADC à approximation successive, d'un FIR et d'un DAC. L'ADC converti des symboles OFDM à la cadence de 1.25 GS/s, ceux-ci sont sur-échantillonnés et filtrés par le FIR et convertis à la fréquence de 5 GS/s.

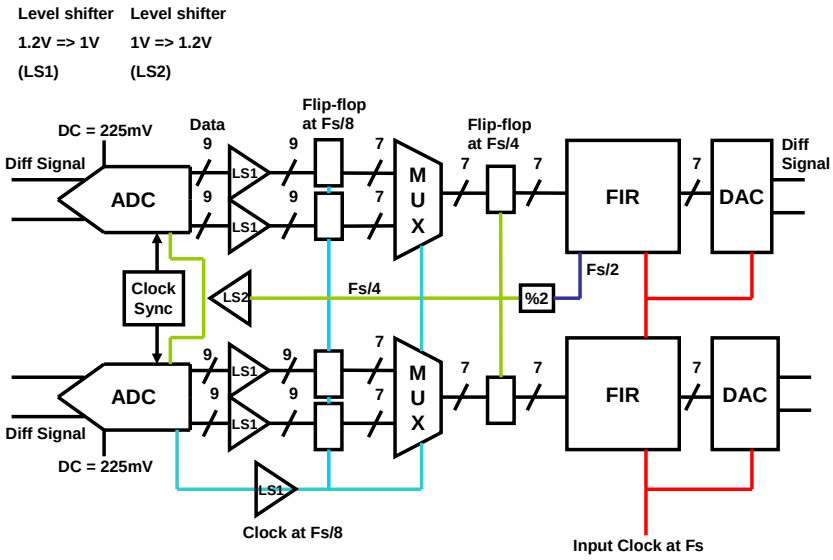
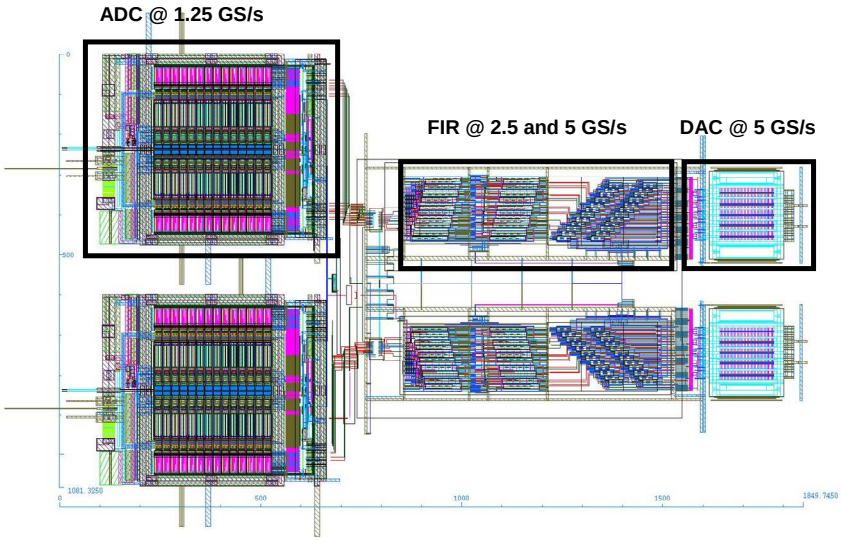


Illustration du système complet.

A noter que l'ADC fonctionne à 1.25 GS/s et offre à sa sortie deux trains de 9 bits à 625 MS/s. Ces signaux représentent le canal gauche et droit de l'ADC. Ces signaux doivent être remis en série jusqu'à la fréquence de 1.25 GS/s.



Layout du second circuit

Pour ce qui est des autres perspectives, la réalisation du DRFC reste un challenge. Le standard a aussi changé ces derniers temps et offre aujourd'hui une version simplifiée du standard étudié 4 ans en arrière. Une perspective serait de réadapter le FIR en simplifiant sa conception selon ce standard et pourquoi pas même dans une technologie plus avancée (par exemple 32nm) afin de réduire la consommation.

Conclusion

Cette thèse propose l'étude d'un émetteur à 60 GHz avec des capacités de radio logicielle. Dans un premier temps (chapitre 1) l'état de l'art actuel présenté montre que seul des solutions analogiques sont mises en place pour des émetteurs à cette fréquence. Néanmoins on trouve dans la littérature des solutions numériques à plus basse cadence. Nous proposons dans cette thèse de numériser une chaine d'émission à 60 GHz en se basant sur les concepts en radio logicielle présentés à plus basse cadence. Ensuite une étude système est réalisée afin de valider l'architecture proposée dans cette thèse. L'étude se concentre sur un filtre interpolateur numérique à la fréquence de 10 GHz. Ce filtre est à même de réaliser en bande de base la fonction de filtrage de toute la chaine. Le chapitre 3 se concentre sur la réalisation d'un point de vue circuit de ce bloc avec une étude poussée de différentes cellules afin d'optimiser la vitesse. Enfin le chapitre 4 fait face à la mise en place d'un système de mesure pour l'interpolateur et présente les résultats de mesure de ce bloc. Le chapitre 5 propose certaines perspectives à cette thèse.

Résumé : Emetteur à 60 GHz avec des possibilités radio logicielle

Mots clef : Radio logicielle, Ondes millimétriques, Radio – Émetteurs et transmission, Radiofréquences, Traitement du signal – Techniques numériques, Filtres numériques, Systèmes de télécommunications à large bande, MOS complémentaires, Convertisseurs numérique-analogique

La radio à 60 GHz émerge comme l'un des candidats les plus prometteurs pour la transmission de données à haut débit (10 Gb/s) sur des courtes distances (1 à 10m). La radio 60 GHz à l'état de l'art utilise des émetteurs-récepteurs exclusivement analogiques.Les technologies CMOS sub-microniques profondes ont permis le développement de circuits de bande de base numériques pour les communications sans fil à plus basse fréquence. Dans ce travail une architecture d'émetteur numérique destinée aux communications à 60GHz a été étudiée. Elle est basée sur un interpolateur numérique et un DRFC (convertisseur direct numérique-RF), structure qui associe un DAC et un mélangeur pour réaliser une conversion directe du flux de données numériques à la fréquence RF. Le standard IEEE 802.15.3c pour communications sans fil à 60 GHz a été pris comme référence pour étudier l'émetteur proposé. Le flux de données numérique à la sortie en bande de base (échantillonnés à 2,5 Géch / s) doit être sur-échantillonné, et les répliques du signal aux multiples de la fréquence d'échantillonnage initiaux doivent être filtrés. Ces images sont atténués avec un interpolateur filtre FIR fonctionnant à 10 Gech/s. Un prototype de l'interpolateur à 10Gech/s a été implémenté dans une technologie CMOS 65nm pour prouver la faisabilité du concept. Le filtre utilise des coefficients « puissances de deux » et de la logique dynamique pour atteindre le taux d'échantillonnage requis. Le circuit prototype de ce transmetteur démontre la pleine fonctionnalité jusqu'à 9,6 GHz et consomme 408mA (571mW) avec une tension d'alimentation de 1.4V. La surface de silicium centrale est de 650 x 170 um2.

Abstract : 60 GHz transmitter with SDR capabilities

Key words : Digital radio, mm Wave, RF transmitter, RF, digital signal processing, large band transmitter, CMOS, digital-to-analog converter.

Recent deep sub-micron CMOS technologies have allowed the development of digital baseband circuits for wireless communications. 60 GHz radio has emerged as one of the most promising candidates for high-data-rate (10 Gb/sec), short-distance (1 to 10 m), wireless telecommunication systems. State-of-the-art 60 GHz radio use exclusively analog transceivers. Recent deep sub-micron CMOS technologies have allowed the development of highly digital transceivers for wireless communications in the lower GHz range. In this work, a digital transmitter architecture targeted at 60GHz c communications has been studied. It is based on the combination of an interpolator and a DRFC (digital-to-RF converter), structure which combines a DAC and mixer in order to realize a direct conversion of the digital data stream to the RF frequency. The 60 GHz wireless standard IEEE 802.15.3c has been taken as a reference to study the proposed transmitter. The digital data stream at the baseband output (sampled at 2.5 GS/s) needs to be oversampled and resulting replicas of the signal at multiples of the initial sampling frequency have to be filtered. Images at multiples of the initial sampling frequency are attenuated with an interpolator FIR filter working at 10 GS/s. A prototype of the 10GS/s interpolator has been implemented in a 65nm CMOS technology to prove the feasibility of the concept. The filter uses powers of two coefficients and dynamic logic to reach the required sampling rate. The fabricated prototype transmitter IC demonstrates full functionality up to a 9.6 GHz and consumes 408mA (571mW) with a 1.4V supply voltage. The core area is 650 x 170 um2.