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BAPTISTE GRAVE

Techniques de Sous-Échantillonnage Appliquées aux Recepteurs Radio à 60 GHz en Technologie 28 nm CMOS

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SUMMARY

Subsampling techniques applied to 60 GHz radio receivers in 28 nm CMOS technology

This thesis presents an IF to DC receiver based on subsampling for 60 GHz applications. A particular arrangement of the frequency plan allows embedded anti-alias filtering. Down-conversion, channel filtering and IQ demodulation are merged into a unique operation at no extra cost in terms of area and power consumption.

The theoretical analysis of the proposed charge-domain quadrature subsampler and its integration into a complete 60 GHz receiver is detailed in this thesis. Advanced analysis is made for critical points of the architecture: generation of the integration windows, IQ demodulation, noise folding and effect of clock jitter. The proposed architecture is validated by simulations and complies with the requirements of the standards for 60 GHz wireless communications. The result of this study shows that sub-sampling is suitable for high bandwidth and high data-rate receiver systems.

A prototype has been designed in 28 nm CMOS technology. It shows that the subsampling operation is fully functional up to the frequency of interest : sampling at 7.04 GHz an RF signal around 21.12 GHz. Modulated BPSK and QPSK data streams at 1.76 GHz can be received with a BER below 10^{-3} for input powers from -10 dBm to 5 dBm. Measurements have also shown that adjacent channels at power equivalent to the channel of interest can be tolerated with only small degradation of the bit error rate thanks to charge domain subsampling architecture.

RÉSUMÉ

Techniques de sous-échantillonnage appliquées aux récepteurs radio à 60 GHz en technologie CMOS 28 nm

Cette thèse présente un récepteur IF vers DC basé sur le sous-échantillonnage pour applications à 60 GHz. Un arrangement particulier dans le plan de fréquence autorise l'intégration du filtrage canal directement à l'intérieur de l'échantillonneur. La conversion basse, le filtrage canal ainsi que la démodulation IQ sont rassemblés en une seule opération sans cout additionnel en termes de surface ou de puissance.

L'étude théorique de l'échantillonneur en courant et son intégration dans un récepteur complet à 60 GHz est détaillée dans cette thèse. Une étude avancée est faite pour les points critiques de l'architecture : la génération de la fenêtre d'intégration, de la démodulation IQ, du repliement de bruit ainsi que de l'effet de la gigue de l'horloge d'échantillonnage. L'architecture proposée est validée par des simulations et remplit les contraintes données par les standards définis pour les communications autour de 60 GHz. Le résultat de cette étude système est que le sous échantillonnage est une technique applicable pour les systèmes à large bande passante et à cadence de données élevé.

Un prototype a été développé en technologie 28nm CMOS. Il montre que l'opération de sous-échantillonnage est fonctionnelle à la fréquence d'intérêt : échantillonnage à 7.04 GHz d'un signal RF autour de 21.12 GHz. Un flux de données BPSK ou QPSK à 1.76 GHz peut être décodé avec un taux d'erreur binaire inférieur à 10^{-3} pour des puissances d'entrée entre -10 et 5 dBm. Les mesures ont également montré que le système est capable de tolérer des canaux adjacents à une puissance équivalente à celle du canal d'intérêt avec seulement une petite dégradation du taux d'erreur binaire grâce aux échantillonneurs en courant.

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En somme des compères que l'on n'oubliera pas.

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INTRODUCTION

Since the introduction of the indoor wireless communication in 1990, there has been a constant demand for higher data rates. To answer this demand, new standards of communication around 60 GHz have been developed. At the same time, the customers need more and more mobility. Regarding this needs the target of this thesis is defined as the creation of a solution able to match the 60 GHz standard while reducing the global power consumption in order to include high data rate wireless communications in mobile devices. The manuscript is organized as follows.

Chapter 1 introduces the evolution of wireless communications since the late 90's and details the first version of the standard for the 60 GHz band. The evolution of the state of the art of 60 GHz wireless receivers is detailed. This shows that years after years, more and more building blocks have been integrated.

Chapter 2 touches on the proposed approach : the subsampling. It is a well-known technique in wireless communications, however it has never been used for carrier frequencies higher than few GHz. A solution is proposed to integrate subsampling in 60 GHz receivers. A theoretical study of the feasibility of such a receiver is detailed to discuss the critical points such as noise folding and sampling jitter.

Chapter 3 details the silicon implementation of the prototype. It goes from a basic sampler to the architecture that has been implemented in 28 nm CMOS. Layout issues in such technological node are detailed such as mismatches between paths or how to deal with parasitics. For a continuous time operation of the samplers, a defined pattern has to be generated. This results in the clock tree that have been integrated on-chip. Finally the architecture has been simulated at transistor level to validate the functionality of the system.

Chapter 4 presents the measurements that have been done on the system. Several parts have been successively tested : downconversion, demodulation of BPSK and QPSK signals and finally the attenuation of outband blockers.

Chapter 5 closes this manuscript with a comparison of the designed prototype with the solutions that have been proposed in the state of the art between 2009 and 2013. Prospects based on this prototype are also introduced : hardware convergence of Wifi and WiGig with automated synchronization

CHAPTER

1

FROM WIFI TO GIGABIT WIRELESS

I. Introduction

I.A. Evolution of WLANs

Since the introduction of the Wireless Local Area Network (WLAN) technology in the late 1990s, there has been a constant demand for higher data rates.

In 1997, the first standard for WLAN was published. Figure 1.1 shows the evolution of the 802.11 standard since the first version.

The first version defines a communication over 20 MHz bandwidth over a 2.4 GHz carrier for 20m of indoor range. However direct sequence spread spectrum (DSSS) limits the data rate to 2 Mbps.

In 1999, the first amendment defines the 802.11a. The spectral efficiency have been increased because the DSSS has been abandoned in favor of OFDM. It operates around 5 GHz because the 2.4 GHz band was heavily used in 1999.

The same year, another amendment was made. In the 802.11b, the DSSS is still used but the complementary code keying (CCK) is added and improves the performance of the communication. Consequently, the maximum data rate is now 11 Mbps in this band.

In 2003, the two first amendments were merged into the 802.11g. This new version can support both 802.11a and 802.11b communication modes but the carrier frequency is kept at 2.4 GHz.

In 2009, the 802.11n is the first amendment which uses Multiple Inputs Multiple Outputs (MIMO). This technique uses multiple antennas in order to use multiple streams at the same time. Complex modulations schemes are used (up to 64-QAM). Moreover, the channels can now be 40 MHz compared to only 20 MHz before. As a result, the maximum theoretical data rate is now 600 Mbps while using 4 streams of 40 MHz.

In 2014, the official amendment 802.11ac will be made. The number of allowable MIMO streams will go up to 8. The carrier will go up to 5 GHz which will enable channels up to 160MHz wide. The 256-QAM modulation scheme is allowed. The maximum theoretical data rate is 6930 Mbps while using 8 streams of 160 MHz.

This growth is saturated because the allocated band is limited : 83MHz around 2.4GHz and 200MHz around 5.25 GHz. Moreover, the latest versions of the standard offer interesting

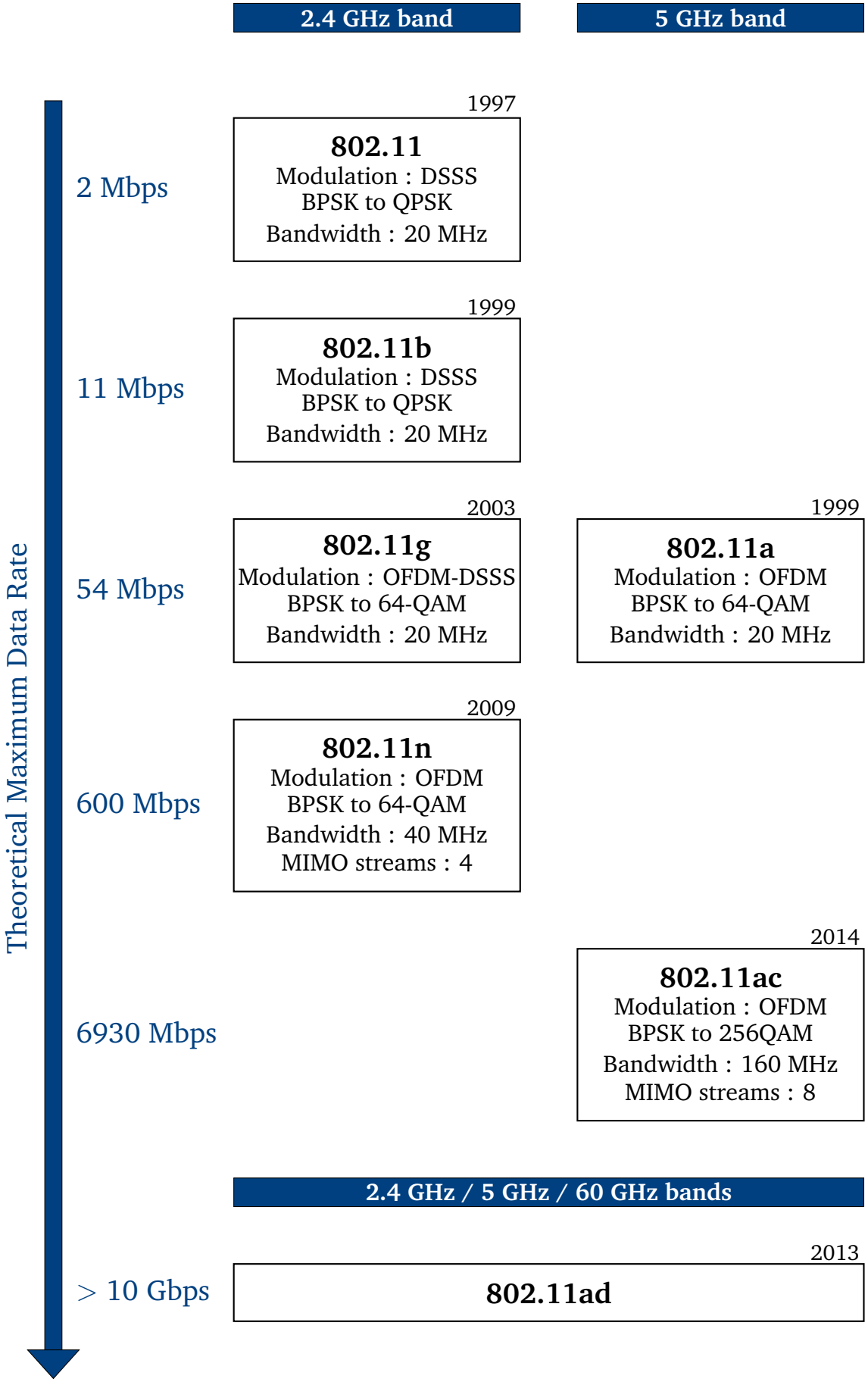


Figure 1.1: Evolution of the 802.11 standard

data rates but they use the whole available band which can be annoying because nobody else can use this band of frequency at the same time.

Consequently, a higher bandwidth standard is necessary to meet the ever increasing data transfer needed. One solution to answer this demand is to use frequency in which large bandwidth are available. It is the case around 60 GHz The amendment 802.11ad is the first which uses these frequencies. With such wide bandwidth, data rates higher than 10 Gbps can be reached.

I.B. Why do we need ever increasing data rates?

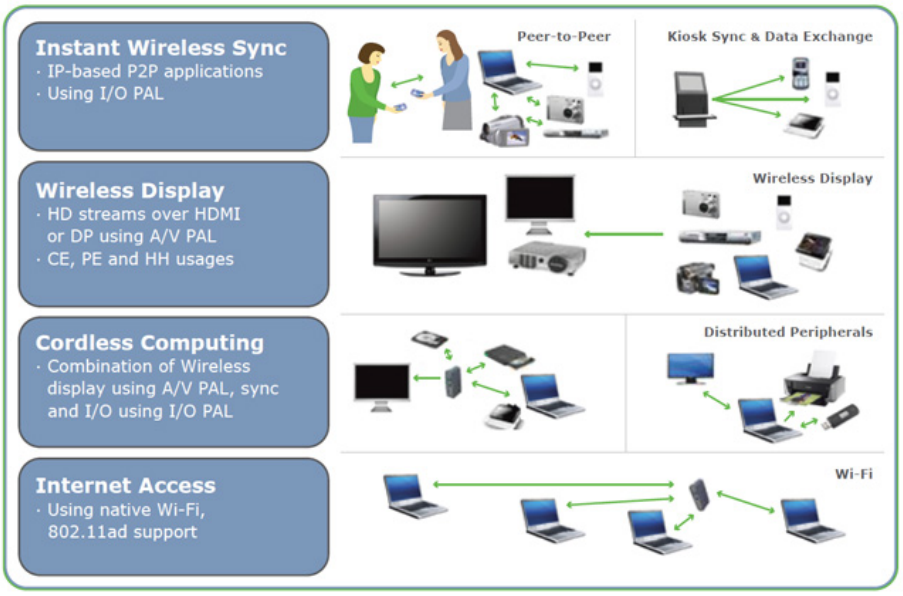


Figure 1.2: Use cases of high data rate wireless applications (http://www.extremetech.com)

Figure 1.2 shows several applications which require high data rates. It is divided into four major categories:

- Wireless synchronization between two devices :

Concerning the data transfer between two devices, if you want to transfer a 2-hour BlueRay movie you will need around 1.4 minutes with 802.11n while it will take less than 12s with a 3 Gbps link and less than 6s with a 6 Gbps link. Who would accept to wait more than a minute to download a movie on his handheld device? The consumer patience for this operation is more in the 10s range than in the minute range.

- Wireless display of high definition video :

Concerning video streaming, why do we need to have ontime uncompressed video stream.

The delay introduced by the compress-decompress operation is not compatible with a live video game, especially when move to the 3D video versions. Uncompressed video stream seems to be the solution for such application.

- Cordless computing and high speed wireless Internet connection

Regarding cordless computing and Internet access, the question is more open, as the router is connected to the Ethernet with low and medium data rates with optic fiber being deployed in the urban environment, with very high data rate capability. The WLAN should follow this evolution. At the same time, we can imagine transmission between two devices in the same LAN at very high data rate, without using a WiFi channel.

II. The standards for the 60 GHz band

II.A. Regulatory Status

In 2006, the standard IEEE 802.15.3c [5] has been published. It defines the foundations of 60 GHz wireless communications.

In order to address the high demand in terms of data rates, 9 GHz of unlicensed band has been opened by the Federal Communication Commission (FCC) in 2001. This band has been exploited for a long time for military purposes. It is now open for commercial use without license. The regulatory status is summarized in Figure 1.3

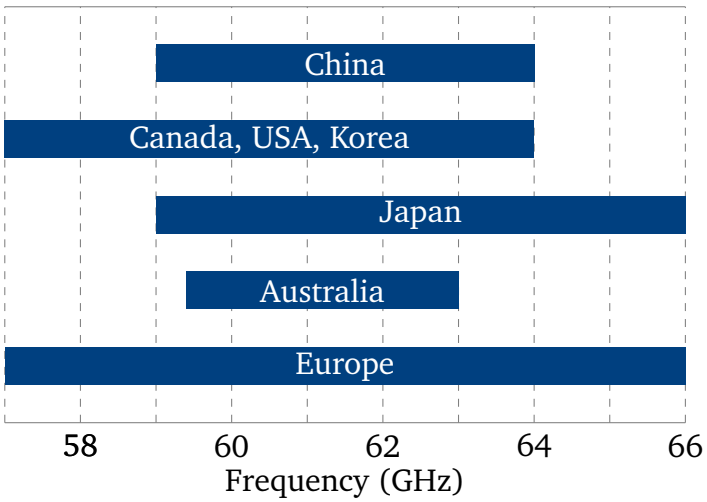


Figure 1.3: Worldwide available spectrum around 60 GHz [5]

II.B. Channelization

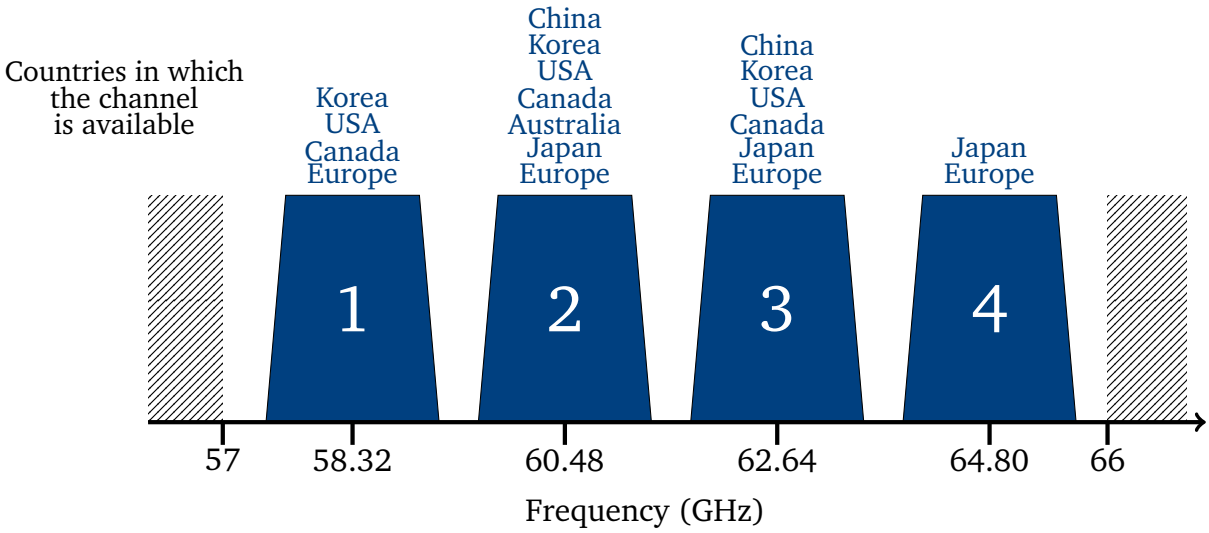


Figure 1.4: Channelization of the 802.15.3c standard [5]

Many companies created their own standards for specific use cases after 2006 : WiHD, ECMA-387 and WiGig. They all follow the IEEE 802.15.3c standard for the channelization. Four channels are defined. The center frequencies are shown in Figure 1.4. The channel spacing is 2.16 GHz. Each channel is 1.76 GHz wide. In Europe, the four channels are defined in the 57 - 66 GHz band while in the rest of the world, some of the channels are not available due to the regulatory status.

II.C. Physical Layer

Three different physical models are defined in [5] :

Single Carrier (SC). It intends to cover systems with a high degree of flexibility in order to allow implementors the ability to optimize for different applications. Three classes of modulation and coding schemes (MCSs) target different wireless connectivity applications. These classes are defined in the following section.

High Speed Interface. This mode is designed for devices with low-latency, bidirectional high-speed data and uses orthogonal frequency domain multiplexing (OFDM). It supports a variety of MCSs using different frequency-domain spreading factors, modulations, and low density parity checks block codes. The data rate could be higher than 5 Gbps which is equivalent to the SC mode but the spectral occupation is lower using OFDM.

Audio / Visual mode. Typical video and audio consumer electronics are configured either as a source of data, e.g., a video disc player, or as a sink, e.g., a display. For these applications, the data flow is highly asymmetric. Thus the Audio/Visual (AV) is implemented with two different modes, the high data-rate and low data-rate, both of which use orthogonal frequency domain multiplexing (OFDM). The data rates goes from 0.952 Gbps to 1.904 Gbps for the high data-rate and from 1.5 to 10.2 Mbps for the low data-rate.

In this work, the target is to implement high frequency wireless links for mobile devices. Targeting mobile devices means that the system design should be aware of the power consumption. Systems using OFDM have to include Fourier transforms and inverse Fourier transforms which are quite complicated to implement, need high signal to noise ratio and are quite expensive. Consequently, this thesis focuses on the single carrier transmission mode.

II.D. Classes defined in the Single Carrier mode

In the single carrier transmission mode, several modulations are allowed. Each class defined for the single carrier transmission mode (Section II.C.) uses a proper modulation scheme and enables consequently a defined data-rate.

Class 1 is specified to address the low-power low-cost mobile market while maintaining a relatively high data rate of up to 0.88 Gbps. Class 2 is specified to achieve data rates up to 3.3 Gbps. Class 3 is specified to support high performance applications with data rates in

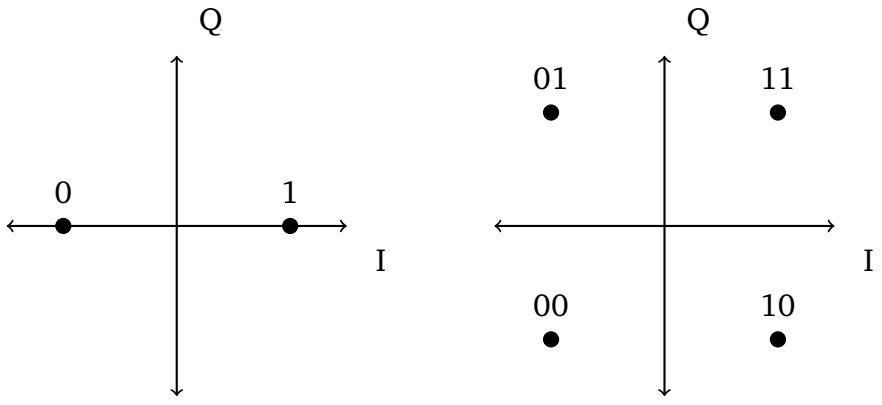
excess of 5 Gbps.

The first class (lowest data rate) uses the simplest constellation : binary phase shift keying (BPSK). The second class uses quadrature phase shift keying (QPSK). The third class uses 8 phases shift keying (8-PSK) and 16 quadrature amplitude modulation (16-QAM). The higher the modulation, the higher the needed signal to noise ratio (SNR). In order to receive the signal with an acceptable bit error rate (BER), the received SNR should be high enough.

Table 1.1 sums up the three classes with their corresponding modulation schemes and the data rate possible in the configuration. This thesis focuses on the first two class which use modulations shown in Figure 1.5.

Class	**Modulation**	**Data-rate**
1	BPSK	From 0.025 to 0.88 Gbps
2	QPSK	From 1.76 to 3.3 Gbps
3	8-PSK or 16QAM	From 3.96 to 5.28 Gbps

Table 1.1: Classes defined in the standard, modulation schemes and data-rate.



(a) BPSK for Class 1 (b) QPSK for Class 2

Figure 1.5: Ideal constellations for single carrier transmission modes (class 1 and 2)

III. State of the art of 60 GHz receivers from 2001 to 2009

Since the opening of the 60 GHz band for commercial use, publications intend to implement more and more elements of a receiver in the same chip. This part of the manuscript shows the evolution of the state of the art from first solutions based on III-V semiconductors to the most advanced solution based on CMOS technology in 2009. This state of the art spans the period preceding the beginning of this thesis work. Latest developments will be detailed in Chapter 5.

III.A. First solutions based on III-V semiconductors

Figure 1.6 shows the evolution of the maximum application frequency of CMOS and Si-Ge with the transistor size.

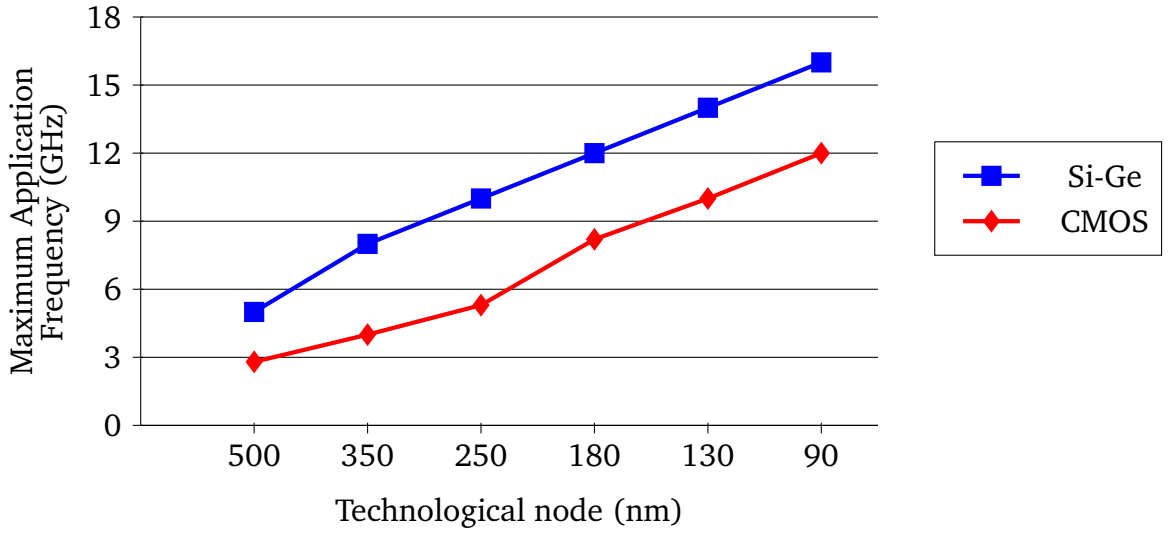


Figure 1.6: Maximum application frequency for CMOS and SiGe by transistor size ($f_T/8$) [6]

For a given technological node, the frequency of operation has always been higher for Si-Ge materials than for CMOS. Consequently, first solutions proposed for 60GHz communications are based on Si-Ge [7]-[8]. These papers integrate the basic blocks of 60GHz receivers: a low noise amplifier and a RF mixer. It shows that it is technically possible to use the 60GHz band for high data rate communications.

Si-Ge technology can operates at a higher frequency for a given technological node than CMOS. Meanwhile, it shows several drawbacks. Si-Ge typically requires more masking steps than conventional CMOS. This generally results in higher wafer costs and slower manufac-

turing cycle times. Moreover, the yield decreases while the number of masks increases. 60 GHz communication systems would require, a lot of processing to be integrated on-chip. Consequently, CMOS would offer a more interesting alternative for 60 GHz transceivers.

III.B. CMOS process: a suitable solution for 60GHz communications

After 2006, the progress of the CMOS technology enables the design of 60GHz transceivers. The receiver part of the first solutions in the 90nm node proposed in [9]-[10] is based on the same architecture presented in Figure 1.7. This is a very simple solution from an architectural point of view.

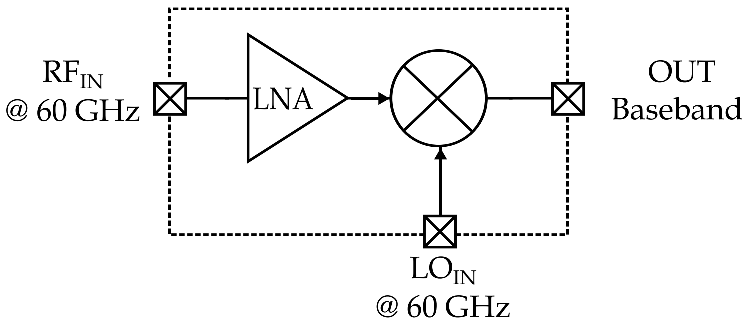


Figure 1.7: First implementation of direct conversion receivers for 60GHz

The radio frequency (RF) signal is mixed with a 60GHz off-chip local oscillator (LO) so the signal is directly demodulated around the baseband. The conversion gains of these solutions are around 15dB for a noise figure around 8dB. These first papers ([9]-[10]) demonstrate that CMOS is a valuable candidate for the implementation of complete transceivers for 60GHz communications.

III.C. First on-chip locals oscillators

The next step leading to a complete receiver is to add the on-chip LO. A direct-conversion receiver requires the generation of quadrature LO phases at 60 GHz which is still a difficult task considering the state of the art of inductors at these frequencies [11]-[12]. A solution to relax these requirements is to implement a lower frequency voltage-controlled oscillator (VCO) together with a frequency multiplier. A first solution has been proposed in 2007 [13] and is represented in Figure 1.8.

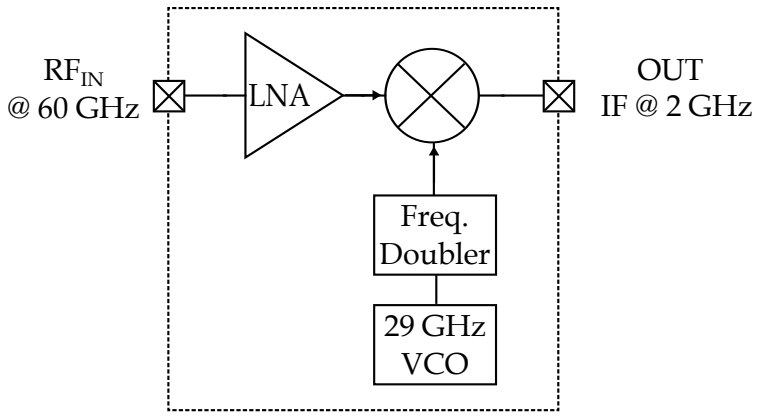


Figure 1.8: Direct Receiver based on 29 GHz LO

The system is a direct conversion receiver which includes a 29 GHz VCO and a frequency doubler in order to create a 58 GHz LO. This architecture suffers from one major drawback: typical doubler topologies do not produce quadrature outputs. Consequently the input signal can not be downconverted directly to DC because in these conditions, demodulation and image rejection would be impossible. In [13], the 60 GHz signal is thus down-converted around a 2 GHz low-IF and the IQ demodulation is performed with off-chip mixer with an additional quadrature oscillator.

III.D. Embedded IQ separation

A solution to suppress this frequency doubler is to use a 30GHz quadrature VCO (QVCO) in a basic heterodyne structure. Meanwhile, while using this architecture for complex signals, the 3rd harmonic of the VCO creates a mirrored replica in the band [14].

To get rid of this effect, the two successive mixers should not work with complex signals. The solution proposed in [14] is shown in Figure 1.9. It adds a poly-phase filter which separates the input RF signal into I and Q channels. This solution achieves a conversion gain up to 22dB while keeping a noise figure of 7dB. This noise figure is equivalent to the results of previous solutions: 8dB, presented in Section III.B. for [9] - [10].

The main drawback in this architecture is that the poly-phase filter is based on passive devices: resistors and capacitors. Matching is a critical point in sub-micron technologies especially with passive devices at such high frequencies. This matching problem in the poly-phase filter results in mismatches between I and Q, that can be compensated in the digital baseband circuitry.

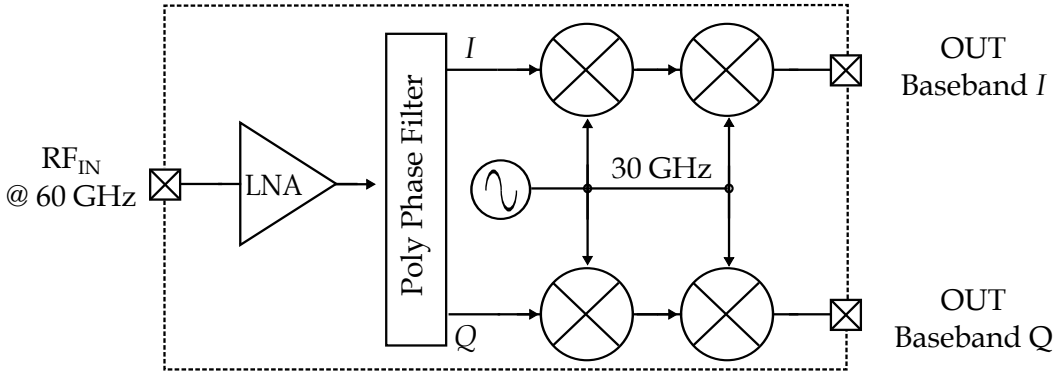


Figure 1.9: Heterodyne Architecture using 30GHz VCO and poly phase filter

III.E. Most advanced solution in 2009

The first solution which embeds a 60 GHz LO is presented in [15]. The system is based on a direct conversion receiver targeting binary phase-shift keying (BPSK) modulation scheme. This simple modulation is used to get rid of problems due to the distribution of the quadrature LO. This receiver is integrated in a full transceiver which reaches up to 6Gbps over a 2 meters wireless link.

In December 2009, the most advanced solution is presented in [16]. As shown in Figure 1.10, this paper mixes the interesting points from the two previous works. A VCO is implemented and integrated in a PLL as presented in [15]. They get rid of the routing of quadrature clock routing by adding a quad hybrid in the RF path in order to separate I and Q as presented in [14].

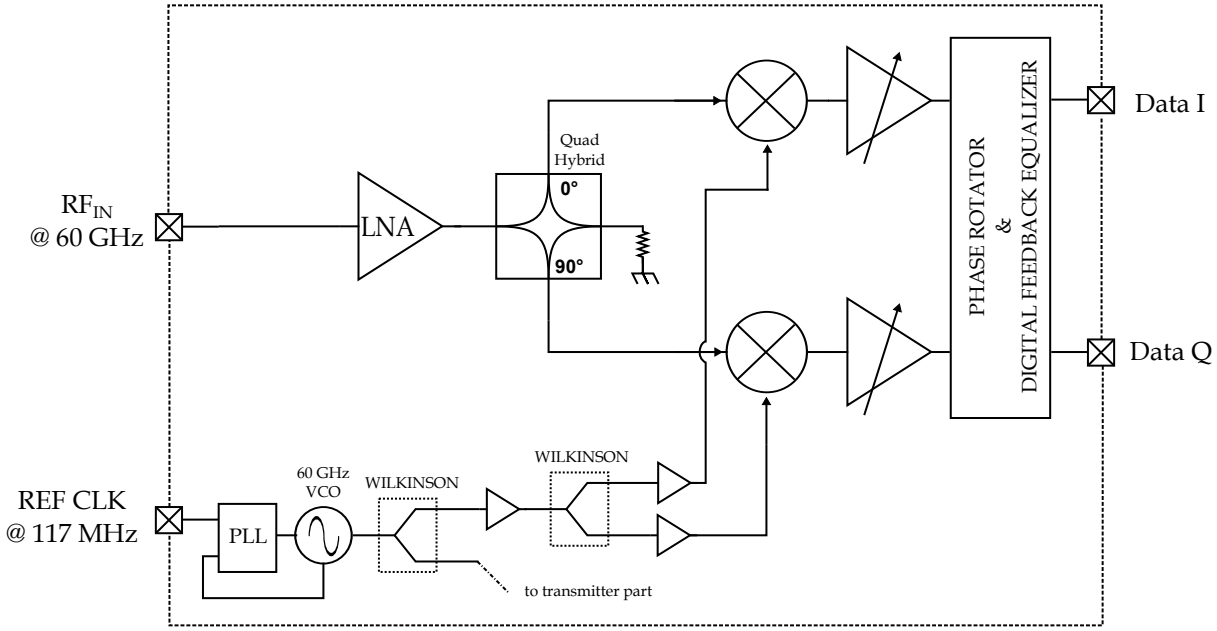


Figure 1.10: Direct receiver including PLL and BB processing

The main added value of this paper is the implementation of baseband processing on-chip. The phase of the VCO is virtually set in baseband thanks to the phase rotator. The effects of the channel are compensated by a digital feedback equalizer. All these techniques push the maximum obtained data rate to 10Gbps for a power consumption of 138mW.

IV. Conclusion and objective of this work

During the last decade, CMOS gate lengths have shrunk, gate oxide thicknesses have decreased, and power supply voltages have dropped. These improvements have provided increased die density, faster transistors and lower power consumption. It made CMOS technology a valuable solution for fully integrated 60 GHz transceiver. However, scaled CMOS for analog circuits does not provide an obvious benefit because the passive components do not scale and are harder to match. That is why research focuses on solutions to reduce the effect of these mismatches and to correct these drawbacks.

Proposed CMOS solutions [9]-[16] try to embed more and more parts of the receiver on-chip. In the state of the art, down-conversion chain, PLL and BB processing are on the same chip. Another issue in this state of the art is how to demodulate I and Q. For high frequency VCOs, the I/Q split is not done on the clock path but in the RF path in order to limit the problems of clock routing. Maximum data rates reached are 10 Gbps for a complete transceiver solution. Meanwhile, the solutions [7]-[16] do not comply with the WiGig standard [5] which has been finalized in 2008. For example, they are not able to reach all four channels defined in the standard.

The first idea of this thesis was to think about the interface between the analog radio signal and the digital baseband stream with a more global approach than a classical receiver followed by an ADC.

The target is to take advantage of analog sampled signal processing to reduce the power consumption and the cost of a RF receiver with an optimized approach based on subsampling. This sampling technique is well know in RF systems but has never been used at such high frequencies. This approach proposes to include channel filtering, direct down-conversion and direct IQ-decoding directly inside the receiver by exploiting its properties.

For demonstration purposes, this thesis focuses then on a short distance line-of-sight communications that do not need multi-path equalization. This type of situation could occur in practice with mobile terminals i.e. for fast video downloading.

CHAPTER

2

THEORETICAL STUDY

I. Introduction

First, this section introduces the basics of subsampling starting from an example and going to the theoretical point of view. This technique is well known in RF receivers, consequently, the second part of this section reports architectures in which the subsampling has been used.

I.A. What is subsampling?

I.A.1 Starting from an example...

The very first rule of the sampling theory is that the signal should be sampled at a rate at least two times higher than the signal frequency: $2f_{SIN}$ for a sine wave around f_{SIN}. This minimum sampling frequency is called "Shannon Frequency".

Assume a sine wave at $f = 20\ GHz$ sampled at $f_{SUB} = 4.88\ GHz$. In these conditions, the Shannon Frequency is not respected because $f_{SUB} < f$.

Figure 2.1 shows the result of this operation in time domain. The blue (plain) sine wave is the original signal, the red one (dotted) is the resulting signal after subampling. This new sine wave appears at a lower frequency: 480 MHz.

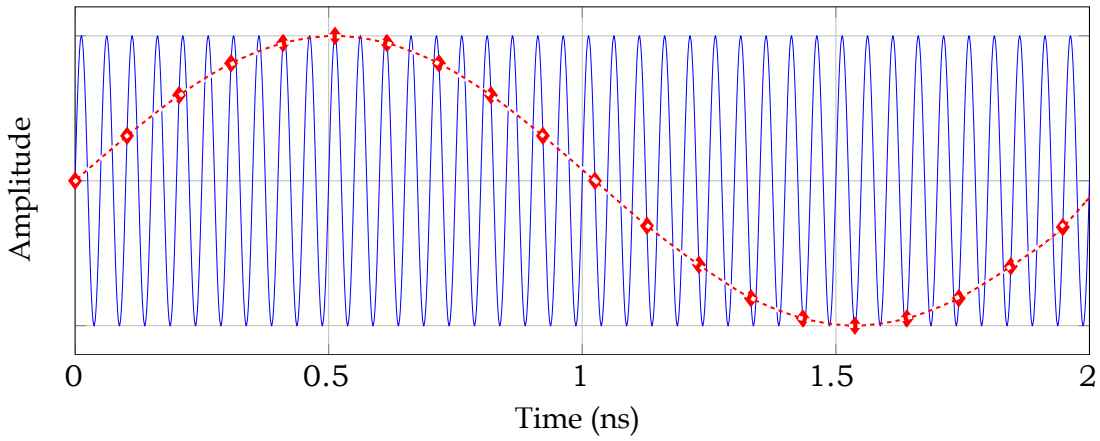


Figure 2.1: Time domain illustration of the subsampling

I.A.2 ..to a theoretical point of view

The process of sampling the input signal at a rate lower than the highest frequency components of the input signal, commonly referred to as subsampling, performs a function equivalent to a mixing operation. In the frequency domain, subsampling results in spectral images

replicated at multiples of the sampling rate. Equation 2.1 shows where these images are located [17].

$$f_{image} = n \cdot f_{SUB} \pm f_{IF} \tag{2.1}$$

where f_{image} is the location of the image, f_{SUB} is the subsampling frequency, f_{IF} is the carrier frequency and n is an integer number.

With the example taken in the previous part, the result of the subsampling operation is shown in frequency domain in Figure 2.2. In this example, $f_{SUB} = 4.88\ GHz$ and $f_{IF} = 20\ GHz$. The sampling operation of the inital 20 GHz sine wave (blue, plain) generates images around every integer multiple of f_{SUB} (red, dotted). Meanwhile, the only useful band after the subsampling operation is $[-f_{SUB}/2 : f_{SUB}/2]$.

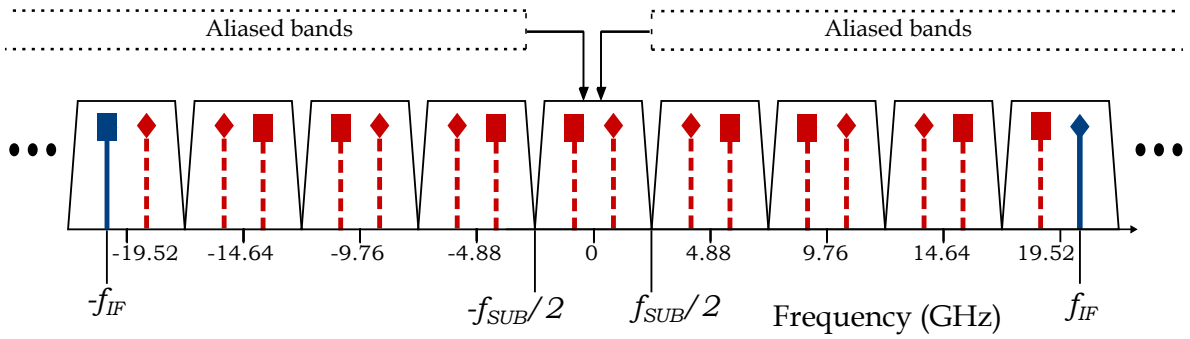


Figure 2.2: Frequency domain illustration of the subsampling

The very first advantage for a system which uses this approach is that the sampling frequency can be reduced and so the power consumption. Meanwhile, as the subampling uses aliasing of signals, it is consequently also subject to aliasing of interferences and to noise folding. These points will be discussed in the following parts.

I.B. Reported solutions using subsampling

Subsampling is quite commonly used in wireless receiver architecture for low frequencies [18], [19].

The sub-sampler described in [18] targets the 800 MHz to 5.8 GHz band. For this target, the sampling frequency is up to 75 MSps for a carrier frequency up to 5.8 GHz. After the sampler, the SNDR is 22.9 dB. In order to overcome the problem of noise folding due to the subampling operation, digital processing such as averaging is introduced. This latter

increases the final SNDR up to 73.1 dB which is large enough to reach the fastest data rate of the 802.11g standard. This baseband processing is possible because the data rate of this standard is 54 Mbps. However it is not a suitable solution for multi-Gbps data rate systems.

Another subampling solution has been presented in [19]. This system is a multi-standard RF heterodyne receiver. The RF signal is sampled by a first track and hold switch clocked at 761.8 MHz. The resulting IF frequency is between 145 and 185 MHz depending on the considered band. A second track and hold switch down-converts the signal from this IF frequency to baseband. The simulation results of this system show that GSM, UMTS and 802.11g standards can be received by a single receiver because the SNR degradation due to the subampling stage complies with the receiver requirements for all these standards. To the author's knowledge, no solution has been proposed for higher RF frequencies.

I.C. Up to 60 GHz?

In these two solutions, the input frequency is few GHz. To transpose these architectures for WiGig applications, the input bandwidth should be increased at least by ten. Moreover, errors dues to clock jitter would be ten times higher. Consequently, these architectures are hardly transposable for direct subampling of signals around a 60 GHz carrier. A solution to relax these constraints is to perform subampling at an intermediate frequency, creating a heterodyne receiver. With this approach, the RF input frequency and consequently the design constraints could be decreased. This is the approach developed in this manuscript.

II. Theory of subsampling applied to the 60 GHz standard

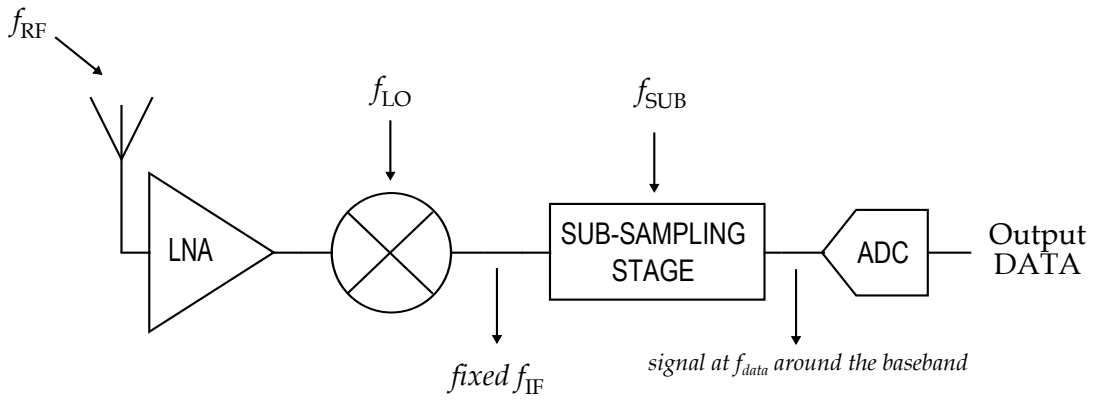


Figure 2.3: Simplified architecture of an heterodyne receiver including a subampling stage

In the present section, the simplified architecture shown in Figure 2.3 is considered. The radio frequency signal at f_{RF} received at the antenna is amplified by a Low Noise Amplifier (LNA). In the following block, the signal around f_{RF} is mixed with a Local Oscillator (LO) at f_{LO}. In order address all the channels defined in the standard, f_{LO} can reach 4 values to down-convert the signal from f_{RF} (four possible carrier frequencies) to a fixed intermediate frequency f_{IF}. This signal is downconverted a second time around DC. The data-rate there is f_{data} thanks to the subsampling stage which operates at the subsampling frequency $f_{SUB} = 4f_{data}$. Finally, the output voltage is converted from analog to digital domain.

II.A. Downconversion

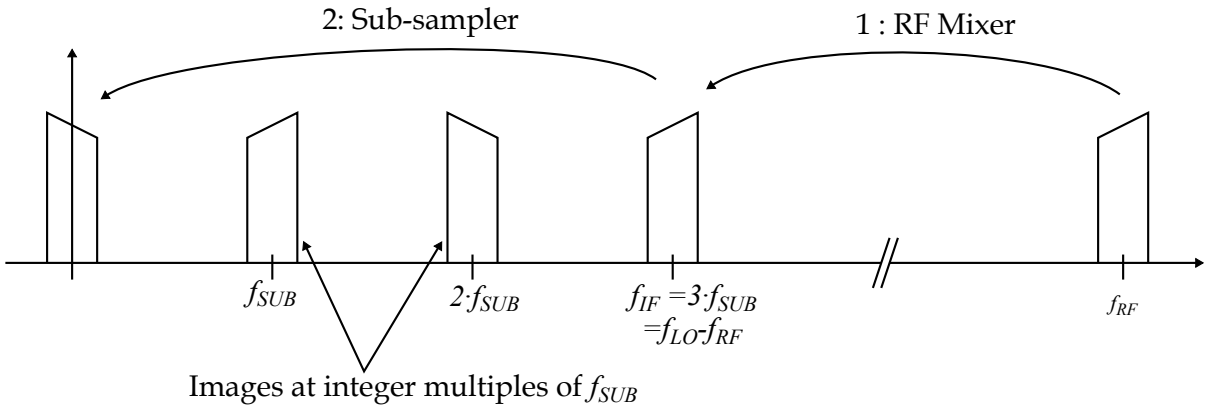


Figure 2.4: Simplified representation of the successive down-conversion operations

Figure 2.4 shows a simplified representation of the two successive operations performed in the system in order to down-convert the signal from the 60 GHz carrier f_{RF} down to DC.

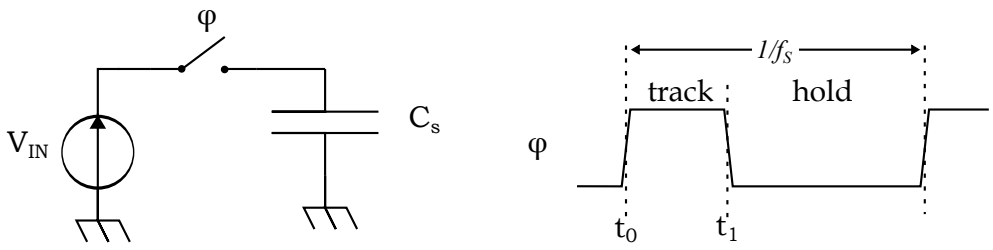
First, the RF mixer in the front-end translates the signal from f_{RF} to f_{IF}. Second, the sub-sampler downconverts the IF signal around DC by sampling the signal at f_{SUB}.

In order to be exactly around DC after the second operation, f_{IF} should be an entire multiple of f_{SUB}. Consequently a defined value of the LO frequency has to be chosen in order to address the desired channel and place it around the fixed IF frequency.

II.B. Sampling Operation

In sampling systems, there are two different ways to sample a signal: in voltage domain or in charge domain. This section firstly compares these two ways and secondly provides a detailed analysis of the charge domain sampling which has been used in this work.

II.B.1 Charge domain versus voltage domain sampling

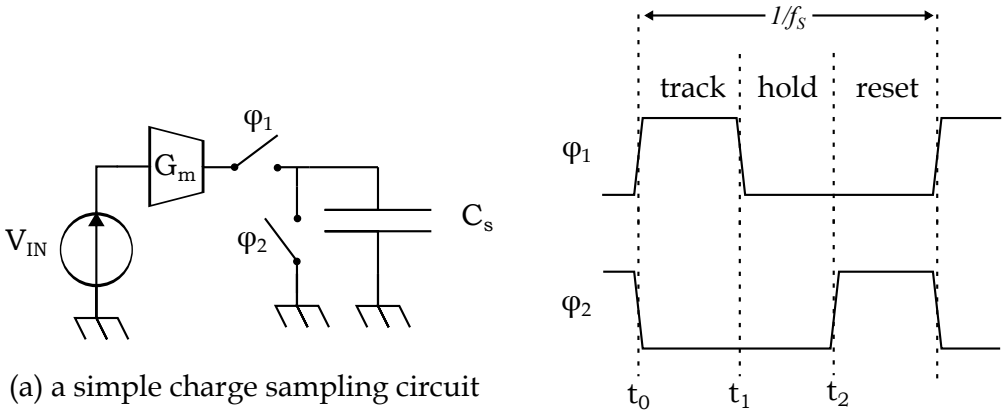


(a) a simple voltage sampling circuit (b) clock strategy of the circuit

Figure 2.5: Voltage sampling system

The voltage domain sampling and its clock strategy is presented in Figure 2.5 . It consists of a switch connected to the signal source on one side and the sampling capacitor on the other side. When the switch turns on, the tracking phase begins, the voltage on the sampling capacitor follows the signal. When the switch turns off, the hold phase begins, the sampled value is stored on the sampling capacitor.

The charge domain sampling and its clock strategy is presented in Figure 2.6. The difference in terms of topology regarding the voltage domain sampling is that the signal is converted to current by a transconductance stage. When the switch turns on, the integration phase begins : the charges coming from the transconductances are integrated in the sampling capacitor. When the switch turns off, the hold phase begins : the sampled value is stored on the sampling capacitor. The capacitor should be reset in oder to sample the following value.



(a) a simple charge sampling circuit

(b) clock strategy of the circuit

Figure 2.6: Charge sampling system

	Voltage Domain	**Charge Domain**
Bandwidth	FIXED Defined by the on-resistance of the switch	CONFIGURABLE Defined by the integration window
Error due to sampling clock jitter	HIGH Depends on 1 single edge	REDUCED Depends on both rising and falling edge
Aliased Noise	HIGH Only RC filter on the input noise	REDUCED SINC filter on the input noise
Implementation	SIMPLE needs : switch and sampling capacitor	COMPLEX needs : switch, sampling capacitor, V-to-I converter, reset system

Table 2.1: Voltage versus Charge domain sampling

Pro and cons of each solution are summed ip in Table 2.1 [20].

In voltage domain sampling, the value of the tracking capacitor and the on-resistance of the switches define the bandwidth of the sampler while in charge domain sampling, the bandwidth is defined by the integration window.

The error due to the sampling clock jitter is reduced in charge domain sampling because the result depends on both rising and falling edge of the clock while in voltage domain, the sampling value only depends on the rising or falling edge [20].

The aliased noise is reduced in charge domain sampling because its frequency response is a sinc function while it is a simple RC low pass filter in voltage domain [20].

From a designer point of view, the voltage domain sampling only requires a sampling

switch and sampling capacitor. The charge domain sampling is more complex because it requires in addition to the previous elements, V-to-I converter, a reset system and a complex clock strategy.

Regarding these results, the voltage domain sampling is the best candidate for low-bandwidth systems because the implementation is simple. However, with the target of high frequency and high bandwidth systems, the charge domain sampling is the best candidate because of its reduced timing constraints. For the targeted architecture the charge domain subsampling is the most suitable solution in terms of bandwidth and reconfigurability

II.B.2 Frequency Behavior of the Charge Domain Sampling

The charge sampler shown in 2.6 is composed of a transconductance stage (G_m) followed by a switch clocked at f_{SUB} and an integration/sampling capacitor C_s. Integration is done between 0 and T_i. The result of the integrated voltage on C_s is given by:

$$V_{OUT}(t) = \frac{1}{C_s}\int_0^{T_i} I_{IN}(t)dt \tag{2.2}$$

where V_{OUT} is the output voltage of the integrator and I_{IN} is the current flowing from the G_m stage. Considering this latter as the result of the conversion of the transconductance, the output voltage is a function of the voltage at the input of the transconductance V_{IN}

$$V_{OUT}(t) = \frac{G_m}{C_s}\int_0^{T_i} V_{IN}(t)dt \tag{2.3}$$

After Fourier transform of this expression, the frequency domain transfer function of the

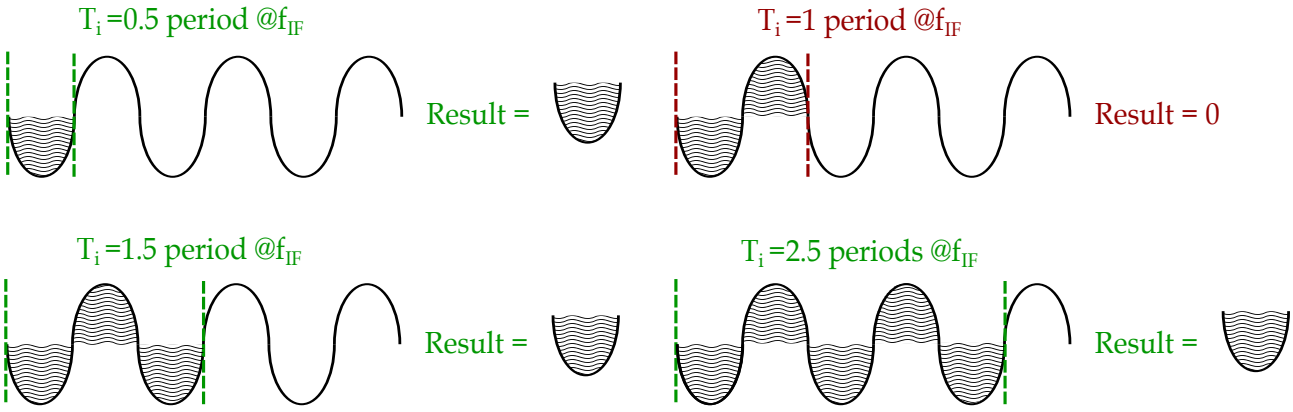


Figure 2.7: Result of the integration of a sine wave at f_{IF} for several values of T_i

charge-domain integrator presents a sinc behaviour and is given by:

$$|H(f)| = \frac{G_m}{C_s} \frac{|\sin(\pi f T_i)|}{\pi f} \tag{2.4}$$

The frequency-dependent part of this transfer function only depends on T_i. Figure 2.7 illustrates the result of the integration of a sine wave at f_{IF} for given values of T_i.

T_i has to be chosen such that $|H(f)|$ has a maximum for $f = f_{IF}$, which translates into the following requirements :

$$T_i = \frac{N_{period} + 0.5}{f_{IF}} \tag{2.5}$$

where N_{period} is an integer number. Figure 2.8 plots the frequency response of a charge domain sampler for several values of T_i.

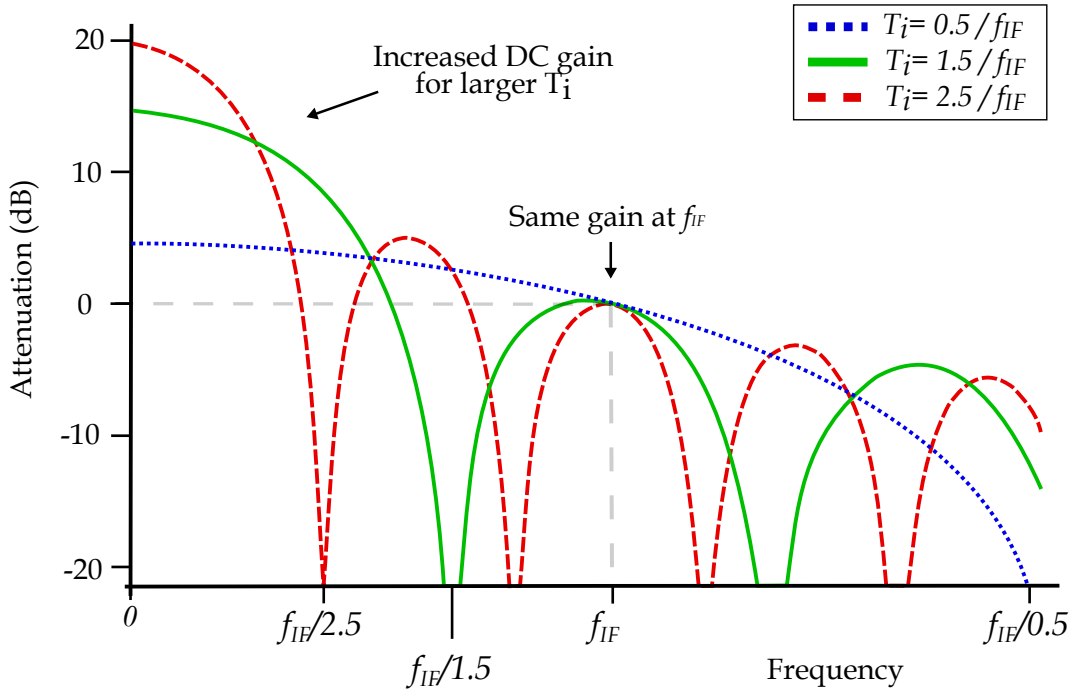


Figure 2.8: Frequency response of the integrator for different N_{period}

For each value of N_{period}, a local maximum is found around f_{IF} and a notch is found every $1/T_i$. The main difference is DC gain: as T_i increases, the DC gain increases. This will influence noise folding as discussed in the next section.

II.C. Considerations on Noise Folding

II.C.1 Why is noise folding a key point in subsampling systems?

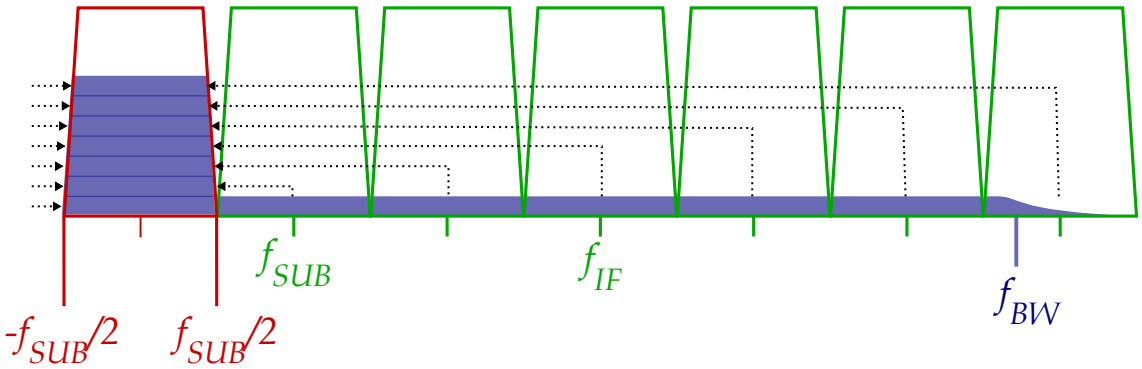


Figure 2.9: Schematic representation of noise folding during the subampling operation

As subampling receivers use aliasing of signals, they are consequently subject to noise folding. Figure 2.9 shows how high frequency noise is aliased into the baseband.

The total integrated noise over the entire band is:

$$P_{noise} = \int_{-\infty}^{\infty} V_{NOISE-OUT}(f)^2 df = \int_{-\infty}^{\infty} V_{NOISE-IN}^2 |H(f)|^2 df \tag{2.6}$$

where $V_{NOISE-IN}$ is the input noise voltage at the antenna, $H(f)$ is the transfer function of the sampler defined in equation 2.4 and $V_{NOISE-OUT}$ is the output voltage, after the sampler. The input noise is considered being white over all the frequencies, so equation (2.6) is equivalent to:

$$P_{noise} = V_{NOISE-IN}^2 \int_{-\infty}^{\infty} |H(f)|^2 df \tag{2.7}$$

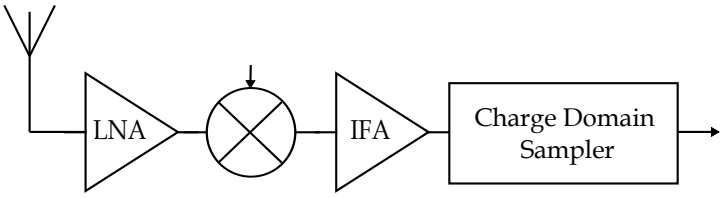
Fortunately the bandwidth of the sampler is limited to f_{BW} thanks to the association of the sampling capacitor and the resistance introduced by the non ideal sampling switch. This limits the integrated noise power. It has been shown in [21] that the noise power is equal to:

$$P_{noise} = T_i (\frac{G_m}{C_s})^2 \tag{2.8}$$

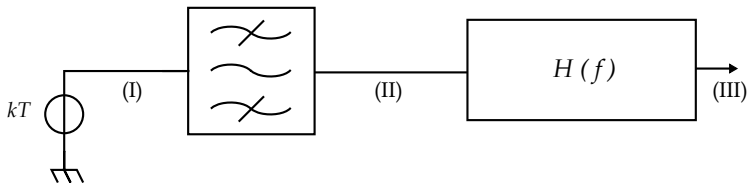
This represents the total theoretical noise power due to thermal noise on the antenna, integrated by the sampler.

II.C.2 Folded noise versus integration window width

Regarding equation (2.8), low values of T_i seem to be the best choice because the total noise power at the output is lower. For f_{IF} around 20 GHz, the integration pulse width would be about 25ps. For larger pulses, DC noise power increases and so the total noise power. However, Equation (2.8) considers an infinite bandwidth for the elements of the receiver.

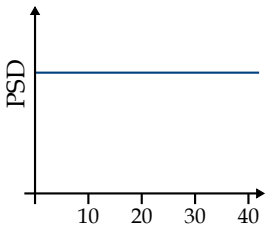


(a) Simplified architecture of a receiver including a charge domain subsampler

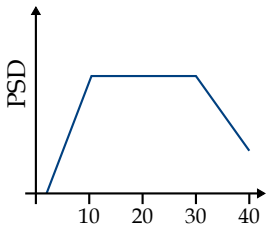


(b) Equivalent model used for calculations

(c) PSD of noise at (I)



(d) PSD of noise at (II)



(e) PSD of noise at (III)

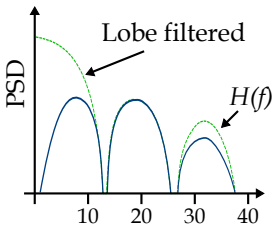


Figure 2.10: Simplified architecture of a receiver including a charge domain subsampler, its equivalent model for calculation and PSD of noise at several points

The input noise at the antenna is considered constant for all frequencies. Knowing that the frequency response of the sampler presents a sinc shape, the most important part of the noise power lies within the first lobe. As shown in Figure 2.10, considering the actual limited bandwidth of the elements of the receiver, the noise within the first lobe is likely to be filtered. Each part of the receiver (Antenna, LNA, Mixer and IF amplifier) can be considered at least as a 2nd order band pass filter, mainly due to AC coupling between stages and attenuation at high frequencies. Consequently the combination of all the front-end elements produces a 4th order high-pass filter shape. An assumption is made on the cut-off frequencies of about 10

GHz and 30 GHz for calculation purposes.

Figure 2.11 shows the impact of the RF frequency selectivity on the integrated noise power for different integration windows T_i. These calculations consider thermal noise only. The other conditions are $G_m = 10mS$, $C_s = 50fF$, the gain of the front-end is 24 dB and the global front-end noise factor is 5 dB.

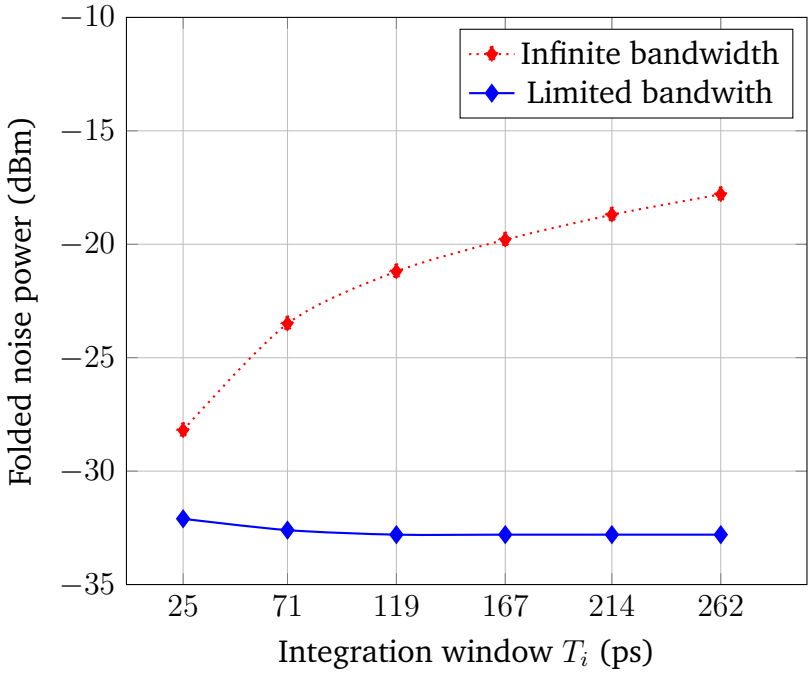


Figure 2.11: Effects of filtering on folded noise power

Considering (2.8), the integrated noise power increases with T_i if no filtering is applied. It is represented by the red (dotted) curve in Figure 2.11. While considering the limited bandwidth of each component of the receiver, the integrated noise power is roughly the same for all values of T_i. This latter is represented by the blue (plain) curve. As a conclusion, N_{period} can be chosen independently of folded noise power considerations.

III. Frequency planning

III.A. In-Band channel aliasing

The baseband data rate defined by the 802.15.3c standard is 1.76GS/s (f_{data}) in the single carrier case. Channel spacing is approximately 2 GHz and the total occupied bandwidth of the standard is therefore approximately 8 GHz. The sampling frequency f_{SUB} in the proposed architecture is chosen to be four times the baseband data rate, i.e. 7.04 GHz.

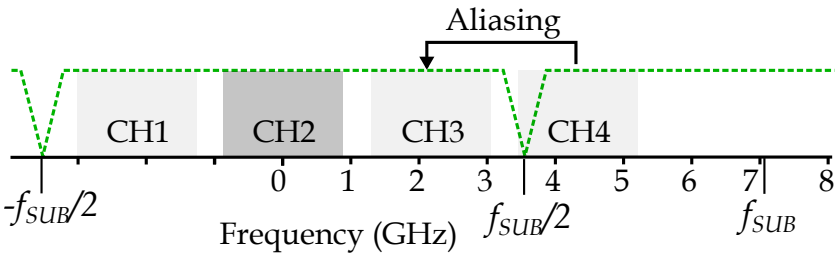


Figure 2.12: Aliasing of channels while listening to the second channel

When using sampling frequencies lower than the standard's allocated bandwidth, in-band aliasing can occur. As shown in Figure 2.12, when listening to the second channel, the channels are aliased out of the band of interest. The effect is identical when listening to the third channel.

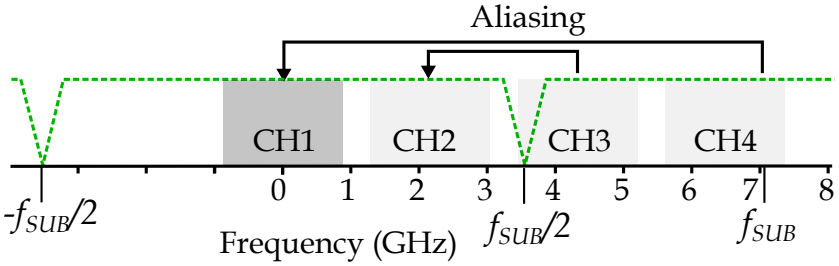


Figure 2.13: Aliasing of channels while listening to the first channel

The critical situation appears when receiving the channels at the low end of the band because, as shown in Figure 2.13, the channel at the other side of the standard's band produces in-band aliasing. The effect is identical when listening to the channel 4, at the high end of the band.

III.B. Alternate channel attenuation

By carefully choosing an IF frequency of 3 times the sampling frequency ($f_{IF} = 21.12GHz$) associated to a T_i of $1.5/f_{IF}$ ($N_{period} = 1$) the sampler provides notches at an offset frequency of 7.04 GHz from the IF frequency. These notches introduce effective anti-aliasing filtering for the critical case. This is illustrated in Figure 2.14(a).

III.C. Adjacent channel attenuation

Moreover, sampling the signal at four times the baseband data rate allows the implementation of a FIR filter. Figure 2.14(b) shows the frequency response of the average of 2, 3 or 4 successive samples. The notch provided by the sampler filters the fourth channel in the critical case. The second and third channels could also be aliased onto the baseband after decimation. As shown in Figure 2.14(b), the FIR filter which offers the best attenuation for the second and third channels is composed by the average of 4 successive samples. This results in the transfer function of (2.9).

$$FIR(z) = 1 + z^{-1} + z^{-2} + z^{-3} \tag{2.9}$$

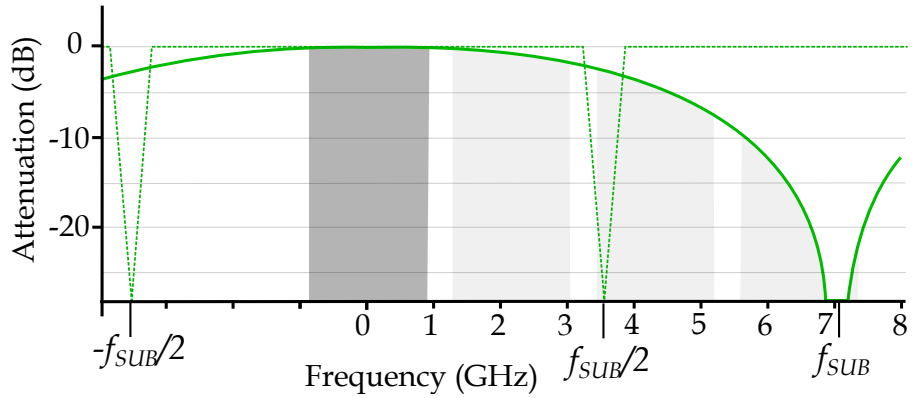
III.D. Resulting theoretical attenuation

As shown in Figure 2.14(c), the combination of both sampler and 4-coefficient FIR filter provides an efficient anti-aliasing filter for all adjacent channels of the 802.15.3c standard. Table 2.2 shows the simulated channel rejection when integrated power over the 1.76 GHz channel bandwidth is considered.

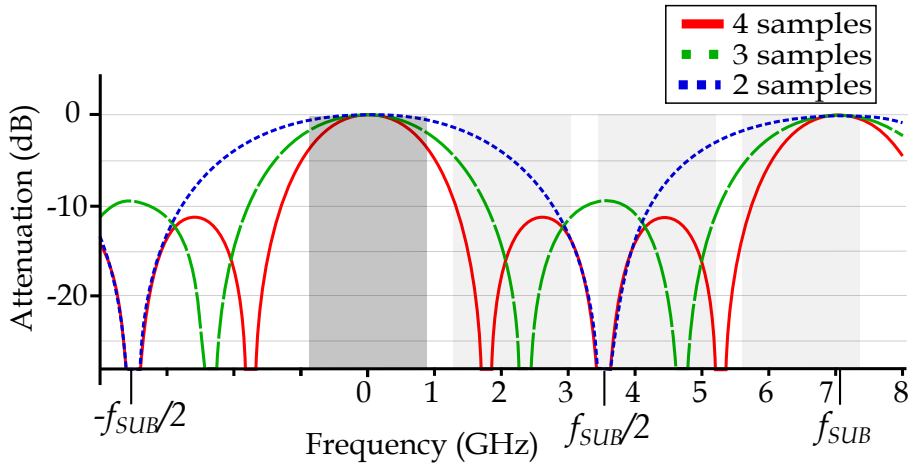
The main advantage of the proposed architecture is the optimal use of the channel filtering capabilities in the down-conversion process and has been presented at the IEEE ISCAS in 2012 [22] and invited to IEEE TCAS in 2013 [23] .

Channel	Rejection (dBc)
n+1	15.7
n+2	23.1
n+3	30.23

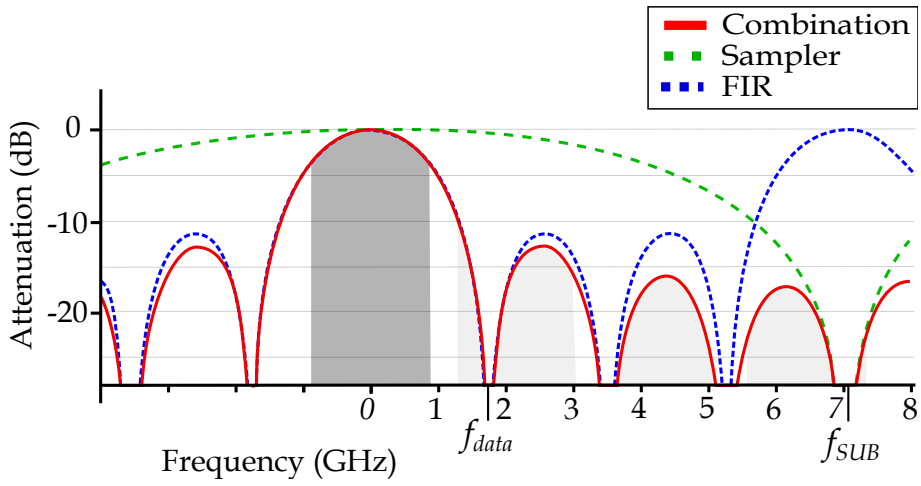
Table 2.2: Adjacent and alternate channel rejection



(a) Effect of the frequency response of the sampler



(b) Frequency response of the FIR filter for different lengths



(c) Frequency response of the sampler combined to the averaging of four successive samples

Figure 2.14: Effect of frequency response of the sampler (a), the FIR (b) and combination of both (c)

IV. System Performance

This part shows the limitations of subampling architectures for 60 GHz applications at the system level. These limitations are mainly due to the aliased noise and the error on the sampling instant due to jitter on the sampling clock.

The constraints and choices presented in the previous section lead to the architecture presented in Figure 2.15. First, transconductance stages (G_m) convert the IF input voltage into current. Then, charge-domain integrators perform down-conversion. Finally, Finite Impulse Response filters (FIR) down-sample the signal to the final data rate (f_{data}).

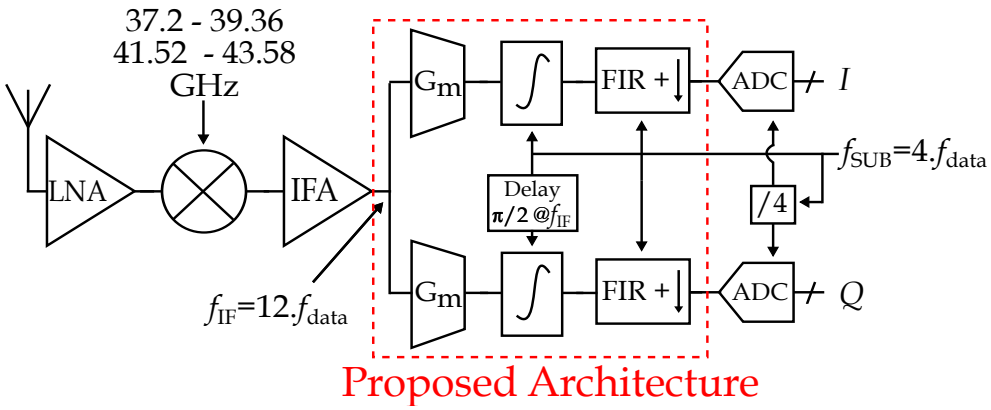


Figure 2.15: Complete Receiver Architecture

IV.A. Reference RF blocks

For this study, the front-end published in [2] is taken as a reference for the characteristics of the RF front-end blocks. It is composed of a low noise amplifier, a mixer and an IF amplifier. The gain of the frontend is 24 dB and it has a 5 dB noise factor. Modulation is single carrier block transmission with QPSK constellation. In this mode, the required sensitivity or minimum input signal power at the antenna is -53.9 dBm. Therefore, the minimum signal power at the transconductance input node is about -30 dBm.

IV.B. Noise analysis

The signal transfer function is function of $1/{C_s}^2$ thanks to the integration process. Most of the noise contributions are also functions of the sampling capacitor value. A simplified model of each component is used for calculating the noise contributions.

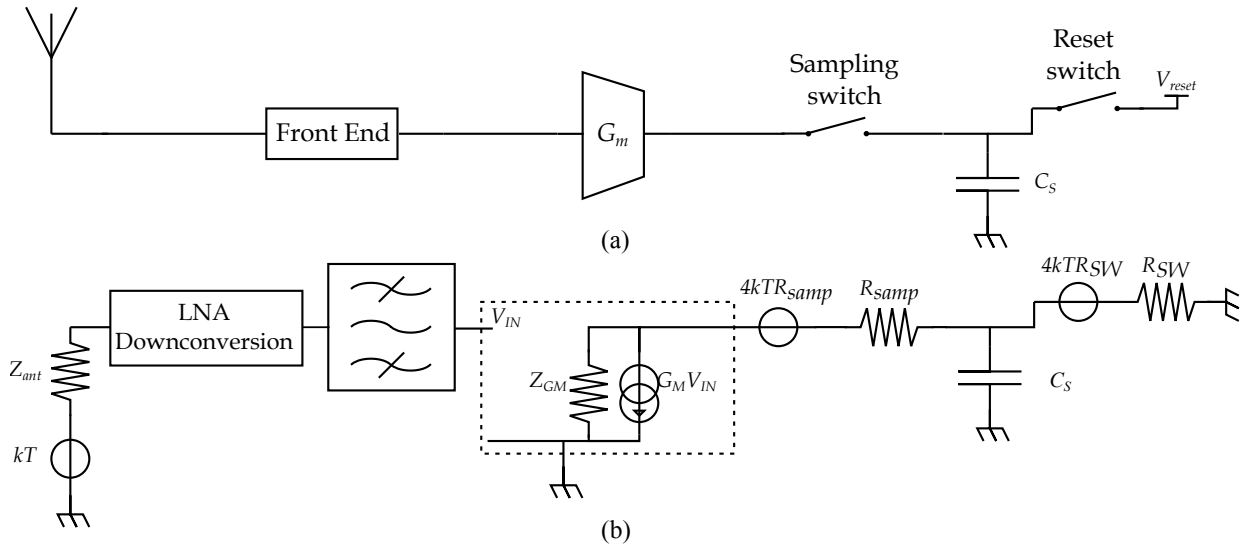


Figure 2.16: Simplified chain of the receiver (a) and its equivalent model used for the noise analysis (b)

IV.B.1 Noise coming from the switches

As represented in Figure 2.16, the antenna is modeled as a simple kT noise source and its corresponding impedance Z_{ant}. The low noise amplifier and the mixer are considered as bandpass filters. Both sampling and reset switches are modeled as noisy resistors. The noise factor of the transconductance stage is not considered because of the very high gain of the low noise amplifier. The global noise factor considered is 5 dB, corresponding roughly to the noise factor of the LNA. The reset switch provides the well known sampling noise:

$$Pnoise_{RST} = 10 \cdot \log\left(\frac{kT}{C_s}\right) \tag{2.10}$$

The sampling switch provides a less important noise contribution thanks to the output impedance of the transconductance stage:

$$Pnoise_{SAMP} = 10 \cdot \log\left(\frac{kT}{C_s}\frac{R_{samp}}{R_{samp} + Z_{Gm}}\right) \tag{2.11}$$

IV.B.2 Folded noise from the antenna

The contribution of the thermal noise coming from the antenna consists in the integration of a thermal noise kT at $-174dBm/Hz$ over the effective bandwidth of the receiver. The antenna, the low noise amplifier and the mixer are all modeled in Matlab as ideal first order

bandpass filters around the total bandwidth of the standard defined in 2.12:

$$BPF(f) = \left| \frac{1}{1 + \frac{f}{30e9}^3 + \frac{10e9}{f}^3} \right| \tag{2.12}$$

As explained in section II.C., the integrator adds a contribution to the global transfer function defined in equation 2.13

$$SAMPLER(f) = |H(f)|_{Ti=1.5/f_{IF}} \tag{2.13}$$

The FIR also adds a contribution defined in equation 2.14

$$FIR(f) = \left| \frac{1}{2} \cdot \cos(3\pi f/f_{SUB}) \cdot \cos(1.5\pi f/f_{SUB}) \right| \tag{2.14}$$

These contributions are considered by modeling the system in Matlab. The output noise contribution from the thermal noise at the antenna is the result of the integration of the thermal noise shaped by the transfer function of the system.

$$Pnoise_{ANT} = 20 \cdot \log \int_{-\infty}^{\infty} SAMPLER(f) \cdot FIR(f) \cdot BPF(f) \cdot df \tag{2.15}$$

which can be simplified to :

$$Pnoise_{ANT} = -333dBm - 20 \log C_S \tag{2.16}$$

The total output noise shown in equation 2.17 is the sum of these three major contributions :

$$Pnoise = Pnoise_{ANT} + Pnoise_{SAMP} + Pnoise_{RST} \tag{2.17}$$

IV.B.3 Resulting sensitivity

Figure 2.17 shows the total noise power as a function of the sampling capacitor. Output signal power is considered as the voltage of the sampling capacitor across a 50 Ω resistor. For these calculations, the output impedance of the transconductor was set to 2kΩ and the sampling switch resistance is 2kΩ. As a result, the signal-to-noise ratio is improved for low values of the sampling capacitor, and is obviously limited by the signal-to-noise ratio at the

antenna.

For a sampling capacitor higher than 50fF, noise contributions from switches become dominant, compared to input noise. Smaller values of the capacitor do not increase the theoretical performance. However, reducing the value of the capacitor will increase sensitivity to parasitic capacitances and matching. Therefore, with a chosen value of 10mS for the transconductance, a capacitor value of 50 fF seems to be a good trade-off. With these conditions, the expected SNR is about 19 dB.

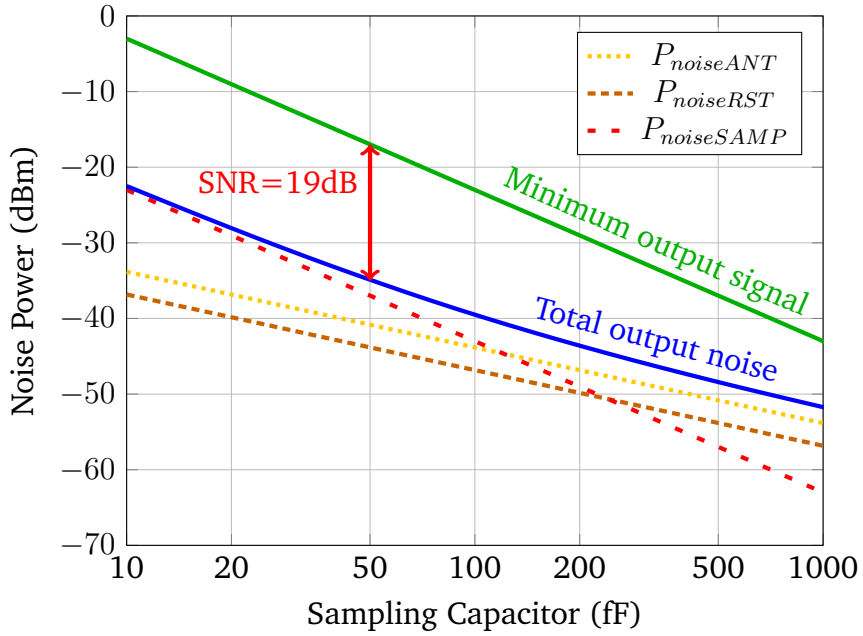


Figure 2.17: Noise contributions as a function of the sampling capacitor

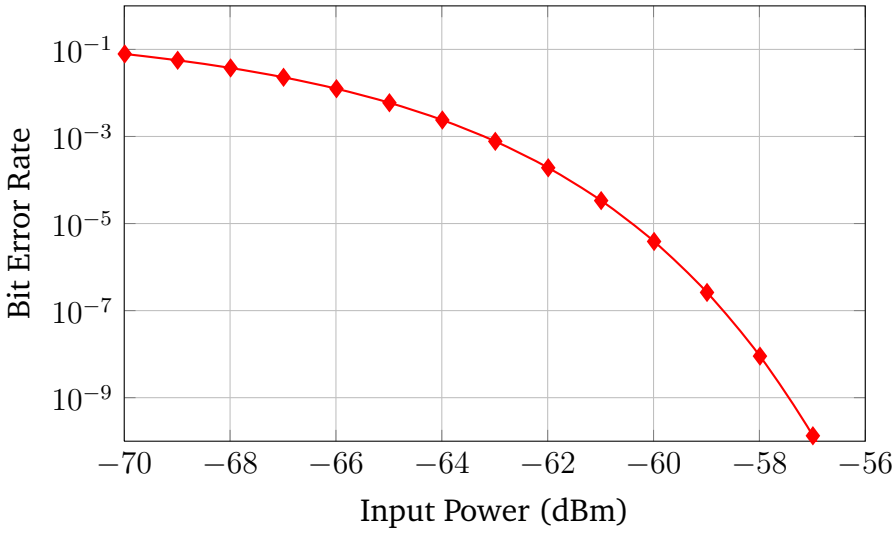


Figure 2.18: Resulting bit error rate for a given input power at system level

A system-level simulation of the bit error rate (BER) versus input power is presented in

Figure 2.18. The simulation includes the folded noise from the antenna and the noise contribution due to the sampling switch. The BER is below 10^{-12} for -54 dBm input power. Consequently, the input power can be reduced while keeping an acceptable BER. The sensitivity of the receiver is defined in [5] as the ability to receive a signal with a BER below 10^{-6} before corrections. Regarding Figure 2.18, the sensitivity of the proposed architecture is -59 dBm. This result shows how the folded noise affects the sensitivity.

IV.C. Sampling jitter

IV.C.1 What is sampling jitter?

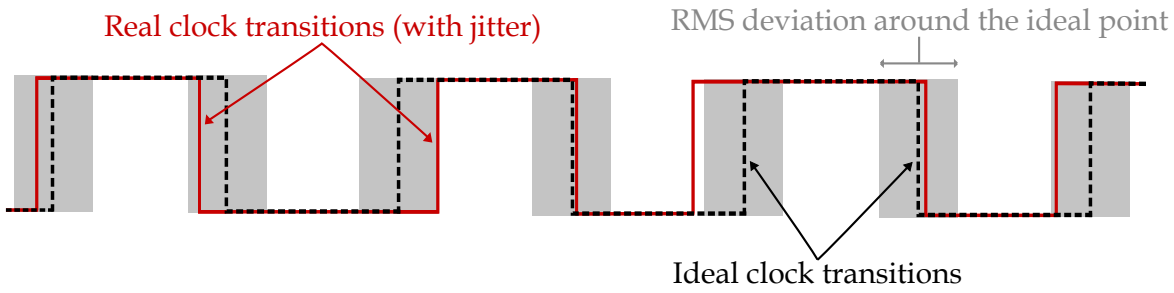


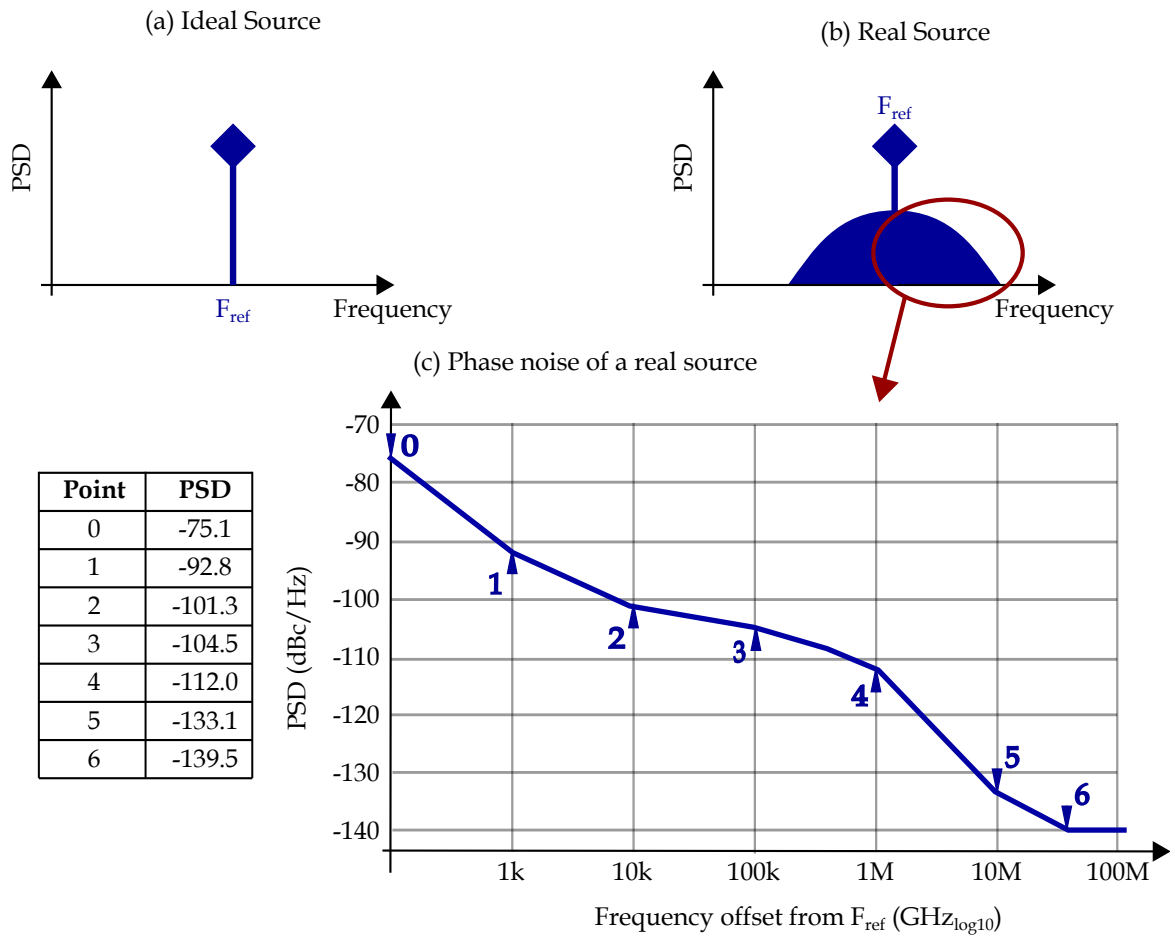
Figure 2.19: Schematic representation of the sampling jitter

According to the definition, jitter is the deviation from the ideal timing of an event. Figure 2.19 shows this effect. The dotted lines represents the ideal clock with ideal edges, the plain lines shows the real clock edges. Each difference between the real and the ideal edge is the effect of the sampling jitter. The jitter is usually measured as the RMS deviation around the ideal value.

IV.C.2 From phase noise to sampling jitter

The community working on VCOs defines the imperfections of oscillators as phase noise in frequency domain. The community working on sampling systems defines the imperfections of the sampling clock as a time domain jitter. This part shows how to go from the phase noise in frequency domain to the jitter in time domain.

An ideal source has a spectrum where all the power in concentrated in a very narrow band as shown in Figure 2.20 (a). A real source leaks in the frequency domain around the ideal frequency (Figure 2.20 (b)). This leakage is usually represented as a power spectral density



Point	PSD
0	-75.1
1	-92.8
2	-101.3
3	-104.5
4	-112.0
5	-133.1
6	-139.5

Figure 2.20: Ideal and Real sine wave sources

at an offset of the frequency of reference F_{REF} as shown in Figure 2.20 (c). The phase noise value given in this Figure are extracted from [24].

The jitter can be calculated from this PSD using Equation 2.18 given in [25].

$$Jitter_{RMS} = \frac{1}{2\pi f_c} \int_{f_{min}}^{f_{max}} PSD(f)df \tag{2.18}$$

The integration of the phase noise up to twice the sampling frequency gives the RMS jitter [26]. For calculation purposes, each part between two points is considered as a rectangle. With this method, the RMS jitter of the oscillator [24] is calculated to be 822fs which complies to the requirements given in the previous section.

IV.C.3 Effects of the jitter on high speed sampling systems

While considering the non ideal sampling instant, errors exists between the ideal value which should habe been sampled and the real sampled value. Figure 2.21 shows the error on the

sampled value due to the sampling jitter.

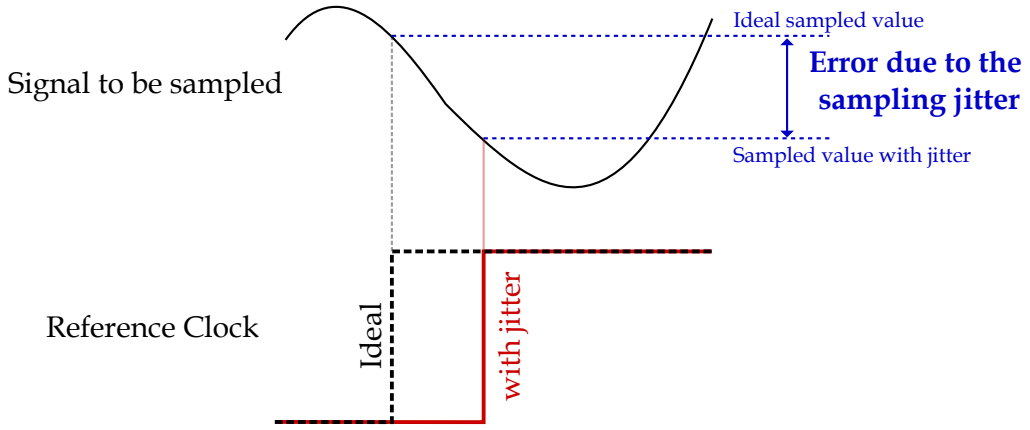


Figure 2.21: Effect of the clock jitter in a high speed sampling system

[27] gives a relation between the RMS jitter and the output SNR due to non ideal sampling instant for voltage sampling :

$$SNR = 20\log(2\pi f \tau_{jitter-RMS}) \tag{2.19}$$

where f is the frequency of the sampled signal and $\tau_{jitter-RMS}$ is the RMS jitter of the sampling clock. For a given jitter value, the higher the frequency, the higher the error on the sampling value. Consequently, in high speed sampling systems, the sampling jitter is an important issue. The reference clock should be clean enough in order to limit its influence on the output SNR. Methods for jitter compensation have been recently described in [28]. However, a high resolution ADC is required which would translate in very high power consumption. Consequently, the sampling clock should be clean enough without any additional processing.

IV.C.4 Jitter in charge domain samplers

In charge domain samplers, the integration window is directly derived from the sampling clock. Hence the clock phase noise directly influences the phase of the demodulated data. Considering the input signal

$$V(t) = I\cos(2\pi f_{IF} t) + Q\sin(2\pi f_{IF} t) \tag{2.20}$$

In charge domain, the sampling operation considering jitter is modeled as follows:

$$V_{OUT} = \int_{a+\delta_0}^{a+T_i+\delta_1} V(t)dt \tag{2.21}$$

where $V(t)$ is the input IQ signal defined in (2.20), a is the sampling instant, T_i is the ideal sampling window, δ_0 and δ_1 are random variables representing the jitter of the sampling clock. I and Q are considered constant in the integration periods. This previous equation is divided in two parts which are the ideal integration window between a and $a + T_i$ called $V_{OUT-signal}$ and the noise contribution $V_{OUT-noise}$.

$$V_{OUT-signal} = \int_{a}^{a+T_i} I \cdot sin(2\pi f_{IF} t) + Q \cdot cos(2\pi f_{IF} t)dt \tag{2.22}$$

$$V_{OUT-noise} = \int_{\delta_0}^{0} I \cdot sin(2\pi f_{IF} t) + Q \cdot cos(2\pi f_{IF} t)dt + \int_{T_i}^{T_i+\delta_1} I \cdot sin(2\pi f_{IF} t) + Q \cdot cos(2\pi f_{IF} t)dt \tag{2.23}$$

Considering In-Phase path sampling, the ideal value is given for the sampling instant : $a = 0$. The standard deviation around the ideal sampling instant is considered short regarding the period of the input signal. Therefore, the following assumptions can be made on the input signal :

$$\cos(2\pi f_{IF}\delta) = 1 \qquad sin(2\pi f_{IF}\delta) = 0 + 2\pi f_{IF}\delta \tag{2.24}$$

Consequently, the result of the ideal integration is:

$$V_{OUT-signal} = \frac{-2 \cdot I}{2\pi f_{IF}} \tag{2.25}$$

The noise contribution is:

$$V_{OUT-noise} = Q \cdot (-\delta_0 + \delta_1) \tag{2.26}$$

Finally, the SNR for one sample taken in charge domain is given by

$$SNR_{1-sample} = 20 \log \left| \frac{V_{OUT-signal}}{V_{OUT-noise}} \right| \tag{2.27}$$

considering on I and Q with a QPSK modulation :

$$|I| = |Q| \tag{2.28}$$

The SNR for 1 sample is :

$$SNR_{1-sample} = 20\log\left|2\pi f_{IF} \cdot \frac{(\delta_0 + \delta_1)}{2}\right| \tag{2.29}$$

The advantage of charge domain sampling with respect to voltage domain sampling is shown in (2.27) and in Figure 2.22. The noise contribution resulting from the sampling instant jitter is reduced by $\sqrt{2}$ when two random values are averaged. The proposed architecture has the advantage of taking four successive values in charge domain. Consequently, the equivalent jitter contribution goes down by $\sqrt{8}$ in comparison to the voltage sampling technique.

$$SNR = 20\log(2\pi f_{IF}\frac{T_{jitter}}{\sqrt{8}}) \tag{2.30}$$

Figure 2.22 plots the resulting SNR versus the sampling jitter for three sampling techniques : voltage sampling (green), charge domain sampling (blue) and the proposed architecture (red).

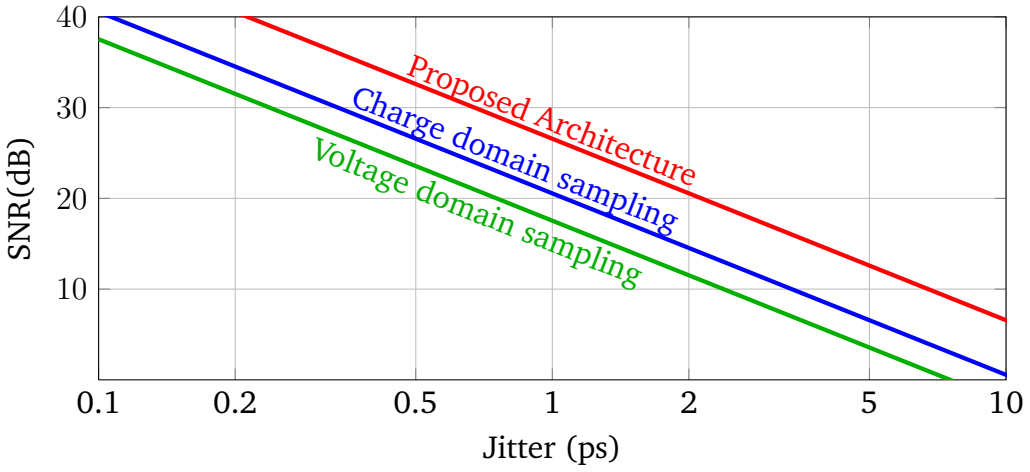


Figure 2.22: Resulting SNR for the sampling of an IQ signal with jitter on the sampling instant

IV.C.5 Limitations due to sampling jitter in the proposed architecture

A system-level simulation has been performed in order to demonstrate the effect of uncertainty due to the sampling clock jitter. This simulation evaluates the error vector magnitude (EVM) as a function of the input power for several values of RMS jitter.

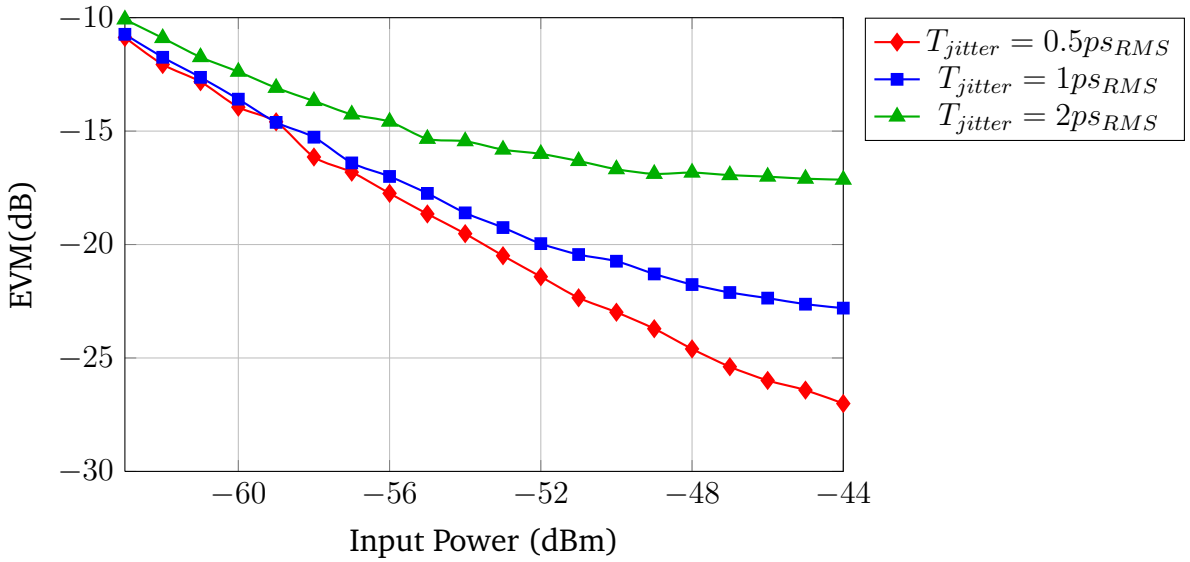


Figure 2.23: EVM versus input power for several values of sampling clock jitter

The simulation includes the folded noise from the antenna, the noise contribution due to the sampling switch, the sampler with time uncertainty and the 4-coefficient FIR. The results are presented in Figure 2.23. It shows that this jitter has a negligible effect at low input power as the noise is dominated by the folded thermal noise. Conversely, when the input power is high, the jitter effect is the most important contribution to the EVM. In order to keep the sensitivity of the receiver at -59 dBm, the RMS jitter should be below 1ps which complies with the state of the art [24].

V. Conclusion

This section has shown that the subsampling is a basic principle of telecommunications but it has never been used in high data rate communications (higher than 1 Gbps) because timing and noise constrains are very high.

This theoretical study proves that subsampling can be competitive in such applications in terms of noise folding which is the most critical issue in high bandwidth sampling systems.

A particular arrangement of the frequency plan allows embedded channel filtering : the combination of the FIR and the charge domain sampler enables up to 23dBc of alternate channel attenuation.

Moreover the proposed architecture averages four successive samples in charge domain which reduces the effect of sampling jitter. Phase noise in recent contribution is low enough to be compatible with subsampling for IF signals at 20 GHz.

CHAPTER

3

SILICON IMPLEMENTATION

I. Introduction

This chapter details the implementation of the quadrature charge domain sub-sampler. Starting from a basic charge domain sampler, the first section shows how the sampler and the sampling capacitors have been designed. The second section goes from the basic sampler to the final system while considering all the constraints related to continuous time operation. The third section shows how to generate a correct pattern to feed the samplers which include monitoring of the quality of the clock and synchronization. Finally the fourth section sums up the results.

II. Samplers

II.A. Architecture of a charge domain sampler

The most common way to perform charge domain sampling is to use a transconductance stage (G_m) and a switch which enables or disables the charges flowing from the G_m to the sampling capacitor. This approach is illustrated in Figure 3.1 (a).

With ideal components, the output impedance of the G_m cell is infinite and the 'on' resistance of the switch is equal to zero. With these considerations, all the current converted by the G_m cell is integrated by the sampling capacitor. The integration process is then ideal.

In order to perform the voltage to current conversion, a high transconductance gain and high-output-impedance amplifier is needed. The cascode transconductance amplifier with

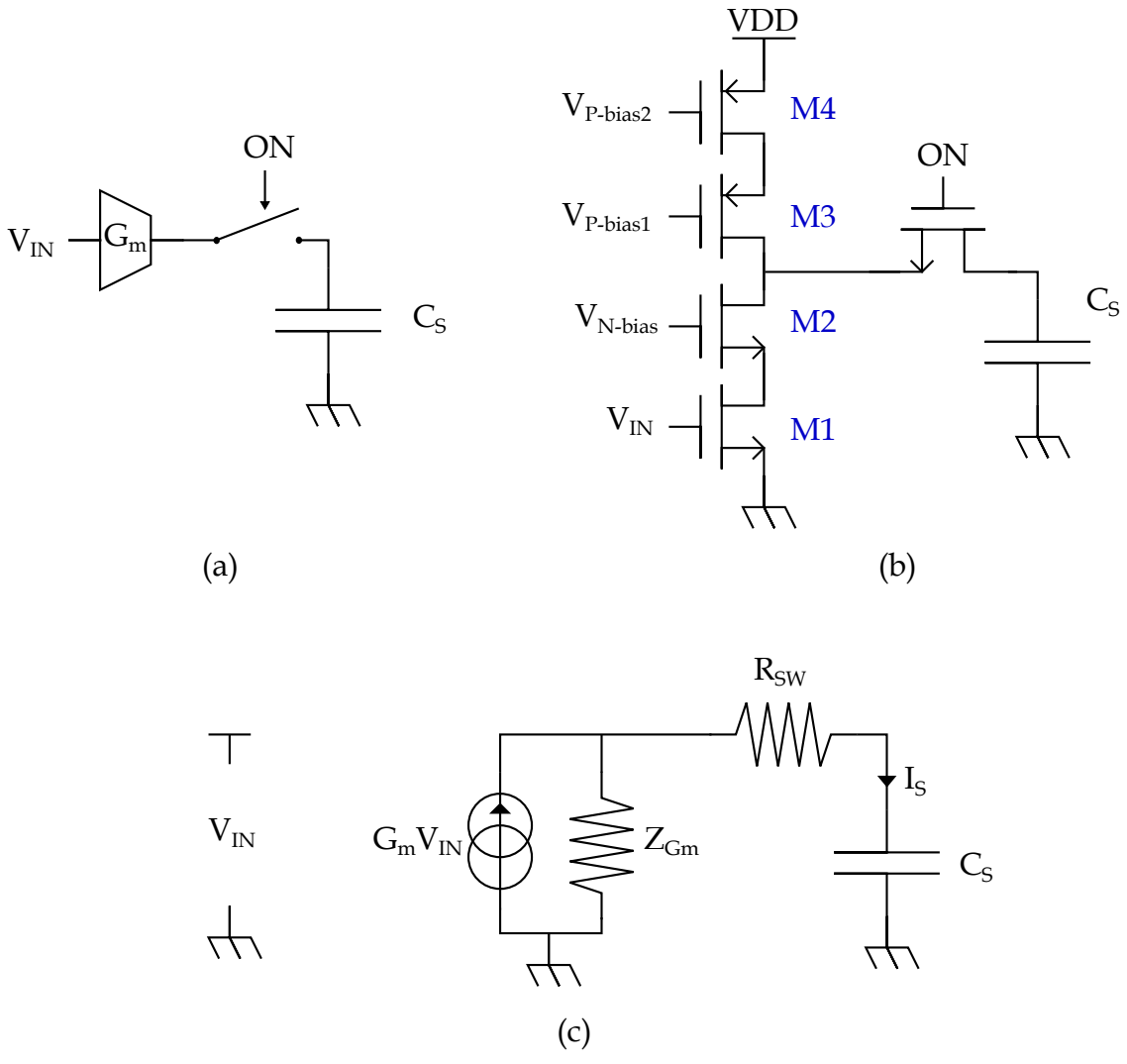


Figure 3.1: Basic charge domain sampler (a), corresponding schematic including a high-gain and high-impedance amplifier (b) and its equivalent model during integration (c)

p-channel current supply is an obvious solution. A sampler including this topology is shown in Figure 3.1 (b). The voltage to current conversion is done by M1. M2 is stacked in order to increase the impedance of the branch. M3 and M4 are used as a high impedance current source.

While considering a real switch, the sampler during the integration period can be modeled as shown in Figure 3.1 (c) where R_{SW} is the impedance of the switch, Z_{G_m} is the output impedance of the transconductance cell and G_m is the transconductance value. The current flowing into the sampling capacitor is then defined in equation (3.1).

$$I_S = G_m V_{IN} \frac{Z_{G_m}}{Z_{G_m} + R_{SW}} \tag{3.1}$$

In order to limit the influence of the switches, two solutions can be envisaged : decreasing the on-resistance of the switches or modifying the architecture. The first solution requires increasing the switch transistor size and consequently an increase in driver size, power consumption and amount of charges injected.

Figure 3.2 (a) shows the transconductance in which M2 and M3 act as enabling switches and are not added in the current paths to C_s as it was the case in Figure 3.1 (b). Consequently the gain reduction due to the switch shown in Equation (3.1) no longer exists. During the integration period, M2 and M3 are saturated while in hold mode, the sampler shows a high impedance because M2 and M3 are both off.

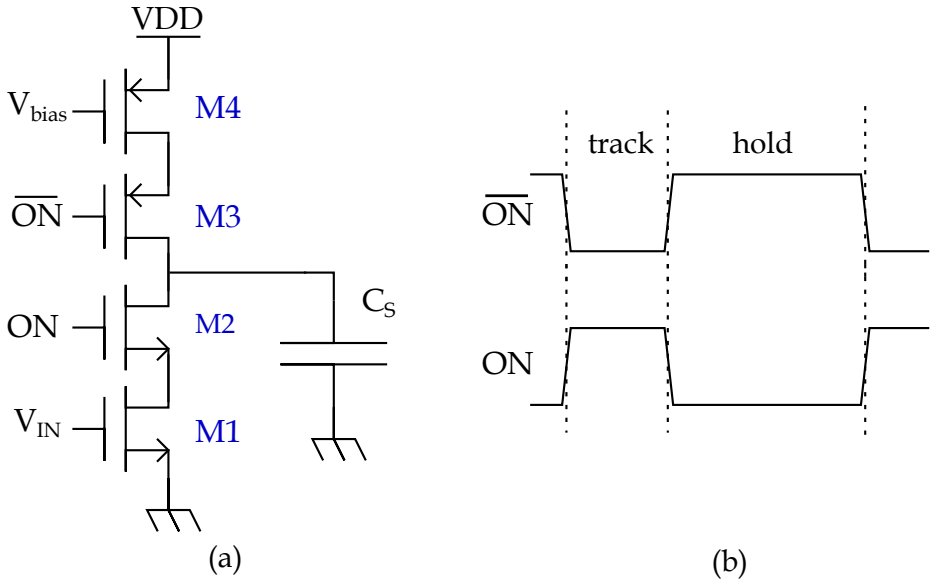


Figure 3.2: Charge domain sampler based on high gain and high impedance amplifier (a) its clock strategy (b)

II.B. Sizing of the samplers

In the first section, the effect of relative size of the transistors of the sampler is analyzed and a trade-off appears in order to increase the efficiency of the sampler (transconductance gain and impedance) and to reduce the parasitic effects due to clock feedthrough . A second part based on the previous trade-off will define the absolute size of the transistors of the samplers taking into account the system level study of the previous chapter.

II.B.1 Relative sizing

In the previous chapter, the system study uses a 10mS transconductance with an infinite output impedance. This subsection details the trade-off between the value of the conductance and the output impedance considering the architecture of the sampler proposed in Figure 3.2. This sampler is equivalent to the model shown in Figure 3.3 where GX, DX, SX represent respectively the gate, source and drain of the X^{th} transistor. V_{GSX}, G_{mX} and R_X are respectively the small signal gate to source voltage, the transconductance value and the drain-source

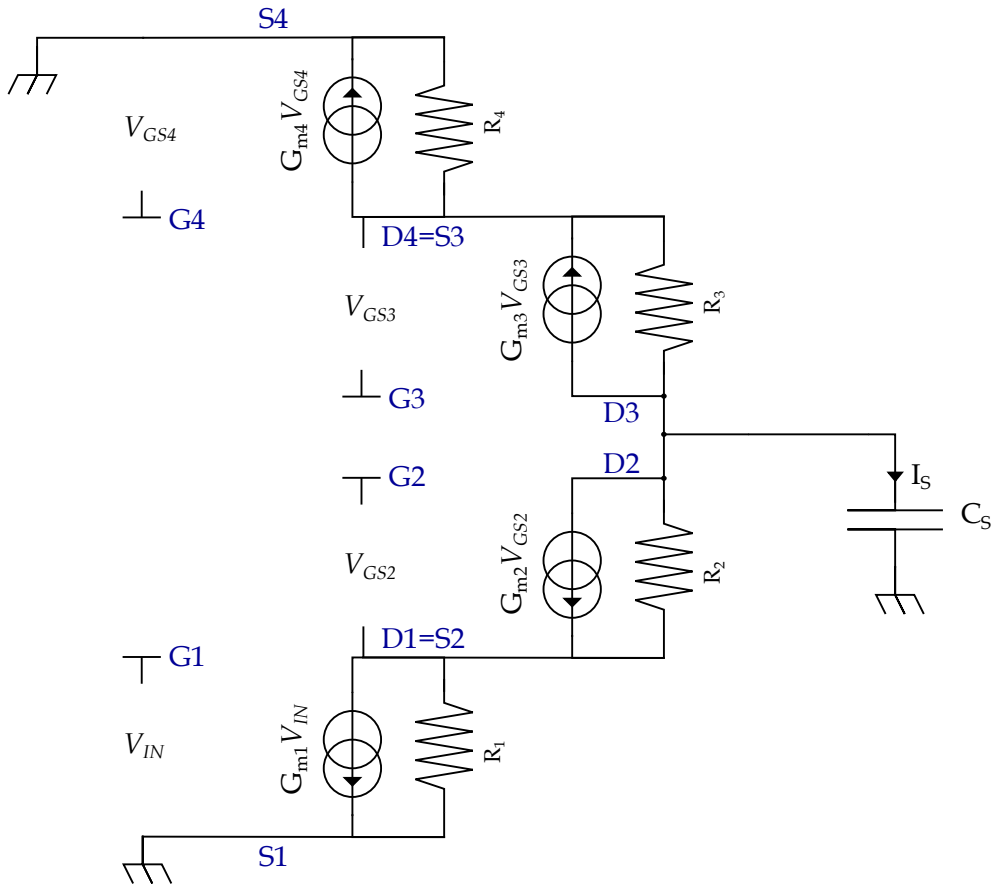


Figure 3.3: Small signal model of the sampler based on high gain and high impedance amplifier during the integration period

resistance of the Xth transistor. This model can be simplified because the gates of M2, M3 and M4 are connected to DC values. Consequently, V_{GS2} is equivalent to V_{DS1}, V_{GS3} is equivalent to V_{DS4} and V_{GS4} is null. The resulting simplified model is shown in Figure 3.4

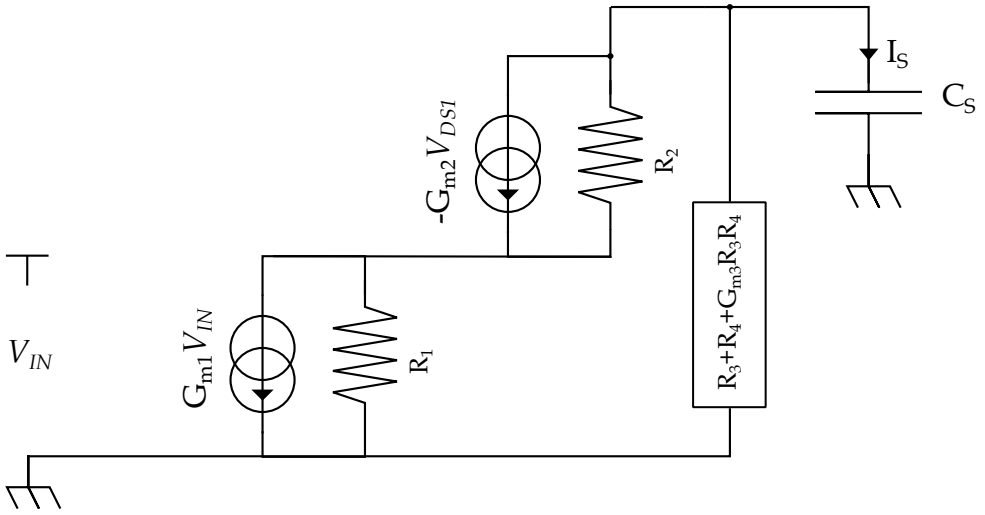


Figure 3.4: Simplified small signal model of the sampler based on high gain and high impedance amplifier during the integration period

This figure shows that M2 is still in the integration path (between M1 and the sampling capacitor). As shown in Equation 3.1, the amount of charges integrated in C_S decreases with the ratio of R_1 and $R_2 + R_1$. Increasing the size of M2 increases the efficiency of the sampler while also increasing the gate capacitance and consequently the power consumption during switching. A good trade off is to size M2 to be equivalent to M1.

While switching transistors, the gate-source and the gate-drain capacitance are quickly charged and discharged. Charge contained in these parasitic capacitors usually flow into the sampling capacitor as shown in Figure 3.5 (a). It results in error on the sampling value. A solution has been proposed in [29] to reduce this effect. Dummy switches are added inside the sampler to catch the charges flowing out of the sampling switch. In the proposed architecture, while taking M2 as large as M3, each switch presents a dummy behavior for the other one 3.5 (b). The amount of charges flowing out of C_{GD-M2} is equivalent to the amount of charges flowing into C_{GD-M3}.

The output impedance of the transconductance cell is given by $R_1 + R_2 + R_2R_1G_{m2}$ in parallel with $R_3 + R_4 + R_3R_4G_{m3}$. To improve the impedance, these two contributions should be equivalent. In order to do so, M4 is taken as large as M1.

As a conclusion, each transistor is sized the same.

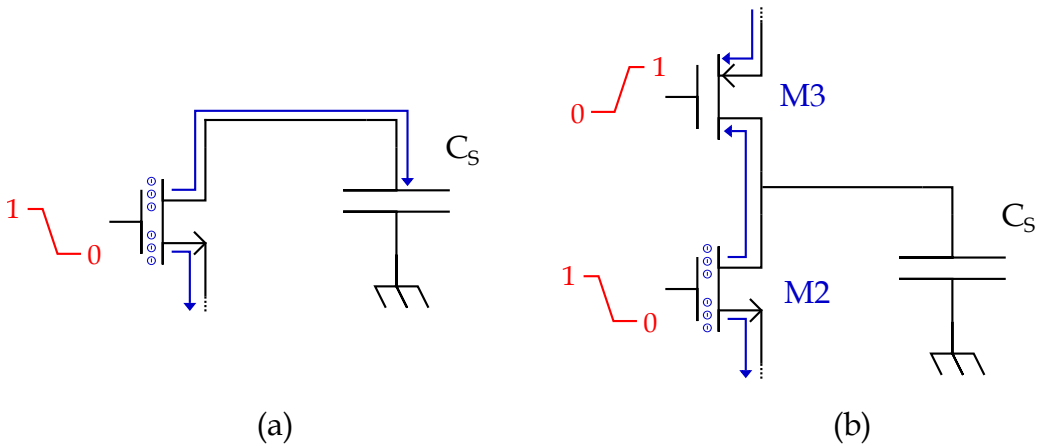


Figure 3.5: Charges injection in the sampling capacitor while switching (a) Charge sharing between transistors during switching in the proposed architecture

II.B.2 Absolute sizing

This part considers the architecture shown in Figure 3.2. The previous section shows that all the transistors of the sampler should share the same width.

In the 28 nm CMOS technology, the minimum gate length is obviously 28nm. With such small transistors, the matching is difficult between several devices (variation $\pm 2nm$ with the process). A solution to reduce the effect of this could be to increase this length. Therefore, the increase also decreases the frequency response of the system. To match the requirements of 21 GHz, the transistors are all 40nm.

This sections shows that a tradeoff should be taken between the target value of transconductance in the previous chapter and all the characteristics of a real sampler : transconductance gain, impedance, switching power.

Figure 3.6 shows the transconductance at 21 GHz versus the transistors' size. Figure

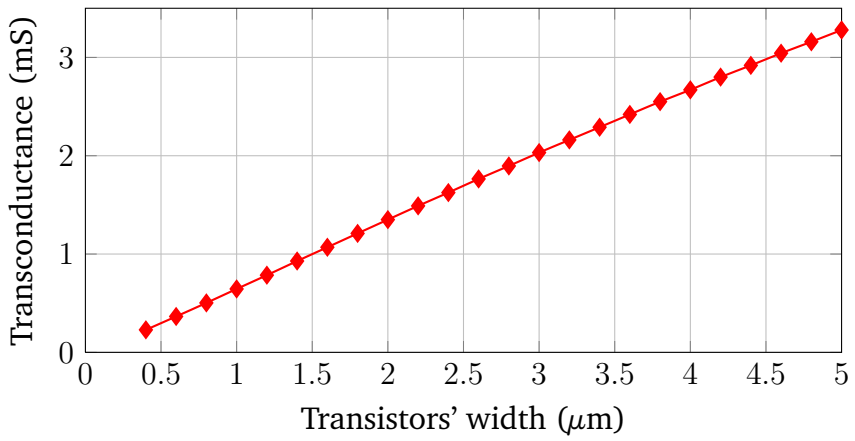


Figure 3.6: Transconductance versus the transistors' width

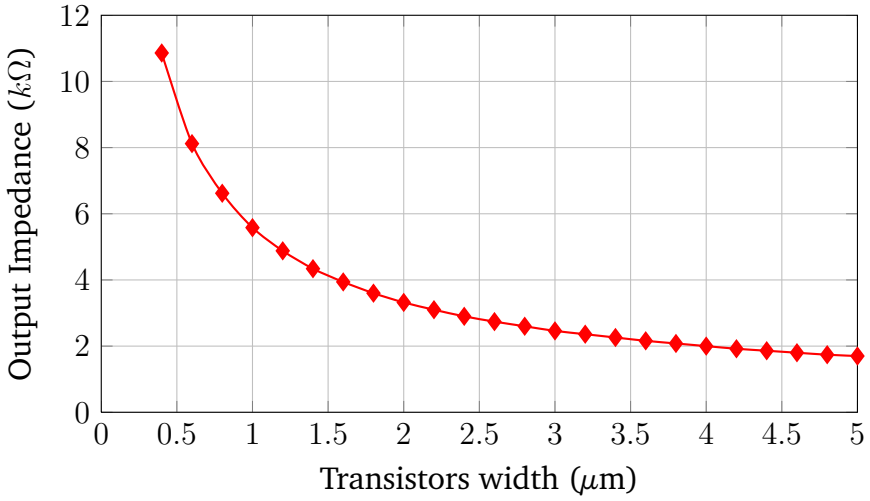


Figure 3.7: Output impedance of the G_m cell versus the transistors' width

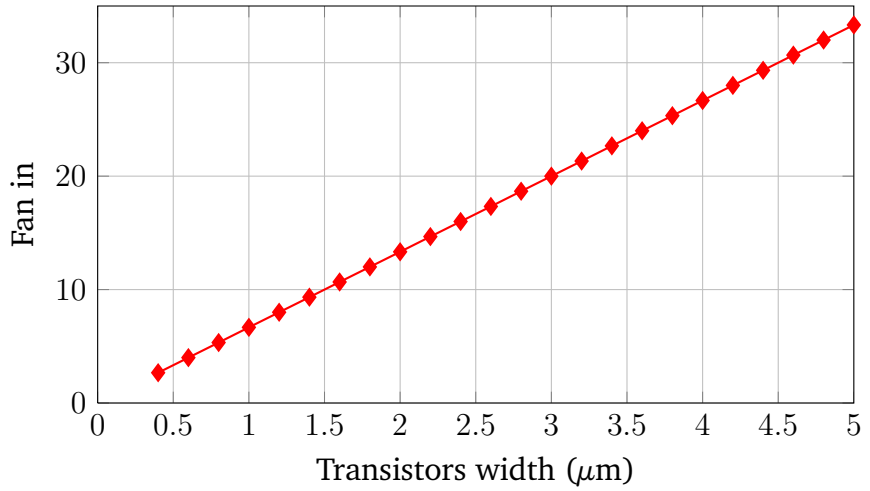


Figure 3.8: Fan in of the switches versus the transistors' width (normalized to the fan in of a minimal inverter)

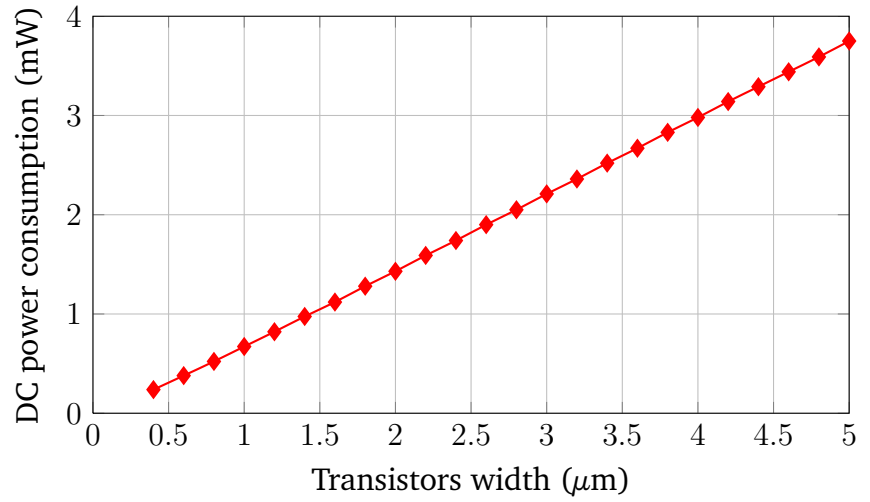


Figure 3.9: DC power consumption versus the transistors' width

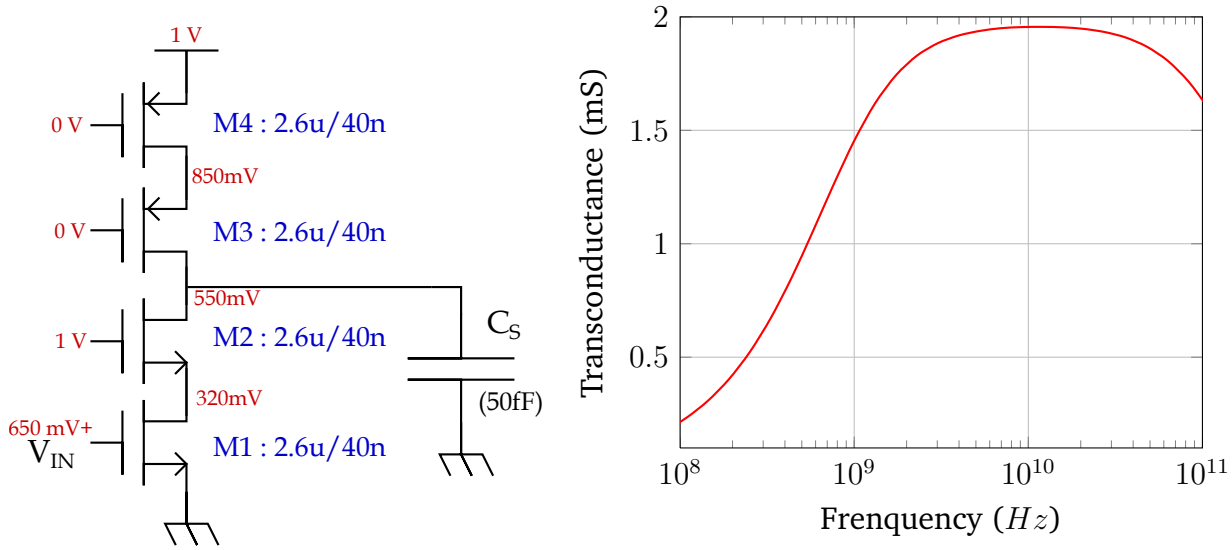
3.7 plots the output impedance of the transconductor versus the transistors' size. This will influence the frequency response of the transconductor. Figure 3.8 shows the fan in of the switches (M2 and M3) of the transconductor versus the transistors' size which is directly linked to the power needed to drive the switches. Figure 3.9 plots the DC power consumption of the transonductor versus the transistors' size.

It shows that the target value of 10mS is not reachable with acceptable transistors sizes in this architecture. Moreover, such a large transconductor would have a very low impedance and the switches would be very large and consequently would consume a lot of power. In the prototype, a width of 2.6 μm is taken as a trade off between these four parameters.

II.B.3 Resulting schematic

Figure 3.10(a) shows the schematic resulting from the considerations taken in the previous sections and the voltages at the biasing point. It shows that with the 1V supply, all the transistors are in triode region.

The frequency response 3.10(b) shows that the sampler reaches a maximum around 20 GHz and can operates over a large range of frequencies.



(a) Resulting schematic of one sampler and biasing voltages

(b) Frequency response of the sampler

Figure 3.10: Resulting sampler implementation with transistor sizes and biasing points (a) and its frequency response (b)

II.C. Mismatch reduction between the samplers

II.C.1 Influence of mismatch between paths on G_m variations

In order to sample successive values, several paths should work in a time interleaved scheme. Simulations have shown that the transconductance value is highly variable with process variations : typically $950\mu S/\mu m \pm 280\mu S$. A solution to avoid the variability problem of different devices is to use a single device as the common G_m for all the paths as shown in Figure 3.11.

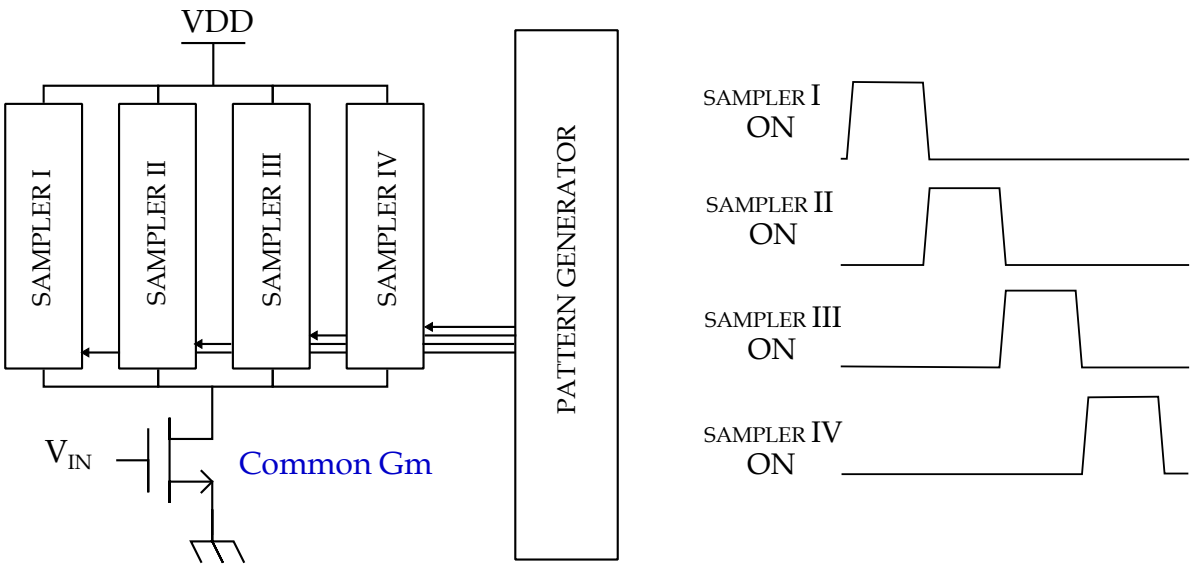


Figure 3.11: Four samplers working in a time interleaved scheme (a) and its corresponding timing diagram (b)

The previous section have shows that the transistors are all in triode mode. In this region, the transconductance gain of a transistor is given by :

$$G_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{OX} \frac{W}{L} V_{DS} \tag{3.2}$$

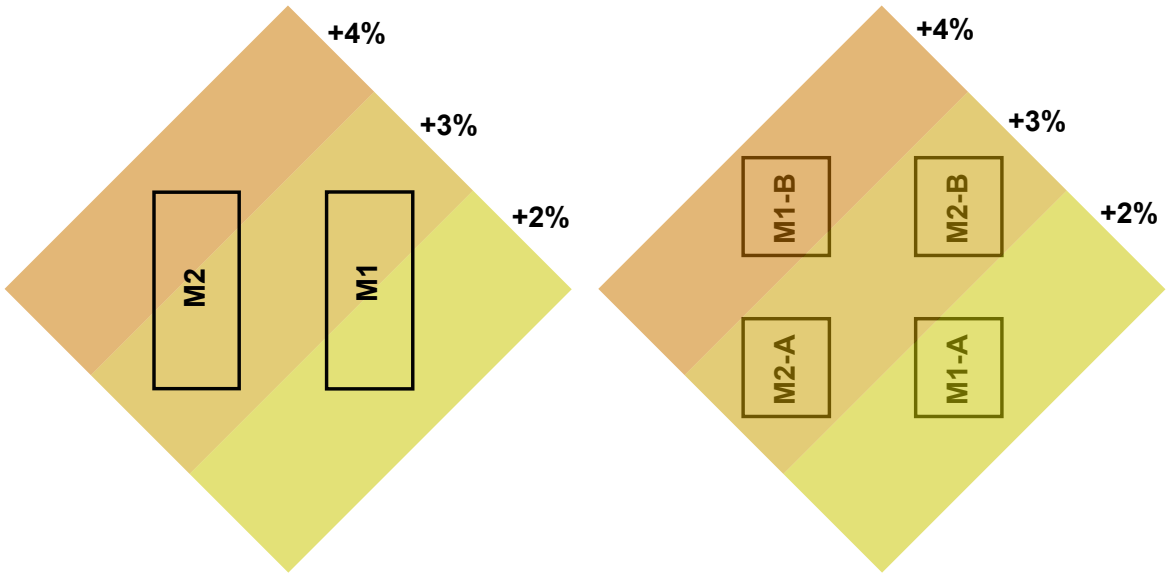
where V_{OV} is the overdrive voltage, W and L are the transistor width and length.

V_{DS} linearly influences the transconductance. Consequently, to have a constant transconductance value for successive integration periods, V_{DS} should be equal for all integration paths. If not, mismatches between two paths (ex : size of the switches, doping levels ...) result in a mismatches of the G_m values for successive integrations periods.

II.C.2 Layout solutions to limit these mismatches

In order to limit the variation of the G_m between paths, the first target is to take care of the layout design. The Common Centroïd layout technique is well known for reducing the effects of the linear gradient [30].

Let's assume the variation of a "X" parameter with a diagonal gradient as shown in Figure 3.12. The target is to match two transistors M1 and M2. Figure 3.12(a) is a basic layout. The value of X for M1 is +2.5% while it is equal to +3.5% for M2. Figure 3.12(b) uses a special technique of layout called common centroid: each transistor is divided in several parts distributed in the layout. With this special distribution, both devices share the same center. With this technique, the average value of X is 2% for M1-A and 4% for M1-B, so for M1, the average value is 3%. In the same way, the average value for M2 is also 3%. In this case, the two transistors are matched. This technique has been used to match the transistor used as switches inside the samplers (Figure 3.13).



(a) (b)

Figure 3.12: Classical layout for two transistors (a) and common centroid layout (b)

Figure 3.12(b) shows one solution for the distribution of the transistors in the layout. The next step is to connect these separated parts of the devices. The way they are connected influences the parasitics on the path. In order to keep the same frequency response for each path, as represented in Figure 3.13, the routing is fully symmetric for each interconnection.

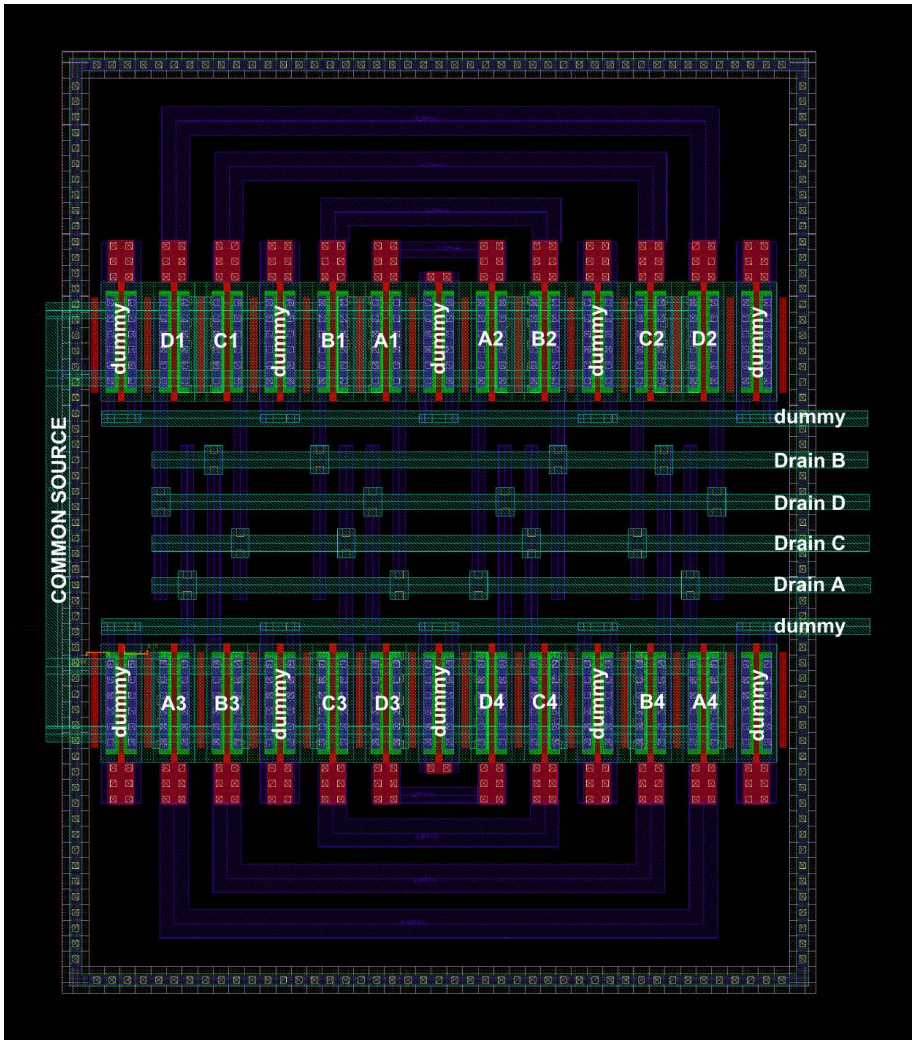


Figure 3.13: Layout of four matched switches

II.D. Sampling capacitors

In CMOS technology, three solutions are available to create a capacitor : Metal-Oxide-Metal (MOM), Metal-Insulator-Metal (MIM), Metal-Oxide-Semiconductor (MOS) and PN junctions, also called varicap. This latter is not interesting in our application because the capacitance is highly variable and dependent on the bias voltage. The first three solutions are developed in the following paragraphs.

II.D.1 MOM Capacitors : metal-oxide-metal capacitors

The very fist example of MOM capacitor is the plane capacitor between two levels of metals. The capacitance is given by (3.3).

$$C = \frac{A\epsilon_0\epsilon_r}{t} \tag{3.3}$$

Where t is the insulator thickness, ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of the insulator, A is area of the capacitor. Meanwhile, the plane capacitor can not offer very high capacitance value because in 28nm CMOS back-end, the oxide thickness between two levels of metal is 80nm. For $1um^2$, with $\epsilon_r = 4$, the capacitance is lower than 1fF. A solution to increase this density is to use both vertical and horizontal flux. An interdigitated MOM capacitor on one single metal is shown in Figure 3.14. The capacitance density can reach $7fF/um^2$ while using all thin metals.

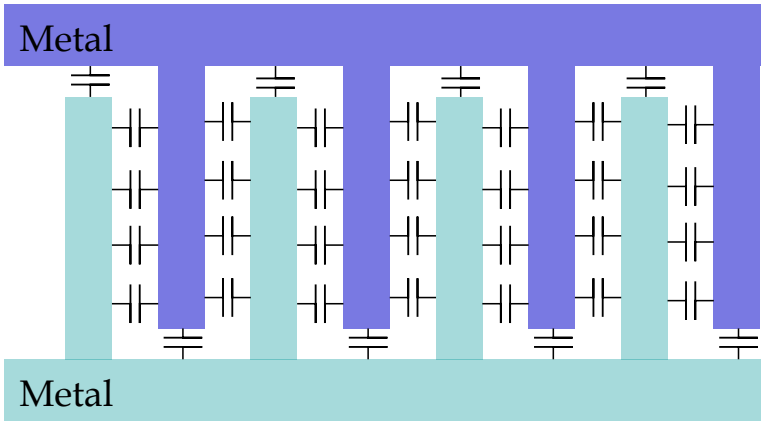


Figure 3.14: Interdigitated MOM capacitor

II.D.2 MIM Capacitors : metal-insulator-metal capacitors

Using a dedicated optional mask, planar MIM capacitors can be created. The MIM insulator is thiner ($t = 11.5nm$) and has a higher relative permittivity ($\epsilon_r = 25$) than the oxide, consequently MIM capacitors can reach higher capacitance values (up to $19fF/um^2$) than MOM.

However, MIM capacitors need a special option which uses 4 additional masks for additional cost. Moreover, this capacitors are placed between thick metals, 9 level above the active area. Consequently, a lot of contacts are needed to reach them which results in high access resistance. This access resistance is critical in high frequency applications. As a conclusion, MIM capacitors are not suitable for the proposed application.

II.D.3 MOS Capacitors : metal-oxide-semiconductor capacitors

In the small signal model of a transistor, capacitors appear between gate, drain, source and bulk. These capacitors are shown in Figure 3.15.

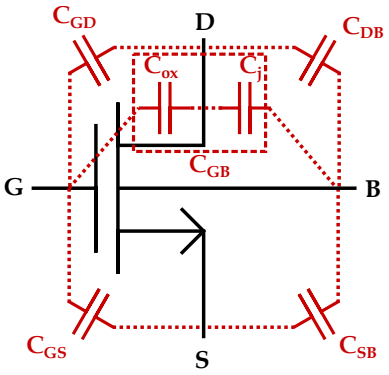


Figure 3.15: Capacitors in a MOS transistor

By connecting the drain, source and bulk to ground, a capacitor appears between the gate of the transistor and ground. It is composed of C_{GS}, C_{GD} and C_{GB} in parallel as shown in the vertical view of the N-MOS transistor shown in Figure 3.16. C_{GB} is a combination of C_j and C_{ox}

As the capacitor value is a function of the insulator thickness and the oxide is very thin (1.4nm), large capacitors can be implemented in small silicon area : the density of this type of capacitor is approximatively $22fF/um^2$.

The drawback of this capacitor is that C_{GB} is a function of the bias voltage. When oper-

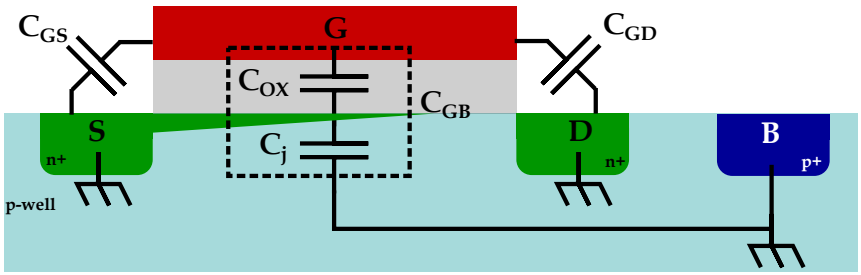


Figure 3.16: Vertical view of the NMOS transistor used as capacitor

ating in weak inversion or sub threshold, the channel resistance is high and consequently C_j and C_{ox} are placed in series. This results in a low C_{GB} value. When the transistor operates in strong inversion, the channel resistance is very low and C_j is placed in parallel with C_{ox}. This results in a high C_{GB} value. Figure 3.17 shows the total capacitance versus the bias voltage.

In the proposed architecture, the voltage is defined by the sampler. In this region, the capacitance is a linear function of the bias voltage. Consequently, an error the bias voltage will modify the sampling capacitor and so the transfer function.

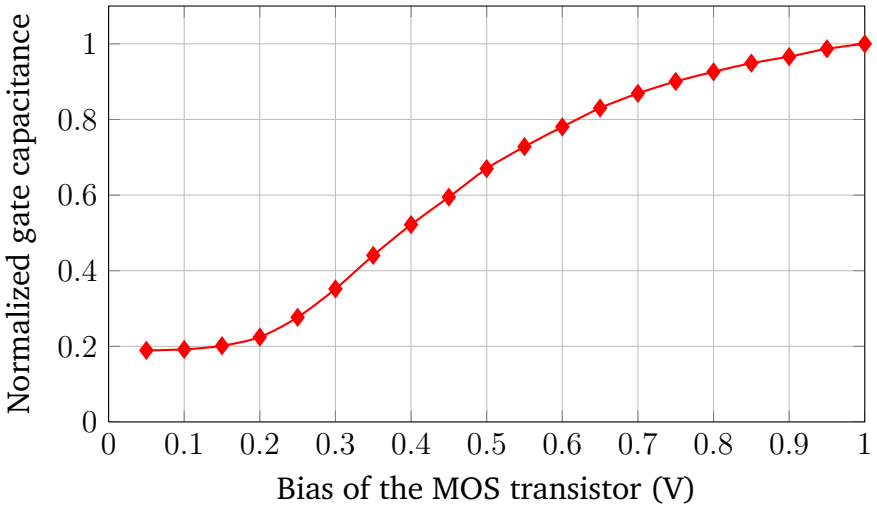


Figure 3.17: Total capacitance vs bias of the MOS transistor used as capacitor

II.D.4 Conclusion and implementation

Table 3.1 sums up the pro and cons of each capacitor. The capacitance density is higher with MOS capacitors, the routing metals are still available over the capacitors, and they do not need additional masks, consequently MOS capacitors are more interesting in this application.

Type	**Density**	**Linearity**	**Repro-ducibility**	**Additionnal Mask**
MOM	-	+	- -	No
MIM	+ +	+ +	+ +	Yes
MOS	+ + +	-	+ +	No

Table 3.1: Benchmark of integrated capacitors [4]

The bias voltage is high regarding the threshold of the transistor. Consequently, the transistor used as capacitor always operates in strong inversion mode. In this region the capacitors is linear. The fact that the MOS capacitor is not linear in the others regions is not considered.

The system study presented in the previous chapter uses a 50 fF sampling capacitor. The layout has been performed in order to limit the mismatches between the several paths. In order to do so, minimal size transistor have been replaced by large transistors and each capacitor has been divided in several parts with the common centroid layout introduced in section II.C.2

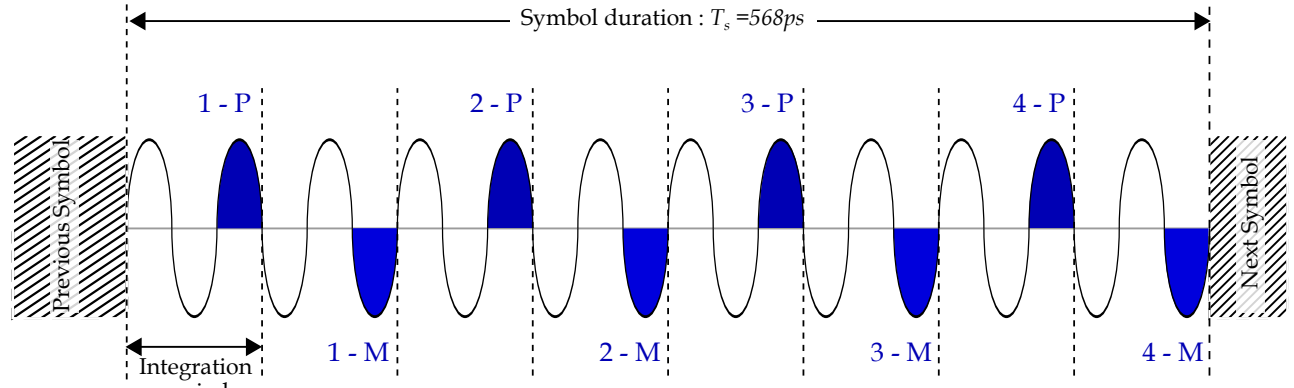
III. From the functionality to the sampler layout

III.A. How to correctly receive a symbol?

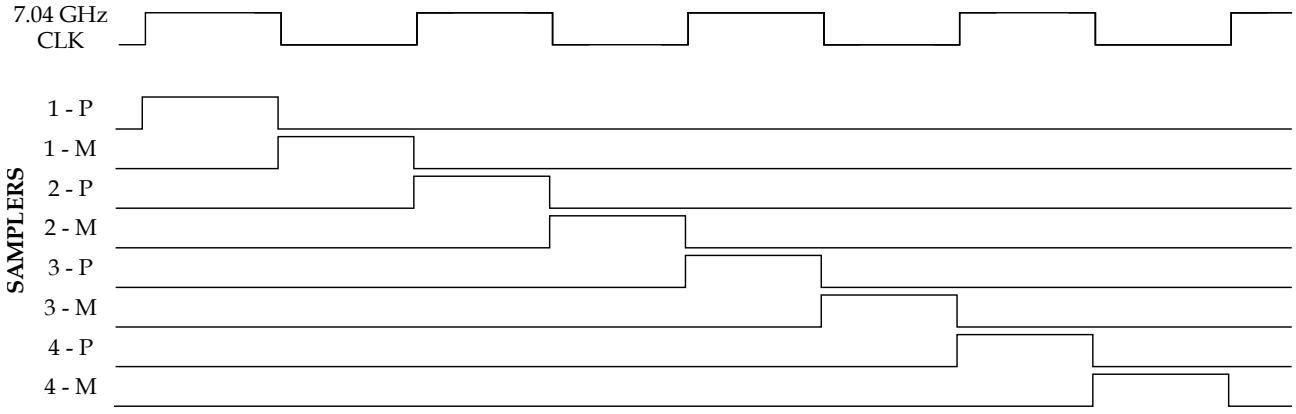
In this section, it is assumed that the sub-sampling clock is ideally synchronized to the incoming data symbols and to a submultiple of the RF frequency.

Each symbol is composed of four samples and each of these samples is divided in a positive and a negative phase. The following naming conventions are taken in Figure 3.18 : the Xth sample is divided in its positive phase "X-P" and its negative one "X-M".

As developed in the previous chapter and shown in 3.18 (a), in order to downconvert a signal from $f_{IF} = 21.12GHz$, samples should be taken at $f_{RF} = 7.04GHz$. In order to decimate the data to $f_{data} = 1.76GHz$, four successive samples need to be averaged.



(a) Input RF Signal : 1 symbol divided in 8 sucessive samples
The plain lobes correspond to the effectively integrated charges



(b) Windows in which the samplers are integrating the input signal

Figure 3.18: Successive integrations for the reception of a complete symbol

Each sample is taken with a different sampler to avoid interference between samples due to finite impedance of the samplers. Each sampler is named after its corresponding

sample, for example, the sampler which samples the negative phase of the second sample is named "$2-M$". Figure 3.18 (b) shows the needed pattern in order to integrate eight samples. The input frequency is $4 \cdot f_{data}$ and the needed integration window (T_i) is $1.5/f_{IF}$, as described earlier. The integration pulses can be directly created using the input clock. Consequently, the duty cycle of the reference clock should be strictly kept at 50% to ensure a correct constellation. This will be discussed in section IV.A.1.

III.B. What is needed to perform continuous time operation?

The previous section shows how one path can sample one single symbol. Once the symbol is sampled, a non-negligible amount of time is needed for averaging and evaluating the charges contained in the capacitors as well as reseting the capacitors. Only two paths would be required from a functional point of view. Meanwhile, in order to avoid high impedance periods at the output, four paths are considered in an interleaved scheme. Each path performs a single operation during one symbol. The corresponding timing diagram is shown in Figure 3.19

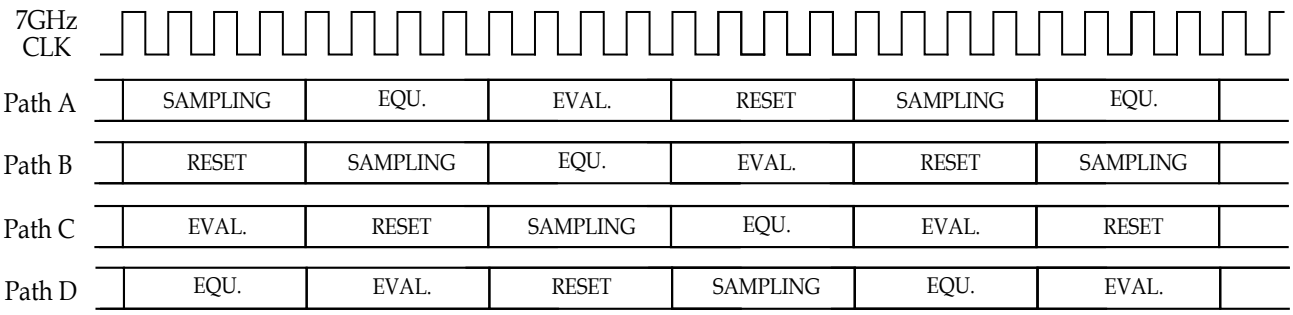
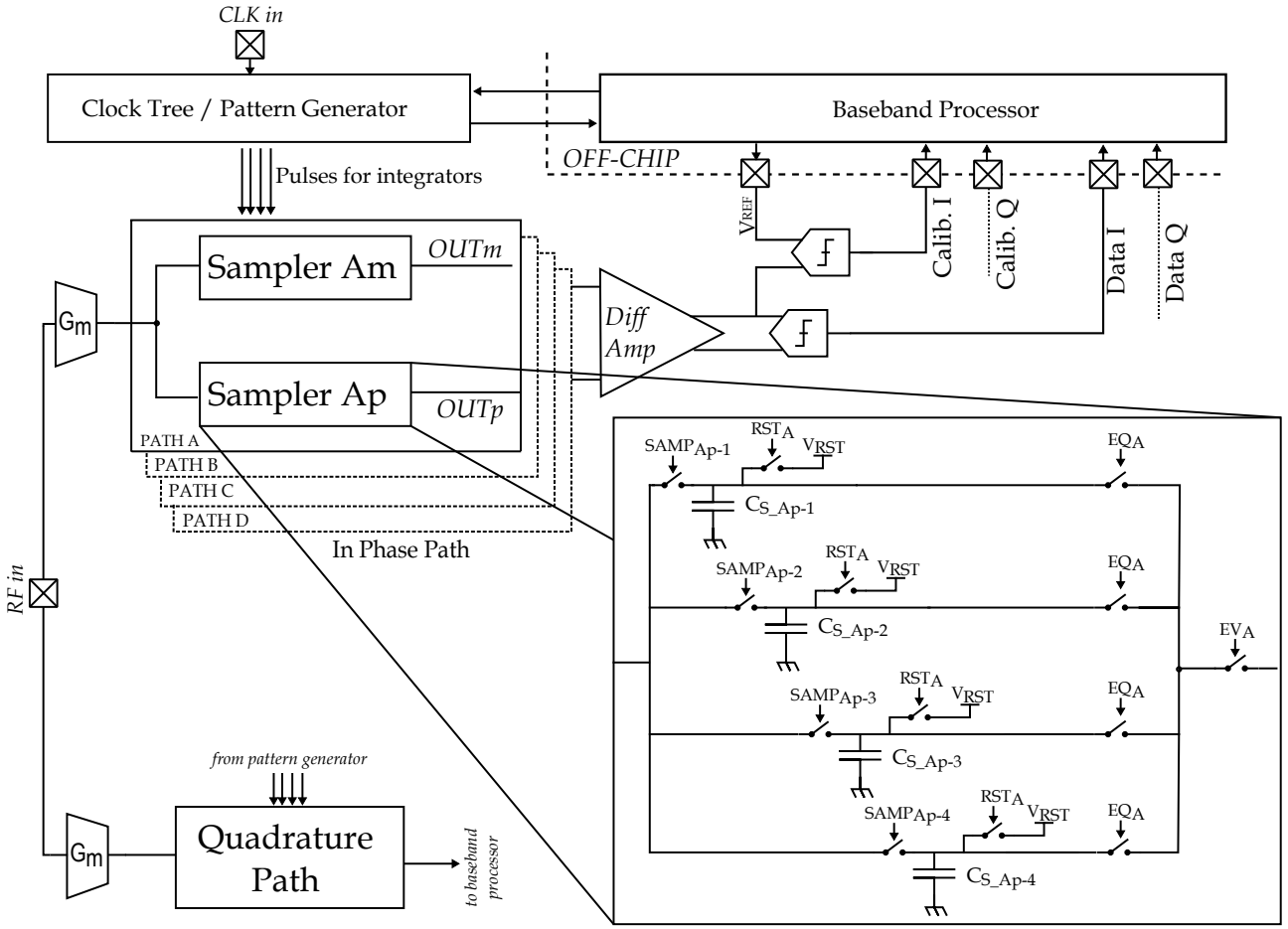


Figure 3.19: Timing diagram of four paths working in a time interleaved scheme

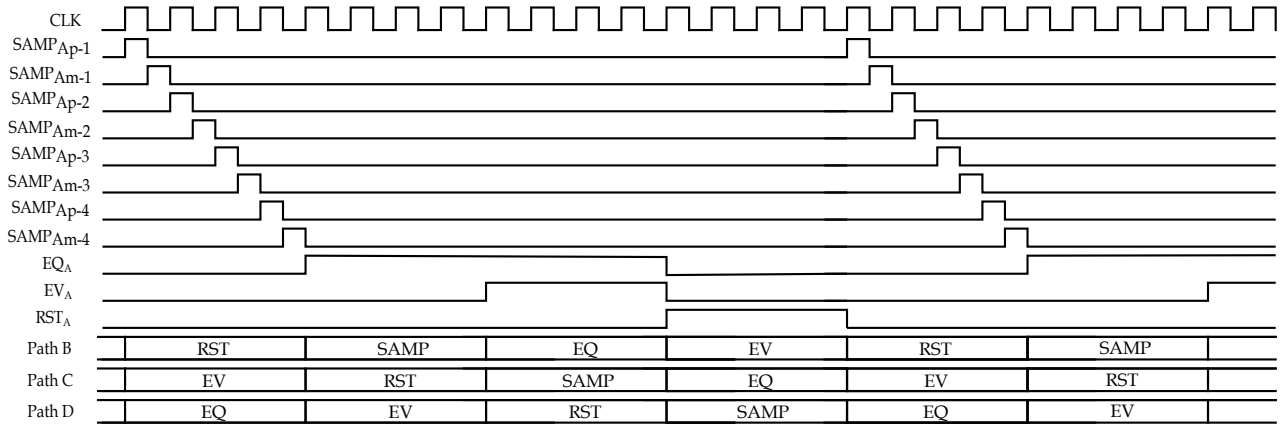
III.C. Resulting sub-sampler implementation

The combination of needs in terms of sampler and timing diagram detailed is sections III.A. and III.B. leads to the principle of operation of the proposed sampler shown in Figure 3.20.

It is composed of 4 paths (A to D) working in an interleaved scheme. Each path comprises two parts: a positive one which samples the signal during a first T_i period and a negative one which samples the signal during the next T_i period, as described on the timing diagram of Figure 3.20 (b). The final result is the difference between both sides.



(a) Subsampler implementation



(b) Timing Diagram

Figure 3.20: Proposed sub-sampler implementation and timing diagram

In the first phase, four successive samples are accumulated at f_{SUB}. The second phase is the averaging of the four values by turning the EQ switches on. All sampling capacitors are identical, so averaging of four successive samples implements a finite impulse response (FIR) filter function because the charges are equally partitioned between the four capacitors.

During the third phase, the EV switch is activated and connects the sampling capacitors to the output amplifier. This amplifier acts as a buffer and introduces bandwidth limitations. When the switches turn on and off, charges are injected and pumped onto the capacitors and this results in voltage glitches. As they appear as a common mode signal, these glitches are rejected by the differential amplifier. The four paths working in parallel ensure that capacitors are always connected to the differential amplifier input in order to avoid an undefined state. The output data value is extracted by a Schmitt trigger. A second Schmitt trigger monitors the absolute value just after the differential amplifier. This monitoring is further used to perform equalization of the output constellation.

During the fourth phase, the sampling capacitors are reset to clear the previous sample values.

III.D. Layout of the subsamplers and interconnections

III.D.1 Layout of the subsampler

The layout of four matched samplers is shown in Figure 3.21. In order to improve matching between each sampler, each device (switches, capacitors, and current sources) has been designed using the common centroid layout technique developed in section II.C.2

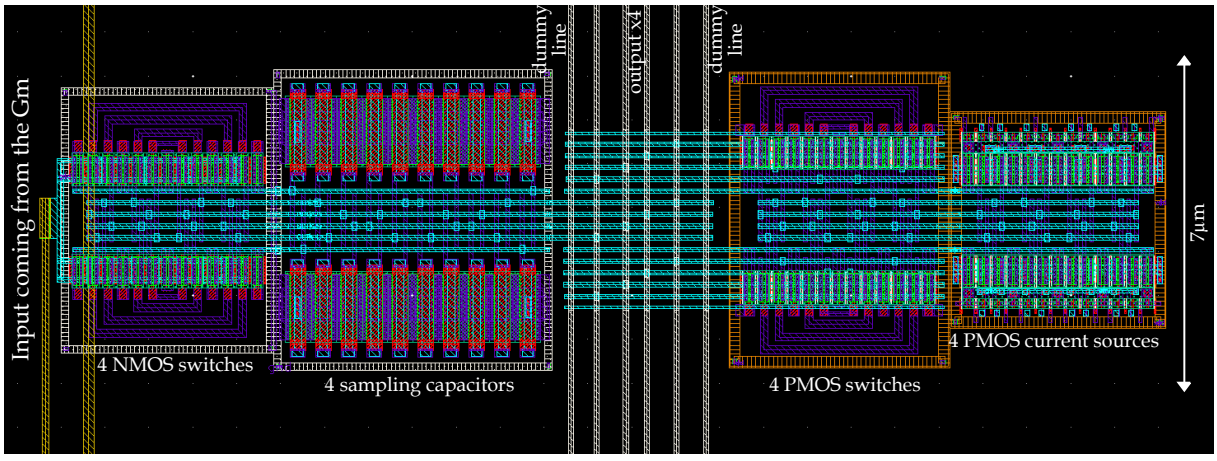


Figure 3.21: Layout of four matched samplers

III.D.2 Optimizing the parasitic elements

Section II.C.1 has shown that a common Gm should be used for all the paths. This represents a total of 32 switches divided in 8 basic cells of 4 switches. Considering the proposed implementation in Figure 3.20 for a basic cell and while adding some space for reset and charge sharing switches, the final layout is quite long : 150μm as shown in Figure 3.22.

The resistance of thin-metal lines is around $10\Omega/\mu m$ for 50nm-wide lines and $1.5\Omega/\mu m$ for 200nm-wide lines. Consequently, resistance of lines can not be neglected while considering the connections between the common G_m and the samplers. In order to limit the effect of these lines, two solutions are available : minimizing or optimizing these parasitic elements.

Regarding the model given in Figure 3.4, resistances of lines act as series resistors and directly reduce the amount of charges integrated into the sampling capacitor. Figure 3.22 shows the two possible connection schemes. With the shortest connections, sampler 1 has a very low access resistance while sampler 4 experiences a large one. With the second approach in which all the connections are matched, the access resistance is large but equivalent for all the samplers.

In order to evaluate which solution is the most suitable, parasitics have been extracted for these two configurations. AC simulations show the quantity of charges integrated in each sampler for both configurations.

	Shortest Connections	**Matched Connections**
Sampler 1	1.964 mS	1.777 mS
Sampler 2	1.903 mS	1.777 mS
Sampler 3	1.856 mS	1.777 mS
Sampler 4	1.794 mS	1.777 mS

Table 3.2: Integrated current inside the sampling capacitor at 21 GHz

In the shortest connections configuration, this value decreases from 1.964 mS for the sampler 1 to 1.794 mS for the sampler 4.

In the second configuration, when the connections are matched, the transconductance is 1.777 mS. This is lower than all the samplers of the previous configuration because the access resistance is high for all the samplers. However this solution is most interesting because the

gain of the sampler is the same wherever they are placed on the layout.

This example illustrates that a trade-off should be taken between the value of parasitic elements and the matching required between different paths. This design methodology has been used several times in the layout of the complete chip.

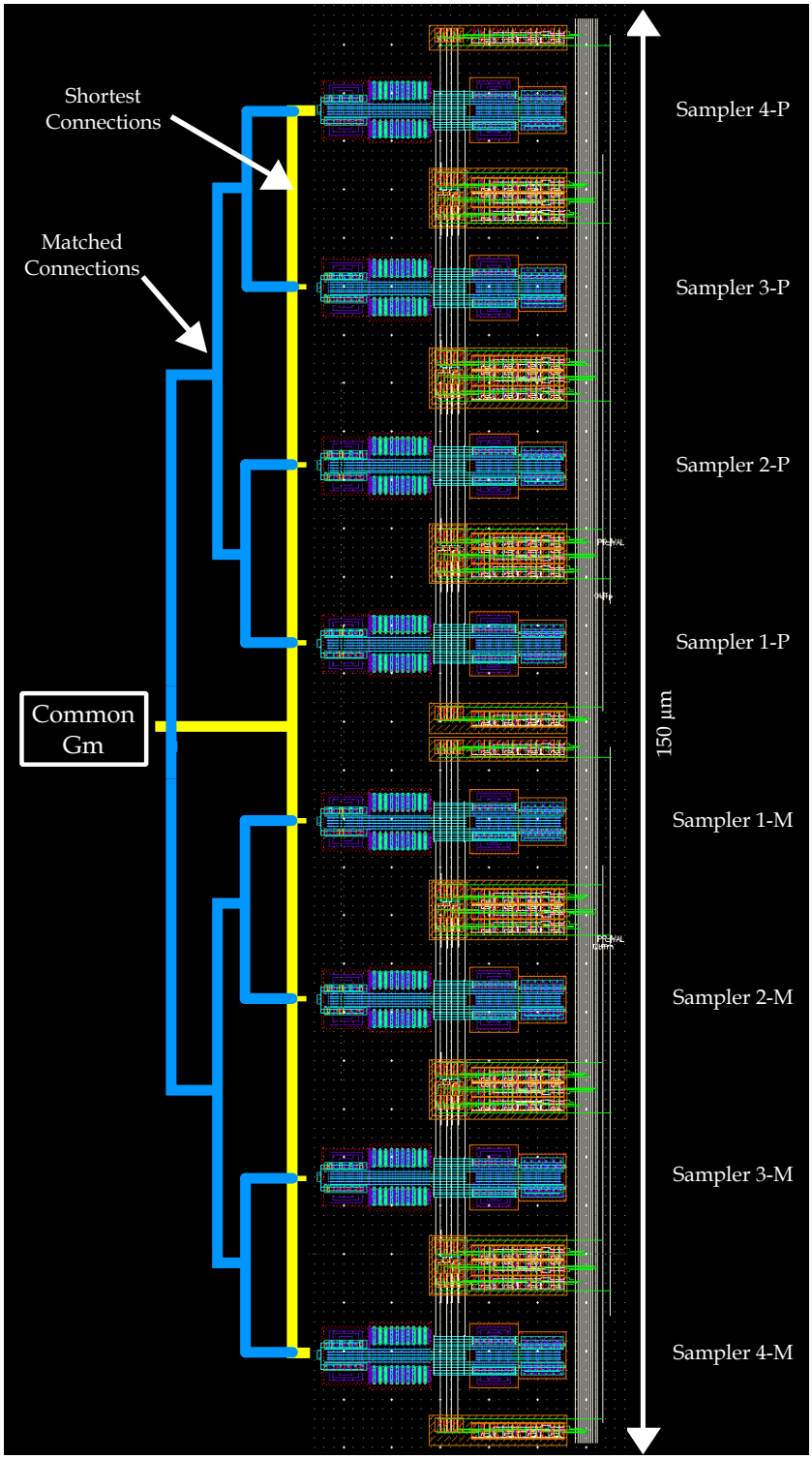
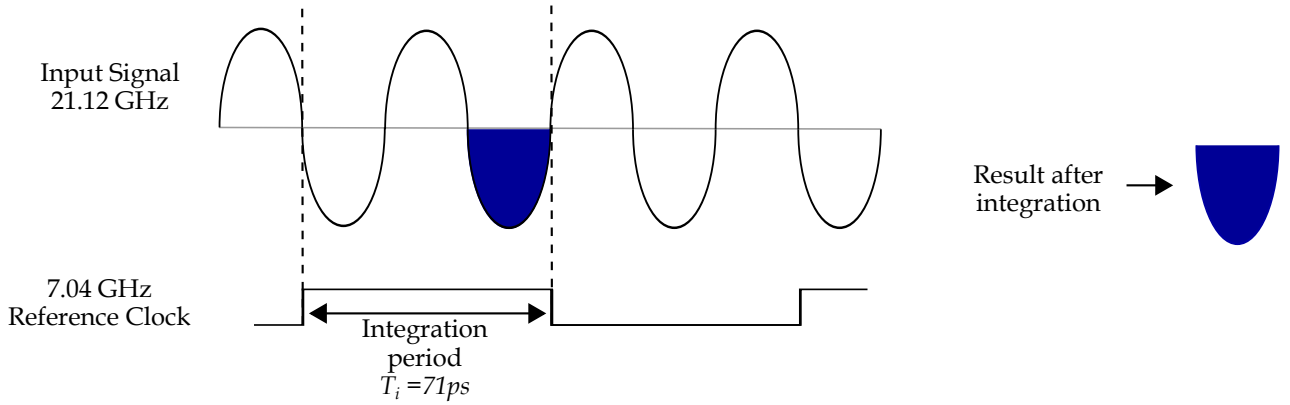


Figure 3.22: Layout of a complete sub-sampler (I or Q)

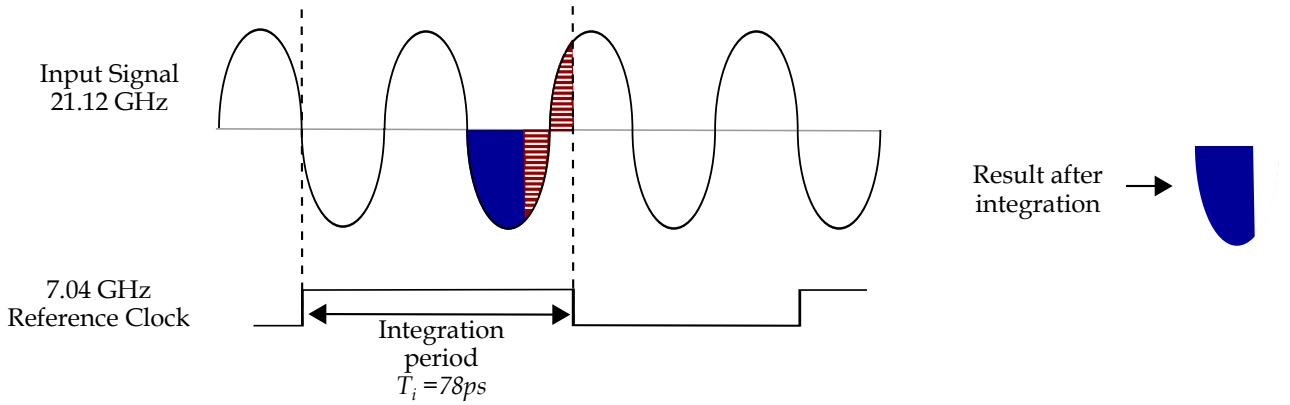
IV. Pattern generation for sampler operation

IV.A. Monitoring of the input clock

As shown in Figure 3.20, the input signal frequency is $f_{IF} = 4 \cdot f_{data}$ and the needed integration period (T_i) is $1.5/f_{IF}$, as described earlier. When this integration period is ideal, the sampled value reaches a maximum as shown in Figure 3.23 (a). When this integration period is not ideal (as shown in Figure 3.23 (b), the window is too large), the sampled value does not reach the maximum.



(a) Ideal case



(b) Non-ideal case : example when the integration period is too long

Figure 3.23: Result after the integration process in the ideal case (a) and in a non-ideal case (b)

This ideal integration period corresponds to an exact duty cycle at 50% of the 7.04 GHz input clock. In a realistic case, this duty cycle can vary due to variations of bias voltages, temperature or process. Consequently, the duty cycle of the reference clock should be strictly regulated at 50% to maximize the integrated value to optimize the integration process. This regulation is discussed in this section.

IV.A.1 Effect of the deviation of the duty cycle

A QPSK signal at f_{IF} frequency is defined as follows:

$$V(t) = I \cdot \sin(2\pi f_{IF} t) + Q \cdot \cos(2\pi f_{IF} t) \quad (3.4)$$

where I and Q are respectively Inphase and Quadrature amplitudes and f_{IF} is the intermediate frequency. Considering an integration interval from 0 to T_i, where T_i is $1.5/f_{IF}$, the output corresponds to the I value. Considering an error on the integration time, a small part of the I (resp Q) signal will leak onto the Q (resp I) value and this will result in coupling between both values. Consequently the integration window width has to be monitored in order to maintain the sensitivity of the receiver.

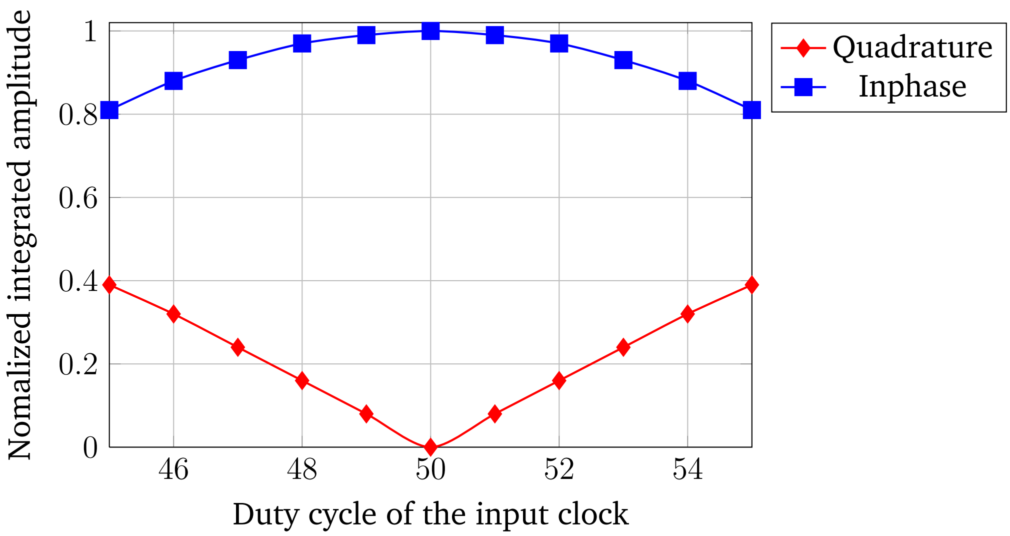


Figure 3.24: Coupling between I and Q after integration

Figure 3.24 illustrates how I and Q are coupled together as a function of the input clock duty cycle. This Figure separates the result of the integration of the two parts of the signal : the in-phase part which holds the data 'I' and the quadrature part which holds the data 'Q'. It shows that the integration of the in-phase part of the signal reaches a maximum for an ideal duty cycle of 50% while the integration of the quadrature part is null for this ideal duty cycle. This calculation considers an ideal sampling instant.

For a duty cycle variation of 1 %, the integrated value on the in-phase path is nearly equal to 1, but on the quadrature path, the value is 0.1. This means that there is a coupling noise that limits the SNR to 20 dB in this case.

IV.A.2 Duty Cycle Regulation : Algorithm and system

State of the art on duty cycle correctors mainly focuses on high speed locking solutions for low frequency clocks (up to 2 GHz)[31],[32]. In our application, the reference clock frequency is higher but the locking time is not critical. Consequently, the idea is to monitor the time domain average of the clock signal which directly relates to the duty-cycle. The regulation algorithm is shown in 3.25. The positive and the negative phase of the clock are respectively named CLKP and CLKm.

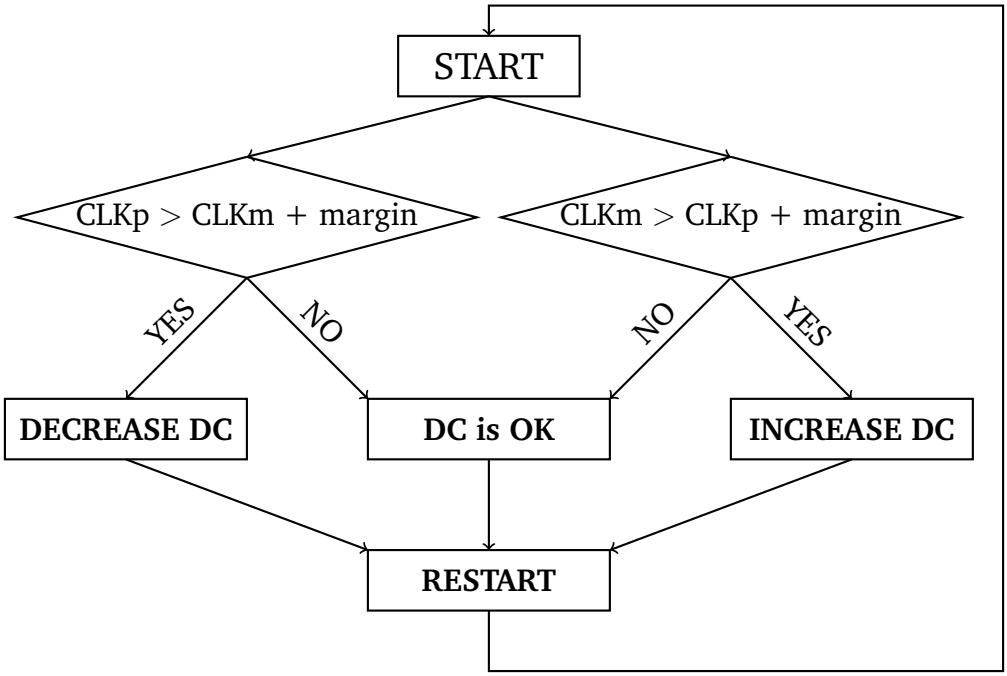


Figure 3.25: Regulation algorithm of the Duty Cycle (DC)

This system is composed of three parts shown in 3.26 : a duty cycle adjuster, a RC stage which extracts the average value and a monitoring system which controls the duty cycle adjuster. The main advantage of this solution is that it operates at low frequencies and is

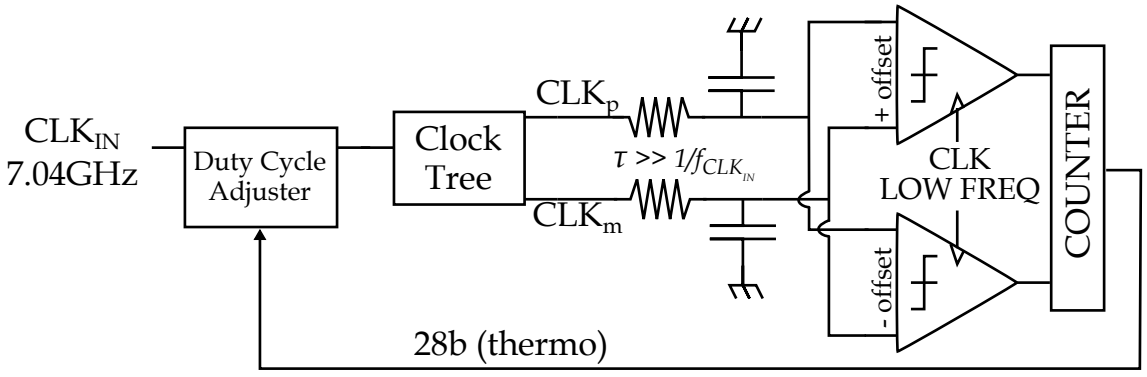


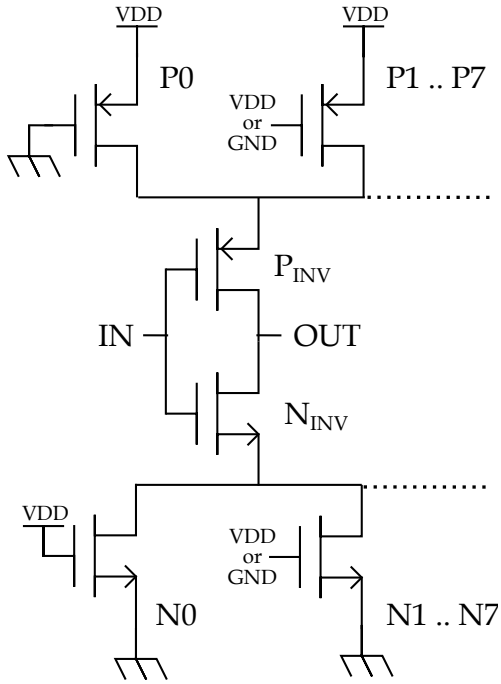
Figure 3.26: Architecture of the duty cycle corrector

sensitive to supply variations.

The margin is used to create a "dead-zone" where CLKp is not exactly equal to CLKm but the difference is acceptable. In order to comply with the previous requirements (+/- 1%) , the dead-zone is 20mV wide.

IV.A.3 Slew-rate controlled inverters used as duty cycle adjusters

In order to modify the duty cycle of a signal, only the rising or the falling edge should be delayed but not both together. For that, one solution is to control separately the slew rate of rising and falling edges of the clock. Figure 3.27 shows the proposed solution based on a basic inverter stacked with a bank of transistors. The inverter constantly operates because P0 and N0 are always active. This path defines the minimum slew rate. Activating N1..7 or P1..7 increase the slew rate for respectively the rising or the falling edge.



Transistor size
(L=28n for all)

Pinv - Ninv	1u
P0 - N0	1u
P1 - N1	560n
P2 - N2	300n
P3 - N3	250n
P4 - N4	210n
P5 - N5	170n
P6 - N6	130n
P7 - N7	110n

Figure 3.27: Schematic of the voltage controlled delay lines and transistor sizes

Figure 3.28 shows how SRC inverters (Figure 3.27) are used as duty cycle adjuster. It illustrates the effect of the control of the slew rate in order to modify the duty cycle. Three different control codes on the N bank are used while the P bank is stuck to a constant value. It shows that for the code $N = 1110000$ the slew rate of the falling edge has been decreased regarding the $N = 1111111$ case. After buffering, this results in delay of this falling edge. The lower the code, the lower the slew rate and the higher the duty cycle at the output.

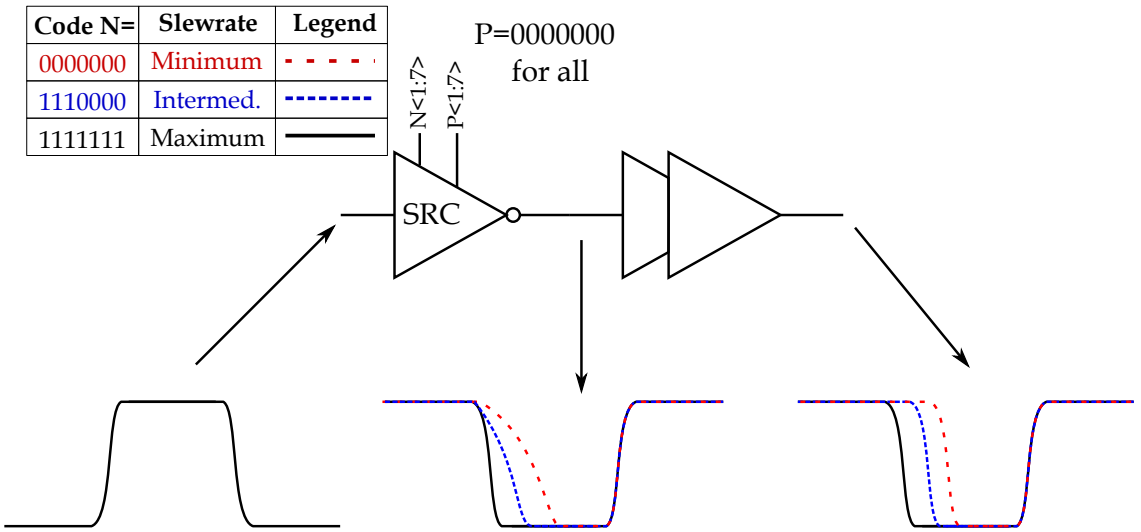


Figure 3.28: Principle of operation of the duty cycle adjuster

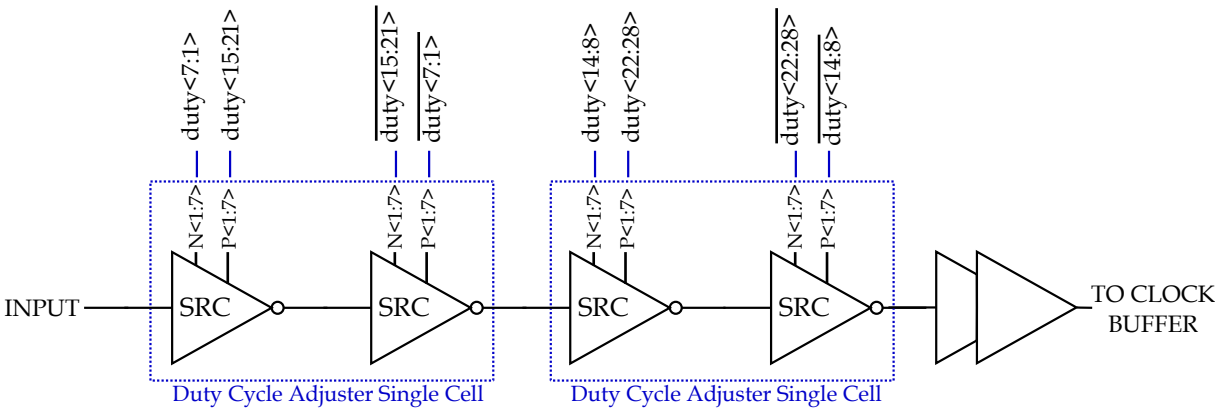


Figure 3.29: Schematic of the duty cycle adjuster assembly

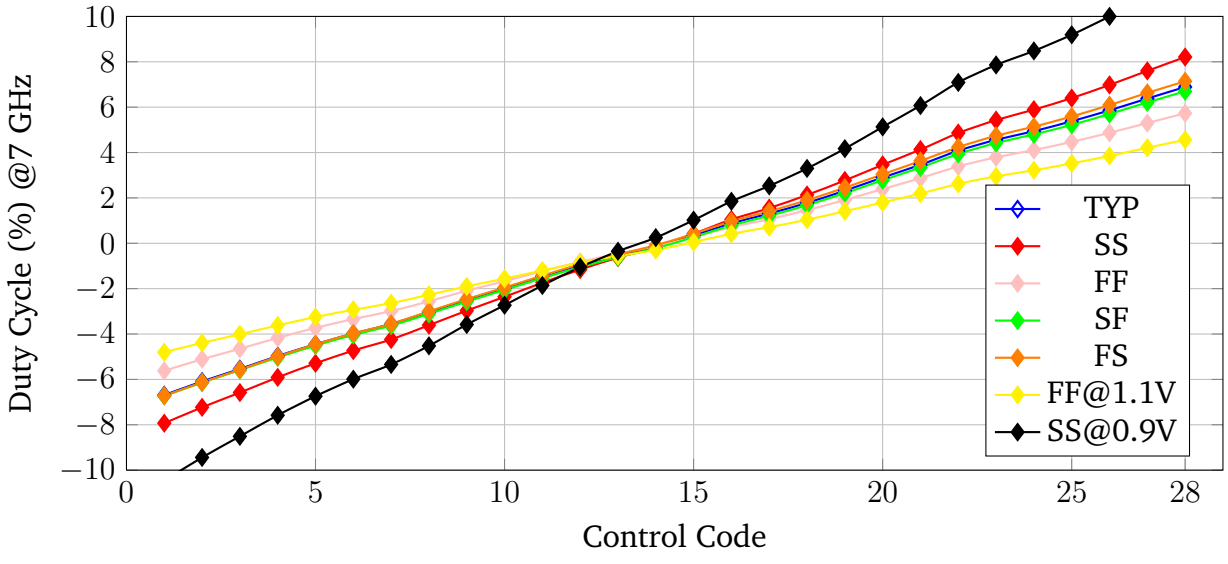


Figure 3.30: Modification of the duty cycle versus the control code

The basic duty cycle adjuster cell shown in Figure 3.29 and Figure 3.30 shows the modification of the duty cycle function of the input code. It shows that for the four SRC inverters used in the duty cycle adjuster assembly, the duty cycle can be corrected up to +/- 5% in all the corners

IV.A.4 Comparators

In order to evaluate the difference between CLKp and CLKm, comparators are needed. A deviation of 1% of the duty cycle relates in a difference of 20mV between the average values of CLKp and CLKm. The comparators presented in [33] shown in Figure 3.31 are based on cross coupled inverters and are consequently able to compare very low differences.

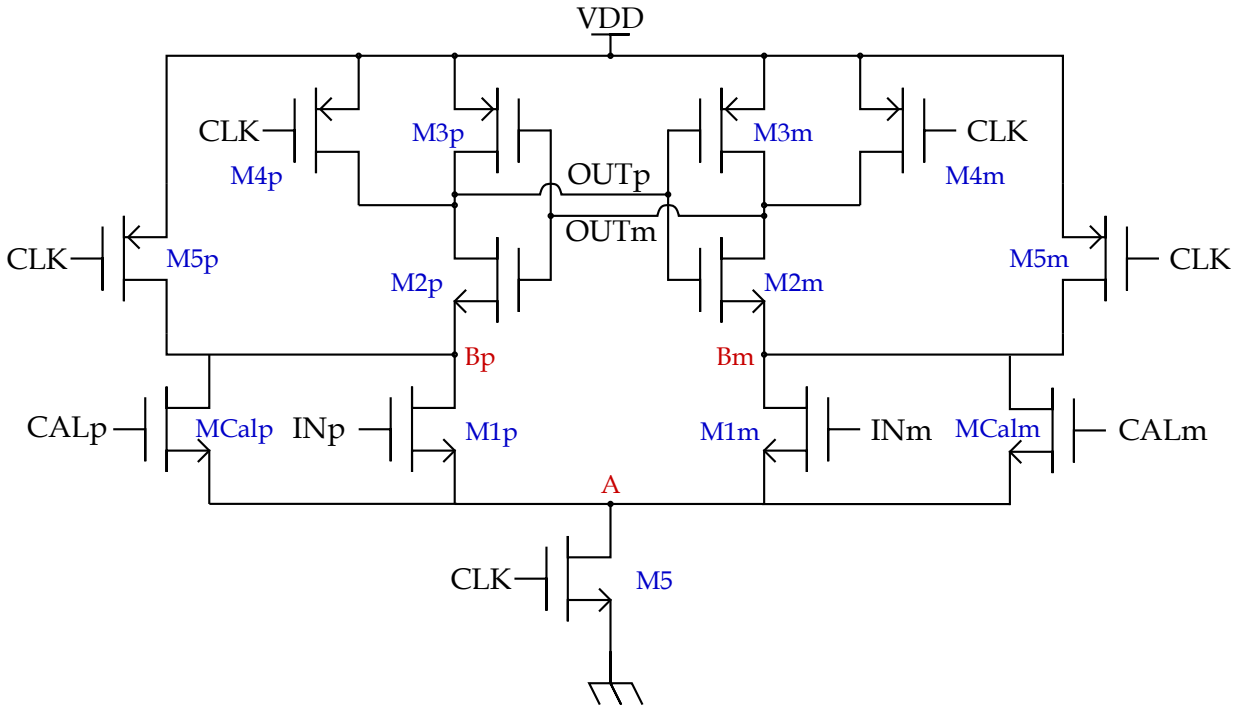


Figure 3.31: Schematic of the comparator

Transistors MCal are used for calibration and are ignored for now. When CLK is low, both nodes Bp, Bm, OUTp and OUTm are stuck to VDD because M5 and M4 are on. Consequently, the cross-coupled inverters formed by M2 and M3 are not in a stable position because their inputs and their outputs are both tied to VDD. After the next clock edge rise at the gate of M5, the input transistors M1 discharge the two cross-coupled inverters with a slew rate dependent on the applied input voltage. The cross-coupled inverters then regeneratively amplify any voltage difference at the input.

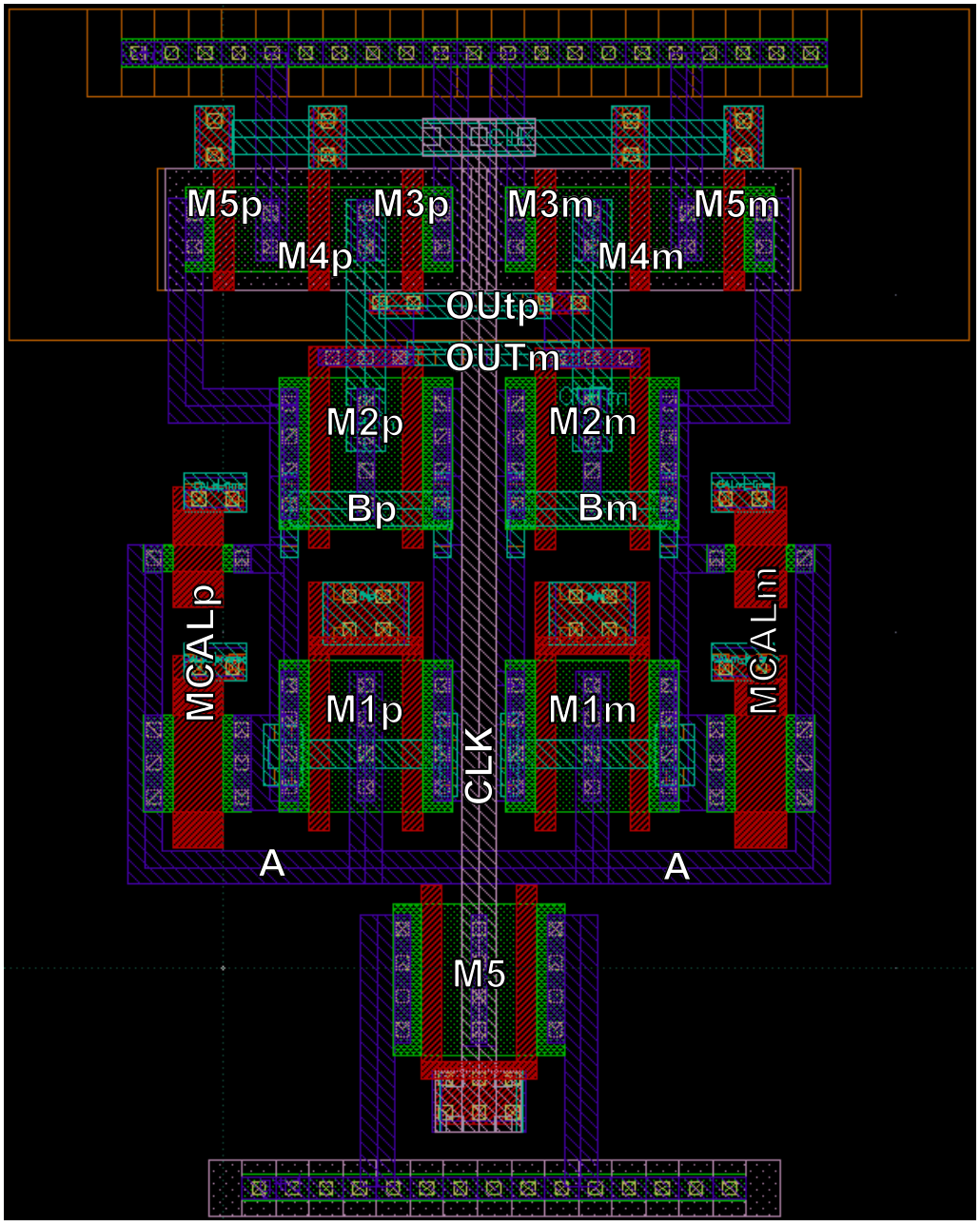


Figure 3.32: Layout of a comparator based on cross coupled inverters

The main drawback of this comparator is that the output value is directly function of the matching between P and M sides. Consequently, a very careful symmetric layout has to be done for both sides (Figure 3.32). In order to limit the mismatch, all the transistors are 60n instead of 28n and the length of interconnections between each transistor are exactly the same.

In oder to create the offset needed in the duty cycle corrector, MCALm and MCALp have been added. This calibration transistors unbalance the inverter pairs on one side. This can be considered as an offset during the comparison and is used to create the dead-zone introduced in the duty-cycle correction system introduced in Figure 3.26.

IV.B. Synchronization of the system

All the previous sections assume a complete time synchronization between the input signal and the sampling clock. As presented in Figure 3.18, synchronization is needed not only between the phase of the sampling clock and the radio frequency clock but also between the phase of the sampling clock and the symbol clock. This section describes how a poor synchronization affects the quality of the receiver. First, the symbol synchronization is studied. Then, RF synchronization is explained. Finally the cells used to reach the synchronization target are presented.

IV.B.1 Synchronization of the sampling clock to the symbol clock

When the symbol synchronization is not correct, the previous or following symbol leaks on the sampled one. Consequently the worst pattern to sample is a stream of 1 / -1 / 1 or -1 / 1 /-1 (while sampling the symbol in the middle). In this subsection, this worst pattern is considered for the symbol synchronization. The ideal synchronization is shown in 3.33(a). This is the sampling instant taken at the reference when all the clocks are synchronized.

As shown in 3.33(b), an offset of one (or minus one) full period do not affect the sampled value. So the result after the integration process is equivalent to the ideal sampling instant.

Figure 3.33(c) shows that for an offset of 3 periods, the sum of the positive samplers is not maximum because the fourth sampler includes a negative phase. In the same way, the sum of the negative samplers is not maximum because the fourth sampler includes a positive phase.

Consequently, the final sampled (positives minus negatives) value is half of the maximum value. This phenomena is identical for offsets of +/- 2, +/- 3 and +/- 4 periods.

Figure 3.33(d) shows that for an offset of 6 periods. The sum of the positive samplers returns zero and the sum of the negative samplers also returns zeros. This result in a null sampled voltage. This phenomena is identical for offsets of +/- 5, +/- 6 and +/- 7 periods.

In the prototype, the adaptive symbol synchronization has not been implemented and control needs to be performed externally. Meanwhile, a solution has been studied and is detailed in the last chapter dealing with the prospects.

IV.B.2 Synchronization of the sampling clock to the RF signal

A QPSK signal at f_{IF} frequency is defined in chapter II as follows:

$$V(t) = I \cdot \sin(2\pi f_{IF} t) + Q \cdot \cos(2\pi f_{IF} t) \tag{3.5}$$

where I and Q are respectively Inphase and Quadrature amplitudes and f_{IF} is the intermediate frequency. In this first subsection, it is assumed that the symbol (I & Q) is constant during the sampling operation. The charge domain sampling operation can then be modeled as shown in (3.6).

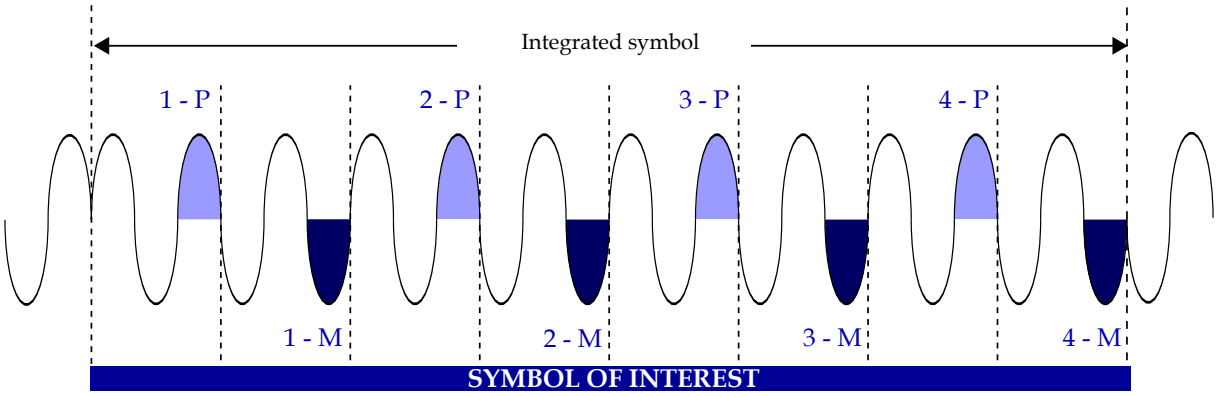
$$V_{1sample}(a) = \int_{a}^{a+T_i} V(t) \cdot dt \tag{3.6}$$

where $V(t)$ is the input signal defined in (3.5), T_i is the ideal integration window and a is the sampling instant. After integration (3.6) is equivalent to :

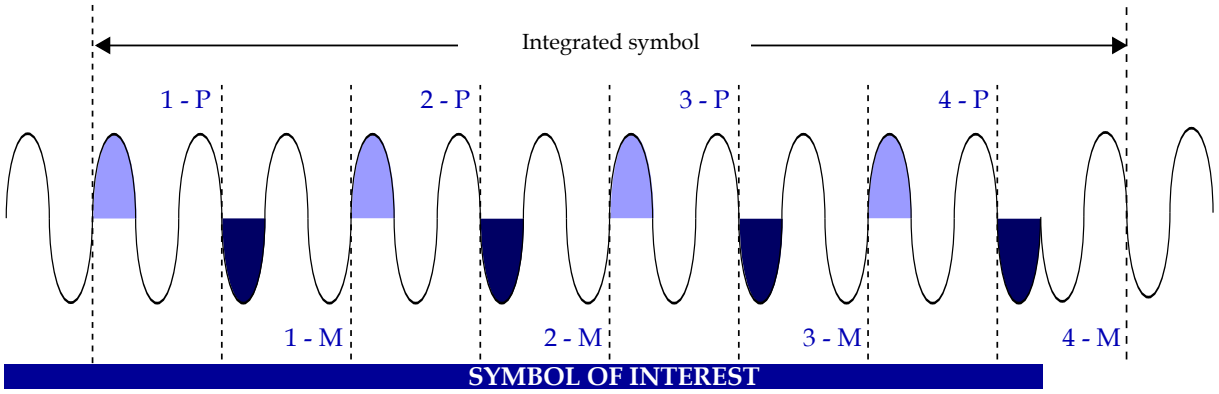
$$V_{1sample}(a) = -I \left[\frac{\cos(2\pi f_{IF} t)}{2\pi f_{IF}} \right]_{a}^{a+T_i} + Q \left[\frac{\sin(2\pi f_{IF} t)}{2\pi f_{IF}} \right]_{a}^{a+T_i} \tag{3.7}$$

This equation shows that the output value for one sampler is a combination of two contributions. The first one is function of I, the second one is function of Q. With an ideal sampling instant for I or Q, one contribution is equal to zero. While sampling Q for instance, the ideal sampling instant is defined in (3.8). This represents the expected 90 degrees phase shift at f_{IF}.

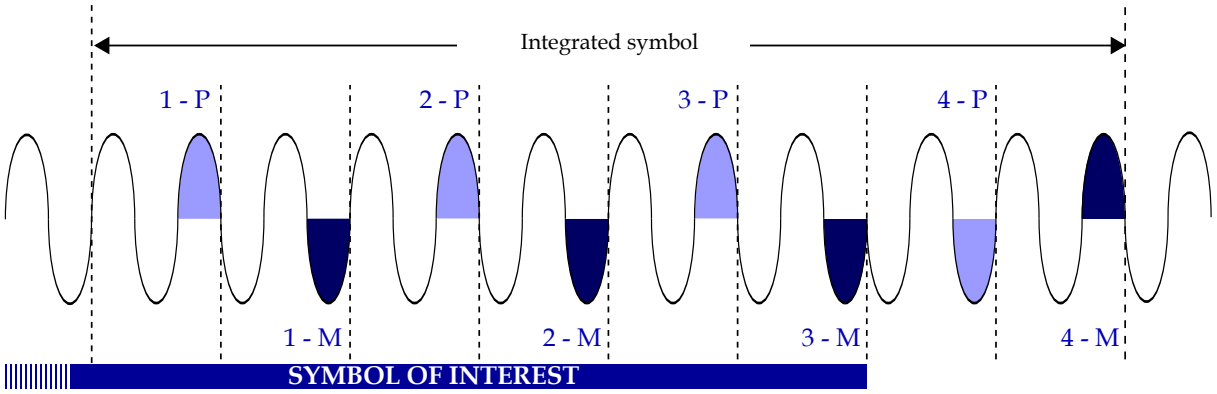
$$a_{ideal} = \frac{1}{4 \cdot f_{IF}} = 11.8ps \tag{3.8}$$



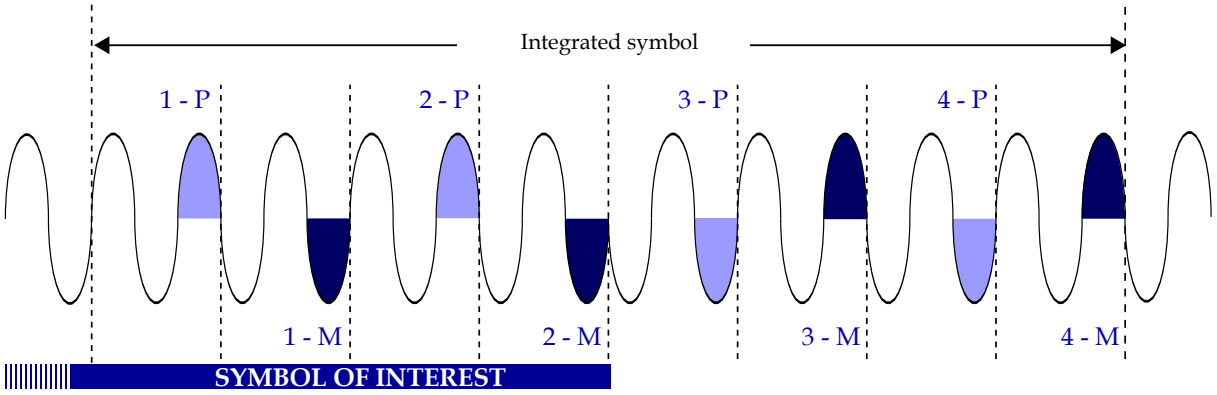
(a) Ideal sampling instant



(b) Ideal sampling instant with one period offset at f_{RF}



(c) Ideal sampling instant with 3 periods offset at f_{RF}



(d) Ideal sampling instant with 6 periods offset at f_{RF}

Figure 3.33: Sampled value for several sampling instant deviation

When the sampling instant differs from the ideal value, coupling appears between I and Q. This coupling noise is given in equation 3.9 by the ratio of the two parts of $V_{1sample}$. Δ is the deviation from the ideal value.

$$IQ_{coupling} = \left[\frac{\cos(2\pi f_{IF}t)}{\sin(2\pi f_{IF}t)}\right]_{a_{ideal}+\Delta}^{a_{ideal}+\Delta+T_i} \tag{3.9}$$

Considering a maximal error of 10%, the previous equation indicates that the synchronization target is less than 1ps around the ideal sampling instant defined in (3.8).

In the 28nm CMOS technology, the minimum delay of a basic inverter is around 6ps. So the required resolution can not be reached by adding or removing inverters.

A resolution lower than 6ps can be reached by modifying the slew rate of inverters as was previously explained for the duty cycle adjusters. A solution based on the SRC inverters introduced in Figure 3.27 can be used but the N and P controls are symmetrical in order to delay both edges.The resulting unit delay cell is shown in Figure 3.34.

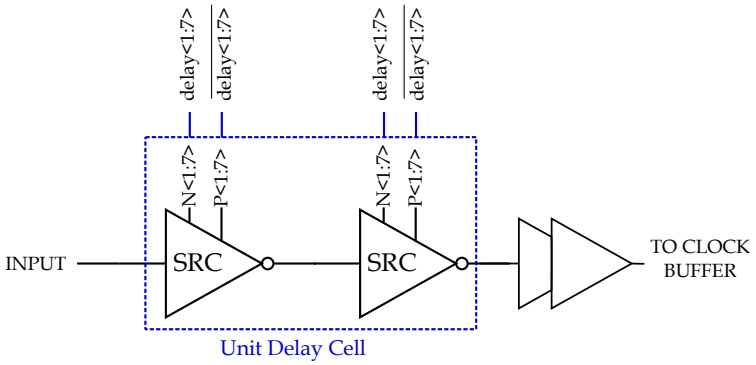


Figure 3.34: Single delay cell based on slew rate controlled inverters

This cell is controlled by a 7-bit thermometric code. Each step in the control code results in a additional delay of 780 fs. Figure 3.35 shows the resulting delay of the unit delay cell through all the process variations.

For the FF configuration, both N and P transistors are fast, consequently, the global delay is reduced comparing to the typical configuration, the average delay for one step is 650fs. For SS configuration, both transistors are slow so the average delay for one step is 930fs.

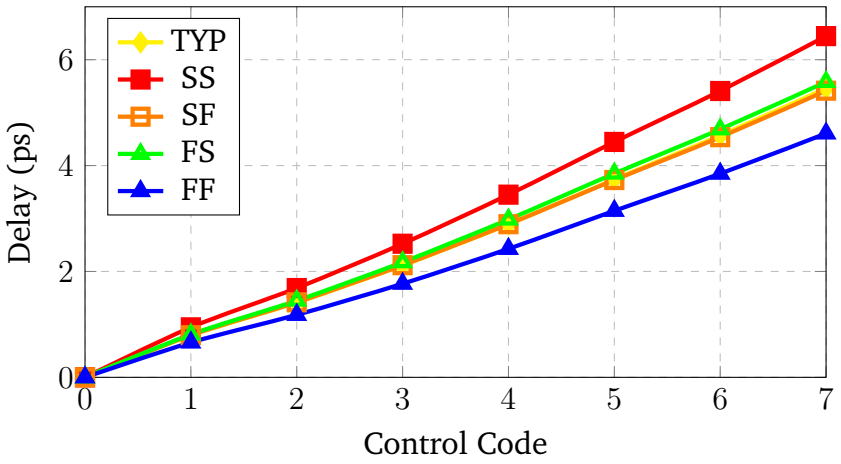


Figure 3.35: Delay vs Control Code for the unit delay cell

IV.C. Resulting clock tree

IV.C.1 Overview of the resulting clock tree

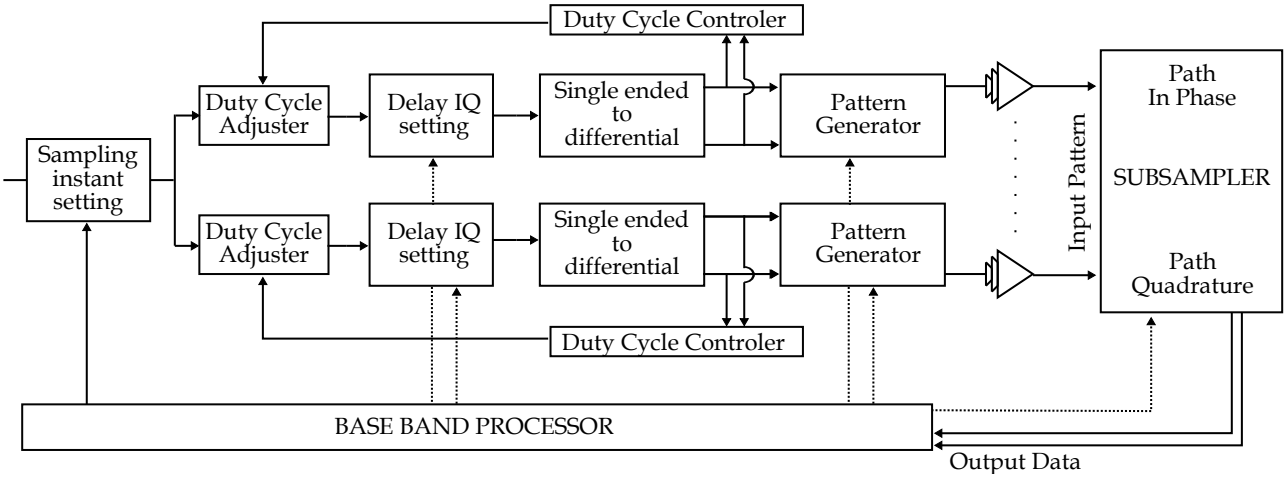


Figure 3.36: Overview of the clock tree

Figure 3.36 represents a detailed block diagram of the clock generator for the proposed sub-sampler.

The clock generator is divided into in-phase and quadrature-phase paths to tune the parameters independently. The first block is common to both paths. It is used for setting the global phase of the whole clock generator in order to sample the signal at the correct instant (section IV.B.1).

If the input clock duty cycle is not equal to 50%, coupling will remain between I and Q. Consequently, a feedback loop allows the duty cycle adjustment (section IV.A.). The adjustment is performed according to the duty-cycle controller that monitors the clock quality on

the leafs of the clock tree in order to take into account the impact of all stages of the clock distribution.

The delay between I and Q is fine-tuned based on the error rate detected by the baseband processor (section IV.B.2).

Finally, coupled inverters perform the single-ended to differential conversion and feed the pattern generator. The latter creates the correct pulses for the sub-sampler.

IV.C.2 Performance summary

Table 3.3 sums-up the tunability of the clock tree in the typical corner case and table 3.4 details the power consumption breakdown of the whole chip while operating at a 7.04 GHz clock.

Parameter	Tunning Range	Setting Step
Sampling Instant Setting	0 to 24 ps	0.7 ps
IQ delay setting	0 to 19 ps	0.7 ps
Duty cycle adjustment	+/- 8 % at 7 GHz	0.5 %

Table 3.3: Tunable parameters of the clock tree

Part	Power Consumption (mW)
Transconductances	2 x 2
Pattern Generator	2 x 2.5
Clock Distribution	40

Table 3.4: Power Consumption under 1 V

V. Simulations and silicon implementation

V.A. Transistor-level simulations

The transfer function of the system is obtained by sweeping a single tone sine wave at the input from 21.12 GHz to 29.12 GHz in 80 steps.

The corresponding output values are shown in Figure 3.37 and compared to the theoretical transfer function. The simulation results and the theoretical values show the same behavior for the global shape and for the notches position. The discrepancies between the simulated and the theoretical values are due to effects that have not been considered in the theoretical analysis such as capacitive coupling between signal lines, switch on-resistance and the charge injection of the switches.

The phase response of the channel bandwidth is shown in Figure 3.38. The simulated phase response is close to the value predicted by theory.

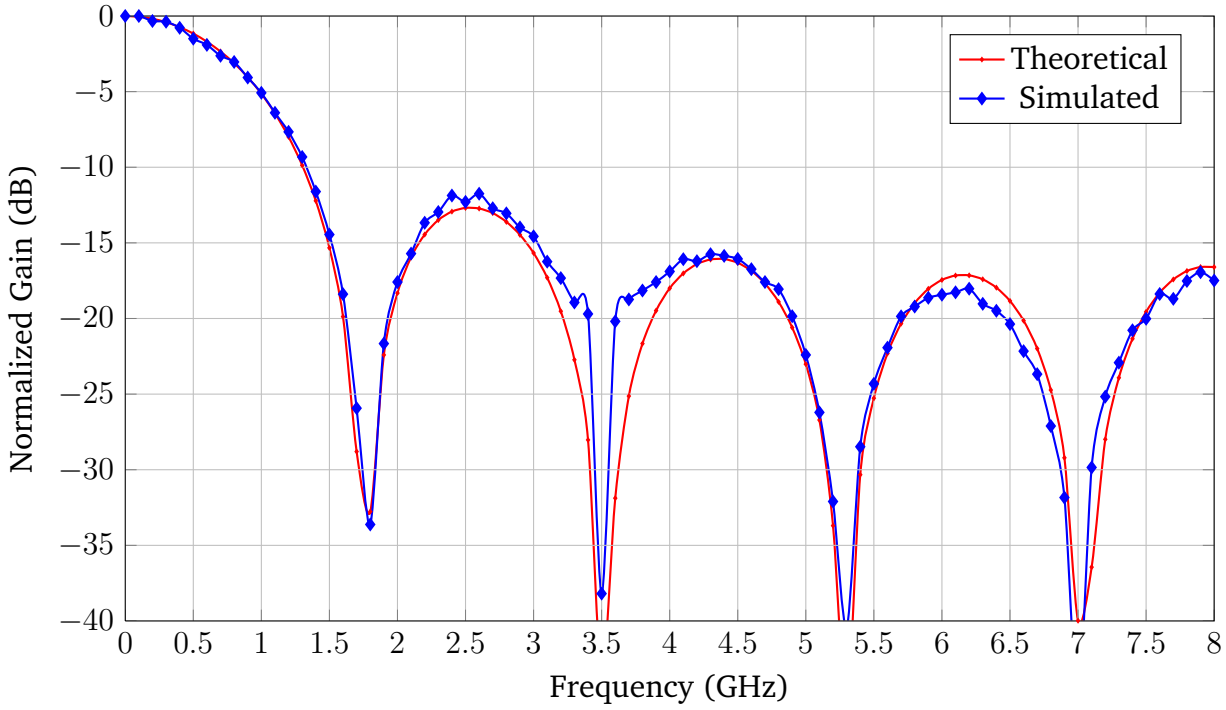


Figure 3.37: Theoretical and simulated transfer function of the proposed architecture at transistor level

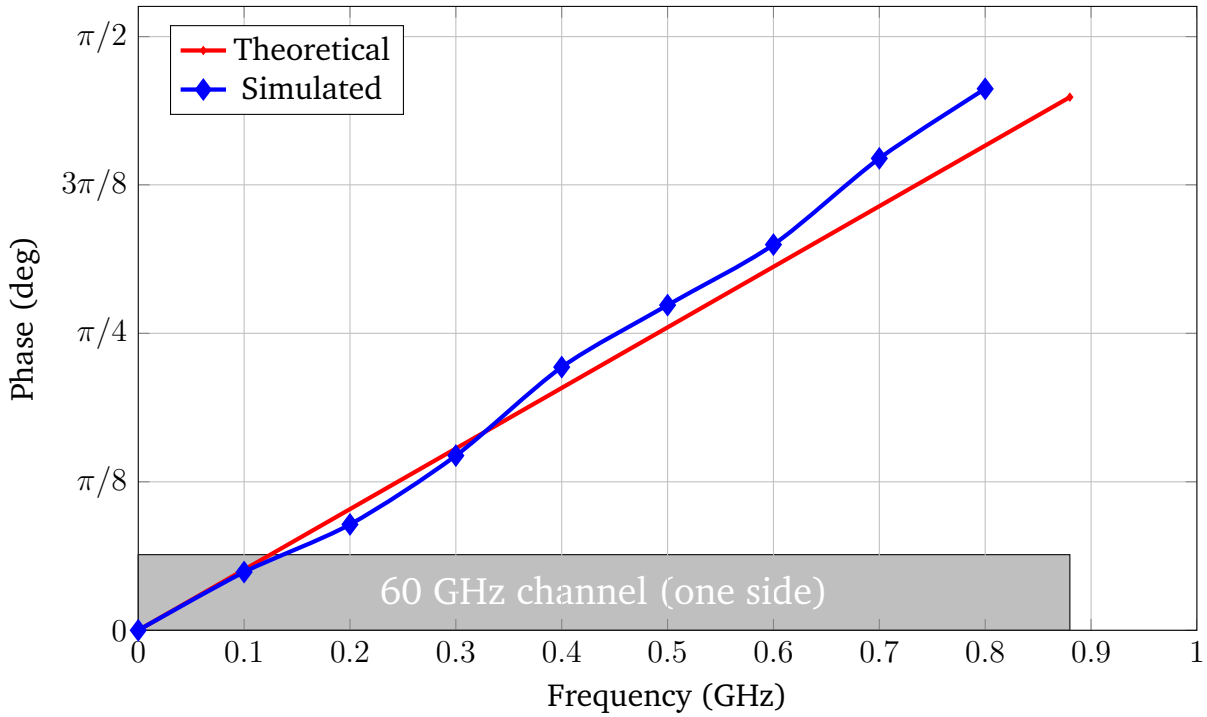


Figure 3.38: Theoretical and simulated in-band phase response of the proposed architecture at transistor level

V.B. Silicon implementation

A 0.9 x 1.4 mm^2 test chip has been designed and fabricated in STMicroelectronics 28nm CMOS process.

The implementation is detailed in Figure 3.41. The chip is fed by the clock at the bottom of the Figure. In the first part, the clock goes through several slew rate controlled inverters used as duty cycle adjusters or delay cells (35x4 μm^2). Then the clock buffers (24x15 μm^2) feed the pattern generator which is composed of static logic and flip flops (40x10 μm^2). This pattern generator is connected to the switches inside the analog core (25x150 μm^2). Finally three output comparators extracts the output value (25x30 μm^2). At the left bottom side, comparators and shift registers are dedicated to duty cycle regulation (40x30 μm^2).

This forms a complete core for I or Q (0.00585 mm^2). Two of this core are integrated in the complete chip. All the area not used for active devices is used for decoupling CMOS capacitors.

By adding an area dedicated to memories for the control of the chip, the total active area is 0.0162 mm^2. Consequently, the implemented test-chip is pad-limited. Figure 3.39 shows the complete test chip and its pad-ring. The south side is used for the RF input signal and the sampling clock. West and east sides are used as outputs for I and Q (data and calibration as shown in Figure 3.20). The north side several 8 pads are used. Three of them supply the chip : ground, core supply and output buffer supply. Three pads are used to program the chip : Memory clock, Memory data, Write mode. One pad is dedicated to set the chip in initialization mode, it can bypass all the values loaded in the memories and using a hardware-defined value. The last pad is used to check the configuration inside the chip.

The chip has been taped out in june 2012 and received in march 2013. A photograph of the die is shown in Figure 3.40.

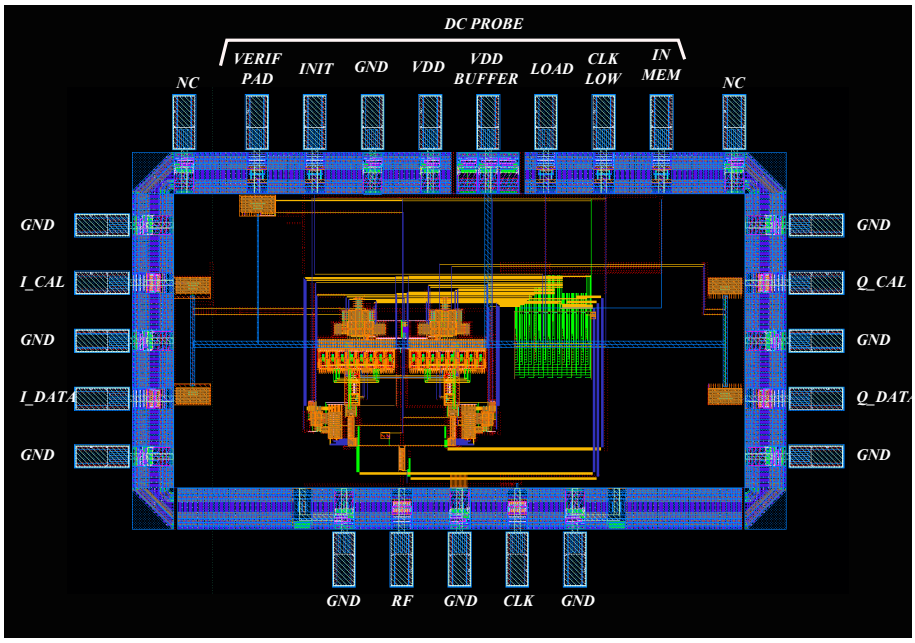


Figure 3.39: Global Layout

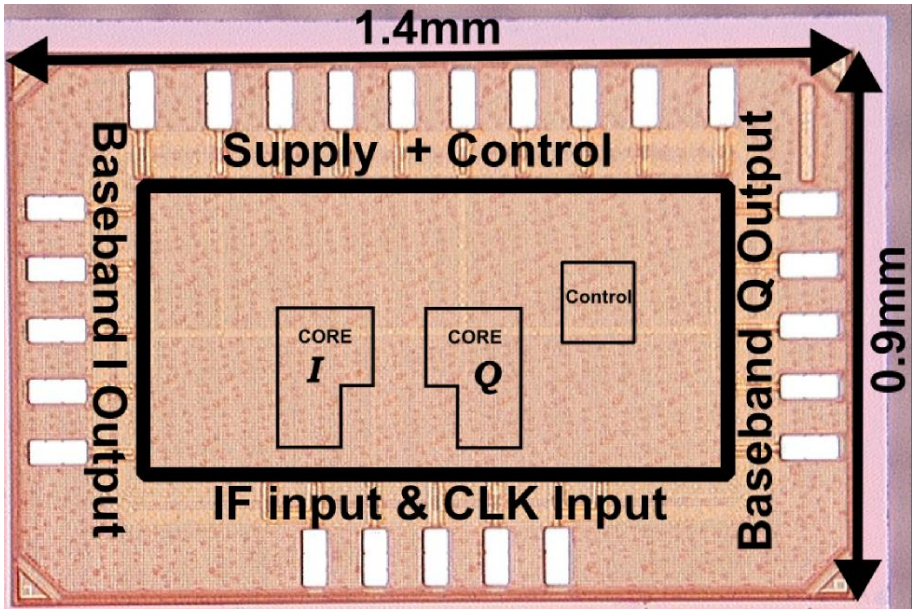


Figure 3.40: Die Micrograph

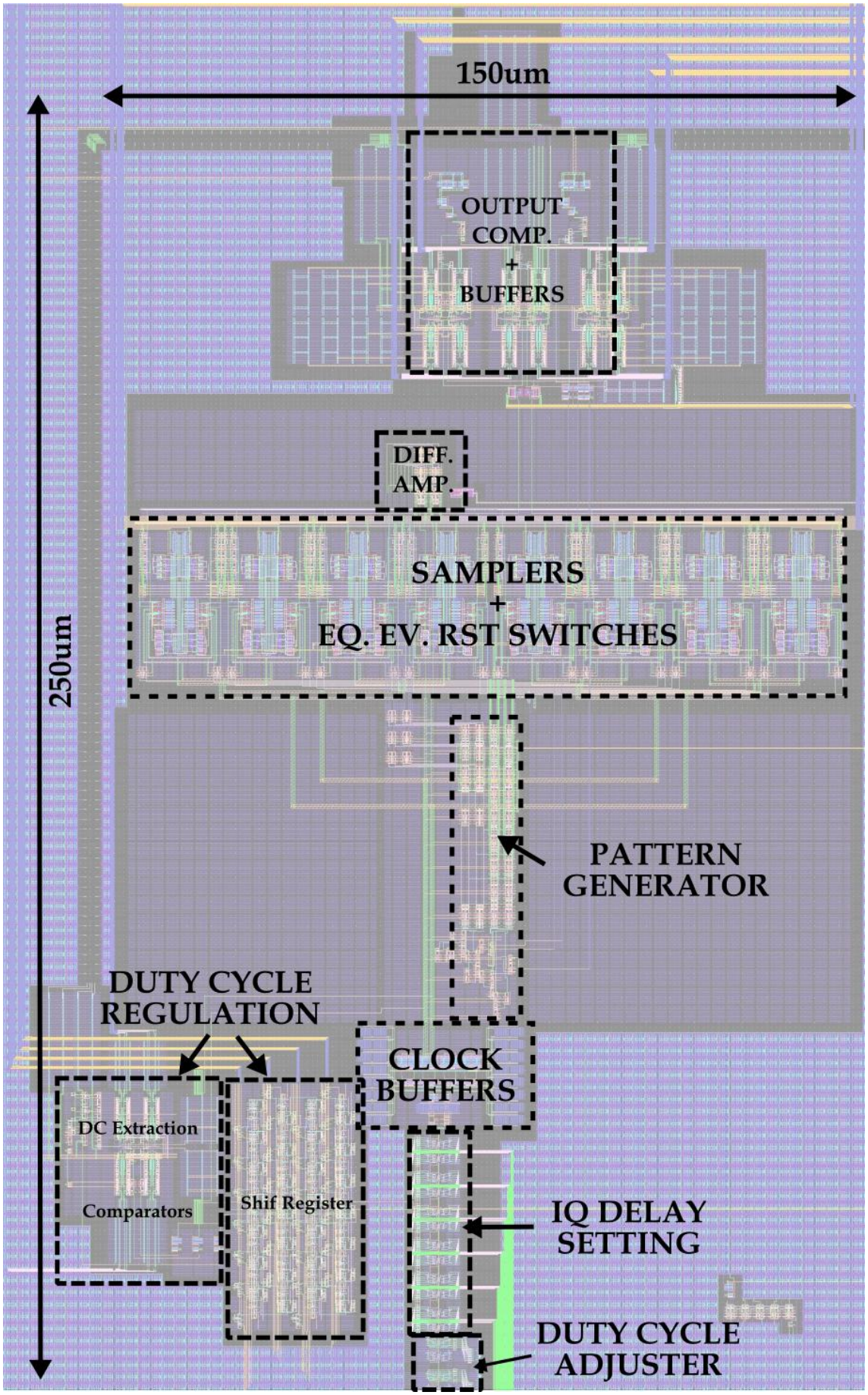


Figure 3.41: Layout of one core

VI. Conclusion

This chapter has detailed the implementation of the quadrature charge domain sub-sampler in 28nm CMOS.

It has been demonstrated in the first part that a traditional sampler is not suitable for the target application. Consequently, a solution that includes the switches directly inside the sampler in order to reach high frequencies has been proposed.

The second part has dealt with continuous time operation, using four paths working in parallel. The layout of these four samplers have been optimized in order to limit the effects of parasitic elements and to minimize the mismatches between the different paths.

The third part has detailed how to generate the correct pattern to feed the subsampler. To properly receive a symbol, the quality of the input clock has to be monitored to stay around 50% because a deviation of the duty cycle results in strong IQ interferences. This regulation and the corresponding building blocks have been detailed. Finally, the synchronization between the sampler clock and the input signal has been studied.

The fourth part has shown that the transistor level simulations are close to the theoretical values presented in the previous chapter and has given the final layout of the implemented prototype.

CHAPTER

4

MEASUREMENTS

I. Introduction

I.A. Test methodology

The chip under test is shown in Figure 4.1 It is composed of two transconductance cells. Their inputs are connected to the "RF_{IN}" pad. Their outputs feed two samplers : one for the Inphase data and one for the quadrature data. The reference clock is connected to the "CLK" pad. Integration windows are produced by the pattern generator to feed the samplers. The output digital bit-streams are connected to the "I Data" and "Q Data". The two outputs "I Ref" and "Q Ref" will be ignored for now and intended to be used in the automated calibration procedure detailed in Annex A. The sampling instant can be configured by programming the memory block.

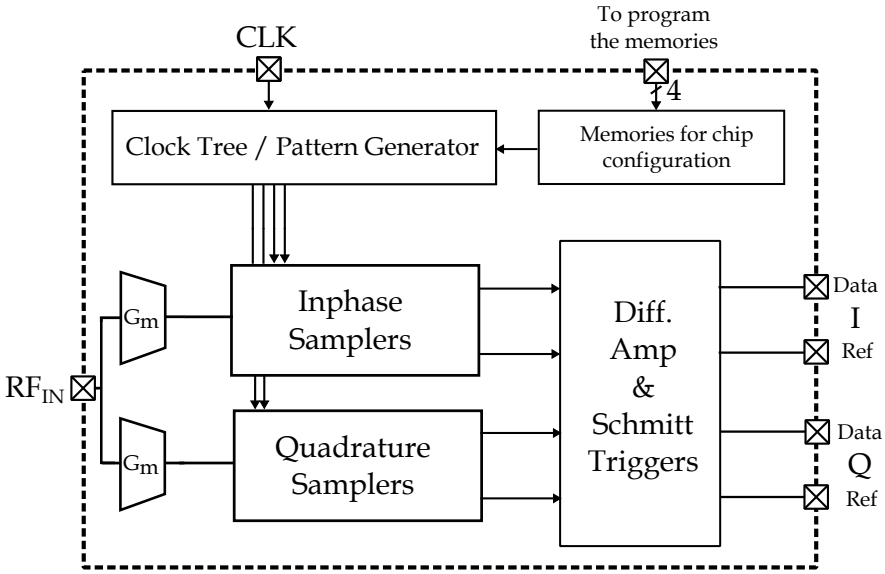


Figure 4.1: Chip under test with input and output connections

The chip has been designed to validate the principle of a direct-receiver based on charge domain subsampling. However, the decoding of the received input signal is included in the circuit, i.e. the sampler outputs are directly fed to comparators to extract the received data. As the output signal is a 1-bit digital stream instead of an analog baseband signal, classical measurements such as SNR or linearity can not be done. Consequently, the measurements of the chip exploit the information given by this digital bit-stream : frequency of the stream or coherence of the bit stream decoded by the chip with the RF input data.

The measurements have been divided in three distinct parts in order to validate each function of the system separately. The tested functions of the receiver are the following and will be detailed in this chapter.

- Downconversion

Check if the system is able to downconvert the input signal from the radio frequency to DC.

- Demodulation

Check if the system is able to demodulate an input signal (coded BPSK or QPSK).

- Channel rejection

Check the sensitivity of the system to input blockers.

I.B. Chip connections

Figure 4.2 describes the 28 nm integrated circuit, together with the dedicated measurement setup. It consists of RF and DC probes connected to laboratory instruments. For the RF and clock inputs, I and Q outputs, 3 RF differential probes provide 2 independent signals surrounded by ground connections. For the fourth side, a 8-pin DC probe has been selected to connect the four pins of the memories, ground, supplies and a control pin for basic checks of the chip.

A probe station is used to provide connections on the four sides of the chip, as shown in Figure 4.3.

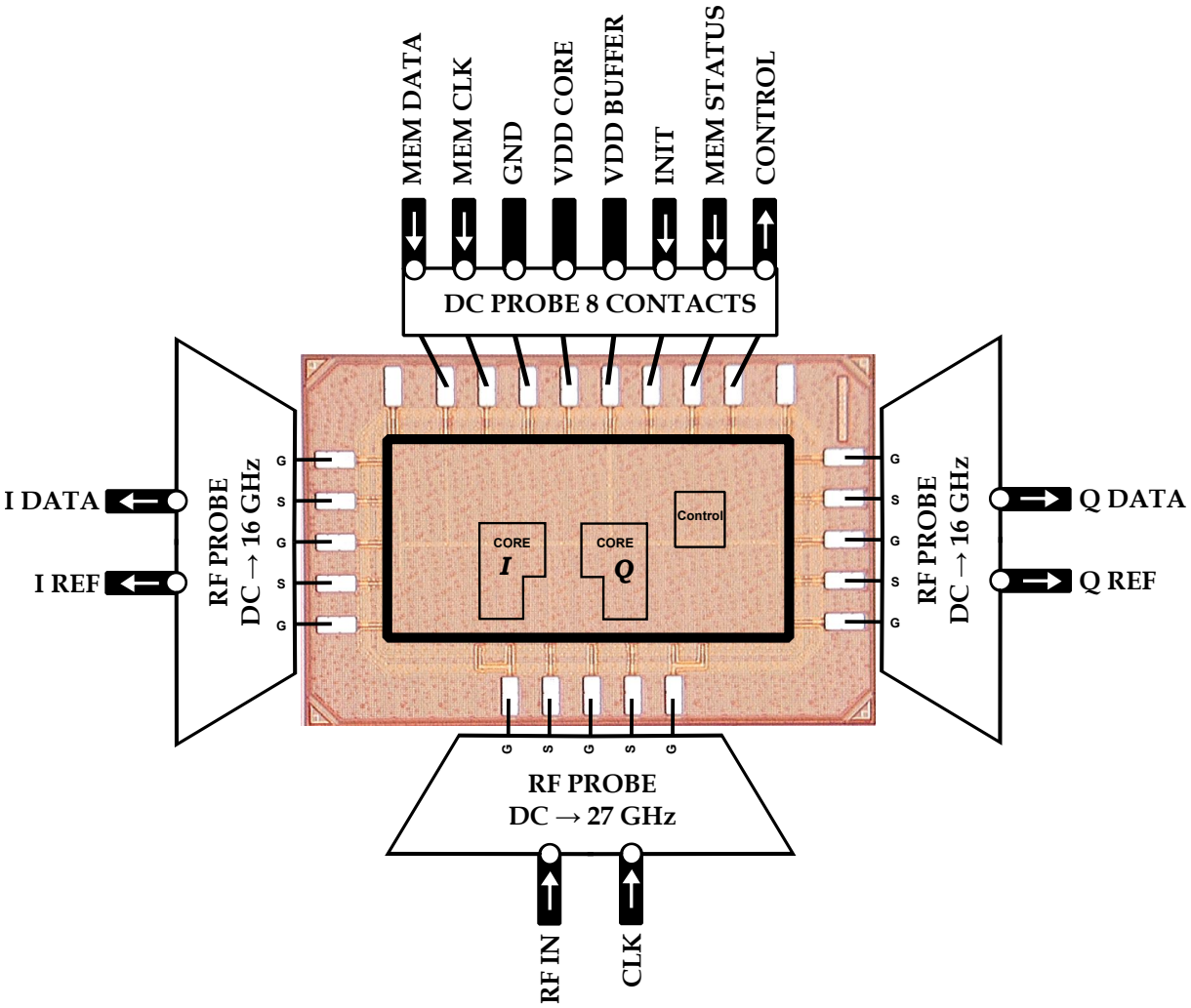


Figure 4.2: Schematic of the probes connections

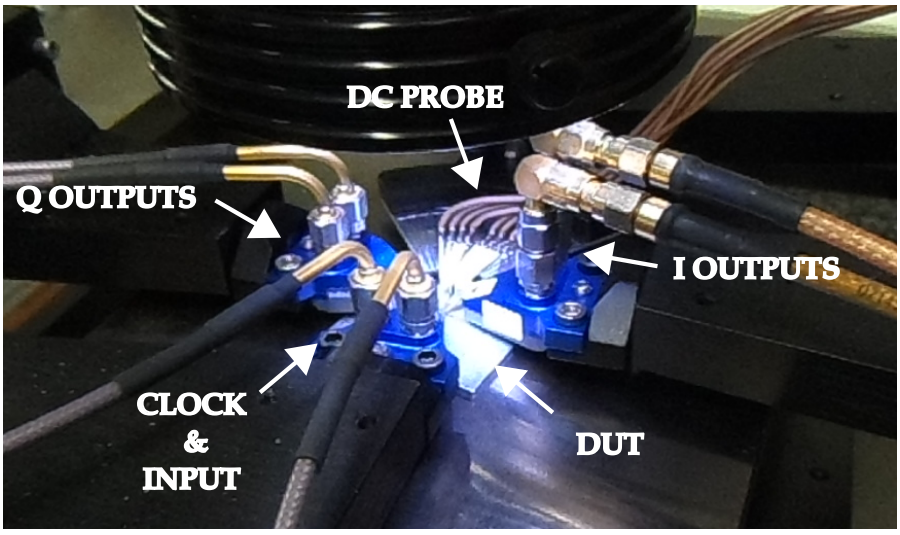


Figure 4.3: Probes connections on the bench

II. Downconversion

II.A. Test setup

The test setup used for the downconversion test is shown in Figure 4.4. Both clock and RF pads are fed by a sine wave source. The two sine wave sources are synchronized by a 10MHz reference. The output is observed on a spectrum analyzer.

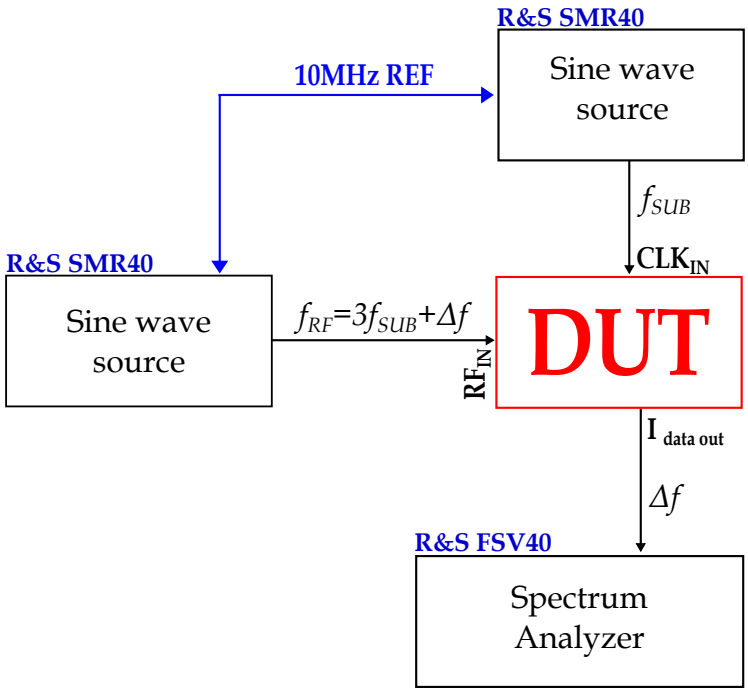


Figure 4.4: Test setup for downconversion test

In this configuration, the target is to check that the downconversion operation is correctly performed. In order to do so, while the chip operates at f_{SUB} and the RF input receives a sine wave at $3 \cdot f_{SUB} + \Delta f$ where Δf is the baseband sinewave frequency. As the output signal is a 1-bit digital stream, the expected output is a square wave at Δf. Figure 4.5 shows an example where the chip is functional : a square wave is observed on the spectrum analyzer at 35 MHz while the chip is working at 3 GHz and is fed by a RF frequency at 9.035 GHz .

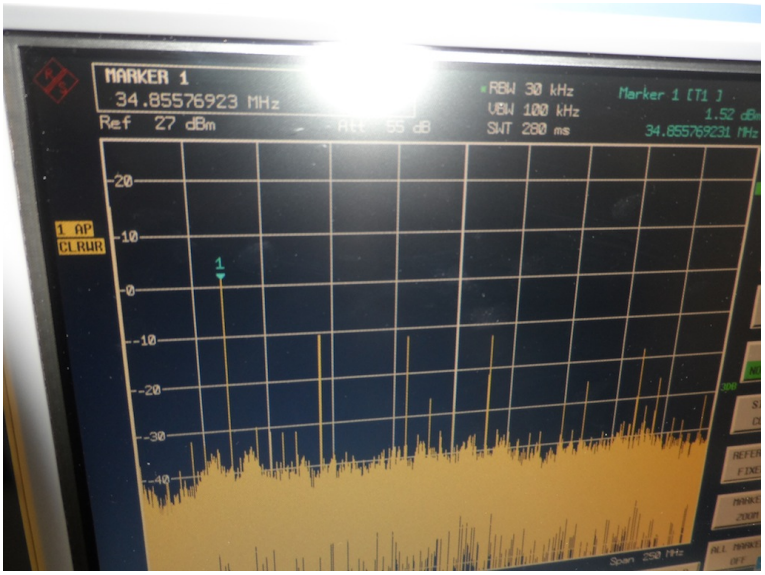


Figure 4.5: Resulting square wave at $\Delta f = 35MHz$ while the chip working at $f_{SUB} = 3GHz$ receives a sine wave at $f_{RF} = 9.035GHz$

II.B. Results

Figure 4.6 shows the power consumption and the maximum operating frequency for several supply voltages. With the nominal VDD (1V) the maximum operating frequency is 5 GHz. The targeted operating frequency of 7.04 GHz can be reached for a supply voltage of 1.2V. While working at 3 GHz, the system is able to receive the RF signal up to 9 GHz with a power consumption of only 15 mW.

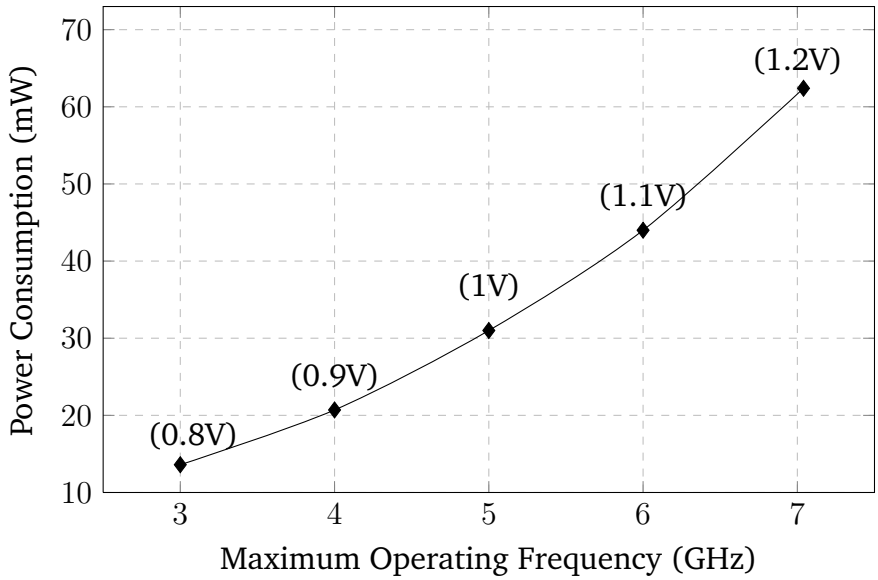


Figure 4.6: Power consumption versus maximum operating frequency for several supply voltages

III. Demodulation of BPSK and QPSK signals

III.A. Test setup

The test setup used for demodulation of BPSK and QPSK signals is shown in Figure 4.7. One data stream at $f_{data} = 1.76GHz$ is generated by a BER Tester (Agilent J-BERT N4903A). For QPSK signals, a second data stream is generated by an Arbitrary Waveform Generator (Agilent AWG7102). These streams are modulated around $f_{IF} = 21.12GHz$ by the RF modulator (LTEQ HMC710LC5). This modulated data feed the RF pad of the chip. The CLK pad is fed by a sine wave source at $f_{SUB} = 7.04GHz$. Due to timing constraints in the principle of operation of the system, all the sources are synchronized with a 10 MHz reference.

The demodulated data coming out of the chip is received back to the BERT. It compares the incoming and the outcoming data streams for the selected channel (I or Q) and it evaluates how many bits are wrong in the sequence.

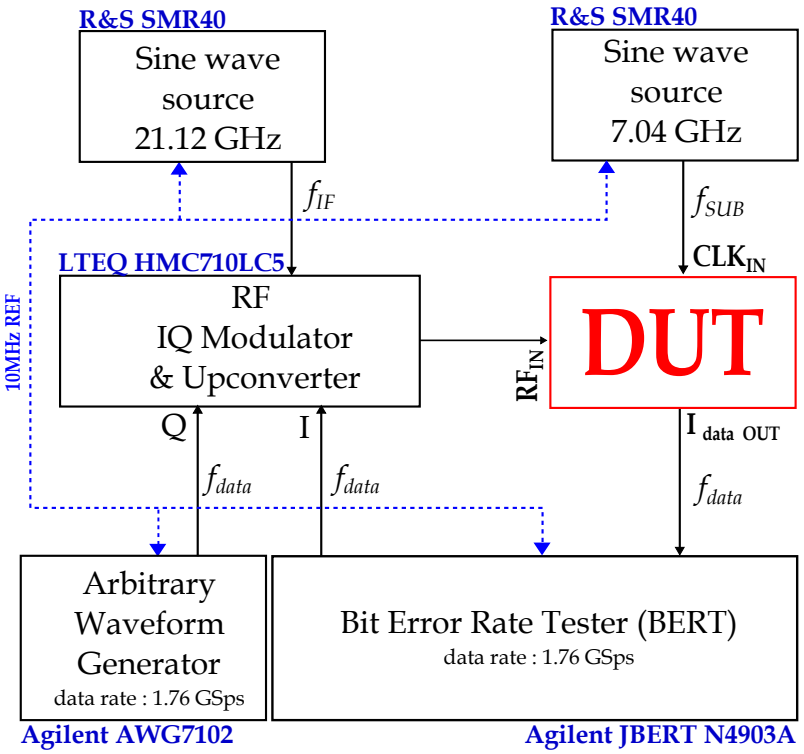


Figure 4.7: Test setup for demodulation test

III.B. Results

III.B.1 BER versus input power

In this first part, a perfect phase and frequency synchronization is assumed between the input signal and the chip. Synchronization issues and their impact on the received signal quality will be detailed in the following section.

Figure 4.8 shows the BER of the system versus input power. In the BPSK test case, the BER is below 10^{-3} for input powers between -12 and +5 dBm. In the QPSK test case, the BER is below 10^{-3} for input powers between -10 and +5 dBm. The minimum BER in the QPSK case is limited to 10^{-4} by IQ leakage during the sampling operation due to jitter-induced mismatch.

Considering a complete system, the front end [2] gives a gain of 24 dB. Consequently, the 10^{-3} raw sensitivity would be respectively -36dBm and -34dBm for BPSK and QPSK.

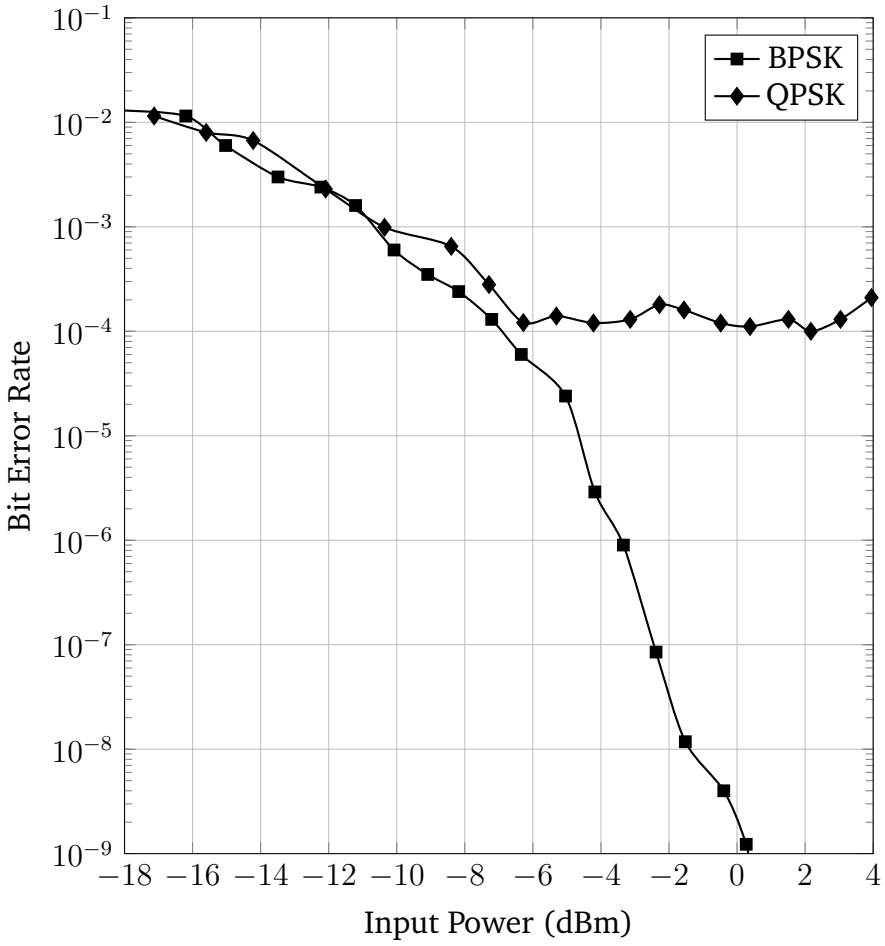


Figure 4.8: Sensitivity with BPSK and QPSK modulations

III.B.2 Sampling instant control

As described in the previous sections, the sampler should be synchronized with the RF input frequency. In order to do so, digitally controlled delay cells set the sampling instant. An algorithm working on based band data stream to automatically find the best synchronization instant has been developed and is explained in annex A.

Figure 4.9 shows how this sampling instant affects the sensitivity of the receiver. For this measurement, the input power is set to -12 dBm for BPSK and -10 dBm for QPSK. As expected, the sampling instant is more sensitive for the QPSK test case because of the I/Q leakage introduced when the sampling instant deviates from the ideal value.

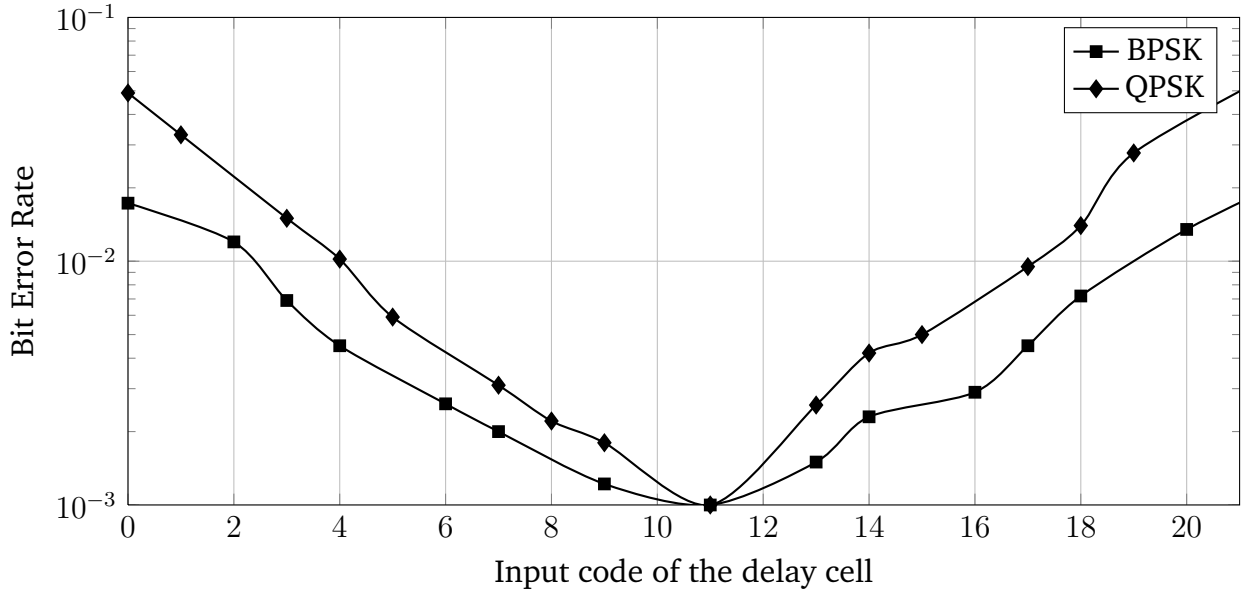


Figure 4.9: BER as a function of the sampling instant for a fixed input power (-12dBm in BPSK and -10dBm in QPSK)

IV. Immunity to blockers

As developed in Chapter 2, the sampler includes frequency domain selectivity intended to attenuate signal from adjacent channels of the standard. Due to the fact that the signal is digitized at the sampler outputs, it is not possible to measure the transfer function directly. Also, measuring the desitization of the receiver by measuring the gain compression is not possible either.

IV.A. Test setup

This test setup considers a BPSK input. To be close to a real case, the blocker should be a channel as defined in the standard. Meanwhile, due to limitations in the bandwidth of the signal generators, the generated blockers can only be sine waves. This sine wave is added using a power combiner on the input as shown in Figure 4.10.

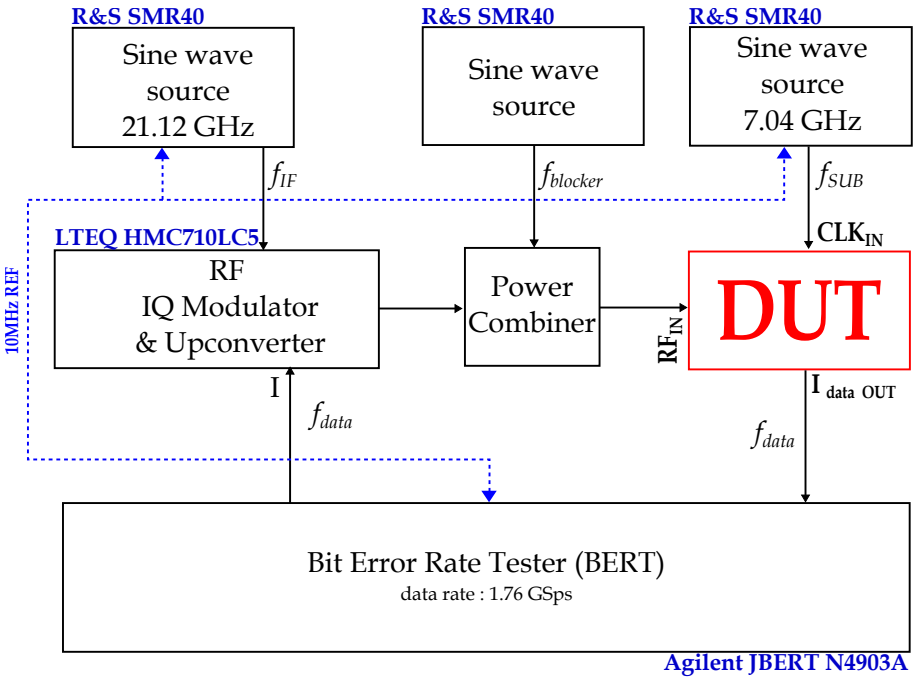


Figure 4.10: Test setup for immunity to blockers test

In this test setup, the level for the channel of interest is taken as the minimum defined 10^{-3} sensitivity (i.e. -12 dBm in BPSK). The blocker emulates a perturbation at the input as shown in Figure 4.11. To quantify the degradation, the power of this blocker ($P_{blocker}$) is increased until the BER degrades to 10^{-2}. This limit has been chosen because over this level, the synchronization becomes difficult to find.

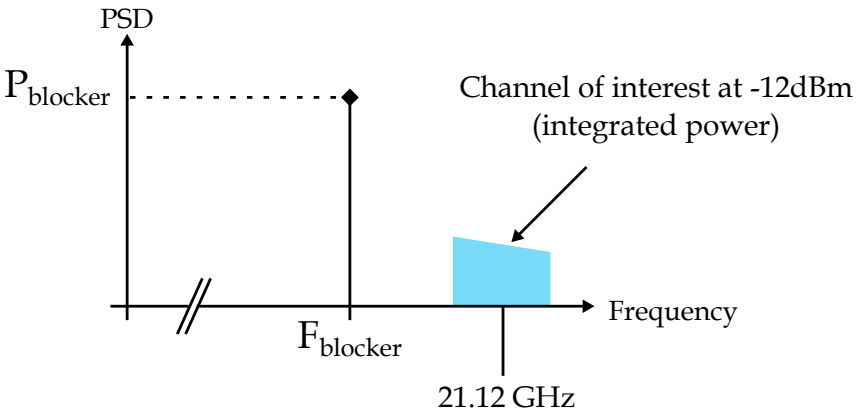


Figure 4.11: Channel of interest with a blocker

IV.B. Measurements results

Figure 4.12 shows the maximum allowable power of a blocker for a 10^{-2} BER while $P_{in-signal} = -12dBm$. As expected, while the blocker is around 21 GHz (inside the channel bandwidth), the power of the blocker needs to be almost 10dB under the signal of interest to limit its influence on the BER.

While decreasing this blocker frequency, for the same BER degradation, its power can be increased up to -13 dBm at 16.5 GHz. This shows an immunity of the system to out-of-band blockers.

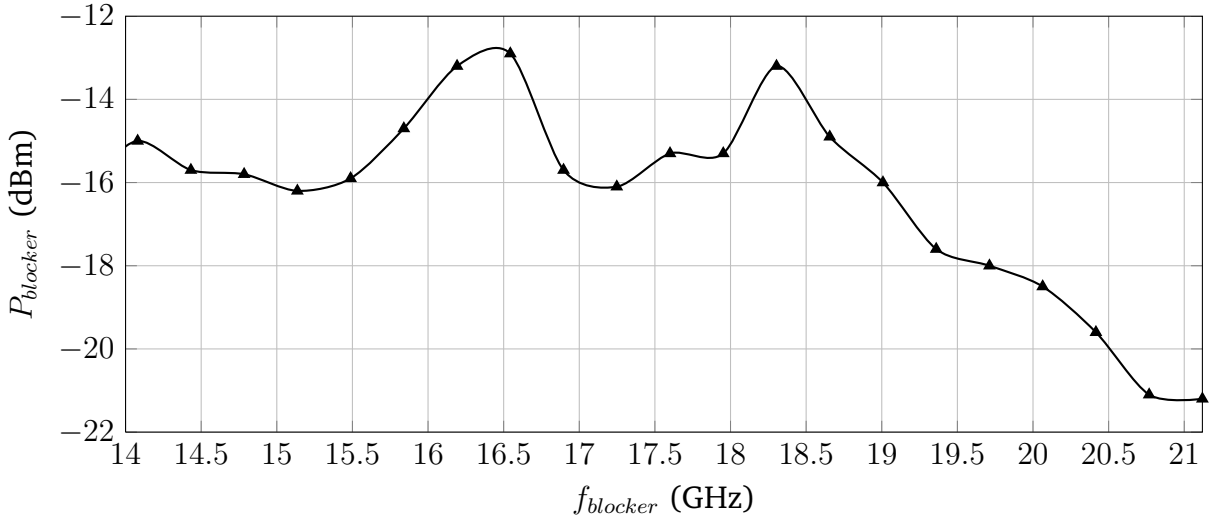


Figure 4.12: Maximum allowable power of a blocker for a 10^{-2} BER while $P_{in-signal} = -12dBm$

IV.C. Discrepancies between theoretical and results

As shown in Figure 4.12, when the blocker is at f_{IF}, its power must be at -21 dBm to decrease the BER from 10^{-3} to 10^{-2}. When the blocker is at 19 GHz, its power could be -16 dBm to have the same effect on the BER. Consequently, an attenuation of 5 dB exists between the reference frequency (f_{IF}) and 19 GHz.

Figure 4.13 shows the out-band attenuation obtained from the previous measurements, normalized and compared to the theoretical results. The ideal transfer function considers linear components. The comparison shows that even if attenuation exists, the attenuation is lower than expected.

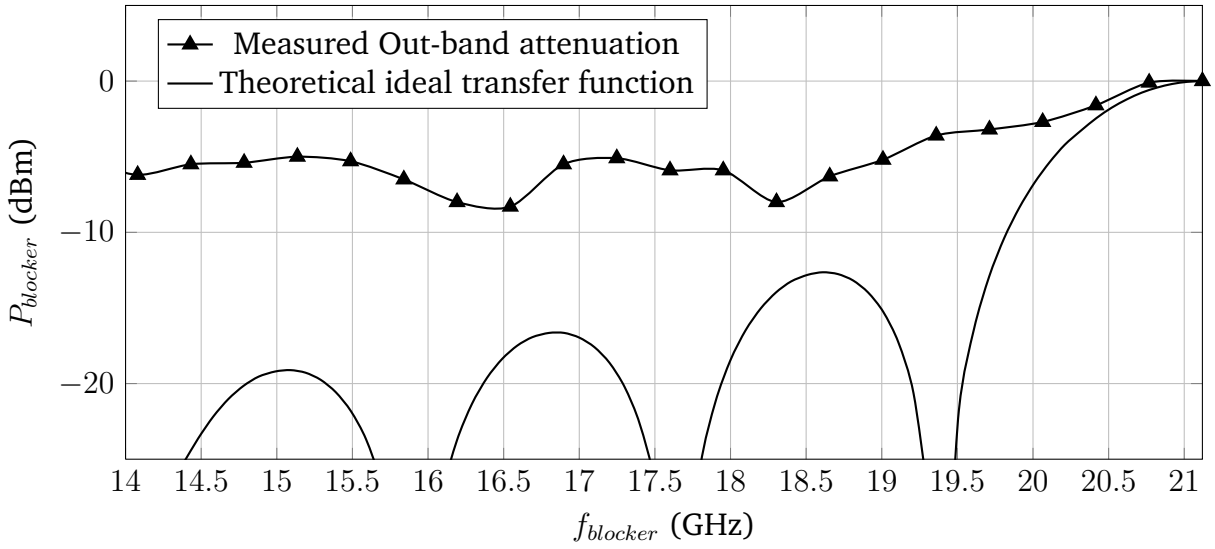


Figure 4.13: Measured attenuation of the blockers versus transfer function

To explain the discrepancies between measured and ideal results, a new simulation has been done in which the RF input of the chip receives the channel of interest at at a defined power $P_{channel}$ at a defined frequency $f_{channel} = 21.12GHz$ combined with a blocker at a defined $P_{blocker}$ at a defined frequency $f_{blocker}$. From a theoretical point of view, the attenuation of this blocker should follow the ideal transfer function of Figure 4.13.

Figure 4.14 shows the simulated attenuation of blockers versus the blocker frequency for several input powers. For frequencies close to 21.12 GHz the attenuation of the blockers fits with the theoretical value in any input power.

Around the notch created by the sampler at 14.08 GHz, the attenuation of the blocker depends on the input power. For a low input power (red, square) the simulated attenuation is close to the theoretical transfer function while for high input power (pentagons, green),

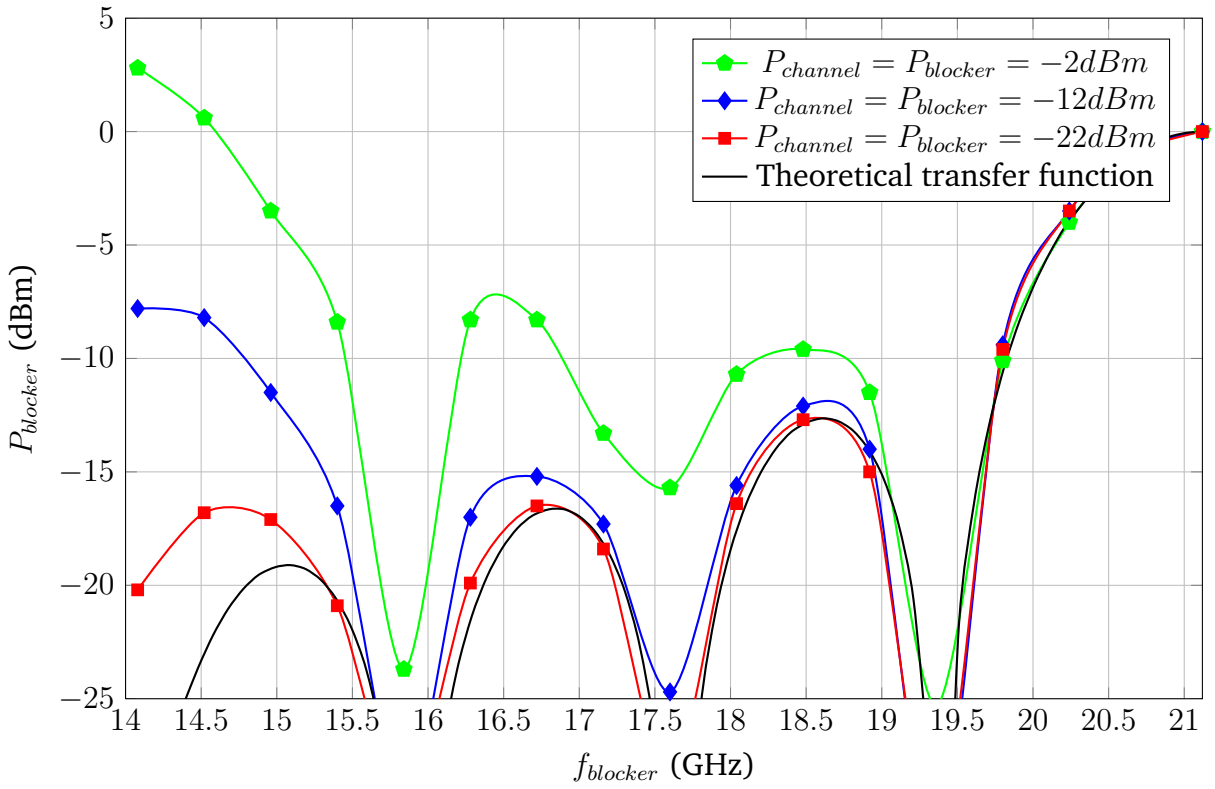


Figure 4.14: Measured attenuation of the blockers versus transfer function

the blocker is not attenuated anymore, it is even amplified.

This reflects the effect of the non-linearity of the sampler that have not been considered in the previous chapter. The transconductance has a finite output impedance and the sampling capacitor is low. Consequently, the voltage swing on the sampling capacitor for high input swings can not be neglected. The transconductance value is modified by this voltage swing. This variation results in the effect shown in Figure 4.13.

This section shows one of the limitations of this chip : the adjacent channel attenuation is efficient only for low input power while high input power is needed to reach bit error rates below 10^{-3}

V. Improvement of the system

The last section has shown the limitations of the architecture in terms of filtering : the behavior of the sampler is degraded for input powers over -10dBm so this filtering effect is not as efficient as expected. This gain decreasing for high input swing is a common problem in OTA design [34]. One solution to increase the efficiency of the system could be to increase the linearity of the sampler.

At the same time, in recent technologies, powers over -5dBm seems to be at the maximum limit of the linearity of front-ends blocks : recent LNA shows an output saturation power between -5 and 2 dBm [35]. Consequently, instead of increasing the linearity of the sampler, it could be coherent to try to reach better sensitivity. With lower input power, the filtering might be more efficient.

This section details the improvements that should be made on the system to be able to receive signals with an input power lower than -12 dBm with acceptable BER. This should improve the overall performance of the receiver and increase the efficiency of the anti-aliasing filtering.

V.A. Supply connections

Due to the 8 contacts probe, the chip was limited in terms of number of pads. Consequently, only one VDD pad was available to supply the core and one pad to supply the buffers. Consequently an oscillation is created on the supply when a large quantity of current is needed (mainly during clock transitions). This creates non-idealities inside the subsampler that can contribute to discrepancies.

In a future version of the chip, the number of supply pads should be largely increased to limit on-chip power supply oscillations. Moreover, the analog part is the most sensitive part to these variations while the current is mostly consumed by the digital part (clock buffers). One solution to limit these interaction could also be to separate these two supplies.

V.B. Gm Calibration

The simulations of the chip suppose that all the samplers share the same gain. Due to mismatches inside the layout, some samplers may have different gains which reduce the minimum reachable sensitivity. In order to avoid this effect, each sampler should be calibrated.

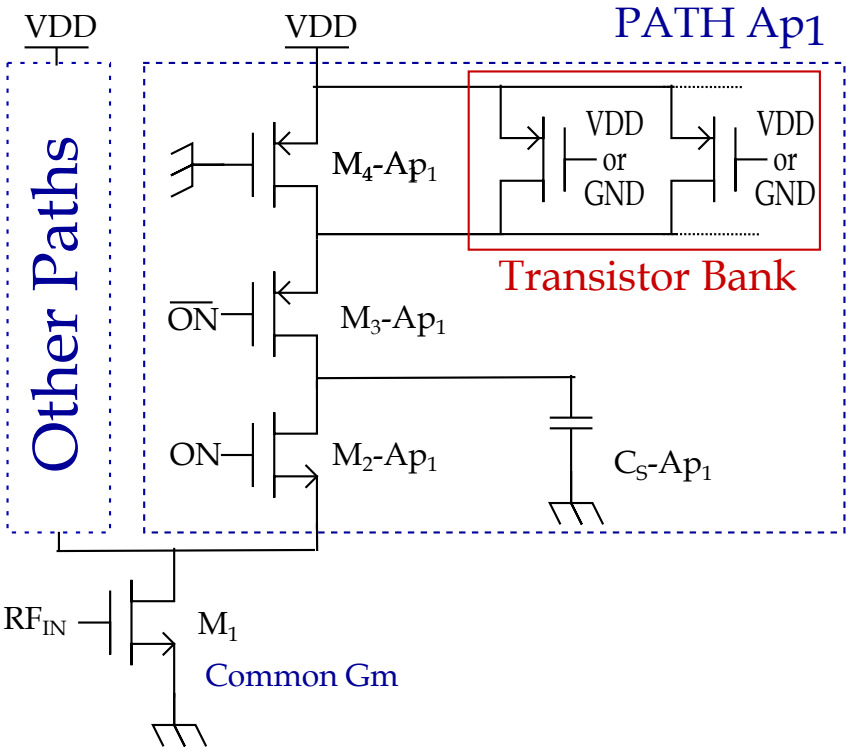


Figure 4.15: Method proposed to calibrate the samplers

A solution is proposed in Figure 4.15. The current in the the common Gm can be calibrated by setting M4 width. Tunning the current between the several integration paths equalizes the biasing between all the samplers and consequently reduces the mismatches in the system.

VI. Conclusion

This chapter has shown the test methodology of the chip and its connections on a probing station.

The first test shows that the chip, while operating at 7.04 GHz, is able to downconvert a signal from 21.12 GHz to DC. This test validates the global functionality of the chip.

A second test bench is created to validate the demodulation operation. BPSK and QPSK signals are demodulated by the chip. It achieves a 10^{-3} BER for input powers between -12 and 5dBm. As expected, the chip is more sensitive to the sampling instant in the QPSK test case than in the BPSK test case.

The aim of the third test bench is to validate the immunity of the system to the blocker. It shows that even if attenuation exists, the attenuation is lower than expected. Some of the discrepancies of this measurement between the expected value and the measured value are due to the non-idealities of the sampler in presence of high input voltage swing.

To conclude, this chip demonstrates that the subsampling is a suitable solution for RF receivers meanwhile, some points developed in Section V. shows available solutions to be able to receive low power signals (below -10dBm) and consequently to reach an efficient channel filtering.

CHAPTER

5

CONCLUSIONS & PROSPECTIVE WORK

I. Introduction

This chapter concludes the manuscript. In a first section, an update of the state of the art is given presenting the three major contributions that have been published during the four years of this thesis. The proposed quadrature subsampler implementation in 28 nm CMOS is compared with respect to the state of the art. The second section introduces a prospective work that has been started to create a component that could handle both high data rate 60 GHz and Wifi at 2.4 and 5 GHz.

II. Proposed work compared to state of the art in 2013

Since the beginning of this thesis the landscape has changed. In 2011, three complete 60 GHz transceiver have been published [1] - [3]. These contributions are detailed in this section. Then, a comparison shows how the quadrature charge domain subsampler can be situated with respect to this state of the art.

II.A. Direct conversion transceiver [1]

Figure 5.1 shows the receiver part of the transceiver proposed in [1] designed in 65nm CMOS. It consists in a LNA, I/Q dowconversion mixers and frequency triplers.

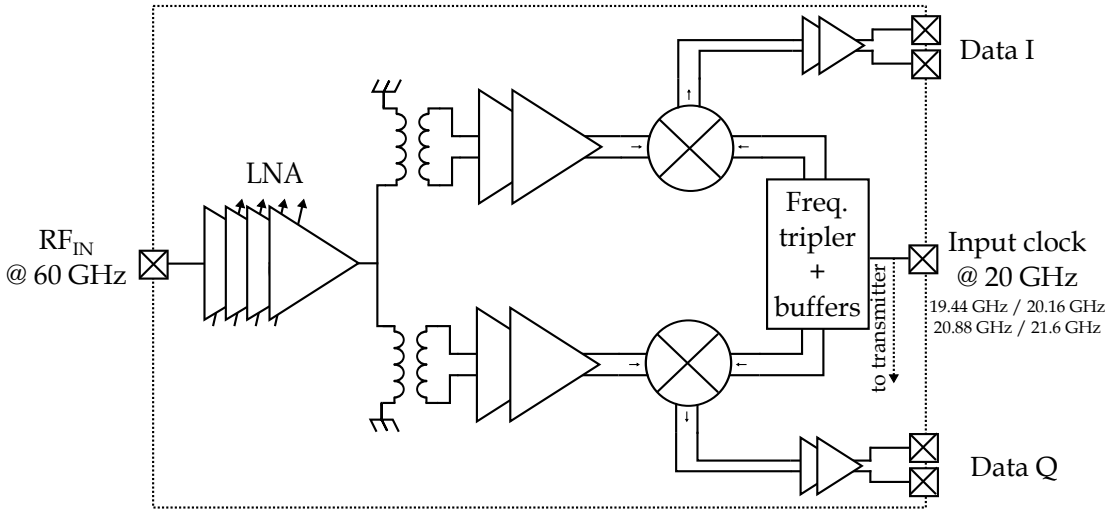


Figure 5.1: Proposed transceiver based on Direct Conversion [1]

The LNA is divided in four stages : two first stages are designed to improve the noise figure and the two following are dedicated to gain. The local oscillator is generated around 20 GHz off chip. The channel selection is done by modifying this input frequency. Frequency triplers converts this input frequency around 60 GHz in order to reach the carrier frequency of the channel of interest.

This receiver achieves a maximum conversion gain of 17.3 dB with a noise factor lower than 8dB. It can handle several modulations schemes in single carrier : BPSK, QPSK, 8-PSK and 16QAM. It achieves a power consumption of 106mW for the complete Rx and 66mW for the PLL shared with the Tx part. In the complete chip, the receiver is approximately 3.5mm^2.

II.B. Heterodyne transceiver integrated Gm-C baseband filtering [2]

Figure 5.2 shows the receiver part of the transceiver proposed in [2] designed in 65nm CMOS. It consists in a LNA, dowconversion mixers from RF to IF, a second IQ donwconversion mixer from IF to DC, Gm-C analog filters and baseband amplifiers

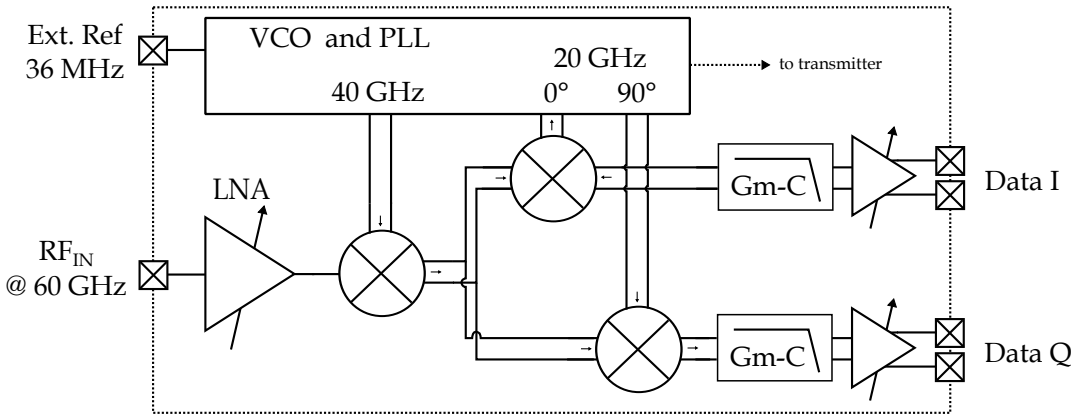


Figure 5.2: Proposed transceiver based on heterodyne conversion with integrated Gm-C baseband filtering [2]

Heterodyne downconversion is used in order to avoid routing of 60 GHz differential clocks inside the chip. A tunable VCO around 40 GHz and a frequency divider enable the generation of the required frequencies for the heterodyne receiver : around 40 GHz and around 20 GHz for respectively the first and second mixer. Consequently, tunning on the VCO modifies both 40 GHz and 20 GHz. This VCO sharing reduces the required span to reach the four channels defined in the standard. Channel filtering is performed by 3th order Gm-C filters which enables strong adjacent channel filtering.

This receiver achieves a maximum conversion gain of 40 dB with a noise factor around 8dB. It has been designed for OFDM 16 QAM. It achieves a power consumption of 374 mW for the complete Rx. The power is manly consumed by the analog baseband (300 mW). The power consumption of the PLL is 80 mW. This latter is shared with the Tx part. In the complete chip, the receiver is approximately 2.5x0.8mm^2.

II.C. Heterodyne transceiver with active IF filtering [3]

Figure 5.3 shows the receiver part of the transceiver proposed in [3] designed in 120nm SiGe BiCMOS. It consists in a LNA, dowconversion mixers from RF to IF, an active IF filter around 9 GHz, a second IQ donwconversion mixer from IF to DC and baseband amplifiers.

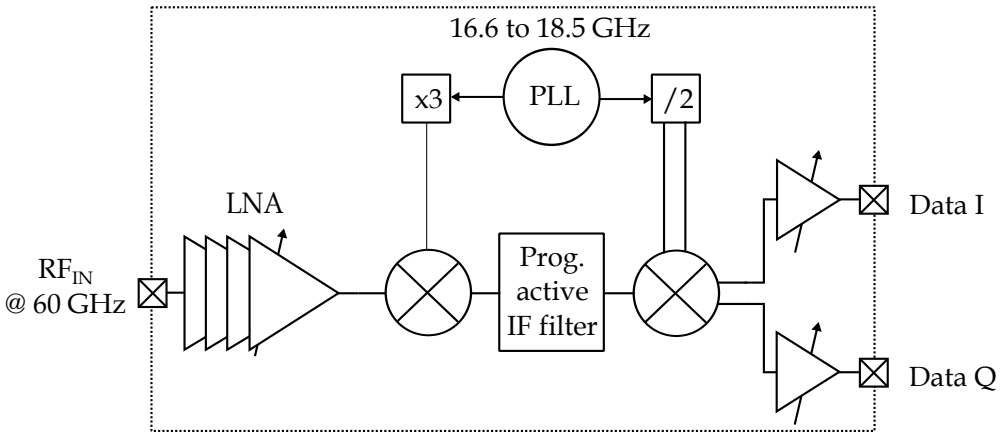


Figure 5.3: Proposed transceiver based on heterodyne conversion with integrated active IF filtering [3]

In the proposed architecture, the channel of interest is reached by tuning the PLL between 16.6 to 18.5 GHz. The channel filtering is performed by the active IF filter around 9 GHz. The overall IF response of the filter is shaped by three main components : the LC load of the RF downconversion filter which has a broad bandpass response and two cascaded active lowpass filters. This filter need to be programmable because the IF frequency is not fixed, it varies function of the channel of interest. The center frequency of the IF filter is tunable through a programmable set of discrete capacitors.

This receiver achieves a maximum conversion gain of 70 dB with a noise factor lower around 6dB. It has been designed for SC OOK, BPSK and MSK. It achieves a power consumption of 573 mW for the complete Rx. The receiver chip is 2.85x1.7mm^2.

II.D. Comparison of the proposed solution with state of the art

The performances of the circuit described in chapter 4 can not be directly compared to the state of the art because published solutions refer to complete systems from RF to analog DC while the proposed chip goes from IF at 20 GHz to digital baseband data after decoding. Consequently, some points are discussed to evaluate the added value of the measured chip.

II.D.1 Power Consumption

Between 2009 and 2013 complete systems have been published. They integrate receiver, transmitter and PLL. For the receiver part, it appears that both heterodyne and direct conversion are valuable solutions. The state of the art shows that the channel filtering is now sometimes taken into account in the design of a complete system at a high cost in terms of power consumption : 573 mW in [3] and 374 mW in [2]. In the mean time a direct receiver which do not implement channel filtering only consumes 172 mW [1]. The power consumption of a complete receiver based on the system describe in this thesis is estimated in Table 5.1 at 250 mW. This estimation uses the power consumption of the front end and the RF PLL presented in [2]. Indeed, the frequency planning in reference [2] is close to the one of the targeted system, and it seems therefore appropriate to use the blocks of [2] for power estimation of the complete 60 GHz receiver. The PLL [24] is used as reference for the low jitter clock generator at 7.04 GHz not present in [2].

	Power Consumption (mW)
Front End RF to IF [2]	80
RF PLL [2]	74
Low jitter reference clock [24]	36
Quadrature Charge Domain Subsampler (This work)	60
Total	**250**

Table 5.1: Estimated Power consumption of a complete 60 GHz receiver including the measured charge domain quadrature subsampler

II.D.2 Channel Filtering

In order to filter the adjacent channels [2] uses Gm-C 3rd order low pass filters which provide attenuation higher than 50 dBc. High attenuation is needed in this system because it targets OFDM transmissions. In [3], active IF filter based on inductors are used. This solution provides efficient filtering on adjacent and alternate channels : respectively 15 and more than 25 dBc. These two solutions are costly in terms of area because inductors are needed and in terms of power consumption because they are based on active components. The channel filtering is not considered in [1].

The system that have been tested embed adjacent channel attenuation inside the sampler between 6 and 9 dBc. The theoretical attenuation given in chapter 2. is 15 dBc and more than 30 dBc for respectively adjacent and alternate channels. The discrepancies between these measured and these ideal attenuations have been detailed in the previous chapter. In a future prototype, attenuation closer to the ideal value could be reached by modifying the layout of the chip (Chapter 4. Section V).

II.D.3 Overall Comparison

Table 5.2 compares the system that has been tested with the state of the art. Comparisons of power consumption and channel filtering are detailed in the previous subsections.

The output decoder is made of a Schmitt trigger so only 2 bits can be decoded (I/Q).This version of the chip is limited to simple modulations such as BPSK and QPSK. In a future version replacing this comparator could enable more complex modulations. However, the principle of operation of the system do not enable OFDM.

The measured chip included the decoding onchip while other systems have to add an external ADC to retrieve the digital bit stream. This work has consequently the advantage to avoid the use of an additional ADC. However, this also has a drawback : multi-path equalization is not possible because the output bit stream is already digital.

	This work	**[2]**	**[3]**	**[1]**
Topology	RF to IF [2] + IF to DC subsampling	Heterodyne	Direct Conversion	Heterodyne
Channel Compatibility	All 4	All 4	All 4	CH1 & CH2
Modulation Scheme	SC BPSK and QPSK	OFDM 16QAM	SC OOK, BPSK, MSK	SC BPSK to 16QAM
Filtering of channels	FIR + Sampler	GmC in ABB	Active IF filters	No Filters
Adjacent Channel Attenuation	6 dBc (meas.) 13.7 dBc (th.)	>50dBc	18dBc	N/A
Alternate Channel Attenuation	8 dBc (meas) 23/30 dBc (th.)	>50 dBc	>25 dBc	N/A
Decoding	Included in the sampler	External ADC	External ADC	External ADC
Technology	28 nm CMOS	65 nm CMOS	120 nm SiGe BiCMOS	65nm CMOS
Power Consumption	250 mW (est. tab. 5.1)	454 mW	573 mW	172 mW

Table 5.2: Comparison of the measured system to existing 60 GHz wireless receivers implementation

III. Convergence of WiFi and WiGig

Subsampling is a flexible approach. This section tends to demonstrate that the system that has been developed is not confined to 60 GHz applications. While using it at lower frequency, the chip can be integrated as is in a WiFi receiver at 2.4 or 5 GHz. These developments around the convergence developed in this section have been supported by the French National Resarch Agency (ANR)by the project WENDY : **W**iGig fl**E**xible tra**N**sceiver a**D**vanced s**Y**stem. The project started in november 2012 and is still ongoing. The aim of the project is to realize a complete transceiver compatible with WiFi and WiGig in 28nm CMOS FDSOI for mobile devices. IMS Bordeaux, ST Microelectronics and IEMN are involved on this project

III.A. Why convergence?

Between 2009 and 2012, first complete transceiver fully compatible with multi-Gb standard have been published [1] - [3]. Meanwhile, this first generation of chipset is stand alone and dedicated to the 60 GHz band. They are still under development in the industry and are not ready yet to be integrated inside mobile devices because the power consumption has not been consider as a key point during the development.

As developed in the first chapter, the 60 GHz band has been explored for high data rate wireless communications in the last decade. The standard IEEE 802.15.3c was created in order to replace the several existing standards for high data rate and short range communications. Due to electromagnetic constraints such as directivity of the waves and strong attenuation in the air, the 60 GHz band of the standard is not able to completely replace the 2.4 / 5 GHz band. Some applications will remain in the 2.4 / 5 GHz frequency band such over the air communications between two separated rooms or wireless communication for mid-range distances, between 5 and 30 meters.

Knowing that WiFi and WiGig will both have to be integrated in a near future of mobile devices, the second generation of chipset are thought as fully integrated systems for wireless communication. This means that a single chip could integrate the RF front end and the digital baseband of a WiFi / WiGig compatible system with high programmability behavior. Doing so, the system will be able to match the evolution of the standards and certainly also the requirements of the future standards which are still to be invented.

III.B. Re-use of the proposed quadrature charge domain subsampler for WiFi 2.4GHz / 5 GHz applications

III.B.1 Solution based on up-conversion

In the WiFi standard, several channels are defined around 2.4 GHz and 5 GHz for bandwidth from 2 to 160MHz. Basically, to re-use the test chip, the WiFi channel should be placed around 21.12 GHz to compel the chip operation at 7.04 GHz. These scheme is shown in Figure 5.4.

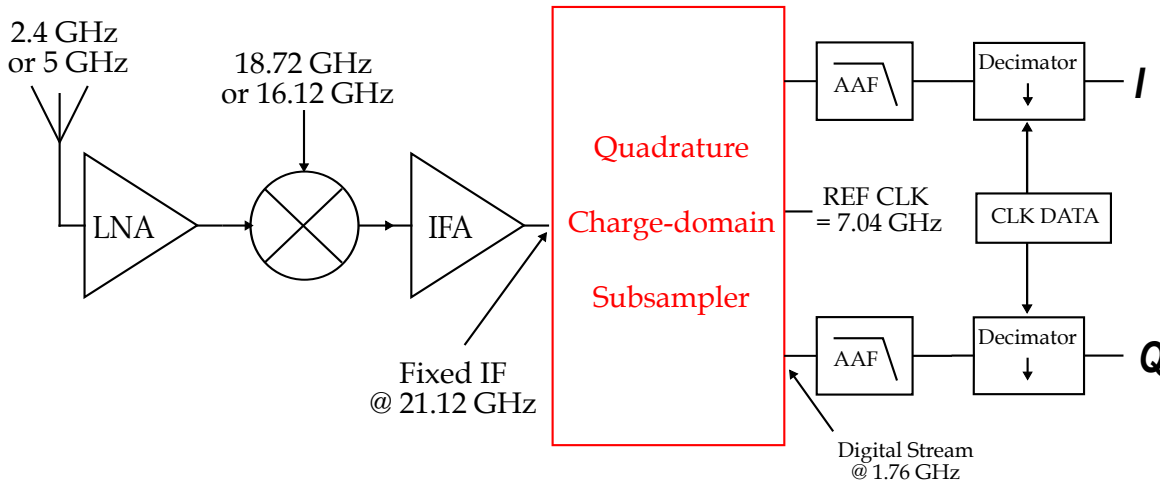


Figure 5.4: Wifi receiver based on up-conversion and including the quadrature charge-domain subsampler

At the output of the quadrature charge-domain subsampler, the data stream is four times lower than the sampling clock frequency : 1,76 GHz. This is more than 10 times higher than the highest symbol frequency defined in the standard. This oversampling ratio enable the implementation of a digital FIR that can be use to filter the adjacent and alternate channels. Finally, the data stream is decimated to reach the correct symbol frequency.

III.B.2 Solution based on direct downconversion

Knowing that the measurements have shown that the test-chip can operate with a reference clock from 1GHz to 7.1 GHz and that the RF input can be fed by frequencies from 1 GHz to 22GHz, another solution shown in Figure 5.5 can be created.

In this solution, the RF signal directly feed the sampler after the LNA. While sampling this RF signal at its exact carrier frequency, it is directly donwconverted around the DC. At the outputs of the quadrature charge-domain subsampler, the data streams are still oversampled

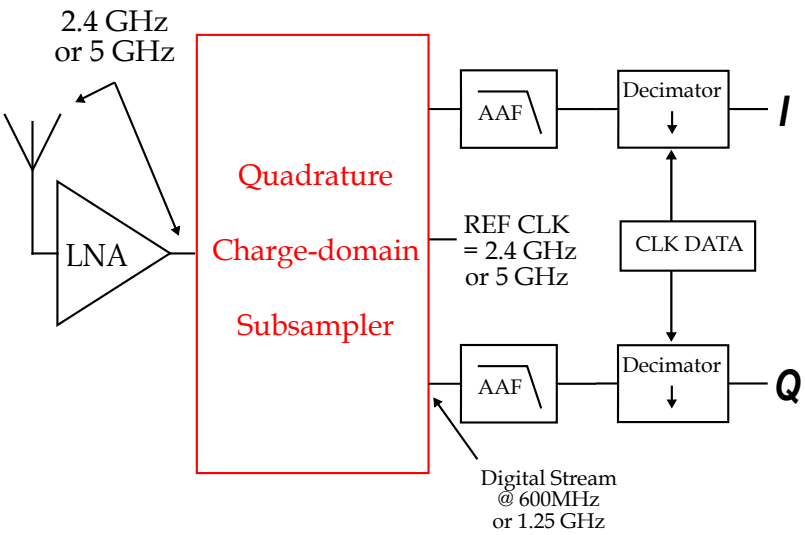


Figure 5.5: Wifi receiver based on direct down-conversion and including the quadrature charge-domain subsampler

so a digital FIR filter can be implemented at not extra cost in terms of hardware. Finally, the data has to be decimated.

III.B.3 Benchmarking of the two solutions

The first solution offers a higher oversampling ration at the output than the second one. Consequently, the anti aliasing filter would be more efficient in the first than in the second solution.

The first solution needs an additional mixer and an additional reference frequency for the up-conversion while the second one does not. Moreover, due to the reduced number of component and to the reduced frequency of operation, the power consumption would be lower in the second solution than in the first one.

Consequently, the solution based on direct downconversion is more suitable while targeting low cost application.

III.C. WiFi and WiGig compatible receiver

Figure 5.6 shows a possible multi-standard system based on the quadrature charge domain subsampler developed in this thesis.

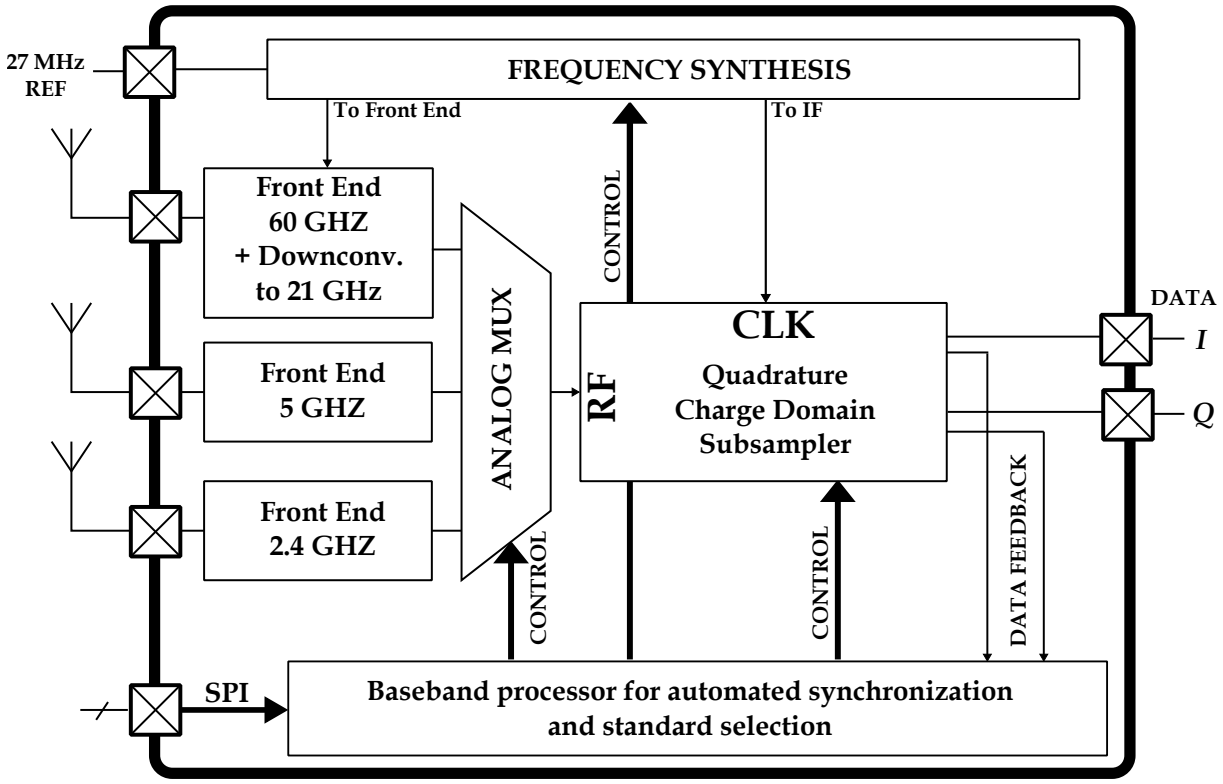


Figure 5.6: Proposed multi-standard receiver system

Three different front ends are integrated in the proposed system. Each front end is dedicated to a particular frequency range : 60 GHz, 5 GHz and 2.4 GHz. Each front end is composed of a low noise amplifier around the frequency of interest and is followed by a programmable gain amplifier in order to adapt the input level for the quadrature charge domain subsampler. The 60 GHz front end also includes a RF mixer in order to downconvert the RF input from 60 GHz to 21 GHz. An analog multiplexer enable the selection of the corresponding front end for the desired band.

The frequency synthesis creates the correct frequency for the quadrature charge domain subsampler and for the RF front end. It is fed by a 27 MHz reference for standardization purposes, a lot of products in the market use this frequency. Table 5.3 summarizes the frequency generated. As described in the previous subsection, in the 60 GHz test case, the quadrature charge domain subsampler works with a fixed 7.04 GHz reference while the channel selection is done by the RF mixer in the front-end. In the 5 GHz and 2.4 GHz test case, clock of the IF

to DC processor has to be adjusted to select the channel of interest. Inside the ANR project WENDY, the frequency synthesis unit is currently developed by IMS in Bordeaux.

	Output "To Front End"	**Output "To IF"**
Wifi 2.4G	Disabled	2.4 GHz (centered on the carrier of the channel of interest)
Wifi 5G	Disabled	5 GHz (centered on the carrier of the channel of interest)
WiGig 60G	37.2 GHz / 39.36GHz 41.52 GHz / 43.68 GHz (Depending on the channel of interest)	7.04 GHz

Table 5.3: Frequency generated by the frequency synthesis unit

The automated automated synchronization of the receiver performed by the baseband processor is detailed in annex A.

IV. Conclusion

The axis of development of the state of the art of 60 GHz wireless receivers are presented in the first section of this chapter. Some architectures use direct conversion and do not implement channel filtering while some others prefer heterodyne receivers. That architecture can integrate channel filtering around the IF or around the DC. Meanwhile, this filtering is added with a high cost in terms of power consumption and area. The first section shows that the proposed IQ charge domain subsampler can provide few dBc of attenuation for a low cost in terms of power and area because it is mainly composed of active components.

The WiFi does not tend to disappear from mobile devices in the future because some applications are not compatible with the 60 GHz waves. Consequently, in order to include both standards in the same device, a single chip that is capable to handle WiFi at 2.4 GHz /5 GHz and WiGig 60 GHz is proposed. It is composed of one front end dedicated to each frequency band, the proposed IQ charge domain subsampler and a dedicated PLL. The architecture and its detailed implementation are presented in the second section.

CONCLUSION

The thesis has been divided in five chapters. The first one introduces the 60 GHz channels and shows that at the beginning of this thesis in 2009 the state the art does not propose advanced receivers compatible with mobile applications. The second chapter proves that the subsampling is a suitable solution for an heterodyne 60 GHz receiver because the noise folding and the sampling jitter can be compatible with the requirements of the standard. A particular arrangement of the frequency plan allows embedded anti-aliasing filtering. This theoretical study has been published at IEEE ISCAS in May 2012 in Seoul. This paper have been invited for contribution to the IEEE TCAS, May 2013 special session ISCAS 2012.

The third chapter details the issues that have been encountered during the design of the prototype chip 28 nm CMOS technology. The fourth chapter details the measurements. They have shown that the subsampling operation is fully functional up to the frequency of interest : sampling at 7.04 GHz an RF signal around 21.12 GHz. Modulated BPSK and QPSK data streams at 1.76 GHz can be received with a BER below 10^{-3} for input powers from -10 dBm to 5 dBm. Adjacent channel attenuation is provided but it is lower than expected the theoretical study and needs improvement especially on the transconductance stage. The design issue limits the adjacent channel attenuation to 9dB. The chip implementation and measurement results will be submitted to IEEE RFIC 2014.

The fifth chapter shows that the prototype can not be directly compared to the state of the art because only the IF to DC part have been implemented. However, the prototype introduces the possibility to include the adjacent channel attenuation directly in the sampler without any extra cost in terms of area or power consumption. The proposed IF to DC has the advantage to be able to receive RF signals from 1 to 21 GHz. Consequently, an ongoing project uses the core of the chip for a Wifi and WiGig complete receiver with integrated synchronization

APPENDIX

A

AUTOMATED SYNCHRONIZATION

During the measurements, the synchronization of the receiver has been done by hand, the bit error rate has been evaluated to check if the sampling instant is correct. In the future, a complete receiver should be able to synchronize by itself on the input signal. Meanwhile the BER can not be used because the receiver does not know what is the correct bit stream. One solution to ensure that the sampling instant is correct is to check that all the points are grouped in a corner in order to form a square constellation. An algorithm based on that principle has been created. This work has been developed with the support of Cristian Marin during his internship from February to August 2013.

The algorithm is divided into three main parts. The first part consists in a "fast detection" which find the correct symbol synchronization and which roughly find an acceptable synchronization between the sampling instant and the phase of the IF frequency. The second part consists in a "fine adjustment" of the sampling instant to be as close as possible to the ideal one. The last one consists in modify if the "IQ delay setting" if the default value was too far from the ideal case.

In order to evaluate the functionality of the algorithm, a Matlab file has been generated and used to emulate the input signal. White noise has been added in order to move from an ideal input to file a realistic case.

I. Synchronization scheme

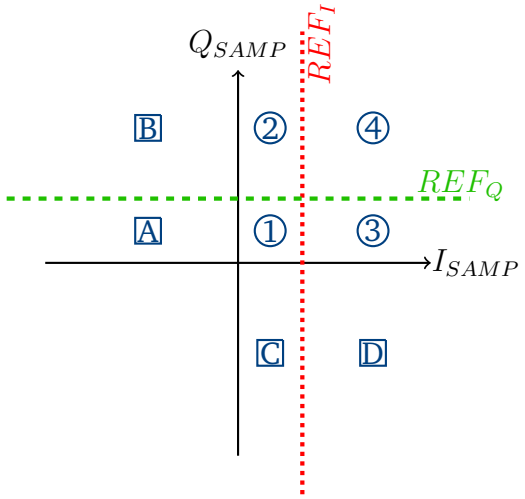
I.A. Fast Detection

During the fast synchronization process, the constellation have been divided into 8 areas as shown in Figure A.1(a). The dashed and dotted lines for REF_I and REF_Q represented are the limits of these areas for a given input power. I_{SAMP} and Q_{SAMP} are respectively the values sampled for I and Q before the Schmitt trigger. Dedicated comparators onchip compares I_{SAMP} and Q_{SAMP} with REF_I and REF_Q in order to know where are the sampled values regarding the references.

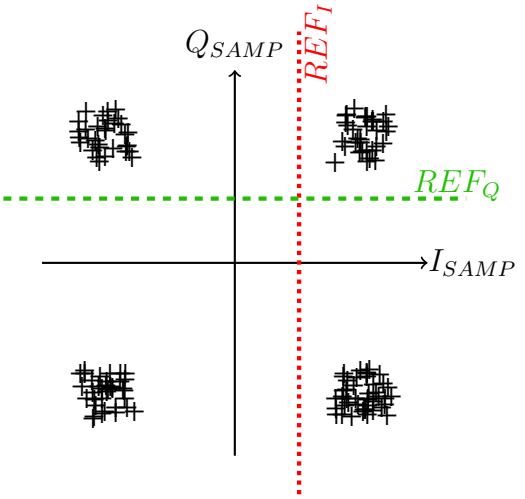
When an offset exists between the sampling instant and the beginning of the symbol, the points either form groups of points in each quadrant (Figure A.1(d)) or are separated in 9 groups (Figure A.1(c)). In these two conditions, a significant amount of points are found in area 1. In this case, the ideal sampling instant is far from the actual one. Consequently, the sampling instant can be increased by 'large size' steps (tens to hundreds of pico-seconds). In order to do so, chain of inverters can be dynamically added in the sampling clock path.

When the symbol synchronization is correct, the points are grouped all together in each quadrant. Meanwhile, the constellation can still suffer of a phase rotation regarding the ideal constellation. When this angle is large, the points are grouped in area 2 or 3 as shown in Figure A.1(e). This represents a large offset between the sampling instant and the phase of the IF frequency. Consequently, the sampling instant can be modified by 'intermediate size' steps (few of pico-seconds). In order to do so, the slew rate controlled inverters presented in Chapter 3 can be used.

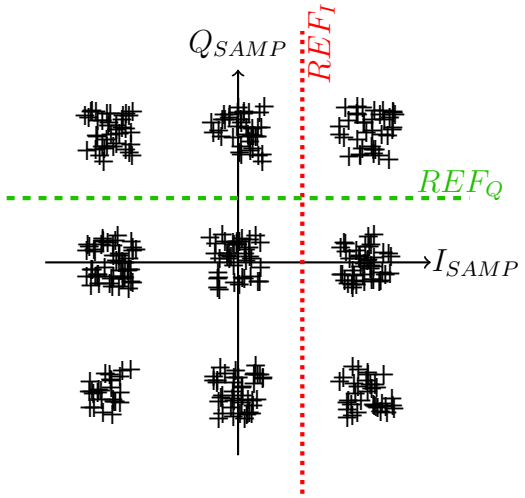
After this second adjustment, the points are grouped inside area 4 as shown in Figure A.1(f). A small error remains between the sampling instant and the phase of the IF frequency. A finer adjustment have to be performed.



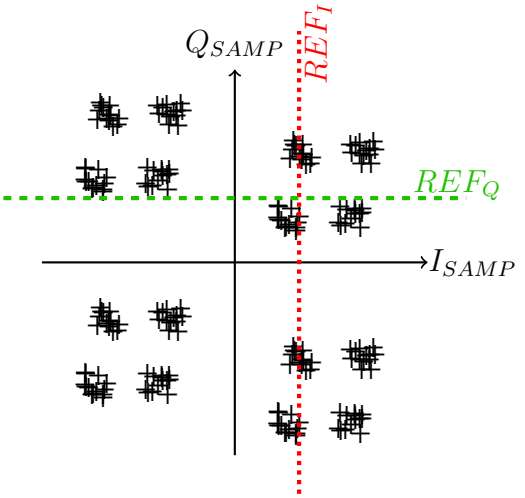
(a) Division of quadrants used for synchronization



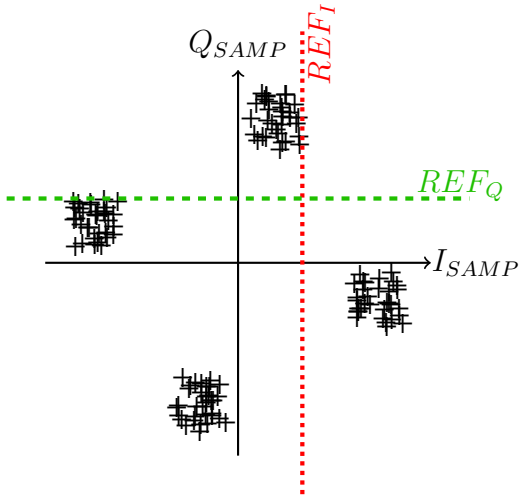
(b) Ideal constellation



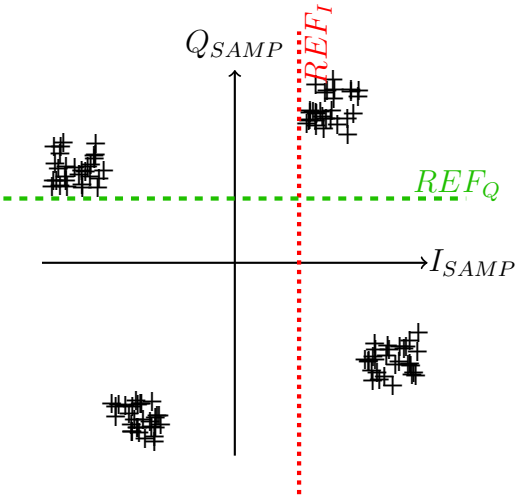
(c) Constellation with a large offset between the sampling instant and the phase of the data clock



(d) Constellation with a small offset between the sampling instant and the phase of the data clock



(e) Constellation with large offset between the sampling instant and the phase of the IF frequency



(f) Constellation with a small offset between the sampling instant and the phase of the IF frequency

Figure A.1: Constellations for several sampling instants during the fast detection procedure

I.B. Fine Adjustment

During the fine adjustment procedure, the idea is to form a square constellation. In oder to do so, the position of the group of points have to be known.REF_I and REF_Q which were fixed references in the fast detection process are now variables in the fine adjustment process : REF_{I-FINE} and REF_{Q-FINE}. They are updated until an equal distribution of the points between the top and the bottom part is achieved. To have a relevant estimation of the position, simulations have shown that 10 points are needed. Figure A.2 shows the resulting placement of the references when the amount of points is found.

When this position is found, the algorithm knows how the sampling has to be modified to reach the ideal case. This latter can be translated for the algorithm by $REF_{I-FINE} = REF_{Q-FINE}$ with an error margin. In order to do so, the slew rate controlled inverters presented in Chapter 3 can be used. After this setting, the sampling instant is close to the ideal case.

I.C. IQ Delay setting

Since the beginning of the synchronization procedure, the IQ delay is set to a default value. When arriving in this last step, the points in the top right quadrant are close to the ideal position. This can be checked on the constellation by evaluating the repartition of the points

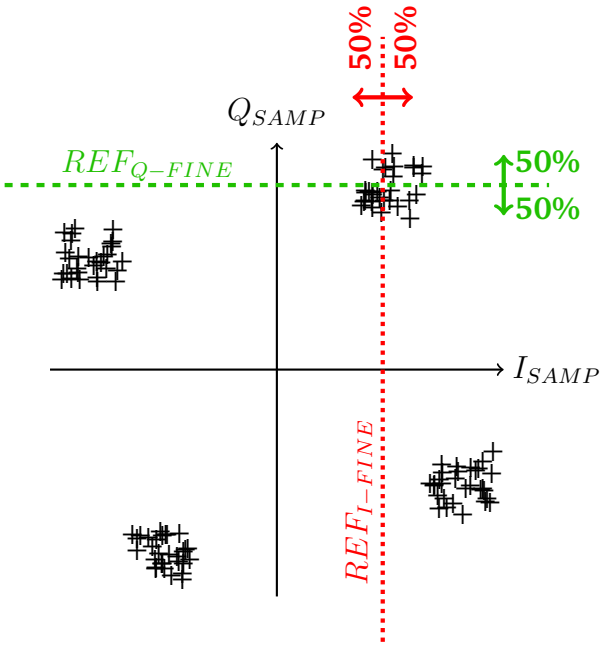


Figure A.2: Placement of the references to detect the position of the group of points

in the top left and in the bottom right corner. If they are not equally distributed around the references as shown in Figure A.3, the constellation is not square. Thus, the IQ delay have to be updated. In order to do so, the slew rate controlled inverters placed after the split of the clock paths between I and Q are used. The resolution needed is still below 1 pico-second. After that setting, the constellation shall be square and with the correct phase.

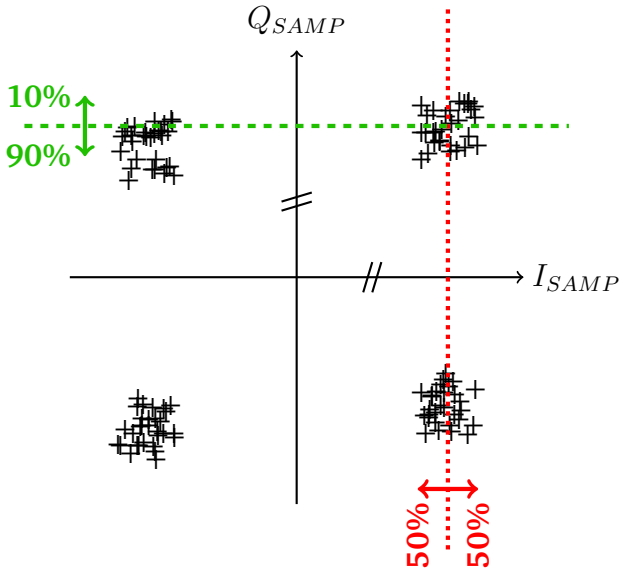


Figure A.3: Detection of a non-square constellation

II. Resulting algorithm

Figure A.4 shows a tree representation of the algorithm that has been explained in the three previous subsections.

II.A. Test of functionality

In order to validate the functionality of the chip, it has been implemented and run with Matlab. Figure A.5 shows the simulation results. Figure A.5(a) shows the sampling instant versus the number of symbols read. Figure A.5(b) shows the evolution of the references REF_{I-FINE} and REF_{Q-FINE} to the maximum possible value where both of them are equal. This maximum value depends on the power at the input of the receiver. Figure A.5(c) shows the evolution of the IQ delay. Finally, the constellations in Figure A.5(d) and Figure A.5(e) shows the state of the sampled value at the beginning of the algorithm (the input signal is

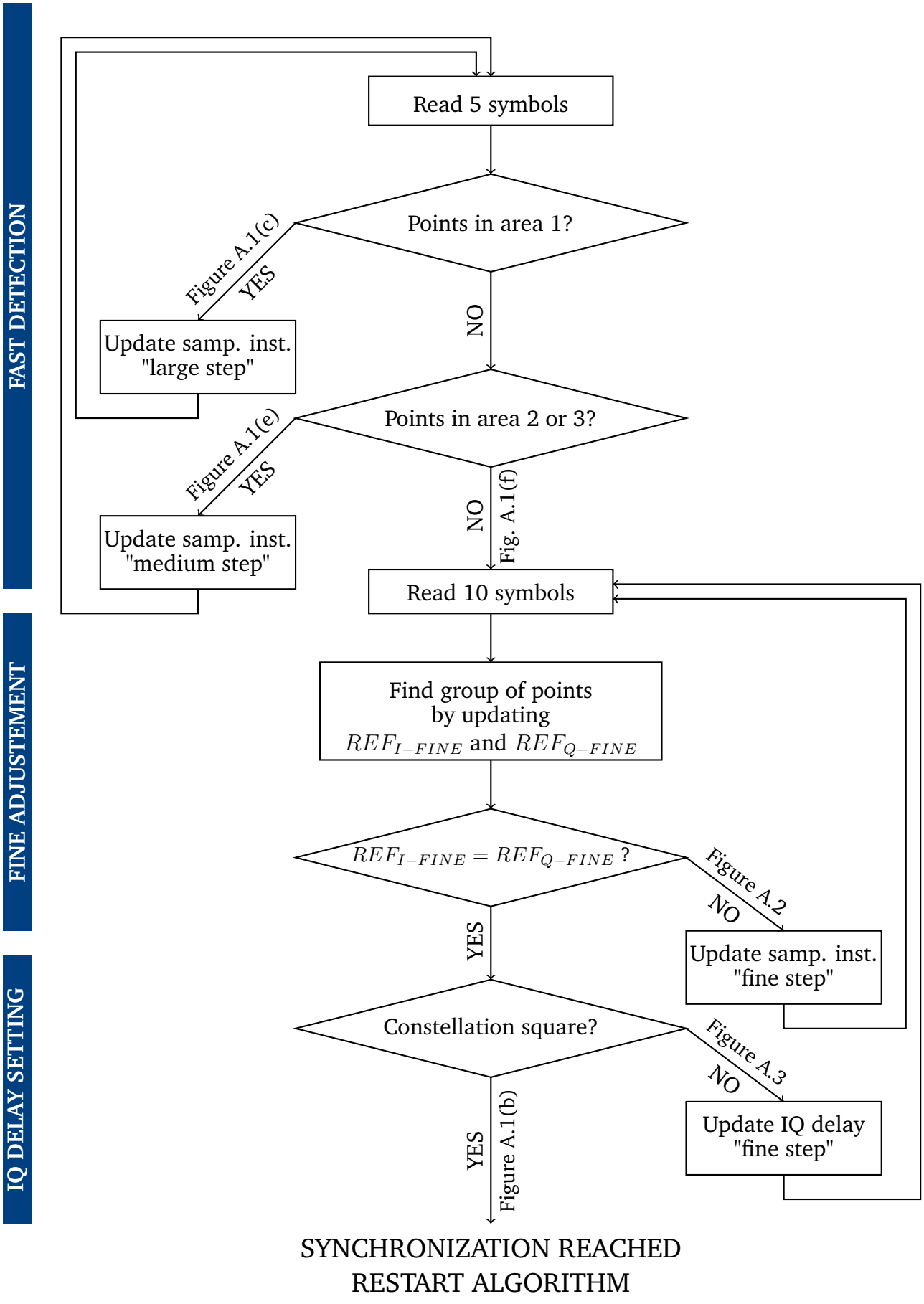


Figure A.4: Block diagram of the synchronization algorithm

sampled at a random instant) and after convergence of the algorithm.

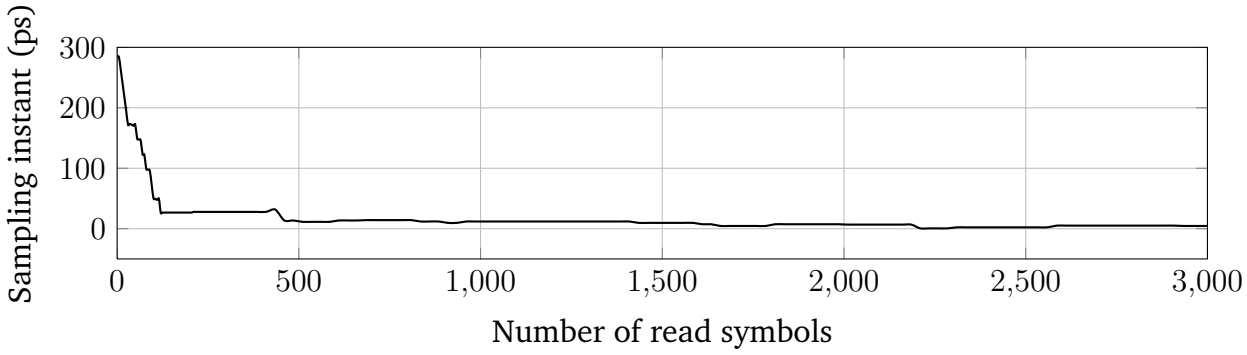
This simulation shows that the algorithm is able to converge in a finite time. In this typical case, Figure A.5 shows that the algorithm needs to read 2575 symbols to converge to the final sampling instant value. At the data rate of the chip (1.76 GSps), this corresponds to 1.3 μs. After the convergence, the references are still updated because the algorithm always tries to find a best solution.

II.B. Speed of convergence through process

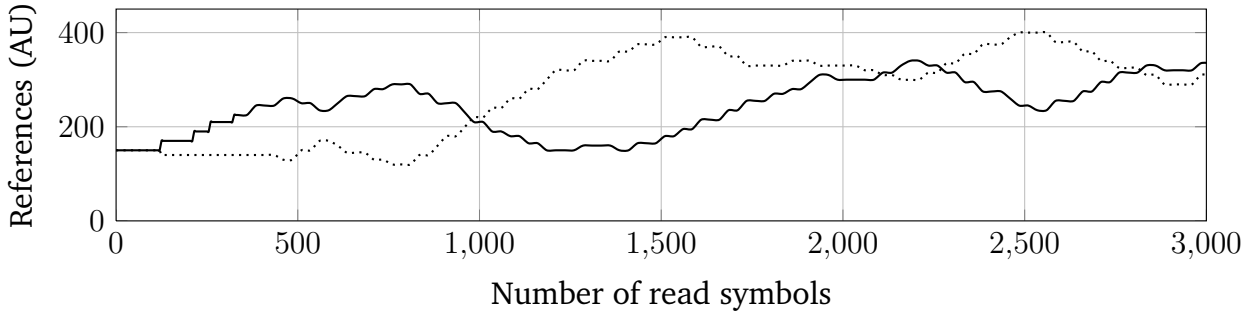
The algorithm uses a digital code to command the sampling instant. Meanwhile this code can result in a different delay due to process variations. These variations have been included in the Matlab code in order to ensure that the algorithm is able to converge in all the corners. Simulations have shown identical behavior for all the corners : the convergence can be reached. Under certain process conditions more symbols have to be read. Table A.1 sums up the number of data necessary for the algorithm to converge under the same scenario.

Corner	**Number of data**	**Corresp. time at 1.76 GSps**
TYP	2275	1.29 μs
SS	2330	1.32 μs
SF	2275	1.29 μs
FS	2060	1.17 μs
FF	2285	1.30 μs

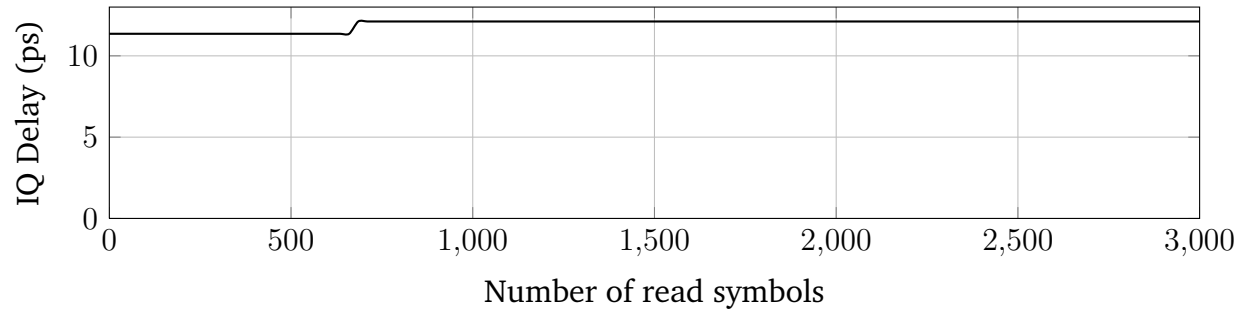
Table A.1: Number of data necessary for the algorithm to converge



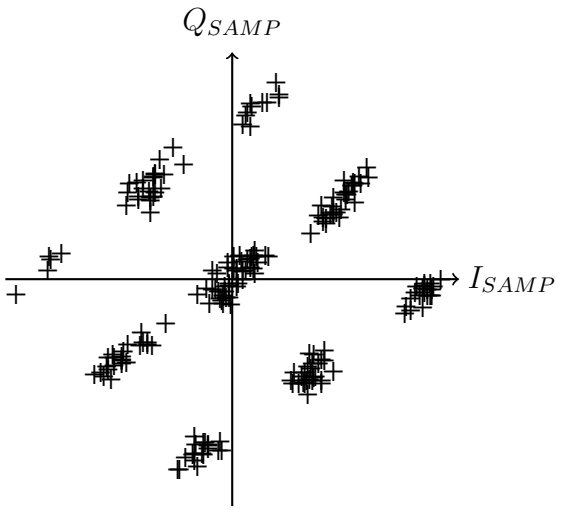
(a) Evolution of the sampling instant (0 is the ideal value)



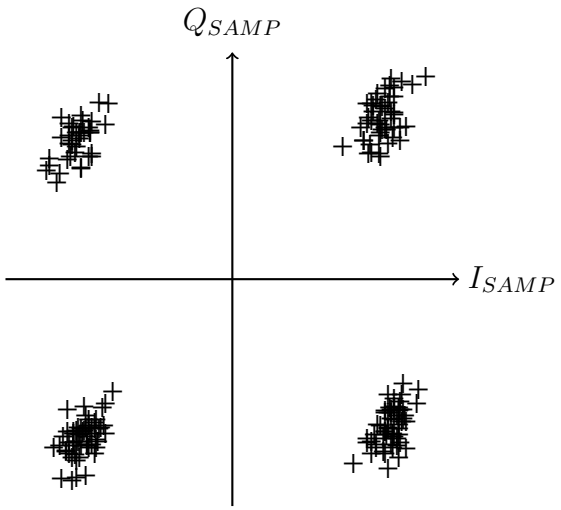
(b) Evolution of REF_{I-FINE} (plain) and REF_{I-FINE} (dotted)



(c) Evolution of the IQ delay



(d) Constellation at the starting point (random)



(e) Constellation after convergence

Figure A.5: Evolution of the parameters of the algorithm during one run

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