UNIVERSITE LILLE 1 SCIENCES ET TECHNOLOGIES

École doctorale : Sciences pour l'ingénieur
Institut d'Electronique, de Microélectronique et de Nanotechnologie

THÈSE

Présentée par

Aurélien LECAVELIER DES ETANGS-LEVALLOIS

Pour obtenir le grade de

Docteur de l'Université

Spécialité Micro et Nano Technologies, Acoustique et Télécommunications

Report de technologie SOI-CMOS sur substrat flexible : une approche convergente vers les hautes fréquences et la stabilité des performances sous déformation mécanique

Soutenue le 21 mars 2013 devant le jury composé de :

M. Claude PELLET, Professeur Université Bordeaux 1	Président
M. Jan VANFLETEREN, Professeur Université de Gand	Rapporteur
M^{me} Mireille MOUIS, Directrice de Recherche CNRS, IMEP-LAHC	Rapporteur
M. Daniel GLORIA, Ingénieur Recherche STMicroelectronics	Examinateur
M^{me} Christine RAYNAUD, Ingénieur Recherche CEA LETI	Examinateur
M. François DANNEVILLE, Professeur Université Lille 1	Examinateur
M. Emmanuel DUBOIS, Directeur de Recherche CNRS, IEMN	Directeur de Thèse

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Very high frequency, mechanically flexible and performance stable integrated electronics based on SOI-CMOS transfer bonding on plastic substrates

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AFM	Atomic Force Microscopy
BEOL	Back End of Line *(interconnection multilayer network)*
BOX	Buried Oxide (*silicon dioxide layer in SOI technology, see SOI*)
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CPW	Coplanar Waveguide
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
dpi	dot per inch
DOD	Drop on Demand
FET	Field Effect Transistor
FIB	Focussed Ion Beam
HEMT	High Electron Mobility Transistor
HNA	Hydrofluoridric, Nitric, and Acetic acids mixture
HR	High Resistivity
HV	High Voltage
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LNA	Low Noise Amplifier
MEMS	MicroElectroMechanical Systems
MESFET	Metal Semiconductor Field Effect Transistor
MM	More-Moore

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MtM	More-than-Moore
MWCNT	Multi Wall Carbon Nanotube
NEMS	NanoElectroMechanical Systems
NRE	Non Recurring Engineering *(cost)*
NT	Nanotube
NW	Nanowire
OFET	Organic Field Effect Transistor
OSC	Organic Semiconductor
OTFT	Organic Thin Film Transistor
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PI	Polyimide
PMMA	Polymethyl methacrylate
POSS	Pad Open Short Short *(deembedding methodology)*
PTFE	Polytetrafluoroethylene
quasi-TEM	quasi-Transverse Electric and Magnetic mode
RF	Radio Frequency
SCE	Short Channel Effects
SEM	Scanning Electron Microscopy
SiP	System in Package
SoC	System on Chip
SOI	Silicon on Insulator
SPM	Scanning Probe Microscopy
SPR	*Megaposit^{TM} positive photoresist*
SS	Subthreshold Slope

SSEC	Small Signal Equivalent Circuit
SU-8	*MicroChem^{TM} epoxy negative photoresist*
SWCNT	Single Walled Carbon Nanotube
TEM	Transmission Electron Microscopy
TFT	Thin Film Transistor
TMAH	Tetramethylammonium hydroxide
VLS	Vapor Liquid Solid
WSN	Wireless Sensor Network

General Introduction

The semiconductor industry started to grow from the late 1960s to be worth more than 300 billions dollars nowadays [1]. The constantly growing electronic market and the emergence of numerous novel applications of integrated circuits required and also gave rise to a constant increase of performance and density, in addition to a concomitant decrease of manufacturing costs. For more than half a century a world wide effort has been devoted to overcome technological hurdles in order to keep this down scaling trend, commonly known nowadays as '*Moore's law*' [2], [3]. However since a decade, a physical and economical limit to miniaturization has been predicted, as the minimal feature size of electronic components is approaching the atomic scale [3].

As a result to this foreseen red brick wall, intense research efforts have been focused on diversification from the historically CMOS (Complementary Metal Oxide Semiconductor) down scaling baseline, also referred to as '*More Moore*'. This trend gave rise to the so called '*More than Moore*' field where added value is provided by the co-integration of various functionalities [4]. In this context, numerous systems were embedded in a single chip, or package, to provide interaction with people or environment [5].

For one or two decades, a growing interest has been devoted to the field of flexible electronics. Intense research activities have been carried out in exploring the possibilities to provide mechanical bendability, or even stretchability to electronic devices and circuits [6]. Numerous applications in local monitoring on non planar and large surfaces (e.g. human body, airplane, or building structure) are foreseen in this field [7]. As a result, flexible communicating, sensing, actuating, energy harvesting and storage systems have to be developed to allow the realization of fully flexible smart systems.

Low cost, large area, but low frequency devices and circuits can be processed with current organic semiconductors. They are intrinsically flexible [8], but their frequency performance is currently limited to the MHz range [9]. As higher frequencies are required for numerous applications [4]–[6], novel strategies have been developed to combine high frequency and bendability. The integration of chemically synthesized nanotubes [10], [11], or patterned thin-films [12]–[15] on plastic foils enabled the realization of GHz flexible devices. Furthermore, transistors initially fabricated on conventional rigid silicon wafers before thinning and transfer on organic films allow the field of flexible electronics to reach the 100-GHz range [16], [17].

The work presented here falls in this context, and its objective is to demonstrate the feasibility of high frequency and low noise flexible building blocks for the development of high performance foldable electronics. In partnership with *STMicroelectronics*, this research project aims to develop and evaluate a methodology that enables the transfer of the potential and capabilities of a mature, high performance, rigid technology to applications where bendability (or non-planarity) is required.

This document is divided into three main chapters, and each one contains two parts. The first chapter provides an overview of the field of flexible electronics for high frequency applications. It then highlights the need for higher performance flexible electronics and presents a mature CMOS technology as a promising solution. The second chapter of this manuscript details the fabrication process developed in this work to realize flexible CMOS chips. It then demonstrates that flexible devices exhibit performance competitive with their

rigid counterparts. The third and final chapter of this document focuses on the mechanical aspects of this work by simulating the impact of bending a flexible CMOS chip on its electrical properties and also propose a method to minimize it. Theoretical calculations are then compared with electrical measurements performed on bent devices.

Chapter 1

The first chapter of this work reviews the recent developments in the field of high frequency flexible electronics, its prospective applications, perspectives, and the associated challenges. Starting from the limitations intrinsically associated with current organic electronics that confine it to low frequency applications [9], this chapter covers various solutions suggested to enhance flexible electronics capabilities. Most of them are based on the hybridation of flexible organic substrates with thin inorganic nanostructures featuring high charge carrier mobilities [6], [7]. It will be shown that this approach has enabled the realization of flexible transistors reaching the GHz range, using either a 'bottom-up' [10], [11], or a 'top-down' approach [12]–[14]. The need for communicating and smart foldable devices requiring higher frequency, flexible electronics is highlighted and the hybridation of organic materials with a mature conventional CMOS technology is suggested as a promising solution.

The second section of this chapter therefore focuses on the 65 nm node silicon-on-insulator (SOI) radio-frequency (RF) CMOS technology, along with the measurement techniques used to characterize it. Models used to describe RF operation of this technology are reported in addition to the description of measurement equipments and methods required to fully characterize transistors. Commonly used measurement equipements, calibration techniques and also deembedding methodologies are presented, in order to take into account the systematic errors of the measurement setup and the parasitic contributions of passive elements surrounding the transistor under test. This section then details the static, radio-frequency and noise performance of the 65 nm node SOI RF-MOSFETs on their initial rigid substrate.

Chapter 2

The aim of the second chapter is first to describe the methodology developed in this work to transfer high performance flexible CMOS chips on a flexible substrate and then to characterize and compare them with their rigid counterparts. The first part of this chapter will then focuses on the transfer process comprising the thinning of inorganic CMOS dies from about 800 µm down to micrometer scale thin films and their transfer-bonding onto plastic foils. It is demonstrated that the 780 µm thick silicon handler of the initial SOI wafers can be completely remove without damaging the 145 nm thick buried oxide layer by successively using different etching techniques (chemical-mechanical lapping, wet etching in hydrofluoric and nitric acids and $Si:Si0_2$ selective dry etching in pulsed gaseous XeF_2). Different transfer and bonding methodologies are then presented and compared in order to finally obtain thinned CMOS chips bonded onto flexible plastic handlers.

After detailing the fabrication process, the second section of the chapter deals with the electrical characterization of the CMOS RF transistors transferred on plastic. Similar static and radio-frequency behaviors between rigid and flexible RF-MOSFETs will be presented, along with (to our knowledge) the highest reported performance in terms of high frequency and low noise operation on a flexible handler. Cut-off and maximum oscillation

frequencies of 150/160GHz and 110/130GHz will be demonstrated for n- and p-MOSFETs on plastic respectively. In addition, both n- and p- type transistors on plastic featuring minimal noise figure and associated gain of 0.57/17.8dB and 0.57/17.0dB at 10GHz respectively will open the way to radio-frequency and low noise flexible electronics. In order to demonstrate that the presented flexible transistors can be used as building blocks for high performance flexible electronics, transmission lines and circuits (low noise amplifiers, LNA) processed on the same technology and transferred on plastic will be characterized, showing that RF circuits can be directly transferred on plastic without resorting to a specific redesign.

Chapter 3

The third chapter focuses on the mechanical aspects of this work. A logical question arising from the two previous chapters is: how would flexible electronic devices and circuits behave under flexure. The aim of this last chapter is thus to provide elements of answer to this question. The first part therefore details some mechanical aspects related to the mechanics associated to cylindrincal bending of multilayer stack systems, and applied them to the flexible CMOS stack presented in previous chapters. From an application point of view, electrical properties stable upon deformation are required. A methodology relying on neutral plane engineering to provide performance stability will therefore be presented and supported by electro-mechanical modeling.

After describing the required theoretical background, electrical measurements performed on bent flexible CMOS devices will be compared with computed values. Their good agreement will demonstrate the efficiency of the neutral plane engineering method. Following this strategy, high frequency performance of flexible n-MOSFETs featuring f_T/f_{MAX} of 120/145 GHz, are reported with relative variations limited to less than 5% even under aggressive bending on cylinders with curvature radii down to 12.5 mm. These results pave the way to a novel high performance and highly foldable flexible electronics. Indeed, the simultaneous demonstration of high frequency, mechanical compliance and performance stability upon deformation will give rise to numerous novel applications.

This manuscript will be concluded by a summary of the important results of the present work. Emphasis will be put on the following indispensable triptych: very high frequency (>100 GHz), mechanical flexibility and performance stability. Perspective for future work will also be discussed.

Chapter 1: **Combining high frequency and high flexibility**

This first chapter reviews the recent developments in the field of high frequency flexible electronics, perspectives, prospective applications and associated challenges. Starting from the limitations intrinsically associated with current organic electronics that confine flexible electronics to low frequency applications, this chapter covers various suggested solutions to enhance performance of flexible electronics. Most of them are based on the hybridation of flexible organic substrates with thin inorganic materials featuring high charge carrier mobilities. This approach enabled the realization of flexible transistors reaching the GHz-range. The need for communicating and smart foldable devices requiring higher frequency flexible electronics is highlighted and the hybridation of organic materials with a mature CMOS technology is suggested as a promising solution.

Therefore, the second section of this chapter focuses on the 65 nm node silicon-on-insulator (SOI) radio-frequency (RF) CMOS technology, along with the measurement techniques used to characterize it. Models used to describe RF operation are reported in addition to the description of measurement equipments and methods required to fully characterize transistors. This section then details the static, radio-frequency and noise performance of the 65 nm node SOI RF-MOSFETs before transfer on a flexible film.

1.1 Recent developments in the field of flexible electronics

1.1.1 Opportunities and challenges of flexible electronics

The first part of this chapter focuses on the recent emergence and rapid development of the field of flexible electronics. In parallel to the continuous world wide effort to scale down transistors and memories, intense research has also been focused on giving a novel dimension to conventional electronics: mechanical bendability. Organic semiconductors allowed the realization of the first flexible electronic devices. Several other methods based on organic/inorganic hybridation enabled the field of flexible electronics to reach higher performance. Recent progress and prospects of this domain will be reviewed and discussed in the following sections. Finally, the objectives of this work will be detailed.

1.1.1.1 *'More-Moore' and 'More-than-Moore' contexts*

1.1.1.1.1 Challenges associated with the 'More-Moore' trend

Since the late 1950's, the microelectronics industry has been experiencing an exponential development, leading to a constant miniaturization of the microelectronics components and a concomitant increase of their performance. This tendency has been predicted in 1965, at the early days of the integrated circuits, by Intel® co-founder Gordon E. Moore [2]. This trend is now commonly referred to as 'Moore's law', and enunciates that the density of transistors per integrated circuit, at which a minimum component cost is reached, doubles every two years. Fig. 1.1-a shows the historical evolution of the manufacturing cost of integrated circuits as their complexity increases, in addition to the concomitant increase of wafer diameter.

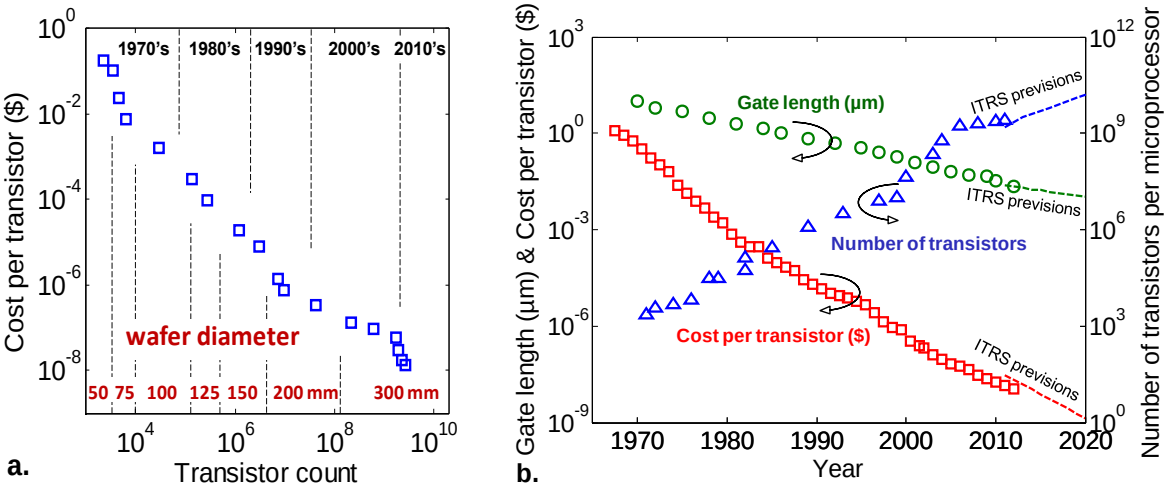


Fig. 1.1 – a. Evolution of the manufacturing cost of integrated circuits as their complexity increases, and b. Moore's law as it is commonly represented: number of transistors per microprocessor as a function of time, gate length and cost per transistors are also plotted in addition to International Technology Roadmap for Semiconductors (ITRS) previsions [2]–[4], [18], [19]

Considered as a prediction at the infancy of the semiconductor industry, this trend became the driver of the world semiconductor industry. This is illustrated in Fig. 1.1-b where it can be observed that the number of transistors per microprocessor was multiplied by a factor of one million in about half a century (reaching 3.1 billions in Intel® Itanium processor in 2011), with a concomitant decrease of the transistors dimensions (by a factor of almost one thousand in 50 years) and cost (from 1$ per transistor in the late 1960s to less than a µ$ nowadays). Even if challenges appeared with the miniaturization of electronic devices, the semiconductor industry has successfully followed Moore's law up to current days. This has been enabled by the development of novel processing equipments (e.g. the use of deep-UV excimer laser photolithography), in addition to novel strategies in device architecture (e.g. the addition of strain engineering, high κ materials, or metal gates), and to a constant increase of wafer diameter (Fig. 1.1-a). However, a physical limit of the current downscaling methodology of transistor dimensions can be foreseen as it is approaching the atomic scale. Furthermore, this miniaturization is concomitant to a drastic increase of the development and production equipment costs for each new technological node. These observations lead to the emergence and growing of a new field, called 'More-than-Moore', where the added value does not rely on downscaling and increasing intrinsic performance but is rather provided by the incorporation of novel functionalities on the same chip.

1.1.1.1.2 Rise of the 'More-than-Moore' trend

The 'More-than-Moore' field has been growing in parallel to the conventional 'More-Moore' effort during the last decades. A large number of nano- or micro-electromechanical systems (NEMS, or MEMS), active or passive radio-frequency (RF) and analog-mixed signal devices, high voltage (HV) power devices, various sensors and actuators have been packaged together in embedded systems to provide better interaction with the environment. This integration of novel functionalities, providing diversification from the baseline CMOS downscaling also results in higher value systems and is driven by the International Technology Roadmap for Semiconductors (ITRS) [4]. Fig. 1.2-a shows a chart detailing that higher value systems can be fabricated by following i) the 'More-Moore' down scaling of CMOS technology, memory, and logic, ii) by providing functional diversification to connect the CMOS chips with the environment, and iii) the ITRS recommendations are to combine both approaches in Systems-on-Chip (SoC) and Systems-in-Package (SiP) [4].

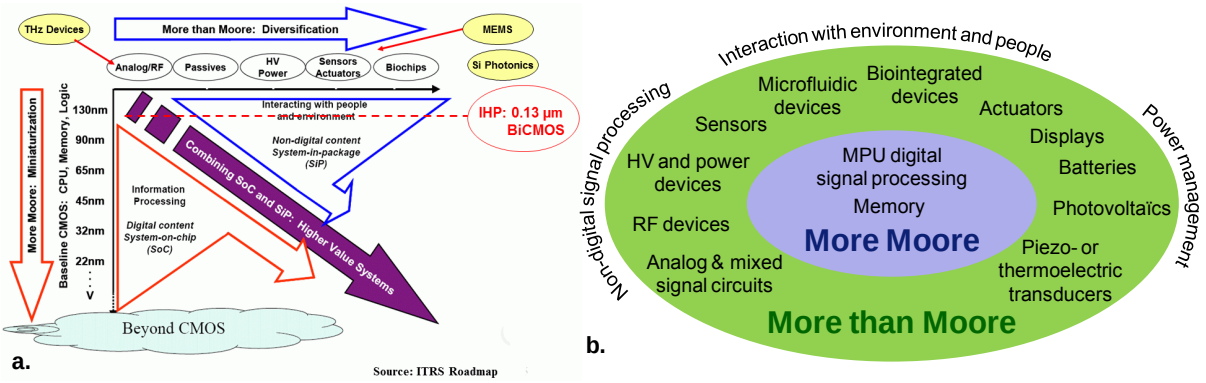


Fig. 1.2 – a. Chart, reproduced from the ITRS [4], showing the parallel developments of the 'More-Moore' and 'More-than-Moore' fields, b. Chart explaining how 'More-than-Moore' components can integrate and complement the digital signal processing, or 'More-Moore' core to add non-digital processing capabilities, power management and interactions with environment and people

The co-integration of a large variety of non-digital systems (Fig. 1.2-b) providing additional functionalities to the digital signal and data processing chip gave rise to the so-called Systems-on-Chip (SoC) and Systems-in-Package (SiP). The former describes the integration on the same chip of novel functionalities, whereas SiP corresponds to the bonding in the same packaging of several chips with different functionalities. SoC usually offers improved performance, lower cost in volume, and higher density at the expense of longer time to market and higher non-recurring engineering (NRE) costs. Conversely, SiP enables the co-integration of different front end technologies, the change or upgrading of individual component assuming that complex assembly and power management for stacked dies can be performed [5]. In this context, the addition of mechanical bendability to single data processing chip or complex SoC or SiP can be seen as another functional diversification.

1.1.1.1.3 Conventional electronics growing interest for the 'More-than-Moore' context

A clear interest of the conventional semiconductor industry in a functional diversification can be noticed since a decade. An increasing number of references to the 'More-than-Moore' development line, and especially to flexible electronics, can be seen in the latest ITRS reports in various chapters. Indeed, numerous required and challenging technological developments related to the field of flexible electronics have been identified in 'assembly and packaging', 'interconnections', 'emerging research devices and materials', and 'modelling and simulation' chapters [4], [20]–[23]. In the 2009 edition[1], the ITRS furthermore predicted that:

> *'Flexible electronics is projected to grow into a multibillion-dollar industry over the next decade and will revolutionize our view of electronics. […] Flexible electronics will enable a broad range of devices and applications not possible today.'[20]*

Challenges related to this field are also present in modelling, where developments in *'dynamic simulation of mechanical problems of flexible substrates and packages'* are required [4]. This is furthermore detailed in the SiP White Paper published with the 2011 edition of the ITRS, in the mechanical simulation tools requirements section [5]:

> *'The incorporation of different devices and materials which present varying heat load, unmatched CTE, different thermal conductivity and a variety of elastic properties results in a complex structure. These structures have dynamic response to mechanical stimuli which may come from changing temperature; vibration in the environment, externally applied forces, etc. Simulation tools that can predict SiP package mechanical behavior are essential to determine if the design requirements are met before fabricating a SiP.' [5]*

This interest in the 'More-than-Moore' trend has also been observed in private companies research [24].

1.1.1.1.4 Growing interest of organic electronics for smart objects

In addition to the will to add mechanical bendability to conventional electronic devices, the organic and printed electronics industry is also starting to look for increased performance

[1] The 'Assembly and Packaging' chapter of the ITRS 2011 Edition was under revision and not yet released when this manuscript was written.

and complexity [25]. Printed electronic systems tend to integrate several functions (as in conventional SiP) and will then require the use of high performance data processing components:

> *'A big advantage of organic and printed electronics is the possibility to combine and integrate multiple electronics devices to so-called smart objects. These will start with some simple functionality, like an animated logo, and constantly grow in complexity and size, enabling large area gameboards or flexible complex systems such as smart cards. The combinations are possible due to the new materials and processes used in organic and printed electronics. This allows the integration of different devices like sensors, transistors, memories, batteries or displays onto one substrate. The integration can be realized either by one process or by a hybrid combination of several separately produced devices.' [25]*

1.1.1.2 *Macroelectronics applications and perspectives*

1.1.1.2.1 The field of macroelectronics and its advantages

Macroelectronics, as first defined by Reuss *et al.*[7], describes the field of flexible and large area electronics. Thanks to the use of organic materials, this is often synonym to thin, light-weight, transparent, bendable, and/or stretchable devices fabricated at high throughput and low cost on large areas (using printing or roll-to-roll techniques for instance). However, current organic semiconductors feature limitations and the co-integration of thin inorganic materials on organic films proved to open the way to novel and promising applications in this field [7]. Indeed, smart and communicating systems, such as wireless sensor networks (WSN), biomedical, structure health, or environment monitoring systems require electrical performance that organic electronics cannot currently achieve. Fig. 1.3-a represents the inherent advantages and drawbacks of both nanoelectronics and macroelectronics. The realization of hybrid devices that could benefit from several advantages of both fields and outperform several of their drawbacks is the objective of this work.

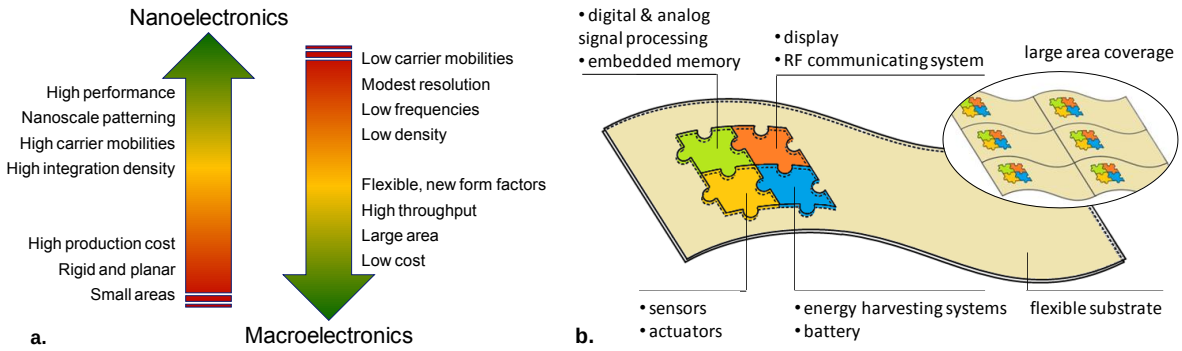


Fig. 1.3 – a. Chart showing the respective advantages and limitations of current nanoelectronic and macroelectronic fields, and b. Schematic of a fully flexible autonomous system integrating information processing and interaction with people and environment capabilities

Fig. 1.3-b presents a schematic representation of a system concept that could be fabricated by combining these two fields. This could result in an autonomous fully flexible system capable to record information from the environment thanks to the integration of various sensors. It could also process data and react accordingly by stimulating actuators, or transferring information via radio-frequency communication for instance. Energy required to power this concept device could also be harvested from the environment using photovoltaic cells, piezoelectric or thermoelectric units and stored in microbatteries embedded in the system. In this context of constant look for the integration of novel functionalities, the possibility to bend, fold, or stretch an electronic device opens new possibilities. Indeed, flexible systems can be conformed on curvilinear surfaces (e.g. the human body, or plane wings) to monitor or stimulate accurate locations on large areas. Next section will review recent developments in the field of high frequency flexible electronics.

1.1.1.2.2 Challenges related to handling of ultra-thin wafers

Before detailing recent progresses and high performance flexible devices that have been realized in the last few years, manufacturing challenges associated to the emergence of low cost, large area, flexible, and high performance devices will be highlighted. As stated before, special attention is currently focused on packaging various functionalities together on flexible films to reach the market of high performance flexible electronics. In addition, performance of organic film can be enhanced by using thin layers of inorganic materials. Developments of conventional semiconductor industry equipments are therefore required to cope with the integration of flexible films in process flow. In the meanwhile, mass-printing techniques used for organic and printed electronics are also studied to process novel semiconducting inorganic ink (featuring high charge carrier mobilities) with high resolution, as required for higher performance. Several roll-to-roll techniques are presented and compared in next section.

However devices reaching the level of performance required for radio frequency communication are currently based on conventional inorganic semiconductor industry. Therefore, there is an urgent need for industrial solutions regarding handling of ultra-thin wafers. Particularly in order to manufacture flexible electronic devices in conventional semiconductor foundries, numerous challenges associated with handling and processing of thin, flexible wafers have to be studied. These problems are common with various fields of the 'More-than-Moore' context requiring thinning and bonding of electronic dies (e.g. the three dimensions integration). Solutions suitable for manipulating micrometer-thinned devices at die-scale will be presented in the next chapter. However, it is important to highlight that these technological hurdles have been identified as '*critical'* in the 2009 edition[2] of the ITRS roadmap:

> *'For flows using wafer thinning before bonding, a robust thin wafer carrier process is required. [...] The temporary glue layers for this process are challenging and critical to the success of 3D-integration schemes. A complex combination of properties is required: Stability during processing with the capability of easy debonding. A wide variety of debonding mechanisms is being studied, such as laser-assisted (glass carriers), melting and*

[2] The 'Interconnect' chapter of the ITRS 2011 Edition was under revision and not yet released when this manuscript was written.

sliding (thermoplastic adhesives), dissolution in solvents, and mechanical debonding (peeling).' [21]

The 2011 edition of the ITRS roadmap also refers to the technological barriers of *'handling technologies for thin wafers'*, and the *'impact of different carrier materials'* as '*difficult challenges*'. [4]. A special interest is furthermore taken in *'flexible systems packaging'*, highlighting *'conformal low-cost organic substrates'*, *'small and thin die assembly'* and *'handling in low-cost operation'* as *'difficult challenges'*. Companies such as SÜSS MicroTech [26], [27], Dupont [28], [29], EVGroup [30], [31], IBM [32], [33] and several others are developing industrial solutions for low cost and reliable handling of ultra-thin wafers and conventional processing on these flexible wafers. These solutions are mostly based on novel adhesive materials that feature reliable bonding and debonding capabilities. Therefore, strong material related research in the adhesive and molding materials are needed:

'Molding compounds will need to support a wide range of applications from high performance stacked chips to flexible electronics, such as smart cards. With increased use of flip chip molding compounds will be needed to underfill the gap between the chip and substrate as well as encapsulating the chip, so viscosity in application and adhesion to all surfaces will be important. Innovation is also needed for materials with designed properties including flexibility to avoid cracking from bending stresses with thin silicon, compatible CTEs between silicon and the flexible substrate, and strong adhesion to IC materials. […]The grand challenge, as identified in the 2007 ITRS ERM chapter, is the concurrent requirements of achieving low CTE, low modulus, high fracture toughness, high adhesion, and lower moisture absorption.' [22]

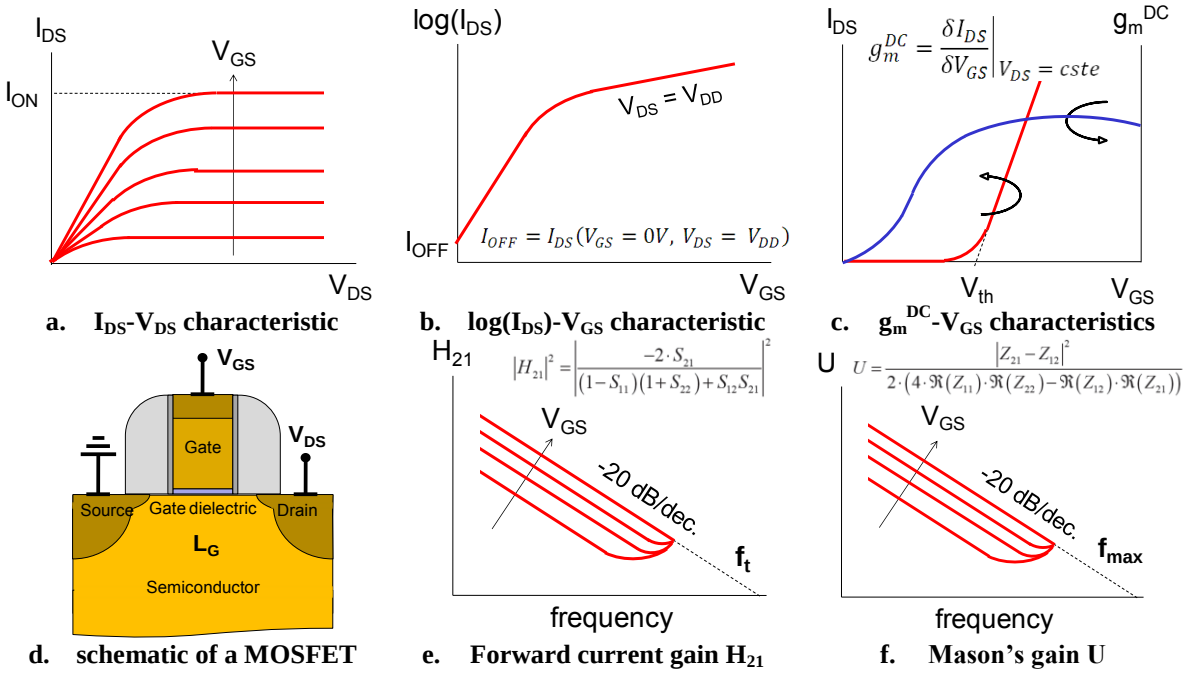
In conclusion, an increased interest in problematics related to flexibility, or bendability of high performance electronic components can be observed both from academic and industrial research communities.

1.1.1.2.3 Prospective applications

Several devices based on the integration on plastic films of poly- or mono-crystalline silicon, compound semiconductors, carbon nanotubes, or graphene demonstrated flexible transistors featuring cut-off frequencies in the GHz range [10]–[14], [16], [17], [34]–[37]. Numerous applications based on this organic/inorganic hybridation have been reported, leading to promising applications in the biomedial field [38], [39], for WSN, and/or embedded electronics. Previous section demonstrated the existence of high market expectations for such devices. Aspects related to fabrication of high performance flexible electronics will be reviewed and discussed in subsequent sections.

1.1.2 Recent realizations of high performance flexible devices

In order to realize devices and circuits combining high electrical performance with high mechanical bendability, numerous fabrication strategies have been developed during the last decades. Depending on the targeted applications market, various electrical and mechanical properties are required. In this work the objective is the realization of high frequency flexible electronics. The review of existing flexible transistor technologies will therefore focus on several geometric, static and high frequency figures-of-merit (Fig. 1.4), namely i) the transistor gate length L_G, ii) on-state current I_{ON}, off-state leakage current I_{OFF}, and on/off currents ratio, iii) static transconductance g_m^{DC}, iv) charge carrier mobility µ, v) current gain cut-off frequency, f_T, and vi) maximum oscillation frequency f_{max}. Physics of semiconductor devices can easily be found in textbooks [40]. It will therefore not be repeated in this document. However, Fig. 1.4 succinctly describes the figures-of-merit that will be used to evaluate and compare different technologies and devices in the following sections. More detailed information on these properties and methods to measure them is provided in paragraph 1.2, page 38, and in references [41], [42].



a. I_{DS}-V_{DS} characteristic **b. log(I_{DS})-V_{GS} characteristic** **c. g_m^{DC}-V_{GS} characteristics**

d. schematic of a MOSFET **e. Forward current gain H_{21}** **f. Mason's gain U**

Fig. 1.4 – Description of the geometric (gate length L_G), static (current ratio I_{ON}/I_{OFF}, transconductance g_m^{DC}) and high frequency (current gain cut-off frequency f_T and maximum oscillation frequency f_{max}) figures-of-merit required to describe and compare the various technologies and devices for the field of hogh performance flexible electronics.

Organic electronics will be considered as a starting point because organic semiconductors are intrinsically flexible materials. Higher frequency technology incorporating inorganic materials will then be reviewed and compared. Patterning of thin inorganic layers and transistor fabrication directly on an organic film allowed the realization of flexible and stretchable devices reaching 10 GHz [12], [13], [37]. In order to reach higher frequencies (e.g., the radio-frequency range), conventionally processed transistors (including several levels of back-end-of-line interconnection) have been fabricated on rigid semiconductor wafers prior to transfer on organic films. This allowed the field of flexible electronics to reach the 100 Ghz range [16], [17].

1.1.2.1 *Organic and printed electronics*

1.1.2.1.1 Inherent advantages of organic materials

Contrary to inorganic materials, organic semiconductors feature low Young's modulus (usually lower than 100 GPa). They have thus been considered as obvious candidates for the field of flexible electronics, giving rise to numerous mature applications. Organic photovoltaic cells [43], flexible displays, and lightning are the major application fields of organic electronics [25]. In addition, the fabrications techniques usually associated with these materials feature high throughput, low cost and high area coverage.

1.1.2.1.2 Comparison of mass printing technologies

Numerous different methods can be used for 'mass printing' [25]. Fig. 1.5, Fig. 1.6 and Fig. 1.7-a describe the working principle of the most common printing techniques, namely i) flexographic printing, ii) gravure printing, iii) offset printing, iv) screen printing, and v) inkjet printing. These techniques are foreseen to enable the fabrication of large area and low cost fully printed electronic devices, or in combination with conventional semiconductor industry techniques to increase performance of current printed electronics or lower manufacture cost of conventional electronics.

1.1.2.1.2.1 *Flexographic printing*

In flexographic printing (Fig. 1.5-a) the pattern of interest is defined in the raised areas of the plate cylinder, which is made of a soft and elastic material. Ink (represented in red in Fig. 1.5) is transferred from the ink fountain (or reservoir) to the plate cylinder via a donor cylinder, referred to as anilox cylinder, featuring dimples in its surface. A doctor blade in contact with the anilox cylinder removes the excess ink, ensuring a constant and controlled volume of ink deposited on the plate cylinder. The pattern is finally transferred to the substrate by passing it between a hard impression cylinder and the inked plate cylinder.

Flexographic printing allows the realization of patterns on various substrates (e.g. paper, glass, plastics) with various inks as long as no aggressive solvents are required (which results in wetting issues or swelling of the soft areas of the plate cylinder [25]). This technique enables rapid (50-500 $m.min^{-1}$) fabrication of printed devices with a resolution ranging from 30 to 75 µm [44]. Printing of thin layers is also possible (down to about 100nm) [25].

Organic thin-film transistors (OTFT) have been realized by flexographic printing, using pentacene as the organic semiconductor, poly(vinyl phenol) (PVP) for gate dielectric and conductive ink based on silver nanoparticles for source and drain electrodes [45], [46]. 16µm long OTFTs featuring mobility of 0.1 $cm^2.V^{-1}.s^{-1}$ and on/off ratio of 10^5 were demonstrated [46]. Selected recent results of mass-printed transistors and circuits are summarised and compared in Table A1.1 (Appendix 1).

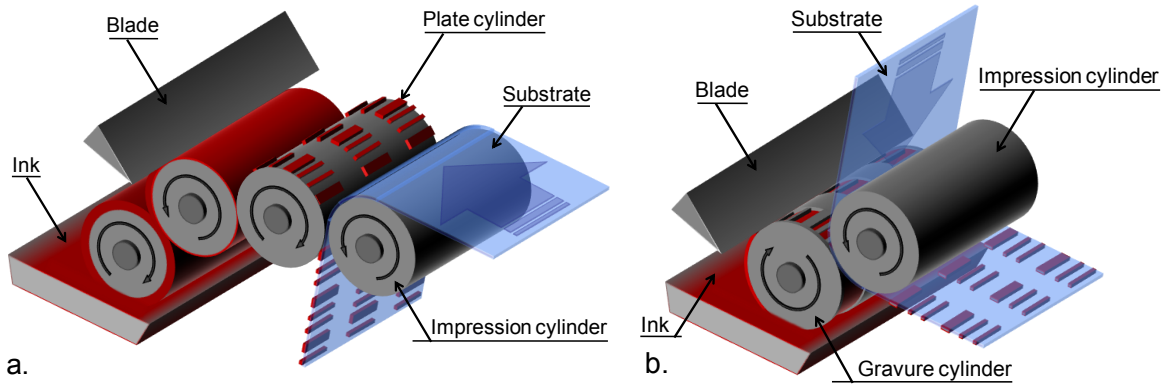


Fig. 1.5 – Schematic drawings of a. flexographic and b. gravure printing. Both methods require the use of a patterned cylinder (plate and gravure cylinders respectively) and an impression cylinder to transfer ink (represented in red) to the flexible substrate (light blue).

1.1.2.1.2.2 *Gravure printing*

Gravure printing, as shown in Fig. 1.5-b, requires the use of only two cylinders. Ink is first deposited on the gravure cylinder and excess is removed by the doctor blade, leaving ink only into the etched printing areas and wiping it from the non-printing areas. By contacting the substrate with the gravure cylinder, ink from the printing cells can be transferred to the film with high resolution (down to 10 µm). However reliable ink transfer requires a strong force applied by the impression cylinder on the substrate and a soft substrate material to ensure good contact between the film and gravure cylinder. Applying gravure printing to hard materials as glass is then more challenging than using it with plastic films or paper [25].

Organic field-effect transistors (OFET) and circuits were realized by gravure printing demonstrating high yield (75%) over large areas (50,000 transistors) [47]. Charge carrier mobilities ranging from 10^{-3} to about 1 $cm^2.V^{-1}.s^{-1}$, and on/off ratios of 10^2 to 10^5 were reported on fully printed p-type OFETs and OTFTs featuring gate lengths ranging from 10 to 100 µm [46]–[51]. Some of these works combine gravure printing with other mass-printing methods, as screen printing [48], offset printing [49], or inkjet printing [51]. 4 kHz 7-stages ring oscillators were also demonstrated by using only mass-printing techniques and print speed of 1 $m.s^{-1}$ [49]. Transition frequency of 300 kHz on OTFTs were measured using gravure printing to pattern the organic semiconductor and inkjet printing for the electrodes (silver nanoparticles ink) [51]. Gravure printing misalignment can be reduced to 15 µm with optimized parameters [52]. Selected recent results of mass-printed transistors and circuits are summarised and compared in Table A1.1 (Appendix 1).

1.1.2.1.2.3 *Offset printing*

Offset printing (Fig. 1.6-a) is one of the most widely used mass printing technique for graphical printing but is currently less common than flexography or gravure printing in printed electronics. This is due to the fact that this indirect printing method usually relies on a dampening fluid (water based) which may alter functional polymers [25], [44]. In contrast to flexographic or gravure printing, both printing and non-printing areas on the plate cylinder lie in the same level. Separation between them is solely due to wetting properties of the dampening and ink fluids on the plate cylinder. As a consequence, the volume of ink and dampening fluid deposited has to be directly controlled by more

complex ink and dampening fluid delivery systems (not represented in Fig. 1.6-a). However this method offers low resolution, high throughput, and low cost (Fig. 1.8-a).

Top-gate OFETs featuring a gate length of 50 µm were demonstrated using waterless offset printing of the source and drain electrodes, achieving charge carrier mobility of 3×10^{-3} $cm^2.V^{-1}.s^{-1}$ and on/off ratio of 10^3 [53]. Longer transistors and circuits were reported using both offset and gravure printing [49]. Selected recent results of mass-printed transistors and circuits are summarised and compared in Table A1.1 (Appendix 1).

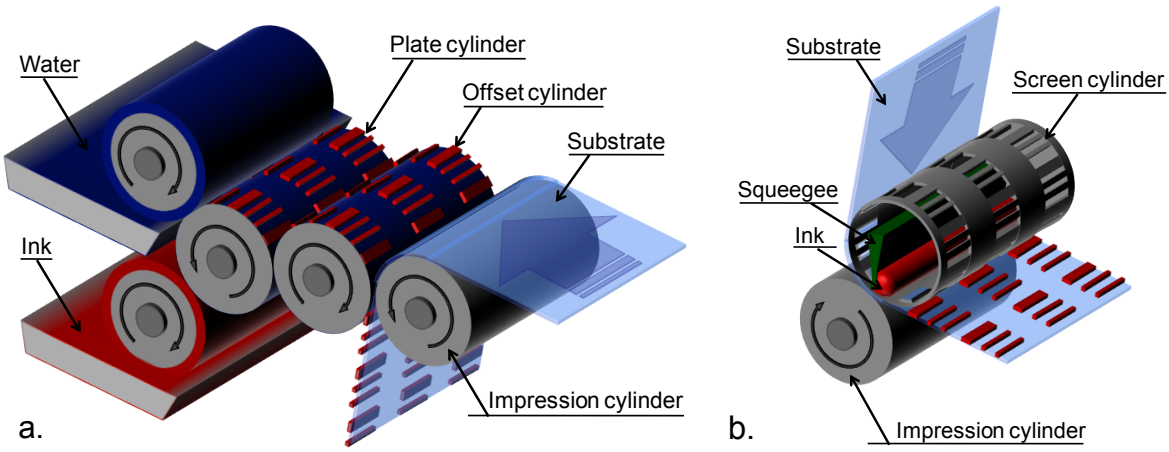


Fig. 1.6 – a. Schematic drawing of offset printing, where the dampening and ink fluids are represented respectively in dark blue and red. Thanks to different surface properties, the dampening fluid wet only non-printing areas of the plate cylinder, preventing ink to flow into them. Ink is then transferred to the offset cylinder and finally to the substrate (represented in light blue) b. Schematic drawing of rotary screen printing, where ink (red) is pushed over the surface of the screen cylinder and through opened printing-areas to the substrate by a squeegee (green).

1.1.2.1.2.4 *Rotary screen printing*

Another common mass printing method is rotary screen printing (Fig. 1.6-b). Here, ink is delivered to the substrate through a mask, or screen cylinder. Ink is spread over the screen surface and pushed through the open printing areas by a squeegee. Screen printing is a very suitable method that can be applied to numerous different substrate materials and shapes. Ink featuring high viscosity can be deposited with this method and relatively high thickness is achievable [54]. However, this method does not feature resolution and speed competitive with other techniques described hereinbefore (see Fig. 1.8-a and Table 1.1) and the roughness of the deposited ink layer can be relatively high [54].

Screen printing has been reported to fabricate top-gate p-type OFETs where source and drain electrodes were first patterned using laser ablation or conventional photolithography [48]. This work resulted in 50 µm long OFETs featuring carrier mobility of 3×10^{-2} $cm^2.V^{-1}.s^{-1}$ and on/off ratio of 10^5. Field effect transistors (FETs) were also fabricated on paper using screen printed semiconducting ink based on silicon nanoparticles and metallic source and drain electrodes with ink based on silver nanoparticles [55]. Selected recent results of mass-printed transistors and circuits are summarised and compared in Table A1.1 (Appendix 1).

1.1.2.1.2.5 *Inkjet printing*

Inkjet printing can be divided into two main categories: continuous inkjet and drop-on-demand (DOD). In continuous printing, a continuous stream of droplets is generated in the print head nozzle enabling high throughput whereas in DOD inkjet printing, droplets are ejected only when required by applying pressure pulse to ink. This pressure is generally applied by a thermal or piezo-element. Inket printers used in printed electronics usually rely on piezoelectric transducers [54]. DOD inkjet printing working principle is simple: ink stocked in the print head is propelled towards the substrate by a piezo-transducer as shown in Fig. 1.7-a. The ink droplet then wets the substrate and the deposited feature size depends on several parameters, namely the droplet volume, ink viscosity, nanoparticle size in ink, surface characteristics of the substrate, surface tension of ink, solvent evaporation, and deposition temperature. Inkjet printing enables the realization of fine structures, from 20 to 50 µm [44]. However, print speed rapidly drops with decreasing minimal feature size, i.e. increasing addressability (dot per inch, dpi) [25]. The major drawbacks of inkjet printing are the so called coffee stain effect, i.e. uneven drying of low viscosity ink resulting in a structure with most of the dried ink in the edge of the initial droplet [56] and the print head clogging that appears when using volatile solvent in ink formulation [25].

Inkjet printing of metal nanoparticles for source and drain electrodes, polymer gate dielectric and semiconducting polymer was reported to fully fabricate OFETs by inkjet printing [16], [57], [58]. This enables the realization of 15 µm long p-type OFETs featuring charge carrier mobility of 0.17 $cm^2.V^{-1}.s^{-1}$ and on/off ratio of 10^4 [58]. The subsequent thermal sintering of the metal nanoparticles by Ar ion laser furthermore results in finer features, down to 1.5 µm [16], [57]. This work demonstrated p-type OFET with charge carrier mobility of 2.10^{-3} $cm^2.V^{-1}.s^{-1}$ and on/off ratio of 10^4 [16]. Subfemtoliter inkjet printing enables the realization of metallic lines only 1 µm wide [59], [60]. Selected recent results of mass-printed transistors and circuits are summarised and compared in Table A1.1 (Appendix 1).

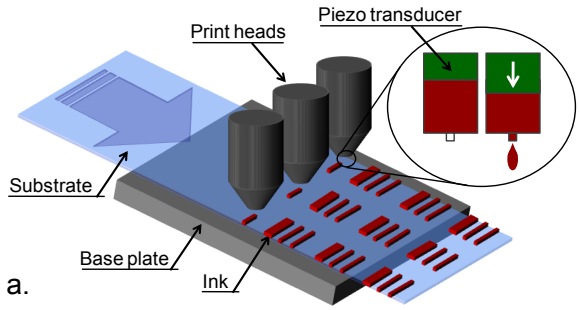


Fig. 1.7 – a. Schematic of inkjet printing, where ink stocked in print head is propelled toward the substrate by a piezo transducer [54].

1.1.2.1.2.6 *Other patterning methods*

Other patterning methods have been studied for mass-printing organic transistors: e.g. aerosol jet printing [61], xerographic printing, laser thermal transfer printing, pad transfer printing, hot stamping, nanoimprint lithography, laser processing, or roll-to-roll photolithography. However, these techniques currently feature low throughput when compared with mass-printing techniques presented in the previous sections.

1.1.2.1.2.7 *Comparison*

Mass printing methods presented in this chapter exhibit different advantages and drawbacks. Trade-off between print resolution and speed is presented in Fig. 1.8-a and Table 1.1. In order to realize high performance printed electronics, resolution below 1 µm should be achieved. Some academic work demonstrated micrometer scale resolution with mass printing techniques, especially inkjet printing [16], [57], [59] (see Table A1.1 in Appendix 1). However this has been done at laboratory scale without the print speed and high throughput usually expected from mass-printing methods. Important parameters, such as ink or substrate requirements for each mass printing techniques are also summarised in Table 1.1. Table A1.1 (Appendix 1) summarises important features of selected recent results reporting fabrication of organic transistors using mass-printing methods.

Table 1.1 – Summary and comparison of the resolution and print speed achievable with the more common mass printing techniques [25], [44], [47], [54]

Printing technique	Resolution µm	Speed m.min^{-1}	Comments	References
Flexographic printing	**30-75**	**50-500**	Various substrates, low ink viscosity, thin layers	**[25], [44]–[46]**
Gravure printing	**10-75**	**20-1000**	Simple process, smooth surface required	**[25], [44], [46], [47], [50], [62]**
Offset printing	**20-50**	**15-1000**	High ink viscosity required, presence of water	**[25], [44]**
Screen printing	**50-100**	**10-100**	High roughness, high ink thickness and viscosity achievable	**[25], [44]**
Inkjet printing	**20-50**	**1-100**	3D possible	**[25], [44]**

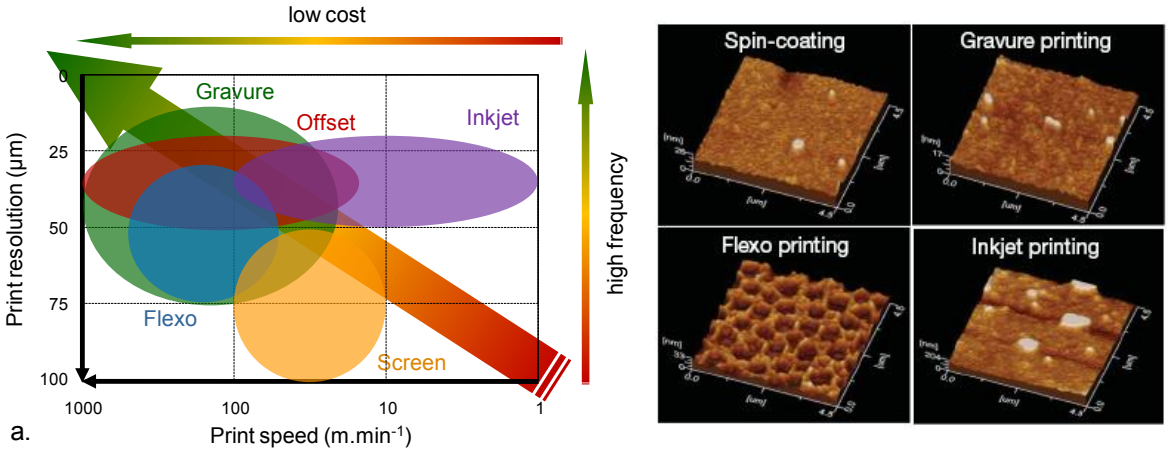


Fig. 1.8 – a. Trade-off between print resolution and print speed for the mass printing methods presented hereinbefore and b. Image reproduced from [50] showing AFM measurement of the surface quality after deposition using different printing techniques.

Fig. 1.8-b (reproduced from [50]) presents AFM[3] images comparing the surface of an organic layer deposited by various printing methods, namely spin-coating (as a reference), gravure, flexographic, and inkjet printing. Roughness of the deposited film is an important parameter that has to be taken into account when developing mass-printing processes. However, this is out of the scope of this work. Therefore, Fig. 1.8-b only highlights the fact that other aspects than only resolution and print speed have to be considered.

1.1.2.1.3 Limits towards the development of high frequency organic electronics

1.1.2.1.3.1 *Modest patterning resolution*

As presented in Fig. 1.8-a, Table 1.1, and Table A1.1 (Appendix 1), patterning resolutions achievable with current mass printing techniques are not competitive with methods used for conventional electronic processing, as photolithography for instance. In summary, conventional semiconductor industry achieve features at nanometer scale, whereas printed devices feature only micrometer dimensions. This limitation in terms of minimal achievable feature size is one of the arguments hindering organic electronics to reach higher frequencies.

1.1.2.1.3.2 *Modest charge carrier mobilities*

Carriers mobilities of current organic semiconductors (OSC) are typically two orders of magnitude lower than mobility of monocrystalline inorganic semiconductors [63]–[66]. For the sake of illustration, Fig. 1.9 presents the carriers mobilities of n- and p-type organic semiconductors achieved in the past three decades. It can be noticed in Fig. 1.9-b that n-type organic semiconductor are nowadays competitive with amorphous silicon in terms of charge carrier mobility, and p-type organic semiconductors almost feature mobilities in agreement with polycrystalline silicon (Fig. 1.9-a). The modest resolution achievable with mass printing methods (Fig. 1.8-a) in addition to modest carrier mobilities of organic semiconductors explains the limitations of organic transistors in terms of high frequency.

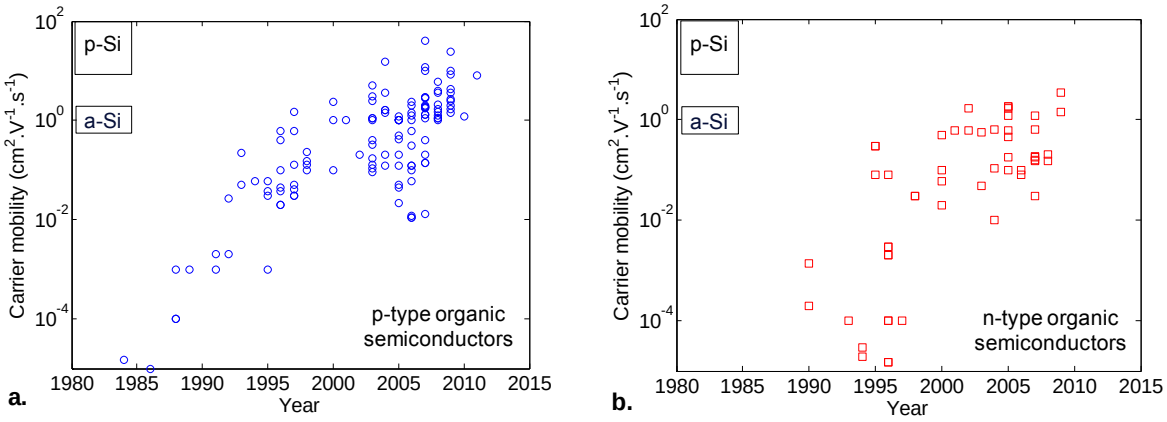


Fig. 1.9 – OSC mobilities for a. p-type, and b. n-type organic semiconductors for the past three decade demonstrating an exponential increase over time. Carrier mobilities of amorphous silicon (a-Si) and polycrystalline silicon (p-Si) are highlighted for easier comparison. Data from [63]–[66] and associated references.

[3] AFM: Atomic Force Microscope

1.1.2.1.4 Examples of organic electronic devices

In conclusion, organic electronics potentially offers high bendability, low cost and are processable with high throughput methods. However, the major drawbacks towards the realization of fully organic high frequency electronics are the modest charge carrier mobilities of organic semiconductors (especially n-type) and patterning resolution achievable with the manufacturing technologies hereinmentioned. Organic transistors have been demonstrated to operate under extreme bending conditions, i.e. even at bending radii in the milimeter range [8], [67], [68], down to 100 µm [8]. Organic transistors fabricated using mass-printing methods have been reported at a print speed close to 1 m/s [49], [51]. Fabrication methods involving various structures and geometries have also been used to decrease the channel length of organic transistors [68]–[71]. However highest reported cut-off frequencies are confined in the MHz range: below 20 MHz for most of them [9], [59], [68], [69], [71]–[74], with record performance of 28 MHz demonstrated on a 2 µm long fullerene C_{60} based thin-film transistor (TFT) biased at 25 V [9]. Selected recent results of high speed organic transistors are reported in Table A1. (Appendix 1).

1.1.2.2 *Organic/inorganic hybrid devices fabricated on organic foils*

In order to overcome limitations associated with current organic semiconductors while preserving the mechanical bendability it offers, flexible organic foils have been enriched with inorganic materials in ultra-thin regime [7], [13], [17]. The property of interest and main advantage of these inorganic materials is their high charge carrier mobility. Secondly, patterning these materials with conventional semiconductor industry fabrication techniques (e.g. electron-beam, or photolithography) allows the realization of devices with minimal features size several orders of magnitudes lower than what is achievable with low cost, mass printing techniques (Fig. 1.8-b). These two advantages offers the opportunity to increase the frequency capabilities of flexible transistors and circuits [10], [11], [13], [14], [16], [17], [34]–[37].

Two main strategies based on transfer of micro- or nano-structures of inorganic materials onto a flexible organic film have been reported. A common distinction between these two approaches can be made, as one is based on *'bottom-up'*[4] synthesis and the second one on *'top-down'*[5] fabrication of the micro- or nano-structures. The former combines the advantages of high carrier mobilities with large area and low cost fabrication by using inorganic semiconductors nanostructures (e.g. nanowires or nanotubes) chemically synthesized and then transferred on a plastic film. The separation of the high temperature fabrication process and the low temperature assembly in ordered network on flexible substrates enables the realization of high performance bendable devices [10], [51], [75]–[84]. The second approach that is reviewed in this section is the transfer of patterned inorganic thin films onto flexible foils. The joint use of monocrystalline semiconductors with nanoscale patterning techniques and reduced thickness enables the fabrication of GHz flexible devices [13], [14], [36], [37], [85].

[4] 'Bottom-up' approaches refer to methods involving the building of a complex assembly from smaller components (e.g. nanoparticles, nanotubes, or molecules)

[5] Conversely to 'bottom-up' approaches, 'top-down' strategies refer to methods where small (i.e. nanoscale) devices are fabricated using larger devices or equipments to pattern them (e.g. electron beam of photolithography)

1.1.2.2.1 Chemically synthesized high mobility nanostructures: a bottom-up approach to high performance flexible electronics

Semiconducting nanostructures can be synthesized with a variety of techniques. The most common strategy is based on chemical vapor deposition (CVD), and especially the vapor liquid solid (VLS) growth mechanism, developed to synthesize silicon nanowires in 1964 [86]. However, the chemical synthesis of inorganic nanowires is out of the scope of this work and has already been widely reviewed [87]–[89]. This section will focus on the integration and characterization of semiconducting nanostructures into high performance devices.

1.1.2.2.1.1 *Single nanowire, or nanotube transistors*

It has already been demonstrated that inorganic nanostructures synthesized by bottom-up mechanism feature high charge carrier mobilities and can be used for high performance nanoscale electronics [90]–[94]. Single nanowire, or nanotube transistors fabricated directly on (rigid) growth substrate demonstate charge carrier mobilities as high as 1×10^4 $cm^2.V^{-1}.s^{-1}$ for single walled carbon nanotube (SWCNT) [91], and 4.1×10^3 $cm^2.V^{-1}.s^{-1}$ for GaAs nanowire based field effect transistors [92] for instance. Novel core/shell (i.e. radial) heterostructure have also been reported to feature high charge carrier mobilities, e.g. 3.1×10^3 $cm^2.V^{-1}.s^{-1}$ for GaN/AlN/AlGaN [93], and 1.2×10^4 $cm^2.V^{-1}.s^{-1}$ for InAs/InP [94] radial nanowire heterostructure transistors.

Chemically synthesized nanostructures can also be assembled at low temperature into high performance devices [77], [95]–[100]. This is often performed by detaching the nanostructures from their growth substrate and dispersing them in appropriate solvent. Post synthesis suspension in solution and subsequent device fabrication offers an attractive alternative due to the fact that it can be entirely performed at room temperature. This enabled the integration of high mobility nanostructures on organic substrates. However, the intrinsic electrical properties of nanostructures can be degraded due to the use of solution processing techniques (e.g. sonification, purification, or sorting) [98]. As a results, solution based devices generally exhibit lower mobilities than achievable on the growth substrate.

Individual nanowire, or nanotube transistors from solution based chemically synthesized nanostructures featuring high field effect mobility have been reported using both top and back gate geometries (as presented in Fig. 1.10-a and Fig. 1.10-b). Furthermore, several different inorganic materials have also been synthesized, then suspended in solution and subsequently assembled at low temperature into single nanowire transistors, demonstrating for instance hole mobilities of 3.3×10^2 $cm^2.V^{-1}.s^{-1}$ [101], and 3.7×10^2 $cm^2.V^{-1}.s^{-1}$ for Si nanowire [82], 6.6×10^3 $cm^2.V^{-1}.s^{-1}$ for InAs nanowire [95], 4.1×10^3 $cm^2.V^{-1}.s^{-1}$ for ZnO nanowire [97], 1.4×10^3 $cm^2.V^{-1}.s^{-1}$ for SWCNT [98], and electron mobility of 2.6×10^3 $cm^2.V^{-1}.s^{-1}$ for As-doped In_2O_3 nanowire [99], and 7.3×10^2 $cm^2.V^{-1}.s^{-1}$ for Ge/Si core/shell heterostructure [100].

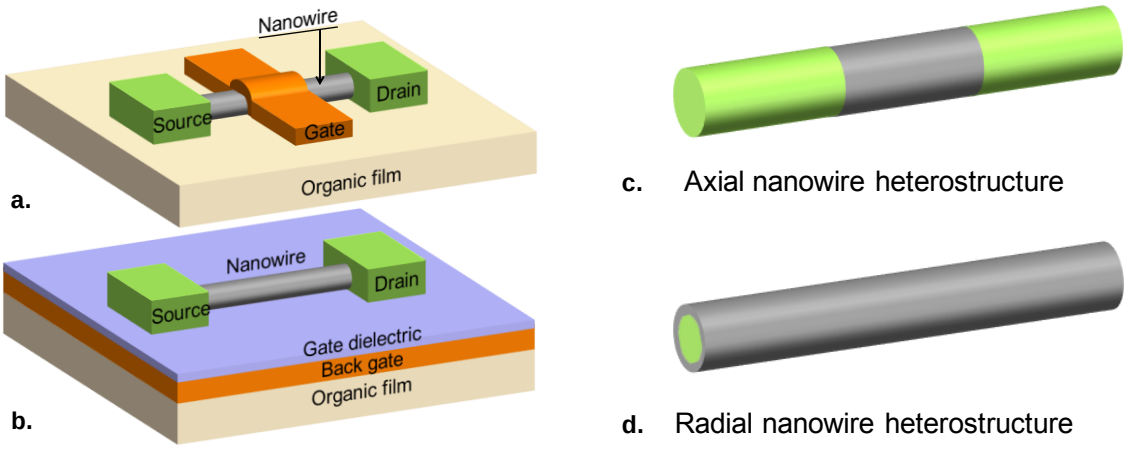


Fig. 1.10 – Schematics of nanowire based transistors on organic substrate (same geometry can be used on rigid substrate): a. Single nanowire (or nanotube) transistor with top gate geometry (the gate dielectric between the nanowire and the gate electode is not represented here) [95], [100], [101], b. Single nanowire (or nanotube) transistor with bottom gate geometry [82], [96]–[99], [101]. And schematics of nanowire heterostructures featuring an interface c. perpendicular [89], [101], and d. parallel [89], [93], [94], [100] to the nanowire axis (i.e. respectively axial and radias nanowire heterostructures).

1.1.2.2.1.2 *Limitations of single nanowire transistors*

Individual nanowire devices feature low current capabilities due to their limited gate width, i.e. nanostructure diameters. Indeed, high mobility devices reported hereinbefore feature ON current per wire in the order of 10 to 100 µA [93]–[96], [98]–[100]. Even if this means high scaled ON currents ranging from 2×10^{-2} to 5.3 mA/µm [82], [92]–[101], a maximum value of 1.2 mA has been reported for a single 250 nm large GaAs nanowire MESFET [92]. Similarly a maximum value for high mobility solution processed devices of 160 µA has been demonstrated for a 30 nm diameter As-doped In_20_3 transistor [99].

The first conclusion that can be drawn is the fact that optimized source and drain contacts are required to increase the available current output and thus achieve high performance single nanowire transistors [83]. Ohmic contacts to silicon nanowires have been reported without annealing step on organic films [82]. Otherwise, axial nanowire heterostructures (Fig. 1.10-c) [101] and core/shell heterostructures also demonstrated optimized contacts on rigid devices (Fig. 1.10-d) [100], [102]. Moreover, electrical characteristics can be altered due to the presence of interface states in the gate dielectric. The growth of high quality dielectric on organic film is therefore another important parameter. For instance, using a self-assembled dielectric instead of an ALD[6]-deposited Al_20_3 thin layer, As-doped In_20_3 nanowire transistors mobility has been enhanced from 1.5×10^3 up to 2.6×10^3 $cm^2.V^{-1}.s^{-1}$, ON current has also been improved from 60 to 160 µA, and on/off ratio decreased from 10^6 to 10^4 [99].

Finally, individual nanowire transistors realized from randomly dispersed nanowire networks are only proof of concept devices that demonstrate the potential of this approach but are not suitable for large area coverage [77]. After solution based deposition of randomly dispersed nanowires, a conventional lithography process is performed to define

[6] Atomic Layer Deposition

the source and drain electrodes which are subsequently realized by metal deposition and lift-off for instance [95]–[100]. In this approach the nanowire transistor location on the substrate highly depends on the random location of the chosen nanowire. In order to realize complex circuits or large area coverage of electronic systems, controlled orientation and interspacing of the nanowire devices are required [77].

As a result, network of numerous nanowires (or nanotubes) as a channel material could enable the fabrication of devices featuring higher ON current [90]. Furthermore, controlled orientation and interspacing of the deposited nanowires generally results in higher performance than randomly dispersed networks [76], [77].

1.1.2.2.1.3 *Randomly dispersed nanostructure networks*

As-deposited solution based random network of nanostructures can be used as the channel material of flexible transistors featuring high ON current (see Fig. 1.12-a and Fig. 1.12-b). Solution based inorganic nanostructures network has therefore been studied as a way to improve the performance of semiconducting ink used for mass printing fabrication methods [76], [103]. Nanowires and nanotubes – and especially carbon nanotubes (CNT) – have been used in dispersed solution to provide semiconducting ink featuring high carrier mobilities. However, several interdependent parameters have to be taken into account in addition to carrier mobilitiy, namely the nanotube density, the on/off ratio of the deposited network, and the presence of metallic nanotubes [103].

For a randomly dispersed network of semiconducting nanotubes, density directly contributes to mobility, as demonstrated in Fig. 1.11-a for two different gate lengths (L_G = 20 µm and 100 µm). It can also be noticed that due to the presence of metallic nanotubes and percolation effects, increasing the gate length results in an increase of mobility [103]. However, an increased nanotube density results in more short-circuits in the channel due to the presence of metallic nanotubes. This leads to a concomitant decrease of the on/off ratio (Fig. 1.11-b). This trade-off between mobility and on/off ratio is highlighted in Fig. 1.12-c for different grades of carbon nanotubes based inks [76].

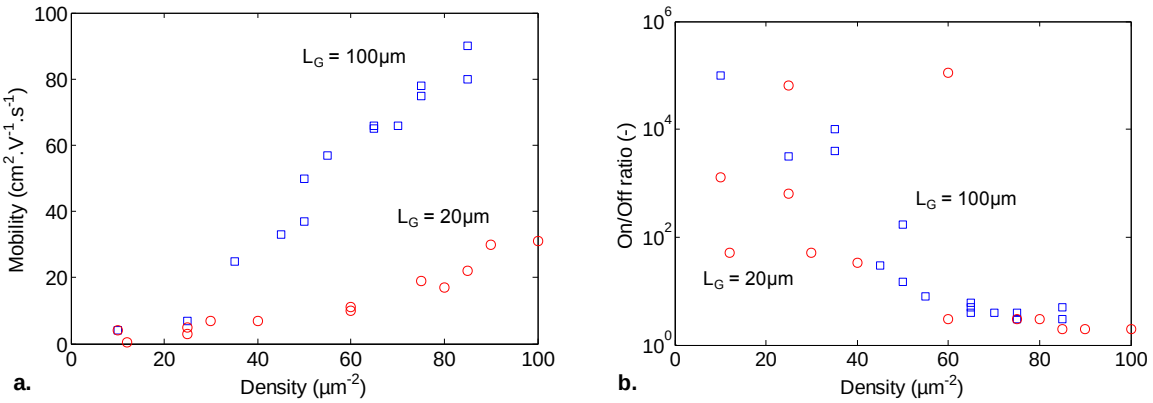


Fig. 1.11 – a. Charge carrier mobility, and b. on/off ratio of diluted carbon nanotubes as a function of their density demonstrating that a trade-off between high mobility (i.e. high density) and high on/off ratio (i.e. low density) has to be made (figures based on [103]).

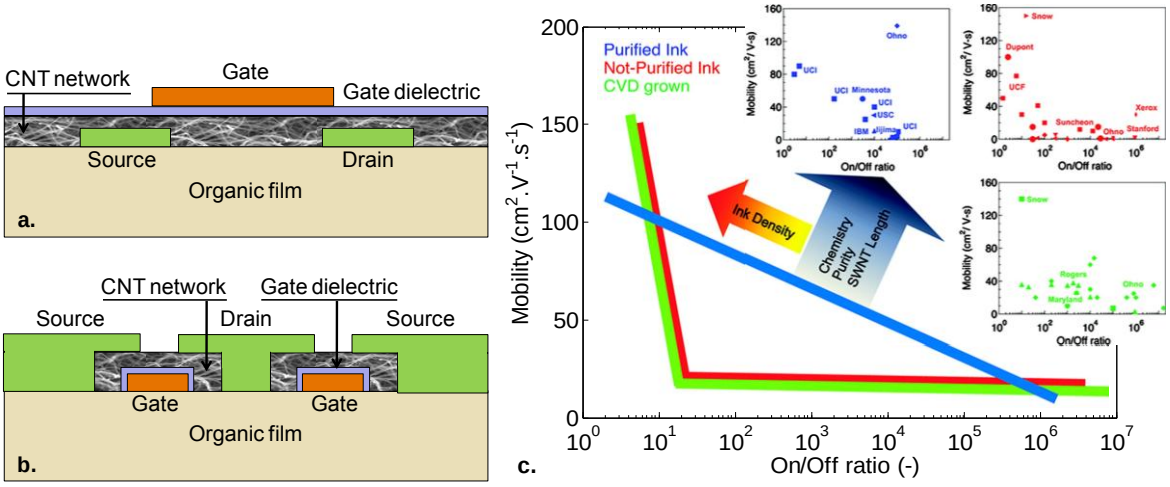


Fig. 1.12 – Schematics of a. top-gate [11], [34], [35], and b. bottom-gate [82], [104] (featuring two gate fingers) thin film transistor (TFT) based on randomly dispersed nanotube network on organic substrate (same geometries can be used on rigid substrate). c. Chart showing the trade-off between carrier mobility and on/off ratio for different CNT-based ink, in addition to solution suggested to enhance both properties: e.g. longer nanotubes, or higher purity (Image reproduced from [76]).

High performance thin film transistors (TFTs) based on carbon nanotube (CNT) networks have been reported [11], [34], [35]. 4 µm long top-gate TFTs featuring a calculated carrier mobility of 4.8×10^4 $cm^2.V^{-1}.s^{-1}$ [34], ON currents above 20 mA [34], [35] and operation frequency of 150 MHz [34] and 312 MHz [35] have been demonstrated on flexible films. However, as shown in Fig. 1.11 and Fig. 1.12-b, the choice that has been done in this work to increase density (> 1000 CNTs/μm^2) results in a poor on/off ratio of only 1.4 [35]. Randomly deposited CNTs network also enabled the fabrication of 4 µm long bottom-gate flexible TFTs featuring a cut-off frequency of 170 MHz and a maximum oscillation frequency of 120 MHz [79]. In contrast to solution based processing, dry transfer stamp-printing on polyimide (PI) film also led to the realization of flexible TFTs based on randomly oriented SWCNTs networks [80]. Mobility of 80 $cm^2.V^{-1}.s^{-1}$ and on/off ratio of 10^5 have been reported, in addition to integrated digital circuits composed of 100 transistors [80]. Stamp printing results in the transfer of CNT networks from random, to perfectly aligned orientations, along with crossed layouts [81].

CNT-TFTs completely fabricated by inkjet printing on a flexible organic (polyimide) substrate and featuring an operating frequency of 5 GHz have also been reported [11]. Source and drain electrodes were first printed using silver nanoparticles ink. An ultrapure, high density (> 1000 CNTs/μm^2) randomly aligned CNT network was subsequently printed (by repeating the printing process several times to obtain an uniform layer). Finally, the gate dielectric and gate electrode were patterned also using inkjet printing. The resulting TFT feature a high ON current and on/off ratio of respectively 221 µA and 1.4×10^2, in addition to an operation frequency of 5 GHz [11]. Selected recent results of bottom-up nanostructure-based high performance transistors are reported in Table A1. (Appendix 1).

Ordered assembly of nanowires, or nanotubes opens another way to achieve high performance devices other than randomly aligned networks [77].The reason is that drain current can be enhanced by aligning nanotubes network, especially in short-channel devices [105]. Long channel devices drain current increases as alignment is improved only up to a certain limit. This value corresponds to the minimal average path length from source to drain. Increasing alignement above this threshold reduce the number of

connecting paths and thus degrade the output current [105]. Furthermore, random nanowire orientations results in degraded transistor performance and uniformity, as crossing nanowires can degrade the gate electrostatic coupling and thus impact the switching properties of the nanowire transistor [106]. Therefore, assembly of ordered nanowires with controlled orientation and spacing is an alternative for large area alectronics and have been widely studied [76], [77], [83].

1.1.2.2.1.4 *Various nanostructures assembly methods*

Various assembly methods have been developed to provide controlled alignment of nanowires network [76], [77], [83], [89], [107]. The most common techniques are flow directed alignement (Fig. 1.13-a) [82], [108], [109], Langmuir-Blodgett method (Fig. 1.13-b) [110]–[115], electric field assisted alignement (Fig. 1.14-a) [116]–[118], bubble-blown techniques (Fig. 1.14-b) [119], [120], contact printing (Fig. 1.15-a) [78], [96], [121], [122], differential roll printing (Fig. 1.15-b) [123], stamp printing (Fig. 1.16) [124]–[126], strain-release assembly (Fig. 1.17-a) [127], and use of a sacrificial layer and spin-coated film (Fig. 1.17-b) [128]. Nanostructures can be ordered in parallel arrays using shear forces [107]. Numerous different techniques have been developed to generate and control forces mainly by moving a fluid on a solid surface (e.g. spin-coating, droplet evaporation, or flow assisted alignement), or by sliding two solid surfaces on each other (e.g. contact printing, or differential roll printing).

Chemically synthesized nanostructures dispersed in solution can easily be deposited in ordered networks by spin-coating [129], [130], or by evaporating a droplet containing nanowires on the surface of a sample [131], [132]. However spin-assisted alignment results in radial orientiations only and evaporation based deposition generates ordered arrays parallel to the fluid flow (i.e. perpendicular to the droplet contact line).

Encapsulating the fuild in microchannels – as used in microfluidic devices – enables to tune both the location and orientation of the nanowire network [82], [104], [108], [109], and provides better control over the deposition than the evaporation method for instance [107]. This flow directed technique is described in Fig. 1.13-a. In parallel to the synthesis and dispersion in appropriate solvent of the nanowires, a microfluidic channel is fabricated on the final substrate, defining the location and orientation of the nanowire devices. Dispersed nanowires are then pushed through the microchannel, and aligned nanowires are deposited on the sample surface. The resulting nanowire density can be controlled by selecting the solution concentration and the flow time. Furthermore, repeating this method in different sample orientations leads to the realization of complex crossed networks [82], [108]. However, it should be mentionned that this method is limited in terms of area coverage to the microchannel width and that achievable density is lower than for other methods [77].

Nanowires field effect transistors (NW FETs) based on chemically synthesized silicon nanowires assembled on a plastic film using flow directed aligment have been reported [82], [104]. After gate electrode patterning using conventional lithographic techniques [82] or nanoimprint [104], p-type silicon nanowires were dispersed in solution and aligned on the gate electrode. Conventional source and drain electrodes patterning was finally processed without annealing to define the NW FETs. Hole mobility of 3.7×10^{2} $cm^{2}.V^{-1}.s^{-1}$ has been demonstrated in addition to a 10^{5} on/off ratio, and normal operation down to a curvature radius of 3 mm [82]. Selected recent results of bottom-up nanostructure-based high performance transistors are reported in Table A1. (Appendix 1).

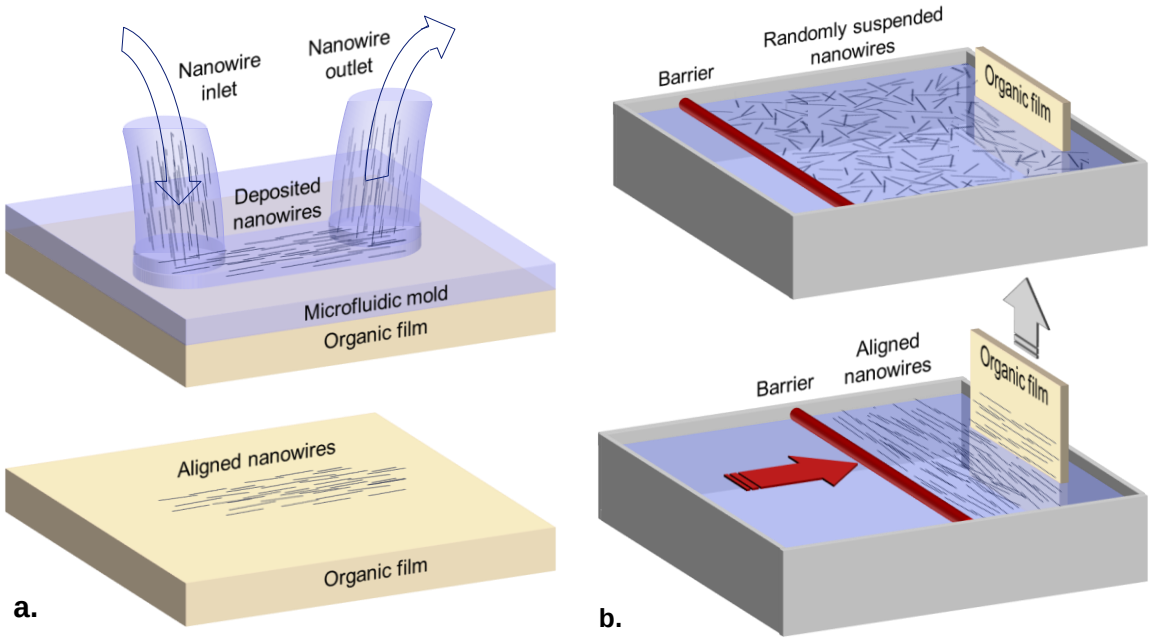


Fig. 1.13 – a. Flow directed alignement [82], [108], [109], where a microfluidic mold (in blue) is patterned on top of the organic film to provide a microfluidic channel for the nanowire containing solution to flow through. After removal of the microfluidic mold, this leads to aligned nanowire network at specific location on the substrate [82], [104]. And b. Langmuir-Blodgett method [110]–[115], where surfactant coated nanowires are dispersed on the surface of a fluid (usually water). Reducing the surface of this fluid by moving a barrier allows ordering nanowires into dense aligned networks. Finally withdrawing the sample from the Langmuir-Blodgett enable coating of its surface by aligned arrays of nanostructures.

The Langmuir-Blodgett technique enables the fabrication of aligned parallel and crossed nanowire networks over large areas with high achievable density [77], [113]. However, it requires the functionalization of the nanostructures with surfactant to prevent aggregation. After suspending surfactant coated nanostructures at the liquid-air interface in a Langmuir-Blodgett though (Fig. 1.13-b), the available surface is reduced by sliding the barrier (represented in red in Fig. 1.13-b). This movement compresses the randomly orientated nanostructure network. In order to minimize the surface energy nanowires are aligned in parallel arrays. This results in a dense network of aligned nanowires that can subsequently be transferred to an immerged sample by slowly pulling it from the liquid [110]–[115]. Rotating the sample and starting again this process can lead to crossed nanowire networks [111]. Similarly, the nanowire transfer from the liquid-air interface to the sample can be performed by positioning the sample surface horizontally (i.e. parallel to the fluid surface). This second method enables higher alignment uniformity in the deposited nanowire network [107], [115].

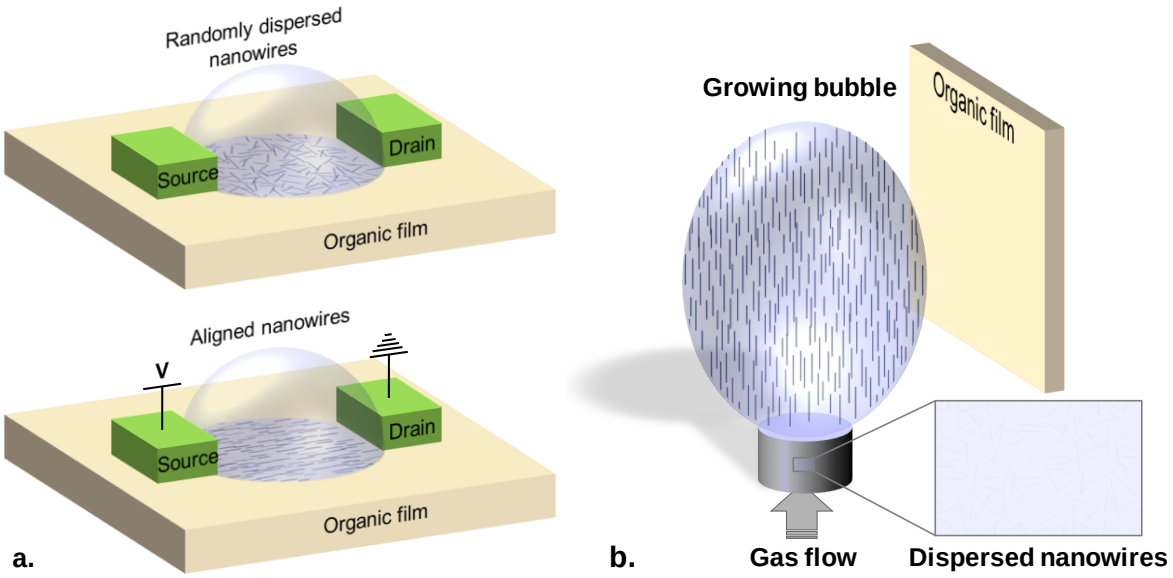


Fig. 1.14 – a. Electric field assisted alignment method, where nanowires in solution are deposited on the sample surface and aligned by generating an ac electric field between several patterned electrodes [116]–[118], [133], and b. Schematic of the three steps bubble-blown technique involving first stable dispersion of nanostructures in a polymer, then controlled formation and expansion of a bubble (or balloon) using a gas inlet at the bottom and a vertical pulling system at the top (not represented here), and finally transfer of the bubble film onto a sample by contacting it and collapse of the bublle [119], [120].

The bubble-blown technique schematically represented in Fig. 1.14-b has been used to assemble network of aligned nanostructures on various large area surfaces, including for instance conventional rigid wafers, flexible plastic sheets (up to 200×300 mm^2), or glass cylinders [119], [120]. This method is similar to a technique commonly used to manufacture plastic films [120]. The starting material is a stable polymer solution including the nanostructures of interest. The controlled formation and expansion of a bubble from this solution is performed using a gas inlet below the solution tank and a ring vertically pulling the top part of the balloon. This vertical pulling enables control over the bubble shape and by promoting one direction (vertical growing over lateral expansion), nanostructures alignement is better. As a result, during the bubble expansion step, the nanostructures dispersed in the solution are aligned along the upward expansion direction [120]. Contacting the final sample on the side of the bubble enables transfer of aligned nanowires. Field effect transistors have been fabricated using silicon nanowires transferred on a polyimide film by the bubble-blown method, demonstrating on current of 16 µA, on/off ratio of 10^5 in addition to good repeatability over 3600 transistors [119], [120].

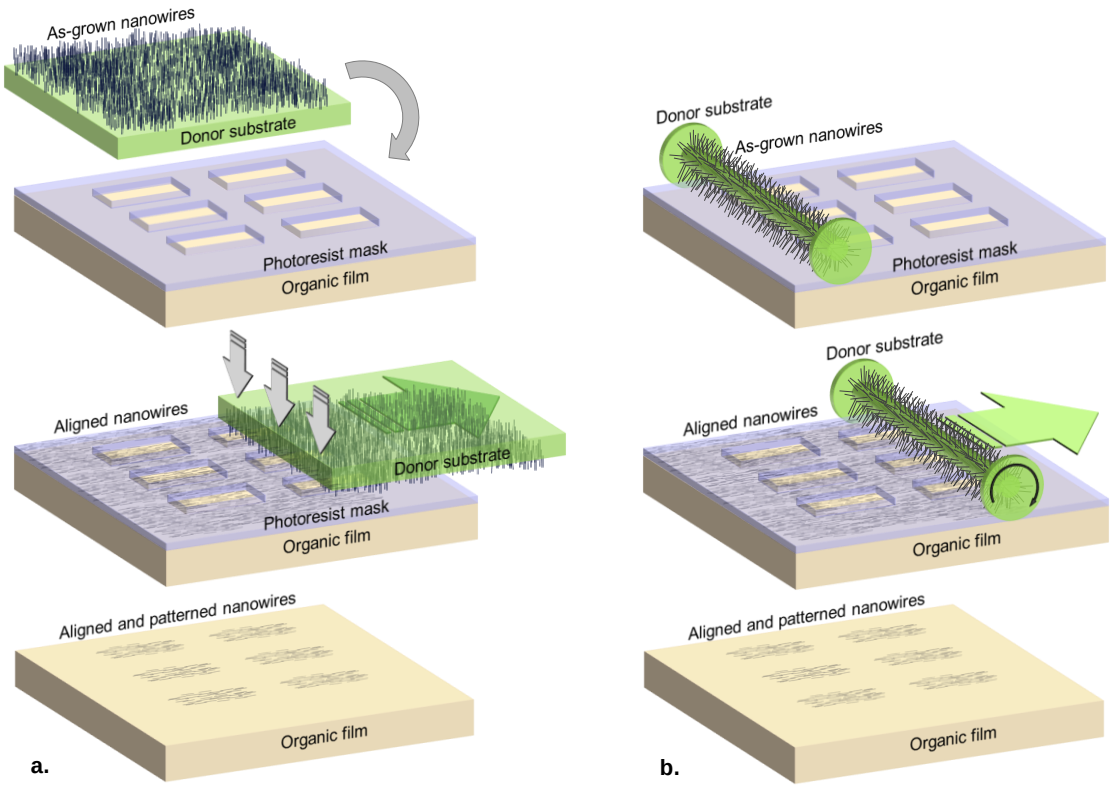


Fig. 1.15 – Contact printing of randomly grown vertical nanowires from a a. Planar [78], [96], [121], [122], and b. Cylindrical [123] growth substrate onto an organic film. In both cases sliding the growth (or donor) substrate surface on the acceptor sample results in a mechanical shear force that detaches nanowires from their initial substrate and aligns them on the final sample (e.g. an organic film). Patterning the acceptor substrate prior to nanowire transfer enable the lift-off of the unwanted areas. In differential roll printing (right), the growth substrate feature an inner cylinder (where nanowires are synthesized), and larger wheels at each end. Sliding of the cylindrical surface on the acceptor is provided by the fact that the movement is controlled by the large wheels rolling on a frame (not represented here).

Nanowire transfer can also be performed by dry contact printing between two solid surfaces. After chemical synthesis on a growth substrate, vertical nanowires can be transferred in aligned arrays onto a sample by sliding the growth substrate on top of the acceptor surface. The generated mechanical shear force detaches nanowires from their growth substrate and aligns them along the direction of the sliding force [77], [107], [121]–[123]. A planar [78], [96], [121], [122], or a cylindrical [123] growth (or donor) substrate can be used as schematically presented in Fig. 1.15-a, and Fig. 1.15-b respectively.

The density of the deposited network can be controlled by changing the chemical properties of the surface [121], and high density is achievable using this method [77] (bottom-up nanostructures assembly techniques are compared in Table 1.2). In addition to this printing process, a conventional lithography process can be used in order to position the aligned nanowire arrays on specific locations on the acceptor surface. This can be performed by a lift-off process (as presented in Fig. 1.15-a and Fig. 1.15-b), or by etching the unwanted areas.

Furthermore, crossed nanowire network can be realized by repeating this process [121]. Up to 10 stacked layers of Ge/Si core/shell nanowires FET fabricated using contact printing have been reported [122]. Nanowire field effect transistors fabricated on each of these ten

layers demonstrated transistor-like behaviour [122]. Finally, InAs nanowires transferred by contact printing method demonstrated 1.1 GHz of cut-off frequency and 1.8 GHz and maximum oscillation frequency transistors on a plastic film [78]. Selected recent results of bottom-up nanostructure-based high performance transistors are reported in Table A1. (Appendix 1).

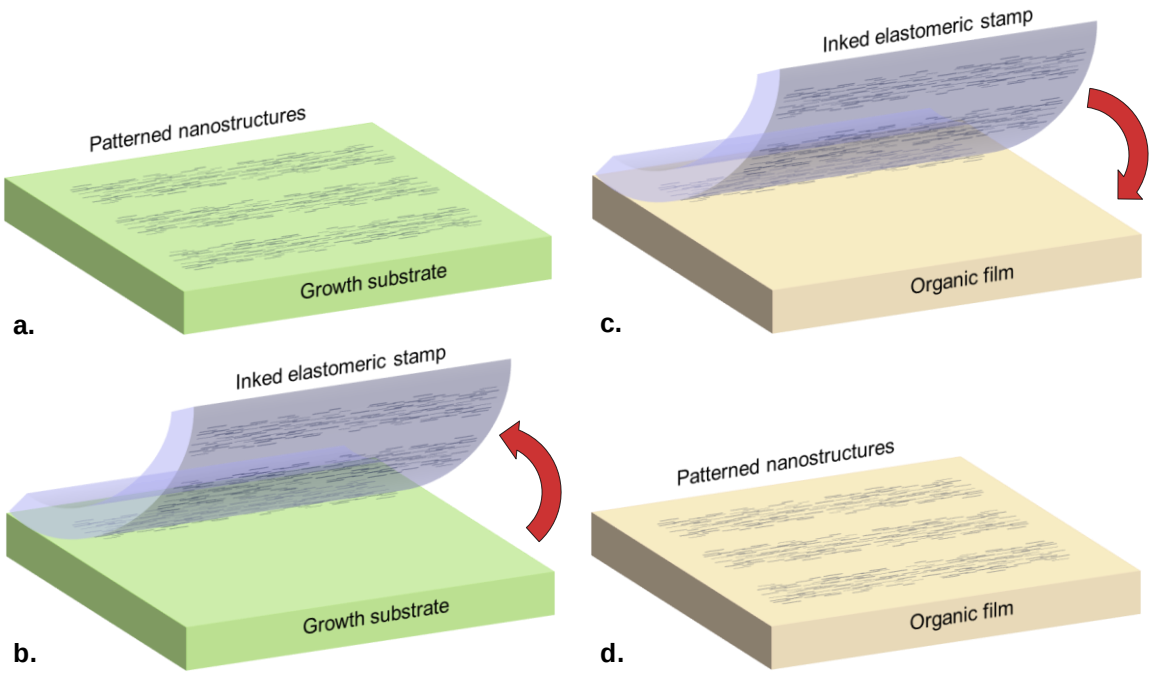


Fig. 1.16 – Dry stamp printing process. a. Nanostructures synthesis on a growth substrate and possible patterning (for bottom-up nanowires/nanotubes, or patterning for top-down micro or nanostructures). b. Release of the nanostructures from the initial substrate and transfer on a stamp. c-d. Transfer from the inked stamp onto the final application substrate [124]–[126].

Another contact printing method has been developed using an elastomeric stamp as a temporary carrier for the nanostructures of interest (Fig. 1.16). This technique is based on the fact that the adhesion to the elastomeric stamp is kinetically switchable [124]. This means that the stamp/nanostructures adhesion strength is speed-dependent and can be chosen higher or lower than the nanostructure/growth substrate bonding. Low peeling speed enables picking of the nanostructures from their growth substrate (i.e. stamp/nanostructures adhesion is higher than nanostructure/growth substrate adhesion). Conversely, at high peeling rate, the stamp/nanostructures adhesion becomes lower and nanostructures are printed on the final sample [124]. CNT networks have been transferred onto plastic films by stamp printing, demonstrating flexible TFTs with modest performance (charge carrier mobility of 17 $cm^2.V^{-1}.s^{-1}$, and on/off ratio of 10^3-10^4) but extreme bendability: normal operation down to curvature radii of 6 mm and level of current similar after extreme bending down to 50 µm [125].

The stamp by itself can also be used as the final flexible substrate (Fig. 1.16-a-b only). [126]. In this case, an adhesion layer can also be deposited on the stamp to increase the bonding strength to the nanostructures. Using a transparent stamp material and a curable adhesion layer enables to first contact the stamp to the nanostructure growth substrate and subsequently cure the adhesion layer. Transfer of multiple layers has been demonstrated

[126], resulting in transparent thin film transistors were all the active layers were made of random CNT networks (either metallic or semiconducting nanotubes) [126]. Selected recent results of bottom-up nanostructure-based high performance transistors are reported in Table A1. (Appendix 1). This method has also been intensively used to transfer top-down micro or nanostructures.

Fig. 1.17-a describes a technique used to improve nanowires network alignement and density. First nanostructures need to be transferred on a pre-stretched elastomeric sample, polydimethylsiloxane (PDMS) can be used for this application [127]. After deposition and alignement on this elastomer using one of the above mentioned techniques, the strain in the elastomer is released. This results in increased nanostructures density and better alignement [127]. Using the unstrained elastomer as an inked stamp for stamp printing (Fig. 1.16) onto a second pre-strained elastomer enables multiple uses of this method, successively increasing both density and alignement [127].

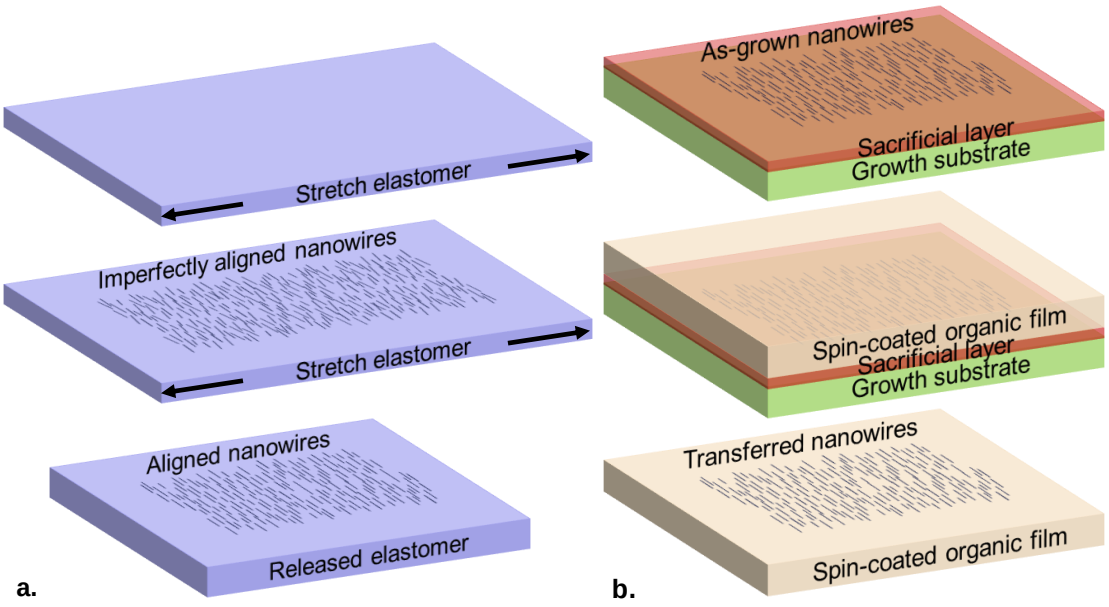


Fig. 1.17 – a. Strain-release assembly of nanowires [127], where nanostructures are first transferred onto a pre-stretch elastomer substrate by one of the above mentioned methods. The transfered network features a given degree of alignment that is then improved when the strain in the elastomer is released. Further transfer from this well-aligned network on another substrate is then possible, and b. Transfer technique based on a growth substrate featuring a sacrificial layer located below the synthesized nanostructures, and spin-coating of the final organic film on top of them. Dissolution of the sacrificial layer enables transfer onto the organic film [128].

The last transfer method presented in this section is based on a sacrificial layer and a spin-coated flexible film (Fig. 1.17-b). After the chemical synthesis of the nanowires on the growth substrate, a polymer is spin-coated, encapsulating the nanostructures. The presence of a sacrificial layer below the chemically synthesized nanowires network results in its easy release from the growth substrate and direct transfer onto the spin-coated film [128]. Flexible CNT FETs featuring a 12 $cm^2.V^{-1}.s^{-1}$ hole mobility fabricated by this method have been reported. Operation at high level of bendability was also demonstrated, with a reversible 12% decrease of conductance after bending on a 500 µm curvature radius [128].

1.1.2.2.1.5 *Comparison of the nanostructures assembly methods*

A comparison of the main properties of the above mentioned bottom-up nanostructures assembly techniques is presented in Table 1.2 and selected recent results of bottom-up nanostructure-based high performance transistors are reported in Table A1. (Appendix 1).

Table 1.2 – Summary and comparison of several properties of the common bottom-up nanostrucutres, (e.g. nanowire (NW), or nanotubes) assembly techniques presented hereinbefore, comparison mainly based on reference [77]

Methods	Area	Density	Speed	Crossed layout	Direct transfer	Comments	References
Fluid assisted	Limited by the channel patterning	Limited	Slow	Yes	No	-	**[82], [108], [109]**
Langmuir-Blodgett	Large	High density is achievable	Slow	Yes	No	Surfactant coated NWs	**[110]–[115]**
Electric field assisted	Limited by the electrode patterning	Limited	Fast	Yes	No	Electrode are required, but accurately position NWs Well suited for conductive NW	**[116]–[118]**
Bubble-blown	Large (tens of cm)	Limited	Slow	Yes	No	-	**[119], [120]**
Contact printing	Limited by the growth substrate	High density is achievable	Fast	Yes	Yes	Well suited for long NWs	**[78], [96], [121], [122]**
Differential roll printing	Limited by the growth substrate	High density is achievable	Fast	Yes	Yes	Requirements on the growth substrate shape	**[123]**
Stamp printing *	Limited by the growth substrate	High density is achievable	Fast	Yes	Both	The stamp can be used as the final substrate	**[124]–[126]**
Strain-release **	Large	Depends on first method	Fast	-	Both	Improves NWs alignment and density	**[127]**
Sacrificial layer	Limited by the growth substrate	High density is achievable	Fast	No	Yes	Sacrificial layer required	**[128]**

* this technique is also widely used to transfer top-down micro or nanostructures
** assembly techniques improving the NW alignement, requires the conjoint use of another trafer method

1.1.2.2.1.6 *Examples of bottom-up high performance flexible transistors*

Several high performance transistors and circuits based on deposition of chemically synthesized carbon nanotubes (CNT), or nanowires (NW) onto an organic substrate have been realized. The CNT, or NW network, which is the charge carrier layer, can be either randomly dispersed or aligned. The direct or indirect transfer of these active materials is performed by using one (or several) of the techniques presented hereinbefore. This led to the first demonstrations of flexible transistors with operation frequencies is the GHz range.

Most of the devices presented in this section are based on CNTs: 150 MHz [34], 170 MHz [79] and 320 MHz [35] operation frequencies have been reported using random CNT networks simply deposited in solution on a flexible organic film. High density inkjet printed randomly aligned CNTs resulted in the fabrication of a flexible TFT featuring a cut-off frequency f_T of 5 GHz [11]. Higher frequency was obtained using SWCNTs aligned by dielectrophoresis, demonstrating a FET with f_T = 8 GHz [10]. Recently, flexible transistors derived from solution-based graphene featuring f_T = 8.7 GHz have been reported [133].

In addition to CNT, InAs NWs were also used to fabricate high performance flexible transistors. Cut-off frenquency of 1.1 GHz in addition to maximum oscillation frequency of 1.8 GHz were then demonstrated [78]. These selected recent results of bottom-up nanostructure-based high performance transistors are reported in Table A1. (Appendix 1135).

1.1.2.2.2 Patterning and transfer of high mobility thin films: a top-down approach to high performance flexible electronics

In parallel to the development of the bottom-up approach to high performance flexible electronics, top-down strategies have been investigated as promising alternatives [12]–[14], [75], [134], [135].

1.1.2.2.2.1 *Lithographic fabrication of inorganic nanomembranes for flexible applications*

The first observation is that free standing inorganic thin films feature both the required level of mechanical bendability and the interesting electrical properties of monocrystalline materials as silicon, or III-V compound semiconductors [134]. Furthermore, even if chemically synthesized nanostructures can be produced in bulk quantities, top-down fabrication features some advantages [75].

First of all, bottom-up synthesis can lead to a broad distribution of nanostructure size, crystallographic orientations, and doping levels and methods to control the uniformity of these parameters benefit from less experience than techniques used conventionally in the semiconductor industry [75]. Indeed, lithographic and etching processes on single crystalline wafers result in the fabrication of well-controlled, reliable and uniform micro or nanoscale devices that can be used for flexible electronics [136], [137]. Secondly, assembling bottom-up nanostructures into perfectly aligned arrays or complex layouts can be challenging (see previous section). The joint use of lithographic processing of top-down nanostructures on rigid wafers with transfer printing that keeps their relative position and orientation enable higher level of alignment [75], [134], [136], [137].

In order to release the fabricated nanostructures, an embedded sacrificial layer is often used. Silicon-on-insulator (SOI) wafers for instance enable easy processing on the monocrystalline top layer and subsequent lift-off of patterned nanostructures by dissolution of the buried oxide layer (BOX) in concentrated hydrofluoridric acid (HF) [12], [13], [36], [37], [136], [138], [139]. This method even leads to the transfer on plastic film of strained

single crystal thin films, allowing flexible electronics to benefit from the advantages of strained silicon layers [139]. Otherwise, undercut can be performed below the nanostructures, facilitating the release from the initial substrate [14], [15], [140]–[142].

1.1.2.2.2.2 *Transferring inorganic nanomembranes on flexible organic films*

After fabrication, micro or nanostructures realized by top-down approaches on conventional rigid semiconducting wafers can be post-processed as their bottom-up counterparts using above-mentioned assembly techniques. Low temperature assembly of monocrystalline nanostructures on plastic films can be achieved using the same differentiation between the initial substrate (used to fabricate the elementary building blocks) and the final film (where the assembly and device patterning is realized). This results in high frequency (i.e. GHz range) flexible electronics based on nanomembranes [12]–[14].

Most of the work associated with the transfer of top-down nanostructures for high frequency flexible electronics focuses on the dry stamp printing technique (Fig. 1.16) [12]–[14], [36], [37], [136], [138], [140], [143], [144]. It has furthermore been demonstrated that using the stamp as the final substrate improves the printing resolution [12]. In this case direct flip transfer occurs from the donor substrate to the final 'stamp' substrate (Fig. 1.16 steps a and b only). Conversely, completing the stamping process by transferring the nanostructure from the stamp onto a second substrate is an indirect transfer method (Fig. 1.16 steps a to d). If the nanostructures can be flipped upside down without impact on the final device properties, the direct method is preferred as it enables higher printing resolution (± 0.5 µm, whereas complete stamping process results in ± 2 µm inaccuracy [12]). Three-dimensional assembly of various active layers have been reported using this stamping process on plastic [144].

1.1.2.2.2.3 *Examples of high performance top-down flexible transistors*

Carbon nanotubes are the major building blocks for bottom-up high performance flexible electronics (Table A1., Appendix 1). In top-down strategy, monocrystalline silicon is the most widely used material as it benefits from well developed and reliable techniques both on the wafer fabrication and nanostructure patterning points of view. Furthermore, GaAs thin films, also used for high performance flexible transistors [14], [140], [143], may prove to be too costly for large area applications [13]. Flexible thin film transistors (TFTs) based on silicon nanostructures featuring a current gain cut-off frequency of 515 MHz along with stable and reversible static properties (< 20% variation) when bent on a 3 mm curvature radius have been reported [36], [136]. Both tensile and compressive strains were applied to these devices to demonstrate their mechanical flexibility and robustness.

Metal semiconductor field effect transistors (MESFETs) based on GaAs NWs with ohmic contacts realized before transfer on plastic also demonstrated cut-off frequency of 1.55 GHz [14]. These flexible transistors furthermore feature less than 20% change in static electrical properties down to a curvature radius of 8 mm [140], [143].

Higher performance flexible TFTs were reported using similar lithographic patterning on SOI wafers and subsequent buried oxide etching before direct transfer (Fig. 1.16-a-b). Cut-off frequencies of 1.9 GHz and 2.04 GHz respectively associated to 3.1 GHz and 7.8 GHz maximum oscillation frequencies have been demonstrated [13], [37]. The enhanced performance is due to improved two-finger gate layout with minimized access resistances [13]. This technique recently resulted in 3.8 GHz of cut-off frequency and 12 GHz of maximum oscillation frequency [12]. In addition to high frequency operation, the reported transistors exhibit stable radio-frequency behavior after applying either tensile or

compressive strains. Constant frequency figures-of-merit have been demonstrated after bending down to a 29 mm curvature radius for tensile strain and 78 mm radius for compressive strain [12]. The up-to-date highest frequency ever reported for flexible transistors based on nanomembranes is (to our knowledge) 105 GHz [15]. This performance has been recently demonstrated on an InAs nanowire MOSFET using dry contact printing of InAs nanostructures on a 12 µm thick polyimide film previously spin-coated on a silicon wafer. Selected recent results of top-down nanostructure-based high performance flexible transistors are reported in Table A1. (Appendix 1).

1.1.2.2.3 Limits associated to fabrication on organic materials

Transferring nanostructures (chemically synthesized or conventionally patterned) onto plastic foils led to the fabrication of GHz flexible devices as presented hereinbefore. However, two major limitations inherent to post-deposition device patterning on flexible organic films have to be highlighted.

First, several fabrications steps are always directly performed on the organic substrate. For instance, the gate stack (and most of the time also source and drain electrodes) patterning for top-gate geometries [12]–[14], [36], [37], [140], and similarly source/drain electrodes deposition for bottom gate devices [138] are performed on the flexible film. The fact that these processes are done on an organic material therefore impedes the use of high thermal budget as can be required for contact silicidation, or dopant diffusion and activation for instance. The reason is that most of the polymers commonly used as substrates for flexible macroelectronics cannot withstand high (i.e. higher than ~200-300 °C) thermal budgets. Thermal properties of several polymers commonly used as substrate for flexible electronics are summarized in Table 1.3. Source and drain contact doping (required to reduce the source and drain contact resistances) are thus always performed on the initial rigid substrate, before transferring the nanostructures [12]–[14], [36], [37]. Self alignment, as conventionnaly used for shtort devices, is therefore not possible on flexible transistors. Furthermore, even a basic lithographic process involves photoresist backing at temperature close to 100°C, which results in slight deformation of the polymer film and induces misalignment [12], [13], [37].

Table 1.3 – Thermal properties of several polymers commonly used as substrates for flexible macroelectronics (data as given by common suppliers: Goodfellow [145], DuPont Teijin Films [146], and Dow Corning [147])

Polymer	Abbeviation	Upper working temperature	Coef. of thermal expansion	Thermal conductivity	References
		°C	10^{-6} K^{-1}	$W.m^{-1}.K^{-1}$	
Polyethylene terephthalate	**PET**	**105-170**	**20-80**	**0.15-0.4**	**[145], [146]**
Polyethylene naphthalate	**PEN**	**155-160**	**13-21**	**-**	**[145], [146]**
Polyimide	**PI**	**250-320**	**30-60**	**0.10-0.35**	**[145], [146]**
Polytetrafluoroethylene	**PTFE**	**180-260**	**100-160**	**0.25**	**[145], [146]**
Polydimethylsiloxane	**PDMS**	**-**	**310**	**0.16-0.2**	**[147]**

Values given at room temperature

Secondly, high frequency optimized layouts, as multi-finger gates transistors, and circuits require the fabrication of a high quality radio frequency interconnection networks on top of the transistor active layer. The presence of several gate fingers requires an interconnection network that increases in complexity with the desired number of gate fingers. Intense research is being performed, and promising progresses are being achieved on the field of flexible interconnects [148]–[154]. However, to our knowledge, no report has been made on radio-frequency behaviour of multilayer network of interconnection on a flexible film or flexible transistors fabricated on plastic featuring more than two gate fingers. Most of the work in flexible interconnects is currently focused on the reliability of mechanically bendable, or even stretchable, interconnections.

1.1.2.3 *Transfer of conventional inorganic electronic devices on organic films*

1.1.2.3.1 Flexible electronic property enhancement using mature fabrication technology

The two limitations due to thermal properties of organic films and lack of studies on high frequency properties of flexible interconnection networks fabricated is a serious hurdle for the realization of transistors featuring frequency figures-of-merit competitive with their industrial semiconductor based rigid counterparts. As a result, a novel strategy toward higher frequency flexible electronics has been developed. It involves three successive processes, namely i) the conventional fabrication of high performance RF transistors on a rigid substrate, ii) the thinning of the back-side of the fabrication substrate in the ultra-thin regime to obtain mechanical flexibility, and finally iii) the transfer and bonding of the thinned chip on an organic foil [16], [17], [155]–[157]. This complete differentiation between the fabrication substrate and the application (final) substrate allows the use of almost any type of devices featuring state-of-the-art performance on foldable foils.

1.1.2.3.2 General fabrication and transfer methodology

The conventional fabrication of high frequency transistors or circuits is out of the scope of this work. Several text books on radio-frequency design [158] and micro, and nanofabrication techniques [159] can be read for more information. It will be considered here (and hereinafter) that the fabrication process of flexible devices starts with high performance rigid devices coming out of an industrial clean room. The strategy is to provide mechanical bendability to this starting material by drastically reducing its thickness. The reason is that ultra-thin film can sustain higher deformation before reaching the breaking stress. In order to facilitate handling of this thin inorganic chip, a flexible foil is usually bonded as a replacement of the original substrate. Alternatively, the flexible thin film can be bonded on a rigid, but non-planar surface.

Numerous etching processes have been developed in the semiconductor industry for several applications. Dry processes based on plasma etching, wet etching in acid or basic solutions, and mechanical methods are available. Most of the published works in the field of flexible electronics report thinning processes based on several of the above-mentionned techniques [17], [155]. This allows to start with rapid, but rough techniques and finish the process with more gentle, slower and selective methods. In addition to provide better control on the final thickness, the combined use of several methods enhance the fracture strength of the thin device [160], [161].

Furthermore, electrical performance should be (as much as possible) unaltered by the back side etching and transfer to flexible foil processes. It has been demonstrated that back side grinding can be performed on CMOS chip down to the micrometer scale without

noticeable impact on the static electrical characteristics of transistors present on the front side [162]. Thinning processes are studied for the added flexibility but are also widely used for three-dimensionnal integration [162].

More information and references on these problems is provided in the first part of next chapter when detailing the fabrication methodology that has been developed in this work (see 2.1 General fabrication methodology).

1.1.2.3.3 Examples of high performance flexible devices: entering the 100-GHz range

High performance, i.e. high frequency and low noise, flexible electronics is mostly based on silicon MOSFETs as it is a relatively low cost and mature technology. Radio frequency transistors fabricated on rigid silicon wafer using conventional nanofabrication techniques, and radio-frequency optimized layouts, have been reduced to an ultra-thin film and transferred on plastic foils. 0.18 µm long MOSFETs featuring up to 32 gate fingers have been thinned down to 30 µm using plasma and wet etching and subsequently bonded on a PET (polyethylene terephthalate) film in 2005 [16], [163]–[165]. This is the first demonstration (to our knowledge) of industrial RF transistors on a plastic film, and set the state-of-the-art of this field at 48 GHz (59 GHz after the application of 0.7% of tensile strain in the longitudinal direction), in addition to 1.1 dB of minimal noise figure and 12 dB of associated gain [16], [163]–[165]. 0.13 µm long flexible MOSFETs were subsequently reported, featuring a cut-off frequency as high as 103 GHz (118 GHz after tensile bending) with 0.9 dB and 14 dB of minimal noise figure and associated gain respectively [17], [166], [167].

Flexible high performance transistors based on III-V compound semiconductors have also been reported recently [155], [168]. Demonstration of 120 GHz of cut-off frequency and 280 GHz of maximum oscillation frequency has recently been performed [168].

1.1.3 Summary and opportunities

1.1.3.1 *Summary of the recent progresses in the field of high frequency flexible electronics*

In order to realize components combining high electrical performance with high mechanical bendability, numerous fabrication strategies have been developed during the last decades (Fig. 1.18). Depending on the targeted applications market, various electrical and mechanical properties are required. In this work, the objective is the realization of high frequency flexible electronics. In this review of existing flexible technologies, the main focus has been laid on frequency figures–of-merit, such as the transistor current gain cut-off frequency f_T. Organic electronics have been considered as a starting point because organic semiconductors are intrinsically flexible materials (yellow area on Fig. 1.18) [59]. Higher frequency technologies incorporating inorganic materials embedded on plastic films were developed [10]–[14], [34]–[37]. Patterning of thin inorganic layers and transistor fabrication after transfer on an organic film has conducted to the realization of flexible and stretchable devices reaching 10 GHz (blue area on Fig. 1.18). In order to reach higher frequencies, conventionnaly processed transistors (including several levels of back-end-of-line interconnection) have been conventionally processed on rigid semiconductor (silicon) wafers prior to transfering on organic films (green area on Fig. 1.18). The field of flexible electronics thus reached the 100 Ghz range [16], [17].

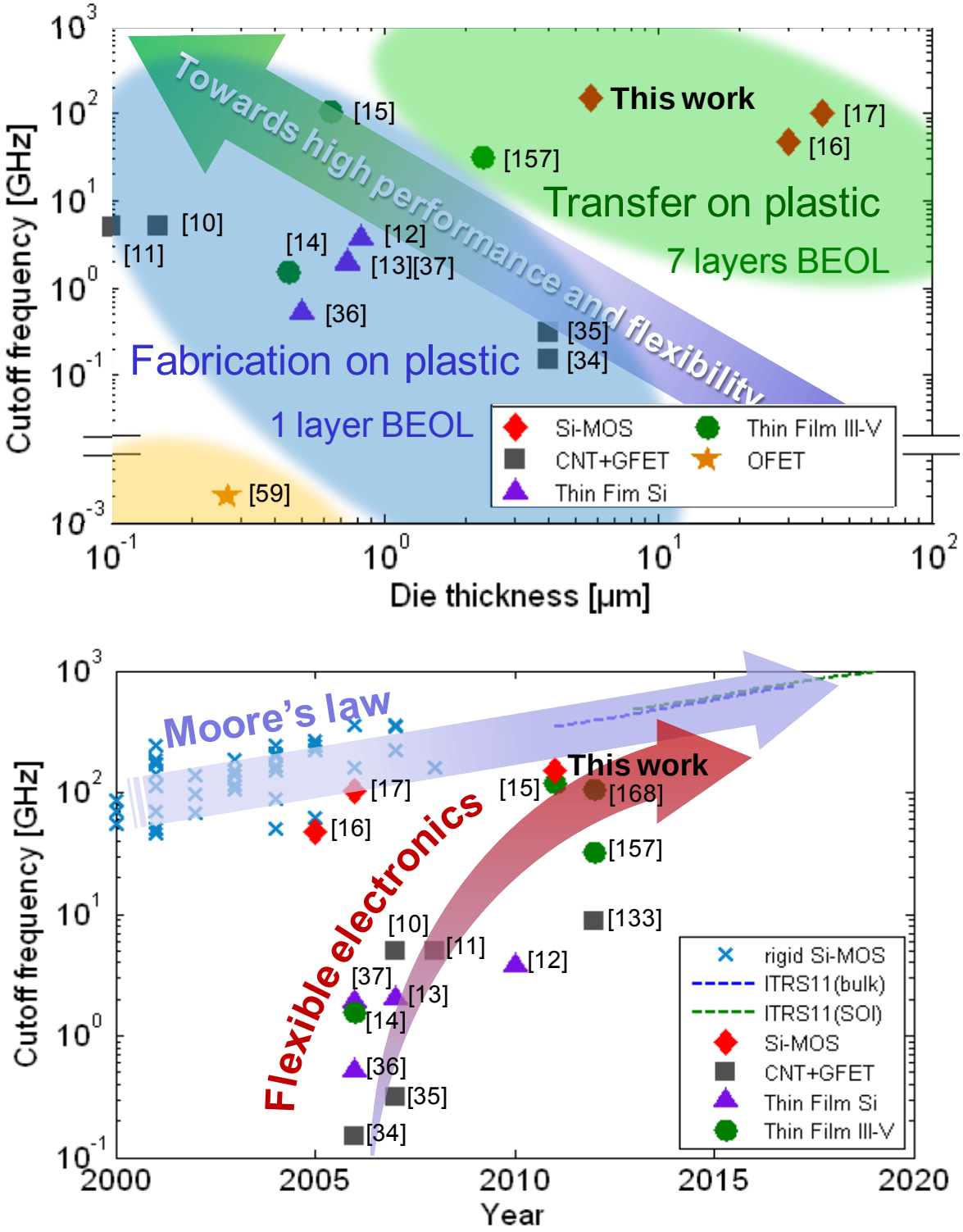


Fig. 1.18 – Charts showing the recent progress in the field of high performance flexible electronics by plotting the cut-off frequency of flexible transistors a. as a function of the thickness of the inorganic die (i.e., the major limitation in terms of mechanical flexibility), and b. as a function of time [10]–[17], [34]–[37], [59], [157]. (NB: two reported devices [133], [168] have not been added to the first graph for lack of data on the thickness of the flexible transistor).

1.1.3.1.1 Opportunities to increase state-of-the-art performance

The objective of the work described in the following chapters is to combine the potentials of a mature and reliable rigid technology with the promising opportunities of mechanical bendability. This has been conducted in partnership with STMicroelectronics.

A well-established 65 nm node CMOS technology on SOI has been chosen for this work (fully described and characterized in next part). The reasons are, i) its high frequency and low noise performance, ii) good understanding of its characterization and modelling, and finally iii) the presence of a buried oxide that helps the transfer on a plastic film.

The main objectives are therefore associated to several workpackages. First, a fabrication technique is required to transfer the RF-MOSFETs on a plastic film. The study of a transfer methodology and the results are presented in chapter 2 (see part 2.1 General fabrication methodology). Validation of this transfer process is then performed by electrical measurements on flexible devices on flat configuration (see part 2.2 Electrical performance of CMOS dies on organic films). Finally the impact of mechanical bending on the electrical performance of the CMOS chips is discussed in the last chapter. The final objective of this document is to unveil and characterize a methodology that combined high electrical performance, with mechanical bendability and stability of the electrical properties upon bending.

1.2 Potentialities of the SOI-RF CMOS 65nm technology for flexible electronics

1.2.1 Silicon-on-Insulator (SOI) technology

1.2.1.1 *SOI wafers*

Silicon-on-Insulator (SOI) technology refers to technology based on wafers featuring a top monocrystalline silicon layer above an insulating film, typically silicon dioxide. The handler, or back side of the wafer usually consists of a thick silicon substrate (Fig. 1.19-a) [169]. Numerous fabrication processes have been reported to fabricate wafers featuring a thin layer of monocrystalline silicon on top of an insulating layer (Fig. 1.19-a) [169], [170].

This top layer can either be produced by epitaxial lateral overgrowth (ELO) of silicon film locally seeded in openings of a silicon dioxide mask [171], recrystallized from a thin silicon layer using for instance laser recrystallisation [172], separated from the silicon handler by oxygen implantation [173], [174], or transferred from a bulk silicon wafer onto a second wafer, relying on wafer bonding [175]–[178]. Among the various SOI material fabrication strategies, three different methods have been widely used to produce SOI wafers during the last decades, namely the SIMOX (Separation by IMplantation of OXygen) [173], [174], BESOI (Bonded and Etch-back SOI) [175], [176], and Smart Cut [177], [178] processes. The former relies on directly implanting oxygen to form a buried oxide layer upon thermal annealing throught the top silicon layer, whereas the BESOI and Smart Cut processes relie on wafer bonding.

1.2.1.1.1 SIMOX process

In the SIMOX (Separation by IMplantation of OXygen) process, SOI structures are produced by implanting oxygen to create the BOX layer. In order to obtain enough oxygen at a given depth below the silicon surface, high dose is required. This results in a high degree of crystalline lattice damage in the top silicon layer, i.e. the SOI layer. The oxygen implantation is thus performed at high temperature (~600°C) in order to preserve the monocrystalline nature of the top silicon film. Finally the last step of this process is a very high temperature annealing occurring after implantation that enables the formation of SiO_2, and reduce the defect density in the silicon layers below and above the buried oxide [170], [175], [176].

1.2.1.1.2 BESOI process

The BESOI (Bonded and Etch-back SOI) fabrication process relies on bulk silicon wafer bonding and etching. The SOI layer thickness is controlled by the etching step. However, grinding, lapping, and polishing processes enable only SOI films thicker than ~10µm with acceptable thickness uniformity [170]. The introduction of a buried etch stop layer (e.g. by boron implantation) and a final selective etch step results in finer control on the SOI layer thickness uniformity [175], [176]. However, it is worth highlighting that this process requires two bulk silicon wafers to produce one SOI wafer.

1.2.1.1.3 Smart Cut process

The Smart Cut process from SOITEC (Fig. 1.19-b) leads to the production of SOI wafers featuring good thickness uniformity, in addition to good crystal quality of the top silicon layer at relatively low cost [177], [178].

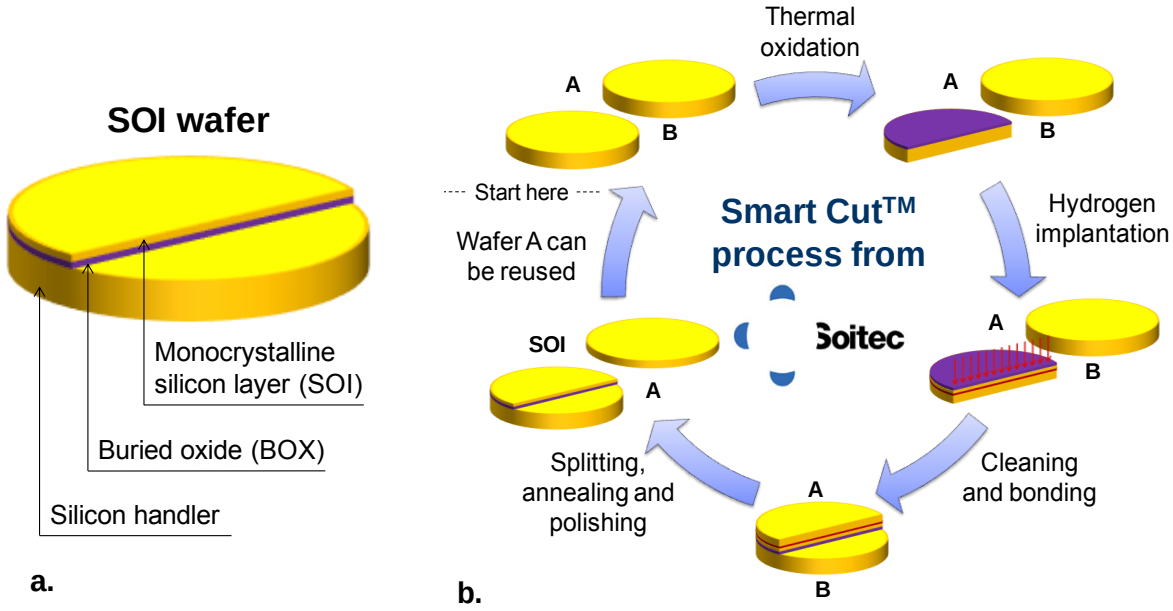


Fig. 1.19 – a. Schematic of a Silicon-on-Insulator (SOI) wafer, b. Schematic of the SOI fabrication process Smart Cut™ from SOITEC. Starting with two bulk silicon wafers A and B, a thermal oxide is first grown of wafer A, followed by the implantation of hydrogen at a chosen depth below the surface of wafer A to create a weakened layer. The two wafers are then bonded together, encapsulating the oxide layer between two silicon layers, wafer A is then separated from wafer B at the weakened layer. Wafer B finally undergoes thermal annealing and polishing, resulting in a SOI wafer, whereas wafer A can be reused [177], [178].

This process involves four main steps [177], [178], as shown in Fig. 1.19-b, namely i) ion implantation, ii) wafer bonding, iii) splitting by heating, and iv) fine polishing. The starting materials of this process are two conventional bluk silicon wafers. One of them, later referred to as wafer A, is first capped with an insulator layer – usually thermally grown silicon dioxide – and subsequently implanted with hydrogen ions. Both wafers are then cleaned in order to remove any organic residus, native oxide and metallic contaminants that may degrade the bonding quality. Wafers are subsequently brought into contact and hydrophilicly bonded together. The splitting process is then performed by applying a first thermal budget (400-600°C) to the bonded stack. Under annealing, the implanted protons induce blistering, i.e. creation of microcavities over the complete wafer surface. This enables in-depth splitting at the depth corresponding to the peak hydrogen concentration. This leads to the transfer of the capped oxide and a thin silicon layer of wafer A onto wafer B, giving rise to the so-called SOI structure. A second thermal annealing (~1100°C) enables to strengthen the chemical bond between the top surface of wafer B and the silicon dioxide layer of wafer A. However, the resulting SOI wafer exhibits microroughness that needs to be removed. A fine polishing is thus finally performed to conclude this process. Note that at the end of this fabrication process, the main part of wafer A can be used again as a starting material for another run. This process is today the dominant industrial technique to produce SOI wafers [179].

1.2.1.2 *SOI CMOS technology*

A comparison of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) on bulk and SOI technologies is schematically represented in Fig. 1.20-a to Fig. 1.20-c. SOI wafers feature a buried oxide layer (BOX) that provides vertical isolation between the top active silicon layer (also referred to as SOI) and the bulk silicon handler. Fig. 1.20-d and Fig. 1.20-e are transmission electron microscopy (TEM) images of SOI MOSFETs. Fig. 1.19-d shows only one gate finger with the source and drain doped areas, the gate oxide (hardly visible) and spacers around the gate stack, as schematically reprensented above. Fig. 1.20-e provides a larger view, showing several gate fingers and the first layer of metalisation providing contacts to the source and drain areas.

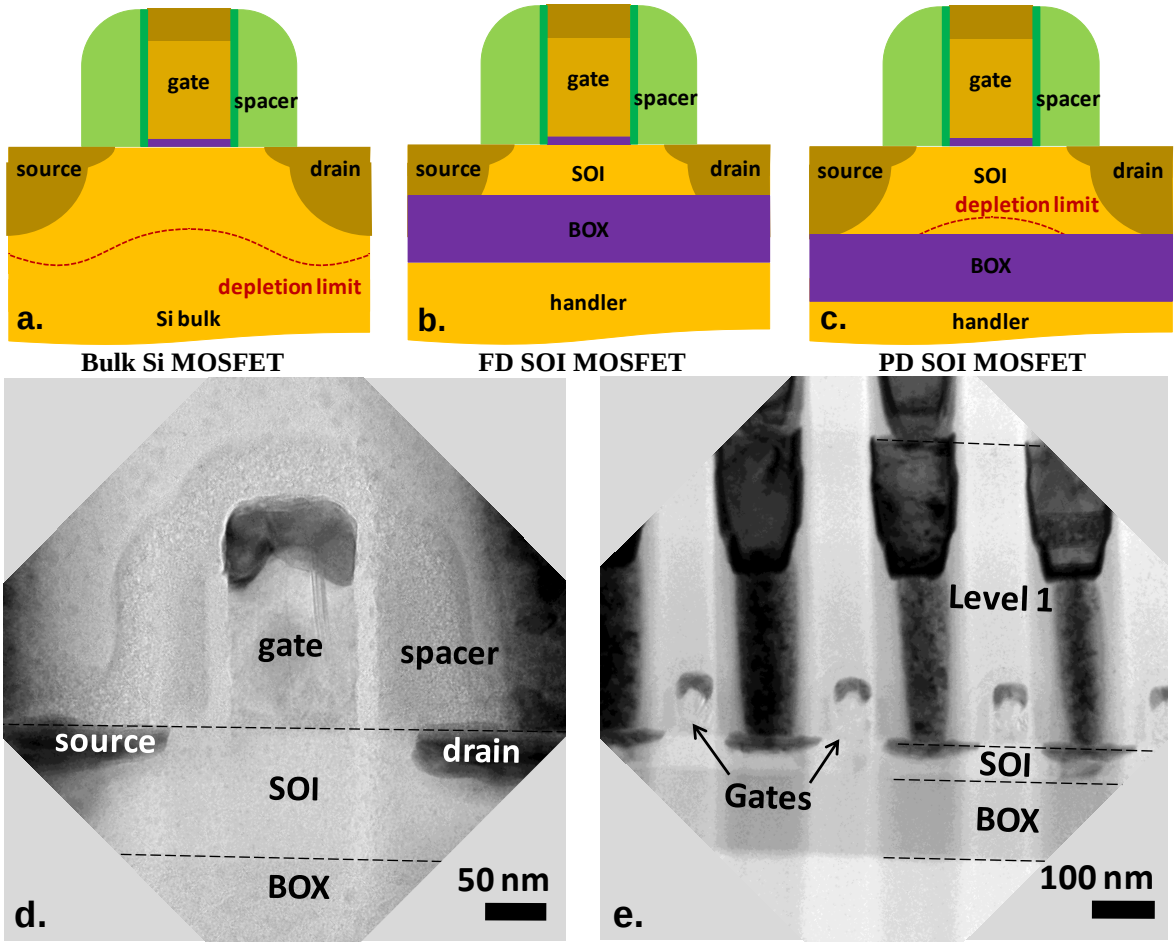


Fig. 1.20 – Schematics of a. a MOSFET on a bulk silicon wafer, b. a Fully Depleted (FD) MOSFET on a SOI wafer, c. a Partially Depleted (PD) MOSFET on a SOI wafer. Depletion areas are highlighted. d. TEM image of one gate finger of a FD SOI MOSFET, and e. TEM image of a larger view, showing several gate fingers of a FD SOI MOSFET.

In SOI technology, the top silicon layer can easily be tuned to provide fully depleted (FD), or partially depleted (PD) devices (Fig. 1.20-b and Fig. 1.20-c respectively). In PD SOI MOSFETs, the bottom part of the top silicon layer is not completely depleted. This body can therefore by contacted (or tied), or floating (more details and comparisons are provided in references [41], [42]).

1.2.1.2.1 Advantages of the SOI technology

SOI CMOS[7] technology features two important advantages over its bulk counterpart, namely a reduced number of processing steps, and an increased yield [169]. SOI technology also benefits from the buried oxide layer (Fig. 1.19-a) that provides enhanced resistance to parasitic effects, improved performance, reduced power consumption and greater integration density relative to bulk technology [42], [169], [170], [180].

1.2.1.2.1.1 *Improved resistance to parasitic effects*

SOI technology features several advantages over bulk silicon technology. First of all, the presence of a buried insulating layer improves resistance to parasitic effects usually observed in bulk technology. SOI processing therefore results in lower parasitic capacitances and leakage current, complete immunity to latch-up effects, improved resistance to radiations, and less performance variation over temperature than bulk technology due to the presence of the buried oxide layer (BOX) [169], [170], [180].

In bulk CMOS technology, parasitic source and drain to substrate capacitances are observed due to the high level of doping (Fig. 1.22-a). In SOI technology, the BOX reduces the value of these parasitic capacitances [42], [170]. This leads also to lower leakage current, higher performance, and lower power consumption, as explained hereinafter (Fig. 1.21).

The latch-up effect consists in triggering a parasitic bipolar structure between a n- and a p-MOSFET improperly designed next to each other on a bulk substrate. This effect can for instance short circuits V_{DD} and GND in a CMOS inverter (Fig. 1.22-a) [42], [169]. One way to prevent the occurence of this effect in bulk technology consists in using heavily doped substrates [42]. In SOI technology, the BOX provides a complete isolation of n- and p-type devices, preventing latch-up to occur [42], [169], [170]. High resistivity (HR) substrates can therefore be used, resulting for instance in high quality factor inductances [181], and low attenuation constant transmission lines at high frequencies [42], [182], [183].

In its infancy, the SOI technology was dedicated to the niche application market of hard radiation environment electronics (i.e. mainly space applications). The reason is that radiation can induce electron-hole pairs generation in silicon. In SOI technology, this has only a limited impact on the transistors characteristics as the majority of the electron-hole pairs generation take place in the bulk silicon handler, isolated from the top silicon layer by the BOX [184].

Current leakage through the substrate in bulk technology increases with temperature. In contrast, the BOX layer provides dielectric isolation regardless of temperature. SOI technology therefore allows operation at higher temperature [179].

1.2.1.2.1.2 *Improved performance and lower power consumption*

Technology based on SOI wafers benefits from the facts that the top active layer is separated from the bulk silicon handler by an insulating film and the source and drain areas extend to the BOX (Fig. 1.20-b). This vertical isolation protects the top active silicon layer from parasitic effects, as parasitic capacitance coupling between the doped source and drain areas and the bulk silicon [42], [170]. This results in higher performance and lower power consumption [42], as highlighted in Fig. 1.21-a where ring oscillators[8] based on

[7] Complementary Metal Oxide Semiconductor

[8] A ring oscillator consists of an odd number of inverters, the first input being the last inverter output.

65nm node CMOS technology on a bulk silicon wafer (blue lines), and on a SOI wafer (red lines) are compared. At given bias and temperature levels, the ring oscillator on a SOI structure features a power-delay product about 20% lower than its counterpart on bulk technology [185].

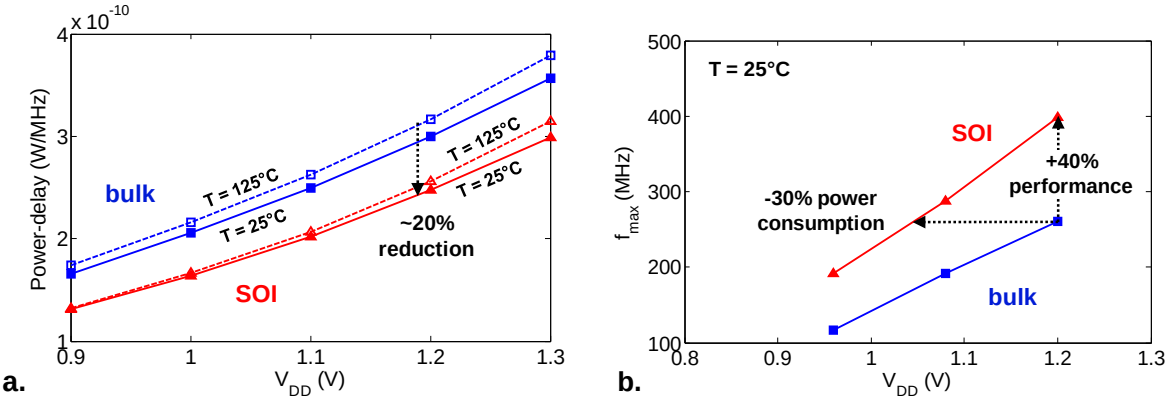


Fig. 1.21 – a. Comparison between power-delay products of ring oscillatiors on bulk (blue lines) and SOI (red lines) 65nm technology showing a ~20% reduction on SOI substrate, and b. Comparison of maximum access frequency of SRAM on bulk (blue lines) and SOI (red lines) 65nm technology demonstrating a ~40% increase of performance at same bias voltage, or ~30% power consumption reduction to reach equivalent performance (Images reproduced from [185]).

This improved performance and reduced power consumption is furthermore demonstrated in Fig. 1.21-b where the access frequencies of Static Random-Access Memory (SRAM) on SOI and bulk technologies are compared. A given bias gives rise to ~40% higher frequency operation on SOI wafer. Otherwise, ~30% less power is consumed using SOI technology rather than bulk technology for the same level of performance [185].

In addition, SOI MOSFETs can feature an inverse subthreshold slope close to the ideal value of 60mV/decade at room temperature [42], [186], [187]. Transistors processed on thin SOI film feature small inverse subthreshold slope [187], [188]. Lower threshold voltage can then be used without degrading the off-state current, therefore allowing really low power operation [42], [186].

1.2.1.2.1.3 *Improved integration density and simplified circuit design*

Among other advantages, SOI technology also provides easy and compact lateral isolation between n- and p-type devices [42].In bulk technology implanted wells formation along with well contacts and shallow trench isolation (STI) are needed (Fig. 1.22-a). Trenches deeper than the implanted wells are required to ensure reliable isolation [169]. In SOI technology, lateral isolation processing only requires to etch trenches down to the buried oxide, resulting in easier processing (Fig. 1.22-b). Furthermore, as the BOX prevents the formation of the latch-up structure, n- and p-type devices can be placed closer to each other. This results in more compact layout and thus greater integration density than achievable with bulk technology (Fig. 1.22) [42], [169], [170], [180], [181], [186], [189].

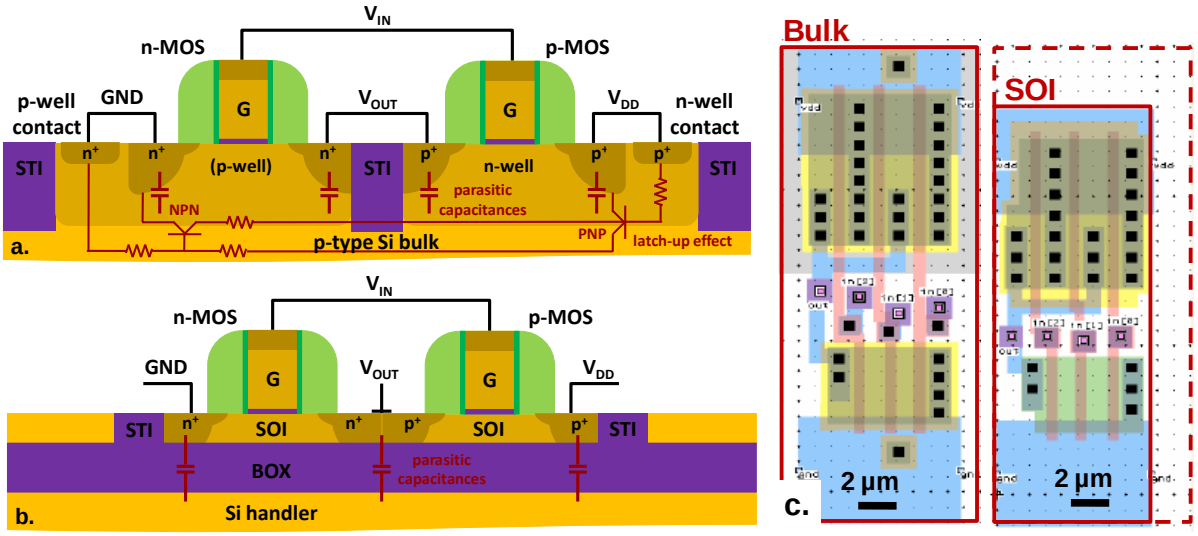


Fig. 1.22 – a. Schematic cross-section of a CMOS inverter on a silicon bulk substrate, including implanted wells, shallow trench isolations (STI), n- and p-well contacts, parasitic capacitances and latch-up circuit representation, and b. schematic cross-section of a CMOS inverter on a SOI substrate, showing an improved integration density thanks to closer doped areas (n^+ and p^+), no well contacts, and parasitic capacitances [42], [169], [186]. c. Example of a layout on bulk (left) and SOI (right) technologies of a NAND gate demonstrating ~25-30% more compact design on SOI substrate (Image reproduced from [189]).

1.2.1.2.1.4 *Short Channel Effect (SCE) reduction*

Down scaling has been a relentless greil during the last decades, as illustrated in Fig. 1.1-b. Scalability challenges associated to submicrometer technology nodes can be more easily addressed with SOI technology as the top silicon layer can be tuned to limit short channel effects (SCE). Considering long devices, it can be assumed that only the electric field generated by the gate controls the depleted area. However, band bending arising at the drain-body junction can not be neglected for short devices. This drain-to-body field penetration that is neglectable for long channels shortens the channel length, therefore modifying the value of the threshold voltage required to cause inversion for short devices. This results for instance in drain-induced barrier lowering (DIBL), favoring parasitic current to flow through the channel even if the applied gate voltage is lower than the threshold voltage. SCE therefore refers to the loss of control over the transistor channel by the gate.

In SOI technology, SCE can be reduced by using a thin top silicon layer. This results in lower field penetration and therefore a better control of the gate over the channel in comparison with bulk technology [42], [170], [186].

1.2.1.2.2 SOI CMOS technology for flexible electronics

As mentioned at the beginning of this document, SOI technology is a promising candidate for application in the field of flexible electronics [170], [179]. Due to the presence of a buried oxide, high performance and low power consumption can be achieved, parasitic effects can be reduced, and the buried layer can act as an etch stop as it will be discussed in next chapter.

1.2.2 LP SOI RF-CMOS 65nm technology

In light of arguments previously discussed, a mature 65nm SOI-CMOS technology node has been selected for this work. High-frequency transistors from this technology node are recognized for delivering a performance level suitable for high frequency, low noise and low power applications. In addition, the 65nm node SOI CMOS technology was considered, at the time this work started, as a good trade-off between state-of-the-art performance, high volume manufacturing, and good understading of its characteristics.This mature technology has been widely characterized in the last years. Therefore, the understanding of its characteristics after transfer on plastic films will take advantage of this experience.

The following sections will describe the static, high frequency, and noise properties of rigid devices from a partially depleted SOI technology with floating body manufactured by *STMicroelectronics*. Methods used to characterize these properties will also be described as the same measurement setups and lumped elements equivalent circuits will be used to characterized the flexible transistors presented in next chapter. Finally, electrical characteristics presented and discussed in this section focus on n-MOSFETs featuring a 60nm gate length L_G, and a total gate width development W_T of 64 µm coming from the parallel association of 1 µm wide unitary gates.Optimization of the number and unitary width of the gate fingers demonstrated that this particular geometry leads to optimal high frequency and noise performance [190].

1.2.2.1 *DC characteristics 65nm RF-SOI n-MOSFETs*

Before any high frequency measurement, the static behavior of a transistor has to be verified. This can be performed by measuring the drain current I_{DS} as a function of the drain voltage V_{DS} for different gate voltage V_{GS} (Fig. 1.23-a). This current-voltage characteristic provides data on the maximum drain current available: here, almost 35 mA (i.e. ~550 mA/mm) at V_{DS} = 1.5 V, and V_{GS} = 1.0 V.

It can be noticed in Fig. 1.23-a that between the linear and saturation modes, the drain current slope suddenly increases, this is known as the ‘kink effect’. It appears for SOI floating body technologies at high drain voltage due to impact ionization. Indeed, the high electric field near the drain region enables the channel electrons to ionize silicon atoms, creating electron-hole pairs. Electrons move through the channel, whereas holes are stored in the body (the BOX prevent them from flowing through the silicon handler, as in bulk technology). Therefore, the body potential increases, lowering the effective value of the threshold voltage, and leading to an increase of the drain current [42], [180], [190].

The static transconductance, defined for a given drain voltage V_{DS} as $g_m^{DC} = \frac{\delta I_{DS}}{\delta V_{GS}}$, can then be extracted (Fig. 1.23-b). The bias condition resulting in the highest static transconductance will subsequently be used for high frequency measurements. Here, V_{DS} = 1.2 V, and V_{GS} = 0.8 V leads to a maximum transconductance g_m^{DC} = 55 mS (i.e. ~780 mS/mm), at a drain current I_{DS} = 270 mA/mm.

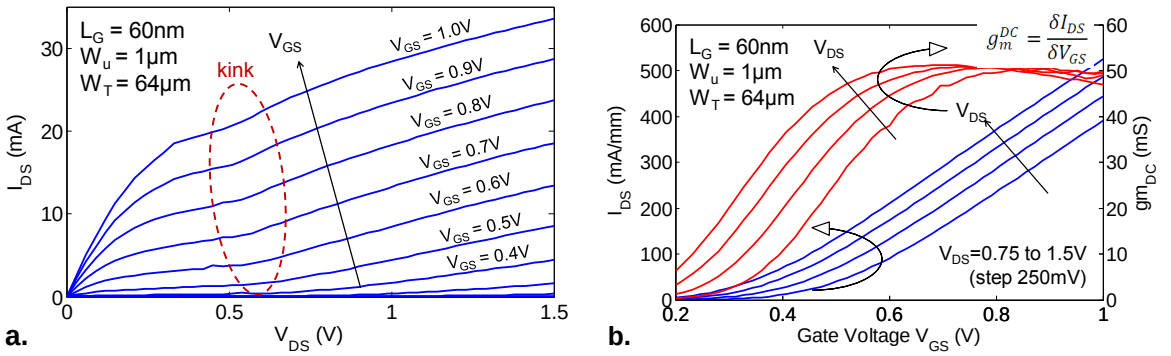


Fig. 1.23 – a. Current-voltage I_{DS}-V_{DS} characteristics, highlighting the 'kink effect' in SOI floating body technologies, and b. drain current I_{DS} and static transconductance g_m^{DC} as a function of gate voltage V_{GS}.

1.2.2.2 *HF characteristics of 65nm RF-SOI n-MOSFETs*

HF characterization methodologies presented in this section are based on several years of experience in the *IEMN-STMicroelectronics* common laboratory, and partially come from work performed by former students [41], [42], [186], [191]. S parameters definition and conversion towards other parameters can also be found in the mentioned references.

1.2.2.2.1 Off-wafer calibration

Before starting to characterize the high frequency (HF) properties of a MOSFET, an off-wafer calibration step has to be performed [41]. An alumina impedance standard substrate (ISS), also refered to as alumina calibration kit, provides standards that enable the vector network analyzer (VNA) calibration [41], [190]. This first step consists in the determination of systematic error terms in order to deembed the HF parasitic characteristics of the measurement setup (e.g. cables, probes), as schematically represented in Fig. 1.24-a. This calibration process complexity grows as the frequency increases [41], [190]. Several calibration methods have therefore been developed as transistor feature size shrinks, involving an increasing number of passive elements and deembedded error terms.

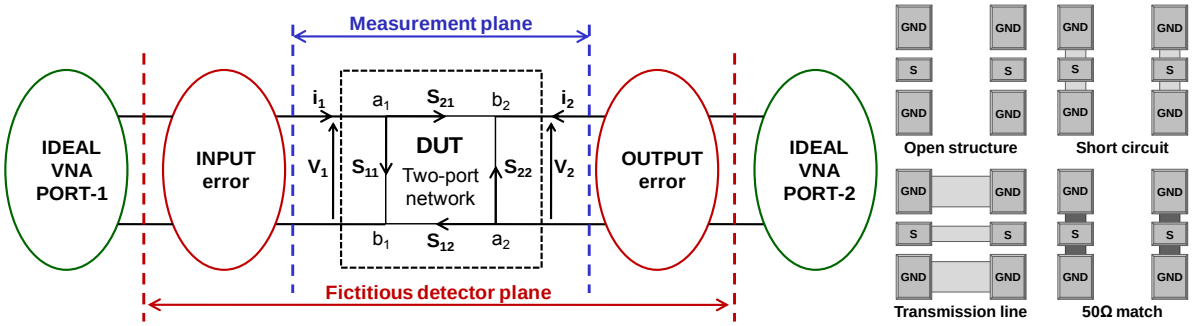


Fig. 1.24 – a. Schematic of a HF measurement setup, including an ideal vector network analyser (VNA), in addition to input and output parasitic systematic errors (due to cables, or probes for instance), reprensented as two-port networks before and after the device under test (DUT) [192]. The VNA calibration step aims to move the VNA reference plane from the fictitious detector plane (including HF errors) to the measurement plane, at the tip of the probes, by deembedding the systematic errors arising from the setup (Image based on reference [192]). b. schematics of four standards used for VNA calibration, namely i) an open structure, ii) a short circuit, iii) a transmission line, andiv) a 50Ω match (Image based on reference [41]).

The thru-reflect-line (TRL) calibration family is based on the measurement of the HF characteristics of three passive elements (including the error two-ports inherent to the measurement setup). Two transmission standards are characterized: usually a thru (i.e. an ideal lossless transmission line) and a transmission line of known length (i.e. known delay). In addition, one reflection standard is also measured, for instance by terminating the measurement planes with short circuits [192]. Fig. 1.24-b describes four standards usually provided on ISS for VNA calibration [41]. The scattering parameters of the input and output parasitic two-ports can be computed from the three HF characteristics of non-ideal standards (i.e. including input and output errors) [41], [190], [192]. Four standards method, as short-open-line-thru (SOLT) [193], or line-reflect-reflect-match (LRRM) [194] for instance, allow to reach better accuracy at high frequency [190]. Extensive comparison of these two calibration methodologies for RF MOSFET characterization is provided in references [41], [190]. In this work, LRRM calibration on alumina ISS (using calkit 138-357 provided by the RF probes supplier, *Cascade Microtech*) were always performed to take the systematic errors arising from the measurement setup into account.

1.2.2.2.2 On-wafer deembedding

After calibrating the VNA, an on-wafer deembedding method is necessary to remove the parasitic contribution of the transistor accesses [41]. The reason is that individual transistors should include contact pads to enable probing and characterization. This is illustrated in Fig. 1.25, where the interconnection multilayer and the vias holes necessary to connect the transistor gates with the top level metallization and the contact pads are highlighted. Fig. 1.26-b provides a picture of a transistor in its probing structure, showing the contact pads, access lines and via holes through the back-end-of-line metallization multilayer.

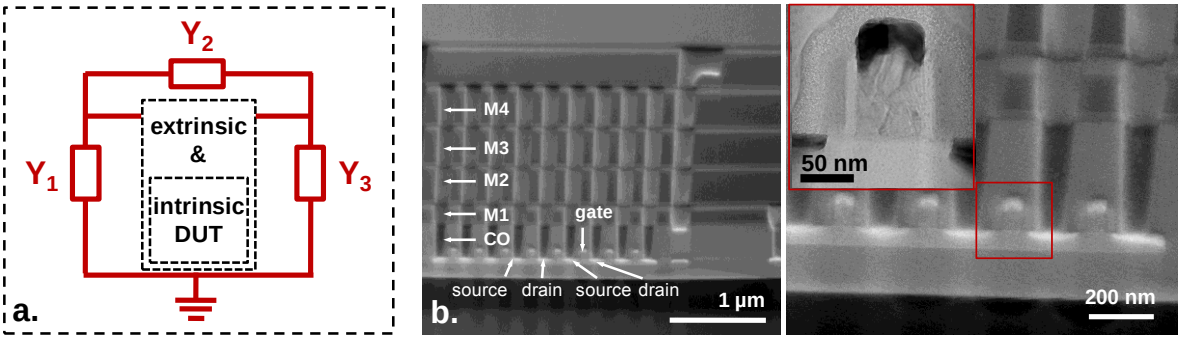


Fig. 1.25 – a. Equivalent circuit of the OPEN deembedding strategy, presenting parasitic contributions of the transistor accesses and the device under test (DUT), b. Scanning and transmission electron microscopy images showing the transistor source and drain regions and gates along with the required interconnection multilayer (metallization levels 1 to 4 and copper vias are highlighted).

1.2.2.2.2.1 *On-wafer deembedding: the OPEN methodology*

In a first approximation, a single step called OPEN deembedding can be applied [195]. The S parameters of a RF transistor and an open structure (featuring the same contact pads, access lines, and vias holes) are measured. The HF characteristics of the deembedded transistor are obtained by substracting the impedance parameters of the open structure Y_{OPEN} to the impedance parameters of the total (undeembedded) transistor Y_{TOT}. Fig. 1.25-a presents the equivalent dircuit of this OPEN deembedding method.

$$Y_{OPEN} = \begin{pmatrix} Y_1 + Y_2 & -Y_2 \\ -Y_2 & Y_2 + Y_3 \end{pmatrix} \qquad Y_{DUT} = Y_{TOT} - Y_{OPEN}$$

1.2.2.2.2 *On-wafer deembedding: the POSS methodology*

As characteristic frequencies of sub-micrometer transistors increases, more complex deembedding methodologies are required to accurately take the HF parasitic effects of the transistor access into account [41]. Extensive comparison of several deembedding methodologies for RF MOSFET characterization is provided in references [41], [190]. Therefore, an improved pad-open-short$_1$-short$_2$ (POSS) methodology [190] has been used as often as possible in this work[9]. Fig. 1.26-a shows a schematic of the parasitic elements taken into account in the POSS method: aluminium contact pads and metallization vias capacitances, in addition to access line inductances [41], [190]. These parasitic elements are also highlighted in Fig. 1.26-b, that presents an optical microscopy image of a MOSFET (left) and a scanning electron microscopy (SEM) cross-section of the same device (right). These two figures enable comparison between the lumped element model and the technological aspects of this deembedding problematic.

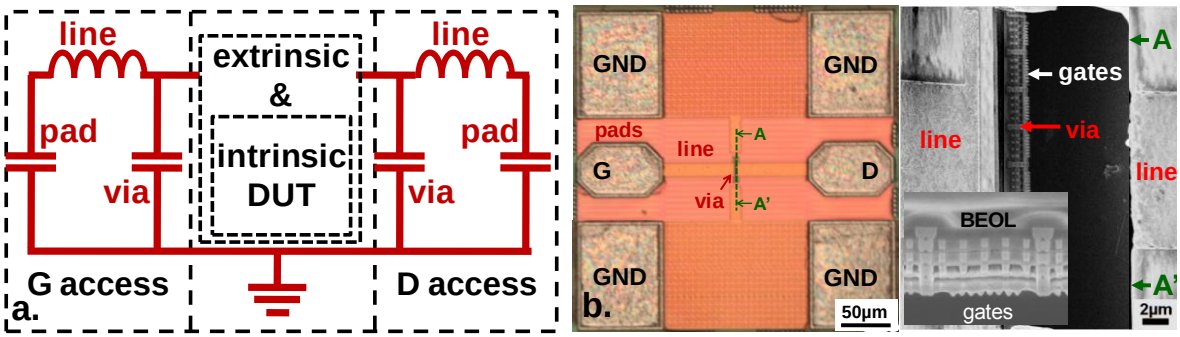


Fig. 1.26 – a. Equivalent circuit of the POSS deembedding strategy, presenting the serial and parallel elements of the accesses around the device under test (DUT), b. (left) image of the transistor of interest, showing the 6 contact pads (source is contacted to GND) and the top level of metallization, and (right) FIB cross-section along the AA' axis highlighting the interconnection line inductance and the 6 levels of BEOL vias capacitance (inset shows transistor copper cias and gates at higher magnification).

In order to remove these parasitic contributions, four deembedding structures need to be measured. First, a 'PAD' structure featuring only aluminium contact pads. Then two 'SHORT' structures, consisting of aluminium contact pads and an access line for SHORT$_1$, whereas SHORT$_2$ also features the metallic vias down to the first interconnection copper level. The 'OPEN' structure is dedicated to the measured transistor, because it includes the gate fingers, in addition to a complete access structure (pads, access line and vias). Contrary to the three first structures that can be used for any transistor of the same technology, the OPEN structure is dedicated to specific transistor geometry (unitary gate width, length and total development width). The measured S parameters of these structures are presented in Fig. 1.27-a.

1.2.2.2.3 S parameters extraction using the POSS deembedding methodology

The deembedded S parameters of the device under test are extracted (Fig. 1.27-b) after measuring the four required standards: S_{pad}, S_{open}, S_{short1}, S_{short2} by calculating two intermediates parameters: S_{line} and S_{via}, as follows:

[9] The OPEN deembedding methodology has been used when measuring bent flexible MOSFETs for reasons explained in chapter 3

$$Z_{line} = \left(Y_{short1} - Y_{pad}\right)^{-1} + \frac{\left(Y_{short2} - Y_{pad}\right)^{-1} - \left(Y_{short1} - Y_{pad}\right)^{-1}}{3}$$

$$Y_{via} = \left[\left(Y_{open} - Y_{pad}\right)^{-1} - Z_{line}\right]^{-1}$$

$$Z_{DUT} = \left\{\left[\left(Y_{TOT} - Y_{pad}\right)^{-1} - Z_{line}\right]^{-1} - Y_{via}\right\}^{-1}$$

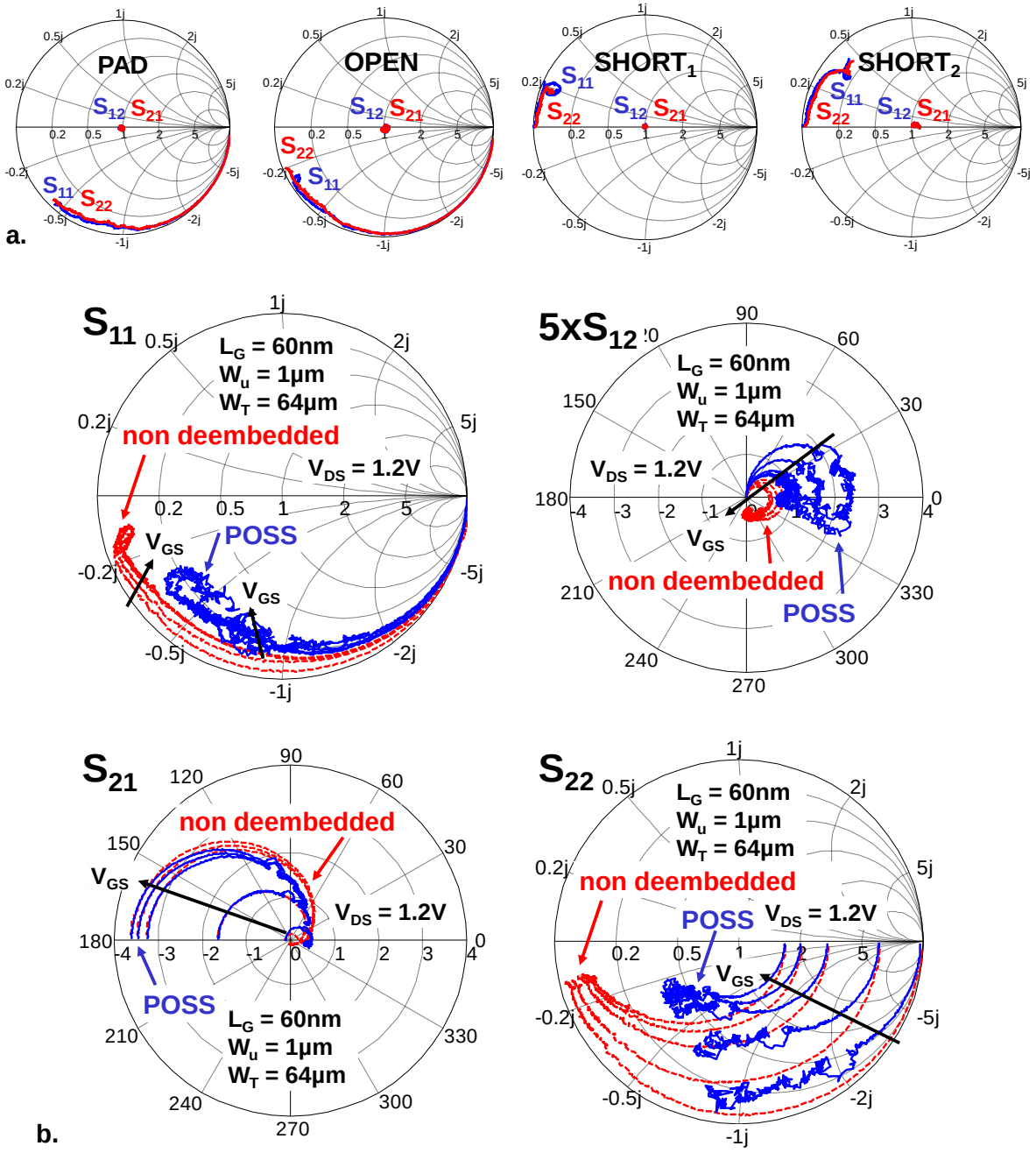


Fig. 1.27 – a. S parameters of the four deembedding structures required for a POSS deembedding methodology: from left to right, pad, open, short$_1$, and short$_2$. b. Comparison of the S parameters of a SOI RF-MOSFET before (ref) and after (blue) POSS deembedding.

1.2.2.2.4 HF figures-of-merit extraction

In a second step, the current gain H_{21} and unilateral power gain, or Mason's gain U can be extracted (Fig. 1.28) using the following definitions:

$$|H_{21}| = \frac{2\,S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$$

$$U = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2\left[k\left|\frac{S_{21}}{S_{12}}\right|-\Re\left(\frac{S_{21}}{S_{12}}\right)\right]} \qquad \text{avec} \qquad k = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}||S_{21}|}$$

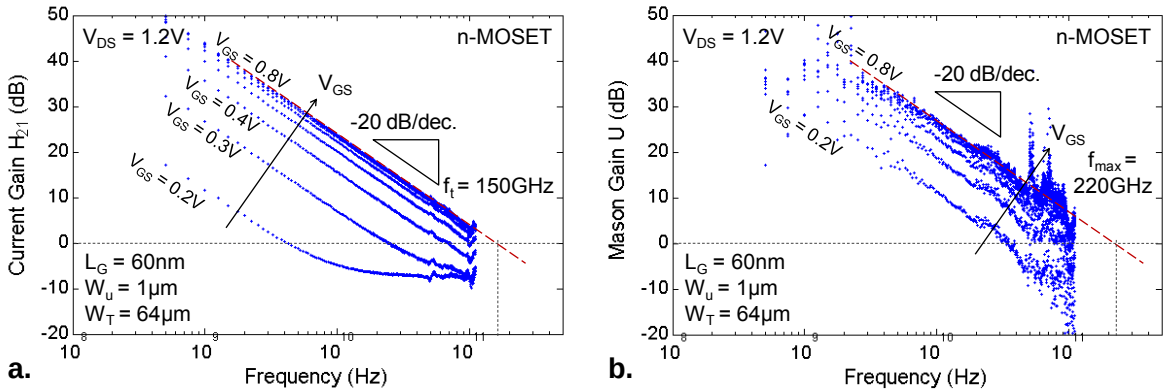


Fig. 1.28 – a. Current gain H_{21}, and b. Mason's gain U of a SOI n-MOSFET as a function of frequency. Gate voltages V_{GS} varying from 200mV to 0.8V

From the frequency dependent current and Mason's gains (Fig. 1.28), two HF figures-of-merit can be extracted. The unity-current-gain cut-off frequency f_T is the frequencies at which the current gain H_{21} is unity (i.e. 0 dB). Likewise, the maximum oscillation frequency f_{max} is the frequencies at which Mason's gain falls to 0 dB. Furthermore, the slopes of these two gains strickly follow the theoretical -20 dB/decade value, ensuring a correct extraction of the characteristic frequencies. This results in f_T = 150 GHz and f_{max} = 220 GHz for n-MOSFET biased at V_{DS}=1.2V, and V_{GS}=0.8V.

The variation of these two characteristic frequencies as a function of drain current (i.e. gate voltage) can be seen in Fig. 1.30-b. This provides information on the bias conditions that result in higher frequencies. Characteristics from p-type devices have been added for the sake of comparison, even if DC and HF measurements of p-MOSFETS are not displayed in this chapter.

1.2.2.2.5 Small Signal Equivalent Circuit (SSEC)

After measuring the HF properties of a MOSFET, and before extracting its noise characteristics, a model of the RF transistor is required. Small signal (or linear) models are often used (as nonlinear ones often require the use of iterative solving) and are well suited to our needs [41], [42], [191]. The small signal equivalent circuit (SSEC) drawn in Fig. 1.29 will be assumed here. More detailed description and hypothesis related to this model, in addition to measurement and extraction techniques used to determine the values of the lumped elements are provided in references [41], [42], [196]–[198]. Therefore, the model extraction will not be discussed here. However, the extracted parameters are presented along with the SSEC in Table 1.4. Measured and retro-simulated S parameters are then compared in Fig. 1.30-a, showing a good agreement, that validates the SSEC parameter extraction. Errors between measurements and model are also presented in Fig. 1.31 and Fig. 1.32.

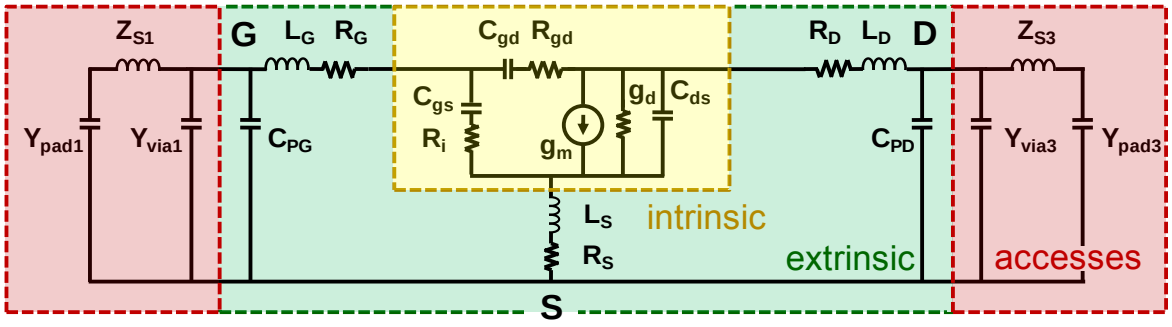


Fig. 1.29 – Noiseless Small Signal Equivalent Circuit (SSEC) including the intrinsic transistor (highlighted in yellow), the extrinsic parameters (green) and the access pads (red).

Table 1.4 – Extracted parameters from the SSEC presented in Fig. 1.29, polarized at a drain voltage V_{DS}=1.2V, and a gate voltage V_{GS}=0.8V, resulting in a drain current I_{DS}=270mA/mm.

Extrinsic parameters								*Intrinsic parameters*							
C_{pg}	C_{pd}	R_g	R_d	R_s	L_g	L_d	L_s	g_m	g_d	C_{gd}	C_{gs}	C_{ds}	R_{gd}	R_i	τ
fF	fF	Ω	Ω	Ω	pH	pH	pH	mS	mS	fF	fF	fF	Ω	Ω	ps
2	8	1	1	0.2	2	2	3	55	10.3	19	40	1	8	7	0

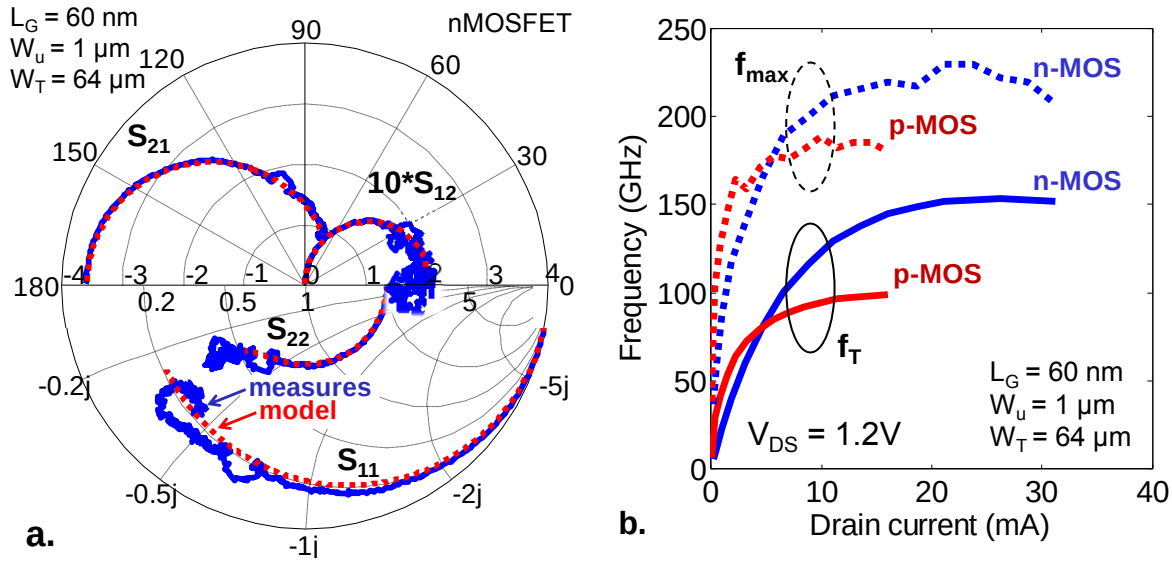


Fig. 1.30 – a. Deembedded S parameters measured from 500MHz up to 110GHz on rigid n-MOSFETs (blue) in addition to retro-simulated S parameters (red) using the model presented in Fig. 1.29, and extracted parameter values given in Table 1.4. Transistor bias conditions are drain voltage V_{DS}=1.2V, gate voltage V_{GS}=0.8V, and resulting drain current I_{DS}=270mA/mm. b. f_T and f_{max} characteristic frequencies as a function of drain current.

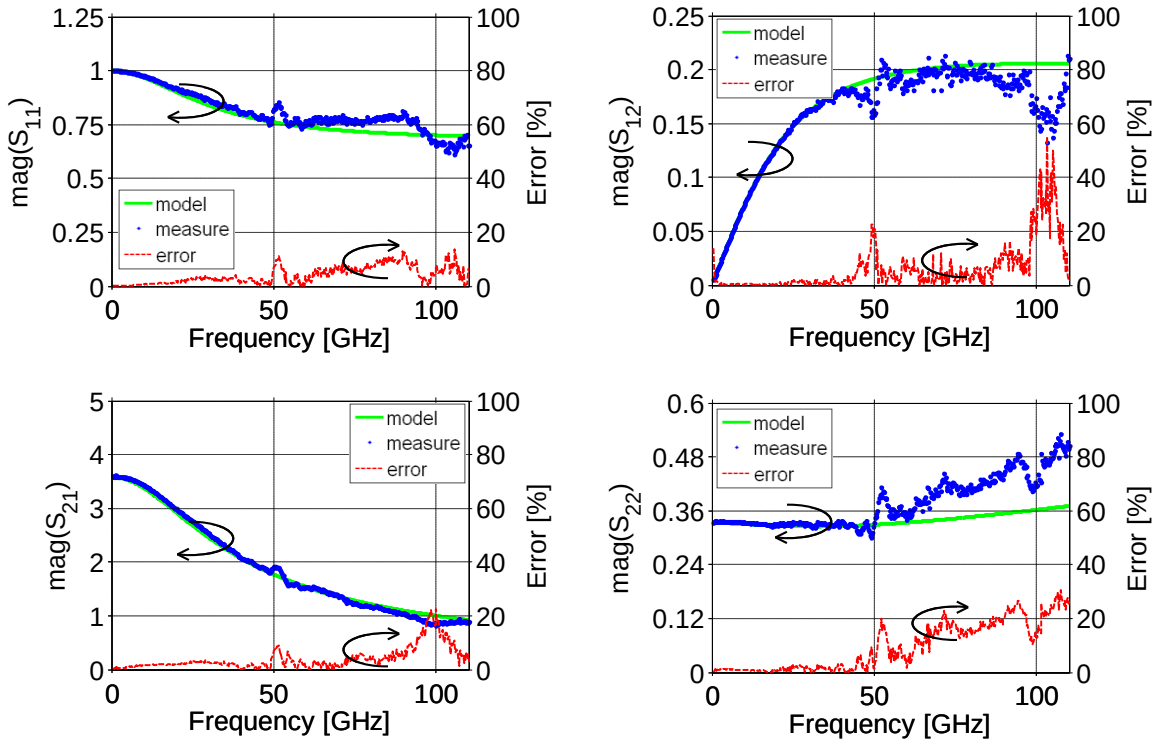


Fig. 1.31 – Magnitude of S parameters measured on a n-MOSFET (blue), retro-simulated from the extracted SSEC (green) and error between model and measurements (red).

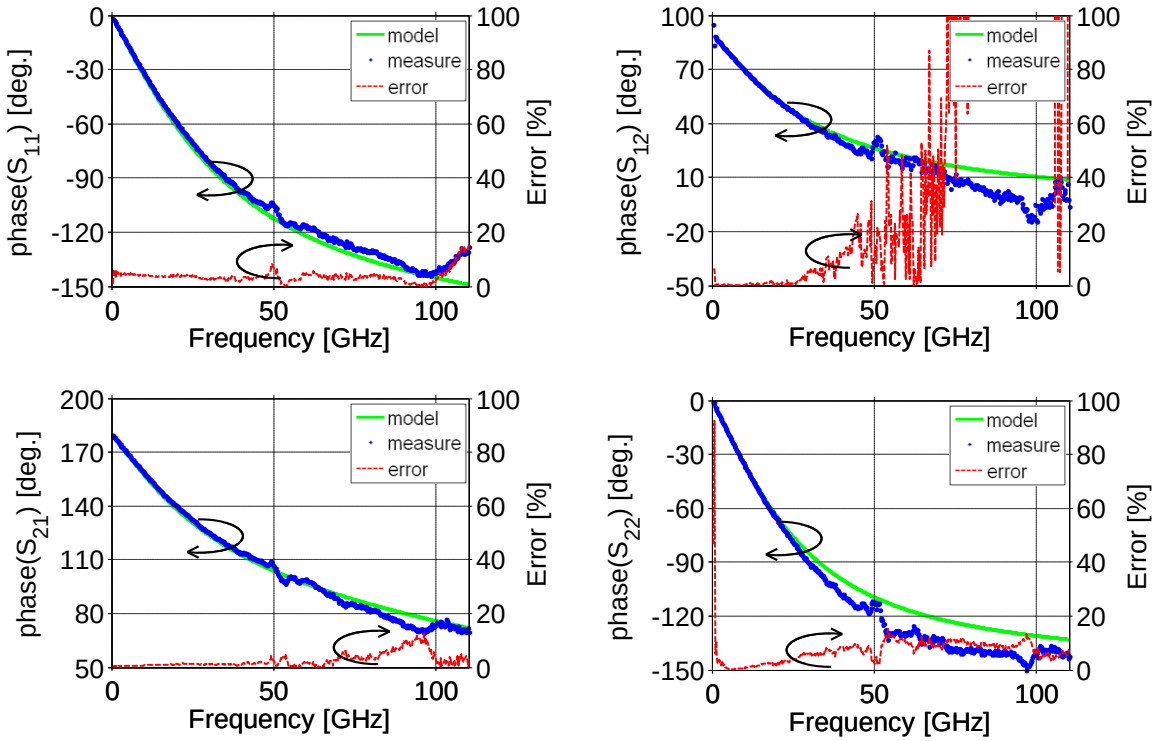


Fig. 1.32 – Phase of S parameters measured on a n-MOSFET (blue), retro-simulated from the extracted SSEC (green) and error between model and measurements (red).

Except for the phase of S_{12}, Fig. 1.31 and Fig. 1.32 demonstrate a good agreement between the deembedded S parameters measured on a RF transistors and the retro-simulated model. Errors higher than 10-15% can only be noticed at high frequency (close to 100 GHz). A final demonstration of the quality of the suggested model can be performed by plotting the modeled H_{21} and U gains (Fig. 1.33), showing excellent matching with measurements. Absolute error in H_{21} modeling only reaches 10% above 50 GHz. Measurement of Mason's gain U shows higher noise. Therefore, an increased error percentage can be seen in Fig. 1.33-b. This error is however relatively low in the 2-50 GHz range, where the measurements fit the theoretical -20dB/dec. slope.

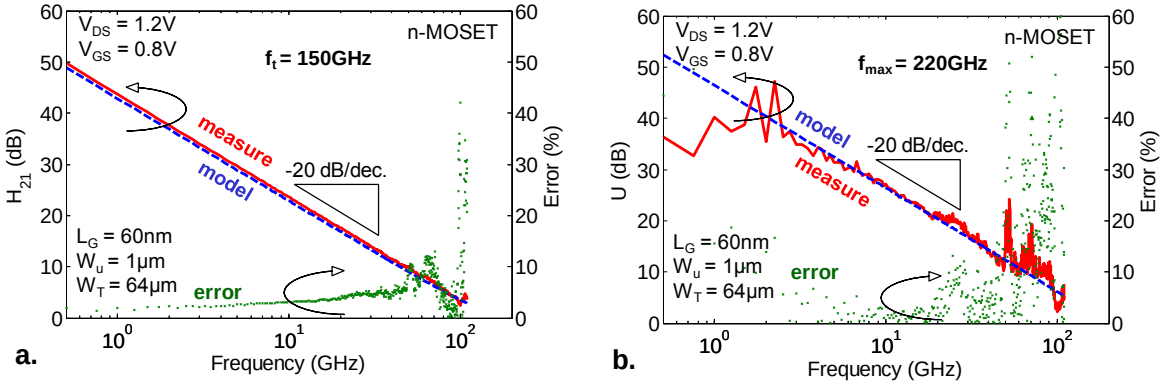


Fig. 1.33 – a. Measured and simulated current gain H_{21}, and b. Mason's gain U as a function of frequency, showing good agreement between model and measurements. Transistor bias conditions are drain voltage V_{DS}=1.2V, gate voltage V_{GS}=0.8V, and resulting drain current I_{DS}=270mA/mm.

1.2.2.2.6 Noise measurement

As already mentioned, one of the advantages of the 65nm SOI RF-CMOS technology selected for this work is its low noise performance. The following section will therefore focus on the noise characteristics of this technology. Noise theory and measurement techniques have been extensively reviewed in references [41], [42], [191], [199] and will thus not be rediscussed here.

A complete description of the noise properties of a two-port device can be given by the four noise figures-of-merit: NF_{min}, R_n, and $\Gamma_{opt} = G_{opt} + i\,B_{opt}$ [199]. The noise figure NF is defined as the ratio between input and output signal to noise ratios at a given noise source admittance Y and temperature T. The minimum value of NF, referred to as NF_{min}, is obtained for an optimum admittance Γ_{opt}. The four noise parameters are linked together as follows (R_n is referred to as the equivalent noise resistance):

$$NF = \frac{S_{in}}{N_{in}}\frac{N_{out}}{S_{out}}\bigg|_{Y,T} \qquad NF(Y) = NF_{min} + \frac{R_n}{G}\left|\Gamma - \Gamma_{opt}\right|^2$$

In order to model noise in field effect transistors, several models and measurement techniques have been proposed [197], [200]–[202]. In this work, a noisy transistor model based on [202] has been used (Fig. 1.34), and noise measurements were carried out using the F_{50} method [203]. Two uncorrelated noise sources have been added to the SSEC presented in Fig. 1.29: a gate noise voltage source e_G, whose equivalent temperature T_{in} is equal to room temperature (T_{in}=290K), and a drain noise current source i_D, whose equivalent temperature T_{out} is unknown [41], [197], [199]. The four noise parameters extraction only requires the knowledge of T_{out} that can be provided by a single 50 Ω generator impedance NF measurement (versus frequency) [42], [203], [204].

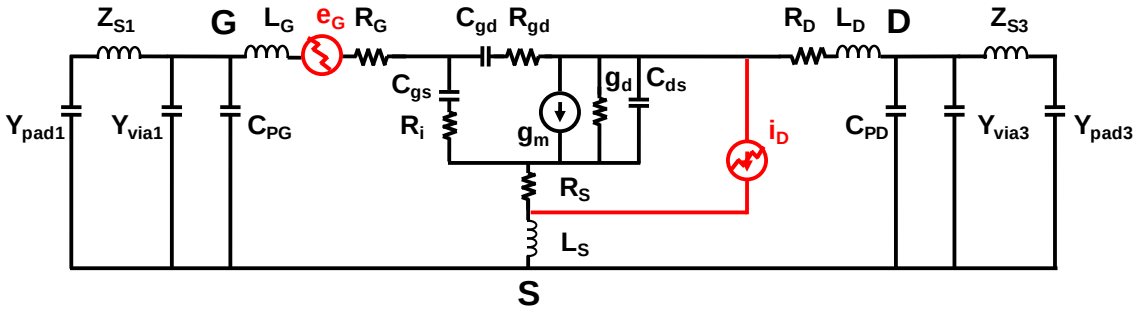


Fig. 1.34 – Small Signal Equivalent Circuit (SSEC) including two uncorrelated noise sources e_G and i_D [41], [191], [202]–[204].

The measurement setup used in this work is described schematically in Fig. 1.35. Noise measurements were performed in two frequency ranges: first between 6 GHz and 20 GHz for a first setup and subsequently from 20 GHz to 40 GHz (this is due to equipment limitations). After calibrating the noise setup by directly connecting the noise source to the noise receiver [191], [205], the output temperature T_{out} can be fitted on NF_{50} measurments, as shown in Fig. 1.36-a. It is important to notice that the four parameters extraction relies on the SSEC extraction described in previous paragraphes (values have been summarised in Table 1.4), and also on the actual value of the 50 Ω noise source impedance, which is slightly frequency dispersive (not shown here) [205].

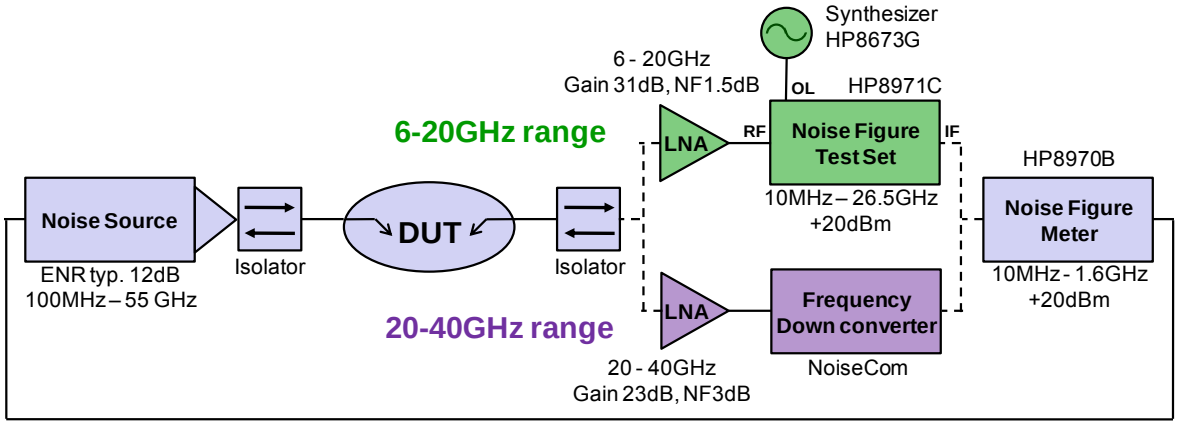


Fig. 1.35 – Noise measurement steup including a noise source in input of the noisy transistor, a noise figure meter in output, and two different routes in between to completely cover the frequency range of interest: from 6 GHz to 40 GHz [205].

From the extracted SSEC and the measured 50 Ω noise figure NF_{50}, the four noise figures-of-merit can be calculated [41], [42], [191]. The resulting parameters are presented here for further comparison with flexible devices (see next chapter). Fig. 1.36-b describes the frequency behavior of the minimal noise figure NF_{min} and the associated available power gain G_a, achieved when the optimum admittance Γ_{opt} is set at the input of the transistor [199]. A minimal noise figure NF_{min} = 0.56 dB with associated gain G_a = 18.2 dB is therefore demonstrated at 10 GHz (and NF_{min} / G_a = 1.10 / 14.5 dB at 20 GHz [205]). Fig. 1.37 shows the equivalent noise resistance R_n and the optimum admittance Γ_{opt}. At 10 GHz, an equivalent noise resistance R_n = 52.2 Ω (51.8 Ω at 20 GHz) is reported [205].

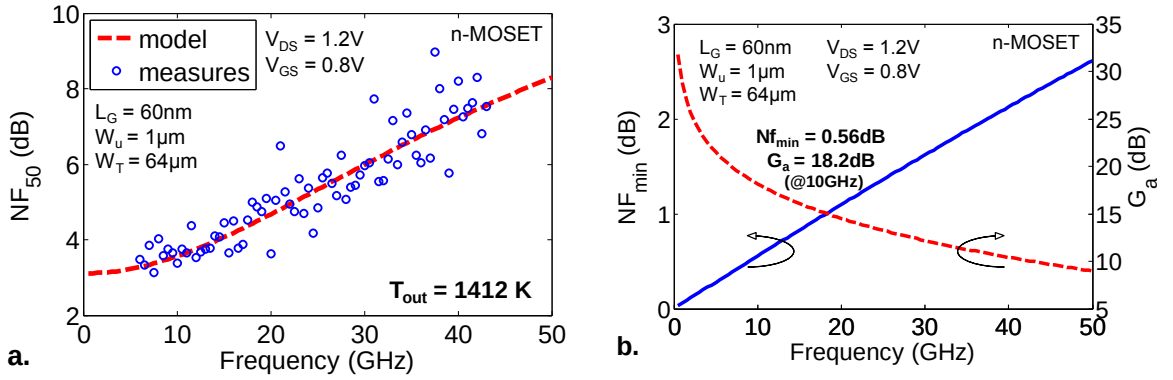


Fig. 1.36 – a. Measured and simulated 50Ω noise figure NF_{50} in 6-20GHz and 20-40GHz frequency ranges for n-MOSFET. Equivalent output noise temperatures T_{out} is reported at drain and gate voltages V_{DS}=1.2V, V_{GS}=0.8V. b. Minimal noise figure NF_{min} and associated gain G_a extracted using the F_{50} method.

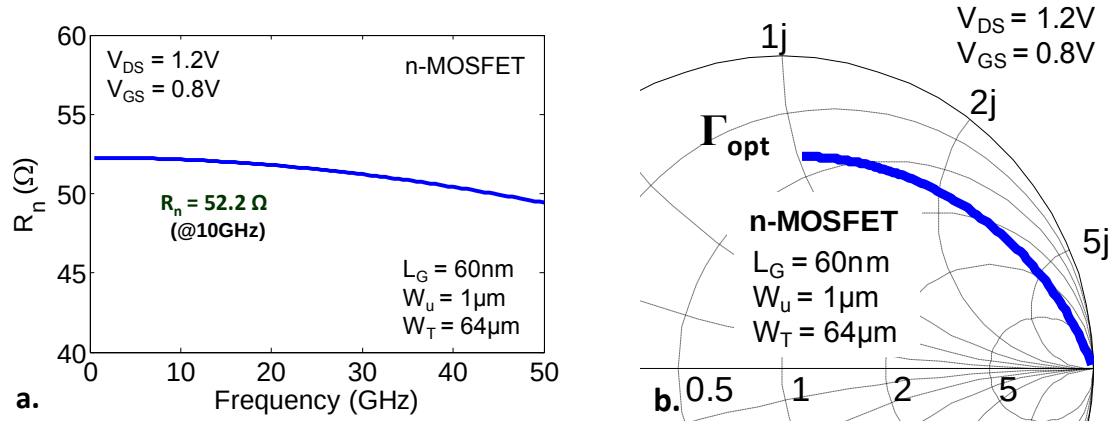


Fig. 1.37 – a. Equivalent noise resistance R_n and b. optimal noise reflection coefficient Γ_{opt} for a SOI RF-MOSFET at drain and gate voltages V_{DS}=1.2V and V_{GS}=0.8V.

1.2.2.3 *Passive devices and circuits*

In order to realize circuits, passive elements are also needed. This work mainly focuses on active MOSFETs, but flexible one-stage amplifiers will be discussed in next chapter. Simple considerations on coplanar waveguides (CPW) and low noise amplifiers (LNA) will therefore be introduced hereinafter.

1.2.2.3.1 CPW: an example of passive devices in 65nm node SOI technology

Coplanar waveguides (CPW) are transmission lines that consist of one central conductor lying in between two grounded lines (Fig. 1.38-c). More details about the equivalent circuit used to model these transmission lines, the deembedding methodologies required to characterize them, and their HF performance can be found in reference [42], [206].

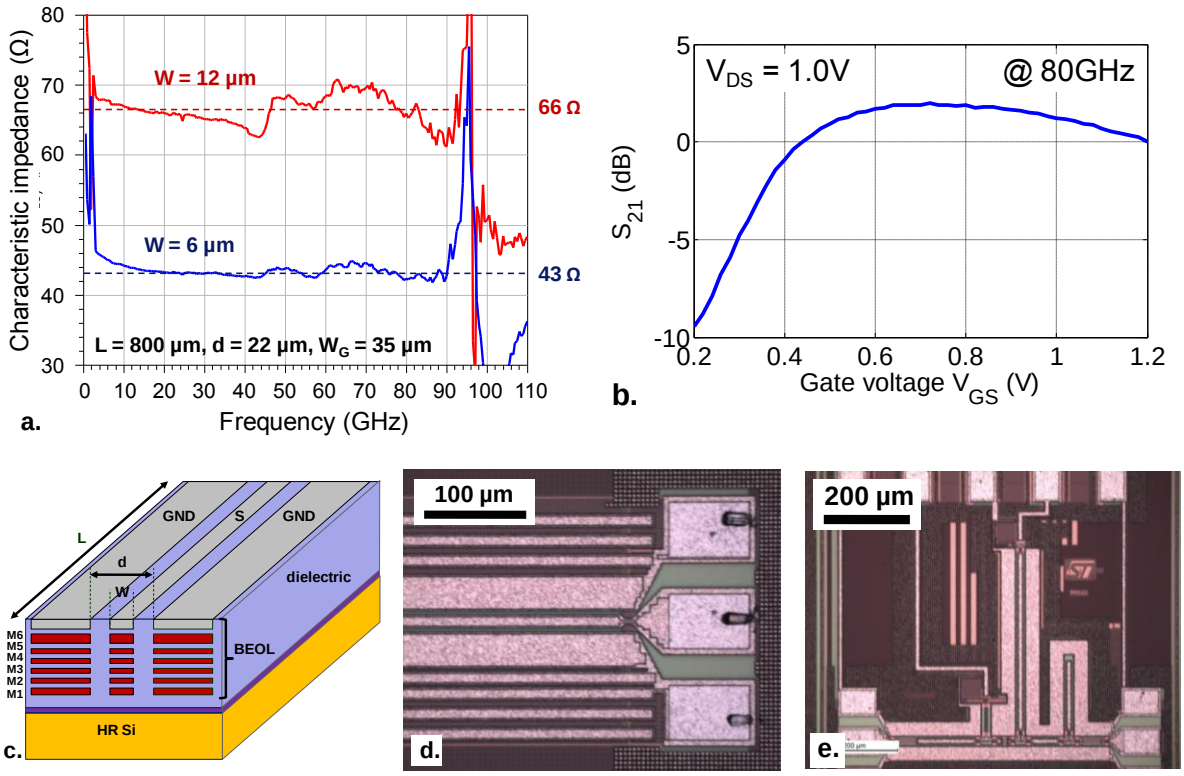


Fig. 1.38 – a. characteristic impedance of two coplanar waveguides (CPW) featuring different geometries, b. Gain S_{21} measured at 80GHz on a low noise amplifier (LNA) biased at V_{DS}=1.0V, c. Schematic, and d. optical microscopy image of a CPW on SOI technology, and e. optical microscopy image of a one-stage LNA.

1.2.2.3.2 LNA: an example of circuit in 65nm node SOI technology

A one-stage low noise amplifiers (LNA) realized on the same 65nm node HR SOI technology have also been characterized [42]. The S_{21} gain parameter measured at 80 GHz is shown in Fig. 1.38-b demonstrating 2 dB of gain for a gate voltage ranging from 0.6 V to 0.8 V.

1.2.3 Integration of 65nm node SOI CMOS technology in flexible electronics

Previous developments have demonstrated the high potentialities of the 65 nm node SOI CMOS technology as a building block for high performance flexible electronics. The combination of high frequency and low noise performance with low power consumption defines a standard for next generation flexible electronics. It will also be highlighted in next chapter that the presence of a buried oxide (BOX) in SOI technology can be an advantage to facilitate the transfer of this technology on a plastic film.

The characteristics presented in this section will subsequently be compared in next chapter with measurement performed on flexible devices to demonstrate the possibility to realize high performance bendable electronics from the 65 nm node SOI CMOS technology.

1.3 Conclusion of the first chapter

As demonstrated in this first chapter, a growing interest in the field of flexible electronics has been identified over the last decade. Both the silicon-based micro- and nanoelectronic industry and the organic and printed electronics community are looking forward bendable, or foldable devices and circuits [19], [25]. The increasing interest in higher performance (in terms of frequency, noise, and power consumption) and more complex devices has also be highlighted (Fig. 1.18-b).

This increasing demand from market and industrial consortia gave rise to several fabrication strategies to enable the realization of devices and circuits combining high electrical performance and high mechanical bendability (Fig. 1.18-a) [10]–[17], [34]–[37], [59], [133], [157], [168]. This first chapter described, discussed and compared these technologies focusing on their ability to provide higher performance bendable electronics. A picture of up-to-date higher reported performance on the field of flexible electronics has been provided (Fig. 1.18), including the work reported here, in addition to papers published during the last three years.

This study leads to the conclusion that the field of flexible electronics could benefit from the high potential of existing rigid technologies (as for instance the suggested 65 nm node SOI CMOS technology). This particular technology was therefore also discussed and characterized on its initial rigid HR silicon substrate for futher comparison after transfer on a plastic film.

The performance described here on conventional rigid silicon wafer are in agreement with requirements enunciated at the beginning of this chapter to cope with challenges associated with fully flexible, smart and communicating devices (Fig. 1.2-a, and Fig. 1.3-b). Transposing such performance from rigid to bendable devices will pave the way to novel and promising applications.

A fabrication process to transfer this high potential from the initial rigid HR silicon wafer onto a flexible plastic film without degrading this technology performance will be presented and discussed in next chapter.

Chapter 2: **Fabrication and characterization of flexible CMOS chips**

The aim of this second chapter is first to describe the methodology developed in this work to integrate high performance flexible CMOS chips and then to characterize and compare them with their rigid counterparts. The first part of this chapter will focus on the transfer-bonding process based on the thinning of thick inorganic CMOS chips from about 800 µm down to micro-scale thin-films and their transfer onto plastic films. The initial substrate is completely removed by successively using different etching techniques (chemical-mechanical lapping, wet etching and $Si:Si0_2$ selective dry etching). Different transfer and bonding methodologies will then be presented and compared in order to finally achieve bonding of the thinned CMOS chips onto flexible plastic films.

The second section of the chapter will deal with electrical characterizations of the CMOS chips transferred on plastic. Static and radio-frequency behaviors will be presented for rigid and flexible RF-MOSFETs chips, along with (to our knowledge) the highest reported performance in terms of high frequency and low noise flexible transistors. Cut-off and maximum oscillation frequencies of 150/160GHz and 110/130GHz will be demonstrated for n- and p-MOSFETs on plastic, respectively. In addition, minimal noise figure and associated gain of 0.57/17.8dB and 0.57/17.0dB at 10GHz for n- and p-type flexible MOSFETs respectively will open the way to radio-frequency and low noise flexible electronics.

2.1 General fabrication methodology

2.1.1 Presentation of the general fabrication process

2.1.1.1 *First considerations about transferring CMOS dies onto plastic films*

2.1.1.1.1 Major steps to consider

As highlighted in the previous chapter, an urgent need for high performance flexible electronics has been predicted [4], [25] and the increasing number of publications [10]–[17], [34]–[37], [59], [133], [157], [168] in this field illustrates the growing interest that both academic research groups and industry hold in this domain (Fig. 1.18). In order to combine high electrical performance and high mechanical bendability, thin-film technology and organic/inorganic hybridation have been recognized as key enabling technologies [6], [7], [207]. The idea first developed by Kao *et al.* [16], [17] to thin and transfer onto plastic film mature technology conventionally processed on silicon led to the realization of radio-frequency flexible circuits.

In order to transfer conventional technology from its initial silicon wafer onto another substrate, the first step to consider is the removal of the major part of the initial handler substrate. By keeping only the active layer and the interconnection layer stack (including protecting layer, contact etch stop liner, and/or embedded stressor layer) the thinned processed film – later referred to as the active die – is only a few micrometers thick and is capable to withstand relatively large deformations. This removal step can be performed from the front side by selectively etching a sacrificial layer that separates the active die from the rest of the initial wafer (the BOX on a SOI wafer [12], [13], [36], [37], [136], [138], [139], or a grown layer on a bulk silicon wafer [14], [15], [140]–[142]). It can also be conducted by thinning the back side of the initial wafer down to the processed layers [16], [17], [155]–[157]. The fabrication methodology developed in this work corresponds to this last strategy and problems arising during the thinning process along with solutions will be discussed in next sections.

After complete thinning of the initial wafer and transfer of the active die onto a flexible film, permanent bonding onto the new substrate has to be considered. Different adhesion mechanisms have been studied, as indirect thermo-compression bonding or solvent enhanced bonding. The principal required characteristics of the permanent bonding are i) a good bonding homogeneity ensuring no or minimal unbonded areas, ii) a relatively thin and hard adhesive layer (because thick and soft materials may lead to large local deformations around the probing tips during electrical characterization, resulting in fracture of the active inorganic die), and iii) a relatively long life time (i.e. no degradation due to water absorption, UV light, or mechanical fatigue).

2.1.1.1.2 Temporary carrier for handling of thin-films

During and after the removal of the initial fabrication wafer, handling of micro-scale thin films is a recurrent issue. In order to prevent the front side of the active die to be damaged and also to ensure a constant flatness and rigidity of this thin film, a temporary carrier is bonded on the front side of the processed wafer as a preliminary step. Trade-off between

strong adhesion bonding, fast de-bonding and selectivity between different adhesive layers will be discussed later. However, it is worth highlighting that such a technology has been recognized as a major challenge in the development of several electronics fields of the More-than-Moore context (3D stacking, packaging, and so on) by the International Technology Roadmap for Semiconductors (ITRS) and that several companies are developing their own solution to this problem (see chapter 1, 1.1.1.2.2 Challenges related to handling of ultra-thin wafers, for more detailed information) [4], [21], [26]–[33].

2.1.1.1.3 Process flow

As a conclusion of these preliminary remarks, a process flow chart of the complete fabrication process is presented in Fig. 2.1. In the first step, the starting material corresponds to a processed SOI wafer featuring 65 nm node RF-CMOS die provided by *STMicroelectronics*. This wafer consists in a 780 µm thick high resistivity (HR) silicon handler, a 145 nm thick buried oxide (BOX), a 60 nm SOI active layer and 5.5 µm of back-end-of-line (BEOL) interconnection layer stack. After bonding a temporary carrier on the front side of the processed CMOS die to ensure flatness and rigidity (step2), the initial silicon handler is completely removed by successively using different etching techniques without altering the BOX layer (step 3). A flexible film is then bonded on the back side of the thinned active CMOS die (step 4) and the temporary adhesive layer dissolution leads to the release of the temporary carrier from the active film (step 5). This fabrication process results in a flexible SOI wafer featuring conventionally processed CMOS dies comprising the interconnection multilayer, the active SOI layer and a BOX layer, the permanent adhesive layer and the plastic handler.

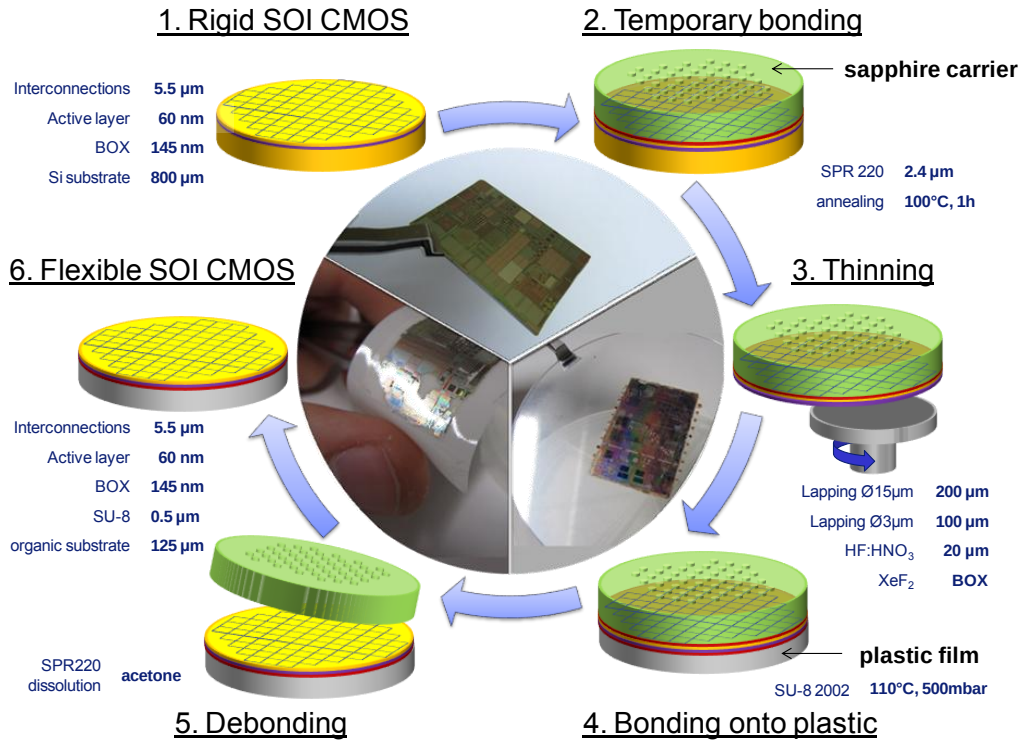


Fig. 2.1 – Process flow describing the fabrication of flexible RF-CMOS circuits from a conventionally processed SOI CMOS wafer (step 1), on which a temporary carrier is first bonded (step 2), ensuring flatness and rigidity during complete removal of the silicon handler of the SOI wafer (step 3). A flexible film is subsequently bonded on the back side of the thin active die (step 4) before releasing it from the temporary carrier (step 5), resulting in a flexible SOI wafer featuring RF-CMOS circuits.

2.1.2 Step 1: Removing the initial bulk silicon substrate

2.1.2.1 *Starting material and available techniques*

2.1.2.1.1 Starting material description

2.1.2.1.1.1 *Description of the stack used in SOI 65nm node technology*

As mentioned in Fig. 2.1, the starting material of this work, provided by *STMicroelectronics*, is a 300 mm processed SOI RF-CMOS wafer (that can be seen in the background of Fig. 2.2-b) featuring a 780 µm thick silicon handler, a 145 nm thick buried oxide (BOX) layer, a 60 nm active patterned silicon-on-insulator (SOI) layer and six levels (5.5 µm of total thickness) of metal and dielectric back-end-of-line (BEOL) interconnections multilayer (see Fig. 2.2).

This 300 mm wafer is first singulated into individual cells in order to develop the transfer process onto organic films at die scale and not at full wafer scale. Each die features RF-MOSFETs which unitary gate length and total width vary respectively from 55 nm to 2 µm and 64 µm to 120 µm with different numbers of gate fingers and cells, in addition to CMOS circuits, including Low Noise Amplifiers (LNA) as presented in the previous chapter. The complete process described in this chapter has therefore been developed at die scale but a transfer to wafer scale should be relatively straightforward assuming the availability of equipments capable to process 300 mm wafers.

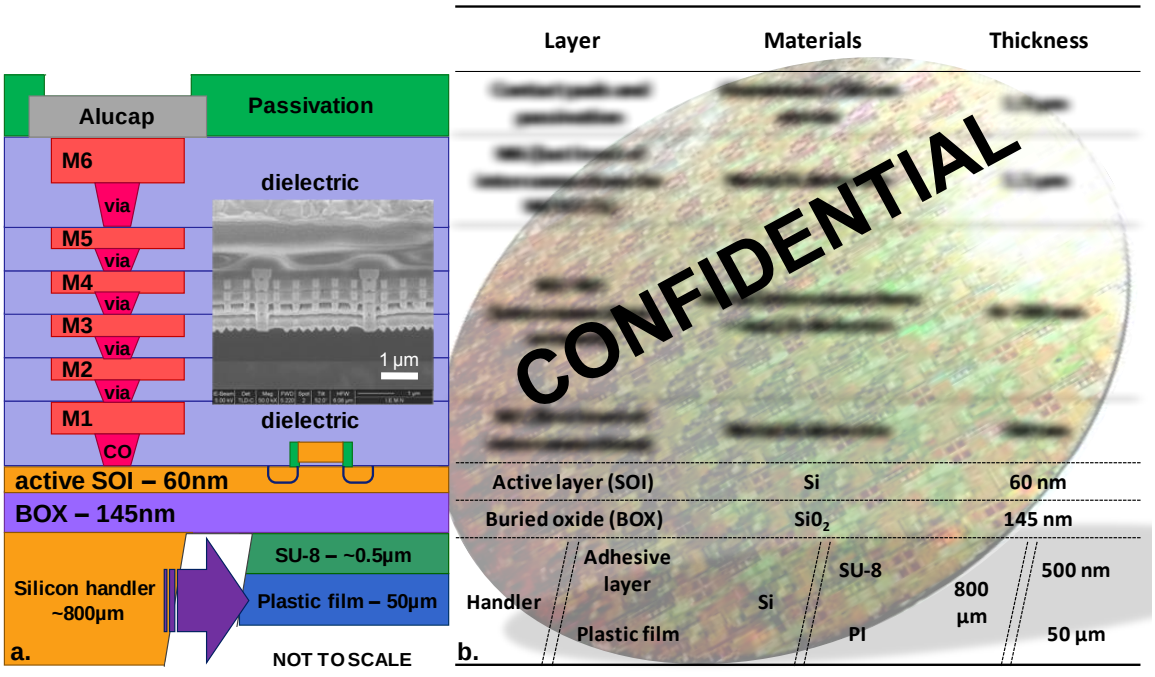


Fig. 2.2 – a. Stack description before and after transfer of the active CMOS die onto a plastic film (not to scale), inset: SEM image of the front- and back-end-of-line multilayer of a 65nm MOSFET, along with b. a table containing the different layers designation, materials, and thicknesses, before and after transfer onto a plastic film (part of the table has been removed for confidentiality reasons).

2.1.2.1.1.2 *Objective of the silicon handler removal step*

The objective of this work is to realize flexible RF-MOSFETs by transferring them from a conventional rigid SOI wafer onto a plastic substrate. In order to ensure that thinned and transferred MOSFETs (Fig. 2.1) will exhibit transistors electrical characteristics, it has been chosen not to remove the buried oxide layer (BOX) to protect and keep undamaged the active SOI layer. Indeed the silicon handler removal exhibits some non-homogeneity (as presented hereinafter) resulting in slight damages to the etch stop layer. By using the BOX as an etch stop layer the active layer is protected during the complete etching process. In conclusion, a constant attention will be focused on the protection of the active SOI and the back-end-of-line (BEOL) layers during the silicon handler removal process.

2.1.2.1.2 Available etchants and selection criteria

Numerous different techniques are described in literature to remove silicon, mainly: i) chemical-mechanical grinding, lapping or polishing, ii) wet etching techniques (anisotropic etchant as TMAH, KOH, NH_4OH, NaOH, or isotropic etchant as the HF-HNO_3 mixture), and iii) dry etching techniques (using SF_6, $SiCl_4$ or CF_4 continuous or pulsed plasma, XeF_2 vapor etching).

The selected etching methods should enable the complete removal of the silicon handler taking into account several specifications: the BOX layer should be kept undamaged, the back side removal should results in a thin active die with a fracture strength compatible with the transfer process from the temporary carrier onto the flexible substrate (Fig. 2.1 step 4-5), and finally the global time and cost of the handler removal process should be kept as low as possible considering previously given conditions.

2.1.2.1.2.1 *Chemical-mechanical techniques*

Mechanical grinding and chemical-mechanical lapping techniques enable to quickly remove a large amount of material. However, sub-surface damages arise on the back-side of the thinned chip. Therefore, important parameters when considering these methods are the final thickness, the resulting fracture strength (mainly determined by the final thickness, the roughness and the surface defect geometry), in addition to the thickness removal homogeneity, and etch rate.

In mechanical wafer thinning processes, thinned die fracture strength mainly depends on the few larger scratch geometry and sharpness [208]. The best way to enhance fracture strength is to perform a subsequent isotropic etch step to turn sharp V-shaped scratches into U-shaped groove, therefore reducing stress concentration [208]. This stress relief etching step is thus an important parameter to consider: high fracture stress can therefore be obtained by removing a large part of the sub-surface damages.

Fig. 2.3-a shows the load required to break silicon wafers that have been thinned to various end thicknesses (from 200 µm down to 75 µm) and then exposed to wet etching in HF:HNO_3 to remove 3 µm of silicon from the damaged surface [209]. The thinner the final sample the lower is its fracture strength. Fig. 2.3-b first highlight the effect of the stress relief step by comparing sample that have only been grinded with samples that have further been etched using HF:HNO_3 solution, or SF_6 plasma etching. The enhanced breaking load after a longer stress relief step, etching 25 µm from the thinned surface, is also pointed out (green symbols in Fig. 2.3-b).

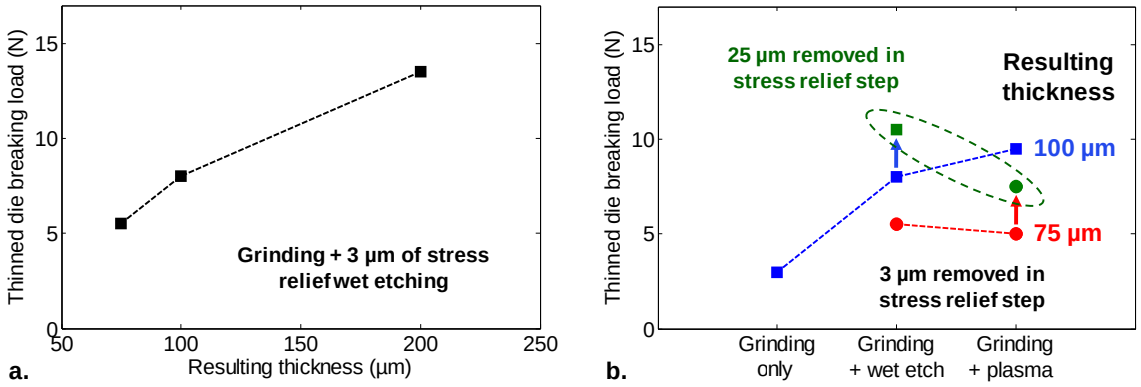


Fig. 2.3 – Breaking loads measured on silicon bulk wafers thinned by grinding, with or without a subsequent stress relief step, performed by wet etching ($HF:HNO_3:CH_3COOH$, 6µm/min), or dry plasma etching (SF_6, 3µm/min), a. as a function of the resulting thickness (after 3 µm stress relief wet etching), and b. for different stress relief conditions: wet etching or plasma, down to 75 µm (blue squares) or 100 µm (red circles), including a 3 µm, or 25 µm (green symbols) stress relief step (Images reproduced from [209], more information on statistical aspects are discussed in [209]).

Similar studies have been performed in [160], [208]. It has been furthermore demonstrated that stress is generated by the grinding step on the back surface and several micrometers below it [160]. Fig. 2.4-a shows the level of generated stress as a function of the distance from the backside grinded surface for different stress relief etching steps (or without performing one). An isotropic plasma etching results in the lower stress concentration [160]. This stress reduction, and therefore the breaking load improvement (Fig. 2.3-b [209]), can be explained by the shape of the larger surface defects [208]. Mechanical grinding results in sharp, V-shaped surface defects. This leads to high stress concentration at the defect tip and therefore decreases the thinned sample fracture strength [208]. Conversely, performing a stress relief plasma etching step tends to smooth the defect geometry into U-shaped defects, thus reducing the stress concentration, as presented in Fig. 2.4-b [208].

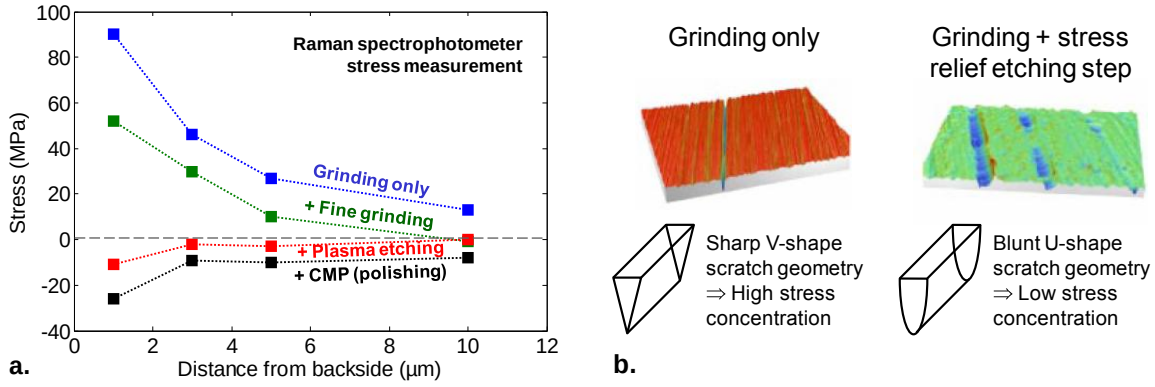


Fig. 2.4 – a. Stress generated by back-side thinning (measured by Raman spectrophotometry as a function of depths below the etched surface) after grinding only (blue), and after a subsequent stress relief step: using finer grid grinding (red), plasma etching (red), or chemical-mechanical polishing (black), image reproduced from [160]. b. Morphology of two grinded surfaces, with (right) or without (left) a stress relief step using plasma etching. Defect geometries are highlighted, images reproduced from [208]

2.1.2.1.2.2 *Wet etching techniques*

The main difference between silicon wet etchants is related to their anisotropic characteristic and etching rate [210]–[212]. Isotropic etchants feature a similar etch rate in all directions, whereas anisotropic etchants etch rates depend upon the silicon orientation to crystalline planes. This leads to vertical and lateral etch rates that may differ and therefore V-shapes groove or pyramidal cavities in the etched silicon layer. In this work, wet etching is used as a stress relief step performed after chemical-mechanical lapping. Therefore, isotropic wet etchants have been privileged to create blunt U-shaped defects (Fig. 2.4-b). Anisotropic etchants will then only be mentioned for the sake of comparison but not studied in details.

2.1.2.1.2.3 *Isotropic wet etching: HNA solution*

The most common isotropic silicon etchant, referred to as 'HNA', is a mixture of hydrofluoric (HF) and nitric (HNO_3) acids, often diluted in acetic acid (CH_3COOH), or water [211]–[213]. The silicon etching process can be divided into two different mechanisms. The silicon surface is first oxidized by the nitric acid (Eq. 2.1). This SiO_2 layer is subsequently dissolved by hydrofluoric acid (Eq. 2.2), exposing a new silicon layer to nitric acid. The complete chemical mechanism is described by Eq. 2.3 [213]. Acetic acid is frequently used as diluent.

$$3\,Si + 4\,HNO_3 \rightleftharpoons 3\,SiO_2 + 4\,NO + 2\,H_20 \qquad \textbf{Eq. 2.1}$$

$$Si0_2 + 6\,HF \rightleftharpoons H_2SiF_6 + 2\,H_20 \qquad \textbf{Eq. 2.2}$$

$$3\,Si + 4\,HNO_3 + 18\,HF \rightleftharpoons 3\,H_2SiF_6 + 4\,NO + 8\,H_20 \qquad \textbf{Eq. 2.3}$$

The silicon etch rate in HNA solution depends on the concentration of the limiting specie, as presented in Fig. 2.5. The dependence of the etch rate on the HF concentration is dominant in HNO_3-rich solution. Conversely, in HF-rich solution, HNO_3 concentration determines the silicon etch rate. Fig. 2.5-a shows a ternary diagram that describes the etch rate of silicon in HF:HNO_3 mixtures diluted in acetic acid (CH_3COOH), or water [214].

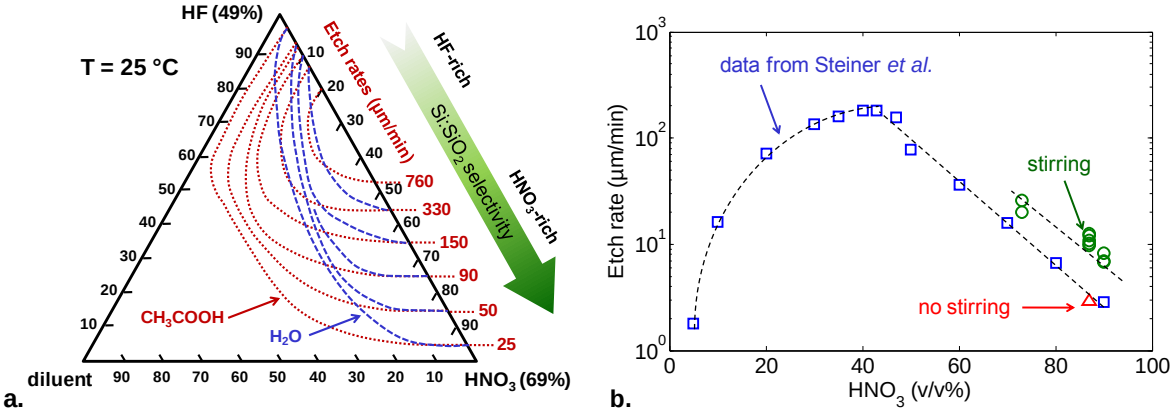


Fig. 2.5 – a. Effect of HF:HNO_3:diluent composition on silicon etch rate showing curves of constant etch rate when using water (blue), or acetic acid (red) as a diluents, increasing Si:SiO_2 selectivity is highlighted (image reproduced from [214]), and b. effect of HNO_3 concentration on the silicon etch rate (image reproduced from [213]), including data measured in this work with (green), or without (red) magnetic stirring, highlighting the fact that other experimental parameters impact the etch rate.

However, acids concentration is not the only important parameter. Aging of the solution due to large amount of dissolved silicon (and concomitant decrease of the NO_2^- ions concentration), stirring speed, and temperature also affect the etch rate and condition the final roughness of the silicon surface [213]. Fig. 2.5-b shows the dependency on concentration, and also highlights the fact that stirring the solution increases the silicon etch rate, for given reactants concentration.

2.1.2.1.2.4 *Anisotropic wet etching*

Several anisotropic wet etchant are commonly used to etch silicon with different etch rates along the various crystal directions: i) organic aqueous solutions as ethylene diamine pyrocatechol (EDP) [215], [216], ii) ammonium hydroxide solution, as NH_4OH [217], [218], or tetramethyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$) [219]–[221], iii) inorganic alkaline aqueous solutions as potassium hydroxide KOH [215], [216], [219], [222], or sodium hydroxide NaOH [215], [216], for instance. These silicon etchants feature orientation dependent etch rates, often resulting in lower etch rate on the (111) planes, i.e. where the silicon atoms are the more densely packed, than on the (100) and (110) planes [210], [219], [220], [222], [223].

EDP solution is carcinogenic, difficult to dispose of and ages rapidly. Therefore, this solution is not as widely used for anisotropic silicon etching as TMAH or KOH for instance [210], [223]. TMAH features similar etch rates, selectivities (to silicon dioxide, aluminium, and different crystallographic orientations), and is easier and safer to manipulate than EDP. KOH is also widely used, due to its low cost, and wide availability. It should however be noticed that KOH features higher silicon dioxide and aluminium etch rates than TMAH and furthermore cannot be considered as CMOS compatible[10] due to the presence of alkali metals [210], [223]. Indeed, these metals may have a detrimental impact on MOSFETs performance. Even if considered CMOS compatible, TMAH may results in unwanter etching when long exposure is considered. Therefore, an encapsulation of the front side may be relevant [221]. Silicon etching mechanism using these anistropic wet etchants is described in [215] as follows:

$$Si + 2\,H_2O + 2HO^- \rightleftharpoons Si(OH)_2O_2^{2-} + 2\,H_2 \qquad \textbf{Eq. 2.4}$$

2.1.2.1.3 Dry etching techniques

Dry etching techniques generally involve higher equipment cost, vacuum pumping and lower throughput than wet etchants [210]. Both isotropic and anisotropic dry etching techniques are also commonly available for silicon manufacturing. Plasma-assisted reactive ion etching (RIE), or inductively coupled plasma (ICP) etching are generally used for anisotropic etching, but can also provide isotropic etching according to the selected experimental parameters [210], [224]. Conversely, plasmaless vapour-phase etchants as xenon difluoride (XeF_2) mostly result in isotropic etching of silicon [210]–[212].

2.1.2.1.3.1 *Plasma*

Plasma etching provides a complete set of solutions to etch different materials (e.g. silicon, oxide, or metals) depending of the selected gas (e.g. O_2, SF_6, CF_4, CHF_3, Cl_2, $CHCl_3$, BCl_3, or various combinaisons of gases) [211], [212], [225]. Flow rate, pressure, power, and gas

[10] Defined as 1) allowing wafer to be immersed directly with no special measures, and 2) no alkali ions [223]

diluents (mainly N_2, or He) are the main parameters that impact etching, in terms of anisotropy, etch rate, roughness, and selectivity to a mask or a stop layer [210]–[212].

Contrary to wet etching, anisotropy in plasma-assisted etching is independent of the crystal orientation, as it arises from the ion bombardment direction [210]. Deep silicon etching, refered to as deep (D)RIE [226], is achieved by protecting side walls using chlorofluorocarbon deposition [226], [227]. This can be performed using the so-called Bosch technique: by alternatively etching (using SF_6 for instance), and passivating side walls (using chlorofluorocarbon gas), or by mixing the two gases [210], [227].

2.1.2.1.3.2 *XeF_2*

XeF_2 is a crystalline solid that can be easily sublimated as it features a vapor pressure of abour 4.5 Torr at room temperature [210], [228]. The mechanism of silicon etching by XeF_2 is given by the following equation [228], [229]:

$$2\,XeF_2 + Si \rightleftharpoons 2\,Xe + SiF_4 \qquad \textbf{Eq. 2.5}$$

Common etch equipment are based on pulsed etching. An expansion chamber is first filled with XeF_2 up to a given pressure. The etchant is then expulsed towards the sample, in the etching chamber, until a target pressure, later refered to as the output pressure, is reached. After a short etch time (generally less than a minute), the chamber is filled with inert nitrogen gas and then pumped down again, evacuating gas-phase byproducts as SiF_4. Another pulse etch cycle can then begin [228], [229].

Silicon etching with XeF_2 is highly dependent on the loading condition, as described in [229]. Indeed, as for plasma etching, the etch rate varies as the area of exposed silicon changes. Temperature, etch pressure, cycle time (as presented for instance in Fig. 2.6-a) and output pressure are also important parameters.

One of the main advantages of XeF_2 etching over alternative techniques is its high selectivity to silicon dioxide, as illustrated in Fig. 2.6-b (also to silicon nitride, and aluminium) [210]–[212], [223], [230], [231]. XeF_2 etching is also CMOS compatible [210], [223], [228]. This explains why XeF_2 etching is often used to release membranes for the realization of CMOS compatible MEMS [228]. Etching of 280 µm of bulk silicon down to a 5 nm SiO_2 stop layer has also been demonstrated [232].

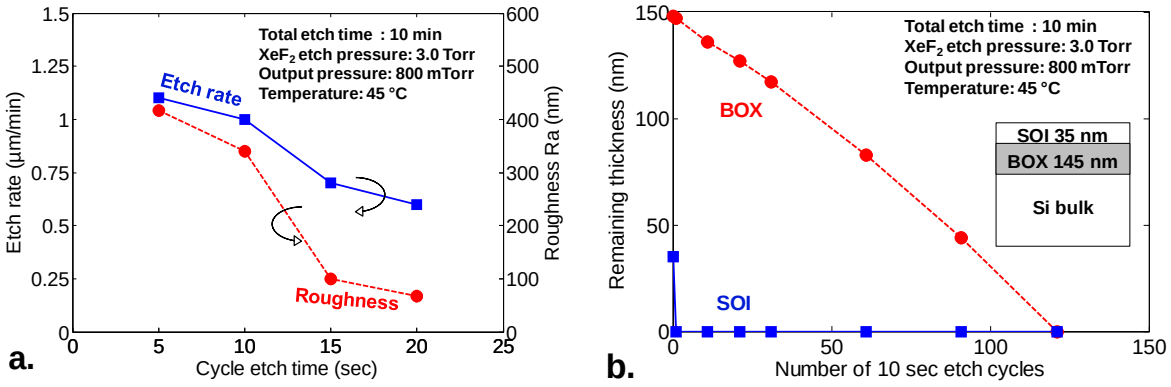


Fig. 2.6 – a. Effect of cycle etch time on the etch rate (blue), and average roughness (red) of silicon, measured by profilometer, during XeF_2 pulsed etching, considering a total etch time of 10 min, an XeF_2 etch pressure of 3.0 Torr and an output pressure of 800 mTorr, and b. measured etching of silicon dioxide in XeF_2 pulsed etching using the same etching parameters. The buried oxide (BOX) thickness of a SOI wafer was measured by ellipsometry.

2.1.2.1.3.3 *Comparison*

A general comparison of common etching techniques is provided in Table 1.2 [210]–[212], [223].

Table 2.1 – Comparison of selected bulk silion etchants, table mainly based on [210]–[212], [223].

	HNA HF:HNO3: CH_3COOH	**Alkali-OH** e.g. KOH, NaOH	**EDP** ethylene diamine pyrocatechol	**TMAH** tetramethyl ammonium hydroxide	**XeF_2**	**SF_6 plasma**	**DRIE** Deep Reactive Ion Etch
Etch type	wet	wet	wet	wet	dry	dry	dry
Anisotropic	no	yes	yes	yes	no	varies	yes
Availability	common	common	moderate	moderate	limited	common	limited
Si etch (µm/min)	> 1	< 3	< 2	< 2	< 3	~ 1	> 1
Roughness	low	low	low	variable*	high[#]	variable	low
Oxide etch[^] (nm/min)	10 to 70	1 to 20	1 to 80	~ 1	< 1:10[4]	low	1:10[2]
CMOS compatible°	no	no	yes	yes	yes	yes	Yes
Cost[+]	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate	high	high

* Varies with %wt TMAH, can be controlled to yield very low roughness.
[#] Addition of Xe to vary stoichiometry in F or Br etch systems can yield optically smooth surfaces.
^ $Si0_2$:Si etch rate selectivity can be provided instead of etch rate itself.
° Defined as 1) allowing wafer to be immersed directly with no special measures, and 2) no alkali ions.
[+] Includes cost of equipment.

2.1.2.1.3.4 *Selected process*

According to the above considerations and tests performed on equipements available in IEMN clean room, a three-step thinning process has been developed. The aim is to completely remove the 780 µm of bulk silicon from the back side of a SOI-CMOS processed chip without damaging the active layer of the stack, i.e. the SOI layer. The selected process involves i) first a coarse chemical-mechanical lapping down to 100 µm of remaining silicon, ii) a wet etch step in HNA then enables to reduce the silicon thickness down to 20 µm, and iii) a final highly selective XeF_2 etching to clean to remaining few micrometers of silicon and stop on the buried oxide (BOX) layer.

A complete and detailed description of this process is presented in next sections. However, a home-made thickness measurement tool will first be presented and then used to evaluate the proposed three-step thinning process.

2.1.2.1.4 Measurement setup description

2.1.2.1.4.1 *Requirements*

In order to characterize the silicon handler removal, an experimental setup able to measure the thickness and uniformity across the whole surface of the thinned die was required. As no such equipment was available at IEMN, it has been decided to build our own-made measurement setup. The specifications for this setup included a thickness measurement accuracy close to the micrometer, a measuring range of at least 1 mm, a travel range allowing the characterization of a 3 inches wafer, a relatively large (i.e. non limiting) positioning accuracy in the x- and y-directions (100 µm error along x- and y- axes was acceptable) but a good repeatability in the z-axis. Non-contact measurement was also a requirement to ensure a non destructive characterization as it would be performed several times during the complete thinning process. To comply with the above specifications, a CCD laser sensor (*Keyence LK-G10*) was selected with two micro-positioning stages (*PI M-403.42S*) to move the sample along the x- and y-axes (Fig. 2.7-a).

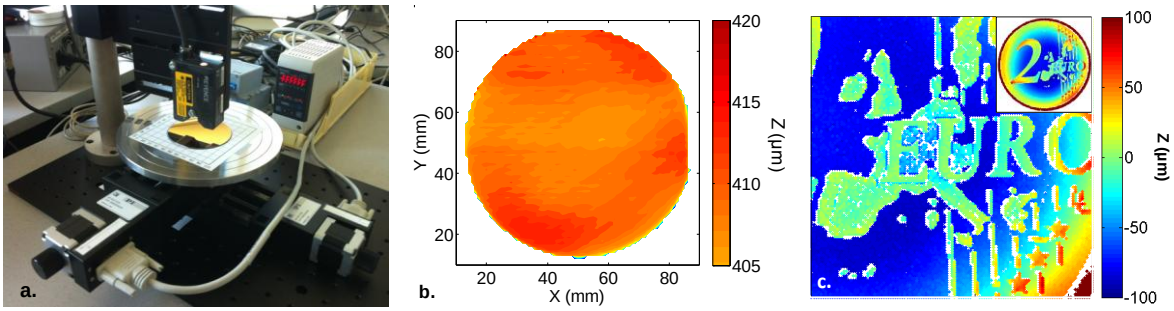


Fig. 2.7 – a. Thickness measurement setup including a laser sensor (*Keyence*) along the z-axis and two micro-positioning stages (*PI*) allowing movement in the xy plane, b. an example of thickness mapping measurement performed on a 3 inches bulk silicon wafer showing some thickness inconsistency, and c. a second example of thickness mapping performed on a 2€ coin.

2.1.2.1.4.2 *Positioning stages and laser sensor description*

The *Keyence LK-G10* laser sensor features a 2 mm measuring range along with a 20 µm diameter spot and a non-limiting resolution (Table 2.2 and Fig. 2.8-a) [233]. However once combined with the two *PI M-403.42S* micro-positioning stages featuring a 100 mm travel range and a positioning resolution in agreement with the above specifications, the limiting parameters in terms of measurement repeatability in the z-direction are the unknown rotation of the micro-positioning stages around their displacement axis. The maximum value of these angular movements is 75 µrad according to PI datasheets (Table 2.2) [234]. Taking into account a sample positioned in the center of each stage main axis (Fig. 2.8 b), the positioning error in the z-direction due to these angular movements can reach 2.9 µm at the edge of a 3 inches wafer and 1.3 µm considering a 20×30 mm sample (typical dimension of a CMOS chips). In the following sections, an error margin of about ± 1 µm will thus always be applied when considering a thickness measurement on a CMOS active sample.

Table 2.2 – Laser sensor and micro-positioning stages technical data [233], [234]

	Keyence LK-G10	*PI M-403.42S*
Measuring/travel range	2 mm	100 mm
Accuracy	0.02 %	-
Repeatability[11]	0.01 µm	~ 4 µm
Maximum velocity	50 kHz	3 mm/s
Diameter spot	20 µm	-
Minimal incremental motion	-	0.2 µm
Angular motion	-	75 µrad.

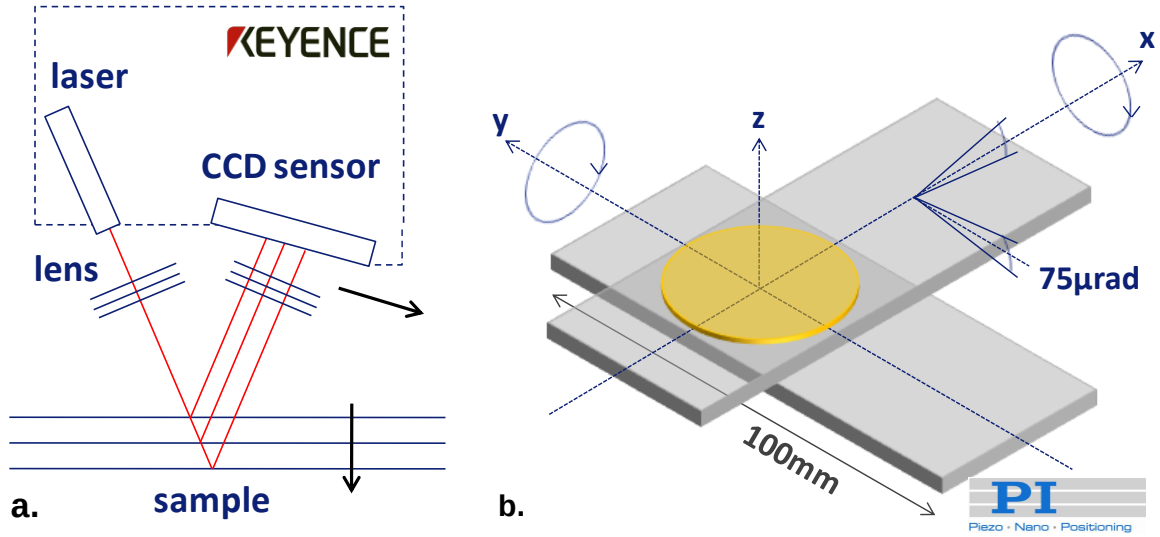


Fig. 2.8 – a. Measurement principle of the laser sensor and b. highlight of the angular motion (Table 2.2) appearing while moving the micro-positioning stages along their principal axis.

2.1.2.2 *Three-step thinning process: from 800 µm down to the buried oxide*

This section will focus on the silicon handler removal, describing in details the methods, equipments, and processes developed to perform this thinning from 780 µm of bulk silicon, down to the buried oxide. Recipes given in this section have been summarised in Table A2.1 (Appendix 2). In the following, active sample refers to the SOI CMOS chip at different steps of the thinning and transfer process.

2.1.2.2.1 Temporary bonding on a sapphire carrier

As already mentioned (see paragraph *1.1.1.2.2 - Challenges related to handling of ultra-thin wafers*), a temporary carrier is required to maintain flatness and rigidity during the complete thinning process. This temporary bonding step requires a high enough bond strength to withstand the shear stress component involved in chemical-mechanical lapping. Therefore, the selected adhesive layer (SPR220-4.5 photoresist) is hardened in a 100 °C oven for 1h. Complete recipe can be found in Table 2.3 and Fig. 2.9.

[11] Repeatability includes unidirectional repeatability, origin repeatability and divers positioning errors that appear upon reversing direction, changing speed, or load.

Table 2.3 – Description of the pre-thinning preparation process: temporary bonding of the SOI CMOS active sample on a sapphire carrier (step 2 from Fig. 2.1)

Object	Step description	Parameters
Temporary carrier	Cleaning	Chloroform ($CHCl_3$), 10 min + US*
		Acetone, 10 min + US
		Isopropanol, 10 min + US
	SPR220-4.5 filling	Perforated carrier filling with resist
Active sample	Dicing	Manual dicing using a diamond pencil
	Cleaning	Acetone, 10 min + US
		Isopropanol, 10 min + US
	Imaging	Optical microscopy imaging (reference)
	Dehydratation	200 °C, 10 min (hot plate)
	HMDS spin-coating	2000rpm/ 1000rpm.s^{-1}/ 20sec (closed lid)
	SPR220-4.5 spin-coating	3500rpm/ 1000rpm.s^{-1}/ 20sec (closed lid)
Both	Contacting	Manual contact
	Annealing	110 °C, 3 min (hot plate)
	Hardening	100 °C, 1 h (oven)
	Mapping	80×80 mm² (6400 points) => reference**

* US stands for ultrasonic agitation

** this thickness mapping provides an initial reference to compare with subsequent measurements

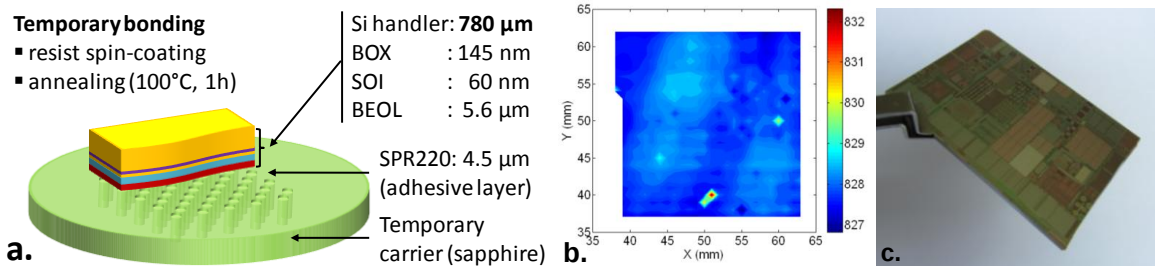


Fig. 2.9 – a. Schematic of the SOI CMOS chip sample at the second step of the process (Fig. 2.1): bonding the front side of the active sample onto a temporary sapphire carrier, and b. thickness mapping of an active CMOS chip before thinning, and c. picture of this sample after dicing.

2.1.2.2.2 Fast, coarse lapping: from 800 µm to 100 µm

The first step of the thinning process is a fast, and coarse chemical-mechanical lapping step, that reduces the bulk silicon thickness from 780 µm down to about 100 µm.

In order to perform this step, the sample should be mounted on a specific glass carrier. A thin wax layer and a wafer bonding system from *Logitech* are used to bond the active sample and temporary carrier onto this new glass carrier (Fig. 2.10-a). *Logitech* OCON-193 thin film bonding wax can subsequently be removed selectively without damaging the active sample, temporary sapphire carrier, or the temporary SPR220-4.5 adhesive layer.

The PM5 lapping & polishing system from *Logitech* can be seen in Fig. 2.10-c, and its working principle is schematically described in Fig. 2.10-b. The silicon etching results from the combined actions of the rotary plate, the alumina abrasive powder (slurry), and the rotation of the sample under a given applied force (Fig. 2.10-b).

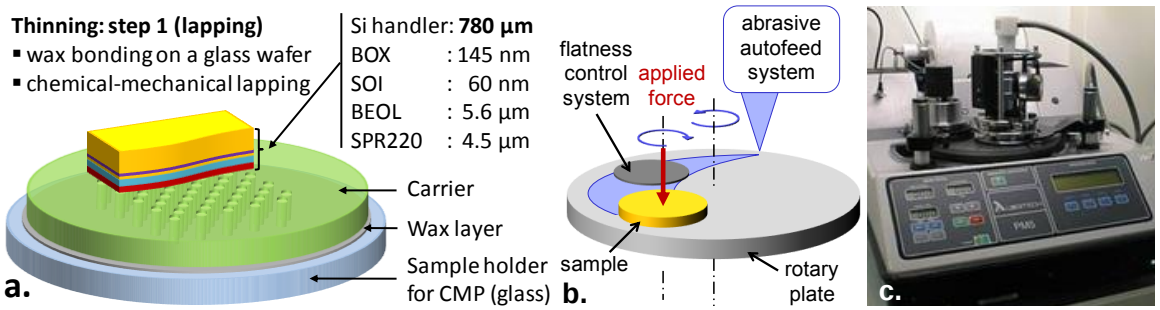


Fig. 2.10 – a. Schematic of the SOI CMOS chip sample before starting the third step of the process (Fig. 2.1): after bonding on a glass sample holder for chemical-mechanical lapping down to 100 µm, b. working principle of the chemical-mechanical lapping and polishing system, and c. picture of the Logitech PM5 Lapping System.

As presented in Fig. 2.4-a, performing a finer lapping after the first coarse and rapid lapping results in higher sample fracture strength. As a consequence, the proposed process involves a first lapping step using a 15 µm diameter alumina powder (diluted in de-ionized water, 10 w/w%) down to 200 µm. This is followed by a 3 µm diameter powder lapping down to 100 µm. Complete description of the lapping process, along with experimental parameters can be found in Table 2.4. It should be noticed that the abrasive powder dispenser was manually set to about 1 droplet per second.

Table 2.4 – Description of the first stage of the three-step thinning process: chemical-mechanical lapping (step 3A from Fig. 2.1)

Object	Step description	Parameters
Glass holder	Cleaning	Acetone, 10 min + US IPA, 10 min + US
Active sample bonded on carrier	Wax bonding on a glass holder	Wafer Substrate Bonding Unit (Logitech) OCON-193 bonding wax (Logitech) 75 °C, 10 min, Controlled heating and colling
	Mapping	80×80 mm² (6400 points) => wax layer*
	Lapping	PM5 Lapping system (Logitech) Ø 15 µm, 10 w/w%, 50 rpm, 1.0 kg Down to 200 µm Ø 3 µm, 10 w/w%, 50 rpm, 1.0 kg Down to 100 µm
	Polishing (not required)	SF_1 polishing fluid (Logitech) 70 rpm, 1.0 kg, 10 min
	Mapping	80×80 mm² (6400 points) => lapping*
	Wax removal	OCON-178 Cleaning fluid (Logitech) 70°C, 30 min Isopropanol rinse, 10 min

* this term describes what can be extracted by substracting a measurement to the previous one

Due to the fact that several parameters are manually controlled (abrasive flow rate, sample holder rotation speed, applied force), the etch rate cannot be accurately determined. The remaining silicon thickness is therefore regularly measured to precisely control the resulting thickness. A typical lapping characteristic is presented in Fig. 2.11-a, where the thickness reduction from 800 µm to 200 µm with 15 µm diameter abrasive powder can be seen, followed by a 3 µm diameter powder lapping, down to 100 µm, and a subsequent

polishing step using commercial SF_1 polishing fluid from *Logitech*. Fig. 2.11-b presents the impact of applied force and sample area on the etch rate.

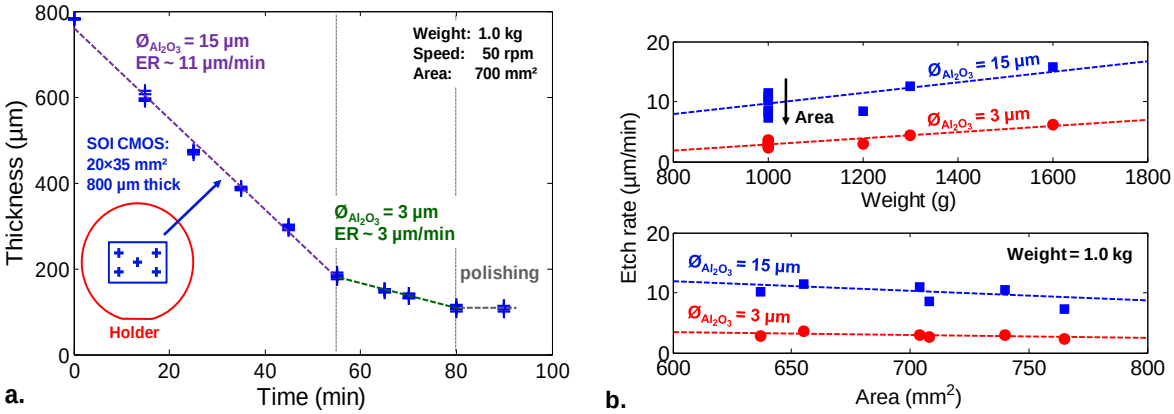


Fig. 2.11 – a. Typical lapping characteristic showing the thickness of a SOI CMOS chip (measured at 5 different locations) as a function of time: abrasive Al_2O_3 powder featuring a 15 µm diameter are first used from 780 µm down to 200 µm, resulting in a high etch rate (e.g. 11 µm/min here), followed by lapping with 3 µm diameter alumina powder down to 100 µm, at 3 µm/min (subsequent polishing can be performed). b. Impact of applied weigth (top) and sample area (bottom) on etch rates, for abrasive alumina powder featuring both 15 µm and 3 µm diameter.

Fig. 2.12 describes the impact of the first thinning step on the thickness of an active sample: from an initial ~800 µm thick sample featuring homogeneous thickness (Fig. 2.12-a) towards a sample thinned down to ~100 µm and showing an increased thickness dispersion (Fig. 2.12-b). In particular, the centre of the thinned sample is thicker that its edges (Fig. 2.12-d). Fig. 2.12-c provides a profile of the sample at different stages of the thinning process.

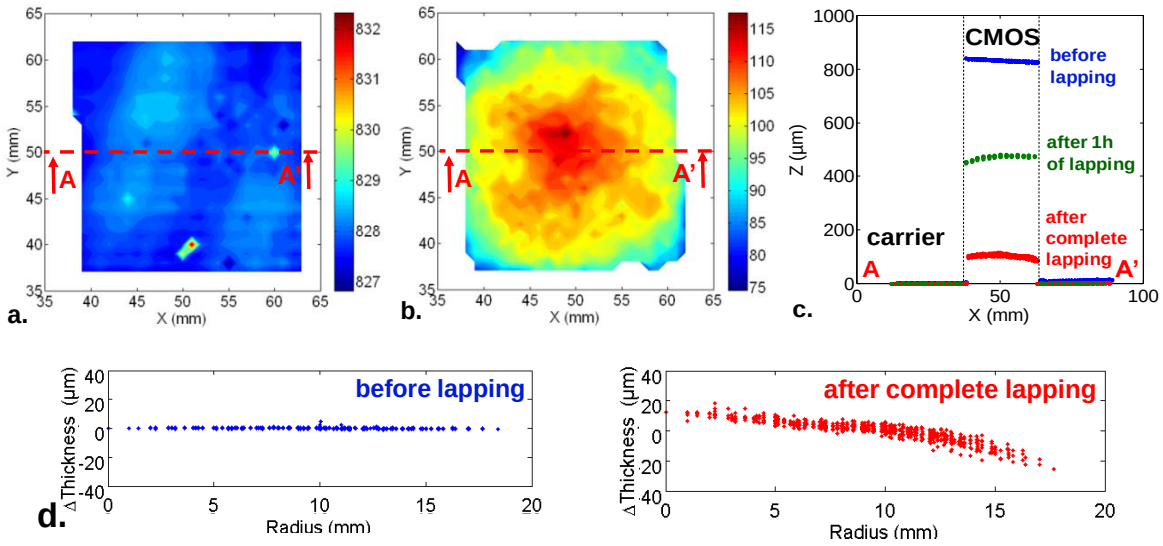


Fig. 2.12 – a. Thickness mapping of an active CMOS sample bonded on its temporary carrier, before chemical-mechanical lapping showing an average thickness of 828 µm (including the adhesive layer), b. thickness mapping on the same sample after completing this first thinning step down to 100 µm, an increased thickness dispersion can be noticed, c. profile of this sample before lapping (blue), after one hour of lapping using a 15 µm diameter abrasive powder (green), and after completing this thinning step (red), and d. distance between measured data and fitted average plane as a function of sample radius before and after chemical-mechanical lapping.

2.1.2.2.3 Soft etching: from 100 µm to 20 µm

After performing a chemical-mechanical lapping, a stress relief step is conducted by wet etching the sample back side from 100 µm down to about 20 µm. A mixture of hydrofluoridric (HF) and nitric (HNO_3) acids, 10:90 v/v%, referred to as HNA solution, is used. However, in order to ensure that the HNA solution does not degrade the active SOI-CMOS sample, a protective wax layer is first deposited. Wax W from *Apiezon* bas been specifically design to be acid resistant and has been used to prevent HNA solution from etching critical part of an immersed sample [235], [236]. Due to the fact that the sapphire temporary carrier used in this work feature 1 mm diameter holes, protective wax has to be deposited both on the back side of the sapphire carrier and around the edges of the active sample (Fig. 2.13-a). The deposited wax thickness should be large enough to protect the temporary SPR220 adhesive, BEOL, SOI and BOX layers. This can be seen in Fig. 2.13-b, where a thickness mapping of a wax protected sample is presented. Finally, Fig. 2.13-c demonstrates that HNA solution does not degrade the wax layer: the profile of the sample before (green), and after (red) wet etching is presented.

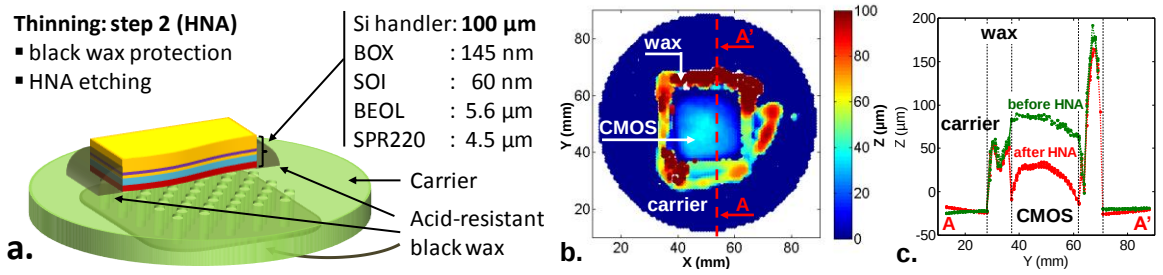


Fig. 2.13 – a. Schematic of the SOI CMOS chip sample during the third step of the process (Fig. 2.1): after chemical-mechanical lapping down to 100 µm, and subsequent acid-resistant wax coating to protect the front side and the edges of the active sample. b. Thickness mapping after wax coating, demonstrating complete coverage of the side walls of the active CMOS sample, and c. profile along the AA' axis, showing that the wax coating is thicker that the CMOS sample.

Magnetic stirring, along with manual vertical agitation is performed in order to enhance the silicon etch rate (see Fig. 2.5, and paragraph 2.1.2.1.2.3 Isotropic wet etching: HNA solution) and also to reduce micromasking arising from vapour phase by-products forming bubbles and therefore impeding further etching [237], [238]. Regular thickness measurements are performed to ensure that the wet etching step stops before reaching the buried oxide layer. Detailed experimental parameters are summarised in Table 2.5.

After performing HNA etching down to about 20 µm (thickness inhomogeneity can be seen in Fig. 2.14), the protecting wax layer is removed in OCON-178 cleaning fluid from *Logitech*, ensuring a selective dissolution that does not degrade the temporary photoresist adhesive layer. A subsequent thickness mapping gives the resulting sample profile and etched thickness (Fig. 2.14-a-b). It can furthermore be noticed in Fig. 2.14-c that the thickness variation is slightly increased by this wet etching step. In the considered example, the center of the sample is almost 60 µm thick, whereas the edges are thinner, close to 20 µm. This thickness inhomogeneity will however be corrected by the last step of the proposed thinning process using dry isotropic XeF_2 etching.

Table 2.5 – Description of the second stage of the three-step thinning process: HNA etching (step 3B from Fig. 2.1)

Object	Step description	Parameters
Active sample bonded on carrier	Acid-resistant wax coating (front side)	Wax W (Apiezon) Front side (around the active chip edges) Manual deposition or spin-coating
	Thickness measurement	Wax thickness measurement (until wax protects the BOX layer)
	Mapping	80×80 mm² (6400 points) => wax layer*
	Acid-resistant wax coating (back side)	Wax W (Apiezon) Back side (covering the carrier holes) Manual deposition or spin-coating Visual inspection
	HNA etching	49% HF : 65% HNO_3 – 10 : 90 (v/v%) Magnetic stirring, 100 rpm Manual vertical agitation Sample rotation (90°) every minute Down to 20 µm
	DI water rinse	De-ionized (DI) water rinse, 5 min
	Acid-resistant wax stripping	OCON-178 Cleaning fluid (Logitech) 70°C, 30 min Chloroform ($CHCl_3$), 1 min Isopropanol rinse, 10 min
	Mapping	80×80 mm² (6400 points) => HNA etch*

* this term describes what can be extracted by substracting a measurement to the previous one

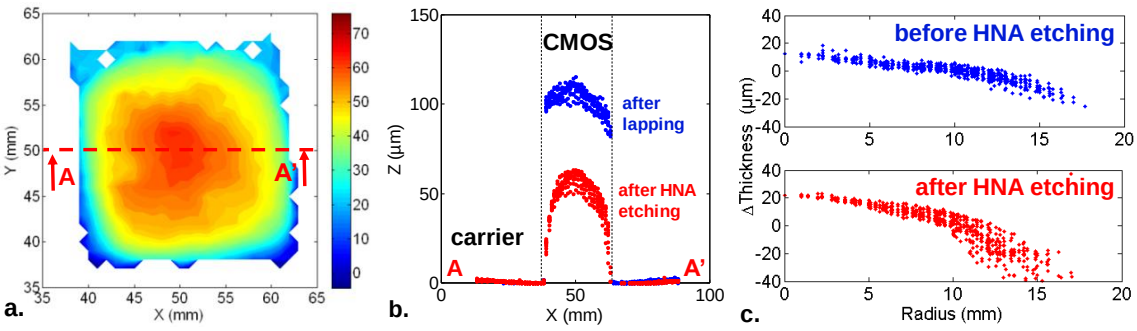


Fig. 2.14 – a. Thickness mapping of an active CMOS sample after HNA etching, b. profile of this sample before HNA etching, i.e. after lapping (blue), and after completing wet etching (red), and c. distance between measured data and fitted average plane as a function of sample radius before (blue) and after (red) wet etching in HNA solution.

2.1.2.2.4 Selective cleaning of the remaining bulk silicon: from 20 µm to the BOX

The last step of the thinning process consists in a highly selective scavenging of the remaining silicon without damaging the buried oxide layer. Due to the high Si:SiO_2 selectivity, it is important to start this step by removing the oxide present on the sample surface (due to HNA oxidation and native oxidation of silicon in air at room temperature). This is performed by quickly diping the sample into diluted HF (1 v/v%) for one minute prior to loading in the XeF_2 etching system. Schematic of the prepared sample and etching

system can be seen in Fig. 2.15-a and Fig. 2.15-b respectively. Experimental parameters are summarised in Table 2.6.

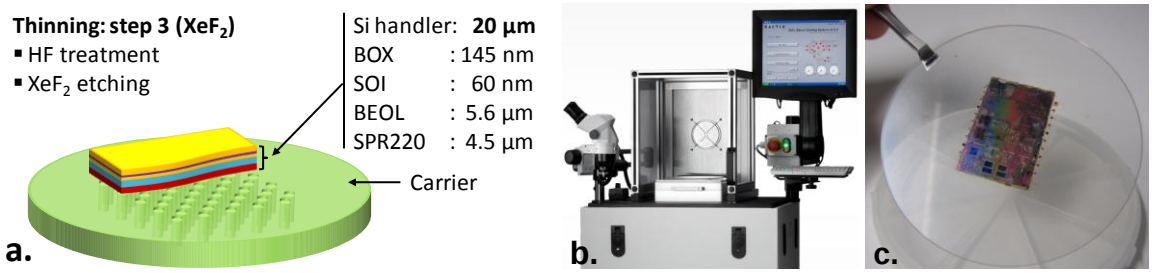


Fig. 2.15 – a. Schematic of the SOI CMOS chip sample during the third step of the process (Fig. 2.1): after HNA etching down to 20 µm, and subsequent surface treatment in HF, b. picture of the *XACTIX* X3 Series Xetch System, and c. picture of the active sample on its temporary carrier after XeF_2 ethcing down to the BOX.

Table 2.6 – Description of the last stage of the three-step thinning process: XeF_2 etching (step 3C from Fig. 2.1)

Object	Step description	Parameters
Active sample bonded on carrier	Surface preparation	1% HF, 1 min DI water rinse, 1 min
	XeF_2 etching	Etch pulse duration: 10 sec Expansion pressure: 3.0 Torr Output pressure: 800 mTorr
	Imaging	Optical microscopy imaging (back side)
	Mapping	80×80 mm² (6400 points) => XeF_2 etch*

* this term describes what can be extracted by substracting a measurement to the previous one

Fig. 2.16-a presents a thickness mapping of the active sample after XeF_2 etching. Some data points are missing, possibly due to bad reflection of the laser on the thinned sample surface. However, it can be seen in Fig. 2.16-c that this last step compensates the thickness inhomogeneity generated by previous etching steps. Dispersion after XeF_2 etching is attributed to the fact that our home-made measurement setup is unable to take into account reflection on a complex stack. Absence of remaining silicon is confirmed in Fig. 2.24-b.

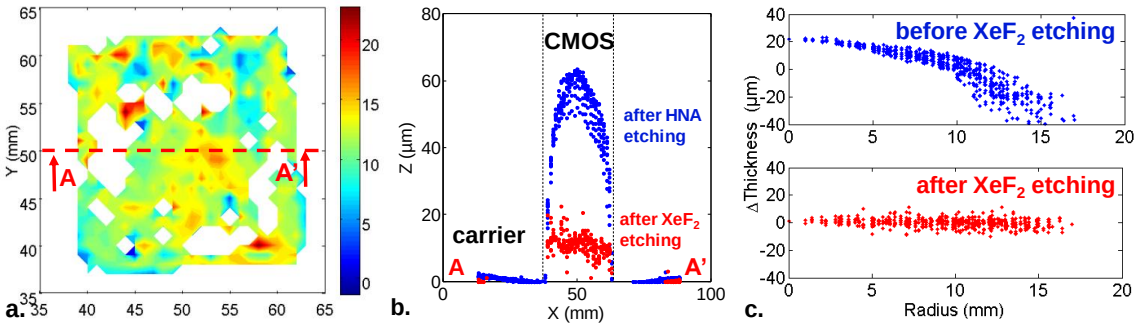


Fig. 2.16 – a. Thickness mapping of an active CMOS sample after XeF_2 etching, b. profile of this sample before XeF_2 etching, i.e. after HNA ethcing (blue), and after completing isotropic dry etching (red), and c. distance between measured data and fitted average plane as a function of sample radius before (blue) and after (red) dry etching in XeF_2.

2.1.2.2.5 Summary of the initial substrate removing

As a conclusion to this section, Fig. 2.17 illustrates the complete bulk silicon removal process, showing a thickness mapping at different stages of this procedure, in addition to the thickness variation as a function of the sample radius.

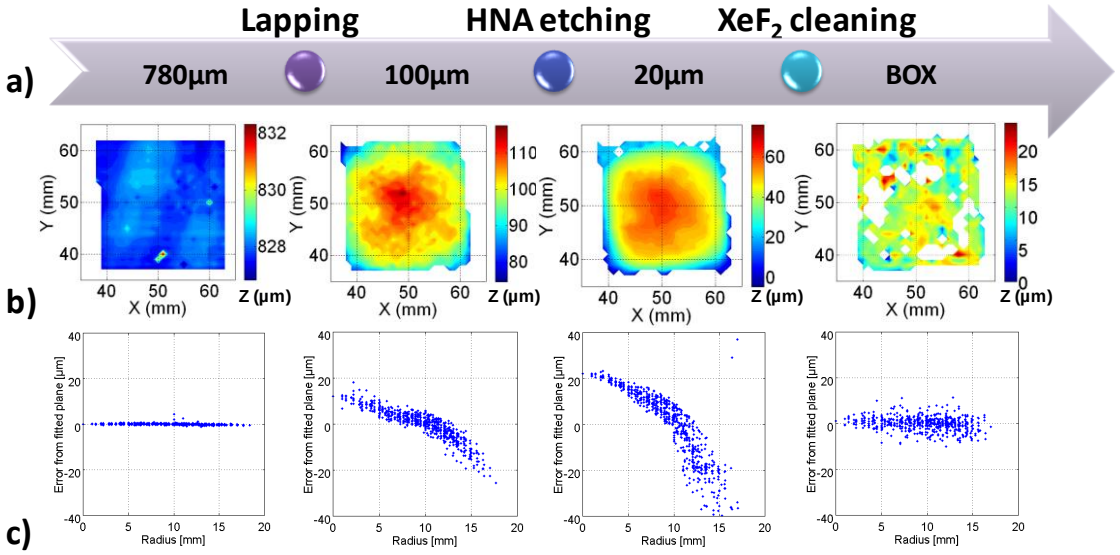


Fig. 2.17 – a. Summary of the three-step etching process, b. active SOI-CMOS sample thickness mapping corresponding to the different steps and c. associated thickness versus radius characteristics.

2.1.3 Step 2: Transfer-bonding the thinned die onto a plastic film

2.1.3.1 *First considerations about adhesive layers*

2.1.3.1.1 Adhesive layers requirements

As already mentioned (Fig. 2.1), the proposed thinning and transfer process involves two adhesive layers: one temporary to bond the active sample front side onto a carrier and one permanent adhesive layer to bond the back side of the thinned active sample onto a flexible handler. Two requirements arise from this process: i) the temporary resist should be removed selectively, without damaging the permanent bond to the flexible plastic film, and ii) the temporary adhesive layer should be able to withstand the aforementioned thinning process.

2.1.3.1.2 Thinning process impacts on adhesive layer

The proposed three-step thinning process involves two phenomena that can degrade the temporary adhesive layer: shear stress generated during chemical-mechanical lapping, and chemical etching due to the immersion in HNA solution. Indeed, as already mentioned, the XeF_2 etching is highly selective to photoresist materials. Therefore no degradation of the bonding has been noticed after dry etching.

This first consideration resulted in the hardening of the SPR220 adhesive layer. Without a long thermal anneaning (1h in a 100 °C oven), the bond strength was not high enough to

withstand the lapping step and sometime resulted in debonding of the active sample from its carrier on the rotary plate. The drawback of this solution is that enhanced bond strength also means harder debonding (step 5 in Fig. 2.1) leading to lower selectivity with respect to permanent bonding. To cope with this effect, a perforated temporary carriers was used in this work, as presented hereinbefore. This enables a faster release of the active sample from the carrier by enhancing dissolution of the photoresist layer through the 1 mm diameter holes of the carrier.

The second consideration was solved by protecting the edge of the photoresist and active sample with an acid resistant wax (Fig. 2.13). This enables to prevent the HNA solution from attacking the temporary adhesive layer from the side. Furthermore, depositing another layer of the same acid resistance wax on the back side of the carrier prevents HNA from etching photoresist through the perforated carrier.

2.1.3.1.3 Organic material related requirements

As explained in the first chapter (Table 1.3), the use of a plastic handler limits thermal budgets to low values (typically below 150 °C). This means that, after bonding the plastic film onto the back side of the thinned active sample, the remaining steps should be thermally and chemically compatible with the organic material. Especially, chemicals used to dissolve the temporary adhesive layer and release the flexible active sample from its sapphire carrier should not degrade the plastic handler. The proposed process, detailed in paragraph 2.1.3.2 Bonding onto a plastic handler, takes these considerations into account.

2.1.3.1.4 Electrical characterization related requirements

Another point to consider is the measurement of the flexible SOI-CMOS devices (transistors, passive components, or complex circtuits), and especially high frequency (HF) characterization. Achieving a good contact between RF probes and the sample aluminium pads is not always straightforward when considering soft, flexible, or even unplanar (see chapter 3) devices. HF characterization requires a contact of good quality for the full frequency range, i.e. from 500 MHz to 110 GHz in this work.

The use of an adhesive film from the *3M* company as a flexible plastic handler was therefore not possible. The reason is that it features a thick (~20 µm) pressure sensitive adhesive layer. Probing thin aluminium contact pads on this thick and soft material results in irreversible damages done to the metallization before achieving a good quality contact. This is illustrated in Fig. 2.18 with DC probes.

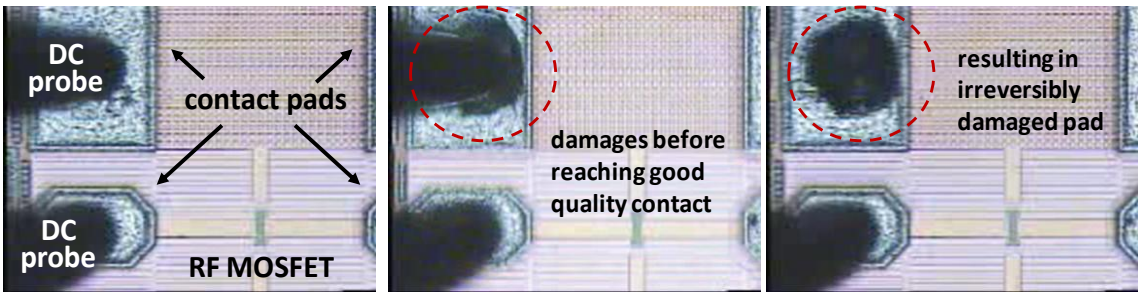


Fig. 2.18 – Illustration of the effect of a thick and soft material below the micrometer scale metallization of a thinned sample transferred onto a *3M* adhesive film: (from left to right) a DC probe is slightly contacted to the ground aluminium pad, the contact quality is however not sufficient to characterize the device, and the contact pad is irreversibly damaged before achieving a good contact.

Unbonded areas, as illustrated in Fig. 2.19-a, lead to similar troubles. If the thin active sample is not correctly bonded below the probes, it may then locally be subjected to high level of strain when lowering the probes. This prevents from characterizing devices in unbonded areas. In order to avoid this phenomenon, bonding of the active sample onto a plastic phandler is performed under vacuum and the permanent adhesive layer is heated above its glass transistion temperature before contact (Fig. 2.20-b).

Other problems that may occur during the transfer process are also shown in Fig. 2.19. After bonding the active sample onto a plastic handler, the temporary adhesive layer should be dissolved to release the carrier. Using a plain, unperforated carrier may result in lower selectivity between the two adhesive layers, due to longer dissolution time of the temporary bonding. As a consequence, part of the active sample is transferred and part of it remains on the carrier (Fig. 2.19-b). Overheating is also damageable as mismatch between the thermal properties of the organic material of the handler and the inorganic materials of the active sample can lead to buckling of the plastic film. This can induce therefore cracking and debonding of the sample (Fig. 2.19-c).

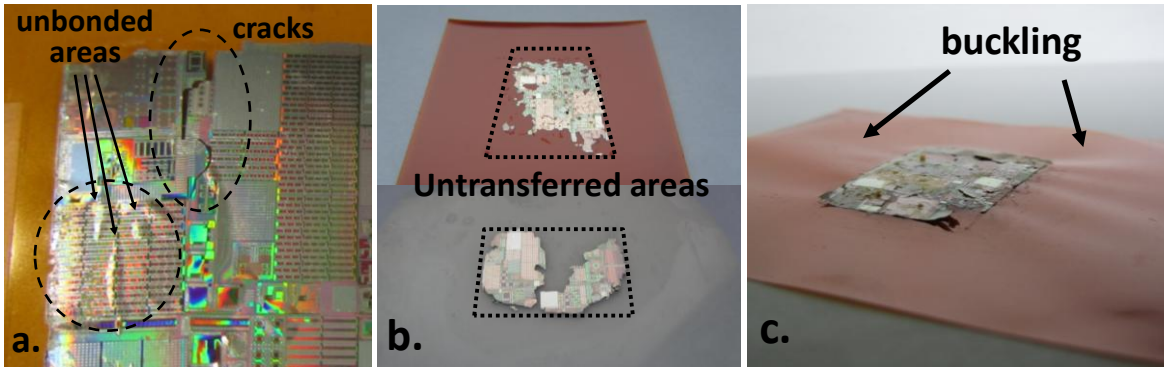


Fig. 2.19 – Illustration of various problems that may arise when transferring a thinned active sample onto a polyimide handler: a. unbonded areas, or gas bubbles trapped between the sample and the handler preventing from probig devices on these areas, and cracks, b. untransferred areas that may be due to a low selectivity between the adhesive layers, and c. buckling of the thin polyimide handler (and resulting debonding and crack in the active sample) due to thermal mismatch.

2.1.3.2 *Bonding onto a plastic handler*

2.1.3.2.1 SU-8 thermo-compression bonding

In order to cope with the above-mentioned problems, a thermocompression bonding process was developed using SU-8 epoxy as an adhesive layer (Fig. 2.20). After spin-coating SU-8 onto the back side of the thinned active sample, the excess epoxy on the carrier was manually removed (to prevent bonding between the plastic handler and the carrier). Contact and bonding were subsequently conducted under vacuum in a wafer bonding system (SB6e from *SÜSS MicroTech*, Fig. 2.20-c). The bonding step involves first a ramp of temperature to soften the epoxy layer. The thinned active sample and plastic handler are then brought into contact and subjected to a bonding temperature (110 °C) and mechanical pressure (500 mbar) for 30 minutes (Fig. 2.20-b). Controlled cool down of the bonded stack at a relatively low rate (< 1 °C/min) and under the applied pressure limits the thermal mismatch effect. This process is summarised in Table 2.7 and Fig. 2.20-b.

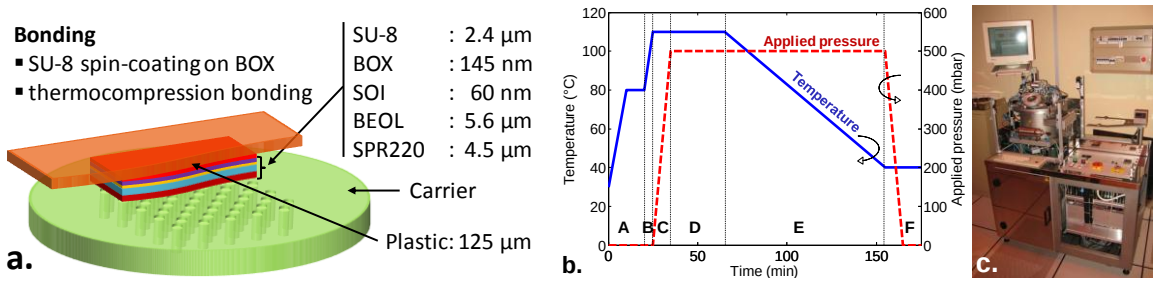


Fig. 2.20 – a. Schematic of the SOI CMOS chip sample at the fourth step of the considered process (Fig. 2.1): bonding the thinned die onto a polyimide film, b. description of the vacuum thermocompression bonding process: A) increase of temperature up to 80°C and pumping of chamber down to primary vacuum level (10^{-5} mbar), B) wait for 10 min to ensure a good vacuum level, and then increase of temperature up to 110 °C, C) then contact sample to plastic handler and apply bonding pressure (500 mbar), D) bonding step (30 min), E) controlled cooling, and F) release applied pressure and vent chamber. c. picture of the SUSS MicroTech SB6e wafer bonding system.

Table 2.7 – Description of the bonding process: thermocompression bonding (step 4 from Fig. 2.1)

Object	Step description	Parameters
Polyimide film	Cleaning	Acetone, 10 min + US Isopropanol, 10 min + US
Active sample bonded on carrier	SU8-2002 spin-coating	500rpm/ 1000rpm.s^{-1}/ 30sec (closed lid) 2000rpm/ 1000rpm.s^{-1}/ 30sec (closed lid) Manually removing excess resist
	Annealing	80 °C, 2 min + 110 °C, 3 min (hot plates)
	Bonding	SB6e wafer bonding (SÜSS MicroTech) Vacuum thermocompression 30 min, 110 °C, 500 mbar, 10^{-5} mbar

2.1.3.2.2 Room temperature bonding

A room temperature bonding and transfer process was also developed in this work. It started from the observation that strain generated by thermal mismatch during the bonding step could be reduced if bonding occurs at room temperature. Polymethyl methacrylate (PMMA) was used as an adhesive layer in this procedure because unbaked PMMA layer develops sufficient adhesion at room temperature.

However, this room temperature bonding requires that the release of the active sample from the sapphire carrier takes place before permanent bonding. Indeed, the temporary adhesive layer cannot be removed selectively with respect to the unbaked PMMA layer. The 5.6 µm thick active sample should therefore be handled without its sapphire carrier during one process step (Fig. 2.21-a-b).

Another advantage of this bonding process in comparison to the thermocompression is the possibility to bond thinned active chips onto unplanar surfaces, as shown in Fig. 2.21-c on the curved surface on a cylinder. Direct bond of active samples onto curved surfaces without first attaching them to a plastic handler changes the strain distribution. This is a promising solution for applications requiring rigid, non planar electronics.

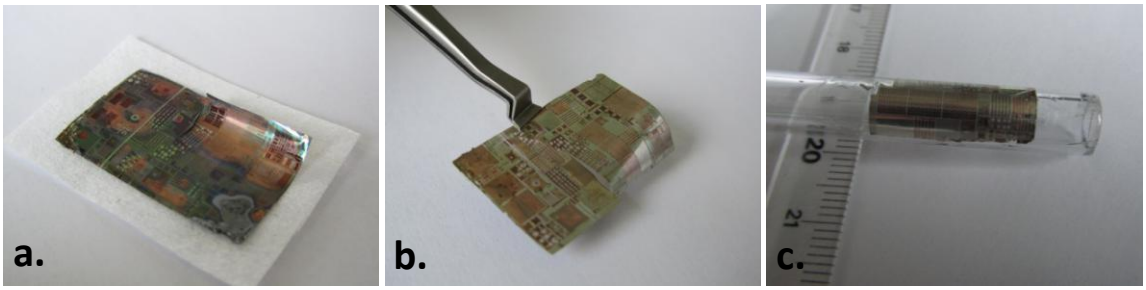


Fig. 2.21 – a. Back side of a thinned active SOI-CMOS sample (5.6 µm thick), the first level of mettalization can be seem through the buried oxide layer, b. same sample seen from the front side, bendingon on corner of the sample can be noticed, and c. thinned CMOS chip bonded onto a 3 mm curvature radius cylinder.

2.1.3.2.3 Final step: release from carrier and cleaning

In the case of an active sample bonded onto a plastic handler using the SU-8 thermocompression bonding process (Table 2.7, and Fig. 2.20), the last step of the thinning and transfer process is the release from the temporary sapphire carrier. This can be performed by simply dipping the bonded stack (carrier/sample/handler) into resist stripper to dissolve the SPR220 temporary adhesive layer selectively to the SU-8 layer. Detailed process in presented in Table 2.8.

Table 2.8 – Description of the release process: final step toward the realization of a flexible SOI CMOS chip (step 5 from Fig. 2.1)

Object	Step description	Parameters
Active sample bonded on plastic	Release	Remover 1165, room temperature
		Acetone, 10 min
		Isopropanol, 10 min
	Cleaning	O_2 plasma, 10 min
	Imaging	Optical microscopy imaging (front side)

After bonding to a plastic handler and releasing the active sample from its temporary carrier, a thin flexible SOI CMOS chip is obtained. A final cleaning step is then required to remove photoresist residues from the front side of the sample for proper electrical characterization. This cleaning step of the front side of the CMOS chip is performed in O_2 plasma (Table 2.8), and results in a clean flexible sample (Fig. 2.22-b).

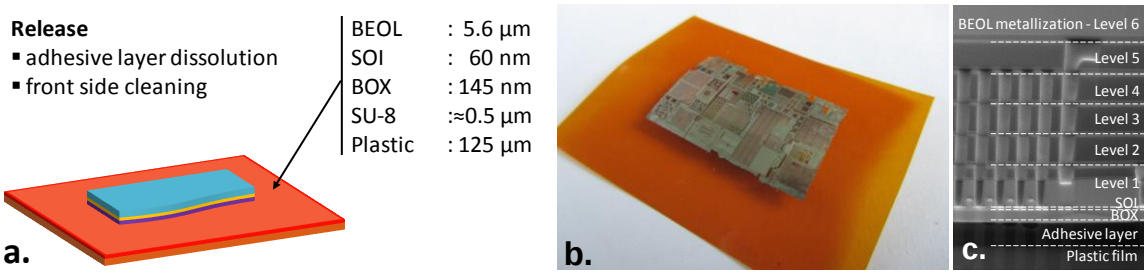


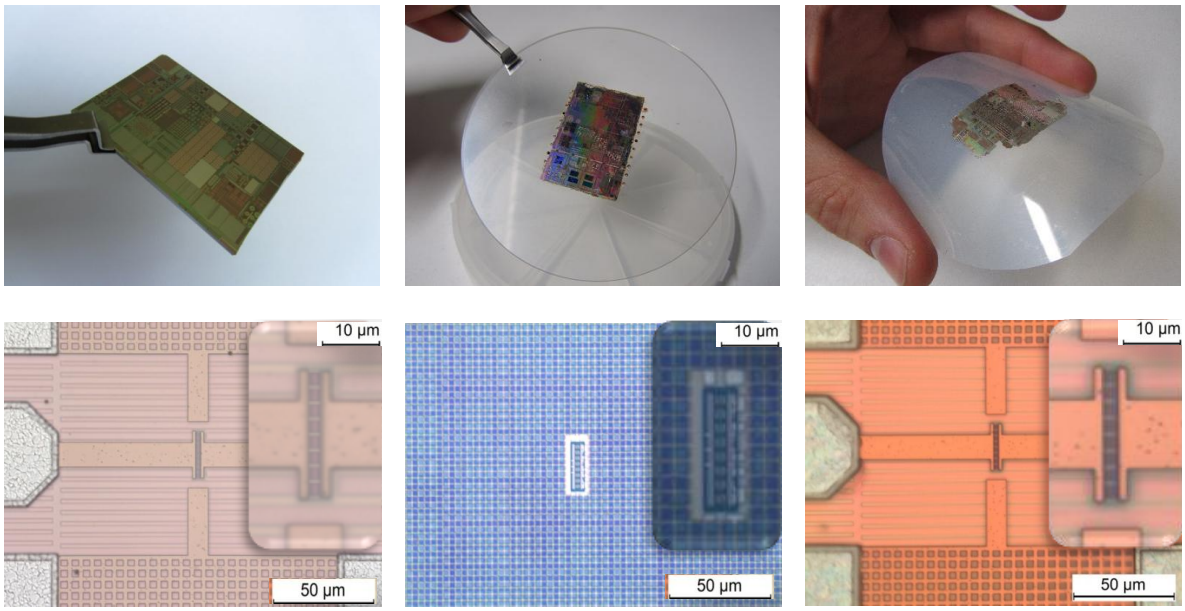
Fig. 2.22 – a. Schematic of the SOI CMOS chip sample at the last step of the process (Fig. 2.1): releasing the flexible active SOI CMOS sample from the temporary carrier, b. picture of a CMOS chip after thinning and transfer onto a 50 µm thick polyimide (PI) fillm, and c. SEM cross-section.

2.1.4 Conclusion on the fabrication process

The fabrication steps to provide SOI-CMOS technology with mechanical flexibility has been presented in this section. Starting from a thick and rigid SOI material featuring CMOS devices and circuits, we developed a fabrication process to thin the initial substrate down to 5.6 µm and transfer active dies onto a flexible organic film. This discussion will be concluded here with several pictures summarising this process (detailed information of the complete process is available in Table A2.1, Appendix 2).

Fig. 2.23 shows pictures and optical microscopy images of an active sample before starting the proposed fabrication process (Fig. 2.23-a), after completely etching the back side of the initial SOI substrate (Fig. 2.23-b), and after transfer of the thinned active sample onto a plastic handler (Fig. 2.23-c). The second and third steps illustrate the fact that the no degradation is visible after removing the silicon handler and transferring onto a flexible film.

The RF MOSFET presented here features 8 cells, each containing 8 unitary gate fingers (the same device will be characterized in next section). The 8-finger cells can be seen in inset of the optical microscopy images, from the front side in Fig. 2.23-a and Fig. 2.23-c, and from the back side after performing the etching process in Fig. 2.23-b.



a. before etch (front side) **b.** after etch (back side) **c.** after transfer (front side)

Fig. 2.23 – Pictures (top), and optical microscopy images (bottom) of a diced 65 nm node SOI CMOS chip from STMicroelectronics at different stages of the thinning and transfer process: a. before etch, i.e. after CMOS processing and dicing, but before starting the thinning and transfer process, this is the reference state in this work, b. after complete removal of the bulk silicon handler (images show the back side of the chip, as the front side is still bonded to the temporaty carrier), and c. after completing the transfer process by bonding the thinned chip onto a polyethylene naphthalate film and releasing the carrier: a flexible SOI CMOS chip is achieved.

In order to provide higher resolution characterization and to demonstrate that no visible degradation arises from the proposed fabrication process, focused ion beam (FIB) trenches were performed in the sample to enable electron microscopy imaging, as presented in Fig. 2.24. The 6 levels of interconnection can be seen in Fig. 2.24-b that shows a scanning electron microscopy (SEM) cross-section of a flexible RF-MOSFET (cross-section location is highlighted in red in Fig. 2.24-a). Fig. 2.24-c and Fig. 2.24-d present transmission electron microscopy (TEM) images of the same cross-section, demonstrating that the front-end of the flexible device remains unaltered.

Electrical measurements (as presented in next section) will confirm that no major degradation arises from the proposed fabrication process.

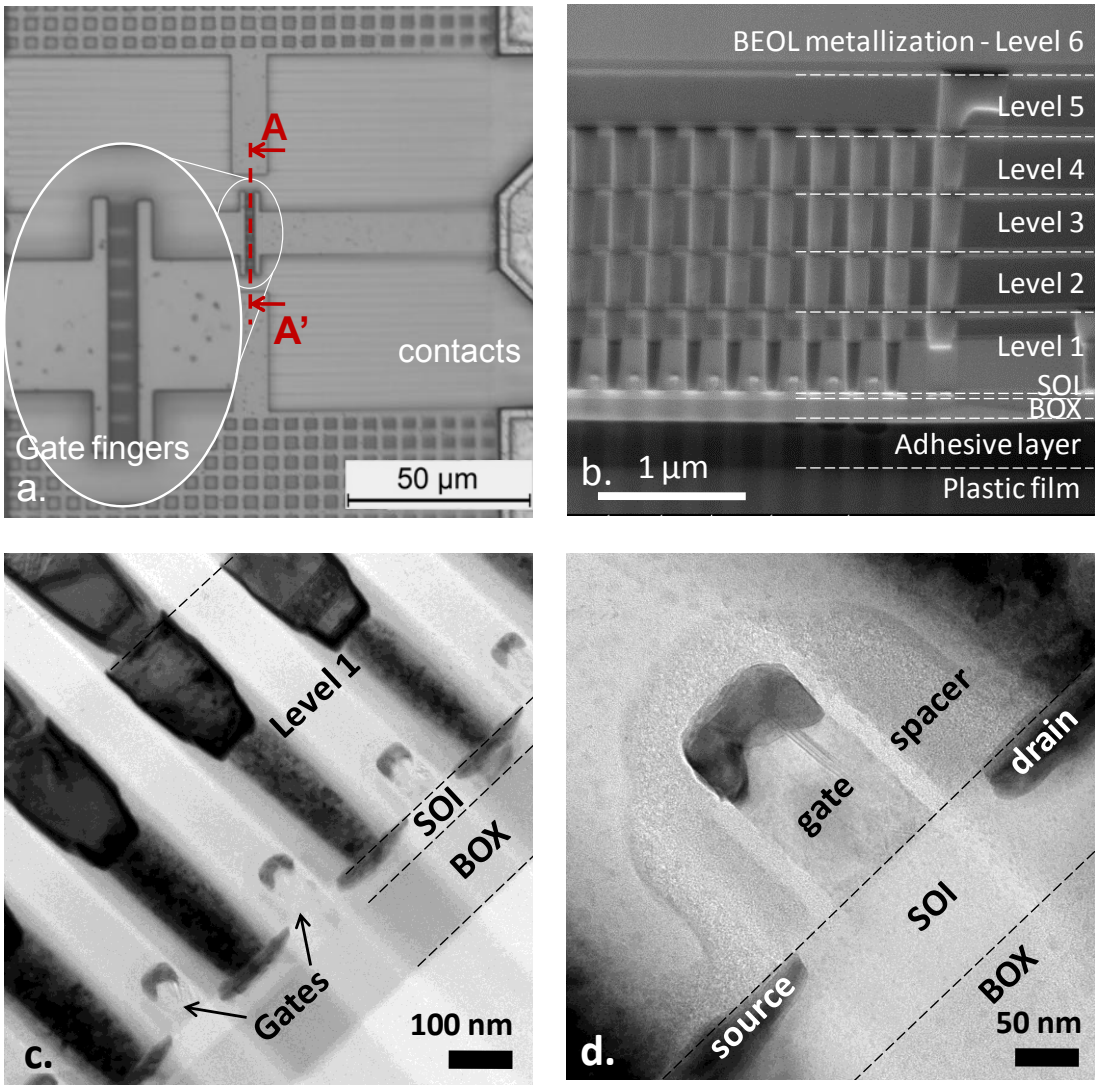


Fig. 2.24 – a. Optical microscopy image of a flexible RF-MOSFET, showing aluminium contact pads, access line, and gates in inset, b. SEM cross-section along the AA' axis highlighting the stack of the flexible transistor: from the polyimide handler, adhesive layer, BOX, SOI, towards le last level of metallization, c. TEM image of the same stack, showing the front-end-of-line, and d. TEM image showing one unitary gate finger in details.

2.2 Electrical performance of CMOS dies on organic films

2.2.1 SOI RF-MOSFET characterization on organic substrate

After transfer-bonding thinned SOI CMOS active dies onto organic films, electrical characteristics of these flexible SOI RF-MOSFETs are compared hereinafter with their rigid counterparts. Measurements presented in this section have been performed mainly on 64-gate-fingers n- and p-MOSFETs, featuring a 60nm gate length and a unitary finger width of 1µm. Flexible devices on which these static and radio-frequency characterizations have been performed were transfer-bonded onto a 125µm thick p*olyethylene naphthalate* (PEN) substrate using the SU-8 thermo-compression bonding technique described in previous section. Without any other indication, all measurements presented in this section will refer to this specific transistor geometry and flexible substrate.

Static measurements have first been performed to demonstrate that the flexible SOI RF-CMOS realized in this work would still feature transistor-like electrical behaviors and furthermore that static characteristics are completely similar to their rigid counterparts. In a second step, radio-frequency measurements will be presented along with the extraction of the small signal equivalent circuit (SSEC) following the methodology presented in former chapter and demonstrating RF figures-of-merit competitive with 65nm node rigid technology. Finally, high-frequency noise characterization of the flexible CMOS dies will fully demonstrate RF noise figures-of-merit in agreement with the rigid version of the CMOS devices. To our knowledge, these radio-frequency characteristics outperform the previous state-of-the-art of high frequency flexible electronics [17].

2.2.1.1 *DC characterization*

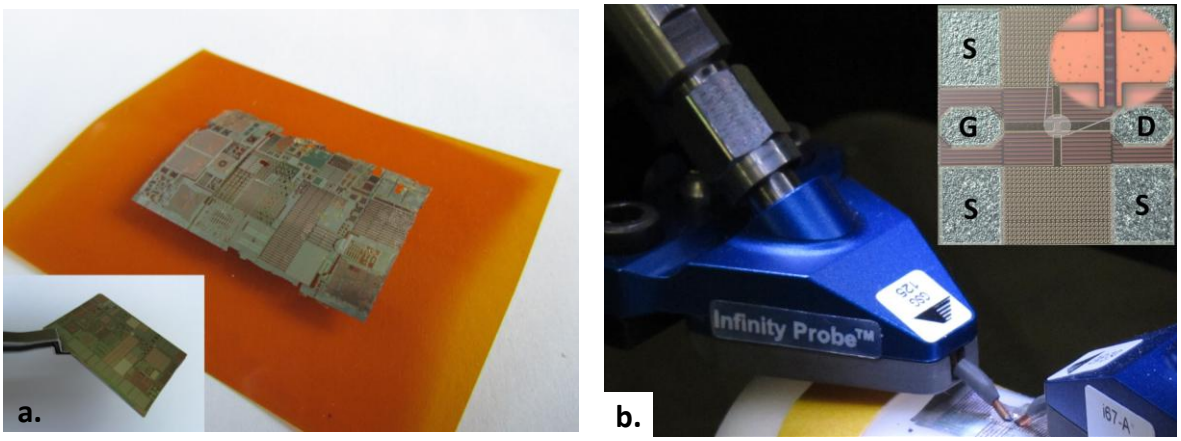


Fig. 2.25 – a. Picture of a flexible SOI RF-CMOS die, thinned and transferred onto a 50µm thick PI (polyimide) film, inset: initial rigid SOI RF-CMOS die, and b. RF Infinity probes used for static and radio-frequency measurements on rigid and flexible CMOS dies, inset: microscope image of a RF-MOSFET including source (S), drain (D) and gate (G) contact pads along with a zoom in the gate finger cells.

DC characterizations have been performed considering that both rigid and flexible CMOS dies (Fig. 2.25-a) were maintained flat on a chuck connected to the ground. 125µm pitch RF Infinity probes were connected to the aluminum gate and drain contact pads, the source being connected to the ground (Fig. 2.25-b).

2.2.1.1.1 Static characteristics of n- and p-MOSFETs on plastic

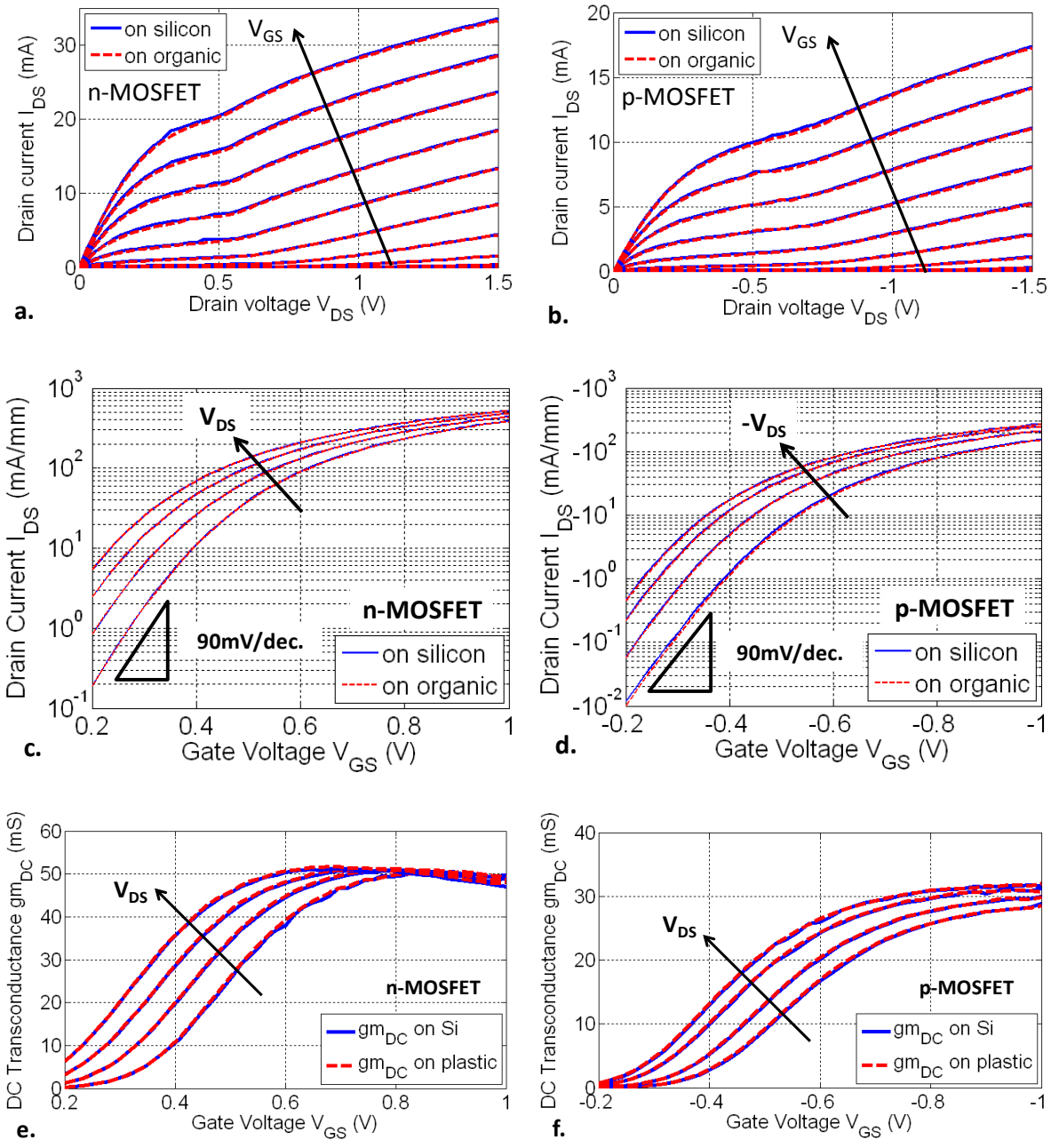


Fig. 2.26 – Static characteristics of n- and p-MOSFETs on their initial rigid substrate (blue lines) and after transfer onto an organic film (red dashed lines), demonstrating high level of on-state drain current and static transconductance.

Fig. 2.26 presents static characteristics of n- and p-MOSFETs both on their initial rigid SOI wafer (blue lines) and after transfer onto an organic film (red dashed lines). Completely similar behavior is demonstrated for devices on rigid and flexible SOI substrates, leading to the demonstration of flexible transistors with currents and transconductance levels competitive with their rigid counterparts. n-MOSFETs on plastic featuring 33mA (521µA/µm) of drain current at V_{DS}=1.5V and V_{GS}=1.2V and 52mS (813µS/µm) of static transconductance at V_{DS}=1.2V and V_{GS}=0.8V are presented here for the first time (to our best knowledge). Flexible p-MOSFETs similarly featuring high values of drain current (-270µA/µm) and static transconductance (495µS/µm) at V_{DS}=-1.5V, V_{GS}=-1.0V are reported. These figures are summarized for n- and p-MOSFETs on their initial substrate and after transfer onto a plastic film in Table 2.9, along with the static figures-of-merit I_{ON}/I_{OFF} ratio, drain induced barrier lowering (DIBL) and subthreshold slope (SS). The off-state leakage current I_{OFF} is defined as the drain current I_{DS} at V_{GS}=0V and $V_{DS}=V_{DD}$, i.e. V_{DS}=1.2V for n-MOSFETs and V_{DS}=-1.5V for p-MOSFETs. The threshold voltage V_{th} is extracted at the same drain voltage $V_{DS}=V_{DD}$. The DIBL value is measured as the difference in threshold voltage V_{th} between low and high drain voltage: respectively V_{DS}=±200mV and V_{DS}=±1.0V. The subthreshold slope, measured at low gate voltage V_{GS}, is highlighted in Fig. 2.26-c and Fig. 2.26-d.

Table 2.9 – Static figures-of-merit of n- and p-MOSFETs on their initial rigid substrate and after transfer onto a plastic film

		I_{ON} µA/µm	I_{OFF} nA/µm	I_{ON}/I_{OFF} $\times 10^4$	g_m^{DC} µS/µm	V_{th} mV	DIBL mV	SS mV/dec.
n-MOSFET	Rigid	525	12.9	4.1	799	490	130	90
	Flexible	521	13.3	3.9	793	490	155	90
p-MOSFET	Rigid	-272	-2.67	10.2	499	570	90	90
	Flexible	-270	-2.65	10.2	495	570	90	90

2.2.1.1.2 Short Channel Effect (SCE) on flexible transistors

As for conventional rigid electronics, short channel effects (SCE) arise for flexible transistors featuring channel lengths of the same order of magnitude as the depletion layer. The scope of this work is not to describe in details the theoretical background of SCE effects but to show that they also have to be taken into account when considering high performance flexible electronics along with all parameters related to conventional electronics scaling down. From the static measurements presented in Fig. 2.26, the threshold voltage V_{th}, the Drain Induced Band Lowering (DIBL) and Subthreshold Slope (SS) can be extracted, as shown in Table 2.9.

2.2.1.1.3 Static characteristics comparison with conventional CMOS technologies

In conclusion, the static measurements performed on n- and p-MOSFETs both on their initial rigid substrate and after transfer-bonding onto a plastic film demonstrate that no static degradation arises from the fabrication process presented in the first part of this chapter. This results in flexible MOSFETs that feature static characteristics completely comparable and competitive with their rigid counterparts.

2.2.1.2 *HF characterization*

2.2.1.2.1 [S] parameters measurements

In addition to static characteristics, radio-frequency measurements have been performed on the same rigid and flexible devices. Fig. 2.27 and Fig. 2.28 show the [S] parameters comparison, measured from 500MHz up to 110GHz using the POSS[12] deembedding methodology presented in the first chapter. These figures demonstrate radio-frequency operations similar before and after transfer-bonding onto an organic film, even if some changes may be noticed at high frequencies. Blue lines correspond to measurements performed on the initial rigid HR SOI wafers and red lines on CMOS dies thinned and transfer-bonded onto plastic films. In addition, green dotted lines show retro-simulation of these [S] parameters on a flexible substrate, as presented in next section.

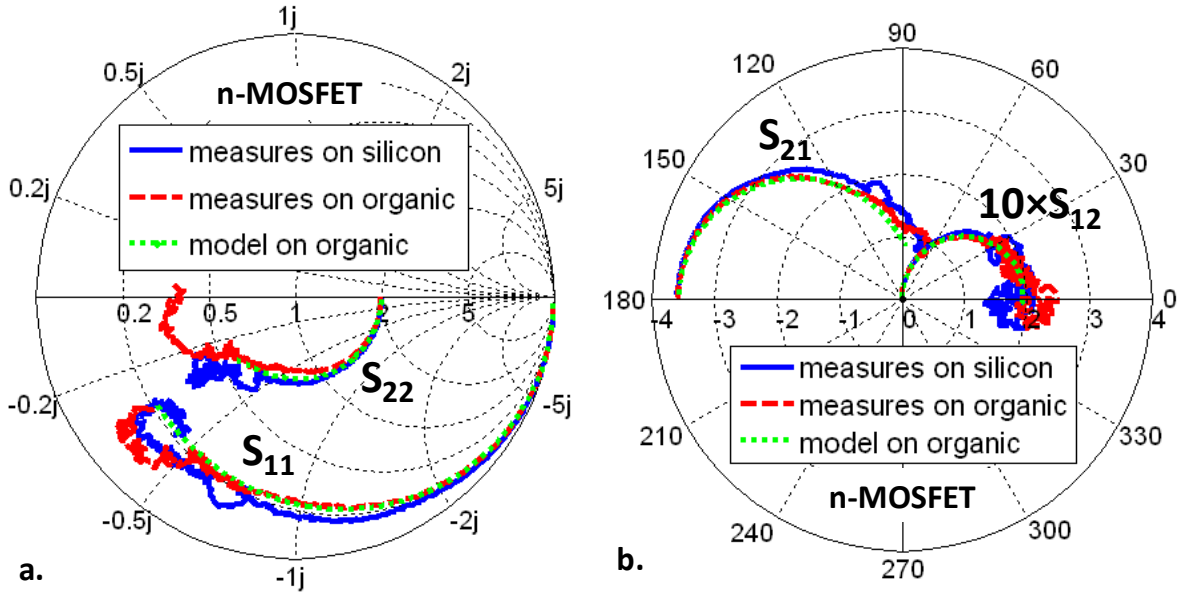


Fig. 2.27 – [S] parameters measured from 500MHz up to 110GHz on rigid n-MOSFETs (blue lines) and after transfer-bonding onto an organic film (red lines) in addition to retro-simulation of flexible devices [S] parameters (green lines), transistors are biased at drain voltage V_{DS}=1.2V, gate voltage V_{GS}=0.8V, and resulting drain current I_{DS}=270mA/mm.

[12] Pad-Open-Short$_1$-Short$_2$ deembedding methodology, for more details please refer to the first chapter, section 1.2.2.2.2.2 On-wafer deembedding: the POSS methodology

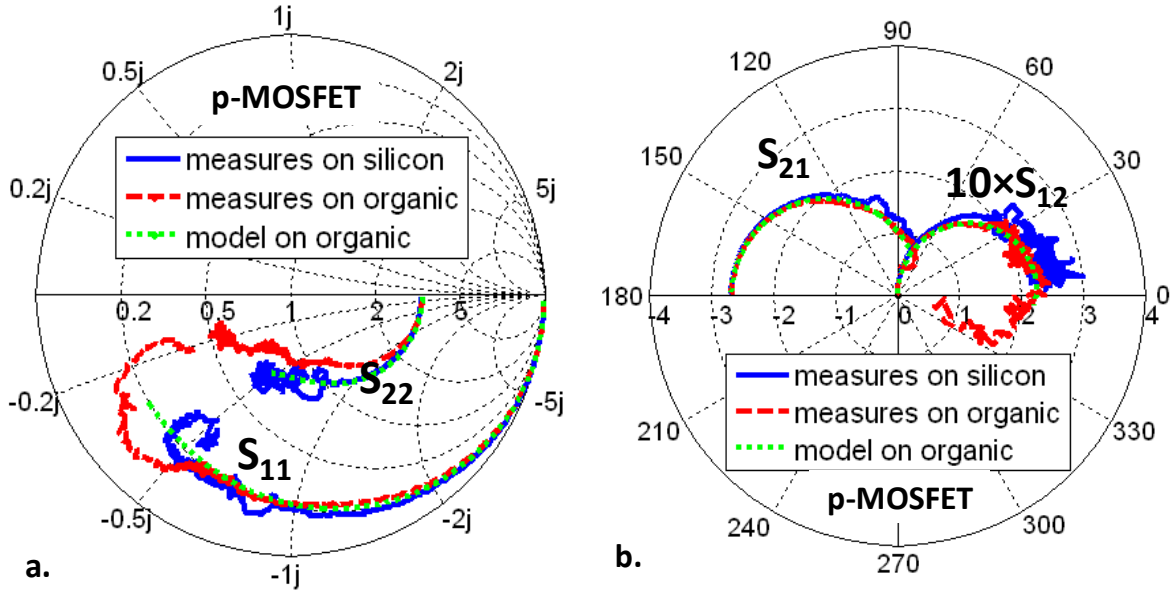


Fig. 2.28 – [S] parameters measured from 500MHz up to 110GHz on rigid p-MOSFETs (blue lines) and after transfer-bonding onto an organic film (red dashed lines) in addition to retro-simulation of flexible devices [S] parameters (green lines), transistors are biased at a drain voltage V_{DS}=-1.5V, a gate voltage V_{GS}=-1.0V, and a resulting drain current I_{DS}=-270mA/mm.

2.2.1.2.2 f_t and f_{max} figures-of-merit extraction

From the [S] parameters measurements, the current gains H_{21} and the Mason's gains U of the rigid and flexible MOSFETs presented in this work have been extracted and plotted as a function of frequency in Fig. 2.29. The first result demonstrated by these curves is that similar radio-frequency operations is obtained for both rigid and flexible MOSFETs: both the current gain H_{21} and the Mason's gain U feature experimental slope in agreement with the theoretical value of -20dB/dec. for each substrate. It is furthermore important to notice that the variation between [S] parameters measurements on rigid and flexible substrates visible at high frequencies in Fig. 2.27 and Fig. 2.28 only results in a slight change of the current gain H_{21} above 80GHz (Fig. 2.29-a and Fig. 2.29-b).

Furthermore, the extraction of the unity gain cut-off frequency f_t and the maximum oscillation frequency f_{max} have been performed at different drain voltage V_{GS} – or corresponding drain current I_{DS} – as presented in Fig. 2.30. The second important result highlighted in Fig. 2.30-a is the perfect matching of the cut-off frequencies of n- and p-MOSFETs before and after transfer onto a plastic film. However, a slight decrease of the Mason's gain U values of n- and p-MOSFETs after transfer on plastic can be noticed on Fig. 2.29-c and Fig. 2.29-d. This leads to a decrease of the maximum oscillation frequencies f_{max}, as presented in Fig. 2.30-b for n- and p-type devices on both rigid and organic substrates as a function of the drain current I_{DS}: unlike f_t, the f_{max} figure-of-merit is reduced by 25-30% at the highest current levels.

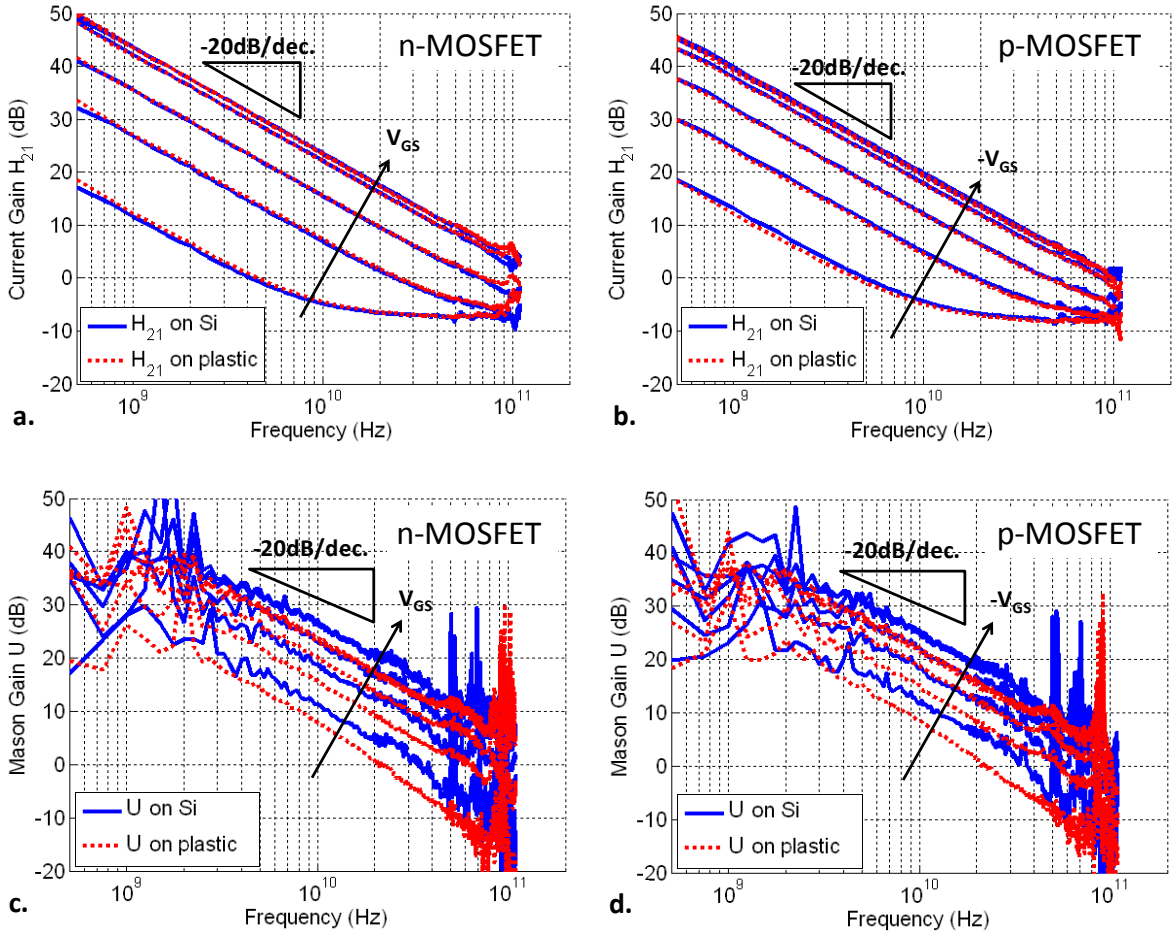


Fig. 2.29 – Current gain H_{21} and Mason's gain U measured on rigid (blue lines) and flexible (red dashed lines) n- and p- MOSFETs, biased at a drain voltage V_{DS}=1.2V, a gate voltage V_{GS}=0.8V, and a resulting drain current I_{DS}=270mA/mm, respectively a drain voltage V_{DS}=-1.5V, a gate voltage V_{GS}=-1.0V, and a resulting drain current I_{DS}=-270mA/mm

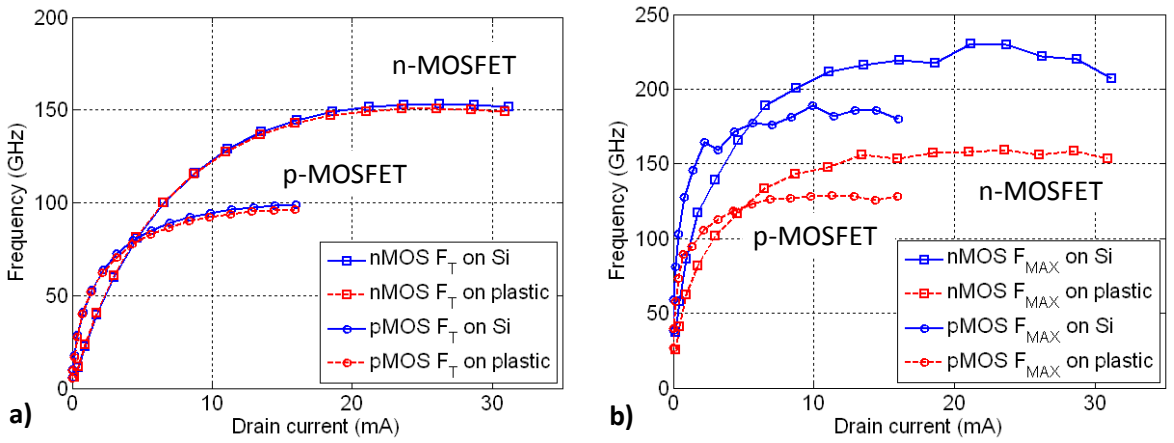


Fig. 2.30 – Cut-off frequencies f_t and maximum oscillation frequencies f_{max} extracted at different gate voltage V_{GS} for n- and p-MOSFETs before (blue lines) and after (red dashed lines) transfer onto a plastic substrate

These complete set of radio-frequency measurements have been performed on several transistors featuring similar geometries, as presented in Table 2.10 and Fig. 2.31 in order to demonstrate the repeatability of these results. Transistors geometries slightly differ by their gate length L_G and by their unitary gate width W_u and feature a total gate width development W_T of 64 µm.

Table 2.10 – Radio-frequency characteristics of several n- and p-MOSFETs before (colored lines) and after (uncolored lines) transfer onto plastic.

L_G nm	W_u µm	W_T µm			V_{DS} V	V_{GS} V	I_{DS} mA/mm	f_t GHz	f_{max} GHz
60	2	64	n-MOSFET	Rigid	1.2	0.8	323	170	210
				Flexible	1.2	0.8	310	170	170
60	1	64	n-MOSFET	Rigid	1.2	0.8	270	150	220
				Flexible	1.2	0.8	270	150	160
60	*1*	*64*	*p-MOSFET*	*Rigid*	*-1.5*	*-1.0*	*-272*	*100*	*160*
				Flexible	*-1.5*	*-1.0*	*-270*	*100*	*130*
65	2	64	n-MOSFET	Rigid	1.2	0.8	303	140	210
				Flexible	1.2	0.8	302	140	165
65	1	64	n-MOSFET	Rigid	1.2	0.8	304	140	210
				Flexible	1.2	0.8	298	140	175

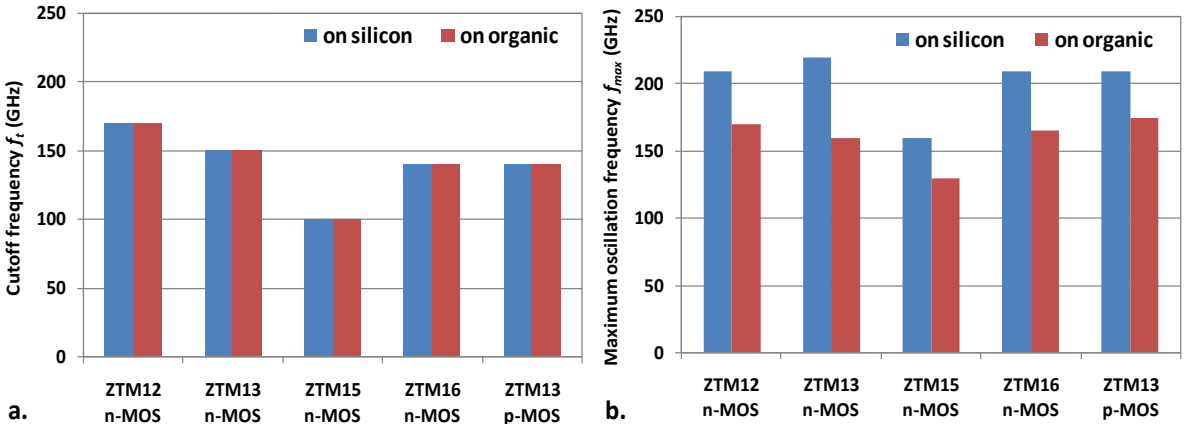


Fig. 2.31 – Comparison of a. cut-off frequencies f_t and b. maximum oscillation frequencies f_{max} figures-of-merit for n- and p-MOSFETs before (blue) and after (red) transfer onto a plastic film

In conclusion to radio-frequency measurements, it has been demonstrated that no major degradation of RF properties of the 65 nm node SOI RF-MOSFETs arises from the thinning and transfer-bonding onto organic films process described in this section. The only noticeable degradation is a maximum oscillation frequency f_{max} decrease by about 25-30%. These results outperform (to our best knowledge) the current state-of-the-art radio frequency performance on plastic, achieved on a 130 nm node bulk CMOS technology [16], [17].

2.2.1.2.3 RF characteristics comparison with conventional CMOS technologies

The radio-frequency measurements performed in this work demonstrated that the field of flexible electronics is currently able to reach a frequency range competitive with conventional rigid electronics. Fig. 2.32-a presents in the same graph data points from

literature for rigid Si-MOSFETs and flexible electronics, showing that flexible transistors reached the mainstream of conventional rigid RF devices. It is furthermore emphasized in Fig. 2.32-b that the field of high frequency electronics has been growing quickly, reaching frequencies competitive with conventional rigid electronics in less than a decade.

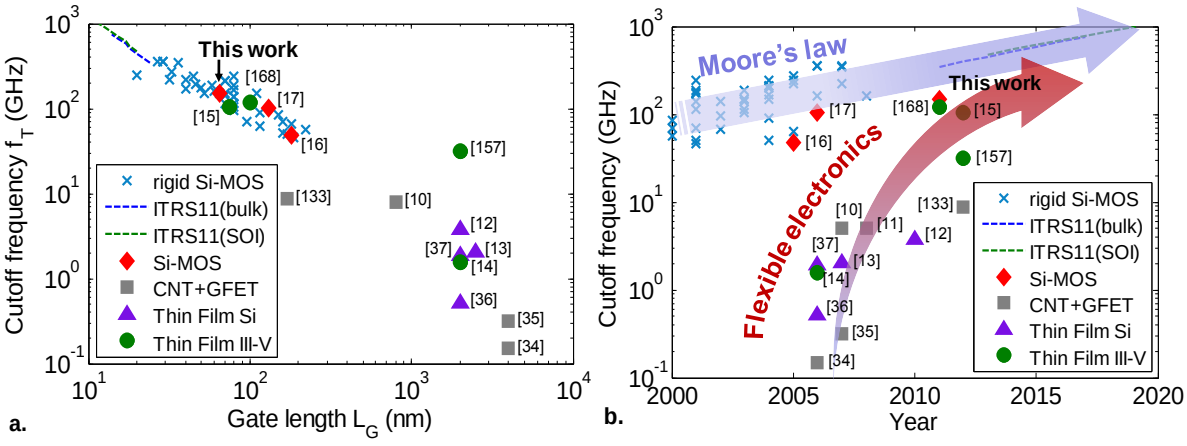


Fig. 2.32 – Comparison of cut-off frequencies f_t as a function of a. gate length and b. year for rigid silicon n-MOSFETs, ITRS previsions and flexible devices [10]–[17], [34]–[37], [59], [133], [157], [168].

2.2.1.3 *Small Signal Equivalent Circuit (SSEC) extraction*

2.2.1.3.1 Intrinsic and extrinsic parameters extraction

In order to complete the radio-frequency characterization of the 65nm node SOI RF-MOSFETs transferred onto organic films, their Small Signal Equivalent Circuits (SSEC) have been extracted, following the methodology presented in Chapter 1, and in [205]. The SSEC used in this work is presented again in Fig. 2.33 for convenience. Its parameters have been extracted for both n- and p-MOSFETs on their initial rigid substrate and after transfer-bonding onto plastic films to explain the variations noticed in RF characterization, i.e, the drop of the Mason's gain and therefore of the maximum oscillation frequency f_{max}.

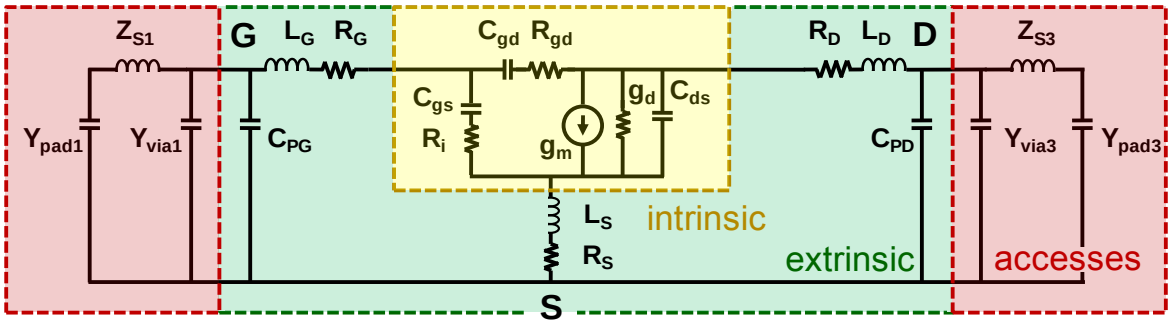


Fig. 2.33 – Noiseless Small Signal Equivalent Circuit (SSEC) including the intrinsic transistor (highlighted in yellow), the extrinsic parameters (green) and the access pads (red).

Intrinsic and extrinsic parameters extracted for both rigid and flexible n- and p-type devices are presented in Table 2.11. Relatively close values for the different parameters can be noticed between rigid and flexible MOSFETs. This is in agreement with Fig. 2.27 and Fig. 2.28 showing relatively similar [S] parameters.

Table 2.11 – Intrinsic and extrinsic parameters after extraction using the SSEC presented in Fig. 2.33 at V_{DS}=1.2V, V_{GS}=0.8V and I_{DS}=270mA/mm for n-MOSFET and V_{DS}=-1.5V, V_{GS}=-1V and I_{DS}=-263mA/mm for p-MOSFET

		Extrinsic					*Intrinsic*				
		C_{pg} fF	C_{pd} fF	R_g Ω/mm	R_d Ω.mm	R_s Ω.mm	g_m mS/mm	g_d mS/mm	C_{gs} fF/mm	C_{gd} fF/mm	C_{ds} fF/mm
n-MOS	Rigid	2.0	8.0	15.6	0.064	0.013	859	160	625	297	16
	Flexible	1.6	7.5	31.3	0.128	0.006	859	160	578	297	16
p-MOS	Rigid	2.5	6.0	15.6	0.006	0.006	559	99	578	265	16
	flexible	2.3	6.3	31.3	0.006	0.006	553	99	625	265	16

2.2.1.3.2 Error between model and measurements

In addition, the error between the measured and simulated [S] parameters on an organic substrate for an n-MOSFET is presented in details in Fig. 2.34 and Fig. 2.35. For most parameters, this error is lower than 20%, especially at low frequencies.

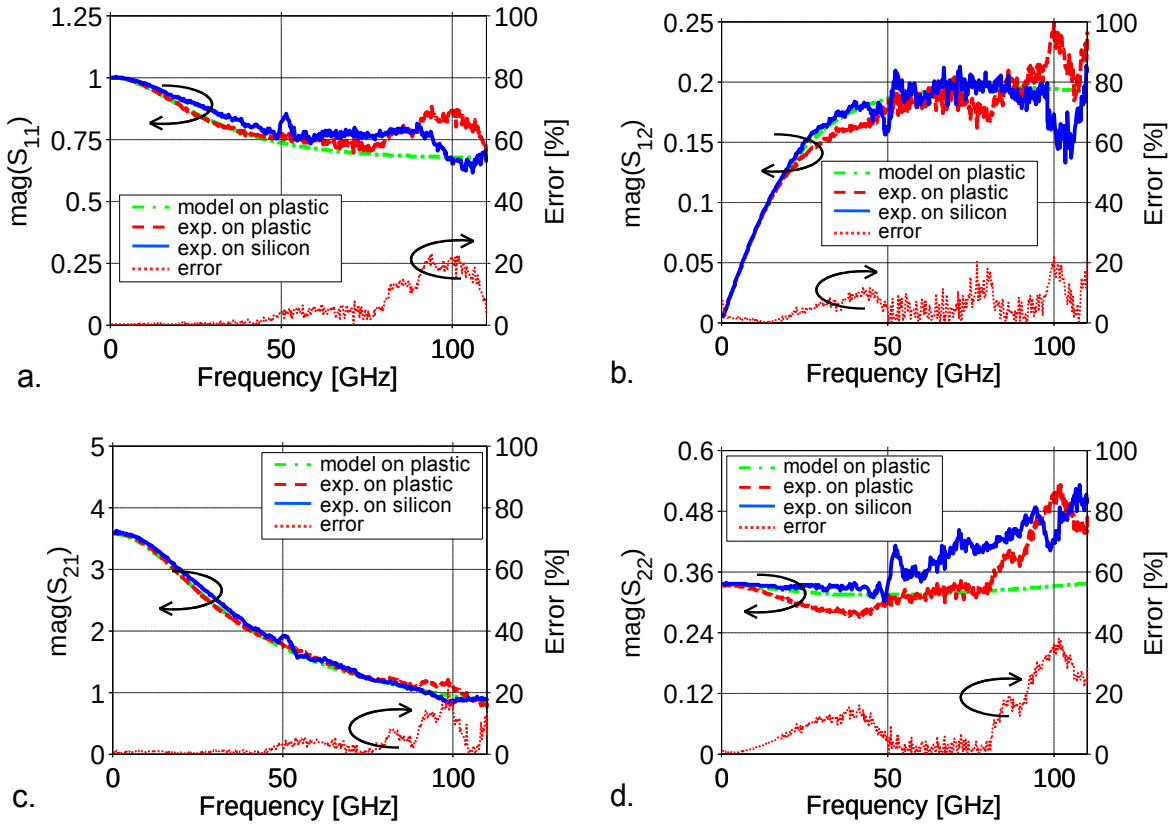


Fig. 2.34 – Magnitude of [S] parameters measured on n-MOSFET only, on rigid substrate (blue line), after transfer-bonding onto plastic (red dashed lines), [S] parameters calculated from the extracted SSEC (green dashed lines) and error between model and measurements on plastic (red dotted lines).

The good agreement between the model presented here and measurements performed on transistors transferred on an organic substrate is furthermore highlighted in Fig. 2.36, where both the simulated and measured current gain H_{21} and Mason's gain U are plotted as a function of frequency. The errors between models and measurements are also presented for both gains as a function of frequency demonstrating that the intrinsic and extrinsic parameters presented in Table 2.11 results in errors lower than ±10% up to 50GHz. The increasing errors above 50GHz may be explained by the fact that the current and Mason's gains values decreased and get close to zero at high frequency, leading to high error

percentages. This may also be due to the increasing inaccuracy of both the [S] parameters measurement and the deembedding methodology at high frequency.

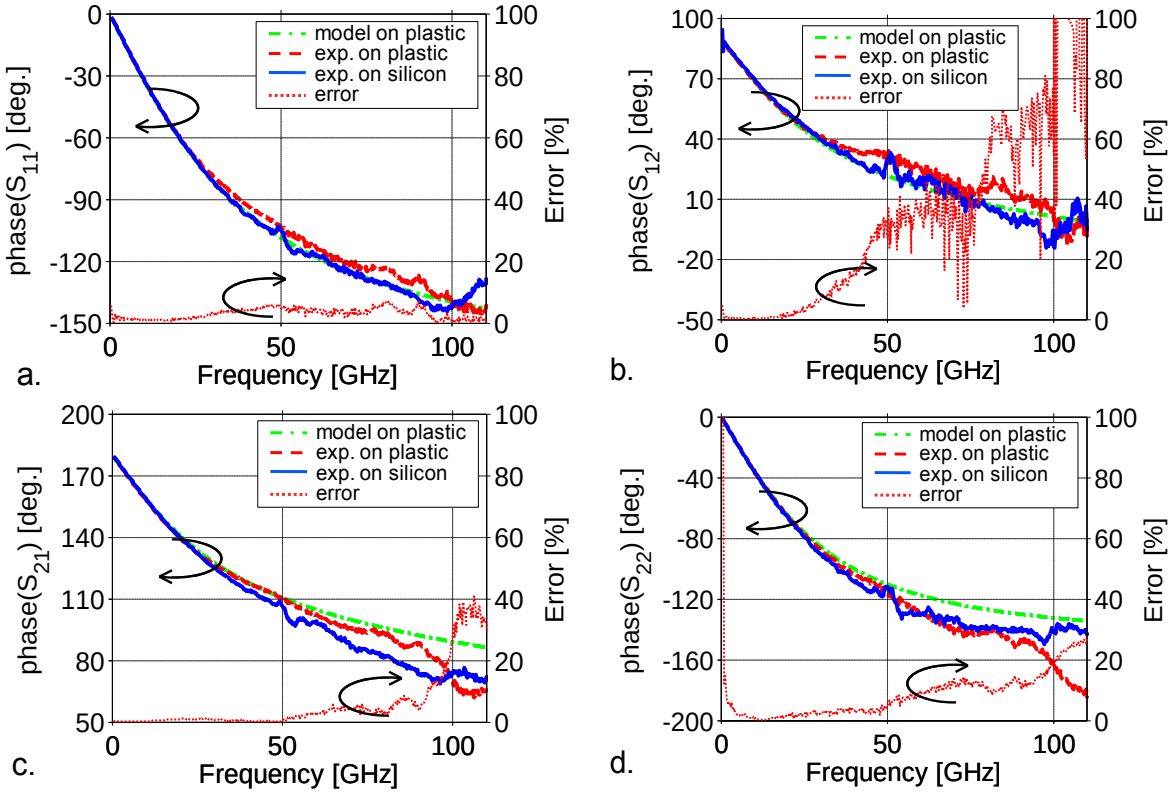


Fig. 2.35 – Phase of [S] parameters measured on n-MOSFET only, on rigid substrate (blue line), after transfer-bonding onto plastic (red dashed lines), [S] parameters calculated from the extracted SSEC (green dashed lines) and error between model and measurements on plastic (red dotted lines).

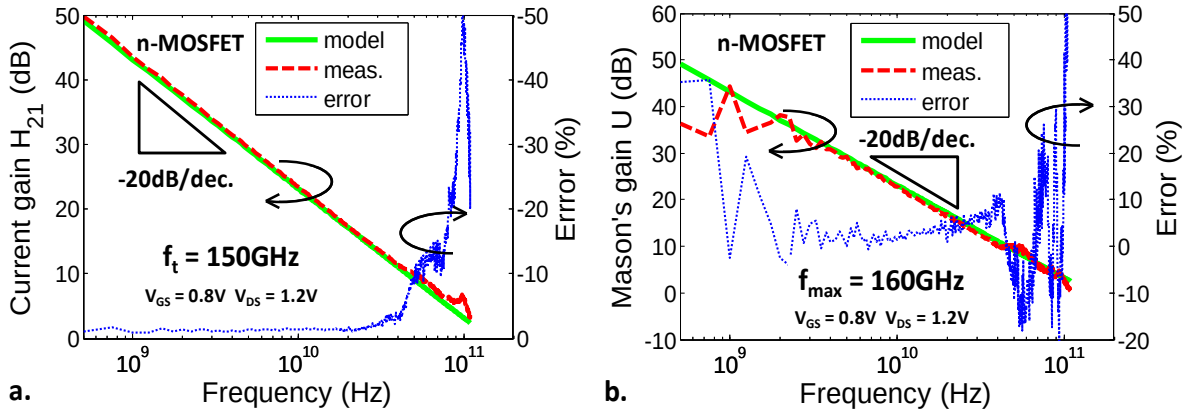


Fig. 2.36 – Measured and simulated a. current gain H_{21}, and b. Mason's gain U as a function of frequency for a n-MOSFET on an organic film showing good agreement between model and measurements. Cut-off frequency f_t and maximum oscillation frequency f_{max} on the organic substrate have been highlighted at a drain voltage V_{DS}=1.2V, a gate voltage V_{GS}=0.8V, and a resulting drain current I_{DS}=270mA/mm.

2.2.1.3.3 Drop of maximum oscillation frequency

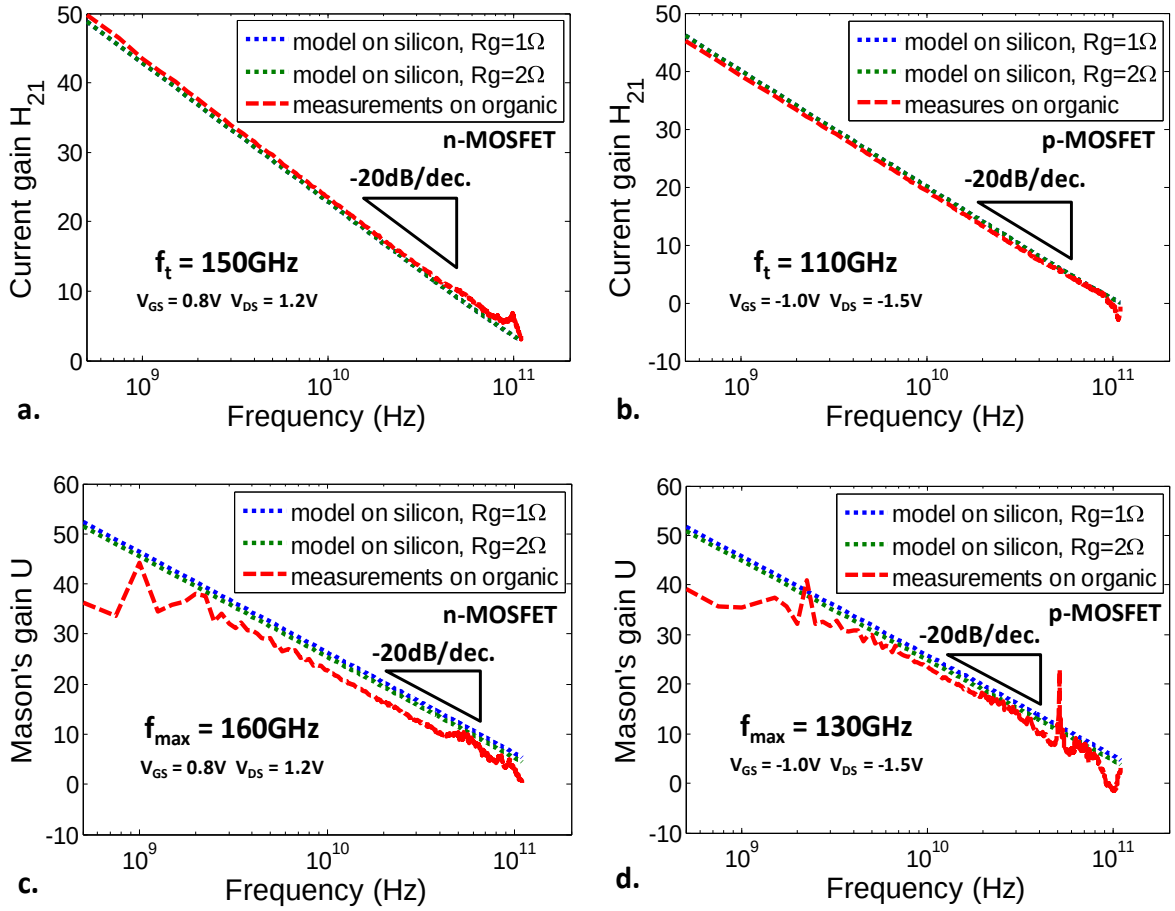


Fig. 2.37 –Measured current gains H_{21}, and Mason's gains U as a function of frequency for flexible n- and p-MOSFETs on a organic films along with gains simulated using the SSEC parameters extracted from measurements on rigid transistors and same parameters with a doubled gate resistance. Cut-off frequency f_t and maximum oscillation frequency f_{max} of flexible transistors have been highlighted at a drain voltage V_{DS}=1.2V, a gate voltage V_{GS}=0.8V, and a resulting drain current I_{DS}=270mA/mm for the n-MOSFET and at a drain voltage V_{DS}=-1.5V, a gate voltage V_{GS}=-1.0V, and a resulting drain current I_{DS}=-270mA/mm for the p-MOSFET.

This maximum oscillation frequency f_{max} performance reduction is partially attributed to a concomitant increase of the gate resistance resulting from the transfer-bonding process, as explained in [6]. The comparison of intrinsic and extrinsic extracted parameters presented in Table 2.11 shows that the gate resistance R_g doubles for both n- and p-type devices after transfer onto a plastic film. Fig. 2.37 supports this explanation by comparing experimental gains H_{21} and U measured on flexible transistors with two models: i) using the SSEC parameters extracted on rigid MOSFETs, and ii) using the same model with a doubled gate resistance. This figure demonstrates for n- and p-MOSFETs that the gate resistance increase leads to a decrease of the maximum oscillation frequency f_{max} without degrading the cut-off frequency f_t. Even if this is the main reason identified to account for the Mason's gain drop highlighted in Fig. 2.30, it only partially explains it (Fig. 2.37-c and Fig. 2.37-d).

2.2.1.3.4 Retro-simulated figures-of-merit on flexible p-MOSFETs

As presented in Table 2.10 and Fig. 2.30, 65nm p-MOSFET transferred on an organic film features a cut-off frequency f_t=100GHz, and a maximum oscillation frequency f_{max}=130GHz at drain and gate voltages V_{DS}=-1.5V and V_{GS}=-1.0V. The model presented previously for n-MOSFETs has also been used for p-MOSFETs modeling (see intrinsic and extrinsic parameters values in Table 2.11) and the retro-simulated radio-frequency figures-of-merit f_t and f_{max} are in agreement with measurements. This is demonstrated in Fig. 2.38, where measured and modeled current gain H_{21} and Mason's gain U are plotted as a function of frequency for a flexible p-MOSFET. The current gain error between model and measurements is lower than 2% up to 50GHz. However a slightly larger error is noticeable on the Mason's gain (±15% up to 60GHz).

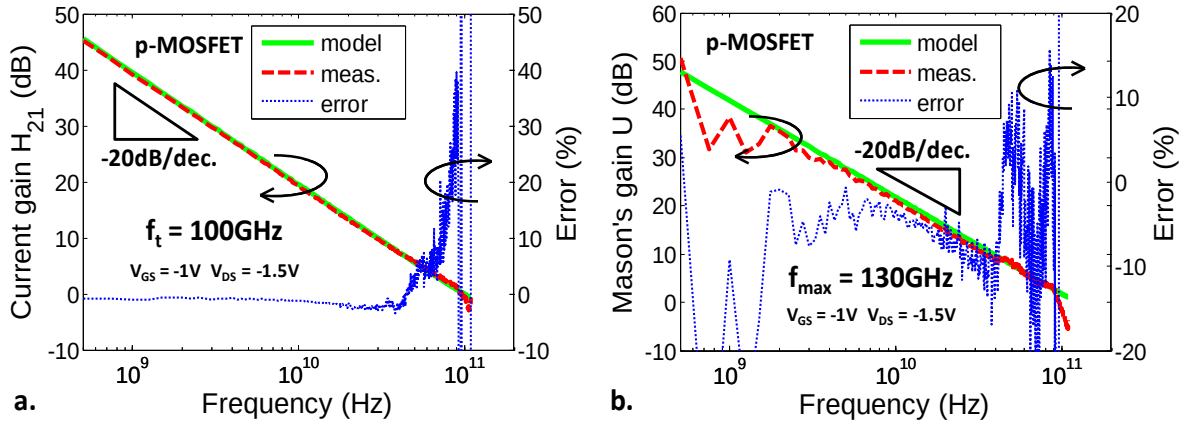


Fig. 2.38 – Measured and simulated a. current gain H_{21}, and b. Mason's gain U as a function of frequency for a p-MOSFET on an organic film showing good agreement between model and measurements. Cut-off frequency f_t and maximum oscillation frequency f_{max} on the organic substrate have been highlighted at a drain voltage V_{DS}=-1.5V and a gate voltage V_{GS}=-1V.

2.2.1.4 *Noise characterization*

Mature 65nm SOI RF-CMOS technology node is recognized for delivering a performance level suitable for high frequency and low noise applications. A large number of prospective applications in the field of high performance flexible electronics require low noise level, in addition to mechanical bendability. In order to completely demonstrate the potentialities of this technology as a major building block for fully flexible communicating devices, high frequency noise characterization has been performed in addition to standard measurements presented previously.

2.2.1.4.1 NF_{50} method

Two uncorrelated noise sources e_G and i_D have been added at the input and output of the noiseless small signal equivalent circuit (SSEC) presented in Fig. 2.33 in order to model the transistor noise (Fig. 2.39).

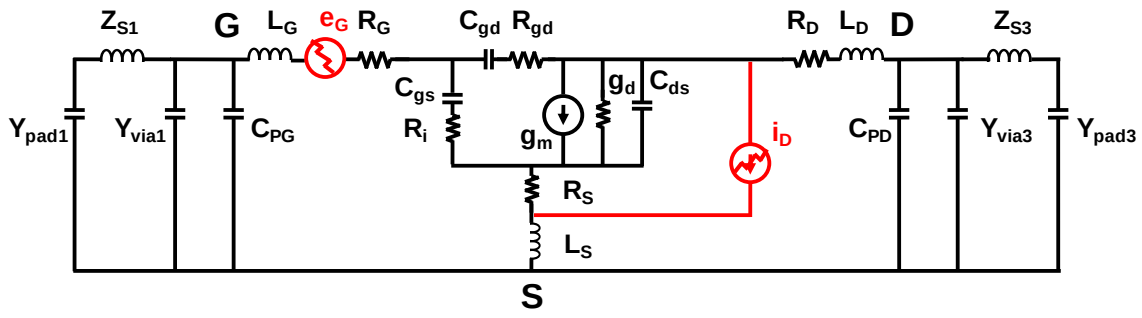


Fig. 2.39 – Small Signal Equivalent Circuit (SSEC) including two uncorrelated noise sources

The F_{50} method described in previous chapter (section 1.2.2.2.6 Noise measurement) is suitable for the extraction of the four noise parameters assuming that the equivalent input temperature T_{in} associated to the input noise source e_G is equal to room temperature. A single 50Ω impedance noise figure measurement[13] enable the extraction of the only unknown: the equivalent output noise temperature T_{out}. Measurements have been performed in two frequency ranges: 6-20GHz and 20-40Ghz (see first chapter, Fig. 1.35 for a description of the measurement setups). The 50Ω noise figure NF_{50} measurement is presented as a function of frequency in Fig. 2.40 for n- and p-MOSFETs on an organic substrate along with the fitted equivalent output temperature T_{out} and the modeled NF_{50}. Equivalent output temperatures for n- and p-MOSFETs on both their initial rigid substrate and their flexible organic substrate are summarized in Table 2.12

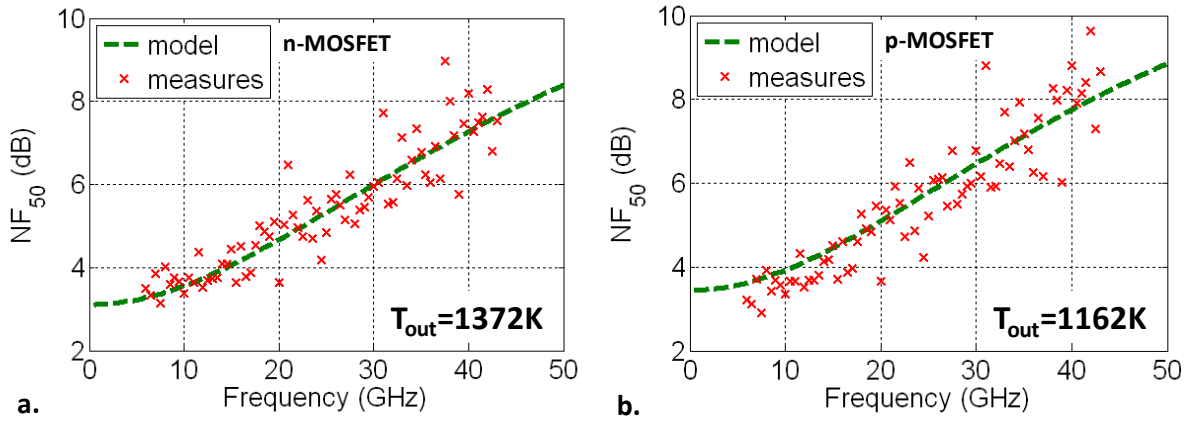


Fig. 2.40 – Measured and simulated 50Ω noise figure NF_{50} in 6-20GHz and 20-40GHz frequency ranges for a. n-MOSFET and b. p-MOSFET after transfer onto a plastic film. Equivalent output noise temperatures T_{out} are reported at drain and gate voltages V_{DS}=1.2V, V_{GS}=0.8V, and V_{DS}=-1.5V, V_{GS}=-1V for n- and p-type flexible transistors respectively.

2.2.1.4.2 Four noise parameters extraction

The combination of the [S] parameters measurements presented hereinbefore and the 50Ω noise figure measurements allows the extraction of the four noise parameters (NF_{min}, R_n, and Γ_{opt}) and the associated gain (G_a) of the considered transistors. The minimal noise figure NF_{min} and the associated gain G_a are plotted as a function of frequency for n- and p-

[13] This noise figure measurement is performed taking the actual noise source impedance into account (about 50Ω), as presented in the first chapter (section 1.2.2.2.6 Noise measurement) and in [205]

type transistors on their initial HR SOI substrate and on an organic film (Fig. 2.41). Almost similar values of noise performance are thus demonstrated after thinning and transfer-bonding onto a flexible substrate. Noise figures-of-merit NF_{min}/G_a=0.57dB/17.8dB (respectively 0.57dB/17.0dB) are demonstrated for a n-MOSFET (respectively p-MOSFET) on a plastic film. These results outperform the current state-of-the-art noise performance on plastic achieved on a 130 nm bulk silicon technology [16], [17]. In addition, the invariability of the noise matching condition Γ_{opt} and the noise resistance R_n is also demonstrated in Fig. 2.42, and Fig. 2.43 for n- and p-MOSFETs respectively. The two noise resistances exhibit a variation after transfer onto a flexible substrate lower than 6%.

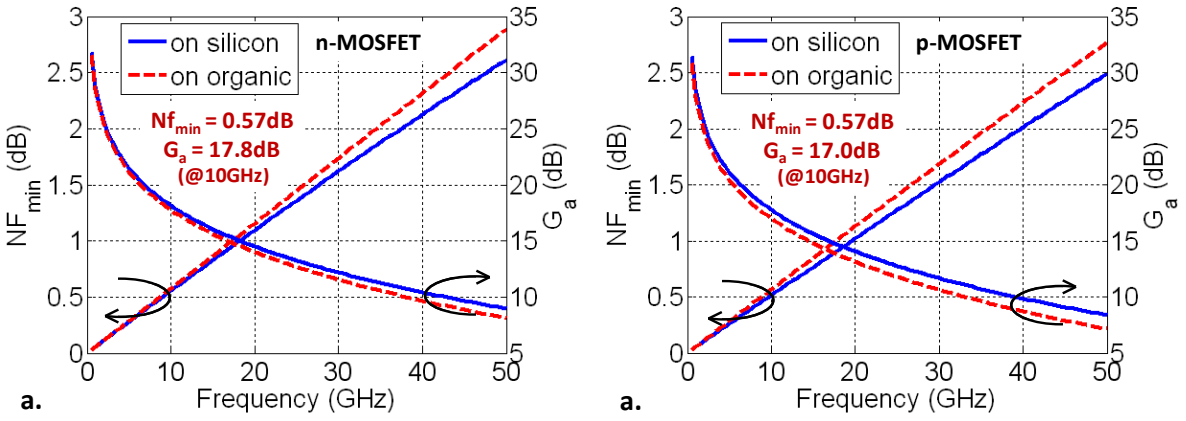


Fig. 2.41 – Minimal noise figure NF_{min} and associated gain G_a for a. n-MOSFETs and b. p-MOSFETS on their initial rigid HR SOI wafer (blue lines) and after transfer onto a flexible organic film (red dashed lines) at drain and gate voltages V_{DS}=1.2V, V_{GS}=0.8V, and V_{DS}=-1.5V, V_{GS}=-1V respectively. The values of both figures-of-merit are reported at 10GHz for the flexible transistors.

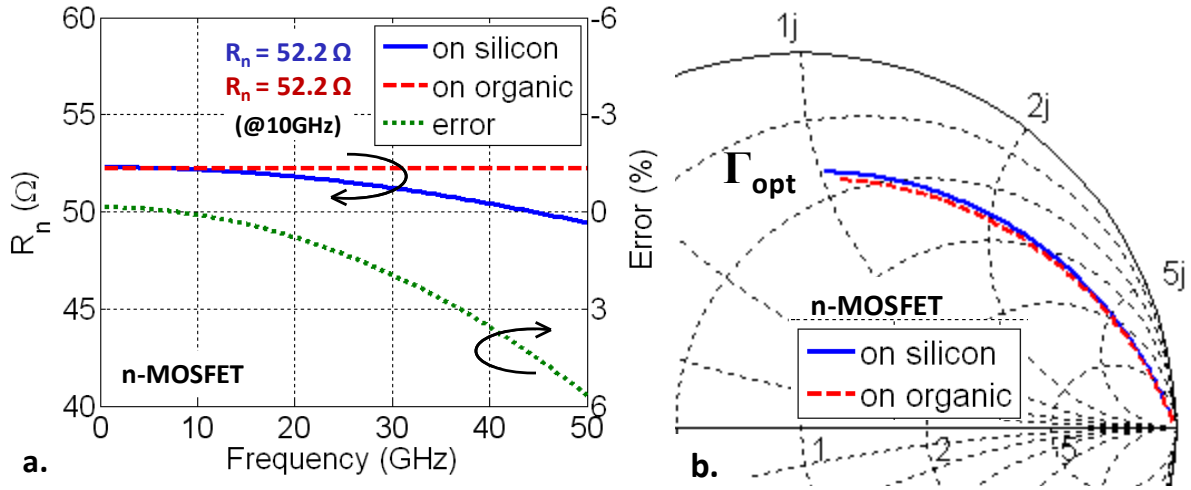


Fig. 2.42 – a. Equivalent noise resistance R_n and b. optimal noise reflection coefficient Γ_{opt} for a n-MOSFET on its initial rigid HR SOI wafer (blue lines) and after transfer onto a flexible organic film (red dashed lines) at drain and gate voltages V_{DS}=1.2V and V_{GS}=0.8V.

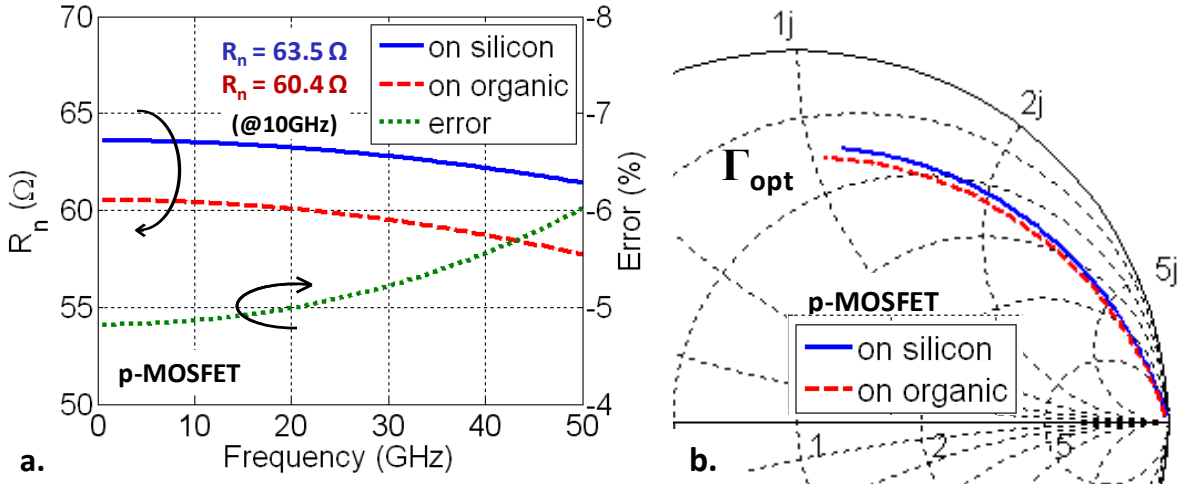


Fig. 2.43 – a. Equivalent noise resistance R_n and b. optimal noise reflection coefficient Γ_{opt} for a p-MOSFET on its initial rigid HR SOI wafer (blue lines) and after transfer onto a flexible organic film (red dashed lines) at drain and gate voltages V_{DS}=-1.5V and V_{GS}=-1V.

As a conclusion, it can be noticed that the equivalent output temperature T_{out} is relatively not affected by the thinning and transfer-bonding process: the variation after transfer is lower than 5% for both n- and p-MOSFETs. This, in addition to similar [S] parameters presented in Fig. 2.34 and Fig. 2.35, leads to invariant noise performance (Fig. 2.41) and matching conditions (Fig. 2.42 and Fig. 2.43) as in Table 2.12, where the four noise parameters along with the associated gain and the equivalent output temperature are presented at 10GHz for n- and p-MOSFETs on both substrates. The variation of these parameters is also highlighted demonstrating a good match between rigid and flexible MOSFETs noise figures-of-merits (less than 6% variation for n-MOSFETs and 17% for p-MOSFETs).

Table 2.12 – Radio-frequency noise parameters extracted at 10GHz before and after transfer onto plastic of a n-MOSFET (biased at V_{DS}=1.2V, V_{GS}=0.8V) and a p-MOSFET (biased at V_{DS}=-1.5V, V_{GS}=-1.0V). Equivalent input noise temperature T_{in} is assumed to be fixed at 296K.

	(@10GHz)	T_{out} K	NF_{min} dB	G_a dB	R_n Ω	G_{opt} mS	B_{opt} mS
n-MOSFET	Rigid	1412	0.56	18.1	52.2	1.25	-3.41
	Flexible	1372	0.57	17.8	52.2	1.26	-3.23
	Error	*-2.8%*	*+1.8%*	*-1.7%*	*0%*	*+0.8%*	*-5.3%*
p-MOSFET	Rigid	1221	0.51	17.8	63.5	0.93	-3.27
	Flexible	1162	0.57	17.0	60.4	1.08	-3.36
	Error	*-4.8%*	*+11.8%*	*-4.5%*	*-4.9%*	*+16.1%*	*+2.8%*

2.2.2 Passive components and circuits

In addition to transistors measurements, CMOS circuits designed for use on a conventional rigid HR-SOI wafer have been transferred and characterized on a flexible film. A one-stage low noise amplifier (LNA) featuring a 2.0dB gain at 80GHz is therefore presented in Fig. 2.44. The static transconductance measured on both rigid and flexible LNA are presented with the discrepancy resulting from transfer-bonding. A 20% decrease in transconductance

can be noticed. This results in a lower gain at the working frequency of this circuit, as highlighted in Fig. 2.44-b: the flexible LNA features a gain of 0.34dB at 80GHz instead of 2.0dB. This loss can be explained by the maximum oscillation frequency drop discussed in previous section in addition to variations of the characteristic impedance of transmission lines after transfer.

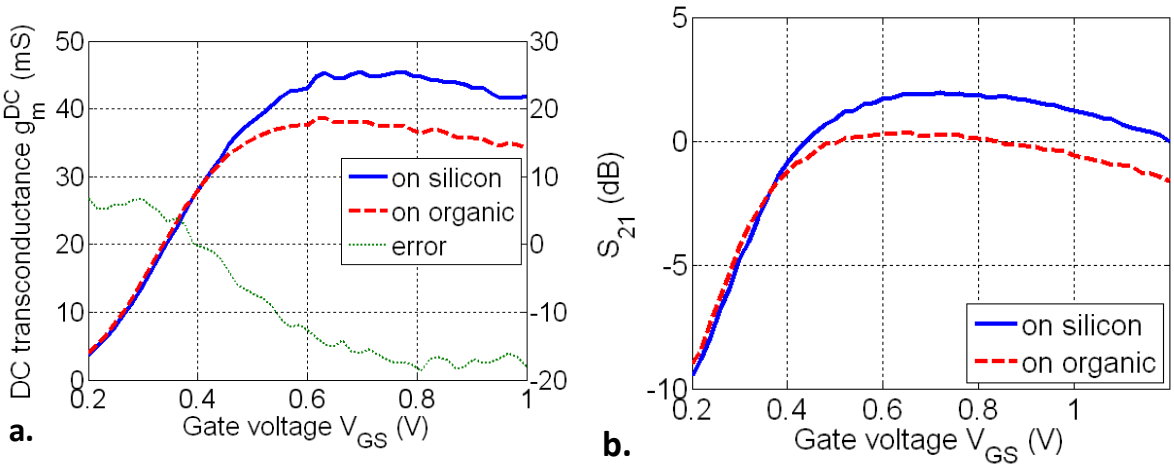


Fig. 2.44 – a. Static transconductance measured on a rigid (blue lines) and flexible (red dashed lines) LNA biased at a drain voltage V_{DS}=1.0V, and b. S_{21} parameters measured for the same LNA on both substrates, at 80GHz.

2.2.3 Conclusion on the electrical performance of transferred CMOS dies

Static characteristics presented in this chapter demonstrate that no major degradation results from from the thinning and transfer processes, leading to flexible MOSFETs with DC figures-of-merit competitive with their rigid counterparts. In addition, high frequency measurements performed on transistors on both types of substrates lead to the conclusion that flexible and rigid transistors feature similar radio-frequency operation. They also exhibit state-of-the-art high frequency performance, invariant cut-off frequencies but reduced maximum oscillation frequencies. This last point is mainly explained by a concomitant increase of the gate resistance during the transfer-bonding process onto a plastic film. Finally, flexible low noise amplifiers measurements lead to the conclusion that CMOS circuitry can be transferred from conventional rigid wafers onto flexible films without specific redesigns.

2.3 Conclusion of the second chapter

The second chapter has presented the fabrication process developed during this work to realize high performance flexible electronics, along with the complete characterization of a 65 nm SOI-CMOS technology thinned and transferred onto a plastic handler.

The proposed fabrication process involves the complete removal of the silicon handler of CMOS processed SOI wafers, and its replacement by an organic film, refered to as plastic handler. A three-step thinning procedure has been developed to enable complete silicon removal.

An organic film was subsequently bonded on the back side of the thinned CMOS chip, in place of the former silicon handler. This results in a thin, light, and flexible SOI-CMOS technology. In comparison to alternative solutions presented in the first chapter, this methodology enables the realization of complex functions as it benefits from the BEOL interconnection network.

One essential conclusion is that transfer-bonding leads to the realization of flexible devices with no visible degradation.As only electrical characterization can demonstrate their high electrical performance, static, high frequency, and noise measurements were therefore performed on the flexible SOI RF-MOSFETs.

Static characterizations demonstrated a complete agreement between rigid and flexible transistors, i.e. before and after transfer onto an organic film. High frequency measurements furthermore unveiled unrivaled HF figures-of-merit: cut-off and maximum oscillation frequencies as high as 150 / 160 GHz for n-MOSFETs on plastic, and 110 / 130 GHz for p-MOSFETs on plastic. These values set a novel standard for high frequency flexible electronics, reporting performance competitive with their rigid counterpart. In addition, low noise performance were also demonstrated, achieving minimal noise figures and associated gains of 0.57 / 17.8 dB for n-MOSFETs on plastic, and 0.57 / 17.0 dB for p-MOSFETs on plastic.

This chapter has therefore presented a fabrication process to transfer commercial SOI CMOS technology onto organic film and demonstrate the potentialities of this approach for future high performance electronics, opening the way to radio-frequency and low noise bendable electronic applications.

Chapter 3: **Bending flexible CMOS**

The logical question arising from the two previous chapter is: how would flexible electronic devices and circuits behave in bent configuration, i.e. under flexure. The aim of this last chapter is thus to provide elements to answer this question. The first part will therefore detail some mechanical aspects related to cylindrincal bending of multilayers, that will be applied them to the flexible CMOS stack presented in the previous chapter. From an application point of view, electrical properties stable upon deformation are required. A methodology based on neutral plane engineering to provide high performance stability will therefore be presented and supported by electro-mechanical modeling.

After describing the required theoretical background, electrical measurements performed on bent flexible CMOS devices will be compared with computed values. Their good agreement will allow us to demonstrate the effectiveness of the neutral plane engineering method. Following this strategy, high frequency performance of flexible n-MOSFETs featuring f_T/f_{MAX} of 120/145 GHz, are reported with relative variations limited to less than 5% even under aggressive bending on cylinders with curvature radii down to 12.5 mm.

3.1 Mechanical considerations

3.1.1 Strain application in microelectronics

3.1.1.1 *Strain engineering: from rigid to flexible CMOS*

In the previous chapter and published work [156], [205], it was demonstrated that the thinning and transfer process does not degrade transistors properties in terms of static, high frequency and low noise operation in straight flat configuration. But apart from performance conservation, a question legitimately arises: how mechanical deformation can affect operation of complex flexible electronic systems?

In the perspective of synthesizing reliable functions with invariant characteristics, electrical properties independent of the strain type, direction and intensity are therefore highly desirable. It is well known that the application of strain to a semiconductor breaks its symmetry leading to band splitting and warping [239]–[246]. As a result, carriers transport properties can be significantly modulated depending on the strain direction and symmetry, in other words, as a function of the strain tensor structure.

Over the last decade, this physical property has been widely used to enhance carriers mobility through uniaxial process-induced stress in the 90 nm CMOS technology node and beyond [247]–[249]. However, the situation considerably differs when flexible electronics is considered because one of its fundamental characteristics is that strain resulting from bending of thinned flexible chips is by essence random.

3.1.1.2 *Objectives*

After providing a brief description of the required basics of mechanics, this chapter will focus on reducing the impact of external strain on electrical properties of flexible CMOS devices. Using neutral plane engineering, it is possible to accommodate aggressive bending configurations while maintaining a minimal strain level in the active channel of transistors. The thickness of the plastic substrate is selected to reduce the strain level developed in the silicon active layer under bending condition. This is performed by positioning the multilayer neutral plane close to the active layer.

3.1.2 Introduction to mechanical considerations and piezoresistivity

The basic mechanics principles described in this chapter are mainly based on [243]–[246], [250]–[253]. The first paragraphs will only focus on linear mechanics, in order to introduce the notions of strain and stress tensors, linear elasticity theory, neutral plane in a multilayer stack and finally piezoresistivity in silicon [243]–[246]. The need and description of non-linearities will be provided afterwards [250]–[253], along with computation of the strain and stress components in the modelled multilayer stack of interest. Expected variations of electrical properties will be extracted, considering linear relationships between electron mobility and figures-of-merit (drain current, transconductance, cut-off, and maximum oscillation frequencies).

3.1.2.1 *General principles*

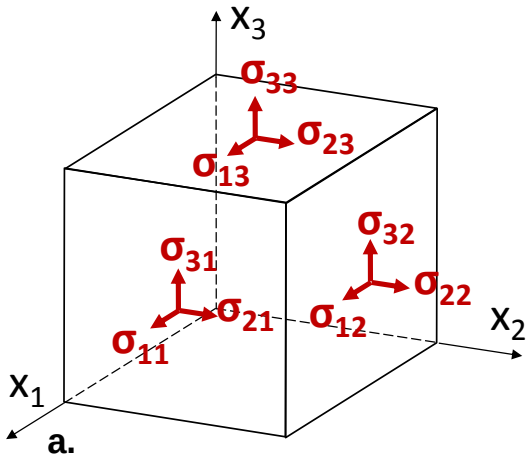
3.1.2.1.1 Stress and strain tensors

3.1.2.1.1.1 *Stress tensor*

Considering an infinitesimal cube of matter, stress – defined as force by unit of area – can be applied on each of its face by its surrounding. The nine-component, second-rank stress tensor **σ** consists of three normal stress components σ_{ii} (i.e. orthogonal to the face plane), and six shear stress components σ_{ij} (i.e. in this plane).

The stress distribution is schematically illustrated in Fig. 3.1-a. The σ_{ij} component refers to the stress applied along the x_i axis on the face orthogonal to the x_j axis. By definition, positive σ_{ii} correspond to tensile stress, whereas negative σ_{ii} correspond to compressive stress. The stress tensor is symmetric, because its antisymmetric part corresponds to torque, not present in a solid at equilibrium [243]. The stress tensor therefore only contains six independent components [244], [245].

Relationships between a force $\vec{F}$ applied on a surface orthogonal to vector $\vec{n}$, and the stress tensor **σ** are provided in Fig. 3.1-b (Eq. 2.1 to Eq. 3.3). Details about several usual forms of the stress tensor can be found in [243]–[245].



b.

$$\vec{F} = \begin{bmatrix} F_1 \\ F_2 \\ F_3 \end{bmatrix} \quad \text{and} \quad \vec{n} = \begin{bmatrix} n_1 \\ n_2 \\ n_3 \end{bmatrix} \qquad \textbf{Eq. 3.1}$$

$$\begin{bmatrix} F_1 \\ F_2 \\ F_3 \end{bmatrix} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix} \begin{bmatrix} n_1 \\ n_2 \\ n_3 \end{bmatrix} \qquad \textbf{Eq. 3.2}$$

$$\text{i.e.} \quad F_i = \sigma_{ij}\, n_j \quad (i = 1, 2, 3) \qquad \textbf{Eq. 3.3}$$

using Einstein convention[14]

Fig. 3.1 – a. Stress tensor components in an infinitesimal cube of matter, and b. relationships between a force $\vec{F}$ applied on a surface orthogonal to vector $\vec{n}$, and the stress tensor σ.

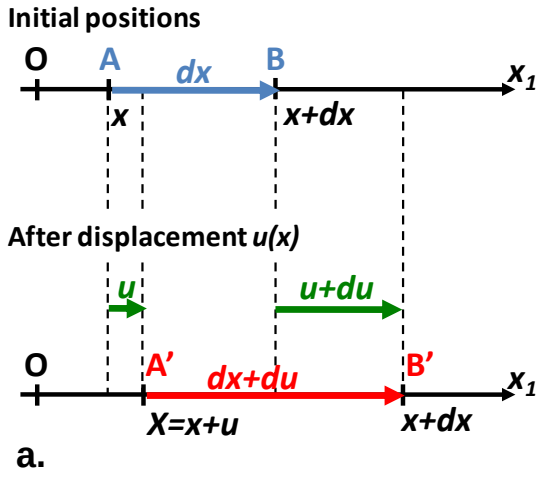
3.1.2.1.1.2 *Strain tensor*

Because strain and stress are interrelated, strain is also a second-rank tensor, defined as dimensionless displacement ratio. If two points A and B separated by an infinitesimal position vector $d\vec{x}$, are both subjected to a displacement $\vec{u}(x)$ resulting in novel positions A' and B', strain can be defined as the ratio of $d\vec{u}(x)$ over $d\vec{x}$. Strain appears only if both points experience different displacements, i.e. if $d\vec{u}(x) \neq 0$.

This is illustrated in Fig. 3.2 on a 1D element for simplicity, where the infinitesimal element AB, initially defined as $\overrightarrow{OA} = \vec{x}$, and $\overrightarrow{AB} = \overrightarrow{dx}$, is subjected to displacement

[14] Summation of any repeated index is implicit in Einstein convention [245]

$\overrightarrow{AA'} = \vec{u}$, and $\overrightarrow{BB'} = \vec{u} + d\vec{u}$. It should be noticed that this representation assumes that strain is infinitesimal, i.e. $du_i \ll dx_i$.



$$\varepsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right) \qquad \text{Eq. 3.4}$$

$$\begin{bmatrix} du_1 \\ du_2 \\ du_3 \end{bmatrix} = \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon_{33} \end{bmatrix} \begin{bmatrix} dx_1 \\ dx_2 \\ dx_3 \end{bmatrix} \qquad \text{Eq. 3.5}$$

b.

$$\text{i.e. } du_i = \varepsilon_{ij}\, dx_j \ \ (\text{i} = 1, 2, 3) \qquad \text{Eq. 3.6}$$

using Einstein convention

Fig. 3.2 – a. Schematic illustration of the strain in an infinitesimal 1D element AB, initially defined as $\overrightarrow{OA} = \vec{x}$, and $\overrightarrow{AB} = \overrightarrow{dx}$, subjected to displacement $\overrightarrow{AA'} = \vec{u}$, and $\overrightarrow{BB'} = \vec{u} + d\vec{u}$, and b. relationships between position $\vec{x}$, displacement $\vec{u}$, and strain tensor ε in general 3D case.

The general 3D concept is taken into account in strain-displacement equations Eq. 3.4 to Eq. 3.6 that define the second-rank infinitesimal strain tensor **ε**. This definition (Eq. 3.4) excludes rotation and therefore only considers pure material deformation, as demonstrated in [245]. As a result, the strain tensor **ε** is a symmetric tensor, like the stress tensor **σ**.

It should also be mentioned that a slightly different notation may be seen in text books for strain, then refered to as engineering strain $\boldsymbol{\epsilon}$ [254], [255], in comparison to the tensorial strain **ε** described hereinbefore. Only off-diagonal terms (i.e. shear strain) differ: $\epsilon_{ij} = 2\varepsilon_{ij}$ for $i \neq j$ (Eq. 3.8). More details on this notation can be found in [245], [254], [255].

3.1.2.1.1.3 *Single-column notation*

As stress and strain tensor are both symmetric, these two tensors can be fully described with only six independent parameters, which can be represented in an equivalent single-column vector assuming relations described in Eq. 3.7 and Eq. 3.8 [7–9].

$$\sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{12} & \sigma_{22} & \sigma_{23} \\ \sigma_{13} & \sigma_{23} & \sigma_{33} \end{bmatrix} \equiv \sigma_i = \begin{bmatrix} \sigma_1 = \sigma_{11} \\ \sigma_2 = \sigma_{22} \\ \sigma_3 = \sigma_{33} \\ \sigma_4 = \sigma_{23} \\ \sigma_5 = \sigma_{13} \\ \sigma_6 = \sigma_{12} \end{bmatrix} \qquad \text{Eq. 3.7}$$

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{12} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{13} & \varepsilon_{23} & \varepsilon_{33} \end{bmatrix} \equiv \varepsilon_i = \begin{bmatrix} \varepsilon_1 = \varepsilon_{11} \\ \varepsilon_2 = \varepsilon_{22} \\ \varepsilon_3 = \varepsilon_{33} \\ \varepsilon_4 = \varepsilon_{23} \\ \varepsilon_5 = \varepsilon_{13} \\ \varepsilon_6 = \varepsilon_{12} \end{bmatrix} \equiv \epsilon_i = \begin{bmatrix} \epsilon_1 = \varepsilon_{11} \\ \epsilon_2 = \varepsilon_{22} \\ \epsilon_3 = \varepsilon_{33} \\ \epsilon_4 = 2\varepsilon_{23} \\ \epsilon_5 = 2\varepsilon_{13} \\ \epsilon_6 = 2\varepsilon_{12} \end{bmatrix} \qquad \text{Eq. 3.8}$$

3.1.2.1.2 Linear elastic theory

3.1.2.1.2.1 *Hooke's law*

Linear elastic theoric assumes that stress is directly proportional to strain, and related by the Hooke's law (Eq. 3.9), which can also be inverted to express strain in terms of stress, as in Eq. 3.10.

$$\sigma_{ij} = C_{ijkl}\epsilon_{kl} \quad \textbf{Eq. 3.9} \qquad \epsilon_{ij} = S_{ijkl}\sigma_{kl} \quad \textbf{Eq. 3.10}$$

The stiffness ***C***, and compliance ***S*** tensors are both fourth-rank tensors as they link together second-rank tensors $\boldsymbol{\epsilon}$ and $\boldsymbol{\sigma}$. Because strain and stress tensors $\boldsymbol{\epsilon}$ and $\boldsymbol{\sigma}$ are symmetric, the 81 components of the two fourth-rank tensors can be reduced to 36 independent coefficients [244], [245]. Therefore, similarly to the single-column notation of $\boldsymbol{\epsilon}$ and $\boldsymbol{\sigma}$, a 6×6 matrix representation of the stiffness ***C*** and compliance ***S*** tensors can be used. However, these two arrays do not form a tensor and change of basis for instance should be performed on the actual fouth-rank tensors [245]. Relationships linking the reduced 6×6 matrix coefficients with the 81 tensorial coefficients can be found in [245].

Due to crystal symmetry reasons, when considering silicon (which is a class m3m cubic crystal), only three independent stiffness and compliance coefficients have to be considered. The 6×6 matrix representation of the stiffness ***C*** and compliance ***S*** tensors can therefore be simplified to Eq. 3.11 and Eq. 3.12 [243]–[245]:

$$\begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \sigma_4\\ \sigma_5\\ \sigma_6\end{bmatrix} = \begin{bmatrix}C_{11} & C_{12} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & C_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & C_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & C_{44}\end{bmatrix}\begin{bmatrix}\epsilon_1\\ \epsilon_2\\ \epsilon_3\\ \epsilon_4\\ \epsilon_5\\ \epsilon_6\end{bmatrix} \quad \textbf{Eq. 3.11}$$

$$\begin{bmatrix}\epsilon_1\\ \epsilon_2\\ \epsilon_3\\ \epsilon_4\\ \epsilon_5\\ \epsilon_6\end{bmatrix} = \begin{bmatrix}S_{11} & S_{12} & S_{12} & 0 & 0 & 0\\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0\\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & S_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & S_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & S_{44}\end{bmatrix}\begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \sigma_4\\ \sigma_5\\ \sigma_6\end{bmatrix} \quad \textbf{Eq. 3.12}$$

Table 3.1 – Numerical values of stiffness C_{ij} and compliance S_{ij} coefficients of silicon [243], [245], [256]

Stiffness (×10^9 Pa)	
C_{11}	167.5
C_{12}	63.9
C_{44}	79.6
Compliance (×10^{-13} Pa^{-1})	
S_{11}	76.8
S_{12}	−21.4
S_{44}	126.0

Numerical values of stiffness and compliance coefficients of silicon are provided in Table 3.1 for the [100], [010], [001] coordinate system [243], [245], [256]. Relationships between stiffness and compliance coefficients can be deduced from definitions and are also demonstrated in [243].

3.1.2.1.2.2 *Young's modulus, Poisson ratio, and Lame coefficients*

When considering homogeneous, isotropic materials, Young's modulus E (expressed in Pa), and Poisson ratio ν (dimensionless) are often considered to characterize mechanical properties. Orientation-dependent E and ν coefficient can also be defined for anisotropic materials (as silicon) by analogy (Fig. 3.3) [243], [245]. They are related to the compliance constants as presented in Eq. 3.13 and Eq. 3.14 [243].

$$E = \frac{1}{S_{11}} \qquad \textbf{Eq. 3.13}$$

$$\nu = -\frac{S_{12}}{S_{11}} \qquad \textbf{Eq. 3.14}$$

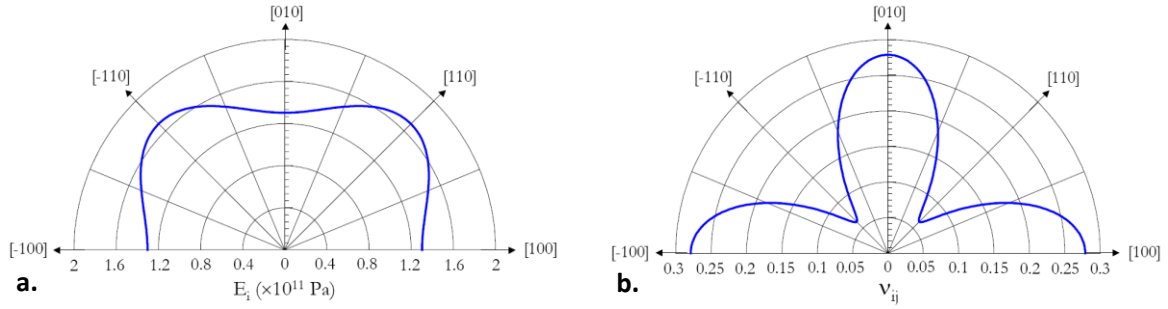


Fig. 3.3 – Orientation-dependent a. Young's modulus E, and b. Poisson ratio ν of n-type silicon (Images reproduced from [245]).

For homogeneous, isotropic materials following the linear elastic theory, Hooke's law can be equivalently expressed using the Young's modulus E and Poisson ratio ν, or the Lamé coefficiens λ and μ, defined in Eq. 3.15 and Eq. 3.16.

$$\lambda = \frac{\nu E}{(1+\nu)(1-2\nu)} \qquad \textbf{Eq. 3.15}$$

$$\mu = \frac{E}{2(1+\nu)} \qquad \textbf{Eq. 3.16}$$

3.1.2.1.3 Piezoresistivity

Piezoresistivity theory describes stress-induced resistivity changes [243]. In strained silicon, the resistivity can be expressed as a second-rank tensor $\boldsymbol{\rho}$ and related to the stress tensor $\boldsymbol{\sigma}$ by the piezoresistivity fourth-rank tensor $\boldsymbol{\pi}$ (assuming infinitesimal strain), in Eq. 3.17 [239], [240], [243], [245], [257]. As the resistivity tensor $\boldsymbol{\rho}$ is symmetric (and the stress tensor $\boldsymbol{\sigma}$ too), it can be expressed in a single-column form (similarly to Eq. 3.7), and the piezoresistivity tensor $\boldsymbol{\pi}$ can be reduced in a 6×6 matrix form, leading to the reduced equation Eq. 3.18.

$$\frac{\partial \rho_{ij}}{\rho_0} = \pi_{ijkl}\,\sigma_{kl} \qquad \textbf{Eq. 3.17}$$

$$\frac{\partial \rho_i}{\rho_0} = \pi_{ij}\,\sigma_j = -\frac{\partial \mu_i}{\mu_0} \qquad \textbf{Eq. 3.18}$$

The charge carrier mobility μ_i expressed in the i direction, can be directly related to the stress σ_j in the j direction by the piezoresistivity matrix π_{ij}, assuming that the charge carrier density is stress-independent. This assumption is validated for doped silicon only [245].

$$\begin{bmatrix} \partial\rho_1/\rho_0 \\ \partial\rho_2/\rho_0 \\ \partial\rho_3/\rho_0 \\ \partial\rho_4/\rho_0 \\ \partial\rho_5/\rho_0 \\ \partial\rho_6/\rho_0 \end{bmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \qquad \textbf{Eq. 3.19}$$

Numerical values of the piezoresistivity coefficients π_{ij} associated to an electron inversion layer of silicon are provided in Table 3.2 (Eq. 3.20 to Eq. 3.22). These values are given in the [100], [010], [001] coordinate system. Transistors presented in this work feature a

channel direction along the <110> crystal orientation. As a result, the piezoresistivity coefficients referred to as longitudinal π_L, transverse π_T, and out-of-plane $\pi_\perp$ are expressed in this coordinate system in equations Eq. 3.23 to Eq. 3.25. Orientation-dependent piezoresistivity coefficients are also represented in Fig. 3.4 [245].

Table 3.2 – Numerical values of piezoresistivity coefficients π_{ij} associated to an electron inversion layer of silicon [245], [257], and relations to express longitudinal π_L, transverse π_T, and out-of-plane $\pi_\perp$ piezoresistivity coefficients in a [110], [-110], [001] coordinate system.

$$\pi_{11} = -84.0 \times 10^{-11}\ \text{Pa}^{-1} \quad \textbf{Eq. 3.20}$$

$$\pi_{12} = 34.0 \times 10^{-11}\ \text{Pa}^{-1} \quad \textbf{Eq. 3.21}$$

$$\pi_{44} = -17.0 \times 10^{-11}\ \text{Pa}^{-1} \quad \textbf{Eq. 3.22}$$

$$\boldsymbol{\pi_L = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44})} \quad \textbf{Eq. 3.23}$$

$$\boldsymbol{\pi_T = \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44})} \quad \textbf{Eq. 3.24}$$

$$\boldsymbol{\pi_\perp = \pi_{12}} \quad \textbf{Eq. 3.25}$$

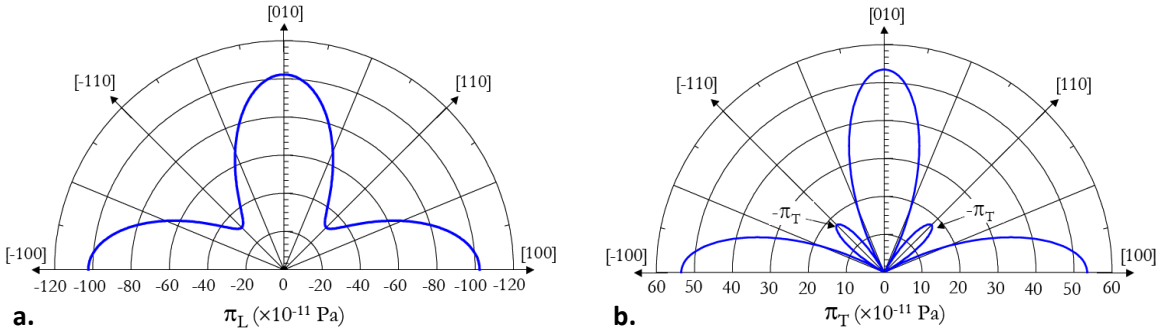


Fig. 3.4 – Orientation-dependent a. longitudinal π_L, and b. transverse π_T piezoresistivity coefficients associated to an electron inversion layer of silicon (Images reproduced from [245]).

3.1.2.2 *First approximation of cylindrical bending*

3.1.2.2.1.1 *Objective*

As explained in the introduction of this chapter, after demonstrating that the thinning and transfer process does not degrade transistors electrical properties, the impact of mechanically applied external strain must be investigated. Furthermore, it is desirable to maintain stable high frequency characteristics of flexible devices and circuits even under aggressive flexure.

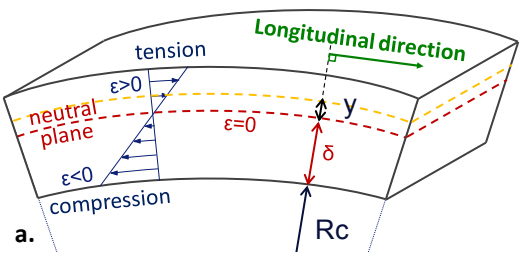
The beginning of this third chapter briefly presented the linear elastic and piezoresistivity theories. This enables – assuming infinitesimal strains and linear relationships between the components of the strain and stress tensors – to relate mechanical strain (or stress) to change in electrical properties. The details of strain effects on semiconductor energy band structures will not be discussed here [239]–[246]. However, the random deformation of a thinned flexible CMOS chip will be assuming a cylindrical bending as a practical study case. The main direction of bending is set in the current flow direction in order to take into account the case that will have the greater impact on electrical properties.

3.1.2.2.1.2 *Neutral plane in a bent multilayer*

In this analysis, the position of the neutral plane, defined as the surface perpendicular to the cross-sectional plane where there is neither compression nor elongation, is a parameter of utmost importance that determines strain distribution over the thickness of the bent

multilayer stack. Considering a homogeneous monolayer, the neutral plane is located in the middle of the monolayer. Therefore, the top part of the material is subjected to tensile strain and the bottom part to compressive strain (Fig. 3.5-a). When considering a multilayer, the neutral plane location depends on the thickness t_i and Young's modulus E_i of the different layers, as illustrated in Fig. 3.5-b. Following a simplified one-dimensional approach, its position from the bottom of the stack, referred to as δ, can formulated as a function of the thickness, t_i, Young's modulus, E_i, and centroidal axis position, z_i, of each layer, according to equation Eq. 3.26 and Eq. 3.27 [151], [241], [258].

Once the neutral plane location is known, longitudinal strain distribution $\varepsilon_L(y)$ (defined in the direction tangent to the curvature, see Fig. 3.5-a) can be estimated through simple geometrical considerations, as in Eq. 3.28.



$$\delta = \frac{\sum z_i E_i t_i}{\sum E_i t_i} \qquad \textbf{Eq. 3.26}$$

$$z_i = \left(\sum_{j=1}^{i} t_j\right) - \frac{t_i}{2} \qquad \textbf{Eq. 3.27}$$

$$\varepsilon_L(y) = \frac{y}{R_C + \delta} \qquad \textbf{Eq. 3.28}$$

Fig. 3.5 – a. Schematic of a material subjected to cylindrical bending over a curvature radius R_C, neutral plane location is highlighted along with the longitudinal strain distribution, and b. Schematic of a multilayer stack with n layers featuring different thickness t_i and Young's modulus E_i, the multilayer neutral plane location δ is calculated using Eq. 3.26 and Eq. 3.27, and longitudinal strain distributin using Eq. 3.28 [151] (also see supporting material of reference [151]).

3.1.2.2.1.3 *Neutral plane engineering*

These relations clearly indicate that the addition of a thin stiff inorganic film (here the topmost layers of CMOS dies) on top of a thicker flexible – i.e. featuring a low Young's modulus – organic handler tends to move the neutral plane towards the interface, or even in the inorganic film. The principle is therefore to associate a thick soft material to an ultra-thin stiff overlayer to locate the neutral plane close to their joining interface.

Although the flexible CMOS stack is a very complex system owing to the heterogeneity of the BEOL interconnection network, the aforementioned principle can be well illustrated and the related mechanics well captured by adopting a simple bilayer system. Fig. 3.6-a quantifies the position *d* of the neutral plane with respect to the interface normalized by the total thickness t_{TOT} (see inset in Fig. 3.6-b) as a function of the thickness ratio $t_{film}/t_{handler}$. This functional dependence of d/t_{TOT} versus $t_{film}/t_{handler}$ is parametrized by the Young's moduli ratio $E_{film}/E_{handler}$ of both materials. This graph emphasizes the fact that the neutral plane of the multilayer can be positioned at, or close to the interface ($d = 0$), or at any position that may be relevant [151], [259]–[261] by a proper selection of materials stiffness and thickness.

From this analysis, it naturally ensues that the position neutral plane of the flexible CMOS system must be adjusted as close as possible to the active layer where electron transport takes place to minimize the impact of bending on transistors performance. For the 65 nm SOI-CMOS technology considered in this work the active layer is the 60 nm thick SOI film. It is only separated from the plastic handler by the BOX layer (145 nm) and the adhesive layer (~500 nm).

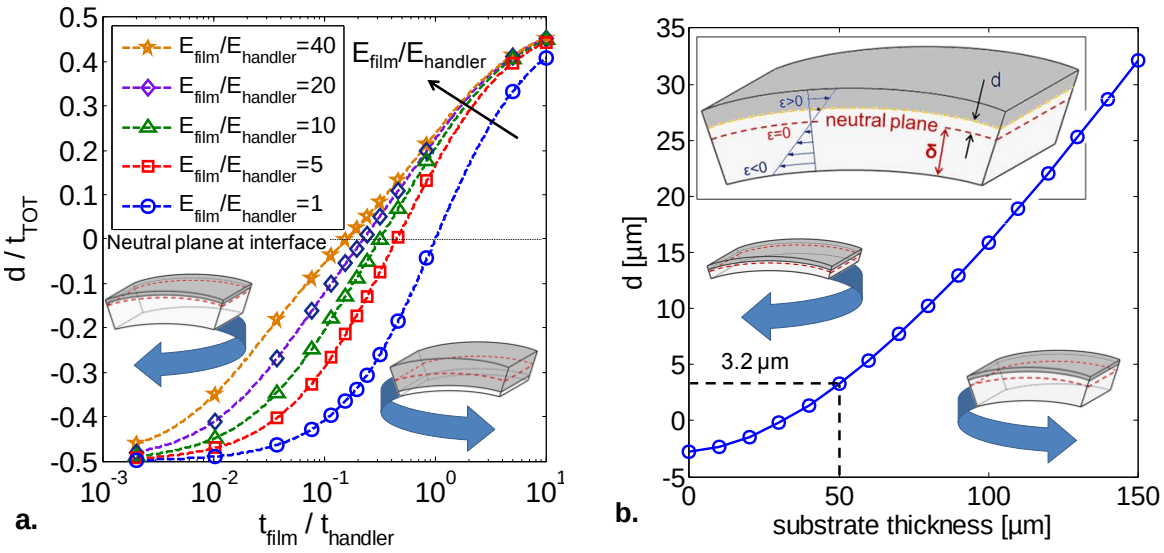


Fig. 3.6 – a. Neutral plane location dependence on thickness and Young's modulus of a bilayer represented by plotting the interface to neutral plane distance *d* over total thickness t_{TOT} versus the thicknesses ratio $t_{film}/t_{handler}$ for various Young's moduli ratios $E_{film}/E_{handler}$. And b. Dependence of the neutral plane to active layer distance *d* on the plastic handler thickness when considering the flexible CMOS stack presented in Table 3.3. Inset: schematic of the sample under flexure where the flexible CMOS multilayer is represented in grey (the neutral plane is defined in red dashed line and longitudinal strain is represented by blue arrows).

In a more realistic description of the flexible CMOS stack, 17 uniform layers of various thicknesses and Young's moduli have been taken into account, as detailed in Table 3.3, for an accurate treatment of the mechanical problem. Using a 50 µm thick polyimide handler, Fig. 3.6-b shows that the distance between the neutral plane and the SOI layer is reduced to approximately 3 µm.

Reducing the thickness of the polyimide handler from 125 µm to 50 µm for instance moves the neutral plane to active layer distance from 23.8 µm to 3.2 µm (using the stack model presented in Table 3.3). Therefore, considering the longitudinal strain distribution described in Eq. 3.28, the longitudinal strain generated in the active layer at a curvature radius R_C = 12.5 mm can be estimated at 0.19 % for a 125 µm thick plastic handler and 0.03 % for a 50 µm thick handler. Neutral plane engineering thus enables to reduce the strain generated under flexure almost by a factor of 10.

3.1.2.2.1.4 *Limitations of this approach*

As stated in the introduction of this section, linear elastic theory assumes infinitesimal strain. This means that both deformation and rotations should be infinitesimal. Bending a thin plate over a cylinder which radius is in the centimeter range results in infinitesimal strains (Fig. 3.8-a) but large rotation angles that invalidate the assumptions inherent to infinitesimal strain theory [250]–[253]. To overcome this limitation, strain and stress distributions in the plate cross-section have been calculated using the finite strain theory. Next section will provide the required basics to model a thin multilayer system under flexure and presents results in the case of the CMOS multilayer stack model described in Table 3.3. The large deformation principles described in the following paragraphs are mainly based on [250]–[253]. Demonstration of the relationships required to model cylindrical bending of flexible CMOS devices and circuits will not be discussed here, and can be found in the aforementioned references.

Table 3.3 –Description of the flexible CMOS multilayer stack after transfer onto a flexible handler along with parameters used for mechanical simulations.

		Material	Thickness	Young's modulus	Poisson's ratio	λ	μ
			nm	GPa	-	GPa	GPa
Alucap		Al	1900	70	0.33	51.1	26.3
M6	metal	Cu	850	100	0.33	73.0	37.6
	dielectric	SiO2	650	75	0.17	16.5	32.1
M2-M5	metal	Cu	150	100	0.33	73.0	37.6
	dielectric	SiO2	230	75	0.17	16.5	32.1
M1	metal	Cu	150	100	0.33	73.0	37.6
	dielectric	SiO2	430	75	0.17	16.5	32.1
SOI		Si	60	165.7	0.28	82.4	64.7
BOX		SiO2	145	75	0.17	16.5	32.1
Glue		SU-8	500	4.5	0.22	1.4	1.8
Handler		PI	50 µm	2.5	0.34	2.0	0.9

3.1.3 Introduction to large deformation theory

3.1.3.1 *General principles and application to cylindrical bending*

After the determination of the neutral plane position, strain and stress distributions across the flexible CMOS multilayer stack can be calculated according to continuum mechanics considerations. The calculation of the deformed shape is performed assuming that planes orthogonal to the original reference surface remain flat and orthogonal to the deformed reference surface [151].

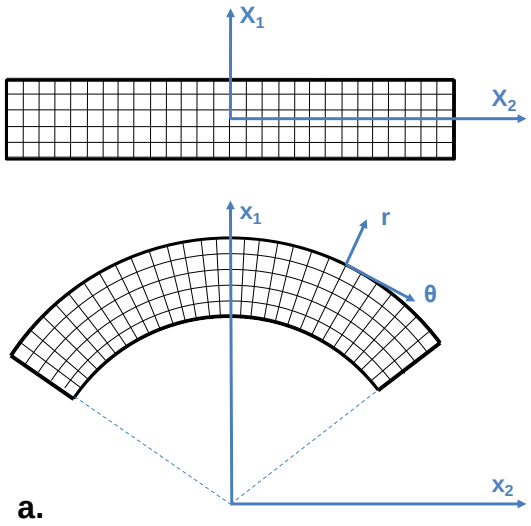
3.1.3.1.1 Transformation gradient

It is considered here that initial positions are referred to as $\boldsymbol{X}$, and time-dependant position as $\boldsymbol{x}(t)$, with corresponding coordinates respectively (X_1, X_2, X_3), and (x_1, x_2, x_3), or (r, θ, z) in a cylindrical coordinate system (Fig. 3.7-a). Then a transformation applied to a material can be described by the transformation gradient $\boldsymbol{F}$, defined as follows in Eq. 3.29 and Eq. 3.30 [250]–[253].

$$d\boldsymbol{x} = \boldsymbol{F}.d\boldsymbol{X} \qquad \textbf{Eq. 3.29}$$

$$\boldsymbol{F} = \frac{\partial \boldsymbol{x}}{\partial \boldsymbol{X}} \qquad \textbf{Eq. 3.30}$$

Assuming cylindrical bending, as presented in Fig. 3.7-a in 2D and Fig. 3.8-b in 3D, the final position $\boldsymbol{x}$ can be expressed as a function of the initial positions $\boldsymbol{X}$ according to equations Eq. 3.31 to Eq. 3.34 in a cylindrical coordinate system. Relation $r = h(X_1)$ describes the fact that horizontal material planes are transformed into concentric tubes and $\theta = v(X_2)$ vertical planes into radial planes [253]. It should also be noticed that in these two equations, δ refers to the neutral plane to middle of the stack distance [253].



$$r = h(X_1) = R_C \sqrt{1 + 2\frac{X_1 - \delta}{R_C}} \quad \textbf{Eq. 3.31}$$

$$\theta = v(X_2) = \frac{X_2}{R_C} \quad \textbf{Eq. 3.32}$$

$$z = X_3 \quad \textbf{Eq. 3.33}$$

$$\boldsymbol{x(X_1, X_2, X_3)} = \boldsymbol{h(X_1)\, e_r(X_2) + X_3 e_z(X_3)} \quad \textbf{Eq. 3.34}$$

Fig. 3.7 – a. Schematic representation of the multilayer stack before (top) and after (bottom) cylindrical bending, a mesh as been drawn on the material to highlight strain (tensile on outer, and compressive strain on the inner part of the material), and b. Equations representing the cylindrical bending of a thin plate: from initial positions $X(X_1,X_2,X_3)$ to final positions $x(x_1,x_2,x_3)$ that can also be expressed as (r,θ,z) in a cylindrical coordinate system.

The material deformation gradient tensor $\boldsymbol{F}$ (Eq. 3.35) associated to the cylindrical bending of a thin plate (Fig. 3.7-a) can furthermore be expressed using equations Eq. 3.36 and Eq. 3.37.

$$\boldsymbol{F} = \begin{bmatrix} h' & 0 & 0 \\ 0 & hv' & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \textbf{Eq. 3.35}$$

According to the polar decomposition theorem presented in equation Eq. 3.36 [251], [253] – stating that '*any particle deformation can be expressed as a pure deformation followed by a rotation or by a rotation followed by a pure deformation'* – the deformation gradient tensor can be expressed as a function of the right and left stretch tensors $\boldsymbol{U}$ and $\boldsymbol{V}$, and the orthogonal rotation tensor $\boldsymbol{R}$ [250]–[253]. The right and left Cauchy-Green stretch tensor $\boldsymbol{C}$ and $\boldsymbol{B}$ can be calculated using equations Eq. 3.37 and Eq. 3.38.

$$\boldsymbol{F} = \boldsymbol{R.U} = \boldsymbol{V.R} \quad \textbf{Eq. 3.36}$$

$$\boldsymbol{U^2} = \boldsymbol{C} = \boldsymbol{F^T.F} \quad \textbf{Eq. 3.37}$$

$$\boldsymbol{V^2} = \boldsymbol{B} = \boldsymbol{F.F^T} \quad \textbf{Eq. 3.38}$$

3.1.3.1.2 Green-Lagrange strain tensor

A convenient and widely used finite strain measure is the Green-Lagrange strain tensor $\boldsymbol{E}$ described in equation Eq. 3.39 [250]–[253], where $\boldsymbol{I}$ is the identity matrix, used to subtract rigid motion.

$$\boldsymbol{E} = \frac{1}{2}(\boldsymbol{C} - \boldsymbol{I}) = \frac{1}{2}(\boldsymbol{F}^{T}.\boldsymbol{F} - \boldsymbol{I}) \qquad \textbf{Eq. 3.39}$$

The computation of the three components of the Green-Lagrange strain tensor $\boldsymbol{E}$ has been performed assuming the modeled stack presented in Table 3.3 and a curvature radius of 12.5 mm. This value of curvature radius has been chosen in order to enable comparison with experimental measurements presented at the end of this chapter.

For symmetry reasons, strain and stress fields only depend of the position along the thickness axis of the sample. Fig. 3.8 shows the three diagonal components of the Green-Lagrange strain tensor across the thickness of the multilayer stack after bending over a cylinder featuring a 12.5 mm curvature radius.

On this graph, the position of the neutral plane and active SOI layer are highlighted with black dotted and dashed lines, respectively. For electrical considerations the strain and stress developed in the SOI active layer have to be taken into account. It can be observed that the strain components in the electrically active SOI layer are 0.03 %, 0 %, and -0.03 % in the longitudinal (defined as the direction parallel to the electronic transport), transverse and out-of-plane directions, respectively (Fig. 3.8-a).

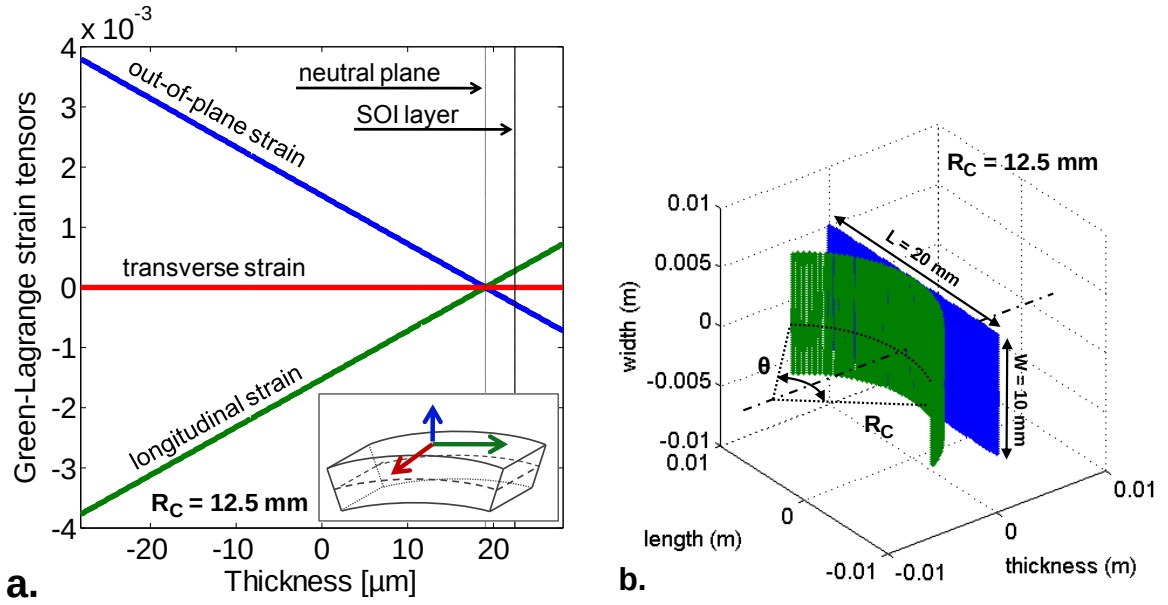


Fig. 3.8 – a. Green-Lagrange strain tensor components simulated at various positions along the thickness of the multilayer stack for a flexible CMOS sample bent over a cylinder with a 12.5 mm curvature radius. The neutral plane and active SOI layer are highlighted in dotted and dashed lines, respectively, and b. 3D view of the material before (blue) and after (green) bending.

3.1.3.1.3 Cauchy stress tensor

The second Piola-Kirchhoff stress tensor $\boldsymbol{S}$ –associated to the Green-Lagrange strain tensor $\boldsymbol{E}$ – is a function of the Lame coefficients λ and μ, described in equations Eq. 3.15 and Eq. 3.16 respectively, and the strain tensor $\boldsymbol{E}$, as written in equation Eq. 3.40. Assuming the relationship presented in Eq. 3.40 linking the second Piola-Kirchhoff stress tensor $\boldsymbol{S}$ and the Cauchy stress tensor $\boldsymbol{\sigma}$, the last one can be computed using equation Eq. 3.42 [250]–[253].

$$\boldsymbol{S} = \lambda \, \mathrm{tr}(\boldsymbol{E}) \, \boldsymbol{I} + 2\mu \, \boldsymbol{E} \qquad \textbf{Eq. 3.40}$$

$$\boldsymbol{S} = \det(\boldsymbol{F}) \, \boldsymbol{F}^{-1}.\boldsymbol{\sigma}.\boldsymbol{F}^{-T} \qquad \textbf{Eq. 3.41}$$

$$\boldsymbol{\sigma} = [\det(\boldsymbol{F})]^{-1} \boldsymbol{F}.\boldsymbol{S}.\boldsymbol{F}^{T} \qquad \textbf{Eq. 3.42}$$

Fig. 3.9 shows the three diagonal components of the Cauchy stress tensor across the thickness of the multilayer stack after bending over a cylinder featuring a 12.5 mm curvature radius.

Similarly to the representation of the strain tensor in Fig. 3.8-a, the position of the neutral plane and active SOI layer are highlighted with black dotted and dashed lines, respectively. For the same curvature radius of 12.5 mm, the associated stress components amount to 36 MPa, 12 kPa, and -36 MPa, respectively (Fig. 3.9-a). A more accurate insight is provided in Fig. 3.9-b that provides a zoom of the three components of stress in the front end and first layers of BEOL under bending.

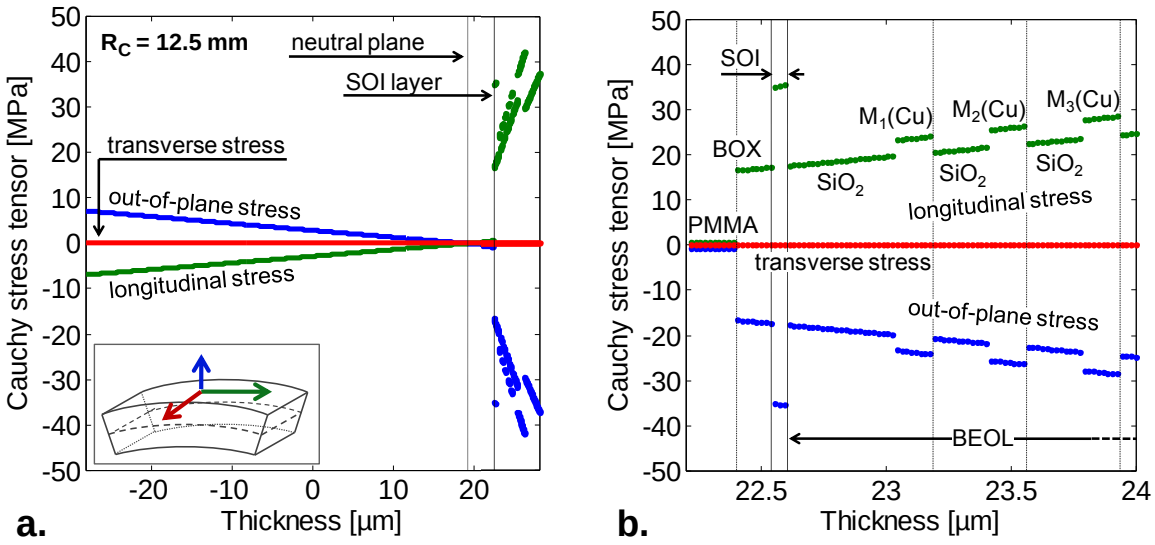


Fig. 3.9 – a. Cauchy stress tensor components simulated at various positions along the thickness of the multilayer stack for a flexible CMOS sample bent over a cylinder with a 12.5 mm curvature radius. The neutral plane and active SOI layer are highlighted in dotted and dashed lines, respectively, and b. Zoom-in of Fig. 3.9-a in the front end and first layers of BEOL of the bent flexible CMOS stack.

3.1.3.1.4 Piezoresistivity in electron-related SOI layer

From the determination of the stress distribution in the SOI layer, the variation of electron mobility can be thoroughly calculated using the piezoresistance coefficients of crystalline silicon (see paragraph *3.1.2.1.3 Piezoresistivity* [239], [240]. Assuming that the drain current I_{DS} is proportional to the electron mobility both in low and high field regimes [243], it is expected that the DC transconductance g_m, the unity gain cut-off frequency f_T, and the maximum oscillation frequency f_{MAX} will follow the same variation trend.

Using the neutral plane engineering methodology presented hereinbefore (see paragraph *3.1.2.2.1.3 Neutral plane engineering*), it is expected that moving the neutral plane close to the active SOI layer will reduce the value of stress and therefore the variation of electrical properties.

This assumption is furthermore supported in Fig. 3.10, where the longitudinal component of the stress tensor (Fig. 3.10-a) and the electron mobility variation (Fig. 3.10-b) in the SOI layer of the modeled stack are ploted as a function of the curvature radius for different thickness of the plastic handler. These simulations demonstrate that the variation of electrical properties can be minimized by a correct position of the neutral plane in the multilayer stack.

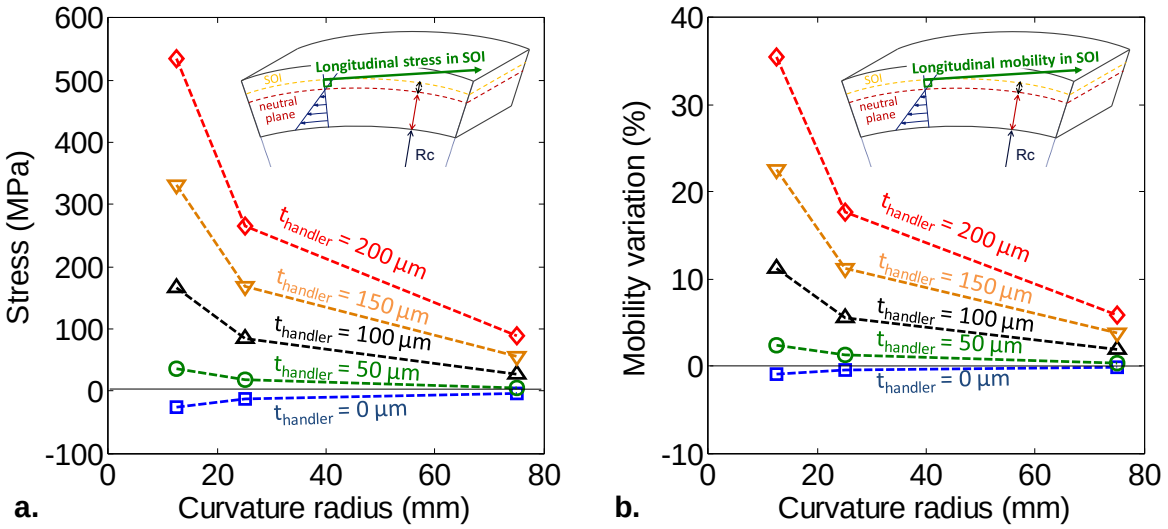


Fig. 3.10 – a. Longitudinal component of the stress tensor, and b. variation of electron mobility in the active SOI layer as a function of curvature radius for plastic handlers featuring different thicknesses.

Fig. 3.11-a emphasizes this point by showing the electron mobility variation in the SOI layer as a function of the stress generated in this active layer by bending over a cylinder of known radii (75 mm, 25 mm, or 12.5 mm) parametrized by the thickness of the plastic handler. A zoom-in of this graph around zero in presented in Fig. 3.11-b. It clearly shows that selecting a plastic handler featuring a thickness below a given limit (~30 µm) results in a neutral plane located above the active SOI layer. As a consequence, compressive stress will be generated in this layer under flexure, leading to a lowering of the mobility for electrons.

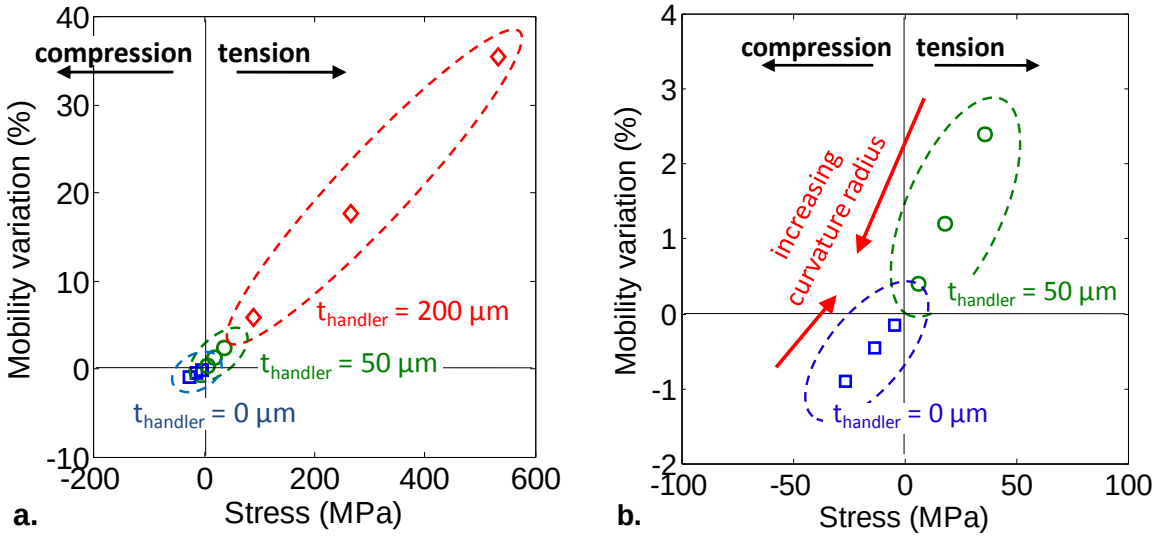


Fig. 3.11 – a. Variation of the electron mobility in the SOI layer as a function of stress generated under flexure for three curvature radii (75 mm, 25 mm, and 12.5 mm), and b. zoom-in of this graph around the optimal zero-variation point.

3.1.4 Conclusion on mechanical considerations

The first part of this last chapter presented the theoretical background required to understand and simulate the mechanical and electrical behavior of flexible CMOS devices and circuits under flexure. After briefly reviewing the linear elastic theory, the need for large rotation and therefore finite strain theory has been highlighted. A model of the CMOS multilayer stack used in this work has been suggested and used to compute the strain and stress distribution under flexure. Piezoresistivity has then been considered to relate stress level with variation of electrical properties in the active SOI layer of the modelled CMOS stack.

In parallel, a methodology to adapt to aggressive bending whitout leading to high variation of electrical figures-of-merit has been presentied. By carefully locating the neutral plane of the multilayer stack close to the active SOI layer, strain, stress, and thus electrical properties variation can be theoretically maintained under 5 % even after bending over a cylinder with a curvature radius of 12.5 mm. This can be performed by properly selecting the thickness of the plastic handler involved in the thinning and transfer process presented in chapter 2.

The simulated variations of electrical properties will now be compared with electrical measurement performed on bent CMOS devices in order to validate the model proposed in this section and the neutral plane engineering methodology.

3.2 Electrical performance of bent CMOS chips

3.2.1 Objectives and measurement setup

3.2.1.1.1 Objectives

Novel flexible electronic building blocks have been presented in this document. The first chapter explained the commercial need for high frequency flexible electronics. A fabrication technology was then proposed along with electrical characterizations in flat configuration. This last chapter theoretically detailed a methodology to stabilize the electrical properties under flexure. In order to completely validate the proposed neutral plane engineering methodology, the last required demonstration is to support the model developed in last section with electrical measurements on bent flexible CMOS chips.

After detailing solutions proposed in this work to enable high frequency characterization on non planar surfaces, the static and high frequency properties of flexible CMOS samples will be presented. Measurements shown in this section have been performed on flexible n-MOSFETs fabricated following the neutral plane engineering methodology presented hereinbefore, by selecting a 50 µm thick plasti handler. Their characteristics will systematically be compared with the expected simulated values for different levels of strain, i.e. different curature radii.

3.2.1.1.2 Bent measurement setup

External mechanical strain is applied to the flexible CMOS transistors by bending on a semi-cylinder of known radius. The DC and HF characterization of flexible n-MOSFETs is successively performed flatwise (as presented in chapter 2) and under flexure using various semi-cylinders: from the larger (Fig. 3.12-a) to the smaller one (Fig. 3.12-c), i.e. from the lower to the higher strain level. Note that neutral plane engineering ensures limited strain even at low radius. Vacuum sucking through these semi-cylinders enables good contact of the device under test to the rigid surface. Indeed, trapped air between the plastic handler and the rigid curved surface prevents from achieving a good quality contact between aluminium pads and HF probes.

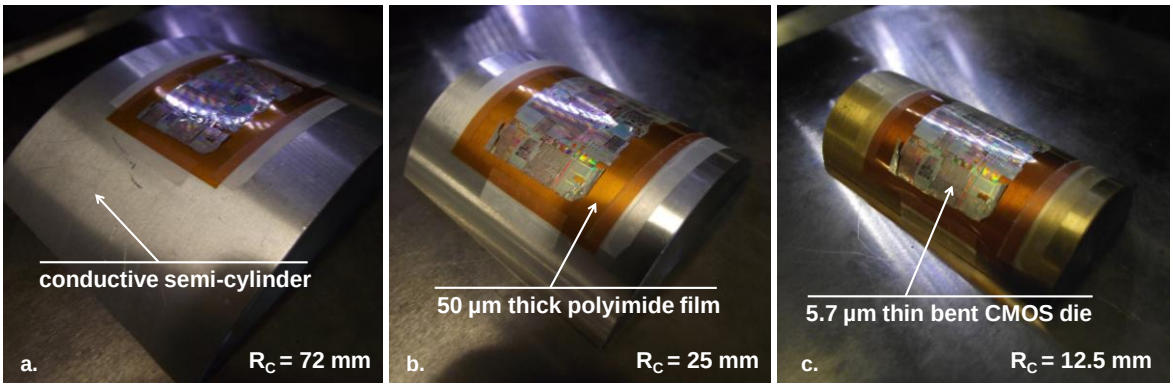


Fig. 3.12 – Conductive semi-cylinders of known radius used to maintain the thinned and flexible CMOS devices presented in this work in bent (i.e. strained) configuration while performing DC and RF characterization. Available curvature radii are: a. 75 mm, b. 25 mm, and c. 12.5 mm.

3.2.2 CMOS devices characterization under flexure

3.2.2.1 *Bent MOSFETs performance*

DC and HF measurements have been performed on a minimum set of four transistors to obtain statistically representative results. Electrical characteristics presented in this chapter focus on 60 nm and 65 nm gate long n-MOSFETs featuring a total gate width development of 64 µm coming from the parallel association of 0.5, 1 or 2 µm wide unitary gates.

3.2.2.1.1 DC characteristics

Static characteristics presented in Fig. 3.13-a and Fig. 3.13-b show I_{DS}-V_{DS}, I_{DS}-V_{GS} current-voltage and static transconductance g_{mDC} characteristics measured on a flexible transistor (featuring a gate length of 65 nm, a unitary gate finger width of 2 µm and a total width of 64 µm) both on flat and bent configurations. Very little discrepancy between DC characteristics measured in flat and bent configurations can be noticed from these two graphics, where measurements performed in flat configuration are represented by solid blue lines whereas characteristics of bent MOSFETs on cylinders with a 25 mm and 12.5 mm curvature radius are drawn in green dashed and red dotted lines, respectively.

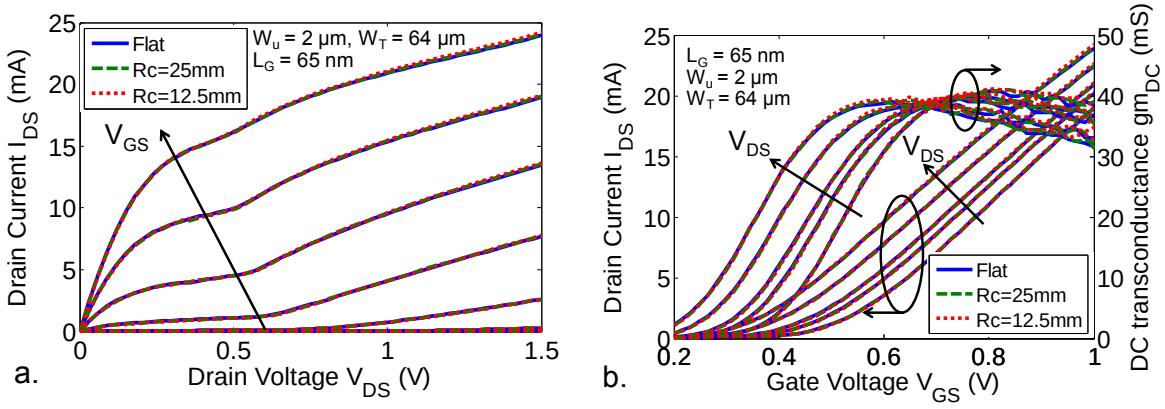


Fig. 3.13 – DC characteristics of flexible n-MOSFETs under flexure: a. Current-voltage I_{DS}-V_{DS} characteristics, and b. current-voltage I_{DS}-V_{GS} and static transconductance g_{mDC}, measured flatwise (blue lines), under flexure on semi-cylinders with a 25 mm curvature radius (green dashed lines) and a 12.5 mm curvature radius (red dotted lines). The considered n-MOSFET transistor features 32 parallel gate fingers of length L_G=65 nm and unitary width W_u=2 µm leading to a total gate width development W_T=64 µm.

The relative variations of I_{DS}-V_{DS} and g_{mDC}–V_{GS} characteristics between the bent and flat configurations are quantified in Fig. 3.14-a and Fig. 3.14-b. For each characteristic, variations after bending the flexible transistor on a cylinder with a 25 mm (respectively 12.5 mm) curvature radius are plotted in green dashed lines (respectively red dotted lines). Note that the special bias condition corresponding to V_{DS}=1.2 V and V_{GS}=0.8 V is highlighted in Fig. 3.14-a and Fig. 3.14-b as it corresponds to the maximum of static transconductance where HF figure-of-merits, namely the unity current gain f_T and Mason's gain cut-off frequencies f_{MAX}, are measured. It can already be noticed in Fig. 3.14 that static properties variation are limited to less than 5 % thanks to the optimal mechanical configuration of the multilayer stack.

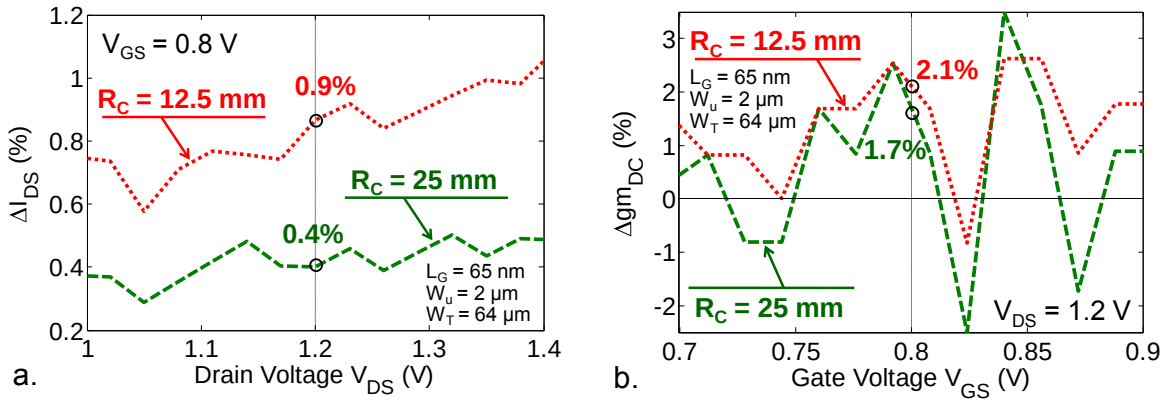


Fig. 3.14 – a. Relative variations of drain current I_{DS} versus V_{DS} and b. rRelative variations of DC transconductance g_{mDC} versus V_{GS} after transistor bending on 12.5 and 25 mm radius cylinder. V_{DS} =1.2 V and V_{GS} =0.8 V correspond to static bias conditions used to perform and extract HF figures-of-merit. The considered n-MOSFET transistor features 32 parallel gate fingers of length L_G=65 nm and unitary width W_u=2 µm leading to a total gate width development W_T=64 µm.

3.2.2.1.2 HF characteristics

In order to extract the intrinsic HF properties of measured devices, a deembedding procedure has classically been applied to eliminate contributions of transistor accesses, as presented in chapter 1. As the purpose of this chatper is to record variations of HF figures-of-merit upon bending, a simple and reliable 'OPEN' deembedding method had been selected instead of the 'Pad-Open-Short1-Short2' ('POSS') methodology used in previous chapter [156], [205] (see *1.2.2.2.2 On-wafer deembedding*, for more information about the 'OPEN' and 'POSS' deembedding methodologies).

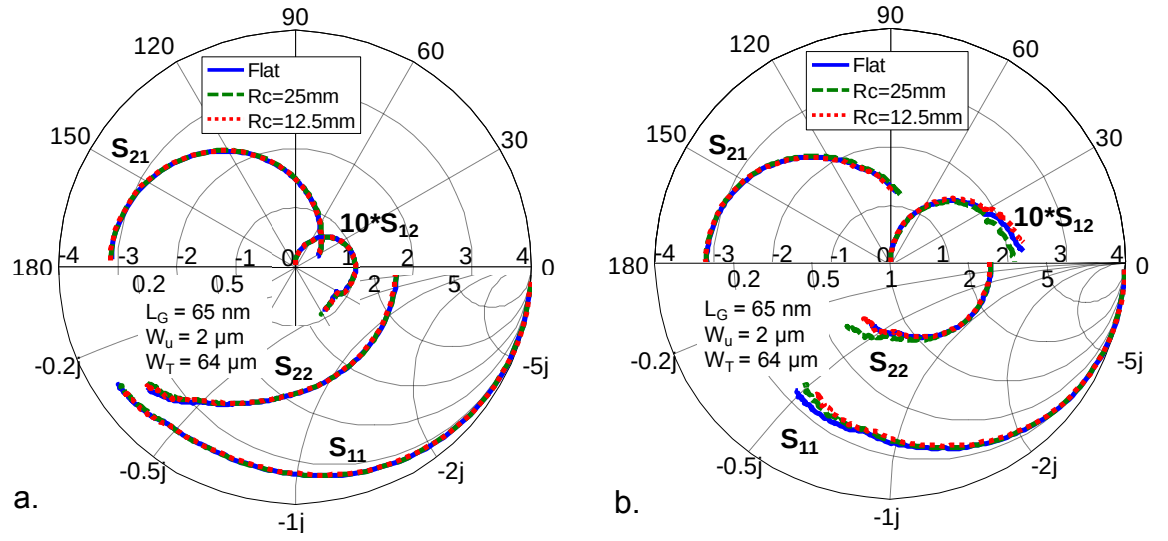
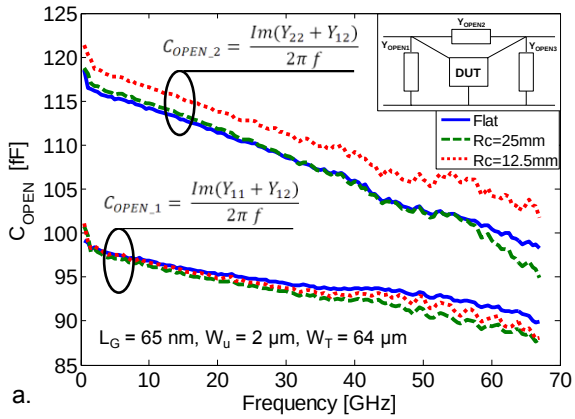


Fig. 3.15 – a. S parameters including extrinsic accesses measured on a flexible HF MOSFET featuring 32 parallel gate fingers of length L_G=65 nm and unitary width W_u=2 µm leading to a total gate development W_T=64 µm, b. deembedded S parameters measured on the same HF transistor, measured flatwise (solid blue lines), under flexure on semi-cylinders with a 25 mm curvature radius (green dashed lines) and a 12.5 mm curvature radius (red dotted lines).

The 'OPEN' deembedding method requires measurements of S parameters of the RF transistor of interest (S_{TOT}, Fig. 3.15-a) and of an open structure featuring the same accesses (S_{OPEN}). The Y parameters of the open structure (Y_{OPEN}) are subsequently subtracted from the extrinsic Y parameters measured on the transistor (Y_{TOT}) to obtain the characteristics of the intrinsic RF transistor (Y_{DUT}, Fig. 3.15-b). Equations Eq. 3.43 to Eq. 3.43 summarize this deembedding technology (as already presented in chatper 2).

Measured S parameters of the flexible HF transistor whose DC characteristics were presented in Fig. 3.13 are shown in Fig. 3.15-a before deembedding, and in Fig. 3.15-b after correction. Blue solid lines correspond to measurements performed on flat, green dashed and red dotted lines to measurements under flexure on a cylinder with 25 mm and 12.5 mm curvature radii, respectively. As in the case of DC measurements, both extrinsic and corrected S parameters exhibit only very slight variations regardless of measurement conditions, i.e. on flat or under flexure.



a.

$$Y = \begin{pmatrix} Y_{OPEN\_1} + Y_{OPEN\_2} & -Y_{OPEN\_2} \\ -Y_{OPEN\_2} & Y_{OPEN\_2} + Y_{OPEN\_3} \end{pmatrix}$$

$$Y_{DUT} = Y_{TOT} - Y_{OPEN}$$

$$C_{OPEN\_1} = \frac{Im(Y_{OPEN}(1,1) + Y_{OPEN}(1,2))}{2\pi f}$$

$$C_{OPEN\_2} = \frac{Im(Y_{OPEN}(2,2) + Y_{OPEN}(1,2))}{2\pi f}$$

b. **Eq. 3.43**, **Eq. 3.44**, **Eq. 3.45**, and **Eq. 3.46**

Fig. 3.16 – a. Open capacitances C_{OPEN1} and C_{OPEN2} characterizing extrinsic contributions of the HF transistor presented in Fig. 3.15 using the 'OPEN' methodology, measured flatwise (solid blue lines), under flexure on semi-cylinders with a 25 mm curvature radius (green dashed lines) and a 12.5 mm curvature radius (red dotted lines), and d. equations summarizing the 'OPEN' deembedding methodology.

For the sake of completeness, it should be noticed that the flexure-dependent difference in extrinsic S parameters (Fig. 3.16-a) at high frequency (> 50 GHz) tends to increase after deembedding correction (Fig. 3.16-b). As shown in Fig. 3.16-c, this effect can be explained by the increasing deviation of extrinsic capacitances of the open structure when the bending state is changed.

At this stage, it is also important to note that the comparison of HF properties for various bending states introduces numerous probe-to-pad landing and lifting operations. Part of the dispersion is therefore attributed to reproducibility errors introduced by these iterative probing steps.

In addition to these experimental inaccuracies, it is well know that the 'OPEN' deembedding method is less accurate at high frequency than more complex techniques [190]. However, the implementation of a more sophisticated deembedding methodology would also increase the number of passive structures that should be measured both on flat and under bending, resulting in increased dispersion due to the multiplication of probing steps. It was therefore deemed relevant to use the 'OPEN' deembedding method that provides reliable measurements at frequencies lower that 50 GHz even if some inaccuracies arise at higher frequencies.

This strategy is all the more legitimate that the current gain H_{21} (Fig. 3.17-a) and the Mason's gain U (Fig. 3.17-b) both closely follow the theoretical -20 dB/dec. slope from which f_T and f_{MAX} can be extracted by extrapolation from a high gain and low frequency region of the characteristics.

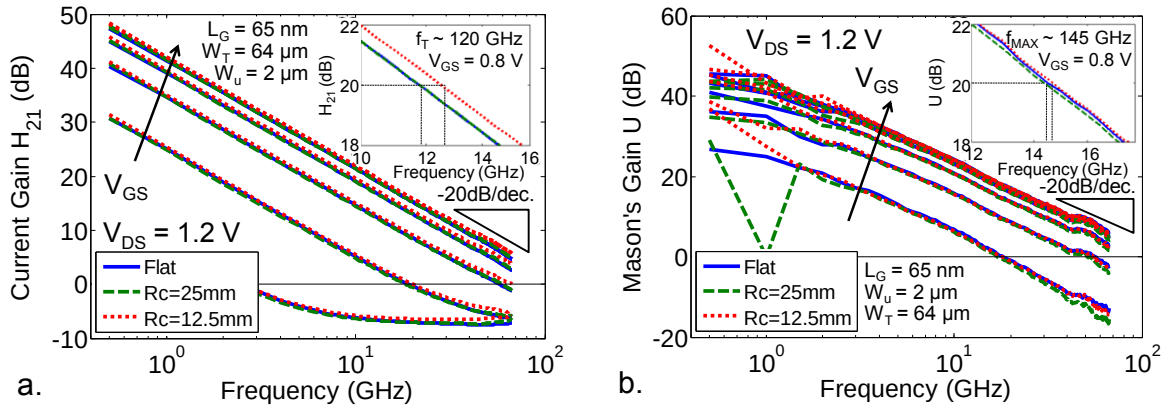


Fig. 3.17 – HF characteristics of flexible n-MOSFETs under flexure: a. Unity gain H_{21}, and b. Mason's gain U, measured flatwise, and under flexure (same line colors as previously) ; both figures demonstrate good agreement between measurements and the theoretical -20 dB/dec. slope. The considered n-MOSFET transistor features 32 parallel gate fingers of length L_G=65 nm and unitary width W_u=2 µm leading to a total gate width development W_T=64 µm.

To summarize results, Fig. 3.17-a and Fig. 3.17-b show almost identical unity current gain H_{21} and Mason's gain U on flat and bent configurations. Slight variations can be noticed in insets of Fig. 3.17-a and Fig. 3.17-b showing zoom-in around 20dB of gain, at frequencies ten times lower than f_T and f_{MAX}. Because the theoretical slope of -20 dB/dec. is well respected, the same f_T ~ 120 GHz and f_{MAX} ~ 145 GHz can be extracted on flat condition, and after bending on cylinders with a 25 mm and a 12.5 mm curvature radii.

The relative variations of H_{21} and U under bending with respect to the flat state is given in Fig. 3.18-a and Fig. 3.18-b at V_{DS}=1.2 V and V_{GS}=0.8 V that correspond to the maximum of transconductance where best frequency performance is expected. Green dashed lines (resp. red dotted lines) correspond to the variation after bending on a cylinder with a 25 mm (resp. 12.5 mm) curvature radius.

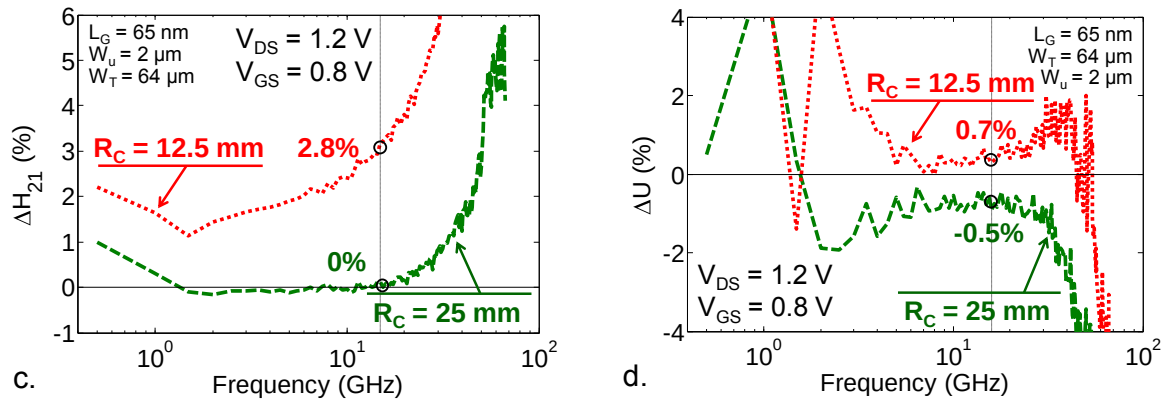


Fig. 3.18 – a. Relative variations of unity gain H_{21} and b. Mason's gain U versus frequency after transistor bending on 25 and 12.5 mm radius curvature. V_{DS} =1.2 V and V_{GS} =0.8 V correspond to static bias conditions used to perform and extract HF figures-of-merit.

Two important points deserve a special attention from the analysis of Fig. 3.18-a and Fig. 3.18-b. First, to ensure that relative variations are meaningful and effectively induced by mechanical bending rather than introduced by the deembedding procedure, two reference frequencies at f_T/10~12 GHz and f_{MAX}/10~14.5 GHz that are outlined by vertical dashed lines have deliberately been chosen. Characteristic frequencies highlighted by a vertical dashed line correspond to one tenth of the HF figure-of-merit (respectively unitary gain cut-off frequency f_T and maximum oscillation frequency f_{MAX}). Around these characteristic frequencies, measured gains strictly follow the theoretical -20 dB/dec. slope. It ensues that relative variations of the H_{21} and U gains at these characteristic frequencies directly translate into variations of f_T and f_{MAX}, respectively. Secondly, relative variations of H_{21} and U remain below 2.8% which is very close to the theoretical estimate previously calculated. These two reference frequencies are used in the following discussion that concentrates on a detailed analysis of the strain effect in neutral plane engineered flexible CMOS transistors.

3.2.2.2 *Validation of the neutral plane engineering method*

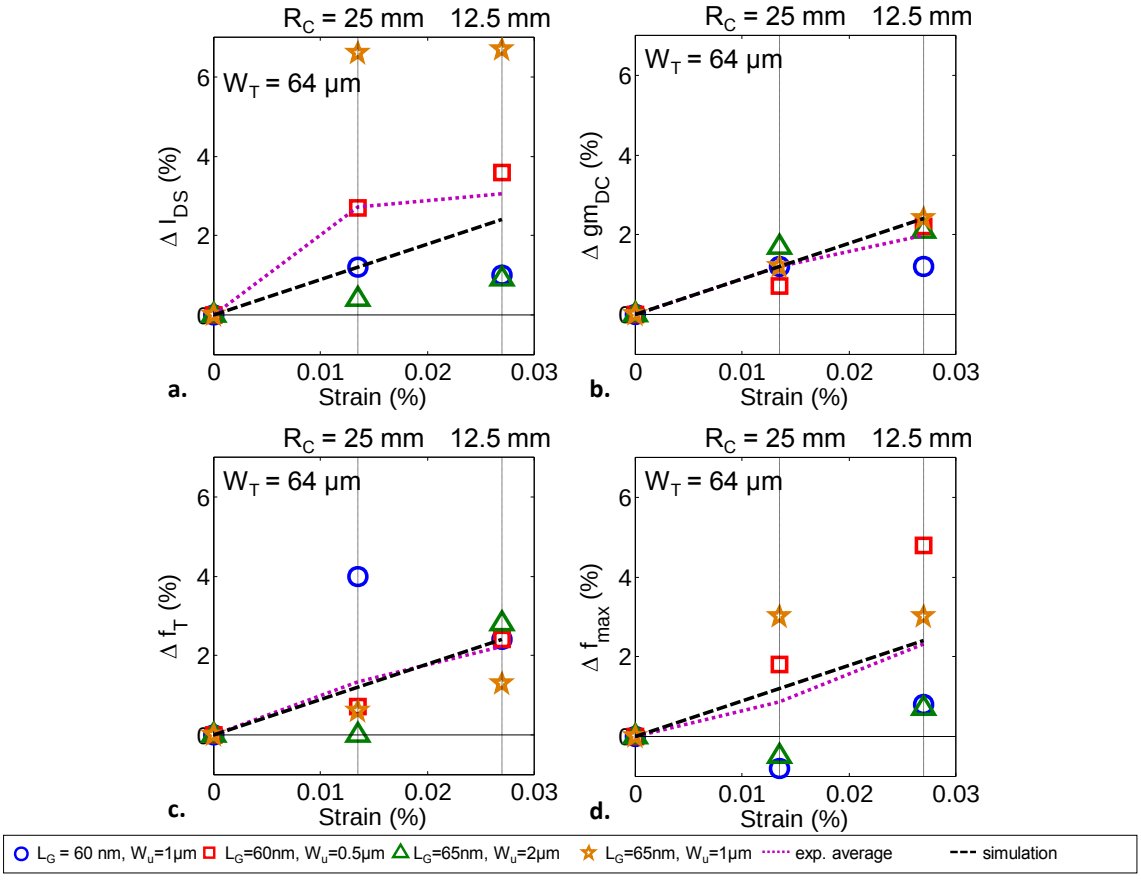


Fig. 3.19 – Comparison of measured and simulated variations of selected electrical parameters. Relative variations of a. drain current I_{DS}, b. DC transconductance gm_{DC}, c. unity gain cut-off frequency f_T, and d. maximum oscillation frequency f_{MAX} versus strain generated in the active SOI layer of four different transistors (symbols) under flexure on 25 and 12.5 mm radius cylinders, in addition to average of experimental data points (magenta dotted lines) and theoretical predictions (black dashed lines).

Fig. 3.19 and Fig. 3.20 give an extended view of relative variations of static (ΔI_{DS} and Δgm_{DC}), and high frequency (Δf_T and Δf_T) figures-of-merit. It globally demonstrates that electrical performance measured in bent configurations provides a good agreement with theoretical predictions.

Each of Fig. 3.19-a to Fig. 3.19-d shows relative variations with strain of one particular figure for four similar transistors with geometries that only slightly differ by their gate length, 60 or 65 nm, and by their unitary gate width, 0.5, 1 or 2 µm. In these four figures, individual measured data are represented by open symbols, average over four transistors is drawn in magenta dotted line and theoretical simulations are plotted in black dashed lines. It can be observed that averaged measured variations for each figure-of-merit agree remarkably well with theoretical predictions.

To complete the analysis, data are presented transistor-wise in Fig. 3.20-a to Fig. 3.20-d where relative variations of I_{DS}, gm_{DC}, f_{MAX} and f_T for each transistor are given as a function of bending. Once again it can be concluded that variations of electrical figures are limited to less than 5 % as expected from the strategy of neutral plane engineering.

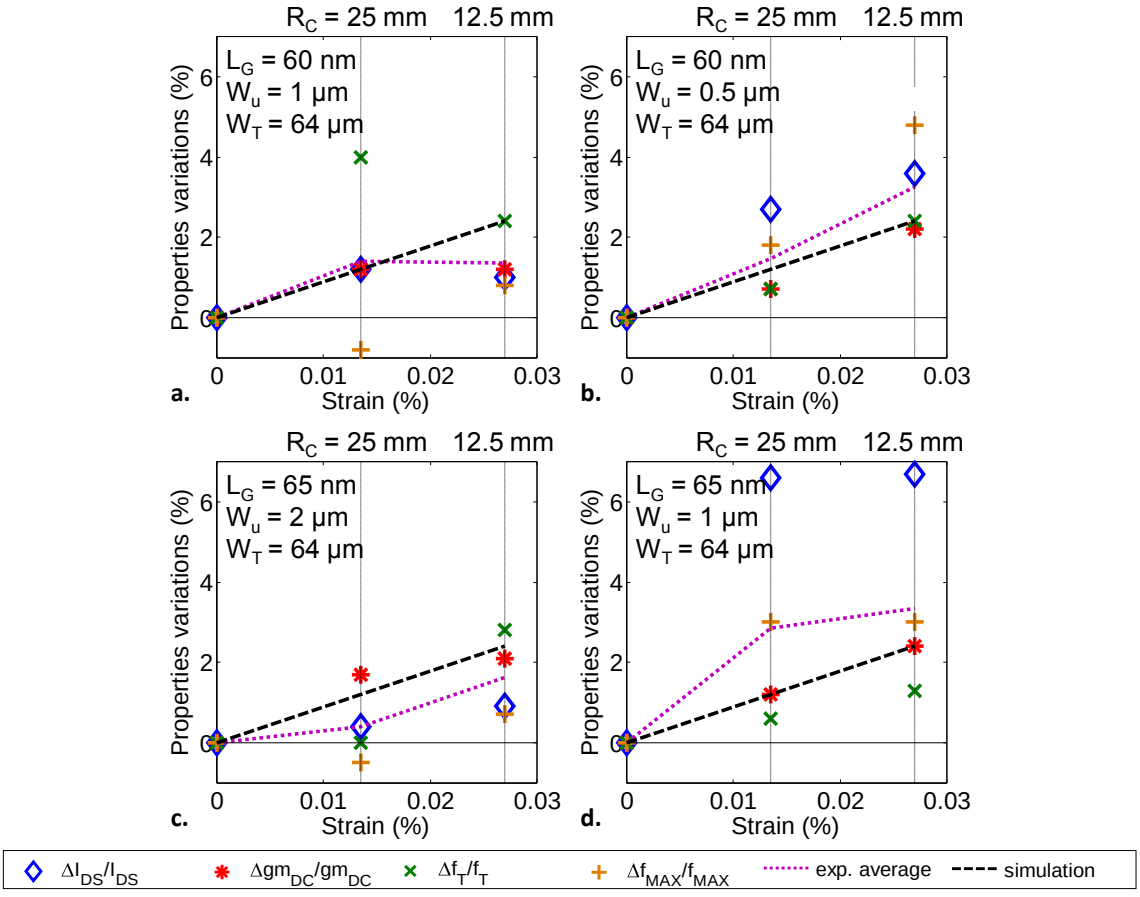


Fig. 3.20 – Comparison of measured and simulated variations of selected electrical parameters. Same relative variations of selected electrical parameters plotted for each different flexible n-MOSFET geometry: a. for a gate length L_G=60 nm and a unitary gate finger width W_u=1 µm, b. for L_G=60 nm and W_u=0.5 µm, c. for L_G=65 nm and W_u=2 µm, and d. for L_G=60 nm and W_u= 1 µm. The four n-MOSFETs feature a total gate width development of 64 µm.

A good agreement is therefore demonstrated in Fig. 3.19 and Fig. 3.20 between experimental variations of selected electrical parameters and their simulated counterpart after bending flexible MOSFETs on cylinders with a curvature radius of 25 and 12.5 mm.

3.2.3 Summary and comparison with recent reported work

This section will be concluded with a brief summary and comparison of the work described in this document with work from other research groups working in the field of highly bendable, high frequency flexible electronics. Fig. 3.21 provides a chart showing the cut-off frequency of flexible transistors as a function of the minimal achievable curvature radius at which HF properties are reported to be stable. The chosen definition is that the change of HF property (or static transconductance as cut-off frequencies were not always reported under flexure) should be less than 10 % at the considered curvature radius.

It should furthermore be noticed that most of the reported work in this field focuses on single devices that do not require the use of several layers of interconnection. The work presented in this document demonstrates competitive performance, in terms of high frequency and high bendability (i.e. low curvature radius) using a commercial 65 nm node SOI-CMOS technology comprising seven layers in the back-end-of-line interconnection network.

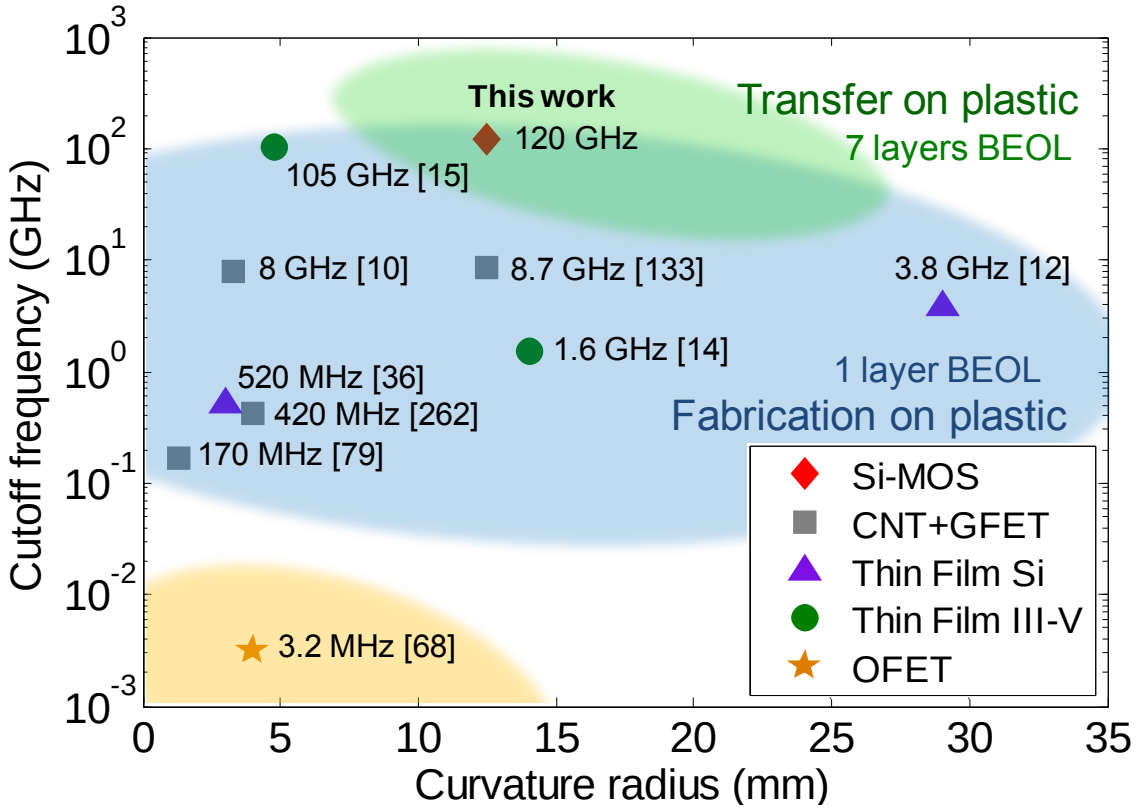


Fig. 3.21 – Chart comparing recent progress in the field of highly bendable high frequency flexible electronics by plotting the cut-off frequency of flexible transistors as a function of the minimal curvature radius at which HF properties have been reported to be stable (defined as varying by less than 10 % when compared to performance measured flatwise) [10], [12], [14], [15], [36], [68], [79], [133], [262].

3.3 Conclusion of the third chapter

This last chapter first presented the mechanical theoretical background required to accurately model the flexible CMOS devices realized and characterized flatwise in chapter 2. A complete model of the flexible CMOS stack was subsequently suggested and variations of electrical properties under flexure were estimated based on the piezoresistivity theory in silicon.

A novel methodology based on neutral plane engineering contributes to significantly reduce variations of electrical characteristics down to an acceptable level even under aggressive bending. This technique has been first simulated and in a second part validated by static and high frequency measurements.

Results presented in this second section demonstrate that industrial 65 nm partially depleted SOI MOSFETs thinned to the micrometer-scale and transferred onto a plastic foil leads to high performance devices with high stability under flexure. Slight variations of electrical properties (< 5 %) even after bending flexible CMOS dies on a cylinder with a curvature radius in the centimeter range pave the way to promising applications for foldable HF systems taking advantage of new form factors for heterogeneous integration.

This work may lead to the development of foldable devices and circuits on plastic films operating in the 100 GHz frequency range for nomadic and SWAP constrained applications. Future investigations will bear on the characterization of HF circuits and communicating systems under flexure.

Conclusions and perspectives

The objectives of this work were to demonstrate the feasibility of high frequency, low noise and highly bendable building blocks to pave the way for high performance foldable electronics.

This research project has been conducted in the nanofabrication and characterization facilities of IEMN, in partnership with STMicroelectronics. It led to the development of a methodology suitable to transfer the high potential and capabilities of a mature, high performance, rigid 65 nm SOI-CMOS technology to applications where bendability (or non-planarity) is required.

Chapter 1

The conventional semiconductor and printed electronics industries have both shown interest in the field of smart and communicating flexible systems. The first chapter of this manuscript therefore reviewed the existing technologies reported in the literature to realize flexible transistors and circuits. This comparison has been mainly focused on the high frequency capabilities of the various technological approaches, by highlighting the highest cut-off frequencies. In addition, stability of the electrical performance upon bending on relatively small curvature radii, and capability to realize complex circuits have also been pointed out.

Starting from the field of organic and printed electronics for the realization of low cost and large area highly bendable devices, several strategies to provide higher performance were presented. The reason for this quest is that limitations related to carrier mobility and printing resolution confine printed organic devices and circuits to applications at low frequency and circuit complexity. To cope with frequency restrictions, the transfer of inorganic semiconductors layers has often been considered in the literature and led to demonstration in the GHz range.

However, these strategies rely on final patterning steps directly performed on a flexible foil. This impedes the use of high thermal budget and the fabrication of complex interconnection network, limiting electrical performance and circuit complexity. In contrast, the method presented in this work therefore relies on the thinning and transfer onto plastic foil of conventionally processed 65 nm SOI-CMOS technology.

Chapter 2

The complete thinning and transfer process is detailed in the second chapter of this work. A three-step thinning process has been developed to completely remove the silicon handler of the initial SOI wafer, only keeping the unaltered buried oxide, top silicon, and back-end-of-line metallization stack. The thinned active die is then transferred from its temporary carrier onto a plastic foil using a permanent adhesive layer. Optical and electron microscopy demonstrated that no visible degradation arises from the complete thinning and transfer methodology.

Electrical measurements were therefore performed and demonstrated similar static and high frequency (HF) characteristics of MOSFETs both on their initial rigid wafer and after transfer onto a flexible plastic foil. The unitary gain cut-off frequency f_T and maximum oscillation frequency f_{max} were then extracted from the HF measurements leading to the demonstration of perfectly matched cut-off frequencies before and after transfer. However, a slight decrease of the Mason's gain U values resulted in a maximum oscillation frequency reduced by 25-30% at the highest current levels. In order to understand this degradation, the small signal equivalent

circuit (SSEC) parameters were extracted before and after transfer on plastic and compared. The f_{max} performance reduction is thus partially attributed to the increase of the gate resistance resulting from the fabrication process. Noise characterizations were subsequently performed using the F_{50} method and the four parameter noise figure-of-merit were extracted using a single 50Ω noise measurement. Invariant noise performance and matching conditions of rigid and flexible MOSFETs were thus demonstrated.

This complete set of static, high frequency and noise characterizations demonstrates that the fabrication process presented in this work leads to the fabrication of high performance electronics on plastic.Characteristic frequencies f_T / f_{max} as high as 150 / 160 GHz were demonstrated, in addition to low noise potentialities: NF_{min} / G_a of 0.57 / 17.8 dB. This performance levels outperform, to our best knowledge the previous state-of-the-art.

Chapter 3

After studying CMOS chips on plastic in flatwise condition, the impact of bending has been taken into account. Modeling of the CMOS multilayer and simulation of the electrical performance variation due to bending has been investigated using large strain and piezoresistivity theories. From an application point of view, stable electrical performance upon deformation is highly desirable. Therefore, a methodology based on neutral plane engineering has been suggested to limit the impact of mechanical bending on electrical properties. Correctly tuning the plastic handler thickness reduces the neutral plane distance to the active layer. The strain level in the transistor channel, and therefore the electrical properties variation, can thus be lowered.

Static and high frequency measurements on bent SOI-CMOS dies validate this solution and demonstrate less than 5% change in drain current, static transconductance, cut-off, and maximum oscillation frequencies even after aggressive bending on a curvature radius of 12.5 mm. In conclusion, the work presented in this thesis proposes a novel solution towards high performance, mechanically flexible and performance stable integrated electronics.

Perspectives

Research conducted in this PhD work represents only a unitary building block to converge towards flexible complex circuits integrating sensing, signal processing, and communicating capabilities. Although this manuscript has briefly presented preliminary results on coplanar waveguides and low noise amplifiers transferred on plastic foil, integration of antennas, sensors, batteries and other components in line with the More-than-Moore philosophy is of great interest.

Future work in this field is projected for a systematic study of the high frequency performance of passive devices after transfer onto plastic foil, flatwise and under flexure. Solutions to demonstrate invariant performance after transfer would be a first step towards stable flexible circuits that do not require a specific design step. Circuits as amplifiers shown in this document could then be studied under flexure. And finally the co-integration of several different components (antennas, sensors, batteries, actuators) with signal processing would be a great achievement in terms of future applications and end-user products. Laser photo-thermal ablation has been identified as an enabling technology that complies with hard constraints (thermal, chemical, and contamination) imposed by flexible organic substrates. It is therefore projected to facilitate quantum leaps in heterogeneous integration of multifunctional systems with dissimilar material classes and components originating from incompatible processes.

Appendix 1: Selected flexible transistors

Table A1.1 – Comparison of selected (fully or partially) mass-printed organic transistors

Type	Printing method	Gate length (µm)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	on/off ratio	Comments	Ref.
p-OTFT	flexographic / gravure	16 / 23	0.1	10^5	-	[46]
p-OFET	gravure	100	5×10^{-4}	10^2	75% yield over 50,000 transistors	[47]
n-OTFT	several	50 *	0.85	10^6	-	[50]
p-OFET	gravure	30	4×10^{-2}	10^4	-	[62]
p-OFET	gravure	50	3×10^{-2}	8×10^4	-	[48]
p-OFET	screen	50	4×10^{-2}	10^5	-	[48]
p-OFET	gravure + offset	100	1.3×10^{-3}	3×10^2	4 kHz 7-stages ring oscillator, 1 $m.s^{-1}$ print speed	[49]
p-OTFT	gravure + inkjet	10	0.1	-	300 kHz transition frequency	[51]
p-OFET	offset	50	3×10^{-3}	10^3	Top-gate OFET	[53]
p-OFET	inkjet	15	0.17	10^4	-	[58]
p-OFET	inkjet	1.5	2×10^{-3}	10^4	Ar ion laser thermal sintering	[16], [57]
p-OTFT	inkjet	1	0.3	10^6	Bottom gate, f_T = 2 MHz	[59]
n-OTFT	inkjet	1	0.02	10^4	Bottom gate	[59]
n-SiFET	screen	200	0.7 **	2×10^3**	Si NP ink **	[55]
CNT TFT	inkjet	100	-	10^2	High density CNT f_T = 5 GHz **	[11]
p-OTFT	aerosol-jet	20	1.8	10^5	-	[61]

* conventional metal evaporation methods have been used for contact realization
** use of inorganic semiconductor ink based on silicon nanoparticles (NP), or carbon nanotubes (CNT)

Table A1.2 – Comparison of selected recent high frequency organic transistors

Material & device	Gate length (µm)	Mobility ($cm^2.V^{-1}.s^{-1}$)	On/off ratio	f_T (MHz)	Comments **	Ref.
n-, p-OTFTs &circuits	2	5×10^{-1} (p) 1×10^{-2} (n)	-	-	Normal operation down to Rc = 100 µm	**[8]**
n-, p-OTFTs	1	3×10^{-1} (p) 2×10^{-2} (n)	10^6 (p) 10^4 (n)	2 (p)	Ag nanoparticles inkjet printed source and drain electrodes (on glass and flexible plastic substrate)	[59]
p-OTFTs *	0.2	3.6×10^{-4}	10^4	2×10^{-2}	On rigid Si wafer	[74]
p-OFETs *	0.5	10^{-2}	-	2	On rigid Si wafer	**[72]**
p-OFETs *	0.25	2×10^{-2}	10^4	1.5	3D-OFETs, on glass	**[69]**
p-OFETs	1	2×10^{-1}	10^6	3.2	3D-OFETs bending down to 4 mm	**[68]**
n-, p-OTFTs	8	1×10^{-1} (p) 9×10^{-2} (n)	5×10^5 (p) 2×10^4 (n)	10^{-2} (p)	Micro-imprinting process 3D-OTFTs	**[70]**
n-OTFTs *	2	1.1	-	20	C_{60} TFTs on glass	**[73]**
n-, p-OTFTs *	2	7×10^{-1} (p) 2.2 (n)	-	11 (p) 28 (n)	Fabricated on rigid glass substrate	**[9]**
p-OTFTs	10	10^{-1}	-	0.3	Gravure, inkjet printing	[51]
p-OFETs*	1	2×10^{-2}	10^4	0.9	3D-OFETs, on glass	**[71]**
p-OFETs	0.1	5×10^{-1}	10^5	-	Normal operation down to R_C = 0.5 mm No change after 60,000 bending cycles (with R_C = 2 mm)	**[67]**

* non flexible devices: fabricated on rigid substrate only (silicon, or glass wafer mainly)
** when bending tests have been performed, curvature radius is refered to as R_C

Table A1.3 – Comparison of selected bottom-up nanostructure-based transistors on flexible films

Material & device	Gate length (µm)	Mobility ($cm^2.V^{-1}.s^{-1}$)	On/off ratio	f_T (GHz)	f_{max} (GHz)	Comments **	Ref.
p-SiNW FET	-	1.4×10^2	10^5	-	-	Fluid assisted assembly R_C = 3 mm	**[82], [104]**
InAs	1.4	-	10^2	1.1	1.8	Contact printing method	[78]
SWCNT FET	0.8	-	-	8	-	Dielectrophoresis Constant operation down to R_C = 3.3 mm	**[10]**
CNT TFT	100	-	10^2	5	-	Inkjet printed high density random CNT	**[11]**
CNT TFT	4	4.8×10^4	-	0.15	-	Random, ultrapure, high density CNTs	**[34]**
CNT TFT	4	-	1.4	0.32	-	Random, ultrapure, high density CNTs	**[35]**
CNT TFT	4	50	10^4	0.17	0.12	Constant operation down to R_C = 1.3 mm (over 2000 cycles)	**[79]**
SWCNT TFT	100	80	10^5	10^{-4}	-	Transfer printed random network 100 TFTs flexible ICs	**[80]**
CNT TFT	5	17	10^3-10^4	-	-	Stamp printing Operation at R_C=50µm	**[125]**
SWCNT	4	4.8×10^2	10^4 *	0.42 *	-	Stamp printed aligned SWCNTs, stable operation at R_C= 4mm	**[262]**
SWCNT TTFT ***	30-300	30	10^2	-	-	Stamp printing 2.2% of strain (i.e. Rc ~ mm scale)	**[126]**
graphene FET	0.17	10^2	-	8.7	0.55	Stable HF properties down to R_C = 12.5mm	**[133]**

* high on/off ratio and cut-off frequency values where demonstrated on rigid growth substrate only
** when bending tests have been performed, curvature radius is refered to as R_C
*** Transparent thin film transistor

Table A1.4 – Comparison of selected recent top-down nanostructure-based transistors on flexible films

Material & device	Gate length (µm)	Mobility ($cm^2.V^{-1}.s^{-1}$)	On/off ratio	f_T (GHz)	f_{max} (GHz)	Comments **	Ref.
InAs MOSFET	0.075	2.3×10^3	10^2	105	22.3	Dry stamp printing Stable g_m down to R_C= 4.8mm	**[15], [142]**
µs-Si TFT	2	-	-	3.8	12	Dry stamp printing Stable RF properties down to $R_C^{\perp}$ = +29mm and $R_C^{\perp}$ = -78 mm	**[12]**
µs-Si TFT	2.5	-	10^5	2.04	7.8	Dry stamp printing	**[13]**
µs-Si TFT	2	2.3×10^2	10^5	1.9	3.1	Dry stamp printing	**[37]**
µs-GaAs MESFET	2	-	10^6	1.55	-	Dry stamp printing < 20% change in static properties down to R_C= ±14mm	**[14], [140]**
µs-Si TFT	2	5.1×10^2	10^5	0.52	-	Dry stamp printing < 20% change in static properties, R_C= ±3mm (2000 cycles)	**[36], [136]**
µs-GaAs MESFET	15	-	-	-	-	Dry stamp printing +20 % I_{DS} at R_C= + 8.4 mm (3 cycles)	**[140], [143]**
µs-Si TFT	-	2.4×10^2	-	-	-	Dry stamp printing Normal operation down to R_C= ± 8 mm	**[138]**
µs-Si MOSFET	19	4.7×10^2	10^4	-	-	3D integration of µs-Si MOSFET, µs-GaN HEMT, and CNT TFT Dry stamp printing Stable performance down to R_C = 3.7 mm (over 2000 cycles)	**[144]**
µs-GaN HEMT	20	-	10^6	-	-		
SWCNT TFT	50	5.9	10^5	-	-		

* µs-Si or (respectively µs-GaAs) stands for microstructures (e.g. nanoribbons) of Si (respectively GaAs)
** when bending tests have been performed, curvature radius is refered to as R_C. If the strain direction has been reported, $R_C^{\perp}$ (respectively $R_C^{/\!/}$) means strain perpendicular (respectively parallel) to the current flow. Positive curvature radii refer to tension strain whereas negative sign denotes compressive strain.

Table A1.5 – Comparison of selected transistors fabricated on rigid wafers and transferred on foils

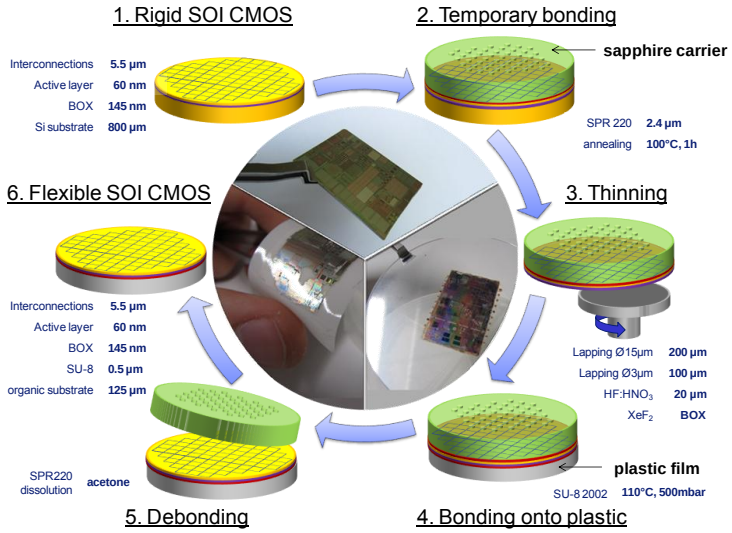
Material & device	Gate length (nm)	f_T* (GHz)	f_{max}	NFmin* (dB) @10GHz	Ga*	Chip thick (µm)	Strain (%)	Comments	Ref.
Si-MOSFET	180	48 (59)	-	1.1 (0.9)	12 (14)	30	0.7	Dry plasma (ICP[15])+ wet etching	[16], [163]
Si-MOSFET	180	47 (54)	-	1.2 (1.0)	13 (14)	30	0.4	Adhesive glue without annealing	**[164]**
Si-MOSFET	180	47	-	1.3	11	30	-		**[165]**
Si-MOSFET	160	-	-	-	-	100	0.3	+11% of $I_{DS,sat}$	**[263]**
Si-MOSFET	130	103 (118)	-	0.9 (0.8)	14 (15)	40	0.7	CMP[16] lapping	**[17], [166], [167]**
AlGaN/ GaN HEMT	2000	32	52	-	-	10	0.16	CMP lapping + wet etching Adhesive tape R_C = 15mm	**[155], [157]**
InGaAs/ InAlAs HEMT	100	120	280	-	-	-	-	Back side contacts	**[168]**
n-type Si-MOSFET	**65**	**150**	**160**	**0.6**	**18**	**6**	**0.03**	**This work**	**[156], [205]**
p-type Si-MOSFET	**65**	**110**	**130**	**0.6**	**17**	**6**	**0.03**		

"Chip thick." corresponds to the reported thickness of the thinned inorganic chip bonded on a plastic film
* values of figures-of-merit after application of strain are reported in brackets

[15] ICP : Inductively Coupled Plasma
[16] CMP : Chemical-Mechanical Polishing

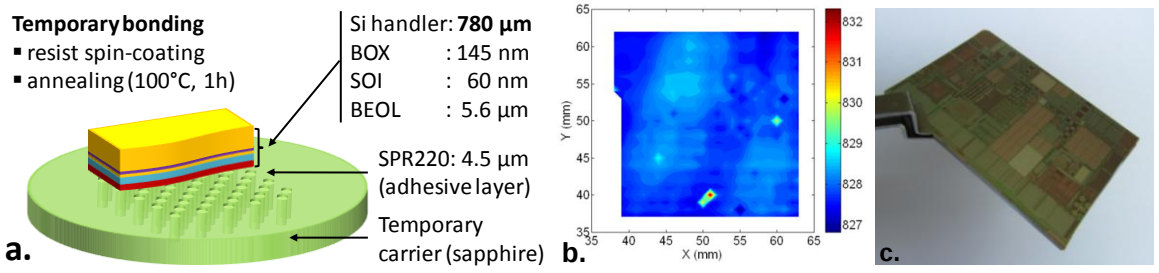
Appendix 2: Fabrication process

Table A2.1 – Detailed fabrication process compiled in a single table



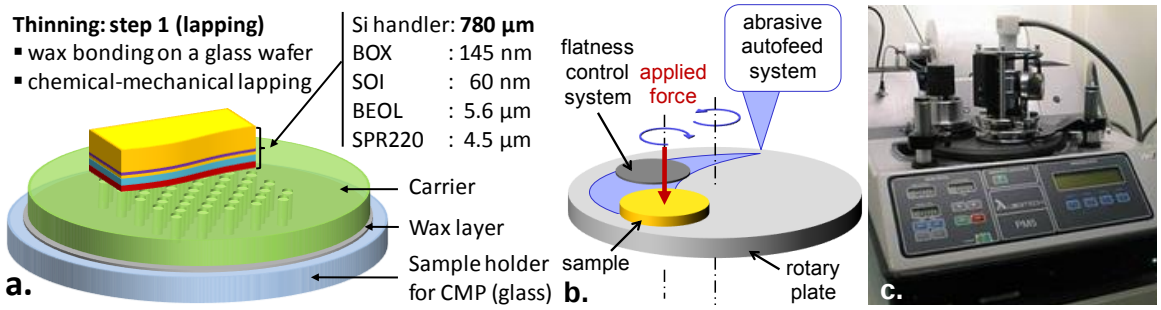
Temporary bonding

Object	Step description	Parameters
Temporary carrier	Cleaning	Chloroform ($CHCl_3$), 10 min + US[1] Acetone, 10 min + US Isopropanol, 10 min + US
	SPR220-4.5 filling	Perforated carrier filling with resist
Active sample	Dicing	Manual dicing using a diamond pencil
	Cleaning	Acetone, 10 min + US Isopropanol, 10 min + US
	Imaging	Optical microscopy imaging (reference)
	Dehydratation	200 °C, 10 min (hot plate)
	HMDS spin-coating	2000rpm/ 1000rpm.s^{-1}/ 20sec (closed lid)
	SPR220-4.5 spin-coating	3500rpm/ 1000rpm.s^{-1}/ 20sec (closed lid)
Both	Contacting	Manual contact
	Annealing	110 °C, 3 min (hot plate)
	Hardening	100 °C, 1 h (oven)
	Mapping	80×80 mm² (6400 points) => reference[2]



Chemical-mechanical lapping

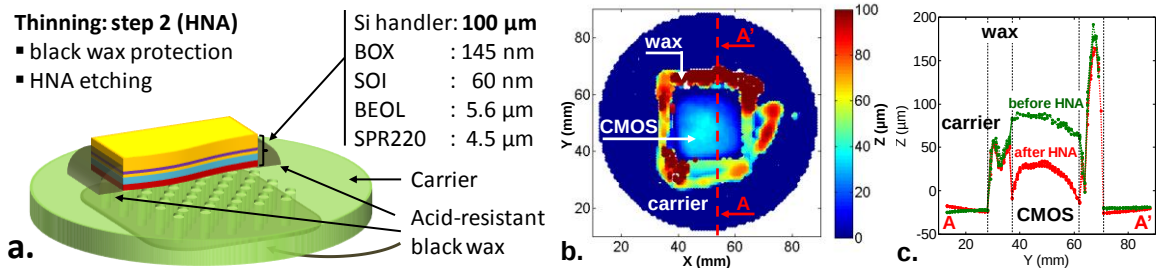
Object	Step description	Parameters
Glass holder	Cleaning	Acetone, 10 min + US IPA, 10 min + US
Active sample bonded on carrier	Wax bonding on a glass holder	Wafer Substrate Bonding Unit (Logitech) OCON-193 bonding wax (Logitech) 75 °C, 10 min, Controlled heating and colling
	Mapping	80×80 mm² (6400 points) => wax layer[3]
	Lapping	PM5 Lapping system (Logitech) Ø 15 µm, 10 w/w%, 50 rpm, 1.0 kg Down to 200 µm Ø 3 µm, 10 w/w%, 50 rpm, 1.0 kg Down to 100 µm
	Polishing (not required)	SF_1 polishing fluid (Logitech) 70 rpm, 1.0 kg, 10 min
	Mapping	80×80 mm² (6400 points) => lapping[3]
	Wax removal	OCON-178 Cleaning fluid (Logitech) 70°C, 30 min Isopropanol rinse, 10 min



HNA wet etching

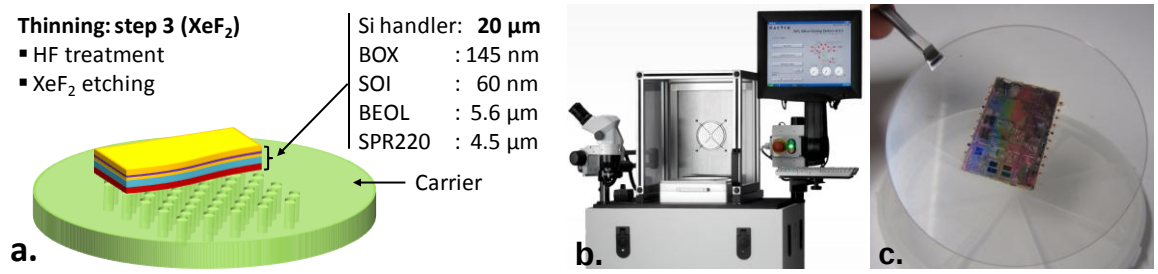
Object	Step description	Parameters
Active sample bonded on carrier	Acid-resistant wax coating (front side)	Wax W (Apiezon) Front side (around the active chip edges) Manual deposition or spin-coating
	Thickness measurement	Wax thickness measurement (until wax protects the BOX layer)
	Mapping	80×80 mm² (6400 points) => wax layer[3]
	Acid-resistant wax coating (back side)	Wax W (Apiezon) Back side (covering the carrier holes) Manual deposition or spin-coating Visual inspection
	HNA etching	49% HF : 65% HNO_3 – 10 : 90 (v/v%) Magnetic stirring, 100 rpm Manual vertical agitation Sample rotation (90°) every minute Down to 20 µm
	DI water rinse	De-ionized (DI) water rinse, 5 min
	Acid-resistant wax	OCON-178 Cleaning fluid (Logitech)

	stripping	70°C, 30 min Chloroform ($CHCl_3$), 1 min Isopropanol rinse, 10 min
	Mapping	80×80 mm² (6400 points) => HNA etch[3]



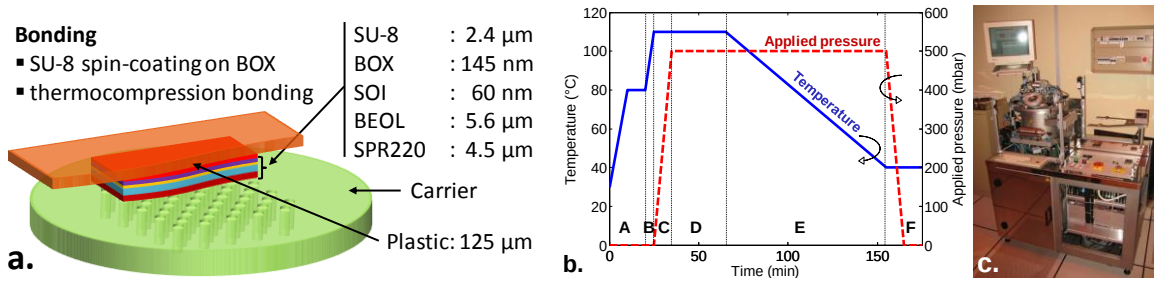
XeF2 dry etching

Object	Step description	Parameters
Active sample bonded on carrier	Native oxide removal	49% HF, 1 min DI water rinse, 1 min
	XeF_2 etching	Etch pulse duration: 10 sec Expansion pressure: 3.0 Torr Output pressure: 800 mTorr
	Imaging	Optical microscopy imaging (back side)
	Mapping	80×80 mm² (6400 points) => XeF_2 etch[3]



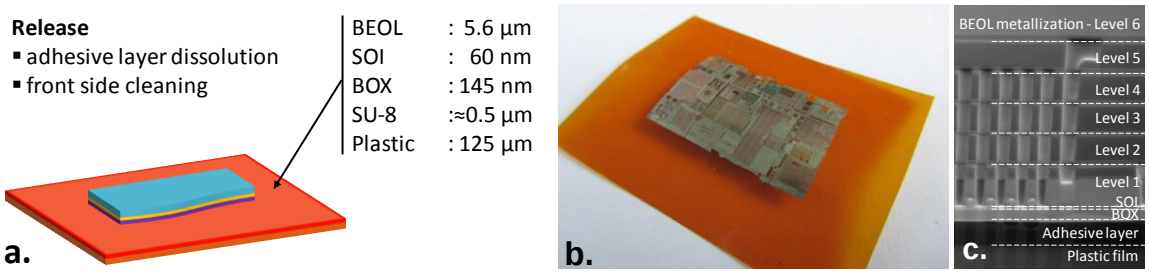
Bonding on a plastic film

Object	Step description	Parameters
Plastic film	Cleaning	Acetone, 10 min + US IPA, 10 min + US
Active sample bonded on carrier	SU8-2002 spin-coating	500rpm/ 1000rpm.s^{-1}/ 30sec (closed lid) 2000rpm/ 1000rpm.s^{-1}/ 30sec (closed lid) Manually removing excess resist
	Annealing	80 °C, 2 min + 110 °C, 3 min (hot plates)
	Bonding	SB6e wafer bonding (SÜSS MicroTech) Vacuum thermocompression 30 min, 110 °C, 500 mbar, 10^{-5} mbar



Release of the temporary carrier

Object	Step description	Parameters
Active sample bonded on plastic	Release	Remover 1165, room temperature Acetone, 10 min Isopropanol, 10 min
	Cleaning	O_2 plasma, 10 min
	Imaging	Optical microscopy imaging (front side)



[1] US stands for ultrasonic agitation.

[2] this thickness mapping provides an initial reference to compare with subsequent measurements.

[3] this term describes what can be extracted by substracting a measurement to the previous one.

References

[1] C. Saunier, *Rapport sur l'évolution du secteur de la micro/nanoelectronique*. Rapport N° 417, fait au nom de l'Office parlementaire d'évaluation des choix scientifiques et technologiques, 2008.

[2] G. E. Moore and others, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[3] G. E. Moore, "No exponential is forever: but 'Forever' can be delayed!," in *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, 2003, pp. 20 – 23 vol.1.

[4] International Technology Roadmap for Semiconductors, ITRS, "Executive Summary - 2011 Edition." 2011.

[5] International Technology Roadmap for Semiconductors, ITRS, "The next Step in Assembly and Packaging: System Level Integration in the package (SiP)." 2011.

[6] J. N. Burghartz, W. Appel, C. Harendt, H. Rempp, H. Richter, and M. Zimmermann, "Ultra-thin chips and related applications, a new paradigm in silicon technology," in *ESSCIRC, 2009. ESSCIRC '09. Proceedings of*, 2009, pp. 28 –35.

[7] R. H. Reuss, B. R. Chalamala, A. Moussessian, M. G. Kane, A. Kumar, D. C. Zhang, J. A. Rogers, M. Hatalis, D. Temple, G. Moddel, B. J. Eliasson, M. J. Estes, J. Kunze, E. S. Handy, E. S. Harmon, D. B. Salzman, J. M. Woodall, M. A. Alam, J. Y. Murthy, S. C. Jacobsen, M. Olivier, D. Markus, P. M. Campbell, and E. Snow, "Macroelectronics: Perspectives on technology and applications," *Proceedings of the IEEE*, vol. 93, no. 7, pp. 1239–1256, 2005.

[8] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "Flexible organic transistors and circuits with extreme bending stability," *Nature Materials*, vol. 9, no. 12, pp. 1015–1022, 2010.

[9] M. Kitamura and Y. Arakawa, "High Current-Gain Cutoff Frequencies above 10 MHz in n-Channel C 60 and p-Channel Pentacene Thin-Film Transistors," *Japanese Journal of Applied Physics*, vol. 50, p. 01BC01, Jan. 2011.

[10] N. Chimot, V. Derycke, M. F. Goffman, J. P. Bourgoin, H. Happy, and G. Dambrine, "Gigahertz frequency flexible carbon nanotube transistors," *Applied Physics Letters*, vol. 91, no. 15, 2007.

[11] J. Vaillancourt, H. Zhang, P. Vasinajindakaw, H. Xia, X. Lu, X. Han, D. C. Janzen, W.-S. Shih, C. S. Jones, M. Stroder, M. Y. Chen, H. Subbaraman, R. T. Chen, U. Berger, and M. Renn, "All ink-jet-printed carbon nanotube thin-film transistor on a polyimide substrate with an ultrahigh operating frequency of over 5 GHz," *Applied Physics Letters*, vol. 93, no. 24, 2008.

[12] L. Sun, G. Qin, J.-H. Seo, G. K. Celler, W. Zhou, and Z. Ma, "12-GHz Thin-Film Transistors on Transferrable Silicon Nanomembranes for High-Performance Flexible Electronics," *Small*, vol. 6, no. 22, pp. 2553–2557, 2010.

[13] H.-C. Yuan, G. K. Celler, and Z. Ma, "7.8-GHz flexible thin-film transistors on a low-temperature plastic substrate," *Journal of Applied Physics*, vol. 102, no. 3, 2007.

[14] Y. Sun, E. Menard, J. A. Rogers, H.-S. Kim, S. Kim, G. Chen, I. Adesida, R. Dettmer, R. Cortez, and A. Tewksbury, "Gigahertz operation in flexible transistors on plastic substrates," *Applied Physics Letters*, vol. 88, no. 18, 2006.

[15] C. Wang, J.-C. Chien, H. Fang, K. Takei, J. Nah, E. Plis, S. Krishna, A. M. Niknejad, and A. Javey, "Self-aligned, extremely high frequency III-V metal-oxide-semiconductor field-effect transistors on rigid and flexible substrates," *Nano Letters*, vol. 12, no. 8, pp. 4140–4145, 2012.

[16] H. L. Kao, A. Chin, B. F. Hung, C. F. Lee, J. M. Lai, S. P. McAlister, G. S. Samudra, W. J. Yoo, and C. C. Chi, "Low noise RF MOSFETs on flexible plastic substrates," *IEEE Electron Device Letters*, vol. 26, no. 7, pp. 489–491, 2005.

[17] H. L. Kao, A. Chin, C. C. Liao, Y. Y. Tseng, S. P. McAlister, and C. C. Chi, "DC-RF performance improvement for strained 0.13 μm MOSFETs mounted on a flexible plastic substrate," in *IEEE MTT-S International Microwave Symposium Digest*, 2006, pp. 2043–2046.

[18] Intel, "Moore's Law backgrounder." [Online]. Available: http://www.intel.com/pressroom/kits/events/moores_law_40th/.

[19] International Technology Roadmap for Semiconductors, ITRS, "Executive Summary." 2001.

[20] International Technology Roadmap for Semiconductors, ITRS, "Assembly and Packaging." 2009.

[21] International Technology Roadmap for Semiconductors, ITRS, "Interconnect." 2009.

[22] International Technology Roadmap for Semiconductors, ITRS, "Emerging Research Materials." 2011.

[23] International Technology Roadmap for Semiconductors, ITRS, "Executive Summary." 2009.

[24] B. Vigna, "More than Moore: micro-machined products enable new applications and open new markets," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, p. 8 pp. –8.

[25] Organic Electronics Association, OE-A, "Roadmap for Organic and Printed Electronics, 4th edition." 2011.

[26] D. Tonnies, M. Gabriel, B. Neubert, M. Hennemeyer, M. Zoberbier, and R. Zoberbier, "Introduction of a unified equipment platform for UV initiated processes in conjunction with the application of electrostatic carriers as thin wafer handling solution," in *Microelectronics and Packaging Conference, 2009. EMPC 2009. European*, 2009, pp. 1–6.

[27] J. Hermanowski, "Thin wafer handling—Study of temporary wafer bonding materials and processes," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, 2009, pp. 1–5.

[28] T. Itabashi, "Integrated materials enabling TSV/3D-TSV," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 1759–1763.

[29] T. Itabashi and M. P. Zussman, "High temperature resistant bonding solutions enabling thin wafer processing (characterization of polyimide base temporary bonding adhesive for thinned wafer handling)," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1877–1880.

[30] J. Charbonnier, S. Cheramy, D. Henry, A. Astier, J. Brun, N. Sillon, A. Jouve, S. Fowler, M. Privett, R. Puligadda, and others, "Integration of a temporary carrier in a TSV process flow," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 865–871.

[31] S. Pargfrieder, P. Kettner, M. Privett, and J. Ting, "Temporary Bonding and DeBonding Enabling TSV Formation and 3D Integration for Ultra-thin Wafers," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 1301–1305.

[32] B. Dang, P. Andry, C. Tsang, J. Maria, R. Polastre, R. Trzcinski, A. Prabhakar, and J. Knickerbocker, "CMOS compatible thin wafer processing using temporary mechanical wafer, adhesive and laser release of thin chips/wafers for 3D integration," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1393–1398.

[33] K. Tamura, K. Nakada, N. Taneichi, P. Andry, J. Knickerbocker, and C. Rosenthal, "Novel adhesive development for CMOS-compatible thin wafer handling," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1239–1244.

[34] J. Vaillancourt, X. Lu, X. Han, and D. C. Janzen, "High-speed thin-film transistor on flexible substrate fabricated at room temperature," *Electronics Letters*, vol. 42, no. 23, pp. 1365–1367, 2006.

[35] X. Han, D. C. Janzen, J. Vaillancourt, and X. Lu, "Printable high-speed thin-film transistor on flexible substrate using carbon nanotube solution," *Micro and Nano Letters*, vol. 2, no. 4, pp. 96–98, 2007.

[36] J.-H. Ahn, H.-S. Kim, K. J. Lee, Z. Zhu, E. Menard, R. G. Nuzzo, and J. A. Rogers, "High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates," *IEEE Electron Device Letters*, vol. 27, no. 6, pp. 460–462, 2006.

[37] H.-C. Yuan and Z. Ma, "Microwave thin-film transistors using Si nanomembranes on flexible polymer substrate," *Applied Physics Letters*, vol. 89, no. 21, 2006.

[38] D.-H. Kim, N. Lu, R. Ghaffari, Y.-S. Kim, S. P. Lee, L. Xu, J. Wu, R.-H. Kim, J. Song, Z. Liu, J. Viventi, B. de Graff, B. Elolampi, M. Mansour, M. J. Slepian, S. Hwang, J. D. Moss, S.-M. Won, Y. Huang, B. Litt, and J. A. Rogers, "Materials for multifunctional balloon catheters with capabilities in cardiac electrophysiological mapping and ablation therapy," *Nature Materials*, vol. 10, no. 4, pp. 316–323, 2011.

[39] D.-H. Kim, J. Viventi, J. J. Amsden, J. Xiao, L. Vigeland, Y.-S. Kim, J. A. Blanco, B. Panilaitis, E. S. Frechette, D. Contreras, D. L. Kaplan, F. G. Omenetto, Y. Huang, K.-C. Hwang, M. R. Zakin, B. Litt, and J. A. Rogers, "Dissolvable films of silk fibroin for ultrathin conformal bio-integrated electronics," *Nature Materials*, vol. 9, no. 6, pp. 511–517, 2010.

[40] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, 2006.

[41] N. Waldhoff, *Caractérisations et modélisations des technologies CMOS et BiCMOS de dernières générations jusque 220 GHz*. Université des Sciences et Technologies de Lille, 2009.

[42] B. Martineau, *Potentialités de la technologie CMOS 65nm SOI pour des applications sans fils en bande millimétrique*, Université des Sciences et Technologies de Lille. 2008.

[43] L. Bian, E. Zhu, J. Tang, W. Tang, and F. Zhang, "Recent progress in the design of narrow bandgap conjugated polymers for high-efficiency organic solar cells," 2012.

[44] D. Tobjörk and R. Österbacka, "Paper Electronics," *Advanced Materials*, vol. 23, no. 17, pp. 1935–1961, 2011.

[45] D. Deganello, J. A. Cherry, D. T. Gethin, and T. C. Claypole, "Patterning of micro-scale conductive networks using reel-to-reel flexographic printing," *Thin Solid Films*, vol. 518, no. 21, pp. 6113–6116, Aug. 2010.

[46] J. Jo, J.-S. Yu, T.-M. Lee, and D.-S. Kim, "Fabrication of Printed Organic Thin-Film Transistors Using Roll Printing," *Japanese Journal of Applied Physics*, vol. 48, no. 4, p. 04C181, Apr. 2009.

[47] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, and A. C. Hübler, "Uniformity of fully gravure printed organic field-effect transistors," *Materials Science and Engineering: B*, vol. 170, no. 1–3, pp. 93–98, Jun. 2010.

[48] J.-M. Verilhac, M. Benwadih, A.-L. Seiler, S. Jacob, C. Bory, J. Bablet, M. Heitzman, J. Tallal, L. Barbut, P. Frère, G. Sicard, R. Gwoziecki, I. Chartier, R. Coppard, and C. Serbutoviez, "Step toward robust and reliable amorphous polymer field-effect transistors and logic functions made by the use of roll to roll compatible printing processes," *Organic Electronics*, vol. 11, no. 3, pp. 456–462, Mar. 2010.

[49] A. C. Huebler, F. Doetz, H. Kempa, H. E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, and U. Hahn, "Ring oscillator fabricated completely by means of mass-printing technologies," *Organic Electronics*, vol. 8, no. 5, pp. 480–486, Oct. 2007.

[50] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler, and A. Facchetti, "A high-mobility electron-transporting polymer for printed transistors," *Nature*, vol. 457, no. 7230, pp. 679–686, Jan. 2009.

[51] H. Kang, R. Kitsomboonloha, J. Jang, and V. Subramanian, "High-Performance Printed Transistors Realized Using Femtoliter Gravure-Printed Sub-10 μm Metallic Nanoparticle Patterns and Highly Uniform Polymer Dielectric and Semiconductor Layers," *Advanced Materials*, vol. 24, no. 22, pp. 3065–3069, 2012.

[52] J. Noh, D. Yeom, C. Lim, H. Cha, J. Han, J. Kim, Y. Park, V. Subramanian, and G. Cho, "Scalability of Roll-to-Roll Gravure-Printed Electrodes on Plastic Foils," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 33, no. 4, pp. 275 –283, Oct. 2010.

[53] D. Zielke, A. C. Hübler, U. Hahn, N. Brandt, M. Bartzsch, U. Fügmann, T. Fischer, J. Veres, and S. Ogier, "Polymer-based organic field-effect transistor using offset printed source/drain structures," *Applied Physics Letters*, vol. 87, no. 12, pp. 123508–123508–3, Sep. 2005.

[54] E. Halonen, K. Kaija, M. Mantysalo, A. Kemppainen, R. Osterbacka, and N. Bjorklund, "Evaluation of printed electronics manufacturing line with sensor platform application," in *Microelectronics and Packaging Conference, 2009. EMPC 2009. European*, 2009, pp. 1 –8.

[55] M. Härting, J. Zhang, D. R. Gamota, and D. T. Britton, "Fully printed silicon field effect transistors," *Applied Physics Letters*, vol. 94, no. 19, pp. 193509–193509–3, May 2009.

[56] R. D. Deegan, O. Bakajin, T. F. Dupont, G. Huber, S. R. Nagel, and T. A. Witten, "Capillary flow as the cause of ring stains from dried liquid drops," *Nature*, vol. 389, no. 6653, pp. 827–829, Oct. 1997.

[57] S. H. Ko, J. Chung, H. Pan, C. P. Grigoropoulos, and D. Poulikakos, "Fabrication of multilayer passive and active electric components on polymer using inkjet printing and low temperature laser processing," *Sensors and Actuators A: Physical*, vol. 134, no. 1, pp. 161–168, Feb. 2007.

[58] S. E. Molesa, S. K. Volkman, D. R. Redinger, A. F. Vornbrock, and V. Subramanian, "A high-performance all-inkjetted organic transistor technology," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 1072 – 1074.

[59] T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk, and T. Someya, "Organic transistors manufactured using inkjet technology with subfemtoliter accuracy," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 105, no. 13, pp. 4976–4980, 2008.

[60] J.-U. Park, M. Hardy, S. J. Kang, K. Barton, K. Adair, D. kishore Mukhopadhyay, C. Y. Lee, M. S. Strano, A. G. Alleyne, J. G. Georgiadis, P. M. Ferreira, and J. A. Rogers, "High-resolution electrohydrodynamic jet printing," *Nature Materials*, vol. 6, no. 10, pp. 782–789, 2007.

[61] J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge, and C. D. Frisbie, "Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic," *Nature Materials*, vol. 7, no. 11, pp. 900–906, 2008.

[62] M. M. Voigt, A. Guite, D.-Y. Chung, R. U. A. Khan, A. J. Campbell, D. D. C. Bradley, F. Meng, J. H. G. Steinke, S. Tierney, I. McCulloch, H. Penxten, L. Lutsen, O. Douheret, J. Manca, U. Brokmann, K. Sönnichsen, D. Hülsenberg, W. Bock, C. Barron, N. Blanckaert, S. Springer, J. Grupp, and A. Mosley, "Polymer Field-Effect Transistors Fabricated by the Sequential Gravure Printing of Polythiophene, Two Insulator Layers, and a Metal Ink Gate," *Advanced Functional Materials*, vol. 20, no. 2, pp. 239–246, 2010.

[63] G. Horowitz, "Organic Field-Effect Transistors," *Advanced Materials*, vol. 10, no. 5, pp. 365–377, 1998.

[64] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM Journal of Research and Development*, vol. 45, no. 1, pp. 11 –27, Jan. 2001.

[65] Y. Yamashita, "Organic semiconductors for organic field-effect transistors," *Science and Technology of Advanced Materials*, vol. 10, no. 2, p. 024313, Apr. 2009.

[66] C. Wang, H. Dong, W. Hu, Y. Liu, and D. Zhu, "Semiconducting π-conjugated systems in field-effect transistors: a material odyssey of organic electronics," *Chem. Rev.*, vol. 112, no. 4, pp. 2208–2267, Apr. 2012.

[67] T. Sekitani, S. Iba, Y. Kato, Y. Noguchi, T. Someya, and T. Sakurai, "Ultraflexible organic field-effect transistors embedded at a neutral strain position," *Applied Physics Letters*, vol. 87, no. 17, pp. 173502–173502–3, Oct. 2005.

[68] M. Uno, K. Nakayama, J. Soeda, Y. Hirose, K. Miwa, T. Uemura, A. Nakao, K. Takimiya, and J. Takeya, "High-Speed Flexible Organic Field-Effect Transistors with a 3D Structure," *Advanced Materials*, vol. 23, no. 27, pp. 3047–3051, 2011.

[69] K. Kudo, T. Takano, H. Yamauchi, M. Iizuka, and M. Nakamura, "High-Speed Operation of Step-Edge Vertical-Channel Organic Transistors with Pentacene and 6,13-Bis(triisopropyl-silylethynyl) Pentacene," *Japanese Journal of Applied Physics*, vol. 49, no. 4, p. 04DK03, Apr. 2010.

[70] J. Jeon, B. C.-K. Tee, B. Murmann, and Z. Bao, "Micro-imprinted prism substrate for self-aligned short channel organic transistors on a flexible substrate," *Applied Physics Letters*, vol. 100, no. 4, pp. 043301–043301–4, Jan. 2012.

[71] T. Takano, H. Yamauchi, M. Iizuka, M. Nakamura, and K. Kudo, "High-Speed Operation of Vertical Type Organic Transistors Utilizing Step-Edge Structures," *Applied Physics Express*, vol. 2, no. 7, p. 071501, 2009.

[72] V. Wagner, P. Wöbkenberg, A. Hoppe, and J. Seekamp, "Megahertz operation of organic field-effect transistors based on poly(3-hexylthiopene)," *Applied Physics Letters*, vol. 89, no. 24, pp. 243515–243515–3, Dec. 2006.

[73] M. Kitamura and Y. Arakawa, "Current-gain cutoff frequencies above 10 MHz for organic thin-film transistors with high mobility and low parasitic capacitance," *Applied Physics Letters*, vol. 95, no. 2, pp. 023503–023503–3, Jul. 2009.

[74] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, "Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films," *Applied Physics Letters*, vol. 76, no. 14, pp. 1941–1943, Apr. 2000.

[75] A. J. Baca, J.-H. Ahn, Y. Sun, M. A. Meitl, E. Menard, H.-S. Kim, W. M. Choi, D.-H. Kim, Y. Huang, and J. A. Rogers, "Semiconductor Wires and Ribbons for High-Performance Flexible Electronics," *Angewandte Chemie International Edition*, vol. 47, no. 30, pp. 5524–5542, 2008.

[76] N. Rouhi, D. Jain, and P. J. Burke, "High-Performance Semiconducting Nanotube Inks: Progress and Prospects," *ACS Nano*, vol. 5, no. 11, pp. 8471–8487, 2011.

[77] X. Liu, Y.-Z. Long, L. Liao, X. Duan, and Z. Fan, "Large-Scale Integration of Semiconductor Nanowires for High-Performance Flexible Electronics," *ACS Nano*, vol. 6, no. 3, pp. 1888–1900, 2012.

[78] T. Takahashi, K. Takei, E. Adabi, Z. Fan, A. M. Niknejad, and A. Javey, "Parallel Array InAs Nanowire Transistors for Mechanically Bendable, Ultrahigh Frequency Electronics," *ACS Nano*, vol. 4, no. 10, pp. 5855–5860, 2010.

[79] C. Wang, J.-C. Chien, K. Takei, T. Takahashi, J. Nah, A. M. Niknejad, and A. Javey, "Extremely Bendable, High-Performance Integrated Circuits Using

Semiconducting Carbon Nanotube Networks for Digital, Analog, and Radio-Frequency Applications," *Nano Lett.*, vol. 12, no. 3, pp. 1527–1533, 2012.

[80] Q. Cao, H. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam, and J. A. Rogers, "Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates," *Nature*, vol. 454, no. 7203, pp. 495–500, Jul. 2008.

[81] S. J. Kang, C. Kocabas, H.-S. Kim, Q. Cao, M. A. Meitl, D.-Y. Khang, and J. A. Rogers, "Printed Multilayer Superstructures of Aligned Single-Walled Carbon Nanotubes for Electronic Applications," *Nano Lett.*, vol. 7, no. 11, pp. 3343–3348, 2007.

[82] M. C. McAlpine, R. S. Friedman, S. Jin, K. Lin, W. U. Wang, and C. M. Lieber, "High-Performance Nanowire Electronics and Photonics on Glass and Plastic Substrates," *Nano Lett.*, vol. 3, no. 11, pp. 1531–1535, 2003.

[83] X. Duan and Y. Huang, "Chapter 2 - Chemically Synthesized Semiconductor Nanowires for High-Performance Electronics and Optoelectronics," in *Semiconductor Nanomaterials for Flexible Technologies*, Oxford: William Andrew Publishing, 2010, pp. 27–66.

[84] C. Wang and Q. Cao, "Chapter 4 - Thin Films of Single-Walled Carbon Nanotubes for Flexible Electronic Device Applications," in *Semiconductor Nanomaterials for Flexible Technologies*, Oxford: William Andrew Publishing, 2010, pp. 105–128.

[85] S.-H. Jeong and K.-H. Lee, "Chapter 5 - Flexible Field Emitters Based on Carbon Nanotubes and Other Materials," in *Semiconductor Nanomaterials for Flexible Technologies*, Oxford: William Andrew Publishing, 2010, pp. 129–158.

[86] R. S. Wagner and W. C. Ellis, "VAPOR-LIQUID-SOLID MECHANISM OF SINGLE CRYSTAL GROWTH," *Applied Physics Letters*, vol. 4, no. 5, pp. 89–90, Mar. 1964.

[87] Y. Sun and J. A. Rogers, "Inorganic Semiconductors for Flexible Electronics," *Advanced Materials*, vol. 19, no. 15, pp. 1897–1916, 2007.

[88] Y. Xia, P. Yang, Y. Sun, Y. Wu, B. Mayers, B. Gates, Y. Yin, F. Kim, and H. Yan, "One-Dimensional Nanostructures: Synthesis, Characterization, and Applications," *Advanced Materials*, vol. 15, no. 5, pp. 353–389, 2003.

[89] W. Lu and C. M. Lieber, "Semiconductor nanowires," *Journal of Physics D: Applied Physics*, vol. 39, no. 21, pp. R387–R406, Nov. 2006.

[90] L.-E. Wernersson, C. Thelander, E. Lind, and L. Samuelson, "III-V Nanowires: Extending a Narrowing Road," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2047 – 2060, Dec. 2010.

[91] X. Zhou, J.-Y. Park, S. Huang, J. Liu, and P. L. McEuen, "Band Structure, Phonon Scattering, and the Performance Limit of Single-Walled Carbon Nanotube Transistors," *Phys. Rev. Lett.*, vol. 95, no. 14, p. 146805, 2005.

[92] S. A. Fortuna and X. Li, "GaAs MESFET With a High-Mobility Self-Assembled Planar Nanowire Channel," *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 593 – 595, Jun. 2009.

[93] Y. Li, J. Xiang, F. Qian, S. Gradečak, Y. Wu, H. Yan, D. A. Blom, and C. M. Lieber, "Dopant-Free GaN/AlN/AlGaN Radial Nanowire Heterostructures as High Electron Mobility Transistors," *Nano Lett.*, vol. 6, no. 7, pp. 1468–1473, Jul. 2006.

[94] X. Jiang, Q. Xiong, S. Nam, F. Qian, Y. Li, and C. M. Lieber, "InAs/InP Radial Nanowire Heterostructures as High Electron Mobility Devices," *Nano Lett.*, vol. 7, no. 10, pp. 3214–3218, Oct. 2007.

[95] S. A. Dayeh, D. P. R. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, and D. Wang, "High Electron Mobility InAs Nanowire Field-Effect Transistors," *Small*, vol. 3, no. 2, pp. 326–332, 2007.

[96] A. Ford, J. Ho, Z. Fan, O. Ergen, V. Altoe, S. Aloni, H. Razavi, and A. Javey, "Synthesis, contact printing, and device characterization of Ni-catalyzed, crystalline InAs nanowires," *Nano Research*, vol. 1, no. 1, pp. 32–39, 2008.

[97] P.-C. Chang, Z. Fan, C.-J. Chien, D. Stichtenoth, C. Ronning, and J. G. Lu, "High-performance ZnO nanowire field effect transistors," *Applied Physics Letters*, vol. 89, no. 13, pp. 133113–133113–3, Sep. 2006.

[98] P. Stokes and S. I. Khondaker, "High quality solution processed carbon nanotube transistors assembled by dielectrophoresis," *Applied Physics Letters*, vol. 96, no. 8, pp. 083110–083110–3, Feb. 2010.

[99] P.-C. Chen, G. Shen, H. Chen, Y. Ha, C. Wu, S. Sukcharoenchoke, Y. Fu, J. Liu, A. Facchetti, T. J. Marks, M. E. Thompson, and C. Zhou, "High-Performance Single-Crystalline Arsenic-Doped Indium Oxide Nanowires for Transparent Thin-Film Transistors and Active Matrix Organic Light-Emitting Diode Displays," *ACS Nano*, vol. 3, no. 11, pp. 3383–3390, Nov. 2009.

[100] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature*, vol. 441, no. 7092, pp. 489–493, May 2006.

[101] Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, "Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures," *Nature*, vol. 430, no. 6995, pp. 61–65, Jul. 2004.

[102] W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Lieber, "One-dimensional hole gas in germanium/silicon nanowire heterostructures," *PNAS*, vol. 102, no. 29, pp. 10046–10051, Jul. 2005.

[103] N. Rouhi, D. Jain, K. Zand, and P. J. Burke, "Fundamental Limits on the Mobility of Nanotube-Based Semiconducting Inks," *Advanced Materials*, vol. 23, no. 1, pp. 94–99, 2011.

[104] M. C. McAlpine, R. S. Friedman, and C. M. Lieber, "Nanoimprint Lithography for Hybrid Plastic Electronics," *Nano Lett.*, vol. 3, no. 4, pp. 443–445, Apr. 2003.

[105] N. Pimparkar, C. Kocabas, S. J. Kang, J. Rogers, and M. A. Alam, "Limits of Performance Gain of Aligned CNT Over Randomized Network: Theoretical Predictions and Experimental Validation," *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 593 –595, Jul. 2007.

[106] Z. Fan, J. C. Ho, Z. A. Jacobson, H. Razavi, and A. Javey, "Large-scale, heterogeneous integration of nanowire arrays for image sensor circuitry," *PNAS*, vol. 105, no. 32, pp. 11066–11070, Dec. 2008.

[107] M. C. P. Wang and B. D. Gates, "Directed assembly of nanowires," *Materials Today*, vol. 12, no. 5, pp. 34–43, May 2009.

[108] Y. Huang, X. Duan, Q. Wei, and C. M. Lieber, "Directed Assembly of One-Dimensional Nanostructures into Functional Networks," *Science*, vol. 291, no. 5504, pp. 630–633, Jan. 2001.

[109] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, and C. M. Lieber, "Logic Gates and Computation from Assembled Nanowire Building Blocks," *Science*, vol. 294, no. 5545, pp. 1313–1317, Sep. 2001.

[110] A. Tao, F. Kim, C. Hess, J. Goldberger, R. He, Y. Sun, Y. Xia, and P. Yang, "Langmuir−Blodgett Silver Nanowire Monolayers for Molecular Sensing Using Surface-Enhanced Raman Spectroscopy," *Nano Lett.*, vol. 3, no. 9, pp. 1229–1233, Sep. 2003.

[111] D. Whang, S. Jin, Y. Wu, and C. M. Lieber, "Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems," *Nano Lett.*, vol. 3, no. 9, pp. 1255–1259, Sep. 2003.

[112] A. R. Tao, J. Huang, and P. Yang, "Langmuir−Blodgettry of Nanocrystals and Nanowires," *Acc. Chem. Res.*, vol. 41, no. 12, pp. 1662–1673, Dec. 2008.

[113] S. Acharya, A. B. Panda, N. Belman, S. Efrima, and Y. Golan, "A Semiconductor-Nanowire Assembly of Ultrahigh Junction Density by the Langmuir–Blodgett Technique," *Advanced Materials*, vol. 18, no. 2, pp. 210–213, 2006.

[114] D. Wang, Y.-L. Chang, Z. Liu, and H. Dai, "Oxidation Resistant Germanium Nanowires: Bulk Synthesis, Long Chain Alkanethiol Functionalization, and Langmuir−Blodgett Assembly," *J. Am. Chem. Soc.*, vol. 127, no. 33, pp. 11871–11875, Aug. 2005.

[115] J. Park, G. Shin, and J. S. Ha, "Controlling orientation of V2O5 nanowires within micropatterns via microcontact printing combined with the gluing Langmuir–Blodgett technique," *Nanotechnology*, vol. 19, no. 39, p. 395303, Oct. 2008.

[116] X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, no. 6816, pp. 66–69, Jan. 2001.

[117] E. M. Freer, O. Grachev, X. Duan, S. Martin, and D. P. Stumbo, "High-yield self-limiting single-nanowire assembly with dielectrophoresis," *Nature Nanotechnology*, vol. 5, no. 7, pp. 525–530, 2010.

[118] S. Shekhar, P. Stokes, and S. I. Khondaker, "Ultrahigh Density Alignment of Carbon Nanotube Arrays by Dielectrophoresis," *ACS Nano*, vol. 5, no. 3, pp. 1739–1746, Mar. 2011.

[119] G. Yu, X. Li, C. M. Lieber, and A. Cao, "Nanomaterial-incorporated blown bubble films for large-area, aligned nanostructures," *Journal of Materials Chemistry*, vol. 18, no. 7, p. 728, 2008.

[120] G. Yu, A. Cao, and C. M. Lieber, "Large-area blown bubble films of aligned nanowires and carbon nanotubes," *Nature Nanotechnology*, vol. 2, no. 6, pp. 372–377, 2007.

[121] Z. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, and A. Javey, "Wafer-Scale Assembly of Highly Ordered Semiconductor Nanowire Arrays by Contact Printing," *Nano Lett.*, vol. 8, no. 1, pp. 20–25, Jan. 2008.

[122] A. Javey, Nam, R. S. Friedman, H. Yan, and C. M. Lieber, "Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics," *Nano Lett.*, vol. 7, no. 3, pp. 773–777, Mar. 2007.

[123] R. Yerushalmi, Z. A. Jacobson, J. C. Ho, Z. Fan, and A. Javey, "Large scale, highly ordered assembly of nanowire parallel arrays by differential roll printing," *Applied Physics Letters*, vol. 91, no. 20, pp. 203104–203104–3, Nov. 2007.

[124] X. Feng, M. A. Meitl, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Competing Fracture in Kinetically Controlled Transfer Printing," *Langmuir*, vol. 23, no. 25, pp. 12555–12560, Dec. 2007.

[125] S.-H. Hur, O. O. Park, and J. A. Rogers, "Extreme bendability of single-walled carbon nanotube networks transferred from high-temperature growth substrates to plastic and their use in thin-film transistors," *Applied Physics Letters*, vol. 86, no. 24, pp. 243502–243502–3, Jun. 2005.

[126] Q. Cao, S.-H. Hur, Z.-T. Zhu, Y. G. Sun, C.-J. Wang, M. A. Meitl, M. Shim, and J. A. Rogers, "Highly Bendable, Transparent Thin-Film Transistors That Use Carbon-Nanotube-Based Conductors and Semiconductors with Elastomeric Dielectrics," *Advanced Materials*, vol. 18, no. 3, pp. 304–309, 2006.

[127] F. Xu, J. W. Durham, B. J. Wiley, and Y. Zhu, "Strain-Release Assembly of Nanowires on Stretchable Substrates," *ACS Nano*, vol. 5, no. 2, pp. 1556–1563, Feb. 2011.

[128] K. Bradley, J.-C. P. Gabriel, and G. Grüner, "Flexible Nanotube Electronics," *Nano Lett.*, vol. 3, no. 10, pp. 1353–1355, Oct. 2003.

[129] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, "Self-Sorted, Aligned Nanotube Networks for Thin-Film Transistors," *Science*, vol. 321, no. 5885, pp. 101–104, Apr. 2008.

[130] M. E. Roberts, M. C. LeMieux, A. N. Sokolov, and Z. Bao, "Self-Sorted Nanotube Networks on Polymer Dielectrics for Low-Voltage Thin-Film Transistors," *Nano Lett.*, vol. 9, no. 7, pp. 2526–2531, Jul. 2009.

[131] R. D. Deegan, O. Bakajin, T. F. Dupont, G. Huber, S. R. Nagel, and T. A. Witten, "Contact line deposits in an evaporating drop," *Phys. Rev. E*, vol. 62, no. 1, pp. 756–765, Jul. 2000.

[132] J. Huang, R. Fan, S. Connor, and P. Yang, "One-Step Patterning of Aligned Nanowire Arrays by Programmed Dip Coating," *Angewandte Chemie International Edition*, vol. 46, no. 14, pp. 2414–2417, 2007.

[133] C. Sire, F. Ardiaca, S. Lepilliet, J.-W. T. Seo, M. C. Hersam, G. Dambrine, H. Happy, and V. Derycke, "Flexible gigahertz transistors derived from solution-based single-layer graphene," *Nano Letters*, vol. 12, no. 3, pp. 1184–1188, 2012.

[134] Z. Ma and G. Qin, "Chapter 3 - Fast Flexible Electronics Made from Nanomembranes Derived from High-Quality Wafers," in *Semiconductor Nanomaterials for Flexible Technologies*, Oxford: William Andrew Publishing, 2010, pp. 67–104.

[135] K. Zhang, J.-H. Seo, W. Zhou, and Z. Ma, "Fast flexible electronics using transferrable silicon nanomembranes," *Journal of Physics D: Applied Physics*, vol. 45, no. 14, p. 143001, Apr. 2012.

[136] E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, and J. A. Rogers, "A printable form of silicon for high performance thin film transistors on plastic substrates," *Applied Physics Letters*, vol. 84, no. 26, pp. 5398–5400, Jun. 2004.

[137] K. J. Lee, J. Lee, H. Hwang, Z. J. Reitmeier, R. F. Davis, J. A. Rogers, and R. G. Nuzzo, "A printable form of single-crystalline gallium nitride for flexible optoelectronic systems," *Small*, vol. 1, no. 12, pp. 1164–1168, 2005.

[138] E. Menard, R. G. Nuzzo, and J. A. Rogers, "Bendable single crystal silicon thin film transistors formed by printing on plastic substrates," *Applied Physics Letters*, vol. 86, no. 9, pp. 093507–093507–3, Feb. 2005.

[139] H.-C. Yuan, Z. Ma, M. M. Roberts, D. E. Savage, and M. G. Lagally, "High-speed strained-single-crystal-silicon thin-film transistors on flexible polymers," *Journal of Applied Physics*, vol. 100, no. 1, pp. 013708–013708–5, Jul. 2006.

[140] Y. Sun, S. Kim, I. Adesida, and J. A. Rogers, "Bendable GaAs metal-semiconductor field-effect transistors formed with printed GaAs wire arrays on plastic substrates," *Applied Physics Letters*, vol. 87, no. 8, pp. 083501–083501–3, Aug. 2005.

[141] A. J. Baca, M. A. Meitl, H. C. Ko, S. Mack, H.-S. Kim, J. Dong, P. M. Ferreira, and J. A. Rogers, "Printable Single-Crystal Silicon Micro/Nanoscale Ribbons, Platelets and Bars Generated from Bulk Wafers," *Advanced Functional Materials*, vol. 17, no. 16, pp. 3051–3062, 2007.

[142] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature*, vol. 468, no. 7321, pp. 286–289, 2010.

[143] Y. Sun and J. A. Rogers, "Fabricating Semiconductor Nano/Microwires and Transfer Printing Ordered Arrays of Them onto Plastic Substrates," *Nano Lett.*, vol. 4, no. 10, pp. 1953–1959, Oct. 2004.

[144] J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, and J. A. Rogers, "Heterogeneous Three-Dimensional Electronics by Use of Printed Semiconductor Nanomaterials," *Science*, vol. 314, no. 5806, pp. 1754–1757, Dec. 2006.

[145] "Goodfellow website." [Online]. Available: http://www.goodfellow.com/.

[146] "DuPont Teijin Films website." [Online]. Available: http://europe.dupontteijinfilms.com/.

[147] "Dow Corning website." [Online]. Available: http://www.dowcorning.com/.

[148] J. Lee, J. Wu, J. H. Ryu, Z. Liu, M. Meitl, Y.-W. Zhang, Y. Huang, and J. A. Rogers, "Stretchable Semiconductor Technologies with High Areal Coverages and Strain-Limiting Behavior: Demonstration in High-Efficiency Dual-Junction GaInP/GaAs Photovoltaics," *Small*, vol. 8, no. 12, pp. 1851–1856, 2012.

[149] X. Hu, P. Krull, B. de Graff, K. Dowling, J. A. Rogers, and W. J. Arora, "Stretchable Inorganic-Semiconductor Electronic Systems," *Advanced Materials*, vol. 23, no. 26, pp. 2933–2936, 2011.

[150] J. A. Rogers, T. Someya, and Y. Huang, "Materials and Mechanics for Stretchable Electronics," *Science*, vol. 327, no. 5973, pp. 1603–1607, Mar. 2010.

[151] D.-H. Kim, J.-H. Ahn, W. M. Choi, H.-S. Kim, T.-H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, and J. A. Rogers, "Stretchable and Foldable Silicon Integrated Circuits," *Science*, vol. 320, no. 5875, pp. 507–511, Apr. 2008.

[152] D.-Y. Khang, J. A. Rogers, and H. H. Lee, "Mechanical Buckling: Mechanics, Metrology, and Stretchable Electronics," *Advanced Functional Materials*, vol. 19, no. 10, pp. 1526–1536, 2009.

[153] D.-H. Kim, J. Xiao, J. Song, Y. Huang, and J. A. Rogers, "Stretchable, Curvilinear Electronics Based on Inorganic Materials," *Advanced Materials*, vol. 22, no. 19, pp. 2108–2124, 2010.

[154] D.-H. Kim, J. Song, W. M. Choi, H.-S. Kim, R.-H. Kim, Z. Liu, Y. Y. Huang, K.-C. Hwang, Y. Zhang, and J. A. Rogers, "Materials and noncoplanar mesh designs for integrated circuits with linear elastic responses to extreme mechanical deformations," *PNAS*, vol. 105, no. 48, pp. 18675–18680, Feb. 2008.

[155] M. Lesecq, V. Hoel, A. Lecavelier des Etangs-Levallois, E. Pichonat, Y. Douvry, and J. C. De Jaeger, "High performance of AlGaN/GaN HEMTs reported on adhesive flexible tape," *IEEE Electron Device Letters*, vol. 32, no. 2, pp. 143–145, 2011.

[156] A. Lecavelier des Etangs-Levallois, E. Dubois, M. Lesecq, F. Danneville, L. Poulain, Y. Tagro, S. Lepilliet, D. Gloria, C. Raynaud, and D. Troadec, "150-GHz RF SOI-CMOS technology in ultrathin regime on organic substrate," *IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1510–1512, 2011.

[157] N. Defrance, Y. Douvry, M. Lesecq, F. Lecourt, V. Hoel, A. Lecavelier des Etangs-Levallois, Y. Cordier, A. Ebongue, and J. C. De Jaeger, "Fabrication, characterization and physical analysis of AlGaN/GaN HEMTs on flexible substrates," *submitted to Transaction on Electron Devices*.

[158] C. Bowick, J. Blyler, and C. Ajluni, *RF Circuit Design*. Newnes, 2008.

[159] S. A. Campbell, *Fabrication Engineering at the Micro and Nanoscale*, 3rd ed. Oxford University Press, USA, 2007.

[160] S. Takyu, J. Sagara, and T. Kurosawa, "A study on chip thinning process for ultra thin memory devices," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 1511 –1516.

[161] S. Takyu, T. Kurosawa, N. Shimizu, and S. Harada, "Novel Wafer Dicing and Chip Thinning Technologies Realizing High Chip Strength," *MRS Online Proceedings Library*, vol. 970, p. null, 2006.

[162] K. De Munck, T. Chiarella, P. De Moor, B. Swinnen, and C. Van Hoof, "Influence of Extreme Thinning on 130-nm Standard CMOS Devices for 3-D Integration," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 322 –324, Apr. 2008.

[163] H. L. Kao, A. Chin, B. F. Hung, J. M. Lai, C. F. Lee, M.-F. Li, G. S. Samudra, C. Zhu, Z. L. Xia, X. Y. Liu, and J. F. Kang, "Strain-induced very low noise RF

MOSFETs on flexible plastic substrate," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2005, vol. 2005, pp. 160–161.

[164] H. L. Kao, A. Chin, C. C. Huang, B. F. Hung, K. C. Chiang, Z. M. Lai, S. P. McAlister, and C. C. Chi, "Low noise and high gain RF MOSFETs on plastic substrates," in *IEEE MTT-S International Microwave Symposium Digest*, 2005, vol. 2005, pp. 295–298.

[165] H. L. Kao, B. F. Hung, A. Chin, J. M. Lai, C. F. Lee, S. P. McAlister, and C. C. Chi, "Very low noise RF nMOSFETs on pastic by substrate thinning and wafer transfer," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 11, pp. 757–759, 2005.

[166] A. Chin, H. L. Kao, C. H. Kao, C. C. Liao, Y. Y. Tseng, and C. C. Chi, "Strain enhanced DC-RF performance of 0.13 m nMOSFETs on flexible plastic substrate," *Electronics Letters*, vol. 42, no. 14, pp. 827–829, 2006.

[167] H. L. Kao, C. C. Liao, S. P. McAlister, and A. Chin, "Improvement of the performance of strained 0.13 μm MOSFETs mounted on flexible plastic substrates," in *2007 International Semiconductor Device Research Symposium, ISDRS*, 2007.

[168] J. Shi, N. Wichmann, Y. Roelens, and S. Bollaert, "Microwave performance of 100nm-gate In0.53Ga0.47As/In0.52Al0.48As high electron mobility transistors on plastic flexible substrate," *Applied Physics Letters*, vol. 99, no. 20, pp. 203505 – 203505–3, Nov. 2011.

[169] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Springer, 1997.

[170] G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," *Journal of Applied Physics*, vol. 93, no. 9, pp. 4955–4978, May 2003.

[171] L. Jastrzebski, J. F. Corboy, and R. Soydan, "Issues and Problems Involved in Selective Epitaxial Growth of Silicon for SOI Fabrication," *J. Electrochem. Soc.*, vol. 136, no. 11, pp. 3506–3513, Jan. 1989.

[172] J. P. Colinge, H. K. Hu, and S. Peng, "Fabrication of thin silicon-on-insulator flims using laser recrystallisation," *Electronics Letters*, vol. 21, no. 23, pp. 1102 –1103, 1985.

[173] K. Izumi, M. Doken, and H. Ariyoshi, "C.M.O.S. devices fabricated on buried SiO2 layers formed by oxygen implantation into silicon," *Electronics Letters*, vol. 14, no. 18, pp. 593 –594, 1978.

[174] P. L. F. Hemment, K. J. Reeson, J. A. Kilner, R. J. Chater, C. Marsh, G. R. Booker, J. R. Davis, and G. K. Celler, "Novel dielectric/silicon planar structures formed by ion beam synthesis," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 21, no. 1–4, pp. 129–133, 1987.

[175] M. Kimura, K. Egami, M. Kanamori, and T. Hamaguchi, "Epitaxial film transfer technique for producing single crystal Si film on an insulating substrate," *Applied Physics Letters*, vol. 43, no. 3, pp. 263–265, Aug. 1983.

[176] W. P. Maszara, "Silicon-On-Insulator by Wafer Bonding: A Review," *J. Electrochem. Soc.*, vol. 138, no. 1, pp. 341–347, Jan. 1991.

[177] M. Bruel, "Silicon on insulator material technology," *Electronics Letters*, vol. 31, no. 14, pp. 1201 –1202, Jul. 1995.

[178] M. Bruel, B. Aspar, and A.-J. Auberton-Hervé, "Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding*1$," *Japanese Journal of Applied Physics*, vol. 36, no. Part 1, No. 3B, pp. 1636–1641, 1997.

[179] G. K. Celler, "SOI Technology Driving the 21st Century Ubiquitous Electronics," *ECS Trans.*, vol. 19, no. 4, pp. 3–14, May 2009.

[180] J.-L. Pelloie and A. Auberton-Hervé, "A new generation of IC processing: Low-power, high-performance SOI CMOS," *Solid State Technology*, vol. 44, p. 63, 2001.

[181] F. Gianesello, D. Gloria, C. Raynaud, S. Montusclat, S. Boret, and P. Touret, "Integrated Inductors in HR SOI CMOS technologies: on the economic advantage of SOI technologies for the integration of RF applications," in *SOI Conference, 2007 IEEE International*, 2007, pp. 119 –120.

[182] F. Gianesello, D. Gloria, S. Montusclat, C. Raynaud, S. Boret, G. Dambrine, S. Lepilliet, B. Martineau, and R. Pilard, "1.8 dB insertion loss 200 GHz CPW band pass filter integrated in HR SOI CMOS Technology," in *Microwave Symposium, 2007. IEEE/MTT-S International*, 2007, pp. 453 –456.

[183] B. Martineau, A. Cathelin, F. Danneville, A. Kaiser, G. Dambrine, S. Lepilliet, F. Gianesello, and D. Belot, "80 GHz low noise amplifiers in 65nm CMOS SOI," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, 2007, pp. 348 –351.

[184] S. Cristoloveanu, "Silicon on insulator technologies and devices: from present to future," *Solid-State Electronics*, vol. 45, no. 8, pp. 1403–1411, Aug. 2001.

[185] C. Raynaud, S. Haendler, G. Guegan, F. Gianesello, B. Martineau, P. Touret, and N. Planes, "65nm Low Power (LP) SOI Technology on High Resistivity (HR) Substrate for WLAN and Mmwave SOCs," *ECS Trans.*, vol. 19, no. 4, pp. 257–264, May 2009.

[186] C. Pavageau, *Utilisation des technologies CMOS SOI 130 nm pour des applications en gamme de fréquences millimétriques*. Université des Sciences et Technologies de Lille, 2005.

[187] J.-P. Colinge, "Subthreshold slope of thin-film SOI MOSFET's," *IEEE Electron Device Letters*, vol. 7, no. 4, pp. 244 – 246, Apr. 1986.

[188] B. Iñíguez, J.-P. Raskin, P. Simon, D. Flandre, and J. Segura, "A review of leakage current in SOI CMOS ICs: impact on parametric testing techniques," *Solid-State Electronics*, vol. 47, no. 11, pp. 1959–1967, Nov. 2003.

[189] P. Simonen, A. Heinonen, M. Kuulusa, and J. Nurmi, "Comparison of bulk and SOI CMOS technologies in a DSP processor circuit implementation," in *The 13th International Conference on Microelectronics, 2001. ICM 2001 Proceedings*, 2001, pp. 107 – 110.

[190] N. Waldhoff, C. Andrei, D. Gloria, S. Lepilliet, F. Danneville, and G. Dambrine, "Improved characterization methology for MOSFETs up to 220 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1237–1243, 2009.

[191] Y. Tagro, *Mise au point d'une methodologie de caracterisation des 4 parametres de bruit HF des Technologies CMOS et HBT avancees dans la bande 60-110 ghz : :*

«□ *developpement de systeme a impedance variable In-Situ*□ ». Université des Sciences et Technologies de Lille, 2010.

[192] G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, no. 12, pp. 987 – 993, Dec. 1979.

[193] P. Crozat, J. C. Henaux, and G. Vernet, "Precise determination of open circuit capacitance of coplanar probes for on-wafer automatic network analyser measurements," *Electronics Letters*, vol. 27, no. 16, pp. 1476 –1478, Aug. 1991.

[194] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM Calibrations with Automatic Determination of Load Inductance," in *ARFTG Conference Digest-Fall, 36th*, 1990, vol. 18, pp. 57 –63.

[195] P. J. van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A new straightforward calibration and correction procedure for 'on-wafer' high frequency S-parameter measurements (45 MHz–18 GHz)," 1987, pp. 70–73.

[196] A. Bracale, *Caractérisation et modélisation des transistors MOS sur substrat SOI pour des applications micro-ondes*. Université Pierre et Marie Curie Paris VI, 2001.

[197] G. Pailloncy, *Propriétés hyperfréquences et de bruit de MOSFETs sur substrat massif et SOI jusqu'au noeud technologique 65 nm*. Université des Sciences et Technologies de Lille, 2005.

[198] M. DEHAN, *Characterization and Modeling of SOI RF integrated components*. Université Catholique de Louvain (UCL), 2003.

[199] F. Danneville, "Microwave Noise and FET Devices," *IEEE Microwave Magazine*, vol. 11, no. 6, pp. 53 –60, Oct. 2010.

[200] A. van der Ziel, "Thermal Noise in Field-Effect Transistors," *Proceedings of the IRE*, vol. 50, no. 8, pp. 1808 –1812, Aug. 1962.

[201] A. Van Der Ziel, "Gate noise in field effect transistors at moderately high frequencies," *Proceedings of the IEEE*, vol. 51, no. 3, pp. 461 – 467, Mar. 1963.

[202] M. W. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1340 –1350, Sep. 1989.

[203] G. Dambrine, H. Happy, F. Danneville, and A. Cappy, "A new method for on wafer noise measurement," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 3, pp. 375 –381, Mar. 1993.

[204] G. Dambrine, J.-P. Raskin, F. Danneville, D. Vanhoenackel Janvier, J.-P. Colinge, and A. Cappy, "High-frequency four noise parameters of silicon-on-insulator-based technology MOSFET for the design of low-noise RF integrated circuits," *IEEE Transactions on Electron Devices*, vol. 46, no. 8, pp. 1733 –1741, Aug. 1999.

[205] Y. Tagro, A. Lecavelier des Etangs-Levallois, L. Poulain, S. Lepilliet, D. Gloria, C. Raynaud, E. Dubois, and F. Danneville, "High frequency noise potentialities of reported CMOS 65 nm SOI technology on flexible substrate," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2012 IEEE 12th Topical Meeting on*, 2012, pp. 89 –92.

[206] W. Heinrich, "Quasi-TEM description of MMIC coplanar lines including conductor-loss effects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 1, pp. 45 –52, Jan. 1993.

[207] H. Richter, H. D. Rempp, M.-U. Hassan, C. Harendt, N. Wacker, M. Zimmermann, and J. N. Burghartz, "Technology and design aspects of ultra-thin silicon chips for bendable electronics," in *IC Design and Technology, 2009. ICICDT '09. IEEE International Conference on*, 2009, pp. 149 –154.

[208] N. McLellan, N. Fan, S. Liu, K. Lau, and J. Wu, "Effects of Wafer Thinning Condition on the Roughness, Morphology and Fracture Strength of Silicon Die," *Journal of Electronic Packaging*, vol. 126, no. 1, p. 110, 2004.

[209] H. H. Jiun, I. Ahmad, A. Jalar, and G. Omar, "Effect of wafer thinning methods towards fracture strength and topography of silicon die," *Microelectronics Reliability*, vol. 46, no. 5–6, pp. 836–845, May 2006.

[210] O. Brand and G. K. Fedder, Eds., *Advances Micro & Nanosystems, volume 2: CMOS - MEMS*. 2008.

[211] K. R. Williams and R. S. Muller, "Etch rates for micromachining processing," *Journal of Microelectromechanical Systems*, vol. 5, no. 4, pp. 256 –269, Dec. 1996.

[212] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-Part II," *Journal of Microelectromechanical Systems*, vol. 12, no. 6, pp. 761 – 778, Dec. 2003.

[213] M. Steinert, J. Acker, S. Oswald, and K. Wetzig, "Study on the Mechanism of Silicon Etching in HNO3-Rich HF/HNO3 Mixtures," *J. Phys. Chem. C*, vol. 111, no. 5, pp. 2133–2140, Feb. 2007.

[214] H. Robbins and B. Schwartz, "Chemical Etching of Silicon II . The System , , , and," *J. Electrochem. Soc.*, vol. 107, no. 2, pp. 108–111, Jan. 1960.

[215] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions I . Orientation Dependence and Behavior of Passivation Layers," *J. Electrochem. Soc.*, vol. 137, no. 11, pp. 3612–3626, Jan. 1990.

[216] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions II . Influence of Dopants," *J. Electrochem. Soc.*, vol. 137, no. 11, pp. 3626–3632, Jan. 1990.

[217] U. Schnakenberg, W. Benecke, and D. Löchel, "NH4Oh-based etchants for silicon micromachining," *Sensors and Actuators A: Physical*, vol. 23, no. 1–3, pp. 1031–1035, Apr. 1990.

[218] U. Schnakenberg, W. Benecke, B. Löchel, S. Ullerich, and P. Lange, "NH4OH-based etchants for silicon micromachining: Influence of additives and stability of passivation layers," *Sensors and Actuators A: Physical*, vol. 25, no. 1–3, pp. 1–7, Oct. 1990.

[219] M. Shikida, K. Sato, K. Tokoro, and D. Uchikawa, "Differences in anisotropic etching properties of KOH and TMAH solutions," *Sensors and Actuators A: Physical*, vol. 80, no. 2, pp. 179–188, Mar. 2000.

[220] K. Sato, M. Shikida, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, "Anisotropic etching rates of single-crystal silicon for TMAH water solution as a

function of crystallographic orientation," *Sensors and Actuators A: Physical*, vol. 73, no. 1–2, pp. 131–137, Mar. 1999.

[221] S. Liebert, "Encapsulation of naked dies for bulk silicon etching with TMAH," *Microelectronics Reliability*, vol. 42, no. 12, pp. 1939–1944, Dec. 2002.

[222] K. Sato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, "Characterization of orientation-dependent etching properties of single-crystal silicon: effects of KOH concentration," *Sensors and Actuators A: Physical*, vol. 64, no. 1, pp. 87–93, Jan. 1998.

[223] G. T. A. Kovacs, N. I. Maluf, and K. E. Petersen, "Bulk micromachining of silicon," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1536 –1551, Aug. 1998.

[224] X. Zhu, D. W. Greve, and G. K. Fedder, "Characterization of silicon isotropic etch by inductively coupled plasma etch in post-CMOS processing," in *The Thirteenth Annual International Conference on Micro Electro Mechanical Systems, 2000. MEMS 2000*, 2000, pp. 568 –573.

[225] C. Cardinaud, M.-C. Peignon, and P.-Y. Tessier, "Plasma etching: principles, mechanisms, application to micro- and nano-technologies," *Applied Surface Science*, vol. 164, no. 1–4, pp. 72–83, Sep. 2000.

[226] A. A. Ayón, R. L. Bayt, and K. S. Breuer, "Deep reactive ion etching: a promising technology for micro- and nanosatellites," *Smart Materials and Structures*, vol. 10, no. 6, pp. 1135–1144, Dec. 2001.

[227] H. V. Jansen, M. J. de Boer, S. Unnikrishnan, M. C. Louwerse, and M. C. Elwenspoek, "Black silicon method: X. A review on high speed and selective plasma etching of silicon with profile control: an in-depth comparison between Bosch and cryostat DRIE processes as a roadmap to next generation equipment," *Journal of Micromechanics and Microengineering*, vol. 19, no. 3, p. 033001, Mar. 2009.

[228] N. H. Tea, V. Milanovic, C. A. Zincke, J. S. Suehle, M. Gaitan, M. E. Zaghloul, and J. Geist, "Hybrid postprocessing etching for CMOS-compatible MEMS," *Journal of Microelectromechanical Systems*, vol. 6, no. 4, pp. 363 –372, Dec. 1997.

[229] P. B. Chu, J. T. Chen, R. Yeh, G. Lin, J. C. P. Huang, B. A. Warneke, and S. J. Pister, "Controlled pulse-etching with xenon difluoride," in , *1997 International Conference on Solid State Sensors and Actuators, 1997. TRANSDUCERS '97 Chicago*, 1997, vol. 1, pp. 665 –668 vol.1.

[230] D. E. Ibbotson, D. L. Flamm, J. A. Mucha, and V. M. Donnelly, "Comparison of XeF2 and F-atom reactions with Si and SiO 2," *Applied Physics Letters*, vol. 44, no. 12, pp. 1129–1131, 1984.

[231] L. R. Arana, N. de Mas, R. Schmidt, A. J. Franz, M. A. Schmidt, and K. F. Jensen, "Isotropic etching of silicon in fluorine gas for MEMS micromachining," *Journal of Micromechanics and Microengineering*, vol. 17, no. 2, pp. 384–392, Feb. 2007.

[232] M. H. Hecht, R. P. Vasquez, F. J. Grunthaner, N. Zamani, and J. Maserjian, "A novel x #x2010;ray photoelectron spectroscopy study of the Al/SiO<inf>2</inf> interface," *Journal of Applied Physics*, vol. 57, no. 12, pp. 5256 –5261, Jun. 1985.

[233] "KEYENCE - serie LK-G." [Online]. Available: www.keyence.fr.

[234] "Physik Instrumente (PI) technical datasheet - M-403 · M-404 Precision Translation Stage Specifications." [Online]. Available: www.pi.ws.

[235] K. M. Wong, X. Zou, P. Chen, and K. M. Lau, "Transfer of GaN-Based Light-Emitting Diodes From Silicon Growth Substrate to Copper," *IEEE Electron Device Letters*, vol. 31, no. 2, pp. 132 –134, Feb. 2010.

[236] X. B. Zou, H. Liang, and K. M. Lau, "Light extraction enhancement from GaN-based thin-film LEDs grown on silicon after substrate removal using HNA solution," *physica status solidi (c)*, vol. 7, no. 7–8, pp. 2171–2173, 2010.

[237] M. S. Kulkarni, "A Review and Unifying Analysis of Defect Decoration and Surface Polishing by Chemical Etching in Silicon Processing†," *Ind. Eng. Chem. Res.*, vol. 42, no. 12, pp. 2558–2588, Jun. 2003.

[238] M. S. Kulkarni and H. F. Erk, "Acid-Based Etching of Silicon Wafers: Mass-Transfer and Kinetic Effects," *J. Electrochem. Soc.*, vol. 147, no. 1, pp. 176–188, Jan. 2000.

[239] C. S. Smith, "Piezoresistance Effect in Germanium and Silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954.

[240] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *Electron Devices, IEEE Transactions on*, vol. 29, no. 1, pp. 64 – 70, Jan. 1982.

[241] B. M. Haugerud, L. A. Bosworth, and R. E. Belford, "Mechanically induced strain enhancement of metal–oxide–semiconductor field effect transistors," *Journal of Applied Physics*, vol. 94, no. 6, pp. 4102–4107, Sep. 2003.

[242] S. Maikap, C.-Y. Yu, S.-R. Jan, M. H. Lee, and C. W. Liu, "Mechanically strained strained-Si NMOSFETs," *Electron Device Letters, IEEE*, vol. 25, no. 1, pp. 40 – 42, Jan. 2004.

[243] Y. Sun, S. E. Thompson, and T. Nishida, *Strain Effect in Semiconductors: Theory and Device Applications*. Springer, 2009.

[244] F. Rochette, *Etude et caractérisation de l'influence des contraintes mécaniques sur les propriétés du transport électronique dans les architectures MOS avancées*. Institut National Polytechnique de Grenoble (INPG), 2008.

[245] T. Guillaume, *Influence des contraintes mécaniques non-intentionnelles sur les performances des transistors MOS à canaux ultra-courts*. Institut National Polytechnique de Grenoble (INPG), 2005.

[246] J.-L. Chaboche, J. Lemaître, A. Benallal, and R. Desmorat, *Mécanique des matériaux solides*, 3e édition. Dunod, 2009.

[247] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," in *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, 2003, pp. 11.6.1 – 11.6.3.

[248] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology

featuring strained-silicon," *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 191 – 193, Apr. 2004.

[249] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Buf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam, "Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 96 –130, Jan. 2008.

[250] J. Garrigues, "Mécanique des milieux continus en déformations finies." 2002.

[251] J. Garrigues, *Fondements de la Mécanique des Milieux Continus*. Hermes Lavoisier, 2007.

[252] S. Forest, M. Amestoy, G. Damamme, S. Kruch, V. Maurel, and M. Mazière, "Mécanique des milieux continus." 2009.

[253] J. Besson, G. Cailletaud, J.-L. Chaboche, and S. Forest, *Non-Linear Mechanics of Materials*. Dordrecht: Springer, 2010.

[254] C. Kittel, *Introduction To Solid State Physics*, 8th Revised edition. John Wiley & Sons Inc, 2004.

[255] M. Levy, "Chapitre 1. Introduction to fundamentals of elastic constants," in *Handbook of Elastic Properties of Solids, Liquids, and Gases*, New York: Academic Press, 2001, pp. 1–35.

[256] J. J. Wortman and R. A. Evans, "Young's Modulus, Shear Modulus, and Poisson's Ratio in Silicon and Germanium," *Journal of Applied Physics*, vol. 36, no. 1, pp. 153 –156, Jan. 1965.

[257] C. Canali, F. Ferla, B. Morten, and A. Taroni, "Piezoresistivity effects in MOS-FET useful for pressure transducers," *Journal of Physics D: Applied Physics*, vol. 12, no. 11, pp. 1973–1983, Nov. 1979.

[258] W. Zhao, J. He, R. E. Belford, L.-E. Wernersson, and A. Seabaugh, "Partially depleted SOI MOSFETs under uniaxial tensile strain," *Electron Devices, IEEE Transactions on*, vol. 51, no. 3, pp. 317 – 323, Mar. 2004.

[259] C.-J. Chiang, C. Winscom, and A. Monkman, "Electroluminescence characterization of FOLED devices under two type of external stresses caused by bending," *Organic Electronics: physics, materials, applications*, vol. 11, no. 11, pp. 1870–1875, 2010.

[260] C.-J. Chiang, C. Winscom, S. Bull, and A. Monkman, "Mechanical modeling of flexible OLED devices," *Organic Electronics*, vol. 10, no. 7, pp. 1268–1274, Nov. 2009.

[261] C.-H. Hsueh, "Modeling of elastic deformation of multilayers due to residual stresses and external bending," *Journal of Applied Physics*, vol. 91, no. 12, p. 9652, 2002.

[262] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nature Nanotechnology*, vol. 2, no. 4, pp. 230–236, 2007.

[263] H. L. Kao, Y. C. Chang, B. S. Lin, M. H. Huang, and C. H. Kao, “Bending effect of Si MOSFETs on flexible plastic substrate,” in *Proceedings of the 7th International Caribbean Conference on Devices, Circuits and Systems, ICCDCS,* 2008.

Résumé en français

Depuis plus de 50 ans, l'industrie des semiconducteurs suit une croissance exponentielle, en augmentant performance et densité d'intégration des composants électroniques, tout en diminuant les coûts de fabrication [1]–[3]. Anticipant une limite à cette continuelle miniaturisation (*More-Moore*), d'intenses efforts de recherche ont été investis pour co-intégrer diverses fonctionnalités (*More-than-Moore*) [4], [5]. Dans ce contexte, l'électronique flexible, voire étirable, offre de nombreuses opportunités [6], [7].

L'industrie de l'électronique organique et imprimée permet de fabriquer à faible coût et sur de larges surfaces des dispositifs souples [8], mais dont la complexité et les fréquences caractéristiques sont limitées [9]. De nombreuses applications requèrant de plus hautes fréquences [4]–[6], différentes stratégies ont été dévelopées pour combiner performances électriques et souplesse mécanique [10]–[17].

Ces travaux de thèse, réalisés en partenariat avec *STMicroelectronics*, s'intègrent dans ce cadre et ont pour objectif la réalisation des briques de base nécessaires à la conception d'une électronique souple très hautes fréquences, à faible bruit et faible consommation. Ils sont présentés dans ce document en trois chapitres, chacun divisé en deux parties.

Le premier chapitre propose un aperçu du contexte de l'électronique flexible et plus spécialement des récents efforts développés pour accéder à de plus hautes fréquences. Différentes méthodes sont présentées, utilisant une approche ascendante (*bottom-up*) [10], [11], ou descendante (*top-down*) [12]–[15]. La combinaison d'une technologie CMOS conventionnelle amincie et d'un film organique souple est alors suggérée comme une solution prometteuse [16], [17]. La seconde partie de ce premier chapitre détaille donc les caractéristiques statiques, hyperfréquences et de bruit, ainsi que les méthodes de mesure associées, pour une technologie CMOS 65 nm sur substrat SOI (*silicon-on-insulator*).

Le second chapitre décrit la méthode de fabrication développée lors de ces travaux pour réaliser des circuits CMOS flexibles : basée sur l'amincissement de tranches processées puis leur transfert sur un film organique souple. Une stratégie d'amincissement en trois temps est détaillée pour permettre de complètement supprimer le substrat de silicium par la face arrière, sans endommager la couche d'oxyde enterré. Le report de ce multicouche aminci depuis un support temporaire vers le film souple final est alors réalisé. La deuxième partie de ce chapitre compare les caractéristiques des dispositifs CMOS rigides et flexibles, démontrant des performances similaires et donc (à notre connaissance) à l'état de l'art pour le domaine de l'électronique flexible, en terme de fréquence de coupure et de bruit.

Le dernier chapitre soulève la question de l'impact des déformations mécaniques des dispositifs souples sur leurs propriétés électriques. La flexion de ces multicouches est dans un premier temps décrite théoriquement. En vue d'applications industrielles, l'invariance des propriétés électriques est préférable, une méthodologie basée sur l'ingénierie du plan neutre est alors proposée pour réduire l'impact des déformations sur ces propriétés. Des mesures électriques réalisées sur des dispositifs CMOS courbés confirment cette solution et démontrent la possibilité de combiner à la fois hautes performances électriques (hautes fréquences, faible bruit et faible consommation), flexibilité mécanique et stabilité des propriétés électriques lors de déformations.

Une conclusion résume ces résultats et propose des perspectives pour de futurs travaux.

Chapitre 1 : Une électronique rapide et flexible

1.1 Récents développements de l'électronique flexible

L'industrie de la microélectronique a suivi un développement basé sur la miniaturisation des fonctions logiques et mémoires depuis la fin des années 1960 : *More Moore* (Fig. 1-a). Une nouvelle approche, *More than Moore*, basée sur l'augmentation de la valeur ajoutée par la cointégration de fonctions variées sur un même support évolue actuellement en parallèle (Fig. 1-b). Le domaine de l'électronique flexible s'intègre dans ce contexte, par l'apport de flexibilité mécanique à un système électronique. Ces dernières années, un besoin urgent de solutions technologiques permettant la réalisation de dispositifs flexibles performants a été exprimé et de nombreux efforts ont été investis dans cette voie (Fig. 1-c). Ce domaine, à la limite entre l'industrie des semiconducteurs et l'électronique organique, tend à bénéficier de certains avantages propres à ces deux secteurs : i) une forte densité d'intégration, une résolution décananométrique, de hautes performances et la complexité nécessaire à la réalisation de circuits, ainsi que ii) une flexibilité mécanique, l'intégration sur de larges surfaces et l'impression de dispositifs ou d'interconnections à faible coût.

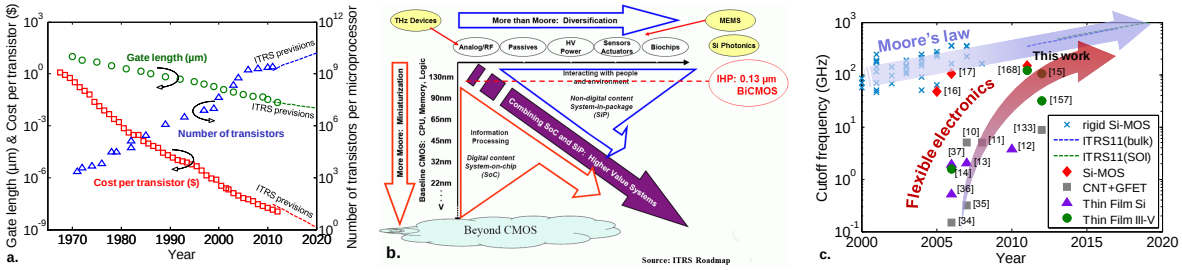


Fig. 22 – a. Loi de Moore, présentant l'augmentation de la complexité, des performances et la reduction des coûts de l'électronique moderne [2]–[4], b. Graphique présentant les recommendations de l'ITRS [4], et c. Evolution des fréquences de coupure des transistors rigides et flexibles.

Afin de comparer les différentes solutions technologiques proposées au cours des dernières années, certains paramètres doivent être introduits : i) la longueur de grille L_G, ii) les courants de drain à l'état passant I_{ON}, et bloqué I_{OFF}, ainsi que leur rapport on/off, iii) la transconductance statique g_m^{DC}, iv) la mobilité des porteurs de charge μ, v) la fréquence de coupure f_T, et vi) la fréquence maximum d'oscillation f_{max}. La physique des semiconducteurs ne sera pas détaillée ici, mais un rapide rappel des caractérisques statiques et hautes fréquences d'un transistor MOS est présenté sur la Fig. 2-a [40].

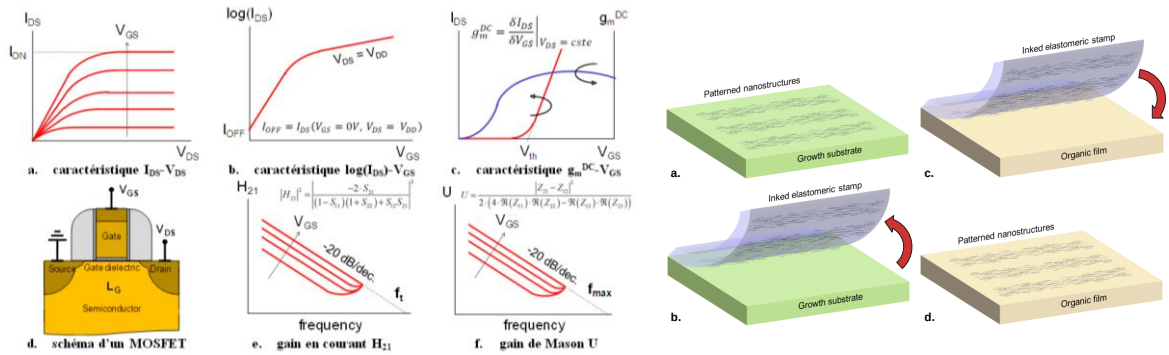


Fig. 23 – a. Rappel des paramètres géométriques, statiques et haute fréquences utilisés dans ce manuscrit, et b. Méthode de report par impression sèche de nanostructures depuis un substrat donneur (vert) vers un substrat accepteur (rose) via l'utilisation d'un tampon (bleu) [124]–[126].

Une première solution pour la réalisation de dispositifs électroniques flexibles est l'électronique organique et imprimée. Cependant, la faible mobilité des semiconducteurs organiques actuels [63]–[66] et les résolutions des techniques d'impression de l'ordre du micromètre [25], [44], [47], [54] limitent les composants issus de cette filière à des fréquences de l'ordre du MHz (voir Table A1.1 et Table A1.2, Annexe 1) [9], [59], [68], [69], [71]–[73].

Afin de dépasser ces limitations, l'association de semiconducteurs inorganiques et de techniques de fabrication issues de l'industrie du silicium avec un support organique souple a été envisagée. Une approche ascendante, proposant le report de nanostructures synthétisées chimiquement vers un film plastique a permis de dissocier les étapes de fabrication à haute température (sur un substrat de croissance) et d'assemblage à faible température (sur film organique). Dans cette optique, après synthèse et dispersion en solution des nanostructures, la réalisation à faible température de transistors à un nanofil a été démontrée, permettant d'obtenir des mobilités électroniques de l'ordre 10^3 $cm^2.V^{-1}.s^{-1}$ [77], [95]–[100]. Cependant ces transistors sont caractérisés par de faibles courants de drain (< 100 µA) [82], [92]–[101] et souvent placés aléatoirement, donc peu appropriés pour des applications circuits et sur de larges surfaces [77].

Des courants plus importants peuvent être obtenus grâce à l'utilisation de réseaux de nanofils [34], [35], [90]. Des transistors flexibles ont été réalisés après transfert de ces nanostructures sur film souple grâce à des méthodes en voie humides, d'impression jet d'encre ou de transfert par impression sèche (Fig. 2-b). Des fréquences de coupure f_T élevées ont ainsi été démontrées : f_T = 1,1 GHz grâce à l'utilisation de nanofils d'arsenic d'indium (InAs) [78], f_T=5GHz par impression jet d'encre de nanotubes de carbone (CNT) non ordonnés [11], f_T=8GHz en utilisant des CNT monofeuillets alignés [10], ou encore f_T=8,7GHz grâce à l'utilisation de graphène [133]. Les récents résultats obtenus grâce à cette méthode ascendante sont résumés en annexe (voir Table A1.3, Annexe 1).

Tableau 1 – Transistors flexibles performants

référence	f_T / f_{max} (GHz)		NF_{min} / G_a (dB)		matériau
[6,16]	**150**	**160**	**0.57**	**17.8**	**Si**
[168]	120	280	-	-	InGaAs
[7]	105	23	-	-	InAs
[8]	103	-	0.89	14.2	Si
[9]	48	-	1.1	12.0	Si
[10,11]	5	-	-	-	CNT
[12]	3.8	12	-	-	Si
[13]	2.0	7.8	-	-	Si
[14]	1.9	3.1	-	-	Si
[15]	1.6	-	-	-	GaAs

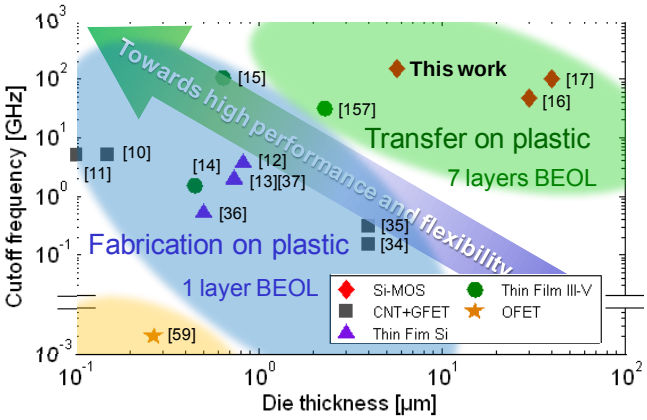


Fig. 3 – Evolution de l'électronique flexible rapide

En parallèle au développement de ces techniques, des méthodes descendantes (*top-down*) ont aussi été étudiées [12]–[14], [75], [134], [135]. En effet, les techniques conventionnelles de lithographie et gravure permettent un meilleur contrôle de l'uniformité des motifs désirés (taille, orientation cristaline, alignement) [75] et l'utilisation d'une méthode de transfert par impression sèche (Fig. 2-b) conserve un plus haut degré d'alignement après report que les méthodes en voie humide [75], [134], [136], [137].

Le report de films minces inorganiques est souvent réalisé en dissolvant une couche sacrificielle présente sous le film structuré à transférer. Des tranches SOI sont généralement utilisées à ces fins, mais une sous-gravure peut aussi être utilisée sur différents substrats. Le processus de transfert des structures relachées est ensuite effectué

par la méthode présentée Fig. 2-b. Le matériau le plus utilisé dans cette approche est le silicium, mais la réalisation de transistors flexibles à base de nanomembranes d'arsenic de galium (GaAs) ou d'indium (InAs) a aussi été démontrée [14], [15], [140], [143], même si ces matériaux peuvent s'avérer relativement coûteux, surtout dans l'optique d'applications sur de larges surfaces [13].

Une sélection des récents résultats obtenus grâce à cette méthode descendante est présentée en annexe (voir Table A1.4, Annexe 1, page 136). L'utilisation de nanofils de GaAs a ainsi permis d'atteindre une fréquence de coupure de 1.6GHz et des propriétés relativement stables en flexion [14], [140], [143]. Des transistors possédant des fréquences de coupure f_T de l'ordre de 2-4GHz et des fréquences maximales d'oscillation f_{max} allant jusqu'à 12GHz ont été réalisés à partir de films de silicium [12], [13], [37]. La meilleure performance démontrée grâce à cette approche est (à notre connaissance) f_T=105GHz mesurée sur un transistor flexible à base de nanofils d'InAs transférées par impression sèche (Fig. 2-b) [15].

Cependant, ces deux approches (ascendante et descendante) sont toutes les deux basées sur le transfert de nanostructures vers un film plastique sur lequel seront ensuite réalisées différentes étapes technologiques pour finaliser les transistors et circuits. Deux facteurs limitent alors les performances des transistors flexibles ainsi fabriqués : i) les propriétés thermiques (faible tenue en température et fort coefficient de dilatation thermique) des polymères utilisés comme substrat, et ii) la difficulté pour réaliser des réseaux d'interconnection complexes. En effet, même si certaines étapes de dopage et recuit d'activation peuvent être réalisées avant transfert [12]–[14], [36], [37], une simple étape de lithographie nécessite habituellement un recuit de la résine photosensible, pouvant entrainer des déformations thermiques et donc potentiellement un défaut d'aligment [12], [13], [37]. Par ailleurs, l'optimisation de la géométrie des transistors en vue d'applications hautes fréquences nécessite l'utilisation de plusieurs doigts de grille et donc de réseaux d'interconnection. Même si de nombreux efforts sont investis dans le domaine des interconnections flexibles (voire étirables) [148]–[154], aucune démonstration (à notre connaissance) d'empilement flexible comprenant une dizaine de niveaux métalliques (comme requis pour des applications circuits hautes fréquences) n'a été publiée.

Afin de s'affranchir de ces limitations, une dernière methode, en trois temps, à été envisagée, comprenant : i) la fabrication conventionnelle de transistors performants sur un substrat rigide, ii) l'amincissement de la face arrière de ce substrat initial jusqu'à ne laisser qu'une dizaine de micromètres d'épaisseur, et iii) le report et collage sur un film souple de ces dispositifs amincis [16], [17], [155]–[157]. La différentiation complète entre le substrat de fabrication (rigide) et final (flexible) permet de réaliser des composents rapides sans imposer de limites dues à un matériau organique. La faible épaisseur conservée après amincissement assure quant à elle la flexibilité mécanique des transistors et circuits.

Des transistors MOS des nœuds technologiques 180nm puis 130nm ont ainsi été amincis jusqu'à 30 µm d'épaisseur et transférés sur film plastique, démontrant des fréquences de coupure de 48GHz (59GHz en flexion) [16], [163]–[165] et 103GHz (118GHz en flexion) respectivement [17], [166], [167] et de très faibles niveaux de bruit : 1,1dB and 0,9dB et des gains associés de 12dB et 14dB respectivement (voir Table A1.5, Annexe 1).

Les travaux décrits dans ce document ont été réalisés en partenariat avec *STMicroelectronics*, dans le but de combiner le fort potentiel d'une technologie industrielle mature avec les nouvelles possibilités offertes par l'apport de flexibilité mécanique. La seconde partie de ce chapitre décrit la technologie SOI-CMOS 65nm utilisée dans ces travaux ainsi que les méthodes de caractérisation qui seront mises en œuvre.

1.2 Potentiel de la technologie SOI-RF CMOS 65nm

La technologie SOI (silicium sur isolant, ou *silicon-on-insulator*) se différencie de la technologie sur silicium massif par le fait qu'une couche de dioxyde de silicum (appelée BOX, pour *buried oxide*) est enterrée sous un film de silicium monocrystallin (Fig. 4-a). L'utilisation de tranches SOI pour la réalisation de transistors et circuits CMOS (Fig. 4-b-c) présente certains avantages par rapport à une technologie sur silicium massif. L'ajout d'une couche diélectrique fournit une résistance plus importante aux effets parasites, de meilleures performances (Fig. 4-d), une plus faible consommation (Fig. 4-d) et une densité d'intégration plus importante [42], [169], [170], [180]. De plus, comme exposé dans le chapitre suivant, la couche d'oxyde (BOX) pourra être utilisée comme couche d'arrêt lors de la gravure de la face arrière de la tranche SOI. Ces éléments font de la technologie SOI un très bon candidat pour l'utilisation dans le domaine de l'électronique flexible [170], [179].

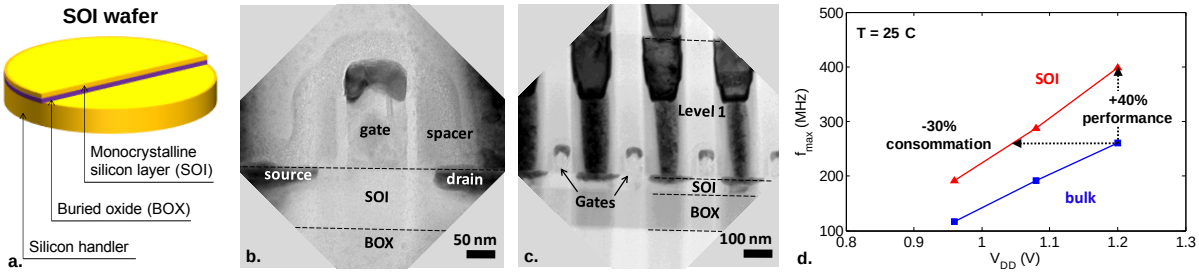


Fig. 4 – a. Schéma d'une tranche SOI *(silicon-on-insulator)*, b-c. Images de microscopie électronique en transmission montrant un transistor sur substrat SOI et le premier niveau de métallisation, et d. comparaison entre les technologies SOI et silicium massif pour un même nœud technologique.

La technologie mature SOI-CMOS 65nm de *STMicroelectronics* a donc été choisie pour ces travaux. Les transistors MOS issus de cette technologie sont en effet reconnus pour délivrer un niveau de performance compatible avec des applications hautes fréquences (HF), faible bruit et faible consommation [185].

La Fig. 5 présente les caractéristiques statiques et HF d'un transistor n-MOS possédant une longueur de grille L_G=60nm et un développement total W_T=64µm, provenant de l'association parallèle de doigts de grille de largeur unitaire W_u=1µm. Les caractéristiques courant-tension I-V et transconductance statique g_m^{DC} (Fig 5-a-b) démontrent une valeur maximale de g_m^{DC}=780mS/mm obtenue pour une tension de drain V_{DS}= 1.2V et de grille V_{GS}=0.8V, correspondant à un courant de drain I_{DS}=270mA/mm. Ce point de polarisation sera utilisé pour l'extraction des fréquences caractéristiques du transistor f_T et f_{max}. Les caractérisations HF présentées dans ce manuscrit sont basées sur le savoir-faire développé dans le laboratoire commun *IEMN-STMicroelectronics* au cours des dernières années [41], [42], [186], [191]. Afin d'obtenir les courbes Fig. 5-c et Fig. 5-d permettant l'extraction des fréquences f_T et f_{max}, différentes étapes de calibration sont requises.

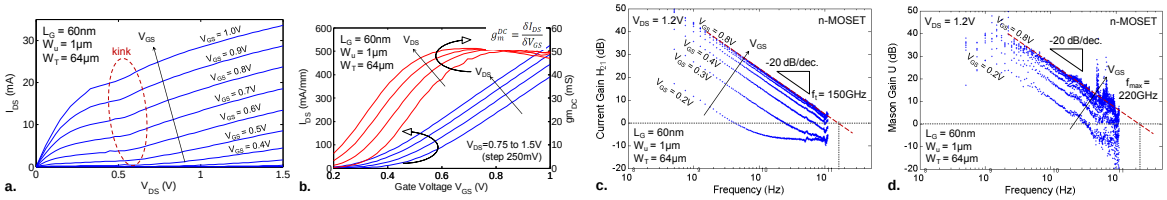


Fig. 5 – a. Caracteristique courant-tension I_{DS}-V_{DS}, b. courant de drain I_{DS} et transconductance statique g_m^{DC} en fonction de la tension de grille V_{GS}, c. gain en courant H_{21}, et d. gain de Mason U en fonction de la fréquence (pour une tension de grille variant de 200mV à 800mV)

Une première calibration dite *off-wafer*, réalisée sur un substrat de calibration permet de prendre en compte les termes d'erreur systématique (Fig. 6-a) dus à l'analyseur de réseau

et au montage expérimental (câbles, pointes HF, etc) [41], [190]. Dans l'ensemble des travaux présentés dans ce document, une méthode de calibration dite '*LRRM*' (*line-reflect-reflect-match*) est utilisée [194].

Une deuxième étape de calibration, appelée *on-wafer*, est faite sur la tranche de silicium sur laquelle ont été réalisés les transistors. Elle permet d'éplucher les contributions parasites des éléments du transistor HF [41]. En effet, l'impact sur les propriétés HF des différents niveaux de métallisation et vias requis pour connecter le transistor aux plots de contact présents en surface doit être pris en considération. Deux méthodes d'épluchage sont utilisées dans ces travaux : i) la méthode '*OPEN*' représentée schématiquement sur le Fig. 6-b et ne prenant en compte que les éléments parallèles des accès [195], et ii) la méthode '*POSS*' (*pad-open-short$_1$-short$_2$*), Fig. 6-c, plus complexe, mais permettant un meilleur épluchage des éléments parasites à hautes fréquences [190].

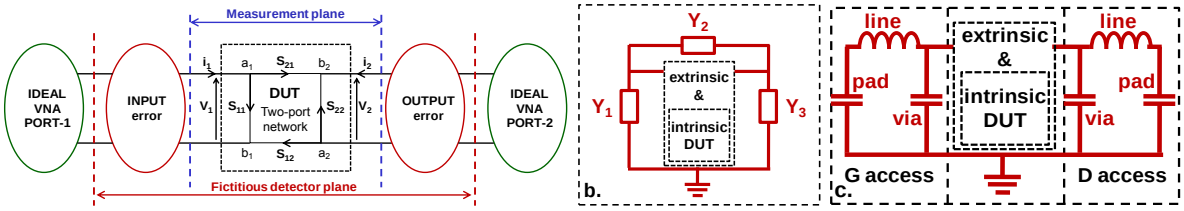


Fig. 6 – a. Schéma d'un banc de mesure HF, incluant le composant sous test (*DUT*), un analyseur de réseau idéal et des termes d'erreur [192], b. schéma électrique présentant la méthode d'épluchage '*OPEN*', et c. la méthode '*POSS*' (*Pad-Open-Short$_1$-Short$_2$*).

L'épluchage '*OPEN*' consiste à mesurer un circuit ouvert dédié possédant la même structure (plots de contact, lignes et vias d'accès) que le transistor sous test et à soustraire leurs paramètres impédances :

$$Y_{OPEN} = \begin{pmatrix} Y_1 + Y_2 & -Y_2 \\ -Y_2 & Y_2 + Y_3 \end{pmatrix} \qquad Y_{DUT} = Y_{TOT} - Y_{OPEN}$$

L'épluchage '*POSS*' requiert la mesure de quatre structures passives : i) un '*pad*' ne contenant que les plots de contact en aluminium, ii) deux structures comprenant les plots d'aluminium et des lignes d'accès, uniquement sur le dernier niveau de métallisation pour la première '*short$_1$*', et aussi les vias permettant d'atteindre le niveau du transistor pour la deuxième '*short$_2$*', et iii) une structure ouverte dédiée '*open*' comme pour la méthode précédente. Le calcul de l'épluchage est alors défini par les équations suivantes :

$$Z_{line} = \left(Y_{short1} - Y_{pad}\right)^{-1} + \frac{\left(Y_{short2} - Y_{pad}\right)^{-1} - \left(Y_{short1} - Y_{pad}\right)^{-1}}{3}$$

$$Y_{via} = \left[\left(Y_{open} - Y_{pad}\right)^{-1} - Z_{line}\right]^{-1}$$

$$Z_{DUT} = \left\{\left[\left(Y_{TOT} - Y_{pad}\right)^{-1} - Z_{line}\right]^{-1} - Y_{via}\right\}^{-1}$$

Une fois la calibration et l'épluchage effectués, les caractéristiques HF du transistor considéré peuvent être présentées en traçant les gain en courant H_{21} et de Mason U définis d'après les formules suivantes :

$$|H_{21}| = \frac{2\,S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[k\left|\frac{S_{21}}{S_{12}}\right| - \Re\left(\left|\frac{S_{21}}{S_{12}}\right|\right)\right]} \qquad \text{avec} \qquad k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|}$$

La fréquence de coupure f_T (respectivement la fréquence maximale d'oscillation f_{max}) est définie sur la Fig. 5-c (respectivement Fig. 5-d) comme la fréquence pour laquelle le gain

en courant H_{21} (respectivement le gain de Mason U) vaut 0 dB, si la pente expérimentale est en accord avec la valeur théorique de -20dB/dec. Ces figures démontrent des valeurs de fréquences caractéristiques f_T =150GHz et f_{max} =220GHz.

Après avoir mesuré les propriétés statiques et HF d'un transistor, les paramètres du circuit équivalent petit signal (*SSEC*) (Fig. 7-a) peuvent être extraits. Les hypothèses reliées à l'utilisation de ce modèle et les techniques d'extraction ne seront pas présentées ici [41], [42], [196]–[198]. Cependant, la bonne adéquation entre les paramètres S mesurés (bleu) et rétro-simulés (rouge) est démontré Fig. 7-b. De plus, le gain en courant H_{21} est présenté Fig. 7-c, l'erreur (vert) entre le gain mesuré et simulé valide aussi la pertinence du modèle.

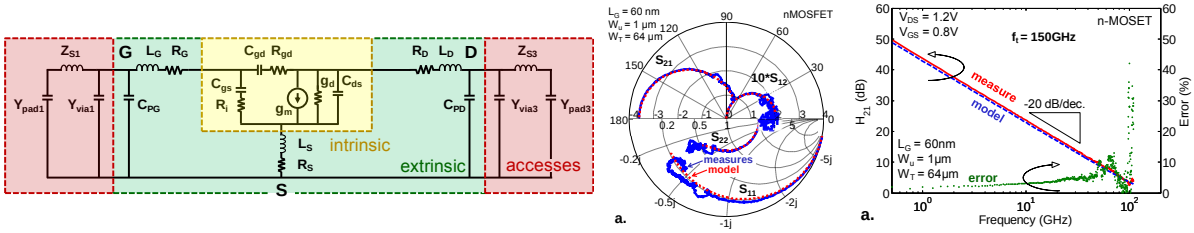


Fig. 7 – a. Circuit équivalent petit signal (*SSEC*), b. paramètres S mesurés et retro-simulés en utilisant le modèle SSEC, et c. gain en courant H_{21} mesuré, simulé et erreur.

La connaissance du circuit équivalent *SSEC* permet de mesurer les paramètres de bruit, grâce à la méthode F_{50} (non décrite dans ce résumé) [42], [199], [203]–[205]. Cette méthode a été utilisée pour extraire les quatre paramètres de bruit présentés sur la Fig. 8 : le facteur de bruit minimal NF_{min}, et le gain associé G_a, atteints pour une admittance optimale Γ_{opt} et la résistance équivalente de bruit R_n [41], [42], [191]. A 10GHz, les valeurs NF_{min}=0,56dB, G_a=18,2dB ont ainsi été démontrées (NF_{min}/G_a=1,10/14,5dB à 20GHz [205]). La résistance de bruit équivalente R_n définit la stabilité des paramètres de bruit autour de l'admittance optimale. A 10GHz, R_n=52,2 Ω (51,8Ω à 20GHz [205]).

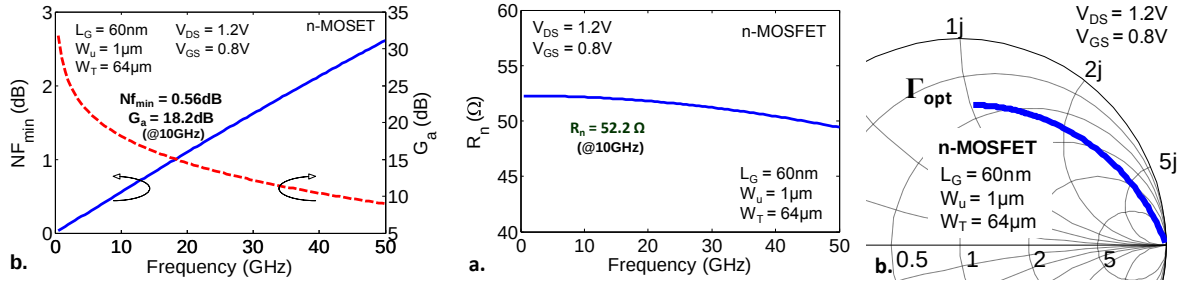


Fig. 8 – a. Facteur de bruit minimum NF_{min} et gain en puissance associé G_a, b. résistance de bruit équivalent R_n, et c. admittance optimale Γ_{opt} (ces paramètres ont été extrait à V_{DS}=1,2V, V_{GS}=0,8V).

Cette partie a démontré le potentiel de la technologie SOI-CMOS 65nm pour des applications en électronique flexible. Les caractéristiques présentées ci-dessus seront comparées dans le chapitre suivant avec les mesures effectuées sur des transistors flexibles.

Conclusion

Un intérêt grandissant est tourné actuellement vers l'apport de flexibilité mécanique à de nombreux dispositifs électroniques et un besoin urgent pour de plus hautes fréquences a été identifié. La réalisation d'une électronique flexible à partir de technologies matures semble présenter toutes les caractéristiques nécessaires pour relever ce défi. Le chapitre suivant présente la fabrication et la caractérisation de transistors et circuits flexibles afin de démontrer la possibilité de combiner hautes performances électriques et flexibilité mécanique.

Chapitre 2 : Fabrication et caractérisation

2.1 Méthodologie de fabrication

Ce second chapitre présente la méthodologie de fabrication développée dans ces travaux. Le matériau inital est une tranche SOI (rigide) fabriquée par *STMicroelectronics* (étape 1 de la Fig. 9-a) et comprenant le multicouche décrit sur la Fig. 9-b : i) 780µm de silicium massif, ii) 145nm d'oxyde enterré (BOX), iii) 60nm de silicium monocrystallin (SOI), puis iv) six niveaux d'interconnection (BEOL) réalisés par un empillement successif de couche de métal et de diélectrique, et enfin v) des plots de contact et une couche de passivation. Après avoir collé un support temporaire sur la face avant de la tranche SOI (afin de maintenir l'ensemble plat et rigide), une étape d'amincissement permet de supprimer le silicium massif de la face arrière, jusqu'à atteindre le BOX. Un film plastique est alors collé en face arrière, puis le support temporaire est retiré, permettant ainsi l'obtention d'une tranche SOI flexible issue d'une technologie CMOS mature.

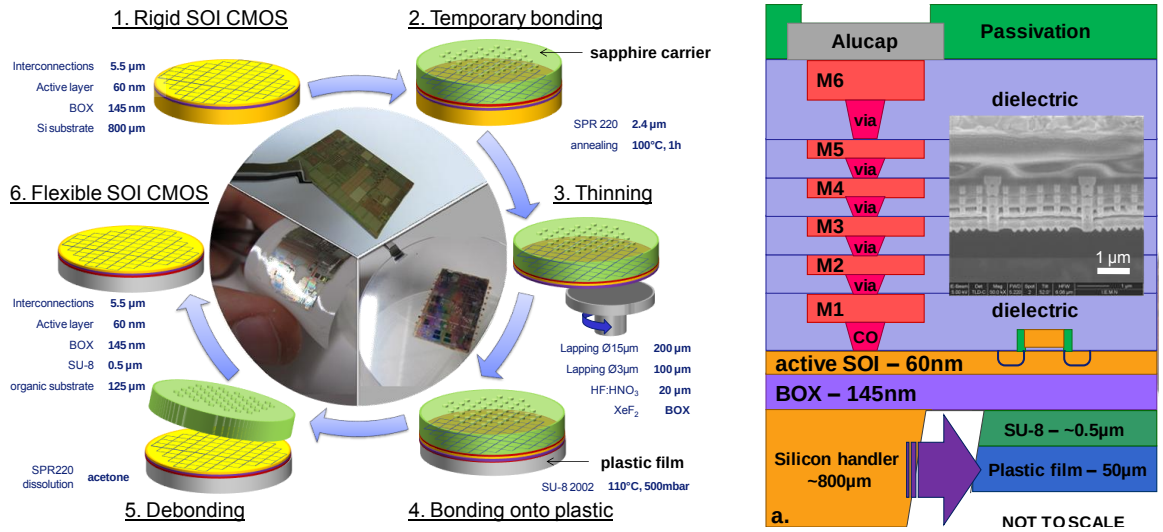


Fig. 9 – Schéma décrivant la méthode proposée dans ces travaux, et b. schéma présentant les différentes couches constituant les transistors et circuits MOS considérés.

Le processus d'amincissement développé dans ces travaux comporte trois étapes : i) un amincissement mécano-chimique rapide mais fragilisant l'échantillon : de 800µm à 100µm, ii) une gravure chimique en voie humide permettant de réduire les contraintes générées lors de la première étape : de 100µm à 20µm, et iii) une gravure sèche extrêmement sélective par rapport à l'oxyde de silicium pour nettoyer les derniers micromètres de silicium sans endommager le BOX. La Fig. 10-a présente un résumé de l'ensemble de cette procédure en présentant l'épaisseur d'un échantillon après les différentes étapes d'amincissement.

Avant de commencer le processus d'amincissement, un support mécanique est collé en face avant. Le collage temporaire (réalisé par une couche de résine optique SPR220 durcie) doit resister à l'ensemble des étapes d'amincissement, tout en permettant un décollement sélectif par rapport au collage permanent reliant l'échantillon aminci au film plastique. Afin d'améliorer cette dernière étape de décollement, le support utilisé lors de ces travaux est une tranche de saphir perforée de trous de 1mm de diamètre à l'emplacement de l'échantillon.

L'amincissement mécano-chimique génère des défauts de surface de faible rayon de courbure, produisant d'importantes concentrations de contrainte et donc réduisant la résistance mécanique de l'échantillon aminci [208]. Compléter ce processus d'amincissement par une étape de gravure isotrope permet d'agrandir le rayon de courbure des défauts de surface et d'améliorer la résistance mécanique de l'échantillon aminci [208]. Différentes techniques peuvent être utilisées pour cette étape de relaxation des contraintes. La méthodologie présentée dans ces travaux utilise une gravure humide.

Une solution d'acides hydrofluorydrique (HF) et nitrique (HNO_3), 1:9 v/v%, appelée HNA, permet d'amincir l'échantillon de 100µm à 20µm (Fig. 10-a) tout en relaxant les contraintes générées lors de l'étape précédente. Afin de ne pas attaquer le film SOI ou le multicouche d'interconnection, une cire de protection encapsulant l'échantillon CMOS est déposée avant l'attaque chimique. Cette cire couvre les flancs de l'échantillon sur une hauteur suffisante pour protéger les différentes couches. De plus, une couche de cire est déposée de l'autre côté du support temporaire, afin d'empêcher la solution acide d'attaquer la face avant de l'échantillon à travers les trous présents dans ce support de saphir. Une étape de nettoyage est ensuite nécessaire pour dissoudre la cire (sélectivement).

Enfin, la dernière étape de cette procédure d'amincissement est réalisée par une attaque sèche du silicium par du difluorure de xenon (XeF_2) en phase gazeuse. Cette technique présente l'avantage d'offrir une très bonne sélectivité entre le silicium et l'oxyde de silicium. Il est ainsi possible de graver les derniers micromètres de silicium sans endommager le BOX (de 145 nm d'épaisseur).

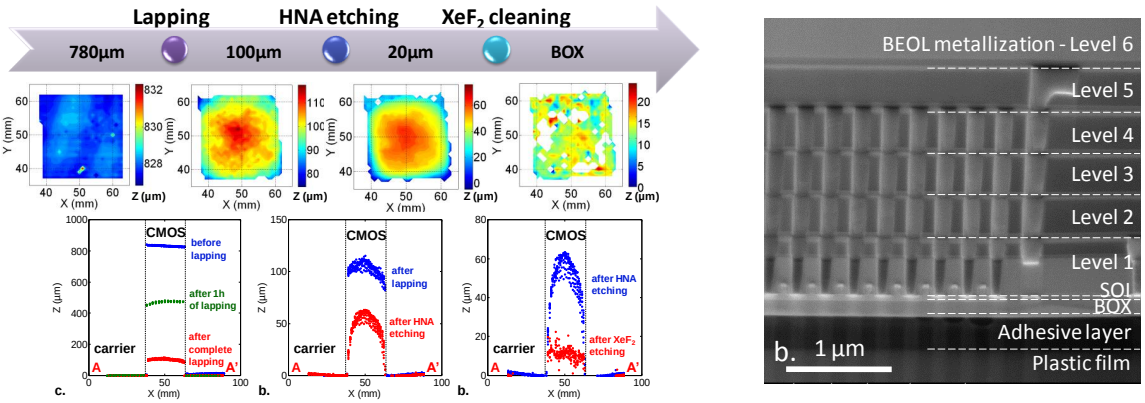


Fig. 10 – a. Résumé du processus d'amincissement et épaisseur de l'échantillon CMOS après les différentes étapes, et b. image de microscopie électronique en transmission d'un MOSFET flexible.

Une fois l'amincissement terminé, l'échantillon comprend alors le BOX, le SOI et les différents niveaux d'interconnexion (Fig. 10-b), soit une épaisseur totale de 5,6 µm. Ce film mince doit alors être tranféré du support temporaire vers un film plastique souple, soit en commençant par le coller sur un film plastique, soit en commençant par le séparer du support temporaire.

Une méthode de thermocompression (Fig. 11-a) d'une couche époxie a été développée pour assurer un collage permanent entre la face arrière de l'échantillon aminci et un film organique. La mise en contact est effectuée sous vide pour prévenir l'encapsulation de bulles d'air à l'interface, qui pourraient empêcher la bonne caractérisation des transistors transférés. Cette méthode permet ensuite de dissoudre la résine assurant le collage sur le support temporaire de manière sélective par rapport à la couche époxie (le solvent pouvant de plus passer à travers le support perforé pour attaquer la couche temporaire). Cependant, comme présenté sur la Fig. 11-a, cette méthode implique un budget thermique de 110 °C et une pression mécanique pour assurer un bon collage.

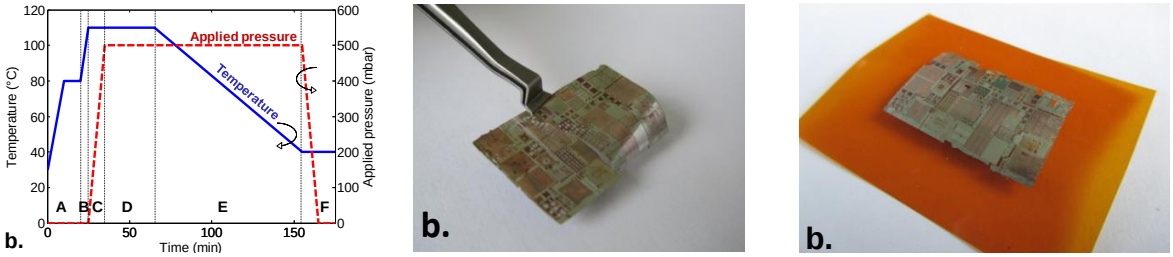
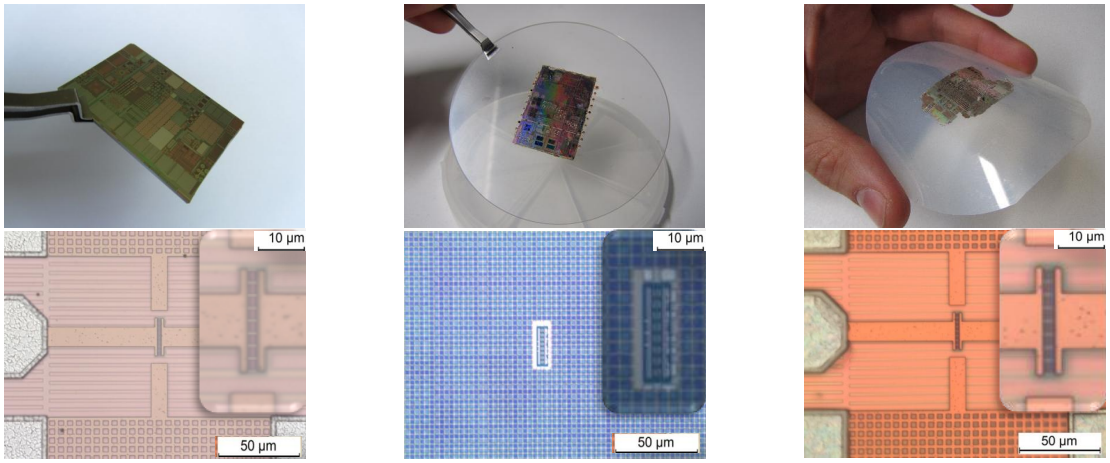


Fig. 11 – a. Paramètres expérimentaux de la thermocompression de l'échantillon aminci sur un film plastique, b. échantillon CMOS aminci à 5,6 µm d'épaisseur, et c. échantillon après transfert.

Par ailleurs, certaines applications peuvent nécessiter le collage de dispositifs électroniques souples sur des surfaces rigides non planes ou imposer de plus fortes restrictions thermiques. Une seconde méthode de transfert a donc été proposée, dans laquelle l'échantillon aminci est dans un premier temps libéré de son support temporaire et ensuite appliqué et collé à température ambiante sur un substrat final (pouvant être un film plastique, ou tout autre surface plane, courbe, ou flexible). La Fig. 11-b montre un échantillon aminci jusqu'à 5,6 µm puis libéré de son support temporaire. Les deux techniques permettent donc de transférer un échantillon aminci sur un film plastique (Fig. 11-c).

Les Fig. 12 et Fig. 13 démontrent qu'aucune dégradation visible (par microscopie optique ou électronique) des transistors amincis ne résulte de la méthodologie de transfert développée dans ces travaux. Les caractérisations électriques présentées dans la partie suivante permettront de conclure quant aux performances de ces dispositifs flexibles.



a. état initial (face avant) **b.** après amincissement (face arrière) **c.** après report (face avant)

Fig. 12 – Images à différents stades de la méthode d'amincissement et de transfert proposée

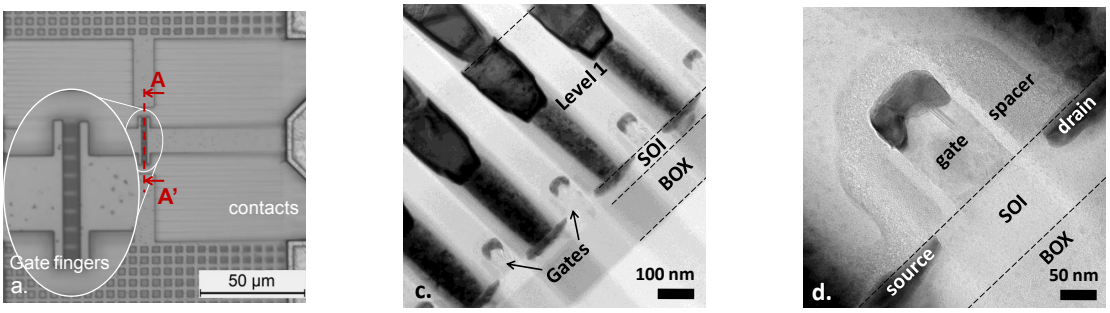
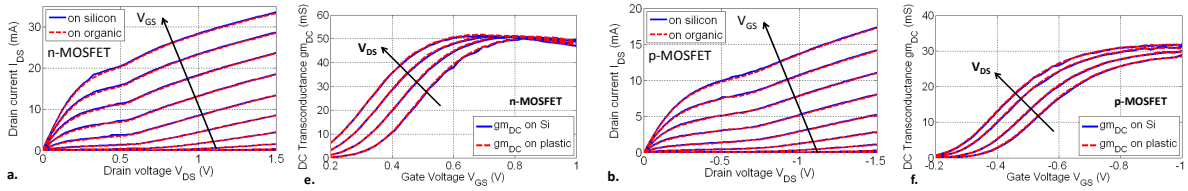


Fig. 13 – Analyse par microscopie électronique en transmission d'un échantillon aminci et reporté

2.2 Performances électriques des transistors MOS sur film souple

Cette deuxième partie s'intéresse aux performances électriques des dispositifs MOS presentés précédemment (*1.2 Potentiel de la technologie SOI-RF CMOS 65nm*) après report sur un film organique. Les mêmes techniques et équipements de mesure et d'analyse (épluchage, circuit équivalent petit signal) sont utilisés pour comparer les performances des transistors avant report (appelés *rigides* et représentés en bleu par défaut) et après report (appelés *flexibles* et représentés en rouge par défaut). Seuls les résultas et discussions seront donc présentés dans le résumé de cette partie.

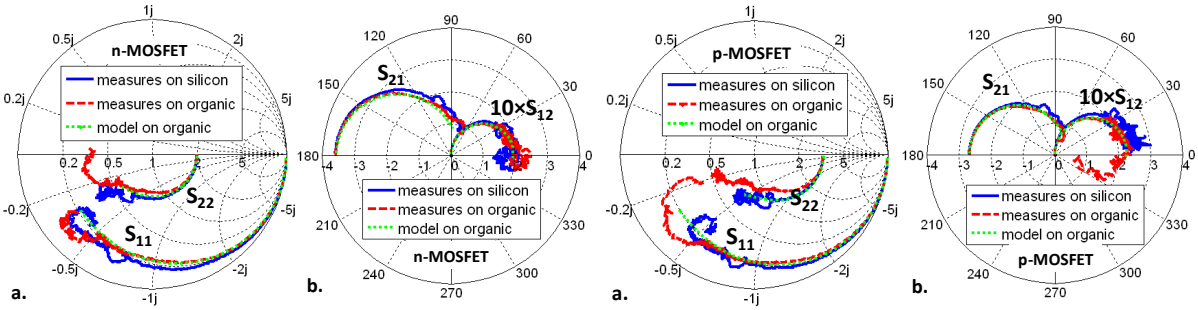
Les caractéristiques statiques des transistors n- et p-MOS présentés sur la Fig. 14 démontrent des comportements similaires en termes de courant et transconductance.



a. Transistor MOS de type n b. Transistor MOS de type p

Fig. 14 – Caractéristiques statiques de transistors MOS rigides (bleu) et flexibles, après report (rouge).

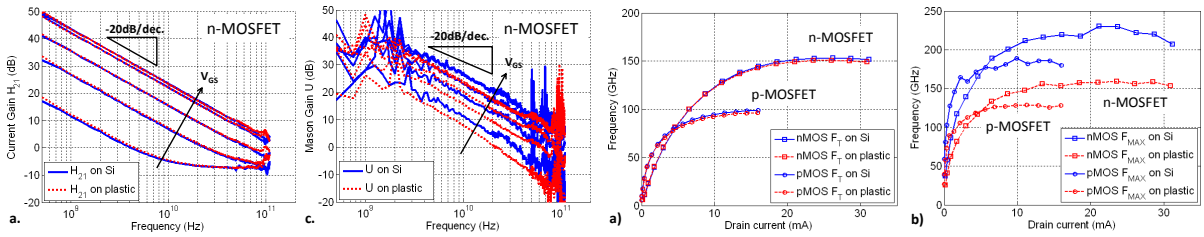
De la même manière que pour les transistors rigides, le point de polarisation permettant le maximum de transconductance statique est utilisé lors des mesures à hautes fréquences : V_{DS}=1,2V, V_{GS}=0,8V pour les transistors MOS de type n et V_{DS}=-1,5V, V_{GS}=-1,0V pour les transistors de type p. La mesure des paramètres S de 500MHz à 110GHz des transistors flexibles est présentée sur la Fig. 15 et comparée à la fois aux mesures réalisées sur les transistors rigides et aux valeurs simulées (SSEC) pour les transistors flexibles. Un comportement similaire entre les dispositifs rigide et flexible peut être noté, des différences entre les paramètres S n'apparaissant qu'à très hautes fréquences.



Transistor MOS de type n Transistor MOS de type p

Fig. 15 – Caractéristiques hautes fréquences de transistors MOS rigides (bleu) et après report (rouge).

Les gains en courant H_{21} (Fig. 16-a) et de Mason U (Fig. 16-b) supportent cette conclusion en démontrant des propriétés hyperfréquences similaires aux dispositifs rigides : i) très proches pour le gain en courant H_{21} et ii) légérement plus faibles pour le gain de Mason U. Ces deux graphiques montrent de plus une pente à -20 dB/dec. en accord avec la théorie et permettant une extraction fiable des fréquences caractéristiques. Les fréquences de coupure f_T (Fig. 16-c) avant et après report sont en accord parfait, sur une large plage de polarisation de grille V_{GS} (ou courant de drain I_{DS}), pour les transistors de type n et p. Seule la fréquence f_{max} (Fig. 16-d) présente une valeur légérement plus faible (~25%) après report. Ces mesures ont été validés sur un ensemble minimal de quatre transistors possédant des géométries proches mais différentes (longueur de grille L_G de 60nm ou 65nm, largeur unitaire W_u de 1µm ou 2µm, et développement total W_T constant, de 64µm).



Transistor MOS de type n f_T f_{max}

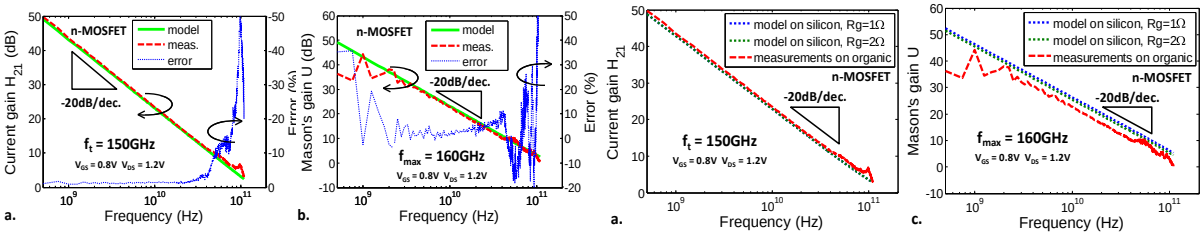
Fig. 16 – Caractéristiques hyper fréquences de transistors MOS rigides (bleu) et après report (rouge).

Afin de compléter les caractérisations hyperfréquences et de tenter d'apporter une explication à la diminution de f_{max}, les paramètres du circuit équivalent petit signal (SSEC) des transistors flexibles ont été extraits en utilisant le même modèle que précédemment. Les valeurs présentées dans le tableau 2 montrent une bonne adéquation entre les paramètres des transistors rigides et flexibles. La validité du modèle proposé dans ce tableau pour le transistor flexible est confirmée Fig. 17-a et Fig. 17-b en démontrant une très bonne rétrosimulation des gains H_{21} et U.

Tableau 2 – Paramètres du circuit equivalent petit signal, à V_{DS}=1,2V, V_{GS}=0,8V et I_{DS}=270mA/mm pour les transistors n-MOS et V_{DS}=-1,5V, V_{GS}=-1,0V et I_{DS}=-263mA/mm pour les transistors de type p.

		Extrinèques					*Intrinsèques*				
		C_{pg}	C_{pd}	R_g	R_d	R_s	g_m	g_d	C_{gs}	C_{gd}	C_{ds}
		fF	fF	Ω.mm	Ω.mm	Ω.mm	mS/mm	mS/mm	fF/mm	fF/mm	fF/mm
n-MOS	rigide	2.0	8.0	64	64	12.8	859	160	625	297	16
	flexible	1.6	7.5	128	128	6.4	859	160	578	297	16
p-MOS	rigide	2.5	6.0	64	6.4	6.4	559	99	578	265	16
	flexible	2.3	6.3	128	6.4	6.4	553	99	625	265	16

Cependant, il est intéressant de noter l'augmentation de la résistance de grille après report, qui peut expliquer la diminution de la fréquence maximale d'oscillation f_{max} sans avoir d'impact sur la fréquence de coupure f_T. Les Fig. 17-c et Fig. 17-d comparent les mesures réalisées après report (rouge) avec le modèle avant report (bleu) et ce même modèle avec une résistance de grille plus élevée (vert). Ceci confirme que cette augmentation de résistance de grille n'a pas d'impact sur le gain H_{21} (et donc f_T) et explique une partie de la diminution du gain U (et donc f_{max}).



Transistor MOS de type n f_T f_{max}

Fig. 17 – Comparaison des mesures (rouge) réalisées après report avec les modèles extraits après report (gauche) et avant report (droite).

Dans le but annoncé de démontrer la faisabilité d'une électronique souple hautes fréquences et faible bruit, il est nécessaire de caractériser les paramètres de bruit des dispositifs après report. En utilisant la même méthode qu'au chapitre précédent, les quatre paramètres de bruit des transistors flexibles peuvent être comparés avec ceux obtenus avant report (Fig. 18 et Fig. 19). Ces courbes démontrent bien que la méthodologie d'amincissement et de transfert proposée dans ces travaux permet de conserver tout le potentiel de la technologie électronique utilisée. La réalisation de composants flexibles à faible niveau de bruit est ainsi rendue possible.

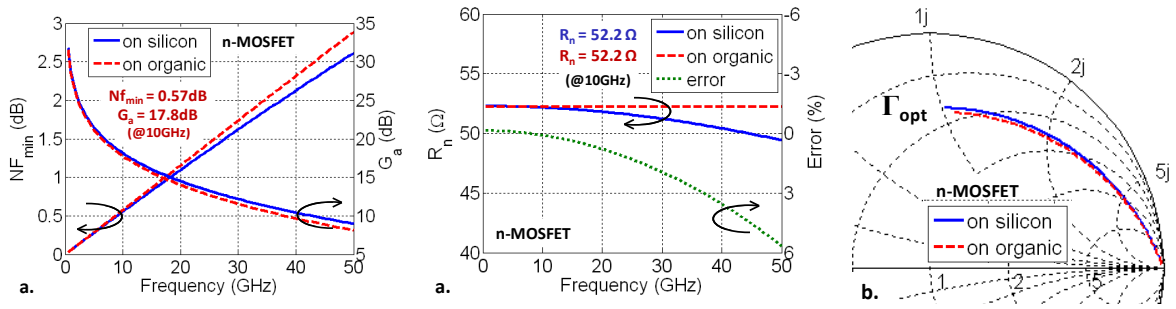


Fig. 18 – a. Facteur de bruit minimum NF_{min} et gain en puissance associé G_a, b. résistance de bruit équivalent R_n, et c. admittance optimale Γ_{opt} (ces paramètres ont été extrait à V_{DS}=1,2V, V_{GS}=0,8V).

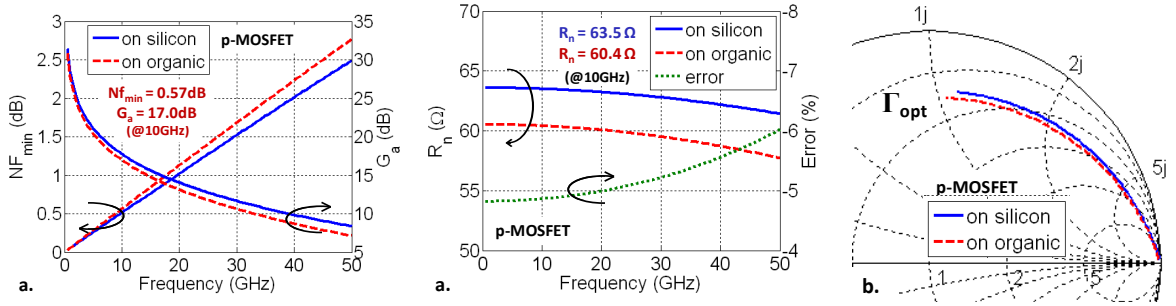


Fig. 19 – a. Facteur de bruit minimum NF_{min} et gain en puissance associé G_a, b. résistance de bruit équivalent R_n, et c. admittance optimale Γ_{opt} (ces paramètres ont été extrait à V_{DS}=-1,5V, V_{GS}=-1,0V).

Cette partie a comparé les performances électriques de transistors MOS issus d'une technologie SOI 65nm avant et après report sur un film plastique. Il est intéressant de noter que les performances statiques, hyperfréquences et en bruit de ces dispositifs ont été conservées même après amincissement jusqu'à la couche d'oxyde enterré et collage sur un film souple. Seule la fréquence maximale d'oscillation semble avoir été légèrement dégradée suite à ce report.

Les performances démontrées dans ces travaux dépassent (à notre connaissance) les meilleures caractéristiques présentées actuellement pour des transistors souples (voir Tableau 1), à la fois en termes de fréquences caractéristiques et de niveaux de bruit. De plus, le fait que la technologie reportée sur film organique possède différents niveaux d'interconnection permet de considérer le report de circuits complexes, sans nécessiter d'étape coûteuse de design spécifique. Ces considérations sont supportées par la caractérisation sommaire de lignes de propagation et amplificateurs faible bruit (non présentés ici).

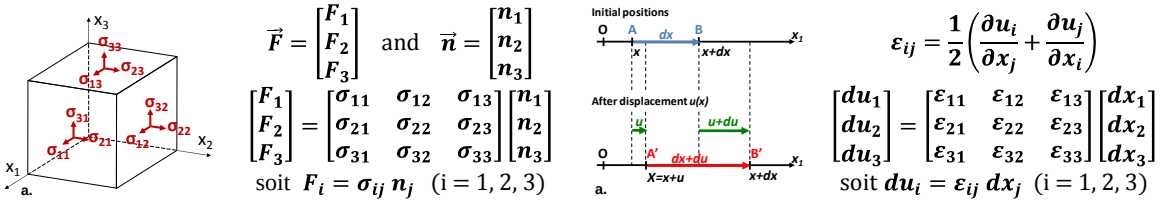
Conclusion

Ce second chapitre a proposé une méthode de fabrication de dispositifs flexibles à partir d'une technologie mature initialement réalisée sur substrat rigide. Ce processus est basé sur l'amincissement de la face arrière de la tranche SOI en trois étapes, puis du report du multicouche résultant (d'épaisseur micrométrique) vers un film organique souple. Ceci permet la réalisation de transistors et circuits performants : présentant les caractéristiques nécessaires pour développer une électronique souple, hautes fréquences, faible bruit et faible consommation. La seconde partie de ce chapitre a détaillé les caractéristiques électriques des transistors après report, démontrant des fréquences f_T/f_{max} de 150/160GHz (110/130GHz pour les transistors de type p), et des paramètres de bruit NF_{min}/G_a de 0.57/17.8dB (0.57/17.0dB pour les transistors de type p), à 10GHz. Ces performances définissent un nouveau standard pour l'électronique souple.

Chapitre 3 : Flexion des dispositifs souples

3.1 Considérations mécaniques

Ce troisième et dernier chapitre se penche sur les aspects mécaniques de ces travaux en tentant de répondre à la question : quel sera l'impact de contraintes mécaniques extérieures sur les propriétés électriques des dispositifs et circuits considérés ? Il faut de plus noter que dans l'optique d'applications commerciales, les contraintes peuvent être aléatoires et leur impact doit, autant que possible, être minimisé. Il a été envisagé dans un premier temps de ne traiter que les problèmes de flexion pour modéliser ces contraintes. Afin de prendre en compte le cas le plus défavorable, une contrainte engendrant une tension dans la direction du courant sera considérée. Les différents concepts de mécanique et de piezorésistivité utilisés ne seront pas rappelés dans ce résumé. La Fig. 20 présente simplement les tenseurs de contraintes σ et de déformation ε [243]–[245].



$$\vec{F} = \begin{bmatrix} F_1 \\ F_2 \\ F_3 \end{bmatrix} \text{ and } \vec{n} = \begin{bmatrix} n_1 \\ n_2 \\ n_3 \end{bmatrix}$$

$$\begin{bmatrix} F_1 \\ F_2 \\ F_3 \end{bmatrix} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix} \begin{bmatrix} n_1 \\ n_2 \\ n_3 \end{bmatrix}$$

soit $F_i = \sigma_{ij}\, n_j$ (i = 1, 2, 3)

$$\varepsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right)$$

$$\begin{bmatrix} du_1 \\ du_2 \\ du_3 \end{bmatrix} = \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon_{33} \end{bmatrix} \begin{bmatrix} dx_1 \\ dx_2 \\ dx_3 \end{bmatrix}$$

soit $du_i = \varepsilon_{ij}\, dx_j$ (i = 1, 2, 3)

Fig. 20 – a. Représentation et définition du tenseur des contraintes σ, et b. des déformations ε.

Il est ensuite important de signaler l'anisotropie des paramètres mécaniques du silicium : modules d'Young E et coefficient de poisson ν (définissant les relations entre déformations et contraintes), et donc aussi des couples de coefficients équivalents, comme les coefficients de Lamé μ et λ (définis ci-dessous) [243]–[245]. De même, les paramètres de piezoresistivité π du silicium sont fortement dépendants de l'orientation crystallographique considérée. Ces derniers paramètres, dont les valeurs considérées sont définies ci-dessous, relient les contraintes dans le silicium avec la variation de mobilité des porteurs de charge.

$$\lambda = \frac{\nu E}{(1+\nu)(1-2\nu)}$$

$$\mu = \frac{E}{2(1+\nu)}$$

Coefficients de Lamé

$$\pi_{11} = -84.0 \times 10^{-11}\ \text{Pa}^{-1}$$

$$\pi_{12} = 34.0 \times 10^{-11}\ \text{Pa}^{-1}$$

$$\pi_{44} = -17.0 \times 10^{-11}\ \text{Pa}^{-1}$$

Coefficients piezoresistifs, Si_{100}

$$\pi_L = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44})$$

$$\pi_T = \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44})$$

$$\pi_\perp = \pi_{12}$$

Coefficients piezoresistifs, Si_{110}

Afin de modéliser le multicouche CMOS complexe utilisé dans ces travaux, un empilement de 17 couches uniformes a été utilisé, comprenant le film plastique, une couche adhésive, l'oxyde enterré, le film de silicium SOI, et les différents niveaux d'interconnection (alternance de couches de cuivre et d'oxyde de silicium). Le paramètre principal influant sur la valeur des contraintes générées dans la couche de silicium SOI est la position du plan neutre (défini comme le plan sur lequel la flexion n'engendre ni contraintes de tension ni de compression, Fig. 21-a). La position de ce plan neutre est déterminée par les épaisseurs et modules d'Young des différentes couches considérées (Fig. 21-b). Il a été montré par calcul qu'une épaisseur de 50μm de film organique permet, dans le cas considéré, de positionner ce plan neutre à faible distance (~3μm) de la couche de silicium dans laquelle à lieu le transport électronique (Fig. 21-c) [151], [241], [258]. La valeur des contraintes étant proportionnelles à la distance au plan neutre, minimiser cette distance permet de minimiser les contraintes générées dans le film SOI.

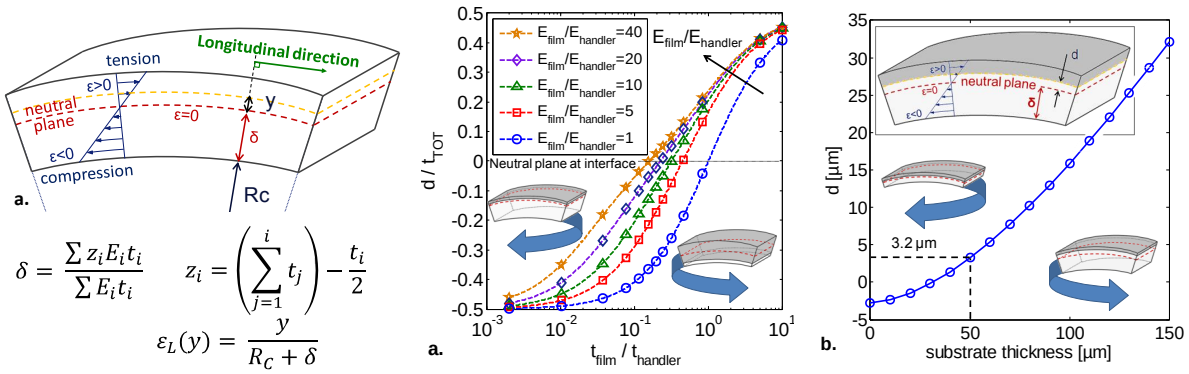
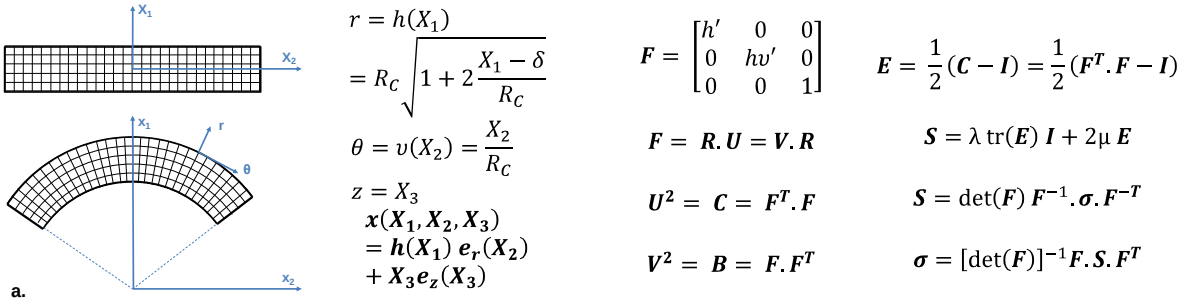


Fig. 21 – a. Schéma d'un matériau soumis à une flexion cylindrique, b. position du plan neutre en fonction des épaisseurs et modules d'Young dans un bicouche, et c. position du plan neutre des dispositifs MOS considérés en fonction de l'épaisseur du film plastique.

Les contraintes générées par la mise en flexion de l'échantillon CMOS souple ont été simulées en se basant sur la théorie des déformations finies [250]–[253]. Le formalisme complet ne sera pas détaillé dans ce résumé, mais la Fig. 22 résume succintement les principales équations intervenant dans le modèle mécanique utilisé dans ces travaux.



Description géométrique de la flexion cylindrique | Transformation | Déformations, contraintes

Fig. 22 – a. Représentation de la déformation générée par la flexion cylindrique et équations correspondantes [250]–[253].

L'impact des déformations sur les propriétés électriques est ensuite estimé via la variation de mobilité dûe aux coefficients piezorésistifs du silicium, en faisant l'hypothèse que les figures de mérite statiques (courant de drain I_{DS}, et transconductance statique g_m^{DC}) et hyperfréquences (fréquence de coupure f_T et fréquence maximale d'oscillation f_{max}) considérées sont proportionnelles à la mobilité des porteurs majoritaires. La Fig. 23 détaille les valeurs simulées des déformations et des contraintes dans les trois directions de l'espace après mise en flexion sur un cylindre de rayon de courbure 12,5mm. Ces composentes des déformations et contraintes sont, pour des raisons de symétrie, uniquement tracées en fonction de l'épaisseur de l'échantillon flexible déformé.

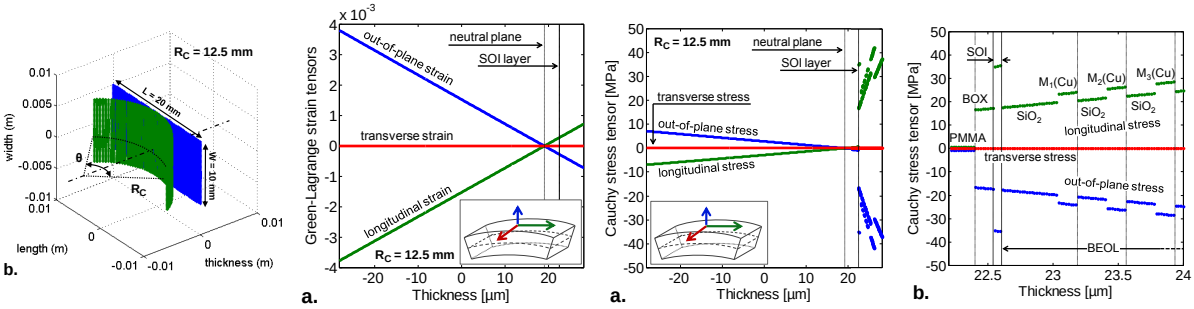


Fig. 23 – a. Représentation de l'échantillon avant (bleu) et après (vert) flexion, b. déformations, c. contraintes et d. zoom sur les contraintes dans le film SOI (pour un rayon de courbure de 12,5mm).

La Fig. 23 démontre que l'utilisation d'une épaisseur optimale de film souple permet de réduire la valeur des déformations et contraintes longitudinales dans le film SOI respectivement à 0,03% et 36MPa pour un rayon de courbure de 12,5mm. Le zoom présenté sur la Fig. 23-d montre de plus que les contraintes dans les différentes couches de métallisation restent du même ordre de grandeur.

La validité de cette méthode d'ingénierie du plan neutre est aussi supportée par la Fig. 24 présentant les contraintes et variations de mobilité longitudinale en fonction du rayon de courbure pour différentes épaisseurs du film plastique. Il est intéressant de noter qu'une épaisseur trop importante résulte en de larges contraintes et donc des variations de mobilité importantes. Ces variations se traduisent alors directement en variation de courant de drain, transconductance statique, et fréquences caractéristiques f_T et f_{max}, ce qu'il est souhaitable de limiter. A l'inverse, une épaisseur trop faible (voire nulle) du film plastique entraine des contraintes de compression lors de la mise en flexion de l'échantillon aminci. Ces contraintes ne sont pas non plus souhaitées. Une épaisseur de 50µm du film organique permet ainsi de limiter la valeur des déformations, contraintes et variations des propriétés électriques à un niveau acceptable. Cette méthode d'ingénierie du plan neutre permet donc (d'après le modèle considéré dans cette partie) aux dispositifs et circuits électriques souples de supporter d'importants niveaux de courbure tout en gardant des propriétés électriques relativement stables.

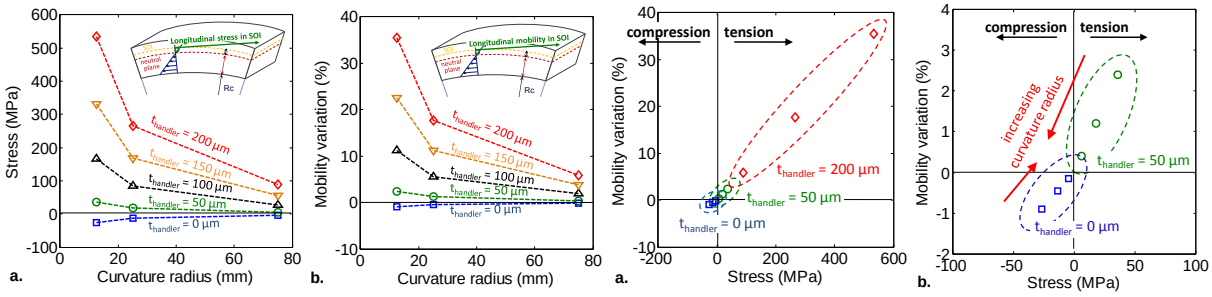


Fig. 24 – a. Contraintes longitudinales, et b. variations de mobilité longitudinale en fonction du rayon de courbure pour différentes épaisseurs de film plastique, c. et d. variations de mobilité en fonction de la contrainte pour différentes épaisseurs.

La validité du modèle proposé dans cette partie sera démontrée dans la dernière partie de ce manuscrit. En effet, les variations estimées des propriétés électriques seront comparées avec les mêmes valeurs mesurées sur des échantillons déformés.

3.2 Performances des transistors MOS déformés

Le second chapitre de ce document a présenté les caractéristiques des transistors MOS amincis et transférés sur un support souple. Cependant, toutes les mesures ont été réalisées sur des échantillons à plat, non déformés. La méthode d'ingénierie du plan neutre proposée dans la permière partie de ce chapitre suggère l'utilisation d'un film souple de polyimide de 50µm d'épaisseur. Après avoir reporté des composants sur un tel film plastique, cette deuxième partie s'intéresse à confronter des mesures électriques pour différents niveaux de déformation (différents rayons de courbure) avec les estimations simulées précédemment.

La Fig. 25 présente les échantillons considérés dans cette étude sur différents rayons de courbure : de 75mm jusqu'à 12,5mm. Il est important de noter que les échantillons sont placés sur le cylindre de telle sorte que la direction principale des contraintes corresponde à la direction du transport électronique. Ceci afin de se placer dans le cas le plus défavorable, c'est-à-dire pour lequel un rayon de courbure donné devrait engendrer les plus grandes variations des propriétés électriques. Ces mesures pourront ainsi permettre de valider la méthodologie d'ingénierie du plan neutre proposée. Enfin toutes les mesures ont été réalisées sur un ensemble de quatre transistors de géométries proches, mais différentes (longueur de grille L_G de 60nm ou 65nm, largeur unitaire W_u de 1µm ou 2µm, et développement total W_T constant, de 64µm).

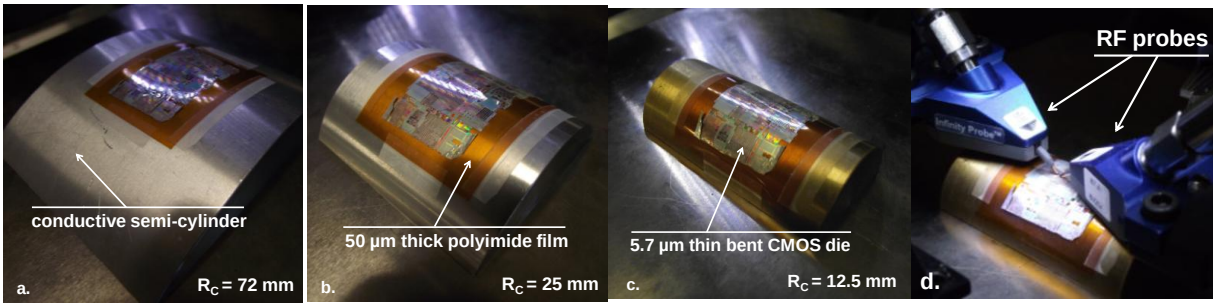
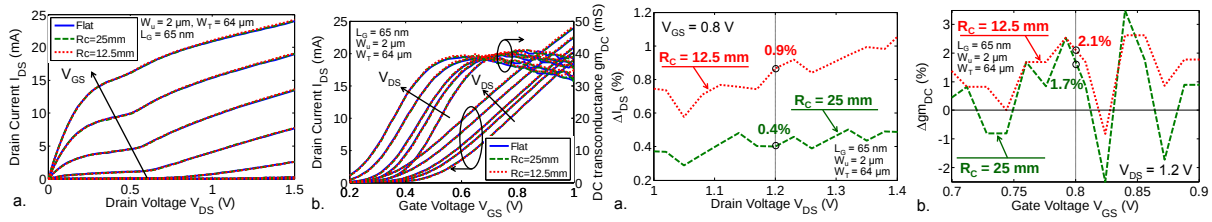


Fig. 25 – Cylindres utilisés pour réaliser les mesures sur des échantillons déformés.

Les caractéristiques statiques des transistors à plat et après conformation sur un cylindre de rayon de courbure R_C=25mm puis un second de rayon R_C=12,5mm sont présentées sur la Fig. 26. Les caractéristiques courant-tension ainsi que la transconductance statique tracée en fonction de la tension de grille (Fig. 26-a) démontrent des propriétés très similaires, et donc relativement insensibles à la flexion. Ceci est validé sur la Fig. 26-b présentant les variations relatives du courant de drain et de la transconductance statique après déformation sur les deux cylindres : ces variations sont limitées à quelques pourcents. Les valeurs mises en évidence correspondent aux valeurs de polarisation utilisées pour l'extraction des figures de mérite hyperfréquences.



a. Caractéristiques statiques b. Variations de ces propriétés

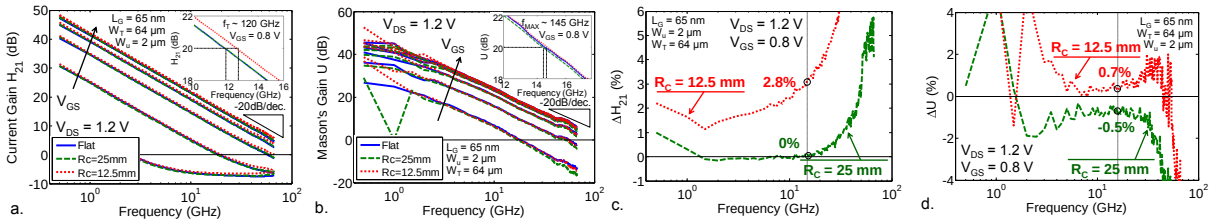
Fig. 26 – Caractéristiques statiques pour différentes configurations : à plat (bleu), et sur un cylindre de rayon de courbure R_C=25 mm (vert), puis 12,5mm (rouge).

Les caractéristiques hyperfréquences des transistors déformés ont aussi été analysées. Afin de ne pas engendrer d'erreurs supplémentaires dûes à un nombre important de posé de pointes RF sur les surfaces courbes, une méthodologie d'épluchage '*OPEN*' a été préférée à la méthode '*POSS*' utilisée dans le second chapitre. En effet une seule structure passive est alors nécessaire pour retirer les effets parasites des accès au transistor. Le manque de précision à haute fréquence de cette méthode d'épluchage par rapport à la méthode '*POSS*' n'est pas critique dans ce chapitre puisque seules les variations relatives des performances sont comparées.

Les gains en courant H_{21} et de Mason U sont présentés sur la Fig. 27-a pour les trois configurations précédentes : à plat, R_C=25mm et R_C=12,5mm. Il est important de noter premièrement que ces courbes suivent la pente théorique de -20dB/dec. permettant d'extraire de façon fiable les fréquences caractéristiques f_T et f_{max}. De plus, de façon similaire aux performances statiques, très peu de différence semble visible entre les différents niveaux de contrainte.

Cette constatation est à nouveau appuyée par la Fig. 27-b présentant les variations relatives des gains H_{21} et U pour les deux rayons de courbure considérés. Sur ces deux derniers graphiques, une fréquence égale à un dixième de la fréquence caractérisée par le gain considéré a été mise en évidence. La bonne corrélation entre la pente mesurée et la valeur théorique permet de conclure que toute variation sur cette fréquence représentera directement une variation sur la fréquence caractéristique considérée : f_T ou f_{max}.

Il est ainsi possible de conclure que la conformation des échantillons sur les deux cylindres considérés entraine une variation des propriétés hyperfréquences de l'ordre de quelques pourcents seulement.



a. Caractéristiques hyperfréquences b. Variations de ces propriétés

Fig. 27 – Caractéristiques hyperfréquences pour différentes configurations : à plat (bleu), et sur un cylindre de rayon de courbure R_C=25 mm (vert), puis 12,5mm (rouge).

Ces constatations sur les caractéristiques statiques et hyperfréquences valident le fait que la méthode d'ingénierie de plan neutre présentée dans la partie précédente et mise en œuvre dans cette dernière partie permet de réduire à un niveau acceptable les variations de propriétés électriques. Les Fig. 28 et Fig. 29 démontrent ce dernier point en présentant sur un même graphique les variations électriques simulées et mesurées sur les quatre transistors considérés. Cette comparaison est présentée dans un premier temps sur la Fig. 28 en regroupant les différentes figures de mérite, pour chaque transistor (c'est-à-dire chaque géométrie) considérée séparemment. Ensuite, la Fig. 29 représente ces mêmes variations pour chaque propriété prise indépendament, toutes géométries confondues.

Une bonne corrélation entre les mesures et les valeurs simulées est visible. Ceci confirme qu'il est possible d'associer de larges déformations avec une stabilité des caractéristiques électriques telle qu'un rayon de courbure de 12,5mm n'engendre que 5% de variation.

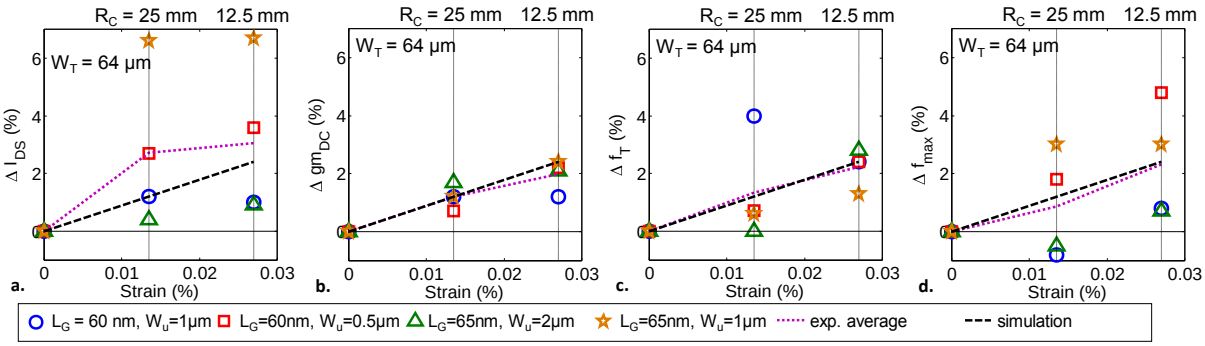


Fig. 28 – Comparaison des variations de propriétés électriques simulées et mesurées (par géométrie).

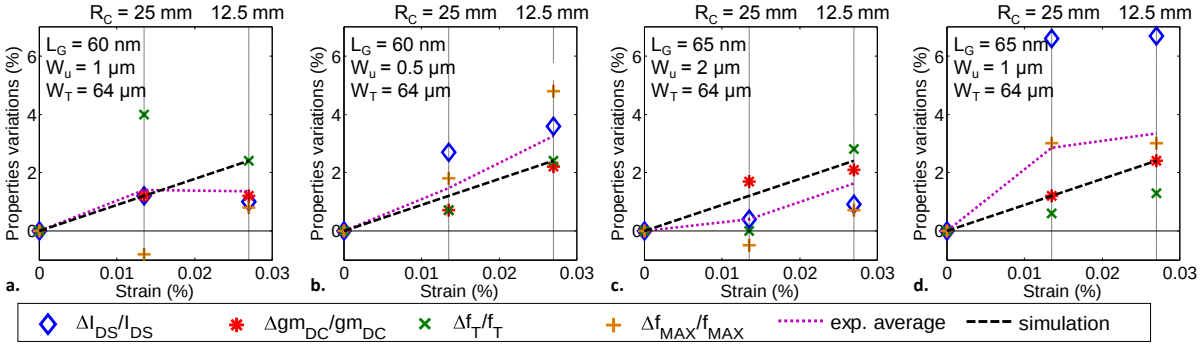


Fig. 29 – Comparaison des variations de propriétés électriques simulées et mesurées (par propriété).

Enfin, ce chapitre sera conclu par une comparaison de ces travaux avec les différentes publications récentes du domaine. La Fig. 30 résume ainsi les fréquences de coupure atteintes avec différentes techniques de fabrication ou report en fonction du rayon de courbure minimal démontré, pour lequel ces propriétés restent stables (moins de 10% de variation). Il est cependant important de noter que les technologies présentées sur cette figure ne comportent généralement qu'un seul niveau de métalisation. Le report de technologie permettant la réalisation de circuits complexes et stable en flexion représente donc une avancée non négligeable.

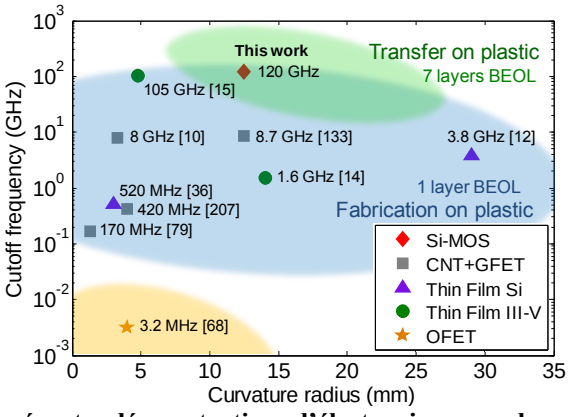


Fig. 30 – Comparaison des récentes démonstrations d'électronique souple.

Conclusion

Ce dernier chapitre a introduit les notions de mécanique permettant de proposer une méthode basée sur l'ingénierie de plan neutre pour minimiser l'impact des déformations sur les propriétés électriques. Cette méthode a été validée par un ensemble de mesure, démontrant des propriétés statiques et hyperfréquences stables même après avoir conformé l'échantillon CMOS souple sur un rayon de courbure de l'ordre du centimètre.

Conclusion générale

Ces travaux de thèse ont été réalisés dans le cadre du laboratoire commun *IEMN-STMicroelectronics* afin d'investiguer les possibilités de coupler une technologie commerciale mature avec des applications dans le domaine émergent de l'électronique souple. L'objectif était de démontrer la faisabilité technologique d'une électronique associant à la fois une grande flexibilité mécanique, de hautes performances électriques et enfin une bonne stabilité de ces performances sous déformation.

Le potentiel grandissant du domaine de l'électronique souple, ainsi que le besoin urgent pour de plus hautes performances a été présenté dans le premier chapitre de ce document. En réponse à ce besoin, de nombreuses technologies ont vu le jour ces dernières années. Certaines sont issues du domaine de l'électronique organique et imprimé, permettant de faibles coûts de production et de larges surfaces. D'autres sont plus proches des technologies de l'industrie du silicium, permettant des résolutions décananométriques et de meilleurs mobilités électroniques. Afin d'atteindre des niveaux de performance comparables aux technologies conventionnelles, il a été suggéré de reporter des composants et circuits d'une technologie mature vers un film souple. Dans cette optique, la technologie SOI-CMOS 65nm réalisée par *STMicroelectronics* a été présentée, ainsi que les méthodes de mesures utilisées.

Afin de répondre à ce besoin de coupler flexibilité mécanique et hautes performances électroniques, une méthodologie de report a été développée lors de ces travaux. La flexibilité provient du fait que la face arrière des tranches SOI est amincie successivement par différentes méthodes, résultant en un film de 5,6µm d'épaisseur qui est alors transféré sur un film plastique. La caractérisation de ces dispositifs souples a permis de démontrer des performances dépassant (à notre connaissance) l'état de l'art précédent. Ainsi des fréquences caractéristiques f_T/f_{max} de 150/160GHz et des niveaux de bruit NF_{min}/G_a de 0.57/17.8dB ont été démontrées pour des transistors de type n.

Enfin, la stabilité de ces performances lors de la mise en flexion a été envisagée. Dans ce but, un modèle a été développé pour simuler l'impact des déformations sur les caractéristiques électriques des transistors MOS contrains. Ce modèle a permis de proposer une méthode basée sur l'ingénierie du plan neutre afin de minimiser l'impact de la mise en flexion sur les propriétés électriques des transistors. Enfin, ceci a été validé par des mesures réalisées sur des dispositifs fabriqués par la méthode de report développée, en prenant en compte les considérations mécaniques. Ces mesures démontrent qu'il est possible de limiter la variation des propriétés statiques et hyperfréquences des transistors considérés à 5% même après conformation sur un cylindre de rayon de courbure de 12,5mm.

En conclusion ces travaux ont démontrés la faisabilité de coupler les trois objectifs initiaux : flexibilité mécanique, performances électroniques et stabilité lors de la déformation. De plus, cette étude met en évidence tout le potentiel de cette technologie qui intégre sur un support souple les différents niveaux de métallisation nécessaires à la réalisation de circuits complexes. L'invariance des propriétés électriques lors du report et de la déformation permet d'envisager le transfert de circuits sur des surfaces non planes ou pour des applications nécessitant une flexibilité mécanique sans recourir à une étape de design circuit spécifique.

List of publications

International journal papers

A. Lecavelier des Etangs-Levallois, Z. Chen, M. Lesecq, S. Lepilliet, Y. Tagro, F. Danneville, J.-F. Robillard, V. Hoel, D. Troadec, D. Gloria, C. Raynaud, J. Ratajczak, and E. Dubois, *A converging route towards very high frequency, mechanically flexible and performance stable integrated electronics*, to be published

N. Defrance, Y. Douvry, M. Lesecq, F. Lecourt, V. Hoel, A. Lecavelier des Etangs-Levallois, Y. Cordier, A. Ebongue, and J.C. De Jaeger, *Fabrication, characterization and physical analysis of AlGaN/GaN HEMTs on flexible substrates*, **IEEE Trans. On Elec. Dev.,** accepted for publication (Oct. 2012)

A. Lecavelier des Etangs-Levallois, E. Dubois, M. Lesecq, F. Danneville, Y. Tagro, S. Lepilliet, D. Gloria and C. Raynaud, *Radio Frequency and low Noise Characteristics of SOI Technology on Plastic for Flexible Electronics*, **Solid State Elec.**, accepted for publication (Nov. 2012)

Y. Tagro, A. Lecavelier des Etangs-Levallois, L. Poulain, S. Lepilliet, D. Gloria, C. Raynaud, E. Dubois, and F. Danneville, *High Frequency Noise Potentialities of Reported CMOS 65 nm SOI Technology on Flexible Substrate*, **2012 IEEE 12th Topical Meeting on Silicon Monolithic IC in RF Systems**, 89-92 (2012)

A. Lecavelier des Etangs-Levallois, E. Dubois, M. Lesecq, F. Danneville, L. Poulain, Y. Tagro, S. Lepilliet, D. Gloria, C. Raynaud, and D. Troadec, *150-GHz RF SOI-CMOS Technology in Ultrathin Regime on Organic Substrate*, **IEEE Elec. Dev. Lett. 32** (11), 1510-1512 (Nov. 2011)

X. Tang, C. Krzeminski, A. Lecavelier des Etangs-Levallois, Z. Chen, E. Dubois, E. Kasper, A. Karmous, N. Reckinger, D. Flandre, L. A. Francis, J.-P. Colinge, and J.-P. Raskin, *Energy-Band Engineering for Improved Charge Retention in Fully Self-Aligned Double Floating-Gate Single-Electron Memories*, **Nano Lett. 11**, 4520-4526 (Oct. 2011)

M. Lesecq, V. Hoel, A. Lecavelier des Etangs-Levallois, E. Pichonat, Y. Douvry, and J. C. De Jaeger, *High Performance of AlGaN/GaN HEMTs Reported on Adhesive Flexible Tape*, **IEEE Elec. Dev. Lett. 32** (2), 143-145 (Feb. 2011)

Patent

A. Lecavelier des Etangs-Levallois, E. Dubois, F. Danneville, D. Gloria, and C. Raynaud, *Dispositifs et circuits semiconducteurs sur substrat flexible aux propriétés électriques invariantes sous application de déformations mécaniques*, to be published

International conferences

Aurélien Lecavelier des Etangs-Levallois, Vikram Passi, Zhenkun Chen, François Morini, and Emmanuel Dubois, *Characterization of PtSi nanowires transferred onto organic film*, **38th International Conference on Micro and Nano Engineering (MNE 2012)**, 16-20 January 2012, Toulouse, France (ORAL presentation).

Vikram Passi, Aurélien Lecavelier des Etangs-Levallois, Zhenkun Chen et Emmanuel Dubois, *Room temperature process for direct writing of nanostructures on plastic*, **38th International Conference on Micro and Nano Engineering (MNE 2012)**, 16-20 January 2012, Toulouse, France (POSTER presentation).

A. Lecavelier des Etangs-Levallois, E. Dubois, M. Lesecq, F. Danneville, Y. Tagro, S. Lepilliet, D. Gloria, and C. Raynaud, *Radio Frequency and low Noise Characteristics of SOI Technology on Plastic for Flexible Electronics*, **8th Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits (EuroSOI 2012)**, 23-25 January 2012, Montpellier, France (ORAL presentation).

Y. Tagro, A. Lecavelier des Etangs-Levallois, L. Poulain, S. Lepilliet, D. Gloria, C. Raynaud, E. Dubois, and F. Danneville, *High Frequency Noise Potentialities of Reported CMOS 65 nm SOI Technology on Flexible Substrate*, **12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems**, 16-18 January 2012, Santa Clara, CA, USA (POSTER presentation)

M. Lesecq, V. Hoel, A. Lecavelier des Etangs-Levallois, E. Pichonat, J.C. De Jaeger, Y. Douvry, F. Lecourt, A. Ebongue, Y. Cordier, *AlGaN/GaN HEMTs reported on flexible polyimide substrate*, **5th Space Agency – MOD Round Table Workshop on GaN Component Technologies**, 2-3 September 2010, Noorwijk, The Netherlands, pp. 9-12

National conference

A. Lecavelier des Etangs-Levallois, E. Dubois, F. Danneville, D. Gloria, and C. Raynaud, *Report hétérogène de dispositifs et circuits CMOS RF sur substrat souple*, **Journées National du Réseau Doctoral en Microélectronique (JNRDM)**, 7-9 June 2010, Montpellier, France (ORAL presentation).

Very high frequency, mechanically flexible and performance stable integrated electronics based on SOI-CMOS transfer bonding on plastic substrates

The ability to realize flexible circuits integrating sensing, signal processing, and communicating capabilities is of central importance for the development of numerous nomadic applications requiring foldable, stretchable and large area electronics. A large number of these applications currently rely on organic electronics, or integrate high mobility active films on plastic foils to provide higher performance. A key challenge is however to combine high electrical performance (i.e. millimeter wave, low noise electronics), with the mechanical flexibility required to conform to curvilinear surfaces, in addition to high stability of these electrical performance upon deformation.

In this work, a solution has been developed, based on thinning and transfer onto plastic foil of high frequency (HF) CMOS devices initially processed on conventional silicon-on-insulator (SOI) wafers. This transfer process first enables the fabrication of high performance electronics on plastic, with n-MOSFETs featuring characteristic frequencies f_T/f_{max} as high as 150/160GHz in addition to low noise potentialities: NF_{min}/G_a of 0.57/17.8dB. Secondly, by locating the neutral plane of the flexible system in its active layer, the relative variation of these high frequency figures-of-merit can be limited to 5% even after aggressive bending, demonstrating flexibility, high performance and stability.

Keywords: flexible electronics, SOI, CMOS, MOSFET, neutral plane, stress, strain

Report de technologie SOI-CMOS sur substrat flexible : une approche convergente vers les hautes fréquences et la stabilité des performances sous déformation mécanique

Le développement de nombreuses applications nomades, souples, déformables et sur de larges surfaces nécessite la réalisation de circuits mécaniquement flexibles, intégrant des capacités d'interaction avec l'environnement, de communication et de traitement de signal. Une part importante de ces applications provient actuellement de l'industrie de l'électronique organique, ou intègre des films semiconducteurs à forte mobilité sur des substrats plastiques afin d'atteindre de meilleures performances. La combinaison de hautes performances électroniques (ondes millimétriques, faible bruit), et d'une bonne flexibilité mécanique avec la stabilité des propriétés électroniques lors de déformations représente un des grands défis de l'électronique future.

Lors de ces travaux, une procédure d'amincissement puis de transfert sur un film plastique des composants CMOS initiallement réalisés conventionnellement sur des tranches SOI (silicium sur isolant) a été développée. Cette solution permet la réalisation de transistors MOS flexibles et performants : possédant des fréquences caractéristiques f_T/f_{max} de 150/160GHz et des performances en bruit NF_{min}/G_a de 0.57/17.8dB. De plus, positionner le plan neutre de l'ensemble au niveau de la couche active du transistor permet de réduire les variations de propriétés électroniques à 5% même lors de déformations agressives. La réalisation de composants souples, performants et stable a donc été démontrée.

Mots-clés : électronique flexible, SOI, CMOS, MOSFET, plan neutre, contraintes, déformations