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Fabrication and characterization of InAlAs/InGaAs High Electron Mobility Transistors on plastic flexible substrate

Par

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General introduction

The industry of electronic component and semiconductor established around 1960 and today, this viable business has been grown exponentially to be the 304 billion dollars market in the world. Over the last 50 years, micro-technology and nanotechnology have brought miniaturized circuit forward with the guideline of '*Moore's Law'*, which enable chip to operate on a dramatically smaller scale, work much more efficiently. Recently, this well-known downscaling trend is faced with the challenge because off-state leakage current appears in the smaller transistor dimensions due to short channel effect. The static power dissipation related to this leakage current, as a significant limiting factor of '*Moore's Law'*, starts to dominate the power consumption in the future micro-processor integration.

Although the effort to further develop advanced CMOS (Complementary Metal Oxide Semiconductor) technology and reduced the associated cost per function is made, some peoples begin to turn their attentions from '*More Moore'* and *'Beyond CMOS'* field to '*More than Moore'* field. So-called '*More than Moore'* devices typically convert non-digital or non-electronic information, such as thermal, acoustic, mechanical, optical and biomedical functions to digital data. In order to broaden the functionalities and satisfy societal needs, integrating various functional systems into the single package is an effective way to maximize the benefit of existing technologies.

During the past several decades, the rapid development of flexible electronics using different technologies have been attracted much interest as they can offer combined advantages such as mechanical flexibility, portability lightweight and reduction in assembly cost. With a flexible substrate, the electronics package might be folded or rolled up for storage when not operational. Silicon-integrated circuits are thinned to become compliant so that the smart card can't be broken when people sit on it. Due to their numerous advantages, this tremendous promising technology has been widely used in various domains: solar cells, display applications, flexible antennas, blast sensors, smart textiles, medical uses and other systems.

Up to now, in order to realize these cool applications, the novel processable solutions have sprung up like bamboo shoots after spring rain: organic electronic, amorphous silicon (a-Si), poly-crystalline silicon thin film transistors and printable semiconductors etc. Nevertheless, because the requirement of more frequency bandwidth applications is increasing nowadays, the need to operate in higher frequency range is scheduled. All the above technologies are limited in the further development of flexible device because of their poor internal transport properties.

General Introduction

The devices and circuits using III-V materials have been developed for high electrical performance, high frequency applications from ultra high frequency (UHF) to millimeter-wave frequencies. These III-V materials have a tendency to replace the traditional Silicon channel owing to their excellent transport properties. For example, the bulk electron mobility of $In_{0.53}Ga_{0.47}As$ is $1.2\times10^4\ cm^2V^{-1}s^{-1}$. This value is 8 times higher than that of the Silicon. And the electron thermal velocity of $In_{0.53}Ga_{0.47}As$ is $5.5\times10^5 m/s$, which is 2 times faster than that of the Silicon. Thus, more and more advanced high electron mobility transistors (HEMT) become the preferred choice for higher frequency as well as better performance application with lower noise figures for low noise amplifiers.

Recently, different technologies of transferring III-V materials onto flexible substrate, and even fabricating the transistors directly on the flexible substrate have been reported , which provides a possibility of employing the advantageous III-V materials in the flexible electronic innovation.

Therefore, the main aim of this dissertation research is to integrate the transistor, the fundamental circuit building block of modern electronic devices, onto the flexible substrate. We tend to add the value of flexibility into mm- and sub-mm-waves applications with ultra low power consumption technology for autonomous electronics. The manuscript is divided into three chapters.

In the chapter 1 of this dissertation, an overview of flexible electronics context and their significant practical applications are presented. Existing flexible transistors based on different materials are introduced subsequently. After a general review of the research in this domain, this chapter lists the different and classical technologies for these interesting devices fabrication process. The state of the art of flexible transistors is given in latter section of this chapter, showing several bottlenecks aspects in current device techniques. Finally, our essential objective of this work is proposed.

The second chapter focuses on the basic technology of fabrication. The standard HEMT fabricated on the rigid substrate (HEMT-RS) is used as benchmark. The key step in the process is to transfer the standard HEMT onto the flexible substrate (Kapton). The adhesive bonding technique is adopted by the bonding agent SU-8. When the device structure is stuck upside-down on the plastic material, the substrate and etch-stop layer will be removed by chemical solution. The mechanical bendability of our final sample is demonstrated. The experimental static and dynamic results of our HEMT-FS are exhibited at last. For clarifying the function of our devices on the flexible substrate, the comparison with the electrical performance of HEMT-RS is described simultaneously.

In the chapter 3, we propose the optimized design of epitaxial layer in order to suppress the Kink effect phenomenon which arises from the defect of previous structure. All improved static and dynamic performances without the negative influence are demonstrated. The last section of this chapter is comprised of mechanical bending test. We will give the answer on how flexible device electronics work under flexure. Three various degrees of bending conditions and different bending directions are studied in our research.

Finally, the manuscript will conclude present flexible electronic work. The perspectives on future work will be also briefly discussed at the end of our dissertation.

CHAPTER I

Introduction and Literature Review

Chapter 1: Introduction and Literature Review

1.1 Introduction

Over the past several decades, the term “flexible electronics” as a research topic has been getting hotter and hotter around the world because of their attractive advantages. In the beginning of this chapter, the discussion covers the context of flexible electronics development and their accompanying applications in various important fields.

As a result of combinational studies in chemistry and physics, material sciences provide enormous support and help in the evolution of flexible device technologies. We represent and compare the performances of the existing flexible transistors based on different materials. III-V materials employed in flexible domains have already shown strong high-frequency potential from numerous publications. The main device fabrication methods widely adopted in the flexible research are also introduced in the later part.

With the descriptions of the state of the art concerning the flexible transistors, several limitations of the existing flexible devices are pointed out. After comparing with the publication of some other techniques and considering the demand of high-frequency and high-speed integrated circuit in the near future, we decide to choose high electron mobility transistors HEMT based on III-V materials as our leading role of flexible electronics plan. The objectives of our research work are enunciated in the final part.

1.2 Contexts of Flexible Electronics

1.2.1 End of the Moore's Law

Over the last fifty years, the development and growth of solid-state-circuits industry has really brought myriad surprises to our daily life everywhere, ranging from communication to transport. The miniaturization of basic electronic element---Transistors and constant enhancement of their performance lead to these cutting-edge electronic products. In 1965, a bold prediction, which is now popularly referred to as '*Moore's* Law', was put forth by Mr. Gordon E. Moore, the co-founder of Intel Corporation. His observation outlines that the number of transistors on the integrated circuit doubles every two years. For nearly 50 years, this golden rule have driven the huge growth of function on a single chip at a lower cost per function and lower power per transistor by introducing new materials and transistor structures. Figure.1-1 (a) describes the exponential increase of transistors number per die during the past decades, showing *Moore's law* for memory chips and microprocessors plotted on a semi-logarithmic scale. The purple curve is the Moore projection based on data up to 1975 and it is marked a point of kink correction in 1980, which implies that the so-called law is only an approximation. From the red line, we can observe that the quantity of transistors per die was multiplied by a factor of almost 1 million from 1970 to 2010.

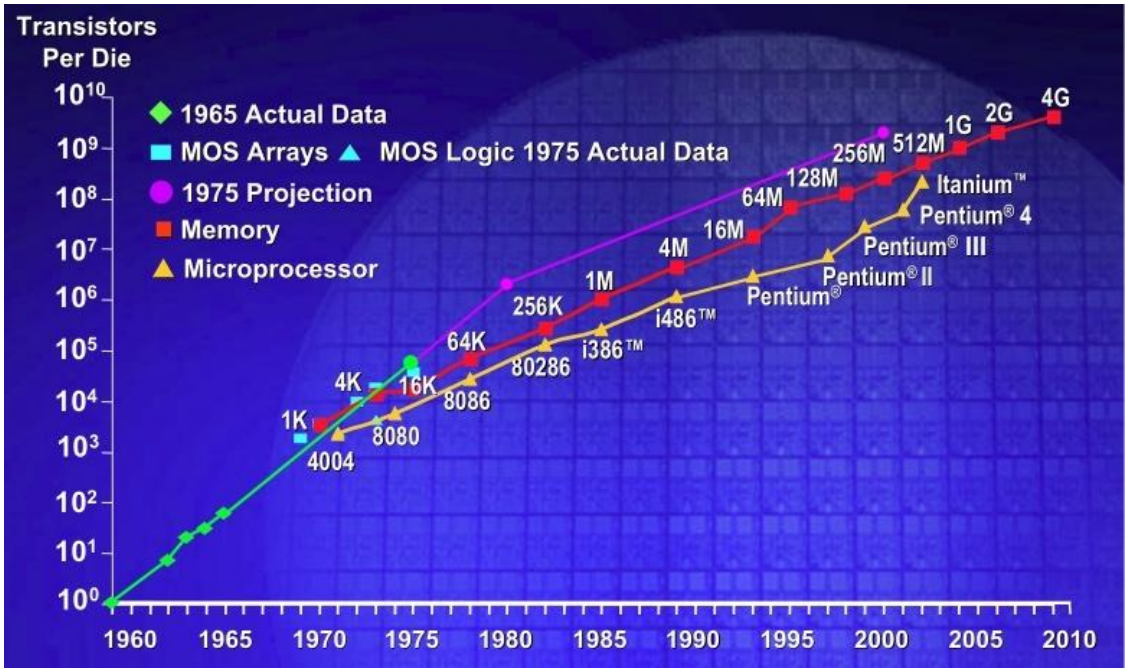


Figure.1-1 (a) Moore's law for memory chips and microprocessors

(Source: Intel Corporation) [1]

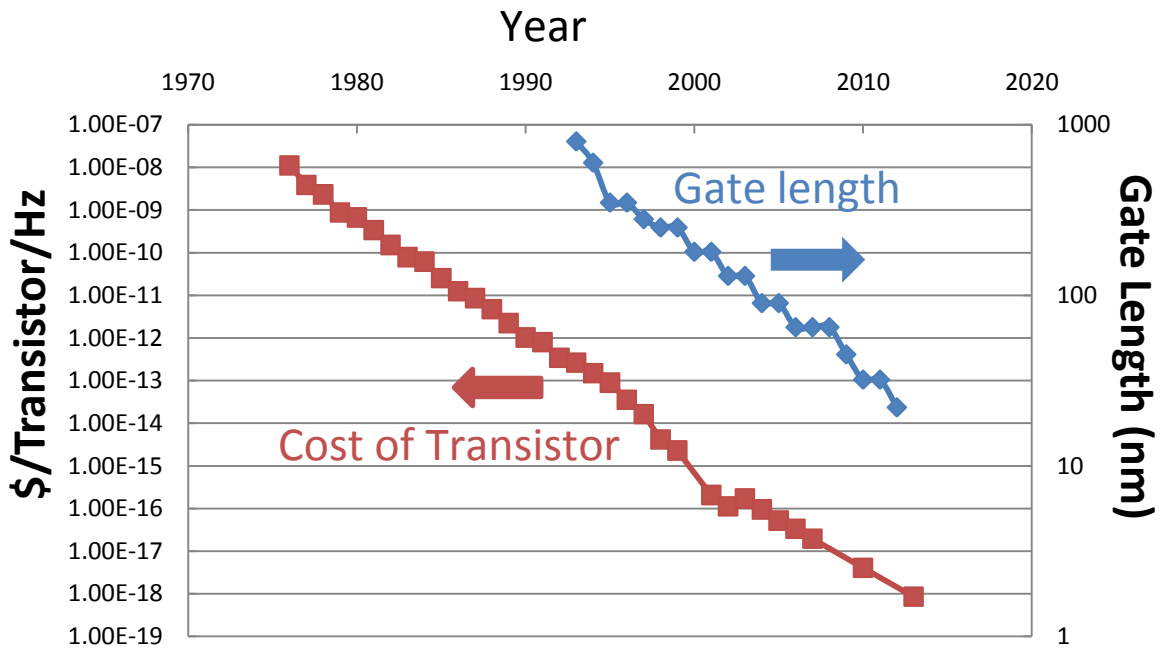


Figure.1-1 (b) Evolution of the cost of manufacturing integrated circuit [2]-[3]

Figure.1-1 (b) illustrates the decrease of one transistor cost per Hz (by a factor of 10 billion) and gate length (from 800nm in 1995 to 22nm in 2012). With the support of novel processing equipments, such as advanced photolithography, the use of high-k material for gate dielectric and larger wafer diameter etc., challenges of shrinking transistor size have been overcome successfully and at least, up to now, we have kept up with *Moore's law*. Nevertheless, the era of atomic scale is approaching. Relying solely on downscaling to improve the density of transistors and intrinsic performance of electronic devices becomes more and more difficult due to short channel effect, current leakage and power dissipation etc. This inevitable physical limit maybe slow down the growth of semiconductor industry in one tendency, but in parallel, it stimulates a brand new trend, called '*More than Moore'*, which addresses an emerging category of devices that incorporate several functionalities that do not necessarily focus on *Moore's law* , but provide additional value to the customer need in different solutions.

1.2.2 Newly-born Trend : *More than Moore*

In 2005, ITRS (International Technology Roadmap for Semiconductors) introduced a concept of Functional Diversification-*More than Moore* for the first time. When minimum feature size of CMOS transistor and interconnect dimensions approach their fundamental limits, the integration of diverse components and devices in a single heterogeneous system tend to provide new value in next generation products of semiconductor industry. The innovative functional requirements of interacting with the environment, such as bio-chips, sensors, actuators, radio-frequency (RF) devices, micro-fluidic devices, micro-, nano-electromechanical systems (MEMS and NEMS) and flexible electronics will play a pivotal role sooner or later. Figure.1-2 represents the possible directions to create higher value systems from ITRS 2007 executive summary. [4]

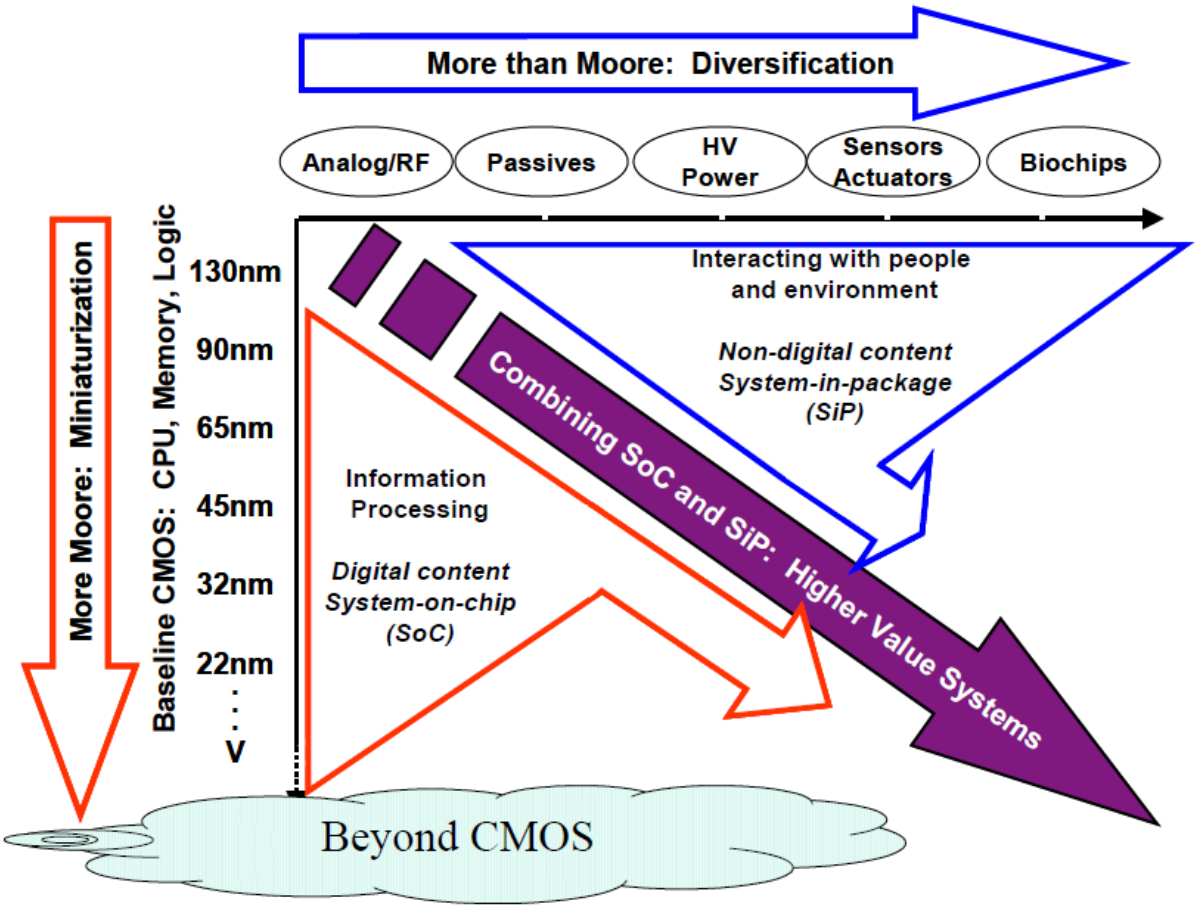


Figure 1-2: Two different development directions of '*More Moore'* and '*More than Moore'*

According to roadmap scope proposed by ITRS, the vertical axis is the '*More Moore'* which focuses on improving computation performance through miniaturization of CMOS technology: CPU, memory, logic. The horizontal axis stands for '*More than Moore'* where add-on

technologies are used for providing additional functionalities and connecting CMOS chips to human being and environment. The purple arrow in the middle means that combining each specific advantages of Systems-on-Chip (SoC) and Systems-in-Package (SiP) is recommended to produce higher value system. Here, SoC is used to integrate diverse IC functions (module of radio-frequency, analog, digital, mixed-signal…) into a single chip, offering greater miniaturization, improved performance, and lower cost in volume but at the cost of longer time to market and higher non-recurring engineering expense. On the other hand, SiP concerns a number of ICs enclosed in a single package. By using existing and available integrated circuits, SiP can assemble different die technologies and applications with active and passive components to form a complete system or subsystem. Although SiP architecture enable people to integrate different front end technologies, different generation devices, upgrade and redesign individual chips, it needs to undergo more complex assembly and excessive power density for stacked dies.

Moreover, against the background of a boost in '*More than Moore'* field, an increasing number of the requirements and challenges concerning the flexible electronics development have been referred to in the latest ITRS reports. For example, in 2009 edition of chapter *'assembly and packaging'*, [5] ITRS predicted as follows:

> ***'Flexible electronics is projected to grow into a multibillion-dollar industry over the next decade and will revolutionize our view of electronics. The unique properties of flexible electronics, such as its compliant structures, ultra-thin profiles, low weight, and potential low cost and high reliability could have enormous impact on consumer electronics, aviation and space electronics, life sciences, military applications and telecommunications. Flexible electronics will enable a broad range of devices and applications not possible today.'***

Huge interest in flexible electronics is also kindled in business market. In July 2012, Global Industry Analyst, Inc (GIA) announces the release of a comprehensive global report on Flexible Electronics markets:

> ***'The global market for Flexible Electronics is forecast to reach US$25.9 billion by the year 2018, propelled by the increasing demand for lighter and smaller electronic products with low power consumption. The market, considered to be in an embryonic stage, is currently the focus of intense research by universities, research institutes, and technology driven enterprises. In future, the market offers immense potential for rapid growth with applications extending beyond the traditional sphere to military, automotive, aerospace, medical, and consumer applications.'***

With these spirits above, rendering our conventional electronics (single chip, SoC, SiP) *'flexible'* for novel applications can be defined as one promising functional diversification in the coming era of '*More than Moore'*.

1.2.3 Brief History of Flexible Electronic

We can see flexible stuffs around us every day, such as paper, clothes, rubber, and plastic bag, etc. Engineers are pushing to weave electronics into the objects all around us and doing that requires flexible circuits. Before getting noticed as a member of '*More than Moore'* family, flexible electronics has a surprisingly long and rich history.

The development of flexible electronics can date back to 1960s. It began with the flexible solar cell. R. L. Crabb and F. C. Treble reduced the thickness of single crystal silicon wafer cells to almost 100μm and transferred them onto a plastic substrate, which, for the first time, provided flexibility for the solar cell arrays [6]. After that, hydrogenated amorphous silicon (a-Si:H) cell lent itself to fabrication on flexible metal or polymer substrates. They can be deposited in thin films at relatively low temperature onto a variety of substrates. In the beginning of 1980s, Schottky barrier and p^+-i-n^+ were made on organic polymer substrate film substrate by Plattner [7] and Okaniwa [8]. And meanwhile, the CdS which had been developed for Cu_2S/CdS hetero-junction thin-film solar cell on glass substrate could be continuously deposited on a moving flexible substrate inside the reel-to-reel vacuum coater [9]. In the following years, the roll-to-roll (R2R) processing technique for a-Si:H cells on flexible steel and organic polymer substrate was spread [10][11] and today, it is maturely used in the fabrication of other flexible materials and devices.

The first flexible transistor can date back to 1967. Mr. Brody and his group made a Te thin film transistor (TFT) on the paper strip and proposed using TFT matrices for display addressing. Brody's group also made TFTs on several different flexible substrates, such as Mylar, Kapton and anodized aluminum wrapping foil. Their TFTs could be bent to 1/16 inch radius without apparent damage and continued to function. [12]

In the mid-1980s, both the success of amorphous silicon based devices in large area active matrix liquid crystal displays (AMLCD's) industry and the demonstration of photovoltaic on flexible substrates stimulated interest in the development of new classes of silicon-based thin-film circuits on novel substrates. Mr. Constant, in 1995, fabricated a-Si:H TFTs based circuit on flexible polyimide substrates [13]. A conformal coating polyimide of 6μm was applied to a rigid silicon wafer to form a polyimide film. In 1996, a-Si:H TFTs were made on flexible stainless steel foil [14]. In 1997, polycrystalline silicon (poly-Si) TFTs fabricated on plastic

substrates by using laser-annealing were reported [15][16]. From then on, industry of flexible electronic has expanded prosperously. More and more laboratories and companies have delivered flexible circuits and display productions using a-Si:H, organic materials, mixed oxide TFT, hybrid organic/inorganic CMOS technologies and Graphene [17][18][19][110]. Some electro-optic materials have been demonstrated for manufacturing flexible displays, such as E-Ink Corp's electrophoretic ink, organic light emitting diodes (OLED) and Kent Display's cholestric material etc. Figure.1-3(a) shows a 1.1 inch flexible displays on heat stabilized polyethylene naphthalate (PEN) by using the backplanes of a-Si:H TFTs [20]. At the CES 2006, Philips showed a rollable display prototype whose screen can retain an image for several months without electricity [21]. In 2013, Samsung integrated its OLED technology into their new flexible display device and LG unveiled the world's first plastic e-paper display which will even revolutionize the E-book market. Both of them are shown in Figure.1-3(b) and Figure.1-3(c). The thinness, lightness and robustness enabled by the flexible displays create digital reader products that are as comfortable and natural to read as paper.

(a)

(b) (c)

Figure.1-3: (a) Amorphous silicon backplane on PEN substrate, (b) Samsung Flexible AMOLED Display, (c) LG e-paper Display

1.3 Applications of Flexible Electronics

As discussed above, in recent years, we have witnessed that flexible display is one of the most intriguing applications for semiconductor industries since it does not require high-speed devices. But in the long run, however, flexible electronics will certainly encompasses an enormous variety of fields far beyond our imagination. The advantages of flexible electronics and some envisions of their possible applications are talked over below.

1.3.1 Flexible Macroelectronics

Before detailing flexible applications, the term *'Macroelectronics'* needs to be explained. The concept of *'Macroelectronics'* is a still young field which was introduced in 2005 by Robert H.Reuss [22]. In the activities of macroelectronics, microelectronic devices need to be integrated onto large area substrates with size much bigger than traditional semiconductor wafer, which enlarges system scale. Having sizes measured in square meters, macroelectronics are currently based on amorphous silicon (a-Si) or polycrystalline silicon (poly-Si), thin film transistors (TFTs) on glass, and are finding important applications in various areas, including flat panel display (FPD), solar cells, image sensor arrays and digital x-ray imagers.

In fact, after the commercial success of flat panel display, large area electronics has entered into a new era. Further increasing desires for macroelectronic systems, including bendability, stretchability, portability and low-cost tends to be realized by integration of organic, inorganic materials and flexible substrates (polymer, polyimide, PEN…). Printing technology and roll-to-roll techniques have already shown great advantages in the throughput improvement and cost reduction of fabrication process. However, it should be pointed out that, limited by their low carrier mobility, current TFT technologies using organic materials, poly-Si or CdS cannot satisfy the high frequency communication requirement on flexible application in large surface area. Figure.1-4 represents the merits and drawbacks comparison between conventional microelectronic and novel macroelectronic at present.

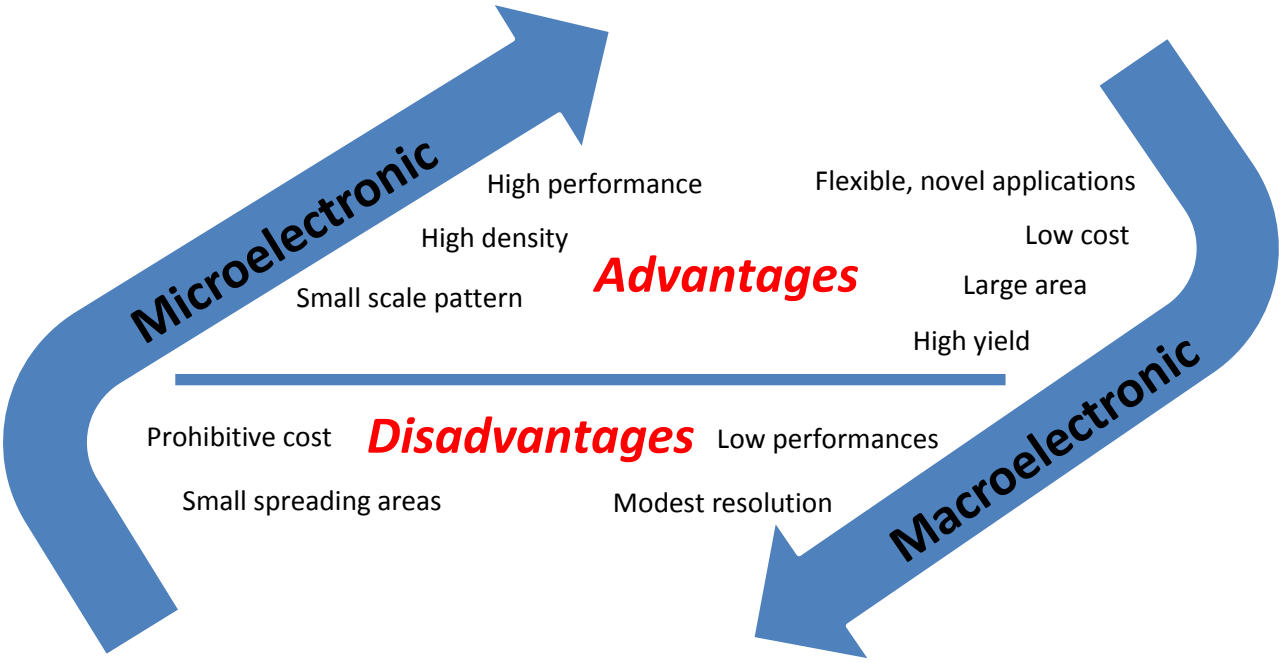


Figure.1-4 Comparisons of advantages and disadvantages between microelectronic field and macroelectronic field

So the 'next generation' flexible electronics can be viewed as a creation of combining their advantages and avoid their shortcomings. And how to open up such avenue to high-performance flexible macroelectronic is also one objective of our work.

1.3.2 Applications in various fields

- **Large area detectors**

As stated above, here is an example of macroelectronic in the medical field. X-ray imager is a kind of important equipment to checking a patient's health condition. Modern digital x-ray imaging has already gained general acceptance and also has a long term economical advantage in recording patient's disease by digital format. If we could realize these x-ray imaging sensors on flexible substrates, it is possible to have portable tools for field use in outside space, such as battle field and some urgent cases like earthquakes, floods, etc. Furthermore, the future integrated system in a stretcher will enable x-ray detector to send the images wirelessly. The hospital servers will receive images quickly for immediate uses. This promising technology can be expanded to detect neutrons and gamme rays for security purposes in ports of entry and public transport stations [23].

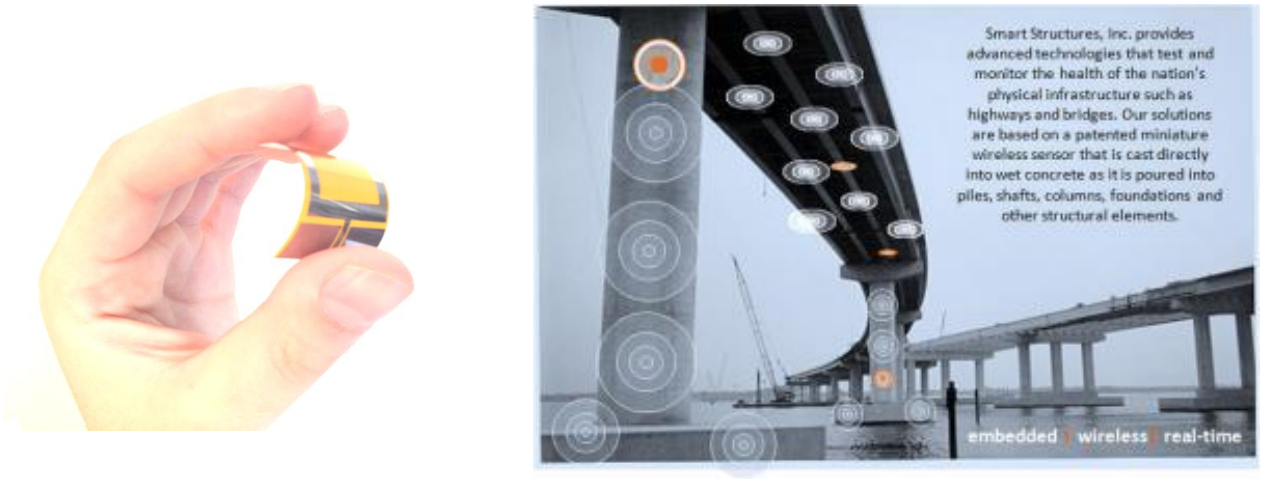
- **Smart textiles**

Smart textiles, also known as E-textiles, are hybrids where electronic components are integrated into textile fibers. Recently, there is increase interest in smart textiles for health monitoring, display applications and entertainment. More and more intelligent clothing, smart clothing, wearable technology, and wearable computing projects involve the use of smart textiles. For example, multiple sensors and display apparatus can be embedded in the fabrics for monitoring heart rate, stress, guided training or toxic gases concentration in the environment etc.

Another key driver for smart textile is that their fabrication processes are capable of creating large-area surfaces automatically and rapidly. Typical industrial weaving machines can fabricate more than 10×10^6 square meters of textile per year [24]. Roll to roll print methods of flexible electronics can print 100~150m/min.

- **Flexible antennas**

Undoubtedly, transceiver components are a key part of any flexible wireless communication in the future. Such applications require high performance transistors as well as integrated antennas. Researchers have shown flexible antenna fabricated on polymer SU-8/PDMS substrate, which not only target the wearable computing, but also fit well in the radio-frequency system-on-package (RF SOP) applications [25]. Designed by University of Arkansas, the antenna based on a polyimide Kapton substrate and fabricated by ink-jet printing technology was shown in Figure.1-5 (a). [26]



(a) (b)

Figure.1-5 (a) Flexible printed monopole antenna based on Kapton Polyimide substrate; (b) Flexible antennas are embedded into smart physical infrastructures such as bridges, highways for testing and monitoring the health of the constructions.

Besides, there is another reason why flexibility is so especially attractive for antennas. The frequency of an antenna is determined by its shape, which means that you can tune the antenna by deforming them. Figure.1-5 (b) gives a beautiful example of monitoring civil construction by flexible antenna. As the bridge expands and contracts, it would stretch the antenna in a flexible silicone shell and change the frequency of the antenna. Civil engineers will receive real-time information about the bridge condition wirelessly. Flexibility and durability are also ideal for military equipment. Antenna could be folded or rolled up into a small package for deployment and unfolded again without any impact on its function.

- **Solar cell**

Flexible solar cell could be one convenient alternative energy source for autonomous flexible system applications both indoor and outdoor in the future. For example, as flexible displays that use organic light-emitting diodes (OLEDs) have applied in thin layers over plastic make electronic viewing more convenient than reading on paper, a flexible solar cell might easily power the OLED device enabling unlimited access to a large number of pages. Thin-film flexible photovoltaics are paving the way to low-cost electricity. Organic, inorganic and organic–inorganic solar cells are deposited over flexible substrates by high-throughput technologies, like roll-to-roll or printing way, to afford lightweight, economic solar modules that can be integrated into various surfaces. Figure.1-6 envisions a possible art of power plastic by *konarka*® in the coming future.

Figure.1-6 *Konarka*'s organic photovoltaic technologies make their flexible solar cell in every corner of our life.

Such organic photovoltaic functionalities get integrated at low cost in commercial buildings and remote structures, printing rolls of the photovoltaic material anywhere, from windows to roofs, through external and internal walls, replacing the traditional installation approach with an integration strategy. The renewable and clean energy is not a dream any more.

- **Sensors and Actuators**

Almost any modern system contains sensors to observe the environment and actuators to influence this environment. A typical example of such an interaction is an automobile which is equipped with temperature, pressure, speed, chemical sensors and various mechanical values and engines. Demonstrations using thin flexible strips equipped with sensors for pressure and chemical monitoring have been reported. [27][28]

For several military and civilian applications which help in exploration, these machines have to be maintained temporarily and transferred to the testing facility. The cost of this exercise is expensive. Flexible sensors can potentially be conformal to the surface of these vehicles and machines so that the onsite tests can avoid the prohibitive cost and save time.

Flexible sensors and actuators are also given more and more concerning in the field of mankind itself. For example, we need well-designed humanoids to simulate human functions such as walking, jumping or reflex behavior. But their inside electrical motors have different mechanical properties from our human muscles. Thus, developing a new pliable muscle model by flexible actuators, we can obtain deeper understanding of our own mechanism. In human health area, such thin and flexible sensors and actuators are capable of being used as surgical sutures for targeted wound monitoring therapy [29].

In fact, organic FET-based flexible sensors and actuators have been already applied in some sensors and actuators. The first application of large area sensor is a pressure sensor used for electronic artificial skin (E-skin) of next-generation robots [28]. Even if the mobility of organic materials is relatively lower than that of single-crystalline Si or poly-Si, such slower speed is still tolerable for most applications in large-area sensors.

In summary, from all applications mentioned hereinbefore, we can conceive a fully autonomous flexible body system. Figure.1-7 is an embryo module of this idea. This system is capable of recording information from the environment by integrating various sensors. It could also react according to the processed data by actuators, or be sent a long distance via antennas. Besides, such concept device could also be powered by energy harvested from the environment using photovoltaic cells, piezoelectric or thermoelectric units and stored in micro-batteries embedded in the system.

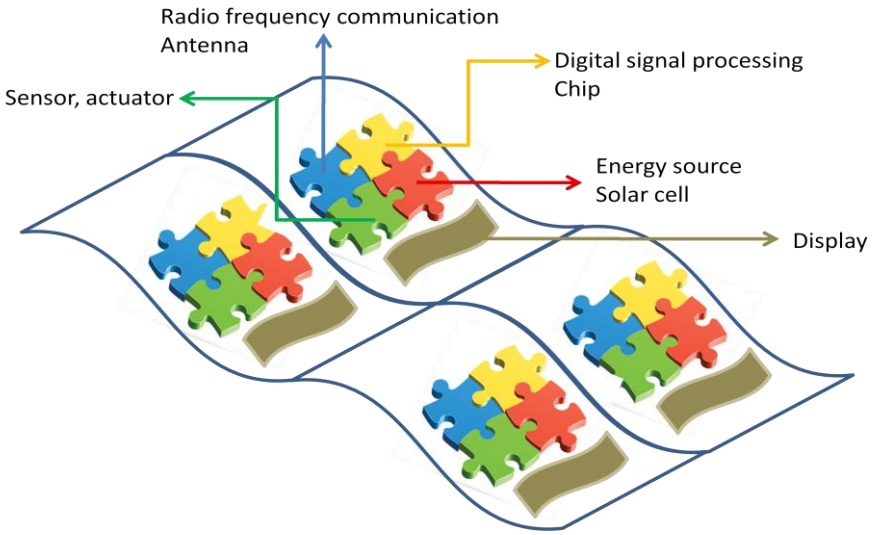


Figure.1-7 One proposed module of total flexible autonomous systems, integrating information receptor, processor, transmitter and energy source, display

1.4 Flexible Transistors

As an electrical connector, a reliable backplane system is the backbone of whole devices and circuits to supply the power and collect the signal for frontplane. In this review, contributing to the basic units in the backplane circuits, a series of existing flexible transistors which have been developed over last several decades are presented. In order to well differentiate the material types, the section is divided into two parts: organic electronics and inorganic electronics.

Before presenting the transistors device in this section, we review some important figures of merit (FOM) for existing flexible transistors relate to the following respects:

1). gate length L_g

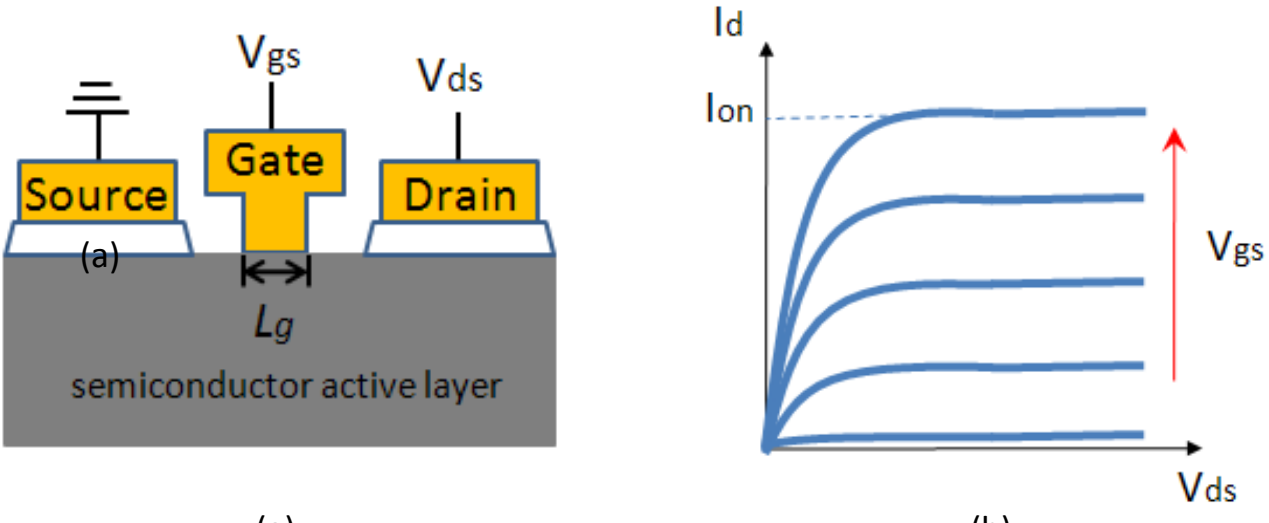
2). current I_{ON}, current I_{OFF} and on/off currents ratio

3). static transconductance g_m

4). charge carrier mobility µ

5). cut-off frequencies f_T and f_{MAX}

These basic parameters of semiconductor physics are succinctly described in Figure. 1-8 (a)-(f), More detailed clues can be acquired handily in textbook [30], therefore we will not rewrite in this dissertation. These FOM are used to assess and compare different technologies and device performances in the following sections.



(a) (b)

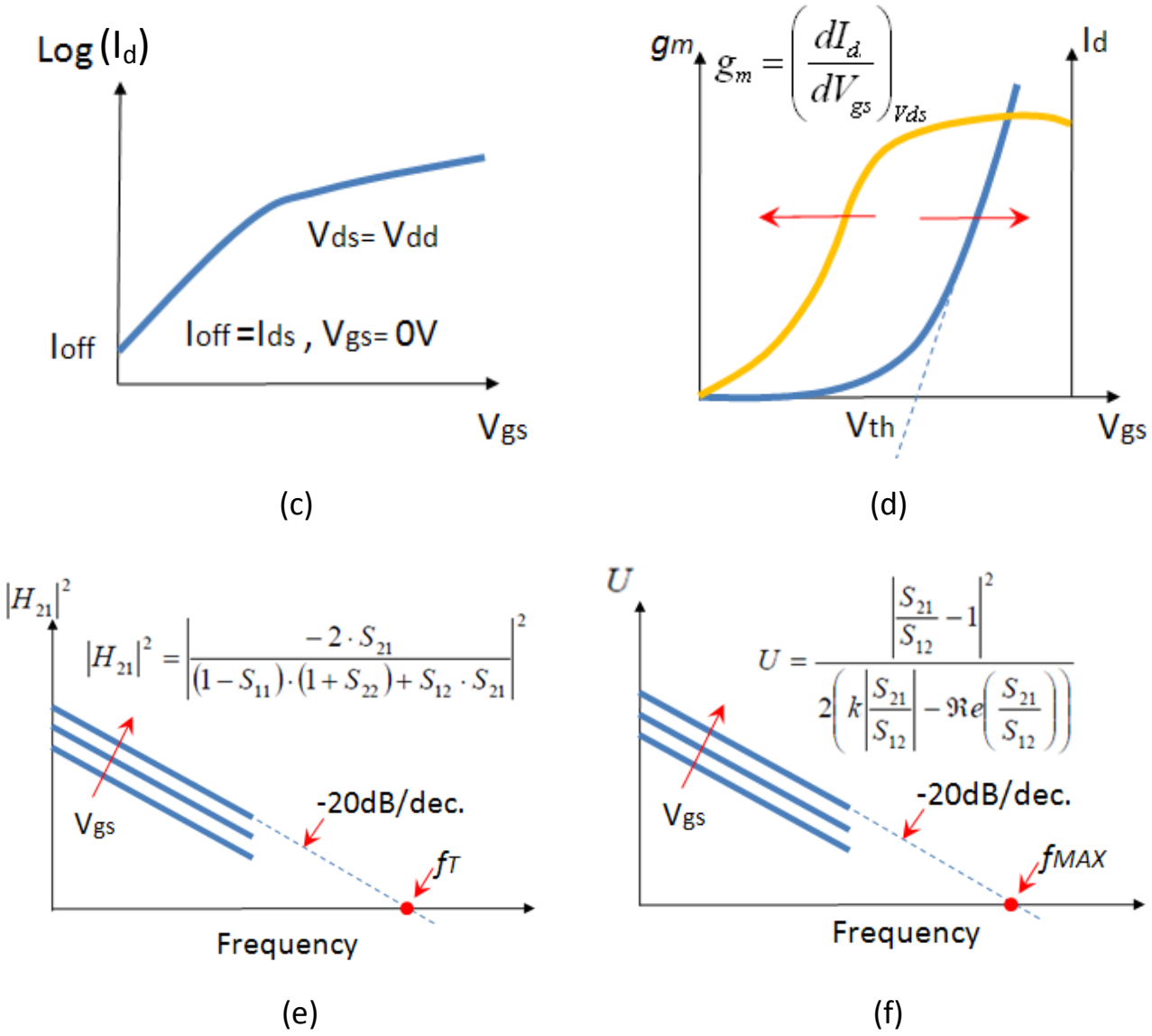


Figure.1-8 : (a) Schema of transistor structure ; (b) Typical I_d-V_{ds} characteristic ; (c) Log(I_d)-V_{gs} characteristic ; (d) Transconductance g_m-V_{gs} characteristic ; (e) Current gain $|H_{21}|^2$-Frequency ; (f) Mason's Unilateral gain *U*-Frequency

1.4.1 Fabrication schemes for flexible electronics

Commonly-used fabrication strategies in flexible industry will be presented in this section. We summarize two main processing methods: (1) Transfer-and-bond onto flexible substrate (2) Device fabrications directly on flexible substrate.

1.4.1.1 Transfer-and-bond Approach

The transfer-and-bond approach has advantage of sticking ready high-performance electronic devices onto flexible substrate, which enables flexible circuits to compete with the rigid-based industries. This fabrication strategy not only benefits the mature conventional fabrication technology, but also avoids the change of organic substrate properties and substrates deformation caused by high temperature during the fabrication process.

The approach includes three main steps:

1. The whole electronic devices are fabricated on a rigid substrate (Silicon, III-V wafer or a glass plate) by standard procedure.
2. The back side of the rigid substrate was thinned by using different etching techniques, which allows devices to be mechanically bendable without losing their functions.
3. The structures are completely transferred and bonded onto a flexible substrate.

The order of second and third steps can be interchanged in some fabrication process.[31]

The micro and nanofabrication of conventional high-performance transistors and circuits do not belong to our research field, and will not be described here. More details can be obtained in other places [32][33]. Herein, we focus more on the second and third fabrication process. By reducing thickness of original rigid substrate, it is possible to curve the fabricated devices on ultra-thin foil to some degree before reaching the damage threshold. Several etching techniques have been developed for this thinning solution:

i) Dry processes based on plasma etching
ii) Wet-etching by chemical solutions
iii) Mechanical ablation methods

Thinning processes based on the above techniques and developed at *IEMN (Institut d'Electronique de Microélectronique et de Nanotechnologie)* laboratory have been reported [31][34][35].

Before bonding the total thinned devices wafer onto flexible substrate permanently, a temporary carrier was bonded previously on the front side of the processed wafer in order to protect the ultra-thin wafer from deformation and improve the substrate's dimensional stability [35][36]. The perforated sapphire wafer was used as a temporary carrier to facilitate its release from the active wafer after thinning die process and transfer bonding of the thinned die onto an organic film. Moreover, the electrical performances should be sustained after the back side etching and the transfer onto flexible foil. Influence of the back side lapping on CMOS chip down to the micrometer scale have been reported [37]. The thinning process showed no obvious impact on the static electrical characteristics of transistors.

Spun or spread over both the surfaces of organic flexible substrate and semi-conductor

devices, SU-8 photoresist is commonly used as an adhesive agent[31][36][38] in the transfer bonding step. Note that SU-8 need to be cross-linked by UV exposure after pressure bonding process in vacuum ambiance. More detailed information about these problems is told in our chapter of fabrication methodology.

However, the transfer-and-bond approach is today only adopted in small surface area coverage and its cost is relatively expensive. Those bonded circuits will likely be added to large-area electronic surfaces at low density for high-speed communication and computation, lasing, and similarly demanding functions.

1.4.1.2 Direct fabrication on flexible substrates

On the contrary, the direct fabrication on flexible substrates is the most direct and more creative approach to the manufacturing of large-area electronics. This research hotbed have developed a series of new process techniques, like printing of etch masks, additive printing of active device materials and the realization of electronic functions by local chemical synthesis. However, it should be pointed out that not all flexible substrate materials are compatible with conventional planar silicon micro-, and nanofabrication processes. For example, the compromise between device performance and relatively low process temperatures tolerated by polymer substrates has to be considered. In the following section, three widely reported strategies of integrating micro or nano electronics devices onto a flexible organic foil are introduced.

1.4.1.2.1 Bottom-up Approach

The term ‘Bottom-Up’ means that we establish a large and complex system from the individual base elements like nanoparticule, nanotube, and molecule. Bottom-Up approaches oftentimes adopt inorganic semiconductors nanostructures, such as nanowires and nanotubes which can be fabricated in large-area and low cost and thereafter, transferred onto the organic film, which enables the subsequent device fabrications (e.g. E-beam lithography, lift-off, metal deposition for source, drain and gate electrode) to be continued on the flexible substrates.

After the first synthesized silicon nanowire was realized in 1964 by vapor liquid solid growth [39], similar approaches of inorganic nanostructure synthesis based on bottom-up mechanism have been developed for single nanowire and nanotube transistors which exactly exhibited excellent charge carrier mobility [40][41]. Moreover, these ways of synthesizing nanostructure can be integrated into nanoscale devices at low temperature [42][43][44]. After nanostructures are released from their growth substrate and are dispersed in appropriate

solution, post synthesis suspension and device fabrication can be finished at room temperature. This advantage facilitates the integration of those nanostructures onto organic flexible substrates without considering the tolerance of organic materials in high temperature processing. However, in this approach, after solution based deposition of randomly dispersed nanowires, a conventional lithography process is performed to define the source and drain electrodes which are subsequently realized by metal deposition and lift-off [42][43][45][46]. The nanowire transistor location on the substrate highly depends on the random location of the chosen nanowire. Such process for drop-casting of random aligned nanowires shows a low device throughput. It is only feasible to study individual nanowire properties, but is limited for more complex circuits and larger area coverage of electronic devices applications.

As a result, the assembly of nanowires employing controlled orientation and interspacing over large area has been developed. In the past several decades, significant research effort has been made on developing generic approaches to assemble nanowires on various substrates: flow-assisted alignment [47], bubble-blown techniques [48][49], electric field-directed assembly [50][51], Langmuir Blodgett [52], contact printing and different roll printing techniques [53][54]. Such ordered assembly of nanowires, or nanotubes enhance the drain current , which opens another way to achieve high performance devices [55].

Numerous high performance transistors and circuit based on CNT or nanowires by chemical synthesis deposition have been demonstrated[47][56][57][58]. Better electrical performances are obtained by ordered assembly methods than randomly dispersed networks.

1.4.1.2.2 Top-down Approach

Different from ‘Bottom-Up’ approach, ‘Top-Down’ strategies fabricate the nanoscale devices using larger devices or equipments to pattern them by photo, or e-beam lithography, which are also shown as promising choice for flexible technique.

The free-standing inorganic thin films exhibit both the mechanical bendability and the intriguing electrical properties of monocrystalline materials, like silicon, or III-V compound semiconductors [59]. Moreover, although chemically synthesized nanostructures can be produced in bulky throughput, top-down fabrication features some following advantages.

First of all, bottom-up synthesis is able to realize numerous distributions in nanostructure sizes, crystallographic orientations, and doping levels. Such methods for controlling the uniformity of these parameters benefit from less experience than techniques used conventionally in the semiconductor industry [60]. In fact, lithographic and etching processes on single crystalline wafers result in the fabrication of well-controlled, reliable and homogenous micro or nanoscale devices that can be used for flexible electronics [61][62].

Next, assembling bottom-up nanostructures into flawless arrays and layouts cannot be easy. In the previous section, those various assembly methods witness the long research. With the help of lithographic processing for top-down nanostructures on rigid wafers realized by transfer printing, the relative position and orientation are able to be kept well, which makes a higher level of alignment standard possible.

In order to detach fabricated nanostructures from initial substrate, an embedded sacrificial layer is usually necessary. For example, silicon-on-insulator (SOI) wafers enable easy processing on the top layer of monocrystalline and subsequent lift-off of patterned nanostructures by dissolution of the buried oxide layer (BOX) in hydrofluoridric acid (HF) [61][63][64][65][66][67][68]. This method even leads to the transfer onto plastic film of strained single crystal thin films, allowing flexible electronics to benefit from the advantages of strained silicon layers [68]. Besides, undercutting can be performed below the nanostructures, which facilitates the release from the initial substrate [69][70][71][72][73].

Micro or nanostructures fabricated by top-down approaches on conventional rigid semiconductor wafers can be post-processed like bottom-up methods using those assembly techniques mentioned above. Low temperature assembly of monocrystalline nanostructures on plastic films can be achieved using the same differentiation between the initial substrate (used to fabricate the elementary building blocks) and the final film (where the assembly and device patterning is realized). This leads to high gigahertz range frequency for flexible electronics based on nanomembranes[63][65][70].

Most work relating to the transfer of top-down nanostructures for high frequency flexible electronics focuses on the dry stamp printing technique [63][65][67][68][70][74][75]. The patterned nanostructure on the substrate is firstly transferred onto an inked elastomeric stamp, and then we release the nanostructure from inked stamp which is a temporary carrier to the final application substrate. The improvement of printing resolution has been demonstrated by adopting the stamp as the final substrate [63]. In this case, direct flip transfer occurs from the donor substrate to the final stamp substrate. On the contrary, completing the stamping process by transferring the nanostructure from the stamp onto a second substrate is an indirect transfer method. If the nanostructures can be flipped upside down without impact on the final device properties, the direct method is preferred due to its higher printing resolution (± 0.5 μm, whereas complete stamping process results in ± 2 μm level [63]. Three-dimensional assembly of different active layers has also been reported using such stamping process on plastic material [75].

1.4.1.2.3 Printed Electronics

Printing technology belongs to another type of direct circuit fabrication on flexible substrate. It is compatible with roll to roll process, is also a high-throughput scheme, using device materials efficiently without vacuum requirement and providing a solution to overlay registration issue through digital compensation. Currently, several main methods for printed electronics exist: i) flexography printing, ii) gravure printing, iii) inkjet printing and iv) screen printing[76]. Combining with conventional semiconductor industry techniques, those techniques are able to improve the performance of current printed electronics and lower their manufacture cost.

The resolution and speed of printing methods are summarized in Table 1-1[76]. Essential characteristics of each technique are presented as well. From all above mass printing methods, in order to achieve better transistor performance of printed electronics, it is necessary to achieve the resolution near or below 1μm. Some research works have demonstrated micrometer scale resolution, adopting inkjet printing [77][78]. Meanwhile, we also expect to increase the throughput as high as possible. The trade-off between these two elements should be considered by academic work.

Table 1-1 Characteristics summary and comparison of the resolution and speed among the different commonly-used printing techniques

Printing Technique	Speed (m/min)	Resolution (μm)	Characteristics
Flexographic printing	50~500	30~75	Wide variety of substrates, low ink viscosity
Gravure printing	20~1000	10~75	Simpler process, surface smoothness required
Inkjet printing	1~100	20~50	No mechanical contact with the substrate, 3D realization possible
Screen printing	10~100	50~100	Enable high ink thickness and viscosity

1.4.2 Organic Thin Film Transistors

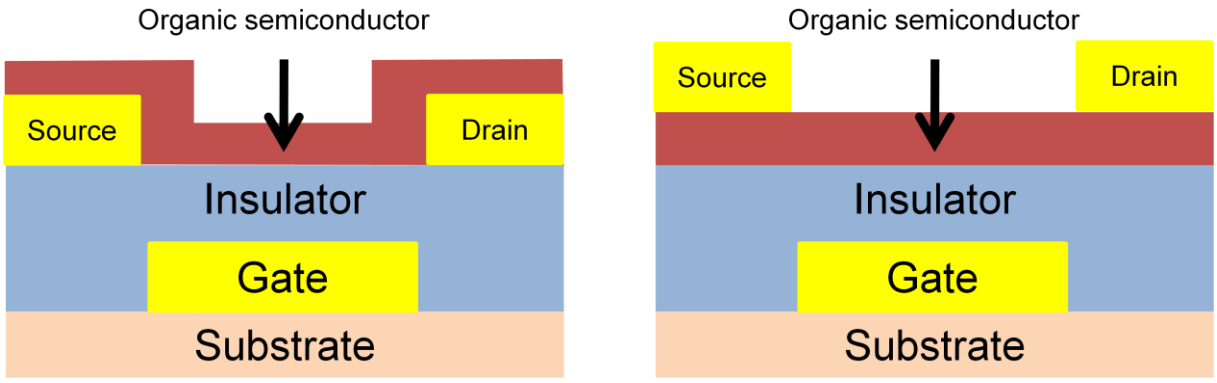
Organic nanostructure semiconductor materials have been considered as an innate candidature for the flexible electronics owing to their intrinsic flexible property whose Young's modulus is inferior to 100GPa and compatible with commercially available plastic substrates. Organic materials offer a direct patterning of active material instead of the long and expensive fabrication steps including photo-lithography, high temperature and strict vacuum evaporation used by conventional silicon-chip architecture. Furthermore, it is possible to manufacture large-area products using R2R fabrication processes. Table 1-2 briefly compares the characteristics of organic electronics with those of traditional inorganic semiconductor technology.

Table 1-2 Characteristics of organic electronics versus inorganic electronics [79]

Organic Electronics	Inorganic Electronics
Low cost per unit area	High cost per unit area
Low capital flexible plant	High capital in dedicated plant
Large area products	Small area products
Flexible substrates	Rigid substrates
Robustness	Fragility

Hence, with these high spots listed in the table above, organic semiconductors and metals have the potential to replace conventional inorganic materials in some applications ranging from individual component: resistors, capacitors and transistors to active matrix displays, analog or digital circuits.

The first demonstration of the field effect in a small molecule organic material (α-copper phthalocyanine films) can date back to 1964 [80]. In 1983, the field effect in a polymer structure made by a solution process was reported [81]. From then on, the field of organic thin-film transistors (OTFTs) has lived to see great developments by the introduction of new organic channel materials and by improved fabrication [82]. In 1997, OTFTs with field-effect mobility as large as 1.5 $cm^2V^{-1}S^{-1}$ and on/off current ratio larger than 10^8, whose characteristics for the first time are all comparable to a-Si:H TFT were reported [83]. In 2000, pentacene TFTs exhibited a hole field-effect mobility of 3.2 $cm^2V^{-1}S^{-1}$ and an on/off ratio of $>10^9$ were demonstrated [84]. Figure.1-9 shows two common device structures adopted in current OTFTs [82].



(a) (b)

Figure.1-9 OTFT device configurations: (a) Top-contact device (b) Bottom-contact device

The left side is top-contact structure with source and drain electrodes evaporated onto the organic semiconducting layer through a mask. The right side is bottom-contact device, with the organic semiconductor deposited onto the gate insulator and the source and drain electrodes are prefabricated.

Besides, OTFTs using organic polymer materials can be fabricated by solution processing in reduced temperature [85], which allows a wide range of possibilities of low-temperature plastic substrates. Since the late 1990s, OTFTs and their circuits have been made on different flexible plastic substrates, including PI [86], PEN [17], PET [87][88], and on paper [89].

In most cases, flexibility and low cost of organic thin film transistors are the main concern. They can operate normally under bending condition of millimeter radius or even 100μm radius level [90]. Commonly used printing methods are already able to output a high print speed (~1m/s). However, the obvious shortcoming of OTFTs is their low carrier mobility and modest patterning resolution. Although different fabrication methods have been tried to reduce their channel length and ameliorate the architecture [91][92][93], the most excellent reported cut-off frequencies are still limited in the MHz range. Such confinement will be discussed in detail by the following section. (P.38)

1.4.3 Inorganic Thin Film Transistors

On the other hand, out of question, traditional silicon, carbon and III-V materials also contribute to flexible electronics field, showing the advantages of a highly mature technology. Conventional semiconductor techniques, like electron-beam and photo-lithography, enable the transistors to be realized in smaller feature size which is several orders of magnitudes lower

than that of printing techniques. Meanwhile, utilizing the channel materials of high carrier mobility property, inorganic-based devices render high-frequency flexible transistors possible.

1.4.3.1 Silicon-based Thin Film Transistors

In the early time, from the mid-1990s, thin film transistors using hydrogenated amorphous-Si (a-Si:H) materials have been made on different foil substrates, including polyimide films [13]and stainless steel foil [14]. However, in order to be adapted to low process temperatures of polymer substrates, the growth process of a-Si:H by plasma-enhanced chemical vapor deposition (PECVD) has been reduced from ~300ºC on glass to even as low as 75 ºC [94]. a-Si:H is a material with reproducible optoelectronic properties that provides n-channel TFTs devices with maximum electron field-effect mobilities of ~1 $cm^2V^{-1}s^{-1}$. Such extent of carrier mobility can be achieved by organic thin film transistors as well and limits their further applications.

Polycrystalline silicon (poly-Si) thin film transistors have become attractive materials in AM-OLED backplane application. They can be deposited by low-temperature chemical vapor deposition (CVD) or made by crystallization technique of amorphous-Si precursor film. Several techniques, such as solid-phase crystallization of high temperature furnace anneal [95], rapid-thermal anneal [96], metal-induced crystallization [97] and excimer laser annealing[98], have been widely used to crystallize a-Si into poly-Si, which achieves better surface quality of poly-Si than that obtained by CVD method. After a few poly-Si TFTs fabricated on steel foils have been reported in the late 1990s [99][100], researchers tried to realize them on different substrates. In 1997, poly-Si TFTs was first demonstrated on inexpensive plastic by excimer laser annealing [98]. Other high-performance large-grain poly-Si TFTs on glass substrate exhibiting 138 $cm^2V^{-1}s^{-1}$ and on/off current ratio of 10^8 have been achieved by short-pulse Flash-lamp annealing of amorphous-silicon.[101]

Synthesized by vapor liquid solid (VLS) technique, nanowires field-effect transistors (NW FETs) using both top and bottom gate structures on plastic films have also shown good flexible performances [42][45][102][43]. Two typical kinds of nanowire transistor structures based on organic substrate are shown schematically in Figure.1-10 (a) and (b). Note that such two geometries can be realized on the rigid substrates in the same way.

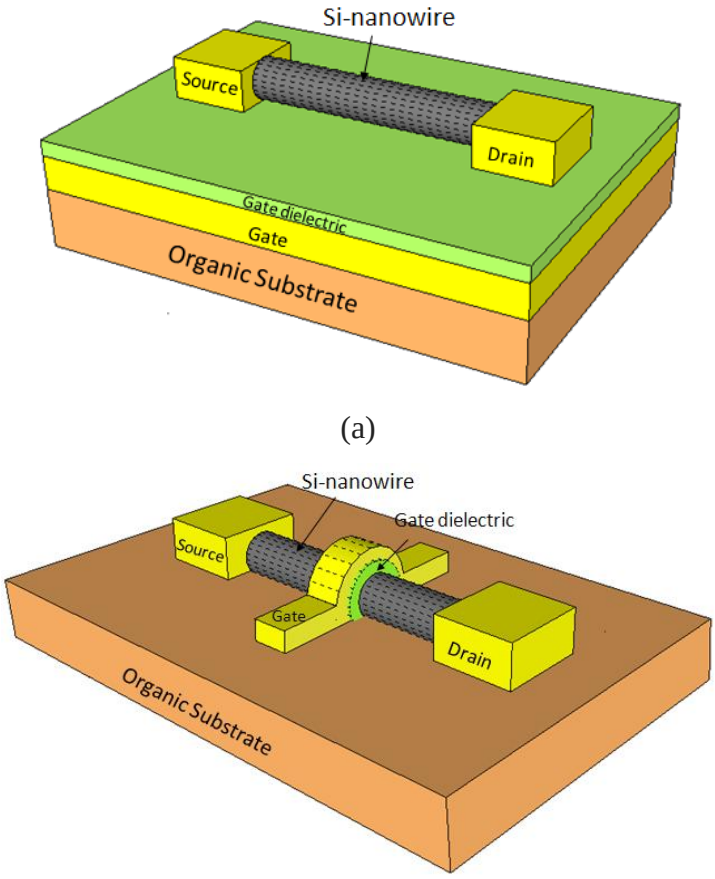


Figure.1-10 Silicon-based nanowire transistors on flexible organic substrate: (a) Single nanowire with bottom gate geometry (b) Single nanowire with top gate geometry [42]-[43]

Several NW TFTs with assembled silicon nanowires on a plastic film have been reported. They employed electrode patterning by conventional lithographic techniques [47] or nano-imprint process [103], p-type silicon nanowires were dispersed in solution and aligned on the gate electrode. Hole mobility of 3.7×10^{2} $cm^{2}\cdot V^{-1}s^{-1}$ has been demonstrated with a 10^{5} on/off ratio and the TFT also performed normally when it was bent a radius of curvature of 0.3 cm, showing a reliable bendability [47].

In the aspect of cut-off frequencies performances, Gigahertz range frequencies were reached by using silicon nanomembrane [65][64]. Those flexible TFTs adopted similar lithographic patterning process on Silicon-On-Insulator (SOI) wafers and subsequent buried oxide etching before direct transfer onto plastic substrates. High frequency response characteristics (cut-off frequencies of f_T=1.9 GHz and f_{MAX}=3.1 GHz [64]; f_T=2.04 GHz and f_{MAX}=7.8 GHz [65]) have been demonstrated. The better performance is due to improved two-finger gate layout and minimized access resistances [65]. With such improvement guidelines, recently, cut-off frequencies increase to f_T=3.8 GHz and f_{MAX}=12 GHz [63]. Meanwhile, these transistors

exhibit constant radio-frequency behavior after bending test of tensile strain (R=29mm) and compressive strain (R=78mm).

1.4.3.2 Carbon-based Thin Film transistors

Carbon nanotube (CNT) materials have been paid much attention owing to their excellent aspect ratio and mechanical flexibility, showing great promises as an active carrier transport channel in making high-speed flexible field-effect transistors. The field-effect mobility of FETs based on single CNT was ultrahigh (~79000 $cm^2 \cdot V^{-1}s^{-1}$)[104]. In this context, flexible CNT-based transistors are able to achieve high frequency operation. Nevertheless, conventional CNTs were grown by chemical vapor deposition (CVD), which represents an obstacle to fabricate these electronic devices on flexible substrate because most flexible substrate materials are unable to compatible with the extremely high temperature of CVD growth method (>900℃) [104]. Ink-jet printing technique can reduce the CNT fabrication temperature to room temperature, which makes CNT transistors on flexible substrate possible. Besides, such ink-jet printing enables mass fabrication of large-area electronic circuits on different flexible material in cost-effective way.

Classical structures of such flexible TFTs are given in Figure. 1-11. Note that both top-gate and bottom-gate geometries can be applied on rigid substrate. Several high performance thin film transistors (TFTs) based on carbon nanotube (CNT) have been reported [105]. TFTs with 4μm top-gate length showing a calculated mobility 47662 $cm^2 \cdot V^{-1}s^{-1}$ and > 150 MHz frequency operation have been demonstrated on flexible foils [106]. Ink-jet printing solution is also capable of integrating high-density CNTs. More than 1000 CNTs per μm^2 have been deposited by dispensing a very small droplet of an electronic-grade CNT solution. These printable CNT-TFTs on plastic transparency substrate exhibited a relatively high-speed modulation of 312MHz, but on/off ratio of 1.4 was extremely poor [107]. The trade-off between mobility and on/off ratio have been researched for various CNT-based ink [108]. It is possible to obtain higher carrier mobility for a given on/off ratio value by improving the purity of nanotube ink.

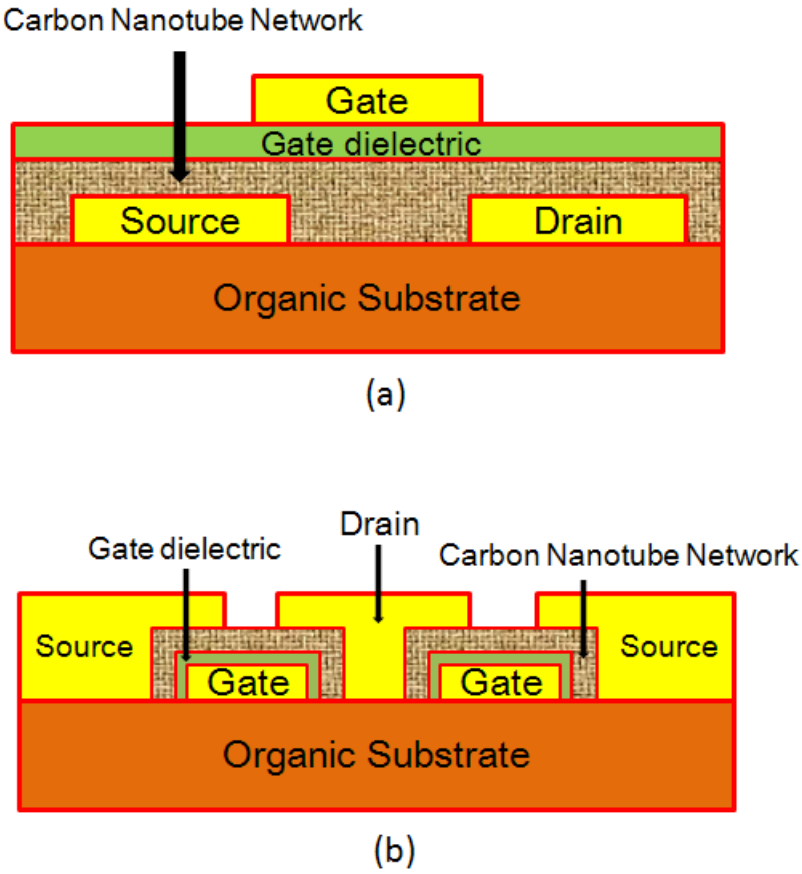


Figure.1-11: (a) top-gate [105]-[106]; (b) bottom-gate (two gate fingers) [57] thin film transistor based on carbon nanotube on organic film

For the bottom-gate example, 4-μm channel length flexible TFT was realized by solution process, atomic layer deposition (ALD) and conventional e-beam/photo-lithography, achieving a cut-off frequency of 170MHz and maximum oscillation frequency of 118MHz [57]. Gigahertz range operating frequency of CNT-TFTs was reached by all-ink-jet-printed process [105]. The source and drain electrodes were previously printed on polyimide substrate using silver nano-ink. Then, the ultra-pure, high density (> 1000 CNTs/μm^2) aligned CNT structure was printed for several times in order to form a well-distributed layer. On top of the CNT films, a thin layer of ion gel was printed as the gate dielectric. In the last step, the gate electrode was patterned by printing a conducting polymer layer. The resulting TFT output a high ON current 221 μA of and on/off ratio of 138 with an operation frequency of 5 GHz [105]. Recently, higher frequency f_T (~8GHz) was obtained in single walled CNTs which defined by dielectrophoresis (DEP).

Graphene is a material composed of pure carbon atoms arranged in regular hexagonal lattice while possessing high mobility and high bendability properties in the same time. The flexible graphene field-effect transistor fabricated on polyimide substrate has been exhibited total good function state when even at the bending raidus of 1.3mm[109]. The extracted electron

and hole mobility were 1015 $cm^2 \cdot V^{-1}s^{-1}$ and 460 $cm^2 \cdot V^{-1}s^{-1}$. Recently, flexible transistors derived from solution-based graphene featuring f_T = 8.7 GHz and f_{MAX} =550 MHz have been reported [110]. Moreover, the device keeps stable high frequency performance when bent down to a curvature of radius 12.5mm.

1.4.3.3 Potential of III-V-based device performances

In this part, our preferred choice of III-V semiconductor material is introduced. Their promising advantages and excellent performances have been confirmed by both existing rigid and flexible high electron mobility transistor (HEMT) devices.

1.4.3.3.1 III-V materials

Nowadays, the group of III-V semiconductor materials provides a broad series of researches in advanced epitaxial heterostructures and nanostructures due to their attractive properties. The III-V materials are formed from elements in columns III-A and V-A of the periodic table. Table 1-3 contains an extract of these classifications. The top numbers and bottom numbers indicate the atomic number and atomic mass, respectively.

Table 1-3 Extract of III-V classifications in periodic table

III.A	IV.A	V.A
$^{5}B_{10.8}$	$^{6}C_{12.01}$	$^{7}N_{14.01}$
$^{13}Al_{27.0}$	$^{14}S_{28.1}$	$^{15}P_{31.0}$
$^{31}Ga_{69.7}$	$^{32}Ge_{72.6}$	$^{33}As_{74.9}$
$^{49}In_{114.8}$	$^{50}Sn_{118.7}$	$^{51}Sb_{121.8}$

These binary, ternary and quaternary alloys in III-V materials are formed by partial substitution of an element by an element in the same column. We know, for example, the alloys such as AlGaAs, InGaAs, InAlAs or AlGaN type. Owing to MOCVD (Metal-organic chemical vapor deposition) and MBE (Molecular beam epitaxy) techniques, we are able to realize heterostructure (InAlAS/InGaAs, GaN/AlGaN and GaAs/AlGaAs) for mobility increase by combining these epitaxial materials whose lattice parameters are not too much different.

Table 1-4 Basic physical parameters of Silicon and III-V materials

Parameter	Si	$In_{0.75}Ga_{0.25}As$	$In_{0.53}Ga_{0.47}As$	InAs
Effective mass electron	$0.19m_0$	$0.032m_0$	$0.041m_0$	$0.023m_0$
Effective mass hole	$0.49m_0$	$0.435m_0$	$0.45m_0$	$0.41m_0$
Band gap (eV)	1.12	0.544	0.74	0.35
Bulk electron mobility ($cm^2V^{-1}S^{-1}$)	$\leq 1.4\times10^3$	$<2.29\times10^4$	$< 1.2\times10^4$	$\leq4\times10^4$
Bulk hole mobility ($cm^2V^{-1}S^{-1}$)	≤ 450	300~400	< 300	500
Electron thermal velocity (m/s)	2.3×10^5	6.3875×10^5	5.5×10^5	7.7×10^5
Hole thermal velocity (m/s)	1.65×10^5	$(1.8\sim2)\times10^5$	2×10^5	2×10^5

Considering their excellent transport properties, we choose our active layers based on III-V material in our HEMT device. As shown in Table 1-4, $In_{0.53}Ga_{0.47}As$ possesses the bulk electron mobility of 1.2×10^4 $cm^2V^{-1}S^{-1}$. Its value is 8 times higher than that of the Silicon, which allows faster operation. And the electron thermal velocity of $In_{0.53}Ga_{0.47}As$ is 5.5×10^5m/s, which is 2 times faster than that of the Silicon material.

Moreover, with the increase of indium content, InGaAs tends to exhibit both higher electron mobility and saturation velocity. Thus, the current I_{ON} is able to be raised by employing high rate indium in InGaAs.

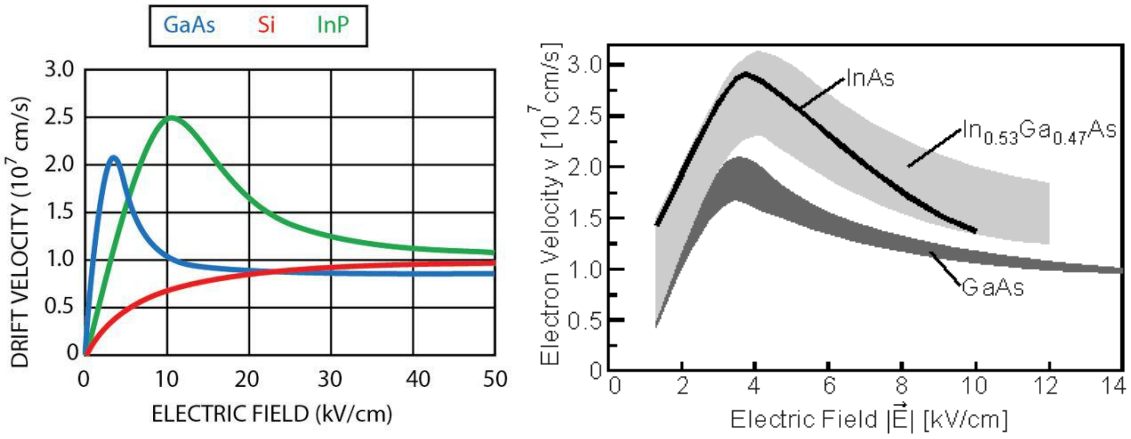


Figure.1-12 Electron velocity of Silicon and III-V as a function of electrical field [111]

Besides, in Figure.1-12, we demonstrate that the critical electric field of materials III-V is much smaller than that of silicon, which means less power supply V_{ds} enables transistors

based on III-V materials to obtain the saturation region. Although there are some other materials showing high mobilities such as graphene, the related fabrication techniques are still immature. More importantly, according to Figure.12, the III-V electrons velocity, both in the aspect of peak and saturation velocity are stronger than that of silicon. Thus, the materials III-V as $In_xGa_{1-x}As$ are the promising candidatures for keeping the high frequency performances and low power consumption simultaneously.

1.4.3.3.2 III-V-based rigid transistors

Outstanding transport properties of III-V compound semiconductors have shown their worth in many communication systems. Both III-V-based integrated circuit using high electron mobility transistors (HEMT) and heterojunction bipolar transistors (HBT) are well-known for high frequency electronic application [128]. Due to HEMT having better low-noise performance up to millimeter wave frequencies and simpler manufacturing approaches compared with those of HBT, we tend to use HEMT to realize our flexible devices of ultra-low power. HEMT is hetero-structure field-effect transistors (FET) which have been developed for high speed digital circuits. The principle is based on a hetero-junction which consists of at least two different semiconducting materials brought into intimate contact. Owing to the distinct band gaps and their relative alignment to each other, band discontinuities occur at the interface between the two semiconducting materials.

Figure.1-13 gives the typical structure of InP-substrate HEMT. T-shaped gate metal helps minimized the gate resistance by enlarging the cross section. The highly n-doped cap layer used to reduce contact resistance of the source and drain sides and protect the beneath sensitive InAlAs layer from oxidation. The Schottky-Barrier layer provides a Shottky contact between gate electrode and semiconductor materials, prevents too large currents from running

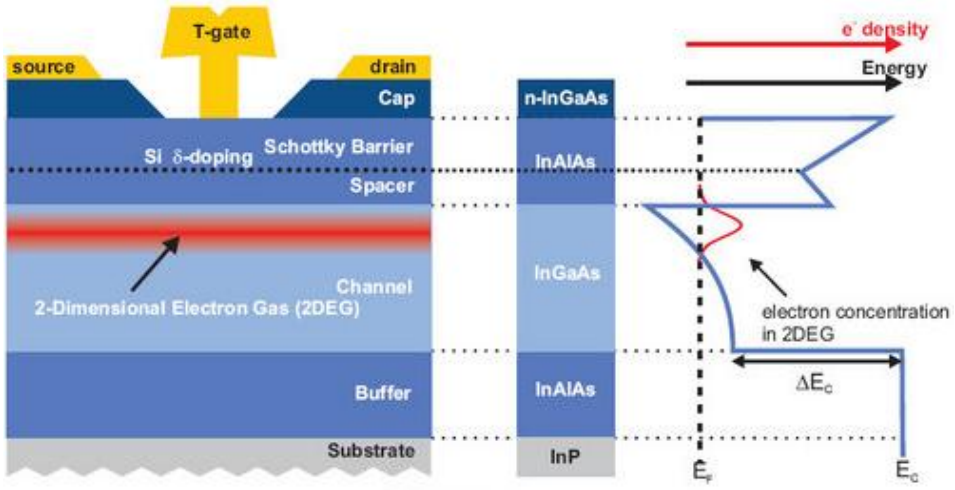


Figure.1-13 Typical InP HEMT structures

through the gate and limits tunneling to the channel as well. Silicon δ-doping layer which is highly doped layer with only few atomic layers thickness locates between the Schottky-Barrier and spacer layer, acting as a donor of charge carriers, providing electrons to the channel layer. The electrons occupying the lowest allowed energy state accumulate into the potential well and form a confined two-dimensional electron gas (*2DEG*) in the channel. Such high δ-doping layer provides high electron densities in the channel and therefore enables the transistors to achieve high transconductances, drain current and cut-off frequencies operation.

The spacer layer plays a role of the separation between the electrons and their positively charged Si-donors, reducing impurity scattering and hence enhancing electron mobility. The channel layer is the key to the device electrical performances. A two-dimensional electron gas inside InGaAs layer offers magnificent high carrier mobility properties (Table.1-4) at room temperature.

Figure.1-14 reports the excellent frequency performances of different transistors over the past years. From the pale yellow region highlighted, we observe that all frequencies higher than 600GHz are dominated by HEMT components which beat other kinds of field-effect transistors overwhelmingly [112]. The best performance of f_T and f_{MAX} is 710GHz [113] and 1.2 THz [114], respectively.

In such context, we believe that the flexible devices fabrication based on III-V HEMTs are one promising choice for large-area radio-frequency applications as well as high-speed processing ability in the future.

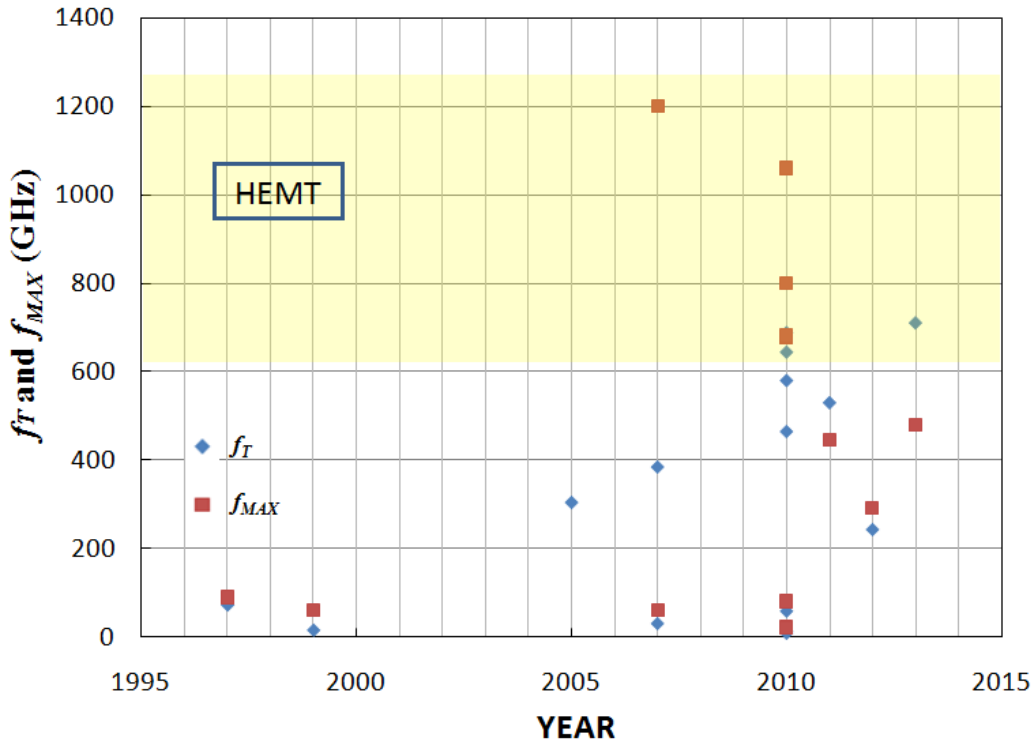


Figure.1-14 State of the art of f_T and f_{MAX} performances for existing excellent transistors

1.4.3.3.3 III-V-based flexible transistors

As a consequence of the above development, III-V compound semiconductors are commonly known as a most promising material for enhancing the performance of electronic devices in the future due to their high internal carrier mobility. Undoubtedly, such power can't be ignored in the flexible electronics developments. Most of excellent III-V flexible devices are made by transferring onto or fabricating directly on plastic substrate. The layer structure of our work also adopts this intriguing synthetic material, detailed in the next section.

Exhibiting high intrinsic electron mobility of 8500 $cm^2 \cdot V^{-1}s^{-1}$, arrays of single crystalline wires of GaAs were used for transport channels in metal-semiconductor field-effect transistors (MESFETs) on plastic substrate. GaAs wires can be transferred onto plastic substrates at low temperature [69]. GaAs wire-based TFTs featuring cut-off frequency f_T=1.55GHz indicate that their speed are acceptable for radio-frequency communication and other applications [70] . Moreover, their saturated currents were varied by less than 20% when the device was bent down to a curvature radius of 8mm.

Recently, indium phosphide (InP) based high electron mobility transistors (HEMTs) were transferred onto PEN substrates by a double-flip process including ion-cutting and adhesive bonding technique, characterizing high field-effect mobility (~2800 $cm^2 \cdot V^{-1}s^{-1}$) [115][38]. And in the wide band gap side, Hetero-structure HEMTs employing μs-GaN ribbons were transferred on plastic substrate. Very stable responses of static electrical characteristics were obtained for bending radii down to 1.1cm[116]

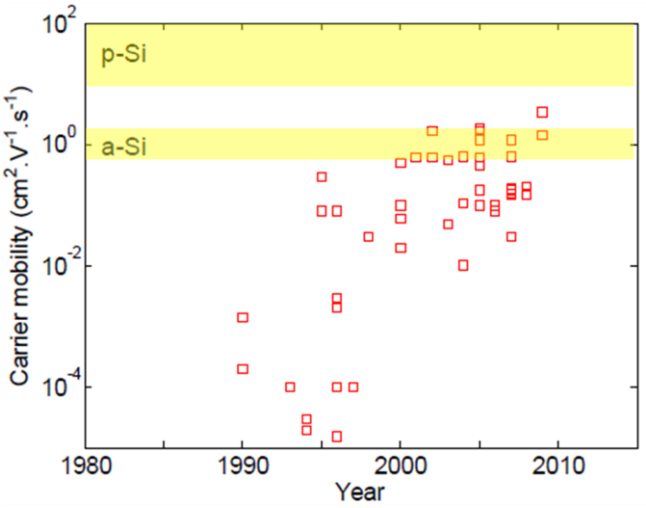
The work of InAs material also presents a new platform to fabricate high performance flexible transistors. High-mobility InAs nanowire firstly brings nanowire arrays transistors into GHz device operation. Cut-off frenquency of 1.08 GHz and maximum oscillation frequency of 1.8 GHz were demonstrated [56]. Up to now, the highest record of frequency for flexible transistors fabricated directly on mechanically bendable substrate reaches 105 GHz by using InAs micro-ribbons. The polyimide substrate of these InAs MOSFETs was previously spin-coated and cured on a silicon wafer. Then, InAs nanostructure was transferred onto polyimide by dry contact printing process [71].

1.5 Limitations of Existing Flexible Transistors and State of the Art

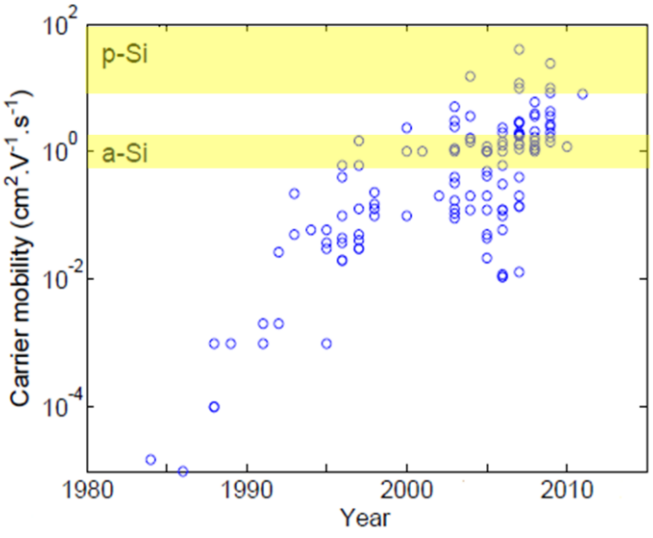
In this section, we will discuss the global limitation in current flexible transistor performances from several aspects, such as carrier mobility, current and operating frequencies parameters etc. State of the art of current gain cut-off frequencies f_T and maxium oscillation frequencies f_{MAX} is presented subsequently.

1.5.1 Limitations of existing flexible transistors family

Firstly, in organic semiconductor part, according to the sections described hereinbefore, we can conclude that the poor charge carrier mobilities are the obvious obstacles for all achieved organic semiconductor devices. Figure.1-15 presents the charge carrier mobilities of n-type and p-type organic-based components in the past several decades.



(a)



(b)

Figure.1-15: Carrier mobilities of (a) n-type and (b) p-type organic semiconductors in the past literature, compared with the carrier mobilites range of amorphous silicon (a-Si) and poly-crystalline silicon (p-Si). Data from [117][118][119]

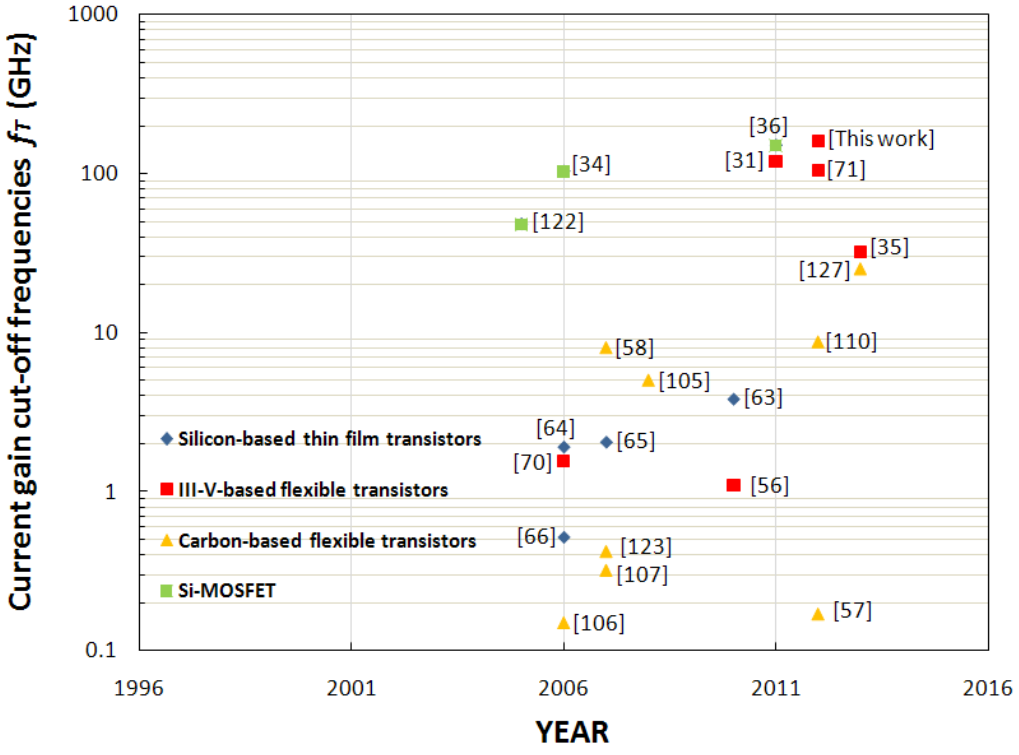
Most of organic semiconductors exhibit much lower mobilities in the comparison of inorganic semiconductors a-Si and poly-Si from the illustration above (yellow part). Even if the mobility of n-type organic semiconductors have achieved the level of a-Si and p-type organic semiconductors are almost competitive with poly-Si at present, the relatively low mobilities around 100 $cm^2V^{-1}S^{-1}$ still limit the organic transistors in terms of high frequency electronic applications.

Secondly, on the inorganic semiconductor side, the mobility of existing silicon-based flexible transistors is too low for achieving high frequency performances as well. To our knowledge, up to now, the highest mobility reported from silicon-based thin film transistor possesses only the effective mobility of ~500 $cm^2V^{-1}S^{-1}$ [66]. In another hand, although better high mobility solutions (>10^3 $cm^2V^{-1}S^{-1}$) have been demonstrated in single nanowire transistors, their intolerably low ON currents arised from limited nanowire diameter hinder the performance. The current of per wire is in the order of 10 to 100μA. [42][46][120] [121][122]. Despite the widespread attention to the excellent mobility of graphene material over the past decade, high frequency performances of graphene FET on flexible substrates have been barely achieved. The best fabricated device affords a cut-off frequency of 25GHz [127].

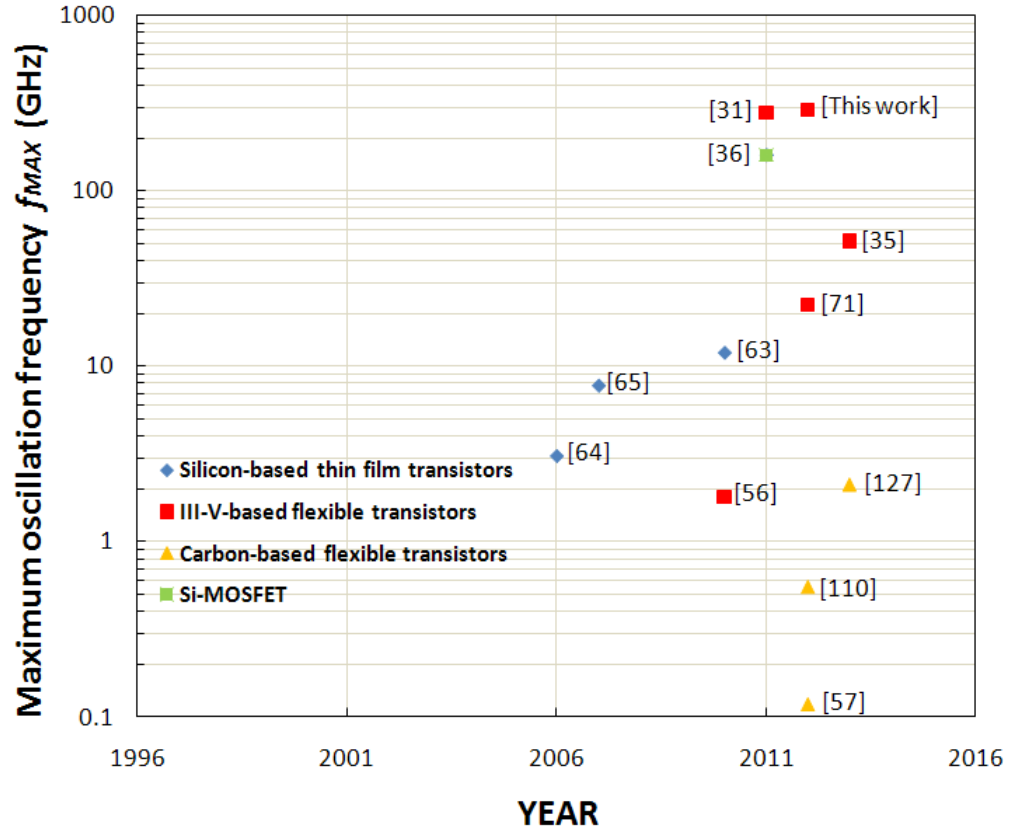
Moreover, in the aspect of fabrication technique, the modest patterning resolutions for printed electronics are incapable of competing with traditional processing ways, showing in Table. 1. Nanometer scale achieved by photo- or e-beam lithography methods can enable transistors to reach higher frequencies than devices realized by printed devices whose resolution of order of magnitude is micrometer. Even if numerous works have adopted conventional semiconductor methods, the direct fabrications flow path performed on the organic substrates risked the misalignement resulting from the deformed flexible substrate in high temperature [63][65][64].

1.5.2 State of the art

In light of several points mentioned in above paragraphs and targeted application market demand, the main focus is to combine high electrical device performances with mechanical flexibility. Our scope of this work is also the realization of high frequency flexible transistors with ultra-low power consumption. The following charts show the progresses in terms of cut-off frequencies performance (f_T and f_{MAX}) of recent flexible transistors. [123][124]



(a)



(b)

Figure.1-16 (a) Current gain cut-off frequency of recent flexible transistors as a function of time ; (b) Maximum oscillation frequency of recent flexible transistors as a function of time.

The III-V-based transistors and Si-MOSFETs occupy all highest frequency performances classes in the above publication summaries. Up to now, the highest f_T and f_{MAX} is 160GHz and 290GHz [125], respectively. On the contrary, silicon-based and carbon-based thin film devices haven't shown strong competitiveness in this field. Organic field effect transistors (OFET) are not listed in those two states of the art because of their extremely low frequency values. To our knowledge, the highest frequency of OFET still stops in MHz range (28MHz) [126].

It should be pointed out that those flexible electronics reaching 100GHz range (both f_T and f_{MAX}) have been fabricated conventionally on rigid semiconductor wafers before the transfer process on organic substrates. Such data enhances the potential of transfer technique.

1.6 Conclusion and Objectives

In the first chapter, the growing interest in the domain of flexible electronics has been demonstrated over the past years. Various hot applications for flexible devices were presented. In terms of the flexible electronics study, several main fabrication strategies focusing on combination of high electrical performance and mechanical flexibility property were described and compared. In the aspect of backplane technology, with the increase of market demand, organic electronics and thin film devices of inorganic electronics such as silicon-based, III-V-based, carbon-based transistors are counted on too much in future bendable devices and circuits. Their advantages and drawbacks were pointed out subsequently.

In addition, this chapter discussed several confinements in existing technologies and summarized the up-to-date charts for high frequency performances on the field of flexible transistors, including our own works. After comparing with other techniques and transistors in the literatures, we conclude that current flexible electronics could benefit from the mature conventional technologies systems and the strong electrical performances on rigid substrates. Transferring those attractive performances from rigid carrier to elastic support will pave a highly promising way to flexible large-area radio-frequency communication devices and high-speed processing units.

Thus, learning from all these preceding experiences, we propose a reliable technique to maximize the benefit of existing high performance transistors. We decide our promising device structures based on III-V materials with transfer-and-bond fabrication scheme to integrate high-frequency communication systems and high-speed applications onto flexible substrate. Our main objective is to add the value of flexibility to mm- and sub-mm-waves applications with ultra low power consumption technology for autonomous electronics.

In the next chapter, the fabrication process and technique details of transferring our selected high potential HEMT devices from the initial rigid III-V wafer onto the flexible plastic substrate will be enunciated.

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CHAPTER II

Fabrication and Characterization of Transistor HEMT on the Flexible Substrate (HEMT-FS)

Chapter 2: Fabrication and Characterization of Transistor HEMT on the Flexible Substrate (HEMT-FS)

2.1 Introduction

In this chapter, we will describe the details in total fabrication of our flexible HEMT components, including our standard high electron mobility transistors and transfer processing techniques.

The initial epitaxial layer structure of our HEMT-FS is presented and explained at the first time. By the schematization of HEMT transistors manufacture on flexible substrate, we are able to point out that the technologies of HEMT-FS consist of four main parts:

First of all, the standard HEMT on rigid substrate should be done through conventional fabrication methods which are identical to those of rigid HEMT benchmark (used subsequently in comparison of electrical performances). These works can benefit the profound experiences and reference data in IEMN laboratory.

Then, the realization of thin film micro-strip (TFMS) access lines by using BCB (***B***enzo***C***yclo***B***utene) polymer will be presented.

Afterwards, we will put forward the adhesive bonding process which acts on transferring the fabricated devices onto the selected flexible substrate. The whole technology will be elaborated step by step.

Finally, we will describe the substrate removal by immersing the sample in chemical solution. The mechanical bendability of our products will be shown obviously.

Both static and dynamic electrical characterizations of HEMT-FS will be analyzed, comparing with the transistor fabricated previously on rigid substrate.

2.2 Initial Epitaxial Layer Structure

Figure 2-1 shows the cross section of layer structures for our proposed device. This 2 inch initial wafer is before the bonding process on the flexible substrate. With the technique support of group EPIPHY in IEMN laboratory, lattice-matched InAlAs-InGaAs HEMT epitaxial layers have been grown on an InP substrate by a solid source molecular beam epitaxy (MBE). Active layer is composed of three parts. From top to bottom, the first part corresponds to a typical HEMT structure: an N^+ InGaAs cap layer ($6\times10^{18}cm^{-3}$), an InAlAs barrier, a Silicon δ-doping plane, an InAlAs spacer, an InGaAs channel and an InAlAs buffer layer. We tend to adopt $In_{0.53}Ga_{0.47}As$ as channel material because this material is able to provide a fabulous compromise between high electron mobility and intermediate band gap. The narrower band gap tends to cause the inter-band tunneling effect. In addition, the density of states will be less favorable to control charge in the case of a smaller band gap.

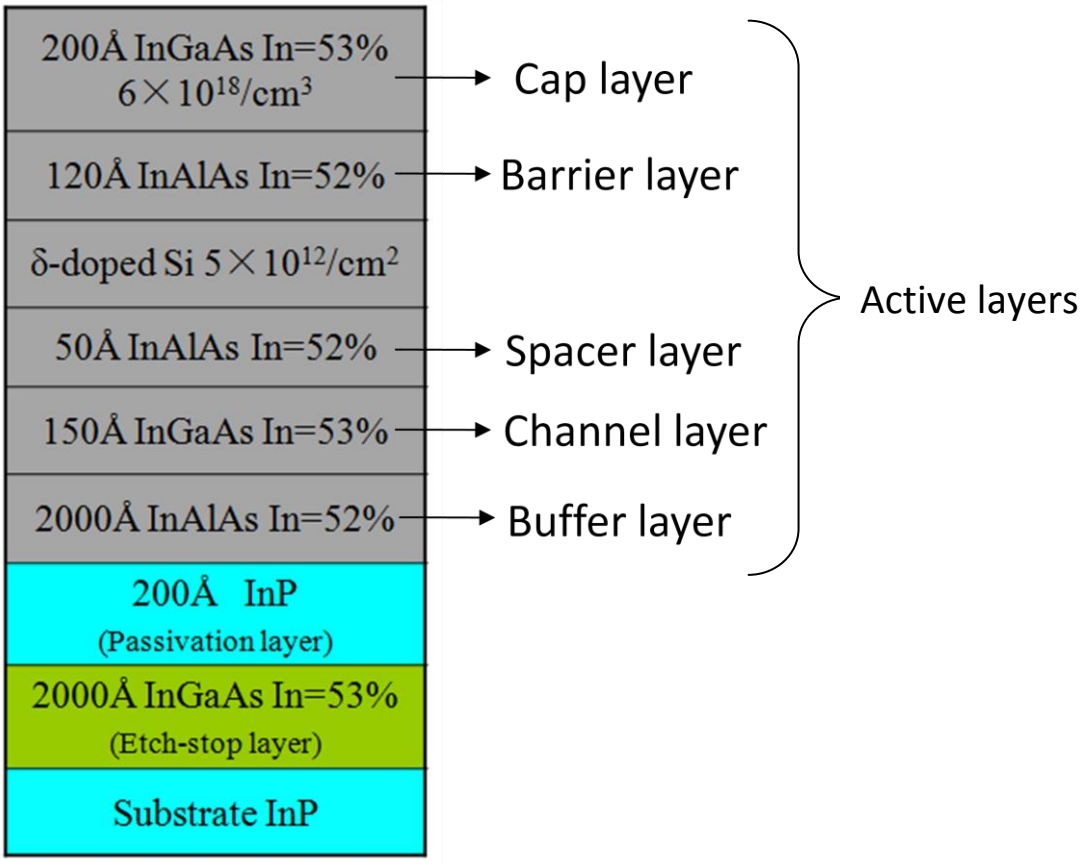


Figure 2-1: The epitaxial layer structures of our HEMT devices

The second part corresponds to a passivation layer (InP, 20 nm) which is used to prevent carrier depletion of the active layer induced by the Fermi level pinning at the surface. In fact,

during HEMT-FS fabrication, the epitaxial structure is upside-down, as a result, InP passivation layer is exposed to the air at the end device technology fabrication.
The last part of epitaxial layers is the etch-stop layer (InGaAs, 200nm) which facilitates the transfer process onto flexible substrate and is etched during last step of device fabrication.

2.3 Schematization of Fabrication Process

As declared in the objective of our work, rigid HEMTs should be, at first, fabricated on III-V wafer before transfer bonding onto flexible substrate. Acquired research experience of those conventional fabrication technologies can be benefited from our group *ANODE*.
The chronological flow charts for different main steps concerning the whole HEMT-FS fabrication are presented in Figure 2-2 and Figure 2-3 separately. Figure 2-2 shows the traditional HEMT fabrication on the rigid wafer and Figure 2-3 shows our transfer processing whose adhesive bonding technique makes the active layers of our HEMT components upside down on the flexible substrate.
We conclude the following schematic flow into 7 main steps:

1. The realization of ohmic contact
2. Mesa isolation
3. Bonding pads deposition
4. Gate realization
5. Thin film micro-strip (TFMS) access lines fabrication
6. Transfer bonding technique [1]
7. InP substrate and etch-stop layer removal [2]

All fabrication processes (1-4) described in the Figure 2-2 are the same as those of traditional transistor HEMT devices, including ohmic contacts, mesa isolation, bonding pads and gate realization.

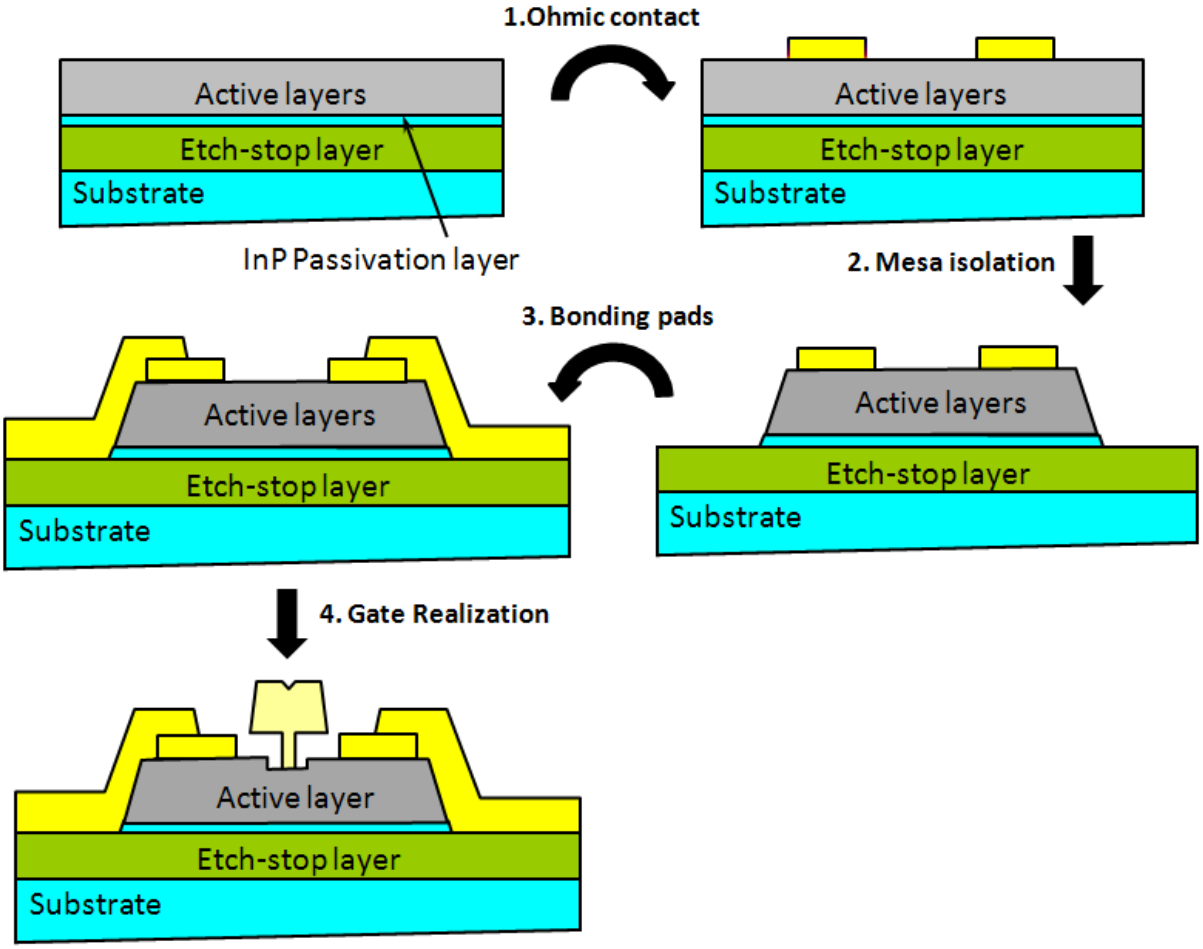


Figure 2-2: The schematic flow of standard HEMT fabrication on rigid III-V wafer

After finishing the gate realization, we set up the core technology of our transfer bonding process with the fabricated HEMTs on rigid wafer. At this moment, it should be pointed out that all the ready HEMT devices were not isolated between them on the wafer because of the conductive etch-stop layer InGaAs. Therefore, their electrical characterizations cannot be performed before we transferred them onto flexible substrate.

Figure 2-3 unfolds the subsequent important procedures (5-7). Step.5 corresponds to TFMS access line fabrication by BCB polymer definition. Step.6 illustrates the transfer and bonding technology which is decisive process in the flexible device fabrication. Step.7 is the last but not the least. The removal of etch-stop layer and InP substrate accomplishes the back-side contact for the following measurements.

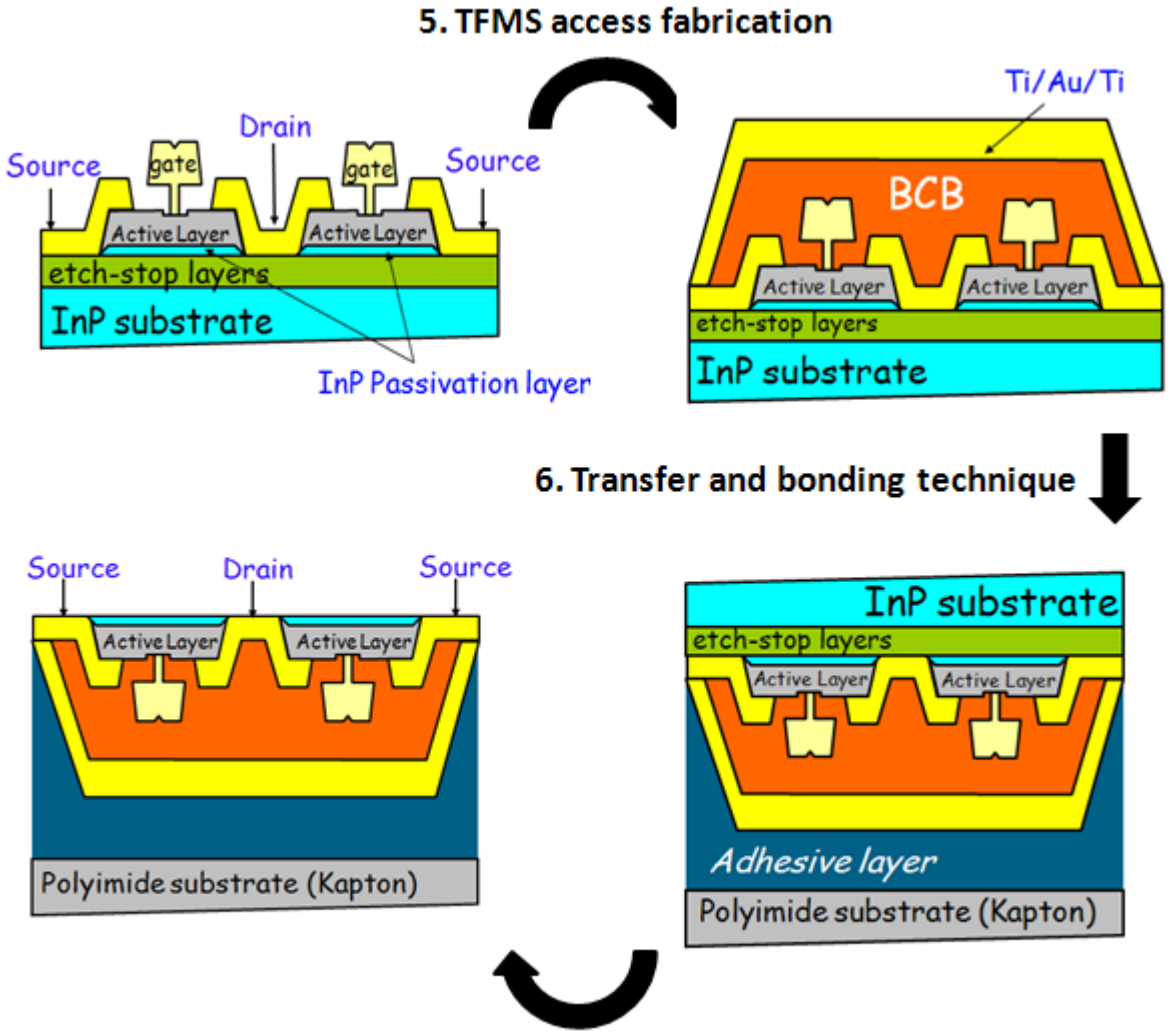


Figure 2-3: The schematic flow of standard HEMT fabrication on rigid III-V wafer

2.4 Basic Fabrication Technologies of HEMT

The fabrication technology of lattice-matched HEMT on InP substrate have been researched for a long time [3][4]. This part will present a series of details in fabrication rigid HEMT on III-V wafer from beginning to end, including mask design work, metal deposition for ohmic contacts, mesa isolation, bonding pads and gate recess realization.

2.4.1 The mask description: springy2011

The mask 'springy2011' has been designed in order to test different HEMT topologies and device widths. We used this conception for estimating the optimal result according to their electrical characterizations on flexible substrate. Figure 2-4 shows the whole view of mask used in our work. It is composed of:

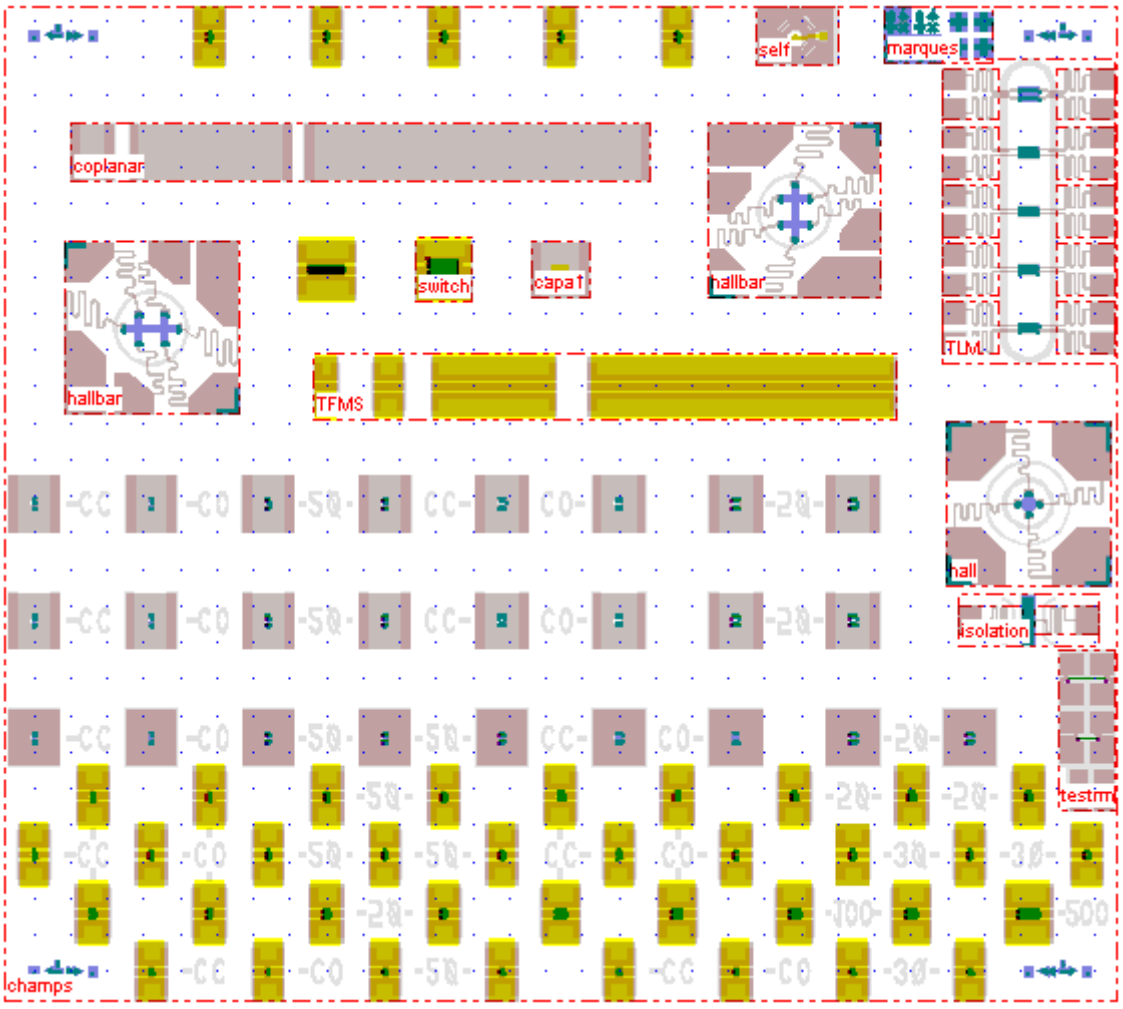


Figure 2-4: Representation of the mask 'springy2011'

- The Hall bars and Hall effects are used for property measurements of carrier concentration and electron mobility in active layers.
- The standard TLM (Transmission Line Method) is used for contact resistance and sheet resistance measurements.

Considering the mechanical deformation of our flexible substrate in the later measurement platform, we elaborate the winding metal wires for connecting bonding pads.

- The 'CO' and 'CC' patterns respectively correspond to 'open' and 'short' structures as RF passive components, which are used to realize the de-embedding methodology from the measured S-parameter of flexible transistors.
- As for the transistors HEMTs with correct TFMS access lines, different dimensions have been drawn on the mask:
    - 9 transistors with device width (*W*) 2×10µm
    - 5 transistors with device width (*W*) 2×15µm
    - 3 transistors with device width (*W*) 2×25µm
    - 3 transistors with device width (*W*) 2×25µm
    - 2 transistors with device width (*W*) 2×50µm
    - 1 transistors with device width (*W*) 2×100µm

Note that all HEMT components possess 100nm gate length. We also prepare some transistors (above the yellow ones) with various definition of BCB shape in order to test the different BCB coverage conditions on the metal bonding pads.

2.4.2 Ohmic contact

Good quality of source and drain ohmic contact is essential for achieving high cut-off frequency during the fabrication process [5]. Indeed, it is these elements that establish relations with the intrinsic part of our components. Thus, obtaining contact resistance *Rc* as low as possible is necessary to reduce source resistance *Rs* and drain resistance *Rd* of our HEMT devices. The *Rd* reduction can shorten the charging rate of parasite capacitance *Cgs* and *Cgd*. On the side of *Rs*, it has effect on reducing the value difference between intrinsic (Gm_{INT}) and extrinsic trans-conductance (Gm_{EXT}).

Besides, we should precisely define the source-drain distance L_{SD} between two ohmic contacts along all device width *W*. Bad metal definition causes some L_{SD} reduction places (not uniform), which leads to higher electric field between source and drain. Intense electric field tends to increase the risk of precocious breakdown of our transistors.

Numerous studies on optimizing ohmic contact metallization of arsenic-based FET have been reported[6][7]. In general, the sequence of metallization is composed of:

1. The first metallic layer is used to improve the adherence between subsequent metallization and semi-conductor surface.
2. The second part has doping species which allow itself to diffuse and integrate into semi-conductor material during rapid thermal anneal (RTA) processing. Then, extremely-doped zone will be realized under the contacts.
3. The last layer is prepared for external system connection by welding gold wires on it, thus, this layer oftentimes consists of gold.

Herein, benefited from previous experiments experience in our laboratory, the ohmic contacts are realized using Ni(25Å)/Ge(400Å)/Au(800Å)/Ni(50Å)/Au(600Å) metallization. We use nickel as metallization adherence on the InGaAs cap layer (Figure 2-1). Ge/Au layer is doping species (Ge: N-type doping). The second nickel layer is a barrier for avoiding diffusion of above gold layer and can improve the contact morphology as well.

In order to obtain precise definition of these ohmic contacts, electron beams (e-beam) lithography by electronic mask is preferred. Figure 2-5 shows the photo of contacts observed by scanning electron microscopy (SEM). L_{SD} uniformity is achieved perfectly.

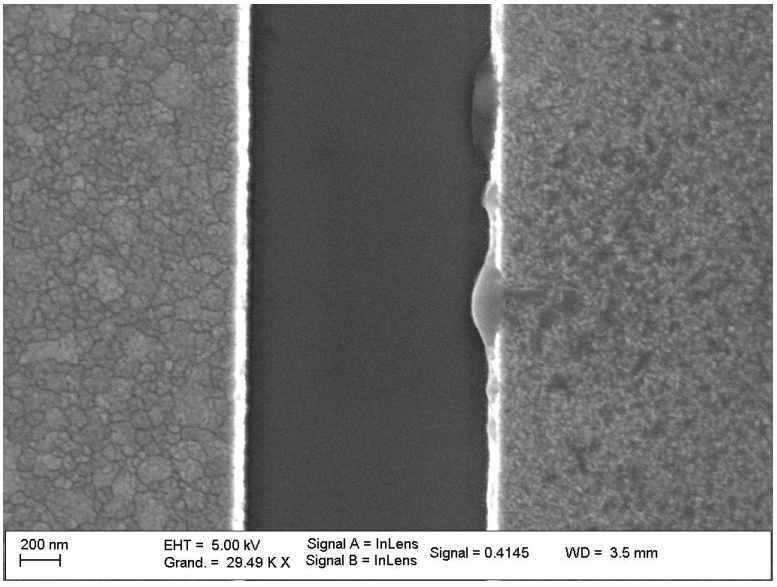


Figure 2-5: Ni/Ge/Au/Ni/Au contact morphology after RTA process

Bilayer resists deposition of co-polymer P(MMA-8.5%MAA)13% and PMMA in the order can form the cap profile which facilitates the subsequent lift-off after e-beam lithography. All metallization process is deposited by electron-gun evaporation in vacuum ambiance. After

lift-off done in acetone and rinse by alcohol, RTA is done at 295 ℃ during 20 seconds within a N_2H_2 ambiance for doping species diffusion in cap layer..

2.4.3 Mesa isolation

Individual components fabricated on the same substrate need to have electrical isolation from each other in order to test their electrical functions. In our work, we adopt wet etching methods by chemical solution to realize the isolation of our component HEMTs.

The thickness of our etching is about 2720Å (Figure 2-1), including active layers and passivation layer. The wet etching is stopped on the interface between InP passivation layer and InGaAs etch-stop layer, showing in the Figure 2-6.

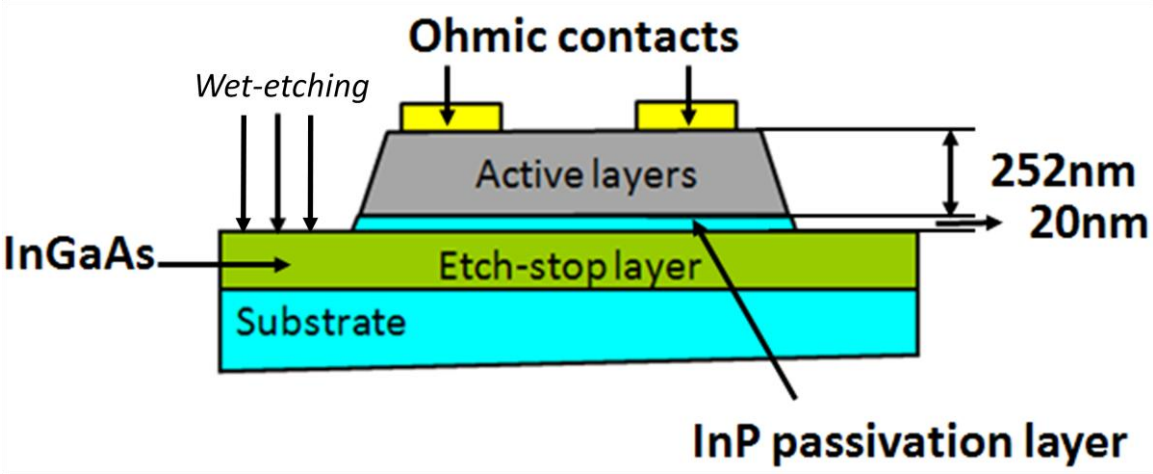


Figure 2-6: Schematic drawing of mesa isolation

The wet etching boundary is defined by optical lithography because the requirement for active zone positioning is micrometer level. The chemical solution of our mesa isolation is composed of orthophosphoric acid (H_3PO_4), hydrogen peroxide (H_2O_2) and EDI water (H_2O) with the rate of 5:1:40. The highly reproducible rate of such wet etching depends on the temperature of solution. The depth of wet etching is linear with time.

After wet etching for InGaAs/InAlAs active layers at the rate of 160nm/min, we execute the wet etching for InP passivation layer immediately by immersing the wafer in prepared hydrochloric acid (HCL) and water mixure by the proportion 2:1. At last, we wash it in electrodeionization (EDI) water.

Due to the conductive InGaAs etch-stop layer, we cannot test the isolation result between each component at this moment.

2.4.4 Bonding pads

Bonding pads is a metalized area on the surface of wafer, enlarging contact zone. After finishing mesa isolation, we deposit bonding pads before the gate realization. The bonding pads are made up by Ti(250Å)/Au(3500Å)/Ti(250Å) metallization. The titanium layer enhances the adherence of deposited metal to semiconductor surface and following BCB polymer.

The same bilayer resists menu as ohmic contacts lithography is put forward with a little adjustment of thickness. The detailed parameters are noted in Appendix. Figure 2-7 shows the first deposition result of our metallic bonding pads by SEM observation.

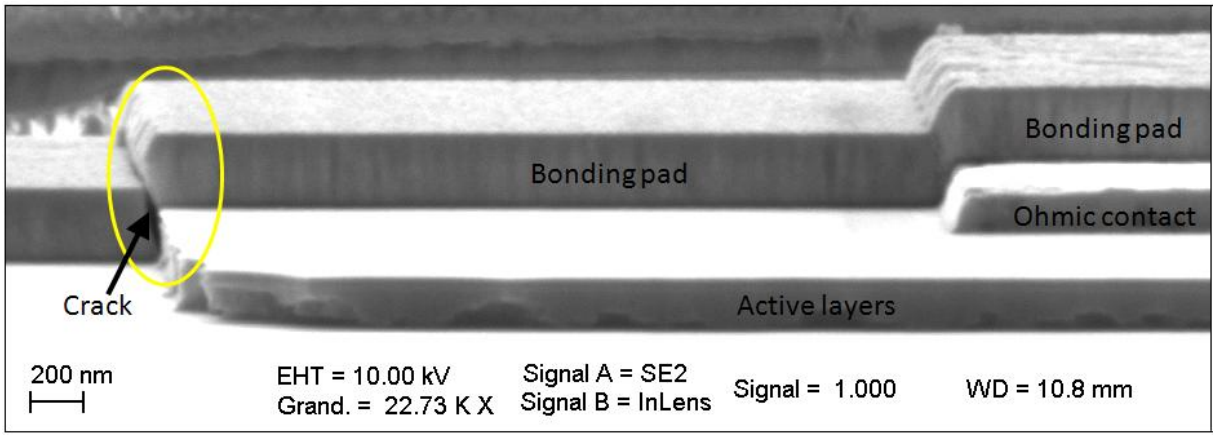


Figure 2-7: Photo of the first bonding pads deposition

Due to excessively steep profile of active layers caused by component isolation process, an obvious crack on the border of active layers is demonstrated. Such unfavorable deposition probably leads to open circuit or extremely high connecting resistance.

We consider mending the crack by adding another metallization. After supplementing a layout in the mask, the second Ti(250Å)/Au(1500Å)/Ti(250Å) metallization is deposited on the previous bonding pads under same condition.

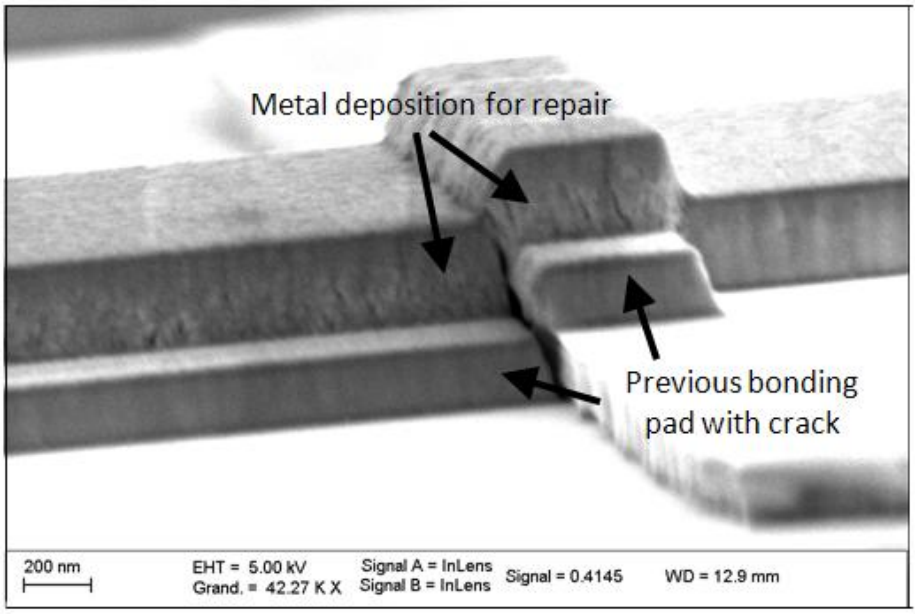


Figure 2-8: Photo of repaired bonding pads connection

From Figure 2-8, the added metal deposition exactly enveloped the previous bonding pad, which repairs the connection crack finely.

2.4.5 T-shaped Gate realization

2.4.5.1 Gate lithography scheme

In order to realize a metallic T-shaped gate for reducing the gate resistance R_G, the gate lithography consists of electro-sensitive bilayer with different thicknesses [8]. As shown in Figure 2-9, we tend to obtain the T profile by just once exposing and developing process.

The resists used for this turn are:

1. PMMA 950K (1500Å), baked in 170°C for 30 minutes
2. P(MMA-8.5%MAA)13% (6600Å), baked in 170°C for 30 minutes

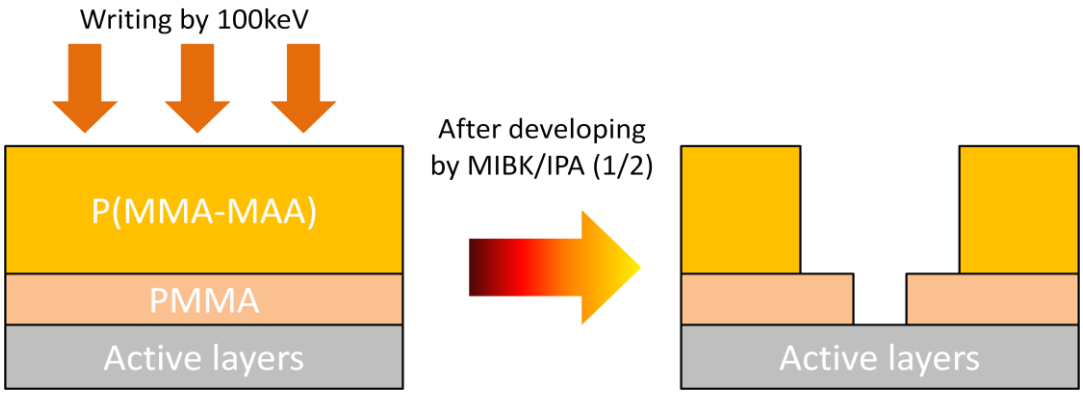


Figure 2-9: Bilayer process illustration for forming T profile resist

Contrary to the resist deposition for ohmic contacts, this technique uses the resist PMMA which is less sensible as the first layer. The bottom of gate is defined in the resist PMMA and gate cap is defined in the resist P(MMA-MAA). Note that before the resist deposition, we spin an adhesion promoter HMDS (Hexamethyldilsilazane) onto the wafer in order to strengthen the adherence between the semiconductor and PMMA. This promoter doesn't influence any parameters in the subsequent lithography process.

Besides, in order to obtain the above mentioned shape of metallic gate, well-designed mask is also necessary. Figure 2-10 gives the writing field of 100keV high energy for our gate part. It is made up by five differently dosed zones:

1. One heavily-dosed zone in the middle define the gate foot
2. Two zones are dosed moderately for supporting gate cap (*Laterals*)
3. Two zones are dosed slightly for forming a better gate foot definition (*Spacers*)

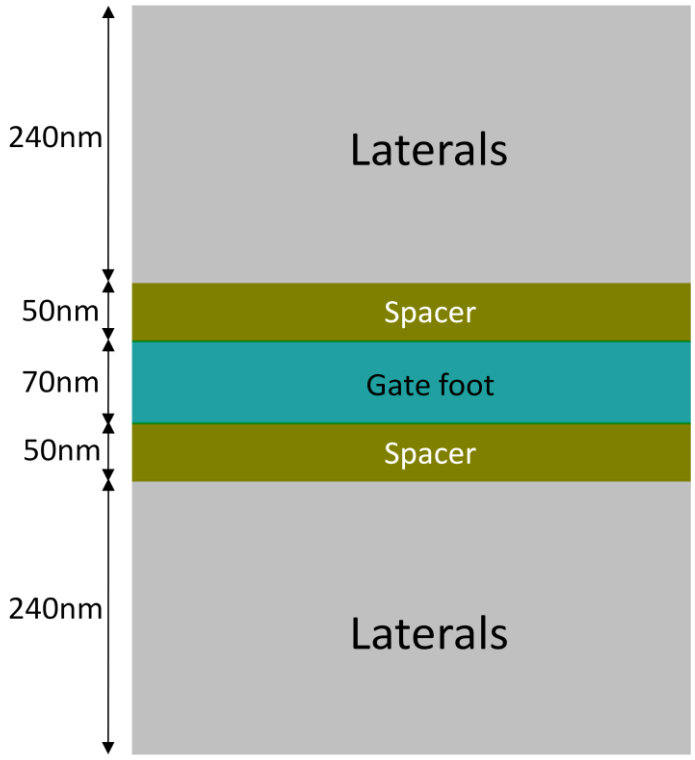


Figure 2-10: Designed mask for our 100nm gate length

The details of dose data are presented in the eventual appendix. Note that, from the above mask, writing on 70nm gate foot leads to a 100nm metallic gate. This heavily-dosed region is for the purpose of precise gate foot definition along all width of transistor, ensuring extremely clean place for subsequent gate recess step. Figure 2-11 exhibits the photo after writing and developing for 100nm gate. There is no resist on the gate foot and the opening of gate foot is defined outstandingly.

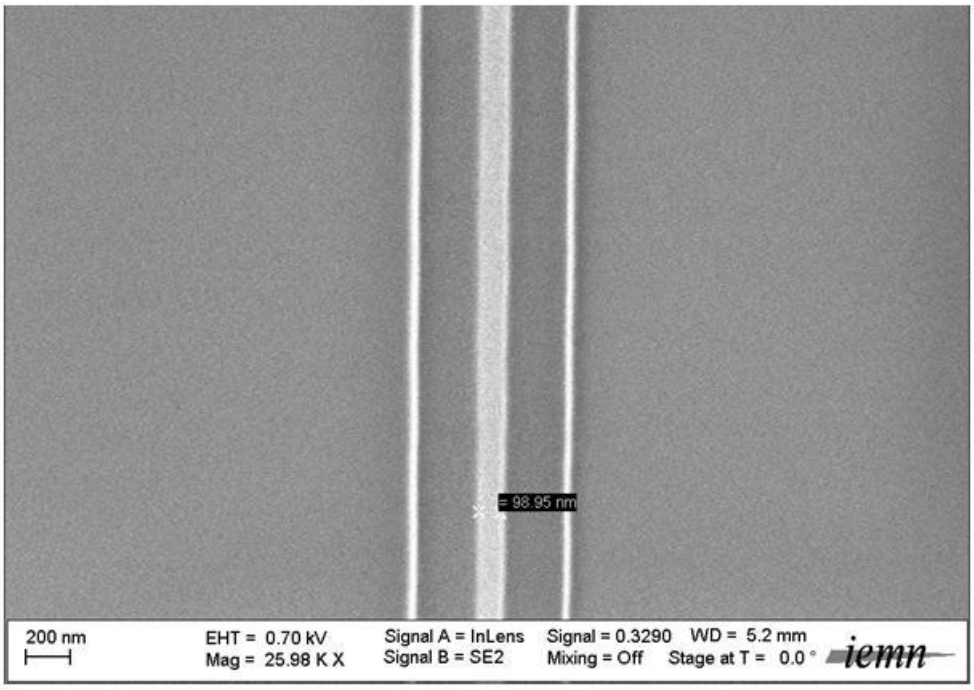


Figure 2-11: SEM observation of the gate lithography after developing

2.4.5.2 Gate recess realization

Without doubt, gate recess is one of the most important processes during the HEMT fabrication. This critical component influences all elements in the small signal equivalent circuit modeling. For obtaining an excellent schottky contact, it is necessary to etch the ohmic contact layer and deposit the metal of schottky contact directly on the undoped material of large band gap.

Too large recess tends to relax electrical field at the gate output and decline the output conductance g_d. Besides, the intrinsic capacitances *Cgs* and *Cgd* will be lowered as well. On the other hand, the resistances *Rs* and *Rd* are increased. With regard to the too narrow recess, it leads to the inverted phenomenons.

Moreover, the depth of recess structure is essential because the threshold voltage V_{TH} depends on basically the distance between the gate electrode and electron gas in the channel. A stable V_{TH} parameter is indispensable for establishing monolithic integrated circuits.

Thereby, four main steps for etching of our gate recess are presented below:

1. Deoxidation the surface by HCl/H_2O (1/10) during 30 seconds
2. Etch Gate recess by succinic acid(pH=5)/H_2O_2 (30/4) during 45 seconds
3. Rinse by EDI water during several minutes.
4. Drying by nitrogen gas.

The gate metallization of Ti/Pt/Au/Ti should be executed immediately after completing the gate recess, which saves the exposed InAlAs layer from oxidation

Figure 2-12 presents the uniform gate foot definition result after the last lift-off process. The gate cap is removed, which makes it possible to observe the morphology of formed gate foot and the recess area. Homogeneous 100nm width of gate recess on the both gate sides are obtained all along the transistor width. In the middle of inset image, the white line is the fabricated gate bottom whose width is 100nm exactly.

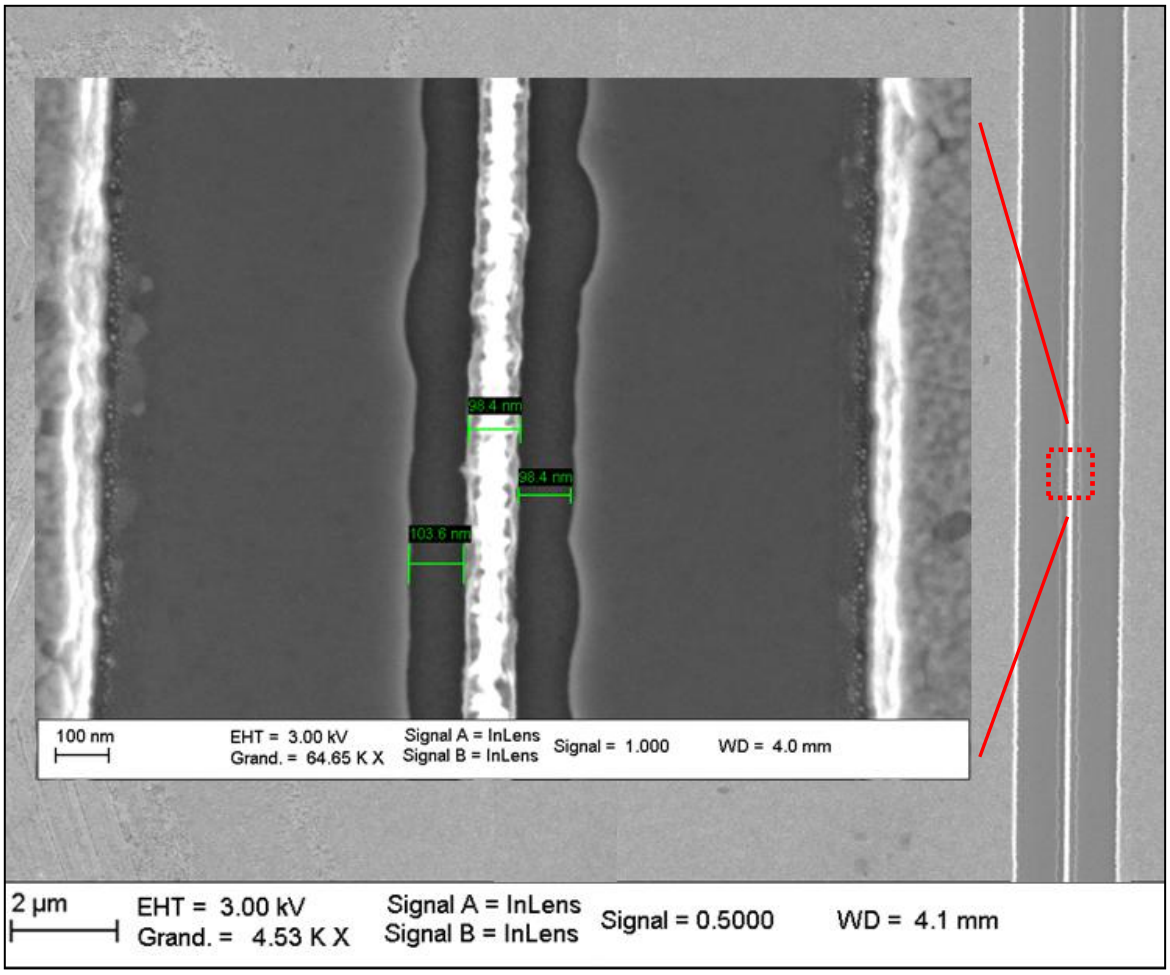


Figure 2-12: SEM observation of our gate foot

Herein, we have already finished our HEMT fabrication on the rigid III-V wafer substrate. Before transferring it onto the flexible substrate, thin film micro-strip access line need to be fabricated for the final S-parameter measurements by vector network analyzer (VNA)

2.5 Thin Film Micro-Strip Access Line

2.5.1 Limitation of Coplanar Waveguide Access Line

In our conventional measurement, the coplanar waveguide (CPW) is oftentimes employed as transmission line access on the rigid III-V wafer with rich experiences [2]. As shown in Figure 2-13, such access structure is composed of one central conductor used as signal line and two reference lines located in each side of the signal plane. *W* is the distance between reference plane and signal plane. *S* stands for the width of central signal plane.

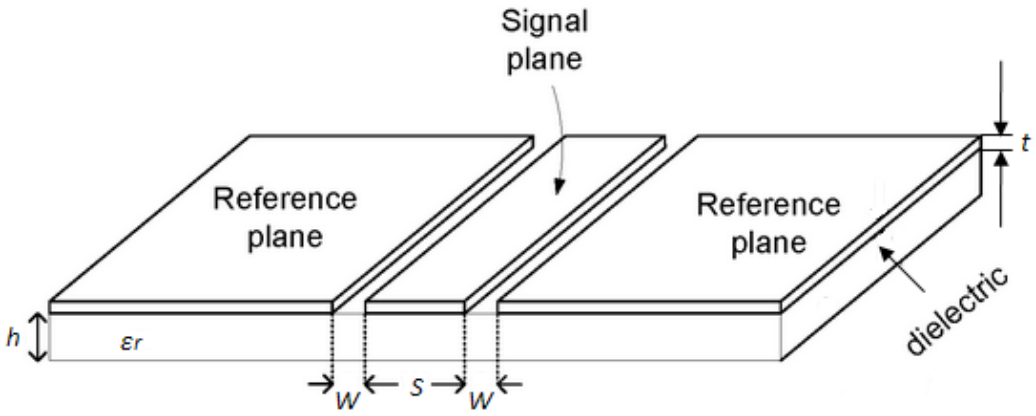


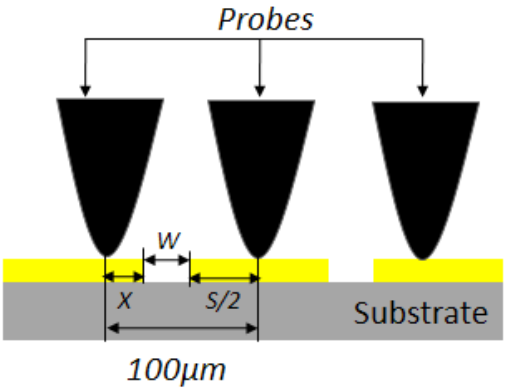
Figure 2-13: Schematic of a CPW on dielectric substrate of finite thickness

In this case, we will explain more about the abandonment of CPW access line solution. The structure of our three probes used for static and RF on-wafer measurements is described in the Figure 2-14 (a). The distance between each probe point, called the pitch, is 100µm. In order to perform a favorable measurement, we should leave at least 10µm space between probe point and the metal strip edge of CPW. It is noted as *X* in Figure 2-14 (a). Here, according to the schematic drawing, the *W*, *S* condition can be calculated by the equations below:

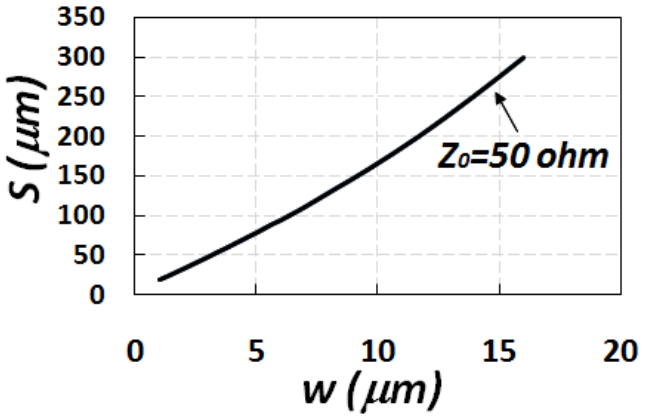
$$\begin{cases} 100\mu m-(S/2+W)=X>10\mu m \\ S/2>10\mu m \end{cases} \Rightarrow \begin{cases} W<80\mu m \\ 20\mu m<S<180\mu m \end{cases}$$

Under such prior conditions, we need to find a reasonable dimension whose characteristics impedance Z_0 can correspond to 50Ω impedance matching. Because the transmission line access will be established on adhesive layer SU-8 which is used to bond wafer onto Kapton, as shown in Figure 2-3, the dielectric material substrate in Figure 2-13 is not semi-conductor any more. Thus, the permittivity ε_r of polyimide or polymer material is much lower than that

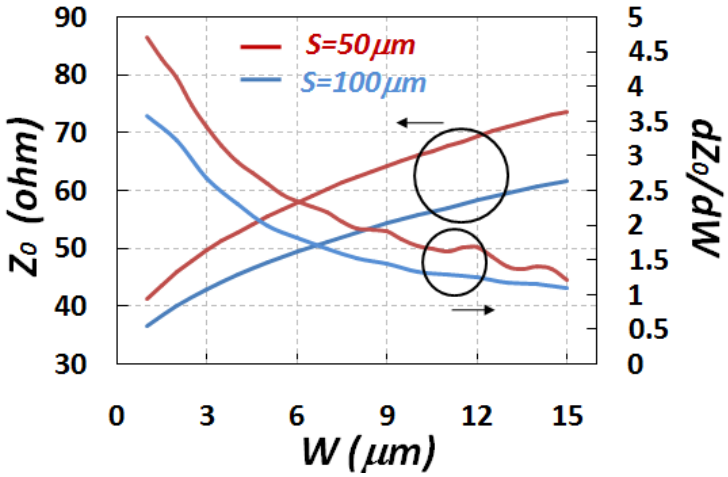
of semiconductor material, which leads to reducing the distance W between reference plane and signal plane in order to keep 50Ω impedance matching [9].



(a)



(b)



(c)

Figure 2-14: (a) Schematic drawing of Probes on the CPW access line; (b) S as function of W when characteristic impedance is 50Ω by *TXLINE* simulation; (c) Characteristic impedance and its variation rate as function of W for both S=50μm and S=100μm dimension by *TXLINE* simulation

With the help of *TXLINE 2003* simulation, we extract the relation between *W* and *S* when characteristic impedance of CPW is equal to 50Ω. Note that in the simulation, the substrate permittivity ε_r of Kapton and SU-8 is almost the same (~3.2). From Figure 2-14 (b), we demonstrate that, in order to maintain 50Ω characteristic impedance, the value of *W* needs to be small (5µm ~10µm) when the size of *S* is in a reasonable range (<180 µm). Moreover, the disturbance of characteristic impedance Z_0 becomes stronger when *W* is reduced as shown in Figure 2-14(c). The variation rate of Z_0 is large when *W* is near 5~10µm. As our substrate is flexible, when the probes are deposited for measurements, the applied pressure tends to cause the deformation of substrate surface. A slight change of the distance *W* may lead to influencing Z_0 value too much. According to Figure 2-15 (b), if we fix *W*>10µm to reduce the dependence of *W* on Z_0, the width of the central signal plane *S* is 170µm for keeping Z_0=50 Ω. This value is larger than the pitch of the measurement probe (100µm). Therefore, such risk of uncertain value of Z_0 makes us choose micro strip as our transmission line access because its special structure is able to get around those problems.

2.5.2 Standard Micro-strip Line

Micro-strip is a kind of electrical transmission line which is widely used to convey microwave frequency signals because of its low cost and light weight. A standard micro-strip line is usually composed of two parallel conductor lines with at least one flat strip of small thickness. The above strip is deposited on a dielectric substrate for mechanical stability. The below strip is a metal ground plane. Figure 2-15 shows the basic configuration of this component.

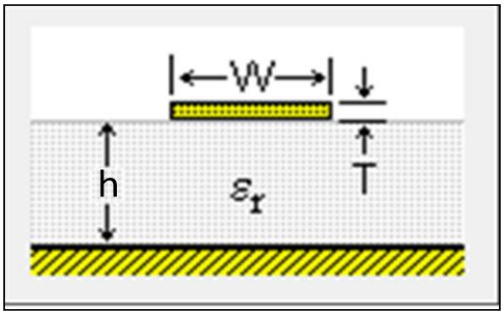


Figure 2-15: Basic structure of a standard microstrip transmission line

h is the thickness of dielectric substrate. ε_r is the relative permittivity of dielectric material. *W* is strip width. *T* is referred as thickness of deposited conductor. Those parameters decide characteristic impedance of the line Z_0:

For W/h>1 (1)

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(\frac{8h}{W} + \frac{W}{4h}\right)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{W}\right)^{-\frac{1}{2}} + 0,04\left(1 - \frac{W}{h}\right)^2\right]$$

For W/h<1 (2)

$$Z_0 = \frac{120\pi/\sqrt{\varepsilon_{eff}}}{\frac{W}{h} + 1,393 + 0,667\ln\left(\frac{W}{h} + 1,444\right)}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{-\frac{1}{2}}$$

By the given range of *W/h* value, we are able to estimate the Z_0 using the different equations. Note that all above calculation methods suppose that the thickness of conductor *T* is much smaller than that of dielectric material (*T/h*<0.005). In our structure, the value *h* of dielectric layer is relatively thin (~11.5 µm). Thus, we call it thin film micro-strip (TFMS).

2.5.3 Thin Film Micro-strip Structure for our access line

Figure 2-16 describes the cross section of thin film micro-strip in our strategy of transmission line access, along with the corresponding view in the mask. The part of brown color is BCB dielectric layer and the part of yellow is metal strip. BCB (***B***enzo***C***yclo***B***utene) is selected as dielectric layer in our TFMS structure due to its interesting physicochemical and electrical properties:

- Low polymerization temperature (<300°C)
- Small relative permittivity ε_r=2.65 (1kHz<f<20GHz)
- Small dissipation factor tanδ=0.0008
- Low water uptake (0.14% at 23°C)
- Excellent thermal stability : Glass transition temperature Tg>350°C
- High resistance 10^{19} Ω·cm

Besides, in our case, the gate electrode is totally covered with BCB resist whose low dielectric constant can inhibit the negative increase of parasite capacitance and ameliorate frequency performance of our device. Also, it is noteworthy that BCB is relatively rigid after final polymerization, which could better prevent the above metal lines from deforming.

The structure is not a very standard TFMS. We use the metallization connection between the two source bonding pads as the ground plane part. The combined structures, two source bonding pads, are indispensable for three probes measurement deposition and form a

Grounded CPW. However, this source bonding pads is able to generate coplanar mode propagation.

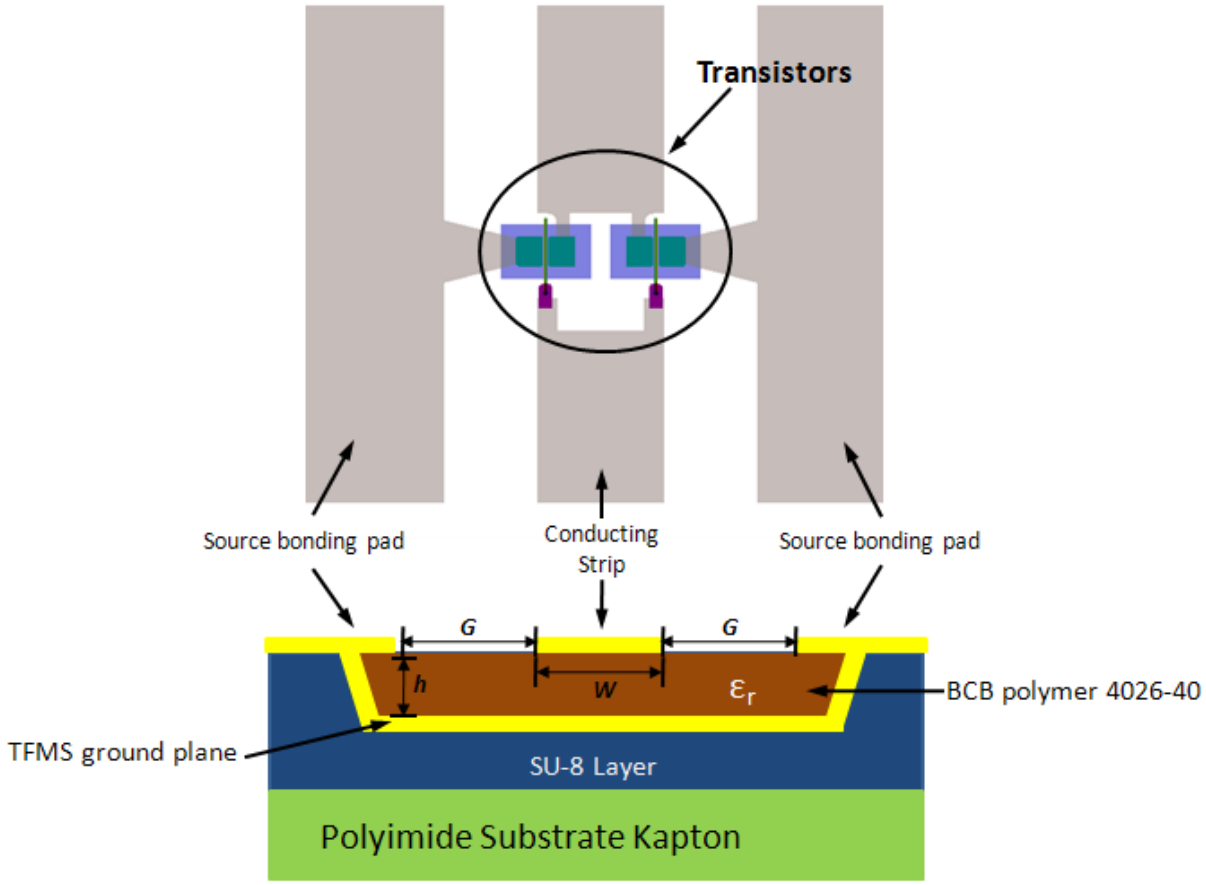


Figure 2-16: Cross section of proposed thin-film micro-strip structure and corresponding part from the designed mask

Herein, before we define the dimension of TFMS structure by *TXLINE* simulation, the electromagnetic field influence caused by source bonding pads on each side of the middle above metal strip (Figure 2-16) should be considered and discussed. By deducing from the *TXLINE* simulation of grounded CPW reference model shown in Figure 2-17 (a), the characteristic impedance Z_0 remains unchanged if the distance G between reference plane and signal plane exceeds 20μm according to the extracted simulation in Figure 2-17 (b). That means, with a fixed ε_r, W and h, the propagation of electromagnetic wave can be independent of the metal plane on two lateral sides when G reaches large enough.

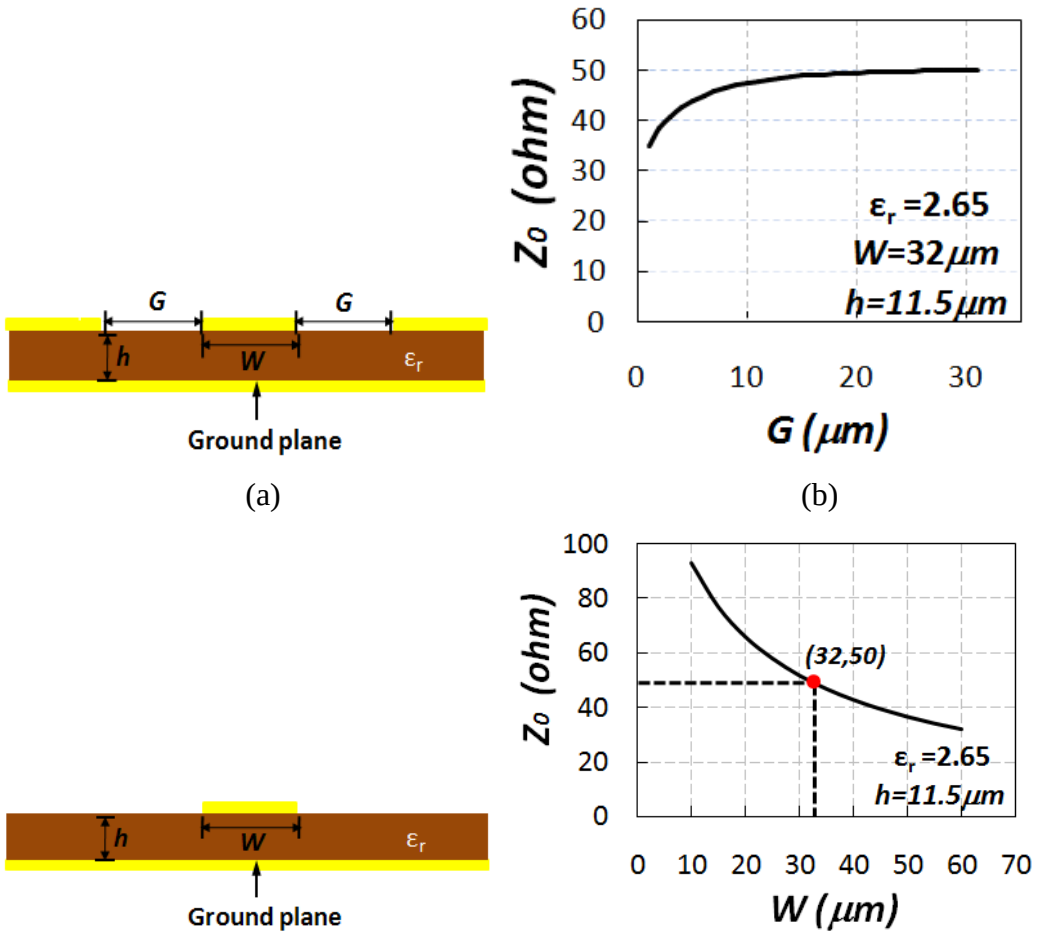


Figure 2-17: (a) Grounded CPW structure used for *TXLINE* simulation; (b) Characteristic impedance for Ground CPW as function of *G* when by *TXLINE* simulation under the defined values of ε_r, *W* and *h*; (c) TFMS structure used for *TXLINE* simulation; (d) Characteristic impedance for TFMS structure as function of *W* by *TXLINE* simulation

Thus, *G* value is certainly possible to be designed 20µm long enough in our case. Ignoring two metal lines on each side, we can only determine the conducting strip width *W* and simulate the structure of Figure 2-15 (c) to obtain the required Z_0. From the given simulation results in Figure 2-17 (d), we design width *W* as 32µm for our 50Ω impedance matching with 11.5µm thickness of BCB polymer

2.5.4 Technologies for TFMS realization

First of all, photosensitive BCB series 4000 commercialized by *Dow chemical company* is indispensable for building the dielectric island. The viscosity of CYCLOTENE 4026-46 BCB resist is acceptable for such extent of BCB thickness (>10µm). After surface treatment by

adherence promoter AP3000, BCB resist is spun onto rigid wafer where fabricated HEMT devices load in the air ambiance [10], and BCB polymer island is defined subsequently by a photolithography process, shown in Figure 2-18 (a).

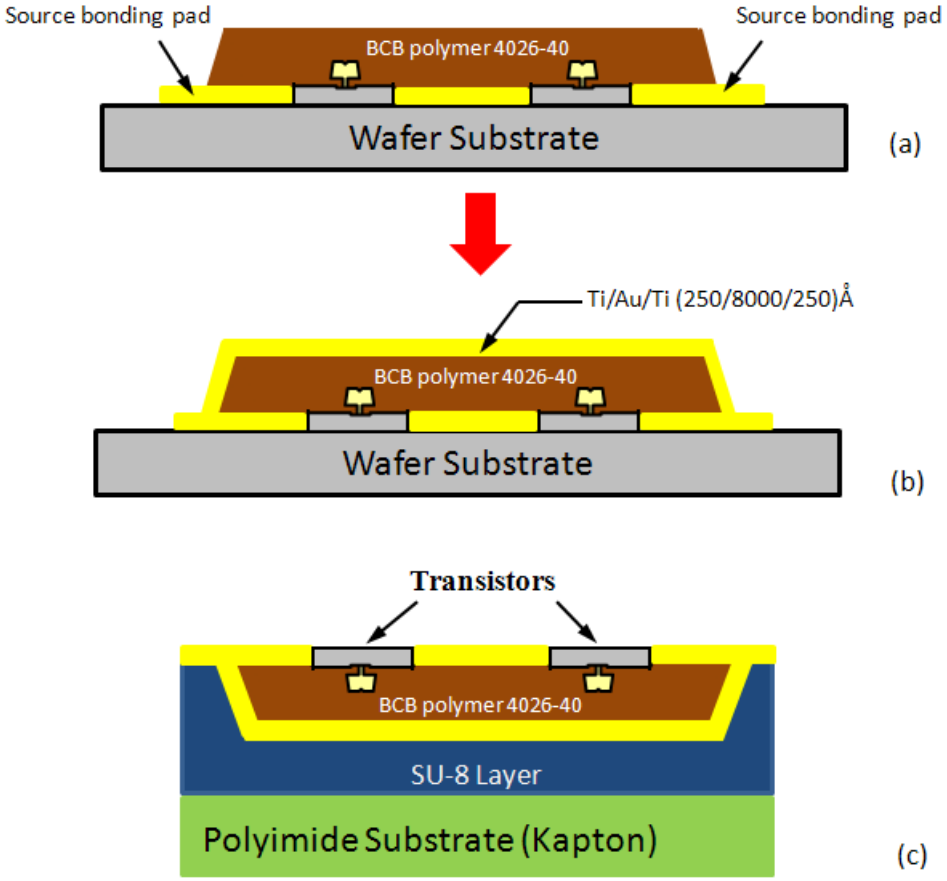


Figure 2-18: Thin Film Micro-strip realization process

Secondly, after achieving well-defined BCB polymer island, a hard bake for BCB is strongly recommended for enhancing the BCB resistance for post process. This polymerization bake must be executed under an inert ambiance at high temperature (<100ppm of O_2) so as to prevent BCB from oxidation.

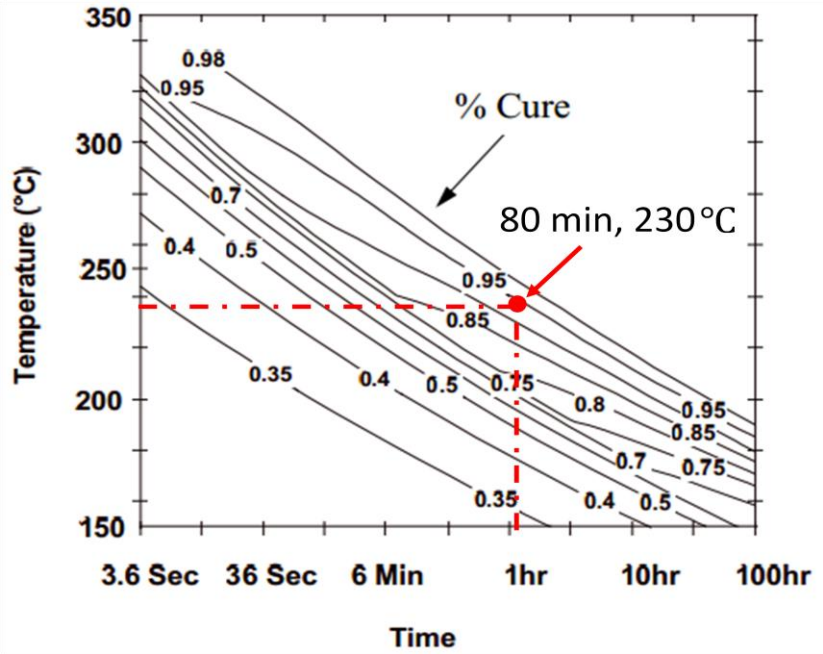


Figure 2-19: Polymerization rate as a function of the temperature and cure duration

Figure 2-19 describes the relation among polymerization rate ,temperature and bake duration [11]. For not degrading the quality of our ohmic contacts and avoiding the Titanium diffusion into barrier layer by gate metal, so-called gate sinking phenomenon [12][13], we choose the polymerization rate line 95% with bake temperature of 230°C during 80 min.

The BCB product supplier recommends using a series of successive temperature before reaching the polymerization temperature so as to evaporate any solvents or organic species. The near-final stage, cooling process should be very slow for inhibiting the massive mechanic stress. Thus, the whole polymerization bake stages are presented in Figure 2-20.

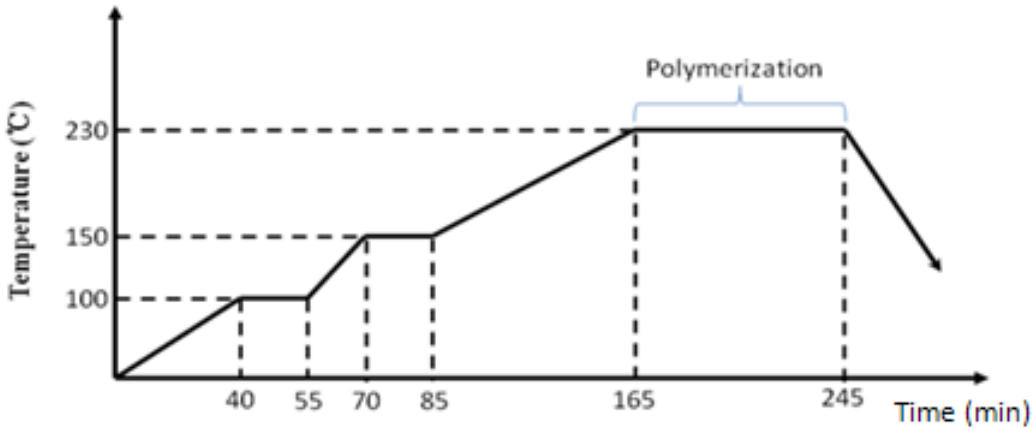


Figure 2-20: Profile of temperature duration in the BCB polymerization process

Finally, as shown in Figure 2-18 (b), a connection of both source bonding pads sides is realized by Ti(250Å)/Au(8000Å)/Ti(250Å)) metallization. This metal line is used as TFMS

ground plane. Note that the whole structure will be upside down during the probes measurement after we finish all fabrication processes, schematized in Figure 2-18 (c).

2.6 Adhesive Bonding Technique

At this point, we have finished all fabrication process for rigid part of our HEMT devices. The adhesive bonding process is followed. Table 2-1 compares all main existing polymer materials in the market. We select regular polyimide Kapton® HN manufactured by *Good Fellow company* as our flexible substrate due to its excellent chemical mechanical and electrical properties over a wide temperature range:

- High working temperature (>300ºC)
- Relatively low coefficient of thermal expansion (CTE)
- Small dielectric Constant (ε_r=3.4)
- Fire retardant, highly resistant to ionizing radiation

Table 2-1 Parameters comparisons of different polymer materials

Polymer name	Upper Working Temperature ºC	CTE ppm/ ºC	Thermal conductivity W/(m·K)
PEN (Polyethylene terephthalate)	155-160	13-21	0.15-0.24
PET (Polyethylene naphthalate)	105-170	20-80	0.15-0.4 (23 ºC)
PI (Polyimide, Kapton)	250-320	30-60	0.10-0.35 (23ºC)
PDMS (Polydimethylsiloxane)	-	310	0.17
PTFE (Polytetrafluoroethylene)	180-260	100-160	0.25

Bonding agent material has to tolerate the final wet-etching solution HCL. After several experiment tests, we focus on SU-8 photoresist provided by *Microchem company*. SU-8 has the similar dielectric constant value of BCB polymer ((ε_r=3.2). Figure 2-21 presents the collage process:

Firstly, SU-8 2002 is spun onto the polyimide Kapton side with relatively thin thickness (~2 µm) in the air ambiance. On the rigid wafer side, a thicker SU-8 (~10µm) is obliged to cover the whole HEMT device structure. Therefore, SU-8 2010, whose property is more viscous, is adopted.

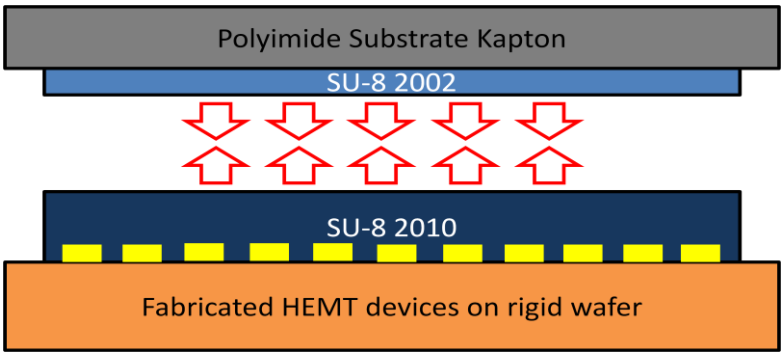
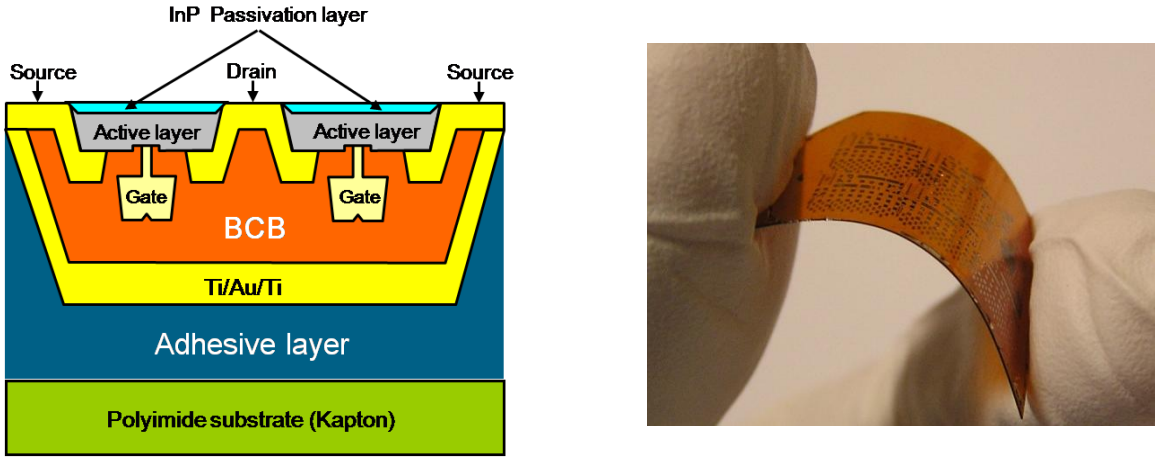


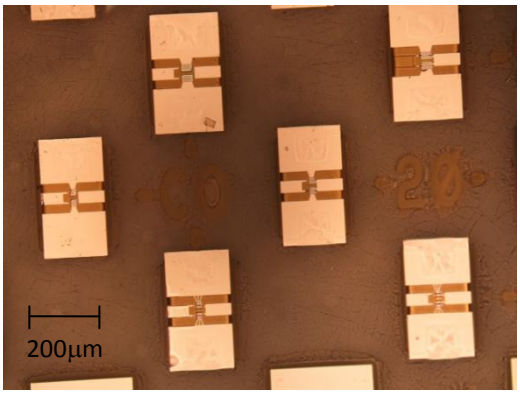
Figure 2-21: Schematic image of collage methods

Secondly, both sides are pressed together (1bar) under vacuum environment and heated at 80ºC during 30 minutes. The structure is presented in the Figure 2-3 (step 6), the whole structure is totally upside-down.

During the last main step, back-side contacts are exposed by two wet-etching processes, including InP substrate and etch-stop layer. For InP substrate, we use hydrochloric acid based solution (HCl/H_2O=2:1). And InGaAs etch-stop layer is selectively etched using a orthophosphoric acid based solution ($H_3PO_4/H_2O_2/H_2O$=5:1:40). This wet-etching process enables to accurately stop on the InP passivation layer. Figure 2-22 (a) shows the final structure of our device. The InP passivation layer and back-side contact metal is exposed to the air. Our devices are upside down status. Figure 2-22 (b) features an optical image of our HEMT-FS, in which the mechanical bendability is clearly observed. Figure 2-22 (c) is the photo of each HEMT component obtained by optical microscopy.



(a) (b)

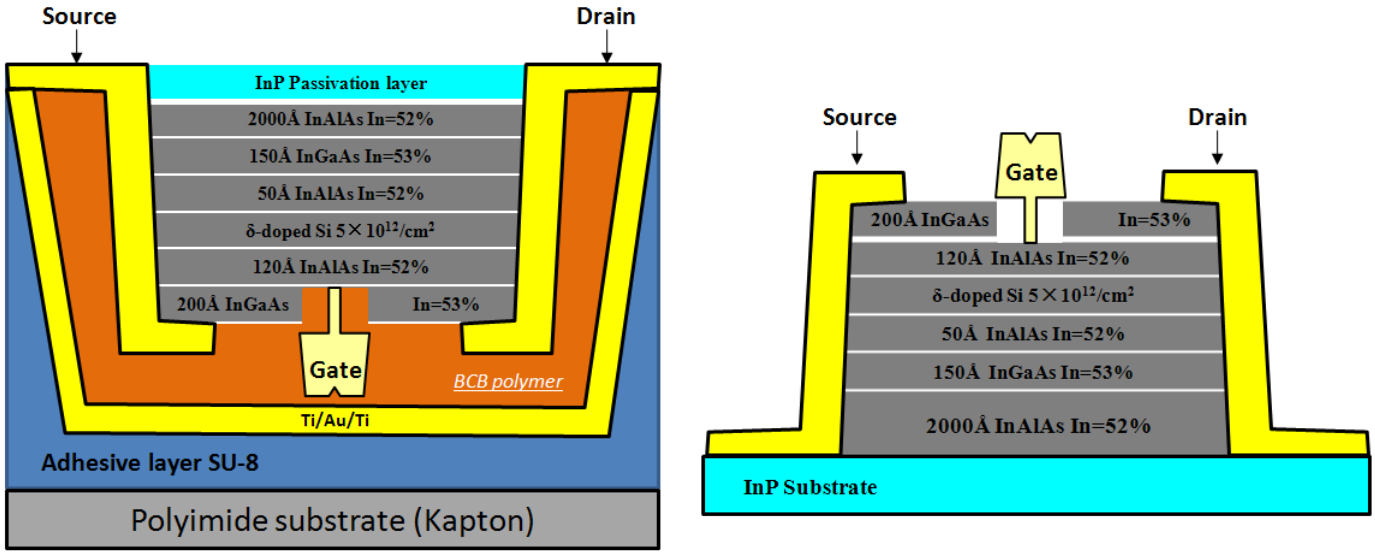


(c)

Figure 2-22: (a) The final structure of HEMT-FS devices; (b), (c) Optical image of HEMT on flexible substrate

2.7 Electrical Characterization of HEMT-FS

In this paragraph, both the static and dynamic performances of HEMT-FS are presented. In addition, for the sake of the benchmark of HEMT-FS structure, standard HEMTs on rigid substrate (HEMTs-RS) have been fabricated on another wafer. Note that HEMTs-RS do have the same epitaxial active layer as HEMT-FS and have identical device geometry with physical gate length of 100nm and gate width of 2×50µm. The final layer structure of both HEMT-FS and HEMT-RS are shown in the Figure 2-23 (a) and (b) for the following comparison.



(a) (b)

Figure 2-23: The layer structure comparison between the (a) HEMT-FS and (b) HEMT-RS

2.7.1 Characterization of ohmic contacts and Hall Measurements

The ohmic contact characterization has been performed by TLM (Transmission Line Method) proposed by W. Shockley. This method can determine both the sheet resistance ($R_{\square}$) of hetero-structure and the contact resistance (R_C). As shown in Figure 2-24, by measuring different resistance values for every distance L with *4 points* measurement, the scales of resistance allow us to calculate $R_{\square}$ and R_C by TLM model.

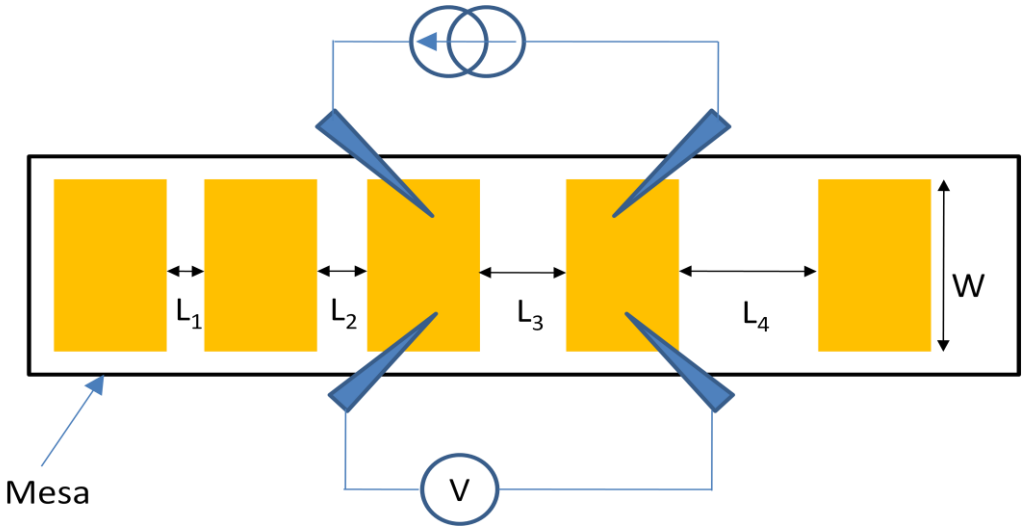


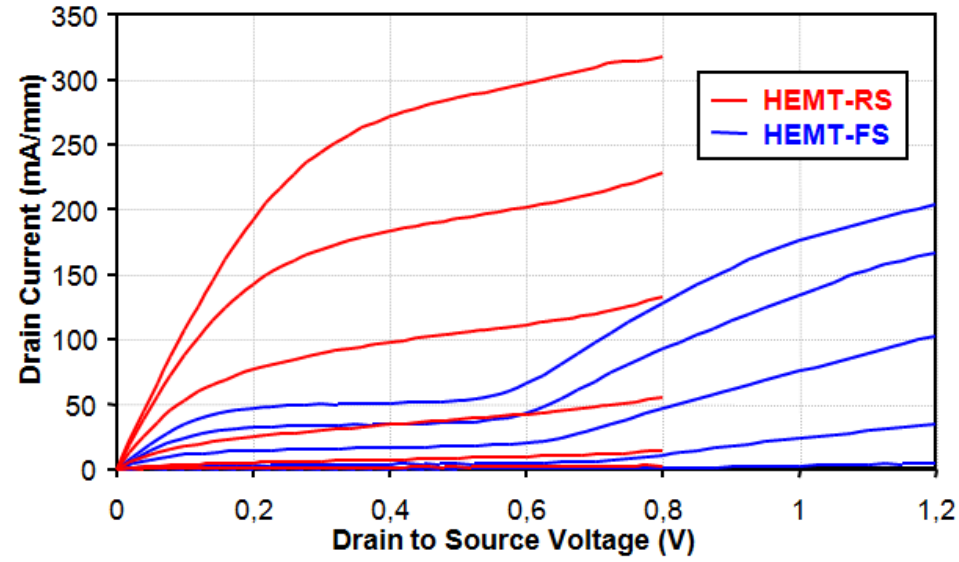
Figure 2-24: Structure test for the TLM measurement

In our case, L_1=2µm, L_2=4µm, L_3=8µm, L_4=16µm and W=100µm. The average value of our obtained contact resistance R_C is equal to 0.125Ω.mm by *TLM calculator* software

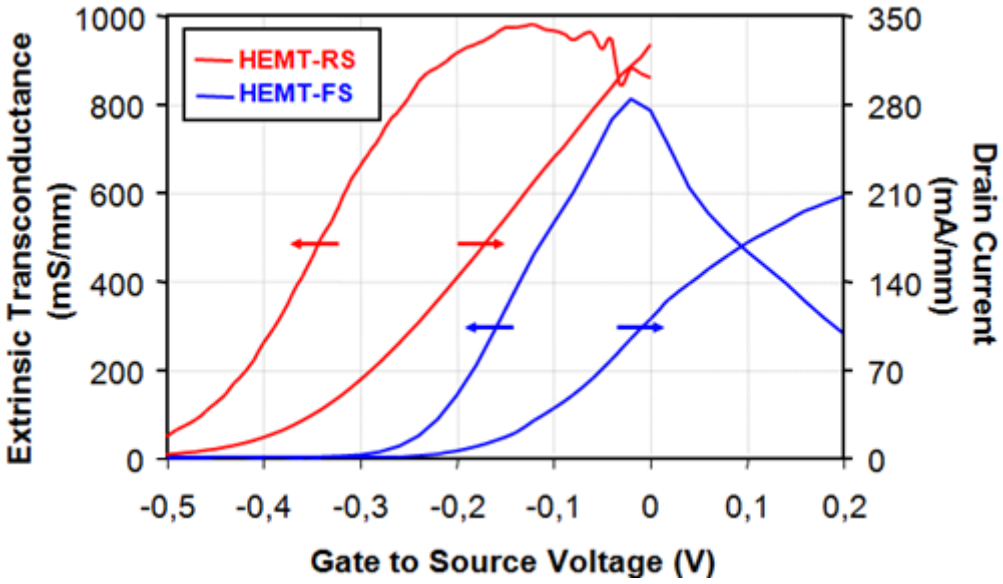
Hall measurements of Van Der Pauw method have been performed at room temperature on both HEMT-FS and HEMT-RS active layers. Note that the measurement for HEMT-RS is after the devices are completely realized on flexible substrate. The hall mask of HEMT-FS is shown in Figure 2-4. HEMT-FS presents a hall mobility and a hall density of 7400 cm^2/V^{-1} s^{-1} and 5.4×10^{12} cm^{-2}, respectively, while HEMT-RS features a hall mobility and a hall density of 6900 $cm^2/V^{-1}s^{-1}$ and 6.8×10^{12} cm^{-2}, respectively. It is to be noted that hall density of HEMT-FS is lower than HEMT-RS one. Since both structures have the same active layer, the difference can be attributed to a partial depletion of the HEMT-FS channel layer by the surface potential related to interface trap density at the InP passivation layer/air interface.

2.7.2 Static performances

Figure 2-25 plots on wafer static measurements at room temperature on both HEMT-RS and HEMT-FS. Figure 2-25 (a) is typical output characteristics, showing, for HEMT-FS, the value of maximum drain current Id_{MAX} reaches 210mA/mm for a gate-to-source voltage V_{GS}=0.2V.



(a)



(b)

Figure 2-25: (a) Output characteristics of the HEMT on rigid substrate (HEMT-RS) and on flexible substrate (HEMT-FS). The top gate bias for HEMT-FS is 0.2V and for HEMT-RS is 0.1V, both gate steps are -0.1V. (b) Transconductance characteristics at V_{DS}=0.8V (HEMT-RS) and V_{DS}=1.2V (HEMT-FS)

According to transfer characteristics shown in Figure 2-25 (b), maximum extrinsic transconductance g_m of HEMT-FS is 800 mS/mm for a drain-to-source voltage V_{DS}=1.2 V. By contrast, this value is about 1000 mS/mm at V_{DS}=0.8V on rigid substrate. Moreover, the threshold voltage V_{TH} is estimated to be 0.25V on HEMT-FS, while it reaches 0.5V on HEMT-RS. A qualitative explanation for these differences (positive shift of V_{TH}, decrease of gm and I_{dMAX} for HEMT-FS) lies in the fact that the HEMT-FS is upside down after transfer,

as shown in Figure 2-22 (a). Indeed, the InP passivation layer, whose surface is exposed to air, does not fully prevent the depletion of the channel due to the Fermi level pinning at the surface. As a result, the depletion of the channel layer leads to the presence of a kink effect phenomenon when impact ionization occurs. Kink effect can be clearly observed when looking at the output characteristics of HEMT-FS at V_{DS} around 0.7 V in Figure 2-25 (a). This phenomenon in HEMTs has been widely reported in the literature [14][15]. The main reason of the kink effect is the combination of the holes accumulation generated by impact ionization on the high-field drain end of the gate area in the channel layer and the low electron channel concentration in the source side in recessed area[16][17]. According to this mechanism, holes accumulation in the source side area leads to an opening of the channel which increases the drain current. The details of Kink effect will be retold in the chapter of optimization research.

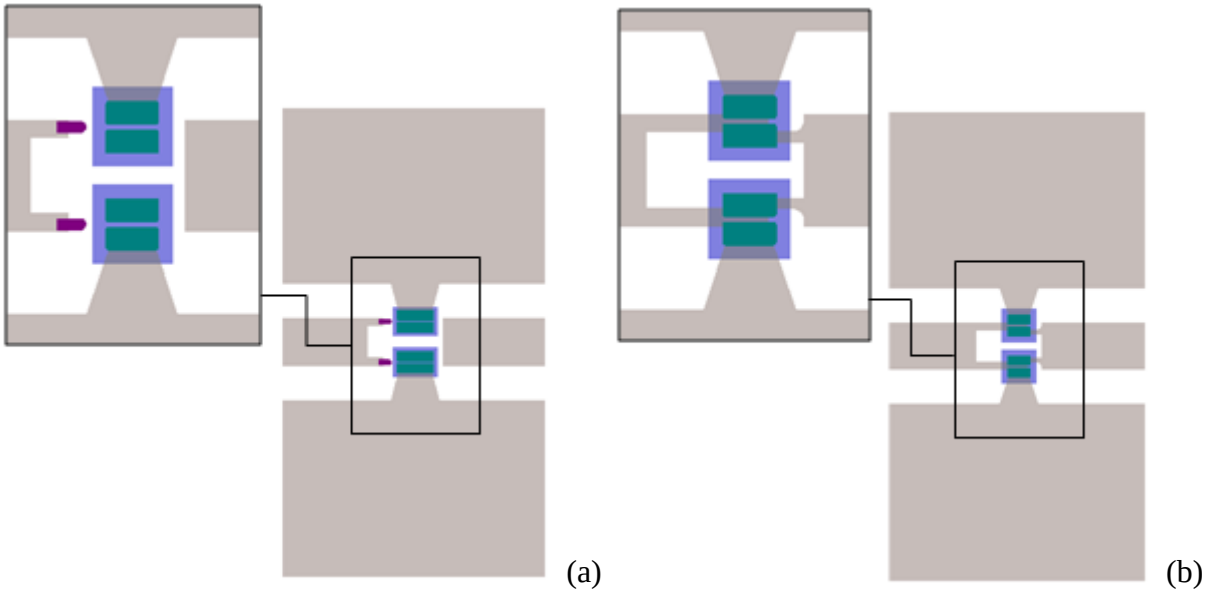
2.7.3 Dynamic performances

The S-parameters of the 100-nm-gate HEMT-FS and 100-nm-gate HEMT-RS are measured on wafer using a vector network analyzer. Before characterizing the dynamic elements, an off-wafer calibration should be taken by an alumina impedance standard substrate (ISS) in order to remove high frequency parasitic characteristics existing in the measuring instruments. In our work, LRRM calibration on alumina ISS (using calkit 138-357 provided by the RF probes supplier, *Cascade Micro-tech*) are always performed.

Besides, the additional parasitic components related to contact pads and access lines must be taken into account in the measured S-parameters of transistors. Thus, in order to remove such parasitic contribution, we apply the method proposed by Mr. van wijnen [18]. This method involves measuring the error matrix subtracted from the gross S-parameters. In our case, TFMS access lines fabricated by BCB polymer cause the error matrix. Two structures are performed on the mask of the transistor, one is a structure of type 'open', and the other structure is type 'short', showing in Figure 2-26. The 'open' and 'short' devices have been fabricated on the same wafer. It is possible to subtract those parasitic elements and extract the matrix Y_{trans} of our transistors by the formula (1).

$$Y_{trans}=((Y_{dut}-Y_{open})^{-1}-(Y_{short}-Y_{open})^{-1})^{-1} \quad (1)$$

Where Y_{dut} represents the undeembeded matrix, Y_{open} is the matrix of the 'open' structure, and Y_{short} stands for the matrix of 'short' structure.

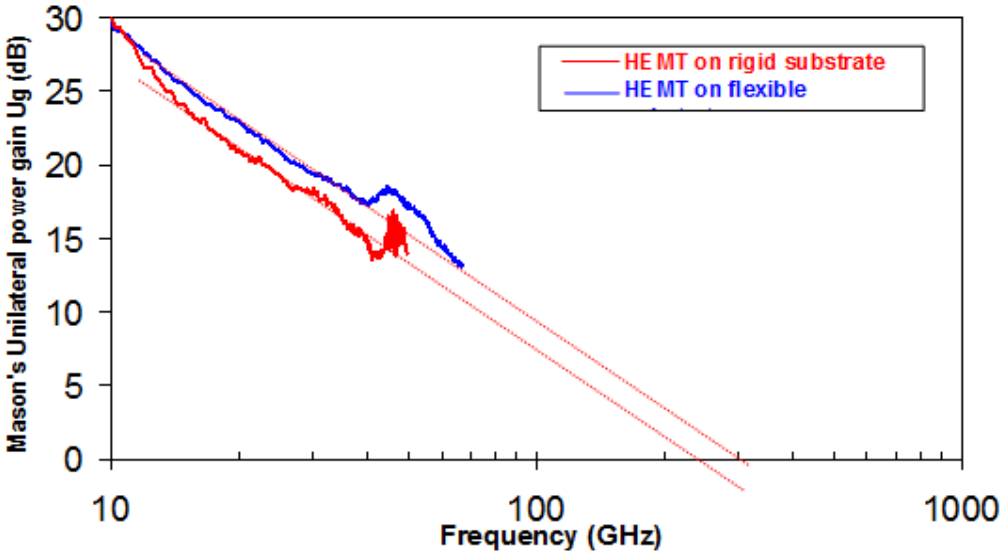


(a) (b)

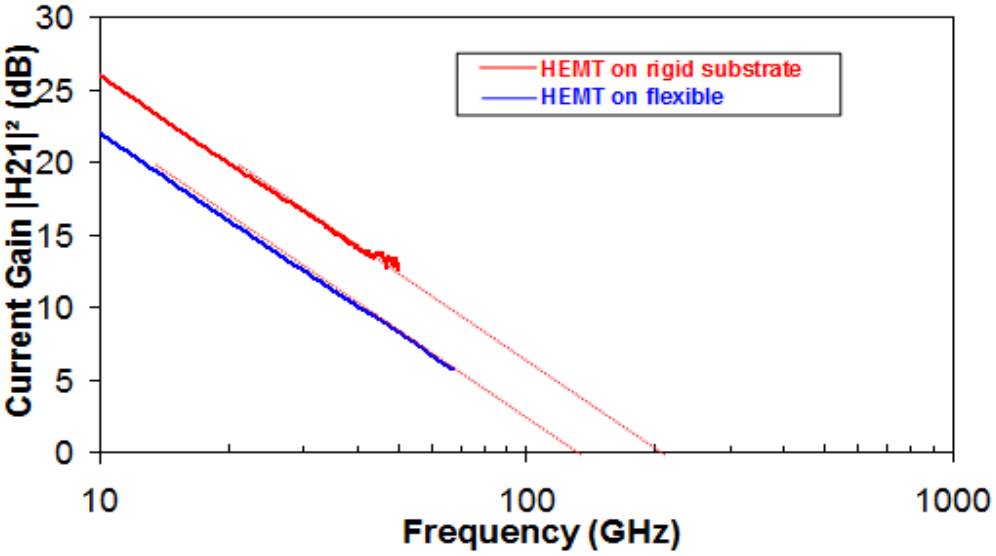
Figure 2-26: 'Open' structure (a) and 'Short' structure (b) used to subtract the error matrix associated with access line of the transistor

Figure 2-27(a) shows the Mason's unilateral power gain *Ug* and Figure 2-27(b) the extrinsic current gain $|H_{21}|^2$ versus frequency for both devices. Note that parasitic capacitances caused by the probing pads are carefully subtracted from the measured S-parameters by using the methods mentioned above. Based on the usual 6dB/octave extrapolation, the HEMT-FS exhibits a f_T of 120 GHz and a f_{MAX} of 280 GHz. For HEMT-RS, cut-off frequencies f_T and f_{MAX} are 203 GHz and 215 GHz respectively.

The lower f_T obtained on HEMT-FS can be attributed to the decrease of *gm* and the use of BCB polymer which increases parasitic capacitances. The higher f_{MAX} for HEMT-FS arises from the surface potential on InP layer. This surface potential counteracts the effect of carrier injection in the InAlAs buffer layer [19] and increases the electrons confinement in the InGaAs channel layer, which leads to lower output conductance $g_{d.}$ So, despite of slight difference in terms of cut-off frequencies particularly due to the kink effect, radio frequency performances obtained for both devices are very similar and seem to be not affected by adhesive bonding process on flexible substrate.



(a)



(b)

Figure 2-27: (a) The Mason's unilateral power gain U_g as a function of frequency measured at V_{DS}=0.8V (HEMT-RS), V_{DS}=1.2V (HEMT-FS). (b) Current gain $|H_{21}|^2$ as a function of frequency measured with the same voltages.

2.8 Conclusion of Chapter 2

The complete fabrication process of our flexible HEMT transistors is introduced in the chapter, providing a feasible method for transferring conventional HEMTs onto the flexible substrate. With the help of adhesive bonding technique, 100nm-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HEMTs have been transferred onto polyimide film Kapton.

Both static and dynamic electrical characterizations of HEMT-FS have been carried out at room temperature. Despite the presence of Kink Effect on these devices, which seems to be related to the partial channel depletion, high cut-off frequencies (f_T=120 GHz and f_{MAX}=280 GHz) have been achieved. These performances are in line with those obtained on 100 nm-gate HEMT on rigid substrate. On the other side, due to Kink Effect, the 210mA/mm maximum drain current is relatively lower than those of HEMT-RS. The mechanical bendability of our HEMT components is demonstrated.

These good characteristics open up the possibility to integrate high-frequency communication systems and other high-speed applications into the flexible devices. In the next chapter, the optimization of the epitaxial layer for lowering the Fermi level surface pinning effect of HEMT-FS is scheduled in order to suppress the kink effect and, thus, enhance the device electrical performance. The above assumption of the cause for Kink Effect will be verified experimentally,

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CHAPTER III

Optimization of HEMT-FS Active Layers and Bending Electrical Characterizations Test

Chapter 3: Optimization of HEMT-FS Active Layers and Bending Electrical Characterizations Test

3.1 Introduction

In the last chapter, we will point out the major defect of previous structure which causes the Kink Effect and subsequently propose an optimized epitaxial layer structure of our HEMT devices for eliminating this negative effect.

All improved static and dynamic performances are demonstrated without the apparition of Kink Effect. The redesigned transistors can operate with higher drain current and cut-off frequencies.

The second section of this chapter is comprised of mechanical bending test which explains how flexible device electronics work under flexure status. By the probe measurements on the arc-shaped metal support, three various degrees of bending conditions and different bending directions of HEMT devices are studied in our research. The study indicates that electrical performances are weakly affected by bending induced strain.

3.2 Optimization of HEMT-FS Active Layers

The first section will describe the optimized layer structure from the *Kink Effect* understanding. And then, the excellent static and dynamic performances resulting from our new HEMT epitaxial structure confirm our assumption. Those improved electrical characteristics successfully overcome the *Kink Effect* phenomenon, meanwhile, enhances both the maximum drain current and cut-off frequencies values.

3.2.1 Mechanism of Kink Effect

From the previous chapter, Figure 2-25 (a) shows the Kink Effect phenomenon which results in an abnormal increase in the static drain current at a certain value of V_{DS} (~0.6V). The Kink Effect is not only a typical phenomenon in HEMT sector, but also exists in the field of MOSFET-SOI (silicon-on-insulator metal oxide semiconductor FET) [1]. In the MOSFET sector, this phenomenon can be explained by the accumulation of minority carriers generated by impact ionization towards the substrate.

As for HEMT devices part, the researchers have pointed out that the Kink phenomena were related to the reduction of the source resistance *Rs* resulting from an electron density increase in the recess area of source side [2][3]. This change in the electron density is illustrated in Figure 3-1. In thermodynamic equilibrium (Figure 3-1-a), the Fermi level is equal within the whole hetero-structure layers and is fixed by surface pinning. There is no current in the perpendicular direction of hetero-interfaces. When V_{DS} increases and approaches the energy of band gap (~Eg/q), the impact ionization occurs and holes begin to accumulate in the high-field drain end of the gate area in the channel layer. Those holes are accelerated and run through the channel toward the source side. The hole accumulation in source recessed area leads to the separation of quasi-Fermi level of electrons E_{Fn} and holes E_{Fp}, and the quasi-Fermi level of channel layer for holes E_{Fp} becomes closer to the valence band (Figure 3-1-b).

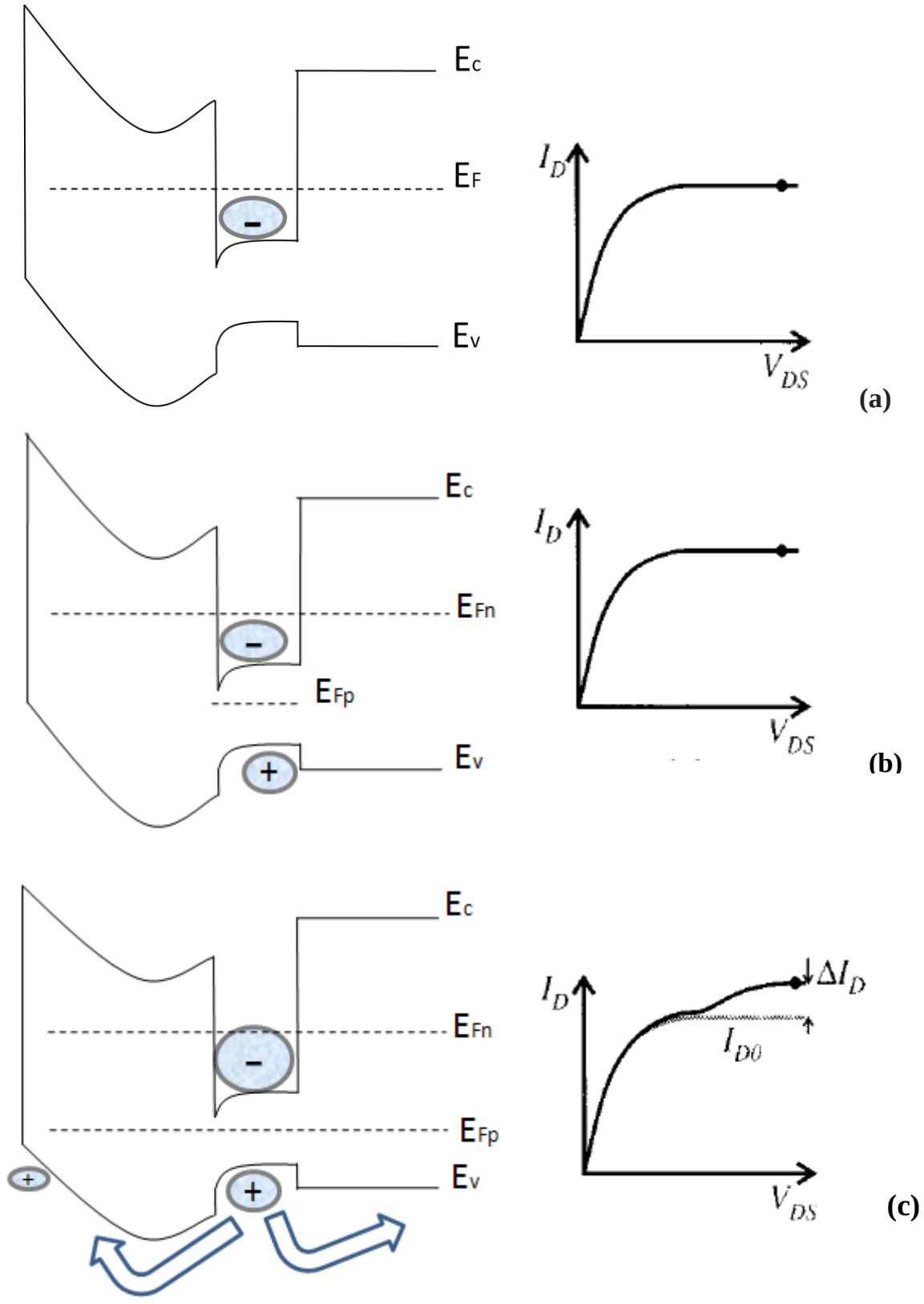


Figure 3-1: Mechanism of the Kink Effect apparition in the source recessed area: (a) Quasi-Fermi levels for electrons E_{Fn} and holes E_{Fp} are equal in thermodynamic equilibrium; (b) When holes begin to accumulate with the increase of V_{DS}, E_{Fp} in the channel moves closer to

valence band; (c) Some of the holes are transferred to the surface and substrate of source recessed regions, resulting in an increase of electron density in the channel layer.

In fact, at this moment, there exists two curvatures of E_{Fp}, one is between the channel and the surface of recessed area, the other is between the channel and buffer substrate. The modified profile of potential causes a small hole current to the surface and/or the buffer substrate interface in order to equalize the quasi-Fermi level for holes E_{Fp} among the channel layer, barrier layer and buffer layer (Figure 3-1-c). As a result, the quasi-Fermi level for electrons E_{Fn} becomes greater than the original E_F, resulting in the electron density increase in the place of source recessed region. Such abnormal increasing leads to the sudden enhancement of drain current.

Moreover, Mr. Suemitsu *et al* pointed out that the impact ionization is just one necessary factor but still not enough for inciting the Kink Effect phenomenon. Before the impact ionization occurs, the low electron density in the source recessed zone which caused by surface depletion is another prerequisite to bring about the Kink Effect. The kink arises from the electron density with increasing V_{DS} and intensity of the kink depends on the inverse of electron density. Thus, if the electron density is so large that the influence of a small change in electron density can be ignored, the kink will not be able to appear [3].

From this point of view, we conclude that our kink effect is mainly caused by two combined reasons:

1. Holes accumulation generated by impact ionization on the high-field drain end of the gate region in the narrow band gap channel.
2. Relatively low electron concentration inside the channel layer of the source recessed area.

These two factors lead to the opening of the channel and the drain current increasing. Therefore, now that we cannot change the channel layer material, only the second point gives us one possible solution for eliminating this negative kink effect. We try to enhance the electron concentration in the channel layer to avoid the kink effect in the end.

3.2.2 HEMT-FS Fabrication with Optimized Layer Structure

In our previous work, InP passivation layer was not sufficient to avoid a partial depletion of the channel caused by the Fermi level pinning due to the surface potential at the air-semiconductor interface leading to high kink effect (Figure 3-2).

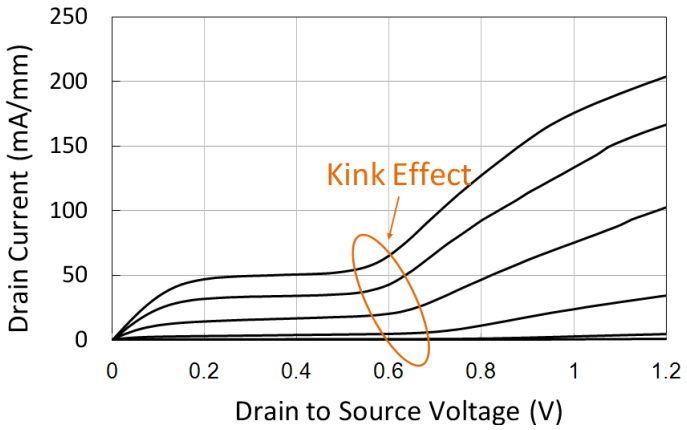


Figure 3-2: Kink Effect observed at V_{DS} around 0.7 V in our previous work. Top gate bias is 0.2V and gate steps is -0.1V

In the optimization work, a second Silicon delta-doping plane (3×10^{12} cm^{-2}) has been added between the channel and the buffer layer which screens the surface potential effect, as shown in Figure 3-3.

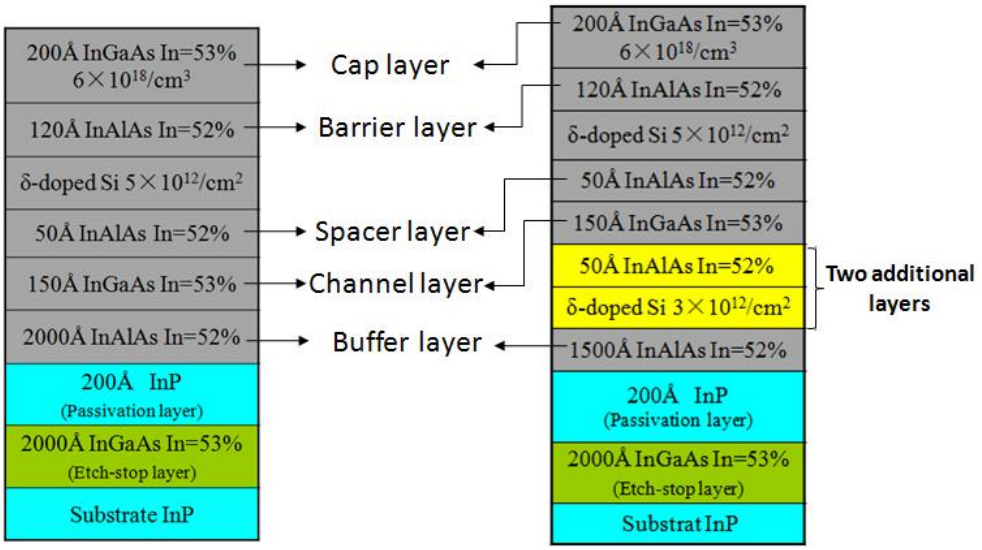


Figure 3-3: Comparison of the structures between the previous epitaxial layers (left side) and the optimized epitaxial layers (right side) of InP-based HEMT on the flexible substrate

In order to confirm this optimized structure, we employ the *Schrödinger-Poisson Equation* software to calculate the electron density value. Without considering the condition of InP passivation layer surface exposed in the air, we compare the electron concentration with that of our previous structure. The electron concentration of channel layer in the optimized structure has doubled, from 2×10^{12} cm^{-2} to 4.3×10^{12} cm^{-2}, which proves our new structure is ameliorated and feasible. The fabrication steps of HEMTs on flexible substrate (HEMT-FS) are the same as those already reported in our previous work with identical device geometry (physical gate length of 100 nm and gate width of 2×50 μm). The Ni/Ge/Au/Ni/Au ohmic contacts are defined by electron beam lithography, metal E-beam evaporation and annealed at 295°C for 20s. Then, the mesa wet-etching for device isolation is performed. This wet-etching stops at the interface between InP passivation layer and InGaAs etch-stop layer. Next, bonding pads are realized by the metallization of Ti/Au/Ti. After the gate-recess process is carried out and Ti/Pt/Au/Ti gate metals are evaporated and lifted off. Next, thin-film microstrip (TFMS) access lines fabrication and adhesive bonding process are involved. During the last step, the InP substrate and InGaAs etch-stop layer of the upside-down HEMT structure are, respectively, removed by an accurate wet etching process which stops on the InP passivation layer.

3.2.3 Improved Electrical Characterization Results

All the following measurements are carried out at room temperature. Hall measurement has been performed on active layer (with cap layer) of HEMT-FS after the devices are completely realized on flexible substrate. Hall density (n_H) and Hall mobility (μ_H) reach 8.9×10^{12} cm^{-2} and 7300 $cm^2\cdot V^{-1}\cdot s^{-1}$, respectively. In our previous work, it was found that n_H and μ_H were 5.4×10^{12} cm^{-2} and 7400 $cm^2\cdot V^{-1}\cdot s^{-1}$. We can observe that hall mobility remains unchanged while n_H is strongly increased due to the additional silicon doping plane.

As the part of static performances, Figure 3-4 shows the typical output characteristics of the transistor in unbent condition. Previously reported output characteristics [4] are also plotted. For this work, the value of maximum drain current I_{dMAX} reaches 580 mA/mm for a gate-to-source voltage V_{GS}=0V. Compared with our previous work, the value of this current increase by ~176% and the kink effect is totally suppressed. The disappearance of the kink effect can be attributed to the optimized layer structure which fully prevents the depletion of the channel layer and, consequently, avoids the low electron channel concentration of the source side in the recessed area.

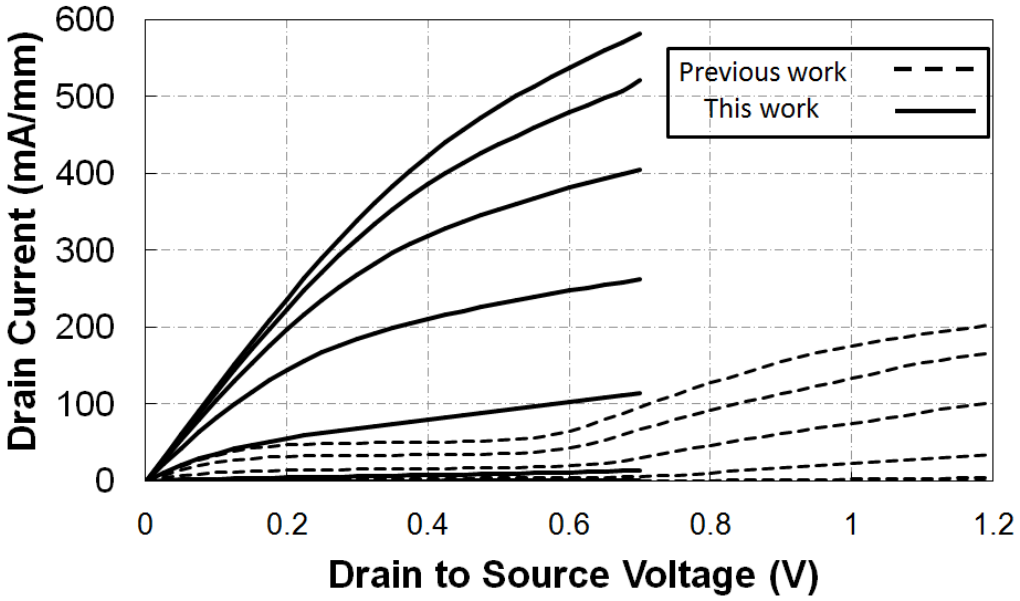


Figure 3-4: (Solid line) Output characteristics of 100 nm-gate length HEMT-FS in unbent status. Gate bias voltage is 0V for the top curve and the gate step is -0.2 V. (Dashed line) Previous output characteristics of 100 nm-gate length HEMT-FS in unbent status. Gate bias voltage is 0.2V for the top curve and the gate step is -0.1 V

Nevertheless, as shown in Figure 3-5, the maximum extrinsic transconductance *gm* is about 750mS/mm for a drain-to source voltage V_{DS}=0.7 V. The g_m in our previous work is equal to 800mS/mm. But it should be pointed out that the previous extrinsic transconductance is under Kink effect condition. From the dashed line in Figure 3-4, around V_{DS}=0.5V where Kink effect hasn't appeared yet, the extrinsic transconductance is much lower than that of V_{DS}=1.2V, shown as the blue dashed line in Figure 3-5. Thus, in the optimized work, the extrinsic transconductance *gm* has been greatly enhanced without any Kink effect.

Besides, threshold voltage V_{TH} is estimated to be -1.2V. The value of V_{TH} is equal to -0.25V in our previous work. This negative shift of V_{TH} can be attributed to the higher charge density in the channel observed on measured hall parameters. Consequently, higher negative gate voltage is needed to deplete the channel layer.

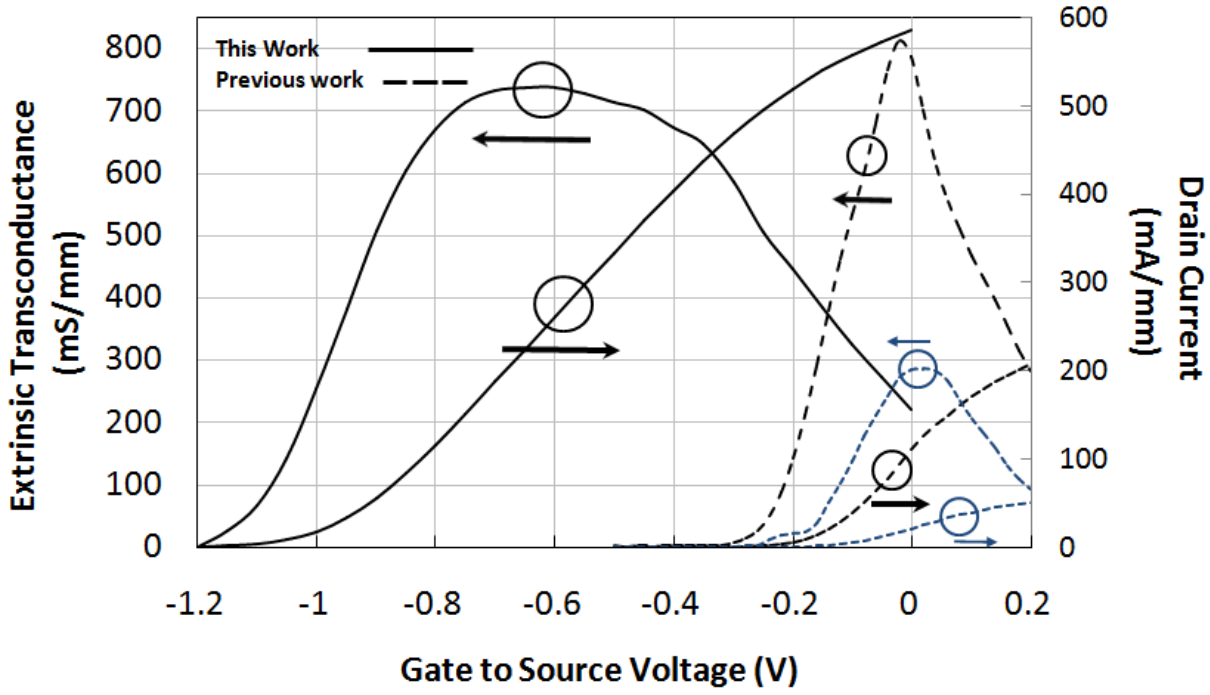


Figure 3-5: (Solid line) Transconductance characteristics of 100 nm-gate length HEMT-FS in unbent status at V_{DS}=0.7V. (Black dashed line) Previous transconductance characteristics of 100 nm-gate length HEMT-FS in unbent status at V_{DS}=1.2V. (Blue dashed line) Previous transconductance characteristics of 100 nm-gate length HEMT-FS in unbent status at V_{DS}=0.5 V.

As the part of the dynamic performances, the S-parameters of the 100 nm-gate HEMT-FS have been measured by using a vector network analyzer. The Mason's unilateral power gain *Ug* and the extrinsic current gain $/H_{21}/^2$ are shown as a function of frequency in Figure 3-6. Note that, as the previous work, parasitic components related to the probing pads have been carefully de-embedded from the measured S-parameters using "open" and "short" devices fabricated on the same wafer [5]. Based on the usual 6dB/octave extrapolation, the HEMT-FS exhibits a f_T of 160 GHz and a f_{MAX} of 290 GHz.

In our previous work, the HEMT-FS exhibited a f_T of 120 GHz and a f_{MAX} of 280 GHz. In fact, during high-frequency (HF) measurements, the Kink effect is almost nonexistent [2]. Thus, the maximum value of extrinsic transconductance g_m under Kink effect condition (at V_{DS}=1.2V) is not applicable in previous HF measurement. The true effective g_m in HF measurement could be estimated after the extraction of small signal equivalent circuit parameters in the following section (P.98)

The calculated g_m of previous work under HF condition is equal to ~600mS/mm which is lower than that of optimized work. Therefore, the higher g_m arises the increased f_T and f_{MAX}.

Moreover, this RF performance improvement can be also attributed to the higher charge density measured in this active layer which decrease source and drain parasitic resistances (R_S and R_D) [25].

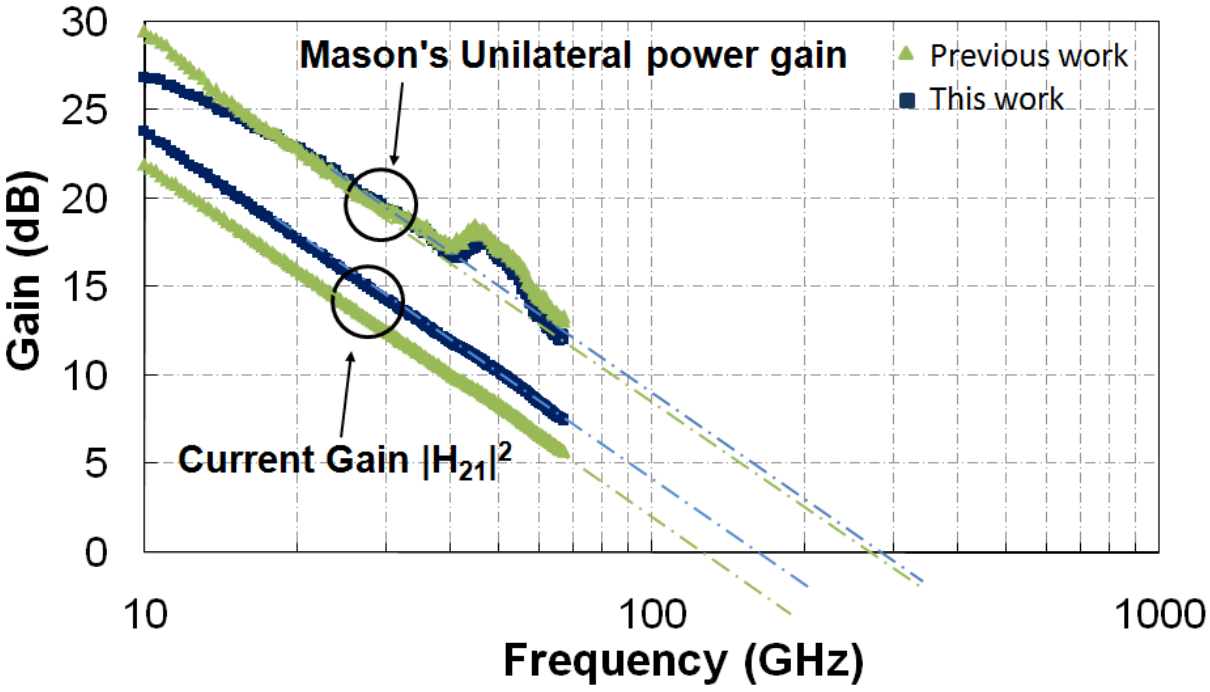


Figure 3-6: Frequency dependence of Mason's unilateral power gain *Ug* and current gain $|H_{21}|^2$ measured at V_{DS}=0.7V for this work and at V_{DS}=1.2V for previous work. Dashed-dotted lines correspond to 20dB/decade extrapolation.

3.2.4 Extracted parameters of the small signal equivalent circuit

The small signal equivalent circuit (SSEC) parameters are also essential for analyzing our HEMT devices in the following section. Thus, herein, the methodologies of these parameter extractions are presented and the experimental results of our transistors in unbent condition are listed subsequently.

Around a bias point, the basic SSEC model of the HEMT can be described by the form of diagram shown in Figure 3-7.

Those elements in the figure are classified into two categories:

- Extrinsic elements, outside the active device, which are independent of the bias point of the transistors, they are:

  L_S, L_G, L_D: the source, gate and drain inductors.

  R_S, R_G, R_D: the source, gate and drain resistances

  C_{PG}, C_{PD}: the gate and drain parasitic capacitances

- Intrinsic elements, characterizing the active device, which strongly depend on the polarization of the transistors, they are:

  C_{GS}, C_{GD}, C_{DS}: the gate-source, gate-drain, and drain-source capacitances

  R_{GD}, R_i: the gate-drain resistance and the intrinsic resistance

  g_{mi}: the intrinsic transconductance

  g_d: the output conductance

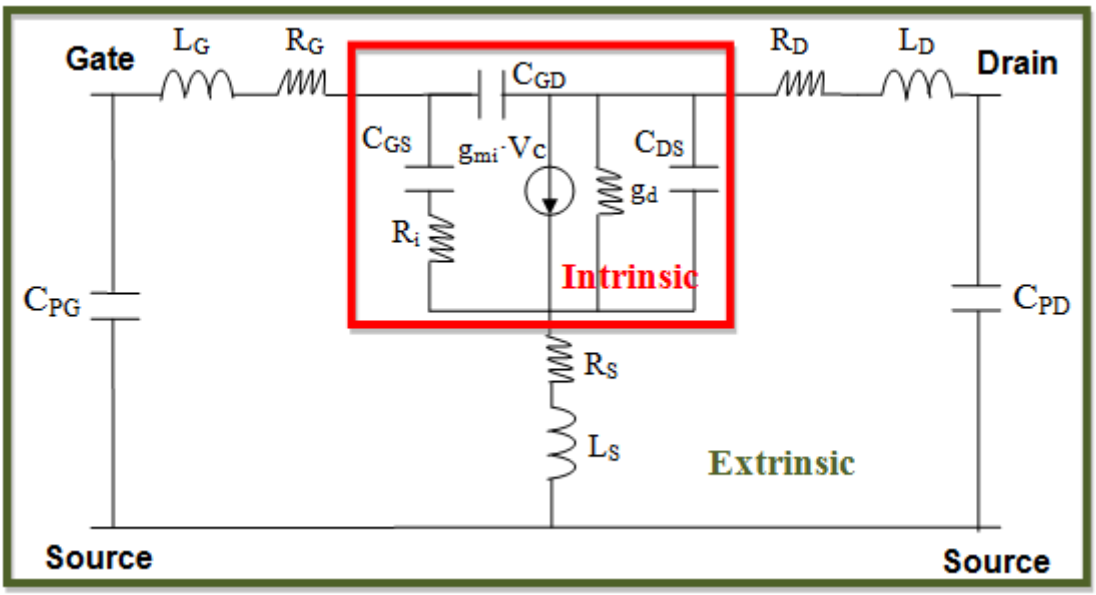


Figure 3-7: Small signal equivalent circuit of HEMT

The off-wafer calibration and on-wafer de-embedding are well done at first. The elements of SSEC model are extracted according to the S-parameter measurement proposed by G. Dambrine [6][7] and the method proposed by Koolen [8].

The flow diagram of this extraction methodology for intrinsic elements of transistor is shown below in Figure 3-7. From the matrix Y_{trans}, we are able to subtract capacitance value of C_{PG} and C_{PD}. Then, the obtained Y parameters are converted into parameter Z to subtract the extrinsic series elements R_S, R_D, R_G and inductances L_S, L_D, L_G. Finally, the obtained matrix Z is converted into a matrix Y. This matrix, called as Y_{int}, will determine all the intrinsic elements of equivalent circuit shown in Figure 3-8.

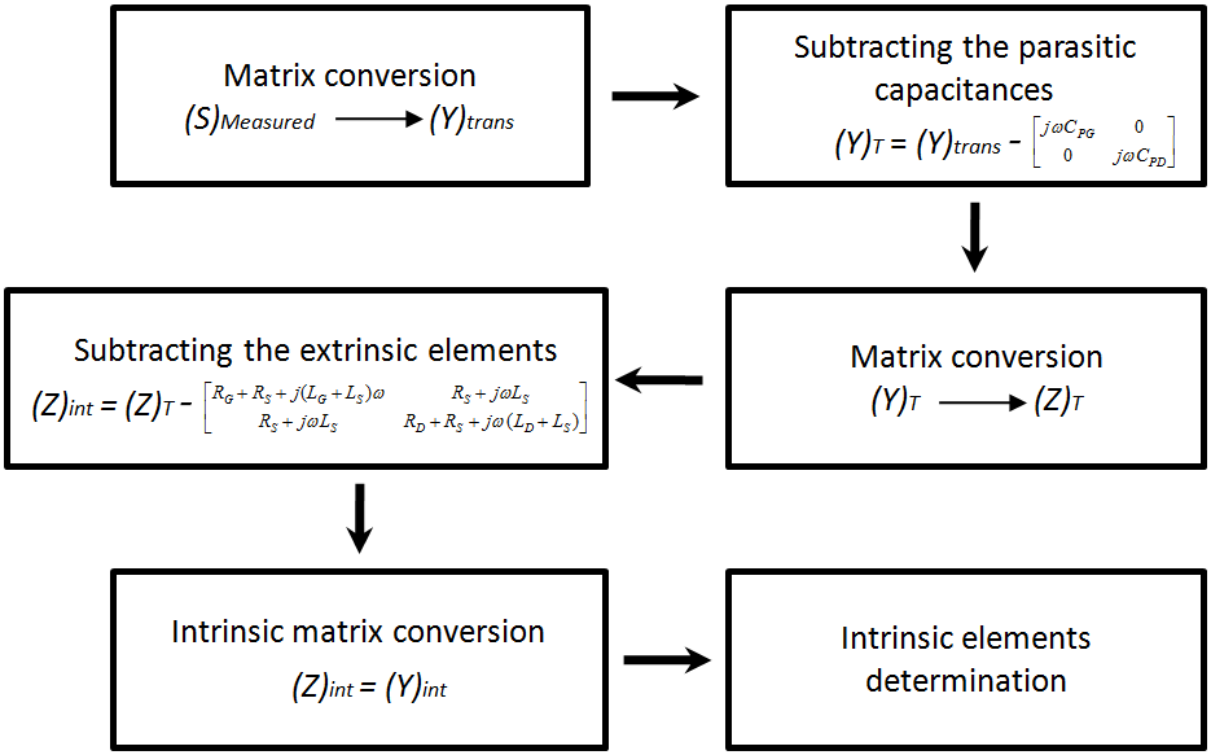


Figure 3-8: Methodology of extracting the elements of HEMT SSEC model

Extraction of capacitance C_{PG} and C_{PD}

The capacitances C_{PG} and C_{PD} are measured by removing the channel conductivity, that is to say, the device is biased at V_{DS}=0V with V_{GS} which is much lower than the threshold voltage V_{TH}. Under this polarization, the capacitance between gate and source is obtained in the same way as that of gate and drain. An additional hypothesis is introduced, consisting of negligible intrinsic capacitance C_{DS} between drain and source. By measuring the parameters *Y*, these capacitances can be calculated by the formula (1) and (2).

$$C_{PG} = \frac{\mathrm{Im}(Y_{11} + 2Y_{12})}{\omega} \qquad (1)$$

$$C_{PD} = \frac{\mathrm{Im}(Y_{22} + Y_{12})}{\omega} \qquad (2)$$

Extraction of extrinsic elements R_G, Rs, R_D, L_G, L_S and L_D

The resistance R_G, *Rs*, R_D and the inductance L_G, L_S, L_D are also able to be extracted when the device is biased at V_{DS}=0V with V_{GS} which is relatively higher than the threshold voltage. The impedance parameters are measured under several normal V_{GS} polarizations. From the obtained Z matrix, the resistances and inductances are calculated using the following equations, from (3) to (5):

$$Z_{11} \approx R_G + R_S + \frac{R_C}{3} + \frac{1}{j\omega Cg} + j\omega(L_S + L_G) \quad (3)$$

$$Z_{12} \approx R_S + \frac{R_C}{2} + j\omega L_S \quad (4)$$

$$Z_{22} \approx R_S + R_D + R_D + j\omega(L_S + L_D) \quad (5)$$

Cg is the capacitance between the gate electrode and channel layer when V_{DS}=0V. R_C is the channel resistance

The extraction of parasitic inductance is difficult. We adjust the values of those inductances in order to have the intrinsic elements series independent of the frequency.

Extraction of intrinsic elements

After the extraction of extrinsic elements, the intrinsic elements such as g_{mi}, g_d, R_i, C_{GS}, C_{GD}, C_{DS} are calculated from Y_{int} using the formulas below, from (6) to (11):

$$g_{mi} = -\left|\frac{Y_{int21} - Y_{int12}}{Y_{int11} + Y_{int12}}\right| \frac{1}{\mathrm{Im}\left(\frac{1}{Y_{int11} + Y_{int12}}\right)} \quad (6)$$

$$g_d = -\mathrm{Re}(Y_{int22}) \quad (7)$$

$$R_i = \mathrm{Re}\left(\frac{2}{Y_{int11} + Y_{int12}}\right) \quad (8)$$

$$C_{GS} = -\frac{1}{\omega\,\mathrm{Im}\left(\frac{1}{Y_{int11} + Y_{int12}}\right)} \quad (9)$$

$$C_{GD} = -\frac{\mathrm{Im}(Y_{int12})}{\omega} \quad (10)$$

$$C_{DS} = \frac{\mathrm{Im}(Y_{int22} + Y_{int12})}{\omega} \quad (11)$$

The extraction of our small signal equivalent circuit has been done on the transistor with gate length of 100nm and gate width of 2×50μm. The devices are biased at V_{DS}=1.2V and V_{GS}=-0.04V in the saturation region (f_T = 120 GHz and f_{MAX} = 280GHz) for our previous work. The device of this work is biased at V_{DS}=0.7V and V_{GS}=-0.62V in the saturation region (f_T = 160 GHz and f_{MAX} = 290GHz). The comparisons of extrinsic and intrinsic elements under unbent condition are listed in the table below.

Table 3-1 Parameters of SSEC model for our HEMT-FS in unbent status

	Extrinsic Elements				
	Rg (Ω/mm)	**Rs (Ω.mm)**	**Rd (Ω.mm)**	**Cpg (fF/mm)**	**Cpd (fF/mm)**
This Work	69	0.34	0.35	13	68
Previous Work	75	0.53	0.56	34	103

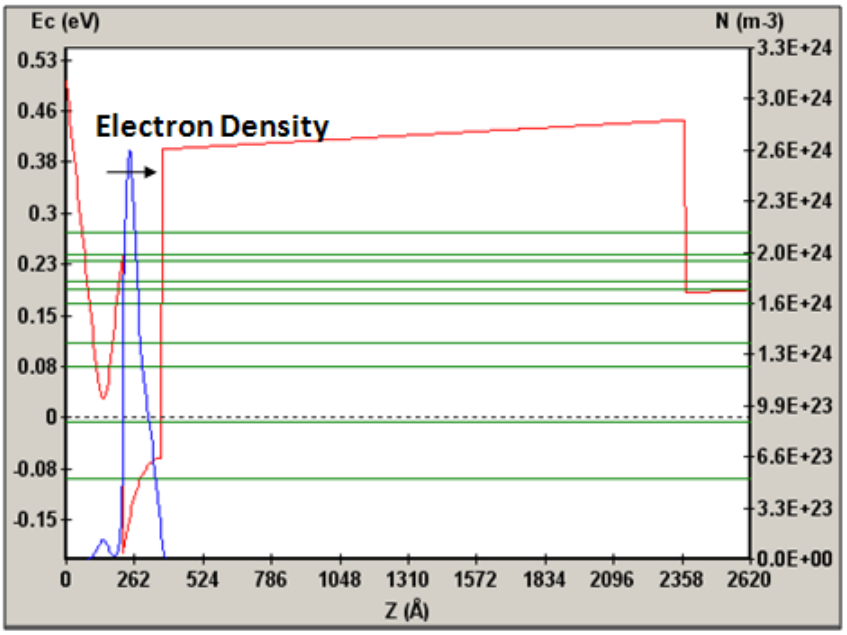
	Intrinsic Elements				
	g_{mi} (mS/mm)	**g_d (mS/mm)**	**Cgs (fF/mm)**	**Cgd (fF/mm)**	**Cds (fF/mm)**
This Work	1020	131	597	194	103
Previous Work	896	72	721	138	17

Firstly, the effective g_m in HF measurement of previous work can be calculated by equation below:

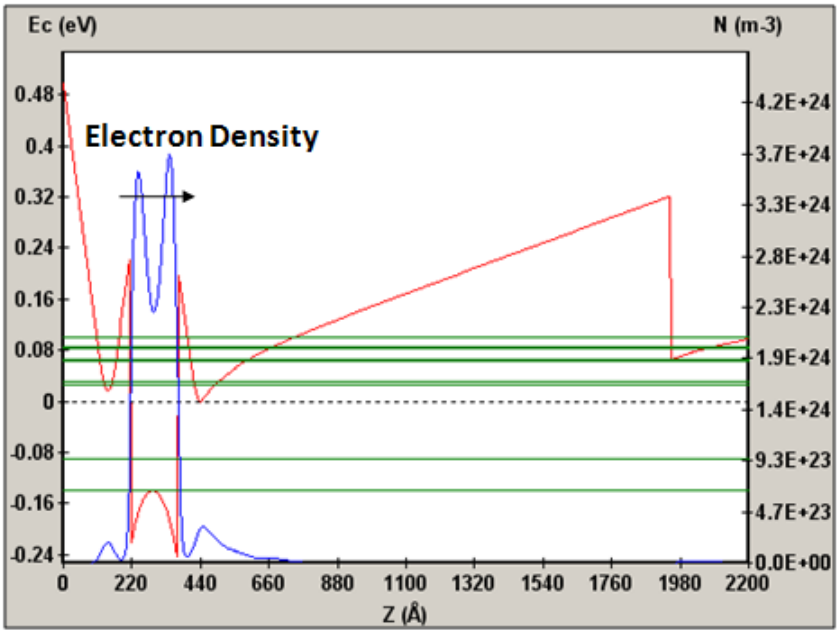
$$g_m = \frac{g_{mi}}{1 + g_{mi} Rs} \qquad (12)$$

g_{mi} is the intrinsic transconductance and *Rs* is the source resistance which can be obtained by above extraction in Table 3-1. The lower calculated effective g_m (~600mS/mm) causes the lower frequency performance in previous work.

Also, as mentioned above, due to higher charge density, the reduction of source and drain resistances (*Rs* and *Rd*) is demonstrated well in this work. The diminution of *Cgs* can be explained by the increase of distance between gate electrode and electron gas due to the additional layers (spacer and Silicon delta-doping plane, Figure 3-3). According to the simulation of conduction band and electron density distribution by *Schrödinger-Poisson Equation* software in Figure 3-9 (a) and (b), the enlarged average distance between electron gas and gate recess area is demonstrated. In other words, the efficiency for the charge control of electron gas in the channel $\frac{\partial Ns}{\partial V_{GS}}$ is lower when the distance between gate electrode and electron gas is larger.



(a)



(b)

Figure 3-9: Conduction band structure and electron density distribution of previous epitaxial layers (a) and optimized epitaxial layers (b)

Those small signal equivalent circuit parameters are also useful to explain and analyze the subtle electrical characteristics variation in the following device test of different bending conditions

3.3 Electrical Characteristics on the Effect of Surface Tensile Strain

In this section, the study of HEMT device under different bending conditions is developed. The mechanical modeling for multi-layers consideration is enunciated. Afterwards, the measurements for various bending radius are performed. The applied strain in the bending test has two directions: source-drain direction and gate width direction. Both measurements comparisons are given and discussed.

3.3.1 Mechanical modeling method of multi-layers for flexible device

To analyze the mechanism of our bending active layers in our device, we use the model solution put forward by Chien-Jung Chiang [9].

At first, let us consider a simple example, a single-material beam shown in Figure 3-10 (a). The longitudinal stress in a bent film is given by:

$$\sigma = E'\varepsilon \qquad (13)$$

$$E' = \frac{E}{1-\nu^2}$$

E is the Young's modulus of the film material. ν is the Poisson's ratio. E' is the reduced elastic modulus. The position of AB layer is called neutral layer (NL). It means that AB layer maintains its original length when this beam is bent with radius R in Figure 3-10 (b). All other layers (CD) above it are stretched while those below it (EF) are compressed. Here, what we need is to calculate the strain value of CD layer. This strain is defined by:

$$\varepsilon = \frac{\Delta l}{l} \qquad (14)$$

Where l is the original unbent length, and Δl is the change of length after bending. Back to our case, before bending, shown in Figure.3-8 (a):

$$\overline{AB} = \overline{CD} = l \qquad (15)$$

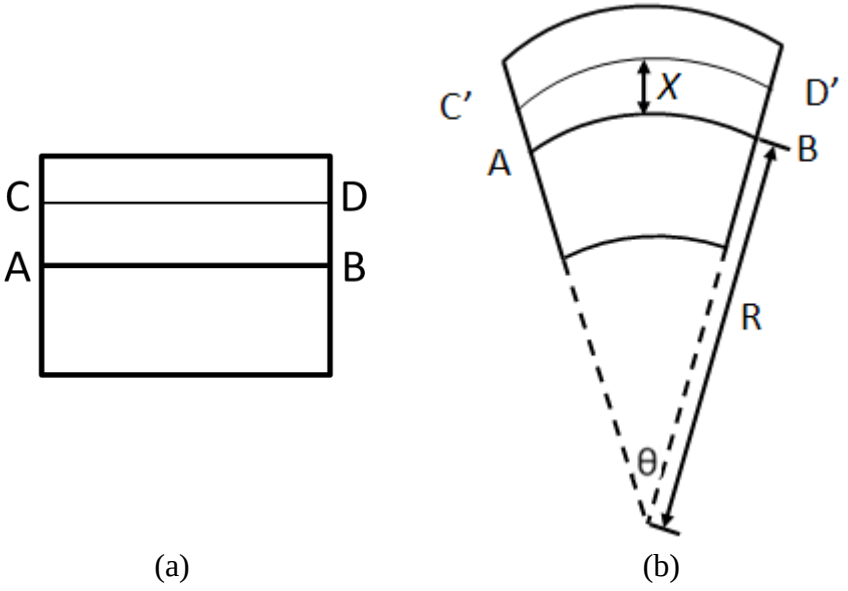
After bending, shown in Figure.3-8(b), the prolonged CD layer becomes C'D' layer:

$$\overline{AB} = l = R\theta \qquad (16)$$

$$\overline{C'D'} = l + \Delta l = (R+x)\cdot\theta \qquad (17)$$

Here, x is the distance from the layer to NL. Thus, the strain value of CD layer becomes:

$$\varepsilon(x) = \Delta l / l = x\theta / R\theta = x / R \qquad (18)$$



(a) (b)

Figure 3-10: One single-material film before bending (a) and after bending (b), AB layer is the neutral layer, C'D' layer is CD layer after bending with radius R

We can deduce the strain value in any layer with its distance from the NL being x. Thus, the stress in any layer can be expressed by:

$$\sigma(x) = \frac{E'x}{R} \qquad (19)$$

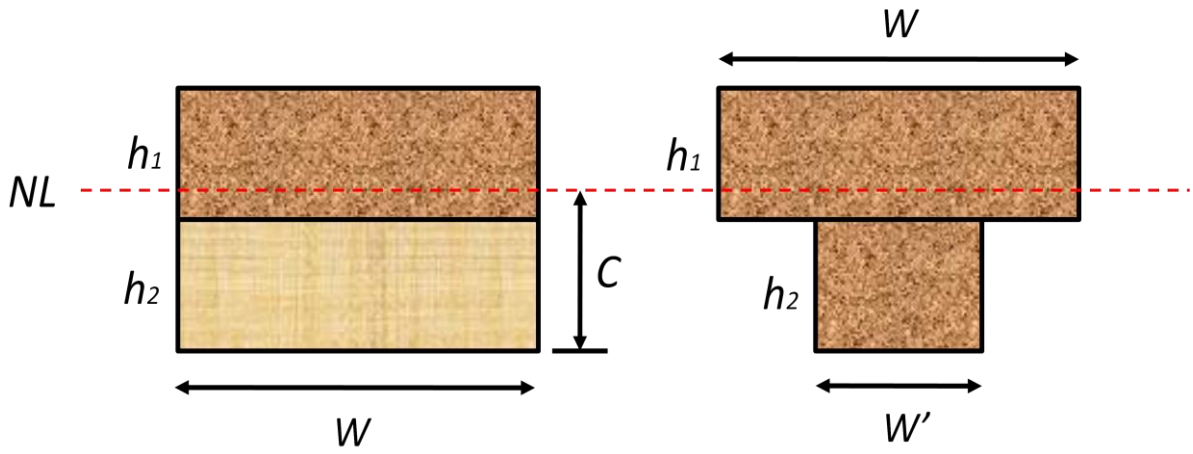
The total bending moment M at one end of the segment is:

$$M = \int_{-C}^{h-C} \sigma w x dx = \frac{E'}{R}\int_{-C}^{h-C} w x^2 dx = \frac{E'}{R} I_x \qquad (20)$$

where h is the thickness of the beam, C is the displacement from the bottom of the material beam to the NL, w is the width of the cross section and I_x is the second moment of area of the cross section.

From above, how to determine the position of the NL is the most critical problem. In a single-material, the position of NL is the centroidal axis of the cross section. If the structure comprises two or much more layers of different materials, just like the case in our fabricated device, it is necessary to consider the different Young's Modulus and Poisson's ratios of each layer property.

Figure.3-11 (a) shows the cross section of a structure with two different materials, assuming both layers have the same width *w* and different Young's modulus: E_1 and E_2.



(a) (b)

Figure 3-11: (a) Cross section of two-material beam; (b) Effective cross section of the left composite beam with pure top-layer material. The thickness of each layers are h_1 and h_2

The total bending moment is:

$$M = \int \sigma_1 w x dx + \int \sigma_2 w x dx = \frac{E_2'}{R}\int_{-C}^{h1-C} w x^2 dx + \frac{E_1'}{R}\int_{h1-C}^{h1-C+h2} w x^2 dx$$

$$= \frac{E_1'}{R}\left(\int_{-C}^{h1-C} w\frac{E_2'}{E_1'} x^2 dx + \int_{h1-C}^{h1-C+h2} w x^2 dx\right) \qquad (21)$$

C is the distance between NL and the bottom of substrate. Compared with Equation (20), the effective section is the original cross section of M_1 plus the cross section of M_2 with the new width *w'* which is given by: $w' = w\frac{E_2'}{E_1'}$

Thus, for the same case of longitudinal stress, a composite beam made up of different materials, as shown in Figure 3-11 (a), is possible to be seen as a pure beam, as shown in Figure 3-11 (b). Such method greatly simplifies the determination of centroidal axis position and avoids solving the complicated equation. Let us get back to the multi-layer structure of our own optimized HEMT device. The whole final structure layer and their parameters of mechanical properties are given in the Figure 3-12. All the Young modulus and ν Poisson's

ratio of each material are collected by references and product suppliers[10][11][12][13]. We calculate the reduced elastic modulus values directly by equation (13).

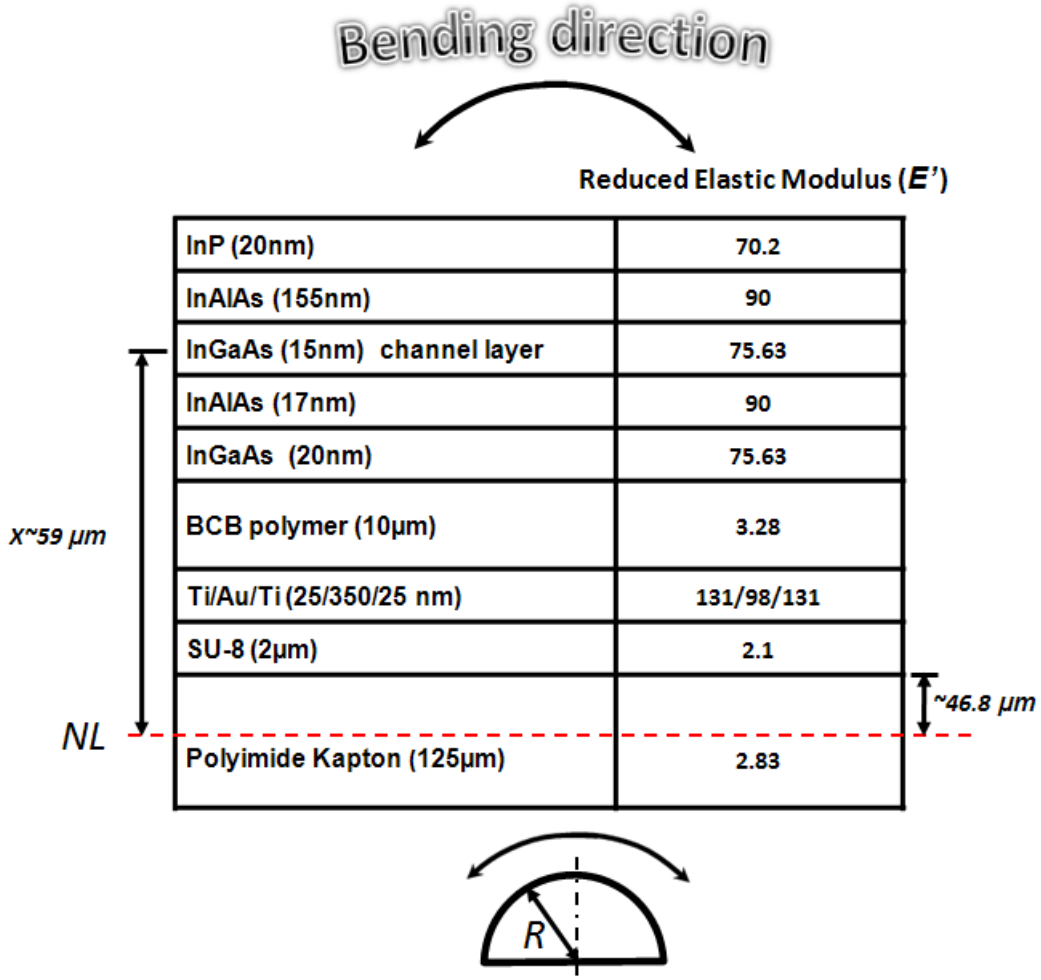


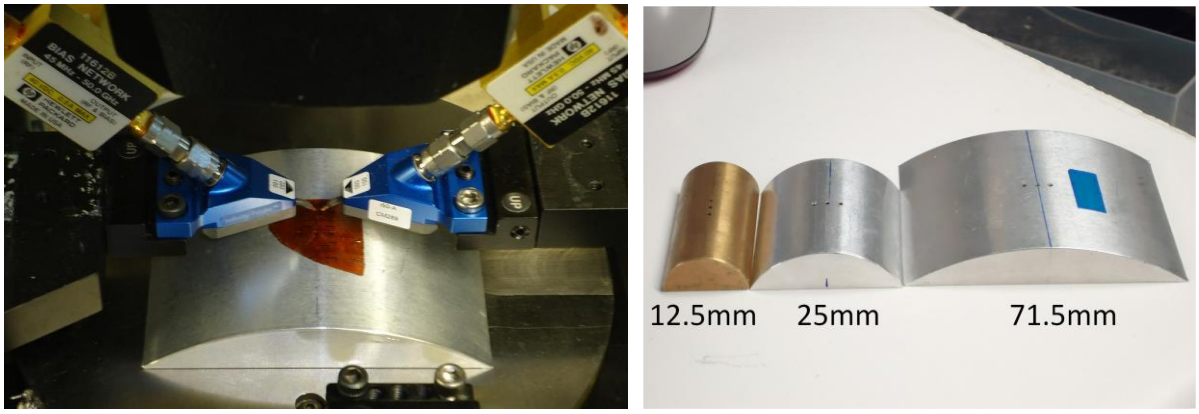
Figure 3-12: Approximate structure of our final upside-down HEMT device

Note that in the figure above, two extremely thin silicon δ-doping planes are neglected in this estimation. As the reduced elastic modulus E' of all layers are known, we are able to consider every different layer as an effective cross section according to the bottom layer polyimide Kapton, and then determine the NL layer position by calculating the centroidal axis of the "new" integration (Figure 3-10).

After defining the NL layer, the last step is to figure out the strain value with the help of equation (17). We choose the middle position of channel layer InGaAs for estimating the average strain value in the channel layer, as shown in Figure 3-10, the distance x is equal to about 59μm. In our case, we tend to measure three different bending radius: 71.5mm, 25mm and 12.5mm. So, the corresponding strain values (x/R) are about 0.08%, 0.23% and 0.47%.

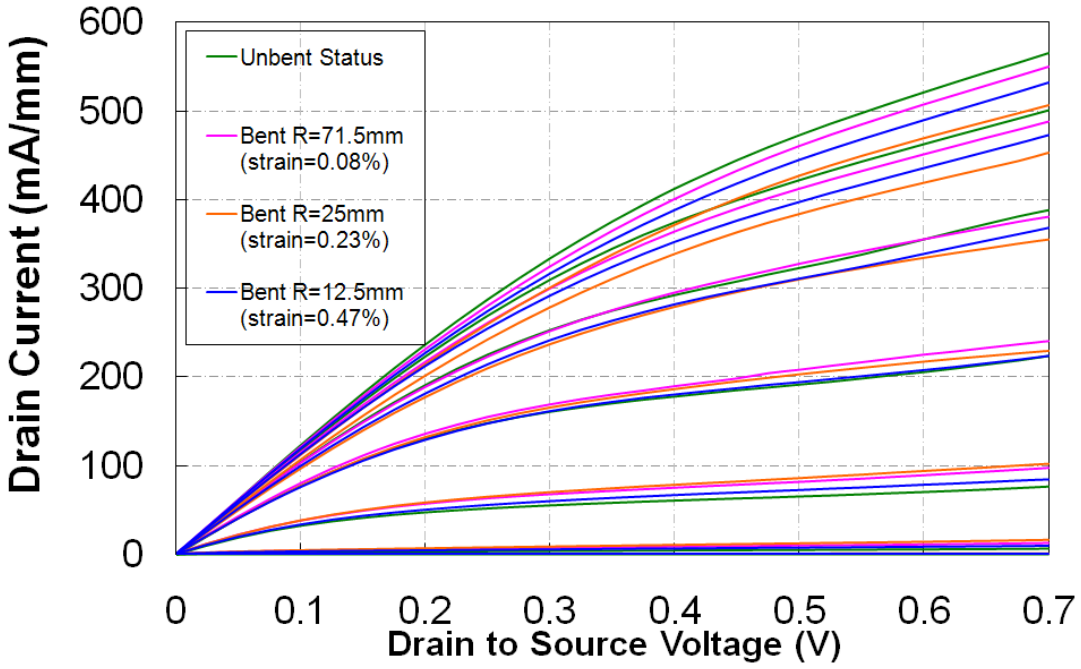
3.3.2 Measurement of different bending degrees

The influences of the substrate mechanical flexure on static and dynamic performance have been investigated. As shown in Figure 3-13 (a) (b), we have measured HEMT-FS by using an arc-shaped metal supports of various bending radius which allows to bend the flexible substrate during measurements. The small holes on the metal supports used for vacuum sucking ensure a good contact between the device under test and metal support surface. All measurements have been performed at room temperature and the bending induced strain has been applied along the gate width. Figure 3-14 (a) shows a sequence of current-voltage curves measured at different bending radius: 71.5 mm, 25 mm, and 12.5 mm with corresponding strain values 0.08%, 0.23% and 0.47% respectively calculated by the above mechanical modeling of multi-layers for flexible devices.

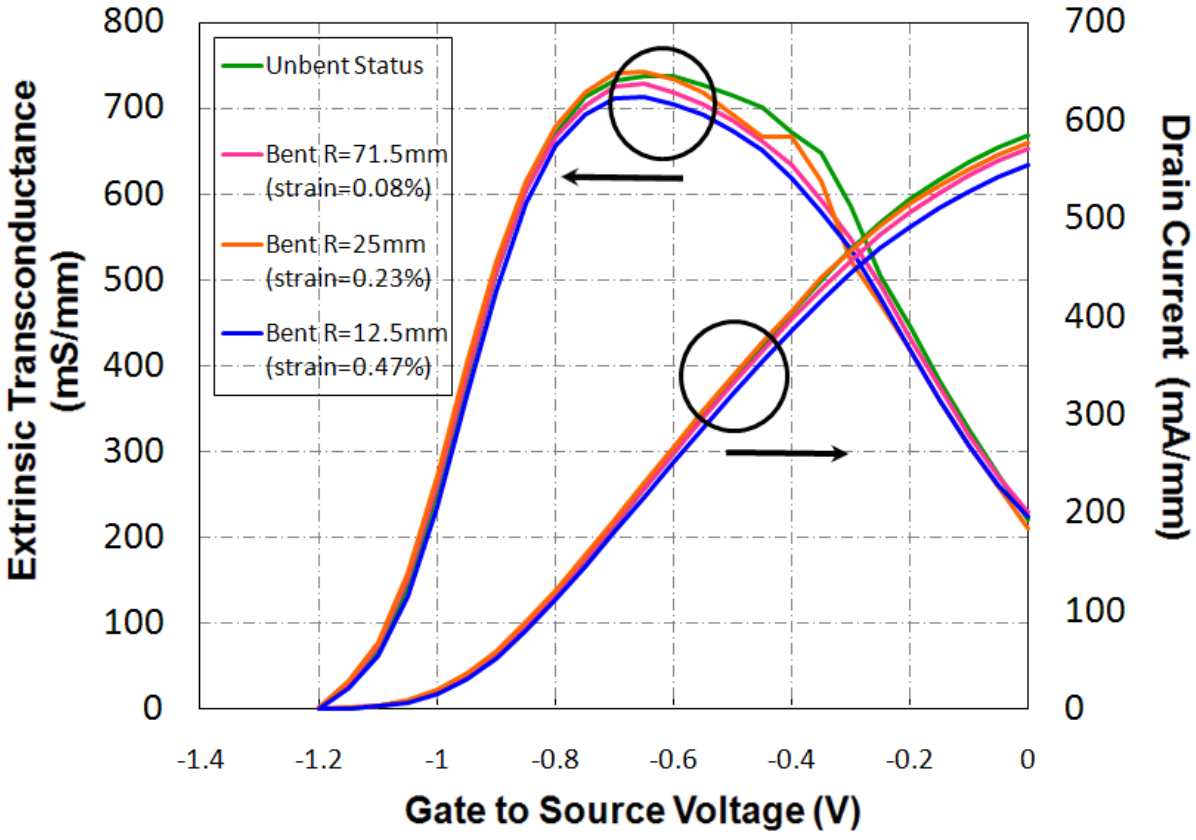


(a) (b)

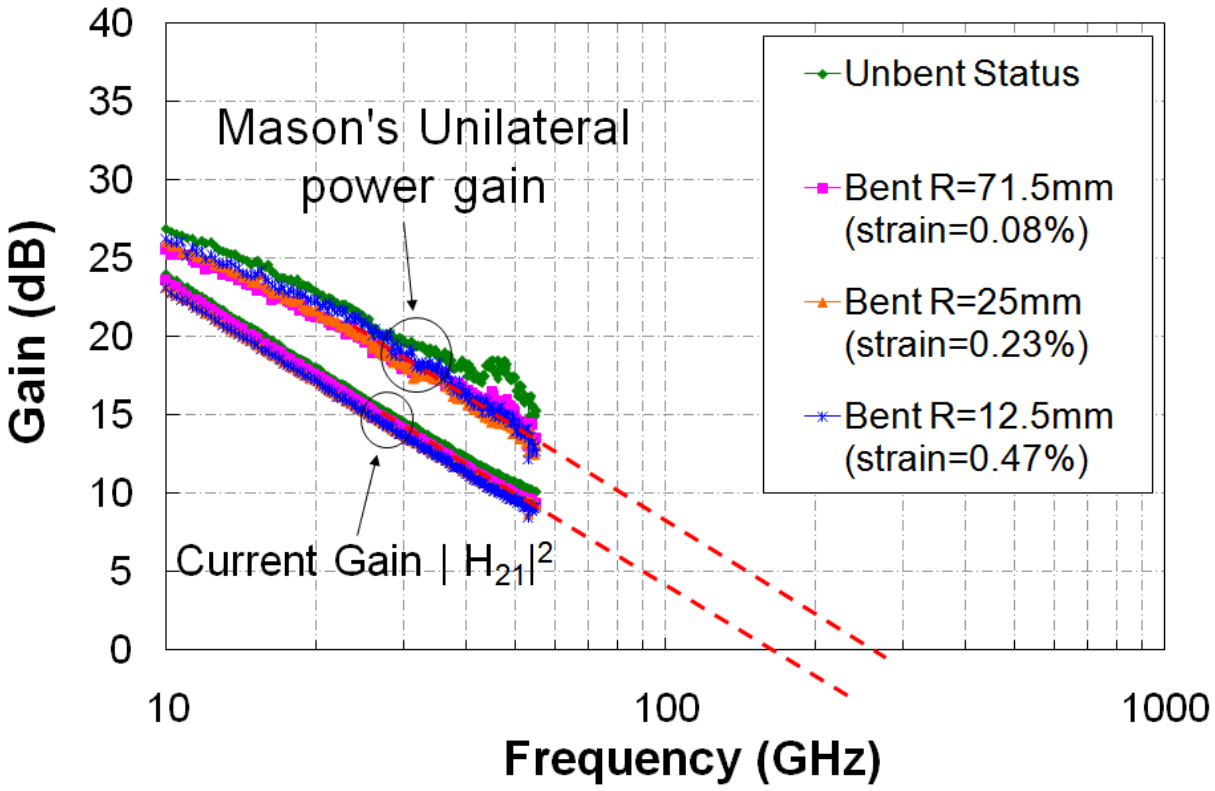
Figure 3-13: (a) Test bench for on wafer DC and RF measurement under bending conditions; (b) Various radii of metal supports for our measurement.



(a)



(b)



(c)

Figure 3-14: (a) Typical HEMT-FS I-V characteristics obtained for various bending radius (and their corresponding surface strains). Gate bias voltage is 0V for top curves and gate step is -0.2 V. (b) Transconductance characteristics of HEMT-FS at V_{DS}=0.7V for various bending radius (and their corresponding surface strains). (c) Frequency dependence of current gain $|H_{21}|^2$and Mason's unilateral power gain *Ug* at V_{DS}=0.7V for various bending radius (and their corresponding surface strains).

The slight difference between the four current-voltage curves suggests that HEMT-FS static characteristics are weakly affected by the bending conditions. Indeed, maximum change of drain current is lower than 13% for these three bending conditions. The transconductance *gm* is almost the same tendency from Figure 3-14 (b). Figure 3-14 (c) shows the comparison of frequency dependence microwave gains for these three bending conditions. One can observe that the decrease of bending radius leads to a slight decrease of f_T. Moreover, f_{MAX} of unbent status is higher than the other three bending status.

In order to interpret these results, for different bending conditions, the hall-bar measurements of active layers and the parameters of SSEC model are extracted.

Table 3-2 Hall-bar measurement of optimized HEMT-FS layer (Gate width direction)

	Unbent Status	71.5mm	25mm	12.5mm
Hall Mobility ($cm^2 \cdot V^{-1}S^{-1}$)	1.02×10^4	9.98×10^3	9.95×10^3	9.91×10^3
Hall Density (cm^{-2})	9.18×10^{12}	9.11×10^{12}	9.05×10^{12}	8.82×10^{12}
Sheet resistance (ohm/sq)	67.3	69	69.5	71

From the summary of Table 3-2, those similar extracted parameters in the active layers cannot give a reasonable explanation for the small difference of frequency performances. Thus, we try to shift the focus onto the relevant elements of SSEC models.

Note that de-embedding procedure of parasitic components has been performed under bending status for each bending radius. From Table 3-3, cut-off frequencies degradation for bent devices seems to be mainly attributed to the decrease of g_{mi} and/or *Rg* since no significant change in intrinsic resistances (*Rs* and *Rd*), output conductance g_d, and intrinsic capacitances (*Cgs* and *Cgd*) is observed. In order to confirm this hypothesis, calculated gains from extracted SSEC models using Advanced Design System (ADS) software have been done. The initial simulation model we established is shown in Figure 3-15. The obtained SSEC parameters under the unbent and highest bending radius conditions are input respectively.

Table 3-3 Extracted SSEC model and extrapolated f_T-f_{MAX} of 100 nm-gate HEMT-FS under various bending status

	Extrinsic Elements				
	Rg (Ω/mm)	**Rs (Ω.mm)**	**Rd (Ω.mm)**	**Cpg (fF/mm)**	**Cpd (fF/mm)**
Unbent Status	69	0.34	0.35	14	68
Bending radius 71.5mm	107	0.34	0.35	31	82
Bending radius 25mm	110	0.34	0.38	21	110
Bending radius 12.5mm	104	0.35	0.39	12	94

	Intrinsic Elements					**Frequency**	
	g_{mi} (mS/mm)	**g_d (mS/mm)**	**Cgs (fF/mm)**	**Cgd (fF/mm)**	**Cds (fF/mm)**	**f_T (GHz)**	**f_{MAX} (GHz)**
Unbent Status	1020	131	597	194	103	160	290
Bending radius 71.5mm	972	124	603	190	62	158	250
Bending radius 25mm	950	128	621	183	55	156	250
Bending radius 12.5mm	893	110	611	186	24	140	255

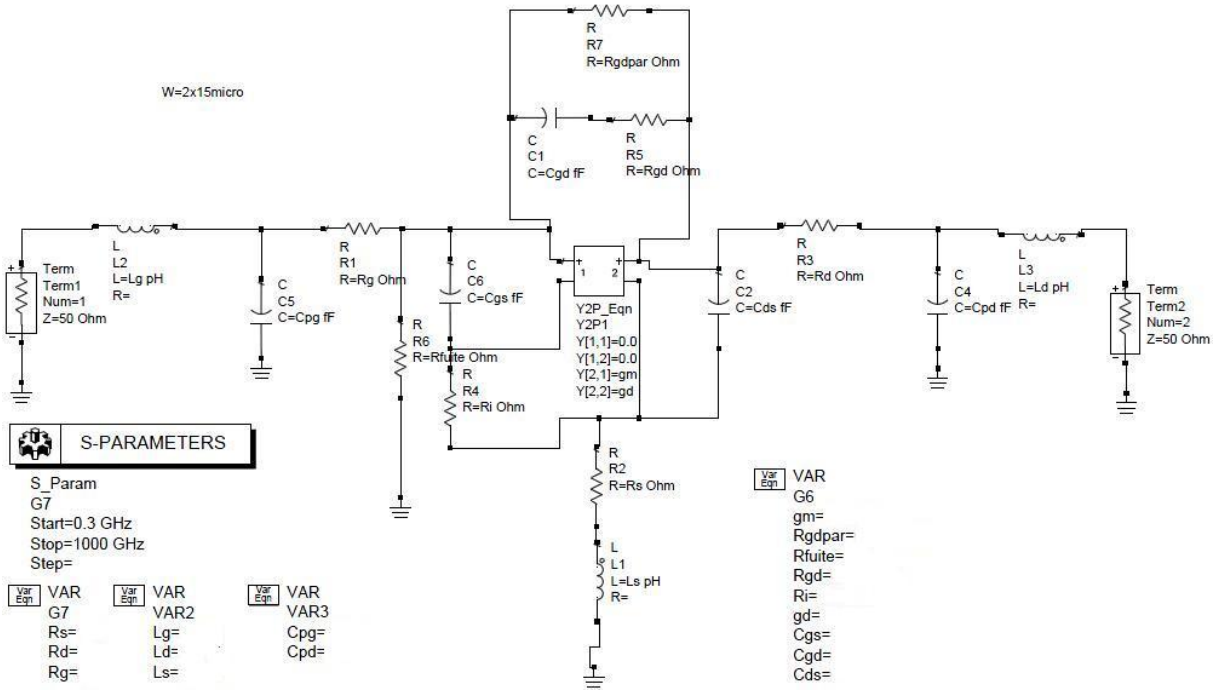
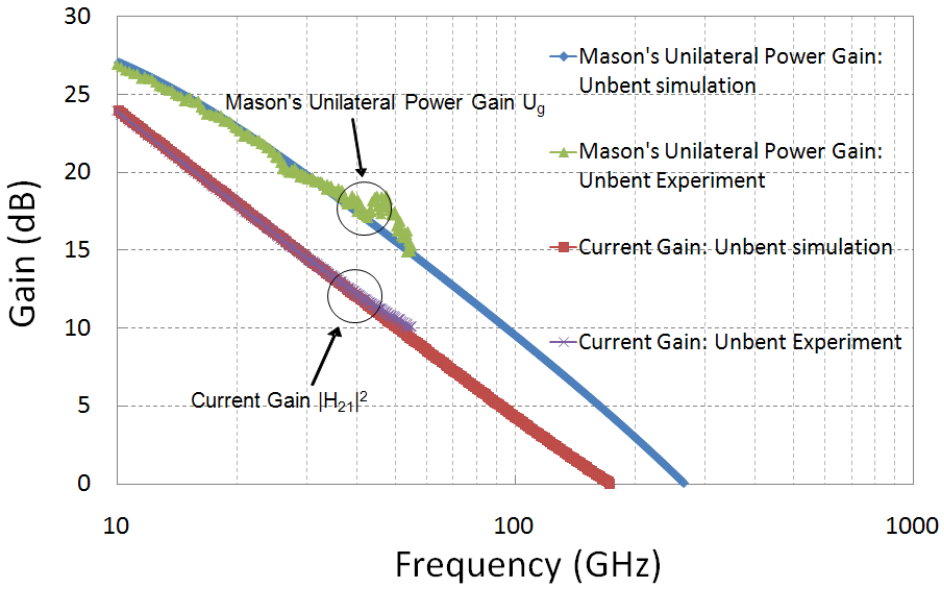
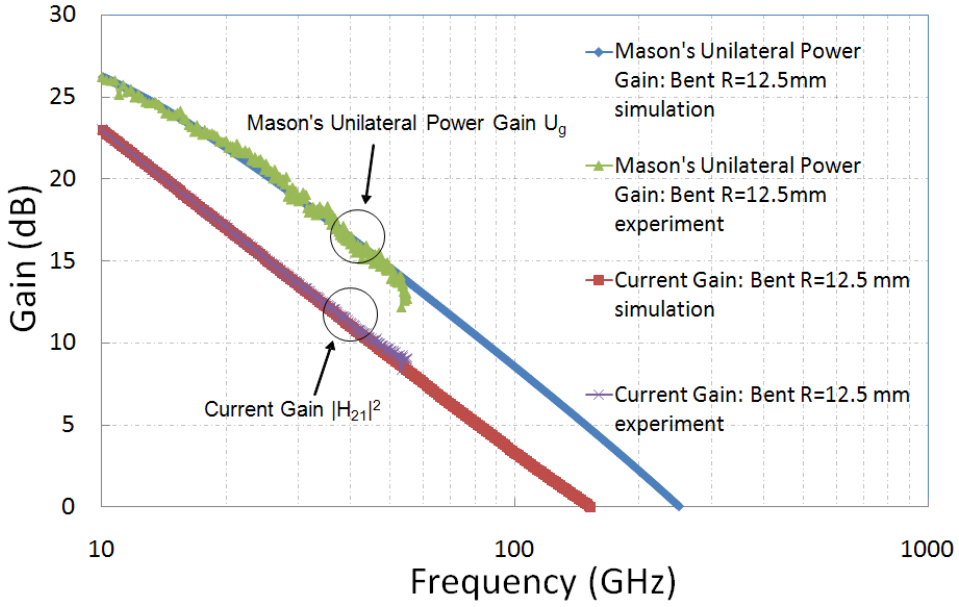


Figure 3-15: The basic model used in ADS simulation for unbent and bent conditions

First, to validate the approach used here, experimental frequency dependence of $|H_{21}|^2$ and Ug gains are compared with those obtained from ADS software for unbent condition and for the highest bending radius. We can observe that simulated results are in good agreement with experimental measurements with similar cut-off frequencies in Figure 3-16 (a) and (b), which validates our SSEC model.



(a)



(b)

Figure 3-16: Comparison of Mason's unilateral power gain *Ug* and current gain $|H_{21}|^2$ measured in fabricated 100 nm-gate HEMT-FS with those obtained from SSEC model: (a): for unbent condition, (b): for 12.5mm bending radius.

Next, in order to estimate the main element of SSEC responsible for cut-off frequencies degradation when strain is applied, $|H_{21}|^2$ and *Ug* gains have been calculated by modifying separately g_{mi} value and/or *Rg* value from unbent SSEC model without changing values of other electrical elements. For these simulations, g_{mi} and *Rg* have taken their respective values obtained for bent condition of R=12.5mm (i.e., 893mS/mm and 104Ω/mm, respectively). Table 3-3 summarizes cut-off frequencies obtained from theses simulations.

Table 3-3 Cut-off frequencies extracted from unbent SSEC model and from unbent SSEC model by changing g_{mi} and/or Rg values obtained with bending radius of 12.5 mm.

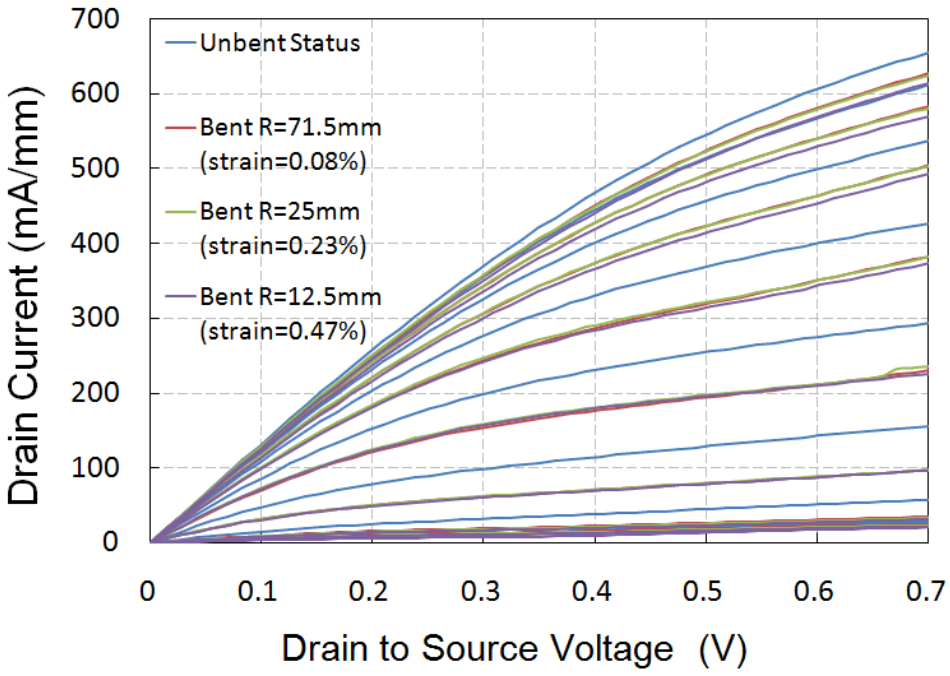
	Experimental results with R=12.5mm	Unbent SSEC model	Unbent SSEC model with gm_{bent}	Unbent SSEC model with Rg_{bent}	Unbent SSEC model with Rg_{bent} and gm_{bent}
f_T (GHz)	140	160	145	160	145
f_{MAX} (GHz)	255	290	275	280	260

From unbent SSEC model, by only changing g_{mi} value from unbent to bent condition (i.e., 1020mS/mm to 893mS/mm), f_T and f_{MAX} reach 145 GHz and 275 GHz, respectively. f_T is close

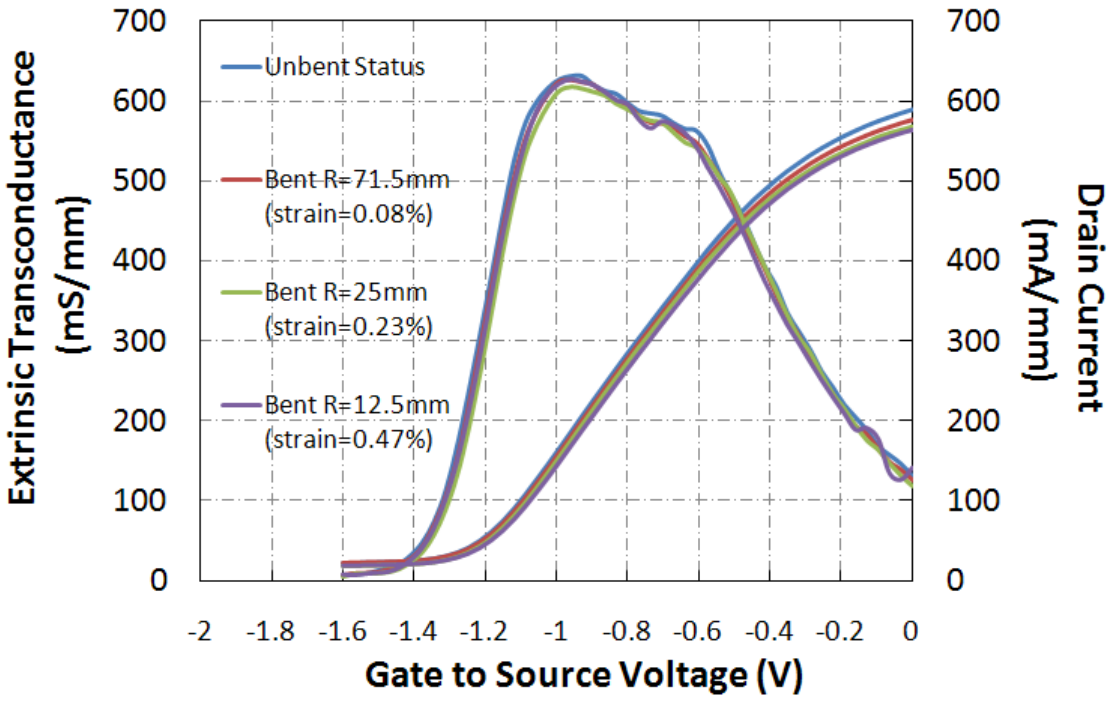
to experimental value (140 GHz) but f_{MAX} is relatively far away. In the same way, by only changing *Rg* value from unbent to bent condition (i.e., 69Ω/mm to 104Ω/mm), f_T and f_{MAX} reach 160 GHz and 280 GHz. In this case, only f_{MAX} is affected by the gate resistance degradation but large difference between experimental value (255 GHz) and simulated value (280 GHz) is observed. Finally, when *Rg* and g_{mi} are simultaneously modified, simulated and experimental results are similar. Consequently, this study shows RF performance degradation is related to the decrease of g_{mi} and *Rg* elements but g_{mi} degradation is mainly responsible of cut-off frequencies variation. g_{mi} decrease can be explained by the bending induced strain on the epitaxial layer which degrades the electron transport properties in the channel. Nevertheless, *Rg* degradation is not clear at this time.

3.3.3 Measurement of Different Bending Directions

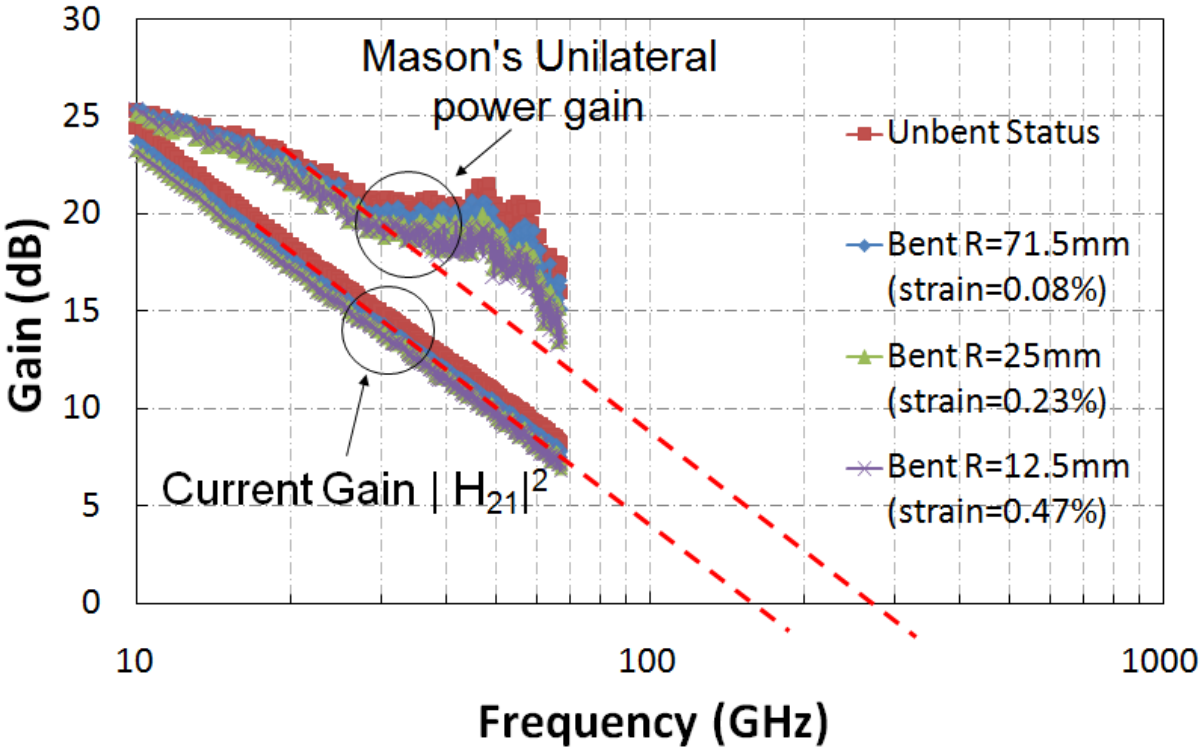
In order to seek more information related to the bent devices, the same measurement on the arc-shaped metal substrate has been performed once more but with a different bending direction: source-drain direction. When strain is applied along the source-drain direction, the similar electrical results have been obtained, showing in the Figure 3-17 (a), (b) and (c).



(a)



(b)



(c)

Figure 3-17: (a) Typical HEMT-FS current-voltage characteristics obtained for various bending radius with source-drain direction (and their corresponding surface strains). Gate bias voltage is 0V for top curves and gate step is -0.2 V. (b) Transconductance characteristics of HEMT-FS at V_{DS}=0.7V for various bending radius (and their corresponding surface strains).

(c) Frequency dependence of current gain $|H_{21}|^2$and Mason's unilateral power gain *Ug* at V_{DS}=0.7V for various bending radius (and their corresponding surface strains).

The HEMT-FS device is not influenced strongly under this bending condition as well. From the static characteristics shown in Figure 3-15 (a), maximum change of drain current is about 6% for these three bending conditions. Their transconductance values *gm* are almost the same as well. The comparison of frequency dependence microwave gains among these three bending conditions is shown in Figure 3-15 (c). A very slight degradation of those four curves is demonstrated. Because there is no large difference between any other extrinsic and intrinsic parameters from the Table 3-4 SSEC extraction, we believe that RF performance degradation is related to the small decrease of g_{mi}. This decrease of intrinsic transconductance g_{mi} is caused by the bending induced strain of the epitaxial active layers which tends to downgrade the electron transport properties in the channel layer.

Table 3-4 Extracted SSEC model and extrapolated f_T-f_{MAX} of 100 nm-gate HEMT-FS under various bending status (Source-Drain direction)

	Extrinsic Elements				
	Rg (Ω/mm)	**Rs (Ω.mm)**	**Rd (Ω.mm)**	**Cpg (fF/mm)**	**Cpd (fF/mm)**
Unbent Status	62	0.34	0.35	34	26
Bending radius 71.5mm	69	0.34	0.35	27	18
Bending radius 25mm	72	0.34	0.38	30	18
Bending radius 12.5mm	65	0.35	0.39	35	17

	Intrinsic Elements					**Frequency**	
	g_{mi} (mS/mm)	**g_d (mS/mm)**	**Cgs (fF/mm)**	**Cgd (fF/mm)**	**Cds (fF/mm)**	**f_T (GHz)**	**f_{MAX} (GHz)**
Unbent Status	876	141	448	200	158	160	280
Bending radius 71.5mm	848	140	459	196	127	156	270
Bending radius 25mm	837	127	468	197	141	152	260
Bending radius 12.5mm	820	135	472	200	131	150	260

Finally, the hall measurements of active layers for the various bending radius in source-drain direction are listed in Table 3-4, showing no big difference in the aspects of hall mobility, hall density and sheet resistance under distinct mechanical bending curvatures.

Table 3-5 Hall-bar measurement of our optimized HEMT-FS layer (Source-Drain direction)

	Unbent Status	71.5mm	25mm	12.5mm
Hall Mobility ($cm^2 \cdot V^{-1}S^{-1}$)	9.13×10^3	9.13×10^3	9.11×10^3	9.06×10^3
Hall Density (cm^{-2})	9.75×10^{12}	9.69×10^{12}	9.6×10^{12}	9.42×10^{12}
Sheet resistance (ohm/sq)	70.25	70.7	71.5	73.3

3.4 Conclusion of Chapter 3

In the last chapter, at first, the Kink Effect mechanism caused the abnormally low static drain current in our previous work is presented and explained thoroughly. We succeed in improving our electrical performances and eliminate the Kink Effect by optimizing our HEMT epitaxial layer structure. The improved transistor exhibits the much higher drain current (580mA/mm) and high cut-off frequencies behavior (f_T=160 GHz, f_{MAX}=290 GHz) in unbent condition. Moreover, measured devices for various bending radius show no obvious electrical degradation (lower than 15%). Figure 3-18 provides a state of the art concerning the cut-off frequency of flexible transistors as a function of the minimal achievable curvature in the recent publications.

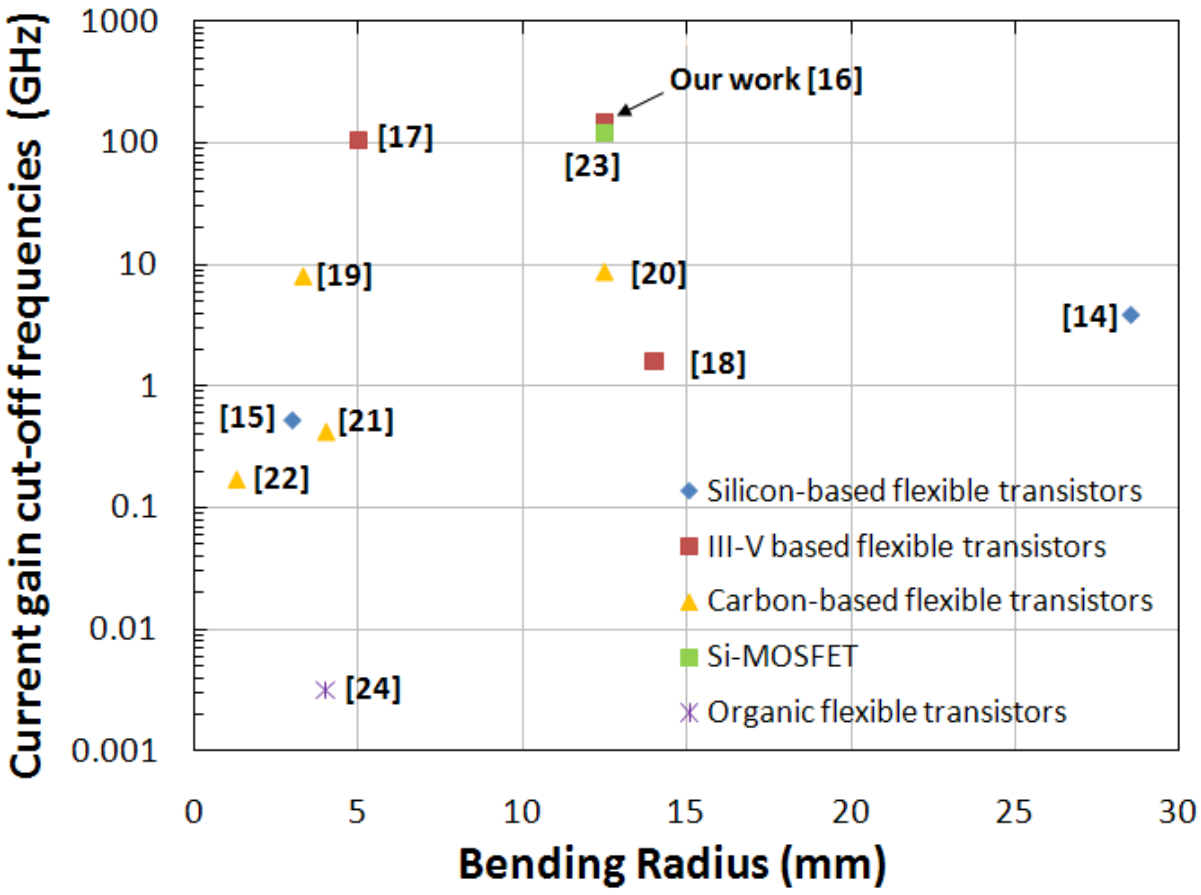


Figure 3-18: Current gain cut-off frequency of flexible transistors as a function of the minimal bending radius in the recent development of high-frequency flexible transistors [14]-[24]

Our work develops the high frequency performance (f_T~140GHz and f_{MAX}~250) of HEMT components under flexure with bending radius of 12.5mm. By means of SSEC model, RF

performance degradation in the bending direction of gate width has been attributed to the decrease of g_{mi} and Rg.

Furthermore, the acceptable slight change of electrical performances in different bending directions (source and drain direction) enhance the feasible bending properties of our devices. All the above characteristics pave the highly promising way to integrating large-area radio-frequency communication devices and high-speed processing units onto the flexible substrate.

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Conclusion and Perspectives

The objective of this work is to propose a feasible strategy and open up the possibility to integrate high-frequency systems and applications onto the flexible devices. By means of transfer-and-bonding technique, the bendable transistors achieve fabulous microwave performances comparable to those obtained by traditional HEMT on rigid substrate.
All the research operations have been carried out in the *IEMN* clean room and supported by high-frequency characterization facilities of *IEMN*.

Conclusion

The dissertation starts with the great interest in flexible electronic coming from current semiconductor industries. The existing fabrication technologies in the literature for realizing flexible transistors or circuits are reviewed in details. The results of their high frequency performances are highlighted as the key point of comparison. Moreover, the capabilities of electrical performances under different bending radii have also been commented.
Flexible devices based on organic materials and printed electronics have the advantage of low cost and large area. However, those strategies are limited by their poor carrier mobility and relatively low printing resolution, which cannot satisfy with high operating frequency and tightly packed logic circuit design. In order to break such frequency restrictions, the transfer of conventional inorganic semiconductors material onto flexible substrate is able to provide much higher frequencies which enter into the gigahertz level.
Nevertheless, their strategies of direct fabrication on flexible materials risk the deformation of flexible substrate under high temperature manufacturing, which leads to the misalignment and limits complex interconnection network. Therefore, under such circumstances, the method proposed in this work relies on the direct transfer of fabricated III-V high electron mobility transistors onto plastic substrate in order to avoid possible technology problems and make breakthrough.
As shown in state of the art, HEMTs based on III-V materials have been showing the strength of high frequency performances in wide electronic applications. Benefiting from the $In_{0.53}Ga_{0.47}As$ material whose electron mobility reaches $1.2 \times 10^4 cm^2V^{-1}s^{-1}$ and its high saturation speed (2.7×10^7cm/s), we tend to realize HEMT devices based on this potential candidate for obtaining high frequency utilization and low voltage supply.

In the chapter 2 of thesis, fabrication scheme of HEMT-FS (FS: Flexible Substrate) is presented step by step. Owing to the mature III-V fabrication technologies, we establish conventional 100nm-gate HEMT using InGaAs as channel layer on the rigid III-V wafer

beforehand. TFMS access line is elaborately designed for the essential HF measurements afterwards. By connecting two sides of source bonding pads on the BCB polymer island, 50Ω impedance matching is realized on the flexible substrate. The subsequent transfer-and-bond handling process is realized by SU-8 adhesive layer under vacuum ambience. The upside-down devices are eventually integrated onto the Kapton polyimide substrate after removing the substrate and etch-stop layer. Back side contact is exposed for our electrical characterizations in static and dynamic regime.

For the preliminary HEMT-FS device, due to partial channel depletion, the maximum drain current I_{dMAX} 210mA/mm and the maximum extrinsic transconductance g_m 800mS/mm are achieved at V_{DS} =1.2V. At lower V_{DS}, the transconductance is only ~200mS/mm. The difference is attributed to kink effect phenomenon. Indeed, the transconductance is overestimated at high V_{DS} by the apparition of kink effect. The true effective extrinsic transconductance g_m without Kink effect influence is calculated by the extracted intrinsic transconducatance g_{mi}. These electrical characteristics are lower than those of HEMT on the rigid substrate. In terms of RF performance, high cut-off frequencies are f_T=120GHz and f_{MAX}=280 GHz have been obtained respectively, which exhibit performance competitive with the rigid counterparts (f_T and f_{MAX} are 203 GHz and 215 GHz). The optimization of fabrication procedures and/or device epitaxial layers is expected in order to overcome the negative Kink effect and ameliorate the device electrical performances.

In the chapter 3, the mechanism of Kink effect is stated in details. The optimized epitaxial layers based on the increase of electron concentration inside the channel layer are proposed for eliminating the Kink Effect phenomenon. The improved HEMT-FS provides higher maximum drain current I_{dMAX} 580mA/mm and maximum extrinsic transconductance *gm* 750mS/mm while the new devices get rid of the Kink effect completely. Besides, cut-off frequencies behavior f_T /f_{MAX} as high as 160/290 GHz on polyimide substrate are well demonstrated. The parameters of small signal equivalent circuit are extracted from both the first work and optimized work for comparison. Those better RF performances are attributed to the reduction of both source and drain resistances and higher extrinsic transconductance g_m in high frequency.

After studying the unbent sample of HEMT-FS, the impact under flexure has been taken into account. The neutral plane methodology for calculating the strain values of our bending multilayer structure is discussed. Three various bending radii (71.5mm, 25mm and 12.5mm) of arc-shaped metal support are applied for their DC and RF measurements. Both bending directions of source-drain and gate width are considered. Measured devices under different

bending conditions show similarity of electrical characterizations in Hall-bar measurements, drain current, extrinsic transconductance and cut-off frequencies. The slight decrease of extracted intrinsic transconductance g_{mi} is attributed to the different bending induced strain inside the device layers. It influences the intrinsic electron transport properties, which leads to the small degradation of radio-frequency performances as well.

In conclusion, to our best knowledge, our work proposes the highest frequency performance level in the field of flexible transistors, particularly the f_{MAX}. With the feasible bending electrical characteristics, the solution provides the possibility to realize high-frequency communications, process units and more complex circuits on the flexible substrate.

Perspectives

So far, our research work only represents the basic building block for converting rigid circuits into flexible circuits. Further development of flexible electronics is expected to occur through the development of more complex integrations on flexible foil which customize for various applications such as sensors, antennas, batteries and logic/memory applications etc.

In our future work, firstly, we tend to focus on the high frequency performances of passive devices transferred onto flexible film. It is essential to demonstrate their performance under flexure before adopting them in the larger specific circuit on flexible substrate. Afterwards, through the acquired transfer-and-bond technique, the design of amplifier or detector based on our III-V HEMT devices could also be studied on bendable substrate. Finally, integration of heterogeneous device technology on the flexible substrate, integrating Si-CMOS and other components (antennas, sensors, batteries, display) onto flexible foil with signal processing would be a possible accomplishment for expanding the current scope functions supported by use of only rigid circuits.

Besides, at the same time, seeking improved manufacturing technologies to produce flexible circuits with cost-efficient materials and fewer manufacturing steps is also a direction for the long-term development of consumer flexible electronic devices.

Appendix

The initial wafer cleanliness is done in Acetone (2min) and IPA (2min)

1. Realization of ohmic contact

i. Bilayer resists: EL 13% MAA8.5 3000/1000/12'' anneal 200℃ 10min
PMMA 3% 495K 3500/1000/12'' anneal 200℃ 10min

ii. E-beam lithography with 50kV and dose 180μC/cm^2

iii. Developing in MIBK/IPA (1:2),1min + IPA, 30sec

iv. Metallization: Ni/Ge/Au/Ni/Au (25/400/800/50/600)Å
Etching by Argon (150eV, 1min)

v. Lift-off in Acetone

vi. Recuit RTA (295 ℃ 20 sec)

2. Mesa isolation

i. AZ 1518 (3500/1000/12'') + anneal 110℃ 1min

ii. Optical lithography (3sec under 9mW/cm^2)

iii. Developing in AZ400/H_2O (1:3) during 40sec + EDI water cleaning

iv. Wet-etching in $H_3PO_4/H_2O_2/H_2O$ (5:1:40) , 2min30sec + HCl/H_2O(2:1), 10sec

v. The depth of etching process (~2720Å) is confirmed by profilometer.

3. Bonding pads deposition

i. Bilayer resists: EL 13% MAA8.5 2800/1000/12'' anneal 200℃ 10min
PMMA 3% 495K 3400/1000/12'' anneal 200℃ 10min

ii. E-beam lithography with 100kV and dose 290μC/cm^2

iii. Developing in MIBK/IPA (1:2),1min 15sec+ IPA, 1min

iv. Ti/Au/Ti (250/3500/250) Å Etching by Argon (150eV, 1min)

v. Lift-off in Acetone

4. Added bonding pads for repairing fissure arising from the first bonding pads on the mesa

The same process as the above bonding pads deposition, except that the metallization thickness is changed: Ti/Au/Ti (250/1500/250) Å

5. Gate realization

i. Promoter: HMDS (3000/1000/12'')

Bilayer resists: ARP 950 4% (3600/1000/8'') anneal 200℃ 10min

COPO ARP 33% (1600/1000/8'') anneal 200℃ 10min

ii. E-beam lithography with 100kV and
- Dose 280μC/cm^2 for gate access
- Dose 185μC/cm^2 for gate foot (coef: 3.5)
- Dose 185μC/cm^2 for spacer (coef: 0.5)
- Dose 185μC/cm^2 for lateral (coef: 1.7)

iii. Developing in MIBK/IPA (1:2), 2min + IPA, 1min

iv. Wet-etching for gate recess: HCl/H_2O (1/10), 35''

AS/H_2O_2 (30/4), 1min+EDI water, 2min

v. Metallization: Ti/Pt/Au/Ti (250/250/3250/250)Å

Etching by Argon (150eV, 1min)

vi. Lift-off in Acetone

6. Thin film micro-strip (TFMS) access lines fabrication

i. BCB 4026-46 deposition：

Promoter: AP3000 (500/1/10'' + rinse 3000/3/30'')

BCB 4026-46 (2500/3/30'')

ii. Baked in oven 80℃ for 30min

iii. Optical lithography (60mJ/cm^2/μm), in our case, before final hard bake, BCB thickness is ~15μm

iv. Puddle developing by DS2100:

1) Dispense onto the wafer without spinning
2) Waiting for 4 min and rinse by spinning (500/1/10'') while a stream of DS2100 is dispensed onto the center of the wafer
3) Final rinse at 2000/3/30''

4) If it is not clean enough, the above developing process should be redone but reducing the wait (1 min) during process 2)
5) Hard bake in oven at 230℃ for 80min

v. Metallization:

1） Resists: Three layers EL 13% MAA 8.5% (2000/1000/12), anneal 120℃, 2min after each deposition
+ One layer PMMA 3% 495K (2000/1000/12), anneal 120℃ 1min30s

2) E-beam lithography with 50kV and dose 280μC/cm^2

3) Ti//Au/Ti (250/8000/250) Å Etching by Argon (150eV, 1min)

vi. Lift-off in Acetone

7. Transfer bonding technique

1) Spinning SU-8 (2002) onto Kapton (3000/3/30'')
2) Spinning SU-8 (2010) onto wafer surface (2500/3/30'')
3) Bonding process realized in (80℃, 30min) by ***Wafer Substrate Bonding Unit*** **(LOGITECH)**
4) Anneal 95℃, 5min

8. InP substrate and etch-stop layer removal

Wet-etching: HCl/H_2O (2:1), 1 hour and 30 min

H_3PO_4/H_2O_2/H_2O (5:1:40), 2min 30sec

Publications and Presentations

[1] ***J. Shi***, N. Wichmann, Y. Roelens, and S. Bollaert, "Microwave performance of 100nm-gate $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ high electron mobility transistors on plastic flexible substrate," ***Appl. Phys. Lett.***, vol. 99, no. 20, pp. 203505, Nov. 2011

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[3] ***J. Shi***, N. Wichmann, Y. Roelens, and S. Bollaert, "100nm-gate InAlAs/InGaAs HEMTs on plastic flexible substrate with high cut-off frequencies," ***24th International Conference on Indium Phosphide and Related Materials***, Aug. 27-30, 2012, Santa Barbara, CA, U.S.A.

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[6] ***J. Shi***, N. Wichmann, Y. Roelens, and S. Bollaert, "High frequency performance of 100nm-gate InGaAs/InAlAs high electron mobility transistors on polyimide flexible substrate," ***21th European workshop on Hetero-structure Technology***, Nov 5-7, 2012, Barcelona, Spain

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[9] ***J. Shi***, N. Wichmann, Y. Roelens, and S. Bollaert, "Réalisation et caractérisation de transistors à effet de champ à hétérojonction de la filière InAlAs/InGaAs sur substrat flexible," ***18th Journée Nationale Microondes***, May 14-17, 2013, Paris, France (Poster)

[10] S. Bollaert, ***J. Shi***, N. Wichmann, Y. Roelens, and, "Bending Effect on frequency performance of InAlAs/InGaAs HEMT transferred on flexible substrate," ***Device Research Conference***, June 23-26, 2013, University of Notre Dame, IN, U.S.A. (Poster)

Abstract

Fabrication and characterization of InAlAs/InGaAs high electron mobility transistors on plastic flexible substrate

The development of future flexible electronics requires combining high electrical performance devices (i.e. millimeter and sub-millimeter wave electronic devices) with mechanical flexibility. However, a variety of existing technologies such as organic thin film transistors, amorphous silicon, and polycrystalline-silicon are limited by their poor transport properties. High electron mobility transistors (HEMTs) based on III-V materials have been used in the field of ultra-high frequency microwave applications for a long time. This work develops a feasible method for transferring conventional HEMTs onto the flexible substrate. By the means of adhesive bonding technique, 100nm-gate InAlAs/InGaAs HEMTs have been transferred onto polyimide film (Kapton) and electrically characterized in static and dynamic regime. Through the epitaxial layers optimization, finally, the fabricated devices are able to suppress Kink effect and provide high cut-off frequencies (f_T=160GHz and f_{MAX}=290GHz) in unbent condition. These microwave characteristics are comparable to those obtained on 100nm-gate HEMTs on rigid substrate. Moreover, measured devices for various bending radius and bending directions show no obvious electrical degradation (lower than 15%).

Key words: flexible electronics, III-V, HEMT, microwave performances, mechanical bending strain, radio frequency transistors, InP substrate

Résumé

Réalisation et caractérisation de transistors à effet de champ à hétérojonction de la filière InAlAs/InGaAs sur substrat plastique flexible

Le développement de produits électroniques flexibles futurs nécessite la combinaison de hautes performances électroniques (ondes millimétriques et sub-millimétriques) avec une bonne flexibilité mécanique. Cependant, l'inconvénient majeur des matériaux utilisés pour concevoir ces transistors flexibles est leurs faibles mobilités des porteurs, limitant les performances fréquentielles. Les transistors à haute mobilité d'électrons (HEMT) à base de matériaux III -V ont été utilisés dans le domaine des applications hyperfréquences depuis longtemps. Ce travail présente une méthode possible pour transférer des HEMT classiques sur substrat flexible. Par un procédé de collage adhésif, des HEMT InAlAs/InGaAs de longueur de grille 100nm ont été transférés sur un film flexible et caractérisés électriquement en régime statique et dynamique. En optimisant la structure épitaxiale, d'excellentes fréquences de coupure ont été obtenues avec un f_T=160GHz et un f_{MAX}=290GHz. Cette optimisation de la structure de couche a permis de supprimer l'effet Kink. Ces performances sont comparables aux résultats obtenus sur des transistors HEMT sur substrat rigide de même dimension et de filière identique. Par ailleurs, les mesures électriques pour différents niveaux de déformation et différent directions de flexion démontrent très peu de dégradation électrique (inférieure à 15 %).

Abstract

Fabrication and characterization of InAlAs/InGaAs high electron mobility transistors on plastic flexible substrate

The development of future flexible electronics requires combining high electrical performance devices (i.e. millimeter and sub-millimeter wave electronic devices) with mechanical flexibility. However, a variety of existing technologies such as organic thin film transistors, amorphous silicon, and polycrystalline-silicon are limited by their poor transport properties. High electron mobility transistors (HEMTs) based on III-V materials have been used in the field of ultra-high frequency microwave applications for a long time. This work develops a feasible method for transferring conventional HEMTs onto the flexible substrate. By the means of adhesive bonding technique, 100nm-gate InAlAs/InGaAs HEMTs have been transferred onto polyimide film (Kapton) and electrically characterized in static and dynamic regime. Through the epitaxial layers optimization, finally, the fabricated devices are able to suppress Kink effect and provide high cut-off frequencies (f_T=160GHz and f_{MAX}=290GHz) in unbent condition. These microwave characteristics are comparable to those obtained on 100nm-gate HEMTs on rigid substrate. Moreover, measured devices for various bending radius and bending directions show no obvious electrical degradation (lower than 15%).

Key words: flexible electronics, III-V, HEMT, microwave performances, mechanical bending strain, radio frequency transistors, InP substrate

Résumé

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Le développement de produits électroniques flexibles futurs nécessite la combinaison de hautes performances électroniques (ondes millimétriques et sub-millimétriques) avec une bonne flexibilité mécanique. Cependant, l'inconvénient majeur des matériaux utilisés pour concevoir ces transistors flexibles est leurs faibles mobilités des porteurs, limitant les performances fréquentielles. Les transistors à haute mobilité d'électrons (HEMT) à base de matériaux III -V ont été utilisés dans le domaine des applications hyperfréquences depuis longtemps. Ce travail présente une méthode possible pour transférer des HEMT classiques sur substrat flexible. Par un procédé de collage adhésif, des HEMT InAlAs/InGaAs de longueur de grille 100nm ont été transférés sur un film flexible et caractérisés électriquement en régime statique et dynamique. En optimisant la structure épitaxiale, d'excellentes fréquences de coupure ont été obtenues avec un f_T=160GHz et un f_{MAX}=290GHz. Cette optimisation de la structure de couche a permis de supprimer l'effet Kink. Ces performances sont comparables aux résultats obtenus sur des transistors HEMT sur substrat rigide de même dimension et de filière identique. Par ailleurs, les mesures électriques pour différents niveaux de déformation et différent directions de flexion démontrent très peu de dégradation électrique (inférieure à 15 %).