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MULTIPLE RATES MULTIPLE PATHS WIDEBAND DIGITAL TRANSMITTER WITH LOW SPURIOUS EMISSIONS APPLIED TO OPPORTUNISTIC RADIO

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Abstract

All-digital RF transmitters for software defined radio based on multi-path architecture

Wireless communication terminals are evolving towards multi-standard terminals. One of the challenges is to use the best standard available at the right moment. The transmit part of a frequency agile cognitive radio must be highly reconfigurable in order to transmit information in an unused spectral zone and to use the suitable standard to obtain the optimum communication. The most critical element in a transmitter is the power amplifier and its interface with the antenna. Key problems that need to be addressed by the Power Amplifier (PA) are the linearity, ability to deliver power to the antenna and efficiency. In this work a digital transmitter based on a digitally controlled power amplifier (DPA) is investigated, and a prototype has been implemented to prove the feasibility of the concept. The DPA is mostly used in polar transmitters rather than Cartesian ones.

The proposed architecture is based on multi-path approach with different sample rate conversions. This diversity of sample rates helps to manage the spurious emissions due to the direct digital to RF conversion performed by the DPA without the need of passive filters. The transmitters implemented in advanced CMOS process are commonly based on multiple paths architecture. The approach proposed in this work takes advantage of this parallel structure to generate several signals with the same information but with different sample rates.

The LTE standard has been taken as the standard example, and a 2-path digital envelope modulator has been designed in a 65nm CMOS technology. The baseband sample rate conversions and control logic have been implemented on FPGA. The path recombination is performed with off-board components.

The fabricated prototype digital envelope modulator IC demonstrates the image attenuation principle with up to 6 dB attenuation. The DPAs support four sample rates {100 MS/s; 133 MS/s; 152 MS/s; 160MS/s}. The amplifier delivers up to 16.7 dBm over a 0.9 - 1.9 GHz band while providing 12.4% PAE and a -28 dB EVMrms. The prototype was tested with a 10 MHz LTE and a 20 MHz 802.11g standards.

The total circuit occupies 1.04 mm^2 and the area dedicated to the DPA and control logic only occupies 0.25 mm^2.

Keywords: digital power amplifier, polar architecture, multi-path, multi-rate, sample-rate conversion, digital transmitter, software defined radio, LTE, 65nm CMOS

This thesis work has been performed in the Integrated Circuits Design group of the ISEN department of the Institut d'Electronique, de Microélectronique et de Nanotechnologies (IEMN), 41 bd Vauban, 59000 Lille, France.

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Glossary

ACLR	:	Adjacent Channel Leakage Ratio
ACPR	:	Adjacent Channel Power Ratio
ACW	:	Amplitude Code Word
ADC	:	Analog to Digital Converter
ADPLL	:	Al-Digital PLL
AltCPR	:	Alternate Channel Power Ratio
AM	:	Amplitude Modulation
ARCEP	:	Autorité de Régulation des Communications Electroniques et des Postes
BP	:	Band-Pass
BPF	:	Band-Pass Filter
BW	:	Bandwidth
CDMA	:	Code Division Multiple Access
Clk	:	Clock
CM	:	Common Mode
CMOS	:	Complementary
CORDIC	:	COordinate Rotation Digital Computer
CR	:	Cognitive Radio
CP1	:	1 dB Compression Point
DAC	:	Digital to Analog Converter
DCO	:	Digitally Controled Oscillator
DCS	:	Digital Cellular System
DDR	:	Double Data Rate
DE	:	Drain Efficiency
DEM	:	Digital Envelope Modulator
DM	:	Differential Mode
DNL	:	Differential Non Linearity
DPA	:	Digital PA or Digitally controled PA

DRFC	:	Digital to RF Converter
DSP	:	Digital Signal Processing
DUT	:	Device Under Test
DVB	:	Digital Video Broadcasting
EDGE	:	Enhanced Data Rates for GSM Evolution
EER	:	Envelope Elimination and Restoration
EM	:	Emission Mask
E-UTRA	:	Evolved Universal Terrestrial Radio Access
EVM	:	Error Vector Magnitude
FW	:	Frequency Code Word
FDD	:	Frequency Division Duplexing
FFT	:	Fast Fourier Transform
FIFO	:	First In First Out
FIR filter	:	Finite Impulse Response filter
FOH	:	First Order Holder
FPGA	:	Field-Programmable Gate Array
G	:	Gain
GMSK	:	Gaussian Minimum Shift-Keying
GPRS	:	General Packet Radio Service
GPS	:	Global Positionning System
GSM	:	Global System for Mobile Communications
HDR	:	Hardware Defined Radio
HSDPA	:	High Speed Downlink Packet Access
HSPA+	:	High Speed Packet Access
HSUPA	:	High Speed Uplink Packet Access
IIP3	:	Input 3rd order Intercept Point
IIR filter	:	Infinite Impulse Response filter
IL	:	Insertion Loss
IM	:	Inter Modulation
INL	:	Integral Non Linearity
IP3	:	Third order Intercept Point
IPD	:	Integrated Passive Device
ISM	:	Industrial Scientific and Medical radio bands
LINC	:	LINear amplification with non-linear Components

LO	:	Local Oscillator
LP	:	Low-Pass
LPF	:	Low-Pass Filter
LSB	:	Least Significant Bit
LTE	:	Long Term Evolution
LUT	:	Look Up Table
LVDS	:	Low Voltage Differential Signaling
MMS	:	Multimedia Messaging Service
MN	:	Matching Network
MSB	:	Most Significant Bit
NFC	:	Near Field Communication
NL	:	Non Linearity
OFDM	:	Orthogonal Frequency-Division Multiplexing
OIP3	:	Output 3rd order Intercept Point
OR	:	Opportunistic Radio
OSR	:	Over Sampling Ratio
P1dB	:	Output power at 1 dB Compresion point
PA	:	Power Amplifier
PAE	:	Power Added Efficiency
PAPR	:	Peak to Average Power Ratio
PCB	:	Printed Circuit Board
PCT	:	Parallel Combining Technique
PDF	:	Probability Density Function
Pin	:	Input Power
PLL	:	Phase Locked Loop
PM	:	Phase Modulation
Pout	:	Output Power
PSK	:	Phase Shift-Keying
PVT	:	Process Voltage Temperature
QAM	:	Quadrature Amplitude Modulation
RBW	:	Resolution Bandwidth
RF	:	Radio-Frequency
RFID	:	Radio-Frequency IDentification
RL	:	Load Resistance

RMS	:	Root Mean Square
Rx	:	Receiver
SCS	:	Signal Component Separate
SDR	:	Software Defined Radio
SFDR	:	Spurious Free Dynamic Range
SMS	:	Short Message Service
SNR	:	Signal to Noise Ratio
SOI	:	Silicon On Insulator
SRC	:	Sample Rate Converter
TDD	:	Time Division Duplexing
TDMA	:	Time Division Multiple Access
Tx	:	Transmitter
UMTS	:	Universal Mobile Telecommunications System
UWB	:	Ultra Wide Band
VBW	:	Video Bandwidth
VCO	:	Voltage Controlled Oscillator
Vds	:	Drain to Source voltage
VGA	:	Variable Gain Amplifier
Vgs	:	Gate to Source voltage
Vth	:	Threshold voltage
VoIP	:	Voice Over Internet Protocol
W-CDMA	:	Wideband-CDMA
WLAN	:	Wireless Local Area Network
WMAN	:	Wireless Media Area Network
ZdVS	:	Zero derivative Voltage Switching
ZOH	:	Zero Order Holder
ZVS	:	Zero Voltage Switching

IEMN	:	Institut d'Electronique de Microélectronique et de Nanotechnologie
IRCICA	:	Institut de Recherche sur les Composants logiciels et matériels pour l'Information et la Communication Avancée
ISEN	:	Institut Supérieur d'Electronique et du Numérique
USTL	:	Université des Sciences et Technologies de Lille

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Chapter 1

Context

1.1 Introduction

Communication between humans play an increasingly role in our society. The amount of data to be exchanged develops in the same way while the nature of data keep changing with the needs of users. Beside the evolution of the information, the users become more and more mobile while requiring the same quality of service such as a fixed high speed connection. These constraints in the constant evolution of the communication necessitate a continuous improvement of the wireless link between users. The wireless communications field must provide a sufficient data transfer speed margin in compliance with the needs of the users. In this way users will be able to find brand new applications to take maximum advantage of the available communication capacity. In this chapter the context in which the works performed during the thesis take place will be explained. The constant evolution of the wireless communications field and its impact on spectrum use will be detailed in the first part. The second part will introduce the general concept of software defined radio and opportunistic radio, such as their impact on transceiver architecture. This will prepare the state of the art of various aspects of transmitters performed in the next chapter.

1.2 New standard emergence and spectral use

The radio-communications area is really wide and various. But if we focus on the wireless communications applied for public, and more specifically on the mobile phone market, several aspects can be underlined. The main one is characterized by the fact that new communication standards successively emerged in order to rectify the lack of their predecessors, and to adapt the wireless communications area to the users needs.
Thus, since the first wireless call on a mobile phone performed the 4^{th} April 1973 between Martin Cooper from the Motorola communication division and Joel Engel from the Bell Labs, the mobile phone was continuously transformed by the implementation of new functionalities to the hand-held device. The standards went through several modifications in order to deal with the voice, messaging (SMS) and data contents (MMS, video, music, internet, terrestrial television, VOIP, ...). Resulting in a succession of standards like AMPS (1G), GSM-DCS (2G), GPRS-EDGE (2G), UMTS (3G), HSPA+ (3G) and finally the LTE Advanced (4G). This last standard appears to be the current best candidate to offer the required data-rate able to support the high content consumption of the modern users, and a good coverage. Figure 1.1 shows the evolution of the peak data rate over the years for commercial devices [16]. The markers indicate the standards and their theoretical maximum data-rate.

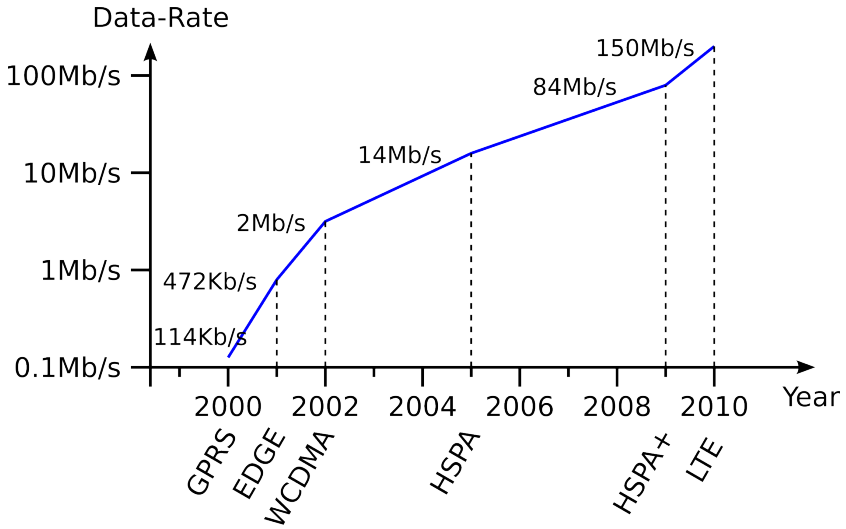


Figure 1.1: *Data rates evolution over the years*

But the current mobile-phone or smart-phone is not only dedicated for long distance communication. In fact, beside the traditional network architecture (user equipment and base station), the hand-held device must also support several short and medium range communications (WiFi, Bluetooth, NFC, Femtocell) and long distance receptions (TV,

GPS). Figure 1.2 shows a typical environment configuration where the user device must manage a large set of communication protocol with different equipments.

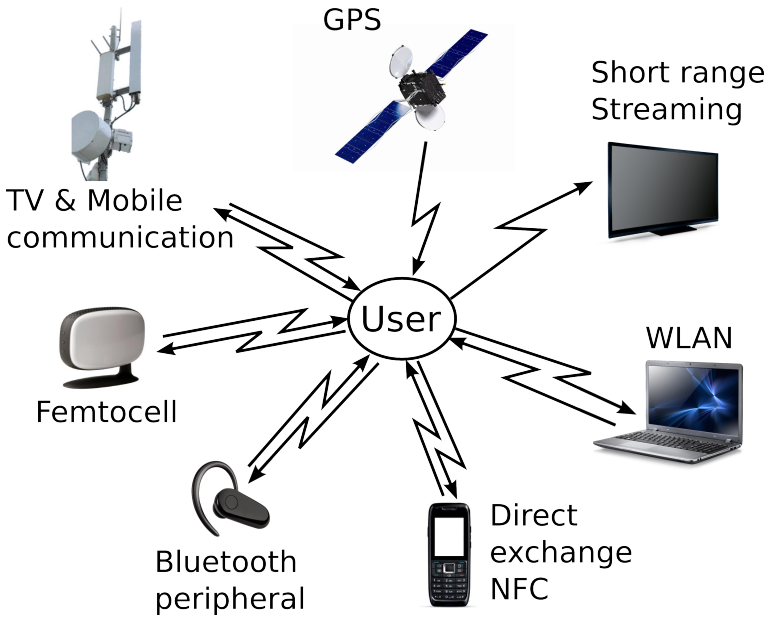


Figure 1.2: *Typical user environment and interaction*

While the standardization resulting from the IMT-2000 [17, 18] norm helps to unify few aspects of the standards from the third generation (capacity, price, mobility,), no one is able to rule them all. Figure 1.3 shows the trade off between the covered distance and the maximum data-rate for several standards.

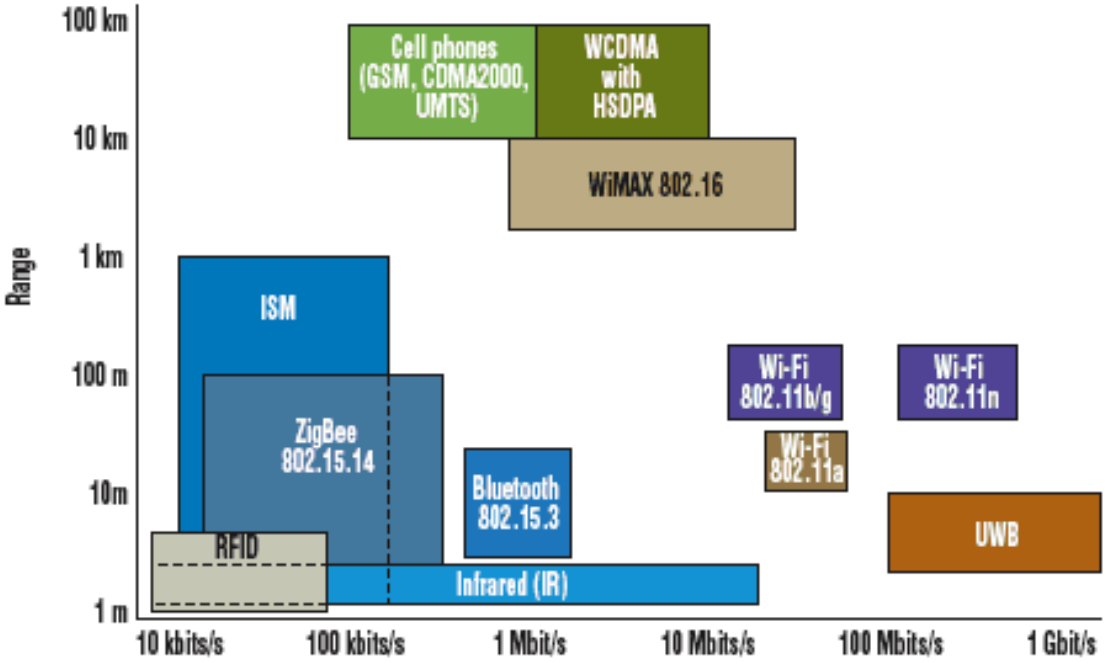


Figure 1.3: *Covered distance vs data-rate [1]*

This results to an overcrowded environment for the user device. Figure 1.4 illustrates the typical spectrum between 0,4 GHz and 6 GHz in France [19]. The ARCEP line refers to the spectrum areas under the supervision of the ARCEP (Autorité de Régulation des

Communications Electroniques et des Postes). These frequencies are dedicated for fix, mobile and satellites communications and also terrestrial television (DVB) or amateur communications. The DivNum FR line refers to the "Dividende Numérique" which is basically the released spectrum due to the transition from analog to digital television. All this released spectrum was reallocated to the LTE Band 20.

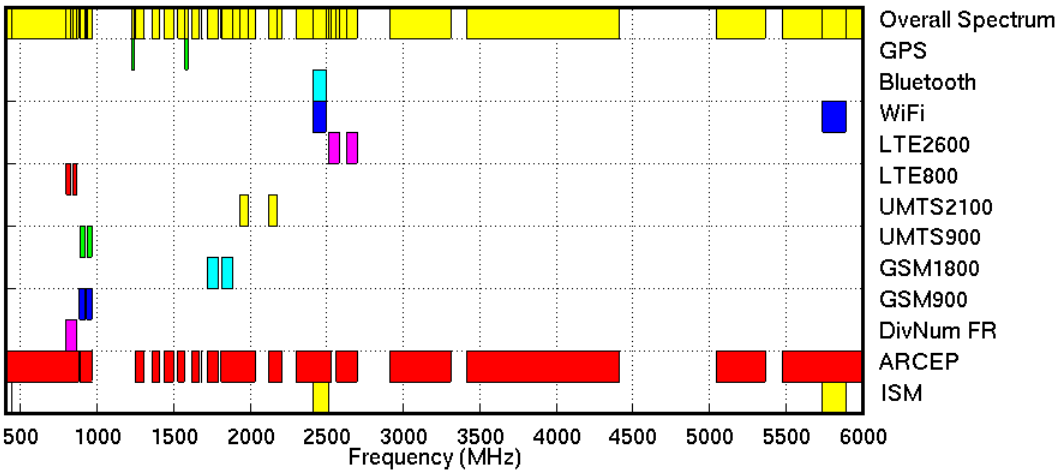


Figure 1.4: *Spectrum use in France*

Apart from the Bluetooth and WiFi standards located in ISM frequency band, the bands allocated for different standards are managed to avoid that their channels fall in the same band than other standards and then generate interferences. It's not just a matter of avoiding channel overlapping, but also avoid spurious emissions in sensitive spectrum bands. In order to avoid this unwanted case, a spectral emission mask defined over a large bandwidth (typical from several 100 Khz to 10 GHz) is specified in each standard release. Then the frequencies dedicated to reception, which are sensitive are well protected. And the signals emitted by neighbor devices are not drown by our signal. Figure 1.5 shows the emission masks for the UMTS [20] and LTE Advanced [2] standards.

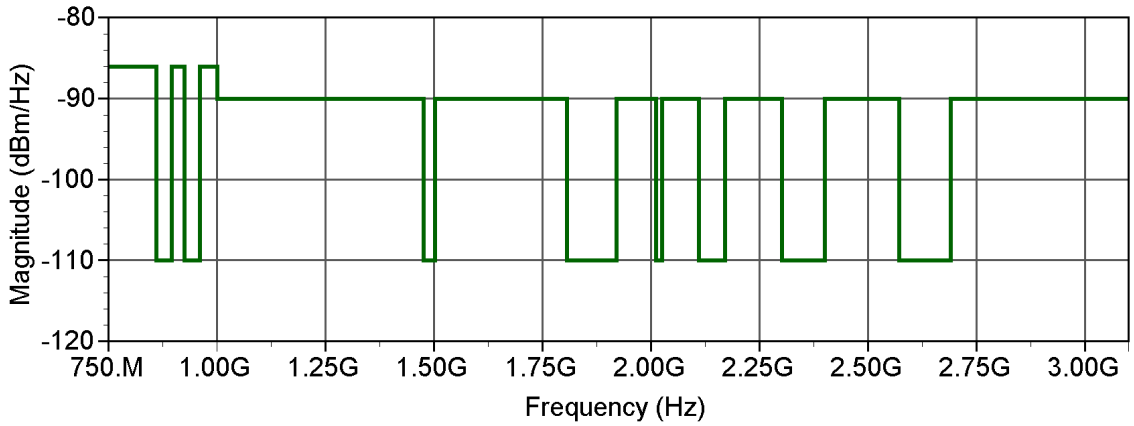


Figure 1.5: *Wideband emission mask as defined in [2]*

The environment is not static, due to the displacement or activation/deactivation of the user device or neighbor devices. The spectral use changes with the time, then the standard

offering the optimum data-rate matching the user needs is not constant. For example, a previous unused band could have offered an high data-rate. But the successively connection of new users in the same band drastically decreased the available data-rate for each user, until the total saturation of the channels. Then some other band can now offer the same or better capabilities.

Another situation could be the fact that moving from one place to another, could result in leaving the covered area of the used standard. In order to avoid any disconnection, the user device should be able to reconnect itself to another resource. For example, a user connected to a Femtocell can start watching a video on internet. But in the case that he leaves the covered area of the access point. He needs to find a new way to access to internet, like a LTE base station. Figure 1.6 illustrates such a situation.

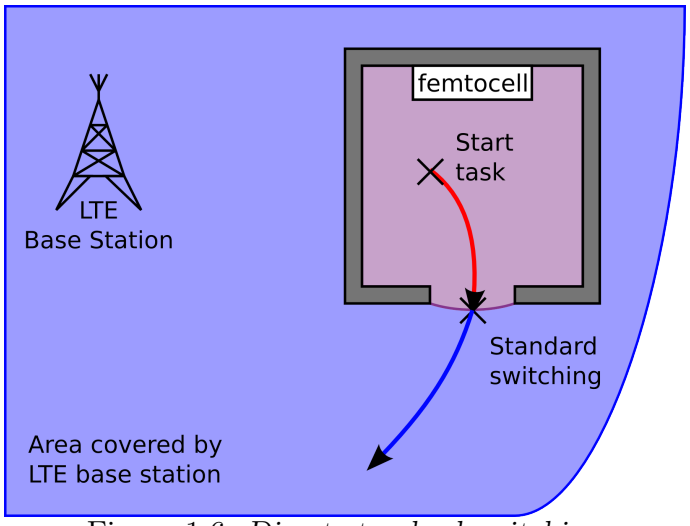


Figure 1.6: *Direct standard switching*

The user device must not be passive facing such variations of its environment. On the contrary, it must be able to adapt itself with the aim of offering the adequate connexion to the services required by the user. The hardware defined radio (HDR) was the main implementation approach for the two first generations of communication standards. But the transceivers were designed to support only few standards with small tuning capability. Then the way to make and hand-held device smart-enough to accommodate itself to the environment was a major research area since the emergence of the 3G and still ongoing. This resulted in the emergence of the software defined radio (SDR) and its declination the opportunistic radio (OR). The next section will define and explain their purposes and principles. Their limitations and difficulties will also be discussed in order to highlight the possible research axes.

1.3 Software Defined Radio and Opportunistic Radio

As explained in the previous part, a modern hand-held device must be able to adapt itself in order to keep the optimal communication among environment variations. This adaptation requires a transceiver with reconfigurable front-end and baseband processing. Which bring us to software defined radio, one of the majors concepts of the last 15 years in the wireless communication field.

The SDR is an evolution of the hardware defined radio, where some functions such as modulators, converters, filters, mixers, amplifiers and demodulators can be implemented by software components (e.g: DSP, FPGA, dedicated processing units). This description can be assimilated to the definition formulated by the SDRF [21] : Radio in which some or all of the physical layer functions are Software Defined.

In order to distinguish the two approaches (HDR and SDR) they will be compared when applied to a real scenario. In this case, a typical transceiver occupying two bandwidths (GSM900 and GSM1800) and supporting the WCDMA (Japan same as UMTS for Europe) and CDMA2000 (North and South America) standards. First, Figure 1.7 shows the transceiver if hardware implemented with a general homodyne architecture.

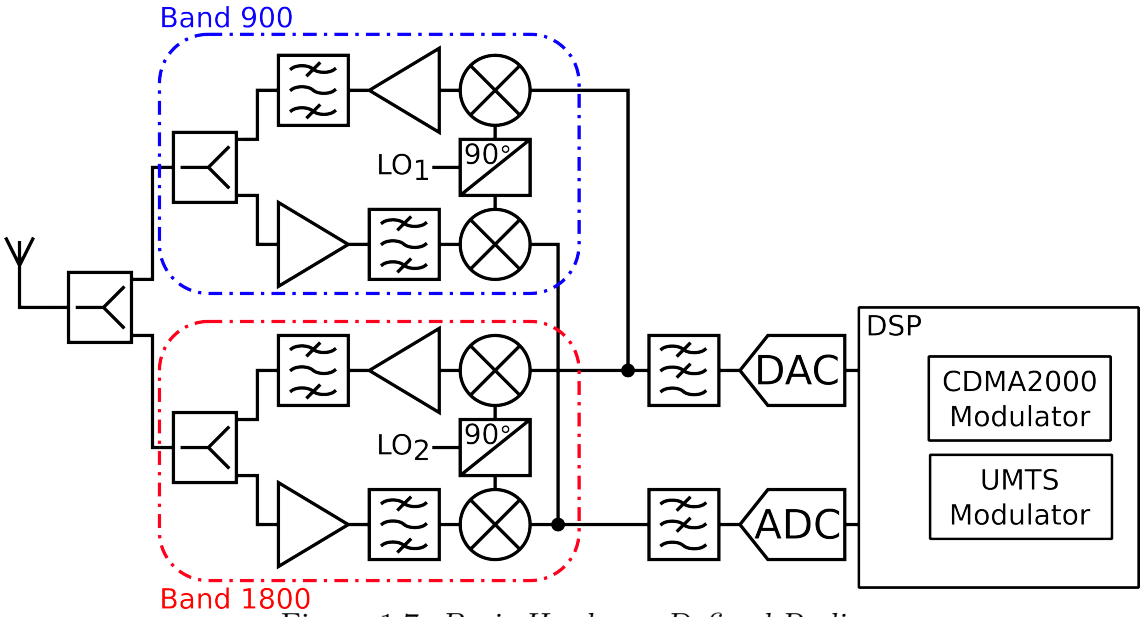


Figure 1.7: *Basic Hardware Defined Radio*

In this implementation, RF blocks such as amplifiers, mixers and filters are dedicated to one frequency band. Then, these blocks are duplicated between both bands. In the same time, baseband analog functions as low pass filters and converters can be merge to be used in 900 and 1800 bands. On the other way, the baseband digital blocks are directly

implemented in the DSP with hard-coded functions and can be configured depending on the standard used. The redundancies of the RF functions, for example one power amplifiers (PA) dedicated for each frequency bands, results to a wider area and then higher manufacturing costs. The overall power consumption and management is also a problematic aspect. Finally, the transceiver is locked on this configuration with no opportunity to change. For example, it would be not possible to reconfigure the system in order to support a new standard in the same frequency bands, even if it only needs small modifications of the modulator. This approach obviously presents some major limitations, even to adapt itself to the emergence of a new standard close to the ones already supported.

Figure 1.8 presents a transceiver based on the SDR approach as previously defined with a hardware defined layer (RF filters and amplifiers) and a software defined layer (mixers, baseband filters, modulator, demodulator).

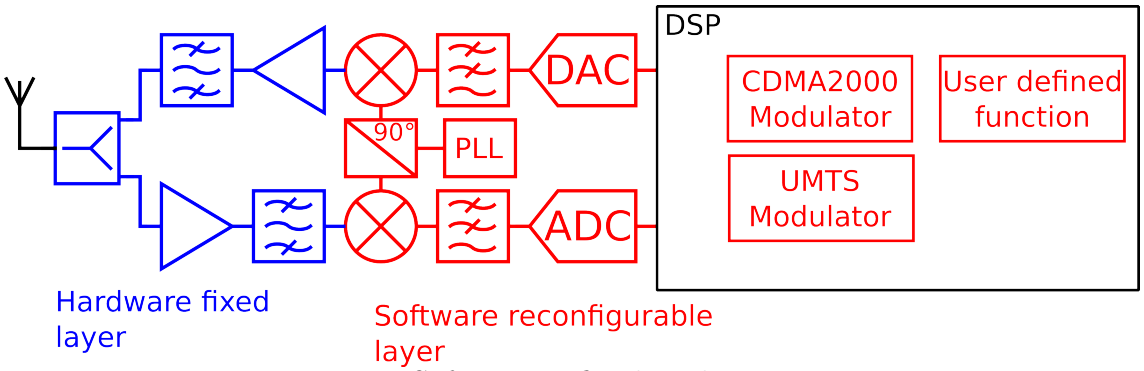


Figure 1.8: *Software Defined Radio transmitter*

A large part of the processing is realized in the digital domain. This implementation take advantage of the high digital processing density, the high working frequency and also the low power consumption of the advanced CMOS technologies. The software defined layer include all the functions needed to support both the standards in the frequency bands (modulation scheme, up/down converters, digital filters) and can also implement extra functionalities like user defined processing blocks. In our examples on Figure 1.7 and Figure 1.8, in order to simplify the view of the system the components defining the modulation (demodulation) scheme were merged in one bloc modulator (demodulator) for each standard. The pooling could have been extended to the common components of both modulation scheme.

The ability of the transceiver to support different standard in SDR is used in several concepts like the Cognitive Radio (CR) and Opportunistic Radio (OR). Cognitive Radio was introduced by Mitola in [22]. CR usually denotes a system aware of its environment with the ability to take decisions and to adapt itself to it. First, the awareness means

the ability of the system to sense and characterize the environment in term of spatial and spectral use in order to determine the available resources. Second, the CR takes decisions thanks to a cognitive process. This process takes into account the state of the environment and more important the behavior of the other users to determine the optimum band and standard. Third, the adaptability refers to the ability to configure the transceiver to support different standards, frequency bands or power level. This aspect is directly related to the SDR approach.

The Opportunistic Radio (OR) [23] is based on the CR approach with a more complex cognitive process. This process allows opportunistic access of the spectrum with SDR based transceiver without impact to other users communications. It includes a sharing algorithm taking into account the needs of other users and the available resources.

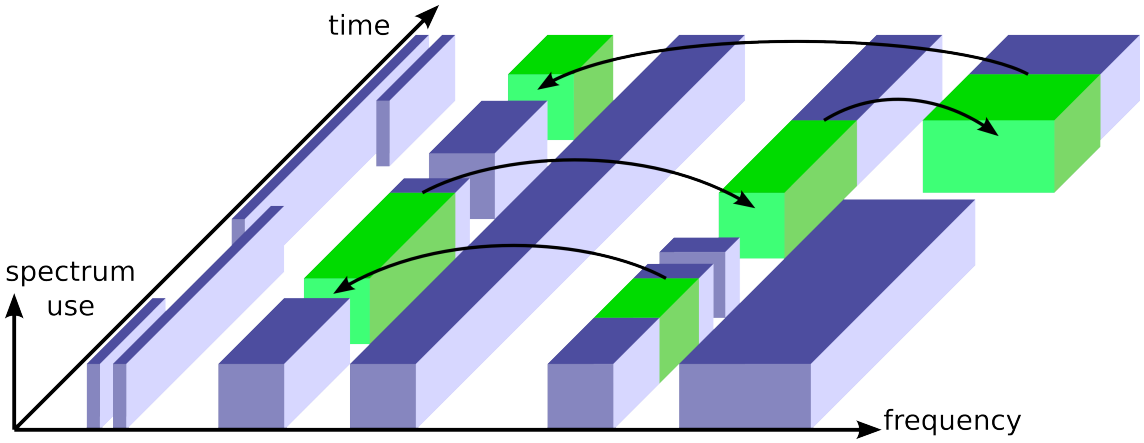


Figure 1.9: *Opportunistic scheme over time*

Figure 1.9 shows the frequency agile ability of an OR based device switching from unused band to unused band. The device front-end shows the ability to reconfigure itself depending on the control of the opportunistic process. The front-end successively changes the transmit channel and used standard. In this way, the user always profit of the optimum connection

1.4 Conclusion

The present overview of the user needs clearly shows the need of smart devices with the ability to sense its environment and manage its transceiver. The resulting concepts of software defined radio and opportunistic radio gained far-reaching importance the last decade. The processing power of the user's device such as smartphone exponentially exploded, allowing more evolved and optimized algorithm to share the available spectrum between users. However, these concepts rely on highly agile front-end. More versatile is the transceiver front-end, more agile will be the device. In this context, several researches focus on the reconfigurability of the transceiver. The work presented in this manuscript intends to analyze the present state of the art of highly configurable transmitters and propose new approach to increase the flexibilty.

Chapter 2

State of the art

2.1 Introduction

The critical elements of any transceiver is the transmission channel and the interfaces with the baseband parts. As discussed before, the Software Defined Radio appears to be the Holy Grail of future wireless communication. Nevertheless, the reconfigurability of the transmitter and receiver still need improvement. In this manuscript, consideration is given to the transmitting part. This chapter will describe the main aspects of a transmitter and analyze their implementation in reconfigurable and wide-band system. A general overview of the Cartesian and polar approaches will be done in the first section, and will be kept in consideration in the following sections. The second section will define the characteristics of the power stage as efficiency and linearity. The main linearization schemes and efficiency improvements will also be addressed. Due to the low power achievable in advance CMOS technology and limited passive integration, power recombination techniques and wide-band impedance matching will be detailed in the third section. After these sections addressing basics aspects of todays transmitters, the future of all-digital transmitters will be considered in the fourth section. And will consist of a survey of the impact of the two main candidates for digitization of RF functions: DRFC and DPA.

2.2 PA implementation

As explained in the previous section, the PA is a critical block in the transmitter design. It is the last active component before the antenna and the higher contributor to the power consumption. Figure 2.1 presents the repartition of the power consumption in a typical smartphone when transmitting an E-mail [3]. As we can see, wireless communication is the main source of power consumption. This section will detail the PA characteristics and specifically linearity and efficiency. An overview of the implementation of power stages will also be done.

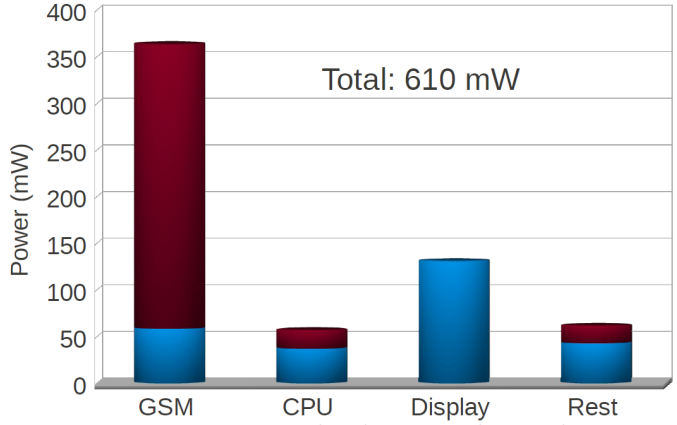


Figure 2.1: *Power consumption in standard smartphone during E-mail transfert [3]*

2.2.1 Efficiency and Output Power

The Power Amplifier can be seen as a black-box, as represented on the Figure 2.2, where RF and DC power go in and out.

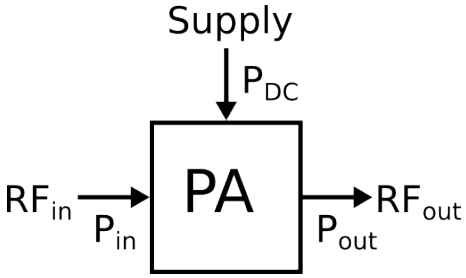


Figure 2.2: *PA as black-box*

There are two common definitions for the efficiency. The first one is called Drain Efficiency (DE) and is defined as the ratio between the power of the output RF signal, and the DC power used to supply and bias the power stage. The drain efficiency is defined on (2.1).

$$DE = \frac{P_{out}}{P_{DC}} * 100 \tag{2.1}$$

This ratio only defines the ability to transform DC power into RF. But it does not take into account the power amplification. The second definition called Power Added Efficiency

(PAE) is the ratio of the power added to the signal over the supplied power as described on (2.2).

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} * 100 \tag{2.2}$$

Thus, the PAE greatly decrease when the output power decreases. The new standards tend to increase the Peak to Average Power Ratio (PAPR). The PA must be designed in order to offer good efficiency at the maximum output power but also at lower level. The maximum and mean value of the PAE are then both important.

2.2.2 PA implementation

The efficiency greatly depends of the class of the PA. These classes can be organized in two categories. The first one is the linear amplifier class and is the most basic implementation. The principle is to use the amplifying transistor in its saturated region. The biasing will determine the class of the PA. Figure 2.3 shows a typical implementation based on a common emitter configuration without the input biasing circuit. Figure 2.4 details the I-V characteristic of the PA of Figure 2.3 The triode and saturated region are specified, while the classes and their respective biasing are plotted.

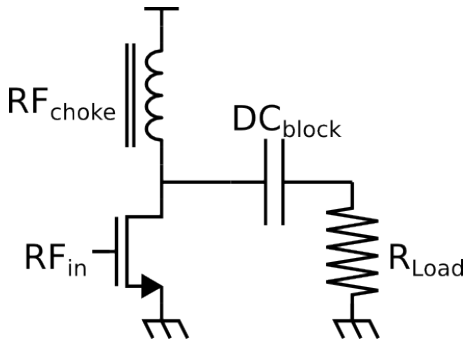


Figure 2.3: *PA implementation with Common-Source amplifier*

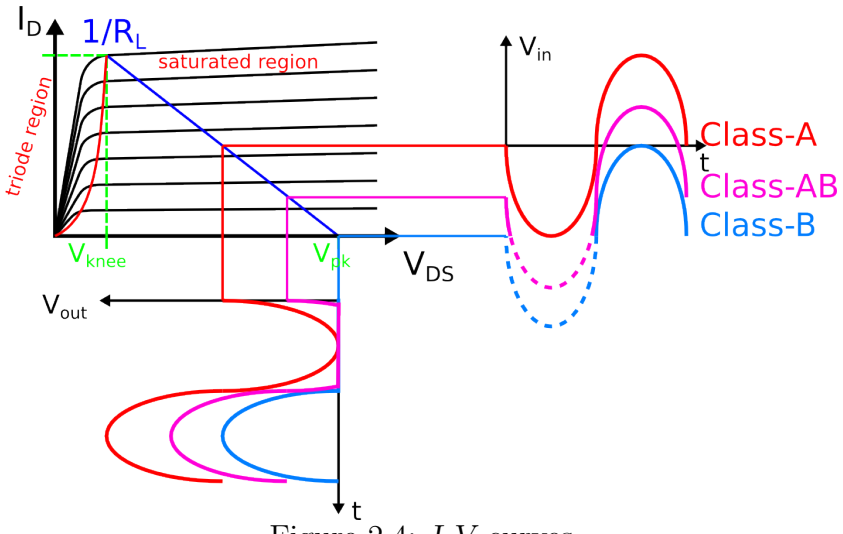


Figure 2.4: *I-V curves*

The output dynamic and gain is set by the load, while the biasing points move along the load-line. The output shape depends on the PA class and its conduction angle. This latter strongly impacts the PA efficiency. Table 2.1 lists the four main class-type and their conduction angle and drain efficiency.

Table 2.1: *Class-type DE*

Class	A	AB	B	C
Conduction angle θ	$\theta = 2\pi$	$\pi < \theta < 2\pi$	$\theta = \pi$	$\theta < \pi$
P_{DC}	$\frac{V_{DD}^2}{R_L}$	$\frac{V_{DD}^2}{R_L} < P_{DC} < \frac{2V_{Peak}^2}{\pi R_L}$	$\frac{2V_{Peak}^2}{\pi R_L}$	$\frac{V_{DD}^2}{\pi R_L} * \frac{\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)}{1 - \cos\left(\frac{\theta}{2}\right)}$
P_{del}	$\frac{V_{DD}^2}{2R_L}$	$\frac{V_{DD}^2}{2R_L}$	$\frac{V_{Peak}^2}{2R_L}$	$\frac{V_{DD}^2}{4\pi R_L} * \frac{\frac{\theta}{2} - \sin\left(\frac{\theta}{2}\right)}{1 - \cos\left(\frac{\theta}{2}\right)}$
DE	50%	$50\% < DE < 78.5\%$	78.5%	$\frac{1}{4} * \frac{\theta - \sin(\theta)}{\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)} * 100\%$

The output power and efficiency are calculated when the PA is used at its maximum output power. The drain efficiencies were calculated with saturation drain-source voltage (VDS_{sat}) supposed null. The class-C can theoretically obtain a drain efficiency of 100%, but this occurs for a conduction angle of 0 which means a zero output power. Class-C also requires high-Q tank with narrow bands of resonance. The classes with a conduction angle lower than 2π introduce clipping effects. The output matching network needs to filter the resulting harmonics.

The second group of amplifiers is based on switching transistors. This group offers better efficiencies but also introduces higher distortions. The two principal implementations in RF are the class-E and class-F PAs. The schematic of a class-E is presented in Figure 2.5. The class-E was introduced by Sokal in 1975 [24]. The idea is to decrease the power dissipated in the transistor during switching. In order to avoid any power dissipation, the load circuit must ensure zero drain-source voltage when current is going through the transistor. This condition is called Zero Voltage Switching (ZVS). In order to avoid any current peak and then stress to the transistor, the derivative of the voltage must be zero when the switching occurs. This second condition is called Zero Derivative Voltage Switching (ZdVS). The I and V curves of the class-E are represented on the Figure 2.6 as explained in [24, 25, 26].

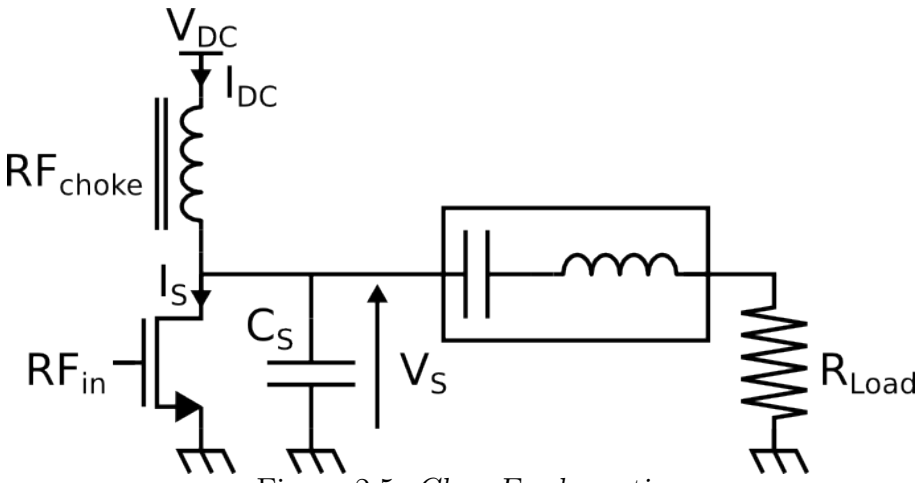


Figure 2.5: *Class-E schematic*

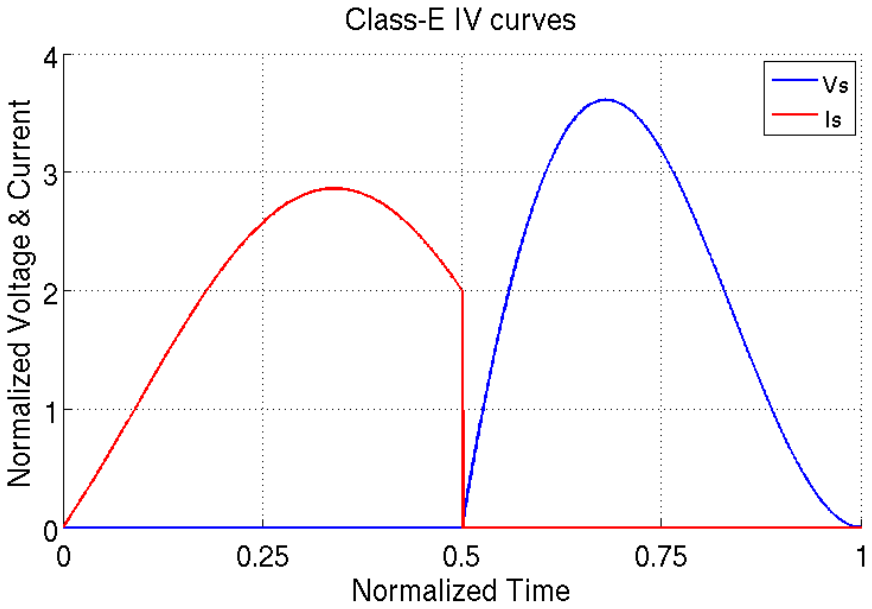


Figure 2.6: *Class-E IV curves*

When the transistor stop to conduct current (T=0.5) the drain voltage start to increase. The output matching network otherwise forces the drain voltage to decrease to zero with a zero slope at T=1 before the transistor start to conduct again. The main limitation of this amplifier class is the high voltage (up to 4 times VDC) across the transistor. In order to avoid any degradation, the supply voltage needs to be several times lower than the maximum drain-source voltage allowed by the process. This makes this implementation challenging in advanced technology where the knee voltage delimiting the saturation region is not negligible compare to the maximum supply voltage.

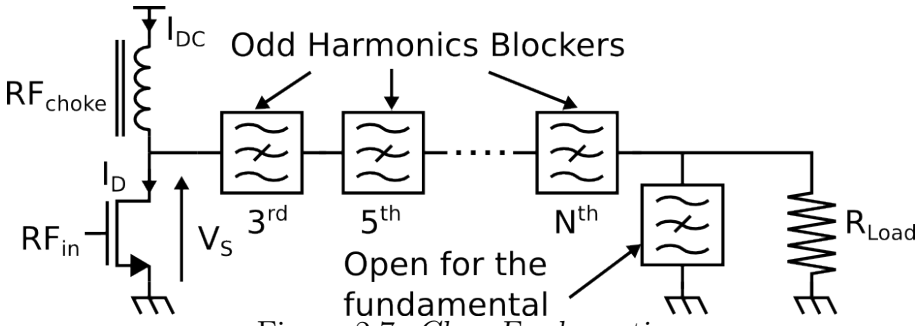


Figure 2.7: *Class-F schematic*

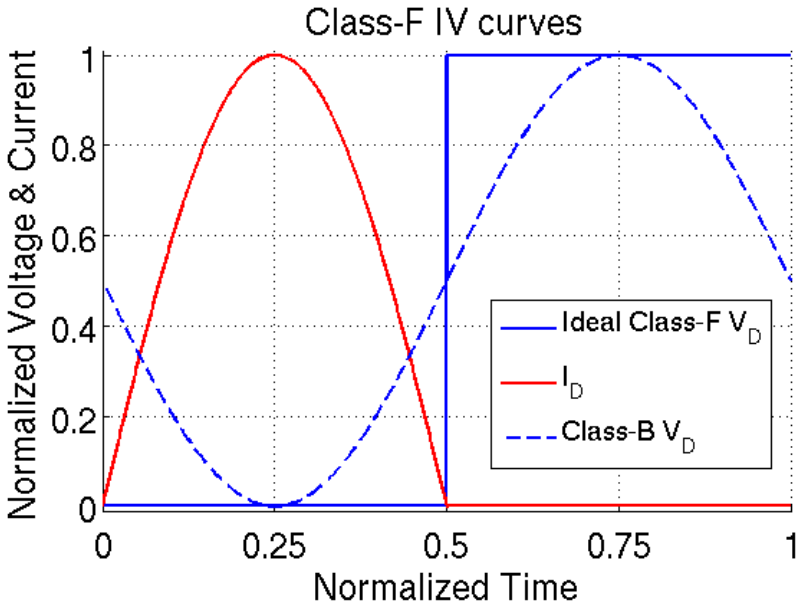


Figure 2.8: *Class-F IV curves*

The last amplifier class is the class-F [27]. The principle is the same as before, the power losses in the transistor are optimized. The class-F is based on a class-B amplifier where the output harmonics are filtered as represented on the Figure 2.7. The odd harmonics are blocked, while the even harmonics are shorted to ground. The ideal waveforms are shown on Figure 2.8. More harmonics filtering induces a voltage curve closer to a perfect square resulting in less and less overlapping of current and voltage. The parasitic drain source capacitance needs to be compensated by inductive components. Finally, high order filters (> 5) introduce passives losses which greatly degrade the overall efficiency.

The PA state of the art presented shows a wide diversity of implementations. The class of the PA must be choose to regard of the linearity and efficiency required by the system. The area is also an aspect impacted by the passives required.

2.2.3 PAE improvement

Beside the PA's class, the efficiency can also be improved at the system level. Figure 2.9 shows the improvement in efficiency obtained by Chowdhury in [4]. The system is based on 4 paths with transformer-based power combiner. Instead of controlling the PA amplitude, Chowdhury proposes to switch on or off the PAs in order to keep the PAs working at high amplitude level offering better efficiency.

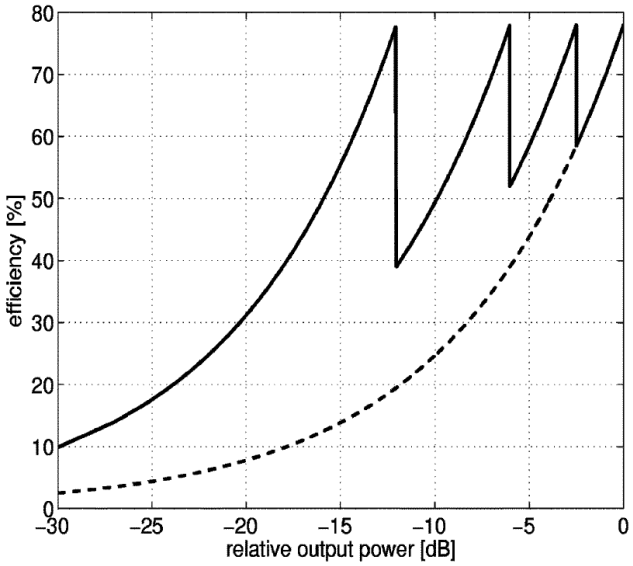


Figure 2.9: *Efficiency improvement in [4]*

2.2.4 Pout and Gain characteristics

Beside the efficiency aspect, the P_{out} vs P_{in} and Gain vs P_{in} curves are two useful informations to characterize a PA. As shown on Figure 2.10, the gain is constant and the output power is proportional to the input power for low power levels, called linear region, but degrade when the power increases. This is called the compression effects and results from the saturation of the PA when the maximum amplitude is achieved.

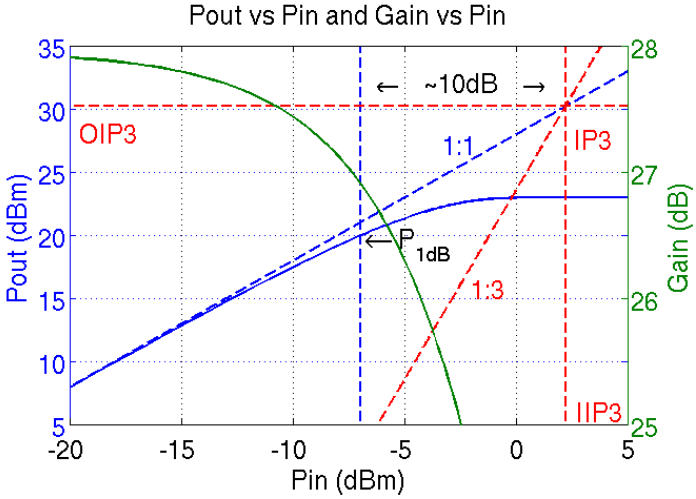


Figure 2.10: *Static PA characteristic*

In order to avoid strong distortions, the PA must work under the 1 dB compression point (P_{1dB}). This means that the output power and gain of the PA are 1 dB under the ideal value $G * P_{in}$. The relation between non-constant gain and the harmonics will be explained in the next point. The harmonics also impact the fundamental producing the compression shape. The rule of thumb approximate the P_{1dB} as the point 10 dB lower than the crossing point of the extrapolation of the linear fundamental with the third harmonic as represented on the Figure 2.10. This is an empirical approximation which can fluctuate depending on the class, implementation and process. The next point will detail basic models of the non-linearities and the typical linearization techniques.

2.2.5 Linearity

The ideal amplifier would only have a linear behavior as described on the (2.3) where x stands for the input signal and y the output while a_1 is the coefficient related to the gain.

$$y(t) = a_1 x(t) \tag{2.3}$$

Nevertheless, some distortions are generated by the non-linear behavior of the active components (transistor) and also some clipping effects. Their impact can be modeled by introducing higher degree coefficients as shown on the (2.4) based on a polynomial model. The impact of these non-linearities grows exponentially with the amplitude.

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + a_4 x^4(t) + a_5 x^5(t) + ... \tag{2.4}$$

A differential implementation suppresses all even harmonics if the two PAs are well-matched. Figure 2.11 shows the spectrum on different nodes of the differential PA.

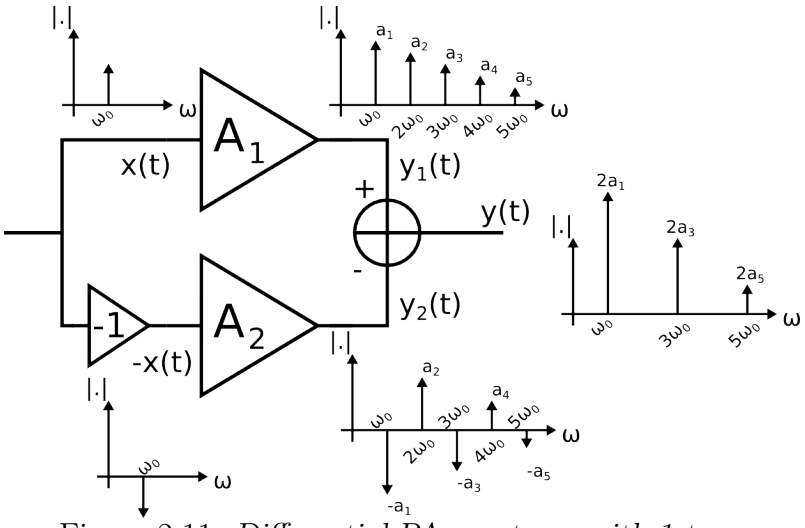
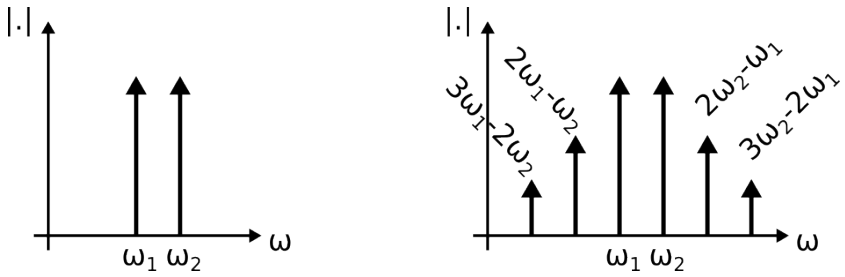


Figure 2.11: *Differential PA spectrum with 1-tone*

The fundamental and odd harmonics are present. It is theoretically possible to measure their amplitude but the harmonics can be well beyond the covered bandwidth of the PA. In order to solve this problem, a two-tone test can be performed. The resulting spectrum is presented on the Figure 2.12. With $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ the 3^{th} harmonics and $3\omega_2 - 2\omega_1$ and $3\omega_1 - 2\omega_2$ the 5^{th} harmonics.



a) ideal output spectrum b) distorted spectrum with

Figure 2.12: *2-tone spectrum*

Measuring the inter-modulation (IM) magnitude allows the generation of a PA model together with linearization schemes. Polynomials models do not cover all the non-linear effects. For example, the behavior of PN junctions in transistors dependents on the temperature. Amplitude modulation causes variation of the current and the temperature in time. This effect is one of the causes of behavior change over the time called memory effects. In order to model these non-constant characteristics of the PA, more complex models must be used such as complex polynomial models or Volterra series. These models are well explained the literature [28, 29, 30] and will not be detailed here.

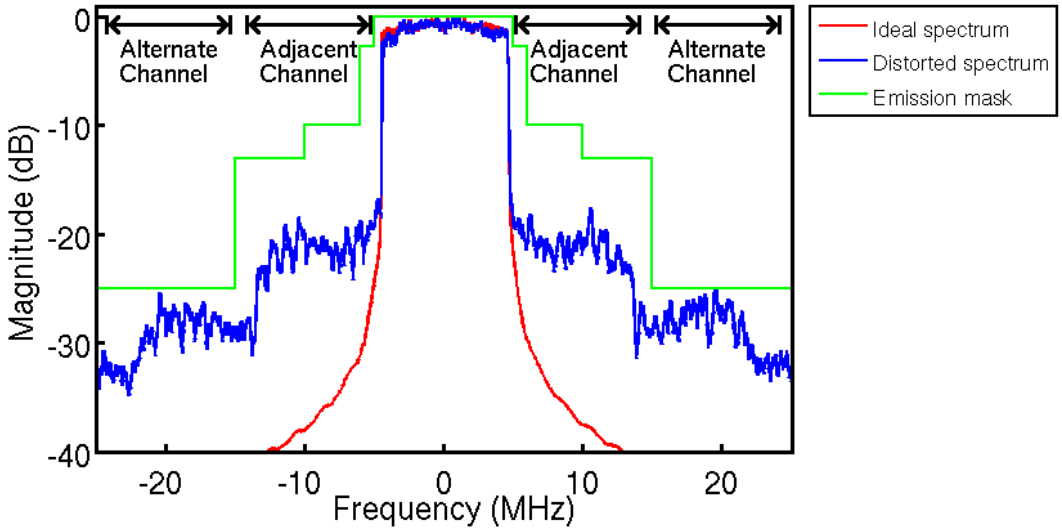


Figure 2.13: *LTE ACPR spectrum*

In order to quantify the distortions, the spectrum can be observed with complex modulation as done with the 2-tone test. Then, the disturbance of the adjacent channels can be

measured through the unwanted spectral emission level. A typical communication standard defines an emission mask which is the maximum spurious emission allowed around the fundamental channel. Figure 2.13 shows a typical in-band spectrum for LTE where the emission mask is drawn alongside an ideal and distorted spectrum at the PA output. The spreading around the fundamental disturbs the two adjacent and alternate channels. Their value are respectively noted Adjacent Channel Power Ratio (ACPR) and Alternate Channel Power Ratio (AltCPR). If their level meets the requirements, then the signals transmitted by other users in these bands will not suffer from any perturbation.

The second useful measurement is the Error Vector Magnitude (EVM) which specifies the deformation of the constellation. Figure 2.14 shows how EVM is measured ($EVM = \frac{\vec{e}}{\vec{v}}$). The RMS EVM of the constellation is obtained by the RMS value of the error vector ($\vec{e}$) over ideal vector ($\vec{v}$) to each points as defined on (2.5).

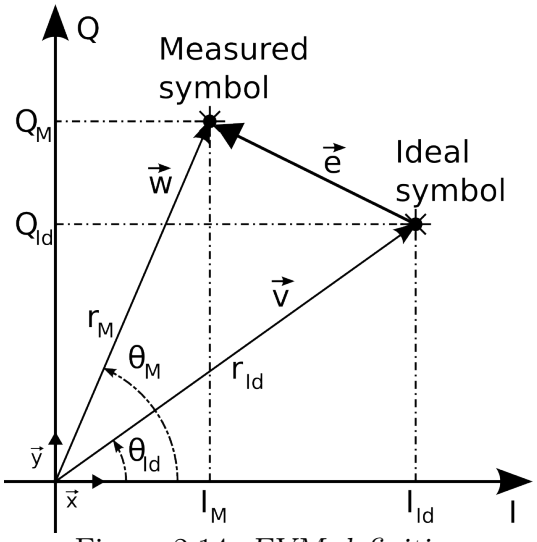


Figure 2.14: *EVM definition*

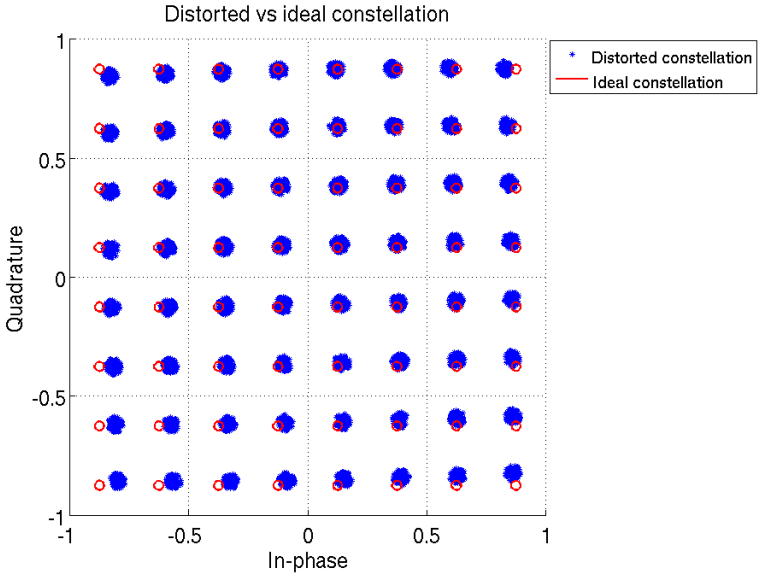


Figure 2.15: *Ideal and distorted constellation*

$$EVM_{RMS} = \sqrt{\frac{\frac{1}{N}\sum_{i=1}^{N}|\vec{e}_i - \vec{v}_i|}{\frac{1}{N}\sum_{i=1}^{N}|\vec{v}_i|}^2} = \sqrt{\frac{\frac{1}{N}\sum_{i=1}^{N}(I_i - I_{Id})^2 + (Q_i - Q_{Id})^2}{\frac{1}{N}\sum_{i=1}^{N} I_{Id}^2 + Q_{Id}^2}} \quad (2.5)$$

Figure 2.15 shows a 64-QAM constellation at the output of a non-linear system. The ideal points are scattered into groups due to memory effects and components imperfections. The gain compression for high amplitude signals deforms the corners of the constellation. A final remark is the increasing difficulty to implement PAs in advanced process. The scaling down of the dimensions impact the PAs characteristics as the design constraints. First, the available power is directly related to the decrease of supply voltages. Of course, using the low threshold voltage option in CMOS processes can help save few 100 mV to the headroom but their values remain constants over node iterations to ensure low leakage current. Then, the output power and efficiency drastically decrease as the output voltage swing reduces.

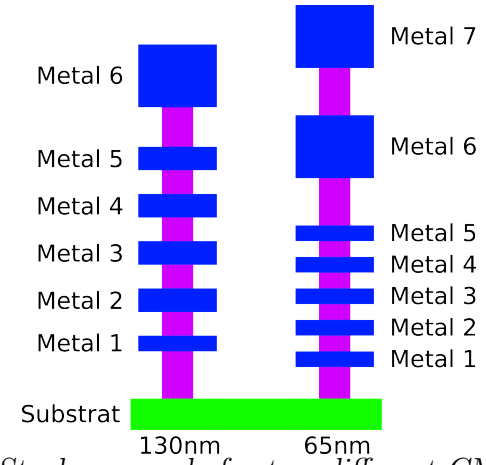


Figure 2.16: *Stacks example for two different CMOS processes*

Second, the back-end also slightly evolves with the transistors channel length. The number of metal layers increases while the metal thickness and isolations decrease as depicted in Figure 2.16. Figure 2.17 shows the evolution of the sheet resistance of the first metal layer at $105°C$. Increase of resistive and capacitive parasitics elements degrades the quality factor of passives and requires well fitted models to allow correct design. This last aspect is mostly done by time-expensive extraction of the passives structures thanks to electromagnetic simulators. The last effect of back-end sizing is the electro-migration constraints which complicate the interconnections in and between power block.

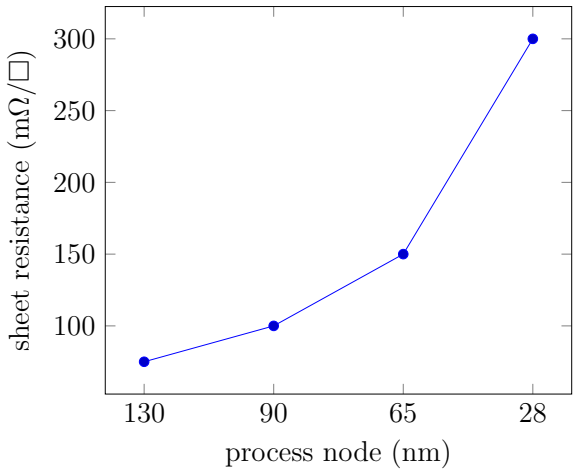


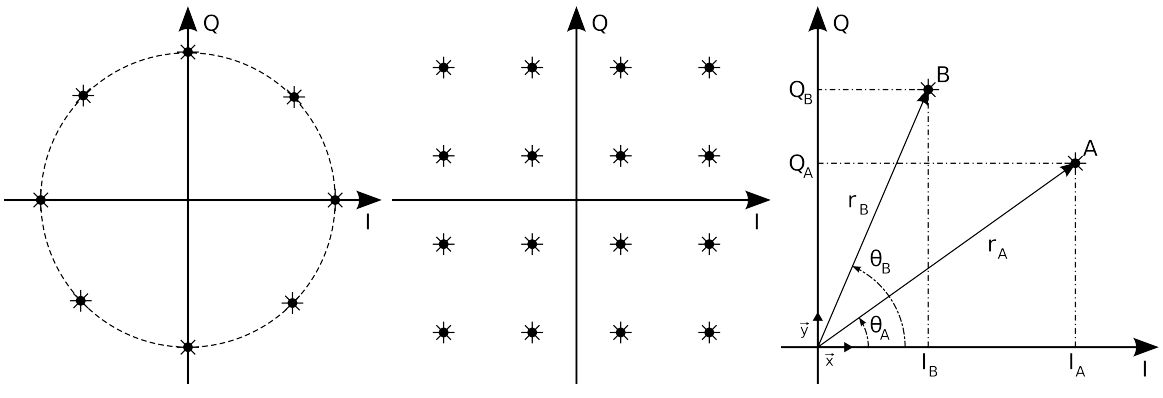
Figure 2.17: *First metal layer sheet resistance evolution*

To summarize, the PA is a critical component of a transmitter. Several notions as efficiency and linearity have to be taken into account during the design and are an important research axis. The architecture and process directly impact its characteristics.

2.3 Cartesian versus Polar Architecture

The goal of any transmitter is to broadcast a RF signal carrying the information through a channel. The signal can be represented in two different forms called Cartesian and polar forms. This section will describe these two main representations and their impact on the transmitter architecture.

Before describing the Cartesian and Polar architecture, we must define the baseband information. In wireless communications, the transmitted information is represented on a constellation as shown on Figure 2.18. They are classified depending on the number of points and their shape, new standards tend to increase the number of point in order to increase the data-rate.



a) 8-PSK b) 16-QAM c) coordinates

Figure 2.18: *Constellation example*

Figure 2.18.a) shows an 8-PSK modulation where the phase can take 8 different values while the magnitude is constant. Figure 2.18.b) shows a 16-QAM modulation where each point is defined by a vector. Figure 2.18.c) shows a general representation of two data points A and B. Each one can be respectively defined by the $\vec{OA}$ and $\vec{OB}$ vectors. Each vector can be defined by Cartesian or polar coordinates. For example, the Cartesian coordinates of point A are obtained by orthogonal projection on the axis Ox and Oy and are equivalent to a complex form $C_A = X_A + jY_A$. X_A represents the in-phase component (I axis) and Y_A represents the quadrature components (Q axis). They will be designated by respectively I_A and Q_A. On the other side, the point A can be defined by the angle θ_A between Ox and OA and the vector magnitude r_A also called radius. This representation is called polar form and is also related to the complex form $C_A = r_A e^{j\theta}$. Both representation can be used, and the transformation from Cartesian to polar is defined by Equation (2.6) and Equation (2.7).

$$r = \sqrt{X^2 + Y^2} = \sqrt{I^2 + Q^2} \tag{2.6}$$

$$\theta = \arctan\frac{Y}{X} = \arctan\frac{Q}{I} \tag{2.7}$$

These transformations are strongly non-linear and are commonly implemented in digital processing systems for example by CORDIC algorithms [31], [32], [33], [34], [35]. Equation (2.8) shows the complex representations of the baseband data.

$$BB(t) = M(t) = I(t) + jQ(t) = r(t).e^{j\theta(t)} \tag{2.8}$$

This baseband information is translated in the RF domain by the modulation of a carrier as depicted on Equation (2.9).

$$\begin{aligned} RF(t) &= BB(t) * F_C(t) = M(t).e^{j\omega_C t} \\ RF(t) &= I(t).e^{j\omega_C t} + jQ(t).e^{j\omega_C t} = I(t).e^{j\omega_C t} + Q(t).e^{j(\omega_C t + \pi/2)} \\ RF(t) &= r(t).e^{j\theta(t)}.e^{j\omega_C t} = r(t).e^{j(\theta(t)+\omega_C t)} \end{aligned} \tag{2.9}$$

The real part of Equation (2.9) is defined by Equation (2.10) and Equation (2.11).

Cartesian:

$$RF(t) = I(t).\cos(\omega_C t) + Q(t).\sin(\omega_C t) \tag{2.10}$$

Polar:

$$RF(t) = r(t).\cos(\omega_C t + \theta(t)) \tag{2.11}$$

In the Cartesian form, two LO signals with $\pi/2$ phase-shift are needed in order to translate the two components to RF. In the case of polar modulation, the carrier needs to be phase modulated. This concludes the mathematical aspects of the Polar and Cartesian approaches. The next two points will detail the physical implementations.

2.3.1 Cartesian implementation

Figure 2.19 shows a typical implementation of a Cartesian transmitter.

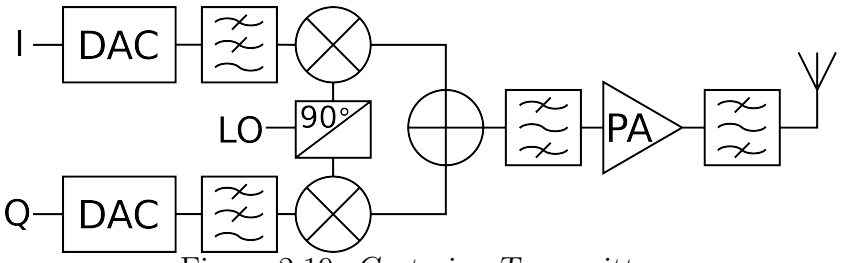


Figure 2.19: *Cartesian Transmitter*

The digital baseband signal I(t) and Q(t) are generated by the DSP. They are translated in RF through several steps. The first one is the Digital-to-Analog conversion performed by the DAC components and followed by an anti-aliases filter in order to suppress any undesired replicas. The second step translates the baseband signals around the RF carrier through the mixer components. The in-phase and quadrature signals are then recombined before the power stage. The RF signal driving the Power Amplifier (PA) is exactly the baseband complex information translated around the carrier. From baseband generation to recombination before the PA, the I and Q signals undergo the same processing. Figure 2.20 shows the spectrum of the baseband and recombined signals for the transmitter presented in Figure 2.19. The total amount of the information is equally separated between the I and Q paths. The I and Q bandwidths are the same than the total signal. Then, the standard bandwidth directly constraints the required bandwidth of the DACs.

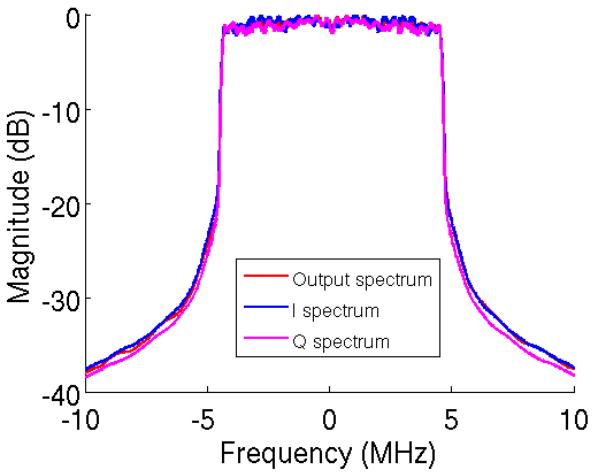
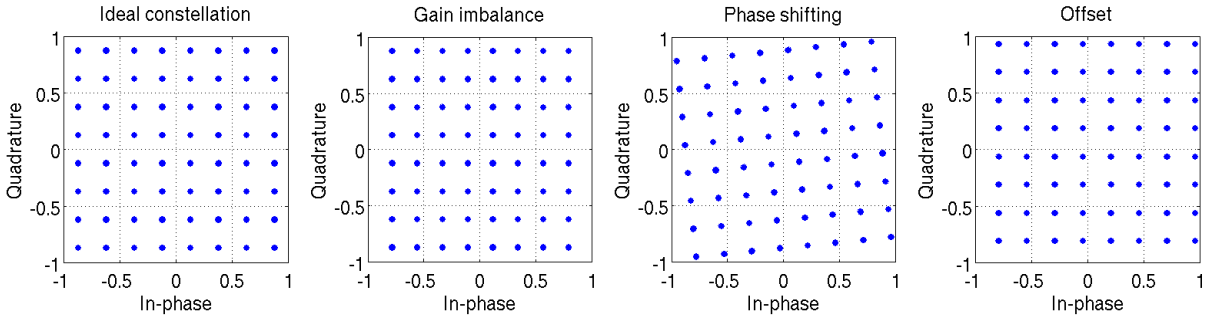


Figure 2.20: *Cartesian spectrum for LTE symbol*

Due to the parallel structure of the Cartesian transmitter, both paths need to be exactly the same. In fact, gain imbalance and offset can distort the constellation and degrade EVM as represented in Figure 2.21. Figure 2.21.a) shows the ideal constellation while the Figure 2.21.b) shows a constellation where the gain on the I and Q paths are different, stretching the constellation.



a) b) c) d)

Figure 2.21: *Constellation and distortions on non-linear system*

Figure 2.21.c) shows a phase error. Finally, Figure 2.21.d) presents a constellation with an offset on the I and Q paths.

2.3.2 Polar implementation

The transmitters based on polar form [36] are fundamentally different. The information is spread into phase and amplitude components. Transmitter based on polar architecture is presented in Figure 2.22.

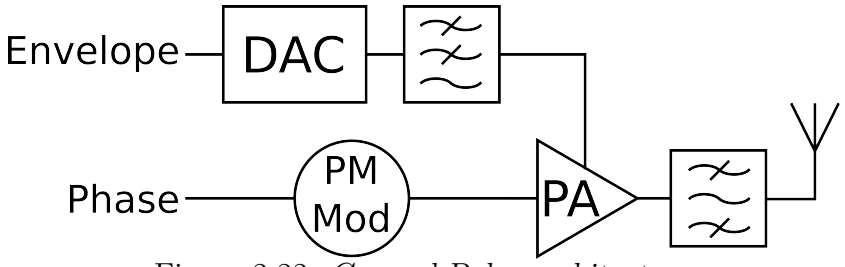


Figure 2.22: *General Polar architecture*

The phase modulates the carrier frequency thanks to the phase modulator (PM Mod). The resulting RF signals drives the PA. The phase and amplitude recombination is performed at the PA stage, which can be done in two ways. First, using a variable gain amplifier (VGA) before the PA allows the envelope signal to modulate the RF amplitude as depicted in Figure 2.23. Finally, Figure 2.24 presents the implementation where the amplitude directly modulates the PA supply thanks to DC-DC converters [37].

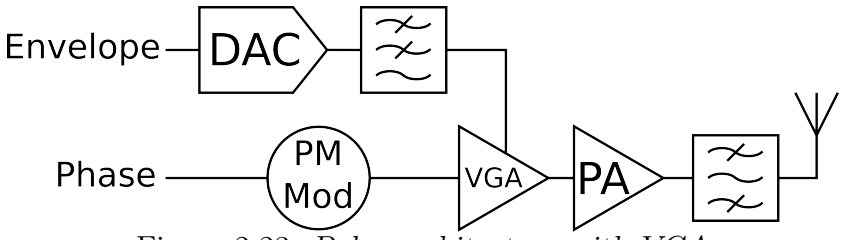


Figure 2.23: *Polar architecture with VGA*

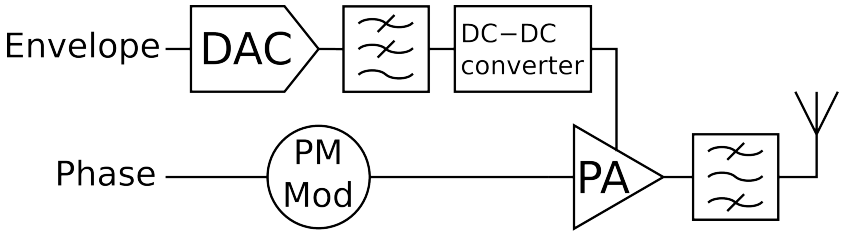


Figure 2.24: *Polar architecture with DC-DC converter*

One of the main advantage of the second implementation is the increase in PA efficiency. In fact, tuning the PA supply allows to set the PA close to its compression region showing a good efficiency. The spectrum of the phase and amplitude signals are distinct due to the different processing performed on the paths, as represented on Figure 2.25.

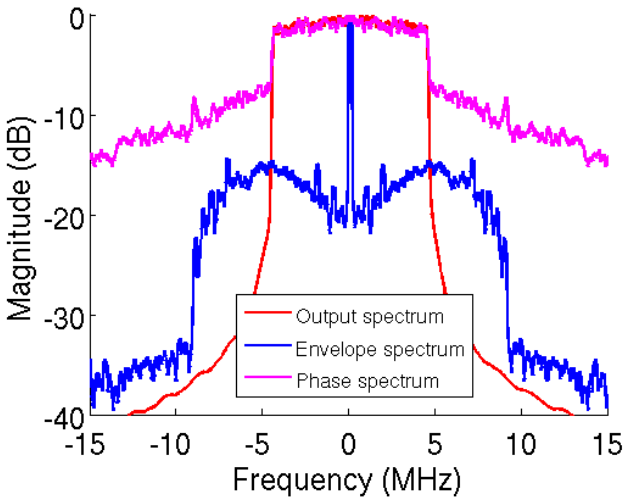


Figure 2.25: *Envelope and phase spectrum in Polar architecture*

Their shapes are different compared to the I and Q spectrum in the Cartesian implementation. But the spectrum of the recombined signals are the same. The envelope spectrum shows a strong DC component resulting of its positive characteristic. Both the phase and magnitude spectra extend way beyond the sharply limited signal spectrum. This spreading results from the non-linear behavior of Cartesian-to-Polar converison as defined in Equation (2.6) and Equation (2.7).

The polar approach is a good candidate to modulations with constant amplitude such as GMSK in the case of GSM. But the wide-bandwidth of the path and amplitude spectra limit its use to more complex modulations. This is the reason why the polar implementation was abandoned in favor of the Cartesian one during this last decade. However,

the use of advanced silicon process paves the way for polar implementation supporting wide-band modulation with non-constant amplitude.

2.3.3 Trade-off

In terms of implementation, Cartesian and Polar transmitters show different design complexities, advantages and disadvantages. For instance, both Cartesian and polar architectures require digital to analog conversions. These conversions can be characterize by two aspects. First, the converters' bandwidth which is around 3 time wider in polar than Cartesian approach. Secondly, the converters' resolution show different constraints. In polar architecture, the phase signal is more sensitive to the converter 's resolution than the amplitude. In order to illustrate this aspect, Figure 2.26 shows a LTE spectrum after quantization in Cartesian and polar architecture. The blue curve represents the Cartesian approach with 5bits conversion on I and Q signals. The cyan curve represents the spectrum in case of polar approach with a 6bits phase and ideal amplitude signals. The magenta curve stand for a 4bits amplitude associate to an ideal phase. Finally, the green curve represents a polar spectrum with a 6bits phase and 4bits magnitude. The polar spectrum is similar to the Cartesian spectrum. But, the polar architecture presents more design challenges than the Cartesian.

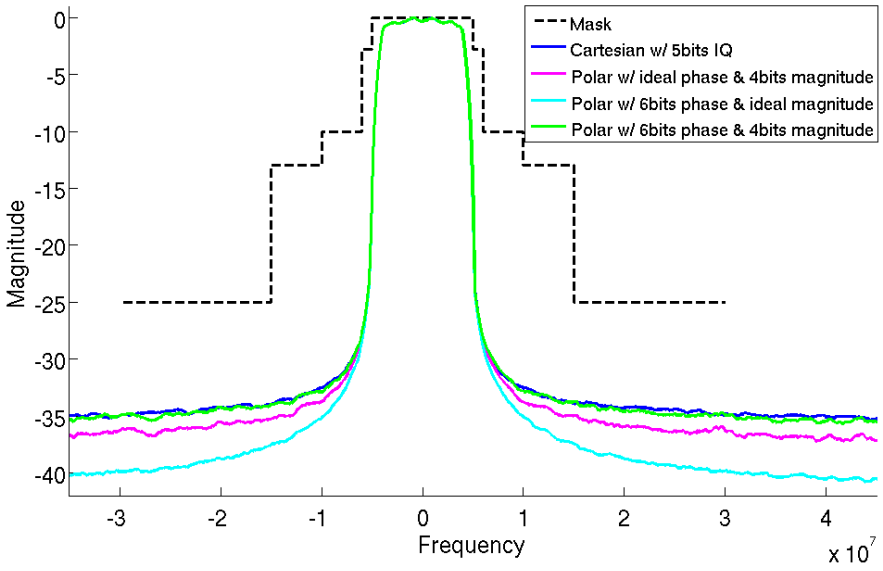


Figure 2.26: *LTE spectrum with quantization effects*

The main advantage of the Cartesian architecture is the identical path for the I and Q signals. The synchronization is then straight-forward. The design can be done for a single path and reproduced to the other. But this redundancy impacts the power consumption and area.

On the other hand, the polar approach suffers from the distinct electrical path of the phase and amplitude. The propagation delays between the baseband generation to the amplitude-phase recombination are not intrinsically the same. Therefore the synchronization of both paths is a critical aspect. Figure 2.27 shows the effect of any phase delay on the spectrum mask, with $T_{sample} = 1/Bw$.

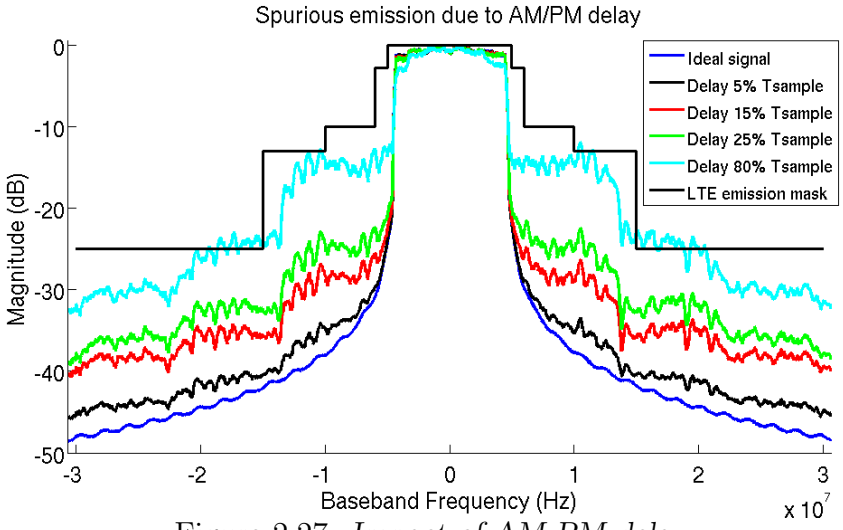


Figure 2.27: *Impact of AM-PM delay*

The phase delay creates spurious emission in the adjacent channel and also distort the in-band signal degrading the EVM [38],[39],[40].

In the case of polar transmitter, the phase modulator needs to tune the phase of the carrier and is challenging. A phase modulator is presented in Figure 5.3. It is basically an IQ modulator with constant envelope.

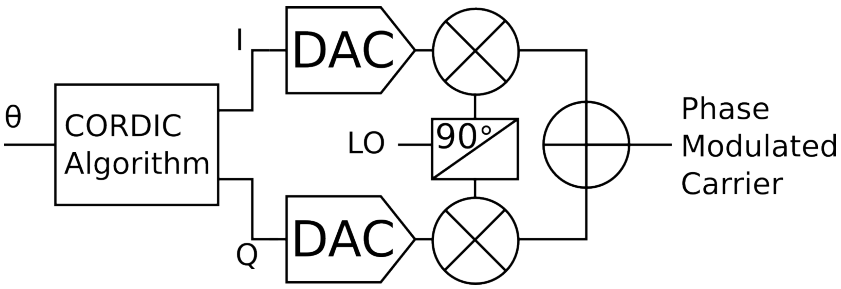


Figure 2.28: *Phase modulator based on IQ modulator*

The main advantage is the wider bandwidth compared to VCO-based solutions. However, its suffers from the Cartesian disadvantages.

The phase modulator implementation is a prolific research filed. Several approaches based on digital PLLs [41, 42] or digital phase modulators [43, 44] offer good characteristics in terms of bandwidth and digital control of the phase.

The [43, 44] approaches require sample rates higher than the carrier frequency which is not suitable for RF transmitters and will not be detailed here. The works of [5, 41] on digital polar transmitters based on all-digital PLL (ADPLL) are presented in Figure 2.29.

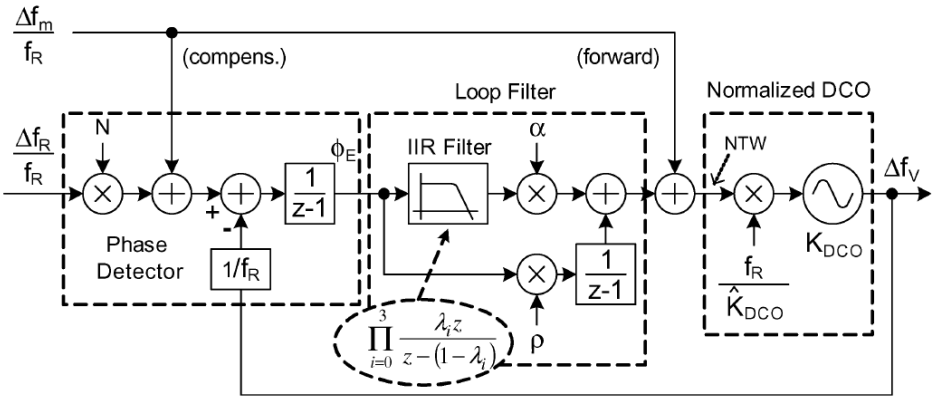


Figure 2.29: *ADPLL [5]*

This ADPLL allows the phase and frequency modulation with low area and low power consumption. The implementation in [41] is able to cover several standards with low constraints on the feed-back delay. The high bandwidth is obtained thanks to a 2-point modulation. The high frequency component of the phase information directly controls the DCO. While, the low frequency component is driven through the feedback loop in order to follow the slow deviations.

2.4 System level optimization

As describe in the first section, the PA impacts several aspects of the overall transmitter. The two addressed in this section are the efficiency and linearity. Of course, they can be improved by components level optimization like higher harmonic blockers for class-F PA. However, this section will focus on the architecture based optimizations. First, the compensating architectures will be detailed. Their principle is to suppress the PA non-linearities by processing before or after the power stage. Finally, architectures insensitive to the PA non-linearities will be presented.

2.4.1 Architectures with non-linearities compensation

The PA can be used in the linear region, then no distortions will appear, this technique is called power back-off. The main drawback of this solution is the degradation of the efficiency and are not suitable for hand-held systems. The next part of this section will focus on architectures offering linearity improvement while looking to their impact on power consumption.

Feed-forward

The first approach lets the PA produces distortions then delete them. This is done by the injection of the distortions with 180° phase shift. This technique known as Feed-forward Linearization is represented in Figure 2.30, and was first introduced by Black [45]. The idea is to sense the main PA output and only keep the distortions by attenuating and removing the fundamental. Then the attenuated distortions are amplified by an auxiliary PA (auxPA). Their low power level allows the auxiliary PA to work in its linear region, so the distortions do not generate new inter-modulation at the output. The initial inter-modulations can then be canceled. The main drawback of this implementation is the need of a second amplifier which degrades the overall efficiency. The auxiliary amplifier needs to be linear enough to avoid any inter-modulation of the distortions and its gain must be chosen carefully in order to exactly suppress the distortions. Delay elements are used to equal electrical path and increase bandwidth.

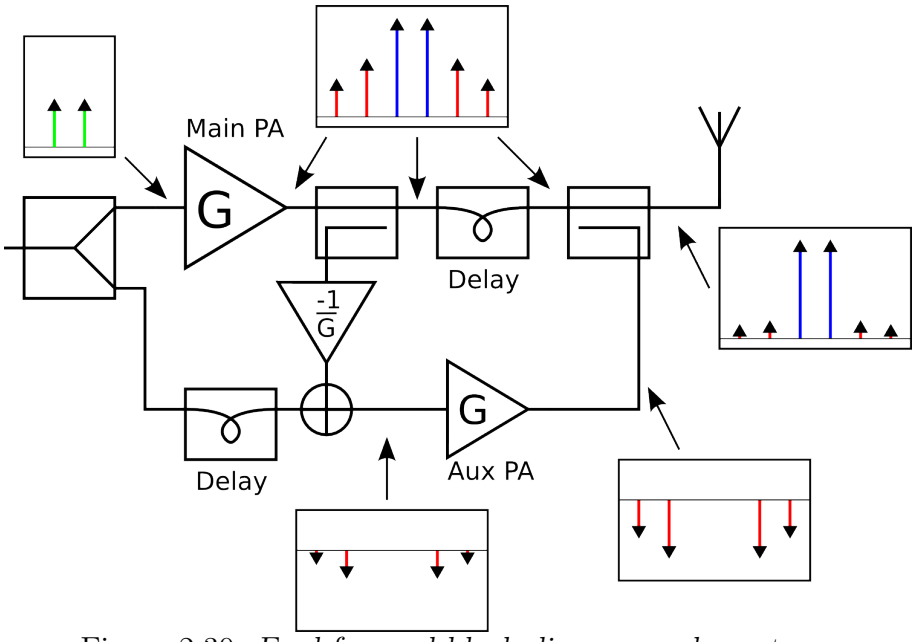


Figure 2.30: *Feed-forward block diagram and spectrum*

The second problem is the slow derivatives of the PAs characteristics. In order to avoid any degradation of the system over the time, some feedback must be implemented to tune the delays, gain and attenuation of the architecture. [46] presents such an implementation.

Pre-distortion

The last method able to linearize a transmitter is to perform pre-processing before the PA. Figure 2.31 illustrates such approach. If a non-linear component is used before the PA, and if the transfer function of this element is the inverse of the PA non linearity, then the overall behavior will be linear.

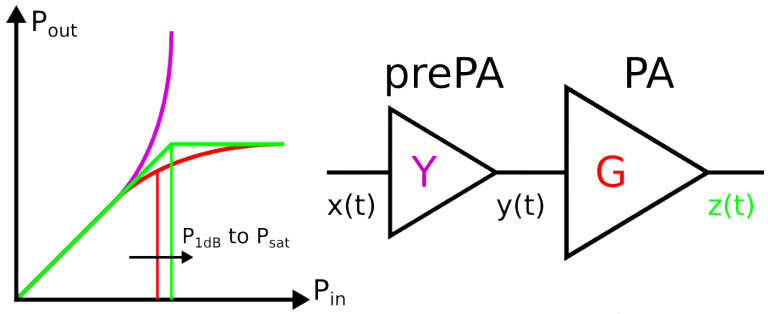


Figure 2.31: *pre-Distortion principle*

Recent implementations [47],[48] tend to directly perform the pre-distortion process in the digital domain with reversed models of the PA and also adaptive feedbacks in order to follow low frequency deviations.

The PA non-linearities are characterized by the AM-AM and AM-PM behaviors. They can be implemented directly on the envelope path in polar transmitter. Figure 2.32 shows a typical pre-distortion implementation in polar architecture where the AM-AM and AM-PM distortions are corrected.

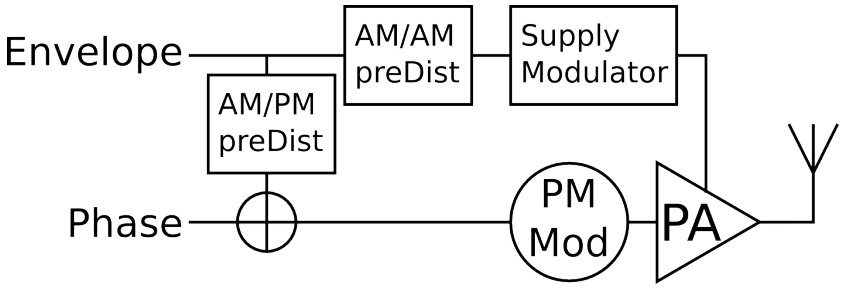


Figure 2.32: *pre-Distortion in polar architecture*

The polar architecture implemented with baseband pre-distortion seems to be a good candidate in terms of linearity and reconfigurability thanks to digital baseband processing.

2.4.2 Architectures unsensitive to non-linearities

Some approaches can handle non-linear components but avoid any distortions. Three techniques will be discussed here: the LINC, the EER and the poly-phase architectures.

LINC

LINC stands for LINear amplification with non-linear Components and was first introduced by Chireix [49], this technique is also known as the out-phasing technique. This technique is based on the fact that distortions generated by non-linear systems are mainly due to the variations of signal amplitude. Then constant envelope signals will introduce less distortions. The LINC architecture is illustrated on Figure 2.33 where the initial signal is split in two signals (V_{I1} and V_{I2}) with constant amplitude by the Signal Component Separate (SCS). Their amplification by the PAs does not produce any distortions. The two signals (V_{O1} and V_{O2}) are then recombined resulting in the original signal amplified by two times the PA gain.

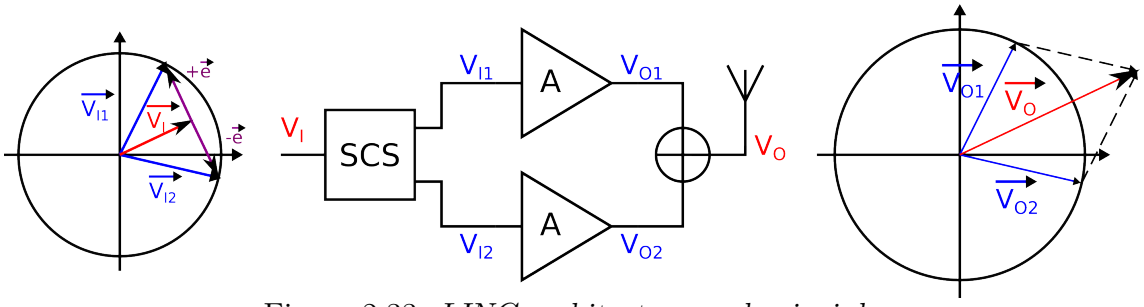


Figure 2.33: *LINC architecture and principle*

With: $\vec{V}_{I1} = \vec{V}_I + \vec{e}$; $\vec{V}_{I2} = \vec{V}_I - \vec{e}$ and $\vec{V}_O = \vec{V}_{O1} + \vec{V}_{O2} = A.\vec{V}_{I1} + A.\vec{V}_{I2} = 2A.\vec{V}_I$

This technique presents two main difficulties. First, the SCS must be able to manage wide-bandwidth signals. Second, the PAs must be well-matched to avoid any distortions during recombination. The state of the art shows interesting implementations in the case of all-digital transmitters [50, 51]. [6] presents an out-phasing transmitter where the recombination of the PAs is done through a transformer as represented on Figure 2.34, with an asymmetrical structure.

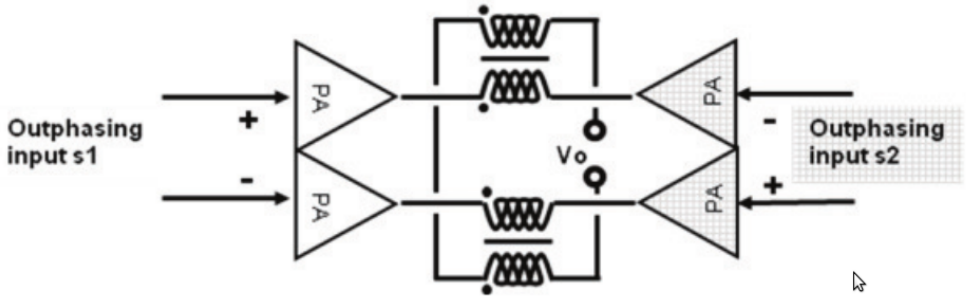


Figure 2.34: *Out-phasing with transformer-based combiner [6]*

EER

The Envelope Elimination and Restoration (EER) was first proposed by Kahn [52]. Like the LINC approach, EER systems take advantage of low distortion when a constant envelope signal is applied to a non-linear amplifier. The typical implementation is presented in Figure 2.35 as proposed by Kahn. A limiter generates a constant envelope signal keeping the phase modulation of the original signal. In parallel, an envelope detector directly controls the power supply of the PA with the amplitude information. Then, the signal is reconstructed at the PA output.

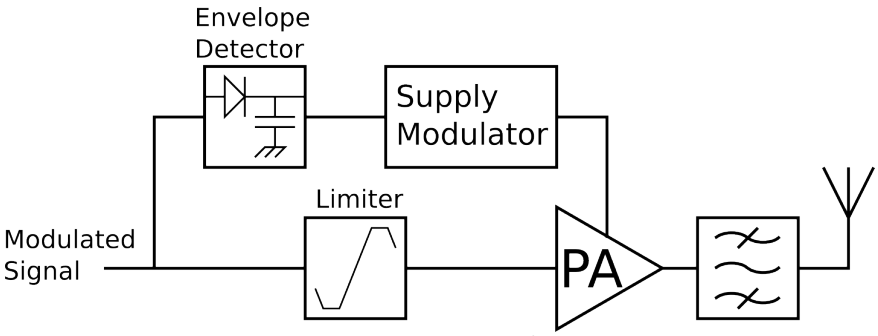


Figure 2.35: *EER architecture*

The first advantage is the ability to use the PA to its maximum power without spectral degradation. This leads to a better efficiency compared to Envelope Tracking (ET) system. The general setup is similar to a polar architecture with the phase modulated carrier amplified by the envelope-controlled PA. The PA efficiency shows a maximum when used at the maximum output power as represented in Figure 2.36. Nevertheless, the maximum of the probability density function (PDF) of a typical application is located at lower power level. The mean efficiency of the PA is largely lower than the maximum. When envelope modulation is performed on the PA supply, the PA can work with a constant envelope signal and then shows an high and constant efficiency.

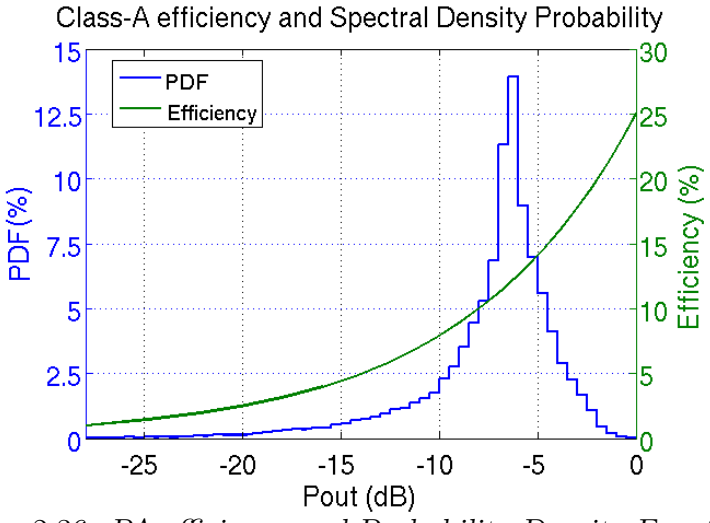


Figure 2.36: *PA efficiency and Probability Density Function*

Poly-phase approach

Mensink [53, 54] proposed a new architecture based on a poly-phase approach, as an extension of the differential approach. In the case of differential amplifiers, the 180° phase shifted signals (π) are recombined in order to suppress even harmonics. Mensink introduced a wider diversity in the system by using N parallel paths where a phase shifting is performed before and after the PA as illustrated on the Figure 2.37.

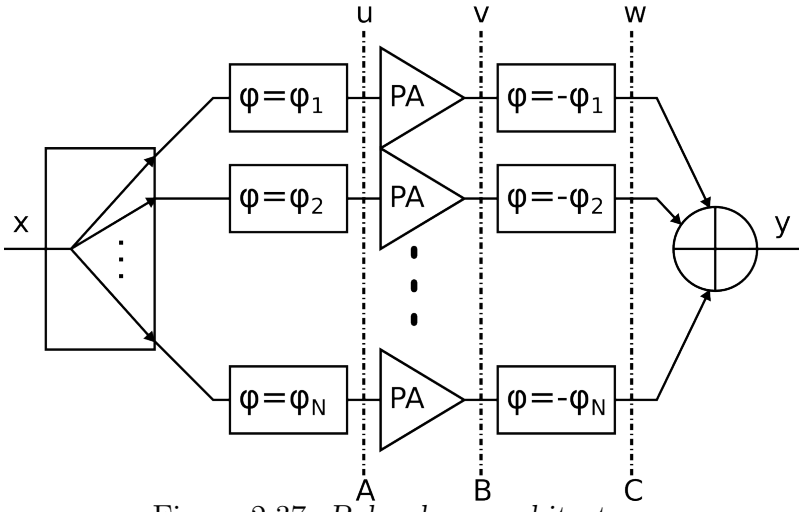


Figure 2.37: *Poly-phase architecture*

The mathematical 3rd order representation is detailed in (2.12), (2.13) and (2.14):

A:

$$u(t) = \cos(\omega_0 t + \varphi) \tag{2.12}$$

B:

$$\begin{aligned} v(t) &= a_1 \cos(\omega_0 t + \varphi) + a_3 \cos^3(\omega_0 t + \varphi) \\ v(t) &= (a_1 + \frac{a_3}{2} + \frac{a_3}{4}) \cos(\omega_0 t + \varphi) + \frac{a_3}{4} \cos(3(\omega_0 t + \varphi)) \\ v(t) &= b_1 \cos(\omega_0 t + \varphi) + b_3 \cos(3(\omega_0 t + \varphi)) \end{aligned} \tag{2.13}$$

C:

$$w(t) = b_1 \cos(\omega_0 t) + b_3 \cos(3\omega_0 t + 2\varphi) \tag{2.14}$$

The recombined signal is detailed in (2.15):

$$\begin{aligned} y(t) &= \sum_{i=1}^{N} (b_1 \cos(\omega_0 t) + b_3 \cos(3\omega_0 t + 2\varphi_i)) \\ y(t) &= N b_1 \cos(\omega_0 t) + \sum_{i=1}^{N} b_3 \cos(3\omega_0 t + 2\varphi_i) \\ y(t) &= N b_1 \cos(\omega_0 t) + \alpha \end{aligned} \tag{2.15}$$

The α term is composed of several sinusoidal signals with the same frequency but different phase shifts. These phases depend on the phase shifting performed on each path. This term can be canceled. if the phase shifting on each path is correctly adjusted. Figure 2.38 illustrates the process for a 3-path architecture at different nodes of the system. As we can see, the third harmonic is canceled. if the phase shifters are set with a $2\pi/3$ step. The number of harmonics canceled by the poly-phase architecture depends on the number of paths. Mensink works with differential amplifiers, where each amplifier is composed of $2N + 1$ paths. So, all even harmonics are canceled and the odd harmonics up to $(2N + 1)^{th}$ harmonics are canceled. This implementation is really innovative due to its ability to manage spurious emissions far away from the fundamental. Nevertheless, increasing the number of paths requires fine phase shifts limiting the feasibility. The main drawback of this solution is the impossibility to cancel inter-modulation around the fundamentals (e.g : $2\omega_1 - \omega_2$; $2\omega_2 - \omega_1$; $3\omega_1 - 2\omega_2$; ... for 2-tone signal). In conclusion, this solution offers good capability of wide-band harmonic rejection, but still needs a standard approach in order to linearize the system around the fundamental.

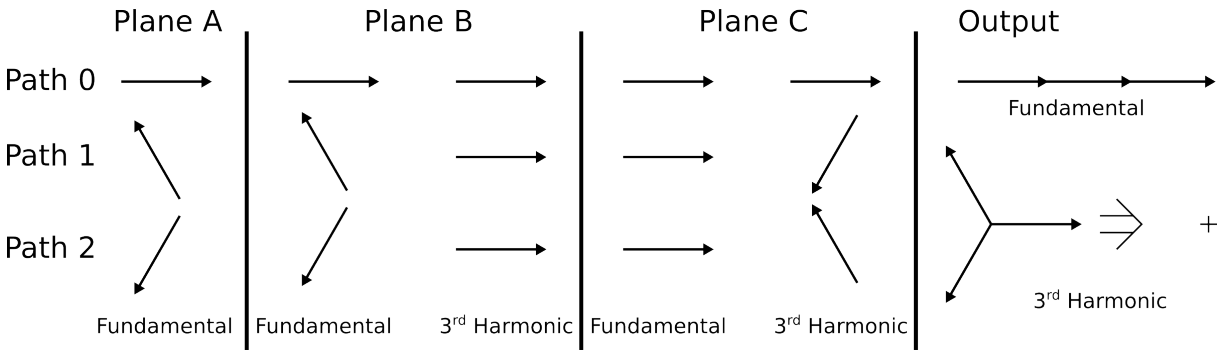


Figure 2.38: *Poly-phase technique: 3-path example*

An overview of the main linearization schemes and power optimization have been detailed in this paragraph. The EER architecture together with a pre-distortion appears as a good candidate to linear and efficient polar system. They also offer high reconfigurability thanks to baseband digital processing. As shown in the EER discussion, the power efficiency can be improved but the maximum power provided by the PA still depend on the PA implementation as power supply limit of the process. The next section will detail the solutions in order to increase the power provided by these low power processes.

2.5 Power recombination in multiple paths architectures

As explained in the previous section, the maximum power provided by a PA highly depends on the process. Mixed-signal components and RF functions tends to be integrated in processes dedicated to low power and high speed digital processing. In this case, the high power level required by current standards (+25 dBm for LTE; +20 dBm for 802.11) becomes more and more challenging. Figure 2.39 shows the evolution of the typical supply voltage for different technology nodes and the required load for a class-A PA delivering +30 dBm. This section will detail the main techniques to increase power, and will be followed by a discussion on the matching between the PA and the antenna.

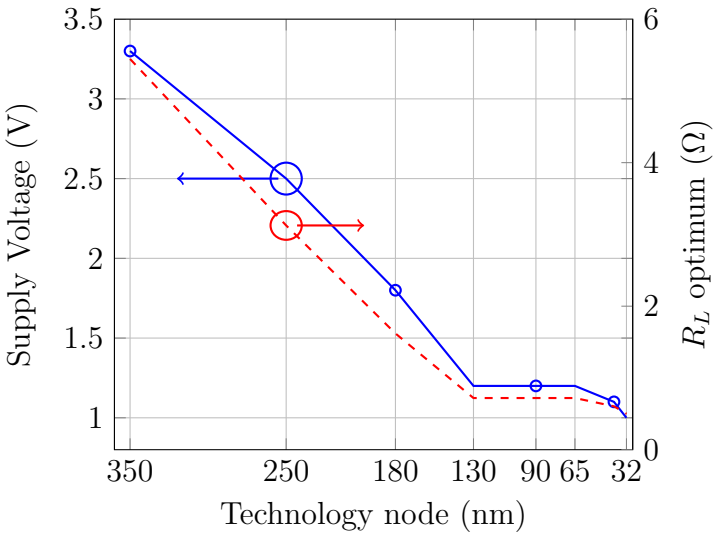


Figure 2.39: *Evolution of the Power Supply*

As represented in Figure 2.39, the optimum load greatly decreases with the power supply. Low impedance means high currents, which could violate the electro-migration rules of the process and make the design challenging. Moreover, the antenna requires high impedance in order to easily excite the desired mode. Then, the PA-Antenna connection requires impedance matching. However, high transformation ratio impacts the achievable bandwidth and insertion losses.

At the transistor level, the cascode structure as represented in Figure 2.40 can greatly increase the available headroom by stacking a thick oxide transistor on top of the gain transistor with thin oxide. This allows the increase of the supply voltage beyond the limit of the process and results in a higher optimum load. As an example, if the maximum voltages are 1.2V for the thin oxide and 2.5V for the thick oxide transistors, the optimum load for a +30 dBm class-A PA is transformed from 0.72Ω @ 1.2V to 6.86Ω

@ 3.7V. The matching constraints are obviously alleviated, but the design still require a high transformation ratio.

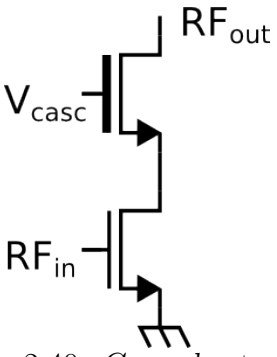


Figure 2.40: *Cascode structure*

Multiple paths approach

If a single amplifier can not reach the required power, then several amplifiers in parallel could. In the approach presented in Figure 2.41, the paths in parallel need to be recombined and matched to the antenna. The main constraints of the power combiner is to provide the optimum load to the amplifiers (Z^*_{PA}) over a wide band and an output impedance (Z_{PC}) close enough from the antenna impedance (Z^*_{ANT}) to lower the impedance transformation ratio done by the matching network. The following paragraphs propose a quick overview of the different implementations. The impact of the power combining scheme on the impedance presented to the matching network will also be detailed.

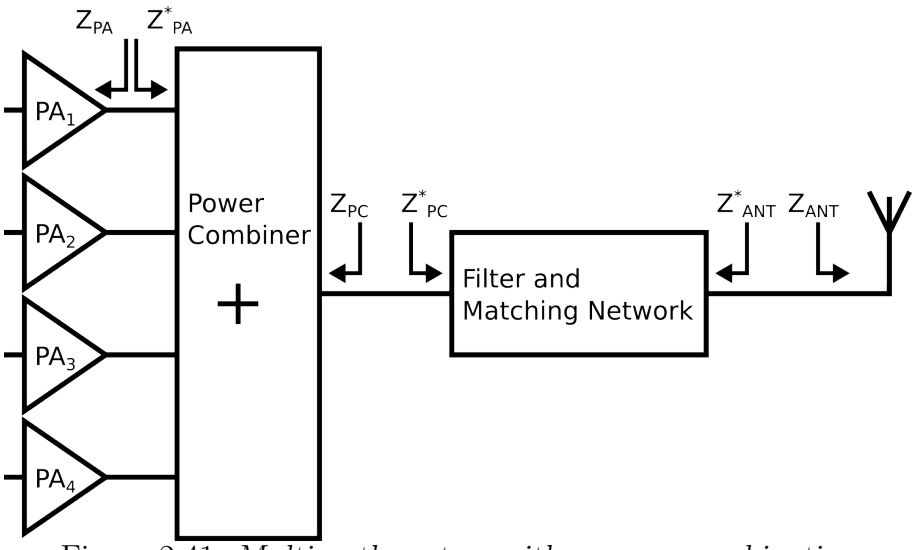


Figure 2.41: *Multi-path system with power recombination*

Direct current recombination

The simplest implementation is based on direct current recombination as illustrated on Figure 2.42. The two main advantages are the low insertion losses and the easy implementation. But two drawbacks limit its utilization. First, current recombination means that the currents are added which increases the risk of electro-migration. Second, the impedance presented to the matching network is the PAs impedances in parallel which is $4Z_{PC} = Z_{PA}$. The matching network needs to transform a lower impedance to the antenna, which results in more complicated matching network and increased insertion losses.

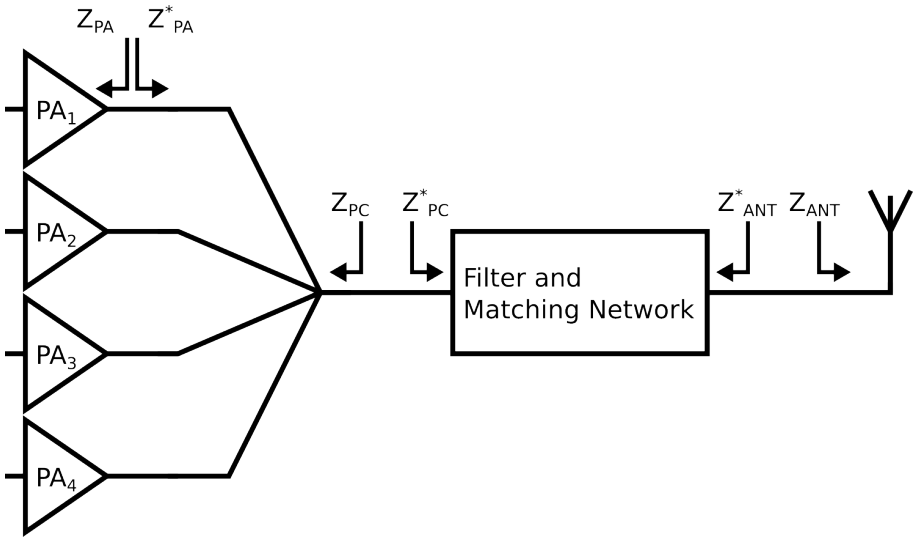


Figure 2.42: *Power combiner based on current recombination*

The digital PA proposed by Kavousian [7] is based on current recombination of four PAs. The recombination is done on-chip with centrally located bond pads as can be seen in Figure 2.43. The output drains of the four PAs are tied together to the PADs.

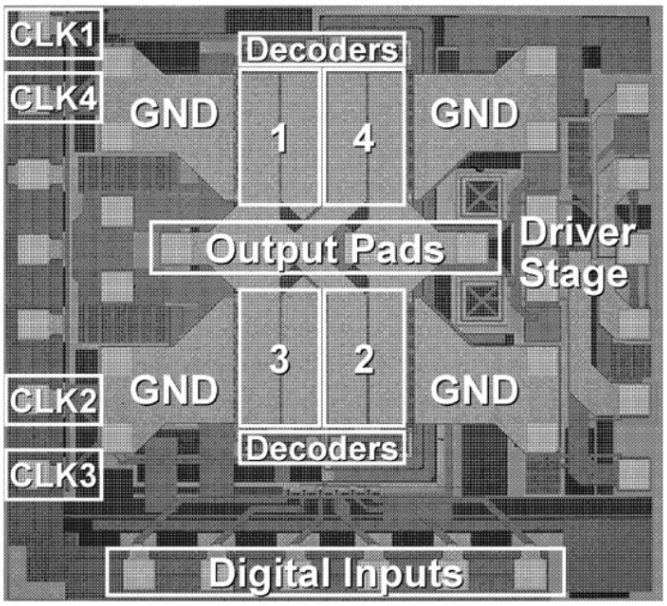


Figure 2.43: *Die micro-graph of PA with current recombination [7]*

Wilkinson Combiner

The power recombination by a Wilkinson Combiner [55, 56, 57, 58, 59] is one of the most used power combining techniques. The 2-way combiner illustrated on Figure 2.44 is based on two quarter wavelength transmission lines.

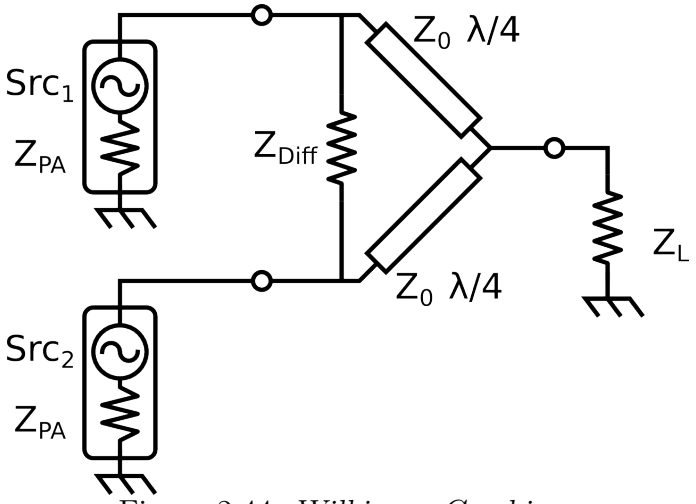


Figure 2.44: *Wilkinson Combiner*

The transmission lines allow in-phase power recombination by summing both waves and performing an impedance transformation. This last property could alleviate the transformation ratio required by the matching network. Figure 2.45 shows the standard representation of a transmission line with the characteristic impedance Z_0, the electrical wavelength l and load impedance Z_L.

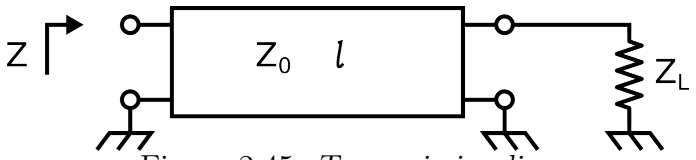


Figure 2.45: *Transmission line*

$$Z = Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)} \tag{2.16}$$

Equation (2.16) defines the impedance Z seen at the transmission line extremity when loaded by Z_L on the other port, where γ is the propagation factor defined as: $\alpha + i\beta$, with α the linear attenuation and β the wave-number equal to $2\pi/\lambda$.

Assuming no insertion losses ($\alpha = 0$) Equation (2.16) becomes:

$$Z = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \tag{2.17}$$

Then, in case of quarter wavelength line at a dedicated frequency f_0, $l = \lambda/4$ which combined with Equation (2.17) results in:

$$Z = Z_0 \frac{Z_L + jZ_0 \tan(\pi/2)}{Z_0 + jZ_L \tan(\pi/2)} \tag{2.18}$$

The load impedance Z_L is transformed into Z_0^2/Z_L. Using this property of the transmission line, the Wilkinson power combiner is able to present different impedance to the PAs in Common and Differential modes. Figure 2.46 shows the Wilkinson combiner from Figure 2.44 and the equivalent half-circuit when common and differential signals are applied. In common mode (CM), the waves are recombined on the second port and the differential impedance (Z_{Diff}) can be ignored due to the symmetry. All the power from the sources is delivered into the load, and no reflections occur. In differential mode (DM) the transmission lines are virtually grounded on the output port which according to Equation (2.18) result in an open circuit on the input ports. Finally, all the power from the sources is dissipated into the differential load without reflection if $Z_{Diff} = 2Z_L$.

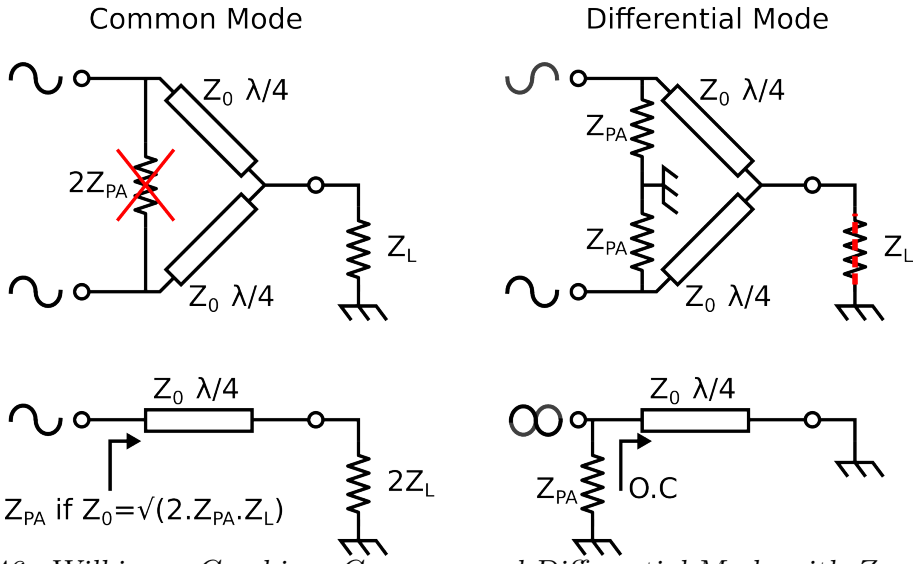


Figure 2.46: *Wilkinson Combiner Common and Differential Mode with* $Z_{Diff} = 2Z_{PA}$

The approach can be extended to more paths as represented on Figure 2.47 with 4-way system.

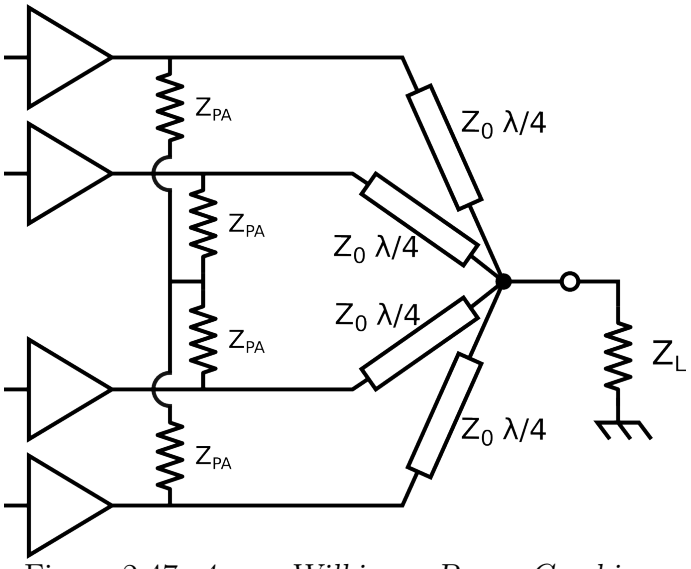


Figure 2.47: *4-way Wilkinson Power Combiner*

Flament [60] presents an analog FIR with transmission line based combiner. The PA stage was implemented in bulk CMOS while the transmission lines where implemented by lumped elements in an Integrated Passive Device (IPD) process.
The main disadvantages of these approaches are the large area required and the intrinsic narrow band behavior of the transmission lines. Thus, the ideal recombination can only be performed at one frequency [61].

Transformer-based combiner

The final power combining technique explained here, transformer based power combining is also the most versatile one. As it will be detailed, the power recombination based on transformer offers an easy way to perform impedance transformations. A simplified model of a transformer [62] is presented in Figure 2.48, where k_m is the coupling factor between both primary and secondary inductors and n is the turns ratio. The primary and secondary self inductors are noted L_P and L_S while r_P and r_S denote their ohmic losses. In order to simplify the model, parasitic capacitances and the skin effect are neglected.

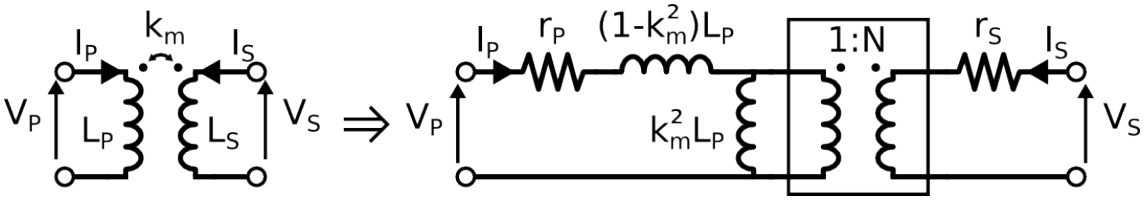


Figure 2.48: *Transformer model*

Where: $\frac{1}{N} = k_m\sqrt{\frac{L_P}{L_S}}$
Figure 2.49 represents the simplified model of transformer without losses ($r_P = r_S = 0$) and perfect coupling ($k_m = 1$).

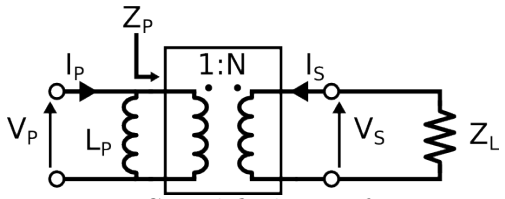


Figure 2.49: *Simplified transformer model*

In this case, the impedance on the primary side is $Z_P = \frac{Z_L}{N^2}$
Transformers can be used in several ways to perform power recombination, depending on the winding configuration (serial or parallel). [4] and [8] present the recombination of several paths based on transformers in a serial configuration. Figure 2.50 and Figure 2.51 represent the schematic and the annotated layout from [8]. The radiated magnetic filed is largely reduced by alternating the directions of each winding, this avoids interference with other integrated blocks.

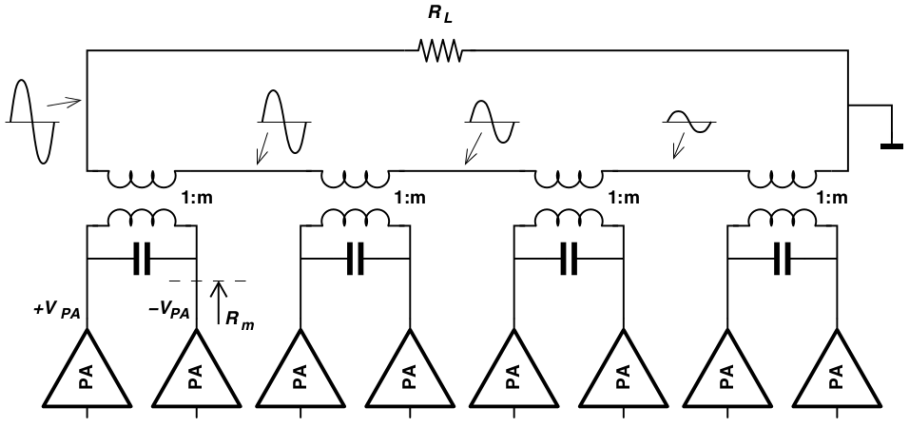


Figure 2.50: *Reynaert [8] schematic*

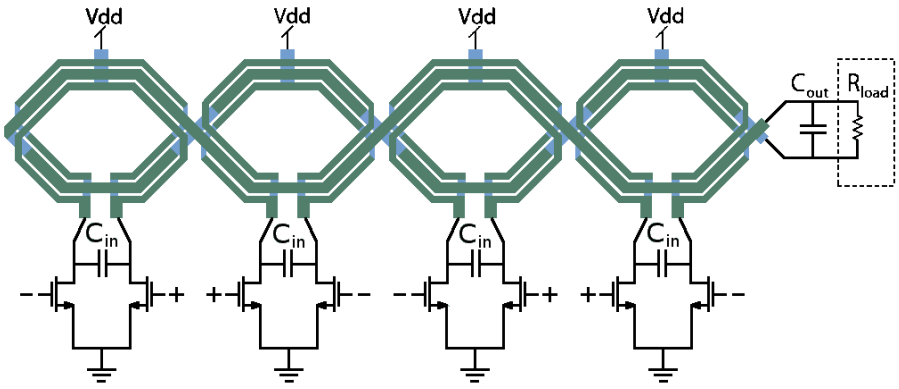


Figure 2.51: *Reynaert [8] Layout*

The main advantage of this implementation is the impedance ratio. As represented on Figure 2.50, if the transformers are supposed ideal with $N = 1$ then $R_L = 8R_m$. High impedances can be obtained in architectures with more than four paths.

On the other side, [9] proposes a parallel configuration. Figure 2.52 illustrates this implementation. The idea is to sum the magnetic fields in order to increase the output current. The most interesting implementation is the serial configuration as used by [4] and [8]. However, coplanar transformers implemented in advanced technologies offer low quality factors (10max) compared to dedicated processes (typically > 50).

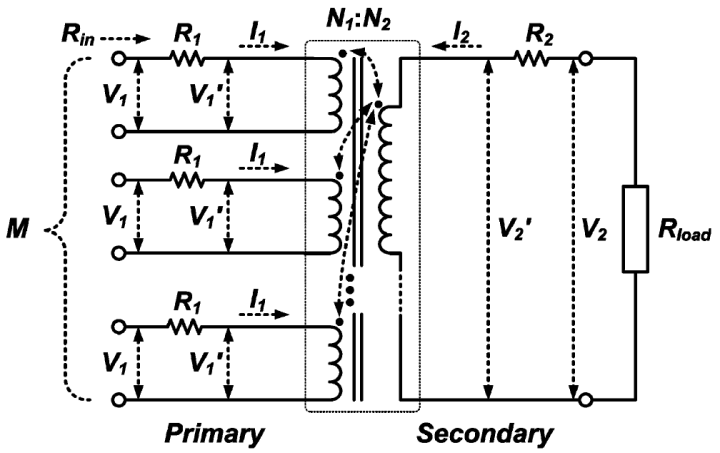
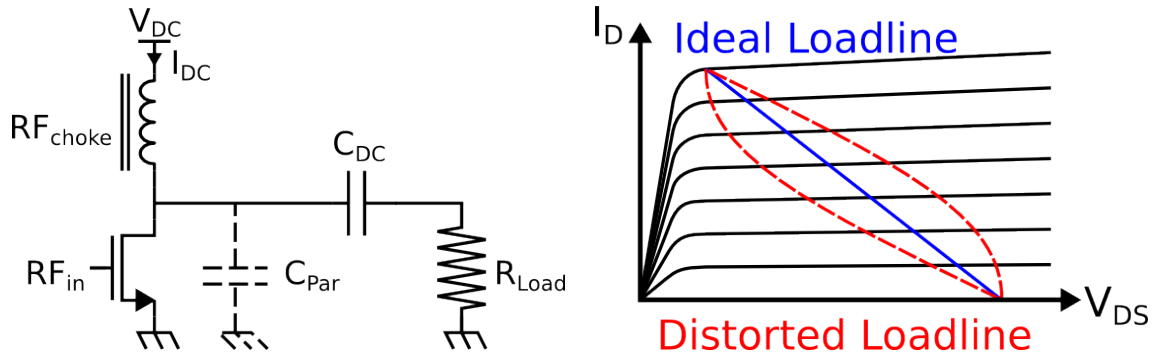


Figure 2.52: *Power Combiner with Parallel Transformer (PCT) [9]*

The design of coplanar transformers with several primary windings in CMOS process limits the transformation ratio between primary and secondary sides close to 1. Then, this solution suffers from a lower load impedance than the output impedance of the PA similar to direct current recombination technique.

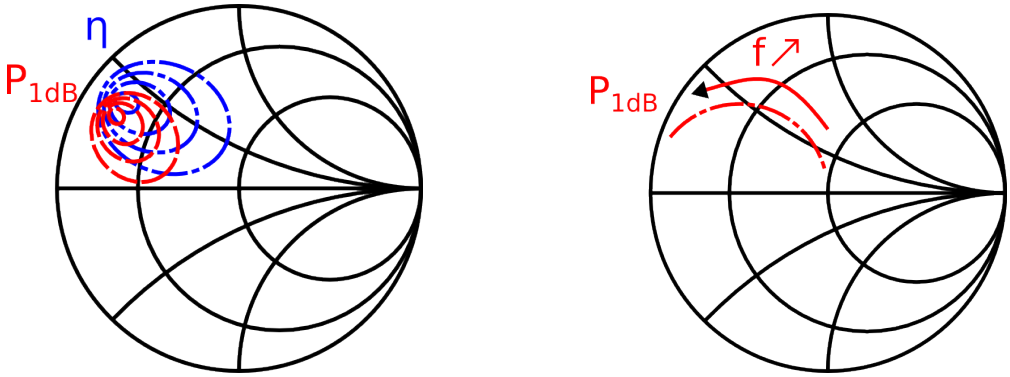
Wide-band impedance matching

Besides the power recombination aspect, the amplifier output impedance approximated by a resistance is not a good wide-band model. In fact, the power stage output presents a parasitic capacitance which distorts the load-line characteristic. Figure 2.53 shows the schematic of a common source amplifier with parasitic capacitance. The distorted load-line and optimum load on a Smith chart are also illustrated.



a) Common Source PA with Parasitic C

b) Load-line distortion



c) Constant Circles

d) Ideal Z_L versus frequency

Figure 2.53: *PA output impedance with Load-pull measurement*

In order to accurately model the optimum PA output impedance under large signal, load-pull measurements is a useful technique [26]. Load-pull characterization consists of measuring the PA performances while sweeping its load impedance along the Smith chart. A map can then be drawn for each PA characteristic, such as efficiency or maximum power delivered to the load. The impedances for which the PA presents an equal performance are connected together and called circles. As an example, Figure 2.53.c) shows a Smith chart

where circles at different levels of efficiency and maximum power are plotted for a single frequency. The optimum load impedance for a given performance can then be defined as the approximate center of the circles, this optimum load impedance can be plotted versus frequency. For example, Figure 2.53.d) shows the optimum PA load impedance to ensure maximum P1dB over the considered frequency band.

In order to cover enough bandwidth, the matching network must cancel the capacitive effect over a wide frequency band. Figure 2.54 shows a parallel inductor with a fixed value, it is a suitable solution for narrow band systems, around 1.1 GHz in this example. However its reactive part changes in inverse proportion than the reactive part of the capacitor, which limit the frequency band with good compensation.

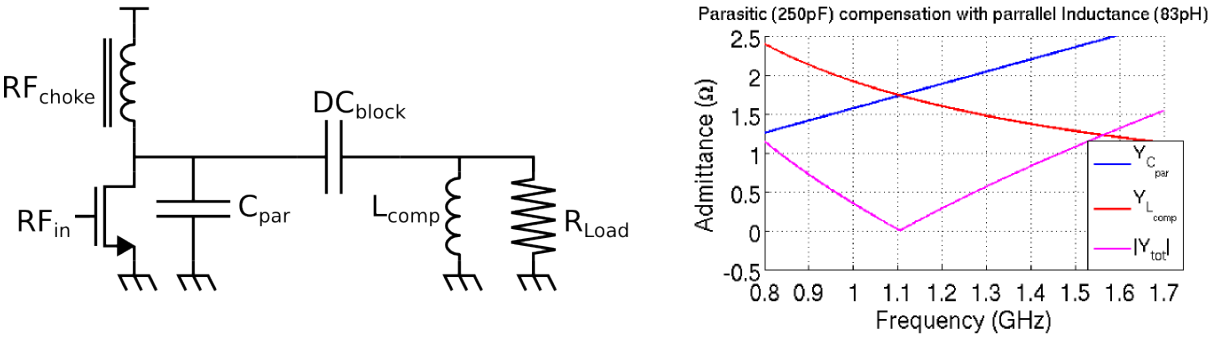


Figure 2.54: *Parasitic capacitance compensation with parallel Inductor*

[63, 64, 65, 66] propose to tune the inductor and capacitor values in order to follow the variation of the parasitic reactance. [63, 64] use a tunable active inductor. This solution degrades the efficiency due to the inductor biasing and also requires a large dynamic range to support the output swing of the PA. The last problem is the low bandwidth covered by the active inductance.

[65, 66] are based on switchable L and C banks. Figure 2.55 represents a matching network principle with adjustable sections. Figure 2.56 shows a possible configuration with switchable L and C components.

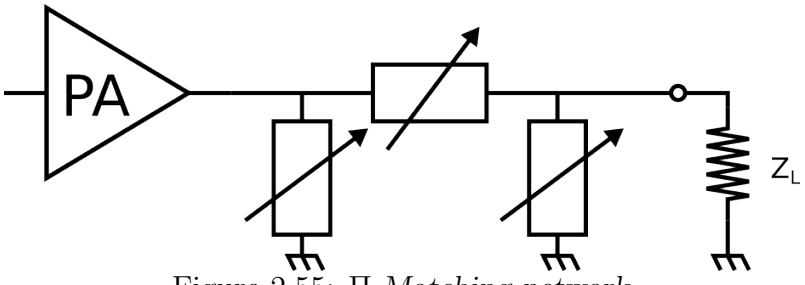


Figure 2.55: Π *Matching network*

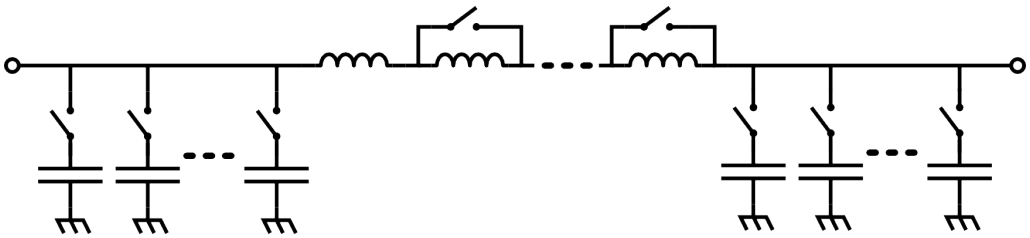


Figure 2.56: Π *network with LC Banks*

The main drawback is the need of analog switches introducing losses and parasitics. The implementation of the L-bank is also challenging due to size and coupling between windings.

In [10], a bank of matching networks is presented in order to select the one covering the required frequency band. Of course, this implementation requires a very large area and high performance switches and is represented in Figure 2.57.

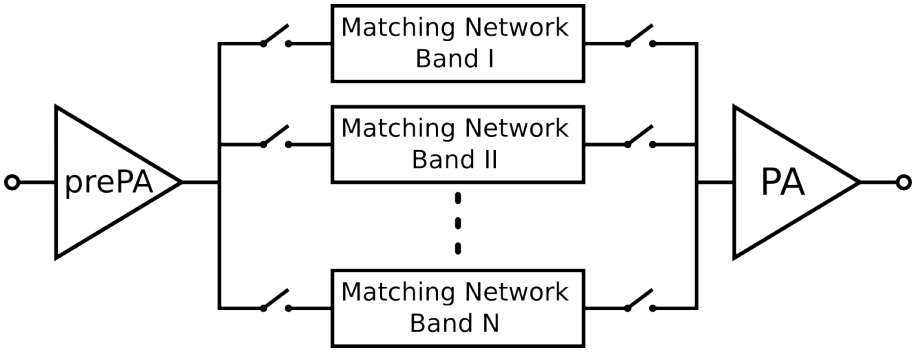


Figure 2.57: *Impedance matching with switchable Matching Network [10]*

The last possibility is to generate a wide-bandwidth matching network. The advantage is the lack of reconfiguration and switches. However, this approach implies trade-offs between the desired bandwidth and insertion losses. The feasibility depends on the model accuracy over the band of interest.

Wang [11] proposes a promising approach. This technique directly absorbs the parasitic capacitance in the matching network. Then, the capacitor does not waste power or limit the bandwidth anymore. Figure 2.58 presents the PA model while Figure 2.59 shows the transformations performed to the matching network. Finally, the matching network is implemented with a transformer.

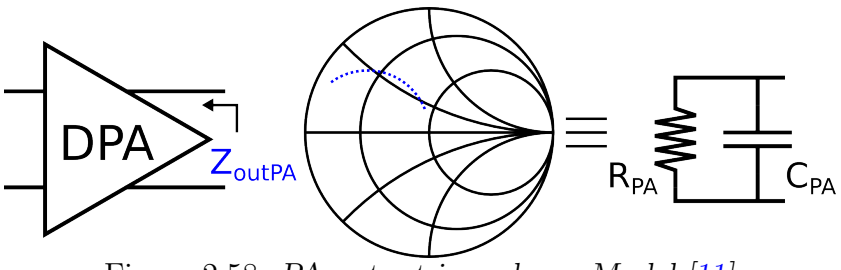


Figure 2.58: *PA output impedance Model [11]*

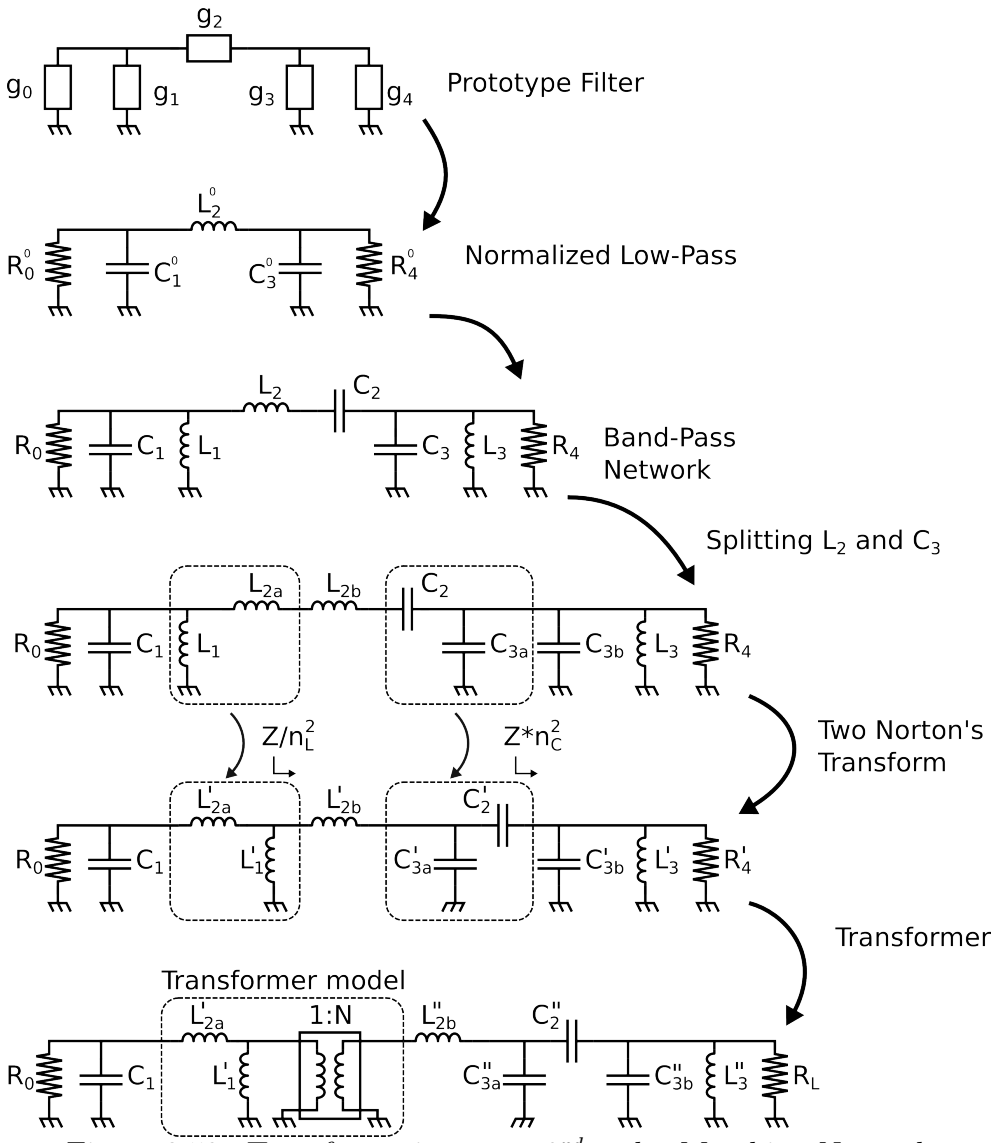


Figure 2.59: *Transformations on a 3^{rd} order Matching Network*

For the Normalized Low-pass Prototype:

$$R_0^0 = R_4^0 = 1 \qquad C_1^0 = g_1 \qquad L_2^0 = g_2 \qquad C_3^0 = g_3$$

For the Band-pass:

$$R_0^0 = R_4^0 = R_{PA} \qquad C_1 = \frac{g_1}{\omega_0 \Delta R_{PA}} \qquad L_2 = \frac{g_2 R_{PA}}{\omega_0 \Delta} \qquad C_3 = \frac{g_3}{\omega_0 \Delta R_{PA}}$$

$$L_1 = \frac{\Delta R_{PA}}{\omega_0 g_1} \qquad C_2 = \frac{\Delta}{\omega_0 g_2 R_{PA}} \qquad L_3 = \frac{\Delta R_{PA}}{\omega_0 g_3}$$

After Norton's Transform:

$$R_0 = R_{PA} \qquad L'_{2a} = \frac{L_{2a}}{n_L} \qquad L'_1 = \frac{L_1}{n_L}$$

$$L''_{2b} = \frac{L_{2b}}{n_L^2} * N^2 \qquad C''_{3a} = C_{3a} \frac{n_L^2}{n_C^2} \frac{1}{N^2} \qquad C''_2 = C_2 \frac{n_L^2}{n_C^2} \frac{1}{N^2}$$

$$C''_{3b} = C_{3b} \frac{n_L^2}{n_C^2} \frac{1}{N^2} \qquad L''_3 = L_3 \frac{n_C^2}{n_L^2} * N^2 \qquad R_L = R_4 \frac{n_C^2}{n_L^2} * N^2$$

with:

$$n_L = \frac{L_{2a} + L_1}{L_1} \qquad n_C = \frac{C_{3a} + C_2}{C_2}$$

Wang starts with a standard Chebyshev filter [67, 68, 69] performing the R_{PA} to R_{ANT} matching. The sections are modified in order to create a transformer model. The transformations based on Norton's transforms are detailed in [70]. [11] details the procedure taking into account the parasitic components and their impact on the set of achievable filters. In [11], the bandwidth of the proposed matching network depends on the coupling factor of the transformer and the coefficient product of the first section of the Chebyshev prototype ($g1.g2$). The overall architecture is presented on Figure 2.60. It is a two stage amplifier with 3^{rd} order interstage matching network based on the proposed design method. The PA covers 5.2 GHz to 13 GHz with a P_{sat} equal to 25.2 dBm as shown in Figure 2.61.

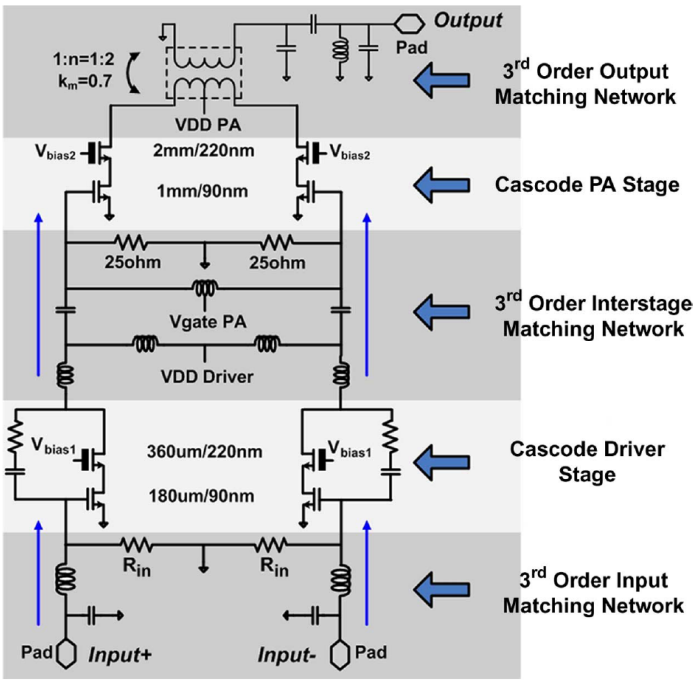


Figure 2.60: *PA implementation proposed in [11]*

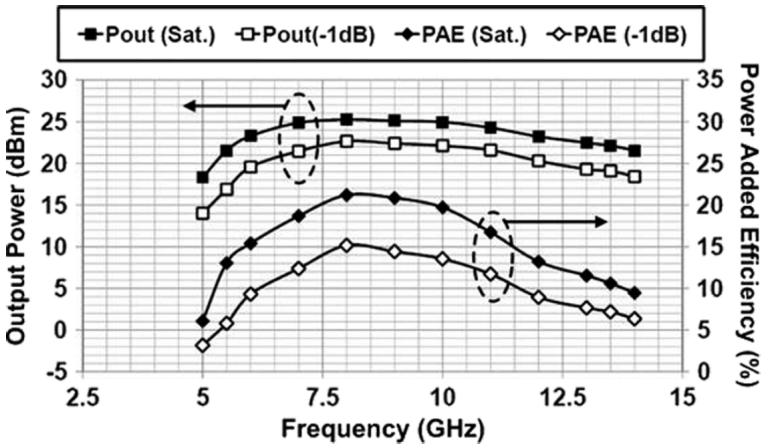


Figure 2.61: *PA characteristic in [11]*

As detailed in this section, the PA-Antenna connection is a challenging task in terms of power recombination and wide-band matching. Several solutions exist, but the methodology introduced by Wang [11] appears to be the most suitable candidate. Furthermore, the transformer allows impedance transformation and power recombination.

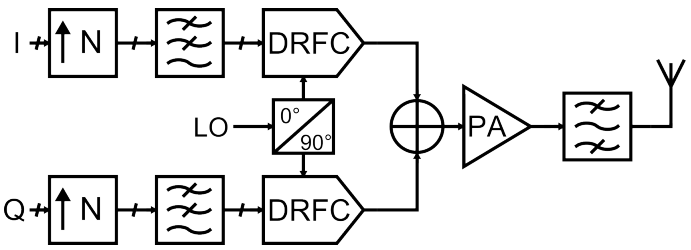
2.6 Digital Power Amplifiers

As explained in the previous section, the power stage design and passive integration are challenging tasks in advanced CMOS technologies. However, these processes present the great advantage to provide high digital processing density without impacting the power consumption. This paragraph will present a state of the art of digitally-implemented RF functions. Substituting the RF blocks by all digital blocks introduces distortions. These side effects need to be handled in order to respect the transmitter constraints.

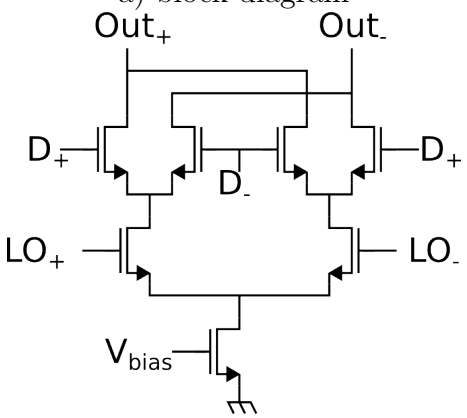
Digital-to-RF Converter

The first digital block used as RF block is the Digital-to-RF Converter (DRFC). It is basically a DAC and mixer merged together. The baseband digital signal is up-converted by the local oscillator. In this configuration there is no filtering between the digital-to-analog conversion and the up-conversion. The DRFC can be used in Cartesian transmitter to replace the DAC and mixer on both I and Q paths. The filters after the DRFC can also be suppressed.

Eloranta [12, 71, 72] presents a 10-bit DRFC implemented with a Gilbert cell matrix. It acts like a current-steering DAC. Each cell is based on a Gilbert cell performing the mixing of the digital LO with the baseband signal. The main advantage of this implementation is the direct current recombination of the I and Q signal. The block diagram of the implemented system in [71] and [12] is presented on Figure 2.62.a), while Figure 2.62.b) illustrates the simplified schematic of a cell. In [12], digital processing is performed before the DRFC, its role is to suppress digital aliases after up-sampling. The filter is implemented using cascaded FIR and IIR filters. The stability is ensured by cascading only 1st order IIRs, but this results in a shrunk bandwidth.



a) block diagram

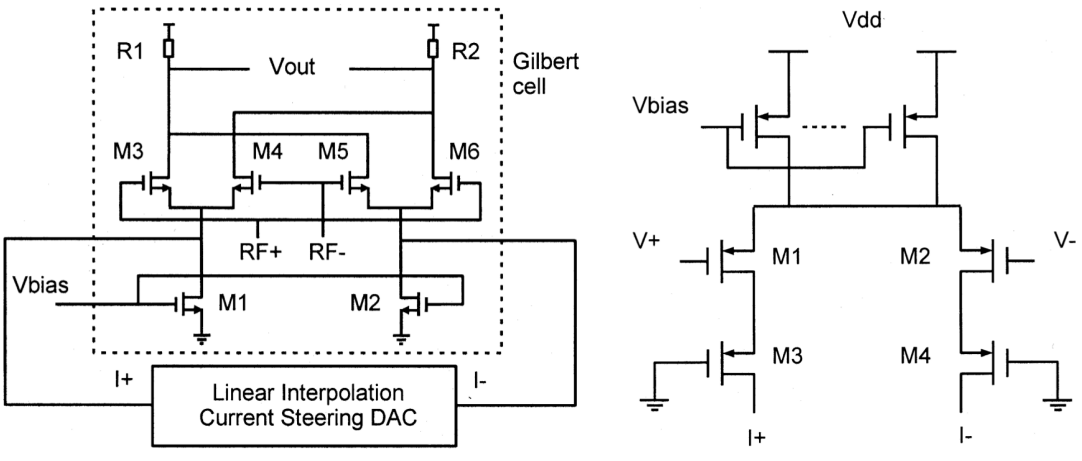


b) Cell schematic

Figure 2.62: *Eloranta DRFC [12]*

Due to the limited bandwidth of the system, the proposed digital transmitter only supports bandwidth up to 10 MHz around 2 GHz. The RF carrier depends on the clock distribution in the matrix, while the fixed matching network restrains carrier tuning. The architecture offers -2 dBm output power, what requires additional PA.

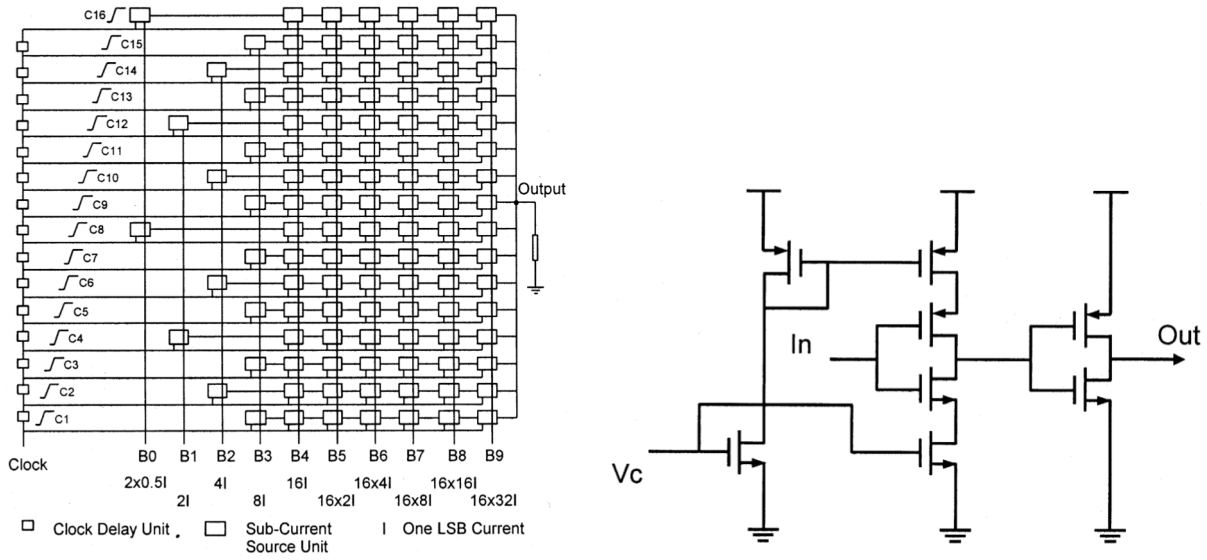
Zhou [13] proposes another DRFC implementation based on a 10-bit current-steering DAC. The main difference with Eloranta's approach is the structure of the DAC. Eloranta implements a mixer in each cell while Zhou only uses one mixer linked to an highly linear interpolation DAC. This configuration is illustrated on Figure 2.63.a) while Figure 2.63.b) represents a current cell of the DAC.



a) Current-steering DAC & Mixer b) Sub-current source unit

Figure 2.63: *Zhou DRFC [13] block diagram and schematic*

The linear interpolation term refers to the alias attenuation performed by a digital linear interpolation based on a 16-tap filter. This filter is represented in Figure 2.64.a). In order to avoid driving the DAC with a clock 16 times higher than the sample rate, 16 phase of clocks are generated by analog delays as represented in Figure 2.64.b). This limits the complexity of the clock distribution and power consumption. The 16 phase of clocks smooth the global switching of the current sources which filter the signal.



a) Linear DAC implementation & Mixer b) Voltage-controlled delay unit

Figure 2.64: *Zhou DRFC [13] DAC and current source*

The output power is -6.5 dBm for a 3.3 MHz bandwidth at 1 GHz. The squared sinc response of the linear interpolation results in a large ratio between the -3 dB bandwidth and the sampling frequency. Therefore, high bandwidth signals require a high sampling frequencies, which are limited by the tuning range of the analog delay. One drawback of this implementation is the impedance variation due to the switching of current sources directly connected to the output.

The main challenge of these implementations is the generation and distribution of the high speed quadrature clocks between both DRFC in Cartesian transmitter.

Digital Power Amplifier

Another digital block can replace RF block, contrary to the DRFC suitable for Cartesian architectures, this block is well suited for polar architectures and is regularly referenced as Digital Envelope Modulator (DEM). Unlike the previous approach which requires two DRFCs, the DEM is based on a digital phase modulator and a digital PA (DPA). Figure 2.65 shows the block diagram of this approach similar to a polar architecture.

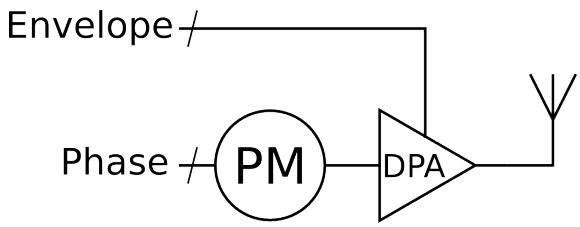


Figure 2.65: *Digital Envelope Modulator*

The phase modulator is basically implemented by a digital PLL. This block is a well-known element and will not be explained in this section. Staszewski [5] proposes an implementation and provides several details. The main challenges of this block are the bandwidth of the phase modulated signal and the center frequency tuning.

The DPA block deserves more attention, and will be detailed in this part. Its main advantage is to realize three baseband and RF function (DAC, PA and Envelope modulator) in only one component. Figure 2.66 represents a simplified model of the DPA. $a(t)$ represents the envelope information while $u(t)$ is the RF signal from the phase modulator, and G is the PA gain.

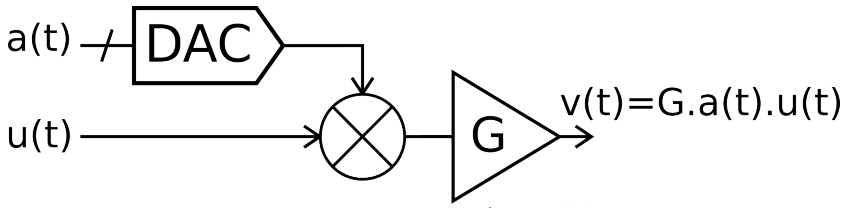


Figure 2.66: *DPA model*

Similar to Eloranta's DRFC based on a matrix of small mixers, the DPA can be implemented by a matrix of unit PAs. Figure 2.67 presents a 6bit DPA and the output signal swing for different Amplitude Code Words (ACW).

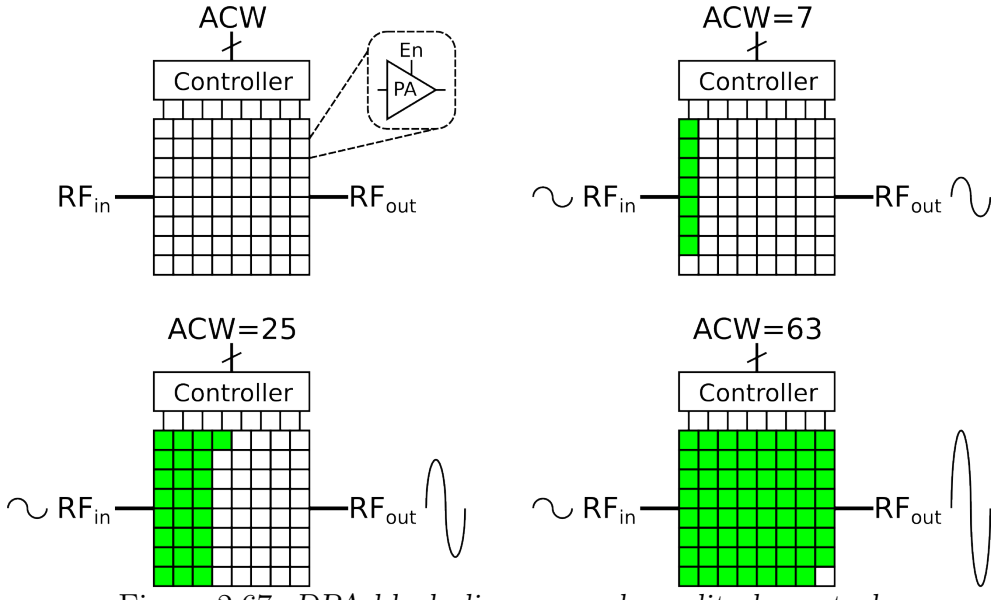


Figure 2.67: *DPA block diagram and amplitude control*

In [14] Van Zeijl presents a DPA with the simplest unit PA implementation. The unit cell schematic is represented on Figure 2.68 and shows the cascading of the switch and

the gain transistor. The gain stage can be driven in class-A,AB or C. The switch (M_{SW}) directly connects the drain of the gain transistor (M_G) to the RF output of the DPA when ON, but also isolates the gain transistor when OFF. Then the power consumption in off-state is null, increasing the overall efficiency.

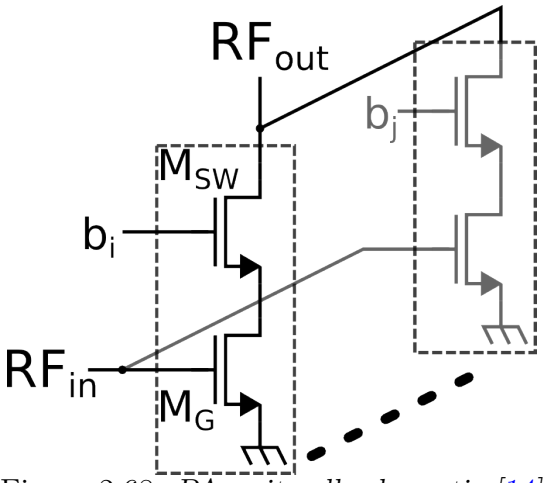
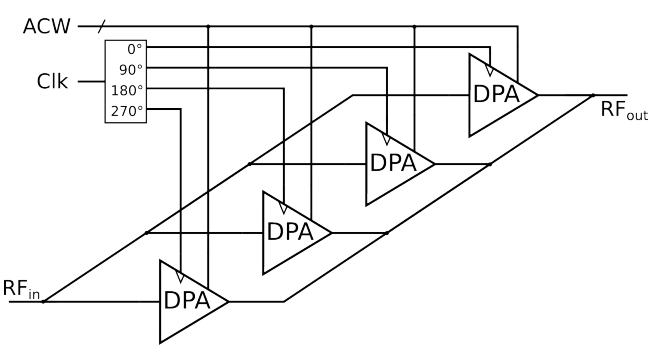
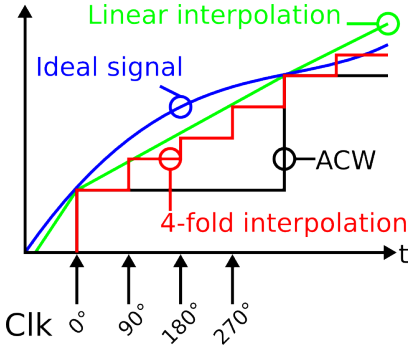


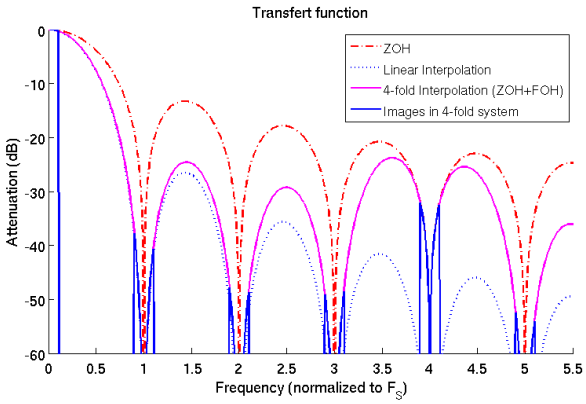
Figure 2.68: *PA unit cell schematic [14]*



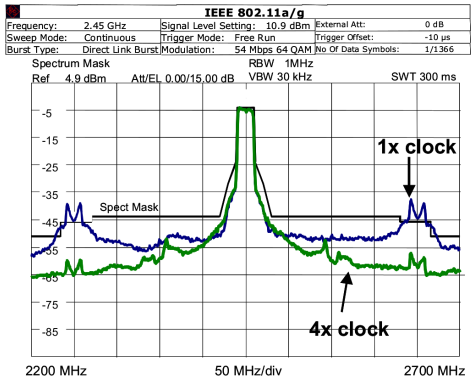
a) 4 DPA with quadrature clocks



b) 4-fold interpolation



c) Transfer function



d) Spectrum

Figure 2.69: *4-fold Linear Interpolation*

The DPA presented in [14] possesses an 8-bit resolution and a center frequency of 2.45 GHz. Its output power is 9 dBm for the 64QAM OFDM 802.11a/g standard, and 14 dBm for the 3 Mb/s medium-rate Blue-tooth standard. Besides, Van Zeijl implements a 4-fold linear interpolation by splitting the DPA matrix in 4 sub-DPAs. The clocks driving

successive sub-DPA are phase shifted by 90°. The block diagram and clock connections are represented on Figure 2.69.a), while the 4-fold interpolation is illustrated on Figure 2.69.b). The transfer function of the 4-fold interpolation is presented on Figure 2.69.c), and the output spectrum with and without interpolation is shown on Figure 2.69.d). As explained in the Zhou's DRFC case, L-fold linear interpolation attenuates replicas but also impacts the available bandwidth. This implementation only attenuates the first images which is enough for narrow bandwidth systems (few 100 MHz around 2.45 GHz).

Presti [15] presents a polar architecture based on a 10-bit DPA. This polar modulator features a digital and analog power control, as well as an adaptive pre-distortion with polar feedback. The block diagram is represented on the Figure 2.70.

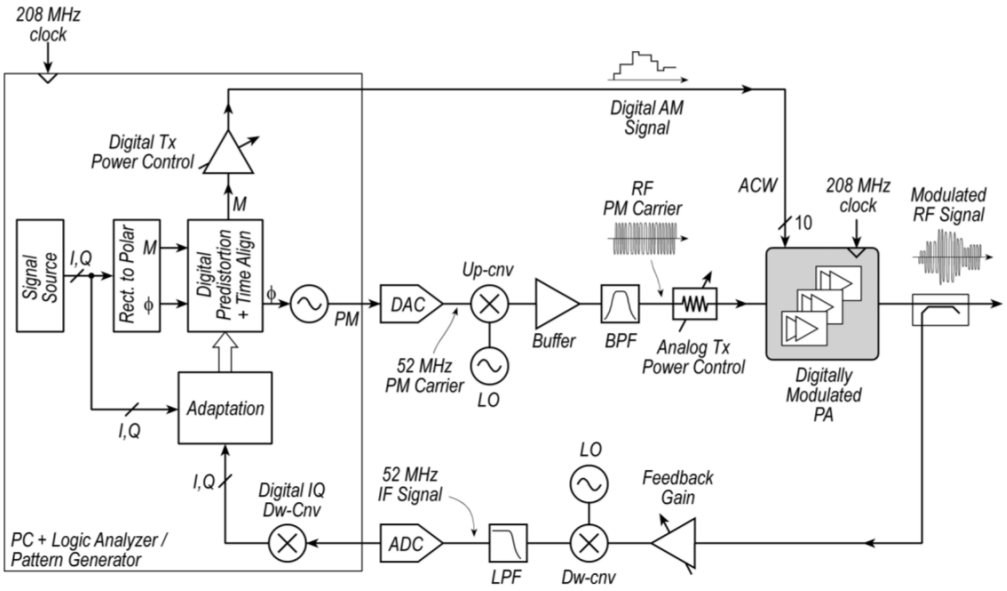


Figure 2.70: *Block Diagram of a Polar modulator with pre-Distortion [15]*

The first power control is performed by tuning the digital gain of the baseband ACW signal, maintaining high PAE with regard of the power level. When no more digital control is available, analog power adjustment can be realized on the RF signal between the phase modulator and the DPA. This will reduce the power of the RF signal driving the DPA and then reduce the efficiency as power back-off does. The DPA in [15] possesses 3 extra bits dedicated to the power control, and to ensure some margin between the quantization noise and ACPR constraints.

The unit PA is implemented with a two-stage amplifier. The unit PA schematic is presented on the Figure 2.71. The DPA efficiency is increased by the output stage set in class-E. R_2 and C_2 soften the switching and then attenuate the digital images. The first stage is a complementary common-emitter amplifier, which is self-biased in order to increase the available bandwidth. Several switches are used to control the cell. M_7 enables the first stage while M_{11} and M_{12} speed up the discharge of C_1. M_9 and M_{10} turn off the

second stage with M_8 forcing the common mode.

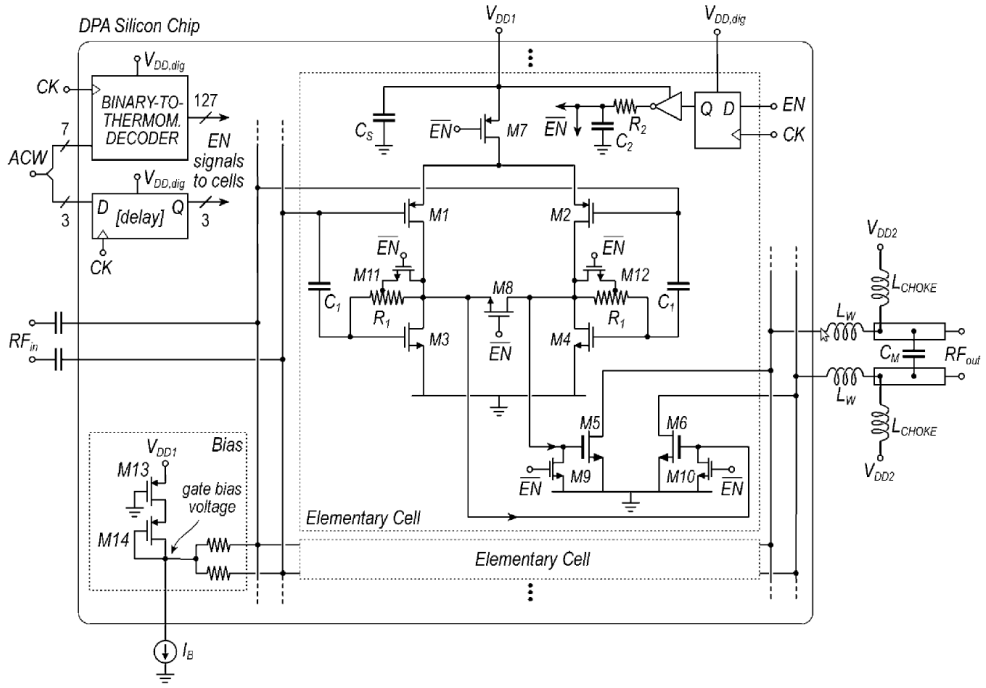


Figure 2.71: *Elementary cell schematic [15]*

The typical problem of DPA is the impedance variation when unit PAs are switched. The input impedance presented by the DPA is set by the input impedances of elementary cells in parallel and can be approximate by $Z_{IN} = (N_{ON} * Y_{ON} + N_{OFF} * Y_{OFF})^{-1}$, in which N_{ON} and N_{OFF} represent the number of cells in ON and OFF state, and Y_{ON} and Y_{OFF} stand for the admittance presented by an elementary cell in ON and OFF states. If Y_{OFF} and Y_{OFF} are the same, the resulting Z_{IN} does not change with ACW. However, any difference between Y_{ON} and Y_{OFF} results in Z_{IN} variation when ACW changes. Therefore, the phase modulator connected to the DPA will not see a constant load impedance. The result is a mismatch between phase modulator and DPA introducing signal distortion. The same effect takes place between the DPA output and load, because of the non-constant optimum load to be presented to the DPA when varying ACW. The implementation proposed by [15] helps to reduce the impedance variation, the input capacitance of the matrix can be approximated as a constant and represented as:

$$C_{IN} = (2^{Nbits} - 1) * (C_{gs_{1,2}} + C_{gs_{3,4}}) \tag{2.19}$$

This first order model supposes no intrinsic channel capacitance variation compared to the total gate capacitance when the first stage is switched. Input impedance model will be discussed in Chapter 4.1.

This overview of [7, 14, 15] show the impact of the implementation of the unit PA on the overall efficiency and impedance distortion. Another aspect is the distortion produced

by the lack of anti-aliasing filters after the digital-to-analog conversion. All the implementations in this section use linear interpolation or oversampling techniques in order to reduce replicas close to the transmit channel. Table 2.2 presents a comparison of different DPA, DRFC and ADPLL of the literature. Except for [15], they all implement coarse interpolation in order to reject images out of their limited bandwidth.

Table 2.2: *DPA and DRFC comparison*

Reference	Process (CMOS)	Power (dBm)	Efficiency (%)	EVM (dB)	Frequency (GHz)	Channel Bandwidth (MHz)	Image Attenuation
[7]	0.18um	13.6	6.7 PAE	-26.8	1.56	20	4x/8x OSR 4-fold interp 40MHz filter
[14]	90nm	-5	2.5 DE	-26.11	2.45	20	
[73]	65nm	17	12.7 PAE	-29.1	1,5	20	4-fold interp
[13]	0.35um	-6.5			1	3.3	16-fold interp
[74]	65nm	24.8	51 DE	-31.37	2	20	4-fold interp
[75]	90nm	-2.5	18 DE	-26.1	2.45	20	2-fold interp
[76]	90nm	10	40	-29,12	1,6		
[15]	0.13um SOI	25.2	40	-36.3	0.8-2	5	
[12]	0.13um	-2		-34	1.9	20	4-IIR, 4-FIR

Where interp stands for interpolation and OSR stands for oversampling ratio.

2.7 Conclusion

The overview of the main aspects of RF transmitters performed in this chapter highlight the difficulty to implement a wide-band and highly reconfigurable transmitter in advance CMOS technology. The bottlenecks are located on the PA-Antenna interface and base-band to RF conversion. The state of the art does not present any wide-band transmitter able to support multiple standards. Only [15] presents an all-digital transmitter covering a wide band, but does not focus on images problem. The other digital transmitters require selective passive filtering between the power stage and antenna in order to avoid spurious emission due to the direct baseband to RF conversion. Thus, a raw oversampling is performed with linear interpolation to translate the images out of the system bandwidth. This approach limits the reconfigurability of the transmitter and its use in SDR.
As explain in this chapter, wideband matching network and power recombination can be implemented in advanced low power CMOS processes. The next chapter will detail the drawback of wideband all-digital transmitters without anti-aliasing filters, then a new architecture will be introduced as suitable approach to SDR.

Chapter 3

Proposed multi-rate digital transmitter

3.1 Introduction

As seen in the previous sections, increasing the digital processing part of a transmitter cannot perfectly replace analog functions. Of course, a cognitive radio would take advantage of advanced technologies to offer the integration of digital baseband processing and digital transmitter on the same die. Nevertheless, their usage on the market is slowed down due to the low output power and the limited quality factor of integrated passive components. As explained before, the multi-path approach helps to overcome the power limitation and impedance matching, while a digital power amplifier leverages high digital density to perform various baseband processing such as pre-distortion.

This chapter will first detail the spurious emissions in all-digital transmitters and attenuation techniques needed to enable wideband digital transmitters. Then, the frequency hopping technique will be explained. Ultimately, the proposed architecture based on a multi-rate approach, will be introduced in order to overcome power limitation and spurious emissions in all-digital transmitter.

3.2 Spurious emission issue in all-digital transmitter

All-digital transmitters based on DPA or DRFC extend the digital processing up to the power stage. Nevertheless, the spectral spurious introduced by digital to analog conversion are not filtered anymore by anti-aliasing filters. This aspect is depicted on Figure 3.1, where spurious emissions are represented for a standard RF modulator and direct digital to RF modulator. The DAC component is supposed ideal without bandwidth limitation.

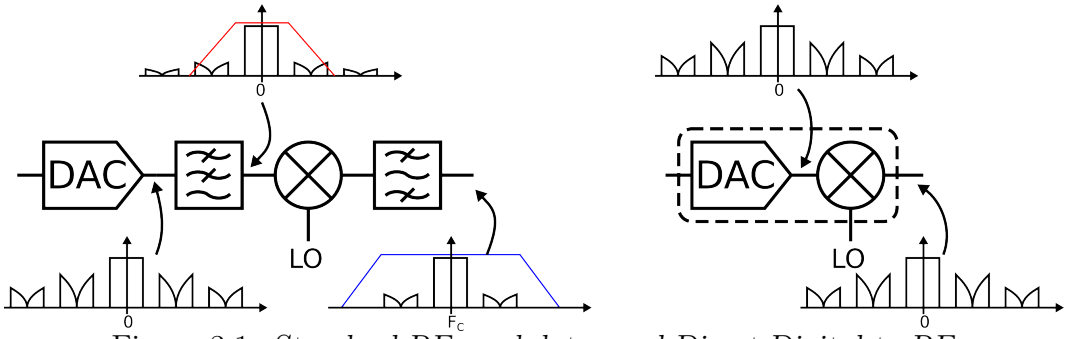


Figure 3.1: *Standard RF modulator and Direct Digital to RF*

As described in the previous chapter, the DPA and DRFC implementations overcome this problem by attenuating the first images. The oversampling is performed by linear interpolation in RF [7, 14], digital filters in baseband [72] or directly during the conversion [13]. Table 3.1 summarizes the characteristics of published digital transmitters.

Table 3.1: *Image filtering in all-digital transmitters*

Ref		Type	Domain	OSR	Baseband Sampling Rate
[13]	DRFC	16-fold linear	RF/Baseband	16x	50MHz
[14]	DPA	4-fold linear	RF	4x	100MHz
[73]	DPA	4-fold linear	RF	4x	240MHz
[74]	DPA	4-fold linear	RF	4x	300MHz
[77]	DPA	2-fold linear	RF	2x	40MHz
[7]	DPA	4-fold linear	RF	4x	80MHz/160MHz
[72]	DRFC	IIR-FIR	Baseband Digital	8x	307,2MHz

Linear interpolation is a good method in case of narrow band systems with RF filters where only the first images must be attenuated. As an example, for 3.84 MHz W-CDMA channels in 1710 MHz - 1980 MHz band (Band I to Band IV UMTS-FDD), a 60x oversampling ratio is needed to avoid any images over a 270 MHz offset.

However in the case of wide-band cognitive radio, the transmitter must cover several

channels, i.e. from 824 MHz ("Dividende Numérique", LTE Band V) to 2570 MHz (LTE Band VII). Rejecting the images out of this large band requires an extremely high over-sampling ratio, and thus an extremely high speed clock, with a non negligible impact on power consumption. Figure 3.2 shows a wideband spectrum of an all-digital transmitter when transmitting a 10 MHz LTE symbol with 25 dBm power. The sampling rate is set to 245.76 MS/s. Both all-digital Cartesian (red) and polar (blue) implementations are represented. The overall spectral emission mask defined in the LTE standard [2] is also indicated. The simulation was performed with complex models and signals (baseband model of RF system). Then, the spectrum was obtained by translating the baseband spectrum around the carrier. The windowing used in the FFT is responsible for the spreading of the fundamental.

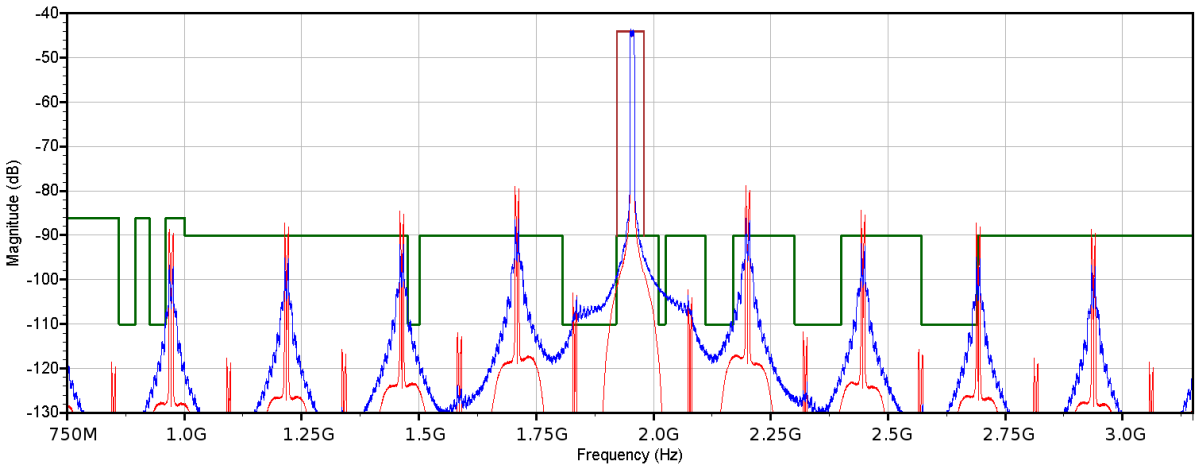


Figure 3.2: *Emission mask violation in wideband all digital transmitter*

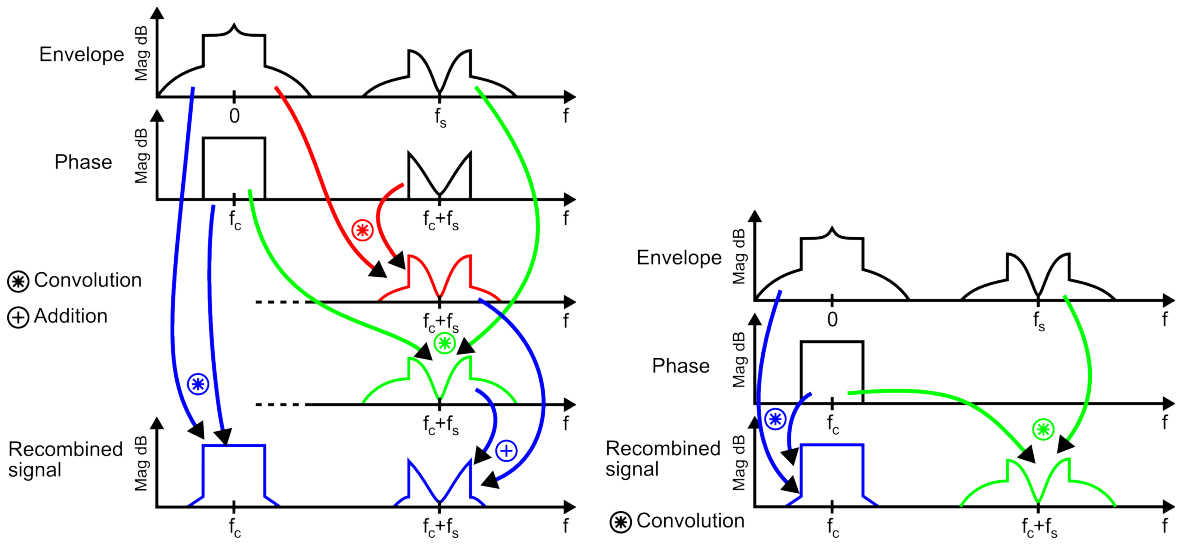
In both cases, the images violate the emission mask on several points. The images on the polar spectrum are spread and attenuated due to a phase filtering performed before the DPA. This atypical shape results from the recombination of the envelope images and the fundamental of the phase signal. This effect was studied and presented on NEWCAS 2011 [78] and will be detailed in the next section. The violation of the wideband emission mask limits the use of all-digital transmitter in SDR. The next point will detail image attenuation techniques, that avoid integrating complex passive filters.

3.3 Spurious emission attenuation techniques

Avoiding spurious emissions is challenging in wideband RF system design. This section will describe two approaches to attenuate spurious without the need of passive filters. First, the images attenuation due to the phase filtering performed in polar transmitters will be covered in the next point. Second, the baseband oversampling shifting these images out of the covered band will be explained.

3.3.1 Image spreading in polar transmitters

Contrary to the IQ modulator, the polar transmitter separates the baseband signal into two components (envelope and phase signals) with different information. Moreover, different processing can be performed on the envelope and phase signals. The processing on either envelope or phase signals can greatly impact the spectrum of the reconstructed output signal. Figure 3.3.a) illustrates the recombination process in all-digital polar architecture, the sharp image of the recombined signal spectrum results from the summation (+) of two spectral convolutions. The first one (*) involves the convolution of the envelope fundamental with the phase images while the second (*) convolutes the phase fundamental with the envelope images. Spreading is present around the resulting partial images, but disappears after the recombination. The same process occurs to the fundamental which mainly results from the convolution (*) between the envelope and phase fundamentals, the other convolution products located around the fundamental can be ignored.



a) all-digital with the same sample rate b) filtered phase

Figure 3.3: *Spectral recombination process in polar transmitters*

Figure 3.3.b) represents the recombination process when the phase images are filtered. Contrary to the previous case, the final image only results from one convolution (*) of the phase fundamental with amplitude image. This image is then spread and attenuated. A Matlab simulation of 1-rate all-digital polar transmitter with and without phase filtering is shown on Figure 3.4. The images of the polar approach with phase filtering are clearly spread and attenuated while the fundamental is unchanged.

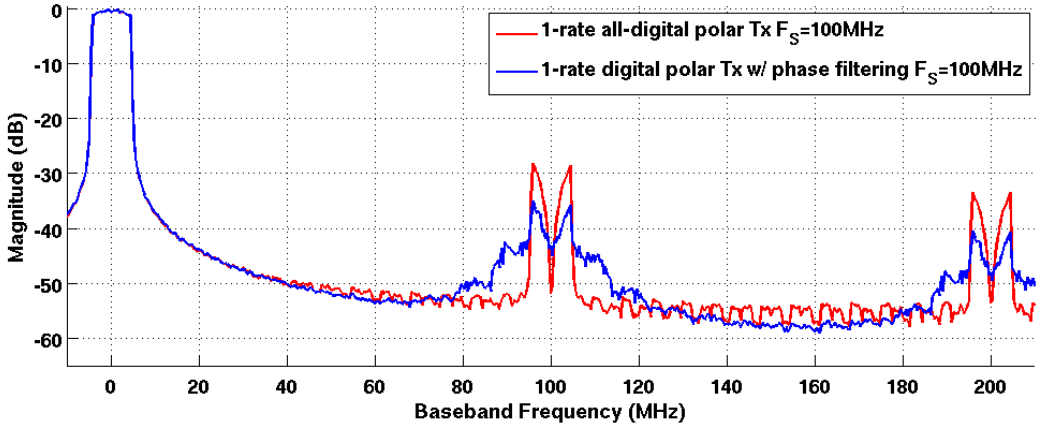


Figure 3.4: *All-digital Polar transmitter simulation with phase filtering*

An interesting configuration appears when the phase and amplitude signals are sampled at different sampling rates. The spectrum of the reconstructed output signal is shown in Figure 3.5 Contrary to Figure 3.3.a), the two convolutions (* and *) are not located at the same frequency. Then, instead of one sharp image the recombined signal spectrum has two spread images at lower levels. This aspect could be useful to reduce spurious emission but attention must be paid to avoid overlapping of images and fundamental, what could degrade the ACPR.

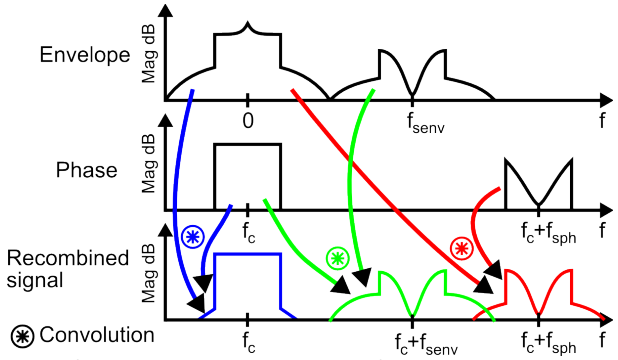


Figure 3.5: *Spectral recombination process in polar transmitters with two different sampling rates*

In polar architectures, the image amplitudes depend on the distribution of the information between the phase and the envelope as explained in the first section. Table 3.2 lists a few standards together with the attenuation of the first image when the amplitude signal or the phase signal is lowpass filtered. It appears that phase filtering offers the highest attenuation of the images and can be roughly approximated to 7 dB.

Table 3.2: *Images attenuation when only one part of the signal is filtered*

Standard (Channel Bw)	Amplitude filtered	Phase filtered
EDGE (200KHz)	3.26 dB	7.2 dB
UMTS-TDD (5MHz)	3.75 dB	7.2 dB
W-CDMA (5MHz)	3.54 dB	6.34 dB
LTE (10MHz)	3.4 dB	6.86 dB
WMAN 802.16 (20MHz)	3.4 dB	8.2 dB

The next point will describe the proposed architecture able to perform wide-band filtering with low clock frequency and implementable in a multi-path transmitter.

3.3.2 Baseband oversampling

Narrow-band systems can easily deal with spurious emissions by translating the images out of the band. Figure 3.6 presents a typical spectrum with the fundamental, the first images and the *sinc* transfer function of an ideal DAC. Equation (3.1) defines the attenuation of the images as a function of the signal bandwidth (Bw), the sampling frequency (F_S) and the index of the image (N). $N = 0$ stands for the fundamental while N>1 stands for the N^{th} image centered at $N * F_S$.

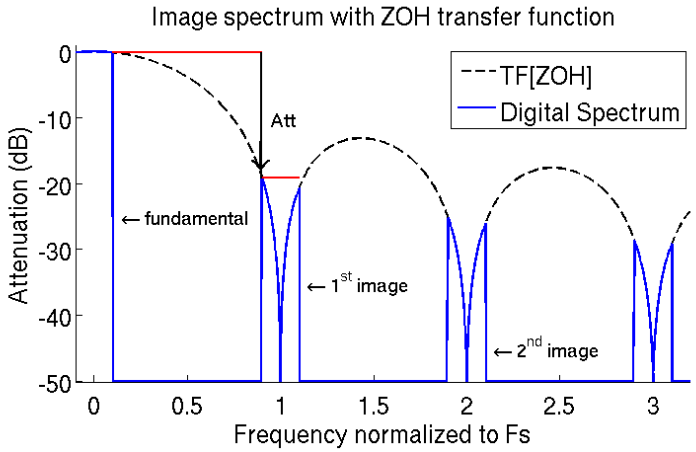


Figure 3.6: *Images attenuation from ZOH transfer function*

$$Att(dB) = 20 * \log_{10}\left(\frac{sinc\left(\frac{Bw}{2}\right)}{sinc\left(N * F_S - \frac{Bw}{2}\right)}\right) \tag{3.1}$$

Increasing the Over Sampling Ratio (OSR) shifts the images and also increases the attenuation. This last effect is depicted on Figure 3.7, where the attenuation of the first 6 images is plotted versus the OSR.

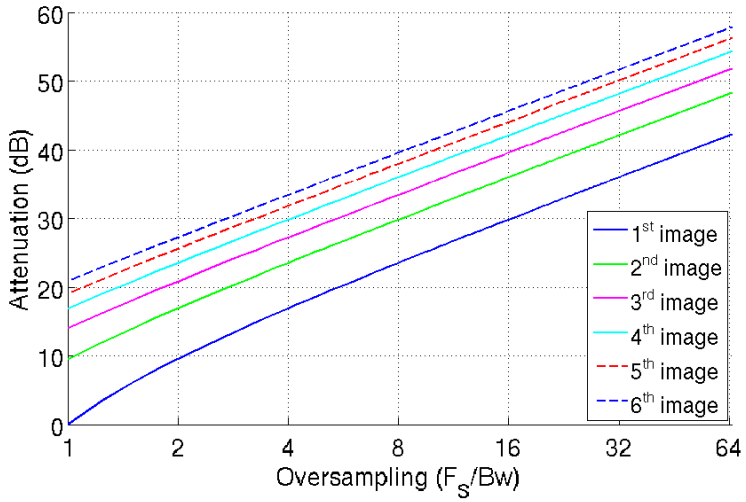


Figure 3.7: *Images attenuation related to Oversampling Ratio*

Each 2x increase of the OSR results in approximately 6 dB images attenuation improvement. In order to illustrate this effect, the efficiency of the OSR will be studied. First, the attenuation efficiency must be defined. Equation (3.2) presents the efficiency as the ratio of the attenuation of the first image, Att_1 to the power consumed by the clock driver of the converter P_{clk}.

$$\eta = \frac{Att_1}{P_{clk}} \tag{3.2}$$

In the case of CMOS process and if the load capacitance C is supposed non negligible, the static, leakage and switching losses can be ignored. Then, P_{clk} is defined as:

$$P_{clk} = C * V_{CC}^2 * F \tag{3.3}$$

with:

$$F = OSR * F_{sig} \tag{3.4}$$

(3.2) can be rewritten:

$$\eta = \frac{Att_1}{OSR} \tag{3.5}$$

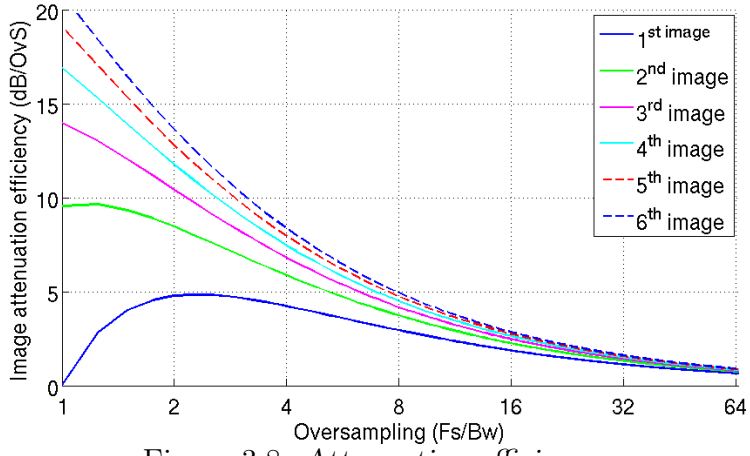


Figure 3.8: *Attenuation efficiency*

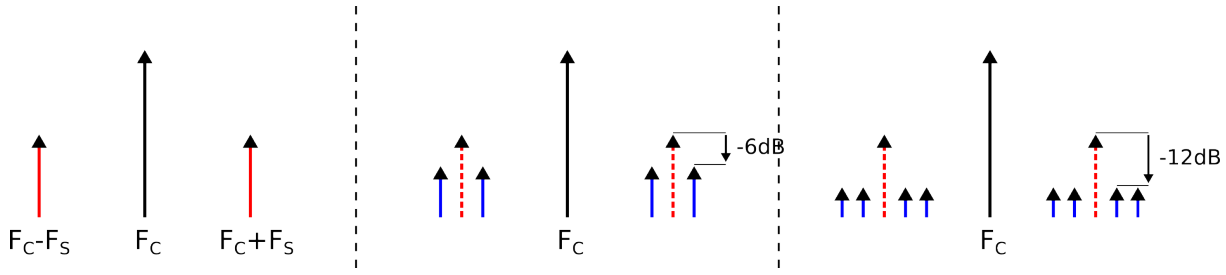
Figure 3.8 represents the efficiency versus the OSR. As remarked before, when increasing the OSR, its impact on images attenuation decreases. Using several relatively low sample rates instead of one high sample rate would offer a better efficiency in attenuating images. Baseband oversampling supposes a sample rate conversion which could be implemented on one path transmitter. However, the high speed clock required by this approach presents two main drawbacks. First, it requires high power which could greatly impact the overall efficiency of the transmitter. Second, the clock distribution in direct digital to RF converters (DPA and DRFC) is a challenging task. In order to overcome these limitations, the next section will present a new approach taking advantage of multi-path and low speed baseband processing.

3.4 Proposed multi-rate approach

This section will introduce frequency hopping and its implementation in multi-path architecture. The impact of power combining and clock efficiency will also be detailed. The last point will describe the simulated transmitter and simulation results under different configurations of the paths.

3.4.1 Frequency Hopping

Chen [37] presents a power amplifier with a switched-mode DC-DC converter as power supply. The main problem of switched-modeDC-DC converters is the spurs generated by the switching frequency when mixed with the RF signal. The leakage of this switching frequency can be attenuated by filtering but this requires large passives components. In order to avoid an increase in area, Chen proposed to attenuate the spurs by varying the switching frequency, thus introducing several small spurs instead of a large one. This method is called frequency-hopping and is illustrated in Figure 3.9, where the spectrum without and with frequency hopping are represented. Figure 3.10 represents the time waveform example with four sampling frequencies.



No Frequency Hopping 2-rate Frequency Hopping 4-rate Frequency Hopping

Figure 3.9: *Frequency Hopping principle*

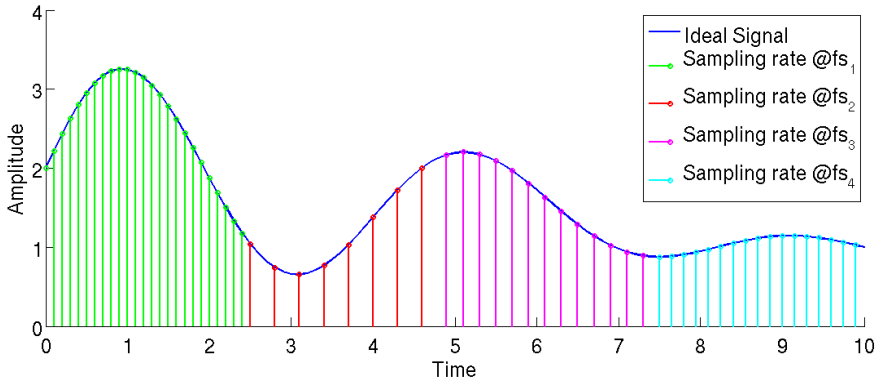


Figure 3.10: *Waveform example for a 4-rate Frequency Hopping*

Chen [37] proposed to tune the switching frequency dynamically. This method is simple and efficient when applied to basic signals with slow variations. But several problems appear when working with more complex signals.

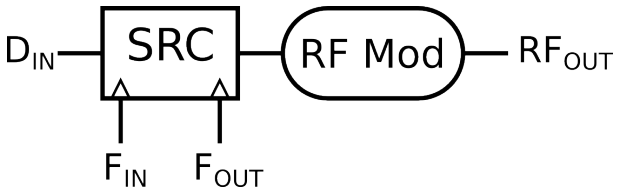


Figure 3.11: *Serial Frequency Hopping block diagram*

Figure 3.11 represents the simplified block diagram of a RF modulator with frequency-hopping applied to the baseband signal. The sampling rate is varied thanks to a sample rate converter (SRC). The two main limitations of the frequency-hopping technique are the following.

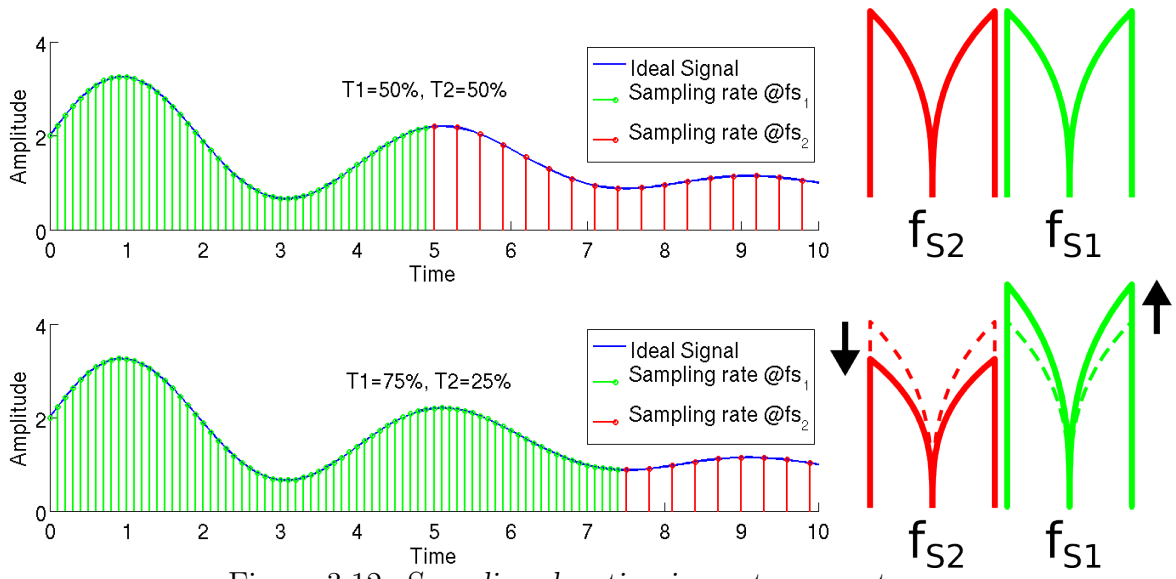


Figure 3.12: *Sampling duration impact on spectrum*

First, the images amplitudes depend on the duration of the signal sampled at a specific rate. If the pieces of signal with different sample rates do not have the same length, then the image amplitudes are not identical. This effect is illustrated in Figure 3.12. The first case represents the ideal case while the second case shows unmatched sampling duration $T1$ and $T2$. The ideal case with $T1 = T2$ produces two images with half power. If $T1$ and $T2$ are different, this generates two images with different power levels, which degrades the images attenuation of the frequency-hopping technique.

The second limitation is the need to dynamically change the sampling frequency. If the frequency switching is performed during a symbol, any glitch will generate spurious emission. Traditionally, the SRC is based on a FIR with re-programmable coefficients as shown in Figure 3.13.

Figure 3.13: *SRC block diagram*

When changing the Fin to Fout ratio, the transfer function needs to be updated while the filter memory needs to be re-filled. If the filter memory is not re-filled, then the latency between the last valid sample with the previous ratio and the first valid sample with the new ratio introduces signal distortions. This effect is depicted in Figure 3.14 and introduces spurious emissions.

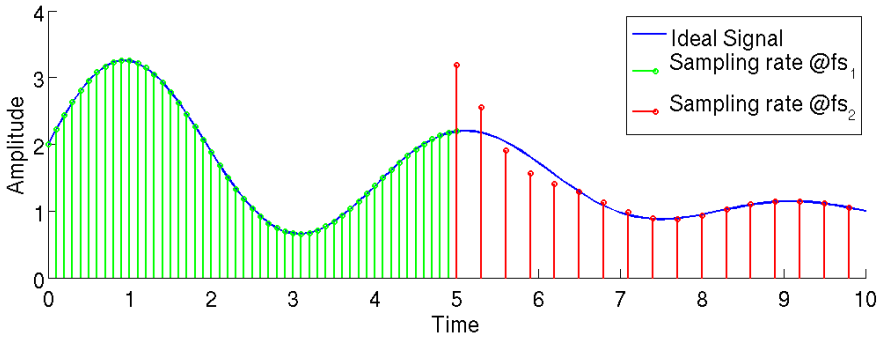


Figure 3.14: *Sample rate transition.*

Serial frequency hopping suffers from complex ratio switching as well as unequal images magnitude and extra spurious emissions. The next point will present the proposed architecture taking advantage of the inherent multi-path approach of the digital power amplifiers.

3.4.2 Multi-rate approach applied to multi-path architecture

In this context, a different approach is proposed. The idea is to perform the same image attenuation with a more robust parallel sample rate conversion instead of serial (cyclic). The block diagram of the proposed architecture is presented on Figure 3.15, this solution can easily be implemented in multi-path transmitters with power recombination. A SRC and RF modulator are embedded on each path. The resulting spectra on the nodes A to D are illustrated in Figure 3.16.

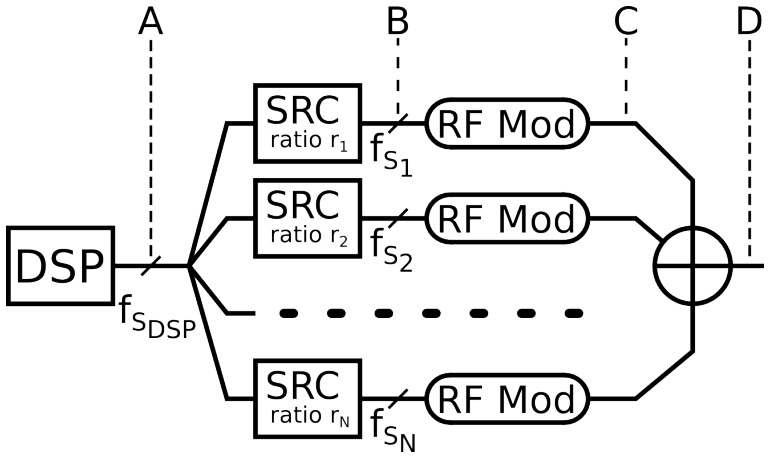


Figure 3.15: *N-path, N-rate proposed architecture*

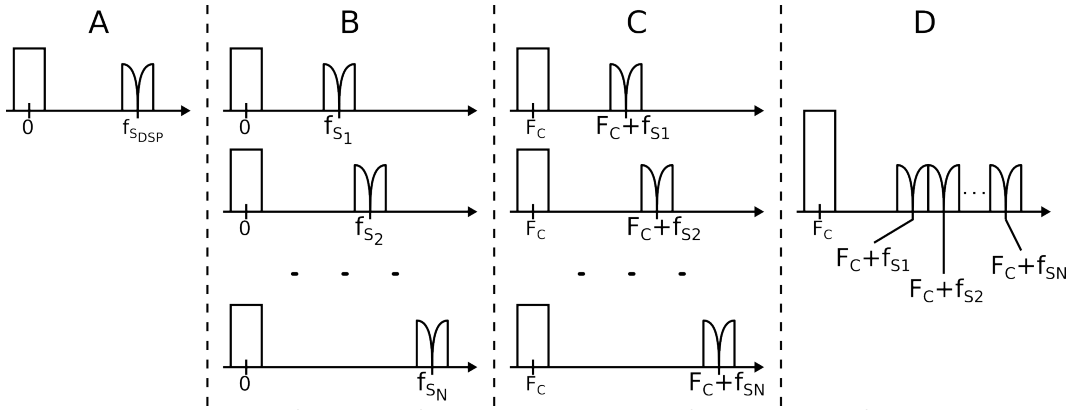


Figure 3.16: *Theoretical spectrum in N-path, N-rate architecture*

Each SRC shifts the image from a multiple of F_{in} to a multiple of F_i. Then the RF modulator translates the baseband spectrum around the carrier frequency F_c. Finally, the power combiner sums the signals. The fundamentals, located around F_c, recombine together, resulting in an amplified fundamental after the power combiner. On the contrary, the images do not fall on the same subcarrier frequencies for each path and do not recombine. The result is an increased fundamental to image ratio. A simple example with two paths is represented on Figure 3.17 where the frequencies are normalized to the signal bandwidth.

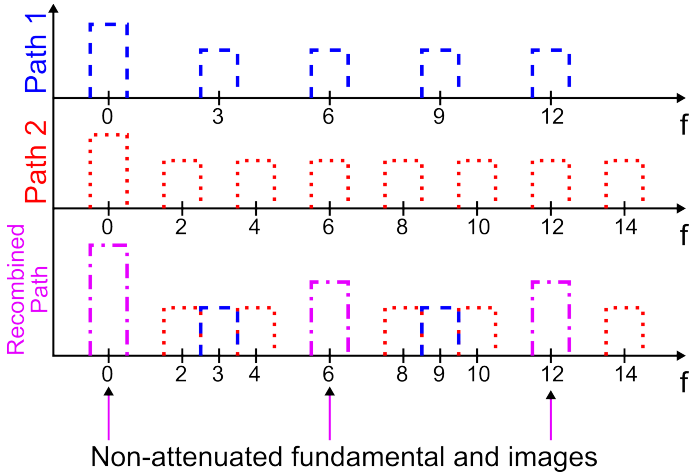
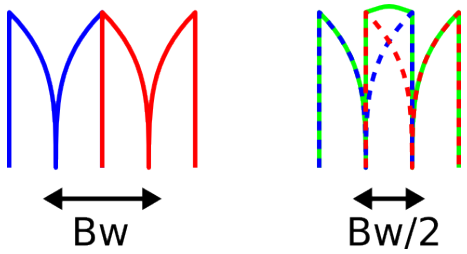


Figure 3.17: *2-path spectrum example*

The fundamentals are recombined and most of the images are unchanged. Nevertheless, some images from two separate paths can be located at the same frequencies (i.e. 6th and 12th) and recombine. This is due to common multiple relation between the Nth image on path 1 and K^{th} image on path 2 with $N * F_{S1} = K * F_{S2}$. The first non-attenuated image can be shifted far away from the fundamental by appropriately setting F_{S1} and F_{S2}, and can theoretically be shifted to infinity if F_{S1} and F_{S2} are in prime relation.

In order to avoid any partial overlapping, the images must be separated by at least the signal bandwidth as represented in Figure 3.18.a). A special case is also represented in Figure 3.18.b), with half the bandwidth spacing and no recombination. The half overlapping of images increases the number of sample rates to be used without degradation of the images attenuation, which improves the system flexibility.



a) no overlap b) overlap

Figure 3.18: *Images overlapping*

The multi-frequency approach offers good attenuation in terms of absolute images attenuation and attenuation efficiency. Besides the power aspect, the multi-frequency approach also facilitates the clock distribution and increases the efficiency depending on the number of paths. The image attenuation depends on the number of possible frequencies relation (3.6) and is represented in Figure 3.19. It is to note that (3.6) does not exactly model the image attenuation, because the power combiner behavior is not taken into account.

$$Att(dB) = 10 * \log_{10}(N) \tag{3.6}$$

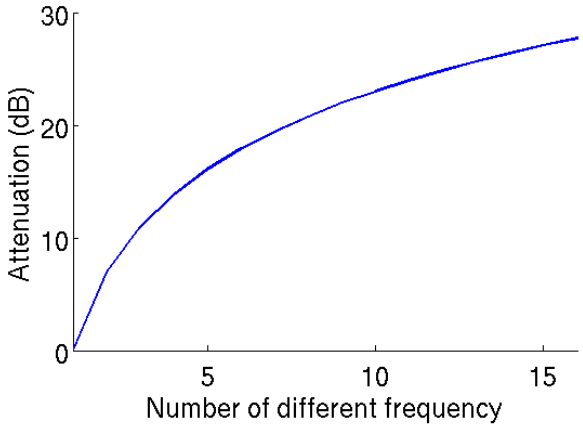
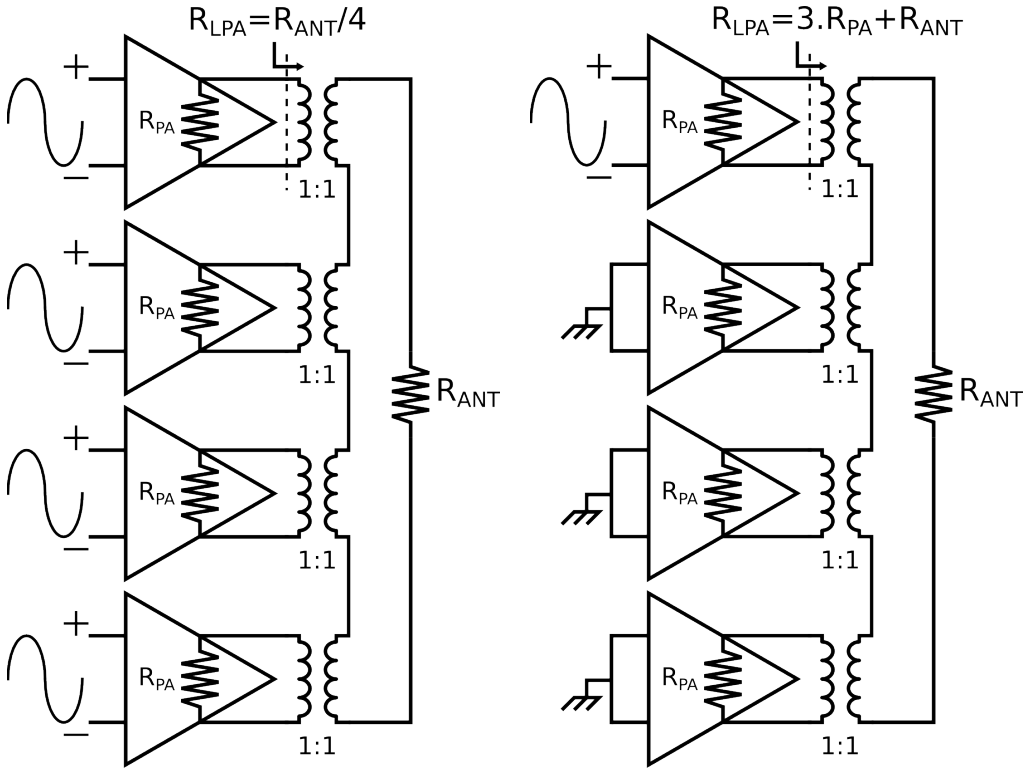


Figure 3.19: *Image attenuation vs number of frequencies*

3.4.3 Images attenuation in power combiner

The power combiner presents the ideal load impedance to each DPA when all of them generate the same signal as represented on Figure 3.20.a) for the case of a transformer-based combiner. The load impedance is then equally divided among the DPAs allowing all DPAs to deliver their maximum power to the load.



a) 4 DPAs ON b) 1 DPA ON

Figure 3.20: *4-path power combiner architecture*

But if only one path is active (i.e. provides spectral information at a defined frequency) then the DPA does not see the optimum load as represented on Figure 3.20.b). This mismatch results in lower power generated by the DPA, which is divided between the load and the other DPA output impedances. The resulting power delivered to the load represented by R_{ANT} is defined by (3.7).

$$P_{ANT} = P_{PA\ opt} * \left(1 - \frac{N_{ON}}{2N_{Path}}\right) * \frac{N_{ON}^2}{2N_{Path} - N_{ON}} = P_{PAopt} * \frac{N_{ON}^2}{2N_{Path}} \qquad (3.7)$$

where N_{ON} represents the number of "ON" paths (i.e. images at the same frequency), N_{Path} is the total number of paths and $P_{PA\ opt}$ is the optimum power delivered by one PA when charged with ideal load equal to Z_{PA}^*. The total attenuation defined as the ratio between the power delivered to the antenna and the optimum power delivered when all

paths are ON, can be written as:

$$Att = \frac{P_{ANT}}{P_{ANT\ opt}} = \frac{N_{ON}^2}{N_{OFF}^2} \tag{3.8}$$

The impedance presented at most of the image frequencies by the power combiner to the DPAs is therefore different from the optimum load impedance and contributes to the image attenuation. The extra attenuation thanks to the power combiner depends on the total number of paths and the number of path providing a signal at the same frequency. Table 3.3 lists the total attenuation of the images compared to a 1-path implementation. The effect of image splitting and impedance mismatch are taken into consideration, beside the total number of paths (N) and the number of "ON" paths (K, with an image at the same frequency).

Table 3.3: *Total image attenuation (in dB)*

N/K	1	2	3	4	5	6	7	8
1	0							
2	-6.02	0						
3	-9.54	-3.52	0					
4	-12.04	-6.02	-2.5	0				
5	-13.98	-7.96	-4.44	-1.94	0			
6	-15.56	-9.54	-6.02	-3.52	-1.58	0		
7	-16.9	-10.88	-7.36	-4.86	-2.92	-1.34	0	
8	-18.06	-12.04	-8.52	-6.02	-4.08	-2.5	-1.16	0

In conclusion, the multi-rate approach offers better image attenuation than first predicted when only taking into account the image placement. The next point will explain another advantage compared to a raw oversampling method.

3.4.4 Impact of the multi-rate approach on clock efficiency

The multi-frequency approach requires low frequencies compared to systems with a single sampling rate. The attenuation efficiency, as defined by (3.5) in section 3.3.2, will now be compared for both approaches. A two-path digital polar architecture is represented on Figure 3.21. The DPAs present a $C/2$ input capacitance at the amplitude input. Figure 3.22 shows the simplified spectrum with frequencies normalized to the signal bandwidth. An arbitrary maximum spurious constraint is also represented. With an OSR of 10, the

spurs violate the constraint while an OSR of 14 meets the 28 dB ACPR constraint. Figure 3.23 represents the images attenuation related to the oversampling ratio.

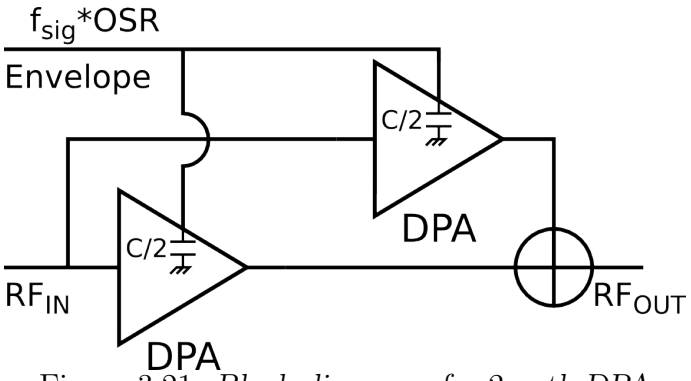


Figure 3.21: *Block diagram of a 2-path DPA*

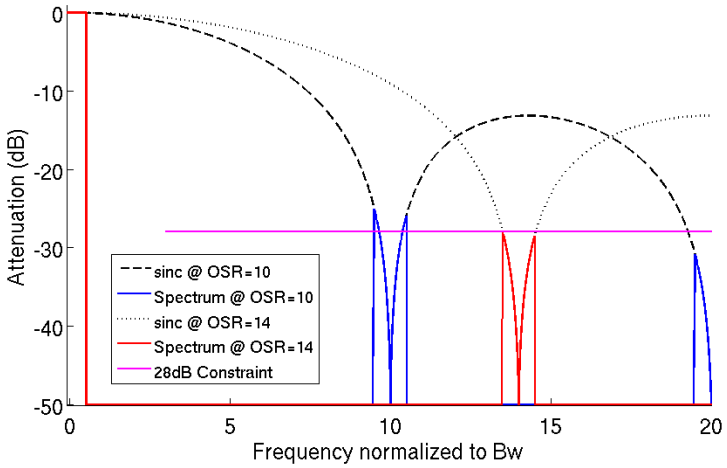


Figure 3.22: *Spectrum of a 2-path DPA with single sample rate*

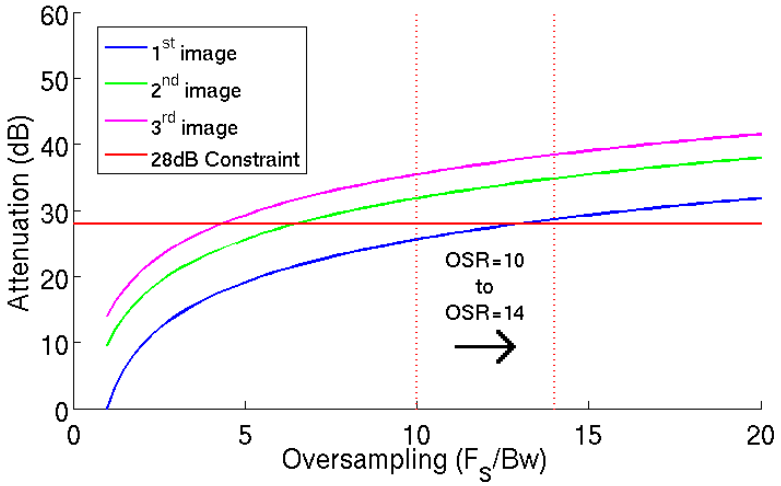


Figure 3.23: *Image attenuation vs OSR*

The power required by the clock can be written as:

$$P_{clk} = 2 * \frac{C}{2} * V_{CC}^2 * F = 2 * \frac{C}{2} * V_{CC}^2 * Bw * OSR = P_{clk\ sig} * OSR \qquad (3.9)$$

With $P_{clk\ sig}$ the power required by the clock signal without oversampling. In these cases: $P_{clk}(OSR = 10) = 10 * P_{clk\ sig}$ with $Att_1(OSR = 10) = 25.6dB$ and $\eta(OSR = 10) = 2.56$

$P_{clk}(OSR = 14) = 14 * P_{clk\ sig}$ with $Att_1(OSR = 14) = 28.6dB$ and $\eta(OSR = 14) = 2.04$ With η the clock power efficiency to attenuate the images. It appears that the image attenuation efficiency degrades from 2.56 to 2.04, which means that increasing the clock sampling does not significantly improve the image attenuation.

In the case of a multi-frequency architecture, the block diagram becomes:

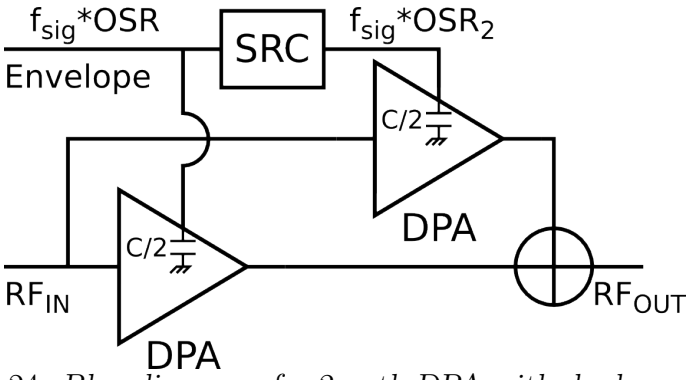


Figure 3.24: *Bloc diagram of a 2-path DPA with dual sample rates*

The resulting spectrum is presented on Figure 3.25, where the OSR of the second path is set to 11.

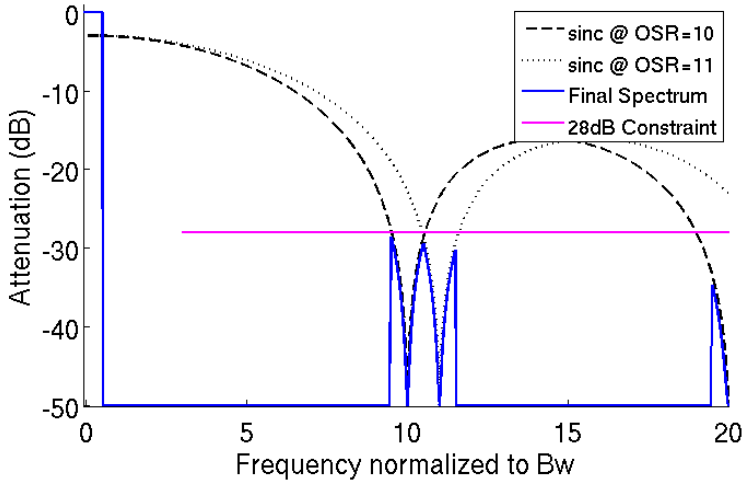


Figure 3.25: *Spectrum: 2-path DPA with different sample rate*

The clock power and efficiency become:

$$P_{clk} = \frac{10 * P_{clksig}}{2} + \frac{11 * P_{clksig}}{2} = 10.5 * P_{clksig} \tag{3.10}$$

$$\eta = \frac{28.6}{10.5} = 2.72 \tag{3.11}$$

The multi-rate approach offers an attenuation efficiency of 2.72 compared to 2.04 for a single frequency system. Although the model for the power consumption is coarse, it appears that the power efficiency improvement due to the multi-rate approach can compensate the power needed to perform the parallel baseband sample rate conversion. As

seen in this section, the proposed architecture offers several advantages compared to basic approaches like oversampling or frequency-hopping.

First, the architecture takes advantage of the multi-path implementation which helps to achieve enough power in advanced low power CMOS process. No RF functions are needed, only baseband processing must be implemented before the RF modulator. Besides, the approach can be implemented in polar or Cartesian architectures. Then, the low frequencies required in baseband ease the implementation by relaxing constraints on the clock distribution. Contrary to the frequency-hopping approach, the multi-path system does not necessitate dynamic reconfiguration. This avoids glitches and amplitude mismatches, both degrading the system efficiency. If needed, the images of each path can be adjusted in frequency and amplitude by tuning the SRC ratio and digital gain directly in the SRC or before the DPA.

3.5 Simulation results of a multi-rate polar transmitter

After this theoretical explanation of the proposed architecture, a more practical model will be presented to confirm the developed concepts. Figure 3.26 shows the model of the simulated system. The system is based on a polar architecture. In order to alleviate the simulation effort, baseband equivalent models are used. The Cartesian baseband signal is generated by the DSP at a sample rate f_{BB}, and is converted in polar form by a CORDIC algorithm. The phase signal is filtered and modulates the carrier while the phase modulator output drives all the DPAs. The multi-frequency aspect is implemented on the amplitude path. The amplitude signal is separated into two paths. The sample rate of each path is converted by SRCs to f_{BB1} and f_{BB2}. The sample rate conversions are performed by the coarse interpolation presented before in Figure 3.13. Each converted amplitude signal drives one DPA. The DPA outputs are then recombined by an ideal voltage combiner.

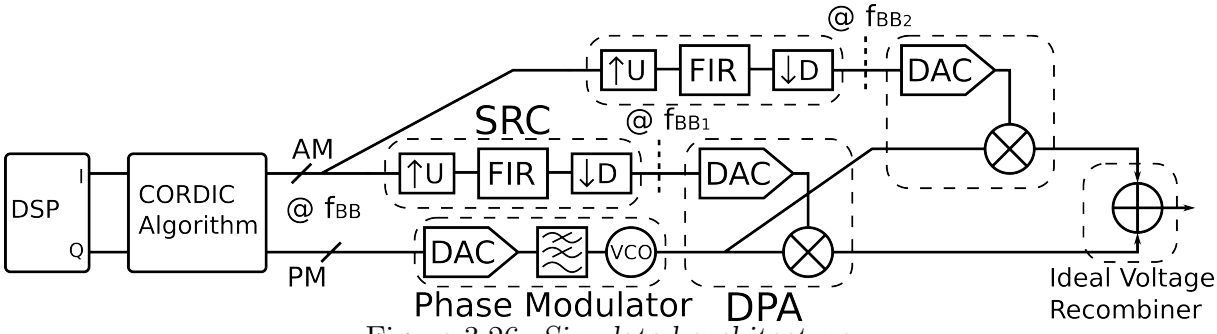


Figure 3.26: *Simulated architecture*

Figure 3.27 presents the wide-band spectrum at the combiner output. The transmitted signal is based on the LTE standard. The power is set to 25 dBm, the bandwidth to 10MHz and the carrier to 1955 MHz (Band 1). The signal generated by the DSP is oversampled with a 16x ratio. The ratio of the SRC on the path 1 is set to 1, and on the path 2 is set to 1.2. The red curve represents the spectrum for a single-path all-digital Cartesian transmitter. The blue plot represents the spectrum for a single-path digital polar architecture. The green curve stands for the emission mask defined by the LTE standard. Finally, the magenta plot represents the spectrum of the simulated architecture. The amplitudes of fundamental are the same in all cases. The images were placed in bands with lower constraints. As explained in the first part of this section, polar systems with phase filtering produce lower images and spectral regrowth. Figure 3.28 shows the first image of the 1-rate all-digital Cartesian transmitter and 1-rate digital

polar architecture. The attenuation and spreading around the images are clearly visible in the polar approach compared to Cartesian. In the case of LTE modulation, the signal information is equally split between the phase and envelope signals, resulting in about 6 dB attenuation of the image when the phase is filtered.

The complex model directly shifts the FFT result around the carrier. Windowing is applied to the signal prior to FFT. For this reason, we observe a spreading around the carrier. The spreading of the fundamental can be ignored as it is an artefact introduced by windowing.

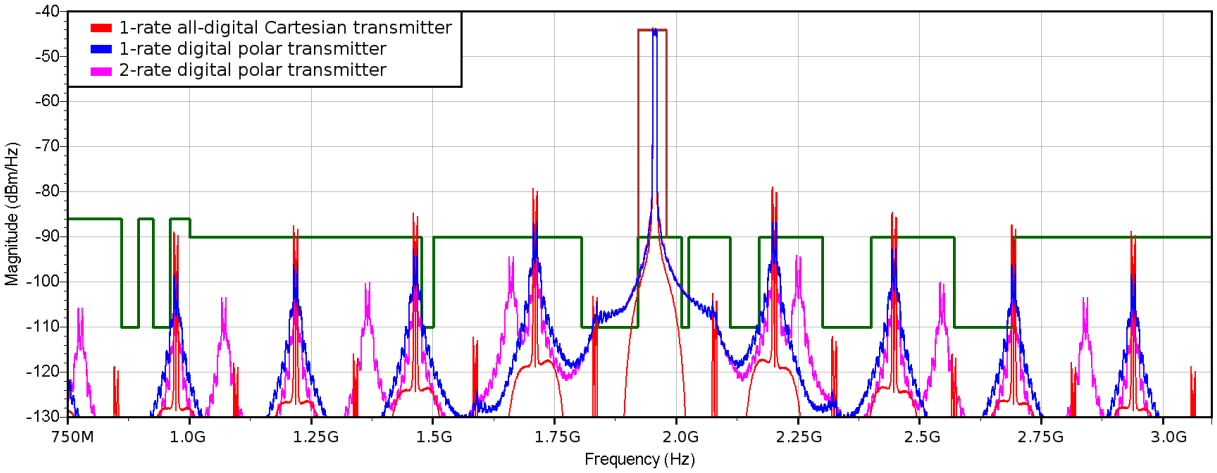


Figure 3.27: *2-rate DPA spectrum with 1955 MHz frequency carrier*

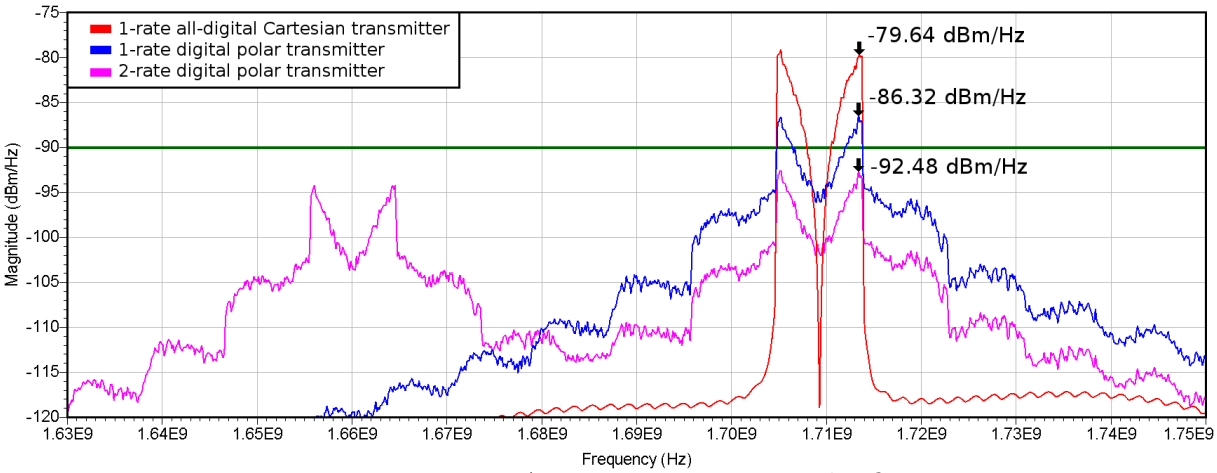


Figure 3.28: *2-rate DPA spectrum zoom on the first image*

Figure 3.29 shows the same approach extended to 4 paths. The sample rate converter ratios are: 1; 1.16; 1.16; 1.25.

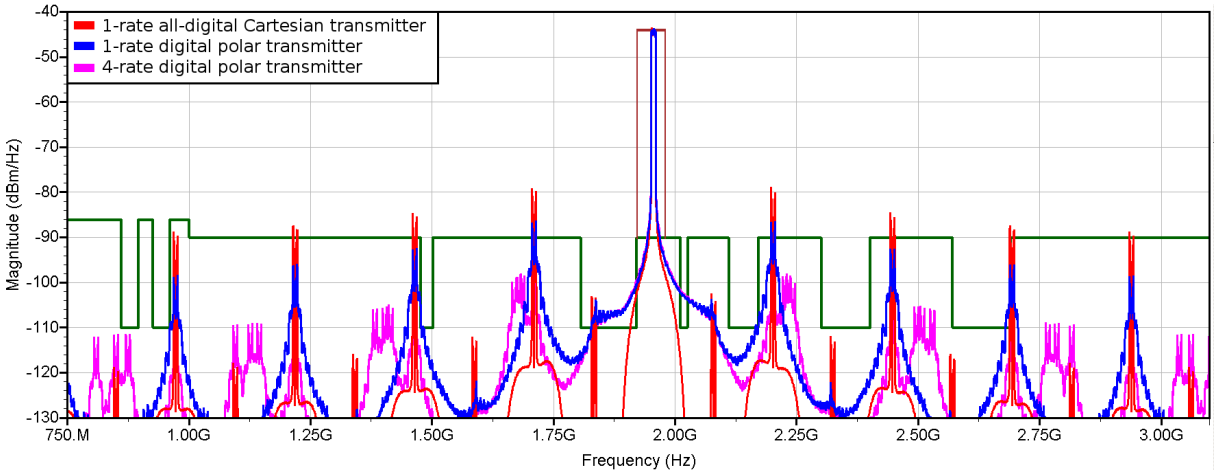


Figure 3.29: *4-rate DPA spectrum with 1955 MHz frequency carrier*

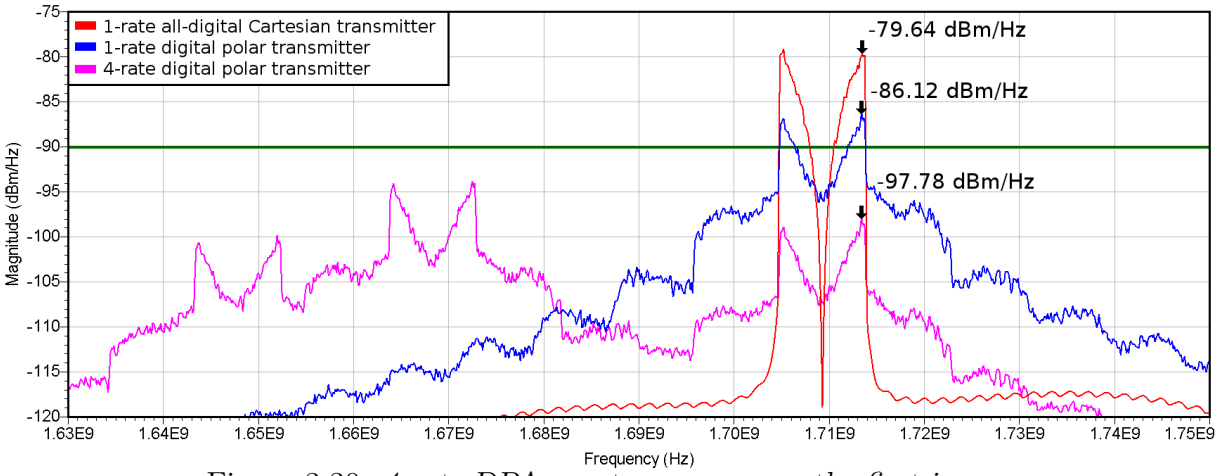


Figure 3.30: *4-rate DPA spectrum zoom on the first image*

Figure 3.28 shows a zoom on the first images in the case of a 2-rate digital polar implementation. The first image of the 2-rate digital polar transmitter is 6.16 dB lower than the 1-rate digital polar transmitter. This attenuation results from the separation of the images and the impedance mismatch introduced by the power combiner. As predicted by the theory, the use of two rates involves 3 dB attenuation while impedance mismatch increases this value by an extra 3 dB. Similarly, Figure 3.30 shows a zoom on the first images in the case of a 4-rate digital polar implementation. The first images of the 4-rate digital polar transmitter corresponding to the ratios 1 and 1.25 are 11.66 dB lowers than the 1-rate digital polar transmitter. In the same way as for the 2-rate implementation, this attenuation results from the separation of the images and the impedance mismatch introduced by the power combiner. As predicted by the theory, the use of four rates involves 6 dB of attenuation while impedance mismatch increases this value by about 6 dB. The interesting point of this configuration is the image close to 1.67 GHz, which results from the combination of the images from the two paths with the sample rate conversion

ratio of 1.16. In this case the general behavior of the 4-rate transmitter is similar to the 2-rate implementation. The multi-rate approach attenuates the first image by only 3 dB, while the power combiner provides a lower mismatch resulting in 3 dB of attenuation.

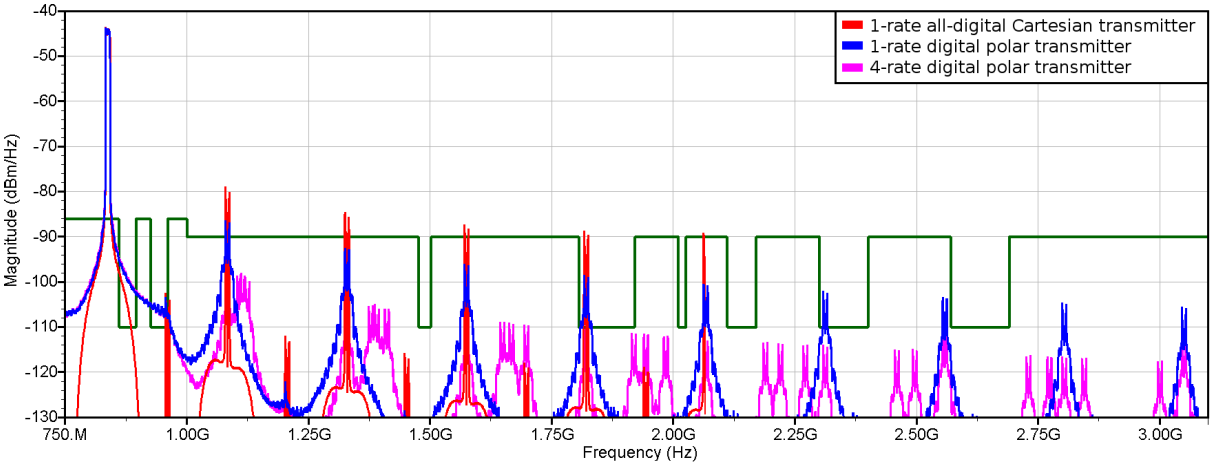


Figure 3.31: *4-rate DPA spectrum with 837 MHz frequency carrier*

Figure 3.31 shows the spectrum in case of a LTE signal with 10 MHz channel bandwidth and 837 MHz carrier corresponding to Band 20. In order to meet the spurious emission constraints, the sample rate conversion ratios are set to 1, 1.1, 1.125 and 1.167. The spectrum below 700 MHz is not shown due to the high level of spurious allowed in this band (>-90 dBm/Hz). These simulation results show the ability of the proposed architecture to manage its spurious emission under different configuration (delivered power, center frequency and channel bandwidth), by simply tuning the SRC ratios.

3.6 Conclusion

The proposed architecture exploits the multi-path approach, together with multi-rate processing, and power recombination. The sampling rate diversity is obtained by sampling rate conversion before the RF modulator. This baseband rate conversion takes advantage of the high digital processing density of advanced low power processes. The images generated by each path appear at distinct frequencies which increases the fundamental to image ratio after the recombination of the paths.

The simulated system was based on a polar approach but the underlying principles can also be implemented in a Cartesian system. Nevertheless, the Cartesian approach requires more signal processing. Sample rate conversion must be performed on both I and Q paths while the polar approach only needs sample rate conversion on the envelope path. The polar approach also offers the possibility to perform phase filtering which increases the image attenuation. The next chapter will detail the prototype designed in an advanced CMOS process to validate the theory presented in this section.

Chapter 4

2-path 65nm CMOS DPA design

4.1 Introduction

The proposed architecture replaces a single RF modulator by several parallel RF modulators with sample-rate diversity. In this way, the RF modulator can be based either on quadrature or polar modulation. However, the polar implementation shows promising advantages such as pre-distortion and enhanced power efficiency. The spurious management ensured by this new approach greatly depends on the number of paths. The verification of the images attenuation implies the design of a complete transmitter from the baseband symbol generation up to the power recombination of the RF modulators output. However, direct implementation of the transmitter in CMOS process would complicate the validation setup. Thus, standard functions will be realized with dedicated equipment. This includes the digital baseband processing, phase modulation, matching network and power recombination. However, the demonstrator requires components of the all-digital to RF modulator to be integrated in order to validate the general principle of the proposed architecture. In this context, it was decided to realize a 2-path digitally-controlled power amplifier in a 65nm CMOS process from STMicroelectronics.

This chapter will cover the design methodology. First, the general 2-path implementation and the choice of the DPA as digital modulator will be detailed with some interface considerations. Second, the DPA implementation itself will be enlighten with the converter segmentation, unit-cell structure, matrix arrangement and PA characterization. Third, the DPA optimizations performed to increase the stability and reduce the input impedance swing will be detailed with special attention on the compensation cells. Finally, the final circuit architecture and layout of the implemented system on silicon will be presented.

4.2 System overview and specification

The spurious emission attenuation performed by the proposed architecture is highly dependent of its number of paths. Of course, the two paths implementation presented on Figure 4.1 is the minimum required in order to observe the effect of image splitting and attenuation and at least four paths would be needed to offer important image attenuation while providing a large set of sample-rate configurations.

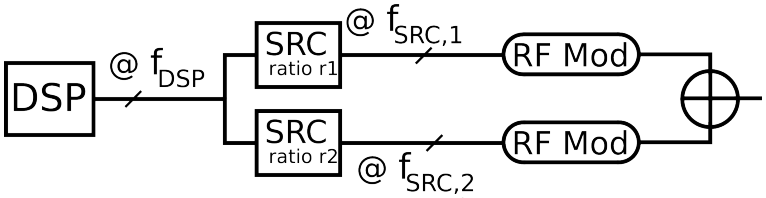


Figure 4.1: *2-rate implementation*

All-digital polar transmitters allow baseband processing that includes digital pre-distortion and power control while offering power efficiency improvement. In this case, each path requires a digital PA. The total area occupied by one DPA is mainly affected by the power stage. The area occupied by a two or more paths DPA is similar when designed to deliver the same recombined output power level. However, the area occupied by baseband processing (sample-rate conversion) and power combiner is proportional to the number of paths. Due to surface limitation the implemented prototype implements only two paths and is depicted on Figure 4.2.

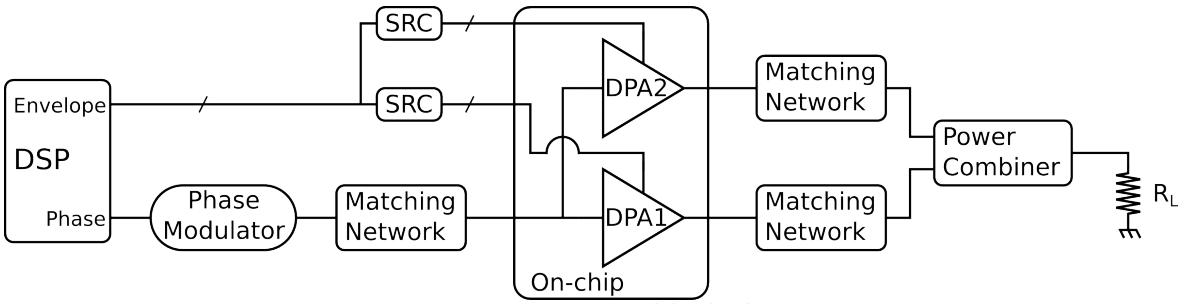


Figure 4.2: *Prototype block diagram*

As demonstrated in [15] and simulated with the architecture on Figure 4.2, in case of narrow band transmitter, 6-bit envelope signal is the minimum to avoid constraints violation due to spectral regrowth around the fundamental. This value increases to 10-bit when phase filtering occurs and wideband transmitters are considered. Two extra bits were added to implement power control.

The sample-rate converter (SRC) is a key block in the proposed architecture. Special attention must be paid to the interpolation filter used to reconstruct the ideal smooth envelope signal before re-sampling to the new sample-rate. Basic N-tap linear interpolation only attenuates the Nth first images with a squared sinc transfer function [13].

These residual images can degrade the signal spectrum at the SRC output. Due to the SRC complexity and time cost, it was chosen to perform the rate conversion off-chip in an FPGA. This point will be detailed in the next chapter regarding the testbench of a 2-path transmitter with the 2-path CMOS DPA and external processing.

Direct control of the DPA matrices by external baseband processing would require 14 digital signals (12bit ACW + enable + clock) for each path resulting in a total of 28 digital pads. Moreover, pad ring rules imply alternate power and I/O pad pattern. In order to lower the area extension introduced by digital interface, the envelope code word is serialized. The serialization scheme is depicted on Figure 4.3. A double data rate format (DDR) is applied to each 4-bit subgroup of the envelope code word while a clock signal with twice the symbol rate is needed.

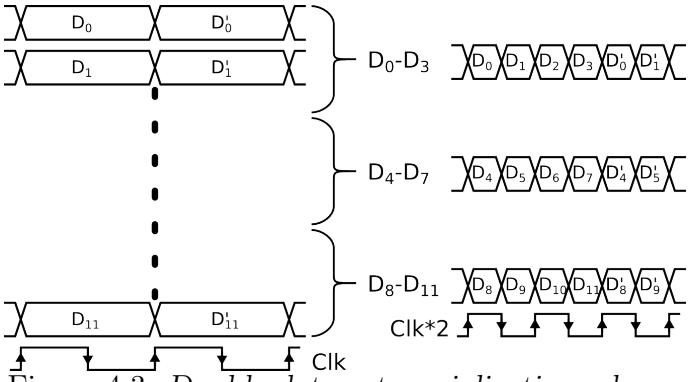


Figure 4.3: *Double data rate serialization scheme*

The amplitude code word is reconstructed by a 4-bit deserializer as represented on Figure 4.4. The clock signal (Clk) is obtained by dividing on-chip the input clock-frequency by two. With the objective of synchronizing the on-chip clock signal and the input serial data, the clock divider block is controlled by an enable signal. The total number of digital inputs required in this configuration is reduced to 5 (3 serial data, 1 clock and 1 enable) per DPA.

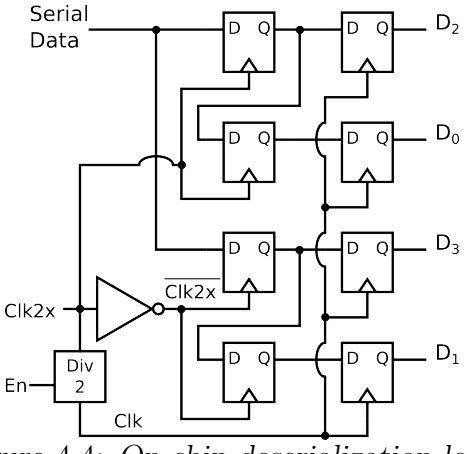


Figure 4.4: *On-chip deserialization logic*

Based on simulations including the pads and the matrix controller, with extracted models and worst case corner, the estimated maximum symbol rate is 800 MS/s and would require a 1600 MHz clock signal. However, the maximum clock speed of the FPGA I/O is 700 MHz which implies a maximum sample-rate of 350 MS/s.

As explained in the state-of-the-art overview of wideband power combiners, the transformer based matching network [11] looks promising. Nevertheless, area limitation restrains its on-chip implementation. Thus, the impedance matching and power combination are performed in two steps with external components.

To demonstrate the wideband image attenuation of the proposed architecture, the targeted frequency band is set from 0.8 to 3 GHz. In order to cover several standards without the need of an additional power amplifier, the total power delivered by the 2-path amplifier must reach the 23 dBm output power of class 3 devices as defined in [2] and listed in Table 4.1.

Table 4.1: *Power Specification*

Standard	Power specification
Bluetooth	4 dBm
802.11b/g	20 dBm
UMTS/3G Class 4	21 dBm
E-UTRA Class 3	23 dBm
UMTS/3G Class 3	24 dBm
UMTS/3G Class 2	27 dBm

The 2-path prototype must support up to 20 MHz bandwidth baseband channels which is the maximum specification for E-UTRA and 802.11a/b/g. Due to the non-linear transformation from IQ to polar form, the envelope signal must be at least oversampled by a factor of 10 to avoid ACPR degradation. Then, the envelope sample rate must be configurable from 100 MHz up to 300 MHz.

The overall targeted performances of the prototype are listed in Table 4.2.

Table 4.2: *Targeted transmitter performances*

P_{1dB}	23 dBm
frequency band	0.8 - 3 GHz
channel bandwidth	20 MHz
sample rate	up to 300 MS/s

The next sections will detail the circuit level implementation of the 2-path DPA.

4.3 DPA implementation

As explained previously, the demonstrator is based on a 2-path digital polar transmitter. It was designed in a 65nm CMOS process from STMicroelectronics with a 1.2 V low power thin oxide and 2.5 V thick oxide transistors.
This section will detail the implemented DPA. The general structure of the DPA will be explained. The converter segmentation and control logic will be depicted. Then, the unit-cell structure will be detailed focusing on its implementation and layout considerations.

4.3.1 General structure

4.3.1.1 MSB-LSB Segmentation

The DPA merges the power stage with the digital-to-analog converter. The design methodology and rule of thumbs for DAC implementation can be applied to the DPA. In order to obtain good Differential Non Linearity (DNL) and Spurious Free Dynamic Range (SFDR), a thermometer-coded approach is desirable. However, the extra logic required to control the 4095 cells in case of 12-bit converter would complicate the design and impact the surface. Then, a segmented approach was chosen to alleviate the design complexity. The trade-off results in an 8-bit thermometer-coded matrix (noted the MSB matrix) combined with a 4-bit binary-weighted matrix (noted the LSB matrix). The 8 bits for the MSB was chosen in order to optimize the DNL over a sufficient dynamic range to avoid ACPR degradation. To limit control connections, the cells control is implemented with a grid pattern. The structure of one DPA is depicted on Figure 4.5. In this configuration, only row and column signals are needed, the rows being controlled by the bits D_4 to D_7 while the columns by the bits D_8 to D_11. The row and column controllers will be detailed in the next point. The LSB matrix is done by using groups of unit-weighted amplifier directly controlled by the respective ACW bits (D_0 to D_3). The weight of the cells from the MSB matrix are 16 times the ones of the LSB matrix. The term unit-amplifier will be used below to designate the cell from the MSB matrix, while weighted-amplifier will define the cells from the LSB matrix. The controllers drive buffers in order to ensure the control of the cells and also synchronize the signals edges. In fact, the clock was not directly rooted in the DPA matrix due to the complexity of such approach. The matrix already requires several digital signals to control the cells and RF signals beside power rails. Thus the buffers must be well aligned to avoid delays.

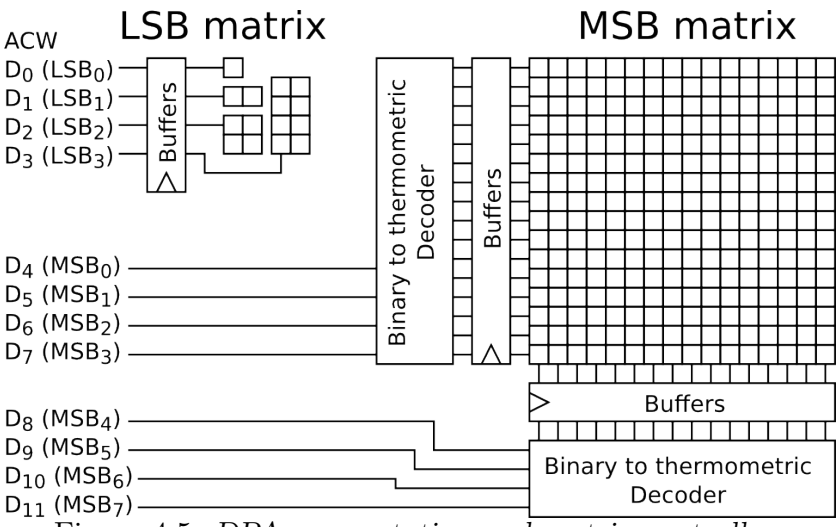


Figure 4.5: *DPA segmentation and matrix controllers*

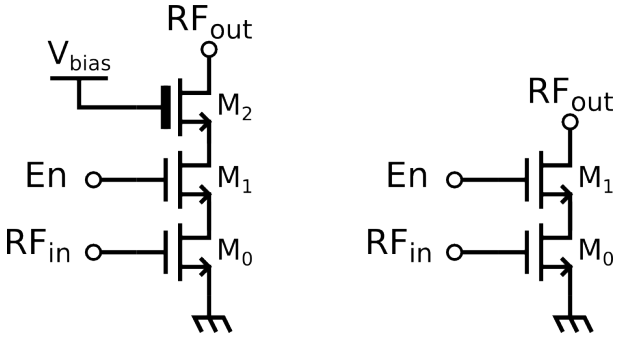
4.3.1.2 Row and column controllers with buffers

The cells of the LSB matrix are directly controlled by the 4 LSB of the envelope code. On the other side, the cells of the MSB matrix require a thermometric code. As represented on Figure 4.5, the chosen approach uses two different thermometric decoders for the rows and columns. Each decoder is controlled by the 4-bit output of a deserializer. The design of the controllers presents no special aspect or challenging fact and will not be detailed. The maximum clocking frequency after extraction is 500 MHz which is sufficient considering the maximum sample-rate forced by the FPGA I/Os.

The main issue with this segmented approach and separated row and column controllers is the delay introduced by the pitch between each unit components and the different capacitances presented by the rows and columns. Delays between the signals when the ACW changes can introduce glitches, which cause spectral spurious. The buffers were designed to synchronize the signals edges at the matrix port for both rows and columns. The simulations were performed with extracted thermometer decoder and especially extracted matrix and clock tree. The electrical paths between the buffers and decoder were compensated with metal lines. The worst delay between edges after extraction is lower than 100 ps, which is small enough compared to the setup time of the amplifier first stage.

4.3.1.3 Unit-cell implementation (pre-PA, PA)

Most of the published DPAs [7, 14, 74] are based on single stage amplifiers with serial switch and potential cascode transistor as represented on Figure 4.6.



a) with cascode transistor b) without cascode transistor
Figure 4.6: *One-stage amplifier with and without cascode transistor*

These simple implementations suffer from three main drawbacks. First, the input capacitance presented by the common source amplifier is proportional to the desired output power. The resulting important capacitance can highly complicate the input matching network limiting the achievable bandwidth. Second, the switch transistor is on the signal path. In this configuration, attention must be paid to ensure reliability of the transistor under potential current and voltage peaks when switching, while the switch size must be large enough to drive the current. Third, the output capacitance is highly dependent of the switch state in the Figure 4.6.b) configuration, which introduces output distortions.

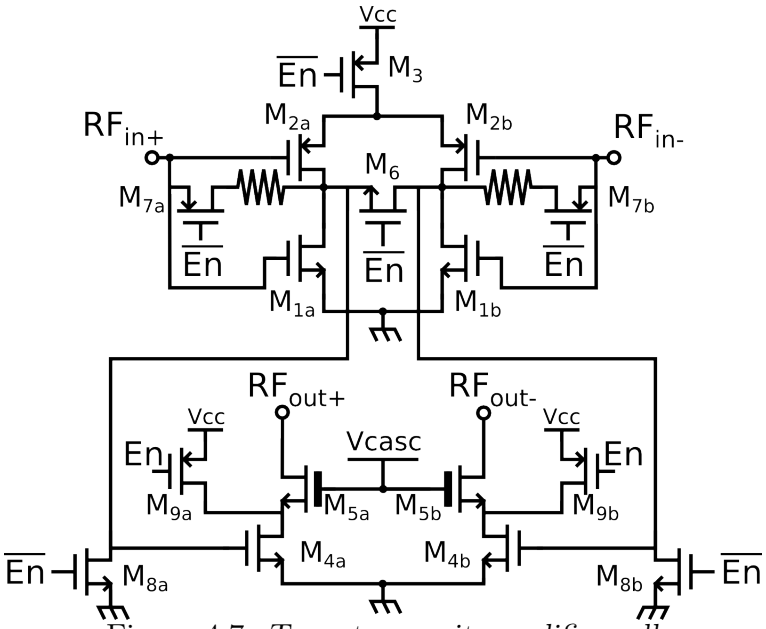


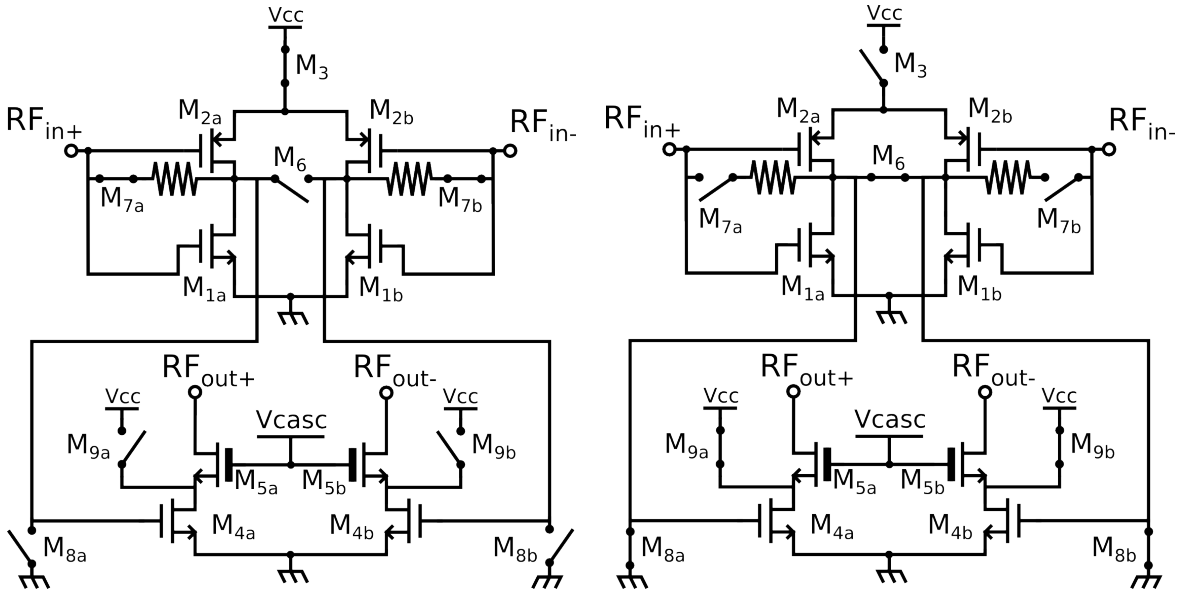
Figure 4.7: *Two-stage unit amplifier cell*

The proposed unit-cell is based on the two-stage implementation described in [15]. The principle is to use the first stage as a controlled source in order to tie the input of the second stage to zero, which avoids the use of serial switches in the output stage and

reduces the output distortions. The schematic of the proposed two-stage unit amplifier cell is shown on Figure 4.7.

The general amplifier is a pseudo-differential implementation with no intrinsic common mode rejection. The first stage is a self-biased complementary common-source amplifier ($M_{1a;b}$ and $M_{2a;b}$) directly coupled to the output stage, which offers a wide operating bandwidth. This last stage is a Class-A amplifier with thick oxide cascode transistors ($V_{DSmax} = 2.5V$) which allow increasing the output swing to 4 V. The Class-A type was chosen to ensure high linearity without the need of narrow-band output matching network. The main objective of the prototype is to demonstrate the image attenuation in multi-rate transmitter, then efficiency improvement was of lower priority than linearity.

The cell switching is ensure by several switches (M_3, M_6-$M_{9a;b}$). When the cell is ON, M_3 supplies the first stage and $M_{7a;b}$ allow self-biasing. Otherwise, when the cell is OFF, M_6 and $M_{8a;b}$ tie the last stage input to the ground while $M_{9a;b}$ reduce the leakage current and limit source voltage swing of the cascode transistors. The configurations of the unit amplifier cell in both states are represented on Figure 4.8.



a) ON state b) OFF state

Figure 4.8: *Unit amplifier cell configurations*

At the contrary of [15] which requires only the inverted enable signal, the proposed architecture also needs the non-inverted enable signal. The delay between the inverted and non-inverted signals must be small enough to avoid direct path from V_{CC} to ground through $M_{9a;b}$ and $M_{4a;b}$. This is not a problem when the cell switches to the ON state due to the setup time of the first stage which delays the $M_{4a;b}$ activation. However, switching off the cell must leave enough time to $M_{8a;b}$ to discharge the gate of $M_{4a;b}$. Delaying the enable signal controlling $M_{9a;b}$ against the one controlling $M_{8a;b}$ by one inverter is suffi-

cient. The final enable logic is represented on Figure 4.9. Column buffers drive twice the input capacitances than the row buffers, and are sized accordingly.

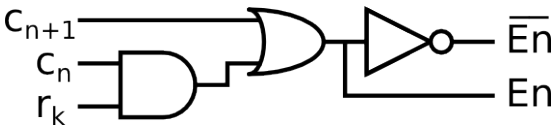


Figure 4.9: *Enable logic*

The layout of the unit-amplifier implemented in the MSB matrix is shown on Figure 4.10 where both amplifier and logic stages are depicted. Special attention was paid to limit the parasitic and lowering the occupied area to 16.6 x 8.4 μm^2. The transistors $M_{7a;b}$ are source connected to the RF input pads and require a latch-up protection ring. This problem could be solved in future designs by using a pre-PA to relax layout constraints. The need for several signals (RF and digital controls) and supply (cascode biasing and first stage supply) greatly complicated the cell arrangement.

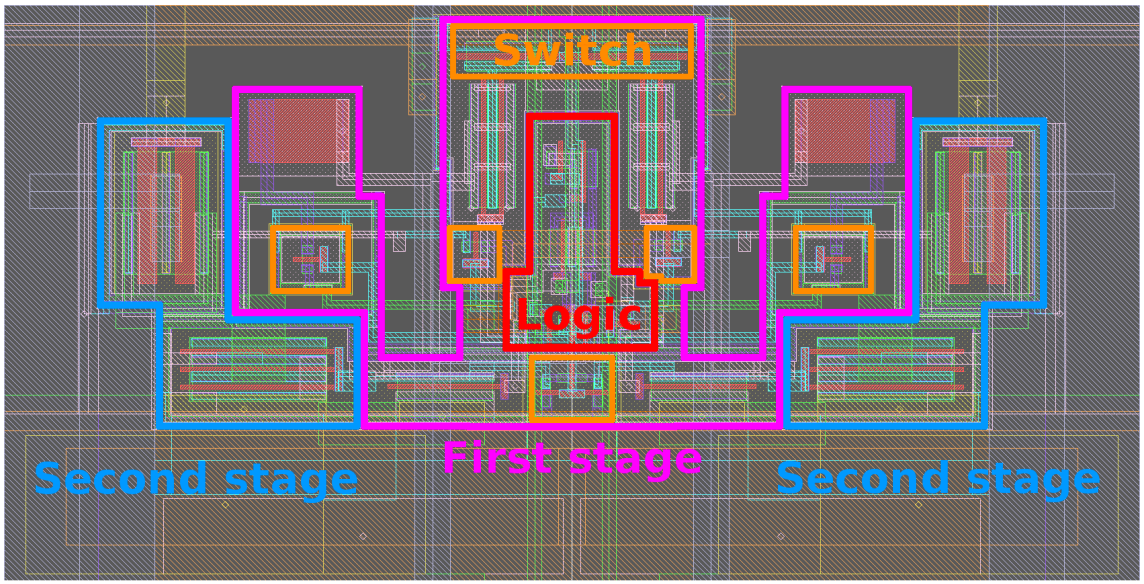


Figure 4.10: *Layout of an unit amplifier cell with annotation*

The RF signals and power supplies require high DC currents. Thus, wide rails are used to respect the electro-migration constraints. These signals connections are symbolized on Figure 4.11. The input RF polarity is inverted compared to the output RF polarity to decrease the coupling between input and output in differential mode, which helps stabilize the amplifier in differential mode. Lower metal levels are used to connect the digital signals (R_k, C_n and C_{n+1}). The configuration with vertical rails for RF signals and horizontal ones to power supplies helps to decrease the coupling capacitances at the crossing points.

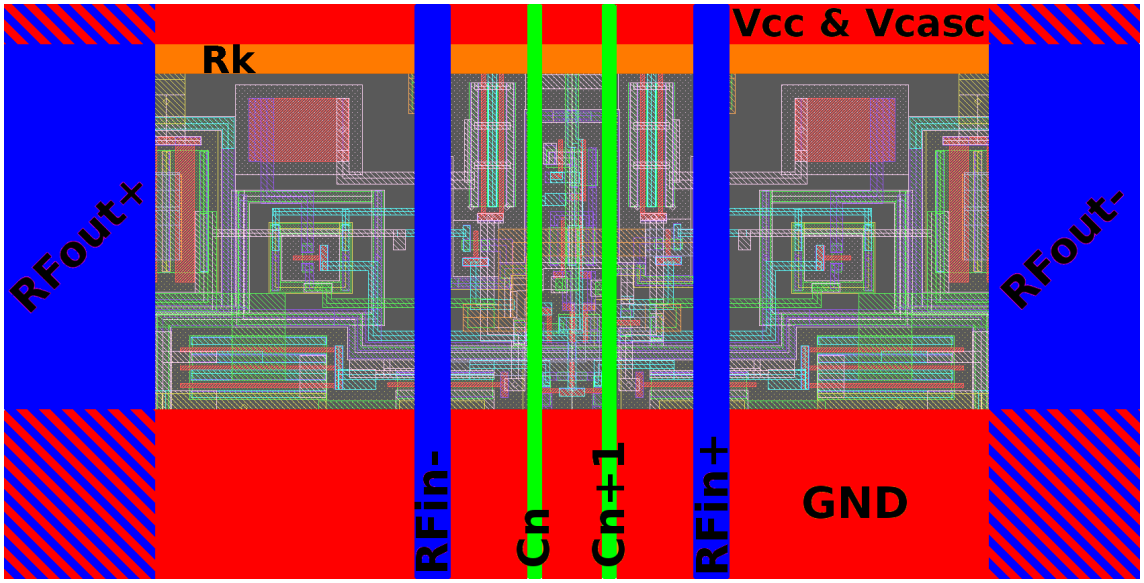


Figure 4.11: *Simplified layout with power rails*

When the unit-cell of the MSB matrix is ON, the total drain current of the cascode stage is 360 μA at 2.5 V and the first stage draws 80 μA from the 1.2 V supply. The DC power consumed by one cell is 1.9 mW.

4.3.1.4 Matrix arrangement

The robustness against matrix mismatches is a critical point to be addressed in converter design. In the case of DPA, the important area required to provide enough power made the unit-amplifier highly dependent of process variability.

Two matrix arrangements were performed to limit mismatch between the unit amplifier cells. First, the cells were placed according to a pseudo random pattern in order to average the impact of process variability along both directions, which lowers the INL. The random scheme is easily applied to the binary weighted LSB matrix as represented on Figure 4.12. The low number of cells allows direct control signal connection.

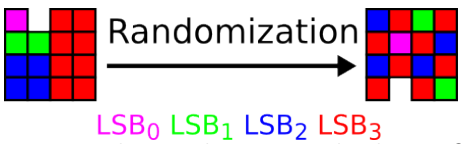


Figure 4.12: *Random scheme applied to LSB matrix*

On the other hand, the connection of the 255 cells in the MSB matrix would be too complicated with a fully balanced pattern when consecutive cells are not located on the same row or column. Then, it was decided to alternate the row and column indexes in order to keep one control signal per row and column. Such scheme is represented on Figure 4.13 where row and column indexes are indicated.

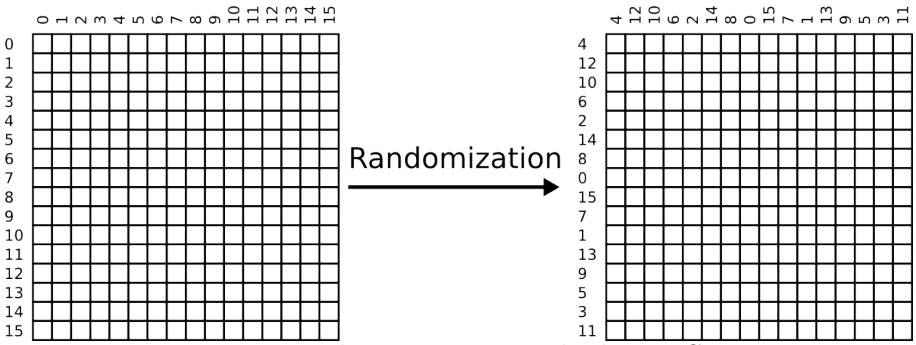


Figure 4.13: *Random pattern applied to MSB matrix*

The MSB and LSB matrices arrangement also ensures an homogeneous distribution of the power consumption and dissipation. Then, the memory effect produced by heating is equally divided over the amplitude code word. While non-patterned matrix would create a memory effect between the cells more often ON and OFF.

The last arrangement to lower the impact of spatial process variability was to add two extra row of dummies along each side of the MSB and LSB matrix as represented on Figure 4.14.

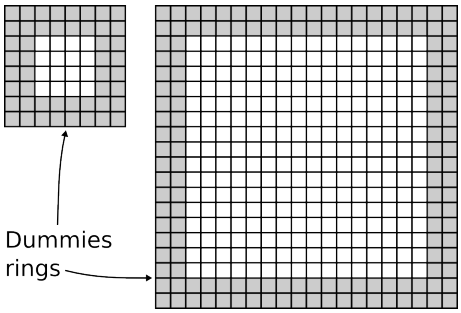


Figure 4.14: *Dummies rings insertion*

The designed DPA occupies a total area of 370 x 235 μm^2 and the layout is represented on Figure 4.15. This surface integrates the LSB and MSB matrices as well as the row and column controllers including buffers.

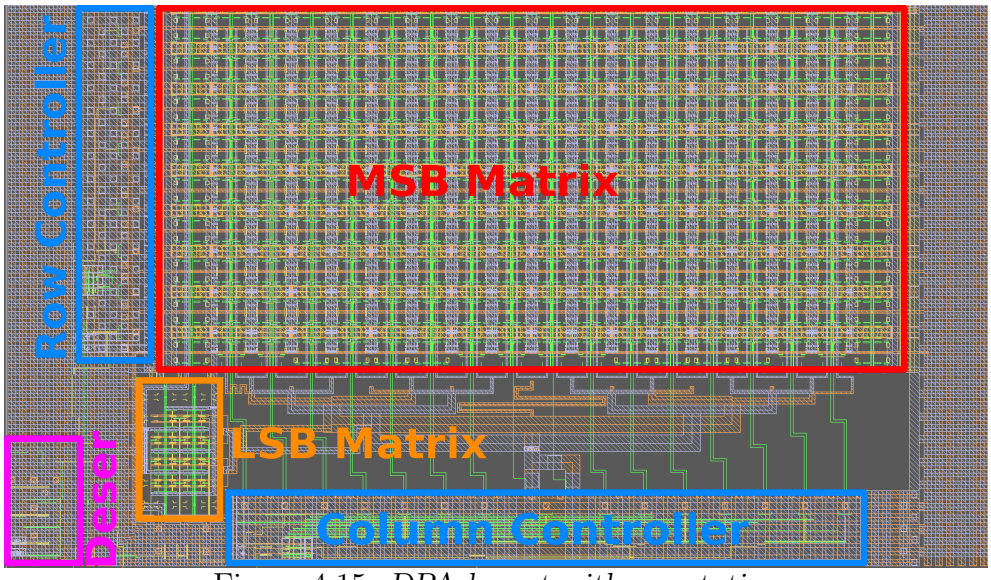


Figure 4.15: *DPA layout with annotation*

4.3.2 Characterization

The extracted DPA was characterized using Load-Pull simulations. The aim was to determine the optimum load to ensure maximum power and efficiency. The characterization was performed under one-tone signal with all the DPA cells activated. Figure 4.16 shows the optimum differential load to be presented to the DPA in order to maximize the 1dB compression point. A simple load approximation is also depicted besides P_{1dB} circles obtained at 1.5 GHz.

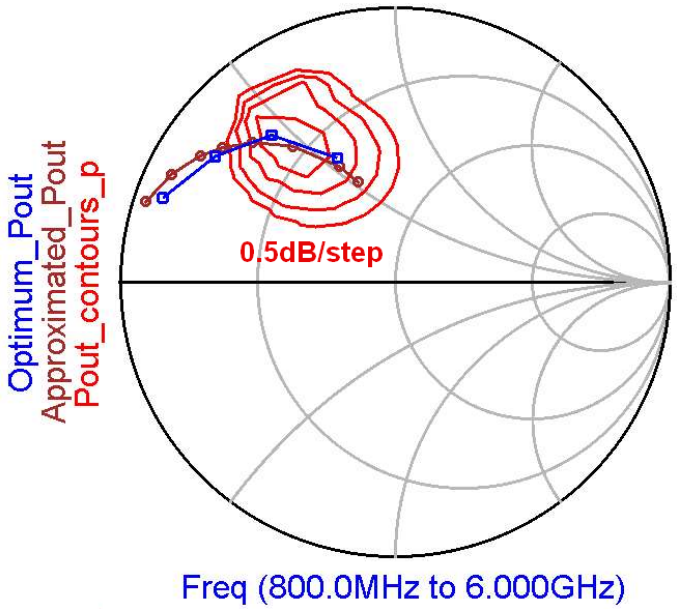


Figure 4.16: *Characteristic of an extracted DPA*

The output differential impedance of the DPA was modeled by a resistance and capacitance in parallel as explained in [11]. The resistance was set to 52 Ω and the capacitance to 3.3 pF. The P_{1dB} for a single DPA in case of approximated load ($P_{out\ Zpa}$) was compared to the optimum one ($P_{out\ Zopt}$) on Figure 4.17. Thanks to the spaced circles, the load approximation does not impact the maximum .

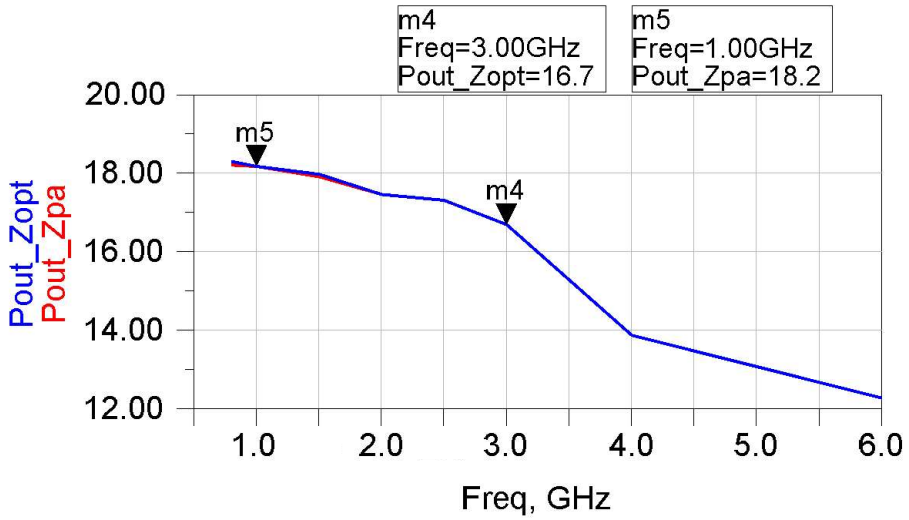


Figure 4.17: *Optimum and approximated P_{1dB}*

The DPA was expected to provide 20dBm of power over the 0.8 3 GHz band. But the optimizations done to stabilize the DPA and its input impedance decrease the 1dB compression point by 0.6 dB at 1 GHz and 1.6 dB at 3 GHz. Figure 4.18 shows the DPA characteristics with input and output matching networks.

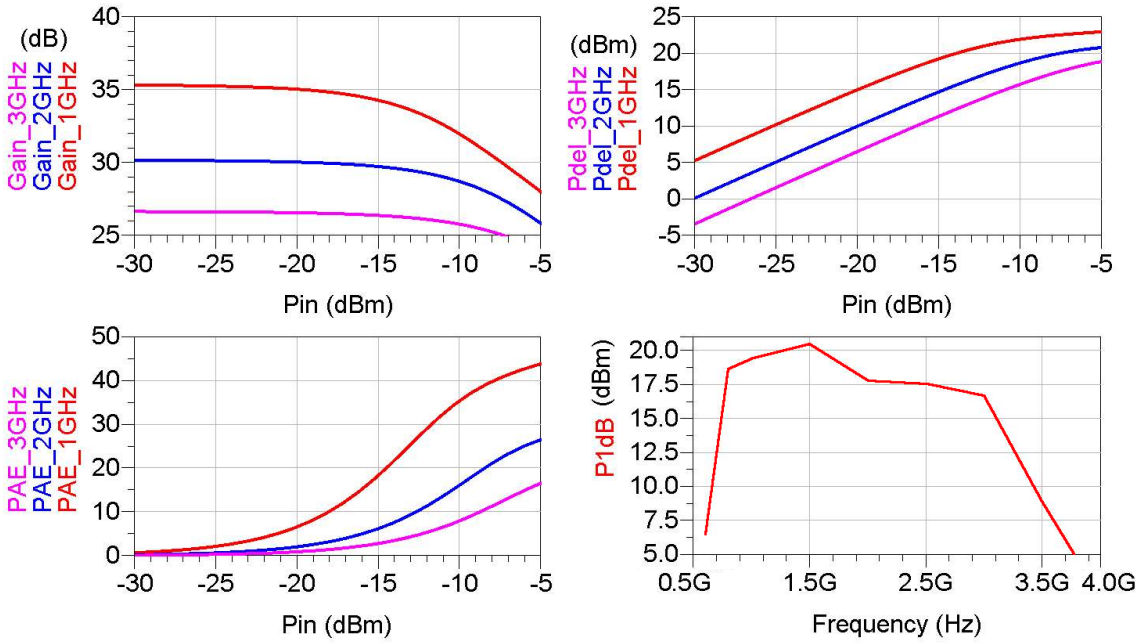


Figure 4.18: *DPA characteristics*

4.4 DPA optimization

Beside the straight-forward design of the DPA, special attention was paid to the optimization of the DPA, such as stability and input impedance. This section will first explain these two limitations of the implemented DPA. Second, the circuits designed to overcome these limitations will be detailed.

4.4.1 Stability issue

The PA must provide significant gain to ensure good efficiency but stability is also a matter of concern. The PA stability study must take into account all the parasitics from the layout. In our case, the implemented DPA was unconditionally stable before layout extraction, but the parasitics introduce instability. This is due to three effects: first, the pseudo differential form of the unit amplifier cells do not implement any common mode rejection. Second, the load impedance presented by the power combiner (i.e: transformer) in common mode can be infinite resulting in high common mode amplification. Third, parasitic coupling between output and input can introduce non-negligible feedback. As stated before, the RF input and output polarity were inverted in order to increase stability in differential mode.

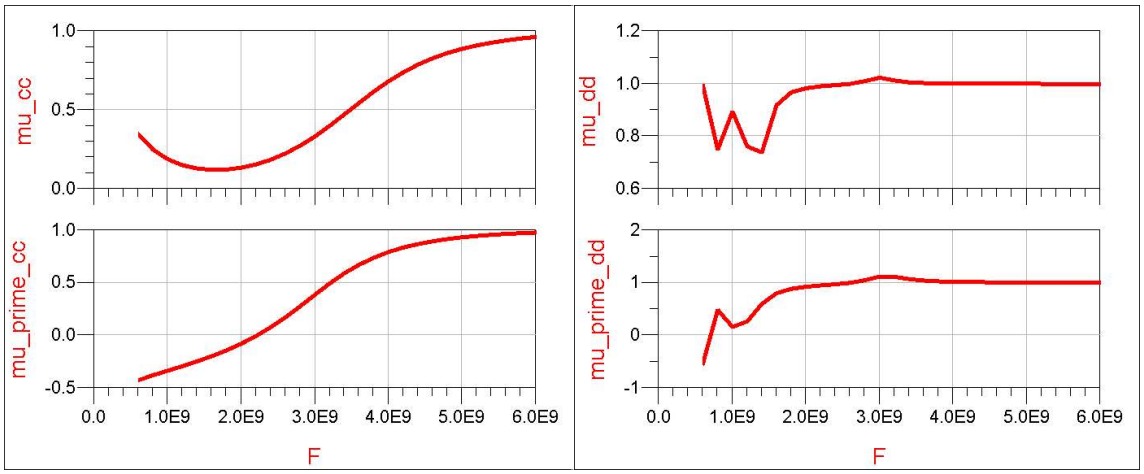


Figure 4.19: *μ and μ' factors of the DPA in both Common-to-Common and Differential-to-Differential mode*

Figure 4.19 shows the stability factors μ and μ' of the DPA after layout extraction for the common-to-common and differential-to-differential mode when loaded with a transformer. μ and μ' define the distance between the center of the Smith chart and the unstable region for the source and load impedance, respectively. The system is unconditionally stable if one of them is greater than 1, otherwise the stability circles must be take into account.

The system is potentially unstable from 0.8 to 1.3 GHz in differential mode but is unstable from DC to 5 GHz in common mode. The negative value of μ_{-cc}' and the close to zero μ_{-cc} lead to the load stable region out of the smith chart and small source stable region. The layout extraction highlights the strong coupling between both input and output RF signals. Figure 4.20 represents the parasitic capacitance for one column (16 parallel unit amplifiers).

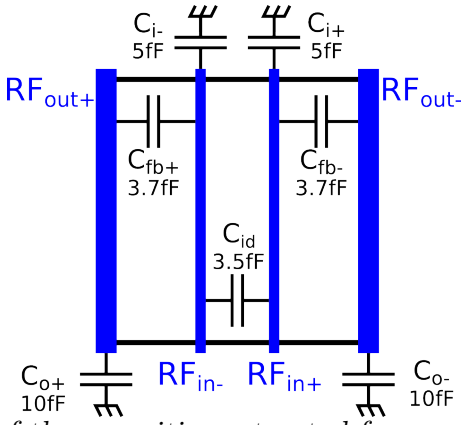


Figure 4.20: *Schematic of the parasitics extracted from one MSB column (16 cells)*

Figure 4.21 represents the total parasitics added to the DPA schematic. The 10 fF difference between both output capacitance C_{o+} and C_{o-} is due to the number of RF rails in the DPA. There are 16 alternate columns resulting into 8 RF_{out-} rails and 9 RF_{out+} rails.

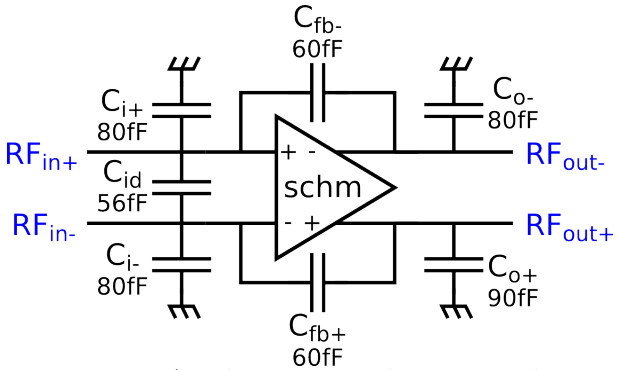


Figure 4.21: *DPA schematic with extracted parasitics*

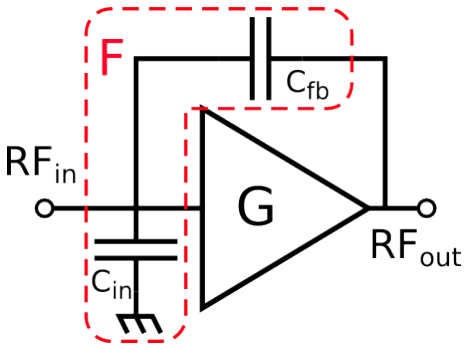


Figure 4.22: *Feedback loop due to parasitic elements*

Common-mode oscillations are mainly due to the feedback gain created by the DPA input impedance in parallel to the input parasitic impedance C_{in} and the capacitance noted C_{fb}

on Figure 4.22. The positive gain of the DPA (G) imply a wide instability zone over the system bandwidth.

Figure 4.23 shows the common-mode open loop transfer function of the DPA with parasitic elements. The loop gain is largely higher than 0 dB over the band of interest.

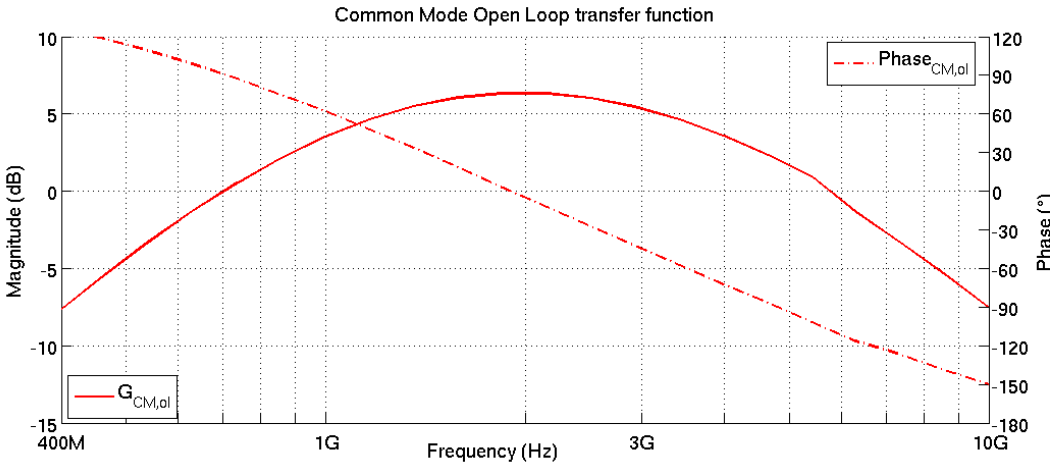


Figure 4.23: *CM transfer function after parasitics extraction*

The first approach to stabilize the system would be to lower the coupling between the input and output RF connections. However the DPA layout was already optimized and no additional metals layer were free. Increasing the gap between the RF rails would affect the silicon surface occupied. Two techniques were used to suppress oscillations. The first one is the addition of a load circuit in order to avoid high common mode gain with low impact on differential gain. The second technique is the use of compensation cells with two main advantages in term of stability and input impedance variation.

4.4.1.1 Limitation of the CM gain with dummy loads

To limit the common gain of the DPA, a dummy load was added as represented on Figure 4.24. The dummy load presents the advantage to only add a small capacitance at the DPA output in differential mode while providing a sufficient load in common mode to lower the open loop gain from 1 to 12,6 GHz.

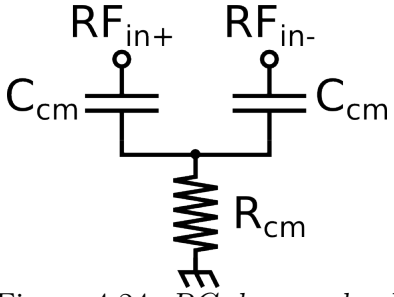


Figure 4.24: *RC dummy load*

Other solutions based on active load such as the cross-coupled circuit on Figure 4.25 present the advantage to provide a high differential impedance and a small common

mode impedance but were rejected due to their impact on the overall efficiency and limited bandwidth.

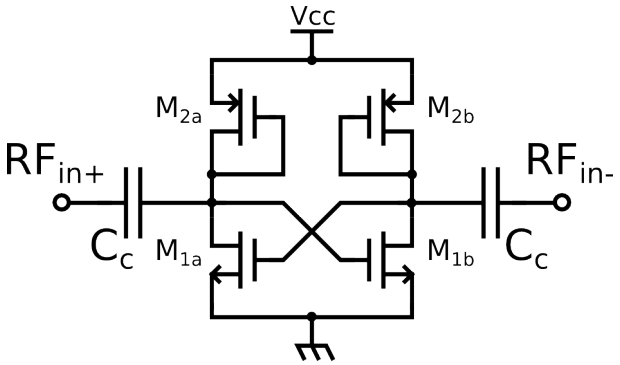


Figure 4.25: *Cross-coupled dummy load*

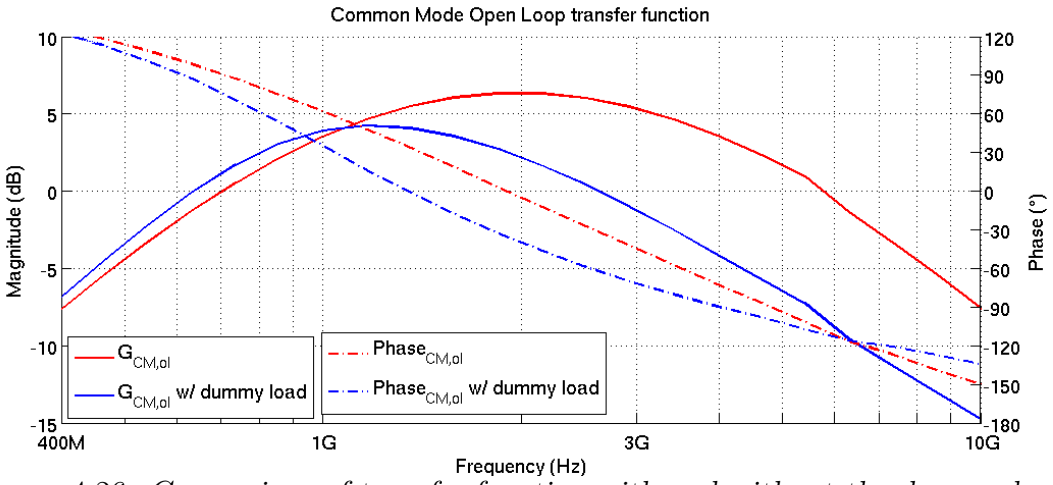


Figure 4.26: *Comparison of transfer function with and without the dummy load*

Figure 4.26 shows the impact of the dummy load on the open loop transfer function. The CM gain is decreased by 2.5 dB. This approach can not lower the CM gain enough without increasing the C_{cm} capacitance which would impact the DM bandwidth and gain. The next point will describe the input impedance variation and the proposed compensation cell.

4.4.2 Input impedance variation

The input impedance presented by a DPA is set by the parallel combination of the input impedance of the unit-cells, and can be approximated by

$$Z_{in} = (N_{ON} * Y_{ON} + N_{OFF} * Y_{OFF})^{-1} \tag{4.1}$$

With N_{ON} and N_{OFF} representing the number of cells in ON and OFF state, and Y_{ON} and Y_{OFF} standing for the admittance presented by a unit-cell as shown on Figure 4.7 in ON and OFF states. As explained in [15], assuming that the intrinsic channel capacitance is a negligible fraction of the total gate impedance, the input differential capacitance can be supposed constant and equal to $C_{in} = N_{cell} * (C_{gs1a;b} + C_{gs2a;b})/2$. However, the gate to drain capacitance variation can be non negligible due to miller effect. Moreover, the switching of the self-biasing path introduces significant variations of the resistive input impedance. The small-signal schematic of the half unit-amplifier cell is represented on Figure 4.27. The transistor M_3 is used as a switch and has no impact on the input impedance either in common or differential mode. With R_{sb} the total self-biasing resistance taking into account the physical resistor and the r_{dson} of the switch $M_{7a;b}$.

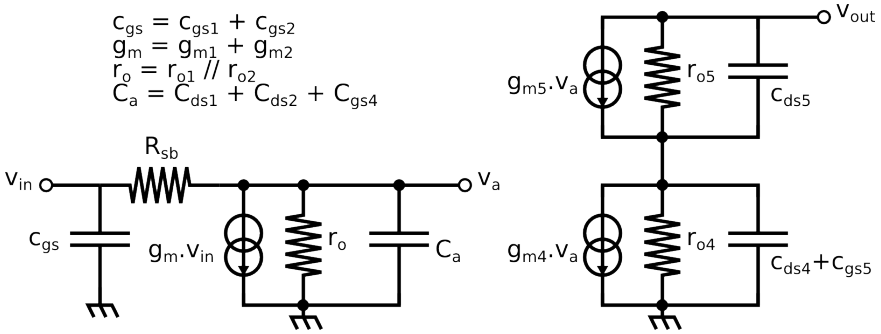


Figure 4.27: *Small-signal schematic of the half unit-amplifier cell*

The impedances and resistances are defined as seen on one RF port and referenced to ground. The Differential Mode noted DM refers to a differential signal apply to RF_{in+} and RF_{in-}, while the Common Mode noted CM refers to a signal applied with the same polarity to both RF_{in+} and RF_{in-}. The term differential impedance refers to the impedance seen between RF_{in+} and RF_{in-} ports, which is equivalent to twice the impedance seen on a single RF port in DM.

The resulting input impedance presented by the half-cell circuit from the MSB matrix

when ON is defined as:

$$Z_{in\ half\ cell} = \left(\frac{1}{j\omega C_{gs}}\right) || \frac{R_{sb} + \left(r_o || \frac{1}{j\omega C_a}\right)}{1 + g_m \left(r_o || \frac{1}{j\omega C_a}\right)} \tag{4.2}$$

Due to the high R_{sb} compare to r_o the equation can be approximated to:

$$Z_{in\ half\ cell} = \left(\frac{1}{j\omega C_{gs}}\right) || \frac{R_{sb}}{1 + j\omega r_o C_a + g_m r_o} \tag{4.3}$$

The natural frequency at the first stage output ($(2\pi r_o C_a)^{-1}$) is greater than 8 GHz and can also be ignored. (4.3) then becomes:

$$Z_{in\ half\ cell} = \left(\frac{1}{j\omega C_{gs}}\right) || \frac{R_{sb}}{1 + g_m r_o} \tag{4.4}$$

In our case, the impedance presented by the half-cell cell is 8.13 kΩ in parallel with 2.8 fF. On the other side, when the cell is OFF the input impedance only includes the capacitance due to the infinite r_{dson} of the switch $M_{7a;b}$. The input impedances of a unit-cell from the MSB matrix in different configurations are listed on Table 4.3.

Table 4.3: *MSB unit-cell input impedance summary*

Unit-cell state		One port
ON	Input Resistance	8.13 kΩ
	Input Capacitance	2.8 fF
OFF	Input Resistance	∞ Ω
	Input Capacitance	2.8 fF

These values combined with (4.1) result in the behavior depicted on Figure 4.28. The curve represents the resistance seen at one RF input port of the 2-path architecture (2 DPA in parallel) for different ACW.

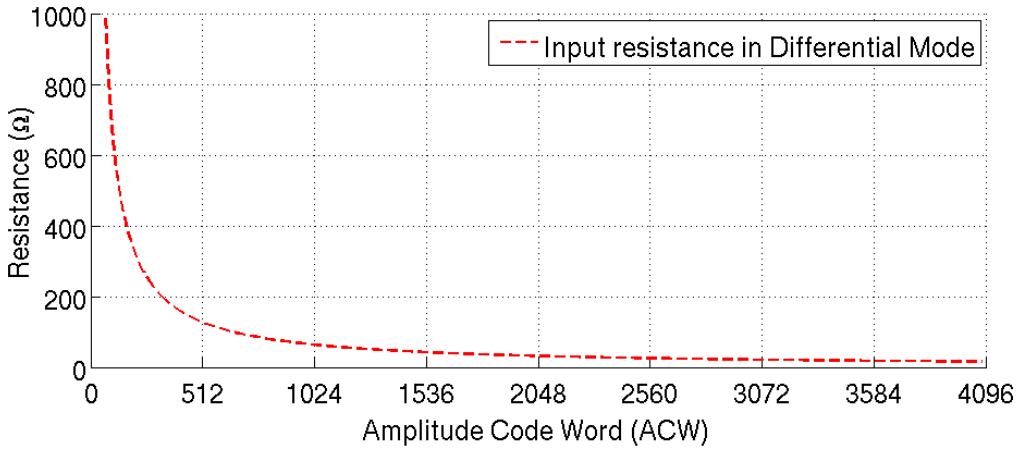


Figure 4.28: *Input impedance in differential mode against ACW variation*

The resistances presented at the RF_{in} ports vary from 4.06 kΩ for one MSB cell activated to 15.94 Ω when the 255 MSB cells and all the LSB cells are activated in both DPA. Thus, ACW variation generates modulation of the input impedance which introduces distortions. The distortions are heavily dependent of the modulation of the amplitude signal. The impedance matching is also impacted by the non-constant resistance part of the impedance. This point is addressed by the compensation cell described in a later section.

4.4.2.1 Compensation cells

Beside limiting the common gain of the output stage, the feedback signal can also be decreased by lowering the impedance presented at the DPA input in common mode. For this purpose, compensation cells were added in parallel with the DPA cells.

4.4.2.1.1 Principle The proposed compensation cell is shown on Figure 4.29. As it will be detailed later in this section, four switches are used to control the input impedance in DM. They are sized in order to provide high cut-off frequency. In our case, the cut-off frequency of the switches is above 20 GHz, thus the switch resistance will be ignored in the discussion.

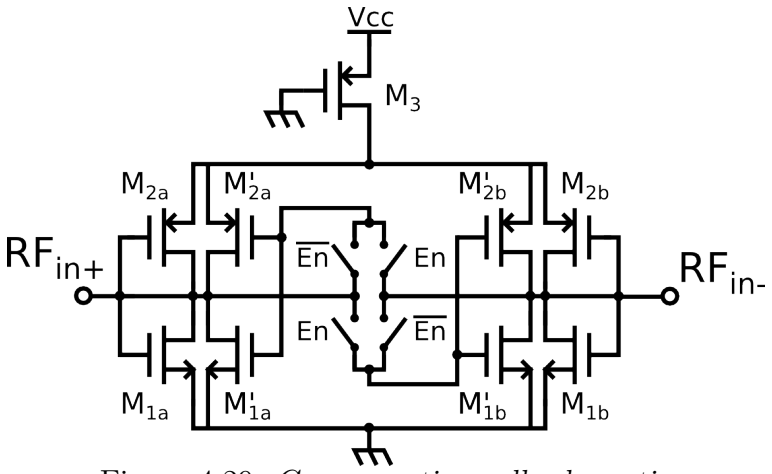


Figure 4.29: *Compensation cell schematic*

The schematic of the compensation cell shown on Figure 4.29 is matched to the input stage of the elementary amplifier cell without the self-biasing resistance and switch. It is composed of a main branch ($M_{1a;b}$ and $M_{2a;b}$) and an auxiliary branch ($M'_{1a;b}$ and $M'_{2a;b}$). The main and auxiliary branches are sized the same. When the cell is enabled, the branches are in cross-coupled configuration. In differential mode, the transconductances $g_{m1a;b}$ and $g_{m2a;b}$ are canceled by $g'_{m1a;b}$ and $g'_{m2a;b}$ while adding in common mode. The enabled configuration is shown on Figure 4.30 while (4.5) and (4.6) define the impedance

seen at the RF_{in+} and RF_{in-} ports, without taking into account the input gate capacitance equal to $C_g = c_{gs1} + c_{gs2} + c'_{gs1} + c'_{gs2} = 2 * (c_{gs1} + c_{gs2})$ and with $g_{m_{1,2}} = g'_{m_{1,2}}$ and $g_{ds_{1,2}} = g'_{ds_{1,2}}$. The drain-source impedance of M_3 greatly impacts the input impedance in the common mode.

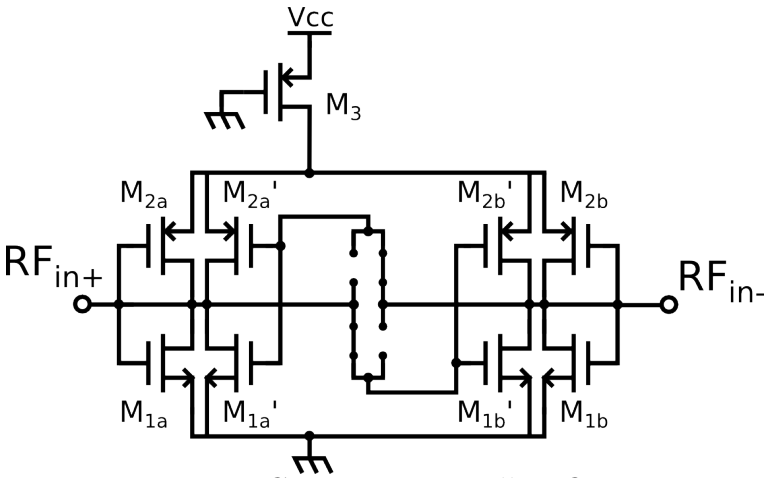


Figure 4.30: *Compensation cell in ON state*

$$\begin{aligned} Z_{in\ cell\ ON\ DM} &= (g_{m1} - g'_{m1} + g_{m2} - g'_{m2} + g_{ds1} + g'_{ds1} + g_{ds2} + g'_{ds2})^{-1} \\ Z_{in\ cell\ ON\ DM} &= 0.5 * (g_{ds1} + g_{ds2})^{-1} \end{aligned} \tag{4.5}$$

$$\begin{aligned} Z_{in\ cell\ ON\ CM} &= \left(g_{m1} + g'_{m1} + g_{ds1} + g'_{ds1} + \frac{1}{\frac{1}{g_{m2} + g_{ds2}} + 4 * r_{o3}} + \frac{1}{\frac{1}{g'_{m2} + g'_{ds2}} + 4 * r_{o3}} \right)^{-1} \\ Z_{in\ cell\ ON\ CM} &= 0.5 * \left(g_{m1} + g_{ds1} + \frac{1}{\frac{1}{g_{m2} + g_{ds2}} + 4 * r_{o3}} \right)^{-1} \end{aligned} \tag{4.6}$$

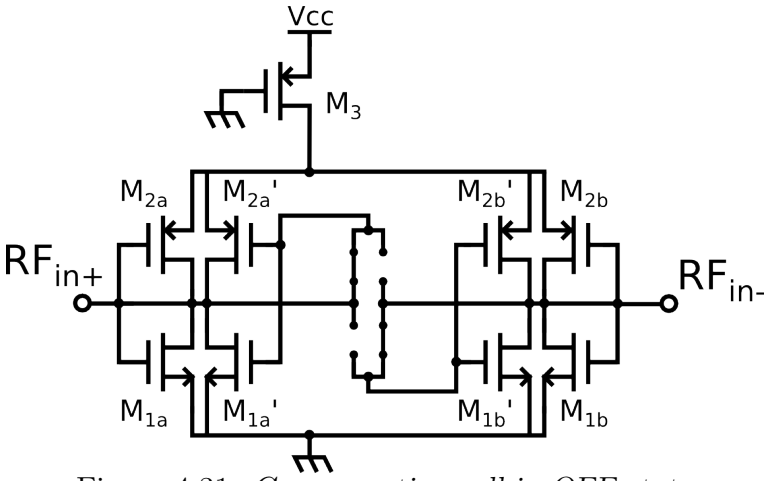


Figure 4.31: *Compensation cell in OFF state*

$$Z_{in\ cell\ OFF\ CM} = Z_{in\ cell\ OFF\ CM} = (2 * (g_{m1} + g_{ds1} + g_{m2} + g_{ds2}))^{-1} \tag{4.7}$$

In the off-state, branches are in parallel in both differential and common mode as represented on Figure 4.31 and defined in (4.7). The simplified impedances including the gate capacitances and presented at the RF_{in+} and RF_{in-} ports are listed in Table 4.4.

Table 4.4: *Compensation cell input impedance*

Cell state	Differential Mode	Common Mode
ON	$(2*(g_{ds1}+g_{ds2})+j\omega C_g)^{-1}$	$\frac{0.5}{g_{m1}+g_{ds1}+\frac{1}{\frac{1}{g_{m2}+g_{ds2}}+4*r_{o3}}+j\omega C_g}$
OFF	$(2*(g_{m1}+g_{ds1}+g_{m2}+g_{ds2})+j\omega C_g)^{-1}$	$\frac{0.5}{g_{m1}+g_{ds1}+\frac{1}{\frac{1}{g_{m2}+g_{ds2}}+4*r_{o3}}+j\omega C_g}$

The S-parameters of the compensation cell are shown on Figure 4.32. As expected by the equations in Table 4.4, the DM impedance in OFF state is slightly different from the CM impedance due to r_{o3}, while the DM impedance in ON state is higher due to the drain-source resistance. The DM impedance presents a low cut-off frequency in ON state, this is due to the switch resistance. The width of the switch transistors are set to 1m, this is the best compromise between switch resistance, occupied area and parasitic capacitance with the bulk.

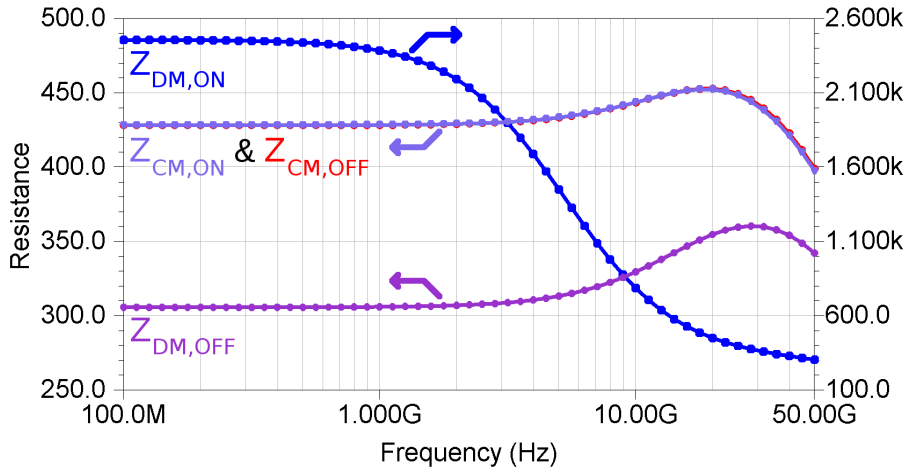


Figure 4.32: *S-Parameters of the compensation cell*

The CM impedances in both ON and OFF states are the same providing a lower feedback gain for CM oscillations. While the DM impedance depend on the state. So, adding several compensation cells to the DPA and controlling them according to the ACW can help to decrease the input impedance variation. The next point describes the implementation of this compensation cell with the DPA.

4.4.2.1.2 Implementation A compensation cell is added every two columns of the MSB matrix and is controlled by the column activation signal as can be seen in the DPA floor-plan in Figure 4.33. In this configuration, one additional compensation cell is enabled for every 512 envelope code word step. This implementation avoids the need of complex controlling scheme for the compensation cell. Moreover, the compensation cells are directly implemented in the dummy rings, which do not impact the total occupied area.

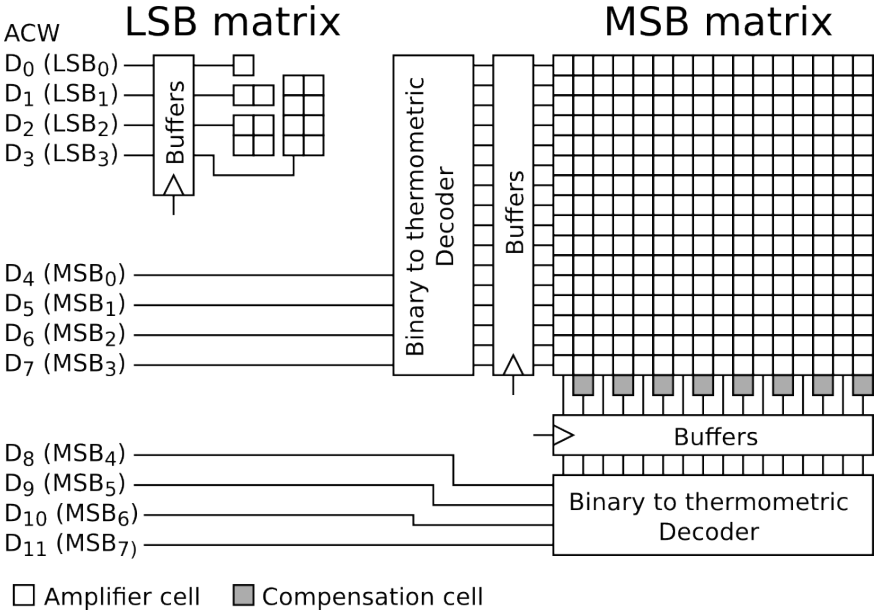


Figure 4.33: *Final DPA block diagram with compensation cell*

Figure 4.34 represents the number of compensation cell activated (N_{CC}) depending on the number of unit-cell activated in the MSB matrix of the DPA ($N_{cell\ ON}$).

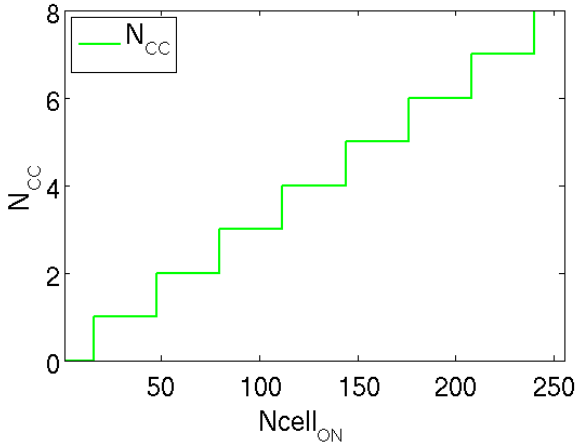


Figure 4.34: *Number of activated compensation cell*

4.4.2.1.3 Characterization Taking into account the compensation cells, the input impedance expression (4.1) becomes:

$$Z_{in} = (N_{ON} * Y_{ON} + N_{OFF} * Y_{OFF} + N_{CC\ ON} * Y_{CC\ ON} + N_{CC\ OFF} * Y_{CC\ OFF})^{-1} \quad (4.8)$$

With $N_{CC\ ON}$ and $N_{CC\ OFF}$ representing the number of compensation cells in ON and OFF state, and $Y_{CC\ ON}$ and $Y_{CC\ OFF}$ standing for the admittance presented by a compensation cell in ON and OFF states. Their differential resistive impedance variation is inversely proportional to the envelope code word, which compensates the one induced by the unit-amplifiers switching.

Figure 4.35 shows the Matlab model of the resistive input impedance variations as a function of the ACW based on DC operating points parameters. Adding the compensation cells limits the impedance variation to less than 6 Ω. The resistive impedance is always comprised between 13.8 Ω and 19.8 Ω. Furthermore, the compensation cells have low common mode impedance which stabilizes the DPA in common mode.

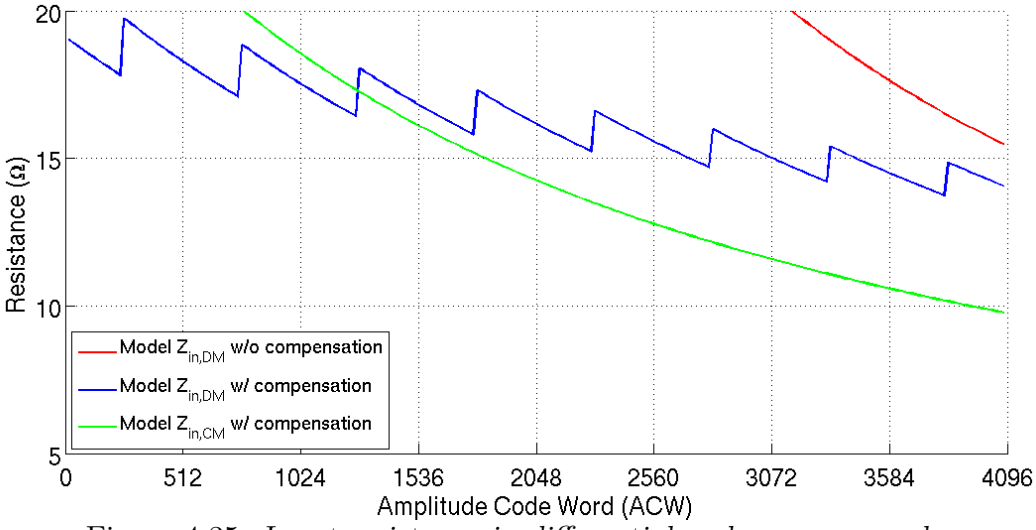


Figure 4.35: *Input resistance in differential and common mode*

Figure 4.36 shows the differential input impedance of one DPA against the ACW without and with compensation cells at 1 GHz. The capacitance variation is small as stated before and the compensation cell greatly reduces the resistive variation. In order to facilitate the reading, the smith chart is normalized to 20 Ω. The red curve represents the DPA input impedance without compensation resulting in high impedance variation. The blue curve represents the case with compensation cells which greatly reduce the impedance variation.

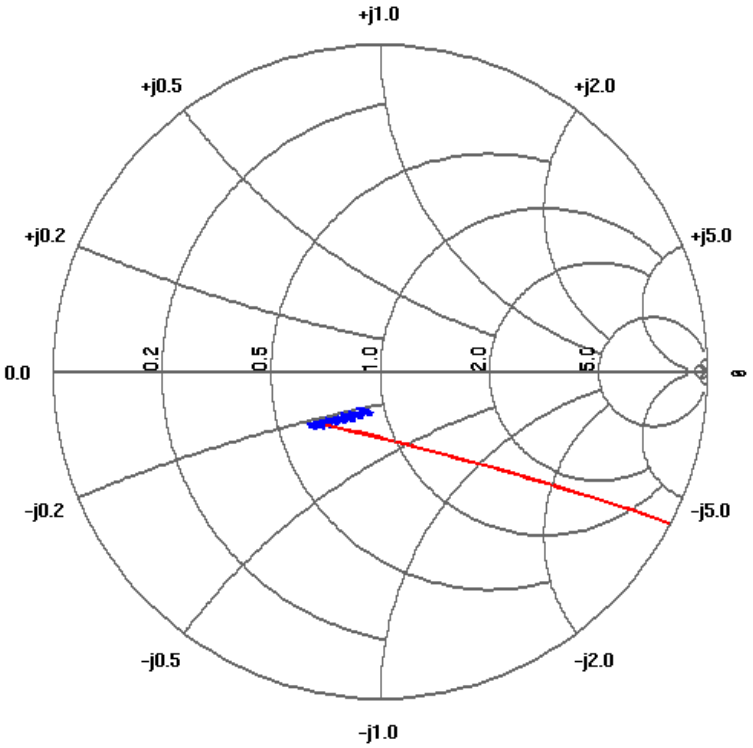


Figure 4.36: *Smith chart representation of the DM impedance variation versus ACW with (blue) and without (red) compensation cell normalized to 20 Ω*

Figure 4.37 shows the resistive part of the input impedance modeled with Matlab and extracted from SP simulation with and without the compensation cells for both the common and differential mode.

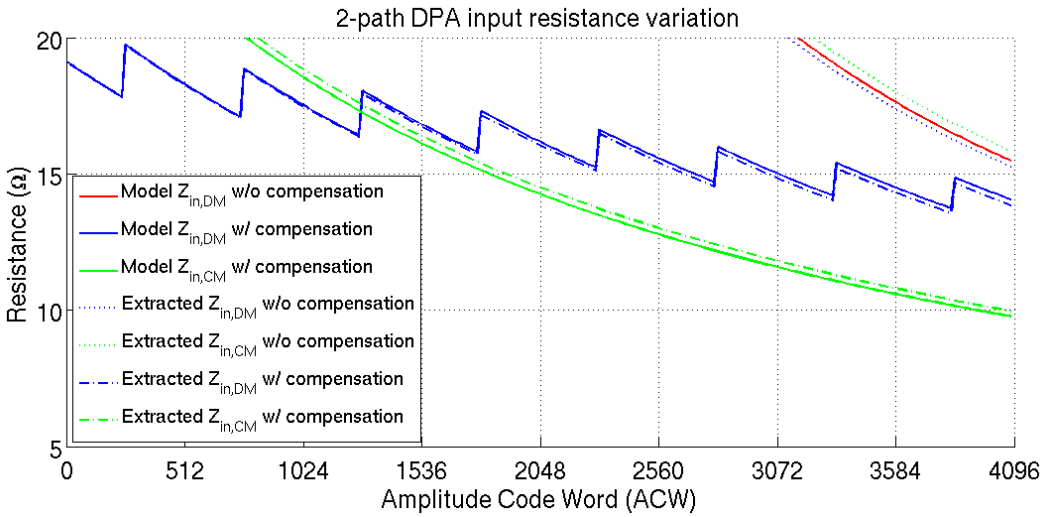


Figure 4.37: *Resistance variation against ACW*

The final transfer function of the open loop common mode is represented on Figure 4.38 and is compared to the cases with and without dummy load. The worst case is now at -4.5 dB at 2.1 GHz, what greatly stabilizes the system.

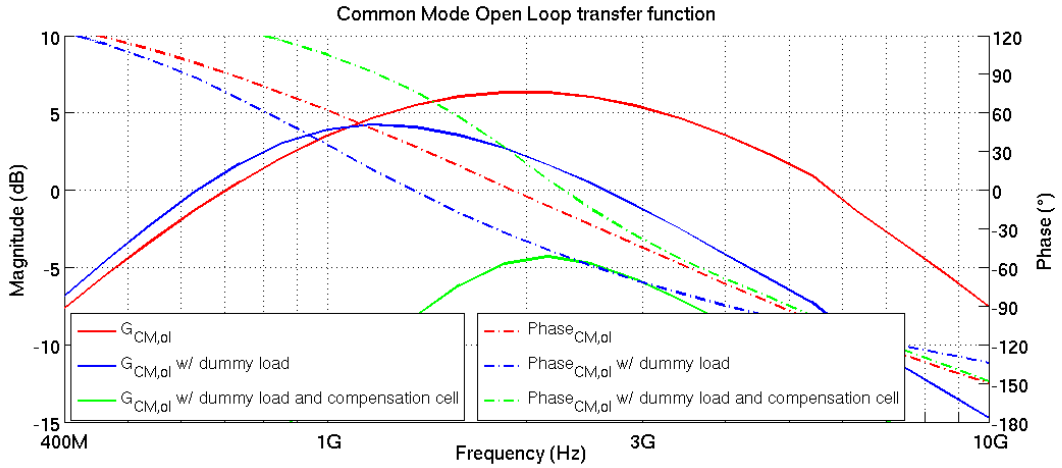


Figure 4.38: *Comparison of the open loop transfer function with and without the dummy load and compensation cell*

4.4.3 Enhanced stability

The dummy loads and compensation cells greatly help to stabilize the system. The news μ and μ' factors for both common and differential modes are plotted on Figure 4.39.

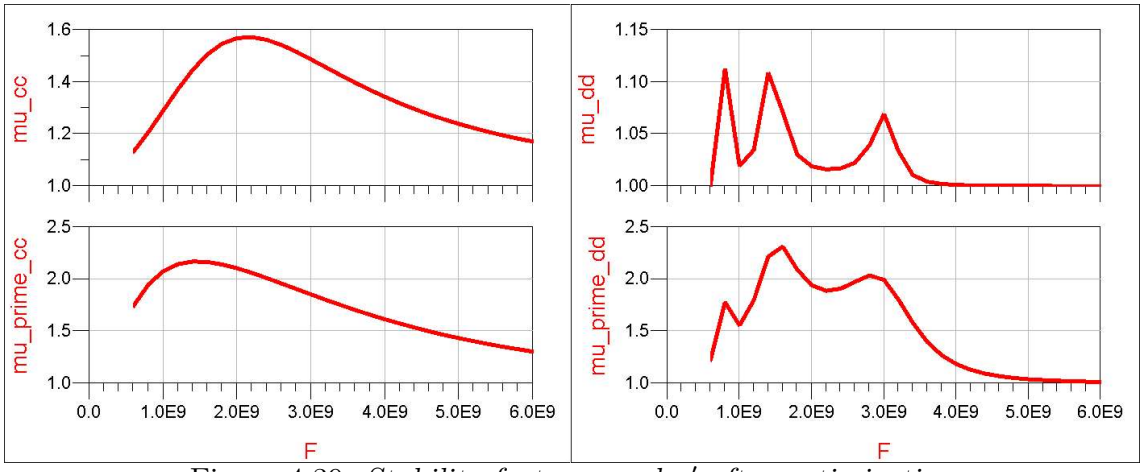


Figure 4.39: *Stability factor μ and μ' after optimization*

Both the common and differential modes are now stable. In fact, μ and μ' factors are well higher than 1 meaning that the source and load stability circles are outside the smith chart, which leads to an unconditionally stable system.

4.5 Final circuit architecture and layout

The overall implemented system PACO for "PA for COgnitive radio" is depicted on the simplified floor-plan presented on Figure 4.40. Figure 4.41 shows the final die micrograph. The total circuit occupies 1.04 mm^2 and the area dedicated to the DPA and control logic only occupies 0.25 mm^2.

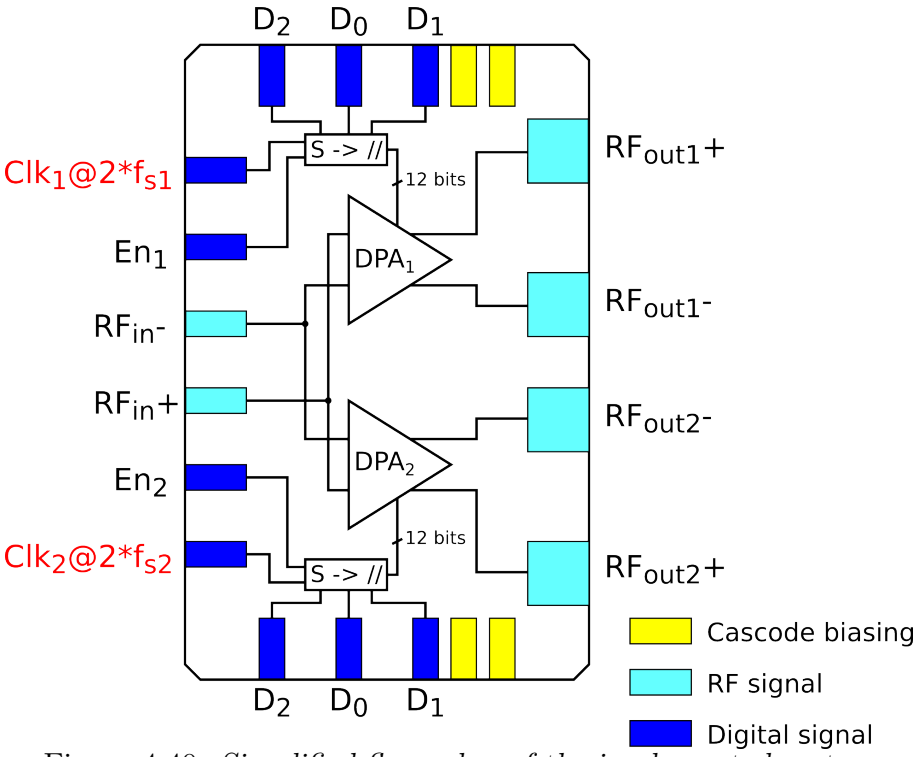


Figure 4.40: *Simplified floor-plan of the implemented system*

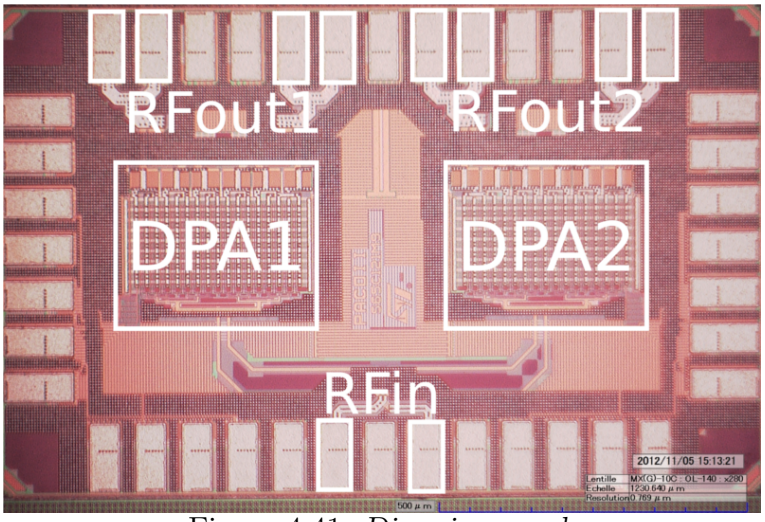


Figure 4.41: *Die micrograph*

4.6 Conclusion

A 2-path digital polar power amplifier implementation in 65nm CMOS process to cover 0.8 GHz - 3 GHz while offering 19 dBm output power per path was presented in this chapter. The 12-bit amplitude code words of the two paths are distinct allowing the use of different sample rates. Compensation cells were added in parallel of each DPA input in two purposes. First, they present a low common mode impedance helping in stabilizing the system by decreasing the common mode gain. Second, the compensation cells can be controlled to change the differential impedance presented in parallel to the DPA. Then, the large swing of the input impedance depending on the amplitude code word can be greatly reduced. This reduced range limits the distortions introduced by amplitude variations. The compensation cells were well studied from basic model up to extracted behavior in parallel to the DPA.

This 2-path CMOS DPA is intended to serve as digital envelope modulator (DEM) in a demonstrator based on the approach proposed in the previous chapter. Such multi-rate and mutli-path all-digital RF transmitter requires several functions beside the DEM. These other blocks are the digital baseband processing, phase modulation, matching network and power recombination and will be detailed in the next chapter, with special attention to the digital processing applied to the amplitude signal.

Chapter 5

2-path transmitter experimental setup

5.1 Introduction

The proposed transmitter architecture requires baseband processing and digital-to-RF modulators in order to manage the undesired images. Thus, the prototype requires external processing besides the implemented 2-path DPA CMOS circuit. This uncommon approach with polar and multi-path aspects implied special attention during the test-bench design. This chapter will detail the experimental setup. Section 5.2 will explain the equipments used to realize the global setup from the baseband generation to the spectral measurement. Then, the phase modulator will be detailed in Section 5.3. Section 5.4 will enlighten the SRC implementation in FPGA and explain the general mechanisms implemented. Finally, Section 5.5 will cover the design of the matching networks and power recombination performed on-board and with external combiners.

5.2 Global experimental setup

The implemented circuit detailed in the previous chapter will serve as a digital envelope modulator and power amplifier as illustrated on Figure 4.2. The test setup was done using the equipments of the Telecom Platform at IRCICA in order to perform the phase modulation and power measurements. The final block diagram of the test-bench setup is shown on Figure 5.1.

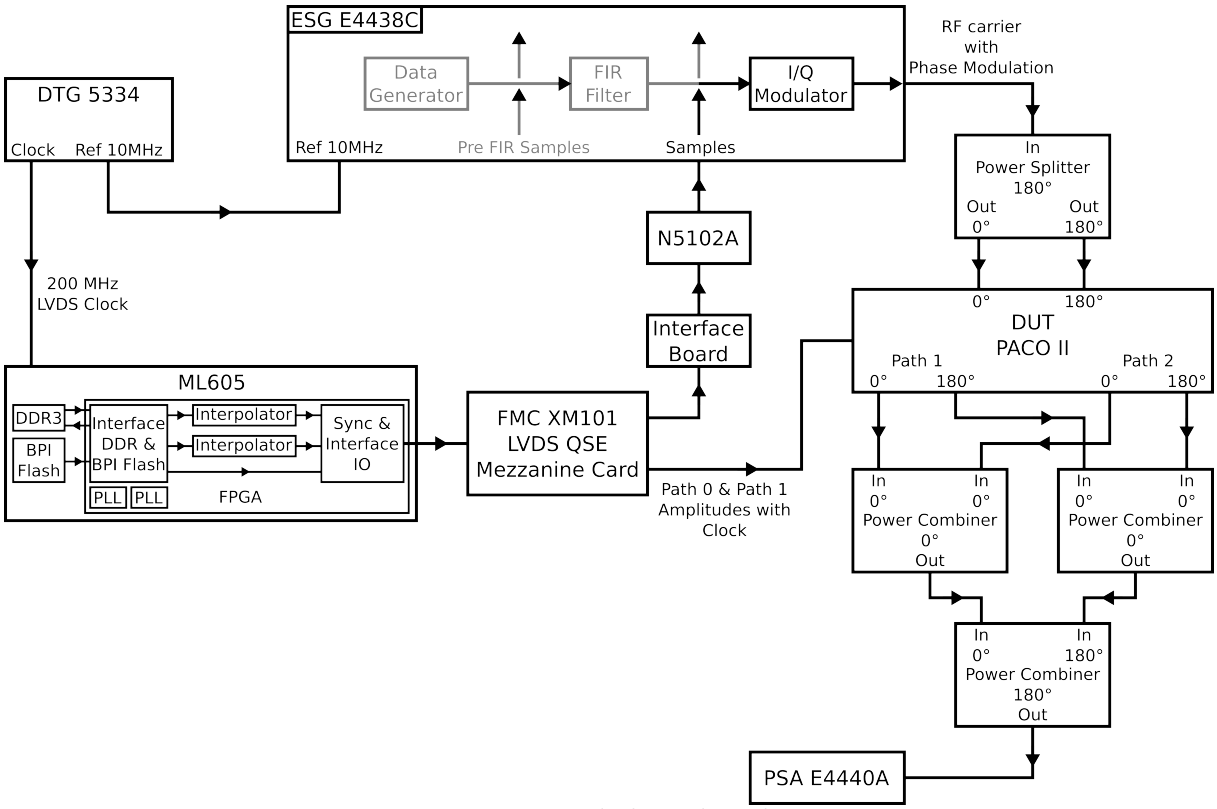


Figure 5.1: *Detailed testbench setup*

The DUT refers to the die mounted on the PCB with on-board matching networks. The baseband symbol generation and sample rate conversions are performed on a FPGA development board from Xilinx (ML605), which provides a Virtex6 FPGA with large amount of high speed IOs and DDR3 RAM.

The FPGA provides the amplitude code words to the DUT and drives the phase modulator implemented in the E4438C. The data generator and FIR filters were shunted and only the I/Q modulator was used to perform the phase modulation. Then, the single-ended RF signal is split into differential signals and drives the DUT RF phase inputs. Finally, the RF outputs of the DUT are recombined with external power combiner into a single-ended signal and observed on a spectrum analyzer.

Figure 5.2 shows the same testbench with illustrated equipment. The same component model is used for the 180° splitter and combiner, which is the 2-Way Power Divider ref. GF-T2-180-1000-3000 from A-INFOMW . The 0° combiners are the 50PD-659 SMA 2-way power divider model from JFW Industries Inc.

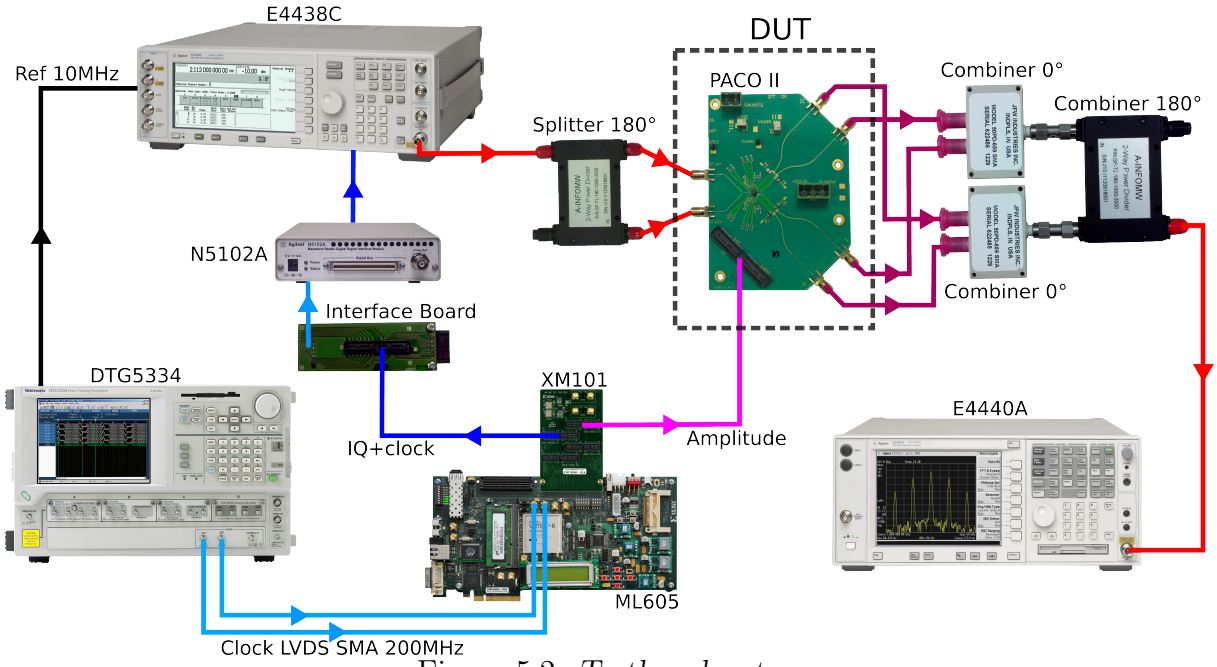


Figure 5.2: *Testbench setup*

5.3 External phase modulation

It was chosen to realize the phase modulation with a generic IQ modulator driven by a normalized 12-bit IQ signal at 100 MS/s, generated by the FPGA. The Vector Signal Generator ESG-4438C is used as the quadrature modulator. The internal baseband symbol generation, mapping and filtering are bypassed to allow direct control of the modulator. The anti-aliasing filters present a 40 MHz bandwidth which imply that complex modulation with up to 32 MHz channel bandwidth can be supported. In fact, the phase information bandwidth can be approximate to 2.5 times the complex modulation one. The N5102A module on Figure 5.1 is used to interface the FPGA data stream with the ESG. Figure 5.3 illustrates the final configuration of the ESG and FPGA.

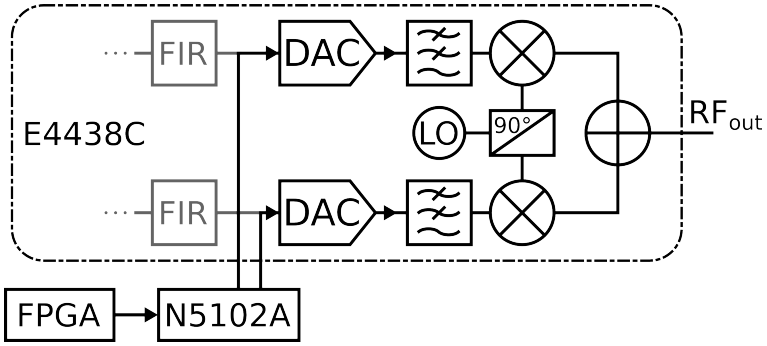


Figure 5.3: *Phase modulation with quadrature modulator*

The output port RF_{out} is a single-ended port, thus a 180° power splitter is used to provide differential signal to the DUT board. The power splitter covers only a 1 to 3 GHz band compared to the 0.8 - 3 GHz bandwidth of the DUT. However, the power splitter is still functional down to 0.9 GHz with less than 0.5 dB deviation.

5.4 Interpolator implementation on FPGA

During the simulations, the ACWs with different sample rates were generated by raw interpolation with rational ratio as represented on Figure 3.13. The need of high frequency FIR filters after up-conversion and dedicated up and down conversion ratios for each path greatly limits its implementation on FPGA. One way to overcome this limitation is to use Lagrange interpolation based on Farrow implementation [79] as demonstrated in [80]. As explained in [81, 82], the interpolated output samples are represented by

$$y(kT_i) = \sum_{i=I_1}^{I_2} x[(m_k - i)T_s]h_I[(i + \mu_k)T_s] \tag{5.1}$$

Where T_s and T_i are the input sample period and the interpolated (output) one, respectively.

$h_I(t)$ stands for the impulse response of the interpolating filter, while m_k, μ_k and i denote the base point index, the fractional interval and the filter index as represented on Figure 5.4. I_1 and I_2 define the boundaries of the FIR composed of $I_2 - I_1 + 1$ taps.

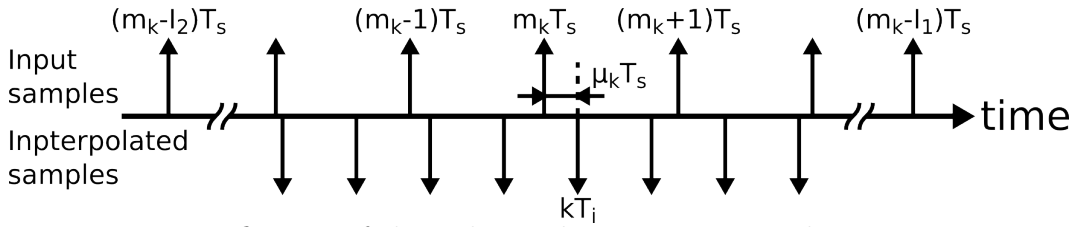


Figure 5.4: *Definition of the indexing between input and output sequence*

The use of piecewise polynomial to describe the impulse response

$$h_I[(i + \mu_k)T_s] = \sum_{l=0}^{N} b_l(i)\mu_k^l \tag{5.2}$$

leads to rewrite Equation (5.1) as

$$y(k) = \sum_{l=0}^{N} \mu_k^l v(l) \tag{5.3}$$

with $v(l) = \sum_{i=I_1}^{I_2} b_l(i)x(m_k - i)$

$v(l)$ are the Farrow vectors and $b_l(i)$ the Farrow coefficients of the polynomial interpolator derived from Lagrange formulas.

The Farrow structure represented by Equation (5.3) is composed of two parts with different time domains. First, the vectors $v(l)$ are fixed FIR filters clocked at the input sample

rate T_s. Second, the fractional interval μ_k refreshes at the interpolated rate T_i which can be easily tuned. In this case, no multipes of the initial sample rate are needed, and a different interpolated sample rate only requires to modify the μ_k generation. The Farrow vectors can be shared between several interpolators. This aspect is used into the FPGA to optimize the synchronization between paths and to lower the allocated resources. Two main constraints must be taken into account during the design of the Farrow structures. First, the clock domain crossing between the Farrow vectors and the polynomial vector μ_k is sensitive to clock jitter. FIFOs with different input and output sample rates were used to switch from clock domains. Second, the recombination of Farrow vectors requires the generation of μ_k to be well aligned with the reference (input) clock. A simple implementation of μ_k generator is depicted on Figure 5.5. The frequency code word (FCW) sets the accumulator step $\Delta\mu$ providing the μ_k coefficient and the PLL generating the interpolated clock.

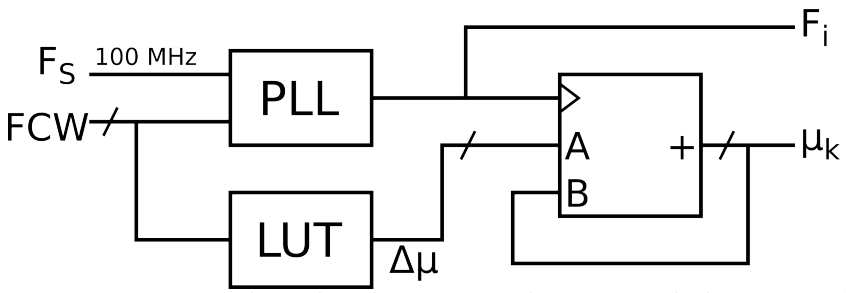


Figure 5.5: *Basic generator based on PLL providing μ_k and the interpolated clock*

Images attenuation by cubic interpolation with 12-bit output resolution is sufficient when working with signal oversampled by at least a factor of 3. In our case, the input symbol rate is fixed to 100 MHz due to RAM speed limitation. So, the residual images after interpolation are lower than the quantization noise floor. Moreover, the supported output sample rate covers 100 MHz to 350 MHz, and the number of interpolated sample rate and so $\Delta\mu$ depends on the μ_k resolution. The implemented Farrow structure with cubic interpolation is represented on Figure 5.6. The logic in the input clock domain before the FIFO is common to both polynomial filters used to generate the two ACWs.

Besides performing the sample rate conversion of the amplitude signal, the FPGA also generates the phase signal with normalized IQ format and ensure synchronization between the phase and envelope paths. The symbol generation is performed by reading data from a file. To do so, the FPGA load the data from the slow Flash memory to the high speed DDR3 RAM. Then, the logic core reads the DDR3 and generates a 100 MHz data stream with IQ and envelope informations. Next, the data stream drives the Farrow structure to interpolate the two ACWs based on interpolated clocks and Farrow coefficients. The syn-

chronization between the IQ signals representing the phase information and both ACWs is done in two steps. First, the IQ signals are delayed with 100 MHz flip-flops to meet the latency of the Farrow vectors. Second, the IQ and ACWs signals are delayed in correlation with the conversion ratios. Perfect synchronization cannot be achieved, but the delays can be set low enough to avoid spectral regrowth.

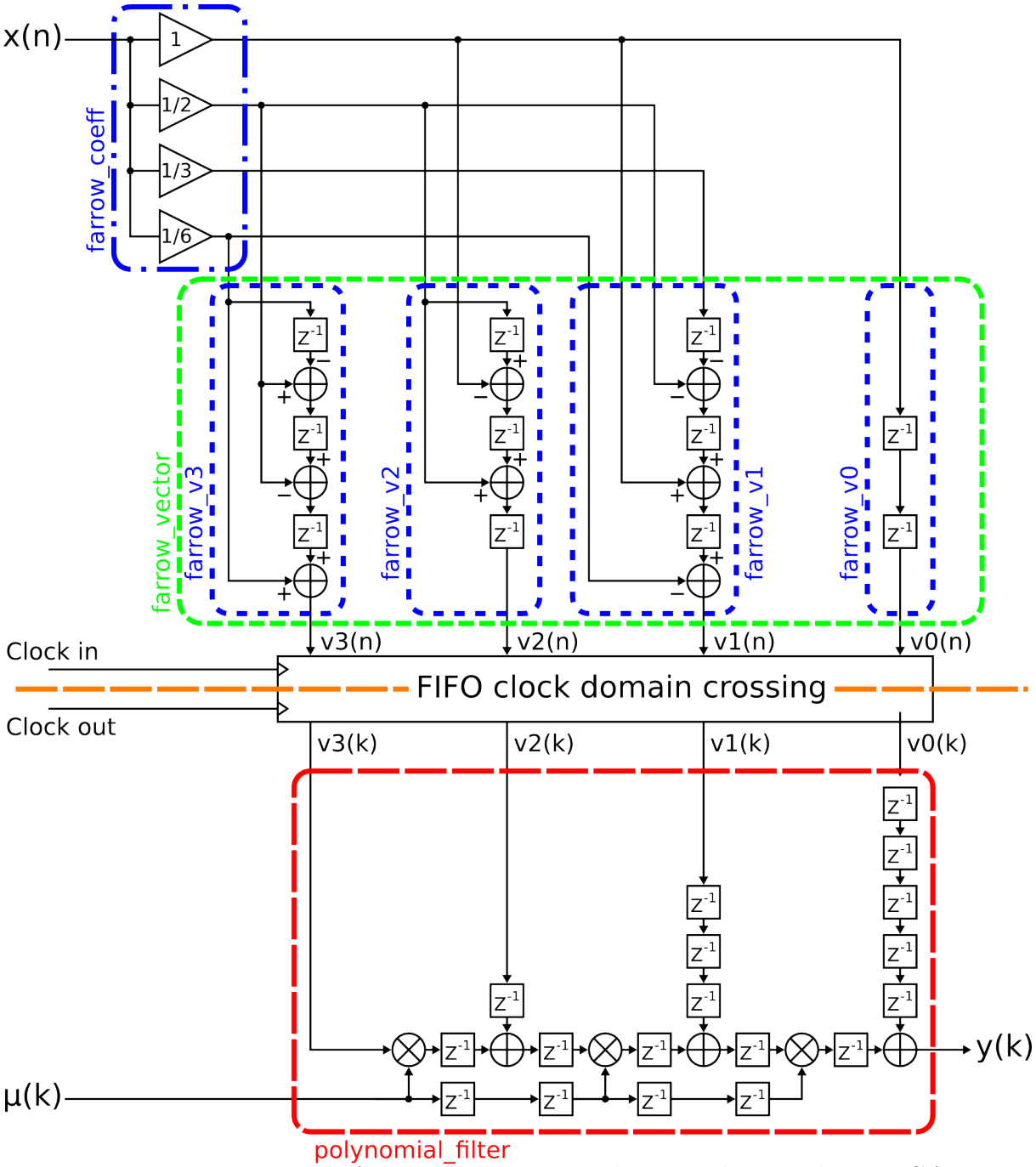


Figure 5.6: *Diagram of the Lagrange interpolator implemented on FPGA*

The FPGA outputs use a fixed logic voltage level of 2.5 V with a 50 Ω load. The signals are divided by two in order to be compatible with the 1.2 V inputs of the die.

5.5 On-board Matching Network and off-board recombination

The 2-path architecture requires power recombination as part of the images suppression process. This section will focus on the design of the matching network implemented on-board and the power recombination performed with external components. The first point to be detailed will be the impedance matchings performed at the output of the two DPAs and the use of external components to recombine the paths. Then, the impedance matching done on the input side of the integrated circuit will be discussed in the last point.

5.5.1 2-way differential to single-ended output circuits

On-chip integration of transformers as 2-way differential to single-ended balun was initially planned and studied. The idea was to perform wide-band recombination by merging the output parasitic capacitances of the DPAs with the transformer as the first matching network step as explained in [11]. However, the implemented circuit does not integrate any impedance matching or output biasing due to area limitations. Thus, the 2-way recombination is performed in two external steps. First, the impedance matching over the 0.8 - 3 GHz band is ensured by an on-board matching network. The differential outputs of the DPAs are both matched to 50 Ω. Second, a set of external power combiners is used to convert the two differential paths into a single-ended port as already depicted on Figure 5.1. The matching networks were designed with ADS in order to model the wire-bonding and the substrate effects. The wire-bonding configuration of one DPA output is presented on Figure 5.7. Two wire-bonds are used for RF signals in order to reduce the inductance value associated with the wires. The wires are not exactly parallel due to some minimum isolation constraints, but were modeled with the same direction. The model takes into account the mutual coupling by working with a set of seven contiguous wires used for RF signals, grounds and power supply. The wires can be classified in three main types depending on their length and purpose. The shorter wires are dedicated to ground connection, the medium length wires are used by power supplies (V_{DD}, V_{Casc} and V_{2V5}) and the longest wires are dedicated either to RF or digital signals.

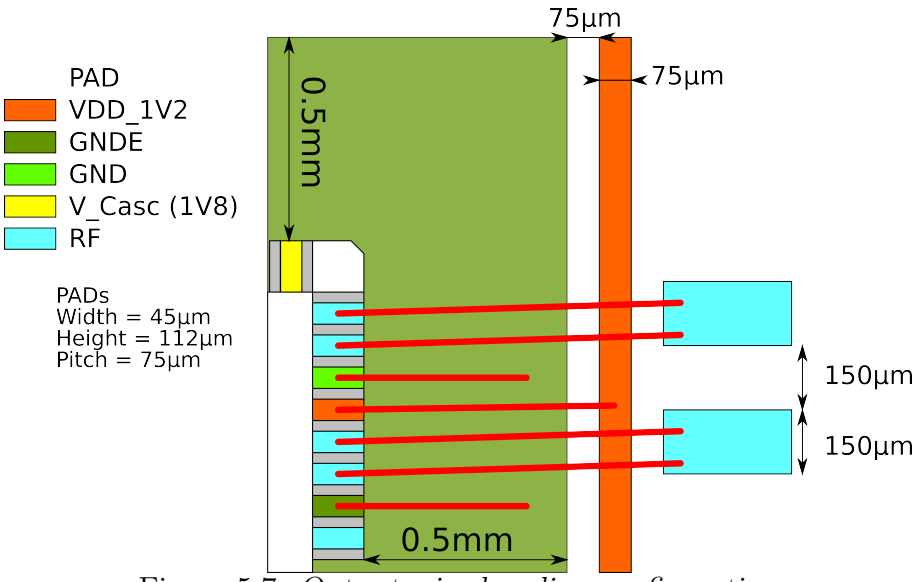


Figure 5.7: *Output wire bonding configuration*

The resulting inductance and resistance of alloyed aluminum wires with 12.5 μm radius are listed in Table 5.1. The self inductances are constant over the 0.8 - 3GHz band, and the serial resistance is negligible against PA output impedance despite their variation up to 66% for GND case. Moreover, the use of two wires in parallel for the RF signals helps to decrease the wire self inductance from 660 pH to 480 pH, keeping in mind that the mutual inductance (around 300 pH) prevent to reach the hypothetical 330 pH.

Table 5.1: *Simulated characteristics of the wires*

Wire type	Self Inductance (pH)	Serial Resistance (Ω) 1GHz ; 3GHz
Signal	660	0.225 ; 0.375
Power	580	0.2 ; 0.325
GND	470	0.15 ; 0.3

The models of the wire bondings, as depicted in Figure 5.7, are used to design the matching network to match the extracted impedance of the DPA to a 50 Ω load. This is done by an optimization process tuning several parameters such as discrete L and C; dielectric and conductor thickness; width and length of microstrip lines. The placement constraints motivated the use of long lines.

During the optimization process, it appeared that conductor and dielectric thickness had an important impact at the interface of the wire and the trace. This resulted in a thick conductor layer (35 μm) and a thin dielectric (100 μm with $\epsilon_r = 3.66$).

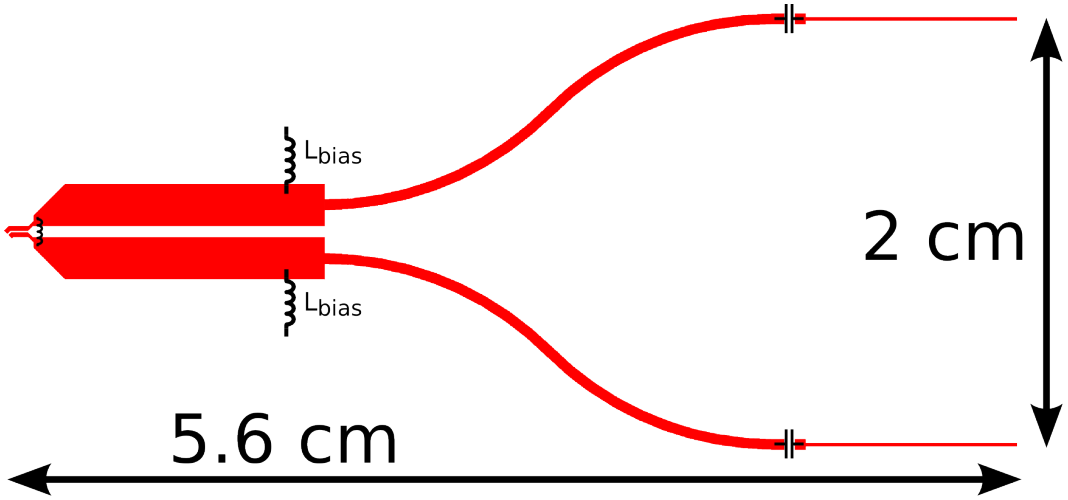


Figure 5.8: *Output matching network layout*

The final layout for one path is depicted on Figure 5.8, while Figure 5.9 shows the transfer characteristics between the differential output to a 100 Ω differential load. The characterization was performed using a 4-port setup and converting the natural 4-port S-matrix to the mixed-mode one as defined by Equation (5.4) and Equation (5.5).

$$\begin{bmatrix} b_{dm1} \\ b_{dm2} \\ b_{cm1} \\ b_{cm2} \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix} \begin{bmatrix} a_{dm1} \\ a_{dm2} \\ a_{cm1} \\ a_{cm2} \end{bmatrix} \tag{5.4}$$

$$S_m = M * S_n * M^{-1} \tag{5.5}$$

with S_n the natural S-parameters, S_m the mixed-mode S-parameters and M the transform matrix defined by:

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \tag{5.6}$$

The difficulty was to ensure 10 dB return loss over the 0.8 - 3 GHz band. In fact, the return loss presents a degradation around 2.3 GHz at -8.4 dB. The forward transmission is maximum at 1.7 GHz with -2.9 dB and the band limits are defined at 0.8 GHz and 2.75 GHz with a -4 dB value.

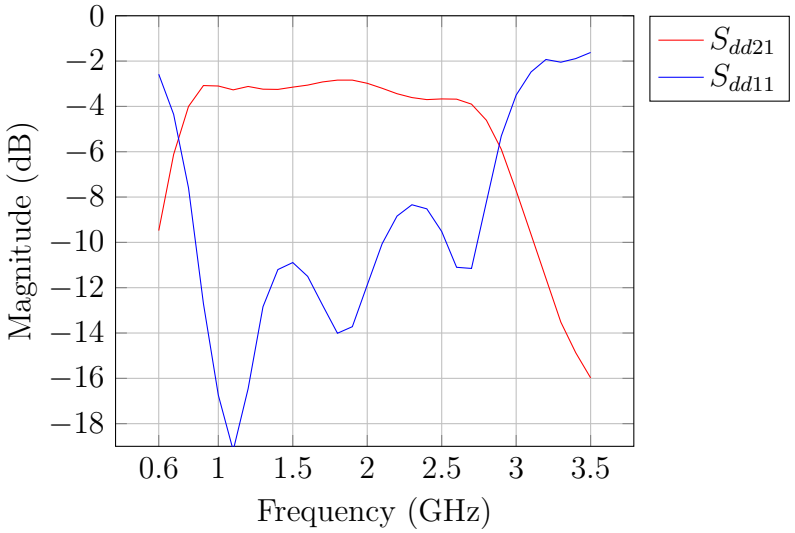


Figure 5.9: *Characteristics of the output matching network*

The 50 Ω output ports of the matching networks are then connected to the external power combiners. Several configurations could have been implemented to recombine the two differential paths. Finding commercial wideband power combiners appeared challenging, what influenced the choice of the configuration. Figure 5.10 illustrates the selected configuration. A 0° combiner is used to recombine the positive outputs of each paths while another 0° combiner recombines the negative outputs. The resulting combined signals are then recombined by a 180° combiner. The final transfer function of the cascaded combiners after characterization is shown on Figure 5.11. The insertion losses are comprised between 0.5 and 1 dB on the 0.6 - 3 GHz band. The 0° combiners models is 50PD-659 SMA from JFW Industries Inc. The 180° combiner is the GF-T2-180-1000-3000 model from A-INFOMW.

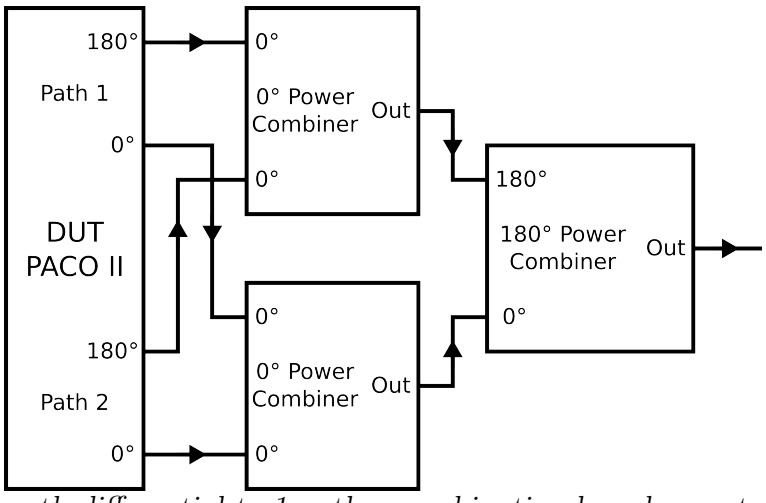


Figure 5.10: *2-path differential to 1-path recombination based on external combiners*

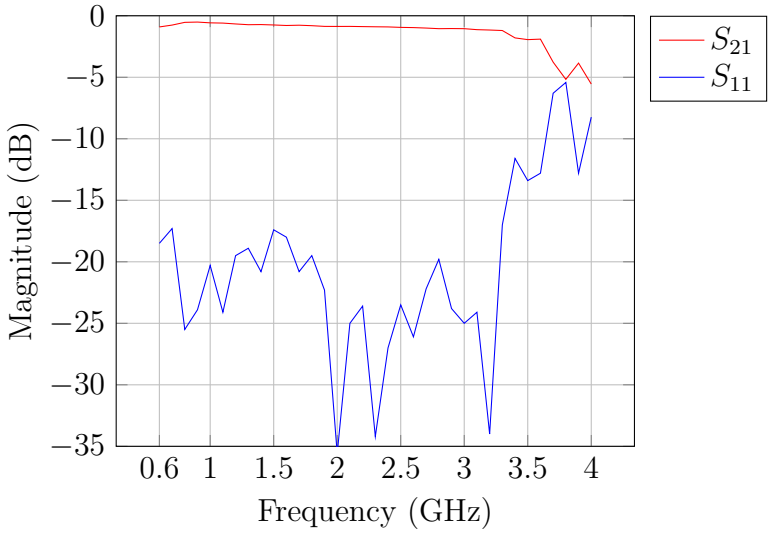


Figure 5.11: *Transfer function of the external power combiner*

5.5.2 Single-ended to differential input circuit

A 180° splitter is used to convert the single-ended signal from the 50 Ω port of the phase modulator to two signals with 180° phase-shift and matched to 50 Ω. The matching is performed on-board and the same methodology as for the outputs ports was used to design the input matching network. The wire-bonding configuration is slightly different as represented on Figure 5.12. Only one wire is used on each RF signals. The matching network needs to match the two 50 Ω input ports to the two pads loaded by the input impedance of the two DPAs, which is 16.25 Ω in parallel with 5.8 pF. The resulting layout is depicted on Figure 5.13 and the transfer function is represented on Figure 5.14.

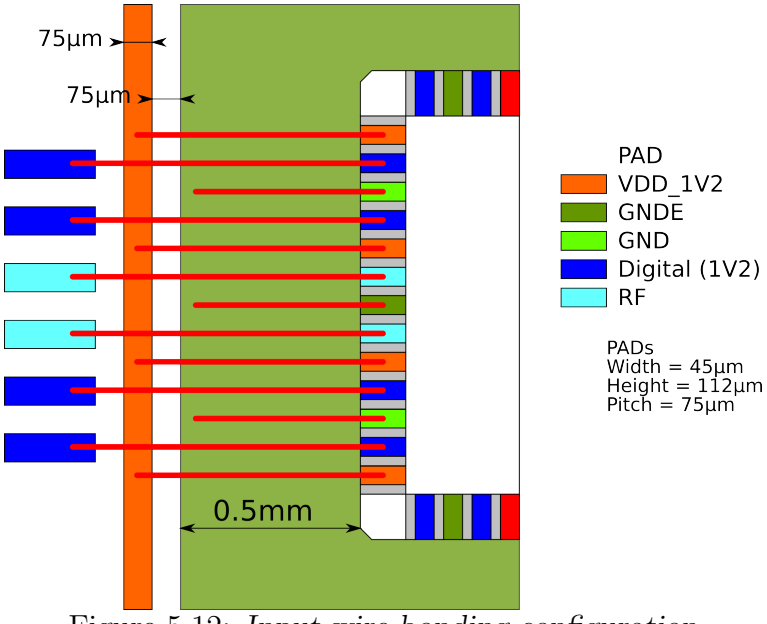


Figure 5.12: *Input wire bonding configuration*

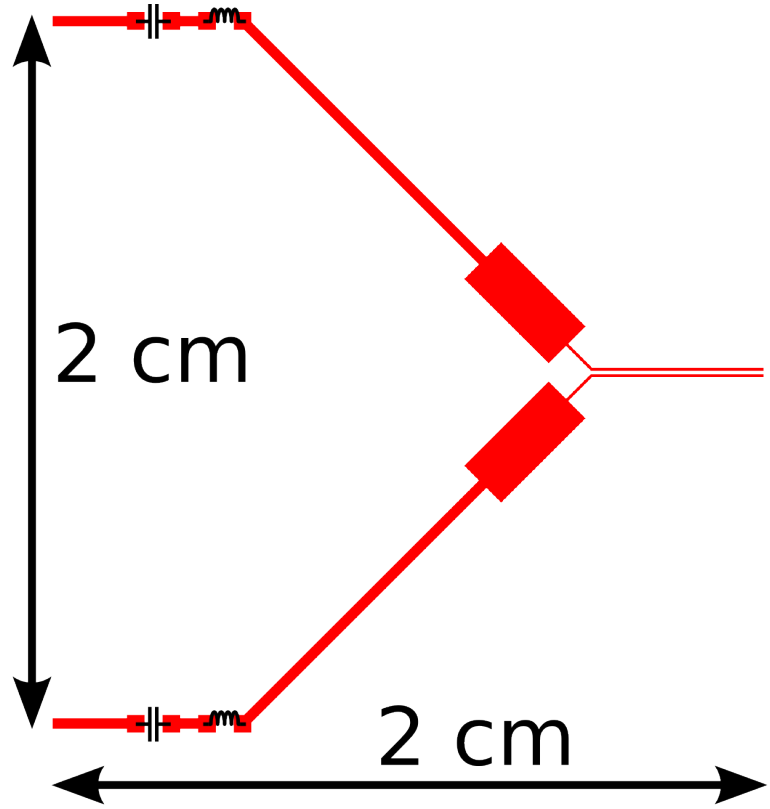


Figure 5.13: *Input matching network layout*

The input matching network suffers from the same return loss degradation than the output network. The return loss presents a -8 dB peak at 2.3 GHz and the forward transmission is higher than -2 dB up to 2.95 GHz.

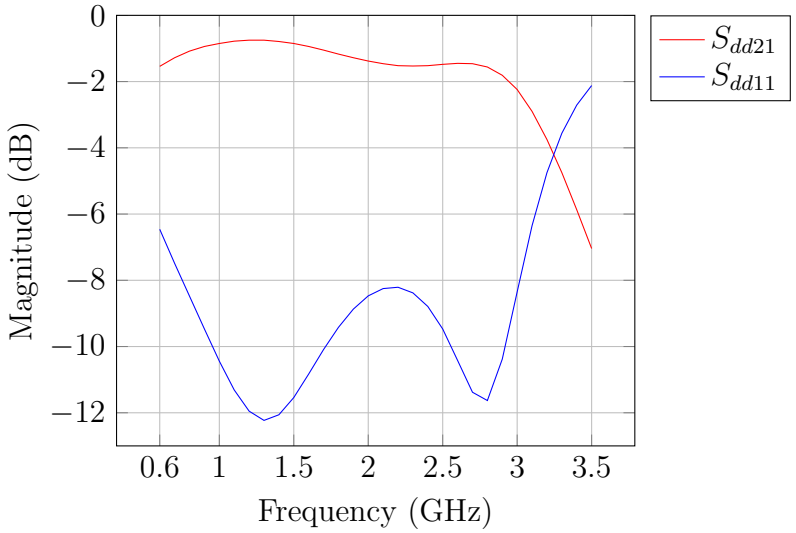


Figure 5.14: *Characteristics of the input matching network*

5.6 Conclusion

The final test board with on-board matching is depicted on Figure 5.15. The connectors of the power supplies (V_{supply}, V_{DD1V2} and $BiasOut$) and the digital signals are placed on the top face. The SMA connectors are edge mounted in order to facilitate the connection of the cables to the external components.

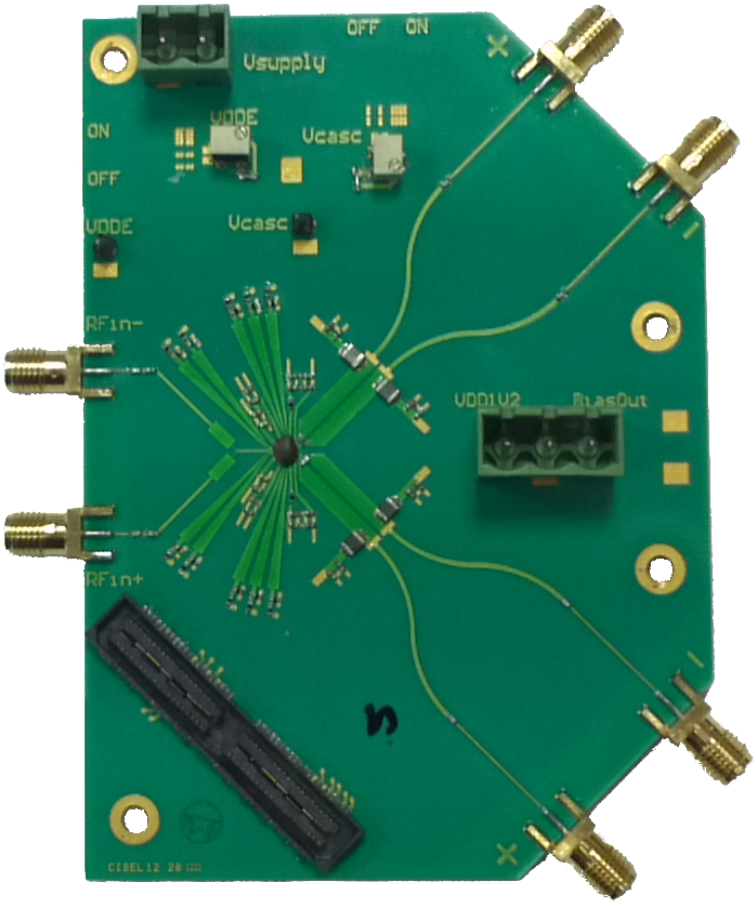


Figure 5.15: *Final board with matching networks and die*

The experimentation setup detailed in this chapter shows the complexity to implement the proposed multi-rate architecture based on an all-digital polar transmitter. In this configuration, the phase modulation is easily achieved by a quadrature modulator as it would be done in the case of a fully integrated system. The interpolator architecture used to implement the sample rate conversions in FPGA is similar to the architecture that would be integrated on-chip with the DPA. However, the impedance matching and power recombination were performed with discrete components and are well different than how it would be implemented on the same die as the DPA. The matching networks designed on PCB is highly dependent of the board and bonding variability, this aspect must be kept in mind when analyzing the measurement results presented in the next chapter.

Chapter 6

Measurement results

6.1 Introduction

This chapter will describe the measurements results of the experimentation setup introduced in the previous chapter. Five dies were mounted for test, but for one of the dies a short circuit on the supply lines appeared after a short time of operation. Before evaluating the performances of the multi-rate architecture with different configurations of the sample rates, the DPA itself is characterized by its digital to RF conversion and RF characteristics. Then, the setup will be used with complex modulation schemes in order to validate the ability to manage the undesired images.

6.2 DPA characterization

The DPA is a complex component performing the digital envelope modulation of a phase modulated RF carrier. Thus, the DPA presents two different behaviors. First, the digital to RF conversion which can be defined by the same performances than for a typical DAC. Second, the amplifier part of the DPA which can be characterized in the same way than for a PA. This section will describe both aspects. However, the first parameter to be verified is the communication between the FPGA IOs and the DPA. The FPGA IOs support DDR signals clocked up to 700 MHz resulting in 350 MS/s data rate. On the other side, based on extracted simulations, the deserializer logic supports data rates up to 500 MS/s. However, the tests show that the communication can only go up to 160 MS/s. Table 6.1 lists the sample rates supported in the DPA test setup and the interpolator coefficient step $\Delta\mu$. After inspection of the connexions, the signals are largely coupled with the clock. This is due to the use of a cable dedicated to LVDS signals in which the clock is close to the ACW signals. The addition of a delay in the FPGA did not help to increase the maximum clock rate.

Table 6.1: *Supported sample rates*

Sample rate (MS/s)	Clock DDR (MHz)	$\Delta\mu$ (10-bit)
100	200	0
133	266	768
152	304	672
160	320	640

6.2.1 Data converter characterization

Using the determined supported sample rates, the conversion aspect of the DPA was characterized. Figure 6.1 shows the notation used to define the measured values. I_{supply} stands for the current drawn by the whole die from the 1.2 V supply noted V_{DD}. This includes the deserializers, the matrix controllers and drivers, the compensation cells and the first amplifier stage of the unit-amplifier cells. I_{bias} denotes the total current drawn from output ports of both DPAs. Finally, V_G is the gate bias voltage of the RF inputs of the DPAs set by the self-biased first stage of unit amplifier cells and cross-coupled compensation cells.

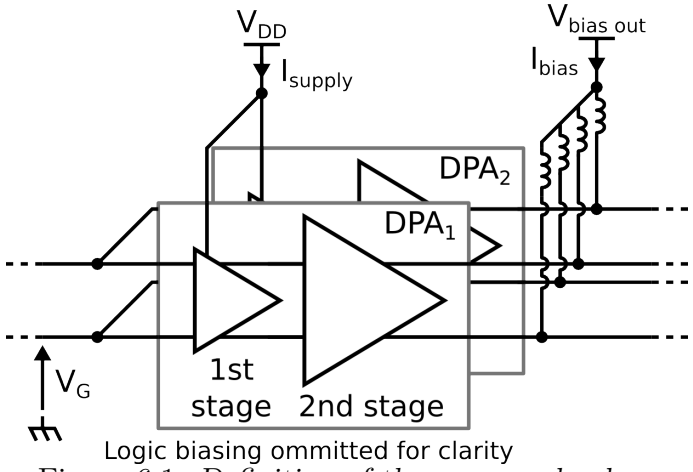


Figure 6.1: *Definition of the measured values*

The evolution of I_{bias} when the two DPAs are controlled by the same ACW is plotted on Figure 6.2. Due to the large number of codes, only the 4 MSBs are sweeped. The curve shows a slight distortion for the higher codes. This effect can be explained by the increase in temperature due to dissipation in the output stage. Extrapolated from the measurements, the biasing current of one cell of the MSB matrix is equivalent to 375 μA. The maximum amplitude code word corresponding to all cells activated in both DPAs implies a DC current of 186.4 mA. A discrepancy appears when these values are compared to the theoretical 718.6 μA consumed by one MSB cell and the total 368.6 mA of the DPAs. This discrepancy is explained in the next paragraphs.

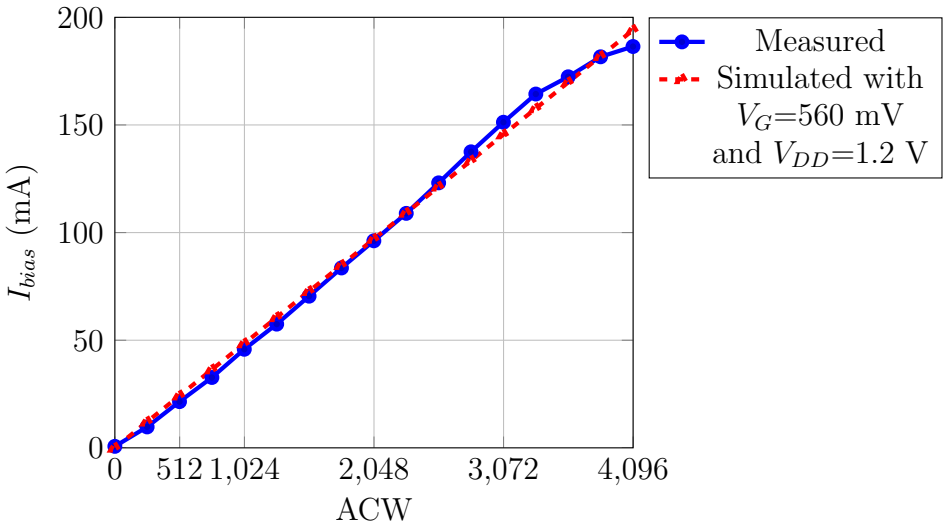


Figure 6.2: *DC current at the output against ACW*

By inspecting the input port of the die, it appears that the measured V_G is 562 mV instead of the theoretical 549.5 mV. To understand the impact of this 10 mV shift on I_{bias}, the unit-amplifier was simulated while forcing the input biasing point V_G of the first stage. The results are depicted on Figure 6.3. The DC current of the output stage is 718.5 μA for 549.5 mV input biasing and is equal to 378.5 μA when the gate voltage is forced to 562.5 mV. This value is close to the measured one. Table 6.2 summarizes the targeted,

measured and simulated current drawn by the output stage of one cell of the MSB matrix and of both DPAs with all the cells activated.

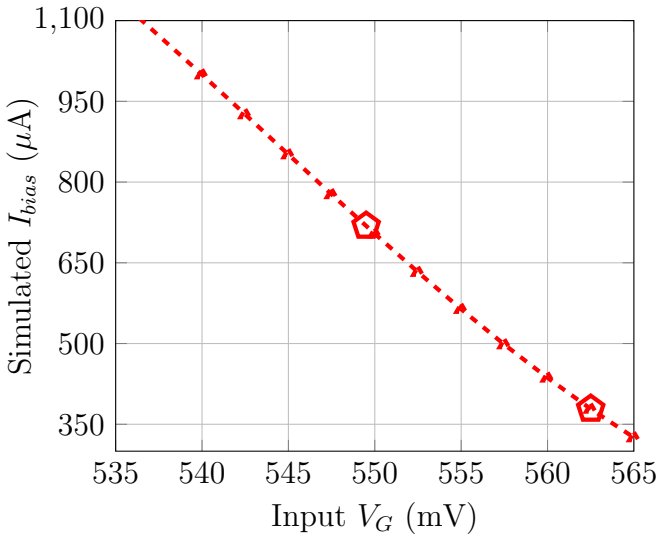


Figure 6.3: *Simulated impact of the input biasing variation on the output current of a unit-amplifier of the MSB matrix*

Table 6.2: *Current drawn by the output stage*

I_{bias}	Targeted (V_G=549.5 mV)	Measured	Simulated (V_G=562.5 mV)
1 cell of the MSB matrix	718.6 μA	375 μA	378.5 μA
2 DPAs with full ACW	368.6 mA	186.4 mA	194 mA

The first stage of each cell is self-biased and the compensation cells connected to the RF ports force the DC point to the same 549.5 mV. No voltage references were implemented on the die and no DC path for on-board biasing was anticipated. The only parameter was the 1.2 V power supply used to supply both logic and first stage of the unit cells. However, the tuning range is limited to the interval from 1.1 V to 1.3 V and has a lower impact to the current of the output stage significantly enough as represented on Figure 6.4. Thus, the supply was kept to 1.2V for next measurements.

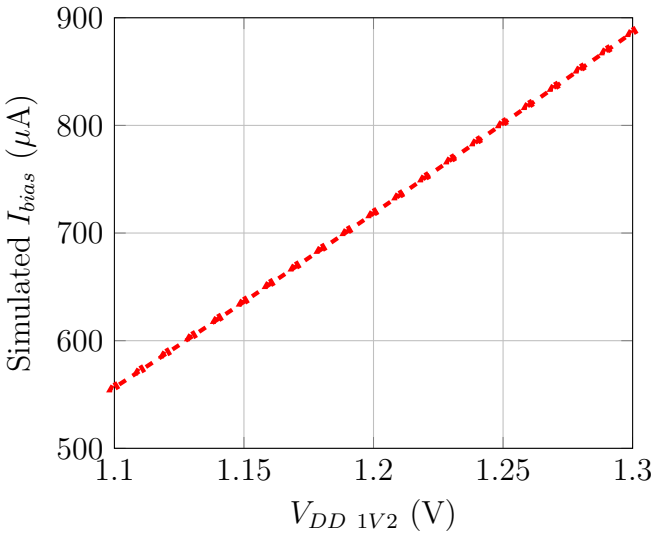


Figure 6.4: *Simulated impact of the 1.2 V power supply on the biasing current of a unit-amplifier of the MSB matrix*

The current drawn from the 1.2 V supply depending on the ACW is depicted on Figure 6.5. When all cells are off, the die consumes 5 mA which is the static power consumption of the logic, the matrix drivers and more importantly the compensation cells. This value meets the expected 5.10 mA current consumption of the 16 compensation cells (8 per DPA) consuming 319 μA each.

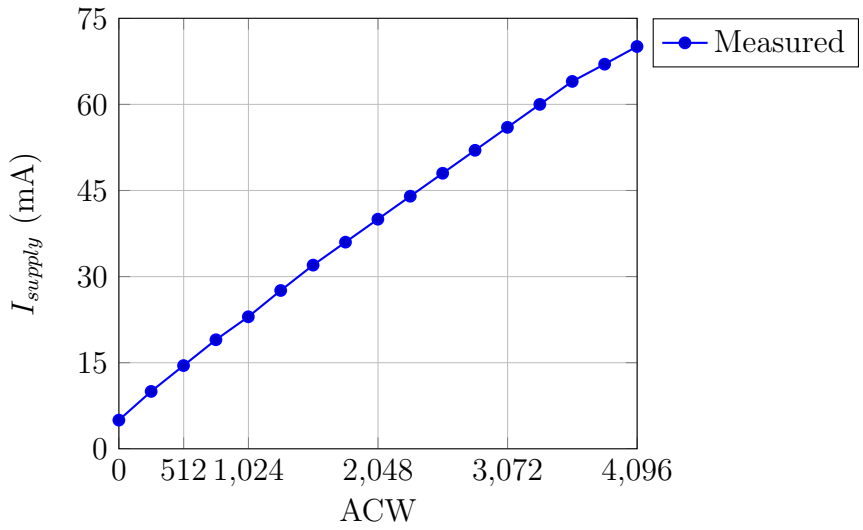


Figure 6.5: *Total DC current of the 1.2 V supply against ACW*

6.2.2 Power Amplifier characterization

The second part of the DPAs characterization focuses on the amplification aspect. The DPAs must cover a wide frequency band, and as explained in Chapter 4.1, the gain can vary over this band. The first measurement, shown on Figure 6.6, is the power characterization of the DPAs. The measurement was performed by stimulating the DUT with a single-tone signal at 1.1 GHz and setting the ACWs to the maximum value. The plotted values are de-embedded results, taking into account the input and output losses due to the matching networks and external components. The 1 dB compression point reaches 16.7 dBm for a -9.8 dBm input power. The gain in the linear region is 27.3 dB.

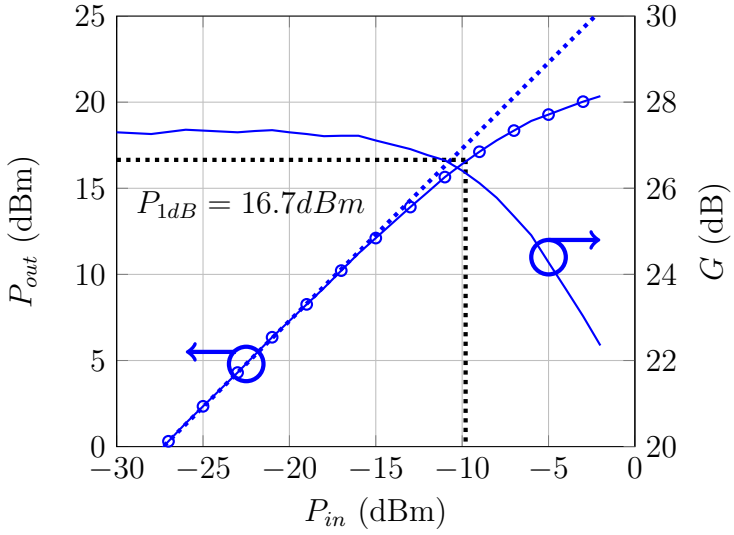


Figure 6.6: *De-embedded P_{out} and gain vs P_{in} for a 1.1 GHz sine wave input and ACW_{max}*

Figure 6.7 represents the output 1 dB compression point and PAE over frequency after de-embedding of the on-board matching network and off-board power combiner for a single-tone signal, when both paths are enabled and set to the maximum ACW.

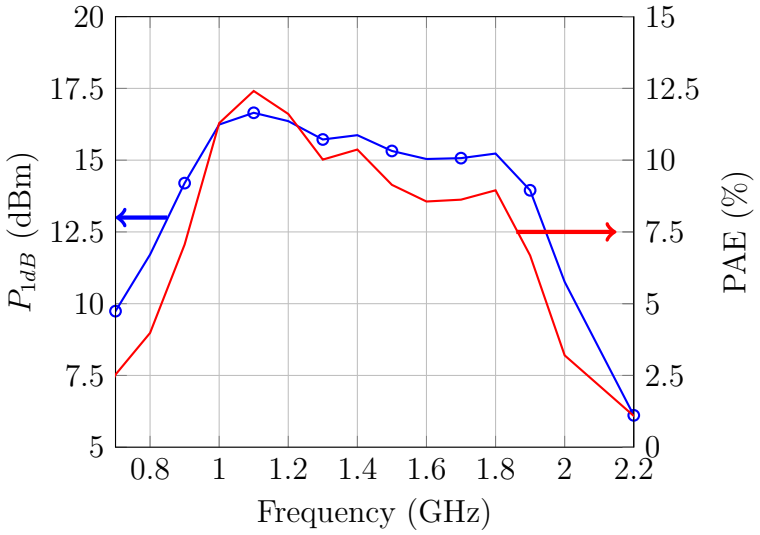


Figure 6.7: *De-embedded P_{1dB} and PAE over frequency for one-tone input with both DPAs set to the maximum ACW*

The maximum output power is obtained at 1.1 GHz and is equal to 16.7 dBm with a maximum PAE of 12.4%. The circuit draws 130.2 mA from the 2.5 V supply and 39.3 mA from the 1.2V supply. The logic interfaces and matrix buffers draw less than 5 mA from the 1.2 V supply. The amplifier was designed to cover a frequency band from 0.8 to 3 GHz. However, the useful frequency range is limited by the on-board matching network to 0.9 - 1.9 GHz. The two paths DPA will now be characterized with a basic QAM modulation. The aim is to ensure that the polar form based on digital envelope modulator is able to reconstruct the original signal. In this context, a 64-QAM modulation was chosen because it provides a large set of amplitude and phase combinations. The data rate was set to 10 MSymbol/s in order to be coherent with the 10 MHz channel bandwidth of the LTE signal used as a reference. The sampling rates of the two amplitude signals driving the DPAs were set to several configurations as listed in Table 6.3. The first configuration was used to avoid any interpolation (input and output frequencies of the SRC are the same) in order to validate the digital polar transmitter behavior. Then, the sampling rates were set to different values to verify if there is any impact on the eye diagram and constellation. As expected by the theory, the useful information is unchanged when changing the sample rate. The four configurations provided the same eye diagrams and constellations with identical EVM.

Table 6.3: *Configurations of sampling rates used with 64-QAM modulation*

Configuration	1	2	3	4
F_{S1}	100 MHz	100 MHz	133 MHz	160 MHz
F_{S2}	100 MHz	133 MHz	152 MHz	160 MHz

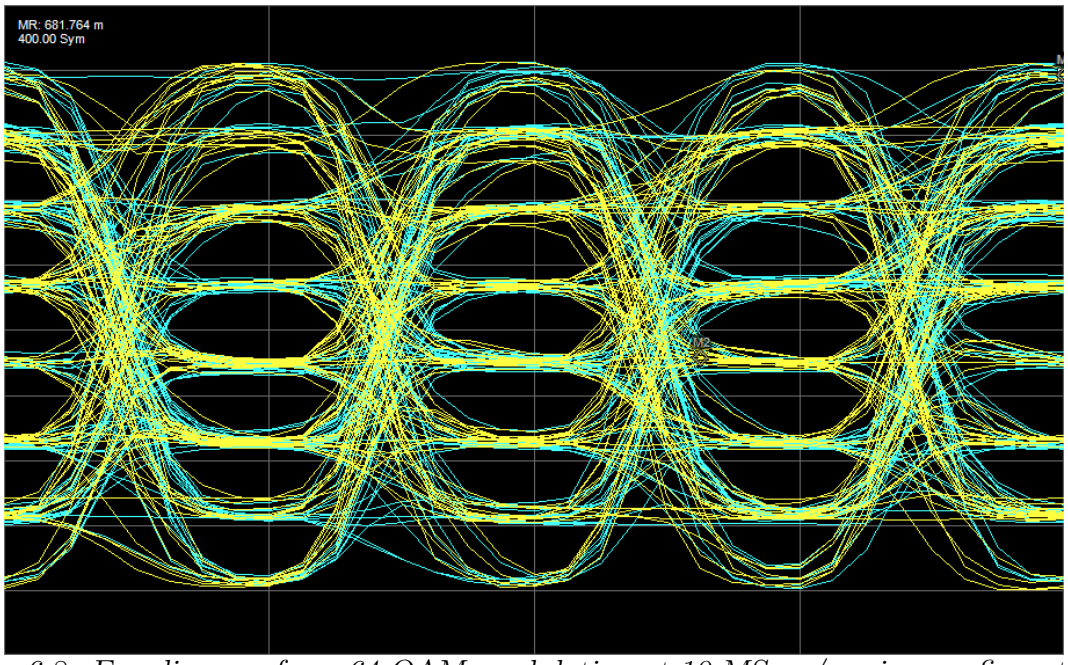


Figure 6.8: *Eye diagram for a 64-QAM modulation at 10 MSym/s using configuration 2*

The eye diagram observed in configuration 2 is depicted on Figure 6.8. The in-phase and quadrature signals are superimposed. The center eyes are well open while the higher and lower ones show distortions.

In order to get a better idea of the impact of the distortions occurring at high ACW, the resulting constellation is plotted on Figure 6.9. As can be observed, the constellation suffers from distortion at the corners. This indicates that the digital to RF conversion performed by the DPAs suffers from saturation at the upper codes. It is interesting to remark that the saturation on RF signals occurs in the same way as the output biasing current (I_{bias}) studied before. The RMS value of the EVM is -28 dB (4%) when considering the total constellation. However, this value drops down to -31 dB (2.8%) when removing the corners. This is calculated by generating a data stream avoiding these points.

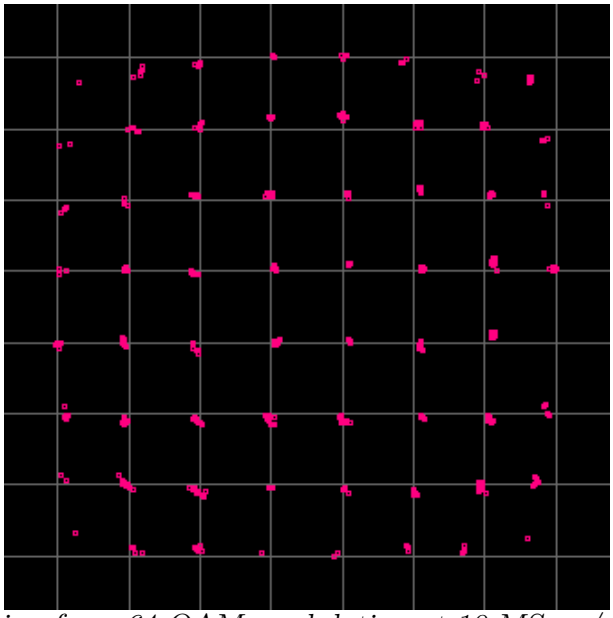


Figure 6.9: *Constellation for a 64-QAM modulation at 10 MSym/s using configuration 2*

All these measurements were done without usinging pre-distortion. The logic implemented on FPGA anticipates the use of pre-distortion, thanks to look up tables (LUT) on the amplitude paths between the sample rate converters and the output blocks. However, the measurement setup was not able to support fine AM-AM and AM-PM characterizations with RF signals. The AM-AM characteristic was measured with static ACW, but the resulting pre-distortion did not improve the EVM and eye diagram. The next measurements are also performed without any pre-distortion.

6.3 Spectrum management in 2-rate architecture

The previous section presented the results in terms of DPA characterization and basic modulation under different configurations. This section will focus on the spectrum management performed by the proposed architecture. Due to the high sampling rate used on the FPGA and limited memory, only LTE and 802.11n standards were used. All the spectra are normalized in dBm/Hz on the magnitude axis and the resolution bandwidth (RBW) will be specified.

6.3.1 Comparison between theory and measurement

First, the two DPAs of the prototype were set to the same sampling rate of 100 MS/s in order to compare the amplitude of the first images with the simulated spectrum for the case of an ideal 12-bit 2-path digital polar amplifier. The input power was set to the 1 dB input compression point. Figure 6.10 shows both the measured and simulated spectra. Few remarks need to be formulated. First, a wide spectral regrowth is present around the fundamental of the measured spectrum. This is directly related to the IQ modulator bandwidth used to generate the phase modulated signal. In fact, the -3 dB bandwidth of the IQ modulator is 95 MHz around the carrier frequency. The symbol generator implemented on FPGA only provides 12-bit IQ signals to generate the phase. It was impossible to verify the impact of the number of bits on the spectral regrowth.

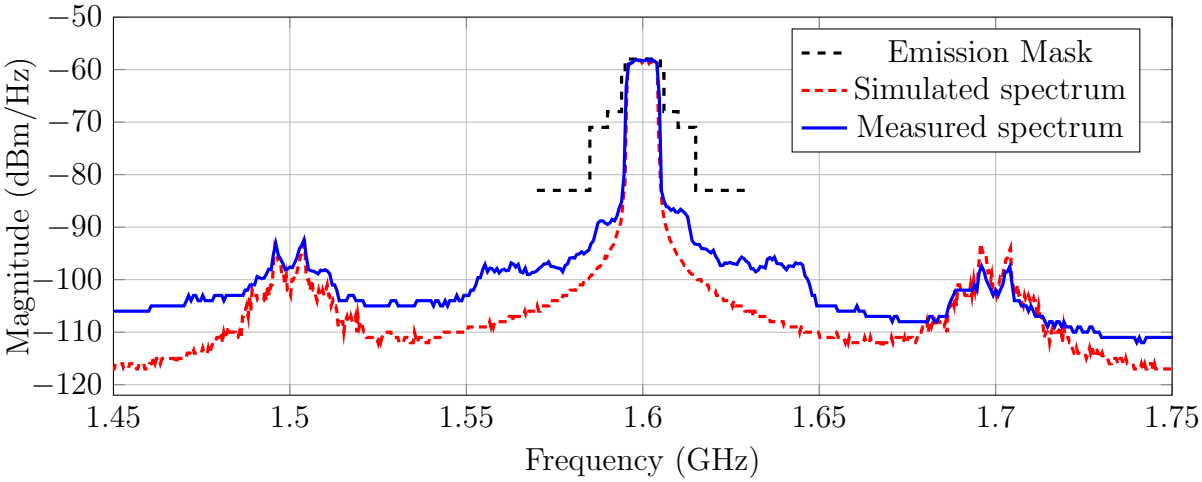


Figure 6.10: *Comparison between the measured (RBW = 510 KHz) and simulated spectrum of the prototype with 10 MHz LTE standard and* $F_{S1} = F_{S2} = 100MS/s$

An other spectral regrowth effect can be observed around the fundamental, between 1.586 GHz and 1.614 GHz. This regrowth can result from three defects of the transmitter:

- bandwidth of the phase modulator;
- synchronization between phase and envelope;
- non-linearity of the envelope converter.

The phase modulator bandwidth is 5 times the channel bandwidth of the LTE signal which is sufficient to avoid spectral regrowth due to the non linear transformation from Cartesian to polar form. The synchronization between the phase modulated RF carrier and baseband envelope is ensured by controllable delays implemented on FPGA using flip-flops. The finest delay step is ensured by flip-flops working at two times the sample rate on both clock edges. In our case the 100 MS/s sample-rate implies a finest delay equals to 2.5 ns which would result in lower regrowth. The remaining explanation of the small spectral regrowth is the non linear behavior of the DPA (INL and DNL) which introduces AM-AM and AM-PM distortion. This is the most probable cause and would require pre-distortion in order to correct it.

Second, the noise floor is higher than expected. The main reason for this is the clock leakage. The spurious at the multiples of the clock frequency are modulated by the envelope signals and the resulting products are added to the noise floor. Figure 6.11 shows a zoom on the fundamental with a finer RBW of 120 KHz. The carrier was set to 1 GHz in order to be closer to the frequency providing the maximum output power. The spectral emission mask is fully met.

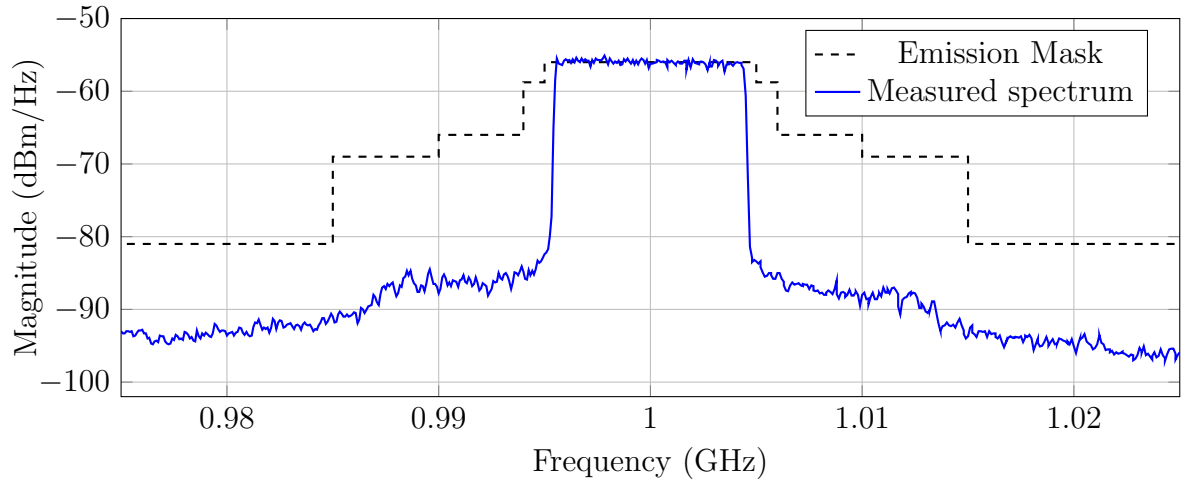


Figure 6.11: *Zoom on the fundamental of the measured spectrum (RBW = 120 KHz) for a 10 MHz LTE channel located at 1GHz and in configuration 1*

Finally, the most noteworthy fact of Figure 6.10 is the strong matching of the images. Indeed, the magnitude of the first images in case of the simulated system are around 35.2

dB lower than the fundamental, while the measured images are 34.4 dB lower. The spread images are consistent to the theory of the recombination of the filtered phase with the digital envelope in digital polar transmitter. The measurements are fully concordant to the simulations. The total power is 13.31 dBm while E-UTRA ACLR is 31.4 dB which meets the 30 dB required by the standard [2]. A current of 86.1 mA is drawn from the 2.5 V supply and 36.3 mA from the 1.2 V supply. The total power consumption is 258.8 mW (24 dBm) resulting in 8.28 % PAE. The PAE with a LTE signal is lower than the PAE with a single-tone sine wave. In fact, the envelope modulation and thus the PAPR results in an average output impedance higher than the impedance in the case of constant ACW. On the other side the average power consumption is reduced. The mismatch between the average output impedance of the DPAs and the impedance presented by the matching network reduces the delivered power, impacting the efficiency.

The prototype was also tested with a 802.11n signal offering a 20 MHz channel bandwidth. Figure 6.12 shows the output spectrum when both paths are set to 100 MS/s sampling rate. The 95 MHz bandwidth is not sufficient anymore to avoid spectral regrowth in the adjacent channel. As can be seen in Figure 6.12, the spectral emission mask is met with low margin. The total power is 11.72 dBm while ACPR is 27.8 dB.

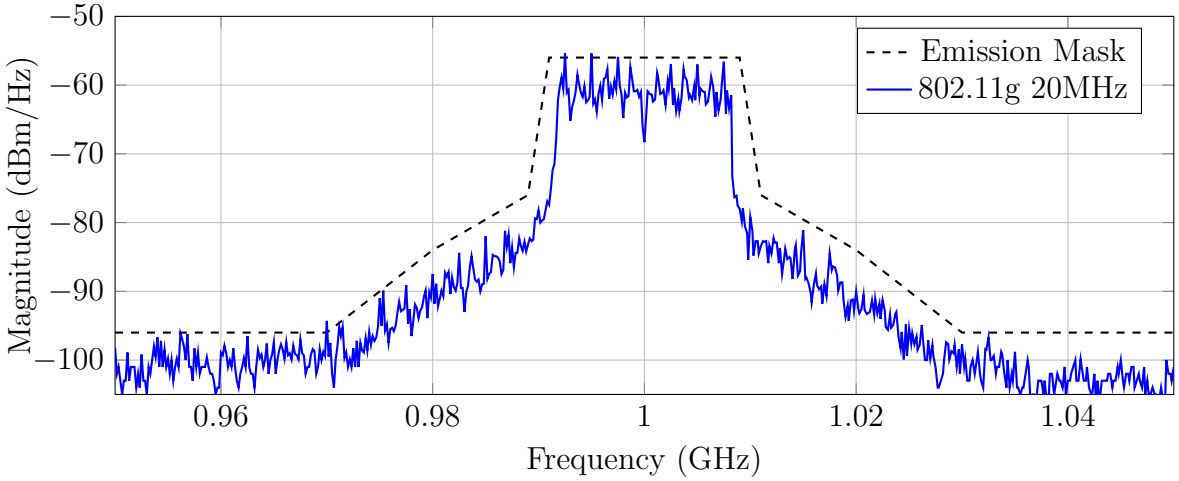


Figure 6.12: *Measured spectrum at the output of the prototype (RBW = 120 KHz) with 802.11g signal with 20 MHz channel*

The next section will discuss of the ability of the system to suppress the images when the envelope signals are sampled at different frequencies.

6.3.2 Measured image attenuation in 2-rate architecture

This section will compare the spectrum after the recombination of both paths when different ratios are applied to the sample rate converters. The configuration of the ratios are listed in Table 6.4. Configuration 1 will serve as a reference to compare the image magnitude with different sampling rates.

Table 6.4: *Configurations of sampling rates used to validate the multi-rate approach*

Configuration	1	2	3	4	5
F_{S1}	100 MHz	100 MHz	100 MHz	100 MHz	160 MHz
F_{S2}	100 MHz	133 MHz	152 MHz	160 MHz	160 MHz

Figure 6.13 depicts the configurations 1 and 2. The strong image located at 1.1 GHz is separated into two images at 100 MHz and 133 MHz offset from the carrier. The peak at 1.067 GHz is due to the leakage of the 8^{th} harmonic of the clock at F_{S2}. In the same way, Figure 6.14 and 6.15 show the images shifting when F_{S2} is set respectively to 152 MHz and 160 MHz. Figure 6.16 illustrates the spectrum when both F_{S1} and F_{S2} are changed from 100 MHz to 160 MHz.

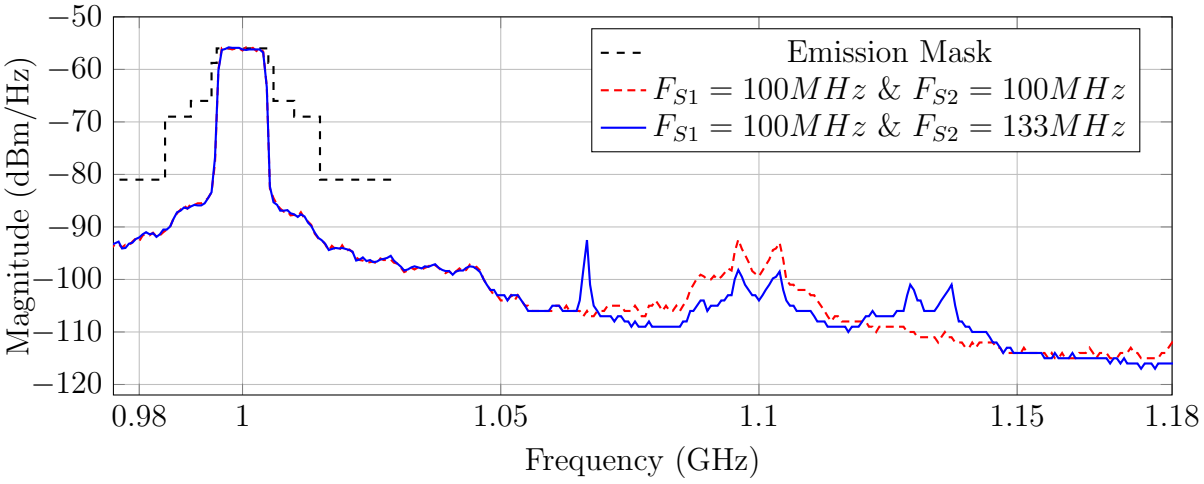


Figure 6.13: *Measured spectrum at the output of the prototype (RBW = 510 KHz) when the SRCs are set in configuration 1 and 2 with 10 MHz LTE standard*

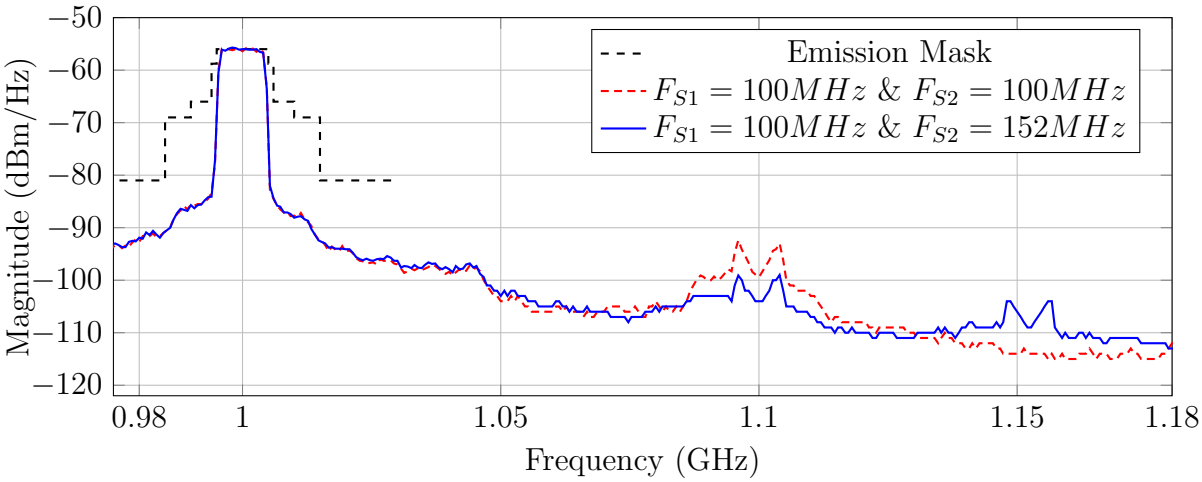


Figure 6.14: *Measured spectrum at the output of the prototype (RBW = 510 KHz) when the SRCs are set in configuration 1 and 3 with 10 MHz LTE standard*

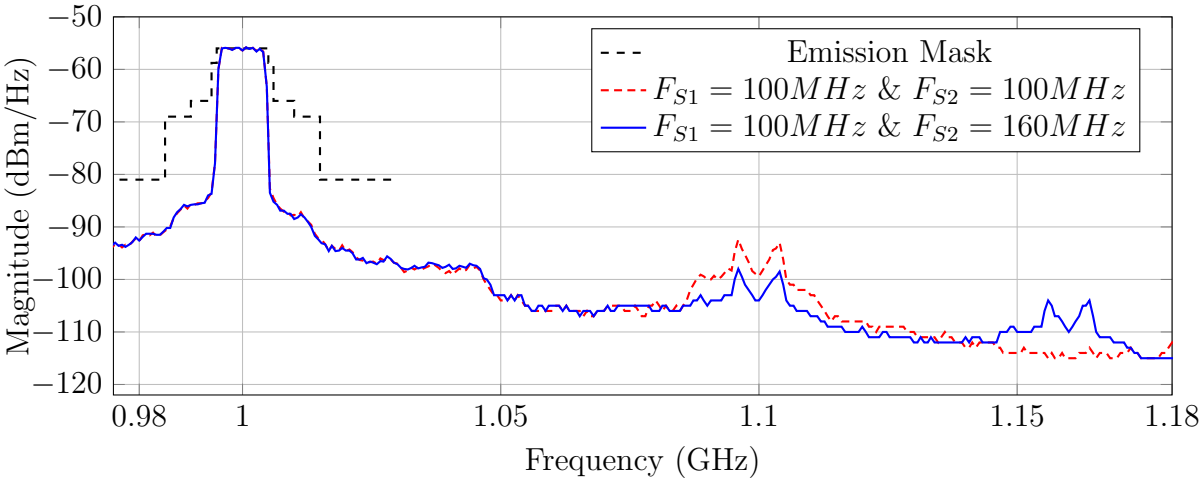


Figure 6.15: *Measured spectrum at the output of the prototype (RBW = 510 KHz) when the SRCs are set in configuration 1 and 4 with 10 MHz LTE standard*

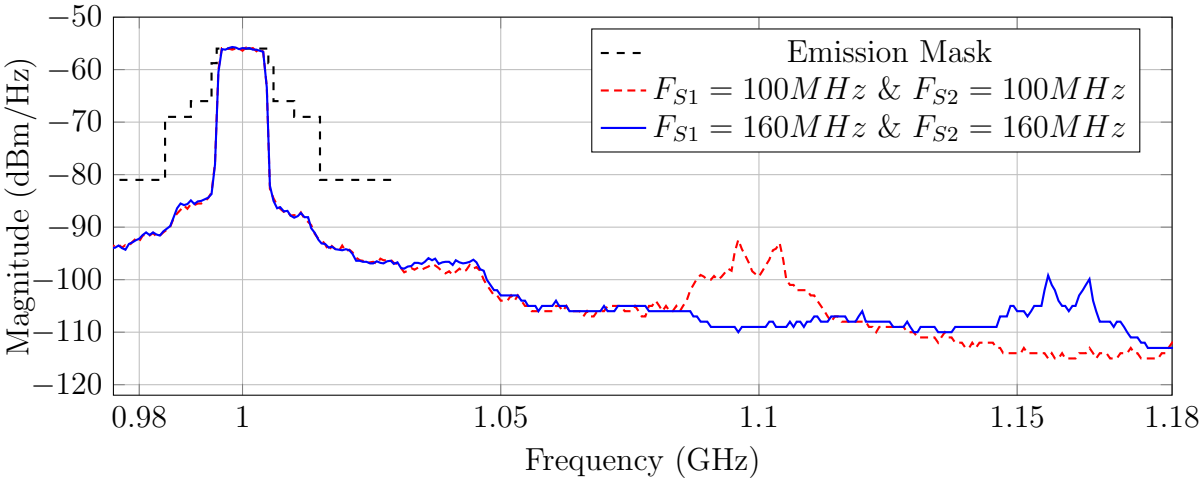


Figure 6.16: *Measured spectrum at the output of the prototype (RBW = 510 KHz) when the SRCs are set in configuration 1 and 5 with 10 MHz LTE standard*

The amplitude of the images located at 1.1GHz in configurations 2, 3 and 4 are 5.5 dB lower than in configuration 1. The amplitude of the image located at 1.16GHz in configurations 4 is 5 dB lower than in configuration 5. The theory expected a 6 dB difference in case of matched paths (DPA, impedance matching and power combining). The results presented on Figure 6.13, 6.14 and 6.15 are coherent with the expected behavior of a 2-rate transmitter.

6.4 Conclusion

The measurement results presented in this section validate the use of DPA as a digital envelope modulator in polar transmitters based on a multi-path architecture. The main restriction to use the proposed architecture with wide-band signal such as 802.111n is due to the external band-limited phase modulator. The proposed architecture could be improved in several ways.

First, the phase modulator must be designed in order to be implemented on the same die as the DPAs and to support a bandwidth wider than 100 MHz.

Second, the non-linearities of the digital to RF conversion were not compensated during the tests. However the EVM characterization with 64-QAM signal shows that AM-AM pre-distortion would at least improve the EVM and potentially the spurious emission. The digital pre-distortion could be implemented on FPGA, together with the sample rate converters.

Third, the implemented system suffers from the self-biased structure of the unit-amplifiers. Any transistor mismatch results in a shift of the biasing point of both first and second stages of the unit-amplifier cells. The addition of input biasing circuits or the use of differential structures for the first stage of the unit-cell could help to tune the system in order to compensate for any biasing deviation.

Besides the in-band behavior of the two-path DPA, the multi-rate theory is verified. The images are attenuated by roughly 6 dB without impacting the EVM and spurious emissions. The next step would of course be to increase the number of paths up to 4. Thus, the system would be able to attenuate the envelope images by 12 dB.

Chapter 7

Conclusion

A wide-band digital polar transmitter dedicated to opportunistic radio and based on a multi-path multi-rate approach has been demonstrated. A 2-path prototype chip has been designed in 65nm CMOS process. The amplifier delivers up to 16.7 dBm over a 0.9 - 1.9 GHz band while providing 12.4% PAE. The main advantage of the multi-path multi-rate architecture is the ability to lower the magnitude of the images due to sampling which results in lower constraints on filtering.

Parallel works

As explained previously in the state-of-the-art, the digital power amplifier and multi-path approach are commonly used together in order to deliver high power and implement basic power control. However, the majority of DPA implementations [7, 13, 14, 73, 74] are optimized for narrow band system. Only the implementation made by Presti et al. [15] in 2009 targeted a wide-band application covering a 0.8 - 2 GHz band. The images were suppressed thanks to a raw oversampling and limited bandwidth of the envelope modulator. This solution is suitable for standards with narrow channel (i.e. 5 MHz), but standards such as LTE and 802.11g/n would require an infeasible oversampling clock frequency and increase of the modulator bandwidth. Our work presents the main advantage to avoid the need of high clock rates or band-limited envelope modulator.

Besides the works on the implementation of the DPA, several works have been performed on the architecture of all digital transmitters. The mains two works [41] and [83] are based on the implementation of a DPA with an all-digital PLL (ADPLL).

In [41], Staszewski proposes the implementation of an ADPLL with spurious suppression (from time-to-digital conversion and digitally controlled oscillator). The power stage and envelope modulator is done by two DPAs in order to cover two different bands, the lower

band (900 MHz) and the higher band (1800 MHz).
In [83], Lai presents a digital-to-RF polar transmitter dedicated to Bluetooth (2.4 GHz). Due to the narrow bandwidth of the system the envelope information is oversampled in order to shift the images out of the band of interest.
The DPA developed during this thesis integrates compensation cells in order to reduce the input impedance variation dependent to the ACW. The same problem occurs at the output with the output impedance modulated by the ACW. Ye et al. in [84] propose a reconfigurable power combiner thanks to a switchable transformer (XFMR). The MSB of the envelope controls the state of the XFMR in order to improve the matching between the load and DPA. This results in an efficiency improvement.

Future directions

Due to area limitation the chip developed in this thesis only integrates two DPAs without baseband interpolation of the envelope signal. This chip served as a prototype to demonstrate the ability of a multi-path architecture to manage its spurious emission over a wide bandwidth without the need of an important oversampling.
Several improvements can be done to the actual prototype. First, the number of paths could be increased up to 4 paths in order to attenuate the images by 12 dB.
Second, the multi-rate interpolator implemented on FPGA and used as a sample rate converter can be directly integrated on the chip. This would reduce the number of digital pads used for the envelope signal. The direct implementation of the interpolator could also lead to the improvement of the clock domain crossing by the use of optimized logic.
Finally, on-chip the wide-band power combiner and matching network for the input and output RF signals would be the last step to lead to a fully operational digital envelope modulator for polar transmitters.

Digital power amplifiers show promising abilities, which make them good candidates to replace the actual narrow band IQ modulators. However, DPAs only performs the modulation of the envelope and are closely related to the phase modulator. Multi-rate DPA paves the way for the implementation of wide-band and highly reconfigurable transmitter but still require a frequency agile and wide band phase modulator. It would be interesting to investigate the use of the multi-rate approach applied to phase modulator based on ADPLL, with several DCO in parallel.

List of publications

Werquin, A.; Frappé, A.; Flament, A.; Stefanelli, B.; Kaiser,A., IEMN/ISEN, "Wideband image rejection in digital polar architectures", Colloque National du GDR SOC-SIP, Lyon, 15-17 June 2011

Werquin, A.; Frappé, A.; Muller, J.; Kaiser, A., "Spectral regrowth analysis in wideband polar architectures applied to software defined radio", New Circuits and Systems Conference (NEWCAS), 2011 IEEE 9th International, pp.305-308, 26-29 June 2011

Werquin, A.; Frappé, A.; Kaiser, A., "Spurious emissions reduction using multirate RF transmitter", Circuits and Systems (ISCAS), 2011 IEEE International Symposium on, pp.965-968, 15-18 May 2011

Werquin, A.; Frappé, A.; Kaiser, A., "A Multi-path Multi-rate CMOS Polar DPA for Wideband Multi-standard RF Transmitters", Radio Frequency Integrated Circuits Symposium (RFIC), 2013. IEEE, 2-4 June 2013

Patent

Werquin Arnaud, Kaiser Andreas, Frappé Antoine, Centre National de la Recherche Scientifique (C.N.R.S); FR2973611(A1) 2012; "Procédé de suppression d'images dans un transmetteur numérique large bande" FR2973611(A1) 2012

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Abstract

Multiple Rates Multiple Paths Wideband Digital Transmitter with Low Spurious Emissions Applied To Opportunistic Radio

Keywords: digital power amplifier, polar architecture, multi-path, multi-rate, sample-rate conversion, digital transmitter, software defined radio, LTE, 65nm CMOS

Wireless communication terminals are evolving towards multi-standard terminals. The transmit part of a frequency agile cognitive radio must be highly reconfigurable in order to obtain the optimum communication. The most critical element in a transmitter is the power amplifier and its interface with the antenna. In this work a digital transmitter based on a digitally controlled power amplifier (DPA) is investigated, and a prototype has been implemented to prove the feasibility of the concept.

The proposed architecture is based on multi-path approach with different sample rate conversions in order to manage the spurious emissions due to the direct digital to RF conversion performed by the DPA without the need of passive filters. The transmitters implemented in advanced CMOS process are commonly based on multiple paths architecture. The approach proposed in this work takes advantage of this parallel structure to generate several signals with the same information but different sample rates.

The LTE standard has been taken as the standard example, and a 2-path digital envelope modulator has been designed in a 65nm CMOS technology. The baseband sample rate conversions and control logic have been implemented on FPGA. The path recombination is performed with off-board components. The fabricated prototype digital envelope modulator IC demonstrates the image attenuation principle with up to 6dB attenuation. The DPAs support four sample rates 100 MS/s; 133 MS/s; 152 MS/s; 160MS/s. The amplifier delivers up to 16.7dBm over a 0.9 - 1.9 GHz band while providing 12.4% PAE and a -28dB EVMrms.The prototype was tested with a 10 MHz LTE and a 20 MHz 802.11g standards. The total circuit occupies 1.04mm^2 and the area dedicated to the DPA and control logic only occupies 0.25mm^2.

Résumé

Transmetteur numérique large bande multi-cadence multi-voie à faible emission parasite appliqué à la radio opportuniste

Mots-clefs: amplificateur de puissance numérique, architecture polaire, multiple voies, multiple cadences, conversion de cadence d'échantillonnage, émetter numérique, radio logicielle, LTE, 65nm CMOS

Les terminaux de communications sans fil évoluent afin de supporter plusieurs standards. L'émetteur d'une radio cognitive agile en fréquence se doit d'être reconfigurable afin d'offrir la meilleure qualité de communication. L'élément le plus critique dans un émetteur est l'étage de puissance et sa connexion avec l'antenne. Un émetteur numérique basé sur un amplificateur de puissance commandé numériquement (DPA) est étudié et un prototype a été implémenté afin de démontrer la faisabilité du concept.

L'architecture proposée est basée sur une approche à multiple voies combinée à une conversion de fréquences. La diversité introduite sur les fréquences d'échantillonnage permet de contrôler le niveau d'impuretés spectrales émisses. Celles-ci proviennent de la conversion directe numérique vers RF. Cette conversion est réalisée par le DPA sans le recours à des filtres passifs. Les émetteurs implémentés en technologies CMOS avancées ont souvent recours à une architecture à multiple voies. L'approche présentée dans ce manuscrit tire avantage de cette structure parallèle afin de générer des signaux portant la même information mais échantillonnés à des fréquences différentes.

Le standard LTE a été pris comme standard de référence, et un modulateur d'enveloppe a été conu en technologie CMOS 65nm. Les conversions de fréquences bande de base et la logique de contrôle on été implémentées sur FPGA. La recombinaison des voies est réalisée à l'aide de composants discrets. Le prototype de modulateur d'enveloppe numérique réalisé, démontre le principe d'atténuation d'images pouvant atteindre 6dB dans le cas d'un système à deux voies. Les DPAs supportent quatre fréquences d'échantillonnage 100 MS/s; 133 MS/s; 152 MS/s; 160MS/s. L'amplificateur délivre jusqu'à 16.7dBm sur la bande 0.9 à 1.9 GHz et assure un PAE de 12.4% avec un EVMrms de -28dB. Le prototype a été testé avec des signaux LTE de 10 MHz et 802.11g de 20 MHz. La surface totale occupée par le circuit est de 1.04mm^2 tandis que la surface dédié aux DPAs et logique de contrôle occupent seulement 0.25mm^2.