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Wide Bandgap (SiC/GaN) Power Devices Characterization and Modeling: *Application to HF Power Converters*

Caractérisation et Modélisation des Composants Semi-conducteurs à Grand Gap (SiC/GaN): *Application aux Convertisseurs HF*

Soutenue le 23 octobre 2014 devant le jury

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To Mei,

To my parents,

Abstract

Compared to traditional silicon (Si) semiconductor material, wide bandgap (WBG) materials like silicon carbide (SiC) and gallium nitride (GaN) have lots of interesting physical properties such as bigger bandgap energy, larger breakdown field and higher saturation velocity. Therefore, they are gradually applied to fabricate power semiconductor devices, which are used in power converters to achieve high power efficiency, high operation temperature and high switching frequency. As those power devices are relatively new, their characterization and modeling are important to better understand their characteristics for better use and for power converters design. This dissertation is mainly focused on those WBG power semiconductor devices characterization, modeling and fast switching currents measurement.

In order to measure their static characteristics, a single-pulse method is at first presented. It is shown in the characterization results that by controlling the pulse duration, power device junction temperature can be maintained constant during the characterization. A SiC diode and a "normally-off" SiC JFET is characterized by this method from ambient temperature to their maximal junction temperature with the maximal power dissipation around kilowatt. Afterwards, in order to determine power device inter-electrode capacitances, a measurement method based on the use of multiple current probes is proposed. With a simple setup, this method allows to isolate the measurement equipment from the power source. This method is validated by characterizing inter-electrode capacitances of power devices of different technologies. It is able to apply this method to characterize unknown impedances from several tens of milliohms to several tens of kiloohms in the megahertz range, which corresponds to the conditions that power devices are in ON and OFF state.

Behavioral models of a Si diode and the SiC JFET are built by using the results of the above characterization methods, by which the evolution of the inter-electrode capacitances for different operating conditions are included in the models. Power diode model is validated by comparing with the measurement on reverse recovery current waveform for different switching conditions.

In order to measure fast switching current waveforms to validate SiC JFET model, a current measurement method based on the use of the current surface probe is proposed. By comparing with other current equipments, it is proved that the presented method can measure GaN HEMT fast switching current transition times of a few nanoseconds. The SiC JFET model is thus validated by comparing with the measurement on switching current and voltage waveforms for different switching conditions.

Keywords: Power semiconductor devices, silicon carbide, gallium nitride, static characteristics, dynamic characteristics, modeling, power converters, high frequency

Résumé

Les matériaux semi-conducteurs à grand gap tels que le carbure de silicium (SiC) et le nitrure de gallium (GaN) ont des propriétés physiques intéressantes. Ils sont utilisés pour fabriquer des composants semi-conducteurs de puissance, qui vont jouer un rôle très important dans le développement des futurs systèmes de conversion d'énergie. L'objectif est de réaliser des convertisseurs avec de meilleurs rendements énergétiques et fonctionnant à haute température. Pour atteindre cet objectif, il est donc nécessaire de bien connaître les caractéristiques de ces nouveaux composants afin de développer des modèles qui seront utilisés lors de la conception des convertisseurs. Cette thèse est donc dédiée à la caractérisation et la modélisation des composants à grand gap, mais également l'étude des dispositifs de mesure des courants des commutations des composants rapides.

Afin de déterminer les caractéristiques statiques des composants semi-conducteurs, une méthode de mesure en mode pulsé est présentée. Le dispositif de mesure développé permet de maintenir la température de jonction du composant constante durant la phase de mesure. Dans le cadre de cette étude, une diode SiC et un JFET SiC "normally-off" sont caractérisés à l'aide de cette méthode. Afin de mesurer les capacités inter-électrodes de ces composants, une nouvelle méthode basée sur l'utilisation des pinces de courant est proposée. Elle permet de réaliser des mesures sous tension grâce à une isolation galvanique entre les équipements de mesure et le circuit de puissance. Cette méthode permet également de mesurer les impédances des composants passifs dans une large bande de fréquence.

Des modèles comportementaux d'une diode Si et d'un JFET SiC sont proposés en utilisant les résultats de caractérisation. Le modèle de la diode obtenu est validé par des mesures des courants au blocage (recouvrement inverse) dans différentes conditions de commutation. Pour valider le modèle du JFET SiC, une méthode de mesure utilisant une pince de courant de surface est proposée. Elle sera également utilisée pour mesurer les courants dans un HEMT GaN. Les résultats obtenus sont comparés à ceux effectués avec d'autres moyens de mesure de courant (sonde de courant passif, sonde de courant à l'effet Hall, shunt). Le modèle du JFET SiC est alors validé dans différentes conditions de fonctionnement.

Mots-clés: composants semi-conducteurs, carbure de silicium, nitrure de gallium, caractéristiques statiques, caractéristiques dynamiques, modélisation, convertisseurs statiques, haute fréquence

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General Introduction

The presented research work in this dissertation has been carried out from October 2011 to September 2014, at Laboratoire d'Électrotechnique et d'Électronique de Puissance (L2EP) of the University of Lille 1.

Scope of the work

Because of lots of interesting physical characteristics like large energy bandgap, high breakdown electrical field, high saturation velocity and small relative permittivity etc., wide bandgap (WBG) materials like silicon carbide (SiC) and gallium nitride (GaN) are gradually applied to power semiconductor devices fabrication in recent years. Compared to traditional silicon (Si) power devices, wide bandgap power devices have less power losses and they can operate in higher temperature and higher operation frequency. Power converter energy efficiency and power density can thus be improved when using these wide bandgap power devices. As those devices are relatively new, their characteristics and modeling are therefore becoming a research interest to better understand their properties for better use and for power converters design.

The main research topic in this dissertation is to develop the characterization method of the wide bandgap devices in order to obtain their static and dynamic characteristics. Afterwards, based on the characterization results, power device behavioral models are built. In order to validate the proposed power device models on fast switching conditions, current measurement methodology is developed to measure current transition during a few nanoseconds.

Different following approaches have been brought concerning the main research topic of the dissertation:

- Characterization

  The power device characteristics can be divided on static characteristics and dynamic characteristics.

1. Static characteristics in which the key issue is to characterize the power devices in a large operation zone while maintaining its junction temperature constant. In order to achieve this objective, the single-pulse method is presented in the dissertation to characterize power device at different junction temperatures with a large power dissipation.
2. Dynamic characteristics in which the key issue is to characterize power device inter-electrode capacitances on high blocking voltage and in different operation zones. With a simple setup, a characterization method based on multiple current probes which helps to isolate the measurement equipment with the external power supply, is proposed in the dissertation in order to achieve this objective.

- Modeling

  As power device behavioral models are presented in the dissertation, the key issue is to apply power device characterization results by the above methods when the power devices are in different operation conditions. To represent diode reverse recovery current, a Si diode is thus modeled with its dynamic impedance characterization results when it is blocked and is in conduction. Afterwards, a "normally-off" SiC JFET is modeled based on its inter-electrode capacitances both when it is blocked and in linear region.

- Validation

  The switching transition of wide bandgap power devices can be shortened to a few nanoseconds. Thus the key issue is how to correctly measure fast switching current in order to validate the presented power device models. With small insertion impedance and large bandwidth, the current measurement method based on current surface probe is proposed in the dissertation to achieve this objective. It is to be validated by measuring GaN HEMT switching current of a few nanoseconds.

Organization of the dissertation

The dissertation is organized with the following chapters.

In Chapter 1, the state of the art of the research work is presented starting from discrete wide bandgap (WBG) power devices to their applications in power converters. The main focus is on WBG materials properties and power devices, their characterization and modeling, their driver circuits. Following by that, the road map of power efficiency and power density of power converters with WBG power devices and their measurement methodology are presented.

In Chapter 2, the single pulse method will be at first presented to determine power devices static characteristics. The principle and measurement configuration are illustrated. Power device junction

temperature T_j is estimated during the measurement to show that it is stable in the measurement. Characterization results of a SiC diode and a "normally-off" SiC JFET at different T_j is shown. Then, multiple-current-probe method is to be demonstrated in order to characterize power device inter-electrode capacitances at high V_{DS} voltage. The proposed characterization method with two current probes is at first presented and applied to characterize power transistor C_{gs}, C_{gd} and C_{ds} values. In order to decrease the measurement error propagation of two-current-probe method, a characterization method based on three current probes is then presented. Afterwards, how to increase the sensibility of the multiple-current-probe measurement method is presented in order to characterize unknown impedance from several dozens milliohms to several tens of kiloohms in megahertz range.

In Chapter 3, a Si diode is modeled with its dynamic impedance measured by multiple-current-probe method when it is blocked and in conduction. The characterized dynamic resistances are converted into corresponding static resistances, which are further represented by mathematical equations in the model. Then, the same SiC JFET is modeled with its measured static characteristics by single pulse method and its inter-electrode capacitances values by multiple-current-probe method when it is blocked and in linear region, which are expressed by mathematical equations using in PSPICE.

In Chapter 4, the presented Si diode model is validated with the measurement on reverse recovery current of different current switching slew rates. The difference between the model and the measurement is analyzed to propose further approaches to improve the model. The diode switching current is measured by an active Hall effect current probe (HECP). The influence of the HECP transfer function on switching current waveform is presented by adding its transfer function on the obtained simulation current.

To measure fast switching current, a current surface probe is presented. Its insertion impedance and transfer impedance are characterized on different configurations, which is further verified by comparing with other current measurement equipments on power device fast switching current measurement. Then, it is used to measure SiC JFET switching current in order to validate the proposed model on different switching conditions. The presented SiC JFET model is then compared with a model which is made with power device datasheet information. The similarity and difference of the two models are analyzed.

The final conclusions are presented at last together with the future work.

Chapter 1

State of the Art of Wide Bandgap Materials and Power Devices

Power electronics technologies are very important in electrical energy conversion systems, where the power semiconductor devices play an important role. Since the birth of the first power transistor in 1947, power electronics technologies have developed in the world of silicon (Si) material [1]. Up until today, with the development of more than 60 years, Si power semiconductor devices fabrication process is very mature and can meet different power demands in electrical energy conversion.

However, compared to Si, wide bandgap (WBG) semiconductor materials have lots of intrinsic advantages which are very attractive for future power electronics applications. From the beginning of the 21st century, silicon carbide (SiC) and gallium nitride (GaN) power devices fabrication develops very fast. For the following decades, they are good competitors to Si.

Physical proprieties of WBG materials and WBG power semiconductor devices will be first presented in this chapter. As those power devices are relatively new, it is necessary to know their characteristics for better use. Then different characterization methods are synthesized. Afterwards, WBG power devices modeling methods, their driver circuits are presented. After that, the integration of WBG power devices in power converters to achieve high energy conversion efficiency and high power density is illustrated. At last, fast switching current and voltage measurement methodologies are reviewed.

1.1 Wide Bandgap Materials and Power Devices

1.1.1 Wide bandgap semiconductor materials

It is shown in Table 1.1 the physical properties of different semi-conductor materials, where the energy bandgap E_g between conduction band and valance band is 1.12eV for Si, while that for SiC[1], GaN and Diamond is 3.2eV, 3.39eV and 5.6eV respectively. Thus, those three materials are called wide bandgap (WBG) semiconductor materials.

TABLE 1.1: Physical properties of different semi-conductor materials [3, 4]

Material	E_g at 300K (eV)	λ (W/cm·K)	V_{sat} (cm/s)	ϵ_r	E_c (MV/cm)
Si	1.12	1.5	1×10^7	11.7	0.3
SiC-4H	3.2	4.5	2×10^7	10	2.4
GaN	3.39	1.3	2.5×10^7	8.9	3.3
Diamond	5.6	20	2.7×10^7	5.7	5.6

A big value of E_g means that an electron is less probable to go through this band when temperature increases. While in terms of thermal conductivity, SiC and Diamond are much bigger than Si, which means that they can transfer heat easily. With these advantages, power semiconductor devices with WBG materials are able to operate in high temperature. It is to be noted, even though there is almost the same thermal conductivity between Si and GaN, thanks to the big E_g value of GaN, the relatively small thermal conductivity does not prohibit its operation in high temperature in comparison with Si. This advantage can help to decrease the cooling equipments and to increase power density of the electrical system. The above description can be illustrated in Figure 1.1 [5], which shows the limited operation temperature of different materials.

It is also observed that WBG materials have smaller relative permittivity ϵ_r and bigger saturation velocity V_{sat} than Si. Thus, smaller ϵ_r helps to realize power semiconductors devices with smaller inter-electrode capacitances, thereby to increase fast switching abilities. Once switching frequency is increased, the passive components volume in power converters can be decreased. Therefore, power density can be further increased [6].

For the breakdown field E_c, there are much bigger values for WBG materials than Si, which indicates that for the materials with the same thickness, there are much bigger breaking voltages for WBG materials than Si. Therefore, for the same breaking voltage, power semiconductor devices with WBG materials can achieve the junction thickness about one tenth smaller than Si, which helps to decrease power device ON-resistance and increase energy efficiency in power converters. The theoretic relation

[1]There are different crystalline forms for SiC. The major polytypes are noted as SiC-3C, SiC-4H, SiC-6H. Different polytypes can have different physical properties.[2]

between specific resistance and breakdown voltage of different materials is given in Figure 1.2 [7]. It is to be noted that the value of the specific resistance is dependent also on other parameters such as power device drift region doping, electron mobility and energy bandgap. It is also to be noted that diamond is not compared in Figure 1.2, because due to its property shown in Figure 1.1, it is more interesting to develop diamond in the application with the breakdown voltage more than 50kV and operation temperature more than 600K [5].

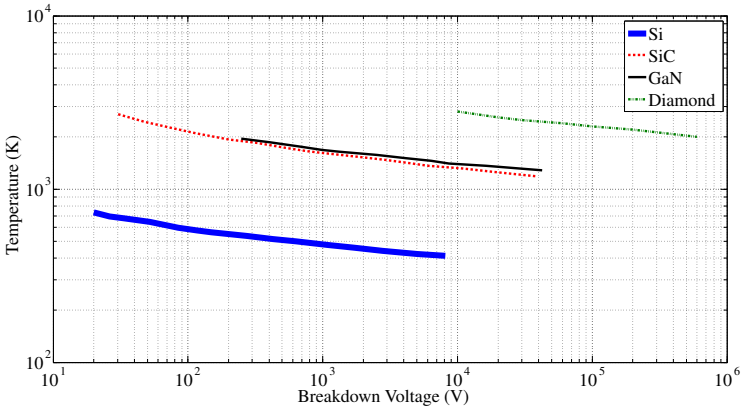


FIGURE 1.1: Limited operation temperature of different materials [5]

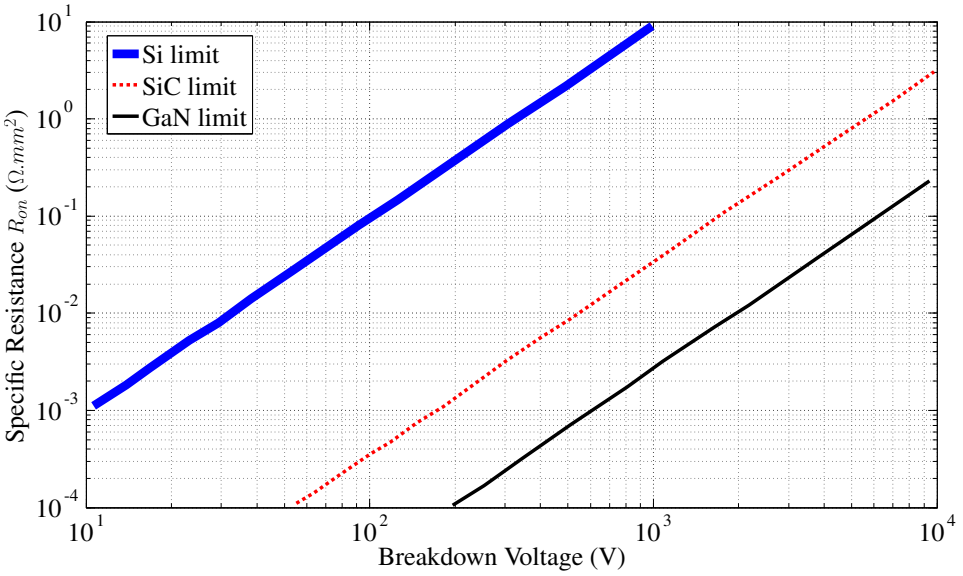


FIGURE 1.2: Theoretic relation between specific resistance and breakdown voltage of different semiconductor materials [7]

From the Table 1.1, it can be seen that diamond is an excellent candidate for power semiconductor devices, however, due to the complexity in the fabrication process, diamond power devices are not yet commercially available. Nevertheless, compared to Si, SiC and GaN materials have enough interesting advantages to be used in power semiconductor devices. Those advantages are illustrated in Figure 1.3 to show the comparison of Si, SiC and GaN properties.

The survey of SiC and GaN power semiconductor devices will be detailed in the next paragraph.

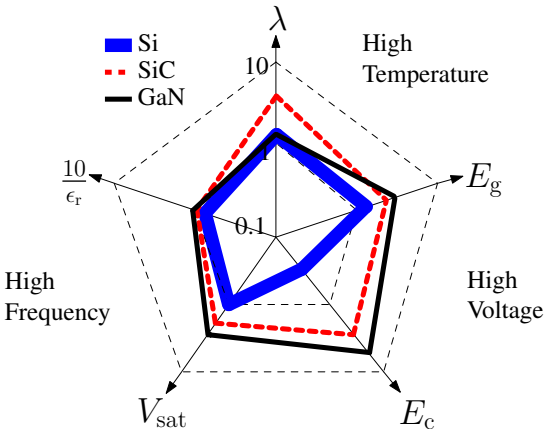
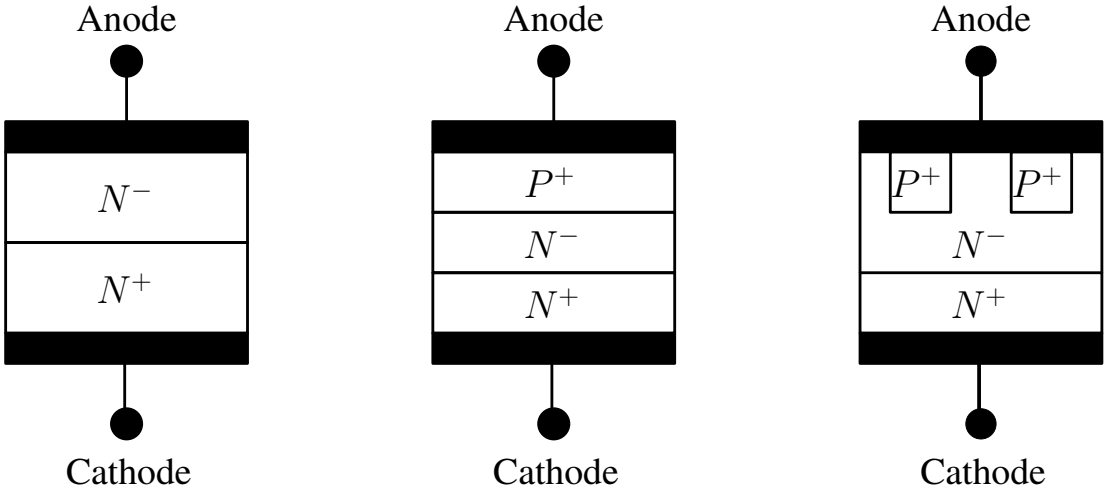


FIGURE 1.3: Physical properties comparison among Si, SiC and GaN

1.1.2 Wide bandgap power devices

The first commercial SiC power semiconductor device was a diode. There are in general three types of diodes [8, 9]:



(a) Schottky Barrier Diode

(b) p-i-n Diode

(c) Junction Barrier Schottky

FIGURE 1.4: Different diode types

- **Schottky Barrier Diode (SBD)** is a unipolar power device. Its structure is shown in Figure 1.4(a). SBD has the advantages such as low ON-state losses and fast switching. However, it has relatively low blocking voltage and high leakage current.
- **p-i-n Diode** is a bipolar device. Its structure is shown in Figure 1.4(b). It has a big blocking voltage, but has higher ON-state losses and reverse recovery phenomenon during the switching, which increases OFF losses.
- **Junction Barrier Schottky (JBS)** is the diode with the mixed characteristics of the SBD and p-i-n diode. Its structure is shown in Figure 1.4(c) [10]. It has bigger blocking voltage than SBD and faster switching capabilities than p-i-n.

For the Schottky diodes, it is difficult to find a Si Schottky diode with the blocking voltages more than 200V. However, the ratings of SiC Schottky diode can be found from 600V/20A to 1200V/40A, 1700V/25A. For the power diodes ratings from 600V to 1200V, compared to Si ultrafast power diodes, SiC Schottky diodes switch even faster and have smaller ON-resistance. Table 1.2 compares several key characteristics among different diodes with the similar rating around 600V/30A when junction temperature T_j is 25°C.

TABLE 1.2: Characteristics of different diodes around 600V/30A rating at $T_j = 25°C$

Reference	Type	V_F(V)	$I_R(\mu A)$	Q_{rr} or Q_c(nC)
ISL9R3060G2	Si	1.7	3	450
DPH30IS600HI	Si	2.2	< 1	450
C3D10060G	SiC	1.6	10	25
SCS230AE2	SiC	1.35	3	23
IDW20G65C5	SiC	1.3	0.3	29

In Table 1.2, the diode forward voltage drop V_F is compared when the forward current I_F is 15A and T_j is 25°C. It is shown that the SiC Schottky diodes have a lower V_F compared to Si diodes, which allows to decrease the conducted losses[2]. For diode leakage current I_R, which is compared when blocking voltage $V_R = 600V$ and T_j is 25°C, it is observed that Si diodes have smaller leakage current than SiC diode. This difference is due to the diode type, because the Si diodes with ratings around 600V are usually p-i-n bipolar diodes, and SiC diodes are usually Schottky unipolar diodes. With the SiC technology improvement, especially the merged PN junction technology applied in Schottky diode fabrication (JBS), small I_R can be observed in recent SiC Schottky diode datasheets (IDW20G65C5 as an example). This improvement can increase the blocking voltages of SiC diodes in the near future. For the terms of the diode recovery charge, Q_{rr} (reverse recovery charge) for p-i-n diode and Q_c (capacitive charge) for Schottky diode, there is fewer charge in SiC Schottky diode than in Si diode. This parameter indicates that SiC diode can switch much faster than Si diode.

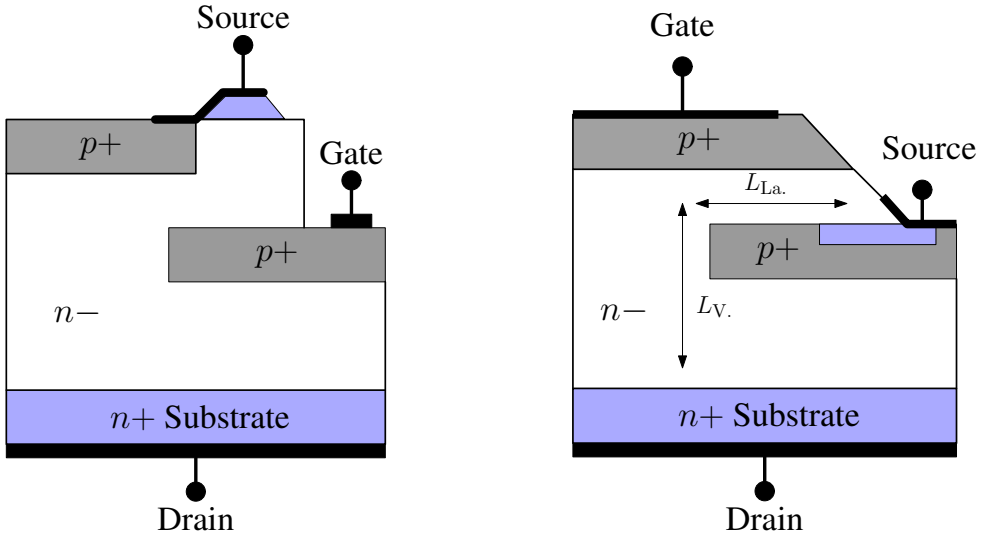
The first commercial WBG power transistor is SiC Junction Field Effect Transistor (JFET), which is a unipolar power device. Nowadays, the SiC JFETs developing in laboratories or having been commercialized[3] are with the blocking voltage around 1200V and nominal current up to 40A. It is to be noted that this power rating is much bigger than a Si unipolar power device. The blocking voltages of Si MOSFET is usually below 1000V. Above 1000V, Si bipolar power transistor like IGBT is widely used in power converters.

Two different SiC JFET structures, which are realized by SiCED and Infineon [11], are presented in Figure 1.5. These transistors are normally-on devices, which means that when the gate and

[2]It is to be noted that when diode is in conduction, junction temperature T_j increases, thus the above difference on V_F might be decreased, but SiC diode has generally less conduction loss than Si diode.

[3]SiC JFET was commercialized by Semisouth during 2005 to 2012. The company is crashed down in 2012.

source is in short-circuit, the transistor is in conduction. In the structure shown in Figure 1.5(a) (Transistor 1), the current flows from drain to source directly, thus it offers a short channel length, which helps to decrease the channel ON-resistance. For the SiC JFET with blocking voltage of 1200V, the specific resistance of Transistor 1 is 12mΩ.cm^2 [12], which is smaller than Si limit value shown in Figure 1.2. However, as the gate is close to the drain, the Miller capacitance C_{gd} in this structure is big, which decreases the switching speed[4]. In comparison, in the structure shown in Figure 1.5(b) (Transistor 2), the current channel length between drain and source includes both the vertical channel length ($L_{\mathrm{V.}}$) and the lateral channel length ($L_{\mathrm{La.}}$), which is longer than Transistor 1 structure. Thus, the ON-resistance in Transistor 2 is big, with the same blocking voltage 1200V, the specific resistance of the Transistor 2 is 22 mΩ.cm^2 [12]. Nevertheless, as the gate is farther to the drain, the Miller capacitance in Transistor 2 is smaller than in Transistor 1, which helps to increase switching speed.



(a) Transistor 1 (b) Transistor 2

FIGURE 1.5: Two SiC JFET structures [11]

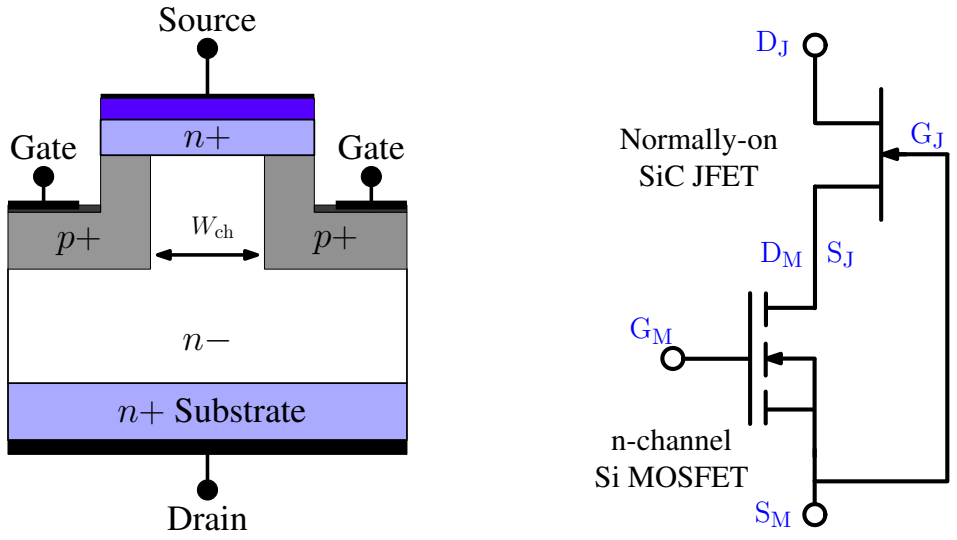
In power converters, normally-off [5] power transistors are always preferred for the security reasons. For normally-on devices, additional protection circuits are usually necessary in power converters to prevent the case like driver power supply is loss [13].

With this consideration, another vertical SiC JFET structure was proposed by Semisouth, which is illustrated in Figure 1.6(a) [14, 15]. By controlling the channel width W_{ch}, the device can be normally-on (with wide channel width) or normally-off (with narrow channel width).

Another solution to have a normally-off power transistor is the cascode configuration, which is shown in Figure 1.6(b) [16]. In this case, a normally-on SiC JFET is combined with an n-channel Si MOSFET. SiC JFET source (S_J) is connected to the Si MOSFET drain (D_M) while SiC JFET gate

[4]The role of C_{gd} in power device switching will be presented in Chapter 1.4.
[5]When gate and source is in short circuit, the transistor is blocked.

(G_J) is connected to the Si MOSFET source (S_M). By the control of the Si MOSFET, the turn-on and turn-off of the cascode device can be controlled. When the Si MOSFET is turned on, D_M and S_M is almost in short circuit ($V_{D_MS_M}$ is almost zero), thus the bias voltage between G_J and S_J is almost zero, so the SiC JFET is in ON state. The selected Si MOSFET is with low voltage and high current rating, of which the ON-resistance is small, so there is little power loss on the Si MOSFET when the cascode device is in conduction. When the Si MOSFET is turned off, V_{DS} across the Si MOSFET increases so as to put a negative bias voltage V_{GS} of the SiC JFET. Thus, the SiC JFET channel is blocked and it will withstand almost the whole blocking voltage.



(a) Vertical structure [14, 15] (b) Cascode configuration [16]

FIGURE 1.6: Normally-off JFET structure and configuration

Besides JFET, the MOSFET is another power transistor which is widely used in power converters. With the improvement technologies especially special oxidation techniques on SiC MOSFET [17], the first commercial SiC MOSFET existed since 2011 with blocking voltage to 1200V and nominal current to 32A ($T_j = 25°C$).

The smallest ON-resistance R_{DSon} of the three transistors given in Table 1.3 with the blocking voltage of 1200V and nominal current of 32A ($T_j = 25°C$) are compared in Figure 1.7. The SiC JFET is a normally-on device, of which the smallest R_{DSon} value is obtained when V_{GS} is 2V; while those are obtained for the SiC MOSFET and Si MOSFET when V_{GS} are 20V and 10V respectively. As shown in Figure 1.7, for power transistors of the same ratings, SiC power transistors have almost one fourth R_{DSon} values compared with Si power transistor. The inter-electrode capacitances[6] of each power transistor with $V_{DS} = 0V$ are also compared in Table 1.3, where SiC power transistors have much smaller capacitances than Si transistor.

[6]The inter-electrode capacitances of a power transistor will be described in details in 1.2.2

Apart from the previously presented physical property difference between Si and SiC, it is to be noted that the above difference among commercial power devices can be also due to the different active chip surface inside the packaging. For constructors, one motivation to develop WBG power devices is mainly to decrease the installed chip surface, so as to reduce the fabrication costs. Once the installed surface is decreased, power device inter-electrode capacitances can be reduced, thus it is very interesting for users to design high frequency power converters. However, power device R_{DSon} can be increased because of the decrease of the active chip surface. It can be seen in Figure 1.7 that R_{DSon} of a SiC MOSFET decreases four times in comparison with a Si MOSFET, however according to the relation shown in Fig. 1.2, theoretical R_{DSon} value of SiC devices can be reduced further. It also explains that WBG materials relative permittivity is a little smaller than Si material, however, inter-electrode capacitances of WBG power devices are much smaller than Si power device.

One application of WBG devices is to realize high frequency power converters, even though they have smaller inter-electrode capacitances, as they switch more than Si power devices at the same switching period, thus the power loss might increase. Therefore, the benefits of the WBG power devices can be exploited depending on specific use.

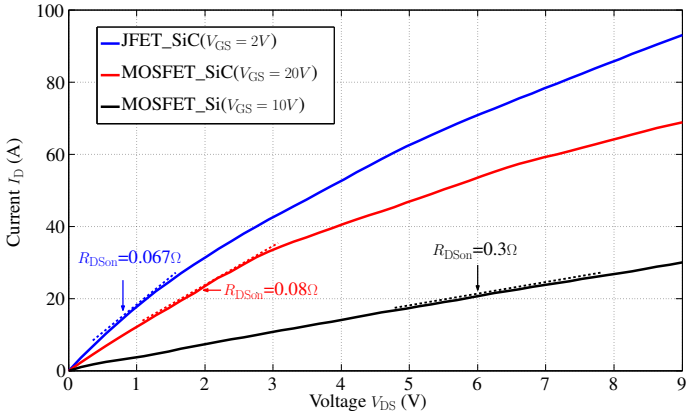


FIGURE 1.7: Different power transistors R_{DSon} comparison

TABLE 1.3: Different power transistors inter-electrode capacitances values comparison ($V_{\mathrm{DS}} = 0$V, $f = 1$MHz)

Reference	Type	C_{iss}(nF)	C_{oss}(nF)	C_{rss}(nF)
IJW120R070	SiC JFET	2	1.35	0.2
C2M0080120D	SiC MOSFET	1.4	1.4	0.5
IXFN32N120P	Si MOSFET	40	40	10

Besides unipolar power devices, bipolar devices are largely used in static converters for higher power ratings. The SiC bipolar power transistors are with the blocking voltage at least 1200V. In the laboratories test, the prototypes are even with the blocking voltages up to 10kV [18]. SiC Bipolar Junction Transistor (BJT) is currently commercialized with the blocking voltages up to 1700V. With the technical information reported by Fairchild, the $V_{\mathrm{CE}}(sat)$ voltages of the SiC BJT has been

greatly decreased in comparison with Si bipolar power transistors [19]. Thus, the ON-resistance of a 1200V/40A SiC BJT can be decreased to about $40m\Omega$. For another commercial 1200V/50A SiC BJT by GeneSic, the ON-resistance is reported to be $25m\Omega$. It is to be noted that there is a big DC current gain up to 60 for SiC BJT, which is much bigger than Si BJT. It is shown by authors in [20] that for a SiC BJT switching at 600V and 7A, the switching time is about 40ns and switching frequency can be up to 200kHz. Furthermore, there is almost no tail current observed. In this regard, SiC BJT is like a current controlled "unipolar" device with small conduction power loss.

It can be summarized that both SiC diodes and SiC power transistors are good competitors to Si power semiconductor devices at present. With the fabrication technology development, the SiC power devices with bigger power ratings can be achieved in the near future.

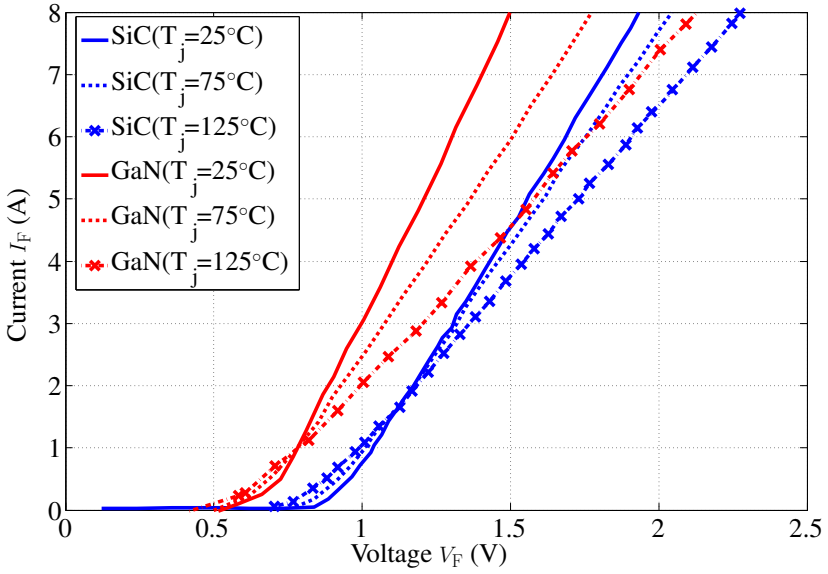


FIGURE 1.8: Static characteristics comparison between GaN diode (TPS3410PK) and SiC diode (C3D04060A)

The gallium nitride power semiconductor devices commercial development is later than that of SiC. Up until now, there are almost no GaN commercial diodes. They are still in the laboratories development. It is reported by Transphorm that the static characteristics of a 600V/6A GaN diode[7] (TPS3410PK) has smaller ON resistance than a commercial SiC diode (C3D04060A) with similar ratings[8]. The comparison of the static characteristics of both Schottky diodes is shown in Figure 1.8. It can be seen that for the same current conduction, there is less V_F in GaN diode than SiC diode, thus, conduction power loss can be further decreased. However, in their technical datasheets, there is more Q_c in the GaN diode (54nC) than in the SiC diode (8.5nC). It is to be noted that this GaN diode is almost the first commercial prototype and there are more than ten years development for SiC diode. It is reported by authors in [21] that with the GaN diode development results in laboratory, it is shown that both GaN and SiC diode have similar dynamic switching behavior and the inter-electrode capacitances in GaN Schottky diode is slightly smaller than in SiC diode.

[7]Shown in its technical datasheet, the nominal current at junction temperature $T_j = 125°C$ is 6A
[8]Shown in its technical datasheet, the nominal current at junction temperature $T_j = 125°C$ is 7.5A

Compared to SiC power transistors, GaN power transistors are more attractive, because the most popular transistor is GaN High Electron Mobility Transistor (HEMT). The structure of the device is shown in Figure 1.9 [7, 22], where the presence of AlGaN and GaN heterostructure creates a two-dimension electron gas (2DEG) which locates at the interface between AlGaN and GaN layers [7]. This 2DEG can double the GaN electron mobility from 1000 $cm^2/(V.s)$ to 2000 $cm^2/(V.s)$ [23]. With electron mobility increasing, GaN power device ON-resistance can be further decreased.

It can be noted that GaN HEMT is first widely commercialized in Radio Frequency (RF) domain. The structure of a normally-on GaN HEMT is shown in Figure 1.9. The normally-on GaN HEMT device can also be used as a "diode". The diode configuration shown in Figure 1.10 is to be commercialized by MicroGaN. The device is in cascode structure with a normally-on GaN HEMT and a Si-diode. The principle of this cascode device is similar to that presented in Figure 1.6(b). When the Si diode is in conduction, the V_{GS} of the GaN HEMT is almost 0V, so the normally-on GaN HEMT is in conduction; while the diode is blocked, V_{GS} of the GaN HEMT is negative biased, thus it is blocked to withstand the whole power source voltage. It is possible that the Si diode can be a Schottky diode with low voltage and high current, thus there is very small ON-resistance and inter-electrode capacitance of the diode.

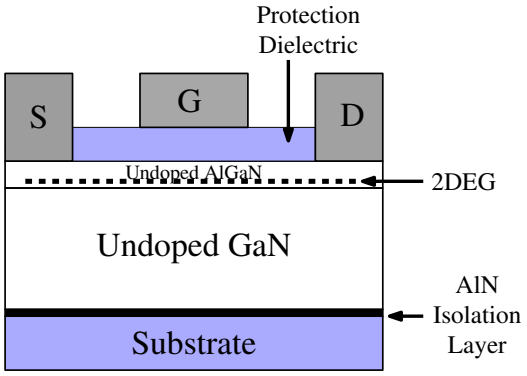


FIGURE 1.9: GaN-HEMT structure [7, 22]

To widely applicate GaN HEMT in power electronics domain, several GaN HEMT structures have been proposed to obtain a normally-off device [24]. One technology is recessed-gate technology, of which the AlGaN layer thickness under the Gate is widely decreased to stop creating 2DEG around Gate area [25, 26]. Thus, a positive threshold voltage V_{th} is needed to make GaN HEMT conduct. This structure is shown in Figure 1.11(a) [25, 26]. Another technology is to fabricate a Gate Injection Transistor (GIT), of which the structure is shown in Figure 1.11(b) [27]. Here, a p-AlGaN is formed at the gate to create a depletion area around the gate. In such a way, GaN HEMT normally-off operation can be achieved [27]. When V_{GS} is superior to V_{th}, holes are injected in the channel, which create the equal number of the electrons to flow from the source to drain, of which the conduction principle is like a MOSFET. A third technology is by implanting fluorine ions under the gate regions to form a normally-off GaN HEMT, which is reported by authors in [28]. Another way to have a normally-off GaN HEMT is in cascode structure as shown in Figure 1.6(b). This cascode structure is

commercially available at GaNSystems and Transphorm, and authors in [29] show that the switching times of this device are around $10ns$ when it switches at 400V and 10A.

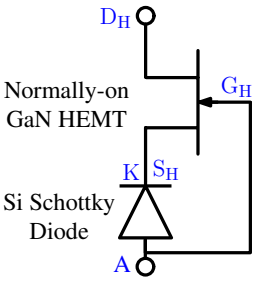
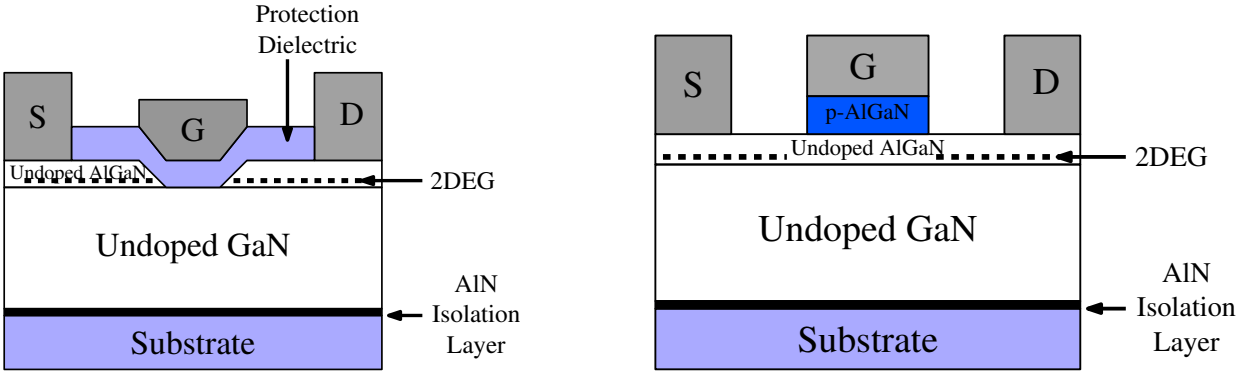


FIGURE 1.10: GaN diode in cascode structure



(a) Recessed gate structure [25, 26]

(b) GIT [27]

FIGURE 1.11: Two normally-off GaN HEMT structures

The comparison of a 200V/3A ($T_j = 25°C$) GaN HEMT (EPC2012) and a Si MOSFET (Si4490DY) with the same power rating is shown in Table 1.4. The R_{dson} for Si MOSFET is about $80m\Omega$ while that for GaN HEMT is about $67m\Omega$. There is much smaller inter-electrode capacitances for GaN HEMT than for Si MOSFET, which guarantees fast switching of GaN HEMT.

TABLE 1.4: 200V/3A Si MOSFET and GaN HEMT comparison (inter-electrode capacitances are compared when $V_{DS} = 100V$)

Reference	Type	V_F(V) ($I_F = 3A$)	C_{iss}(pF)	C_{oss}(pF)	C_{rss}(pF)
Si4490DY	Si MOSFET	0.24	1700	113	44
EPC2012	GaN HEMT	0.2	128	73	3.3

Another way to better exploit GaN materials advantages is the monolithic technology [30]. As reported by authors in [30], a GaN normally-off HEMT and a GaN diode is monolithically integrated in the same wafer to be used in a boost converter. This technology can greatly increase the power density and is important for power integrated circuits.

Nowadays, almost all GaN power transistors are in lateral structure, which limits the maximal power device blocking voltages and conduction current. In the near future, if GaN power device on vertical

structure can be developed [31], advantages of GaN power semiconductor devices can then be further exploited in the very high power converters.

Actually, for better using WBG power devices, besides from developping WBG power devices fabrication technologies, there are still following challenges: power devices packaging to make power devices operate in high temperature [32, 33]; passive power components associated in the power circuits to be allowed operating at high frequency, high voltage, high current and high temperature; and the design of the Electromagnetic Compatibility (EMC) filters to resolve the electromagnetic interference (EMI) problem due to the fast switching of the WBG power devices [34].

The wide bandgap materials and different WBG power semiconductor devices have been presented in this section. As SiC and GaN power semiconductor devices are relatively new, it is necessary to first characterize them for a better use.

1.2 WBG Power Devices Characterization

Power semiconductor devices characteristics can be represented by static and dynamic characteristics. In this section, first, state of the art on WBG power semiconductor devices static characteristics measurement will be presented, which is followed by a survey on how to determine WBG power device dynamic characteristics.

1.2.1 Static characteristics

In the first time, diode static characteristics will be presented; afterwards, those of transistors are to be stated.

The static characteristics of a power diode can be divided according to the conditions when the diode is conducting or blocked. When a diode is in conduction, the static characteristic represent the relation between the forward voltage and the conduction current, which is already shown in Figure 1.8 for a SiC and a GaN diodes. The forward characteristic is usually temperature dependent. The diode conduction loss can be calculated when knowing these characteristics. When a diode is turned-off, the static characteristics represent the relation between the reverse leakage current I_R and blocking voltage V_R, which is represented in Figure 1.12 for the GaN diode (TPS3410PK) and SiC diode (C3D04060A). The reverse characteristic is also temperature dependent. As mentioned in Chapter 1.1.2, generally, in OFF state, the WBG power diodes have bigger leakage current than Si power diodes. With the technology improvement by reducing the leakage current, the blocking voltages of the WBG power diodes can be further increased.

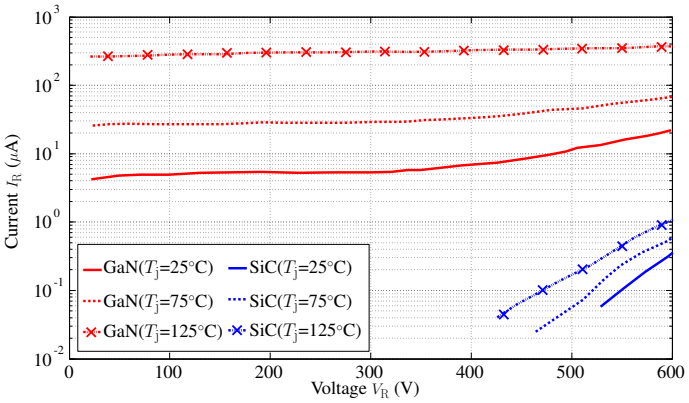


FIGURE 1.12: GaN diode (TPS3410PK) and SiC diode (C3D04060A) static characteristics in OFF state

Temperature is a key factor that influence the power diode static characteristics. When diode is in ON state, junction temperature T_j can be estimated by the equation 1.1:

$$T_j = T_m + R_{th} \times P, \tag{1.1}$$

where T_m is the measured temperature, R_{th} is the equivalent thermal resistance from junction to the measurement point and P is the power dissipation in the junction. If the temperature is measured at the point shown in Figure 1.13, R_{th} can be calculated in equation 1.2,

$$R_{th\_tot} = R_{th(j-c)} + R_{th(c-s)} + R_{th(iso)}, \tag{1.2}$$

where, it equals to the sum of the thermal resistance from junction to case $R_{th(j-c)}$, the thermal resistance from case to heat sink $R_{th(c-s)}$ and the thermal resistance of the isolation material $R_{th(iso)}$ if they are used.

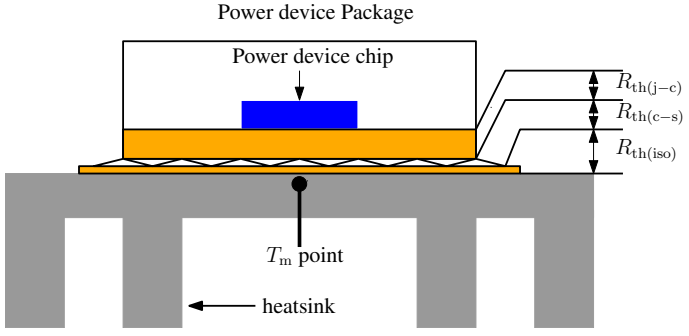


FIGURE 1.13: Equivalent thermal resistance of a power device mounted on a heatsink

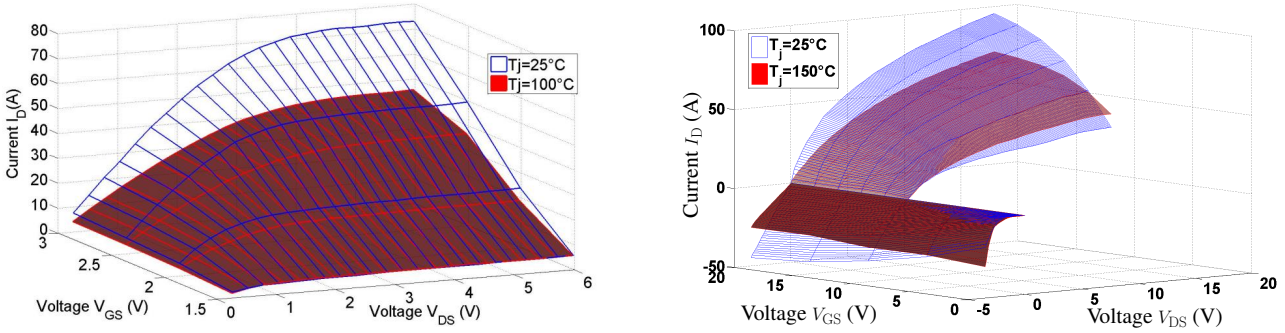
For a GaN diode (TPS3410PK) in TO-220 package mounting on a heatsink, $R_{th(j-c)}$ is 1.8 °C/W, and $R_{th(c-s)}$ for is about 0.5 °C/W, while $R_{th(iso)}$[9] is about 3 °C/W. Thus, R_{th_tot} is 5.3 °C/W. With the GaN diode static characteristics shown in Figure 1.8, when it conducts its nominal current 6A,

[9]With Sil-pad 400 isolation material of which the thermal resistance is 0.45 °C.in^2/W

the power dissipated in the junction is about 10W, which means that there is a 53 °C temperature difference between T_{m} and T_{j} when the diode conducts nominal current continuously.

If the power diode is not mounted onto a heatsink, R_{th} in this case equals to the thermal resistance from junction to the ambient $R_{\mathrm{th(j-a)}}$. For the same GaN diode, $R_{\mathrm{th(j-a)}}$ is 62 °C/W, which is much bigger than $R_{\mathrm{th\_tot}}$ in equation 1.2. This shows that without a heatsink, it is very difficult to measure the diode static characteristics with its nominal current.

For a WBG power transistor, the static characteristic represents that at one T_{j}, the evolution of the drain current I_{D} in function with the gate source voltage V_{GS} and the drain source voltage V_{DS}. The static characteristics of a SiC JFET 1200V/40A and a SiC MOSFET 1200V/32A varying with different T_{j} are represented in Figure 1.14. As shown in Figure 1.14(b), nowadays most WBG power transistors are unipolar power devices, they can conductor both on 1st and 3rd quadrant (reverse conduction with $V_{\mathrm{DS}} < 0$ and $I_{\mathrm{D}} < 0$).



(a) SiC JFET (SJEP120R063)

(b) SiC MOSFET (C2M0080120D)

FIGURE 1.14: SiC JFET (SJEP120R063) and SiC MOSFET (C2M0080120D) static characteristic at different T_{j}

For the presented SiC JFET, it is shown that I_{D} decreases at the same V_{GS} and V_{DS} when the temperature increases, which is negatively temperature dependent. This characteristic shows that the presented SiC JFET can easily be connected in parallel to further increase conducted current [35]. While for SiC MOSFET, when V_{GS} is inferior to 14V, I_{D} is positively temperature dependent and only when V_{GS} superior to 14V, I_{D} becomes negatively temperature dependent. The static characteristics of a Si MOSFET 1200V/32A (IXFN32N120P) is compared with the SiC MOSFET (C2M0080120D) in Figure 1.15. As shown in this Figure, first, the ohmic region and linear region can be separated clearly in the static characteristics of the Si MOSFET while it is not clear for the SiC MOSFET. This difference will lead to different V_{GS} waveform during the switching, which will be presented in Chapter 1.4.

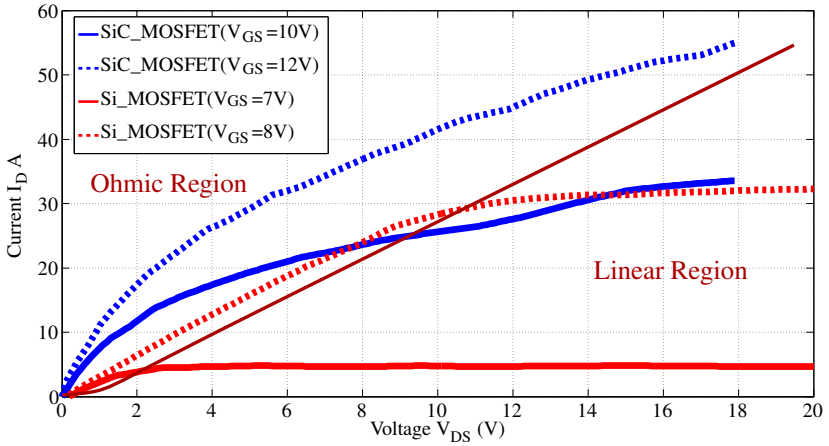


FIGURE 1.15: SiC MOSFET (C2M0080120D) and Si MOSFET (IXFN32N120P) static characteristics comparison

If power transistor is characterized when power dissipates continuously in the junction, with the measurement setup shown in Figure 1.13, because of the thermal resistance value, the power dissipation is limited to several tens of watts which is much smaller than SiC MOSFET power ratings (1200V/32A for C2M0080120D). As expressed in equation 1.2, in order to increase power dissipation, it is necessary to decrease R_{th} value. It is shown in Figure 1.16 the relation between the pulsed power duration (t_{p}) with the junction to case thermal impedance $Z_{\text{th(j-c)}}$ of SiC MOSFET at different duty cycles. When the pulse duration is longer than 0.1s, which is bigger than power device thermal time constant, therefore at any duty cycle value, $Z_{\text{th(j-c)}}$ equals to $R_{\text{th(j-c)}}$, which is a constant 0.6°C/W value. However, at single pulse condition, when the pulse duration is shortened to 10μs, which is much smaller than power device thermal time constant, $Z_{\text{th(j-c)}}$ decreases from 0.6°C/W to 0.005 °C/W, which means that at this condition the characterization can be done with a hundred time bigger power dissipation in the power device junction than at continuous state.

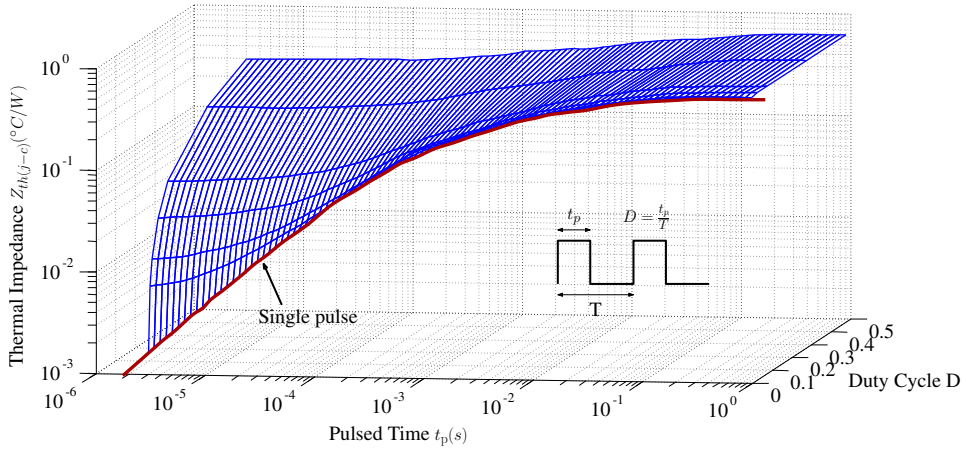


FIGURE 1.16: SiC MOSFET (C2M0080120D) transient thermal impedance

The commercial curve tracer is based on this principle to characterize the power devices on single pulse. Author in [3] presented the static characteristics of a SiC JFET (1500V, 4A) by using a commercial curve tracer. The maximal dissipated power in the SiC JFET is 240W (20V, 12A),

while it is able to characterize the power device from 25°C to 225°C. The characteristics of the same device is further reported by authors in [36, 37] to research on its dependency on temperature for high temperature application. Authors in [38] presented a 1200V, 27A normally-on SiC JFET characteristics both on 1st and 3rd quadrant for the design of a power converter. Author in [39] presented I_D at different V_{GS} voltages in the linear region—the transfer characteristic—for a normally-on SiC JFET. The maximal dissipated power in the characterization is about 684W (57A,12V) while the power device power rating is 1200V, 75A. The static characteristics of a SiC MOSFET (1200V, 20A) was presented by authors in [40] by using a similar curve tracer, while the maximal dissipated power in the device is about 49W (7V, 7A).

For the GaN HEMT, a current collapse phenomena is observed and reported by authors in [41, 42]. This phenomena leads to a different I_D-V_{DS} static characteristics when the power device is characterized in DC state and in pulsed mode. Authors in [42] reported that an anticlockwise hysteresis was observed in I_D-V_{DS} plot when the device is characterized in pulsed mode with certain gate bias voltage. This phenomena can decrease the overall power rating and power efficiency in power converters. Fortunately, with the GaN HEMT device fabrication technology improvement, the use of field plate in the device [43] and new passivation techniques [44] can almost remove current collapse phenomena and greatly improve GaN HEMT performance. It is shown by authors in [45] the static characteristics of a GaN HEMT in cascode structure (similar to that shown in Figure 1.6(b)) with maximal power dissipation of 400W (8V, 50A) while the power rating for the device is 600V, 17A.

It can be seen that even with the commercial curve tracer, the power dissipation in the power device is still limited to avoid the device auto heating. In our thesis work, a static characterization circuit based on single pulse method is applied to characterize WBG power devices. The objective is to increase the power dissipation in the power device junction so as to characterize power device in a large operation zone. More details will be presented in Chapter 2.1.

1.2.2 Dynamic characteristics

The dynamic characteristics of the power semiconductor device are represented by the evolution of power device inter-electrode capacitances, which influence directly power device switching behaviors.

In the diode structure shown in Figure 1.17, the contact of the PN junction creates a space charge region, and forms a junction capacitor C_j. In the diode, C_j is a nonlinear capacitor and its value decreases when the diode blocking voltage increases.

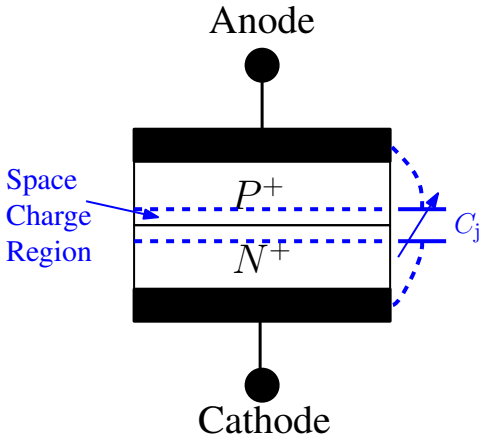
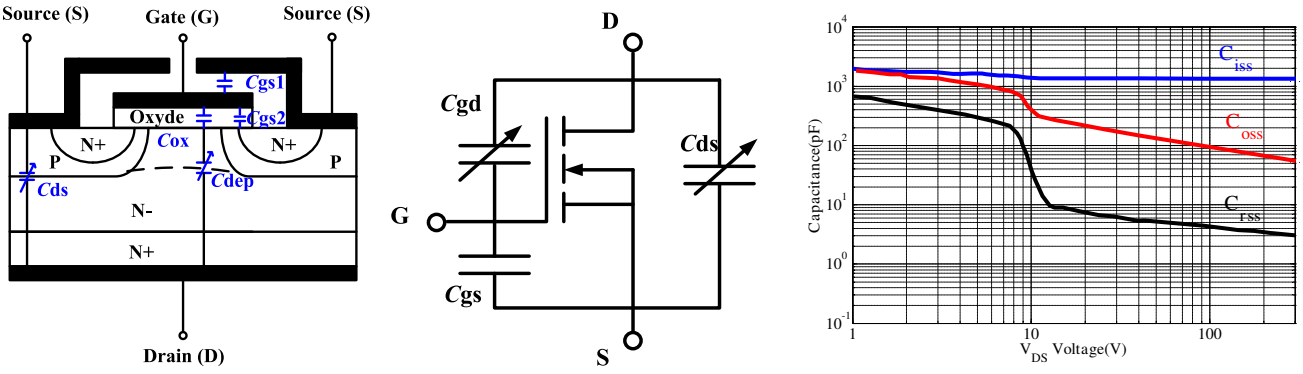


FIGURE 1.17: Junction capacitor of a diode

The junction capacitors can be found also in power transistors. Figure 1.18 shows the structure of a MOSFET and its equivalent inter-electrode capacitances: C_{gd}, C_{gs} and C_{ds}. These capacitances are generally voltage dependent [46]. They not only play an important role on the power device commutation (notably influencing switching losses), but also are involved in the parasitic resonances that occur at the end of the turn-off commutation (thereby influencing the overall spectrum of electromagnetic noise level [47] (EMC aspects)). How to characterize these capacitances determines the accuracy of the power devices models [48, 49].



(a) MOSFET structure (b) Equivalent inter-electrode capacitances (c) Capacitance values (IRFB9N60A)

FIGURE 1.18: Structure of MOSFET and its equivalent inter-electrode capacitances [50]

In the datasheet of a power semiconductor device, instead of being given separately the values of these capacitances, the following values are given as: the input capacitance $C_{iss} = C_{gd} + C_{gs}$, the output capacitance $C_{oss} = C_{gd} + C_{ds}$, and the reverse transfer capacitance $C_{rss} = C_{gd}$. As shown in Figure 1.18(c) with datasheet values of a MOSFET IRFB9N60A, these capacitances are generally dependent on V_{DS} voltage and some are dependent both on V_{GS} and V_{DS}.

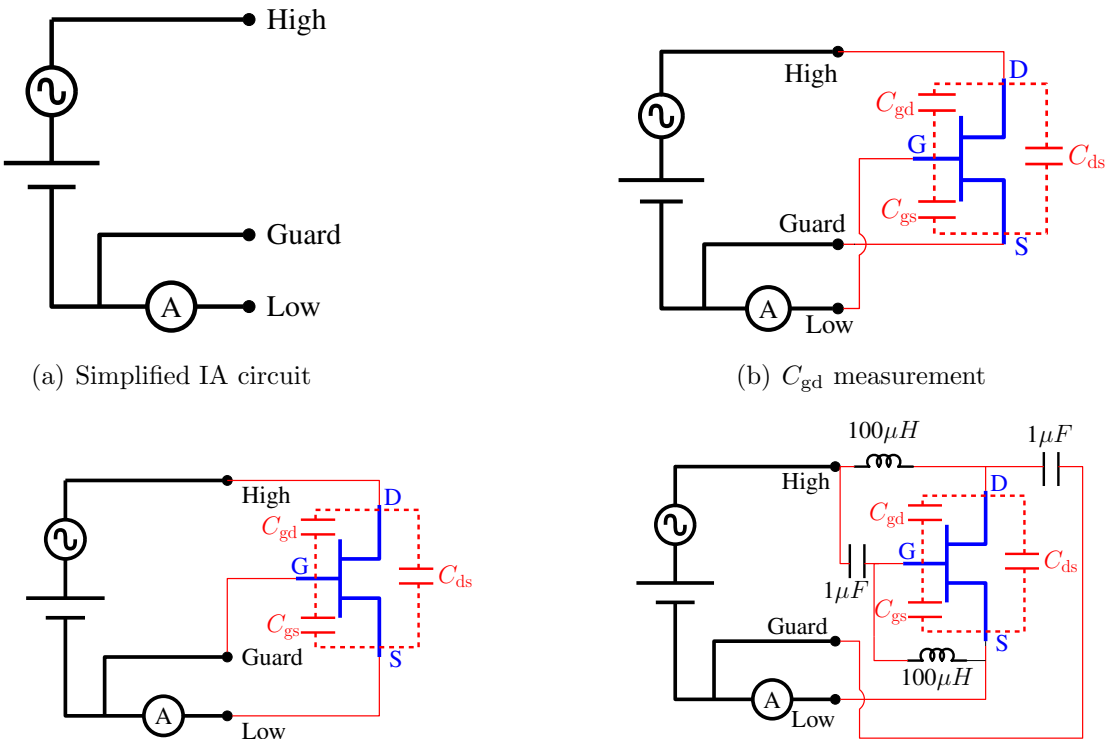
For a power device operating under several hundred volts or even above one thousand volts, these values are usually given for only a few dozen volts of V_{DS} in the datasheets of a Si MOSFET or Si IGBT. Thus, the question is how the evolution of these capacitances can be precisely predicted in

high voltage? Even if in a datasheet of WBG power devices, the evolution of these capacitances in high voltage are provided by manufacturers, can these values be reliable? It is not rare that the characteristic of a power device does not follow the exact information given in a datasheet, especially for SiC and GaN power devices whose datasheets are often preliminary and can be updated within a few months. It also needs to be noted that C-V_{DS} curves in datasheets are not always given in logarithmic-logarithmic coordinates. Due to the strong nonlinearity of these inter-electrode capacitances, their value in high voltage can be more than a hundredfold smaller than that in low voltage, which makes it impossible to get accurate information in linear coordinate. Moreover, in the technical datasheets, C-V_{DS} curves are always given for one V_{GS} voltage. Therefore, it is necessary to develop a simple method to characterize these capacitances.

To achieve the objective of the power device inter-electrode capacitances measurement, there are several methods which are to be presented in the following paragraphs.

The method proposed by Agilent [51] is to use an impedance analyzer (IA). There is a Guard connection in the impedance analyzer, of which the measurement circuit can be simplified in Figure 1.19. The impedance of the amperemeter can be considered to be zero.

With the use of Guard in impedance analyzer, each inter-electrode capacitance can be characterized directly, of which the measurement configuration is shown in Figure 1.19.



(a) Simplified IA circuit

(b) C_{gd} measurement

(c) C_{ds} measurement

(d) C_{gs} measurement

FIGURE 1.19: Power transistor inter-electrode capacitances measurement by impedance analyzer [51]

- C_{gd} measurement circuit is shown in Figure 1.19(b), in which V_{GS} is in short-circuit to keep the power transistor in OFF state. V_{DS} is obtained by the impedance analyzer internal DC power source. The AC current flows through C_{ds} and C_{gd}, however only the current flowing through C_{gd} is measured by the impedance analyzer. Thus, C_{gd} values can be characterized.

- C_{ds} measurement circuit is shown in Figure 1.19(c), of which the principle is similar to C_{gd} measurement. The impedance analyzer measures only the AC current flowing through C_{ds}.

- C_{gs} measurement circuit is shown in Figure 1.19(d). A 100μH inductor is connected between High and D of the power transistor. This inductor makes High and D short-circuit in DC which guarantees a DC polarization between D and S. Its impedance in megahertz range is much bigger than that of the 1μF capacitor between High and G to withstand the bias DC voltage, which allows that the AC current flows through the capacitor. Another 100μH inductor between G and S is in the same principle to make G and S in short-circuit in DC and high impedance in AC (much bigger than C_{gs} impedance in megahertz range), so that V_{GS} is kept zero during the measurement to make sure the power device in OFF state and the AC current then flows through C_{gd} and C_{gs}. The AC current flowing through C_{gs} is measured by the impedance analyzer while that flowing through C_{gd} then passes through the 1μF capacitor between D and Guard, because its impedance is much smaller than that of the C_{ds}. This capacitor also helps to block the DC voltage between High and Guard. Thus, with this configuration, the values of C_{gs} in series with 1μF capacitor are finally obtained, as C_{gs} is much smaller than 1μF, its value is characterized.

The above measurement configuration can be applied to any normally-off power transistor. The advantage of the measurement by impedance analyzer is that the circuit configuration is simple and it is accurate to predict these capacitances values around 1MHz with the evolution of V_{DS}. However, the impedance analyzer is typically limited to 40V for the V_{DS} bias value. In order to increase V_{DS} bias value and measure inter-electrode capacitances in a higher voltage, the authors in [52, 53] connect an extra high voltage power source and a DC blocking capacitor between the power source and the impedance analyzer, which helps to characterize C_{iss}, C_{oss} and C_{rss} values with V_{DS} up to 250V.

Another method proposed by authors in [54] is to use an LCR meter, in which an extra power source combined with many passive components is used in the measurement configuration. It is able to use this method to characterize each inter-electrode capacitance directly, but as there are so many passive components used, the measurement frequency range is decreased to about 100kHz in this method.

The authors in [55] adopted a measurement method based on Time-Domain Reflectometry (TDR) principle, in which an oscilloscope is connected in the measurement circuit with a 50Ω coaxial cable

to measure the reflected signals while an extra power source is used to increase the bias V_{DS} value. When inter-electrode capacitance is inferior to $10pF$, this method is not able to correctly characterize the capacitance values.

The measurement equipments used in the above methods are impedance analyzer, LCR meter, oscilloscope respectively. In our thesis, another measurement equipment—vector network analyzer together with current probes—is used, which provides a new characterization method of the power device inter-electrode capacitances. Compared to the above methods, the main advantage of the proposed method is that it can isolate the measurement equipment from the high voltage so as to reduce risk in practical use. Furthermore, the measurement circuit configuration is quite simple.

The principle of the method by using current probes was proposed by authors in [56] to measure power line impedance, in which two current probes are used for the power line impedance measurement. The basic setup of this method to measure an unknown impedance Z_x is illustrated in Figure 1.20. The measurement setup is constituted of a vector network analyzer, a current injection probe (CIP) and a current receiving probe (CRP). The principle of this method is that one current probe injects a current in the measurement circuit and another current probe receives this current. With the calculation on S parameters, the unknown Z_x can be characterized. This method was applied by authors in [57, 58] for the noise source impedance measurement of a converter. The L2EP research work presented in [34, 59] has developed this method and showed that the current probes volumes can be decreased by choosing proper magnetic materials. Thus, the sensibility of the measurement method has been increased and the frequency validity of the method is up to 30MHz. More details of this method by using current probes to characterize WBG power device inter-electrode capacitances are presented in Chapter 2.2.

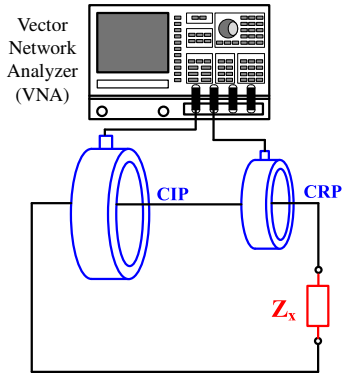


FIGURE 1.20: Measurement configuration with two current probes and vector network analyzer

Different characterization methods of the power device static characteristics and dynamic characteristics are presented in this section. Now, the WBG power devices models can be built based on those characterization results, which will be presented in the next section.

1.3 WBG Power Devices Modeling

Generally, there are physical models and behavioral models for semiconductor power devices. In this section, first, a survey on WBG power device physical models will be presented; then, state of the art on the behavioral models will be detailed.

1.3.1 Physical models

The power device physical models can be divided according to physical equations models (PHEM) and extracted parameters models (EXPM).

PHEM aims at developing physical equations to express power devices characteristics.

Authors in [60] presented a SiC diode model which can express electrothermal behaviors and which validated on different SiC SBD, p-i-n, and JBS diodes. However, not all the physical parameters in this model are easy to get. Authors in [61] presented an analytical model to express a SiC diode reverse recovery phenomena, which shows good agreements with numerical simulation and measurements. Nevertheless, it demands designers an excellent knowledge of semiconductor physics to well use this analytical model. Physical equations to express SiC JFET drain current are developed by authors in [62], in which the physical model represents well a SiC normally-off JFET. Authors in [63] developed physical equations to model normally-off JFET I_D-V_{GS} characteristics. The model showed its robustness for power devices with different structures. However, it is necessary to know the parameters like gate region doping, drift region channel length etc. which relates to the power device fabrication process and they are not available for power device users.

It can be seen that PHEM can well represent power device characteristics and switching behaviors, but those models are generally too complicated to be developed by users. Simulation is usually time consuming [64]. To keep the advantage of PHEM like precision and improve its drawback like complexity, EXPM is developed by researchers to build a power device physical model. The parameters of EXPM can be found either on power device technical datasheets or on power devices static and dynamic characteristics measurement. There are the following two ways to apply the extracted parameters:

1. The parameters can be extracted in order to apply in power device classical models which are based on physical equations in circuit simulation softwares like PSPICE or Saber.

2. If classical power device physical models in circuit simulation software need to be adapted to WBG power devices, then the extracted parameters are intended to be employed in those adapted physical models.

TABLE 1.5: Extracted parameters by authors in [65] for a normally-on SiC JFET

Parameters	Meaning	Unit	Extraction ways
VTO	Threshold voltage	V	Static characteristics
BETA	Transconductance coefficient	A/V^2	Static characteristics
LAMBDA	Channel-length modulation	V^{-1}	Static characteristics
IS	Gate p-n saturation current	A	Static characteristics
VTOTC	VTO temperature coefficient	V/°C	Static characteristics
BETATCE	BETA temperature coefficient	$°C^{-1}$	Static characteristics
CGS	zero-bias gate-source p-n capacitance	F	Dynamic characteristics
CGD	zero-bias gate-drain p-n capacitance	F	Dynamic characteristics
RD	Drain ohmic resistance	Ω	Impedance measurement
RS	Source ohmic resistance	Ω	Impedance measurement
PB	Gate p-n potential	V	By default
M	Gate p-n grading coefficient	-	By default
FC	Forward-bias depletion capacitance coefficient	-	By default
XTI	IS temperature coefficient	-	By default
KF	Flicker noise coefficient	-	By default
AF	Flicker noise coefficient	-	By default

In the first case, the power device models in PSPICE are generally based either on U.C.Berkeley SPICE models for diode and MOSFET [66], or on Hefner model for IGBT [67, 68]. Those models are developed for Si power devices. Authors in [65] showed that a Si JFET model in PSPICE can be used to model a normally-on SiC JFET. The parameters can be extracted from several measurements to characterize JFET static characteristics, dynamic characteristics, temperature dependent characteristics and several parameters can be the default values in the software. For this JFET, the parameters are summarized in Table 1.5 [65].

It is reported by author in [69] that the parameters of a Si IGBT in PSPICE can be extracted by using a fitting program to make sure that the device static and dynamic characteristics correspond well with power devices characteristics either from datasheet or from the measurement. The same method is applied by authors in [53] to model a SiC MOSFET in Saber by using a Si MOSFET modeling tool in the software, and the parameters are extracted by using a visual curve-fit tool.

The advantage to build an EXPM is that there is no need to develop physical equations. Major power device parameters can be extracted in an relatively easy way either from the datasheet or from the measurement. However, this method is limited by physical equations for Si power devices. If the classical power device models can not fully represent power device characteristics, the difference between the simulation and measurement is always existing. For example, it is reported by authors in [70] that when MOSFET or IGBT is negatively biased, the capacitive coupling effect between gate and drain is lost. However, this phenomena is not included in PSPICE classical MOSFET and IGBT models.

The classical Si power devices models are enhanced to be better adapted for WBG power devices. It is reported by author in [3] that Si JFET model in PSPICE needs to be modified to represent a normally-on SiC JFET with the structure shown in Figure 1.5. Thus, new parameters can be extracted based on the power device characterization for the modified physical equations. It is reported by authors in [71] to add the SiC material temperature dependent properties in the classical MOSFET model to represent a SiC MOSFET. And the loss of the capacitive coupling effect when gate negatively biased is also added in this model. Authors in [72] described a gradual drain current transition from ohmic region to linear region (which is illustrated in Figure 1.14(b)), which is better adapted to model a SiC MOSFET. Furthermore, all the necessary parameters in this model are from SiC MOSFET datasheet, which makes an easy extraction procedure. Authors in [73] presented newly developed physical equations for SiC diodes, in which all the parameters can be extracted from SiC diodes datasheets. The method can be applied on different diodes with different power ratings.

Power device physical models can represent power device characteristics precisely. However, no matter PHEM or EXPM, physical equation development is a key factor. In comparison with physical models, power device behavioral models are more applicable, because mathematically no-physical-meaning equations and fitting programs can be used to make models that represent well power devices behaviors.

1.3.2 Behavioral models

A power diode can be generally modeled with the equivalent circuit shown in Figure 1.21. Current generator I_{D} and R represent the static characteristics of the diode and C_{j} is a non-linear capacitance which represents the junction capacitance when the diode is blocked and diffusion capacitance to store the charge when the diode is in conduction.

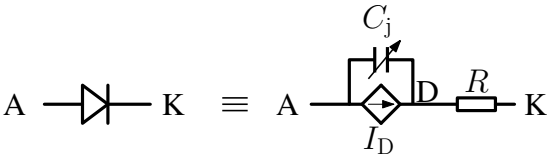


FIGURE 1.21: Power diode equivalent circuit

Authors in [74–76] represented Si, SiC and GaN diode models respectively with the above equivalent circuit. The basic expressions of the I_{D} current when diode is in conduction and the C_{j} capacitance when the diode is blocked are from the following classical physical equations:

$$I_{\mathrm{D}} = I_{\mathrm{s}} \left[\exp\left(\frac{qV_{\mathrm{AD}}}{NkT_{\mathrm{j}}} \right) - 1 \right] \tag{1.3}$$

where k (1.38×10^{-23} J/K) is Boltzmann constant, q (1.6×10^{-19} C) is elementary charge and T_j (K) is the junction temperature.

$$C_j = \frac{C_{\mathrm{j0}}}{\left(1 + \frac{V_{\mathrm{KA}}}{V_{\mathrm{j}}}\right)^m} \tag{1.4}$$

I_{s}, N, C_{j0}, V_{j} and m can be fitted to express each diode static and dynamic characteristics.

Generally, for a power diode, the junction capacitor is characterized to be modeled as a nonlinear capacitor in the diode [75], few work is done to characterize the capacitor nonlinearity when the device is in conduction. R is usually a resistance with constant value, and few work is done to report its nonlinearity. In our thesis work, diode behavioral models are build which are based on its dynamic impedance characterization. More details can be found in Chapter 3.1.

A power transistor can be generally modeled with the equivalent circuit shown in Figure 1.22. A current generator represents the power transistor static characteristics and the dynamic behaviors are modeled by three non-linear capacitors C_{gd}, C_{ds} and C_{gs}.

The nonlinearity of the current generator and those capacitors are modeled by mathematical equations. Based on the equivalent circuit shown in Figure1.22, authors in [77] introduced several non-physical parameters to model SiC MOSFET static and dynamic characteristics dependency on T_{j}, which makes the model operate in a wide temperature range. Mathematical equations are developed by author in [78] to describe the nonlinear behavior of those inter-electrode capacitances with V_{DS} evolution. Authors in [29] use the same transistor equivalent circuit to represent a cascode GaN-HEMT in order to research on power loss during the switching. Authors in [79, 80] represent a SiC diode and a GaN HEMT with the above power device equivalent circuits in a buck converter to obtain power devices switching waveforms, power loss [79] and the influence of the parasitic elements on switching behavior [80]. GaN HEMT behavioral models which are based on the equivalent circuit shown in Figure 1.22 are proposed by EPC manufacture. In their models, the non-linear capacitors are modeled in the form of the charges Q_{gs}, Q_{ds} and Q_{gd}. The evolution of the charges is expressed by mathematical equations.

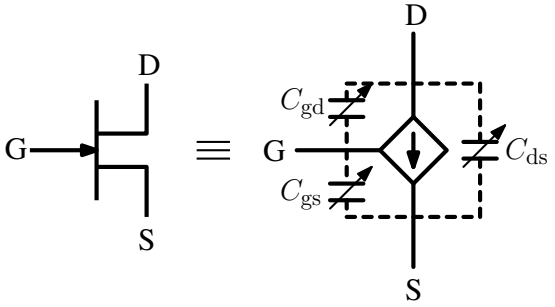


FIGURE 1.22: Power transistor equivalent circuit

The power device behavioral models are more applicable to different circuit simulation softwares. In order to improve their accuracy, it is necessary to correctly characterize power devices in different operation conditions.

The nonlinearity of the inter-electrode capacitances C_{gd}, C_{ds} and C_{gs} is usually modeled with V_{DS} evolution [77, 78]. It is reported by authors in [81–83] the influence of both V_{GS} and V_{DS} on inter-electrode capacitances values. Few work is done to report how to characterize the power transistor inter-electrode capacitances evolution when the power device is in linear region. In our thesis work, inter-electrode capacitances of power transistors are characterized not only when the power device are blocked but also when they are in linear region. A SiC JFET behavioral model is built with all those capacitance nonlinearity. More details are reported in Chapter 3.2.

WBG power devices physical models and behavioral models have been presented in this section. These models can be used in circuit simulation to study WBG power devices driver strategy, which will be presented in the following section.

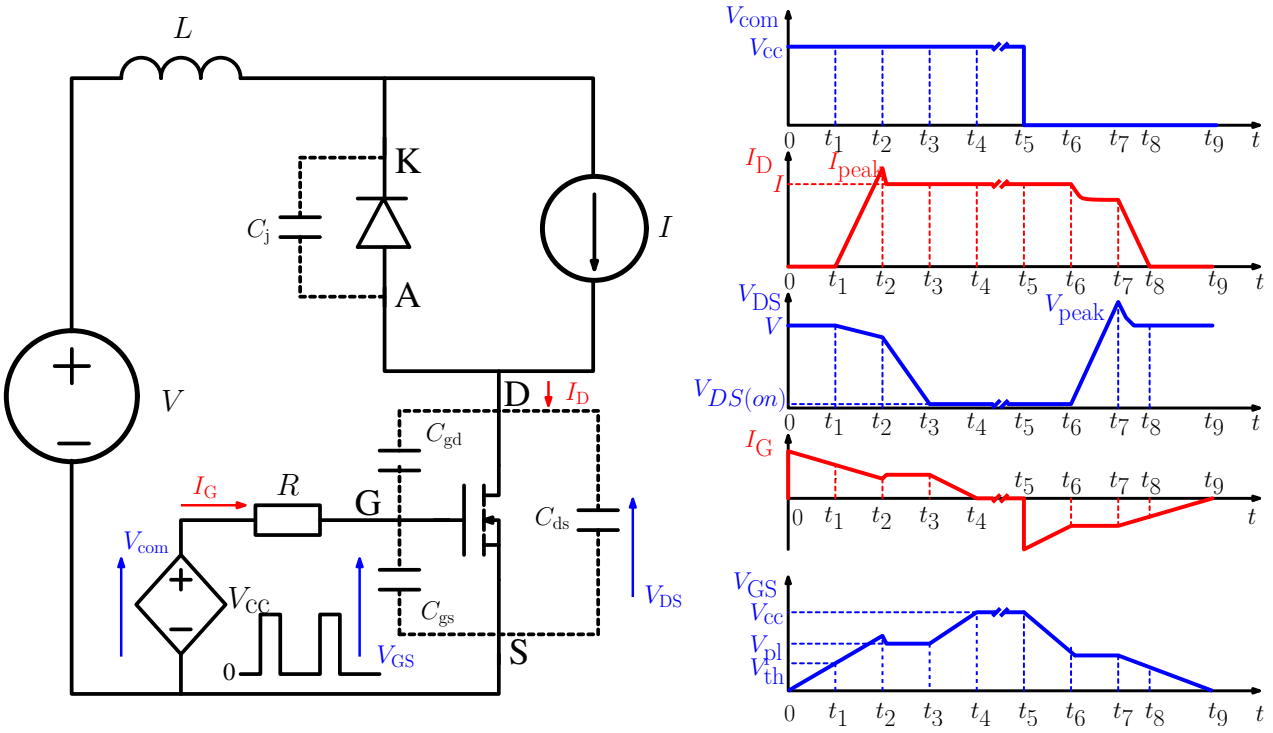
1.4 WBG Power Devices Driver

In this section, first, Si MOSFET commutation process will be detailed and then different driver technologies of Si and WBG power transistors are presented. As the knowledge of how to control power transistors switching is important for the purpose of electromagnetic interference reduction, this will be presented in the third part of this section.

1.4.1 Si MOSFET commutation process

A MOSFET buck converter circuit is shown in Figure 1.23(a). It is constituted with a current source as the load, a voltage source as the input power source, a diode, a MOSFET with inter-electrode capacitances, parasitic inductance L of the commutation mesh and the driver circuit.

It is shown in Figure 1.23(b) the switching waveforms of the command voltage V_{com}, drain current I_D, drain-source voltage V_{DS}, gate current I_G and MOSFET gate voltage V_{GS} during the turn-on and turn-off switching. It can be divided on four main steps in MOSFET turn-on, and each step is illustrated on Figure 1.24.



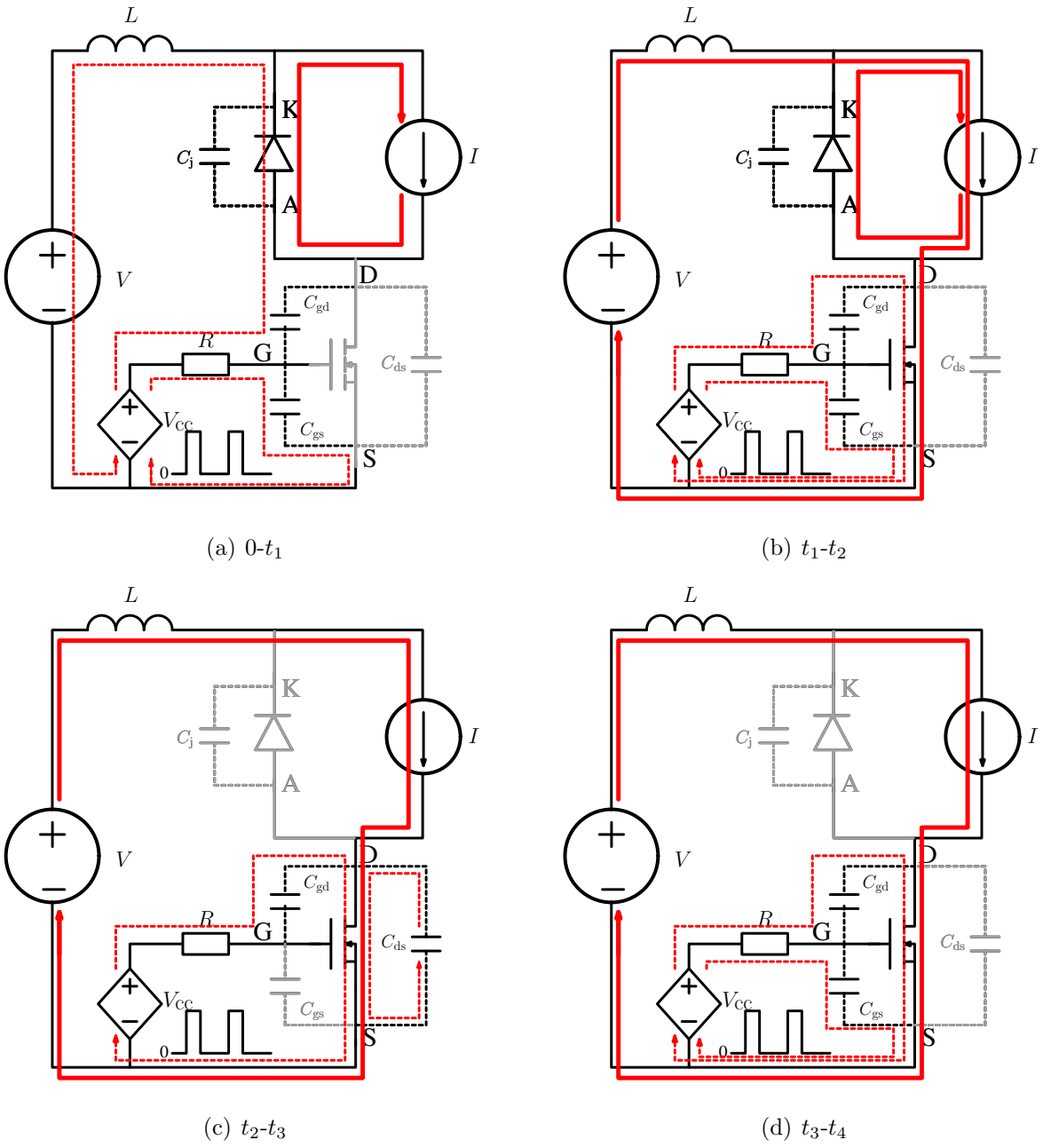
(a) MOSFET commutation mesh

(b) MOSFET turn-on and turn-off switching waveforms

FIGURE 1.23: MOSFET buck converter and switching waveforms

1. $\mathbf{0 - t_1}$ The current loops are illustrated in Figure 1.24(a) for the first step. V_{com} turns to V_{cc} immediately, which induces a current $I_G = \frac{V_{cc}-V_{GS}}{R}$ to charge both C_{gd} and C_{gs} of the MOSFET, which leads to the increase of the V_{GS}. At t_1, V_{GS} rises to the MOSFET threshold voltage V_{th}.

2. $\mathbf{t_1 - t_2}$ (shown in Figure 1.24(b)) When V_{GS} is superior to V_{th}, MOSFET begins to conduct the current. There is current flowing through the parasitic inductance L, which gives rise to a voltage $L\frac{dI}{dt}$ across the L. That makes V_{DS} decrease to $V - L\frac{dI}{dt}$, which is represented graphically in Figure 1.23(b). The increase of I_D makes the current flowing through the diode decrease at the same slope. When diode current decreases to zero, the diode begins reverse recovery. At t_2, I_D arrives at a peak value which equals to the sum of the load current I and diode maximal reverse recovery current. In this step, C_{gd} and C_{gs} are still be charged by I_G, thus V_{GS} continues to increase.



(a) 0-t_1 (b) t_1-t_2

(c) t_2-t_3 (d) t_3-t_4

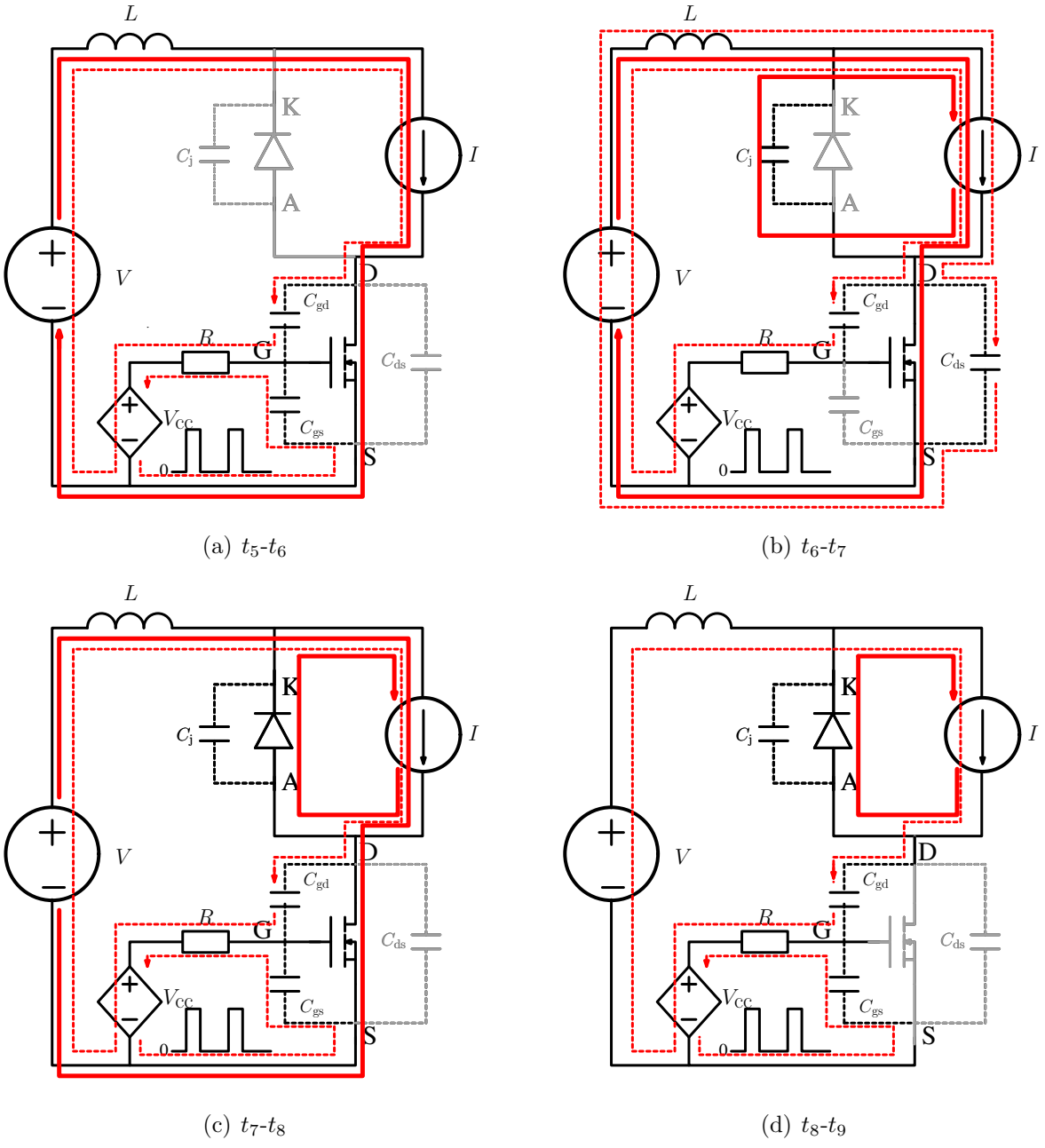
FIGURE 1.24: MOSFET turn-on switching process

3. $\boldsymbol{t_2 - t_3}$ (shown in Figure 1.24(c)) The diode finishes the reverse recovery at the beginning of this step[10]. I_D drops from I_{peak} to I, thus V_{GS} drops slightly. C_{ds} and C_{gd} begin to discharge, the discharge of the two capacitors makes V_{DS} and V_{DG} decrease. Thus, via C_{gd}, the decrease of V_{DG} plays a negative feedback on V_{GS}, thus, I_G no more charges C_{gs}, which makes V_{GS} constant at this step. The constant V_{GS} is called Miller Plateau voltage V_{pl}. Together with I, the C_{oss} discharge current flows through the MOSFET channel. At t_3, V_{DS} decreases in a non-linear way because of the non-linearity of the inter-electrode capacitances to $V_{DS(on)}$.

[10]The reverse recovery of Si diode may give rise to a rapid decrease of V_{DS} voltage at the beginning of the t_2 [84], however this phenomena is neglected in the analysis.

4. $\boldsymbol{t_3 - t_4}$ (shown in Figure 1.24(d)) At this step, I_G continues to charge C_{gs} and C_{gd}, which makes V_{GS} increase to V_{cc} at t_4. The MOSFET turn-on switching finishes at t_4.

The MOSFET turn-off switching is similar to that of turn-on, and it can be still divided on four main steps which is illustrated on Figure 1.25.



(a) t_5-t_6 (b) t_6-t_7

(c) t_7-t_8 (d) t_8-t_9

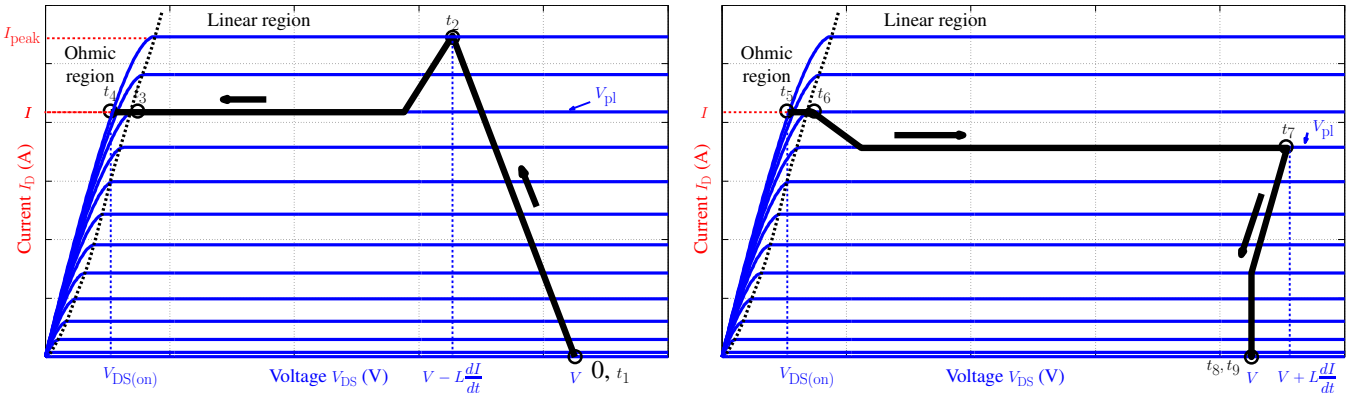
FIGURE 1.25: MOSFET turn-off switching process

1. $\boldsymbol{t_5 - t_6}$ The current loops are illustrated in Figure 1.25(a) for the first step of the turn-off. V_{com} turns to 0 immediately, which induces a current $I_G = -\frac{V_{GS}}{R}$ to discharge both C_{gd} and C_{gs} of the MOSFET. Therefore, V_{GS} begins to discharge. The decrease of the V_{GS} brings the MOSFET to the linear region from ohmic region as shown in Figure 1.26(b). At t_6, C_{gd} and C_{ds} begin to be charged.

2. $\boldsymbol{t_6 - t_7}$ (shown in Figure 1.25(b)) The charge of C_{gd} and C_{ds} make V_{DS} increase in a non-linear way because of the non-linearity of the inter-electrode capacitance. Thus, the charge of C_{gd} by load current plays a negative feedback on V_{GS} voltage, which leads to another constant V_{pl} at turn-off. As C_{ds} is charged by one part of the load current, there is less current in MOSFET channel at this step than $t_2 - t_3$ step of turn-on, which makes V_{pl} at turn-off smaller than that at turn-on. The increase of V_{DS} makes diode voltage V_{KA} decrease, thus, the diode junction capacitor C_j is discharged. The diode discharge current decreases I_D value. At t_7, V_{DS} increases to V.

3. $\boldsymbol{t_7 - t_8}$ (shown in Figure 1.25(c)) At t_7, C_{gs} and C_{gd} begin to discharge, which makes I_D start to decrease. The decrease of I_D induces a voltage $L\frac{dI}{dt}$ across the L, which makes V_{DS} arrive to a peak value $V + L\frac{dI}{dt}$ at this moment. At t_8, V_{GS} falls to V_{th} and I_D decreases to 0.

4. $\boldsymbol{t_8 - t_9}$ (shown in Figure 1.25(d)) At this step, I_G continues to discharge C_{gs} and C_{gd}, which make V_{GS} decrease to 0 at t_9. The MOSFET turn-off switching finishes at t_9.



(a) Turn-on trajectory

(b) Turn-off trajectory

FIGURE 1.26: MOSFET switching trajectories

It can be seen in Figure 1.26 that the main switching trajectories of the MOSFET are during $t_1 - t_3$ for turn-on and $t_6 - t_8$ for turn-off. A detailed power transistor switching analysis will be presented in Chapter 4 to compare WBG power transistor model with the measurement.

1.4.2 Driver technology

A MOSFET is widely commanded by the driver circuit shown in Figure 1.27.

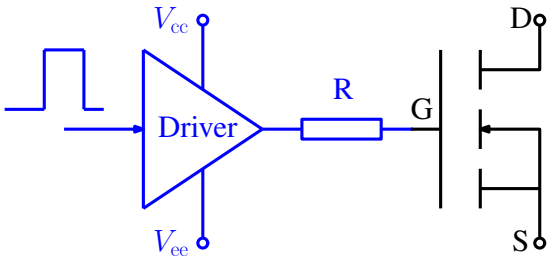


FIGURE 1.27: MOSFET driver circuit

The driver generates a command voltage between V_{cc} and V_{ee} to turn-on and turn-off the MOSFET. For a Si MOSFET, generally, V_{ee} and S is of the same electrical potential and V_{cc} is 15V. Thus, the MOSFET is commanded by a voltage generator between 15V and 0V. The same type of the driver circuit can be applied to an IGBT.

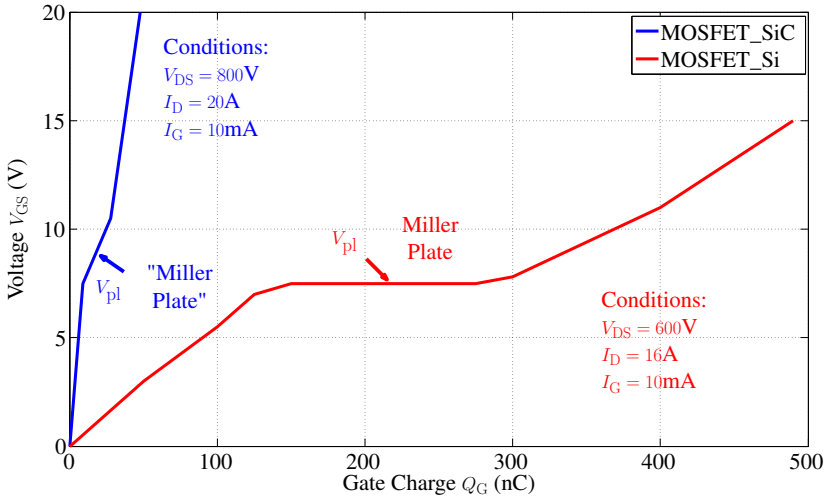


FIGURE 1.28: Gate charge difference between Si MOSFET and SiC MOSFET

The driver and switching performance of a SiC MOSFET is similar to those of Si MOSFET, nevertheless there are still some following differences can be found:

- The threshold voltage V_{th} of a Si MOSFET (IXFN32N120P, 1200V/32A) is about 6V at 25°C, while that of the SiC MOSFET (C2M0080120D) with the same power rating is about 2V at 25°C and it further decreases to 1.7V at 150°C. This difference makes that a SiC MOSFET is normally turned off by a negative voltage to accelerate the turn-off process and to avoid false trigging during the OFF state. The SiC MOSFET is usually turned on by 20V to have a small R_{DSon}.

- The comparison of the gate charge $Q_G(nC)$ and V_{GS} of Si MOSFET and SiC MOSFET is illustrated in Figure 1.28. It can be seen that at similar switching conditions, Q_G of SiC MSOFET is much smaller than that of Si MOSFET due to the smaller inter-electrode capacitances, which guarantees fast switching of the SiC power transistor.

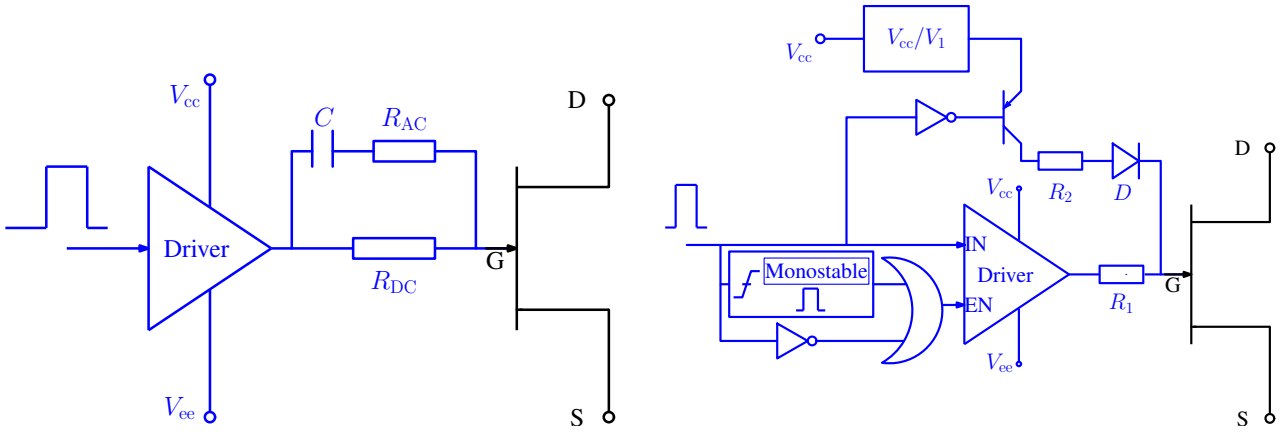
- It was presented in Figure 1.15 the difference of the static characteristics between the Si and SiC MOSFET. For the SiC MOSFET, when it is in linear region, I_D still increases when V_{DS} increases, this difference makes V_{GS} increase at $t_2 - t_3$ trajectory shown in Figure 1.26(a) and V_{GS} decrease at $t_6 - t_7$ trajectory shown in Figure 1.26(b). Thus, it is not a real miller plate for SiC MOSFET as shown in Figure 1.28.

The normally-off GaN HEMT can be commanded by the driver circuit shown in Figure 1.27. For the GaN HEMT (EPC2012), they are commanded by $\pm 5V$ to switch [7]. For the normally-on GaN

HEMT in cascode structure, the associated serial Si MOSFET is commanded by the driver circuit to turn-on and turn-off [29].

SiC JFET is another widely used WBG power transistor. With its structure shown in Figure 1.5 and in Figure 1.6(a), there is one gate body diode between gate and source D_{GS} and another between gate and drain D_{GD}. For a normally-off SiC JFET, V_{th} is about 1V. If the normally-off JFET is commanded by the driver circuit shown in Figure 1.27 with $\pm 15V$, then lots of power loss will be produced at the gate diodes when the JFET is in conduction. If it is commanded by $+3/-15V$, then turn-on switching will be too long. Thus, the driver for SiC JFET is different of that for MOSFET.

There are usually two types of driver for SiC JFET: AC coupled driver [14, 85, 86] and DC coupled driver [14, 87], which are shown in Figure 1.29.

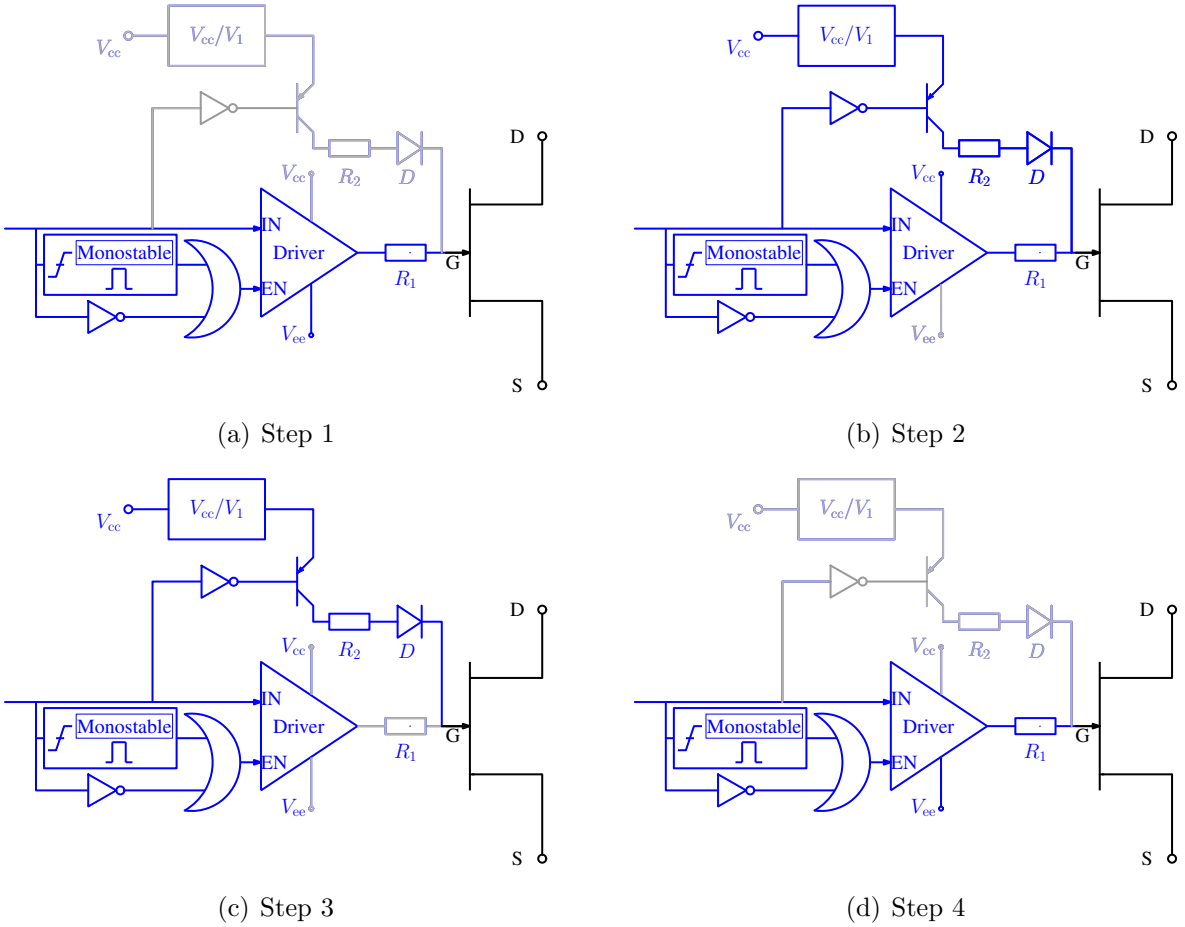


(a) AC coupled driver[14, 85] (b) DC coupled driver[14, 87]

FIGURE 1.29: Two types of SiC JFET drivers

The basic AC coupled driver circuit is presented in Figure 1.29(a). When the JFET is in conduction, a continuous DC current is supplied by V_{cc} and this current flows through R_{DC}. By choosing the R_{DC} values, the continuous DC current in the gate can be chosen, thus the desired V_{GS} can be achieved based on the body diode D_{GS} static characteristics. The capacitor C stores the charge $C \times (V_{cc} - V_{GS})$ when JFET is in conduction. When the JFET is in turn-off switching, the gate discharge current flows through C and R_{AC}. The stored charge in C needs to be fully discharged through R_{AC} and R_{DC} when the JFET is blocked. When the JFET is in turn-on switching, as there is no charge stored in C, thus, JFET gate can be quickly charged by V_{cc}. The charge current flows through C and R_{AC}. It can be seen that the current flowing through C changes the direction during turn-on and turn-off switching, thus, C is a bypass capacitor so the driver is called AC coupled driver. The drawback of this circuit is that the limit of duty cycle and frequency due to the fact that C needs to be fully discharged when the JFET is blocked. Authors in [86] improved this driver by adding a Zener diode between G and S to clamp the turn-off voltage of the JFET and another Zener diode in parallel with R_{DC} to maintain the voltage difference of V_{ee} and V_{GS} during turn-off switching.

The DC coupled driver circuit is presented in Figure 1.29(b). A commercial SiC JFET driver is based on this circuit [14]. The driver circuit is constituted with two parts: one part is the three-state driver (High, Low and High-impedance) with R_1 to charge and discharge the gate for switching; another part is V_1 together with R_2 and D to supply a continuous DC current when the JFET is in conduction. The operation of the driver can be divided in 4 steps and they are illustrated in Figure 1.30(a)-1.30(d). The key waveforms in the driver circuit are presented in Figure 1.31.



(a) Step 1

(b) Step 2

(c) Step 3

(d) Step 4

FIGURE 1.30: JFET DC coupled driver operation

1. At the first step (shown in 1.30(a)), the signal at input of the driver "IN" is 0. The inverter inverses the signal to the PNP BJT, so the BJT is blocked. The enable of the driver "EN" is 1. V_{ee} and R_1 operate at this step. Thus, the JFET is initially blocked.

2. At step 2 (shown in 1.30(b)), the signal at input of the driver turns to 1. The inverter inverses the signal to the PNP BJT immediately, and the BJT is ready to conduct as soon as the gate G potential is low enough for the diode D to be forward biased. The monostable is activated in the rising edge of the signal IN with sufficient time (100ns in the commercial driver) delay. Thus at this step, both "EN" and "IN" are 1. V_{cc} and R_1 operate primarily at this step to turn-on the JFET. With a small R_1, JFET can be switched ON rapidly.

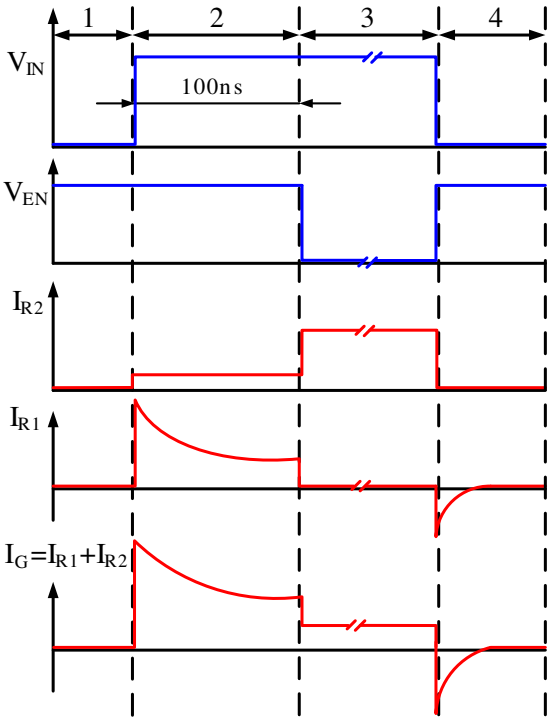


FIGURE 1.31: JFET DC coupled driver Key waveforms

3. At step 3 (shown in 1.30(c)), at the end of the 100ns, the entrance of "EN" turns to 0. The driver is in high impedance state. V_1 together with R_2 and D operates at this step and supplies a reduced DC current to the JFET gate. JFET is in conduction at this step.

4. At the last step (shown in 1.30(d)), the signal at input of the driver "IN" turns to 0. The inverter inverses the signal to the PNP BJT immediately, so the BJT is blocked. The enable of the driver "EN" is 0. V_{ee} and R_1 operate at this step. Thus, the JFET is discharged to switch off at this step and it returns to the step 1, so the cycle is finished.

The principle of the above driver circuits presented in Figure 1.27 and Figure 1.29 is to turn-on and turn-off the power transistor by a voltage source. However, the charge and discharge of the power transistor gate source capacitor C_{gs} cause power loss at the gate resistance during the switching of the device. Authors in [88–90] report a current source driver with the basic circuit shown in Figure 1.32. The circuit were used to command a MOSFET. By controlling the power switches S_1-S_4 of the driver circuit, the stored energy in the L can be sent to the MOSFET gate to turn-on the device and during the MOSFET turn-off, the gate energy can be restored in L. Therefore, there is less power loss in the driver circuit than with a voltage source driver. Authors in [91] showed that it is possible to apply the current source driver circuit for WBG power devices. A GaN HEMT was driven by a similar current source driver with a maximum switching frequency up to 5.55MHz.

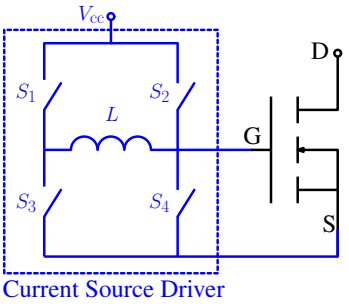


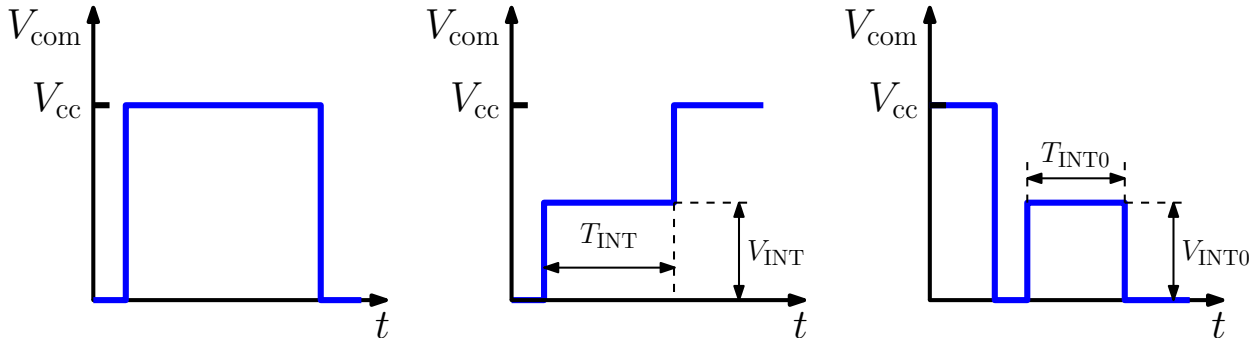
FIGURE 1.32: MOSFET current source driver

In electrical systems, realizing fast switching is a solution to decrease switching loss, therefore to increase power efficiency. However, fast switching gives rise to electromagnetic interference problems. It is also necessary to know how to control the switching process. The different technologies to control power transistor switching $\mathrm{d}I/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t$ will be presented in the next section.

1.4.3 Power transistor switching control

With what has been presented in the above section, by changing gate resistor R in the driver circuit in Figure 1.23(a), I_{G} can be changed, therefore I_{D} and V_{DS} switching duration can be changed. This is one method to control power transistor switching $\mathrm{d}I/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t$.

Besides this method, in traditional Si MOSFET and IGBT, active gate control technologies have been widely used. Authors in [92] proposed an active gate control method by regulating the command voltage. In the power transistor driver circuit shown in Figure 1.27, instead of commanding a transistor with the command voltage V_{com} shown in Figure 1.33(a), command voltages in Figure 1.33(b) 1.33(c) are applied. At turn-on switching, V_{INT} and T_{INT} are regulated during the current rise, thus, power transistor $\mathrm{d}I/\mathrm{d}t$ can be controlled. At turn-off switching, V_{INT0} and T_{INT0} are regulated during the voltage rise, thus the $\mathrm{d}V/\mathrm{d}t$ can be controlled in such a way.



(a) Traditional V_{com} (b) Proposed turn-on V_{com} in [92] (c) Proposed turn-off V_{com} in [92]

FIGURE 1.33: Active gate voltage control method [92]

It is reported by authors in [93] to realize active gate control by adding a closed loop between the power IGBT V_{CE} voltage and the driver circuit. The principle is illustrated in Figure 1.34. Gate

driver is controlled by comparing the measured V_{CE} voltage with the reference, thus the dV/dt control can be realized with this principle.

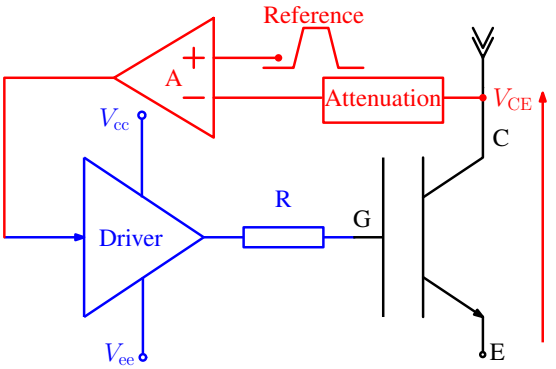


FIGURE 1.34: IGBT active gate control circuit [93]

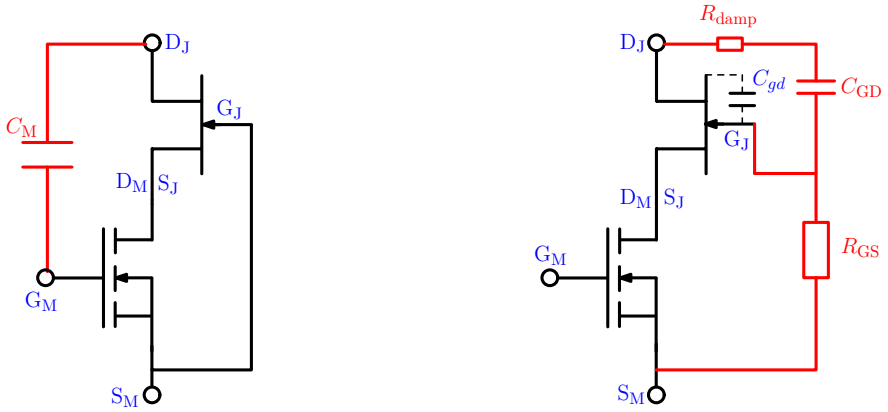
For WBG power transistors switchings, dV/dt control method has been proposed by authors in [94] on a SiC cascode JFET. Generally, in the cascode structure shown in Figure 1.6(b), the Si MOSFET is controlled during the switching and dV/dt of the SiC cascode JFET can not be controlled by the driver circuit. Authors in [94] proposed two controlling concepts which are illustrated in Figure 1.35.

1. In Figure 1.35(a), an external capacitor C_M is connected between JFET drain and MOSFET gate, in which a Miller effect during JFET voltage switching with a negative feedback on MOSFET gate can be achieved. Thus, the dV/dt of the JFET turn-on and turn-off switchings can be controlled by varying C_M values.

2. In Figure 1.35(b), an external resistor R_{GS} is connected between JFET gate and MOSFET source while an external capacitor C_{GD} in series with a damping resistor R_{damp} are connected between JFET gate and drain. By varying R_{GS} values, the total discharge and charge current of JFET inter-electrode capacitors C_{gd} and C_{GD} during the switching can be controlled. While by varying C_{GD} values, the discharge and charge current of the C_{gd} of the JFET during the switching can be controlled. Results are shown that changing R_{GS} while keeping C_{GD} constant or changing C_{GD} while keeping R_{GS} constant can realize the same object to control SiC cascode JFET dV/dt.

It is to be noted that the above methods allow to decrease dI/dt and dV/dt, but increase the switching power loss, thus it is always a choice between EMC and energy efficiency.

The different driver circuits of WBG power transistors and how to control power device switching process have been analyzed in this section. With all those power devices driver technologies, it is possible to design fast switching and high frequency power converters using WBG power devices to increase power efficiency and power density in power electronics systems, which will be presented in the next section.



(a) C_M structure (b) R_{GS} C_{GD} structure

FIGURE 1.35: Cascoded SiC JFET dV/dt controlling method [94]

1.5 High Frequency Power Converters with WBG Power Devices

The WBG power devices advantages such as low specific resistance, fast switching and operation in high temperature have been presented in the above sections. Their integration in power converters is able to achieve the two main objectives: to increase power efficiency and to increase power density.

1.5.1 Power efficiency

It is illustrated in Figure 1.36 the reported evolution of the power converter power efficiency together with power rating and switching frequency in recent years. Power converters with Si, SiC and GaN power devices are compared.

At present, for fast switching, power ratings of the commercial SiC power devices can reach up to 1kV and several tens of amperes. One possibility to further increase power ratings of the power converters is to connect those WBG power devices in parallel [35]. It is reported by authors in [95] that a 6kW boost converter is realized by connecting four SiC BJTs and two SiC diodes in parallel. The power efficiency of the whole power converter is 98.23% and the switching frequency is 250kHz. Authors in [96] put ten normally-on SiC JFETs in parallel as a power switch to realize a three-phase inverter. The switching frequency is 10kHz, with an output power up to 20kW and efficiency to about 99.5%.

The commercial power ratings of the GaN power devices are much lower than that of SiC power devices. Therefore the power ratings of the power converters with GaN devices nowadays are about several hundreds of watts. Authors in [97] demonstrate that a 500kHz, 350W power converter with GaN HEMTs can achieve a power efficiency up to 98.7%. It is reported by authors in [98] that a 1.2kW synchronous boost converter was realized with GaN power transistors switching at 1MHz and

the efficiency is up to 94%. A boost 300W converter with a GaN HEMT and a SiC diode switching at 1MHz is reported by authors in [99], of which the power efficiency is 97.8%. The authors in [100] demonstrated that a 6kHz three-phase inverter is realized with GaN power transistors, in this study, compared to the traditional inverter with Si IGBT as power switches, there is no need of an anti-parallel diode as free-wheeling diode in the power switch with a GaN power transistor. And the overall power efficiency can reach up to 99.3%.

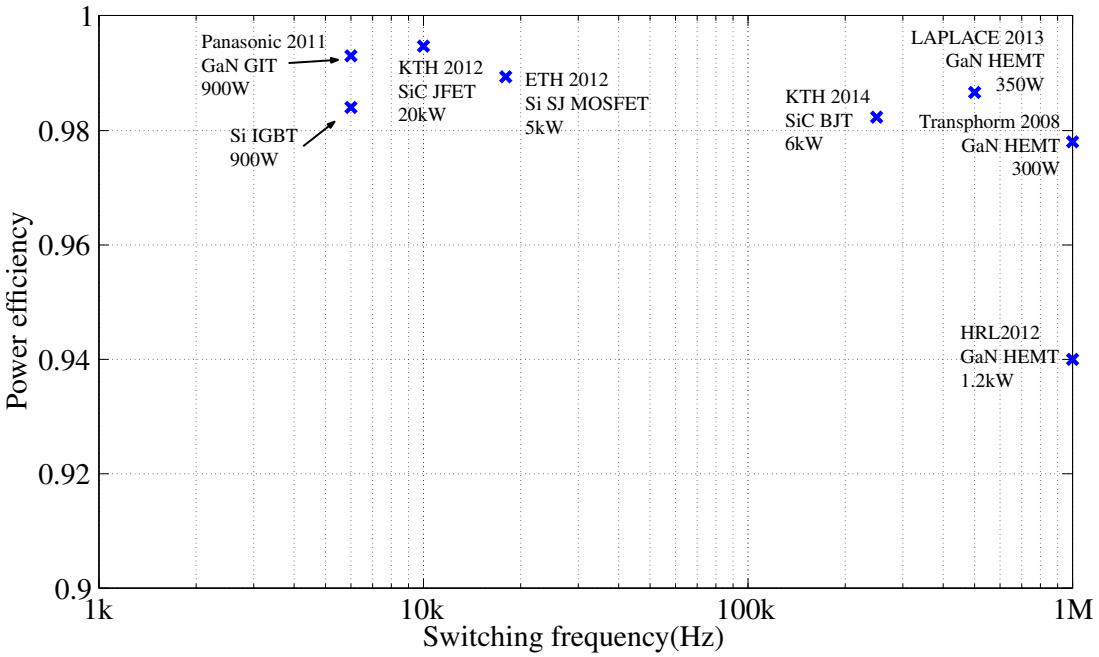


FIGURE 1.36: Power efficiency of different power converters

It is to be noted that with improved Si power devices and special modulation schemes to optimize switching loss, high efficiency power inverters can be realized even with Si power transistors. This is reported by authors in [100], in which a 900W three-phase power inverter can achieve the power efficiency over 98% with Si IGBTs as power switches. Authors in [101] adopted a switching loss optimization modulation scheme to realize a 5kW three-phase power converter with Si super junction MOSFETs as power switches. The overall power efficiency can reach up to 98.9%. However, switching frequency of Si power devices in those power converters is reported to be limited at less than 20kHz.

Switching frequency of power converters with WBG power devices is much faster than with Si power devices. This advantage is able to further increase power density in a power converter.

1.5.2 Power density

It is illustrated in Figure 1.37 the reported evolution of the converter power density together with power rating and switching frequency in recent years. Power converters with Si, SiC and GaN devices are compared[11].

[11] It is to be noted that power density should be compared at the same criteria such as at which operation temperature and at which electromagnetic compatibility (EMC) standard. However, this criteria remains vague in the literature. Thus, the reported power density by different researchers is summarized in this section.

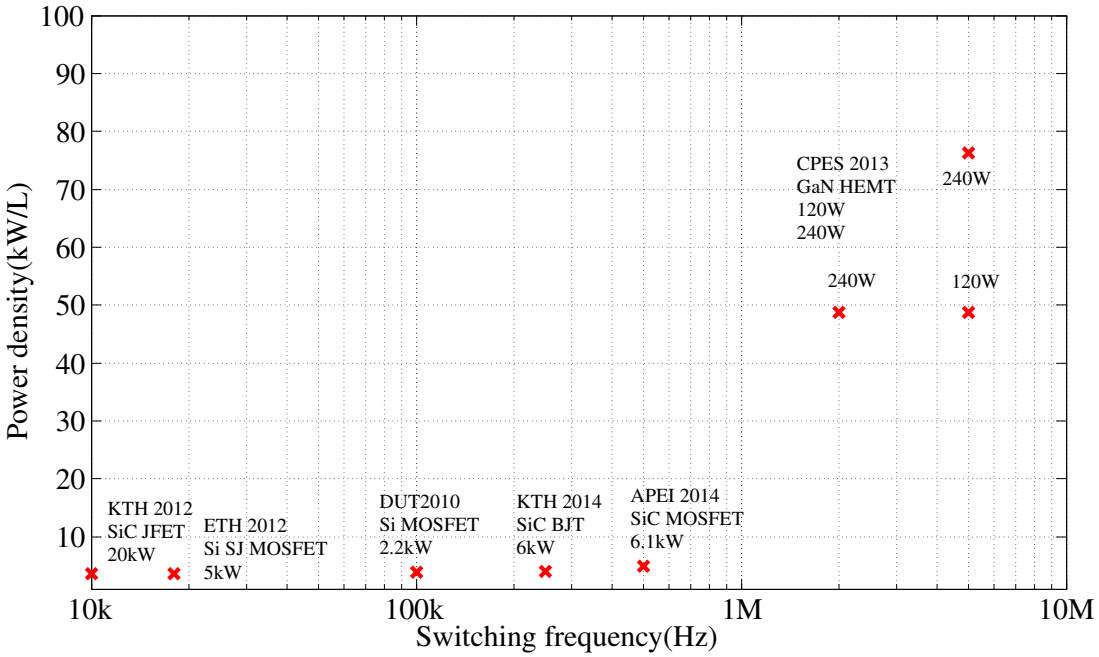


FIGURE 1.37: Power density of different power converters

The three-phase power converter using Si MOSFET reported by authors in [101] can reach a power density of 3.67kW/L (without EMI filter) and 2.2kW/L (with EMI filter) with the 5kW output power and 18kHz switching frequency. A DC-DC converter with Si MOSFET reported by authors in [102] can reach a power density of 3.97kW/L with the 2.2kW output power and 100kHz switching frequency.

For converters with SiC devices, power density can be increased. Authors in [103] reported that an AC-DC converter with SiC MOSFET of 6.1kW and 500kHz switching frequency, the power density can be up to 5kW/L, which is more than ten times bigger than the same converter with Si devices in the literature. In the aforementioned power converters [95, 96], the power density can reach up to 4kW/L and 3.66kW/L respectively, which is bigger than power converters with Si power devices with the same power ratings.

As power ratings of GaN power devices at present are smaller than SiC devices, when converters are with GaN devices, the switching frequency can increase to several megahertz, thus the volume of passive components can be greatly decreased. Power density can be further increased. As what have been reported by authors in [6, 78], in a 240W power converter switching at 2MHz and a 120W power converter switching at 5MHz with GaN HEMTs, the power density can reach 48.8kW/L. While in a 240W power converter switching at 5MHz, the power density can reach 76.3kW/L. Such power density is much bigger than that of a power converter with Si power devices at the same power rating [6].

With WBG power devices fabrication technologies development [104], the design of high power efficiency, high power density converters with these devices is the future development trend. The switching time in high frequency power converters is short. Therefore, how to measure the power

devices switching waveforms is important to design high frequency power converters. WBG devices switching measurement methodology will be finally presented in the next section.

1.6 Power Semiconductor Devices Switching Waveforms Measurement Methodology

In this section, fast switching voltages measurement will be presented at first, then the state of the art on fast switching current measurement will be reviewed.

1.6.1 Voltage measurement methodology

In the switching test results of a SiC MOSFET switching at 600V and 20A presented by authors in [40], with a 10Ω gate resistance R_G, V_{DS} switching time is about 30ns, with a dV/dt equal to 20V/ns, which can be bigger than a Si IGBT voltage slope [105]. It is well known that decreasing the R_G values, V_{DS} switching time can be further shortened.

Because of smaller inter-electrode capacitances, the voltage switching time of the GaN transistors is even faster than SiC devices, which yields a much bigger dV/dt slope. The switching time of a GaN HEMT (at 100V and 1A) is about 4ns, with a dV/dt ofe about 25V/ns [106]. The switching time of a GaN HEMT (at 380V and 6A) is about 5ns, which yields a dV/dt slope about 76V/ns [107], and the same GaN HEMT can arrive a voltage slope up to 100V/ns according to the results shown in [29] when the device switches at 400V and 10A.

To measure the switching voltages, there are active differential voltage probes (ADVP) and passive voltage probes (PVP) can be used, which are shown in Figure 1.38.

1. There are an active circuit in ADVP to compensate the measured voltages. Nowadays, the maximum measured voltages in commercial ADVP can be above 1000V with the maximum bandwidth up to about two hundreds megahertz. As shown in Figure 1.38(a), the ADVP possess a long cable and big measurement plunger clips from the measurement point to the active circuit. It creates an inevitable loop, which may capture the HF interference signals. The advantage is that ADVP brings no connection to the ground of the oscilloscope in the measurement circuit, which isolates the oscilloscope of the measurement circuit. Several voltages can be measured at the same time by using more ADVPs in the measurement circuit.

2. The PVP equivalent circuit is shown in Figure 1.39 [8]. The termination resistance of the oscilloscope is chosen 1MΩ, thus the input resistance R_{PVP} with the attenuation factor of 10 is 9MΩ. C_{comp} values can be adjusted to keep the same attenuation factor in HF: $\frac{R_{PVP}}{1M\Omega} = \frac{C_{Input}+C_{comp}}{C}$. By changing R_{PVP} values, the attenuation factor can be increased, therefore the

maximum measurement voltage of the PVP can be up to several kilovolts. The maximum bandwidth of the PVP to measure 4kV voltage can arrive up to 400MHz. As shown in Figure 1.38(b), the loop between the measurement point and the probe body is much smaller than that of ADVP, which improves HF interference signals immunity. The drawback of the PVP is that it brings a connection of the ground in the measurement circuit with the oscilloscope. Therefore in a switching mesh shown in Figure 1.23(a), the voltage across the diode V_{AK} and MOSFET V_{DS} voltage should not be measured directly and simultaneously by two PVPs.

(a) ADVP (b) PVP

FIGURE 1.38: Voltage measurement probes configuration

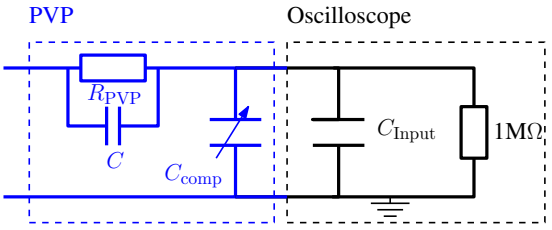


FIGURE 1.39: PVP equivalent circuit

It is to be noted that both ADVP and PVP bring an insertion impedance in the measurement circuit. Thus, this insertion impedance may probably modify the switching voltages at fast switching conditions.

Another important issue concerning the use of the voltage probes is that their maximum measurement voltage V_{max} changes with the frequency. It is compared in Figure 1.40 the V_{max} with the frequency among a 1000V/100MHz ADVP (ADP305), a 400V/400MHz PVP (PP008) and a 4kV/400MHz PVP (PPE4kV). It can be seen in Figure 1.40 that the V_{max} decreases both for ADVP and PVP. To measure a SiC MOSFET V_{DS} switching at 600V and during 30ns (which equals to about 10MHz), there is no guarantee that the use of the above ADVP will not modify the real switching voltage waveform due to its attenuation of the V_{max} down to about 200V at 10MHz. To measure the GaN HEMT V_{DS} switching at 380V and during 5ns (which equals to about 60MHz), it is certain that the measured V_{DS} by ADVP is not the real switching voltage waveform.

Even though the use of PVP brings a connection to the ground problem, with its large bandwidth and high voltage rating, it is adaptable to measure WBG fast switching voltages. More details about

the use of the above voltage probes to measure a GaN HEMT fast switching V_{DS} voltages will be presented in Chapter 4.2.

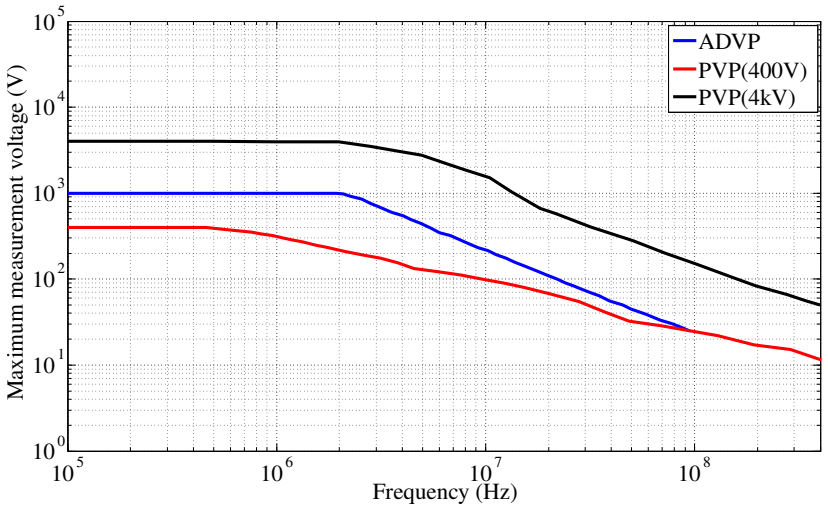


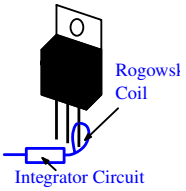
FIGURE 1.40: Maximum measurement voltages with frequency of different voltage probes

1.6.2 Current measurement methodology

In a traditional power converter with Si transistors, current switches during several tens to hundreds of nanoseconds with a current slope less than 1A/ns [105]. With the current measurement results presented by authors in [108], for a SiC JFET switching at 365V and 10A, the current switching time is about 10ns with a current slope about 1.5A/ns. While for GaN power transistors, this current transition time can be shortened to about 5ns with a current slope about 5A/ns [109] when the device switches at 100V and 15A. The current switching time was further shortened to about 2ns with a current slope about 7.5A/ns when the device switches at 400V and 10A according to the results shown by authors in [29].

This current switching time requires that the current measurement probes are with high bandwidth and with small insertion impedances, because current probes insertion impedance in the measurement circuit may modify the current switching waveforms [80]. Among all the current measurement techniques presented by authors in [110, 111], at present, there are Hall Effect Current Probe (HECP), Rogowski Coil (RC) and Current Shunt (CS) used to measure power devices switching current in power converters.

(a) Hall effect current probe



(b) Rogowski coil

(c) Current shunt

(d) Current probe

FIGURE 1.41: Current measurement probes

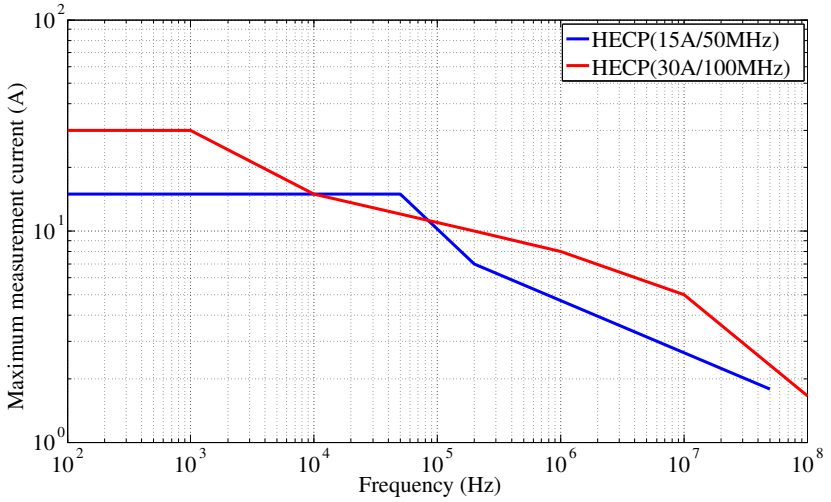


FIGURE 1.42: Maximum measurement current with frequency of different HECP

1. **Hall effect current probe (HECP)** is an active current probe (shown in Figure 1.41(a)). The advantage of this probe is that it is able to measure DC current. The maximum bandwidth of a commercial HECP nowadays can reach up to 120MHz, with a maximum measurement current 30A at DC state. However, HECP brings an inevitable insertion impedance in the measurement circuit, which may have influence on both switching current and switching voltage waveforms. Otherwise, similar to ADVP, the maximum measurement current decreases when the frequency increase. It is shown in Figure 1.42 the relation between the maximum measurement current and the frequency for a 15A/50MHz HECP (TCP202) and another 30A/100MHz HECP (CP031). It can be seen that when frequency is 1MHz, the maximum measurement current by HECP decreases to a factor of 3-4 in comparison with their maximum measurement DC current, while when frequency is 10MHz, the maximum measurement current can decrease to a factor of 6. Thus, it is difficult to use a HECP to measure GaN HEMT switching current during 2-5 ns.

2. **Rogowski coil (RC)** is constituted by a number of turns of evenly wound air cores. The principle of the RC is that the change of the measurement current induces a voltage in the coils, by integrating the induced voltage, an output voltage V_{out}, which is proportional to the measurement current, can be created [112, 113]. As there is no magnetic materials inside the RC, there is no saturation current. As shown in Figure 1.41(b), another advantage of the RC is that its volume is small, and it brings almost no insertion impedance on the measurement circuit. No special current measurement circuit is necessary, because it can be wound around one leg of the power device in TO220 or TO247 packaging. Therefore, the commutation mesh of the power devices when using RC is small. However, the commercial RC is limited in the bandwidth of 30MHz, which corresponds to the current switching time of about $10ns$. Authors in [114] measured a SiC BJT switching current by a RC with the current switching time of about $40ns$.

3. **Current shunt (CS)** is nowadays widely used for fast switching current measurement. Authors in [8, 45, 108] used the CS to measure SiC diode, SiC JFET and GaN HEMT switching current. Its main advantage is large bandwidth above 1GHz, which makes it totally adapted for switching current during few nanoseconds. However, CS brings the ground of the oscilloscope to the measurement circuit, which makes it difficult to measure different power devices currents simultaneously in a switching mesh. This drawback also limits the use of PVP together with the CS to measure voltage and current simultaneously in the circuit. Furthermore, there is no isolation between the CS and the oscilloscope, thus there is no protection for the oscilloscope when the CS is in operation. For the CS shown in Figure 1.41(c), it can be modeled by the electrical circuit shown in Figure 1.43 [45, 115]. Parasitic inductors L_A and L_B can be found at each side of the shunt resistor R_s. The values of L_A decides the CS insertion impedance in the measurement circuit, which varies among different CS models from several nH to 10nH [45, 108]. While L_B decides the validity of the transfer function between the measurement voltage induced at oscilloscope V_{osc} and the real measurement voltage V_{mes}. With the value 5nH presented by authors in [45], $\frac{V_{osc}}{V_{mes}}$ decreases by -3dB around 300MHz if the CS is connected directly to the oscilloscope. With the presence of a BNC cable between CS and the oscilloscope, the validity of the CS measurement bandwidth may be decreased. Besides that, heating is also a drawback of CS [116].

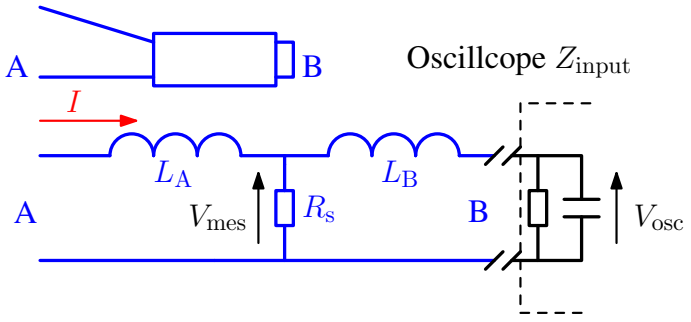
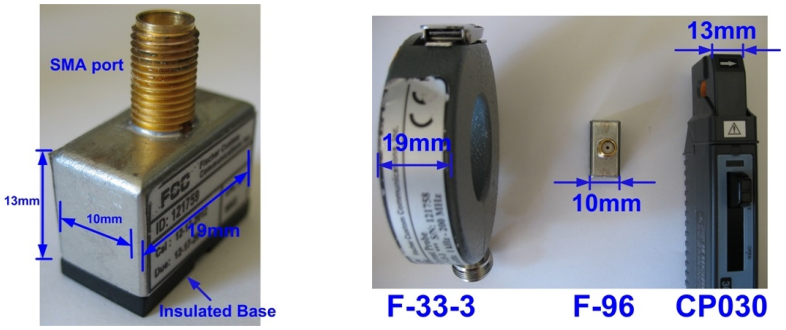


FIGURE 1.43: CS equivalent electrical circuit

4. **Current probe (CP)** is a one kind of passive clamped-on current transformer, which can be used to measure power converter common mode and differential mode currents. The advantage of the CP is that it has a large bandwidth up to several hundreds megahertz, however, the CP is usually bulky, which brings an inevitable insertion impedance in the power converter. There are smaller clamp-on CPs, but they can not be generally opened, which is not practical in use.

To measure a very fast switching current of WBG devices, using a current surface probe (CSP) is proposed in the thesis. The dimension of the CSP (FCC F-96, 1MHz-450MHz) is shown in Figure 1.44(a). It is a passive probe to measure currents on metallic conductors. An insulated base at one end of the probe helps to provide a galvanic isolation with the conductor, so that the probe can contact directly with the surface over which the current flows (PCB track). At another end, it is an SMA port. Compared to the HECP (Lecroy CP030, DC-50MHz), and another commercial

passive current probe (CP) (FCC F-33-3, 1kHz-200MHz), the dimension of the CSP is much smaller as shown in Figure 1.44(b), which guarantees a small insertion impedance brought by the CSP in the measurement circuit. Its bandwidth is up to 450MHz, which guarantees fast switching current measurement. More details about the use of CSP to measure power devices switching current will be presented in Chapter 4.2.



(a) F-96 (b) Dimension comparison

FIGURE 1.44: Dimension of different current probes

1.7 Conclusions

Physical properties of the wide bandgap materials have been presented first in this chapter. Power semiconductor devices fabricated based on the WBG semiconductor materials can have higher operation temperature and blocking voltages, smaller specific resistances and inter-electrode capacitances than Si power semiconductor devices. The methods to characterize and to model those power devices are thus presented. Their different driver technologies are reviewed to integrate the discrete power devices in the power converter. Power efficiency and power density of static converters with WBG devices are further investigated to prove their advantages. To further increase power efficiency and power density, it is necessary to have very fast power semiconductor devices. Fast switching voltage and current measurement is very important for high frequency power converters design. Therefore, different voltage and current measurement methodologies are presented at last.

As shown in this chapter that WBG power devices are relatively new, understanding their characteristics is very important to better use those devices in power converters. Thus, WBG power devices static characteristics measurement by single pulse method and dynamic characteristics measurement by multiple-current-probe method will be presented in Chapter 2.

Chapter 2

Power Semiconductor Devices Characterization: Multiple-Current-Probe Method

In this chapter, the method to determine power semiconductor devices static and dynamic characteristics will be presented.

First, power devices static characteristics measurement using single-pulse method will be detailed. This method is able to control power device junction temperature and increase the device power dissipation.

Second, power device dynamic characterization by the proposed multiple-current-probe method will be presented. This method is able to isolate the measurement equipments with the power source and to characterize power device inter-electrode capacitances at high voltage.

This chapter is finished by a discussion about a study of the characterization methods. A brief conclusion is given at last.

2.1 Static Characteristics

In this section, the principle of the single-pulse method will be illustrated at first. Then the presented method will be applied to characterize a SiC diode (CSD20060D) and a SiC JFET (SJEP120R063) static characteristics at different junction temperatures (T_j), which is estimated during the measurement.

2.1.1 Characterization principle

One possibility to apply the single-pulse method principle to characterize a power device is illustrated in Figure 2.1. The measurement is basically constituted by a bulk capacitor C_{bulk}, a power transistor T with its driver circuit, an inductor L, a power device under test (DUT) and a freewheeling diode D. The DUT can be either a power diode or a power transistor. If it is a power transistor, a power supply like a battery is necessary to supply power transistor V_{GS} voltages.

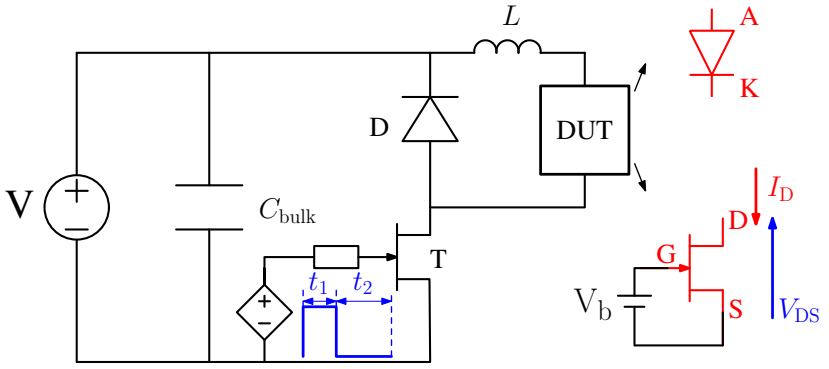
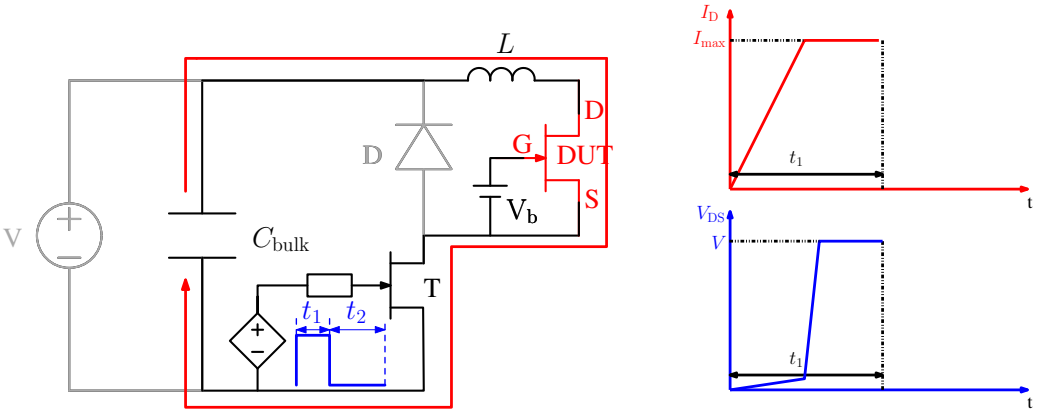


FIGURE 2.1: Single pulse method principle

When T is controlled by the single-pulse control signal shown in Figure 2.1, the circuit operation with a power transistor can be divided on two steps:

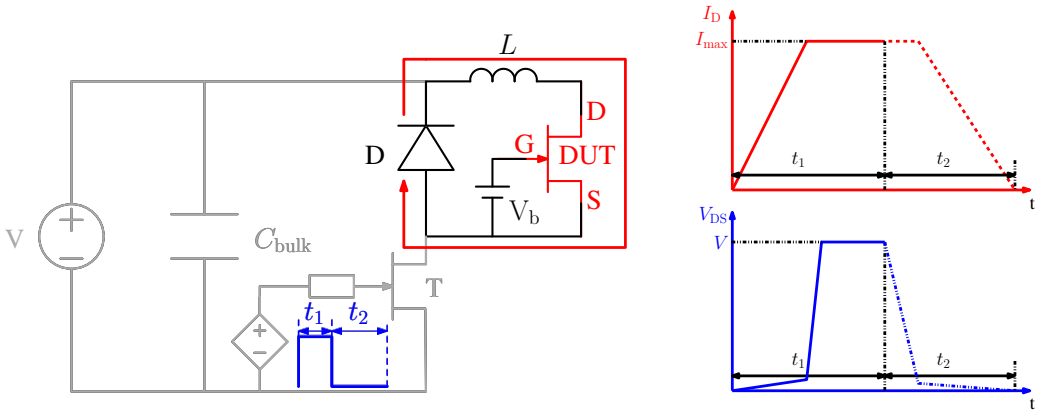


(a) Circuit (b) I_{D}, V_{DS} waveforms

FIGURE 2.2: Pulse on circuit and DUT waveforms

1. **Step 1:** During t_1, T is in ON state. The current loop is illustrated in Figure 2.2(a). DUT current I_{D}, V_{DS} waveforms are presented in Figure 2.2(b). The current from the C_{bulk} flows through the DUT. I_{D} increases to I_{max} value, which is determined by DUT V_{GS} voltage which equals to V_{b}. By varying L value, the current slope can be adjusted. When I_{D} reaches I_{max} value, V_{DS} increases rapidly and finally reaches the power source value V. It is shown in Figure 2.4 that the power device trajectory moves from the ohmic region to the linear region at this step. The energy is transfered from the C_{bulk} to the DUT.

2. **Step 2:** During t_2, T is in OFF state. The current loop is illustrated in Figure 2.3(a). DUT current I_D, V_{DS} waveforms are presented in Figure 2.3(b). V_{DS} begins to decrease, and the DUT moves from the linear region to the ohmic region. Once the DUT in the ohmic region, I_D begins to decrease rapidly. At this step, I_D flows through the diode. The DUT trajectory can be summarized in Figure 2.4.



(a) Circuit (b) I_D, V_{DS} waveforms

FIGURE 2.3: Pulse off circuit and DUT waveforms

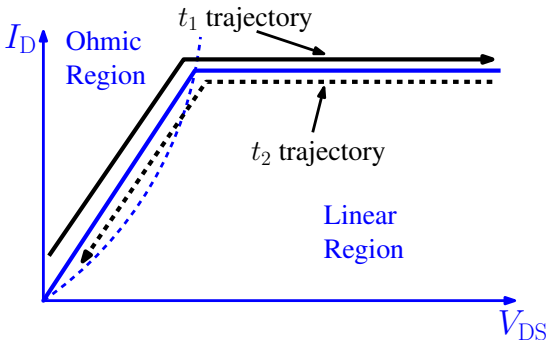


FIGURE 2.4: DUT trajectory during the pulse

According to the power device transient thermal impedance presented in Chapter 1.2.1, by regulating the power pulse duration t_1, power device junction temperature can be controlled.

2.1.2 Characterization configurations

The experimental set up used to characterize the SiC JFET is shown in Figure 2.5. An IGBT (IXGR40N60C2, 600V/56A) is chosen as the controlled power transistor T, and a diode (CSD20060D, 600V/30A) is chosen as the freewheeling diode D. The inductance value is chosen to be 43μH and the bulk capacitor value is 680μF. The DUT gate voltage V_{GS} is regulated by a potentiometer and a 2.2μF capacitor is connected between DUT G and S to stabilize V_{GS} voltage during the measurement. The pulse duration t_1 is chosen to be 50μs to avoid power device heating.

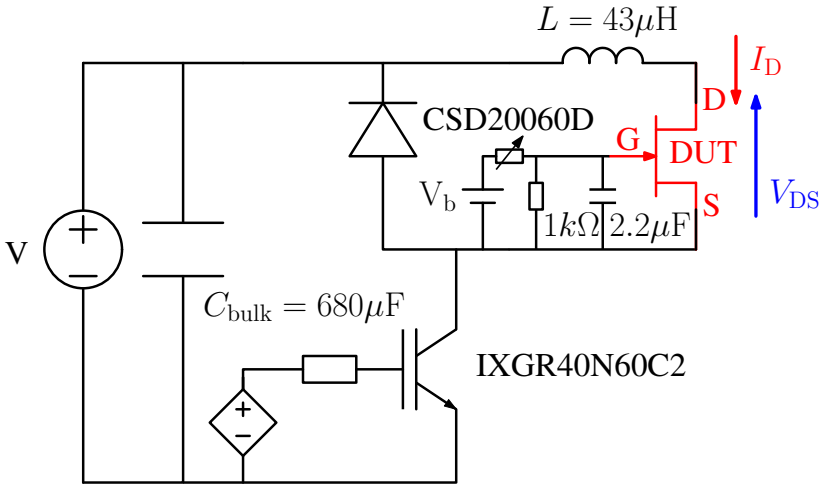


FIGURE 2.5: Experimental setup used to measure device static characteristics on single-pulse

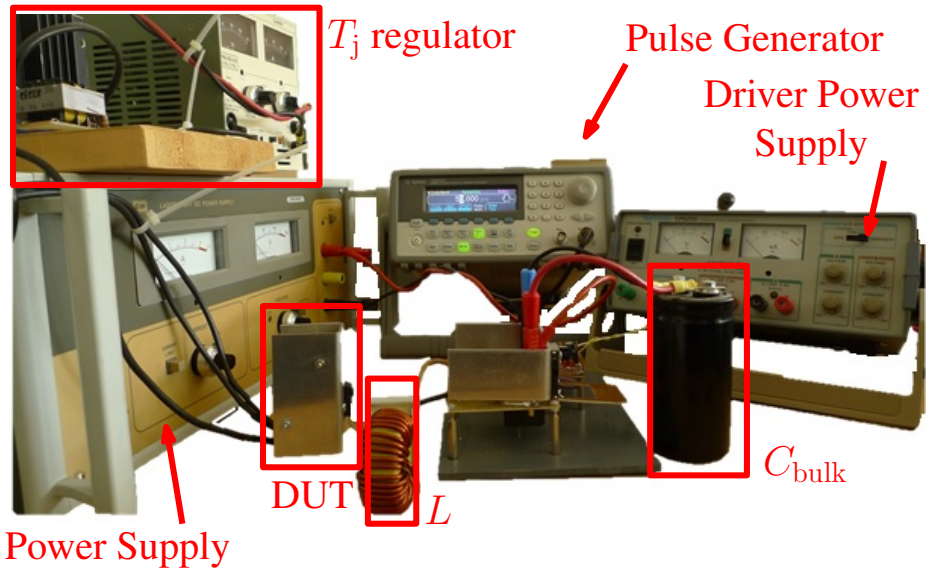


FIGURE 2.6: Measurement setup photo

Each above part is illustrated in the measurement setup photo, which is shown in Figure 2.6. The thermal resistances are connected together with the power device dissipater in order to regulate temperature, so as to characterize power device for different T_j.

The voltage waveform V_{DS} is measured by an active differential voltage probe (ADP305, DC-100MHz, 1000V). The drain current waveform I_D is measured by an Hall effect current probe (CP030, DC-50MHz, pulse current 50A). The oscilloscope is with the bandwidth of 600MHz and in 12-bit.

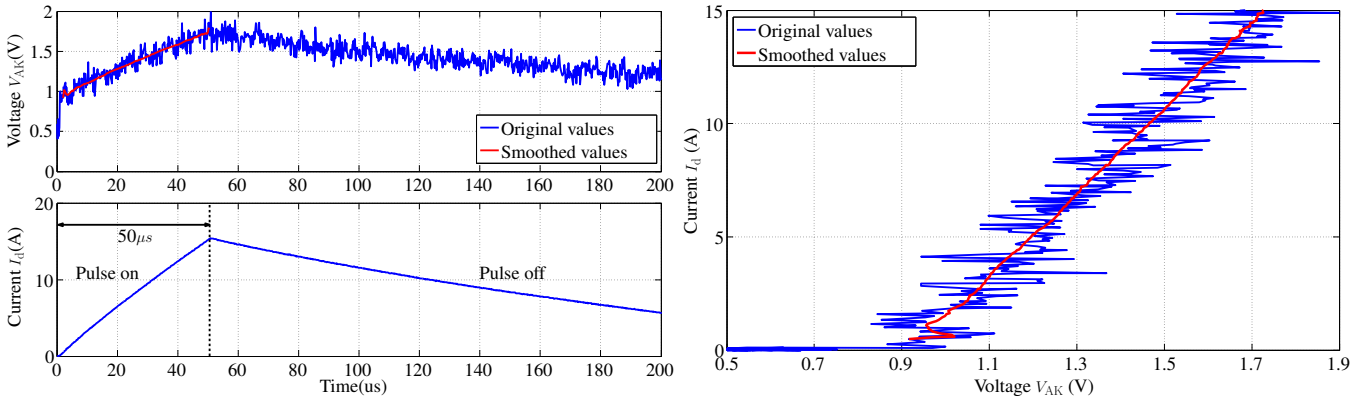
2.1.3 Characterization of the SiC devices

2.1.3.1 SiC diode

It is shown in Figure 2.7(a) the measured voltage V_{AK} and current I_d waveforms of a SiC diode (CSD20060D) when $T_j = 25°C$[1]. There is the noise in the measured V_{AK} voltage, because it is

[1]It is to be noted that diode static characteristic is able to be measured also when it is in continuous state.

measured by a 1000V ADVP. The use of the differential probe brings no connection of the ground in the measurement circuit, which isolates the oscilloscope with the measurement circuit. However, for a 1000V ADVP, it is not sensible to measure a few volts. A smooth method is necessary to take the mean value of the measured voltage as shown in Figure 2.7(a). In order to obtain diode static characteristics, during the period of pulse on, the measured V_{AK} and I_{d} can be plotted in V_{AK}-I_{d} figure which is shown in Figure 2.7(b). The diode capacitive current I_{c} can be neglected during the measurement because of a small $\frac{\mathrm{d}U}{\mathrm{d}t}$[2], thus the measured I_{d} current and V_{AK} voltage represent its static characteristics, which is shown by smoothed values in Figure 2.7(b).



(a) I_{d} and V_{AK} waveforms

(b) Static characteristic

FIGURE 2.7: SiC diode V_{AK} and I_{d} waveforms when $T_{\mathrm{j}} = 25°C$ used to plot the static characteristic

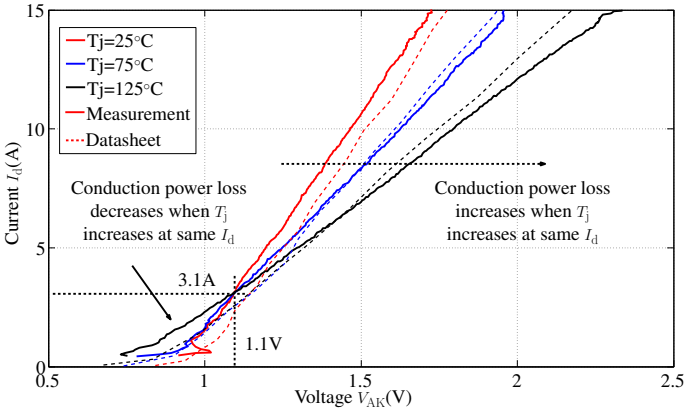


FIGURE 2.8: SiC diode static characteristics at different T_{j}

It is shown in Figure 2.8 that the measured SiC diode static characteristics at different T_{j} in comparison with datasheet values (dotted lines). The measurement results correspond well with the datasheet values, which helps to validate the presented method. It can be seen that the three measurement curves at different T_{j} intersect at one point 1.1V, 3.1A. When I_{d} is below 3.1A, the diode conduction power loss decreases when T_{j} increases for the same I_{d}, thus the power diode has a positive temperature coefficient. When I_{d} is above 3.1A, the diode conduction power loss increases when

[2] $I_{\mathrm{c}} = C \times \frac{\mathrm{d}U}{\mathrm{d}t}$, $\frac{\mathrm{d}U}{\mathrm{d}t}$ is about $1V/50\mu$s in the measurement, even if the value of C is 1μF in the measurement, I_{c} is about 0.02A, which is neglected if I_{d} is above 0.5A.

T_j increases for the same I_d, thus the power diode has a negative temperature coefficient. In the diode technical datasheet, when the pulse duration is 50μs, its junction to case transient thermal impedance $Z_{th,j-c}$ is 0.06°C/W, therefore the maximal diode power dissipation during the measurement is about 27W, which yields a less than 2°C temperature variation. Thus, the temperature variation has almost no influence on measurement results.

2.1.3.2 SiC JFET

To characterize the SiC JFET, the gate voltage is first fixed at $V_{GS} = 1.4$V and junction temperature $T_j = 25$°C. The measured waveforms of different V_{DS} and I_D values are shown in Figure 2.9. It can be seen that during the 50μs pulse-on period, V_{DS} and I_D stabilize after 10μs. More power is dissipated in the power transistor during the measurement. As what has been presented in Chapter 1.2.1, there is a huge influence of T_j on power device static characteristics. Therefore, T_j evolution during the measurement needs to be evaluated.

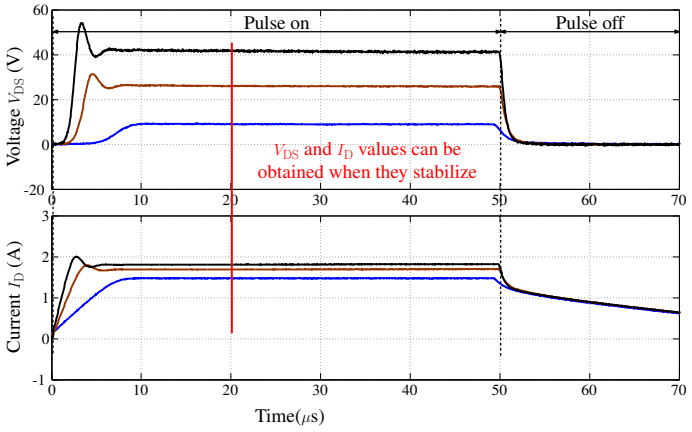


FIGURE 2.9: V_{DS} and I_D waveforms when $V_{GS} = 1.4V$ and $T_j = 25°C$

At first, for the presented V_{DS} and I_D values shown in Figure 2.9, the power dissipation can be obtained by multiplying V_{DS} with I_D and it is shown in Figure 2.10(a). The transient thermal impedance $Z_{th,j-c}$ of the power device is shown in Figure 2.10(b), which is obtained from the SiC JFET technical datasheet[3].

For any power dissipation waveform shown in Figure 2.10(c), the T_j can be calculated in the following way:

At instant A shown in Figure 2.10(c), the dissipated power at this instant is $P(t-\tau)$, thus its contribution during the power pulse t to the T_j increase ($\Delta T_j(t)$) can be calculated by

[3]There is no $Z_{th,j-c}$ curve available in the characterized JFET SJFP120R063 technical datasheet. Therefore, the presented $Z_{th,j-c}$ curve is from another JFET SJEP120R100A, which is from the same supplier Semisouth and is in the same type TO247 packaging and similar power rating with SJEP120R063. Therefore, $Z_{th,j-c}$ curve of SJEP120R063 can be supposed to be somehow similar with that of SJEP120R100A.
As case temperature T_c does not evolve during the measurement, thermal impedance $Z_{th,j-c}$ is sufficient to calculate T_j.

$$\Delta T_{\mathrm{j}}(t) = P(t-\tau) \times Z_{\mathrm{th,j-c}}(\tau) \tag{2.1}$$

At instant B, the contribution of the dissipated power to the $\Delta T_{\mathrm{j}}(t)$) can be calculated by

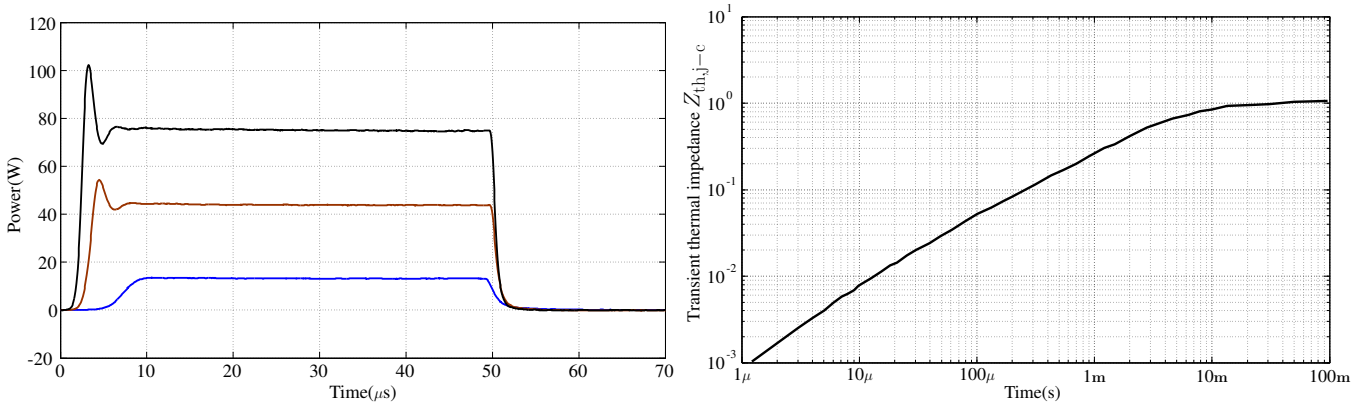
$$\Delta T_{\mathrm{j}}(t) + dT_{\mathrm{j}}(t) = P(t-\tau-d\tau) \times Z_{\mathrm{th,j-c}}(\tau+d\tau) \tag{2.2}$$

Supposing $d\tau$ is tiny, then $P(t-\tau-d\tau) \approx P(t-\tau)$. Following eq.(2.3) can be obtained by subtracting eq.(2.1) to eq.(2.2):

$$dT_{\mathrm{j}}(t) = P(t-\tau) \times \frac{dZ_{\mathrm{th,j-c}}(\tau)}{d\tau} \times d\tau \tag{2.3}$$

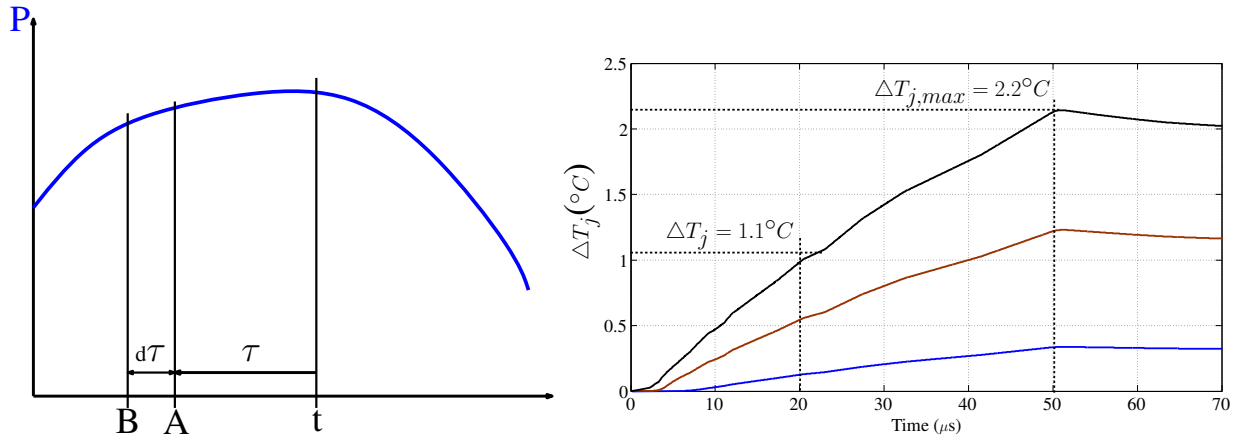
By integrating eq.(2.3), $\Delta T_{\mathrm{j}}(t)$ can be finally obtained by:

$$\Delta T_{\mathrm{j}}(t) = \int_0^t P(t-\tau) \times \frac{dZ_{\mathrm{th,j-c}}(\tau)}{d\tau} \times d\tau \tag{2.4}$$



(a) Power dissipation

(b) SiC JFET $Z_{\mathrm{th,j-c}}$



(c) T_{j} calculation

(d) $\triangle T_{\mathrm{j}}$

FIGURE 2.10: Power device power dissipation and $\triangle T_{\mathrm{j}}$ calculation when $V_{\mathrm{GS}} = 1.4V$ and $T_{\mathrm{j}} = 25°C$

Thus, the evolution of the junction temperature ($\triangle T_j$) for different V_{DS} and I_D values are calculated and presented in Figure 2.10(d). It can be seen that when $V_{DS} = 40V$, the maximal power dissipation is about 75W and the maximal T_j variation is about $2.2°C$. If V_{DS} and I_D values are obtained at $20\mu s$, $\triangle T_j$ is only about $1.1°C$. Therefore, the T_j influence on power device static characteristics can be neglected in the above measurement results.

At one V_{GS} voltage, by varying more V_{DS} values, V_{DS}-I_D characteristics can be obtained. Furthermore, V_{GS} can be regulated to characterize power devices static characteristics for different values.

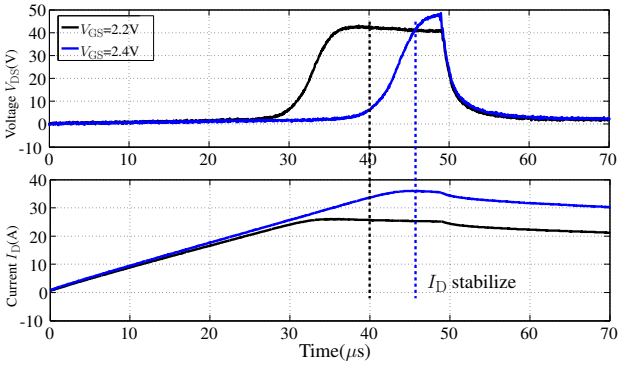
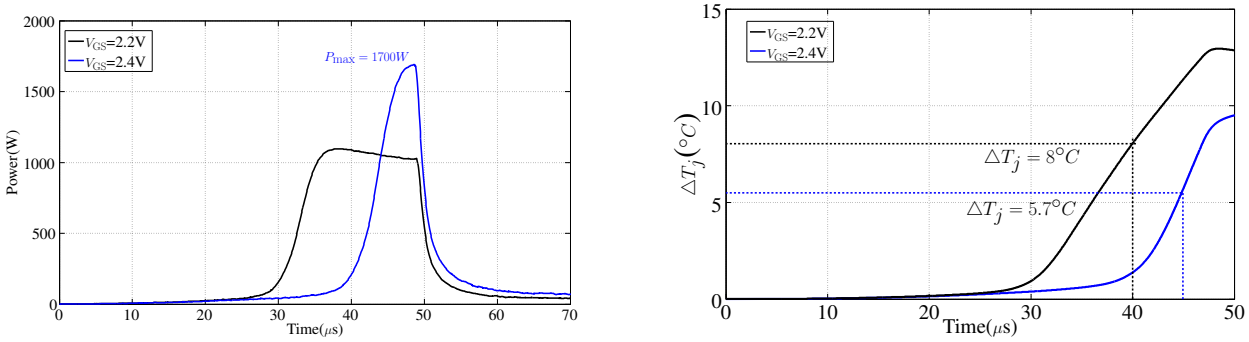


FIGURE 2.11: V_{DS} and I_D waveforms when $V_{GS} = 2.2V, 2.4V$ and $T_j = 25°C$



(a) Power dissipation (b) $\triangle T_j$

FIGURE 2.12: Power dissipation and $\triangle T_j$ when $V_{GS} = 2.2V, 2.4V$ and $T_j = 25°C$

It is presented in Figure 2.11 that the measured V_{DS} and I_D values when $V_{GS} = 2.2$V and $V_{GS} = 2.4$V respectively. It can be seen that more current flows through the power device during the measurement, and it takes more time for the V_{DS} and I_D to stabilize. When $V_{GS} = 2.2$V, V_{DS} and I_D values can be obtained at about $40\mu s$ and when $V_{GS} = 2.4$V, they can be obtained at about $45\mu s$[4]. The power dissipation and $\triangle T_j$ are calculated with the same method and the results are presented in Figure 2.12. It can be seen that the maximal power dissipation during the measurement is 1700W. When $V_{GS} = 2.2$V, if V_{DS} and I_D values are obtained at $40\mu s$, $\triangle T_j$ is about 8 °C; When $V_{GS} = 2.4$V, if V_{DS} and I_D values are obtained at $45\mu s$, $\triangle T_j$ is about 5.7 °C. The influence of the T_j on power device static characteristics can still be neglected in the above measurements.

[4] I_D stabilize, which indicates that the device is in linear region, even though V_{DS} has not been stabilized at this moment, the obtained value does not influence a lot the measured static characteristic (I_D-V_{DS} plot).

It is shown in Figure 2.13 the measured SiC JFET static characteristics at different T_j, which varies from 25°C to 120 °C. Compared to its technical datasheet values, the presented method helps to increase V_{DS} value from 6V (in datasheet) up to 30V and helps to get I_D evolution on more V_{GS} values. Therefore, it helps to know better power devices characteristics than their technical datasheet values. When the power device is in ohmic region, its $R_{ds(on)}$ evolution with T_j can be calculated and is shown in Figure 2.14(a). The $R_{ds(on)}$ is calculated when $I_D = 10A$. It is shown that $R_{ds(on)}$ increases when T_j increases for the same V_{GS} value and it decreases as expected when V_{GS} increases for the same T_j value. When the power device is in linear region, its transconductance, which shows the relation between I_D and V_{GS}, is presented in Figure 2.14(b), where V_{DS} is taken to be 20V. It can be seen that when V_{GS} is inferior to 1.6V, the SiC JFET has a positive temperature coefficient and when V_{GS} is superior to 1.6V, the power device temperature coefficient becomes negative.

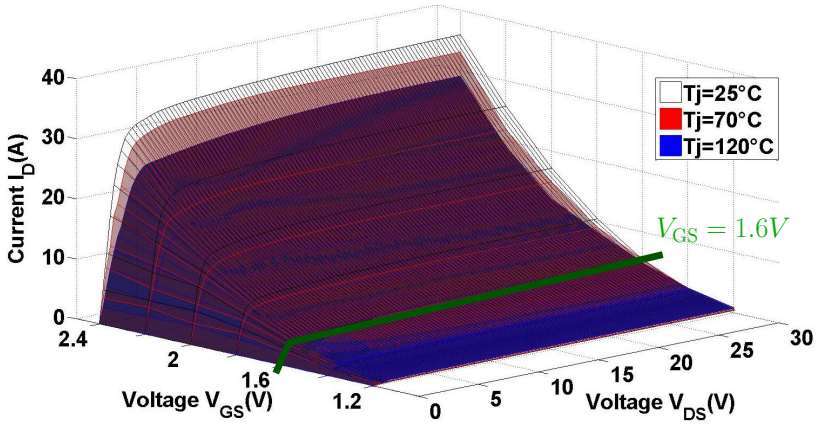
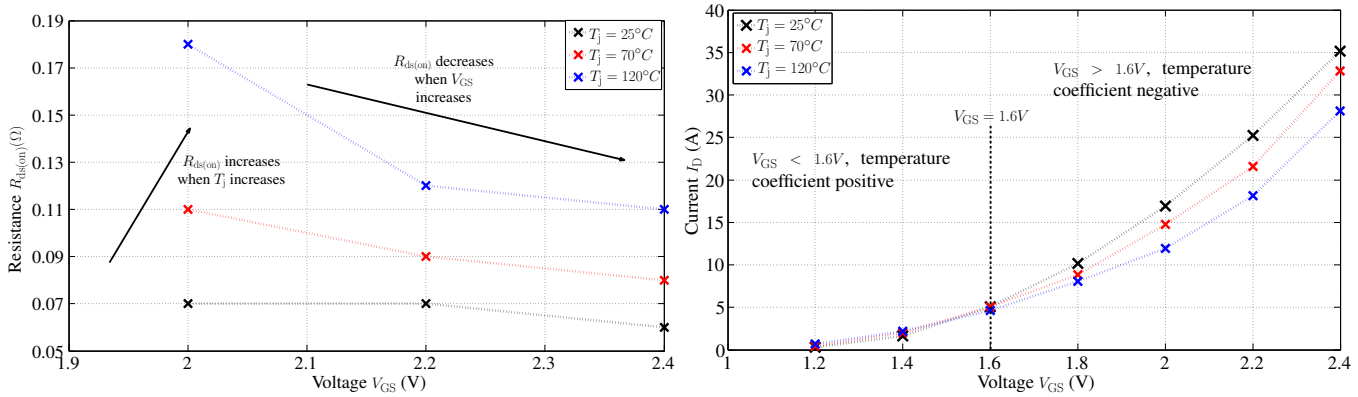


FIGURE 2.13: JFET static characteristics at different T_j



(a) $R_{ds(on)}$ at different T_j and $I_D = 10A$ (b) Transconductance at different T_j and $V_{DS} = 20V$

FIGURE 2.14: JFET $R_{ds(on)}$ and transconductance on different T_j

It is to be noted that when V_{GS} and V_{DS} increase, there is more power dissipated in the device, and it may take more time to stabilize the I_D and V_{DS}, thus junction temperature is likely to increase in this case, which limits the method.

All the above measured power device static characteristics results are intended to propose their models, which will be presented in Chapter 3.

2.2 Dynamic Characteristics Measurement Method

As presented in Chapter 1.2.2, the proposed method based on multiple current probes (MCP) is to be detailed in this section. At first, the method by using one Current Injection Probe (CIP) and another Current Receiving Probe (CRP) is applied for the inter-electrode capacitances measurement of a Si MOSFET (IRFB9N60A).

Afterwards, a Normally-off trench SiC JFET (SJEP120R063) has been likewise characterized. The principle and results of this method are presented in the following Chapter 2.2.1. Then, to increase its measurement accuracy, a third CRP is added in the circuit configuration for the capacitance measurement of the same power devices, which is presented in Chapter 2.2.2. Results are compared between the two methods. Afterwards, the method to increase the multiple current probes characterization sensibility is presented in Chapter 2.2.3 and applied to a GaN HEMT.

2.2.1 Two-current-probe method

2.2.1.1 Principle

The principle of the two-current-probe method is detailed in [58]. The basic setup of this method to measure an unknown impedance $\underline{Z_x}$ is illustrated in Figure 2.15.

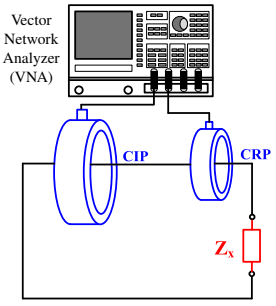


FIGURE 2.15: Basic setup of the measurement with two current probes and vector network analyzer

The measurement system is constituted of a vector network analyzer (VNA), a current injection probe and a current receiving probe. The current probes are modeled as equivalent transformers. By setting an equivalent circuit of this configuration [58], the following equation can be obtained:

$$\underline{Z_x} = \underline{K} \cdot \left(\frac{\underline{S_{11}} + 1}{\underline{S_{21}}} \right) - \underline{Z_{setup}} \tag{2.5}$$

where $\underline{K}$ is a parameter that represents the coupling effect between current probes and connecting wires. $\underline{Z_{setup}}$ is another parameter that represents the insertion impedance of the current probes and connecting wires. $\underline{S_{11}}$ and $\underline{S_{21}}$ are S-parameters that are measured by VNA. $\underline{K}$ and $\underline{Z_{setup}}$ are first determined by replacing $\underline{Z_x}$ in Figure 2.15 with two precision standard resistors so as to obtain two

equations from these preliminary measurements. Once these equations are solved and $\underline{K}$ and $\underline{Z_{\text{setup}}}$ are found, eq.(2.5) can be used to measure the unknown impedance $\underline{Z_{\text{x}}}$ by means of S parameters.

It is proposed to apply this method for the characterization of inter-electrode capacitances, which makes it possible to polarize the device under tester independently from the measurement system.

2.2.1.2 Characterization configurations

In the aim of validating the proposed methods, inter-electrode capacitance measurements have been carried out on power devices that are biased off, so as to permit comparison with datasheets information.

The inter-electrode capacitances of the Si MOSFET are firstly measured with this method. This MOSFET has been chosen as a reference for the method validation because its datasheet provides the inter-electrode capacitances evolutions up to 400V of V_{DS} (log-log scale) [117]. Furthermore, its inter-electrode capacitances evolutions below 40V of V_{DS} are verified by means of an impedance analyzer (HP4294A, 40Hz-110MHz) with the method proposed in [51] and the circuit presented in Chapter 1.2.2 to prove the validity of the datasheet information in low voltage. The bias voltage for V_{DS} is obtained by applying an external DC power source, of which the impedance is stabilized by a Line Impedance Stabilization Network (LISN). The impedance of the LISN may be included in the final measurement results, in which case the determination of $\underline{K}$ and $\underline{Z_{\text{setup}}}$ (equation (2.5)) may be obtained by the configuration shown in Figure 2.16(a), where R_1 and R_2 represent two known resistors used for obtaining two equations. The vector network analyzer Agilent E5071C (9kHz-4.5GHz) is used for S-parameters measurement. Current probes FCC F-120-3 (10kHz-100MHz) and FCC F35 (1kHz-100MHz) are used as the current injection probe and current receiving probe respectively, while EMCO 3180/2 (9kHz-30MHz) is used as the LISN. To compare with the datasheet, the inter-electrode capacitances of the power devices are measured around 1MHz. Below 1MHz, the mutual inductance between two probes can be neglected. As there are three inter-electrode capacitances of a MOSFET, this method is applied to measure the sum of two capacitances in three measurements, the measurement configuration of which is shown in Figure 2.16.

- The circuit configuration used to measure $C_{\text{oss}} = C_{\text{ds}} + C_{\text{gd}}$ is shown in Figure 2.16(b). Gate and source are short circuited to ensure that the MOSFET is in off state. It could be noted that in this measurement, the impedance of the LISN is already included into Z_{setup} (equation (2.5)).
- The circuit configuration to measure $C_{\text{iss}} = C_{\text{gs}} + C_{\text{gd}}$ is shown in Figure 2.16(c). Gate and source of the MOSFET are short circuited to keep it in off state. Moreover, drain and source have to be short-circuited in AC (at 1MHz) while a DC bias voltage is applied between these terminals. For that means, an additional capacitor is connected between drain and source; its value (2.2μF) is chosen so that the capacitor impedance around 1MHz is much smaller

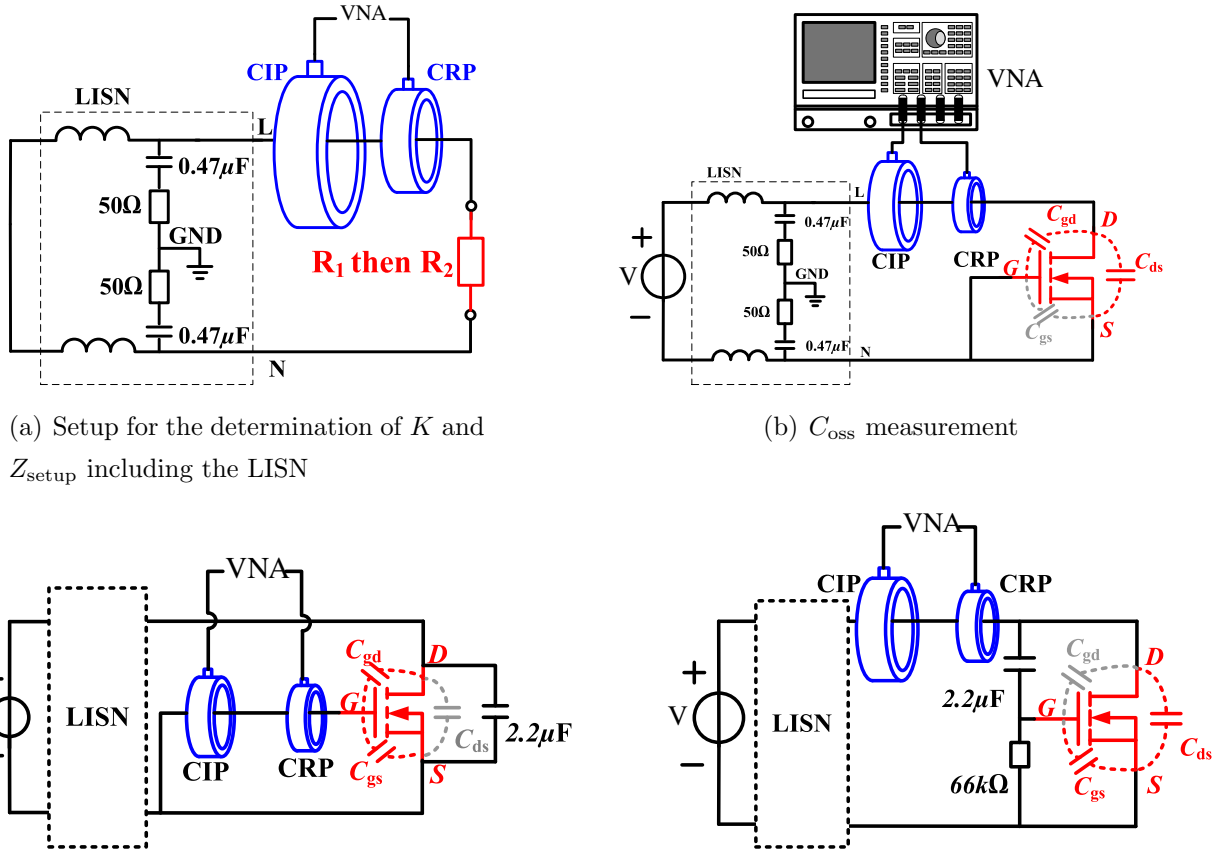
than that of both C_{ds} and the LISN (100Ω). Thus, the total capacitance measured in this configuration is:

$$C_{measure} = C_{gs} + \frac{C_{gd} \cdot 2.2\mu F}{C_{gd} + 2.2\mu F}. \tag{2.6}$$

Since C_{gd} is much smaller than 2.2μF, C_{iss} is directly obtained in this configuration.

- The circuit configuration used to measure the sum of C_{ds} and C_{gs} (this term is called $C_x = C_{ds} + C_{gs}$) is shown in Figure 2.16(d). A 2.2μF capacitor is connected between gate and drain of the MOSFET and a resistor ($R = 66k\Omega$) is connected between gate and source. As C_{gd} is much smaller than 2.2μF, drain and gate are short circuited in AC. The role of the resistor R is to discharge C_{gs} so as to keep V_{gs} lower than its threshold voltage (MOSFET is in off state). Furthermore, around 1MHz, the impedance of this resistor R is much bigger than that of C_{gs} which guarantees that the injected current flows through C_{gs}. Similar to the C_{oss} measurement, the impedance of the LISN is included into Z_{setup}. C_{gd} can then be obtained indirectly by :

$$C_{gd} = \frac{C_{iss} + C_{oss} - C_x}{2}. \tag{2.7}$$



(a) Setup for the determination of K and Z_{setup} including the LISN

(b) C_{oss} measurement

(c) C_{iss} measurement

(d) C_x measurement

FIGURE 2.16: Si MOSFET inter-electrode capacitances measurement by two-current-probe method

2.2.1.3 Characterization results

The results of the measured capacitances of the MOSFET compared to the datasheet are shown in Figure 2.17.

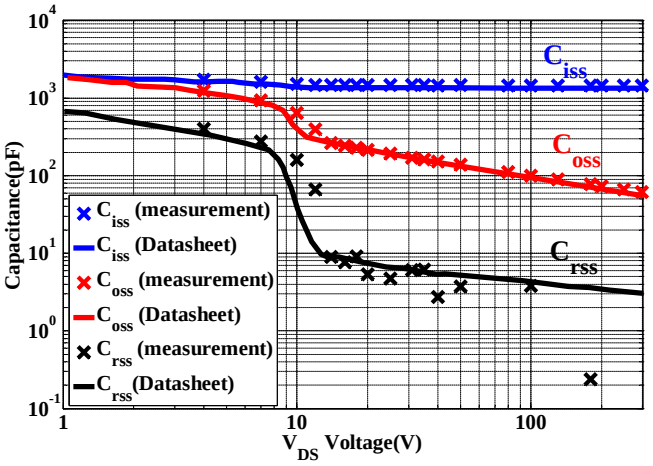
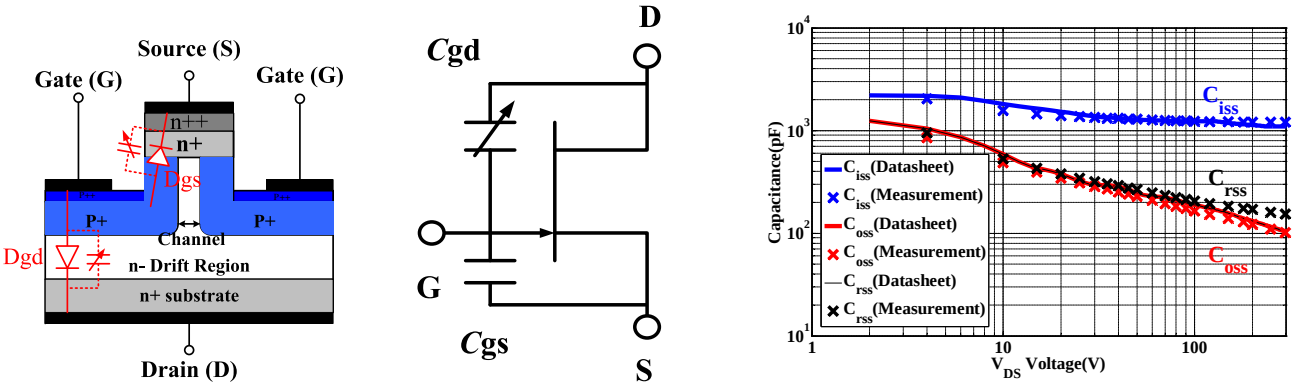


FIGURE 2.17: Result of the Si MOSFET inter-electrode capacitances measurement by two-current-probe method

From these results, the values of C_{iss} and C_{oss} in the datasheet concur well with the values measured by applying the above method, so the validity of this method seems to be confirmed. However, the obtained value of C_{rss} (equals to C_{gd}) appears inaccurate and even negative values are found when V_{DS} is above 200V. The reason is that C_{rss} is not measured directly: it is obtained in an indirect way (equation (2.7)). Furthermore, at high voltage, C_{rss} (a few pF) is much smaller than C_{iss} and C_{x} (several nF), of which the subtraction in equation (2.7) involves propagation of measurement errors. As a consequence, the result may be unreliable.



(a) SiC JFET structure

(b) Inter-electrode capacitances

(c) Measurement results

FIGURE 2.18: SiC JFET structure and inter-electrode capacitances measurement results by two-current-probe method

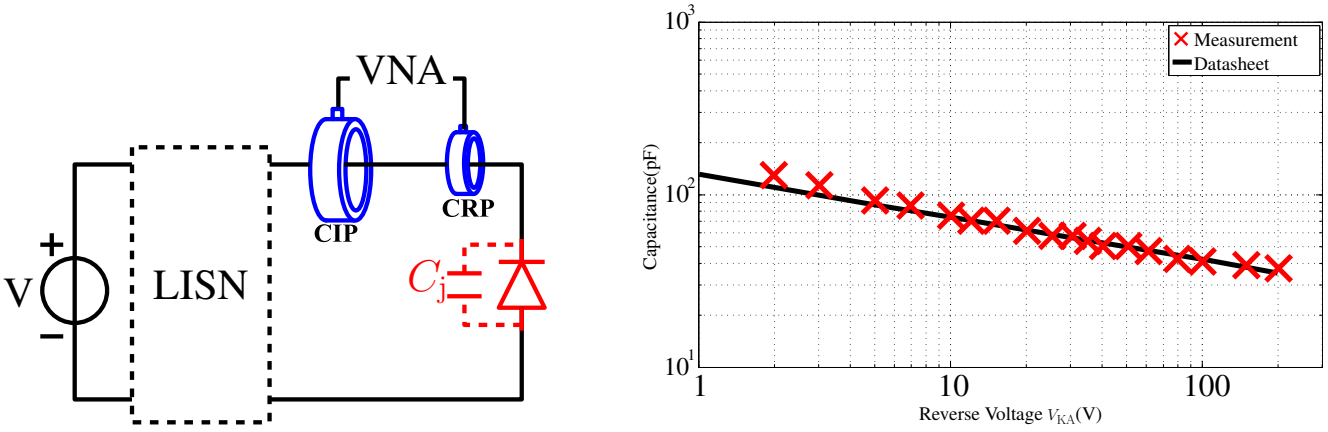
The same method is then applied to measure the inter-electrode capacitances of the SiC JFET (SJEP120R063), of which the structure is shown in Figure 2.18(a). It can be seen that in its

structure, there is no inter-electrode capacitance C_{ds} (Figure 2.18(b)). As shown in the datasheet of the JFET [118] as well, C_{rss} and C_{oss} are considered as the same capacitance because C_{ds} can be neglected. This is quite different from a MOSFET.

The results of the measured capacitances of the JFET compared to the datasheet are shown in Figure 2.18(c). From the results, the values of C_{iss} and C_{oss} in the datasheet correspond to the values measured by applying the above method. However, the obtained value of C_{rss} appears superior to C_{oss}, which is a non-physical result. Again, it can be explained by the indirect measurement of C_{rss}, as the previous paragraph stated in the case of the MOSFET.

Thus, the two-current-probe method is able to measure the inter-electrode capacitance of the power device in high voltage while providing isolation of the measurement power circuits from the DC bias source.

It is to be noted that as there are only two terminals anode (A) and cathode (K) of a power diode, the presented two-current-probe method is totally adapted to characterize power diode junction capacitance C_j at high blocking voltage V_{KA}. The measurement circuit is shown in Figure 2.19(a). It is shown in Figure 2.19(b) the inter-electrode capacitance measurement result of a power diode (STTH15R06) in comparison with its datasheet values, which confirms the validity of the presented method.



(a) Measurement circuit

(b) Measurement results

FIGURE 2.19: Power diode (STTH15R06) measurement circuit and capacitance measurement results

In conclusion, it can be noted that for a power transistor, only the sum of two inter-electrode capacitances can be measured and C_{rss} is not measured directly. Its value is obtained by calculation, so it is possible that C_{rss} is calculated negative (as the MOSFET example has shown) or superior to C_{oss} (JFET example). The two-current-probe method needs to be improved to resolve this problem, so C_{rss} can be measured directly and thereby, accurately. In the following section, a three-current-probe method is proposed.

2.2.2 Three-current-probe method

One additional current receiving probe is added to improve the two-current-probe method so as to better adapt this method to the inter-electrode capacitances measurement of power transistors. The proposed method is constituted of one current injection probe and two current receiving probes as shown in Figure 2.20.

2.2.2.1 Principle

The principle of the proposed three-current-probe method is: Port 1 generates an AC signal through the CIP, this current is measured at port 2 and at port 3 individually by two CRPs. Unlike the two-current-probe method, the impedance of each branch can be obtained with this three-current-probe method.

The equivalent circuit of the measurement is shown in Figure 2.21. $\underline{V_1}$ is the signal source of VNA port 1, while $\underline{V_{p1}}$, $\underline{V_{p2}}$ and $\underline{V_{p3}}$ are the resultant signal voltages measured at port 1, port 2 and port 3 respectively. The output impedance of port 1 and input impedance of port 2 and port 3 are all $Z_0 = 50\Omega$. $\underline{Z_{p1}}$, $\underline{Z_{p2}}$ and $\underline{Z_{p3}}$ are the input impedances of the injection and the receiving probes respectively. The impedances of the wire connections in each part are represented by $\underline{Z_w}$, $\underline{Z_{w1}}$ and $\underline{Z_{w2}}$. M_1, M_2 and M_3 are mutual inductances between the probe and the circuit correspondingly. $\underline{V_1}$ induces a current $\underline{I_w}$ in the circuit through the injection probe. $\underline{I_w}$ is divided into $\underline{I_{w1}}$ and $\underline{I_{w2}}$ which flow through two unknown impedances in parallel. $\underline{V_{x1}}$ and $\underline{V_{x2}}$ are the voltages across the unknown impedances. $\underline{I_{w1}}$ and $\underline{I_{w2}}$ are measured by two receiving probes, which induces $\underline{I_2}$ and $\underline{I_3}$ in port 2 and port 3 respectively through the receiving probes. From Figure 2.21, five equations based on Kirchhoff's Voltage Law are obtained in the matrix equations (2.8). Eliminating $\underline{I_1}$, $\underline{I_2}$, and $\underline{I_3}$ in equations (2.8) and applying $\underline{I_w} = \underline{I_{w1}} + \underline{I_{w2}}$, equations (2.8) can be simplified into the following equations (2.9) and (2.10):

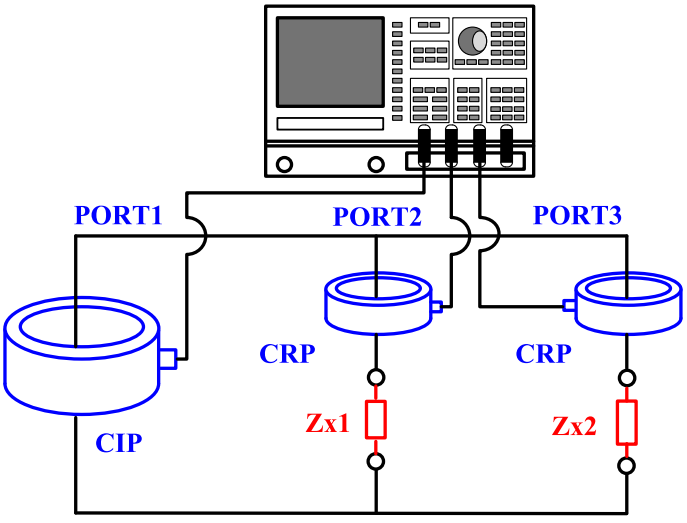


FIGURE 2.20: Configuration of the measurement by three-current-probe method

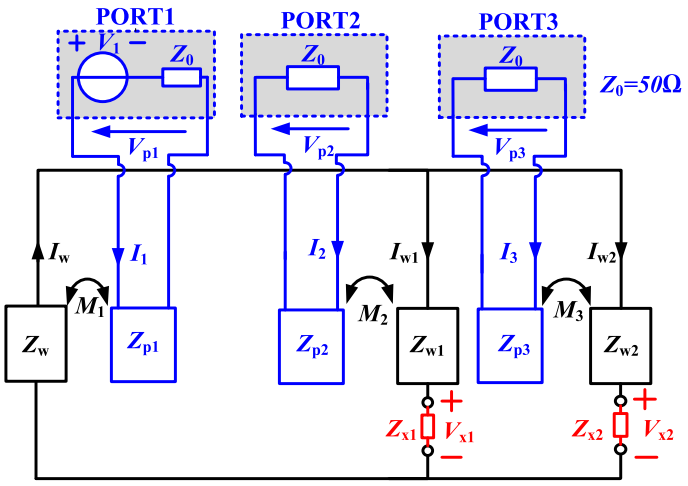


FIGURE 2.21: Equivalent circuit of the three-current-probe measurement

$$\begin{bmatrix} \underline{V_1} \\ 0 \\ \underline{V_{x1}} \\ 0 \\ \underline{V_{x2}} \end{bmatrix} = \begin{bmatrix} (50+\underline{Z_{p1}}) & 0 & 0 & -j\omega M_1 & 0 & 0 \\ 0 & (50+\underline{Z_{p2}}) & 0 & 0 & j\omega M_2 & 0 \\ j\omega M_1 & -j\omega M_2 & 0 & -\underline{Z_w} & -\underline{Z_{w1}} & 0 \\ 0 & 0 & (50+\underline{Z_{p3}}) & 0 & 0 & j\omega M_3 \\ j\omega M_1 & 0 & -j\omega M_3 & -\underline{Z_w} & 0 & -\underline{Z_{w2}} \end{bmatrix} \times \begin{bmatrix} \underline{I_1} \\ \underline{I_2} \\ \underline{I_3} \\ \underline{I_w} \\ \underline{I_{w1}} \\ \underline{I_{w2}} \end{bmatrix} \tag{2.8}$$

$$\underline{V_{M1}} = (\underline{Z_M} + \underline{Z_w}) \cdot (\underline{I_{w1}} + \underline{I_{w2}}) + (\underline{Z_{M1}} + \underline{Z_{w1}} + \underline{Z_{x1}}) \cdot \underline{I_{w1}} \tag{2.9}$$

$$\underline{V_{M1}} = (\underline{Z_M} + \underline{Z_w}) \cdot (\underline{I_{w1}} + \underline{I_{w2}}) + (\underline{Z_{M2}} + \underline{Z_{w2}} + \underline{Z_{x2}}) \cdot \underline{I_{w2}}. \tag{2.10}$$

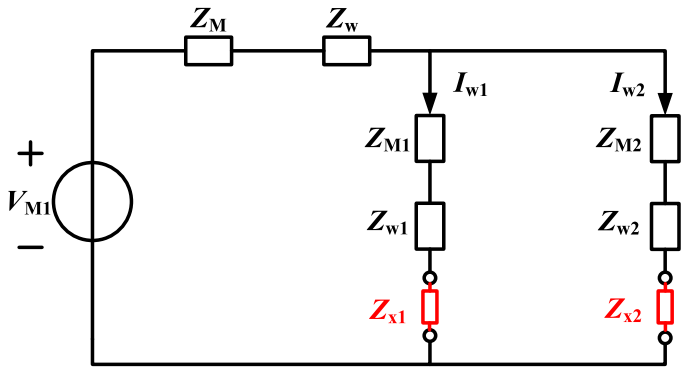


FIGURE 2.22: Final equivalent circuit of the three-current-probe measurement

With equations (2.9) and (2.10), the equivalent circuit of the measurement (Figure 2.21) can then be obtained in Figure 2.22, in which $\underline{V_{M1}}$ is an equivalent voltage source in the measurement circuit.

$\underline{Z_{\mathrm{M}}}$, $\underline{Z_{\mathrm{M1}}}$ and $\underline{Z_{\mathrm{M2}}}$ are the equivalent impedances in the measurement circuit of the CIP and CRPs respectively. These parameters represent the coupling effect between the current probes and the measurement circuits, whose expressions are listed below:

$$\begin{aligned}
\underline{V_{\mathrm{M1}}} &= \frac{j\omega M_1 \underline{V_{\mathrm{p1}}}}{\underline{Z_{\mathrm{p1}}}} \\
\underline{Z_{\mathrm{M}}} &= \frac{(\omega M_1)^2}{50 + \underline{Z_{\mathrm{p1}}}} \\
\underline{Z_{\mathrm{M1}}} &= \frac{(\omega M_2)^2}{50 + \underline{Z_{\mathrm{p2}}}} \\
\underline{Z_{\mathrm{M2}}} &= \frac{(\omega M_3)^2}{50 + \underline{Z_{\mathrm{p3}}}}.
\end{aligned} \tag{2.11}$$

$\underline{I_{\mathrm{w1}}}$ and $\underline{I_{\mathrm{w2}}}$ can be measured by the receiving probes,

$$\underline{I_{\mathrm{w1}}} = \frac{\underline{V_{\mathrm{p2}}}}{\underline{Z_{\mathrm{T2}}}} \tag{2.12}$$

$$\underline{I_{\mathrm{w2}}} = \frac{\underline{V_{\mathrm{p3}}}}{\underline{Z_{\mathrm{T3}}}} \tag{2.13}$$

where $\underline{Z_{\mathrm{T2}}}$ and $\underline{Z_{\mathrm{T3}}}$ are the respective transfer impedance of the receiving probes. $\underline{V_{\mathrm{p1}}}$, $\underline{V_{\mathrm{p2}}}$ and $\underline{V_{\mathrm{p3}}}$ can be obtained with the transfer parameter (S-parameters) definition in the vector network analyzer:

$$\underline{V_{\mathrm{p1}}} = \underline{V_1} \cdot \left(\frac{\underline{S_{11}} + 1}{2} \right) \tag{2.14}$$

$$\underline{V_{\mathrm{p2}}} = \underline{V_1} \cdot \frac{\underline{S_{21}}}{2} \tag{2.15}$$

$$\underline{V_{\mathrm{p3}}} = \underline{V_1} \cdot \frac{\underline{S_{31}}}{2}. \tag{2.16}$$

Equations (2.17) and (2.18) are finally obtained by replacing equations (2.12)-(2.16) into equations (2.9) and (2.10):

$$\underline{Z_{\mathrm{x1}}} = \left(\frac{j\omega M_1}{\underline{Z_{\mathrm{p1}}}} \cdot \underline{Z_{\mathrm{T2}}} \right) \cdot \left(\frac{\underline{S_{11}} + 1}{\underline{S_{21}}} \right) - \left(\underline{Z_{\mathrm{M}}} + \underline{Z_{\mathrm{w}}} + \underline{Z_{\mathrm{M1}}} + \underline{Z_{\mathrm{w1}}} \right) - \left(\frac{\underline{Z_{\mathrm{M}}} + \underline{Z_{\mathrm{w}}}}{\underline{Z_{\mathrm{T3}}}} \cdot \underline{Z_{\mathrm{T2}}} \right) \cdot \left(\frac{\underline{S_{31}}}{\underline{S_{21}}} \right) \tag{2.17}$$

$$\underline{Z_{x2}} = \left(\frac{j\omega M_1}{\underline{Z_{p1}}} \cdot \underline{Z_{T3}}\right) \cdot \left(\frac{\underline{S_{11}}+1}{\underline{S_{31}}}\right) - (\underline{Z_M} + \underline{Z_w} + \underline{Z_{M2}} + \underline{Z_{w2}}) - \left(\frac{\underline{Z_M} + \underline{Z_w}}{\underline{Z_{T2}}} \cdot \underline{Z_{T3}}\right) \cdot \left(\frac{\underline{S_{21}}}{\underline{S_{31}}}\right). \quad (2.18)$$

Unknown impedances $\underline{Z_{x1}}$ and $\underline{Z_{x2}}$ can finally be expressed as

$$\underline{Z_{x1}} = \underline{K_1} \cdot \left(\frac{\underline{S_{11}}+1}{\underline{S_{21}}}\right) - \underline{Z_{setup1}} - \underline{Q_1} \cdot \left(\frac{\underline{S_{31}}}{\underline{S_{21}}}\right) \quad (2.19)$$

$$\underline{Z_{x2}} = \underline{K_2} \cdot \left(\frac{\underline{S_{11}}+1}{\underline{S_{31}}}\right) - \underline{Z_{setup2}} - \underline{Q_2} \cdot \left(\frac{\underline{S_{21}}}{\underline{S_{31}}}\right) \quad (2.20)$$

where $\underline{K_1}$ represents the coupling effect between the current probes in port 1 and 2 with the connecting wires; $\underline{K_2}$ represents the coupling effect between the current probes in port 1 and 3 with the connecting wires; $\underline{Z_{setup1}}$ represents the impedance of the current probes in port 1 and 2 with the connecting wires; $\underline{Z_{setup2}}$ represents the impedance of the current probes in port 1 and 3 with the connecting wires; $\underline{Q_1}$ and $\underline{Q_2}$ represent the coupling effect of two CRPs and the impedance of the CIP with the connecting wires. The parameters $\underline{K_1}$, $\underline{K_2}$, $\underline{Z_{setup1}}$, $\underline{Z_{setup2}}$, $\underline{Q_1}$ and $\underline{Q_2}$ can be obtained by the following steps. Firstly, $\underline{Z_{x1}}$ and $\underline{Z_{x2}}$ in Figure 2.20 can be replaced by two precision standard resistors R_1 and R_2 to have two equations: (2.21) and (2.22). As there are six parameters to be determined, four more equations are needed.

It is necessary to repeat the above step twice and in each step, two precision standard resistors of different values can be used to have two more different equations. By resolving the six equations, the above six parameters can be obtained.

$$R_1 = \underline{K_1} \cdot \left(\frac{\underline{S_{11}}+1}{\underline{S_{21}}}\right)\Bigg|_{\underline{Z_{x1}}=R_1} - \underline{Z_{setup1}} - \underline{Q_1} \cdot \left(\frac{\underline{S_{31}}}{\underline{S_{21}}}\right)\Bigg|_{\underline{Z_{x1}}=R_1} \quad (2.21)$$

$$R_2 = \underline{K_2} \cdot \left(\frac{\underline{S_{11}}+1}{\underline{S_{31}}}\right)\Bigg|_{\underline{Z_{x2}}=R_2} - \underline{Z_{setup2}} - \underline{Q_2} \cdot \left(\frac{\underline{S_{21}}}{\underline{S_{31}}}\right)\Bigg|_{\underline{Z_{x2}}=R_2} \quad (2.22)$$

This three-current-probe method can be used now to measure inter-electrode capacitances of the power devices in a direct manner.

2.2.2.2 Characterization configurations

In this section, the proposed three-current-probe method is applied for measuring inter-electrode capacitances when power devices are biased off, in order to compare with datasheet information when it is available.

Similar to the two-current-probe measurement method, the impedance of the LISN may be included in the final measurements, in which case the determination of the six parameters (equations (2.19) and (2.20)) can be obtained by the configuration shown in Figure 2.23 where R_1 and R_2 are chosen with the following three groups of values: 50Ω/50Ω, 50Ω/33Ω and 33Ω/50Ω. Thus, with those configurations to determine the six parameters, $\underline{Z_{\text{setup1}}}$ and $\underline{Z_{\text{setup2}}}$ not only represents the impedance of the current probes with the connecting wires, but also the LISN impedance.

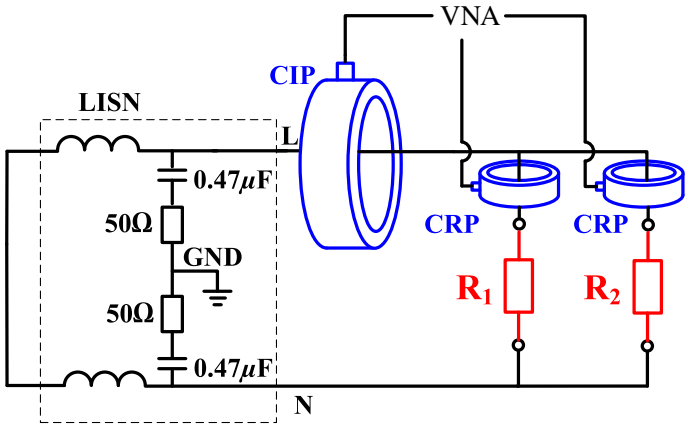
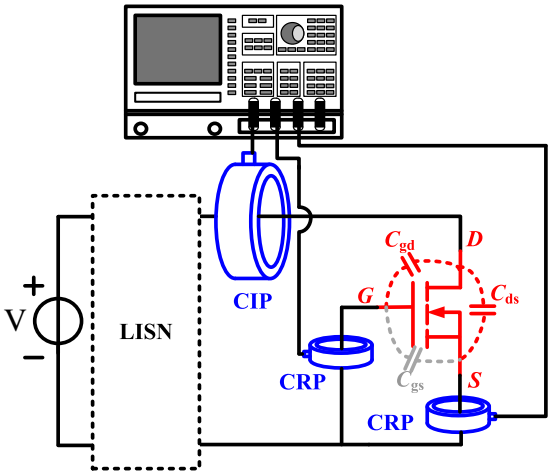
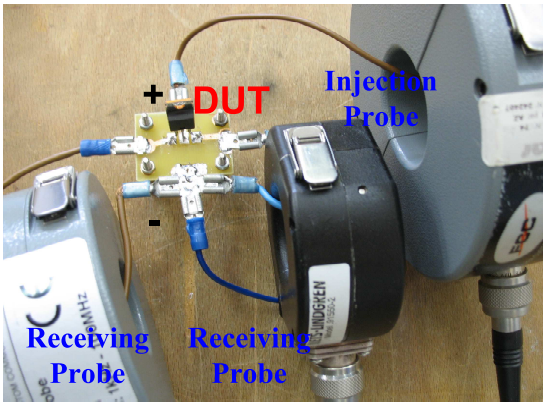


FIGURE 2.23: Parameters determination of the three-current-probe method



(a) Measurement configuration using three current probes



(b) Measurement photo

FIGURE 2.24: MOSFET inter-electrode capacitances measurement by three-current-probe method

This method is applied to measure the inter-electrode capacitances of the same MOSFET and SiC JFET as presented in Chapter 2.2.1.3. The objective of this method is to measure C_{gd} directly with more accuracy. The configuration of the measurement system is shown in Figure 2.24(a), while the

practical operation is shown in Figure 2.24(b). The gate and source of the MOSFET are in short-circuit. The injected current is divided into two branches: in one branch where C_{gd} is located, the current is measured by one CRP and in another branch where C_{ds} is located, the current is measured by another CRP.

Before the power device inter-electrode capacitances are measured, the sensibility of this three-current-probe method could be considered. Indeed, unlike the two-current-probe method where C_{gd} is difficult to obtain, an obvious advantage of three-current-probe method is to measure it directly. Yet, inter-electrode C_{gd} is usually small: about a few dozen pF to several pF in high voltage for a power transistor depending on its structure. Thus, the sensibility of the three-current-probe method to measure a capacitance of a few pF has to be proved. Moreover, the second capacitor to be measured in the parallel branch of Figure 2.20 could be of a completely different value. For those reasons and in worse case of very low capacitance value, a 1pF capacitor and a 10pF capacitor are chosen as the unknown impedances to be measured with the configuration in Figure 2.20. The measurement value in the impedance analyzer is 1.07pF and 10.07pF for each capacitor. The measurement results by the three-current-probe method are shown in Figure 2.25. As shown in the result, the average values of each capacitor measured by the three-current-probe method around 1MHz is 1.26pF and 10.33pF, with 17.7% and 2.6% the relative error compared to the impedance analyzer measurement. This result allows to validate the sensibility of this method to measure small inter-electrode capacitances of a power semiconductor device. The solution to further increase the accuracy of this method will be presented in Chapter 2.2.3.

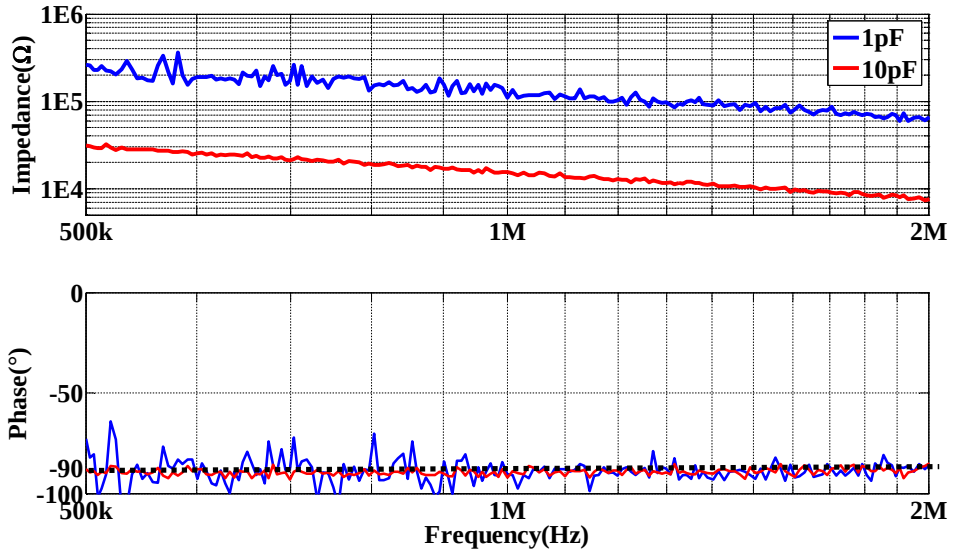
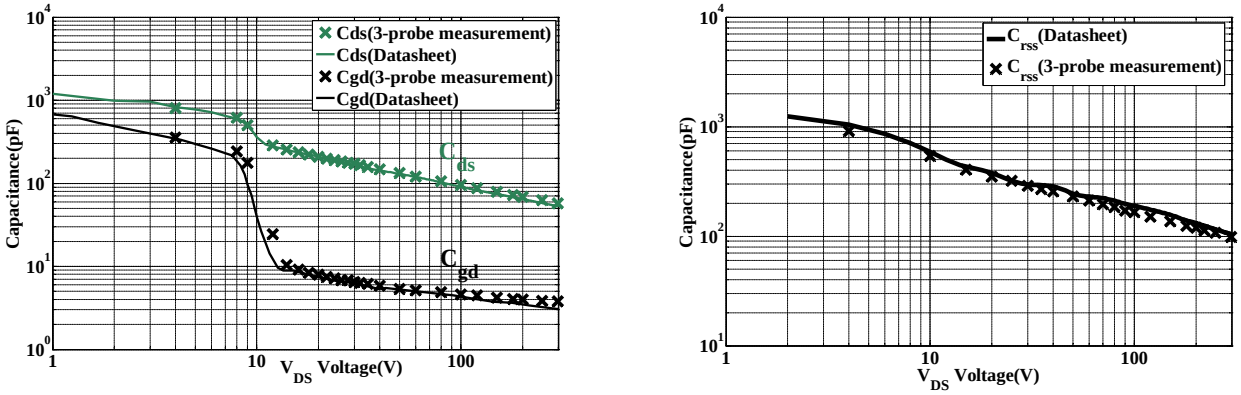


FIGURE 2.25: Result of the 1pF and 10pF capacitor measurements

2.2.2.3 Characterization results

The measurement results of inter-electrode capacitances of the Si MOSFET with the proposed three-current-probe method compared to the datasheet are shown in Figure 2.26(a). It is shown that the

measurement of both C_{ds} and C_{gd} with three-current-probe method concurs well with the datasheet, so the validity of the three-current-probe method can be confirmed.



(a) Si MOSFET(IRFB9N60A)

(b) SiC JFET(SJEP120R063)

FIGURE 2.26: C_{rss} measurement result by three-current-probe method

For this MOSFET, the two-current-probe method became inaccurate for C_{rss} measurement when V_{DS} was over 30V and even negative values appeared. The numerical calculation comparison between these two methods in C_{rss} measurement when V_{DS} is above 30V is shown in TABLE 2.1. Three terms are compared based on the relative error (ε_{r}) between the measurement ($C_{\mathrm{rss(m)}}$) and the datasheet ($C_{\mathrm{rss(d)}}$):

$$\varepsilon_{\mathrm{r}} = \frac{C_{\mathrm{rss(d)}} - C_{\mathrm{rss(m)}}}{C_{\mathrm{rss(d)}}} \tag{2.23}$$

Both the mean value ($\bar{\varepsilon_{\mathrm{r}}}$), the standard derivation ($\sigma(\varepsilon_{\mathrm{r}})$), and the maximum absolute value ($|\varepsilon_{\mathrm{r}}|_{(\mathrm{max})}$) of this error are reported in TABLE 2.1. It is to be noted that the datasheet has been chosen here as a reference, though it remains unclear which of the datasheet or the measurement is closer to the real capacitance value in high voltage. With three-current-probe method, as C_{rss} is measured directly, negative values are avoided and the maximum error drops from 166.0% to 24.0%. Furthermore, the three-current-probe method helps to decrease $\sigma(\varepsilon_{\mathrm{r}})$ and $|\bar{\varepsilon_{\mathrm{r}}}|$ (down to 7.5% and 9.7%, respectively), which proves that the three-current-probe method is more stable and accurate than the two-current-probe method for C_{rss} measurement.

TABLE 2.1: Numerical calculation between two-current-probe method and three-current-probe method in C_{rss} measurement of Si MOSFET (IRFB9N60A)

Method	Two-current-probe	Three-current-probe
$\bar{\varepsilon_{\mathrm{r}}}$	83.2%	-9.7%
$\sigma(\varepsilon_{\mathrm{r}})$	58.5%	7.5%
$\lvert\varepsilon_{\mathrm{r}}\rvert_{(\mathrm{max})}$	166.0%	24.0%

The measurement results of C_{rss} for the SiC JFET with the three-current-probe method compared to the datasheet are shown in Figure 2.26(b). It is shown to concur well with the datasheet, which confirms the validity of this method again. More importantly, the measurement result of C_{rss} with three-current-probe method almost equals to C_{oss} (Figure 2.18(c)). This reasonable result resolves the problem in the two-current-probe measurement, which shows the accuracy of the three-current-probe method for C_{rss} measurement.

Finally, the proposed multi-probe method is applied for the capacitances measurement of an IGBT (IXGR40N60C2) as shown in Figure 2.27 in comparison with the datasheet as well as with a measurement using the Impedance Analyzer (I.A) based on the method proposed in [51]. As shown in the results, the datasheet of this particular device does not coincide with neither I.A measurement nor the proposed multi-probe measurement. Even though the I.A measurement is limited to 40V of V_{CE}, its results up to this voltage concur well with the proposed multi-probe method. This result suggests that the datasheet information should not always be blindly followed, and that proposing an effective method to measure inter-electrode capacitances is relevant in order to accurately characterize a power device. This is especially important when considering SiC or GaN power devices whose technical data in datasheets may be not fully complete or subject to future revisions. In this regard, the proposed method in this chapter provides the possibility to easily measure power devices inter-electrode capacitances and to compare them with other methods.

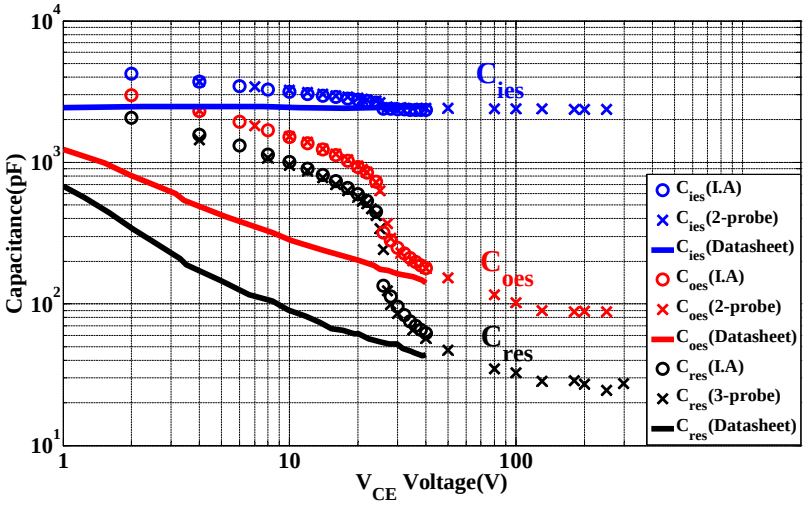


FIGURE 2.27: Result of the IGBT (IXGR40N60C2) inter-electrode capacitances measurement by the two methods compared to datasheet

2.2.3 Increase of multi-current-probe measurement method sensibility

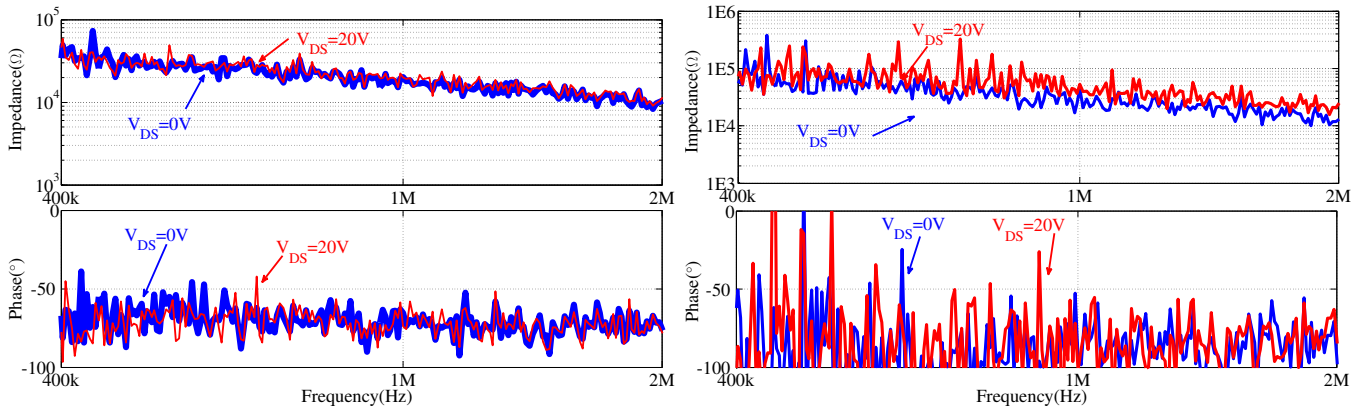
The method to increase the sensibility of the proposed multiple-current-probe (MCP) method is presented in this section.

2.2.3.1 When power device is blocked

As presented in Chapter 1.1, the inter-electrode capacitances of WBG power devices are very small which guarantees fast switching. For GaN power devices, the inter-electrode capacitances are typically around picofarads. Therefore, it is important to increase the MCP measurement method sensibility to accurately characterize small inter-electrode capacitance values.

For this reason, the inter-electrode capacitances of a normally-on radio-frequency (RF) power GaN HEMT (NPTB00025) is characterized. The measurement circuit is almost the same with that shown in Figure 2.24(b) except that a battery is used to supply a negative voltage between gate and source ($V_{\mathrm{GS}} = -5V$) to block the power device.

The C_{ds} impedance and phase measurement results when V_{DS} equals to 0V and 20V are shown in Figure 2.28(a), while those of C_{gd} are shown in Figure 2.28(b). As shown in the result, the measured values of both C_{ds} and C_{gd} is almost in the noise range of the VNA at 1MHz, which makes it difficult to obtain a precise value of the capacitance. The reason is that the inter-electrode capacitances of the GaN HEMT are so small that around 1MHz, the measured impedance by VNA is quite big, which yields a measurement sensibility issue.



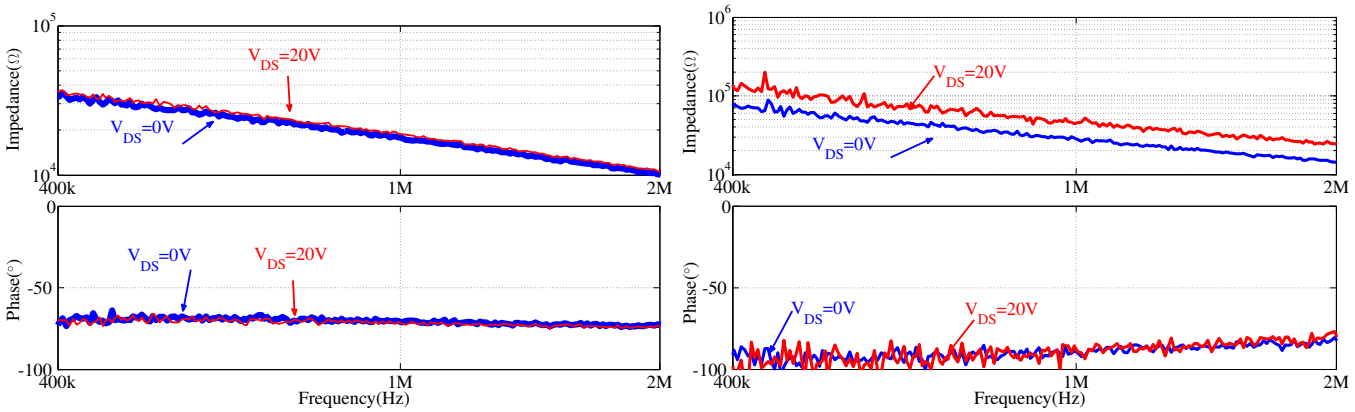
(a) C_{ds} impedance measurement result

(b) C_{gd} impedance measurement result

FIGURE 2.28: GaN HEMT inter-electrode capacitances measurement result of the three-current-probe method

To overcome this drawback, CRP is wound by six turns to increase its coupling effect with the measurement configuration, and thereby increase the sensibility of the proposed method. This modification does not modify the presented equations of three-current-probe method.

After this modification, the C_{ds} impedance and phase measurement results when V_{DS} equals to 0V and 20V are shown in Figure 2.29(a), while those of C_{gd} are shown in Figure 2.29(b). It is shown in the results that the sensibility of the three-current-probe method has been greatly improved. The GaN HEMT inter-electrode capacitances can be calculated with an average value around 1MHz (900kHz-1.1MHz) by calculating the obtained imaginary parts.



(a) C_{ds} impedance measurement result (b) C_{gd} impedance measurement result

FIGURE 2.29: GaN HEMT inter-electrode capacitances measurement result of the accurately improved three-current-probe method

The results of the measured capacitances of the HEMT using multi-current-probe method and impedance analyzer are shown in Figure 2.30, which show that the inter-electrode capacitances measured by the improved MCP method concur well with the impedance analyzer result, which proves that this improvement helps to increase measurement method sensibility to measure small capacitance values.

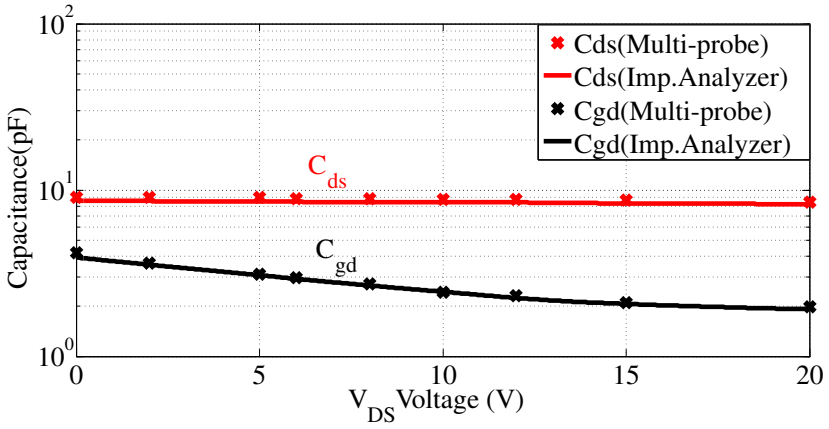


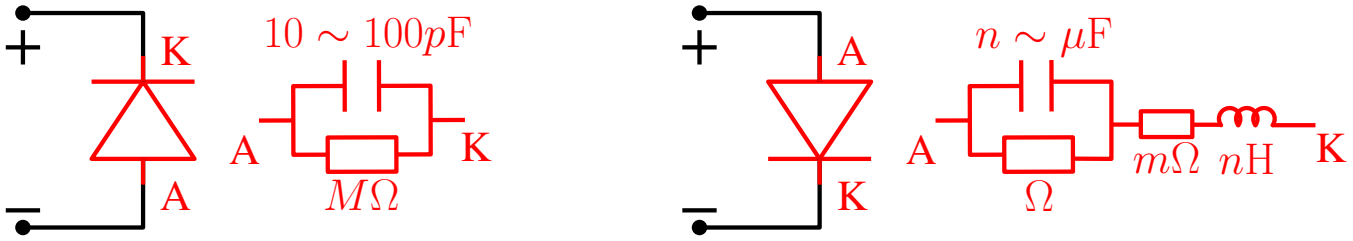
FIGURE 2.30: GaN HEMT inter-electrode capacitances measurement results comparison (V_{GS}= −5V)

2.2.3.2 When power device is in conduction

The presented multiple current probes method can not only be applied to characterize power semiconductor devices when they are blocked, but also can be applied to characterize power devices when they are in conduction in order to model power devices.

For the power ratings of diodes with 100 1000V blocking voltage and 1-10A direct current, it is shown and compared in Figure 2.31 the measured impedance of a power diode when it is blocked (OFF-state) and in conduction (ON-state). When the power diode is blocked, junction capacitance is mainly characterized, thus a big impedance is measured. However, when the power diode is in

conduction, not only capacitance is measured, but also the power device dynamic resistances and parasitic inductances. The impedance of the power device when it is polarized positively is very small in comparison with the case when it is blocked. Therefore, it is important and necessary to increase the proposed method measurement reliability in a large measurement frequency range to accurately characterize small impedance values when the power diode is in conduction.



(a) Equivalent circuit when blocked

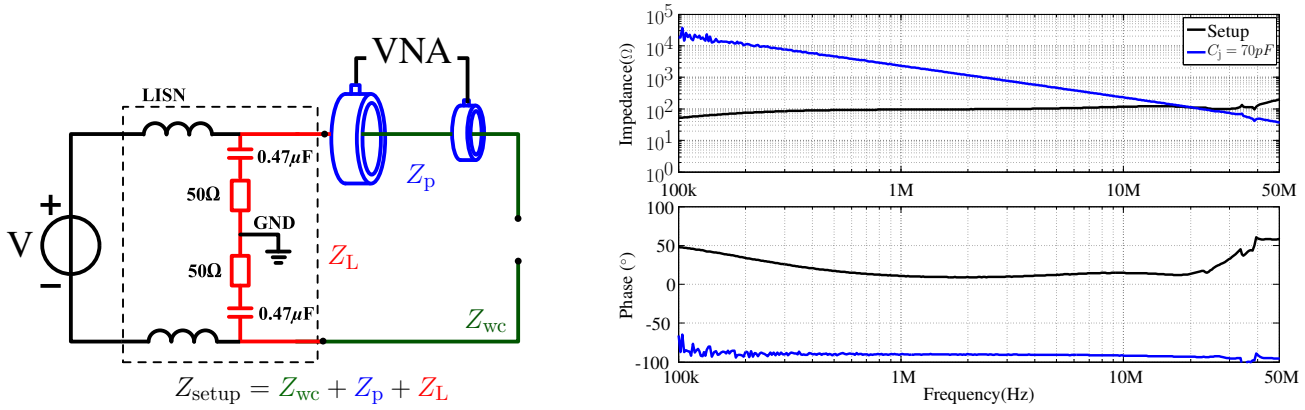
(b) Equivalent circuit when in conduction

FIGURE 2.31: Diode measurement impedance when blocked and in conduction

It is shown in equations (2.5), (2.19) and (2.20), that unknown impedance $\underline{Z_x}$ is obtained by subtracting $\underline{Z_{setup}}$ value. With the measurement circuit shown in Figure 2.19(a) to characterize diode junction capacitance C_j by two-current-probe method, $\underline{Z_{setup}}$ is illustrated in Figure 2.32(a), which is the sum of the connection wire impedance $\underline{Z_{wc}}$, the current probes insertion impedance $\underline{Z_p}$ and LISN impedance $\underline{Z_L}$. The measured $\underline{Z_{setup}}$ is shown in Figure 2.32(b) and it is compared with the measured diode impedance when $C_j = 70pF$. It is shown in Figure 2.32(b) that the measured C_j impedance is much bigger than $\underline{Z_{setup}}$ until 10MHz, thus a relatively small value $\underline{Z_{setup}}$ is subtracted in a relatively big value $\underline{K} \cdot \left(\frac{\underline{S_{11}}+1}{\underline{S_{21}}}\right)$ to get a relatively big value $\underline{Z_x}$ in equation (2.5), which brings small error and the measurement result $\underline{Z_x}$ is reliable.

However, it is necessary to minimize $\underline{Z_{setup}}$ value to minimize measurement error if a small $\underline{Z_x}$ is to be characterized, which corresponds to the situation when the power diode is in conduction.

In order to realize this objective, it is necessary to decrease current probes volume. According to the research results of the L2EP laboratory presented by authors in [59], current probes can be made by appropriate magnetic materials in order to reduce their volumes. Nanocrystalline is chosen for the CIP because of its relatively big permeability and NiZn ferrite is chosen for the CRP because of its small insertion impedance. It is presented in Figure 2.33(a) the realized current probes in the L2EP by those magnetic materials in comparison with the commercial ones. It can be seen that the volume can be greatly reduced, therefore $\underline{Z_{wc}}$ and $\underline{Z_p}$ can be reduced. It is to be noted that those small current probes are easier to be saturated by big currents.



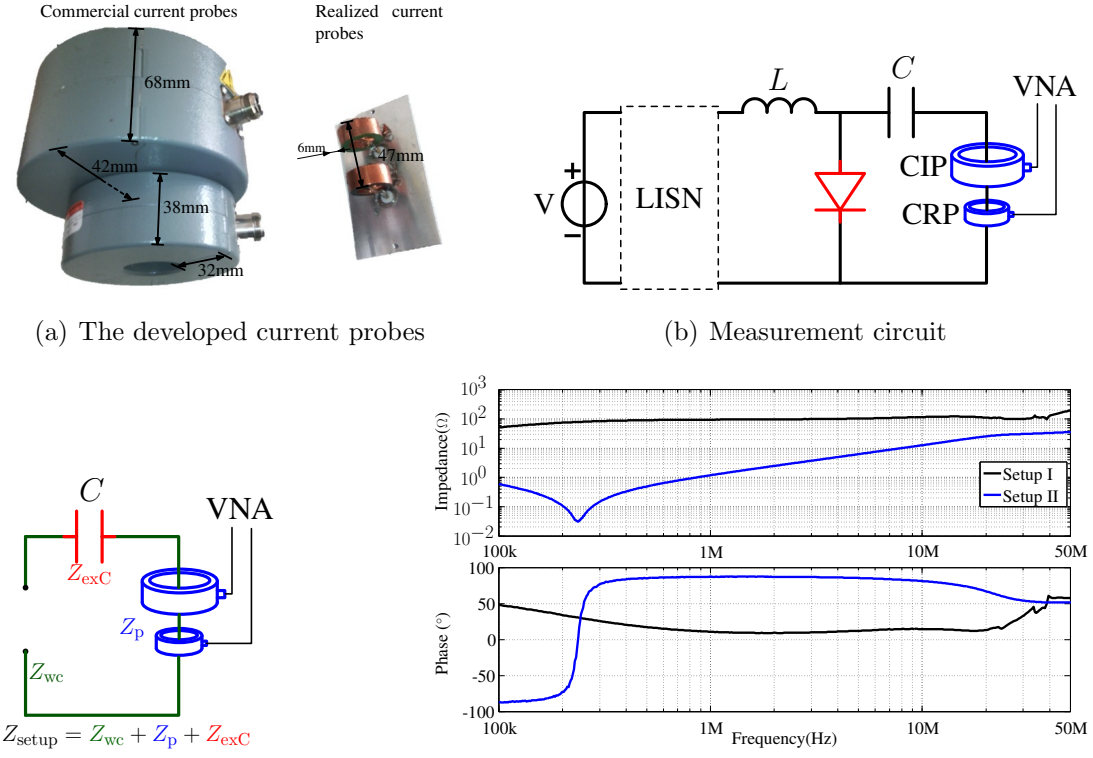
(a) Z_{setup} circuit

(b) Z_{setup} and C_j impedances

FIGURE 2.32: Two-current-probe measurement Z_{setup} circuit and value

Diode

A measurement configuration in Figure 2.33(b) is proposed to characterize diode when it is in conduction in order to avoid continuous DC current flowing through those current probes.



(a) The developed current probes

(b) Measurement circuit

(c) Z_{setup} circuit

(d) Z_{setup} evolution

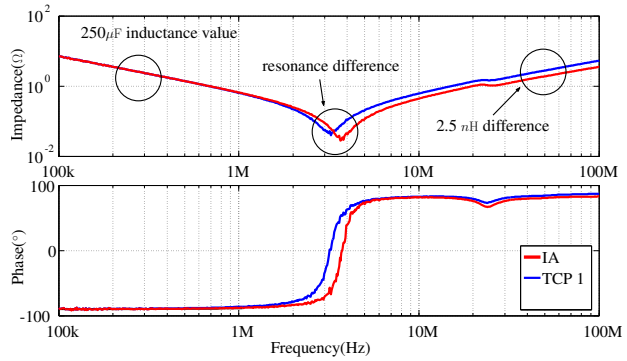
FIGURE 2.33: Measurement circuit to minimize Z_{setup} to characterize diode conduction impedance

As shown in Figure 2.33(b), an external capacitor C is used to block the DC current which flows through the current probes. Thus, $\underline{Z_{setup}}$ of this measurement configuration is shown in Figure 2.33(c), in which $\underline{Z_{setup}}$ equals to the connection wire impedance $\underline{Z_{wc}}$, the current probes insertion

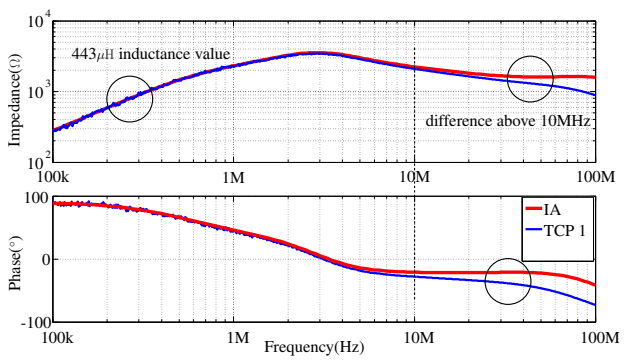
impedances $\underline{Z_{\mathrm{p}}}$ and the external capacitance impedance $\underline{Z_{\mathrm{exC}}}$[5].

It is compared in Figure 2.33(d) the $\underline{Z_{\mathrm{setup}}}$ of the setup circuit shown in Figure 2.33(c) (Setup II) and the setup circuit shown in Figure 2.32(a) (Setup I). It can be seen that the $\underline{Z_{\mathrm{setup}}}$ of the Setup II is hundredfold and thousandfold smaller than that of the Setup I from 100kHz-1MHz, and tenfold smaller until 10MHz. Therefore, $\underline{Z_{\mathrm{setup}}}$ is greatly reduced by the measurement configuration shown in Figure 2.33(b).

In order to validate the measurement results in a large frequency range, a 250nF capacitor and a 443μH inductor are measured at first with the measurement circuit shown in Figure 2.33(c). Before the measurement, a connection wire (short-circuit, 0Ω) and a 22Ω resistor are used to determine the unknown parameters $\underline{K}$ and $\underline{Z_{\mathrm{setup}}}$ in eq.(2.5). The measurement results of the capacitor and the inductor by previously presented two-current-probe method (TCP 1) are compared with that measured by IA, which are shown in Figure 2.34.



(a) 250nF capacitor



(b) 443μH inductor

FIGURE 2.34: Measurement results of the capacitor and the inductor by IA and TCP 1

As shown in Figure 2.34(a), the 250nF capacitor value is correctly measured by the TCP 1 in comparison with the IA measurement result. However, there is a difference in the capacitor equivalent series inductance (ESL) value. There is about 2.5nH more inductance value measured in IA than the TCP 1. The difference in the measured ESL is due to the choice of the precision resistors used to calibrate the measurement circuit. The impedances of the the connection wire and the 22Ω resistor are measured in IA and are shown in Figure 2.35. It can be seen that there is an about 2.5nH parasitic inductance in the connection wire. If 0Ω is used as the resistance value in equation (2.5) to calibrate the system, then a 2.5nH more value will be added in the $\underline{Z_{\mathrm{setup}}}$ value, which leads to the ESL measurement difference between the TCP 1 with the IA measurement. Therefore, in equation (2.5), instead of using simple resistor values to calibrate the system, their impedance values

[5]It is to be noted that in this configuration, the impedance of both diode and a high impedance branch constituted by L and the LISN are measured.

measured by IA are used. The measured 250nF capacitor impedance by this improved two-current-probe (TCP 2) method is shown in Figure 2.36(a), in which the measurement result is improved and corresponds well with the IA measurement until 100MHz.

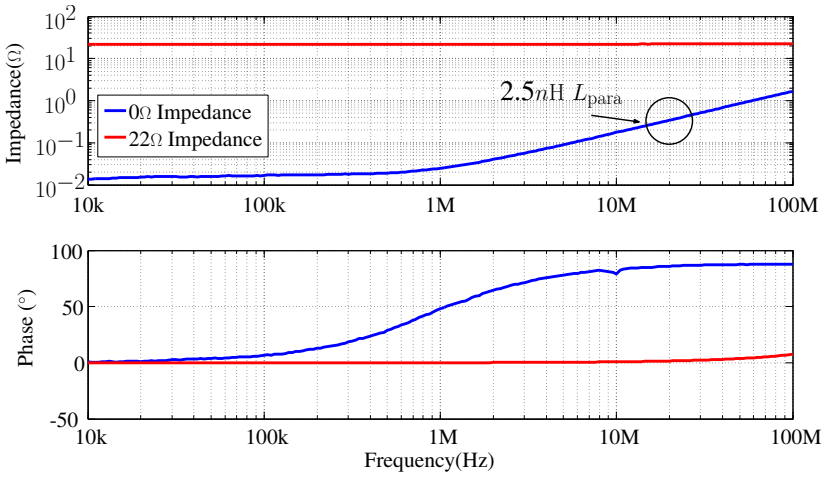
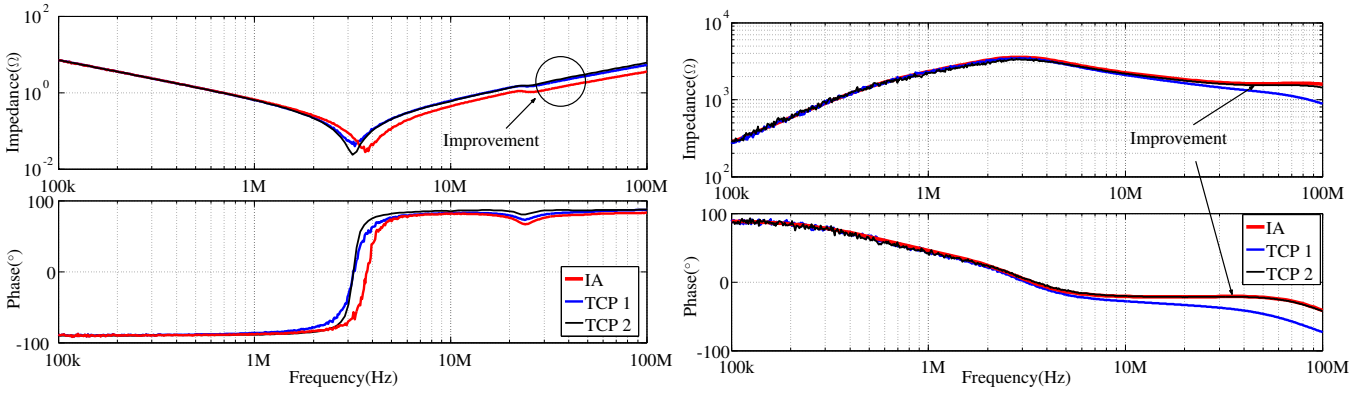


FIGURE 2.35: Measurement of the connection wire and the 22Ω resistor impedance



(a) 250nF capacitor (b) 443μH inductor

FIGURE 2.36: Measurement results of the capacitor and the inductor by IA, TCP 1 and TCP 2

It is shown in the measurement results (Figure 2.34(b)), the 443μH inductance value is correctly measured by the TCP 1 in comparison with the IA measurement result. However, there is a difference in the inductor inter-spire capacitance measurement after 10MHz. As shown in the measured phase by the TCP 1, a higher capacitance value seems to be measured than IA. Therefore, after calibrating the system by using resistor impedance values, one more measurement in open circuit is done to measure a parasitic open circuit impedance ($\underline{Z_{\mathrm{OC}}}$) in order to subtract its value in the measured inductor impedance ($\underline{Z_{\mathrm{mes}}}$). Then the true inductor impedance ($\underline{Z_{\mathrm{L}}}$) can be obtained by the following equation:

$$\frac{1}{\underline{Z_{\mathrm{L}}}} = \frac{1}{\underline{Z_{\mathrm{mes}}}} - \frac{1}{\underline{Z_{\mathrm{OC}}}}; \tag{2.24}$$

The measured 443μH inductor value after this improvement (TCP 2) is shown in Figure 2.36(b), in which the measurement result is improved and corresponds well with the IA measurement until 100MHz.

The above improvements can be applied to characterize diode impedance when it is in conduction, of which the measurement circuit is already shown in Figure 2.33(b). Therefore, the measurement steps are summarized in the following sequences:

- Determining unknown parameters:
  1. One measurement in short-circuit ($\underline{Z_{SC}}$).
  2. One measurement with a 22Ω resistor ($\underline{Z_{22\Omega}}$).
     Using $\underline{Z_{SC}}$ and $\underline{Z_{22\Omega}}$ to solve the equation (2.5) to calibrate the measurement system[6].
- Measurement:
  1. One measurement of the high impedance branch to get its impedance value $\underline{Z_H}$, which is illustrated in Figure 2.37.
  2. One measurement to get the $\underline{Z_{mes}}$ with the circuit shown in Figure 2.33(b).
     Finally, the diode conduction impedance ($\underline{Z_d}$) at each direct polarization voltage V_{AK} can be obtained by the following equation:

$$\frac{1}{\underline{Z_d}} = \frac{1}{\underline{Z_{mes}}} - \frac{1}{\underline{Z_H}}; \tag{2.25}$$

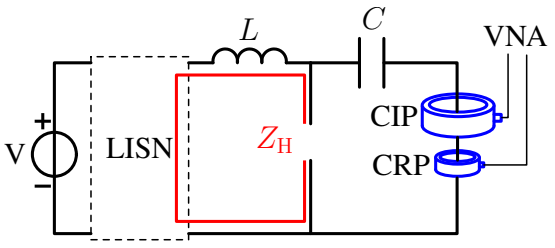


FIGURE 2.37: High impedance branch measurement circuit

It is shown in Figure 2.38 the measured diode (STTH15R06) conduction impedance results using TCP 2 and IA when $V_{AK} = 0.3V$ and $T_j = 25°C$. The diode polarization when using IA is done by IA internal DC bias power source[7]. It can be seen in Figure 2.38 that because of the decrease of the $\underline{Z_{setup}}$ value in measurement circuit (Setup II) shown in Figure 2.33(c), the measured diode

[6]The values of the resistors using to determine unknown parameters have no obvious influence on characterized results. 0Ω and 22Ω resistors are used in the measurement because unknown impedance is in the same magnitude value.

[7]The IA internal DC bias in this case is limited by the current to 100mA.

conduction impedance ($\underline{Z_{\mathrm{d}}}$) is much bigger than $\underline{Z_{\mathrm{setup}}}$ value before 10MHz. From 10MHz-50MHz, the measured $\underline{Z_{\mathrm{d}}}$ is of the same order of magnitude with $\underline{Z_{\mathrm{setup}}}$ value, therefore, the measured $\underline{Z_{\mathrm{d}}}$ value can be reliable. It is proved by comparison that the measurement result by TCP 2 corresponds well with the IA measurement, thus the measurement results can be reliable. It is to be noted that, if the measurement setup circuit (Setup I) shown in Figure 2.32(a) is used to characterize $\underline{Z_{\mathrm{d}}}$, as shown in Figure 2.38, above 1MHz, $\underline{Z_{\mathrm{d}}}$ is much smaller than $\underline{Z_{\mathrm{setup}}}$ value, of which the measurement propagation error is more likely to be yielded by the subtraction in equation (2.5).

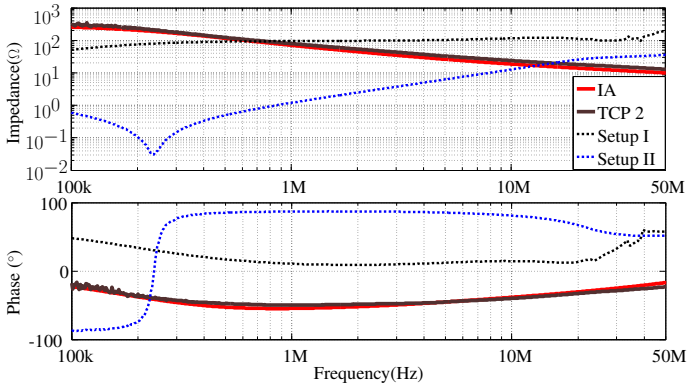


FIGURE 2.38: Diode (STTH15R06) conduction impedance measurement results ($V_{\mathrm{AK}} = 0.3V$, $T_{\mathrm{j}} = 25°C$)

It can be seen in Figure 2.38 that when the diode is in conduction, $\underline{Z_{\mathrm{d}}}$ is quite different in comparison with that when diode is blocked as shown in Figure 2.32(b). The presented multiple-current-probe method is also available to characterize power transistor impedance when it is in linear region.

Transistor

When the power transistor is in linear region, the measurement configuration to characterize C_{gd} by the three-current-probe method is shown in Figure 2.39. The developed smaller current probes are used. G and S of the power transistor is polarized positively by a battery while an extra power source V is connected between D and S. Two external 2.2μF capacitors are used to block the DC voltage between D and G, and between G and S. Thus, there is no DC current flowing through the current probes to saturate the magnetic materials. A high impedance circuit in AC is constituted by an external 43μH in series with the LISN to guarantee that all the current around megahertz injected by the CIP passes through the transistor.

In the current loop represented by the red dotted line in Figure 2.39, the injected current by CIP passes through C_{gd} and is then measured by the CRP, so C_{gd} values can be measured directly when the power device is in linear region.

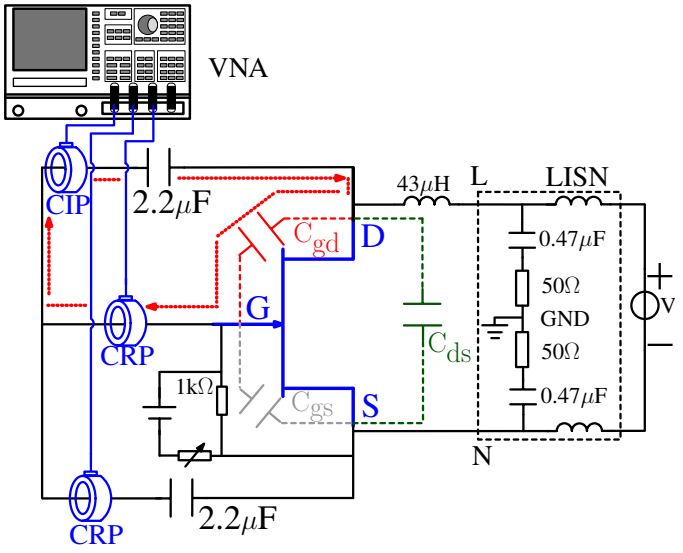


FIGURE 2.39: C_{gd} measurement configuration by three-current-probe method when power transistor is in linear region

More details on how to apply the measured diode conduction impedance to model the power device as well as how to determine and model power transistor inter-electrode capacitances when they are in linear region will be presented in Chapter 3.

2.3 Discussion

It is presented in this chapter the different methods used to characterize power devices and determine their static and dynamic characteristics. There are the following issues which are necessary to be discussed.

Static characteristics

As presented in Chapter 2.1, an active differential voltage probe (100MHz, 1000V) is used to measure power device voltage waveforms. According to the measurement results shown in Figure 2.7 and Figure 2.13, it can be seen that the diode conduction voltage V_{AK} and JFET V_{DS} when it is in ohmic region are small values less than 2V. The advantage of using an ADVP is that it isolates the ground of the oscilloscope with the measurement circuit. However, it is to be noted that the measurement noise of a 1000V ADVP used to measure small voltage values is higher. As it is an active probe, the offset to zero in the oscilloscope is necessary to measure such small voltage values. Comapred to 100MHz 1000V ADVP, a 400MHz 400V passive voltage probe (PVP) is more sensible to measure small voltage values. However, the use of the PVP brings the ground connection of the oscilloscope in the measurement circuit. In order to protect the measurement equipment, the measurement circuit shown in Figure 2.40 can be used when a PVP is used to measure V_{DS} voltage.

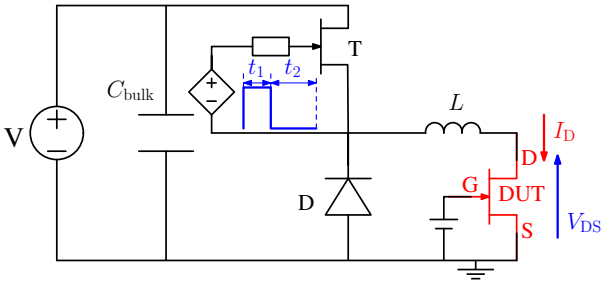
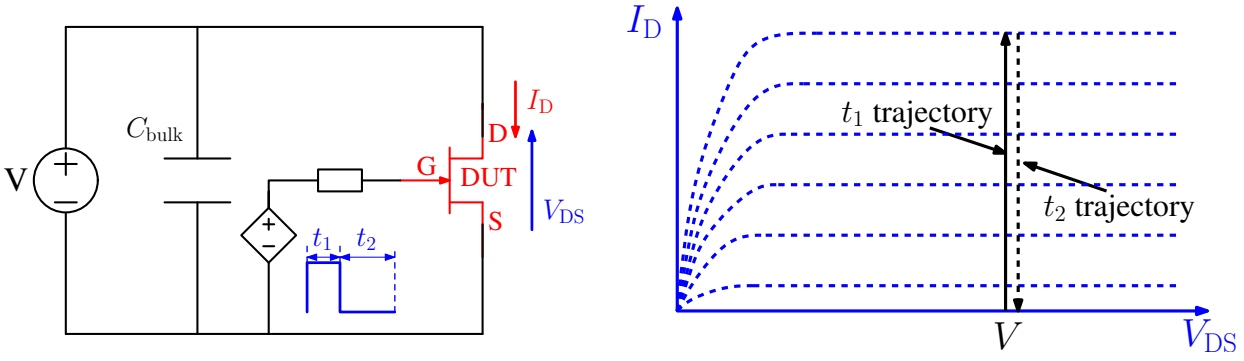


FIGURE 2.40: Measurement circuit when using a PVP

The measurement trajectory is presented in Figure 2.4 when the power transistor is characterized with the measurement circuit shown in Figure 2.1. Besides this measurement circuit, another measurement possibility to characterize power devices by single-pulse method can be illustrated with the circuit shown in Figure 2.41(a). The measurement circuit is constituted by a bulk capacitor C_{bulk}, the power device under test (DUT) and its driver circuit. The DUT is controlled directly by the single-pulse between its gate and source, thus V_{GS} is varied during the measurement from 0V to certain V_{GS} value. As V_{DS} is almost stable during the measurement [8], I_D can be measured directly. Therefore, the DUT trajectory in this characterization circuit is presented in Figure 2.41(b). The DUT transconductance can be directly characterized when the V_{DS} is chosen as a voltage in the power device linear region. By varying V_{DS} values, power device static characteristics can be obtained.



(a) measurement (b) DUT trajectory

FIGURE 2.41: Single-pulse measurement circuit II

Dynamic characteristics

It can be seen that above 300kHz, inductive behavior appears in the $\underline{Z_{setup}}$ of the Setup II as illustrated in Figure 2.33(d). The inductive value of Setup II is about 200nH and it increases the $\underline{Z_{setup}}$ value in HF. This inductance value can hardly be further decreased, because it is mainly constituted by the current probe insertion impedance, which is determined by the use of magnetic materials in the current probes. If $\underline{Z_{setup}}$ value in HF needs to be further decreased, the magnetic materials shall be avoided to use in the current probes.

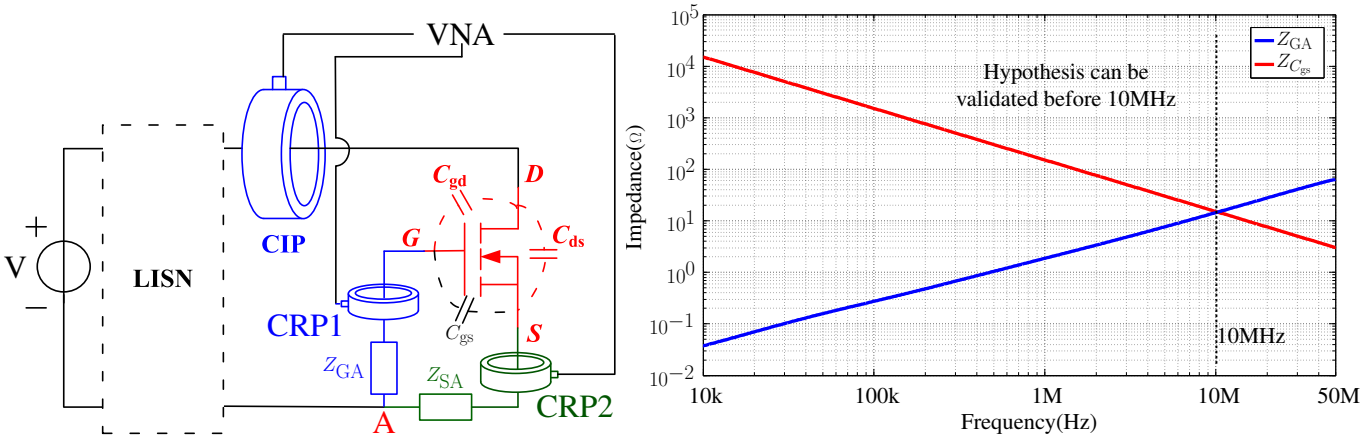
[8] The influence of the parasitic resistances of the C_{bulk} and connection wires are neglected.

For the three-current-probe measurement method, in the measurement circuit shown in Figure 2.42(a), if the injected current flowing through C_{gd} then completely flows through CRP1, and the injected current flowing through C_{ds} then completely flows through CRP2, the following hypothesis need to be verified:

$$\underline{Z_{\text{GA}}} \ll \underline{Z_{\text{SA}}} + \underline{Z_{C_{\text{gs}}}}; \tag{2.26}$$

$$\underline{Z_{\text{SA}}} \ll \underline{Z_{\text{GA}}} + \underline{Z_{C_{\text{gs}}}}. \tag{2.27}$$

where $\underline{Z_{\text{GA}}}$ represents the impedance of the connection wire between G and A together with the CRP1 insertion impedance, $\underline{Z_{\text{SA}}}$ represents the impedance of the connection wire between S and A together with the CRP2 insertion impedance and $\underline{Z_{C_{\text{gs}}}}$ represents the impedance of the C_{gs}.



(a) HF equivalent circuit

(b) $Z_{C_{\text{gs}}}$ and Z_{GA} comparison

FIGURE 2.42: Hypothesis validation on three-current-probe measurement method

Both C_{gd} and C_{ds} measurement results are reliable only when the hypothesis 2.26 and 2.27 are satisfied simultaneously, which means:

$\underline{Z_{C_{\text{gs}}}} \gg \underline{Z_{\text{GA}}}$ or $\underline{Z_{\text{SA}}}$. Both $\underline{Z_{\text{GA}}}$ and $\underline{Z_{\text{SA}}}$ are inductive impedances, which increase when frequency increases. $\underline{Z_{C_{\text{gs}}}}$ is capacitive impedance, which decreases when frequency increases. It is shown in Figure 2.42(b) the comparison of $\underline{Z_{C_{\text{gs}}}}$ value and $\underline{Z_{\text{GA}}}$ value. C_{gs} is supposed to be $1n$F and the connection between G and A is the measurement circuit shown in Figure 2.24(b), which is measured by IA. It can be seen in Figure 2.42(b) that at 10MHz, $\underline{Z_{C_{\text{gs}}}} = \underline{Z_{\text{GA}}}$. Thus, the presented three-current-probe method is validated for the measurement results until 10MHz. This frequency is higher than datasheet, of which inter-electrode capacitances are given at 1MHz.

2.4 Conclusions

It is presented in this chapter the measurement methods of the power devices static and dynamic characteristics.

The measurement of the power device static characteristics are based on a Buck converter which is controlled by a single-pulse method. The duration of the pulse is chosen to be $50\mu s$. The presented method is applied to characterize a SiC diode and a SiC JFET. The static characteristics at different junction temperatures T_j is presented. T_j is calculated during the characterization, which shows that the choice of the power duration makes that T_j has almost no influence on measurement results. The maximal power dissipation of the SiC JFET in the characterization is about 1700W and SiC JFET static characteristics with T_j varying from 25°C to 120°C are measured. Voltage-dependent inter-electrode capacitances of power semiconductor devices in high voltage are measured by multiple-current-probe (MCP) method. Using a simple setup, the proposed method provides the advantage of isolating the measurement equipments from the DC bias power source. By applying a two-current-probe method in the measurement, the results of C_iss and C_oss of a transistor are accurate, but the result of C_rss is not convincing, because of indirect calculation inducing measurement errors propagation. To overcome this inconvenient, a three-current-probe method is proposed to directly measure C_rss. Experimental results have been obtained on several power devices of different technologies (Si MOSFET and IGBT, SiC JFET, GaN HEMT) and confirm that this method offers a precise characterization of their inter-electrode capacitances in high voltage. A solution to increase the measurement sensibility is presented. It is shown that the MCP method is able to characterize power devices a-few-picofarad inter-electrode capacitances. By increasing the measurement sensibility, the MCP method can be applied not only to characterize power devices when they are blocked, but also when they are in conduction, in which a special measurement configuration is proposed with developed smaller current probes.

Power devices characterization results based on the above presented methods will be applied to fabricate their models, which will be presented in Chapter 3.

Chapter 3

Power Devices Modeling

In this chapter, characterization results based on the measurement methods presented in Chapter 2 will be applied for power devices modeling. Simulations are carried out in PSPICE software.

First, a power diode behavior model is built using its dynamic impedance measurement results. The presented modeling method is applied for two Si power diodes with different reverse recovery charges[1].

Then, a "normally-off" SiC JFET behavior model is presented. Its static characteristic is represented by the drain current (I_D) evolution with drain source voltage (V_{DS}) and gate source voltage (V_{GS}), which is based on the measurement results. Its dynamic characteristic is represented by its inter-electrode capacitances evolution, and it is based on the measurement results when the power device is blocked and in linear region.

At last, several issues concerning on the power device modeling will be discussed and a brief conclusion will be presented.

3.1 Diode Modeling

In this section, a power diode spice physical model is first analyzed by characterizing its dynamic impedance in PSPICE. Then two Si power diodes (STTH15R06 and MUR880E) are characterized and modeled.

[1]The Si diodes are chosen here to be modeled in order to simulate their reverse recovery behavior. The same modeling method can be applied to SiC diode, which is easier to be modeled than Si diode because the reverse recovery behavior can be neglected.

3.1.1 Diode spice model characterization and modeling

A power diode (STTH15R06) spice model is first analyzed in this section. It is a physical model with the parameters given by constructors. The model is based on physical equations in PSPICE. Therefore, it is like a black box, because several equations and parameters to model this power device are unknown to the users. It is characterized with the simulation circuit shown in Figure 3.1.

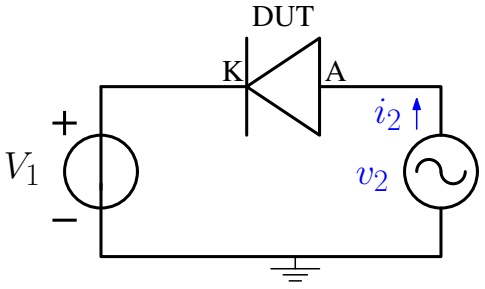


FIGURE 3.1: Simulation circuit in PSPICE to characterize a diode spice model

V_1 is a DC voltage which can polarize the diode either positively or negatively at a DC point. v_2 is a small signal AC voltage. In the simulation, it is set to be $1m$V. Therefore, the dynamic impedance of the diode Z_{dd} can be gotten in the following equation:

$$\underline{Z_{\mathrm{dd}}} = \frac{\underline{V_2}}{\underline{I_2}} \tag{3.1}$$

By using AC sweep in PSPICE, Z_{dd} values at different frequencies can be obtained.

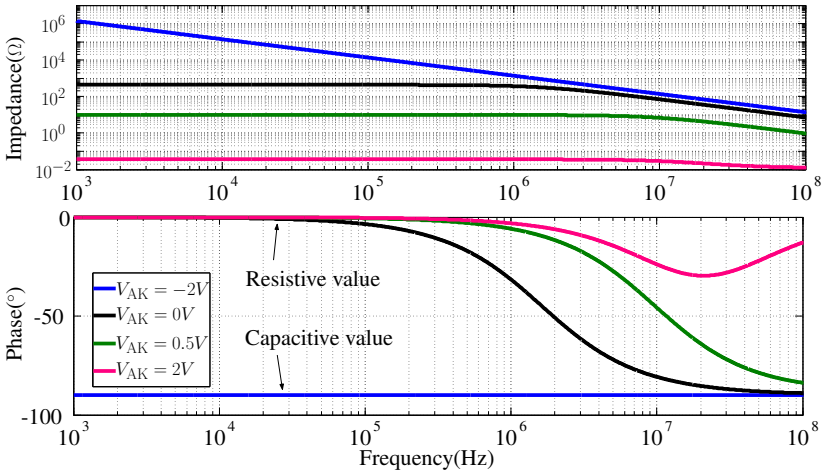
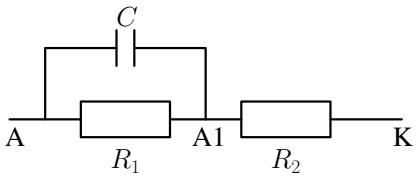


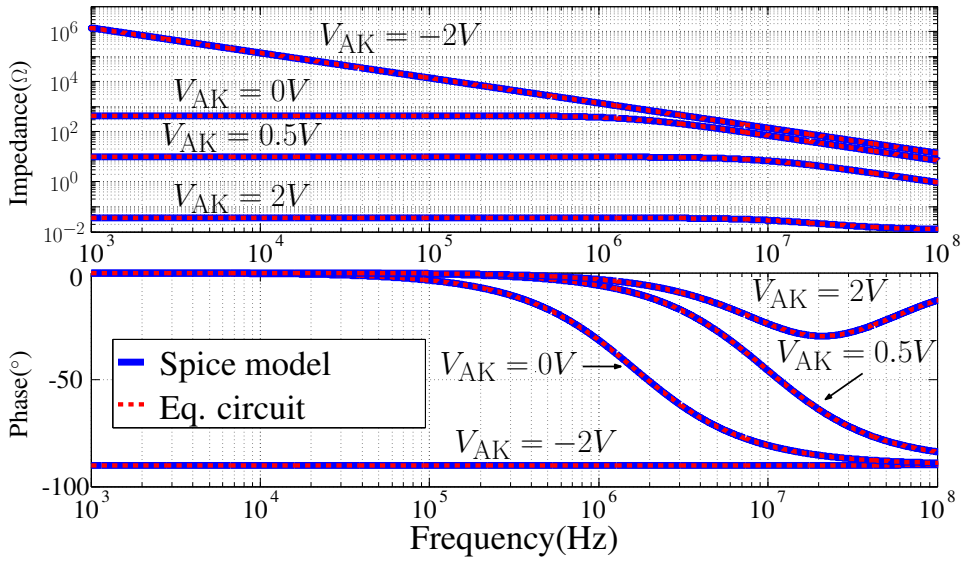
FIGURE 3.2: Characterization results of a spice diode model at different V_{AK} voltages

The characterization results are shown in Figure 3.2 when the diode is polarized from a negative bias voltage (V_1 in Figure 3.1) to a positive bias voltage (-V_1 in Figure 3.1). It can be seen that the measured diode impedance changes with the polarization voltage. As expected, when the diode is negatively polarized, junction capacitance value is mainly obtained and when the diode conducts the current, on-state dynamic resistance value is mainly measured.

An equivalent circuit shown in Figure 3.3(a) can be used to model the "measured" diode impedance. The values of C, R_1 and R_2 can be obtained according to the curve fitting method in MATLAB optimization tool. The impedance and phase comparison between the characterization results and the above equivalent circuit is shown in Figure 3.3(b). It is shown that the equivalent circuit of Figure 3.3(a) represents well the characterization results. The evolution of C, R_1 and R_2 with V_{AK} is thus presented in Figure 3.4. It can be seen that the fitted R_2 value in the equivalent circuit is almost constant. When the diode is negatively polarized, R_1 is a big value and C is around a hundred pF and when the diode is positively polarized, R_1 decreases sharply to a small value almost in the same magnitude with R_2, while C increases dramatically to several hundreds nF.



(a) Diode equivalent Circuit



(b) Impedance and phase comparison of different V_{AK} voltages

FIGURE 3.3: Equivalent circuit and comparison with the spice model

A diode behavior model with the equivalent circuit shown in Figure 3.3(a) is thus compared with the spice model in commutation. It is to be noted that the values of R_1 and R_2 in Figure 3.4 are obtained by small-signal characterization, therefore, they represent the dynamic values of each resistance when the power diode is polarized at a DC point. Their static values are necessary for the simulation to represent power device static characteristics. As R_2 is constant, its dynamic value equals to its static value. R_1 static value (R_{1s}) can be obtained by the following method. At first, the static characteristic of the diode spice model is obtained by the simulation with DC sweep and it is shown in Figure 3.5. With the equivalent circuit shown in Figure 3.3(a), the static values of

R_1 and R_2 together represent the diode static characteristics. $V_{\mathrm{A1K}} = I_{\mathrm{D}} R_2$ is then represented in Figure 3.5. For the same current I_{D}, $V_{\mathrm{AA1}} = V_{\mathrm{AK}} - V_{\mathrm{A1K}}$, therefore, $R_{1\mathrm{s}} = \frac{V_{\mathrm{AA1}}}{I_{\mathrm{D}}}$.

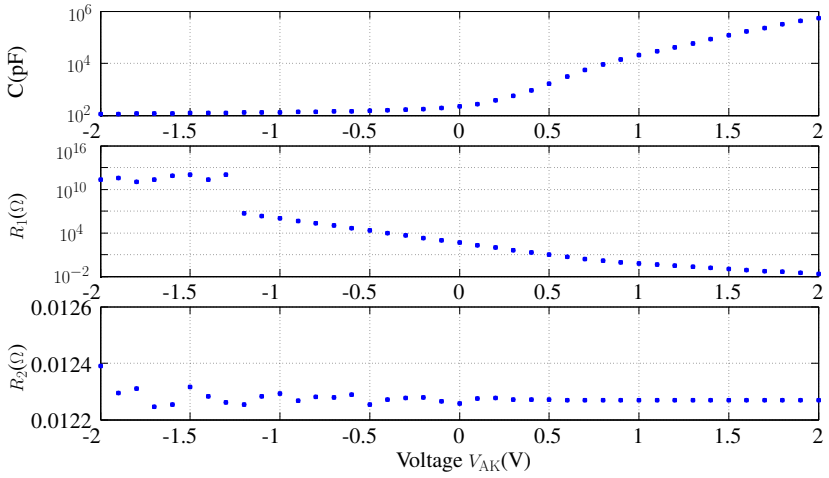


FIGURE 3.4: C, R_1 and R_2 evolution

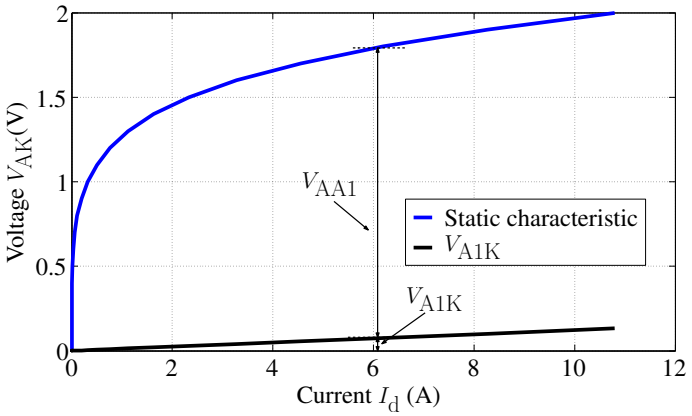


FIGURE 3.5: Diode static characteristic with $V_{\mathrm{A1K}} = R_2 I_{\mathrm{d}}$ and $V_{\mathrm{AA1}} = V_{\mathrm{AK}} - V_{\mathrm{A1K}}$

According to the results shown in Figure 3.4 and Figure 3.5, both C and $R_{1\mathrm{s}}$ change their values when V_{AK} changes, the non-linearity of the two elements can be represented by two voltage-controlled current sources in PSPICE. Therefore, $R_{1\mathrm{s}}$ can be represented by $I_{\mathrm{R1}} = \frac{V_{\mathrm{AA1}}}{R_{1\mathrm{s}}}$ and C can be represented by $I_{\mathrm{C}} = C\frac{\mathrm{d}V_{\mathrm{AA1}}}{\mathrm{d}t}$, and the derivation can be expressed by the DDT function in PSPICE. However, the question remains that C and $R_{1\mathrm{s}}$ are dependent on which parameter? It is illustrated in Figure 3.6 the current direction during the diode reverse recovery. The capacitor which stores the charge during diode conduction begins to discharge by the sum of the current I_{c} and I_{d}. As long as the discharge process is not finished, voltage V_{AA1} remains positive (the diode was initially forward biased) as indicated in Figure 3.6. The discharge current I_{D} flows reversely through the diode, and at certain moment, diode voltage $V_{\mathrm{AK}} = V_{\mathrm{AA1}} - V_{\mathrm{KA1}}$ becomes negative. Thus, it is with more physical signification that both C and $R_{1\mathrm{s}}$ are dependent on voltage V_{AA1}. For this reason, they are chosen to be dependent on the voltage V_{AA1} in the model.

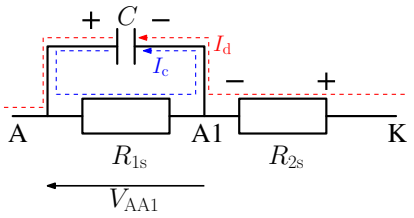


FIGURE 3.6: Current direction when diode is in reverse conduction

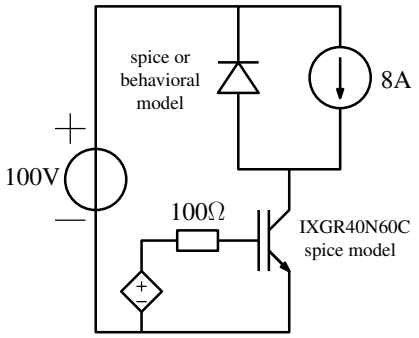
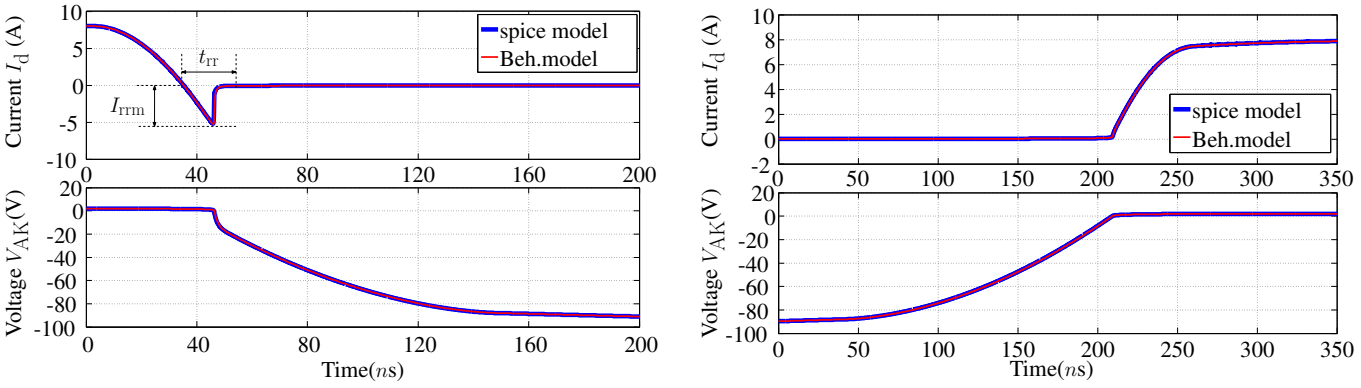


FIGURE 3.7: Commutation mesh in simulation

The diode spice model and the presented behavior model based on equivalent circuit represented in Figure 3.3(a) are simulated in a commutation mesh shown in Figure 3.7 to compare the diode switching waveforms. The results are compared in Figure 3.8 for both turn-off and turn-on. It can be seen that the presented behavior model is similar to the spice diode model on $\frac{\mathrm{d}I}{\mathrm{d}t}$, $\frac{\mathrm{d}V}{\mathrm{d}t}$, maximal reverse recovery current I_{rrm} and reverse recovery time t_{rr}. Thus it can be said that the behavior model can reproduce almost the same switching waveforms of a diode spice model. With this behavior model, the diode stored charge, the diode switching power loss can be calculated easily, which is very important for the power converter design.



(a) Turn-off

(b) Turn-on

FIGURE 3.8: Diode (STTH15R06) switching waveforms comparison between spice model and behavioral model

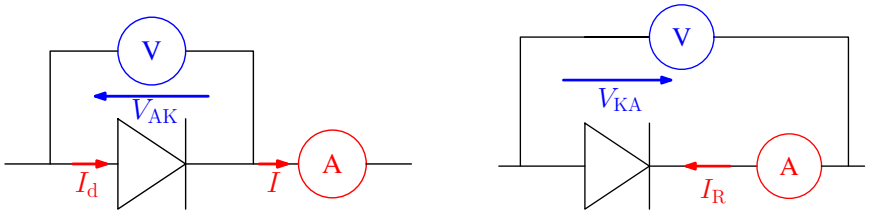
Can a real diode, regarding as a black box, be modeled in the same way? To answer this question, the diode dynamic impedance characterization results will be first represented in the next section.

3.1.2 Diode dynamic impedance characterization

As most SiC diodes are schottky type, there are almost no excess charge stored in the diodes, thus there is almost no reverse recovery phenomena. For this reason, a Si power diode (STTH15R06, 600V/8A) is first characterized in this section, in order to verify whether the presented diode behavior model can represent the diode reverse recovery phenomena.

3.1.2.1 Characterization results

To have more measurement precision than the single-pulse method presented in Chapter 2.1, the diode static characteristic when it is in conduction is measured by the circuit shown in Figure 3.9(a), and T_j is maintained constant according to the equation shown in eq.(1.1). The current is measured by an amperemeter with the minimal measured current 1μA and the voltage is measured by a voltmeter with the minimal measured current 1μ V. The internal resistance of the voltmeter used in the measurement R_V is about $77k\Omega$. The real diode conduction current I_D can be obtained by $I_D = I - \frac{V_{AK}}{R_V}$. When the diode is blocked, its leakage current I_R is measured with the circuit shown in Figure 3.9(b). However, I_R of the diode is much smaller than the minimal amperemeter measurement value, so I_R can not be measured.



(a) ON-state (b) OFF-state

FIGURE 3.9: Diode static characteristic measurement at ON and OFF states

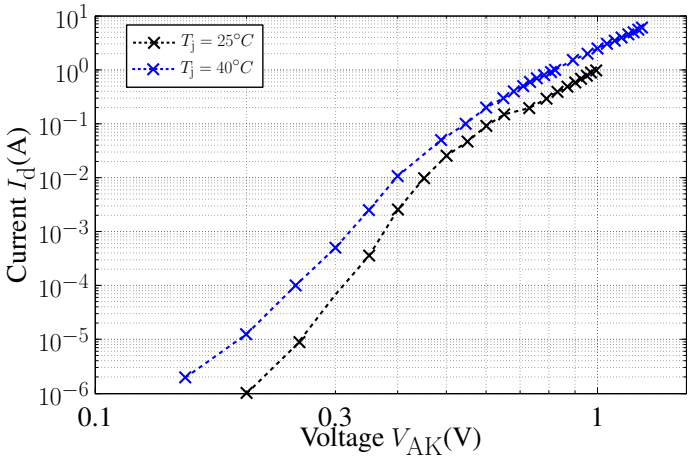


FIGURE 3.10: Si diode (STTH15R06) static characteristics at different T_j

The measured diode static characteristic is shown in Figure 3.10 when $T_j = 25°C$ and $T_j = 40°C$. It can be seen that when diode conducts 0.1A current, V_{AK} is about 0.6V when $T_j = 25°C$ and V_{AK} is

about 0.5V when $T_j = 40°C$. The static characteristics show that the temperature coefficient of the diode is positive.

When diode is blocked, its impedance can be characterized with two-current-probe method as shown in Figure 2.19(a). When diode conducts current, its impedance can be characterized with the circuit shown in Figure 2.33(b). The measurement process is presented in Chapter 2.2.3.2. The obtained results are shown in Figure 3.11 when T_j is $40°C$. When the diode is slightly positively biased, the measured impedance values are much bigger or are in the same magnitude as the Z_{setup}, thus the obtained results can be reliable. When the diode begins to conduct current, the measured impedance is almost in the same magnitude as Z_{setup} and when the diode is fully conducted ($V_{AK} = 1.22V$, $I_D = 6A$), the dynamic impedance value is small, so the measured impedance is about one tenth of the Z_{setup}.

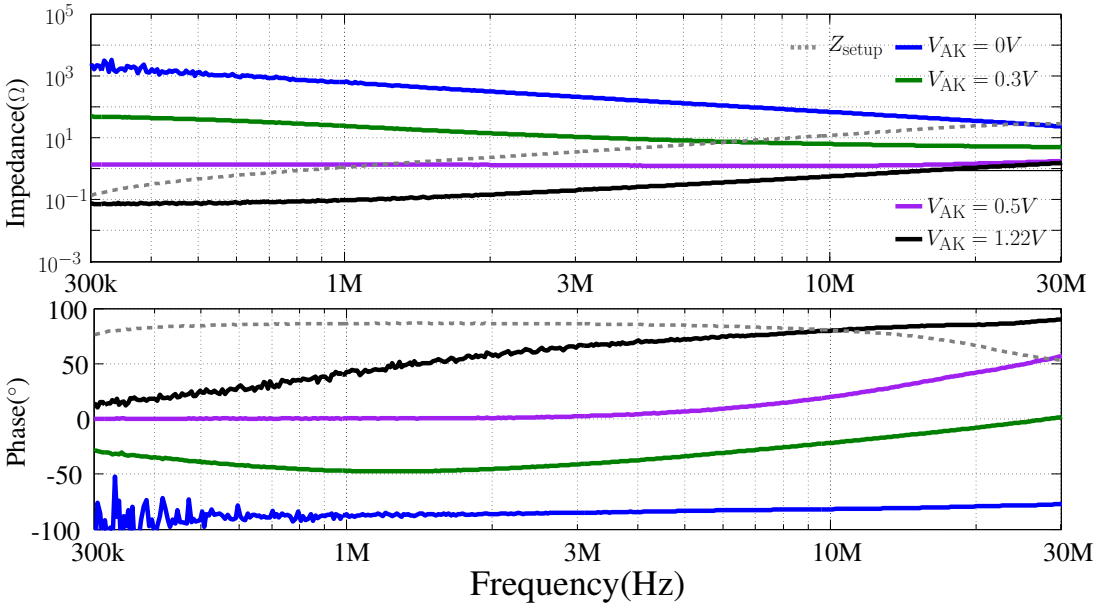


FIGURE 3.11: Diode impedance characterization results at different V_{AK} voltages ($T_j = 40°C$)

It is also shown in Figure 3.11 that when diode is fully conducting, the measured phase is positive, which is quite different of the results from a diode spice model shown in Figure 3.2. The measured inductive part in Figure 3.11 is mainly due to the parasitic inductor L_{para} of the diode packaging, which is illustrated in Figure 3.12. At low frequency (LF), the value of R_1, R_2 and L_{para} are characterized; and at high frequency (HF), C, R_2 and L_{para} are characterized. However, the impedance of L_{para} in HF is much bigger than that of the C, so it is mainly inductive in the measured phase when the diode is fully conducted.

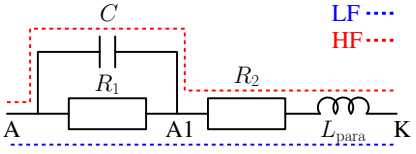


FIGURE 3.12: Small-signal equivalent circuit including L_{para} inside the diode packaging

An equivalent circuit shown in Figure 3.12 can be used to represent the measured impedance, and the value of C, R_1, R_2 and L_{para} can be obtained by fitting method. The comparison between the measured impedance and the equivalent circuit at different V_{AK} values is shown in Figure 3.13.

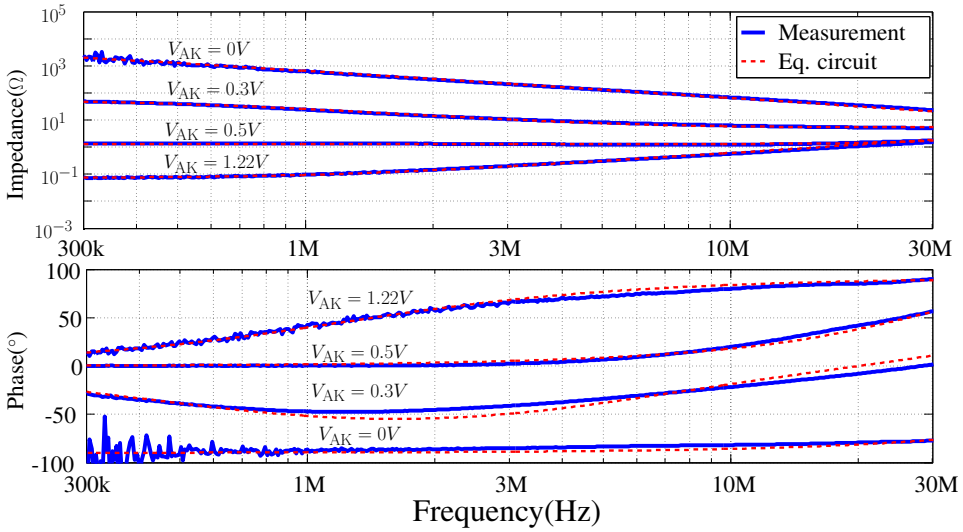


FIGURE 3.13: Comparison between the diode impedance measurement results and the model at different V_{AK} voltages ($T_{\text{j}} = 40°C$)

It can be seen in Figure 3.13 that the equivalent circuit of Figure 3.12 represents well the measurement results. The obtained L_{para} values by the fitting method at different V_{AK} voltages are shown in Figure 3.14. It is shown that when $V_{\text{AK}} \geq 0.3V$, L_{para} is almost a constant value that equals to about $10n$H. However, when $V_{\text{AK}} \leq 0.3V$, the obtained L_{para} is very small. According to the measurement results shown in Figure 3.11, when $V_{\text{AK}} \leq 0.3V$, C is mainly characterized and its impedance is much bigger than that of L_{para}, therefore the value of L_{para} does not influence the difference between the measurement and the equivalent circuit shown in Figure 3.12. Thus a constant value $10n$H can be chosen for L_{para} in Figure 3.12.

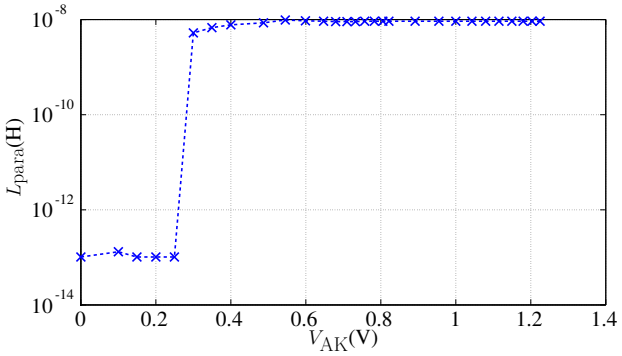
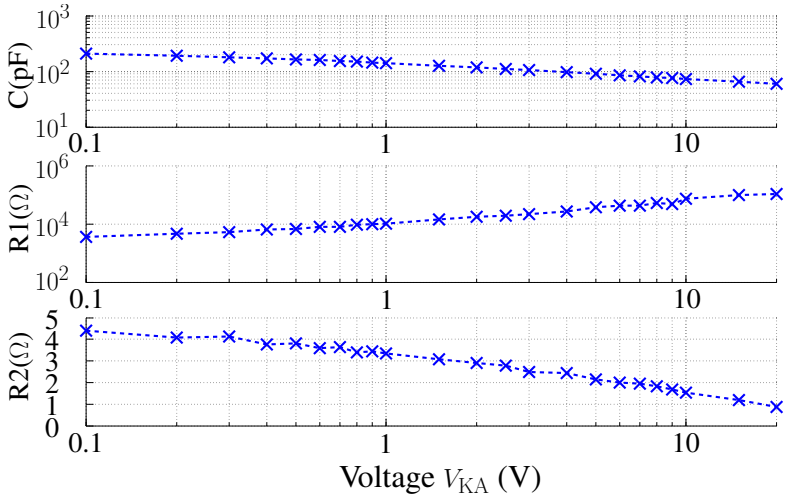
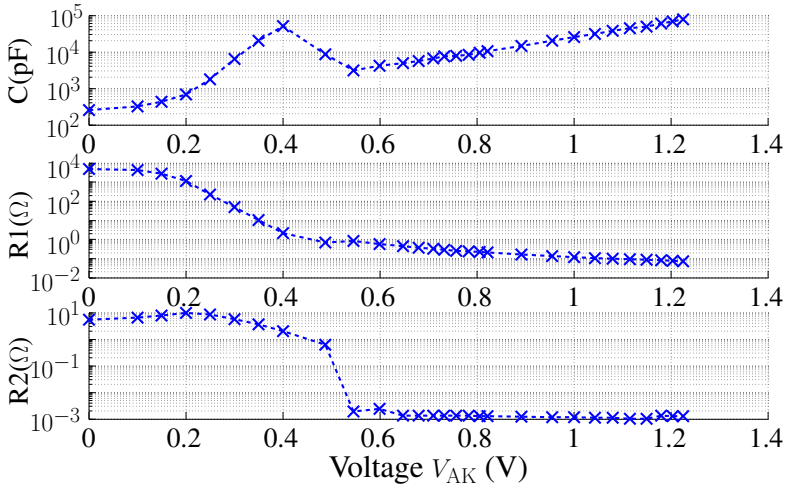


FIGURE 3.14: Obtained L_{para} values for different V_{AK} voltages in the equivalent circuit

The evolution of C, R_1, R_2 at different V_{AK} voltages are shown in Figure 3.15 when the diode is blocked and when it is conducting. It is shown that when the diode is blocked, C is around a hundred pF and R_1 remains a big value about several dozens of thousands ohms. Those results are similar to that of a diode spice model presented in Figure 3.4.



(a) Diode blocked



(b) Diode conducting

FIGURE 3.15: C, R_1, R_2 evolution ($T_j = 40°C$)

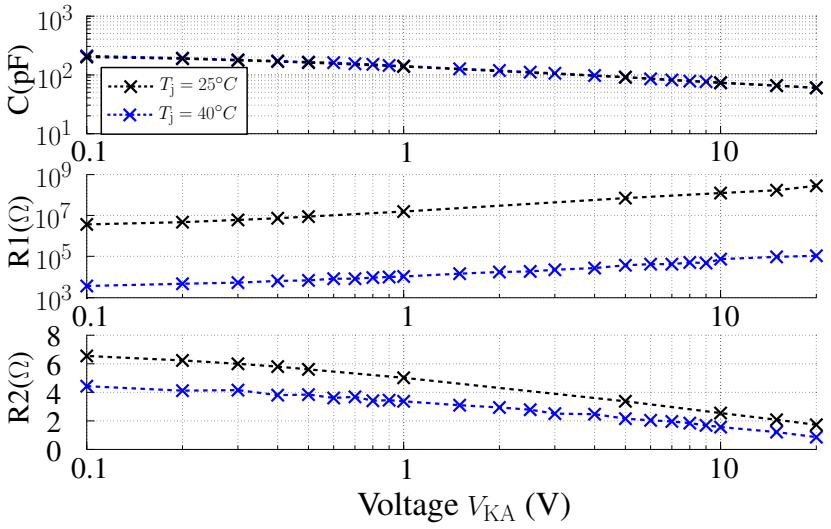
However, it is shown in Figure 3.4 that R_2 is almost constant when diode is blocked, but it is much bigger in the measurement than in its spice model and it decreases when diode negative bias voltage V_{KA} increases.

It is shown in Figure 3.15(b) the C, R_1 and R_2 evolution when diode is in conduction. The obtained values of R_1 is similar to that of a spice model shown in Figure 3.4. R_1 decreases when diode positive bias voltage V_{AK} increases. The obtained values of R_2 slightly increases at first when V_{AK} increases to $0.2V$ and then it deceases when V_{AK} increases. The variable evolution of R_2 with V_{AK} is not reproduced by a spice model. The obtained values of C increases at first when V_{AK} increases to $0.4V$, which is in the same trend as shown by a spice model. Then there is a discontinuity in the obtained values when V_{AK} increases. The reason of this discontinuity is similar to that explained in Figure 3.14 for the obtained L_{para} values. As what is shown in Figure 3.11, when diode begins to conduct the current, R_1 decreases dramatically, thus inductive impedance is mainly characterized in HF. The obtained values of C hardly influences the difference between the measurement and the

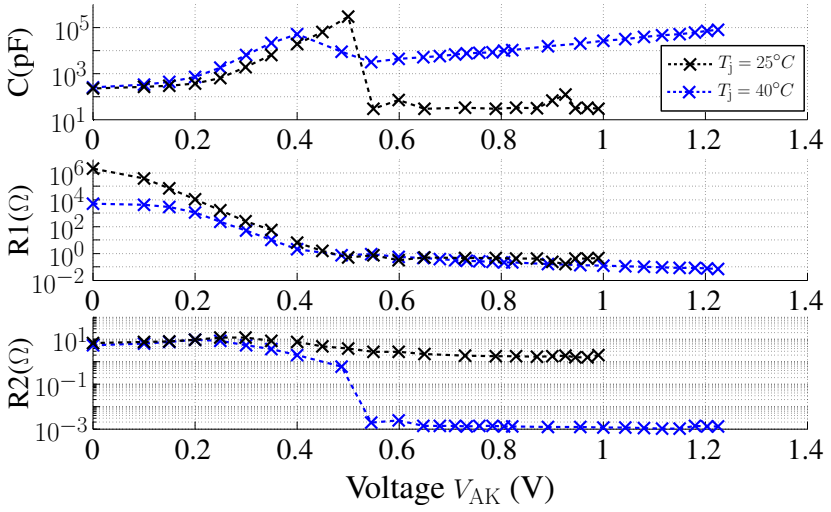
equivalent circuit shown in Figure 3.12. Therefore, the true C values when diode in conduction can not be correctly determined by the fitting method. There is also a discontinuity in the obtained R_2 values when V_{AK} is about 0.5V. This is due to the same reason, as C can not be correctly characterized, only the sum of the R_1 and R_2 is obtained by fitting method. Thus, the obtained R_2 values when $V_{\mathrm{AK}} \geq 0.5V$ is not reliable.

3.1.2.2 Comparison on different junction temperatures

It is shown in Figure 3.16 the comparison of the obtained C, R_1 and R_2 values when $T_{\mathrm{j}} = 25°\mathrm{C}$ and $40°\mathrm{C}$ based on the same equivalent circuit model shown in Figure 3.12.



(a) Diode blocked



(b) Diode conducting

FIGURE 3.16: Diode model parameters C, R_1, R_2 evolution at different T_{j}

It is shown that when the diode is blocked, T_{j} does not influence the obtained C values. However, the obtained R_1 and R_2 values increase at the same V_{KA} voltage when T_{j} increases. It is to be noted that the evolution of all the above three values with voltage V_{AK} is presented in Figure 3.16(b) when

diode is in ON-state, however, as presented previously, their evolution with voltage V_{AA1} is more appropriate, which will be presented in the next chapter.

It is illustrated in Figure 3.17 that the slope of the tangent of the diode static characteristic at one voltage equals to $\frac{1}{R_1+R_2}$. For this diode, at the same negative bias voltage V_{KA}, the leakage current decreases when T_j decreases, which makes sense that $\frac{1}{R_1+R_2}$ when $T_j = 40°C$ is smaller than that when $T_j = 25°C$. Thus, the obtained R_1 and R_2 increases with T_j, which is shown in both case when diode is blocked (Figure 3.16(a)) and in conduction (Figure 3.16(b)). It is also shown in Figure 3.16(b) that at $T_j = 25°C$, when the diode begins to conduct the current, the values of C can be hardly characterized.

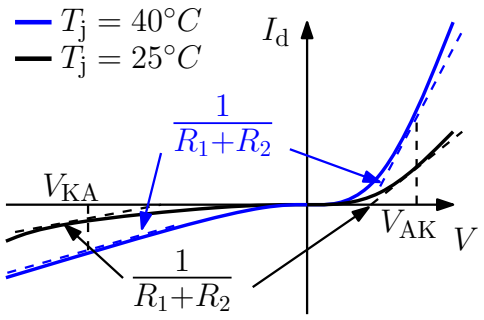
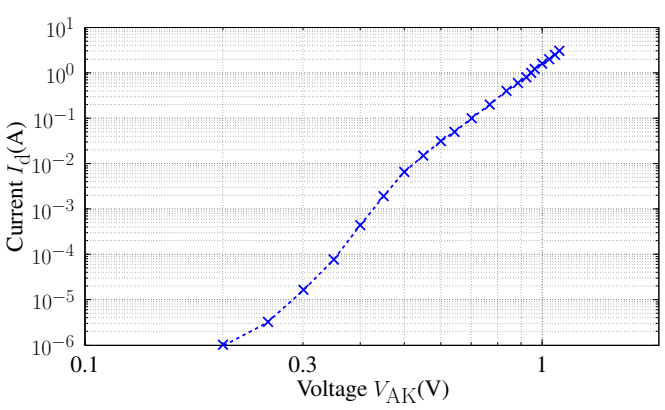
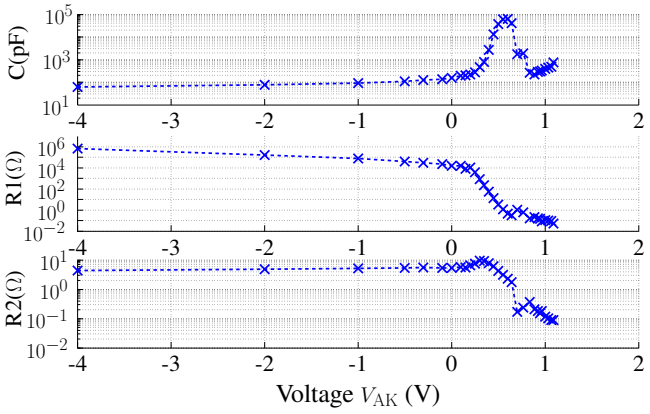


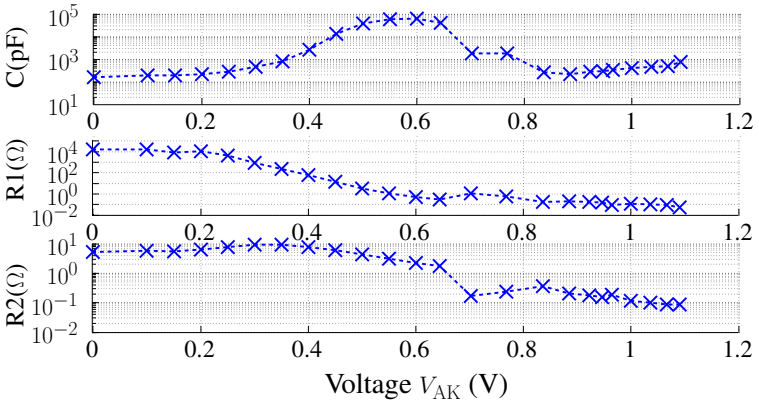
FIGURE 3.17: Dynamic resistance evolution with T_j



(a) Static characteristic



(b) Parameters evolution



(c) Zoom of parameters evolution when diode is in conduction

FIGURE 3.18: Static characteristic and C, R_1, R_2 evolution of the diode MUR880E ($T_j = 40°C$)

The proposed method is then applied to characterize another Si power diode (MUR880E), the reverse recovery charge of which is bigger than that of the diode STTH15R06 through its technical datasheet. The measured diode conducted static characteristic is shown in Figure 3.18(a) when $T_j = 40°C$. The obtained C, R_1, R_2 evolution based on the same equivalent circuit shown in Figure 3.12 and at the same T_j are shown in Figure 3.18(c) and the obtained L_{para} is 5.5nH. It is shown in Figure 3.18(c) that C, R_1, R_2 evolution is similar to that of the STTH15R06. When the diode starts to conduct more that 0.1A, C is not correctly characterized because of the influence of L_{para}. Thus, only the sum of R_1 and R_2 values are obtained like the previous case.

In the next section, the obtained C, R_1, R_2 values are to be used to model the diode.

3.1.3 Diode modeling

It is presented in Chapter 3.1.1 that the obtained R_1 values are dynamic resistances values and they need to be converted into static resistance values. Unlike a diode spice model in which R_2 is almost constant, the R_2 in the measurement is in non-linear change with V_{AK} voltage. Therefore, the method presented in Chapter 3.1.1 to get R_{1s} is not suitable for the measurement results.

The following method is used to obtain R_{1s} and R_{2s} values. The diode static characteristic can be represented in Figure 3.19 by two static resistances R_{1s} and R_{2s}, both C and L_{para} are omitted. Based on Figure 3.19, following equations can be obtained:

$$\begin{aligned} I_d \cdot R_{1s} &= V_1 \\ I_d \cdot R_{2s} &= V_2 \\ V_{AK} &= V_1 + V_2 \end{aligned} \tag{3.2}$$

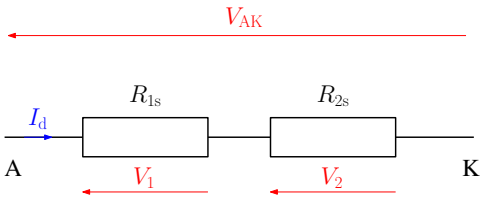


FIGURE 3.19: Diode static characteristic represented by two static resistances

The derivation of the eq.(3.2) can be obtained in the following equations:

$$\begin{aligned} R'_{1s} = R_1 &= \frac{dv_1}{dI_D} \\ R'_{2s} = R_2 &= \frac{dv_2}{dI_D} \\ dv_{AK} &= dv_1 + dv_2 \end{aligned} \tag{3.3}$$

Eq.(3.3) can be further simplified into:

$$\mathrm{d}v_{\mathrm{AK}} = \mathrm{d}v_1 + \frac{R_2}{R_1}\mathrm{d}v_1 \tag{3.4}$$

$$\mathrm{d}v_1 = \frac{1}{1+\frac{R_2}{R_1}}\mathrm{d}v_{\mathrm{AK}} \tag{3.5}$$

Therefore, at one voltage V_{AK}, V_1 can be obtained by integrating eq.(3.5):

$$\int_0^{V_1} \mathrm{d}v_1 = \int_0^{V_{\mathrm{AK}}} \frac{1}{1+\frac{R_2}{R_1}}\mathrm{d}v_{\mathrm{AK}} \tag{3.6}$$

Once V_1 is obtained, $R_{1\mathrm{s}}$ and $R_{2\mathrm{s}}$ can be obtained by:

$$\begin{aligned} R_{1\mathrm{s}} &= \frac{V_1}{I_{\mathrm{d}}} \\ R_{2\mathrm{s}} &= \frac{V_{\mathrm{AK}} - V_1}{I_{\mathrm{d}}} \end{aligned} \tag{3.7}$$

As shown in Figure 3.15(b), when diode conducts the current, because of the existence of L_{para}, the C can not be well characterized, which means that C can be neglected in the equivalent circuit shown in Figure 3.12. Therefore, only the sum of the obtained R_1 and R_2 values can be correctly obtained by the fitting method, so the repartition of R_1 and R_2 values can not be correctly expressed in such a case. For this reason, the R_1 real values $R_{1,\mathrm{real}}$ and R_2 real values $R_{2,\mathrm{real}}$ can be represented in the following equation:

$$\begin{aligned} R_{1,\mathrm{real}} &= \alpha \cdot (R_1 + R_2) \\ R_{2,\mathrm{real}} &= (1-\alpha) \cdot (R_1 + R_2) \end{aligned} \tag{3.8}$$

where α is a factor to determine the $R_{1,\mathrm{real}}$ and $R_{2,\mathrm{real}}$ repartition values.

It is shown in Figure 3.20 the comparison of R_1 and R_2 with $R_{1,\mathrm{real}}$ and $R_{2,\mathrm{real}}$ respectively in the assumption that α is 0.5. It can be seen that there is no discontinuity in $R_{1,\mathrm{real}}$ and $R_{2,\mathrm{real}}$ values, which brings more physical meaning in the obtained $R_{1,\mathrm{real}}$ and $R_{2,\mathrm{real}}$ values than original R_1 and R_2 values. Thus, the actual repartition between $R_{1,\mathrm{real}}$ and $R_{2,\mathrm{real}}$ is yet to be determined.

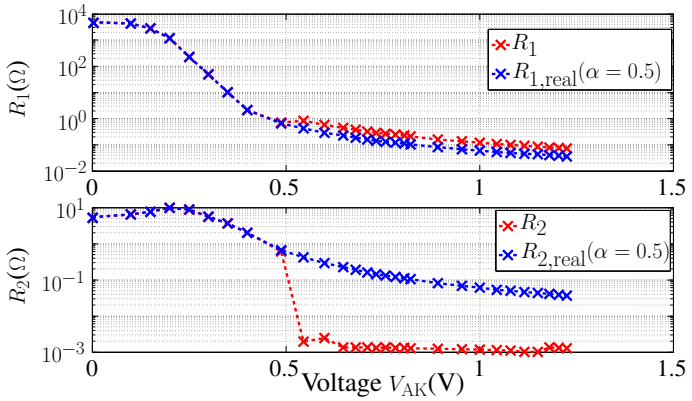


FIGURE 3.20: Comparison of R_1 and R_2 with $R_{1,\text{real}}$ and $R_{2,\text{real}}$ when $T_j = 40°C$ ($\alpha = 0.5$)

For resolving eq.(3.6) to get V_1 values, the following method can be used:

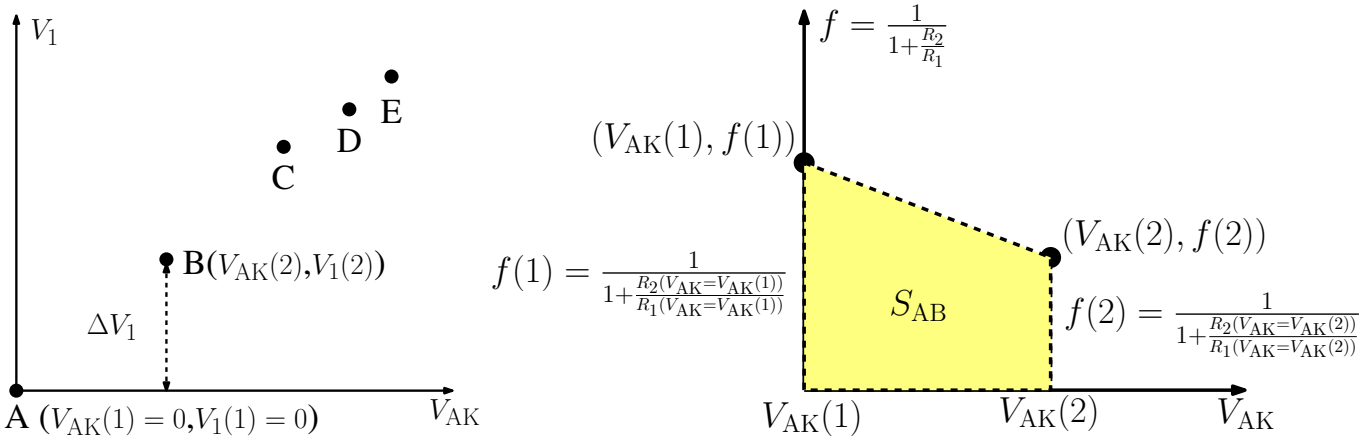
1. The first point corresponds to the point A ($V_{\text{AK}}(1)$,$V_1(1)$) in Figure 3.21(a), in which case $V_{\text{AK}}(1) = 0$, $V_1(1) = 0$ and $R_1 = R_{1s}$, $R_2 = R_{2s}$, because static and dynamic resistances are the same at zero voltage.

2. The second point corresponds to the point B ($V_{\text{AK}}(2)$,$V_1(2)$) in Figure 3.21(a), in which case ΔV_1 equals to the surface S_{AB} in Figure 3.21(b) according to eq.(3.6). S_{AB} can be approximately calculated by the following equation:

$$S_{\text{AB}} = \left(\frac{f(1) + f(2)}{2} \right) \cdot \Delta V_{\text{AK}}, \tag{3.9}$$

   where $\Delta V_{\text{AK}} = V_{\text{AK}}(2) - V_{\text{AK}}(1)$.

3. The rest of the points C, D, E...in Figure 3.21(a) can be obtained with the same method in the above step. When the diode is blocked, the same method can also be applied to get each V_1 value.



(a) V_1-V_{AK} plan (b) $f - V_{\text{AK}}$ plan

FIGURE 3.21: Method to get V_1 values

To minimize the integration approximate calculation error of eq.(3.9), it is necessary that ΔV_{AK} is as small as possible. Therefore, mathematical functions are used to express R_1 and R_2 values and when $V_{\mathrm{AK}} \geq 0.5V$, $R_{1,\mathrm{real}}$ and $R_{2,\mathrm{real}}$ values presented in Figure 3.20 are used.

To express R_1 values, following equations are used:

1. When $V_{\mathrm{AK}} \geq 0V$

$$R_1 = \frac{a1}{d1 + \left(\frac{V_{\mathrm{AK}}}{b1}\right)^{c1}} + e1 \cdot \exp\left(f1 \cdot V_{\mathrm{AK}}\right), \tag{3.10}$$

2. When $V_{\mathrm{AK}} < 0V$

$$R_1 = a2 - b2 \cdot \exp\left(c2 \cdot V_{\mathrm{AK}}\right), \tag{3.11}$$

The parameters in eq.(3.10) and eq.(3.11) can be obtained by fitting method and they are given in Table 3.1. The comparison between the chosen functions and R_1 values at ON and OFF states are presented in Figure 3.22(a), in which V_{AK} means that the diode is forward biased (ON state) and V_{KA} means that the diode is in OFF state. It is shown that the chosen functions represent well R_1 values, in the zone where there are no measured data, R_1 values can be obtained by extrapolation of the chosen functions.

TABLE 3.1: Parameters of eq.(3.10) and eq.(3.11)

$a1$	$b1$	$c1$	$d1$	$e1$	$f1$	$a2$	$b2$	$c2$
10	0.347	9.44	0.002	1.14	-2.88	1.828×10^5	1.796×10^5	0.04

TABLE 3.2: Parameters of eq.(3.12) and eq.(3.13)

$a3$	$b3$	$c3$	$d3$	$e3$	$f3$	$a4$	$b4$	$c4$	$d4$	$e4$
202.6	0.194	6.35	19.84	0.51	-2.21	14	0.5364	0.72	4.767	0.823

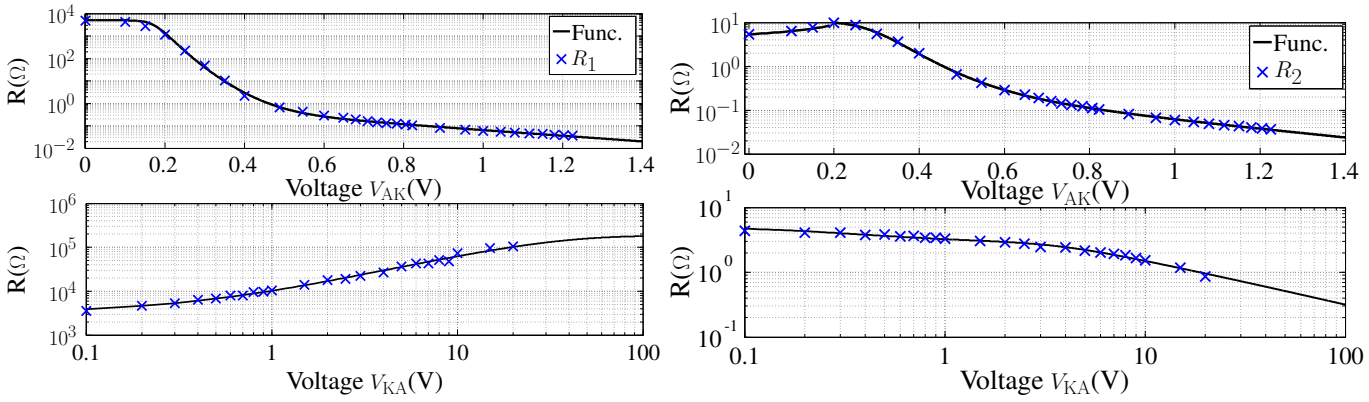
To express R_2 values, following equations are used:

1. When $V_{\mathrm{AK}} \geq 0.2V$

$$R_2 = \frac{a3}{d3 + \left(\frac{V_{\mathrm{AK}}}{b3}\right)^{c3}} + e3 \cdot \exp\left(f3 \cdot V_{\mathrm{AK}}\right), \tag{3.12}$$

2. When $V_{\mathrm{AK}} < 0.2V$

$$R_2 = \frac{a4}{1 + \left(\frac{0.2 - V_{\mathrm{AK}}}{b4}\right)^{c4}} - d4 \cdot \exp\left(-e4 \cdot (0.2 - V_{\mathrm{AK}})\right), \tag{3.13}$$



(a) R_1 (b) R_2

FIGURE 3.22: Functions used to express R_1 and R_2values of the diode model at ON and OFF states

The parameters in eq.(3.12) and eq.(3.13) can be obtained by fitting method and they are given in Table 3.2. The comparison between the chosen functions and R_2 values at ON and OFF states are presented in Figure 3.22(b). It is shown that the chosen functions represent well R_2 values, in the zone where there are no measured data, R_2 values can be obtained by extrapolation of the chosen functions.

Thus, eq.(3.10)-(3.13) are then applied in eq.(3.9) to get V_1 values[2], then both R_{1s} and R_{2s} values can be obtained according to eq.(3.7). To get I_D value which corresponds to each V_1 value, the measured diode static characteristic at $T_j = 40°C$ shown in Figure 3.10 can be used and linearly interpolated between the measured points. As the diode reverse static characteristic is not obtained through the measurement, the following method is used to get I_D values when diode is blocked.

Following equation can be obtained based on Figure 3.19:

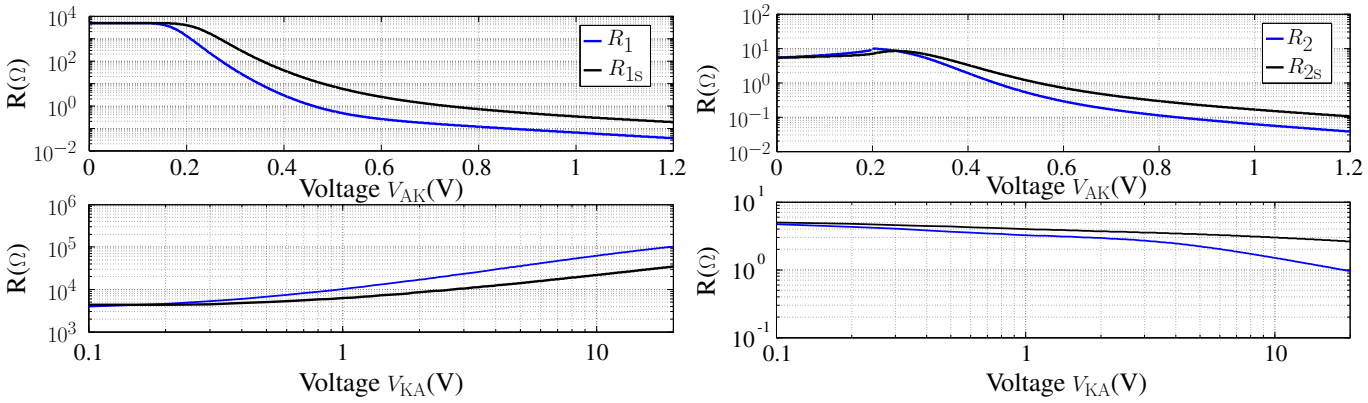
$$dI_D = \frac{1}{R_1 + R_2} \cdot dv_{AK}, \tag{3.14}$$

By integrating eq.(3.14), I_D can be obtained through the following equation:

$$\int_0^{I_D} dI_D = \int_0^{V_{AK}} \frac{1}{R_1 + R_2} \cdot dv_{AK} \tag{3.15}$$

In the proposed diode STTH15R06 model, the obtained R_{1s} and R_{2s} values in comparison with their dynamic values R_1 and R_2 are shown in Figure 3.23. Up until now, R_{1s} and R_{2s} values with the evolution of voltage V_{AK} can be obtained based on their dynamic values, which helps to get a non-linear evolution of the voltage V_{AA1} (shown in Figure 3.12) in the next step, which will be presented in the next chapter.

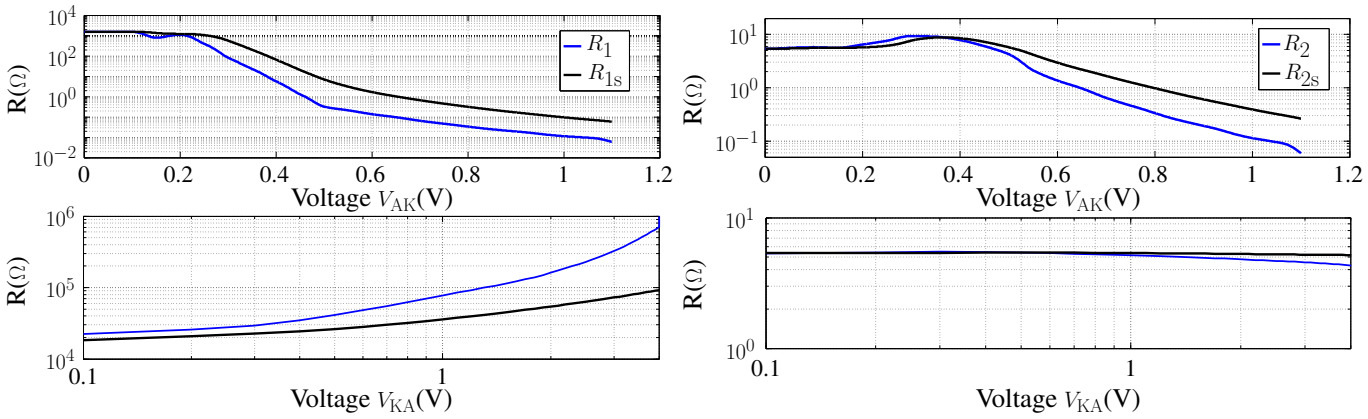
[2]Both integration and interpolation are allowed to be in an easy way because of those equations.



(a) R_1 (b) R_2

FIGURE 3.23: R_{1s} and R_{2s} in comparison with R_1 and R_2 values of diode STTH15R06

The same method is then applied for the diode MUR880E to get model resistance parameters. For this diode, it is shown in Figure 3.24 the comparison between R_{1s}, R_{2s} values and R_1, R_2 values obtained in Figure 3.18.



(a) R_1 (b) R_2

FIGURE 3.24: R_{1s} and R_{2s} in comparison with R_1 and R_2 values of diode MUR880E

In the next section, the obtained R_{1s}, R_{2s} and C values will be applied in PSPICE to model the diode.

3.1.4 Simulation implementation

There are three non-linear components used in the diode model: C, R_{1s} and R_{2s}. They can be represented by three voltage-controlled current sources shown in Figure 3.25. With the similar reason explained in Chapter 3.1.1, the voltage dependency of all the three components are chosen to be V_{AA1} in the equivalent circuit shown in Figure 3.12, so the three current sources are $I_C = C\left(V_{AA1}\right)\frac{dV_{AA1}}{dt}$ for C, $I_{R1} = \frac{V_{AA1}}{R_{1s}(V_{AA1})}$ for R_{1s} and $I_{R2} = \frac{V_{A1K1}}{R_{2s}(V_{AA1})}$.

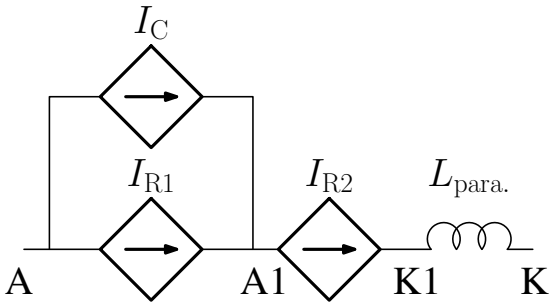


FIGURE 3.25: Diode behavior model in PSPICE simulation

The evolution of R_{1s} and R_{2s} with V_{AA1} are shown in Figure 3.26. Their evolutions can be expressed by the following functions with the parameters listed in Table 3.3 and Table 3.4. Those functions are compared with R_{1s} and R_{2s} values in Figure 3.26.

TABLE 3.3: Parameters in eq.(3.16)(3.17) for diode STTH15R06

$a1$	$b1$	$c1$	$d1$	$e1$	$f1$	$a2$	$b2$	$c2$	$d2$	$e2$	$f2$
1985	0.259	11.63	0.415	6.15	4.51	9.19	0.35	9.98	1.516	0.954	2.77

TABLE 3.4: Parameters in eq.(3.18)(3.19) for diode STTH15R06

$a3$	$b3$	$c3$	$a4$	$b4$	$c4$	$d4$	$e4$	$f4$
1.06×10^5	1.01×10^5	0.0174	2.3	131.8	0.6	0.553	0.97	1.56

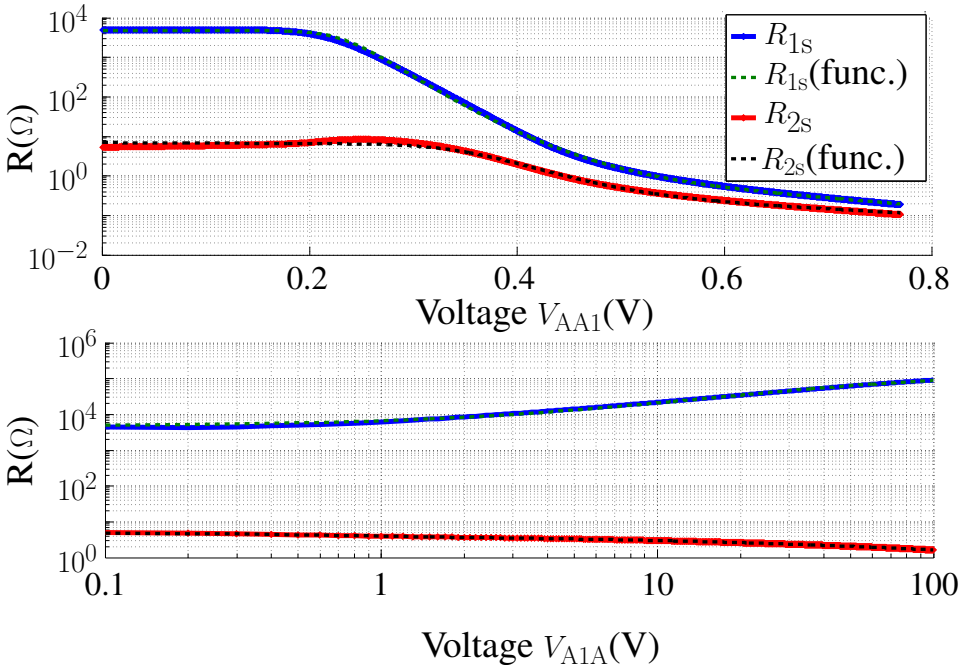


FIGURE 3.26: $R_{1s}(V_{AA1})$ and $R_{2s}(V_{AA1})$ values and functions for diode STTH15R06

1. When $V_{AA1} \geq 0V$

$$R_{1s} = \frac{a1}{d1 + \left(\frac{V_{AA1}}{b1}\right)^{c1}} + e1 \cdot exp\left(-f1 \cdot V_{AA1}\right), \tag{3.16}$$

$$R_{2s} = \frac{a2}{d2 + \left(\frac{V_{AA1}}{b2}\right)^{c2}} + e2 \cdot exp\left(-f2 \cdot V_{AA1}\right); \tag{3.17}$$

2. When $V_{AK} < 0V$

$$R_{1s} = a3 - b3 \cdot exp(c3 \cdot V_{AA1}), \tag{3.18}$$

$$R_{2s} = \frac{a4}{d4 + \left(\frac{-V_{AA1}}{b4}\right)^{c4}} + e4 \cdot exp\left(f4 \cdot V_{AA1}\right), \tag{3.19}$$

TABLE 3.5: Parameters in eq.(3.16)(3.17) for diode MUR880E

$a1$	$b1$	$c1$	$d1$	$e1$	$f1$	$a2$	$b2$	$c2$	$d2$	$e2$	$f2$
53.64	0.47	13.12	0.004	43.3	5.76	57.32	0.418	11.33	8.95	0.26	0.06

TABLE 3.6: Parameters in eq.(3.18)(3.19) for diode MUR880E

$a3$	$b3$	$c3$	$a4$	$b4$	$c4$	$d4$	$e4$	$f4$
2.014×10^6	2×10^6	0.0114	5.17	5.1×10^4	1.4×10^{-4}	9×10^{-5}	0.28	0.56

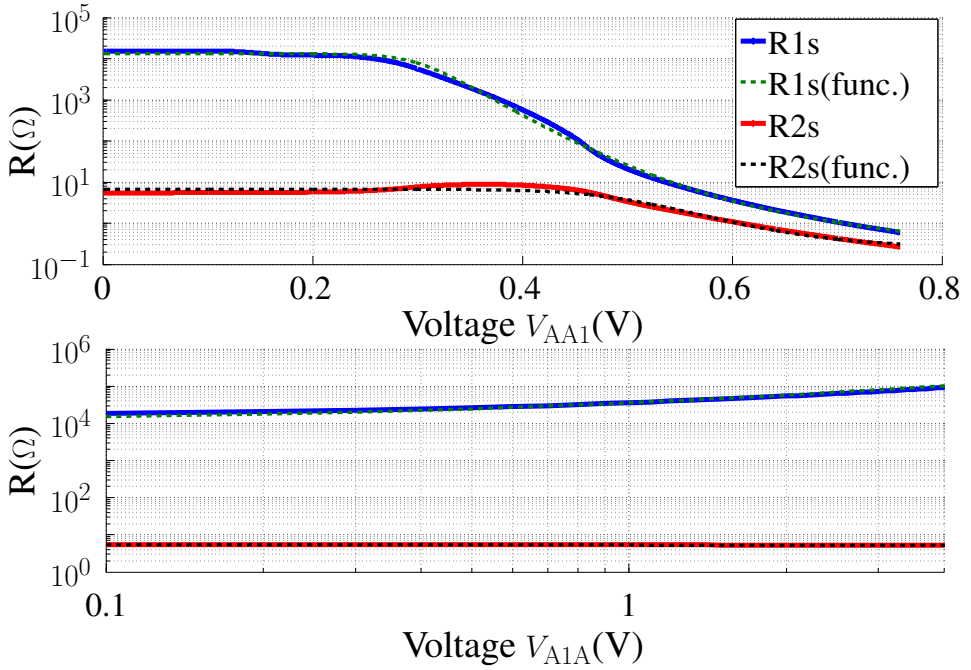


FIGURE 3.27: $R_{1s}(V_{AA1})$ and $R_{2s}(V_{AA1})$ values and functions for diode MUR880E

It is shown in Figure 3.26 that the chosen functions represent well the $R_{1s}(V_{AA1})$ and $R_{2s}(V_{AA1})$ values. Those functions can be applied in PSPICE for simulation. It is to be noted that discrete values can be also used in PSPICE for simulation, but they are limited to certain number of data points and they can only be interpolated linearly in the software. For this reason, it is preferred to develop behavioral mathematical functions for the models in the software.

The same functions are then used to obtain R_{1s} and R_{2s} values shown in Figure 3.24 for diode MUR880E. The parameters are shown in Table 3.5 and Table 3.6. Those functions are compared with R_{1s} and R_{2s} values in Figure 3.27 for diode MUR880E.

The switching waveforms of the above diode behavior models are to be compared with the measurement, which will be presented in Chapter 4.1. The modeling of a SiC diode is simpler than that, which will be presented in Chapter 4.3.1. In the next chapter, a SiC JFET behavior model will be presented based on the characterization results.

3.2 SiC JFET Characterization and Modeling

In this section, a "normally-off" SiC JFET (SJEP120R063) is modeled. The model allows to represent its static characteristic which is based on the characterization results presented in Chapter 2.1. Then its dynamic characteristics when the power device is blocked and is in linear region are presented in the form of C_{gs}, C_{gd} and C_{oss} evolution with V_{DS} and V_{GS}. The model to represent its inter-electrode capacitances is based on those characterization results.

3.2.1 Static characteristics results and modeling

From the internal structure shown in Figure 2.18(a), the SiC JFET can be represented by its equivalent circuit shown in Figure 3.28. The static characteristic of the power device can be represented by channel characteristic and gate characteristic. The former is modeled by a current source controlled by V_{GS} and V_{DS} while the latter is modeled by two body diodes D_{GS} and D_{GD}.

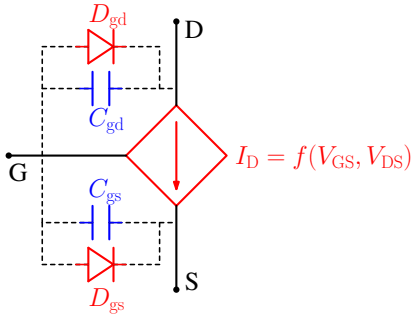


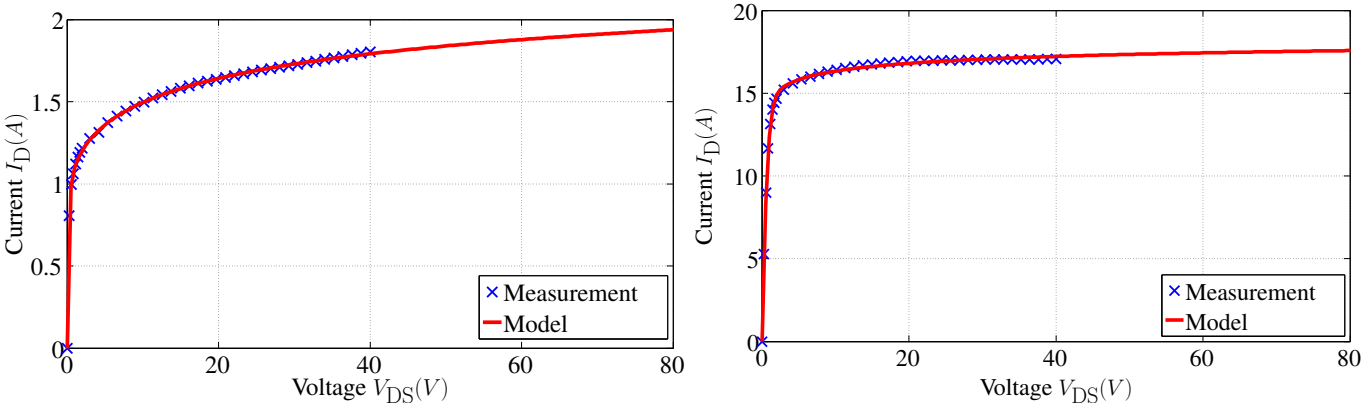
FIGURE 3.28: SiC JFET equivalent circuit

The channel characterization result is represented in Figure 2.13. It is modeled by a voltage-controlled current-source in PSPICE, so it is necessary to develop a mathematical function to represent channel characteristic[3].

At one V_{GS}, the eq.(3.20) can be used to represent $I_D - V_{DS}$ relation. The choice of this equation is inspired by a developed physical equation by authors in [119] to represent the static characteristic

[3]Interpolation in two dimension is not possible in PSPICE.

of a GaAs FET. It is to be noted that as it is a behavior model presented in this section, there is no physical meaning in parameters a, b, c, d, e in eq.(3.20). Those parameters can be obtained by fitting method. The obtained results are shown in Figure 3.29 for the the comparison between the model and the measurement when $V_{\mathrm{GS}} = 1.4V$ and $V_{\mathrm{GS}} = 2V$ at $T_{\mathrm{j}} = 25°C$.



(a) $V_{\mathrm{GS}} = 1.4V$ (b) $V_{\mathrm{GS}} = 2V$

FIGURE 3.29: SiC JFET static characteristic comparison at $V_{\mathrm{GS}} = 1.4V$ and $V_{\mathrm{GS}} = 2V$ ($T_{\mathrm{j}} = 25°C$)

It can be seen that the chosen function represent well the power device static characteristic at one V_{GS}. When $V_{\mathrm{DS}} > 40V$, the relation I_{D}-V_{DS} can be estimated by extrapolation of the presented function.

$$I_{\mathrm{D}} = -\frac{a}{1 + \left(\frac{V_{\mathrm{DS}}}{b}\right)^{c}} + a + d \cdot \tanh\left(e \cdot V_{\mathrm{DS}}\right) \tag{3.20}$$

TABLE 3.7: s_1-s_4 values in eq.(3.21) for each parameter(various units without physical meaning)

s	s_1	s_2	s_3	s_4
a	-7.238	1.56	9.65	7.238
b	22.43	1.5	30.54	1.65
c	0	1	0	0.456
d	-60.66	2.41	7.768	60.66
e	2.59	1.78	12.4	0.56

The obtained parameters a, b, c, d, e at different V_{GS} values are shown in Figure 3.30. The evolution of all those parameters with V_{GS} voltage can be represented by a single function (3.21), where s indicates either a, b, c, d or e. The values of s_1-s_4 for each parameter a, b, c, d, e are shown in Table 3.7. The functions are compared together with the obtained parameters of eq.(3.20) in Figure 3.30. In the area where there is no measured values, the parameters can be estimated by extrapolation of the presented functions.

$$s = \frac{s_1}{1 + \left(\frac{V_{GS}}{s_2}\right)^{s_3}} + s_4 \tag{3.21}$$

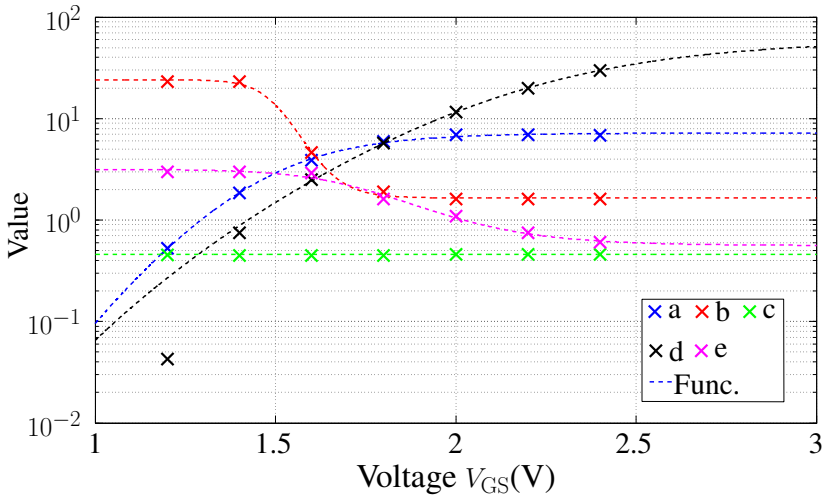
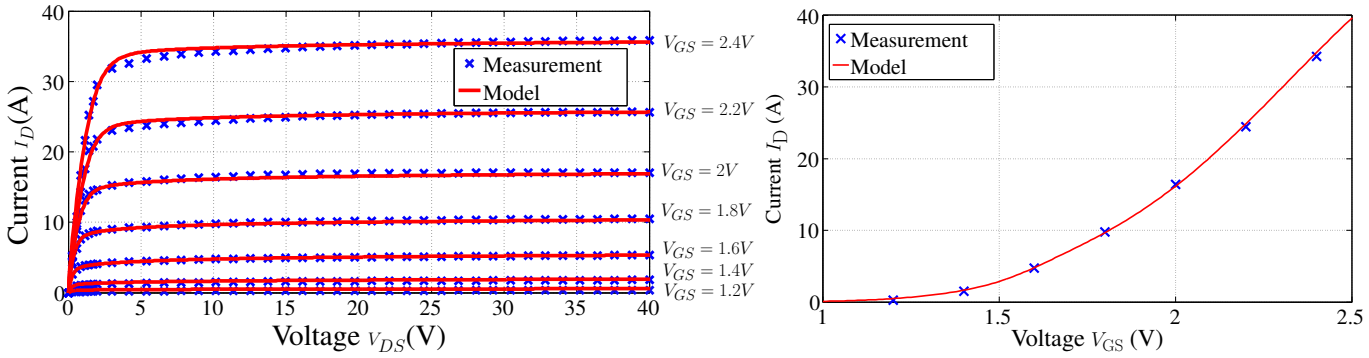


FIGURE 3.30: Comparison between the functions and the obtained parameters of eq.(3.20) with V_{GS} evolution

Therefore, relations (3.20) (3.21) can be used together to model power device channel static characteristic. When $T_j = 25°C$, the comparison between the model and the measurement for different V_{GS} and V_{DS} voltages is shown in Figure 3.31(a), while the comparison of the power device transconductance when $V_{DS} = 10V$ is shown in Figure 3.31(b). These results show that the model represents well the power device channel static characteristic.



(a) Static characteristic

(b) Transconductance

FIGURE 3.31: The comparison between the model and the measurement on static characteristic and transconductance when $T_j = 25°C$

The body diode D_{GS} static characteristic can be represented by the equation (3.22), which is inspired by the diode classical physical equation represented in eq.(1.3). As it is a behavior model, there is no physical meaning in the parameters a, b, c in eq.(3.22). The values of the parameters[4] can be obtained by the fitting method: $a = 1 \times 10^{18}, b = 0.068, c = 0.342$. It is shown in Figure 3.32 the

[4]The units of the parameters are: $a(\mathrm{A}^{-1})$, b(V) and $c(\Omega)$.

comparison between the model and the datasheet values ($T_j = 25°C$) for the static characteristic of the diode D_{GS}. As there is no diode D_{GD} static characteristic found in the datasheet, it is supposed to follow the same static characteristic.

$$V_{GS} = b \cdot log\,(a \cdot I_{GS} + 1) + c \cdot I_{GS} \tag{3.22}$$

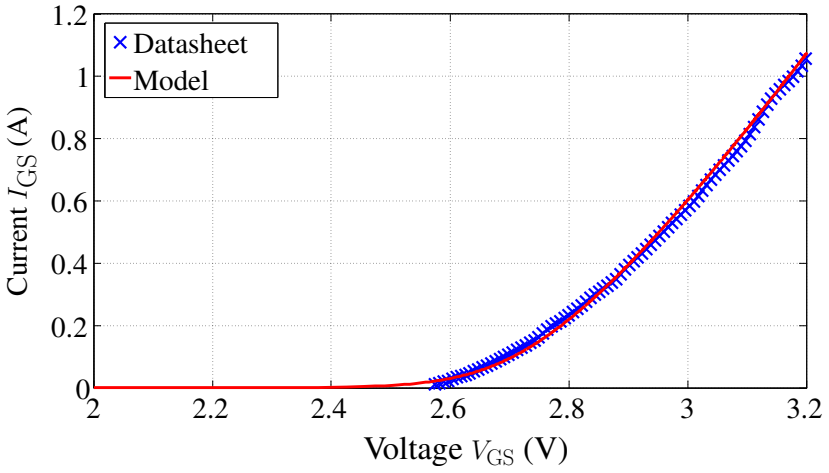


FIGURE 3.32: Comparison between the function and datasheet values of diode D_{GS} static characteristic when $T_j = 25°C$

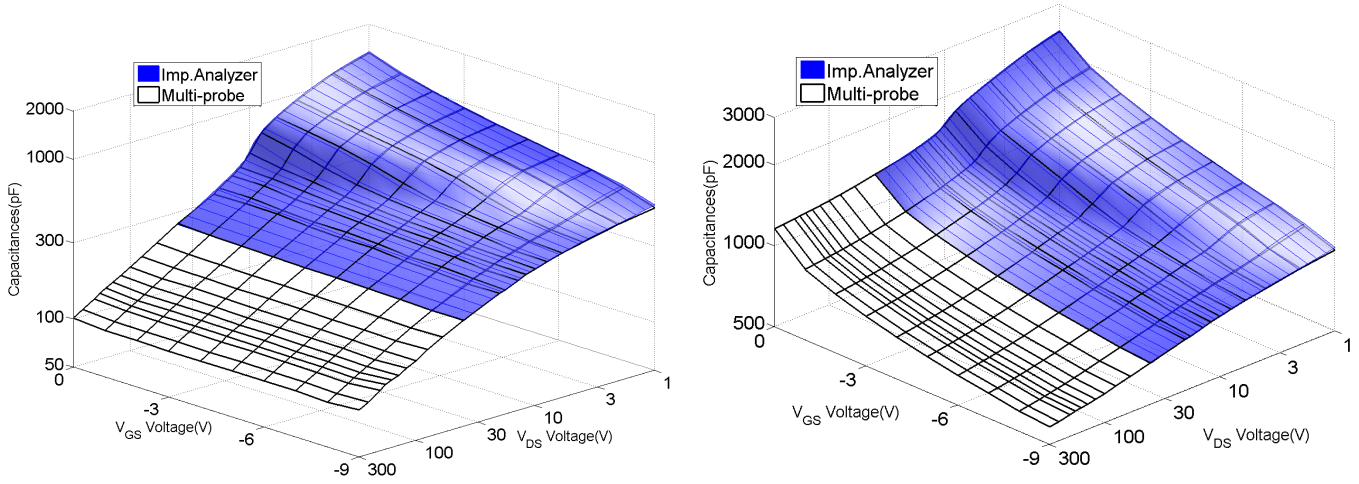
3.2.2 Dynamic characteristics: power device is blocked

The SiC JFET inter-electrode capacitances evolution with both V_{DS} and V_{GS} voltages are first characterized when the power device is blocked. For this JFET, because of the negligence of C_{ds} when the device is blocked, C_{rss} can be measured in the similar configuration shown in Figure 2.16(b); while C_{iss} can be measured in the similar configuration shown in Figure 2.16(c). The bias voltage of V_{GS} can be obtained by using a battery, of which the inner resistance can be neglected in the measurement. The inter-electrode capacitances values are measured around 1MHz.

The results of the measured C_{rss} and C_{iss} capacitances of the JFET using multi-current-probe (MCP) method and impedance analyzer are shown in Figure 3.33. As shown in the results, SiC JFET inter-electrode capacitances evolution is related with both V_{DS} and V_{GS}, while this result is not given in its datasheets. Below 40V, two surfaces are almost overlapping, which means that both C_{iss} and C_{rss} measured with the impedance analyzer concur well with the proposed MCP method. Thus, it proves the validity of the method in low voltage. This makes the measurement results of the presented method in high voltage reliable, which can be a reference for not-presented capacitance evolution in a datasheet.

In addition, compared to the impedance analyzer of which the bias V_{DS} voltage is limited to 40V, the MCP method allows to increase bias V_{DS} voltage, which is important for SiC power devices switching in high voltage, because the values of the inter-electrode capacitances under full switching voltage

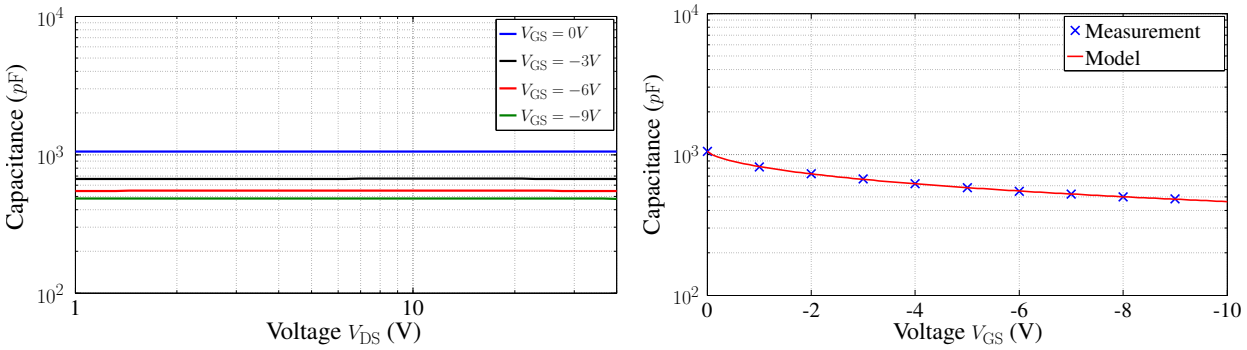
influence the overall spectrum of electromagnetic noise level by involving in the parasitic resonances at the end of the turn-off commutation [47].



(a) C_{rss} measurement (b) C_{iss} measurement

FIGURE 3.33: SiC JFET inter-electrode capacitances measurement results

Similar to the diode capacitance modeling, the non-linearity of the above inter-electrode capacitances can be represented by voltage-controlled current-source in PSPICE. As their evolution is both on V_{GS} and V_{DS} voltages, it is necessary to develop proper functions to represent the evolution.



(a) C_{gs} evolution (b) C_{gs} modeling

FIGURE 3.34: SiC JFET C_{gs} evolution on V_{GS} and V_{DS} voltages and modeling when the device is blocked

The obtained C_{gs} ($C_{\text{gs}} = C_{\text{iss}} - C_{\text{rss}}$) values on different V_{GS} and V_{DS} voltages are shown in Figure 3.34(a). It is shown that V_{DS} has almost no influence on C_{gs} evolution when the device is blocked; however, when V_{GS} decreases, C_{gs} value decreases. Thus, C_{gs} can be modeled with the equation (3.23). The parameters a, b, c are obtained by fitting method: $a = 1052, b = 6.89, c = 0.65$[5]. The comparison between the model and the measurement is shown in Figure 3.34(b).

[5]Various units without physical meaning with a(pF), b(V) and c without unit.

$$C_{gs} = \frac{a}{1 + \left(\frac{-V_{GS}}{b}\right)^c} \tag{3.23}$$

According to the C_{rss} measurement results shown in Figure 3.33(a), at one V_{DS} voltage, C_{rss} value decrease when V_{GS} voltage decreases; while at one V_{GS} voltage, C_{rss} value decrease when V_{DS} voltage decreases. C_{rss} values can be represented with the dependency on V_{DG} voltage. A similar function given in (3.24) can be applied to express C_{rss} values, where $V_{DG} = V_{DS} - V_{GS}$. The parameters a, b, c can be obtained by fitting method: $a = 1997, b = 1.936, c = 0.6$. The comparison between the model and the measurement is shown in Figure 3.35.

$$C_{rss} = \frac{a}{1 + \left(\frac{V_{DS}-V_{GS}}{b}\right)^c} \tag{3.24}$$

It is shown in Figure 3.34(b) and Figure 3.35 that the presented functions represent well both C_{gs} and C_{rss} evolution when the power device is blocked.

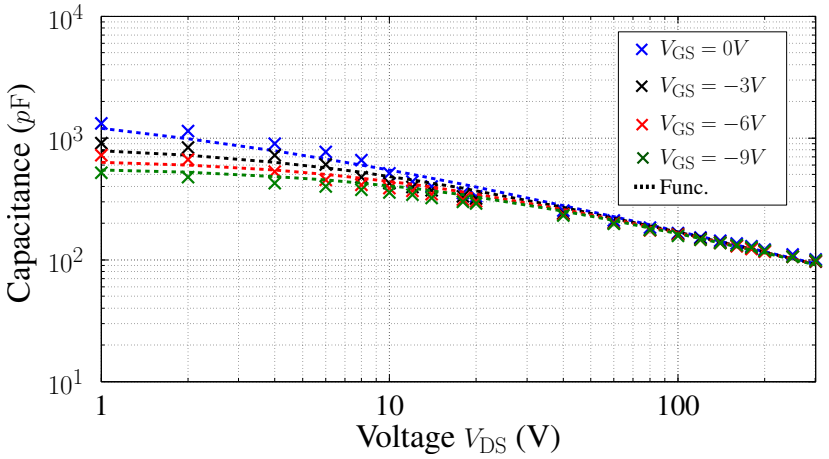


FIGURE 3.35: SiC JFET C_{rss} modeling when the device is blocked

3.2.3 Dynamic characterization: power device in linear region

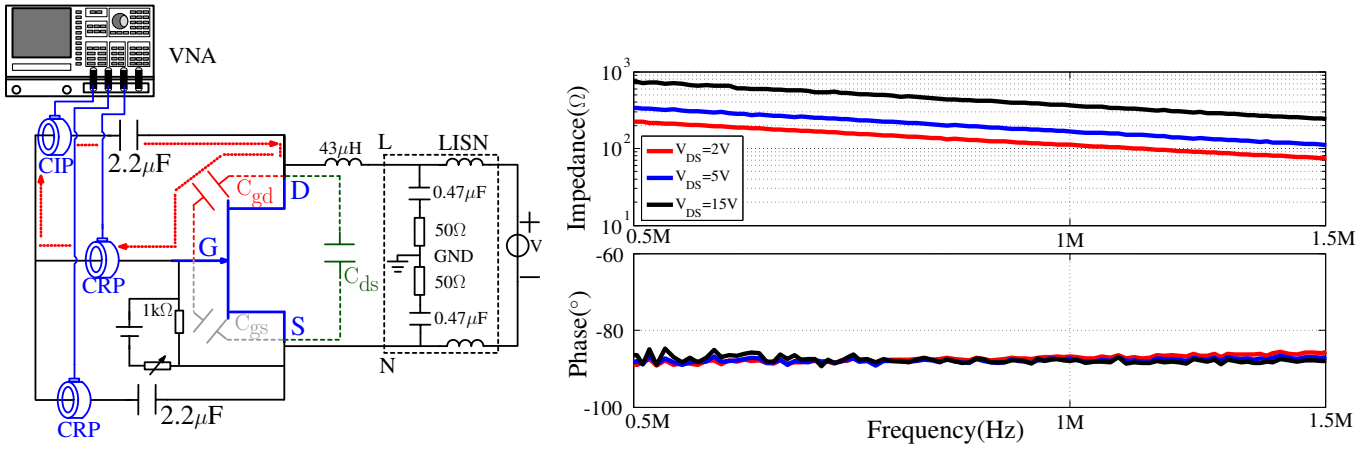
It is shown in Figure 1.23(b) the power transistor switching waveforms. It can be seen that during the increase and decrease of the V_{DS} voltage, V_{GS} value is higher than the power transistor threshold voltage V_{th} and the power transistor conducts the current I_D in its channel. To finely model the power transistors, it is necessary to investigate the influence of I_D or V_{GS}, V_{DS} voltages on inter-electrode capacitances evolution.

In this section, the inter-electrodes capacitances evolution of the SiC JFET when it is in linear region is presented.

3.2.3.1 C_{gd} measurement results

When the SiC JFET is in linear region, C_{gd} is first characterized by the three-current-probe method. The measurement configuration is shown in Figure 3.36(a), which has been presented in Chapter 2.2.3.2 "Transistor".

In the measurement, junction temperature T_j is controlled to be constant at $25°C$. When $V_{GS} = 1.4V$, the measured C_{gd} impedance and phase at different V_{DS} voltages is shown in Figure 3.36(b). It can be seen that the measured phase is almost -90° around 1MHz, which corresponds to a capacitance value. Thus, C_{gd} values can be obtained directly.



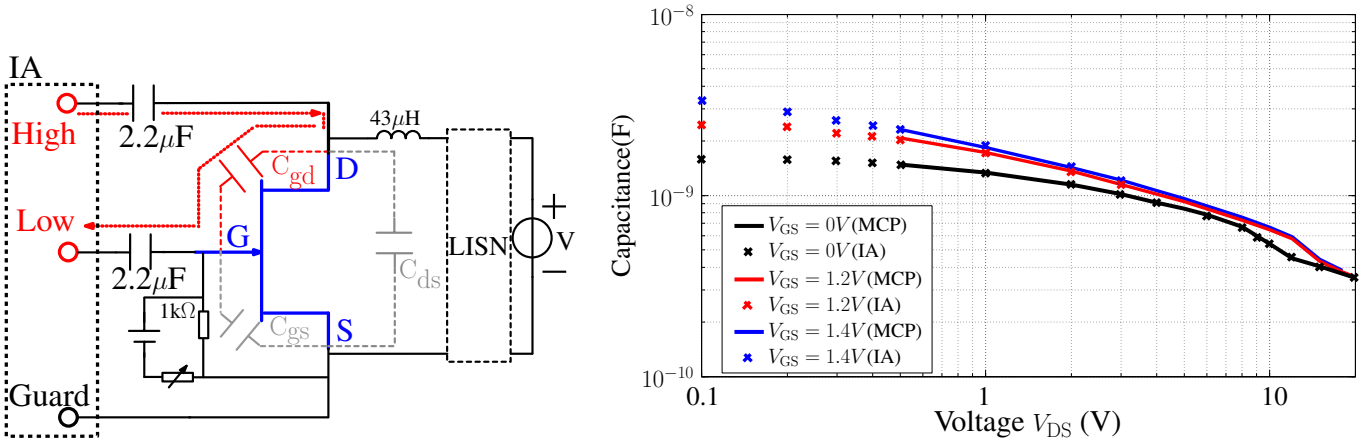
(a) Measurement configuration

(b) C_{gd} measurement results when $V_{GS} = 1.4V$

FIGURE 3.36: C_{gd} measurement configuration and results at different V_{DS} values by MCP method

To validate the above C_{gd} measurement results by the MCP method, another measurement based on impedance analyzer (IA) is presented in Figure 3.37(a). The measurement principle is similar to that presented in Chapter 1.19(b). C_{gd} evolution is thereby directly measured, which is illustrated by the red dotted line showing the current flow in Figure 3.37(a). Its values are also obtained around 1MHz.

When V_{GS} is $1.2V$ and $1.4V$, C_{gd} measurement results of the above two methods are compared in Figure 3.37(b). It is shown that C_{gd} measured by the MCP method corresponds well with that measured by IA for the small V_{DS} voltage values. This result is able to validate the presented MCP method to characterize C_{gd} values when the power device is in linear region. With the advantage such as galvanic isolation between the measurement equipment and the power source, the MCP method is well adapted to characterize C_{gd} values when the power device in linear region. As what is shown in Figure 3.37(b), when the power device is in the linear region, C_{gd} increases with the increase of the V_{GS} voltage value. This result, which is involved in the power transistor switching trajectory, is important to model power device switching.



(a) Measurement configuration (b) Comparison of the measurement results

FIGURE 3.37: C_{gd} measurement configuration and results at different V_{DS} and V_{GS} voltages

3.2.3.2 C_{oss} measurement results

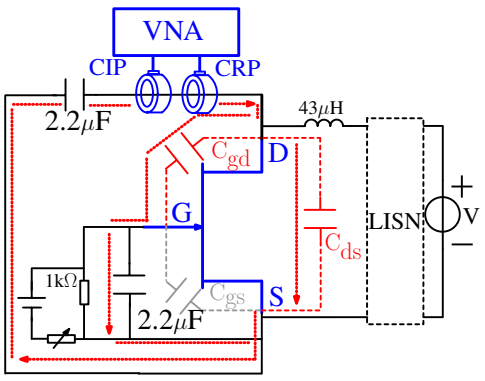
The capacitance C_{oss} is characterized by the MCP method by using two current probes. The measurement configuration is illustrated in Figure 3.38(a). The current probes are the same to those presented in Figure 2.33(a). This measurement configuration is similar to that shown in Figure 2.33(b), as a first 2.2μF is used to block the DC voltage between D and S. Meanwhile a second capacitor of the same value is connected between G and S, in order to make a short circuit around megahertz, because its impedance is much smaller than that of C_{gs}. An equivalent circuit of the power device in this configuration can be represented in Figure 3.38(b), where R represents dynamic resistance value of the transistor channel.

As shown previously, both equivalent bonding wire inductance L and the influence of the 2.2μF capacitor between G and S can be neglected when the measurement frequency is inferior to 10MHz. Therefore, the measured admittance can be expressed by the following equation:

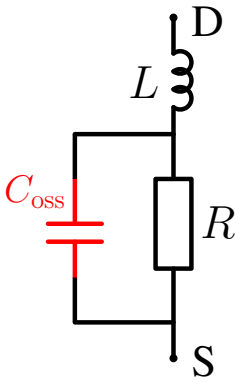
$$Y_{mes} = \frac{1}{R} + j\omega(C_{oss}) \tag{3.25}$$

According to the eq.(3.25), output capacitance (C_{oss}) values can be finally determined by calculating the imaginary part of the measured admittance.

It is presented in Figure 3.39(a) the measured C_{oss} admittance and phase when $V_{GS} = 1.4V$ and $T_j = 25°C$. From those measurement curves, C_{oss} values can be determined around 1MHz and they are shown in Figure 3.39(b).



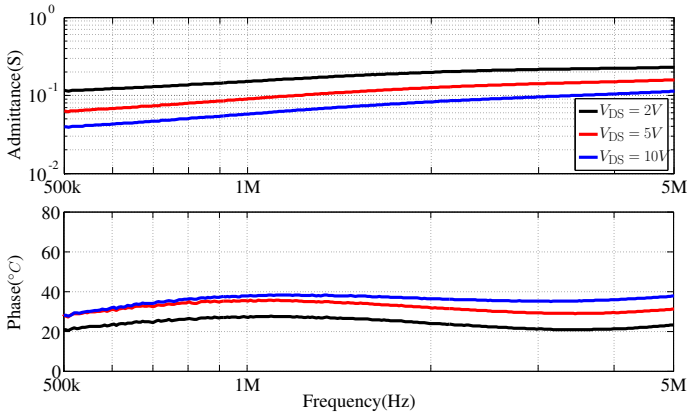
(a) Measurement configuration



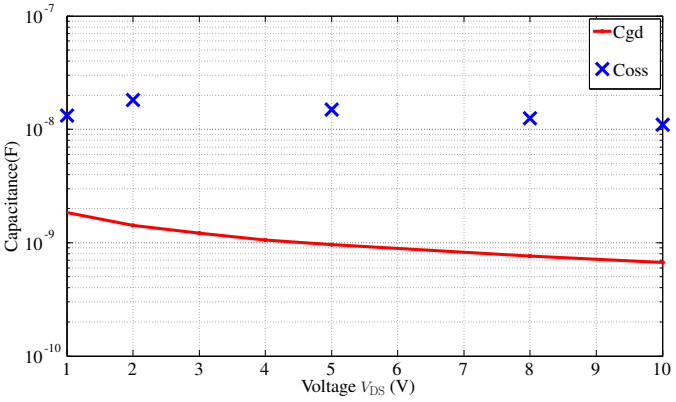
(b) Small-signal equivalent circuit

FIGURE 3.38: C_{oss} measurement configuration and equivalent circuit by the MCP method

According to the internal structure of the power device presented in Figure 2.18(a), C_{ds} capacitance can be neglected. However, with the measurement results shown in Figure 3.39(b), it is shown that C_{oss} values seem to increase to a few tens of nF when the power device is in linear region. It is surmised by this result that there is a surge increase of the C_{ds} values. In order to validate this result, the same power device is characterized by another measurement based on the single-pulse method.



(a) Measurement result

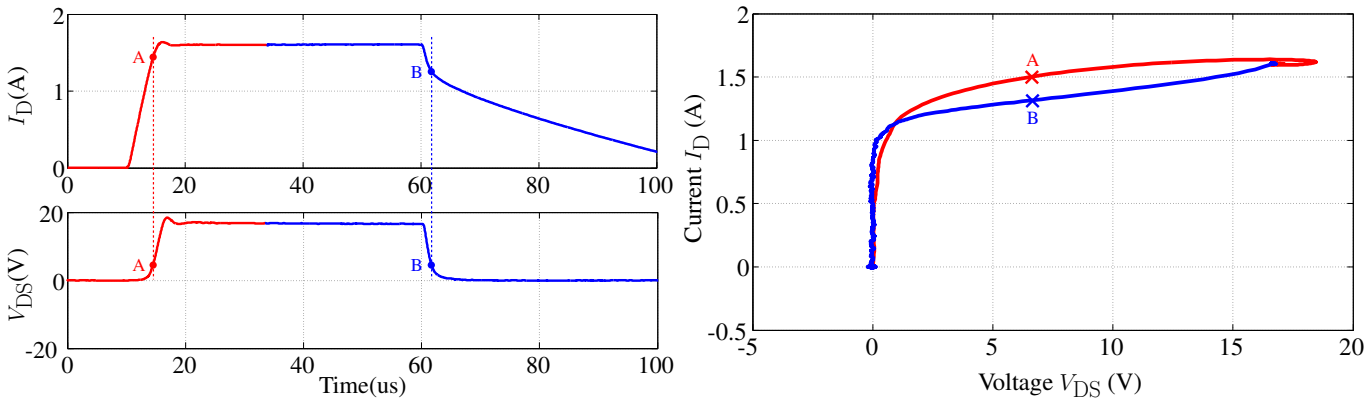


(b) C_{oss} and C_{gd} values

FIGURE 3.39: C_{oss} measurement results (V_{GS}=1.4V)

The principle of the single-pulse method has been presented in Chapter 2.1. It is presented in Figure 3.40(a) the waveforms of the current I_D and the voltage V_{DS} when the pulse duration is 50μs. They are then combined and presented in Figure 3.40(b) in the form of I_D-V_{DS} plan.

It is shown in Figure 3.40(b) that at one V_{DS} voltage, the measured I_D during the pulse-on is different to that measured during the pulse-off. This current difference is possibly due to the charge and discharge of C_{oss} capacitances at pulse-on and pulse-off.



(a) Waveforms

(b) V_{DS}-I_D relation

FIGURE 3.40: I_D-V_{DS} waveforms and relation (V_{GS}=1.4V)

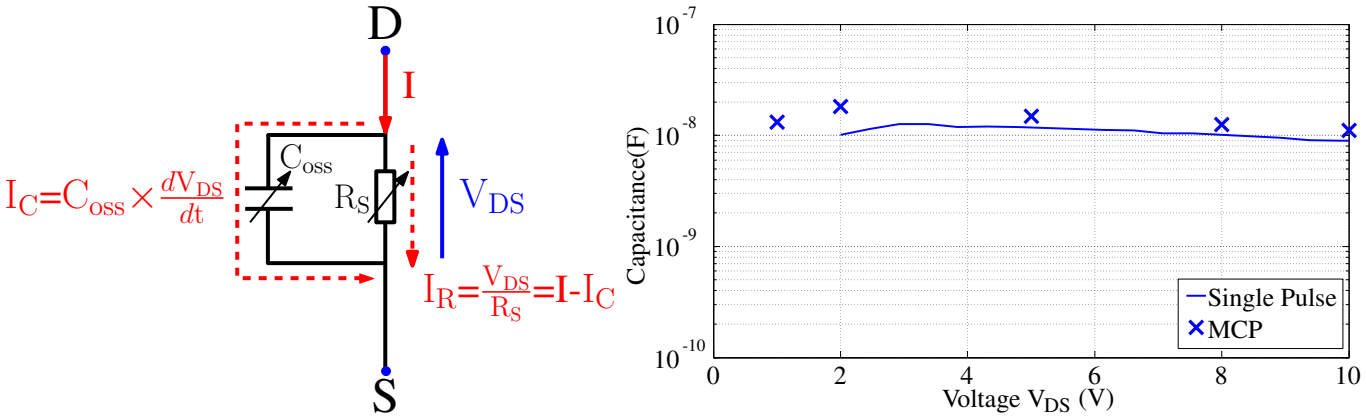
To verify this hypothesis, C_{oss} capacitance values are then calculated according to the RC equivalent circuit shown in Figure 3.41(a). The current I_D slope during the measurement shown in Figure 3.40(a) is smaller than 1A/μs, so the bonding wires inductance L inside the power device packaging can be neglected. In Figure 3.41(a), R_S represents static resistance values of the SiC JFET channel. Points A and B shown in Figure 3.40(b) represent one V_{DS} value at two different instants, thus the following equation can be applied to calculate C_{oss} values.

$$\frac{V_{DS}}{R_S} = I - C_{oss} \times \left(\frac{dV_{DS}}{dt}\right) \tag{3.26}$$

In eq.(3.26), $\frac{dV_{DS}}{dt}$ corresponds to points A and B respectively. When the power transistor is in linear region, C_{oss} evolution can be determined by varying V_{DS} voltage values in eq.(3.26).

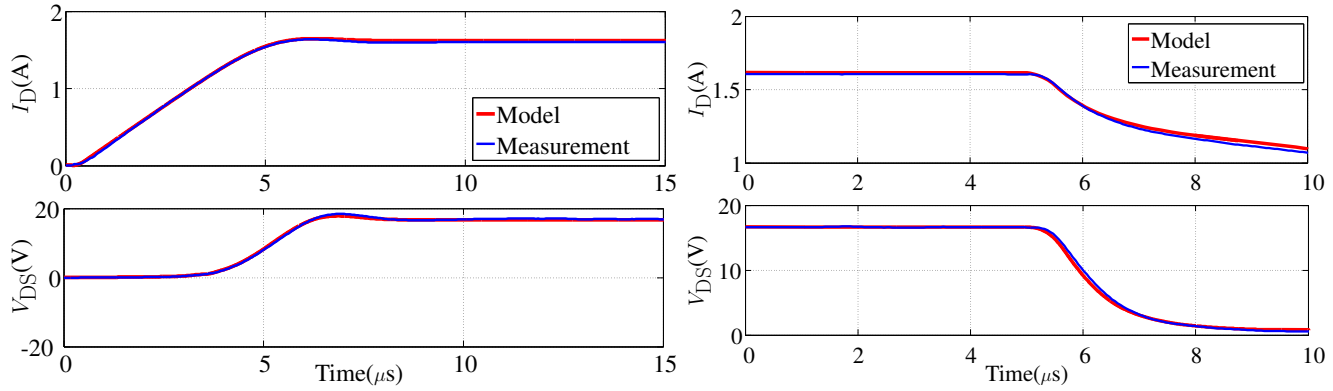
It is presented in Figure 3.41(b) the comparison of C_{oss} values between the calculation based on single-pulse method and the measurement by the MCP method. It is shown that the obtained C_{oss} values by these two methods are similar, which confirms the apparent increase of C_{oss} values when the power device is in linear region.

Then, by using the obtained R_S and C values, the equivalent circuit shown in Figure 3.41(a) is simulated in the circuit presented in Figure 2.1 in order to validate V_{DS} dynamic effect as rising and falling. It is presented in Figure 3.42 the comparison between the measurement and the simulation results, which proves a good consistency between the model and the measurement. It is surmised by this result that at one V_{GS} voltage, the power transistor can be represented by a RC model shown in Figure 3.41(a), of which C represents C_{oss} values. It can be noted that, compared to the MCP method, this calculation method based on the single-pulse measurement makes it possible to control T_j easily and to determine C_{oss} values on high V_{DS} voltage values when the power device in linear region.

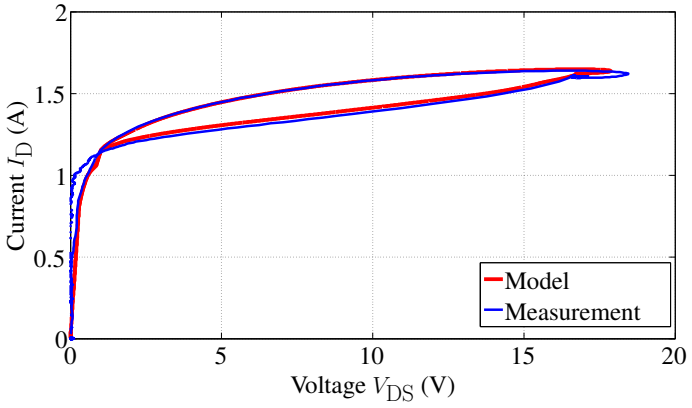


(a) Equivalent circuit (b) Measurement results

FIGURE 3.41: Equivalent circuit and C_{oss} measurement results



(a) V_{DS} rising (b) V_{DS} falling



(c) I_D-V_{DS} relation

FIGURE 3.42: Comparison between the model and the measurement with V_{DS} rising and falling (V_{GS}=1.4V)

The above SiC JFET inter-electrode capacitances characterization results reveal that, when the power device is in linear region, C_{gd} capacitance increases slightly with V_{GS} voltage and C_{oss} capacitance seems to increase to a few tens of nF. Furthermore, it is presented by authors in [120] that the channel current might increase C_{ds} capacitance values by a factor of 10 for a MOSFET. Thus, it

seems consistent that for this SiC JFET, the increase of the measured C_{oss} apparent values are due to the surge increase of the C_{ds} capacitance values.

However, it is observed that there is a non-neglected internal gate resistor R_g inside the power device packaging in the technical datasheet of the SiC JFET. According to authors [121], the origin of one part of the R_g is due to the gate electrode. The influence of the R_g on characterization results is to be presented in the next section.

3.2.4 Internal gate resistance influence

In order to study the influence of the internal gate resistor R_g on SiC JFET characterization results when the power device is in linear region, it is necessary to model the characterization circuit with a detailed power device model. Therefore, R_g, the resistor of drain R_d and that of source R_s are included in the power device model in order to obtain an analytical expression of the measured impedance.

3.2.4.1 Multiple-current-probe method characterization circuit modeling

It is presented in Figure 3.43 the small-signal power device inter-electrodes capacitances (with C_{ds} and internal resistances) characterization circuit by the MCP method when the power device is in the linear region, in which the power device physical accessible electrodes are G', D' and S'. The influence of the parasitic inductances inside the packaging on measurement results can be neglected when the measurement frequency is inferior to 10MHz. The measurement circuit is modeled by AC small signal method. The voltage generator v_1 represents the inciting voltage source.

It is to be noted that the principle of the two-current-probe method is like that of the impedance analyzer without using Guard. It is able to measure an impedance by knowing the relation between the incited current and the inciting voltage, which can be expressed by $\frac{v_1}{i_D}$ in Figure 3.43 for the case of C_{oss} measurement.

The principle of the three-current-probe method is like that of the impedance analyzer while using Guard. It is able to measure an impedance by knowing the relation between one incited current and the inciting voltage, which can be expressed by $\frac{v_1}{i_G}$ in Figure 3.43 for the case of C_{gd} measurement.

Thus, the DUT behavior is studied in this section when it is incited by the voltage source v_1. By knowing the incited current i_G and i_D, the inter-electrode capacitance C_{gd} and C_{oss} values can be obtained.

The bias voltages of V_{GS} and V_{DS} are DC voltages, so they are not represented in the circuit. The v_{GS} gate voltage variation can induce a channel current $i_{ch} = g \cdot v_{GS}$, where g represents the power transistor dynamic transconductance.

From the circuit shown in Figure 3.43, the following six equations can be obtained:

$$\underline{V_{\mathrm{DS}}} = \underline{V_1} - \underline{I_{\mathrm{D}}} \cdot R_{\mathrm{d}} - \underline{I_{\mathrm{S}}} \cdot R_{\mathrm{s}} \tag{3.27}$$

$$\underline{V_{\mathrm{DG}}} = \underline{V_1} - \underline{I_{\mathrm{D}}} \cdot R_{\mathrm{d}} - \underline{I_{\mathrm{G}}} \cdot R_{\mathrm{g}} \tag{3.28}$$

$$\underline{V_{\mathrm{GS}}} = \underline{I_{\mathrm{G}}} \cdot R_{\mathrm{g}} - \underline{I_{\mathrm{S}}} \cdot R_{\mathrm{s}} \tag{3.29}$$

$$\underline{I_{\mathrm{D}}} = \underline{I_{\mathrm{S}}} + \underline{I_{\mathrm{G}}} \tag{3.30}$$

$$\underline{I_{\mathrm{G}}} = \frac{\underline{V_{\mathrm{DG}}}}{\underline{Z_{\mathrm{C_{gd}}}}} - \frac{\underline{V_{\mathrm{GS}}}}{\underline{Z_{\mathrm{C_{gs}}}}} \tag{3.31}$$

$$\underline{I_{\mathrm{D}}} = \frac{\underline{V_{\mathrm{DG}}}}{\underline{Z_{\mathrm{C_{gd}}}}} + g \cdot \underline{V_{\mathrm{GS}}} + \frac{\underline{V_{\mathrm{DS}}}}{\underline{Z_{\mathrm{C_{ds}}}}} \tag{3.32}$$

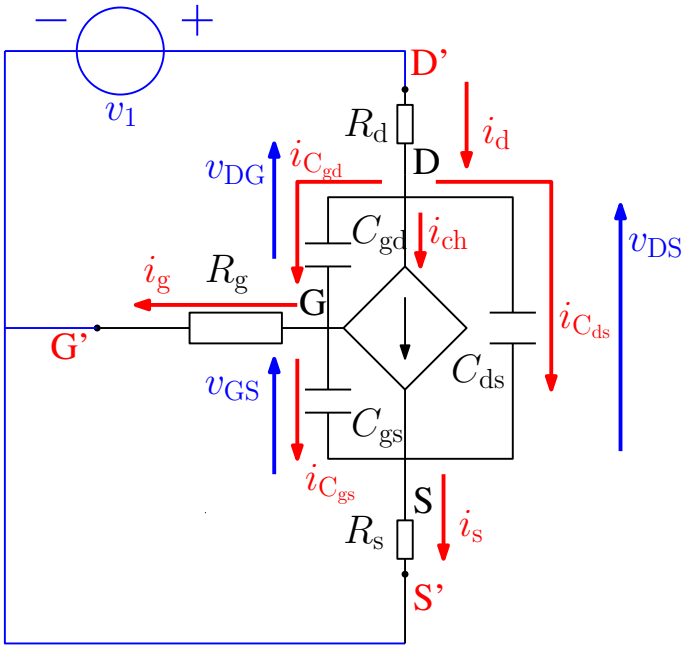


FIGURE 3.43: AC small signal model of the characterization circuit by the MCP method when power transistor in linear region

Therefore, for the presented C_{gd} measurement in Chapter 3.2.3.1, the measurement result can be expressed as $\underline{V_1}/\underline{I_{\mathrm{G}}}$.

By replacing the equations (3.28) (3.29) (3.30) into (3.31), following equations can be obtained:

$$\underline{I_{\mathrm{G}}} = \frac{\underline{V_1} - \underline{I_{\mathrm{D}}} \cdot R_{\mathrm{d}} - \underline{I_{\mathrm{G}}} \cdot R_{\mathrm{g}}}{\underline{Z_{\mathrm{C_{gd}}}}} - \frac{\underline{I_{\mathrm{G}}} \cdot R_{\mathrm{g}} - \underline{I_{\mathrm{S}}} \cdot R_{\mathrm{s}}}{\underline{Z_{\mathrm{C_{gs}}}}} \tag{3.33}$$

$$\underline{I_{\mathrm{G}}} = \frac{\underline{V_1}}{\underline{Z_{\mathrm{C_{gd}}}}} - \left(\frac{R_{\mathrm{g}}}{\underline{Z_{\mathrm{C_{gd}}}}} + \frac{R_{\mathrm{g}}}{\underline{Z_{\mathrm{C_{gs}}}}} + \frac{R_{\mathrm{s}}}{\underline{Z_{\mathrm{C_{gs}}}}} \right) \cdot \underline{I_{\mathrm{G}}} + \left(\frac{R_{\mathrm{s}}}{\underline{Z_{\mathrm{C_{gs}}}}} - \frac{R_{\mathrm{d}}}{\underline{Z_{\mathrm{C_{gd}}}}} \right) \cdot \underline{I_{\mathrm{D}}} \tag{3.34}$$

Similarly, by replacing the equations (3.27) (3.28) (3.29) (3.30) into (3.32), following equation is obtained:

$$\underline{I_{\mathrm{D}}} = \frac{\underline{V_1} - \underline{I_{\mathrm{D}}} \cdot R_{\mathrm{d}} - \underline{I_{\mathrm{G}}} \cdot R_{\mathrm{g}}}{\underline{Z_{\mathrm{C_{gd}}}}} + g \cdot \underline{I_{\mathrm{G}}} \cdot R_{\mathrm{g}} - g \cdot \underline{I_{\mathrm{S}}} \cdot R_{\mathrm{s}} + \frac{\underline{V_1} - \underline{I_{\mathrm{D}}} \cdot R_{\mathrm{d}} - \underline{I_{\mathrm{S}}} \cdot R_{\mathrm{s}}}{\underline{Z_{\mathrm{C_{ds}}}}} \tag{3.35}$$

By using $s = j\omega$ in the equations (3.34) et (3.35), following equations can be obtained:

$$sC_{\mathrm{gd}}\underline{V_1} = (1 + sC_{\mathrm{gd}}R_{\mathrm{g}} + sC_{\mathrm{gs}}R_{\mathrm{g}} + sC_{\mathrm{gs}}R_{\mathrm{s}}) \cdot \underline{I_{\mathrm{G}}} - (R_{\mathrm{s}}sC_{\mathrm{gs}} - R_{\mathrm{d}}sC_{\mathrm{gd}}) \cdot \underline{I_{\mathrm{D}}} \tag{3.36}$$

$$(sC_{\mathrm{gd}} + sC_{\mathrm{ds}}) \cdot \underline{V_1} = (R_{\mathrm{g}}sC_{\mathrm{gd}} - R_{\mathrm{s}}sC_{\mathrm{ds}} - gR_{\mathrm{g}} - gR_{\mathrm{s}}) \cdot \underline{I_{\mathrm{G}}} + (1 + sC_{\mathrm{gd}}R_{\mathrm{d}} + sC_{\mathrm{ds}}R_{\mathrm{d}} + sC_{\mathrm{ds}}R_{\mathrm{s}} + gR_{\mathrm{s}}) \cdot \underline{I_{\mathrm{D}}} \tag{3.37}$$

In the SiC JFET technical datasheet, the value of the resistor R_{g} is several ohms, while that of R_{s} is inferior to several tens of milliohms. Thus, with the hypothesis $R_{\mathrm{g}} \gg R_{\mathrm{s}}$, the above equations (3.36) and (3.37) can be simplified into the following forms:

$$sC_{\mathrm{gd}}\underline{V_1} = (1 + sC_{\mathrm{gd}}R_{\mathrm{g}} + sC_{\mathrm{gs}}R_{\mathrm{g}}) \cdot \underline{I_{\mathrm{G}}} - (R_{\mathrm{s}}sC_{\mathrm{gs}} - R_{\mathrm{d}}sC_{\mathrm{gd}}) \cdot \underline{I_{\mathrm{D}}} \tag{3.38}$$

$$(sC_{\mathrm{gd}} + sC_{\mathrm{ds}}) \cdot \underline{V_1} = (R_{\mathrm{g}}sC_{\mathrm{gd}} - R_{\mathrm{s}}sC_{\mathrm{ds}} - gR_{\mathrm{g}}) \cdot \underline{I_{\mathrm{G}}} + (1 + sC_{\mathrm{gd}}R_{\mathrm{d}} + sC_{\mathrm{ds}}R_{\mathrm{d}} + sC_{\mathrm{ds}}R_{\mathrm{s}} + gR_{\mathrm{s}}) \cdot \underline{I_{\mathrm{D}}} \tag{3.39}$$

Multiplying eq.(3.38) by $(1 + sC_{\mathrm{gd}}R_{\mathrm{d}} + sC_{\mathrm{ds}}R_{\mathrm{d}} + sC_{\mathrm{ds}}R_{\mathrm{s}} + gR_{\mathrm{s}})$ and eq.(3.39) by $(R_{\mathrm{s}}sC_{\mathrm{gs}} - R_{\mathrm{d}}sC_{\mathrm{gd}})$ and then adding the two equations, the current $\underline{I_{\mathrm{D}}}$ can be canceled in equations (3.38) and (3.39), so the equation below is thus obtained:

$$A1 \cdot \underline{I_{\mathrm{G}}} = B1 \cdot \underline{V_1} \tag{3.40}$$

R_d is supposed to be the same magnitude to R_s, so the following hypothesis can be validated:

$$\begin{aligned} &R_g \gg R_s \quad \text{and} \quad R_g \gg R_d, \\ &\text{and until 10MHz} \quad 1 \gg w^2 C_{XY} C_{XY} R_X R_Y \end{aligned} \tag{3.41}$$

where X,Y are indexes which indicates either d, g or s.

By applying this hypothesis, A1 and B1 in eq.(3.40) can be expressed in the following forms:

$$A1 = 1 + gR_s + s\left(C_{gd}R_g + 2C_{ds}R_s + C_{gs}R_g + 2gC_{gd}R_gR_s\right) \tag{3.42}$$

$$B1 = -R_s w^2 \left(C_{gd}C_{gs} + C_{gd}C_{ds} + C_{ds}C_{gs}\right) + s\left(1 + gR_s\right)C_{gd} \tag{3.43}$$

For C_{gd} measurement, the imaginary part of $\underline{V_1}/\underline{I_G}$ can be expressed by:

$$Im\left(\frac{\underline{V_1}}{\underline{I_G}}\right) = \frac{s\left(-R_s w^2 \left(C_{gd}C_{gs} + C_{gd}C_{ds} + C_{ds}C_{gs}\right)\left(C_{gd}R_g + 2C_{ds}R_s + C_{gs}R_g + 2gC_{gd}R_gR_s\right) - \left(1 + gR_s\right)^2 C_{gd}\right)}{\left(R_s w^2 \left(C_{gd}C_{gs} + C_{gd}C_{ds} + C_{ds}C_{gs}\right)\right)^2 + w^2\left(1 + gR_s\right)^2 {C_{gd}}^2} \tag{3.44}$$

By using the same hypothesis (3.41), eq.(3.44) can be simplified into:

$$Im\left(\frac{\underline{V_1}}{\underline{I_G}}\right) = \frac{1}{sC_{gd}} \tag{3.45}$$

It is shown in the above equation that when the power device is in linear region, C_{gd} measurement in the circuits presented in Figure 3.36(a) and Figure 3.37(a) is valid to characterize its values. In other words, the internal resistor R_g does not interfere with the C_{gd} measurement.

In contrast, the determination of C_{oss} is not so straightforward, as will be shown below.

For the C_{oss} measurement presented in Chapter 3.2.3.2, the measurement result can be expressed in admittance by $\underline{I_D}/\underline{V_1}$. Multiplying eq.(3.38) by $(R_g sC_{gd} - R_s sC_{ds} - gR_g)$ and multiplying eq.(3.39) by $(1 + sC_{gd}R_g + sC_{gs}R_g)$ and then subtracting the two equations, the current $\underline{I_G}$ in equations (3.38) and (3.39) can be canceled, the following equation can thus be obtained:

$$A2 \cdot \underline{I_D} = B2 \cdot \underline{V_1} \tag{3.46}$$

By applying the same hypothesis (3.41), A2 and B2 in eq.(3.46) can be expressed in the following form:

$$A2 = 1 + gR_s + s\left(C_{gd}R_g + 2C_{ds}R_s + C_{gs}R_g + 2gC_{gd}R_gR_s\right) \tag{3.47}$$

$$B2 = -R_g w^2 \left(C_{gd}C_{gs} + C_{gd}C_{ds} + C_{ds}C_{gs}\right) + s\left(C_{ds} + C_{gd} + gC_{gd}R_g\right) \tag{3.48}$$

For C_{oss} measurement, by using the same hypothesis (3.41), the imaginary part of the measurement can be expressed in the following relation:

$$Im\left(\frac{\underline{I_D}}{\underline{V_1}}\right) = \frac{C_{ds} + C_{gd} + gR_gC_{gd}}{1 + gR_s} \tag{3.49}$$

Unlike C_{gd} measurement, it is shown in the above relation that when the power device is in linear region, the measured C_{oss} values by the circuit shown in Figure 3.38(a) no longer equals to $C_{oss} = C_{ds} + C_{gd}$. In fact, power transistor dynamic transconductance g and its internal gate resistance R_g will increase the apparent capacitance values by a term $g \cdot R_g \cdot C_{gd}$, which reveals the influence of the internal gate resistance on measurement results.

3.2.4.2 Single-pulse characterization circuit modeling

It is presented in Chapter 3.2.3.2 that the difference of the current I_D values at one V_{DS} voltage (Figure 3.40(b)) is probably due to the charge and discharge of the C_{oss} capacitance at pulse-on and pulse-off. It is presented in Figure 3.44 the SiC JFET characterization circuit by single-pulse method, in which R_g, R_d and R_s are included in the power device model. It is illustrated by red lines in Figure 3.44 the direction of each electrical variable during the pulse-on, which corresponds to $dV_{DS}/dt > 0$ with the indicated trajectory in Figure 3.40(b). It is illustrated by blue lines in Figure 3.44 the direction of each electrical variable during the pulse-off, which corresponds to $dV_{DS}/dt < 0$ with the indicated trajectory in Figure 3.40(b).

It is shown in Figure 3.44 that during pulse-on, C_{gd} charge current $I_{C_{gd}}$ passes through R_g, which induces a voltage V_{R_g} across R_g; source current I_S passes through R_s, which induces a voltage V_{R_s} across R_s. Thus, during the pulse-on, the voltage V_{GS1} can be calculated by the following equation:

$$V_{GS1} = V_G + I_{G1}R_g - I_{S1}R_s \tag{3.50}$$

The similar analysis can be applied in pulse-off process, thus during the pulse-off, the voltage V_{GS2} can be calculated by:

$$V_{GS2} = V_G - I_{G2}R_g - I_{S2}R_s \tag{3.51}$$

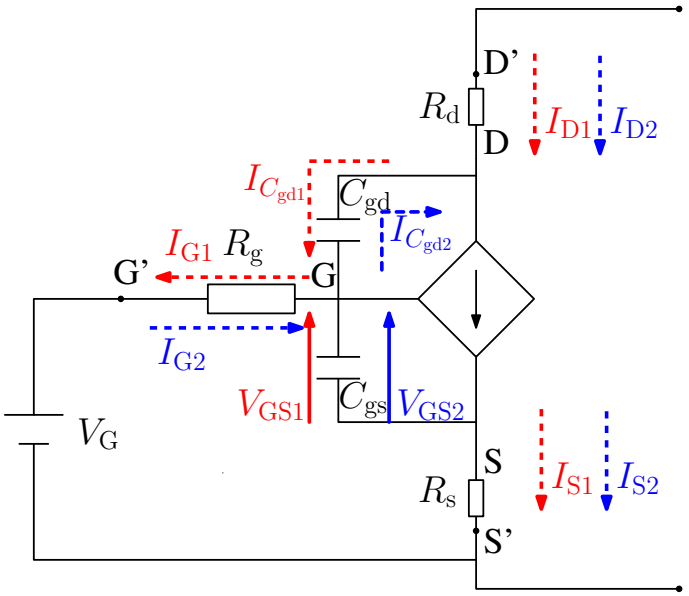


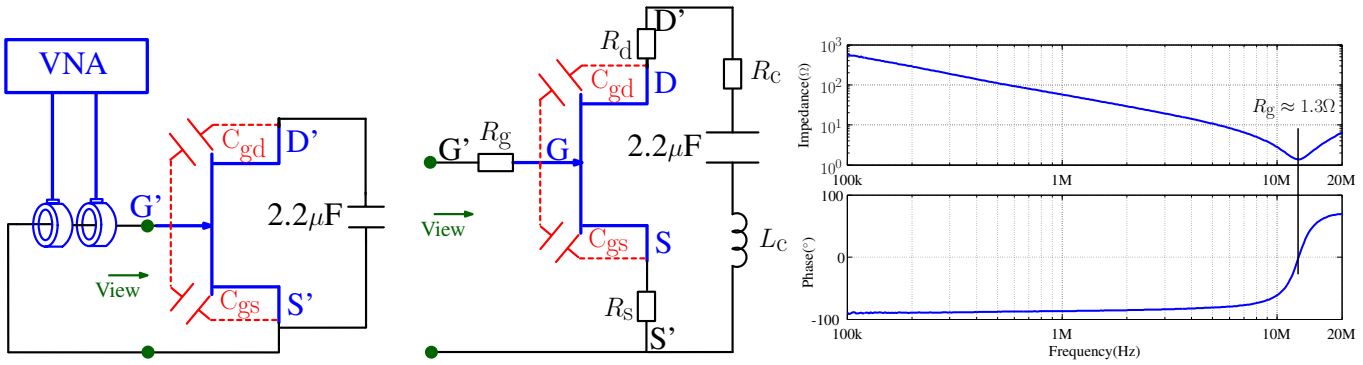
FIGURE 3.44: SiC JFET characterization by single-pulse method with R_g, R_d and R_s

It is shown in the equations (3.50) and (3.51) that because of the R_g and R_s resistances, V_{GS} is no longer the imposed voltage V_G during the characterization. By applying the measurement data in Figure 3.40(b), it can be verified that $V_{GS1} > V_{GS2}$ during the characterization. Thus, the difference of the drain current in Figure 3.40(b) is partly due to this V_{GS} voltage difference and not due to the surge increase of C_{ds} capacitance values.

It is shown in this section and the previous one that both R_g and R_s resistances have influence on the obtained capacitance values, thus it is necessary to estimate their values, which is presented in the next section.

3.2.4.3 R_g and R_s estimation

The SiC JFET R_g resistance can be estimated with the measurement circuit shown in Figure 3.45(a) by the MCP method, of which is the same principle presented in Chapter 2.2.1 for C_{iss} measurement. When the SiC JFET is blocked, the power device can be represented by the equivalent circuit shown in Figure 3.45(b), in which the 2.2μF external capacitor is modeled by its capacitance in series with the equivalent series resistance (ESR) R_c and the equivalent series inductance (ESL) L_c. As R_g is the biggest resistance and it is much bigger than R_s, its value is characterized in the results shown in Figure 3.45(c), in which it is represented by the resonance point. Thus, its value can be estimated about 1.3Ω.



(a) Measurement circuit (b) Equivalent circuit when SiC JFET is blocked (c) Measurement result

FIGURE 3.45: Measurement circuit to determine R_g value

There is also a term $1 + gR_s$ in the denominator of the eq.(3.49), so it is necessary to estimate R_s value to quantify its influence on the measurement results. For this reason, its superior boundary is calculated by the following method. First, according to the power device model presented in Figure 3.44, the obtained V_G-I_D curve in the measurement is an apparent transconductance g', in which V_G is altered by the term $I_D \cdot R_s$ that is illustrated in Figure 3.46.

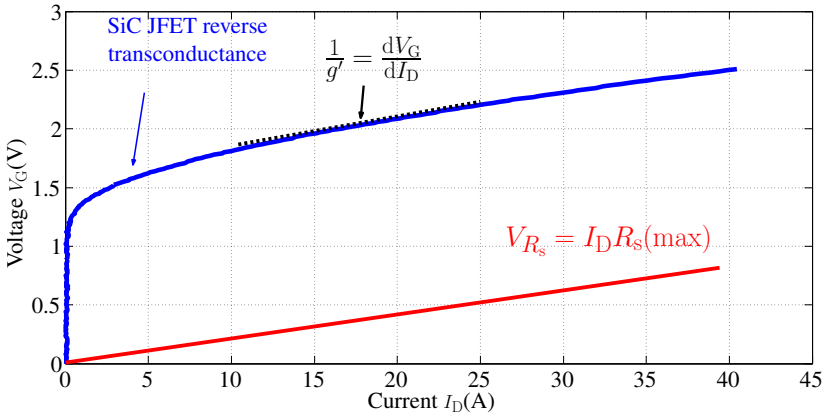


FIGURE 3.46: The method to estimate SiC JFET R_s resistance

Nevertheless, as shown in Figure 3.46, R_s can not be superior to reverse apparent dynamic transconductance: $\frac{1}{g'} = \frac{dV_G}{dI_D}$. Otherwise, the real power device dynamic transconductance $g = \frac{dI_D}{dV_{GS}}$ obtained from:

$$\frac{1}{g} = \frac{dV_{GS}}{dI_D} = \frac{dV_G}{dI_D} - R_s = \frac{1}{g'} - R_s, \tag{3.52}$$

is inferior to 0, which means an impossible negative dynamic transconductance is obtained. Therefore, it is necessary that R_s is inferior to $\left(\frac{dV_G}{dI_D}\right)_{min}$, which is about 14 milliohms in this case. As a consequence, it can be stated that $R_g >> R_s$.

The estimated R_g and R_s values are used in the following paragraphs to validate the characterization results.

3.2.4.4 R_g influence on characterization results

By MCP method

As shown in eq.(3.45), C_{gd} capacitance measurement results are not influenced by the R_g resistance when the SiC JFET is in linear region.

With the measured C_{gd} capacitance values, the apparent "Coss" capacitance values can be calculated according to the eq.(3.49) and then compared to the measurement. The R_s value in eq.(3.49) can be varied from its minimal value 0Ω to its estimated maximal value $14m\Omega$ in Chapter 3.2.4.3, by which the calculation result of eq.(3.49) can reach its maximal value and minimal value correspondingly. Because of the SiC JFET internal structure, $C_{ds} = 0$ is imposed in eq.(3.49). The calculation results are compared with the measured apparent "Coss" capacitance values in Figure 3.47.

It is shown in Figure 3.47 that the measured apparent "Coss" capacitance values are between the minimal and maximal calculation result of the eq. (3.49). Therefore, when the power device in linear region, the surge increase of the "Coss" capacitance values is certainly due to the influence of gR_g on the measurement and not due to an increase of the C_{ds} capacitance values.

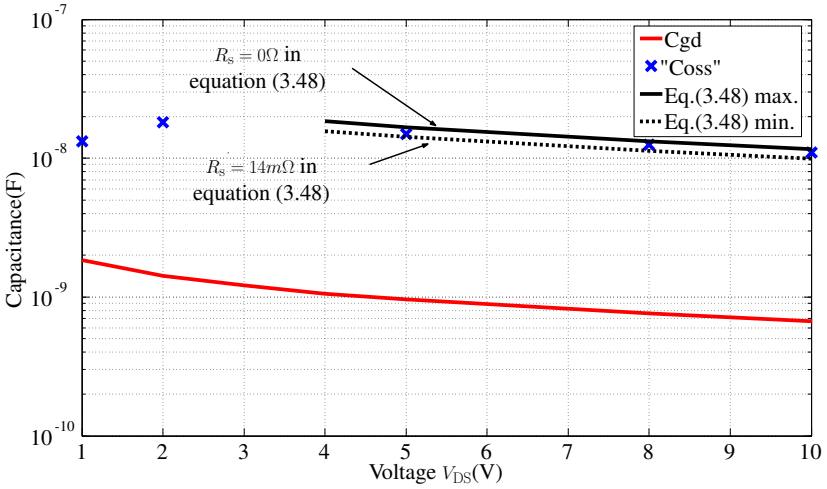


FIGURE 3.47: Apparent "Coss" capacitance measurement results when the SiC JFET in linear region ($V_{GS} = 1.4V$)

By single-pulse method

To validate the influence of R_g on the current I_D difference observed in Figure 3.40(b), a SiC JFET behavior model presented in Figure 3.28 together with a gate resistor R_g is used in the simulation circuit shown in Figure 2.1. The comparison between the simulation and the measurement results on channel static characteristic has been presented in Figure 3.31(a). The equation (3.53) is used to express C_{gd} capacitance values when the SiC JFET is in linear region with $0V \leq V_{GS} \leq 2V$. The parameters[6]are obtained by the fitting method: $a = 8.24\times10^3, b = 0.7625, c = 1.12, d = 1.5\times10^2, e =$

[6]The units of these parameters are a(pF), d(pF), b(V), e(V^{-1}) and c without unit.

0.0021. The comparison between the model and the measurement is shown in Figure 3.48. In the simulation, SiC JFET is polarized with $V_{\mathrm{GS}} = 1.4V$.

$$C_{\mathrm{rss}} = \frac{a}{1 + \left(\frac{V_{\mathrm{DS}} - V_{\mathrm{GS}} + 2}{b}\right)^{c}} + d \cdot exp\left(-e \cdot (V_{\mathrm{DS}} - V_{\mathrm{GS}} + 2)\right) \tag{3.53}$$

It is presented in Figure 3.49(a) that the presented power device model reproduces almost the same current difference ΔI_{D} at one V_{DS} voltage during the current rising and falling. It is shown in this result that ΔI_{D} is principally due to the ΔV_{GS} variation during the characterization. However, it is observed in Figure 3.49(a) that when $V_{\mathrm{DS}} = 10V$, the difference between the measurement and model is about $\frac{\Delta I_{mes.}}{\Delta I_{model}} = 1.2$ while when $V_{\mathrm{DS}} = 5V$, this difference is about $\frac{\Delta I_{mes.}}{\Delta I_{model}} = 1.38$. As $\Delta I_{\mathrm{D}} \propto g$, this difference between the model and the measurement is principally due to their difference on dynamic transconductance. Indeed, small differences are likely to occur between the static characterization dataset and the fitting functions, because I-V curves are first fitted for each V_{GS}, and then the obtained parameters are fitted as functions of V_{GS}.

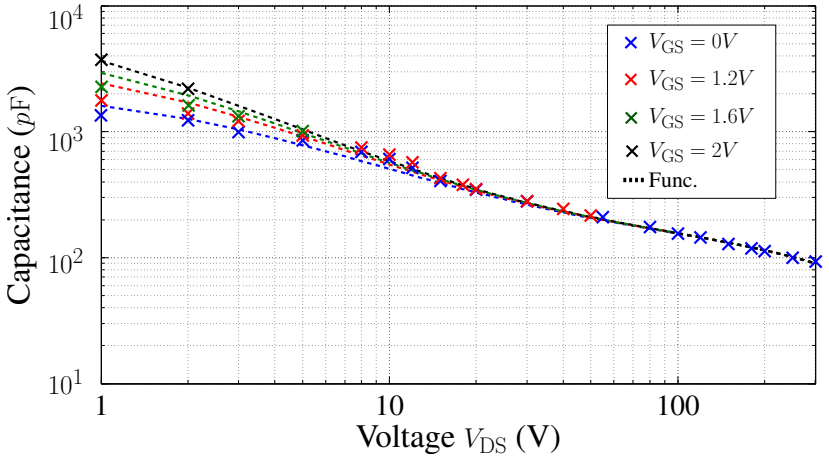
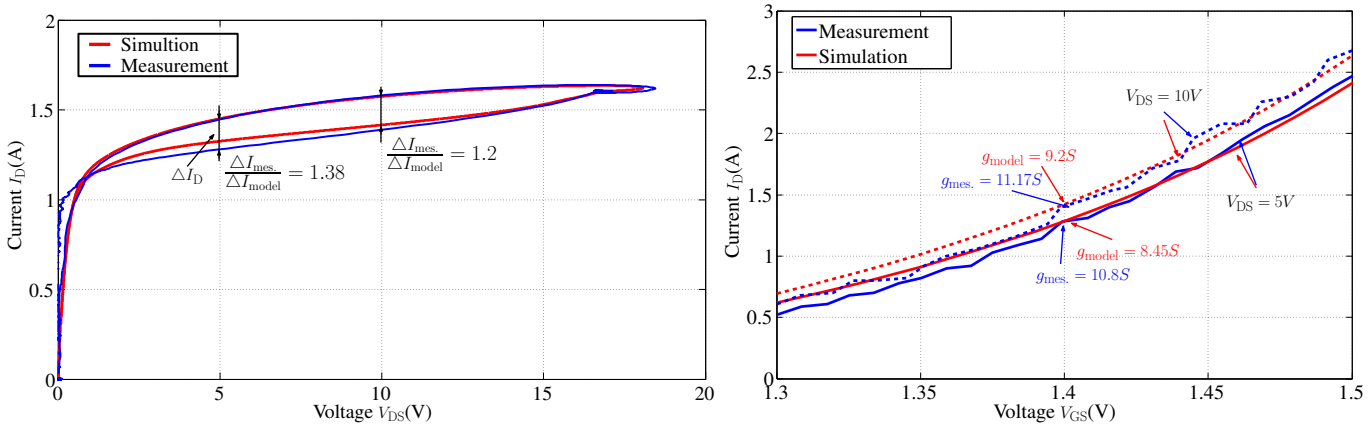


FIGURE 3.48: Comparison between the model and measurements of C_{gd} capacitance values of SiC JFET in linear region

It is presented in Figure 3.31(a) that the current I_{D} increases slowly when the power device is in linear region, so the obtained transconductance at different V_{DS} voltages might be different. It is compared in Figure 3.49(b) the SiC JFET dynamic transconductance between the model and the measurement when $V_{\mathrm{DS}} = 5V$ and $V_{\mathrm{DS}} = 10V$. When $V_{\mathrm{GS}} = 1.4V$ and $V_{\mathrm{DS}} = 10V$, the dynamic transconductance difference between the model and the measurement is about $\frac{\Delta g_{mes.}}{\Delta g_{model}} = \frac{11.17}{9.2} = 1.21$; while for $V_{\mathrm{GS}} = 1.4$V, and $V_{\mathrm{DS}} = 5V$, this difference is about $\frac{\Delta g_{mes.}}{\Delta g_{model}} = \frac{10.8}{8.45} = 1.28$. Thus, the difference of ΔI_{D} in Figure 3.49(a) is mainly due to the different dynamic transconductance values between the model and the measurement.



(a) Comparison in I_D-V_{DS} at $V_{GS} = 1.4V$ (b) Transconductance difference

FIGURE 3.49: Comparison of I_D-V_{DS} and dynamic transconductance between the model and the measurement of SiC JFET at $T_j = 25°C$

It is presented in the above results the influence of the R_g resistance on characterization results by single-pulse method. The results in this section reveal that the increase of the apparent C_{oss} capacitance values when the power device in linear region is due to the internal gate R_g resistance. This resistance can vary V_{GS} voltage during the characterization, thus increase the C_{oss} capacitance values.

3.2.4.5 C_{iss} measurement results

The measurement circuit to characterize C_{iss} when the power device in linear region is shown in Figure 3.50(a), which is similar to the classical two-current-probe method for the measurement of one impedance.. A 2.2μF capacitor is connected between G and S to block V_{GS} DC voltage and a second capacitor of the same value is connected between D and S to make a short circuit in AC. The measurement AC current injected by the CIP is illustrated by the red line in Figure 3.50(a), with this configuration, apparent C_{iss} capacitances values can be measured.

Similar to the modeling method of C_{rss} and C_{oss} measurement presented in Chapter 3.2.4.1, the AC small signal model of the equivalent C_{iss} measurement circuit is presented in Figure 3.50(b).

Following equations can be obtained from Figure 3.50(b).

$$\underline{V_{DS}} = \underline{I_D} \cdot R_d - \underline{I_S} \cdot R_s \tag{3.54}$$

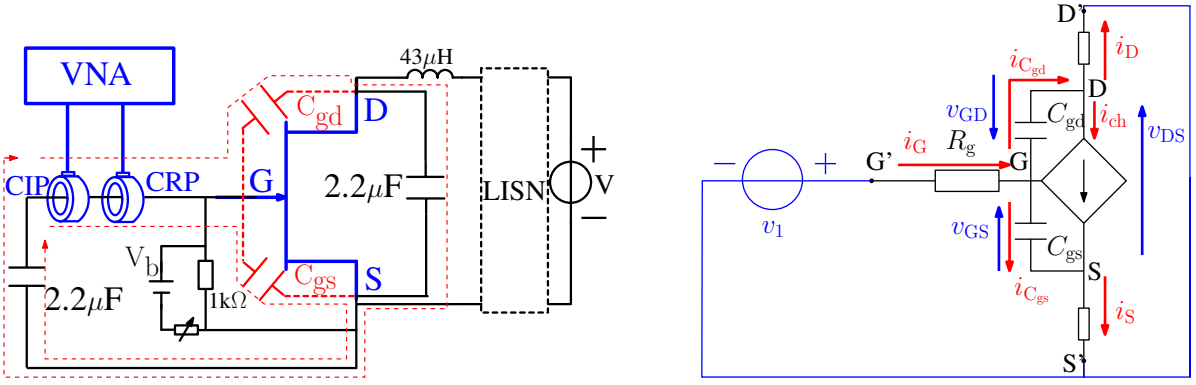
$$\underline{V_{GD}} = \underline{V_1} - \underline{I_D} \cdot R_d - \underline{I_G} \cdot R_g \tag{3.55}$$

$$\underline{V_{GS}} = \underline{V_1} - \underline{I_G} \cdot R_g - \underline{I_S} \cdot R_s \tag{3.56}$$

$$\underline{I_{\mathrm{G}}} = \underline{I_{\mathrm{S}}} + \underline{I_{\mathrm{D}}} \tag{3.57}$$

$$\underline{I_{\mathrm{D}}} = \frac{\underline{V_{\mathrm{GD}}}}{\underline{Z_{\mathrm{C_{gd}}}}} - g \cdot \underline{V_{\mathrm{GS}}} \tag{3.58}$$

$$\underline{I_{\mathrm{S}}} = \frac{\underline{V_{\mathrm{GS}}}}{\underline{Z_{\mathrm{C_{gs}}}}} + g \cdot \underline{V_{\mathrm{GS}}} \tag{3.59}$$



(a) C_{iss} measurement circuit

(b) AC small signal model of measurement circuit

FIGURE 3.50: C_{iss} measurement circuit and its AC small signal model

For the C_{iss}, the measurement result can be expressed by $\underline{V_1}/\underline{I_{\mathrm{G}}}$. With the similar calculation method presented in Chapter 3.2.4.1, following equation can be obtained:

$$A1 \cdot \underline{I_{\mathrm{G}}} = B1 \cdot \underline{V_1}. \tag{3.60}$$

By applying the same hypothesis (3.41), A1 and B1 in eq.(3.60) can be expressed in the following form:

$$A1 = 1 + gR_{\mathrm{s}} + s\left(C_{\mathrm{gd}}R_{\mathrm{g}} + C_{\mathrm{gs}}R_{\mathrm{g}} + 2gC_{\mathrm{gd}}R_{\mathrm{g}}R_{\mathrm{s}}\right) \tag{3.61}$$

$$B1 = -2R_{\mathrm{s}}w^2C_{\mathrm{gd}}C_{\mathrm{gs}} + s\left(C_{\mathrm{gd}} + C_{\mathrm{gs}} + 2gR_{\mathrm{s}}C_{\mathrm{gd}}\right) \tag{3.62}$$

For C_{iss} measurement, by using the same hypothesis (3.41), the imaginary part can be expressed by:

$$Im\left(\frac{V_1}{\underline{I_G}}\right) = \frac{1}{sC_{\text{mes}}}, \tag{3.63}$$

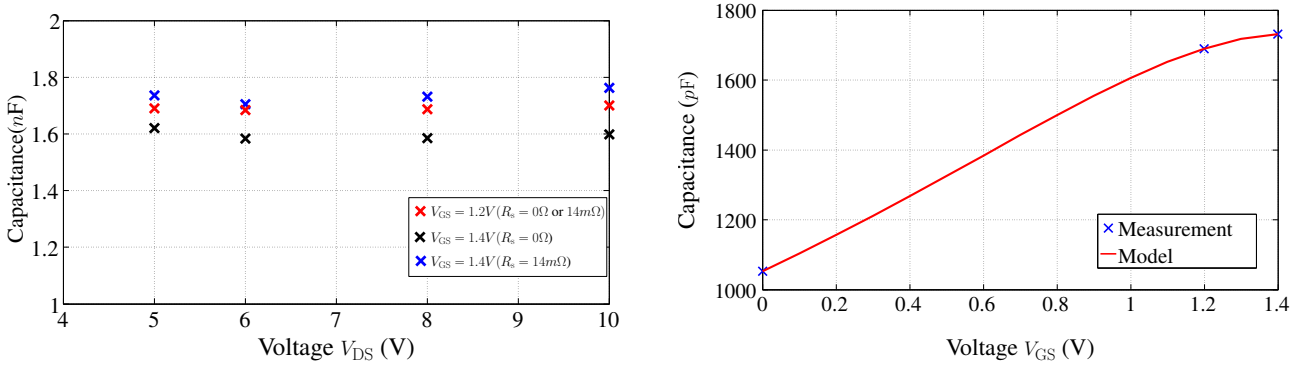
where C_{mes} in eq(3.63) is expressed by the following form:

$$C_{\text{mes}} = \frac{C_{\text{gs}} + C_{\text{gd}} + 2gR_{\text{s}}C_{\text{gd}}}{1 + gR_{\text{s}}}, \tag{3.64}$$

It is presented in eq.(3.64) that gR_{s} can interfere the measurement results, and no more $C_{\text{iss}} = C_{\text{gs}} + C_{\text{gd}}$ is measured by the circuit shown in Figure 3.50(a). C_{gs} values can then be obtained by the following relation:

$$C_{\text{gs}} = (1 + gR_{\text{s}})\, C_{\text{mes}} - (1 + 2gR_{\text{s}})\, C_{\text{gd}}. \tag{3.65}$$

When $V_{\text{GS}} = 1.2V$ and $1.4V$, the obtained C_{gs} values are shown in Figure 3.51(a), in which R_{s} in eq.(3.65) equals to 0Ω and its estimated maximal 0.014Ω in Chapter 3.2.4.3.



(a) C_{gs} measurement results

(b) C_{gs} model and measurement

FIGURE 3.51: C_{gs} measurement results and its model in linear region

It is shown in Figure 3.51(a) that when $V_{\text{GS}} = 1.2V$, R_{s} value does not influence the obtained C_{gs} values, because the transconductance g is still quite low at this voltage. However, when $V_{\text{GS}} = 1.4V$, when $R_{\text{s}} = 0\Omega$, the obtained C_{gs} values are slightly smaller than its values when $V_{\text{GS}} = 1.2V$, the result of which is not reasonable, because C_{gs} represents the junction capacitance of the diode D_{GS}. When $R_{\text{s}} = 0.014\Omega$, it is shown in the result that the obtained C_{gs} values are bigger than its values when $V_{\text{GS}} = 1.2V$, the result of which is more reasonable.

The capacitance C_{gs} can then be modeled with the equation (3.66) in linear region ($0V \leq V_{\text{GS}} \leq 1.4V$). The parameters a, b, c are obtained by fitting method[7]: $a = 1731, b = 1.82, c = 1.685$. The comparison between the model and the measurement is shown in Figure 3.51(b).

$$C_{\text{gs}} = \frac{a}{1 + \left(\frac{1.4 - V_{\text{GS}}}{b}\right)^c} \tag{3.66}$$

A SiC JFET behavior model is presented in this section and the model will be validated in Chapter 4 to compare with the measurement on power device switching waveforms.

3.3 Discussion

It is presented in this chapter, the power device behavior models which are based on the characterization results. There are the following issues which are necessary to be discussed.

Diode behavior models

As presented in Chapter 3.1.2, when diode is in conduction, even $5n$H parasitic inductance L_{para} inside the packaging makes that it is impossible to precisely characterize diode capacitance values, which will in theory influence the precision of the presented behavior model. To resolve this problem, an active negative inductor can be considered to be used in the characterization circuit to compensate both the L_{para} values and the inductive impedance of Z_{setup} values in the measurement configuration. Different negative inductor circuits (NIC) have been presented by authors in [122]. The principle of the NIC can be illustrated in the following figure.

From the circuit in Figure 3.52, following equations can be obtained:

$$v_{\text{in}} - v_{\text{o}} = i_{\text{in}} \cdot R_1 \tag{3.67}$$

$$\frac{v_{\text{in}}}{R_2} = \frac{v_{\text{o}} - v_{\text{in}}}{Z_{\text{C}}} \tag{3.68}$$

Combining eq.(3.67) (3.68) to cancel v_{o} in the two equations, the following equation can be obtained:

$$\frac{v_{\text{in}}}{i_{\text{in}}} = -\frac{R_1 \cdot R_2}{Z_{\text{C}}} = -j\omega R_1 R_2 C \tag{3.69}$$

[7]The units are: $a(p\text{F})$, $b(\text{V})$ and c without unit.

Thus, a negative inductor with $-R_1R_2C$ inductance is created in such a way.

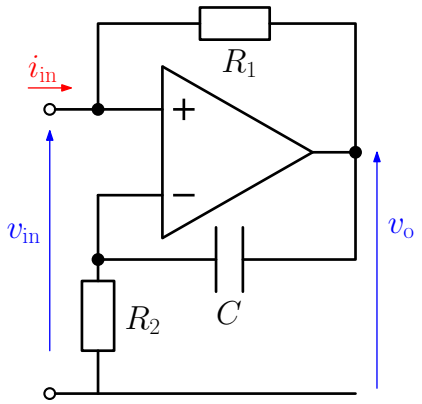


FIGURE 3.52: Negative inductor circuit principle

It is presented a parameter α in Chapter 3.1.3 to determine the $R_{1,real}$ and $R_{2,real}$ repartition values when diode is in conduction. It is to be noted that the choice of the α is able to improve the behavioral model. More details about the α value will be presented in Chapter 4.1.

Power transistor behavior model

1. When the power device inter-electrodes capacitances are characterized in linear region, it is important to control T_j. As the characterization is done in ON-state, maximal power dissipation is limited to 60W in our measurement configuration. In order to characterize power device on high V_{DS} voltage in linear region by the proposed MCP method, it is necessary to cool down the measurement system. For that means, it is necessary to synchronize the measurement system (VNA) with the pulse generator. A measurement configuration based on the synchronization can be illustrated in Figure 3.53.

   At step 1, power device V_{GS} voltage is trigged on and power device is from the blocking point to the linear region as illustrated in Figure 2.41(b). When current I_D is stabilized, a trigger on signal is sent to the VNA to characterize the power device which has been polarized in one DC point in linear region at step 2. When the measurement is finished by VNA, a signal is sent to the control unit (step 3) in order to turn-off the power device at step 4. By setting the length of the pulse, T_j can be controlled.

2. It is shown in eq.(3.49) that the apparent C_{oss} capacitance values are increased by the term gR_gC_{gd}, which is much bigger than C_{ds} capacitance values in theory. For the power transistors in which there is a C_{ds} inter-electrode capacitance, its values in linear region can hardly be correctly characterized by the proposed method due to the propagation error by the subtraction of gR_gC_{gd} in eq.(3.49). However, the proposed method can still be a reference to compare with other measurement methods.

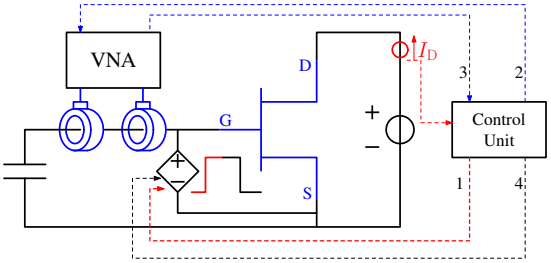


FIGURE 3.53: Measurement system synchronization

3.4 Conclusions

It is presented in this chapter the behavioral models of a power diode and a SiC JFET, which are simulated in PSPICE. The power diode behavioral model is based on its dynamic impedance measurement, in which its impedance at one DC polarization point is measured by the previously presented two-current-probe method. The obtained dynamic resistances values are then converted into their static resistances values, which are further expressed by mathematical functions to be used in the simulation software.

The SiC JFET behavior model to represent its static characteristic is based on the characterization results by single-pulse method presented in Chapter 2. The model to represent its dynamic characteristic is based on the inter-electrode capacitances characterization results obtained by the multiple-current-probe (MCP) method presented in Chapter 2, in which power device inter-electrode capacitances are characterized not only when the device are blocked, but also in linear region. The measurement results by the MCP method has been validated by either impedance analyzer or by single-pulse characterization system. It is shown in the measurement results that when the power device is blocked, C_{oss} values equal to C_{rss} values, but when in linear region, the obtained apparent C_{oss} values is ten times bigger than C_{rss} values.

To further investigate this issue, internal gate resistor R_{g}, drain resistor R_{d} and source resistor R_{s} are included in the power device model. The obtained results show that R_{g} can vary V_{GS} voltages during the characterization, thus increase the characterized C_{oss} capacitance values. Similar like diode modeling, both power device static and dynamic characteristics are represented by different mathematical functions in the model.

The presented power device models in this section are to be validated with the measurement on switching waveforms in the next chapter.

Chapter 4

Experimental Validations

In this chapter, at first, the simulation of the presented diode behavior models in Chapter 3 are compared with the measurement on diode reverse recovery current in different $\mathrm{d}i/\mathrm{d}t$ switching conditions.

Then, in order to validate the proposed SiC JFET model of Chapter 3 on different switching conditions, it is necessary to measure fast switching current. Therefore, using a current surface probe (CSP) to measure switching current of a few nanoseconds is studied. The advantage of the CSP is with small insertion impedance and high bandwidth. In order to validate its use, specific PCB tracks and power converters are designed in order to compare it with other current measurement equipments.

Afterwards, the simulation of the SiC JFET behavior model is compared with the measurement on I_{D} switching current and V_{DS} switching voltage in different $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ conditions, where the switching current is measured by the presented CSP.

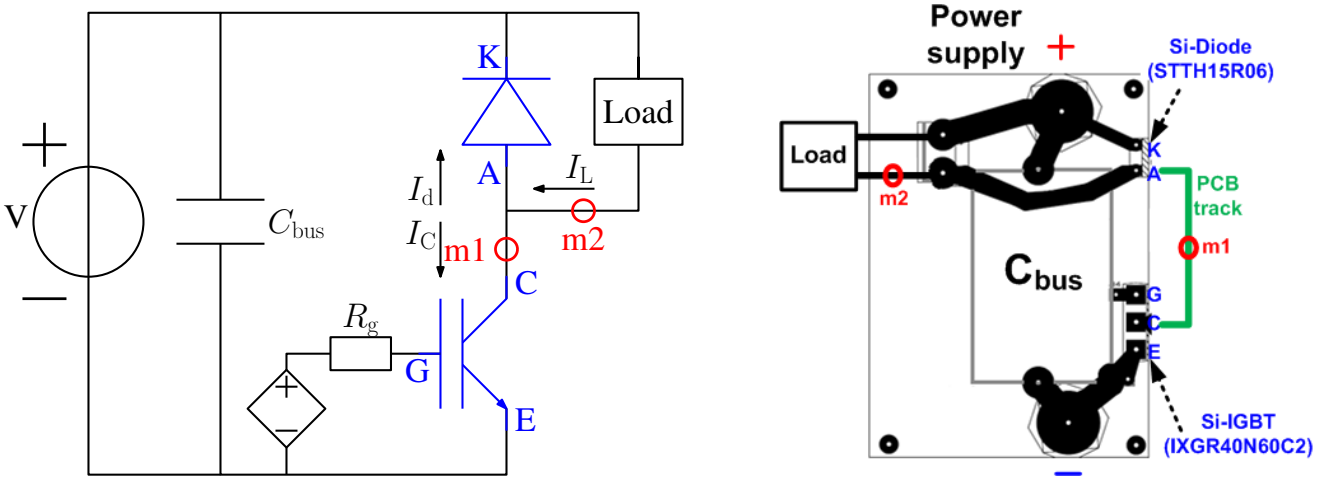
Several issues on those experiment results will be discussed and a brief conclusion will be presented at last.

4.1 Diode Models Validation

In this section, the diode switching mesh will be presented and modeled at first, then diode switching current in different commutation conditions between the simulations and the measurement results will be compared.

4.1.1 Experimental setup

A buck converter shown in Figure 4.1(a) is used to measure diode switching current. It is mainly constituted by a DC bus capacitor C_{bus}, a series R-L load, a Si IGBT (IXGR40N60C2) with its driver and the studied Si diode (STTH15R60). The PCB of the power circuit is shown in Figure 4.1(b). IGBT collector current I_{C} and load current I_{L} are measured by an active Hall effect current probe (HECP) (Lecroy CP030, DC-50MHz). The measurement points are indicated as "m1" and "m2" in Figure 4.1. Diode current I_{d} can be obtained by $I_{\text{d}} = I_{\text{L}} - I_{\text{C}}$. The bandwidth of the 12-bit measurement oscilloscope is 600MHz. The different components of the circuit will be modeled by electrical equivalent circuit from 1kHz-100MHz.



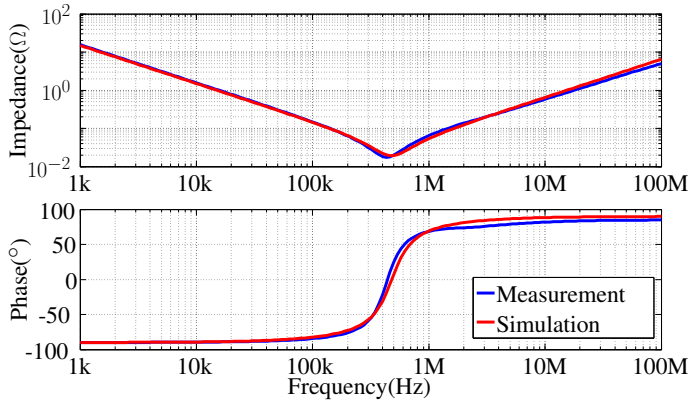
(a) Experimental setup circuit

(b) PCB of power circuit

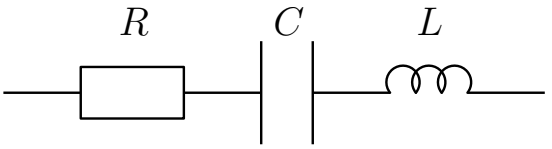
FIGURE 4.1: Experimental setup circuit to study the diode switching

The impedance of the above passive components is first measured with an impedance analyzer (HP4294A, 40Hz-110MHz). The measurement results of the C_{bus} is shown in Figure 4.2(a). It can be represented by the equivalent circuit shown in Figure 4.2(b), in which R represents its equivalent series resistance (ESR) value, C represents its capacitance value and L represents its equivalent series inductance (ESL) value. The values of R, C and L can be obtained by the fitting method: $R = 19m\Omega, C = 10.6\mu\text{F}, L = 10n\text{H}$. The simulation results of the C_{bus} is compared with the measurement data in Figure 4.2(a), in which it is shown that the model represents well the capacitor impedance.

The impedance measurement results of the R-L load is shown in Figure 4.3(a). It can be represented by the equivalent circuit shown in Figure 4.3(b). The values of each parameter is shown in Table 4.1, which is obtained by the fitting method. The simulation results of the load is compared with the measurement in Figure 4.3(a), in which it is shown that the model represents well with the measurement. It is to be noted that this is a HF equivalent circuit of the load, and the load is basically constituted by a 4.3Ω resistor R_{L} and a 158μH inductor L_{L}.

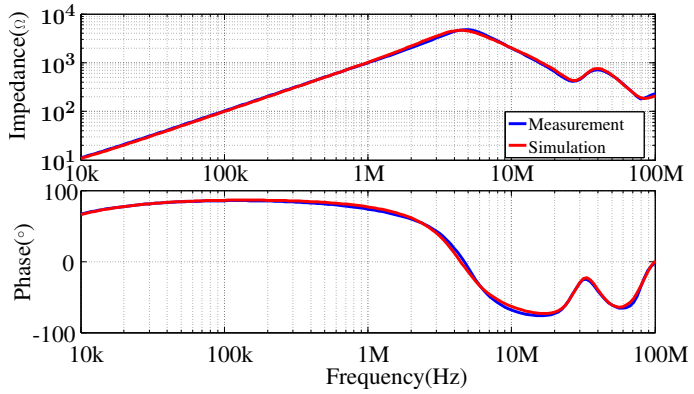


(a) Measurement and simulation results

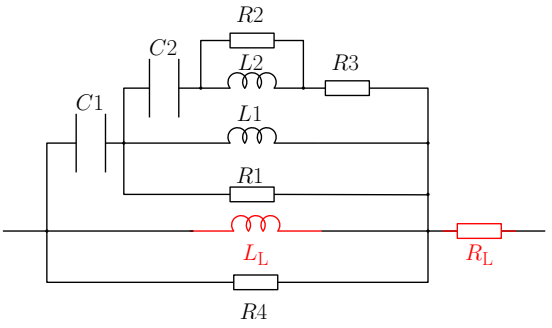


(b) Electrical equivalent circuit

FIGURE 4.2: C_{bus} measurement and simulation results



(a) Measurement results



(b) Model

FIGURE 4.3: Load simulation and measurement results

TABLE 4.1: Parameters of the load model given in Figure 4.3(b)

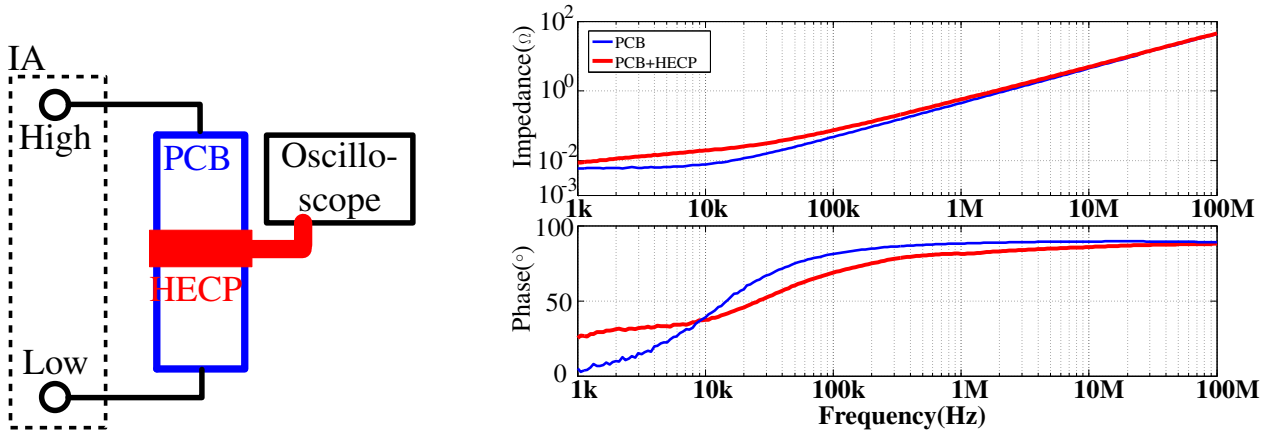
$R_{\text{L}}(\Omega)$	$L_{\text{L}}(\mu\text{H})$	$R1(\Omega)$	$L1(\mu\text{H})$	$C1(p\text{F})$	$L2(\mu\text{H})$	$R2(\Omega)$	$C2(p\text{F})$	$R3(\Omega)$	$R4(\Omega)$
4.3	158	849	2.12	8	1.23	1880	5.47	40.76	4620

The measured parasitic resistance R_{para} and the parasitic inductance L_{para} of the PCB track connecting diode anode and IGBT collector, which is indicated as "PCB track" in Figure 4.1(b), are $11m\Omega$ and $44n$H respectively.

4.1.2 Current probes characterization

It is presented in Chapter 1.6.2 that the use of the HECP brings an insertion impedance in the measurement circuit. This insertion impedance may influence the measured switching current waveform. Therefore, the insertion impedance of the used HECP is measured as illustrated in Figure 4.4(a). At first, the impedance of a PCB is measured with the IA; after that, HECP is clamped on the PCB, and it is connected to the oscilloscope to have the power supply because it is an active probe; then the impedance of the whole measurement configuration is measured. The impedance measurement

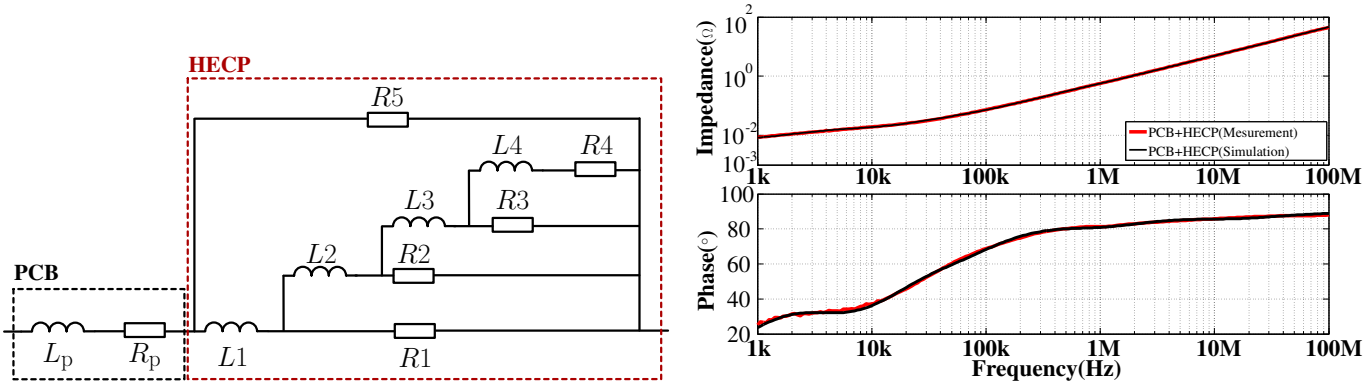
results of both the PCB and the HECP with PCB are compared in Figure 4.4(b), in which it is shown that there is an obvious influence of the HECP insertion impedance on the measurement circuit before 10MHz.



(a) Measurement circuits (b) Measurement results

FIGURE 4.4: HECP insertion impedance measurement circuit and results

Based on the above measurement result, an equivalent circuit, which is shown in Figure 4.5(a), can be used to model the HECP insertion impedance measurement results. The parameters are obtained by fitting method and they are given in Table 4.2. The comparison of the simulation and the measurement result is shown in Figure 4.5(b), in which it is shown that the presented equivalent circuit represents well the measurement. Once the presented HECP is used to measure power device current, its equivalent circuit shown in Figure 4.5(a) is added in the simulation circuit.



(a) HECP model (b) Comparison between the model and the measurement

FIGURE 4.5: HECP model and comparison between the simulation and the measurement

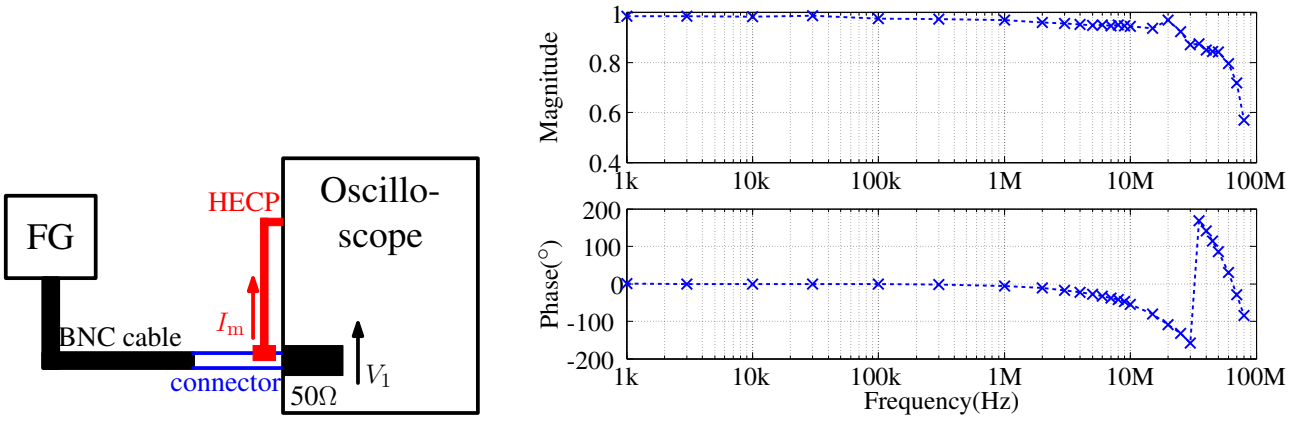
As shown in the HECP technical manual, the bandwidth of the HECP is 50MHz. Thus, there is a transfer function between the real current and the HECP measurement current, which reveals the attenuation of the measured current by the HECP. However, this transfer function is not usually given by constructors. Even it can be found in some technical manuals, there is usually only magnitude values, but phase values are hardly found. In order to have a complex current probe transfer function

and to quantify the influence of the HECP attenuation on measured current, the following method is used to obtain HECP transfer function.

TABLE 4.2: Parameters of the HECP model given in Figure 4.5(a)

$R_p(m\Omega)$	$L_p(n\text{H})$	$R1(m\Omega)$	$L1(n\text{H})$	$R2(m\Omega)$	$L2(n\text{H})$	$R3(m\Omega)$	$L3(n\text{H})$	$R4(m\Omega)$	$L4(n\text{H})$	$R5(m\Omega)$
6.2	72.6	139	11.2	25	24	14	118.7	0.8	436	910

The measurement configuration is shown in Figure 4.6(a), in which it is mainly constituted by a function generator (FG), an oscilloscope and a BNC cable with a connector. The FG and the oscilloscope are connected by the BNC cable, and the termination resistance of the oscilloscope is set to be 50Ω. FG generates an AC signal at one frequency, and the HECP is clamped on the connector to measure the generated current value (I_m).



(a) Measurement configuration

(b) Measurement result

FIGURE 4.6: HECP attenuation measurement configuration and result

At the same time, the generated real current value (I_{real}) can be calculated by its induced voltage across the oscilloscope termination resistor 50Ω: $I_{real} = \frac{V_1}{50}$. Thus, at one frequency, the HECP attenuation can be obtained by the following relation:

$$\text{Attenuation} = \frac{I_m}{I_{real}} \tag{4.1}$$

By varying the generated AC current frequency, the HECP attenuation at different frequency can be obtained. The FG in the measurement is an Agilent 33250A, with a maximal generated function frequency of 80MHz. The generated sinusoidal voltage amplitude at each frequency is 5V. The measured magnitude and phase of the HECP attenuation is shown in Figure 4.6(b). It can be seen in the measurement result that at 50MHz, HECP attenuation is about 0.8 and at 80MHz, it falls down to about 0.6. It is also shown in Figure 4.6(b) that at about 30MHz, there is a phase shift from -180° to 180° of the measured attenuation. This is due to the delay between the HECP and the

oscilloscope, which means the delay between I_{m} and V_1 including propagation time into the HECP cable.

It is necessary to include HECP attenuation to correct the obtained diode switching simulation current. Therefore, the measured HECP attenuation is represented by two simple functions. The first function F1 shown in eq.(4.2) is based on the transfer function of a first-order RC filter, in which parameter τ represents the signal delay. The two parameters τ and ω_p can be obtained by the fitting method: $\tau = 9.7 \times 10^{-9}$(s), $\omega_p = 4.4 \times 10^{8}$(Hz). The comparison between F1 and the measurement is shown in Figure 4.7. It can be seen that F1 represents well the measured attenuation up to 70MHz. Above 70MHz, the measurement attenuates bigger than F1, which suggests that the measured HECP transfer function above 70MHz attenuates by more than first order.

$$F1 = \frac{exp\left(-\tau \cdot j\omega\right)}{1 + j\frac{\omega}{\omega_p}} \tag{4.2}$$

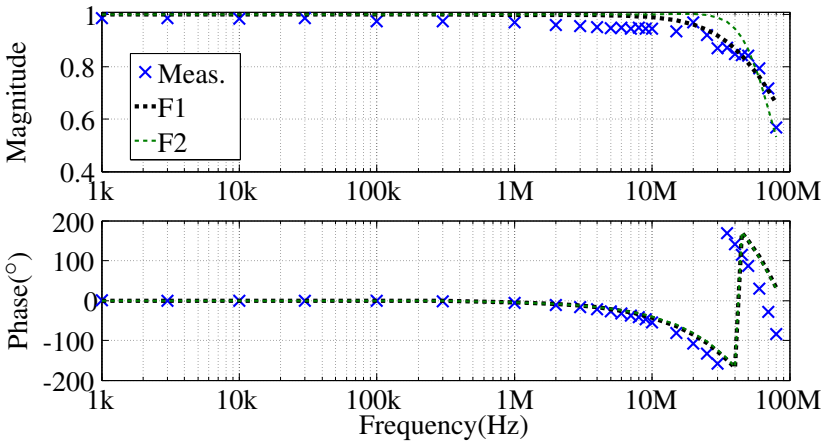


FIGURE 4.7: Functions to represent HECP attenuation

The second function F2 shown in eq.(4.3) is based on the transfer function of a second-order series RLC filter, in which parameter τ represents the signal delay. The three parameters τ, A and B can be obtained by the fitting method: $\tau = 7.6 \times 10^{-9}$(s), $A = 3.5 \times 10^{-9}$(s), $B = 6.2 \times 10^{7}$(Hz). The comparison between F2 and the measurement is shown in Figure 4.7. It can be seen that F2 represents well the measured attenuation of the HECP transfer function above 60MHz.

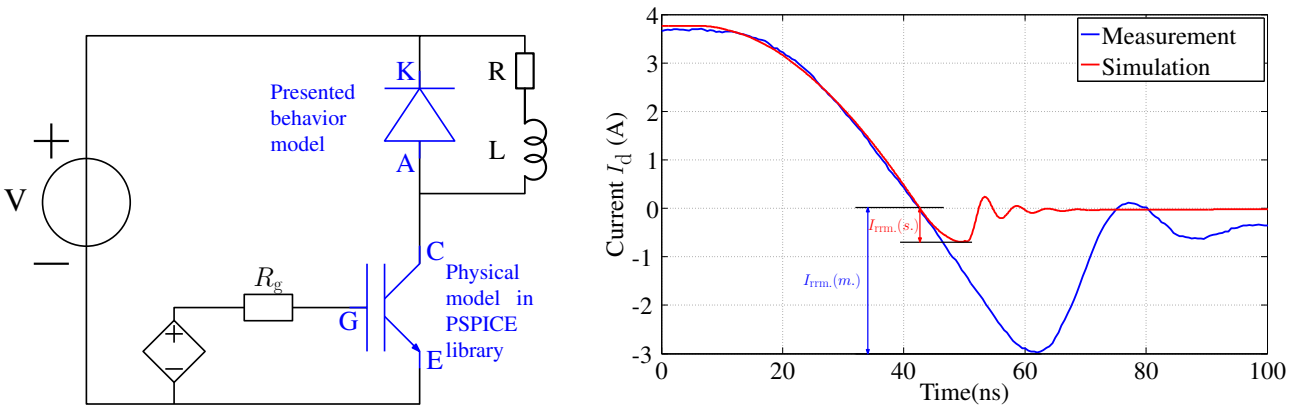
$$F2 = \frac{exp\left(-\tau \cdot j\omega\right)}{1 + j\omega A + \left(j\frac{\omega}{B}\right)^2} \tag{4.3}$$

In the next section, the obtained passive components models and HECP transfer functions are used in the circuit simulation in order to validate the diode model.

4.1.3 Measurement results

4.1.3.1 Results of different switching conditions

In the buck converter shown in Figure 4.1(a), the diode switching current I_d is measured at first under the following conditions: the input voltage $V = 50$V, the output current $I_L = 3$A and the power transistor switches at 100kHz. The simulation circuit is shown in Figure 4.8(a), in which the IGBT IXGR40N60C2 model is a PSPICE physical model given in the software library. The load is at first represented by its basic model R and L in Figure 4.3(b) and neither C_{bus} model nor HECP insertion impedance is added in the simulation circuit. R_g in the simulation circuit is regulated in order to have a similar dI_d/dt with the measurement. The diode STTH15R06 is represented by its behavior model when T_j=40°C shown in Figure 3.26 for R_{1s}, R_{2s} and in Figure 3.15(b) for C. It is shown in Figure 3.15(b) the evolution of C with voltage V_{AK}, according to Figure 3.26, the evolution of C with voltage V_{AA1} can be obtained and used in the model.



(a) Simulation circuit

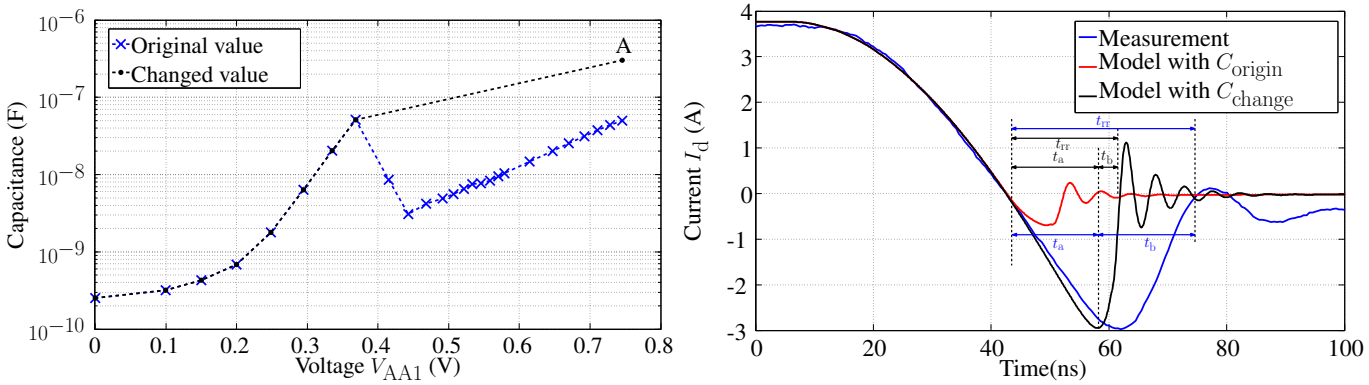
(b) Simulation and measurement result of diode reverse recovery current (T_j=40°C)

FIGURE 4.8: Simulation circuit and result

It is shown in Figure 4.8(b) the comparison between the simulation and measurement results. It can be seen that the presented behavior model does not reproduce measured diode maximal reverse recovery current I_{rrm}. The obtained I_{rrm} value in simulation I_{rrm}(s.) is much smaller than that of the measurement I_{rrm}(m.). This first result is not surprising, because it is presented in Chapter 3.1.2 that when the diode begins to conduct the current, the values of C in Figure 3.15(b) is not well characterized, so there is a discontinuity in its obtained values. It is proved by the comparison in Figure 4.8(b) that the stored charge when diode in conduction is not correctly represented by the model due to the inaccurately obtained C values, thus I_{rrm}(s.) is not correct. To resolve this problem, a first approach is to increase the C values when diode in conduction.

The discontinuity part in the original C values is replaced by the evolution of the capacitance to its value A, which is indicated in Figure 4.9(a). This extrapolation makes the capacitance continuous,

of which the evolution with the voltage is like a Spice diode model. The value of A can be obtained when I_{rrm}(s.)=I_{rrm}(m.) at one switching condition, which is represented in Figure 4.9(b). It is shown that in order to represent the same I_{rrm}(m.) value by the model, the C values should be increased by one order of magnitude compared with its original values. It is also shown in Figure 4.9(b) that the reverse recovery time t_{rr} in the simulation t_{rr}(s.) is much shorter than the measurement t_{rr}(m.), especially the time of t_{b}.

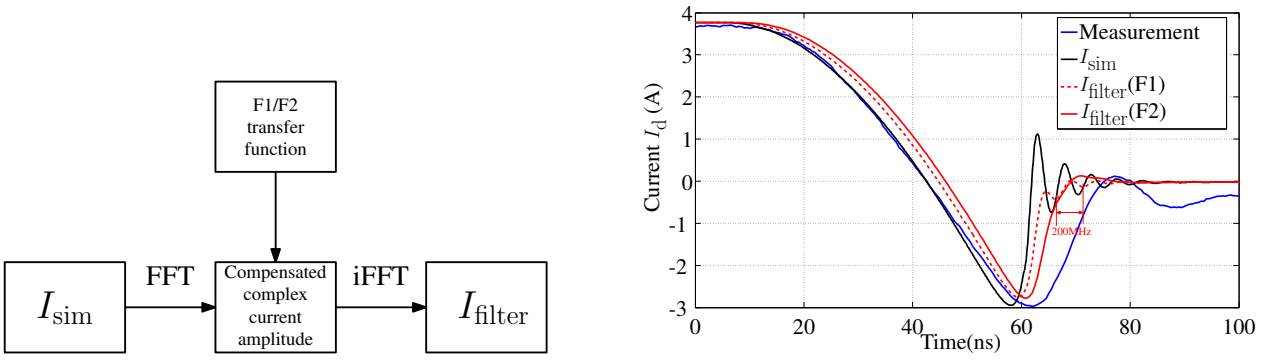


(a) Changed C values

(b) Simulation and measurement result of diode reverse recovery current (T_{j}=40°C)

FIGURE 4.9: Model with changed C values and simulation result

It is presented in Figure 4.7 that the measured current can be attenuated by HECP transfer function, which means that an attenuated measurement current I_{m} is compared with a non-attenuated simulation current I_{sim} in Figure 4.9(b). To investigate the influence of the HECP transfer function on I_{sim} and to compare I_{m} with an attenuated simulation current I_{filter}, the following operation which is illustrated by the flowchart shown in Figure 4.10(a) is applied on I_{sim}. The presented HECP transfer functions F1 and F2 are used to compensate I_{sim} after FFT calculation in frequency domain. The current I_{filter} in time domain can then be obtained via iFFT.



(a) Flowchart

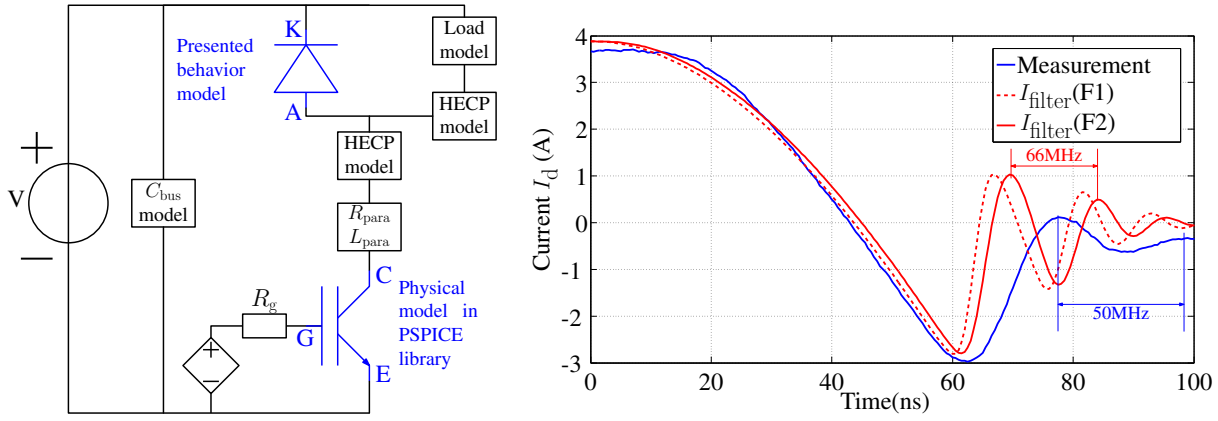
(b) Simulation and measurement results

FIGURE 4.10: Flowchart to get I_{filter} and comparison between I_{sim} and I_{filter}

Currents I_{filter} by F1 and F2 are then compared with I_{sim} and I_{m}, which are shown in Figure 4.10(b). It can be seen that both the filtered currents by F1 (I_{filter}(F1)) and F2 (I_{filter}(F2)) are closer to the

measurement on reverse recovery time. It is also shown in that switching current slope is about 150A/μs and the I_{rrm}(s.) in filtered currents is slightly smaller than I_{sim}. If current switches much faster, then this difference of I_{rrm}(s.) will be bigger. The above results prove the attenuation effect of the HECP on obtained simulation current. As F2 is a second-order filter, the 200MHz LC resonance observed in I_{sim} which is due to the L_{para} inside the diode model with its junction capacitance C_{j} is attenuated more by F2 than by F1.

The presented C_{bus} model shown in Figure 4.2(b), load model shown in Figure 4.3(b), HECP insertion impedance model shown in Figure 4.5(a) and PCB parasitic impedances (R_{para} and L_{para}) are added in the simulation circuit shown in Figure 4.11(a) to study the influence of the above passive component models on diode switching waveform.



(a) Simulation circuit

(b) Simulation and measurement results

FIGURE 4.11: Simulation and measurement results including circuit passive components models of Buck converter

As there are more L_{para} added in the simulation circuit, which slows down the slope of the current switching, thus R_{g} in Figure 4.11(a) is readjusted to have a similar $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$ to the measurement in simulation. It can be seen that the simulation circuit shown in Figure 4.11(a) represents almost the same measurement circuit shown in Figure 4.1(b).

The currents I_{filter}(F1), I_{filter}(F2) are compared with the measurement results as shown in Figure 4.11(b). It can be seen that the added passive component models does not obviously influence the t_{rr}(s.) value in comparison with the result in Figure 4.10(b). Nevertheless, the LC resonance frequency at the end of the current switching is about 66MHz in simulation in Figure 4.11(b), which is closer to the 50MHz in the measurement in comparison with the 200MHz simulation result in Figure 4.10(b). The difference of this LC resonance frequency shown in Figure 4.11(b) is probably due to the mutual L_{para} in the commutation mesh which can not be measured directly with an impedance analyzer.

A presented diode (STTH15R06) PSPICE model in Chapter 3.1.1 is simulated in the same simulation circuit shown in Figure 4.11(a) to compare with the proposed diode behavioral model based on

experimental characterization. The comparison result is shown in Figure 4.12. It is shown that the PSPICE model does not reproduce neither a satisfying I_{rrm} value nor a t_{rr} value in comparison with the measurement. In contrast, the presented behavioral model can be modified easily to make it reproduce a similar I_{rrm} to the measurement, while it is difficult to modify several parameters in PSPICE physical model to make it reproduce a satisfying I_{rrm} value. It is also shown that diode datasheet information is not sufficient to make a diode behavioral model, because there is hardly any capacitance value when diode in conduction can be found in its technical datasheet, which proves the necessity of the diode ON-state characterization presented in Chapter 3.1.2.

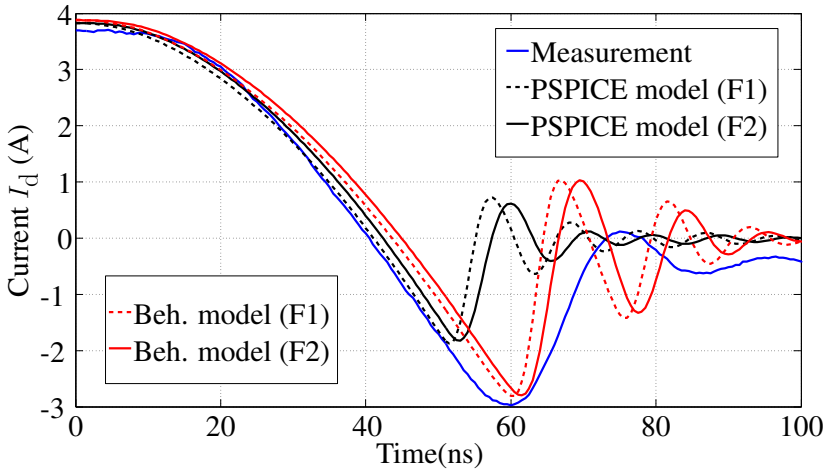
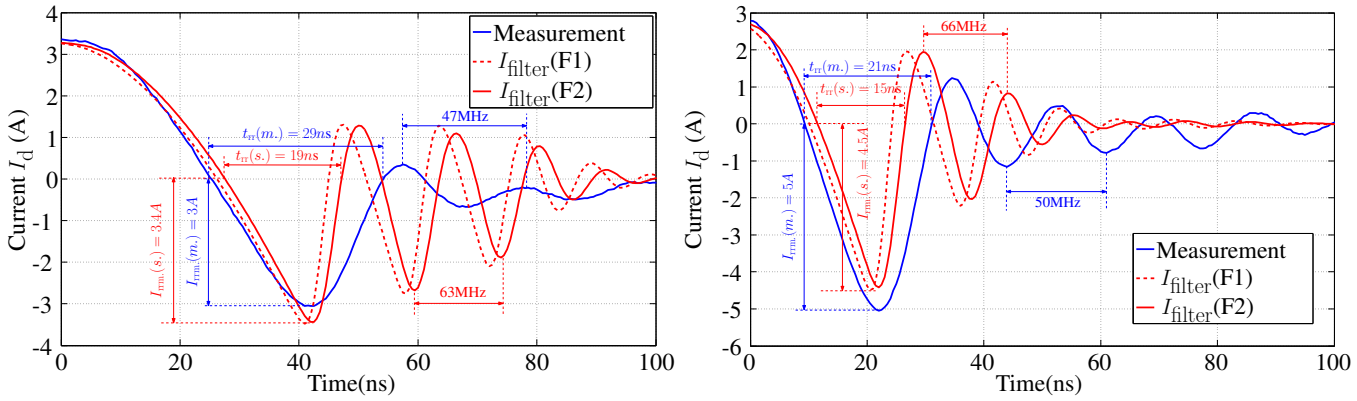


FIGURE 4.12: Comparison between PSPICE model, proposed behavioral model and measurement

The measurement $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$ is then varied in order to validate the stability of the presented diode model in different operation conditions as shown in Figure 4.13.



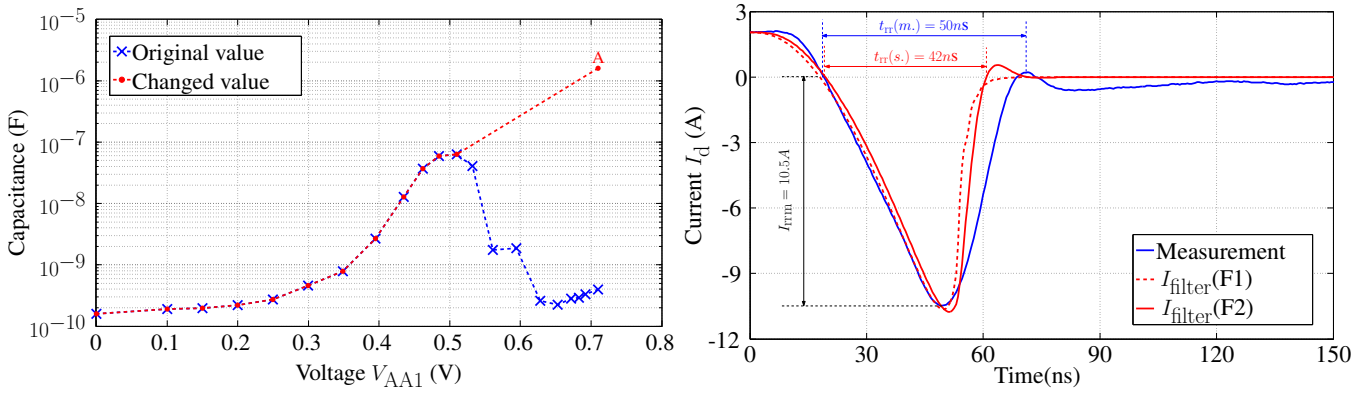
(a) $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t = 200\mathrm{A}/\mu\mathrm{s}$ (b) $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t = 460\mathrm{A}/\mu\mathrm{s}$

FIGURE 4.13: Comparison of different $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$ between the measurement and the diode model

When $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t = 200\mathrm{A}/\mu\mathrm{s}$, the comparison result is shown in Figure 4.13(a), in which it is shown that I_{rrm}(s.) value is almost the same to I_{rrm}(m.) value. The difference between the model and the measurement is about 13% of the I_{rrm}(m.). t_{rr}(s.) is 19ns, while t_{rr}(m.) is 29ns. The difference between the model and the measurement is about 30% of the t_{rr}(m.). The resonance frequency of the simulation is about 63MHz, while that of the measurement is about 47MHz.

When $\mathrm{d}I_\mathrm{d}/\mathrm{d}t = 460\mathrm{A}/\mu\mathrm{s}$, the comparison result is shown in Figure 4.13(b), in which it is shown that I_rrm(s.) value is still close to I_rrm(m.) value. The difference between the model and the measurement is about 10% of the I_rrm(m.). t_rr(s.) is 15ns, while t_rr(m.) is 21ns. The difference between the model and the measurement is about 30% of the t_rr(m.). The resonance frequency of the simulation is about 66MHz, while that of the measurement is about 50MHz.

It can be seen in the above results that after increasing C values when diode is in conduction, the proposed diode (STTH15R06) behavioral model can better represents the diode reverse recovery current in different switching conditions. In order to validate the robustness of the proposed diode modeling method, another diode MUR880E behavioral model represented in Figure 3.27 for R_1s and R_2s values and in Figure 3.18(c) for C values is compared with the measurement in different switching conditions. The measurement circuit is the same with that shown in Figure 4.1. The simulation circuit is the same with that shown in Figure 4.8(a).



(a) Changed C values (b) Simulation and measurement results

FIGURE 4.14: Changed C values and comparison of simulation and measurement results of diode MUR880E behavioral model

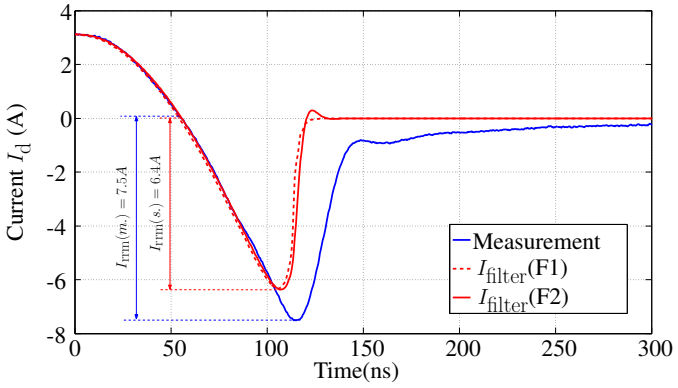


FIGURE 4.15: Comparison between diode MUR880E behavioral model and measurement with a different current slope

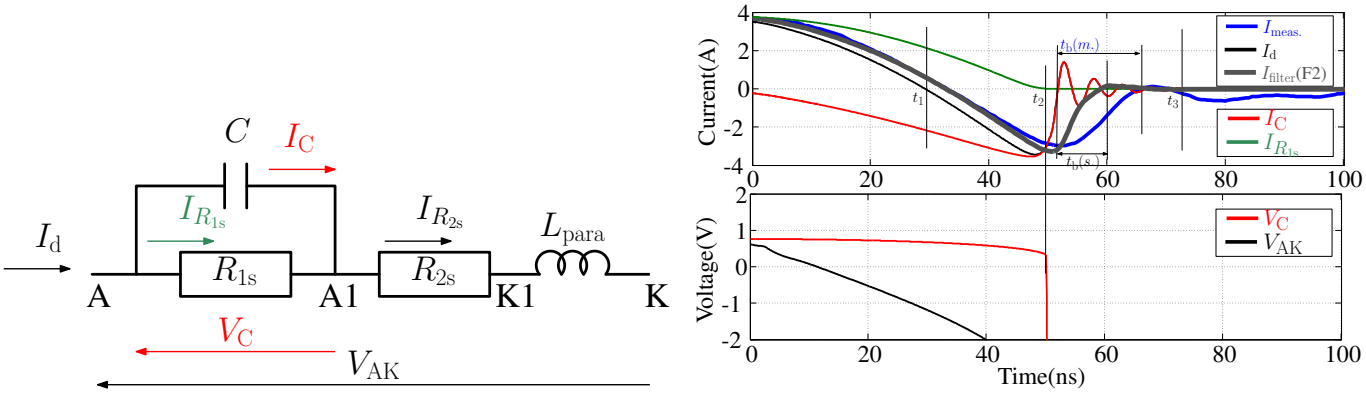
The C values are changed in the same way with that shown in Figure 4.9(a) when diode is in conduction. The changed C values of diode MUR880E behavioral model are shown in Figure 4.14(a). The simulation results compared to measurement data are shown in Figure 4.14(b). It can be seen

that for this diode, its stored charge is much bigger than that of the previous diode (STTH15R06), so the measured I_{rrm} and t_{rr} at switching current $I = 2\mathrm{A}$ and $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t = 340\mathrm{A}/\mu\mathrm{s}$ is much bigger than diode STTH15R06. The changed C values make the model to reproduce an almost same I_{rrm} value to the measurement. t_{rr} obtained in the simulation is about $42ns$, which is close to that in the measurement about $50ns$.

Then the diode waveform is measured when it switches at $I = 3\mathrm{A}$ with a current slope $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t = 125\mathrm{A}/\mu\mathrm{s}$. The comparison between the measurement and the simulation results are shown in Figure 4.15. It can be seen that I_{rrm}(m.) is about 7.5A, while I_{rrm}(s.) is about 6.4A. The difference between the model and the measurement is about 15% of the I_{rrm}(m.). Similar like the previous diode STTH15R06 model, t_{rr}(s.) is shorter than t_{rr}(m.).

4.1.3.2 Model improvement

It can be seen in the above results that once C values are changed to represent I_{rrm} value at one $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$, the model can generally represent satisfactorily the diode reverse recovery switching waveform at different switching conditions. The main difference between the model and the measurement is on t_{rr} value. Its value of the measurement is bigger than that of the simulation. To further investigate on this difference, $R_{1\mathrm{s}}$ current $I_{R_{1\mathrm{s}}}$, C current I_{C} and its voltage V_{C}, diode current I_{d} (which is the same as $R_{2\mathrm{s}}$ current $I_{R_{2\mathrm{s}}}$) and its voltage V_{AK} waveforms are separated to be analyzed. Each above variable of the diode model is shown in Figure 4.16(a) and they are represented in Figure 4.16(b) for the simulation results based on the simulation circuit shown in Figure 4.8(a) (without parasitic inductance added in the simulation circuit).



(a) Each variable of the model

(b) Different waveforms

FIGURE 4.16: Each variable of the diode model and their waveforms

According to the simulation results shown in Figure 4.16(b), it can be seen that the diode turn-off switching can be mainly divided on three steps by the presented model:

1. During 0-t_1, when the I_{d} current begins to decrease, C begins to discharge at the same time, the discharge current flows through $R_{1\mathrm{s}}$, with $I_{R_{1\mathrm{s}}} = I_{\mathrm{d}} - I_{\mathrm{C}}$. The $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$ slew rate during this

period induces a negative voltage V_{K1K} across the L_{para}, which at some point makes the voltage V_{AK} negative because of the relation $V_{\mathrm{AK}} = V_{\mathrm{C}} + V_{\mathrm{A1K1}} + V_{\mathrm{K1K}}$, even though the voltage V_{C} is still positive during this period. At instant t_1, I_{d} is equal to 0.

2. During t_1-t_2, I_{d} changes the direction as indicated in Figure 4.16(a). During this step, C continues to discharge. Different from the previous step, C is discharged both by $I_{R_{1\mathrm{s}}}$ and I_{d} current. At instant t_2, the stored charge in C is totally discharged, therefore both discharge current $I_{R_{1\mathrm{s}}}$ and the voltage V_{C} decrease to 0.

3. During t_2-t_3, C is charged reversely by the current I_{d}, so V_{C} increases reversely at this step. As there is about no current $I_{R_{1\mathrm{s}}}$ during this step, $I_{\mathrm{d}} = I_{\mathrm{C}}$. At the end of this step, V_{C} increases reversely to the same value as V_{AK}.

Based on the above analysis, in order to reproduce a similar t_{b} value in the simulation $t_{\mathrm{b}}(s.)$ by the model to the measurement $t_{\mathrm{b}}(m.)$, it can be seen that one possible solution shall be brought to the model: at instant t_2, V_{C} shall not decrease to 0, thus there will be stored charges that are necessary to be swept by $I_{R_{2\mathrm{s}}}$ during t_2-t_3, which might increase the $t_{\mathrm{b}}(s.)$ value.

To realize the above solution, there are the following two conditions that are necessary:

1. The swept charge by $I_{R_{2\mathrm{s}}}$ during t_1-t_2 should be less than the presented model, thus there will be more charge to be swept by $I_{R_{2\mathrm{s}}}$ during t_2-t_3.

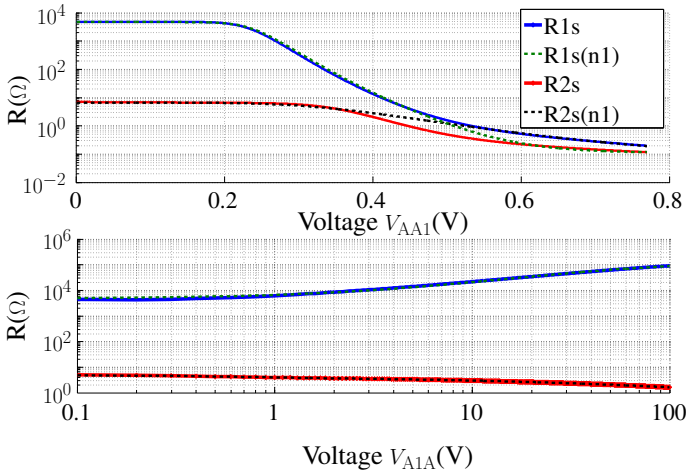
   To make the model satisfy this condition, it is necessary to increase the time constant $R_{2\mathrm{s}}C$ during t_1-t_2 period, which means to increase $R_{2\mathrm{s}}$ values. During this period, V_{C} in the above simulation is above 0.5V, so $R_{1\mathrm{s}}$ value is from several ohms to a dozen ohms and $R_{2\mathrm{s}}$ value is from several hundreds milliohms to several ohms according to the results shown in Figure 3.26.

   The results in Figure 3.26 is based on the results presented in Figure 3.20, in which a factor α is introduced to redistribute the obtained R_1 and R_2 values when diode in conduction in eq.(3.8), and $\alpha = 0.5$ in the presented model. The α value brings a liberty degree in the model and its value can be varied from 0 to 1 for each obtained sum value of R_1 and R_2 at one V_{AK} voltage above 0.5V. When $\alpha < 0.5$, the obtained R_2 values are bigger than R_1 values according to eq.(3.8), so the $R_{2\mathrm{s}}$ values might be bigger than $R_{1\mathrm{s}}$ values when diode in conduction. There are α values to make the following change in the model, that when diode is in conduction, the new $R_{1\mathrm{s}}$ values $R_{1\mathrm{s}}(\mathrm{n1}) = R_{2\mathrm{s}}$ and the new $R_{2\mathrm{s}}$ values $R_{2\mathrm{s}}(\mathrm{n1}) = R_{1\mathrm{s}}$. This change may make the model satisfy the above condition. $R_{1\mathrm{s}}(\mathrm{n1})$ values and $R_{2\mathrm{s}}(\mathrm{n1})$ values are shown in Figure 4.17(a), where voltage V_{AA1} indicates that the diode is in ON-state and V_{A1A} indicates that the diode is in OFF-state.

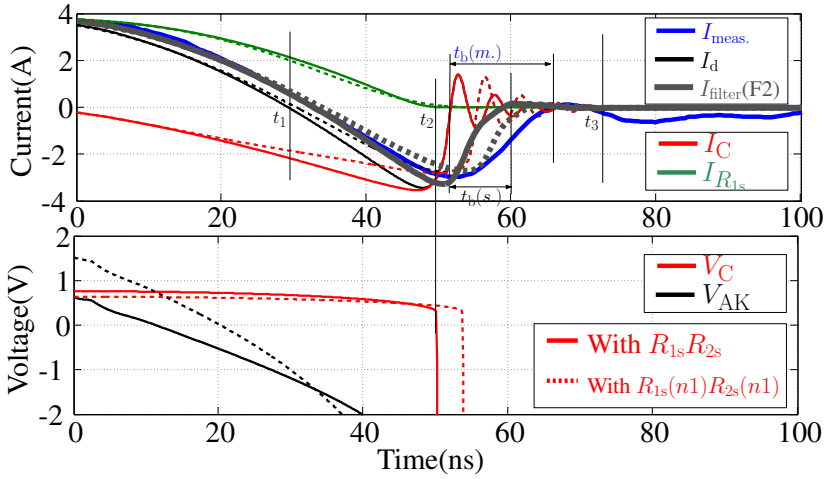
   The model with $R_{1\mathrm{s}}(\mathrm{n1})$ values and $R_{2\mathrm{s}}(\mathrm{n1})$ values is simulated and the obtained results are compared with the measurement in the same condition shown in Figure 4.16(b). As $R_{1\mathrm{s}}(\mathrm{n1})$

values and R_{2s}(n1) values are changed when V_{AK} above 0.5V, therefore the value of A presented in Figure 4.9(a) is changed to 0.8μF to make the model reproduce a similar I_{rrm} value to the measurement.

The comparison between the model with R_{1s}(n1) and R_{2s}(n1) values and that with R_{1s} and R_{2s} values is shown in Figure 4.17(b). It can be seen that I_C current during t_1-t_2 is smaller than the previous simulation result, which means that there are less swept charges in the model with $R_{2s}(n1)$ values. Those changes also make that V_C remains positive after instant t_2, which makes the filtered current by transfer function F2 is closer to the measurement than the previous model.



(a) R_{1s}(n1) and R_{2s}(n1) values



(b) Waveforms comparison

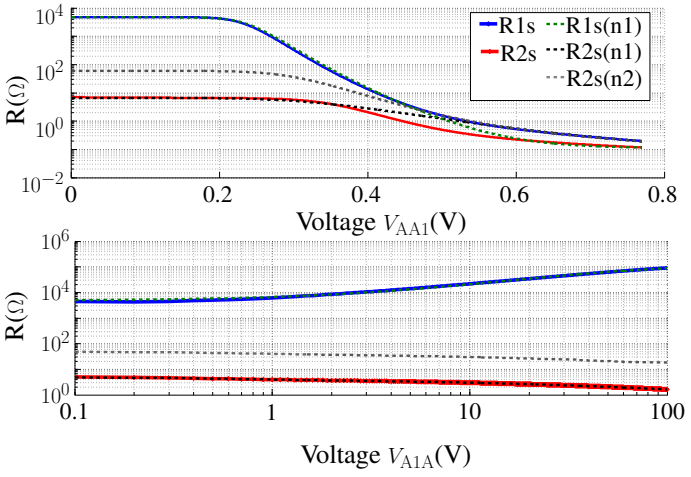
FIGURE 4.17: R_{1s}(n1) and R_{2s}(n1) values and the waveforms comparison

However, it is shown in Figure 4.17(b) that the stored charge in C is rapidly swept out by the I_d current soon after instant t_2.

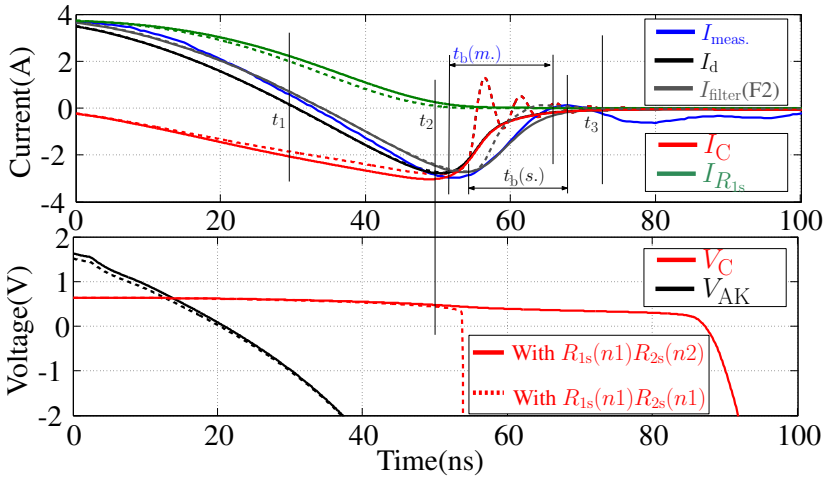
A second following condition is thus necessary.

2. The discharge current $I_{R_{2s}}$ evolution during t_2-t_3 shall be more slowly than the presented model in order to increase t_b time.

   To make the model satisfy this condition, it is necessary to increase the time constant $R_{2s}C$ during t_2-t_3 period, which means to increase R_{2s} values. During this period, V_C in the above simulation is from $0 - 0.3V$, and R_{2s} values are around several ohms according to the results shown in Figure 3.26.



(a) R_{1s}(n2) and R_{2s}(n2) values



(b) Waveforms comparison

FIGURE 4.18: R_{1s}(n2) and R_{2s}(n2) values and the waveforms comparison

It is to be noted that when V_{AK} is around 0V, the capacitance C values are mainly characterized in low frequency, which means R_1 values can hardly be correctly characterized, because its obtained values by fitting method in this situation may not influence the error between the measurement and the model. The real R_1 value at this condition may be much bigger than its obtained values according to the result shown in Figure 3.16. As what has been presented in Chapter 3.1.3, I_d can not be measured when V_{AK} is around 0V, and its obtained values are dependent on the sum of R_1 and R_2 values. A bigger R_1 value may give rise to a smaller I_d value, therefore bigger R_{1s} and R_{2s} values can be obtained. This uncertainty of R_1 values might

increase R_{2s} values when V_{AK} is around 0V. With this reason, R_{2s} new values (R_{2s}(n2)) when $V_{AK} \leq 0.3$V are increased by a factor of 10 to investigate their influence on diode switching waveform. R_{2s}(n2) values are shown in Figure 4.18(a) in comparison with previously presented R_{2s} and R_{2s}(n1) values.

The model with R_{1s}(n1) values and R_{2s}(n2) values is simulated and the obtained results are compared with the measurement in the same condition shown in Figure 4.16(b). As R_{2s}(n2) values are changed when $V_{AK} \leq 0.3$V, therefore the value of A presented in Figure 4.9(a) is changed to 1μF to make the model reproduce a similar I_{rrm} value to the measurement.

It is shown in Figure 4.18(b) the comparison of the current switching waveform between the diode model with R_{2s}(n2) values and $R_{2s}(n1)$ values. It can be seen that the stored charge in the C is increased when $R_{2s}(n2)$ values are used in the model, so V_C remains positive during t_2-t_3 period. During this period, a big R_{2s}(n2) value slows down the C discharge time constant so as to make the obtained switching waveform closer to the measurement than the previous model.

It can be seen that the above two changes improve the performance of the model to express diode reverse recovery current. The model is then compared with the measurement on different dI_d/dt switching conditions. I_{filter}(F2) is compared with the measurement, and the results are shown in Figure 4.19. It is shown that the presented behavioral model represents well both diode I_{rrm} value and t_{rr} value on different dI_d/dt switching conditions. Compared to the results in Figure 4.13, the improvement in the diode model by the above two changes can be validated.

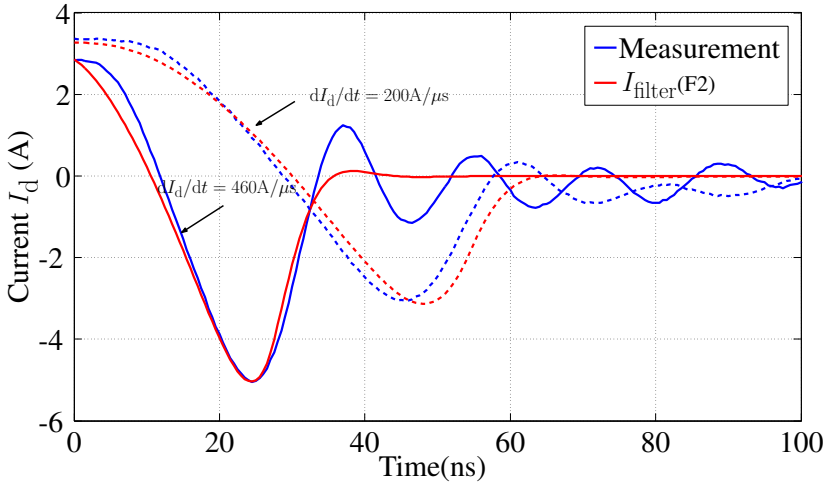


FIGURE 4.19: Comparison between simulation waveforms obtained with improved diode model and measurement results on different dI_d/dt

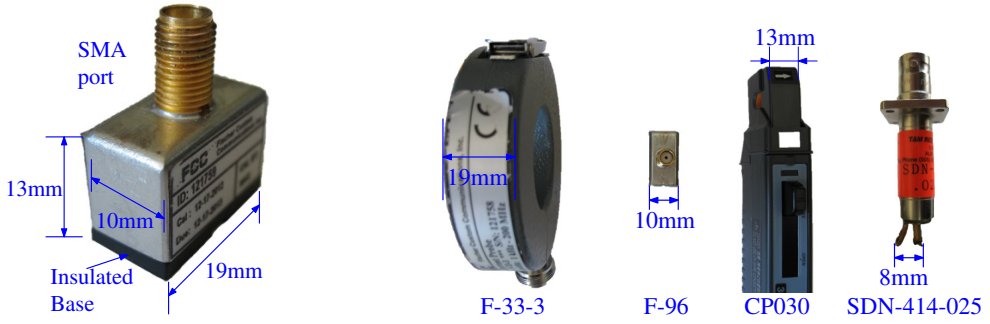
Diode SiC is usually a Schottky diode and it reproduces almost no reverse recovery phenomena during turn-off switching. For this reason, its modeling, which is presented in Chapter 4.3, can be simpler than a Si bipolar diode.

As shown in this section, the use of the HECP may change the current switching waveform due to its limited bandwidth of 50MHz. The minimal diode current switching time is about $20ns$ in the measurement, and the switching time of the wide bandgap power devices can be shorter than that, which proves that the use of the HECP is not adapted to measure power device fast switching waveform. Therefore, a current surface probe is to be presented in the next section to measure power device fast switching current in order to validate the power device model.

4.2 Fast Switching Current Measurement Methodology

It has been presented in Chapter 1.6.2 that current switching time of wide bandgap power devices can be shortened to a few nanoseconds, which requires that the current measurement probes must have a high bandwidth and a small insertion impedance. For this reason, a current surface probe (CSP) (FCC F-96, 1MHz-450MHz) is proposed to use in this thesis to measure power devices fast switching current. Once its use is validated, it is applied to measure SiC JFET switching current in order to validate the model which will be presented in the Chapter 4.3.

The dimension of the used CSP is presented in Figure 4.20.



(a) F-96 dimension

(b) Dimension comparison of the three current probes

FIGURE 4.20: Dimension of different current probes

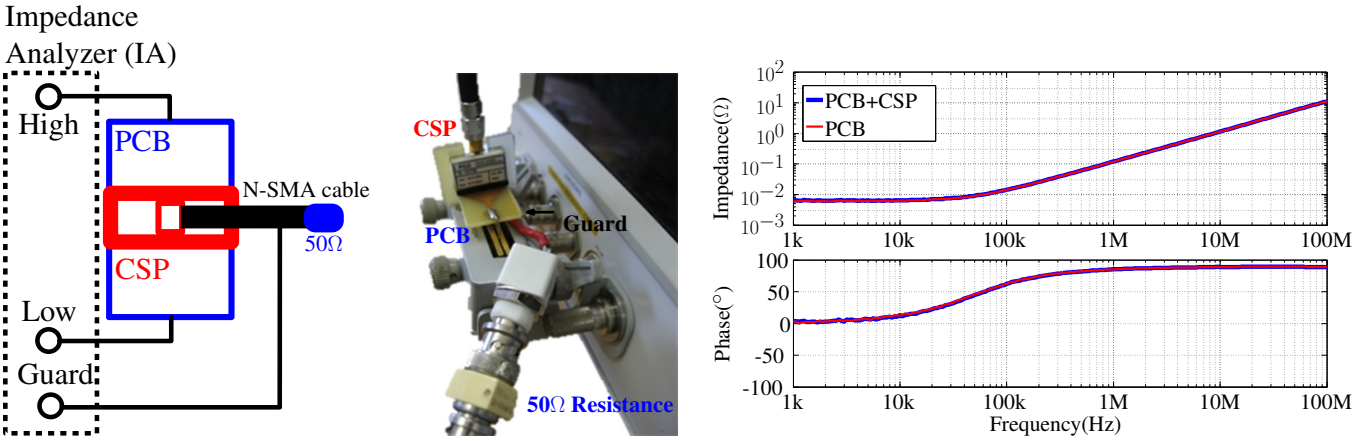
In this section, at first, the insertion impedances of the CSP is measured and compared with that of a current probe (CP) (FCC F-33-3, 1kHz-200MHz) shown in Figure 4.20). Then CSP complex transfer impedance is measured on different configurations. Subsequently, its transfer impedance is verified by comparing the measured IGBT collector current I_C waveform with CP and HECP. In order to measure fast switching current, a GaN HEMT power converter is used where drain current I_D waveform is measured and compared between CSP and CP. Furthermore, V_{DS} is measured to demonstrate the influence of the current probe insertion impedance on voltage waveform without and with the current probes. Then, in order to minimize parasitic inductances of the power converter, a special power converter is designed with the purpose of comparing I_D switching current measurement between the CSP and a current shunt (CS) (SDN-414-025, DC-1.2GHz).

4.2.1 Current surface probe characterization

Before using the CSP, it is necessary to characterize its insertion impedance and transfer impedance. The obtained transfer impedance will be used to correct the measured current values[1].

4.2.1.1 Insertion impedance

The insertion impedance of CSP is measured by the similar method presented in Chapter 4.1.2 for HECP: firstly, the impedance of a PCB associated to CSP is measured by an impedance analyzer. Then, the CSP is fixed above the PCB with one end connected to a 50Ω termination resistor via an N-SMA cable and the shielding part of the cable is connected to the Guard of the impedance analyzer. Thus, the impedance of the PCB with CSP is measured together. The measurement configuration is shown in Figure 4.21(a), of which the measurement photo is shown in Figure 4.21(b).



(a) Measurement configuration (b) Measurement Photo (c) Measurement results

FIGURE 4.21: CSP insertion impedance measurement configuration and results

The measurement impedances of the PCB and PCB with CSP are shown in Figure 4.21(c). As shown in the results, the PCB parasitic resistance and inductance are 0.062Ω and 18.3nH respectively, and the measured CSP insertion impedance is less than 1nH, thus, it has almost no influence on the measurement results, which means it is the associated PCB rather than the CSP which brings parasitic inductance in the measurement circuit.

The insertion impedances of the current probe (CP) is measured in the similar condition. The measurement results are shown in Figure 4.22. It can be noted that, before 10MHz, CP has an obvious influence on the measurement configuration. As a consequence, the insertion impedance of the CP is likely to influence both I_D and V_{DS} measurement, which will be shown later.

[1]It is to be noted that the transfer impedance in low frequency is also very important, because switching waveforms can not be simply obtained if switching frequency is in an attenuated zone.

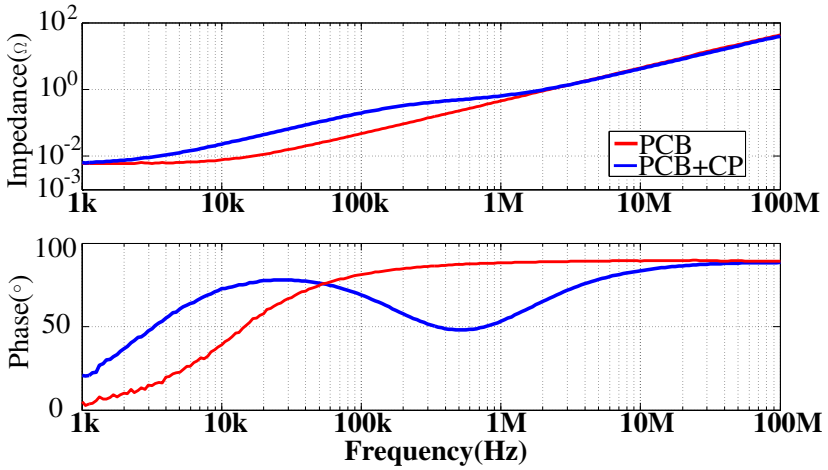


FIGURE 4.22: CP insertion impedance measurement results

Compared to that, CSP has small insertion impedance, which guarantees that it will not modify V_{DS} switching voltage waveform.

4.2.1.2 Transfer impedance

The definition of the transfer impedance of a CP or CSP is shown in Figure 4.23.

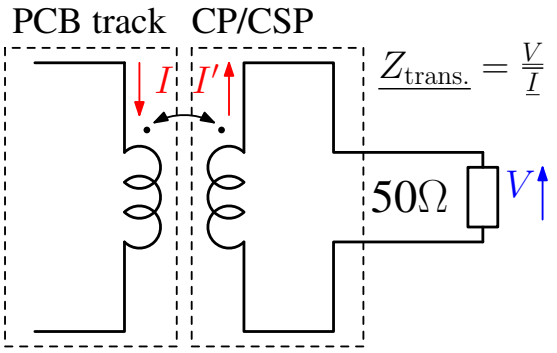


FIGURE 4.23: Current probe transfer impedance definition

The coupling effect between the CP and the PCB track can be modeled in the form of a transformer. The CP is terminated by a 50Ω resistance of the measurement equipment. The current flowing through the CP induces a voltage across the 50Ω termination resistance. The transfer impedance is defined by $\underline{Z_{\mathrm{trans}}} = \frac{\underline{V}}{\underline{I}}$. The method proposed in [59, 123] is adapted in this work to determine the CSP transfer impedance using a Vector Network Analyzer (VNA) on three ports[2]. The CSP transfer impedance is characterized in the following two situations.

Situation 1

The measurement configuration is illustrated in Figure 4.24(a) and its realization is shown in Figure 4.24(b), where the voltage source in port 2 of the VNA induces a current I_{m} in the measurement

[2]The presented method in Chapter 4.1.2 is to characterize the transfer function of an active current probe by using an oscilloscope, which is limited to 80MHz. To measure fast switching current, it is necessary to characterize the transfer impedance of a passive current probe in higher frequency. For this reason, this method by using a VNA is able to achieve this objective.

system. When I_m passes to port 3, it induces a voltage V_{p3} across the internal 50Ω resistance of the port 3. Thus, I_m can be calculated by:

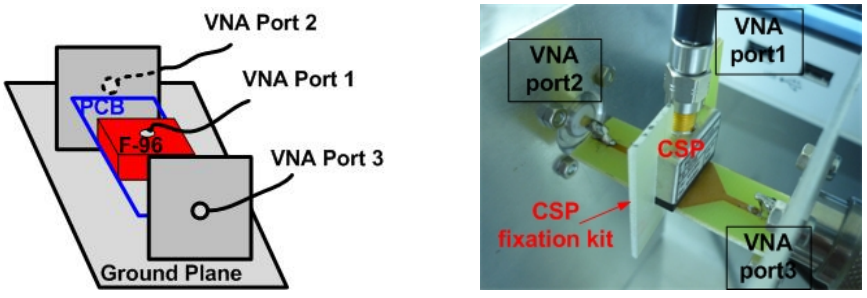
$$\underline{I_m} = \frac{\underline{V_{p3}}}{50}. \tag{4.4}$$

When I_m flows below the CSP, it induces a voltage V_{p2} across the internal 50Ω resistance of the port 2. I_m can also be calculated by

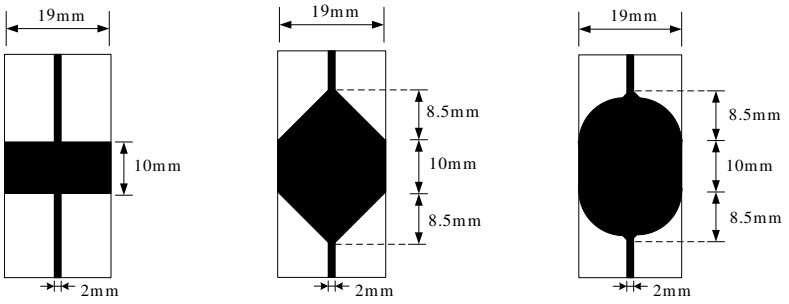
$$\underline{I_m} = \frac{\underline{V_{p1}}}{\underline{Z_{trans}}}. \tag{4.5}$$

By combining eq.(4.4) and eq.(4.6) and using S parameters definition, CSP transfer impedance Z_{trans} can be obtained by:

$$\underline{Z_{trans}} = 50\frac{\underline{S_{12}}}{\underline{S_{32}}}. \tag{4.6}$$



(a) Measurement configuration (b) Measurement setup photo



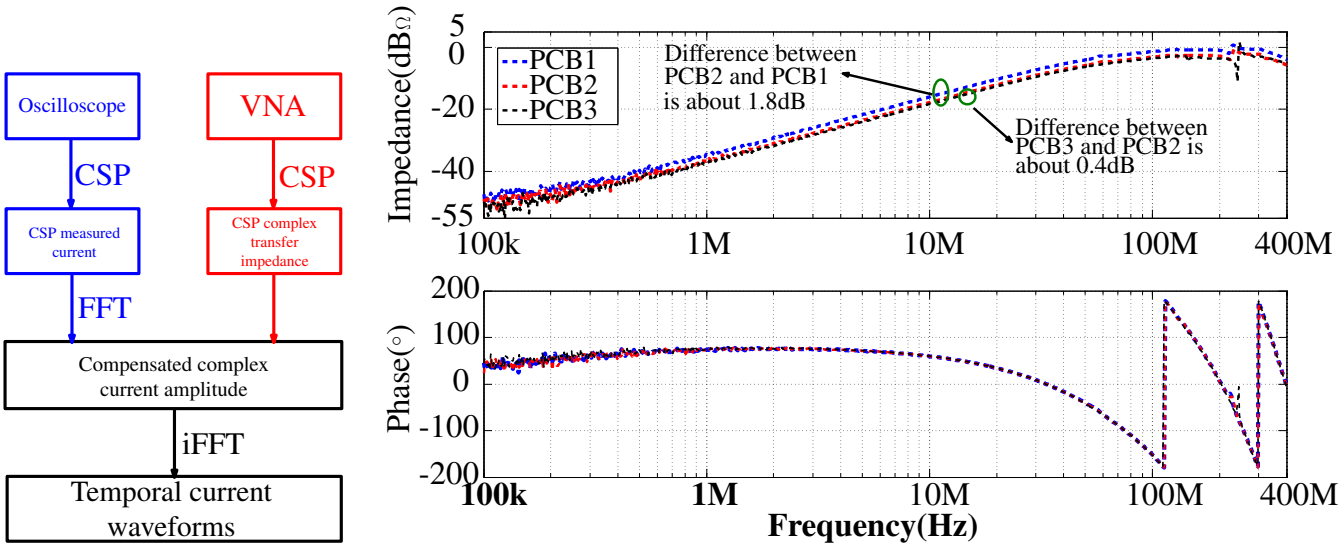
(c) PCB1 (d) PCB2 (e) PCB3

FIGURE 4.24: CSP transfer impedance measurement configuration with three different PCBs

Due to CSP dimension (shown in Figure 4.20) and its special half clamp-on structure, its transfer impedance is suspected to be dependent on PCB geometry. Thus, three PCB configurations shown in Figure 4.24(c)-Figure 4.24(e) are designed in the aim of studying PCB geometry influence on CSP transfer impedance. The width of all PCBs is 19mm which equals to the CSP width. The transfer

impedance characterization helps to get not only the impedance but also the phase information, which is not generally given in current probes technical datasheets. Hence, CSP complex transfer impedance can be used to compensate its measured current amplitude in frequency domain. Then the compensated current amplitude can be converted into time domain via iFFT to have temporal current waveforms. The flowchart is shown in Figure 4.25(a).

The measurement results are shown in Figure 4.25(b). Above 100MHz, there is a phase shift from -180° to 180°, which shows a signal delay due to the N-SMA cable connecting CSP with the VNA. Below 1MHz, CSP transfer impedance is so small that the characterization results are almost in the noise level. From 10MHz to 200MHz, the difference between PCB1 and PCB2 is about 1.8dB (which corresponds to 24% difference on the delivered probe voltage, which is notably visible on time-domain waveforms), while that between PCB2 and PCB3 is about 0.4dB (which equals to 5% difference in time domain). The characterization result in this situation shows that CSP transfer impedance depends on the PCB geometry. Thus, it is necessary to keep the PCB in the same configuration both in transfer impedance characterization and in power converter current measurement.



(a) Flowchart

(b) CSP complex transfer impedance measurement results

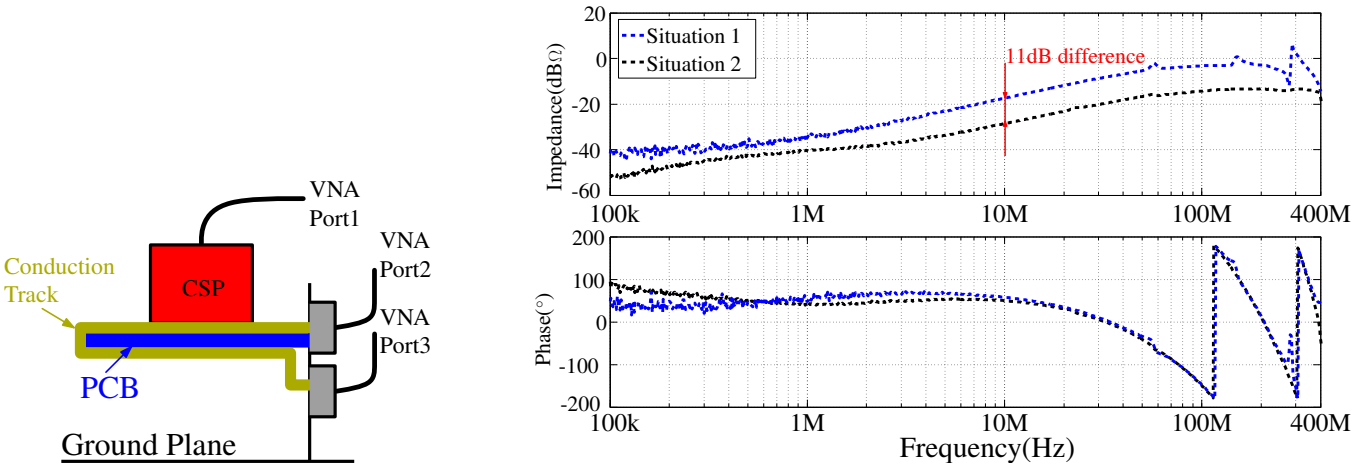
FIGURE 4.25: Flowchart and CSP complex transfer impedance measurement results

Situation 2

The transfer impedance of the special half clamp-on structure of the CSP might be influenced by the current around it. For this reason, another measurement configuration is illustrated in Figure 4.26(a). In this situation, the current injected by the VNA in Port 2 flows through the top side of the conduction track firstly, then it passes through the bottom side of the PCB to Port 3. When using CSP in power converters, this configuration is able to minimize the current loop therefore decreases the parasitic inductances brought in the circuit. The return current flowing at the bottom side of the PCB generates a magnetic filed in opposite direction that created by the current flowing on the top

side of the PCB. This return current may influence its transfer impedance. Therefore, this influence can be demonstrated in this characterization.

The comparison of the transfer impedance measurement results of the situation 1 and 2 are shown in Figure 4.26(b), in which the PCB top side dimension is the same in the two cases. It can be seen that a return current under the PCB can greatly reduce the CSP transfer impedance by 11dB above 10MHz, because it reduces the magnetic field density captured by the CSP in situation 1. It is proved by this result that if a CSP is used in a power converter with a return current beneath it, the influence of this return current should be included in its transfer impedance.



(a) Measurement configuration

(b) Measurement results

FIGURE 4.26: New CSP transfer impedance measurement configuration and results

It is to be noted that CSP transfer impedance is degraded in this condition, thus it is important to research on its sensitivity on lateral displacement and angular rotation. For this reason, its transfer impedance is characterized by displacing the CSP from the center of the PCB track with ±2mm and by rotating from the center with ±20°.

The measurement results of its transfer impedance (Z_t) sensitivity on lateral displacement (dZ_t/dx) and on angular rotation ($dZ_t/d\theta$) are shown in Figure 4.27, in which dZ_t/dx is less than 1dBΩ/mm and $dZ_t/d\theta$ is much less than 0.1dBΩ/degree. Furthermore, during all the measurements, the standard derivation of Z_t is less than 1dBΩ from 10MHz to 100MHz, which shows that CSP Z_t is only little influenced by imprecise centering on the PCB track.

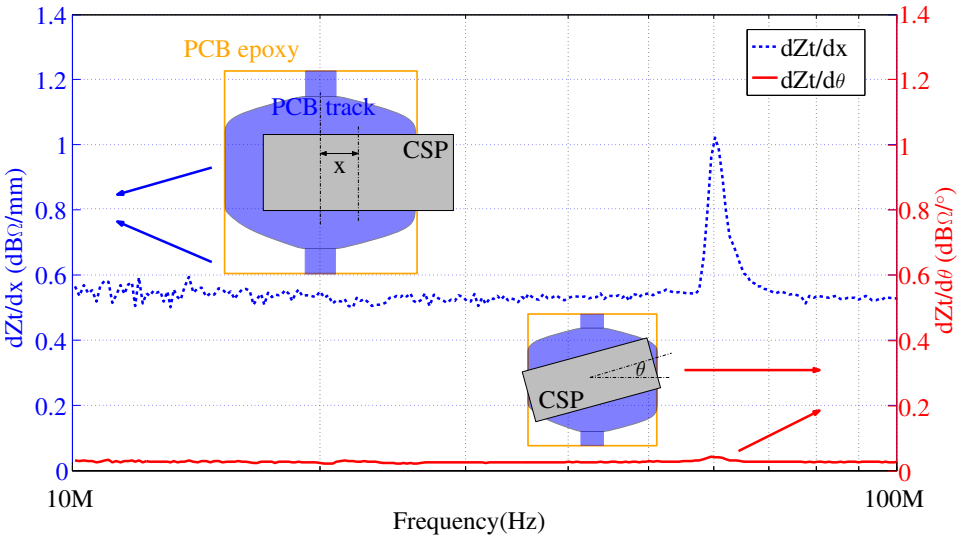


FIGURE 4.27: CSP transfer impedance sensitivity on lateral displacement and angular rotation

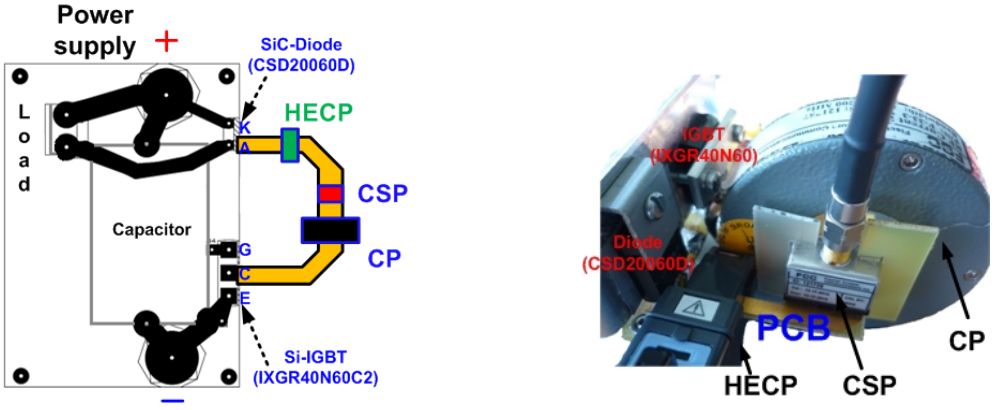
Using the transfer impedance characterization results, the switching current waveforms for different power devices measured by the CSP is compared with other current measurement equipments in the following section.

4.2.2 Switching current waveform measurement

In this section, a Si IGBT (IXGR40N60C2) collector switching current (I_C) and a GaN HEMT (EPC2012) drain switching current (I_D) are measured by the presented CSP.

4.2.2.1 Si IGBT switching current measurement

The aforementioned current probes HECP, CP and CSP are used in a buck converter (shown in Figure 4.28) to measure IGBT I_C current simultaneously.



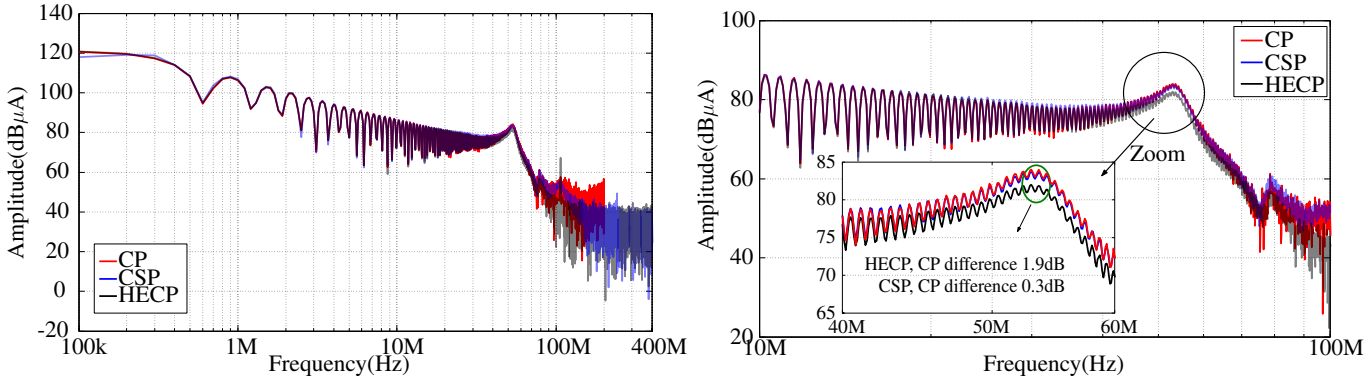
(a) Measurement setup (b) Measurement setup photo

FIGURE 4.28: IGBT current measurement configuration and its realization

The width of the PCB connecting the diode anode to the IGBT collector is 19mm. CSP transfer impedance based on PCB3 (Figure 4.24(e)) is used to compensate CSP measured current, while CP

transfer impedance is characterized with the same method. The power converter switches at 100kHz and the switching current is about 3.5A. The bandwidth of the measurement 12-bit oscilloscope is 600MHz.

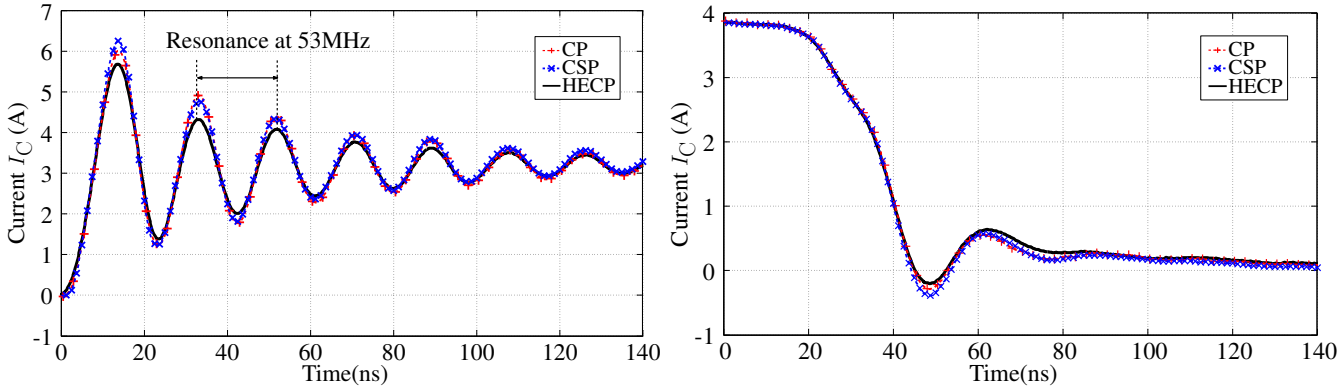
The measured I_C current amplitude is shown in Figure 4.29 via FFT, where CP and CSP are compensated each one by their respective transfer impedance. The bandwidth of the CP is up to 200MHz, so its measured current amplitude is shown until 200MHz. It is shown in Figure 4.29 that above 20MHz, measurement difference between HECP and the other two probes appears. At the resonance frequency 53MHz, the measured difference between CP and HECP is about 1.9dB.



(a) 100kHz-400MHz (b) 10MHz-100MHz

FIGURE 4.29: IGBT collector current amplitude comparison of all three probes

While above 20MHz, the difference of the measured current amplitude by CSP and CP is tiny, and at 53MHz, the difference is only 0.3dB. Then the measured currents with CP and CSP in frequency domain are converted into time domain via iFFT and the obtained results are shown in Figure 4.30.



(a) IGBT turn-on (b) IGBT turn-off

FIGURE 4.30: Comparison of the IGBT I_C current waveform measurement with three probes

As CSP and CP transfer impedances are characterized until 400MHz and 200MHz respectively, the converted currents in time domain are sampled at 800MHz and 400MHz individually. As shown in the Figure 4.30, the current measured by CSP and CP in time domain corresponds perfectly to

the current measured by HECP, the same I_C peak current and resonance amplitude at 53MHz in Figure 4.30(a) are measured both by CSP and CP, which is consistent with the above analysis on current amplitude comparison in frequency domain. The IGBT turn-off switching is relatively slow, therefore the measured I_C turn-off current by the three current probes is almost the same.

This result proves the validity of the CSP transfer impedance characterization results presented in the above section in "*Situation 1*". Otherwise, if CSP transfer impedance characterization based on PCB1 or PCB2 were used, a 24% or 5% difference will be observed between CSP and CP in the measured current.

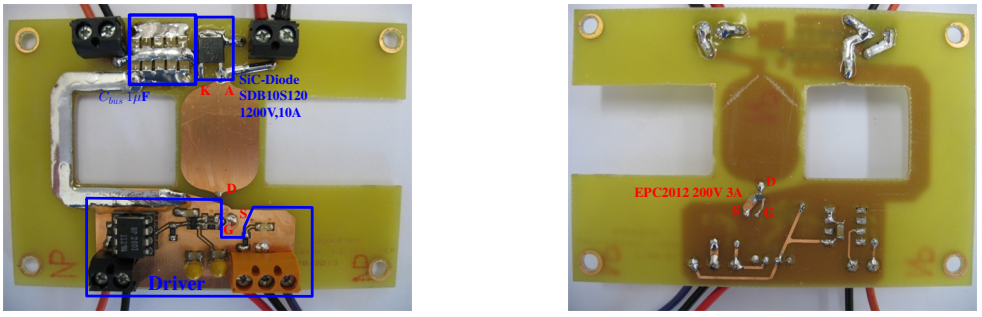
In the following section, CSP will be used to measure power device fast switching current on GaN HEMT.

4.2.2.2 GaN HEMT switching current measurement

In this section, GaN HEMT drain current waveform is first measured with the CP and CSP; then, a specific buck converter is designed to minimize the switching current loop in order to compare the CS and the CSP in very fast switching conditions.

Measurement with CP and CSP

To realize the buck converter, a GaN HEMT (EPC2012) and a SiC-diode (Semisouth SDB10S120) are used. The top side and bottom side of the PCB are shown in Figure 4.31. The hole in the PCB is used for putting CP. Due to CP dimension (shown in Figure 4.20), a big commutation mesh has to be designed. If only the CSP is used to measure current, the switching mesh will be much smaller, so as to decrease parasitic inductances. The operating frequency of the converter is 100kHz, while the load current is 1.8A and the input voltage is 40V. The drain current waveform I_D is measured respectively by CSP and CP. As presented in the previous Chapter 4.2.1.2 "*Situation 1*", CSP transfer impedance is first characterized with a PCB shown in Figure 4.31.

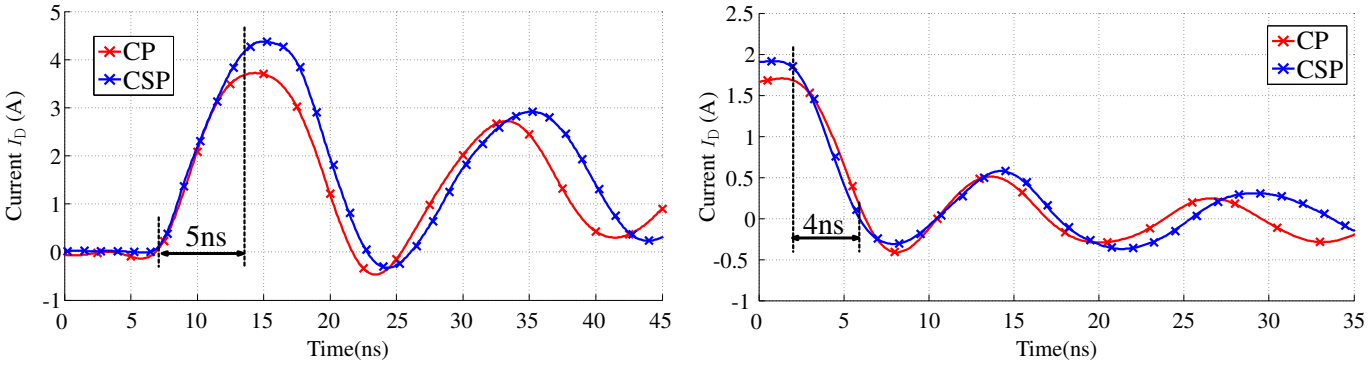


(a) Top side (b) Bottom side

FIGURE 4.31: Realization of the buck converter

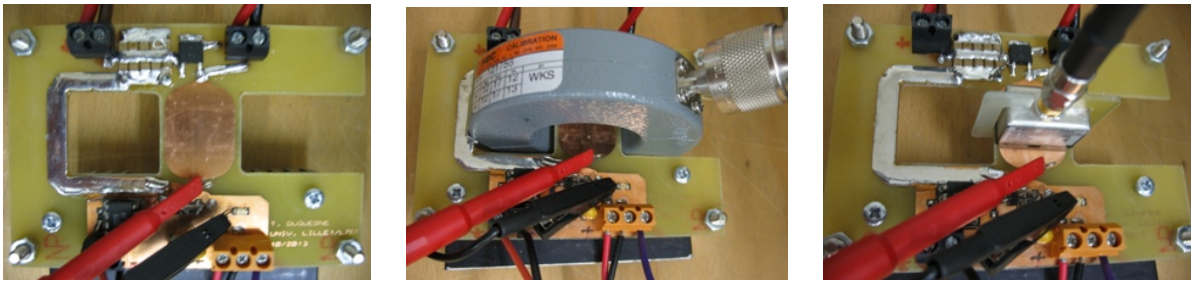
The current waveforms of the GaN-HEMT at turn-on and turn-off transitions are shown in Figure 4.32. For the turn-on switching current, the measured rise time both by CSP and CP is about

5ns, while for the turn-off transition, the measured fall time by the two probes is about 4ns. This result proves that CSP is able to measure the fast switching currents. The waveforms of the Figure 4.32(b) show a difference on the value of the turn-off switched current that is due to the switching frequency limited at 100kHz, and the CSP transfer impedance below 1MHz is so small that the measured current is the same as the noise level of the equipment. For this reason, to measure I_D current on a whole switching period by CSP, the switching frequency should be at least above 1MHz. The use of the PCB for the CP, shown in Figure 4.31 creates a long current loop in the circuit, which not only limits the converter operating frequency, but also slows down the current switching. For this reason, CSP is suitable to measure current of the very fast switching semiconductor devices.



(a) I_D at turn-on (b) I_D at turn-off

FIGURE 4.32: GaN HEMT switching current waveforms measured with two probes

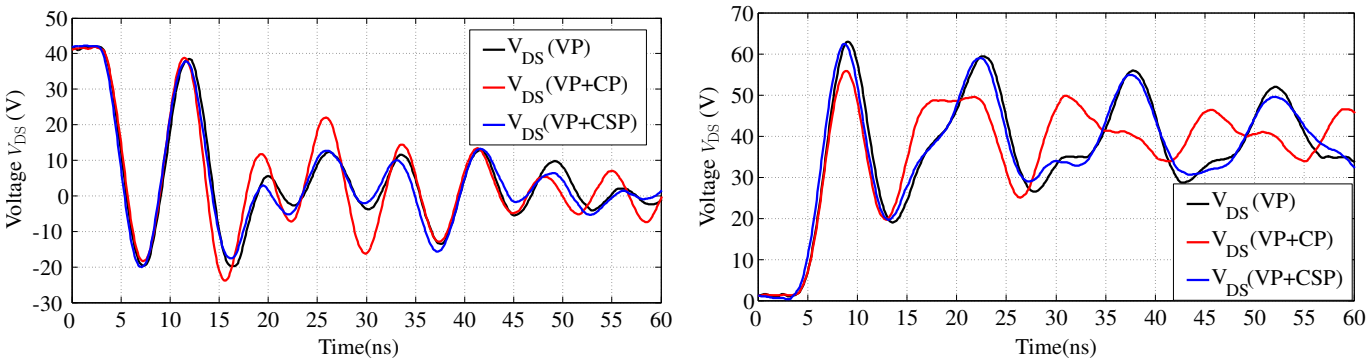


(a) VP (b) VP+CP (c) VP+CSP

FIGURE 4.33: GaN HEMT V_{DS} switching voltage measurement

In order to compare the influence of the CP and CSP insertion impedance on the GaN HEMT voltage waveform, V_{DS} is measured by a passive voltage probe (VP) (Lecroy PPE4kV, DC-400MHz) in the situations without and with the current probes. First, V_{DS} is measured when there is no current probes, of which the measurement photo is shown in Figure 4.33(a); then it is measured when CP and CSP are put in the circuit, of which the measurement photo is shown in Figure 4.33(b) and Figure 4.33(c) respectively.

The measurement results of all the above situations are shown in Figure 4.34. It is shown that the use of CSP has almost no influence on V_{DS} waveform measurement because of its small insertion impedance. However, the use of CP modifies the measured waveform because of its insertion impedance that is added in the switching loop circuit.



(a) Turn-on (b) Turn-off

FIGURE 4.34: Influence of the current probes on V_{DS} waveform measurement

In the following section, in order to optimize the PCB design to measure faster switching current and less noisy voltage waveforms, a comparison between a current shunt and CSP to measure GaN-HEMT drain current is carried out.

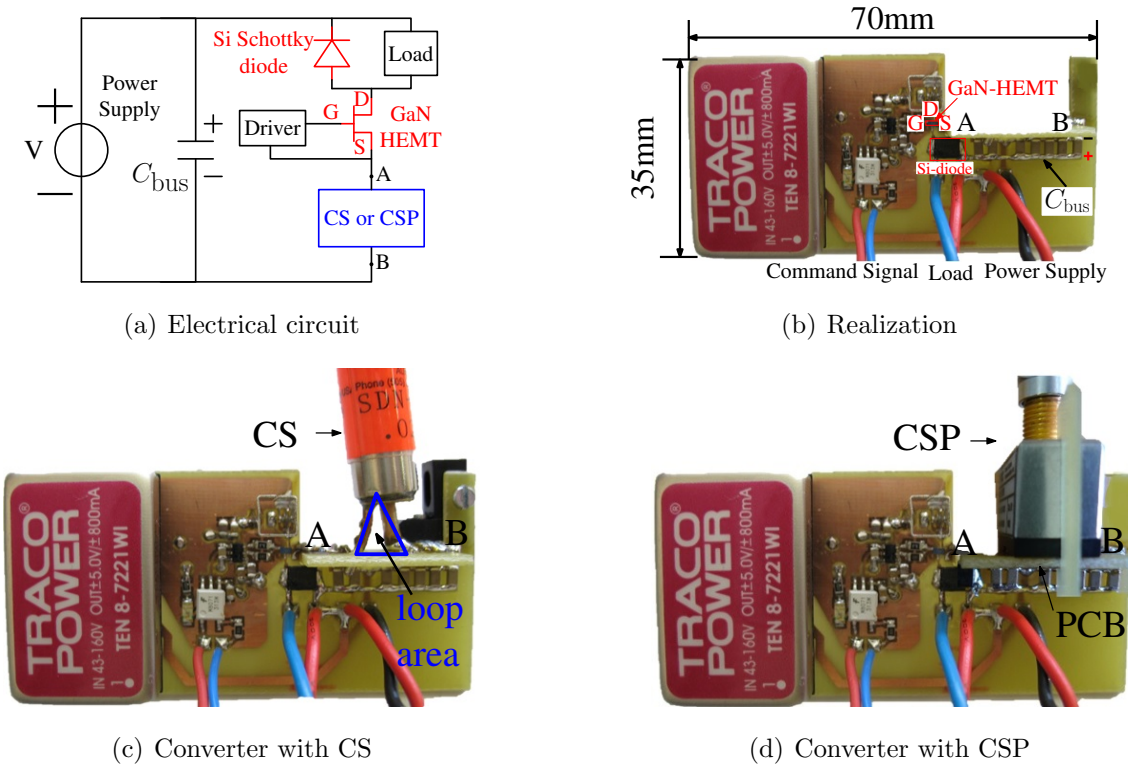
Measurement with CS and CSP

For this study, a buck converter (Figure 4.35(a)) with a GaN-HEMT (EPC2012) and Si Schottky diode (MBRS3200T3G) is designed with a specific PCB shown in Figure 4.35(b). Thus, the drain current flows from the source S of the power transistor to the negative end "-" of the DC-bus capacitors C_{bus}. Here, S and "-" are indicated as point A and point B respectively in Figure 4.35(b). Therefore, to measure I_D, either CS or CSP is connected from point A to point B as shown in Figure 4.35(c) and 4.35(d).

When CS is used to measure I_D current, the measurement equipment connecting points A and B shown in Figure 4.35(c) brings about $14nH$ parasitic inductance L_{para}, which is due to the connection pins and the internal parasitic inductance of the CS itself [108, 115]. Compared to that, with the measurement equipment shown in Figure 4.35(d), the CSP-mounted PCB brings only about $L_{para} = 4.5nH$ in the measurement circuit, which is less than with the CS.

It is shown in Figure 4.35(d) that the measured I_D switching current flows first through the top side of the PCB, then it flows to the negative end of the C_{bus} at the bottom side of the PCB. This design helps to minimize the L_{para} values in the power converter. The return current beneath the PCB track is in the opposite direction to that at the top side. According to the CSP transfer impedance characterization results presented in Chapter 4.2.1.2 "*Situation 2*", its transfer impedance in this

situation is characterized with the measurement configuration shown in Figure 4.26(a), in which the PCB is of the same geometry as that used in the buck converter.



(a) Electrical circuit

(b) Realization

(c) Converter with CS

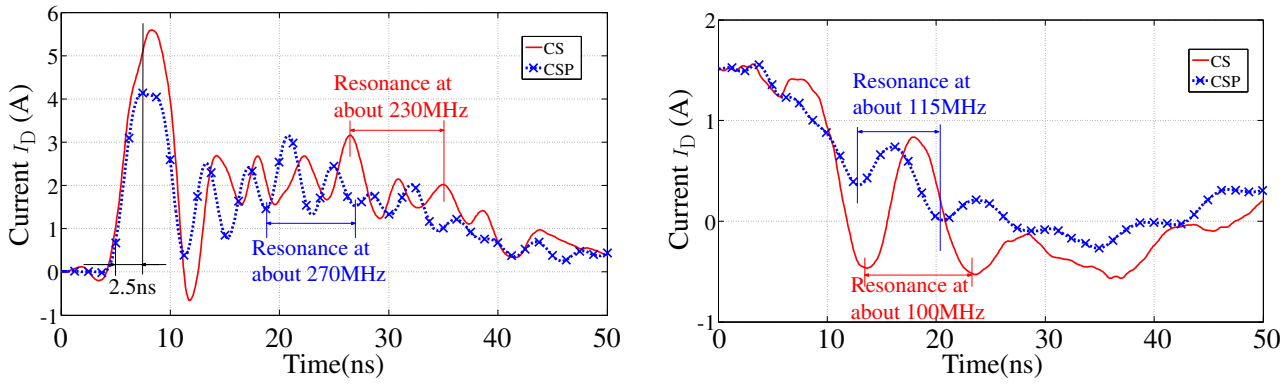
(d) Converter with CSP

FIGURE 4.35: GaN HEMT buck converter

The power converter switching condition is double-pulse test. The width of the pulse is controlled to have a switching current about 1.5A. The switching voltage (V_{DS}) is 50V. In the turn-on switching current shown in Figure 4.36(a), the measured current rise time by CSP and CS is almost the same, which is about 2.5ns. An almost same resonance amplitude above 200MHz at the end of the turn-on switching is represented both by CSP and CS. In the turn-off switching current shown in Figure 4.36(b), except for the resonance amplitude at around 100MHz, the current waveform measured by CSP is similar to that measured by CS. All the above results prove that CSP is able to measure the fast switching current of a few nanoseconds as well as the CS, and its transfer impedance characterization results presented in Figure 4.26(b) can be validated.

The main difference between the measured current waveforms is that there is more peak current amplitude measured by CS than CSP both in turn-on and turn-off switchings. This difference is mainly due to the difference in current measurement circuit of CS and CSP. It is to be noted that in Figure 4.35(c), the CS creates a loop area which might capture the high frequency interferences. As shown in the resonance frequency in Figure 4.36, that measured by CS is lower than that measured by CSP, which shows more parasitic inductances brought by the CS than CSP in the power device switching mesh, thus it gives rise to more current resonance amplitude. CS and CSP could be simultaneously inserted in the power converter to measure the exact same switching current, however,

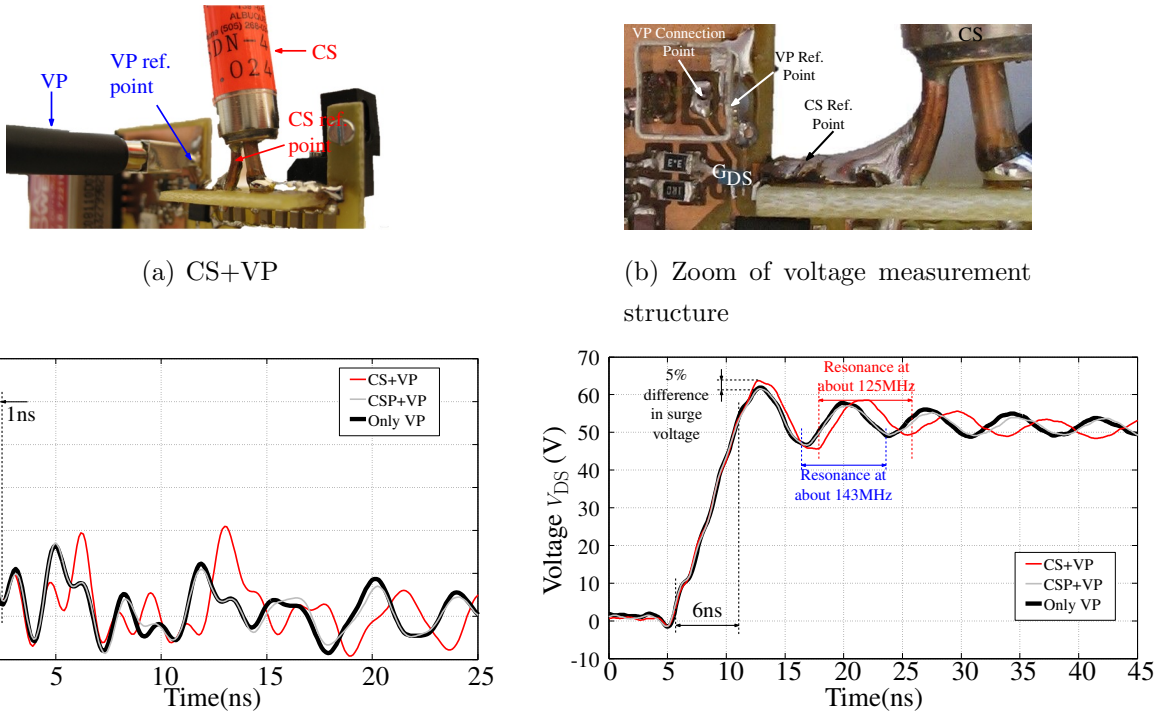
L_{para} would be increased in the GaN HEMT switching mesh and it might slow down the current transition times in this situation.



(a) I_D at turn-on

(b) I_D at turn-off

FIGURE 4.36: GaN HEMT switching current waveform measurement results with CS and CSP



(a) CS+VP

(b) Zoom of voltage measurement structure

(c) Turn-on

(d) Turn-off

FIGURE 4.37: GaN HEMT V_{DS} switching voltage measurement and results

The lower insertion impedance of the CSP can be also proved by measuring turn-off voltage waveform. For this reason, V_{DS} is measured by the presented passive voltage probe (VP) in the following conditions: first case, there is CS and VP in the measurement circuit (shown in Figure 4.37(a)); second case, there is CSP and VP in the measurement circuit and third case, there is only VP. It is to be noted that special cautions are necessary when both VP and CS are used together, because both of them bring the connection of the oscilloscope ground in the measurement power circuit. On the contrary, the use of CSP does not have the ground connection drawback. In order to minimize

voltage probe measurement loop, a special connection shown in Figure 4.37(b) was designed for the measurement.

The measured V_{DS} switching voltage waveforms at each condition are shown in Figure 4.37. It can be seen in Figure 4.37(d) that the use of CS causes a 5% more V_{DS} turn-off surge voltage than CSP for the voltage rise time about 6ns. This difference will be further increased if the voltage switching time is further shortened. The use of CS also causes a lower turn-off resonance frequency than that of CSP. The above results prove that the use of CSP brings less L_{para} than CS in the measurement circuit. It can be also observed that the use of CSP does not modify V_{DS} switching voltages, even in the case that the V_{DS} turn-on switching time is about 1ns. This result confirms the measurement results in Figure 4.21(c) that the advantage of the CSP is that it brings almost no insertion impedance in the measurement circuit.

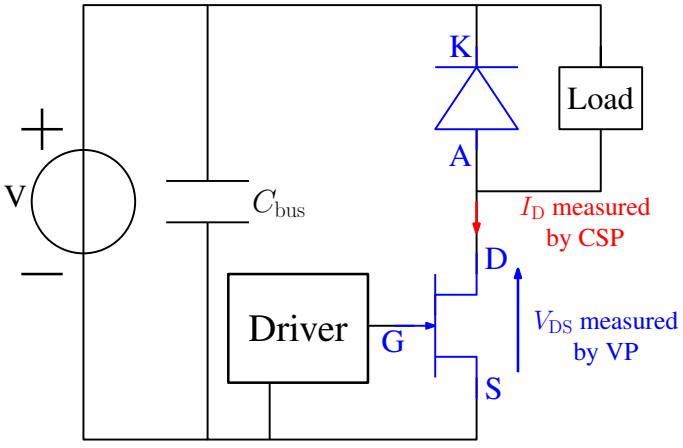
The presented CSP in this section will be used to measure SiC JFET fast switching current in order to validate the model presented in Chapter 3.

4.3 SiC JFET Model Validation

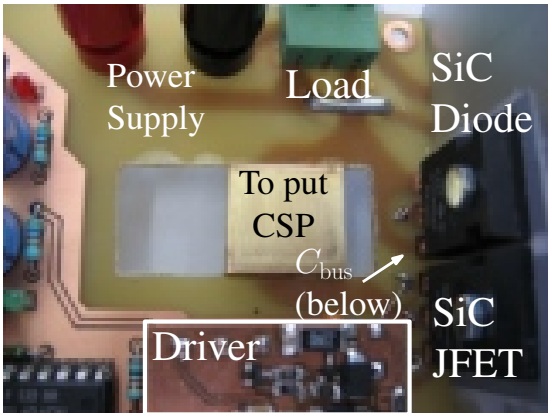
In this section, the SiC JFET switching mesh will be presented and modeled at first, then SiC JFET switching current in different switching conditions between simulation results obtained from the model presented in Chapter 3 and the measurement data will be compared.

4.3.1 Commutation mesh

A buck converter of the circuit shown in Figure 4.38(a) is used to measure SiC JFET switching current waveform.



(a) Switching circuit



(b) Photo of the realization

FIGURE 4.38: SiC JFET Buck converter circuit and photo

It is mainly constituted by a bus capacitor C_{bus}, a load (which is the same as presented in Figure 4.3(a)) , a SiC diode (CSD20060D) and the presented SiC JFET (SJEP120R063) with its driver circuit. The driver circuit of the SiC JFET is the same as presented in Figure 1.30 [14, 87]. The photo of the power converter is shown in Figure 4.38(b). SiC JFET drain current I_{D} is measured by the presented CSP and drain source voltage V_{DS} is measured by the same VP used in Figure 4.33, of which the input capacitance value is about 9.5pF. The bandwidth of the 12-bit measurement oscilloscope is 600MHz.

The measurement results of the C_{bus} impedance is shown in Figure 4.39. It can be represented by the equivalent circuit shown in Figure 4.2(b), in which the values of R, C and L are obtained by the fitting method: $R = 9m\Omega, C = 4.3\mu\text{F}, L = 4.2n\text{H}$. The model of the C_{bus} is compared with the measurement in Figure 4.39, in which it is shown that the model corresponds well with the measurement.

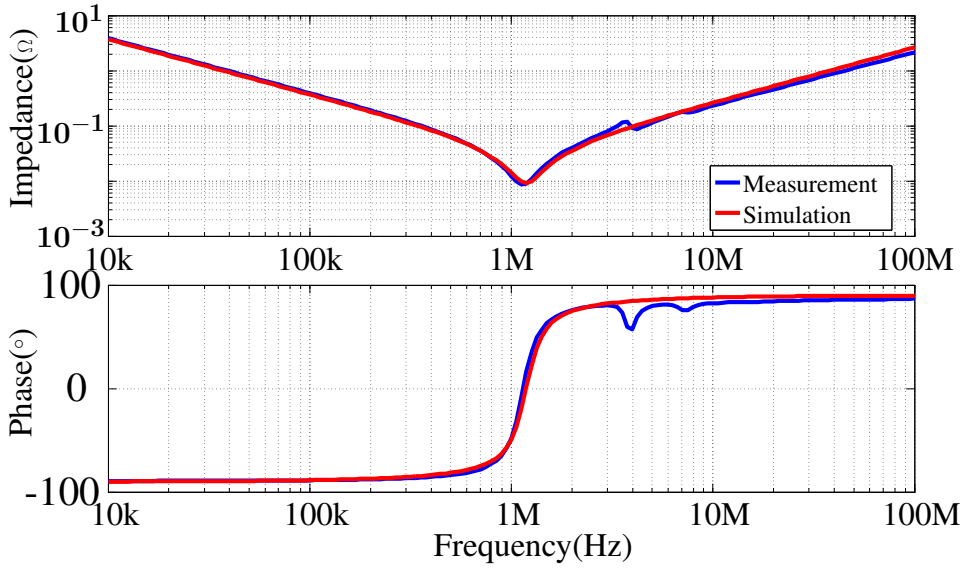


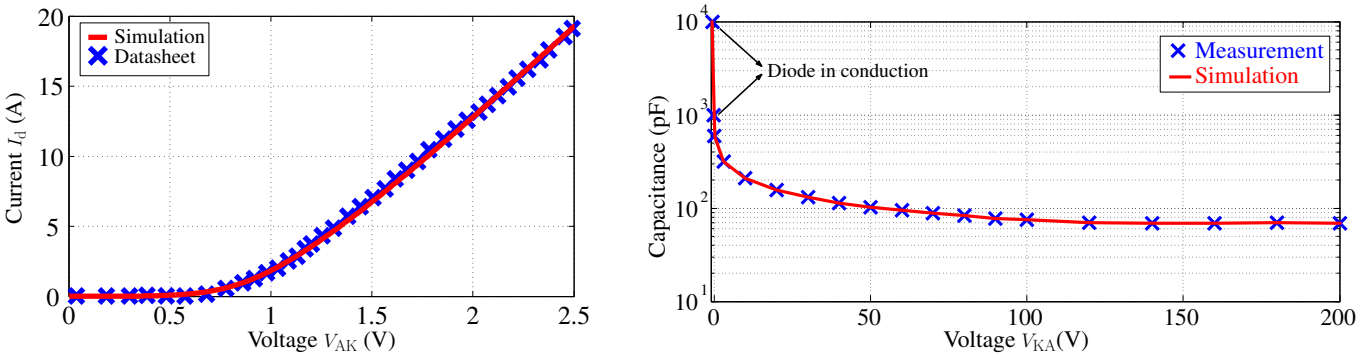
FIGURE 4.39: Comparison of C_{bus} impedance between the measurement and the model

The diode is modeled with the equivalent circuit shown in Figure 3.6, in which both $R_{1\text{s}}$ and $R_{2\text{s}}$ represent the diode static characteristics. The function to express I_{d}-V_{AK} is already shown in eq.(3.22), in which the value of c represents $R_{2\text{s}}$ value. As the presented diode is a SiC Schottky diode, there is almost no reverse recovery charge during the diode turn-off switching. The stored capacitive charges when diode in conduction are swept rapidly by the reverse current, thus a relatively small and constant $R_{2\text{s}}$ value is sufficient to express this phenomena. The values of a, b, c in eq.(3.22) are obtained by fitting method and they are[3]: $a = 651, b = 0.123, c = 0.07$. The comparison between the model of the static characteristic and the datasheet values are shown in Figure 4.40(a).

The junction capacitance C_{j} is modeled in the same way by a voltage-controlled current source presented in Chapter 3.1.4. The comparison between the measurement and the model of the dynamic characteristic are shown in Figure 4.40(b).

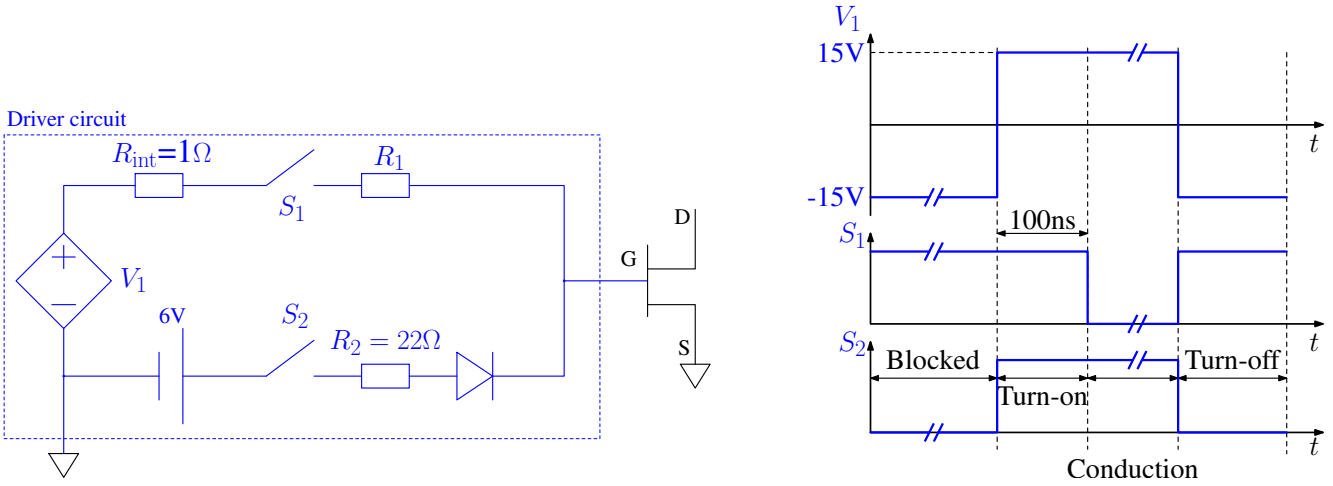
[3]The units of the parameters are: a(A^{-1}), b(V) and c(Ω).

The driver circuit of the SiC JFET presented in Figure 1.30 can be modeled by the circuit shown in Figure 4.41(a). It is constituted by three controlling devices: V_1, S_1 and S_2. The signals of these controlling devices are shown in Figure 4.41(b), which represents the function of the monostable in the driver circuit in Figure 1.30. The driver internal resistance R_{int} is 1Ω.



(a) Static characteristic (b) Dynamic characteristic

FIGURE 4.40: SiC diode characteristics and modeling



(a) Driver circuit (b) Signals

FIGURE 4.41: SiC JFET driver circuit modeling

In the next section, the presented passive component models are to be used in the circuit simulation in order to validate SiC JFET switching current and voltage waveforms by the measurement.

4.3.2 Measurement results

4.3.2.1 Results of different switching conditions

In the buck converter shown in Figure 4.38(a), the SiC JFET switching current I_{D} and switching voltage V_{DS} are measured in the following conditions: the input voltage V = 120V, the output current I_{L} = 10A and the power transistor switches at 100kHz.

The simulation circuit is shown in Figure 4.42, in which the C_{bus} model, VP model, driver circuit model and SiC diode model are those presented in the above Chapter 4.3.1, the load model is that presented in Chapter 4.1.1. The measured $L_{\text{para1}} = 25n\text{H}$, $L_{\text{para2}} = 15n\text{H}$, $L_{\text{driver}} = 36n\text{H}$, $L_{\text{diode}} = 4n\text{H}$ represent parasitic inductances in the power converter and the driver circuit. The estimated $L_{\text{d}} = 2n\text{H}$ and $L_{\text{s}} = 6n\text{H}$ represent parasitic inductances inside the power transistor packaging. The gate parasitic inductance can be neglected in comparison with L_{driver}, thus only internal gate resistor R_{g} which presented in Chapter 3.2.4 is added in the simulation circuit. The model of the SiC JFET is its behavioral model presented in Chapter 3.2.

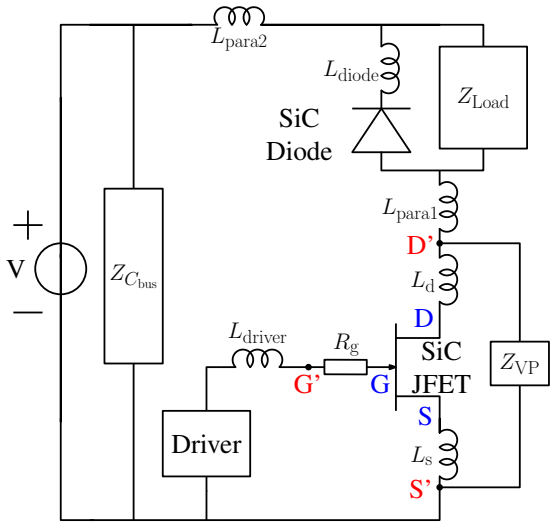
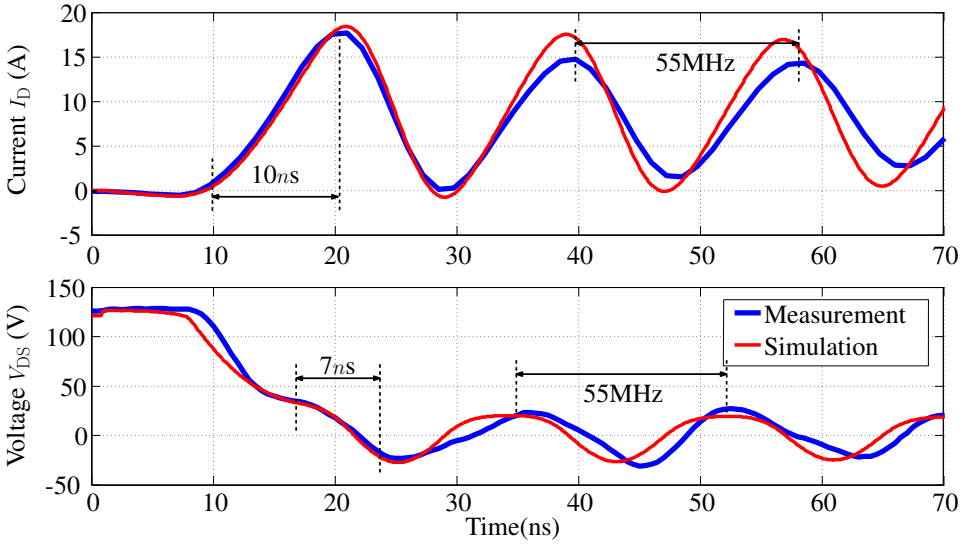


FIGURE 4.42: Simulation circuit of the SiC JFET Buck converter

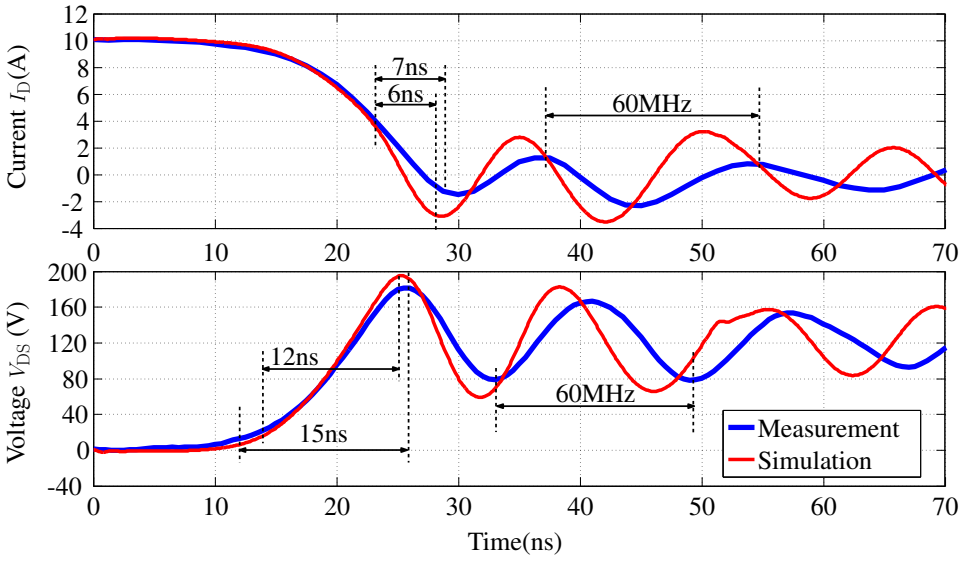
When the resistor R_1 in Figure 4.41(a) is 1Ω, the comparison of I_{D} switching current and V_{DS} switching voltage between the simulation and the measurement results are shown in Figure 4.43.

It is shown in Figure 4.43(a) the comparison of turn-on switching, that the I_{D} rise time is about $10n$s and the V_{DS} fall time is about $7n$s. The simulation corresponds well with the measurement results on the above I_{D} and V_{DS} switching times. The measured resonance frequency at the end of the turn-on is about 55MHz, which is correctly expressed by the model.

It is shown in Figure 4.43(b) the comparison of turn-off switching, that the V_{DS} rise time of the measurement is about $15n$s and that of the simulation is about $12n$s. While the I_{D} fall time of the measurement is about $7n$s and that of the simulation is about $6n$s. The relative error between the simulation and the measurement is about 20% on V_{DS} switching and 14% on I_{D} switching, which shows that the switching time of the measurement is generally well expressed by the model in simulation. The measured resonance frequency at the end of the turn-off is about 60MHz, which is correctly expressed by the model.



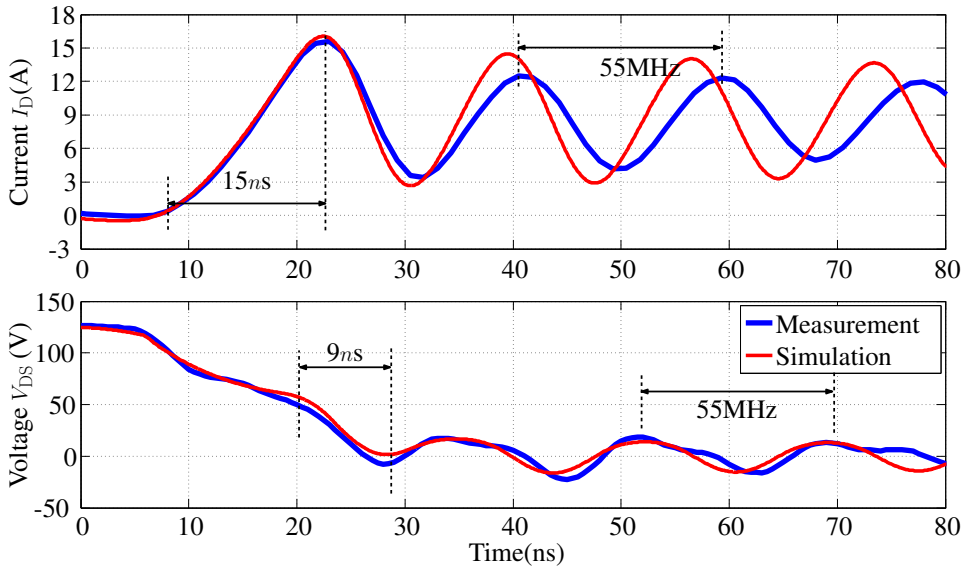
(a) JFET turn-on



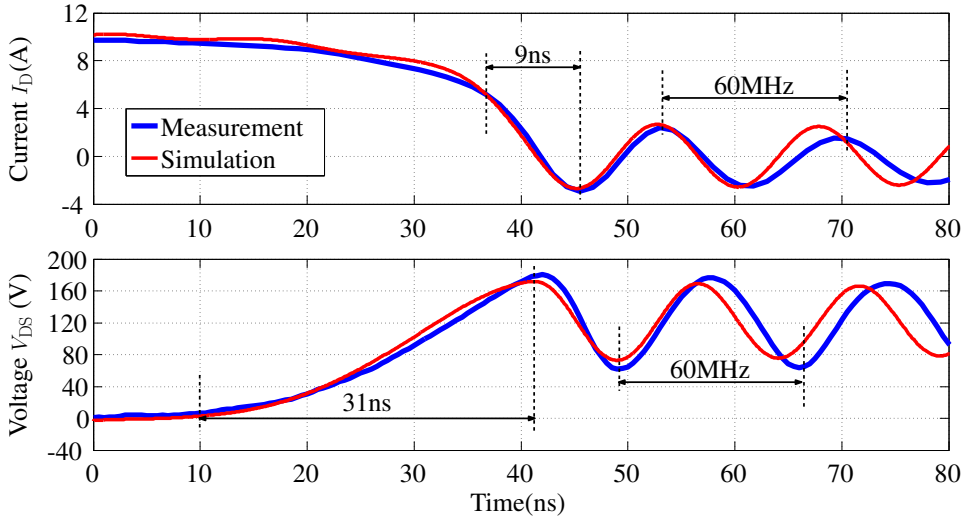
(b) JFET turn-off

FIGURE 4.43: Comparison between the simulation and the measurement results when $R_1 = 1\Omega$

In order to test the model robustness, the simulation results are now compared with measurement in another switching condition when R_1 (Figure 4.41(a)) is 10Ω, which will show down the commutation process. The results are shown in Figure 4.44. It is shown that the I_D rise time of the model is about 15ns in turn-on switching, which is almost the same as in the measurement; while the V_{DS} fall time of the model is about 9ns in turn-on, which corresponds well with the measurement. The model also corresponds well with the measurement on resonance frequency at the end of the turn-on switching. It is shown in Figure 4.44(b) that the V_{DS} rise time of the model is about 31ns in turn-off switching, which is almost the same to the measurement; while the I_D fall time is about 9ns in turn-off switching, which corresponds well with the measurement. The model also corresponds well with the measurement on resonance frequency at the end of the turn-off.



(a) JFET turn-on

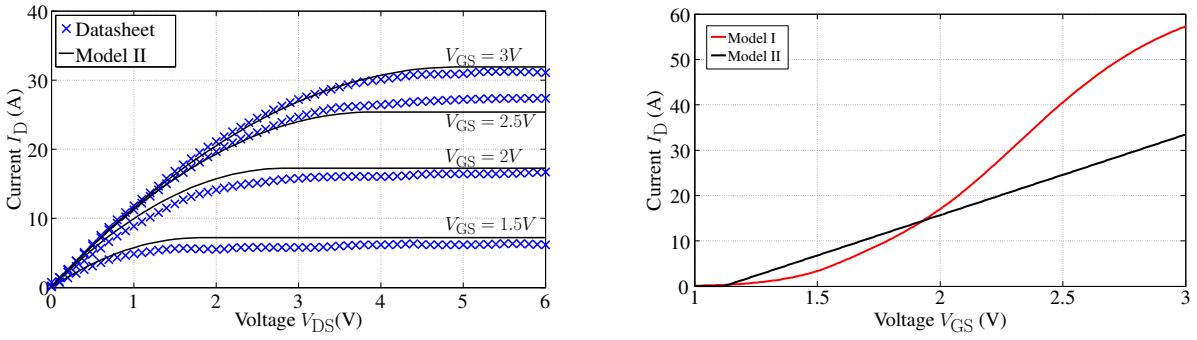


(b) JFET turn-off

FIGURE 4.44: Comparison between the simulation and the measurement results when $R_1 = 10\Omega$

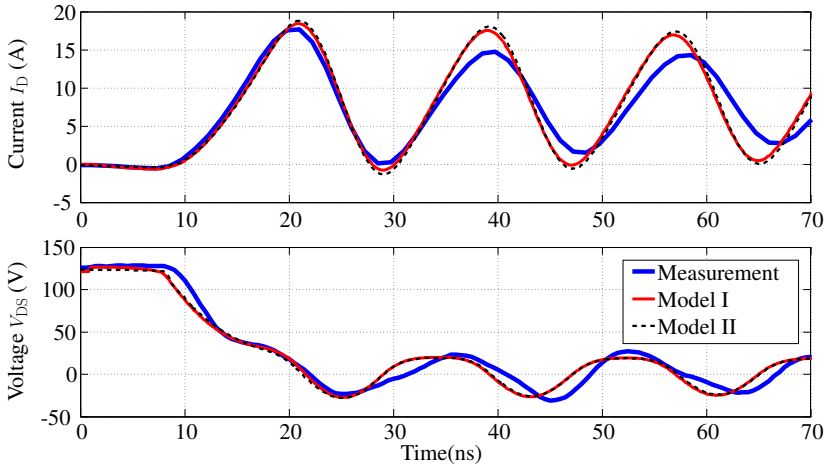
4.3.2.2 Comparison between different models

The presented SiC JFET behavioral model (indicated as model I) in Chapter 3.2 can be validated according to those measurement results. To further research on whether datasheet information is sufficient to make a power device model, another SiC JFET behavioral model (indicated as model II) is made with the same equivalent circuit shown in Figure 3.28, in which the current generator and C_{gd}, C_{gs} are modeled with the values given in its technical datasheet. The comparison of the SiC JFET static characteristics between the model II and the datasheet is shown in Figure 4.45(a). The comparison of the power transistor transconductance is shown in Figure 4.45(b) between model I and model II. It is shown in Figure 2.18(c) that C_{gd} and C_{gs} values in the datasheet corresponds well with their measurement values, thus their values when $V_{GS} = 0V$ are used in the model.

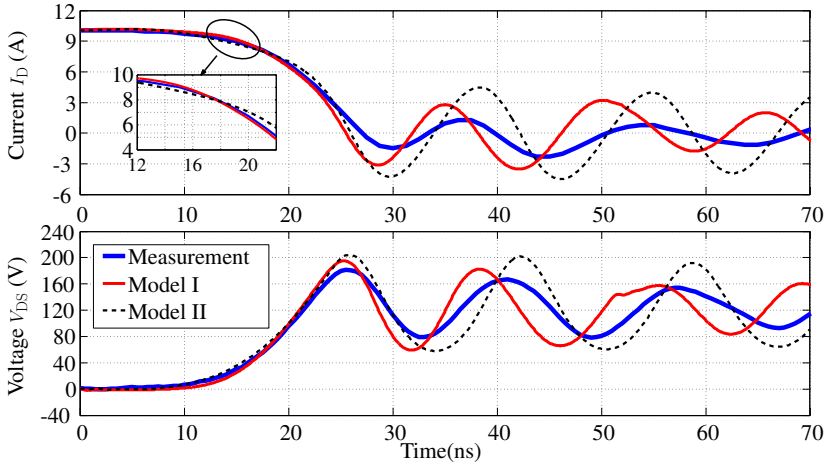


(a) Static characteristics (b) Transconductance

FIGURE 4.45: Comparison of the SiC JFET static characteristics among the model II, model I and the datasheet



(a) Turn-on



(b) Turn-off

FIGURE 4.46: Comparison among the model II, model I and the measurement when $R_1 = 1\Omega$

The compared switching waveforms of the two models with the measurement are shown in Figure 4.46 when $R_1 = 1\Omega$. It is shown in Figure 4.46(a) that the model II reproduces almost the same switching waveforms to the model I at turn-on switching. However, at turn-off switching, the model II does not reproduce a satisfying dv/dt as well as the model I. Besides that, the model II reproduces a

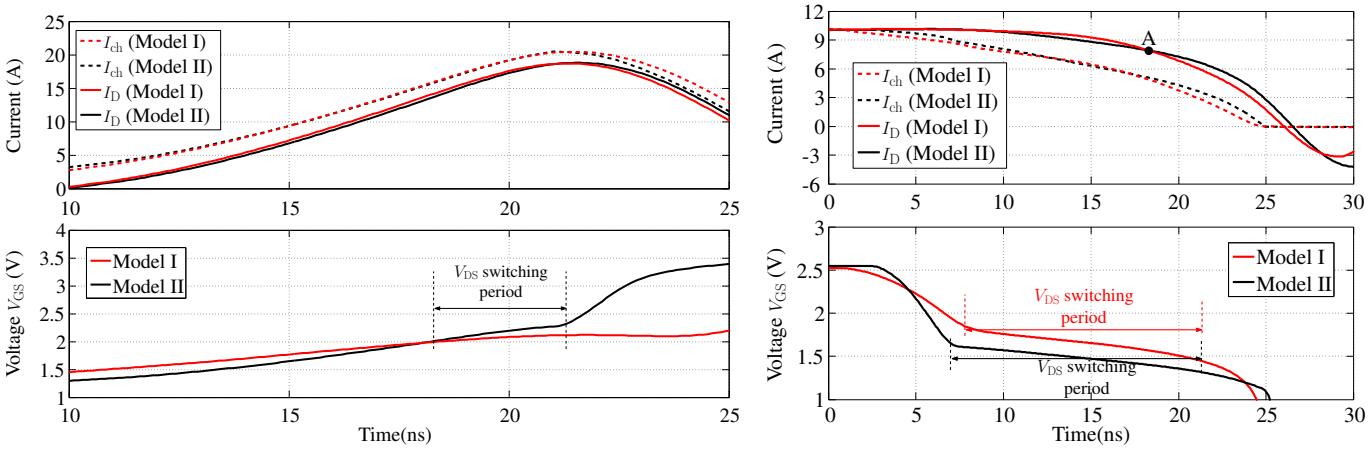
bigger resonance amplitude than model I at the end of the turn-off switching. In summary, model II is as good as model I at turn-on switching, but worse than model I at turn-off switching.

To further research this similarity and difference between the two models, the SiC JFET channel current I_{ch} and V_{GS} of the two models during the switching are compared in Figure 4.47. It is shown in Figure 4.47(a) that during the turn-on switching, I_{ch} is bigger than I_D, because the rise of I_D causes a drop of voltage $L_{para}\frac{dI_d}{dt}$ across the SiC JFET, thus C_{gd} begins to discharge at the same moment and I_{ch} equals to the sum of I_D and C_{gd} discharge current $I_{C_{gd}}$. As shown in Figure 3.48, C_{gd} values in model I is similar to its values in model II at high V_{DS} voltage, thus $I_{C_{gd}}$ current at turn-on switching is almost the same in both model I and model II, which results an almost same current turn-on switching waveform in two models. The V_{DS} switching slope of the SiC JFET can be approximately calculated by the following equation based on the switching waveforms presented in Figure 1.23(b) and the driver circuit shown in Figure 4.41:

$$\begin{aligned} I_G &\approx -C_{gd}(V_{DS})\frac{dV_{DS}}{dt} \\ I_G &= \frac{V_{com}-V_{pl}}{R_1} \end{aligned} \tag{4.7}$$

where V_{com} is the command voltage value in Figure 4.41 and it equals to 15V at SiC JFET turn-on, and V_{pl} is the Miller plateau voltage value and it is about 2V shown in simulation (Figure 4.47(a)), thus the difference of I_G is tiny between the two models. It is explained in the above paragraph that C_{gd} values at high V_{DS} voltage is similar in both two models, so $\frac{dV_{DS}}{dt}$ slope yielded by the two models are almost the same in the simulation.

It is shown in Figure 4.47(b) that during the turn-off switching, I_{ch} is smaller than I_D, because during the rise of V_{DS}, one part of I_D begins to charge C_{gd} and I_{ch} equals to the difference of I_D and C_{gd} charge current $I'_{C_{gd}}$. According to the results shown in Figure 3.48, C_{gd} values in model I can be twice bigger than its values in model II, so at the beginning of the turn-off, V_{GS} drops faster and V_{DS} rises faster in model II than model I, which yields a bigger I_D current drop in model II than in model I until point A shown in Figure 4.47(b). This I_D current drop is due to the $C_{diode}\frac{dV_{DS}}{dt}$, which is already illustrated in Figure 1.23(b). Eq.(4.7) can still be used to approximately calculate V_{DS} slope at turn-off and V_{com} is -15V at this time. With the increase of V_{DS} voltage, the difference of the C_{gd} values between two models is tiny. Shown in Figure 4.47(b), V_{pl} value in model I is bigger than that of model II, which yields a bigger I_G current in model I than in model II during V_{DS} switching. V_{DS} slope in model I is thus bigger than that in model II at the end of the V_{DS} switching, which causes an intersection point A in Figure 4.47(b).



(a) Turn-on (b) Turn-off

FIGURE 4.47: Comparison of the two models on V_{GS}, I_D and I_{ch} switching waveforms

It is also shown in Figure 4.47 that switching losses can not be simply calculated by integrating measured switching current I_D and switching voltage V_{DS}. The presented power transistor behavior model can be used to calculate switching power losses, because I_{ch} current can be obtained in simulation.

It is explained by the above analysis that model I represents well V_{DS} turn-off switching voltage compared with model II. The difference of the two models on resonance amplitude at the end of the turn-off switching can be explained with the following analysis.

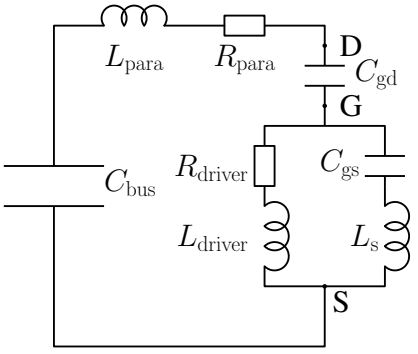


FIGURE 4.48: Equivalent circuit to express resonance loop at the end of the SiC JFET turn-off

The LC resonance at the end of the SiC JFET turn-off observed both in I_D current and V_{DS} voltage is due to the resonance between total parasitic inductance of the switching mesh L_{para} and C_{gd} of the SiC JFET[4]. Based on the simulation circuit shown in Figure 4.42, an equivalent circuit shown in Figure 4.48 can be used to express the LC resonance loop at the end of the SiC JFET turn-off. G and S is connected by two circuits, one of which is the SiC JFET driver circuit with the total gate resistor R_{driver} and driver circuit parasitic inductance L_{driver}; another is the inter-electrode capacitance C_{gs} with L_s. At the end of the turn-off, V_{GS} voltage value equals almost to the V_{com} voltage value, which

[4]It is usually the LC resonance between L_{para} and C_{oss}, however the C_{ds} of the JFET can be neglected as presented previously.

is -15V. C_{gs} evolution on V_{GS} (shown in Figure 3.34(b)) is included in model I, of which C_{gs} value when $V_{GS} = -15V$ is smaller than its value when $V_{GS} = 0V$. Therefore, at the end of the turn-off, the impedance of the C_{gs} in model I is bigger than that in model II, so more resonance current passes through R_{driver} in model I than model II and it is attenuated by the gate resistor. The same analysis can explain that the measured resonance amplitude in Figure 4.44(b) when $R_1 = 10\Omega$ is bigger than that in Figure 4.43(b) when $R_1 = 1\Omega$. When $R_1 = 10\Omega$, more resonance current passes through C_{gs}, so it is less attenuated.

To validate the above analysis, turn-off switching waveforms of the following three models are compared: the presented model I; model Ia, which is with the measured SiC JFET static characteristics, C_{gd} evolution on both V_{DS} and V_{GS} voltages and C_{gs} with its values when V_{GS}=0V; model Ib, which is with the measured SiC JFET static characteristics, C_{gs} evolution on V_{GS} voltage and C_{gd} with its values when V_{GS}=0V. The comparison results are presented in Figure 4.49.

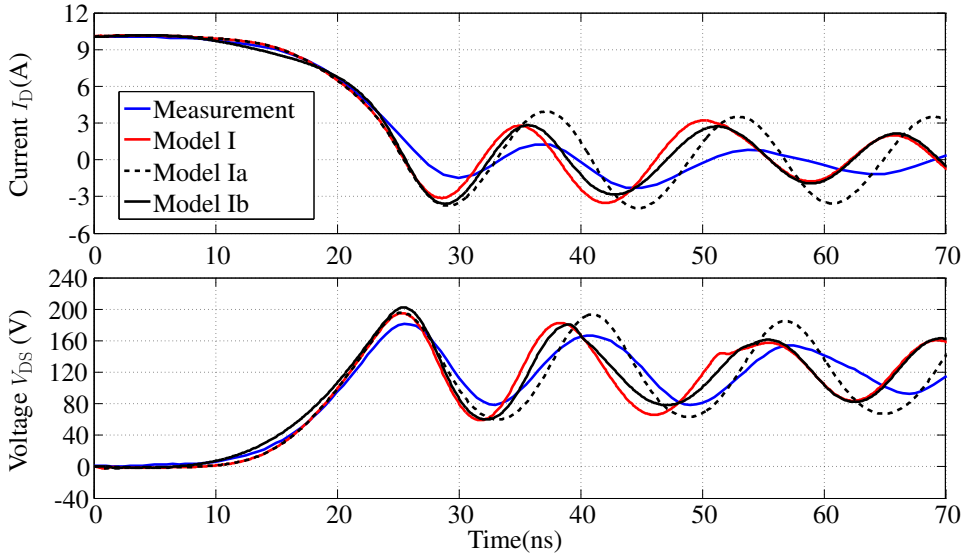
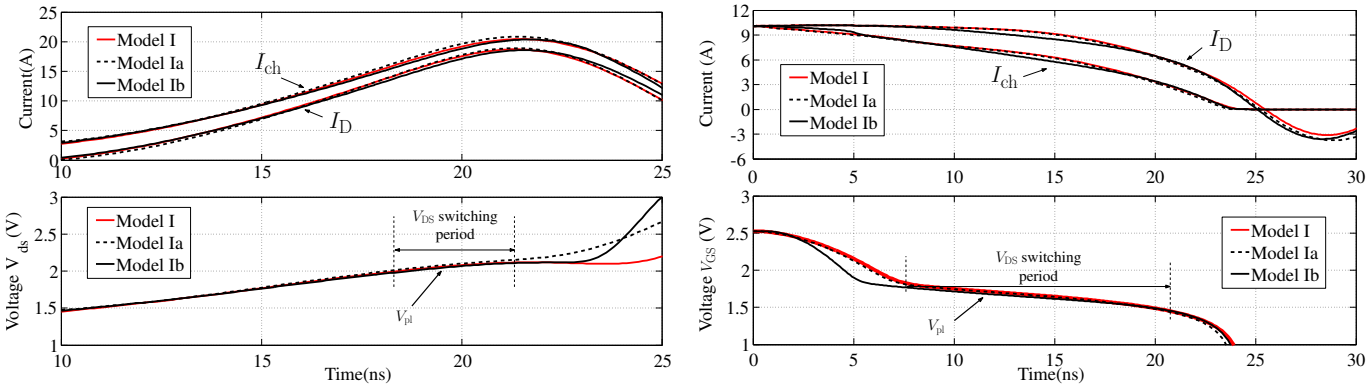


FIGURE 4.49: Comparison of model I, model Ia and model Ib on SiC JFET turn-off

It is shown in Figure 4.49 that model Ia represents the turn-off V_{DS} switching waveform as well as model I, but yields a bigger turn-off resonance amplitude than model I; while model Ib represents the turn-off resonance amplitude as well as model I, but yields a less accurate V_{DS} turn-off slope. The above analysis can be validated through those results.

4.3.2.3 Relation between inter-electrode capacitance values and V_{pl} value

Following analysis is done to further research on the relation between power device inter-electrode capacitances values and V_{pl} value. It is shown in Figure 4.50 that there is a same V_{pl} value obtained by model I, model Ia and model Ib during V_{DS} switching both in SiC JFET turn-on and turn-off. It is shown in Figure 4.51 a simplified equivalent circuit to analyze power transistor switching, in which the power transistor is represented by a current generator with three inter-electrode capacitances C_{gs}, C_{gd} and C_{ds} and the driver circuit is modeled by a voltage source V_{com} with a gate resistor R_G.



(a) Turn-on (b) Turn-off

FIGURE 4.50: Comparison of the three models on V_{GS}, I_D and I_{cH} switching waveforms

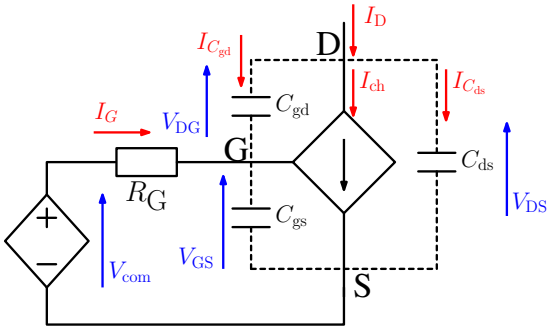


FIGURE 4.51: Equivalent circuit to analysis power transistor switching

Supposing that during the V_{DS} switching, V_{GS} voltage value is almost constant and it equals to the V_{pl} value, then following equations can be obtained:

$$\begin{aligned} I_{ch} &= I_D - I_{C_{gd}} - C_{ds} \\ I_{C_{gd}} &= C_{gd}\frac{dV_{DG}}{dt} = C_{gd}\left(\frac{dV_{DS}}{dt} - \frac{dV_{GS}}{dt}\right) = C_{gd}\frac{dV_{DS}}{dt} \\ I_{C_{ds}} &= C_{ds}\frac{dV_{DS}}{dt} \end{aligned} \tag{4.8}$$

During the V_{DS} switching, V_{pl} is almost constant, so $I_G = -I_{C_{gd}}$ as indicated in Figure 4.51. By combining eq.(4.7) with (4.8), following equations can be obtained:

$$\begin{aligned} \frac{V_{com} - V_{pl}}{R_G} &= -C_{gd}\frac{dV_{DS}}{dt} \\ \frac{dV_{DS}}{dt} &= -\frac{V_{com} - V_{pl}}{R_G C_{gd}} \end{aligned} \tag{4.9}$$

By combining eq.(4.10) with eq.(4.8), following equation can be obtained:

$$I_{ch} = I_D + \frac{V_{com} - V_{pl}}{R_G}\left(1 + \frac{C_{ds}}{C_{gd}}\right) \tag{4.10}$$

V_{pl} and I_{ch} are related by power transistor transconductance, which is shown in Figure 4.52. The relation between the two parameters is also revealed by eq.(4.10), which represents a curve shown in Figure 4.52. It is shown in eq.(4.10) that $V_{pl} = V_{com}$ and $I_{ch} = I_D$ is one solution of the equation, thus this curve passes at the point (V_{com}, I_D) and the slope is $-\frac{1}{R_G}\left(1 + \frac{C_{ds}}{C_{gd}}\right)$. For power transistor turn-on, the intersection point X of the power transistor transconductance curve and eq.(4.10) determines the V_{pl} value during the V_{DS} falling. For power transistor turn-off, the same method can be used to calculate V_{pl} value during V_{DS} rising.

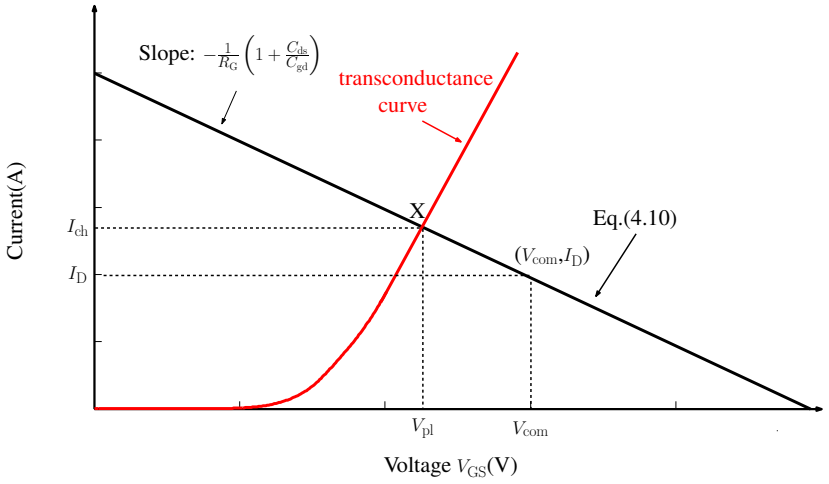


FIGURE 4.52: Relation between V_{pl} and I_{ch}

In the proposed SiC JFET behavioral model, inter-electrode capacitance C_{ds} value is 0 in the model, thus the slope of the eq.(4.10) in Figure 4.52 is only determined by R_G. This result shows that at this condition the intersection point X in Figure 4.52 is not determined by power device inter-electrode capacitance values, which proves the case that all model I, model Ia and model Ib produce a same V_{pl} value in the simulation during the power device switching. It is also proved by the above analysis that for a power transistor in which C_{ds} value can be neglected in comparison with C_{gd} value, the dynamic characteristics of the power transistor has less influence on the precision of the power device model to reproduce power device switching waveforms in comparison with a power transistor in which C_{ds} value can not be neglected.

4.4 Discussion

It is presented in this chapter the power device behavior models validation and fast switching current measurement methodology. There are the following issues which are necessary to be discussed.

HECP, CSP characterization

It is shown in Figure 1.42 that HECP maximum measurement current decreases when frequency increases, thus HECP transfer function is determined by at least two parameters: frequency and current amplitude. The HECP transfer function in Chapter 4.1.2 is measured at one current amplitude by the proposed characterization method. Its dependency on current amplitude is not included in the obtained transfer function. The proposed method can be applied to characterize HECP transfer function at different current amplitudes in order to get its transfer function on different frequency and different current amplitude.

The current surface probe (CSP) is a passive probe and it is not verified that its transfer impedance is influenced by the measured current amplitude. The presented characterization method in Chapter 4.2.1.2 can be applied to characterize CSP transfer impedance in different current amplitude in order to further research on this aspect.

The use of CSP does not bring the ground connection problem. However, its metal part shown in Figure 1.44(a) is connected with the oscilloscope ground when it is in use, which brings a parasitic capacitance between the ground and the PCB track that is shown in Figure 4.53. Its value is characterized in the impedance analyzer and is about $4pF$. Special connection may still be necessary if CSP is used together with ground connection equipment in fast switching power converters.

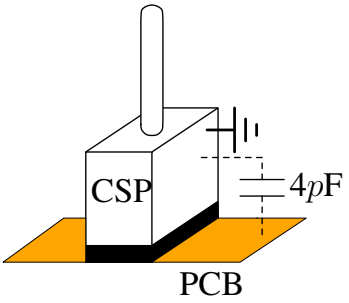


FIGURE 4.53: Parasitic capacitance brought by the CSP in the circuit

Model validation

The proposed SiC JFET behavioral model can correctly represent the di/dt and dv/dt at different operation conditions. The main difference between the model and the measurement is the resonance amplitude observed in Figure 4.43 and in Figure 4.44. There are the following two possible aspects to further improve the precision of the presented model:

1. The parasitic inductance L_{para} of each PCB track in the power converter is measured separately by impedance analyzer and they are added in the simulation circuit to validate power device models. However, the mutual effect between each parasitic inductance is not included in the simulation circuit. This coupling effect may modify the total L_{para} values in the power converter,

thus influence the resonance amplitude and frequency. To represent this coupling effect, it is necessary to calculate the parasitic inductances in the power circuit by a specific software: for example, Q3D, which is based on method of moments; InCa3D, which is based on the partial element equivalent circuit (PEEC) or Flux, which is based on finite element method.

2. The proposed power transistor model is mainly constituted by a current generator with three inter-electrode capacitances as shown in Figure 4.51 (only C_{gs} and C_{gd} for SiC JFET). Authors in [124] present another equivalent circuit with more precision to model a RF HEMT, in which inter-electrode capacitances C_{gd} and C_{gs} are in series with a resistor $R_{C_{\mathrm{gd}}}$ and $R_{C_{\mathrm{gs}}}$. The model is illustrated in Figure 4.54. This model can thus be validated at different gate bias voltage values. It is to be noted that although this is a model of a RF transistor, the addition of $R_{C_{\mathrm{gd}}}$ in the model can help to decrease resonance amplitude at the end of the turn-off switching in the simulation, which makes the model closer to the measurement. This modeling method can be inspired and applied to model a power semiconductor transistor. $R_{C_{\mathrm{gd}}}$ and $R_{C_{\mathrm{gs}}}$ values can be obtained by the presented multi-current-probe method.

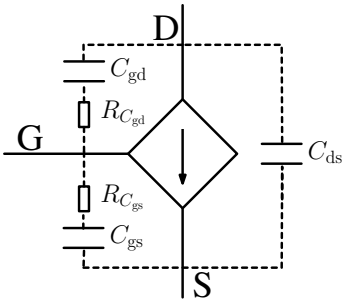


FIGURE 4.54: Power transistor model with resistances in series with inter-electrode capacitance

It is shown in Figure 4.50 the difference of the V_{GS} voltage waveform of the three models. V_{GS} voltage waveform comparison can be also a criteria to validate the model. It is important to research on power device intelligent driver circuits design, in order to control $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ as an example, by using a power device model which is able to reproduce a reliable V_{GS} voltage.

4.5 Conclusions

In this chapter, the diode behavioral models are at first compared with the measurement on reverse recovery current. It is shown that as diode capacitance C values can not be correctly characterized when it is in ON-state, the maximal reverse recovery current I_{rrm} can not be correctly represented by the model.

The first approach is to increase the values of C when diode in ON-state, so that the model can represent well I_{rrm} value at one switching condition. It is shown in the results that the improved model is validated to represent well both I_{rrm} and reverse recovery time t_{rr} at different switching

conditions. However, the main difference is that the t_{rr} of the model is about 30% shorter than the measurement. The second approach to further improve model performance is to increase R_2 values when diode is in OFF-state and to vary the introduced factor α when diode in ON-state. It is shown in the results that after the second approach, the performance of the proposed model is improved to represent well diode reverse recovery current at different switching conditions. It is also demonstrated the influence of the Hall effect current probe (HECP) transfer functions on the obtained switching current waveform in simulation.

To measure fast switching current, a current surface probe (CSP) is presented. With the advantage of small dimension and isolation, CSP creates a small commutation mesh in the circuit while bringing no connection to the ground of the measurement equipment. Its insertion impedance is first characterized to show its small insertion impedance less than $1nH$. Compared to the clamp-on passive current probe (CP) and active HECP, this advantage of CSP is that it hardly influences measurement configuration. Then, CSP transfer impedance is characterized with different PCBs to show its dependency on PCB track dimensions. It is also shown that a return current under the PCB on which is put the CSP can greatly reduce the CSP transfer impedance, so it is necessary to characterize its transfer impedance on the PCB with the same dimension and in the same situation as that in current measurement. CSP complex transfer impedance is used to compensate its measured current in frequency domain, and then the compensated current amplitude is converted into time domain via iFFT to have temporal current waveforms. By comparing with CP and HECP on IGBT collector switching current measurement, CSP transfer impedance characterization is verified. By comparing with a CP to measure GaN-HEMT I_{D} switching current and V_{DS} voltage, it is shown that CSP is able to measure fast switching current while having no influence on V_{DS} measurement. By comparing with a CS, it is demonstrated the return current influence on CSP transfer impedance and that CSP is able to measure fast switching current during a few nanoseconds as well as the CS. Furthermore, the use of the CSP brings less parasitic inductance than CS in the measurement circuit and it does not bring a ground connection drawback, which is the case for CS.

The CSP is then used to measure SiC JFET switching current in order to validate its behavioral model. It is shown in the results that the proposed model can represent correctly I_{D} switching current slope $\mathrm{d}i/\mathrm{d}t$, V_{DS} switching voltage slope $\mathrm{d}v/\mathrm{d}t$ and the resonance frequency at the end of the commutation at different switching conditions. The SiC JFET behavioral model based on the measured static and dynamic characteristics is compared with the model based on datasheet values. It is shown that the model with datasheet values can represent well the SiC JFET turn-on switching, but it is not as good as the model with the measured values to represent SiC JFET turn-off switching. It is analyzed that as C_{ds} of the SiC JFET is neglected in the model, the inter-electrode capacitance values of the power transistor has less influence on the precision of the model to reproduce power device switching waveforms in comparison with the one that C_{ds} value can not be neglected.

General Conclusions and Perspectives

The wide bandgap (WBG) power semiconductor devices are gradually applied in power converters to achieve high power efficiency, high power density. Their characterization and modeling are thus very important to better understand their characteristics to design high efficiency, high frequency power converters. This dissertation is mainly focused on characterization methods, WBG power devices modeling and fast switching current measurement in order to validate the models. The main results achieved in this dissertation can be reviewed through the following realized work.

Realized work

There are two main realized work in Chapter 2, one of which is the power device static characteristics measurement by single-pulse method. Characterization results of a SiC diode and a "normally-off" SiC JFET at different junction temperatures T_j from 25°C to 120°C are presented. The duration of the pulse is set to control junction temperature T_j constant in the measurement and the maximal power dissipation of the SiC JFET in the characterization is about 1700W. T_j is calculated during the SiC JFET characterization, which shows that it is almost constant.

Another realized work in Chapter 2 is to characterize power device dynamic characteristics by multiple-current-probe (MCP) method at high V_DS voltage. Using a simple setup, the proposed method provides the advantage of isolating the measurement equipments from the DC bias power source. In the two-current-probe method, the sum of the two inter-electrode capacitances can be measured at one measurement. Each capacitance value can then be calculated. By comparing with the datasheet, the results of C_iss and C_oss of a transistor are accurate, but the result of C_rss is not convincing, because of indirect calculation inducing measurement errors propagation. To overcome this inconvenience, a three-current-probe method is proposed to directly measure C_rss value. It is shown in the measurement results that this method offers a precise characterization of their inter-electrode capacitances in high voltage. The sensibility of the MCP method has been improved by adding more turns around current receiving probes to increase its coupling effect in order to measure

a few picofarad capacitance; and by using small current probes developed by L2EP to decrease measurement setup impedance in order to measure impedance values of several tens of milliohms around megahertz. Special measurement configuration is proposed to characterize power device in ON state without a continuous DC current passing through the small probes. Therefore, it is possible to apply the MCP method to characterize power devices when they are in OFF and ON state. Experimental results have been obtained and validated on several power devices of different technologies (Si diode, MOSFET and IGBT, SiC JFET, GaN HEMT).

Power device modeling, which is presented in Chapter 3, is another mainly realized work in the dissertation. Behavioral models of a Si power diode and a SiC JFET, which are based on their characterization results, are presented to be simulated in PSPICE. The Si power diode is modeled with its dynamic impedance measurement results, in which its impedance at one DC polarization point is measured by the previously presented two-current-probe method. It is shown that because of internal parasitic inductance L_{para} inside diode packaging, only total dynamic resistance value and L_{para} value are obtained when the diode is in conduction, and capacitance value can not be correctly characterized in this case. The obtained dynamic resistances values are then converted into their static resistances values, which are further expressed by mathematical functions in the model. It is shown that there are two non-linear resistances in the presented diode model, in comparison with the PSPICE diode physical model in which there is only one non-linear resistance.

The static characteristic of the SiC JFET is obtained by single-pulse method, and they are represented by mathematical functions in the model. The dynamic characteristic of the power device is obtained by MCP method, in which inter-electrode capacitance values when power device is blocked and in linear region are characterized. When the power device is in linear region, the characterization results by the MCP method are verified by either impedance analyzer or by single-pulse characterization. It is shown that when the power device is blocked, its output capacitance value C_{oss} equals to its reverse transfer capacitance value C_{rss}. However, in linear region, the obtained apparent C_{oss} values are up to ten times bigger than C_{rss} values. The influence of the power transistor internal gate resistor R_{g} is thus studied, revealing the inter-electrode capacitances measurement problem when the power device is in linear region. It is shown that R_{g} can vary V_{GS} voltages during the characterization when power device in linear region, thus increase the characterized C_{oss} apparent capacitance values. The evolution of the inter-electrode capacitances values are then represented by different mathematical functions in the model.

Power device behavioral models are then validated with the measurement on switching current and voltage waveforms in Chapter 4.

First, diode behavioral models are compared with the measurement on reverse recovery current. As diode capacitance C values can not be correctly characterized when it is in conduction, it degrades the model to precisely express maximal reverse recovery current I_{rrm}. To improve the model, the

first approach is to increase the values of C when diode in conduction, in order to represent correctly I_{rrm} value at one switching condition. After this approach, the diode model is validated to be robust to represent I_{rrm} values of different switching conditions, but yields an about 30% shorter time than the measurement on reverse recovery time t_{rr}. The second approach is to increase one non-linear resistance value. It is shown in the results that after the two approaches, the performance of the proposed model is well improved to represent correctly both I_{rrm} and t_{rr} at different switching conditions, which is better than a PSPICE diode physical model. It is also demonstrated the influence of the Hall effect current probe (HECP) transfer function on switching current waveforms.

In order to measure fast switching current, using a current surface probe (CSP) is proposed in the thesis. The advantage of the CSP is that it has small dimension and it brings a galvanic isolation with no connection to the ground of the measurement equipment. Following work have been realized in the dissertation to present how to use CSP to measure fast switching current. Its insertion impedance is first characterized to show its small insertion impedance less than $1n$H, thus it has no influence on V_{DS} voltage measurement while it is not the case for a clamped-on passive current probe (CP). Then, CSP transfer impedance is characterized on different situations to show that it is dependent on PCB track dimensions. It is also shown that CSP transfer impedance can be greatly reduced by a return current under the PCB on which is put the CSP. These results prove the necessity to characterize its transfer impedance on the PCB with the same dimension and the same situation used in current measurement.

The CSP transfer impedance is used to correct the measured current. The characterized results are validated by measuring simultaneously IGBT collector switching current with CP and HECP. By comparing with a CP and with a current shunt (CS) to measure GaN HEMT drain switching current, it is demonstrated that CSP is able to measure fast switching current during a few nanoseconds and it brings even less parasitic inductance than CS in the measurement circuit.

The proposed SiC JFET behavioral model is validated by comparing the simulation with the measurement, in which the switching current is measured by the CSP. It is shown in the results that the model is robust to reproduce $\mathrm{d}i/\mathrm{d}t$, $\mathrm{d}v/\mathrm{d}t$ and the resonance frequency of the measurement. The proposed model based on measured SiC JFET static and dynamic characteristics is better than the model with datasheet values to reproduce power device turn-off switching. It is also analyzed that due to the negligence of C_{ds}, it reduces the influence of the dynamic characteristic on the precision of the power device model to reproduce switching waveforms.

Future work

The realized work in the dissertation can be applied to better exploit WBG power semiconductor devices in order to integrate them in high frequency, high power density power converters. However,

there are still several aspects that are necessary to be continued in the future.

Regarding the presented characterization methods to measure power device static and dynamic characteristics, an automatic data acquiring system can be considered to be realized to rapidly obtain power device characteristics in the future work. The power device characterization time can thus be greatly reduced.

It is shown in the diode modeling that its impedance is very small when it is in conduction. Therefore, the characterization method sensibility can be further increased if measurement system setup impedance can be further decreased, which can be a research direction for the future work. It is shown in Chapter 4 that several approaches can help to further improve the proposed diode model, thus it is interesting to study how to systematically propose a preciser diode behavioral model by combining those approaches together.

It is shown in SiC JFET modeling that when power transistor is in linear region, its output capacitance values are boosted by the term $g \cdot R_{\mathrm{g}} \cdot C_{\mathrm{gd}}$. For the specific structure of the SiC JFET, C_{ds} capacitance value can be neglected in power device modeling. However, it is not validated in the dissertation that C_{ds} capacitance value can be correctly characterized when the power device is in linear region for the case of a SiC MOSFET. The presented characterization and modeling method in the dissertation can be applied on SiC MOSFET or GaN HEMT modeling in the future work.

When the above work is finished, automatic generation of power device models can be considered. The power device models can be based on the equivalent circuit with the same functions presented in the dissertation. Based on the characterization results, the parameters in these functions can be obtained directly by the fitting method. Therefore, power device models can be automatically generated after characterization results.

Once power device models are able to be obtained in such a way, they can be widely used in simulation software to research on switching losses, power device driver circuits, power converter topologies, power converter filters design, which is the objective of another dissertation started on September, 2013 on how to increase power density of power converters with GaN power transistors in the laboratory.

Publications

1. K. Li, A. Videt, and N. Idir, "Multiprobe Measurement Method for Voltage-Dependent Capacitances of Power Semiconductor Devices in High Voltage," *Power Electronics, IEEE Transactions on*, vol. 28, no. 11, pp. 5414–5422, 2013.

2. K. Li, A. Videt, and N. Idir, "GaN-HEMT Fast Switching Current Measurement Method Based on Current Surface Probe," in *Power Electronics and Applications (EPE), 2014 16th European Conference on*, Aug. 2014.

3. K. Li, A. Videt, and N. Idir, "SiC/GaN power semiconductor devices inter-electrode capacitances characterization based on multiple current probes," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, Sep. 2013.

4. K. Li, A. Videt, and N. Idir, "Caractérisation des capacité inter-électrodes d'un SiC-JFET "Normally-off" en régime désaturé," in *Symposium de Génie Electrique-SGE2014*, ENS Cachan, France, 2014.

5. K. Li, "Mesure des Capacités Inter-électrodes des Composants Semi-conducteurs de Puissance dans Différents Points de Fonctionnement par la Méthode Multipinces," in *JCGE2013*, Saint-Nazaire, 2013.

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