Thèse

Présentée à

L'Université de Lille 1 – Sciences et technologies
Institut d'Electronique, de Microélectronique et de Nanotechnologies, UMR 8520

Pour l'obtention du diplôme de doctorat
Discipline : Micro et nanotechnologies, acoustique et télécommunication

par

José MORON GUERRA

Design of Sub-THz heterodyne receivers in 65 nm CMOS process

Soutenance prévue pour le 9 juillet devant le jury composé de:

Nathalie **ROLLAND**	**Président**
Jean-François **LAMPIN**	**Directeur de Thèse**
François **DANNEVILLE**	**Co-directeur de Thèse**
Jean-Baptiste **BEGUERET**	**Rapporteur**
Jean-Louis **COUTAZ**	**Rapporteur**
Baudouin **MARTINEAU**	**Examinateur**
Patrick **MOUNAIX**	**Examinateur**
Alexandre **SILIGARIS**	**Encadrant industriel**

« Equipped with his five senses, man explores the universe around him and calls the adventure science»

Edwin Hubble

Remerciements

Ce travail a été réalisé au CEA-LETI de Grenoble au sein du laboratoire LAIR. Je tiens à remercier tout d'abord Alexandre Siligaris pour m'avoir encadré et accompagné tout le long cette thèse (surtout dans les moments difficiles). Son support a été primordial pour la réussite technique et personnelle de ce doctorat. Je tiens à remercier énormément Pierre Vincent pour m'avoir accueilli au sein du LAIR.

Je voudrais exprimer ma reconnaissance aux membres du laboratoire LAIR pour leurs amitiés et leur soutien. Je remercie Clément Jany (for the win), Gauthier Tant, Amine Didioui, Nelvynn, Robert Polster, Alexandre Giry, Vincent Puyal, José Luis González-Jiménez, Matthieu Verdy, Alin Ratiu, Benjamin Caillat, Alexandre Fonseca, Karl Marechal, Matthieu Dubois, Dominique Morche, Cédric Dehos, Patrick Villard, Emeric De Foucauld, Christopher Mounet et Jérôme Prouvée. Excusez-moi si j'oublie quelqu'un !

Je tiens à remercier aussi les amis du LETI : Micha, Jean-Fred, Florent, Aurélien, Guillaume, Momo, William, Karim et Armelle.

Je souhaite remercier mes directeurs de thèse Jean-François Lampin et François Danneville ainsi qu'au personnel de la centrale de caractérisation de l'IEMN, surtout à Sylvie Lepilliet. Je remercie aussi Marina Deng et Guillaume Ducournau.

J'adresse également mes remerciements à tous les membres de mon jury de thèse pour avoir accepté d'évaluer et juger mon travail. C'est un honneur.

Je tiens à remercier vivement tous mes amis, surtout à ceux qui ont subi la fin de ma rédaction de thèse : Farid (squat bureau), Olivier et Cassandre (squat rédaction), Alexandra et Alexandre Ferret. Un gros merci à Bruno, Rafael, Romina, Laura, Mauricio, Steve, Will, Yannick, Perle, Maxime, Jérôme et Elise pour leur soutien même à distance.

Finalmente un agradecimiento especial a toda mi familia y amigos en Perú. A mis padres por ser un ejemplo de vida y mis hermanos por ser geniales.

Contents

General introduction

In the recent years, the CMOS community reached a breaking point in the wireless communication paradigm: the development of fully CMOS based mmW systems was actually possible. Historically speaking, mmW systems were designed using advanced processes such as SiGe and III-V compounds, nowadays there are many functional CMOS based transceivers in the 60 GHz band; this demonstrates that CMOS technologies challenge their well-known frequency limits.

In the spirit of pushing even more the limitations of CMOS processes, this PhD thesis is one of the first efforts to explore design opportunities beyond CMOS cut-off frequencies (f_t/f_{max}) by developing heterodyne receivers at around 280 GHz. As a first step, the main application of such a component is to be used as a Sub-THz heterodyne image detector. This detection method can provide an alternative to the lately developed CMOS square law detector built with cold fet self-mixers; however, wireless communication applications is worth to be considered in a near future. The title of this work encourages the examination of the following research questions:

1. The frequency: Why is the THz band important? What are the applications of THz imaging?
2. The process: It is well know that CMOS transistors are outperformed by SiGe and III-V components nevertheless the low cost opportunity of having CMOS based high frequency systems is highly tempting. Broadly, why is CMOS technology so important for Sub-THz systems despite their frequency limitations?
3. The method: How is it possible to design a 280 GHz heterodyne receiver with a CMOS process whose f_{max} is around 200 GHz?

This work is divided into two main parts, each one being split into two chapters. The first part describes the context; the “frequency” and the “process” are presented and analyzed.

Chapter I provides a background of THz technology and techniques with a focus on THz imaging. It delivers a broad view of the THz detection by explaining the two detection methods: direct and heterodyne while presenting the state of the art of CMOS THz detectors.

Chapter II complements the first chapter; it provides enough information on CMOS process, focusing the attention of the high frequency behavior for such technology. Transistor modeling is discussed as well as passive components in the back end of line. There is a sub-

section dedicated to the development and evaluation of different parasitic extraction methods. Finally this chapter identifies the critical building blocks of a (at this point) “potential” sub-THz heterodyne receiver using CMOS.

The second part of this work addresses the development of the heterodyne receivers; this part is directly related to the “method” and it answers the following questions: how is it possible to design beyond CMOS cut-off frequencies?

Chapter III provides information about the local oscillator which is one of the most important and challenging building blocks in a heterodyne receiver. The basics and operating principles of classic oscillators are presented as well as the used architectures allowing signal generation beyond f_{max}. This chapter delivers also the state of the art of Sub-THz CMOS oscillators and finally the design, implementation and test of two sub-harmonic injection locked oscillators at 280 GHz is presented.

Chapter IV presents all the building blocks of the two developed heterodyne receivers excepted for the oscillators prior described: the operating principle of the resistive mixers is introduced as well as their design; the intermediate frequency amplifier design is presented as well. Moreover, the test results of both receivers are shown and their performances are compared with other silicon based heterodyne receivers from the state of the art. Finally, a set of THz images detected using one of the receivers is presented.

The final part of this thesis is dedicated to the general conclusion and perspectives; in this part all the technical and intellectual achievements will be highlighted and reviewed. Finally, a list of scientific publications is presented.

PART I: Context

Chapter I: The THz and Sub-THz bands

There is a growing interest of the mmW community on the THz band; there are two main reasons for this phenomenon: the first one is the numerous potential applications of THz radiation (T rays) and the second one is the late massive increment on cut-off frequencies of silicon technologies as well as their potentialities in the THz band. The first reason is discussed in this chapter whereas the second one is introduced and developed in depth in chapter II.

The purpose of this chapter is to give a general explanation and context about the THz and Sub-THz frequency bands. The first section of this chapter is a THz overview; it starts with a brief explanation of the THz (Sub-THz) band as well as the possible applications and opportunities around those frequencies; the THz gap between photonics and electronics is the main subject.

The second section of this chapter is about THz imaging which is one of the main applications of the THz gap. First a study of atmospheric absorption is presented giving the justification of the chosen frequency of operation of this work. Second a classification of the different types of THz imaging techniques is introduced providing to the readers a better understanding of where this work is placed in the whole universe of the THz imaging. For that, various types of THz imaging are described and the different detection methods are presented and developed with a consistent state of the art on CMOS and BiCMOS THz imagers. Thus, the chosen approach of this thesis is given: the development of heterodyne receivers (detectors) in CMOS for THz imaging applications.

I.1. The THz Gap

In the electromagnetic spectrum there is a band known as the THz Gap. This frequency band spans from 300 GHz (Sub millimeter wave threshold) to 10 THz (Infrared frontier) and it is the middle ground between electronics and photonics; the name THz Gap comes from the (historically) lack of suitable technology to “bridge the gap” between classic microwave electronics and optics [1], this is explained clearly in the electromagnetic spectrum presented in Figure I-1.

Historically, the THz Gap band could not be approached using classic photonic principles because of the larger wavelengths of the Terahertz radiation [2] (if compared with the ones from the infrared and visible bands). From a solid state electronics point of view this frequency band was also hard to reach due to the low cut-off frequencies of most processes.

However, this “gap” has been diminishing lately because of the optical advancements from the high frequency side, and microelectronics improvements in terms of high operating frequencies and design from the low frequency side [3]. In [4] the THz Gap is even divided into two different bands depending on the nearest frontier: from 100 GHz to 1 THz the band is called THz electronics because is closer to the microwave edge and from 300 GHz to 10 THz the band is named THz photonics since is nearer to the infrared upper limit, both bands overlap from 300 GHz to 1 THz. In this work, the main focus is on the techniques used to reach the lower side of the THz photonics frequency band using a standard CMOS process.

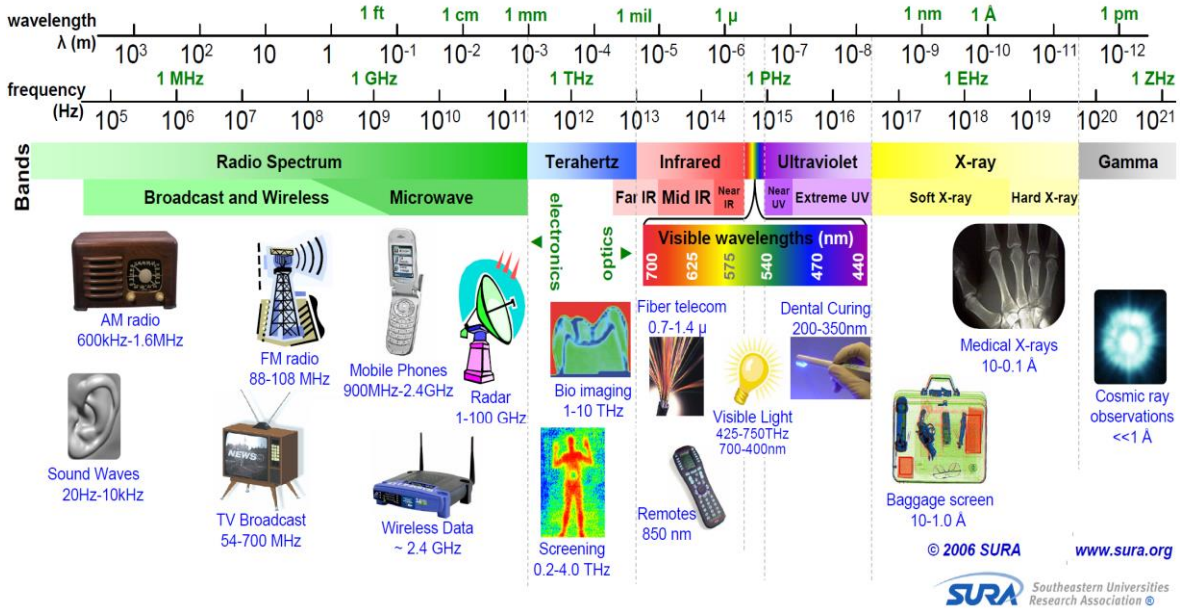


Figure I - 1 : Electromagnetic spectrum proposed by the Southeastern Universities Research Association.

In the following sub-section, the properties of T rays are presented in order to introduce the potential applications and opportunities of this frequency band.

I.1.1. Applications and opportunities

Condensed matter can be grouped in three different categories (based on optical properties at THz frequencies): water, metal and dielectric [3].

Polar molecules like water are very absorptive in the THz region. Since metals present high electrical conductivity, this type of material is very reflective at THz frequencies. Dielectrics such as paper, plastic or ceramic are usually more transparent for T rays [3].

From the paragraph below, these properties present mostly advantages for one of the most important applications of this band which is the THz imaging. Since T rays penetrate through

dielectrics (clothes, paper, cardboard, plastic, ceramic and many more[1]) the applications in the safety and security areas are obvious. For instance THz imaging can detect concealed objects such as guns and blades inside packages, clothes or mattresses, which enable its use in airports and postal/custom offices. The fact that dielectrics are transparent for T rays also allows the use of THz imaging in the area of quality control.

Since the Terahertz radiation has low energy photons (4,1 meV for 1 THz), this kind of imaging cause no potentially harmful photo ionization in biological tissues enabling its use for non-invasive sampling [5], biomedical imaging or environmental studies like the one performed by [6] which allowed to see the moisture content and structure of different leaves thanks to a THz image. In Figure I-2, the leaves THz image from [6] and a concealed knife into a mattress from [1].

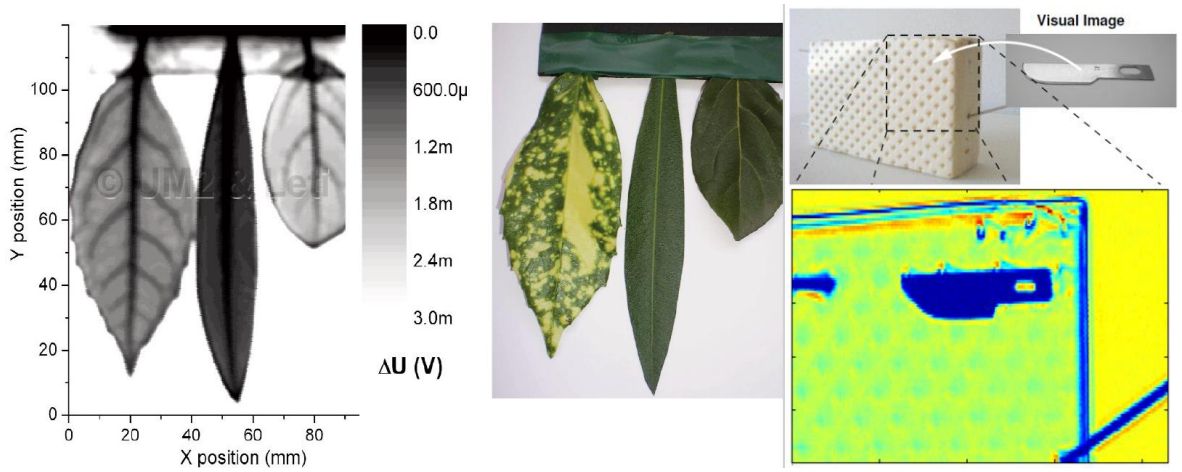


Figure I - 2 : THz images of (a) moisture and structure of leaves from [6] and (b) concealed knife in mattress from [1].

Even if the main application of this work is the THz imaging, the THz Gap presents many other opportunities, especially in space exploration and astronomy. Results from NASA projects (COBE and DIRBE) as well as examination of the spectral energy distributions point to the fact that around half of the total luminosity and 98% of the photons emitted since the Big Bang descend into the far infrared spectrum [5]. This makes THz detectors authentic probes into the early universe [5]. Also another major application in astronomy is the planetary and small body observations [5].

However, historically, THz radiation was generated with femto-second lasers pulses and one of the first applications was spectroscopy for scientific purposes [1]. In any case, the development of silicon based THz circuits can enable the use of the THz technology for mass consumer applications such as high speed communication and short/long range radar.

In Figure I-3, the electromagnetic spectrum of the total atmospheric absorption of water/vapor and oxygen is presented. Since the challenge of this work is to reach the THz gap from the solid state electronics side, the frequency operation of the circuits developed here is around 300 GHz. Based on Figure I-3, there is a valley of absorption between the 180 GHz and 310 GHz peaks. In order to be as near as possible to the THz gap band, the chosen operation frequency is between 250 GHz and 290 GHz.

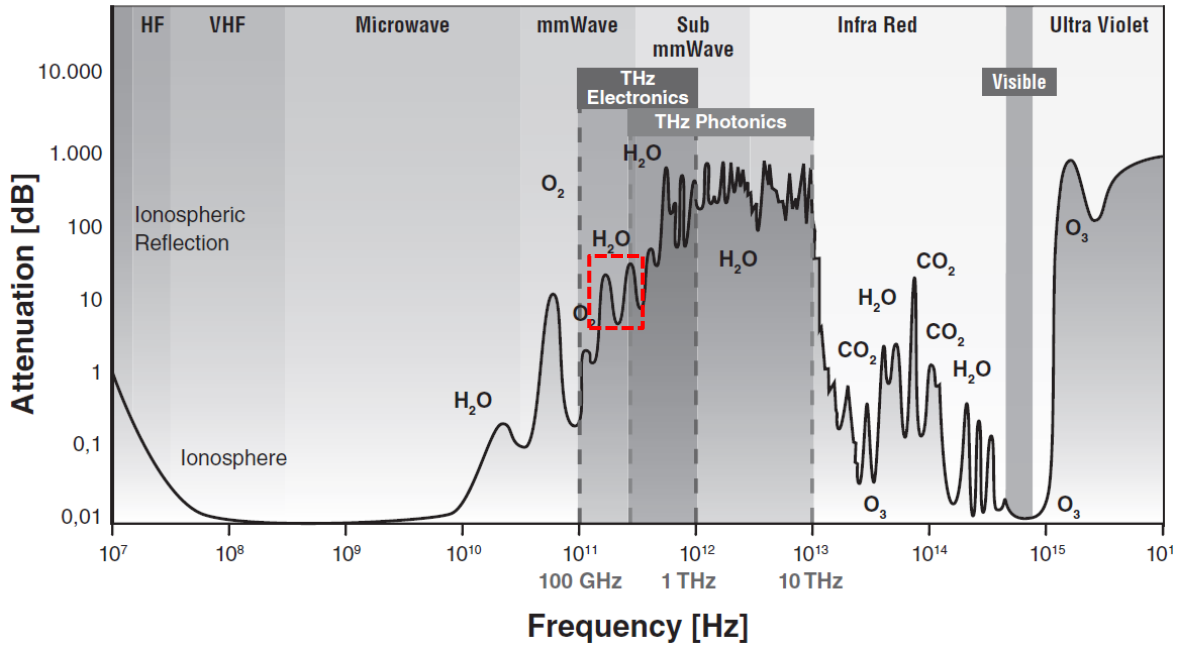


Figure I - 3 : Atmospheric attenuation spectrum from [4]. The valley which represents the operating frequencies of this work is highlighted.

Since the aimed application for the circuits is (at first) THz imaging, the following section of this chapter is entirely dedicated to this subject.

I.2. THz Imaging

X rays are ionizing radiations and can cause harm to the living tissues. Also some tissues are imperceptibles to X rays, for that kind of material or when high contrast is needed magnetic resonance imaging is the best choice; however this technique is limited in terms of spatial resolution. T rays with their particular optical properties and low energy photons (potentially harmless to living tissues) offer countless opportunities in terms of imaging [7] and has become a very researched field nowadays.

There are many ways of classifying the different types of THz imaging. The following paragraphs summarize this field and place this work in the broad THz research topic.

Figure I-4 presents a schematic that classifies THz imagers. There are two main categories: Pulsed broadband THz imaging and continuous wave (CW) THz imaging. Inside the category of CW there are two main sub-categories: Passive imaging (radiometry) and active imaging. A silicon based state of the art is presented in the following pages about active continuous wave THz imaging, since this work is placed into this sub-category, specifically using the heterodyne detection method. Both of the detection methods are presented in detail in I.2.1.

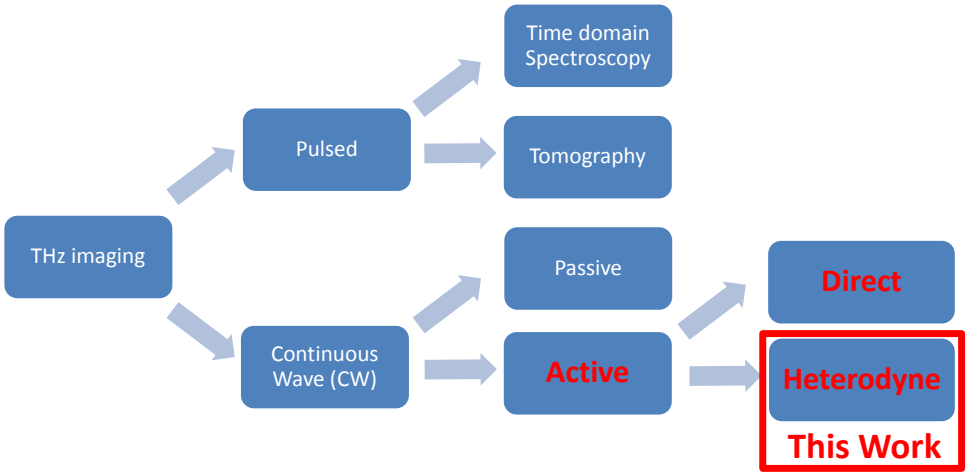


Figure I - 4 : Classification of THz imaging. In red the subjects close to this work are highlighted.

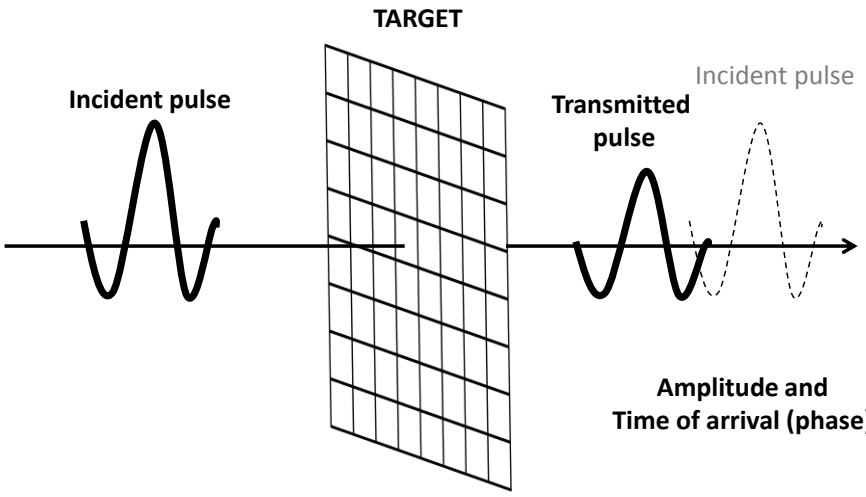


Figure I - 5 : Standard operating principle set up for THz time domain spectroscopy [3].

In the field of the THz imaging with broadband pulses, the most popular technique is the THz time domain spectroscopy: In this method, a laser pulse is sent to the target and then analyzed, the difference in amplitude and phase (arrival time) allows the reconstruction of an image from a focal plane raster scanner [3], THz pulses are usually generated using femto

second lasers and photoconductive antennas. In Figure I-5, the standard THz time domain spectroscopy operating principle set up is presented.

Another sector that uses THz pulses is the T ray tomography which is used generally for 3D reconstruction; this technique can refer to the reflection tomography, computed tomography or diffraction tomography. In the case of reflection tomography, a pulse is sent into multilayer structure and then the reflected pulse is treated using a time of flight analysis in order to map out the internal layers of the structure. Computed tomography is a technique mostly used for X ray imaging and can be as well used with T rays, this technique consists in taking a series of shadowgraphs around the axis of rotation of an object, this contains enough information to generate cross-sectional image using specific algorithms [3].

Continuous wave (CW) THz imaging can be easily divided in two simple categories: Active CW THz imaging and passive CW THz imaging. Pulsed THz imaging operates always with a source (laser generated pulse), CW THz imaging, on the other hand, can operate with or without a source. This aspect defines the difference between active and passive CW imaging.

The operation principle of THz radiometry (Passive CW THz imaging) is the detection of the background temperature of the imaged object (thermal radiation). By measuring this radiation it is possible to detect small temperature differences, passive THz imagers need highly sensitive detectors [3] which in terms of complexity compensates all the advantages of the absence of THz source [1]. This type of imaging can be used for outdoor detection because of its large detection range (from few meters to several kilometers)[1], this long distance is the reason why most of passive imagers operate between 50 and 110 GHz in order to avoid atmospheric absorption [1] (Figure I-3). The main problems with THz radiometry are the lack of phase information and the long acquisition time. Figure I-6 presents the standard schematic of a passive imager detector from [3].

Low noise amplifiers are used to raise the signal above the noise floor of the detector; these LNA's are usually designed using III-V processes such as GaAs and InP. Passive imaging detectors need more sensitivity if compared with active detectors; this sometimes enables the need of cryogenic cooling in order to increase the sensitivity. The pre-amplification performed by the LNA's reduces the needed sensitivity avoiding the necessity of cryogenic cooling. The detectors are commonly bolometers or Schottky diodes [1] [3]. The sensitivity of passive imagers is defined by the noise-equivalent temperature difference (NETD). In 2010, [8] presented the first silicon based passive mmW radiometer.

Active CW detectors need a source to illuminate the scene and they have a small acquisition time if compared with passive detectors. Also active imaging can potentially obtain phase information enhancing the detection capabilities. Table I-1 sums up the main differences between active and passive THz imaging.

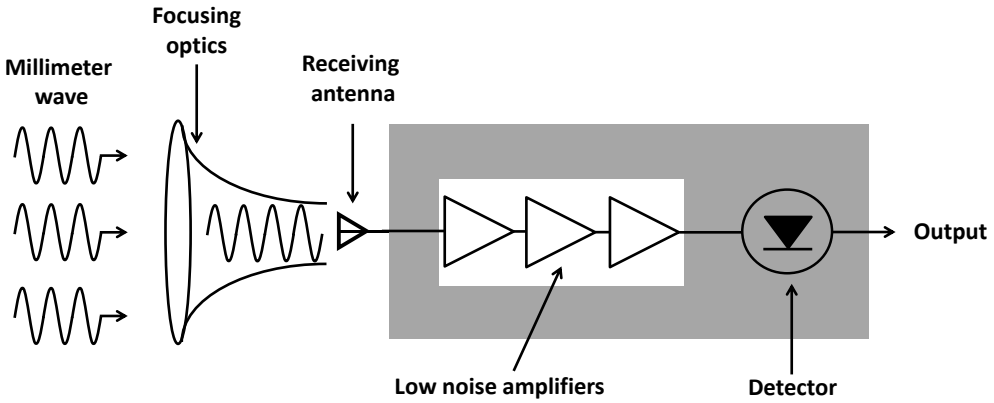


Figure I - 6 : Standard schematic of a passive THz imager from [3].

	Active Imaging CW	Passive Imaging
Detector sensitivity	Low	High
Sensitivity to environment	Relatively low	High
Detection range	Limited by source-object distance	Relatively long
Image interpretation	Difficult due to coherent artifacts	Easy
Covert operation	No	Yes
Safety concern	Unknown	No
Acquisition time	Short	Long

Table I - 1 : Active versus Passive THz Imaging [3].

I.2.1. Active continuous wave detection methods

Since the main goal of this work is to develop a heterodyne THz detector, the active detection methods are the main focus of this sub-section; the sources will not be treated even if the source power has a major impact on the detector sensitivity. The sensitivity definition of active detectors depends on the type of detection.

There are two detection methods for active imaging. Direct or non-coherent detection and the heterodyne detection, the main difference being the fact that the direct detection only identifies the amplitude of the THz signal whereas the heterodyne detection can also give information on the phase.

Up until 2008, most of THz detectors were discrete bulky components. Also in terms of THz imaging, most imagers used raster scanning 1 pixel at the time, nowadays CMOS

technologies can easily allow the development of focal plane arrays which can dramatically decrease the image acquisition time [9]. In this sub-section, both types of detection are presented with their respective CMOS/BiCMOS state of the art.

I.2.1.1. Direct

The sensitivity of the direct detection is defined by the Noise-equivalent power (NEP) and the integration bandwidth. The NEP is defined as the input power at which the signal to noise ratio (SNR0) is unity in a 1 Hz bandwidth at the output [10]. Direct detectors are mostly based on the physical principle of power/energy absorption such as calorimeters or bolometers, nevertheless detectors based on opto-acoustic principles such as Golay cells or square law detectors are included as direct detectors as well [9].

In 2008, the first CMOS 600 GHz Focal Plane Array (FPA) was presented in [9]. The presented detector was based on the square law detection principle of MOSFET, however field effect transistors (usually III-V compounds) have been used as square law detectors for lower microwave frequencies for many years before [2].

A square law CMOS detector is based on the self-mixing principle of a resistive mixer: since the cut-off frequencies are defined only for a specific drain to source voltage and a resistive mixer has no V_{ds}, the definition of cut-off frequency does not apply for a cold-FET circuit. In Figure I-7 the operation principle of a CMOS passive mixer operating in self-mixing mode is presented. This mode is obtained when the THz signal is applied to the LO and RF port simultaneously using a coupling capacitor. The result is a dc signal that is the square product of the power of the original THz signal.

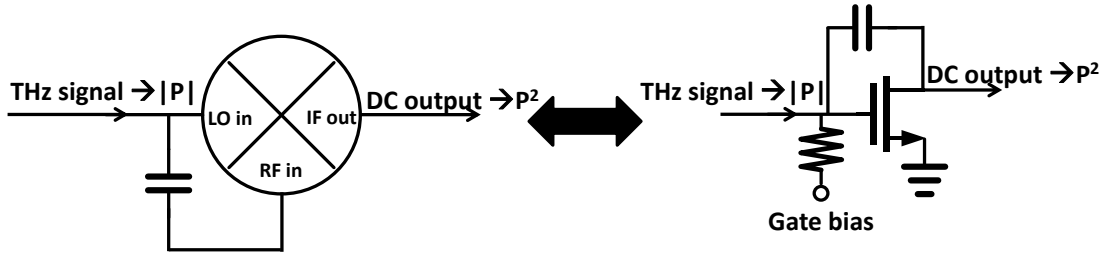


Figure I - 7 : Operation principle of the cold field effect transistor as a square law detector.

Since the first CMOS FPA, many CMOS THz direct imagers have appeared including the first 1K pixel THz video camera presented in [11] and in [12], this device can achieve 500 frames per second and is based on the same detection principle. In appendix 1.1, the expression of the Noise equivalent power for CMOS square law direct detectors is presented based on the analysis performed in [2].

Square law detectors based on the self-mixing principle of cold CMOS transistors are not the only way to design direct THz detectors on CMOS, in [13] Schottky barrier diodes were implemented in a standard 130 nm CMOS process achieving better performance in terms of NEP. Also, [14] presented a time encoded regenerative receiver as a detector for THz imaging: the operating principle is very different if compared with the previous ones however only the amplitude is detected, so I classified this detector into the direct category even if the system presents gain and it is active.

Direct detection is probably the most affordable way to implement real time THz detection for all the applications mentioned before; focal plane arrays have been implemented in CMOS many times since 2009, however because of the fact these detectors cannot acquire the phase information of the THz signal, heterodyne detection can still be an asset to the whole CMOS THz imaging industry. In table I-2, the direct detection CMOS imagers are compared in terms of process, array size, frequency, responsivity, NEP and frame rate. At the bottom of the table some industrial THz detectors from Virginia Diodes are presented for comparison purposes.

Process	Detection type	year	Array size	Frequency THz	Max responsivity KV/W	Min NEP pW/(Hz)$^{1/2}$	Frame rate	Extra optics	Reference
250 nm CMOS	Square law	2008	3x5	0.6	50	400	Image	No	[9]
250 nm CMOS	Square law	2009	3x5	0.65	80	300	Image	No	[2]
65 nm CMOS SOI	Square law	2010	3x5	0.65	1.1	50	Image	No	[15]
65 nm CMOS	Square law	2011	3x5	0.6 to 1	0.8	66	Image	Si Lens	[16]
130 nm CMOS	Square law	2011	3x4	0.3 to 1	1.8	-	Image	No	[6]
65 nm CMOS	Time encode regenerative Rx	2011	1x1	0.183	-	0.00151 (from KTB)	Image	No	[14]
65 nm CMOS	Square law	2012	32 x 32	0.79 to 0.96	56.6	470	25	Si lens	[11]
130 nm CMOS	Schottky barrier diode	2013	4x4	0.28	5.1	32	Image	No	[13]
Model: WR1.5ZBD	Zero bias Schottky diode			0.5 to 0.75	0.75	5.1			[17]
Model: WR1.9ZBD	Zero bias Schottky			0.4 to 0.6	1	4.1			[17]

Table I - 2 : CMOS based direct receivers for THz imaging.

I.2.1.2. Heterodyne

The heterodyne detection is entirely based on the same operating principle than heterodyne receivers: a high frequency RF signal (THz in this case) is down-converted using a mixer and a

Local Oscillator (LO). The mixer behaves as an analog multiplier and generates two signals as a result of the multiplication of the RF and LO signals (RF±LO). The main disadvantage of this detection is the need of a local oscillator, however the fact that heterodyne receivers can detect phase information open the gates for new opportunities in the THz world. Also heterodyne receivers are more sensitive than the direct receivers in terms of amplitude detection.

In [1], a system study of the sensitivities of each type of detector was performed. The link in terms of sensitivity between the direct and heterodyne detection is the signal to noise ratio (SNR0) of the image. This study states that in the interest of obtaining an image with 20 dB SNR0 the needed NEP of direct detectors is 20 pw/(Hz)$^{1/2}$ which is hard to achieve according to Table I-2. On the other hand, heterodyne detection requires a receiver of 90 dB NF in order to achieve the same 20 dB SNR0 image. In telecommunication a 90 dB NF receiver is far beyond acceptable; however a receiver like this can significantly increase the quality of a THz image. The SNR0 in practical terms of imaging is related to the contrast: the better SNR0 the best the contrast is. This study is presented in Figure I-8.

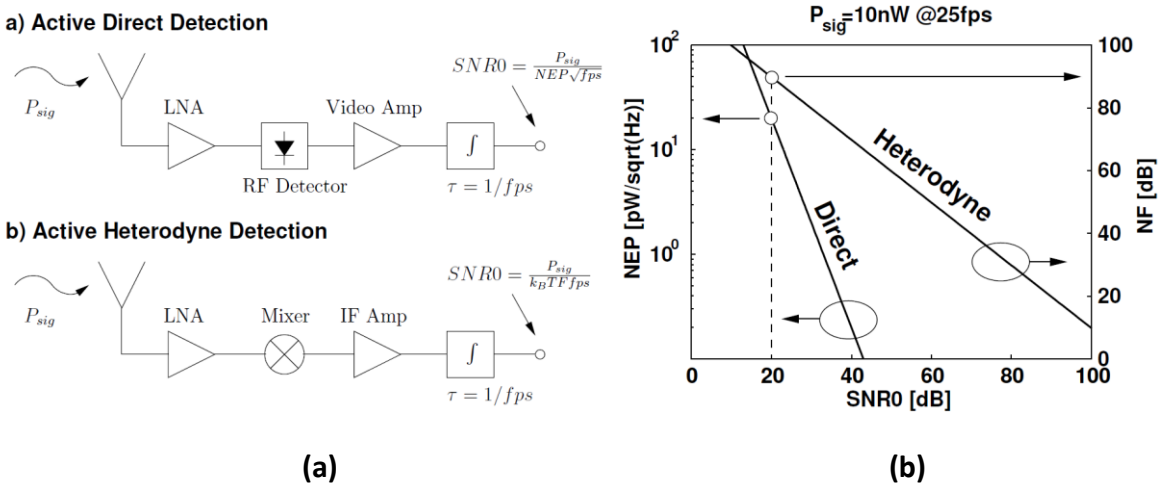


Figure I - 8 : (a) Active direct and heterodyne detection architectures with signal to noise ratio expression for both methods. (b) NEP, NF & SNR0 comparison [1].

The advantage of heterodyne detection over direct detection has also been presented in [18]. In this paper, the direct square law detectors are used as standard passive mixers. The differences of the respective images are presented in Figure I-9. It can be observed that the heterodyne detection can detect weaker signals allowing the identification of elements imperceptibles for direct detection. Both of these studies justify the choice of the heterodyne detection as the core of this work. For differentiation purposes, Table I-3 presents the “equivalent” NF of direct detectors (including two from VDI) based on the SNR0 analysis developed in [1].

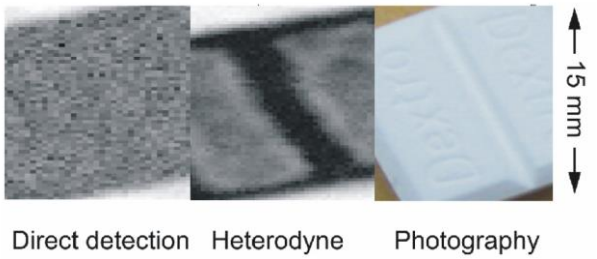


Figure I - 9 : Image difference between the direct and heterodyne detection. The photography is also presented [18] .

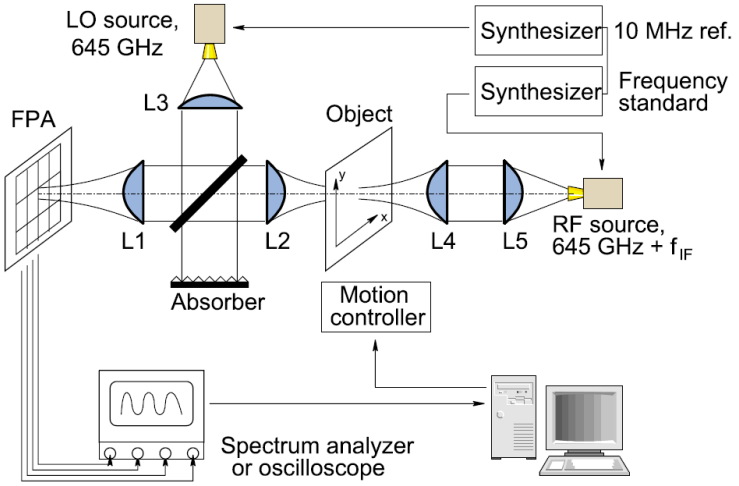


Figure I - 10 : Experimental test setup for THz heterodyne imaging with LO and RF signals radiated [19] [20] .

Detector - Reference	Type	Frequency THz	Min NEP pW/(Hz)$^{1/2}$	NF equivalent
VDI WR1 5ZBD [17]	Schottky	0.5 to 0.75	5.1	83 dB
VDI WR1 9ZBD [17]	Schottky	0.4 to 0.6	4.1	80 dB
Ojefors_2010 [15]	Self-mixing CMOS SOI	0.65	50	95 dB
Zhang_2013 [13]	Schottky CMOS	0.28	32	92 dB

Table I - 3 : CMOS based direct receivers for THz imaging

Broadly, if a Sub-THz heterodyne detector achieves a NF of at least 50 dB, the SNR0 of the image can be increased by 40 dB according to Figure I-8 and the NF values from Table I-3. This and the results from Figure I-9 show the advantage of the heterodyne method over the direct method in terms of amplitude detection.

The first heterodyne receiver in CMOS was developed in 2009 [18] [19] [20] for 650 GHz detection, in this receiver, the local oscillator signal was illuminated (as well as the RF signal)

over the focal plane array using a particular experimental setup presented in Figure I-10. This receiver presents a NF of 70 dB, an IF bandwidth of 100 KHz to 10 MHz and a conversion gain of 10 dB (not taking into account the antenna losses).

In 2010 [21] presented a 0.13 µm SiGe (f_t/f_{max} =240/330 GHz) heterodyne receiver for 650 GHz detection. In this component the high frequency local oscillator signal (162 GHz) was generated using an external synthesizer and multiplier. This external LO signal is then amplified, adapted and recombined with the radiated RF signal into a folded dipole integrated antenna. The recombined signal is then driven to an active sub-harmonic mixer. This heterodyne receiver presents a NF of 43 dB and a conversion gain of -14 dB for 433 mW DC power consumption.

A similar architecture was presented in [22] in 2011 where the oscillator multiplier chain was integrated this time and the overall system was designed to operate at 820 GHz. The process was a 0.25 µm SiGe (f_t/f_{max} =280/435 GHz); in terms of performance the receiver presents a NF of 47 dB and a -22 dB conversion gain for a 1.2 W DC power consumption (2x2 receiver array).

Up until now most of the silicon based heterodyne receivers were developed having THz imaging as a target application, however, there are also CMOS/BiCMOS heterodyne receivers for data communications and/or radar applications. This is the case of a SiGe component presented in [23] in 2011 which is the very first THz silicon based fully integrated transceiver. It presents a NF of 35 dB and a conversion gain of -7 dB for 364 mW DC power (entire transceiver) and operates a 380 GHz. Also the first CMOS THz transceiver was presented in 2012 in [24].

Many more silicon based heterodyne receivers will be presented as well in chapter IV where they will be compared with receivers developed in this work.

I.3. Conclusion

One of the main goals of this chapter is to provide a general overview of the THz gap: in the first section this frequency band was presented as well as the applications and opportunities such as THz imaging and astronomy.

In the second section the subject of the THz imaging was developed: first a classification of this entire field was made in order to help the reader to place this work inside this broad research topic. Second, a CMOS/BiCMOS state of the art was presented for the continuous wave active THz imaging: both detection methods were presented and the choice of the heterodyne detection was justified.

I.4. References

[1] U. R. Pfeiffer and E. Ojefors, "Terahertz imaging with CMOS/BiCMOS process technologies," in *ESSCIRC, 2010 Proceedings of the* , 2010, pp. 52–60.

[2] E. Ojefors, U. R. Pfeiffer, A. Lisauskas, H. G. Roskos, E. Öjefors, and S. Member, "A 0.65 THz Focal-Plane Array in a Quarter-Micron CMOS Process Technology," *Solid-State Circuits, IEEE J.*, vol. 44, no. 7, pp. 1968–1976, 2009.

[3] Y.-S. Lee, *Principles of Terahertz Science and Technology*. Springer , 2008.

[4] U. R. Pfeiffer, E. Öjefors, A. Lisauskas, H. G. Roskos, and E. Ojefors, "Opportunities for silicon at mmWave and Terahertz frequencies," in *Bipolar/BiCMOS Circuits and Technology Meeting, 2008. BCTM 2008. IEEE* , 2008, pp. 149–156.

[5] P. H. Siegel, "Terahertz technology," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.

[6] F. Schuster, H. Videlier, A. Dupret, D. Coquillat, M. Sakowicz, J.-P. Rostaing, W. Knap, M. Tchagaspanian, and B. Giffard, "A broadband THz imager in a low-cost CMOS technology," in *2011 IEEE International Solid-State Circuits Conference*, 2011, no. 11, pp. 42–43.

[7] J.-L. Coutaz, R. Boquet, N. Breuil, L. Chusseau, P. Crozat, J. Demaison, L. Duvillaret, G. Gallot, F. Garet, J.-F. Lampin, D. Lippens, J. Mangeney, P. Mounaix, G. Mouret, and J.-F. Roux, *Optoélectronique Térahertz*. Les Ulis, 2008.

[8] J. W. May and G. M. Rebeiz, "Design and Characterization of W-Band SiGe RFICs for Passive Millimeter-Wave Imaging," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1420–1430, May 2010.

[9] U. R. Pfeiffer and E. Ojefors, "A 600-GHz CMOS focal-plane array for terahertz imaging applications," in *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European* , 2008, pp. 110–113.

[10] A. M. Cowley and H. O. Sorensen, "Quantitative Comparison of Solid-State Microwave Detectors," *IEEE Trans. Microw. Theory Tech.*, vol. 14, no. 12, pp. 588–602, Dec. 1966.

[11] H. Sherry, J. Grzyb, Y. Zhao, R. Al Hadi, A. Cathelin, A. Kaiser, U. Pfeiffer, and T. I. Applications, "A 1kpixel CMOS camera chip for 25fps real-time terahertz imaging applications," in *2012 IEEE International Solid-State Circuits Conference*, 2012, no. March 2011, pp. 252–254.

[12] R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Forster, H. M. Keller, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "A 1 k-Pixel Video Camera for 0.7–1.1 Terahertz Imaging Applications in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2999–3012, Dec. 2012.

[13] Y. Zhang, R. Han, Y. Kim, D. Y. Kim, H. Shichijo, S. Sankaran, C. Mao, E. Seok, D. Shim, and K. O. Kenneth, "Schottky diodes in CMOS for terahertz circuits and systems," in *2013 IEEE Radio and Wireless Symposium*, 2013, pp. 43–45.

[14] A. Tang and M.-C. F. M. F. Chang, "183GHz 13.5mW/pixel CMOS regenerative receiver for mm-wave imaging applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International* , 2011, no. May 2010, pp. 296–298.

[15] E. Ojefors, N. Baktash, Y. Zhao, R. A. Hadi, H. Sherry, and U. R. Pfeiffer, "Terahertz imaging detectors in a 65-nm CMOS SOI technology," in *ESSCIRC, 2010 Proceedings of the* , 2010, pp. 486–489.

[16] R. Al Hadi, H. Sherry, J. Grzyb, N. Baktash, Y. Zhao, E. Ojefors, A. Kaiser, A. Cathelin, and U. Pfeiffer, "A broadband 0.6 to 1 THz CMOS imaging detector with an integrated lens," in *2011 IEEE MTT-S International Microwave Symposium*, 2011, pp. 1–4.

[17] "Virginia Diodes, Inc - Detectors." [Online]. Available: http://vadiodes.com/index.php/en/products/detectors.

[18] D. Glaab, A. Lisauskas, S. Boppel, U. Pfeiffer, E. Ojefors, and H. G. Roskos, "Terahertz heterodyne detection with silicon CMOS transistors," in *Infrared, Millimeter, and Terahertz Waves, 2009. IRMMW-THz 2009. 34th International Conference on* , 2009, pp. 1–2.

[19] U. R. Pfeiffer, E. Ojefors, A. Lisaukas, D. Glaab, and H. G. Roskos, "A CMOS focal-plane array for heterodyne terahertz imaging," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, 2009, pp. 433–436.

[20] D. Glaab, S. Boppel, A. Lisauskas, U. Pfeiffer, E. O uml jefors, and H. G. Roskos, "Terahertz heterodyne detection with silicon field-effect transistors," *Appl. Phys. Lett.*, vol. 96, no. 4, p. 042106 (3 pp.), 2010.

[21] E. Ojefors, U. R. Pfeiffer, and E. Öjefors, "A 650GHz SiGe receiver front-end for terahertz imaging arrays," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* , 2010, vol. 43, no. 5, pp. 430–431.

[22] E. Ojefors, J. Grzyb, Y. Zhao, B. Heinemann, B. Tillack, and U. R. Pfeiffer, "A 820GHz SiGe chipset for terahertz active imaging applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International* , 2011, pp. 224–226.

[23] J.-D. Park, S. Kang, Niknejad, .M., E. Engineering, and C. Sciences, "A 0.38THz fully integrated transceiver utilizing quadrature push-push circuitry," in *2011 Symposium on VLSI Circuits (VLSIC)*, 2011, pp. 44–45.

[24] J.-D. Park, S. Kang, S. V Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *2012 Symposium on VLSI Circuits (VLSIC)*, 2012, pp. 48–49.

Chapter II: CMOS at mmW and Sub-THz frequencies

The possibilities and opportunities of CMOS technologies around the THz gap are discussed in this chapter. First the context is presented; the evolution of CMOS cut-off frequencies and a comparison between CMOS, SiGe and III-V compounds is made.

The second section treats about the electrical behavior of the used CMOS process (65 nm from ST Microelectronics). The active components (transistors) are presented as well as the implications of using them beyond cut-off frequencies. The second sub-section introduces the passive components of the 65 nm CMOS process. The back end of line is presented as well as the capacitors, resistors and thin film micro strip lines behaving as inductances. Finally the developed techniques for parasitic extraction using EM simulations are discussed.

The next section presents the core of this PhD thesis: the CMOS THz heterodyne pixel. The architectures choices are justified according to the context and the critical building blocks are identified.

II.1. Context

Sub-micron technologies have evolved enough in terms of cut-off frequencies that the design of purely based CMOS Sub-THz/THz is actually possible. In comparison of classic high frequency processes like III-V compounds and SiGe, CMOS transistors present lower cut-off frequencies and breakdown voltages [1], nevertheless CMOS processes offer the advantage of high level of integration, maturity and specially mass production low cost.

With the arrival of the industrial-scientific-medical (ISM) band at 245 GHz in Europe [2], there will be a high demand of Sub-THz chip-sets to address the various applications in this frequency band.

The context is divided in two sub-sections: In the first one, the CMOS transistors cut-off frequencies evolution is presented and in the second one, a comparison between III-V, SiGe and CMOS processes is made.

II.1.1. ft/fmax evolution

Both f_t and f_{max} are parameters used to characterize the high frequency performance of a transistor [3]. f_t is called “Transition frequency” and it corresponds to the intrinsic performance of a transistor. It can be obtained from the forward current gain h_{21}; f_t is the

frequency for which $|h_{21}|$=1. The expression of $|h_{21}|$ as a function of the S parameters is presented in [4]:

$$|h_{21}|^2 = \left|\frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}\right|^2 \quad (1)$$

The transition frequency value depends on the length and current density of the transistor, for the 65 nm CMOS process this value is 150 GHz for a current density of 0.35 mA/µm and a gate length of 60 nm [3].

The second cut-off frequency (f_{max}) is the maximum oscillation frequency of a transistor. This represents the frequency where Mason Gain (U) becomes unity. The expression of this gain as a function of the S parameters is presented in [5].

$$\mathrm{U} = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left(k\left|\frac{S_{21}}{S_{12}}\right| - real\left(\frac{S_{21}}{S_{12}}\right)\right)} \quad (2)$$

Where k is the stability factor given by:

$$\mathrm{k} = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{21}S_{12}|^2}{2|S_{21}||S_{12}|} \quad (3)$$

For the 65 nm ST Microelectronics process this value is around 200 GHz for a current density of 0.35 mA/µm and a gate length of 60 nm [3]. The evolution of f_t and f_{max} of different CMOS processes is presented in Figure II-1 and compared with the 2005 ITRS roadmap, the 2011 HP[1] ITRS roadmap and the 2011 LSTP[2] ITRS roadmap.

The evolution of both cut-off frequencies is remarkable. It can be observed that the trend of both parameters to approach Sub-THz frequencies allows the potential use of CMOS processes in this frequency band.

II.1.2. CMOS, SiGe and III-V technologies

High frequency systems are historically related to the advanced integrated processes such as SiGe or III-V compounds. This last one is nowadays widely used for high frequency communications, defense and spatial applications; it is well known that III-V compounds components outperform CMOS and SiGe circuits in systems where high reliability is essential

[1] High performance logic transistor for mmW applications.
[2] Low standby power logic transistor for microwave and mobile applications.

[6]. However the interest of the semiconductor community currently focuses on the use of SiGe and CMOS for high frequencies because lately they have become viable options to replace the expensive GaAS (III-V) [7].

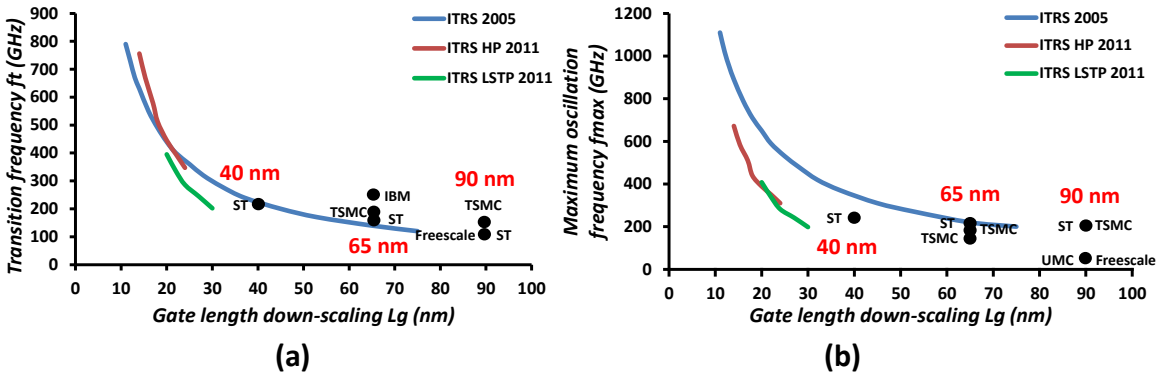


Figure II - 1 : (a) f_t and (b) f_{max} evolution of different CMOS processes compared with the 2005 and 2011 HP/LSTP ITRS roadmaps [3].

It is common knowledge that III-V compounds processes offer the highest cut-off frequencies, nevertheless these technologies suffer from expensive processes that prohibit mass production. The arrival of the ISM band in Europe [2] and the current interest for THz/Sub-THz applications, the potential mass consumer chipsets demand on this frequency band is imminent and that last fact clearly gives the advantage for the long term development to the silicon based technologies.

In 2009, authors stated in [7] that SiGe has two technology generations advantage over CMOS, which leads to a higher f_t and f_{max}. In terms of noise the CMOS transistors are more sensitive to the flicker noise (1/f) because of the Si/SiO_2 interface; however the 1/f noise on SiGe increases with scaling [8]. CMOS processes are extremely sensitive to the low noise amplifier (LNA) layout design; there are a lot of LNAs designed using the same CMOS process and featuring different noise performances. In the case of SiGe technology, the NF performance depends on the emitter length but most of the time the noise figure of a LNA on a known process can be predictable [7].

There are many comparable parameters in play for a proper comparison of RF SiGe Bipolar and MOS transistors, but in summary it can be stated that even if nowadays RF SiGe transistors are superior in terms of high frequency of operation, for the long-term, RF MOS transistors have the potential to become extremely competitive. Finally, standard CMOS processes are still cheaper for high massive production.

II.2. Sub-THz electrical behavior of 65nm CMOS technology

In this section the electrical behavior of the components of the 65 nm CMOS process is presented. This section is divided in three parts; the first one is dedicated to the active components (transistors) and their behavior at Sub-THz frequencies. The passive components are presented in the second part: the ones developed for this project and the ones provided by the ST Microelectronics design kit. The developed parasitic extraction techniques based on electromagnetic simulations are presented in the third sub-section.

II.2.1. Transistors

The ST Microelectronics 65 nm design kit provides a BSIM3 model for the transistors. Despite the fact that this model is very complex and accurate (especially for large signal simulations), modeling the active components using a small signal equivalent circuit (SSEC) allows a better understanding of the physics behind a RF MOS transistor. The equivalent model is presented in Figure II-2 and represents the high frequency electrical behavior of the transistor as accurately as the BSIM3 model. This equivalent circuit was proposed by [9].

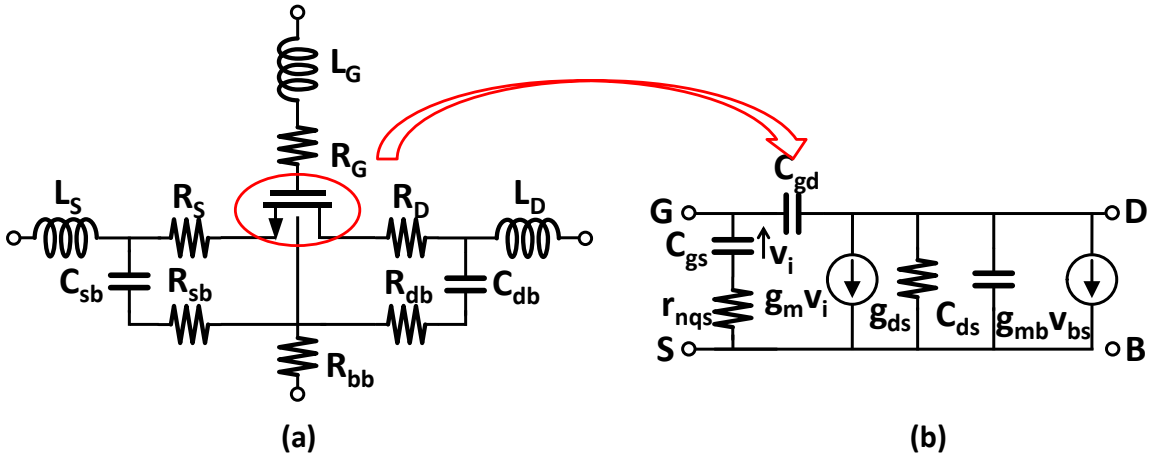


Figure II - 2 : (a) small signal transistor model including accesses and (b) intrinsic lumped model of the RFCMOS [9].

In Figure II-2 (a), the resistors R_S, R_G and R_D represent the access resistances; the other resistors (R_{bb}, R_{sb} and R_{db}) are related to the resistive substrate network. The inductors L_S,L_G and L_D represent the delay effects associated with interconnections [9]. Figure II-2 represents the behavior of the entire implementation of the transistor. And Figure II-2 (b) shows the intrinsic lumped elements of the transistor.

In order to considerably reduce the access resistances and particularly the gate resistance R_g, a multi-finger structure is commonly used on RF MOS transistors; this also allows the increase of the maximum oscillation frequency (f_{max}) because of its dependency on parasitic

extrinsic elements [9], especially R_g. The equivalent small signal model of one finger is presented in Figure II-3.

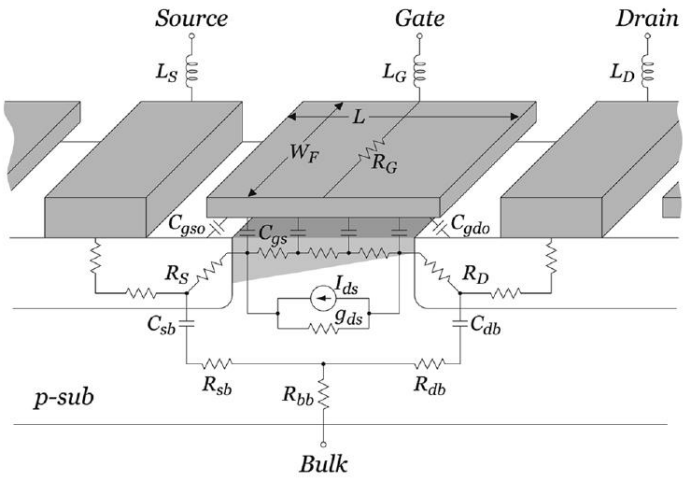
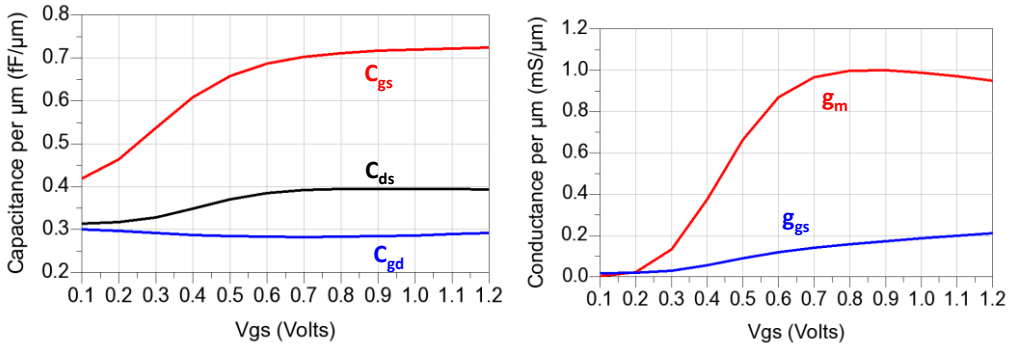


Figure II - 3 : Small signal equivalent model of one finger of a RFCMOS [9].



(a) **(b)**

Figure II - 4 : Simulated intrinsic capacitances (a) and conductances (b) per µm for different V_{gs} bias voltage.

Most of the previously represented lumped elements of a RF MOS transistor are very important for accurate electric simulations at Sub-THz frequencies. However, the elements that have the bigger impact at high frequency design (especially oscillators) are the intrinsic ones (C_{ds}, C_{gs}, C_{gd}, g_{ds} and g_m). Figure II-4 shows a simulated extraction of the intrinsic elements of the multifinger structure of a RF nMOS transistor from the used CMOS process.

Based on the analytical equations presented in [10], most of the intrinsic and extrinsic elements have major impact on both cut-off frequencies; however since the expression of f_{max} depends on R_g (which is not the case of f_t), f_{max} can often be decreased through layout optimization. The extraction expressions as well as the cut-off frequencies equations from [10] are presented in Appendix 2.1 and Appendix 2.2, respectively.

The values of f_t and f_{max} of the 65 nm CMOS process from ST Microelectronics were simulated in this work and correspond to the ones presented in [3]: measured f_t/f_{max} = 150/205 GHz for a 60 nm length and 72 µm width RF MOS transistors.

The fact that the system must operate 100 GHz beyond f_{max} defines one of the main challenges of this PhD work: design beyond cut-off frequencies.

When transistors operate near or beyond those frequencies a non-quasi static model is needed. Classic transistor models are based on quasi-static asumptions which means that the charging time of the inversion layer is considered to be instantaneous [11]; this basically admits that the applied gate to source voltage will immediately modify the channel. NQS effects are represented by the r_{nqs} resistor in Figure II-2 (b). This resistor adds a delay together with the C_{gs} capacitor between the V_{gs} voltage and the current source.

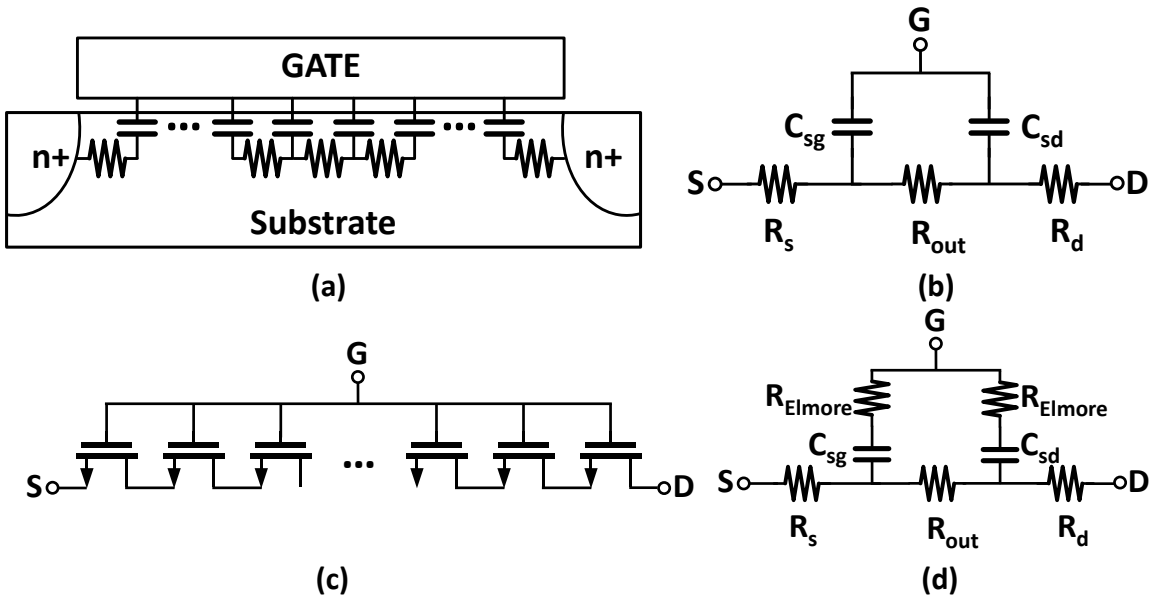


Figure II - 5 : (a) Equivalent RC network. (b) Conventional Quasi-Static model. (c) Equivalent transistor based circuit. (d) Elmore equivalent model [11].

As a matter of fact the channel of a MOSFET is analogous to a distributed RC network (Figure II-5 (a)). In a Quasi Static approach the gate capacitor is plugged directly to both source and drain nodes (Figure II-5 (b)), neglecting completely the finite time for the channel charge to build up. One Non-Quasi Static approach is to replace the RC network by a transistor network (Figure II-5 (c)); this model is very accurate but the simulations are time consuming. Figure II-5(d) shows the equivalent circuit implemented in the used BSIM model in order to represent the non-quasi static phenomena on CMOS transistors; by adding a R_{Elmore} resistor to each lumped gate capacitor the gate time delay is implemented [11]. This equivalent model accurately represents the channel charge build-up because it keeps the lowest frequency pole of the first RC network [11].

The NQS option of the implemented BSIM model of the 65 nm ST microelectronics process is only used in this work for transistors operating beyond 100 GHz.

II.2.2. Passives

In this sub-section the development and the design of passive components is presented. First, a brief description of the 65 nm CMOS back end of line is introduced; second, the passive components provided by the design kit are discussed and finally the developed components using the back end of line are presented such as transmission lines, RF pads and Baluns.

It is common knowledge that the lack of power of CMOS transistors at Sub-THz frequencies is one of the most important limitations of high frequency circuits. For instance, the passive components which prevent the loss of the small amount of power generated by CMOS transistors have even a more important role in mmW/Sub-THz CMOS design, especially for matching networks and waveguides.

II.2.2.1. 65 nm Back end of line

The ST Microelectronics 65 nm CMOS technology offers a Back End Of Line (BEOL) with 7 Copper (Cu) layers: 5 Thin layers (M1 to Mx5) and two thick layers (Mz6 and Mz7). An 8th thick aluminum layer is also present on the top of the BEOL but is mostly used for pads. In typical CMOS design the thin layers are used for interconnections between components (especially transistors terminals) and the thick layers (metal 6 and 7) are mostly used as power supply rails. In mmW/Sub-THz design, the thicker layers (M6 and M7) are used to propagate RF signals because of the better conductivity thanks to larger section of conductors. The lower thinnest layers are mostly used as ground planes and interconnections.

The 65 nm CMOS process from ST microelectronics offers very accurate models for resistors and capacitors at high frequencies, however the inductive components, pads and baluns had to be designed from scratch using the metal layers and via arrays of the BEOL as building blocks.

Figure II-6 (a) shows the metal stacks of various advanced CMOS processes; in Figure II-6 (b) a scanning electron microscope (SEM) image of the 65 nm BEOL is presented as well. Metal and dielectric layers are thinned along with technology progress.

II.2.2.2. Resistors and capacitors

The RF design kit of the 65 nm CMOS technology from ST Microelectronics offers very accurate models and parametric cells of resistors and capacitors. Resistors are only used as DC feeds for gate bias voltages so high accuracy modeling is not necessary.

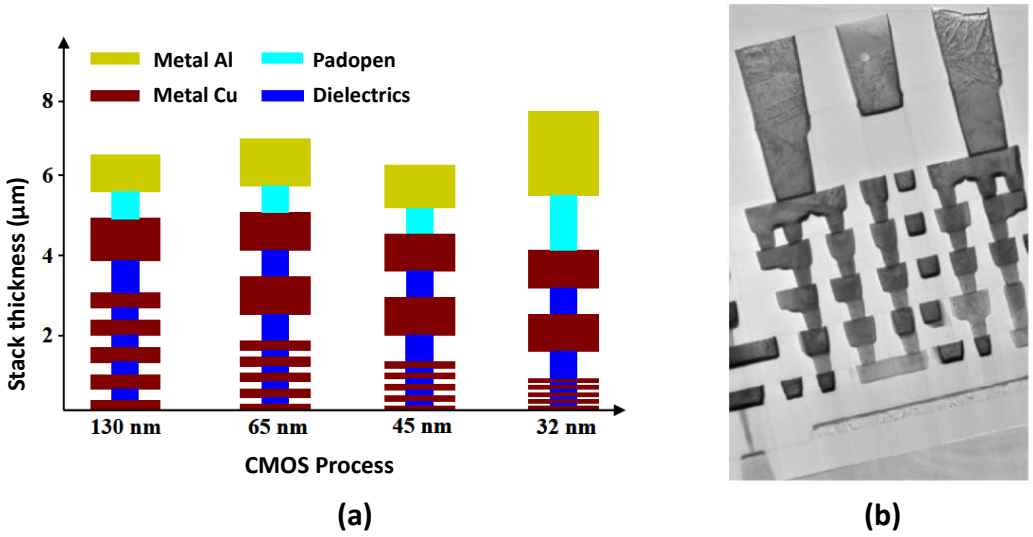


Figure II - 6 : (a) Comparison of stack thickness on different CMOS process [3]. (b) Scanning electron microscope image of ST 65nm CMOS Back end of line [12].

In this work MOM capacitors are used for DC-decoupling and RF-shunts. MOM capacitors have a higher capacity density if compared with the classic parallel plate capacitors and they are compatible with the standard manufacturing process of CMOS. Indeed, MIM capacitors need additional expensive options for fabrication [3]. Even if the use of MOM capacitors does not require high capacitance accuracy (DC Block and RF shunt), the design kit model also takes into account the inductive and resistive behavior added by the layout. Figure II-7 (a) shows a 3D model of a MOM Capacitor from [12] and Figure II-7 (b) depicts the top-section of a MOM capacitor from [3].

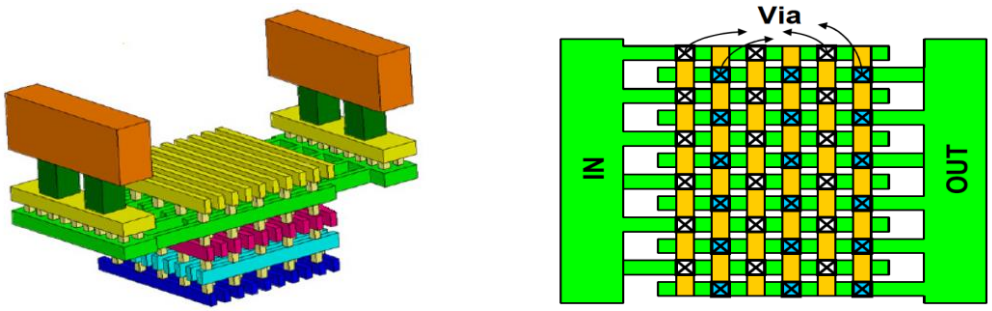
II.2.2.3. Developed passive components

In this sub-section, the development and the modeling of transmission lines, baluns and pads are presented. These components not being present in the design kit library are developed from scratch using the back end of line.

II.2.2.3.1. Thin Film MicroStrip Lines (TFMSL)

The main difference between a classic microstrip line and a TFMSL is the fact that TFMSL are built inside integrated circuits' BEOL. The thin film term comes from the small thickness of the used metal layers and dielectrics. These transmission lines are mostly used in this work

as waveguides for impedance matching, however they accomplish the role of inductances as well. The structure of a TFMSL is presented in Figure II-8.



(a) (b)

Figure II - 7 : (a) 3D model of a MOM Capacitor [12], (b) 2D top-section of a MOM capacitor with via represented [3].

TFMS lines are widely used in mmW and Sub-THz on CMOS because of the shielding ground plane that prevents electric and magnetic fields to penetrate into the lossy bulk silicon substrate. Moreover, the discontinuities such as tee's, bends, underpasses and crosses are easier to implement if compared to integrated coplanar waveguides. In this sub-section, the development of a parametric model, based on full wave simulations is presented. This model was successfully integrated in the used IC design environment (CADENCE/ADS).

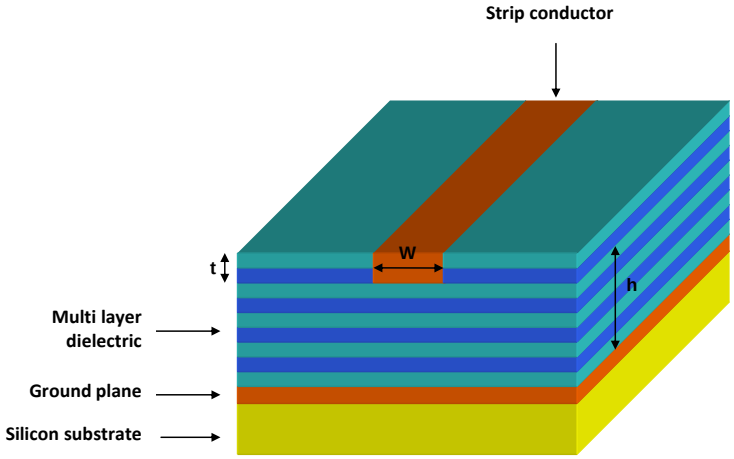


Figure II - 8 : Thin Film micro strip line.

The first step towards proficient 3D full wave electromagnetic simulations is the simplification of the multi-layer of dielectrics and conductors. There are more than 20 dielectric layers on the 65 nm CMOS BEOL; this can cause extremely time consuming electromagnetic simulations.

The dielectric layers are simplified by step of two using the expression developed in [13] in 1977 and successfully used in [14] and [15]:

$$\varepsilon_{r\_eq} = \left(\sqrt{\varepsilon_n} + \frac{h_{n-1}}{h_{n-1} + h_n} \left(\sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n} \right) \right)^2 \quad (4)$$

Metallic layers are made of copper whose conductivity is well known however via arrays between the stacked metallic layers can increase the electromagnetic simulation time. To avoid this, via arrays and metallic layers are merged into a unique fully-filled conductive layer which presents a modified conductivity due to the smaller density of the via array. The following expression is used to simplify and transform the conductivity of the new metallic layer:

$$\sigma_{eq} = \frac{\sigma_m h_m + \sigma_{m+1} h_{m+1}}{h_m + h_{m+1} + t_{via}} \quad (5)$$

Both modifications are presented in Figure II-9. These simplifications are already validated by measurements up to 110 GHz [15]. In this work, HFSS simulations of the used TFMSL structures are made up to 600 GHz. Parametric simulations are also performed varying length and width of the transmission lines.

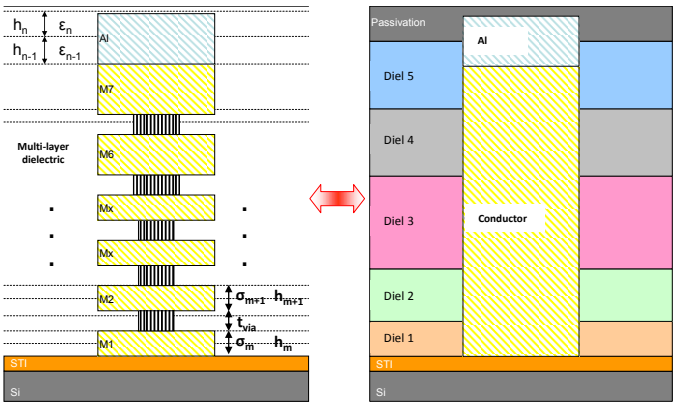


Figure II - 9 : Dielectric and conductor simplifications.

An RLCG model is used to implement all the S parameters data from HFSS to a compact model, the main reasons for this are the fact that this model physically represents the electrical behavior of most kinds of transmission lines and also that it can be frequency based as the S parameters. The schematic of this model is presented in Figure II-10.

Each lumped element represents an infinitesimal part of the transmission line for which the physical length is much lower that the wave length at the frequency of interest. The values

of R,L,C and G are resistance per length, inductance per length, capacitance per length and conductance per length, respectively [16]. Each element of this model corresponds to a lumped representation of a physical behavior operating for the transmission lines; in Table II-1 all the effects and origins represented by these lumped elements are briefly explained.

In order to build a RLCG model from HFSS results (S parameters), the following matrix transformations and calculations are performed: First a matrix transformation from S to ABCD is made; from the classic ABCD matrix transmission lines expressions (equation 6) the formulas of the characteristic impedance (Z_C) and the propagation constant (γ) are extracted directly from simulations results. The classic expressions of Z_C and γ are provided by equation (7) and (8), respectively.

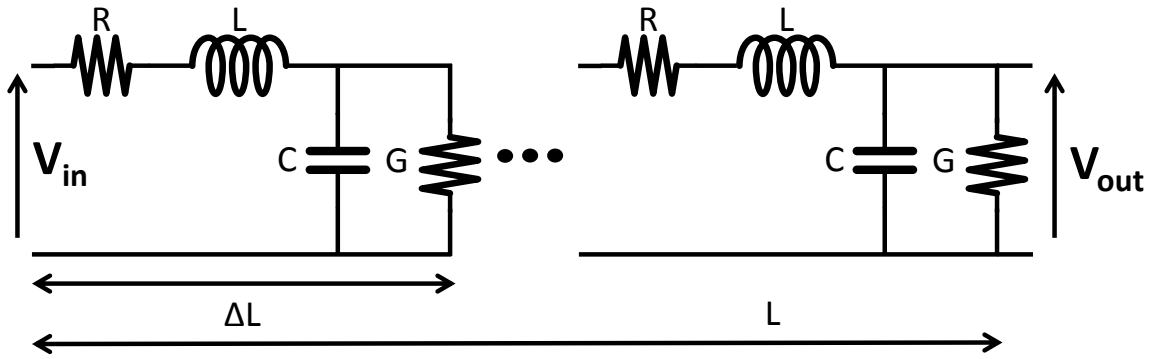


Figure II - 10 : RLCG Transmission line lumped model [16].

From equations (6), (7) and (8) the RLCG expressions can be extracted. These parameters are presented in equation (9), (10), (11) and (12).

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \Leftrightarrow \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma.l) & Z_c.\sinh(\gamma.l) \\ \frac{1}{Z_c}.\sinh(\gamma.l) & \cosh(\gamma.l) \end{bmatrix} \quad (6)$$

$$\gamma = \sqrt{[(R + j\omega L)(G + j\omega C)]} \quad (7)$$

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (8)$$

$$\mathrm{R} = \mathrm{real}(\gamma * Z_c) \quad (9)$$

$$\mathrm{L} = \frac{imag(\gamma * Z_c)}{\omega} \quad (10)$$

$$G = real(\frac{\gamma}{Z_c}) \quad (11)$$

$$C = \frac{imag(\frac{\gamma}{Z_c})}{\omega} \quad (12)$$

This way, the RLCG model is built from simulation results. The implemented RLCG model is in fact a set of empirical equations which fit properly the simulation results from equation (9) to (12) versus frequency and transmission line width. In [15], the same method was used to implement a RLCG model for CPW. The only difference is the fact that in [15] the fitted equations were not the RLCG ones but Z_c and γ (α and β/ε_{eff}).

The entire modeling flow, from test patterns to the CAD implementation is presented in Figure II-11. There are two validation processes in this graphic, the first one represents the verification of the dielectric and metallic simplifications in HFSS and the second one represents the overall accuracy of the cad implemented model if compared with the test results. Figure II-12 shows the attenuation of the transmission lines (dB/mm) vs. the frequency (GHz).

Model Parameter	Origin	Comment
R	Conductance	Atomic property of metal used
	Geometry	Larger cross section = lower R; longer = higher R
	Radiation	Fields not contained are losses
	Skin Effect	Current flows in smaller cross-section as frequency increases
	Proximity	Adjacent conductor's field forces current into smaller cross-section
L	Permeability	Property of metal used
	Geometry	Larger cross section = lower L; longer = higher L
	Skin Effect	Currents at different depths in conductor have different phases, net effect is inductive
	Proximity	Adjacent conductor's field forces current into smaller cross-section
	Radiation	
C	Geometry	Larger area = higher C; closer conductors = higher C
	Permittivity	Higher ε_r = higher C
G	tan(δ)	Higher loss tan = higher losses in dielectric
	Conductance	semiconductor dielectrics
	Geometry	

Table II - 1 : Transmission line RLGC model parameters and sources from [16].

The major interest of a compact model is the efficient use of custom made transmission lines in an industrial CAD environment without any EM simulation after the first implementation; discontinuities such as bends, tee's and underpasses are also implemented.

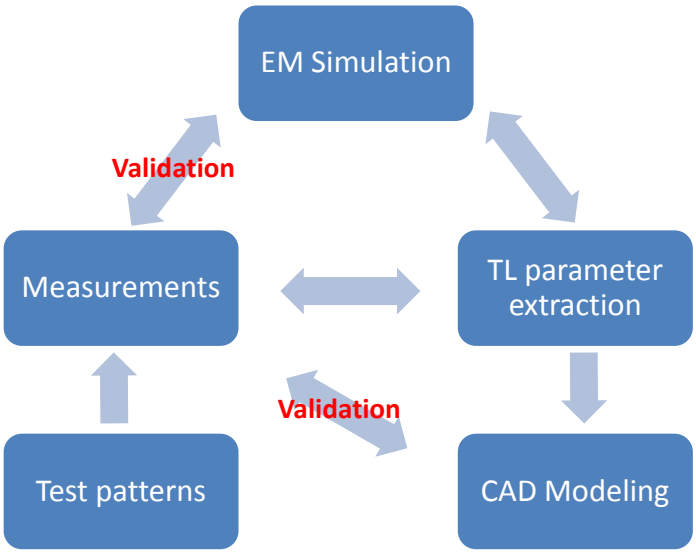


Figure II - 11 : Thin film microstrip line modeling flow.

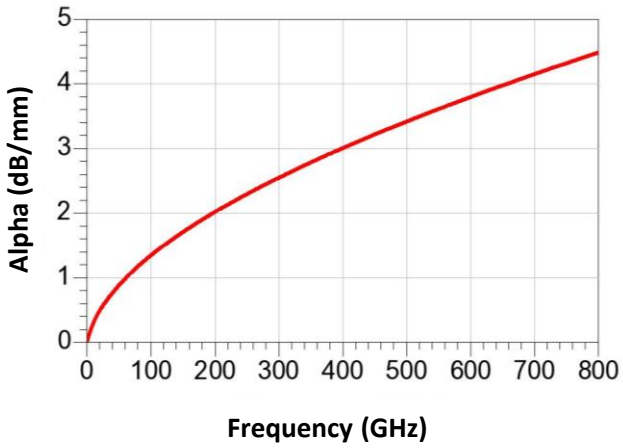


Figure II - 12 : Attenuation (Alpha) vs. the frequency (GHz)

II.2.2.3.2. Baluns

Two baluns were used in this work. The first one is used at 47 GHz to transform a single signal to a differential signal. A second balun was designed at 280 GHz to combine a differential signal to a single signal. Both Baluns were modeled using AGILENT's Momentum. The 47 GHz balun has a 200 µm diameter for 10 µm width and it was designed to achieve sub-harmonic injection in an oscillator. The 280 GHz balun has a 55 µm diameter for 3 µm width and it was designed in order to test the differential output of an oscillator with a single ended probe. Figure II-13 shows a micrograph of the oscillator where both baluns were implemented. This circuit will be presented in detail in chapter III.

II.2.2.3.3. RF Pads

RF pads have a major impact at high frequencies because they have basically a very significant parallel capacitance. Reducing the size of the pad without degrading the testing potential of the integrated circuit requires a lot of experience and feedback from previous measurements. In the case of this work, the most sensitive port is the Sub-THz one (280 GHz).

Using feedback from test engineers, the size of the pad is reduced 25% if compared with the classic 60 GHz mmW pads. The new RF pad is designed using ANSYS's HFSS. A spice model is implemented in CADENCE based on the EM simulation results. In Figure II-14 a snapshot of the HFSS 3D model of the pad is presented as well as the detailed spice model implemented in CADENCE.

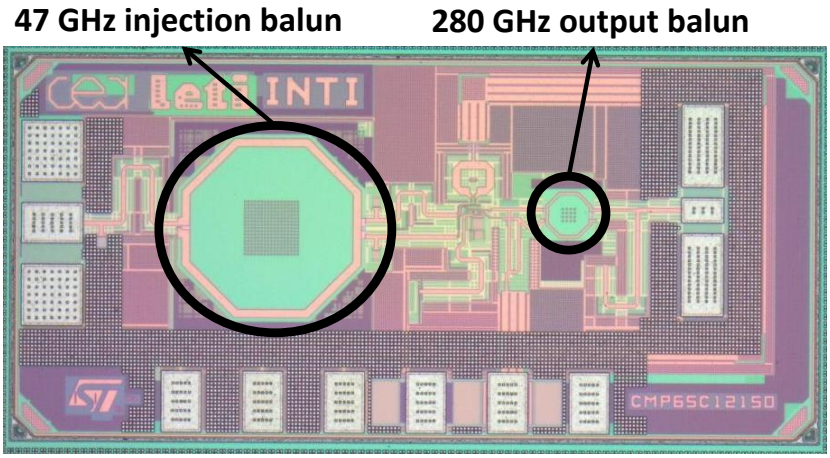


Figure II - 13 : Micrograph of the 280 GHz oscillator; both baluns are highlighted.

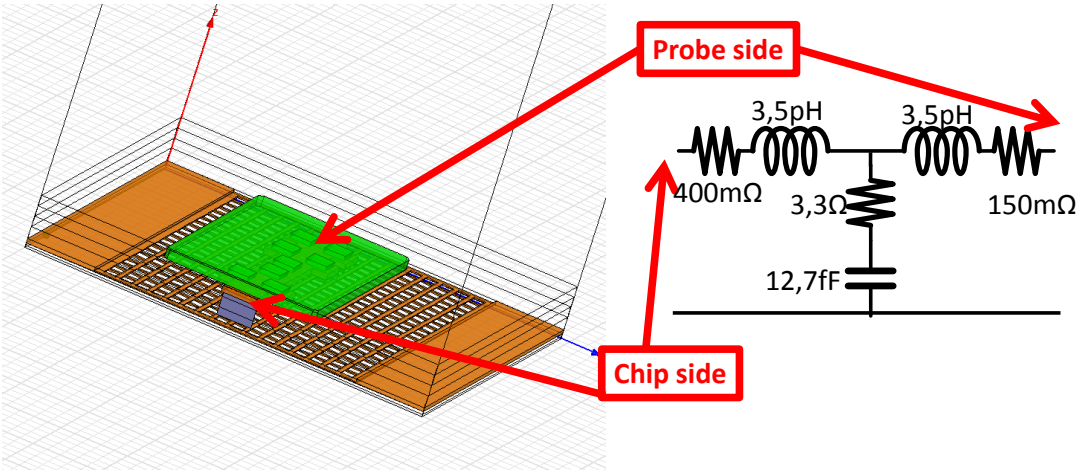


Figure II - 14 : (a) HFSS 3D model of the 285 GHz RF Pad. (b) Detailed spice equivalent model of the 285 GHz RF Pad.

II.2.3. Parasitic extraction techniques

It is common knowledge that inductive, capacitive and resistive parasitic elements have a major impact on the performance of CMOS systems especially at high frequencies. In this sub-section, the developed methods to extract parasitic elements that are added by the interconnections of active and passive components are presented. The goal is to compare different techniques used to evaluate the parasitic extraction.

A simple way to describe these techniques is to use an example: During the first steps of the design of an oscillator, a matrix of varactors is used in order to achieve tuning range. In this example this matrix is studied.

This matrix in fact corresponds to 8 lumped varactors in parallel; this component is designed in order to replace a single bigger varactor, this way the tuning range can be achieved in a more fine way. 7 varactors out of 8 are implemented as a digital control for coarse tuning and the eighth one is responsible for analog fine tuning. Figure II-15 (a) shows the electric schematic of this matrix. Figure II-15 (b) shows the layout implementation of this structure as well as small signal equivalent model representing the frequency behavior of this circuit when all tuning inputs are not connected.

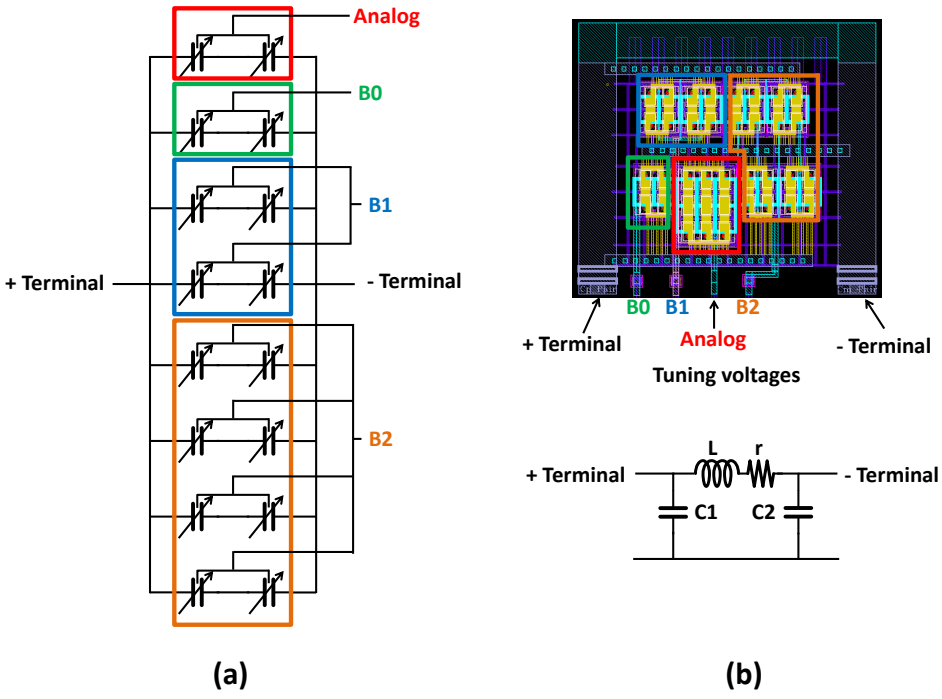


Figure II - 15 : (a) Schematic of the varactor matrix. (b) Layout implementation of the varactor matrix and small signal RLC equivalent model.

There are three methods for parasitic extraction. The first one (classic one) consists on using a standard parasitic tool such as star-rcxt or calibre and perform an RCc extraction of the

layout. The second method uses the previously developed transmission line (TFMSL) models and performs a standard RCc extraction only on the components provided by the design kit and connected to the top access metals. The macroscopic accesses behavior is represented by the transmission lines models. The third method divides the modeling areas like the second method, but the macroscopic accesses and paths are modeled by EM simulations using AGILENT's Momentum.

In order to evaluate and analyze each of the three methods, the RLC components are extracted and plotted in Figure II-16.

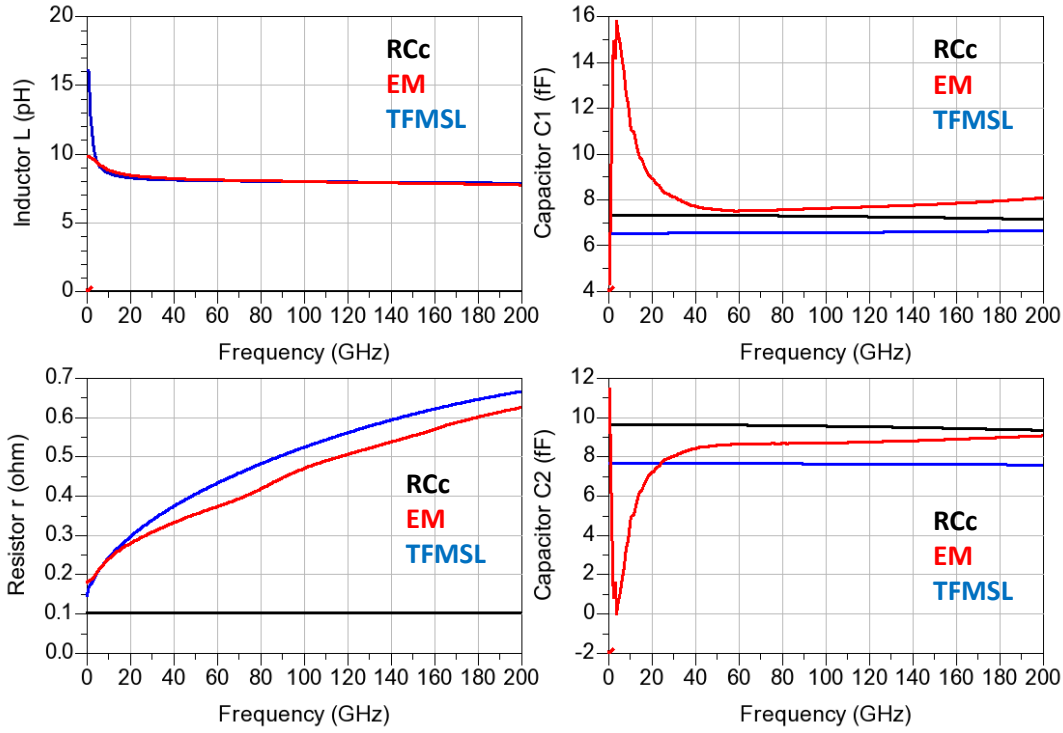


Figure II - 16 : The RLC components versus the frequency for all three parasitic extraction methods.

In terms of inductive effect, both the EM and TFMSL methods present similar results however the standard RCc extraction does not provide any inductive component (as expected). Regarding the resistance extraction, RCc method only provide a DC resistance whereas the EM and TFMSL methods show the resistance increasing with frequency as a result of the skin effect.

On the subject of capacitance extraction, the three methods presented high accuracy in the extraction nevertheless the TFMSL method does not calculate capacitive coupling and because of that, the extracted values are slightly smaller if compared with RCc and EM method.

Three different methods were presented, evaluated and analyzed. In terms of accuracy, the EM and TFMSL methods have the advantage over the standard RCC however the EM methods is very time consuming because of all the layout preparations and simulation time. In this work the EM and TFMSL are used most of the time and the choice depends on the specific situation and layout complexity. In every case the RCc extraction of the local design kit component is made. A summary of this evaluation is presented in Table II-2.

Method	RCc	TFMSL	EM
Inductance	NA	Accurate	Accurate
Resistance	Just DC	Accurate	Accurate
Capacitance	Accurate	Accurate but no coupling	Accurate
Preparation	Easy	Moderate	Hard
Implementation	Easy	Easy	Hard
Time consuming	Low	Low	High

Table II - 2 : Summary of the three parasitic extraction method results

II.3. Receiver specifications

In chapter one the advantages of the heterodyne detection over the direct detection were established in terms of THz imaging applications. In this sub-section, most of the architecture choices are justified. Also a preview of the possible techniques to achieve design beyond cut-off frequencies is introduced. In figure II-17, the classic architecture of a modern heterodyne receiver is presented.

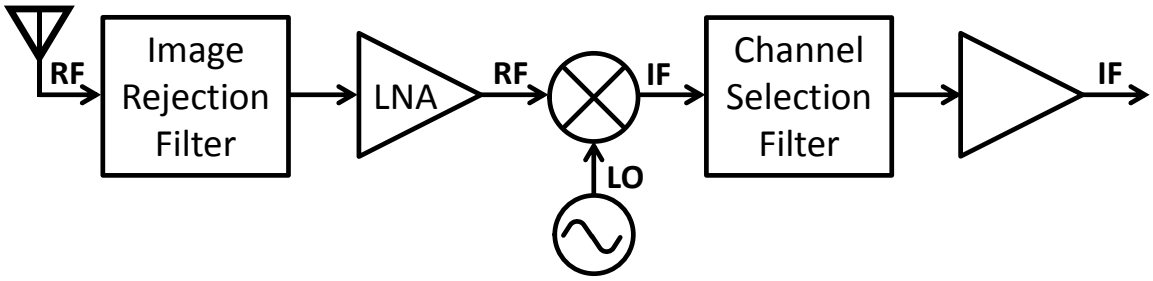


Figure II - 17 : Classic architecture of a heterodyne receiver.

An heterodyne receiver is basically a frequency down conversion of the RF signal band to an intermediate frequency (IF) signal. In other words the RF signal band is translated to a much lower frequency. The term heterodyne derives from *hetero* (different) and *dyne* (dynamic)[17]. The downconversion operation is effectuated using a mixer. This component behaves as an analog multiplier and generates the following mixer products: $F_{RF} \pm F_{LO}$. Since the addition of the RF and LO frequency is really high and the goal is to downconvert the RF signal, the wanted mixer product is F_{RF}-F_{LO} also known as the intermediate frequency (IF).

Because of the fact that the f_t/f_{max} of the 65 nm CMOS technology is 150/205 GHz [3] and the RF signal is defined at around 280 GHz (according to chapter 1), the first modification from the classic schematic of a heterodyne receiver is the suppression of the low noise amplifier (LNA). The main application of this receiver is to perform heterodyne detection for THz imaging, this disables also the need of a channel selection filter and an image rejection filter.

In more classic frequency bands, the IF is defined taking into account the tradeoff between image rejection and suppression of nearby interferers [17] (supposing that the used architecture is based on Figure II-17). In this work, since an image rejection filter is not used and the lack of near 280 GHz interferers signals is obvious, this tradeoff has no use. The IF value is chosen from 40 MHz to 2 GHz. The only requirement for this is a local oscillator and a mixer capable of operating around 280 GHz.

The receiver mixer is passive since it has to operate beyond f_t/f_{max}. At lower frequencies passive mixers are mostly used because of their linearity [18], low conversion loss and absence of power consumption. At Sub-THz frequencies this kind of mixers is used for a unique reason: operation beyond cut-off frequencies. The work of [19] using cold fet for self-mixing purposes has demonstrated operation beyond 600 GHz many times.

The absence of low noise amplifier in the receiver deteriorates considerably the overall noise figure since the first component of the front end is passive. In order to overcome this, the local oscillator must generate enough amplitude to decrease the mixer conversion loss and thus the overall receiver noise figure.

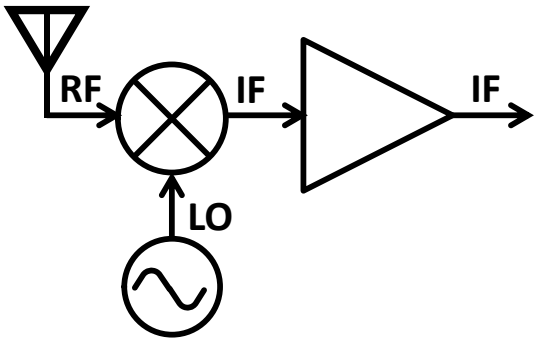


Figure II - 18 : Heterodyne receiver architecture adapted to Sub-THz operation on CMOS.

To achieve oscillation beyond f_{max} the common technique is the harmonic generation, which means that a fundamental tone is generated below f_{max} and then higher harmonics are boosted by different means and techniques. Second [20], third [1] [21] and fourth [22] [23] harmonic generation are the most common techniques. In this work the oscillator must

operate at around 280 GHz. The modified architecture of the heterodyne receiver is presented in Figure II-18.

II.4. Conclusion

This chapter provided a useful background for a better understanding of this entire work. In the context the evolution of both cut-off frequencies was presented and the fact that they are starting to approach Sub-THz frequencies for advanced CMOS processes was highlighted. This evolution was accompanied by a brief discussion about the main differences of advanced technologies such as SiGe and III-V compounds with standard CMOS processes; it was established that even if SiGe bipolar transistors present higher cut-off frequencies at this current time, the CMOS technologies have the advantage for long term development.

Following the context, the Sub-THz behavior of the used CMOS process was presented. In that sub-section all the active and passive components were presented as well as the components developed from scratch using the back end of line such as transmission lines, baluns and RF pads. Also three different techniques of parasitic extraction were presented and evaluated in this sub-section.

In the third sub-section of this chapter the overall heterodyne receiver specifications were presented. Most of the architectural choices were justified using the context and the limitations of CMOS process. Moreover, some techniques for design beyond f_t/f_{max} were presented such as using passive cold FET for mixers and higher harmonics generation for oscillators.

II.5. References

[1] O. Momeni and E. Afshari, “High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach,” *Solid-State Circuits, IEEE J.*, vol. 46, no. 3, pp. 583–597, 2011.

[2] Y. Mao, K. Schmalz, J. Borngraber, J. C. Scheytt, and J. Borngräber, “245-GHz LNA, Mixer, and Subharmonic Receiver in SiGe Technology,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 12, pp. 1–11, 2012.

[3] X. TANG, “Apport des lignes à ondes lentes S-CPW aux performances d’un front-end millimétrique en technologie CMOS avancée,” Université de Grenoble, 2012.

[4] A. Siligaris, “Modelisation Grand Signal de Mosfet en hyperfréquence : Application à l’étude des non linéarités des filieres SOI,” Université des Sciencee et Technologies de Lille, 2004.

[5] T. Parenty, “Etude et perspective des transistors à hétérostructure AlInAs/GaInAs de longueur de grille inférieure à 100nm et conception des circuits intégrés en bande G,” Université de Sciences et Technologies de Lille, 2003.

[6] J. A. Alamo, D. Kim, T. Kim, D. Jin, D. A. D. A. Antoniadis, J. A. del Alamo, Dae-Hyun Kim, Tae-Woo Kim, and Donghyun Jin, "III–V CMOS: What have we learned from HEMTs?," in *Compound Semiconductor Week (CSW/IPRM), 2011 and 23rd International Conference on Indium Phosphide and Related Materials*, 2011, pp. 1–4.

[7] A. Margomenos, "A Comparison of Si CMOS and SiGe BiCMOS Technologies for Automotive Radars," in *2009 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2009, pp. 1–4.

[8] Guofu Niu, Jin Tang, Zhiming Feng, A. J. A. J. Joseph, D. L. D. L. Harame, G. Niu, S. S. Member, J. Tang, and Z. Feng, "Scaling and technological limitations of 1/f noise and oscillator phase noise in SiGe HBTs," *Microw. Theory Tech. IEEE Trans.*, vol. 53, no. 2, pp. 506–514, 2005.

[9] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[10] A. Siligaris, G. Pailloncy, S. Delcourt, R. Valentin, S. Lepilliet, F. Danneville, D. Gloria, and G. Dambrine, "High-Frequency and Noise Performances of 65-nm MOSFET at Liquid Nitrogen Temperature," *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1902–1908, Aug. 2006.

[11] M.-C. J. Weidong Liu, Xiaodong Jin, James Chen, M. C. Zhihong Liu, Yuhua Cheng, Kai Chen, P. K. K. and Kelvin Hui, Jianhui Huang, Robert Tu, and C. Hu, "BSIM3v3.2 MOSFET MODEL, Users' Manual." 1998.

[12] N. Seller, "Contribution à l'Étude, au Développement et à la Réalisation d'Oscillateurs à Contrôle Numérique en Technologie Silicium Avancée," Université de Bordeaux I, 2008.

[13] A. Kraszewski, "Prediction of the dielectric properties of two-phase mixtures," *J. Microw. Power*, vol. 12, no. 13, pp. 215–22, 1977.

[14] C. Pavageau, "Utilisation des technologies CMOS SOI 130 nm pour des applications en gamme de fréquences millimétriques," Université de Sciences et Technologies de Lille, 2005.

[15] A. Siligaris, C. Mounet, B. Reig, P. Vincent, C. E. A. Leti-minatec, and G. Cedex, "CPW and discontinuities modeling for circuit design up to 110 GHz in SOI CMOS technology," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE* , 2007, pp. 295–298.

[16] B. C. Wadell, *Transmission Line Design Handbook*. Arctech House , 1991.

[17] B. Razavi, *RF Microelectronics*, 2nd ed. New York: Prentice Hall, 2012.

[18] F. Ellinger, “26.5-30-GHz Resistive Mixer in 90-nm VLSI SOI CMOS Technology With High Linearity for WLAN,” *Microw. Theory Tech. IEEE Trans.*, vol. 53, no. 8, pp. 2559–2565, 2005.

[19] U. R. Pfeiffer, E. Öjefors, A. Lisauskas, H. G. Roskos, and E. Ojefors, “Opportunities for silicon at mmWave and Terahertz frequencies,” in *Bipolar/BiCMOS Circuits and Technology Meeting, 2008. BCTM 2008. IEEE* , 2008, pp. 149–156.

[20] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C.-M. Hung, K. K. O, and C. P. Antenna, “A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna,” in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International* , 2008, pp. 472–629.

[21] Y. Zhao, J. Grzyb, and U. R. Pfeiffer, “A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology,” in *2012 Proceedings of the ESSCIRC (ESSCIRC)*, 2012, pp. 289–292.

[22] M.-C. F. Daquan Huang and LaRocca, T.R. and Samoska, L. and Fung, A. and Chang, “324GHz CMOS Frequency Generator Using Linear Superposition Technique,” *Solid-State Circuits Conf. 2008. ISSCC 2008. Dig. Tech. Pap. IEEE Int.*, pp. 476–629, 2008.

[23] Y. M. Tousi, O. Momeni, and E. Afshari, “A 283-to-296GHz VCO with 0.76mW peak output power in 65nm CMOS,” in *2012 IEEE International Solid-State Circuits Conference*, 2012, vol. 59, no. 10, pp. 258–260.

PART II: Development

Chapter III: 280 GHz Sub-harmonic injection locked oscillators in 65 nm CMOS

In the previous chapters the context of this entire thesis was introduced: in Chapter I, the frequency band (THz gap) was presented and the main topic in Chapter II was the used process (65 nm CMOS). This chapter describes the development of the different circuits needed in order to implement the Sub-THz heterodyne receivers.

Specifically, this chapter discusses the analysis, the implementation and the measurements of one of the key building blocks of a Sub-THz heterodyne receiver: the oscillator. This particular circuit is also one of the most challenging to design in the receiver chain due to the fact that the oscillator must generate a signal beyond cut-off frequencies; indeed, the used CMOS process f_{max} is 205 GHz and the circuit must operate close to 285 GHz.

As stated in chapter II (II.3), the low f_{max} of the 65 nm CMOS process disables the use of a low noise amplifier at the input of the receiver chain, also knowing that the receiver mixer is passive; the oscillator needs to provide enough output signal swing in order to drive this mixer and to reduce its conversion loss and thus the overall receiver noise figure. Since THz imaging is one of the main applications of this receiver, every pixel of the imager must contain an oscillator: either the image is created by an array of receivers or raster scanning, it's clear that the oscillator must consume low power.

In the first section, the oscillator basics are presented as well as a classification of the various integrated oscillators capable of generating a signal beyond f_{max}. Then, some general points about injection locking are discussed. Moreover the state of the art of CMOS oscillators around 300 GHz is introduced in the second section. Finally, two designed and fabricated oscillators are presented. The architecture, the design and the measurements are treated in section 3 and 4; furthermore a comparison of both integrated oscillators with the current the state of the art is shown in the fifth section.

III.1 Oscillator Basics

In this section, most of the oscillator basics are presented. First, the operating principle as well as the theoretical approaches of oscillators are discussed. Furthermore, the different oscillators architectures adapted to the Sub-THz band are described. Finally, the concept of injection locking in oscillators is introduced and the used techniques to design the circuits are developed.

III.1.1 Operating principle

A simple but quite accurate definition of an oscillator is stated in [1]: "Oscillators are autonomous circuits that produce a stable periodically time varying waveform. They have at least two states and they cycle through those states at a constant pace". Another accurate definition but deeper than the previous one can be found in [2]: "An oscillator generates a periodic output. As such, the circuit must involve a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal".

Based on the previous definitions we can state that oscillators produce periodic signals at one specific frequency and must contain an active mechanism in order to maintain the oscillation stable without attenuation. Those requirements are represented by the Barkhausen conditions in micro-wave oscillator design.

III.1.1.1 Two port approach

In this approach (Figure III-1) the oscillator is observed as a negative feedback amplifier with a close loop transfer function of:

$$\frac{Y}{X}(j\omega) = \frac{H(j\omega)}{1 + H(j\omega)} \quad (1)$$

At a specific frequency ω_1, H(jω) becomes -1 making the close loop gain to tend to infinite. This causes the circuit to amplify the noise of its components at ω_1. In order to ensure the self-sustain of the oscillation a second condition is needed; this condition ensures the positive feedback between the input and output being responsible for the stable oscillations. At ω_1 the phase shift of H(jω) must be 180°[2].

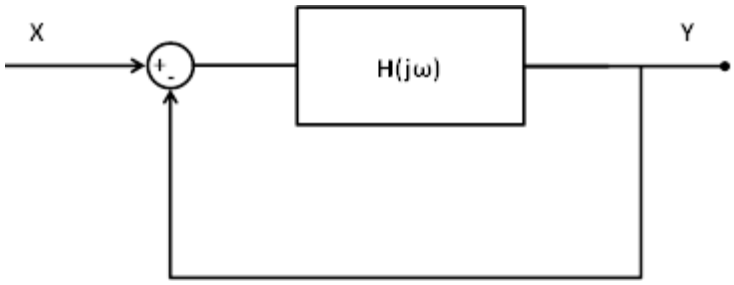


Figure III - 1 : Two port model of an oscillator.

In Figure III-2, the evolution of the oscillating signal during startup can be observed as a suite of fictional "snapshots". In this image, the signal ω_1 is inverted by H(jω) and then subtracted to the original signal creating a waveform of twice the amplitude, (eventually the amplitude growth stops due to nonlinearities).

Summing up, an oscillator needs two conditions in order to operate at a specific frequency without attenuation of the oscillating signal. With this approach the two conditions are represented as the following expressions:

$$|H(j\omega_1)| = 1 \quad (2)$$

$$\arg\big(H(j\omega_1)\big) = 180° \quad (3)$$

Equation (2) corresponds to the self-sustain factor and equation (3) corresponds to the frequency of oscillation.

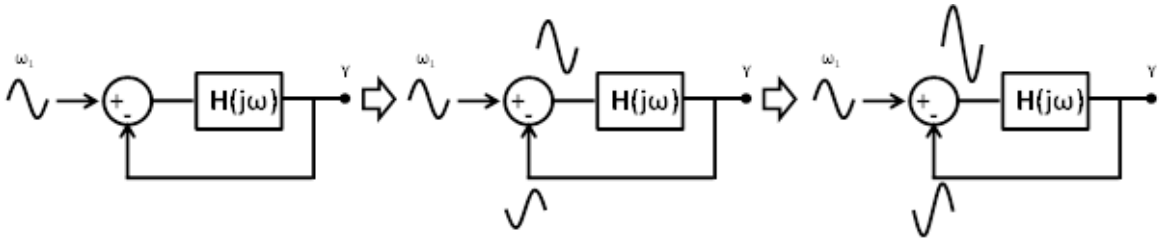


Figure III - 2 : Successive « snapshots » of an oscillator during startup [2].

III.1.1.2 One port approach

The two port network approach is mostly used by the analog circuit community because it is much related to the systems control feedback theory. The microwave community prefers in fact the one port approach, because of its relation with the negative resistance theory, impedance analysis and because it was introduced by Kurokawa in [3] and [4] during the early seventies.

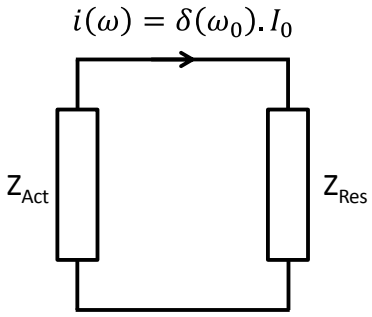


Figure III - 3 : One port model of an oscillator.

In this approach, we consider a lossy resonator with an active circuit that cancels the losses [2]. The frequency is set by the resonator and the self-sustain is provided by the active circuit. It is called one port because it studies the exchange of energy in the parallel connection between the lossy resonator and the active circuit. In Figure III-3 the impedances

of the active nonlinear circuit and the resonator are represented by Z_{Act} and Z_{Res}, respectively.

In the case of an LC oscillator, we assume that the higher harmonics are filtered and the current is purely sinusoidal with I_0 as its amplitude. When oscillating, the sum of Z_{Act} and Z_{Res} must be zero.

$$[Z_{Act}(I_0, \omega_0) + Z_{Res}(\omega_0)]I_0 = 0 \quad (4)$$

The Z_{Act} dependency on I_0 comes from the fact that the active circuit impedance depends on bias currents; thus Z_T is defined as the total impedance of both parts in series:

$$Z_T(I_0, \omega_0) = Z_{Act}(I_0, \omega_0) + Z_{Res}(\omega_0) \quad (5)$$

Z_T is split also in real and imaginary parts:

$$Z_T(I_0, \omega_0) = Re(Z_T) + jIm(Z_T) = R_T(I_0, \omega_0) + jX_T(I_0, \omega_0) = 0 \quad (6)$$

The oscillator condition for the real part is:

$$R_T(I_0, \omega_0) = R_{Act}(I_0, \omega_0) + R_{Res}(\omega_0) = 0 \quad (7)$$

The resonator's impedance real part is positive. Thus, the oscillation start-up condition is rewritten as:

$$R_{Act}(I_0, \omega_0) < -R_{Res}(I_0, \omega_0) \quad (8)$$

With:

$$R_{Act}(I_0, \omega_0) < 0 \quad (9)$$

Equation (9) represents the need of a negative resistance for the self-sustain condition. The frequency of oscillation condition depends on the imaginary part of the total series impedance [5]:

$$X_T(I_0, \omega_0) = X_{Act}(I_0, \omega_0) + X_{Res}(\omega_0) = 0 \quad (10)$$

III.1.2 Oscillators classification (mmW and beyond)

There are three main classes of integrated oscillators: relaxation, ring and LC tuned oscillators. Ring oscillators are built from an odd number of single ended inverters, they can also be built from differential inverters with proper connections [1] [6]; the operating frequency of the ring oscillator depends on the delay time of each inverter. Relaxation oscillators are based on the principle of charge and discharge of a capacitor with a constant

current, this way the oscillation frequency depends on the capacitor size and on the injected current.

LC tuned oscillators use passive resonators (LC tank) in order to set the oscillation frequency. If compared with ring and relaxation oscillators, LC tank oscillators present superior performance in terms of phase noise and frequency stability [1]. To develop an LC integrated oscillator, an inductance, a capacitor and an active circuit which compensates the losses of the LC tank are needed [6].

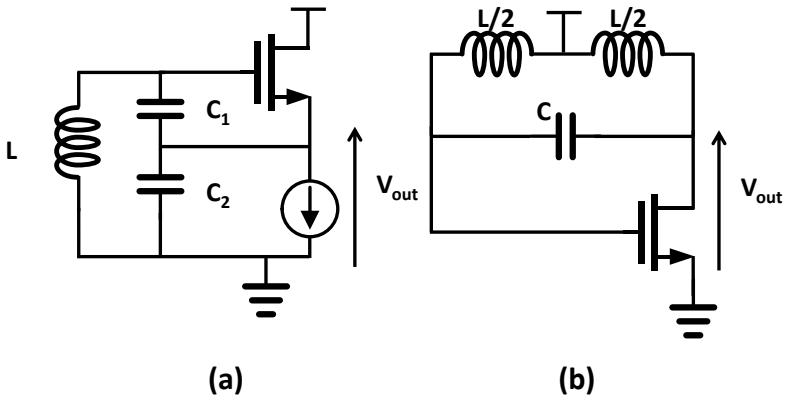


Figure III - 4 : (a) Single Common drain Colpitts oscillator and (b) single Common source Hartley oscillator [6].

Into the category of LC oscillators, there are two principal classes: The Hartley oscillator and the Colpitts oscillator: The Hartley oscillator uses two series inductances with a parallel capacitor whereas the Colpitts oscillators uses two series capacitors with a parallel inductance [6].

As simple as it seems, both architectures were defined at the beginning for one transistor structure; in Figure III-4, a common drain Colpitts oscillator and a common source Hartley oscillator are presented.

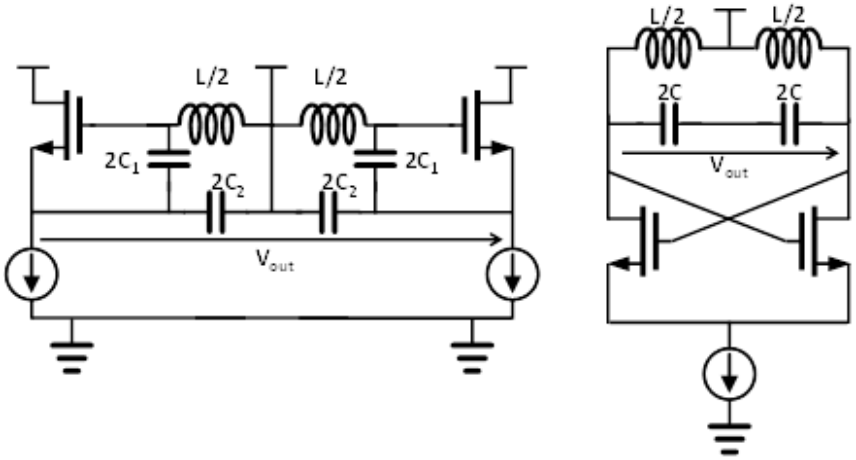
The operation frequency of the Colpitts oscillator is:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{C_1 C_2}{C_1 + C_2}.L}} \tag{11}$$

In a similar way, the oscillation frequency of the Hartley oscillator can be calculated:

$$f_{osc} = \frac{1}{2\pi\sqrt{L.C}} \tag{12}$$

Of course, the two previous calculations examples neglect the internal capacitances of the transistor. In Figure III-5, the differential Colpitts and Hartley are presented; the values of the capacitances and inductances on the schematics are adapted in order to keep equations (11) and (12) valid.



(a) **(b)**

Figure III - 5 : (a) Differential Colpitts and (b) differential Hartley.

In Figure III-5 (b), the differential Hartley structure is one of the most popular high frequency oscillators: the cross coupled pair with a LC Tank. It brings us to the first category of mmW and beyond oscillators: cross-coupled oscillators.

In the interest of achieving operation frequency around 300 GHz, high harmonic boost techniques are needed (push-push, triple-push, quadrature-push, etc.); most of these techniques are developed and explained in the second category of mmW and beyond oscillators: High harmonic boost oscillators.

III.1.2.1 Cross coupled oscillators

The cross coupled pair LC tank oscillators are probably the most used at high speed CMOS systems, they show many advantages that make them very popular: symmetric configuration that promotes high-speed and inherent differential signal, large output swing, low phase noise, reasonable tuning range, low power consumption and operation with low VDD voltages [7]. This architecture is also known for being robust and reliable for RF applications [2]. In the previous frequency calculations, the internal capacitances of the transistors were neglected. Figure III-6 illustrates a small signal equivalent circuit (SSEC) of the used transistor. C_{ds}, C_{gs} and C_{gd} definitely modify the oscillation frequency. Figure III-7 shows the SSEC inserted into the classic cross-coupled LC tank oscillator; the goal here is to calculate the free running oscillation frequency taking into account the transistor

capacitances. For that, we consider that the cross-coupled pair transistors have the same size (W and L) so the capacitances C_{ds}, C_{gs} and C_{gd} of both transistors have the same value.

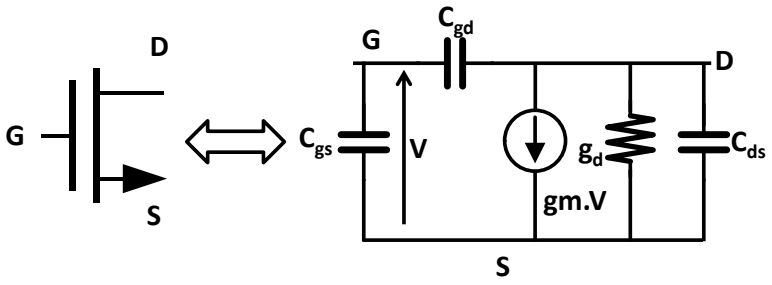


Figure III - 6 : A simplified small signal equivalent circuit of the high frequency nMOS transistor.

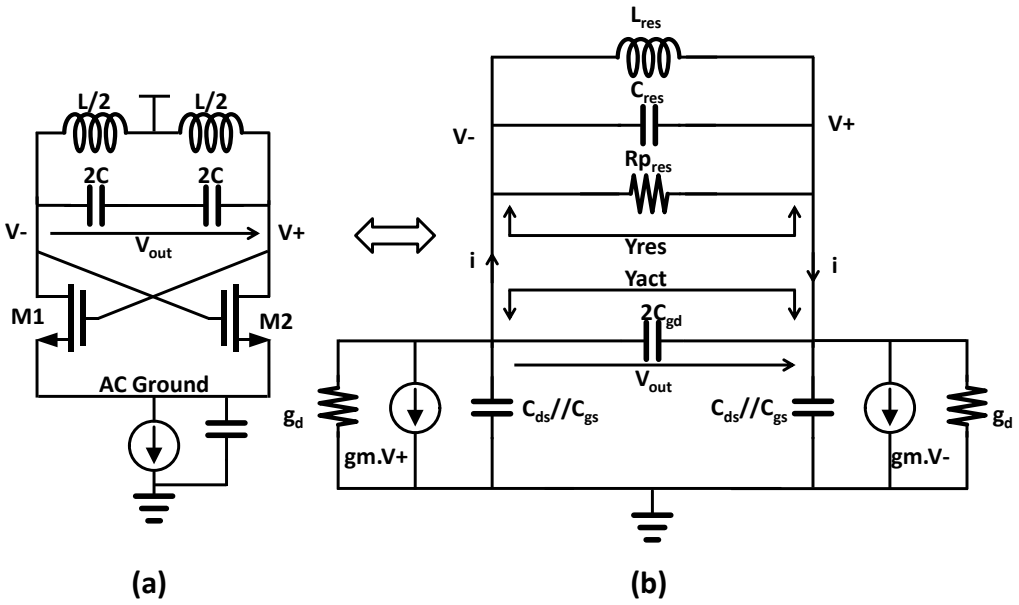


Figure III - 7: (a) Cross coupled LC tank oscillator and (b) its small signal equivalent model.

Because of the parallel nature of the connection between the resonator and the cross-coupled pair, the following analysis is done using admittance calculations:

$$Y_{res} = Y_{Cres} + Y_{Lres} + Y_{Rpres} = jC_{res}\omega + \frac{1}{jL_{res}\omega} + \frac{1}{R_{pres}} \quad (13)$$

$$Y_{act} = 2j\omega C_{gd} + \frac{j\omega(C_{gs} + C_{ds})}{2} + \frac{g_d}{2} - \frac{gm}{2} \quad (14)$$

The oscillation frequency and the self-sustain condition are obtained from (13), (14) and the Barkhausen conditions:

$$F_{osc} = \frac{1}{2\pi\sqrt{L_{res}(C_{res} + 2C_{gd} + \frac{C_{gs}}{2} + \frac{C_{ds}}{2})}} \quad (15)$$

$$gm > gd + \frac{2}{R_{pres}} \quad (16)$$

III.1.2.2 High harmonic boost oscillators

All of the circuits developed in this work were fabricated using the 65 nm CMOS technology. The cut-off frequencies of this process are 150 GHz (f_t) and 205 GHz (f_{max}), this implies that a different set of techniques must be used in order to produce oscillation beyond f_{max}. One solution is to boost higher harmonics; this can allow an output frequency beyond f_{max} and at the same time a fundamental oscillation frequency below this value.

The higher harmonic generation technique is based on the signal rectification at a superior harmonic. Depending on the desired harmonic number (N), this rectified signal is extracted using tuned transmission line at $N*F_0$. F_0 being the fundamental oscillation frequency. This technique is explained in detail using the push-push, triple-push and quadrature-push architectures as examples. This method is also called superposition technique.

III.1.2.2.1 Push-push oscillators

The Push-push oscillator architecture is probably one of the most popular harmonic techniques for high frequency systems; it presents all the advantages of the cross-coupled oscillator and also allows the system to extract the second harmonic. Figure III-8 (a) shows the push-push architecture and Figure III-8 (b) depicts the operating principle by presenting one by one all the involved signals.

As we can observe in this Figure, the differential nature of the fundamental cross-coupled oscillator allowed the extraction of the second harmonic signal at the common mode node v_L. The transmission line is tuned to $\lambda/4$ at 2*F0 in order to maximize the voltage swing at the second harmonic.

In fact the very first oscillators beyond 100 GHz in CMOS used the Push-push technique [8] [9].The main drawback of this architecture is that the extracted second harmonic signal is limited to twice the maximum fundamental oscillation frequency. The analysis performed in Figure III-8 (b) can be extended to the third and fourth harmonic extraction as well.

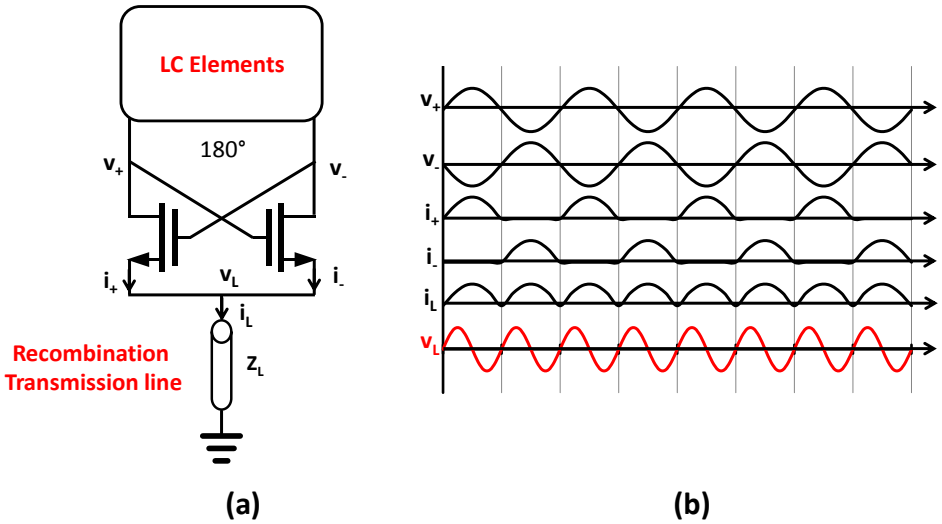


Figure III - 8 : Operating principle of the second harmonic using a cross coupled oscillator.

III.1.2.2.2 Triple-push oscillators

The triple-push architecture was recently introduced to the THz frequencies by [10]. This circuit presented lots of advantages in terms of frequency of operation, output power, dc power and phase noise, the only drawback being the layout complexity.

In the case of the push-push architecture, the extraction of the second harmonic is possible because of the 180° phase shift of the fundamental differential signals. The triple push architecture generates three 120° phase shifted fundamental signals which allows the extraction of the third harmonic.

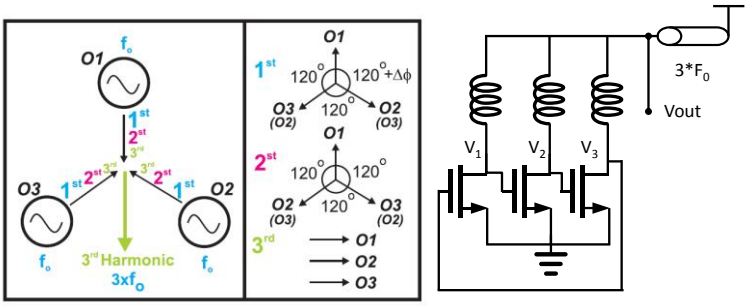
The operating principle is depicted in Figure III-9 (a). As we can observe, this oscillator is a three stage inductive ring oscillator. Because of that, the first and second harmonics are shifted of 120° and cancel themselves at the common node allowing only the extraction of the third harmonic. The transmission line used for the extraction is tuned to $3*F_0$.

This architecture will be explained in detail later in this chapter. Figure III-9 (b) shows the schematic of this oscillator.

III.1.2.2.3 Quadrature-push oscillator.

Other common architecture used by the CMOS community for design beyond ft/fmax oscillators is the quadrature push technique. This circuit allows the extraction of the fourth harmonic as presented in [11] [12] where a quadrature oscillator is used to drive 4 currents

sources in order to obtain the fourth harmonic. The operating principle of this architecture is presented in Figure III-10. The principle is the very similar to the push-push and triple-push architectures but in this case the four currents are not extracted from the oscillator itself but from a second stage circuit.



(a) (b)

Figure III - 9 : (a) Operating principle and (b) schematic of the Triple-Push oscillator [29].

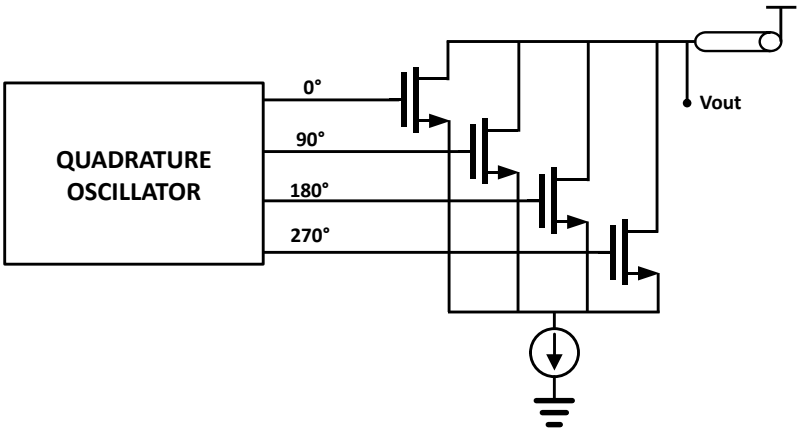


Figure III - 10 : Operating principle of the 4th harmonic extraction superposition technique.

This architecture is based (again) on the signal rectification produced by the four transistors. The four 90° phase shifted current signals are injected into a $4*F_{osc}$ tuned transmission line, generating this way the fourth harmonic. The main drawback of this technique is the lack of power at the fourth harmonic output (-46 dBm [11] [12]).

III.1.2.3 Injection locked oscillator

"The term injection-locked oscillator (ILO) refers to a circuit where two asymptotically stable oscillators are connected unilaterally, with a coupling signal flowing from the master/reference oscillator to the slave/local oscillator" [13]. The main advantage of such a system is the fact that the locked local oscillator tends to copy the phase and frequency characteristics of the reference injection source [14]. It implies that the overall phase noise of the oscillator can be considerably reduced using a low phase noise injection source.

The oscillators presented in this chapter have operating frequencies of 285 GHz and 276 GHz, respectively, and this disables the use of a low phase noise fundamental injection source. For that, both oscillators are locked using an injection source whose frequency (~47 GHz) is set at one sixth of the targeted oscillation frequency. The global oscillator acts as a multiplier by six and thus, the copied phase noise from the injection source becomes:

$$PN_{oscillator} = PN_{ref} + 20\log(6) \quad (17)$$

$PN_{oscillator}$ being the phase noise of the locked oscillator at 285 GHz (or 276 GHz) and PN_{ref} is the phase noise of the injection source at around 47 GHz.

The fact that the local oscillator of the heterodyne receiver is locked allows the phase recovering of the RF signal and this way the detection becomes coherent. This enables the use of the developed heterodyne receiver not only as a coherent detector for Sub-THz imager, but also as a possible communication device around those frequencies. Another advantage of a locked oscillator is the output signal stability which enhances the measurements quality using a spectrum analyzer.

In most cases, injection locked oscillators (sub-harmonic injection locked oscillators in this particular context) are used in RF for the implementation of low-power frequency multipliers, as an easy alternative to an entire PLL operating at high frequency which is often power-expensive. Injection locking can be even used for phase noise measurement techniques as well [13].

Because of the complexity of the architecture, the used transistor models and the locking phenomenon itself, the approach in this work neglects classic locking analysis techniques [15]; instead, it is mainly based on simulations and measurements.

The locking sensitivity of a locked oscillator is a characteristic that can only be extracted by transient simulations and measurements. The obtained Arnold's tongues are displayed in the following sections of this chapter.

III.2 State of the art

Since 2001, when the first CMOS 50 GHz oscillator was published [16], many research groups started working towards higher and higher frequencies. In this section, the state of the art of CMOS oscillators beyond 100 GHz is presented. The evolution is remarkable and it goes hand to hand with the development of new sub-micron CMOS technologies. Some SiGe and InP oscillators are also shown for comparison purposes.

For CMOS oscillators, the oscillation signal frequency is in most cases far beyond the f_{max} cut-off frequency; this is achieved using most of the higher harmonics boosts techniques previously presented in III.1.2.2.

Ref	Architecture	Process	Frequency	Power (dBm)	Free running PhN dBc/Hz	DC Power mW	Year
[9]	Push - Push	90 nm CMOS	131 GHz	-15.2	-108 @ 10 MHz	20	2005
[17]	Push - Push	SiGe Bipolar (fmax=275GHz)	190 GHz	-4.5	-73 @ 1 Mhz	215	2005
[8]	Push – push	130 nm CMOS	192 GHz	-20	-100 @ 10 MHz	16.5	2006
[18]	Fundamental	130 nm CMOS	105.2 GHz	N/A	-97.5 @ 10 MHz	7.2	2006
[19]	Fundamental	InP HEMP 35nm (fmax=600GHz)	250, 300 et 340 GHz	-0.8, -1.34 & -1.6	N/A	11.7 , 7.2 & 11.7	2007
[20]	Push - Push	130 nm CMOS	114 GHz	-22.5	-107.6 @ 10 MHz	8.4	2007
[21]	Fundamental	SiGe Bipolar (fmax = 300GHz)	106 GHz	2.7	-96.6 @ 1 MHz	135	2007
[22]	Fundamental	90 nm CMOS	104 GHz	-8.2	-96 @ 1 MHz (sim.)	6.5	2007
[11][12]	Superposition	90 nm CMOS	324 GHz	-46	-78 @ 1 MHz	12	2008
[23]	Push -Push	40 nm CMOS	410 GHz	-47	N/A	16.5	2008
[24]	Fundamental	90 nm CMOS	128 GHz	-37	-105 @ 10 MHz	9	2008
[10]	Fundamental	130 nm CMOS	104 GHz	-2.7	-93 @ 1 MHz	28	2011
[10]	Fundamental	130 nm CMOS	121 GHz	-3.5	-88 @ 1 MHz	21	2011
[10]	Triple push	130 nm CMOS	256 GHz	-3.5	-88 @1 MHz	71	2011
[10]	Triple push	65 nm CMOS	482 GHz	-7.9	-76 @1 MHz	61	2011
[10]	Triple push	65 nm CMOS	482 GHz	-9	-79@1 MHz	27.5	2011
[25]	4^{th} harmonic	65 nm CMOS	290 GHz	-1.2	-78@1 MHz	325	2012
[25]	4^{th} harmonic	65 nm CMOS	320 GHz	-3.3	-77@1 MHz	339	2012
[26]	Differential Triple push	65 nm CMOS	288 GHz	-1.5	-87@1 MHz	275	2012
[27]	3^{rd} Harmonic	40 nm CMOS	543 GHz	-31	N/A	16.8	2013

Table III - 1 : State of the art of Sub-THz oscillators.

III.3 285 GHz Sub-harmonic injection locked oscillator

This section is dedicated to the design and test of a 285 GHz sub-harmonic injection locked oscillator. This circuit is based on the differential LC tank push-push architecture presented in III.1.2.2.1 but it uses a modified schematic in order to exploit the third harmonic at 285 GHz.

III.3.1 Architecture

In order to extract the third harmonic from a purely differential structure, an active up-converting mixer is used; this circuit multiplies the fundamental differential output with the second harmonic signal generated by the push-push technique.

The architecture of the sub harmonic injection locked oscillator is presented in Figure III-11. A differential oscillator generates the fundamental signal; the second harmonic is obtained using a quarter wavelength transmission line at twice the fundamental frequency (push-push). Both signals are injected into a mixer in order to obtain a third harmonic signal. At the same time, the fundamental oscillator is sub-harmonically locked with an injection signal at half of the fundamental frequency (or one sixth of the overall output frequency).

In Figure III- 12, the transistor level schematic is presented; for analysis purposes the system has been divided into three parts. Part *A* corresponds to the oscillator core: it consists of a cross coupled pair and an inductance that generate the fundamental signal at 95 GHz. The cross coupled pair nMOS capacitances together with the inductance define the fundamental oscillation frequency. The second harmonic is obtained using push-push technique with the help of a short ended quarter wave-length micro-strip line at 190 GHz in the common mode node.

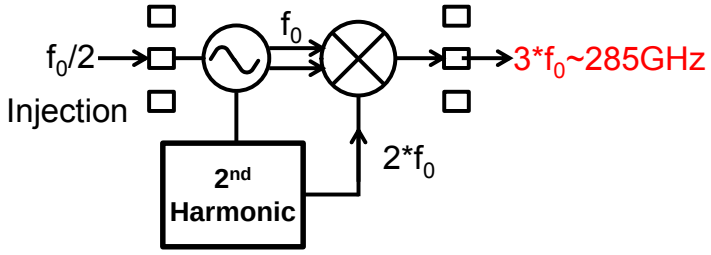


Figure III - 11 : Operating principle of the 285 GHz sub-harmonic injection locked oscillator.

The injection transistors (part *B*) are used for locking the oscillator in order to stabilize the oscillation frequency, fixing the phase noise to the one presented by the injection source, enabling this way the coherent detection in the heterodyne receiver. The injection signal (around 47 GHz) is one sixth of the output oscillation frequency. In order to generate the third harmonic, a single balanced differential active mixer is used to mix the fundamental tone and the second harmonic (part *C*). Output 50 Ohm matching is adjusted to 285 GHz using microstrip transmission lines and an output balun for single ended measurements.

Even if the oscillation mechanism comes only from the fundamental oscillator (Inductance and transistors capacitances), the free running oscillation frequency depends also on the injection and the mixing circuitry transistors; those components add parallel capacitances to the overall tank capacitance.

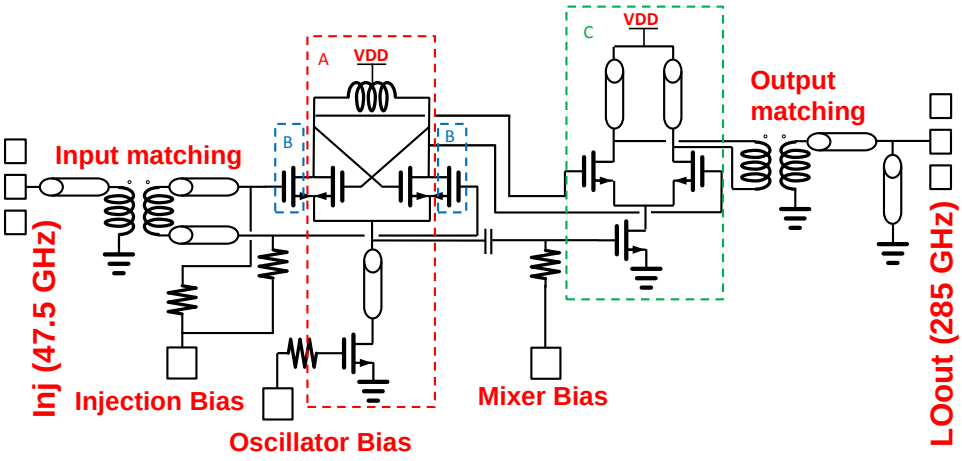


Figure III - 12 : Transistor level schematic of the 285 GHz sub-harmonic injection locked oscillator.

III.3.2 Design

The oscillator, being based on the Figure III-7 circuit, can be analyzed in a similar way. In Figure III-13, a simplified schematic of the small signal equivalent circuit is depicted. Each drawn parallel capacitance corresponds to a different part of the circuit; C_A corresponds to the oscillator core, C_B represents the injection transistors and C_C is the capacitance of the up-converter mixer. Thus, the free running fundamental operation frequency can be expressed as:

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C_A + C_B + C_C)}} \tag{18}$$

C_A can be recovered from equation (15):

$$C_A = 2C_{gd} + \frac{C_{gs} + C_{ds}}{2} \tag{19}$$

The injection transistors bring the differential capacitance C_B:

$$C_B = \frac{C_{gd} + C_{ds}}{2} \tag{20}$$

For the up-converter mixer the equivalent added capacitance is:

$$C_C = \frac{1}{2}\left(\frac{C_{ds}C_{gd}}{C_{ds}+C_{gd}} + C_{gs}\right) \quad (21)$$

C_A, C_B and C_C depend on the transistors size (W, L) and the biasing voltage.

In Figure III-14, the C_A, C_B and C_C capacitances are depicted versus the transistor width. The impact of each part of the circuit can be observed in this graphic; the capacitance C_A from the oscillator core is the one that has the greatest influence on the overall parallel capacitance, followed then by the mixer capacitance C_C and the injection pair capacitance C_B, respectively. More details on the capacitances calculations can be found in Appendix 3.1. As a reminder, in Table III-2, the normalized C_{gd}, C_{gs} and C_{ds} capacitances are presented for a 60 nm gate length transistor.

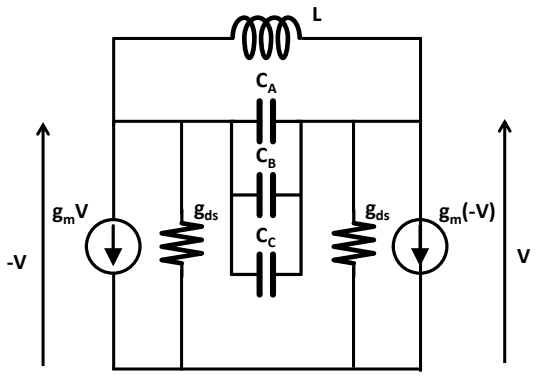


Figure III - 13 : Simplified small signal equivalent model of the 285 GHz sub-harmonic injection locked oscillator.

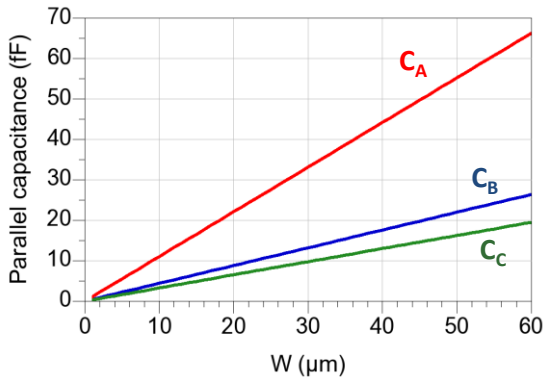


Figure III - 14 : Parallel capacitances values for the same width size.

Capacitance	Value
C_{gd}	0.28fF/µm
C_{gs}	0.72fF/µm
C_{ds}	0.37fF/µm

Table III - 2 : Intrinsic capacitances per µm of the used transistors.

Baluns, matching networks and DC bias resistors have a minor impact on the fundamental oscillation frequency and are not included in the frequency calculation. Since the frequency expression has many variables, the accuracy in the frequency domain extremely depends on the capacitance extraction of all the transistors (intrinsic part and accesses), as well as on the inductance modelling. The inductive components used for the resonator and matching networks are thin film micro-strip lines modelled using full wave electromagnetic simulations with ANSYS HFSS. Injection and output Baluns and pad models are generated using AGILENT MOMENTUM. In order to reduce transistors capacitances, a multi-finger structure is used. More details on the passive components modelling are given in chapter II.

The inductance value was chosen using a layout placement criterion, in order to take into account the geometric form of previously designed and tested transmission lines parametric cells. In this way, the simulated inductance of the transmission lines is as close as possible to the measurements on standard patterns. Using these criteria, the selected equivalent inductance value is around 20.6 pH at 140 GHz.

The calculated values from Figure III-14 and Table III-2 do not take into account the post-layout parasitic capacitances, neither the capacitances added by using thin film micro strip lines as inductances. That being said, the chosen initial fundamental oscillation frequency is around 140 GHz in order to compensate the absence of parasitic modelling at this state of the design.

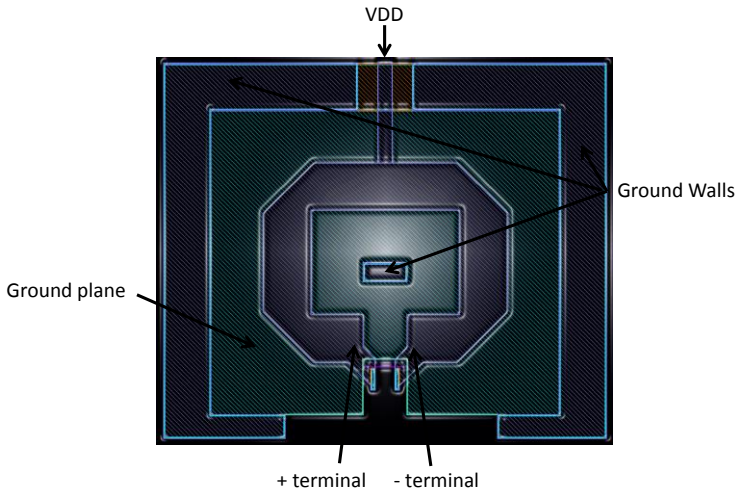
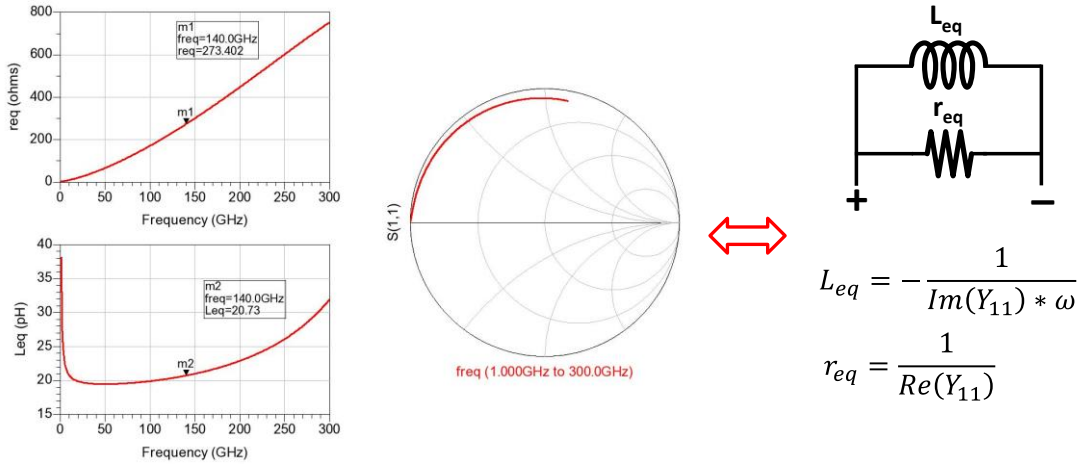


Figure III - 15 : Simplified layout of the resonator inductance.

Figure III-15 is a simplified layout of the inductance used in order to perform electromagnetic simulations. The overall transmission line length is 134 µm and has a width of 10 µm. Figure III-16 (a) shows the simulation results of this component as well as the RL parallel equivalent model (Figure III-16(b)). The total parallel resistance of the inductor is

around 273 Ω at 140 GHz; this is the value that must be compensated by the negative resistance.



(a) **(b)**

Figure III - 16 : Small signal equivalent model of the transmission line based inductor.

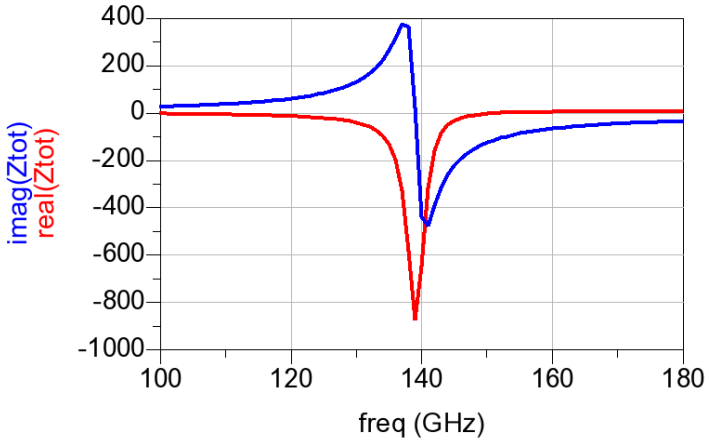


Figure III - 17 : Barkhausen conditions of the fundamental oscillator.

The transistors size were then optimized to achieve fundamental oscillation at 140 GHz and to obtain enough amplitude on the fundamental and on the push-push signals in order to drive the mixer with as much power as possible. In the interest of reducing the impact of the injection and mixer transistors capacitances on the oscillation frequency, the width of the cross-coupled pair transistors is the highest. The optimized values of the three transistor pairs are given in Table III-3.

W_A	W_B	W_C
41 µm	18 µm	15 µm

Table III - 3 : Optimized width values of the cross coupled pair, injection and mixer transistors.

The Barkhausen conditions of the oscillator at around 140 GHz are depicted in Figure III-17.

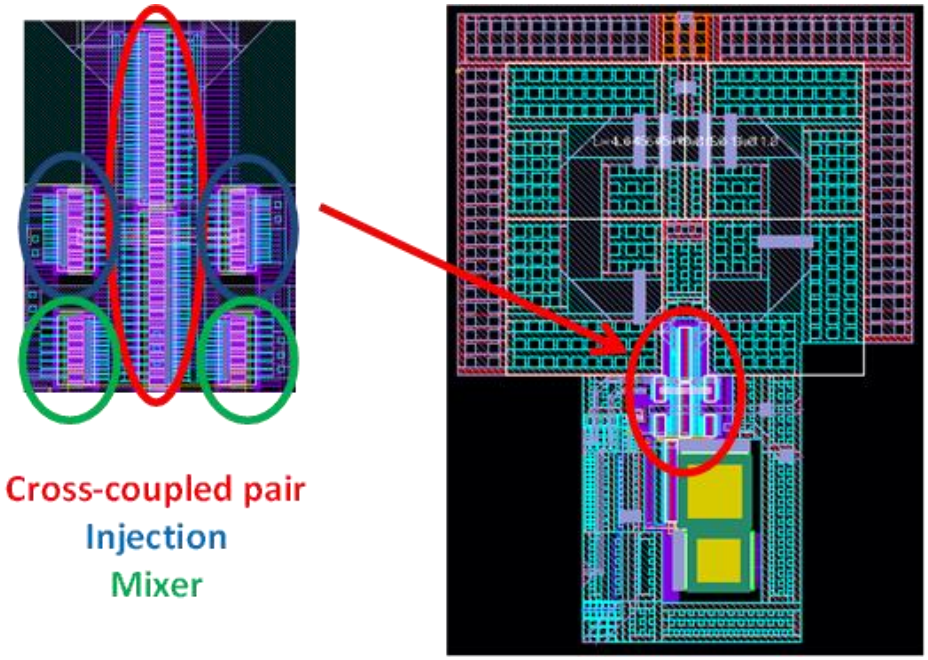


Figure III - 18 : Transistor level implementation of the three transistor pairs.

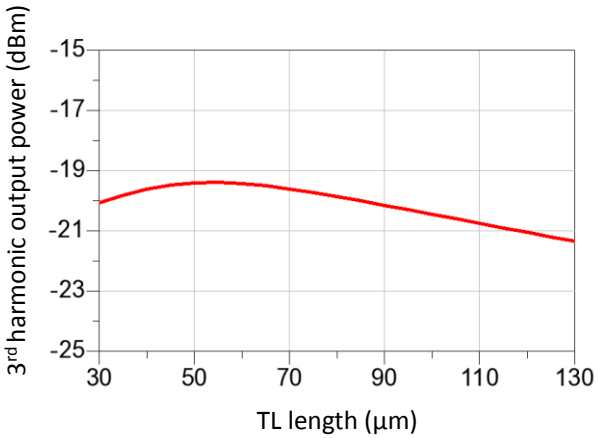


Figure III - 19 : Third harmonic power vs. mixer transmission line length.

Figure III-18 shows the layout of the transistors and the inductance of this oscillator. This implementation allows the extraction of parasitic capacitances which enables the design finalizations such as optimization of the third harmonic output power, fundamental oscillation frequency tuning (95 GHz) and implementation of Baluns and RF pads.

The added capacitances of the layout back end and the transmission lines implementation impact the oscillation frequency but they provide a more accurate model of the entire oscillator core which enables the output power optimization process. Figure III-19 presents the third harmonic output power versus the transmission line size of the mixer output stage.

In Figure III-20, the output power spectrum is shown after the back-end layout parasitic extraction.

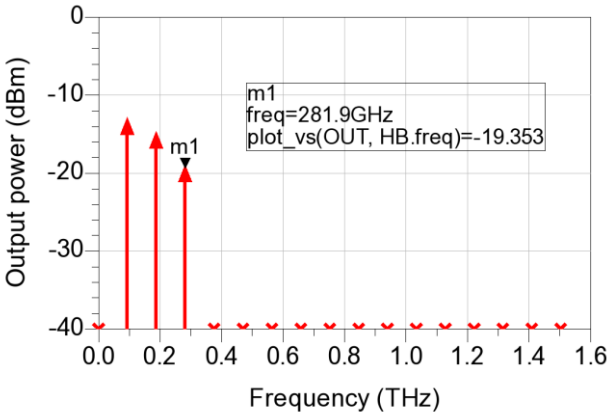


Figure III - 20 : Simulated output power spectrum after the back-end layout extraction.

The up-converting mixer transmission lines were optimized in order to obtain as much power as possible at $3*F_0$, however the isolation aspects were neglected and this causes the lack of rejection of the first and second harmonic that can be observed in Figure III-20. Since the IF band (40 MHz to 2 GHz) is very low compared to the 300 GHz of the RF input, both (fundamental and push-push) non rejected signals have little impact on the IF.

The oscillation frequency can be tuned despite the lack of varactors; in fact, the intrinsic capacitances C_{gs}, C_{gd} and C_{ds} of the cross coupled pair are inherently tuned as the biasing current changes, modifying this way the total LC tank capacitance. Figure III-21 shows the oscillation frequency and output power versus the current bias voltage.

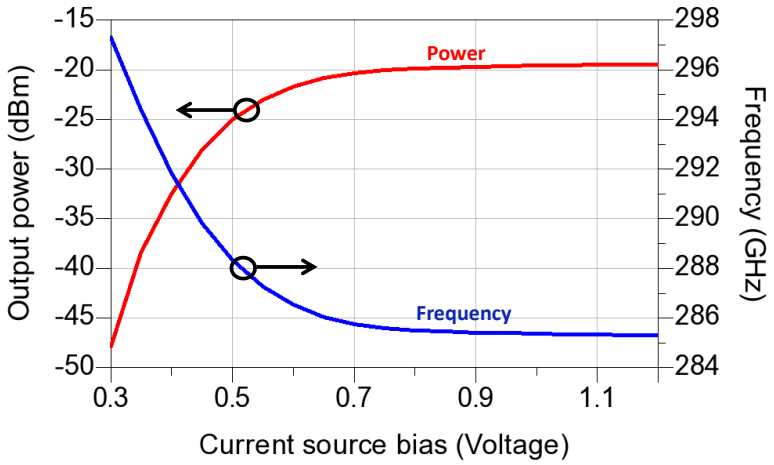


Figure III - 21 : Third harmonic output power and frequency vs. oscillator bias voltage.

It can be observed that this oscillator offers a tuning range from 285.3 to 288.3 GHz with more than –25 dBm output power.

Finally, the total implementation of the 285 GHz sub-harmonic injection locked oscillator is presented in Figure III-22.

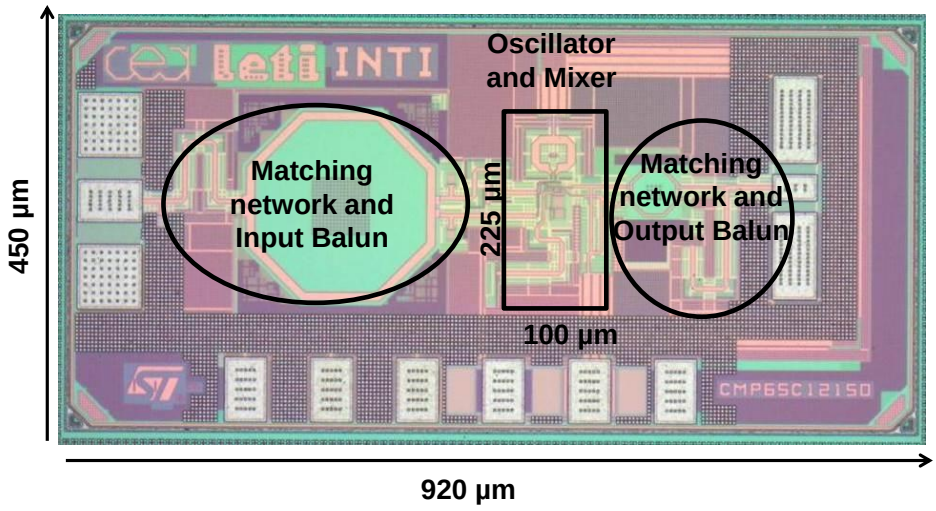


Figure III - 22 : Micrograph of the 285 GHz sub-harmonic injection locked oscillator.

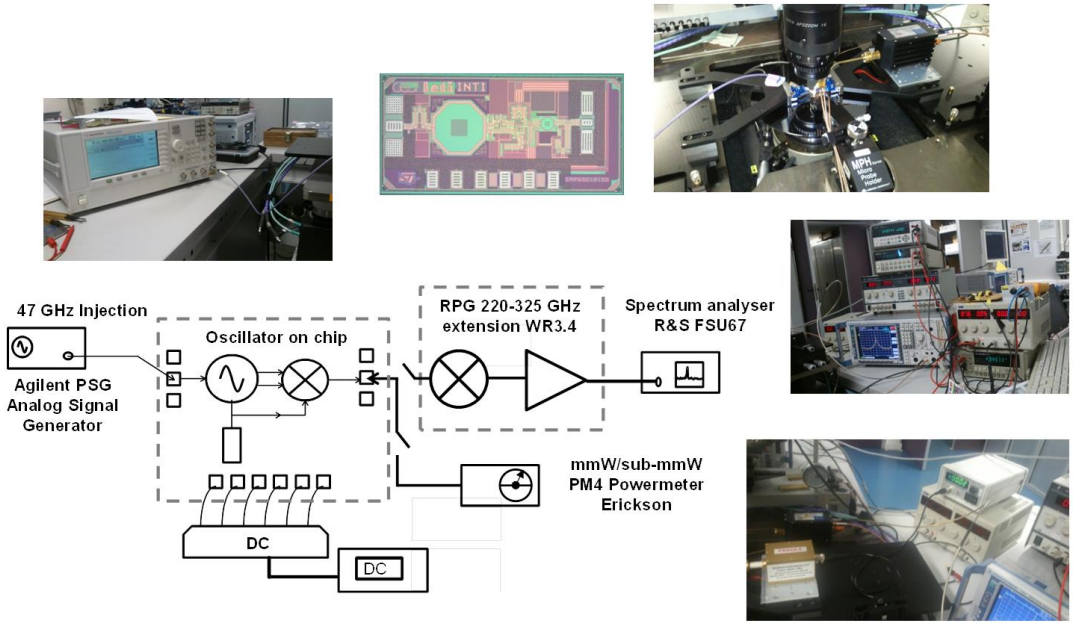


Figure III - 23 : Oscillator test setup.

The overall size of the circuit is 450 µm x 920 µm, including baluns, matching networks and pads. The size of the oscillator core and the up-converting mixer is only 225 µm x 100 µm.

III.3.3 Measurements

This section presents the test setup as well as the measurement results of this oscillator. Output power, oscillation frequency, locking range and phase noise measurements are the hot topics of this sub-section.

For the oscillator characterization a spectrum analyzer is used for operation frequency, locking range and phase noise measurements. Output power measurements are performed with a power meter. Figure III-23 shows the test setup as well as some pictures of the used equipment.

III.3.3.1 Test setup 1: Spectrum analysis

The spectrum analyzer used to perform free running oscillation frequency is a Rhode & Schwartz FSU67; this device is able to analyze signals up to 67 GHz. A 220 GHz to 325 GHz RPG extension is added in order to characterize this oscillator.

In Figure III-24, the free running oscillation frequency and DC power versus the bias voltage are presented; the simulated frequency is also shown for comparison purposes. This test was performed in free running oscillation condition (injection source OFF).

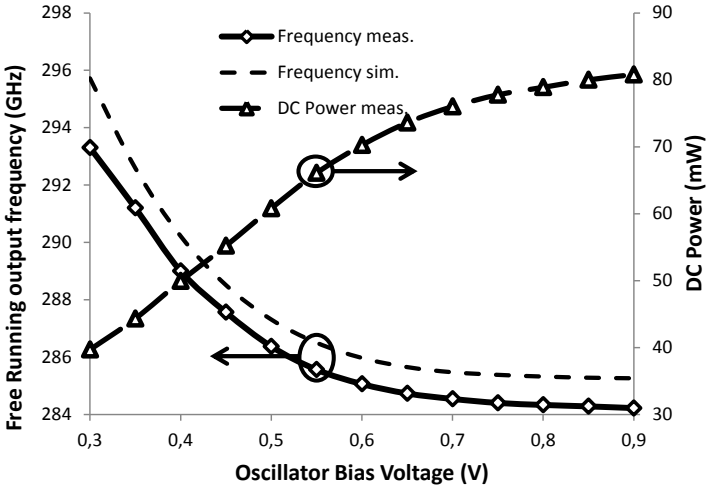


Figure III - 24 : Free running oscillation frequency vs. Bias voltage.

In order to measure the locking range, an injection source (Agilent PSG Analog Signal Generator) is used as shown in Figure III-23. In Figure III-25 the sub-harmonic injection locking sensitivity is presented. The measured frequencies are lower than in the free running regime because the injection transistors are biased and thus their capacitances increased, modifying equation (20). This type of graphic is called Arnold tongue.

It can be observed that at least 8 dBm of injected power is needed to overlap the Arnold tongues, allowing in these conditions to cover a frequency range from 278.7 GHz to 283.08 GHz.

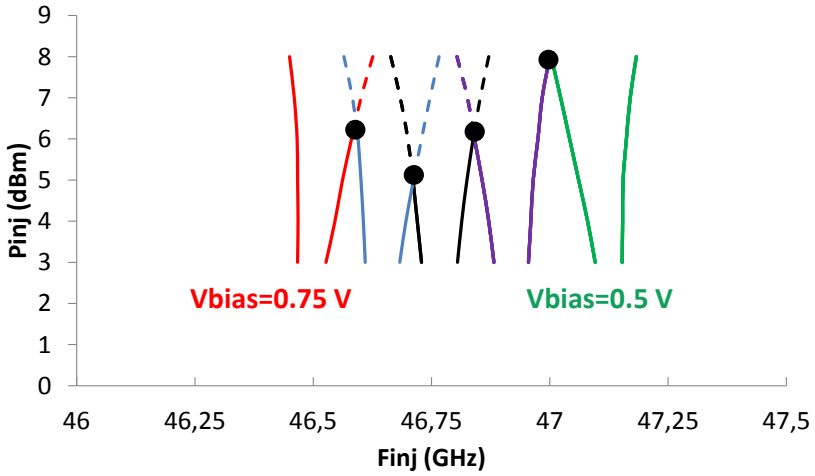


Figure III - 25 : Sub-harmonic injection locking sensibility.

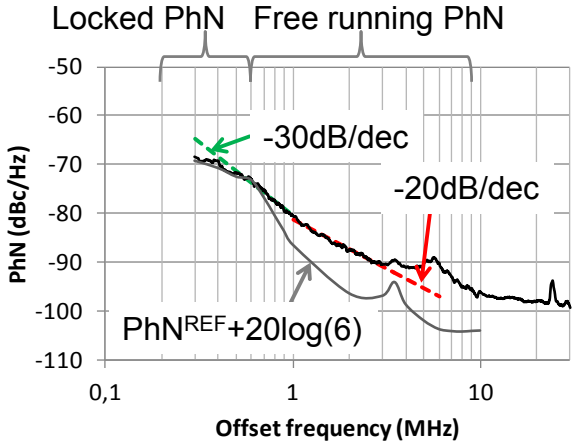


Figure III - 26 : Measured free-running oscillator phase noise.

For phase noise measurements the oscillator was locked, according to [28]; because of the nature of the injection locking phenomenon, the measured phase noise of a locked oscillator when the locking range is smaller than frequency offset "faithfully reflect" the phase noise of the free running oscillator. In Figure III-26, this phenomenon can be observed: up to 700 KHz frequency offset the measured phase noise is the phase noise of the injection source $+20\log_{10}(6)$ which corresponds to the phase noise of the oscillator being locked. For higher frequency offset, the measurement corresponds to the free running oscillator phase noise.

Finally, Figure III-27 shows a snapshot of the locked oscillator spectrum. Note that test bench calibration is taken into account into the spectrum analyzer for this snapshot (probe losses, waveguide losses and RPG 220-325 GHz extension conversion loss).

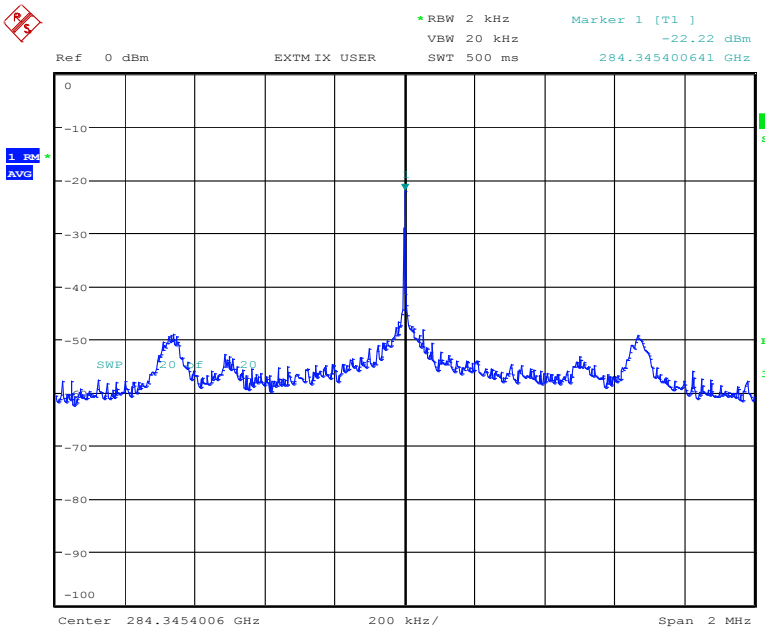


Figure III - 27 : Snapshot of the locked oscillator: Resolution bandwidth = 2 KHz, span = 2MHz, Fosc= 284 GHz and Posc = -22 dBm.

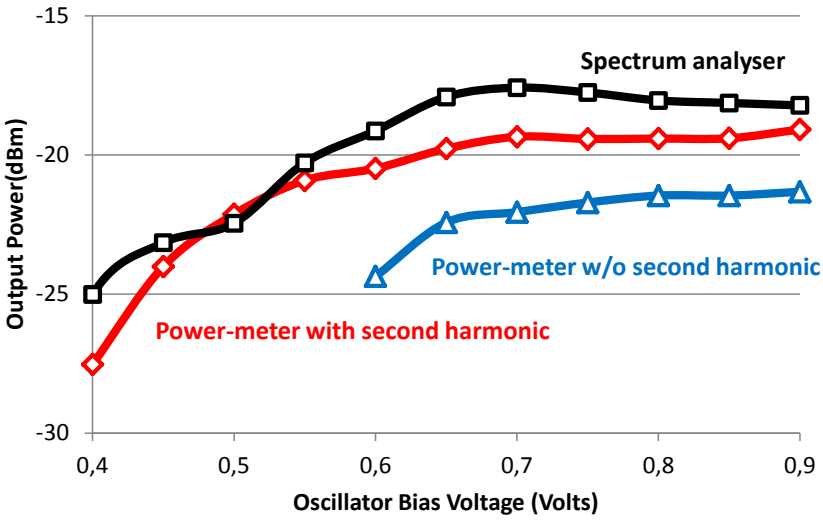


Figure III - 28 : Output power measurements.

III.3.3.2 Test setup 2: Power measurements

For this test setup the Erickson mmW/Sub-mmW PM4 Power-meter is used. The goal is simply to perform accurate output power measurements.

This oscillator was measured twice; the first measurement includes the impact of the second harmonic (~190 GHz). For the second measurement, a filter was added to the circuit output in order to filter out the 190 GHz power and measure only the third harmonic. The output power of both measurements is showed in Figure III-28. The output power provided by the

spectrum analyzer is also given. Note that impact of the second harmonic signal (192 GHz) on the third harmonic output power corresponds to a 3 dBm reduction. The waveguides, probes and transitions losses are taken into account.

The overall performances of the oscillator are presented in Table III-4:

Architecture	Process	Frequency	Output power	DC Power	Tuning	Locking?	Phase noise @ 1 MHz
Push-Push & mix	65nm CMOS	285 GHz	-21dBm	70mW	4.8 GHz	Yes, narrow locking range	-82dBc/Hz

Table III - 4 : 285 GHz sub-harmonic injection locked oscillator performance.

III.4 276 GHz Sub-harmonic injection locked oscillator

In this section, the architecture, design and test of a 276 GHz sub-harmonic injection locked oscillator is presented; the used architecture is called triple-push and is a three stage inductive ring oscillator. This architecture was brought to the high frequencies by [10] and showed superior performance but it was not locked. In this sub-section, the higher performance of this architecture will meet the advantages of a locked oscillator.

III.4.1 Architecture

The basic operating principle schematic of this oscillator is presented in Figure III-29; the architecture is based on three coupled oscillators whose outputs are combined in order to obtain the third harmonic signal.

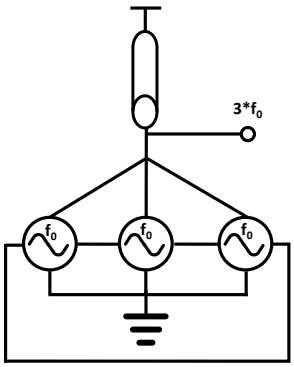


Figure III - 29 : Operating principle of the triple push oscillator.

As a matter of fact, this architecture is a three stage inductive ring oscillator, it generates a fundamental signal from the ring oscillator mechanism and it recombines the output power at a common node; the three 120° phase shifted signals are used to boost the third

harmonic and cancel lower harmonics. The transistor level schematic is shown in Figure III-30. The transmission lines are used as inductances.

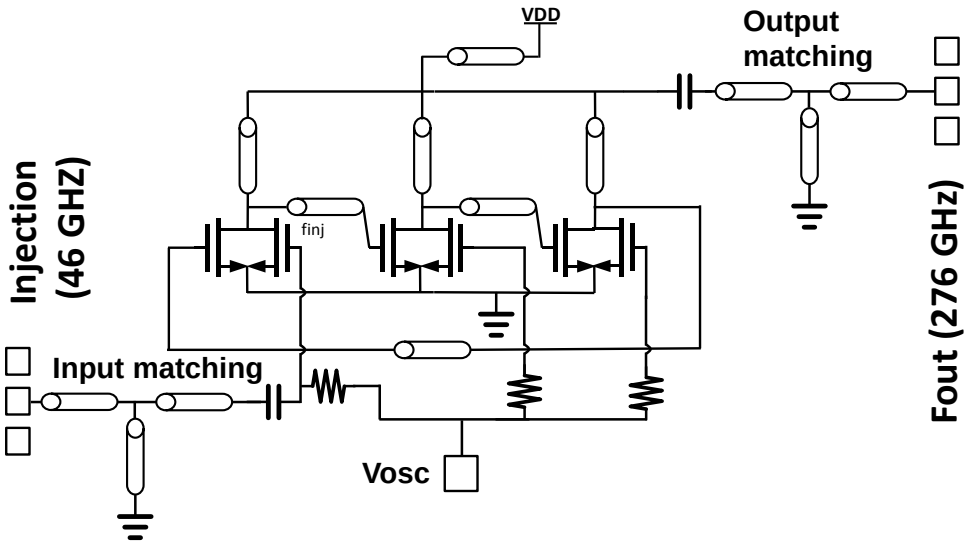


Figure III - 30 : Transistor level schematic of the 276 GHz triple push oscillator.

It can be observed that there are two groups of transmission lines: the first one corresponds to the three transmission lines from the transistors' drains to VDD and the second one consists of the three transmission lines from the transistors gates to drains. The drains to VDD transmission lines provide the needed inductive effect in order to produce oscillation; these lines ensure the 120° phase shift between the three branches of the ring oscillator that allows the extraction of the third harmonic and cancels the lower harmonics. The second group of transmission lines is used in order to change the phase shift between gates and drains increasing massively the output power of each transistor at the third harmonic. A simpler way to see this is analyzing this inductance as a matching network between each transistor drain and the output port at the third harmonic [10]. The transmission lines belonging to the same group must have the same length in order to obtain as much output power as possible at the third harmonic.

III.4.2 Design

Since the drains to VDD transmission lines are the ones responsible for the oscillation of this circuit, they will be used for the analysis of this architecture with the Barkhausen conditions. In order to determine the fundamental operation frequency, a small signal equivalent circuit must be drawn and analyzed (Figure III-31); this schematic does not take into account the second group of transmission lines as well as the C_{gd} internal capacitances of the transistors in the interest of facilitating the calculations. Still the calculated operation frequency expression is useful enough to define a preliminary size of the transistors and inductances.

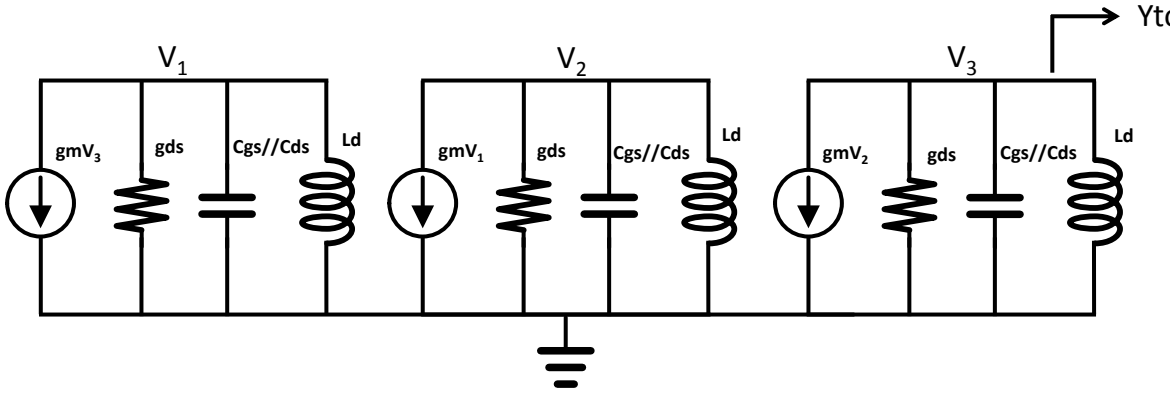
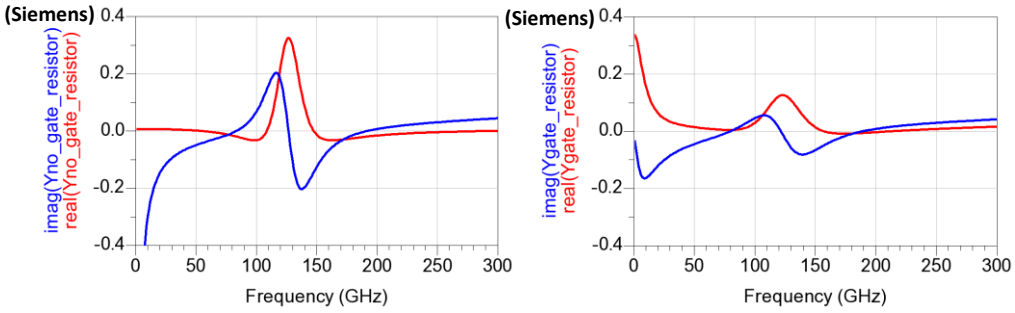


Figure III - 31 : Small signal equivalent model of the triple-push (C_{gd} capacitances not taken into account).



(a) **(b)**

Figure III - 32 : Barkhausen condition of the triple push with (a) and without (b) gate resistors.

The analytical resolution (step by step) is shown in appendix 3.2. The total admittance is given by the following expression:

$$Y_{tot} = j\omega(C_{gs} + C_{ds}) + \frac{1}{jL_d\omega} + gds + \frac{gm^3}{\left(gds + \frac{1}{jL_d\omega} + j\omega(C_{gs} + C_{ds})\right)^2} \qquad (22)$$

The fundamental oscillation frequency and the self-sustain condition can be obtained for the oscillator using the Barkhausen criteria thanks to the equation (22) and are presented in Figure III-32 (a). These results represent the fundamental oscillation frequency.

It can be observed that the real part of the total admittance is negative twice, creating two steady state oscillations at different frequencies (around 85 GHz and 190 GHz), this is caused by the lack of gate resistors in the model. Figure III-32 (b) shows the Barkhausen conditions of the same oscillator with gate resistors taken into account; these resistors have more impact on the real part of the total admittance cancelling this way the first steady state frequency at 85 GHz and keeping the wanted fundamental oscillation frequency at 190 GHz.

The fundamental oscillation frequency is higher than the real oscillator to compensate the lack of C_{gd} internal capacitances, the second group of transmission lines and layout parasitic elements.

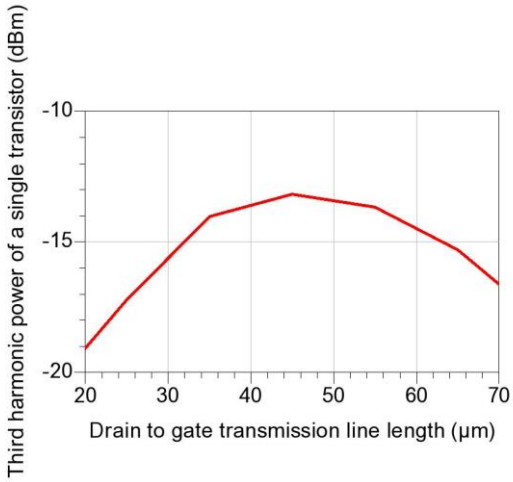


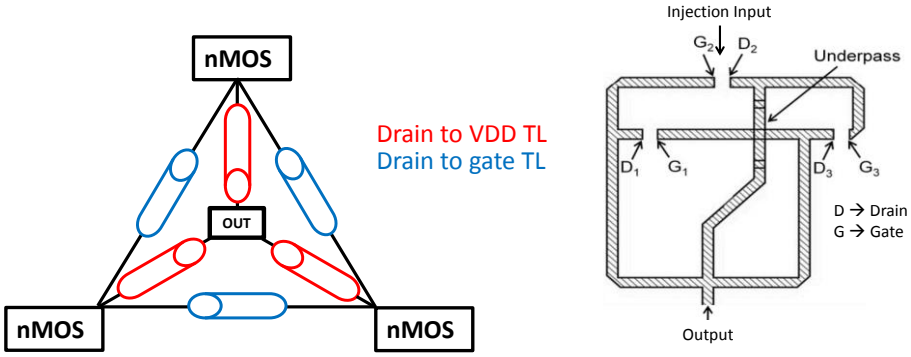
Figure III - 33 : Impact of the drain to gate transmission line length.

As previously stated, the transistors gates to drains transmission lines (second group) increase the third harmonic power of each transistor, these lines change the phase shift between gates and drains. According to [10] there is an optimum phase shift which allows maximum power at the third harmonic. This Figure III-33 shows specifically the third harmonic output power of the drain of a transistor; note that the third harmonic is extracted at the common mode node and not at transistors' drains. The optimization of the third harmonic output power of each transistor allows the overall increase of the output power of the oscillator at the recombination node.

In the state of the art implementations of this circuit at sub-THz frequencies [10] and [26], each transmission line of each group has the same length. Since the oscillator presented in this work is injection locked by an external source, there is one more RF port in the system at 47 GHz. In order to achieve perfectly matched transmission line lengths, the floor plan presented in Figure III-34 (a) must be used. The lack of functionality of a layout of this sort is based on the oscillator output port being on the middle of the system. In this work, the goal is to place the injection port on one side of the circuit and the output port on the opposite side, as presented in Figure 34 (b).

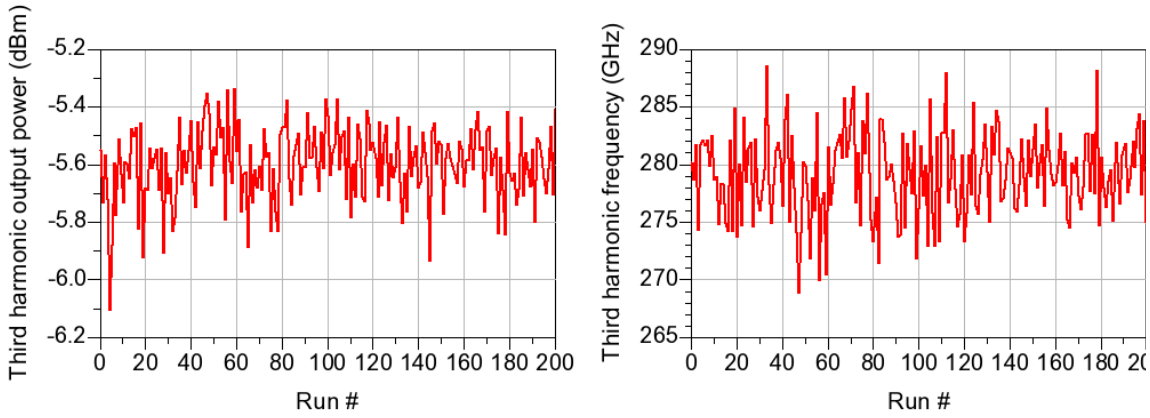
In order to achieve a layout based on this floor plan, the impact of the transmission lines length mismatch on the overall oscillator performance must be studied. This dispersion analysis is presented in Figure III-35: (a) third harmonic output power and (b) oscillation frequency.

The results show a variation of less than 1 dBm for the third harmonic output power; however the oscillation frequency is very sensitive to length variations and fluctuates from 268 GHz to 288 GHz. In conclusion, it can be said that the modifications in transmission lines lengths mostly affect the imaginary part of the total impedance, which is reflected on the frequency variations.



(a) (b)

Figure III - 34 : Geometrical implementation of the triple push layout.



(a) (b)

Figure III - 35: Dispersion analysis of the 6 transmission lines lengths: the length values are randomly changed from 120 to 145 µm (first group) and from 80 to 100 µm (second group).

Table III-5 presents the length values of all the transmission lines in order to implement this structure and have a layout with the injection input port and the output port on opposite sides:

Inductance	Connect	Size
L_{d1}	Drain 1 to VDD	135 µm
L_{d2}	Drain 2 to VDD	128 µm
L_{d3}	Drain 3 to VDD	135 µm

L_{dg1}	Drain 1 to Gate 2	90.5 µm
L_{dg2}	Drain 2 to Gate 3	91.7 µm
L_{dg3}	Drain 3 to Gate 1	85 µm

Table III - 5 : Transmission lines sizes. L_d represents the first group and L_{dg} the second one.

In Figure III- 36, the simulated output spectrum is presented; this result takes into account the post layout parasitic extractions of the transistors, matching networks and the RF pads. It can be observed that this architecture presents better rejection of lower harmonics than the previous one.

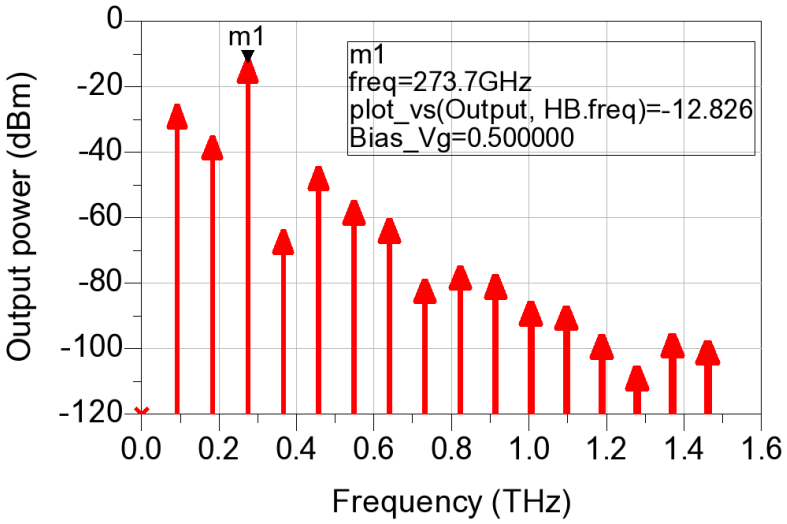


Figure III - 36 : Simulated triple-push output spectrum.

The transmission lines structure presented in Figure III-34 (b) was also simulated electromagnetically using HFSS in order to verify the robustness of the models up to 300 GHz. Figure III-37 shows the third harmonic output power and oscillation frequency versus the oscillation bias voltage, it presents results of two simulations: the first one using the transmission lines models and the second one using HFSS. In terms of output power both simulation results show similar values (less than 1 dBm difference) however concerning the oscillation frequency there is a 8 GHz difference (around 3%): for a 0.7 bias voltage the HFSS results present an oscillation frequency of 282.5 GHz whereas the transmission line models oscillate at 274 GHz. This difference comes from the lack of accurate modeling of unexpected dummies on the transmission lines used in the recombination point (cross) of the oscillator core.

Figure III-38, presents the final implementation of this oscillator: The chip size is 426 µm x 682 µm including RF/DC pads and matching networks. The size of the oscillator core is 141 µm x 142 µm.

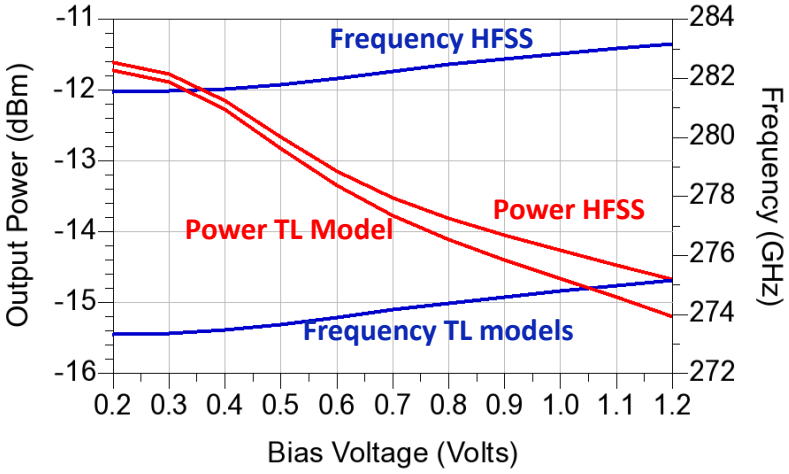


Figure III - 37 : Final power and frequency results using different modeling methods.

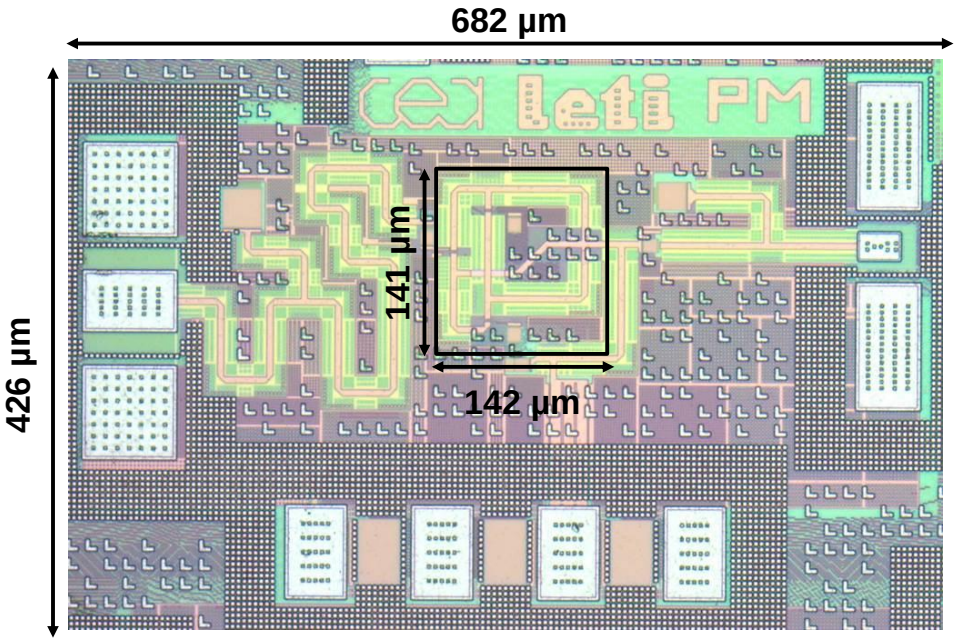


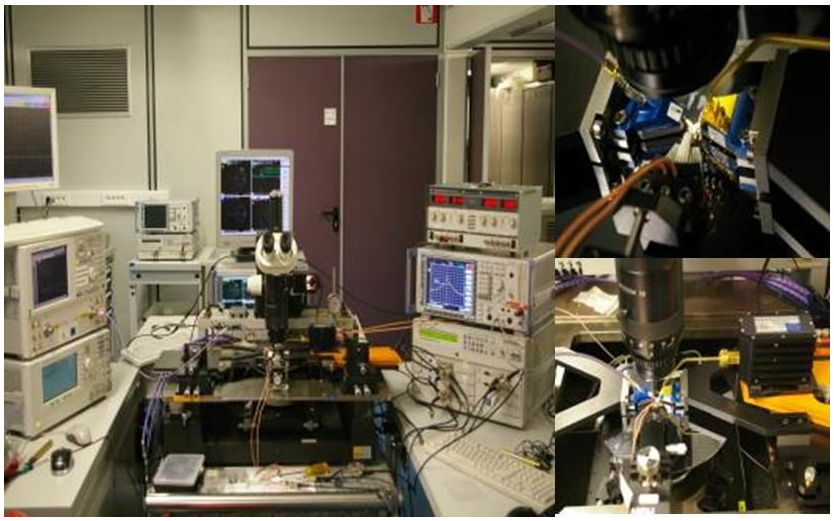
Figure III - 38 : Micrograph of the 276 GHz Sub-harmonic injection locked oscillator

III.4.3 Measurements

The test setups used in this sub-section are the same as in III.3.3. Figure III-39 shows pictures of the measurement test setup. (a) Overall oscillator test bench and (b) probes on the chip.

III.4.3.1 Test setup 1: Spectrum analysis

Again, the spectrum analyzer FSU67 was used with a 220-325 GHz extension from RPG. This setup was used to perform oscillation frequency, locking range and phase noise measurements. In Figure III-40, the third harmonic output frequency is presented versus the bias voltage (injection bias); the DC power consumption is presented as well.



(a) (b)

Figure III - 39 : (a) Oscillator test bench and (b) probes on the chip.

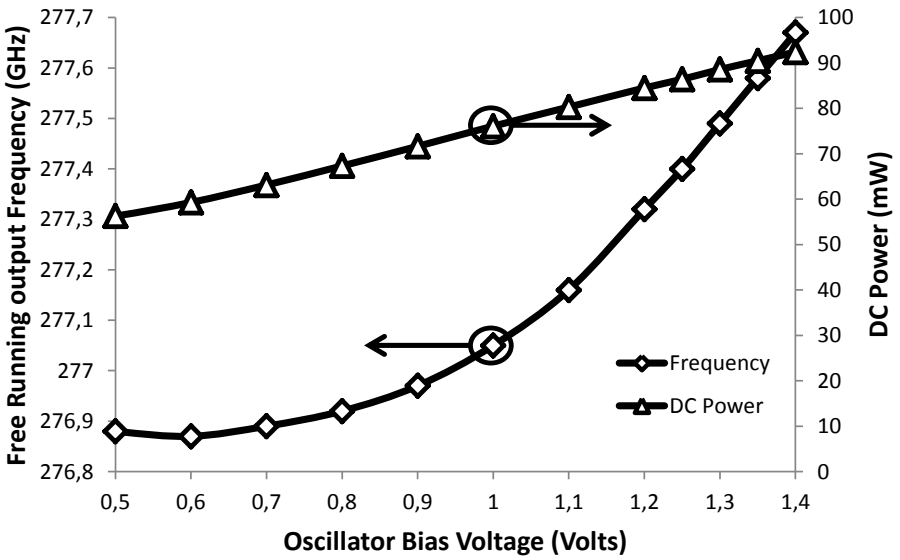


Figure III - 40 : Measured free running oscillation frequency and DC power consumption versus bias voltage for a VDD of 1.2 V.

The tuning range mechanism in this architecture is the injection transistors bias voltage. Again, the internal capacitances of these transistors change when this voltage is modified.

For the locking range measurements, an AGILENT PSG analog signal generator was used as injection source. Figure III-41 shows the measured sub-harmonic injection locking sensitivity.

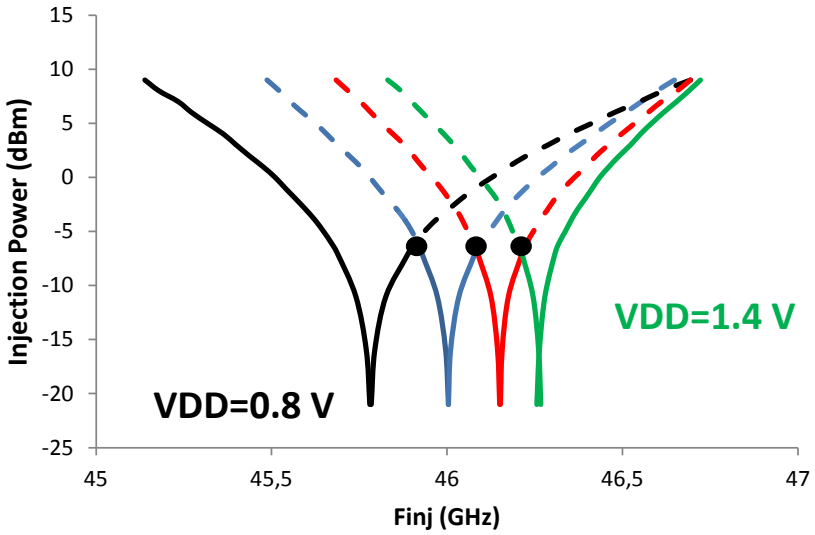


Figure III - 41 : Sub-Harmonic injection locking sensitivity.

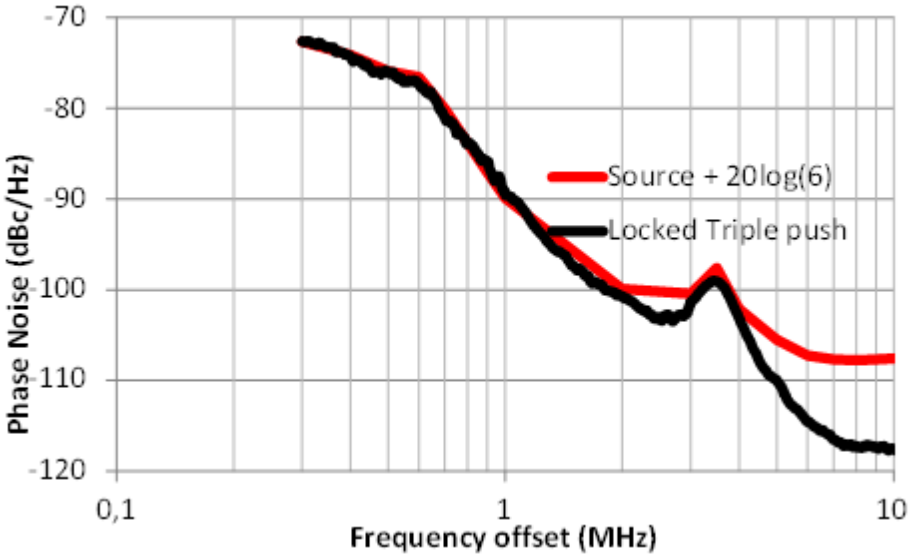


Figure III - 42 : Phase noise of the injection source and the locked oscillator.

Clearly this oscillator needs at least –7 dBm of injection power to overlap the Arnold's tongues which is around 13 dBm less than the first measured oscillator in paragraph III.3.3.1. The locking range covers from 274.1 GHz to 277.8 GHz for -7 dBm of injection power. This range can increase if more power is injected.

The Agilent synthesizer having better phase noise performance than the source of the FSU67 Rohde & Schwarz spectrum analyzer, had to be replaced with a noisier injection source: a

VNA source in this case. Having an injection source cleaner than the spectrum analyzer source can compromise any phase noise measurement.

In paragraph III.3.3.1 the free running oscillator phase noise was measured while the oscillator was locked, this is because the locking range of that oscillator was narrow. In this case, as it can be observed in Figure III-41, the locking range is wider and the measured phase noise corresponds to the one presented by the injection source to which is added $20\log_{10}(6)$. The results are presented in Figure III-42.

The implemented sub-harmonic injection locking system is fully functional and it can be used with a significantly cleaner injection source in order to tremendously decrease the phase noise.

III.4.3.2 Test setup 2: Power measurements

This test setup is exactly the same as the one in III.3.3.2. In order to cancel the impact of the second harmonic on the overall third harmonic output power a filter was added as well.

In Figure III-43, the measured output power of the third harmonic versus the VDD voltage is presented, the spectrum analyzer results are shown as well.

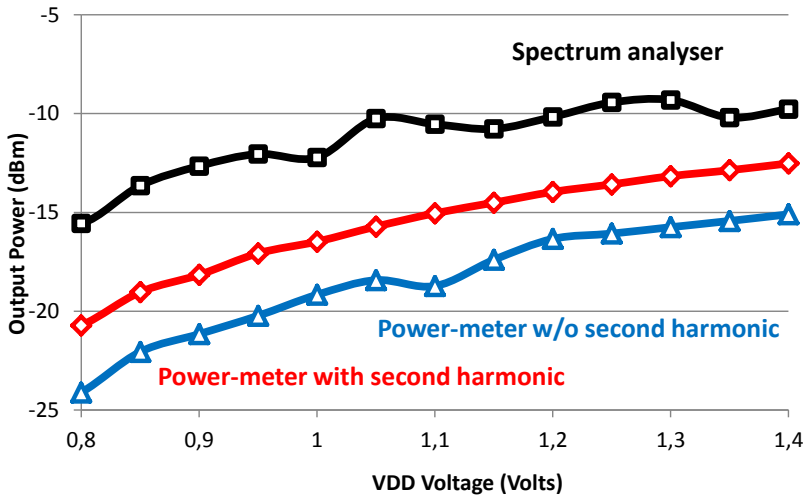


Figure III - 43 : Output power of the triple push oscillator measured with a powermeter and a spectrum analyzer.

III.5 Comparison and Conclusion

Evidently, the second oscillator offers overall better performance if compared with the first one. This difference comes from the fact that the triple push oscillator is a natural third harmonic oscillator and the modified push-push was forced to extract a third harmonic. The

differences between both oscillators are shown in table III-6 where they are also compared with the state of the art of CMOS Sub-THz oscillators. The oscillators developed here present a very low DC power consumption. This is very important because of the fact that each oscillator is going to be implemented in a heterodyne receiver that will behave as a detector in a Sub-THz imaging system. Whereas the imaging system uses a raster scanning or an array, the detector(s) must consume low power.

In terms of output power, the fact that the developed oscillators are sub-harmonically locked adds another transistor to the oscillator core deteriorating this way the overall output power.

Ref	Process	Frequency	Power	DC Power	Tuning	Locking	Phase Noise @ 1MHz
[10] 2011	65 nm CMOS	482 GHz	-7,9 dBm	61mW	No	No	-76dBc/Hz
[26]2012	65 nm CMOS	288 GHz	-1,5dBm	275mW	No	No	-87dBc/Hz
[25]2012	65 nm CMOS	290 GHz	-1,2dBm	325mW	13GHz	No	-78dBc/Hz
INTI (Push-Push & mix)	65nm CMOS	285 GHz	-21dBm	70mW	4.8 GHz	Yes, narrow locking range	-82dBc/Hz
PM (Triple-push)	65nm CMOS	276 GHz	-15dBm	40mW	5 GHz	Yes, wide locking range	Depends on source

Table III - 6 : Comparison of the developed oscillators and the CMOS state of the art

To conclude, both developed oscillators offer state of the art performances. All the passive components as well as most of the general connections were designed relying mostly on electromagnetic simulations in order to avoid unexpected capacitive or inductive behavior; the parasitic extraction techniques developed in chapter 2 were also applied.

The result of all this work is two state of the art oscillators, each one of them is going to be used as local oscillators in two heterodyne receivers. They are also the only locked oscillators around 300 GHz in CMOS.

III.6 References

[1] P. Kinget, M. Hill, W. Sansen, J. Huijsing, and R. Plassche, “Integrated GHz Voltage Controlled Oscillator,” in *Analog Circuit Design*, Springer, 1999, pp. 353–381.

[2] B. Razavi, *RF Microelectronics*, 2nd ed. New York: Prentice Hall, 2012.

[3] K. Kurokawa, “Injection locking of microwave solid-state oscillators,” *Proc. IEEE*, vol. 61, no. 10, pp. 1386–1410, 1973.

[4] K. Kurokawa, “SOME BASIC CHARACTERISTICS OF BROADBAND NEGATIVE RESISTANCE OSCILLATOR CIRCUITS,” *BELL Syst. Tech. J.*, vol. 48, no. 6, p. 1937–+, 1969.

[5] E. De Foucauld, “Conception et réalisation d’oscillateurs accordables en fréquence en technologie SiGe pour les radio-téléphones.,” UNIVERSITE DE LIMOGES, 2001.

[6] N. Seller, “Contribution à l’Étude, au Développement et à la Réalisation d'Oscillateurs à Contrôle Numérique en Technologie Silicium Avancée,” Université de Bordeaux I, 2008.

[7] J. Lee, “Voltage-Controlled Oscillators and Frequency Dividers,” in *mm-W Silicon Technology*, A. M. Niknejad and H. Hashemi, Eds. Boston, MA: Springer, 2008, pp. 159–200.

[8] C. Cao, E. Seok, and K. K. O, “192 GHz push-push VCO in 0.13 mu;m CMOS,” *Electron. Lett.*, vol. 42, no. 4, pp. 208–210, 2006.

[9] P.-C. Huang, R.-C. Liu, H. Chang, C. Lin, M. Lei, H. Wang, C.-Y. Su, C.-L. Chang, and A. G. P. Vco, “A 131 GHz push-push VCO in 90-nm CMOS technology,” in *Radio Frequency integrated Circuits (RFIC) Symposium, 2005. Digest of Papers. 2005 IEEE* , 2005, pp. 613–616.

[10] O. Momeni and E. Afshari, “High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach,” *Solid-State Circuits, IEEE J.*, vol. 46, no. 3, pp. 583–597, 2011.

[11] D. Huang, T. R. LaRocca, L. Samoska, A. Fung, and M.-C. F. Chang, “Terahertz CMOS Frequency Generator Using Linear Superposition Technique,” *Solid-State Circuits, IEEE J.*, vol. 43, no. 12, pp. 2730 –2738, 2008.

[12] M.-C. F. Daquan Huang and LaRocca, T.R. and Samoska, L. and Fung, A. and Chang, “324GHz CMOS Frequency Generator Using Linear Superposition Technique,” *Solid-State Circuits Conf. 2008. ISSCC 2008. Dig. Tech. Pap. IEEE Int.*, pp. 476–629, 2008.

[13] T. Djurhuus and V. Krozer, “Theory of Injection-Locked Oscillator Phase Noise,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 58, no. 2, pp. 312–325, Feb. 2011.

[14] P. Maffezzoni and D. D’Amore, “Phase-Noise Reduction in Oscillators via Small-Signal Injection,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 58, no. 10, pp. 2498–2507, Oct. 2011.

[15] B. R. D. Huntoon and A. Weiss, “Synchronization of oscillators,” 1947. [Online]. Available: http://archive.org/details/jresv38n4p397. [Accessed: 25-Jul-2013].

[16] HongMo Wang, H. Wang, B. Labs, and M. Hill, “A 50 GHz VCO in 0.25 μm CMOS,” in *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*, 2001, vol. 5, pp. 372–373.

[17] R. Wanner, R. Lachner, and G. R. Olbrich, “A monolithically integrated 190-GHz SiGe push-push oscillator,” *Microw. Wirel. Components Lett. IEEE*, vol. 15, no. 12, pp. 862–864, 2005.

[18] C. Cao and K. K. O, “Millimeter-wave voltage-controlled oscillators in 0.13- mu;m CMOS technology,” *Solid-State Circuits, IEEE J.*, vol. 41, no. 6, pp. 1297–1304, 2006.

[19] V. Radisic, X. B. Mei, W. R. Deal, W. Yoshida, P. H. Liu, J. Uyeda, M. Barsky, L. Samoska, A. Fung, T. Gaier, and R. Lai, “Demonstration of Sub-Millimeter Wave Fundamental Oscillators Using 35-nm InP HEMT Technology,” *Microw. Wirel. Components Lett. IEEE*, vol. 17, no. 3, pp. 223–225, 2007.

[20] P.-C. Huang, M.-D. Tsai, G. D. Vendelin, H. Wang, C.-H. Chen, and C.-S. Chang, “A Low-Power 114-GHz Push ndash;Push CMOS VCO Using LC Source Degeneration,” *Solid-State Circuits, IEEE J.*, vol. 42, no. 6, pp. 1230–1239, 2007.

[21] S. T. Nicolson, K. H. K. Yau, P. Chevalier, A. Chantre, B. Sautreuil, K. W. Tang, and S. P. Voinigescu, “Design and Scaling of W-Band SiGe BiCMOS VCOs,” *Solid-State Circuits, IEEE J.*, vol. 42, no. 9, pp. 1821–1833, 2007.

[22] B. Heydari, M. Bohsali, E. Adabi, A. M. Niknejad, and S. Member, “Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS,” *Solid-State Circuits, IEEE J.*, vol. 42, no. 12, pp. 2893–2903, 2007.

[23] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C.-M. Hung, K. K. O, and C. P. Antenna, “A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna,” in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International* , 2008, pp. 472–629.

[24] B. Razavi, “A Millimeter-Wave Circuit Technique,” *Solid-State Circuits, IEEE J.*, vol. 43, no. 9, pp. 2090–2098, 2008.

[25] Y. M. Tousi, O. Momeni, and E. Afshari, “A 283-to-296GHz VCO with 0.76mW peak output power in 65nm CMOS,” in *2012 IEEE International Solid-State Circuits Conference*, 2012, vol. 59, no. 10, pp. 258–260.

[26] Y. Zhao, J. Grzyb, and U. R. Pfeiffer, “A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology,” in *2012 Proceedings of the ESSCIRC (ESSCIRC)*, 2012, pp. 289–292.

[27] W. Steyaert and P. Reynaert, “A 0.54 THz signal generator in 40 nm bulk CMOS with 22 GHz tuning range,” in *2013 Proceedings of the ESSCIRC (ESSCIRC)*, 2013, pp. 411–414.

[28] K. F. Tsang and C. M. Yuen, “Phase noise measurement of free-running microwave oscillators at 5.8 GHz using 1/3-subharmonic injection locking,” *IEEE Microw. Wirel. Components Lett.*, vol. 15, no. 4, pp. 217–219, Apr. 2005.

[29] B. Catli and M. M. Hella, “A 30-GHz triple-push oscillator on silicon for mm-wave applications,” in *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on* , 2009, pp. 2037–2040.

Chapter IV: Developed heterodyne receivers

The main architecture of the heterodyne receivers is presented in chapter II (II.3). In this chapter, all the designed building blocks of this architecture are presented in detail for the two versions of the receiver with the exception of the oscillators that were presented in chapter III.

This chapter starts with an introduction; in this section a brief state of the art of silicon based heterodyne receivers is presented followed by a discussion about the implications of using injection locked oscillators in this work. Finally the critical points of this receiver architecture are reminded.

The 283 GHz and the 277 GHz receivers are presented in section two and three, respectively. The operating principle of the resistive mixer (passive) is presented as well as the design of the mixer and IF amplifier. Finally the test setup and measurements are shown.

In the fourth section both receivers performances are compared with the state of the art of CMOS and BiCMOS receivers around 300 GHz. The main differences and advantages are highlighted.

Finally, the 277 GHz receiver is tested with an integrated antenna in order to perform free space measurements for THz imaging. The first images using a CMOS heterodyne detector are presented.

IV.1 Introduction

The first silicon based THz heterodyne receiver was presented in [1] [2] [3] in 2009. This receiver used an external illuminated local oscillator signal which was radiated simultaneously with the RF signal. In terms of THz imaging, the superiority of the SNR0 of the heterodyne detection was demonstrated thanks to this particular receiver.

Since then, many other silicon based receivers have been presented. In [4] (2010) and in [5] (2011) two SiGe BiCMOS heterodyne receivers were presented using external oscillators and multiplier chains. But the first BiCMOS THz heterodyne receiver with integrated oscillator was presented in [6] in 2011 and in [7] the first CMOS heterodyne receiver with integrated oscillator.

The last two receivers did not have any locking system which means that the phase noise from the oscillator was present in the intermediate frequency signal: the main difference

between this work and the previously presented ones is the fact that both of the used oscillators are sub-harmonically locked using a lower frequency injection signal.

Both receivers share the same architecture (Figure II-17). The main inconvenient of a CMOS based heterodyne receiver at Sub-THz frequencies is the lack of low noise amplifier at the beginning of the Rx chain; this leads to the need of an oscillator capable of providing enough power to reduce the passive mixer conversion loss and thus the overall NF.

Even if the general architecture is the same, the architecture of each building block is defined according to the used oscillator structure. Since the first oscillator has a differential output, most of the building blocks of the 283 GHz receiver are differential. For the 277 GHz receiver, the oscillator is single ended and thus most of the building blocks are also single ended.

IV.2 283 GHz heterodyne receiver (TIW)

This receiver uses the push-push and mixer architecture (developed in chapter III (III.3)) as local oscillator. The differential nature of its signals enabled the use of a differential mixer and intermediate frequency amplifier in the receiver chain.

IV.2.1 Mixer

At lower frequencies passive mixers are mostly used because of their high linearity [8], low conversion loss and absence of power consumption. Nevertheless, at sub-THz frequencies, this kind of mixers is used to multiply signals far beyond the active CMOS frequency limitations (f_t/f_{max}) allowing the THz design on low cut-off frequencies CMOS processes. The high linearity advantage is kept but the conversion loss increases with frequency [9]. Also self-mixing beyond cut-off frequency was demonstrated many times before [10] [11]. The RF and LO signals are around 283 GHz and the IF signal is defined according to the IF amplifier (from 40 MHz to 2 GHz).

IV.2.1.1 Resistive mixing principle

This sub-section is based on the quasi static analysis performed in [2]. Figure IV-1 (a) presents the cold fet resistive mixer configuration. Since V_{ds} is definitely lower than $V_{ds\text{-}sat}$ the expression of the current of this transistor is:

$$i_{ds}(t) = \frac{W}{L}\mu C_{ox}(V_{LO} * V_{RF} - V_{th} * V_{RF} - \frac{{V_{RF}}^2}{2}) \qquad (1)$$

The V_{LO} and V_{RF} terms correspond to V_{gs} and V_{ds}, respectively. The term of cross-modulation (mixing) is the first one and is represented as $F_{LO}\pm F_{RF}$ in Figure IV-1 (b), the second and third term are presented as well as the self-mixing product of the local oscillator signal ($2*F_{LO}$).

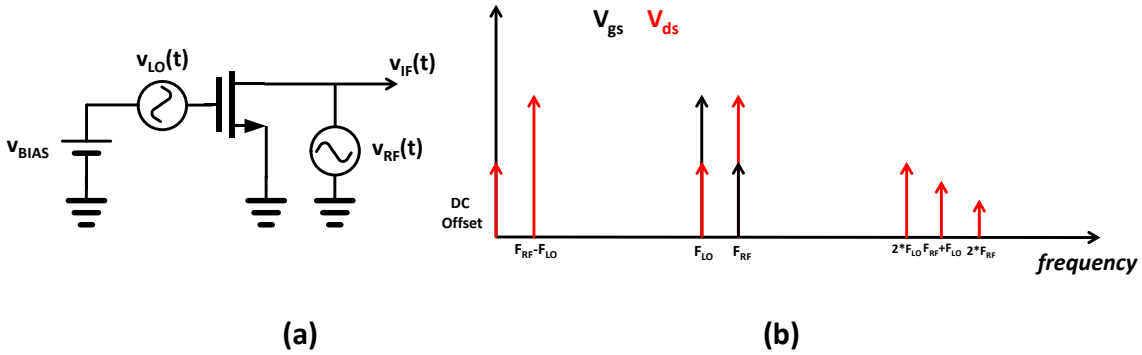


Figure IV - 1 : (a) Cold fet resistive mixer configuration. (b) Spectrum of the signals of the passive mixer: in red V_{ds} signals and in black V_{gs} signals.

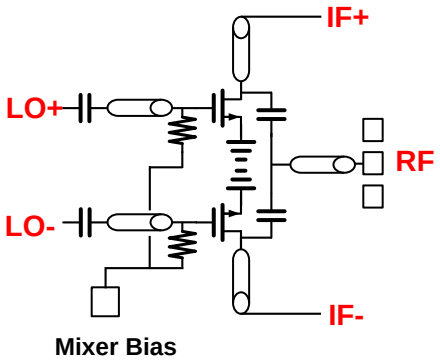


Figure IV - 2 : passive mixer with a differential LO input, a single ended RF input and a differential IF output.

Since the resistive mixer operates beyond f_t/f_{max}, a non quasi static analysis is needed; however such operation results in the numerical resolution of a differential equation which is more accurate but less intuitive for the understanding of the resistive passive mixing. Nevertheless such analysis was performed in [2] demonstrating cross-modulation between the LO and RF signal in this configuration, as predicted by the classic quasi static analysis.

IV.2.1.2 Design

The choice of the passive mixer architecture was made accordingly with the overall receiver architecture presented in Figure II-17: the RF signal is single ended and the LO is differential. The chosen architecture can be found in [12] and it was originally developed for V band down and up conversion. The circuit is presented in Figure IV-2. Simulation results show 24 dB LO/IF isolation and 30 dB LO/RF isolation. For better high frequency accuracy the NQS

option implemented in the BSIM3 transistor model was used. The simulated conversion gain is presented in Figure IV-3.

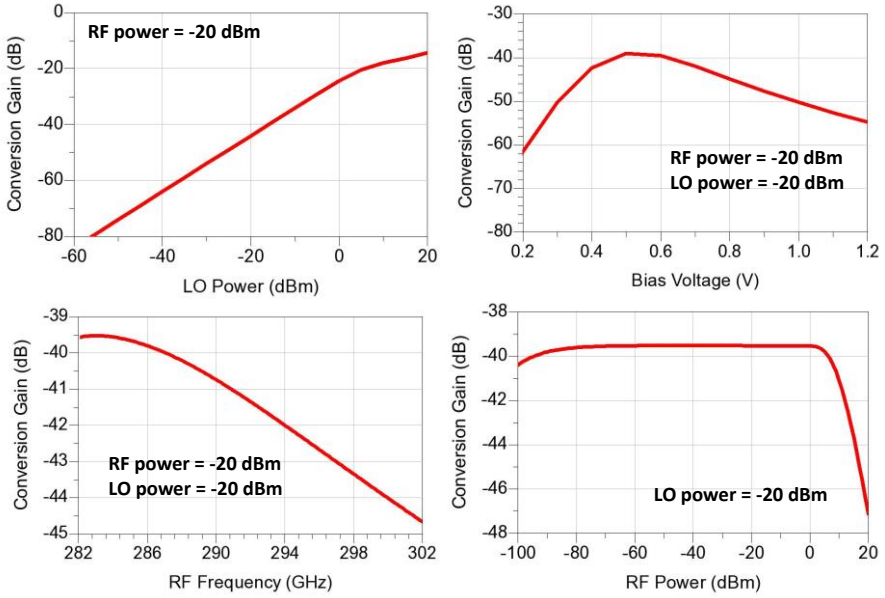


Figure IV - 3 : Passive mixer conversion gain (loss) vs LO Power, Bias voltage, RF Frequency and RF Power.

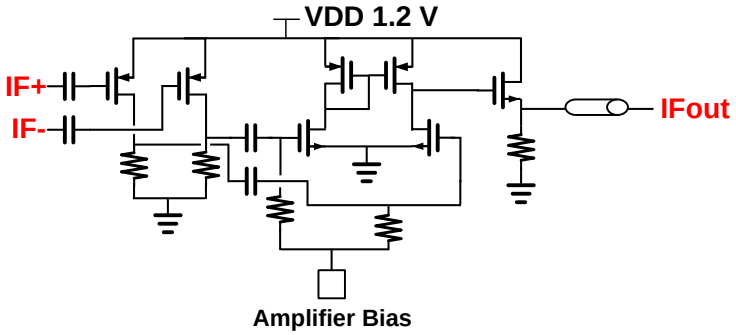


Figure IV - 4 : Schematic of the three stages intermediate frequency amplifier.

The expected conversion loss of this mixer is around 38 dB according to the used RF frequency, bias voltage, LO Power (around -20 dBm) and RF Power (-20 dBm).

IV.2.2 IF Amplifier

The goal of this amplifier is to increase the IF signal output level for testing purposes. It presents three stages: the first one is a common source pMOS differential broadband stage, the second one is a differential to single ended common source nMOS high gain stage and the third one is a single ended source follower for 50 Ω matching. The amplifier is designed to operate from 40 MHz to 2 GHz. Figure IV-4 presents the transistor level schematic of this amplifier. The power gain is presented in Figure IV-5. The maximum power gain is 27 dB and the DC power consumption is around 12 mW.

IV.2.3 Oscillator

The oscillator used in this receiver was presented in chapter III (III.3). Figure IV-6 reminds the operating principle as well as the architecture.

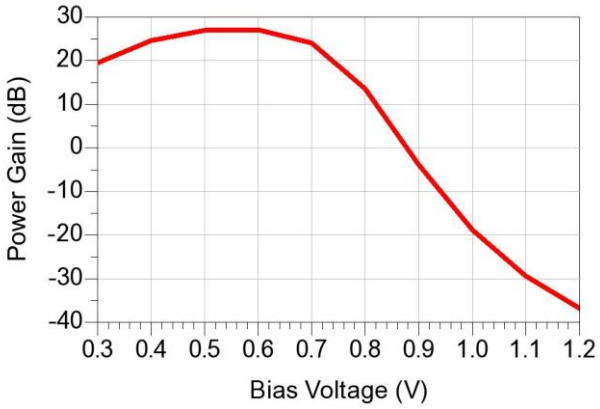
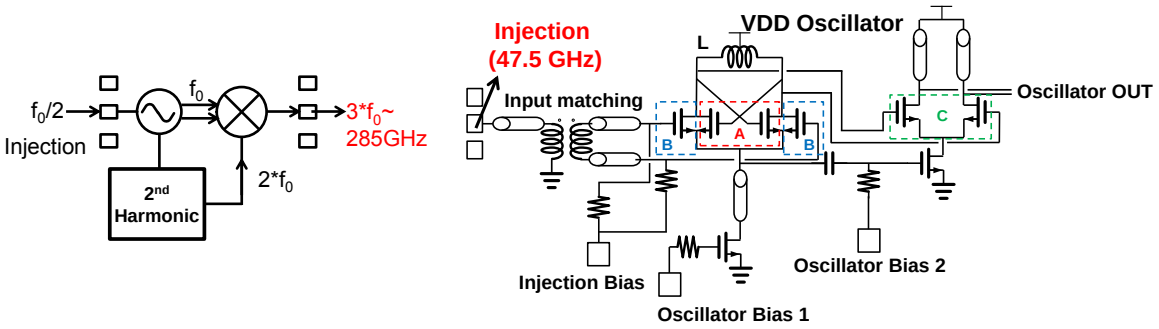


Figure IV - 5 : Schematic of the three stage intermediate frequency amplifier.



(a) **(b)**

Figure IV - 6 : (a) Operating principle of the sub-harmonic injection locked oscillator. (b) Transistor level schematic of the oscillator.

This circuit exploits the operating principle of the push-push architecture (second harmonic generation) then it extracts the third harmonic using an active mixer that multiplies the fundamental and the second harmonic. The system is locked sub-harmonically with a 47 GHz signal (around one sixth of the output frequency). The stand alone version of this oscillator presented a maximum output power of -21 dBm for a DC power consumption of 80 mW.

IV.2.4 Entire receiver

Figure IV-7 presents the entire receiver schematic: The injection input is on the left side (one sixth of the oscillator output frequency) as well as the IF output. The RF input (283 GHz) can be found on the right side. Simulation results of the entire receiver are presented in Figure IV-8.

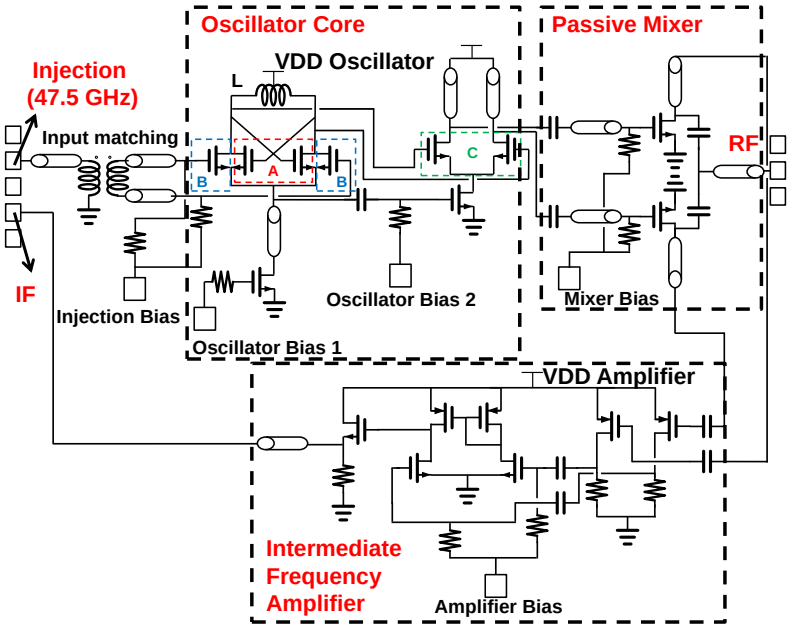
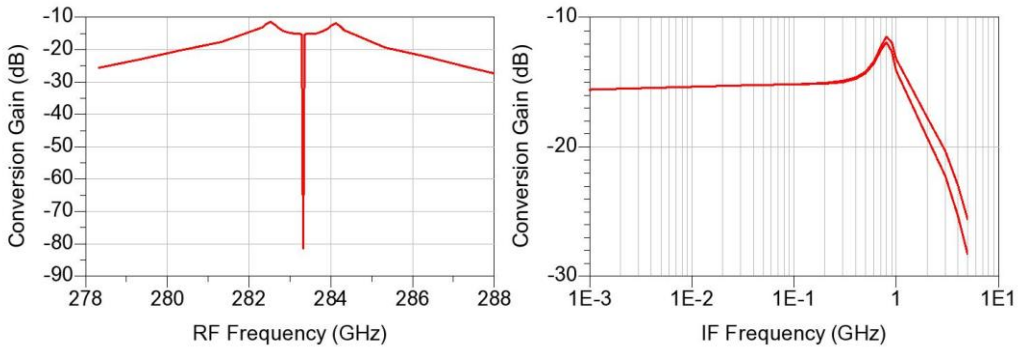


Figure IV - 7 : Entire schematic of the 283 GHz heterodyne receiver.



(a) **(b)**

Figure IV - 8 : (a) Receiver conversion gain vs RF frequency. (b) Receiver conversion gain vs IF frequency.

The maximum simulated conversion gain is around -11 dB. The overall DC power consumption is less than 100 mW.

IV.2.5 Test setup and results

Figure IV-9 presents the test setup used to characterize this receiver. The injection source was an AGILENT PSG synthesizer at around 47 GHz, the IF signal (frequency and power) was analyzed using a Rohde & Schwarz FSU67 spectrum analyzer and the RF signal was generated with a Rohde & Schwarz vector network analyzer in CW mode with a 220 to 325 GHz extension.

Figure IV-10 (a) presents a micrograph of the entire receiver chip. The size is 820 µm x 780 µm including DC/RF pads and matching networks. Figure IV-10 (b) shows a snapshot of the IF spectrum taken from R&S spectrum analyzer at 500 MHz for a RF signal at 282.3 GHz and a LO at 281.2 GHz.

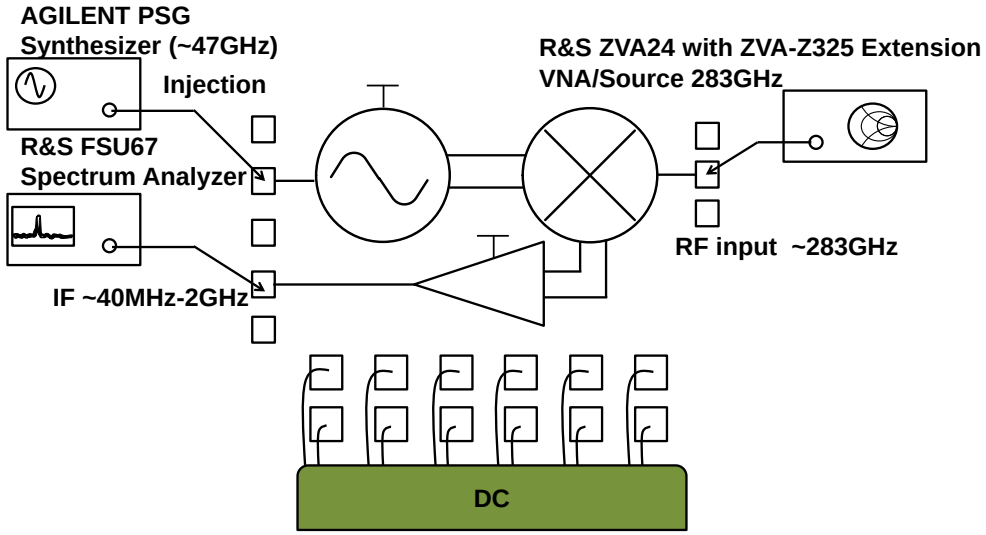


Figure IV - 9 : 283 GHz receiver test setup.

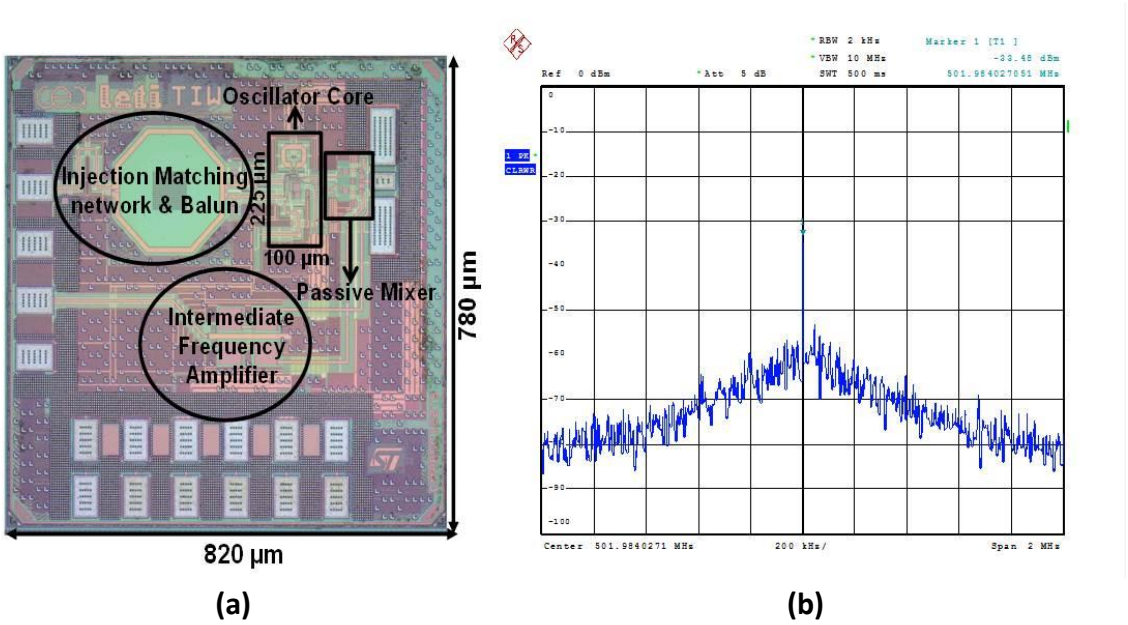


Figure IV - 10 : (a) Micrograph of the 283 GHz receiver. (b) 500 MHz IF signal with a 2 MHz span.

Figure IV-11 presents the measured conversion gain of this receiver vs the RF (a) and the IF (b) frequencies, the receiver achieved a maximum conversion gain of -6 dB and a 3 dB IF bandwidth of 1.5 GHz, as predicted in simulation. High symmetry is achieved between lower and upper side bands.

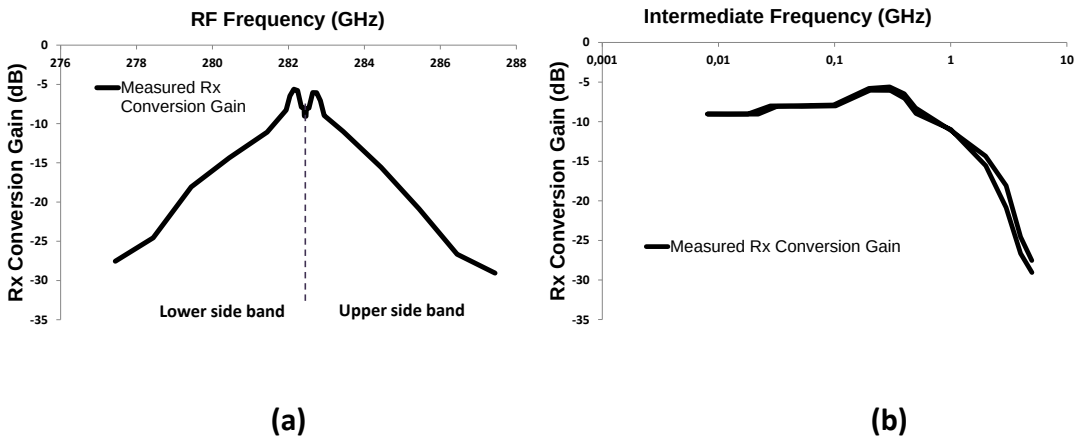


Figure IV - 11 : (a) Receiver conversion gain vs RF frequency signal. (b) Receiver conversion gain vs IF frequency. The LO frequency of both graphics is 282.5 GHz.

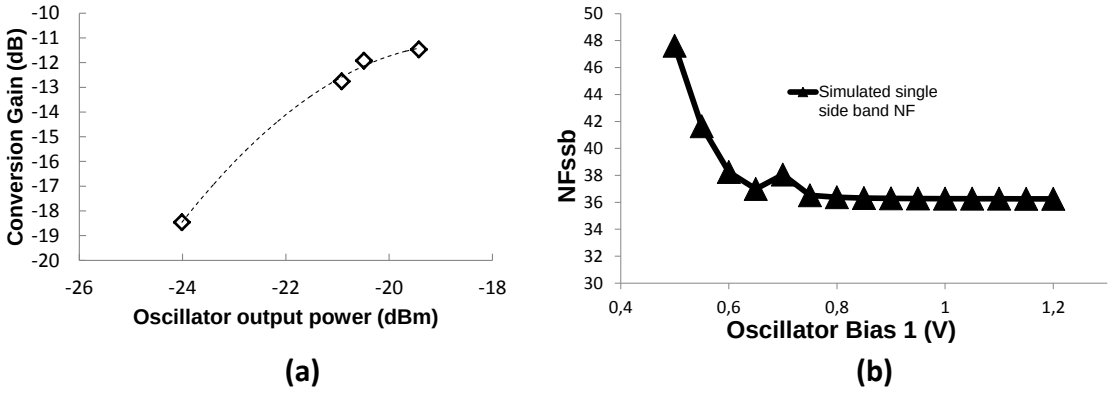


Figure IV - 12 : (a) Measured correlation between LO power and conversion gain. (b) Simulated receiver NF.

The fact that the local oscillator needs to provide enough power to reduce the passive mixer conversion loss and the overall receiver NF was mentioned before in chapter I and II. Figure IV-12 (a) presents the measurement of the direct correlation between LO power and receiver conversion loss (which is directly related to the NF). The noise figure (NF) could not be measured since a noise source was not available at 282 GHz; however simulation results showed an overall NF of 36 dB, this simulation is presented in Figure IV-12 (b). The high value of the NF can be explained by the Friis formula:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1} G_n} \qquad (2)$$

In this case the total noise factor F_{tot} (in linear) only depends on the first two terms of this equation since there are only two blocks in the receiver chain (mixer and IF amplifier). The mixer being a passive component has a negative gain ($0<G_1<1$ in linear) and its noise factor

corresponds to the losses. Considering the absence of LNA at the beginning of the receiver chain, it's not surprising to have a high NF.

Table IV-1 summarizes the overall performance of this receiver:

Process	Frequency	Conversion Gain	DC Power	NF ssb	Locking	Integration level
65 nm CMOS	283 GHz	-6 dB	97.6 mW	36 dB	Yes	Mixer, LO and IF Amp.

Table IV - 1 : Performance summary of the 283 GHz CMOS receiver.

IV.3 277 GHz heterodyne receiver (PM)

This receiver uses the sub-harmonic injection locking oscillator presented in III.4. The oscillator architecture is called triple-push and it was introduced by [13] as a mmW/Sub-THz oscillator. The main difference between this receiver and the previous one is the single ended nature of the oscillator which enables the use of single ended mixer and IF amplifier.

IV.3.1 Mixer

The resistive mixer principle was presented in IV.2.1.1 using a quasi-static analysis; the mixer presented in this sub-section uses the same operation principle. The architecture is a single ended version of the mixer presented in [12] and in IV.2.1.2. The circuit schematic is shown in Figure IV-13.

Again, the NQS option of the transistors was activated for the design of this mixer. Simulation results show 15 dB of LO/IF isolation and 22 dB of LO/RF isolation. Since the LO power is around -13 dBm, the conversion loss of the mixer is expected to be around 33 dB (5 dB lower than the previous one). Simulation results are presented in Figure IV-14.

IV.3.2 IF Amplifier

The used IF amplifier of this receiver is also a modified singled ended version of the amplifier presented in IV.2.2. It presents three stages, the first one is a broadband pMOS common source stage, the second one is an nMOS common source high gain stage and the third one is a source follower for matching network purposes. The circuit is presented in Figure IV-15.

This amplifier was designed to present a 3 dB bandwidth from 40 MHz to 2 GHz. The DC power consumption is around 6.5mW. The amplifier power gain is presented in Figure IV-16.

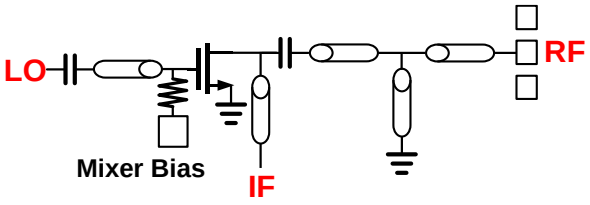


Figure IV - 13 : Single ended resistive mixer.

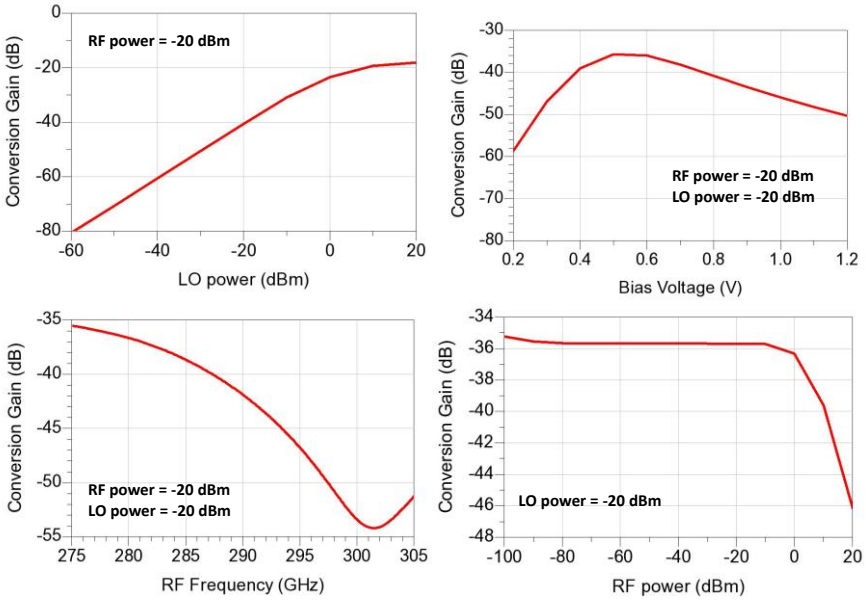


Figure IV - 14 : Passive mixer conversion gain (loss) vs LO Power, Bias voltage, RF Frequency and RF Power.

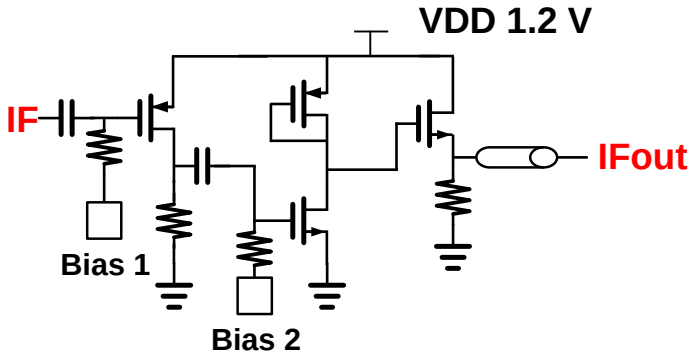


Figure IV - 15 : Single ended three stage intermediate frequency amplifier.

IV.3.3 Oscillator

Figure IV-17 (a) presents the operation principle of this architecture and Figure IV-17 (b) presents the transistor level schematic. More information about this architecture can be found in Chapter III.

This circuit is a three stage inductive ring oscillator: the third harmonic is exploited by the recombination of the three 120° phase shifted signals. The fundamental frequency is set to 92 GHz, the injection frequency to 46 GHz and the output frequency (third harmonic) to 276 GHz.

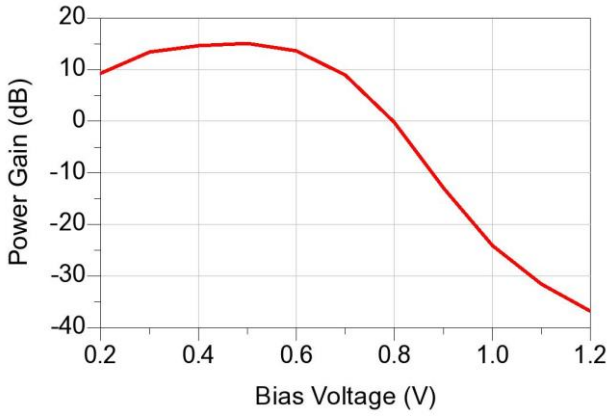


Figure IV - 16 : Amplifier power gain.

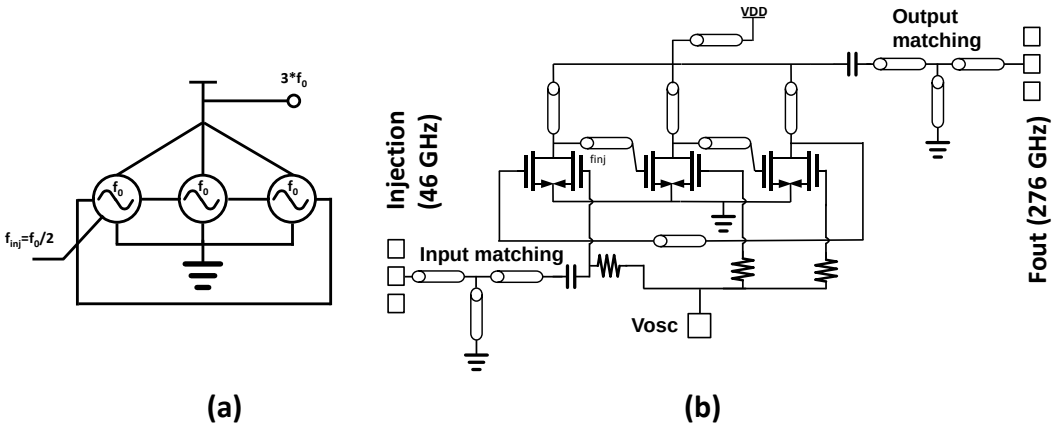


Figure IV - 17 : (a) Operating principle schematic of the 276 GHz oscillator. (b) Transistor level schematic of the oscillator.

IV.3.4 Entire receiver

Figure IV-18 presents the entire transistor level schematic of the 277 GHz heterodyne receiver.

The 46 GHz injection input as well as the IF output are located in the left part of the circuit using a differential mmW pad. The RF input is on the right side of the chip. Simulation results of the overall conversion gain are presented in Figure IV-19. Simulation results show a maximum conversion gain of -13 dB for a DC power consumption of around 50 mW.

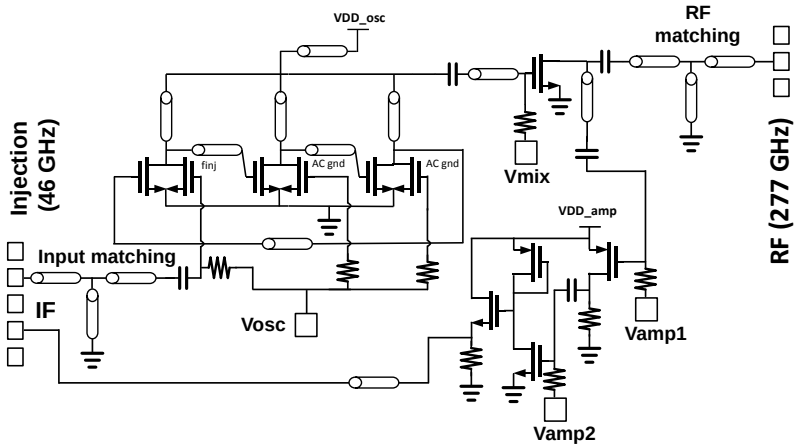
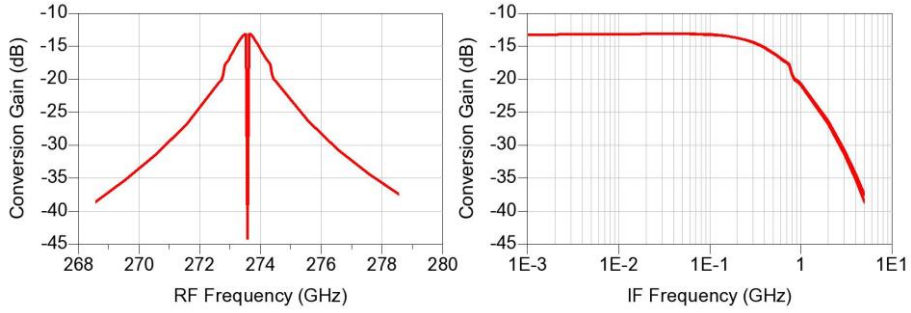


Figure IV - 18 : Single ended three stage intermediate frequency amplifier.



(a) **(b)**

Figure IV - 19 : (a) Receiver conversion gain vs RF frequency. (b) Receiver conversion gain vs IF frequency.

IV.3.5 Test setup and results

The used test setup for this receiver is exactly the same used in IV.2.5 for the previous component: a R&S FSU67 spectrum analyzer for the IF output, an AGILENT PSG analog signal generator synthesizer for the injection input and a R&S VNA with a 220-325 GHz extension for the generation of the RF signal.

Figure IV-20 (a) presents a micrograph of the 277 GHz receiver. The size is 760 µm x 830 µm including pads and matching networks. Figure IV-20 (b) shows a snapshot of the IF signal spectrum taken from the spectrum analyzer at 241 MHz for a RF signal of 277.241 GHz and a LO signal of around 277 GHz.

The conversion gain is presented in Figure IV-21 vs. the RF (a) and IF (b) frequency. Both upper and lower side bands are symmetric below 1 GHz IF frequency as predicted in simulations. The maximum conversion gain is -11 dB which is 3 dB higher than simulation results presented in Figure IV-19. However the conversion gain measurements for an IF fixed frequency (Figure IV-22) show a maximum conversion gain of -6 dB. In terms of DC

power consumption the receiver dissipates 40 mW: 34 mW from the oscillator and 6 mW from the IF amplifier.

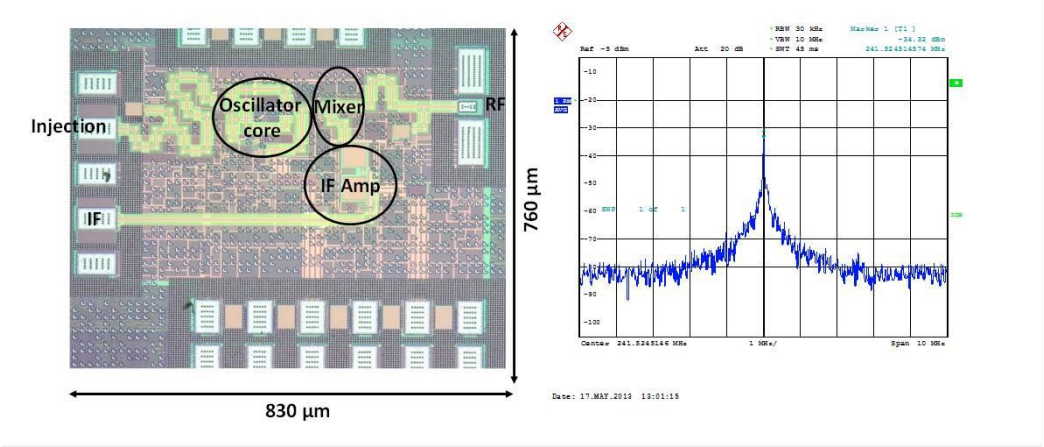


Figure IV - 20 : (a) Micrograph of the 277 GHz heterodyne receiver. (b) IF snapshot at 241 MHz for a 277.241 GHz RF and a 277 GHz LO.

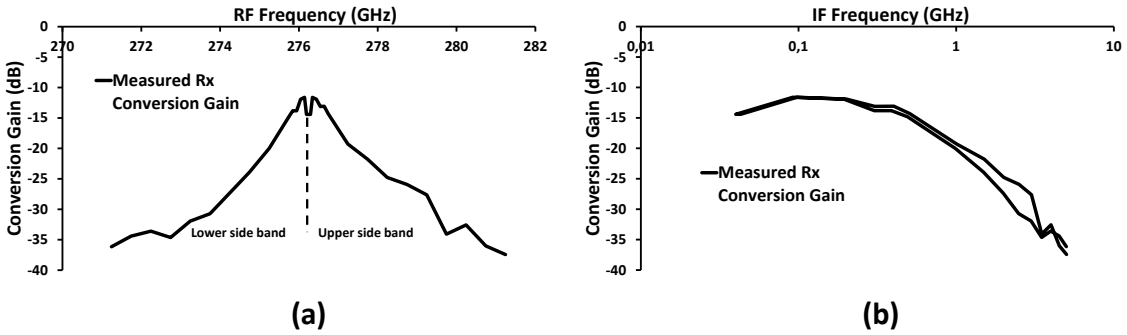


Figure IV - 21 : (a) Receiver conversion gain vs RF frequency signal. (b) Receiver conversion gain vs IF frequency. The LO frequency of both graphics is 276.2 GHz.

Figure IV-23 presents the correlation between heterodyne receiver conversion gain and local oscillator power, this demonstrates again that the higher the LO power is, the lower the conversion losses are.

The performance of this receiver is compared with the state of the art in IV.4. Table IV-2 summarizes its performance.

Process	Frequency	Conversion Gain	DC Power	NF ssb	Locking	Integration level
65 nm CMOS	277 GHz	-6 dB	40 mW	30 dB	Yes	Mixer, LO and IF Amp.

Table IV - 2 : Performance summary of the 277 GHz CMOS receiver.

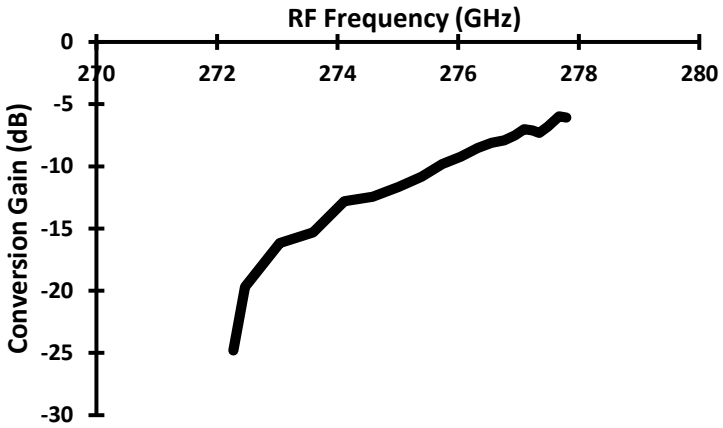


Figure IV - 22 : Conversion Gain vs. RF Frequency at 150 MHz fixed IF Frequency.

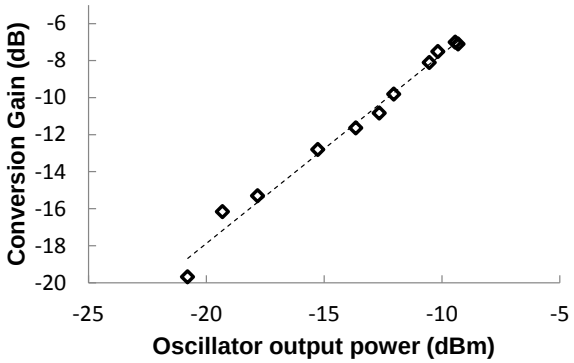


Figure IV - 23 : Measured correlation between LO power and Rx conversion gain. (b) Simulated receiver NF.

IV.4 Conclusion and state of the art comparison

This chapter provided the core of this PhD work: design, implementation and measurements of the two developed Sub-THz heterodyne receivers. This final chapter is the result of all the background presented in chapter I and chapter II as well as the sub-harmonic injection locked oscillators presented in chapter III.

First, the building blocks of each receiver were introduced: the operating principle and design of the passive mixers was presented, the schematics and simulation results of the intermediate frequency amplifiers were provided and the architecture of each oscillator was reminded.

Following the building blocks, the entire receiver was presented; simulation results in this sub-section give a preview of the overall performance in terms of DC power and conversion gain before the tests.

Finally, the test setup and the measurement results were presented: Table IV-3 summarizes the performance of both receivers and compares them with the state of the art of silicon based sub-THz heterodyne receivers:

Ref	Process	Frequency	Conversion Gain	DC Power	NF ssb	Locking	Integration level	year
[14]	130 nm SiGe	245 GHz	21 dB	358 mW	33 dB	N/A	LNA, Mixer & LO.	2012
[7]	65 nm CMOS	260 GHz	17 dB (sim)	485 mW	19 dB (sim)	N/A	Mixer, LO, demodulator & IF buffer.	2012
[15]	130 nm SiGe	220 GHz	16 dB	216 mW	18 dB	N/A	LNA & Mixer.	2012
[15]	130 nm SiGe	320 GHz	-14 dB	3072 mW	36 dB	Yes, multiplier.	Mixer & LO-chain	2012
This work	**65 nm CMOS**	**285 GHz**	**-6 dB**	**97.6 mW**	**36 dB (sim)**	**Yes, Sub-harmonic.**	**Mixer, LO and IF Amp.**	**2013**
This work	**65 nm CMOS**	**277 GHz**	**-6 dB**	**40 mW**	**30 dB (sim)**	**Yes, Sub-harmonic.**	**Mixer, LO and IF Amp.**	**2013**

Table IV - 3 : Comparison of the developed receivers and the state of the art of silicon technologies Sub-THz receivers.

The main difference of the two developed receivers is the core architecture of the local oscillator. The 277 GHz receiver beneficiates of local oscillator that outperform the one used in the 285 GHz version. This oscillator provides more output power for less DC power consumption and the impact of this component on the overall performance of the receiver can be easily observed in Table IV-3, especially in terms of DC power consumption and noise figure (which is directly related to the oscillator output power).

To conclude, there are only three receivers that used locked sources as local oscillator, two with CMOS (this work) and one with SiGe BiCMOS [15]. First, in terms of DC power consumption , the receivers that we have developed dissipate less than 100 mW whereas the 320 GHz receiver from [15] consumes more than 3 W. Regarding the conversion gain, our receivers present -6 dB of conversion gain which is the highest value for receivers using locked oscillators, nevertheless receivers which are not using locked oscillator present conversion gains considerably higher.

IV.5 Receiver application: THz imaging

As an application for the 277 GHz receiver, THz imaging was performed. For that, an antenna was integrated on the PMRx chip. The imaging was performed at the IEMN facilities using a

specific THz-optical bench[1]. The antenna of the heterodyne receiver was developed by Telecom Bretagne: It uses a dipole structure that feeds the mixer 50 Ω input microstrip line. Since the previous version of the receiver was tested using probes, this version was adapted for wire-bonding connections. The chip was mounted on a PCB board. An additional matching network was designed on the board in order to compensate the mismatch introduced by the 50 Ω injection locking input.

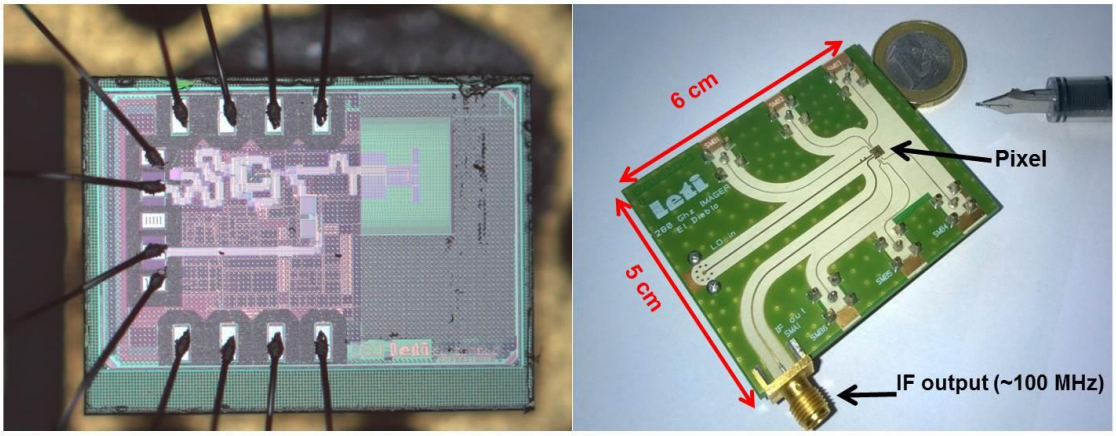


Figure IV - 24 : (a) Micrograph of the 277 GHz heterodyne receiver. (b) Photograph of the detector board with a euro coin for size comparison.

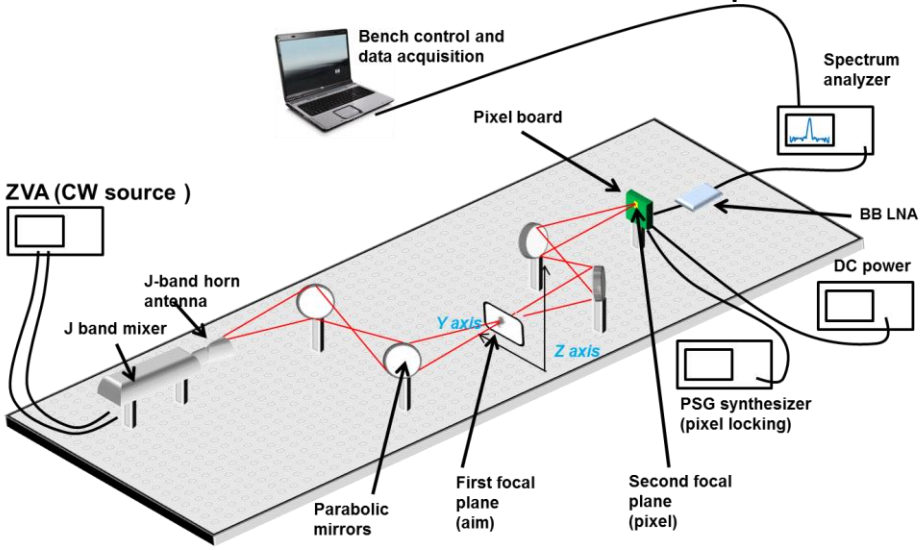


Figure IV - 25 : Schematic of the optical test setup.

Figure IV-24 (a) shows a micrograph of the 277 GHz heterodyne receiver used as image Sub-THz detector; Figure IV-24 (b) presents a photograph of the board next a euro coin for comparison purposes. The overall size of the board is 6 cm x 5 cm.

[1] Test setup and images performed by A. Siligaris and G. Ducourneau.

The optical test setup schematic is presented in Figure IV-25. The RF source is a VNA with a Sub-THz extension configured as a continuous wave source with a J band horn antenna. The external injection source is a PSG synthesizer from AGILENT and the IF output is examined using the FSU67 spectrum analyzer from R&S.

There are two focal planes in this setup: the first one is located at the target and the second one is at the pixel. The maximum signal power at the receiver antenna is around -24 dBm; this power is obtained as a result of the two focal planes aligned using parabolic mirrors. An external base band low noise amplifier is used to increase the IF output level. In order to detect an entire image, a raster scanning is performed at the first focal plane. Figure IV-26 shows a photograph of the setup.

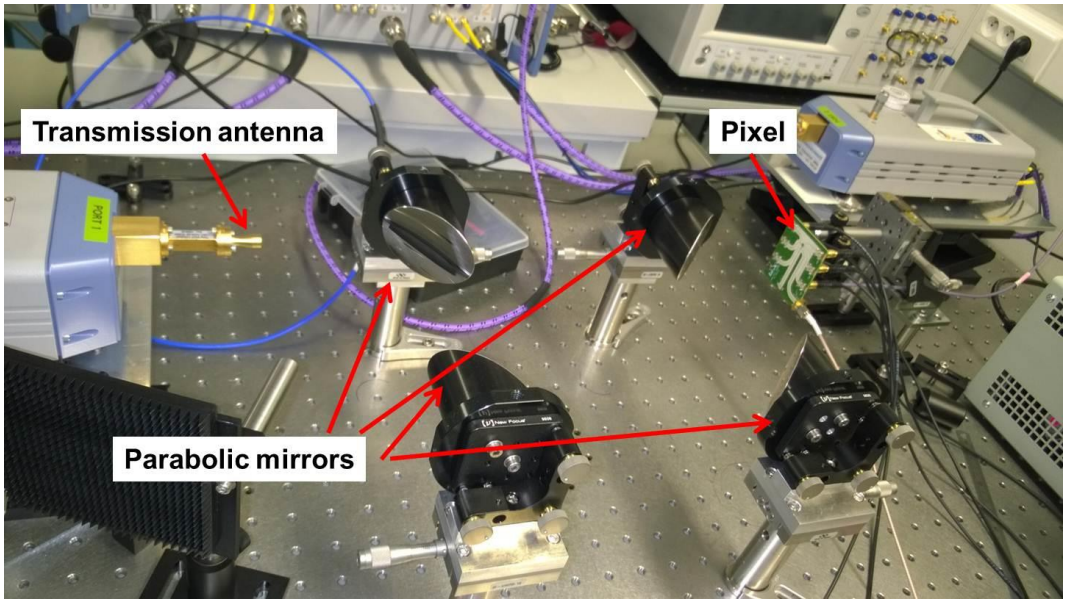
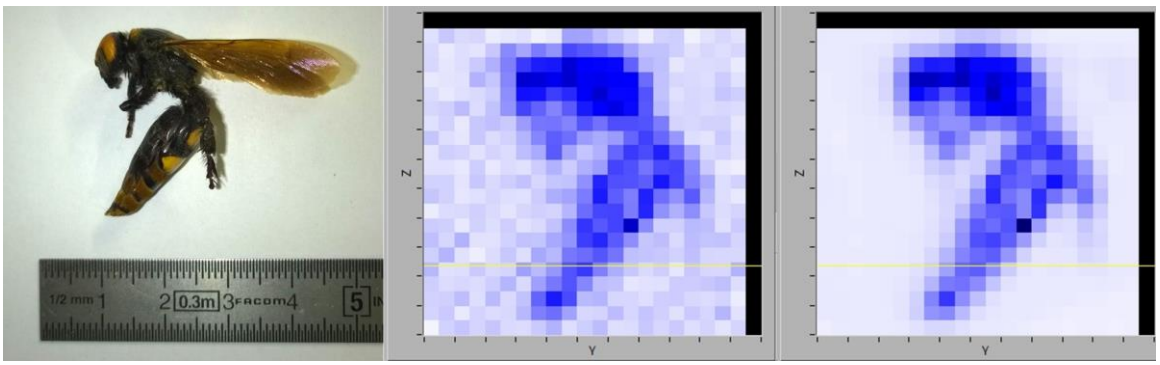


Figure IV - 26 : Photograph of the optical test setup.

The detected images were taken with the following setup specifications: the total receiver chain gain is 14 dB (-36 dB from the receiver and 50 dB from the external LNA). The detected power spans from -70 dBm (black) to -9.8 dBm (white) that corresponds to 60 dB of dynamic range for 10 KHz resolution bandwidth. The noise floor can be reduced to -110 dBm if the resolution bandwidth is downscaled to 100 Hz. Figure IV-27 presents 278 GHz images of a wasp. The first one (Figure IV-27 (b)) is done with a free running oscillator and the second one (Figure IV-27 (c)) is done with a locked oscillator. Both images were taken with a 60 dB dynamic range, a 1.5 mm spatial step and a resolution bandwidth of 10 KHz. The quality of the image with a locked oscillator is significantly higher. In order to obtain a higher quality image with an unlocked oscillator, the resolution bandwidth of the spectrum analyzer must be increased; this will significantly rise the noise floor level reducing the dynamic range of the detection.

Figure IV-28 presents the same wasp as target. This figure shows a comparison between images detected using 20 dB of dynamic range (Figure IV-28 (b)) and 60 dB of dynamic range (Figure IV -28 (c)). The contrast in Figure IV -28 (c) is tremendously higher since more shades between black and white can be detected. The spatial step in Figure IV-28 (b) and (c) was 0.75 mm.



(a) **(b)** **(c)**

Figure IV - 27 : (a) Photograph of a wasp. (b) Sub-THz image detected with a free running oscillator receiver and (c) Sub-THz image detected with a locked oscillator receiver.

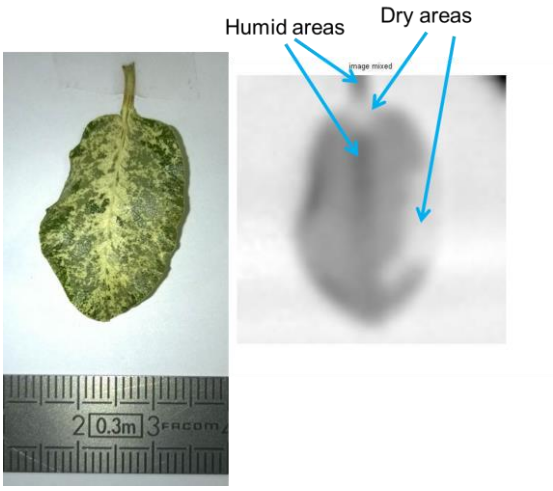
(a) **(b)** **(c)**

Figure IV - 28 : (a) Photograph of a wasp. (b) Sub-THz image detected with 20 dB of dynamic range (c) Sub-THz image detected 60 dB of dynamic range.

Figure IV-29 (b) shows a detected image whose number of pixels has been increased artificially using post processing. The original target (Figure IV-29 (a)) is a leave. Because of this modification this image is blurry, however this proceeding allows a better analysis of the results, for instance the dry and humid areas can be identified in Figure IV-29 (b).

As shown in the previous results, heterodyne receivers can be easily adapted also for THz-imaging. Moreover, a heterodyne receiver using locked oscillator increases the dynamic

range and decreases the noise floor of the receiver system. Thus it offers a much higher contrast to the image, and a high sensitivity for the imaging system.



(a) **(b)**

Figure IV - 29 : (a) Photograph of a leave. (b) Post treated sub-THz image.

IV.6 References

[1] D. Glaab, A. Lisauskas, S. Boppel, U. Pfeiffer, E. Ojefors, and H. G. Roskos, “Terahertz heterodyne detection with silicon CMOS transistors,” in *Infrared, Millimeter, and Terahertz Waves, 2009. IRMMW-THz 2009. 34th International Conference on* , 2009, pp. 1–2.

[2] U. R. Pfeiffer, E. Ojefors, A. Lisaukas, D. Glaab, and H. G. Roskos, “A CMOS focal-plane array for heterodyne terahertz imaging,” in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, 2009, pp. 433–436.

[3] D. Glaab, S. Boppel, A. Lisauskas, U. Pfeiffer, E. O uml jefors, and H. G. Roskos, “Terahertz heterodyne detection with silicon field-effect transistors,” *Appl. Phys. Lett.*, vol. 96, no. 4, p. 042106 (3 pp.), 2010.

[4] E. Ojefors, U. R. Pfeiffer, and E. Öjefors, “A 650GHz SiGe receiver front-end for terahertz imaging arrays,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* , 2010, vol. 43, no. 5, pp. 430–431.

[5] E. Ojefors, J. Grzyb, Y. Zhao, B. Heinemann, B. Tillack, and U. R. Pfeiffer, “A 820GHz SiGe chipset for terahertz active imaging applications,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International* , 2011, pp. 224–226.

[6] J.-D. Park, S. Kang, Niknejad, .M., E. Engineering, and C. Sciences, “A 0.38THz fully integrated transceiver utilizing quadrature push-push circuitry,” in *2011 Symposium on VLSI Circuits (VLSIC)*, 2011, pp. 44–45.

[7] J.-D. Park, S. Kang, S. V Thyagarajan, E. Alon, and A. M. Niknejad, “A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication,” in *2012 Symposium on VLSI Circuits (VLSIC)*, 2012, pp. 48–49.

[8] F. Ellinger, “26.5-30-GHz Resistive Mixer in 90-nm VLSI SOI CMOS Technology With High Linearity for WLAN,” *Microw. Theory Tech. IEEE Trans.*, vol. 53, no. 8, pp. 2559–2565, 2005.

[9] J. Moron Guerra, A. Siligaris, J.-F. Lampin, F. Danneville, and P. Vincent, “A 283 GHz low power heterodyne receiver with on-chip local oscillator in 65 nm CMOS process,” in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 301–304.

[10] U. R. Pfeiffer and E. Ojefors, “A 600-GHz CMOS focal-plane array for terahertz imaging applications,” in *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European* , 2008, pp. 110–113.

[11] E. Ojefors, U. R. Pfeiffer, A. Lisauskas, H. G. Roskos, E. Öjefors, and S. Member, “A 0.65 THz Focal-Plane Array in a Quarter-Micron CMOS Process Technology,” *Solid-State Circuits, IEEE J.*, vol. 44, no. 7, pp. 1968–1976, 2009.

[12] M. Varonen, M. Karkkainen, M. Kantanen, and K. Halonen, “Millimeter-Wave Integrated Circuits in 65-nm CMOS,” *Solid-State Circuits, IEEE J.*, vol. 43, no. 9, pp. 1991–2002, 2008.

[13] O. Momeni and E. Afshari, “High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach,” *Solid-State Circuits, IEEE J.*, vol. 46, no. 3, pp. 583–597, 2011.

[14] Y. Mao, K. Schmalz, J. Borngraber, J. C. Scheytt, and J. Borngräber, “245-GHz LNA, Mixer, and Subharmonic Receiver in SiGe Technology,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 12, pp. 1–11, 2012.

[15] E. Öjefors, B. Heinemann, U. R. Pfeiffer, S. Member, and E. Ojefors, “Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 5, pp. 1397–1404, May 2012.

General conclusion and perspectives

This section summarizes and reviews all the scientific achievements of this entire work. First the contribution of each chapter is presented, then all the intellectual and technical innovations are reminded. Finally, potential improvements and the perspective on future work is given.

Chapter I had two main goals: the first one was to provide a general background on the THz gap as well as its applications. The second goal was to justify the choice of the heterodyne detection method by showing previous analysis.

Once the detection method justified, chapter II aimed to explain the choice of a CMOS technology for a Sub-THz system, this was done by presenting the evolution of CMOS cut-off frequencies and specifically providing the advantages of CMOS over SiGe and III-V processes. This chapter also delivered the high frequency behavior of the used process: active and passive components were presented even the ones built in the back end of line (TFMSL and baluns). The developed parasitic extraction techniques were presented as well as the identification of the critical building blocks of a Sub-THz CMOS heterodyne receiver.

The second part of this thesis is focused on the development of the heterodyne detector: Chapter III was dedicated to one of the most critical circuits of the receiver: the oscillator. The operating principle and CMOS Sub-THz state of the art was presented as well as the design, implementation and measurements of two sub-harmonic injection locked oscillators at 285 GHz and 276 GHz respectively. Both components presented state of the art performances such as output power of -21 and -15 dBm for less than 100 mW of DC power consumption and they are the only locked oscillators on CMOS at Sub-THz frequencies.

Chapter IV started with the operating principle of the passive mixer which allowed the cross-modulation of signals beyond the active CMOS cut-off frequencies (f_t/f_{max}), then the passive mixer and the IF amplifier of both version of the receiver were presented. Overall conversion gain and NF simulations were also provided. Both receivers showed a maximum measured conversion gain of - 6 dB for less than 100 mW of DC power consumption. Also the Sub-THz images taken with the 277 GHz heterodyne receiver as a detector were presented.

The first innovation provided by this work is the introduction of EM simulations in the RF design flow: by simulating paths and interconnections between transistors, the risk of unwanted capacitive, inductive and resistive behavior is reduced. Since the impact of

parasitic components is bigger at higher frequencies, this part was a key factor to warrant successful results.

The first oscillator architecture (push-push and mix) provided an alternative to other high harmonic boost architectures by using a highly predictable and well-known core circuit (the push-push LC Tank). Even if this architecture presents many drawbacks such as high frequency limitations and first and second harmonic leakage it's still very robust for high frequency accuracy.

In order to reduce the phase noise of the oscillators, both of them were locked using an external injection source. Both developed oscillators presented fully functional sub-harmonic injection systems operating at one sixth of the output frequency (~47 GHz). The 276 GHz oscillator is the only injection locked triple push architecture at sub-THz frequencies.

Finally, since the cold fet based resistive mixer provides cross-modulation far beyond the active transistors frequency limits, the design, implementation and test of a Sub-THz CMOS heterodyne receiver was possible. I believe the THz images presented in chapter IV are the first of its kind detected using a fully integrated CMOS heterodyne receiver.

Before presenting the perspectives and future work I rather mention the potential improvements in terms of design: I think that the first and second harmonic leakage can be significantly lowered for the 285 GHz oscillator as well as the gain of both IF amplifiers if optimized properly.

The antenna version of the 277 GHz receiver was already used for Sub-THz imaging, the next step is to use this chip for data links in order to study the possibility of improvements for a second version that would be wireless communication oriented. Also implementing this receiver and oscillator architecture on an advanced SiGe process could tremendously decrease the overall NF since the oscillator could provide more power.

The list of scientific publications is presented below:

J. Moron Guerra, A. Siligaris, J.-F. Lampin, F. Danneville, and P. Vincent, "A 285 GHz sub-harmonic injection locked oscillator in 65nm CMOS technology," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2013, pp. 1–3.

J. Moron Guerra, A. Siligaris, J.-F. Lampin, F. Danneville, and P. Vincent, "A 283 GHz low power heterodyne receiver with on-chip local oscillator in 65 nm CMOS process," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 301–304.

1. Appendix chapter I

1.1. Noise equivalent power expression for CMOS based square law detectors

Figure A-1 shows the schematic of the CMOS square law detector (self-mixer):

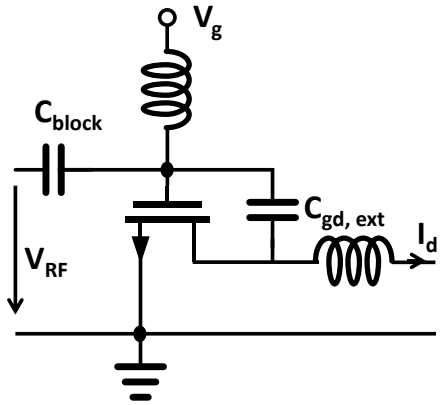


Figure A - 1 : MOSFET resistive mixer used as a RF power detector from [1]

This appendix presents the analytical calculations performed in [1] in order to obtain the NEP of a CMOS square law detector. From Figure A-1:

$$v_{gs}(t) = v_{RF}(t) + V_g \tag{1}$$

And because of the presence of the external C_{gd} capacitor:

$$v_{ds}(t) = v_{RF}(t) \tag{2}$$

Since the transistor is operating in the linear region:

$$i_{ds}(t) = v_{ds}(t) g_{ds}(t) = v_{RF}(t) g_{ds}(t) \tag{3}$$

For strong inversion $g_{ds}(t)$ can be approximated to :

$$g_{ds}(t) = \frac{W}{L} \mu_n C_{ox} (v_{gs}(t) - V_{th} - v_{ds}(t)) \tag{4}$$

$$g_{ds}(t) = \frac{W}{L} \mu_n C_{ox} (\frac{v_{RF}(t)}{2} + V_g - V_{th}) \tag{5}$$

W, L, μ_n, C_{ox} and V_{th} have the usual meaning in the classic CMOS equations. The expression of $i_{ds}(t)$ can be obtained from equation (5).

$$i_{ds}(t) = \frac{W}{L}\mu_n C_{ox}\left(\frac{v_{RF}(t)^2}{2} + v_{RF}(t)(V_g - V_{th})\right) \quad (6)$$

The DC response can be calculated from (6):

$$I_{ds} = \frac{W}{L}\mu_n C_{ox}\frac{{V_{RF}}^2}{4} \quad (7)$$

Where V_{RF} is the RMS value of $v_{RF}(t)$.

The current responsivity calculated from equation (7):

$$I_v = \frac{I_{ds}}{P_{in}} = I_{ds}\frac{R_{in}}{{V_{RF}}^2} = \frac{W}{L}\mu_n C_{ox}\frac{R_{in}}{4} \quad (8)$$

Where R_{in} corresponds to the real part of the detector RF input impedance. In order to obtain the voltage responsivity, the expression of V_{ds} must be calculated first:

$$V_{ds} = \frac{I_{ds}}{G_{ds}} = \frac{{V_{RF}}^2}{4(V_g - V_{th})} \quad (9)$$

$$R_v = \frac{V_{ds}}{P_{in}} = \frac{R_{in}}{4(V_g - V_{th})} \quad (10)$$

According to [1], the NEP is only determined by the thermal noise associated to the channel transconductance G_{ds} and the voltage responsivity R_v. Since the transistor channel is not DC biased, the noise spectral power density at the drain output is $4K_BT/G_{ds}$.

$$NEP = \frac{\sqrt{N_0}}{R_v} = \sqrt{\frac{64K_BT}{{R_{in}}^2\frac{W}{L}\mu_n C_{ox}}(V_g - V_{th})} \quad (11)$$

2. Appendix chapter II

2.1. Transistors' intrinsic elements extraction

The intrinsic elements are extracted using the admittance matrix from a two port network analysis. Figure A-2 shows the transistor small signal equivalent circuit used for the extraction.

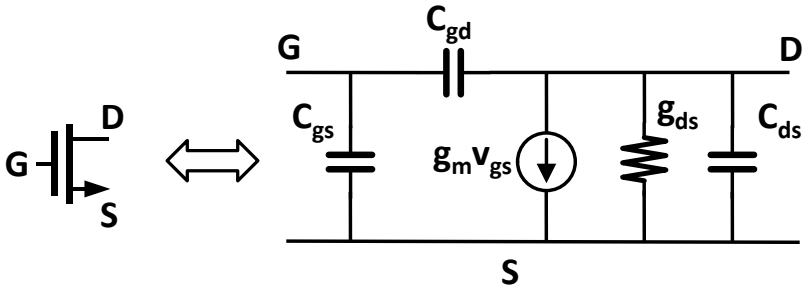


Figure A - 2 : Transistor small signal equivalent circuit.

$$Y_{11} = jC_{gs}\omega + jC_{gd}\omega \quad (12)$$

$$Y_{12} = -jC_{gd}\omega \quad (13)$$

$$Y_{22} = jC_{ds}\omega + g_{ds} + jC_{gd}\omega \quad (14)$$

$$Y_{21} = g_m - jC_{gd}\omega \quad (15)$$

$$g_m = Y_{21} - Y_{12} \quad (16)$$

$$g_{ds} = real(Y_{22}) \quad (17)$$

$$C_{gs} = \frac{imag(Y_{11} + Y_{12})}{\omega} \quad (18)$$

$$C_{gd} = -\frac{imag(Y_{12})}{\omega} \quad (19)$$

$$C_{ds} = \frac{imag(Y_{22} + Y_{12})}{\omega} \quad (20)$$

2.2. Transistor cut-off frequencies

Figure A-3 presents the advanced small signal equivalent circuit from [2] in order to develop the cut–off frequencies equations (21) and (22).

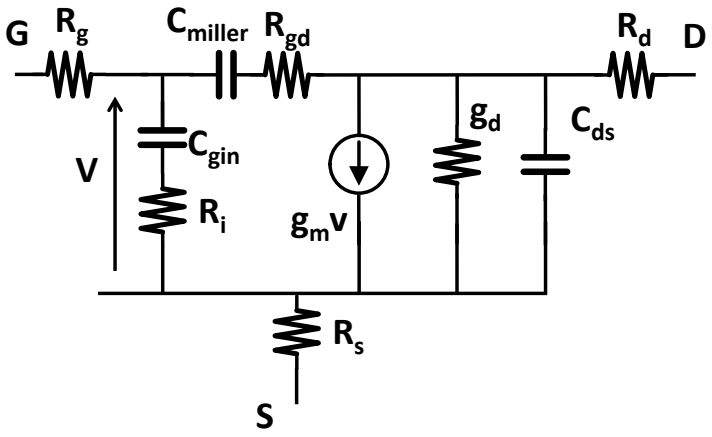


Figure A - 3 : advanced transistor small signal equivalent circuit from [2].

$$f_{max} = \frac{f_c}{(1+\frac{C_{miller}}{C_{gin}})} \frac{1}{\sqrt{4g_d\left(R_g+R_s+R_i\right)+2\frac{C_{miller}}{C_{gin}}(\frac{C_{miller}}{C_{gin}}+g_m(R_s+R_i))}} \quad (21)$$

$$f_t = \frac{f_c}{1+\frac{C_{miller}}{C_{gin}}\left(1+(R_s+R_d)(g_m+g_d)\right)+(R_s+R_d)g_d} \quad (22)$$

Where C_{miller}, C_{gin}, g_d, g_m, R_g, R_s, R_i and R_d can be identified in Figure A-3. $fc=g_m/2\pi C_{gin}$.

3. Appendix chapter III

3.1. 285 GHz oscillator capacitance calculations

Figure A-4 shows transistor schematic of this oscillator.

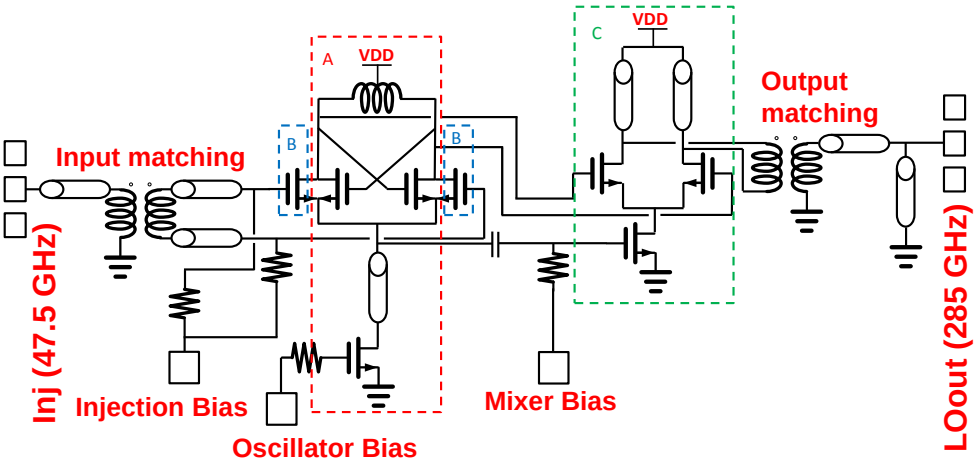


Figure A - 4 : transistor schematic of the 285 GHz oscillator.

The core of the oscillator corresponds to the part A. This part can be analyzed as a classic cross coupled pair LC tank oscillator. The small signal equivalent circuit is presented in Figure A-5.

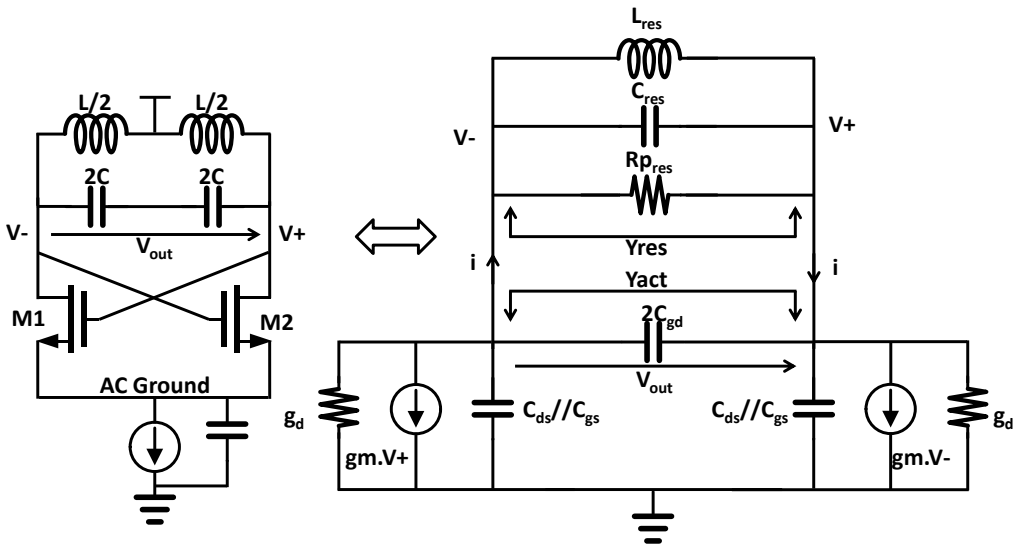


Figure A - 5 : small signal equivalent circuit of the cross coupled pair LC tank oscillator.

The total resonator admittance Y_{res} is:

$$Y_{res} = \frac{1}{jL_{res}\omega} + jC_{res}\omega + \frac{1}{Rp_{res}} \qquad (23)$$

The equivalent capacitance of part A: C_A can be obtained from the total admittance of the cross-coupled pair Y_{act}.

$$Y_{act} = \frac{i}{V_{out}} \tag{24}$$

The current i can be calculated by doing a Kirchhoff analysis of the circuit:

$$i = g_m V_- + g_d V_+ + j\left(C_{ds} + C_{gs}\right)\omega V_+ + 2jC_{gd}\omega V_{out} \tag{25}$$

Knowing that $V_{out} = V_+ - V_-$ and $V_+ = -V_-$. $V_{out}=-2V_-=2V_+$. Y_{act} becomes:

$$Y_{act} = \frac{-g_m}{2} + \frac{g_d}{2} + \frac{j\left(C_{ds} + C_{gs}\right)\omega}{2} + 2jC_{gd}\omega \tag{26}$$

This yields the expression of C_A:

$$C_A = \frac{\left(C_{ds} + C_{gs}\right)}{2} + 2C_{gd} \tag{27}$$

Since the goal is to calculate the free running oscillation frequency, the C_{gs} capacitor of the injection transistors are shorted allowing only the C_{gd} and C_{ds} capacitors to have an impact on the overall oscillation frequency. Because of the fact that these capacitors are connected in parallel the expression of C_B is:

$$C_B = \frac{C_{gd} + C_{ds}}{2} \tag{28}$$

The mixer used to multiply the fundamental signal with the push-push harmonic adds also a capacitance to the system. This circuit has been simplified by only taking into account the differential pair capacitances. The C_C parallel capacitance expression is:

$$C_C = \frac{1}{2}\left(\frac{C_{ds}C_{gd}}{C_{ds} + C_{gd}} + C_{gs}\right) \tag{29}$$

3.2. 276 GHz triple push oscillator admittance calculations.

The small signal equivalent circuit of the triple push architecture is presented in Figure A-6:

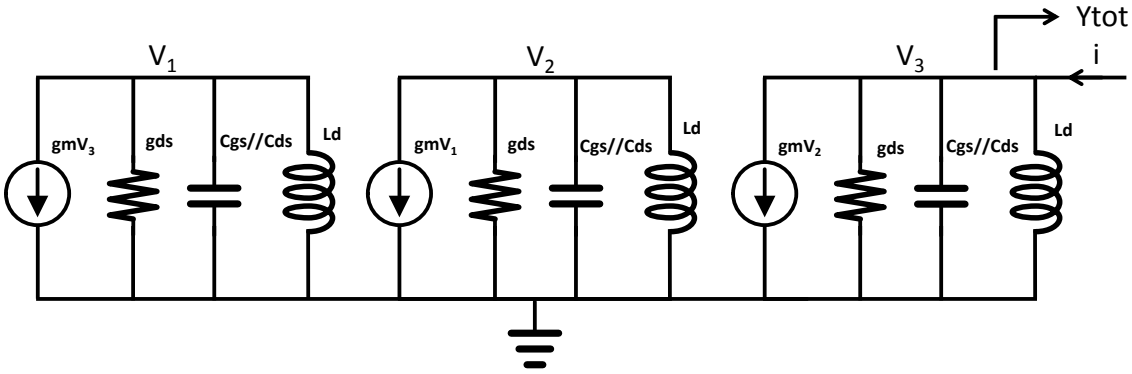


Figure A - 6 : small signal equivalent circuit of the triple push oscillator.

In order to obtain the fundamental oscillation frequency, the total admittance of the oscillator must be calculated. The C_{gd} capacitances have been removed for simplification purposes. The admittance Y_A is the parallel association of g_{ds}, C_{gs}, C_{ds} and L_d:

$$Y_A = j\omega(C_{gs} + C_{ds}) + \frac{1}{jL_d\omega} + gds \tag{30}$$

The voltage equations are:

$$V_1 = -\frac{g_m V_3}{Y_A} \tag{31}$$

$$V_2 = \frac{{g_m}^2 V_3}{{Y_A}^2} \tag{32}$$

Since the general expression of Y_{tot} is:

$$Y_{tot} = \frac{i}{V_3} \tag{33}$$

The goal is to find an expression with i and V_3:

$$Y_A V_3 = i - \frac{{g_m}^3 V_3}{{Y_A}^2} \tag{34}$$

$$Y_{tot} = Y_A + \frac{{g_m}^3}{{Y_A}^2} \tag{35}$$

$$Y_{tot} = j\omega(C_{gs} + C_{ds}) + \frac{1}{jL_d\omega} + gds + \frac{{g_m}^3}{(j\omega(C_{gs} + C_{ds}) + \frac{1}{jL_d\omega} + gds)^2} \quad (36)$$

4. References

[1] E. Ojefors, U. R. Pfeiffer, A. Lisauskas, H. G. Roskos, E. Öjefors, and S. Member, "A 0.65 THz Focal-Plane Array in a Quarter-Micron CMOS Process Technology," *Solid-State Circuits, IEEE J.*, vol. 44, no. 7, pp. 1968–1976, 2009.

[2] A. Siligaris, G. Pailloncy, S. Delcourt, R. Valentin, S. Lepilliet, F. Danneville, D. Gloria, and G. Dambrine, "High-Frequency and Noise Performances of 65-nm MOSFET at Liquid Nitrogen Temperature," *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1902–1908, Aug. 2006.