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Récepteurs de réveil très faible consommation utilisant des techniques de filtrage de type N-Path

Ultra-Low Power Wake-Up Receivers Using N-Path Filtering Techniques

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Abstract

Ultra-Low Power (ULP) Wake-Up Receivers (WuRx) using N-path filtering techniques

The continuous development of performant systems intended for Wireless Sensor Networks (WSN) sets an exciting motivation to bring “intelligence” to our environment. Multiple researches have been addressed to the development of advanced methodologies enabling the possibility of providing objects with individual wireless sensing devices. Set as sensor networks, these emerging WSN enables autonomous monitoring of diverse environments for applications such as medical care, environmental monitoring, system security and smart structures. To guaranty dense node deployment and long lifetime, each sensor node must be small, low-cost and low-power. In order to fulfill the WSN low-energy requirements, asynchronous rendez-vous schemes based on Wake-Up Receivers (WuRx) may be implemented.

This thesis research focuses on the development of a compact and low-cost ultra-low power wake-up receiver providing high sensitivity and strong interference rejection. The proposed architecture overcomes the need of high-Q time-base references by combining a low-Q resonator-referred local oscillator and distributed multi-stage signal-path high-Q filtering obtained by means of integrated ULP electronic means. Based on a Dual-IF architecture, this WuRx takes creative advantage of the N-path passive-mixers (N-PPM) impedance frequency translation principle to enhance the sensitivity and provide strong interferer immunity. Implemented in a 65nm CMOS technology from STMicroelectronics, this thesis work pushes the state-of-the-art boundary, proposing a 2.4GHz On-Off Keying (OOK) dual-IF WuRx with -97dBm sensitivity and -27dB carrier-to-interferer ratio at 5MHz carrier frequency offset, while consuming 99µW.

Résumé

Récepteurs de réveil très faible consommation utilisant des techniques de filtrage de type N-Path

Le développement continu des systèmes dédiés à des réseaux de capteurs sans fils présent une grande motivation afin d'apporter "intelligence" à notre environnement. Plusieurs recherches ont été adressées au développement des méthodologies permettant de doter notre environnement avec des capteurs sans fils permettant un contrôle autonome des systèmes pour des applications médicales, environnementales, de sécurité et de structures intelligentes. Afin de garantir un déploiement dense des capteurs avec une longue durée de vie, chaque nœud doit être petit, pas cher et très faible en consommation de puissance. Afin de garantir une faible consommation, ces réseaux des capteurs doivent être implémentés suivant des schémas de rendez-vous asynchrones basés sur des récepteurs de réveil (en anglais, Wake-Up Receivers – WuRx).

Cette recherche de thèse porte sur le développement d'un récepteur de réveille compacte et à faible cout, fournissant très faible niveaux de consommation de puissance, une forte sensitivité et une forte tolérance aux interférences. L'architecture proposée survient aux besoins des références de temps à haut facteur-Q en combinant un oscillateur local, référée à un résonateur à faible facteur-Q, et des filtres passives a N-chemins à haut facteur-Q, distribués en plusieurs étages tout le long du chemin de réception. Implémenté en une technologie 65nm CMOS de STMicroelectronics, ce travail de thèse propose un WuRx à double bande IF, avec une architecture travaillant à 2.4GHz avec une consommation de puissance de 99μW, une sensitivité de -97dBm et une rejection d'interférence de -27dB à une fréquence offset de 5MHz.

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Table of Contents

Chapter 1
Introduction

The continuous development of performant systems intended for Wireless Sensor Networks (WSN) sets an exciting challenge to bring "intelligence" to our environment. Multiple studies have addressed the development of advanced methodologies and techniques enabling the possibility of providing objects with individual wireless sensing devices. These emerging WSN solutions allow the monitoring of diverse environments through an autonomous sensing methodology. To guarantee dense node distribution and long lifetime of the system, each sensor node must be small, extremely low-cost, must present Low-Power (LP) consumption and must provide successful wireless communication. This system optimization is obtained through several layers of optimization including: technology, device architecture, circuit architecture design and protocol communication. This thesis focuses on the wireless reception communication path optimization, at the circuit architecture design level and the implementation of Ultra-Low Power (ULP) Wake-Up Receivers (WuRx) using N-path filtering techniques.

This chapter introduces the global concepts of WSN with their different requirements, communication protocols and applications. A concrete description of different applications involving wake-up receivers is also addressed. This chapter concludes with the thesis purpose and the thesis dissertation organization.

1.1. Wireless Sensor Networks (WSN)

Wireless sensor networks are composed of an autonomous mesh of sensing nodes. From tenths to thousands of nodes, these networks are designed to procure multi-hop wireless communication at any environmental complexity level. WSN are defined within the standard IEEE 802.15.4 [Adams]. This protocol defines the technical specifications to ensure communication between nodes. A summary of the principal parameters is presented in Table

1.1 [Adams] [Henkel]. This standard is characterized by its ease of attaining LP performances. Sensitivity is defined according to the frequency band and the data rate. Coexistence within multiple nodes in the same band is an important issue to highlight, in order to guarantee successful system wireless communication [Howitt]. Adjacent channel rejection specifications are not so aggressive in this protocol, however, higher rejection performances may be considered for dense WSN with high number of nodes.

Frequency band $(\boldsymbol{MHz})$	868.3	$902-928$	$2400-2483.5$
Number of channels	1	10	16
Channel bandwidth $(\boldsymbol{MHz})$	0.6	2	5
Data rate $(\boldsymbol{kb/s})$	20	40	250
Sensitivity $(\boldsymbol{dBm})$	-92	-92	-85
Adjacent channel rejection	$0dB$		
2nd adjacent channel rejection	$30dB$		
Unlicensed geographic usage	Europe	Americas (approx.)	Worldwide

Table 1.1. IEEE 802.15.4 global receiver specifications.

1.1.1. WSN requirements

In order to make WSN technology viable, each individual node of the network has to respect drastic physical and wireless reception constraints including physical occupied volume, cost, power consumption, sensitivity and immunity against interferers. Below is a description of each of these parameters:

- **Size:** To fit discreetly within diverse environments, each node must be very compact, such as to not affect the functionality and the physical aspect of the targeted systems.
- **Cost:** To ensure success deployment of dense node WSN, each of the nodes should bear the lowest cost possible.
- **Power consumption:** For WSN each node is ideally supplied with a harvested energy system. In order to provide autonomous functionality and extended

lifetime, each node should be energy efficient so as to fit within the power budget provided by the energy harvesting module.

- **Sensitivity:** Power optimization is also obtained through the reduction of the number of nodes. To provide an energy efficient system, the receivers should present high sensitivity in order to provide long distance wireless communications, therefore minimizing the number of nodes.
- **Interference rejection:** In order to guarantee the coexistence of several nodes communicating on the same band, their receiver should have a robust architecture designed to tolerate interference.

1.1.2. WSN rendez-vous schemes

The study of WSN had caused engineers to search for the most power efficient way to provide communication between nodes. Knowing that nodes do not need to communicate continuously, effective energy reduction can be obtained using duty-cycled nodes. Three main *rendez-vous* schemes providing duty-cycled wireless communication have been proposed [Lin]:

- **Synchronous:** In this case, all nodes from the network accord a periodically synchronized rendez-vous. Success communication is ensured, but the power attributed to the synchronization may exceed the power budget of the system.
- **Pseudo-Asynchronous:** In order to further reduce the power consumption, receptor nodes remain in standby mode and are awaken only through a request made by the source node. These nodes may present little standby power (leakage power), in order to optimize the system average power under long off periods.
- **Asynchronous:** Classified as the most power efficient, this rendez-vous scheme involves nodes composed of two circuits: a main radio and a wake-up receiver. In this case, the main radio is turned-off while the WuRx remains on, monitoring the channel for the reception of any incoming wake-up signal. As soon as the WuRx detects a wake-up signal, the main radio is turned-on to proceed with the main data transmission.

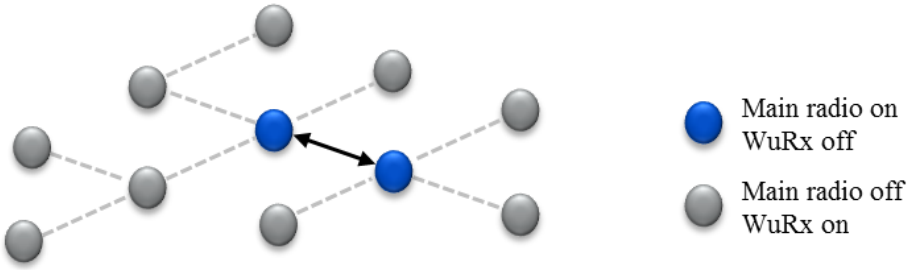


Figure 1.1. WSN asynchronous scheme using always-on WuRx.

To justify the use of WuRxs, their effective active power must be negligible compared to the one of the main radio [Lin]. If further power consumption reduction is required, the WuRx should be duty-cycled. This methodology classifies the asynchronous scheme in two operational modes: the reactive mode (Figure 1.1), also called always-on mode, and the duty-cycled mode. According to the targeted application, if latency is the priority, then the reactive mode would be preferred; otherwise, if power is the priority, the duty-cycled mode would be preferred. This leads to a trade-off between minimum achievable power and minimum latency.

Other detailed analysis involving asynchronous duty-cycled WuRx based WSN is presented in [Mazloum] [Su] [Vodel]. Further low-power and interference robustness optimization may be provided by digitally encoding the transmitted wake-up signal [Oller]. This leads to strong immunity against interferers in dense node WSN. Other analysis of different WuRx schemes, sensor node clustering methodologies and networking algorithm are respectively provided in [Demirkol], [Blanckenstein] and [Otis03].

In conclusion, asynchronous WuRx based scheme appears to be the most power efficient rendez-vous scheme for WSN applications. This communication scheme may be used for network lifetime extension enabling system full power autonomy. Always-on operational mode may be used for systems demanding reactive sensing. Duty-cycled operational mode may be employed for extreme low-power WSN where latency is not the priority.

1.1.3. WSN applications

The simplicity and the flexibility of WSN have opened the doors for multiple applications in different domains. It principally concerns the monitoring and the surveillance of processes with the objective of providing ambient intelligence [Weber]. The deployment of nodes usually depends on the physical environment, the physical area to cover, the network expected lifetime, the type of data to transmit and the number of required nodes. Below are some of the most relevant WSN applications:

- **Health-care monitoring:** Medical applications involve the monitoring of several different processes including: motion and activity monitoring, physiological monitoring and mobile patient vital sign monitoring [Z.Zhang] [Garcia] [Jara]. Other applications such as biosensors provide the study of physiological change and presence of chemical or biological materials [Hart].
- **Environmental monitoring:** Applications for environmental monitoring include volcano activity, forest fire detection, natural disaster prevention, air pollution, air temperature, humidity, water quality and solar radiation monitoring [Hart].
- **Smart structures:** The flexibility of WSN provides an easy way for sensor nodes to provide smart autonomous behavior to complex structures. In this way, WSN enables the possibility of developing smart homes, smart buildings, smart cities, smart hospitals, smart forests, and so on.
- **Security:** WSN may also be applied in secure environments to provide surveillance monitoring, confidential physical access and personal tracking [Jelicic].
- **Entertainment:** WSN also allow for applications designed for personal entertainment. They principally involve intelligent Body Area Networks (BAN) for high data rate applications such as video games [Wada].

1.2. Wake-up receivers for WSN applications

WuRxs may follow the IEEE 802.15.4 standard specifications. Nevertheless, the data rate and the adjacent channel rejection may be reviewed for the target WuRx based WSN applications. In this case, we may consider a data rate below $100kb/s$, because a wake-up

signal does not need high data rate, and higher interference rejection to allow coexistence of multiple nodes.

Taking into account these specifications, WuRx based WSN may target applications requiring slow periodical information sampling for process presenting small changes over long time periods. Some examples are: temperature monitoring, autonomous irrigation fields, motion presence monitoring in isolated environments, smart roads preventing of traffic jams, accidents or frozen soils, and biosensors integrated in the human body for periodical health monitoring.

1.3. Thesis purpose

The research in this thesis focuses on the development of a wake-up receiver compliant with all the physical and wireless reception specifications required for wireless sensor networks applications in accordance with the standard IEEE 802.15.4. With the objective of providing a compact and ultra-low cost solution, this study aims to develop an ULP WuRx architecture enabling high sensitivity levels and strong immunity against interferers. Multiple methodologies used to address different technologies, circuit architecture designs, system designs and protocol communication layers are discussed and developed in this thesis to reach the initial specifications established. To start, a complete analysis of the main WuRxs design considerations and the different WuRx architectures proposed in the literature is presented. In order to successfully achieve the main objective of the proposed WuRx, a key ULP filtering technique allowing aggressive narrow band-pass filtering for high bandwidth reduction and strong interference rejection is developed. Detailed theory analysis of this N-path filtering technique, is also presented.

In order to validate the theory and the methodology, this thesis then focuses on the solid state implementation for the proposed WuRx by using the 65nm CMOS technology from STMicroelectronics. Another purpose of this study concerns the validation of an innovative and compact packaging solution allowing for the co-integration of the silicon die with external passive components, as required by the system.

Finally, this research sets out to provide a critical overview of the proposed work, in order to encourage new perspectives and propose novel and improved WuRx architectures for a better WSN implementation.

1.4. Thesis organization

This thesis is organized as follows: Chapter 2 presents the main objectives and specifications of this thesis. It also describes the principal considerations for ultra-low-power receiver design optimization. Three main specifications are analyzed in depth: the power consumption, the sensitivity and the interference rejection. A global overview of the different WuRx architectures proposed in the literature is also provided. This chapter concludes by highlighting the main advantages and drawbacks of previous works, for a better understanding of the path to follow to achieve the established objectives.

In Chapter 3, an analysis of the ULP N-path passive mixer principles is provided. Three principal 2-path based ULP configurations enabling high-Q filtering are studied: the single-to-differential, the fully differential and the parallel 2-path passive mixer configurations.

Chapter 4 presents a first circuit implementation integrating some of the WuRx design consideration presented in Chapter 2, and the single-to-differential 2-path passive mixer filtering technique developed in Chapter 3. This Chapter proposes an N-Path Filter Based Front-End section of a wake-up receiver. A complete circuit design and packaging implementation is developed. Measurement circuit results are used to validate the theory, design and packaging proposed.

Chapter 5 presents the final full WuRx circuit of this thesis. Based on the different techniques developed in Chapter 3 and demonstrated in Chapter 4, this chapter proposes an Interferer Resilient WuRx with Multi-Layer N-Path Dual-IF Architecture. A description of the WuRx architecture is presented and an IC and packaging implementation are also provided. Characterization and circuit measurements are detailed.

Research thesis conclusions are addressed in Chapter 6 with a global overview of the proposed work and future research perspectives.

Chapter 2

Wake-Up Receiver Considerations

This chapter outlines the main considerations for ULP wake-up receiver design. The first part presents a characterization of the main RF reception specifications allowing for power optimization, sensitivity enhancement and strong immunity against interferers. The second part provides an overview of the state-of-the-art in wake-up receivers. To conclude, the chapter highlights the key design strategies for wake-up receivers dedicated to wireless sensor nodes.

2.1. WuRx considerations

Wake-up receiver's strategy is the result of multiple design optimizations interacting with different system techniques, receiver architectures and hybrid-technologies; in view of energy efficiency optimization applied to the emerging age of the Internet-of-Things (IoT). In addition to the restricted energy specifications, the WuRx should also provide high radio frequency sensitivity and selectivity reception performance to ensure wireless communication within dense node networks. Table 2.1 shows the targeted WuRx specifications for WSN applications. Wake-up receivers should target a power consumptions below $100\mu W$ for autonomous energy-harvested nodes [Ingram], data rates below $100kb/s$ for system energy-efficiency, a minimum sensitivity of $-92dBm$ to be IEEE.802.15.4 standard compliant and an out-of-band interferer rejections larger than $25dB$ and $45dB$, for the first and the second adjacent channels respectively, for immunity in dense sensor node environments. This section describes the major considerations for such ULP WuRx design.

Power consumption	$< 100\mu W$
Data rate	$< 100kb/s$
Sensitivity	$< -92dBm$
Adjacent channel rejection	$> 25dB$
2nd adjacent channel rejection	> 45dB
Physical requirements	Compact and cost-less

Table 2.1. Wake-up receiver specifications for the work presented in this thesis.

2.1.1. Power consumption

In modern integrated circuits, power consumption optimization is achieved at different design levels according to the receiver system specifications, through global design techniques and specific design strategies, involving voltage supply reduction, receiver architecture design and system specifications.

Voltage supply reduction

In general, the power dissipation of an electrical system can be reduced by reducing the voltage supply. With the scaling down of the voltage supply, CMOS transistors work in the subthreshold operational mode, also called weak inversion regime, for which the gate to source voltage V_{GS} is smaller than the transistor threshold voltage V_{TH} ($V_{GS} < V_{TH}$). This operation mode has been used for years in CMOS IC design [Vittoz] and has become very popular in modern low-voltage designs. Transistors operating in this regime behave as bipolar transistors, for which the drain to source current (I_{DS}) follows an exponential behavior with respect to its V_{GS} voltage [Rabaey01].

$$I_{DS,WI} = I_S e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \tag{2.1}$$

Where $I_S = 2n\mu C_{ox} \frac{W}{L} V_T^2$, n is the slope factor ($n = 1 + C_d/C_{ox}$), V_T is the thermal voltage ($V_T = KT/q$), C_d is the depletion transistor capacitance, C_{ox} is the transistor oxide layer capacitance, μ is the transistor charge-carrier effective mobility, W is the transistor gate

width, L is the transistor gate length, K is the Boltzmann constant ($K = 1.38 \cdot 10^{-23} J/K$), T is the temperature in degrees Kelvin and q is the elementary proton charge ($q = 1.602 \cdot 10^{-19} C$). Considering the expression above, the transistor transconductance can be easily derived.

$$g_{m,WI} = \frac{\delta I_{DS,WI}}{\delta V_{GS}}\Big|_{V_{DS}=Cte} = \frac{I_{DS,WI}}{nV_T} \tag{2.2}$$

From this equation, the weak-inversion drain to source current can be also expressed as a function of its transconductance: $I_{DS,WI} = nV_T g_{m,WI}$. The key advantage of this regime is the transistor power efficiency, defined as the ratio between the transistor transconductance and drain to source current. In weak-inversion mode, the power efficiency is optimized and is defined as $g_{m,WI}/I_{DS,WI} = 1/nV_T$. Figure 2.1 shows the power efficiency of an N-MOS transistor as a function of V_{GS}. Here, the transistor is forced to be in saturation by setting $V_{GS} = V_{DS}$. As V_{GS} increases, the $1/nV_T$ subthreshold power efficiency is gradually decreased to approximately $2/(V_{GS} - V_{TH})$ in strong inversion. Clearly, power efficiency optimization is obtained in the transistor weak-inversion operational mode.

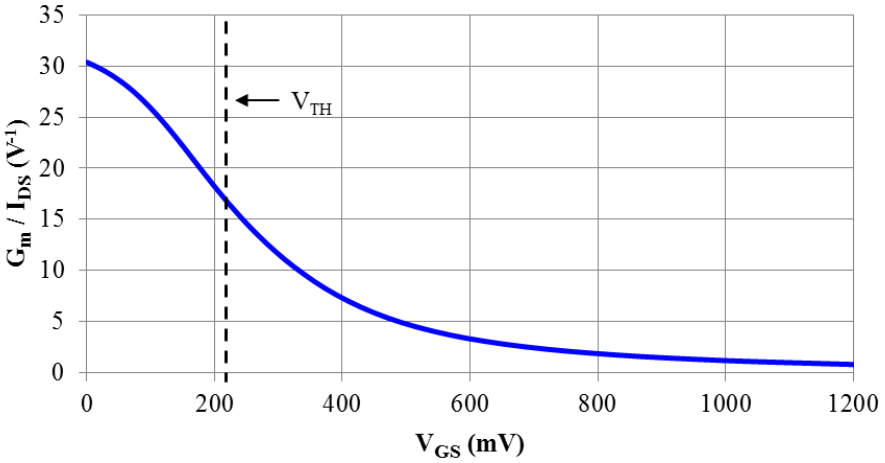


Figure 2.1. Low Voltage Threshold General Purposes (LVTGP) 65nm N-MOS transistor saturation power efficiency as a function of the gate to source voltage with $V_{GS} = V_{DS}$ and $V_{TH} = 230mV$.

A popular solution to extend the transistor performance for low voltage IC design is body biasing. This technique brings the possibility to reduce the threshold voltage to effectively increase the transistor transconductance gain, particularly suited for analog design. Nevertheless, this threshold voltage reduction technique is usually translated to a leakage

current increment, which entails a signal-to-noise reduction. A common way to reduce this effect without increasing V_{TH}, is to avoid minimum transistor lengths, so as to minimize the leakage current and process variations. Special attention must also be paid to do not forward bias the source-to-bulk or the drain-to-bulk PN diode junctions when applying body biasing. In modern CMOS technologies, this constraint is eliminated by back-to-back diode based body structures.

Another important parameter to define is the voltage headroom allocated to each transistor. In low-voltage weak-inversion based configurations the functionality of each transistor must be optimized according to its functionality. In this case, it is preferable to allocate maximum voltage headroom to transistors working in amplification, and minimum voltage headroom to transistors working as DC bias supplies, such as current sources. For low-power low-voltage analog IC design, it is also highly recommended to apply stacking current-reused strategies. The concept behind this technique is to reuse the same DC current in different blocks or for different MOS devices, in a vertical configuration, in order to minimize the power consumption. Of course, this stacking methodology needs to cope with the signal cross-talk generated between the different stages, especially for stacked RF stages working at different operational frequencies, such as the Low-Noise Amplifier (LNA) and passive mixer stacked configuration used in [Pandey].

Receiver architecture

The power restriction constraints demanded on WuRxs have consecutively caused engineers to question the design methodology and entirely rethink the architectures for further power optimization. In order to obtain power efficiency at a system level, high-frequency blocks must be minimized, and in some cases, even totally eliminated. In the case of receivers, the most critical blocks are the Phase Locked Loop (PLL) frequency synthesizer, the Low-Noise Amplifier (LNA) and the RF mixer.

From the stand point of PLLs, energy optimization is achieved by the complete elimination of the active feedback loop. In this case, the LO signal is provided through open-loop VCO systems by using different types of architectures and methodologies. In the literature, we find two different architectures for the open-loop LO signal generation: the ring

oscillators and the LC oscillators. Recent research has shown that with technology scaling, the most power efficient topology is the ring oscillator [Pletcher02]. Despite its power consumption performances, open-loop ring oscillators suffer from very low frequency accuracy and high phase noise. To compensate this behavior, several architectures including high-Q tank resonator based oscillators and injection locking techniques have been proposed. Further description of the different architectures proposed in the State-of-the-Art is addressed in section 2.2.

With voltage supplies scaling down, the transistor transition frequency f_T is decreased. Figure 2.2 shows the f_T frequency of an N-MOS transistor with $V_{GS} = V_{DS}$ and $V_{TH} = 230mV$. The maximum f_T frequency decreases exponentially (in a logarithmic scale) as the V_{GS} voltage is reduced. For subthreshold voltages, the f_T hardly exceeds the gigahertz range. Important design efforts have to be performed for weak inversion based clock generation stages where maximum voltage headroom should be allocated to the amplification transistors used in the oscillator's loop gain.

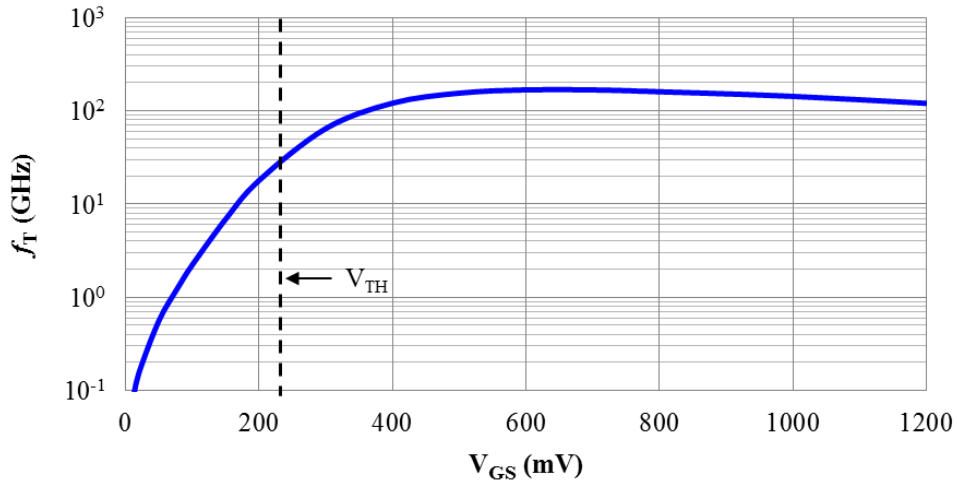


Figure 2.2. Low Voltage Threshold General Purposes (LVTGP) 65nm N-MOS transistor f_T frequency as a function of the gate to source voltage with $V_{GS} = V_{DS}$ and $V_{TH} = 230mV$.

LNAs are usually used as the first active block of receivers in order to provide substantial low-noise voltage gain (Figure 2.3.a). Unfortunately, due to its high operational frequency and wide-bandwidth requirements, the LNA structures require very high power consumption. As an alternative, designers have proposed mixer-first configurations in which the LNA is no longer at the RF-band but at the Intermediate Frequency (IF) band, to

aggressively reduce the power consumption and effective bandwidth requirements (Figure 2.3.b) [Richmond]. In this case, the mixer must provide high linear frequency responses in order to guarantee a wide RF input signal dynamic. Further power optimization can be reached by using passive mixer structures [Cook01]. However, the implementation of these solutions is usually transformed in a trade-off between power, noise and linearity.

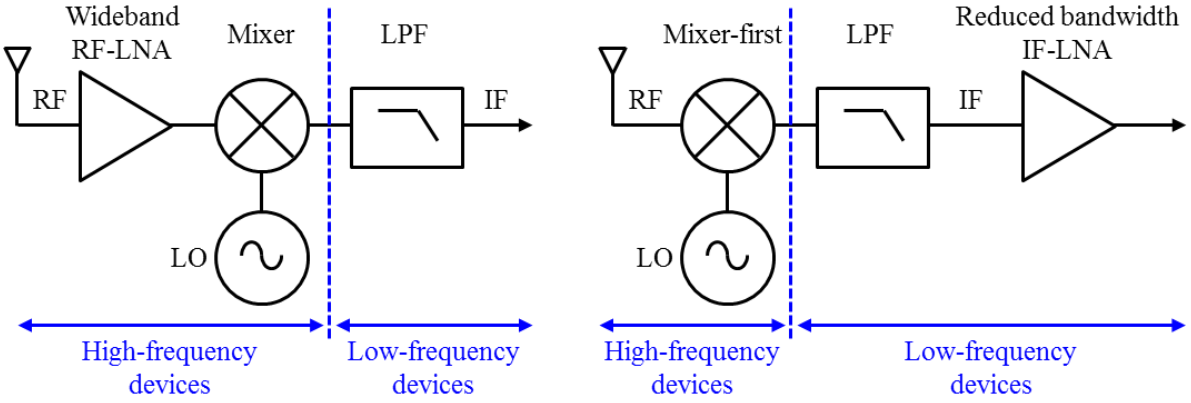


Figure 2.3. Traditional front-end receiver architecture (a) and low-power mixer-first receiver architecture.

Having identified the key parameters for power saving on the RF blocks, it is worth specifying which receiver architecture and which frequency plan to adopt.

Homodyne receivers, perform direct downconversion of the desired RF signal directly to DC. Though widely known for its simplicity and its non-image frequency advantage, the popularity of homodyne architectures has been compromised in light of multiple constraints including: the high-Q filtering required either at the front-end or at the baseband to provide the appropriate channel selection and interference signal attenuation, the flicker noise, the reciprocal mixing and the DC-offset problems, which can completely drown the desired signal at the output of the mixer if not enough front-end gain is provided. Furthermore, these configurations require low-noise and precise LO signal generation resulting in a power hungry solution. To overcome this issue, self-mixing architectures can be implemented. However, they still require high power for the front-end LNA. In summary, homodyne receivers appear to be the most power efficient architectures; however, their wireless communication performances can be limited by the noisy behaviors found at the output of the mixer.

Heterodyne receivers take advantage of the IF frequency to reduce the influence of DC flicker noise, DC voltage offsets and reciprocal mixing problems. However, homodyne receivers suffer from one serious drawback: the image frequency. Defined as $\omega_{IM} = \omega_{LO} - \omega_{IF}$, the image frequency response suggests that all in-band noise and interferers found at ω_{IM} are downconverted, together with the desired RF signal, to the same IF frequency ($\omega_{IF} = \omega_{RF} - \omega_{LO} = \omega_{LO} - \omega_{IM}$). The superposition of both signals might disturb the reception of the desired signal. To overcome this issue, very narrow RF Band-Pass Filters (BPF) [Bae03] [Pletcher02] or IF-polyphase networks [Brown] [D.R.Barber] [Behbahani] [Drago] can be implemented. In ultra-low power receivers, the image rejection can be performed at the RF signal-path by introducing external High-Q Microelectromechanical System (MEMS) as fixed frequency BPFs. IF-polyphase networks should be avoided as they request extra power budget, to generate the I/Q quadrature LO signals and IF band amplification chains. To conclude, heterodyne receivers offer the best power-to-noise performances, however, the image frequency problem must be studied carefully for optimum performance.

System specifications

Wake-up receivers' power consumption optimization is achieved by also considering top level system specifications, such as the modulation scheme of the RF input desired signal. Due to its simplicity and its power efficient behavior, the On-Off Keying (OOK) Amplitude-Shift Modulation (AM) scheme shows to be the most suitable modulation scheme for WuRxs applied to WSN applications. This amplitude modulation is characterized by a simple signature for which the digital symbol "0" is understood as the absence of signal, and the digital symbol "1" is agree by the presence of a sinusoidal carrier frequency. For low power requirements, complex modulation schemes, like quadrature shift keying modulations, should be avoided for their heavy digital modulation and demodulation treatment. Since the WuRx objective is to detect incoming wake-up signals with very weak bit-information, low data rates below $100kb/s$ should be considered.

For extreme-low-power applications it is highly recommended to integrate duty-cycle operational modes in wake-up receivers. This technique can be optimized by reducing the

receiver leakage power by implementing stacked transistor structures or dynamic transistor body biasing circuits for threshold enhancement and current leakage reduction. Nevertheless, this methodology may result in a power-latency trade-off, which has to be optimized according to the targeted WSN application.

In summary, ultra-low power consumption in WuRx is obtained thanks to several efforts applied at different layers including: technology, architecture design and system design. Generally speaking, power consumption optimization is usually translated in a power and noise tradeoff. The most intuitive way to reach low-energy levels is to reduce the voltage supply. In this way, transistors can operate at the most power efficient operational mode: the weak-inversion regime. High frequency blocks should also be minimized. For high reception performance, heterodyne architectures are preferred for their superior performance in terms of DC flicker noise, DC voltage offsets and reciprocal mixing. Image frequency rejection can result in a trade-off between power and desired signal distortion. From a system perspective, low data rate OOK modulation is identified as being the most energy efficient modulation scheme. Duty-cycled asynchronous WuRx based systems can provide extended power saving, with the drawback of communication latency.

2.1.2. Sensitivity

The most challenging specification for wake-up receivers is the sensitivity. The low power and the high noise constraints limit the level of the minimum detectable RF input power with an acceptable signal-to-noise ratio. In IC design, the receiver sensitivity is directly derived from the expression of the Noise Figure (NF). This parameter is defined as a function of the noise factor (F) described by the ratio between the Signal-to-Noise Ratio available at the input (SNR_{in}) and the total Signal-to-Noise Ratio presented at the output (SNR_{out}) [Razavi02].

$$NF = 10log(F) = 10log\left(\frac{SNR_{in}}{SNR_{out}}\right) = 10log\left(\frac{P_{in}/P_{RS}}{SNR_{out}}\right) \quad (2.3)$$

Where P_{in} is the input signal power and P_{RS} is the source resistance (R_S) noise power, both per hertz of bandwidth. Assuming conjugate matching from the receiver to the source, the source resistance noise power delivered to the receiver is

$$P_{RS} = \frac{4kTR_s}{4}\frac{1}{R_{in}} = kT \tag{2.4}$$

Where k is the Boltzmann constant given in joules per degrees Kelvin and T is the temperature in degrees Kelvin. At room temperature $(T = 300°K)$, $P_{RS} = -174dBm/Hz$. Therefore, the minimum input power that the system is able to detect (minimum sensitivity S_{min} defined in dBm or in dB), over the effective integrable bandwidth (BW) defined in hertz, is given by

$$S_{min} = P_{in,min} = -174dBm/Hz + NF + 10log(BW) + SNR_{out,min} \tag{2.5}$$

This expression highlights the key parameters necessary to achieve high sensitivity performance. Knowing that P_{RS} and $SNR_{out,min}$ are constant for a given BER and a given modulation, the two parameters that need to be optimized are the noise figure and the effective bandwidth.

2.1.3. Interference rejection

As the number of nodes in WSN increases, the complexity to guarantee correct wireless communication between nodes becomes higher. In dense node WSN systems, each WuRx must offer high performance against undesired interferers. The Interference Rejection Ratio (IRR) is defined as a measure to characterize the out-of-band attenuation provided by a system. This parameter corresponds to the ratio between the in-band and the out-of-band analog frequency response of the system. Further description of this parameter is provided in section 3.2.2. Another commonly used parameter in wireless system characterization is the Carrier-to-Interference Ratio (CIR). This ratio measures the capacity of a system to receive a desired signal (Carrier) with a certain Bit Error Rate (BER), under the presence of interferers. Usually, this practice is done using a two-tone measurement, setting the carrier power $3dB$ above the minimum detectable power (minimum sensitivity), and increasing the interferer power until reach the desired BER. This procedure is repeated for different carrier-to-

interferer frequency offsets ($\Delta f_{CI} = f_{CARRIER} - f_{INTER}$). This parameter is usually given in decibels (dB) and is negative if the interferer tolerated power is higher than the carrier power ($CIR = P_{CARRIER}/P_{INTER}$). Note that the CIR differs from the IRR because it depends, not only on the analog frequency response, but on the global response of the system architecture, the digital signal filtering, the BER targeted and the signal modulation attributed.

In order to improve immunity against interferers, the WuRx must offer very sharp filtering for high out-of-band interferer attenuation. Further interference tolerance can be provided by introducing additional digital coding to the wake-up signal, so as to define individual Node Identification (Node ID) addresses for each of the system nodes. This technique allows addressing multiple nodes with a single carrier RF frequency and can also be used, to extend the immunity performance of heterodyne receivers which are not able to provide image frequency rejection. The combination of analog narrow band filtering and digital coding results in a complete solution for providing high interference resilient wake-up receivers dedicated for dense node WSN applications.

Another aspect that has to be taken into account concerning interference resilience is the reciprocal mixing. In receiver architectures, the CIR is directly related to the reciprocal mixing of the LO phase noise in presence of interferers. In most of the cases, the interferers' powers can be tens dBs above the desired RF signal. The reciprocal mixing with the LO results in an undesired overlapping of the downconverted interferer phase noise, evaluated at the frequency offset between the desired and the interferer IF signals $|(f_{INT} - f_C)|$, over the downconverted desired signal, along the effective IF integrable bandwidth (BW_{IF}). Figure 2.4 shows the reciprocal mixing in downconversion systems. The maximum phase noise at a certain frequency offset (f_{offset}) required to achieve a given $CIR = P_C - P_{INT}$ [dBm] is defined by [Pozar]

$$PN_{LO,max}\ (f_{offset}) = P_C - P_{INT} - SNR_{min} - 10log(BW_{eff})$$
$$= CIR - SNR_{min} - 10log(BW_{eff}) \quad (2.6)$$

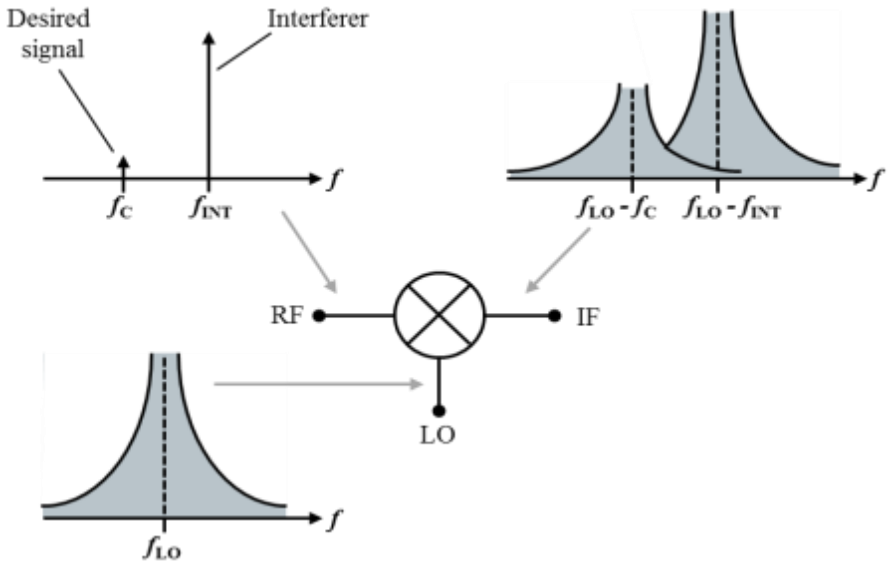


Figure 2.4. Reciprocal mixing in downconversion systems.

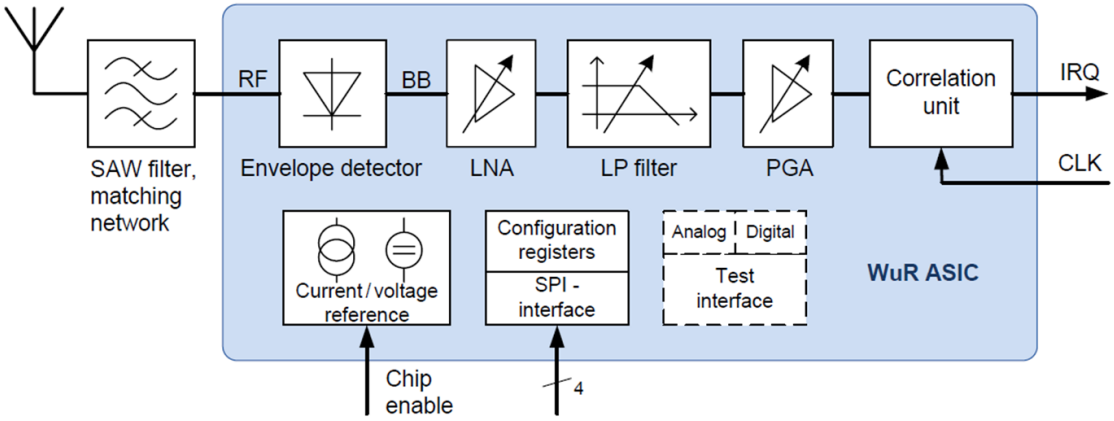
Where P_C is the desired carrier power, P_{INT} is the interferer power, SNR_{min} is the minimum signal-to-noise ratio at the output chain and BW_{eff} is the effective integrable bandwidth. In the case of a receiver requiring $-30dB$ CIR at $1MHz$ offset, with $10dB$ SNR_{min} and $1MHz$ IF bandwidth, the minimum phase noise of the LO is equal to $-100dBc/Hz$ at $1MHz$ offset. This example highlights the difficult challenge on ULP systems aiming narrow bandwidth, low LO phase noise and minimum CIR.

To conclude, the design of WuRx is achieved through the optimization of the following: power consumption, sensitivity and interference rejection. Power consumption can be reduced through the application of different techniques including low voltage supply, weak-inversion transistor operational mode and high frequency blocks reduction. Extended power saving can be obtained by implementing duty-cycled asynchronous WuRx systems. Sensitivity enhancement is attained through the reduction of the noise figure and the effective bandwidth. High interference rejection is achieved through the combination of analog narrow band filtering, digital coding and LO phase noise optimization. These three parameters lead to a true implementation of WuRx in WSN. The next section provides a global overview of several wake-up receiver architectures proposed in the State-of-the-Art.

2.2. State-of-the-Art in Wake-Up Receivers

Several WuRx architectures have been proposed in recent years in response to the high demand for power efficient WSN. These architectures offer solutions for different needs according to their intended applications. From simple envelope detection to robust low-IF configurations, this section provides an overview of the principal strengths and limitations of the different sub-$1mW$ WuRx architectures proposed in the State-of-the-Art. The global analysis of these configurations will allow us to highlight key considerations.

2.2.1. Envelope detection WuRx



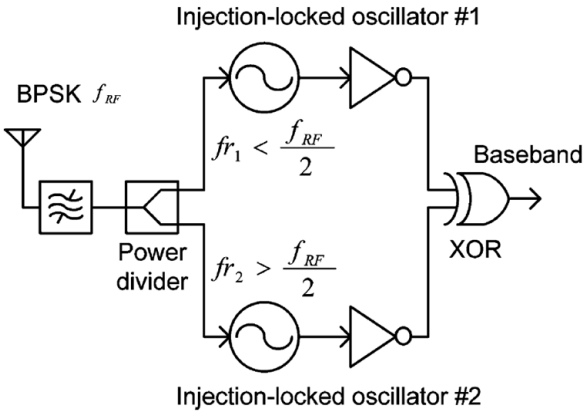
* C. Hambeck, et. al, "A 2.4µW Wake-up Receiver for wireless sensor nodes with −71dBm sensitivity", *IEEE ISCAS*, 2011.

Figure 2.5. An envelope detection based wake-up receiver block diagram.

Envelope detection WuRx architectures target OOK-AM modulated RF input signals. They are implemented using homodyne receiver architecture, presenting a direct downconversion to the DC Base-Band (BB) by self-mixing the input RF desired signal. The two main advantages of this architecture are its extremely low-energy performance, reporting sub-$1\mu W$ active power consumptions [Roberts] [Oh] [Marinkovic], and its non-image frequency homodyne behavior. Figure 2.5 presents an example of the envelope detection based WuRx presented in [Hambeck]. The principal circuit (highlighted in blue) is composed of an envelope detection stage, in this case an RF diode-based architecture, a BB amplification chain within a low-pass filter stage and a correlation unit to digitalize the output of the receiver. Despite its ULP performances, this architecture suffers from two main drawbacks linked to homodyne configurations: the DC flicker noise and the DC voltage

offsets, found at the output of the envelope detection structure. As a result of wide-band self-mixing behavior, the sensitivity of these architectures is seriously compromised by the downconversion of the RF in-band noise found at the envelope detector input. Additionally, they do not provide any rejection to out-of-band interferers. To alleviate the excess RF in-band noise downconversion and provide interference rejection, while still maintaining good energy performance, a passive narrow BPF may be added at the RF input node, before the envelope detector [Hambeck] [Daly] [Cheng]. In the case of the example presented in Figure 2.5, an external high-Q ($\sim 10^3$) RF Surface Acoustic Wave (SAW) filter is added. For noise reduction at the BB, a low-power LNA may be added at the input RF node of the receiver [Yoon]. Other techniques, such as the two-tone RF transmission, can be adopted to enhance the sensitivity and the immunity of the system [Huang01]. In conclusion, envelope detection WuRx configurations offer the advantage of image frequency rejection with very LP performance ($P_{min} = 98nW$ [Roberts]). However, they require high-Q external RF BPF for sensitivity enhancement.

2.2.2. Injection-locked WuRx



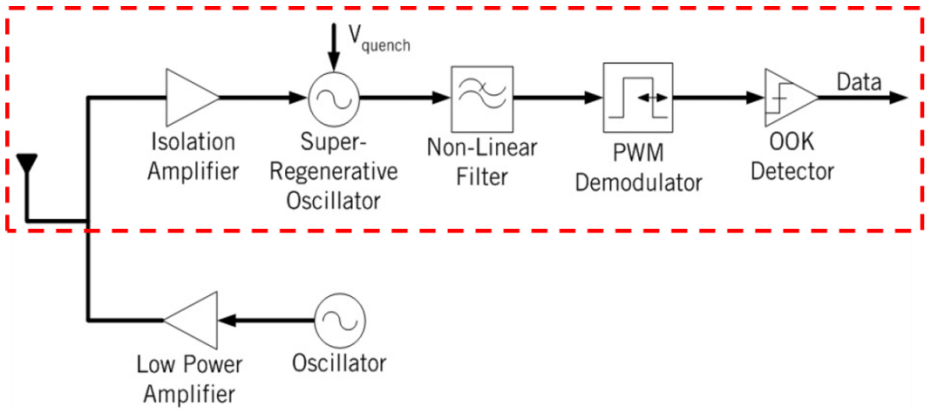
* H.Yan, et. al, "An Ultra-Low-Power BPSK Receiver and Demodulator Based on Injection-Locked Oscillators", *IEEE TMTT*, 2011.

Figure 2.6. An injection-locked based wake-up receiver block diagram.

Injection-locked WuRx architectures are designed for digital Frequency-Shift Keying (FSK) and Phase-Shift Keying (PSK) modulations. The goal of these architectures is to detect the incoming wake-up signals by feeding the RF input signal into the local ring oscillators as injection locked frequency. An example of this architecture is depicted in Figure 2.6 [Yan]. The WuRx consists of a front-end band-pass filter, a RF splitter to differentiate each of the

carrier frequencies (for FSK modulated signals) or phases (for PSK modulated signals), an injection-locked oscillator on each signal-path, and a baseband digital logic circuitry. Since the power of the injection-locked ring oscillators is directly proportional to the desired RF injection frequency, optimum power consumption is obtained by minimizing the RF frequency [Cho]. In this case, the receiver sensitivity is not limited by the noise figure or by the bandwidth; it is principally determined by the locking range of the oscillators [Bae01]. An extended technique using double FSK modulation and Injection-Locked Frequency Divider (ILFD) can allow sensitivity and CIR enhancement [Bae02]. In summary, injection-locked WuRxs proves moderate sensitivity performances ($S_{min} = -73dBm$ [Bae01]) at the price of high power consumption and external front-end high-Q band-pass filters.

2.2.3. Super-regenerative WuRx



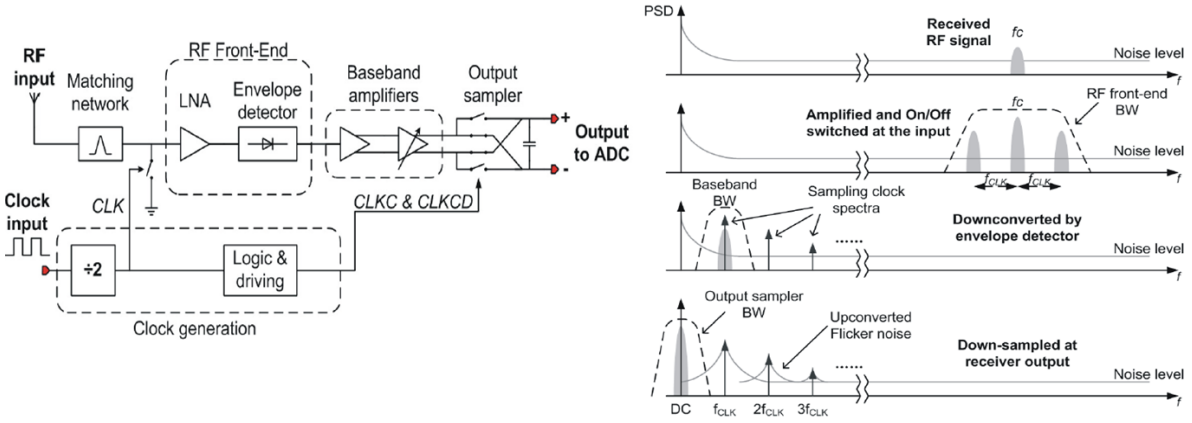
* B. Otis, et. al, "A 400 μW-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks", *IEEE (ISSCC)*, 2005.

Figure 2.7. A super-regenerative based wake-up receiver block diagram.

Super-regenerative WuRx configurations are used for OOK-AM RF modulated signals [Ayers] [Bohorquez] [Petäjäjärvi] [Vidojkovic]. The key idea behind these architectures is to use a duty-cycled (quench node) detector oscillator to store the received RF signal energy in the tank of the oscillator, and periodically dissipate it through the baseband amplification stages (non-linear filter) (Figure 2.7) [Otis01]. The periodical behavior of the oscillator allows for energy efficient performance. The higher the Q-factor resonator element employed for the oscillator, the lower the duty-cycle ratio required. Usually, these configurations use external high-Q resonators, such as the Bulk Acoustic Wave (BAW) used in [Otis01]. Thanks to the reduced bandwidth provided by these resonators, excellent sensitivities below

$-100dBm$ can be achieved. While these architectures provide very good sensitivity, they present, nevertheless, power consumption levels above $200\mu W$ and require high-Q bulky and costly external resonators.

2.2.4. Sub-sampling WuRx



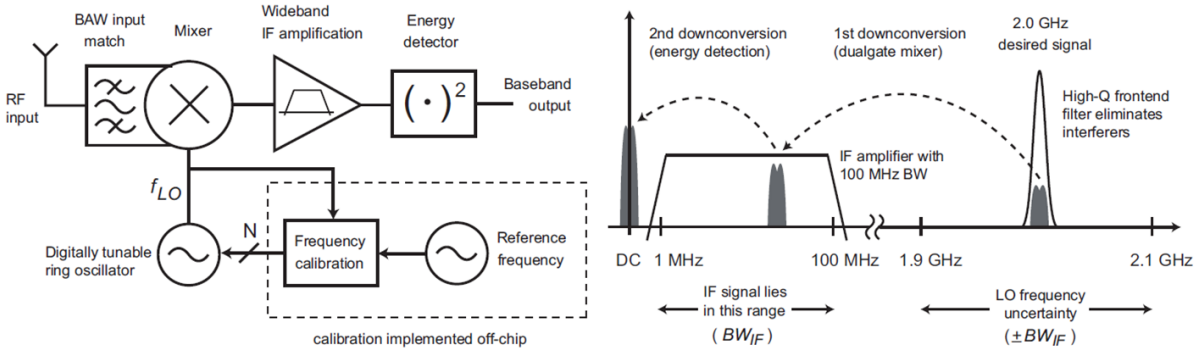
* X. Huang, et. al, "A 2.4GHz/915MHz 51µW Wake-Up Receiver with Offset and Noise Suppression", IEEE ISSCC, 2010.

Figure 2.8. A sub-sampling based wake-up receiver block diagram and frequency plan.

Sub-sampling based WuRxs work with OOK-AM RF modulations. Their main objective is to eliminate power hungry high frequency local oscillators and replace them with low frequency oscillators working at frequency ranges between $10MHz$ [Huang03] and $200MHz$ [Moazzeni02]. Shown in Figure 2.8, is an example of sub-sampling based WuRx [Huang03]. The RF input signal is first band-pass filtered and then sampled by the CLK signal. At this point (at the LNA input) the desired signal is only modulated by CLK, but it is stills an RF signal with three fundamental tones (ω_{RF}, $\omega_{RF}+\omega_{CLK}$ and $\omega_{RF}-\omega_{CLK}$). Note that the symmetrical behavior of this modulation leads to a two-image frequencies drawback. Very high-Q RF BPFs are required in order to correctly attenuate interferers centered at these two frequencies ($\omega_{IM1}=\omega_{RF}+\omega_{CLK}$ and $\omega_{IM2}=\omega_{RF}-\omega_{CLK}$). Next, the signal is amplified by the LNA and then self-mixed by an envelope detector. At this point the desired signal has two frequency components one at DC and one at ω_{CLK}. In order to avoid the self-mixing DC flicker noise and DC voltage offsets problems, only the frequency component centered at ω_{CLK} is amplified and then directly downconverted to DC by mixing with the same CLK frequency. For further detail, the reader is kindly invited to refer to [Huang02]. In the case of these architectures, the CLK signal needs to provide low phase noise

performances in order to avoid signal drown by reciprocal mixing. In summary, sub-sampling architectures are well suited for ULP WuRx based applications demanding high sensitivity. Their main strength focuses on the elimination of high frequency LOs. However, four main drawbacks can be listed: first, its high-Q front-end BPF dependence; second, the generation of a dual RF image frequency; third, the large in-band noise found at the envelope detector input, which may limit, somehow, the sensitivity of the system; fourth, the low phase noise CLK requirements for avoiding signal drown by reciprocal mixing.

2.2.5. Uncertain-IF WuRx



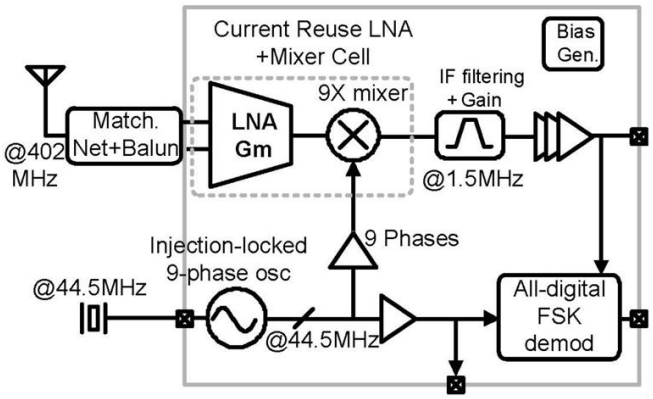
* N. Pletcher, et. al, "A 2 GHz 52µW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture", IEEE ISSCC, 2008.

Figure 2.9. An uncertain-IF based wake-up receiver block diagram and frequency plan.

The uncertain-IF WuRx architectures target RF input signals with OOK-AM modulation [Richmond]. An example of these configurations is shown in Figure 2.9 [Pletcher01]. The innovative feature of uncertain-IF architecture is the unlocked low accuracy LO. In this way, power hungry PLLs can be eliminated and only unlocked local oscillators are used. These configurations are usually implemented with front-end RF high-Q RF resonator filters for image and interferer rejection (in this case a Bulk Acoustic Wave (BAW) resonator). The inaccuracy of the local oscillator generates an uncertain IF signal when mixing with the RF input desired signal. At the IF-band, the signal is wide-band amplified and then downconverted to the baseband by self-mixing through an envelope detector. Note that these topologies usually avoid RF LNAs for power optimization. Periodical LO frequency calibrations may be introduced to compensate temperature variation. The duty-cycled behavior of this frequency calibration block should not increase the overall average power consumption of the system [Pletcher01]. Despite good LP performance, uncertain-IF

find their sensitivity limited because of two reasons: first, the non-use of LNAs, which degrades the noise on the following stages; and second, the wide IF bandwidth presented at the input of the envelope detector, which limits the effective integrable sensitivity bandwidth.

2.2.6. Low-IF WuRx



* J. Pandey, et. al, "A 120μW MICS/ISM-Band FSK Receiver with a 44μW Low-Power Mode Based on Injection-Locking and 9x Frequency Multiplication", *IEEE ISSCC*, 2011.

Figure 2.10. A low-IF based wake-up receiver block diagram.

Low-IF WuRxs are characterized by their performance in generating accurate high frequency LO signals. The accuracy of the LO generates a precise downconverted IF signal, allowing aggressive IF-bandwidth reduction for sensitivity and interference rejection enhancement. The nature of this architecture enables the possibility of receiving OOK-AM or FSK modulated signals according to the application. Figure 2.10 presents an example of a low-IF WuRx block diagram [Pandey]. At the input, an external BPF matching network followed by an LNA provides selectivity and low noise amplification. Here, the LNA and the mixer are designed as stacked current reuse devices for energy saving. The LO signal is generated from a very high-Q ($\sim 10^5$) crystal resonator by injection-locking. A chain of frequency multipliers (ring oscillators) generates the desired high frequency LO signal. Note that the received RF frequency is only at $402MHz$. If higher RF signal reception is required, the power consumption of the ring oscillators would exceed the power budget of the entire receiver. At the baseband the IF desired signal is amplified within a reduced bandwidth and then digital FSK demodulated. Other techniques, such as high-Q LC resonators [Cook01] [Bae03] or ULP PLL systems [Drago], are implemented to generate the accurate LO signal.

In summary, despite good sensitivity, low-IF architectures present poor power performances because of the expensive energy requirements to generate an accurate LO frequency, which in most cases requires external bulky components such as crystals or high-Q inductors.

2.3. Chapter conclusions

This chapter presents a review of the principal considerations of ULP WuRx intended for dense node WSN applications. In the first part, a complete analysis highlights the principal WuRx considerations allowing low power consumption, high sensitivity and strong immunity against interference. Optimization of these three specifications is obtained through the mutual effort at several technology layers, receiver architecture design and system design, resulting in a trade-off between power, noise and physical volume occupied.

The second part of this chapter provides a detailed description of the strengths and the limitations of the principal sub-$1mW$ state-of-the-art WuRx architectures.

Architecture	**Minimum power consumption** ($\boldsymbol{\mu W}$)	**Minimum sensitivity** ($\boldsymbol{dBm}$)	**CIR** ($\boldsymbol{dB}$)
Envelope detection	0.098 $S = -41dBm$ @ $100kb/s$ [Roberts]	-73 @ $200kb/s$ and $P_{avg} = 8.5\mu W$ [Yoon] *	-19 @ $5MHz$ offset [Huang01]
Injection-locked	37.5 ($f_{RF} = 45MHz$) $S = -63dBm$ @ $200kb/s$ [Cho]	-73 ($f_{RF} = 920MHz$) @ $5Mb/s$ and $P_{DC} = 420\mu W$ [Bae01]	$+9$ @ $5MHz$ offset -17 @ $100MHz$ offset [Bae01]
Super-regenerative	215 $S = -86dBm$ @ $250kb/s$ [Ayers]	-100.5 @ $5kb/s$ and $P_{DC} = 450\mu W$ [Otis01]	N/A
Sub-sampling	28 $S = -70dBm$ [Moazzeni02]	-86 @ $10kb/s$ and $P_{DC} = 123\mu W$ [Huang02]	N/A
Uncertain-IF	52 $S = -72dBm$ @ $100kb/s$ [Pletcher01]	-72 @ $100kb/s$ and $P_{DC} = 52\mu W$ [Pletcher01]	N/A
Low-IF	44 $S = -70dBm$ @ $200kb/s$ [Pandey]	-90 @ $200kb/s$ and $P_{DC} = 120\mu W$ [Pandey]	N/A

* Average power with 0.6% duty-cycle.

Table 2.2. Principal performances of wake-up receivers proposed on the State-of-the-Art.

Table 2.2 presents the most relevant figures for the different WuRx architectures. Generally speaking, injection-locked and super-regenerative architectures seem to be obsolete solutions for WuRx based WSN applications. Despite their moderate sensitivity performance, these solutions present high power consumption levels which are not in line with respect to the WuRx specifications established in this thesis.

On the other hand, envelope detection architectures present the best energy performances over all other configurations. They are able to achieve power levels below $100nW$ [Roberts]. However, due to their homodyne behavior and its large integrable bandwidth, their sensitivity hardly exceeds $-40dBm$ (for this levels of power consumption). In terms of interference rejection, a two-tone envelope detection configuration can be used to present interference rejection [Huang01]. However, this solution requires the development and the implementation of dedicated transmitters for the WuRxs, resulting in a higher bill of materials and a higher WSN system power consumption.

In terms of sensitivity, the super-regenerative configurations present the best behavior revealing sensitivity levels below $-100dBm$ [Otis01]. The main drawback of these topologies is their high power levels ($> 215\mu W$ [Ayers]), dedicated to the generation of accurate LO frequencies. Better power-sensitivity performance can be obtained by using low-IF architectures [Pandey]. Sub-sampling architectures appears also as an attractive LO energy efficient solution requiring a low frequency clock with orders of magnitude below the RF frequency. However, these configuration are subject to the use of external high-Q resonators in order to provide appropriate filtering at the RF signal-path and accurate clock signal at the LO signal path. On the other hand, if a LP solution minimizing the uncertainty range of the LO frequency is achieved, uncertain-IF based WuRxs may be considered as well-suited architectures for WSN applications. Therefore, uncertain-IF and low-IF architectures are then the best candidates to equally improve the power, the sensitivity and the CIR performances. According to this thesis, the ideal WuRx architecture should combine these two configurations to achieve the targeted specifications presented in Table 2.1. Apart from digital node ID coding, further research should be dedicated to developing novel strategies for providing high immunity against interferers, without requiring any costly and bulky external high-Q resonator.

Chapter 3

Ultra-Low Power N-Path Passive Mixer Principles

The architecture review that has been presented in the previous chapter highlighted the main challenges on ULP wake-up receivers. Apart from the low power requirements, the principal target of WuRxs is to provide highest sensitivity possible. Previous architectures attained these performances by using high-Q external resonators, placed at the RF front-end path as high Q-factor filtering element or at the LO path as high Q-factor resonator tank. However, the use of these bulky and costly external resonators implies high manufacturing cost per device, and this is not compatible with the philosophy of these devices that should be lower cost than a postal stamp, hence deployable in a large number for dense networks.

This chapter presents the analysis of compact and low cost ultra-low power high-Q filters. In particular, the optimization of ULP 2-Path Passive Mixers (2-PPM), dedicated to WuRxs is discussed. The principles of different 2-Path Passive Mixer (2-PPM) architectures and configurations targeting high-Q band-pass filtering are developed in three main sections: the Single-to-Differential 2-PPM (SD-2PPM), the fully Differential 2-PPM (DD-2PPM) and the parallel 2-PPM.

Later a qualitative description of the different 2-PPM configurations and their correspondent optimum IC design implementations and applications are discussed.

3.1. N-Path Passive Mixers

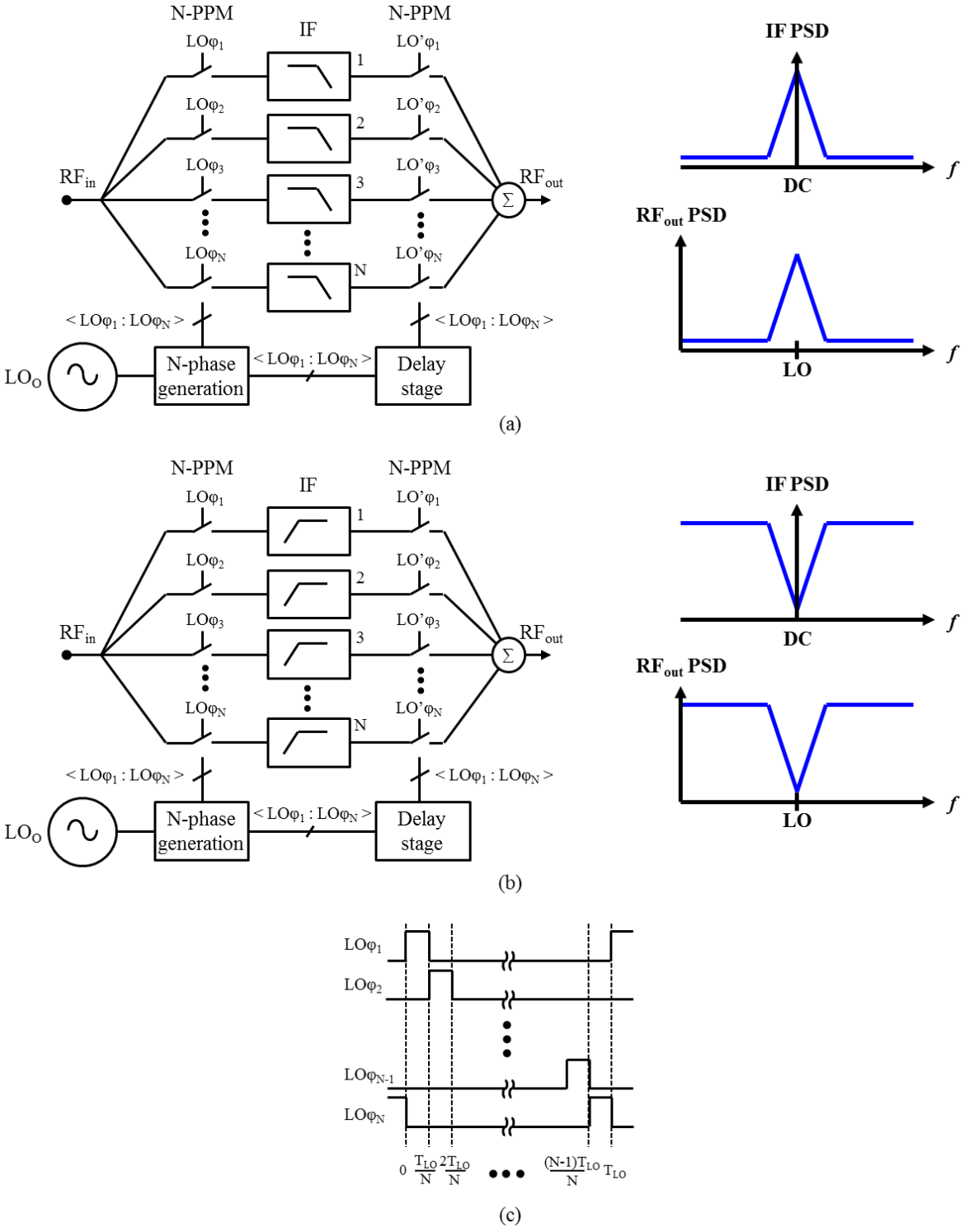


Figure 3.1. N-path passive mixer (a) band-pass filter and (b) notch filter configurations. (c) N-path mixer clock distribution.

The theory of N-path narrow band-pass filters has been first developed by N.Y. Barber in 1947 [Barber], and, several years after, revisited by L.E. Franks, in 1960 [Franks] and by D.C. von Grunigen, in 1983 [Grunigen]. This theory is based on a double modulation in which a Low-Pass Filter (LPF) is placed in between two N-path passive mixers, each one modeled as a parallel switch network (Figure 3.1.a), driven by a non-overlapping N-phase LO signal generated from a global clock LO_O. Here, each LO phase has an on-state duty-cycle interval time equal to the LO cycle-period T_{LO} over the number of N paths (T_{LO}/N) (Figure 3.1.c). The first mixer downconverts the input RF signal to the IF frequency by mixing with the LO $\left(\omega_{IF} = \omega_{RF,in} - \omega_{LO}\right)$. At the IF-band the signals are low-pass filtered through identical low-pass filters placed in each path. The resulting IF signals are upconverted back to RF by mixing with the LO through the second mixer $\left(\omega_{RF,out} = \omega_{IF} + \omega_{LO}\right)$. In order to provide isolation between the two switches of each path, a delay stage is introduced at the LO signal-path to drive the second N-path mixer. The resulting output frequency response presents a narrow Band-Pass Filter (BPF) centered at the LO frequency. This BPF response is the IF LPF frequency centered at DC translated to RF. This theory can be extended to narrow-band notch filters by replacing the LPF by a High-Pass Filter (HPF) (Figure 3.1.b) [Darabi] [Madadi] [Ghaffari01].

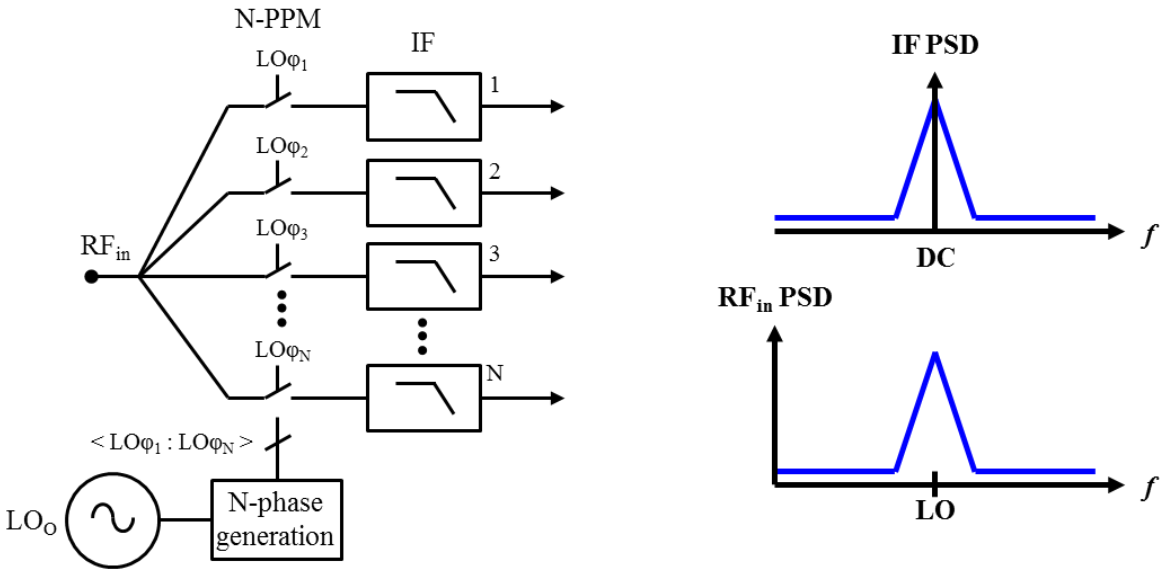


Figure 3.2. Single mixer N-path BPF configuration and respective frequency responses.

Ideal N-PPMs are defined by the combination of N passive paths connected in a parallel configuration. Each path is composed of an ideal switch that allows current to flow in both directions: from input to output and from output to input. The transparency of passive mixers

offers a bidirectional response between the high-frequency input and the downconverted output. As a result, the BPF response can be obtained on the input node by a single N-PPM as shown in Figure 3.2. This effect is understood as an impedance frequency translation from the low-frequency IF mixer output node to the high-frequency RF mixer input node.

Recently, the flexibility of the N-PPM has been widely studied through different architectures for diverse types of wireless telecommunication applications. Generally, three types of N-path mixer configurations have been proposed according to the number of paths: 2-PPM, 4-PPM and 8-PPM. These architectures take benefit of the N-path mixer BPF response to provide high interferer rejection while avoiding external high-Q piezoelectric resonators. In the context of standardized radio communications, addressed so far with such techniques, the design effort has been principally targeted at linearity and noise optimization. High IIP3 mixer linearity has been obtained by driving the passive mixers with large swing LO signals provided from high voltage supplies [Soer01] [Andrews02] [Andrews03]. Low noise figure performance has been achieved by increasing the number of paths and by using active feedback loop Frequency-Translational Noise-Cancelling (FTNC) techniques, implemented by parallel N-PPM configurations placed at the receiver front-end [Murphy] [Fujian] [Hedayati]. However, despite their performance, these active feedback loops are not suitable for ULP applications. Furthermore, by increasing the number of paths the clock circuitry complexity is increased, therefore degrading the overall system power consumption. Typically, in IC design the N-phase LO signal is generated from a global LO_O clock (see Figure 3.1) by using digital frequency dividers. In this case, the LO_O frequency is directly proportional to the number of paths used $\left(f_{LO,0} = Nf_{RF}/2\right)$. Hence, for a 4-PPM and a 8-PPM the respective global LO_O frequency is $2f_{RF}$ and $4f_{RF}$. This behavior can strongly affect the system power consumption, especially in the case of digital circuits (ring oscillator), for which the power consumption is directly proportional to their frequency of operation. For all these high-performant N-PPM based receivers the power consumption is set above $10mW$. Taking into account the high-frequency LO_O generation requirement, the digital circuitry required to generate the N-phase LO and the buffer stages required to drive each mixer switches, we can realize that N-PPM power consumption optimization is obtained by minimizing the number of paths.

	[Molnar]	[Cook01]
Architecture	Heterodyne RX	Low IF RX
RF input	Single-ended	Differential
N-PPM architecture	2-PPM (floating C_{IF})	Reconfigurable 2-PPM and 4-PPM (floating C_{IF})
f_{RF} (GHz)	0.82 – 0.97	1.95 – 2.38
LO_O	f_{RF}	f_{RF}
NF (dB)	12	5.1 – 11.8
IIP3 (dBm)	N/A	-7.5
Power supply (V)	3	0.36 – 0.6
Power consumption (mW)	1.2	0.36 – 1.45

Table 3.1. Ultra-low power N-PPM based receivers.

Ultra-low power N-PPM based heterodyne receivers were proposed in [Molnar] and [Cook02] (Table 3.1). Their main advantage concerns the effective LO_O frequency, which in this case, is equal to that of the desired RF signal. This allows significant energy reduction showing power consumption levels on the order of $1mW$, by avoiding any complex digital circuitry and by minimizing the number of buffers required to drive the N-path switches. In the case of [Molnar], a 2-PPM was implemented with an LO signal generated from a LC resonator. On the other hand, [Cook02] proposed a reconfigurable LC quadrature topology able to generate single-phase or quadrature LO signals according to the N-PPM configuration required (2-PPM or 4-PPM). Both receivers used a N-PPM architecture with a *floating* IF capacitor connected between the differential mixer outputs. The main disadvantage of this floating architecture concerns the input impedance and the voltage frequency response which depends on the LO frequency. Here, the equivalent mixer input impedance is described by the frequency translate N-path mixer behavior but also by the equivalent LO frequency dependent switched-capacitor impedance $Z_{SC} = 1 / f_{LO} C_{IF}$ [Razavi01]. This effect may represent a drawback for wideband passive mixer-first receiver applications where the LO frequency may vary by several MHz, thus degrading the antenna matching impedance and therefore the mixer frequency output voltage.

From this overview, we can conclude that 2-path passive mixers are the most suitable N-PPM structures for ULP applications. These simple architectures minimize the required effective LO_O clock frequency, avoid any digital circuitry for the N-phase LO generation and

minimize the number of mixer driving buffers. This chapter presents the 2-PPM theory indicating their principal advantages concerning their low power consumption and their passive voltage gain response, but also highlighting their two main drawbacks concerning the RF input phase shift dependence for zero-IF structures and the minimum switch resistance required to ensure impedance matching to the RF input. Indeed, unlike the 2-PPM configuration, the 4-PPM and the 8-PPM structures do not suffer from these two drawbacks given their orthogonal polyphase behavior. In this section three 2-PPM configurations suitable for ultra-low power applications are described: The Single-to-Differential 2-PPM (SD-2PPM), the fully differential 2-PPM (DD-2PPM) and the parallel 2-PPM.

3.2. Single-to-Differential 2-Path Passive Mixer (SD-2PPM)

The goal of this section is to provide an analysis of the SD-2PPM configuration through the description of three aspects: the input impedance, the frequency response and the noise. In the first part, the Linear Time Variant (LTV) 2-path mixer is modeled as a zero-IF Linear Time Invariant (LTI) system. This LTI model allows us to have a simple interpretation of the passive mixer input impedance highlighting the key electrical parameters to provide impedance matching to the RF input. This model is then extended to heterodyne architectures to characterize their input impedance as a function of the downconverted IF frequency. In the second part, the SD-2PPM frequency response is analyzed. This characterization provides an overview of the strengths and the limitations of these passive mixer structures from the stand point of voltage gain and filtering robustness against interferers. Finally, the SD-2PPM noise figure analysis is provided.

3.2.1. SD-2PPM impedance analysis

Figure 3.3.b shows the simplified SD-2PPM model with its respective clock distribution (Figure 3.3.a). The RF input is represented by an RF voltage source with a source impedance in series (the antenna impedance), modeled as a purely resistive impedance: $|Z_s| = |Z_a| = |R_a + jX_a| = R_a$ with the assumption that $X_a \approx 0$. Each path is implemented by a CMOS switch transistor, so far modeled as an ideal switch connected with the on-resistance in series

(switch resistor R_{sw}), and a *grounded common-mode* load $R_{IF}C_{IF}$ low-pass filter. In a first approach, the CMOS transistor parasitic capacitances are neglected. An analysis taking into account these parasitic capacitances is provided in section 3.4.

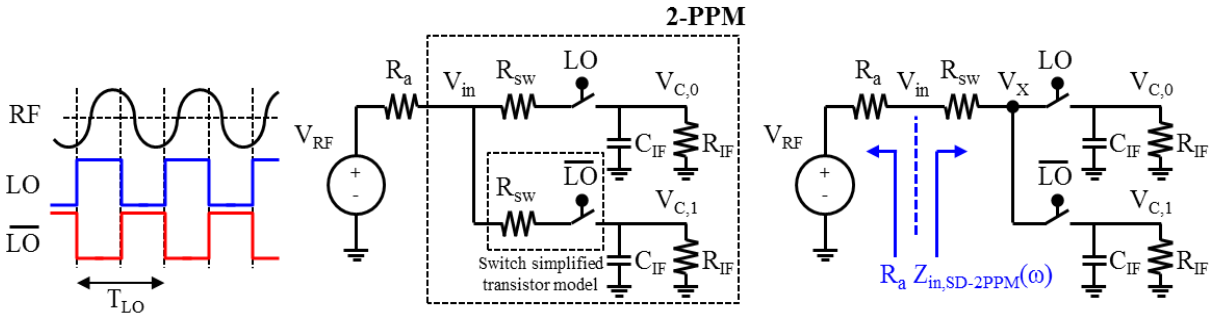


Figure 3.3. (a) Non-overlapping 50% LO square driving waveform with $\omega_{RF} = \omega_{LO}$. (b) Simplified single-to-differential 2-path passive mixer model. (c) Equivalent single-to-differential 2-path passive mixer circuit.

Assuming an LO square wave signal defined from 0 to A_{LO} with 50% duty-cycle, the LO Fourier series is defined as

$$V_{LO}(t) = \frac{1}{2} + \sum_{n=1,3,5\ldots}^{\infty} \frac{2A_{LO}}{n\pi} \sin\left(\frac{n\pi}{2}\right) cos(n\omega_{LO}t) \tag{3.1}$$

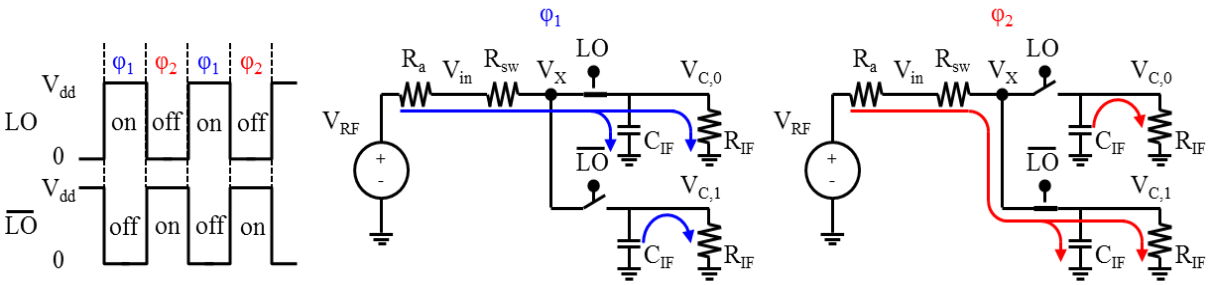
Where ω_{LO} is the carrier frequency and n represents the LO odd harmonics. This analysis assumes a sinusoidal RF input voltage defined by equation 3.2, where ω_{RF} is the RF carrier frequency, $A_{RF}(t)$ is the time-variant amplitude and $\varphi_{RF}(t)$ is the time-variant phase shift with respect to the LO. The following development assumes the time-variation of $A_{RF}(t)$ and $\varphi_{RF}(t)$ relative slow compared to the LO cycle-period. These two quantities are hereinafter considered as constant quantities.

$$V_{RF}(t) = A_{RF}(t)Cos(\omega_{RF}t + \varphi_{RF}(t)) \tag{3.2}$$

Metric 1- Zero-IF SD-2PPM input impedance:

For the zero-IF input impedance analysis we consider $\omega_{RF} = \omega_{LO}$. Assuming a non-overlapping 50% duty-cycled square LO waveform and considering the fact that each path is switched one after the other, we can consider the RF input as being always connected to at least one of the paths at any given time. Figure 3.3.c illustrates the equivalent circuit model representing the previous behavior, where each path's switch resistor is modeled as a global R_{sw} directly connected to the antenna, followed by the ideal path switches and their corresponding LPF network.

For this 2-path mixer architecture, each m-path $(m = 0,1)$ works with two clock phases (Figure 3.4). During the on-state (Figure 3.4.b), the RF input current charges the IF capacitor while a fraction of this current flows to ground through the corresponding IF resistor. When the switch is turned-off (Figure 3.4.c), part of the charge stored on the IF capacitor is lost through the IF resistor.



(a) (b) (c)

Figure 3.4. (a) Non-overlapping 50% LO square driving waveform. (b) SD-2PPM charge distribution phase one (c) SD-2PPM charge distribution phase two.

To ensure steady-state mixing behavior, the time constants $(R_a + R_{sw})C_{IF}$ and $R_{IF}C_{IF}$ must be significantly larger compared to the LO time period (T_{LO}) [Soer02]. These conditions set two minimum values for the IF capacitors.

$$C_{IF} \gg \frac{T_{LO}}{2\pi R_{IF}} \tag{3.3}$$

$$C_{IF} \gg \frac{T_{LO}}{2\pi(R_a + R_{sw})} \tag{3.4}$$

Assuming the previous time constant conditions are satisfied, the voltage $V_{c,m}$ held by each IF capacitor during a complete LO cycle period can be considered as being constant for a zero-IF downconversion system in the steady-state. As a result, the average IF resistor current provided by the RF input signal during the on-state ($I_{R_{IF,avg,on,m}}$), equals the average IF resistor current generated by the IF capacitor during the discharge off-state ($I_{R_{IF,avg,off,m}}$).

$$I_{R_{IF,m,avg,on}} = I_{R_{IF,m,avg,off}}$$

$$\frac{V_{c,m}}{R_{IF}} = \frac{2}{T_{LO}} \int_{\frac{T_{LO}}{2}(m-\frac{1}{2})}^{\frac{T_{LO}}{2}(m+\frac{1}{2})} I_{C_{IF}}(t)dt \qquad m = 0,1. \tag{3.5}$$

Hence, the on-state charge distribution generated during half an LO time period ($T_{LO}/2$) for each mixer path can be defined by the charge conservation theorem, which involves an equality between the RF input charge $Q_{RF,m}$ and the sum of the charge injected into the IF capacitor $Q_{C_{IF,m}}$ and the charge drained to ground by the IF resistor $Q_{R_{IF,m}}$.

$$Q_{RF_m} = Q_{C_{IF,m}} + Q_{R_{IF,m}}$$

$$= \int_{\frac{T_{LO}}{2}(m-\frac{1}{2})}^{\frac{T_{LO}}{2}(m+\frac{1}{2})} \frac{V_{RF}(t) - V_{c,m}}{R_a + R_{sw}} dt = \int_{\frac{T_{LO}}{2}(m-\frac{1}{2})}^{\frac{T_{LO}}{2}(m+\frac{1}{2})} I_{C_{IF}}(t)dt + \frac{V_{c,m}T_{LO}}{2R_{IF}} = \frac{V_{c,m}T_{LO}}{R_{IF}} \tag{3.6}$$

Substituting equation 3.2 in the equation above, the voltage across each IF capacitor is

$$V_{c,m} = \frac{2}{\pi}\left[\frac{R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF} Cos(m\pi + \varphi_{RF}) \tag{3.7}$$

This result give the zero-IF SD-2PPM voltage response with respect to the RF phase shift φ_{RF}. As we can realize, for $\varphi_{RF} = 0$ the voltage across the capacitor is maximized. However, as φ_{RF} shifts towards $\pm\pi/2$, the baseband signal is attenuated until complete cancellation at $\varphi_{RF} = \pm\pi/2$. This effect is very important and reflects the first of the two major 2-PPM drawbacks with respect to the 4-PPM and 8-PPM architectures, which do not present this problem given their high number of polyphase N-paths that ensure the signal reception for any RF phase shift value. This behavior makes 2-PPMs not suitable for zero-IF receiver architectures unable to provide RF signal phase control.

In order to reach our targeted LTI SD-2PPM model, we continue our analysis by considering the model illustrated in the Figure 3.3.c. From this circuit model, the LTV antenna RF input current is defined as a function of the RF input voltage and the virtual voltage V_x.

$$I_{A,LTV}(t) = \frac{V_{RF}(t) - V_x(t)}{R_a + R_{sw}} \tag{3.8}$$

In the case of 2-PPMs, the virtual node V_x tracks the value held by each of the capacitors at each respective half period. Since the voltages across the IF capacitors are considered as being constant and different from each other, the virtual voltage V_x describes a square waveform centered at ω_{LO}. Considering $\omega_{RF} = \omega_{LO}$, the zero-IF fundamental component of the virtual V_{x0} square waveform is defined by the upconverted multiplication between the differential baseband voltage average $(V_{c,0} - V_{c,1})/2$ and the fundamental Fourier series square LO component.

$$V_{x0,fund}(t) = \frac{(V_{c,0} - V_{c,1})}{2} V_{LO}(t)$$

$$= \left[\frac{\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}[\cos(\omega_{LO}t + \varphi_{RF}) + \cos(\omega_{LO}t - \varphi_{RF})] \tag{3.9}$$

Where $\gamma = 2/\pi^2 \approx 0.203$. Equation 3.9 is in line with the previous $V_{c,m}$ analysis development (equation 3.7) for which we had demonstrated that the voltages across the baseband IF capacitors were maximized for $\varphi_{RF} = 0$ and zeroed for $\varphi_{RF} = \pm\pi/2$. Taking into account this result, the fundamental component of the RF input current is written as

$$I_{A,fund,LTV}(t) = \frac{V_{RF}(t) - V_{x0,fund}(t)}{R_a + R_{sw}}$$

$$= \frac{A_{RF}\{[2(R_a + R_{sw}) + R_{IF}(1-\gamma)]\cos(\omega_{LO}t + \varphi_{RF}) - \gamma R_{IF}\cos(\omega_{LO}t - \varphi_{RF})\}}{(R_a + R_{sw})[2(R_a + R_{sw}) + R_{IF}]} \tag{3.10}$$

This result indicates the influence of the LO spectrum whose energy is spread onto the RF input signal path. Taking into account the mixer frequency translation, this LO energy loss can be modeled by a baseband *virtual shunt resistor* (R_{sh}), *representing the power lost due to upconversion by LO harmonics*, through the switches, to the RF input [Andrews01].

This assumption can be demonstrated by considering the limit values of the fundamental RF input current where $R_{IF} \to 0$ and $R_{IF} \to \infty$. Note that this development is valid for the entire LO spectrum indicating that this virtual shunt resistor is also defined at every LO harmonics. This point is analyzed right after our LO fundamental component development.

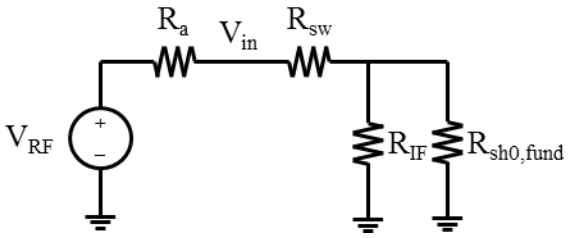


Figure 3.5. Antenna and linear time-invariant passive mixer model for $\omega_{RF} = \omega_{LO}$.

Making the analogy with a fully resistive circuit, the zero-IF SD-2PPM can be modeled as a Linear Time-Invariant (LTI) circuit as shown in Figure 3.5. Note that this LTI model is only valid for zero-IF SD-2PPMs where $\omega_{RF} = \omega_{LO}$ and can be extended to every LO harmonics. In order to determine the expression for the virtual shunt resistance we derive the LTI RF input current

$$I_{A,fund,LTI}(\omega_{LO}) = V_{RF}(\omega_{LO}) \frac{R_{IF} + R_{sh,fund}}{R_{IF}(R_a + R_{sw}) + R_{sh,fund}(R_a + R_{sw}) + R_{sh,fund}R_{IF}} \tag{3.11}$$

Equalizing both LTV (equation 3.10) and LTI RF input currents (equation 3.11), the virtual shunt resistance is

$R_{sh0,fund}$

$$= \frac{\gamma(R_a + R_{sw})R_{IF}[\cos(\omega_{LO}t + \varphi_{RF}) + \cos(\omega_{LO}t - \varphi_{RF})]}{[(R_a + R_{sw})(2 - \gamma) + R_{IF}(1 - \gamma)]\cos(\omega_{LO}t + \varphi_{RF}) - \gamma(R_a + R_{sw} + R_{IF})\cos(\omega_{LO}t - \varphi_{RF})} \tag{3.12}$$

This equation demonstrates that maximum virtual shunt resistance is obtained for an RF phase shift equal to zero. As φ_{RF} shifts towards $\pm\pi/2$, $R_{sh0,fund}$ is degraded until complete cancellation at $\varphi_{RF} = \pm\pi/2$.

In order to have a first approach of the zero-IF SD-2PPM input impedance, let's assume $\varphi_{RF} = 0$ and let's calculate its maximum input impedance. Considering equations 3.7 and

3.12, the respective maximum value for the zero-IF differential baseband signal $\left(V_{IF0} = V_{C0,0} - V_{C0,1}\right)$ and the virtual shunt resistance is

$$V_{IF0,max}(\varphi_{RF} = 0) = \frac{4}{\pi}\left[\frac{R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right]A_{RF} \tag{3.13}$$

$$R_{sh0,fund,max}(\varphi_{RF} = 0) = \frac{2\gamma(R_a + R_{sw})R_{IF}}{2(R_a + R_{sw})(1-\gamma) + R_{IF}(1-2\gamma)} \tag{3.14}$$

Replacing $R_{sh0,fund,max}$ on the LTI model, antenna input impedance matching $\left(Z_{in,SD-2PPM} = R_a\right)$ is provided for

$$R_{IF0,match,max}(\varphi_{RF} = 0) = \frac{2R_a^2 - 2R_{sw}^2}{R_a(4\gamma - 1) + R_{sw}} \tag{3.15}$$

Equation 3.15 indicates that $R_{IF0,match,max}$ is not defined $\left(R_{IF0,match,max} = \infty\right)$ for $R_{sw} = R_{sw,min} = (1-4\gamma)R_a \approx 0.19R_a$ and presents positive values $\left(R_{IF0,match,max} \geq 0\right)$ for the switch resistance range and the virtual shunt resistance range specified in equations 3.16 and 3.17. The minimum switch resistance $\left(R_{sw,min} \approx 0.19R_a\right)$ describes the second major ULP 2-PPM drawback with respect to the 4-PPMs and the 8-PPM structures. Indeed, in the case of the 2-PPM the maximum virtual shunt resistance value for which $\varphi_{RF} = 0$ and $R_{IF0,match,max} = \infty$ is $R_{sh,2PPM,fund,max} \approx 0.68\left(R_a + R_{sw,min}\right) \approx 0.81R_a$. On the other hand, for the four and height N-PPM, the maximum shunt resistance for which $R_{IF} = \infty$ is respectively $R_{sh,4PPM,fund,max} \approx 4.3(R_a + R_{sw})$ and $R_{sh,8PPM,fund,max} \approx 18.9(R_a + R_{sw})$ [Andrews01]). This behavior enables the possibility in these polyphase architectures to ideally reduce the switch resistance down to zero, while still presenting matching to the RF input by the combination of the equivalent parallel baseband $R_{IF0,match}||R_{sh,fund}$ resistance. This drawback inherently affects the 2-PPM mixer performance in terms of out-of-band interference rejection, voltage frequency response and noise figure. These points will be discussed in sections 3.2.2 and 3.2.3. However, if some extra power budget is available, this disadvantage may be overcome by the implementation of active feedback circuits enabling the possibility of generating the required negative IF resistance. Since the target of this study focuses on ultra-low power 2-PPM architectures, this solution is discarded, limiting our analysis to only positive passive IF resistance values.

$$0.19R_a \lesssim R_{sw}(\varphi_{RF} = 0) \leq R_a \tag{3.16}$$

$$0.68(R_a + R_{sw}) \gtrsim R_{sh0,fund,max}(\varphi_{RF} = 0) \geq 0 \tag{3.17}$$

From the foregoing LTI model impedance analysis, the maximum zero-IF SD-2PPM input impedance, can be described as a function of a simple resistive network

$$\begin{aligned} Z_{in0,fund,max,SD-2PPM}(\omega_{LO}) &= R_{in0,fund,max,SD-2PPM}(\omega_{LO}) \\ &= R_{sw} + R_{sh0,fund,max}(\varphi_{RF} = 0)||R_{IF} \\ &= \frac{2R_{sw}(R_a + R_{sw}) + R_{IF}(2\gamma R_a + R_{sw})}{2(R_a + R_{sw}) + R_{IF}(1 - 2\gamma)} \end{aligned} \tag{3.18}$$

Figure 3.6 presents the zero-IF SD-2PPM RF input impedance matching IF resistance (blue lined), the virtual shunt resistance (red lined) and the equivalent SD-2PPM input impedance (yellow lined), evaluated at ω_{LO} as a function of the switch-to-antenna resistance ratio. Simulation results are realized using Periodical Steady State (PSS) analysis, including the MOS transistor model and an ideal square wave LO as defined in equation 3.1. Positive IF resistance values are defined between $R_{sw,min}$ and $R_{sw,max}$ as specified in equation 3.16. The function describes an asymptotic curve centered at $R_{sw,min}$. As the R_{sw}/R_a decreases towards $R_{sw,min}$, $R_{IF0,match,max}$ increases exponentially towards infinity. On the other hand, as the switch-to-antenna resistance ratio increases towards $R_{sw,max}$, $R_{IF0,match,max}$ is decreased down to zero at $R_{sw} = R_{sw,max}$. In the case of the virtual shunt resistance, its maximum value is given for $R_{IF} = \infty$ $\left(R_{sh0,fund,max} \approx 0.68\left(R_a + R_{sw,min}\right) \approx 0.81R_a\right)$ and its zero for $R_{sw} = R_a$. As we can observe, the equivalent SD-2PPM input resistance defined by equation 3.18, provides 50Ω RF input impedance matching along the different switch resistance values. Analytically speaking the mixer is able to provide RF input matching impedance even for negative IF resistances. However, for our ultra-low power application perspectives only the range defined between $R_{sw,min}$ and $R_{sw,max}$ is considered. This figure shows close matching between analytical and simulation results, thus validating our zero-IF SD-2PPM LTI input impedance development, as a simple approach to characterize the LTV SD-2PPM input impedance.

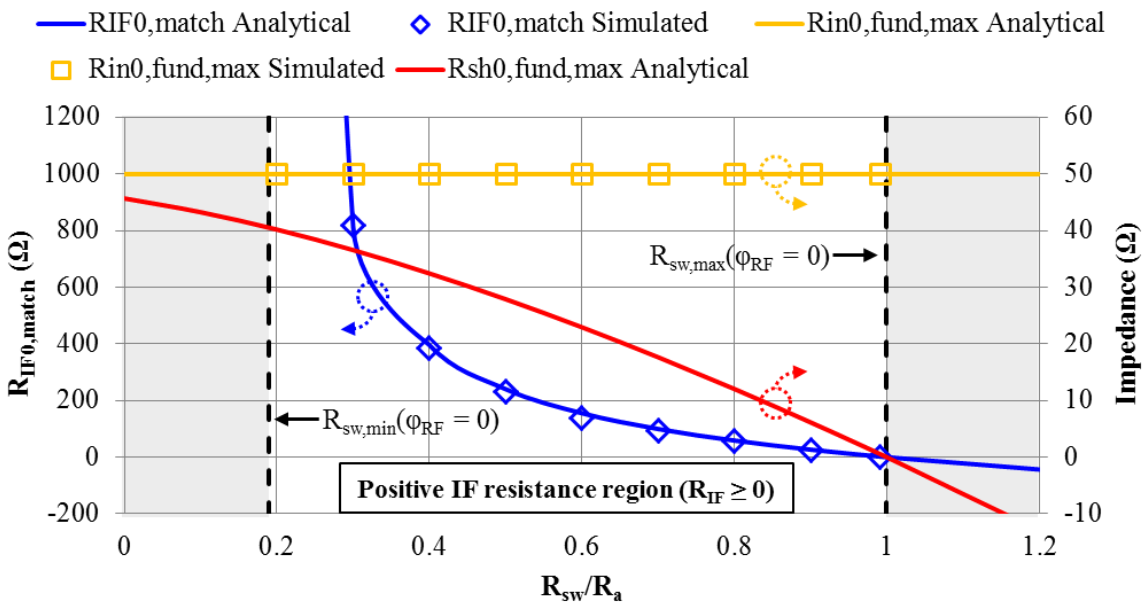


Figure 3.6. Zero-IF SD-2PPM analytical and simulated RF input impedance matching IF resistance, and analytical virtual shunt resistance and equivalent SD-2PPM input impedance, evaluated at ω_{LO} as a function of the R_{sw}/R_a. $f_{RF} = f_{LO} = 900MHz$, $R_a = 50\Omega$, $C_{IF} = 100pF$, $R_{IF} = R_{IF0,match,max}$ $(Z_{in,SD-2PPM} = R_a)$ and $\varphi_{RF} = 0$.

In order to complete our LTI zero-IF input impedance analysis, we derive the zero-IF matched IF resistance and the zero-IF input impedance as a function of the RF input phase shift.

$$R_{IF0,fund,SD-2PPM} = \frac{2(R_a^2 - R_{sw}^2)cos(\omega_{RF}t + \varphi_{RF})}{[R_a(2\gamma - 1) + R_{sw}]cos(\omega_{RF}t + \varphi_{RF}) + 2\gamma R_a cos(\omega_{RF}t - \varphi_{RF})} \quad (3.19)$$

$$Z_{in0,fund,SD-2PPM} = R_{in0,fund,SD-2PPM} = R_{sw} + R_{sh0,fund}||R_{IF}$$

$$= \frac{[2R_{sw}(R_a + R_{sw}) + R_{IF}(\gamma R_a + R_{sw})]cos(\omega_{RF}t + \varphi_{RF}) + \gamma R_a R_{IF} cos(\omega_{RF}t - \varphi_{RF})}{[2(R_a + R_{sw}) + R_{IF}(1 - \gamma)]cos(\omega_{RF}t + \varphi_{RF}) - \gamma R_{IF} cos(\omega_{RF}t - \varphi_{RF})} \quad (3.20)$$

This first zero-IF SD-2PPM input impedance metric validates our charge conservation methodology, which allowed us to model the LTV 2-PPM through a fully resistive LTI network, including a baseband virtual shunt resistance representing the energy loss due to the LO harmonic upconversion to the RF input signal path. Unlike the floating IF capacitor 2-PPM architectures developed in [Molnar] and [Cook02], our grounded common mode 2-path passive mixer architecture avoids any equivalent switched-capacitor frequency dependent impedance behavior $(Z_{SC} = 1 / f_{LO}C_{IF})$ and provides a constant input impedance with

respect to the LO frequency. This advantage enables RF input impedance matching, through large frequency ranges by simply tuning the LO frequency to the desired RF frequency.

This analysis also highlighted two principal SD-2PPM drawbacks: first, the RF input signal phase shift dependence of the input impedance and the output voltage response. This characterization indicates that complete signal attenuation results for $\varphi_{RF} = \pm\pi/2$. Second, the minimum switch resistance value $\left(R_{sw,min} \approx 0.19R_a\right)$ for which RF input impedance matching is guaranteed. It is important to recall that these two limitations are uniquely proper to 2-path passive mixers. 4-PPM and 8-PPM do not suffer from these limitations.

The following metric shows a practical solution to overcome the RF phase shift drawback by implementing the 2-PPMs as heterodyne mixing devices.

Metric 2 – Heterodyne SD-2PPM input impedance:

So far, we have analyzed the zero-IF SD-2PPM input impedance evaluated at ω_{LO}. In the case of heterodyne mixers, the downconverted output signal is no longer centered at DC but at an Intermediate Frequency (IF). Here, the desired RF input frequency is defined as $\omega_{RF} = \omega_{LO} \pm \omega_{IF}$. Since the 2-PPM has a non-orthogonal output architecture, the band-pass filter response generated at its RF input node is symmetrical with respect to the LO frequency. This behavior indicates that 2-PPMs receive both the desired RF input frequency and the Image Frequency (IM).

Following the same zero-IF charge conservation development and considering both IF frequency sidebands ($\pm\omega_{IF}$), the voltage across each IF capacitor for heterodyne SD-2PPMs is given by

$$V_{c,m}(t) = \frac{2}{\pi}\left[\frac{R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}$$

$$\times \left[Cos(\omega_{IF}t + \varphi_{RF} + m\pi) + Cos(-\omega_{IF}t - \varphi_{RF} + m\pi)\right] \quad (3.21)$$

Since the output voltage response is characterized by a sinusoidal signal with carrier frequency ω_{IF}, the influence of the RF input phase shift is eliminated. This behavior is the

key advantage of heterodyne 2-PPM architectures, which completely eliminates the zero-IF RF phase shift dependence drawback.

Following our analysis, the fundamental component of the virtual V_x square wave is

$$V_{x,fund}(t) = \frac{\left(V_{c,0}(t) - V_{c,1}(t)\right)}{2} V_{LO}(t)$$

$$= \left[\frac{2\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}[Cos(\omega_{IF}t + \varphi_{RF}) + Cos(-\omega_{IF}t - \varphi_{RF})]\, cos(\omega_{LO}t)$$

$$= \left[\frac{2\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}\left[Cos\left((\omega_{LO} + \omega_{IF})t + \varphi_{RF}\right) + Cos\left((\omega_{LO} - \omega_{IF})t - \varphi_{RF}\right)\right]$$

$$= \left[\frac{2\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}[\cos(\omega_{RF}t + \varphi_{RF}) + \cos(\omega_{IM}t - \varphi_{RF})] \quad (3.22)$$

Where $\gamma = 2/\pi^2 \approx 0.203$. Assuming no energy at the IM frequency,

$$V_{x,fund}(t) = \left[\frac{2\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF} \cos(\omega_{RF}t + \varphi_{RF}) \quad (3.23)$$

This result is very important because in the case where $\varphi_{RF} = 0$, equation 3.23 perfectly matches the zero-IF $V_{x0,fund}$ voltage response provided in equation 3.9. Having this in mind, the foregoing zero-IF SD-2PPM input impedance development with $\varphi_{RF} = 0$, can be also considered for the heterodyne SD-2PPM analysis. Hence, the heterodyne virtual shunt and IF match resistances are defined as demonstrated in equations 3.14 and 3.15.

$$R_{sh,fund} = \frac{2\gamma(R_a + R_{sw})R_{IF}}{2(R_a + R_{sw})(1 - \gamma) + R_{IF}(1 - 2\gamma)} \quad (3.24)$$

$$R_{IF,match} = \frac{2R_a^2 - 2R_{sw}^2}{R_a(4\gamma - 1) + R_{sw}} \quad (3.25)$$

This IF matched resistance is defined for $\omega_{IF} \neq 0$ and makes reference to the fact of providing RF input impedance matching at LO frequency, but not at the desired RF frequency. Similarly to the foregoing zero-IF development, in order to ensure positive IF matched resistance values, the switch and the virtual shunt resistances are defined between

the ranges $0.19R_a \lesssim R_{sw} \leq R_a$ and $0.68(R_a + R_{sw}) \gtrsim R_{sh,fund} \geq 0$, as demonstrated in equations 3.16 and 3.17.

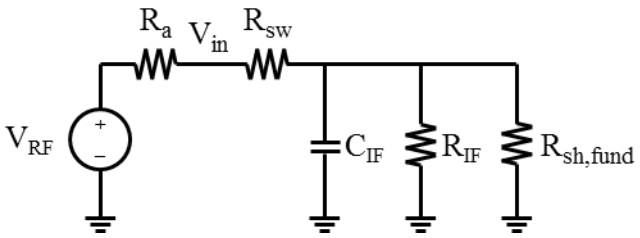


Figure 3.7. Equivalent steady-state heterodyne passive mixer simplified model.

In order to properly characterize the steady-state heterodyne SD-2PPM input impedance, we modify the zero-IF fully resistive LTI model, by introducing the IF capacitor and by evaluating its impedance as a function of the IF frequency (Figure 3.7). Hence, considering the resistances derivations above and the influence of the IF capacitor, the SD-2PPM steady-state input impedance generated around the LO fundamental harmonic frequency is given by

$$Z_{in,fund,SD-2PPM}(\omega_{LO} \pm \omega_{IF}) = R_{sw} + \left(R_{sh,fund}||R_{IF}\right)||Z_{CIF}(\pm\omega_{IF})$$

$$= R_{sw} + \frac{\left(R_{sh,fund}||R_{IF}\right)}{1 + \left(\pi\omega_{IF}\left(R_{sh,fund}||R_{IF}\right)C_{IF}\right)^2} \pm j\frac{\pi\omega_{IF}\left(R_{sh,fund}||R_{IF}\right)^2 C_{IF}}{1 + \left(\pi\omega_{IF}C_{IF}\left(R_{sh,fund}||R_{IF}\right)\right)^2} \quad (3.26)$$

Figure 3.8 shows the analytical and the simulated SD-2PPM input impedance as a function of the RF frequency for different IF capacitor values. Simulated and analytical results present close matching with a slight difference on the imaginary input impedance response due to the parasitic MOS transistor capacitances of the switch devices. This behavior gets more evident as the IF capacitance is reduced. From the stand point of frequency response, the input impedance is degraded as the RF frequency is shifted away from the LO frequency. This effect creates a band-pass like input impedance response, whose bandwidth gets reduced as the IF capacitor is increased. This figure provides a first approach of the SD-2PPM input band-pass filter frequency response for which the quality factor appears as being proportional to C_{IF}. Here, the N-path mixer presents a capacitive behavior for positive IF frequencies ($\omega_{IF} > 0$) and an inductive behavior for negative IF frequencies ($\omega_{IF} < 0$). For $\omega_{IF} = 0$ ($\omega_{RF} = \omega_{LO}$), the zero-IF SD-2PPM input impedance response

depends on the RF phase shift. In this figure, the zero-IF input impedance is represented assuming $\varphi_{RF} = 0$.

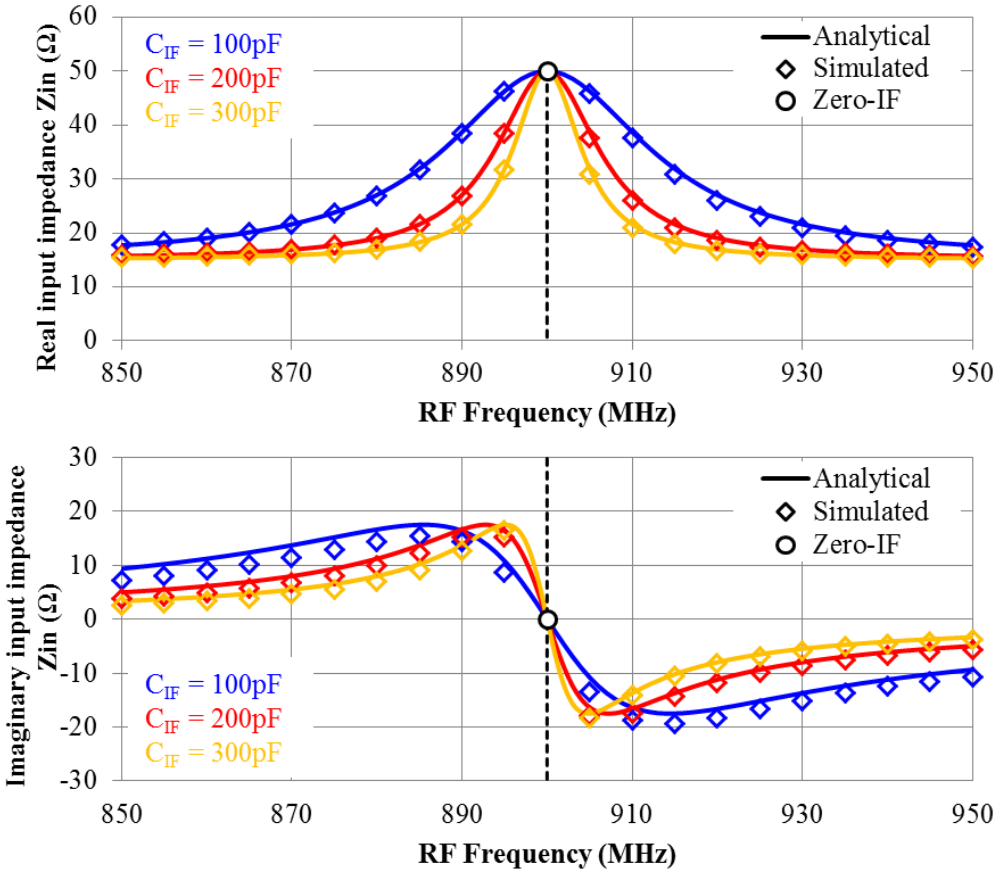


Figure 3.8. Analytical and simulated SD-2PPM input impedance as a function of the RF frequency for different IF capacitor values. $f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{sw} = 15\Omega$ and $R_{IF} = 812\Omega$.

Another interesting behavior that has to be analyzed is the influence of the IF capacitor on the S_{11}-parameter. As described by equations 3.3 and 3.4, in order to ensure a correct mixing behavior, the IF capacitor must be much larger than the ratio between the LO period and the two resistive networks $R_a + R_{sw}$ and R_{IF} [Soer02]. Figure 3.9 characterizes this behavior presenting the SD-2PPM S_{11} periodical steady-state simulation response for different IF capacitor values as a function of the RF input frequency. As we can observe, as the RF frequency approaches the LO frequency the S_{11} response gets reduced, hence creating a notch frequency response centered around the LO frequency. On the other hand, as the IF capacitor decreases the imaginary component of the input impedance is degraded, shifting the zero-crossing imaginary complex conjugate and the S_{11} notch response towards lower frequencies. In this case, equation 3.26 is no longer applicable. Note that even for very high

IF capacitance values, the parasitic capacitances of the MOS switch transistors generate a slight offset on the S_{11} notch frequency. This effect is neglected in our analysis.

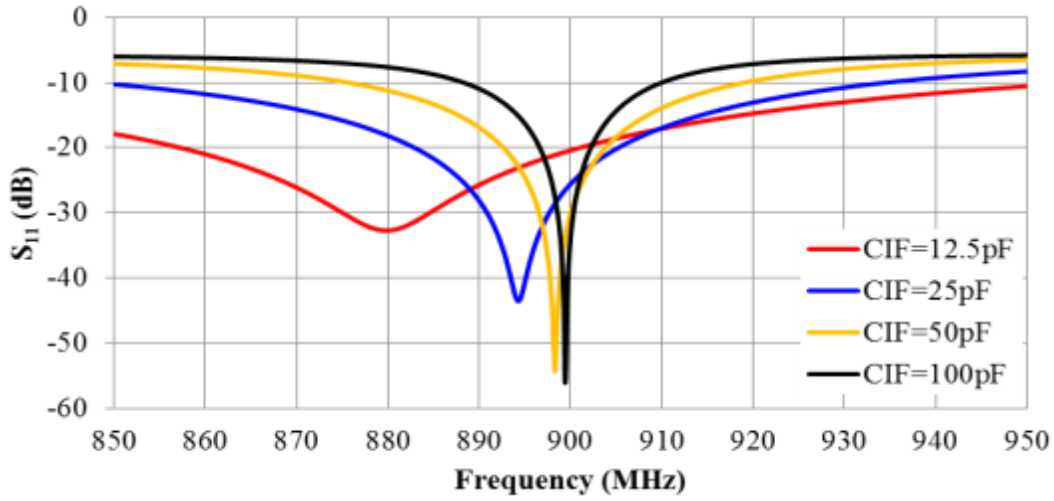


Figure 3.9. PSS simulated SD-2PPM S_{11} response as a function of the RF frequency for different IF capacitor values. $f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{sw} = 15\Omega$ and $R_{IF} = 812\Omega$.

This analysis has demonstrated the heterodyne N-PPM independence with respect to the RF signal phase shift. The steady state simplified heterodyne SD-2PPM model has also demonstrated the transparency behavior, for which a band-pass filter impedance response is generated at the 2-path mixer input node, by the upconversion of the IF low-pass filter impedance response, through mixing with the LO. Since our LO signal has a square waveform, this band-pass filter behavior is extended to the entire LO spectrum.

Metric 3 - Influence of LO harmonics:

The analysis done so far has only taken into account the fundamental component of the LO signal. The square waveform of the LO extends this analysis to all other LO harmonics. Hence, assuming a constant RF input impedance over the frequency and considering both IF frequency sidebands ($\pm\omega_{IF}$), the heterodyne square wave virtual $V_{x,n}$ voltage is defined as

$$V_{x,n}(t) = \frac{\left(V_{c,1}(t) - V_{c,0}(t)\right)}{2} V_{LO,n}(t)$$

$$= \frac{1}{n^2}\left[\frac{2\gamma R_{IF} A_{RF}}{R_{IF} + 2(R_a + R_{sw})}\right]\left[Cos\left(n(\omega_{IF}t + \varphi_{RF})\right) + Cos\left(n(-\omega_{IF}t - \varphi_{RF})\right)\right] Sin\left(\frac{n\pi}{2}\right) Cos(n\omega_{LO}t)$$

$$= \frac{1}{n^2}\left[\frac{2\gamma R_{IF} A_{RF}}{R_{IF} + 2(R_a + R_{sw})}\right]\left[Cos\left((n(\omega_{LO} + \omega_{IF})t + \varphi_{RF})\right) + Cos\left((n(n\omega_{LO} - \omega_{IF})t - \varphi_{RF})\right)\right]$$

$$= \frac{1}{n^2}\left[\frac{2\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}\,[Cos(n\omega_{RF}t) + Cos(n\omega_{IM}t)] \quad (3.27)$$

Where $\gamma = 2/\pi^2 \approx 0.203$, n represents the odd harmonics of the LO square wave signal and V_{IF} is the baseband differential output signal $\left(V_{IF} = V_{c,1} - V_{c,0}\right)$. Assuming no energy at the image frequency,

$$V_{x,n}(t) = \frac{1}{n^2}\left[\frac{2\gamma R_{IF}}{R_{IF} + 2(R_a + R_{sw})}\right] A_{RF}\, Cos(n\omega_{LO}t) \quad (3.28)$$

Following the same LTV and LTI models development provided in the previous sections, the heterodyne shunt resistance R_{sh} is defined as a function of the LO harmonics:

$$R_{sh,n}(n\omega_{LO}) = \frac{2\gamma(R_a + R_{sw})R_{IF}}{2(R_a + R_{sw})(n^2 - \gamma) + R_{IF}(n^2 - 2\gamma)} \quad (3.29)$$

This virtual shunt resistance appears at every LO harmonic, as a consequence of the energy lost due to the LO harmonics upconversion to the RF input signal path. Therefore, the SD-2PPM input resistance at every LO harmonic is

$$R_{in,n,SD-2PPM}(n\omega_{LO}) = R_{sw} + R_{sh,n}(n\omega_{LO})||R_{IF} \quad (3.30)$$

Considering the frequency translated IF capacitance effect, the input impedance of the SD-2PPM is expressed as

$$Z_{in,n,SD-2PPM}(n\omega_{LO} \pm \omega_{IF}) = R_{sw} + \left(R_{sh,n}(n\omega_{LO})||R_{IF}\right)||Z_{CIF}(\pm n\omega_{IF}) \quad (3.31)$$

Figure 3.10 presents the analytical and simulated results for the heterodyne SD-2PPM input impedance as a function of the LO harmonics. Analytical and simulated results shows relative matching, expect for near DC frequencies for which 2-PPM DC analytical response has been neglected in equation 3.31. The SD-2PPM provides a resistive impedance at each odd LO harmonics. 50Ω RF input impedance matching is provided at the LO fundamental harmonic. As the LO harmonics increases, the resulting virtual shunt resistance is decreased following a $1/n^2$ ratio. For out-of-band frequencies with respect to each LO harmonic, the

virtual shunt resistance and the IF capacitor shorts the mixer output node and provides an equivalent input impedance equal to the switch resistance $(R_{sw} = 15\Omega)$.

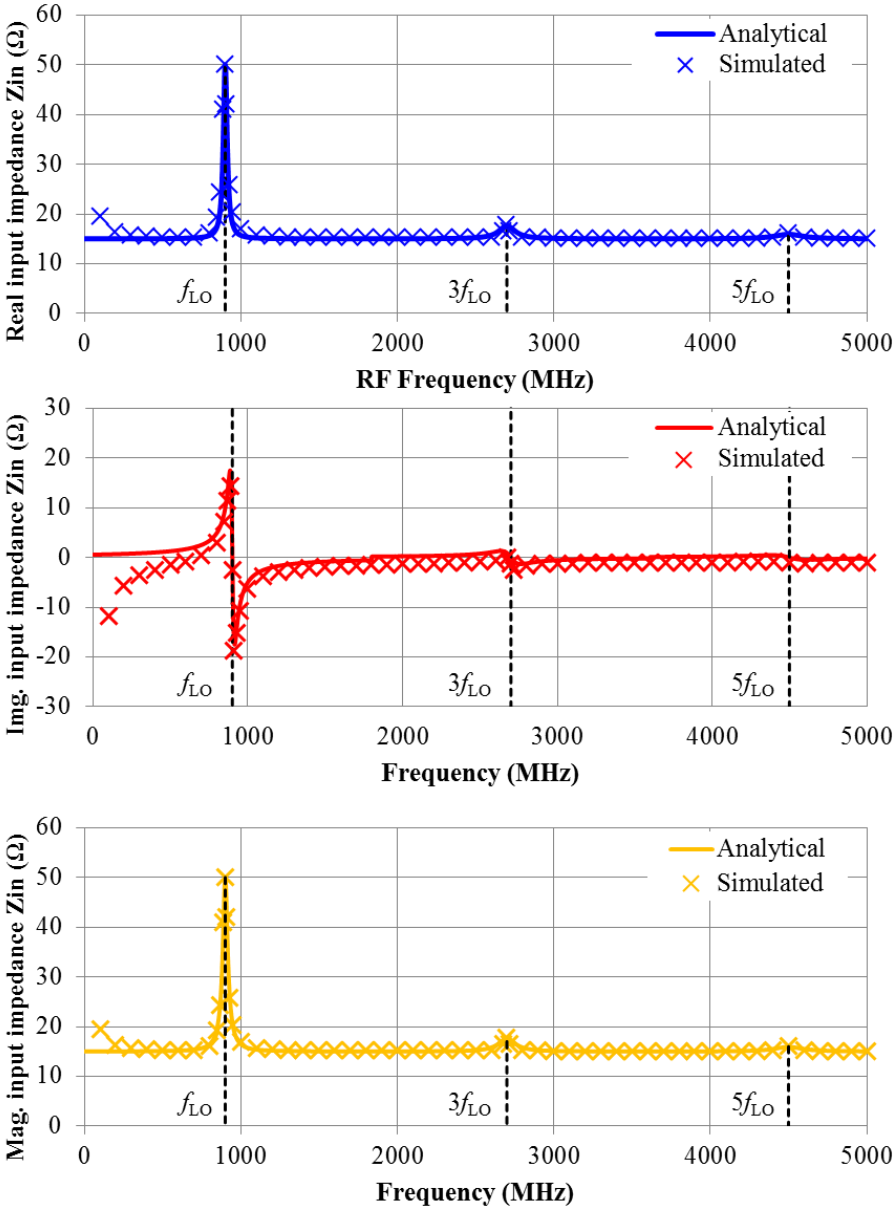


Figure 3.10. Analytical and simulated results for the heterodyne SD-2PPM input impedance as a function of the LO harmonics. $f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{sw} = 15\Omega$, $R_{IF} = 812\Omega$ and $C_{IF} = 100pF$.

To summarize, this section has provided an analysis of the SD-2PPM input impedance with respect to three different metrics: the zero-IF input impedance, the heterodyne input impedance and the heterodyne input impedance at the LO harmonics. This analysis has shown that the SD-2PPM input impedance can be characterized by modeling the LTV circuit

as an equivalent fully resistive LTI model. This LTI model is composed of a frequency translated baseband virtual shunt resistance $\left(R_{sh}(n\omega_{LO})\right)$, representing the energy lost due to the upconversion of the LO harmonics to the RF input path. This two-path only mixer architecture presents two drawbacks: the RF phase shift dependence voltage response for zero-IF configurations and the minimum R_{sw} required to provide matching to the RF input. In order to overcome the phase shift limitation, heterodyne architectures can be used. The 2-PPM provides a BPF input impedance response, thanks to the upconversion of the baseband LPF impedance to the RF node. Given the square waveform of the LO, this band-pass filter response is also extended to the entire spectrum of the local oscillator.

3.2.2. SD-2PPM frequency response

The previous impedance analysis provides us a first approach on the 2-path mixer frequency response. This passive architecture translates the baseband LPF impedance to high-frequencies to generate a BPF response at the RF input node. This section presents the frequency response for homodyne and heterodyne SD-2PPMs. Since most of the received energy is generated by the first LO harmonic, this section is limited to the frequency response analysis with respect to the fundamental LO component.

Metric 1 - SD-2PPM input frequency response:

The SD-2PPM input frequency response is defined by the resistive divider network response formed by the antenna resistance and the SD-2PPM input impedance. Considering Figure 3.7, the SD-2PPM input frequency response is given by the ratio between the SD-2PPM input voltage (V_{in}) and the RF input voltage (V_{RF}).

$$\left|A_{v,in,SD-2PPM}(\omega_{RF} \pm \omega_{IF})\right| = \left|\frac{V_{in}(\omega_{LO} \pm \omega_{IF})}{V_{RF}(\omega_{LO} \pm \omega_{IF})}\right| = \left|\frac{Z_{in,SD-2PPM}(\omega_{LO} \pm \omega_{IF})}{Z_{in,SD-2PPM}(\omega_{LO} \pm \omega_{IF}) + R_a}\right| \quad (3.32)$$

Where $Z_{in,SD-2PPM}(\omega_{LO} \pm \omega_{IF})$ represents the SD-2PPM input impedance evaluated at the fundamental LO component (equation 3.26). Optimum input frequency response is

achieved when RF input impedance matching is provided. In this case, the voltage at the input node is half the one of the RF voltage.

The key point of the SD-2PPM input frequency response is to characterize its capacity to attenuate out-of-band non-desired signals. Considering Figure 3.7, the SD-2PPM input Interference Rejection Ratio (IRR) is defined as the ratio between the SD-2PPM input frequency response evaluated at the RF frequency and the SD-2PPM input frequency response evaluated at the offset frequency.

$$IRR_{SD-2PPM,in} = \frac{\left|A_{v,in,SD-2PPM}(\omega_{LO} \pm \omega_{IF})\right|}{\left|A_{v,in,SD-2PPM}(\omega_{LO} \pm \omega_{IF} + \omega_{offset})\right|} \tag{3.33}$$

Maximum out-of-band input IRR is obtained for a zero-IF 2-path mixer architecture with $\varphi_{RF} = 0$ and an infinite offset frequency. Hence, assuming impedance matching to the RF input, the maximum IRR is expressed as

$$IRR_{SD-2PPM,in,max} = \frac{\left|A_{v,in,SD-2PPM}(\omega_{LO})\right|}{\left|A_{v,in,SD-2PPM}(\omega_{LO} + \omega_{offset})\right|}\Bigg|_{\omega_{offset}=\infty} = \frac{R_a + R_{sw}}{2R_{sw}} \tag{3.34}$$

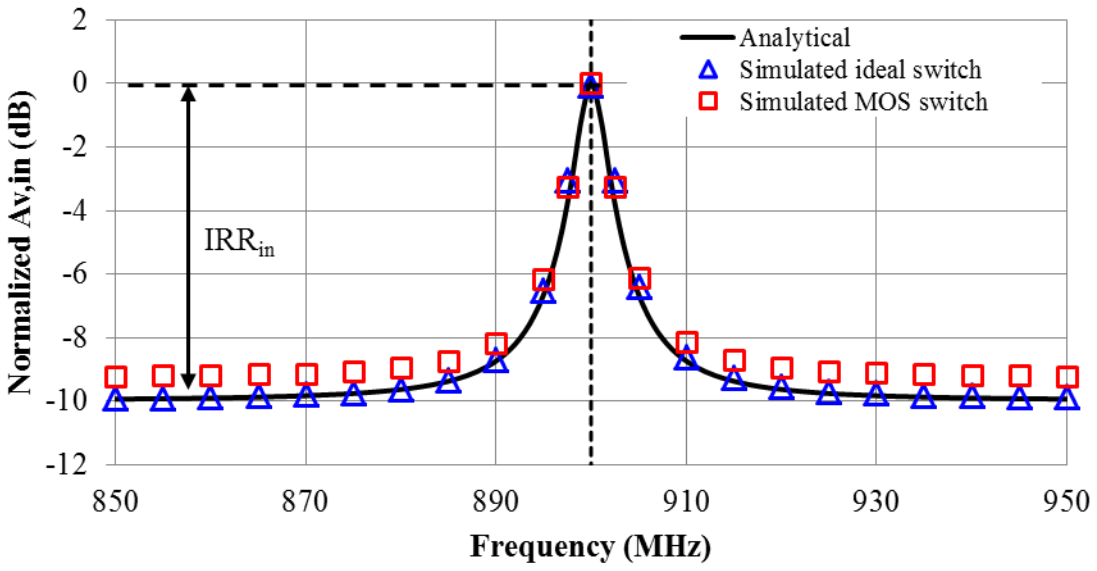


Figure 3.11. Normalized analytical and simulated SD-2PPM input frequency response for $\varphi_{RF} = 0$ as a function of frequency, considering ideal and MOS switch devices. $\omega_{LO} = \omega_{RF}$, $f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{sw} = 9.4\Omega$, $R_{IF} = \infty$, $C_{IF} = 1nF$.

In the particular case where $R_{IF} = \infty$ and $R_{sw} = R_{sw,min} \approx 0.19R_a$, the SD-2PPM IRR is $10dB$. Figure 3.11 presents the normalized analytical SD-2PPM input frequency response for $\varphi_{RF} = 0$, as a function of the frequency. Here, R_{sw} and R_{IF} are chosen so as to provide matching to the antenna. $1nF$ IF capacitor is used in order to observe the influence of the maximum out-of-band input IRR at $50MHz$. The input frequency response describes a band-pass filter function centered at the LO frequency. Two switch models have been employed for the periodical steady state simulations: an ideal switch model with a 9.4Ω switch resistance and a MOS transistor model working in triode region with an effective on-resistance of 9.4Ω. As we can observe analytical results show good agreement with respect to the simulation results using the ideal switch models. Here, the maximum IRR reaches $10dB$ as specified in equation 3.34. In the case of the MOS transistor model, the out-of-band IRR presents a slightly attenuation coming from the transistor parasitic elements and the silicon substrate losses.

Metric 2 - SD-2PPM zero-IF output frequency response:

The zero-IF frequency response ($\omega_{IF} = 0$) considers a LO frequency equal to the input RF frequency ($\omega_{LO} = \omega_{RF}$). The SD-2PPM output voltage gain can be easily derived considering the LTI model (see Figure 3.5) and calculating the ratio between the differential baseband output voltage (V_{IF0}) and the mixer input voltage evaluated at ω_{RF}. Considering Figure 3.5 and considering the zero-IF input impedance expression derived in equation 3.20, the mixer input voltage is

$$V_{in}(\omega_{RF}) = V_{RF}(\omega_{RF}) \frac{Z_{in0,fund,SD-2PPM}}{Z_{in0,fund,SD-2PPM} + R_a}$$

$$= V_{RF}(\omega_{RF})$$

$$\times \frac{[2R_{sw}(R_a + R_{sw}) + R_{IF}(\gamma R_a + R_{sw})]cos(\omega_{RF}t + \varphi_{RF}) + \gamma R_a R_{IF} cos(\omega_{RF}t - \varphi_{RF})}{(R_a + R_{sw})[2(R_a + R_{sw}) + R_{IF}]cos(\omega_{RF}t + \varphi_{RF})} \quad (3.35)$$

Considering equation 3.7, the differential DC baseband output is expressed as $V_{IF0} = V_{C,0} - V_{C,1} = 2V_{C,0}$. Hence, the zero-IF SD-2PPM voltage gain is given by

$$\left|A_{v0,SD-2PPM}\right| = \left|\frac{V_{IF0}}{V_{in}(\omega_{RF})}\right|$$

$$= \frac{2\pi\gamma(R_a + R_{sw})R_{IF}cos(\varphi_{RF})}{[2R_{sw}(R_a + R_{sw}) + R_{IF}(\gamma R_a + R_{sw})]cos(\omega_{RF}t + \varphi_{RF}) + \gamma R_a R_{IF}cos(\omega_{RF}t - \varphi_{RF})} \quad (3.36)$$

Where $\gamma = 2/\pi^2 \approx 0.203$. From the equation above, maximum peak voltage gain is obtained for $\varphi_{RF} = 0$.

$$\left|A_{v0,SD-2PPM}(\varphi_{RF} = 0)\right| = \frac{2\pi\gamma(R_a + R_{sw})R_{IF}}{2R_{sw}(R_a + R_{sw}) + R_{IF}(2\gamma R_a + R_{sw})} \quad (3.37)$$

However, for $\varphi_{RF} = \pm\pi/2$ the baseband output signal is completely attenuated and the linear voltage gain is zero. Figure 3.12 presents the peak zero-IF SD-2PPM output voltage gain as a function of the switch-to-antenna resistance ratio, for $\varphi_{RF} = 0$, in the particular case of RF input impedance matching $(Z_{in0,SD-2PPM} = R_a)$. As specified by equation 3.37, as the switch resistance increases towards R_a the zero-IF voltage gain decreases asymptotically towards minus infinity. Given the SD-2PPM minimum switch resistance limitation ($R_{sw,min} \approx 0.19R_a$), a maximum voltage gain of $8.13dB$ is obtained for $R_{IF} = \infty$. This figure shows very close matching between the analytical and simulated results.

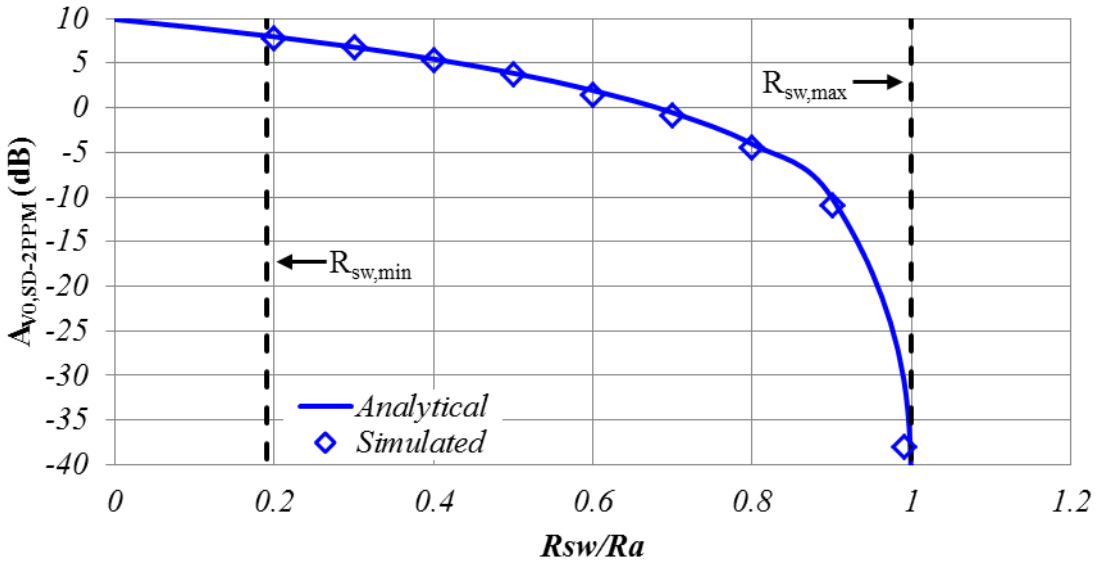


Figure 3.12. Analytical and simulated peak Zero-IF SD-2PPM output voltage gain as a function of the switch-to-antenna resistance ratio, with $\varphi_{RF} = 0$ and RF input impedance matching. $f_{RF} = f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{IF} = R_{IF0.match}$ and $C_{IF} = 100pF$.

This analysis is very important because it demonstrates the possibility of providing voltage gain by using a simple passive mixer structure. The main reason behind this is the single-to-differential transformation, which provides a gain factor of two (6dB). The remaining voltage gain ($2.13dB$ in the case of $R_{sw} \approx 0.19R_a$ and $\varphi_{RF} = 0$) comes from a passive impedance transformation that boosts the input impedance to higher values.

Metric 3 - SD-2PPM heterodyne output frequency response:

Unlike the zero-IF configurations, the heterodyne 2-PPM output frequency response does not depend on the RF phase shift. Similarly to the heterodyne input impedance, the DC voltage gain component of the heterodyne SD-2PPM is equal to that of the zero-IF SD-2PPM with $\varphi_{RF} = 0$. Therefore, considering the influence of the IF capacitance, the heterodyne SD-2PPM output voltage gain is given by

$$\left|A_{v,SD-2PPM}(\omega_{IF})\right| = \left|\frac{A_{v0,SD-2PPM}}{1 + j\dfrac{\omega_{IF}}{\omega_{BW,SD-2PPM}}}\right| = \frac{\left|A_{v0,SD-2PPM}\right|}{\sqrt{1 + \left(\dfrac{\omega_{IF}}{\omega_{BW,SD-2PPM}}\right)^2}} \tag{3.38}$$

With,

$$A_{v0,SD-2PPM} = \frac{2\pi\gamma(R_a + R_{sw})R_{IF}}{2R_{sw}(R_a + R_{sw}) + R_{IF}(2\gamma R_a + R_{sw})} \tag{3.39}$$

$$\omega_{BW,SD-2PPM} = \frac{2(R_a + R_{sw}) + R_{IF}}{2\pi\gamma(R_a + R_{sw})R_{IF}C_{IF}} \tag{3.40}$$

Where $\omega_{BW,SD-2PPM}$ represents the $-3dB$ corner frequency of the baseband IF LPF, and is obtained considering the whole system including the antenna impedance. Figure 3.13 shows the analytical and simulated heterodyne SD-2PPM output voltage gain as a function of the IF frequency, considering ideal and MOS switch devices. The function describes a band-pass filter shape centered at DC. This figure assumes $\varphi_{RF} = 0$ for the zero-IF frequency response. Analytical and ideal switch simulated results show close matching. In the case of switch MOS devices, the frequency response shows a slight attenuation, for out-of-band frequencies ($f_{IF} > 25MHz$), due to the parasitic and substrate losses. This figure validates

our analytical SD-2PPM output frequency response model and demonstrates the important strength of this simple structure able to provide an in-band passive voltage gain above $8dB$.

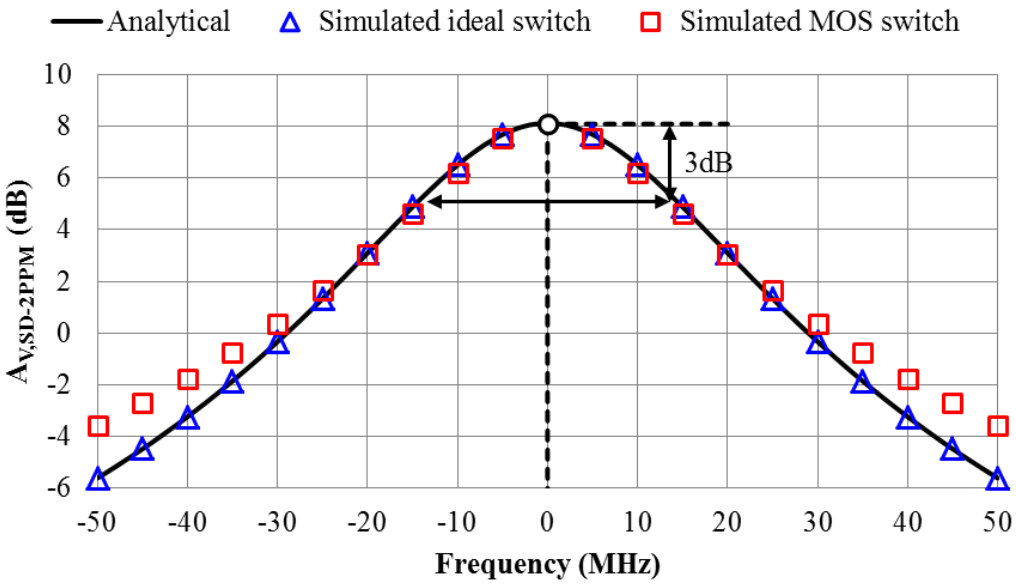


Figure 3.13. Analytical and simulated heterodyne SD-2PPM output voltage gain as a function of the IF frequency, considering ideal and MOS switch devices. $f_{RF} = f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{sw} = 9.4\Omega$, $R_{IF} = \infty$ and $C_{IF} = 100pF$.

Taking into account the $-3dB$ bandwidth, the quality factor of the BPF generated at the RF input node is written as

$$Q_{SD-2PPM} = \frac{\omega_{RF}}{2\omega_{BW,SD-2PPM}} = \frac{\omega_{RF}\pi\gamma(R_a + R_{sw})R_{IF}C_{IF}}{2(R_a + R_{sw}) + R_{IF}} \tag{3.41}$$

This quality factor is the key parameter of this analysis, indicating that it is directly proportional to the IF capacitance and that it can be further optimized by increasing the antenna resistance, while holding the switch resistance to its minimum value. As an example, in order to have a Q-factor of 100 at $f_{RF} = 900MHz$ with $R_a = 50\Omega$, $R_{sw} = 0.19R_a$ and $R_{IF} = \infty$, the load IF capacitor must be equal to $467pF$. In IC design, such capacitor value cannot be considered because of the high area required. Instead, if the antenna impedance module is boosted to $R_a = 1k\Omega$ the capacitor value may be reduced to only $23pF$. Aside from the extra noise brought by this impedance enhancement, this 2-path passive mixer approach offers the possibility to provide some passive voltage gain and generate very high-Q band-pass filters by means of integrated electronics with reduced power budget.

3.2.3. SD-2PPM noise analysis

To analyze the noise response of the SD-2PPM, we recall the noise figure expression presented in Chapter 2.

$$NF = 10log(F) = 10log\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{3.42}$$

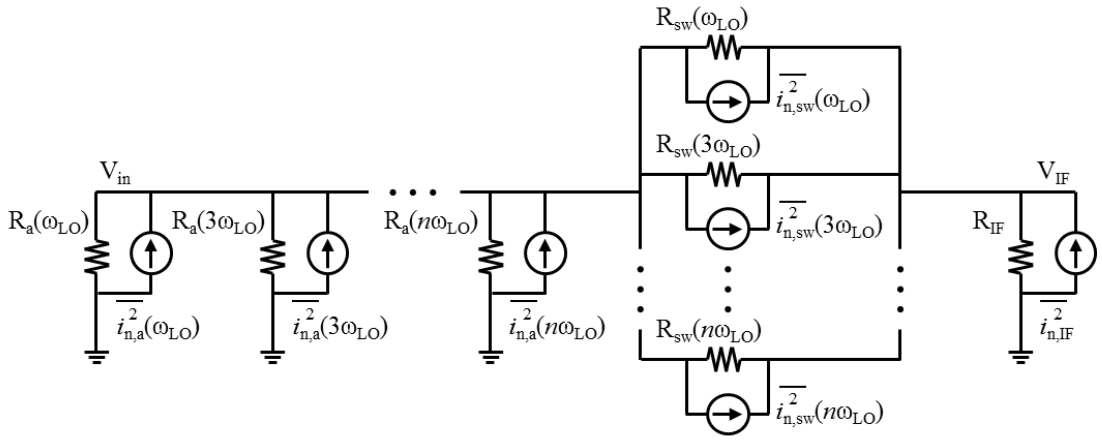
In the case of a two-port system, the noise factor can be expressed as [Razavi02]

$$F = \frac{v_{n,out}^2}{A^2}\frac{1}{4kTR_s} \tag{3.43}$$

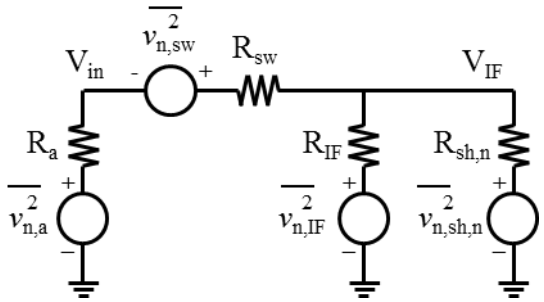
Where R_s is the source resistance, k is the Boltzmann constant, T is the absolute temperature, A is the voltage gain provided by the system and $v_{n,out}^2$ is the output mean square noise voltage per hertz bandwidth. The noise figure of active and passive mixers is defined as a function of the noise contributions generated by the LO harmonics. In the case of a square wave LO, the energy from the LO odd harmonics fold into the mixer IF output [Niknejad]. Hence, the mixer noise factor is represented by

$$F = \sum_{n=1,3,5\ldots}^{\infty} \frac{V_{n,out}^2{}_n}{A^2{}_n}\frac{1}{4kTR_s} \tag{3.44}$$

Where n represents the odd LO harmonics and $V_{n,out}^2{}_n$ and $A^2{}_n$ are, respectively, the output noise voltage per unity bandwidth and the in-band voltage gain evaluated at the respective n^{th} harmonic. In the case of the SD-2PPM, the influence of the LO harmonics suggests that each resistor generates a mean square noise current ($\overline{i_n^2}$) at every odd LO harmonic as depicted in Figure 3.14.a. Our impedance analysis provided in section 3.2.1 allows us to represent the equivalent linear time invariant SD-2PPM noise model as shown in Figure 3.14.b. Here, the virtual shunt resistor (equation 3.29) models the energy lost due to the LO harmonics upconversion to the RF input and ($\overline{v_{n,sh,n}^2}$) represents the correlated mean square noise voltage due to the LO harmonics that fold into the IF-band.



(a)



(b)

Figure 3.14. (a) Equivalent SD-2PPM noise model and (b) equivalent linear time invariant SD-2PPM noise model.

From equation 3.44, the SD-2PPM noise factor is derived taking into account that R_s represents the RF input antenna resistance (R_a) and V^2_{n,out_n} represents the output noise voltage per hertz bandwidth generated by the SD-2PPM output resistance evaluated at each LO harmonic $(R_{out,n})$. Considering the voltage gain provided by the fully resistive LTI network $(A_{v,fund,RaLTI})$, the heterodyne SD-2PPM in-band noise factor is written as

$$F_{SD-2PPM} = \sum_{n=1,3,5\ldots}^{\infty} \frac{V^2_{n,out_n}}{A^2{}_n} \frac{1}{4kTR_s} = \sum_{n=1,3,5\ldots}^{\infty} \frac{R_{out,n}}{A^2_{v,fund,RaLTI}R_a}$$

$$= \sum_{n=1,3,5\ldots}^{\infty} \frac{(R_{sh,n}||R_{IF})||(R_a+R_{sw})}{A^2_{v,fund,RaLTI}R_a} = \sum_{n=1,3,5\ldots}^{\infty} \frac{(R_a+R_{sw})[2(R_a+R_{sw})+R_{IF}]}{2\gamma n^2 R_a R_{IF}} \quad (3.45)$$

Considering RF input matching impedance with $R_{IF} = R_{IF,match}$ (equation 3.15), the in-band noise factor becomes

$$F_{SD-2PPM,match} = \sum_{n=1,3,5\ldots}^{\infty} \frac{2(R_a + R_{sw})}{n^2(R_a - R_{sw})} \tag{3.46}$$

Figure 3.15 shows the analytical and the simulated impedance matched heterodyne SD-2PPM noise figure as a function of the switch-to-antenna resistance ratio (R_{sw}/R_a) evaluated at $1MHz$ DC offset. Periodical steady-state noise figure simulations are obtained considering the first 100 LO harmonics. As depicted, the NF increases and tends to infinity as the R_{sw}/R_a ratio increases towards one. A minimum NF of $4.66dB$ is obtained for $R_{IF} = \infty$ and $R_{sw}/R_a = 0.188$.

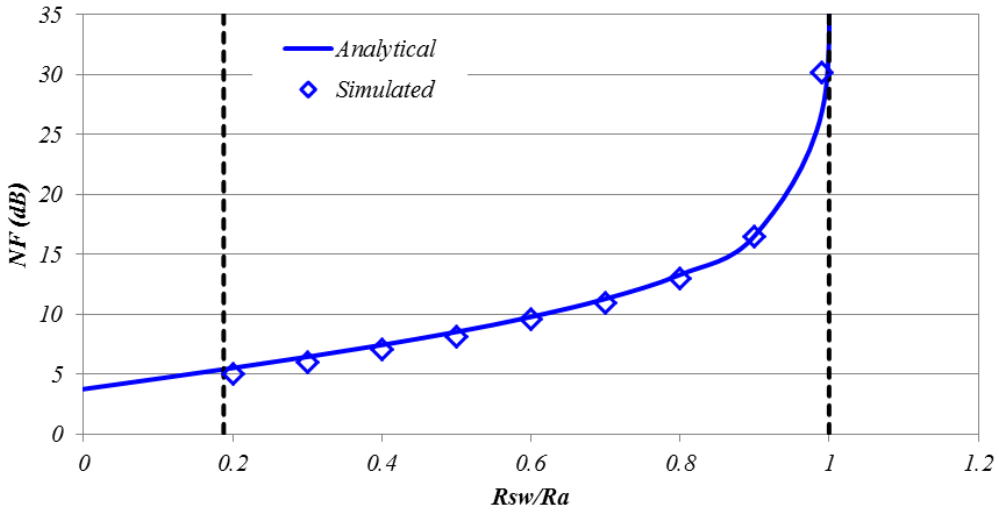


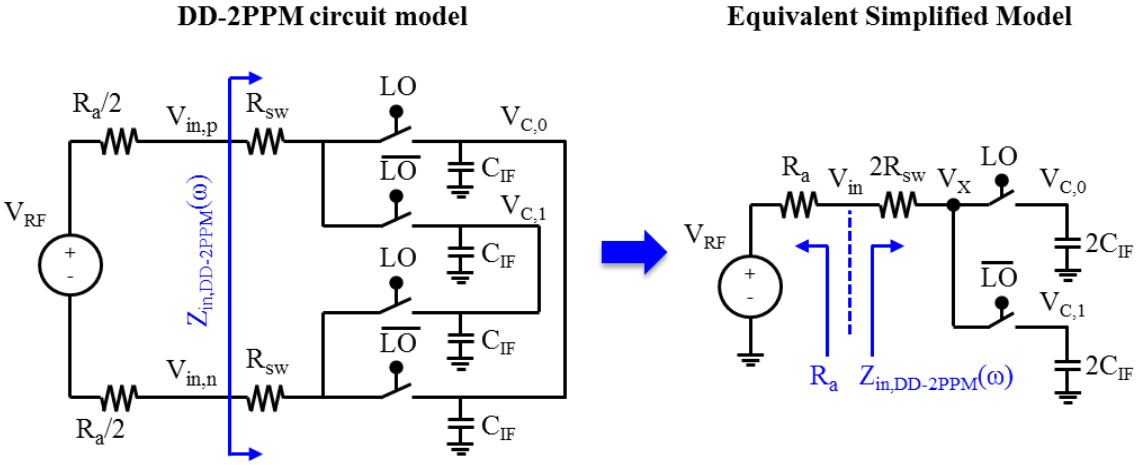
Figure 3.15. Comparison between analytical and simulated SD-2PPM noise figure as a function of the switch-to-antenna resistance ratio. $f_{RF} = f_{LO} = 900MHz$, $R_a = 50\Omega$, $R_{IF} = R_{IF.match}$ and $C_{IF} = 100pF$.

In this section we have demonstrated the interesting features of the single-to-differential 2-path passive mixers. Key parameters enabling the generation of high-Q band-pass filters, with passive voltage gain and moderate noise figure are presented. Despite the SD-2PPM minimum switch resistance limitation, these 2-path architectures are suitable for heterodyne mixer-first receivers requiring narrow band-pass filtering and very low power consumption. Due to the input phase shift AM downconversion dependence, zero-IF 2-path mixer architectures should be avoided, unless continuous phase shift control is guaranteed.

3.3. Fully differential 2-Path Passive Mixer (DD-2PPM)

The analysis presented so far takes only into account single-ended input N-path architectures. In order to provide input common mode rejection, fully differential 2-PPM can be used. Based on the previous SD-2PPM analysis, this section characterize DD-2PPMs in terms of input impedance, frequency response and noise figure.

3.3.1. DD-2PPM impedance analysis



(a) (b)

Figure 3.16. DD-2PPM circuit model (a) and its equivalent simplified model (b).

Figure 3.16 presents the DD-2PPM circuit model and its corresponding equivalent single-ended input simplified model. The N-path mixer is designed without IF resistance ($R_{IF} = \infty$), so as to optimize the voltage gain and the noise performance. Similarly to the SD-2PPM, the zero-IF DD-2PPM input impedance depends upon the RF phase shift. In order to overcome this issue, DD-2PPMs should be used as heterodyne downconvert devices. Considering the LO and the RF signals defined in equations 3.1 and 3.2, and applying the charge conservation model, the heterodyne DD-2PPM input impedance is represented by

$$Z_{in,n,SD-2PPM}\big(n(\omega_{LO} \pm \omega_{IF})\big) = 2R_{sw} + \left(\frac{R_{sh,n}(n\omega_{LO})}{2}\right) || Z_{CIF}(\pm n\omega_{IF}) \tag{3.47}$$

Where $\gamma = 2/\pi^2 \approx 0.203$ and

$$R_{sh,n,DD-2PPM}(n\omega_{LO}) = \frac{4\gamma}{(n^2 - 2\gamma)}(R_a + 2R_{sw}) \tag{3.48}$$

Similarly to the SD-2PPM, the resulting RF DD-2PPM input impedance follows a BPF shape centered at the LO frequency as a function of the IF frequency. Following the same analysis performed for the SD-2PPM structure and considering $R_{IF} = \infty$, the minimum switch resistance to provide RF input impedance matching is equal to

$$R_{sw,DD-2PPM,min} = \frac{1-4\gamma}{2} R_a \approx 0.094 R_a \tag{3.49}$$

This represents half of the SD-2PPM minimum switch resistance (equation 3.16).

3.3.2. DD-2PPM frequency response

Following the same SD-2PPM development, the maximum DD-2PPM out-of-band rejection for $\omega_{offset} = \infty$, $\omega_{IF} = 0$, $R_{IF} = \infty$ and $\varphi_{RF} = 0$ is

$$IRR_{DD-2PPM,max} = \frac{R_a + 2R_{sw,DD-2PPM,match}}{4R_{sw,DD-2PPM,match}} \approx 10dB \tag{3.50}$$

Thanks to the possibility of using half the minimum SD-2PPM switch resistance, the fully differential 2-PPM reaches the same SD-2PPM interference rejection. In terms of the output frequency response, the heterodyne DD-2PPM output voltage gain for $R_{IF} = \infty$ is

$$\left|A_{v,DD-2PPM}(\omega_{IF})\right| = \left|\frac{A_{v0,DD-2PPM}}{1 + j\frac{\omega_{IF}}{\omega_{BW,DD-2PPM}}}\right| = \frac{\left|A_{v0,DD-2PPM}\right|}{\sqrt{1 + \left(\frac{\omega_{IF}}{\omega_{BW,DD-2PPM}}\right)^2}} \tag{3.51}$$

Where

$$A_{v0,DD-2PPM} = \frac{\pi\gamma(R_a + 2R_{sw})}{2(\gamma R_a + R_{sw})} \tag{3.52}$$

$$\omega_{BW,DD-2PPM} = \frac{1}{\pi\gamma(R_a + 2R_{sw})C_{IF}} \tag{3.53}$$

Replacing equation 3.49 in 3.51, the maximum DD-2PPM passive voltage gain provided is $2.11dB$. Given the single-to-differential transformation, the SD-2PPM presents $6dB$ higher voltage gain than the fully differential 2-PPM configuration.

Considering the $-3dB$ bandwidth expression given by equation 3.53, the RF input quality factor can be written as shown by equation 3.54. Considering the two extra IF capacitors used on the fully differential architecture and considering the factor of two between the SD-2PPM and the DD-2PPM quality factor, the fully differential 2-PPM requires a four times larger load IF capacitor to achieve the same SD-2PPM quality factor. This behavior can rapidly become a limitation due to the extra silicon area required.

$$Q_{DD-2PPM} = \frac{\omega_{RF}}{2\omega_{BW,DD-2PPM}} = \frac{1}{2}\omega_{RF}\pi\gamma(R_a + 2R_{sw})C_{IF} \tag{3.54}$$

3.3.3. DD-2PPM noise analysis

Similarly to the SD-2PPM, the in-band DD-2PPM NF for an RF input impedance matched DD-2PPM $\left(Z_{in,DD-2PPM}(\omega_{IF} = 0) = R_a\right)$ is given by equation 3.55. A minimum NF of 4.66dB is obtained for $R_{sw} = R_{sw,DD-2PPM,min} \approx 0.094R_a$. Again, this result is equal to that of the SD-2PPM thanks to the advantage using a switch resistance twice smaller than the one of the SD-2PPM.

$$F_{DD-2PPM,match} = \sum_{n=1,3,5\ldots}^{\infty} \frac{2(R_a + 2R_{sw})}{n^2(R_a - 2R_{sw})} \tag{3.55}$$

DD-2PPMs are an efficient solution to provide moderate passive voltage gain and high-Q band-pass filtering, while providing common mode rejection at its input. However, compared to SD-2PPMs, they prove less efficient in terms of voltage gain and silicon area, taking into account the four times larger IF capacitor required. The two extra paths also lead to a power consumption increase due to the two extra buffer stages required to drive the switches. These architectures should be implemented as heterodyne mixing devices and should be used at intermediate frequencies where the extra buffer power requirements would not affect the overall receiver power budget.

3.4. Parallel 2-Path Passive Mixers

The transparency and bidirectional behavior of the N-path passive mixers suggest that they also may be used as simple band-pass filters, by using only their input RF node in a parallel configuration. Hence, by using multiple N-PPM in parallel, very high narrow band-pass filtering with very high out-of-band attenuation can be obtained.

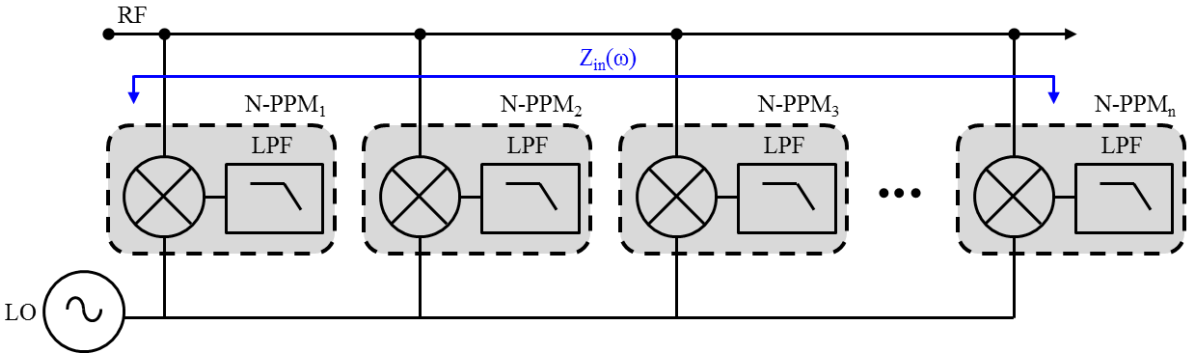


Figure 3.17. n-parallel N-PPM block diagram.

Figure 3.17 shows an n-parallel N-PPM block diagram configuration. This architecture presents an RF input node common to all the n-passive mixers. All N-PPMs are equally designed and are driven by the same N-phase LO signal. The parallel configuration superposes the frequency response of each N-PPM, thus the Q-factor and the IRR are optimized as the number of parallel N-PPM is increased. However, given their common RF input node, the equivalent input impedance is degraded as the number of mixers is increased. One way to overcome this issue is to increase the switch resistance; nevertheless, this solution brings higher noise figure, lower voltage gain and lower interference rejection.

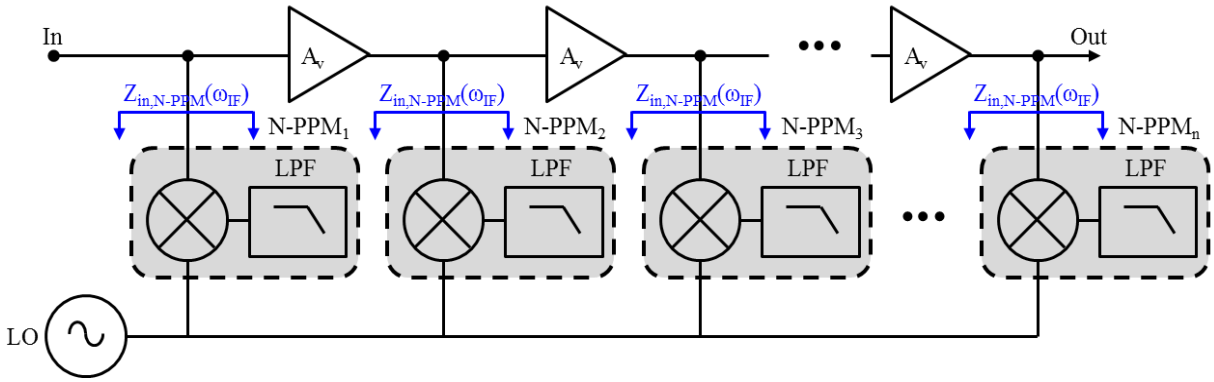


Figure 3.18. Amplifier with parallel N-PPM load in cascaded n-stage configuration.

A fair way to overcome this problem without degrading the N-path mixer performance is to isolate each cascaded parallel N-PPM. A very simple implementation of this solution can be done by using an active amplification stage between each N-PPM as shown in Figure 3.18. This amplifier presents three main advantages: first, it provides isolation between each cascaded parallel stage. Second, it presents a very high output impedance (as for example, by using common source amplifiers) that is used by the N-PPM as source resistance, in order to reduce the IF capacitance value, while boosting the Q-factor and the IRR of the system. Third, thanks to its very high input impedance, it does not load the N-PPM of the previous stage. These three advantages are given at the obvious drawback of extra power consumption. In the case of ultra-low power systems using 2-path mixer configurations, three additional drawbacks appear: the voltage gain RF phase shift dependence for zero-IF mixers, the non-negligible influence of the MOS switch transistor parasitic capacitances and the LO upconvert modulation.

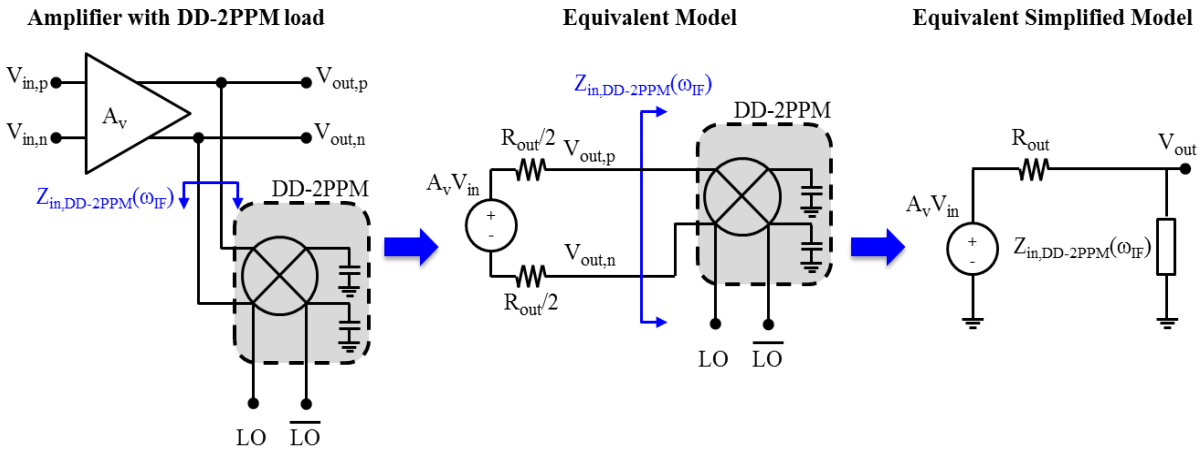


Figure 3.19. Circuit model of an amplifier stage loaded with a DD-2PPM (a), correspondent equivalent model (b) and equivalent impedance simplified model (c).

Figure 3.19.a presents an example of this solution showing a single stage of an amplifier loaded by a DD-2PPM. The amplifier stage is modeled as an ideal voltage source representing the unloaded voltage gain $A_v = G_m R_{out}$, in series with a differential output resistance R_{out} (Figure 3.19.b). The differential amplifier stage model is replaced by its equivalent single-ended circuit model and the fully differential passive mixer is represented as an equivalent frequency dependent input impedance $Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF})$ as defined

in equation 3.47 (Figure 3.19.c). Considering the equivalent output impedance divider formed by R_{out} and $Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF})$, the amplifier output voltage gain is written as

$$\left|A_{v,eq}(\omega_{LO} \pm \omega_{IF})\right| = |A_v| \left|\frac{Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF})}{Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF}) + R_{out}}\right|$$

$$= G_m \left|\frac{R_{out} Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF})}{Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF}) + R_{out}}\right| \quad (3.56)$$

The key point of this configuration is the large interference rejection provided at the output of the amplifier. Equation 3.56 shows that gain optimization is provided for very large mixer input impedance values where $Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF}) \gg R_{out}$ and $A_{v,eq} \approx A_v$. However, this is only provided by setting a large switch resistance value, meaning that the interference rejection ratio would be degraded down to $0dB$ (see equation 3.50). This effect appears as a trade-off between voltage gain and interference rejection. In the case of ULP receivers, voltage gain optimization can be achieved by the simple implementation of unloaded amplifiers. If filtering is required, the 2-path mixer can be designed such as to provide matching to the amplifier output impedance at its resonant frequency ω_{LO}, while presenting minimum R_{sw} for IRR optimization. In this case, the maximum voltage gain provided at ω_{LO} is $A_v/2$ and the maximum IRR is nearly $10dB$ (Figure 3.20). Given the 2-path mixer RF phase shift dependence, this architecture is not recommended to be used in a zero-IF configuration, unless continuous phase control is provided.

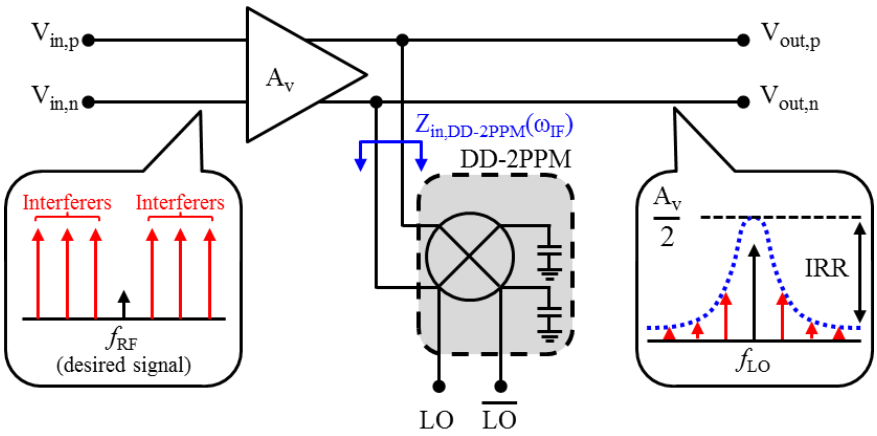


Figure 3.20. Amplifier with a parallel DD-2PPM load with $f_{LO} = f_{RF}$, $\varphi_{RF} = 0$ and $Z_{in,DD-2PPM}(\omega_{LO}) = R_{out}$.

Influence of the MOS switch transistor parasitic capacitances:

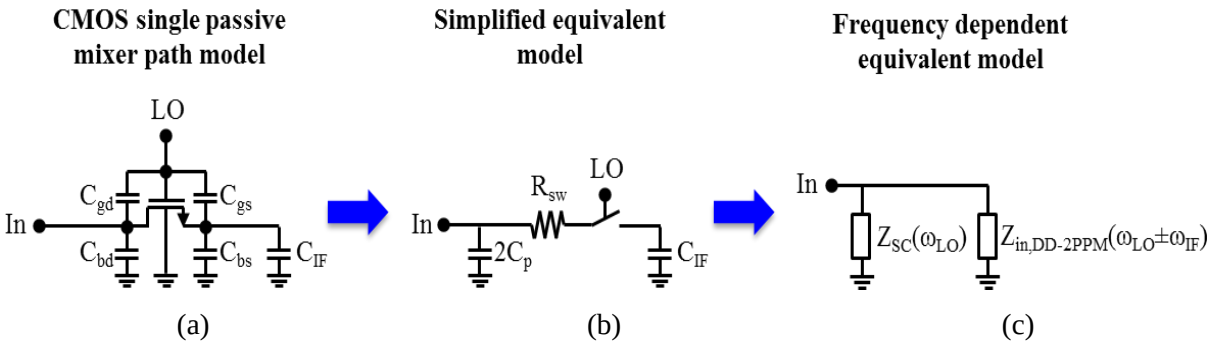


Figure 3.21. CMOS single passive mixer path model (a), simplified equivalent model (b) and frequency dependent equivalent model.

The direct consequence of working with N-path filters with very high source resistances (in this case, the amplifier output impedance R_{out}) and very high N-PPM input impedances ($> 100k\Omega$), is the non-negligible effect of the on-state MOS switch transistor parasitic capacitances (C_{gd}, C_{bd}, C_{gs} and C_{bs}).

In ideal switched-capacitor systems, the charge transferred to the capacitor C over a clock cycle T_{CLK}, can be modeled as an equivalent frequency dependent impedance equal to $1 / f_{CLK}C$ [Razavi01]. In the same way, neglecting the voltage drop across the switch on-resistance, the parasitic capacitances of the MOS switches used on the DD-2PPM, generates a frequency dependent parasitic impedance in parallel to the input impedance as shown in Figure 3.21. Assuming the effective parasitic capacitance C_p seen at the N-MOS drain and source terminals $(C_p = C_{gd} + C_{bd} = C_{gs} + C_{bs})$, the DD-2PPM equivalent four paths switched-capacitor impedance is equal to

$$Z_{sc,DD-2PPM}(\omega_{LO}) = \frac{\pi}{2\omega_{LO}C_p} \tag{3.57}$$

The resulting DD-2PPM input impedance is therefore written as

$$Z'_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF}) = Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF}) || Z_{sc,DD-2PPM}(\omega_{LO}) \tag{3.58}$$

Where $Z_{in,DD-2PPM}(\omega_{LO} \pm \omega_{IF})$ is the DD-2PPM input impedance derived in equation 3.47. Figure 3.22 shows the analytical and simulated DD-2PPM input impedance as a function of the LO frequency evaluated at $\omega_{IF} = 0$ $(\omega_{LO} = \omega_{RF})$ under the influence of N-

MOS switch transistor parasitic capacitance. The source resistance modeling the amplifier output impedance (R_{out}) is set to $100k\Omega$. The switch on-resistance is chosen such as to provide matching impedance to R_{out}. The common mode of the system is set to $V_{dd}/2$. The LO squared signal is defined between 0 and V_{dd}. The MOS transistor is designed such as to provide the desired on-resistance at the on-state with $V_{gs} = V_{gs,on}$ and a very high off-impedance ($\sim 10M\Omega$ including MOS on-resistance and parasitic capacitances) with respect to R_{out}, to ensure a good "open circuit" operation at the off-state $(V_{gs} = V_{gs,on})$. Good matching between analytical and simulated results is obtained. As the LO frequency increases, the equivalent input impedance is degraded, following a LPF shape.

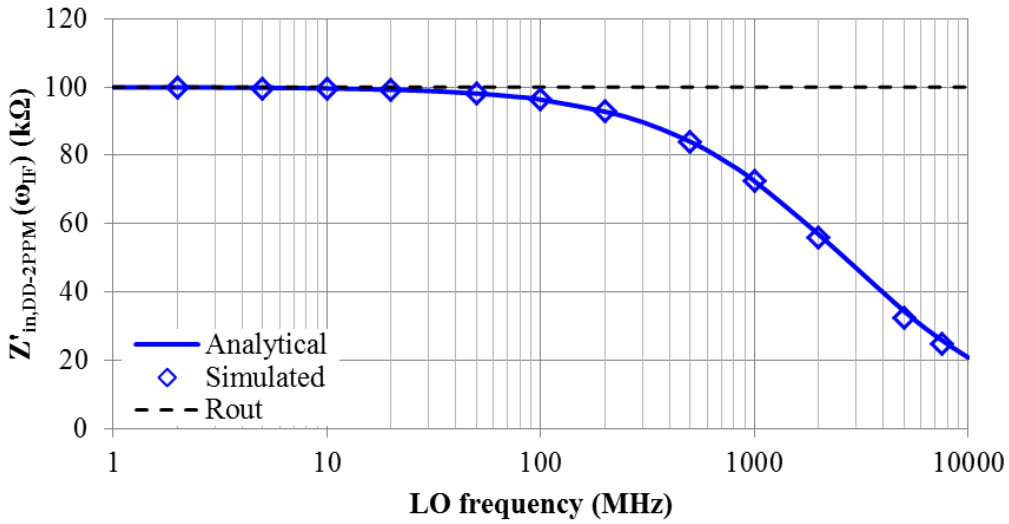
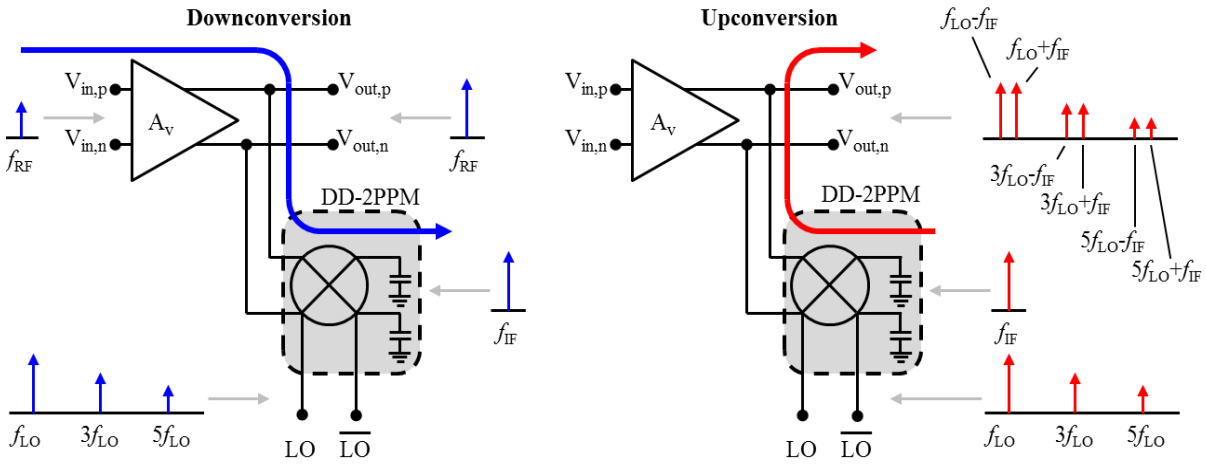


Figure 3.22. Fully differential 2-PPM input impedance as a function of the LO frequency, evaluated at $\omega_{IF} = 0$, under the influence of MOS switch transistor parasitic capacitance. $R_{out} = 100k\Omega$, $R_{sw} = 6.92k\Omega$, $C_{IF} = 10pF$, $C_p = 475aF$, $V_{gs,on} = -V_{gs,off} = 250mV$, $V_{cm} = V_{dd}/2 = 250mV$.

Effects of the LO upconvert modulation:

Another interesting behavior that has to be analyzed in N-PPMs is the clock modulation generated at its proper input node. The transparency of N-path passive mixers allows current to flow in both directions: from the RF input to the IF output (downconversion) and from the IF output to the RF input (upconversion). This last behavior may result in an RF input signal modulation, generated by the IF signal upconversion through mixing with the LO signal, and may become handicapping for parallel heterodyne N-PPM band-pass filter configurations. In order to properly explain this behavior, we analyze the amplifier stage loaded by a DD2PPM in two different steps: one for the downconversion effect (Figure 3.23.a) and another for the upconversion effect (Figure 3.23.b).



(a) (b)

Figure 3.23. VGA and fully differential 2-PPM downconversion and upconversion frequency response.

In the case of the downconversion effect, the desired RF input signal $V_{RF}(t)$ (defined by equation 3.2) is first amplified through the amplifier providing a voltage gain $A_{v,eq}(\omega_{IF})$ (see equation 3.56) and then downconverted to the IF-band by mixing with the squared LO signal $V_{LO}(t)$ (defined by equation 3.1). The sharp low-pass filter loading the mixer attenuates the high-frequency mixing component. The IF downconverted output signal is therefore given by

$$V_{IF,down}(t) = \left|A_{v,eq}(\omega_{IF})\right| V_{RF}(t) V_{LO}(t)$$

$$= \frac{\left|A_{v,eq}(\omega_{IF})\right| A_{RF} A_{LO}}{\pi} cos\big((\omega_{RF} - \omega_{LO})t + \varphi_{RF}\big)$$

$$= \frac{\left|A_{v,eq}(\omega_{IF})\right| A_{RF} A_{LO}}{\pi} cos(\omega_{IF} t + \varphi_{RF}) \quad (3.59)$$

The upconversion effect is analyzed from the IF output to the RF input of the DD-2PPM. The bidirectional behavior of passive mixers indicates that the previously downconverted output signal $V_{IF}(t)$ can be also upconverted to the input, by mixing with the LO clock frequency. The upconverted signal found at the input of the DD-2PPM is given by

$$V_{RF,up}(t) = V_{IF,down}(t) V_{LO}(t)$$

$$= \sum_{n=1,3,5\ldots}^{\infty} \frac{\left|A_{v,eq}(\omega_{IF})\right| A_{RF} A_{LO}^2}{n\pi^2} \big[cos\big((n\omega_{LO} - \omega_{IF})t - \varphi_{RF}\big) + cos\big((n\omega_{LO} + \omega_{IF})t + \varphi_{RF}\big)\big] \quad (3.60)$$

The overall system frequency response is given by the combination of the RF desired signal and the LO upconvert effect. The resulting amplifier output voltage (input of the DD-2PPM) is written as

$$V_{out}(t) = \left|A_{v,eq}(\omega_{IF})\right| V_{RF}(t) + V_{RF,up}(t)$$

$$= \left|A_{v,eq}(\omega_{IF})\right| V_{RF}(t) + V_{IF,down}(t) V_{LO}(t) \quad (3.61)$$

The modulation of the RF input signal by the upconverted effect containing the LO and IF signals is here defined as the *LO upconvert modulation effect*. For a zero-IF N-PPM architectures, the mixer input signal is modulated by the LO and a DC voltage, representing the IF downconverted signal. Since $\omega_{RF} = \omega_{LO}$, the RF input signal will not have any extra IF frequency components. On the other hand, for heterodyne N-PPM configurations, the LO upconvert modulation generates an input signal modulation, injecting an IF sinusoidal envelope and a high LO frequency component to the desired RF signal. This effect may disturb the band-pass filtering of the desired RF signal.

Figure 3.24 presents the PSS single-tone transient simulation response for an amplifier loaded by a parallel DD-2PPM, using the same configuration as shown in Figure 3.19, for $f_{RF} = 10.5MHz$, $f_{LO} = 10MHz$, and $f_{IF} = 500kHz$. Figure 3.24.a shows the sinusoidal RF

input desired signal. As we can observe the amplified signal at the output of the amplifier (Figure 3.24.b) has not only the RF input signal tone but a modulated component coming from the upconvert modulation of the IF signal (Figure 3.24.c) and the LO square waveform (Figure 3.24.c). This example clearly shows the LO upconvert modulation effect in parallel N-PPM configurations. For optimum band-pass filtering performance, accurate LO signals should be used in order to perfectly track the RF frequency. Moreover, the system should be able to control the RF phase shift in order to avoid signal attenuation. In architectures with non-accurate LO signals, this behavior may be overcome by using a second IF-band in order to eliminate the influence of both LO and IF upconvert components. An example of this solution is proposed in Chapter 5, section 5.1.4.

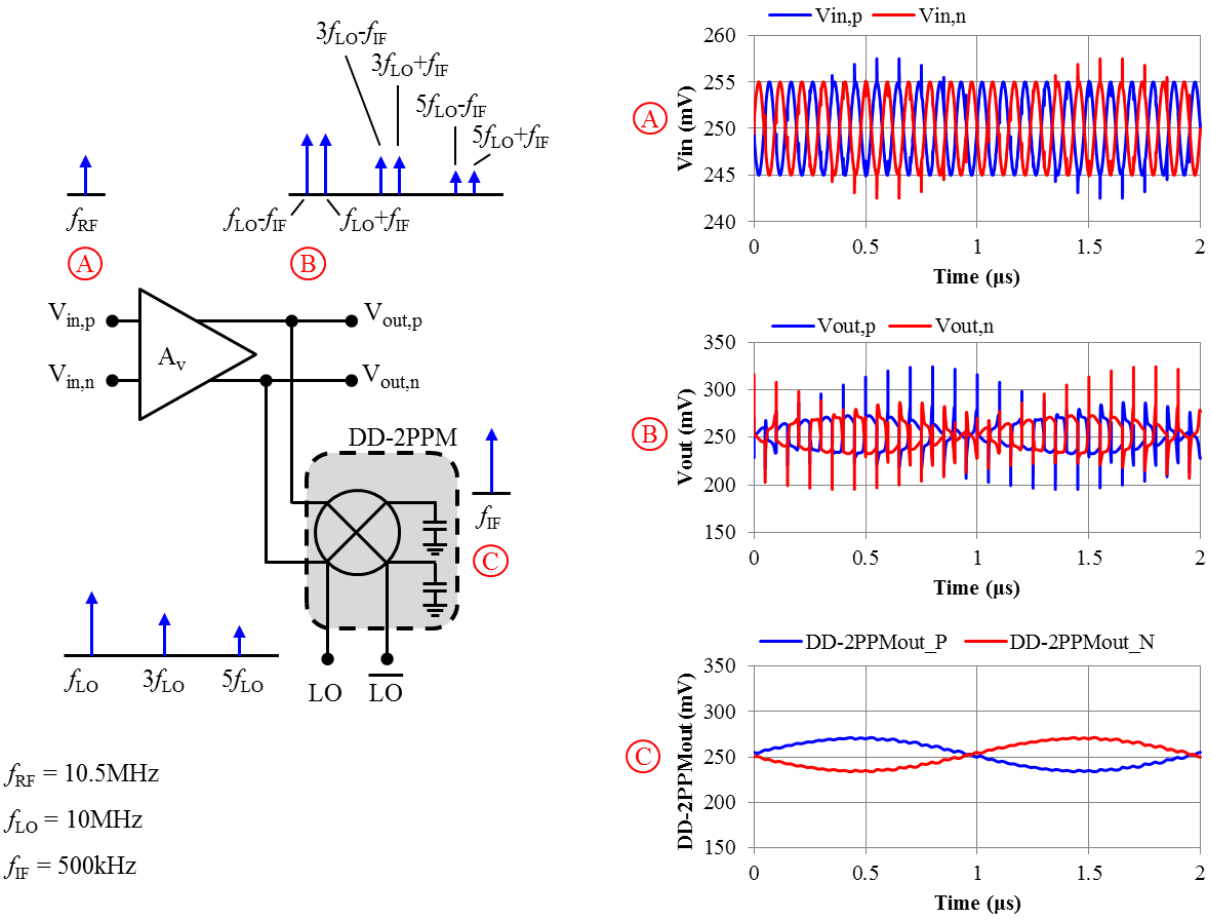


Figure 3.24. VGA and fully differential 2-PPM and its correspondent PSS single-tone transient simulation response for an amplifier loaded by a parallel DD2PPM, with $A_{RF} = 10mV$, $A_{in} = 5mV$, $f_{RF} = 10.5MHz$, $f_{LO} = 10MHz$, $f_{IF} = 500kHz$, $R_{out} = 100k\Omega$, $R_{sw} = 12.9k\Omega$, $C_{IF} = 1pF$, $\varphi_{RF} = 0$, $A_{v,eq}(f_{IF} = 500kHz) = 8.5dB$, $A_{v,DD-2PPM}(f_{IF} = 500kHz) = 2.35dB$, $V_{gs,on} = -V_{gs,off} = 250mV$, $V_{cm} = V_{dd}/2 = 250mV$.

To summarize, parallel 2-PPM architectures enable the possibility of achieving very high-Q band-pass filtering and very high IRR by means of cascading multiple parallel 2-PPM stages. However, given their common input node, this technique results in input impedance degradation. To overcome this, the configuration of the amplifier loaded by a parallel DD-2PPM appears as the simplest structure to provide isolation between each parallel N-path filters. Given the RF phase shift 2-PPM frequency response dependence, zero-IF configuration should be avoided if no phase shift control is guaranteed. Optimum band-pass filtering performance is obtained by using accurate LO signals set at the desired RF input signal. Given the transparency behavior of these N-PPM, heterodyne architectures are subject to the LO upconvert modulation effect. This behavior has to be carefully taken into account in order to avoid distortion in the desired RF input signal. From the stand point of energy, parallel N-PPM architectures should be used at intermediate frequencies in order to keep the required power consumption negligible with respect to the overall system power consumption.

3.5. Chapter conclusions

This chapter presents the principles of integrated 2-path passive mixers targeting ultra-low power consumption and very high BPF Q-factor (> 100), for sensitivity and interferer rejection enhancement in WuRx for WSN applications.

Three main 2-path passive mixer architectures are analysed: the SD-2PPM, the DD-2PPM and the parallel 2-PPM. Two major drawbacks limit the functionality of these 2-path mixer devices: the RF phase shift dependence for zero-IF configurations and the minimum switch resistance required for RF input impedance matching. In order to overcome the phase shift drawback, heterodyne configuration can be used. However, the minimum switch resistance stills a limitation that cannot be resolved with a low power consumption budget.

From the three configurations the SD-2PPM is the simplest configuration providing the advantage of single-to-differential conversion, which is commonly required at receiver's front-end. This architecture offers the best performances in terms of power consumption, voltage gain, Q-factor, IRR, NF and IF capacitor silicon area. It is suited for high frequency

implementations, such as RF front-end receivers. On the other hand, compared to the SD-2PPM, the DD-2PPM configuration presents the advantage of input common mode rejection. However, its voltage gain is degraded by a factor of two and its power consumption is increased, due to the two extra buffer stages required. This fully differential architecture may be used at intermediate frequencies, where the extra buffer power requirements would not affect the receiver overall power budget. Finally, the parallel 2-PPM architecture enables the possibility to achieve extreme high-Q band-pass filtering and very high IRR. This configuration have to be judiciously designed in order to tolerate the zero-IF RF phase shift dependence and the LO upconvert modulation effect. For power consumption optimization, parallel 2-PPM configurations should be used at intermediate frequencies.

To conclude, 2-path passive mixers appears as well-suited low-power devices for WuRx applications, opening the possibility to generate very high Q band-pass filtering (> 100) with high interference rejection by means of integrated electronic devices, while avoiding any costly and bulky external piezoelectric resonators.

Chapter 4

N-Path Filter Based WuRx Front-End

In order to validate the N-path theory that has been presented in the previous Chapter, a first WuRx front-end prototype circuit is designed. The objective of this circuit is to demonstrate the possibility of generating very high-Q RF band-pass filters by using a simple single-to-differential 2-PPM (SD-2PPM) architecture. Q-factor enhancement is provided through two methodologies: the implementation of a passive impedance transformation technique which boosts the RF input impedance seen by the first section of the receiver (the SD-2PPM); and the implementation of very high value IF capacitors to reduce the effective bandwidth of the band-pass filter generated at the SD-2PPM input. In the case of this circuit, the high value IF-capacitors are provided by external Surface Mounted Device (SMD) components, embedded in the cavity of the Ball Grid Array (BGA) packaging, together with the IC die. Power efficiency is obtained by applying different low power techniques previously discussed in Chapter 2, such as low voltage power supply, subthreshold CMOS operational modes, current reuse architectures, passive RF front-ends and bandwidth reduced low-power amplifiers.

This chapter presents a full analysis and characterization of an N-path filter based WuRx front-end prototype circuit. Measurement results of the proposed circuit designed in 65nm CMOS technology are presented. This section concludes with a comparison with the State-of-the-Art WuRx front-end architectures.

4.1. WuRx Front-End architecture

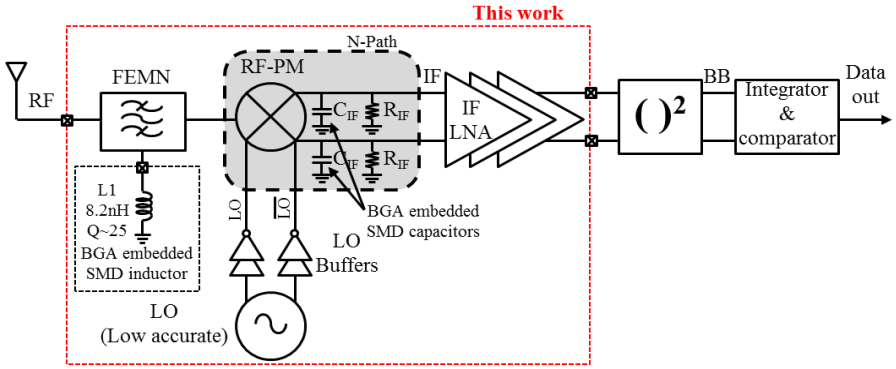


Figure 4.1. N-Path filter based wake-up receiver front end diagram block diagram.

Figure 4.1 shows the proposed WuRx front-end block diagram. The architecture is designed following an uncertain-IF frequency plan presented in Figure 4.2. The RF input is directly connected to a LC Front-End Matching Network (FEMN) to provide impedance matching to the RF input. At the FEMN output, an heterodyne SD-2PPM is connected in order to provide RF signal downconversion to the IF-band, through mixing with the LO signal. The passive mixer is driven by a low power, but low accuracy unlocked ring oscillator. Given the LO inaccuracy, the resulting downconvert IF frequency has a frequency uncertainty nature $(\omega_{IF} \pm \Delta\omega_{IF} = \omega_{RF} - \omega_{LO} \pm \Delta\omega_{LO})$. Unlike standard LNA based receivers, this WuRx front-end optimizes its power consumption by implementing a bandwidth reduced pseudo IF-LNA placed at the IF SD-2PPM output. After the IF-LNA, two low-power fully differential amplifiers are implemented. To alleviate the IF-uncertainty, envelope detection is performed as a last demodulation to DC. For excess noise reduction an integration stage is introduced in between the envelop detector and the comparator [Zhou]. Low data node identification decoding is performed to wake-up the main radio only when requested. This WuRx front-end is designed with a $500mV$ power supply voltage in order to take profit of the CMOS weak-inversion boosted g_m/I_{ds} efficiency.

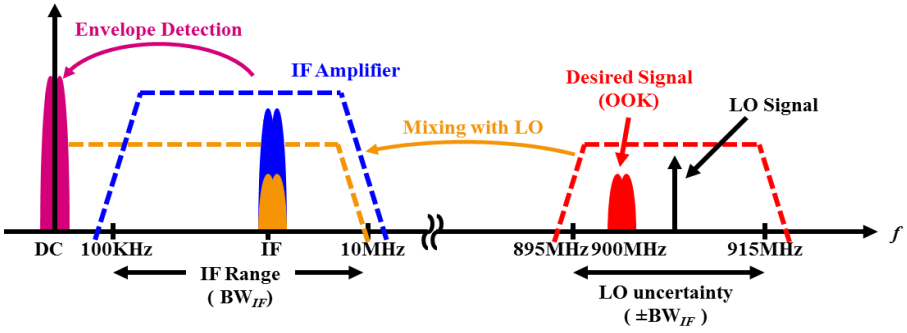


Figure 4.2. Frequency plan of the proposed WuRx front-end.

4.1.1. Passive RF Front-End

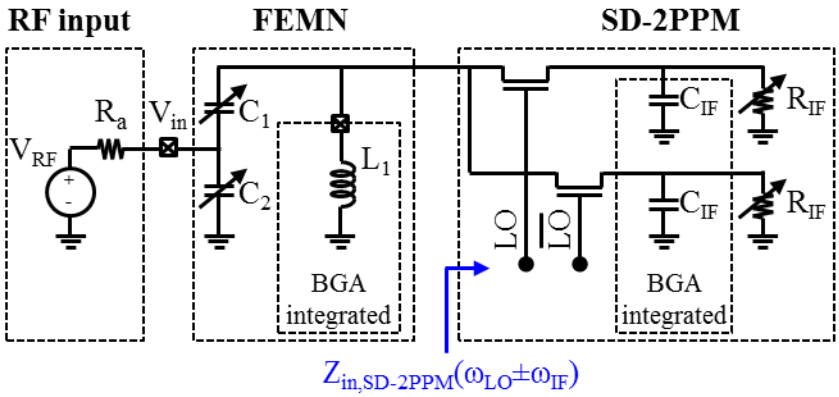


Figure 4.3. Passive front-end circuit model.

Figure 4.3 presents the passive Front-End (FE) circuit model which is constituted of a front-end LC matching network loaded by a SD-2PPM. The goal of the FEMN stage is to provide impedance matching to the RF input, while providing passive voltage gain and RF input impedance enhancement to the SD-2PPM. Impedance enhancement is obtained through the capacitor divider network, which boosts the antenna impedance from 50Ω to roughly $1k\Omega$. Here, an inductance is introduced to compensate the capacitive behavior of the capacitor divider. In order to compensate the process and temperature variations while still providing impedance matching to the antenna ($Z_a = Z_{in,FEMN}(\omega_0)$) at the desired resonant frequency ω_0, C_1 and C_2 are implemented as 4-bits capacitor networks. At the output of the FEMN, the SD-2PPM downconverts the desired RF signal to the IF-band. High Q-factor band-pass filter response is obtained thanks to the high output impedance provided by FEMN ($Z_{out,FEMN}(\omega_{RF})$) to the SD-2PPM and the use of high value IF capacitors. Given the second order band-pass filter nature of the LC network, the noise performance of the 2-path mixer architecture is extended by providing some filtering attenuation at high order LO harmonics ($n = 3,5,7 \ldots$).

In order to have a better understanding of the FEMN, we first analyze the system without any load at its output, and then we proceed to the analysis taking into account the equivalent input impedance provided by the SD-2PPM.

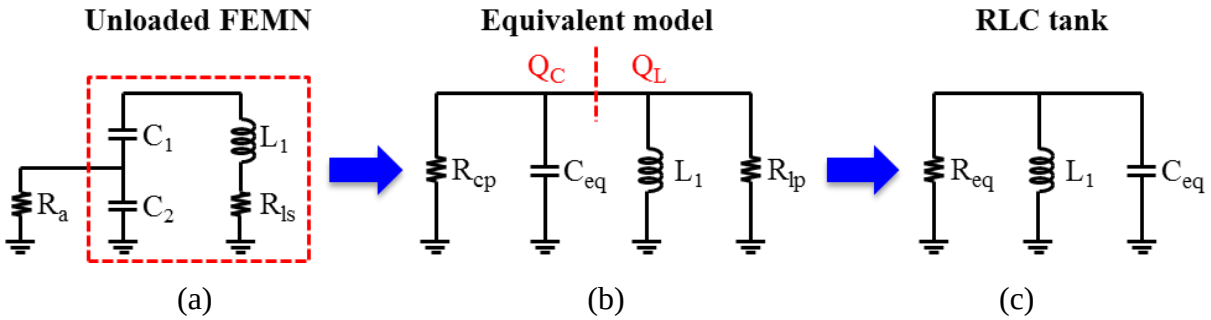


Figure 4.4. RF input impedance – unloaded front-end matching network and its equivalent RLC tank model.

In the case of the unloaded FEMN, we first consider the non-idealities of the inductor, whose equivalent model is composed of the inductance L_1 placed in series with a parasitic series resistance R_{ls} (see Figure 4.4.a). The quality factor of the inductor is defined as $Q_L = \omega L_1/R_{ls}$. By passive impedance transformation of the series inductive network can be modeled as an equivalent parallel network where $L_p \approx L_1$ and $R_{lp} = R_{ls}(1 + Q_L^2)$ (see Figure 4.4.b) [Razavi01]. Considering $Q_L^2 \gg 1$ and assuming the RF input impedance (the antenna impedance) as being a purely resistive impedance where $|Z_s| = |Z_a| = |R_a + jX_a| = R_a$ with $X_a \approx 0$, input impedance matching is provided to the RF input for

$$C_1 \approx \frac{1}{\omega}\left(\frac{Q_L + \sqrt{\frac{R_a Q_L}{\omega L_1} - 1}}{\omega L_1 Q_L - R_a}\right) \tag{4.1}$$

$$C_2 \approx \frac{1}{\omega R_a}\left(\frac{(R_a + \omega L_1 Q_L)\sqrt{\frac{R_a Q_L}{\omega L_1} - 1} + 2(R_a Q_L - \omega L_1)}{R_a + \omega L_1\left(Q_L + \sqrt{\frac{R_a Q_L}{\omega L_1} - 1}\right)}\right) \tag{4.2}$$

From the stand point of output impedance, the FEMN can be modeled as an equivalent RLC tank circuit as shown in Figure 4.4.c. Here, the capacitor divider network composed of C_1, C_2 and R_a, is modeled as an equivalent capacitance (C_{eq}) in parallel with an equivalent parallel resistance (R_{cp}) (see Figure 4.4.b).

$$C_{eq} = \frac{C_1 C_2}{C_1 \frac{(\omega R_a C_2)^2}{(1 + (\omega R_a C_2)^2)} + C_2} \tag{4.3}$$

$$R_{cp} = \frac{R_a}{1 + (\omega R_a C_2)^2}(1 + Q_C^2) \tag{4.4}$$

Where,

$$Q_C = \frac{1}{\omega R_a C_1} + \omega R_a C_2 \left(1 + \frac{C_2}{C_1}\right) \tag{4.5}$$

At the resonant frequency (ω_0), the capacitive and the inductive quality factors are equal $(Q_L = Q_C)$ [Cook02] and the equivalent FEMN output impedance is given by the equivalent resistance R_{eq}, resulting from the parallel configuration between R_{cp} and R_{lp}.

$$Z_{out,FEMN}(\omega_0) = R_{eq}(\omega_0) \approx \omega_0 L_1 \left(\frac{Q_L Q_C}{Q_L + Q_C}\right) = \frac{\omega_0 L_1 Q_L}{2} \tag{4.6}$$

Given the passive impedance transformation, the passive voltage gain provided by the FEMN from its input node voltage (V_{in}) to its output is defined by

$$\left|A_{v0,FEMN}(\omega_0)\right| \approx 2\sqrt{\frac{\omega_0 L_1}{R_a Q_L}}\left(\frac{Q_L Q_C}{Q_L + Q_C}\right) \approx \sqrt{\frac{\omega_0 L_1 Q_L}{R_a}} \tag{4.7}$$

To characterize the noise figure response, we consider the voltage gain provided from the RF input voltage node (V_{RF}) to the FEMN output $A_{v0,Ra}$.

$$\left|A_{v0,Ra}(\omega_0)\right| \approx \frac{1}{2}\sqrt{\frac{\omega_0 L_1 Q_L}{R_a}} \tag{4.8}$$

Therefore, at the resonant frequency the noise factor is given by equation 4.9, which represents $3dB$ of noise figure.

$$F_{0,FEMN}(\omega_0) = \frac{Z_{out,FEMN}}{A_{v0,Ra}^2 R_a} \approx 1 + \frac{Q_L}{Q_C} = 2 \tag{4.9}$$

In order to characterize the voltage response for the complete passive front-end, we first analyze the case where the FEMN is loaded by a zero-IF SD-2PPM where the RF phase shift is equal to zero $(\varphi_{RF} = 0)$, and then we derive the expression for the heterodyne SD-2PPM configuration.

When loading the FEMN with the zero-IF SD-2PPM, the equivalent inductive quality factor (Q_L') is degraded. Assuming the FEMN resonant frequency equal to that of the SD-2PPM ($\omega_0 = \omega_{LO}$), the resulting equivalent quality factor is written as

$$Q_L' = \frac{R_{lp}||Z_{in0,fund,SD-2PPM}}{\omega_{LO}L_1} = \frac{Q_L}{1 + \frac{\omega_{LO}L_1Q_L}{Z_{in0,fund,SD-2PPM}}} \tag{4.10}$$

Where $\gamma = 2/\pi^2 \approx 0.203$ and $Z_{in0,fund,SD-2PPM}$ is the zero-IF SD-2PPM input impedance evaluated at ω_{LO} with $\varphi_{RF} = 0$ (equation 3.18). In this case, the RF input impedance (R_a) from equation 3.18 is replaced by the equivalent FEMN output impedance seen by the SD-2PPM at the resonant frequency$\left(R_{cp}||R_{lp}\right)$. Therefore, considering the zero-IF SD-2PPM voltage gain defined in equation 3.37 and replacing R_a by $R_{cp}||R_{lp}$, the zero-IF front-end voltage gain provided at the SD-2PPM output is

$$\begin{aligned}\left|A_{v0,FE}(\omega_{IF} = 0)\right| &= \left|A_{v0,FEMN}(\omega_{LO})\right|\left|A_{v0,SD-2PPM}(\omega_{IF} = 0)\right| \\ &\approx \sqrt{\frac{\omega_{LO}L_1Q_L'}{R_a}}\left(\frac{2\pi\gamma\left(R_{cp}||R_{lp} + R_{sw}\right)R_{IF}}{2R_{sw}\left(R_{cp}||R_{lp} + R_{sw}\right) + R_{IF}\left(2\gamma R_{cp}||R_{lp} + R_{sw}\right)}\right)\end{aligned} \tag{4.11}$$

In the case of an heterodyne configuration, considering equation 3.38 and considering a large FEMN bandwidth compared to that of the SD-2PPM for which $Q_L'(\omega_0) \approx Q_L'(\omega_{RF})$, the in-band front-end voltage gain provided at the IF SD-2PPM output is

$$\begin{aligned}\left|A_{v,FE}\right| &= \left|A_{v,FEMN}(\omega_{RF})\right|\left|A_{v,SD-2PPM}(\omega_{IF})\right| \\ &\approx \sqrt{\frac{\omega_{RF}L_1Q_L'}{R_a}}\left(\frac{\frac{2\pi\gamma\left(R_{cp}||R_{lp} + R_{sw}\right)R_{IF}}{2R_{sw}\left(R_{cp}||R_{lp} + R_{sw}\right) + R_{IF}\left(2\gamma R_{cp}||R_{lp} + R_{sw}\right)}}{\sqrt{1 + \omega_{IF}^2\left(\frac{2\pi\gamma\left(R_{cp}||R_{lp} + R_{sw}\right)R_{IF}C_{IF}}{2\left(R_{cp}||R_{lp} + R_{sw}\right) + R_{IF}}\right)^2}}\right)\end{aligned} \tag{4.12}$$

This equation sets a trade-off between the maximum achievable voltage gain for both FEMN and SD-2PPM stages with respect to the SD-2PPM switch resistance R_{sw}. In order to maximize the FEMN gain Q_L' and therefore R_{sw} must be maximized. However, in order to optimize the SD-2PPM gain R_{sw} must be set to its minimum value. Another way to boost the

passive voltage gain can be using high-Q high-inductive devices. As an example, for $12dB$ FEMN voltage gain at $900MHz$ with $R_a = 50\Omega$, $\left|Z_{in,DD-2PPM}\right| = 1\text{k}\Omega$ and $L_1 = 10nH$, the inductor quality factor required is 67. In IC design, such high values of inductance and quality factor are not reachable with regular IC metal layers. In order to reach these performances, we took the opportunity to host an external high-Q SMD inductor in the package cavity already available.

In terms of quality factor, assuming a large FEMN bandwidth compared to that of the upconverted SD-2PPM BPF, the equivalent front-end quality factor is

$$Q_{FE} \approx Q_{SD-2PPM} = \frac{\omega_{RF}\pi\gamma\left(R_{cp}||R_{lp}+R_{sw}\right)R_{IF}C_{IF}}{2\left(R_{cp}||R_{lp}+R_{sw}\right)+R_{IF}} \tag{4.13}$$

In order to achieve the highest RF band-pass filter quality factor, the IF capacitance must be maximized. For this, external SMD capacitors are implemented, together with the FEMN SMD inductor, on the cavity of the BGA package.

4.1.2. Local Oscillator

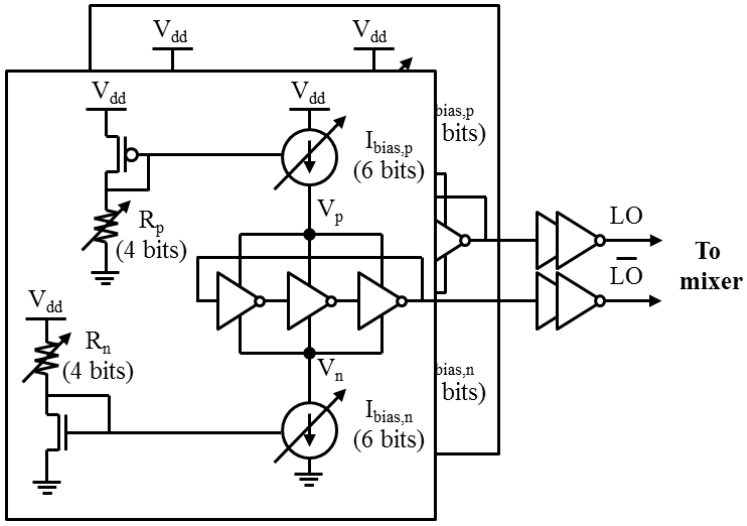


Figure 4.5. Digital controlled oscillator and mixer buffering stages.

Previous works have demonstrated the power efficiency superiority of ring oscillators compared to LC resonators [Pletcher02]. In order to meet our power consumption specification, a $900MHz$ Digital Controlled three-stage ring oscillator (DCO) is proposed

(Figure 4.5). The architecture is composed of two identical parallel ring oscillators symmetrically controlled by a P-MOS and a N-MOS 6-bits current source for linear coarse frequency tuning. For fine frequency tuning, a 4-bits resistance network is introduced at each of the current source voltage biasing blocs. To generate the 50% non-overlapping LO signal, the parallel oscillators are mutually synchronized by connecting their equivalent adjacent logic nodes carrying the same logic phase, through always-on CMOS digital transmission gates. In order to provide the required LO amplitude to drive the mixer, a two-stage buffer is implemented at the output of each ring oscillator. In the case of this architecture the oscillation frequency is given by

$$f_{osc} = \frac{I_{bias}}{6C_{eff}(V_p - V_n)} \tag{4.14}$$

Where C_{eff} is the effective capacitance per stage, I_{bias} is the biasing current and $(V_p - V_n)$ is the effective voltage across the CMOS inverter stages. This equation shows the linear frequency response of the oscillator with respect to the biasing current.

4.1.3. IF Amplification Chain

The IF amplification chain is composed of an IF-LNA and two low-power amplifiers. Figure 4.6 presents the fully-differential current reuse IF-LNA suited for ULP design. The input signal is AC coupled by the R_bC_b high-pass filter to reduce low frequency flicker noise and provide DC input biasing. At high frequencies, C_d is shorted and the input signal is bring to the gate of the P-MOS transistors. In this way, the input signal is amplified by both N and P-MOS transistors halving the power consumption for a given gain. This architecture provides a voltage gain equal to

$$A_{v,IF-LNA} = -\frac{g_{m,n} + g_{m,p}}{g_{ds,n} + g_{ds,p}} \tag{4.15}$$

The IF-LNA is designed to provide low noise amplification over the IF-band of interest, defined between $60kHz$ and $10MHz$. The output of this amplifier is used to bias the input of the following IF-amplifier, thus the R_bC_b network can be omitted in the next stage. The

following two IF amplifiers are designed with the same current reuse architecture consuming four times less power than the IF-LNA.

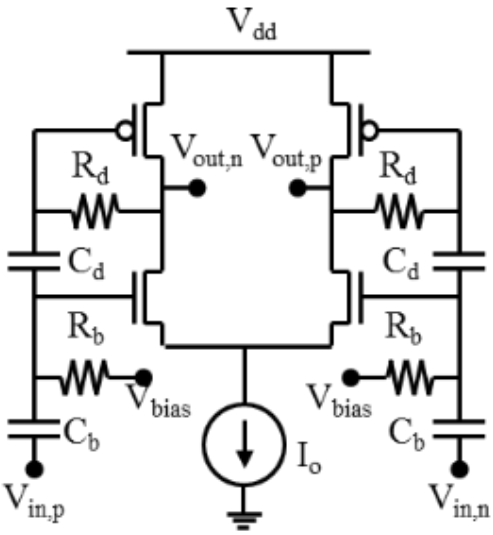


Figure 4.6. Simplified fully-differential current reuse IF-LNA circuit model.

4.2. Wake-up receiver front-end physical implementation

The prototype is implemented in a low-cost and compact co-integrated packaging solution, giving the possibility to integrate the IC die together with the SMD components (L_1 and C_{IF}). This section describes the IC and the packaging implementation, as well as, the measurement results of the prototype.

4.2.1. IC implementation

The circuit implemented in a 65nm Low-Power (LP) CMOS process from STMicroelectronics has an area of $1.5x1.5mm^2$, while the active area is only $120x260\mu m^2$ (Figure 4.7). Flip-chip $1.2V$ RF LP IO pads are implemented in an 8x8 peripheral ring array for Electro-Static Discharge (ESD) protection and flip-chip IC-BGA co-integration packaging. A dedicated $1.2V$ Serial Peripheral Interface (SPI) is implemented on chip for the bit tuning management required to control the DCO and the front-end passive devices C_1, C_2 and R_{IF}. The circuit voltage supply is $500mV$. A specific level shifter network between the

SPI and the WuRx bit nodes is introduced to step-down the voltage control level from $1.2V$ to $500mV$.

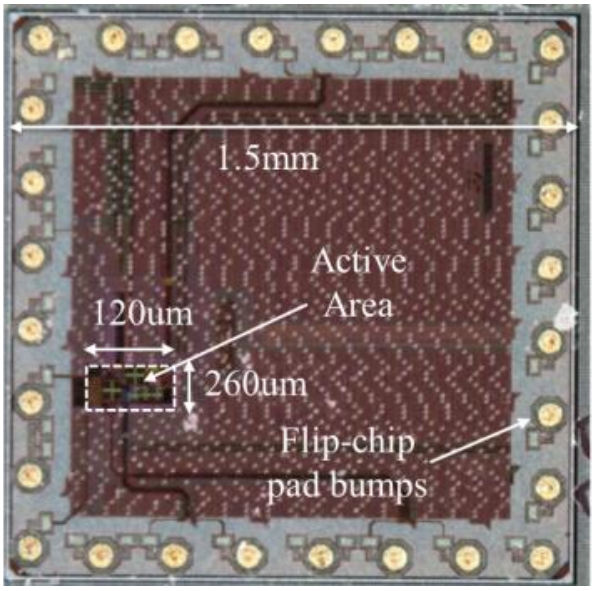


Figure 4.7. IC die photo.

The LC FEMN is implemented by using an external SMD inductor. C_1 and C_2 capacitors are designed as a 4-bits MIM capacitor network, to compensate IC, packaging and SMD process and temperature variations. The SD-2PPM *lvtlp* N-MOS switch transistors is designed with a 300Ω on-resistance impedance in order to provide an input impedance near to 750Ω to the FEMN. The IF capacitors (C_{IF}) are also implemented as external SMD elements. The IF resistances (R_{IF}) are implemented as 6-bits tunable devices for test flexibility on the antenna impedance matching. The DCO is designed in order to work in the standard temperature range of $-25°C$ to $-125°C$. Simulation results present a S_{11} response of $-17dB$ at the $900MHz$ targeted resonant frequency. The FEMN and the SD-2PPM provides an output voltage gain of $12dB$ with an effective RF quality factor of 410 at 900MHz for $C_{IF} = 100pF$, $L_1 = 8.2nH$ and $Q_{L1} = 25$. The noise figure presented at the SD-2PPM output is equal to $9.09dB$ at $1MHz$ IF frequency. In terms of linearity, this passive front-end structure presents a $-1dB$ compression point of $-16dBm$ for a $27pF$ IF capacitor. The simulated average power consumption of the DCO and the LO buffer stages is $16\mu W$ and $11\mu W$, respectively. The N-MOS and P-MOS 6-bits tunable current sources presents a coarse frequency step of $9MHz$. The 4-bits current source voltage bias provides a fine frequency step of $1MHz$. The voltage gain and the power consumption of the IF-LNA and

each of the two IF-amplifiers is respectively $28dB$ and $17dB$, and $12\mu W$ and $3\mu W$. The IF amplification chain bandwidth is defined between $60kHz$ and $10MHz$. The output noise figure is $14.6dB$ at $1MHz$.

4.2.2. Packaging implementation

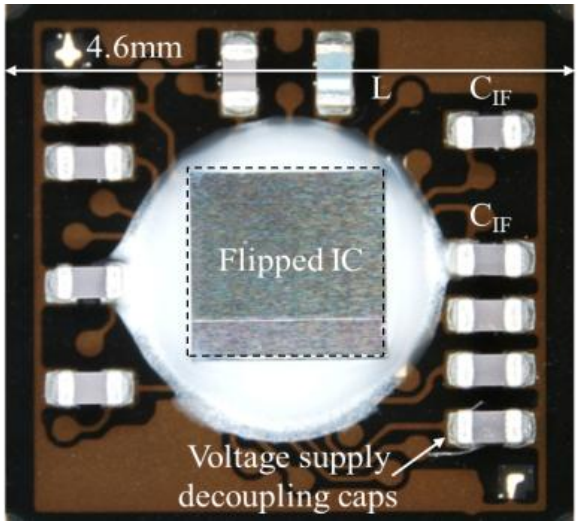


Figure 4.8. BGA package cavity photo.

A specific two metal layer Ball Grid Array (BGA) package has been designed under industrial conditions, hosting in its cavity not only the flip-chipped die but also several SMD (Figure 4.8). This allows the integration of the required high Q-factor passive inductor and the high value IF capacitors. The SMD inductor presents $8.2nH$ inductance and 25 quality factor. Four different BGA versions are implemented with four IF capacitance values of $27pF$, $47pF$, $82pF$ and $100pF$. The BGA cavity offers also free of charge space for the integration of some extra voltage supply decoupling capacitors very close to the IC, which are precious in a design using a non-locked frequency synthesis. Specific electromagnetic care has been provided for the layout of the sensitive RF paths. A high Q-factor piezo device has somehow been replaced early in the system architecture design by a higher-than-on-Si Q-factor inductor, and some die area for large capacitors has been saved by the opportunistic cavity-integration of these devices. Compared to the expensive and bulky piezoelectric resonator based WuRx architectures, this flip-chipped BGA packaging allows for a compact and low-cost solution for the future wake-up radio. The BGA is a 64 balls $0.5mm$ pitch $4.7mm\ x\ 4.7mm$ structure, designed upon full industrial rules.

4.2.3. Prototype measured results

The prototype measurement setup is shown in Figure 4.9. A dedicated Printed Circuit Board (PCB) is designed in order to host the Device Under Test (DUT). A mechanical push arm is used for practical test purposes to ensure contact connection between the BGA and the PCB. The IC SPI is directly driven from an Opal Kelly XEM3001 FPGA. DC biasing is provided from external voltage and current controlled sources. Frequency response measurements are made by injecting a single signal tone from a Rhode & Schwarz SMU200A vector signal generator, at the antenna RF input of the WuRx. Results are recorded by using a Rhode & Schwarz, FSUP, spectrum analyzer.

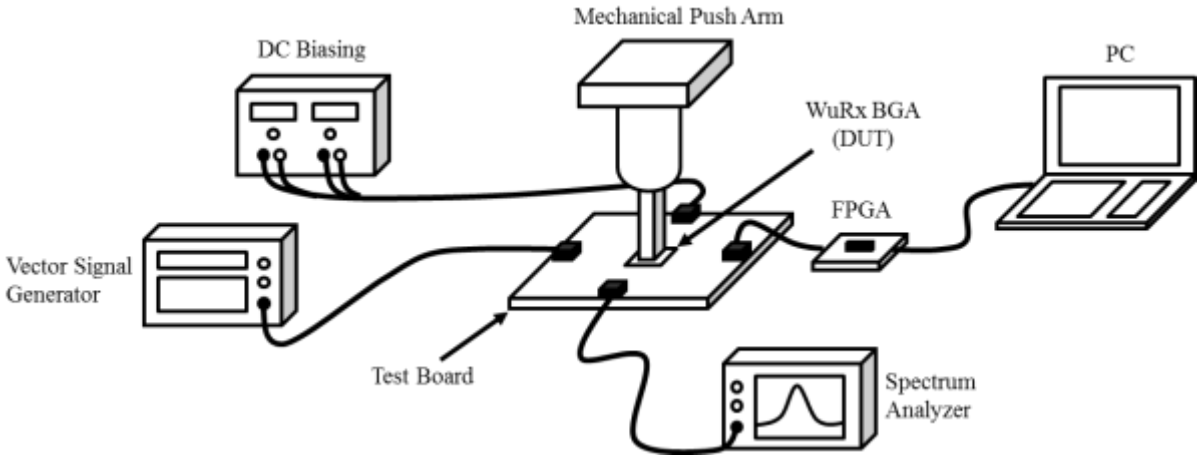


Figure 4.9. Prototype measurement setup.

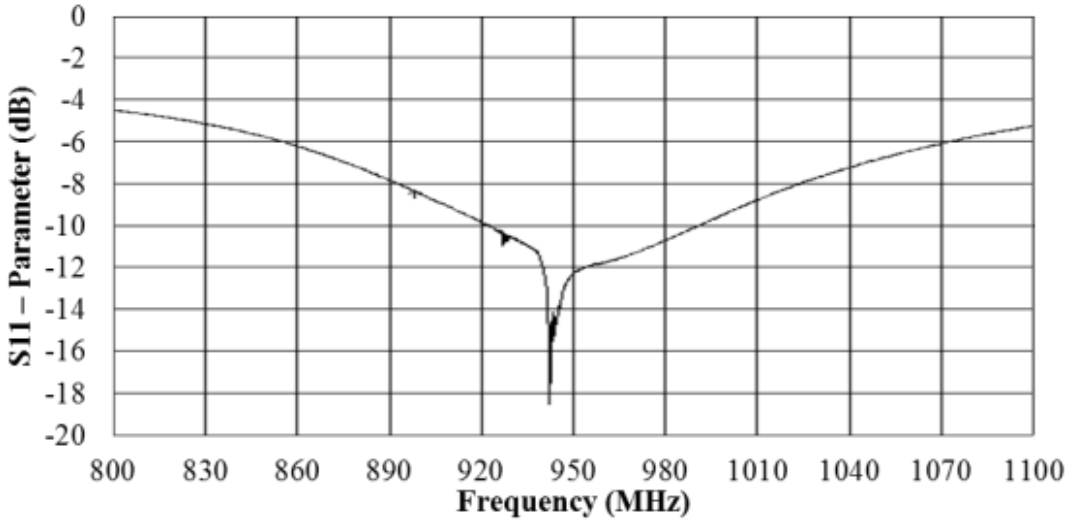


Figure 4.10. Measured S_{11}-parameter response.

The circuit S_{11}-parameter response is measured by replacing the vector signal generator with a Performance Network Analyzer (PNA-L) Agilent N5230A. Figure 4.10 shows the measured S_{11}-parameter of the WuRx front-end. The circuit presents wide $-10dB$ range between $925MHz$ and $992MHz$ for an LO frequency of $942MHz$. Centered around f_{LO}, the S_{11} response puts into evidence the sharp band-pass filter generated by the WuRx front-end.

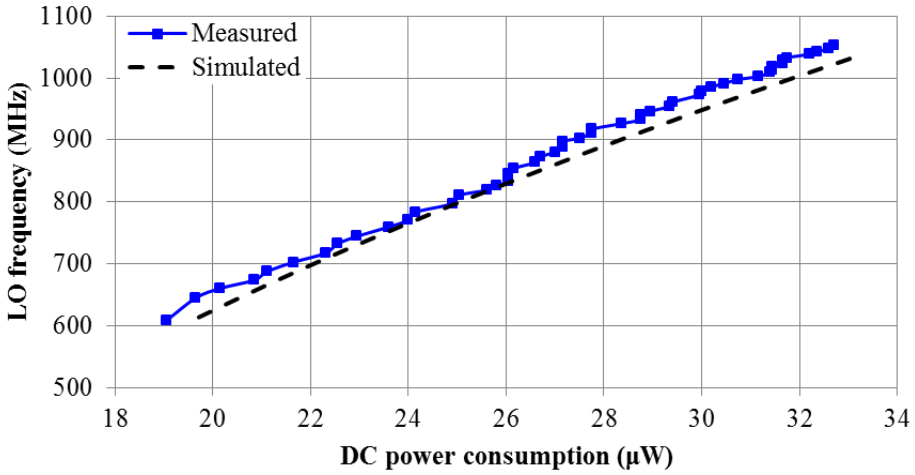


Figure 4.11. Measured and simulated local oscillator frequency as a function of its DC power consumption.

The DCO presents a linear frequency response with respect to the power consumption as suggested by the previous analysis developed in equation 4.14. Measured results show a DCO tuning range defined from 608MHz to 1052MHz for a power consumption comprised between $19\mu W$ and $32.7\mu W$, representing 49.3% of tuning range respect to the targeted nominal 900MHz LO frequency (Figure 4.11). The tunable integrated current and voltage sources driving the oscillator are symmetrically controlled (both N and P-MOS current and voltage sources with equivalent digital control logic word value) from the FPGA. Simulation and measured results present close matching with a slight power consumption diminution on the measured results, due to the voltage drop coming from the parasitic resistance of the PCB, BGA and IC routing paths, which reduces the effective voltage supply across the LO.

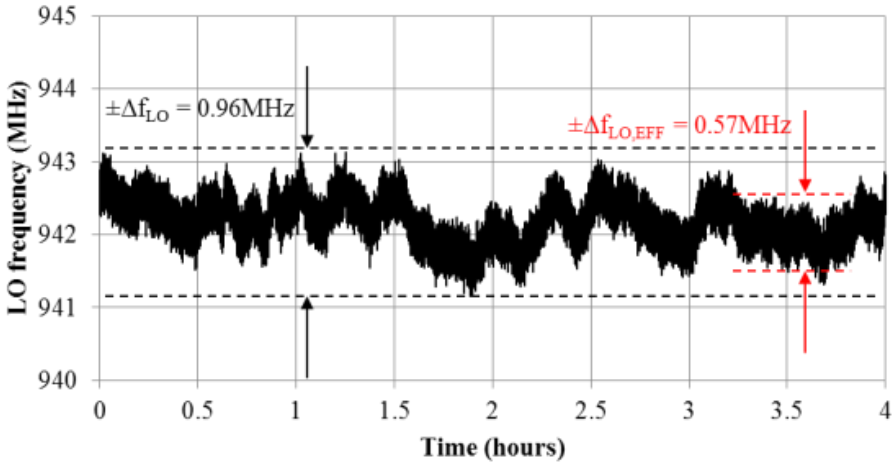


Figure 4.12. Measured 22˚C instantaneous free-running LO frequency.

Figure 4.12 shows the measured 22˚C instantaneous free-running LO frequency over 4 hours. Measurements have been correlated with the very precise room temperature control data coming from the facilities team at ST Crolles site. The frequency shift is equal to $\pm 0.96MHz$, which is equivalent to $\pm 1019.1ppm$. The LO frequency follows a pseudo-periodical variation behavior coming from the test room temperature variations, which is in this case regulated at $\pm$1°C difference from the standard 22°C. Effectively, the frequency shift is equal to $\pm 0.57MHz$ and the $\pm 0.96MHz$ represents the LO frequency drift within $\pm$1°C variation. This large uncertainty may results in signal miss-detection for systems with an IF bandwidth below $2MHz$.

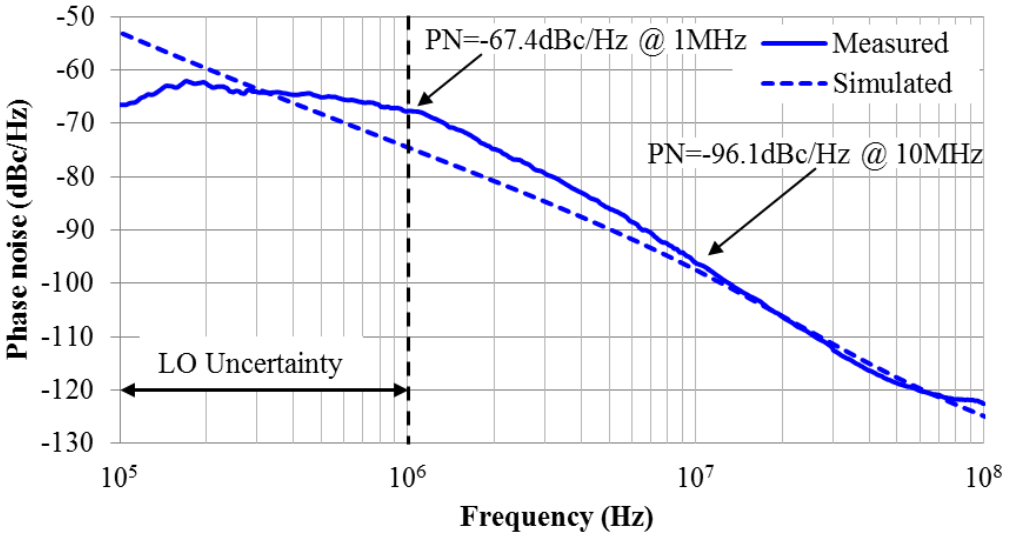


Figure 4.13. Measured and simulated LO phase noise.

Figure 4.13 presents the measured and the simulated $942MHz$ LO phase noise. In terms of measurements, for frequencies in the range of the LO uncertainty ($< 1MHz$), the spectrum analyzer finds difficult to lock to the LO carrier frequency. Hence, the phase noise is represented by a pseudo-constant value representing the effective integrated LO phase noise over its uncertainty bandwidth. The measured oscillator phase noise is $-67.4dBc/Hz$ and $-96.1dBc/Hz$ at $1MHz$ and $10MHz$ offset, respectively. With and average power consumption of $28.75\mu W$ and $-96.1dBc/Hz$ phase noise at $10MHz$ offset, the DCO presents a figure of merit [Kinget] of $-155.5dBc/Hz$. Given the uncertainty of the spectrometer locking range, measured results presents an offset with respect to simulated results on the range of the LO uncertainty and few megahertz afterwards. On the range of 10MHz to 100MHZ both results have close response.

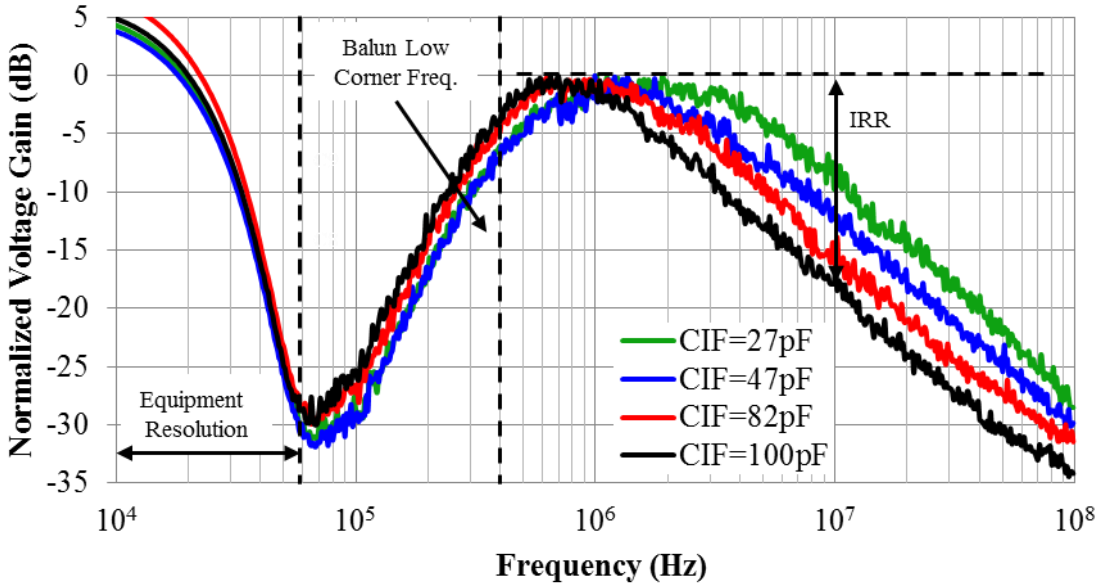


Figure 4.14. Measured SD-2PPM output IF frequency response.

In order to characterize the quality factor of the WuRx front-end, a fully differential wideband integrated test buffer stage is implemented at the SD-2PPM output. Its differential BGA output is transformed into a single-ended node, through and external SMD balun, implemented on the PCB. Figure 4.14 presents the measured normalized frequency response for the four different die versions, containing four different IF capacitor values. The spectrum analyzer resolution bandwidth is set to $30kHz$ providing a clean measured response beyond $60kHz$. The low cutoff frequency of the balun is about $400kHz$. The frequency response of the filter presents a $-20dB/dec$ slope, confirming the RC first-order LPF response of the

SD-2PPM. The four die measurements presents a LPF bandwidth proportional to the IF load capacitance value. In order to accurately extrapolate the effective quality factor of the wake-up receiver, a replica of the balun model used on the PCB is introduced on the simulation design. The resulting measured RF quality factor and IRR (evaluated at $10MHz$ DC offset) are plotted in Figure 4.15. This circuit presents a maximum Q-factor of 468 and a minimum IRR of $-17dB$, for $C_{IF} = 100pF$.

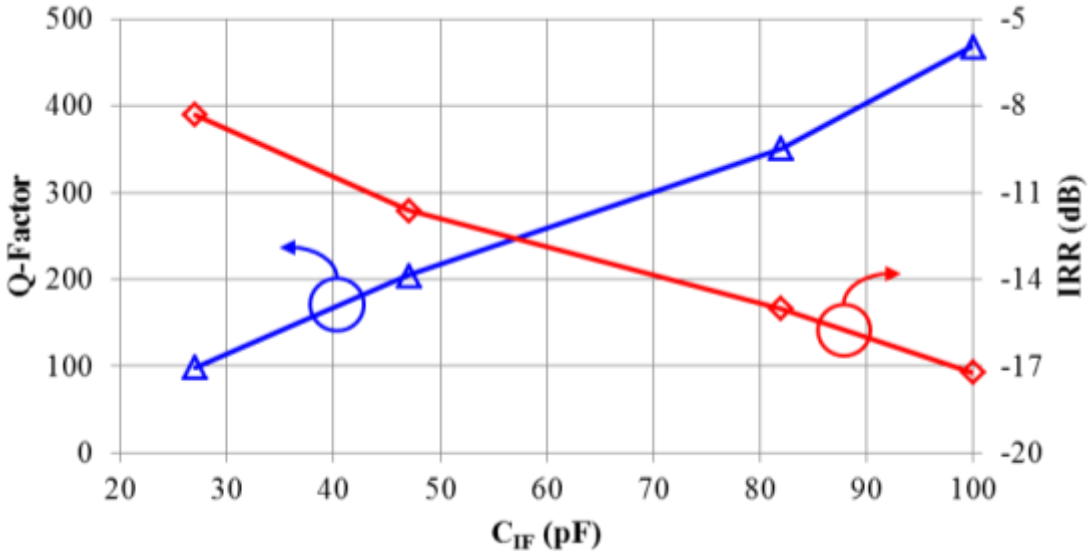


Figure 4.15. Measured RF quality factor and interference rejection ratio (IRR) evaluated at 10MHz DC offset for different IF capacitor values.

Figure 4.16 shows the measured and simulated results of the SD-2PPM output power and voltage gain response as a function of the input RF power, for $C_{IF} = 27pF$, $f_{IF} = 2MHz$ and $f_{IF} = 944MHz$. From the four IF capacitor BGA versions, the $C_{IF} = 27pF$ version is chosen to measure the SD-2PPM voltage gain and linearity so as to have the uncertain-IF signal ($f_{IF} \pm \Delta f_{LO} = 2MHz \pm 0.96MHz$) within the effective -3dB signal path bandwidth including the SD-2PPM, the output test buffer and the external SMD balun. Measured results show a slight difference of less than $1dB$ compared to simulation results. This behavior is principally due to the process variations including the SD-2PPM switches, the SMD inductor and the BGA packaging routing, which affects the voltage gain of the FEMN and the passive mixer. For high RF input power levels, measured results show faster output response saturation compared to simulation results. In both cases, the SD-2PPM $-1dB$ compression point is equal to $-16dBm$. This moderate linearity performance comes from the reduced LO amplitude ($V_{DD} = 500mV$) that drives the passive mixer, which limits the SD-2PPM

linearity to input signal amplitudes close to $V_{DD} - V_{TH}$. The passive voltage gain of the cascaded FEMN and heterodyne SD-2PPM is $11.3dB$.

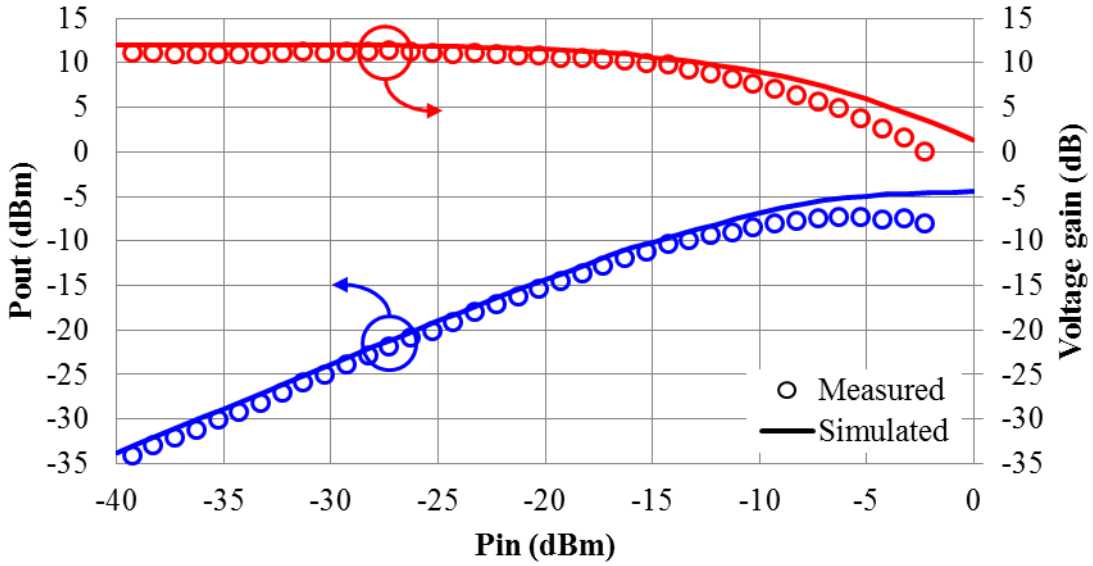


Figure 4.16. Measured output power and voltage gain of the SD-2PPM with respect to the input RF power, for $C_{IF} = 27pF$, $f_{IF} = 2MHz$ and $f_{IF} = 944MHz$.

Given the high flicker noise presented at the 2-PPM test buffer output when no signal is injected to the RF input, and given the high uncertainty of the desired signal at the IF-band, no noise figure measurements were able to be performed. This problem should be avoided in future implementations by replacing our test buffer amplifier with a dedicated low-noise amplifier and by increasing the cutoff frequency of the high-pass AC coupling network found at the test amplifier and the IF-LNA input.

All the measurements have been performed on a dedicated PCB with fixed regulated $500mV$ supply and 50Ω T-lines. The WuRx front-end consumes a total active power consumption of $47\mu W$ with $28.75\mu W$ accounting for the LO and the 2-PPM buffer stages at $942MHz$ and $18.2\mu W$ accounting for the three stage IF amplification chain. The total measured WuRx front-end voltage gain is $72dB$.

4.3. Chapter conclusions

The proposed circuit validates the theory and design of ULP N-path filters. This design was aimed to demonstrate the passive scheme methodology for Q-factor enhancement, by means of antenna impedance boosting and external IF-capacitors packaging co-design integration.

The proposed WuRx front-end implements a FEMN structure which enhances the RF input impedance value presented to the rest of the circuit, while providing passive voltage gain and LO harmonic rejection. The SD-2PPM provides the key high-Q band-pass filter response achieving an effective RF Q-factor of 468 with an IF capacitor of $100pF$. The passive front-end structure including the FEMN and the SD-2PPM presents a S_{11} response of $-18dB$ at $942MHz$ and provides $11.3dB$ of passive voltage gain with $-16dBm$ of $-1dB$ compression point. The IF amplification chain validates the benefit of the subthreshold and current reuse techniques, presenting a voltage gain of $60dB$ while consuming only $18\mu W$. In terms of local oscillator, the ring oscillator validates the energy efficiency of the proposed implementation presenting a power consumption below $29\mu W$ (including LO buffers) at $942MHz$. The DCO presents a wide frequency tuning range of 440MHz. Its unlocked nature presents a frequency drift of $\pm 0.96MHz$ ($\pm 1019.1ppm$) over 4 hours' time. This behavior may results in signal miss detection for very narrow IF-band structures, like for the $100pF$ IF capacitance die version. The entire WuRx front-end delivers a voltage gain of $72dB$ while presenting a power consumption of $47\mu W$. The BGA packaging strategy validates the co-design integration of silicon dies and SMD RF components as a low cost and compact BGA solution.

A performance comparison with previous works is presented in Table 4.1. This work demonstrates the advantageous strength of the N-path filter structures. Among the different discrete sampling, uncertain-IF, envelope detection and injection locking architectures, this uncertain low-IF 2PPM based receiver front-end achieves a comparable quality factor to that of MEMs resonators. The proposed circuit presents a power consumption of $47\mu W$. $5\mu W$ to $10\mu W$ of extra power budget should be attributed for the baseband signal treatment including the envelope detection, the integrator and the threshold stages. This performance is in line with the power budget established in Chapter 2 (see Table 2.1). Considering the full wake-up receiver architecture including the envelope detection and the threshold blocks, and

considering $8dB$ of SNR, the noise figure obtained from simulated results ($14.6dB$) and the effective IF bandwidth obtained for the $47pF$ IF capacitance ($2 \times 2.3MHz$), which is optimal to host the IF uncertainty, the estimated sensitivity of this wake-up receiver is $-85dBm$ (equation 2.5). Clearly, this implementation demonstrates the potential benefits of N-path filter based wake-up receivers able to achieve sensitivity levels on the range of $-85dBm$ with a power consumption below $100\mu W$.

	[Otis01] 2005	**[Pletcher01] 2008**	**[Hambeck] 2011**	**[Yan] 2011**	**This Work**
RX architecture	Discrete sampling	Uncertain-IF	Envelope detection	Injection locking	**Uncertain low-IF**
RF interference filtering	BAW	BAW	SAW + off-chip L network	External LC network	**BGA integrated Off-chip L**
Frequency (GHz)	1.9	2	0.868	0.868-0.915	**0.950**
Supply voltage (V)	1	0.5	1	1.2	**0.5**
RF Filtering Q	3800	101	78.91	N/A	**468**
Power (µW)	450	52	2.4	120	**47***
Sensitivity (dBm)	-100.5	-72	-71	-50	**-85****

* Only WuRx front-end power. Envelope detection and BB stages power consumption excluded.

** Analytical estimated sensitivity.

Table 4.1. Performance comparison with previous works.

Despite the presented performance, this architecture requires several modifications for further optimizations in view of a complete wake-up receiver implementation:

- SD-2PPM: In order to optimize the SD-2PPM noise and voltage gain performance, the IF resistor should be avoided.
- Uncertain-IF band: To avoid signal miss detection, a larger IF-bandwidth may be preconized to be able to entirely host the uncertainty of the desired IF signal. This specification should reduce the constraint of external SMD IF capacitors, leading to a trade-off between size, high-Q filtering and sensitivity. On the other hand, in order to reduce the DC flicker noise influence, a higher high-pass filter cutoff frequency

$(\sim 1MHz)$ of the IF-LNA AC coupling network should be defined. Variable voltage gain stages may also be considered to provide large reception dynamic range to the desired RF input signal.

- Ring oscillator: To generate the LO signal, a more energy efficient architecture should be implemented. As an example, in [Nadeau] (proposed in time just after this circuit implementation) a 50% two-phase LO signal is generated from a single three-stage ring oscillator with a matched delay transmission gate. This architecture avoids the second parallel three-stage ring oscillator leading to approximately $7\mu W$ power saving.
- LO uncertainty: To reduce the effective integrable bandwidth and therefore enhance the sensitivity of the receiver, the LO uncertainty should be reduced. As a first option, the uncertainty of the ring oscillator can be optimized through the implementation of a dedicated ultra-low power PLL. However, this solution implies some extra power consumption for the entire feedback loop and requires an external high-Q time reference resonator. On the other hand, unlocked LC resonators appear as a fair solution in order to provide better accuracy while still avoiding power hungry PPLs. As previously mentioned, LC configurations require higher power consumption compared to the one of ring oscillators. However, we believe that better energy efficient LC architectures can be developed. This concept sets an exciting motivation for further research on LC architectures in order to push the boundaries of the minimum reachable power consumption.
- Interferer rejection: As presented in Chapter 2, in order to meet dense node clustering, the receiver must present high immunity against interferers. For this, a better LO phase noise must be guaranteed in order to minimize the reciprocal mixing effect and hence, maximize the sensitivity of the intended WuRx.

The presented circuit opens the door to novel wake-up receiver topologies aiming ULP and high sensitivity performances while avoiding external high-Q resonators. The passive front-end of this circuit is validated and is highly recommended for future WuRxs. Further bandwidth reduction for sensitivity enhancement and further interference rejection performances may be reached by using multi-layer N-PPM configurations through all the wake-up receiver signal-path.

Chapter 5

Interferer Resilient WuRx with Multi-Layer N-Path Filters Dual-IF Architecture

This chapter presents the design methodology of a complete 2.4GHz wake-up receiver intended for dense nodes WSN environments. OOK modulation is chosen for its energy efficient performances, as discussed in Chapter 2. In order to overcome the LO uncertainty drawback presented by the ring oscillator developed in the first circuit, an ULP LC oscillator is implemented. To reduce the high inductance value and high power consumption requirements of the LC oscillator, 2.4GHz is chosen as the targeted RF input frequency compliant with the IEEE 802.14.5 standard (further details about these specifications are provided in section 5.1.1). One bit digital signal is defined as the WuRx output signal, for power optimization.

The effort behind this design is mainly focused on the improvement of the overall receiver sensitivity, as well as the development of an ULP filtering methodology to enable strong interference rejection, using very low-Q external elements.

To relieve the challenge on high sensitivity wake-up receivers, it is worth to identify the main contributor susceptible to be optimized for truly enhancement. From the sensitivity expression derived in equation 2.5, the source resistance power noise and the $SNR_{out,min}$ are considered as constants and cannot be further optimized. The noise figure can be hardly decreased with the present energy specifications, but 3 to $6dB$ improvement can be obtained by attributing extra passive voltage gain at the front-end. On the other hand, the bandwidth is the most flexible contributor and is only limited by the desired signal data rate itself. This

contributor is therefore the key element that may be optimized for sensitivity optimization in wake-up receivers. In the case of low data rate WuRx systems ($< 100kb/s$), optimal performance is achieved when the effective bandwidth equals twice the data rate. $33dB$ improvement compared to the $20MHz$ bandwidth system described in the previous chapter should be reached in the particular case of a $10kHz$ bandwidth system.

Furthermore, for realistic implementation in dense WSN environments, the WuRx should be able to deal with a large number of RF interferers. Considering the fact that in most of the cases, the power of interferers is hundred times larger than that of the desired signal, an efficient filtering methodology must be developed avoiding any extra energy expense, noise, cost or physical volume.

Implementation details and measurement results for the proposed WuRx in 65nm CMOS technology are presented. Finally, a comparison with the most relevant State-of-the-Art WuRx architectures is shown.

5.1. WuRx architecture

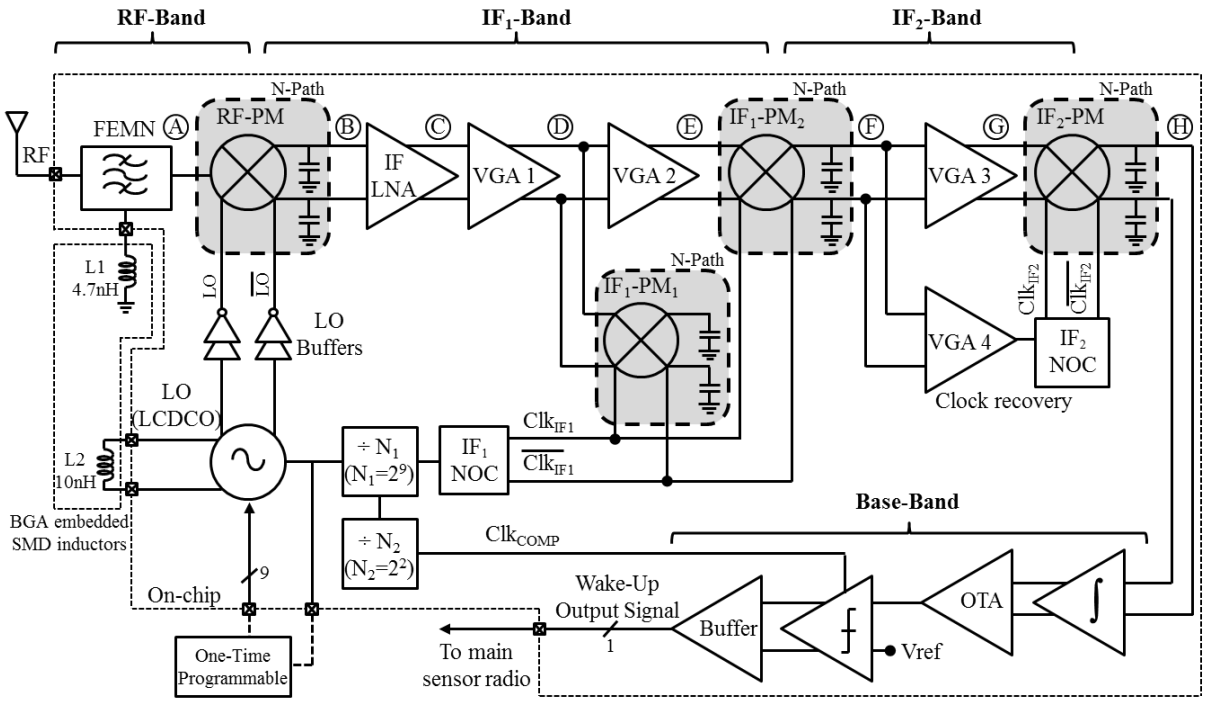


Figure 5.1. Dual-IF Multi-Layer N-Path Wake-Up Receiver block diagram.

Figure 5.1 presents the proposed dual-IF WuRx block diagram. The architecture overcomes the need of high-Q time-base references by combining a low-Q resonator-referred LO and distributed multi-stage Signal Path (SP) high-Q filtering obtained by ULP integrated electronic means. The receiver takes advantage of the N-path passive mixer impedance frequency translation principle to sharpen the effective bandwidth all along the signal-path, and hence, enhance the system overall sensitivity and interferer immunity. Two-path only passive mixers (2-PPM, N=2) structures are chosen in this system to minimize the LO path complexity and minimize power requirements, while still achieving elevated Q-factor filtering. This receiver provides the flexibility to set the WuRx as an always-on or as a duty-cycled device, according to the application. The entire architecture is operated from a single $500mV$ power supply.

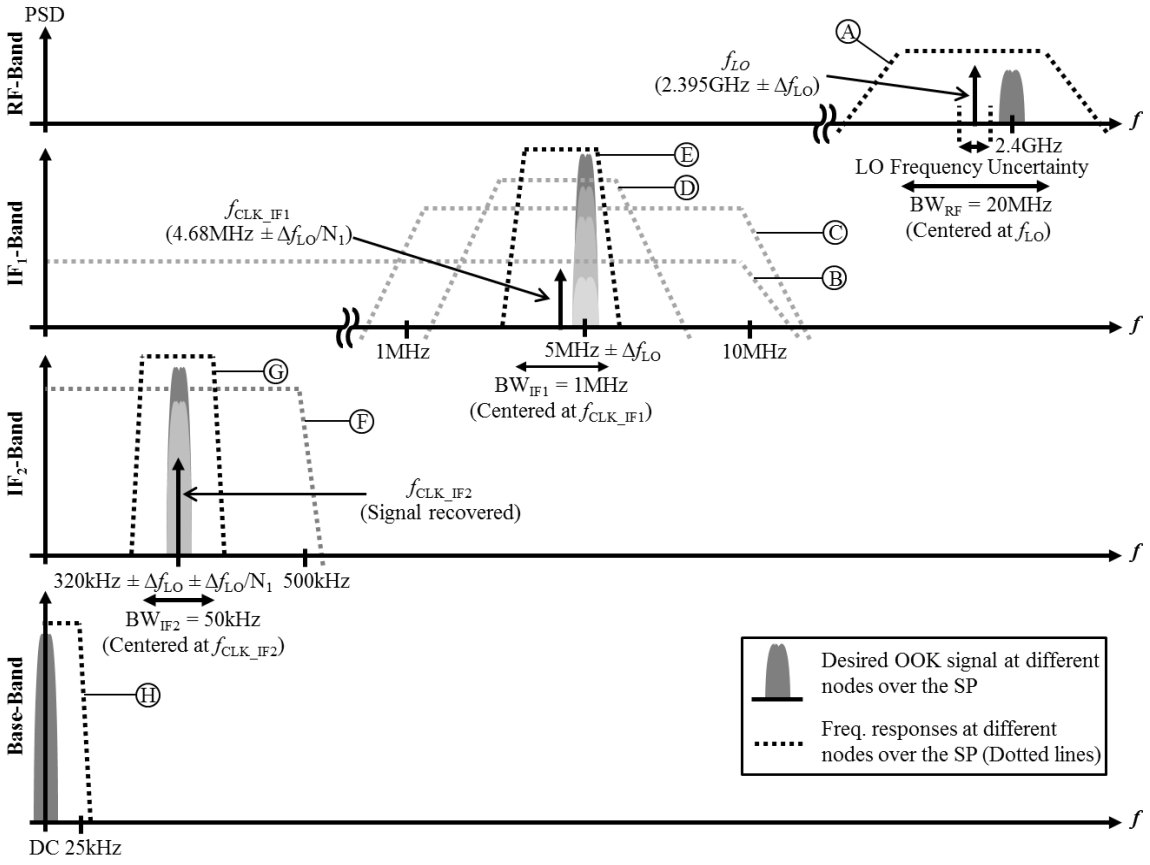


Figure 5.2. Method of operation and frequency plan of the proposed Dual-IF WuRx.

The method of operation and the frequency plan are depicted in Figure 5.2. The first N-PPM (RF-PM in Figure 5.1) is used to translate the incoming RF signal to IF_1-band by mixing with LO and presents an effective RF band-pass filtering with Q-factor of 120 (RF-band frequency diagram in Figure 5.2). After some low noise amplification, the IF_1 signal is

band-pass filtered anew by a second N-PPM (IF_1-PM_1 at point D) in a parallel configuration [Zhang]. The translation to the second IF is obtained by mixing with CLK_{IF1} through another N-path passive mixer (IF_1-PM_2), now placed in series. The IF_1-band frequency diagram in Figure 5.2 shows the overall frequency response at the end of IF_1-band (point E), illustrating the narrow band-pass filter response for strong out-of-band interferer rejection. Here, a second IF-band is required to eliminate the CLK_{IF1} modulation introduced at the IF_1-band singal-path by the IF_1-PM_1 and IF_1-PM_2 passive mixers. The frequency response in point F has a low-pass shape (IF_2-band frequency diagram in Fig. 2), while the overall frequency response at the end of IF_2-band (point G) is also a N-PPM band-pass-like, adding further interferer attenuation. Finally, the signal is innovatively self-mixed to the Base-Band (BB), by using a high linear and gain boosted N-PPM based envelope detection technique (IF_2-PM). At base-band (after point H), the signal is integrated for excess bandwidth noise reduction, amplified and converted to a one bit digital signal through a simple latch comparator. The signal-path frequency bandwidths values indicated in Figure 5.2 are selected as a compromise between the smallest possible signal bandwidth and the expected LO uncertainty for this particular WuRx system implementation.

5.1.1. Clock generation

As previously discussed, despite the ring oscillator energy efficiency presented for the first circuit implementation, its inaccuracy bounds the overall WuRx sensitivity. To overcome this drawback, a study on lowering the effective power consumption of LC resonators should be addressed, in order to enable high-accuracy in weak time-reference unlocked oscillators.

Previous State-of-the-Art has revealed the advantage of using high-Q external RF-MEMS resonators to push-down the power consumption limits of LC oscillators [Chee] [Nelson]. The oscillator proposed in [Chee] uses the Pierce configuration with a CMOS inverting amplifier. With the help of a high-Q (Q ~ 10^3) Film Bulk Acoustic Resonator (FBAR), the oscillator achieves a minimum power consumption of $90\mu W$. In [Nelson], the power consumption was further reduced to $20\mu W$ by using an FBAR Pierce oscillator with CMOS weakly-forward body biasing for gain loop boosting.

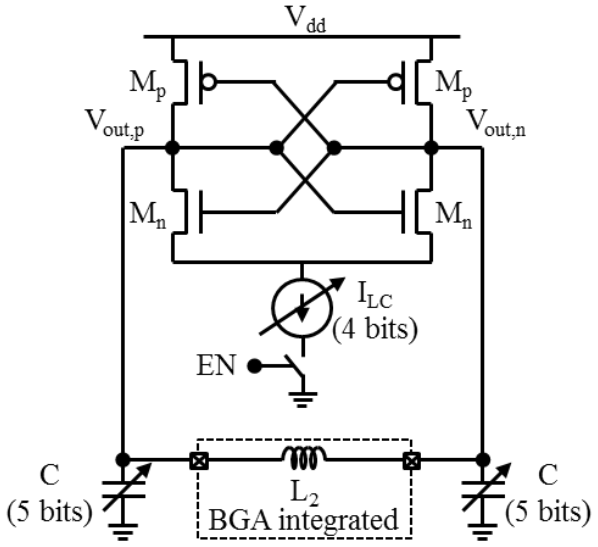


Figure 5.3. Simplified schematic of the current reuse CMOS cross-coupled LC-DCO.

The time-base of the proposed WuRx consists of a low-cost "*low Q-factor"* (compared to the high-Q factor provided by crystals or even RF MEMS resonators such as BAWs) external resonant structure (an inductor). Figure 5.3 shows the simplified schematic of the proposed CMOS current reuse cross-coupled LC-Digital Controlled Oscillator (LC-DCO). This current reuse architecture, biased in weak-inversion regime for high CMOS power efficiency g_m/I_d, takes advantage of both N-MOS and P-MOS transconductances to half the power consumption for the same required loop gain. The fully differential configuration ensures some common-mode rejection and provides symmetrical falling time and rising time on the LC differential outputs for phase noise optimization, thanks to the flicker noise upconversion reduction [Razavi03] [Hajimiri] . A four bits variable current source is implemented to compensate process and temperature variations, while providing flexibility of minimum current consumption for different environments. The resonant frequency of the system can be written as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{2}{LC}} \tag{5.1}$$

Where L is the inductance and C is the effective capacitance of the system that takes into account the effective CMOS transistors $(C_{dd} + C_{gg})$, ESD, pads and packaging parasitic capacitances. For low power requirements and low inductance values, this LC oscillator is designed to work at the $2.4GHz$ IEEE 802.15.4 band. Compared to the traditional Pierce oscillators, this architecture profits of the cross-coupled configuration to double the number

of single amplification stages, and hence, exponentially reduce the power consumption for a given gain. The total loop gain of the system is expressed as

$$H(\omega_0) = \left[\frac{(g_{m,n} + g_{m,p})R_p}{2}\right]^2 \tag{5.2}$$

Where R_p represents the parallel inductance resistance (not included in Figure 5.3). The cross-coupled architecture transforms the transistor transconductances into a negative resistance (R_{neg}) to compensate the lossy effect of the parallel inductance resistance

$$R_{neg} = -\frac{2}{g_{m,n} + g_{m,p}} \tag{5.3}$$

According to Barkhausen criterion, to ensure the oscillation of the system the condition $|H(\omega_0)| \geq 1$ needs to be satisfied [Razavi02]. Therefore the minimum transconductance required is

$$(g_{m,n,min} + g_{m,p,min}) = \frac{2}{R_p} \tag{5.4}$$

This positive feedback system provides zero-phase shift at each g_m stage. Thus, the overall phase shift is zero and the second Barkhausen condition is the also satisfied.

As previously discussed in Chapter 2, since the CMOS transistors are operated in weak-inversion regime, the drain-source current is expressed as $I_{ds,WI} = g_{m,WI} n V_T$, where n is the subthreshold slope factor and V_T is the thermal voltage ($V_T = KT/q$). At the steady-state of the oscillator, differential behavior is assured. Considering the unity loop gain bound condition, the minimum LC resonator power consumption can be expressed as

$$\begin{aligned} P_{LC,min} &= V_{dd} I_{LC} \\ &= V_{dd}(g_{m,n,min} + g_{m,p,min}) n V_T \\ &= \frac{2 V_{dd} n V_T}{R_p} \end{aligned} \tag{5.5}$$

Assuming high-Q and replacing the parallel inductance resistance by its equivalent quality factor dependent expression

$$P_{LC,min} = \frac{2 V_{dd} n V_T}{\omega L Q_L}$$

$$= \frac{V_{dd}}{Q_L}\sqrt{\frac{2C}{L}}nV_T \tag{5.6}$$

The equation above clearly shows the right way of power consumption optimization on LC oscillators operated in subthreshold regime. For energy efficiency at a given resonant frequency, the voltage supply and the effective capacitance must be minimized and high quality factor and inductance values must be preconized. To overcome the limitation of high-Q high-L IC inductors, an external SMD inductor packaged in the BGA is implemented. Again, it is important to point out the significant effort required on the IC-BGA co-design to minimize the overall parasitic capacitances for power and K_{VCO} optimization, as well as, the series routing path resistance to avoid inductor Q-factor reduction.

Equation 5.6 indicates the minimal power consumption required to equalize the parallel inductance resistance. However, to assure start-up and maintain the oscillation, the maximum negative resistance should be smaller than the overall parallel inductance resistance. A factor of four is considered as a result of the optimum *fan-out* value defined for a minimum delay in a logical gate (in this case an inverter) [Rabaey01].

$$P_{LC,0} = \frac{4V_{dd}}{Q_L}\sqrt{\frac{2C}{L}}nV_T \tag{5.7}$$

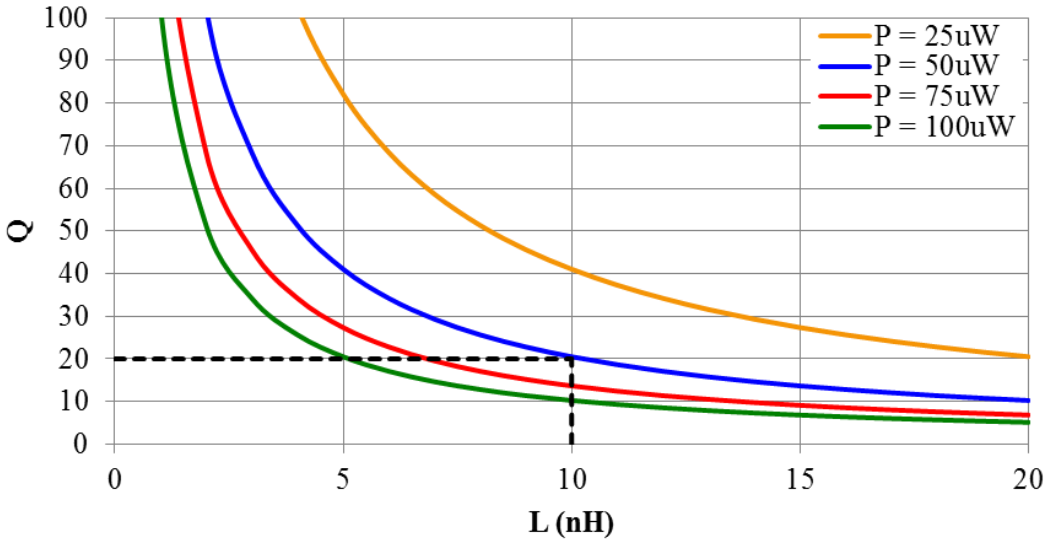


Figure 5.4. Minimum quality factor as a function of the inductance for different LC power consumption values. $n = 1.5$, $V_{dd} = 0.5V$ and $f_0 = 2.4GHz$.

Figure 5.4 shows the minimum quality factor as a function of the inductance for different LC power consumption values (referred to equation 5.7). We can observe the handicapping limitation for integrated inductors, for which a quality factor of 30 is required to achieve an energy consumption below $50\mu W$ with $10nH$ inductance. This requirement can be easily obtained from a commercial low cost SMD inductor.

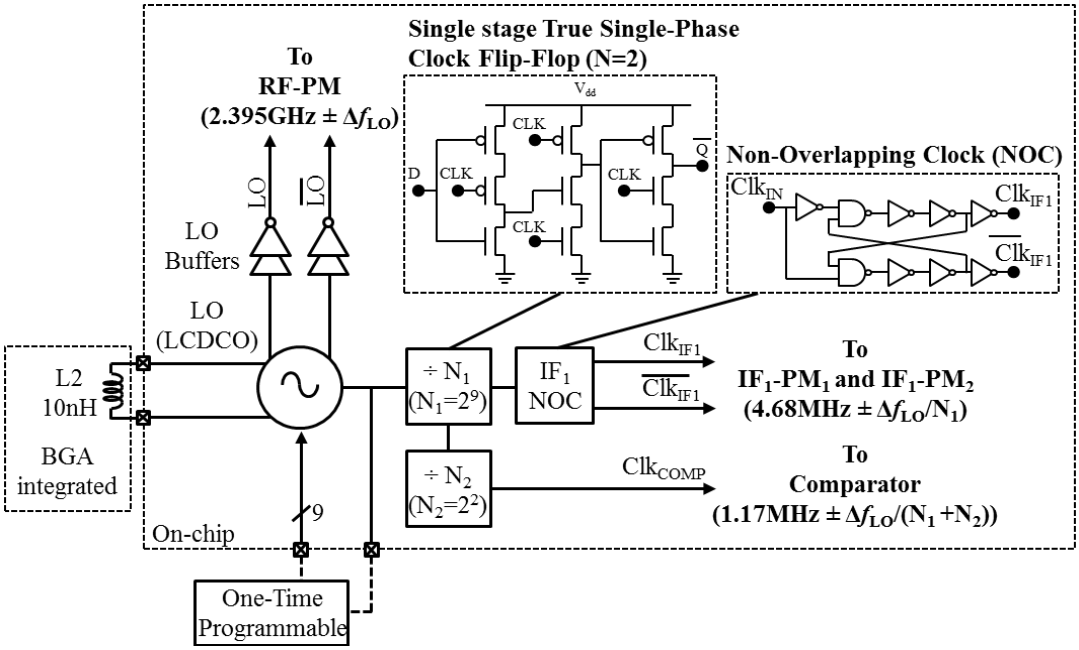


Figure 5.5. WuRx clock generation block diagram.

In this receiver, the LC-DCO is first calibrated at the desired frequency by One Time Programmable (OTP) logic and then allowed to free-run. The overall signal-path of the WuRx is designed to completely mitigate the LO uncertainty Δf_{LO}. Apart from the unlocked LO frequency $(f_{LO} \pm \Delta f_{LO})$, the proposed WuRx requires multiple clocks working at different frequencies for the different N-path filters and the BB comparator. In view of this prerequisite, an ULP frequency divider chain is designed (Figure 5.5). The clock signals CLK_{IF1} and CLK_{COMP} are derived from the $2.395GHz \pm \Delta f_{LO}$ LO through cascaded True Single-Phase Clock (TSPC) frequency dividers, each with a frequency divider factor of two. The signals CLK_{IF1} and CLK_{COMP} involve nine and eleven single TSPC stages, and generate a frequency of $4.68MHz \pm \Delta f_{LO}/2^9$ and $1.17MHz \pm \Delta f_{LO}/2^{11}$, respectively. A Non-Overlapping Clock (NOC) is implemented at the end of the CLK_{IF1} chain for N-path filter frequency response optimization. Note that the clock signal CLK_{IF2} is obtained by signal clock recovery from the OOK modulated desired signal at point F. We will come back to this point in section 5.1.4.

5.1.2. RF Front-end section

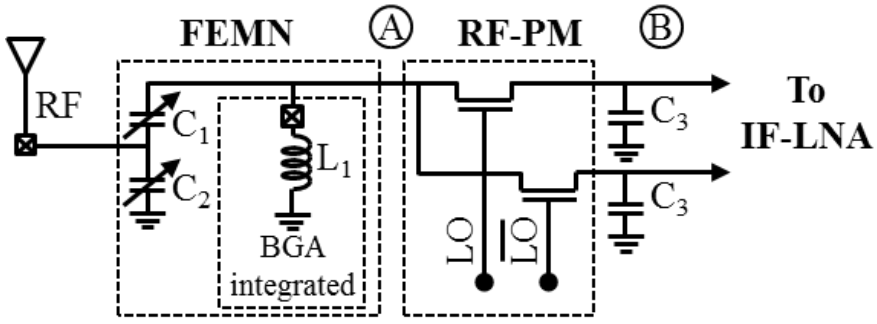


Figure 5.6. Simplified schematic of the fully-passive WuRx Front-End.

Figure 5.6 shows the RF front-end simplified transistor schematic. This design follows the same architecture developed for the first prototype presented on Chapter 4. Passive RF voltage gain is achieved by means of antenna impedance boost transformation and single-to-differential PSS charge conservation, respectively provided by the FEMN and the RF-PM. The use of a high Q-factor external surface mounted inductor $\left(Q_{L,effective} = 25\right)$ enhances the voltage gain at point A and provides band-pass filtering to attenuate the LO harmonics. Capacitors C_1 and C_2 are implemented as tunable devices for input impedance matching calibration. Unlike the front-end presented in Chapter 4, this RF-PM overcomes the constraint of high capacitance values (C_3) by enlarging the downconverted IF_1 bandwidth. The RF-PM is designed without a resistive load (R_{IF}), for gain and noise optimization. Given the band-pass filter response of the equivalent FEMN RLC network, the influence of the LO harmonics are partially attenuated.

Similarly to the front-end structure presented in Chapter 4, the voltage gain and the Q-factor of the system are respectively given by equations 4.12 and 4.13, considering an infinite IF resistance $(R_{IF} = \infty)$. Given the BPF response of the FEMN, the influence of LO harmonics is attenuated at the RF-PM input. This FE architecture provides moderate RF linearity performances for strong power RF input signals.

5.1.3. IF_1-band section

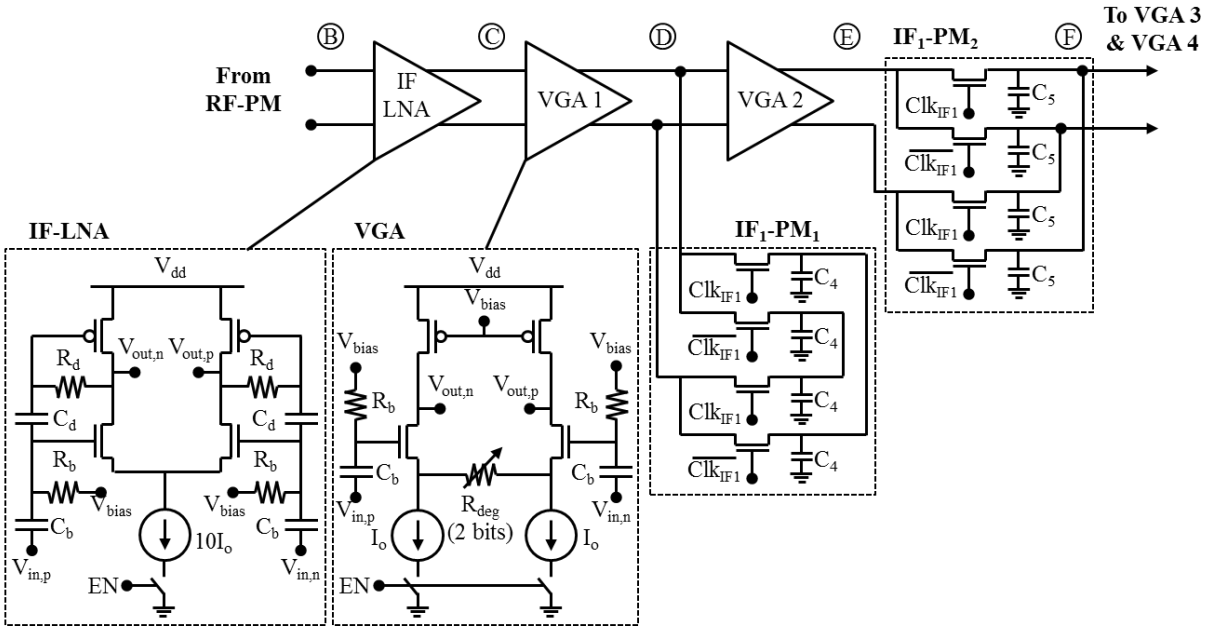


Figure 5.7. Simplified schematic of the IF_1-band.

The IF_1-band is the key section that ensures the main narrow band filtering with low noise amplification and provides the remarkable interferer rejection of the receiver. Shown in Figure 5.7 is the simplified schematic of the IF_1-band. At node B, the signal is amplified by the band-limited low noise amplifier IF-LNA. As previously discussed in Chapter 4, this current reuse structure exploits the transconductance of both N-MOS and P-MOS transistors to halve the current consumption for a given gain. Its voltage gain is defined by equation 4.15. The gain of the following common source degenerated amplifiers (VGA1 and VGA2) is controlled by 2-bits source resistances, in order to handle large input power dynamic range. The passive mixers IF_1-PM_1 and IF_1-PM_2 are implemented using a Fully Differential 2-PPM (DD-2PPM) structure as the insets in Figure 5.7. The clock driven signal CLK_{IF1} is generated from a Non-Overlapping Clocks (NOC) for filtering optimization. The IF_1 passive mixers take advantage of the high VGAs output impedance $(R_{VGA,out})$ and the mixer load capacitance values ($C_{4,5}$), to provide a sharp BPF frequency response (points D and E). AC coupling is implemented at the input of each amplification stage to reduce the flicker noise and eliminate DC offsets. A low-leakage enable circuit common to all stages (EN command) is provided for duty-cycling purposes.

The voltage gain of the IF-LNA is the same as the one derived on the previous chapter in equation 4.15. The unloaded common source degenerated VGA in-band voltage gain is given by

$$A_{v0,VGA} = -\frac{g_{m,n}}{(g_{ds,n}+g_{ds,p})(1+g_{m,n}R_{deg}/2)} \tag{5.8}$$

Following the parallel 2-PPM analysis developed in Chapter 3 and considering the equation 3.56, the frequency translated voltage gain of each VGA1 and VGA2, respectively loaded by the passive mixers IF_1-PM_1 and IF_1-PM_2, is given by

$$A_{v,VGA-DDPPM}(\omega_{IF2}) = A_{v0,VGA}\frac{Z_{in,DD-2PP}(\omega_{IF2})}{Z_{in,DD-2PP}(\omega_{IF2})+R_{VGA,out}} \tag{5.9}$$

Where ω_{IF2} is the downconverted IF_2 frequency $(\omega_{IF2} = \omega_{IF1} - \omega_{CLK,IF1})$ and $Z_{in,DD-2PPM}(\omega_{IF2})$ is the passive mixer input impedance of each IF_1-PM_1 and IF_1-PM_2 mixers. The last stage of the IF_1-band is the IF_1-PM_2. As previously explained, this passive mixer is set as a narrow BPF load, with respect to VGA2. Compared to the first IF_1-PM_1 mixer, the IF_1-PM_2 is placed in a series configuration and its downconverted signal is used to generate the second IF-band. Considering the equation 3.51, the output voltage gain of the IF_1-PM_2 is defined by

$$A_{v,IF1-PM2}(\omega_{IF2}) = \frac{\left(\frac{\pi\gamma(R_{VGA2,out}+R_{sw,IF1-PM2})}{2\gamma R_{VGA2,out}+R_{sw,IF1-PM2}}\right)}{1+j\omega_{IF2}\pi\gamma(R_{VGA2,out}+R_{sw,IF1-PM2})C_5} \tag{5.10}$$

Where $1/[2\pi\gamma C_5(R_{VGA2,out}+R_{sw,IF1-PM2})]$ is the 3dB IF_1-PM_2 downconverted LPF bandwidth $(f_{BW,LPF,IF1-PM2})$. Neglecting the filtering effect of the preceding VGA1 stages (FEMN, RF-PM and IF-LNA) and assuming an equivalent VGA1 and VGA2 BPF response, the resulting LPF bandwidth found at node E, is equal to $\left(\sqrt{\sqrt{2}-1}\right)f_{BW,LPF,IF1-PM2}$. Considering the complex bandwidth of the downconverted IF_1-band and the IF_2-band, the effective quality factor at the output of the IF_1-band (node E) is written as

$$Q_{IF1} = \frac{f_{IF1}}{4\left(\sqrt{\sqrt{2}-1}\right)f_{BW,LPF,IF1-PM2}} = \frac{\pi\gamma f_{IF1}C_5}{2\left(\sqrt{\sqrt{2}-1}\right)}(R_{VGA2,out}+R_{sw,IF1-PM2}) \tag{5.11}$$

The effective quality factor at node E with respect to the RF input frequency is

$$Q_{IF1,eff} = \frac{f_{RF}}{4\left(\sqrt{\sqrt{2}-1}\right) f_{BW,LPF,IF1-PM2}} = \frac{\pi\gamma f_{RF} C_5}{2\left(\sqrt{\sqrt{2}-1}\right)} \left(R_{VGA2,out} + R_{sw,IF1-PM2}\right) \quad (5.12)$$

To get a better insight of this architecture, let us assume the WuRx configuration with a $2.4GHz$ RF input signal and a clock CLK_{IF1} frequency equal to $5MHz$. Assuming a VGA output impedance of $200k\Omega$, a switch resistor of $10k\Omega$ and a load capacitance of $3pF$, the IF_1 quality factor is only about 1.56. However, the effective Q-factor with respect to the RF input signal is boosted to 738. By cascading N-path filters the effective quality factor can be remarkably increased beyond 10000. Clearly, this architecture results in a very low cost and compact solution for ULP WSN with extremely high-Q filtering and strong interferer rejection specifications.

The fact of cascading N-PPM also provides the possibility of boosting the out-of-band interference rejection ratio. Considering the DD-2PPM IRR equation 3.50 derived in Chapter 3, and assuming the same value for the VGA1 and VGA2 output impedances, and for the IF_1-PM_1 and the IF_1-PM_2 passive mixers switch resistance $\left(R_{sw,IF1-PM1} \approx R_{sw,IF1-PM2}\right)$, the maximal IRR provided by the parallel passive mixers at the output of the IF_1-band (node E) is written as

$$IRR_{IF1,max} = \left(\frac{R_{VGA2,out} + 2R_{sw,IF1-PM2}}{4R_{sw,IF1-PM2}}\right)^2 \quad (5.13)$$

For a VGA2 output impedance of $200k\Omega$ and a IF_1-PM_2 switch resistor of $10k\Omega$, the maximal IF_1-band IRR provided by the parallel passive mixers is $-30dB$.

In terms of noise, thanks to the high voltage amplification provided by the preceding RF front-end and the IF-LNA stages, the noise contribution coming from each of the IF N-PPM may be neglected. However, $3dB$ NF degradation is observed at the IF_1-PM_2 output as a consequence of the image downconversion, which folds on top of the desired IF output signal [Niknejad]. Additionally, considering the noise contributions coming from all the different LO harmonics folding into the output spectrum, the overall IF_1-PM_2 output noise figure is incremented by approximately 19% to $3.76dB$.

Figure 5.8 illustrates the simulated frequency response of the IF1-band from the node B to the node E with $CLK_{IF1} = 4.68MHz$. At node B, the RF front-end provides a low-pass

filter response. At C, the signal is low noise amplified by the LNA with a BPF shape. At point D, the signal passes through the first VGA-DD2PPM filter creating a band-pass filtering around CLK_{IF1} with $3MHz$ bandwidth. At node E, the overall IF_1-band frequency response is a very narrow BPF with $1MHz$ bandwidth. The squared clock upconvert modulation generates spurious at every odd harmonic of CLK_{IF1} ($14.04MHz$, $23.4MHz$, … etc) with $27dB$ and $39dB$ rejection, for the third and fifth clock harmonics, respectively. The rejection at $5MHz$ CLK_{IF1} frequency offset is about $35dB$.

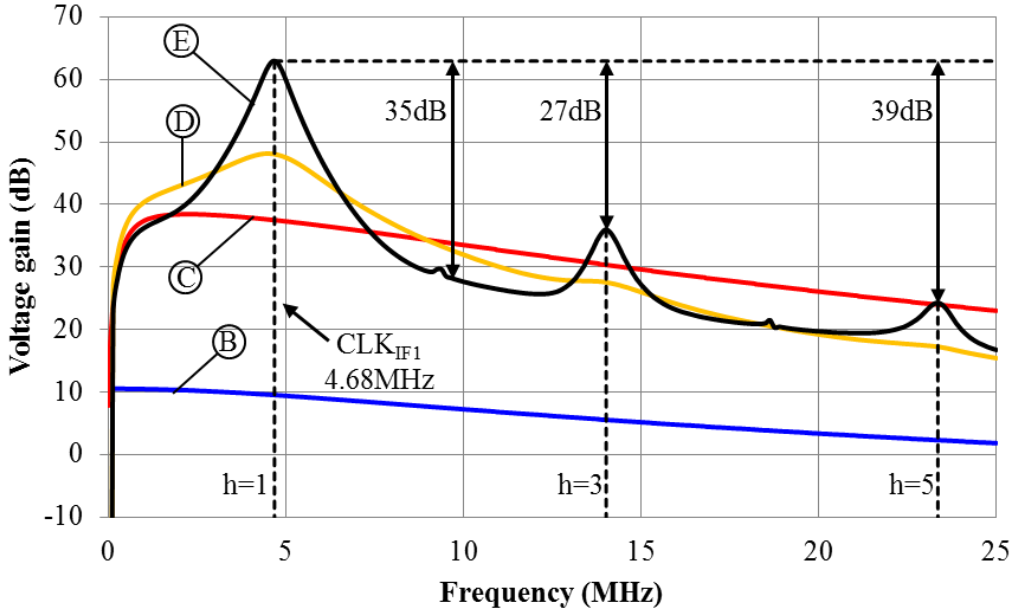


Figure 5.8. Simulated IF_1-Band frequency response. 2-bits VGAs gain tuning set to maximum, $CLK_{IF1} = 4.68MHz$.

The last key elements analyzed in this section are the effect the LC oscillator uncertainty, the limitation of non-quadrature AM direct-downconversion mixers and the LO upconvert modulation. Since the time reference of this WuRx is given by an *unlocked low quality factor* resonant element, the uncertainty of the LO signal may result in a miss-detection response degrading the Bit Error Rate (BER). This limitation impedes therefore any direct downconversion from IF to DC. Even if there was a way to generate a precise LO with a CLK_{IF1} signal perfectly aligned to the frequency of the desired signal, the 2-path mixer might cancel completely the AM downconverted output signal at node F, if the phase difference between the CLK_{IF1} and the desired IF_1 signal is equal to $\pm\pi/2$. This non-coherent architecture limits the control of the desired signal phase, hence, prohibiting the possibility of implementing a single-IF super-heterodyne architecture, with a direct downconversion from

IF to BB. To overcome this, our architecture proposes a second IF-band providing full resilience to the RF phase shift drawback, as well as, full resilience to the *LO* (CLK_{IF1}) *upconvert modulation* generated by the heterodyne parallel 2-PPM used in the IF_1-band. The remaining LC uncertainty problem is overcome through coherent non-quadrature envelope detection at the second IF. This point will be discussed in section 5.1.4.

The overall frequency response of the IF_1-band presents an innovative methodology on ultra-low power narrow band-pass filtering for high interferer rejection, by means of fully integrated electronics.

5.1.4. IF_2-band section

The IF_2-band is designed to overcome the LC uncertainty drawback limitation and provide linear direct downconversion towards the baseband. To fulfil these requirements a newly envelope detection architecture is proposed.

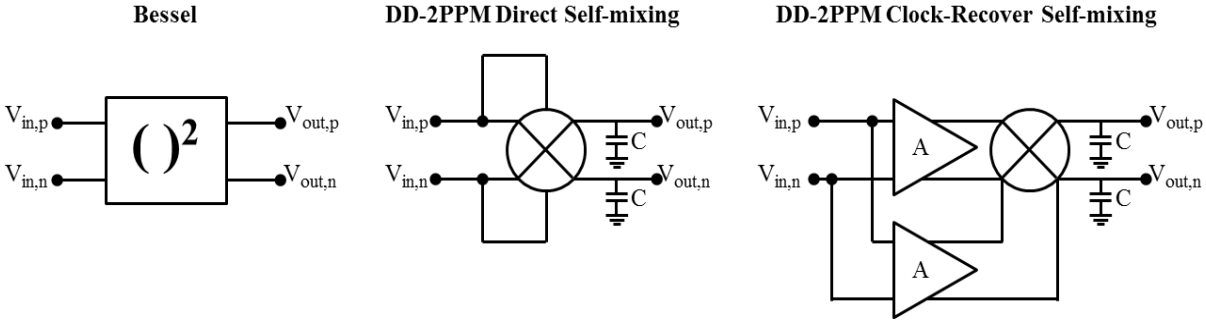


Figure 5.9. Bessel squared function, DD-2PPM direct self-mixing and DD-2PPM clock-recover self-mixing block diagrams.

In this section we analyze three fully differential envelope detectors: the Bessel squared function (Figure 5.9.a) [Meyer] [Pletcher03], the fully differential 2-PPM (DD-2PPM) direct self-mixing (Figure 5.9.b) and the proposed DD-2PPM clock-recover self-mixing (Figure 5.9.c). Figure 5.10 presents the analytical Bessel voltage gain and the simulated DD-2PPM based envelope detection voltage gain as a function of the input voltage amplitude. Here, the input and the output voltages are considered as differential signals ($V_{in} = V_{in,p} - V_{in,n}$ and $V_{out} = V_{out,p} - V_{out,n}$). The sinusoidal input signal is generated from an impedance matched

RF port with $100k\Omega$ source resistance (R_s) modeling the VGA output impedance. This signal is then fed into an ideal balun for differential input signal generation.

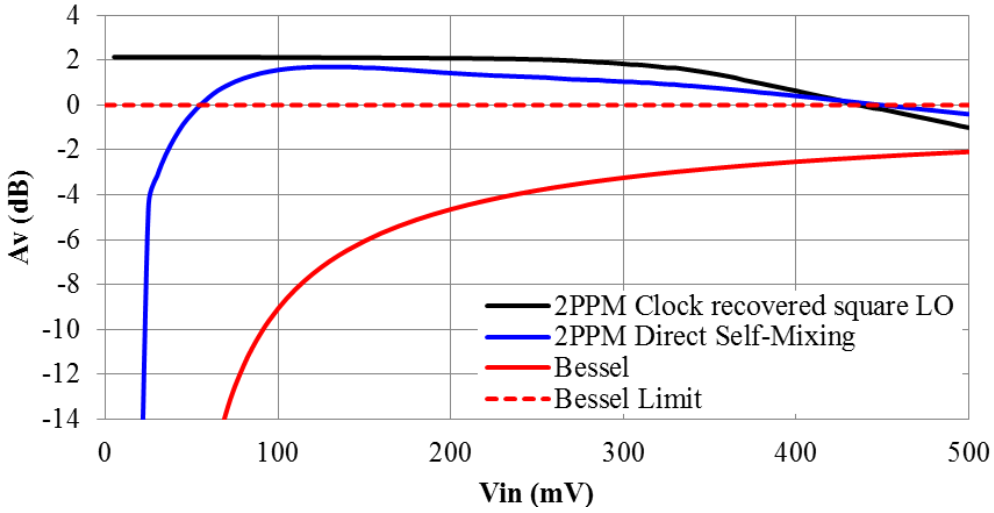


Figure 5.10. Analytical Bessel function voltage gain and simulated 2-PPM direct self-mixing and 2-PPM clock-recover self-mixing voltage gain as a function of the input voltage amplitude. $f_{in} = 10MHz$, $R_s = 100k\Omega$, $R_{on} = 10k\Omega$, $R_{off} = 3.9\text{G}\Omega$, $C = 10pF$, $V_{cm} = V_{gs,on} = -V_{gs,off} = 250mV$ and $\varphi = 0$.

A. Bessel squared function:

In the literature, the most popular self-mixing architecture is the high-frequency diode based envelope detection. This simple topology has proven extremely ultra-low power performances [Roberts] [Marinkovic] [Oh]. Its transfer function is described by the Bessel function reported in [Meyer], and is simply represented as a square function (Figure 5.9.a). The question here is: does this envelope detection square law technique provide an energy efficient zero-IF downconversion? Unfortunately, as the input signal decreases the squared function output response results in a non-linear attenuation. To alleviate this issue, an active amplification stage is usually implemented before the envelope detection. To compensate the non-linearity, feedback or forward loops with variable gain stages are required. The entire solution results in a non-suited energy efficient solution. Figure 5.10 plots the voltage gain response of this architecture. At low input voltage amplitudes, the square function architecture presents strong attenuation. As the input signal increases, the voltage gain rises

towards its maximum limit, roughly set at $0dB$. This architecture is not suited for voltages below $150mV$, for which attenuation exceeds $6dB$.

B. Fully differential 2-PPM (DD-2PPM) direct self-mixing:

From our previous analysis developed in Chapter 3, a fully differential 2-PPM (DD-2PPM) connected in a self-mixing configuration may be also used as an envelope detector (Figure 5.9.b). The main advantage of this solution is its near zero power consumption. However, since the switch-transistors of the DD-2PPM are directly driven by the input signal, their frequency response is strongly dependent of the input signal amplitude. Also since the switch on-resistance of the MOS transistors is inversely proportional to its V_{gs} voltage, the DD-2PPM input impedance presented to the previous stage would vary exponentially. These two considerations result in a response as shown in Figure 5.10. This architecture presents a wide linear region providing passive voltage gain between $60mV$ and $440mV$. Over this region, the voltage gain presents a constant degradation describing the impact of the $1/I_{ds}R_{on}$ efficiency, which is optimized at the low voltage weak-inversion regime. For input voltages below $60mV$, the structure presents an aggressive exponential attenuation. For input voltages above $440mV$, the output signal saturates due to the reduced V_{gs} voltage of the mixer switch MOS transistor.

C. Proposed DD-2PPM clock-recover self-mixing:

In order to overcome the non-linearity gain problem, a novel OOK N-path based envelope detection architecture is proposed (Figure 5.9.c). At the input of this section (Figure 5.9.c), the signal is split in two different paths: one which provides linear amplification and high output impedance to the N-PPM, and another one which affords very high amplification, until signal saturation, in order to generate a clock recovery from the desired OOK signal and provide the rail-to-rail clock driving the N-PPM. This proposed novel topology takes advantage of the N-PPM highly-linear and gain boosted response, to ensure bandwidth reduction and direct downconversion to DC, while removing the undesired effect of the LC uncertainty.

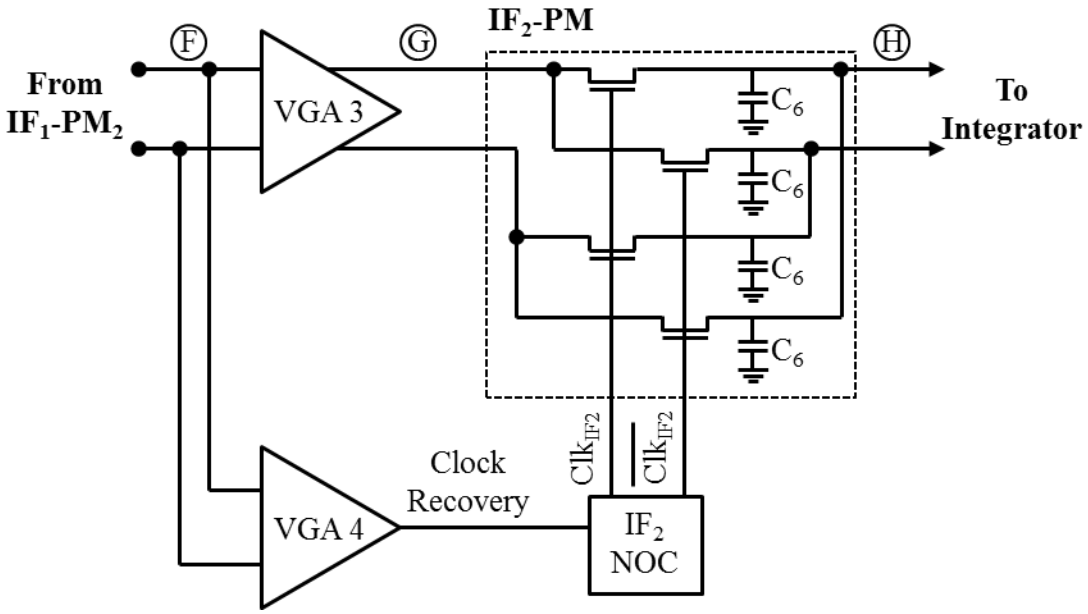


Figure 5.11. IF_2-band simplified block diagram.

Figure 5.11. shows the simplified block diagram of the IF_2-band. It is mainly constituted of two VGAs, an IF_2 non-overlapping clock generator and a fully differential 2-path passive mixer. At node F, the signal is highly amplified by VGA4. The signal is converted to a single ended output for large signal sinusoidal symmetry and power saving from the standpoint of clock IF_2-PM driving buffers. Here, the overall gain of the VGA4 and the non-overlapping clock digital blocks provides clock recovery from the desired input signal. The resulting clock recovered signal at the IF_2 Non-Overlapping Clock (NOC) output (CLK_{IF2}) is a non-overlapping squared signal, and its frequency is proportional to the data rate of the OOK modulated input signal. On the other hand, the VGA3 linearly amplifies the input signal from point F to point G. The N-path filter effect of the IF_2-PM reduces the signal bandwidth (at node G) in a band-pass-like behavior, centered at the IF_2 desired signal carrier frequency. The DD-2PPM (IF_2-PM), ensures direct downconversion to baseband. The low-pass network loading the mixer attenuates the high order harmonics (3, 5, 7…) generated by the CLK_{IF2} upconvert modulation. As shown in Figure 5.10, the proposed N-path based envelope detection with squared LO driving signal, offers a gain boosted and highly linear gain over a very large input range. Instead of implementing the extra amplification stages required to overcome the signal attenuation of previous architectures, this configuration implements a linear amplification stage on the signal path and a strongly saturated amplification stage on the clock path. This results in a very efficient technique to provide passive voltage gain while reducing the effective extra noise bandwidth. Excluding the

voltage gain provided by VGA3, the voltage gain provided by the mixer it-self, from node G to node H, is defined by the fully-differential 2-PPM gain expression presented in 3.51. For high input voltages, the mixer response saturates and the gain is degraded. This effect is principally due to the switch non-linearity which is related to the variation of the on-resistance with respect to the input signal amplitude. Indeed, as the input voltage amplitude increases the effective V_{gs} of the switch transistor at the on-state is decreased, and the on-resistance increased. Despite this behavior, the gain presented at $V_{in} = V_{dd}$ still higher than the one provided by the Bessel function and very close to the N-path based direct self-mixing configuration.

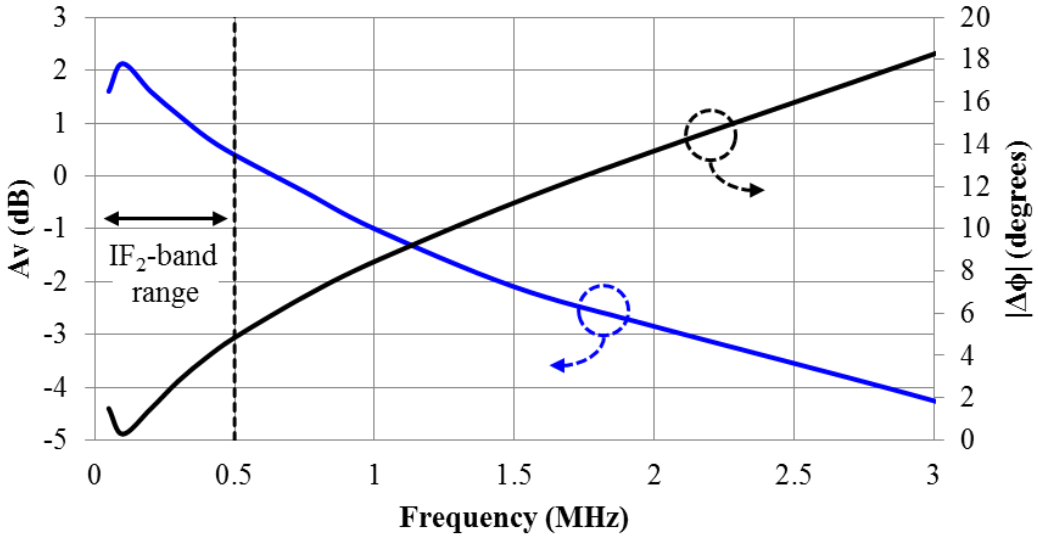


Figure 5.12. Simulated effect of frequency on the IF_2-PM voltage gain and phase difference between the signal at node G and the clock recovered CLK_{IF2}. $R_{VGA,out} = 205k\Omega$, $R_{on} = 10k\Omega$, $R_{off} = 3.9\text{G}\Omega$, $C = 3pF$, $V_{cm} = V_{gs,on} = -V_{gs,off} = 250mV$.

In order to avoid signal cancellation at the output node of the IF_2-PM, the phase shift between the clock-recovered signal CLK_{IF2} and the mixer input signal (node G) is maintained close to zero. This is guaranteed by setting the clock-recovered frequency (IF_2 frequency) at a very low frequency ($< 500kHz$), such as to present a negligible IF_2 NOC delay time compared to that of the desired the IF_2 frequency. Figure 5.12 shows the effect of the phase shift (between the signal at node G and the clock recovered CLK_{IF2}) on the IF_2-PM voltage gain with respect to the IF_2 frequency. As frequency increases, the inherently delay time of the IF_2 NOC becomes relatively comparable to the input carrier frequency ($\omega_c = \omega_{IF2}$). This results in a phase shift increment that degrades the voltage gain of the whole mixer. If the

phase difference continues to rise up to $\pi/2$, the signal at the output of the IF_2-PM is completely canceled. In the case of this WuRx, the maximum frequency of the IF_2-band at node G is defined below $500kHz$. The phase shift is therefore hold below five degrees, providing a passive voltage gain above $0dB$.

As previously discussed, the VGA-DD2PPM configuration of this second IF band generates a narrow band-pass filtering around the signal itself. The question here is: does this filtering operation helps to improve the overall receiver interferer rejection? To answer this question we need to consider the basic principle of envelope detection. In the case of a single-tone input signal, the envelope detector self-mixes the desired signal and downconverts it to DC. On the other hand, in a two tones input signal configuration, the envelope detector downconverts both input signals to DC, resulting in an overlapped DC signal that corrupts the output of the system. In the same way, if two different tones with equivalent amplitude power are applied to the input of the proposed envelope detection, the clock recovery path would generate a modulated signal clock, therefore creating corruption on the downconverted output signal. This phenomenon is translated into BER degradation.

The fact of having a VGA-DD2PPM architecture on the IF_2-band only reduces the in-band excess noise but the entire interferer rejection is mainly attributed to the effective band-pass filtering provided at the IF_1-band. For this WuRx receiver the maximum CIR is equal to -35dB at $5MHz$ (Figure 5.8).

Figure 5.13 shows the overall frequency response of the IF_2-band, including all previous WuRx stages (RF and IF_1 bands), at the F and G signal-path nodes for a zero phase shift between the two mixing signals. Here, the frequency response includes the overall voltage gain of the previous WuRx stages. For simulation flexibility, the clock recovering path is here replaced by an ideal non-overlapping squared clock with center frequency at $250kHz$. At node F, the frequency response of the IF_1-PM_2 follows a sharp low-pass filter shape. The amplified signal at node G is band-pass filtered again, around the IF_2 carrier recovered signal ($CLK_{IF2} = 250kHz$) by the IF_2-PM.

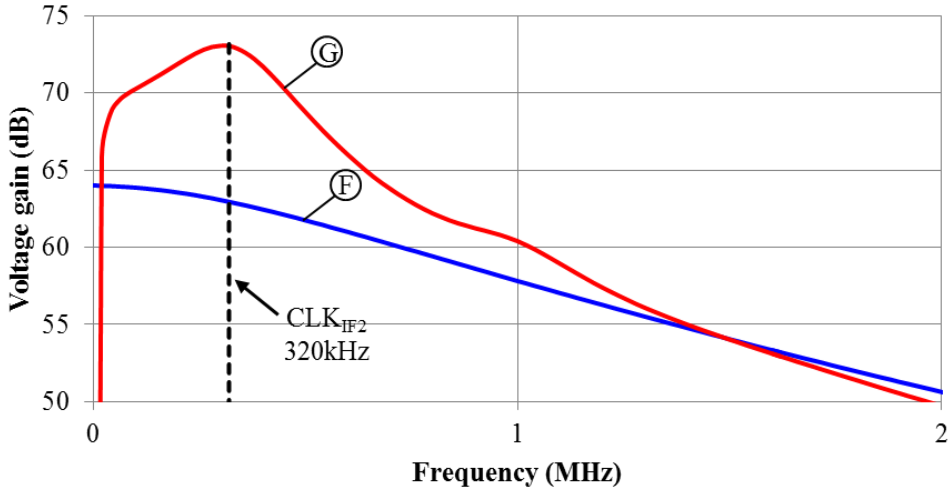


Figure 5.13. Frequency response of the IF$_2$-band at signal-path nodes F and G. 2-bits VGA3 gain tuning set to maximum, $CLK_{IF2} = 250kHz$, $\varphi_{IF2} = 0$.

5.1.5. Base-band section

The baseband section is implemented in order to: reduce the excess in-band noise by integration [Zhou], amplify the signal and convert it into a one bit digital signal. This signal defines the overall WuRx output signal and is used to awake the main radio of the sensor node in case of wake-up signal detection.

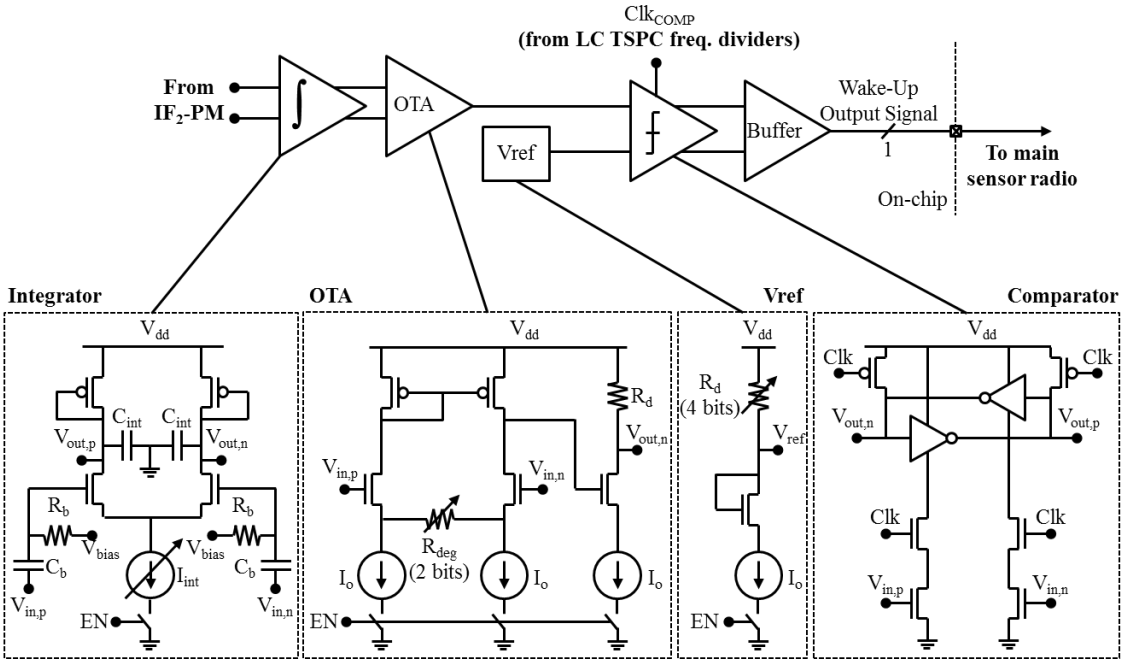


Figure 5.14. Simplified base-band schematic.

Figure 5.14 shows the simplified base-band schematic. At the BB the output signal of the IF_2-PM is low-pass filtered to remove all the high frequency CLK_{IF2} harmonics. To ensure immunity against DC offsets, the integrator is AC coupled through a high-pass filter to allow only the reception of signals with data rates higher than $2kb/s$ (minimum effective frequency higher than $1kHz$). The fully differential integrator profits of the high impedance of the diode-connected P-MOS transistors and the integration capacitance (C_{int}) to set a very low corner low-pass cutoff frequency. Considering the integrator tail current I_{int}, the low-pass cutoff frequency is written as

$$f_{c,int} = \frac{I_{int}}{C_{int}V_{dd}} \tag{5.14}$$

In order to provide a linear dynamic range up to the cutoff frequency according to the data rate received, the proposed lossy integrator has a variable current source. Apart from the linear response, this solution results in large area saving if we consider integrated tunable capacitors providing a variable capacitance range between $10pF$ and $100pF$. Figure 5.15 shows the integrator frequency response for different bias currents. As suggested by equation 5.14, the integrator low-pass cutoff frequency is directly proportional to the current consumed. In the case of this integrator, the maximum data rate $(DR_{max} = 2/T_{c,int}\ [kb/s])$ for an OOK input signal is equal to $20kb/s$, $100kb/s$ and $200kb/s$ for a current consumption of $50nA$, $250nA$ and $500nA$, respectively. To avoid BER degradation, the minimum data rate frequency of the desired OOK signal must be higher than $1kHz$.

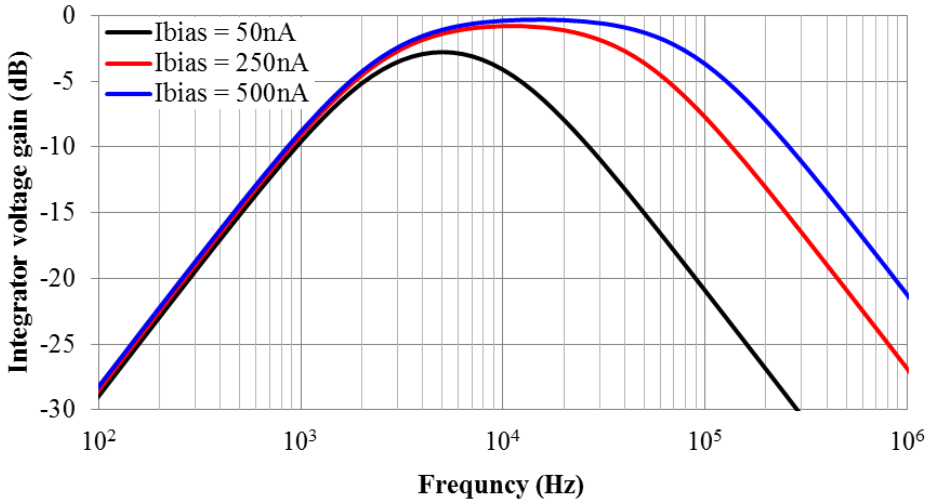


Figure 5.15. Lossy integrator frequency response for different bias current values.
$C_{int} = 12.5pF$ and $V_{cm} = V_{dd}/2$.

After the integrator, the OTA provides variable voltage gain (2-bits) and transforms the differential signal into a single-ended signal. The OTA output stage is composed of a common-source with high output impedance ($Z_{out} \approx R_d$). For symmetry performance, the reference voltage provided to the comparator is given by a replica of the OTA output stage. A four bits variable resistor is implemented in order to provide different voltage levels comprised between $V_{cm} = V_{dd}/2$ and V_{dd}. The comparator is implemented using a fully differential flip-flop architecture. The driven clock signal ($CLK_{COMP} \approx 1.17MHz$) is derived by the LO frequency through eleven cascaded true single-phase clock frequency divider stages. The $1.17MHz$ frequency is chosen such as to oversample the maximum OOK data rate signal by a factor of twenty. The output buffer stage provides a single ended termination to send the recovered signal to the main sensor radio.

5.1.6. Duty-cycled operational mode

For flexibility purposes on WSN applications, the overall WuRx is implemented with an enable circuitry common to all stages. This feature allows the WuRx to work in an extremely low-power operational mode allowing high node battery lifetime enlargement.

Considering the duty-cycle ratio D, defined as the ratio between the on-interval and the signal period

$$D = \frac{T_{ON}}{T} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \tag{5.15}$$

Where T is the duty-cycle time period, T_{ON} is the on-time interval of the system and T_{OFF} is the off-time interval of the system. The average power consumption for a duty-cycled WuRx is therefore written as

$$P_{WuRx,avg} = DP_{WuRx,act} + (1 - D)P_{WuRx,leak} \tag{5.16}$$

Where $P_{WuRx,act}$ is the WuRx active power consumption and $P_{WuRx,leak}$ is the leakage power consumption drained during the off-time interval. For heavy duty-cycled systems, the minimum power consumption of a duty-cycled system is limited by the leakage power consumption of the WuRx. In order to optimize this parameter, high voltage threshold low-power (*hvtlp*) N-MOS transistors are used for the enable tail switches.

5.2. Wake-up receiver physical implementation

The low-cost and compact WuRx is implemented in STMicroelectronics flip-chip 65nm CMOS technology. The external inductors are implemented in a dedicated BGA packaging hosting the flip-chip die and the external SMD components. Dedicated BGA RF Electro-Magnetic (EM) and parasitic analysis is provided in order to guarantee optimum performances of the receiver. The co-designed integration introduces other SMD decoupling capacitances for optimum DC biasing generation and on-board test measurements.

5.2.1. IC implementation

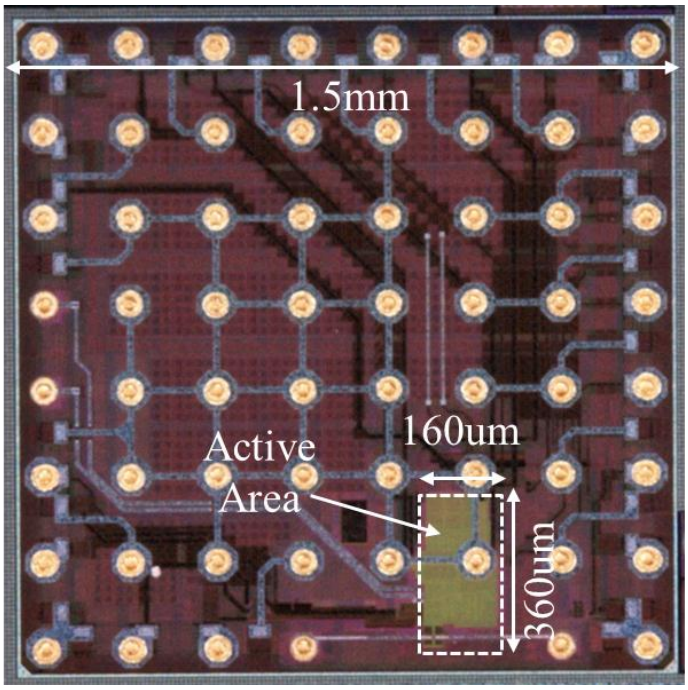


Figure 5.16. Test-chip photomicrograph.

The IC is implemented in a LPGP 65nm CMOS technology. The flip-chip die has a 8x8 matrix bump architecture with a symmetrical pitch of $200\mu m$. Only the two external pad rings are used for useful signal access. The internal pads are used as a central ground plane common to the entire circuit. The pads have specific ESD protection, according to the node type (RF, Analog or Digital). An industrial high performance ultra-low parasitic capacitance ESD protection $(C_{ESD} = 50fF)$ is implemented on the most critical RF nodes of the system: the antenna RF input and the nodes connecting to the SMD components (L_1 and L_2). Multiple

test buffer stages are integrated in the flip chipped IC in order to measure the signal response at different points of the WuRx signal path. The WuRx power supply voltage is $500mV$. Separate power supplies are used for the test circuitry so as to differentiate its power consumption from the one of the WuRx. A dedicated $1.2V$ SPI is also implemented for test facility purpose. A specific level shifter network between the SPI and the WuRx control bit nodes is used to step-down the voltage control level from $1.2V$ to $0.5V$. Figure 5.16 shows the full flip-chip test-chip photomicrograph. The area of the whole die is $2.25mm^2$ due to the multiple test nodes and the wide flip-chip pad minimum required pitch. Only $0.0576mm^2$ area is attributed to the active WuRx circuit.

The FEMN capacitors C_1 and C_2 are respectively implemented as a 4-bits MIM capacitor with an LSB capacitance of $50fF$ and a 2-bit tunable MOM capacitors with an LSB capacitance of $20fF$. The RF-PM is implemented using small size transistors ($W/L = 0.8\mu m/0.1\mu m$) for power optimization and is loaded with a $3pF$ MIM capacitance. This circuit was designed in order to use a front-end SMD inductor (L_1) of $12.55nH$ with a quality factor of 34. However, due to some miss-considerations done during the IC post-layout parasitic extraction of the routing paths going to the antenna pad and the external L_1 inductor, its value was reduced to $4.7nH$ with a Q-factor of 33, therefore degrading the overall front-end voltage gain by approximately $6dB$.

The $2.4GHz$ LC resonator is implemented by using a $10nH$ SMD inductor (L_2) with a quality factor of 34. Electro-magnetic and parasitic extraction are performed for the nodes connected to the inductor, in order to reduce theirs parasitic capacitance and their series resistance, by using stacked low-resistive top metal layers. The 5-bits capacitor banks of the LC core are implemented by a combination of MOM and MIM capacitances with a LSB capacitance of $23fF$. The 4-bits tunable tail current is implemented using low threshold voltage high-performance analog (lvthpa) transistors to allow high current density with very reduced gate-to-source voltage. An hvtlp switch transistor is stacked to reduce the current leakage, when the enable node (EN) is set in off-mode. The differential LC oscillator output is first AC coupled and then buffered through two cascaded inverter stages to provide the desired LO amplitude to the RF-PM.

The IF amplification chain is implemented with all transistors biased in weak-inversion regime. The R_bC_b DC input decoupling (see Figure 5.7) is provided according to the

bandwidth of interest at each node of the signal-path. The VGA amplifiers are designed with a 2-bits degeneration resistance, with $R_{LSB} = 50k\Omega$. The IF passive mixers are designed with small size switch transistors and a load capacitance of $500fF$, $1.75pF$ and $3pF$ for the IF_1-PM_1, IF_1-PM_2 and IF_2-PM, respectively. The baseband integrator capacitance (C_{int}) is designed using MIM capacitances with an effective value of $12.5pF$. The current source tuning is implemented through a current mirror network, which uses an external current source for test flexibility, according to the data rate of the OOK desired signal.

Simulation results present a RF front-end voltage gain of $9.4dB$ at $5MHz$ DC offset ($f_{IF1} = 5MHz$). The LC oscillator frequency tuning range is defined between $1.77GHz$ and $2.53GHz$ and its phase noise is $-100dBc/Hz$ at $1MHz$ offset and $f_{LO} = 2.4GHz$. At $2.4GHz$, the LC oscillator consumes $51\mu W$ (buffers included). The power consumption of the frequency divider chain is $10\mu W$. The IF-LNA amplifier provides an in-band voltage gain of $28dB$ for a power consumption of $15\mu W$. The VGAs provide four different voltage gains defined between $3dB$ and $14dB$ with a power consumption of $3\mu W$.

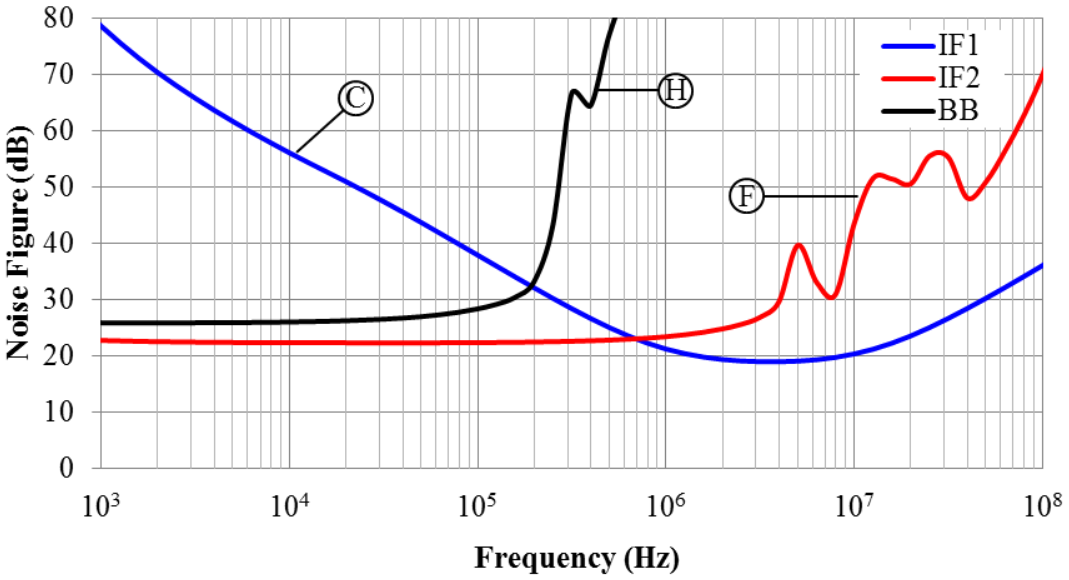


Figure 5.17. Simulated WuRx noise figure response at the different IF_1, IF_2 and base-bands. $f_{LO} = 2.395GHz$, $f_{CLK,IF1} = 4.68MHz$ and $f_{CLK,IF2} = 320kHz$.

Figure 5.17 presents the simulated WuRx noise figure response at the different IF_1, IF_2 and base bands. The in-band NF at the IF-LNA output (node C) is $19dB$. The high NF level at this node is principally due to the post-layout miss-consideration of the antenna and the FEMN node connecting to the external L_1 (point A), which increased our noise figure

estimation approximately by $4dB$. At the IF_2-band, the in-band noise figure is increased by $3.55dB$ due to the SSB and the CLK_{IF1} harmonics folding downconversion effects, as predicted by the analysis made in section 5.1.3 (the 0.2dB difference is due to the simulation setup that only includes seven harmonics for convergence facility). The different IF_2 high frequency NF peaks corresponds to the low-gain present at the downconverted even harmonics of the square clock CLK_{IF1}. At the BB, the in-band noise figure is increased again by $3.55dB$ and a peak is observed at the downconverted even harmonic of CLK_{IF2}.

The simulation results of the proposed WuRx, indicates a global power consumption of $97\mu W$. Considering the frequency offset between the IF_1 desired signal and the clock CLK_{IF1}, the overall voltage gain range of the receiver is defined between $60dB$ and $82dB$. Therefore, considering the maximum $(-2dBm)$ and the minimum $(-24dBm)$ detectable voltages at the comparator, the RF input dynamic range is defined between $-62dBm$ and $-106dB$.

The previous analysis gives us an approach of the minimum detectable power that can be reached by the proposed WuRx. For a $NF = 27dB$, an $SNR_{out,min} = 8dB$ and an effective bandwidth of $10kHz$ and $50kHz$, the minimum respectively sensitivity to achieve a 10^{-3} BER, is

$$S_{min} = -99dBm \qquad \text{at } 10kb/s \text{ data rate} \tag{5.17}$$

$$S_{min} = -92dBm \qquad \text{at } 50kb/s \text{ data rate} \tag{5.18}$$

Figure 5.18 shows the simulated transient response along the signal path of the WuRx. Here, an OOK modulated $2.4GHz$ input signal, equally alternating '1' and '0' symbols, is fed at the antenna RF input. The signal input power is set to -92dBm with an RF-band $SNR_{in} = 0dB$. The LO frequency is equal to $2.395GHz$, therefore, the IF_1 and IF_2 downconverted signals are respectively centered at $5MHz$ and $320kHz$. As we can observe, the noisy RF input signal is progressively filtered along the WuRx signal-path and generates a successfully 1-bit digital output signal. This simulation results show the N-path filtering efficiency, allowing the detection of low power OOK modulated RF signals in a noisy environment.

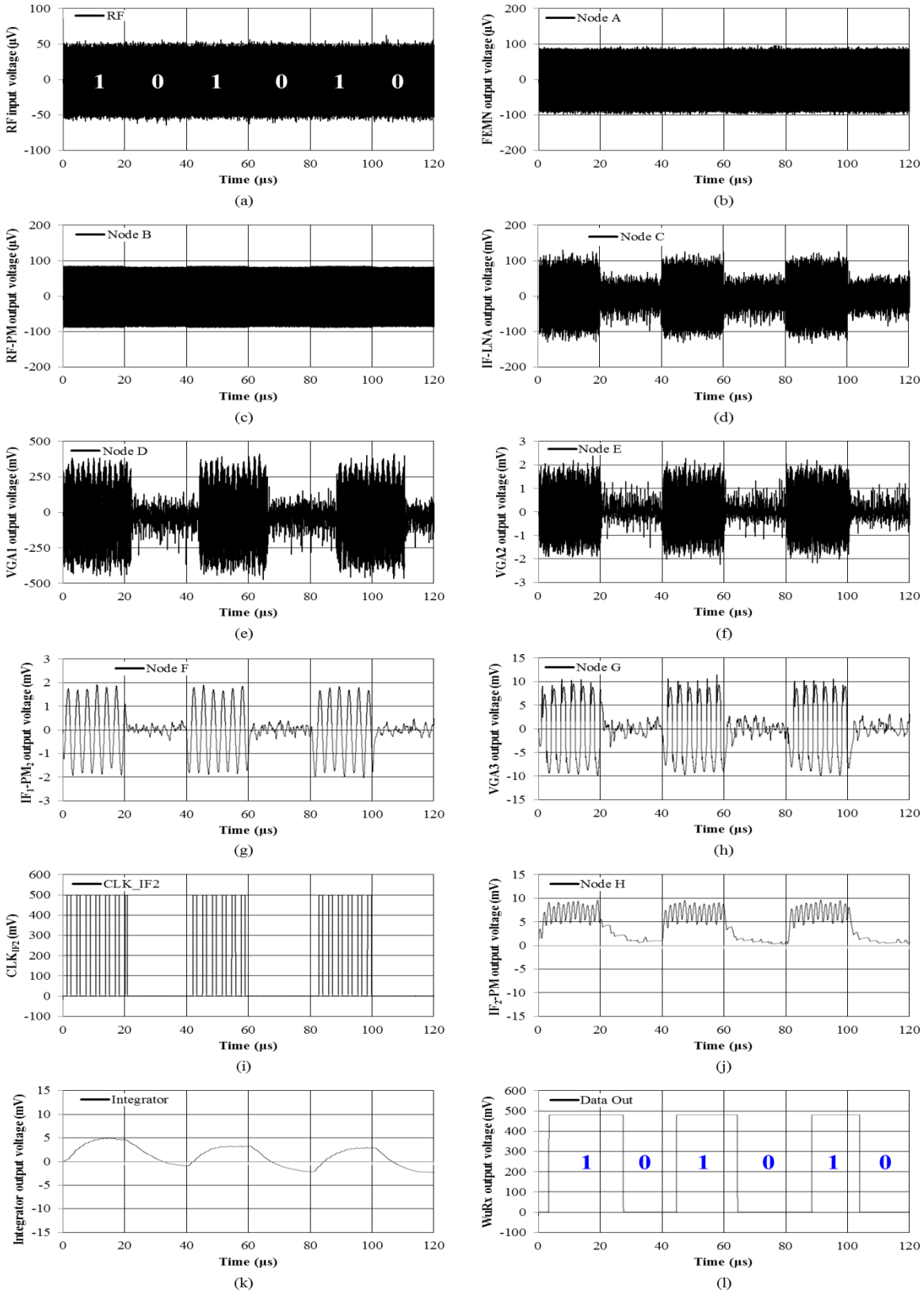


Figure 5.18. Simulated transient response along the signal path of the WuRx.

$P_{in} = -92dBm$, $SNR_{in} = 0dBm$, $DR_{OOK} = 50kb/s$, $f_{RF} = 2.4GHz$, $f_{LO} = 2.395GHz$, $f_{CLK,IF1} = 4.68MHz$, $f_{CLK,IF2,recovered} = 320kHz$, $I_{int} = 125nA$.

5.2.2. Packaging implementation

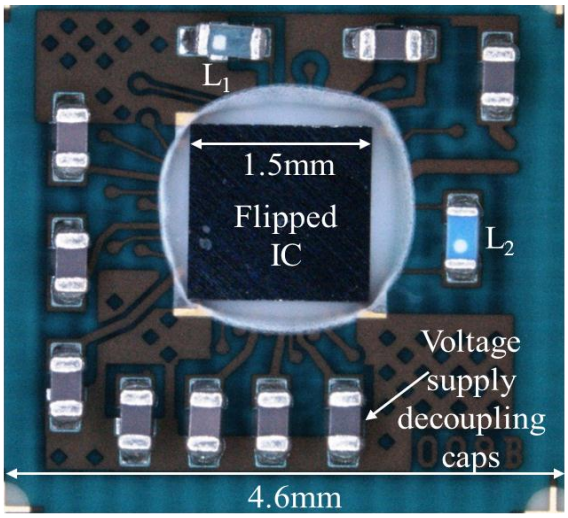


Figure 5.19. Assembled BGA top view photo.

In order to minimize parasitic elements of the RF paths connecting the SMD external inductors, a dedicated compact and low cost four metal layer BGA packaging is designed, providing the possibility to host the flip-chip IC and the SMD components in its cavity. Figure 5.19 depicts the BGA top view photo, including the assembled flip-chip die and the $600\mu m\ x\ 300\mu m$ SMD devices. The $4.6mm\ x\ 4.6mm$ BGA uses a $200\mu m$ pitch 8 x 8 bumps configuration (top metal layer) to host the flipped IC and a $500\mu m$ pitch 8 x 8 balls configuration (bottom metal layer not depicted) to drive out the IC signals. The two RF surface mounted inductors L_1 and L_2, are integrated the closest possible to the IC, according to the minimum allowable space defined by the BGA design rules. Dedicated EM and routing-path parasitic minimization is provided to the nodes connected to the SMD inductors. The exceeding cavity free-space is advantageously exploited by integrating nine extra supply decoupling capacitors. The output signal distribution uses only the two external BGA ring balls for test measurements facility.

5.2.3. Prototype measured results

The WuRx prototype frequency response measurement setup is shown in Figure 5.20. A dedicated PCB with a dedicated power management unit has been designed in order to provide proper bias voltage from separate power supplies. A mechanical push arm is used for practical test purposes to ensure contact connection between the BGA and the PCB. The IC SPI is directly driven from an Arduino Nano FPGA, which is controlled through a Matlab

program. DC biasing is provided from external voltage and current controlled sources. Frequency response measurements are made by injecting a single signal tone from a Rhode & Schwarz SMU200A vector signal generator, at the antenna node of the WuRx. Results are recorded by a Rhode & Schwarz, FSUP, spectrum analyzer.

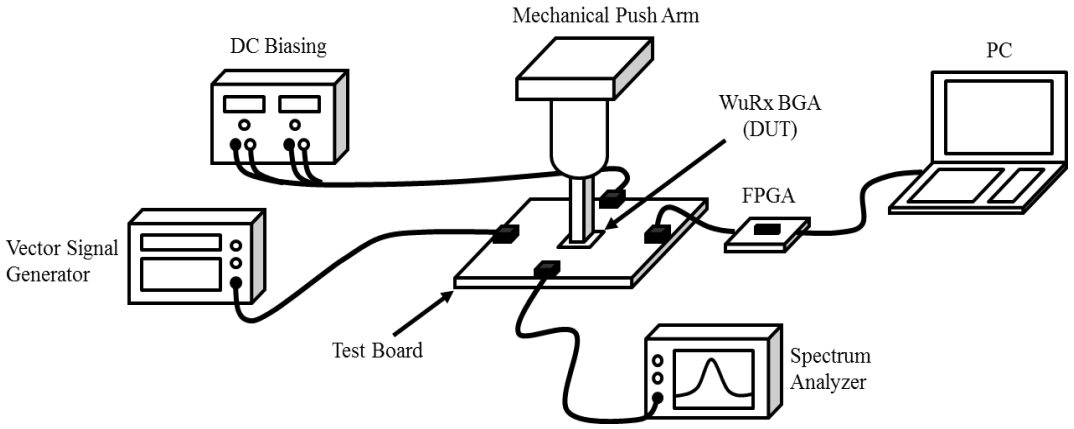


Figure 5.20. Measurement setup for WuRx frequency response.

The clock generation chain is measured at three different points: the LO frequency, the CLK_{IF1} frequency and the recovered clock CLK_{IF2}. The LC-DCO presents a frequency tuning range from $2.31GHz$ to $2.703GHz$, which represents 16.6% of tuning range with respect to the targeted $2.4GHz$ (Figure 5.21). The 5-bits digital controlled oscillator presents an average least significant bit frequency step of $12.5MHz$. The tunable frequency follows a pseudo-linear function, rather than an exponential one, due to the reduced tunable C bank capacitance value, compared to the overall parasitic capacitance of the system.

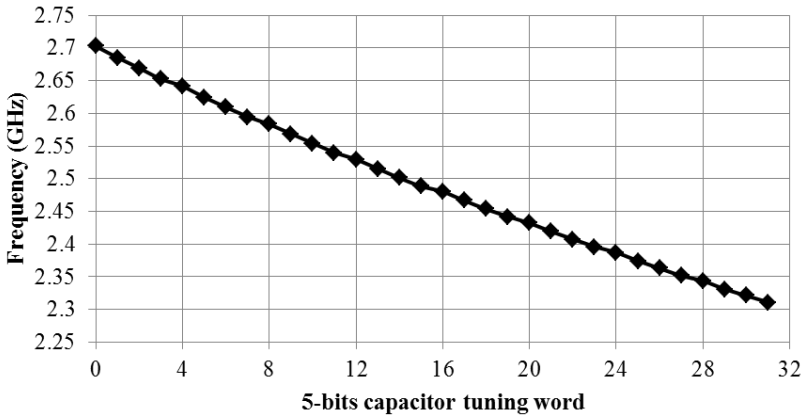


Figure 5.21. Measured LC-DCO frequency as a function of the 5-bits capacitor tuning word.

Figure 5.22 presents the measured LO spectrum at $f_{LO} = 2.4005GHz$ with $50MHz$ frequency span. Spurs from the squared $4.68MHz$ CLK_{IF1} appear on the LO

spectrum due to the CLK_{IF1} and LO test circuitry buffers, that drive high load of currents ($> 25mA$) and share the same voltage supply, thus generating a signal coupling between each other. These spurs are, nevertheless, $40dB$ below the LO carrier signal. As previously specified, since the voltage supply of the WuRx and the test circuitry are independent, spurs are avoided by turning-off the CLK_{IF1} and LO test circuitry buffers. This effect do not affects the normal functionality of the WuRx.

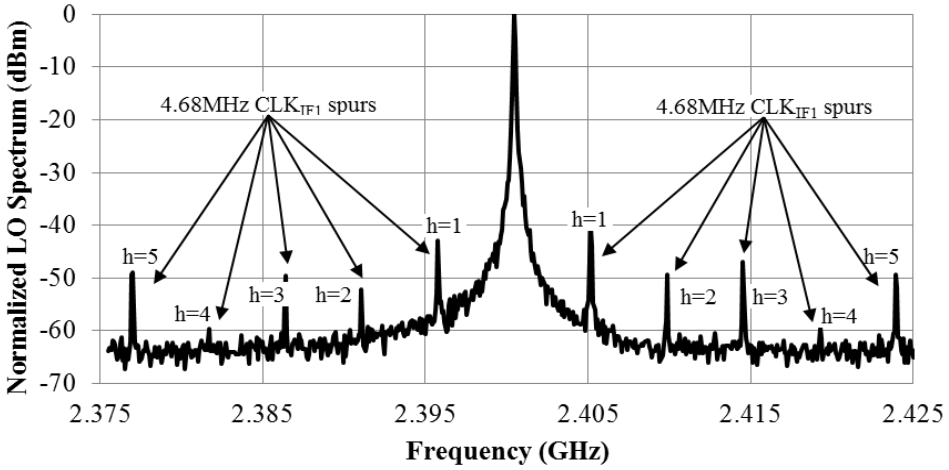


Figure 5.22. Measured LO spectrum at $f_{LO} = 2.4GHz$.

The wake-up receiver is designed such as to be calibrated by a One-Time Programmable (OTP) system. For practical measurements purposes, the LC oscillator is programed directly from Matlab. Once the LO is set at the desired frequency (in this case $2.395GHz$), the oscillator is allowed to free-run. Figure 5.23 shows the measured 22° C instantaneous free-running LO frequency over 5 hours. The frequency shift is equal to $\pm 68.5kHz$, which is equivalent to $\pm 28.6ppm$. It has to be noted that the LO frequency follows a pseudo-periodical variation behavior due to the test room temperature variations, which is in this case regulated at $\pm$1°C difference from the standard 22°C. Effectively, the frequency shift is equal to $\pm 15kHz$ and the $\pm 68.5kHz$ represents the LO frequency drift within $\pm$1°C variation. Considering the $500kHz$ IF_2 bandwidth at point F (Figure 5.2), and an IF_2 desired signal with a carrier frequency centered at $320kHz$, the maximum allowable LO frequency drift is $180kHz$. As depicted in Figure 5.23, the LC-DCO frequency remains below this maximum allowable frequency drift, confirming the possibility of using unlocked "low-Q" LC resonators. Temperature induced frequency deviations may be easily compensated by periodical re-calibrations, not affecting the average power consumption of the whole receiver [Pletcher01].

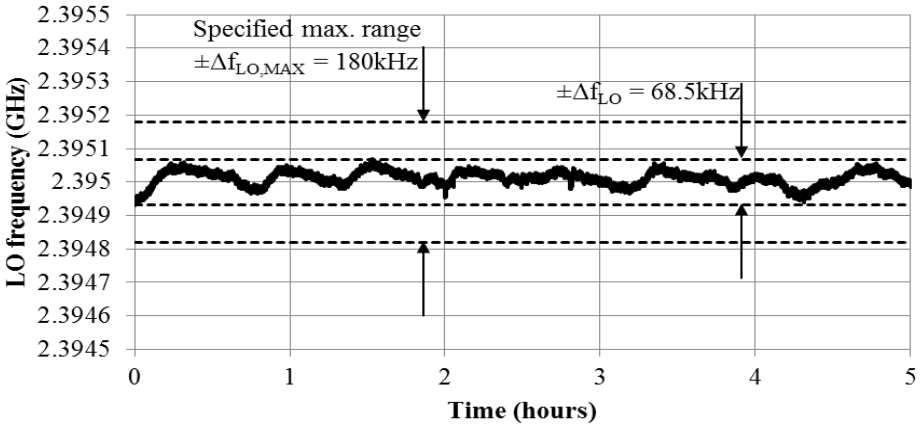


Figure 5.23. Measured 22˚C instantaneous free-running LO frequency.

As discussed in section 5.1.3, the phase noise of the oscillator is inherently related to the maximum attainable interference rejection of the system by means of reciprocal mixing. Figure 5.24 shows the measured and the simulated phase noise of the $2.395GHz$ LC resonator. Given the LO uncertainty, the spectrum analyzer's PLL bandwidth is set to its maximum (30kHz). Hence, phase noise measurements are meaningful for frequencies above $100kHz$. Compared to simulation results, measurements show a very high 1/f noise corner frequency set at $8MHz$. This is probably due to the combination of two effects: On one side, the 1/f noise related phase noise of the oscillator is higher than expected due to electro-magnetic coupling generated between the LO test buffer and the SMD inductance routing paths. This introduces dissymmetry on the differential architecture and increases sensitivity to common-mode noise sources. On the other side the measurement results show a better phase noise performance at high frequencies. This indicates that the Q of the oscillator tank is actually higher than expected. Measured results present a LO phase noise of $-71.6dBc/Hz$, $-101.2dBc/Hz$ and $-125.2dBc/Hz$ at $100kHz$, $1MHz$ and $10MHz$ offset, respectively. With $44\mu W$ power consumption and $-101.2dBc/Hz$ phase noise at $1MHz$ offset, the LC-DCO presents a figure of merit [Kinget] of $-182dBc/Hz$. According to this, and considering equation 2.6 with a $SNR_{min} = 8dB$ and a $BW = 2BW_{IF1} = 2MHz$ (taking into account the complex image IF_1 frequency), the maximum reachable CIR at $5MHz$ offset is equal to $-48dB$. This result meets the $-35dB$ IRR specifications shown in Figure 5.8 at $5MHz$ offset. The spurs coming from the CLK_{IF1} feedthrough are visible at 4.68MHz and 9.36MHz as in Figure 5.22. Note that this spurs are proper to the test circuitry coupling but it does not affects the functionality of the WuRx itself. Compared to the ring oscillator proposed in Chapter 4, this LC oscillator improves the frequency uncertainty and the phase noise

respectively by $900kHz$ and $34dB$ at $1MHz$ offset, at the expense of $31\mu W$ extra power consumption.

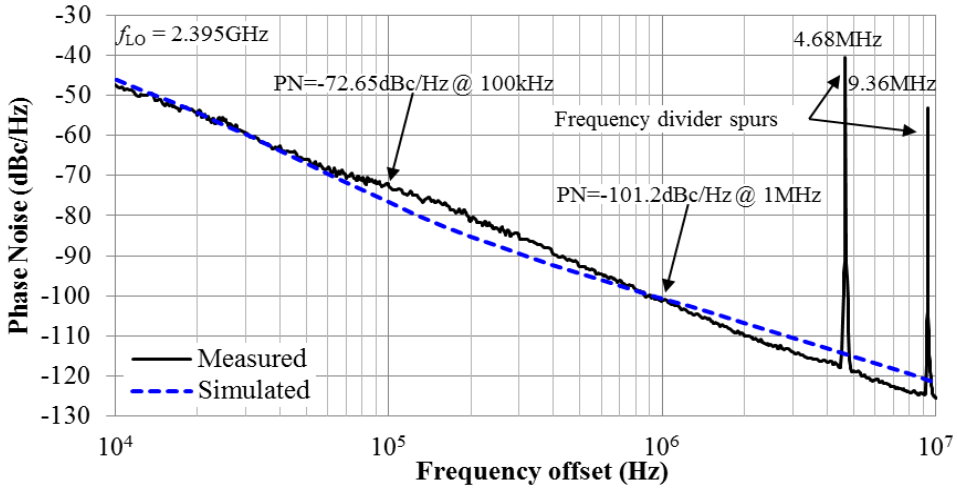


Figure 5.24. Measured and simulated LC-DCO phase noise.

In frequency divider circuits, the phase noise at the output of an ideal N-frequency divider is equal to the input frequency phase noise divided by the N factor ($PN_{out} = PN_{in}/N$). In the case of the proposed WuRx, the $4.68MHz$ CLK_{IF1} frequency is derived from the $3.95GHz$ LO frequency, with a frequency divider factor of $2^9 = 512$. According to the LO phase noise results shown in Figure 5.24, the phase noise of the CLK_{IF1} at $100kHz$ offset should be equal to $-71.6dBc/Hz - 20\log(512) = -125.8dBc/Hz$. Figure 5.25 confirms this behavior by presenting a CLK_{IF1} phase noise of $-123.73dBc/Hz$ at $100kHz$ offset. The $2dB$ difference is mainly produced by the phase noise contribution of the non-ideal frequency dividers and measurement imperfections brought by the equipment tolerance.

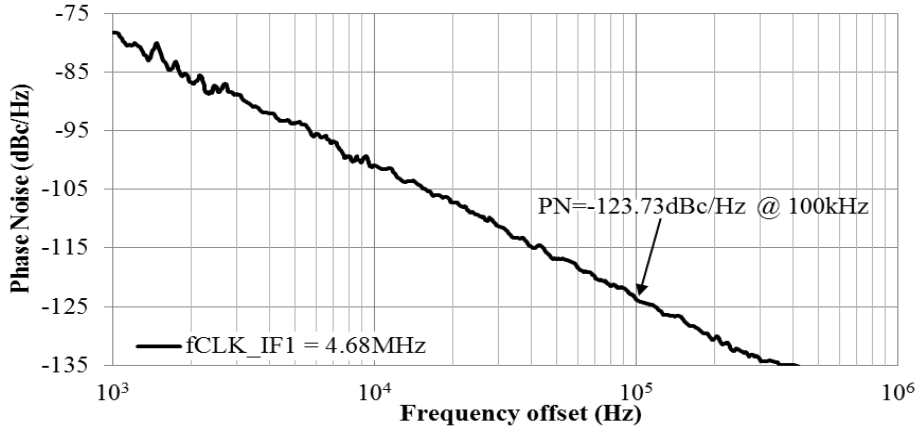


Figure 5.25. Measured CLK_{IF1} phase noise.

Figure 5.26 shows the measured time domain response of the recovered clock CLK_{IF2} for a $-90dBm$ $2.4GHz$ RF input signal with $10\,kb/s$ data rate. The transmitted sequence of alternated "1" and "0" logic symbols are successfully recovered by the WuRx, producing a squared clock signal of $140kHz$ for logic symbols equals to "1". For "0" logic symbols the clock recovery does not generate any clock signal. As the RF input power is reduced, random noisy spikes are generated. The downconversion provided by these spikes at the IF_2-PM mixer output (node H) reduces the signal-to-noise ratio and limits the overall WuRx sensitivity. This in-band noise drawback is common to all envelope detection structures.

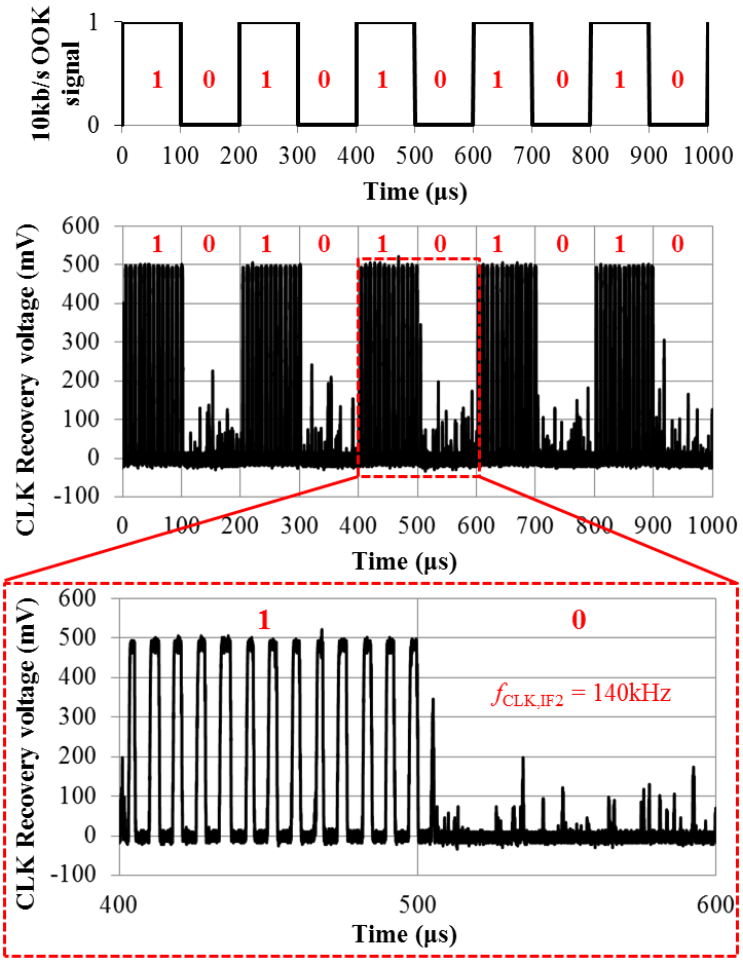


Figure 5.26. Measured time domain response of the recovered clock CLK_{IF2}.
$P_{RF,in} = -90dBm$, $f_{RF,in} = 2.4GHz$, $DR = 10\,kb/s$, $f_{CLK,IF2} = 140kHz$.

Figure 5.27 shows the S_{11} parameter response of the WuRx with a minimum value of $-18.5dB$ with an LO frequency of $2.395GHz$. The circuit presents a wide -10dB range from 2.3GHz to 2.48GHz. Figure 5.28 shows the influence of the digital tunable capacitance

values for C_1 and C_2. As C_1 decreases, the equivalent capacitance C_{eq} (equation 4.3) is decreased and the FEMN resonant frequency $\left(\omega_0 = 1/\sqrt{L_1 C_{eq}}\right)$ is increased; therefore, the S_{11} notch frequency is shifted towards high frequencies. Impedance matching at the LO carrier frequency is obtained when the FEMN resonant frequency matches the one of the RF-PM $(\omega_{LO} = 2.4GHz)$ (Figure 5.28.a). The 2-bits C_1 capacitor provides a wide S_{11} tuning range of $100MHz$. On the other hand, by tuning C_2 the real component of the FEMN input impedance is modified, thus matching can be provided to the RF input (Figure 5.28.b).

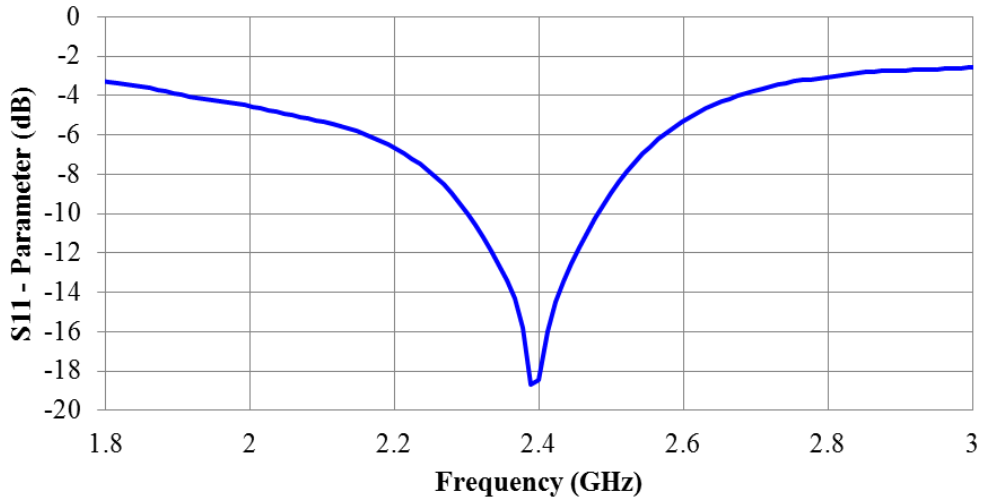


Figure 5.27. Measured S_{11}-parameter of the proposed WuRx.

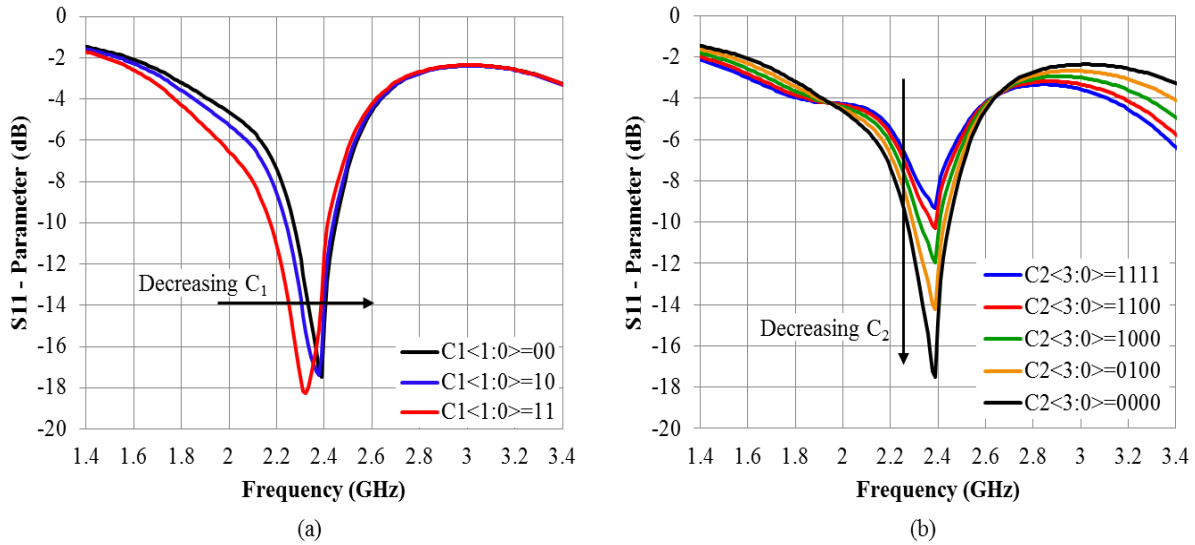


Figure 5.28. Measured S11-parameter response as a function of C_1 and C_2. $f_{LO} = 2.4GHz$

Figure 5.29 presents the measured and the simulated frequency response at the output of the IF-LNA (Figure 5.29.a) and the IF_1-PM_2 (Figure 5.29.b). The normalized low noise

amplifier frequency response describes a second-order BPF shape. The in-band frequency response follows a slightly LPF slope generated by the previous RF-PM stage. The measured bandwidth is about $6.65MHz$ and is defined between $1.45MHz$ and $8MHz$. The voltage gain at this node is equal to $40dB$. Compared to simulation results, the measured IF-LNA response presents a higher HPF cutoff frequency due to the diminution of the effective resistance provided by the DC decoupling (R_bC_b) and the AC coupling (R_dC_d) networks (see Figure 5.7), which in this case was generated by triode MOS transistors. The effective silicon substrate resistance together with the eventual DC offsets and process variations reduced the equivalent HPF resistance by approximately 40%. The measured LPF cutoff frequency is also shifted towards lower frequencies due to some top level routing parasitic capacitance miss considerations. Figure 5.29.b shows the IF_1-PM_2 frequency response presenting a very sharp LPF shape with corner frequency at $450kHz$. The driving clock signal CLK_{IF1} feedthrough into the desired signal through both IF_1 passive mixers (IF_1-PM_1 and IF_1-PM_2), with an equivalent spur power $13dB$ and $32dB$ below the in-band desired signal, for the first and the second CLK_{IF1} harmonic, respectively. Compared to simulated results, the measured IF_1-PM_2 frequency response presents a lower cutoff frequency due to top level routing parasitic capacitance miss considerations.

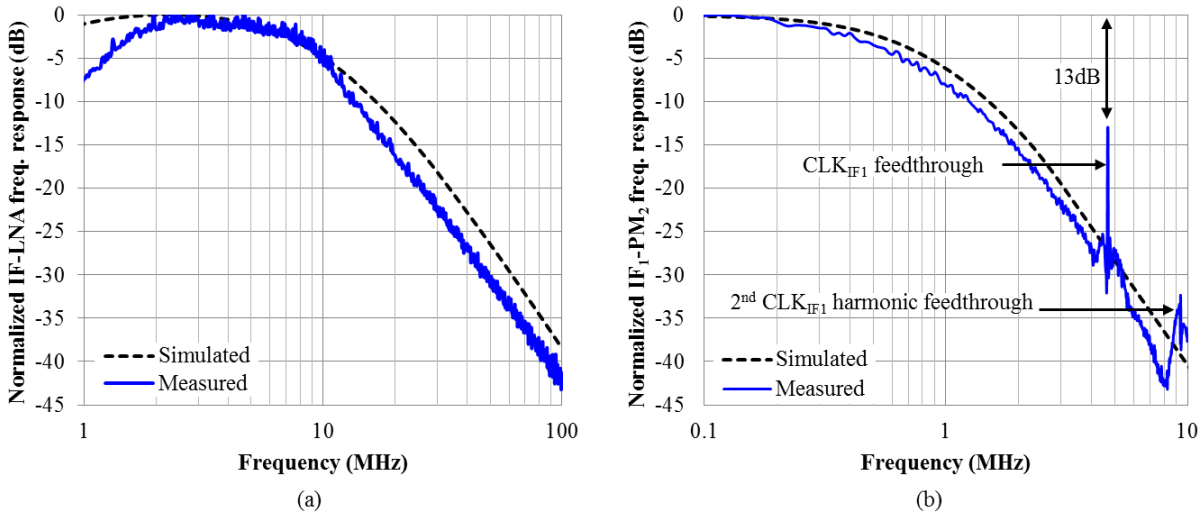


Figure 5.29. Measured and simulated IF-LNA and IF_1-PM_2 frequency response.

As previously discussed, the noise figure of the WuRx is principally defined by the noise contributions of the active IF-LNA. Thanks to the passive front-end voltage gain amplification, the IF-LNA is allowed to drive minimum power consumption for moderate NF contributions. Figure 5.30.a compares the in-band measured and simulated IF_1 noise figure at

the output of the IF-LNA. At $4.68MHz$, the amplifier presents a measured NF of $19.8dB$. Figure 5.30.b shows the influence of the IF_1-PM_2 mixer, which increases the NF by $3.7dB$ due to the image and clock harmonics downconversion that fold into the output spectrum. The measured IF_2 noise figure at $1MHz$ is $23.5dB$. The offset between measured and simulated results for frequencies below $700kHz$, is mainly due to the test buffer amplifier AC input coupling network that reduces the low frequency voltage gain, thus increasing the noise figure. This AC coupling network is proper to the test buffer amplifier. For IF_2 in-band signals, the noise figure for frequencies below $700kHz$, remains constant at $23.5dB$.

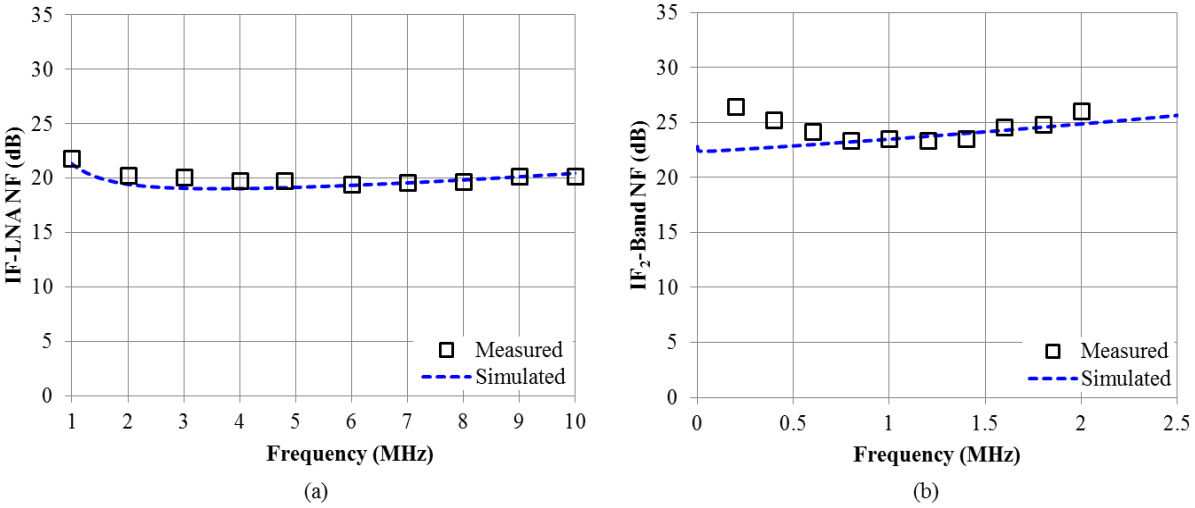


Figure 5.30. In-band measured and simulated IF-LNA and IF_2-Band noise figure.

The WuRx power consumption breakdown is shown in Table 5.1. The WuRx drains a total active power of $99\mu W$ in the always-on mode. The global leakage power consumption when the system is set to its off-mode is equal to $18nW$. A minimum average power consumption of $28nW$ is achieved for a 0.01% duty-cycle.

Wake-up receiver power consumption breakdown									
Block	FEMN	Passive Mixers	IF-LNA	VGA (1-4) & IF_2 NOC	OTA, Integ. and Comp.	LC	LO Buffers	Freq. Divider	**Total**
Power (µW)	0	0	17.4	12.3	3.1	44	12.2	10.3	**99.3**

Table 5.1. WuRx power consumption breakdown.

BER and CIR measurements are done following the setup depicted in Figure 5.31. For one-tone BER measurements, only one of the vector signal generators is utilized. The OOK envelope signal is generated from an 81130A Agilent pulse-pattern generator. The OOK signal is feed into a Rhode & Schwarz SMU200A vector signal generator, which modulates the OOK signal with the RF desired carrier frequency, and feeds it into the WuRx. After signal filtering and demodulation, the WuRx 1-bit output signal is recovered by a Tektronix TLA 721 logic analyzer.

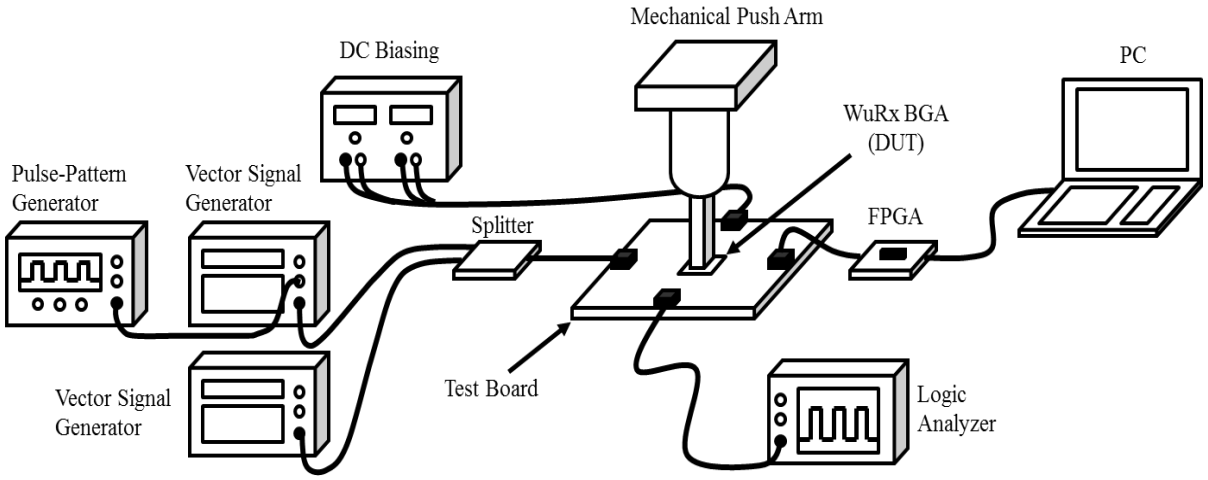


Figure 5.31. BER and CIR measurement setup.

Figure 5.32 presents the measured wake-up receiver bit error rate for $10kb/s$ and $50kb/s$ data rate. The 10^{-3} BER full receiver sensitivity is $-97.5dBm$ and $-92dBm$, respectively . Measurement results are in good agreement with the analysis provided in section 5.2.1.

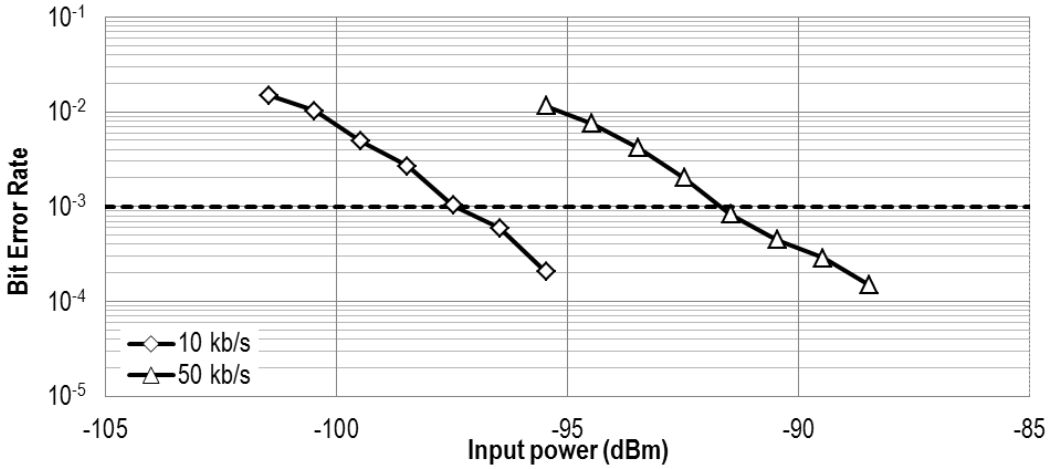


Figure 5.32. Measured Wake-Up Receiver bit error rate for different data rates.

Figure 5.33 presents the carrier-to-interference ratio for a 2.4GHz OOK RF signal at 3dB above the minimum sensitivity ($P_{CARRIER} = -94dBm$). A 10^{-3} BER CIR of -31dB and -27dB at +/- 5MHz offset are respectively measured in the most unfavorable test case, with a sinusoidal tone as interferer. This is not so far from the $-35dB$ value obtained in simulations (See Figure 5.8).

For $f_{INTER} = f_{CARRIER}$, the "0" logic symbols of the desired signal are completely drown by the continuous sinusoidal interferer tone. Here, the IF_2-band envelope detector response is simply a consecutive sequence of "1". Measurement results show that the interferer power must be at least four times $(6dB)$ less important than the desired signal power, for a 10^{-3} BER. The same behavior is also reported for interferer frequencies centered at the RF and the IF_1 image frequencies ($f_{INTER} = f_{RF,IMAGE} = f_{LO} - f_{IF1}$, $f_{INTER} = f_{RF\_IF1,IMAGE} = f_{LO} - f_{CLK,IF1} + f_{CLK,IF2}$ and $f_{INTER} = f_{IF1,IMAGE} = f_{CLK,IF1} - f_{CLK,IF2}$). At $f_{INTER} = f_{LO}$, the resulting IF_1 downconverted signal coming from the mixing between the LO and the interferer frequency, falls precisely at DC. Thanks to the DC offset AC coupling of each IF_1 amplifier, the downconverted interferer signal is highly attenuated, hence, providing a minimal CIR of $-57dB$.

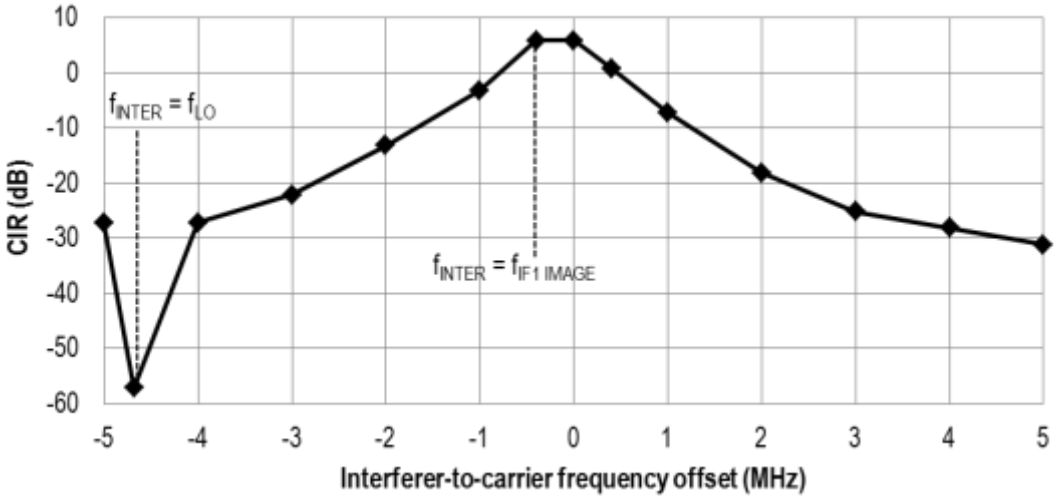


Figure 5.33. Measured Wake-Up Receiver carrier-to-interference ratio at $P_{CARRIER} = -94dBm$ for $10kb/s$.

5.3. Chapter conclusions

In this chapter, we have addressed the design methodology of a fully crystal-less WuRx intended for dense WSN environments. The main target of this design was focused on the optimization of the receiver sensitivity and the development of a robust filtering technique to for high immunity against interferers using multi-layer N-path filters architectures.

The proposed WuRx implements an innovative multi-layer N-path filtering architecture distributed all along the signal-path, which eliminates the need for high-Q RF front-end filters. It also introduces a dual-IF architecture to overcome the drawbacks of LO uncertainty and upconvert modulation generated by the parallel N-PPM at the IF_1-band. Given the single side-band downconvert behavior, each N-path mixer placed in a series configuration adds $3.76dB$ to the global receiver noise figure. A dedicated ULP current-reuse cross-coupled LC-DCO employing a "*low-Q"* (compared to the high MEMS and crystals Q-factor) external SMD inductor is designed to generate the overall time base reference of the system. The CIR and IRR of the WuRx are principally provided at the IF_1-band by the two parallel passive mixers stages. Full resilience to the LO uncertainty and the zero-IF phase shift dependence is provided at the second IF by a novel gain boosted and high linear envelope detection architecture based on N-path filters. Sensitivity optimization is ensured by the sharp filtering provided all along the SP and the in-band excess noise elimination provided by the integrator at the baseband.

The IC is implemented in a LPGP 65nm CMOS technology with an active area of only $0.0576mm^2$. The two external RF inductors employed by the FEMN and the LC-DCO are integrated on the BGA cavity, together with the IC, as SMD devises. Industrial high performance ultra-low parasitic capacitance ESD protections are implemented on the most critical RF nodes connecting to the BGA embedded SMD components. Layout optimization on the antenna and the L_1 SMD routing paths, may increase the passive voltage gain of the FE by $6dB$, hence, the sensitivity may be increased by roughly 3 to $4dB$ up to $-101dBm$ for $10kb/s$ data rate.

Measurement results present a large LO frequency tuning range defined between $2.31GHz$ and $2.703GHz$. Its phase noise is equal to $-101.2dBc/Hz$ at $1MHz$ offset for a power consumption of $44\mu W$ and an equivalent FOM of $-182dBc/Hz$. The S_{11} presented

by the receiver is $-18.5dB$. The overall WuRx drains an active power consumption of $99\mu W$ and its average power consumption drops to $28nW$ for a 0.01% duty-cycle. The WuRx sensitivity at 10^{-3} BER is equal to $-97dBm$ and $-92dBm$ for data rates of $10kb/s$ and $50kb/s$, respectively. The CIR is equal to -31dB and -27dB at +/- 5MHz offset for 10^{-3} BER. Further interferer immunity can be obtained by adding a node ID block at the output of the WuRx. Despite good performance results, this architecture is vulnerable to image frequencies. Given the influence of these image frequencies, the CIR is highly degraded and false wake-up alarms can be raised.

The reader is kindly invited to Chapter 6 for detailed conclusions of this work with respect to preceding works proposed on the state-of-the-art.

Chapter 6

Thesis Conclusions

6.1. Research conclusions

The research work is concentrated on the development of novel ultra-low power high sensitivity wake-up receivers that addresses WSN applications. Ultra-low power design considerations are first provided in order to identify the key parameters offering the possibility to reach the targeted energy, sensitivity and interference rejection specifications. Next, the existing wake-up receiver architectures are reviewed in order to identify their weakness and open-to-improve parts. Afterwards, the concept of 2-path passive mixer structures is analyzed and is presented as the most energy efficient solution to generate narrow band-pass filtering for sensitivity enhancement and interference robustness. Taking into account these structures, novels wake-up receiver architectures that are developed during this work to overcome existing limitations are presented. The proposed circuits are implemented on IC using STMicroelectronics 65nm technology node in order to validate the theory. The silicon measurements show that the proposed wake-up receiver is well suited for dense node WSN applications.

After presenting the ultra-low power considerations, a review of several wake-up receiver architectures including: envelope detection, injection-locking, super-regenerative, sub-sampling, uncertain-IF and low-IF, is provided. Generally speaking, the power consumption of the different architectures is well satisfied with respect to the specifications established for WSN applications. In terms of sensitivity, wake-up receivers finds difficult to reach sensitivity levels beyond $-90dBm$. Almost all the proposed WuRx configurations presented in literature are subject to costly and bulky high-Q external resonators, which is not in line with our specifications established for dense nodes WSN deployment.

In order to overcome this drawback, the 2-path passive mixer architecture is proposed as the most compact and energy efficient solution to overcome the narrow band-pass filtering specifications. An analysis highlighting the advantages and the drawbacks of three 2-PPM architectures including: single-ended, fully differential and parallel configurations, is provided. Key parameters providing electrical 2-PPM optimization for IC implementation including: RF input impedance matching, input interference rejection, output voltage response, BPF quality factor and output noise response, are provided.

A first prototype circuit implementing ULP N-path filters has been designed in STMicroelectronics 65nm CMOS technology allowing the validation of the proposed theory. A passive scheme methodology for Q-factor enhancement has been implemented, using antenna impedance boosting and external IF-capacitors packaging co-design integration. This circuit also validates the design and the implementation of a BGA solution, enabling the possibility of hosting both the IC and external SMD components. This circuit demonstrates the strength of integrated N-path filter structures in providing high-Q BPF responses comparable to the one of high-Q BAWs resonators. One should consider this circuit as a first step towards the implementation of a full WuRx. Further design improvements concerning integrated IF capacitors, accurate LOs, variable voltage gain stages and noise figure reduction should be considered in order to reach the targeted power and sensitivity WSN requirements.

A second circuit including a complete low-cost and compact WuRx is implemented using the same CMOS technology node. The proposed WuRx implements an innovative multi-layer N-path filtering architecture distributed all along the signal-path, to alleviate the need of high-Q RF front-end filters. It also introduces a dual-IF architecture to overcome the drawbacks of LO uncertainty and upconvert modulation generated by the parallel N-PPM at the IF_1-band. A dedicated ULP LC-DCO employing a "*low-Q"* (compared to the high MEMS and crystals Q-factor) external SMD inductor is proposed. An innovative gain boosted and high linear envelope detection architecture based on N-path filters is also presented. This WuRx is provided with an enable circuitry that is common to all the stages for duty-cycle purposes, in view of extreme power efficient WSN applications. This circuit operates at a $2.4GHz$ RF frequency. An improvement for the packaging implementation compared to the one used in the first circuit is also proposed. WuRx measurement results present a total active power consumption of $99\mu W$ for the full radio and an average power consumption of $28nW$ if a 0.01% duty-cycle is considered. The WuRx sensitivity at 10^{-3} BER is equal to $-97dBm$

and $-92dBm$ for data rates of $10kb/s$ and $50kb/s$, respectively. The CIR is equal to -31dB and -27dB respectively for +/- 5MHz offset for 10^{-3} BER.

	[Pletcher01] 2008	[Pandey] 2011		[Huang01] 2012		[Abe] 2014	[Bryant] 2014		This Work	
Architecture	Uncertain-IF	Low-IF		2-Tones Envelope Detection		2-step Low-IF (Energy Detection RX + Address Detection RX)	Uncertain IF		**Dual-IF**	
Interferer filtering technique	High-Q BAW external passive filter	IF filter		High-Q SAW external passive filter + 2-Tone Transmission		Gm-C filter + Digital bit length	RF N-Path Filter		**Multi-Layer N-Path Filters**	
LO generation	Low accurate ring oscillator	Injection locked ring oscillator		Self-mixing RF diode + External clock		PLL (EDRX) and LCDCO (ADRX)	Unlocked ring oscillator		**Unlocked LC-DCO**	
Modulation	OOK	FSK		OOK		GFSK	OOK		**OOK**	
Power Supply (V)	0.5	1		1		0.7	0.75		**0.5**	
Frequency (GHz)	2	0.402		0.915		0.9244	2.45		**2.4**	
External components	BAW filter	Crystal and FE passive matching network		Crystal, SAW filter and FPGA demodulator		Crystal, FE matching network and FPGA demodulator	Tunable resistor and comparator clock		**BGA Embedded SMD Inductors**	
Duty-cycled	No	No		No		Yes	No		**Available**	
Power consumption (µW)	52	44 (LP mode)	120 (Main mode)	63 *1 (LP mode)	120 *1 (Main mode)	45.5 *2	50 *3		**99**	
Data Rate (kb/s)	100	200 *4		10		50	250	650	**10**	**50**
Sensitivity @10^{-3} BER (dBm)	-72	-70	-90	-56	-83	-87	-88	-71	**-97**	**-92**
CIR (dB) @ +/-3MHz *5	N/A	N/A		-19/-19 *6	-10.5/-10.5 *6	-5/-38 *7	N/A		**-25/-22**	
CIR (dB) @ +/-5MHz *5	N/A	N/A		-19/-19 *6	-10.5/-10.5 *6	N/A	N/A		**-31/-27**	

*1 Excluding FPGA and IF clock generation.
*2 Average power (44.2µW for the energy-detection receiver and 0.1% of 1.3mW for the address detection receiver), FPGA excluded.
*3 Comparator clock excluded
*4 Using on-chip demodulator the data rate is limited to 100kb/s.
*5 CIR = ($P_{CARRIER,MIN\ SENSITIVITY}$ +3dBm)/$P_{INTERFERER}$ [dB].
*6 CIR measured within the two carrier tones.
*7 CIR available only through address detection receiver.

Table 6.1. Performance comparison with state-of-art.

Table 6.1 presents the performance comparison of the proposed WuRx with the state-of-the-art. It is important to remark that other WuRx architectures, such as [Abe] [Brown] [Milosiu] [Sjöland] with different low-IF configurations, [Oh] with an extreme low-power envelope detection WuRx architecture, [Petäjäjärvi] with a super-regenerative configuration,

[Huang04] [Moazzeni01] with very performant sub-sampled architectures and [Bryant] with an uncertain-IF N-path filter based architecture, have been proposed very recently during the last year of this thesis research. Despite their satisfactory performance, our work presented in Chapter 5 remains as the state-of-the-art. Below are the global WuRx design trends of the state-of-the-art:

- In terms of architecture, low-IF and reduced bandwidth uncertain-IF topologies are the most convenient methods to obtain low-power and high sensitivity. Other architectures based on two-tone RF input signal protocols show also high performance, especially in terms of CIR [Huang01]. Nevertheless, this solution demands a dedicated transmitter design which may involve extra design requirements to the already available main radio transmitters. The proposed work combines both low-IF and bandwidth reduced uncertain-IF architectures to enhance the receiver overall sensitivity.
- Sensitivity is still the major target for WuRxs, however, it presents as a parameter that can hardly exceeds $-90dBm$. Our proposed WuRx pushes this boundary and improves the sensitivity to $-97dBm$ with a sub-$100\mu W$ power budget.
- Few WuRx works present CIR performances and none of them fulfill the requirements specified in this thesis for real WuRx implementations for dense nodes WSN applications. This parameter shows as the principal target to be optimized by future WuRxs.
- The new trend of integrated interferer filtering techniques permits the elimination of costly and bulky MEMS resonators (Gm-C or N-path filters). However, most of these ULP architectures still requiring external low-frequency crystal devices, to generate accurate time-base references. Our proposed multi-layer N-path filtering technique overcomes this drawback by means of integrated electronics means.
- WuRxs' power consumptions boundary is defined below $100\mu W$. Almost all architectures are designed with CMOS weak-inversion operational mode architectures to guarantee optimized transistors' power efficiency. OOK modulation proves to be the suited for system energy efficiency performance. The data rate is still a point of discussion, but the trend is to minimize it below $100kb/s$ for high power performance.

- The operation frequency is defined according to the IEEE 802.15.4 and the ISM standards but is principally chosen in order to optimize the electrical constraints in terms of power, inductance value (when concerned) and silicon area. The LO architecture still a dilemma between unlocked or locked schemes. The choice of these topologies has to deal with a power, noise and external component trade-off, and depends on the targeted application specifications.
- Generally speaking, duty-cycling mode in WuRx has not really been developed. Few architectures present this feature, however, they do not present it as an option but as a requirement to achieve low-power performances. This work presents the first WuRx suitable to both reactive and duty-cycled asynchronous WSN applications.

Compared to recent works, the proposed WuRx architecture presents for the first time a dual-IF WuRx architecture using a multi-layer N-path filter configuration for interferer resilience. It also proposes the first sub-$100\mu W$ LC oscillator based WuRx, using a BGA embedded SMD inductor. This WuRx presents the best sub-$100\mu W$ sensitivity, reaching the best level of $-97dBm$ at $10kb/s$ for a 10^{-3} BER. The ingenious multi-layer N-path filter configuration enables the best CIR results obtained in WuRxs, achieving -31dB and -27dB at +/- 5MHz offset for 10^{-3} BER.

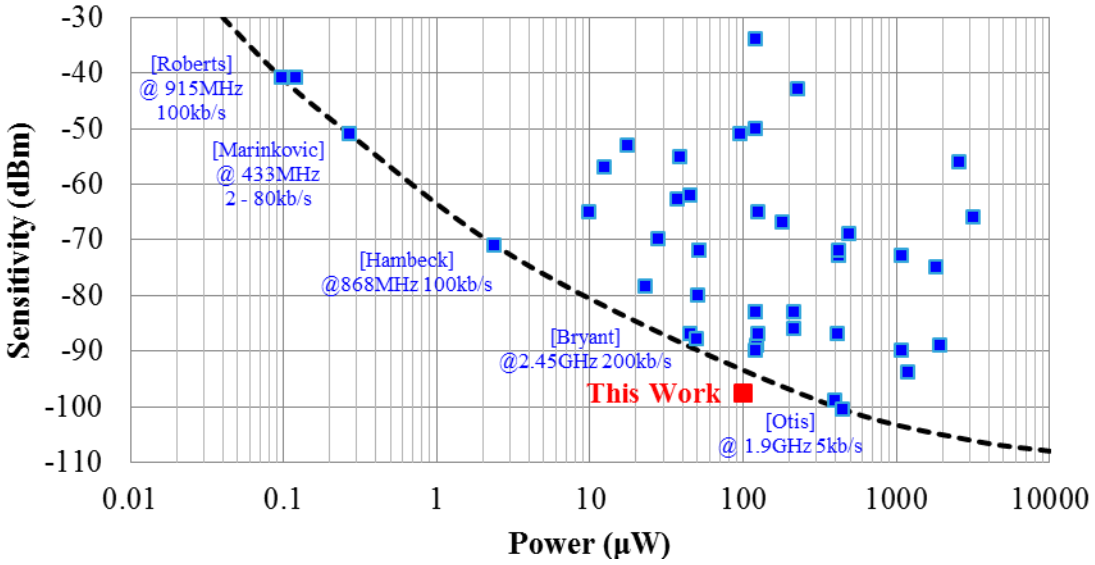


Figure 6.1. Active power consumption and sensitivity performance comparison for WuRx and low-power receivers works.

Figure 6.1 presents the sensitivity performance versus the active power for previous WuRx and low-power receivers works. The proposed wake-up receiver extends and pushes the boundary of the sensitivity versus power WuRx performances with respect to the state-of-the-art. For very low active power performance, the envelope detection based WuRx appears as the best candidate [Roberts]. However, for very high sensitivity performances, BAW resonator based architectures, such as the super-regenerative architecture presented in [Otis01], remain the best. Nevertheless, these BAW dependent configurations do not fulfill the WuRx specifications due to their high power consumptions exceeding $100\mu W$.

Figure 6.2 presents the duty-cycled (0.01% duty-cycle) WuRx state-of-the-art in terms of sensitivity versus power performances.

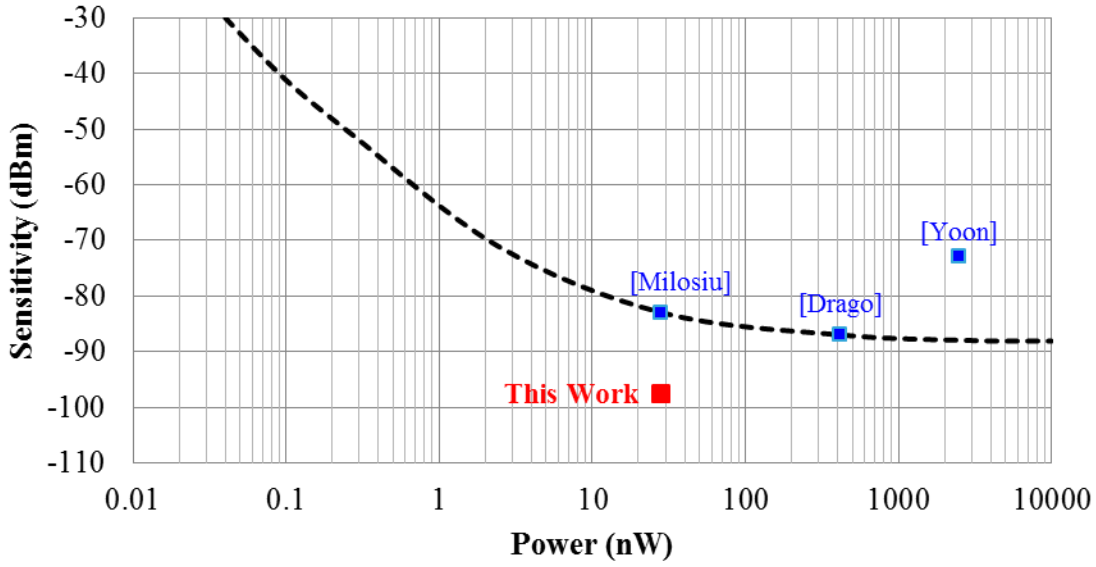


Figure 6.2. Average power consumption and sensitivity performance comparison of previous WuRx and low-power receivers works with 0.01% duty-cycle.

This research work illustrates how architectures based on multi-N-PPM stages can deliver high sensitivity and superb interferer rejection while avoiding high-Q external reference resonators. This wake-up receiver is suited for dense nodes WSN applications, following reactive or duty-cycled asynchronous rendez-vous schemes.

6.2. Future work

Further improvements for the presented WuRx may be obtained through the optimization of several aspects.

- Additional robustness against interferers, especially against image frequencies, may be obtained by a smart implementation providing the WuRx with the ability of receiving wake-up signals labeled with node ID addresses. This feature may be obtained through the implementation of an ULP digital block capable of comparing the received node ID frame, and then proceed to a final decision of waking-up the main radio.
- In view of a fully integrated implementation, high-Q high-inductance value inductors may be studied. Inductance architectures using top metal layers with a stacked configuration may satisfy these requirements, for few extra micro-watts of power consumption.
- A design optimization of the routing paths connecting the external SMD FEMN inductance may be addressed. This would allow a sensitivity improvement of approximately $4dB$, boosting the sensitivity to roughly $-101dBm$.

The flexibility of the N-path filtering suggests that this technique may be extended to other RF blocks, such as Power Amplifiers (PA), found on the transmitter path of ULP transceivers. The idea behind this is to apply the same methodology used for our IF-LNA. In order to avoid high-frequency RF blocks with large bandwidths, the PA may be placed at baseband frequencies with reduced bandwidth and low-power consumption. Placed between the PA and the antenna, a N-PPM may provide the required frequency translation to the desired RF frequency. In this way the PA power consumption would be reduced by approximately a factor of one hundred and the generated RF output spectrum would be a very precise sinusoidal tone contained in a sharp narrow BPF response.

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In October 2011, he joined STMicroelectronics, Crolles, France as a PhD candidate in Microwaves and Micro-Technologies in collaboration with the IEMN-ISEN, University of Lille, France, and the Berkeley Wireless Research Center (BWRC) at the University of California, Berkeley. His research focused on the development of Ultra-Low Power Wake-Up Receivers for Wireless Sensor Network applications. He completed his PhD degree (mention très honorable) in March 2015.