N° d'ordre :41935

THESE

Présentée à l'Université de Lille 1
Ecole Doctorale Sciences Pour l'Ingénieur

Pour obtenir le grade de :

DOCTEUR DE L'UNIVERSITE

Spécialité MICRO ET NANO TECHNOLOGIES, ACOUSTIQUE ET TÉLÉCOMMUNICATIONS

Par

WEI Wei

Process technologies for graphene-based high frequency flexible electronics

Soutenance le 17 décembre 2015 devant la Commission d'examen

Membres du jury :

Mr. Henri HAPPY	Directeur de thèse (IEMN – Lille)
Mme.Mireille MOUIS	Rapporteur (INP –Grenoble)
Mr. Abhay SHUKLA	Rapporteur (Université Pierre et Marie Curie – Paris)
Mr. Dimitris PAVLIDIS	Membre (Boston University – Boston)
Mr. Pierre LEGAGNEUX	Membre (THALES –Palaiseau)
Mr. Jean-FRANÇOIS DAYEN	Membre (IPCMS –Strasbourg)
Mr. Gilles DAMBRINE	Membre (IEMN – Lille)

Acknowledgement

Foremost, I would like to express the deep and sincere appreciation to my supervisor Prof. Henri HAPPY for continuous support of my Ph.D study and research, for his patience, kindness, expertise and excellent guidance. Without his supervision and constant help, it would not have been possible for me to finish this doctoral thesis.

I am grateful to my co-directors Dr. E. Pallecchi and Dr. E. Pichonat, who guide my research work in cleanroom and assist me when I write this thesis. Without their help, it is also impossible to obtain the results that I presented in this thesis. Particularly, I give my deep appriciation to Dr. D. Vignaud, who gave me valuable discussions and sincere help during all my PhD study.

My sincere thanks also goes to Dr. D. Mele, Mr. B. Moez, Mr. M. Khenissa, Dr. X. Zhou and Dr. J. Thielleux, who introduce me and help me to the device fabrication work in cleanroom, and the microwave characterization of the graphene filed effect transistors. Their help are so important and it ensures the high efficiency of my work. Mr. M. Colin helped me for the 3-D image of our device structure and I highly appreciate his help.

Because my work has deep cooperation with other groups, I am also grateful to them. They are: professor C. Luxey and his group; professor L. Tuami and his group for making inkjet printing devices. They are: Dr. G. Deokar, Dr. K. Haechon and company of Graphenea for supporting the high quality graphene and optimizing the graphene transfer process.

I would also like to express my gratitude to all of the engineers in cleanroom who helped me in many ways. They are Mr. M. Francois; Mr. F. Vaurette ; Mr. Y. Deblock; Mr. P. Tilmant; Ms. C. Legrand; Mr. B. Grimbert; Ms. A. Fattorini; Ms. E. Galopin; Mr. M. Dewitte; Ms. I.R. Jeune and Ms. C. Brillard. The engineers in microwave characterization center, who are Ms. V. Avramovic; Mr. E. Okada and Ms. S. Lepilliet.

I would like to thank my reviewers: Professor. M. Mouis and Professor. A. Shukla for their great contribution to review this dissertation and thank Professor. D. Pavlidis; Professor. P. Legagneux; Professor J. Dayen and Professor G. Dambrine for participating in my final defense committee.

I have also to thank all my friends in IEMN who helped me. They are Colin, Theo, Moez, Mohamed, Sarah, Marina, Ewa, Pierre, Nadine, Philipp.Latzel, Philippe Altuntas, Adrien, Natalia, Chong, Jinshan, Justine, Valeria, Jorge, Alain, and I spent a pleasant time with them. We had a rich memory together.

Last but not the least, I would like to thank my family: my parents and my wife. They give me all the supports and love, which endows me power for moving forward.

Table of Content

General Introduction

Flexible electronics has drawn growing attention for the past several years due to its numerous potential applications. The relevant research relies on the existence of suitable fabrication technologies and novel materials. The objective of my PhD work is to develop devices based on flexible substrates. There are mainly two parts involved: (i) passive devices (transmission lines, antenna, etc) fabricated by inkjet printing technology; (ii) Graphene field effect transistors (GFET) fabricated by conventional electron-beam lithography.

In chapter 1, we show how to utilize inkjet printing technology to fabricate passive devices on flexible substrates and the characterization of these devices. Inkjet printing is a promising fabrication technology for flexible electronics due to the advantages of being low cost, mask-free process, waste reduction and compatible with arbitrary substrate. The challenge of this technology is the quality and reliability of printed patterns in terms of geometry. In this work, we firstly present the work of optimizing inkjet printing technology based on Dimatix printer equipment, commercial ink from Suntronic (U5603 - silver nanoparticles based solution) and commercial flexible substrates, KAPTON and PEN. After optimization, we are able to print patterns with well controlled geometry. Some microwave passive devices such as coplanar wave guide and antenna were fabricated. For RF characterization, the device performances were explored with flat (without strain) or bent (strained) substrates. We show that inkjet printing technology has promising potential for flexible electronics.

In chapter 2, we discuss the field effect transistors based on graphene material on rigid substrates. Graphene, a two-dimensional carbon based material, has attracted attentions due to its unique electronic properties. Additionally, the truly two-dimensional nature and strong mechanical property makes graphene very suitable for flexible electronics. In our work, we present the fabrication and characterization of GFETs on rigid substrates. The bottom gate structure using aluminium as metal gate is chosen. The GFET dielectric is formed by the natural oxide of aluminium. This approach is used to avoid conventional atomic layer deposition method, which needs high temperature. Chemical vapor deposition grown graphene on copper foil is adopted, and transferred using an optimized wet transfer process. The high quality monolayer graphene is preserved both after graphene transfer and device fabrication process. Contact resistance is explored by using different transmission line model structures. The transistors with different geometry (gate length of 100, 200 and 300 nm combining with gate width of 12, 24 and 50 μm) is characterized by both static and

dynamic measurements.

In chapter 3, we discuss the fabrication and characterization of graphene field effect transistors on flexible substrates. By using almost the same fabrication process on rigid substrates, we successfully fabricate GFETs on a flexible substrate, kapton. Pure Au is used to form contact metal and low contact resistance is obtained. The transistors with different geometry (gate length of 100, 200 and 300 nm and width of 12, 24 and 50 μm) are characterized by both static and dynamic measurements. We report as measured current gain cut-off frequency ($f_{t\text{-}DUT}$,without any de-embedding) of 39 GHz and maximum oscillation frequency (f_{max}) of 13.5 GHz in devices with 100 nm gate length and 12 μm gate width. To our knowledge, these results reach to the state of the art for flexible GFET. Moreover, the evaluation of RF performances for different substrate bending radius (strain varying from 0% to 0.5%) is discussed and the thermal dispersion of substrate in channel region for different drain source bias is explored. The results presented in chapter 3 further demonstrate the great potential of our process for graphene based flexible electronics.

Chapter I

Inkjet printing of microwave passive components

Table of Content-Chapter I

Chapter I Inkjet printing of microwave passive components

I.1 Introduction

Printed electronics is a set of printing methods for depositing electronic materials (insulating, conducting, and semiconducting) onto arbitrary substrates to create a wide range of devices, such as organic thin film transistors (OTFTs), light-emitting devices (LEDs), diodes, detectors, etc[1-10]. Compared with conventional electronics, printed electronics has attracted attention due to its significant advantages such as compatibility with various substrates (flexible, transparent and low cost substrates, such as paper), low temperature processing, and no requirement for vacuum processing[11-14]. Printed electronics has become a growth industry that already has generated significant revenue. Source from Organic Electronics Association (OE-A) manifests that the sales of products including printed electronics were 23-24 billion US $ in the year of 2014, and future annual growth rates of 20% were predicted.(as shown in Figure I-1).

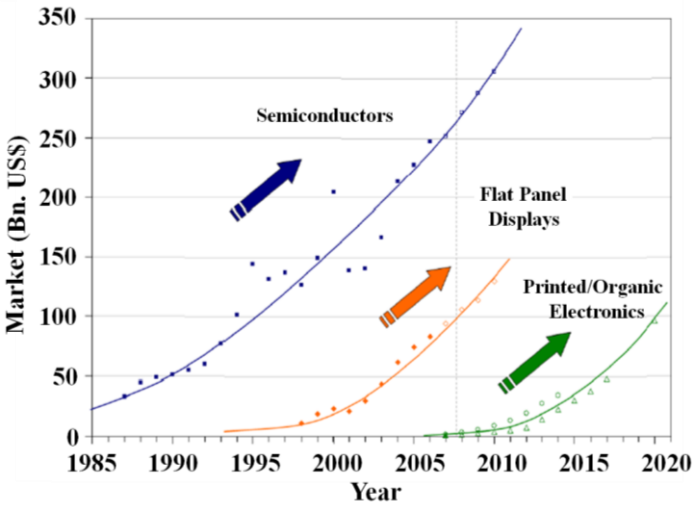


Figure I-1: Evolution of printed/organic electronics market [15]

Inkjet printing is a promising fabrication technology for flexible electronics. However, improving the quality and the reliability of printed patterns in terms of geometry and resolution remains challenging. It means, the printed pattern dimensions must be as close as possible to the designed value, and the pattern defects such as holes and the rough pattern boundary must be well controlled.

This chapter is oriented to the printing technology for design and fabrication of flexible radio frequency (RF) components. At this frequency range, the geometry of

devices has high impact on their performances. The objective of this chapter is to use printing technology to fabricate devices with well controlled geometry. In this work, the inkjet printing technology has been chosen as fabrication technique. Therefore, in the first part of this chapter, I will describe the printing equipment (Fujifilm Dimatix printer) and printing principal associated with commercial silver nanoparticles ink (SunTronic U5603) and flexible substrates of PEN and Kapton. The process optimization will be described in appendix I while the main results will be shown in main text.

In second part, based on optimized printing parameters, the structures of CPW transmission lines with nice printing quality were realized. The RF characterization of these transmission lines combining the considerations of geometric dimensions, sintering temperature, and substrate bending will be presented. For CPW lines on KAPTON, the loss lower than 0.4 dB/mm up to 40 GHz was obtained, which shows possibility to design RF circuits using this technique. Also, it has been found that the RF performance of the CPW lines on KAPTON is minimally affected by substrate bending. Besides, two collaboration works about antenna printing and three omega method structures printing will be shortly presented, which both further indicate the potential of our work for flexible electronics.

Figure I-2 shows two examples of printed achievements in this work: (a) is a pattern of IEMN shaped by array of droplets on PEN substrate; (b) shows a bended Kapton substrate on which the CPW transmission lines with different dimensions have been fabricated by inkjet printing. The study of this new technology was completed in the beginning of my PhD thesis.

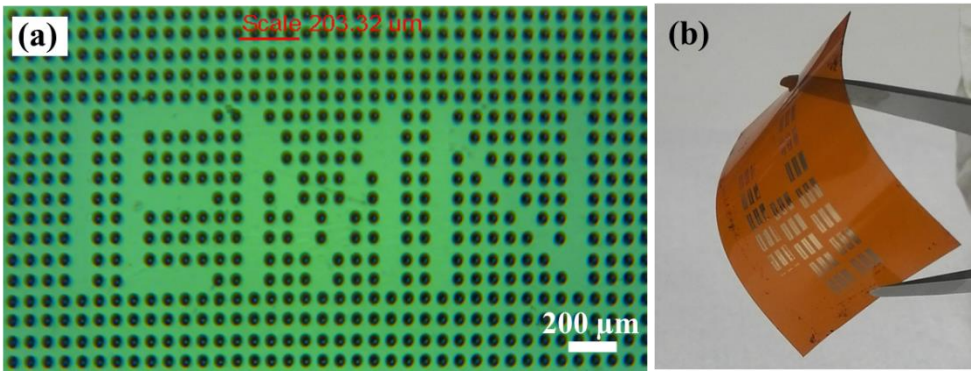


Figure I-2: Examples of some printed results by Dimatix in this work, (a) Pattern of IEMN shaped by array of droplets on PEN substrate; (b) CPW transmission lines on Kapton substrate

I.2 Inkjet printing technology

I.2.1 Inkjet printing working principle

Inkjet Printing is a type of material deposition technique that forms a patterned layer by ejecting ink droplets from a chamber through a hole, called nozzle, onto arbitrary substrates, such as paper, plastic etc. Additionally, an annealing process, or referred as sintering, is necessary to make the ink solvents evaporate leaving a solid layer on the substrate. Figure I-3 (a) shows a typical illustration of inkjet printer, and (b) shows the picture of Fujifilm Dimatix inkjet printer, which is used in this work. The pattern is first designed in a computer, and then is realized by inkjet printing on substrate. Dimatix is based on Drop-on-Demand (DoD) approach[16][17]. All the droplets ejected are directly deposited to the target substrate and form the patterned layer. One major advantage of DoD inkjet printing is that it is a mask-free process, which reduces the cost.

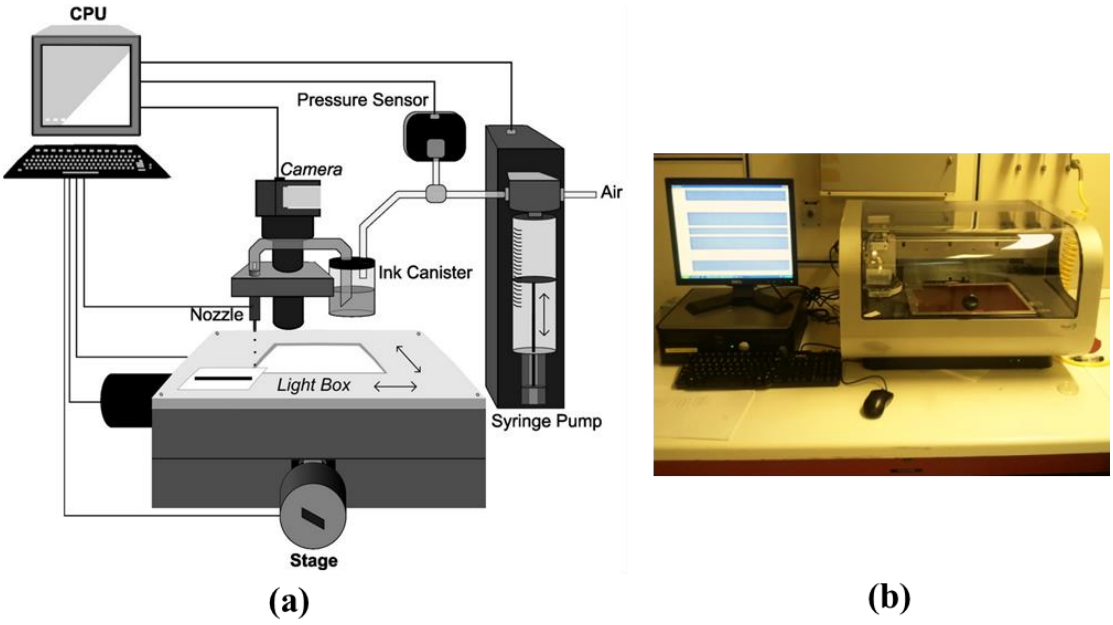


Figure I-3:(a) Illustration of inkjet printer (b) Picture of the Fujifilm Dimatix Materials Printer used in this work, with the screen showing a designed mask.

I.2.2 Description of printing equipment: Dimatix Fujifilm inkjet printer

The Dimatix inkjet Printer is a laboratory tool that enables researchers, scientists, and engineers to evaluate the use of ink jetting technology for new manufacturing processes[18-21]. It is designed to be convenient and easy to carry out “proof of concept”

and development work using inkjet technology. The printer is made up of different components mainly detailed as Figure I-4 shown.

-Cartridge. The part which contains ink materials and ejects ink droplet with a certain formation setting, see more details below section of printing principle.

-Platen. A turntable surface to maintain substrate for printing. It has a vacuum system to maintain flexible substrate as flat.

-Drop watcher. A camera to observe droplet formation in real time. It provides important information, such as, stability, volume and speed of as printed droplets, and by which different parameters could be determined.

-Fiducial Camera. A camera right above the as printed substrate with two main functions: first, to select position where printing originates and also align the pattern position before printing, and second, to verify the printing result after fabrication process.

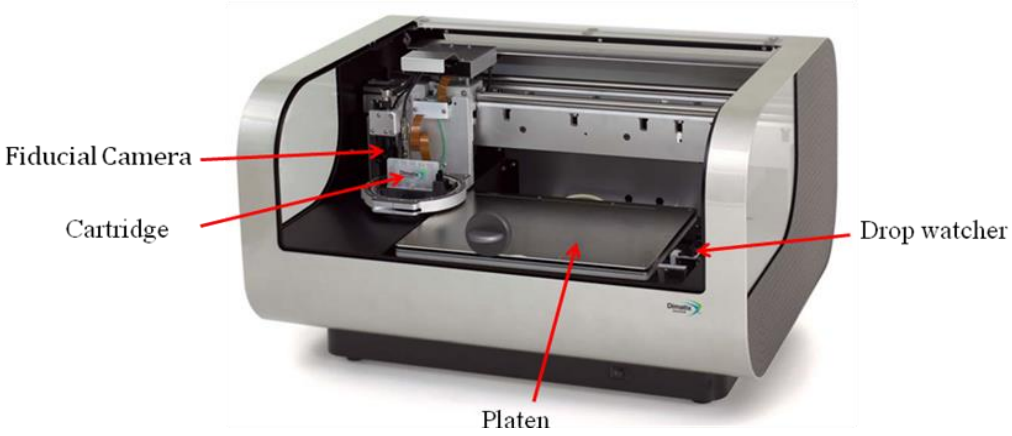


Figure I-4:Picture of the Fujifilm Dimatix Materials Printer

I.2.2.1 Cartridge description

As Figure I-5 (a) shows, with 16 identical nozzles beneath, the cartridge is filled with ink. Each nozzle has been connected with a tube through which the ink is allowed to pass. On one side of the tube a piezoelectric element can be found to induce pressure and depression inside the tube, because this piezoelectric element has shape deformation according to various voltage applied on it. Therefore, by setting different voltage value and their duration time, which is named as waveform parameter (or as drop formation), the jetting process would be accordingly formed. Typically, waveform is divided into four segments, as shown is Figure I-5 (b). Each segment has three properties: duration, level and slew rate. Duration and slew rate are two parameters linked with jetting frequency, which can be defined for inks with different viscosity. Additionally, slew rate can also define the velocity of droplet ejected from nozzle.

Level parameter is used to define the volume of one jetted droplet, and it reflects how much the piezoelectric element would be deformed while duration and slew rate reflects how fast the piezoelectric element verifies.

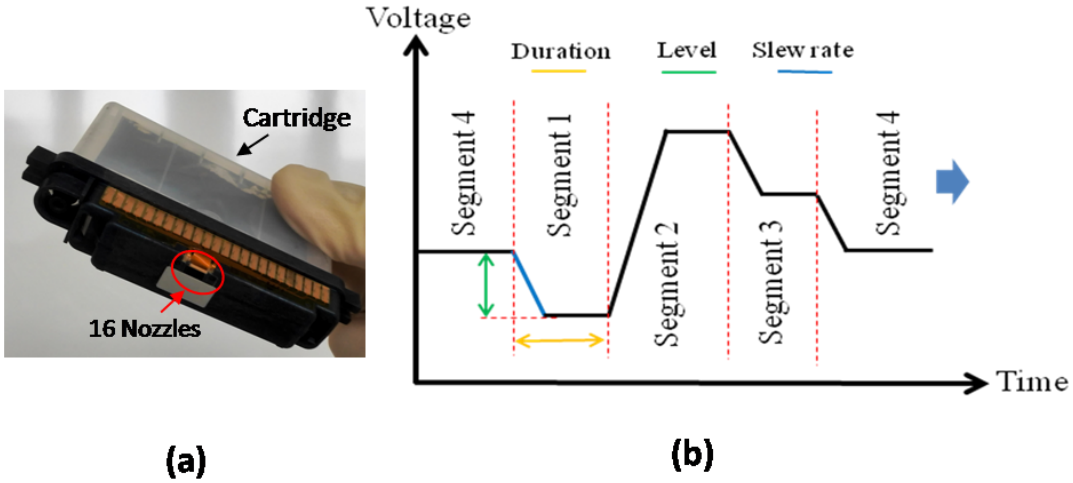


Figure I-5: (a) picture of a cartridge and (b) simplified schematic of waveform for ejection voltage

Figure I-6 gives more details about droplet ejecting process. In segment 1, which is the beginning of an ejecting pulse, a negative voltage makes the piezoelectric element back to a relaxed or straight position from depressed state of segment 4, and the chamber with its maximum volume have the ink pulled in. In segment 2, a main drop ejection phase, the chamber would be compressed by the piezoelectric element with its maximum level and the output pressure would generate a droplet ejected. In segment 3, a recovery phase, the voltage would be set back down and piezoelectric element decompresses a bit to have ink refilled into chamber again. In addition, the pulling back force in this segment is also helping to break off the droplet ejected in previous segment. In segment 4, zero voltage moves the piezoelectric element back to its original position in preparation for segment 1 again. To this end, a cycle of droplet ejecting has been finished.

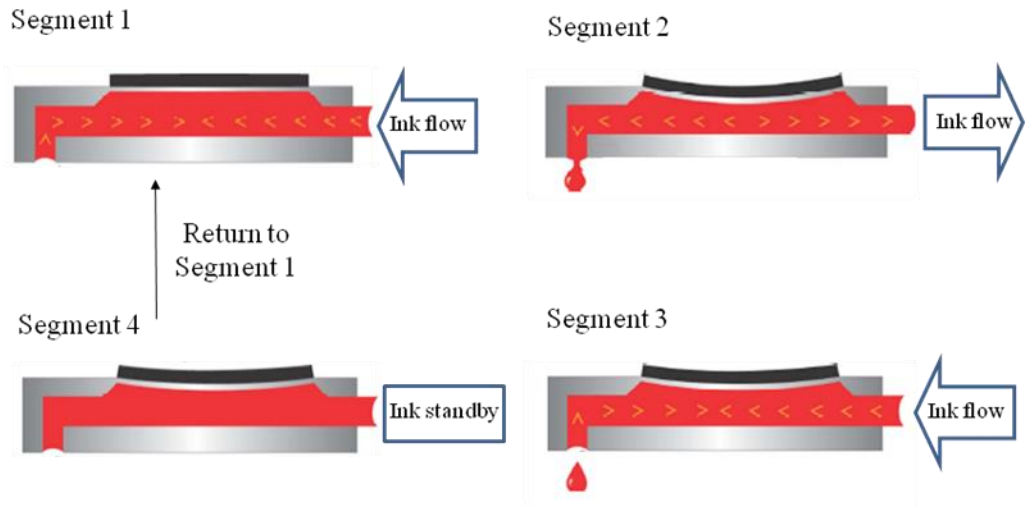


Figure I-6: Schematic of four-segment voltage waveform of the piezoelectric crystal

It is clear now that by verifying the parameters of these four segments: duration, level and slew rate, different drop formation for different viscosity liquid can be obtained. It should he noted that during the printing process, a clean nozzle without clotting by some particles in solution based ink is critical to the head performance. To avoid the cases of blocked fluid path, DMP2800 has a special nozzle cleaning treatment, purging. As a maintenance function, purging will apply air pressure to outside of fluid bag to force ink through entire fluid path and out all nozzles promptly. Therefore, purging is an inevitable action for an error free jetting process.

I.2.3 Substrates

Among the flexible substrates, the properties of PET, PEN and Kapton have retained our attentions for RF application. Figure I-7 represents an image of commercial version of the three substrates, as well as their monomer formulation. Table I-1 provides the thermal, physical and electrical properties of these three substrates.

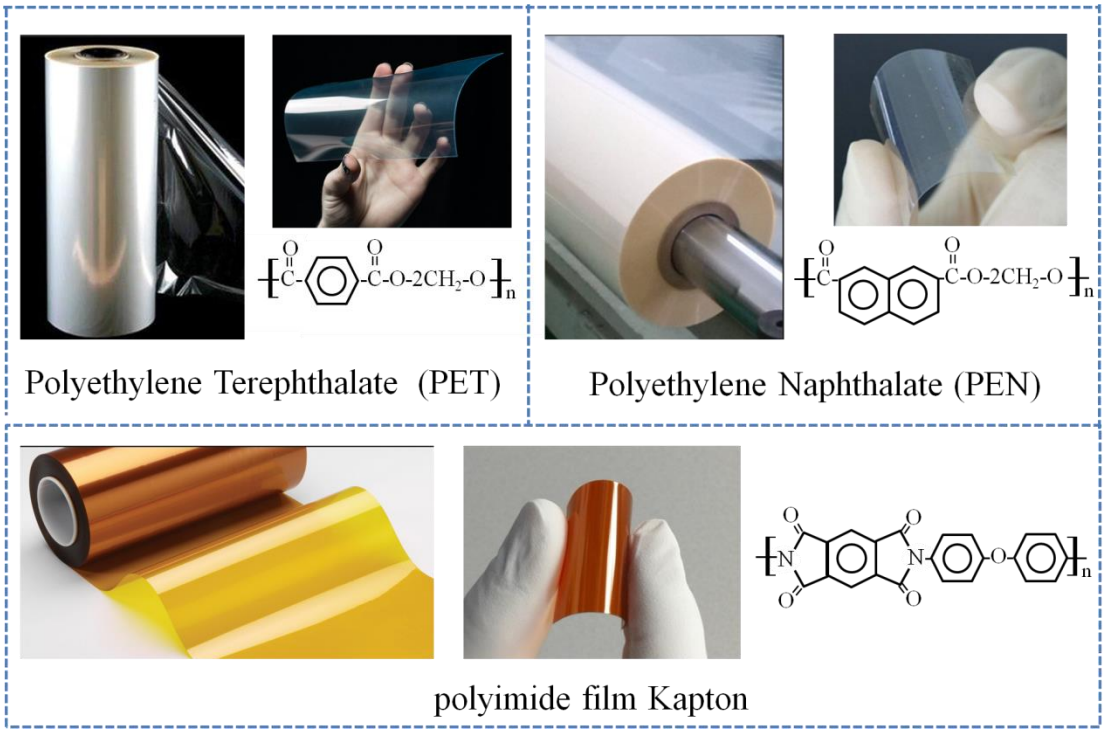


Figure I-7: Image of substrate PET, PEN and Kapton with their monomer formulation

Thermal property is a crucial parameter to be considered by engineers during the fabrication process. One can find that Kapton is more suitable for applications which require higher temperature since it has the highest melting point and the lowest shrinkage. For this reason Kapton was selected for my thesis.

Among the physical properties, surface roughness has an important role on determining the morphology of the patterns that can be printed on the surface. PEN features the lowest roughness, with 0.6 nm, therefore it was also used in this thesis.

The electrical properties of the substrate are important when the substrates are used for electric devices[22][23]. For example, the resistivity needs to be very high for radio frequency application. From an electronics point of view, the three substrates are relatively similar with high resistivity and a dielectric constant varying between 2.9 and 3.5.

Table I-1: Main Properties of PET, PEN and Kapton substrates

	Properties	PET	PEN	Kapton
Thermal	*Shrinkage,at 150 ℃ (%)*	1.5	0.4	0.17
	Melting Temperaure,Tm(℃)	258	269	410
	Glass transition temperature,Tg(℃)	110	155	360
Physical	*Surface roughness(nm)*	0.8	0.6	5
	Youngs Modulus, at 150 ℃ (GPa)	1	3	2
Electrical	*Dielectric Constant*	3.1	2.9	3.5
	Resistivity (Ω·cm)	10^{16}	10^{15}	10^{17}

I.2.4 Ink

One key component of the printing technology is the ink[24-26]. The properties of the ink depend on the specific printing technique. Generally, the printable solution-based ink for piezoelectric nozzles must have properties listed below:

- Surface tension between 28 to 33 dynes/cm, an important parameter to determine its contact angle on a certain substrate.
- Viscosity between 10 to 30 cps, directly affecting waveform as mentioned previously.
- Low evaporation rate after printing, thus solvent with high boiling point is preferable.
- Nano-particles uniformly dispersed in solution without aggregating each other.

In this study, we use a commercial ink, Suntronic U5603, which has 20wt% Silver nanoparticles with ethanol based solution, in addition with ethanediol(10-20wt%) and glycerol(5-10wt%). The datasheet of this product shows a surface tension of 27-31 dynes/cm and viscosity of 10-13 cps at 25 ℃.

Importantly, regardless of the formation method of inks, the sintering process is always necessary to remove the solvent and surfactant layer on surface of nanoparticles.

The metallic nanoparticles dispersed in solvent have large surface curvature, i.e., very high surface energy due to the large surface-to-volume ratio, they tend to aggregate. In further, the direct contact between individual nanoparticles in the aggregation may lead to merging behavior, and subsequently, to a larger cluster. All these bigger particles can be threats to printing stability or even to cause nozzle clotting. Therefore, to have a stable and uniform dispersion in solution, the nanoparticles have to be modified on their surfaces to avoid aggregation.

Figure I-8 illustrates different status of metallic nanoparticles (taking silver as an example here) from dispersing in ink solvent to form densified and conductive bulk layer. With surface modification, a protection shell, or referred as surfactant will be present on each nanoparticles to avoid nanoparticles aggregation[14], as Figure I-8 (a) shows. The solvent evaporation will occur right after inkjet printing, which renders the particles close together, shown in Figure I-8 (b). Nevertheless, the surfactant layer, usually some non-conductive organics, even as thin as few nanometers, is still sufficient to prevent electrons moving from one particle to another [27]. To have direct physical contacts between nanoparticles, typically, the surfactant can be removed by an increase in temperature. In low temperature range, the nanoparticles began to lose their organic shell and partly contact physically, as Figure I-8 (c) depicted. In this phase, due to the reduction of surface energy as driving force for sintering, the necks between particles begin to form. As temperature increased, all the organic materials will be burnt off and necks area will further increase, leaving a more condensed structure as depicted in Figure I-8 (d).

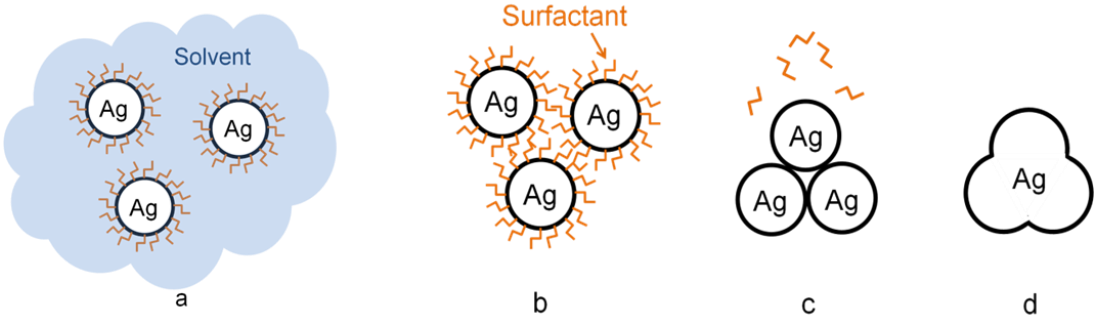


Figure I-8: Simplified schematic of sintering process of silver nanoparticles

In this study, with consideration of commercial ink Suntronic U5603, we performed experiments for the effect of two factors, sintering temperature and sintering time, on the morphologies and electrical resistivity of printed pattern. Relative results will be presented in section I.3.3.

I.3 Parameters optimization of the inkjet printing on flexible substrate

The previous paragraph highlights the general information about printing principle, substrates (especially PEN and Kapton) properties, and the thermal sintering treatment of nanoparticles-based ink. Particularly, we explained the formation process of one droplet from ink cartridge to substrate through nozzles, which is a critical part of inkjet printing technique.

Various electrical components with different structures realized by inkjet printing on flexible substrate have been reported in literature[15]. These studies demonstrate the possibility of realizing microwave circuit by inkjet printing technology. However, improving the quality and the reliability of printed patterns in terms of geometry and resolution remains a major challenge. Briefly speaking, for electrical components fabricated by inkjet printing, such as coplanar wave guide (CPW) transmission line, there are four important criteria which will finally determine the printed device performance: 1) as low as possible the mismatch between printed and designed pattern; 2) well controlled pattern defects (holes, cracks and rough pattern boundary); 3) minimum printable distance between two separated tracks; 4) a sufficiently low resistivity of the pattern.

In details, to meet the four criteria as mentioned in last paragraph, there are several parameters concerning to Dimatix equipment, substrate and ink which are possible to be optimized. In this section, we will give the optimized printing parameters by showing the good results. Although many works has been done in optimization, the details of parameters optimization will not appear in the main text, but be presented in annexes.

I.3.1 Firing voltage

As mentioned previously, waveform is consisted of four segments to have one droplet ejected. The voltage amplitude of second segment, referred as firing voltage, is regarded as a main parameter in waveform. Two aspects of the droplet ejection, volume and velocity of the as ejected droplet, would be effectively controlled by firing voltage. An increased value of firing voltage results in both larger volume and higher velocity of as-ejected droplet. We find that a high firing voltage and thus high jetting velocity destroys the completeness of the droplet shaped on substrate. As Figure I-9 (a) shows, in high firing voltage range (30~40V), the formation of droplets with good shape

becomes difficult. The jetting velocity as a function of firing voltage is plotted in Figure I-9 (b). The droplet jetting velocity can be obtained directly from Dimatix manipulate software. We find that for ink of SunTronic U5603, jetting velocity in range from 4 to 12 m/s (firing voltage from 16 V ~ 25 V) is preferable to obtain droplets with good shape.

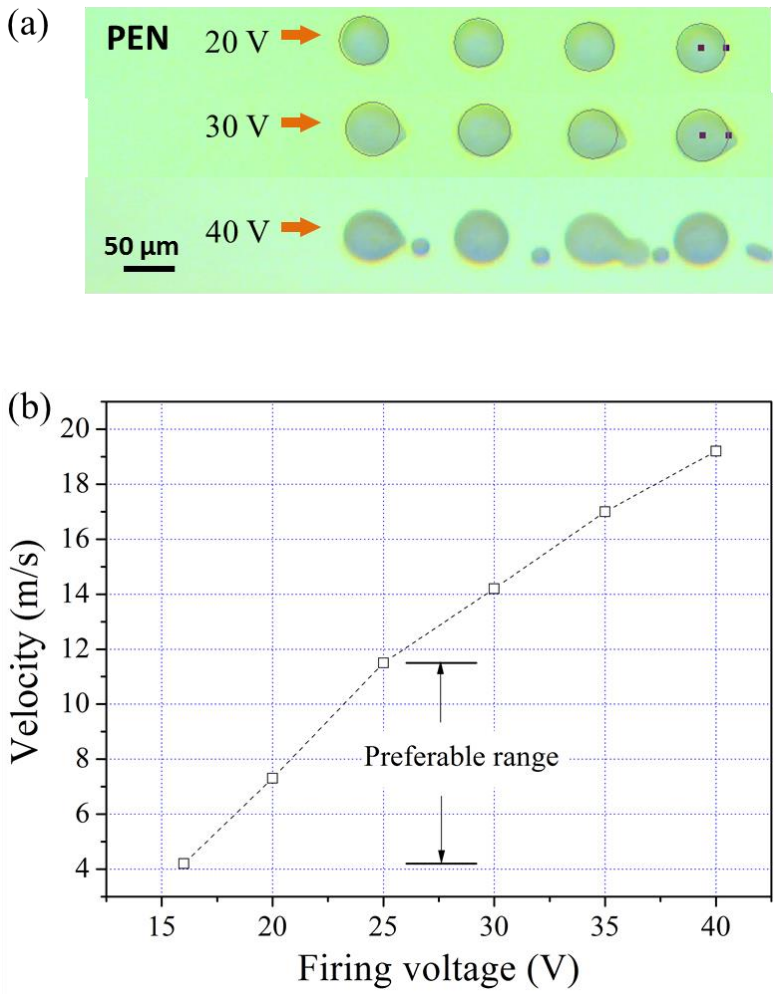


Figure I-9: (a) Optical image of droplets formed on PEN by three different firing voltage (20, 30 and 40 V); (b) jetting velocity as a function of firing voltage

As shown in Figure I-10, with the firing voltage of 16 V, arrays of droplets with intact round shape are formed on substrates of PEN and Kapton. The diameters of the droplets on these two substrates are slightly different: 38 µm for PEN and 47 µm for KAPTON. It indicates the surface tension of PEN and KAPTON should be slightly different.

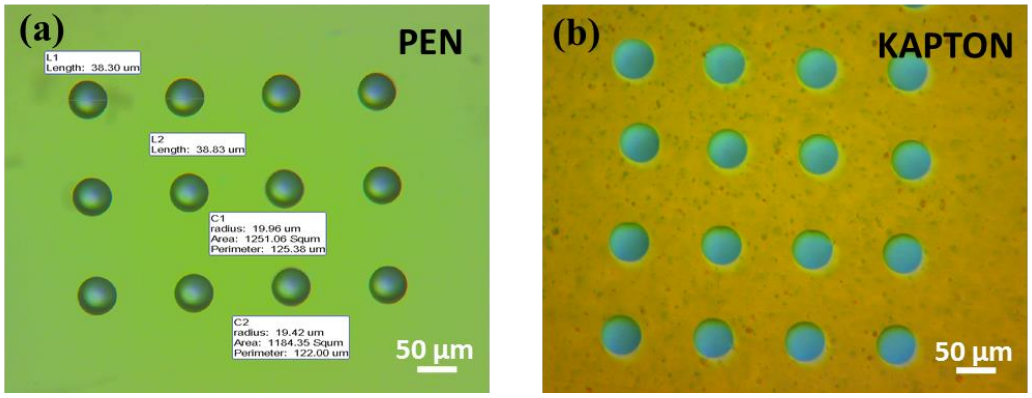


Figure I-10: Droplets formation on substrates of PEN in (a) and KAPTON in (b), both by firing voltage of 16V

I.3.2 Pattern design

In pattern design, a Dimatix software based computer work, we can create and modify printing patterns. There is a very important parameter in terms of smooth pattern control, drop spacing, which gives the centre to centre distance from one droplet of ink to another adjacent in X and Y direction, as what Figure I-11 (a) shows. Figure I-11 (b) shows a part of the real design of a rectangular shaped pattern in Dimatix software.

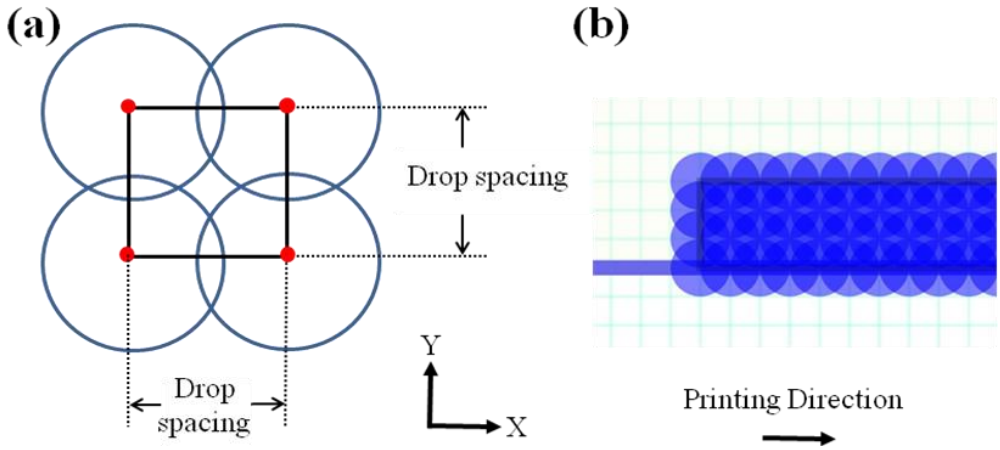


Figure I-11: (a) Schematic diagram of drop spacing and (b) a real design in Dimatix software

The final pattern geometry is strongly determined by drop spacing. The optimization work of drop spacing is provided in Appendix I, in which the pattern geometry depending on different drop spacing values is carefully explored on PEN (we don't show the details of optimization of printing patterns on Kapton, because of the identical process as presented for PEN). Because the droplet diameter on PEN and Kapton are different, the optimized drop spacing values are also different accordingly.

Therefore, we have normalized the drop spacing by dividing the droplet diameter, so that the ratio of drop spacing over droplet diameter can be regarded as a universal reference for pattern geometry control. Table I-2 shows the remarks of pattern geometry obtained from different ratio of drop spacing over droplet diameter. Note that these results are based on many tests as shown in appendix I from both on PEN and Kapton substrates.

Table I-2: Lines smooth control depending on the ratio of drop spacing over droplet diameter

Drop spacing /Droplet Diameter	**Smooth control comment**
< 0.6	Lines will be continuous, but bulging phenomenon and wave-like boundary are often observed
~ 0.7	**Good range to obtain continuous lines with smooth boundary control**
> 0.8	Although the smooth boundary control is good, but the lines are highly risk to be not continuous

Figure I-12(a) shows a line pattern printed on PEN. The jetting voltage used is 20V, and drop spacing of 28 μm is used to keep ratio of drop spacing over droplet diameter around 0.7. Figure I-12(b) shows the thickness of the line, which has been measured by profile meter from point A to B as illustrated in Figure I-12 (a). Note that the scale of the thickness is nanometer and that of the width is micrometer. A standard thermal sintering process is explored prior to thickness measurement so that the ink solvent is removed.

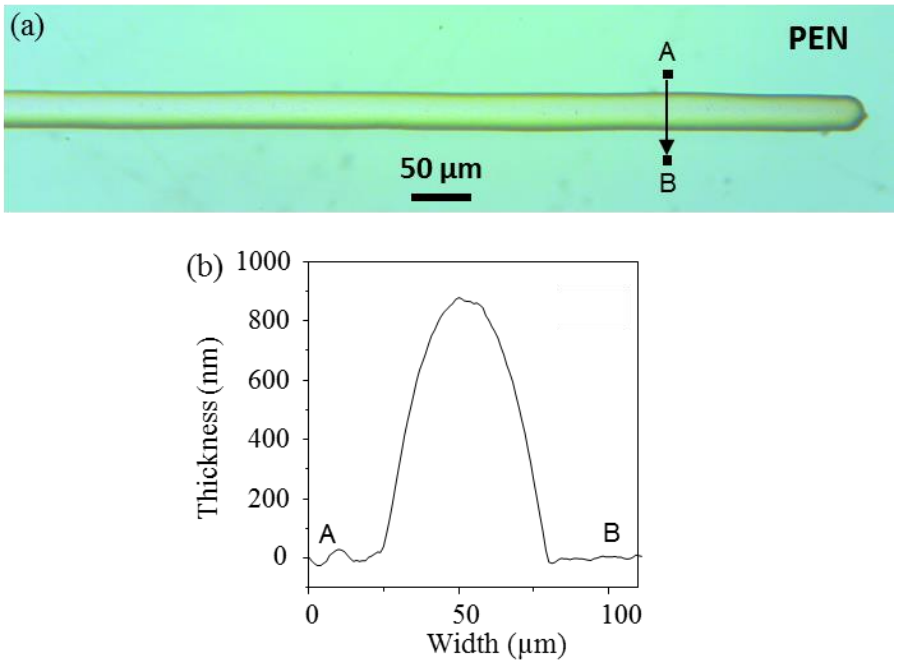


Figure I-12: (a) optical image of a line printed on PEN by 20V jetting voltage; (b) thickness measurement from point A to B as illustrated in (a)

The minimum printable distance between two separated tracks is another challenge for inkjet printing technology. In this work, Dimatix is capable to print two separate patterns either in one time printing (the two patterns belong to one design file) or in two times printing (the two patterns belong to two different design file). The reproducible minimum distance between two patterns of around 17 µm is obtained in this work by one time printing method, as shown in Figure I-13.

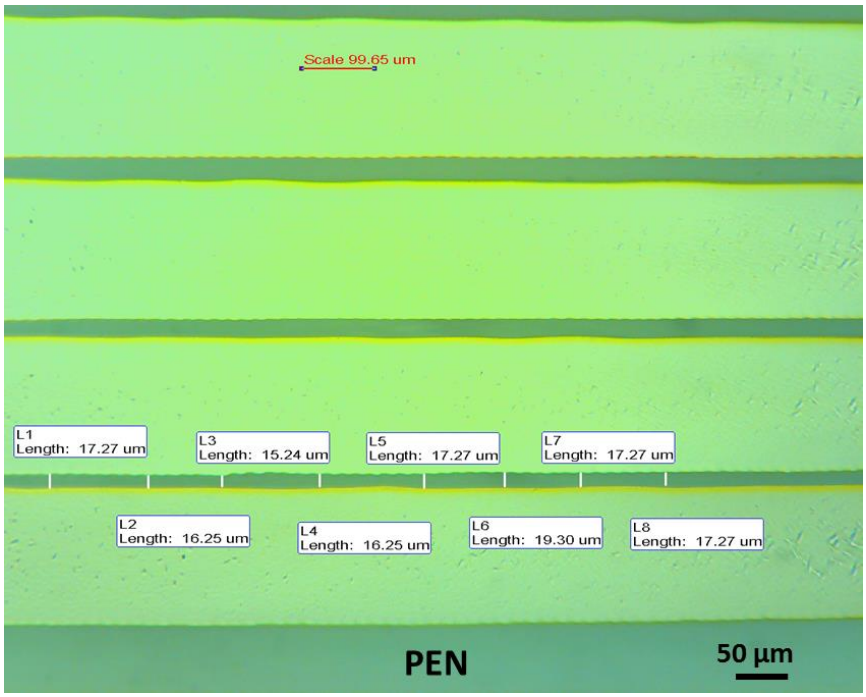


Figure I-13:patterns printed on PEN with a reducing gap, the minimum separation between two patterns of 17 µm is obtained

On substrate of Kapton, with the optimized parameter obtained on PEN, the same printing results are obtained. To this end, we have discussed about equipment-dependent parameters: firing voltage and drop spacing. Next section will focus on the properties of the ink and also its interaction with substrate.

I.3.3 Wettability

Wettability is normally used to describe how a liquid maintain its contact with a solid substrate which results from a balance between adhesive and cohesive forces. This balance, in Yong's equation: $\gamma_{SL} + \gamma_{LG}\cos\theta = \gamma_{SG}$, equals the balance of surface tension between the three phases: solid, liquid and gas[17]. From Figure I-14 we see a contact angle θ which provides us important information of wettability as it is determined by the balance of those three phases surface tension.

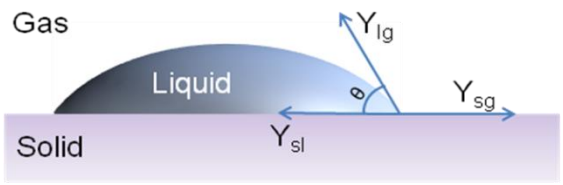


Figure I-14: Schematic for Yong's equation and contact angle

The surface tension of a substrate is determined by either the material or temperature of the substrate [28]. Taking PEN as an example, to verify the wettability

evolution of Suntronic U5603 ink on PEN substrate with different surface tension, we separately deposit single droplets on different PEN substrates which are already baked up to 25 ℃, 70 ℃, 110 ℃ and 150 ℃, respectively. Figure I-15 shows the contact angle measurements of these single droplets. Supposing surface tension of ink is a constant value, deduced from Yong's equation, we believe that the variation of contact angle from 12.3 º to 28.1 º are resulted from different surface tension of PEN caused by different substrate temperatures. It is concluded that ink of Suntronic U5603 shows the best wettability on PEN substrate at room temperature(around 25 ℃). In further, the effect of wettability on pattern formation is studied. Figure I-16 shows a line pattern printed on PEN substrate with 25 ℃ in (a) and with 70 ℃ in (b). We observe that the printed line pattern on PEN with temperature of 25 ℃ exhibits good boundary control, and a uniform line without holes or bulging is obtained. However, line pattern printed on PEN with temperature of 70 ℃ shows a quite worse boundary control, and non-uniform line was observed due to the high contact angle.

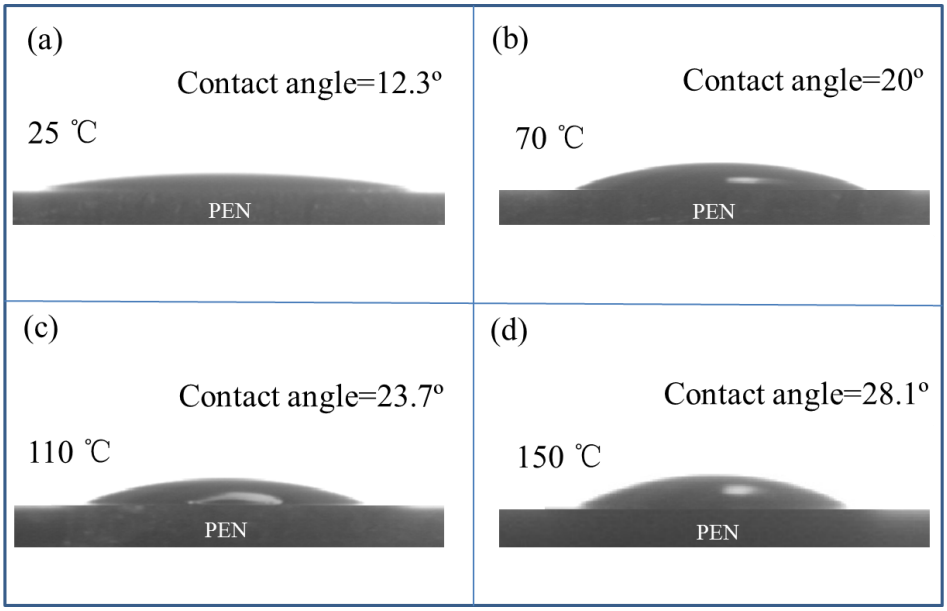


Figure I-15: contact angle variation on substrate of PEN with its different temperature

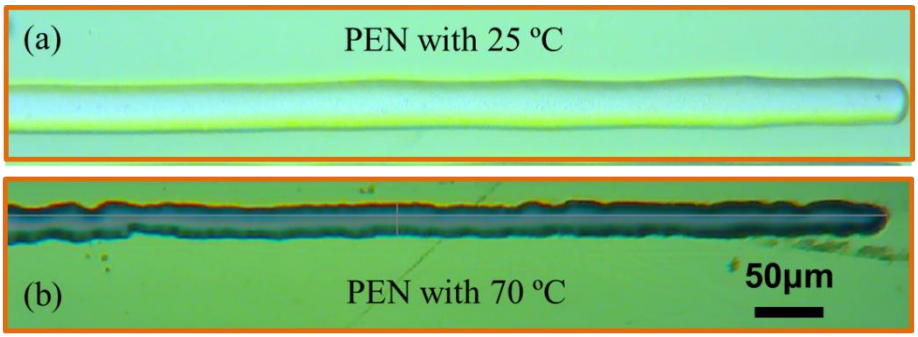


Figure I-16: One line printed on PEN with substrate temperature of 25 ℃, in (a) where a line with good geometry has been obtained; and of 70 ℃ in (b), where a poor shaped line has been formed

I.3.4 Ink of Suntronic U5603, sintering and resistivity

I.3.4.1 Realization of Van der Pauw structures for resistivity measurement

Several sintering methods have been reported for inkjet printing technology, such as microwave, laser and thermal sintering[29-36]. The conventional thermal sintering method has been used in this work. Van der Pauw method has been used for resistivity measurement. Van der Pauw patterns has been printed on silicon wafer and sintered at different temperature. HL5500PC with four tips platform was used for measurement. Below, details of Van der Pauw fabrication by inkjet printing and resistivity extraction will be provided. Based on that, the effect of sintering temperature and time on resistivity will be explored.

Van der Pauw method is widely applied for resistivity and mobility measurement of two-dimensional materials. More details of measurement principle will be provided in Chapter2. The goodness of this technology lies in a highly accurate measurement which thus requires a symmetrical pattern with contacts located on the circumference. Figure I-17 (a) shows the Van der Pauw pattern designed mask in Dimatix software. The pattern consists of one square shape (width of w), the measurement area, with four contacts on each of its corner where to place the probes. Totally, squares with three different dimensions (w=1, 1.25 and 1.5 mm) have been designed and printed. As Figure I-17 (b) shows, no holes, pattern defects, or inhomogeneous parts could be found in the printed Van der Pauw pattern (w=1 mm), which satisfies the Van der Pauw conditions.

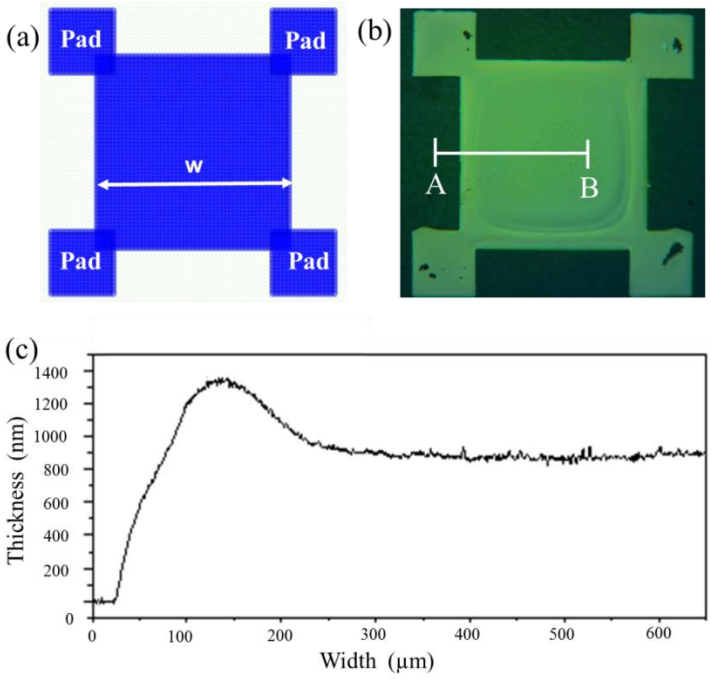


Figure I-17: (a) Van der Pauw pattern designed in Dimatix; (b) optical image of the Van der Pauw pattern after printing; (c) measured thickness of Van der Pauw pattern followed the trace of AB as illustrated in (b)

Figure I-17 (c) shows the Van der Pauw pattern thickness measured by profile meter. We observe a relative flat surface except for a bit thicker edge area caused by coffee ring effect. Coffee ring effect describes the phenomenon that during the evaporation of a droplet, the liquid evaporates faster from interior to the edge. In this study, after 30 min @150℃ sintering treatment, we find about 1300 nm thickness for edge and 900 nm for the rest area.

In such case, the average thickness for the whole area would be calculated for resistivity measurement. For statistic, five patterns for each Van der Pauw dimension (x=1, 1.25 and 1.5 mm) have been printed. And with sintering conditions of 30 min @150℃, Figure I-18 shows the resistivity obtained by Van der Pauw measurement for different pattern dimension.

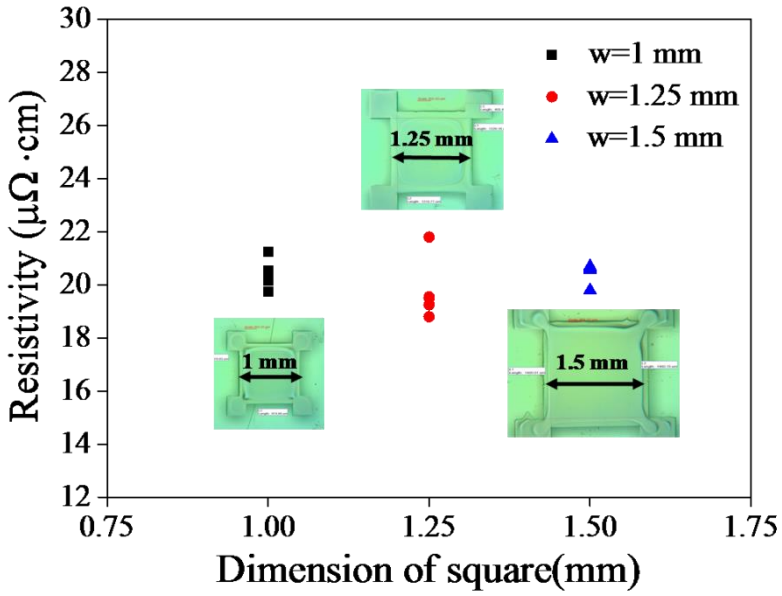


Figure I-18: Resistivity obtained from Van der Pauw pattern with pattern length of 1mm, 1.25 mm and 1.5 mm

I.3.4.2 Effect of sintering temperature on resistivity

Several Van der Pauw patterns with identical dimensions (side length of 1.5mm) were inkjet printed on five Si/SiO_2 substrates, respectively. Under ambient condition, five samples were separately heated up to 100℃, 125℃, 150℃, 175℃ and 200℃ on hot plate with heating rate of 15℃/min from room temperature. After having reached to target temperature, 30 min of duration with the target temperature and then a cooling down at 20℃/min were followed. Sheet resistance ($R_{\square}$) was directly measured by using Van der Pauw method, and resistivity(ρ) was calculated by taking into account the pattern thickness(t) as given by formula ($\rho = R_{\square}\, t$).

Figure I-19 shows the electrical resistivity variations of Suntronic U5603 as a function of sintering temperature. Scanning electron microscopy (SEM) images in Figure I-20 shows the morphology and particle packing within the printed patterns after different sintering temperature. Figure I-21 shows the silver nano-particle size distribution obtained by SEM image analysis.

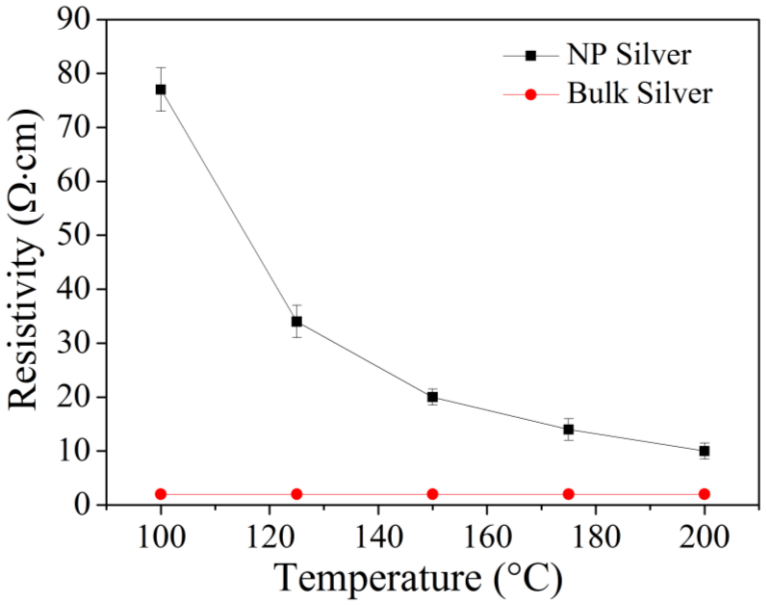


Figure I-19: Dependence of patterns resistivity on different sintering temperatures

As shown in Figure I-19, in the beginning with sintering temperature of 100℃, the resistivity is still relatively high. Probably in this early stage the organic protective shell are still not completely removed and the neck formation is not effectively started. Confirmed by Figure I-20 and particles size distribution analysis in Figure I-21, the silver nanoparticles with a typical diameter 20 to 50 nm can still be distinguished individually.

As the sintering temperature increased up to 150℃, more organic materials would be removed and the coalescence of Ag nanoparticles begin to occur due to a tendency to minimize the overall surface area of particles. Confirmed by SEM image of Figure I-20, many of the particles are connected to each other while some still keep their shapes and are not fully connected yet. The resistivity drastically drops from 76 μΩ cm to 34 μΩ cm, according to 100℃ and 150℃ respectively. This improvement of resistivity indicates that conduction path between the particle is established by inter particle neck formation. Good agreement can also be found in Figure I-21 which shows an increased diameter of 40-70nm for Ag nanoparticles after 150℃ sintering.

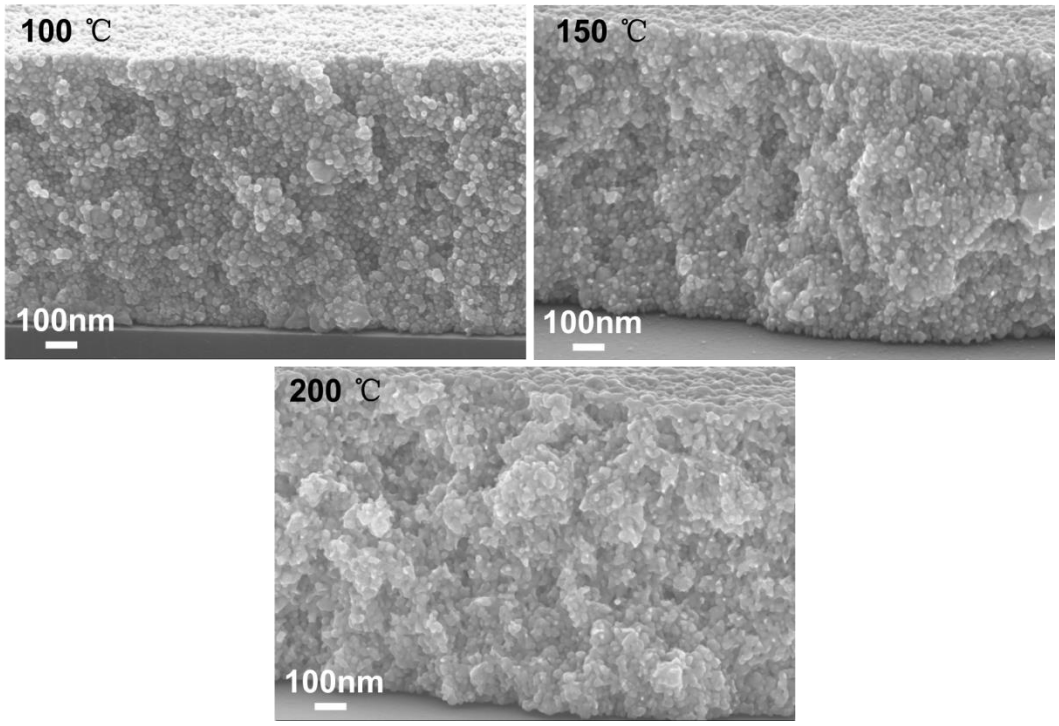


Figure I-20: SEM images of patterns cross section sintered by 100℃, 150℃ and 200℃ for 30 min

Further increasing the sintering temperature up to 200℃ reveals an even lower resistivity of 11.6 μΩ cm, which is about 8 times higher than the theoretical value of bulk silver. It is also noticed that the resistivity decrease rate from 150℃ to 200℃ is much smaller than that from 100℃ to 150℃. Probably because in this stage, the organic materials have been burned off already, and only the neck formation between nanoparticles contributes the resistivity decrease. A clear particle shape change from discrete-and spherical particles to continuous-and sintered particles could be observed in Figure I-20, particles begin to merge into larger agglomerates and these increased three-dimension continuous network structures explain the further drop of resistivity. The typical nanoparticles diameter distributes in the range of 40 to 120 nm after 200℃ sintering are shown in Figure I-21.

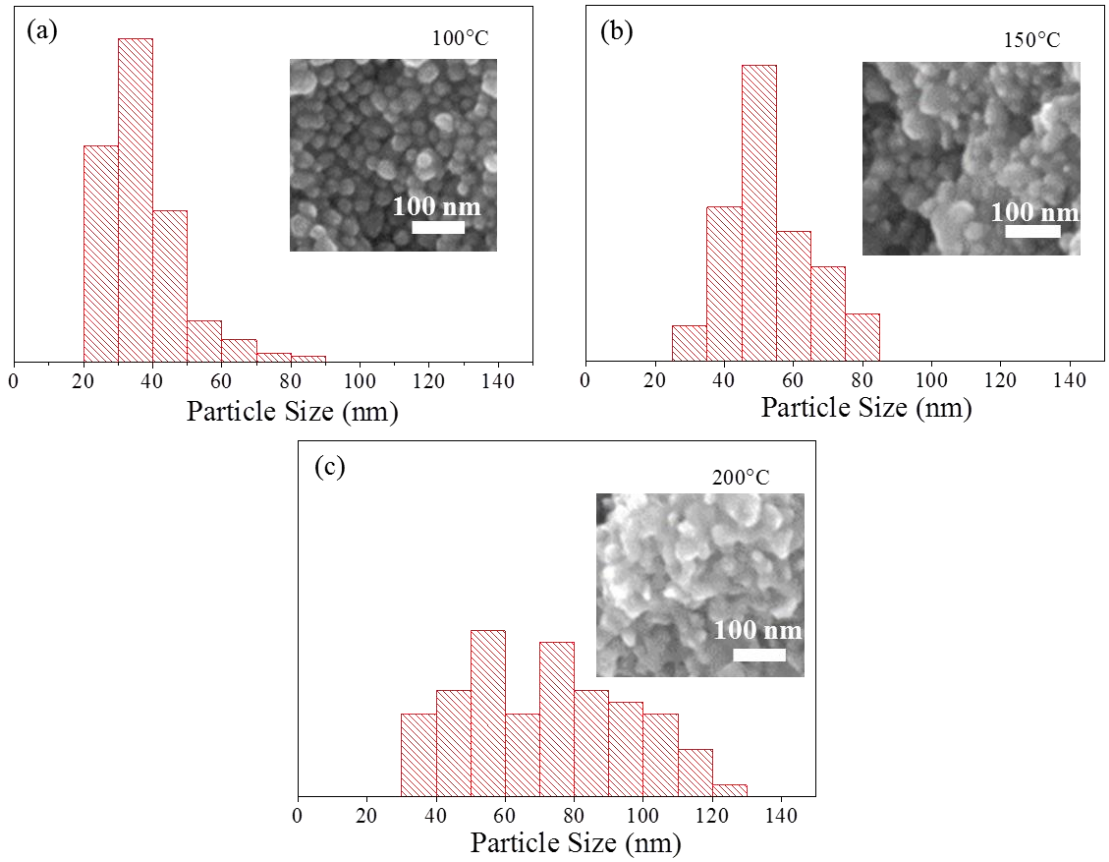


Figure I-21: Particle size distributions for patterns with different sintering temperatures,100 ℃ in (a), 150 ℃ in (b) and 200 ℃ in (c),which are obtained by SEM image analysis (inset SEM image shows the typical nanoparticle morphology according to different sintering temperature)

I.3.4.3 Effect of sintering time on resistivity

Similar to the effect of sintering temperature discussed in above paragraph, the effect of sintering time on ink of Suntronic U5603 was studied in terms of resistivity. Several Van der Pauw patterns with identical dimensions (side length of 1.5mm) were inkjet printed on six Si/SiO_2 substrates, respectively. Under ambient condition, six samples were all heated up to 200 ℃ on the hot plate with heating rate of 30 ℃/min from room temperature but separately remains for 10, 20, 30, 40, 50 and 60 min. Then a cooling down at the rate of 40 ℃/min was followed. The resistivity as a function of sintering time (sintering temperature of 200 ℃) is shown in Figure I-22.

After the pattern was annealed for 10 min, the resistivity significantly drops to a value of 19 ± 3 μΩ cm. It means probably all the chemical part in the ink has been burned off in the first 10min. As the sintering time increases to 20 min, the resistivity reaches to 12 ± 1 μΩ cm. However, after sintering time of 30min, the resistivity value remains quite stable. It indicates that after 30 min sintering the neck formation between particles should be almost finished and we can conclude that 30 min is the effective

sintering time.

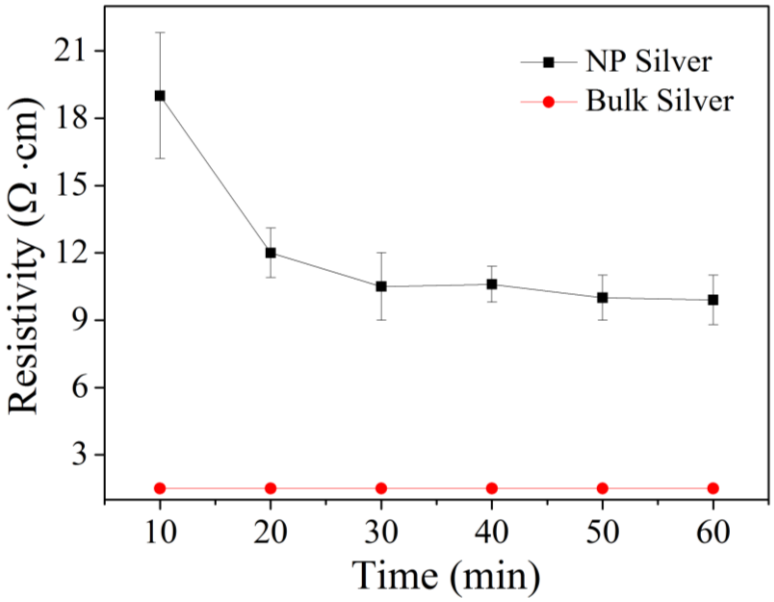


Figure I-22:Resistivity of patterns as a function of the sintering time with a fixed sintering temperature of 200℃

I.4 Realization of printed microwave devices

I.4.1 Coplanar wave guide (CPW) transmission line

CPW is a type of electrical transmission line which can be applied to convey high frequency signals with minimum reflections and power loss.[37] It consists of three metal strips placed on the same side of a dielectric substrate. Figure I-23 shows the schematic of a CPW line. The central line with width *W*, conveys microwave signals while the two other metal lines separated from the central line on each side with a small gap of *S* are ground plane, or return conductor. Both central line and ground plane have the identical thickness, *t*, and length, *L*, approached by a simultaneous fabrication.

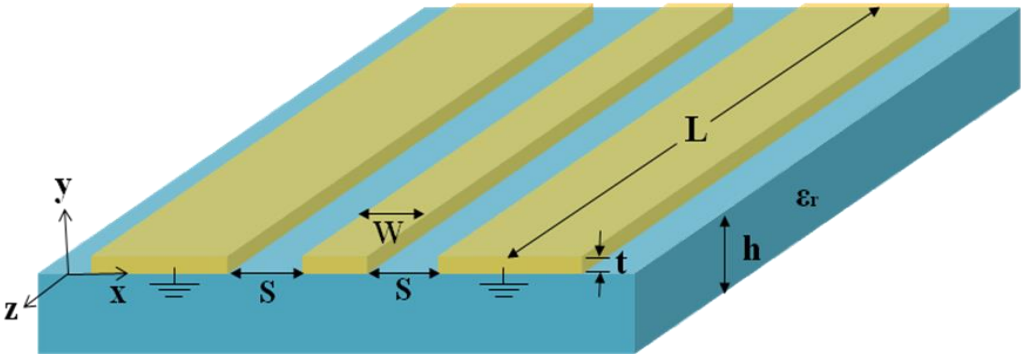


Figure I-23: Three-dimensional schematic of CPW transmission line with geometric parameters

I.4.1.1 Fabrication process of inkjet printing

In this study, CPW transmission line were both inkjet printed on substrate of PEN and KAPTON. in previous section, we find that the diameters of the droplets on these two substrates are different: 38 µm for PEN and 45 µm for KAPTON. It indicates the surface tension of PEN and KAPTON should be slightly different from each other. Therefore, accordingly the printing parameters applied on PEN would be distinguished to that on KAPTON. Table I-3 shows the optimized printing parameters for both these two substrates.

Table I-3: Printing parameters used for printing CPW transmission lines on both PEN and KAPTON substrates

Substrate	Firing voltage (V)	Drop space (μm)	Jetting frequency (KHz)	Substrate temperature (℃)	Sintering treatment (min & ℃)	Resistivity (μΩ·cm)
PEN	16	27	3	25	30min @150 ℃	~20
KAPTON	16	30	5	25	30min @200 ℃	~11

CPW transmission line with six different geometry dimensions have been designed in Dimatix software in terms of central line width *W*, gap *S* to the ground plane, and length *L*. Note that the length of Pad are not taken into account when we design and measure the length *L*. In these six different geometric structures, by using the optimized printing parameters, three were realized on PEN (P_{N1}, P_{N2} and P_{N3}) and another three were realized on KAPTON (K_{N1}, K_{N2} and K_{N3}). Figure I-24 (a) shows the design in Dimatix software with different value of *W* and *S*, and Figure I-24 (b) and (c) show the optical images of these lines obtained on PEN and Kapton.

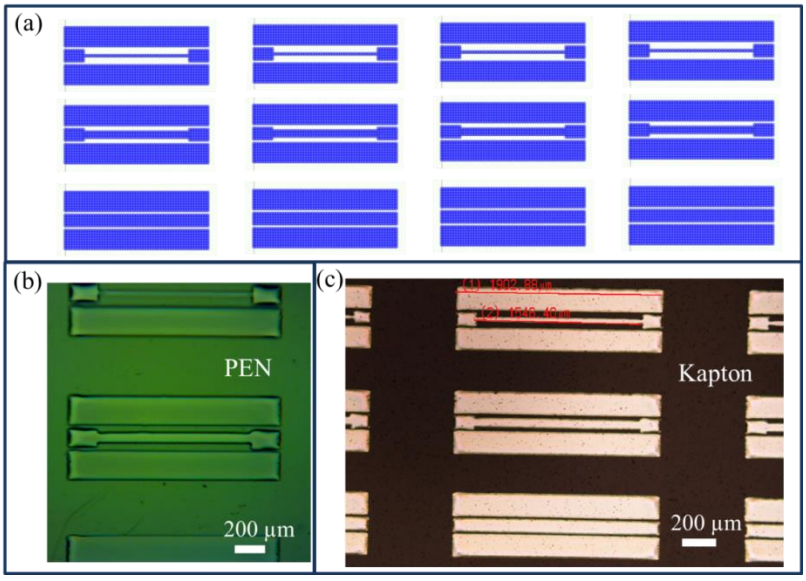


Figure I-24: CPW structures in (a) mask design; (b) obtained on PEN; and (c) obtained on Kapton

(1) CPW on PEN

Figure I-25 shows the patterns of PN1, PN2 and PN3 obtained on PEN. From zoomed-in images, we can see that the minimum value of 18 μm for S has been achieved thanks to the optimized printing parameters. In further, we don't find any

defects such as holes or cracks. The as printed patterns are quite homogeneous and continuous, and a very good boundary control has been obtained. Table I-4 shows the printing results, which include the information of dimensions and the printing accuracy by comparing the structure dimensions of both designed and measured. Note that the dimensions of *W*, *S* and *L* have been illustrated in Figure I-23.

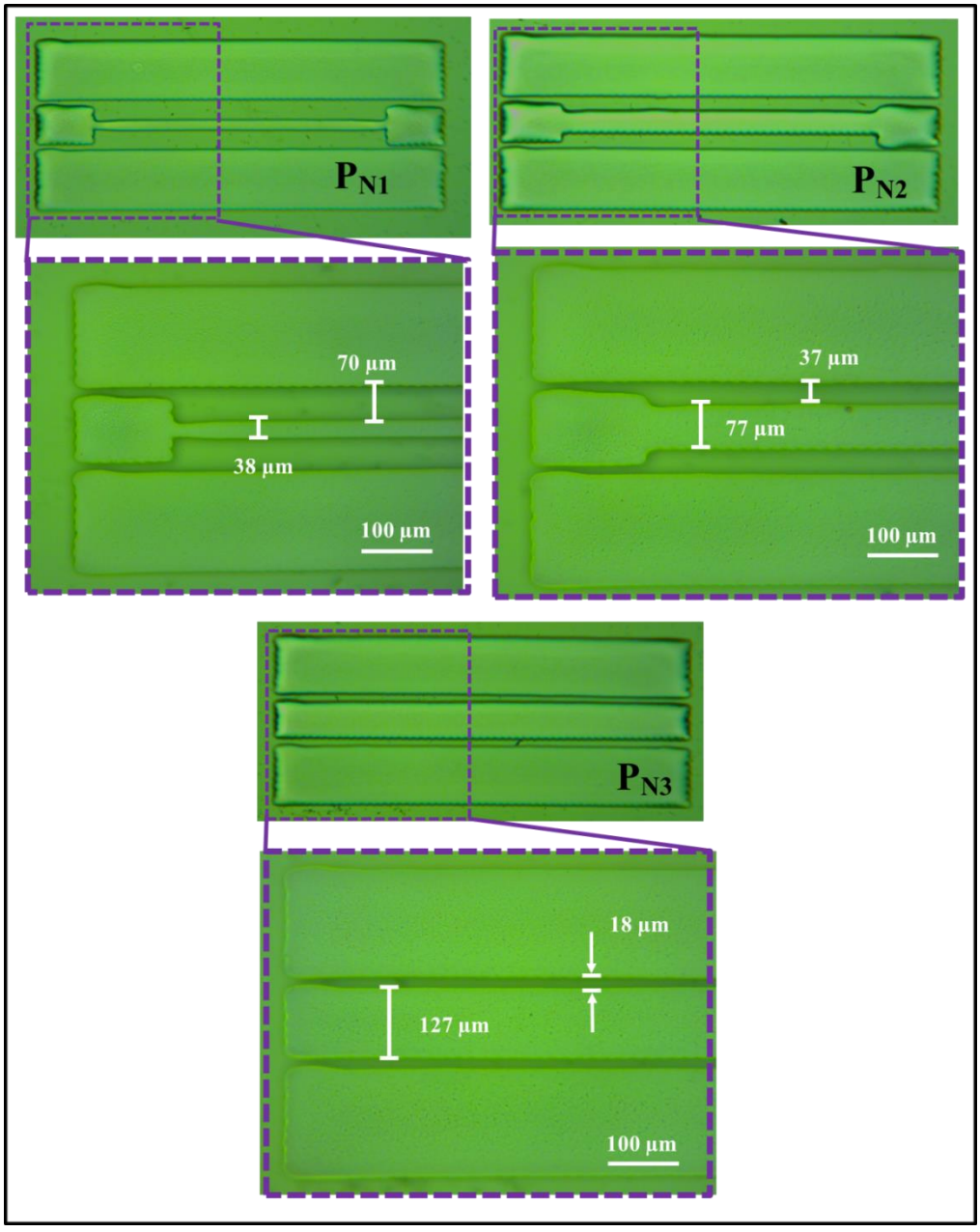


Figure I-25: Optical images of PN1, PN2 and PN3 CPW lines on PEN, with zoomed-in images where the values of W and S are marked.

(2) CPW on Kapton

Figure I-26 shows the patterns of KN1, KN2 and KN3 obtained on Kapton. From zoomed-in images, we can see that the minimum value of 20 µm for S has been

achieved. The printed structures with good quality (patterns are homogeneous and continuous) are also obtained. Table I-4 shows the printing results, which includes the information of dimensions and the printing accuracy by comparing the structure dimensions of both designed and measured.

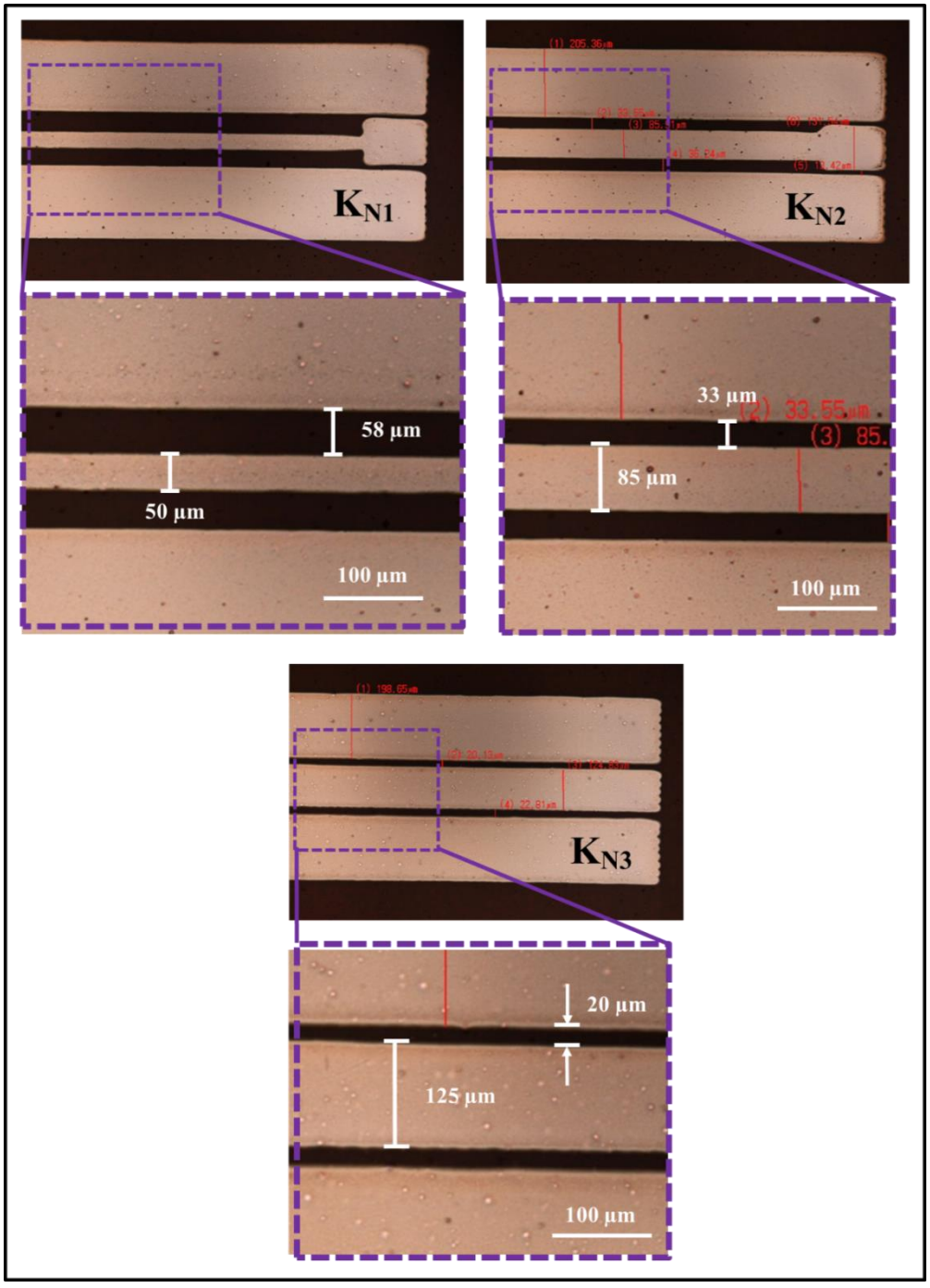


Figure I-26: Optical images of KN1, KN2 and KN3 CPW lines on Kapton, with zoomed-in images where the values of W and S are marked

Table I-4:Summary of CPW transmission lines printing results on both PEN and KAPTON substrates

Substrate	**PEN**			**KAPTON**		
Samples	**P_{N1}**	**P_{N3}**	**P_{N5}**	**K_{N1}**	**K_{N3}**	**K_{N5}**
W_d, Desgined (µm)	40	92	146	50	105	135
W_m, Measured (µm)	38	77	127	45	85	124
Accuracy	95%	84%	87%	90%	81%	92%
S_d, Desgined (µm)	70	43	16	65	46	15
S_m, Measured (µm)	70	37	18	60	33	20
Accuracy	99%	86%	83%	93%	72%	67%
L_d, Desgined (mm)	1000	1000	1000	1020	1020	1020
L_m, Measured (mm)	983	978	980	1029	1033	1025
Accuracy	98%	98%	98%	99%	99%	99%

Accuracy: (1- |measured value – designed value| / designed value) x 100 (%)

I.4.1.2 RF Characterization of CPW transmission lines printed on both PEN and KAPTON when substrate is flat

In this work, for RF measurement of CPW transmission line fabricated by inkjet printing, what we want to know are the characteristic impedance *Zc* and attenuation constant α, which can be both extracted from S-parameters measurement, appendix II gives more details. The measurement is finished by another PhD student Moez, and the relative explanation will be given in his thesis. The measurements have been carried out using an HP8510C precision network (10MHz-40GHz) analyser (PNA) connected to the Cascade ground-signal-ground probes. The LRRM calibration technique was performed to shift the reference plan up to the probe tips by using an impedance-standard-substrate (ISS) from the probes manufacturer. Afterward, the

corresponding S-parameters of CPW transmission lines on both PEN and KAPTON were measured from 0.025 to 40 GHz. From the as measured S-parameters, the *Zc* and α were extracted. Below, for the CPW transmission lines on both PEN and KAPTON, the characteristic impedance and attenuation constants will be presented.

(1) Zc and α of CPW on PEN

Figure I-27 shows the characteristic impedances versus frequency for P_{N1}, P_{N2} and P_{N3}. In frequency range up to Giga hertz, the characteristic impedances can be expressed as $z_c = \sqrt{\frac{L}{C}}$, because the imaginary part becomes prominent and the real part can be negligible. Both *C* and *L* are highly dependent of the geometry of CPW transmission lines, especially the ratio of gap-to-central line width (*S/W*). This explains that for samples of P_{N1}, P_{N2} and P_{N3} with different *S/W* ratio, different *Zc* were obtained, as shown in Figure I-27. Figure I-27 also shows the attenuation constant versus frequency for P_{N1}, P_{N2} and P_{N3}. Up to 40 GHz, the attenuation is found to be about 1.3 dB/mm, 0.8 dB/mm and 0.9 dB/mm for P_{N1}, P_{N2} and P_{N3} respectively.

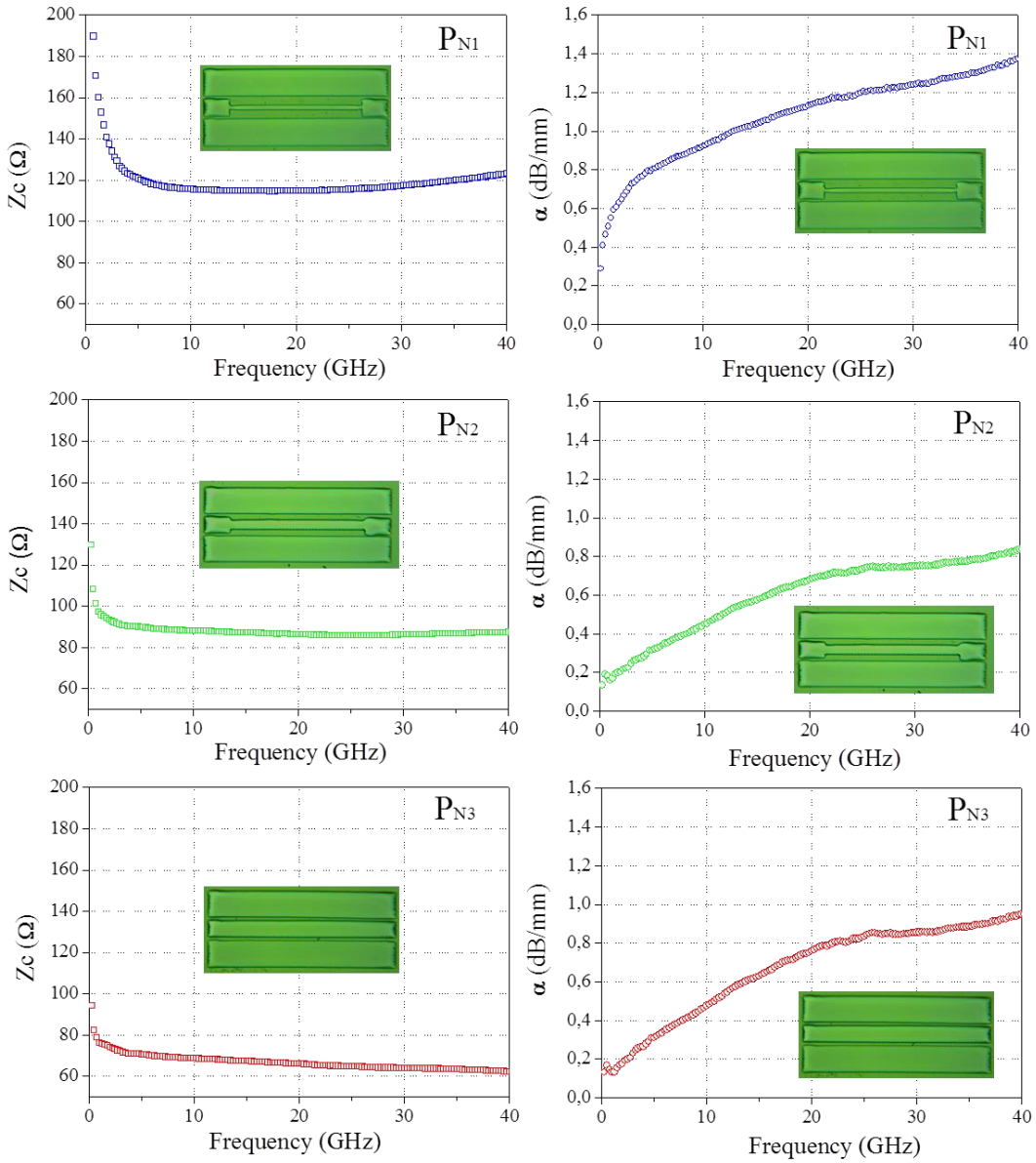


Figure I-27: Characteristic impedance Zc and attenuation constant α of samples PN1,PN2 and PN3 on PEN substrate

(2) Zc and α of CPW on KAPTON

Similar to the discussion on PEN, Figure I-28 shows the characteristic impedances versus frequency for K_{N1}, K_{N2} and K_{N3}.

Figure I-28 also shows the attenuation constant versus frequency for K_{N1}, K_{N2} and K_{N3}. Up to 40 GHz, the attenuation is found to be about 0.7 dB/mm, 0.5 dB/mm and 0.7 dB/mm for K_{N1}, K_{N2} and K_{N3} respectively. We believe that the less loss obtained from CPW lines on KAPTON comparing to that on PEN comes from the lower resistivity of CPW lines on KAPTON which thanks to the higher sintering temperature (see Table I-3).

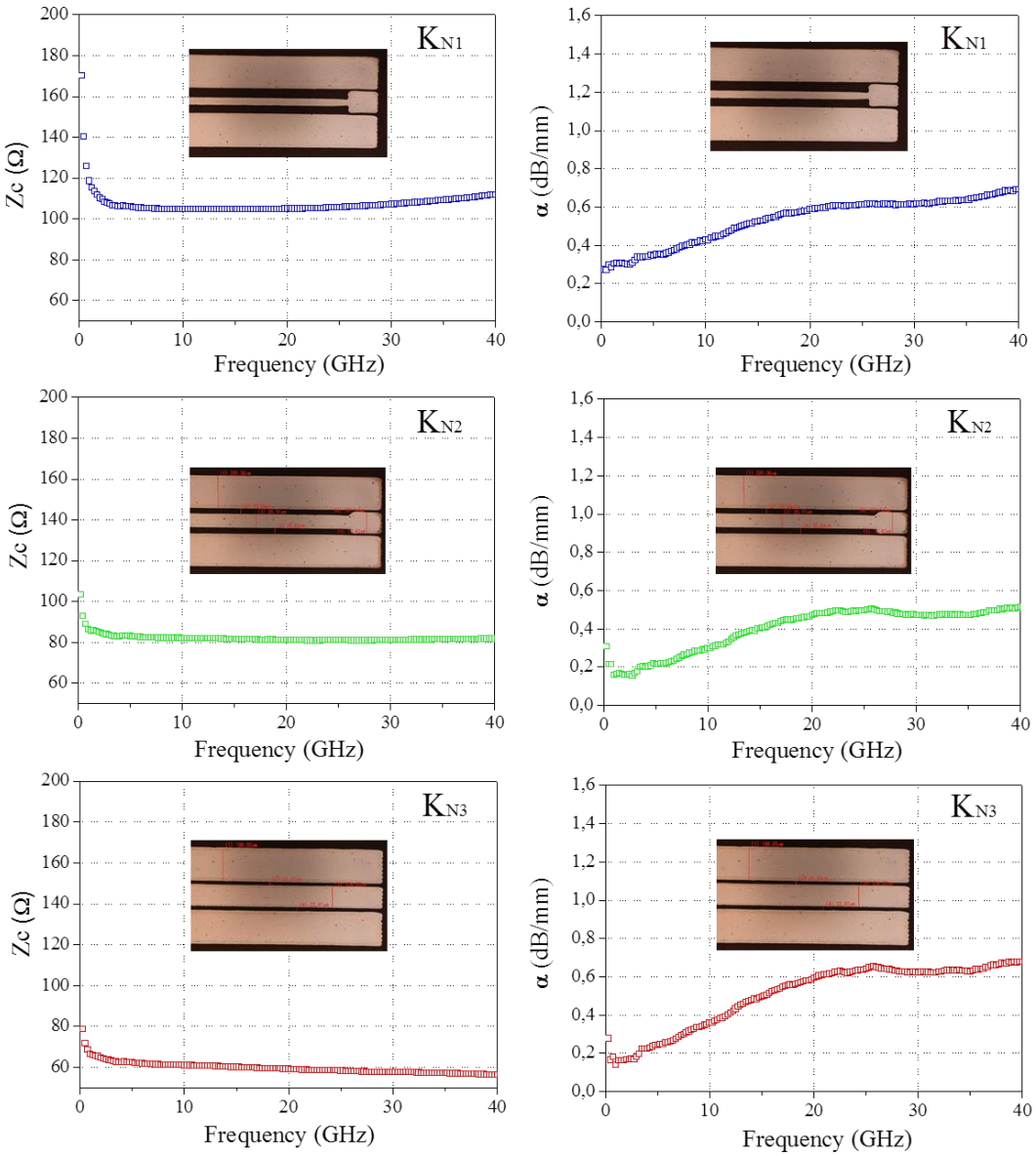


Figure I-28: Characteristic impedance ZC and attenuation constant α of samples KN1, KN2 and KN3 on KAPTON substrate

I.4.1.3 Effect of substrate strain on attenuation constant

(1) Strain calculation of bended substrate

Since the flexible electronics is one major application for inkjet printing technology, the relative bending measurement needs to be developed. To analyse the mechanism of the bending layer in our substrate, the model from Chiang [38] is used here. For a simple case that the flexible substrate is composed by only single material, Figure I-29 (a) shows the substrate cross section with thickness of 2t. Before bending, in each layer of the substrate the lengths are identical: CD=AB=EF. Let's define the layer CD, AB and EF are in the top, middle and bottom positions of the substrate

respectively. When the flexible substrate is bended on a supporter with radius of R, as shown in Figure I-29 (b), layer AB will keep its original length L and all the layers above AB will be stretched while those below it will be compressed. Because of this, the layer of AB is named as neutral layer (NL). The strain value of CD layer is defined by:

$$\varepsilon = \frac{\Delta l}{L}, \qquad \text{(I-1)}$$

where L is the original length and ΔL is the change of length after bending. In the case illustrated in Figure I-29, the strain of CD layer becomes:

$$\varepsilon = \frac{C'D' - CD}{AB} = \frac{\theta(R+2t)}{\theta(R+t)} - 1 = \frac{t}{R+t}, \quad \text{(I-2)}$$

In most cases, $R \gg t$, so the strain can be estimated as $\varepsilon \approx \frac{t}{R}$. From this equation, we can conclude that thicker substrate thickness t or smaller bending radius R can both yield higher value of strain on the bending surface.

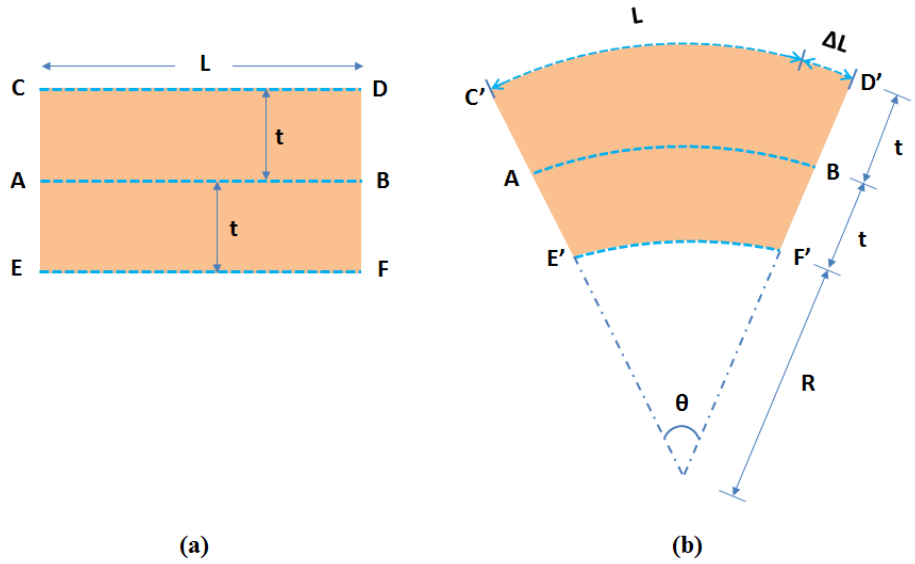


Figure I-29: Illustration of one single-material film cross section of (a) before bending and (b) after bending on supporter with radius R

(2) Evolution of attenuation constant with different substrate strain

As an important nature of flexible electronics, microwave measurement based on KAPTON substrate being bended on supports with radius curvature of 25 mm and 15 mm were carried out. The strain calculation using the method discussed above gives strain value of 0.5% and 0.3% for 15 mm and 25 mm radius supports. Figure I-30 (a) shows the flat and bended measurement. All the measurement results discussed before were based on this flat measure. After, the substrate was fixed onto bended support. To guaranty the measurement is adapted to this bending system, the substrate was bended

along the Z direction of a CPW line (Figure I-23). In this way, the centre and ground must be in the same plane for putting the RF tips. Figure I-30 (b) shows the measured attenuation constant versus frequency corresponding to strain of 0, 0.3 % and 0.5% from sample KN3. One can see that almost negligible difference could be found when the CPW line was bended with strain of 0.3 % and 0.5%. It indicates that the inkjet printed CPW lines possess very stable performance after bending, so that the CPW lines could be fully utilized without degrading the performance.

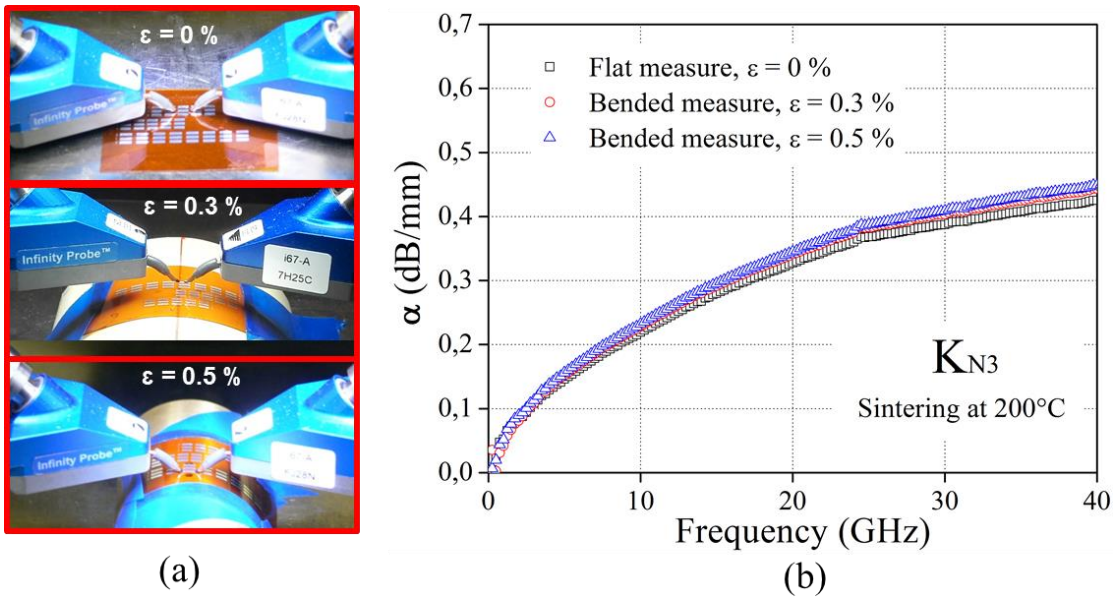


Figure I-30: Illustration of Kapton substrate under different strain with RF probes in (a) and evolution of the attenuation constant versus frequency based on different strain in (b)

I.4.1.4 Effect of sintering temperature on attenuation constant

Because KAPTON has excellent thermal stability, we also studied the effect of sintering temperature on attenuation in the range of more than 200℃. Three K_{N3} CPW lines were inkjet printed on KAPTON with the same printing parameters discussed above, so that the same dimension could be obtained. Afterward, these three lines were sintered at 200℃, 250℃ and 300℃ for 30 min, respectively. Figure I-31 shows the evolution of the attenuation constant versus frequency for these three K_{N5} lines. Losses smaller than 0.3 dB/mm at 40 GHz is obtained after sintering treatment of 300℃, and this improvement is believed to be the result of a higher conductivity.

It is worth to mention that 0.2 dB/mm at 40 GHz achieves the same order of attenuation from CPW lines fabricated by photolithography with the same dimension but with a 350 nm thick gold deposited by metal evaporation.

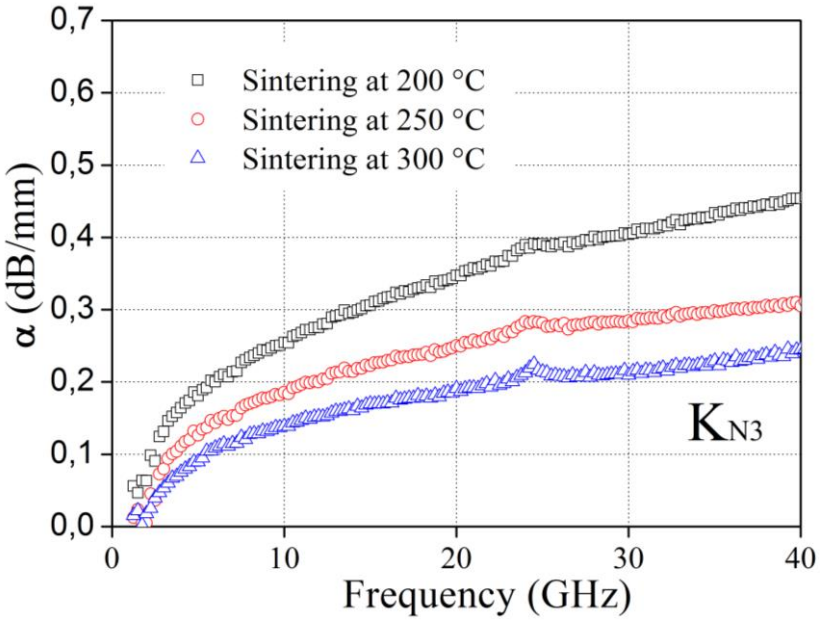


Figure I-31: Comparison of attenuation constant for sample KN3 sintered by temperature of 200℃, 250℃ and 300℃, respectively

I.4.2 Coplanar square monopole antenna

I.4.2.1 Fabrication process of inkjet printing on PEN substate

Several circuits and antennas have been realized on flexible substrates with inkjet technology for applications at frequency below 10 GHz, such as RFID tags or sensor systems[39-41], however no antenna fabricated by inkjet printing technology on flexible substrate with characterization up to 60 GHz has been fully presented.

This work has been done with a collaboration of a group in University of Nice (Leat Group). We are in charge of structures fabrication. Note that the dimensions of the antenna are required for good precision because the performance is highly dimension-dependent.

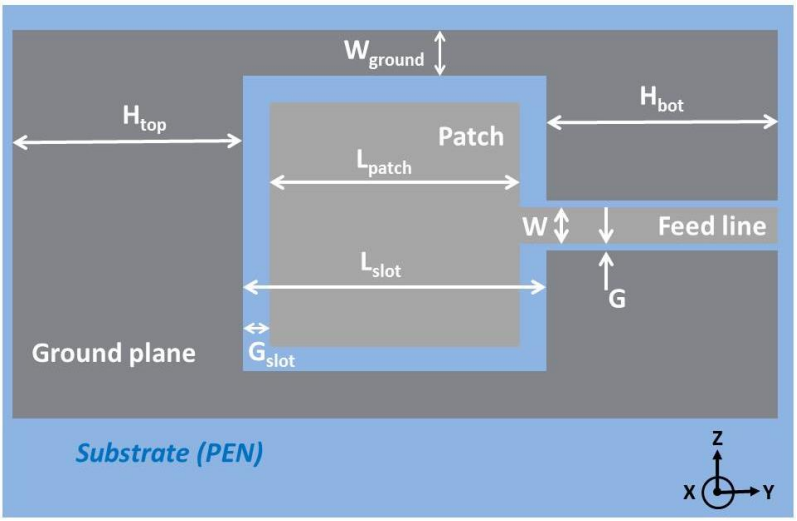


Figure I-32: Top view of the layout of the antenna

To obtain antenna patterns with accurate dimensions and also to have good boundary control, we have made many tests with different printing parameters until the best optimized parameters have been achieved (Table I-5). Particularly, this antenna design has several different components, such as *patch*, *feed line* and *ground plane* and the dimensions are differing from each other. Here, we used different firing voltages and drop space for these components according to different dimensions. With these optimized parameters which we believe are very suitable for this structure design, the final antenna has been printed, as shown in Figure I-33 and all the critical dimensions have been measured and compared with design values as presented in Table I-6. From Figure I-33, as-printed patterns are found to be homogeneous and continuous. The precision report in Table I-6 also indicates the quality and accuracy of our inkjet process.

Table I-5: Optimized printing parameters for printing antenna on PEN substrate

Parameters	**Firing voltage** (V)	**Drop space** (μm)	**Jetting frequency** (KHz)	**Substrate temperature** (℃)	**Sintering treatment** (min @ ℃)	**Resistivity** (μΩ·cm)
Values	16~25	20~25	3	25	30min @150 ℃	~20

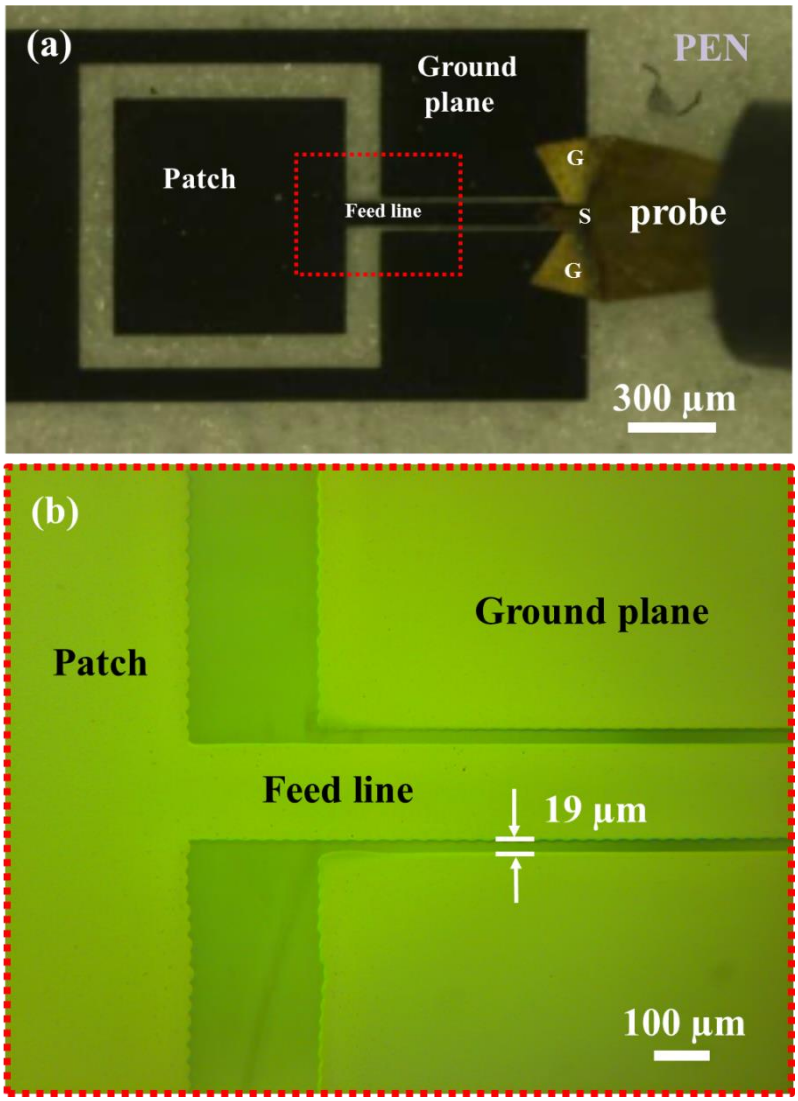


Figure I-33: Optical image of (a) the antenna fed by a 400 µm GSG probe (b) zoomed-in of red marked area

Table I-6: Summary of dimension performance for antenna

Demensions	Designed value **Vd** (mm)	Measured value **Vm** (mm)	Accuracy $100 - \frac{\lvert V_m - V_d \rvert}{V_d} d(\%)$
$\mathbf{H_{top}}$	1.12	1.124	99.4%
$\mathbf{H_{bot}}$	1.27	1.255	99%
$\mathbf{W_{groud}}$	0.195	0.204	95.4%
$\mathbf{L_{slot}}$	1.8	1.808	99.6%
$\mathbf{G_{slot}}$	0.2	0.197	98.5%
$\mathbf{L_{patch}}$	1.4	1.401	99.9%
W	0.15	0.152	98.7%
G	0.018	0.019	95%

I.4.2.2 The gain of antenna

Figure I-34 gives the simulated and measured gain of the coplanar square monopole versus frequency in the (φ, θ) = (0°, 90°) direction. The total realized gain is found to be higher than 0 dB in the range of 50 to 62 GHz. The very good agreement between simulation and measurement results demonstrates the quality of inkjet fabrication process in this work. The relative work has been published, and a comment from one reviewer is quoted as "*a very good technology push*" in this work.

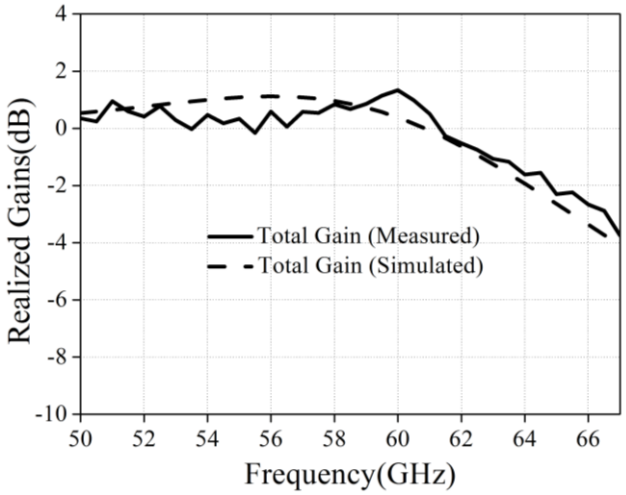


Figure I-34: Simulated (dashed line) and measured (plain line) total realized gain patterns at 60 GHz versus frequency

I.4.3 Structures for thermal conductivity measurement

I.4.3.1 Fabrication process of inkjet printing on polyimide substrate

Thermal conductivity is an important issue to be considered especially for the applications of flexible electronics, in which the polymer materials are commonly used as substrate, such as polyimide (PI) etc. Three omega method is one of the methods to measure thermal conductivity of solid or soft materials but with accuracy and simpleness. Nevertheless, the structure fabrication is still challenging due to the limitations of conventional technique of lithography, such as time consuming, costly and poor compatibility with arbitrary polymer substrates caused by using different chemical products during the process. Therefore, inkjet printing offers another alternative fabrication method and was first time, to our best knowledge, applied to deposit metallic line on polymer substrate for three omega method measurement.

The three omega method requires a metallic line, deposited on the surface of the sample to be tested, which serves as a heater and a temperature sensor. The thermal conductivity can be experimentally extracted from some analysis based on metallic resistance fluctuations when passing through alternating current.As shown in Figure I-35 (a), the metallic line with a certain length of L and width of 2b has two contact pads. To make fair comparison, six metallic lines were fabricated: three by conventional photolithography (lines A, B and C) and another three by inkjet printing (lines 1, 2 and 3).

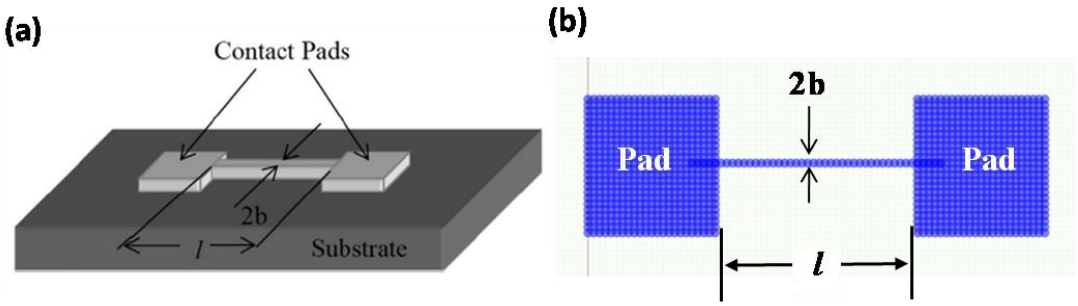


Figure I-35: Schematic of two pads metallic line with 2b width and l length of (a) original design and (b) Dimatix software design

The substrate used in this study is a black opaque polyimide sheet with thickness of 1 mm bought from Goodfellow Company. The challenge for inkjet printing is the relatively high roughness of this polyimide as shown in Figure I-36(a). To obtain a continuous line on such a rough surface, high firing voltage and jetting frequency were found to be preferable after different parameters test, and the final optimized parameters are presented in Table I-7. Figure I-36 (b) shows the metallic line (Au)

deposited by photolithography and Figure I-36 (c) shows the metallic line (Ag) fabricated by inkjet printing. As shown in Figure I-36 (b), the smooth boundary control of the printed line is difficult to obtain due to the high surface roughness, and the line width varies between 57 μm and 62 μm which yields an average width of around 60 μm.

Table I-7: Optimized printing parameters for printing metallic line on polyimide substrate

Parameters	**Firing voltage** (V)	**Drop space** (μm)	**Jetting frequency** (KHz)	**Substrate temperature** (℃)	**Sintering treatment** (min & ℃)	**Resistivity** (μΩ·cm)
Values	35	25	5	25	30min @200 ℃	~11

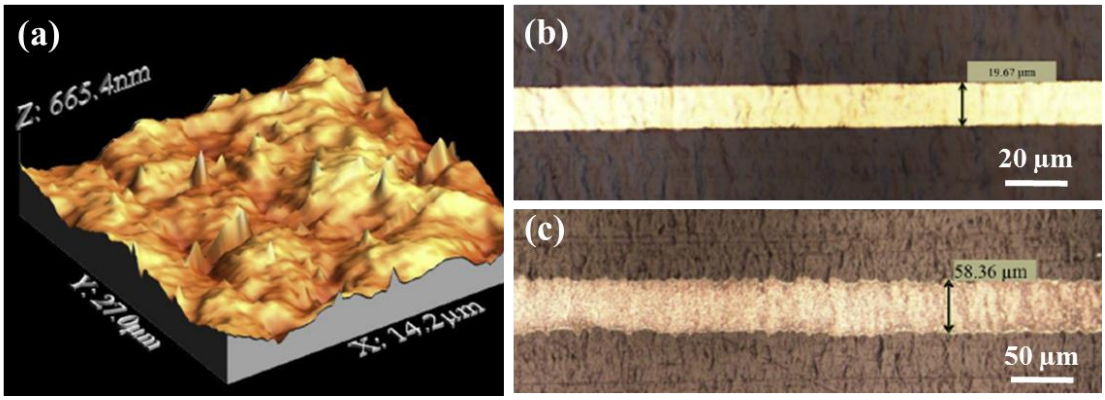


Figure I-36: (a) Scanning probe microscopy image of a the surface of polyimide and optical image of metallic line on polyimide fabricated (b) by photolithography and (c) by inkjet printing

I.4.3.2 Thermal conductivity

Table I-8 summarizes the properties of all the six metallic lines: the width 2b, the length L, the line resistance R, and the thermal conductivity K. We can find that by using three omega method, the thermal conductivity of the metallic lines obtained by inkjet printing technology agrees very well with that of metallic lines prepared by photolithography. The relative work has been published, and we hope this technique will be a promising method for characterization of many polymers that have low chemical resistance.

Table I-8: properties of metallic lines deposited by photolithography and inkjet printing on polyimide substrate

Technology	**Line**	**2b** (µm)	**L** (mm)	**R** (Ω)	**K** (W/m.K)
Photolithography	A	10	3	24.253	0.493
	B	20	10	38.806	0.511
	C	10	5	39.651	0.508
Inkjet printing	1	50	1	36.675	0.517
	2	60	2	39.825	0.498
	3	65	2	32.838	0.529

Conclusion of Chapter I

Firstly, we have explored the parameters optimization of inkjet printing technology based on Fujifilm Dimatix printer, commercial ink of Suntronic U5603 and substrates of PEN and KAPTON. Printing qualities variations caused by different equipment-dependent parameters were fully presented. We find that in general case, setting the ratio of drop spacing over droplet diameter around 0.7 could give nice printing qualities. Nevertheless, different firing voltage needs to be taken into account for different pattern dimension, and also for the consideration of nozzle jetting conditions. For the commercial ink and substrates of PEN and KAPTON, room temperature on substrate surface during printing is preferable due to the better wettability. The sintering temperature dependent resistivity of the ink Suntronic U5603 was also studied, the resistivity as low as 11.6 μΩ•cm could be achieved by sintering the ink at 200 ℃ for 30 mins.

Secondly, for applications based on our optimized printing parameters, different components have been realized. CPW transmission lines with different characteristic impedance on both PEN and KAPTON substrates have been successfully printed with good printing quality. The RF characterizations of these lines combining the considerations of geometric dimensions, sintering temperature, and substrate bending have been performed. For CPW lines on KAPTON, the loss lower than 0.4 dB/mm up to 40 GHz after 300 ℃ sintering was obtained, which is comparable to similar CPW lines fabricated by conventional lithography techniques. Also, we find that the RF performance of the CPW lines on KAPTON is minimally affected by substrate bending. Additionally, two collaboration work about antenna printing and three omega method structures printing have been shortly presented, which both further indicate the promising potential of the optimized inkjet printing technology in this work.

References of Chapter I

[1] B.-J. de Gans, P. C. Duineveld, and U. S. Schubert, "Inkjet Printing of Polymers: State of the Art and Future Developments," Advanced Materials, vol. 16, no. 3, pp. 203–213, Feb. 2004.

[2] O. Azucena, J. Kubby, D. Scarbrough, and C. Goldsmith, "Inkjet printing of passive microwave circuitry," in *Microwave Symposium Digest, 2008 IEEE MTT-S International*, 2008, pp. 1075–1078.

[3] S. Chung, S. O. Kim, S.-K. Kwon, C. Lee, and Y. Hong, "All-Inkjet-Printed Organic Thin-Film Transistor Inverter on Flexible Plastic Substrate," *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1134–1136, Aug. 2011.

[4] A. Nathan, A. Ahnood, M. T. Cole, Sungsik Lee, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, A. Dyadyusha, S. Haque, P. Andrew, S. Hofmann, J. Moultrie, Daping Chu, A. J. Flewitt, A. C. Ferrari, M. J. Kelly, J. Robertson, G. A. J. Amaratunga, and W. I. Milne, "Flexible Electronics: The Next Ubiquitous Platform," *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1486–1517, May 2012.

[5] D. Kim, S. Jeong, S. Lee, B. K. Park, and J. Moon, "Organic thin film transistor using silver electrodes by the ink-jet printing technology," *Thin Solid Films*, vol. 515, no. 19, pp. 7692–7696, Jul. 2007.

[6] E. Tekin, P. J. Smith, and U. S. Schubert, "Inkjet printing as a deposition and patterning tool for polymers and inorganic particles," *Soft Matter*, vol. 4, no. 4, p. 703, 2008.

[7] J. Perelaer, P. J. Smith, D. Mager, D. Soltman, S. K. Volkman, V. Subramanian, J. G. Korvink, and U. S. Schubert, "Printed electronics: the challenges involved in printing devices, interconnects, and contacts based on inorganic materials," *Journal of Materials Chemistry*, vol. 20, no. 39, p. 8446, 2010.

[8] P. Calvert, "Inkjet Printing for Materials and Devices," *Chemistry of Materials*, vol. 13, no. 10, pp. 3299–3305, Oct. 2001.

[9] J. Perelaer, C. E. Hendriks, A. W. M. de Laat, and U. S. Schubert, "One-step inkjet printing of conductive silver tracks on polymer substrates," *Nanotechnology*, vol. 20, no. 16, p. 165303, Apr. 2009.

[10] H. M. Haverinen, R. A. Myllylä, and G. E. Jabbour, "Inkjet printing of light emitting quantum dots," *Applied Physics Letters*, vol. 94, no. 7, p. 073108, 2009.

[11] Y. Neuvo, S. Ylönen, "Bit Bang – Rays to the Future," Helsinki University Print, Helsinki, Finland, pp. 63-102, 2009.

[12] M. L. Kleper, "Printed electronics and the automatic identification of objects: an investigation of the merging and developing technologies related to the generation beyond print-on-paper," Graphic Arts Technical Foundation, Pittsburgh, US, 2004

[13] A. Hodgson. "The role of paper in the future of printed electronics," Proc. 2nd International Workshop on Collaborating over Paper and Digital Documents, London, UK, 2007

[14] J. M. Xu, "Plastic electronics and future trends in microelectronics," *Synthetic Metals*, vol.115, no.1-3, pp.1-3, 2000

[15] OE-A workshop "polymer electronics on flexible substrates," Lyon, 2009

[16] B.-J. de Gans, P. C. Duineveld, and U. S. Schubert, "Inkjet Printing of Polymers: State of the Art and Future Developments," *Adv. Mater.*, vol. 16, no. 3, pp. 203–213, Feb. 2004.

[17] M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, "Inkjet Printing-Process and Its Applications," *Adv. Mater.*, vol. 22, no. 6, pp. 673–685, Feb. 2010.

[18] Dimatix Materials Printer DMP-2800 Series User Manual, FUJIFILM Dimatix, Inc.

[19] H.-Y. Tseng, V. Subramanian, "All Inkjet Printed Self-Aligned Transistors and Circuits Applications," IEEE International Electron Devices Meeting (IEDM), 2009, pp.1-4

[20] L. Yang and M. M. Tentzeris, "Design and characterization of novel paper-based inkjet-printed RFID and microwave structures for telecommunication and sensing applications," in Microwave Symposium, 2007. IEEE/MTT-S International, 2007, pp. 1633–1636.

[21] J. Doggart, Y. Wu, and S. Zhu, "Inkjet printing narrow electrodes with <50 μm line width and channel length for organic thin-film transistors," *Appl. Phys. Lett.*, vol. 94, no. 16, p. 163503, 2009.

[22] W. MacDonald, K.Rollins, D. MacKerron, R. Eveson, R. Rustin, R. Adam, K. Looney, K. Rakos and K. Hashimoto, Latest Developments In Polyester Film For Flexible Electronics, DuPont Teijin Films

[23] DuPont Kapton HN polyimide film, Technical Data sheet

[24] J. S. Kang, H. S. Kim, J. Ryu, H. Thomas Hahn, S. Jang, and J. W. Joung, "Inkjet printed electronics using copper nanoparticle ink," *Journal of Materials Science: Materials in Electronics*, vol. 21, no. 11, pp. 1213–1220, Nov. 2010.

[25] Y. Li, Y. Wu, and B. S. Ong, "Facile Synthesis of Silver Nanoparticles Useful for Fabrication of High-Conductivity Elements for Printed Electronics," *Journal of the American Chemical Society*, vol. 127, no. 10, pp. 3266–3267, Mar. 2005.

[26] Y. Lee, J. Choi, K. J. Lee, N. E. Stott, and D. Kim, "Large-scale synthesis of copper nanoparticles by chemically controlled reduction for applications of inkjet-printed electronics," *Nanotechnology*, vol. 19, no. 41, p. 415604, Oct. 2008.

[27] J. Perelaer, M. Klokkenburg, C. E. Hendriks, and U. S. Schubert, "Microwave Flash Sintering of Inkjet-Printed Silver Tracks on Polymer Substrates," *Adv. Mater.*, vol. 21, no. 47, pp. 4830–4834, Dec. 2009.

[28] T. H. J. van Osch, J. Perelaer, A. W. M. de Laat, and U. S. Schubert, "Inkjet Printing of Narrow Conductive Tracks on Untreated Polymeric Substrates," *Adv. Mater.*, vol. 20, no. 2, pp. 343–345, Jan. 2008.

[29] S. H. Ko, H. Pan, C. P. Grigoropoulos, C. K. Luscombe, J. M. J. Fréchet, and D. Poulikakos, "All-inkjet-printed flexible electronics fabrication on a polymer

substrate by low-temperature high-resolution selective laser sintering of metal nanoparticles," *Nanotechnology*, vol. 18, no. 34, p. 345202, Aug. 2007.

[30] M. L. Allen, M. Aronniemi, T. Mattila, A. Alastalo, K. Ojanperä, M. Suhonen, and H. Seppä, "Electrical sintering of nanoparticle structures," *Nanotechnology*, vol. 19, no. 17, p. 175201, Apr. 2008.

[31] J. Perelaer, B.-J. de Gans, and U. S. Schubert, "Ink-jet Printing and Microwave Sintering of Conductive Silver Tracks," *Advanced Materials*, vol. 18, no. 16, pp. 2101–2104, Aug. 2006.

[32] D. Tobjörk, H. Aarnio, P. Pulkkinen, R. Bollström, A. Määttänen, P. Ihalainen, T. Mäkelä, J. Peltonen, M. Toivakka, H. Tenhu, and R. Österbacka, "IR-sintering of ink-jet printed metal-nanoparticles on paper," *Thin Solid Films*, vol. 520, no. 7, pp. 2949–2955, Jan. 2012.

[33] J. Niittynen, R. Abbel, M. Mäntysalo, J. Perelaer, U. S. Schubert, and D. Lupo, "Alternative sintering methods compared to conventional thermal sintering for inkjet printed silver nanoparticle ink," *Thin Solid Films*, vol. 556, pp. 452–459, Apr. 2014.

[34] I. Reinhold, C. E. Hendriks, R. Eckardt, J. M. Kranenburg, J. Perelaer, R. R. Baumann, and U. S. Schubert, "Argon plasma sintering of inkjet printed silver tracks on polymer substrates," *Journal of Materials Chemistry*, vol. 19, no. 21, p. 3384, 2009.

[35] B. J. Perelaer, A. W. M. de Laat, C. E. Hendriks, and U. S. Schubert, "Inkjet-printed silver tracks: low temperature curing and thermal stability investigation," *Journal of Materials Chemistry*, vol. 18, no. 27, p. 3209, 2008.

[36] S. Jang, Y. Seo, J. Choi, T. Kim, J. Cho, S. Kim, and D. Kim, "Sintering of inkjet printed copper nanoparticles for flexible electronics," *Scripta Materialia*, vol. 62, no. 5, pp. 258–261, Mar. 2010.

[37] Rainee N. Simons, Coplanar Waveguide Circuits, Components, and Systems. John Wiley & Sons, 2001

[38] C.-J. Chiang, C. Winscom, S. Bull, and A. Monkman, "Mechanical modeling of flexible OLED devices," Org. Electron., vol. 10, no. 7, pp. 1268–1274, Nov. 2009.

[39] L. Yang, A. Rida, R. Vyas, and M. M. Tentzeris, "RFID Tag and RF Structures on a Paper Substrate Using Inkjet-Printing Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2894–2901, Dec. 2007.

[40] V. Subramanian, P. C. Chang, J. B. Lee, S. E. Molesa, and S. K. Volkman, "Printed organic transistors for ultra-low-cost RFID applications," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 4, pp. 742–747, Dec. 2005.

[41] V. Lakafosis, A. Rida, R. Vyas, L. Yang, S. Nikolaou, and M. M. Tentzeris, "Progress Towards the First Wireless Sensor Networks Consisting of Inkjet-Printed, Paper-Based RFID-Enabled Sensor Tags," *Proceedings of the IEEE*, vol. 98, no. 9, pp. 1601–1609, Sep. 2010.

Chapter II

On rigid substrate: bottom gate Graphene Field Effect Transistor with dielectric of natural oxide

Table of Content-Chapter II

Chapter II On rigid substrates: bottom gate Graphene Field Effect Transistor with dielectric of natural oxide

II.1 Introduction

Graphene, a two-dimensional carbon material, has attracted attention for developing novel electronic devices due to its unique electronic properties, the high mobility and saturation velocity of carriers. One promising application of graphene is to be used as channel material for radio frequency field effect transistors.

In this chapter, after a brief presentation of graphene material and state of the art of graphene field effect transistors (GFETs), we present the fabrication and characterization of GFETs on rigid substrates. A bottom gate with natural aluminum oxide as its dielectric is used to avoid the conventional atomic layer deposition (ALD) technique beacause it needs high temperature. Chemical vapor deposition (CVD) grown graphene on copper foil is adopted and, particularly, an optimized conventional graphene wet transfer process is developed. The quality of monolayer graphene is well preserved both after graphene transfer and device fabrication process.

In the second part, the transistors with different geometry (gate length of 100, 200 and 300 nm combining with gate width of 12, 24 and 50 μm) have been characterized by both static and dynamic measurements. We report an intrinsic current gain cut-off frequency ($f_{t\text{-}int}$) of 15.5 GHz and maximum oscillation frequency (f_{max}) of 11 GHz in devices with 100 nm gate length and 12 μm gate width.

It's important to note that the objective of this work is not to compete with the state of the art on rigid substrates, but to achieve proof of concept of a low thermal budget process compatible with flexible substrates. The results presented in this chapter indicate that the full fabrication process exhibits great potential for graphene based flexible electronics.

II.2 Description of graphene and graphene transistor

Before talking about graphene transistors, we will start by a brief discussion about the graphene material properties, especially the unique electronic properties which are relevant to transistors. Besides, the mechanical and optical properties of graphene will be shortly mentioned, which also show that graphene is a very suitable material for flexible electronics.

We will then introduce graphene field effect transistors, because so far most work on graphene devices has been related to field effect transistors (FET). The GFETs operation principle will be shortly introduced. Compared to conventional silicon or III-V materials, we will find why graphene is regarded as a promising candidate channel material for post-silicon era. Finally, the state of the art for radio frequency GFETs figures of merit, cut-off frequency (f_T) and maximum oscillation frequency (f_{max}), will be presented.

In this work, the chemical vapor deposition (CVD) growth of graphene and a wet transfer technique were used. The work of graphene growth was carried out by G. Deokar, who is from the EPIPHY group in IEMN. She also worked on the optimization of the graphene wet transfer process. The optimized transfer recipe is used in my device fabrication. Therefore, in last part of introduction, we will discuss about graphene growth and transfer. Particularly, it's worth to provide more details of the graphene transfer process, because the transistor performances are strongly determined by this process.

II.2.1 Graphene properties

Graphene, a single atomic layer of sp2-hybridized carbon atoms arranged into a hexagonal honeycomb lattice, is the first truly two-dimensional crystalline material with extremely high carrier mobility and has attracted intense scientific interest.

The low-energy electronic band structure of graphene can be well described by a simple tight-binding Hamiltonian considering only nearest-neighbor hopping and one π orbital per carbon atom. In pristine non-doped graphene, the conduction and valence bands touch at the K and K' points, so graphene is a zero-gap material. The energy bands near K (K') yields a linear dispersion which produces touching conic bands at the K and K' points of the Brillouin zone as shown in Figure II-1. Electrons in graphene are referred to as Dirac fermions because the energy–momentum relation is linear for low energies near the 6 individual corners of the Brillouin zone and these 6 touching points in momentum space on the edge of the Brillouin zone are called Dirac points. At the

Dirac point, electrons and holes have zero effective mass[1-3].

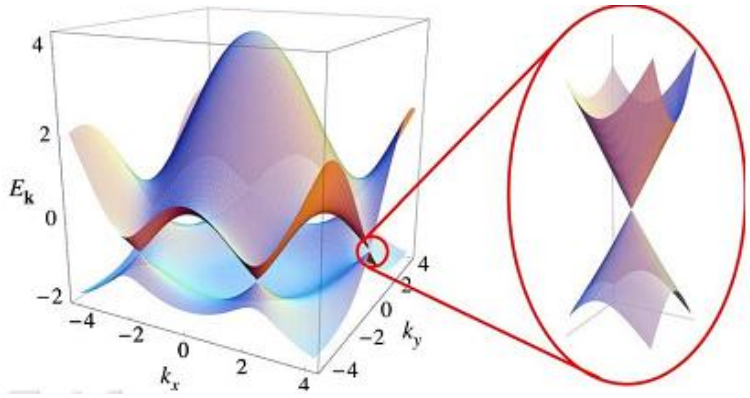


Figure II-1: Electronic dispersion in the honeycomb lattice. Right: zoom in of the energy bands close to one of the Dirac points.

II.2.1.1 Transport properties

Owing to its unique band structure, graphene exhibits novel transport effects, which leads to exceptional transport properties in comparison with common semiconductors. This can be seen on Table II-1 which compares two of the main electronic properties (carrier mobility and saturated velocity) of graphene with those of common bulk semiconductors.

Table II-1:Comparison between the electronic properties of graphene and common bulk semiconductors. Energy band gap (Eg), electron effective mass (m^*/m_e), electron mobility (μ_e) and electron saturation velocity (v_{sat})

	Eg at 300K (eV)	m^*/m_e	μ_e at 300K ($cm^2V^{-1}s^{-1}$)	v_{sat} (10^7 cm/s)
Si	1.1	1.08	1350	1
Ge	0.67	0.55	3900	0.6
Ga As	1.43	0.067	4600	2
AlGaN/GaN 2DEG	3.3	0.19	1500-2000	3
lnSb	0.17	0.014	8×10^4	
Graphene	0	0	500-2×10^5	4

In graphene, the E-k relationship near the Dirac point is linear [4]; this makes the velocity of carriers independent of energy, and is equal to the Fermi velocity. Hence, spin in graphene can be transported at the Fermi velocity. In the case of graphene, Fermi velocity V_F is expected to be 1×10^6 m/s for high quality graphene.

With this graphene device in hand, one can tune the charge carrier density between holes and electrons by applying a gate voltage (V_g) above graphene, see the insets of Figure II-2. The gate voltage induces a surface charge density $n=\varepsilon_0\varepsilon V_g/t_e$, where ε_0 is the dielectric permittivity, where e is the electron charge and t is the thickness of the dielectric layer. This charge density shifts with the Fermi level position (E_f) in the band structure.[1][5]

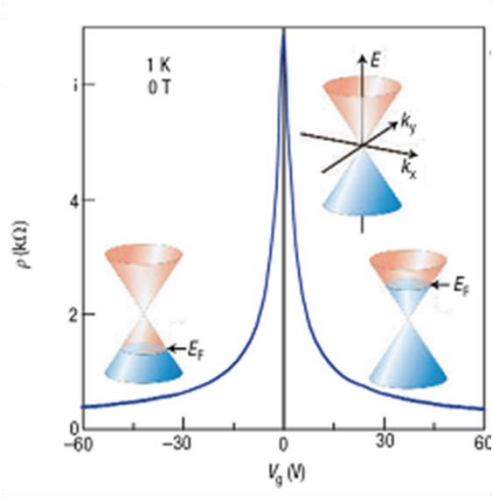


Figure II-2: Ambipolar electric field effect in graphene corresponding to the change in resistivity. The insets show the changes in the position of the Fermilevel Ef as a function of gate voltage[6]

Another important advantage of graphene is its high carrier mobility at room temperature. Mobility, as high as 10^6 $cm^2V^{-1}s^{-1}$, has been recently reported for suspended graphene[1]. For large-area graphene grown on Cu and transferred to a substrate, mobility greater than 7,000 $cm^2V^{-1}s^{-1}$have been measured.

The mobility is constant but only for low electric fields. As the channel length decreased, the field becomes higher so that at high electric field, the carrier velocity saturates. In this case, the concept of mobility is no longer valid but the saturation velocity becomes important for carrier transport. For graphene, the maximum carrier saturation velocity of 4×10^7 cm s^{-1} has been predicted as compared to 2×10^7 cm s^{-1} for GaAs and 1×10^7 cm s^{-1} for silicon.

II.2.1.2 Other properties

Besides its unique electrical properties, graphene is a promising transparent conductor with unique optical properties, and also the strongest material ever measured with a high elasticity.

Simply because graphene is very thin, photons can easily pass through it. Consequently, the optical properties, in particular, the high transparency and low

reflectance of graphene make it an attractive choice for use in optoelectronic devices. Each single layer graphene will contribute an absorbance of 2.3% to visible light. The absorbance of few-layer graphene sheets is roughly proportional to the number of layers.

Graphene is also the strongest material ever tested, with a Young's modulus of 1 TPa and an intrinsic breaking strength of 42 Nm^{-1}. Therefore, combined with its excellent electrical property, it is very promising for applications in flexible electronics.

II.2.2 Field effect transistors based on graphene

For the past decades, the semiconductor industry has enjoyed a dynamic evolution which leads to an annual market growth of around 17%. The famous Moore's law has been followed so far mainly due to the success of continuous scaling of silicon metal-oxide-semiconductor field-effect transistor (Si MOSFET) [7]. 20 nm gates have been achieved for MOSFET and are in mass production today with future perspective of 10 nm gates anticipated by the International Technology Roadmap for Semiconductors (ITRS)[8]. However, it becomes increasingly difficult to further reduce the Si MOSFET dimensions for higher performance. The bottleneck comes from short-channel effects, increased parasitic elements and difficulties in terms of fabrication technology at the industry level. Therefore, the device engineers are making considerable effort to find new channel materials particularly with high carrier mobility, so that the Moore's law can be continued in a healthy way [9].

Graphene, a two dimensional lattice of carbon atoms arranged in a honeycomb lattice, has attracted enormous attentions for the development of novel electronic devices since 2004[10][11]. The interest for this material stems from the unique electronic and mechanical properties of graphene which derive from its truly two-dimensional nature, the high mobility, high Fermi velocity and massless Dirac fermions character of the charge carriers[12][13]. Many works have been achieved on field effect transistors using graphene as the channel material. Figure II-3 shows the main aspects involved for the application of graphene based transistors. Among these works, two main directions of the GFETs have been explored.

One is the transistors switching ability, with the potential of being used for logic integrated circuits application. Owing to the absence of gap in graphene, the channel of GFET does not switch off, and consequently the I_{on}/I_{off} ratio is very low (large-area gapless graphene with on-off ratio only 2~20, comparing to 10^4~10^7 for Si MOSFET)[14][15]. Nevertheless, there are several ways of opening the graphene gap, such as to pattern graphene as nano-ribbons[16][17], to obtain A-B staked bilayer

graphene[18][19], or even to apply strain onto graphene sheet[20][21]. Meanwhile, it should be noticed that the high mobility will suffer from creating a bandgap[22]. Therefore, many challenges still remains in this direction and intensive work on such type of transistor application is under way.

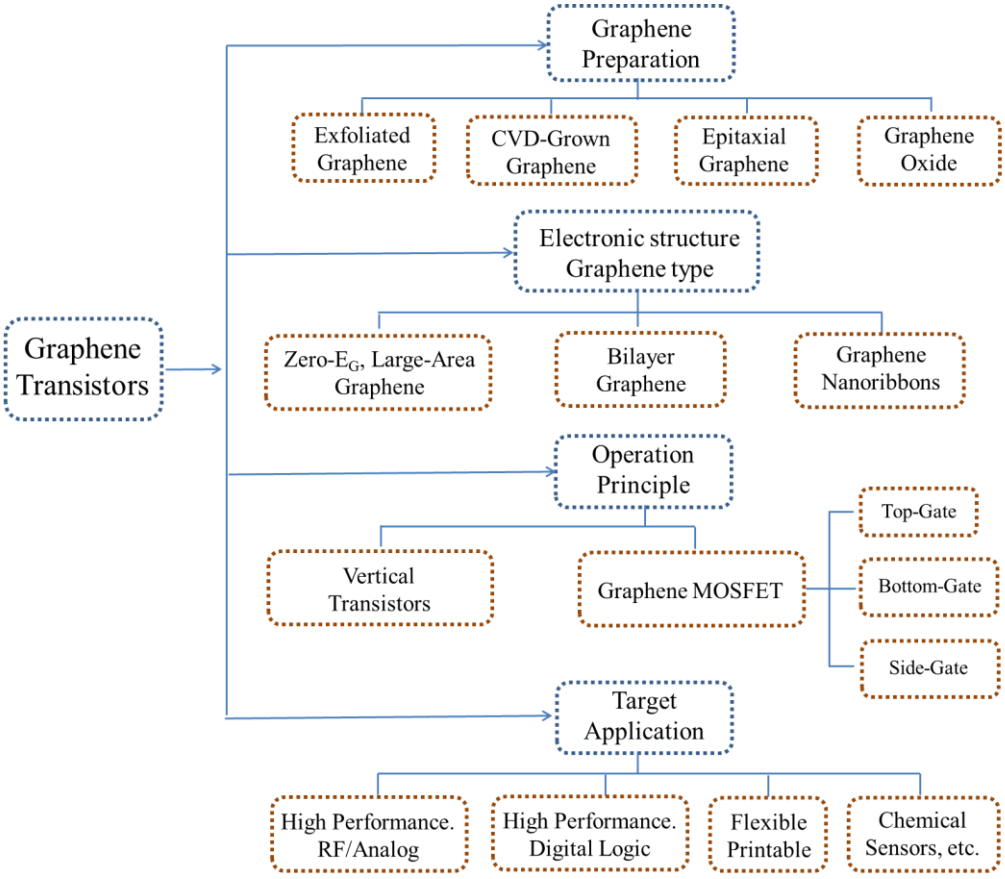


Figure II-3: Classification schemes for graphene transistors, source from[12]

Another direction is to amplify signals and provide gain, which is suitable for analog/radio-frequency (RF) applications. The field of RF transistors has seen fast advances in wireless communications, and many different transistor types based on various materials have been realized, such as high-electron-mobility transistors (HEMTs) based on III-V semiconductors (GaAs, InP, Si n-channel MOSFETs) and different types of bipolar transistors[23][24]. For such RF transistors, the device does not need to switch off in the operating regime and high mobility plays a critical role. Therefore, large area graphene has been regarded as a promising candidate to be used as channel material for post-silicon RF electronics. Additionally, the short channel effect due to scaling down the gate length could be suppressed if a thin enough (in thickness) channel material is used [25]. With just one atomic layer thickness, graphene perhaps is the most attractive material.

The basic operation principle for a FET relies on the variation of channel

conductivity, and thus the drain current Ids is controlled by gate voltage Vgs. See Figure II-4, the Ids-Vgs behavior is shown in transfer characteristic, the variation of drain current according to gate voltage is defined as transconductance, gm ($g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$).

For high speed applications, FETs should respond quickly to the variation of Vgs, which means a large gm is desired. As seen in Figure II-4, the transfer characteristic of GFETs has an unique ambipolar effect due to the gapless nature of graphene. The carrier density and type of carrier (electrons or holes) are controlled by gate voltage. Positive gate voltages promote an electron accumulation in the channel (n type channel), and negative gate voltages cause a p-type channel. The type of carriers changes at the Dirac point. Figure II-4 shows an ideal case without any doping. The output characteristic of the conventional Si MOSFET exhibits two regimes, the linear regime of Ids with low Vds and the saturation regime with high Vds. For graphene FET, the output curve always shows a linear shape without any saturation or only weak saturation. The absence of drain current saturation is also due to the graphene's gapless band structure. The output conductance, g_{ds} ($g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$), can be extracted from the output drain current curve.

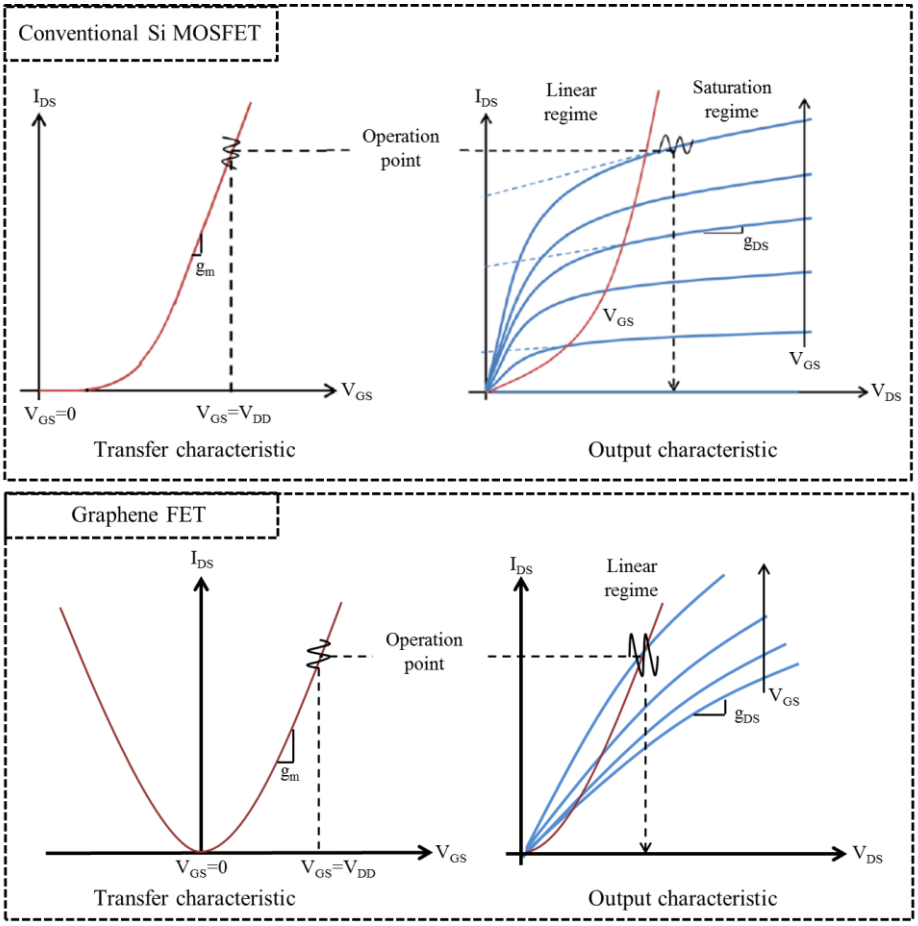


Figure II-4: Illustration of transfer characteristic and output characteristic for both conventional Si MOSFET and Graphene FET.

To discuss the radio frequency performance, a small signal equivalent circuit is needed, and is schematized in Figure II-4. As shown in Figure II-4, when optimized DC values of Vds and Vgs (with the best gm) are found, an input small radio frequency signal is superimposed to the fixed DC value of Vgs. The small gate voltage variation ±ΔVgs leads to a drain current which varies accordingly, and this amplified current signal is the GFET output. The amplification characteristics of transistors are described in terms of current gain H_{21} and unilateral power gain U. Two figures of merits are often used for RF transistors, the cut-off frequency f_T (related to the current gain) and the maximum oscillation frequency f_{max} (which measures the power gain). The cut-off frequency is the frequency at which the magnitude of H_{21} has dropped to unity (0 dB) and the unilateral power gain equals unity at f_{max}. Therefore, f_T and f_{max} mark upper frequency limits and transistors will lose the ability to amplify the input signal if used beyond these frequencies. Since RF transistors are operating at high frequency (Gigahertz or Tera Hertz), the parasitic effects of the measurement setup and probe pads on the transistor parameters can be notable. Therefore, a de-embedding procedure is commonly used to exclude all those effects so that the intrinsic performance of the

transistor can be explored. Equation II-1 and II-2 give an approximation of intrinsic f_T and f_{max} respectively. The useful approximations for extrinsic performances can be found in [26-28]

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs}+C_{gd}} \qquad \text{(II-1)}$$

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \cdot \frac{1}{(g_d R_i)^{1/2}} \qquad \text{(II-2)}$$

Where Cgs is the gate-source capacitance, Cgd the gate-drain capacitance, gd the output conductance and Ri the sum of gate resistance and drain source resistance (all these elements are deduced from small signal equivalent circuit shown in section II.4.3.2).

Generally, to achieve high intrinsic f_T and f_{max}, the transistor's transconductance should be as large as possible and all the other elements should be as small as possible. The g_m is mainly dependent on the mobility of the channel material, making graphene a very interesting material due to its high mobility. Therefore, GFETs have shown impressing f_T performances, which are even competitive with the best performances of conventional FET[29-32]. On the contrary, GFETs behave rather poorly in terms of maximum frequency of oscillation f_{max}, as it is difficult to obtain the saturation of drain current and thus a small value of gd, due to the gapless nature of graphene and also to contact resistance issues. Table II-2 shows the state of the art for both f_T and f_{max} intrinsic performance of GFETs on rigid substrates. Large value of f_T >300 GHz have been reported. The gate length scaling has revealed that in GFETs f_T generally increases with decreasing gate length, similarly to conventional semiconductor based FET transistors. The current record f_{max} of 38 GHz has been reported for a 70 nm gate length with self-aligned T-shaped gate geometry (f_{max} = 70 GHz after de-embedding)[33].

Note that the result of IEMN shown in Table II-2 comes from the work of a previous PhD student, Nan Meng, who has reported 60 GHz of intrinsic f_T and 30 GHz of f_{max} from top-gated graphene nanoribbon-based FET on SiC substrate[34].

In this chapter, we report an intrinsic current gain cut-off frequency of 15.5 GHz and a maximum oscillation frequency of 11 GHz from 100 nm gate length (12 µm gate width) bottom-gated GFET on Si/SiO_2 substrate. Although our performances are lower than the state of the art for rigid substrate, the purpose of this work is to develop a fabrication method which is compatible with flexible substrates. We use natural oxidation of aluminum to make the dielectric layer, which avoids high temperature processes such as ALD and thus reduces the risk of damaging flexible substrates. Our device fabrication relies on an optimized CVD graphene wet transfer work[35]. We believe that our fabrication method provides an alternative way for future flexible

GFETs. Such devices have been realized on a flexible substrate, kapton, which will be discussed in Chapter 3.

Table II-2: Details of the performance reported in Figure II-3

	Transistor	f_t (GHz)	f_{max} (GHz)	g_m (mS/μm)	L_g (nm)	μ ($cm^2/V^{-1}s^{-1}$)	Ref.
Graphene	CVD	427	-	1.33	67	2000	[36]
	Exfoliation	300	-	1.27	nanowire	3300	[37]
	Epitaxy	350	42	-	-	3000	[38]
	CVD	300	44	-	-	3000	[38]
	Epitaxy	110	70	0.25	100	8700	[33]
	Epitaxy	93	105	0.7	100	1170	[39]
	Epitaxy GNRFET(IEMN)	**60**	**30**	**0.9**	**150**	**460**	**[34]**
Si	Silicon	485	-	1.3	29	1400	[40]
	ITRS 2014	480	540	-	18	-	[40]
III-V	InP	385	>1100	1.2	<50	15000	[40]
	IbAs	628	331	1.62	30	13200	[40]

II.2.3 Graphene synthesis

There are several methods for production of graphene, which can be classified as: (1) top down method, such as mechanical exfoliation of highly oriented pyrolitic graphite (HOPG), liquid phase exfoliation from bulk graphite and graphene oxide reduction; (2) bottom up method, such as Molecular beam epitaxy (MBE) on silicon carbide (SiC) and Chemical Vapor Deposition (CVD) on metals**.** Figure II-5 shows the comparison of these mass-production methods of graphene in terms of quality and price. Table II-3 gives the properties and applications of graphene obtained by different methods. It can be seen that CVD graphene combines the advantages of being able to provide large scale material with good quality and low cost. The according transfer technique in development makes an unlimited possibility to apply CVD graphene on

arbitrary substrate, especially on flexible substrates. Therefore, the CVD graphene is used in this work.

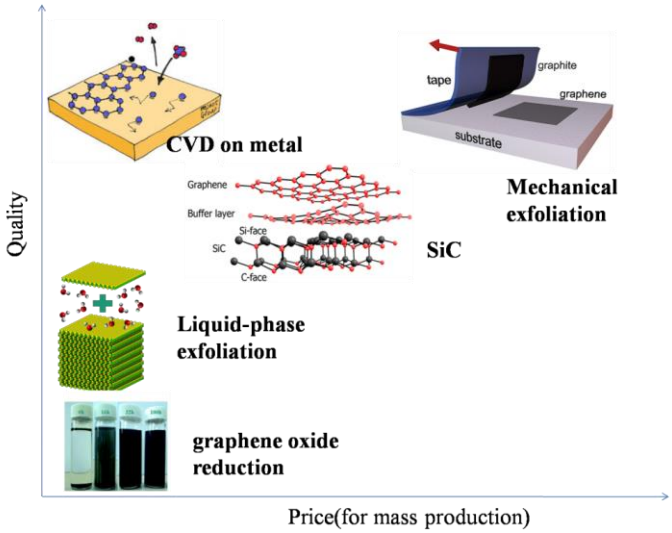


Figure II-5: Several methods of mass-production of graphene, which allow a wide choice in terms of size, quality and price for any particular application[41].

Table II-3: Properties and application of graphene obtained by different methods

Method	**Advantage**	**Disadvantage**	**Mobility ($cm^2V^{-1}s^{-1}$)**	**Applications**
Mechanical exfoliation	Low cost, good quality crystalline	Unproducible, small area	$>2\times10^5$	Research
Liquid-pahase exfoliation	Mass production	Requirement of reduction	10^2	Coatings, paint/ink, composites, transparent conductive layers, energy storage, bioapplications
graphene oxide reduction	Large scale	inferior electrical properties requirement of reduction	1	Coatings, paint/ink, composites, transparent conductive layers, energy storage, bioapplications
CVD on metal	Large covered area	Requirement of transfer	$10^2$$10^3$	Photonics, nanoelectronics, transparent conductive layers, sensors, bioapplications
SiC	High quality	Costly growth	$10^3$$10^4$	High-frequency transistors and other electronic devices

II.2.3.1 Graphene growth by CVD in this work

CVD method is an attractive approach to produce graphene, because large graphene domains can be obtained, and most importantly, graphene deposited on some transition metals [Cu, Ni, Ru, Ir, Co, Pt, Pd] can be transferred to other substrates[42][43]. In the beginning of this work, Ni was used for graphene synthesis. But very soon we changed to use Cu for mainly two reasons. First, the carbon solubility in Cu at graphene growth temperature (~1000 to 1070 ℃) is extremely low (0.03 atom%)[44], so single-layer graphene growth will predominantly occur on Cu. Second, the flexible Cu foils are available at low cost.

Cu foil (50 μm thick Alfa-Aesar, purity 99.9999%) is used in this work for graphene growth. Figure II-6 (a) shows the picture of rapid thermal processing CVD reaction chamber used for graphene growth; (b) shows the schematic of the chamber structure. Prior to graphene growth, the Cu foil was pre-cleaned in acetic acid to remove surface oxide. The optimized growth parameters in terms of temperature and time are described in Figure II-6 (c). During the annealing phase, the sample is exposed to Ar/H_2: 100/10 sccm with 10 Torr chamber pressure. In the growth phase, 20 sccm of CH_4 is introduced into chamber for five minutes. After growth, the sample is fast cooled down (30 ℃/s) below 700 ℃ and further slowly to room temperature with Ar and H_2 ambient.

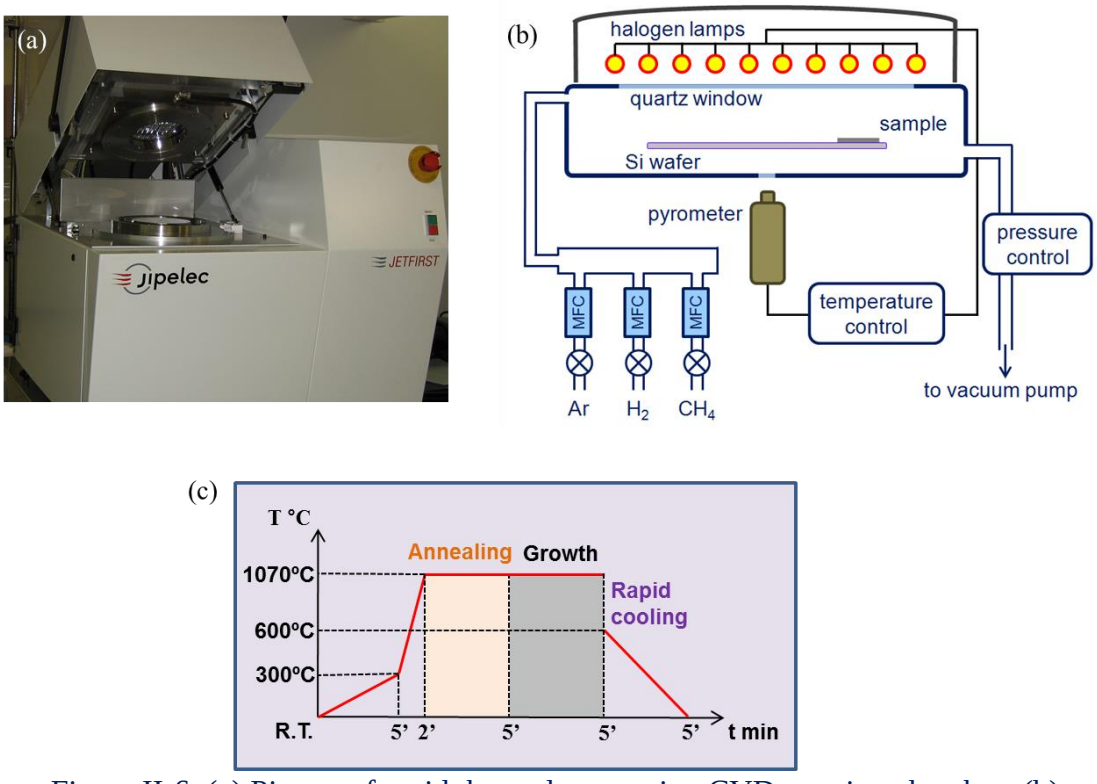


Figure II-6: (a) Picture of rapid thermal processing CVD reaction chamber; (b) schematic of the chamber structure; (c) optimized growth parameter

Figure II-7 (a) shows an example of a Cu foil after graphene growth; (b) provides a zoomed-in optical image of the selected region in (a). T1 and T2 in (b) represent two points where we measured the Raman spectra which are shown in (c). We observe that the Raman intensity ratio between 2D band and G band is 3.5, which indicates that monolayer graphene is obtained on Cu. Typically, the high 2D/G intensity ratio (>2) indicates monolayer graphene with low charged impurity concentration. Besides, the Raman intensity ratio between the D and G bands is 0.2 or even less, which demonstrates a low defect density. From these two ratio, we can conclude that high quality monolayer graphene has been obtained on Cu foil using optimized growth parameters. Note that graphene growth optimization has been completed by G. Deokat during her postdoctoral stay.

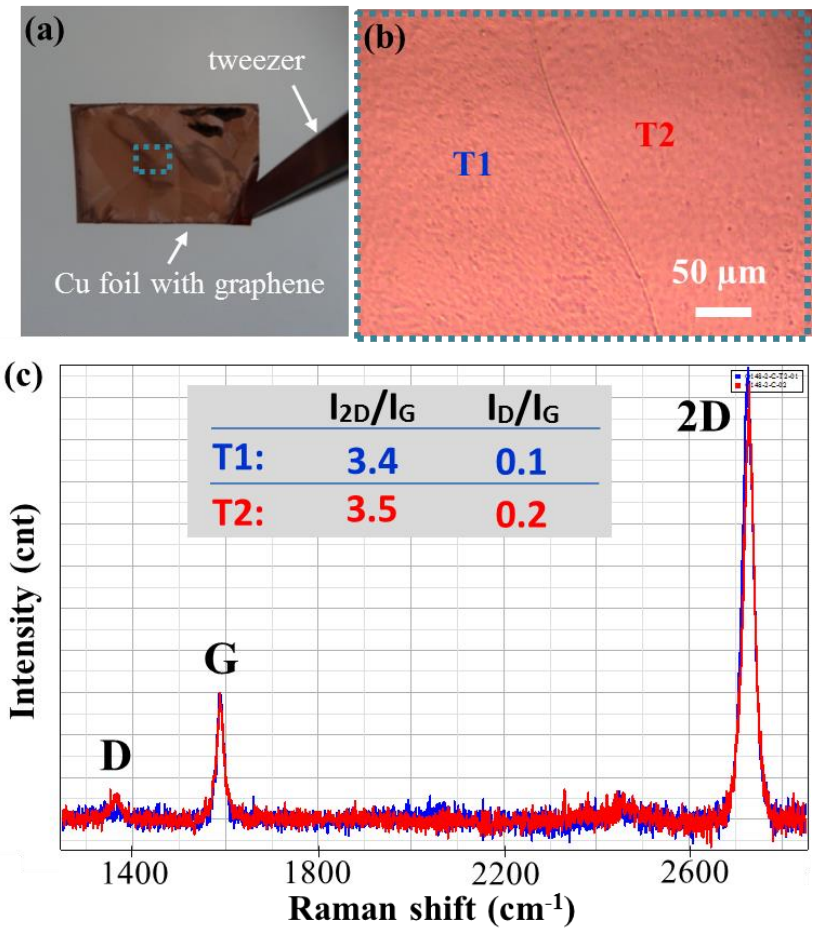


Figure II-7: (a) Picture of Cu foil after graphene growth; (b) zoomed-in optical image of selected area in (a), in which T1 and T2 in represent two points where we make the Raman measurement; (c) Raman spectra obtained in two neighboring Cu grain (denoted by T1 and T2 in (b))

II.2.3.2 Graphene transfer process in this work

I was mainly involved in graphene transfer and device fabrication, including

optimizing many crucial processing steps. A conventional PMMA based wet chemical transfer process has been used all through my PhD work for different samples, but with significant improvement from the beginning to the end. The challenges for this transfer process can be summarized as (1) the selection of an optimum Cu etchant to avoid metallic contaminations; (2) a reproducible method to avoid crack, hole and fold formation; (3) an efficient way of PMMA removal; (4) formation of strong adhesion between graphene and target substrate to avoid graphene delamination. To tackle these challenges, a transfer process was optimized, which is shown in Figure II-8, and more details for each step will be provided in the following part.

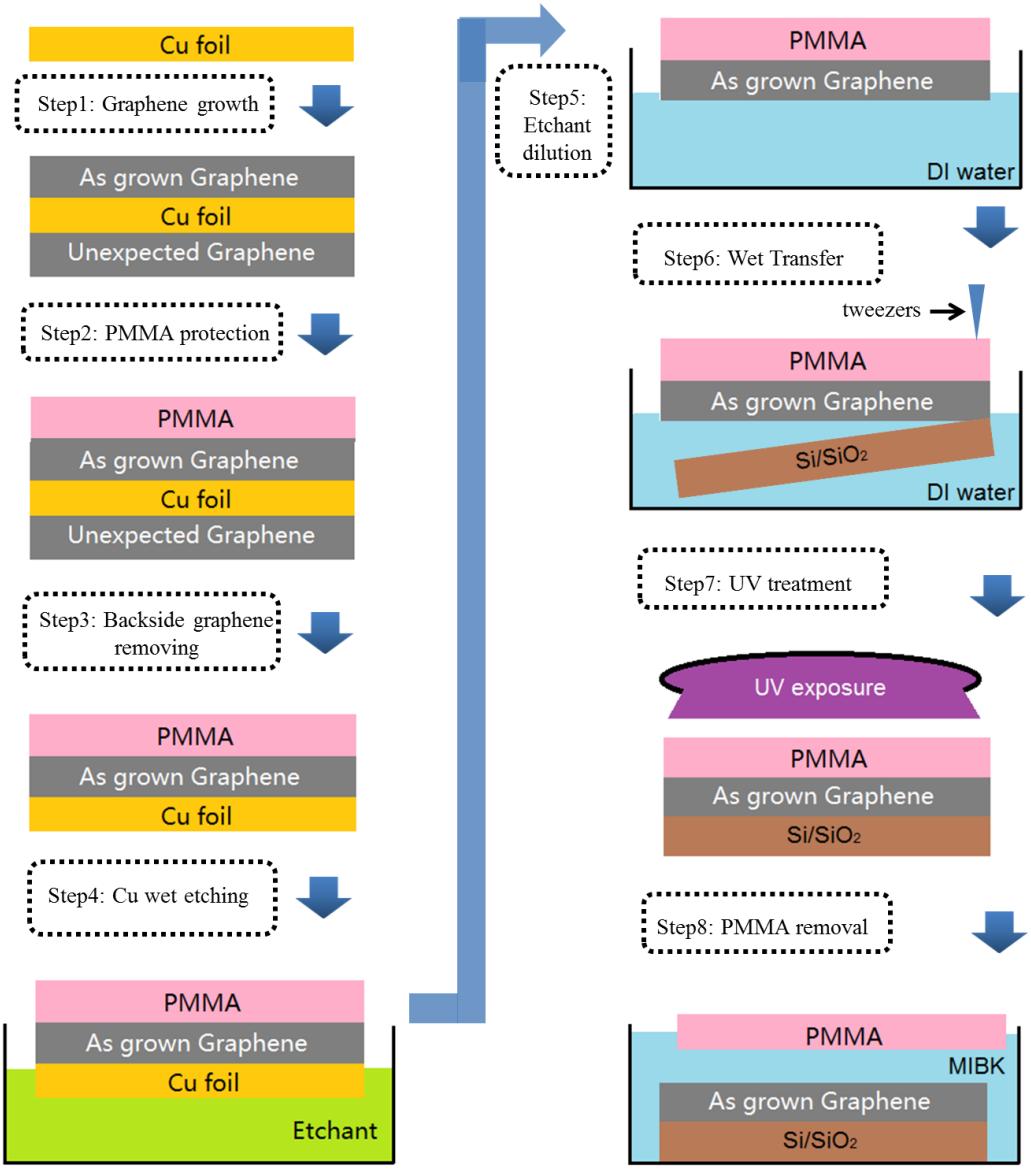


Figure II-8: General wet graphene transfer process with optimized steps

Step 1: Graphene growth

As discussed above, graphene grown by CVD on Cu foil with centimeter scale was used. High quality monolayer graphene has been confirmed by Raman

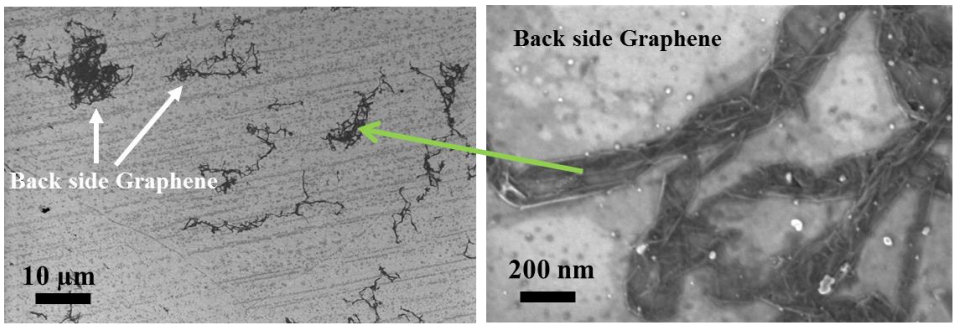
measurements. Note that graphene growth occurs on both sides of the Cu foil.

Step 2: PMMA protection

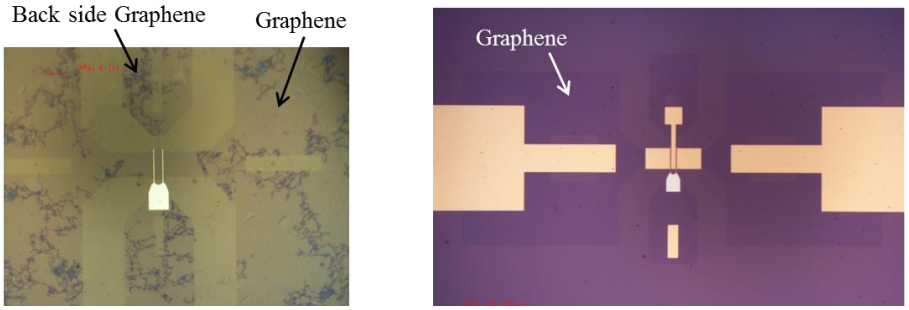
To provide protection and also a mechanical support to graphene, a PMMA layer of 200 nm thickness was spin-coated on top of the graphene/Cu foil as transfer medium. This layer also helps to locate the graphene during the wet process. Afterwards, the PMMA/graphene/Cu sample was baked at 170 ℃ for 10 min and slowly (1 hour) cooled down to room temperature.

Step 3: Back side graphene removing

Because the graphene growth occurs on both sides of the Cu foil, the removal of the graphene on the back side is necessary. If the back side graphene was not removed, it could easily become teared and aggregated after Cu etching, as shown in Figure II-9 (a). Therefore, an oxygen plasma (90s, 50W RF power, 25 sccm at 100 Torr) is used to etch the back side graphene, the efficiency of this process being always confirmed by Raman measurement. In the beginning of my work, this step was neglected, and Figure II-9 (b) compares the graphene morphology after transfer without backside graphene etching (left) and with backside graphene etching (right). Apparently, the graphene appears much more homogeneous after this treatment.



(a)



Without backside graphene etching on Si08

With backside graphene etching on Si10

(b)

Figure II-9: (a) SEM image of graphene after transferring onto Si/SiO2 with backside graphene, (b) Comparison of back side graphene removing treatment: optical images of one device just after process of isolation etching from sample Si08 (on left, without back side etching) and one device just after process of drain & source deposit (on right, with back side etching)

Step 4: Cu wet etching

After backside graphene etching, the next step is Cu substrate etching. There are already various chemical etchant for Cu such as aqueous ammonium persulfate ($(NH_4)_2S_2O_8$), iron nitrate ($Fe(NO_3)_3$), iron chloride ($FeCl_3$), nitric acid (HNO_3), and a mixture of hydrochloric acid/hydrogen peroxide ($HCl+H_2O_2$). Among these candidates, we finally choose $(NH_4)_2S_2O_8$ or $HCL+H_2O_2$ in our work, because other etchants are more likely to introduce metal contaminants due to the incomplete Cu etching [45][46]. The rate of the etching process, which is achieved at room temperature, is controlled by diluting the etchant with DI water. When the etching rate is too high, which occurs when a high etchant concentration is used, the fast etching may lead to gas aggregating beneath the graphene (as shown in Figure II-10). We observed that these gases (bubbles) result in broken graphene with many holes and cracks after transfer. Therefore, the recipe of $HCl/H_2O_2/H_2O$ (1/1/50) and $(NH_4)_2S_2O_8$ 0.5M were finally adopted although the etching time is relatively long. Nevertheless, we believe that enough time for graphene/PMMA floating on the solution may lead to a complete removal of Cu and other ions. Figure II-14 shows a PMMA/graphene sample after Cu etching by $(NH_4)_2S_2O_8$ 0.5M, without bubbles formation. Table II-4 summarizes the bubble size and density for different etching rate. Note that the ratio in each recipe is considered by volume.

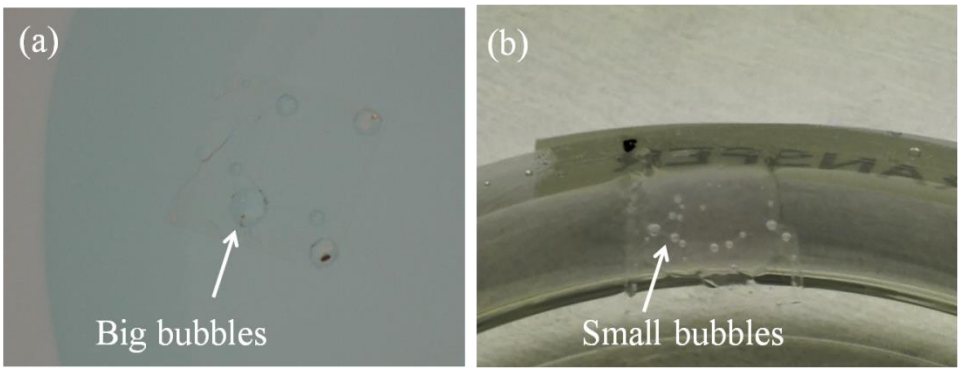


Figure II-10: (a) using $HCl + H_2O_2$ (10/1) with big bubbles observed, (b) using $HCl + H_2O_2+H_2O$ (3/3/20) with many small bubbles observed

Table II-4: Different recipe for Cu etching

HCl	H_2O_2	H_2O	Time	Remarks
10	1	0	5 mins	Big and Many bubbles
4	1	4	10 mins	Big and Many bubbles
5	5	20	<1 h	Small but Many bubbles
3	3	20	<3 h	Small and some bubbles
1	1	20	<5 h	Small and a few bubbles
1	1	40	<8 h	Small and few bubbles
1	1	50	<10 h	Almost no bubbles
	$(NH_4)_2S_2O_8$ 0.5M		<15 h	Almost no bubbles

Step 5: etchant dilution

After Cu etching, the etchant must be removed by DI water dilution as much as possible, because the Al bottom gates could be etched by either HCl or $(NH_4)_2S_2O_8$. Figure II-11 (a) shows one damaged bottom gate. The dilution is carried out by carefully transferring the sample of graphene/PMMA which is always floating on liquid from the original solution to pure DI water. It is preferable to repeat this transfer process for more than 15 times to insure the solution is far less dangerous to the bottom gate. Figure II-11(b) shows an example of a bottom gate which remained intact after transfer thanks to a sufficiently diluted solution.

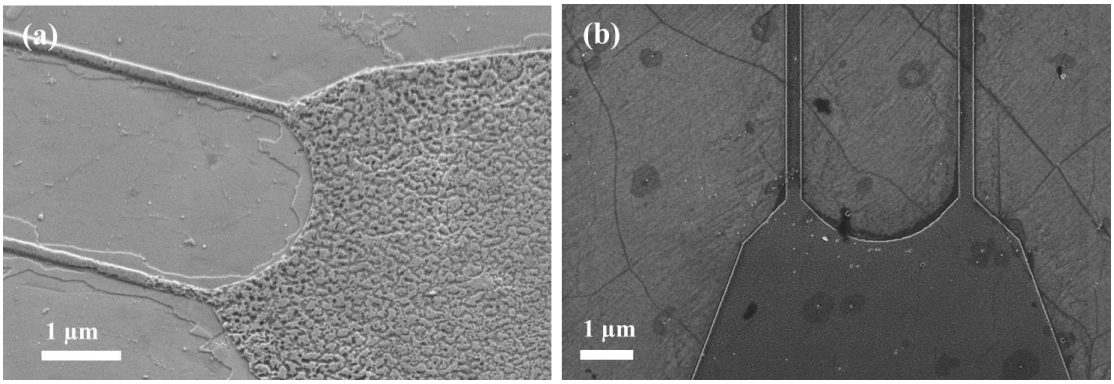


Figure II-11: Bottom gate after graphene transfer (a) without enough dilution transfer, gate are partly etched, (b) with enough dilution transfer, gate remains intact

Step 6: wet transfer

In this step, the target substrate (rigid Si/SiO_2 or flexible Kapton with bottom gates processed) is placed in the water at an inclined angle (as shown in Figure II-21 step6) and the substrate position is adjusted to have PMMA/graphene membrane floating right

above the device area. Then, by keeping the inclined angle and lifting the target substrate, PMMA/graphene is gently transferred onto its surface. Sometimes, tweezers are useful for positioning the membrane exactly on the device area. The substrate is inclined to help the PMMA/graphene membrane spread across the substrate from one side to avoid water being trapped between graphene and substrate, which could result in broken graphene.

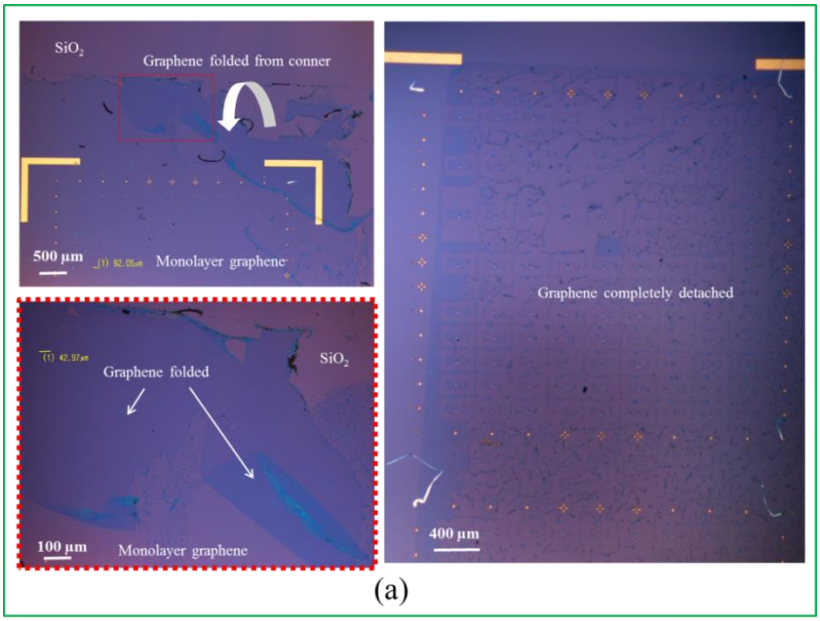


Figure II-12: (a) left, graphene folded due to partial detachment with zoomed-in of red rectangle marked region; right, graphene completely detached (b) graphene transferred onto bottom gates with optimized baking step

Thereafter, a slow baking at 90 ℃ needs to be carried out. The remaining water droplets trapped underneath the graphene will be removed by this baking step, which helps not only to reduce the occurrence of holes and cracks in graphene, but also to increase the adhesion between graphene and target substrate. Deficient baking may lead to a poor graphene/target substrate adhesion which consequently results in graphene delaminating from substrate. Figure II-12 (a) left image shows that the graphene from

the corner part became detached from the substrate, several layers of graphene being formed by folding onto each other. The right image shows graphene completely detached from substrate. Both problems occured during after-transfer processes. Figure II-12 (b) shows bottom gates fully covered by monolayer graphene without any observations of holes, cracks or detachment, thanks to the optimized baking step.

Step 7: UV treatment & Step 8: PMMA removal

It has been reported that PMMA results in P-type doping of graphene[47]and that polymeric residues still remain on graphene surface if only acetone is used as PMMA remover[48]. Several techniques for removing polymeric residues on graphene have been reported, but an easy and efficient process tolerant PMMA removal method is still desired. In this work, we used a deep UV exposure (from a Xe-Hg arc lamp) carried out on the sample prior to dipping it into MIBK for PMMA dissolution. After, the sample was rinsed by first acetone and then isopropyl alcohol. The efficiency of this PMMA removal technique is examined by Raman spectra measurement, as shown in Figure II-13. The PMMA peaks radically disappear after UV exposure- MIBK dissolution-acetone resin treatment, which indicates an efficient PMMA removal. This technique efficiency was further confirmed by X-ray photoelectron spectroscopy (XPS) analysis. Finally, the clean monolayer graphene has been transferred from its host substrate, Cu, to the new target substrate. Figure II-14 illustrates some of the key transfer process from step4 to step8.

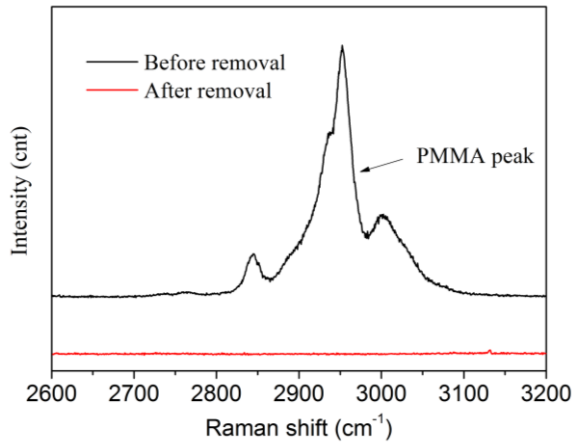


Figure II-13: Raman spectra of PMMA for removal confirmation

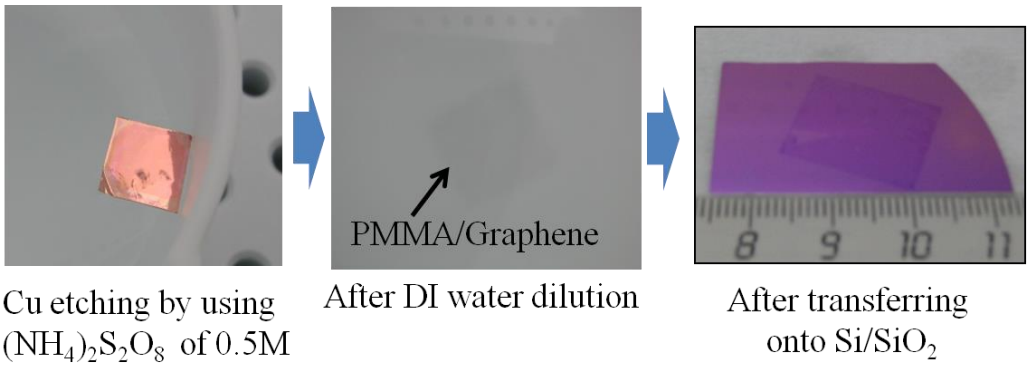


Figure II-14: One successful transfer process from step4 to step8

Transfer results:

In this work, an improved wet transfer process has been developed. The efficiency of our transfer process were confirmed by using optical microscopy, SEM and Raman spectroscopy mapping. Figure II-15(a) shows an optical image of graphene after transfer onto the bottom gate. The transferred graphene has an excellent surface uniformity. Structural defects such as holes, cracks or folds are not observed, which are achieved, we believe, thanks to the optimized transfer process. Moreover, Raman mapping in the region marked by a white dotted rectangle was performed. The Raman mapping, as shown in Figure II-15(b), gives the ratio of the 2D and G peak integrated intensities A_{2D}/A_G. This ratio stands above 2 for 90% of the mapping points, and Raman spectra of three selected points, marked as blue, red and black circles in the mapping region, are given in Figure II-15(c) with A_{2D}/A_G values of 2.8, 2.2 and 0.95, respectively. The A_{2D}/A_G ratio is sensitive to the numbers of graphene layer and also to the presence of charged impurity[49]. The high A_{2D}/A_G ratio (>2) indicates monolayer graphene with quite low charged impurity concentration[49]. The D peak is barely observable, suggesting that a very low density of defects was present in the graphene even after the transfer process. The Raman measurement confirms the highly homogeneous monolayer and defect-free graphene coverage on our samples.

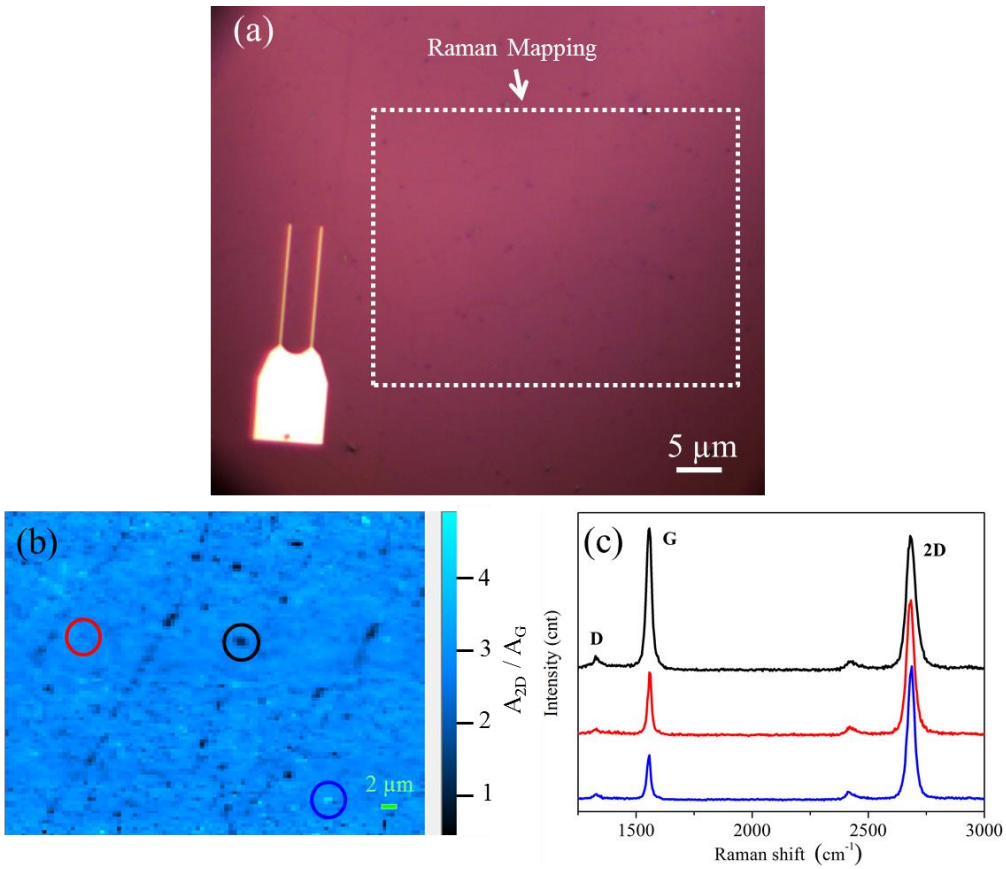


Figure II-15: (a) Optical image of graphene transferred on SiO2/Si substrate with bottom gate using improved transfer process, (b) Integrated intensity ratio of the 2D and G peaks measured by Raman mapping, (c) Normalized Raman spectra at three elected points marked

Furtherly, Figure II-16 shows the SEM image of the graphene morphology before and after transfer onto Si/SiO_2 substrate with bottom gates, using our optimized process. In Figure II-16, no obvious residues or holes are observed, which confirms again the high efficiency of our transfer work.

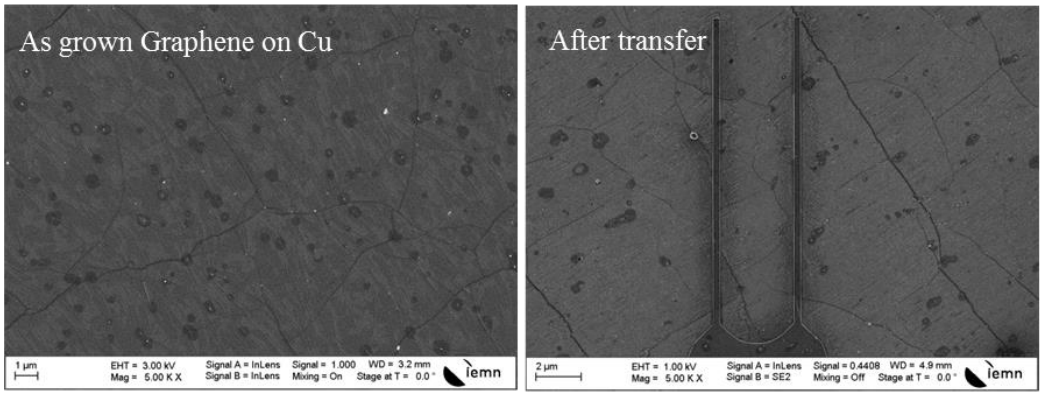


Figure II-16: SEM images of graphene grown on Cu, and after transfer onto the bottom gates

II.3 Process technology for bottom gate GFETs with natural oxide as dielectric

This section will discuss the fabrication process of bottom-gate graphene field effect transistors (GFETs) based on CVD grown graphene. Figure II-17 shows the three dimensional imaginary image of the GFET in this work. Before device fabrication, substrate selection and preparation need to be considered. For devices applied for high frequency, the substrate needs to be highly isolated, to prevent either the leakage current in DC regime or signal loss in RF regime. Because of this, commercial silicon wafer with resistivity higher than 5000 Ω•cm was selected, and then around 300 nm SiO_2 was obtained by thermal growth on the surface of silicon.

The objective of developing this fabrication process is to make it compatible with different substrates, especially with flexible substrate. For example, when the ambient temperature is higher than 200 ℃ for PEN and 300 ℃ for KAPTON, the phenomenon of shrinkage for both substrates becomes very predominant (>0.5%). For this reason, high temperature process (>200 ℃) need to be avoid by using alternative method, such as the dielectrics, between gates and channel material of graphene. The dielectric is formed by natural oxidation at room temperature rather than by using atom layer deposit method which may be operated at temperature higher than 300 ℃. The bottom-gates structures with its natural oxide as dielectric differs this work from all the other previous reports about GFETs.

In following, this section will start by the work of device design in layout software. Following that are some details of electron-beam lithography, which is the crucial part almost used in each step. And after, the device fabrication process with several steps will be discussed in detail.

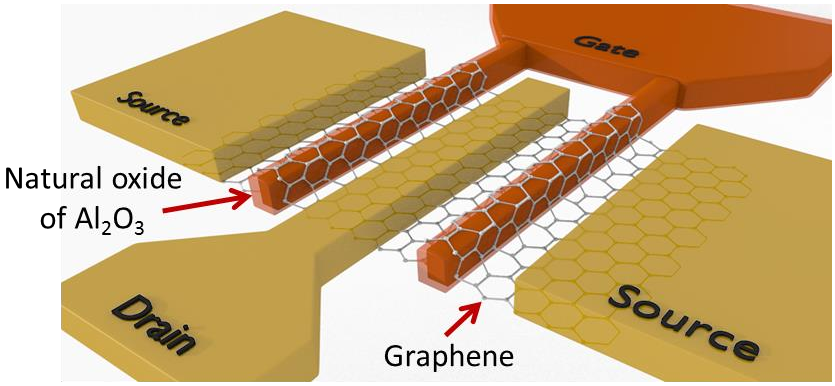


Figure II-17: Three dimensional illustration of the GFET structure in this work

II.3.1 Layout design

The geometry of device with different dimensions and also other structures such as alignment marker, Hall effect and TLM structures have been all designed by layout prior to any real fabrication step. The layout design for sample Si08 is shown in Figure II-18 (a) and (b) shows the optical image of final devices and other structures according to this design; (c) shows an overview of the whole chip of Si08.

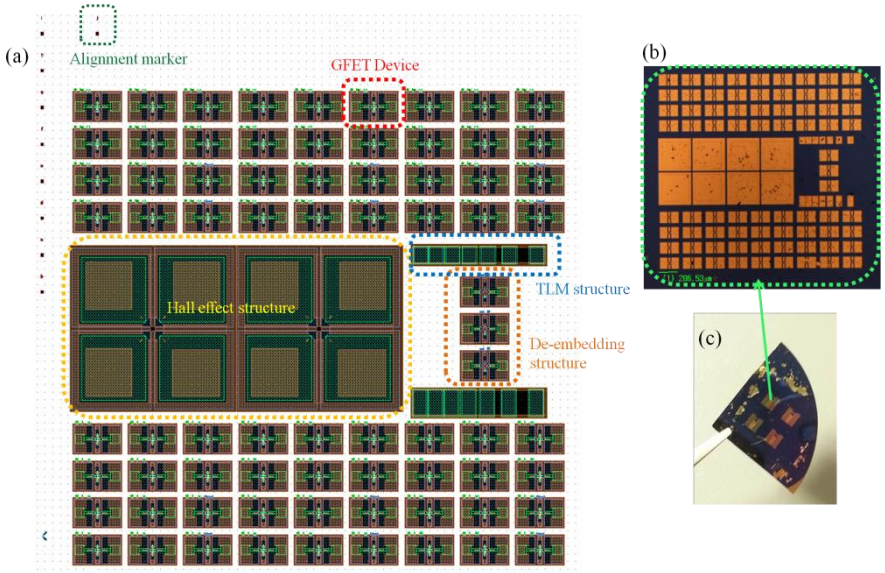


Figure II-18: (a) pattern design of transistors with all the other structures in layout; (b) optical image of a final completed structures according to the design; (c) an overview of the chip Si08

II.3.2 Electron-Beam lithography

Electron-Beam lithography (EBL) is the crucial technology in nano-devices fabrication. It is mask-free (as shown in Figure II-19) and has high resolution (sub-10 nm) due to the much smaller wavelength of electron comparing to photon for photolithography. The pattern realization starts by scanning a focused beam of electrons on resist to change its solubility. The trace of the scanning is defined by pattern design in software such as layout. The solubility difference between electrons exposed and non-exposed regions enables a selective removal of resist by immersing the sample in a solvent, which is referred as developing process.

In this work, the device patterns (transistors, Hall effect and TLM structures) have been pre-designed in layout as mentioned in previous section. Two-layer electron sensitive resist, COPO/PMMA (copolymere/polymethyl-methacrylate, positive electronic resist) were used to form lift-off structure which may ease the lift-off process.

The resist thickness is defined by the speed of spin-coating, and should be proportional to the metal deposition thickness, i.e.normally 1.5 times higher. Otherwise the lift-off process would be difficult. Table II-5 gives details for each step. For the process of developing after electron beam exposure, a mixture of MIBK and IPA (1:2 by volume) was used to remove the resist exposed by electrons.

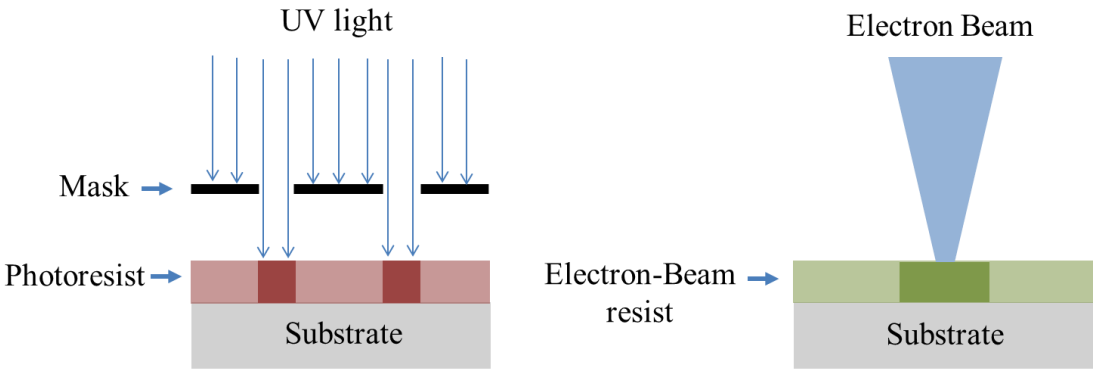


Figure II-19: Simple schematic of photolithography (left) and electron-beam lithography (right).

During the process of EBL, most electrons (the forward scattered electron) have elastic collisions with atoms of resist and substrate, the energy loss is low so that these electrons are able to reach deeply into the substrate. However, besides these forward scattered electrons, there are some other electrons referred as back scattered electrons. Instead of going forward down to the substrate, the back scattered electrons will be strongly deflected to any direction even back to surface due to the non-elastic collisions where the energy loss is not negligible. The back scattered electrons are the killer of the writing resolution since they have enough energy to affect the resist around the exposure region. One solution to reduce the impact of back scattered electrons is to deposit a conductive layer on resist for evacuating these electrons promptly. Nevertheless, if the substrate has some certain conductivity, this conductive layer can be negligible. In this work, the devices fabricated on rigid substrate (SiO_2/Si) are not always necessary to deposit conductive layer before electron beam exposure. However, for flexible substrate such as kapton, it is obliged to deposit this conductive layer each time before EBL, and here 5 nm of Ge was always used due to the fast removal method of Ge (several seconds in H_2O_2).

With a fixed given power to electrons, here is 100 keV, dose is the most decisive parameter which will result in the EBL resolution. The term of dose reflects the number of electrons received per unit area, expressed as $\mu C/cm^2$. Additional to dose, parameter of current will determine the whole exposure time and slightly affect the resolution. Figure II-20 gives two groups of examples with comparison of using wrong and correct dose. Table II-5 gives the optimized EBL parameters used for each step. The following

paragraph will provide details of those each step.

Table II-5: Parameters of EBL used in each step

Steps	PMMA / COPO Thickness (nm)	Ge Deposit 5 nm	Dose ($\mu C/cm^2$)	Current (pA)	Exposure time (min)	Metalization (nm)
Step1: Alignment Marker	70/560	No	370	20000	~ 5	Ni/Au (50/150)
Step2: Bottom-gate	160/170	Yes	350	12000	~ 15	Al (40)
Step5: Graphene Isolated pattern etching	70/450	No	350	25000	~ 40	-
Step6: Drain & Source Deposit	70/450	No	350	20000	~ 20	Ni/Au (20/30)
Step7: Pads Deposit	70/600	No	370	25000	~ 50	Ni/Au (50/300)

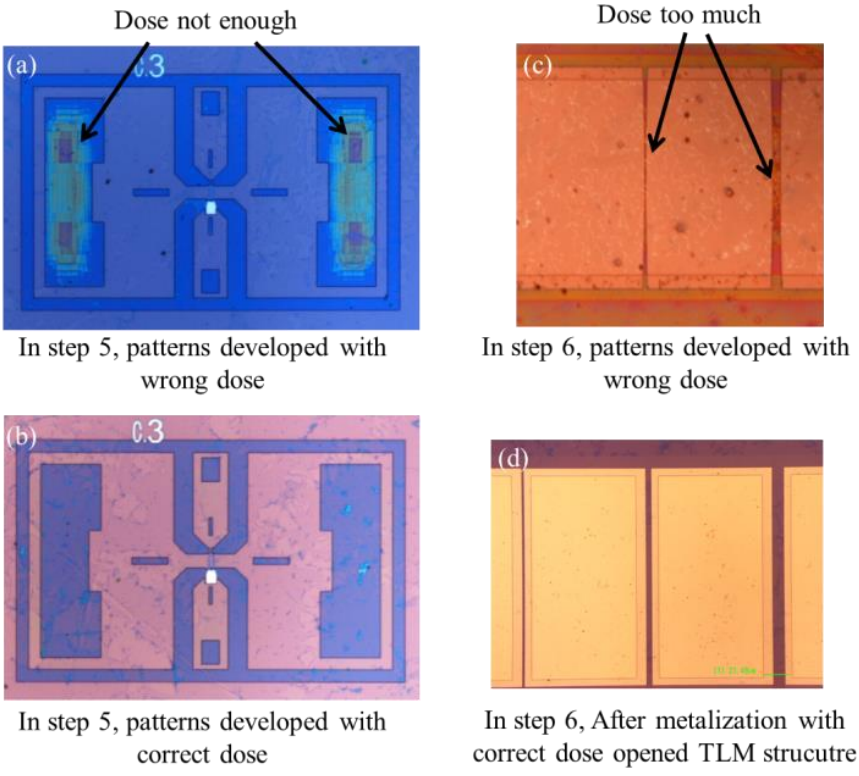


Figure II-20: Examples of different pattern profile with correct and wrong dose

II.3.3 GFET fabrication process

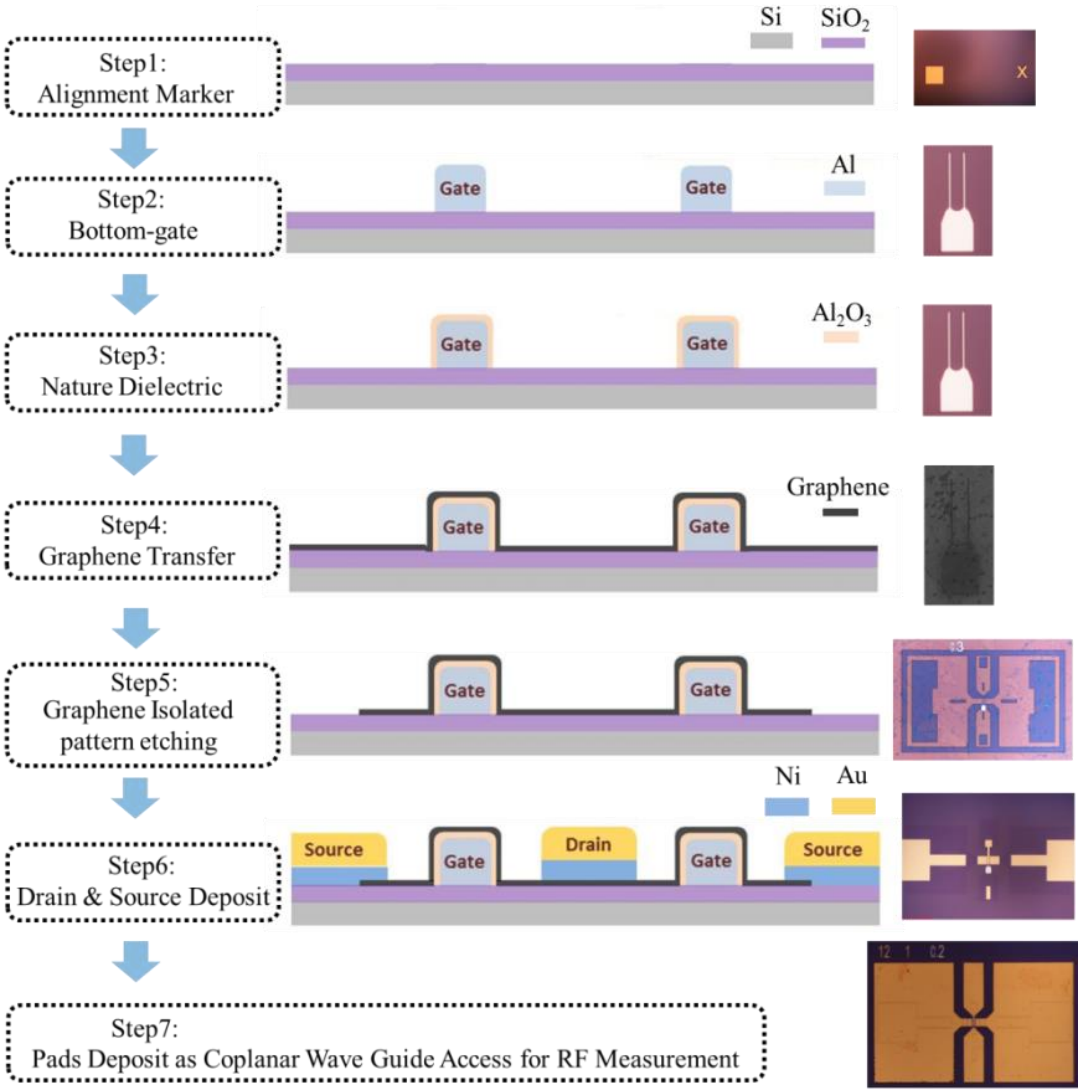


Figure II-21: General device fabrication process for GFETs on rigid substrate

A general description of the whole device fabrication process is provided (see Figure II-21). Following by this part, details of each important subsidiary process will be discussed. Table II-6 shows the main techniques used for each subsidiary process.

Table II-6: Fabrication method used for each step

Steps	E-Beam lithography	Metallization	Etching	
			Graphene	Al_2O_3
Step 1	●	●	○	○
Step 2	●	●	○	○
Step 3	○	○	○	○
Step 4	○	○	●	○
Step 5	●	○	●	○
Step 6	●	●	○	○
Step 7	●	●	○	●

● used ○ not-used

Step1: Alignment Marker

Alignment marker is a crucial element for electron beam lithography (or optical lithography) based fabrication process, because a multilevel writing mask requires perfectly realign with each new step. The aligning procedure is automatically realized by e-beam lithography system, and according to the equipment of IEMN, typically the markers being metal squares with side of 8 or 20 µm and thicker than 200 nm is preferable.

In this work, the dimensions (squared shape with side length of 20 µm) of the markers have been precisely patterned by e-beam lithography, and the final markers were obtained by Ni/Au (50/150 nm in thickness) deposition (metal thermal evaporation) and lift-off process (in Acetone at room temperature). The Ni is used here to strength the adhesion between Au and substrate, since Au has very poor bonding strength with SiO_2. Figure II-22 (a) and (b) shows the alignment marker designed in layout and Figure II-22 (c) shows an optical image of one marker from sample Si10.

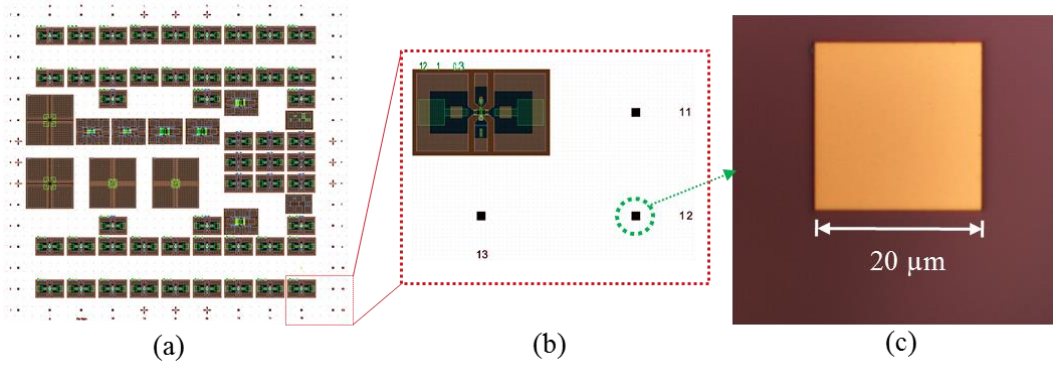


Figure II-22: Illustration of alignment marker (a) and (b) layout design, (c) optical image of alignment marker obtained on Si/SiO_2

Step2: Bottom Gates

For bottom gates, 40 nm Al was selected to deposit. Because in air Al can easily form a layer of Al_2O_3 with high density on its surface due to a self-limit oxidation. We take this advantage to form the dielectric in our GFETs. The thickness of bottom gate can't be too large or too small. If the thickness is too large, the graphene layer might be easily damaged after transferred above gates due to the stress. If the thickness is too small, the gate resistance will increase rapidly and consequently the RF performance such as f_{max} suffers decreasing.

The bottom gates with different geometry design (gate length L_g= 100, 200, and 300 nm; gate width W= 12, 24, 50 µm) were precisely patterned by e-beam lithography and then finished by 40 nm Al metallization and lift-off process (in Acetone @ room temperature). Figure II-23 (a) shows the optical images of 300 nm gate length with different gate width W from sample Si10. Figure II-23 (b) shows examples of SEM images of the bottom gate with different gate length L_g.

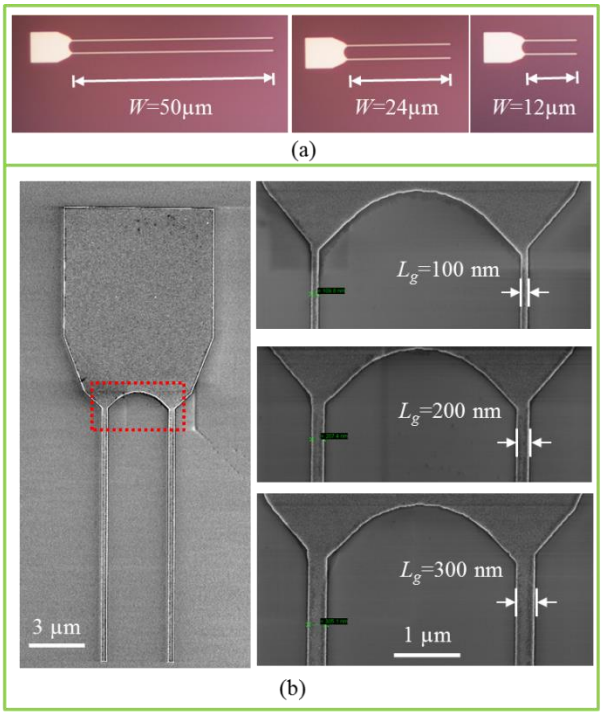


Figure II-23: Illustration of bottom gate geometry (a) with different gate width *W*, (b) with different gate length *Lg*

Step3: Natural Dielectric

The nature dielectric of Al_2O_3 was obtained by exposing the substrates with bottom-gate structure to the air for more than 24 hours. The thickness of Al_2O_3 formed by this natural oxidation process was confirmed to be 4.3 nm by spectroscopic ellipsometer. This thickness value is obtained by parameters fitting, as shown in the following Figure II-24. Note that Ψ and Δ describe the change in polarization that

occurs when the measurement beam interacts with a sample surface causing a change in the outgoing polarization. So the best fit has been found for a Al_2O_3 thickness of 4.3 nm.

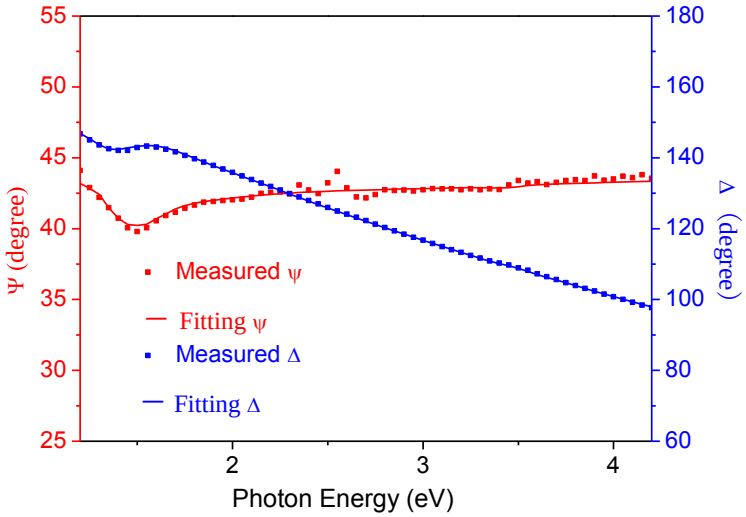


Figure II-24: Ellipsometer measurement and data fitting for Al_2O_3 thickness

This natural oxidation process avoids high temperature deposition of dielectric layer, which is compatible with the GFET fabrication process on various flexible substrates. This technique has been already used in fabrication of GFET with top-gate structure[50-52]. In our work, bottom-gate structure is used in order to further reduce the possibilities of degrading graphene mobility due to electron irradiation which could happen in directly e-beam writing on the top of graphene channel[53].

Step4: Graphene Transfer

In this work, graphene grown by CVD on copper foil was used. A wet chemical transfer process has been developed to transfer monolayer graphene from host substrates to various target substrates. The details of graphene transfer process has been provided in section of graphene transfer. Figure II-25 shows an optical image taken after graphene transfer process on sample Si10. This image was randomly taken from a small part of the whole chip, and where we can find bottom gates with gate width of 50 µm and gate length of 0.1 µm (marked by green circle) and 0.2 µm (marked by red rectangle). All the gates have been well covered by graphene and a graphene crack observed in the image helps us distinguish the contrast between substrate and graphene.

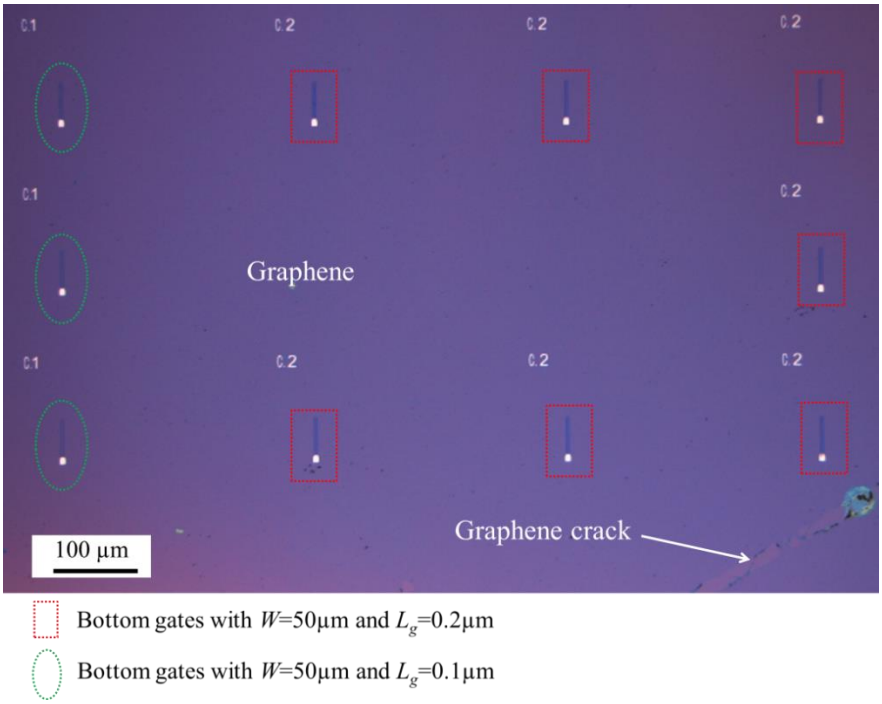


Figure II-25: Overview of bottom gates with graphene transferred

Step5: Graphene Isolated pattern etching

After graphene transferred onto substrate with bottom gates, graphene etching process is followed to obtain isolated patterns. Oxygen plasma is an effective and inexpensive method which has been widely used to clean the substrate and also to etch organic materials, such as carbon nanotube or graphene. The high activity of O +ions makes the oxidation of carbon possible and thus the C-C bond would be broken with production of CO and CO_2. These newly generated gases would be eliminated by a pumping system. The optimized etching parameter (50w, 25sccm, 100 mTorr and 2min) will etch at least 2 layers of graphene. Figure II-26 (a) shows an graphene isolated patterns (for Hall effect pattern) after O_2 plasma etching. Accordingly, an Raman spectroscopy mapping (see Figure II-26(b)) has been explored on this pattern. Three points, marked as blue, red and black, have the spectroscopy shown in Figure II-26 (c). One can see that in graphene region, the signal of G and 2D peak are very strong. The high A_{2D}/A_G ratio (>2) and very low D peak indicate the existence of monolayer graphene with quite low charged impurity concentration and low defects density[49]. So graphene quality is not degraded during the O_2 plasma etching. In the red point, i.e.graphene etching region, all the graphene feature peaks disappear, which indicates that the graphene layer has been efficiently etched.

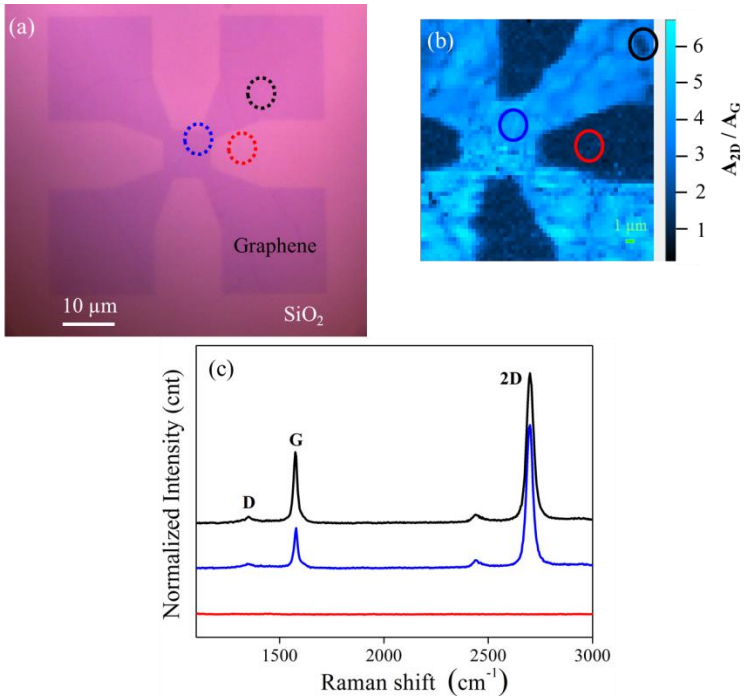


Figure II-26: (a) optical image a graphene pattern for Hall effect structure; (b) the according Raman mapping; (c) Normalized Raman spectra at three elected points marked in (b)

Step6: Drain & Source Deposit

Drain and source contacts have been defined by depositing Ni/Au (20/30nm thickness) followed by a lift-off process. The drain source distance L_{ds} is mainly defined as 1 µm to make our process tolerant to the misalignment induced by electron beam lithography, which is a problem in the fabrication process on flexible substrates. Nevertheless, the L_{ds} of some transistors has been designed to be 0.7 µm only on rigid substrate for RF performance comparison. To decrease the value of L_{ds} for further device optimization will be our future work. Figure II-27 shows an overview optical image of devices with drain and source contacts. Note that both Figure II-25 and Figure II-27 are showing the same devices in the same region of Si10 substrate. Figure II-28 shows one transistor (50 µm gate width) with drain source illustrated.

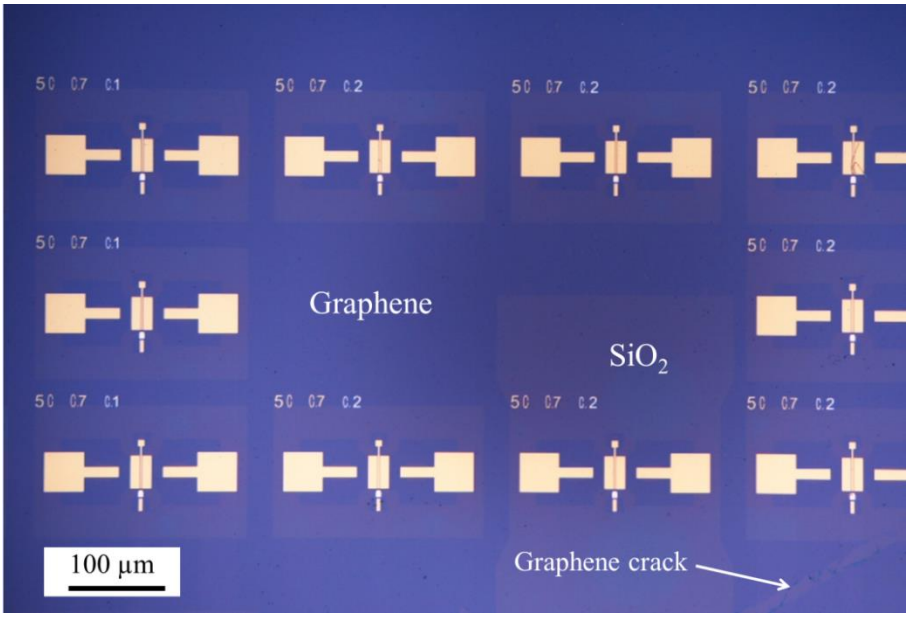


Figure II-27: Overview of devices with drain and source deposited.

For drain and source, the purpose is to form ohmic contact between graphene and electrode with contact resistance as low as possible. Metals of Cr, Ni and Au with different combination have been studied, contact resistance in the range of 200~3000+ Ω·µm are found in this study and section for contact resistance provides more details. Regardless of the metal choice, the total thickness is controlled as 50 nm. If the thickness is small, the contact resistance would increase accordingly; if the thickness is large, the capacitance between drain, gate and source would increase as well. For both two cases, the RF performance would reduce.

There is another reason for Ni and Au used here, i.e. their excellent chemical stability. Comparing to other metals such as Ti or Pd, they have good resistance to chemical attack of acid, such as hydrofluoric acid which is used in dielectric wet etching.

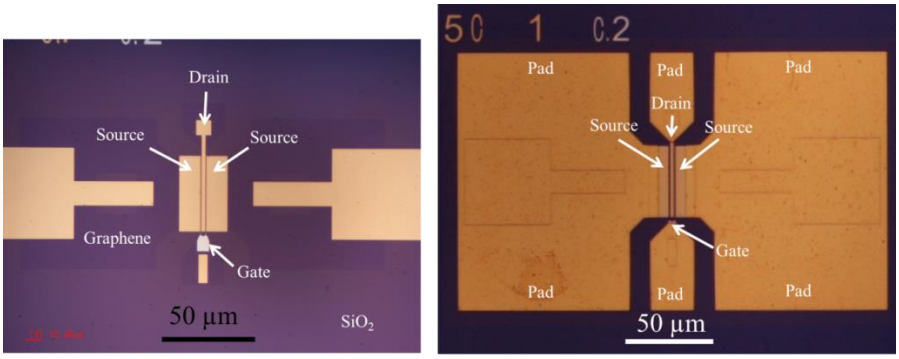


Figure II-28: Optical image of (a) device with drain source deposited, (b) device with pads completed

Step7: Pads Deposit as Coplanar Wave Guide Access for RF Measurement

In order to make our devices compatible with on-chip probe measurements, the device fabrication were finished by depositing Ni/Au (50/300 nm in thickness) for gate, source and drain pads (coplanar wave guide access). The total thickness of 350 nm satisfies well the on-chip probe measurement. A typical GFET device with 24 µm gate width is shown in Figure II-29, illustration of pads in (a) and details of active region in (b).

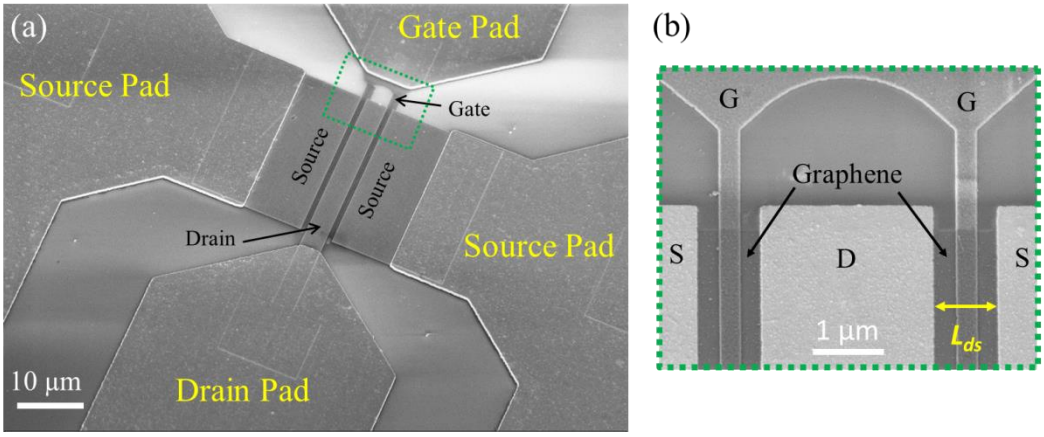


Figure II-29: SEM image of (a) one GFET with pads finished (b) zoomed-in of the rectangle marked region in (a)

In this last process, one challenge is to realize metal contact between gate and gate-pad by removing the layer of natural oxidation of Al_2O_3. The contacting area between gate and pad is clearly presented in Figure II-30 . Here, the thickness of this layer oxide is 4.3 nm which is obtained by Al nature oxidation. A wet chemical etching method was used in this work, with a solution of hydrofluoric acid buffer (BOE 1:7) diluted 20 times by DI water. The etching time was optimized as 30 second.

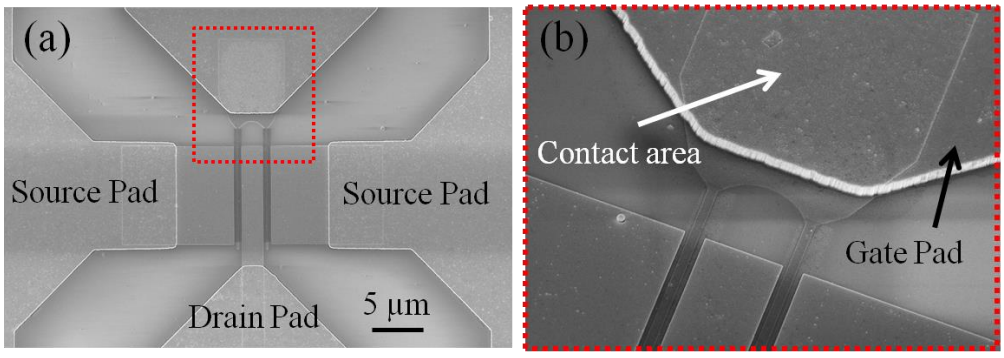


Figure II-30: SEM image of final device with illustration of gate and gate pad contact area in (a) the rectangle marked area and (b) a further zoomed-in

After all these device fabrication process, the graphene quality was verified by Raman measurement. Figure II-31 (a) shows the optical image which has a marked area

for Raman spectroscopy mapping. From optical image, graphene presents a good uniformity without observation of structures defects such as cracks or folds. The uniformity is further confirmed by Raman mapping. In Figure II-31 (b), the ratio of 2D and G peak integrated intensities A_{2D}/A_G standing above 2 of 90% of the mapping region. Three selected points marked as blue, red and black circles in the mapping region, give the A_{2D}/A_G values of 5, 3.8 and 1.7 respectively. The A_{2D}/A_G ratio is sensitive to the numbers of graphene layer and also the presence of charged impurity[49]. The high A_{2D}/A_G ratio (>2) indicates monolayer graphene with quite low charged impurity concentration[49]. The D peak is barely observable, suggesting that very low density of defects were deduced after device fabrication process. The Raman measurement confirms that highly homogeneous monolayer and defects free graphene after all the fabrication process.

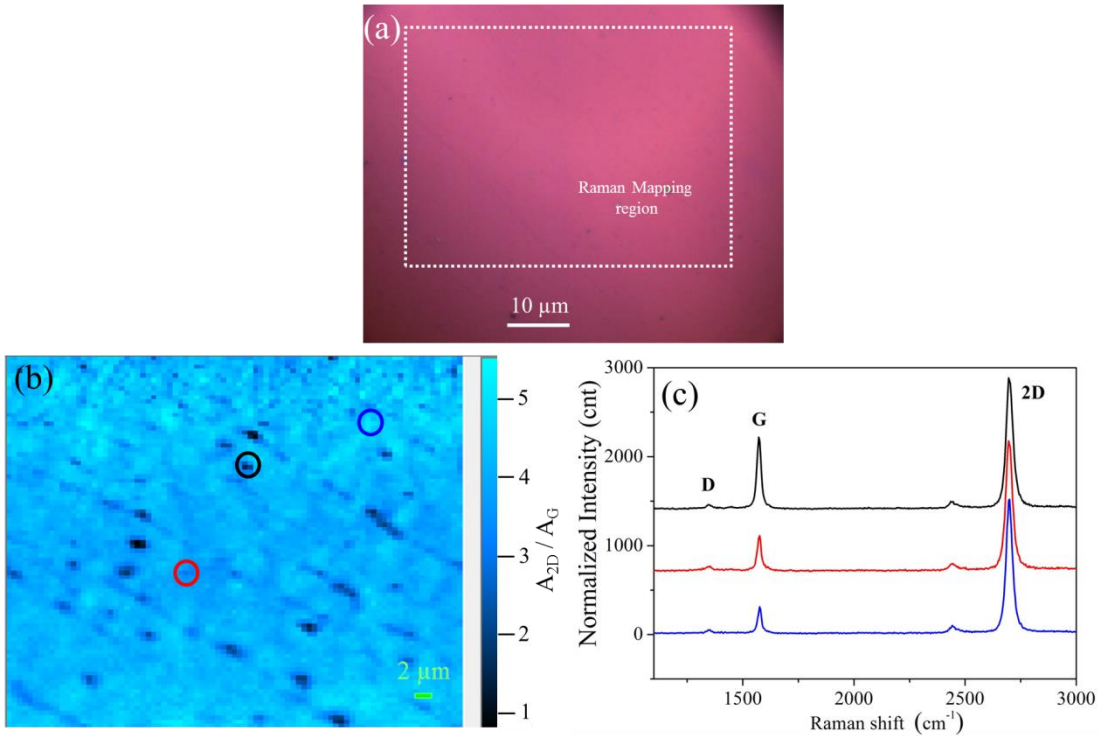


Figure II-31: (a) Optical image of graphene transferred on SiO2/Si substrate after all device fabrication process (b) Integrated intensity ratio of the 2D and G peaks measured by Raman mapping, (c) Normalized Raman spectra at three elected points marked in (b)

Final device images

Figure II-32 upper part shows optical images of complete devices with different gate width *W* and Figure II-32 below part shows the according zoomed-in SEM images of the channel region. Figure II-33 shows the complete devices with different gate length L_g. From both Figure II-32 and Figure II-33, the gates are found well covered by

monolayer graphene. The patterns obtained with well-defined dimensions indicates that the GFETs geometry designed in this work are fully achievable by our fabrication process, even for the case of 100 nm short gate length with gate width up to 50 µm. Additionally, very few contaminations, defects of devices and graphene such as cracks or holes could be observed, which all proves a reproducible, reliable and contamination-free fabrication process for bottom-gate GFETs with CVD transferred graphene.

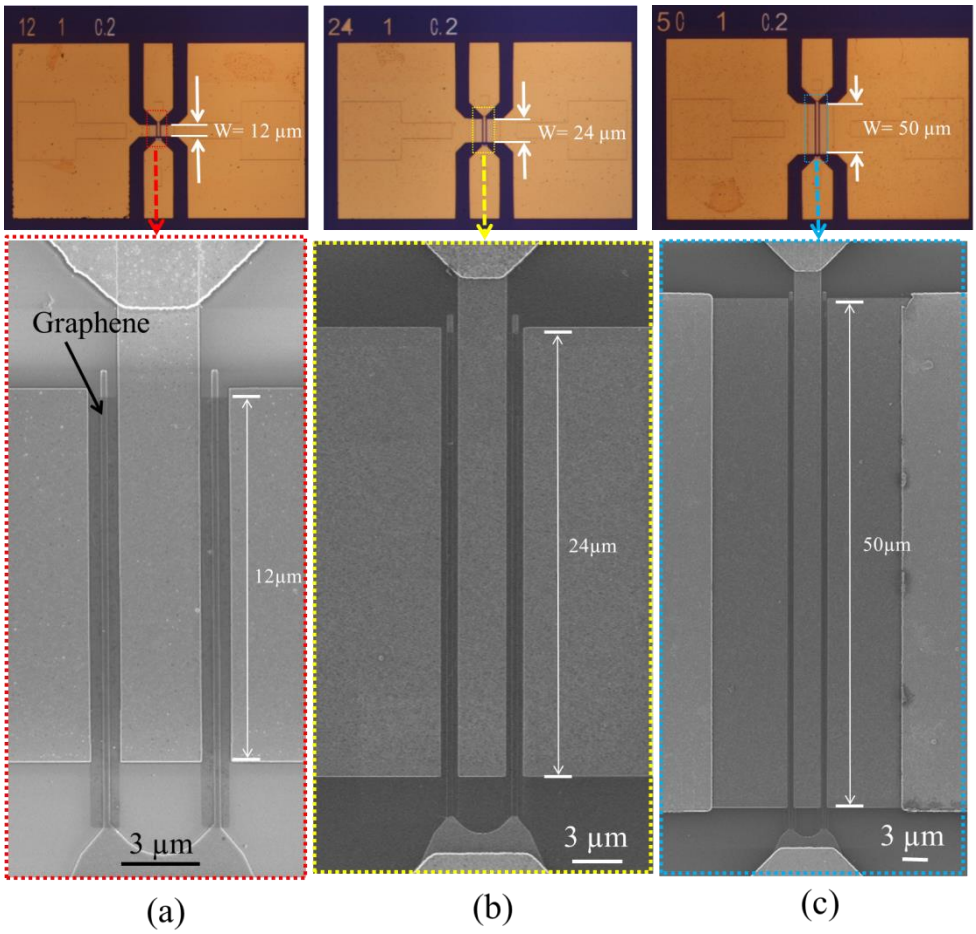


Figure II-32: complete devices with gate width of 12 µm in (a), 24 µm in (b) and 50 µm in (c).

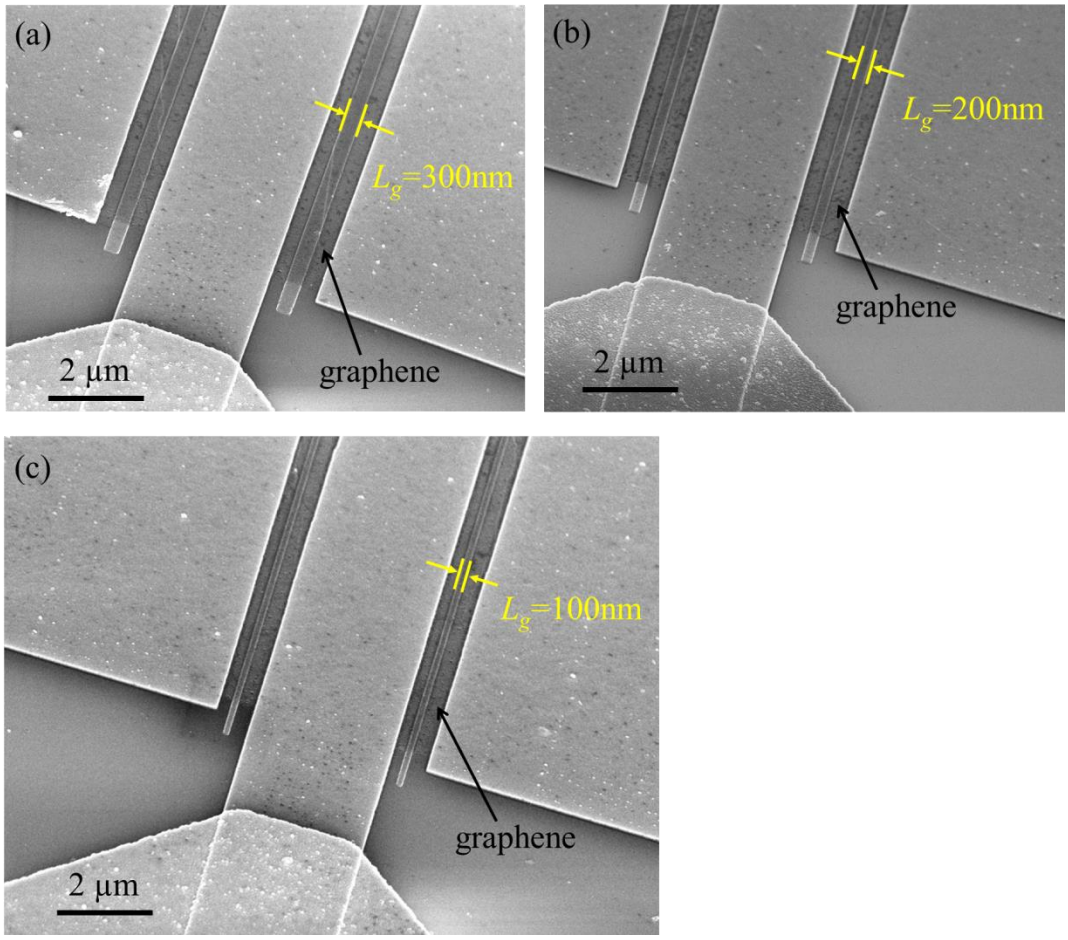


Figure II-33: complete devices with gate length of 300 nm in (a), 200 nm in (b) and 100 nm in (c).

II.4 Physical and electrical characterization

The study of characterization will firstly start by graphene mobility and device contact resistance extraction. Because these two information is important to understand the device performance in both DC and RF regime.

II.4.1 Graphene mobility

In response to an electric field, mobility describes the ability of charge (electron or hole) moving through a medium, given by formula $\mu = \frac{V_d}{E}$, where μ is the mobility, E is the electric field, and V_d is the drift velocity. Practically, the mobility of a certain material can be measured by Hall Effect measurement. As mentioned above, high mobility is one outstanding property of graphene, and therefore we start by mobility extraction based on our transferred graphene.

II.4.1.1 Method illustration

(1) Hall effect

As shown in Figure II-34, in a two-dimensional material with rectangle shape, a magnetic field applied (z-direction) which is perpendicular to the current flow (x-direction) through the material will cause the carriers affected by magnetic force, referring as Lorentz force. If considering that a carrier with charge q moves with velocity v in the presence of an electric field E in conjunction with a magnetic field B, the Lorentz force will be defined as: $F = q[E + (v \times B)]$. As a result, described in Figure II-34, carriers will change their original motion direction (x-direction) and begin to accumulate on the two sides of this material (y-direction). Note that holes and electrons will experience the opposite Lorentz force and thus a separation is found on the two sides. This new charge distribution then results in an establishment of a transverse voltage, V_H, and this measureable value can be expressed as: $V_H = \frac{IB}{nq}$. Where I is the current applied, B is the magnetic field; q is carrier charge; n is carrier density

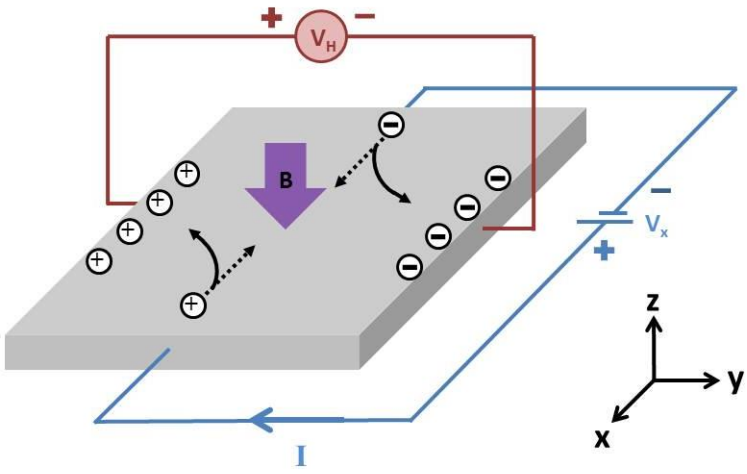


Figure II-34: Schematic of Hall effect measurement

(2) Van der Pauw

The technique of Van der pauw method is capable of implementing resistivity measurement (sheet resistance, Rs) and Hall Effect measurement for especially two-dimensional materials. Firstly, as shown in Figure II-35 (a), a current source is applied to contacts 2,3 (I_{23}) and the voltage measured across contacts 1,4 (V_{14}). From these two value, a resistance named as $R_{23,14}$ can be found as $R_{23,14} = \frac{V_{14}}{I_{23}}$. In the same way, by making an additional reciprocal measurement, i.e. current flow through contacts 1,4 and voltage is measured from contacts 2 and 3, another resistance named as $R_{14,23}$ can be obtained. Here, we find an average value defined as vertical resistance: $R_{vertical} = \frac{R_{23,14}+R_{14,23}}{2}$. Next, as shown in Figure II-35 (b), a current source (I_{12}) is applied to contacts 1,2 and voltage (V_{34}) is measured from contacts 3 and 4. After, the same reciprocal measurement as mentioned above is carried out and an average resistance named as $R_{horizontal}$ is obtained from: $R_{horizontal} = \frac{R_{12,34}+R_{34,12}}{2}$. Then, the sheet resistance (R_s) is related to the measured resistances $R_{vertical}$ and $R_{horizontal}$ by Van der Pauw formula:

$$e^{-\pi\frac{R_{vertical}}{R_S}} + e^{-\pi\frac{R_{horizontal}}{R_S}} = 1 \quad \text{(II-3)}$$

If considering the two-dimensional material with squared pattern is symmetrical and free of defects (holes, cracks etc.), then $R_{vertical} = R_{horizontal} = R$ and $R_s = \frac{\pi R}{\ln 2}$.

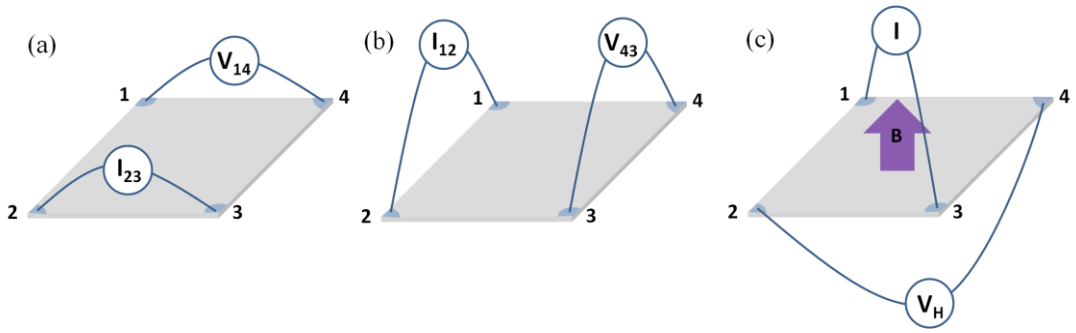


Figure II-35: Schematic of Van der Pauw method

For Hall Effect measurement, as shown in Figure II-35 (c), a magnetic field *B* perpendicular to sample plane is applied while there is a current flow *I* between contacts 1 and 3. By measuring the voltage V_H across contacts 2 and 4, and a further calculation combining sheet resistance R_s and carrier charge *q*, sheet carrier density (n_s) and Hall mobility (μ_H) will be obtained by equation II-4:

$$n_s = \frac{IB}{qV_H},\ \mu_H = \frac{V_H}{R_S IB} = \frac{1}{R_S q n_s} \qquad \text{(II-4)}$$

(3) Hall bar

Similar to Van der Pauw, technique of Hall bar is another approach for resistivity and Hall effect measurement, but it is more suitable for material with high orientation. Firstly, material should be symmetrically patterned as what illustrated in Figure II-36. Shown in Figure II-36 (a), the contacts 5 and 6 are only applied a current source (*I*) while measuring the voltage between contacts 1,4 and also contacts 2,3. Then the sheet resistivity Rs could be obtained by calculation: $R_s = \frac{VW}{IL}$, where V is the average value of V_{14} and V_{23} ,W is the pattern width and L is the length between contacts 1 and 4.

For Hall effect measurement, the principle of Hall bar is identical to Van der Pauw. As shown in Figure II-36 (b), because of the asymmetrical structure, the current is only applied to contacts 5,6 and Hall voltage V_H is measured across contacts 1,2 and 4,3 (the average of these two) with the presence of a magnetic field (perpendicular direction to the pattern plane). The same case as Van der Pauw, sheet carrier density (n_s) and Hall mobility (μ_H) could be obtained by equation II-4.

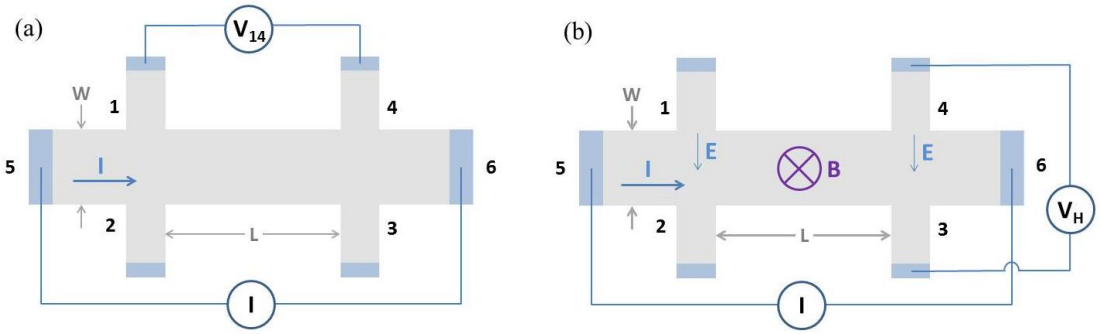


Figure II-36 Schematic of Hall bar

II.4.1.2 Results

In our study, HL5500PC is used to carry out the sheet resistivity and Hall effect measurement for CVD graphene transferred onto both Si/SiO_2 and Kapton substrates, as shown in Figure II-37. Structures of Van der Pauw, with square side of both 15 µm and 30 µm, and structures of Hall bar have been fabricated (Figure II-37) and measured. Table II-7 presents the measurement results for different samples with different structures. Note that all the Hall measurement values presented in Table II-7, are based on measurements with symmetry factor Q < 1.5, indicating that these measurement results are reliable enough.

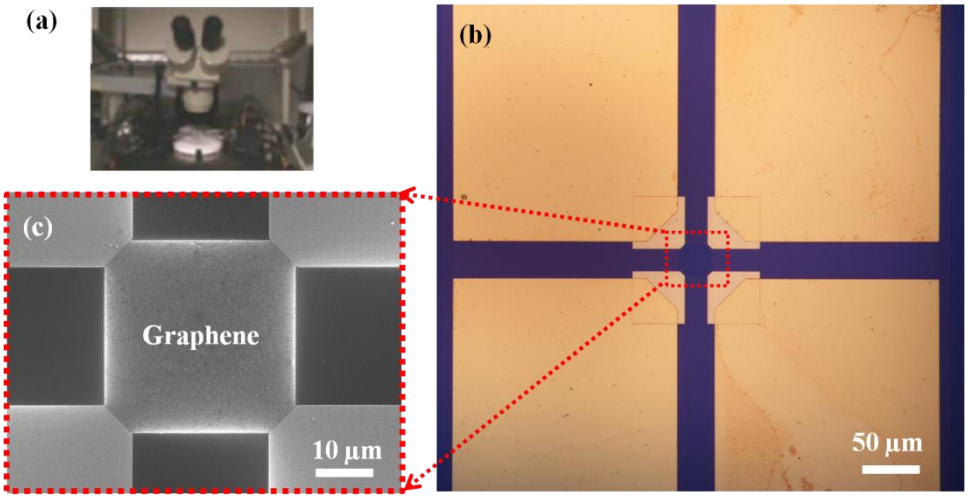


Figure II-37 (a) HL5500PC measurement platform, (b) optical image of a Van der Pauw pattern, (c) SEM image of the graphene sample with Van der Pauw pattern contacts

Table II-7 Information obtained from Hall effect measurement

Sample (Graphene source)	Substrate	Hall structure	Sheet resistance (ohm/sq)	Doping type & Carrier density (cm^{-2})	Hall Mobility (cm^2/Vs)
Si07 (Cambridge)	Si/SiO_2	VDP HB	900	4.3×10^{12}	1900
Si08 (IEMN)	Si/SiO_2	VDP	1500	1.3×10^{12}	3200
Si09 (Korea)	Si/SiO_2	VDP	1600	1.2×10^{12}	3400
Si10 (IEMN)	Si/SiO_2	VDP	1000	2.6×10^{12}	2800

VDP: Van der Pauw; HB: Hall bar

In Table II-7, the variation of mobility for different samples could be ascribed to several reasons. For example: graphene quality (defects of cracks or holes etc) after transfer technique; residuals of eb-resist (PMMA) after device fabrication process; or the different substrates. In this work, four samples with rigid substrate (Si07, Si08, Si09 and Si10) and one sample with flexible substrate have been completed. More details of these samples will be provided in appendix III.

II.4.2 Graphene contact resistance

II.4.2.1 Contact resistance reported in literature

In general, contact resistance is the resistance to current flow in the interface between two different contacting materials. It can be determined by the work function of these two materials, surface conditions and contact area, etc.[54-56] In graphene-based devices, the resistance of metal-graphene interface is referred as *contact resistance*.

Importantly, in GFET devices, the contact resistance is a major issue to be considered. Because the contacts in device must be able to supply the sufficient current, which means the voltage drop across the contacts should be as small as possible comparing to the voltage drop across the active regions, especially when the graphene channel has been designed to be very short(few hundreds nanometers) in nowadays. Furtherly, the high mobility nature of graphene would be obscured if the contact resistance is high[57]. Thus, contact resistance has become one major limiting factor for the device electrical performances, such as on/off current ratio, cutoff frequency and

maximum oscillation frequency [54][58]. However, to obtain low contact resistance is always a challenge due to the small density of states (DOS) of graphene in its Dirac point[57]. To date, various metal-graphene contact resistance have been reported concerning different metal materials, such as. Ni, Au, Cr, Pd, Ti, Cu, and Ag, and some special treatments which are all shown in Table II-8, such as oxygen plasma or ultraviolet ozone treatment[59], rapid thermal annealing[55] and graphene contact area patterning[60]. Many outstanding results have been achieved. For example, ref[60] has reported R_C of 150 Ω·μm from Cr/Pd/Au thanks to edge-contact pattern design; in ref[55],it has been found that there is a significant improvement of R_C if the rapid thermal treatment is applied; and ref[57] has reported *Rc* less than 100 Ω·μm for Pd with 50V back-gate voltage, since R_C is gate-voltage dependent. Note that for fair comparison, all the results presented in Table II-8 are based on the conditions of monolayer graphene, room temperature measurement and gate voltage at zero volt since Rc might be dependent of graphene layers, ambient temperature and gate voltage.

Here, regarding to obtain good graphene contact resistance, we can draw some main conclusions from previous reports: (1) a clean interface beneath contacts on graphene, which means a residues free process is required, (2) high quality graphene is needed to have sufficiently long carrier mean-free-path, (3) metal roughness control of graphene-metal interface is important, which means that probably post-annealing is preferable and metal evaporation is prior to sputtering, and (4) the metals with high work function might be preferable [61] although some other groups have reported the independence of Rc on work function of metals.

In this work, based on transferred CVD grown graphene on both rigid substrate (Si/SiO_2) and flexible substrate (see more details in chapter 3), different contact metals of pure Au, Cr/Au and Ni/Au (with different thickness ratio) have been formed by thermal evaporation. Note that thermal evaporation has become a common method for the formation of electrodes on graphene due to the low level of defects comparing to the defects of metals made by sputtering[62]. Besides the different metal contacts, different pattern of graphene-metal contacting area (pattern A, pattern B and pattern C) have been studied and sections II.4.2.2 gives more details and results. Among the metal contact candidates shown in Table II-8, there are two further considerations in our choosing criterion. First is the adhesions between contact and substrate, ig, Cr and Ni have better adhesion with Si/SiO_2 than pure Au. Second is compatibility of these metals with our chemical etching process. Table II-9 gives a summary of Rc obtained in IEMN.

Table II-8 Contact resistance Rc reported in literature

E-bE: electro-beam evaperation; TE: thermal evaporation

Contact (nm)	**RcW** (ohm ·µm)	**Rch** (ohm/sq)	**Method** Graphene/Metalization	**Special treatment**	**Ref**
Cu	2900	~1400	CVD / E-bE	Rapid thermal treatment	[8]
Cu (35)	135	~1500	Exfoliated / TE	Annealing	[15]
Cu (50)	125	~1900	Epitaxial / E-bE	edge-contact geometry + Annealing	[16]
Au	630	~1400	CVD / E-bE	Rapid thermal treatment	[8]
Au (20)	340	~1300	CVD / E-bE	-	[17]
Ag	1400	~1400	CVD / E-bE	Rapid thermal treatment	[8]
Pd	570	~1400	CVD / E-bE	Rapid thermal treatment	[8]
Pd (50)	457	~570	Epitaxial / E-bE	edge-contact geometry + Annealing	[16]
Ti	700±500	~5000	Cleavage / E-bE	Annealing	[9]
Ti/Au (20/80)	570±240	~450	CVD / E-bE	Ultraviolet Ozone treatment	[16]
Ti/Au (10/25)	800±200		Exfoliated / E-bE	-	[15]
Ni (100)	100	~2400	Exfoliated / TE	Zigzag graphene edges contact + Annealing	[18]
Ni/Au (30/20)	2100	~3000	CVD / E-bE	-	[10]
Cr/Pd/Au (1/15/60)	150	40	CVD / E-bE	edge-contact geometry + h-BN protection for graphene	[13]
Cr/Au (15/20)	10000	~2500	Cleavage / TE	-	[19]
Pd/Au (30/50)	400	~400	Exfoliated / E-bE	-	[12]

Table II-9 Contact resistance obtained in IEMN

Sample name	Contact (nm)	RcW (ohm ·µm)	R_S (ohm/sq)	Method	Pattern type	Ref
Si10	Ni/Au (20/30)	370 - 960	1000	CVD	B	Wei
Kap10	Au (40)	190 - 580	1100	CVD	A	Wei
GF5	Ni/Au (20/30)	930	2300	Epitaxial	A	Mele

Pattern type A, B and C can be found explanation in following sections

II.4.2.2 The contact resistance obtained in this work based on different TLM pattern structure

We calculated the contact resistance from Transmission Line Method (TLM). Theoretical consideration of this method is provided in appendix IV. On the same chip with other transistors, TLM pattern is fabricated by graphene transfer process, O_2 plasma isolating etching and the metal evaporation followed by a lift-off process. There are totally three different TLM structures explored in my thesis: pattern A on sample Si08 and Si09; pattern B on sample Si10 and pattern C on sample Si10. Detailed discussion and the difference of these three structures will be illustrated in following.

(1) Evaluation of Rc based on Pattern A

Pattern A was used for samples Si08 and Si09. Figure II-38 (a) shows sample Si09 with two probes DC measurement platform which is also applied for all the other samples. Figure II-38 (c) and (d) show that pattern A was designed to have metal contact with two different width of graphene channel, which are 100 µm and 160 µm respectively. The separation between two adjacent contacts (d1,d2,d3,d4,d5 and d6) are designed to be 2, 5, 10, 20, 40 and 80 µm. Additionally, the metal contacts were designed big enough to be pads where the probes for measurement could be placed, as shown in Figure II-38 (b). In this way, the three-dimensional metal contact are directly stacked on the two-dimensional graphene, and thus a conventional surface contact has been formed[60].

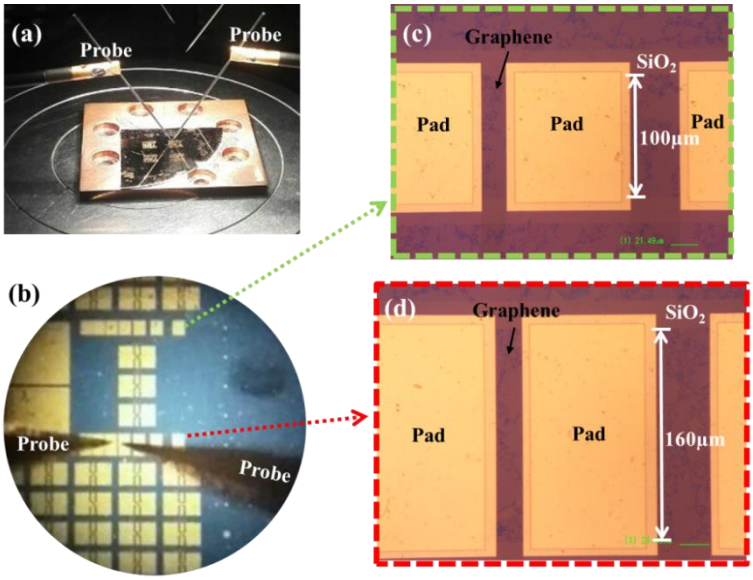


Figure II-38 (a) Sample of Si09 with DC probes for resistance measurement, (b) TLM patterns A with probes placing on the pads, (c) pattern A with graphene channel of 100 µm, (d) pattern A with graphene channel of 160 µm

Figure II-39 (a) shows the measured I-V curve obtained from two adjacent pads with different separation. The linear behavior in I-V curve indicates the formation of ohmic contacts in the pattern A. This behavior is expected for a metal-graphene contact, which behaves like a metal-semimetal system at room temperature [62]. By equation $R = \frac{V}{I}$, the resistance are calculated and plotted as function of separation distance. Figure II-39(b) shows the measured resistance with error bar (average value from several TLM patterns measured results) and linear fitting for both the two kinds of patterns with different channel width (W= 100 µm and W=160 µm). According to the description in Appendix IV, the information such as $R_C W$, R_S, L_T and graphene homogeneity are deduced from Figure II-39 (b) and presented in Table II-10.

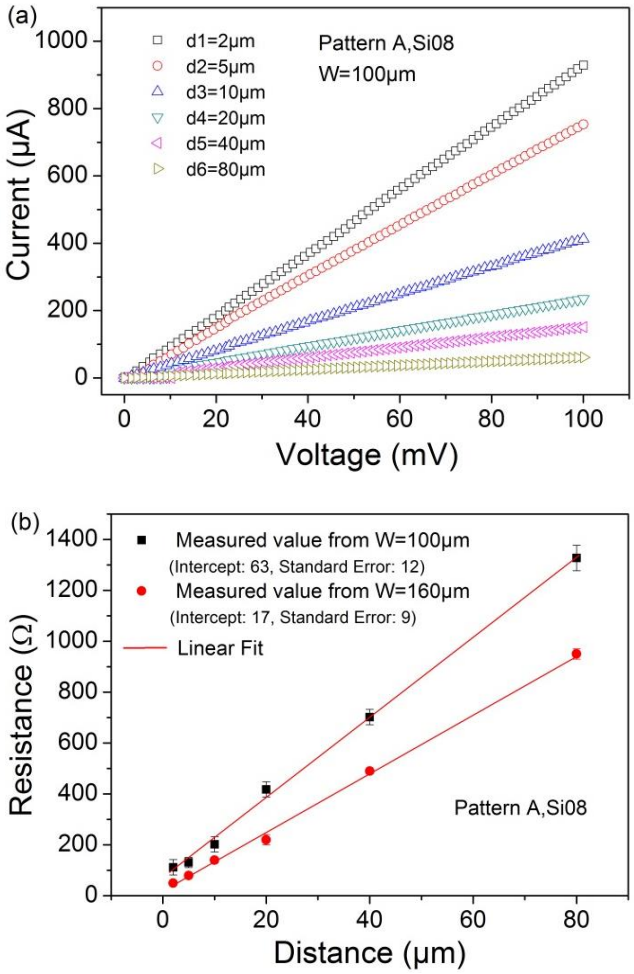


Figure II-39 (a) I-V curve with different channel length (separation between two adjacent pads), (b) Interpretation of TLM results for two channel width, W =100 μm and W =160 μm

Table II-10 Information obtained from TLM of Pattern A

Pattern A Sample	**W (μm)**	**R_CW (Ωμm)**	**L_T (μm)**	**$\rho_{\square}$ (Ω/□)**	**E**	**homogeneity**
Si08 Ni/Au (20/30nm)	100	3000	2.5	1600	12	√
	160	1400	1.5	1800	9	√
Si09 Ni/Au (20/30nm)	100	2800	2.8	1900	17	√
	160	3300	3	1800	13	√

E: Standard error of linear fitting √: Good

(2) Evaluation of Rc based on Pattern B

Pattern B was used for samples Si07 and Si10. Different from pattern A, in pattern B, the metal contacts on graphene are designed to be separate from pads for placing probes, as shown in Figure II-40 (a), (b) and (f). Two different width of graphene

channel have been designed, which are 12 µm and 48 µm respectively, as shown in Figure II-40 (c) and (d). The separation between two adjacent contacts (d1,d2,d3,d4,d5 and d6) are designed to be 1, 2, 4, 6, 8 and 14 µm for graphene channel with width of 12 µm; and 1, 2, 4, 8, 16 and 24 µm for the channel with width of 48 µm. Figure II-40 (e) is the SEM image of Figure II-40 (d), from which the graphene channel with rectangle shape below the contacts could be easily identified. In pattern B, comparing to pattern A, two different things may occur due to the separation of pads and contact metal. **First**, besides the surface contact in the case of pattern A, there is also the part of edge contact making contribution when current flows from metal contacts into graphene. Because the probes are not directly placed on the metal contacts above the graphene, instead, they are placed on pads which are away from channel with some certain distances, the edge contact needs to be taken into account in the current flowing path. In this way, a mixed contact method combining both the surface contact and edge contact has been formed. **Second**, because the pads are formed directly on SiO_2, the metal-substrate adhesion is believed to be stronger than the ones from pattern A, which has pads directly formed on graphene. Thanks to this stronger bonding, no pads movement was observed during measurement in pattern B and also the measurement results were found to be less fluctuating than the ones obtained from pattern A.

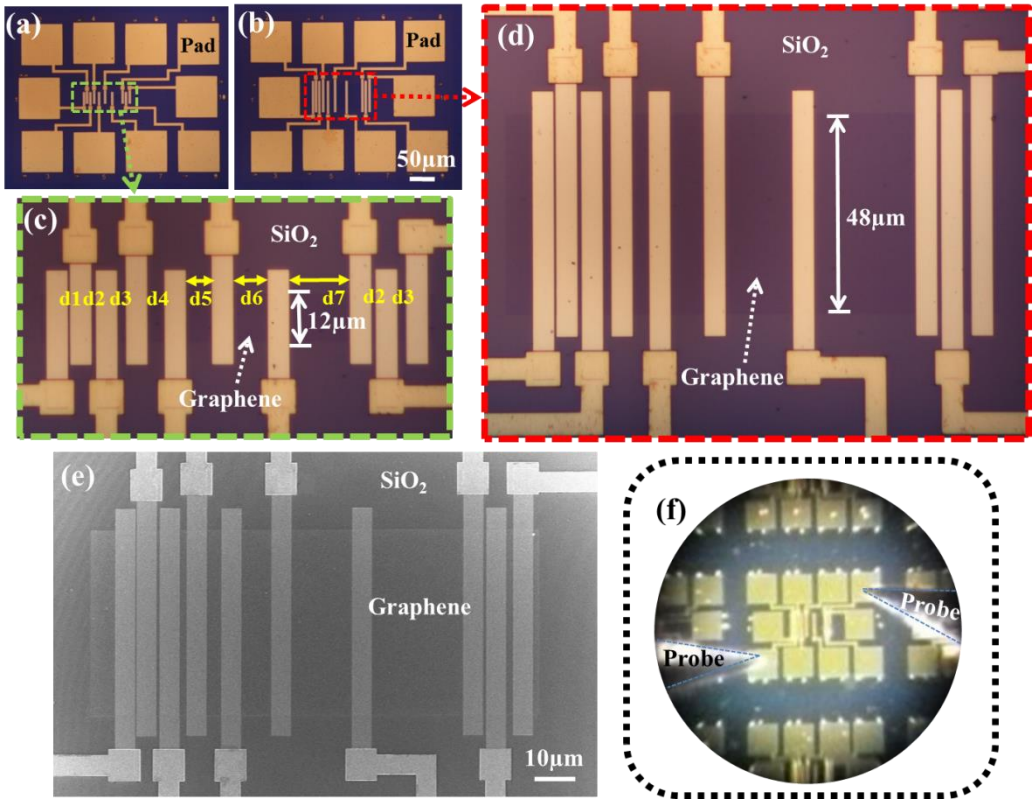


Figure II-40 (a) pattern B with graphene channel of 12 µm, (b) pattern B with graphene channel of 48 µm, (c) zoom-in of (a), (d) zoom-in of (b), (e) SEM image of (d), (f) TLM patterns B with probes placing on the pads

Figure II-41 (a) shows the measured I-V curve obtained from two adjacent pads with different separation. The formation of ohmic contacts in the pattern B is verified by the linear behavior of I-V curve. Then, the resistance are calculated and plotted as function of separation distance. Figure II-41 (b) shows the measured resistance with error bar (average value from several TLM patterns measured results) and linear fitting for both the two kinds of patterns with different channel width (W= 12 µm and W=48 µm). According to the description in Appendix IV, the information such as $R_C W$, R_S, L_T and graphene homogeneity are deduced from Figure II-41 (b) and presented in Table II-11.

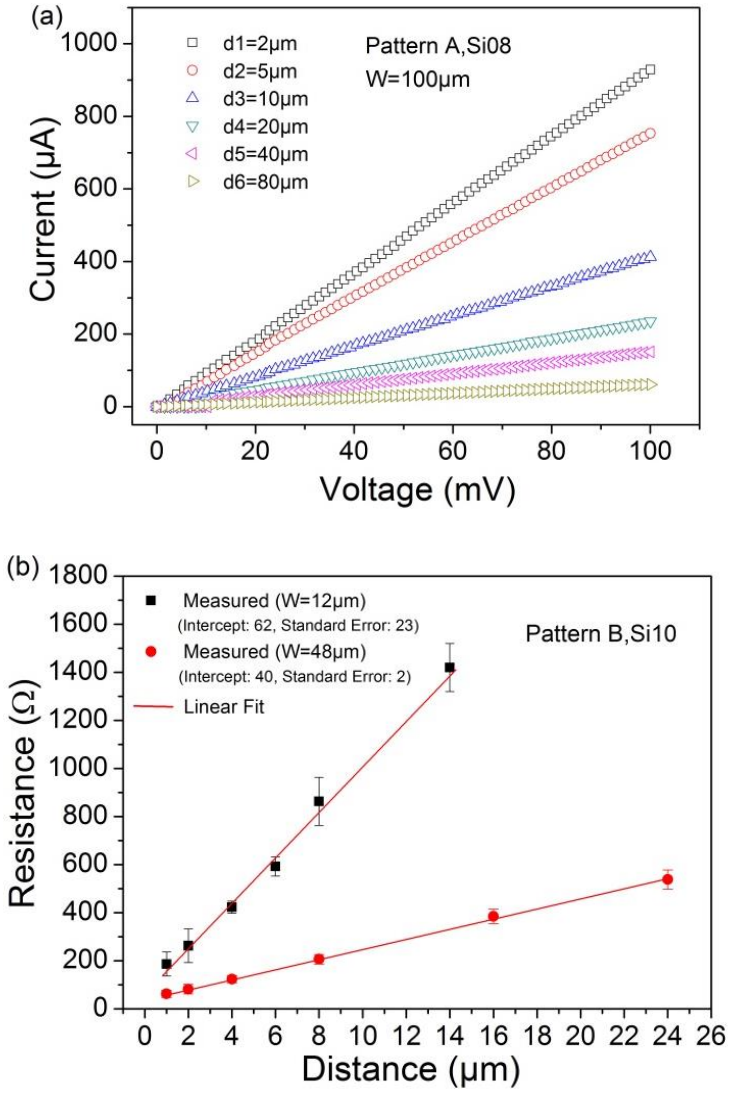


Figure II-41 (a) I-V curve with different channel length, (b) Interpretation of TLM results for two channel width, W =12 µm and W =48 µm

Table II-11 Information obtained from TLM of Pattern B

Pattern B Sample	W (μm)	$R_C W$ (Ω μm)	L_T (μm)	$\rho_{\square}$ (Ω/□)	E	homogeneity
Si10 Ni/Au (10/40nm)	12	370	0.6	1100	23	√
	48	960	2	1000	2	√
Si07 Cr/Ni/Au (2/20/30nm)	12	6600	> 5	660	96	√
	48	7400	> 5	1200	20	√

E: Standard error of linear fitting √: Good

(3) Evaluation of Rc based on Pattern C

Pattern C was used for samples Si07 and Si10. The pattern design is similar to Pattern B, the metal contacts on graphene and pads for placing probes are separate, as shown in Figure II-42 (a). The only modification is that the metal strips on graphene have several squared area with metal-SiO_2 formation. These formations are achievable thanks to the fabrication process of graphene isolated pattern etching. Figure II-42 (b) shows the SEM image of metal contact strips on graphene channel, and the squared holes patterns beneath the strips can be dimly distinguished. Figure II-42 (c), an optical image, shows the squared holes etched on graphene. This image has been taken during the fabrication process after development of PMMA with opening the strips pattern and before metallization. In pattern C, to have enough space for holes patterns, only 48 μm channel width is designed. The separation between two adjacent contacts (d1, d2, d3, d4, d5 and d6) are designed to be 1, 2, 4, 8, 16 and 24 μm. The objective of creating these squared holes with metal-SiO_2 formation is to increase the edge contacts comparing to pattern B. As illustrated in Figure II-42 (d), a layout design, the edge contacts could be introduced.

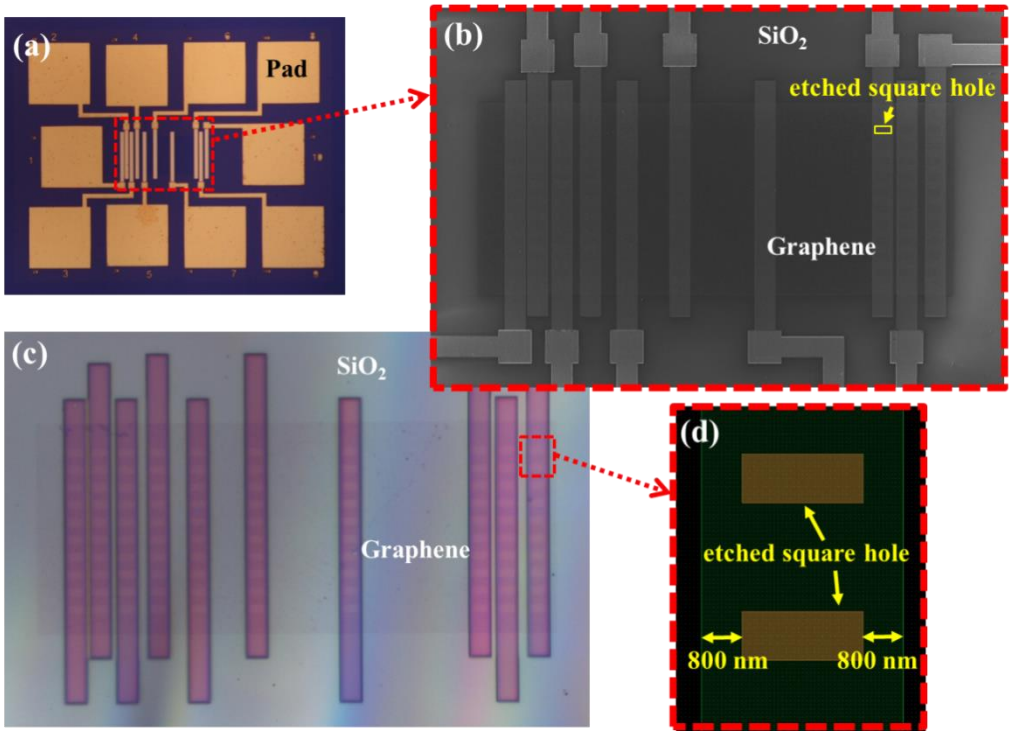


Figure II-42 (a) pattern C with graphene channel of 48 μm, (b) SEM image of zoom-in from (a), (c) optical image of pattern C during the fabrication process of contacts patterns opened, (d)Layout design illustration of zoom-in of (c)

The measured linear behavior of I-V curve obtained from two adjacent pads with different separation indicates the ohmic contacts in the pattern C (see Figure II-43(a)). The resistance are calculated and plotted as function of separation distance. Figure II-43 (b) shows the measured resistance with error bar (average value from several TLM patterns measured results) and linear fitting for sample Si10. According to the description in Appendix IV, the information such as $R_C W$, R_S, L_T and graphene homogeneity are deduced from Figure II-43 (b) and presented in Table II-12. We find the relatively higher value of $R_C W$ comparing to that from pattern B. The possible reason could be the less effective area for transferring the current from metal to graphene. The distance from the square holes to contact strips edge is designed to be 800 nm, as shown in Figure II-42 (d), and this value seems shorter than the transfer length of 1.2 μm which is deduced from TLM measurement. The transfer length would be further discussed in (5).

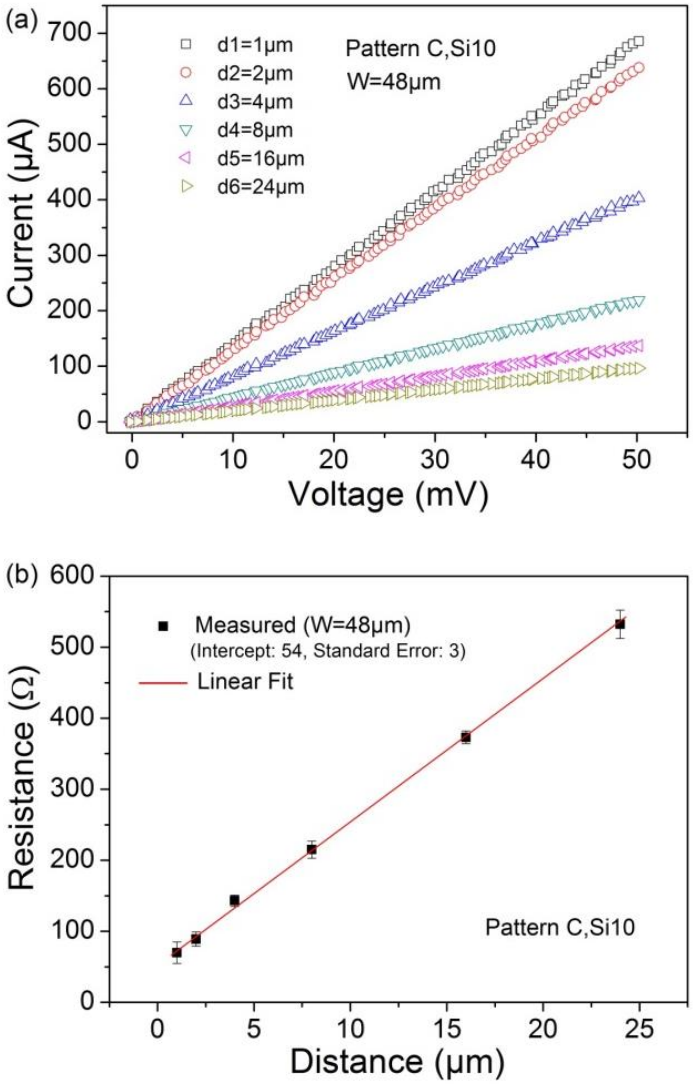


Figure II-43 (a) I-V curve for sample Si10 with different channel length, (b) Interpretation of TLM results for channel width of W =48 μm

Table II-12 Information obtained from TLM of Pattern C

Pattern C Sample	**W (μm)**	**$R_C W$ (Ω μm)**	**L_T (μm)**	**$\rho_{\square}$ (Ω/□)**	**E**	**homogeneity**
Si10 Ni/Au (10/40nm)	48	1300	2.5	910	3	√
Si07 Cr/Ni/Au (2/20/30nm)	48	5700	> 5	1200	17	√

E: Standard error of linear fitting √: Good

(4) Removing resistance from measurement system and pattern

Because in pattern B and also pattern C, the pads and contact metals on graphene are connected by metal strips, and these strips have different length according to different pads. Therefore, for a more precise TLM measurement, a pattern to extract unit resistance of the metal strip has been designed and fabricated together with other TLM patterns on the same chip, as shown in Figure II-44. The strip connecting different pads has a length of 20 µm. The same fabrication process allows the same geometry (thickness and width) of these strips as the ones in TLM patterns. After resistance measurement with different combination of the six pads, as shown in Table II-13, the resistance coming from two probes and the resistance of metal strip are estimated as 1 Ω and 2 Ω per 100 µm, respectively. Based on this result, the resistance presented for pattern B and pattern C are the values after subtracting the resistance from probes and the metal strips.

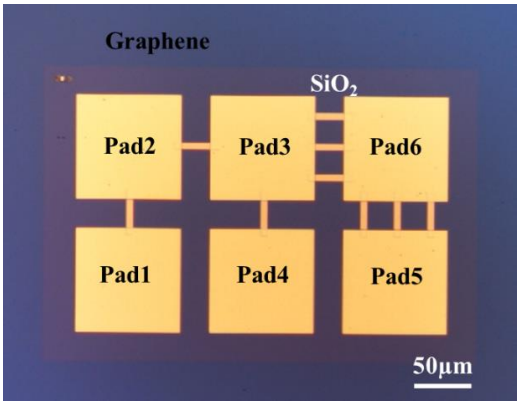


Figure II-44 Optical image of patterns for strip metals resistance extraction

Table II-13 Resistance obtained from different pads combination

Combination		Component	Measured value
Case 1	Pad3→Pad6 Pad6→Pad5	$R_{probe} + 1/3R_{strip}$	1.9 Ω
Case 2	Pad3→Pad5	$R_{probe} + 2/3R_{strip}$	2.2 Ω
Case 3	Pad1→Pad2 Pad2→Pad3 Pad3→Pad4	$R_{probe} + R_{strip}$	2.3 Ω
Case 4	Pad1→Pad3 Pad2→Pad4	$R_{probe} + 2R_{strip}$	2.8 Ω
Case 5	Pad1→Pad4	$R_{probe} + 3R_{strip}$	3.2 Ω

(5) Transfer Length L_T based on Pattern B.

As the current always preferentially flow the least resistance path, from the edge of the contact to far edge area, the current density is not uniform, as shown in Figure 9 (b) of Appendix IV, which is known as *current crowding*. Moving a certain distance away from the edge, the current drops off until zero and this according length is defined as transfer length L_T. Note this extraction method for L_T is based on the assumption that the carrier concentration of graphene has no variation from the channel region to contacts parts where graphene is beneath the metals, which means the linear fitting deduced L_T as illustrated in Figure 9 (c) of Appendix IV is possible. However, some other groups have reported the variation of carrier concentration of graphene from channel to graphene beneath the metal[63]. Therefore, the L_T values presented in this work are only robust approximation.

In order to verify the effect of transfer length on contact resistance, a pattern with different metal/graphene (Au/Ni/Graphene) contacting area has been fabricated, as shown in Figure II-45. In this pattern, the separation between two contacts is kept as a constant value, which is 3µm. But the contacting strips width are varied as: L1= 1µm for pad "a"; L2= 2µm for pad "b"; L3= 4µm for pad "c"; L4= 6µm for pad "d"; L5= 10µm for pad "e"; L6= 14µm for pad "f".

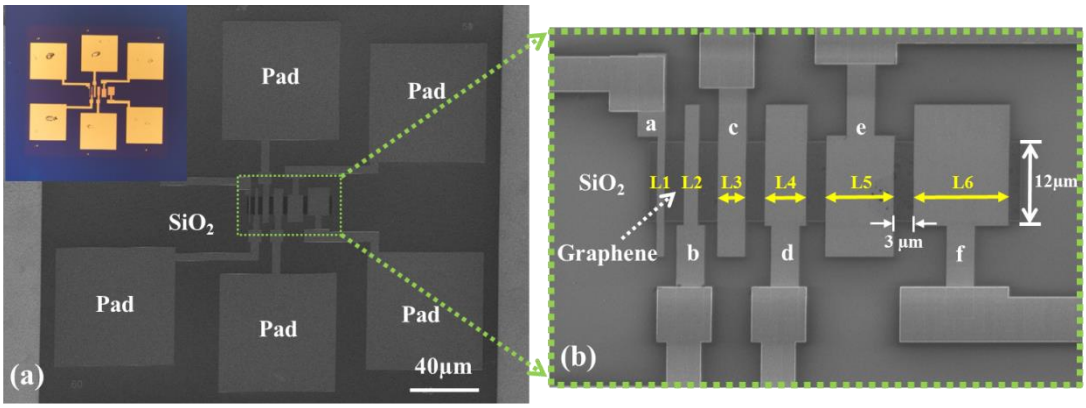


Figure II-45 (a) SEM image of pattern for study of transfer length, with insert of an optical image, (b) zoom-in of (a)

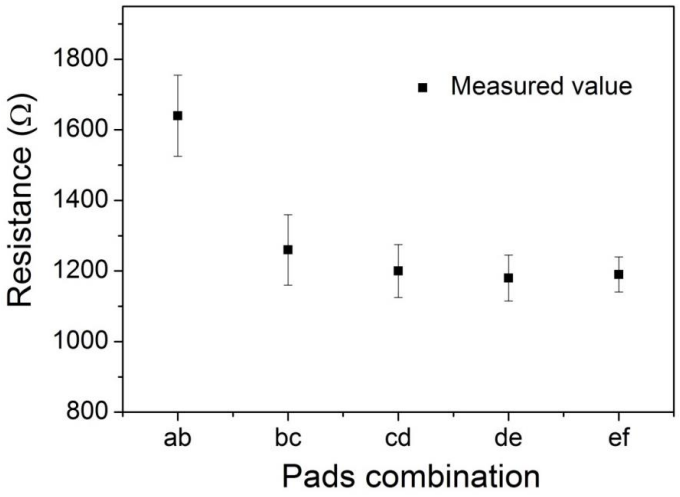


Figure II-46 Resistance vs different pads combination

The resistances between two pads are measured as shown in Figure II-46. Since the channel length is constant for all strips separation, the variations of the measured resistance are due to the changing of contact resistance. It is clear to see two phenomenons. First, when strip width is < 4 µm, as shown in Figure II-46, the resistance between two strips is increasing as the strip width decreased. It proves that the effective transfer area for current from metals to graphene is defined by transfer length. Second, when the strip width is > 4 µm, as shown in Figure II-46, the resistance between two strips becomes constant. It is evident that the contact resistance is determined by edge.

II.4.3 GFETs characterization

In this section, the electrical characterization of GFETs with different dimensions (gate length and gate width) fabricated on rigid substrate of Si/SiO_2 will be discussed. For device performance, the discussion will start from DC behavior of our GFETs, i.e. out-put and transfer characteristic. The dimensions-dependent performance will be presented both from some typical devices and statistical analyses. The result obtained in DC will help to well explore RF performance.

The RF measurement will be carried out by a vector network analyzer (with frequency range of from 0 to 67 GHz), which allows to superimpose high frequency signal to the gate in form of voltage with low amplitude (small signal regime). The microwave detailed study in this section consists of current gain $|H_{21}|$ and unilateral gain U as a function of the frequency of input signal. Additionally, the extrinsic and intrinsic device performance will be deduced by a de-embedding process which will be briefly introduced prior to RF measurement discussion. Importantly, the purpose of this work is to realize GFETs without using high temperature fabrication process, which is

to obtain the dielectric layer by Al natural oxidation on bottom gate. Therefore, the gate capacitance will be explored together with the discussion of RF measurement.

Note that three samples (Si08, Si09 and Si10) will be discussed for Dc and RF measurement, as sample Si07 gives too high contact resistance. The main difference between sample Si08, Si09 and Si10 is the graphene transfer process. The device fabrication of Si08 and Si09 with un-optimized transfer process has been completed several months before Si10, but Si10 has been finished by adopting the optimized transfer process. Although we don′t observe significant improvement in terms of f_t and f_{max}, the performance dispersion of all the devices measured in Si10 was found less fluctuating than what was obtained in sample Si08 and Si09.

II.4.3.1 DC Characterization

Approximately 130 GFETs devices from Si08 and Si09, and 50 devices from Si10 have been characterized. More than half of them are found to be functional. For different device dimension (gate length of L_g = 100, 200, 300 nm and gate width of W= 12, 24, 50 µm), the best performance will be presented, and also a statistic of the performance dispersion will be provided.

(1) transfer characteristic

This DC measurement was carried out at room temperature with an Agilent DC parametric Analyzer (E5260B) in the static mode (gate voltage Vgs was applied in linear way) to determine the variation of drain to source current Ids in a response to Vgs. As mentioned before, being a bend gapless material, the type and concentration of carriers in graphene will continuously change as the function of gate voltage[64][65].

In low V_{ds} bias of 10 mV

Firstly, the transfer characteristic was performed in low bias which has V_{ds} of 10 mV. In such a low bias, the intrinsic properties of graphene such as channel resistance and carrier mobility could be extracted more precisely. Figure II-47 shows the transfer characteristic of devices with different gate width (12 µm gate width device from sample Si09, 24 and 50 µm gate width device from sample Si10). All the devices exhibit ambipolar behavior and Figure II-47 (a) shows the Vgs dependent drain source current I_{ds}, where the minimum Ids is found around Vgs= 0.25 V, indicating the Dirac point. The increase of Ids before (towards negative gate voltage) and after (towards positive gate voltage) indicates the accumulation of holes or electrons as controlled by the gate voltage. Importantly, the position of Dirac point locating at positive gate voltage range indicates a p-type behavior which is due to the p-doped graphene. It is has been well discovered that CVD grown graphene with transfer process is easily p-doped.

Because the long time exposure to air during the device fabrication process leads to graphene channel doped by water, oxygen or even PMMA residue which possibly remain from the transfer process[66][67]. This p-type doped behavior observed here is also in good agreement with Hall effect measurements results.

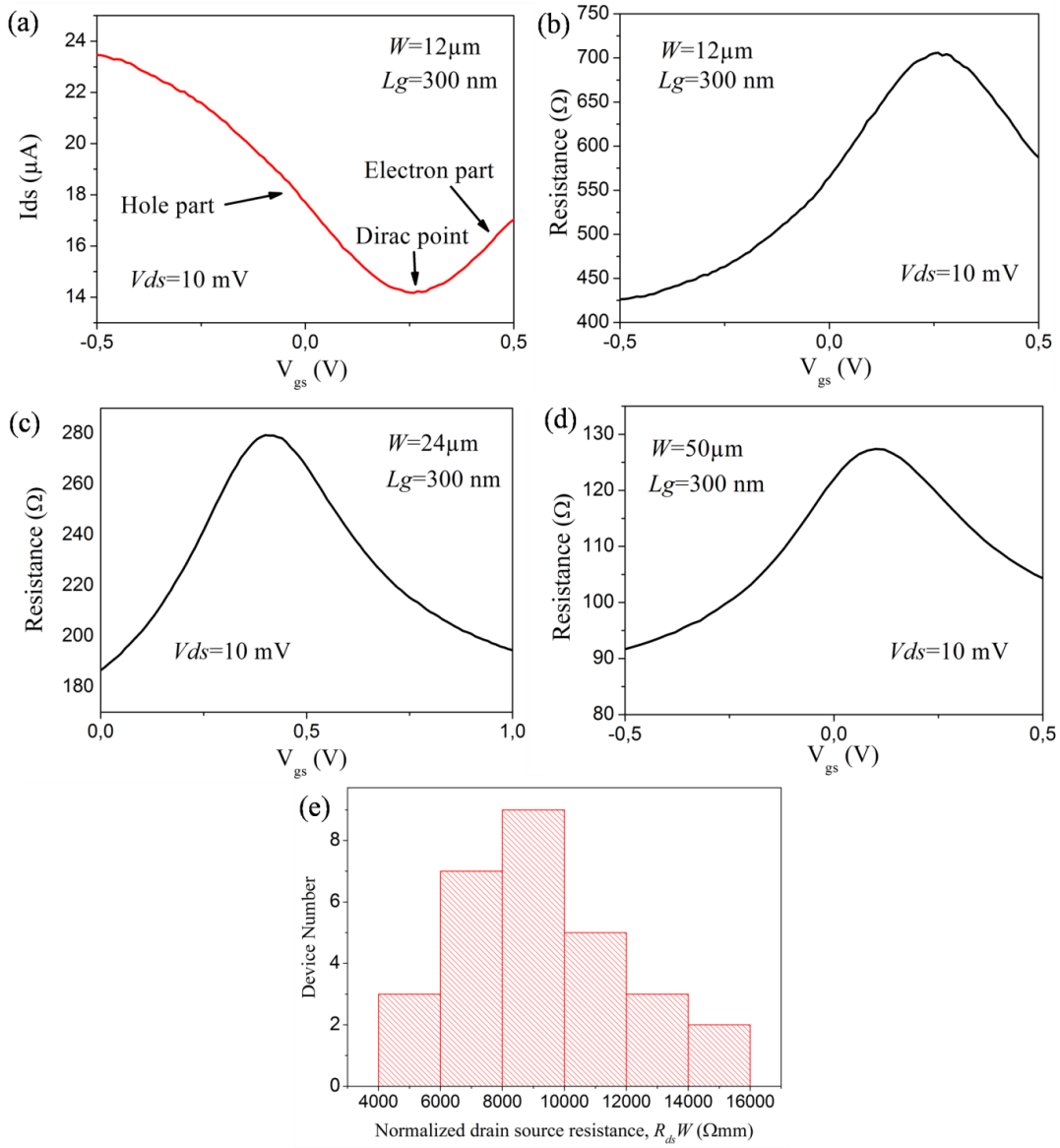


Figure II-47: DC transport characteristics of the device with gate length of 300 nm at Vds = 10 mV, (a) Ids as function of Vgs for device with gate width of 12 µm ; (b) resistance deduced from Vds/Ids of (a), (c) resistance deduced from Vds/Ids of device with 24µm gate width and (d) resistance of device with 50µm gate width; (e) distribution of drain source resistance normalized by gate width

Figure II-47 (b) presents the resistance as a function of Vgs deduced from Vds/Ids of Figure II-47 (a), only the current value is converted to resistance. Note that the resistance presented here consists not only the graphene channel resistance, but also contact resistance and graphene access resistance (the resistance from graphene between drain and source where has not been governed by gate voltage). In such way,

the Dirac points are still clearly visible, but the influence of gate width becomes more obvious in terms of resistance. We find all these three devices have been p-type doped. The resistance at Dirac point almost proportionally decreases as the gate width increases, which indicates the graphene in the channel region should be intact and complete. Additionally, the gate modulation over the total resistance are found to be in the range of 40% to 50% for all the three devices. Figure II-47(e) shows the distribution of the measured drain-to-source resistance normalized by gate width from devices with all different geometry. The resistance variation can be caused by graphene broken or contact instability, which is due to the fabrication process.

To further explore the graphene doping, a statistic of gate voltage dispersion at Dirac points dispersion from around 50 devices in Si08 and Si09 is presented in Figure II-48. In Figure II-48 (a), it is found that most of the devices are p-type doped and some devices are not doped or even n-type doped when Vds of 10 mV is applied.

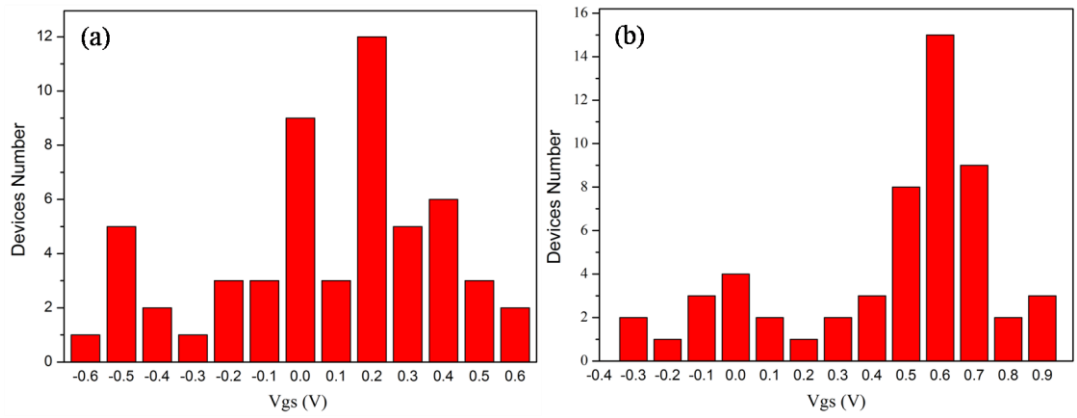


Figure II-48: Distribution of Dirac points at Vgs out of 52 devices (a) in Vds of 10 mV and (b) in Vds of 1 V

In high V_{ds} bias of 1 V

A higher bias with Vds of 1 V is then applied and the ambipolar behavior is still observed (see Figure II-49 (a)). However, comparing to the Ids curve obtained with low bias with Vds of 10 mV (dot red line), three variations could be found. First, the whole Ids value have increased to *mA* from *μA*. Taking the Dirac point as an example, the minimum Ids are found to be 14 μA and 1.8 mA for Vds of 10 mV and 1V respectively. Second, the Vgs position of Dirac point has shifted from 0.25 V to 0.55 V . This shift indicates that the concentration of p-type carriers has increased in graphene channel, which is due to the larger bias voltage[68]. Third, the shape of the ambipolar curve has become less obvious, which is also due to the larger density of carriers.

To further explore the graphene doping, a statistic of gate voltage dispersion study at Dirac points is employed again. In Figure II-48, as Vds increases up to 1 V, the whole Dirac points are found to be moved towards positive Vgs, which agrees well with the

occurrence observed in Figure II-49(a).

Figure II-49(b) shows the leakage current through the dielectric, the 4.3 nm Al_2O_3 natural oxidation, is very low with the order of nA for both 10 mV and 1 V of Vds. It indicates the good quality of this oxidation layer, even comparing to the previous work where 10 nm of Al_2O_3 was deposited by the ALD method for the same Vds of 1V.

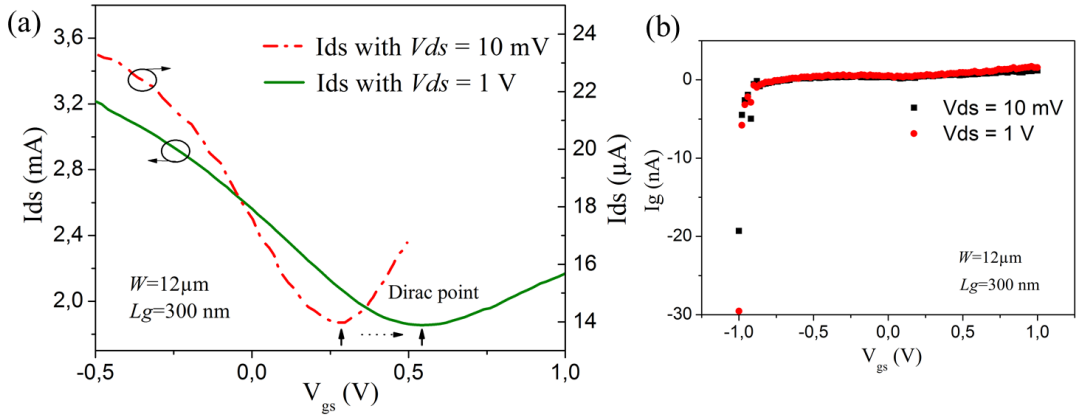


Figure II-49: From sample Si09, (a) Transfer characteristics with two different bias voltage Vds (10mV and 1V); (b) leakage current through the gate

(2) Transconductance

Transconductance describes the ratio of drain current (Ids) variation to the gate voltage (Vgs) variation, and it is written as gm. It reflects how much the current through channel is responding to the gate modulation via gate voltage. It is a crucial parameter for determining the device performance in RF regime. In DC regime, the gm definition is found below:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}}\left(ne\mu V_{Ch}\frac{w}{L}\right) \qquad \text{(II-5)}$$

Where n:carrier concentration; e: element charge; μ:carrier mobility; V_{ch}: the voltage drops in channel region; W: gate width; L: gate length

Importantly, the Vch is proportional to Vds, and the ratio is constant which is determined by channel resistance, access resistance (graphene region between drain and source which has not been governed by gate) and contact resistance. Therefore, Vch will increase proportionally with increasing Vds. Figure II-50 (a) shows the gm deduced from Ids curve with Vds of 1V, and (b) shows the evolution of gm according to different Vds. The absolute value of gm is found to be increased as the increase of Vds, which can be explained by Equation II-5.

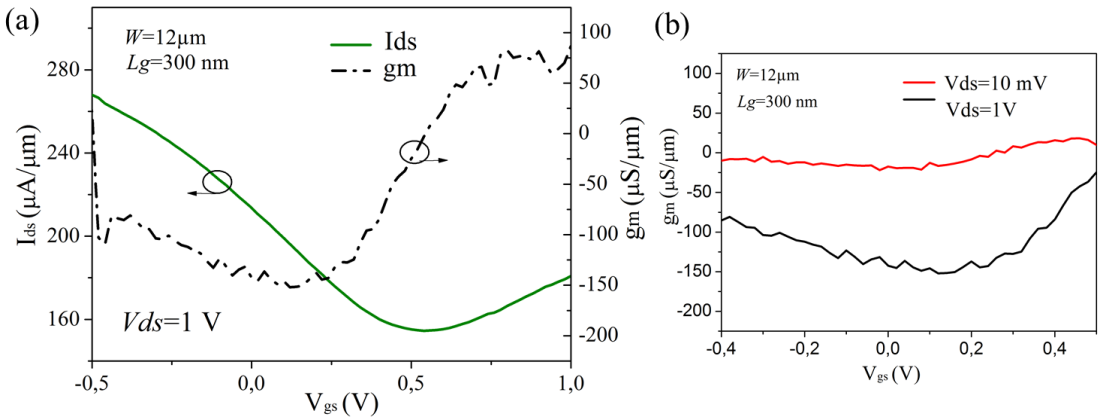


Figure II-50: From sample Si09, (a) Transfer characteristics with gm deduced with Vds of 1V (b) evolution of gm with different Vds (10mV and 1V)

In Figure II-50 (a), the maximum static transconductance of 150 µS/µm in absolute value could be extracted. One can find that in the electron branch, the maximum gm is around 90 µS/µm, which is smaller than what we find in hole branch, indicating that the p-type branch of our GFETs varies faster than that of n-type branch. This is due to the contribution of high holes density of our p-type graphene layer. Therefore, in this work, we mostly explore the hole branch of our devices.

Table II-14 gives the measured gm (summarized as an average value without normalized by gate width, an average value normalized by gate width, and best individual value) for devices with different geometry in terms of gate width W and gate length L_g. In Table II-14, we find that the value of gm decreases slightly with the decrease of gate length for all the three gate width devices. We believe that this can be attributed to the competition between decreases of effective gating area and the increase of the non-gating area. Because in this work, the drain source separation is a constant value of 1 µm, which means the decrease of gate length will increase the access area (non-gating area graphene between drain and source), and consequently the access resistance will increase. It means, from equation II-5, when gate length L decrease, the value of V_{ch} will also decrease. Therefore, the final gm value will be determined by the competition of these two items.

Table II-14: evolution of gm for devices with different geometry, @ Vds of 1V

W (μm)	L_g (nm)	g_m average ms	g_m average μs/μm	g_m best μs/μm
12	100	1.2	100	150
	200	1.5	128	167
	300	1.9	155	208
24	100	1.8	75	146
	200	2.3	96	104
	300	3.2	133	166
50	100	2.1	42	80
	200	3.8	76	100
	300	4.4	88	108

(3) Output characteristics

This DC measurement was carried out at room temperature with an Agilent DC parametric Analyzer (E5260B) to explore the drain source current Ids as function of both drain voltage Vds and gate voltage Vgs.

Figure II-51 shows the output curves from devices with the same gate length (Lg=300nm) but different gate width (W= 12, 24 and 50 μm, from Si09 sample and Si10 sample, respectively). In Figure II-51 (a), the transfer characteristic can be found in Figure II-50 (a). The range of Vgs was selected from the hole branch observed from transfer characteristic. For example in Figure II-51(a), for the same device (*Lg*= 300 nm, *W*= 12 μm) with transfer characteristic shown in Figure II-50, the Vgs from -1 V to 200 mV have been explored to cover the best gm value for output drain current. In the same way, Figure II-51 (b) and (c) presents the output curve based on the same analysis. Note that the drain current shown in Figure II-51 is not normalized by gate width. After normalization (divided by gate width), the drain current reaches a maximum value of 292, 308 and 260 μA/μm for device with gate width of 12, 24 and 50 μm respectively, at drain voltage of Vds=1V and Vgs=-1 V.

We don't observe the phenomenon of current saturation, even in the higher Vds region. Indeed the saturation is difficult to obtain in graphene due to the effect of contact resistance and the absence of proper bandgap [69]. Therefore, these devices will not operate in saturation mode. Nevertheless, for the devices fabricated on flexible substrate (see next chapter), we observed the tendency of current saturation

phenomenon, which is believed due to the decrease of the contact resistance.

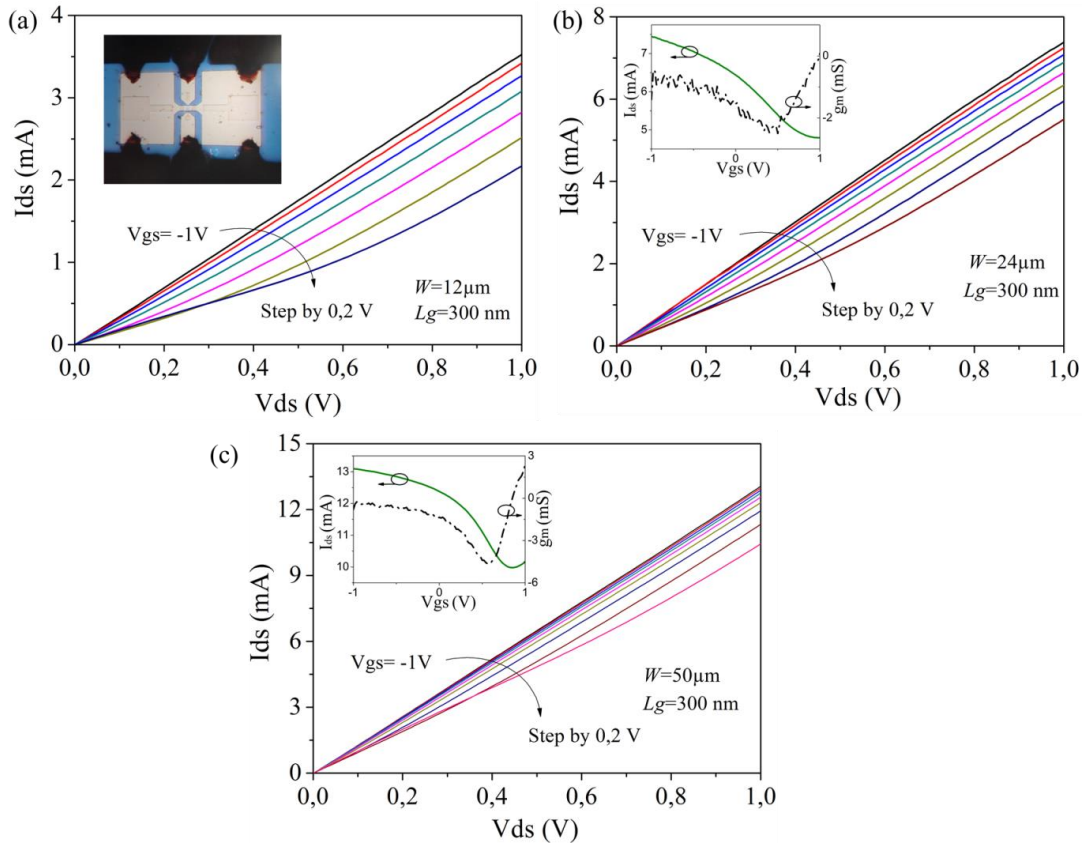


Figure II-51: Output characteristic of devices with (a) gate width of 12 µm, the inset image show a final device with probes on its coplanar wave guide access; (b) gate width of 24 µm, the inset image show its transfer characteristic with Vds=1V; (c) gate width of 50 µm, the inset image show its transfer characteristic with Vds=1V

II.4.3.2 Small-signal high frequency characteristics

(1) Background knowledge

In high frequency regime, the transistor can be seen as a two-port network. The high frequency signal will be treated as a wave, and its power will be considered and measured by S parameter, which are easier to be measured and worked with than any other voltage- or current-based parameters. More details about two-port network and S parameters have been given in chapter1. For our GFETs, an input small signal (voltage) with high frequency is superimposed with a certain voltage (gate voltage for best gm obtained in DC) on the gate, and the output signal (current) with a certain response high frequency will be measured. Both these input and output signal will be considered and measured in terms of S parameters by a Vector Network Analyzer (VNA), which is the most common and important measurement equipment in high frequency range. The measurement setup used in this work, see Figure II-52, composes of a probing station of

ground-signal-ground (GSG) coplanar microwave infinity cascade and an Agilent E8361 A Vector Network Analyzer which has a measurement frequency range of 0.01 GHz ~ 67 GHz. The devices could be externally biased by a computer controlled external voltage sources and bias tees and the VNA could measure in this way the bias dependence of the S-parameters.

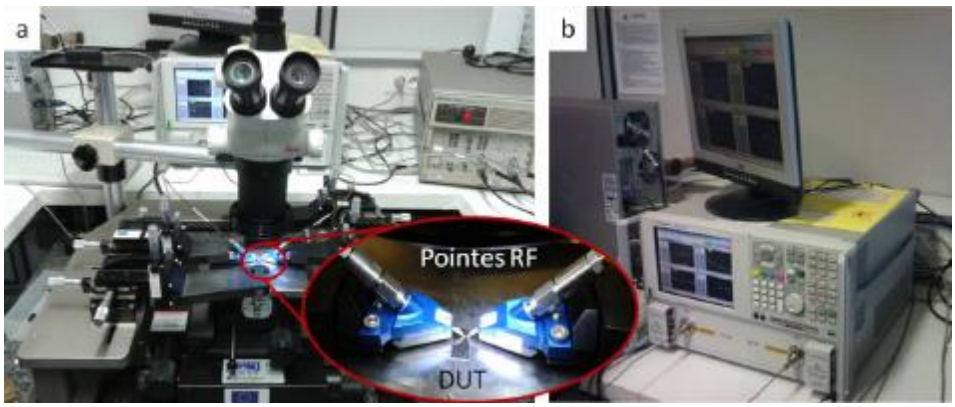


Figure II-52: (a) Microwave station with microwave probes (b) Vector Network Analyzer

For more precise measurement results, a calibration procedure has to be applied each time before the measurement, Figure II-53 shows the procedure of RF measurement for GFETs. The purpose of this calibration is to remove the errors introduced by external probes or coaxial cables so that the measurement reference plane could be moved near to the access component (device under test, DUT). In this work, a standard calibration method Line-Reflect-Reflect-Match is performed, which needs a transmission line (through); structures of both open circuit (open) and short-circuited (short); and a resistance of 50 Ω for matching the cable impedance (match).

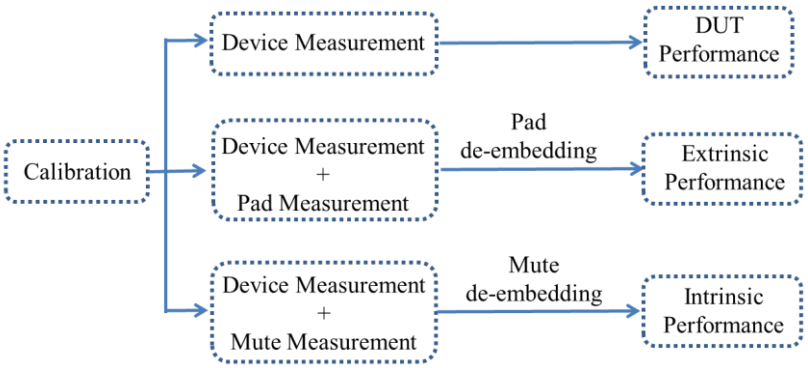


Figure II-53: Procedure of RF measurement for GFETs

(2) De-embedding

On-wafer high frequency measurements always employ CPW as access to the

active region. However, parasitic effects from these CPW structures will be introduced to the final measurement results. Therefore, these effects have to be removed to obtain more accurate device characteristics. This removal procedure is implemented by de-embedding.

Field Effect transistors working with small signals can be normally described by using an equivalent circuit, in which assuming all the elements are constant and independent of frequency. In previous work for GFETs, a small signal equivalent circuit has been extracted from the measured S parameters and all elements are confirmed to be independent of frequency, see Figure II-54 (a). Three levels (or reference plane) have been illustrated, which are plan of DUT, extrinsic, and intrinsic, the according elements for each plan has been marked by different color in Figure II-54(a). The performance of extrinsic and intrinsic can be obtained by pad de-embedding and mute de-embedding, respectively. To realize these two de-embedding procedures, two special open structures, denoted as “pad” and “mute” have been fabricated together with other transistors by the same fabrication process to keep the same geometry. See Figure II-54 (b), the pad structure has only the coplanar access of GFET. The mute structure has the same geometrical structure as the active part of transistors but without graphene between source and drain. S parameters of DUT, pad and mute are first obtained by measurement, which are then converted to Y parameters, the admittance matrix [Y]. The de-embedding procedure is simply based on [Y] subtraction. Y parameters of extrinsic are obtained by $[Y_{extr}]=[Y_{DUT}] - [Y_{Pad}]$ and Y parameters of intrinsic are obtained by $[Y_{intr}]=[Y_{DUT}] - [Y_{Mute}]$. The $[Y_{extr}]$ and $[Y_{intr}]$ are then converted to $[S_{extr}]$ and $[S_{intr}]$ for device extrinsic or device intrinsic performance extraction.

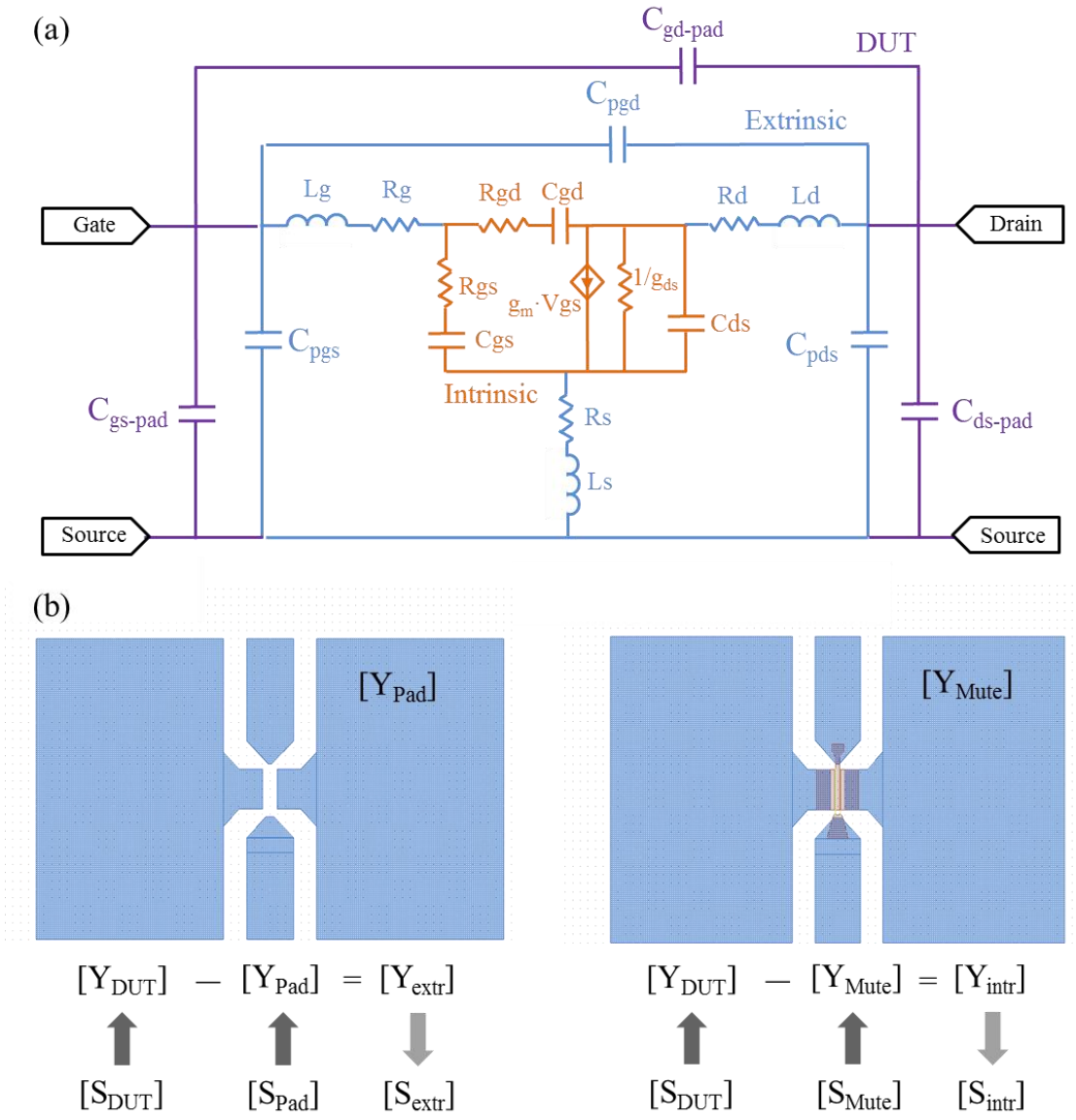


Figure II-54: (a) a small signal equivalent circuit (b) practical de-embedding structure of *Ypad* and *Ymute* for extrinsic and intrinsic performance, respectively

Note that in this work, the de-embedding structures of "pad" and "mute" were designed to mainly consider the effect of capacitance. Therefore, after "pad" de-embedding, the effect of capacitance Cgs-pad, Cgd-pad and Cds-pad will be removed (see Figure II-54(a), elements marked by purple), to obtain extrinsic performance. After "mute" de-embedding, only the effect of capacitance Cpgs, Cpgd and Cpds will be removed (see Figure II-54(a), elements marked by blue), but the effect of resistance and inductance still remains with "intrinsic" performance. A future work for a complete de-embedding is needed, in which not only the capacitances, but also the items of resistance and inductance will be taken into account.

(3) Figure of Merit

Current gain, $|H_{21}|$

In this section, the current gain (ratio of output current to the input current) as function of frequency, together with the information of cut-off frequency, f_t (at which frequency the current gain drops to unity) for GFETs with different geometry will be discussed. The evolution of $|H_{21}|$ should decrease with a variation of -20 dB/ decade as increasing the frequency of the input signal. Equation II-1 gives the definition of f_t based on elements of small signal equivalent circuit in intrinsic plane.

From Figure II-55, it can be seen that for a given device with a constant value of gate capacitance, C_{gs}, f_t will be determined by gm which is Vg dependent. To explore the best value of f_t a certain range of Vg is selected to find the best gm based on transfer characteristic in DC regime. Figure II-55 gives an example of Vg dependent current gain from a device with 100 nm gate length and 300 µm gate width. Note that the current gain is intrinsic value, which was deduced after de-embedding operation. The relative discussion is shown in next paragraph.

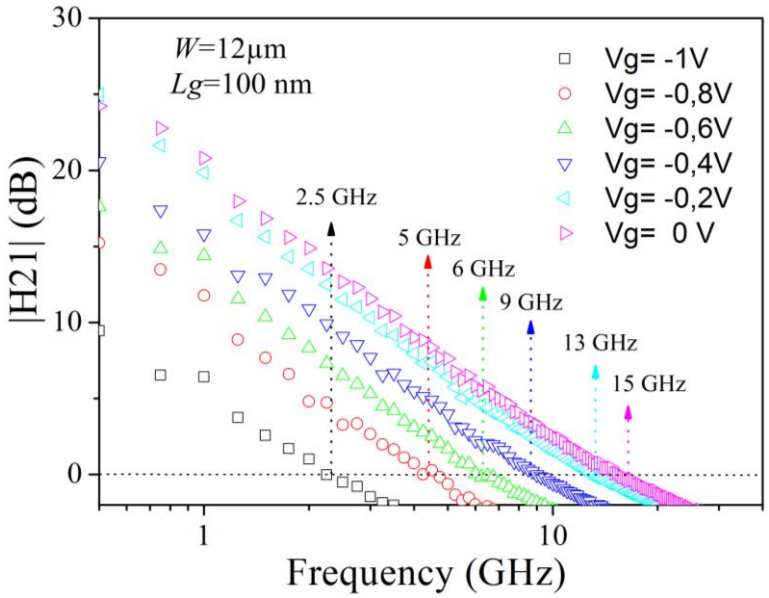


Figure II-55: The intrinsic current gain |H21| of GFET device with 100 nm gate length and 12 µm gate width as function of frequency for different Vgs, Vds= 1V

Additionally, the performance before de-embedding, DUT, and also the after de-embedding performance of extrinsic and intrinsic will be provided. Equation II-6 gives the current gain derived from S parameters. From S parameters of DUT, extrinsic and intrinsic based on different de-embedding procedure, current gain is deduced respectively. Figure II-56 (d) shows the scaling of gate length with f_t, the cut-off frequency increasing with the decrease of gate length partially agrees with literatures, which is determined by both the variation of gm and total gate capacitance.

$$|H_{21}|^2 = \left|\frac{-2S_{21}}{(1-S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}}\right|^2 \quad \text{(II-6)}$$

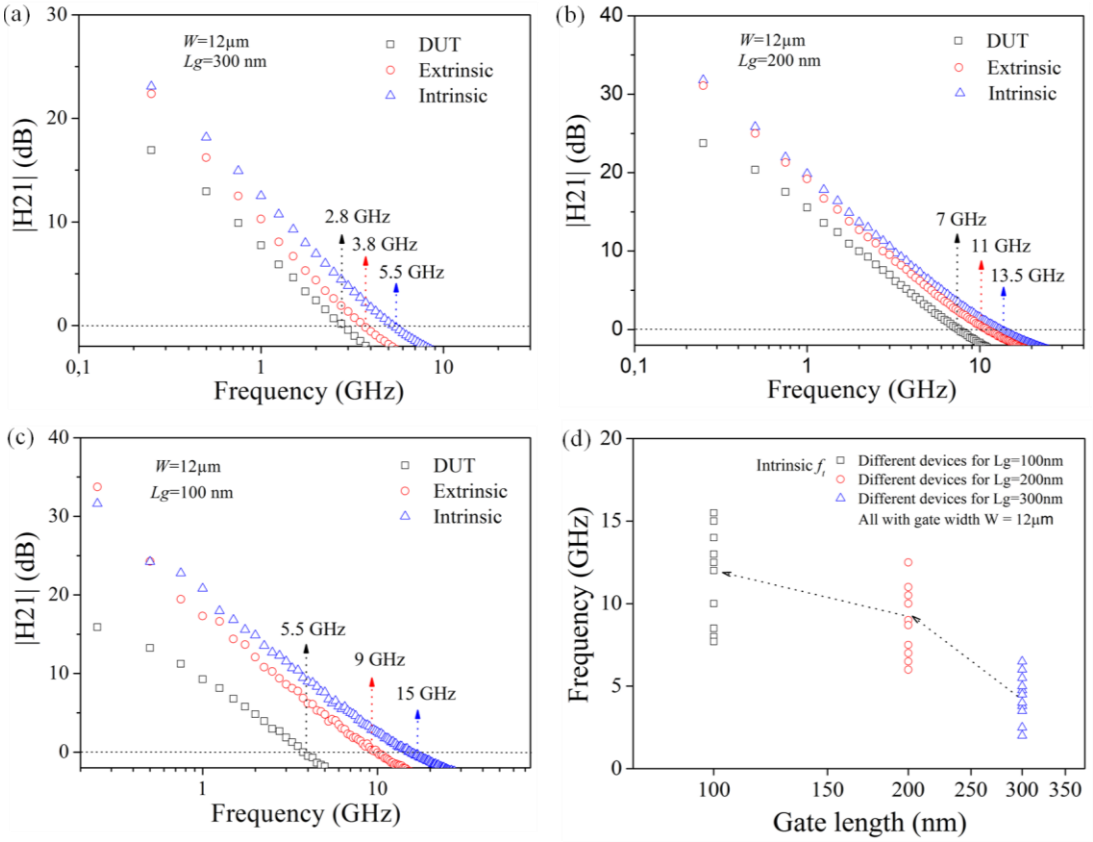


Figure II-56: The DUT, extrinsic and intrinsic current gain |H21| as function of frequency of GFET device with 12 µm gate width and different gate length of (a)300 nm, (b)200 nm and (c)100nm,Vds=1V; (d) the scaling of gate length with f_T

Unilateral gain, U

Mason's unilateral gain U is the power gain with an evaluation of -20 dB/ decade as a function of frequency. The maximum oscillation, f_{max}, is the frequency at which U equals 1, indicating that power gain is not possible with frequency beyond f_{max}. Unilateral gain can be deduced from S parameters, as given by equation II-7. In this work, only the performance without de-embedding will be presented, because U is much less sensitive to the de-embedding procedure as explained previously.

$$U = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2\left(k\left|\frac{S_{21}}{S_{12}}\right|-Re\left(\frac{S_{21}}{S_{12}}\right)\right)} \quad \text{(II-7)}$$

Where $k = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{21}S_{12}|^2}{2S_{21}S_{12}}$

We also find that maximum oscillation frequency is gate voltage dependent. Figure II-57 shows an example of best f_{max} extraction from evolution of U with different gate voltage. Figure II-58 shows the best f_{max} value obtained for device with

different gate length with gate width of 12µm, all the best and average performance of this device and other devices with 24 and 50 µm gate width are provided in Table II-15.

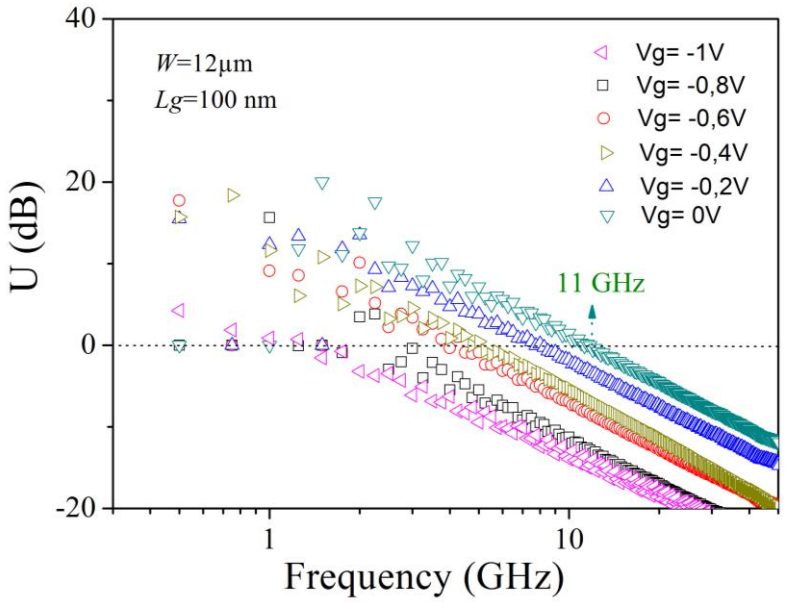


Figure II-57: Evolution of unilateral gain (U) with different gate voltage, Vds=1V

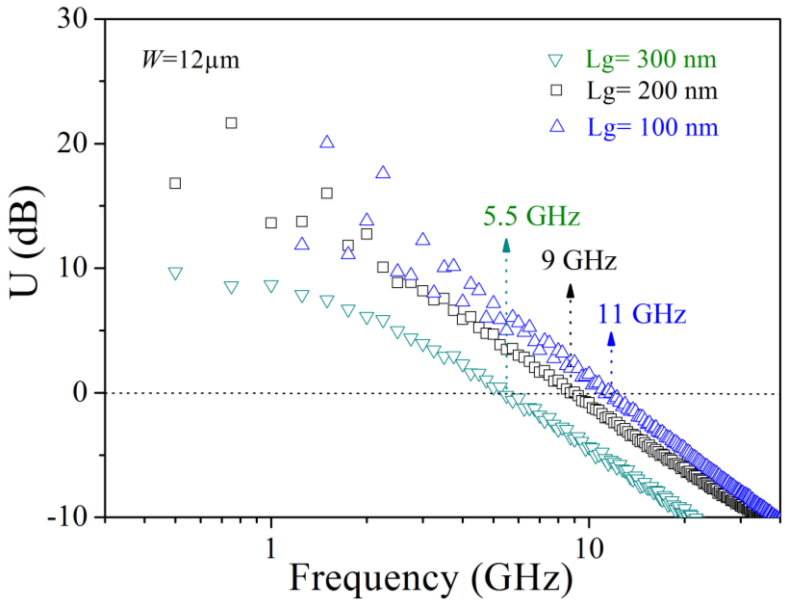


Figure II-58: Unilateral gain (U) with different gate length, and a constant value of gate width, W= 12 µm and Vds=1V

Table II-15: Summary of device performance with different gate length and width

W (μm)	L_g (nm)	f_T average GHz	f_T best GHz	f_{max} average GHz	f_{max} best GHz
12	100	12	15.5	8	11
	200	9	13	7	9
	300	5	7.5	3.5	5.5
24	100	8	10	5	8
	200	6.5	8	5	7
	300	4	8.5	2	6
50	100	5	13	3.5	10.4
	200	4.5	8.5	2	5
	300	3.5	7	1.5	4

In Table II-15, it is found that all the devices with gate width of 12, 24 and 50 μm, both the average and best cut-off frequency increase with the decrease of gate length. Here, this tendency is due to the effect from both gm and total gate capacitance, which is in accordance with previous reports [70]. Also, we have observed that for the 50 μm gate width devices, the values of f_t are smaller than that obtained from 12 and 24 μm gate width devices. This is ascribing to the less increasing of gm comparing to the total gate capacitance increase. For maximum oscillation frequency, the scaling behavior with both gate length and gate width is not as clear as f_t. Because it is determined not only by gm and total gate capacitance, but also by the competition between gate resistance R_g and drain source resistance R_{ds}. Note that in Table II-15, the values of f_t are intrinsic performance after "mute" de-embedding, and f_{max} are DUT performance without any de-embedding procedure.

Figure II-59 shows the device performance dispersion according to different drain-to-source resistance. Three range of as measured drain to source resistance are explored: 300 to 500, 500 to 700 and 700 to 1200 Ω. The variation of drain to source resistance can be caused by either graphene quality or contact resistance variation. We observe that devices with low drain to source resistance yields the best performance. It demonstrates the importance of keeping graphene quality intact and reducing

contact resistance.

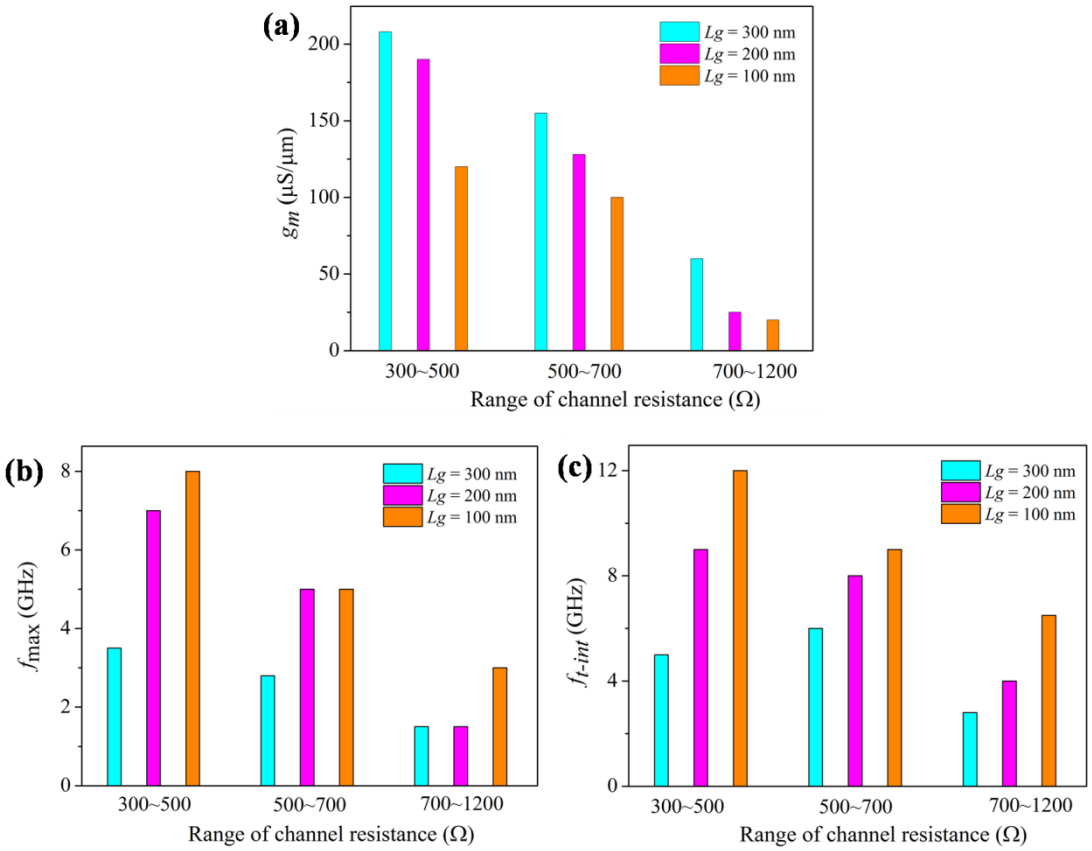


Figure II-59:Device performance dispersion according to different drain/source resistance: (a) transconductance, *gm*; (b) f_{max} and (c) $f_{t\text{-}int}$

Gate capacitance

Because gate capacitance is an important parameter to determine both current gain and unilateral gain, and it is derived from 4.3 nm natural oxide of Al_2O_3 on bottom gates, which mainly differs this work from others, hereafter some discussion on it will be followed.

We choose the 12 μm gate width devices to explore the gate capacitance because of their stable and excellent performance in RF. Deduced from S parameters, the average value of total gate capacitance were obtained to be be 16±0.8 fF, 28±1 fF, 42±1.4 fF corresponding to gate length Lg=100 nm, 200 nm and 300 nm. After graphene transfer process, the graphene may suspend partly on the lateral side of gates after transfer process. As shown in Figure II-60(a) and (b), this suspending introduces a gap between graphene and gate dielectric with air inside. When the gate capacitance is calculated, this stray capacitance, C_x, needs to be taken into account as well. Therefore, to fully analyze the gate capacitance, we evaluated the geometric capacitance C_{gs}, quantum capacitance C_Q and stray capacitance C_x which is caused by the air gap.

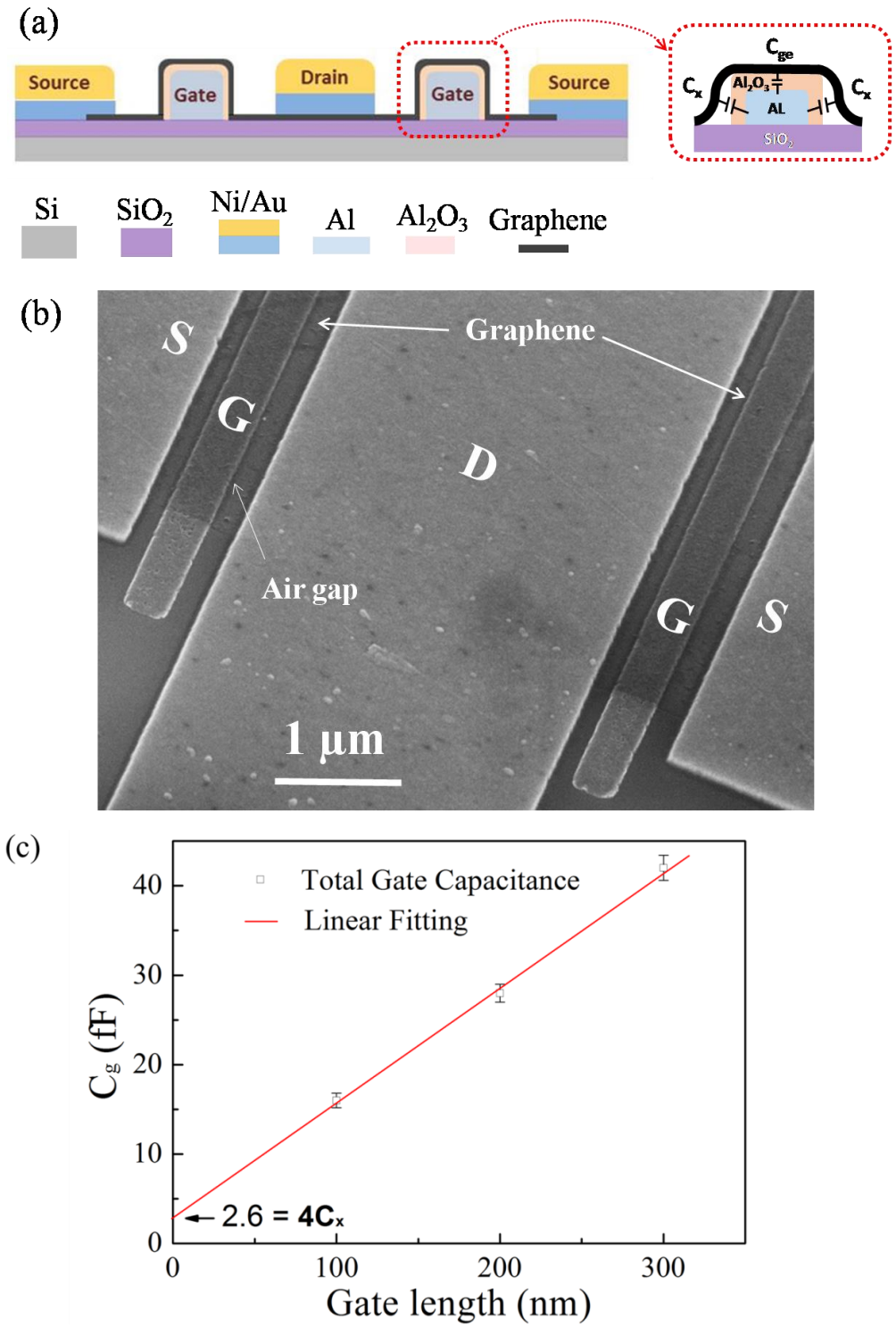


Figure II-60: Illustration of air gap between graphene and dielectric in (a) schematic and (b) SEM images, (c) scaling of total gate capacitance with gate length

We first plot the total gate capacitance deduced from S parameter with the according gate length, and by a linear fit, about 0.65 fF of stray capacitance is obtained, as shown in Figure II-60(c). The quantum capacitance C_Q describes the response of the charge inside the channel to the conduction and valence band movement due to the gate

voltage variation. C_Q should be proportional to the density of states (DOS).When in conventional systems, C_Q is large and can be neglected because it is parallel with the geometric capacitance. However, in low-dimensional system, such as graphene based devices, it can be very small and in this way have some contribution to the total capacitance which can not be neglected. Figure II-61 shows the total gate capacitance verse bottom gate voltage measurement. The clear variation of the total gate capacitance for different gate voltage indicates the existence of quantum capacitance in our devices.

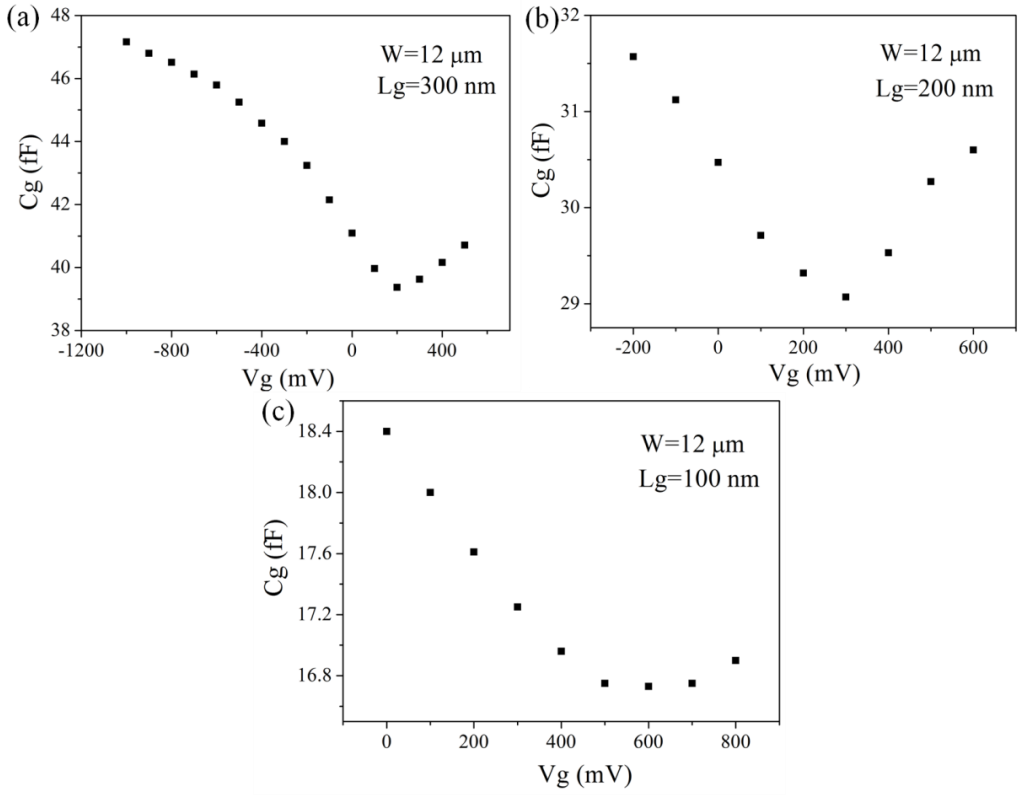


Figure II-61: Measurement of total gate capacitance Cg deduced from S parameters versus gate voltage for devices with 12 µm gate width and different gate length of (a) 300nm, (b) 200nm and (c)100nm

The quantum capacitance is evaluated by using formula equation: $C_Q = \frac{2e^2}{h\sqrt{\pi}V_F/(2\pi)}\sqrt{n}$, here, h is planck constant, V_F is the Fermi velocity of Dirac electron, e is the electron charge, and n is the carrier concentration[71]. The carrier density $n \approx 2.6\times10^{15}$ m^{-2} is evaluated by using experimental data from both *I-V* measurement and Hall measurement. This gives the value of C_Q = 16.8 fF, corresponding to the gate length L_g = 100 nm and gate width W=12 µm. Based on the values of C_Q and total gate capacitance mentioned above, geometric capacitance C_{gs} is about 11.2±1.4 fF corresponding to the gate length L_g = 100 nm and gate width W=12 µm (Note that we calculate it as a total value, by considering double-gate structure).

Conclusion of Chapter II

For graphene transfer, we have optimized the conventional wet transfer process, and applied it to our device fabrication. Optical microscope, SEM and Raman mapping measurement have been used to analyze the transfer efficiency. Homogeneous, clean and defect free (holes, cracks or folders) graphene is observed by both optical and SEM images. High value of 2D to G peak ratio (around 5) and low value of D peak from Raman spectra fatherly indicate that good quality monolayer graphene has been obtained after transfer process.

For device fabrication, we have developed a fabrication process based on natural oxidation of aluminum as dielectrics of bottom gates structure. This process avoids the conventional ALD method for dielectric which needs high temperature, thus it is very suitable for flexible devices. Importantly, the graphene quality is well preserved after all the fabrication process, which has been confirmed by SEM and Raman mapping. Devices of GFETs with different geometry (gate width of 12, 24 and 50 μm combining with gate length of 100, 200 and 300 nm) and also together with other components, such as Hall effect pattern and TLM structures have been realized after fabrication process.

For device characterization, we first find p-type graphene with high value of mobility, 3400 cm^2/Vs, obtained by using Hall effect measurement. Contact resistance has been deduced from different TLM pattern and the best value of contact resistance in range of 370~960 ohm ·μm is obtained from pattern B with Ni/Au (20/30nm). After, DC behavior of our devices has been discussed prior to RF performance. Best transconductance, gm, is found to be 155 μs/μm for device with 300nm gate length and 12 μm gate width. A tendency of gm decreasing with the decrease of gate length has been observed, and explained as the competition between gating and non-gating area due to the constant drain to source distance of 1μm. In RF regime, current gain and unilateral gain for devices with different geometry have been fully discussed. De-embedding procedures of pad and mute are used to extract extrinsic and intrinsic device performance. The intrinsic value of cut off frequency f_t of 15.5 GHz and maximum oscillation frequency f_{max} of 11 GHz are obtained in device with 100 nm gate length and 12μm gate width. The scaling of f_t with decreasing gate length is observed. Besides, overall performances disperse according to different channel resistance and device geometry has been also summarized. Additionally, total gate capacitance, stray capacitance and quantum capacitance have been evaluated.

In final, this work provides an reliable graphene transfer and device fabrication techniques which can be another opportunity for further development of GFET on

flexible substrate.

References of Chapter II

[1] D. R. Cooper, B. D'Anjou, N. Ghattamaneni, B. Harack, M. Hilke, A. Horth, N. Majlis, M. Massicotte, L. Vandsburger, E. Whiteway, and V. Yu, " Experimental review of graphene." *ISRN Condensed Matter Physics,* Vol. 2012, no. 501686, pp.1-56, 2012.

[2] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, Jan. 2009.

[3] J.-N. Fuchs and M. O. GOERBIG, "Introduction to the physical properties of graphene," *Lect. Notes*, 2008.

[4] V. N. Kotov, B. Uchoa, V. M. Pereira, F. Guinea, and A. C. Neto, "Electron-electron interactions in graphene: Current status and perspectives," *Rev. Mod. Phys.*, vol. 84, no. 3, p. 1067, 2012.

[5] A. K. Geim, "Graphene: status and prospects," *Science*, vol. 324, no. 5934, pp. 1530–1534, 2009.

[6] A. K. Geim and K. S. Novoselov, "The rise of graphene", *Nature Materials*, vol, 6, pp.183-191, 2007.

[7] Shoab Ahmed Khan, Digital Design of Signal Processing Systems: A Practical Approach, John Wiley & Sons, Ltd. 2011.

[8] ITRSV The International Technology Roadmap for Semiconductors. [Online]. Available: http://www.itrs.net

[9] S. Damaraju, V. George, S. Jahagirdar, T. Khondker, R. Milstrey, S. Sarkar, S. Siers, I. Stolero, and A. Subbiah, ''A 22 nm IA multi-CPU and GPU system-on-chip,'' in *Solid-State Circuits Conference Digest Of Technical Papers (ISSCC)*, 2012, pp. 56–57.

[10] Y. Takahashi, Y. nho, A. Fujiwara and H. Inokawa, "Silicon single –electron devices" *J. Phys Condens Matter*, vol. 14, no. 39 , pp. 995-1033, Oct. 2002.

[11] F. Schwierz, "Graphene transistors," *Nature nanotechnology*, vol. 5, pp. 487-495, May. 2010

[12] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems," *Proc. IEEE,* vol. 101, no. 7, pp. 1567–1584, Jul. 2013.

[13] A. K. Geim, K. S. Novoselov, "The rise of graphene", *Nature Materials*, vol. 6, pp. 183-191. 2007

[14] The International Technology Roadmap for Semiconductors http://www.itrs.net/ Links/2009ITRS/Home2009.htm (Semiconductor Industry Association, 2009).

[15] G. Iannaccone, G. Fiori, M. Macucci, P. Michetti, M. Cheli, A. Betti, and P. Marconcini, "Perspectives of graphene nanoelectronics: probing technological options with modeling," in *IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 245–248.

[16] Z. H. Chen, Y-M. Lin, M. J. Rooks, and P. Avouris, "Graphene nano-ribbon electronics," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 40, no. 2 , pp. 228–232, Dec. 2007.

[17] L. Yang, C.-H. Park, Y.-W. Son, M. L. Cohen, and S. G. Louie, "Quasiparticle energies and band gaps in graphene nanoribbons," *Phys. Rev. Lett*., vol. 99, no. 18, p. 186801, 2007.

[18] P. Gava, M. Lazzeri, A. M. Saitta, and F. Mauri, "Ab initio study of gap opening and screening effects in gated bilayer graphene," *Phys. Rev. B*, vol. 79, no. 16, p. 165431, 2009.

[19] T. Ohta, A. Bostwick, T. Seyller, K. Horn, and E. Rotenberg, "Controlling the electronic structure of bilayer graphene,". *Science*, vol. 313, no. 5789, pp. 951-954, 2006.

[20] V. M. Pereira, A. H. Castro Neto, and N. M. R. Peres, "Tight-binding approach to uniaxial strain in graphene," *Phys. Rev. B*, vol. 80, no. 4, p. 045401, Jul. 2009.

[21] Z. H. Ni, T. Yu, Y. H. Lu, Y. Y. Wang, Y. P. Feng, and Z. X. Shen, "Uniaxial strain on graphene: Raman spectroscopy study and band-gap opening," *ACS Nano*, vol. 2, no. 11, pp. 2301–2305, 2008.

[22] B. Obradovic, R. Kotlyar, F. Heinz, P. Matagne, T. Rakshit, M. D. Giles, M. A. Stettler and D. E. Nikonov, "Analysis of graphene nanoribbons as a channel material for field-effect transistors,". *Appl. Phys. Lett*. vol. 88, no. 14, p. 142102, 2006.

[23] F. Schwierz, & J. J. Liou, Modern Microwave Transistors – Theory, Design, and Performance (Wiley, 2003).

[24] F. Schwierz, and J. J. Liou, "RF transistors: recent developments and roadmap toward terahertz applications," *Solid-State Electron*. vol. 51, no. 8, pp. 1079–1091, 2007.

[25] D. J. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Lett*., vol. 19, no. 10, pp. 385–387, Oct. 1998.

[26] F. Schwierz, H. Wong, and J. J. Liou, Nanometer CMOS. Singapore: Pan Stanford, 2010.

[27] D. Das and J. Appenzeller, ‘‘On the importance of bandgap formation in graphene for analog device applications,’’ *IEEE Trans. Nanotechnol*., vol. 10, no. 5, pp. 1093–1098, Sep. 2011.

[28] P. Wolf, ‘‘Microwave properties of a Schottky-barrier field-effect transistor,’’ *IBM J. Res. Develop*., vol. 14, pp. 125–141, 1970.

[29] D.-H. Kim, B. Brar, and J. A. del Alamo, ‘‘fT ¼ 688 GHz and fmax ¼ 800 GHz in Lg ¼ 40 nm In0:7Ga0:3As MHEMTs with gm max > 2.7 mS/ m,’’ in *Tech. Dig. Int.Electron Devices Meeting*, 2011, pp. 319–322.

[30] D.-H. Kim and J. A. del Alamo, ‘‘30-nm InAs PHEMTs with fT ¼ 644 GHz and fmax ¼ 681 GHz,’’ *IEEE Electron Device Lett*., vol. 31, no. 8, pp. 806–808, Aug. 2010.

[31] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, ‘‘Record RF performance of 45-nm SOI CMOS technology,’’ in *Tech. Dig. Int. Electron Devices Meeting*, 2007, pp. 255–258.

[32] L. D. Nguyen, P. J. Tasker, D. C. Radulescu, and L. F. Eastman, ‘‘Characterization of ultra-high-speed AlGaAs/InGaAs (on GaAs) MODFETs,’’ *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2243–2248, Oct. 1989.

[33] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, and W. A. de Heer, “Record Maximum Oscillation Frequency in C-Face Epitaxial Graphene Transistors,” *Nano Lett*, vol. 13, no. 3, pp. 942-947, Feb. 2013

[34] N. Meng, J. F. Fernandez, D. Vignaud, G. Dambrine, and H. Happy, “Fabrication and Characterization of an Epitaxial Graphene Nanoribbon-Based Field-Effect Transistor,” *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1594-1596, Jun. 2011

[35] G. Deokar, J. Avila, I. Razado-Colambo, J.-L. Codron, C. Boyaval, E. Galopin, M.-C. Asensio, and D. Vignaud, “Towards high quality CVD graphene growth and transfer,” *Carbon*, vol. 89, pp. 82–92, Aug. 2015.

[36] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y. C. Lin, S. Jiang, Y. Huang, and X. Duan, “High-frequency self-aligned graphene transistors with transferred gate stacks,” Proceedings of the National Academy of Sciences, vol. 109, no 29, pp. 11588–11592,2012.

[37] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, “High-speed graphene transistors with a self-aligned nanowire gate,” *Nature*, vol. 467, no 7313, pp. 305-308, sept. 2010.

[38] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Y.-M. Lin, "State-of-the-Art Graphene High-Frequency Electronics," *Nano Letters*, vol. 12, no 6, pp. 3062-3067, jun 2012.

[39] Z. H. Feng, C. Yu, J. Li, Q. B. Liu, Z. Z. He, X. B. Song, J. J. Wang, and S. J. Cai, "An ultra clean self-aligned process for high maximum oscillation frequency graphene transistors," *Carbon*, vol. 75, pp. 249–254, Aug. 2014.

[40] K. Kim, J.-Y. Choi, T. Kim, S. H. Cho, and H. J. Chung, "A role for graphene in silicon-based semiconductor devices," *Nature*, vol. 479, no. 7373, pp. 338-344, nov. 2011.

[41] K. S. Novoselov, V. I. Fal′ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," *Nature*, vol. 490, no. 7419, pp. 192–200, Oct. 2012.

[42] C. Mattevi, H. Kim, and M. Chhowalla, "A review of chemical vapour deposition of graphene on copper," *J Mater Chem*, vol. 21, no. 10, pp. 3324–3334, 2011.

[43] M.Roberto and G.A. Cristina, "Review of CVD Synthesis of Graphene" *Chemical Vapor Deposition*, vol.19, no 10-11-12, pp.297–322, Dec. 2013

[44] T. B. Massalski, H. Okamoto, P. R. Subramanian, L. Kacprzak, "Binary alloy phase diagrams," vol.3, ASM International (1986).

[45] M. Regmi, M. F. Chisholm, G. Eres. "The effect of growth parameters on the intrinsic properties of large-area single layer graphene grown by chemical vapor deposition on Cu," *Carbon*, vol. 50, no. 1, pp. 134–141, Jan. 2012.

[46] S. Bhaviripudi, X. Jia, M. S. Dresselhaus, and J. Kong, "Role of Kinetic Factors in Chemical Vapor Deposition Synthesis of Uniform Large Area Graphene Using Copper Catalyst," *Nano Lett.*, vol. 10, no. 10, pp. 4128–4133, Oct. 2010.

[47] K. Kumar, Y.-S. Kim, and E.-H. Yang, "The influence of thermal annealing to remove polymeric residue on the electronic doping and morphological characteristics of graphene," *Carbon*, vol. 65, pp. 35–45, Dec. 2013.

[48] J. W. Suk, W. H. Lee, J. Lee, H. Chou, R. D. Piner, Y. Hao, D. Akinwande, and R. S. Ruoff, "Enhancement of the Electrical Properties of Graphene Grown by Chemical Vapor Deposition via Controlling the Effects of Polymer Residue," *Nano Lett.*, p. 130319160156007, Mar. 2013.

[49] Z. H. Ni, T. Yu, Z. Q. Luo, Y. Y. Wang, L. Liu, C. P. Wong, J. Miao, W. Huang, and Z. X. Shen, "Probing charged impurities in suspended graphene using Raman spectroscopy," *ACS Nano*, vol. 3, no. 3, pp. 569–574, 2009.

[50] C.-H. Yeh, Y.-W. Lain, Y.-C. Chiu, C.-H. Liao, D. R. Moyano, S. S. H. Hsu, and P.-W. Chiu, "Gigahertz Flexible Graphene Transistors for Microwave Integrated Circuits," *ACS Nano*, vol. 8, no. 8, pp. 7663–7670, Aug. 2014.

[51] A. Badmaev, Y. Che, Z. Li, C. Wang, and C. Zhou, "Self-Aligned Fabrication of Graphene RF Transistors with T-Shaped Gate," *ACS Nano*, vol. 6, no. 4, pp. 3371–3376, Apr. 2012.

[52] C. Lu, Y. Lin, C. Yeh, J. Huang and P. Chiu, "High Mobility Flexible Graphene Field-Effect Transistors with Self-healing Gate Dielectrics," *ACS Nano*, vol. 6, no. 5, pp. 4469-4474, Apr. 2012.

[53] I. Childres, L. A. Jauregui, M. Foxe, J. Tian, R. Jalilian, I. Jovanovic and Y. P. Chen, "Effect of electron-beam irradiation on graphene field effect devices", *Appl. Phys. Lett*, vol. 97, no. 17, p. 173109, 2010.

[54] D. K. Schroder, Semiconductor Material and Device Characterization, WILEY-INTERSCIENCE, 2005.

[55] O. Balci and C. Kocabas, "Rapid thermal annealing of graphene-metal contact," *Appl.Phys.Lett*, vol.101, no.24, p.243105, 2012

[56] E. Watanabe, A. Conwill, D. Tsuya, Y. Koide, "Low contact resistance metals for graphene based devices, Diamond related material," *Diamond and Related Materials*, vol. 24, pp. 171–174, Apr. 2012

[57] H. Zhong, Z. Zhang, B. Chen, H. Xu, D. Yu, L. Huang, and L. Peng, "Realization of low contact resistance close to theoretical limit in graphene transistors," *Nano Res.*, vol. 8, no. 5, pp. 1669–1679, May 2015.

[58] B. C. Huang, M. Zhang, Y. Wang and J. Woo, "Contact Resistance in Top-gated Graphene Field-effect Transistors," *Appl.Phys.Lett*, vol. 99, no. 3, p. 032107, 2011

[59] W. Li, C. A. Hacker, G. Cheng, Y. Liang, B. Tian, A. R. Hight Walker, C. A. Richter, D. J. Gundlach, X. Liang, and L. Peng, "Highly reproducible and reliable metal/graphene contact by ultraviolet-ozone treatment," *J. Appl. Phys.*, vol. 115, no. 11, p. 114304, Mar. 2014.

[60] L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, and C. R. Dean, "One-Dimensional Electrical Contact to a Two-Dimensional Material," *Science*, vol. 342, no. 6158, pp. 614–617, Nov. 2013.

[61] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Appl. Phys. Lett.*, vol. 97, no. 14, p. 143514, 2010.

[62] A. Venugopal, L. Colombo, and E. M. Vogel, "Contact resistance in few and multilayer graphene devices," *Appl. Phys. Lett.*, vol. 96, no. 1, p. 013512, 2010.

[63] F. Xia, V. Perebeinos, Y. Lin, Y. Wu & P. Avouris, "The origins and limits of metal-graphene junction resistance," *Nature Nanotechnology*, vol. 6, no. 3, pp. 179–184, 2011

[64] A. K. Geim, K. S. Novoselov. "The rise of graphene," *Nature Material*, vol. 6, no. 3, pp. 183-191, 2007

[65] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos and A. A. Firsov, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature*, vol. 438, no. 7065, pp. 197-200, 2005

[66] A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. W. Magnuson, S. McDonnell, L. Colombo, E. M. Vogel, R. S. Ruoff, and R. M. Wallace, "The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO2" *Appl. Phys. Lett*, vol. 99, no. 12, pp. 122108, Sep. 2011

[67] S. Ryu, L. Liu, S. Berciaud, Y. J. Yu, H. Liu, P. Kim, G. W. Flynn, and L. E. Brus, "Atmospheric Oxygen Binding and Hole Doping in Deformed Graphene on a SiO2 Substrate" *Nano Lett*, vol. 10, no. 12, pp. 4944-4951, Nov. 2010

[68] Han Wang, A. Hsu, Jing Kong, D. A. Antoniadis, and T. Palacios, "Compact Virtual-Source Current-Voltage Model for Top- and Back-Gated Graphene Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1523–1533, May 2011

[69] J. Zheng, L. Wang, R. Quhe, Q. Liu, H. Li, D. Yu, W. Mei, J. Shi, Z. Gao and J. Lu, "Sub-10 nm Gate Length Graphene Transistors: Operating at Terahertz Frequencies with Current Saturation," *Scientific Reports*, vol. 3, no. 1314, pp. 1-9, Feb. 2013

[70] Y. Wu, Y. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon" *Nature*, vol. 472, no. 7341, pp. 74-78, Apr. 2011

[71] J. Xia, F. Chen, J. Li, and N. Tao, "Measurement of the quantum capacitance of graphene," *Nat. Nanotechnol.*, vol. 4, no. 8, pp. 505–509, Aug. 2009.

Chapter III

On flexible substrate: bottom gate graphene field effect transistor with dielectric of natural oxide

Table of Content-Chapter III

Chapter III On flexible substrates: bottom gate graphene field effect transistor with dielectric of natural oxide

III.1 Introduction

Graphene is highly suitable for flexible electronics due to the excellent electronic and mechanical properties which derive from its truly two-dimensional nature. Thanks to its inherent mechanical robustness and flexible nature, large area monolayer graphene can be transferred to flexible substrate. Graphene flexible transistors have been recently achieved.

In this chapter, we present the fabrication and characterization of GFETs on flexible substrate. Since the fabrication process is almost transplanted from what we do on rigid substrate, only the parts with new modification will be highlighted. For example, the greatest challenge in fabrication work is mis-alignment of electro-beam lithography process caused by the non-flat surface of flexible substrate. So we make a stable bonding between flexible substrate and rigid wafer to keep the flexible substrate flat. With the modified fabrication process, transistors with different geometry (gate length of 100, 200 and 300 nm combining with gate width of 12, 24 and 50 μm) are realized on flexible substrate. Both static and dynamic measurements of the devices are carried out. Besides, the evolution of device performance according to different substrate strain (varying from 0% to 0.5%) is evaluated, and the thermal dispersion of substrate in channel region for different drain source bias is explored.

III.2 General description of flexible GFET

Two-dimensional material is bendable, and thus it has drawn enormous attention recently for the application of flexible devices. For example, the strain limit of graphene has been reported to be more than 20% [1][2]. The large area grown graphene can be transferred from its host substrate onto flexible substrate without seriously degrading the high value of mobility. Graphene with high mobility on flexible substrates have been reported[3-15]. For example, electron mobility of 12000 $cm^2V^{-1}s^{-1}$ and hole mobility of 13000 $cm^2V^{-1}s^{-1}$ have been reported for CVD grown graphene transferred to PEN substrates[8]. Thanks to this, radio frequency GFETs on flexible substrate has been reported. Among all these reports, GFETs with both top gate and bottom gate have been realized.

Figure III-1(a) shows the top gate structure GFET from the work of [16]. T-gate is used and self-aligned source/drain contacts is realized. The dielectric (AlO_X) between top gate and graphene is formed by a natural self-oxidation of Al. They report extrinsic cutoff frequency of 32 GHz and maximum oscillation frequency of 20 GHz. Figure III-1 (b) and (c) show the bottom gate structure GFET from the work of ref[17] and ref[18], respectively. The difference between these two works is the dielectric formation. In ref[17], dielectric of 6 nm HfO_2 is grown by atomic layer deposition (ALD), while in ref[18], dielectric of 10 nm Al_2O_3 is grown by ALD. Ref[17] reports 23.6 GHz of f_t and 6.5 GHz of f_{max} before de-embedding. Ref[18] reports 3.1 GHz of f_t and 2.1 GHz of f_{max}.

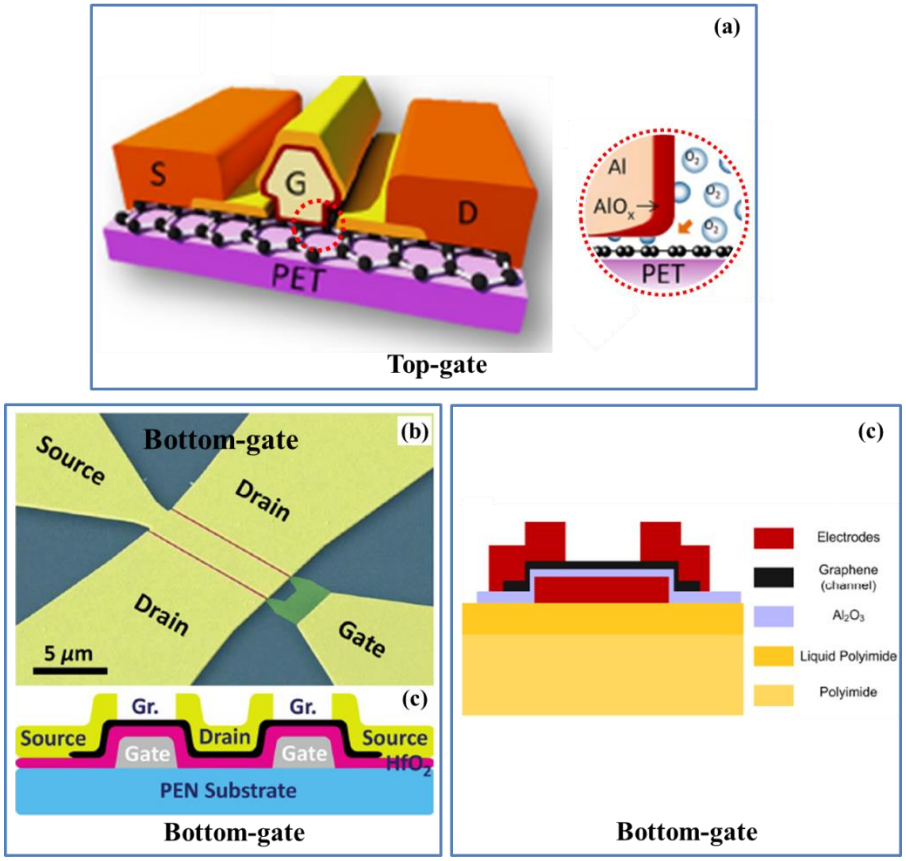


Figure III-1:illustration of different GFETs structures reported before, in (a), from [16], transistor with T-shaped top gate and self-aligned deposited source & drain contact, the inset zoomed-in image illustrates the occurrence of Al natural oxidation in the interface between gate and graphene; in (b-c), from [17], top view and cross section schematics of bottom gate transistor with dielectric of HfO_2 deposited by ALD; in (c), from [18],cross section schematics of bottom gate transistor with dielectric of Al_2O_3 deposited by ALD

Figure III-2 shows the GFET structure designed in this work. The bottom gate structure was used in order to further reduce the possibility of degrading the graphene mobility due to electron irradiation which would happen in directly e-beam writing on the top of graphene channel[19]. The dielectric of Al_2O_3 was formed by natural oxidation of aluminum, with thickness of 4.3 nm which was confirmed by spectroscopic ellipsometer (discussed in chapter 2). Our process avoids deposition process of dielectrics by ALD, which greatly reduces the risk of damaging flexible substrate, thus provides an easy alternative fabrication method for future flexible electronics. To our best knowledge, our GFET structure (bottom gate with natural oxide of Al_2O_3 as dielectric) has not been reported before.

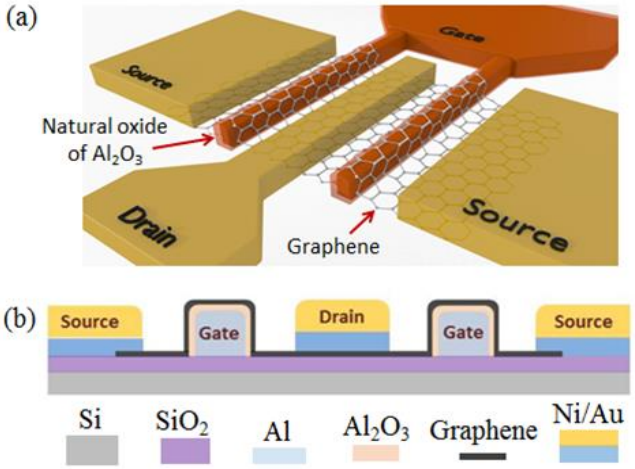


Figure III-2:bottom gate with natural oxide of Al2O3 transistor structure in this work, (a) Schematic of GFET device; (b) cross section schematic of a GFET device

III.3 Device fabrication process and graphene characterization on Kapton substrate

This section will discuss the fabrication process of bottom gate GFETs with CVD grown graphene on flexible substrate. Because the techniques applied for flexible GFETs are almost transplanted from what has been discussed for rigid GFETs in chapter 2, the identical parts will be skipped. Here, with the same structures, bottom gates with natural oxidation as dielectric; and also with the same device geometry, gate length of 100, 200 and 300 nm combining with gate width of 12, 24 and 50 μm, have all been realized on flexible substrate of Kapton. Besides, together with the GFETs devices, other components such as Hall effect structures, TLM structures and de-embedding structures of "pad" and "mute" have also been completed in the same time. Figure III-3 shows the design from layout, and the complete structures.

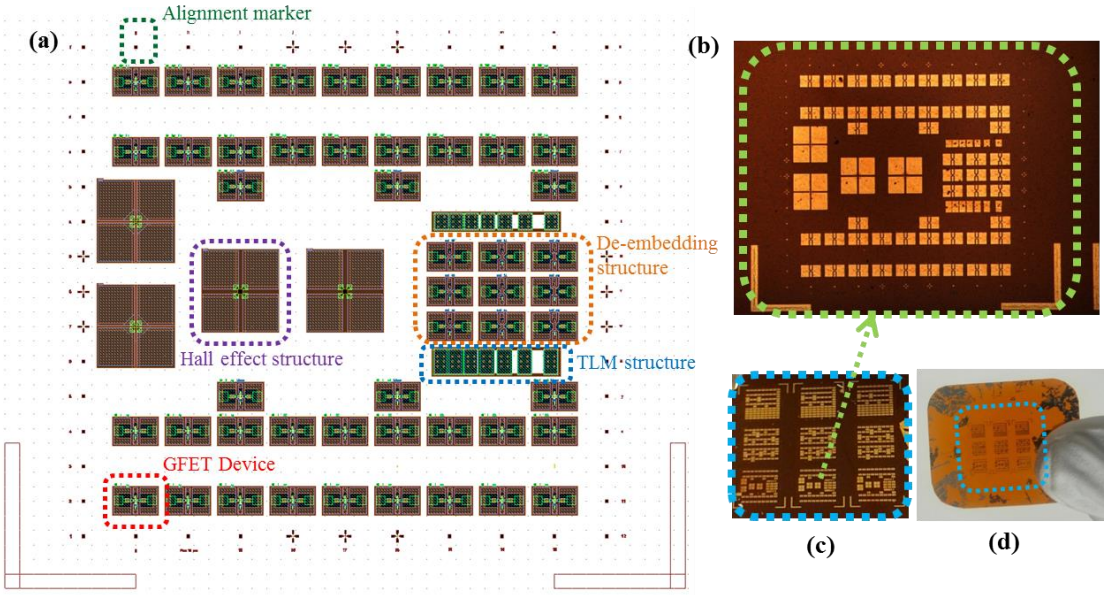


Figure III-3:(a) pattern design of transistors with all the other structures in layout; (b) optical image of a final completed structures according to the design; overview of all the devices in (c) and with kapton substrate in (d)

The main challenge for GFETs devices fabrication on flexible substrate is to overcome the errors or instabilities of electron-beam lithography (EBL) alignment procedure due to the rough and fluctuating surface of flexible substrate. The solutions we adopted include two things. First, prior to device fabrication, the flexible substrate was bonded onto a rigid substrate, a silicon wafer for instance, to keep the surface relatively flat. Second, the device map was designed to be smaller (as compared to what is on rigid substrate) so that the reduced distance between two furthest alignment

markers (four alignment markers with furthest distance between each other will be used for EBL alignment procedure) can help to improve the alignment precision.

III.3.1 Optimization of alignment process

As mentioned above, the biggest challenge of GFETs fabrication on flexible substrate is the crucial accuracy of alignment process between each step. In layout design, we have introduced cross-shaped structure to examine the alignment process. As shown in Figure III-4, these cross-shaped structures have been designed in four sides of one EBL writing field for the most critical device fabrication steps: bottom gate, graphene isolated pattern etching and drain & source deposit. In this way, we are able to fully examine the alignment process between different steps. Before the optimization work, we have failed many samples because of the poor alignment process, and Figure III-4 (b) and (c) shows an example. We have observed an obvious shift of the cross-shaped structure from its right position, and the shift of device structure due to this failed alignment process.

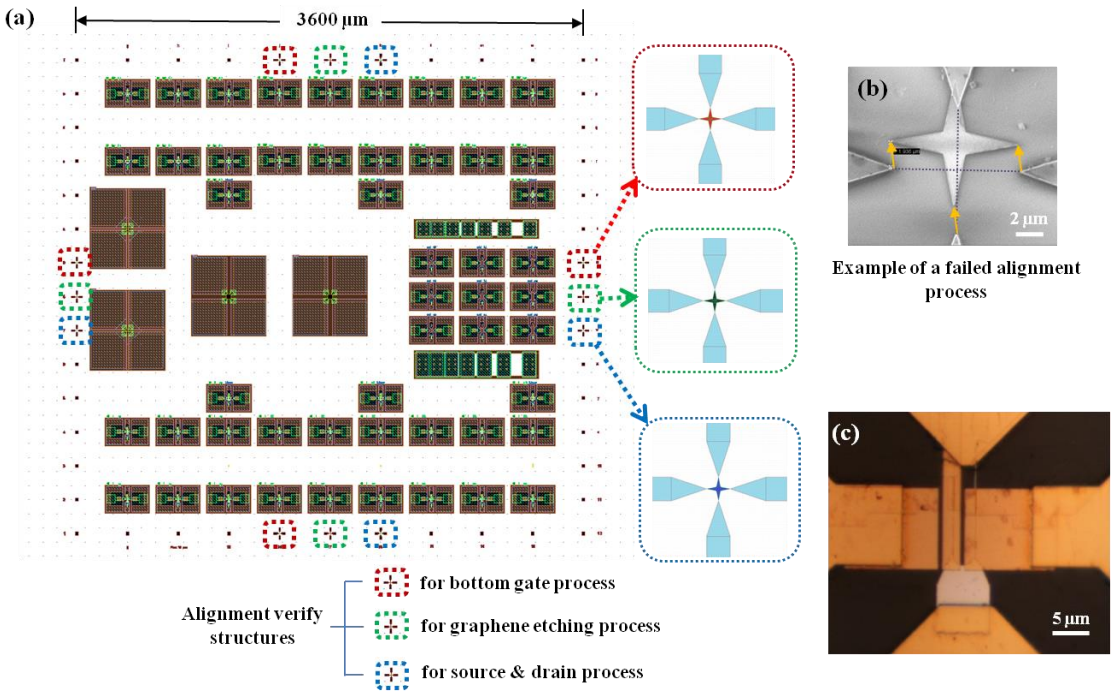


Figure III-4:(a) layout design of device map with alignment testing structure, which are marked by different color (red, blue and green) representing different layer process; (b) an example of failed alignment process reflected by testing structure; (c) an example of a failed device due to the poor alignment process

Figure III-5 shows the SEM images of the cross-shaped structures in their right positions thanks to our improved alignment process.

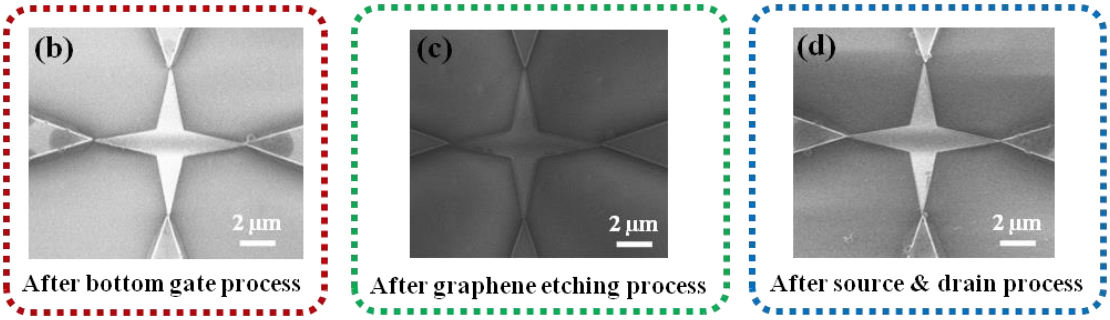


Figure III-5:SEM image of alignment testing structure verified by good alignment process

We have compared the offset value of cross-shaped structures from all the fabrication process, before and after optimizing the alignment process. Figure III-6 shows the statistic results. It can be seen that thanks to the optimization, the offset value between two electro-beam writing steps has been largely reduced.

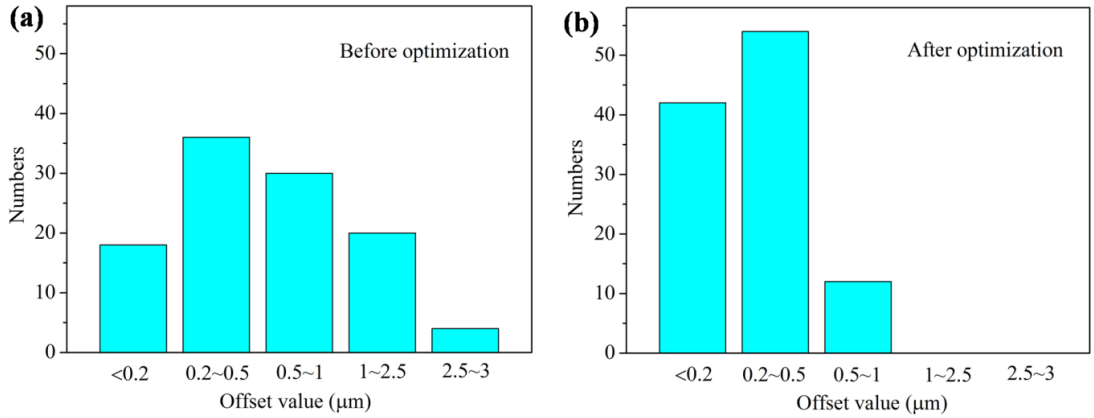


Figure III-6:Statistic offset value from all the fabrication process in (a) results from fabrication before optimization; (b) results from fabrication after optimization. Less offset value are observed after the process is optimized

III.3.3 Device fabrication process

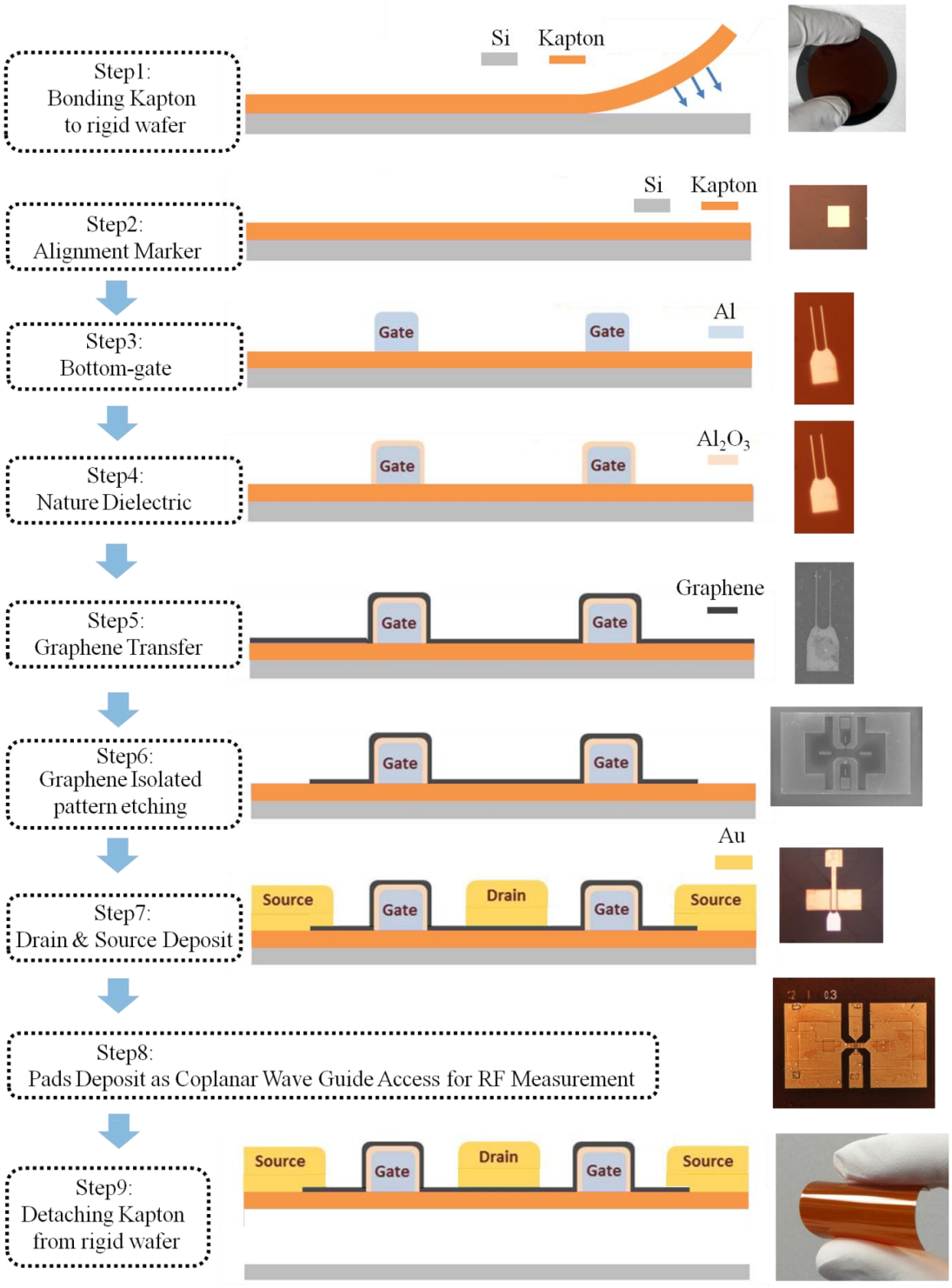


Figure III-7:General fabrication process for GFETs on flexible substrate, Kapton

The general description of the whole device fabrication process is provided in Figure III-7. Since the most parts of the fabrication process are transplanted from the process discussed in Chapter 2, only the different steps will be discussed, these steps are: Step 1, bonding Kapton with rigid substrate; step 6, graphene isolated pattern

etching; step 7, drain source deposit and step 9, detaching Kapton from rigid substrate.

Step1: Bonding Kapton with rigid substrate

The major challenge for GFETs devices fabrication on Kapton is the non-flat surface due to the nature of plastic material. This non-flat state is not compatible with the conventional device fabrication system. For example, the metal evaporation system requires a flat target substrate so that the thickness uniformity of deposited metal can be guaranteed; and also the EBL system requires flat enough substrate, otherwise the focus of electron beam occurrs at different height levels and the precision of pattern writing suffers. Therefore, the first task is to make Kapton substrate as flat as possible. We choose to bond Kapton with a silicon wafer (or any other rigid flat substrate) so that the Kapton can be relatively as flat as the wafer. Here, the bonding between wafer and Kapton has to meet two conditions: 1) to stand with the chemical products used in this work (Acetone, IPA, MIBK, BOE, H_2O_2, etc); 2) possible to detach Kapton from wafer when fabrication process is finished. Different bonding materials and methods have been tested, and Table III-1 gives the remarks of the experimental results. Finally, PDMS and commercial tape have been selected to bond Kapton due to their excellent stability with the presence of Acetone. Acetone is found to be the most aggressive chemical product to bonding materials in this work. Note that the bubbles in bonding material must be well controlled, because in any vacuum system (plasma, metal evaporation, EBL etc) these bubbles will inflate and thus damage the bonding layer. Because bonding strength of both PDMS and commercial tape comes from physical attraction and no chemical bonding is generated, the Kapton can be easily peeled off from wafer by using tweezer without using any special chemical product.

Table III-1: Bonding experiments

Materials	**Treatment**	**Result**
Eb-resist, COPO MAA8.5 EL6%	Spin-coat, stick, and bake	No resistance to lift-off, big bubbles
ParyleneC	CVD, plasma , bonding machine	<3h resistance to lift-off, no bubbles
Su8	Soft baking, bonding machine	<5h resistance to lift-off, no bubbles
PDMS	Pump to remove bubbles	>6h resistance to lift-off, bubbles controlled
Double sides tape	no	>6h resistance to lift-off, no bubbles

Step6: Graphene isolated pattern etching

For step of graphene etching on flexible substrate, where the bottom gates have been covered by monolayer graphene, the same oxygen plasma recipe (50w, 25sccm, 100 mTorr and 2min) as mentioned in chapter 2 was used. After oxygen plasma etching, we find that not only the graphene, but also the substrate of Kapton have been etched. Figure III-8 (a) shows the SEM image of bottom gate with graphene isolated pattern after oxygen plasma etching; (b) and (c) show the Atomic force microscopy (AFM) image illustrating substrate height difference caused by etching. Verified from AFM measurement, the Kapton substrate has been etched around 70 nm after our graphene etching process.

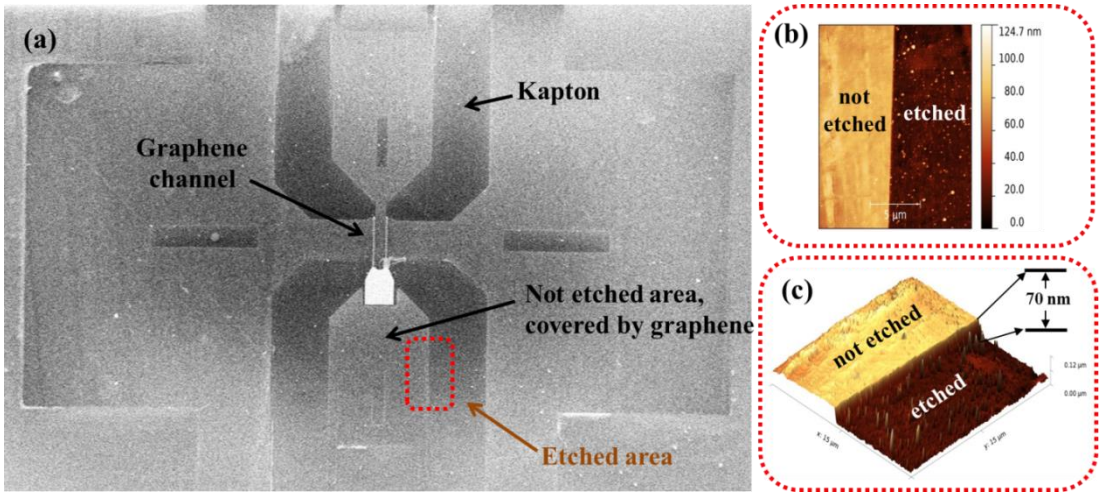


Figure III-8:(a) SEM image of device after the process of graphene isolated pattern etching; (b) and (c) the AFM image of the red rectangle marked region in (a), indicating the Kapton substrate is etched of 70 nm due to graphene etching process

Step7: Drain source deposition

The drain source contacts fabrication process is the same as the process on rigid substrate as discussed in chpter2, except that the contact material is different. Instead of Ni/Au (20/30nm) on rigid substrate, pure Au of 50 nm in thickness has been used as drain and source contact metal for flexible samples. The adhesion strength of gold to substrate or gold to graphene is an important issue to be considered. Because Au has relatively poor adhesion strength with Si or SiO_2. Therefore, in this work, pure gold is only used to contact graphene in the region of drain and source, and it has been afterwards firmly fixed by pads pattern, as shown in Figure III-9. The same process as rigid sample, Ni/Au of 50/300 nm in thickness have been deposited for pads on Kapton substrate, the strong adhesion between Ni and Kapton has been afterwards confirmed by on chip DC and RF measurements. The probes can be easily placed on the pads without any observation of device movement with probes.

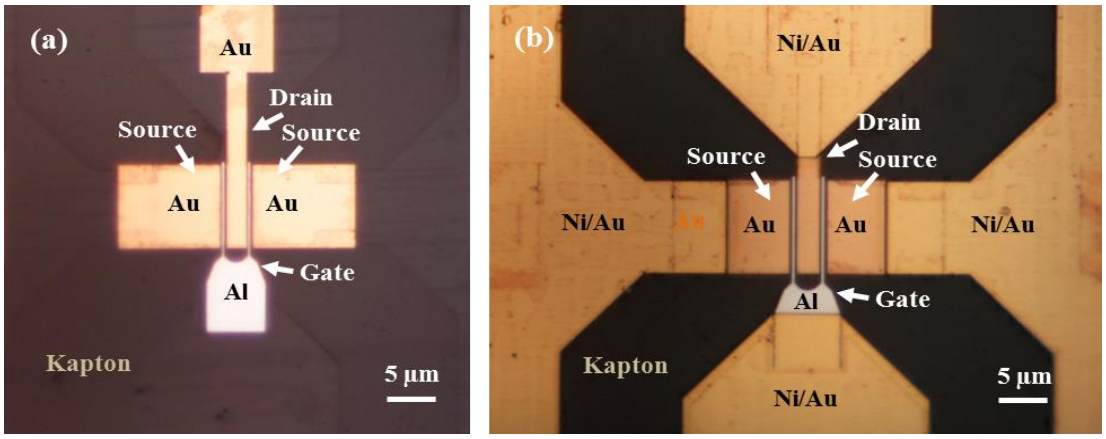


Figure III-9:(a) transistor after process of depositing pure Au drain & source contacts; (b) transistor after process of depositing coplanar wave guide access as pads for measurement (Ni/Au 50/300nm)

Step 9: Detaching Kapton from rigid substrate

When all the fabrication process are complete, the Kapton will be carefully removed from silicon wafer. A gentle force has been applied by using a tweezers from one side of the kapton to lift it up. Figure III-10 shows the schematic of this detaching process.

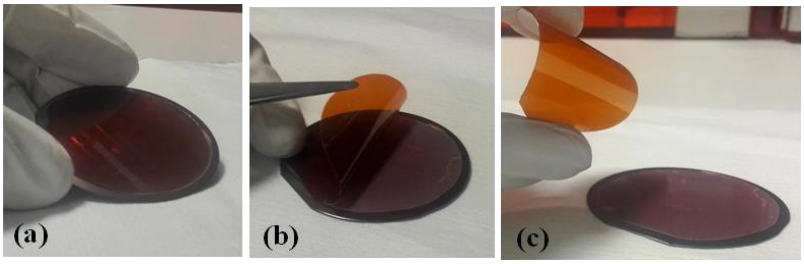


Figure III-10: illustration of detaching Kapton from silicon wafer, in (a) the Katpton as stick on wafer; (b) the kapton is detached carefully by tweezers; (c) Kapton is successfully detached from wafer

Final device images

Figure III-11 shows optical images of complete devices with different gate width *W* (12, 24 and 50 µm) on Kapton substrate. By solving the difficulties of alignment process, plastic substrate etched by using oxygen plasma, bonding and detaching the Kapton with silicon wafer, which are all discussed as before, the final GFETs structures have been proved to be fully achievable. Even the structure with gate length of 100 nm and gate width up to 50 µm has been found well patterned. We have demonstrated a feasible GFETs fabrication process based on flexible substrate.

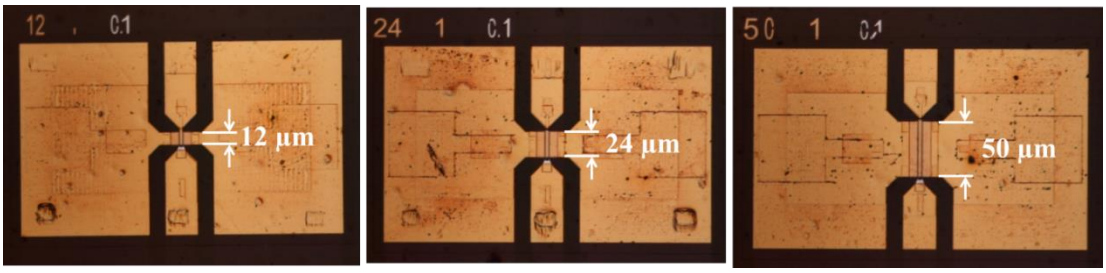


Figure III-11:Optical images of transistors fabricated on Kapton, with different gate width of 12, 24 and 50 µm

III.4 Characterization of material and contact resistance

Prior to explore the GFETs performance in DC and RF regime, we firstly study the transport properties in terms of mobility measurement and the contact resistance for the unique case here: graphene on flexible substrate of Kapton. These information will help us to understand the flexible transistors performance, such as f_t and f_{max}, especially as comparing to the GFETs on rigid substrate reported in chapter 2.

III.4.1 Graphene mobility on Kapton substrate

Hall effect measurement was carried out by using Van der Pauw method. Figure III-12 shows the Hall effect structures fabricated on Kapton.

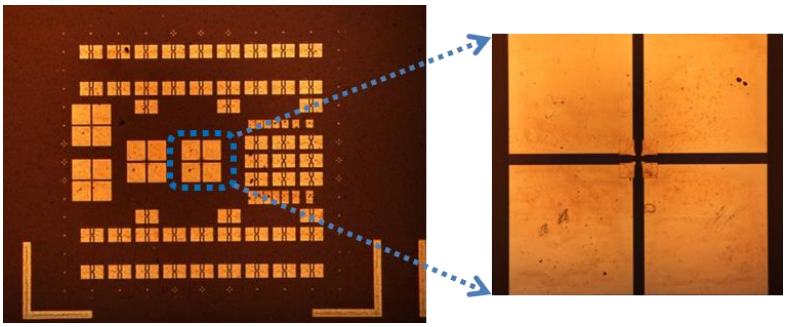


Figure III-12:Optical image of Hall effect structure (Van der Pauw) on kapton substrate

Table III-2:Comparison of informations obtained from Hall measurement of different samples

Sample (Graphene source)	Substrate	Hall structure	Sheet resistance (ohm/sq)	Doping type & Carrier density (cm^{-2})	Hall Mobility (cm^2/Vs)
Si07 (Cambridge)	Si/SiO_2	VDP HB	900	$+ 4.3 \times 10^{12}$	1900
Si08 (IEMN)	Si/SiO_2	VDP	1500	$+ 1.3 \times 10^{12}$	3200
Si09 (Korea)	Si/SiO_2	VDP	1600	$+ 1.2 \times 10^{12}$	3400
Si10 (IEMN)	Si/SiO_2	VDP	1000	$+ 2.6 \times 10^{12}$	2800
Kap10 (Spain)	**Kapton**	**VDP**	**900**	**$+ 2.7 \times 10^{12}$**	**2500**

VDP: van der pauw structure; HB: Hall bar structure

III.4.2 Graphene contact resistance

We have developed three types of TLM structures for samples with rigid substrate, Pattern of A, B and C, which have been carefully discussed in chapter 2. For sample Kap10 with flexible substrate, only pattern A has been used to extract graphene contact resistance. Because Kapton will be also etched during graphene etching process, to realize Pattern B and Pattern C become quite complicated. Like the Pattern A on rigid substrate, the same structure dimensions have been realized here: two different contact width, 100 µm and 160 µm, with separation length between two adjacent contacts which are 2, 5, 10, 20, 40 and 80 µm. The only difference is the contact metal, instead of Ni/Au (20/30 nm) used for rigid substrate, pure Au of 50 nm in thickness has been used here to contact graphene. Figure III-13 (a) shows the structure with contact width of 100 µm. Figure III-13 shows the measured resistance with error bar (average value of three TLM patterns measured results) and the linear fitting compared to the results obtained from rigid substrate with contact width of 160 µm in (b) and 100 µm in (c). For both contact width of 160 and 100 µm, we see the significant drop of resistance for each channel from sample Kap10 as compared to sample Si08. Because of the identical TLM structures from both samples of Si08 and Kap10 (the same channel width and length), we believe that the resistance decreases mainly results from much lower contact resistance by using pure Au. As expected, from the two TLM structures with different channel width, the contact resistance deduced from the linear fitting is 190 Ω·µm (160 µm channel width) and 580 Ω·µm (100 µm channel width) respectively. More information obtained from TLM measurement are presented in Table III-3.

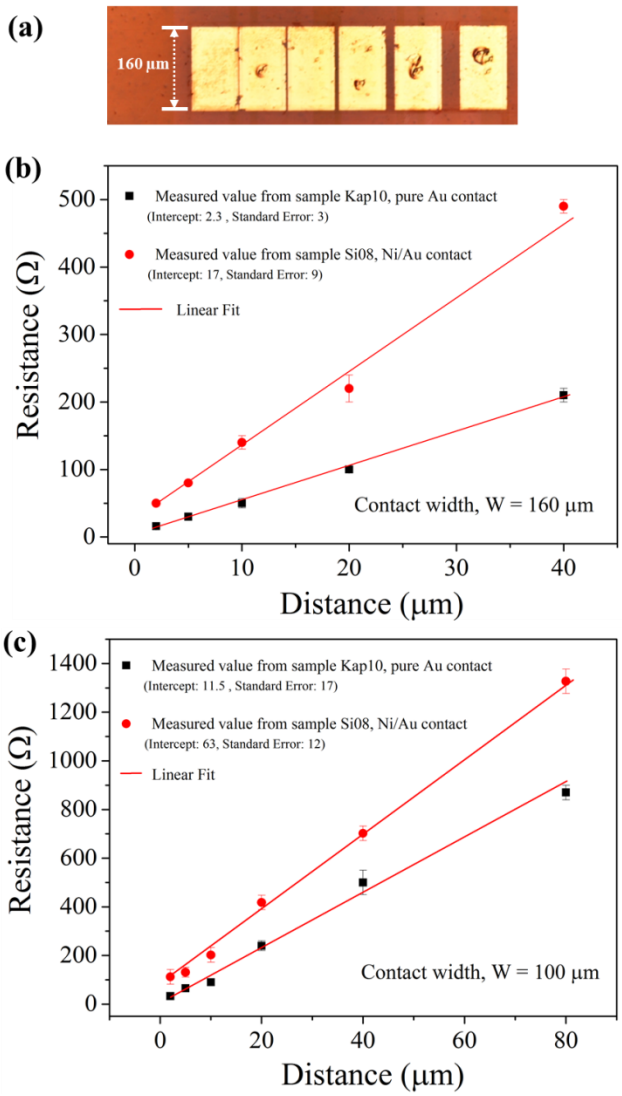


Figure III-13:(a) Optical image of a TLM structure on Kapton substrate, with contact width of 160 µm; Comparison of TLM results between sample Kap10 (metal contact of pure Au) and sample Si08 (metal contact of Ni/Au) with contact width of 160 µm in (b) and with contact width of 100 µm in (c).

Table III-3:Information obtained from TLM structures in sample of Kap10

Sample **Contact Metal**	**W** **(µm)**	**R_CW** **(Ω µm)**	**L_T** **(µm)**	**$\rho_{\square}$** **(Ω/□)**	**E**	**homogeneity**
Kap10 Au (50nm)	160	190	0.3	1200	3	√
Kap10 Au (50nm)	100	580	0.5	1050	17	√

E: Standard error of linear fitting √: Good

III.5 Characterization of GEFTs devices

In this section, the electrical characterization of GFETs with different dimensions (gate length and gate width) fabricated on flexible substrate of Kapton will be discussed. We will start from DC behavior of our GFETs, i.e. out-put and transfer characteristic. The dimensions-dependent performance will be presented both from some typical devices and statistical analyses. The result obtained in DC will help to well explore RF performance. Additionally, a comparison (in terms of channel resistance, transconductance, etc.) between GFETs on flexible and rigid substrate will be provided.

The RF measurement is carried out by a vector network analyzer (with frequency range from 0.1 to 67 GHz), which allows to superimpose high frequency signal to the gate in form of voltage with low amplitude (small signal regime). Microwave transistors figures of merit, the current gain $|H_{21}|$ (in terms of f_t) and unilateral gain U (in terms of f_{max}), of the GFETs with different geometry will be fully discussed. Importantly, to explore the performance of our GFETs when different strain were applied to the flexible substrate, the RF characterization with substrate bended on different radius supporter (strain varies up to 0.5%) is carried out. In further, the thermal dispersion of the flexible substrate in channel region with different drain source bias is explored since the thermal sensitivity of flexible substrate is a major issue to be considered.

III.5.1 DC Characterization when substrate is flat

There are nearly 100 GFETs devices from sample Kap10 have been characterized. More than 80% of them have been found to be functional. For different device dimension (gate length of Lg = 100, 200, 300 nm and gate width of W= 12, 24, 50 μm), the best performance will be presented, and also a statistic of the performance dispersion will be provided.

III.5.1.1 Transfer characteristic and transconductance

This DC measurement was carried out at room temperature with an Agilent DC parametric Analyzer (E5260B) in the static mode. Similar to chapter 2, the transfer characteristic in both low bias (10mV) and high bias (300 mV and 500 mV) will be presented.

In low Vds bias of 10 mV

Figure III-14(a), (b) and (c) shows for GFETs with different gate width (12, 24

and 50 µm) but with the same gate length (100 nm), the gate modulation over drain to source resistance including the contributions from both graphene channel and metal contacts which were obtained from low bias of 10mV Vds. Because the curve of *drain source resistance vs gate voltage* is deduced from *drain source current vs gate voltage*, we will find the Dirac point in Vgs where has the maximum drain source resistance. As shown in Figure III-14, for devices with different gate width, the Dirac points are all found in positive branch of gate voltage, which indicates the p-doped graphene on Kapton substrate. This result agrees well with the conclusion in chapter 2, which is due to CVD grown graphene and its transfer process. This p-doped behavior observed here is also in good agreement with Hall effect measurement in previous section. Furtherly, the gate modulation over the total resistance are found very superior. It is worthy to note that variation of total resistance contains the contribution from both graphene channel and graphene metal contact. Figure III-14(d) shows the distribution of drain to source resistance normalized by gate width from devices with all different geometry. The resistance variation can be caused by non-homogeneity of graphene quality and graphene metal contact. Importantly, as comparing to the same statistic study from rigid substrate (Figure II-47), the overall resistance distributions on flexible substrate are much smaller. This is mainly due to the much lower contact resistance obtained on flexible substrate by pure Au.

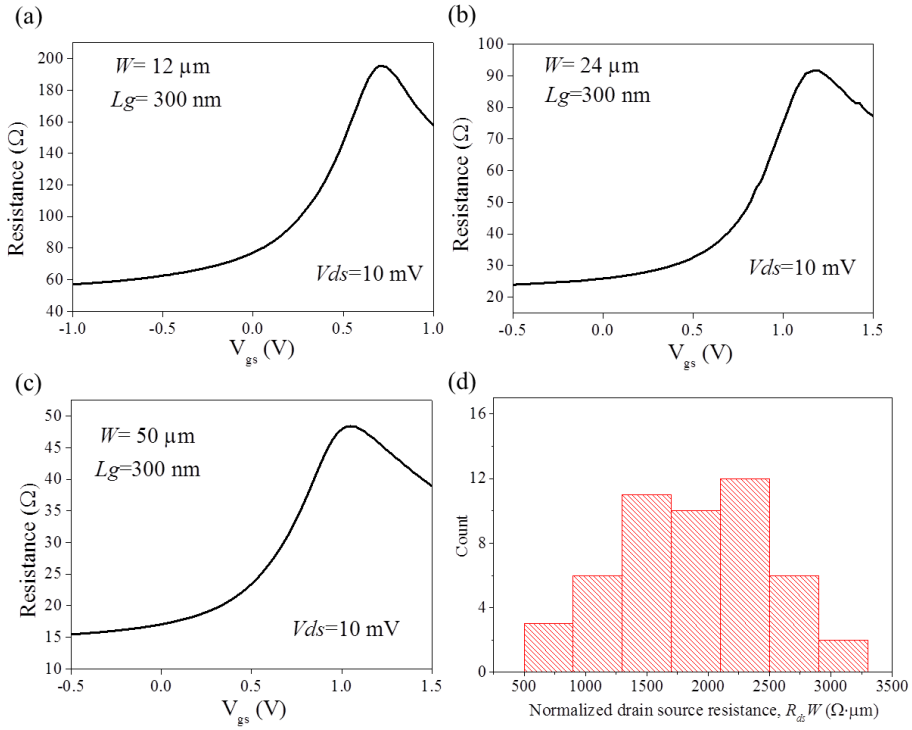


Figure III-14:DC transport characteristics of the device with gate length of 300 nm at Vds = 10 mV, drain to source resistance vs gate voltage for devices with gate width of 12, 24 and 50 µm in (a), (b) and (c); in (d), distribution of drain to source resistance normalized by gate width from all the devices with different geometry.

In high Vds bias of 500 mV

Higher bias with Vds of 300 mV and 500 mV have been then applied to explore the transconductance, gm. Figure III-15(a) shows the transfer characteristic and the deduced gm with 500 mV bias for transistor with 12 µm gate width and 100 nm gate length. The maximum absolute gm value of 3 mS is obtained in the hole branch, which is due to the contribution of high holes density of our p-doped graphene. Therefore, for our devices on flexible substrate we mostly explore the hole branch. Figure III-15(b) shows the leakage current through the dielectric (4.3 nm Al_2O_3 natural oxidation, as discussed in chapter 2) is very low, i.e. in the order of nA for both bias of 10 mV and 500 mV. It demonstrates the good quality of the natural oxidation layer formed on flexible substrate in this work.

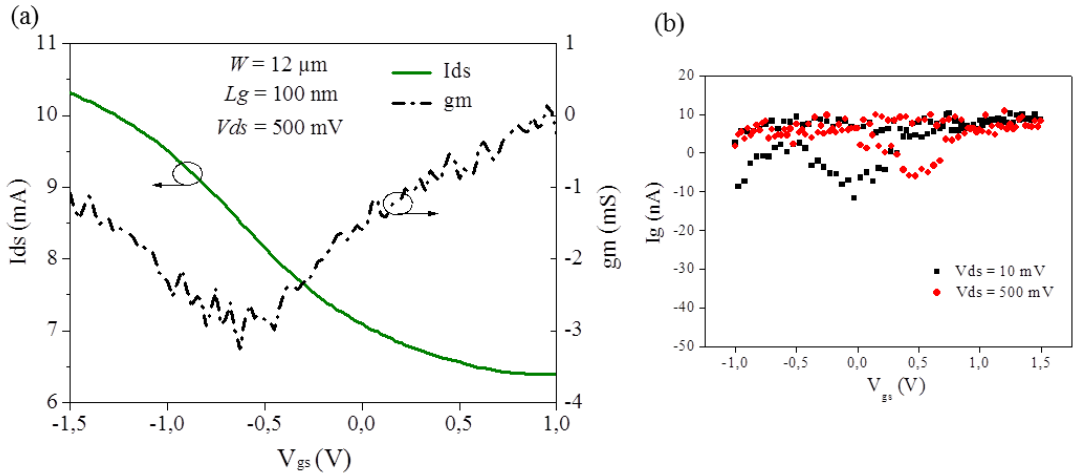


Figure III-15:(a) transfer characteristics with gm deduced with Vds of 500 mV; (b) leakage current through the gate

Table III-4 gives the measured gm (summarized as an average value without normalizing by gate width, an average value normalized by gate width, and the best individual value) for devices with different geometry in light of gate width W and gate length Lg. We find that the value of gm decreases slightly with the gate length decreasing for all the three gate width devices. We believe that this can be attributed to the competition between decreases of effective gating area and the increase of the non-gating area, which has been carefully discussed in chapter 2. We also noticed that as comparing to the results obtained from rigid sample (Table II-14), the gm are generally increased. We believe that the improvement of gm is partially due to the higher effective channel voltage, Vch, thanks to the lower value of contact resistance. Although the drain to source voltage applied on sample Kap10 is 500 mV, only half of the value applied for devices on rigid substrate (1V), the voltage drops on graphene channel (channel voltage) becomes another case here because of the different contact

resistance. Taking the device with 300 nm gate length, 12 µm gate width and 1 µm drain to source separation for example, let's first consider the devices on rigid substrate. With contact resistance of 2000 Ω· µm, and graphene sheet resistance of 1500 Ω/□, the channel voltage is estimated around 90 mV when drain to source voltage of 1V is applied. For devices on flexible substrate, with contact resistance of around 200 Ω· µm and graphene sheet resistance of 1200 Ω/□, the channel voltage is estimated around 120 mV when drain to source voltage of 500 mV is applied.

Table III-4: Evolution of gm for devices with different geometry, with Vds of 500 mV

W (µm)	L_g (nm)	g_m average mS	g_m average µS/µm	g_m best mS
12	100	1.6	130	3.2
	200	2.8	233	3.7
	300	2.9	241	4.2
24	100	3.8	158	7.1
	200	6.1	254	11
	300	9.2	383	9.7
50	100	4.4	88	9.6
	200	7.4	148	8.8
	300	11.3	226	14.5

III.5.1.2 Output characteristics

We use Agilent DC parametric Analyzer (E5260B) to explore the drain source current Ids as a function of both drain voltage Vds and gate voltage Vgs. Figure III-16 shows the output curves from devices with the same gate length (Lg=100 nm) but with different gate width (W= 12, 24 and 50 µm). In Figure III-16 (a), the transfer characteristic has been provided in Figure III-15. The range of Vgs was selected from the hole branch observed from transfer characteristic to cover the best gm value. In the same way, Figure III-16 (b) and (c) presents the output curve based on the same analysis. Note that the drain current shown in Figure III-16 are not normalized by gate width. After normalization (divided by gate width), the drain current reaches a maximum value of 900, 850 and 360 µA/µm for device with gate width of 12, 24 and 50 µm respectively, at Vds of 500 mV and Vgs of -1.5 V(for W=12 µm) and -0.5V (for W=24 and 50 µm). We also observe the tendency of current saturation, in the higher

Vds region. This is believed mainly due to the low contact resistance obtained for these devices [20][21].

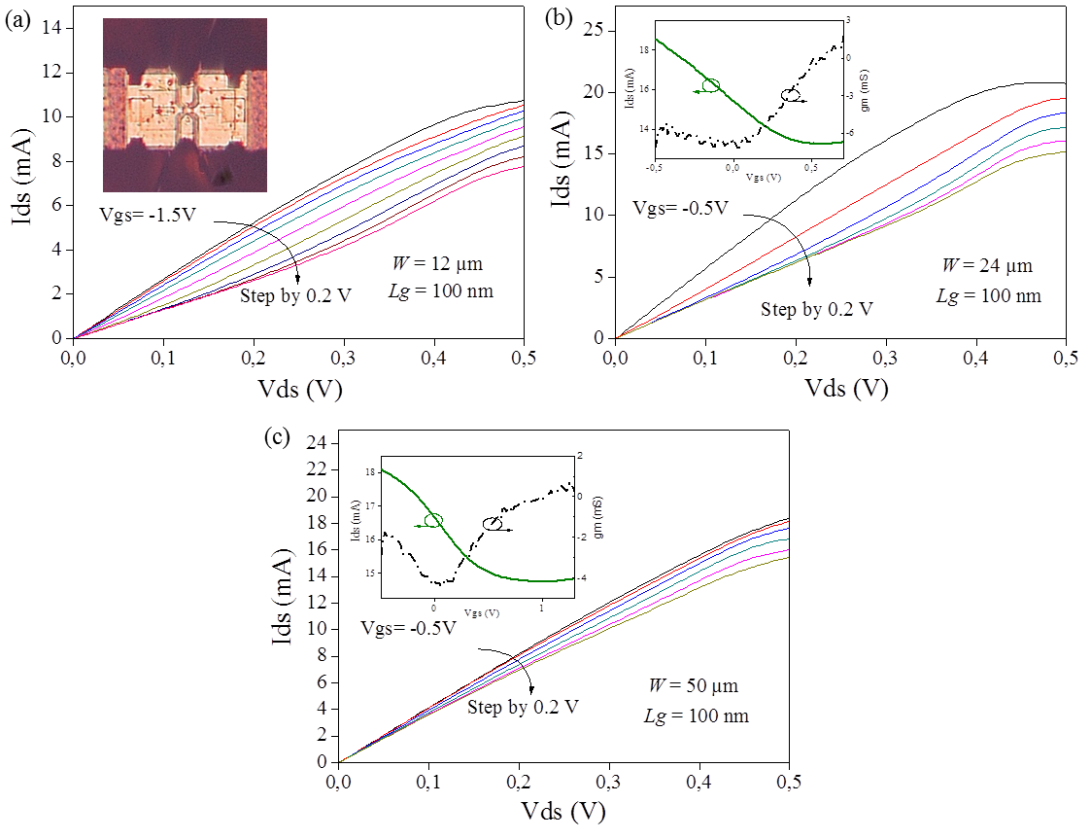


Figure III-16:Output characteristic of devices with 100nm gate length and gate width of (a) 12 µm, the inset image shows a final device with probes on its coplanar wave guide access; (b) 24 µm; and (c) 50 µm, both with an inset image of showing its transfer characteristic with Vds of 500 mV.

III.5.2 Small-signal high frequency characteristics when substrate is flat

The high frequency performance of our flexible GFETs have been characterized by using the PNA Network Analyzer (Agilent E8361A) under ambient conditions in the frequency range of 0.1 ~ 67 GHz. The calibration procedure has been mentioned in chapter 2.

III.5.2.1 Current gain, |H21|

Figure III-17 shows the best value of current gain for devices with different gate length and gate width. The best performance of cut-off frequency is found to be 39 GHz for device with 100 nm gate length and 12 µm gate width. We also find good result of 35 GHz f_t from device with 100 nm gate length and 24 µm gate width. To our best

knowledge, these performances are approaching to the state of art for GFETs, especially considering the fact that no de-embedding procedure in our results. It indicates the great potential of our fabrication scheme for flexible GFETs.

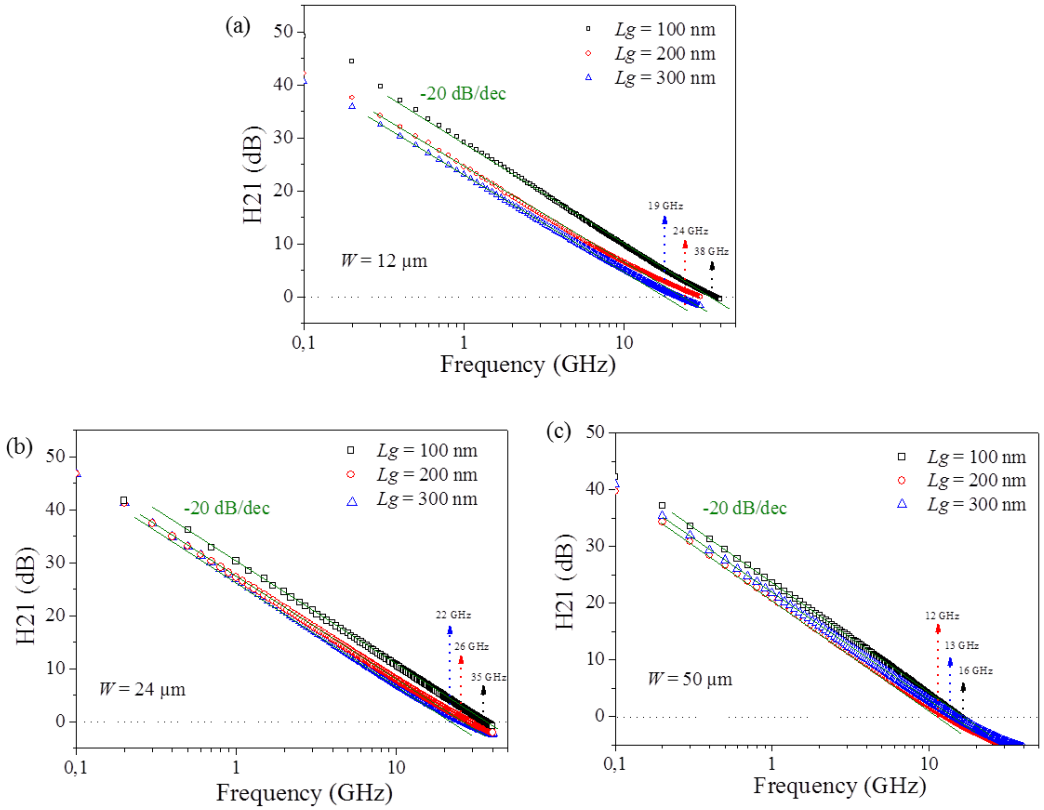


Figure III-17:The best value of as measured (DUT) current gain |H21| for GFETs with different gate length and gate width, in (a) W = 12 µm; in (b) W = 24 µm and in (c) W = 50 µm

III.5.2.2 Unilateral gain U

Figure III-18 shows the best value of unilateral gain for devices with different gate width. Because the value of maximum oscillation frequency is not simply scaling with the gate length, as discussed in chapter 2, we only present the best value of f_{max} obtained in devices with different gate width. The best performance of f_{max} is found to be 13.5, 12 and 5 GHz for devices according to gate width of 12, 24 and 50 µm. These results are competitive with literatures.

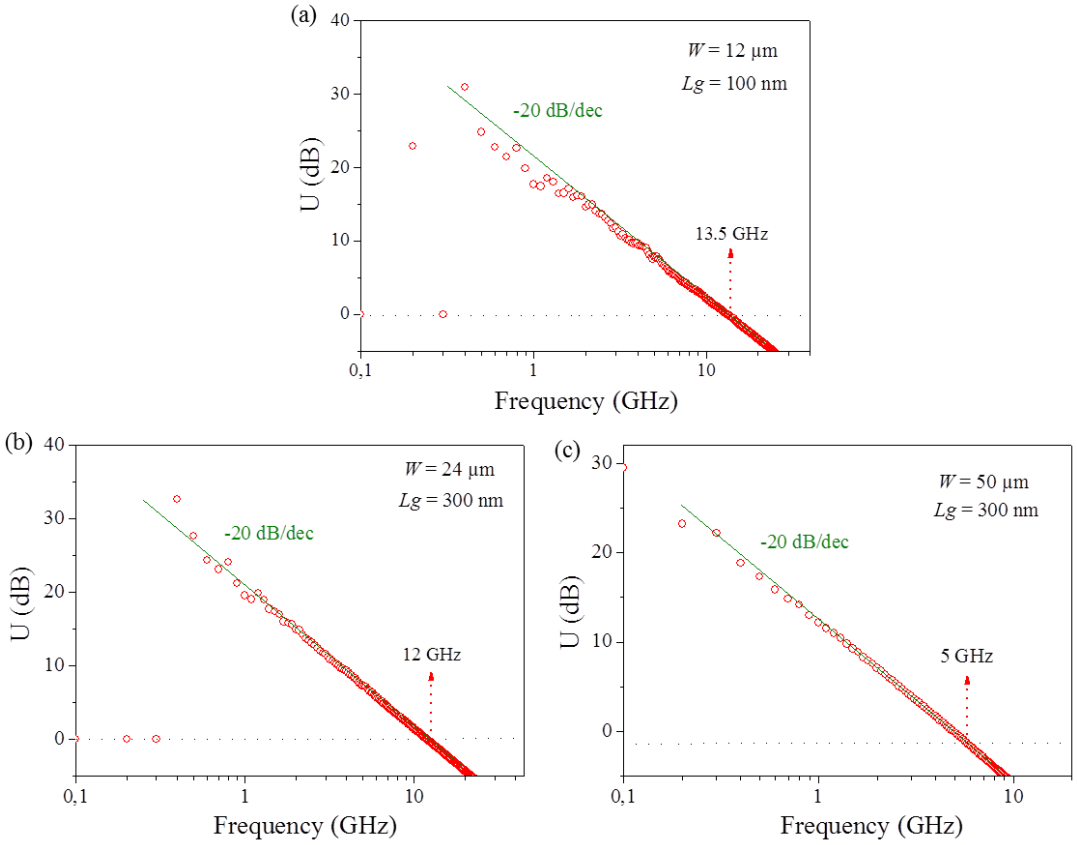


Figure III-18:The best value of unilateral gain (U) of GFETs with different gate width, in (a) W = 12 µm; in (b) W = 24 µm and in (c) W = 50 µm

Figure III-19(a) shows the average value of f_t for devices with different gate length and gate width. For all the three gate width of 12, 24 and 50 µm devices, the performance of f_t are found to be increasing as the gate length decreases from 300 nm to 100 nm. This gate length dependent scaling is also observed for GFETs on rigid substrate, which is due to the variation of gm and gate capacitance (equation of II-1). Figure III-19 (b) shows the evolution of f_{max} depending on devices geometry, which is not scaling with gate length, the same conclusion as mentioned before. It is worthy to note that both 12 and 24 µm gate width devices give the better RF performance compared to that of devices with 50 µm gate width.

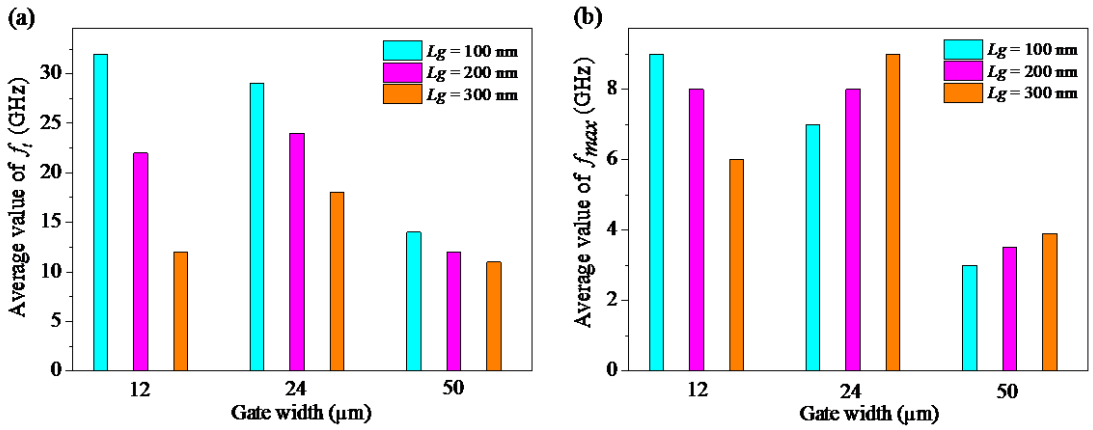


Figure III-19:Average performance dispersion of GFETs with different gate width and length in terms of ft in (a) and fmax in (b)

III.5.3 GFET characterization when substrate is bended

To explore the evolution of device performance in both DC and RF regime with different strain limits, the flexible substrate has been fixed on curve-shaped supporters with different radius (65mm, 25 mm and 1s mm) by using adhesive tape. The strain values are calculated by using equation I-1 in chapter1. Figure III-20 shows the measurement setup adapted for different bending radius supporters.

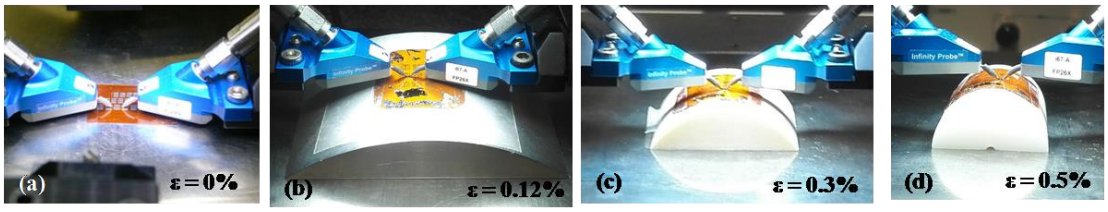


Figure III-20:Test bench for on wafer DC and RF measurement under bending conditions of (a) flat supporter; (b) bended supporter with 65 mm radius, strain limits of 0.12%; bended supporter with 25 mm radius, strain limits of 0.3%; bended supporter with 15 mm radius, strain limits of 0.5%.

For devices with different geometres (combination of 100, 200 and 300 nm gate length with 12, 24 and 50 µm gate width), we selected one or two transistors which typically possess the average or the best performance in its geometry for the DC and RF measurement with strain of 0.13, 0.3 and 0.5 respectively. We firstly choose the device with best performance of f_{max} with strain of 0.5% to present. The DC and RF characterization of this device will be provided. After, in a more general case, the device parameters, such as drain source resistance, transconductance, cut-off frequency and maximum oscillations frequency in variation with strain change for each gate width device will be discussed.

In this work, with strain of 0.5%, we have firstly examined if the nature oxide

layer of Al_2O_3 can stand with the substrate bending by checking the gate leakage current. Figure III-21 (a) shows the leakage current through the dielectric when the substrate is flat and bended with strain limit of 0.5%, both at drain source voltage of 500mV. We have observed very low current value in order of nA regardless the substrate is flat or bended with strain of 0.5%. It indicates no occurrence of dielectric breakdown when the substrate is bended with strain of 0.5%. Figure III-21 (c) and (d) show the output characteristics with two different strain values. When the substrate is flat (ε=0%), the drain-source current (Ids) as function of drain (Vds) has been measured by varying gate voltage from -1 V to 0.6 V by step of 0.2 V. The drain current reaches a maximum value of 6.3 mA at drain voltage Vds=0.5 V and Vgs= -1V. When the substrate is bended on supporter with 15 mm radius (ε=0.5%), the gate voltage is varied from -0.5 V to 0.9 V by step of 0.2V. The gate voltage variation is due to the shift of Dirac point. At drain voltage of 0.5 V and Vgs= -0.5V, the maximum drain current is 6 mA.

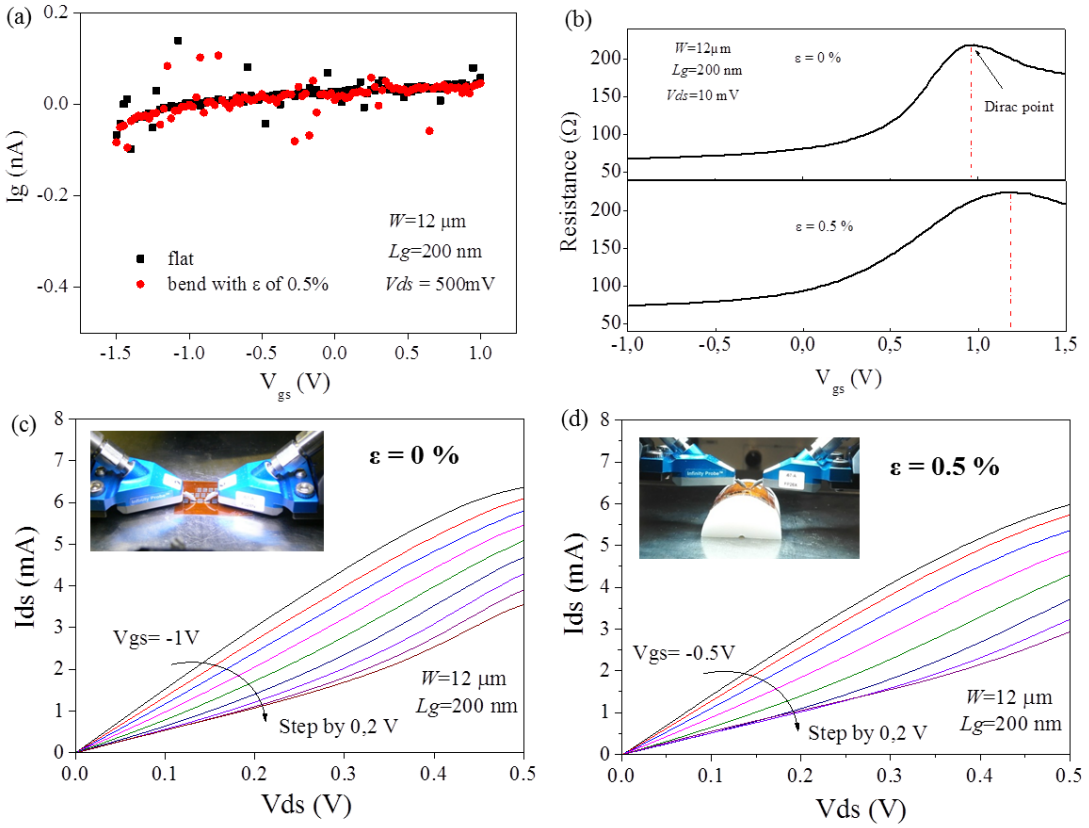


Figure III-21:Device with 12 µm gate width and 200 nm gate length, (a) leakage current through the gate dielectric; (b) comparison of drain to source resistance versus gate voltage for flat and bending conditions; (c and d) output characteristic of the device with increasing strain, for values of 0% and 0.5%.

Figure III-22 shows the RF characteristic of the same device (200 nm gate length and 12 µm gate width) discussed in DC measurement in previous paragraph. Both the

performance (DUT) of current gain (H21) and unilateral gain (U) have been extracted from as-measured S-parameters. A range value of gate voltage, Vgs, has been explored to find the maximum value of transconductance, thus to yield the best RF performance. Vgs of 0V and 0.5V have been chosen respectively for flat (ε=0%) and bended (ε=0.5%) measurement to extract the best performance. The change of the Vgs with strain may be due to the shift of Dirac point discussed in previous paragraph. With strain of 0.5%, we have obtained maximum oscillation frequency f_{max} of 11 GHz and cutoff frequency f_t of 15 GHz, as compared to fmax of 12 GHz and f_t of 18 GHz with strain of 0%.

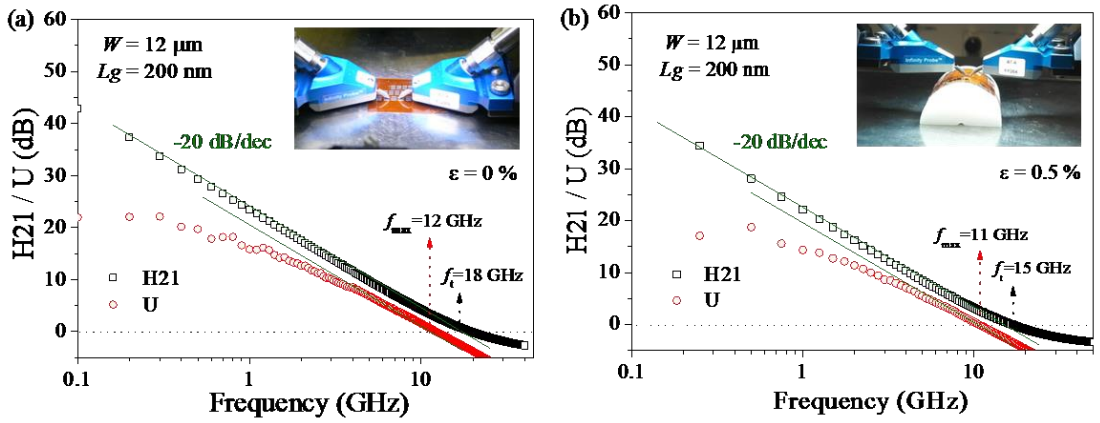


Figure III-22:Radio-frequency characteristics with Vds of 500mV, current gain (h21) and unilateral gain (U) plotted as a function of frequency with strain of 0% in (a) and with strain of 0.5% in (b)

In general, the evolution of some relevant device parameters with strain for different gate width (12, 24 and 50 µm) has been summarized in Figure III-23. In Figure III-23(a) – (c), the drain to source resistance (value extracted from Dirac point at Vds of 10 mV) for all the three gate width devices shows low variance (less than ±10%). It demonstrates the intact of graphene channel and drain/source metal to graphene contact with the strain changes from 0% to 0.5%. Figure III-23 (d) – (f) plots the maximum transconductance as a function of strain. We observe that gm decrease less than 10% for device with 12 and 50 µm gate width. The drop of gm may result from the shift of Dirac point or the variation of carrier mobility. Figure III-23(g)-(i) and Figure III-23 (j)-(l) show the evolution of f_t and f_{max} as function of strain. For all the RF measurement with different strain, specific Vgs is selected to obtain the best performance. In general, for both f_t and f_{max}, low variance (less than ±15%) are observed. Comparing the evolution of these four parameters (Rds, gm, f_t and f_{max}) for each gate width device, approximately the similar tendency could be found. Note that all the values of transconductance, f_t and f_{max} discussed above are deduced with Vds of 500mV.

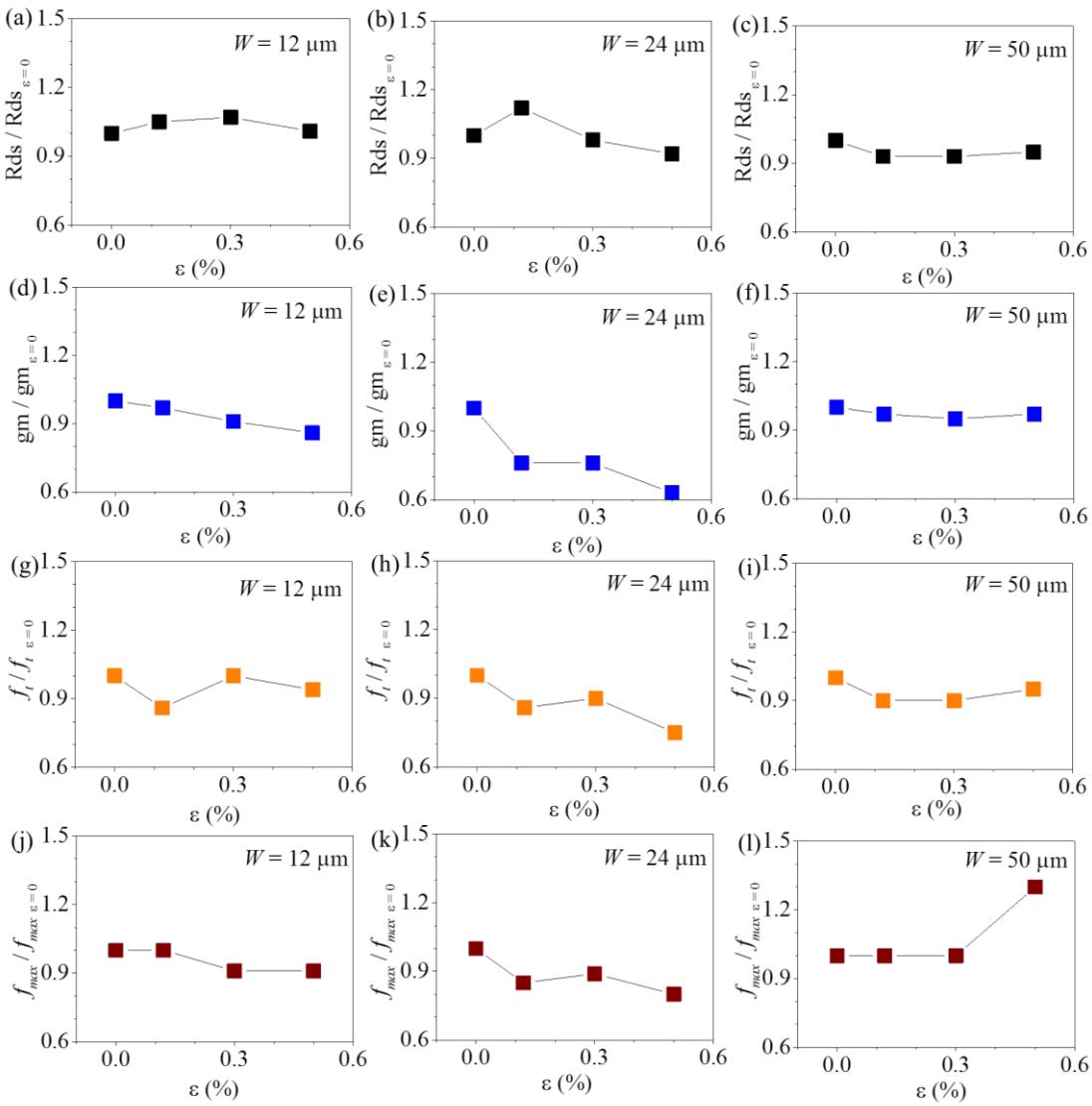


Figure III-23:The evolution of device characteristics, all normalized by the unstrained values (ε=0%), for different gate width (12, 24 and 50 µm) device: (a)-(c), maximum drain to source resistance, Rds, extracted at Dirac point with Vds of 10 mV; (d)-(f), maximum transconductance, gm; (g)-(i), current gain cutoff frequency f_t; and (j)-(l), unilateral gain, maximum oscillation frequency f_{max}.

III.5.4 Thermal effect from substrate

The thermal constraint of polymer substrate is an important issue to be considered for flexible GFETs [22]. This issue is due to the relatively poor thermal conductivity of polymer material. Here, the thermal conductivity of Kapton is 0.12 W/(mK), compared with 140 W/(mK) of silicon. With low thermal conductivity, the substrate material does not allow the heat from device (channel, contact, etc) to dissipate promptly. As a result, the accumulation of heat in substrate will continuously increase the temperature (self-heating) which may degrade the device performance. For most metal materials,

the higher temperature results in the higher resistivity [23]. In the worst case, either the substrate or the device might be damaged (melted or even burned) due to the high temperature. Normally, the heat caused by device is proportional to the value of current passing through. Therefore, in this section, higher value of Vds is further explored to find out the operation limit of our GFETs. In the same time, according to the different Vds, the temperature of active region is recorded by using an infrared camera .

Because increasing Vds is risk to damage the device, we did not choose the device which has the best performance. The resolution of the infrared camera is relatively low (1 μm^2), so 24 and 50 µm gate width transistors are more suitable than 12 µm gate width transistor for infrared measurement because of larger active region. Additionally, 50 µm gate width transistor exhibits poorer performance than that of 24 µm gate width transistor. Therefore, a GFET with 24 µm gate width and 300 nm gate length was used to test higher Vds. Figure III-24(a-e) show under two values of Vgs (Vgs = 0 V and Vgs = -0.6V), the drain-source current Ids as a function of drain-source voltage Vds. We observe that with the increase of Vds (from 0.5 V to 0.7 V), the current starts to saturate, which is due to the low contact resistance. In addition to that, the gate modulation is also enhanced, which is confirmed by gm measurement (as shown in Figure III-25(i)). When Vds increases to 0.8V, the saturation continues but the gate modulation becomes weaker. With Vds of 0.9V, the gate modulation over the current decrease. The drop of gm for Vds of 0.8 and 0.9V is also shown in Figure III-25 (i). Figure III-24(f) shows the RF performance, f_t and f_{max}, as function of Vds. The maximum value of 20 GHz f_t and 9 GHz f_{max} have been obtained at Vds of 0.7V, which is seen significantly increased from 7.3GHz f_t and 2.6 GHz f_{max} with Vds of 0.3V. However, with Vds of 0.8 and 0.9 V, both f_t and f_{max} begin to decrease dramatically. The same tendency is observed also in Figure III-25 (i), which has the plot of gm as function of Vds.

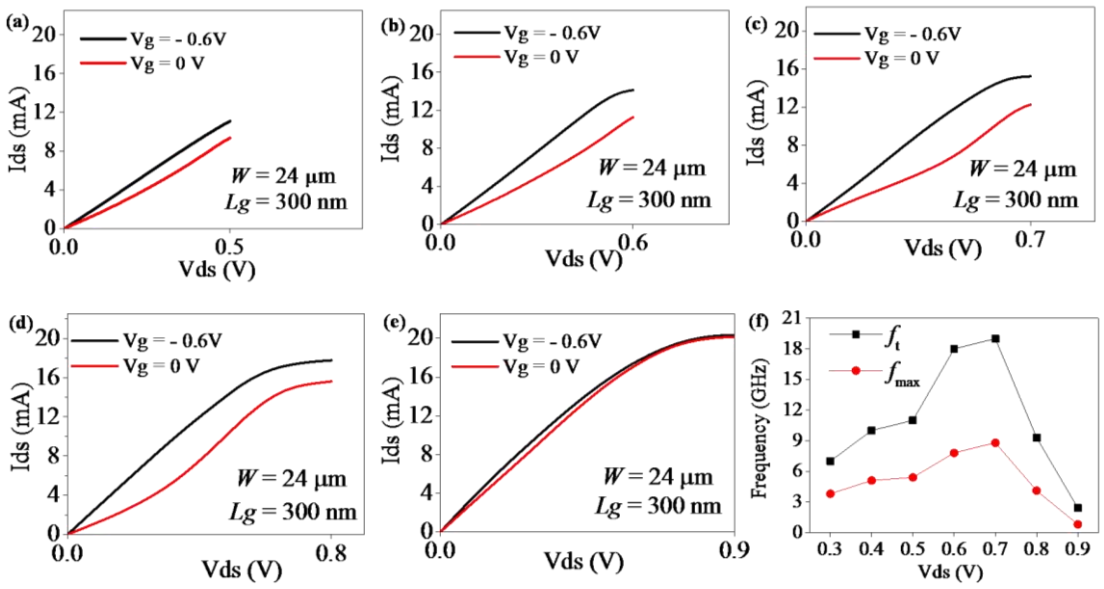


Figure III-24:With two values of gate voltage (Vg = -0.6 and Vg = 0V), drain to source current Ids as function of drain voltage Vds which stops at (a) 0.5 V; (b) 0.6 V; (c) 0.7 V; (d) 0.8 V; and (e) 0.9 V. In (f) plots the ft and fmax as function of Vds.

Figure III-25 shows the temperature infrared images recorded from infrared camera according to different drain to source voltage, with gate voltage at zero. From the infrared measurement, we are able to read the temperature of active region (channel area). Note that limited by the infrared camera resolution, the temperature information is mainly contributed by substrate. It means the real temperature of graphene channel is not measureable here by this tool. Nevertheless, it implies the occurrence of higher temperature on graphene channel. As shown in Figure III-25, the temperature of substrate in device active region is increasing rapidly with Vds increased, from 64 ℃ with 0.3 V to 255 ℃ with 0.9 V. The drain to source resistance, Rds, is found increasing with the increase of Vds. The raise of resistance might be caused by contact resistance or graphene itself. It is worthy to note that on rigid substrate(Si/SiO_2) , the temperature in active region is only 62 ℃ when Vds is applied as 0.9 V.

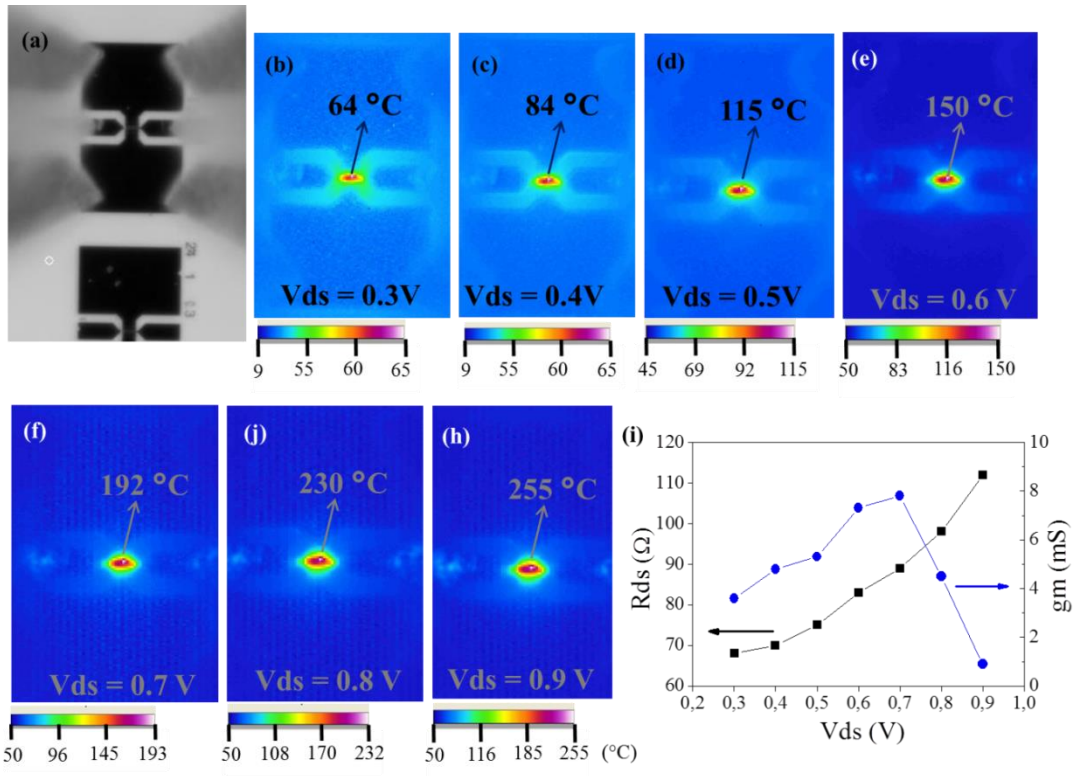


Figure III-25:Infrared image of device with Vds of (a) 0V (before any measurement); (b) 0.3V; (c) 0.4V; (d) 0.5V; (e) 0.6 V; (f) 0.7 V; (j) 0.8 V and (h) 0.9 V. (i) plots the gm and resistance of Rds as function of drain voltage

Conclusion of Chapter III

With the fabrication experience accumulated from devices on rigid substrate, we have successfully fabricated GFETs on flexible substrate, kapton. In chapter 3, we present the results from the flexible GFETs. Contact metal of pure Au is used and low contact resistance in range of 192~500 ohm ·μm are deduced. P-type graphene with mobility up to 2500 cm2/Vs is measured. The transistors with different geometry (gate length of 100, 200 and 300 nm combining with gate width of 12, 24 and 50 μm) have been characterized by both static and dynamic measurements. We report as measured current gain cut-off frequency (f_t-DUT ,without any de-embedding) of 39 GHz and maximum oscillation frequency (f_{max}) of 13.5 GHz in devices with 100 nm gate length and 12 μm gate width. To our knowledge, these results reach to the state of art for flexible GFETs. Besides, both values of f_t-DUT and f_{max} for different gate length and gate width are also discussed. Moreover, RF measurement based on different substrate bending radius (substrate strain varying from 0% to 0.5%) shows less than 15% variation of RF performance. Importantly, the thermal dispersion of substrate in channel region for different drain source bias has been explored, we record 255 ℃ in channel region with Vds of 0.9V, compared to rigid substrate (Si/SiO_2) of only 64 ℃ under the same bias. RF performance decreasing has been observed when Vds ≥ 0.7 V is applied.

Figure III-26 shows the comparison between flexible GFETs RF performance in literatures and that in this work. Our result is at state of the art.

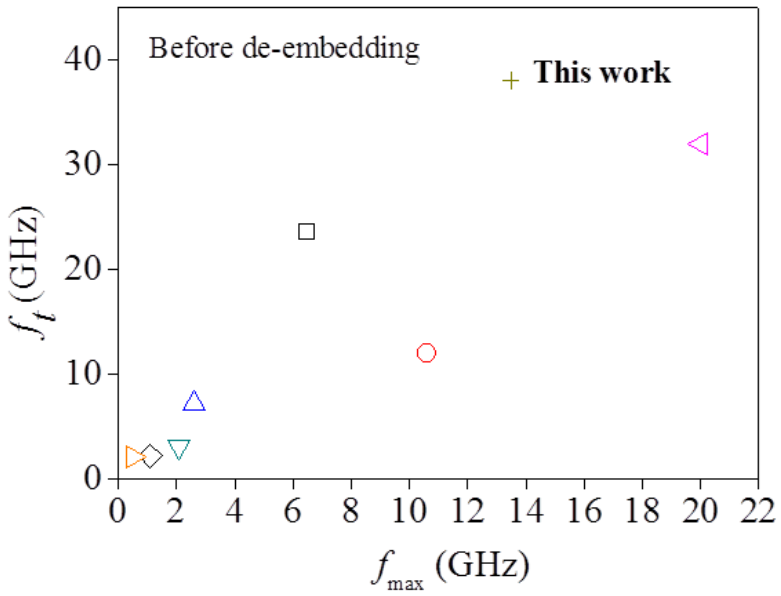


Figure III-26:(a) Comparison of ft and fmax as measured performance (without de-embedding) of this work with literatures from [16][17][18] and [24][25][26][27]

Reference of Chapter III

[1] I. Meric, C. R. Dean, N. Petrone, L. Wang, J. Hone, P. Kim, and K. L. Shepard, "Graphene field-effect transistors based on boron-nitride dielectrics," *Proc. IEEE*, vol. 101, no. 7, pp. 1609–1619, Jul. 2013.

[2] A. K. Geim, "Graphene: Status and prospects," *Science*, vol. 324, no. 5934, pp. 1530 1534, 2009.

[3] J. Lee, H.-Y. Chang, T.-J. Ha, H. Li, R. S. Ruoff, A. Dodabalapur, and D. Akinwande, "High-Performance Flexible Nanoelectronics : 2D Atomic Channel Materials for Low-Power Digital and High-Frequency Analog Devices," Electron Devices Meeting (IEDM), pp.19.2.1-19.2.4, 2013.

[4] S.-K. Lee, B. J. Kim, H. Jang, S. C. Yoon, C. Lee, B. H. Hong, J. A. Rogers, J. H. Cho, and J.-H. Ahn, "Stretchable Graphene Transistors with Printed Dielectrics and Gate Electrodes," *Nano Letters*, vol. 11, no. 11, pp. 4642–4646, Nov. 2011.

[5] S.-K. Lee, H. Y. Jang, S. Jang, E. Choi, B. H. Hong, J. Lee, S. Park, and J.-H. Ahn, "All Graphene-Based Thin Film Transistors on Flexible Plastic Substrates," *Nano Letters*, vol. 12, no. 7, pp. 3472–3476, Jul. 2012.

[6] S. M. Kim, E. B. Song, S. Lee, J. Zhu, D. H. Seo, M. Mecklenburg, S. Seo, and K. L. Wang, "Transparent and Flexible Graphene Charge-Trap Memory," *ACS Nano*, vol. 6, no. 9, pp. 7879–7884, Sep. 2012.

[7] B. J. Kim, S.-K. Lee, M. S. Kang, J.-H. Ahn, and J. H. Cho, "Coplanar-Gate Transparent Graphene Transistors and Inverters on Plastic," *ACS Nano*, vol. 6, no. 10, pp. 8646–8651, Oct. 2012.

[8] Y. Liang, X. Liang, Z. Zhang, W. Li, X. Huo, and L. Peng, "High mobility flexible graphene field-effect transistors and ambipolar radio-frequency circuits," *Nanoscale*, vol. 7, no. 25, pp. 10954–10962, 2015.

[9] J. Meng, J.-J. Chen, L. Zhang, Y.-Q. Bie, Z.-M. Liao, and D.-P. Yu, "Vertically Architectured Stack of Multiple Graphene Field-Effect Transistors for Flexible Electronics," *Small*, vol. 11, no. 14, pp. 1660–1664, Apr. 2015.

[10] S. Lee, O. D. Iyore, S. Park, Y. G. Lee, S. Jandhyala, C. G. Kang, G. Mordi, Y. Kim, M. Quevedo-Lopez, B. E. Gnade, R. M. Wallace, B. H. Lee, and J. Kim, "Rigid substrate process to achieve high mobility in graphene field-effect transistors on a flexible substrate," *Carbon*, vol. 68, pp. 791–797, Mar. 2014.

[11] M. E. Ramón, K. N. Parrish, J. Lee, C. W. Magnuson, L. Tao, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, "Graphene frequency doubler with record 3GHz bandwidth and the maximum conversion gain prospects," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, 2012, pp. 1–3.

[12] J. Lee, T.-J. Ha, K. N. Parrish, S. F. Chowdhury, L. Tao, A. Dodabalapur, and D. Akinwande, "High-Performance Current Saturating Graphene Field-Effect Transistor With Hexagonal Boron Nitride Dielectric on Flexible Polymeric Substrates," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 172–174, Feb. 2013.

[13] A. C. Ferrari, F. Bonaccorso, V. Fal'ko, K. S. Novoselov, S. Roche, P. Bøggild, S. Borini, F. H. L. Koppens, V. Palermo, N. Pugno, J. A. Garrido, R. Sordan, A. Bianco, L. Ballerini, M. Prato, E. Lidorikis, J. Kivioja, C. Marinelli, T. Ryhänen, A. Morpurgo, J. N. Coleman, V. Nicolosi, L. Colombo, A. Fert, M. Garcia-Hernandez, A. Bachtold, G. F. Schneider, F. Guinea, C. Dekker, M. Barbone, Z. Sun, C. Galiotis, A. N. Grigorenko, G. Konstantatos, A. Kis, M. Katsnelson, L. Vandersypen, A. Loiseau, V. Morandi, D. Neumaier, E. Treossi, V. Pellegrini, M. Polini, A. Tredicucci, G. M. Williams, B. Hee Hong, J.-H. Ahn, J. Min Kim, H. Zirath, B. J. van Wees, H. van der Zant, L. Occhipinti, A. Di Matteo, I. A. Kinloch, T. Seyller, E. Quesnel, X. Feng, K. Teo, N. Rupesinghe, P. Hakonen, S. R. T. Neil, Q. Tannock, T. Löfwander, and J. Kinaret, "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, 2015.

[14] S. Lee, K. Lee, C.-H. Liu, G. S. Kulkarni, and Z. Zhong, "Flexible and transparent all-graphene circuits for quaternary digital modulations," *Nature Communications*, vol. 3, p. 1018, Aug. 2012.

[15] B. J. Kim, H. Jang, S.-K. Lee, B. H. Hong, J.-H. Ahn, and J. H. Cho, "High-Performance Flexible Graphene Field Effect Transistors with Ion Gel Gate Dielectrics," *Nano Letters*, vol. 10, no. 9, pp. 3464–3466, Sep. 2010.

[16] C.-H. Yeh, Y.-W. Lain, Y.-C. Chiu, C.-H. Liao, D. R. Moyano, S. S. H. Hsu, and P.-W. Chiu, "Gigahertz Flexible Graphene Transistors for Microwave Integrated Circuits," *ACS Nano*, vol. 8, no. 8, pp. 7663–7670, Aug. 2014.

[17] N. Petrone, I. Meric, T. Chari, K. L. Shepard, and J. Hone, "Graphene Field-Effect Transistors for Radio-Frequency Flexible Electronics," IEEE J. Electron Devices Soc., vol. 3, no. 1, pp. 44–48, Jan. 2015.

[18] J. Lee, T.-J. Ha, H. Li, K. N. Parrish, M. Holt, A. Dodabalapur, R. S. Ruoff, and D. Akinwande, "25 GHz Embedded-Gate Graphene Transistors with High-K Dielectrics on Extremely Flexible Plastic Sheets," *ACS Nano*, vol. 7, no. 9, pp. 7744–7750, Sep. 2013.

[19] I. Childres, L. A. Jauregui, M. Foxe, J. Tian, R. Jalilian, I. Jovanovic and Y. P. Chen, "Effect of electron-beam irradiation on graphene field effect devices," *Appl. Phys. Lett*, 97, 173109, 2010

[20] F. Schwierz, "Graphene transistors," *Nature nanotechnology*, vol. 5, pp. 487-495, May. 2010

[21] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems," Proc. IEEE, vol. 101, no. 7, pp. 1567–1584, Jul. 2013.

[22] F. Schwierz, J. Pezoldt, and R. Granzner, "Two-dimensional materials and their prospects in transistor electronics," *Nanoscale*, vol. 7, no. 18, pp. 8261–8283, 2015.

[23] H. M. Milchberg, R. R. Freeman, S. C. Davey, and R. M. More, "Resistivity of a Simple Metal from Room Temperature to 10^6 K" *Phys. Rev. Lett*. 61, 2364, Nov. 1988

[24] N. Petrone, I. Meric, J. Hone, and K. L. Shepard, "Graphene Field-Effect Transistors with Gigahertz-Frequency Power Gain on Flexible Substrates," *Nano Lett.*, vol. 13, no. 1, pp. 121–125, Jan. 2013.

[25] J. Lee, K. N. Parrish, S. F. Chowdhury, T.-J. Ha, Y. Hao, L. Tao, A. Dodabalapur, R. S. Ruoff, and D. Akinwande, "State-of-the-art graphene transistors on hexagonal boron nitride, high-k, and polymeric films for GHz flexible analog nanoelectronics," in Electron Devices Meeting (IEDM), 2012 IEEE International, 2012, pp. 14–6.

[26] N. Petrone, T. Chari, I. Meric, L. Wang, K. L. Shepard, and J. Hone, "Flexible Graphene Field-Effect Transistors Encapsulated in Hexagonal Boron Nitride," *ACS Nano*, vol. 9, no. 9, pp. 8953–8959, Sep. 2015.

[27] C. Sire, F. Ardiaca, S. Lepilliet, J.-W. T. Seo, M. C. Hersam, G. Dambrine, H. Happy, and V. Derycke, "Flexible Gigahertz Transistors Derived from Solution-Based Single-Layer Graphene," *Nano Lett.*, vol. 12, no. 3, pp. 1184–1188, Mar. 2012.

General conclusion and Perspective

Conclusion

In this thesis, fabrication processes for flexible devices have been developed.

First, we have optimized the parameters for inkjet printing technology, based on Fujifilm Dimatix printer, commercial ink from Suntronic U5603 and substrates of PEN and Kapton to obtain printed-patterns with well controlled geometry. The resistivity of the ink material, which depends on sintering temperature and time, has been studied by using the Van der Pauw method. An optimum resistivity of 11.6 μΩ·cm has been extracted under the sintering conditions of 200 ℃ with 30 min. Structures of CPW transmission lines have been well realized and different characteristic impedances (Z_C) have been reported after RF characterization. The minimum separation value, S= 20 μm, has been achieved on PEN and Kapton substrates, which yields Z_C of 60 Ω and 57 Ω, respectively. The attenuation as a function of the sintering temperature has also been explored, and loss lower than 0.4 dB/mm up to 40 GHz after 300 ℃ sintering have been achieved on Kapton substrate. Furthermore, the evolution of RF performances with an applied strain has been explored. We find that the RF performance of the CPW lines is minimally affected by bending the substrate with a strain up to 0.5%. In addition, we have successfully printed structures of antenna on PEN, in collaboration with University of Nice (group of Pr. Luxey), and structures for thermal conductivity measurement on polyimide, in collaboration with the MITEC group in IEMN. Both works further demonstrate the promising potential of the optimized inkjet printing technology.

Second, we have developed a fabrication process based on an optimized wet graphene transfer process and bottom gate field effect transistors using natural oxidation of aluminum as dielectrics. GFET devices with different geometry, gate width of 12, 24 and 50 μm combined with gate length of 100, 200 and 300 nm, have been realized on rigid substrate of Si/SiO_2. Graphene hole mobility up to 3400 cm^2/Vs has been measured by using Hall Effect measurements. In DC characterization, output and transfer characteristics have been carried out. In RF characterization, current gain and unilateral gain for all the devices have been fully discussed. Finally, we report an intrinsic current gain cut-off frequency ($f_{t\text{-}int}$) of 15.5 GHz and maximum oscillation frequency (f_{max}) of 11 GHz in devices with 100 nm gate length and 12 μm gate width.

Third, we have successfully fabricated GFETs devices with similar length and width on flexible substrate, Kapton, by using almost the same fabrication process as for rigid substrates.. Some modifications have been added to make the process compatible

with flexible substrates. By using pure Au, low contact resistance down to 192 Ohm.µm have been obtained. Both static and dynamic measurements have been carried out. We report as measured (without de-embedding) current gain cut-off frequency f_t of 39 GHz, and maximum oscillation frequency f_{max} of 13.5 GHz in devices with 100 nm gate length and 12 µm gate width. This performance is obtained using the graphene material grown and transferred by Graphenea (one of our partner in the Flagship graphene project). The associated hole mobility up to 2500 cm^2/Vs were extracted from Hall measurement.

To our knowledge, these results reach the state of the art for flexible GFETs. Moreover, the evolution of RF performance according to different substrate bending radius (substrate strain varying from 0% to 0.5%) is evaluated, and performance variance less than ±20% has been observed.

Perspective

Based on the results of this work where we have shown the efficiency of the fabrication process for GFET on flexible substrates, one of the main perspective will be to achieved RF circuits on flexible substrates. From the process point of view, hybrid circuit will be first explored with several orientations:

(i) Fabrication of circuit using conventional technology: this approach is preferable if high performances are required.

(ii) Combination of inkjet printing technology (for passive devices) associated to conventional process (for active devices) to maintain high performance.

(iii) Finally, we can also imagine a fully printed circuit, where active and passive devices are fabricated using inkjet printing technology. In this case it is necessary to used also graphene in solution (graphene ink). The preliminary work on fully printed GFET is illustrated on the figure below.

The device channel is fabricated using graphene ink, the contacts (source and drain) are printed using silver nanoparticle ink, the gate dielectric is fabricated using deposition of parylene, and finally the gate contact is printed using silver nanoparticle ink.

Based on the resolution of the printing technology, the cut-off frequency of this kind of devices is under the GHz range.

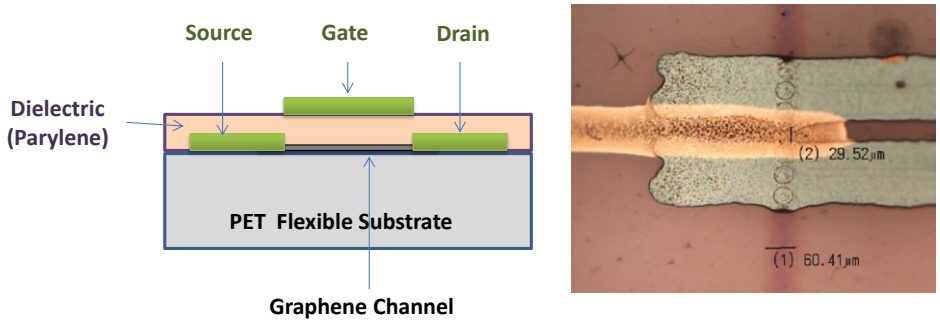


Figure 1: (a) Illustration of the side view of fully printed GFT; (b) Top view of the printed GFET.

Publications list

Journal

[1] **W. Wei**, X. Zhou, G. Deokar, H. Kim, M. Belhaj, E. Galopin, E. Pallecchi, D. Vignaud, H. Happy, Graphene Field-Effect Transistors with Aluminium Bottom-gate Electrodes and its Natural , *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp: 2769-2773 (2015).

[2] A. Bisognin, J.Thielleux, **W. Wei**, D. Titz, F. Ferrero, P. Brachat, G. Jacquemod, H. Happy and C. Luxey, Inkjet Coplanar Square Monopole on Flexible substrate for 60 GHz applications, *IEEE Antennas and Wireless Propagation Letters*, 13: 435-438 (2014)

[3] N. Al-Khudary, P. Y. Cresson, **W. Wei**, H. G. Happy and T. Lasri, Inkjet printing technology for polymer thermal conductivity measurement by the three omega method, *Polymer Testing*, 40: 187-195 (2014)

[4] **W. Wei**, E. Pallecchi, A. Centeno, M. Belhaj, H. Samiul, H. Happy, Flexible Graphene Field-Effect Transistors with high RF performance (under redaction)

Conference

[5] **W. Wei**, T. Dargent, V. Hoel, H. Happy, Fabrication de Composants Passifs par Impression Jet d'encre Caracterisation RF, 12es JOURNEES PEDAGOGIQUES CNFM, poster, 28-30 novembre 2012, Saint malo (Poster)

[6] **W. Wei**, M. M. Belhaj, Technology of Inkjet Printing applied for Flexible Electronics, Journées Nationales du Réseau Doctoral en Microélectronique, Grenoble, France, 5-7 Jun, 2013 (Oral presentation)

[7] **W. Wei**, M. Belhaj, G. Deokar, D. Mele, E. Pallecchi, E. Pichonat, D. Vignaud, H. Happy, Back-gated Microwave Field-Effect Transistors Based on Transferred CVD-Grown Graphene, Graphene 2014, Toulouse, France, 6-9 May, 2014 (Oral presentation)

[8] **W. Wei**, G. Deokar, M. Belhaj, D. Mele, E. Pallecchi, E. Pichonat, D. Vignaud, H. Happy, Fabrication and Characterization of CVD-grown graphene based Field-Effect Transistor, European Microwave Week 2014, Rome, Italy, 5-10 Oct, 2014 (Oral presentation)

[9] **W. Wei**, G. Deokar, M. Belhaj, D. Mele, E. Pallecchi, E. Pichonat, D. Vignaud, H. Happy, Key Parameters of CVD-grown Graphene on Copper foil and its Transfer for radio-frequency Application, Journées Nationales du Réseau Doctoral en

Micro électronique, Lille, France, 23-25 Jun, 2014 (Prize of best oral presentation)

[10] **W. Wei**, G. Deokar, M. Belhaj, D. Mele, E. Pallecchi, E. Pichonat, D. Vignaud, H. Happy, CVD-grown Graphene and its Transfer technique Applied for back-gated Field-Effect Transistor, 13es JOURNEES PEDAGOGIQUES CNFM, Saint-Malo, France, 19-21 Nov, 2014 (Invited oral presentation)

[11] **W. Wei**, M. Belhaj, G. Deokar, D. Mele,X. Zhou, E. Pallecchi, E. Pichonat, D. Vignaud, H. Happy, Radio-Frequency Application of Bottom-gated Graphene Field-Effect Transistors Compatible with Flexible Substrate, EEA Electonique 2014, Villeneuve d'ascq, France, 20-21 Oct, 2014 (Poster)

[12] M. M. Belhaj, **W. Wei**, E. Pallecchi, C. Mismer, I. Roch-Jeune, H. Happy, Inkjet Printed Flexible Transmission Line for high Frequency Applications up to 67 GHz, European Microwave Week 2014, Rome, Italy, 5-10 Oct, 2014 (Poster)

[13] A. Bisognin, J. Thielleux, **W. Wei**, H. Happy, D. Titz, F. Ferrero, C. Luxey, G. Jacquemod, P. Brachat, Conception et mesure d'une antenne à 60 GHz imprimée par jet d'encre sur un substrat souple PEN, 18èmes Journées Nationales Microondes, 15-17 Mai 2013, Paris

[14] A. Bisognin, C. Luxey, G. Jacquemod, F. Ferrero, D. Titz, J. Thielleux, **W. Wei**, H. Happy, P. Brachat, Antenna on PEN substrate for Millimeter-wave applications, Antenna and Propagation Symposium (AP-S/URSI), Orlando, USA, 7-13 July 2013

[15] V. Semkin, M. Kyro, A. V. Raisanen, A. Bisognin, F. Ferrero, C. Luxey, H. Happy, J. Thielleux, **W. Wei**, Characterization of Inkjet Patch Antenna on Different Ground Planes at Millimeter-Wave Frequencies, Loughborough Antennas & Propagation Conference, Loughborough, UK, 11-12 Nov,2013

Appendix I

Considerations of inkjet printing parameters

For the study of drop spacing, we have to determine the dimension of certain ink droplet on certain substrate. With the knowledge of droplet diameter and drop spacing, the pattern design will respect the following equation (1).

$$\text{Length or width} = D+(n-1)\cdot\Phi \qquad (1)$$

where D is diameter of droplet; n is the number of droplet for length direction or width direction; Φ is the drop space. With respect to the ratio of drop spacing over droplet diameter as constant value 0.67, different firing voltage (16V, 20V, 30V and 40V) and together with different width design (*N*=1,3 and 5) have been tested on PEN substrate @ 20℃. Here, we define *N* as the number of droplets printed in y-direction, which is vertical to printing direction, as illustrated in Figure 1. For different firing voltages and width design, the theoretical width value, W_t, practical width value, W_p, together with its according image, and the final smooth control assessment are presented totally in Table . We find that with the same ratio of D/Φ, the printing quality are found to be different when different number of lines were printed. In the case of one line, N=1, for different firing voltages all the lines are continuous and have smooth boundary control. As the firing voltage increased, the width dimension difference between designed and measured is getting smaller. In the case of three lines, N=3, good quality line was obtained only when firing voltage is 20 V. A hole was observed in the line obtained by 16V firing voltage and boundary with fluctuation were found in the lines obtained by 30V and 40V firing voltage. In the case of five lines, N=5, very good printing quality were obtained. For all the firing voltage, the lines were found to be continuous, and have good smooth control. What's more, the dimension differences between designed and measured are almost negligible.

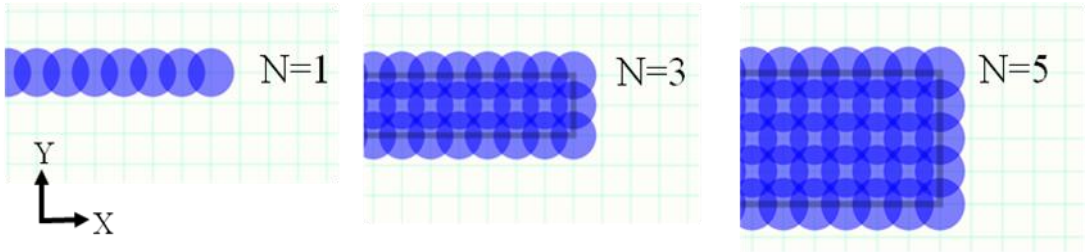
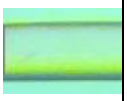
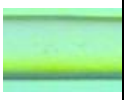
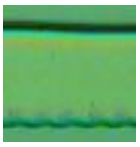
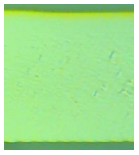
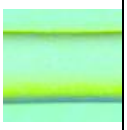
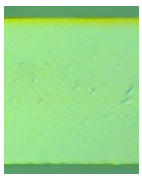


Figure 1: Schematic of patterns designed in Dimatix which have one (N=1), three (N=3) and five (N=5) lines to be printed in printing direction of X

The conclusion from Table 1 is: when we find the best ratio of drop spacing over droplet diameter, firing voltage is another important parameter to be considered. In

practice, for arbitrary substrates, we need to find the most suitable firing voltage for each case, particularly for different needs of dimensions.

Table 1: Summary of pattern lines with constant ratio of droplet diameter to drop spaceing but different firing voltage togther with considering dimension both designed and measured and also smooth control

V (v)	D (μm)	Φ (μm)	N=1		N=3		N=5		Smooth Control	
			W_t W_p	Image	W_t W_p	Image	W_t W_p	Image		
16	40	23	40 33		86 76		132 128		N=1 N=3 N=5	☺ ☹ ☺ ☺
20	44	25	44 37		94 88		144 142		N=1 N=3 N=5	☺ ☺ ☺ ☺ ☺
30	46	26	46 42		98 95±4		150 150		N=1 N=3 N=5	☺ ☺ ☹ ☺ ☺
40	48	27	48 47		102 98±9		156 158		N=1 N=3 N=5	☺ ☺ ☹ ☹ ☺ ☺

V: firing voltage; D: droplet diameter; Φ: drop space; W_t ,W_p : theoretical and practical width value of printed line.

Appendix II

Parameters extraction of CPW transmission lines

The CPW transmission line can be regarded as an infinite series of two-port elementary components. As Figure 2 (a) shows, we define these elementary components with a unit length, ΔL, representing an infinitesimally short segment of the whole transmission line. Based on this elementary components, Figure 2 (a) illustrates the parameters of primary line constants (per unit length) such as the resistance, R, and the inductance, L, of conductors; the sum of capacitance, C, and conductance, G, between each of two conductors. Figure 2 (b) shows the according equivalent diagram to the two-port elementary components. Derived from the primary line constants, there are several parameters could be considered for the characterization of CPW transmission lines, such as character impedance Zc, and secondary line constant: propagation constant γ, attenuation constant α and phase constant β.

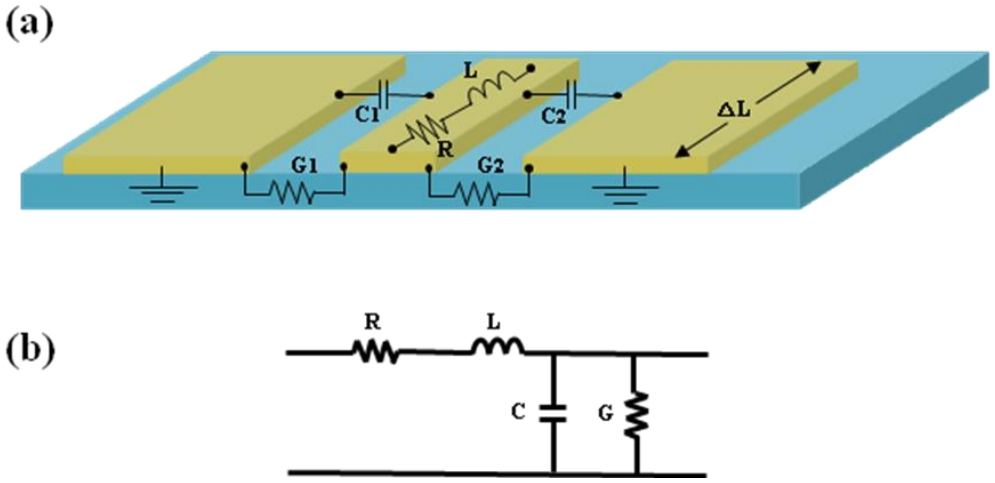


Figure 2: (a) Representation of parasitic elements (primary line constants) in a unit length of CPW transmission line (b) equivalent circuit model of (a)

Practically, all those parameters concerning the characterization of CPW transmission line could be obtained via the measurement of Scattering parameters (S-parameters). The section below introduces some basic background knowledge of S-parameters.

(1) S-parameters.

Differing to DC signals, in microwave frequency range, it is difficult to describe the electrical signals behaviour by considering the changes of voltage and current. In such case, therefore, any devices (CPW transmission line or transistors) in high frequency circuit can be treated as a two-port network [1] and the signal power

change is considered here which is more easily quantified than currents and voltages. The power change of RF signal can be equated with the propagation of a wave, which can be decomposed into an incident wave and a transmitted wave. In Figure 3, S_{11} and S_{22} represent coefficient of reflection ($S_{11} = b_1 / a_1$ when $a_2=0$ and $S_{22} = b_2 / a_2$ when $a_1=0$); S_{21} and S_{12} represent coefficient of transmission ($S_{21} = b_2 / a_1$ when $a_2=0$ and $S_{12} = b_1 / a_2$ when $a_1=0$). If the two-port network is symmetrical either considering from port 1 or port 2, we should have $S_{11}= S_{22}$ and $S_{21}=S_{12}$. The advantage of using two-port network is that one can obtain the property of the network only by the performance of two ports, without the analysis of what components are exactly included, which might be complicated. Equation (2) gives the relationship between the reflected, incident power waves and the S-parameter in matrix.

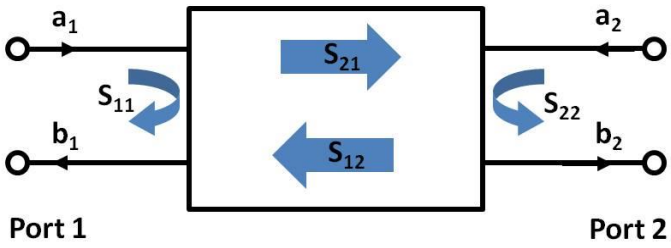


Figure 3: Schematic of a two-port network

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2)$$

(2)Relations of the CPW parameters considered in this study

For the CPW transmission line fabricated by inkjet printing in this study, what we want to know is the characteristic impedance, Zc, and attenuation constant, α, which can be both extracted from S-parameters measurement based on equations of eq(3) and eq(5), as shown in Figure 4. The performance of Zc and α are linked to the primary line constants of R,L,C and G (illustrated in first paragraph of this Appendix) as described in equations of eq(4) and eq(6). By equations in eq(7), the primary line constant could be derived by geometric parameters of CPW lines, W,S and t (illustrated in Figure I-23), resistivity ρ of CPW lines and relative permittivity ε of substrate. In this work, the geometric parameters of CPW lines would be determined by inkjet printing technology, and the lines resistivity will depend on sintering parameters. Relative equations are listed in Table 2.

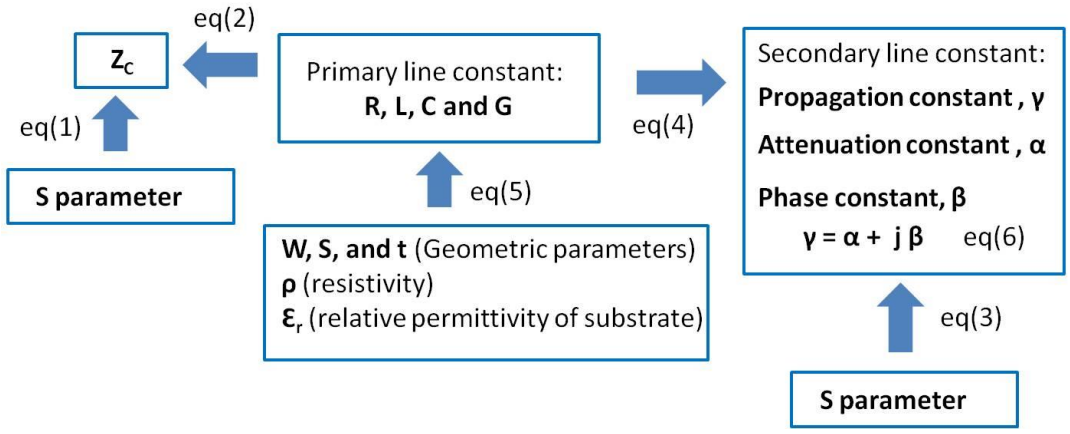


Figure 4: A schematic to show the relationship between some of the CPW parameters considered in this study

Table 2: Equations for Figure 4

$Z_C = \pm Z_0 \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}$	Eq(3)
$Z_C = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$	Eq(4)
$e^{-\gamma l} = \frac{2S_{21}}{1 - S_{11}^2 + S_{21}^2 \pm \sqrt{\left(1 + S_{11}^2 - S_{21}^2\right)^2 - 4S_{11}^2}}$	Eq(5)
$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$	Eq(6)
$C = (\varepsilon_\gamma + 1)\varepsilon_0 2\frac{K(k)}{K'(k)}, \quad L = \frac{1}{c^2 C_a}, \quad R = \frac{1}{\sigma W t}$	Eq(7)

Z_C: characteristic impedance; Z_0: load impedance, S_{11} and S_{21}: S-parameters; ω: frequency; *R,L,C* and *G:* definitions are given in first paragraph of this Appendix; l: the length of transmission line; γ: propagation constant; ε_0: vacuum permittivity; ε_r: relative permittivity; $\frac{K(k)}{K'(k)}$: geometry coefficient; c: speed of light; C_a: capacitance with the substrate replaced by air; σ:conductivity of CPW lines; *W* and *t*: illustrated in Figure I-23.

[1] C. T. Tai, Complementary Reciprocity Theorems for Two-Port Networks and Transmission Lines, IEEE transactions on Education,37: 42-45 (1992)

Appendix III

Samples information

Table 3: Information of GFET samples presented in thesis

samples			Si07	Si08	Si09	Si10	Kap10
substrate			Si/SiO_2, rigid	Si/SiO_2, rigid	Si/SiO_2, rigid	Si/SiO_2, rigid	Kapton, flex
Graphene source			Cambridge	IEMN	Korea	IEMN	Graphena
Transfer work finished at:			Cambridge	IEMN	IEMN	IEMN	Graphena
TLM Structure			Pattern B & C	Pattern A	Pattern A	Pattern B & C	Pattern A
Measured devices	W=12 um	Lg=100 nm	5	14	10	3	15
		Lg=200 nm	6	18	15	2	9
		Lg=300 nm	6	22	19	2	12
	W=24 um	Lg=100 nm	0	0	0	9	8
		Lg=200 nm	0	0	0	9	7
		Lg=300 nm	0	0	0	8	10
	W=50 um	Lg=100 nm	0	0	0	10	5
		Lg=200 nm	0	0	0	6	5
		Lg=300 nm	0	0	0	6	7

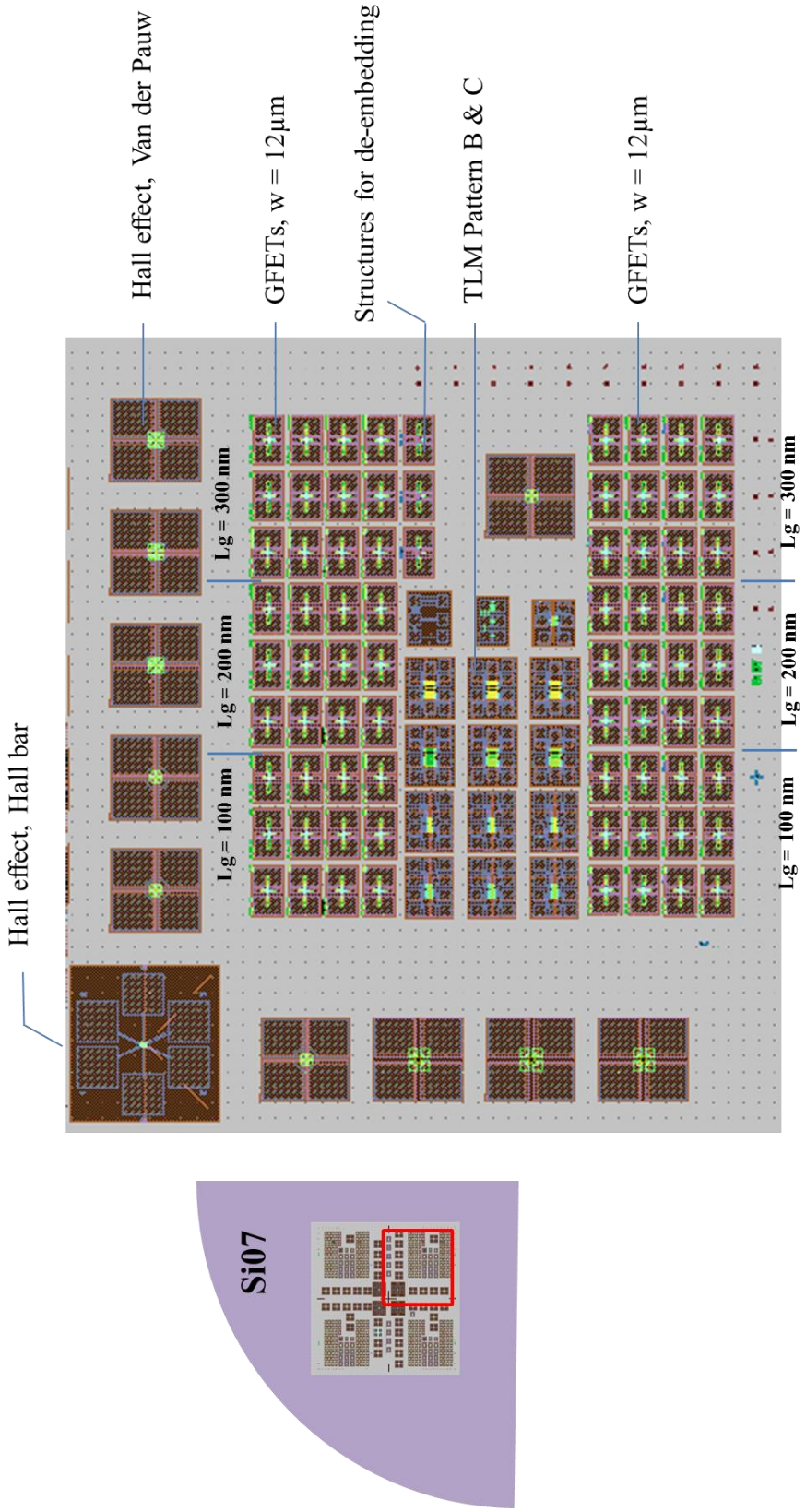


Figure 5: Device map on sample Si07 (on rigid substrate)

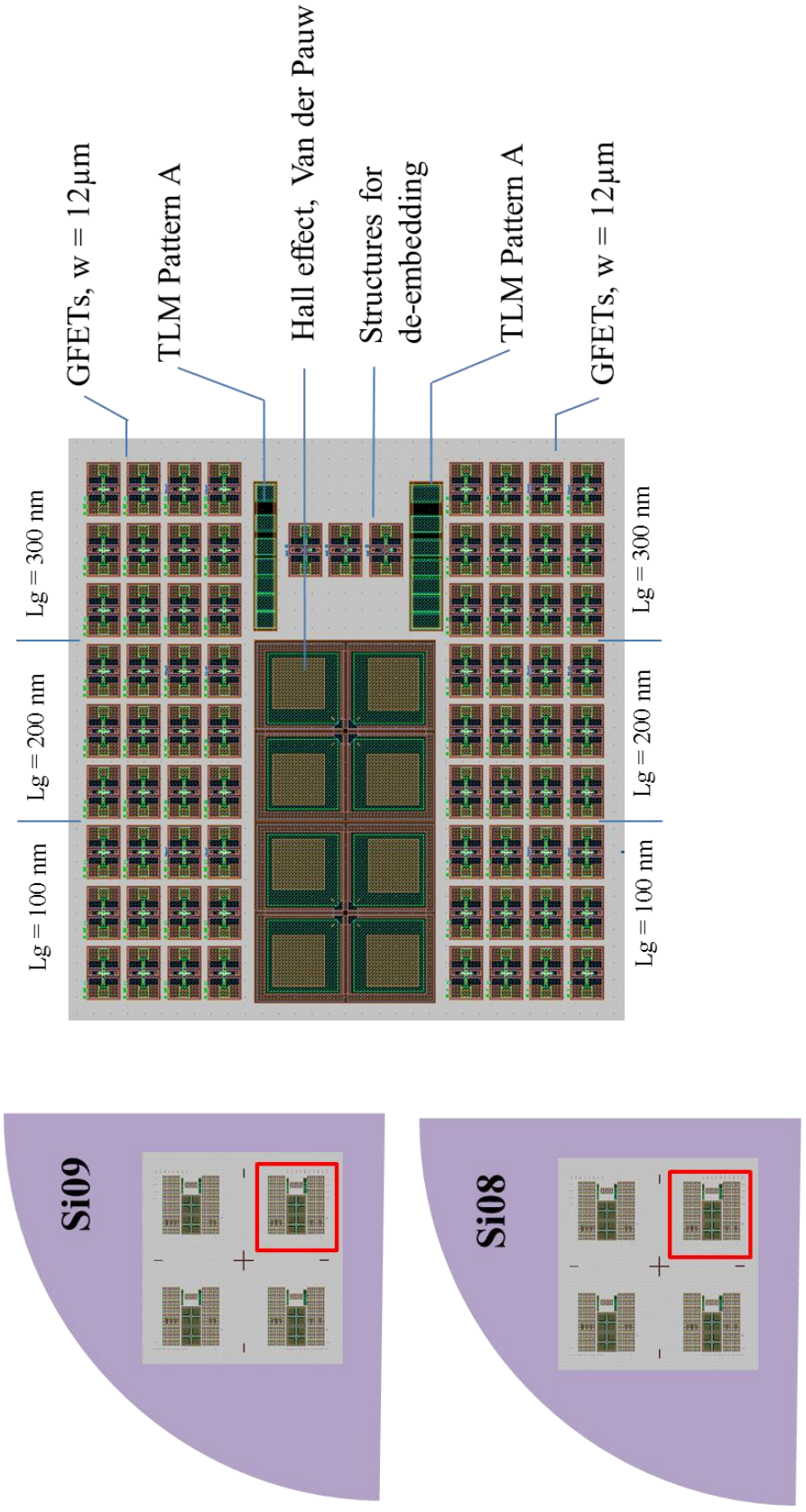


Figure 6: Device map on sample Si08 and Si09 (on rigid substrate)

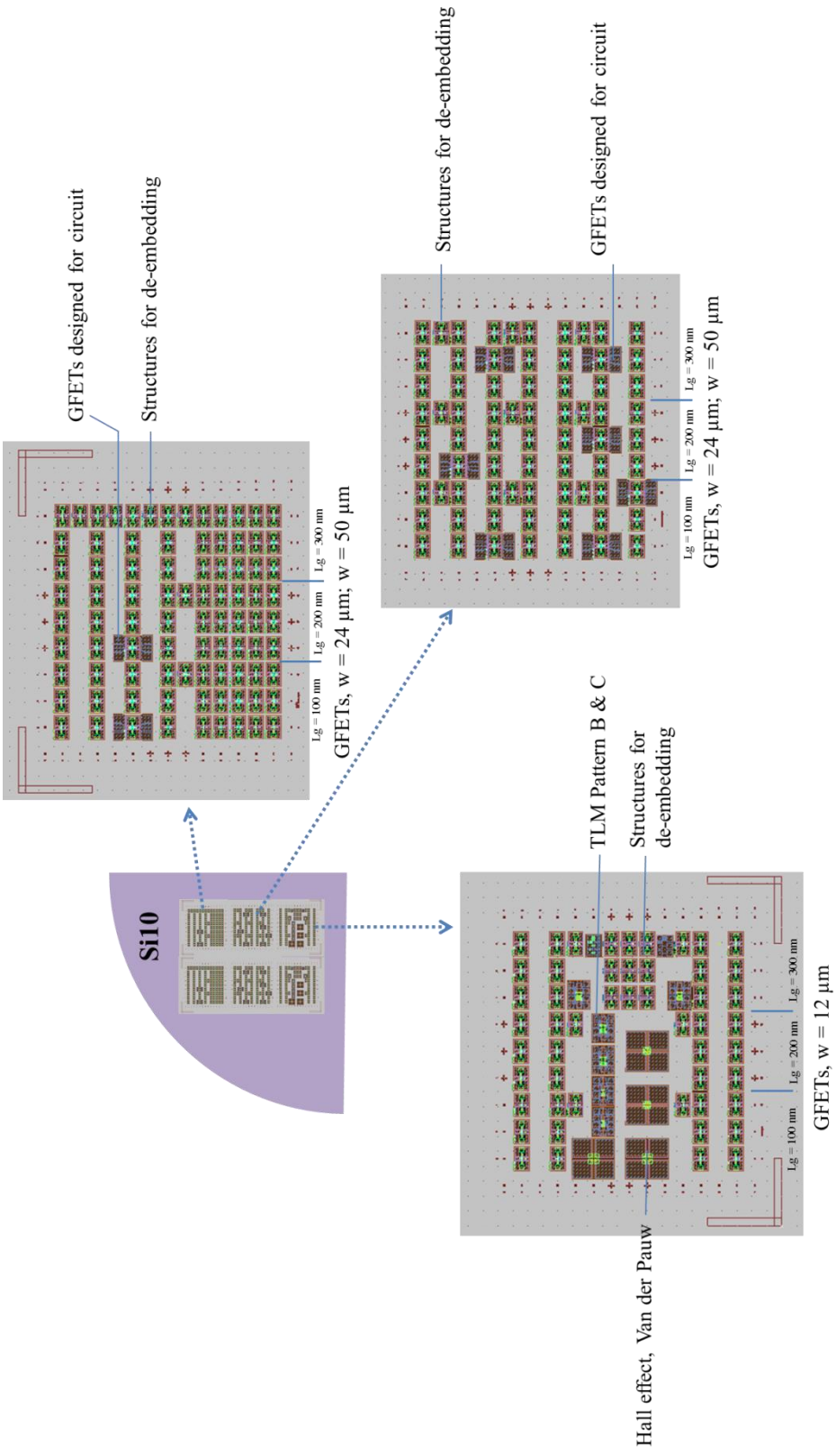


Figure 7: Device map on sample Si10 (on rigid substrate)

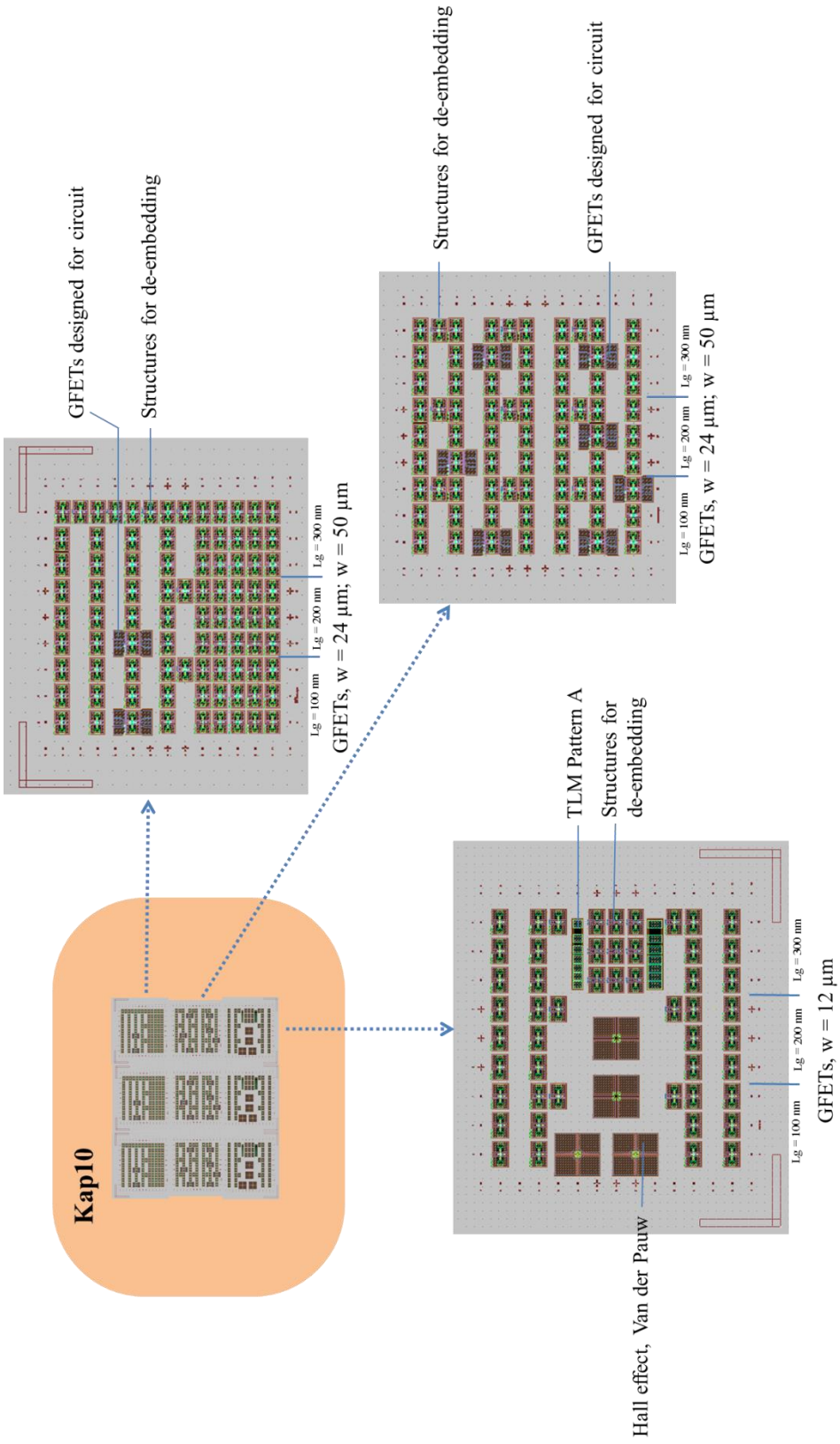


Figure 8: Device map on sample Kap10 (on flexible substrate)

Appendix IV

Calculation of Rc based on Transmission Line Method

We calculated the contact resistance from Transmission Line Method (TLM). On the same chip with other transistors, TLM pattern is fabricated by graphene transfer process, O_2 plasma isolating etching and the metal evaporation followed by a lift-off process. As depicted in Figure 9 (a), an isolated patterned graphene with rectangle shape is connected by several metal pads with different separation (d1,d2,d3…). The total resistance (R_T) measured between two metal contacts consists of several components as shown in Figure 9 (b) and formula 8.

$$R_I = 2R_C + R_{ch} + 2R_m \quad (8)$$

where R_m is the resistance due to contact metal and measuring platform, ig, DC tips. R_C is metal/graphene contact resistance, and R_{ch} is the channel resistance coming from graphene, which can also be written as $Rch = Rs\frac{L}{W}$ (R_S: sheet resistance of graphene channel; W and L: width and length of graphene channel). In approximation (for pattern A in this study), since the resistance of R_m is much smaller than R_C, $R_m << R_C$, the R_m was neglected. Therefore, the formula 9 will become:

$$RT = \frac{Rs}{W}d + 2Rc \quad (9)$$

By measuring the total resistance R_T between two adjacent contacts pads with different separation, and plotting the measurement results, the parameters of contact resistance R_C, sheet resistance R_S and transfer length L_T could be deduced by a linear fitting. Figure 9 (c) gives an example to extract R_C, R_S and L_T based on sample Si10 with pattern B TLM structure (see more details about pattern B in below section). The measured resistance corresponding to different separation (d_1,d_2…d_7) between two adjacent contacts are plotted and then linear fitted. The standard error of value 3 indicates an rather accurate linear fitting and thus a highly reliable measurement. From the fitting line, R_C, R_S and L_T can be extracted as: $2R_C$= intercept to resistance axis; L_T= intercept to distance axis; R_S= slope times width of graphene channel. Additionally, the variations of measured resistance which are well proportional to contacts separation distance (a linear fitting with small value of standard error) indicate the homogeneity of graphene between two contacts.

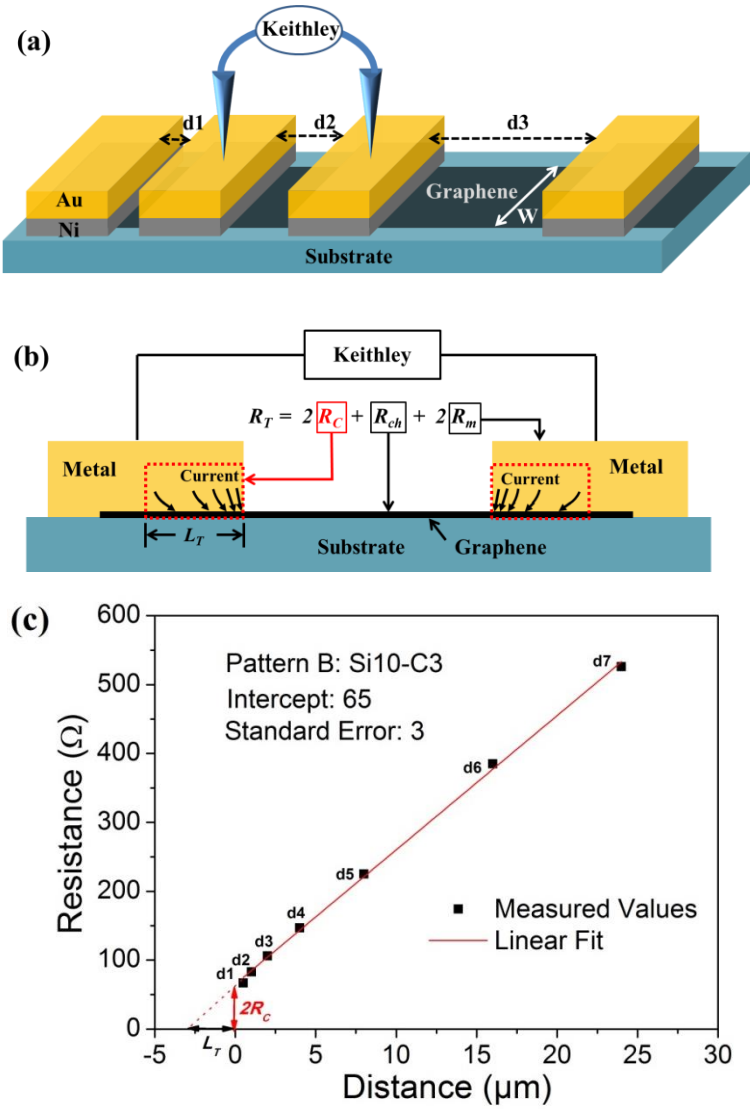


Figure 9 : (a) and (b) Schematic of TLM structures, (c) Example of a data plotting obtained from TLM structure on sample Si10

Appendix V

Table 4: Abbreviation

2-DEG	two-dimensional electron gas
AFM	Atomic force microscopy
ALD	atomic layer deposition
BOE	hydrofluoric acid buffer
Cgs	GFET bottom gates geometric capacitance
COPO	Copolymere, , e-beam resist
CPW	coplanar wave guide transmission line
C_Q	quantum capacitance
CVD	Chemical vapor deposition
DoD	Drop-on-Demand, printing technique
DOS	density of states
DUT	device under test, without de-embedding
E-BE	electro-beam evaporation, metal deposition method
EBL	Electron-Beam lithography
E_f	Fermi level position
FET	Field effect transistor
f_{max}	maximum oscillation frequency
f_t	cut-off frequency
$f_{t\text{-}int}$	intrinsic current gain cut-off frequency
GFETs	graphene field effect transistors
g_m	Transconductance
GSG	ground-signal-ground
H_{21}	Current gain
HB	Hall bar, method for Hall effect measurement
h-BN	hexagonal boron nitride
HEMTs	high-electron-mobility transistors
HOPG	highly oriented pyrolitic graphite
I_{ds}	drain current
I_{ds}	Drain-to-source current
I_{gs}	Gate-to-source current, leakage current
IPA	Isopropyl alcohol
ISS	impedance-standard-substrate
ITRS	International Technology Roadmap for Semiconductors
KAPTON	Polyimide, poly-oxydiphenylene-pyromellitimide, flexible substrate
LEDs	light-emitting devices
LRRM	Line-Reflect-Reflect-Match, calibration method
MBE	Molecular beam epitaxy
MIBK	Methyl isobutyl ketone, e-beam resist developer

MOFET	metal-oxide-semiconductor field-effect transistor
NL	neutral layer
NP	nano-particle
n_s	sheet carrier density
OE-A	Organic Electronics Association
OTFTs	organic thin film transistors
PDMS	Polydimethylsiloxane
PEN	Polyethylene naphthalate, flexible substrate
PET	Polyethylene terephthalate, flexible substrate
PI	polyimide
PMMA	polymethyl-methacrylate, e-beam resist
R_C	Contact resistance
RF	radio frequency
RFID	Radio-frequency identification
RIE	Reactive ion etching
S	S parameters, scattering parameters
SEM	Scanning electron microscopy
TE	thermal evaporation, metal deposition method
TLM	Transmission Line Method
U	Unilateral gain
VDP	Van der Pauw, method for Hall effect measurement
V_{ds}	Drain-to-source voltage
V_F	Fermi velocity
V_{gs}	Gate-to-source voltage
VNA	Vector Network Analyzer, microwave measurement
XPS	X-ray photoelectron spectroscopy
Z_C	Characteristic impedances
μ_H	Hall mobility, carrier mobility measured by Hall effect

Process technologies for graphene-based high frequency flexible electronics

Abstract

Flexible electronic has drawn growing attentions for past several years due to its largely potential applications. The objective of my PhD work is to develop devices based on flexible substrate, for RF applications. There are mainly two parts involved: (i) fabrication of passive devices (transmission lines, antenna, etc) using inkjet printing technology; (ii) fabrication of graphene field effect transistors on flexible substrate using graphene growth by CVD technique. This work is partially involved in the European Flagship program GRAPHENE, and the ANR program GRACY.

Inkjet printing is a promising fabrication technology for flexible electronics. The challenge of this technology is the quality and reliability of printed patterns in terms of geometry. Based on optimized printing parameters, the structures of coplanar wave guide (CPW) transmission lines with nice printing quality were realized (definition of 50 µm, resolution down to 20 µm). The RF characterization of these transmission lines combining the considerations of geometric dimensions, sintering temperature, and substrate bending are presented.

The outstanding electrical and mechanical properties make graphene suitable for flexible transistors. In this thesis, we have developed and optimized a new low temperature process based on back-gated structure either on rigid substrate than on flexible substrate (here kapton). From flexible transistors, we report as measured current gain cut-off frequency ($f_{t\text{-}DUT}$,without any de-embedding) of 39 GHz and maximum oscillation frequency (f_{max}) of 13 GHz in devices with 100 nm gate length and 12 µm gate width. This result is at the level of the state of art for flexible GFETs.

Key words: flexible electronics, inkjet printing, Graphene Field-Effect transistors, High-frequency characterization

Procédés technologiques pour l'électronique flexible à base de graphène

Résumé

L'électronique flexible est une thématique en plein essor, et impacte de nombreux secteurs applicatifs. L'objectif de cette thèse est de développer des composants sur substrats flexibles, pour des applications dans le domaine des radiofréquences. Elle est constituée de deux grandes parties : (i) la fabrication de composants passifs RF en utilisant la technologie d'impression par jet d'encre ; (ii) la fabrication de transistors graphène sur substrats flexibles. Ces travaux sont partiellement intégrés au projet Européen flagship GRAPHENE, et au projet ANR GRACY.

La technique d'impression jet d'encre est particulièrement adaptée à la fabrication de composants sur substrats flexibles. L'un des challenges de cette approche technologique est de pouvoir atteindre une définition et une résolution adaptée au fonctionnement en régime radiofréquence. Le travail mené dans cette thèse a permis de réaliser des lignes homogènes de largeur minimale de 50 µm, et une résolution (distance entre 2 lignes de l'ordre de 15 µm. Différents composants passifs ont été fabriqués et caractérisés avec succès, et ce même en appliquant des contraintes en flexion aux dispositifs.

Nous avons également développé et optimiser un procédé technologique, adapté à la fabrication de transistors à effet de champ à base de graphène (GFET), sur substrat flexible. Ce procédé présente un bilan thermique faible, et est basé sur l'utilisation d'une grille arrière à base d'aluminium dont l'oxyde naturel sert d'oxyde de grille. De nombreux transistors ont été fabriqués sur substrat kapton, et avec un bon rendement. Les meilleures performances en termes de fréquence de coupure du gain en courant (f_t=39 GHz) et la fréquence maximale d'oscillation (f_{max}=13GHz) ont été mesurées sur un transistor de longueurs de grille Lg=100 nm et un développement de 12 µm. Cette performance est à l'état de l'art de GFET flexibles. Ces performances sont conservées pour des contraintes atteignant 0,5%.

Mots clefs: Electronique flexible, Impression jet d'encre, GFETs, Charactérisation HF