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Processeur Numérique/RF Adaptatif pour Émetteur Sans Fil Multi-bandes Multi-standard Faible Consommation à 5 GHz et 60 GHz

Scalable Digital-to-RF Processor for Multi-standard and Multi-band Low Power Wireless Transmitter in 5 GHz and 60 GHz

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Abstract

Proliferation of application specific wireless communication standards have resulted in the multiple standards, multiple devices for one user scenario of today. Consequently, research in multi-standard, and multi-band systems, architectures, and circuits has been a popular theme. The vision is to have devices which can hope seamlessly from one network to the other while delivering excellent functionality on different radio access technologies.

Configurable transmitter architectures targeting complementary use cases of the multi-Gb/s WiFi-WiGig standards have been studied. Novel approaches based on high speed configurable semi-digital FIR DACs are proposed and published in international journal. In this architectures, transmitter mask and linearity requirements are respected because the single-bit FIR DAC is inherently linear and combines in its functionality both digital-to-analog conversion and filtering of noise. A delta-sigma modulator can be employed for resolution conversion so that baseband signals with wide range of bandwidths and resolutions are processed.

FIR DACs require long filters with high resolution coefficients to achieve stopband attenuation levels that meet out-of-band noise requirements. Normally, this limits high speed multi-standard operation, and results in large silicon area and complex layout. In this work, circuit techniques are developed so that a unit circuit element realizing a coefficient of one transfer function can be re-used in realizing a different-valued coefficient of another transfer function. This multi-modal hardware-sharing capability of the FIR DAC is maximized by system-level coefficient optimization.

The work also proposes topologies that exploit digital signal processing at advanced nodes to implement quadrature modulation while realizing up conversion, digital-to-analog conversion and image and quantization filtering in one configurable passband FIR DAC block.

A prototype high pass filter FIR DAC chip which can be configured for the operation of the IEEE 802.11ac and IEEE 802.11ad standards was implemented in STMicroelectronics® CMOS 28nm FDSOI technology. The test of this chip has demonstrated the validity of the proposed transmitter architectures. The prototype chip can process passband OFDM signals as wide as 136 MHz at a clock frequency of 3 GHz and reaches an output carrier frequency of 1.5 GHz in the 802.11ac mode. It also can channelize random SC signals as wide as 700 MHz at a clock frequency of 1.4 GHz and reaches an output carrier frequency of 700 MHz. The chip has a total power consumption 103.07 mW in the 802.11ac and 86.89 mW in the 802.11ad modes at 1.4 GHz clock frequency. It is supplied with three separate voltage

supplies: the digital circuits work from 0.6 V to 1.55 V, the analog output network requires a supply of 1.2 V and the biasing circuits are supplied with a separate 1.2 V.

Key words: *WiFi, WiGig, IEEE 802.11ac, IEEE 802.11ad, WLAN, Transmitter, Multi-standard, Multi-band, Multi-mode, Configurable, DAC, FIR, DRFC, DDRM, High pass, Low pass, Band pass, Delay line, Filter, Delta-Sigma, Half-Band, DSP, CMOS, FDSOI, 28nm*

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Contents

List of Figures

List of Tables

Nomenclature

Symbols

ω & f	Angular frequency & frequency
σ	Standard Deviation
A_p	Passband Ripple
A_{st}	Stopband Ripple
f_{out}	Output Frequency
f_s	Sampling rate, also clock frequency
g_m	Transconductance
g_{ds} & r_o	Drain-to-source conductance & resistance
L	Transistor length
P_{out}	Output Power
V_{OV}	Overdrive voltage
W	Transistor width

Abbreviations

1G	First Generation Wireless Communication
3G	Third Generation Wireless Communication
4G	Fourth Generation Wireless Communication
5G PPP	5G Infrastructure Public Private Partnership
5GNOW	Fifth Generation Non-Orthogonal Waveforms for Asynchronous Signalling
5G	Fifth Generation Wireless Communication
ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
BW	Signal Bandwidth
CDMA	Code Division Multiple Access
CIFB	Cascade-of-Integrators, Feedback Form
CMOS	Complementary Metal Oxide Semiconductor

CRFB	Cascade-of-Resonators, FeedBack Form
CVSL	Cascode Voltage Switch Logic
DAC	Digital to Analog Converter
DBPSK	Differential Binary Phase Shift Keying
DCO	Digitally Controlled Oscillator
DC	Direct Current
DIDIMO	Direct Digital Modulation
DMG	Directional Multi Gigabit
DNL	Differential Non-Linearity
DR	Dynamic Range
DSP	Digital Signal Processing
EDGE	Enhanced Data rates for GSM Evolution
ETSI	Mobile and wireless communications Enablers for the Twenty-twenty Information Society
EVM	Error Vector Magnitude
FDMA	Freqeuncy Division Multiple Access
FDSOI	Fully Depleted Silicon On Insulator
FEC	Forward Error Correction
FIR	Finite Impulse Response
FM	Frequency Modulation
FSK	Frequency Shift Keying
GCD	Greatest Common Divisor
GPS	Global Positioning System
GSM	Global System for Communications
HDMI	High Definition Multimedia Interface
HD	Harmonic Distortion
HPF	High Pass Filter
I/Q	Inphase-Quadrature
IDFT	Inverse Discrete Fourier Transform
IFFT	Inverse Fast Fourier Transform
IF	Intermediate Frequency
IIR	Infinite Impulse Response
IMD3	Third-Order Intermodulation
INL	Integral Non-Linearity

ISI	Intersymbol Interference
LO	Local Oscillator
LP	Low Power
LSB	Least Significant Bit
LTE-AG	Long Term Evolution Advanced
MAC	Media Access Control
MCS	Modulation and Coding Scheme
MIMO	Multiple Input and Multiple Output
MU-MIMO	Multi-User MIMO
NRZ	Non-Return to Zero
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency Division Multiplexing
OSR	Oversampling Ratio
PAPR	Peak to Average Ratio
PA	Power Amplifier
PDAC	Power DAC
PHY	Physical layer
PLL	Phase Locked Loop
PM	Phase Modulation
PRBS	Pseudo-Random Bit Stream
PSD	Power Spectral Density
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non Leaded
QPSK	Quadrature Phase Shift Keying
RAT	Radio Access Technology
RRC	Root Raised Cosine
RZ	Return to Zero
SC	Single Carrier
SDR	Signal to Distortion Ratio
SFDR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
STA	Station
TDMA	Time Division Multiple Access

TPSC	True Single Phase Clock
UCC	Unit Current Cell
UMTS	Universal Mobile Telecommunications System
VCO	Voltage Controlled Oscillator
VHT	Very High Throughput
WCDMA	Wideband Code Division Multiple Access
WENDY	**W**iGig Fl**E**xible Tra**N**sceiver A**D**vanced S**Y**stem
WiGig	Wireless Gigabit
WiGig	Wireless Gigabit
WiHD	Wireless High Definition
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network
ZOH	Zero Order hold

Chapter 1

Introduction

1.1 The Scope of this Study

The aim of this work has been to analyze, design, and demonstrate a digital-to-IF/RF converter circuit that can be configured for processing both high resolution, medium bandwidth and low resolution, wideband baseband signals of recent WiFi standards. Initially, FIR DACs were proposed as ideal blocks to achieve the required design objectives, such as low power consumption and small area, of such a mixed-signal circuit block. Along the course of this PhD work, however, the work has evolved to study and determine how much a performance can be expected from the digital signal processing blocks in a baseband of such transmitters.

The initial goal of this work was to validate at system-level a transmitter baseband architecture for processing IEEE 802.11ac and IEEE 802.11ad signals. Subsequently, given time constraints, it was important to demonstrate a key circuit block, by measuring a CMOS implementation, of the mulit-standard transmitter architecture proposed. A configurable FIR DAC was identified as the bottleneck in the transmitter chain as it determines the maximum achievable carrier frequency and the corresponding signal bandwidth, spectral purity of the analog output, and the lowest power consumption and circuit area that can be targeted.

Even though the solid literature in the area of traditional multi-bit DAC has eased the burden of derivation required in the design of a configurable multi-standard FIR DAC, the scarcity of works in the specific area of high speed configurable FIR DACs required analysis of each design decision and has led to some original contributions.

A top-down research methodology was followed during implementation of the FIR DAC chip. The specifications for the baseband transmitter system were based largely on IEEE 802.11ac and IEEE 802.11ad transmitter standard requirements. Specification for each block in the baseband chain, mainly the FIR DAC block, were then drawn; and those were translated as targets for the parameters of the FIR DAC circuit. Then, simulation at transistor, layout and extracted abstraction levels were carried out until the desired margin was respected.

1.2 Original contributions

These are the main original contributions of this PhD work:

- Novel digital wireless transmitter architectures based on:
  - low pass filter FIR DAC
  - high pass filter FIR DAC
  - band pass filter FIR DAC
- System-level validation of a configurable low pass filter FIR DAC transmitter as communicated in [GFK16a]
- A semi-digital FIR DAC for LP SC 60 GHz IEEE 802.11ad as communicated in [GFK15]
- Matlab based modeling and simulation alogrithms for EVM of a IEEE 802.11ac/ad transmitter
- A delay-line of a 1-bit FIR DAC configurable for a LPF/BPF/HPF operations
- Thorough small-signal analysis of the noise-limited dynamic range of a differentially-switched cascode current source
- A novel pseudo double common centroid placement method for unary-implementation of a FIR DAC as communicated in [GFK16b]
  - Analysis of its bandwidth limitation
  - A novel floorplan based on this placement method
- A yield model for thermometric FIR DACs based on stopband rejection of their filtering transfer function
- Design of a prototype FIR DAC that
  - is configurable for 160MHz channel bandwidth of the IEEE 802.11ac and IEEE 802.11ad standards
  - proves for the first time a low power, multi-GHz operation of a 63-order 1-bit high pass filtering FIR DAC
- The prototype high pass FIR DAC chip is characterized up to a clock frequencies of 3 GHz in the 802.11ac mode, consumes 103.07 mW at 1.4 GHz, and can process passband OFDM signals as wide as 136 MHz. In the 802.11ad case, it can processes SC signals up to a bandwidth of 700 MHz at a clock frequency of 1.4 GHz and consumes 86.89 mW.

1.3 Outline

The work is divided into eight chapters as follows:

- Chapter 1: introduces the problem statement the work has tried to solve. It sets the scope of the study, lists the main original contributions, and gives an outline of the dissertation.
- Chapter 2: examines the historical background of the application area of this work. It recapitulates the predictions related to the capabilities of future 5G standards, and introduces the principal challenges and solutions. The chapter puts the application of this PhD work in perspective with the predicted possible evolution of radio systems.
- Chapter 3: briefly introduces theoretical operation of a modern wireless transmitter. It reviews digital cartesian transmitter architectures. It further delves into review of multi-modal digital transmitters architectures in recently published works. The chapter closes with a proposal of novel FIR DAC based multi-modal transmitter architectures.
- Chapter 4: starts with basics of a traditional multi-bit DAC: its operation, specifications, and architectures. Then it follows it with a general discussion of the design challenges of $L-bit$, $N-tap$ FIR DACs. It introduces a novel configurable delay-line for a 1-bit FIR DAC. A thorough review of published transmitter-side filtering DACs paves the way for analysis of high speed 1-bit FIR DAC design. Main performance metrics of a 1-bit current-steering FIR DAC architecture and its modeling is derived.
- Chapter 5: presents the system-level validation of the baseband of a digital transmitter based on a low pass filter FIR DAC. High level design and simulation results of each block of the transmitter are included. The chapter ends with further discussion of the high level design of a configurable FIR DAC.
- Chapter 6: details the circuit implementation of a prototype configurable FIR DAC in 28nm CMOS FDSOI. A novel pseudo double common centroid placement method, and the FIR DAC floorplan are discussed. Design of each block of the prototype converter are presented in great detail.
- Chapter 7: is where the results of the measurement of the prototype are explored. The experimental setup, the different ways by which the configurable FIR DAC is characterized are elaborated.
- Chapter 8: stipulates the main conclusions. It also extends the scope of this work by proposing plausible future research directions.

Chapter 2

Wireless Communication Systems

The aim of this chapter is to give an overview of wireless communication standards. It covers a bit of history and a bit of the expected future of communication standards. Since the focus of this work is on multi-mode DAC for multi-standard transmitters, some motivations are listed in this chapter. It starts with evolution of standards in section I. In section II, a discussion of challenges and solutions with regard to 5G networks in included. The prototype chip targets the complementarity that exists in the WiFi-WiGig use cases; it is in section 3. The chapter closes with a customary summary and conclusions section.

2.1 Aggregation of Standards

Cellular technology has evolved from the analog, voice only 1G to the current Gb/s data rate LTE-A 4G standard. To accommodate this increase in throughput, the transmission frequencies has also increased from sub-GHz carrier frequency to 2–3 GHz range that is at work today. However, this increase is not totally attributed to increase in available transmission bandwidth. One technology that contributed to this increase is the evolution of access technologies from FDMA to TDMA to CDMA to contemporary access technology based on OFDM.

The same can be said of the evolution of the WLAN standards, namely WiFi. It has evolved from the early 2 Mb/s data rate local area network to the current multi-Gb/s 802.11ac/ad standards. Other standards including short distance, low power Zigbee and Bluetooth, and long distance, low data rate GPS still add their own set of requirements on the design of devices.

Therefore, the proliferation of application specific wireless communication standards have resulted in the multiple standards, multiple devices per user scenario of today. The need for design of multi-standard devices is exacerbated by the crowded spectrum, and the resulting tough out-of-band requirements. Moving to higher carrier frequency, and, thus, broader bandwidths could relax the requirements, and fulfill the increasing demand for faster communication rates. However, the challenges of designing multi-standard devices at higher carrier frequencies or broader bandwidths will be harder to overcome.

Innovation in access technologies, similar to the gains made by using OFDM, will not suffice either. A single innovation in either of transmission frequency, access technologies, channel bandwidth, or type

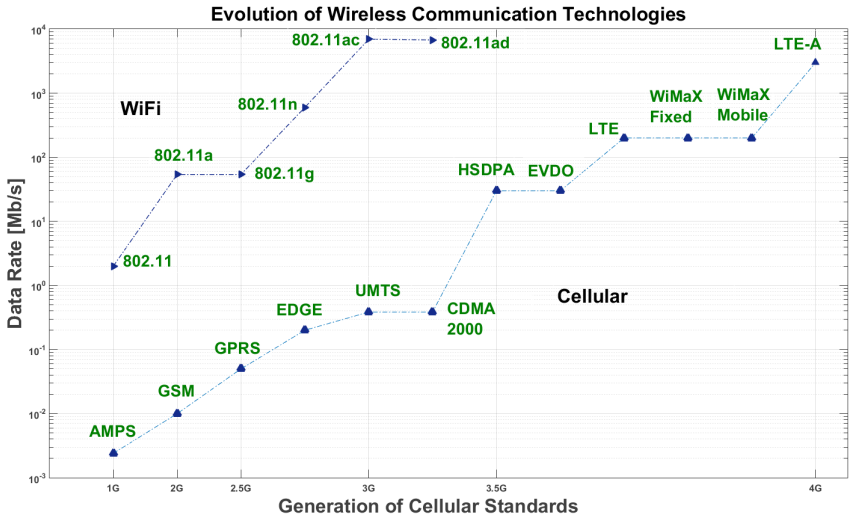


Figure 2.1: Evolution of theoretical data rates of wireless technologies from first generation networks to current giga-bit data rate 4G networks

of antenna may not satisfy the expected needs. A radical change combining all of the above solutions have a better probability of addressing the problem.

The evolution of theoretical data rates of cellular and WiFi standards through the years is plotted in Figure 2.1. The latest standards of WiFi achieve several Gb/s data rates—with the 802.11ac at 160MHz and the IEEE 802.11ad at 2.16GHz maximum channel bandwidths. The uplink and downlink data rates of the latest cellular standard also reaches Gb/s with a maximum of 20MHz channel bandwidth. There is, however, a difference in the achievable distance between these standards. For example, IEEE 802.11ad has an expected reach of less than 10 m. Future networks can be envisioned where the capabilities in both short and long distance standards are combined seamlessly for best user experience. In the next section, a brief summary of the discussion on future 5G networks is presented.

2.2 Networks of the future

Current networks are not expected to support the data demand of the future. This is because of the explosive rise in user data demand coupled with the increasing number of new applications that require low latency, high data rate communications. The 2015 virtual networking index report by Cisco shows that 4G mobile networks account for 47% of mobile data traffic with just 14% of mobile connections while 3G networks contribute for 43% traffic with 34% of connections. In general, a 4G traffic takes the biggest share with 85% more traffic than a non-4G connection. It also reports an increase of more than half a billion in global mobile devices and connections in 2015. Although the growth in mobile data and

increase in mobile devices does not imply similar proportion of growth in other networks, it does show the exponential demand for faster data. The mobile data traffic growth from 2015 to 2020 is shown in Figure 2.2 [CVM16].

These exponential demands have pushed many governing bodies to plan for the networks of the future. Flagship projects such as METIS 2020 project, 5GNOW, and 5G PPP in Europe, and IMT-2020 under the International Telecommunication Union have led the way for the development and standardization of 5G networks—a generic name for the networks of 2020.

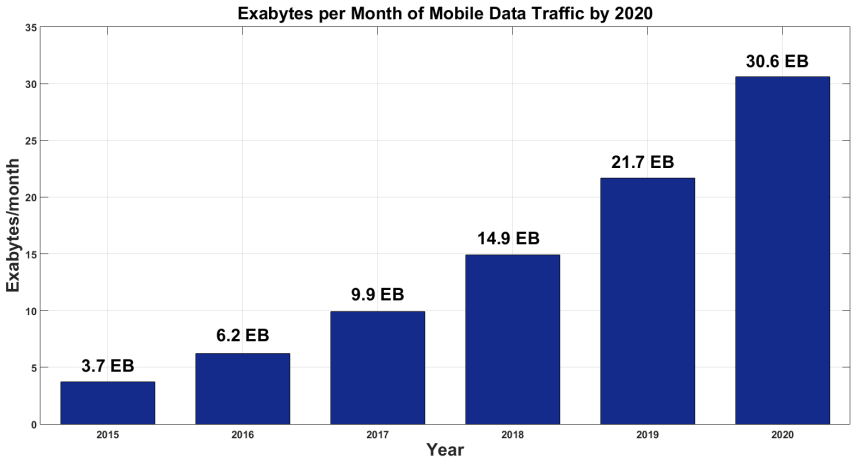


Figure 2.2: Mobile data traffic by 2020 as predicted by Cisco in [CVM16]. Global mobile data traffic is expected to grow eightfold between 2015 and 2020 with a compound annual growth rate of 53%

Although a clear set of requirements have not yet been developed for what the 5G networks should look like, there are some targets which show the capacity of the networks of the future. Under the IMT-2020, initiative, the expected capabilities and needed enhancement compared against the current IMT-Advanced are depicted graphically in Figure 2.3.

The METIS project, in its initial project, had also set five requirements that a mobile network in 2020 should support with the same cost and energy dissipation of contemporary networks. These are 1000x increase in mobile data throughput, 10 to 100x increase in number of connected devices and increase in user data, 10x longer battery life for low power massive machine communication, and 5x reduced end-to-end latency [Ola15]. These are achievable objectives with the technologies available today, but require innovation at the network, system and architecture levels.

Some of the techniques that has been mentioned for meeting these requirements include increase in bandwidth by moving to new unlincensed spectrum, denisification of networks with shorter transmission distance, massive MIMO with greater antenna elements, more efficient transmission schemes to improve OFDM, and flexible radio interfaces [Ola15].

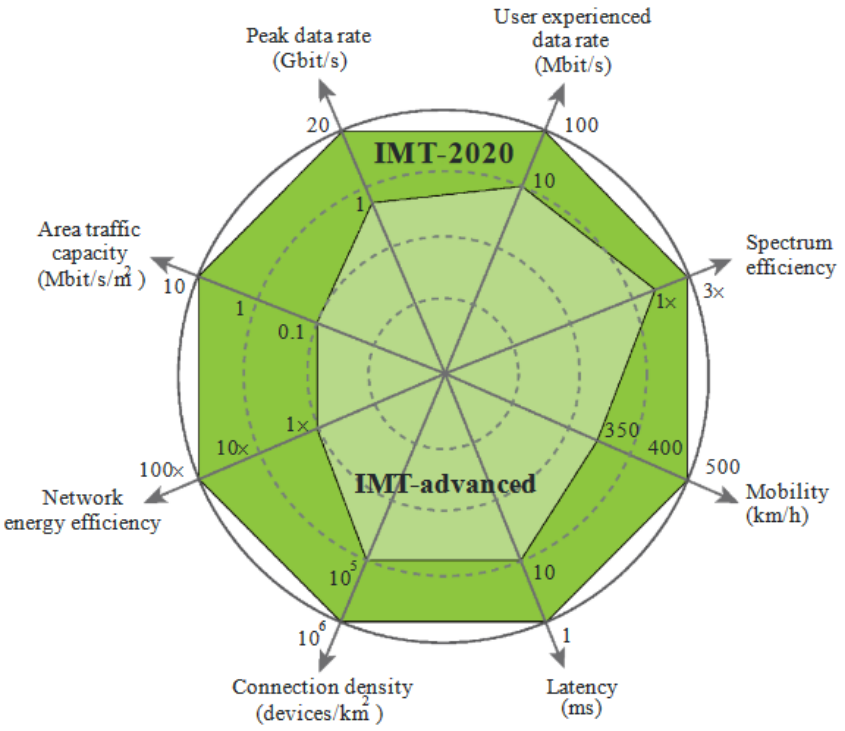


Figure 2.3: Expected IMT-2020 capabilities as compared with those of IMT-Advanced [ITU15]

2.2.1 Challenges and Solutions

Many of the proposed solutions are an extension of the current technologies. Still, there are many challenges that have to be overcome. A good depiction of the capabilities of a 5G device, with a focus to the communication block, is in Figure 2.4. It shows the challenges and the expected innovations at different parts of the device. For example, of interest to the scope of this work are the number of RATs the transceiver baseband is expected to process, the multi-standard design at the RF parts of the transceiver and the resulting challenges at the front-end module, and the expected challenges of a multi-antenna operation. In this subsection, a brief discussion of the challenges and solutions proposed for future 5G networks are presented.

One of the proposed solutions to free up spectrum and serve more users is decreasing the distance between base stations also called densification. While this allows the incorporation of short-distance communication standards in the 5G network, it faces some challenges, among which the cost of increased infrastructure due to deployement of large number of base stations within small area, and the support of fast and efficient handoff in an environment where there are many RATs [And+14].

A more viable solution for future high data rate networks is increasing bandwidth in an unlicensed spectrum. The challenges to this solution in the PHY layer are design of power efficient and small form factor transceiver architectures that can support MU-MIMO, and antennas that overcome the propagation

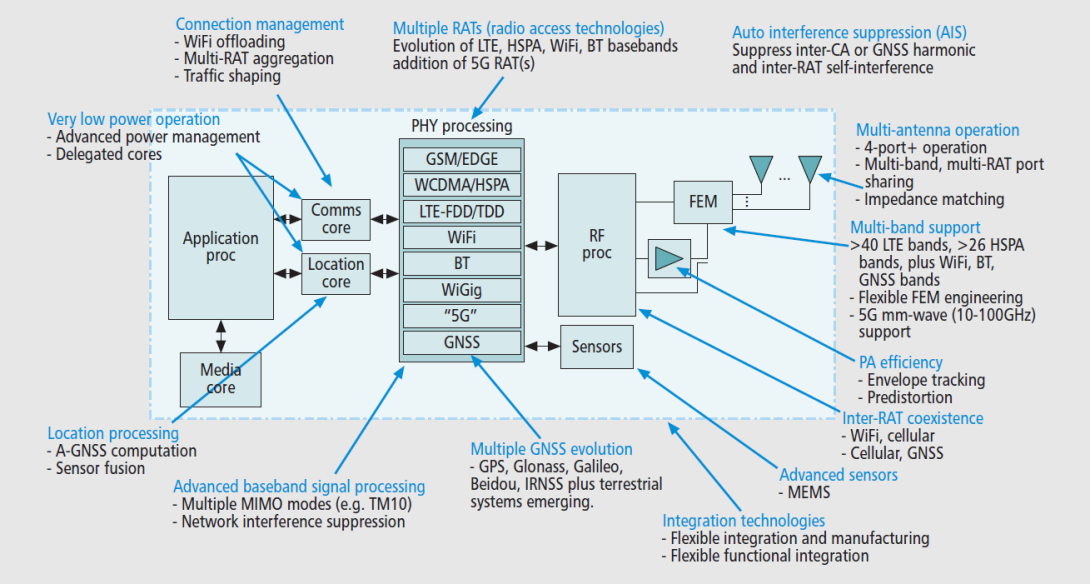


Figure 2.4: A 5G device will have to support multiple existing RATs and new ones. The expected capabilities that different parts of the device are shown here[Ban+14b]

loss and atmospheric absorption at mm-waves. These challenges are already being tackled by circuit and antenna designers at this time to some degree. Yet, novel architectures may be needed if massive MIMOs are to be part of mobile terminals [Ban+14b].

Another solution for increasing throughput is novel spectral efficient modulation technique and access technology. While OFDM is a widely used modulation technique, it presents drawbacks. One is the high PAPR that limits the linearity and efficiency of power amplifiers although this may not be a critical problem in a dense network where the transmitted signal does not need to have high power. The other is the need for synchronization and the fact that a big part of an OFDM symbol is taken by the guard interval. It is also a usual practice to fill the edge of an OFDM symbol with null subcarriers. This also results in decreasing the spectral efficiency of OFDM. A technology where the advantages of OFDM are kept with improvements on its drawbacks will be important for 5G networks. Some candidate technologies are already being proposed to supercede OFDM in a 5G network. They are discussed in detail in [Ban+14a].

2.3 The WiFi-WiGig Complementarity

The 802.11ad was developed from the WiGig MAC and PHY. However, WiGig has now merged with WiFi under the WiFi Alliance and standardized in 802.11ad.

Initially released in 1997, WiFi, as standardized by the IEEE 802.11, has hugely impacted the

medium distance local area and personal communications. The latest flavor, 802.11ac, enables WiFi to keep its medium distance capability and reach multi-Gb/s using MIMO. On the other hand, 802.11ad strengthens WiFi in for low power, short distance applications by increasing its capability to multi-Gb/s data rate without the need for MIMO and using simpler modulation schemes. The two standards have made WiFi an indispensable standard, and a candidate for highly dense future networks [VFC13].

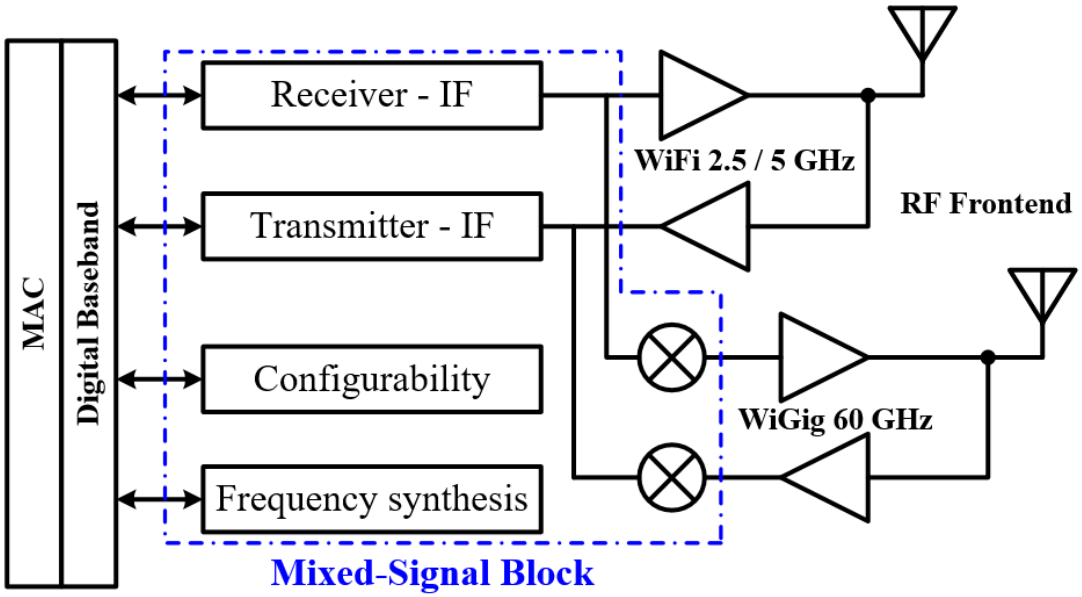


Figure 2.5: Block diagram of a configurable transceiver for WiFi and WiGig applications

The 802.11ac and 802.11ad standards have created a good test case for seamless operation of short distance and medium distance communications. Due to its high data rate at low power capabiities, 802.11ad can be used for tasks that require small time duration. For instance, device-to-device data transfer, wireless sync, and wireless display to name a few. Hence, it can be turned on for such tasks. On the contrary, the 802.11ac requires higher power consumption to reach Gb/s data rates. Thus, it is better suited for medium distance, traditional local area network applications.

2.3.1 Tri-band WiFi Radio

The 802.11n, 802.11ac and 802.11ad stretch the reach of WiFi from the crowded 2.4 GHz bands, to 5 GHZ, and mm-wave frequencies respectively. Both 802.11ac and 802.11ad are backward compatible. 802.11ac can be considered as a 5 GHz, wide channel bandwidth version of 802.11n. The idea of tri-band radio is to employ 2.4 GHz 802.11n for existing networks, 802.11ac for new faster medium distance applications, and 802.11ad for short distance, low power applications [VL11].

There has been some demonstration of this idea in commericial products with the Intel® Tri-band

Wireless-AC 17265 and WiGig Antenna-M10041R. The research in this area is to maximize hardware sharing between the mm-wave 802.11ad and 5 GHz 802.11ac while guaranteeing good performance.

Under the WENDY project of the French National Research Agency, the idea of tri-band radio was targeted. The objective of the project was to research techniques by which a 60 GHz standard could be part of the WiFi ecosystem with respect to how its use cases are entertained and how its circuits are implemented. It targeted the second generation of WiGig based products—the first being standalone WiGig chipsets. Although WiHD was released earlier than WiGig, it specifically targets video streaming application as HDMI cable replacement and was not suited, for instance, with respect to cost, for wireless transfer of general data of other nature.

To implement a highly integrated, configurable and low power tri-band transceiver, the MAC, digital baseband, and the RF front-end circuits should be configurable for operations in all bands. A common frequency synthesizer can deliver a low phase noise signal to all the baseband and mixing blocks at low power constraints. In the RF front-end, the project investigated among other issues how to:

- digitally process baseband signals ranging from 20 MHz to 2 GHz,
- implement digital-to-analog conversion of those baseband signals, and
- upconvert and downconvert IF and RF transmission frequencies of as diverse as 2.5 GHz, 5 GHz, 20 GHz and 60 GHz.

The general block diagram of the transceiver is shown in Figure 2.5. Prototype chips were fabricated for some parts of the tranceiver. In the receiver side, subsampling techniques were employed to solve the problems listed above [GFK13]. In the frequency synthesizer, a wide tuning range mm-wave voltage controlled oscillator was implemented in CMOS 28nm FDSOI [Val+14]. In the transmitter side, it should be understood that the starting objective of this thesis work was to investigate the questions listed above.

2.4 Summary and conclusions

An overview of wireless communication standards commensurate with the scope of this dissertation is presented. Special attention has been given to future networks in line with the initial aim of this PhD work. Recent literature on future 5G networks from both academia and industry is briefly introduced with focus on the challenges and proposed solutions.

Finally, a summary of the ANR project, WENDY, under which this work was started is introduced. The objective of the project was to demonstrate next generation tri-band WiFi transceiver. Design of a configurable mixed-signal block in the transmitter part of such a transceiver was the initial goal for this work.

Chapter 3

Multi-standard Digital Transmitters

This chapter investigates the methods that can be implemented for multi-standard transmitter operation. Before that, it will introduce briefly the theoretical operation of a transmitter. Signal processing in cartesian, polar and outphasing transmitter systems is discussed along with modulation schemes. The first section is closed with a highlight of the fundamental transmitter metrics such as transmit mask, EVM, and ACPR.

In the next section, I/Q transmitter architectures are discussed with additional details. It starts with classical architectures such as direct conversion or low-if, heterodyne or two-step transmitter architectures, and ends with a review of modern architectures used in wireless devices. Only the architectures with relevant specs will be discussed.

The last part of this chapter is a theoretical discussion of the possible methods available for implementing a multi-standard transmitter using the traditional architectures. The focus is on the opportunities in the baseband part of the transmitter. Similar to the previous section, this section closes with a mention of recent publications of multi-standard transmitters.

3.1 Brief Theory of Transmitter Operation

From the scope of this dissertation, the name transmitter will refer to the blocks in the lower part of Figure 3.1. However, for completeness, a general block diagram of a WLAN transmitter is shown including the MAC layer. The MAC layer prepares the data units that are exchanged with the PHY according to the transmission format of the standard. It adds the necessary header and defines the payload structure for each user. For example, the 802.11ac standard defines a MU-MIMO capability where an access point transmits data units to multiple receiving stations with one or more antennas. In this case, the MAC layer could define multiple independent data units. The data bits are filled in the PHY layer.

The physical layer mainly performs FEC, and modulation in its digital baseband part and, traditionally, frequency translation, digital-to-analog conversion, filtering and amplification in its analog/RF part. Modulation consists of constellation mapping where bit streams are mapped to complex constellation points, and where the complex symbols are converted to time domain blocks. In a single carrier

modulation transmitter, only constellation mapping is done, and the rest of the functions fall under the responsibility of the analog/RF designer. In other words, they are not necessarily implemented in digital baseband. That is the case in 802.11ad where the mapped high speed baseband data can be upconverted and converted to analog without much digital processing (more on this later).

However, advancement in digital signal processors have enabled digital implementation of traditionally analog blocks. The possibility to tune and calibrate digital circuits for best performance have relegated the analog implementation only to the blocks close to the antenna such as the power amplifier or co-existence band pass filter. With this comes the opportunity to implement different standards using one digital hardware. This is the main topic of the final section of this chapter.

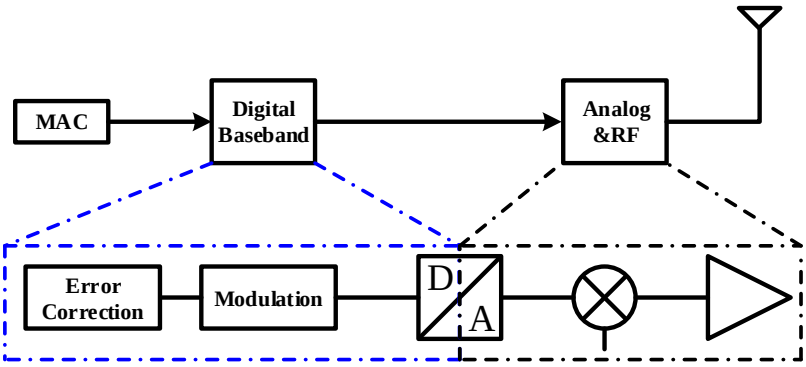


Figure 3.1: Essentials blocks of a basic WLAN transmitter. In traditional transmitter, the mixer follows the DAC. However, they can also be implemented in the same circuit.

3.1.1 Modulation

Modulation is the mapping of information carried in one electrical signal, called the modulating signal, into the amplitude, frequency, and/or phase of another signal, called the carrier. Modulation has many advantages in wireless communication which are well covered in many wireless communication text books [Hay09].

Single Carrier

There are three main modulation types. AM is when the modulating signal controls the amplitude of the carrier, it is FM when it controls the frequency, and PM if the modulation is on the phase of the carrier. Both FM and PM are called angle modulation because, ultimately, both phase and frequency variation can be obtained by varying the angle of the carrier. Each modulation types have different bandwidth efficiency. Probability of error versus energy per bit per spectral noise density ($\frac{E_b}{N_o}$) graphs are used for

comparing different modulations schemes.

An analog signal modulated by a single carrier of frequency, f_c, can be generally expressed in polar form as:

$$y(t) = a(t)cos(2\pi f_c t + \theta(t)). \tag{3.1}$$

This can be expanded to:

$$y(t) = a(t)cos(\theta(t))cos(2\pi f_c t) - a(t)sin(\theta(t))sin(2\pi f_c t). \tag{3.2}$$

The cartesian form of the modulated signal is then:

$$y(t) = x_I(t)cos(2\pi f_c t) - x_Q(t)sin(2\pi f_c t). \tag{3.3}$$

Where $x_I(t) = a(t)cos(\theta(t))$ and $x_Q(t) = a(t)sin(\theta(t))$. The modulating signal $x(t)$ is generally given by: $x_I(t) + jx_Q(t) = a(t)e^{j\theta(t)}$.

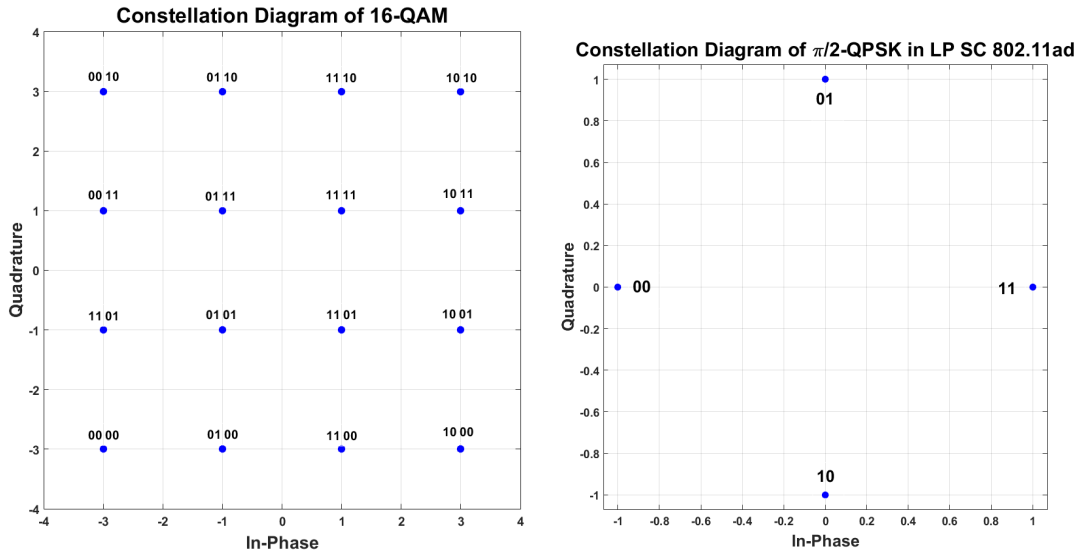
The amplitude $a(t)$ follows the modulating signal, $x(t)$, in AM with no modulating signal information on the phase $\theta(t)$; and the angle $\theta(t)$ varies according to the modulating signal, $x(t)$, in angle modulation with no modulating signal information on the amplitude $a(t)$. In digital modulation, the modulating signal is a sequence symbols. ASK, FSK, and PSK are the digital modulation versions of AM, FM and PM respectively. There are higher order digital modulation schemes such as M-PSK, M-ASK, and M-QAM which are more spectrally efficient. The constellations of 16-QAM and $\frac{\pi}{2}$-QPSK are shown as an example in Figure 3.2.

OFDM

Modern wireless communication standards such as IEEE 802.11ac rely on different mechanisms to increase spectral efficiency. Higher order modulation schemes are used to reach Gb/s data rates, for example, 256-QAM in 802.11ac. In addition, OFDM is used to increase throughput in a crowded spectrum.

The basic stages in the generation of one OFDM symbol in the baseband of a transmitter is shown in Figure 3.3. The stream of bits are converted to parallel and are mapped to N subcarriers according the complex constellation points of the modulation scheme selected. Then the orthogonal subcarriers are summed using an IFFT or IDFT block and converted to time domain. A guard interval is inserted at the end of the summed signal to prevent inter-symbol interference due to multi-path propagation. The IFFT output and the guard interval, can be implemented using cyclic prefix, form an OFDM symbol.

An example based on the 802.11ac standard is given in Figure 3.4 and 3.5. The symbol is generated by mapping a random bit stream to 468 16-QAM data subcarriers, 16 pilot subcarriers and the remaining



(a) (b)

Figure 3.2: Constellation diagrams of 16-QAM modulation in 802.11ac and 802.11ad standards, and $\frac{\pi}{2}$-QPSK modulation of the LP SC mode of the 802.11ad standard

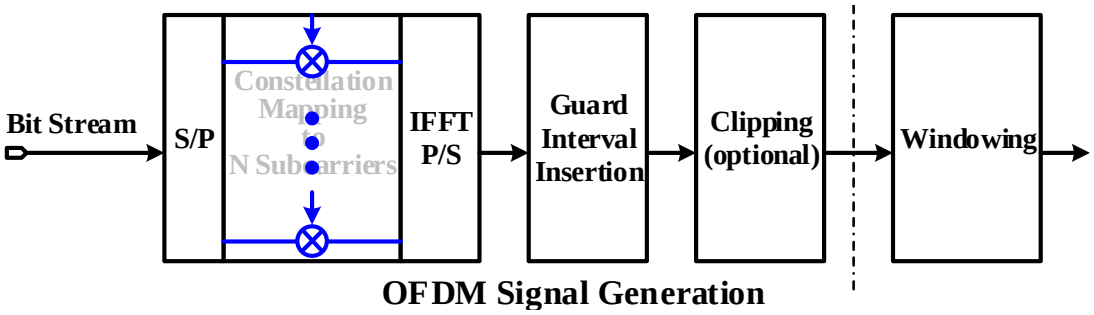


Figure 3.3: Basic blocks in the generation of one OFDM symbol

of a 512-subcarriers OFDM to zeroes or null subcarriers. The windowed spectral plot of the IFFT output is shown in Figure 3.4. The null subcarriers are placed in the middle of the symbol and at the end as guards subcarriers.

The roles of the remaining transmitter blocks are, basically, converting this signal to analog, frequency translating it to the band allocated to the standard and amplifying it. The first task can be carried out by using multi-bit DAC. The output signal, in time-domain, shown in Figure 3.5, has multi-bit resolution with the high magnitude samples occuring less frequently. The high magnitude samples can be clipped to relax the requirements on the DAC [MSB94]. The SNR loss that results from this process should not degrade the EVM to a degree where the remaining transmitter blocks are put on stringent EVM requirements. Depending on the constellation size, number of subcarriers of the OFDM modulator,

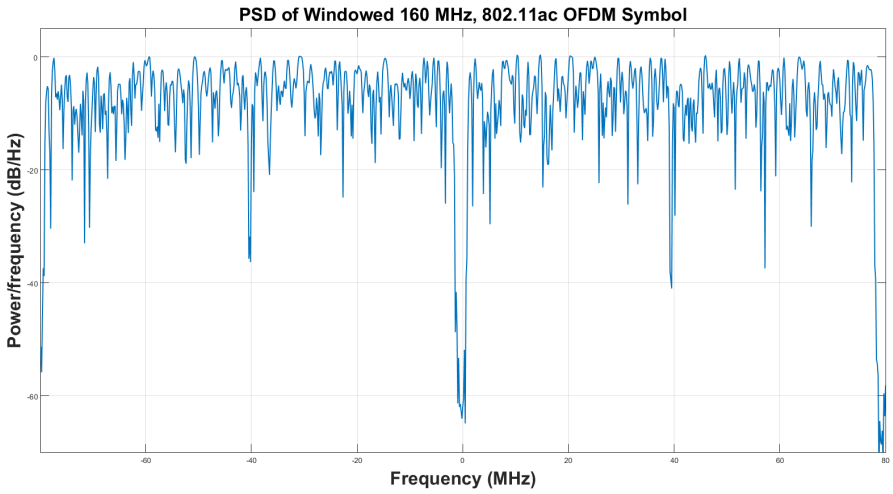


Figure 3.4: PSD of a 160 MHz, 802.11ac OFDM symbol using a hann window

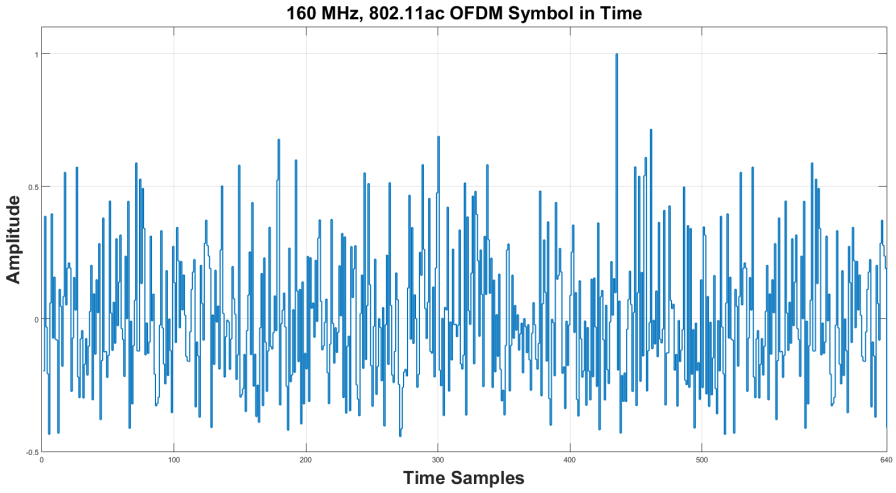


Figure 3.5: Time domain plot of a 160 MHz, 802.11ac OFDM symbol

the resolution of the DAC could be higher than 10 bits.

Frequency translation of the OFDM modulator output can be carried out in single stage or two-step depending on the transmitter architecture. It can also be implemented by digital upconversion if the mixer precedes the DAC, but this requires an RF DAC. If cartesian transmission is required, then the real and imaginary components of the OFDM output signal has to be transmitted separately using I/Q transmitter architecture [Raz12]. One of the main alterantive is to convert the complex samples to their amplitude and phase components and impart the amplitude on the phase modulated component in the amplifying block or upconversion block in a polar transmitter architecture [Yua03].

3.1.2 Cartesian Transmitters Architectures

Frequency translation is basically time-domain multiplication of the baseband output by an exponential signal at the desired carrier frequency, f_c. It is generalized by Equations (3.1) and (3.3) for SC signal. Mathematically,

$$y(t) = x(t)e^{j2\pi f_c t} \tag{3.4}$$

For a complex modulating signal $x(t)$, $y(t)$ can expressed by expanding the real, $x_I(t)$, and imaginary, $x_Q(t)$, components of $x(t)$ and multiplying by the exponential. Further, the exponential can be expanded using Euler's formula to its trigonometric equivalents:

$$y(t) = \left(x_I(t) + jx_Q(t)\right)\left(\cos(2\pi f_c t) + j\sin(2\pi f_c t)\right) \tag{3.5}$$

$$y(t) = x_I(t)\cos(2\pi f_c t) - x_Q(t)\sin(2\pi f_c t) + j\left(x_Q(t)\cos(2\pi f_c t) + x_I(t)\sin(2\pi f_c t)\right) \tag{3.6}$$

Therfore, complex upconversion can be achieved with four multipliers, two adders and a single-tone signal and it's 90^0 shifted component [Mar04]. Downconversion of the transmitted output is easily down by replicating the upconversion process in the receiver. There are practical problems resulting from the difference of the carrier signals in the receiver and transmitter sides, but theoretically $x(t)$ is fully recovered.

In I/Q modulation transmitter, upconversion is carried out with only the real part of Equation (3.4) as shown in Equation (3.7). This is possible because a real upconverted signal has also an image on the negative frequency. If the transmitted output signal is multiplied by the same orthogonal functions, cosine and sine, in the receiver, $x(t)$ can still be recovered after filtering. The clear advantage is the ease of generating the cosine and sine signals and the reduced number of multiplication and additions required. Both $x_I(t)$ and $x_Q(t)$ are translated to f_c and $-f_c$. The downside of using real version of the complex modulation is the image filtering problem in the receiver. Quadrature modulation is then:

$$y(t) = x_I(t)\cos(2\pi f_c t) - x_Q(t)\sin(2\pi f_c t) = \Re\left[x(t)e^{j2\pi f_c t}\right] \tag{3.7}$$

Direct Conversion Transmitter

Direct implementation of Equation (3.7) results in a single-step upconversion transmitter architecture, also known as direct conversion transmitter, shown in Figure 3.6. If there is no filter between the summed output of the mixers and the power amplifier, carrier leakage to the output from the mixers could be problematic [Raz12]. Another problem is the receive band noise floor can be affected by the outut from

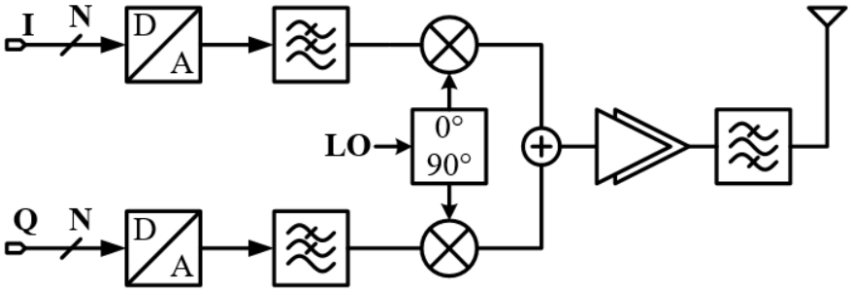


Figure 3.6: Direct Conversion transmitter

the transmitter. This problem can be addressed using digital signal proecssing techniques, or using a sufficiently high stopband rejection filtering after the DAC. The direct conversion architecture also suffers from injection pulling where the spurs of the power amplifier affect the phase of the local oscillator resulting in the output frequency of the oscillator shifting [Raz12].

Two-step Upconversion Transmitter

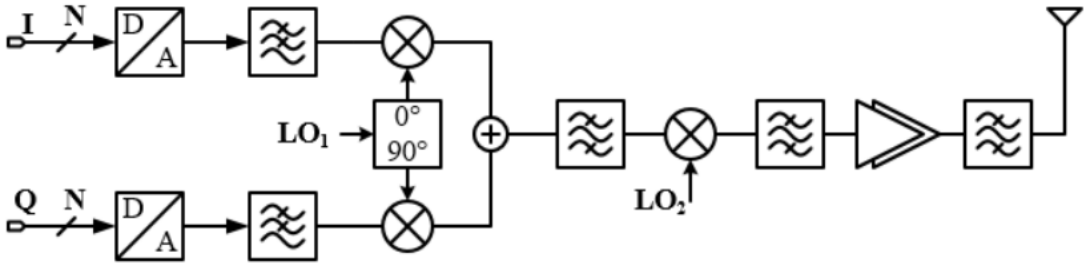


Figure 3.7: Heterodyne transmitter

Some of the problems of the direct conversion transmitter such as carrier leakage, and mainly injection pulling, can be solved by adding another stage of frequency translation in a two-step conversion transmitter or Heterodyne transmitter shown in Figure 3.7. The first stage mixers upconvert the baseband signal to an IF. Then the second mixer translates the IF to the final transmission carrier frequency at $f_{LO1} + f_{LO2}$. Quadrature modulation is performed at lower frequency with less effect from the PA. Nevertheless, the mixing products in the two blocks can interfere with each other and proper filter is required [Raz12]. Another problem of the heterodyne transmitter is the effect of the increased number of filtering and mixing stages on silicon area and power consumption.

3.1.3 Polar Transmitter Architecture

An alternative architecture to the cartesian-based transmitters is a polar transmitter architecture shown in Figure 3.8. The amplitude, also envelope, and the phase of the OFDM or SC baseband output are extracted for separate digital or analog processing. In a conventional architecture, the envelope controls the supply of a non-linear amplifier while the angle modulated bandpass signal is its input. It performs both PM and FM as $\omega(t) = \frac{d\theta(t)}{dt}$. The angle modulator can be a PLL with a DCO or a VCO.

One of the main limitation of this architecture is inherent to the nature of its amplitude and phase inputs. The fact that amplitude and the phase can change abruptly lowers the spectral efficiency of this architecture. This can be explained by following how the amplitude and the phase change during constellation mapping.

Any two consecutive data to be transmitted can take any two values in the complex constellation of the modulation scheme selected. This means the in-phase and quadrature components can assume any two values, 0 or 1, and change to the other in the next. Then there is a chance that the amplitude or magnitude of the complex points can move from a III-Quadrant to the I-Quadrant, from the IV-Quadrant to the II-Quadrant, or vice versa. This causes the amplitude component to abruptly change its time-domain value which creates a wideband spectra full of harmonics in the frequency domain. Similary, there is a chance the phase component can change its value abruptly by 180^0 which requires also broad bandwidth.

Thus, the polar architecture needs around 3 times bandwidth of their cartesian counterparts for effective representation of its amplitude and phase components [Wer13]. With limitation in maximum sampling frequency due to technological and power consumption issues, this main problem of the polar architecture limits its applicability to narrow-band applications.

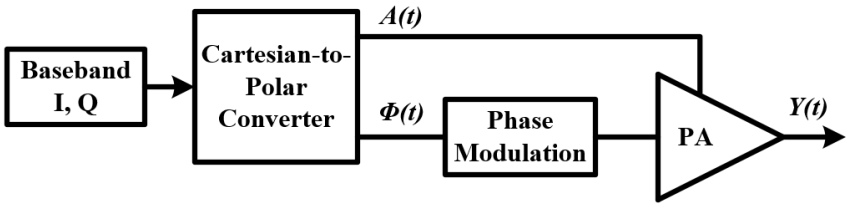


Figure 3.8: General block diagram of a polar transmitter

Another major disadvantage with this architecture is the different amplitude and phase branches. For perfect operation, the timing of the two branches has to be matched. This is difficult given the fact that they have different circuit blocks in each branch unlike the I/Q modulator. Dummy blocks can be inserted to lower the timing misalignments [NRD14].

A critical difference between the polar and the I/Q modulator transmitter is the way the output is obtained. In I/Q modulator, the output is a linear sum, at least ideally, but in the polar architecture it is a product of amplitude and phase components. This means spurs from each of the branches can mix and move to the desired bandwidth [NRD14].

Innovative circuit techniques have been used to mitigate most of the problems discussed above. A great deal of that discussion is in [NRD14; HS11]. For the sampling frequencies, and signal bandwidths targeted in this work, the polar transmitter is less effective. Hence, the reviews of the transmitters in this remaining part of this chapter are focused on the I/Q modulation architecture.

3.1.4 Transmitter Performance Metrics

Here some important transmitter parameters are defined. They are useful to the discussions in this manuscript. The main metrics are EVM, the spectral mask of the transmitter output, ACPR in the case of a simulation/measurement carried out using a proper channel of a standard. The simulation of the proposed transmitter architecture in Chapter 5 is assessed based on the parameters that will be briefly discussed in this subsection. There are also some less reported results at the baseband part of the transmitter such as the spectrum flatness. It is a measure of how much difference in power there is between the spectral tones of a desired channel bandwidth. A brief discussion of the rest follows.

Error Vector Magnitude

EVM is one of the parameters by which the modulation accuracy of a transmitter is measured. It is a measure of the degree by which the actually transmitted bits, after reception, decoding and measurement, are different from the intended ideal constellation. For example, for the SC PHY EVM of the 802.11ad, the EVM is calculated according to the formula [Int+14]:

$$EVM = 20\log_{10}\left(\sqrt{\left(\frac{1}{N_s P_{avg}}\sum_{i=1}^{N_s}\left[(I_i - I_i^* - I_0)^2 + (Q_i - Q_i^* - Q_0)^2\right]\right)}\right) dB \quad (3.8)$$

Where N_s is the number of samples, P_{avg} is the average power of the ideal constellation, I_i^* and Q_i^* and I_i and Q_i are the coordinates of the complex points of the i^{th} ideal and measured symbols respectively. I_0 and Q_0 are complex DC components which the designers can chose so that the EVM is reduced.

Several factors contribute to the degradation of the EVM. In an I/Q transmitter, an imbalance, whether in gain or phase, between the two channels leads to a shift of the received constellation points. Every circuit block in each channel contributes to this imbalance. In baseband, the bits to be transmitted are shaped using a pulse shaping filter to reduce ISI [Gu05]. These filters are designed for a flat passband so

that the frequencies components, or subcarriers in the case of OFDM, at the edge of the band does not experience a different gain.

Transmitter Spectrum Mask

The transmit mask defines the level of the output transmitted power at different frequencies from the center of the band. It is a primary restictions of a given standard. There are additional far-out spectrum restictions such as the out-of-band noise profile. The transmitter output power spectral density should be such that it does not raise the receive-band noise floor of communication standards at nearby frequencies. A discussion of this in relation to IEEE 802.11ad and IEEE 802.11ad standards is in available in Chapter 5.

Adjacent Channel Power Ratio

The occupied power is integrated for a given channel at a given resolution bandwidth of the output transimtted spectrum. The ratio of the occupied power of the main desired channel bandwidth to be transmitted to the adjacent channel is expressed by ACPR. ACPR is also sometimes called Adjacent Channel Leakage Ratio. The center of the upper and lower adjacent channels are usually defined as BW, the desired bandwidth, away from the center of the main channel bandwidth, i.e. with no gap between the main and the adjacent channels. Similar expression can be specified also for the upper and lower alternate, sometimes nonadjacent, channels. The ratio of the power occupied in the main channel to that of the upper or lower alternate channel is called the Alternate CPR.

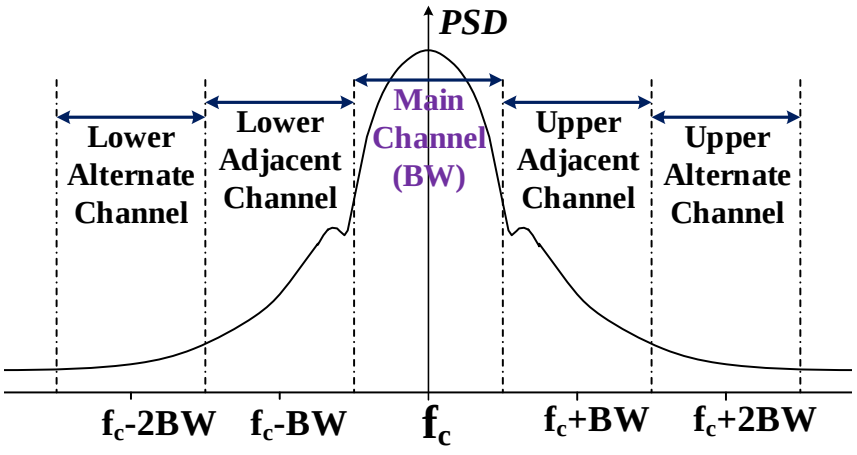


Figure 3.9: The ACPR is defined based on the spacing of the main, adjacent and alternate channels in this figure. The ACPR and Alternate CPR measurement results of Chapter 7 are also consistent with this definition.

An illustration of these definitions are shown in Figure 3.9. In this figure, f_c is the carrier frequency at which the desired channel is transmitted. Some standards such as GSM and CDMA specify the width of the adjacent channel and the offset frequencies at which the estimation or measurement should be done.

3.2 Review of Digital Transmitter Architectures

Advanced CMOS technologies have opened the opportunity to leverage digital signal processing in assisting or replacing the analog front-end of wireless transmitters. The objective in the design of transmitter has been then to push the realm of DSP towards the antennna at the same time reducing the pure analog blocks. As the DSP blocks are more scalable, and configurable, the transmitter as a system becomes more flexible for multi-modal operation.

Architecturally, there has been attempts, regardless of their effectiveness, in simplifying or totally taking out the analog reconstruction filter following the DAC, even pushing the digital implementation all the way to the final amplifying stages by driving the PA by digital signals in PDAC-based transmitters. In this section, recent digital transmitters in literature are discussed.

3.2.1 Digital Quadrature Modulators

Traditionally, quadrature modulation is carried out using multipliers. Multiplier-free digital domain implementation of quadrature modulation is reported in [Van+03]. Selected samples of the orthogonal Cosine and Sine signals are multiplied with input I and Q digital signals for frequency translating these inputs to fractional frequencies of f_s—anywhere from baseband (low pass) to $\frac{f_s}{4}$ (band pass) to $\frac{f_s}{2}$ (high pass) sections of the first Nyquist zone. The output summed complex data was used to drive a 12-bit segmented DAC to obtain the analog IF. The concept is validated for GSM, EDGE, and WCDMA. The desired transmit filters are met by oversampling the input I and Q signals using half-band interpolation filters.

Due to the limit on the highest sampling rate of the DAC, 500 MHz, the digital quadrature modulation of the above implementation was valid only as replacement for the first analog mixer stage. Another frequency translation stage is required.

A more advanced CMOS node was used in [Fra+09] where the first 1-bit digital RF signal generator using delta-sigma modulation was reported. It implements the baseband DSP and I/Q modulation of a delta-sigma based digital-IF transmitter in 90nm CMOS chip. A low pass delta-sigma modulator converts a moderately oversampled high resolution input to single-bit as shown in Figure 3.10. This architecture is validated for WCDMA application and some cases of the UMTS standard.

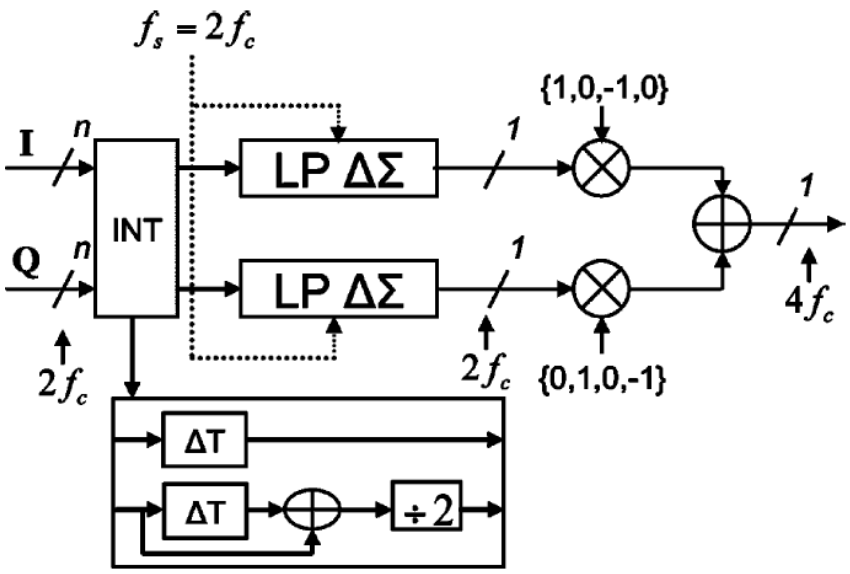


Figure 3.10: Block diagram of the digital quadrature mixer based on LPF ΔΣ modulator in [Fra+09]

A higher frequency band is achieved in this work, and it shows that the 1-bit digital I/Q modulated output, $\frac{f_{clk}}{4}$, can be directly used to drive a DAC without the need for analog frequency translation. In [Fla+08] the realm of the digital is further pushed to the antenna by feeding the digital 1-bit output to PDACs to implement the power amplifier. Quantization noise filtering is performed using bandpass FIR filters embedded in the PDAC structure.

The above two works show that for below 3-GHz bands, an analog frequency translation circuit may not be needed. Direct digital-to-analog conversion of the output of a digital quadrature modulator may suffice. To reach higher bands, though, different architectures have been proposed. One of them is using RF DACs. In the following sub-section, works employing the RF DAC concept are reviewed.

3.2.2 The RF DAC Concept

The RF DAC concept is the mergig of the digital-to-analog converter and mixing stages of a direct conversion transmitter into a common circuitry. In a current-steering architecture, the unit cell of the conventional DAC is replaced by the circuit of a Gilbert mixer whose RF inputs are driven by digital data destined to the DAC [Moh+12]. With some design choices, such as the LO frequency being at integer multiples of the clock driving the digital data so that the output power is higher than what is normally achieved with a $sin(x)/x$ response of the DAC, the conversion and mixing functionalities are delivered [LSH04].

RF DAC In Direct Conversion Architectures

Early demonstration of the RF DAC concept is in [YJ03] using L-fold interpolation. In ZOH sampling, a data is sampled by a clock rising or falling edge and the next data in the next clock cycle. The idea with L-fold interpolation is instead of waiting for the next clock cycle holding the actual value, the output of the DAC can be made to progressively increase/decrease, L times, in one clock cycle. Since the holding times are shorter, Fourier Series indicates that the frequency response rolls faster for a high image rejection. However, due to increased number of unit current cells and high number of clock activity, high power consumption is expected. The concept is demonstrated for L=16, for a 3.3 MHz input bandwidth at 50 MHz clock and 1 GHz carrier frequencies.

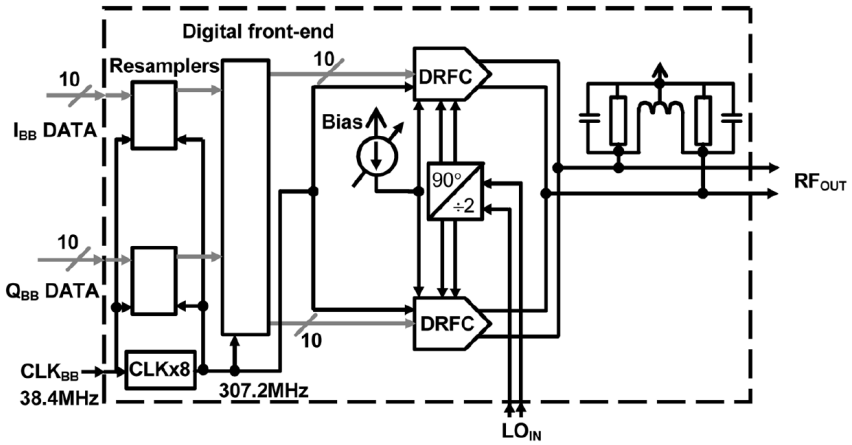


Figure 3.11: Block diagram of the DDRM in [Elo+07]

Another early demonstration of the RF DAC concept using an RZ output is in [LSH04] for a half-GSM bandwidth of 17.5 MHz at a center frequency of 942 MHz in 0.18μm CMOS. The carrier frequency reached, however, does not show the advantage of the RF DACs over the digital quadrature modulators discussed above.

Naturally, a high order analog output LC BPF is used for filtering of emissions in RF DACs. In [Elo+07], a DDRM, shown in Figure 3.11, was implemented in 0.13μm CMOS. Front-end digital filters are used for performing most of the transmit mask requirements of GSM/WCDMA/WLAN standards. In this work, the output of the DDRM can be transmitted without an additional frequency translation circuit.

The number of mixing unit cells of the RF DAC can be lowered by inserting a delta-sigma modulator. The shaped quantization noise is filtered by a combination of output analog filter and high OSR. This method increases the operating speed and results in higher power consumption. In [Poz+08], a combination of FIR and IIR digital filters perform most of the channel shaping while oversampling the data by

more than 60. The delta-sigma modulator is used to decrease resolution of data input to the RF DACs. Similar techniques are used in [Moh+12].

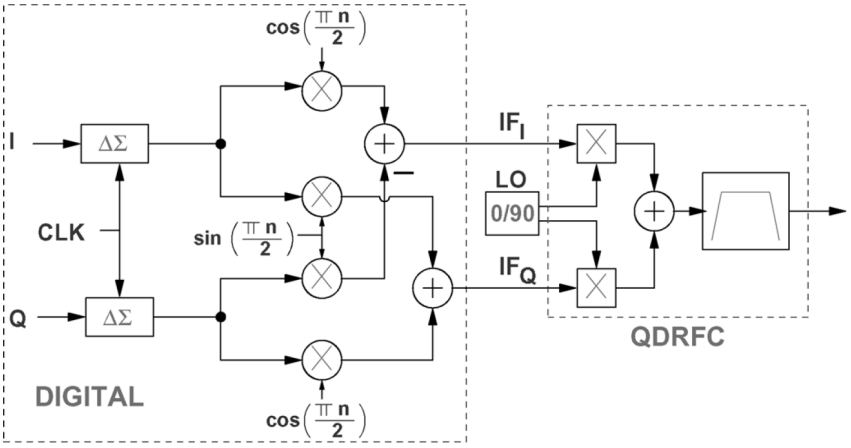


Figure 3.12: Block diagram of the digital-IF direct conversion transmitter in [JS07]

RF DAC and Digital PA

In [Ala+14], digital IQ modulation is further pushed to include some level of power amplification using digital-to-RF amplitude converters. The converters are formerly used in a polar transmitter architecture in [Cru+05]. They are combined with the RF DAC concepts in a direct conversion transmitter architecture. The I/Q modulation is carried out using four 25% duty-cycle non-overlapping LO signals. Each LO phase switches either positive or negative components of the in-phase or quadrature inputs. Output summing is realized by using an on-chip balun combining network. The concept is demonstrated in a $2x$13-bit DAC 65nm CMOS implementation. ACPR of -19dBr is obtained for a 154.1 MHz bandwidth, 1024-QAM, SC input at 2.4 GHz output frequency, and up to -44 dBr ACPR for 7 MHz input using digital predistortion.

RF DAC in Heterodyne Architectures

In [JS07], shown in Figure 3.12, two-step upconversion is implemented in a direct-conversion transmitter architecture. Delta-sigma modulators are used for lowering input data resolution in a moderate OSR operation. The first-step complex mixing translates the digital data to $\frac{f_{clk}}{4}$ while canceling either negative or positive frequency replicas. The second-stage upconversion is implemented using an RF DAC with an output 4^{th}-order Bessel LC BPF tunable for a wideband 260 MHz transmission.

In two-step upconversion digital transmitters, the RF DAC can implement second stage mixing of summed complex data. Thus, the I/Q modulation can be performed in the first stage mixing at lower

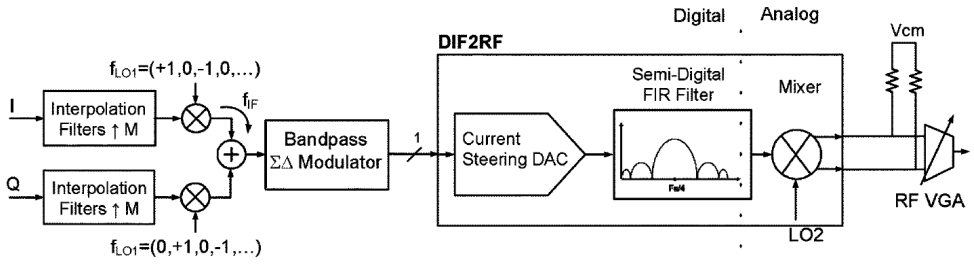


Figure 3.13: Block diagram of the digital-IF transmitter with embedded FIR filtering RF DAC in [Tal+08]

speeds. In [Tal+08], shown in Figure 3.13, a digital-IF heterodyne transmitter [LLG04] inspired architecture implements a bandpass delta-sigma modulator that converts the high resolution quadrature output to single-bit stream for second-stage upconversion using FIR RF DAC. The filtering of the shaped quantization noise is performed using the embedded six-tap bandpass FIR filter of the RF DAC. Depending on the order of the FIR filter, the output analog filter is relaxed. Any analog filter implemented is only for far-out spectra filtering to mitigate emission to nearby communication. For high stopband rejection and meeting the transmit mask requirements of modern wireless standards, the FIR filter has to be high order with high resolution coefficients. This digital-IF transmitter reports a bandwidth of up to 15 MHz bandwidth at 1 GHz LO frequency.

The summary of the reviewed digital transmitters is in Table 3.1. The main characteristics of the works are tabulated. The differences in their architecture with respect to their upconversion stages, the number of RF signals processed in their conversion stage, the main co-existence filtering mechanisms, order of a $\Delta\Sigma$ used and the resolutions of their DACs are contrasted. In addition, measurement results relevant to the discussion in this section are compared. Although some of the works have higher clock rates, and most of the RF DACs have both clock and LO frequencies, they are compared by the final f_c, carrier frequency, at which the data can be transmitted.

3.3 Multi-standard Digital Transmitters

Due to the various applications and radio standards that address them, devices are expected to operate over wide spectrum while maintaining the usual requirements such as efficient power management and small form factor. To address these demands, system, and architectural level solutions have been proposed [Mit09]. On transmitter circuit design, the challenges boil down to hardware reusability and ability to reconfigure the hardware for a range of channel bandwidths, modulation and coding indexes, power

* LO and $\frac{LO}{2}$ † L-fold Interpolation ‡ Not Used § Not Implemented, but can be embedded in PDAC

Table 3.1: Summary of the reviewed digital transmitters

Parameters	**[YJ03]**	**[LSH04]**	**[Elo+07]**	**[Poz+08]**	**[Moh+12]**	**[JS07]**	**[Tal+08]**	**[Fra+09]**	**[Ala+14]**
Conversion Stages	Direct	Direct	Direct	Direct	Direct	Two	Two	Direct	Direct
RF Signals	Clock + LO	Clock + LO	Clock + LO	LO *	Clock + LO	Clock + LO	Clock + LO	Clock	LO
Structure	RF DAC	RF DAC	RF DAC	RF DAC	RF DAC	RF DAC	RF FIR DAC	Digital Quadrature	RF PDAC
Co-existence Filtering	$\frac{sin(x)^2}{x^2}$ †	$\frac{\sin(x)}{x}$	Digital Filters + $\frac{\sin(x)}{x}$	Digital Filters + $\frac{\sin(x)}{x}$	$\frac{\sin(x)}{x}$	4^{th}-Order LC	Embedded FIR	N/I ‡	$\frac{\sin(x)}{x}$
DAC Resolution	10-bit	3-bit	10-bit	9-bit	9-bit	3-bit	9-bit	N/I	13-bit
$\Delta\Sigma$ *Order*	N/U §	Off-chip	N/U	3^{rd}	3^{rd}	2^{nd}	4^{th}	3^{rd}	N/U
Bandwidth	3.3 MHz	17.5 MHz	10 MHz	20 MHz	20 MHz	200 MHz	15 MHz	5 MHz	154.1 MHz
f_c	1 GHz	0.9 GHz	1.9 GHz	2.4 GHz	1 GHz	5.25 GHz	1 GHz	1 GHz	2.4 GHz
Supply Voltage	3.3 *V*	1.8 *V*	1.2 *V*	1.2 *V*	2.5—3.3 *V*	2.5 *V*	2.5 *V*	1 *V*	1.3 *V*
Technology	0.35μm CMOS	0.18μm CMOS	0.13μm CMOS	90nm CMOS	65nm CMOS	0.13μm SiGe 8HP BiCMOS	0.18μm CMOS	90nm CMOS	65nm CMOS

levels, and spectrum mask requirements.

Multi-standard operation could be achieved by reconfigurable circuit block, or an innovative architecture. Reconfigurability in circuit blocks is usually achieved by leveraging most transmitter operations to DSP or based on digitally-assisted analog circuits. A purely analog reconfigurable circuit would require big area, is less tunable, and power hungry. In this section, a review of recent multi-standard digital transmitters is presented with a focus to novel solutions in the digital-analog interface.

3.3.1 Multi-modal Transmitters in Literature

Wireless standards that are transmitted at nearby carrier frequencies with similar channel bandwidths, and whose transmitter parametric requirements—EVM, ACPR for instance—are quantitatively close to each other offer the best scenario for multi-modal circuit design. A set of common requirements can be drawn for each parameter, and a common circuit can be designed on those requirements. The multi-standard transmitter in some cases can have only one signal chain and without a need for complex external reconfiguration. This scenario was exploited in [Elo+07] with digital-to-RF converter based direct conversion transmitter for GSM/EDGE, WCDMA and WLAN. The WLAN transmitter has the stringent requirement in channel bandwidths (16.6 MHz), MCS (64-QAM), and EVM (5.6% with 64-QAM); the WCDMA transmitter has additional requirement which is a power control range of 74 dB; and the GSM/EDGE transmitter also requires a receive band noise of -162 dBc/Hz. The multi-standard transmitter in [Elo+07] has 10-bit digital-to-RF converters with an OSR of eight. This fulfills the receive band noise requirement. Filtering of images and quantization noise is done by a digital front-end IIR filter which also incorporates FIR filter with notches to target specific input signal replicas. Power control is provided by digital control of biasing current sources of the DRFC.

The innovative DRFC circuit block simplified the multi-standard design by eliminating the circuit blocks (mixer and analog reconstruction filter) which contribute highly to non-ideal performance in a traditional direct conversion transmitter. However, if one of the standards, say IEEE 802.11a WLAN, were replaced by a one with wider channel bandwidth, say 80 MHz of the IEEE 802.11ac, the approach would be difficult to follow. For one thing, high oversampling requirement, due to wider channel bandwidth, would push the clock rate to multi-GHz ranges, and design of a multi-bit, multi-GHz RF DAC while still fulfilling narrow channel bandwidth mask requirements is challenging. Additional DSP signal chains, or circuit blocks only specific to one standard, could be used with a common digital-analog interface. Otherwise, the DSP chain would be overly complex.

This is true in [Poz+08] where an RF DAC based direct conversion transmitter is demonstrated for all bands of WiFi-WiMAX standards. Additional oversampling signal chains are included to arrive at the

needed sample rates at the input of the digital-analog interface. Although many interpolation stages are used in the digital front-end to oversample the data by a factor larger than 60, the reliability of the digital circuits even at advanced CMOS nodes should enable them to deliver the expected performance.

In some works, only the blocks that are bottlenecks for realizing a multi-standard transmitter are presented. An implicit performance expectation is put on the remaining blocks of the transmitter. In [McM+14; Spi+13; EKR12], although their target applications are cable TV transmitters, they can be used for wireless communication standards. Direct sampling digital-to-RF converters are designed to support wideband input frequencies with the assumption that digital quadrature modulation is carried out at low IF frequencies using standard DSP blocks. Their input is then a complex output of that quadrature modulator. The clock speed of these converters reaches up to 5 GHz [Spi+13], 4.6 GHz [McM+14], 3 GHz [EKR12] and this enables them to convert GHz range input data frequencies. They do not support any filtering, mask requirements are fulfilled with sheer increase in resolution of the converters as shown in Table 3.2. In other words, the baseband quadrature modulation is carried out with no reduction in resolution. An analog filter at the output is necessary at least for image rejection.

Table 3.2: A summary of RF DACs for cable TV transmitters

References	Sampling rate	Resolution	Power	Effective Bandwidth	Technology
[Spi+13]	5 Gs/s	9-bit	375 mW	2.2 GHz	40nm CMOS
[McM+14]	4.6 Gs/s	14-bit	2.3 W	1 GHz	0.18μm CMOS
[EKR12]	3 Gs/s	14-bit	600 mW	1.5 GHz	0.18μm CMOS

While the approach is novel for multi-standard transmitter operation, they come at large power consumption cost even disregarding the power consumption of the remaining transmitter blocks. The reported bandwidth may be enough for most cellular applications. However, the output frequency of the quadrature modulator can not be guaranteed to be within that bandwidth.

Rather than increase the sampling speed of the DAC, it is possible to use n-path parallel RF DACs to target images which are very close to the fundamental signal so as to increase the supported input bandwidth [DPS04; Bal+12]. This is demontrated in [McC+15] where a reconfigurable 2-path parallel delta-sigma RF DACs sample the quadrature digital output of a digital-IF transmitter. The parallel $\Delta\Sigma$ RF DACs are clocked with 180^0 phase-shifted clocks to cancel input images. The $\Delta\Sigma$ modulators can be configurable for band pass or high pass noise shaping, at $\frac{f_s}{4}$, $\frac{f_s}{2}$, and $\frac{3f_s}{4}$, for processing wideband IF inputs. Although not shown, the digital quadrature modulator has also to support this reconfigurability. The concept is implemented in 130nm SiGe BiCMOS; it can process up to 50 MHz bandwidth at maximum sampling clock rate of 2 GHz for all $\Delta\Sigma$ modes.

Even though the achieved bandwidth is not wide enough for modern wireless applications, such as IEEE 802.11ac, the method of using n-path parallel ΔΣ RF DACs after the quadrature modulator is novel and interesting. The bandwidth can be improved by increasing the clock rate or the resolution. The image rejection is highly dependent on the timing delay difference between the two clocks. Thus, increasing the clock rate or the resolution does not scale linearly with image rejection as the former increases timing errors and the latter contributes to timing errors by increasing the number of elements to be clocked and the area. For high image rejection, incorporating an embedded image filtering into the structure and finding a trade-off between the filter order and the clock rate to improve timing alignment could enhance performance.

3.3.2 FIR DAC Based Multi-modal Transmitter Archtiectures

As a continuation to the discussion on multi-standard transmitters, in this sub-section, digital transmitter architectures based on FIR DACs are proposed. They are original contributions of this work. They are not previously published except one, in [GFK16a]. The system level results of this published work are presented in Chapter 5. The others are qualitatively discussed in relation with the IEEE 802.11ac standard.

Three of the architectures have similarity to those architectures based on mixing-DACs except they incorporate semi-digital filtering with no analog mixing. The second architecture is similar to the RF DAC implementation in [JS07] except it does not incorporate analog mixing.

LPF in Direct Conversion Transmitter

A LPF FIR DAC based direct conversion transmitter is shown in Figure 3.14. To maximize hardware sharing, the different input rates are resampled to a common sample rate. Then a delta-sigma modulator is used to decrease the resolution and its coefficients can be reconfigured to realize different OSR settings. The FIR DAC coefficients are also reconfigurable to meet the transmit mask requirements of each channel bandwidth. Finally, quadrature modulation is performed in analog domain at the desired carrier frequency.

The advantages of using FIR DAC are three fold. Firstly, even with long filters and high resolution coefficients, the embedded FIR filter can be designed to fulfill the desired mask, EVM, and out-of-band noise floor requirements. This is the difference between RF DAC approaches where a missing reconstruction filter results in using LC bandpass filter to attentuate images and generally high OSR. Secondly, the FIR DAC coefficients can be reconfigured to realize a different impulse response with the same number of elements used representing the coefficient set of the first filter. Although using long

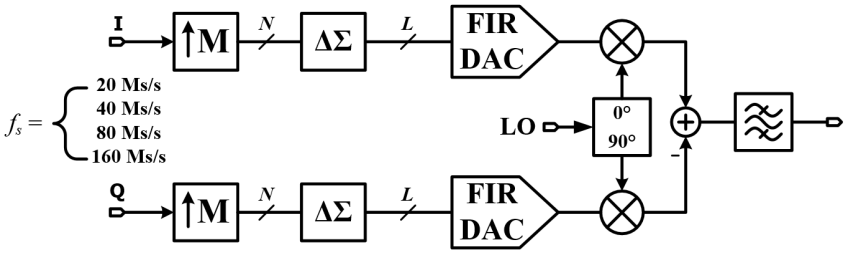


Figure 3.14: Block diagram direct conversion transmitter architecture for IEEE 802.11ac based on LPF FIR DAC

filter with high resolution coefficients for a standard that can be implemented with a simpler filter and coefficient resolution is not efficient, reconfigurability in similar channel bandwidths can be carried out efficiently. Thirdly, the 1-bit FIR DAC, for $L = 1$, is inherently linear, and coefficient mismatch errors only result in changes in the stopband rejection of the filter.

However, the limitation of this architecture also emanates from the FIR DAC. To achieve high stopband rejection, - 40 dBr for 802.11ac transmit masks at $\frac{3f_{CH-BW}}{2}$, the filter tends to be long and the coefficients have high resolution. This could result in big area which, in turn, can increase the clock timing errors, and decrease the maximum achievable SFDR.

The quadrature mixers in Figure 3.14 can be implemented in analog. The passive voltage upconversion mixers discussed in [HSR10] can also be used for SAW-less implementation so that the output can directly drive a power amplifier.

BPF in digital-IF Direct Conversion Transmitter

A BPF FIR DAC in a direct conversion architecture is shown in Figure 3.15. To generate a bandpass input signal to the FIR DAC, the output of the delta-sigma modulator is fed to a digital complex mixer with complex output. The output is at $\frac{nf_s}{2}$ for band pass or high pass operation of the FIR DAC. The final mixing is carried using 90^0 phase shifted clocks of the two FIR DACs.

Image suppression in this architecture is achieved by the 90^0 shifted clocks, i.e., at the summed output. The effectiveness of this is left for investigation.

The summed signal at the output of the FIR DACs can reach up to $\frac{f_s}{2}$. A HPF mode achieves higher carrier frequency than the BPF implementation.

BPF/HPF in Digital-IF Transmitter

A BPF/HPF FIR DAC based digital-IF transmitter architecture is shown in Figure 3.16. In this case, the quadrature modulation is carried out digitally. The delta-sigma modulator and the FIR DAC are operating

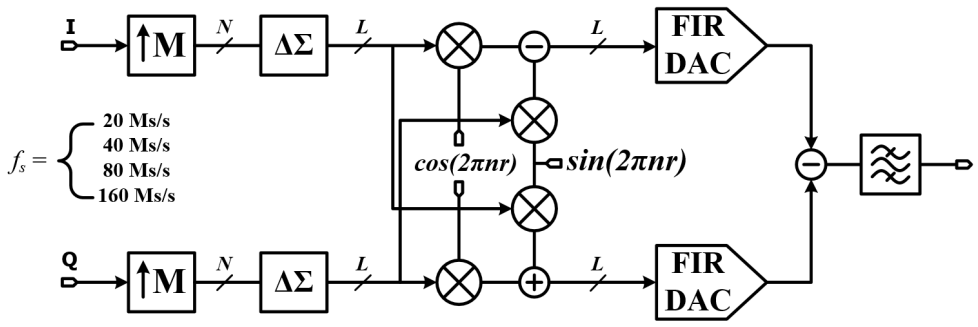


Figure 3.15: Block diagram direct conversion transmitter architecture with upconverted ΔΣ input to a BPF FIR DAC. r is ratio of f_{IF} to f_{CLK}.

in the same mode as high pass, or band pass. This architecture has similarity to what is implemented in [Tal+08] except the mixing DAC is replaced with a reconfigurable FIR DAC. Low voltage RF DAC implementation suffers from limited output impedance of current sources more than traditional DACs. This is because high output impedance cascode current sources can be used when there is no additional switching devices overhead for LO. Hence, an architecture with high stopband rejection FIR DAC is more suitable to low voltage operation than RF DACs. Since it does not have LO caused linearity problems, it can deliver better high frequency performance.

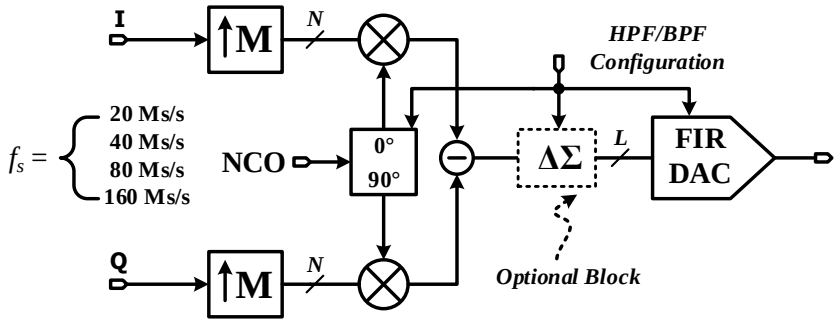


Figure 3.16: Block diagram of digital-IF transmitter architecture based on ΔΣ BPF/HPF FIR DAC

This architecture can be easily reconfigured for operation at different sections of the first Nyquist zone. It can be reconfigured such that the NCO and delta-sigma modulator and FIR DAC can be programmed for the different IF frequencies. For example, the NCO has to generate { 1,0,-1,0 } for IF of $\frac{f_s}{4}$, then the ΔΣ has to change configuration for band pass noise shaping, and the FIR DAC has also to be reconfigured for band pass filtering with only changes in the delay line as will be explained in Chapter 4. If a different IF is desired, say $\frac{f_s}{3}$, then the NCO has to generate {1,-0.5,0.5 and 0, $\frac{\sqrt{3}}{2}$, -$\frac{\sqrt{3}}{2}$}, and the ΔΣ and FIR DAC can be reconfigured as easily [Van+03].

The FIR DAC in this architecture has to work at higher clock rate and input frequency. It is possible to

use another mixer following the FIR DAC if the desired carrier frequency is too high to be implemented with reasonable performance in the FIR DAC. Additionally, to decrease the effect of the SINC roll-off on the FIR DAC response, the NRZ holding has to be replaced with a RZ-type pulse holding [CKR08].

3.4 Summary and Conclusions

The chapter introduces basic transmitter operation. It discusses modulation in SC and OFDM transmitters, and briefly summarizes the pros and cons of traditional Cartesian transmitter architectures and polar transmitters. It also highlights some important performance metrics for transmitters.

All-digital transmitter architectures from recent literature are thoroughly reviewed. A special attention is given to digital-to-RF converters. A summary table of the discussed works is also included.

In accordance with the target application of this work, multi-standard transmitters are reviewed. More importantly, novel multi-standard transmitters architectures based on LP, BP, and HP FIR DACs are also proposed. The FIR DAC concept is discussed in Chapter 4.

Chapter 4

Configurable Finite Impulse Response Digital-to-Analog Converter

4.1 Operation of a DAC

A digital-to-analog converter is used for converting digital signals into analog signals. In wireless communication transmitters, it is usually followed by an analog reconstruction filter to smooth the staircase signal into pure analog form. Digital processing blocks can be used to change the resolution of the signal before it is fed to the converter.

In this section we are going to introduce time and frequency domain operation of an ideal DAC in a classical wireless transmitter. It will be followed by a discussion of a semi-digital FIR DAC. To help explain the FIR DAC, a brief highlight of traditional multi-bit DAC specifications and architectures are included.

4.1.1 Traditional Multi-bit DAC

The operation of a DAC in time domain is shown in Figure 4.1. An L-bit digital word is the input to an L-bit resolution DAC. The DAC reads the input data at instance nT_s and holds the new output until $(n+1)T_s$ for a clock period, T_s, in what is called an NRZ scheme. The DAC could also read the sample and hold the output for half the period of the clock and return the output to zero for the remaining half in an RZ scheme. In time domain, the response of the DAC can be approximated by a rectangular pulse with a width of T_s.

The rectangular pulse in time domain is a SINC function in frequency domain. The duty cycle of the RZ DAC in time sets the zero-crossings in frequency as shown in Figure 4.2. While the RZ has a flatter magnitude response in the first Nyquist zone, the NRZ is more selective. For input signals whose bandwidth stretches to near $\frac{f_s}{2}$, using RZ response ensures a smaller ripple across the desired band. Given a sampled input as shown in Figure 4.1, the NRZ response can attenuate the immediate image signal by more than 10 dB. However, the attenuation provided by the DAC response is for most applications not

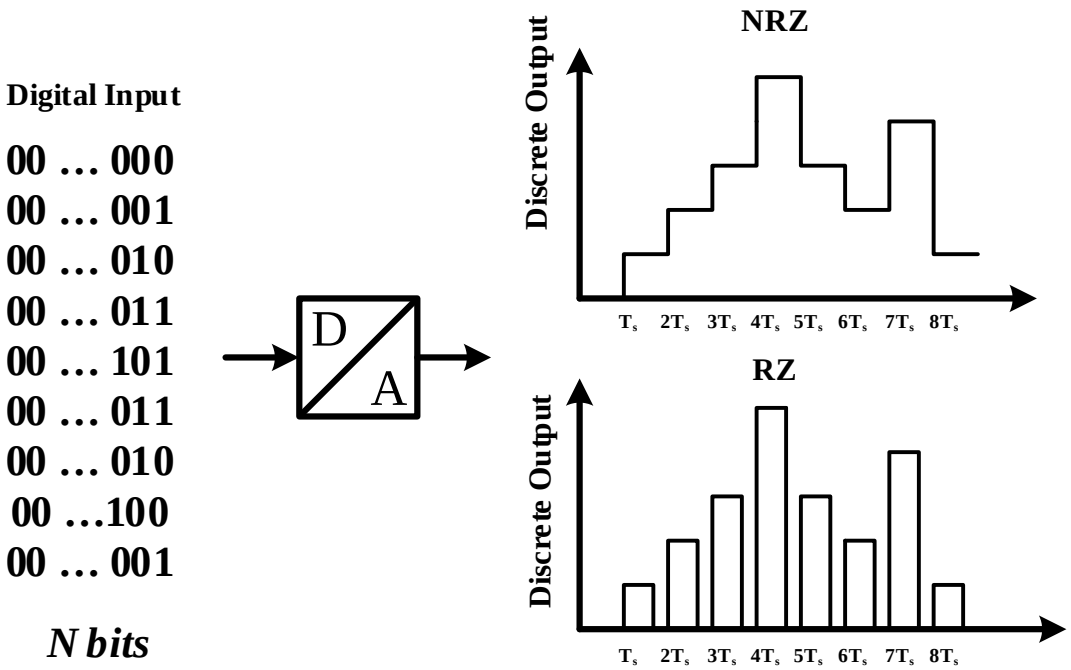


Figure 4.1: Time domain operation of a DAC

enough. Hence, an analog reconstruction low pass filter could do most of the job of filtering out the image.

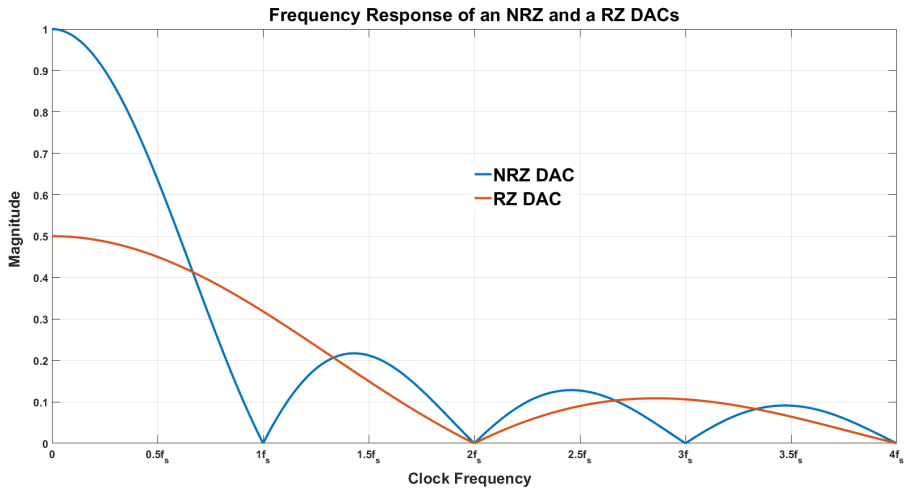


Figure 4.2: Frequency domain operation of a DAC

4.1.2 Multi-bit DAC Specification

The performance of a DAC is commonly specified as static performance, dynamic performance and frequency domain performance. In this sub-section, the main DAC performances metrics are defined,

and some formulas are derived in some cases to clarify the concepts. A graphically summary is shown in Figure 4.3.

Resolution

Normally, an N-bit input signal is converted to analog by using a N-bit resolution DAC. However, that is not always the case as $\Delta\Sigma$ modulators can be used to ease design complexity and lower input signal resolution so that an originally N-bit signal can be converted to analog by using a lower resolution DAC at higher speed.

Output Signal Bandwidth

In wireless communication, a Nyquist rate DAC is designed to convert input signal bandwidths up to half its update rate. The problem with such a target is that the reconstruction filter that follows the DAC becomes complex as it has to filter out a nearby image when the desired signal is close to $\frac{f_s}{2}$.

Nonlinearity

Nonlinearity of a DAC are measured by the INL and DNL. DNL is defined as the maximum difference between the LSB and the measured difference of two consecutive output values. On the other hand, INL is a measure of the total deviation of the time-domain response of the DAC from the ideal response.

Settling Time

At each update time, the output may change to a new value, and the time it takes to reach within some range of the value is the settling time. The range of values are usually defined as the percentage of the final theoretical value and they are called percentage tolerance.

Clock Feedthrough

This is a manifestation of the clock in the output spectrum. This happens due to parasitic capacitances which link the input side, usually digital, to the analog output. It is easily noticeable in the output spectrum because it appears at the clock frequency and its harmonics.

Spurious Free Dynamic Range

SFDR measures the relative power difference between the desired signal and the highest harmonic or spur at the DAC output. This measurement is carried out using a single tone input signal as shown in Figure 4.2.

Harmonic Distortion

HD_n measures the ratio of the power of the n^{th} harmonic to the power of the fundamental signal. The total harmonics distortion is the ratio of the power of the fundamental to the total power of all the harmonics.

The Third-Order Intermodulation Product

IMD3 is a measure of the ratio of power of the third order intermodulation product to the power of the fundamental input signals. If the two input single tones are f_1 and f_2, the third-order intermodulation product is one of $2f_1 \pm f_2$, or $2f_2 \pm f_1$ which falls in the signal band.

Dynamic Range

DR measures the difference between the maximum output power, also called the full-scale output, and the minimum output power. The minimum output power can be approximated by the total noise at the output. The noise may include the quantization error, thermal noise, and flicker noise depending on the application and their influence on the circuit.

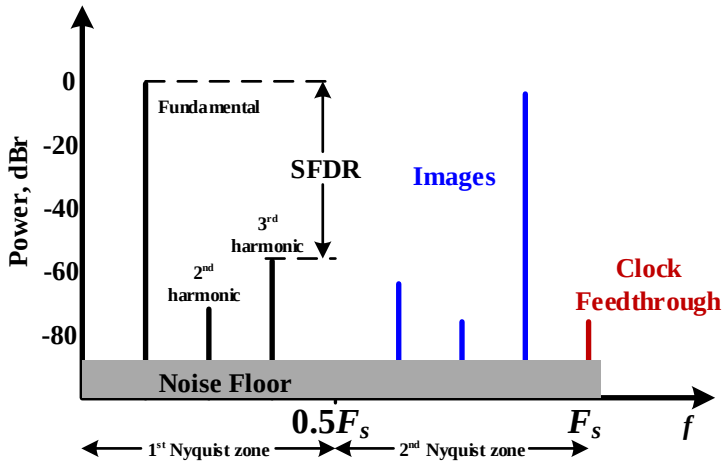


Figure 4.3: Metrics of the dynamic performance of a DAC

4.2 Traditional DAC Topologies

DAC can be implemented mainly in three modes: voltage, current and charge. We present in the following sections some classical DAC architectures.

4.2.1 R-2R Ladder DAC

The most straightforward method of implementation is based on switching binary weighted values depending on the N-bit digital input to the output. The values can be realized using voltage/current division in voltage/current mode implementation respectively or charge-redistribution. If we take the R-2R ladder network as an example, Figure 4.4, a reference voltage is divided according binary-weighted resistance ladder, and the digital inputs bits are used to switch the corresponding weighted resistor to a common node or ground. Usually an op-amp is used for summation [Bak10].

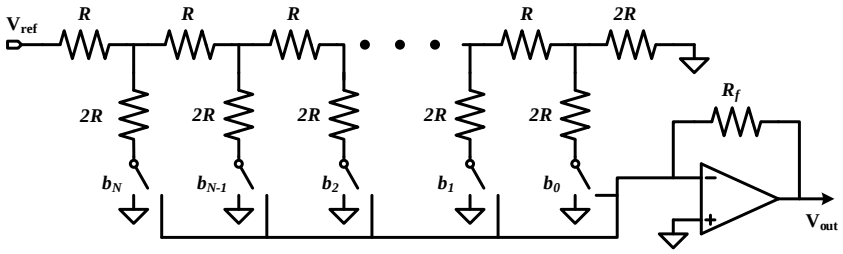


Figure 4.4: A $N-bit$ R-2R resistance ladder DAC

4.2.2 Resistor String DAC

This is a more bulkier type of implementation because it has all the possible analog values of an N-bit digital input. The digital inputs are used to decode which value to send to the output. In resistor string implementation, a reference voltage is divided using identical resistors such that all the analog values can be tapped to the output depending on the digital input as shown in Figure 4.5. The decoding could be done as shown in the figure, with a switch array or even with a row/column matrix to lower the required number of components or to improve dynamic performance.

4.2.3 Current Steering DAC

This is the type of implementation more suitable for high speed, high resolution DAC implementation. In the case of thermometric implementation, Figure 4.6, the output is obtained from summation of identical valued current sources. The digital inputs control an identical number of current source proportional to their values. Since there is an LSB (I_{unit}) difference between consecutive output values, the transition is smooth and the glitch energy associated with it is low. Mismatch could also be reduced due to the identical nature of the current cells.

The thermometric current steering approach requires a large number of unit current cells for high resolution DACs. The routing requirement limits the achievable speed. To remedy this, a segmented

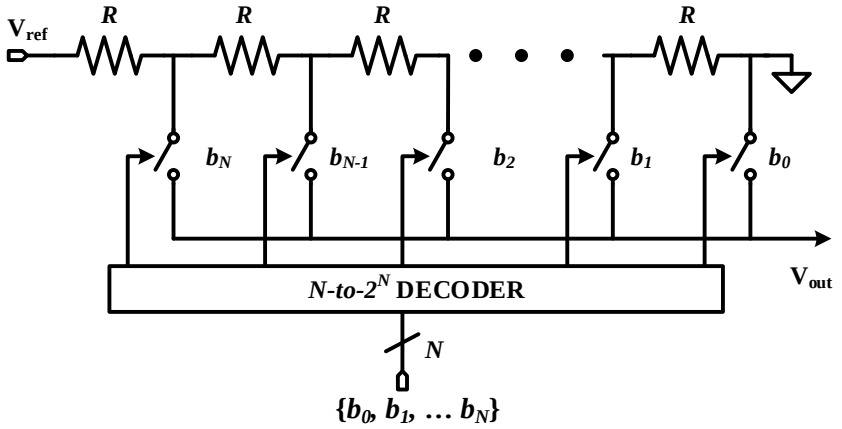


Figure 4.5: A $N-bit$ resistor string DAC

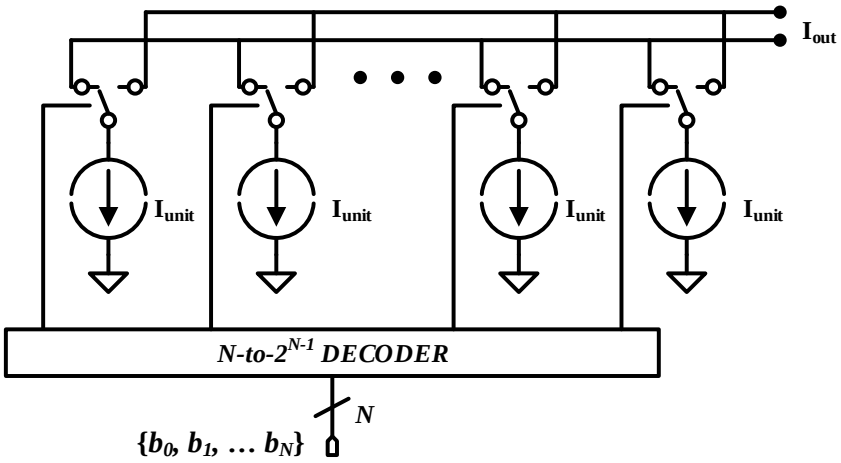


Figure 4.6: A thermometric current steering DAC

architecture could be implemented where the some of the binary digital inputs can be implemented in binary weights, and the MSB bits in unary thermometric weights. A current steering segmented DAC implementation is shown in Figure 4.7.

4.3 Finite Impulse Response DAC

A general L-bit, N-tap FIR DAC architecture is shown in Figure 4.8. C_1 to C_N are the filter coefficients which are implemented by using an L-bit DAC. N is the length of the filter.

A FIR DAC can be viewed as a digital filter whose coefficients are implemented in analog. It can be used as a DAC because its coefficients can be designed to form any desired frequency response and shape the analog output. It can also be seen as a general structure from which the traditional multi-bit

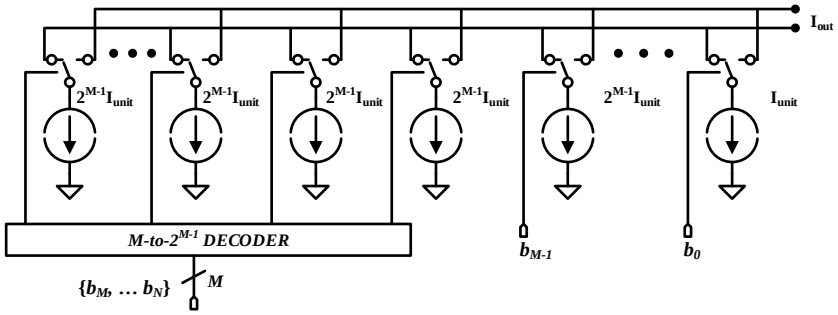


Figure 4.7: A segmented current steering DAC

DAC is derived. As it is an *L*-bit, 1-tap, power-of-two weighted coefficients version of the FIR DAC.

The main strengths of the general FIR DAC structure is the flexibility to configure the coefficients to obtain any desired frequency response. The output is a linear sum of each tap output. The other strength is the inherently linearity of the output for the case that the coefficients in the taps are linear.

Each DAC has as an input which is the delayed version of the input to the FIR DAC. Therefore, the output is a sum of the delayed and scaled versions of the input. If *L* equals one, the DACs realizing the coefficients can be replaced by a single switch device that controls a passive or active realization of a coefficient value. This arrangement leads to an *N*-tap, 1-bit FIR DAC. For the case where both *L* and *N* are greater than one, it is an *L*-bit, *N*-tap FIR DAC. The classical DAC is considered as an *L*-bit, 1-tap FIR DAC.

There are many important differences between an *L*-bit, *N*-tap; 1-bit, *N*-tap; and *L*-bit, 1-tap FIR DACs. They differ in the ease of dealing with mismatches, the maximum speed each can achieve under the same constraints, the area required to implement them and other parameters [VFM90]. In the following sub-section, the general issues common to all flavors of the FIR DAC structure are discussed. Subsequently, a quantitative comparison of the different flavors is presented. At the end, the comparisons are summarized in a table.

4.3.1 FIR DAC Implementation Issues

The delay cells are usually implemented using clocked dynamic or static or semistatic logic. They can also be implemented with analog circuits. Some power consumption reduction could be obtained using non-clocked delay cells, but the resulting delay inaccuracy could be detrimental to the performance of the filter[OT14].

To faithfully replicate the transfer function, the coefficients have to be realized with high degree of accuracy. Thermometric implementation of the coefficients gives higher accuracy. On the contrary,

weighted implementation of the coefficients is prone to mismatch errors, but could be arranged to save area.

For analog implementation, coefficients have to be quantized as their quantitative values have to be translated to hardware. In other words, accurate coefficients are difficult to realize. In addition to quantization, coefficients assume random values. It increases mismatch errors due to loss of symmetry. Furthermore, the fact that the coefficients are random means we have to look into asymmetrical layout methods to decrease systematic process mismatches during layout. Therefore, coefficient quantization helps in representing one coefficient as a ratio of another smaller one. If integer relationship is maintained for all ratios between any two coefficients, all of them can be represented as a sum of a unit coefficient.

The other source of error is the spread of the coefficients. When there is large spread, the number of required unit coefficients increases exponentially. Therefore, filter design should target low resolution coefficient set. The length of the filter is another factor that increases the number of unit coefficients. Long filter are required to achieves high stopband rejection, but results in large area and big unit coefficient count.

All these factors have to be considered during selection of a FIR DAC topology. Topologies that use passive components to implement FIR DACs can result in big areas due to the relative size of the unit passive component realizing the unit coefficient. For large bandwidth applications, the unit coefficients should be able to switch at high speeds. In this regard, current-steering architectures are preferable. Topologies that exploit the symmetry of FIR DAC impulse responses have generally lower area due to hardware sharing. Because an implementation of a coefficient would be reused to realize two same-valued coefficients in the left and right side of the impulse response. However, the circuit implementing the coefficient now has to entertain additional conditions. For example, a 1-bit input could be translated to a 0 or a 1 for a coefficient, but a 0, 2, and -2 i.e. 1.5-bit for two coefficients. These would be require a different implementation of the coefficient.

4.3.2 *L*-bit, *N*-tap FIR DAC Design Challenges

Generally, filter design is a compromise between the number of coefficients of the filter, the transition band and the passband and stopband ripples. With strict requirements on the transition band and stopband rejection for narrowband applications in crowded spectrum, a long filter length is needed. On the other hand, in broadband applications where the required stopband rejection ais low, a short filter length can achieve the required transition band.

The digital input of the FIR DAC can be oversampled to reduce quantization noise and complexity of analog low pass reconstruction filter. The oversampling process eases filtering, so short length filter with

low coefficient spread could be used. In this scenario, the *L*-bit, *N*-tap FIR DAC shares the challenges of a traditional *L*-bit DAC and would closely follow the linearity of the *L*-bit DAC.

A delta-sigma modulator is used for converting the resolution of the digital input, then the FIR DAC has low number of input bits and high number of coefficients with considerable coefficient spread to reduce quantization noise. In this scenario, the *L*-bit, *N*-tap FIR DAC has to maintain matching *N* number of *L*-bit DACs. In other words, a single *L*-bit DAC would outperform the multi-tap FIR DAC. The advantage of the *L*-bit, *N*-tap FIR DAC over the the *L*-bit DAC would be in image rejection.

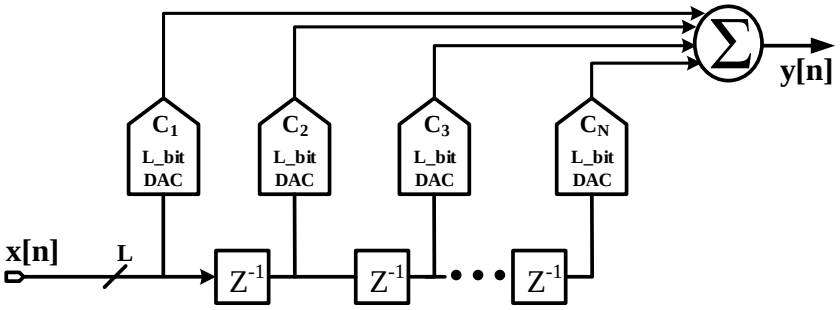


Figure 4.8: A general *L*-bit, *N*-tap FIR DAC architecture

4.3.3 *N*-tap, 1-bit FIR DAC Design Challenges

A 1-bit, N-tap FIR DAC is inherently linear. This is because the 1-bit DACs realizing the coefficients are inherently linear and the output is a sum of the delayed and scaled versions of these linear outputs.

The 1-bit, *N*-tap FIR DAC is best suited, then, for obtaining high filtering performance. However, it has to work at higher speeds compared to an *L*-bit, *N*-tap FIR DAC. This is because the serial data at the 1-bit FIR DAC input passes through a conversion stage containing an oversampling and delta-sigma modulator blocks with higher OSR.

A comparison of the three common structures of a FIR DAC is provided in Table 4.1. Some of the assumption used for comparison are shown as a footnote. The first two structures are assumed to have the same resolution in their coefficients and, also, equal number of coefficients. The third structure is the traditional multi-bit DAC. It is presented in the table as a special FIR DAC with a single-tap, or no delay cell, between its coefficients. Besides, its coefficients are implemented with only weights of two.

As expected, an *L*-bit, *N*-tap FIR DAC have the worst mismatch linearity and speed. A traditional multi-bit DAC can achieve the highest speed due to the absence of a delay line, lowest number of unit coefficients and smaller coefficient spread. A 1-bit, *N*-tap FIR DAC can achieve the same coefficient

‡ $L > 1$ § $N > 1$ ¶ Traditional multi-bit DAC ‖ Thermometric implementation assumed

Table 4.1: Comparison among the three structures of an FIR DAC

Parameters	**FIR DAC**		
	***L*-bit,** ‡ ***N*-tap**	**1-bit, *N*-tap** §	***L*-bit, 1-tap** ¶
Mismatch Linearity	– –	++	–
Speed	– –	–	++
Image Rejection	++	++	–
Coefficient Spread	– –	++	++
Number of Unit Coefficients ‖	– –	–	++

spread as a multi-bit DAC, but the number of unit coefficients usually increase as N increases. Image rejection is better in the first two structures due to the flexibility to implement a filter responses sharper than a SINC function.

4.3.4 Frequency Translation of FIR DACs

Once a low pass filter is designed, a bandpass and a high pass filter can be generated by only changing the delay line while keeping the coefficients values the same. In circuit implementation, this behavior of the FIR filter makes it amenable to reconfiguration. By only adding redundant delay cells which can be switched to be in the signal path of the active delay line or not, the filter is frequency translated. Since delay cells consume relatively low power and occupy relatively small area, the share of this frequency translation feature on the total FIR DAC power and area budget is negligible.

LPF to HPF Transformation

A linear-phase symmetrical or asymmetrical low pass FIR filter impulse response can be changed to a high pass filter response centered at $\frac{f_s}{2}$ by multiplying each coefficient by $(-1)^n$ where n is the tap to which the coefficient belongs. Mathematically, this can be expressed as [Lyo04]:

$$h_{hp}[k] = h_{lp}[k]\, S_{shift}[k] \tag{4.1}$$

$$S_{shift}[k] = \{\ldots, 1, -1, \ldots\} \tag{4.2}$$

In circuit design, this is simply implemented by changing the flip-flops of the delay line. One method in a 1-bit FIR DAC is to drive coefficients by the negative output, $\bar{Q}$ of flip-flops, every other tap. For reconfigurability, the coefficients can be switched between the positive output, Q, and negative output, $\bar{Q}$, for low pass and high pass filtering respectively.

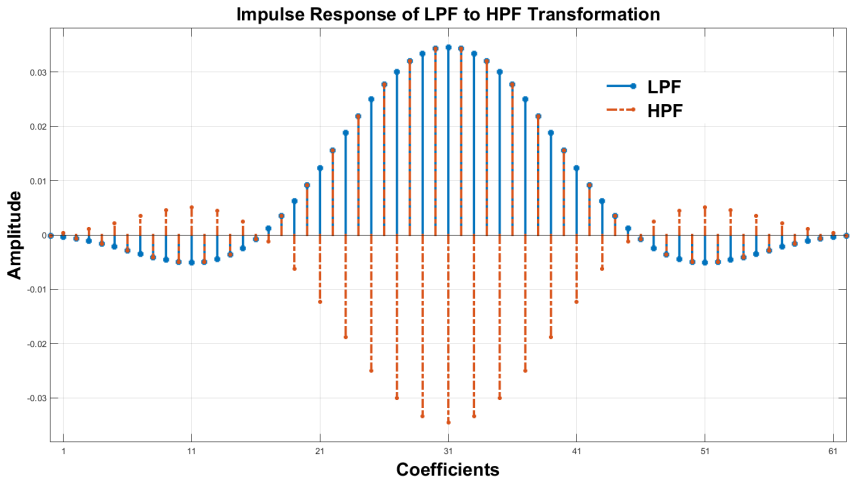


Figure 4.9: Impulse response of LPF FIR and its frequency translated HPF version

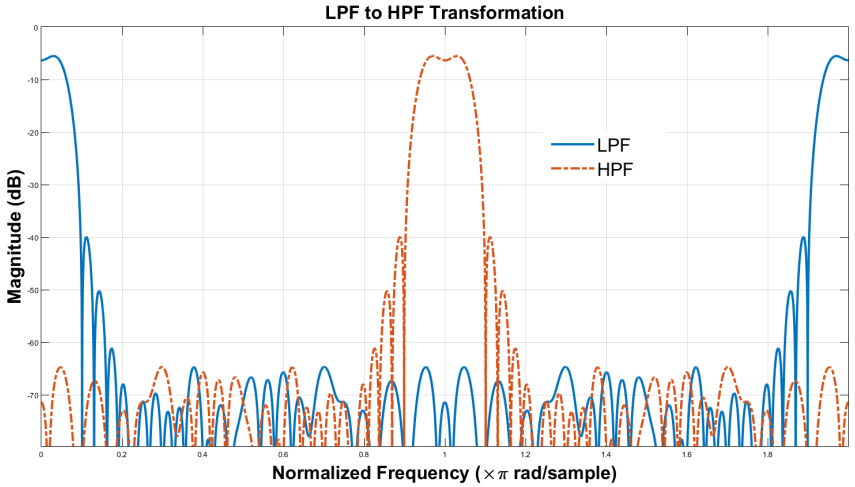


Figure 4.10: Magnitude response of LPF FIR and its frequency translated HPF version

An impulse response in Figure 4.9, which will be revisited in subsequent chapters, is used for explaining the discussed transformation. The LPF impulse response is multiplied by $(-1)^n$ to convert it to a HPF response with the same number of coefficients. The resulting frequency response can be seen in Figure 4.10 where the HPF has the same magnitude as the LPF.

LPF to BPF Transformation

A linear-phase symmetrical or asymmetrical low pass FIR filter impulse response can be frequency translated to a band pass filter centered at $\frac{f_s}{4}$ by multiplying every other coefficient by 1 and -1 and inserting additional zeros in between each multiplication. Mathematically, this can be expressed as [Lyo04]:

$$h_{bp}[k] = h_{lp}[k]\, S_{shift}[k] \tag{4.3}$$

$$S_{shift}[k] = \{\ldots, 1, 0, -1, 0, \ldots\} \tag{4.4}$$

In circuit implementation, this is easily realized by adding an untapped delay line between the taps that are switched to the positive output and negative output at every other tap. This transformation, however, comes at a cost due to the inserted zeros. For the same filter length, the magnitude response of the resulting band pass filtering FIR DAC decreases by 6 dB. Nonetheless, the good news is that the effective length of the filter is also decreasing. Thus, for a LPF FIR whose length is twice than desired can be designed and transformed to a BPF filter, and still the resulting number of non-zero coefficients will be the same.

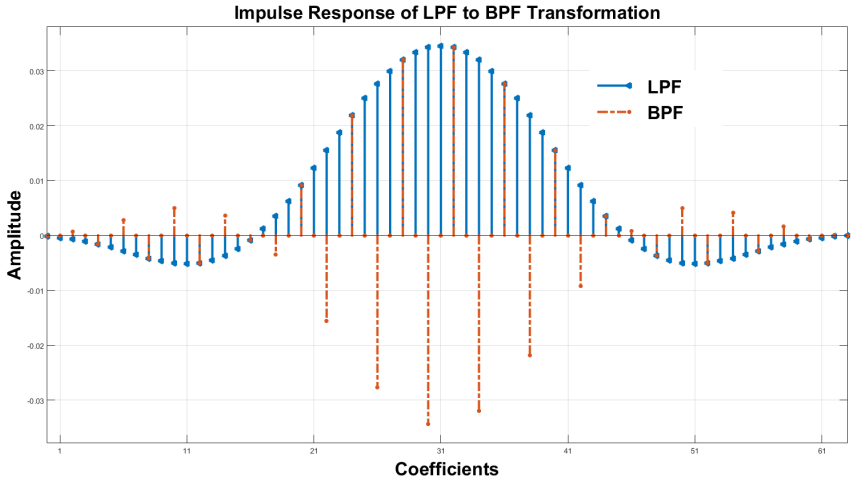


Figure 4.11: Impulse response of LPF FIR and its frequency translated BPF version

The LPF impulse response from the previous example is again transformed to a BPF response as shown in Figure 4.11. The magnitude response of the resulting band pass filter is lower by 6dB, as can be witnessed in Figure 4.12, while the number of coefficients have decreased

Configurable 1-bit FIR DAC Delay Line

The implementation of the above discussed transformation in a 1-bit FIR DAC is straightforward. By designing a reconfigurable delay line with a minimum cost of power consumption and area, a set of FIR DAC coefficients designed for LPF mode can be made to work in BPF and HPF modes also. Figure 4.13 shows the frequency translation of a 1-bit FIR DAC by only exploiting the delay line. This means, the components implementing the coefficients can remain unchanged. The advantages of this approach

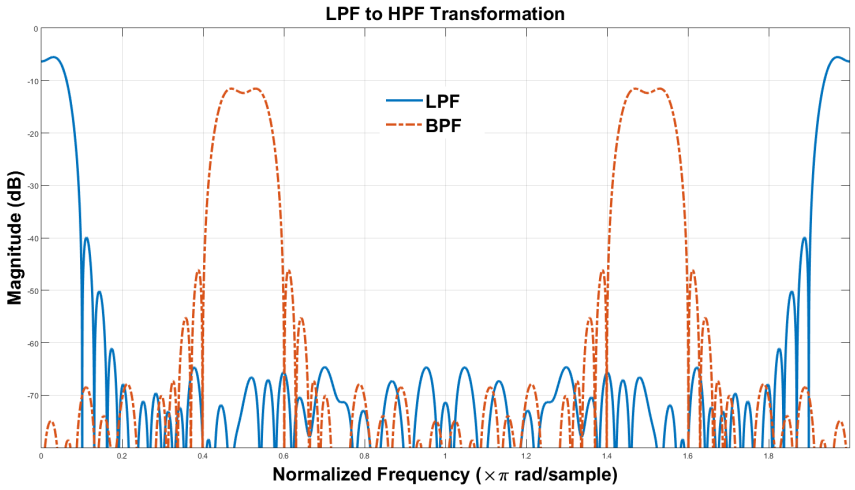


Figure 4.12: Magnitude response of LPF FIR and its frequency translated BPF version

is that the frequency behavior of the FIR DAC can be changed without modifying the placement and routing of the coefficient circuits array.

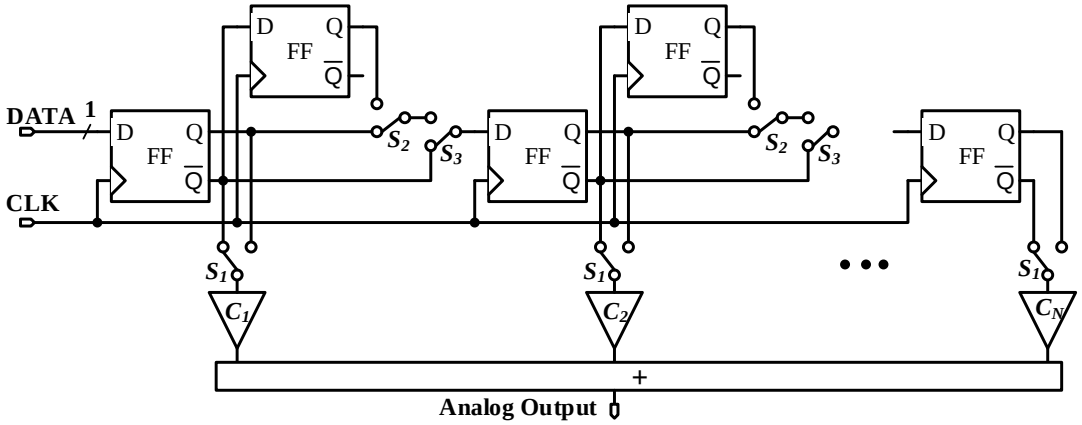


Figure 4.13: Transformation of a 1-bit FIR DAC from LPF to BPF and HPF using a configurable delay line

Assume the switches in their current state in Figure 4.13 are in state 1, and the other state is 0, then the following table could be used to obtain the transformation discussed in the previous topics.

The configurable delay line can be optimized further by fixing the position of switch S_1 to the output of the positive output of a delay cell as shown in Figure 4.14. For this delay line, the additional hardware needed is $2(N-1)$ switches and $N-1$ delay cells for a total of $2N-1$ delay cells. The power consumption and area contribution of these additional cells and switches, which are required for the configurability, is a small fraction of the total power consumption and area of the total FIR DAC.

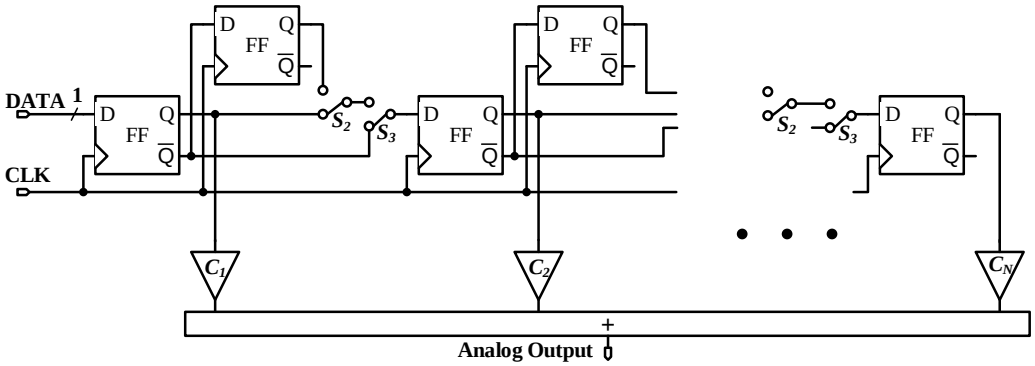


Figure 4.14: An optimized configurable delay line with only $2(N-1)$ switches and $2N-1$ delay cells.

Table 4.2: Switch states of delay line for frequency translation of the 1-bit FIR DAC

Frequency Response	**Switch,** S_1	**Switch,** S_2	**Switch,** S_3
LPF FIR DAC	0	1	0
HPF FIR DAC	X	X	1
BPF FIR DAC	X	0	0

4.4 FIR DAC Architectures in Literature

In this section, the discussion on FIR DAC topologies will continue by reviewing briefly previously published works. Initially, a discussion on reported FIR DAC architectures, their application, and specifications will be presented. The discussion focuses on FIR DAC implemented on the transmitter side. However, it is important to mention that they are also applied in the receiver side as part of the analog-to-digital converter. In [AA10], a discussion of the design of continuous time sigma-delta modulators based on FIR DACs is presented.

4.4.1 Multi-bit FIR DACs

Traditional transmitter architectures have a digital filter followed by a DAC and then a reconstruction analog low pass filter. Early works targeted reducing the complexity of the digital filters using what they called digital-analog filter converters [VFM90]. This removed power consuming, silicon area demanding, albeit flexible, multiplication blocks while combining two functionalities into one. A silicon demonstrator of this approach was fabricated in 3μm CMOS technology where the coefficients of a 4-tap FIR filter are implemented using 8-bit algorithmic DACs. The operational amplifier based swtiched-capacitor summing output generally is a speed bottleneck and could have limited the reported speed of 20 kHz.

A more recent implementation of a multi-bit dac is the 4-bit, 60-tap semidigtal filter implementation in [Lin+06]. The idea in the work of Lin et al. is to filter shaped quantization noise out of a delta-sigma modulator using a steep transition band semidigital filter. The drooping at the edge of the passband of the semidigital filter is compensated by a pre-emphasis digital filter. Since steep transition, and high stopband rejection require long filter length, the semidigital filter was designed using interpolated coefficients. The problem with this approach is that it requires a complex analog low pass filter to remove the additional passband in the middle of the semidigital filter response. A third-order low pass filter is used in their work due to the high oversampling ratio, 88, in their frequency planning. For lower OSR values, a higher order analog LP filter would have been used. In other words, effective bandwidth of output signal is exchanged for complexity of analog filter.

4.4.2 1-bit Semi-digital Reconstruction Filter

The potential of an $N-tap$, 1-bit FIR DAC to lower the complexity of the analog reconstruction filter that follows a DAC in a classical transmitter architecture is demonstrated in 1.2μm CMOS technology in [SW93]. The implementation is shown in Figure 4.15. A 128-tap current-mode FIR DAC, clocked at 7.76 MHz, is used to remove shaped quantization noise at the output of a $\Delta\Sigma$ modulator. Such a long filter implementation normally has a big area and systematic mismatch errors are a big concern.

A method to reduce the number of filter coefficients based on interpolation was reported in [Kim+98]. A sharper transition band filter is obtained from a filter with twice large passband by upsampling its coefficient set. In other words, delays are inserted, i.e. zero values, between coefficients of an impulse response of a filter normally designed for a twice large passband than is desired. This method results in an unwanted additional passband at $\frac{f_s}{2}$. To circumvent this problem, an interpolated low pass $\Delta\Sigma$ modulator that generates an additional low noise region at $\frac{f_s}{2}$ is used.

The high linearity performance of $N-tap$, 1-bit semi-digital FIR is employed in the signal path of a dual-truncation $\Delta\Sigma$ DAC. In this switched-capacitor 0.18 μm CMOS implementation, the symmetry of a 67-tap FIR impulse response is exploited using a folded delay chain to reduce the number of capacitors by half [FFQ04]. While the method of employing complementary clocks to reuse a coefficient decreases the area required, it normally limits high speed operation due to delay in the decoding logic.

In a similar application to the work in [FFQ04], a 1-bit semi-digital FIR is employed together with a digital filter to suppress shaped quantization noise in [Bar+04].

In [Doo+05], a semi-digital 322-tap FIR DAC with only positive coefficients is designed for quantization noise filtering at audio frequencies. Silicon area limits the use of high resolution coefficients in long filter implementation. This problem is overcame in [Doo+05] by limiting the coefficient spread to

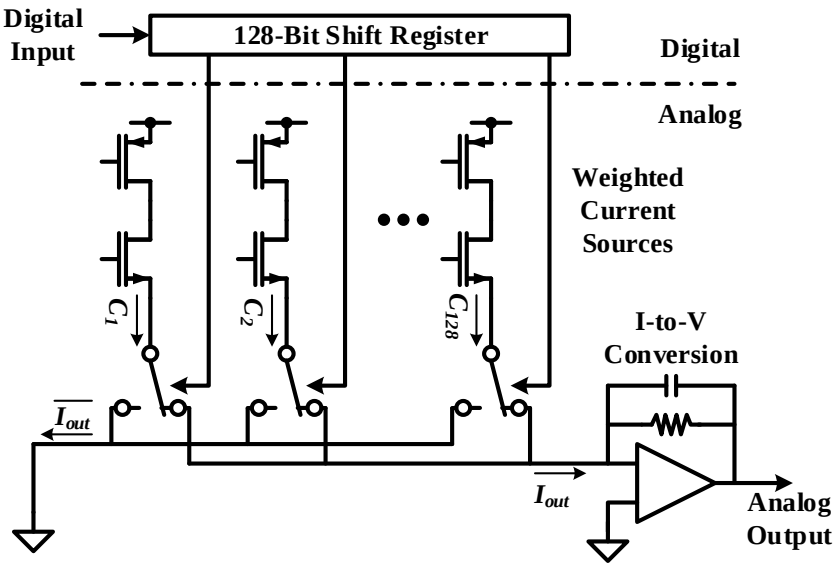


Figure 4.15: Current-mode FIR DAC architecture in [SW93]

25 and selecting only positive coefficients to improve the mismatch. In implementation, a transmission gate based dynamic delay line was used to save power consumption and area needed for 322 flip-flops. Normally, dynamic circuit implementations have problems of charge injection, and charge sharing. For a robust FIR DAC design at high speeds, a static or semi-static delay line is more robust against noise at the expense of increase in the total power and area by a small percentage.

4.4.3 Programmable Filtering DAC

The compatability of the FIR DACs approach for implementing programmable filtering DACs was demonstrated at a bigger area and power cost in [HF94]. The delay line of the FIR DAC was improved by adding redundant delays which were useful for realizing different filter responses. Each tap of the FIR DAC were implemented by segmented 8-bit current steering DACs. The programmability of coefficients was possible by changing the overdrive voltage of current sources in the segmented DAC. Current steering implementation enabled them to switch at higher rates than previously reported.

Programmability of FIR DACs was revisited using a novel current steering architecture in [AR01]. A constant bias current was divided into two positive and negative output branches using a set of differential switches as shown in Figure 4.16. The number of differential switches at each tap are proportional to the coefficient values and are enabled or disabled by a control switch that ensures programmability. A wide swing cascode current source mirrors the currents in the output branches. The frequency domain performance of the architecture depends on the high frequency linearity of the current mirrors at the output. This concept was demonstrated for a 64-tap FIR DAC with limited coefficient spread for audio

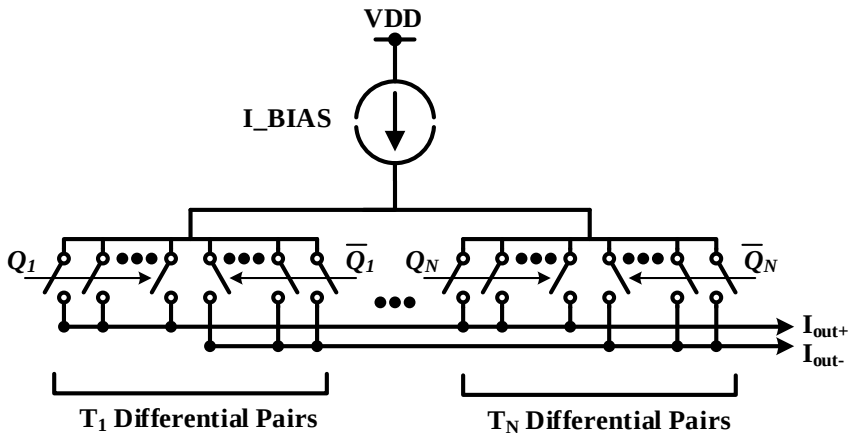


Figure 4.16: Current steering FIR DAC architecture in [AR01]

applications in 0.25μm CMOS technology.

4.4.4 Receive-band Noise Filter

The $N-tap$, $L-bit$ FIR structure is also embedded in DIDIMO transmitters for receive-band noise filtering. In [Fuk+12], a 3 + 7 segmented DAC realizes the coefficients of 3-tap FIR filter. Due to the large circuitry at each tap of the filter, the length of the filter is usually short. The coefficients are also equal to avoid mismatch problems. The only flexibility in generating different impulse responses is obtained by controlling the number of delays between the taps. This technique makes the FIR filter in DIDIMO transmitters suitable as a notch-filter to target a specific receive band. The digital signals are directly fed to the filtering structure without major filtering previous stages. Hence, high oversampling ratios are used and high resolution RF-DAC are implemented in each tap of the filer [Gab+11].

4.4.5 FIR Power DAC

Delta-sigma noise shaped digital outputs can be directly frequency translated by using image-reject digital mixers [Fra+09]. The resulting single-bit stream can be directly fed to parallel power DACs for amplification and digital-to-analog conversion. The power DACs, tapered buffers, can also form the coefficients of an FIR filter for bandpass filtering of their combined output.

In [Fla+08], a 5-tap reconfigurable bandpass FIR filter with unity positive and negative coefficients is implemented in 65nm CMOS process. The outputs of 56 TPSC dynamic flip-flops of the delay line are connected to three multiplexer. The multiplexers select five taps to drive five power DACs as shown in Figure 4.17. The outputs of the PDACs were, then, combined to realize three different bandpass filters.

Unity coefficient, short length filters may reduce the quantization noise to even fulfill transmit mask

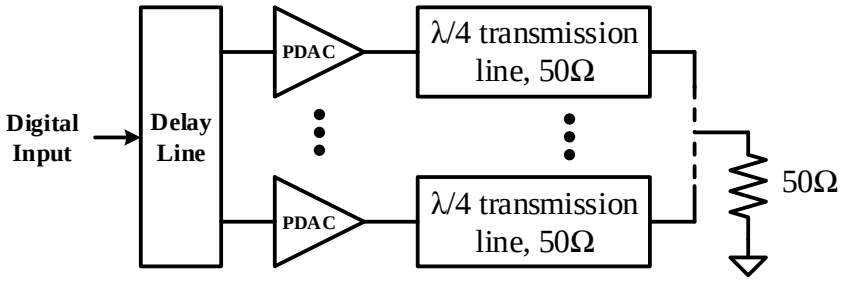


Figure 4.17: General structure of the reconfigurable bandpass FIR power DAC architecture in [Fla+08]

requirements. However, the architecture is not fit for applications where the out-of-band noise profile of the transmitter is expected to respect co-existence issues in a crowded spectrum.

4.5 High Speed 1-bit, N-tap FIR DAC Design

Unlike passive components, current mode DAC architectures are amenable for high speed operation. Their mismatch is characterized, they occupy lower area and are scalable. In this analysis, current steering FIR DAC architectures are assumed.

The analysis presented in this section are important contributions of this PhD work. As explained in the conclusions chapter at the end of this dissertation, a scarcity of literature providing design formulas for estimating non-idealities of high speed current-steering thermometric FIR DAC implementations was the reason that led to these derivations.

4.5.1 Current Steering Architecture

Current mode implementation of a FIR DAC is shown in Figure 4.18. The current sources are weighted to implement the coefficients. The differential output enables implementing signed coefficients. For example, the cross-connected outputs of the first and last coefficients realize a negative coefficient values relative to the other coefficients in Figure 4.18.

A UCC is a circuit realization of a unit coefficient. It contains analog current source and a digital latch. It can be replicated in all coefficients as many times as the quantized coefficient values to create a resultant current in the desired sign and magnitude of the coefficient as in Figure 4.18. All that is required is to maintain an integer ratio between all the coefficients. This can be accomplished by quantizing the coefficients in a fixed number of bits where the largest coefficient represents $2^{quantization\_bits}$. Then the GCD of the integer values of the coefficients becomes the value of the unit coefficient that is realized by one UCC. If there is no GCD greater than one, the unit coefficient becomes one, still realized by one

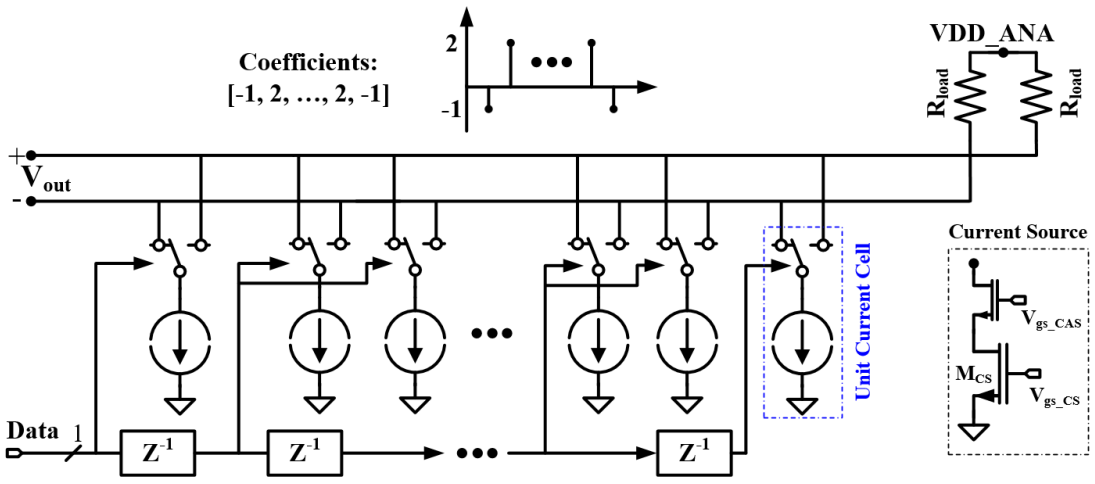


Figure 4.18: Current-steering structure for implementing a FIR DAC

UCC, and the largest coefficients requires $2^{quantization\_bits}$ UCCs in implementation.

4.5.2 Performance Metrics and Modeling

In a current steering DAC architecture, the main sources of non-idealities are current source mismatch, finite output impedance of current sources, clock feedthrough, global and local timing errors, output and cell dependent errors. Modeling these non-idealities and factoring them in the design of the DAC is important for the measurement to match the theory. In this section, we are going to analyze how these non-idealities influence the performance metrics discussed earlier in this chapter.

Effect of Coefficient Mismatch

The main advantage of a single-bit FIR DAC is the inherent linearity of the 1-bit DACs it uses at each tap. Coefficient mismatch has negligible effect on the passband of the transfer function, but it puts a limit on the stopband attenuation to a degree that even an increase in the length of the filter would not affect it. An FIR filter output is given by the following equation:

$$y[n] = \sum_{k=1}^{N} c_k x[n-k-1] \tag{4.5}$$

Where c_k are the coefficients and N is the length of the filter. The filter transfer function for a general input $x[n] = e^{-j\omega n}$, where $-\infty < n < \infty$, is [PS08]:

$$H(\omega) = \sum_{k=0}^{N-1} c_{k+1} e^{j\omega k} \tag{4.6}$$

If each c_k has a mismatch generated error ϵ_k, then the error transfer function can be written as:

$$H_e(\omega) = \sum_{k=0}^{N-1} \epsilon_{k+1} e^{j\omega k} \tag{4.7}$$

The filter magnitude response variation due to error is derived in [PM91] with the assumption that ϵ_k are uncorrelated Gaussian random variables which are identically distributed with zero mean and standard deviation σ_ϵ:

$$|H_e(\omega)| = \frac{\sqrt{\pi N}}{2}\sigma_\epsilon \tag{4.8}$$

While this equation is important in the characterization of FIR DAC coefficient mismatch errors, it is derived based on the coefficient being implemented as a lumped component. It fails to take into account that coefficients are implemented by replicating a single unit coefficient. A standard deviation which is representative of the errors of all the coefficients should be taken. A slight modification can be applied for the current steering implementation based on unit coefficient. If all the unit coefficients have errors that are uncorrelated Gaussian random variables which are identically distributed with zero mean and a standard deviation of σ_u, then a coefficient with a c_k unit coefficients has a standard deviation of $\sigma_u\sqrt{|c_k|}$. An average standard deviation of all the coefficients which are implemented with unit coefficients can be found from the pooled variance as:

$$\sigma_{ave} = \sqrt{\frac{\sigma_u^2|c_1|+\sigma_u^2|c_1|+...+\sigma_u^2|c_N|}{N}} \tag{4.9}$$

The error on the magnitude response can then be modified to

$$|H_e(\omega)| = \frac{\sqrt{\pi N}}{2}\sigma_{ave} \tag{4.10}$$

A new formula for estimation of magnitude variation due to coefficient mismatch and more suitable to a current-steering FIR DAC architecture can then be found using:

$$|H_e(\omega)| = \frac{\sqrt{\pi\sum_{k=1}^{N}|c_k|}}{2}\sigma_u \tag{4.11}$$

To put this in perspective, an impulse response of an 802.11ad FIR DAC is used in Figure 4.19. The mismatch error magnitude for a 14% standard deviation on each unit coefficient can be estimated using Equation (4.11) to be 0.0143. In other words, the passband can vary from 0.9857 to 1.0143(i.e. -0.1251 to 0.1233 in dB). The passband ripple, A_p, is then 0.2484 dB. The stopband, now at < -33 dB or < 0.02239, is raised by this error to 0.03669 or -28.71 dB. The stopband ripple, A_{st}, is then 4.29 dB. Then, it can be concluded that the mismatch error affects the stopband more than the passband. The stopband can be affected by the mismatch error to a degree where even longer filter would not deliver better stopband attenuation.

As will be seen in 4.5.2, this estimate gives an optimistic value. A more accurate ripple due to coefficient mismatch is obtained using large number simulation such as Monte Carlo.

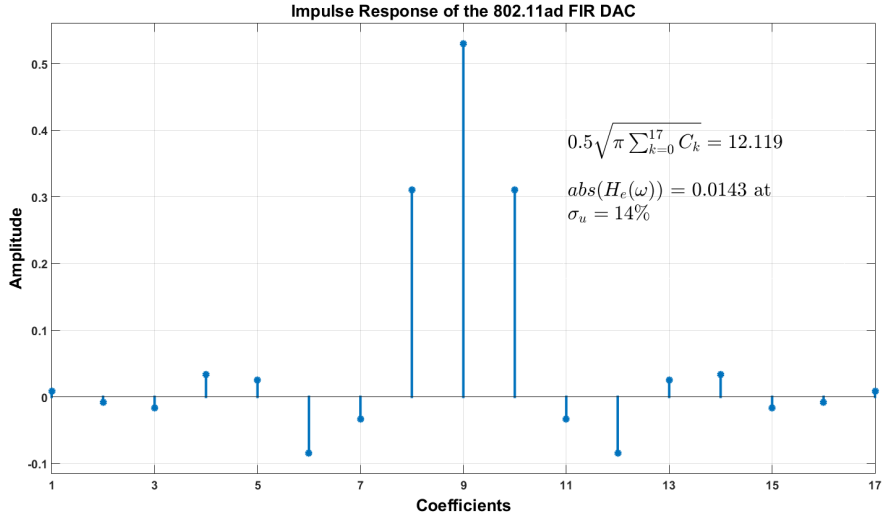


Figure 4.19: Impulse response of the 802.11ad FIR DAC. The values from Equation (4.11)

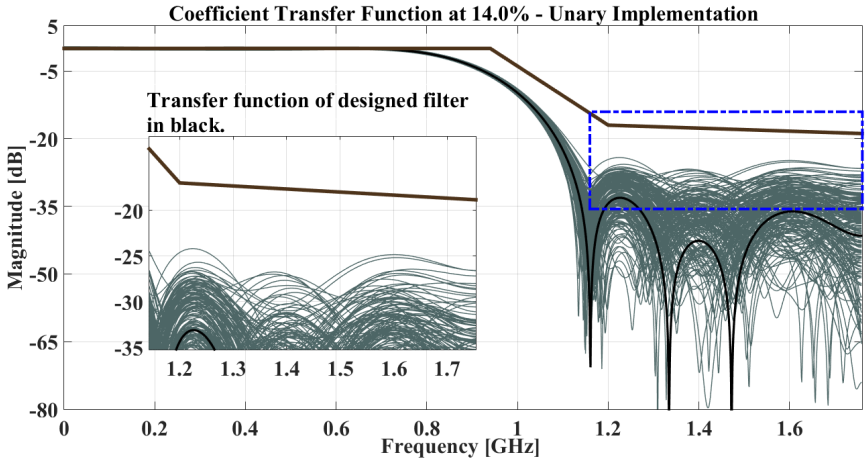
Yield Model

This parameter can be further utilized in defining a yield of a FIR DAC. A FIR DAC functionality is dependent on faithfully rendering the theoretically designed transfer function, the yield is defined as the number of FIR DACs that have an acceptable transfer function. Coefficient inaccuracy results in changes in the stopband rejection, then the transfer functions that crosses a certain limit in the stopband can be rejected.

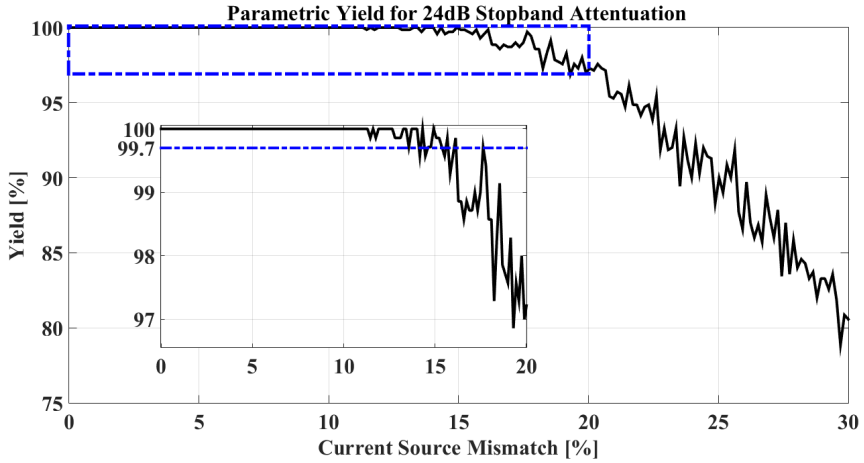
A transfer function with stopband rejection of δ_2 can be guaranteed to be below a desired stopband rejection level of $\hat{\delta}_2$ at a maximum standard deviation $\sigma_{ave,max}$ of with a probability of p given by [PM91]:

$$p = \mathrm{e}^{-\frac{1}{N}\left(\frac{\hat{\delta}_2 - \delta_2}{\sigma_{ave,max}}\right)^2} \tag{4.12}$$

This approach was used in the design of an LP SC mode 802.11ad FIR DAC as reported in [GFK15]. The percentage of the FIR DAC transfer functions that fulfill the 802.11ad mask with a margin are plotted against the standard deviation of the random mismatch in the current sources implementing the coefficients. It was concluded that the stopband of the transfer function does not raise to above 5 dB of the lowest part of the transmit mask with as big as 14% random mismatch standard deviation at a confidence level of 3σ. This is shown in Figures 4.20a and 4.20b.



(a)



(b)

Figure 4.20: The change in passband ripple is small as predicted. The transfer function can withstand coefficient mismatches up to 14%, and still fulfill the stopband attenuation with at least 5 dB margin. The percentage yield is plotted against random coefficient mismatch of unary current sources with coefficients realized as a sum of independent unary current sources.

Random Device Mismatches

Transistors which implement the coefficients are prone to process mismatches. These mismatches can be tackled by classifying them into two: random and systematic mismatches. The random mismatches are dependent on device size, biasing conditions and some technological constants whereas the systematic mismatches appear over the chip area and impart a relativistic error on a device as a function of its distance from the center of the chip (more discussion on this in Chapter 6).

In [Pel+89], a relationship between the device size and biasing and the standard deviation of the normalized random errors of a current flow through the device are observed.

$$\delta^2\left(\frac{\Delta I_u}{I_u}\right) = \frac{1}{Area}\left(A_\beta + \frac{4A_{VT}}{V_{OV}^2}\right) \tag{4.13}$$

Where $Area = WL$ of the current source transistor, V_{OV} is the overdrive voltage, and A_β, and A_{VT} are technological constants.

$$\delta\left(\Delta I_u\right) = I_u \sqrt{\frac{1}{Area}\left(A_\beta + \frac{4A_{VT}}{V_{OV}^2}\right)} \tag{4.14}$$

Equation (4.14) can be inserted in Equation (4.9) to find the maximum σ_{ave} from transistor level parameters. The σ_{ave} can be used to calculate the probability until an acceptable confidence level is obtained.

Effect of Finite Output Impedance

The effect of finite output impedance on the dynamic behavior of the FIR DAC can be analyzed by considering the unary implementation in Figure 4.18.

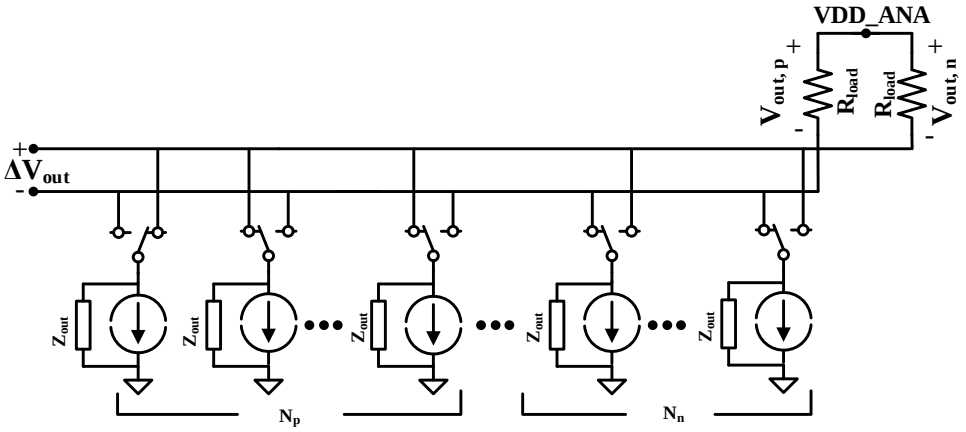


Figure 4.21

The current sources that implement the coefficients have a finite output impedance. The effect of this on the output voltage of a current-steering DAC is analyzed in [Mik+86]. Similar approach can be followed for a current-mode FIR DAC modeled as shown in Figure 4.21. N_p, and N_n indicate the total number of current sources that correspond to the coefficients contributing to the positive and negative branches of the output line respectively. Since differential implementation is considered, the negative coefficients which are driven by a 0-bit are grouped under N_p; and the positive coefficients driven by a 0-bit are grouped under N_n as the negative coefficients driven by a 1-bit.

$$I_{load,p} = N_p(I_{out} - G_{out}V_{out,p}) \tag{4.15}$$

$$I_{load,n} = N_n(I_{out} - G_{out}V_{out,n}) \tag{4.16}$$

Where $I_{load,p}$, $I_{load,n}$ are the output currents belonging to positive and negative coefficients respectively; G_{out} is the output resistance of a unit current source; and I_{out} is the ideal full scale current divided by the number of current sources. The output voltages of the positive and negative coefficients $V_{out,p}$, $V_{out,n}$ are given as:

$$V_{out,p} = R_{load}I_{load,p} \tag{4.17}$$

$$V_{out,n} = R_{load}I_{load,n} \tag{4.18}$$

The above pair of equations can be combined with equations (4.17) and (4.18) to arrive at:

$$V_{out,p} = I_{out}\left(\frac{N_pR_{load}}{1+N_pR_{load}G_{out}}\right) \tag{4.19}$$

Similarly for the negative branch,

$$V_{out,n} = I_{out}\left(\frac{N_nR_{load}}{1+N_nR_{load}G_{out}}\right) \tag{4.20}$$

The differential output of a current-mode FIR DAC with G_{out} current source output impedance is then:

$$\Delta V_{out} = V_{out,p} - V_{out,n} = I_{out}R_{load}\left(\frac{N_p-N_n}{(1+N_pR_{load}G_{out})(1+N_nR_{load}G_{out})}\right) \tag{4.21}$$

In the ideal case, where $\frac{1}{G_{out}}$ is ∞, ΔV_{out} is the difference between the total output currents of positive and negative coefficients times the load resistance. However, for finite output resistance, it changes depending on ratio between the load resistance and the total output resistance of the paralleled current sources, $\frac{N}{R_{out}}$. This creates data dependent distortion on the output. This has been analyzed in [BSS04]. The SFDR determined by the second-order harmonic for a FIR DAC with N number of current sources is [BSS04]:

$$SFDR_2 = \frac{NR_{load}}{4R_{out}+2NR_{load}} \tag{4.22}$$

Similar derivation were followed to obtain an expression for the third order harmonic distortion, IMD3, of a fully-differential implementation [LL03]:

$$IMD3_{FD} = \frac{\frac{14}{3}G_{out}^2N^2+\frac{16}{3}(G_{load}^2+G_{load}G_{out}N)}{G_{out}^2N^2} \tag{4.23}$$

Where G_{load} is the load conductance.

Differential circuits cancel even harmonic distortions. Thus, the SFDR is determined by the dominant third order harmonic component. For the case where the output resistance of the current sources is much greater than the load resistance times the number of current sources, $R_{out} \gg NR_{load}$, the n^{th} harmonic distortion components due to the finite output resistance can be simplified by a general formula [PS10]:

$$HD_n \approx \left(\frac{NR_{load}}{4R_{out}}\right)^{n-1} \tag{4.24}$$

Furthermore, the output impedance decreases with frequency. This affects the dynamic performance of the FIR DAC. To ensure high linearity in the 802.11ad mode, the current sources has to maintain the required Z_{out} up to near GHz output frequencies.

Assuming Figure 4.22a is the current source in cosideration, the parasitic capacitances from the drains of M_{CAS} and M_{CS} to the ground set the poles and zeroes of Z_{out} versus frequency curve [BSS04]. If the layout of the transistors of the differentially-switched cascode current source shown in Figure 4.22a is such that the parasitic capacitances of the interconnects between each transistor is minimal, the output impedance can be made to keep its DC value even at frequency values. This type of placement is discussed in Chapter 6.

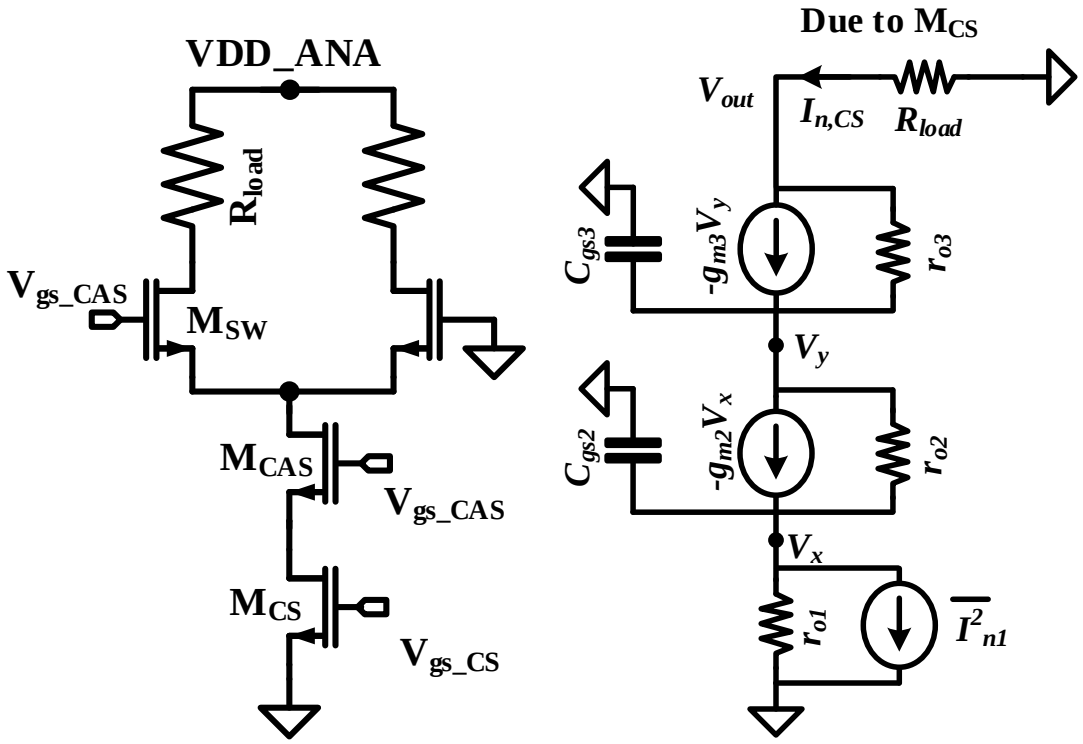
Effect of Noise on FIR DAC Dynamic Range

The generated noise at the output of the current sources of the FIR DAC puts a limit on its dynamic range. For the output of the circuit to have the desired DR, the circuit has to be modeled and the noise output should also be quantified. The analysis is based on the differentially switched cascode current source of Figure 4.22a. The noise sources are mainly drain current thermal noise and $\frac{1}{f}$ noise of the transistors, and thermal noise of the resistors. [Raz01].

The assumption is that the noise sources are uncorrelated. The output-referred noise of each source are superposed to obtain the total noise output. Then, the ratio of the total signal power to the total noise at the output is the DR.

$$\overline{I^2}_{n,total} \approx \overline{I^2}_{n,CS} + \overline{I^2}_{n,CAS} + \overline{I^2}_{n,SW} + \overline{I^2}_{n,load} \tag{4.25}$$

The small signal equivalent circuit for calculating the output-referred noise due to the drain noise of transistors M_{CS}, $\overline{I^2}_{n,CS}$, is shown in Figure 4.22b. The two circuits in Figure 4.23a and 4.23b are for calculating the output-referred noise due to the noise of transistors M_{CAS} and M_{SW} respectively. Using KVL equations at x, y, and output,



(a) (b)

Figure 4.22: a) Differentially switched cascode current source, b) Small signal model to find the output-referred noise due to $\overline{I}_{n1}$

$$\overline{I}_{n1} + \frac{V_x}{r_{o1}} + V_x S C_{gs2} + \frac{V_x}{r_{o2}} + g_{m2} V_x - \frac{V_y}{r_{o2}} = 0 \tag{4.26}$$

$$V_y\left(S C_{g3} + \frac{1}{r_{o2}} + \frac{1}{r_{o3}} + g_{m3}\right) - g_{m2} V_x - \frac{V_x}{r_{o2}} + \frac{I_{out} R_{load}}{r_{o3}} = 0 \tag{4.27}$$

$$\overline{I}_{n,CS} + g_{m3} V_y + \frac{I_{out} R_{load}}{r_{o3}} + \frac{V_y}{r_{o3}} = 0 \tag{4.28}$$

The above three equations can be combined to solve for the gain from $\overline{I}_{n1}$ to output-referred component $\overline{I}_{n,CS}$,

$$\frac{\overline{I}_{n,CS}}{\overline{I}_{n1}} = K_1 = \frac{AB\left[r_{o2}\left(g_{m3} + \frac{1}{r_{o3}}\right)\right]}{-AB\left(\frac{R_{load}}{r_{o3}} + 1\right) - \left(\frac{r_{o2}}{g_{m3} + \frac{1}{r_{o3}}}\right)\left(1 + \frac{R_{load}(1-A)}{r_{o3}}\right)} \tag{4.29}$$

Where $A = \frac{g_{m3} + \frac{1}{r_{o3}}}{\frac{1}{r_{o2}} + \frac{1}{r_{o3}} + g_{m3} + S C_{gs3}}$, and $B = \frac{g_{m2} + \frac{1}{r_{o2}}}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2} + S C_{gs2}}$.

Similar approach can be followed to find the gains from $\overline{I}_{n2}$ to output-referred component $\overline{I}_{n,CAS}$, and from $\overline{I}_{n3}$ to output-referred component $\overline{I}_{n,SW}$ to arrive at:

$$\frac{\bar{I}_{n,CAS}}{\bar{I}_{n2}} = K_2 = \frac{A(B+1)}{\frac{\frac{-AB}{r_{o2}}\left(\frac{R_{load}}{r_{o3}}-1\right)}{g_{m3}+\frac{1}{r_{o3}}}+1+\frac{R_{load}}{r_{o3}}-\left(\frac{AR_{load}}{r_{o3}}\right)} \tag{4.30}$$

$$\frac{\bar{I}_{n,SW}}{\bar{I}_{n3}} = K_3 = \frac{1-\frac{1}{A}+\frac{g_{m2}+\frac{1}{r_{o2}}}{Dr_{o2}}}{\frac{R_{load}}{r_{o3}-\frac{1}{A}\left(\frac{R_{load}}{r_{o3}}-1\right)}+\left(\frac{g_{m2}+\frac{1}{r_{o2}}}{Dr_{o2}}\right)\left(\frac{R_{load}}{r_{o3}}+1\right)} \tag{4.31}$$

Where $D = \left(g_{m3}+\frac{1}{r_{o3}}\right)\left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}+g_{m2}+SC_{gs2}\right)$.

Each of the drain noise components, $\overline{I^2}_{n,1}$,$\overline{I^2}_{n2}$, $\overline{I^2}_{n3}$, contain both thermal noise, $\overline{I^2}_{n,d}$, and flicker noise, $\overline{I^2}_{n,\frac{1}{f}}$. The flicker noise is represented in the same manner as the drain thermal noise from drain to the source. Thus, the drain noise of the three transistors can be formulated as follows [Gra01].

$$\overline{I^2}_{n,d} = \overline{I^2}_{n,t} + \overline{I^2}_{n,\frac{1}{f}} = \left(4\gamma kT g_m + K'\frac{I_{UCC}}{f}\right)\Delta f \tag{4.32}$$

The other noise components is the thermal noise of the resistor and is given by:

$$\overline{I^2}_{n,load} = 4kT\frac{1}{R_{load}}\Delta f \tag{4.33}$$

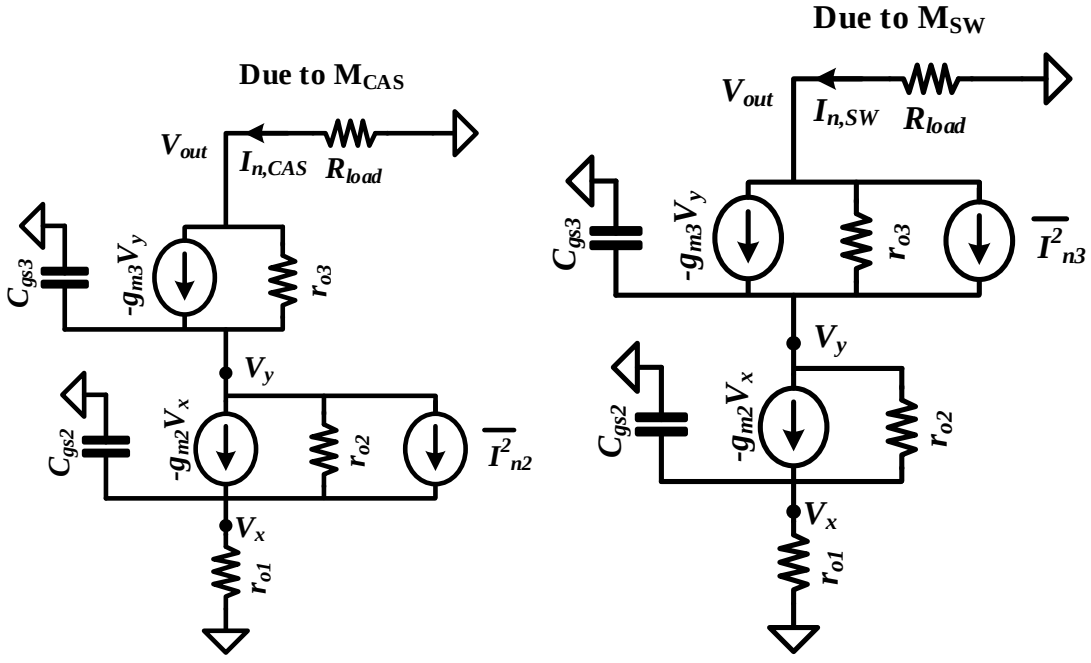


Figure 4.23: Small signal model to find the output-referred noise due a) $\bar{I}_{n2}$ b) $\bar{I}_{n3}$

Where γ is device dependent coefficient. A value of 2/3 is taken for long channel devices, but it increases for devices in nanometer processes [Gra01]. $k = 1.38x10^{-23}$ is Boltzmann's constant, $T = 300°K$ is taken for room temperature, K' is another device dependent constant and Δf is the bandwidth over which the noise is integrated.

$$\overline{I^2}_{n,CS} = K_1^2 \overline{I^2}_{n,d}|_{g_m=g_{m1}} \tag{4.34}$$

$$\overline{I^2}_{n,CAS} = K_2^2 \overline{I^2}_{n,d}|_{g_m=g_{m2}} \tag{4.35}$$

$$\overline{I^2}_{n,SW} = K_3^2 \overline{I^2}_{n,d}|_{g_m=g_{m3}} \tag{4.36}$$

The total noise power at the output is then:

$$P_{noise} = N\overline{I^2}_{n,total} = N\left(\overline{I^2}_{n,CS} + \overline{I^2}_{n,CAS} + \overline{I^2}_{n,SW} + \overline{I^2}_{n,load}\right) \tag{4.37}$$

N is number of UCCs in the FIR DAC implementation. The gate-source parasitic capacitance are evaluated at the bandwidth of the FIR DAC. It is 880 MHz for the 802.11ad mode, and 160 MHz for the 802.11ac 160 MHz modes.

Some assumption could be taken to simplify expressions of K_1, K_2, and K_3. For example, $r_o \gg \frac{1}{g_m}$. Another assumption is the product of the load resistance and the drain-to-source conductance is much smaller than one: $\frac{R_{load}}{r_o} \ll 1$. At the frequency of operation $g_m \gg SC_{gs}$. A and B are approximated to unity with those assumptions. $D \approx g_{m2}g_{m3}$.

$$K_1^2 \approx \left(r_{o2}g_{m3}\right)^2 \tag{4.38}$$

$$K_2^2 \approx \left(\frac{2g_{m3}}{g_{ds2} + g_{m3}}\right)^2 \approx 4 \tag{4.39}$$

$$K_3^2 \approx 1 \tag{4.40}$$

With this new values the total noise power is approximated to:

$$P_{noise} \approx 4kTBW\left[g_{m1}\left(r_{o2}g_{m3}\right)^2 + 4g_{m2} + g_{m3}\right] + K'I_{UCC}\left[5 + \left(r_{o2}g_{m3}\right)^2\right]\ln BW \tag{4.41}$$

The average signal power is a summation of the full-scale current flowing in the load resistors.

$$P_{sig} = 0.5NI_{UCC}^2 \tag{4.42}$$

$$DR = \frac{P_{sig}}{P_{noise}} \tag{4.43}$$

The dynamic range can then be expressed as follows:

$$DR \approx \frac{NI_{UCC}^2}{8kTBW\left[g_{m1}\left(r_{o2}g_{m3}\right)^2+4g_{m2}+g_{m3}\right]+K'I_{UCC}\left[5+\left(r_{o2}g_{m3}\right)^2\right]\ln BW} \tag{4.44}$$

The transconductance term in K_1 can be replaced by an equation containing the current value, I_{UCC}, and some technological constants. However, the r_{o2} term in K_1 would have to be calculated for each new current value. Hence, it is not straightforward to run multiple simulations with this expression of DR. As can be seen from the values of the gains, the noise contribution from the current source transistor, M_{CS}, is much greater than the contribution from both the cascode transistor, M_{CAS}, and the switch device, M_{SW}. This is because the ratio $(r_{o2}g_{m3})^2$ is on the order of hundreds as per transistor-level simulation of a differentially-switched cascode current source circuit. Therefore, if some additional tolerance is taken on the output noise value of the current source transistor, it simplifies the analysis to ignore the switch and cascode devices. For that, let $(r_{o2}g_{m3})^2$ be K_{CS_R} then:

$$g_{m1}\left(r_{o2}g_{m3}\right)^2 + 4g_{m2} + g_{m3} \approx g_{m1}K_{CS\_R} \tag{4.45}$$

Then the dynamic range formula can be simplified to an expression containing technological constants and the variables N, unit current, I_{UCC}, and bandwidth, BW.

$$DR \approx \frac{NI_{UCC}^2}{8kTBWg_{m1}K_{CS\_R}+K'K_{CS\_R}I_{UCC}\ln BW} \tag{4.46}$$

This DR expression can be further expanded so that it is expressed only in terms of I_{UCC} and constants. The transconductance of the current source transistor, g_{m1}, can be expressed in terms of I_{UCC}. Since M_{CS} is expected to be in saturation, the transcondcutance is given as:

$$g_{m1} = \sqrt{2k_{ox}\frac{W}{L}I_{UCC}} \tag{4.47}$$

This can be inserted in Equation (4.46) to arrive at an expression for DR which is more insightful.

$$DR \approx 10\log_{10}\left[\frac{NI_{UCC}^2}{D_1\sqrt{I_{UCC}}+D_2I_{UCC}}\right] \tag{4.48}$$

Where k_{ox} is a technological constant, the left-hand side denominator constant, D_1 is $8kTBW\sqrt{2k_{ox}\frac{W}{L}}K_{CS\_R}$, and the right-hand side denominator constant, D_2 is $K'K_{CS\_R}\ln BW$. It is observed in simulation that K_{CS_R} decreases as current increases due to decrease in drain-source output resistance. Therefore, the dynamic range value given by Equation (4.48) increases with increase of unit current, I_{UCC}, and then plateaus.

The dynamic range formula in Equation (4.48) is used to find the optimum current value in the design of the UCC in Chapter 6. Since the BW and the number of UCCs, N, are different for in the two modes of operation the FIR DAC is designed, the unit current values for the same DR in each mode are separately estimated. A maximum value of the two I_{UCC} which guarantees the required dynamic range for the two modes is taken.

If the I_{UCC} is to be controlled off-chip by a reference current as is the case in the implementation of the prototype FIR DAC discussed in Chapter 6, then the dynamic range can be improved by using higher reference current values.

4.6 Summary and Conclusions

Starting from basic DAC operation, specification, and architecture, the chapter has evolved to analysis of FIR DACs. A detailed treatment of the pros and cons of the different FIR DAC architectures has been presented. The traditional multi-bit DACs are classed under the a general FIR DAC structure as $L-bit$, 1-tap, and they are compared with L-bit, N-tap, and 1-bit, N-tap FIR DACs.

Furthermore, frequency translation of FIR DACs, from LPF to BPF, and LPF to HPF, is explained theoretically with examples using impulse responses. A novel configurable delay line that can be used to implement these frequency translation is also introduced.

A thorough literature review on FIR DAC is conducted by grouping the different works according to their applications—multi-bit, 1-bit, programmable, receive-band noise filter and amplifying FIR DACs.

Finally, analysis of a current-steering FIR DAC is presented where expressions for coefficient mismatch, yield model, and effect of finite output impedance are derived. The discussion of the last section will be useful in Chapter 6 where the implementation of a FIR DAC in 28nm CMOS FDSOI is discussed.

Chapter 5

Proposed IEEE 802.11ac/ad Transmitter Baseband Architecture

In the discussion of multi-standard transmitters in Chapter 3, the possibility of multi-standard operation by modifying some circuit blocks of the transmitter has been studied. Many of the works that were reviewed focused on the interface between digital and analog parts of the transmitter. In Chapter 4, the FIR DAC was introduced as a key enabling block for multi-standard transmitter. In this chapter, a FIR DAC based multi-standard, multi-mode transmitter baseband architecture is presented.

The proposed architecture is validated using MATLAB® on system level for two recent multi-Gb/s standards. The chapter will start by introducing these standards. Then in the next section, the main components that make up the digital processing block are presented. This is followed by developing the FIR DAC specification for these standards. The chapter ends by presenting some interesting simulation results.

5.1 Specification of the standards

This work takes the IEEE 802.11ac and IEEE 802.11ad WiFi standards as target application. The reason this two standards are selected is the extreme nature of their baseband signals—802.11ac has high resolution, medium bandwidth baseband data and 802.11ad has low resolution, wideband baseband data. The FIR DAC specification was driven with the requirements of these two standards in mind. In this section, a brief overview of the features, applications and requirements of these standards is stipulated.

5.1.1 IEEE 802.11ac

The IEEE 802.11ac is a VHT WiFi standard that is transmitted in frequency bands at 5 GHz. It extends the 802.11n standard by adding new channel bandwidth options that achieve higher data rates. It also comes with the advantage of avoiding the crowded 2.4 GHz standard. It supports MIMO to reach gigabit data rates. It has the capacity to support data rates of 7 Gb/s using an 8 x 8 MIMO architecture and a 256QAM modulation. However, for portable devices, only a single spatial stream is envisaged, providing

data rates up to 780 Mb/s. It is also backward compatible with the older WiFi standard such as the 802.11n.

The standard support four contiguous channel bandwidths—20 MHz, 40 MHz, 80 MHz, and 160 MHz—and additional non-contiguous 80+80 MHz channel bandwidth [Int+14]. The 80 MHz, 160 MHz and 80+80 MHz channel bandwidths are new additions compared to the 802.11n 2.4 GHz standard. However, only 20 MHz, 40 MHz and 80 MHz are mandatory, the 80+80 MHz and 160 MHz are stipulated under those the VHT STA can optionally support. The 802.11ac VHT PHY is only defined for OFDM with total number of subcarriers 56, 114, 242, 242, and 484 for the channel widths 20 MHz, 40 MHz, 80 MHz, 80+80 MHz and 160 MHz respectively. The supported modulation methods are BPSK, QPSK, 16-QAM, 64-QAM, and an optional 256-QAM.

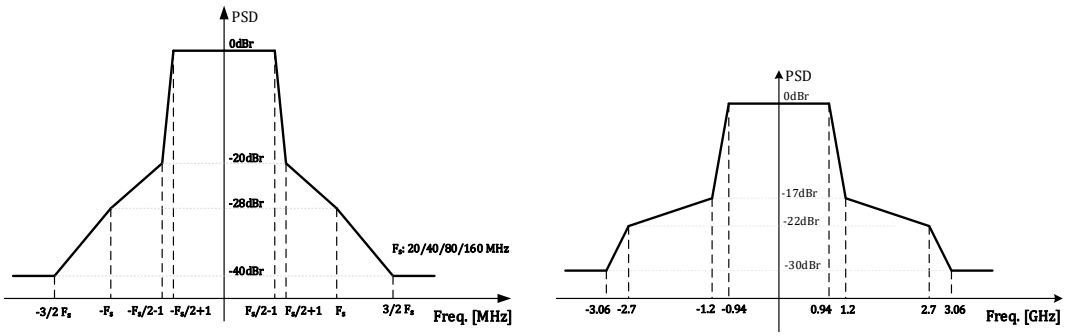
An IEEE 802.11ac conforming transmitter has an output spectrum that conforms to the spectrum mask shown in Figure 5.1a. The transmit mask shapes for all of the contiguous channel bandwidths are the same with only the offet frequency changed. A common transmit constellation error is also defined equally for all the contiguous channel bandwidths. There are other additional requirements; however, with respect to the scope of this work they are not applied here.

5.1.2 IEEE 802.11ad

Obstruction and propagation losses, at 60 GHz, limit the applicability of the 802.11ad to line-of-sight and short-range services such as wireless display of data, wireless sync, wireless docking, and high speed file transfer between devices. Since the application area which this standard targets are different from the other standards, the possibility of tri-band single radio operation with the 2.4 GHz 802.11n standard and the 5 GHz 802.11ac standard was discussed in Chapter 2.

The IEEE 802.11ad standard, adopted from WiGig, utilizes the unlicensed spectrum from 57 GHz–66 GHz in Europe [Int+14]. There are four available channels that have a channel spacing of 2.16 GHz. The 802.11ad PHY supports four modes of with distinct MCS. They are the Control PHY which is transmitted using $\frac{\pi}{2}$-DBPSK modulation; the SC PHY which is transmitted using $\frac{\pi}{2}$-BPSK, $\frac{\pi}{2}$-QPSK, and $\frac{\pi}{2}$-16QAM modulation methods and at different coding rates; the LP SC PHY which shares the same MCS as the SC PHY except for the absence of the $\frac{\pi}{2}$-16QAM; and finally the OFDM PHY which in addition to the MCS listed in the SC PHY includes 64-QAM in its MCS.

All the first three modes have a chip rate of 1.76 GHz whereas the OFDM mode has a 2.64 GHz sample rate. The standard offers data rates up to 6757 Mb/s in OFDM, 4620 Mb/s in SC, and up to 2503 Mb/s with the low power version of the SC mode. In the transmitter side, a common preamble is defined for both OFDM and SC. While a windowing function is defined for the OFDM, the SC fields are not



(a) (b)

Figure 5.1: The transmit masks of the IEEE 802.11ac and IEEE 802.11ad standards

windowed. Beamforming training fields are common to all modes. They are added because of the losses at the frequency of transmission of this standard. It makes the transmission directional—hence the name DMG.

A common transmit mask is defined as shown in Figure 5.1b, and different EVM values for each MCS of the OFDM and SC PHYs. The OFDM mode has additional requirements. However, the target applications of this work are mainly low power mobile devices. Transmission with OFDM tend to result in higher power consumption. Hence, the LP SC PHY of the 802.11ad standard is the target mode.

5.2 System Level Simulation of Proposed Transmitter Architecture

The purpose of the system level simulation was to obtain a better understanding of the FIR DAC as part of a complete multi-standard transmitter baseband. It helped to set realistic specifications on the rest of the transmitter chain and assess the potential performance limits of the FIR DAC. Furthermore, from a design point of view, a top-down approach helps to keep exploring a single block without losing sight of what the specifications set on the lower level abstraction of that block guarantee on system level.

Table 5.1: Summary of the Specifications of the 802.11ac and 802.11ad standards

Parameter	**802.11ac**				**802.11ad**
Bandwidth (MHz)	20	40	80	160	1760
Input Resolution	9-bit	10-bit	11-bit	12-bit	1-bit
	@ 16-QAM (channelized)				@ $^{\pi}/_{2}$-QPSK
Mask (@ offset in MHz)	-40dBr @				-30dBr @
	30	60	120	240	3060

The system level simulation was carried out for the different channel bandwidths and transmission modes of the 802.11ac and 802.11ad. While it is less challenging to demonstrate the system for the channel bandwidths of 20 MHz and 40 MHz in the 802.11ac case, the potential of the proposed system to integrate with new applications that take advantage of the full potential of the 802.11ac standard would be demonstrated better if the system is validated for the new channel bandwidth flavors of 80 MHz and 160 MHz. Therefore, most of the simulation results would be that of 160 MHz channel bandwidth of the 802.11ac standard.

Complex baseband 802.11ac signals are generated using a reference waveform generator by the IEEE 802.11. The code can generate all channel bandwidths, MCS for both single user and multi-user transmission. As an example, the 160 MHz baseband signal is shown in Figure 5.2.

5.2.1 Standard Coexistence

As a 60 GHz standard, 802.11ad offers only a line-of-sight, short-range wireless networking. The fact that it does not interfere with nearby communication is one of its strengths. On the contrary, a 802.11ac transmitter has to still be designed with consideration for its out-of-band noise profile so that it can coexist with others standards. This is despite the fact that the 802.11ac bands at 5 GHz are less crowded than the 2.4 GHz bands.

There are many standards within one octave below the carrier frequencies of the 802.11ac bands. Some of the nearby standards such as GPS, for example, require the interfering emissions in their receive noise floor to be limited to less than or equal to -174 dBm/Hz . This is the same value as the thermal noise floor at room temperature.

If possible the required value for the PSD of the out-of-band noise profile of the 802.11ac transmitter should not also be greater than -174 dBm/Hz. To take this into consideration while designing the FIR DAC transfer function, some practical assumptions can be taken. The expected output PSD at the receiver due to the interfering out-of-band noise of the transmitter can be equated as:

$$PSD_{OOB} - P_{BPF} - P_{ANT} \leqslant -174dBm/Hz \tag{5.1}$$

Where P_{BPF} and P_{ANT} are the the power losses which the out-of-band noise experiences on its way to the receiver. A coexistence bandpass filter at the output of the transmitter can be expected to attenuate the noise by about 40 dB. Then there is coupling loss from antenna of 802.11ac to the receiving antenna of the other standard. This can be taken to be around 12 dB.

$$PSD_{OOB} - 40dB - 12dB \leqslant -174dBm/Hz \tag{5.2}$$

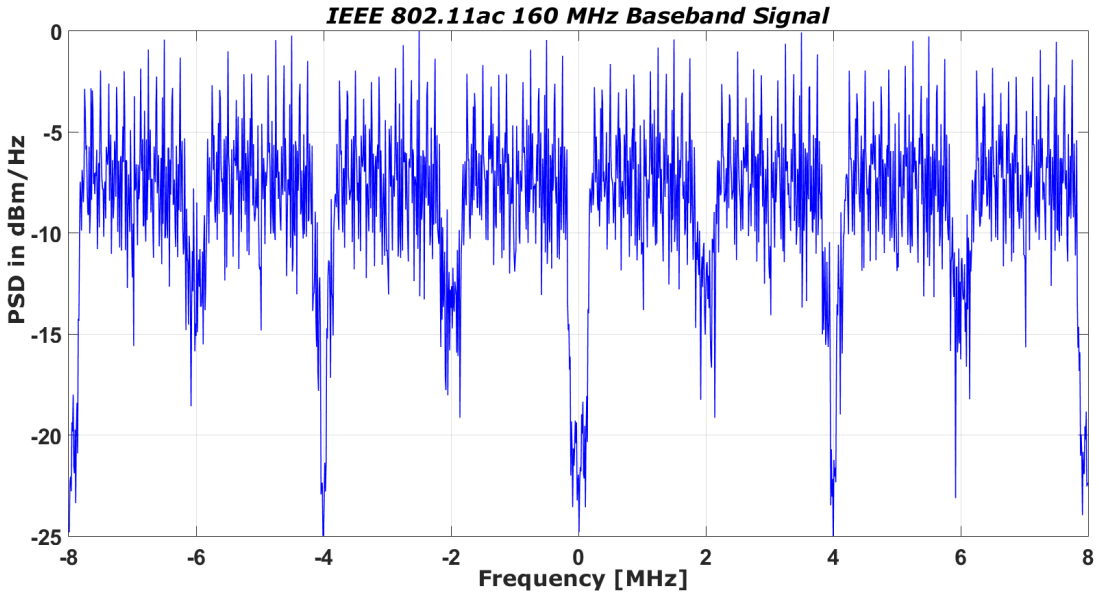


Figure 5.2: 160 MHz Baseband Signal at 802.11ac Transmitter Input

The resulting PSD_{OOB} value is less than or equal to -122 dBm/Hz. If worst case scenario is assumed, then PSD_{OOB} should still be less than -122 dBm/Hz even when transmitting at the maximum allowed output power i.e., 20 dBm in Europe. For the 160 MHz mode of the 802.11ac, this maximum output power divided by the 160 MHz results in a PSD of -62 dBm/Hz in the passband of the 160 MHz channel. The stopband rejection is then estimated relative to this maximum PSD. Therefore, the filter has to attenuate its stopband spurs by at least -60 dB relative to the PSD in the passband of the transmitted output signal for PSD_{OOB} to be lower than -122 dBm/Hz.

The same approach can be followed for the other modes of the 802.11ac. The PSD for the 20 MHz channel bandwidth becomes -53 dBm/Hz in the passband of the 20 MHz channel, which is about 10 dB higher than that of 160 MHz, at the maximum output power of 20 dBm. Everything being the same, the 20 MHz mode of the FIR DAC has to reduce its spurs by further 10 dB for PSD_{OOB} to be lower than -122 dBm/Hz. Therefore, the filter in the 20 MHz mode of the 802.11ac has to be designed for -72 dBc out-of-band attenuation. The good news is that the 20 MHz channel bandwidth can expect a higher SNR from the DSP blocks compared with the 160 MHz due its higher OSR.

5.2.2 Transmitter Baseband Architecture

This architecture targets devices that normally operate in a high-throughput 802.11ac standard, but can switch the hardware to an 802.11ad configuration for specific LP multi-Gb/s services. Therefore, the two standards complement each other to deliver power-efficient and high speed communication.

One of the challenges in designing a single-hardware 802.11ac/ad multistandard transmitter stems from the extreme difference in the nature of the signal to be transmitted, as summarized in Table 5.3. The 802.11ac presents high-resolution and narrow-to-medium bandwidth channels. On the other hand, the 802.11ad has a low-resolution broadband input. Additionally, the transmitter mask requirements in the 5 GHz bands are more stringent than those at 60 GHz.

A traditional way of transmitting these data is depicted in Chapter 3 using direct conversion architectures with oversampled DACs followed by low-pass filters to reject the image replicas and respect the required transmission masks. To address a multi-standard within the same hardware, one of the works discussed in Chapter 3 introduces a direct-digital RF modulator for 802.11g WLAN, WCDMA, and GSM/EDGE [Elo+07]. However, this approach is limited to narrow bandwidth signals because of high OSR requirements. In addition, this architecture requires additional image replica filtering or needs highly programmable sample rate converters, as proposed in [Rov+13], to adapt to the appropriate radio channel.

Multi-standard transmitters take advantage of high OSR by introducing noise-shaping $\Delta\Sigma$ modulators to reduce the DAC resolution. This is only possible in the highly oversampled 802.11ac digital front-end path. In the 802.11ad path, the low OSR limits the noise-shaping capability of the modulator. Noise-shaping architectures produce a great deal of quantization noise outside the band of interest, and filtering of this noise is challenging. Otherwise, a high oversampling configuration and an off-chip LC bandpass filter to reject image spectra and minimize the shaped out-of-band quantization noise is required [Moh+12]. However, the required rejection is hardly achievable for large bandwidths with this method.

In order to overcome image and quantization noise requirements, this architecture proposes a low-power multi-mode, multi-standard transmitter based on a 1-bit semi-digital filtering DAC, which is configurable for both narrow band and broadband standards, while optimally reusing hardware. The idea is to configure the semi-digital filter to remove the quantization noise in the 802.11ac mode and to shape the broadband channel according to the mask requirements of the 802.11ad standard. This would advantageously replace the multi-bit DAC and the analog low pass filter, while moderately increasing the complexity of the DSP blocks.

5.2.3 DSP Blocks of 802.11ad

The LP SC baseband output of the 802.11ad has a chip rate of 1.76 GHz with a resolution of 1-bit in each I/Q branch in QPSK modulation. To ease filtering of image replicas, the data can be oversampled by a minimum of two to a sample rate of $\geqslant$ 3.52 GS/s at the FIR DAC input. This can be justified by

considering the filtering required to attenuate sampling images sufficiently. A 3.52 GHz clocked DAC output will attenuate the images by at least 2 dB starting from an offset of 2.64 GHz from the center of the desired band of the 802.11ad. However, the required rejection is more than 22 dB, Figure 5.1b, which can be achieved using a reconstruction analog low pass filter following the DAC. Assuming a 2nd-order filter, it has at least 12 dB/octave roll-off starting the cut-off frequency. Since 2.64 GHz is more than 3 octaves, the desired image rejection is achieved with the a simple analog circuitry. With no oversampling, the same analysis can be done and a complex high-order analog filtering is required to fulfill the spectrum mask requirements.

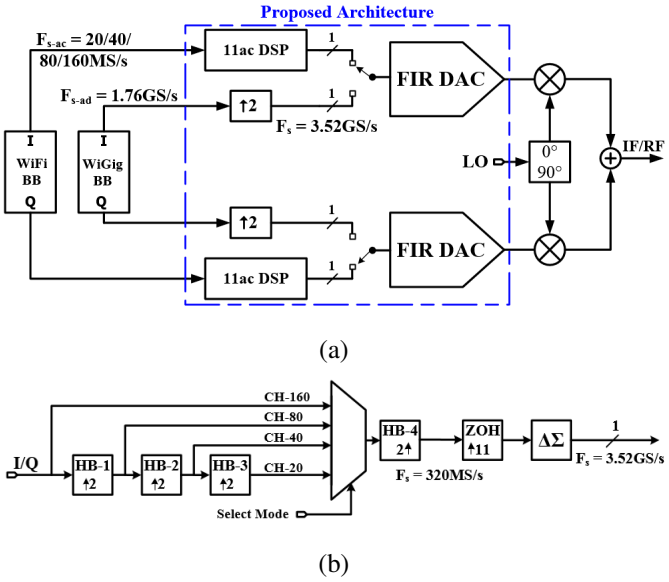


Figure 5.3: Poposed transmitter architecture for IEEE 802.11ac/ad standards and the DSP part of the 802.11ac

There are different types of oversampling processes that can be implemented for the 802.11ad mode. Oversampling of the 802.11ad LP SC data with interpolation filters is not required at this stage to avoid adding resolution to the data. As that necessitates usage of multi-bit digital to analog converter, or a delta-sigma modulator to convert it to 1-bit. In the second scenario, as the noise shaping capability of a delta-sigma converter is dependent on the OSR of its input data, a modulator with an OSR of two would not achieve high SNR in its in-band. For example, with a 3rd-order CRFB 1-bit output delta-sigma modulator at an OSR of two, the peak theoretical in-band SNR is less than 2 dB. It only stabilizes at less than 0.67, i.e. -3.5 dB, of the full scale amplitude [Sch00]. A different approach and a different structure of a modulator may achieve better results than the predicted peak, but generally high OSR is required for the delta-sigma to add value.

There was also a possibility to choose an OSR of more than two. In this scenario, the usage of a

delta-sigma modulator is justified as it shapes the noise with high SNR in its in-band. For example, a 2nd-order modulator with an OSR of six is employed here [BA15] for 802.11ad transmitter that also processes higher order modulations such as 16-QAM of the SC mode. For the low power application sought usng the LP SC mode of the 802.11ad, however, an oversampling of two is chosen .

Table 5.2: Frequency Planning for IEEE 802.11ac/ad Transmitter

Standard	**IEEE 802.11ac**				**IEEE 802.11ad**
Channel Bandwidth (MHz)	20	40	80	160	1760
Half-band filter OSR	16	8	4	2	upsample by 2
New Sample Rates (MHz)	320				3520
Common ZOH OSR	11				N/A
Multi-standard rate	3.52 GHz				

An oversampling method which does not introduce new data are upsampling, also called zero-insertion, and ZOH response. The SINC response of the ZOH introduces passband drooping which degrades the EVM. Thus, a zero-insertion process is chosen as it requires no additional hardware and keeps the passband ripple unchanged. Zero-insertion leaves the added zeros to be shaped by an interpolation filter. The FIR DAC, in this case, is functioning as an interpolation filter.

5.2.4 DSP Blocks of 802.11ac

The required out of band attenuation for the 802.11ac is 60 dBr (discussed in sub-section 5.2.1). The same reconstruction filter as for the 802.11ad is assumed, 2nd-order low pass filter with 12 dB/octave roll-off. This filter is not considered in the simulation in this chapter. It is only being assumed for analysis. For the 160 MHz channel bandwidth, a stopband rejection of 60 dBr would be obtained at an offset of 2560 MHz assuming the cut-off frequency of the filter is 80 MHz. In other words, the data has to be oversampled by an OSR of $\frac{2560}{160}$ or 16. To operate the FIR DAC at lower speeds, a higher order reconstruction filter than the 2nd-order assumed is needed to filter out the images.

An interesting frequency plan is to use a single clock for the FIR DAC for the two standards. To use 3520 MHz clock rate of the 802.11ad at the FIR DAC, the OSR of 802.11ac has to increase to 22 for the 160 MHz mode. Similarly, the other modes of the 802.11ac are oversampled as tabulated in Table 5.2. Intermediate DSP blocks clocking requirements are easily derived from the same frequency synthesizer due to the integer relationship between the different sampling rates. This is a necessary sacrifice to optimize hardware sharing, and it makes the proposed architecture, as detailed in Figure 5.3a, easier to adapt to a complete transceiver implementation.

Half-Band Filters

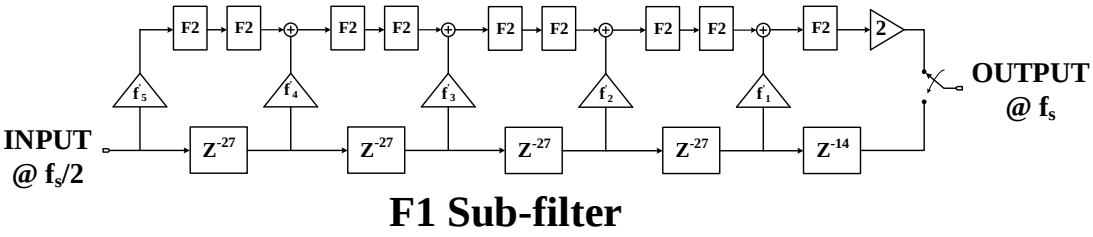


Figure 5.4: Schematic of the multiplierless half-band filter with coefficients of sub-filter F1 shown

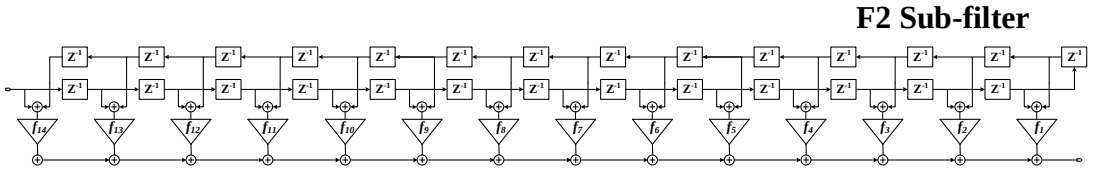


Figure 5.5: Schematic of the sub-filter F2 with its 14 long coefficients

In the 802.11ac case, the input data are oversampled using first stage oversampling block to a common sampling rate of 320 MS/s as shown in Figure 5.3b. Half-band filters are the initial interpolating block because of their ability to suppress the lowest image of the input signal without significantly degrading the SNR of the in-band. They are designed based on multiplierless half-band filters [Sar87]. The required coefficients of the filters are generated using functions from a MATLAB® Toolbox [Sch00].

Each half-band filter is designed at $0.23 f_s$ cutoff frequency, f_s is sampling rate of the half-band filter, and achieves -89 dB stopband attenuation and a 10^{-4} passband ripple. The structure of the half-band filter is shown in Figures 5.4 and 5.5. The half-band filter can be implemented with only 264 additions.

The responses of the main half-band filter and its sub-filters, F_1 and F_2, are shown in Figure 5.6. Sub-filter F1 has a length of five whereas F2 is 14. Interpolation is included in the structure. The plot shown are for an interpolation by two.

As an illustration, for the 160 MHz of the 802.11ac case, the data is resampled by two to reach an sampling rate of 320 Ms/s. The spectrum of the output of the half-band filter for this case is shown in Figure 5.7.

ZOH

The 320 MS/s data are then oversampled by a ZOH by a ratio of 11 to reach the final 3.52 GS/s sampling rate. Interpolation using a ZOH method is straightforward but produces residual images at 320-MHz offsets. However, these images will be eliminated by the semidigital low-pass filtering provided to remove

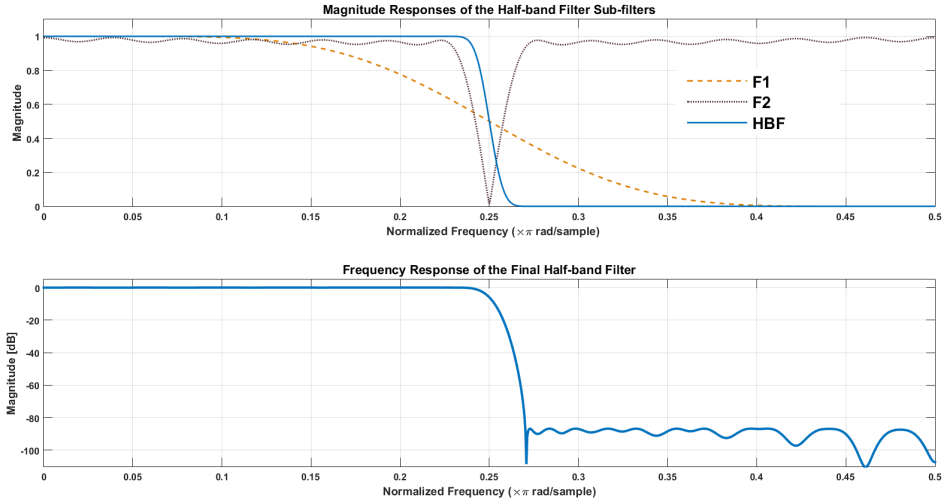


Figure 5.6: The frequency responses of the main interpolation by two half-band filter and its sub-filters

the out-of-band quantization noise. In addition, the passband ripple due to the SINC function of the ZOH does not degrade the integrity of the signal as it passes through at least one half-band filter.

The 160 MHz signal at the output of the ZOH is shown in Figure 5.8. The first image is attenuated by not more than 15dB. As expected, filtering notches as per the OSR are seen at the multiples of the original sampling rate.

Delta-Sigma Modulator

A configurable third-order 1-bit delta–sigma modulator, at a noise transfer function gain of 1.6, with coefficient sets adjusted for the four different OSR values, delivers the lowest in-band noise floor for each channel bandwidth of the 802.11ac standard. The modulator has scaled coefficients to guarantee maximum input range and stability. This modulator uses the CRFB topology of the Schreier Toolbox [ST05]. The configurability of this block can be implemented at the register transfer level with minimum hardware overhead. A 3rd-order delta-sigma modulator with CIFB architecture whose coefficients are quantized for the four modes of the 802.11ac standard, albeit at relatively higher OSR, is also reported in [Mar+15].

The signal transfer function of the CRFB structure can be made flat in the passband as shown in Figure 5.10 by feeding the input only on the first adder in Figure 5.9 [Sch00]. The noise transfer function is optimized to implements a zero in the in-band of the signal.

The output of the $\Delta\Sigma$ modulator with the ZOH output signal as its input is shown in Figure 5.10.

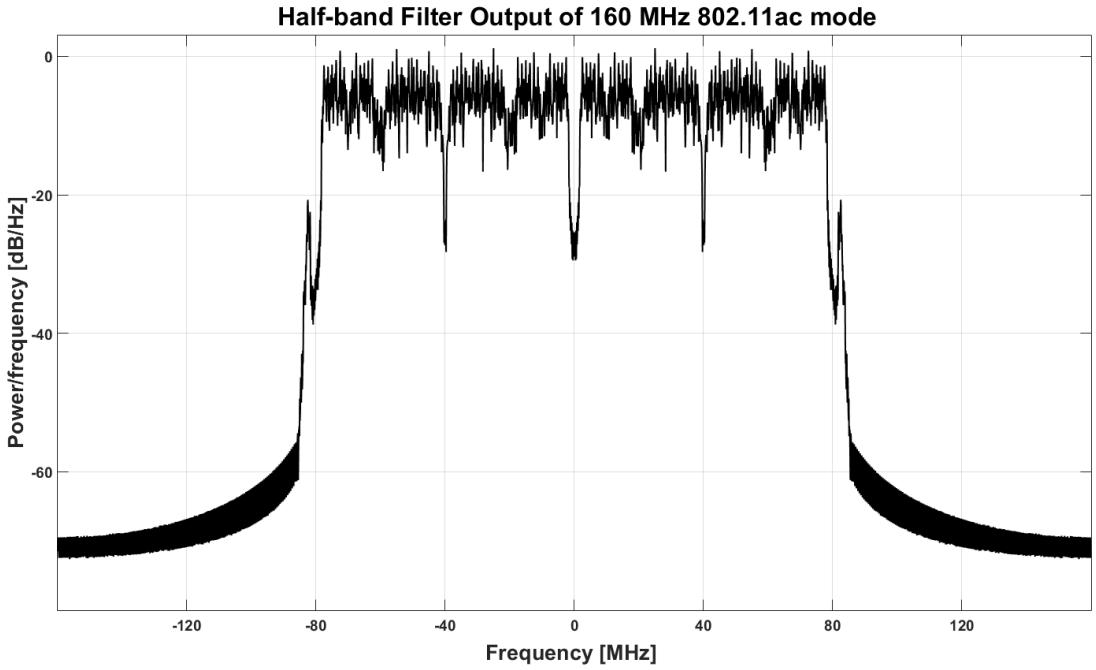


Figure 5.7: Signal at the Output of Half-band Filters for 160 MHz Input

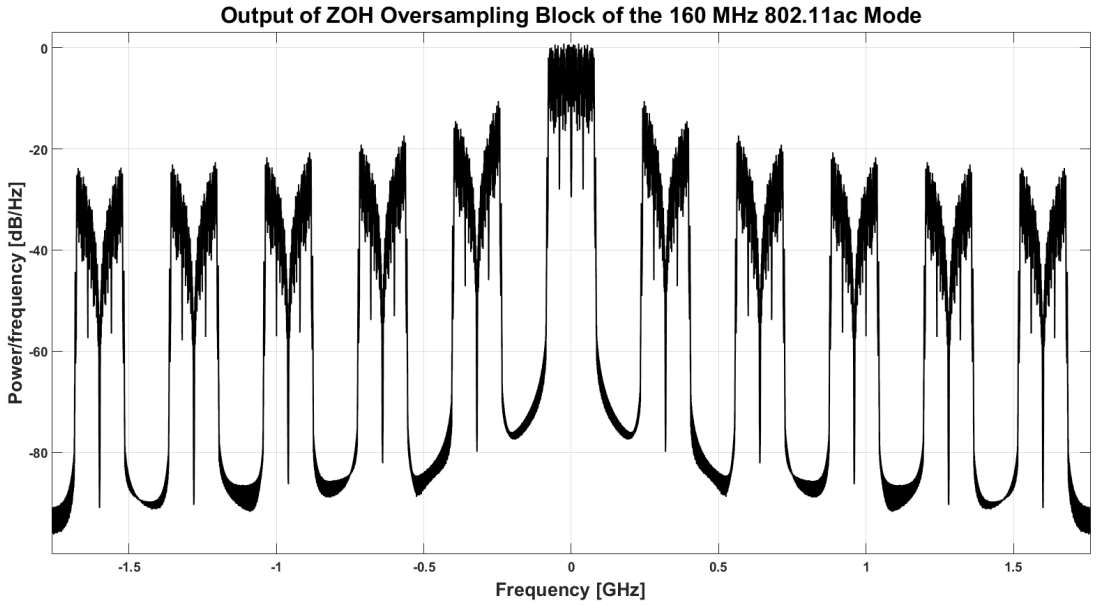


Figure 5.8: Output of Zero-Order-Hold for 160 MHz Baseband Input

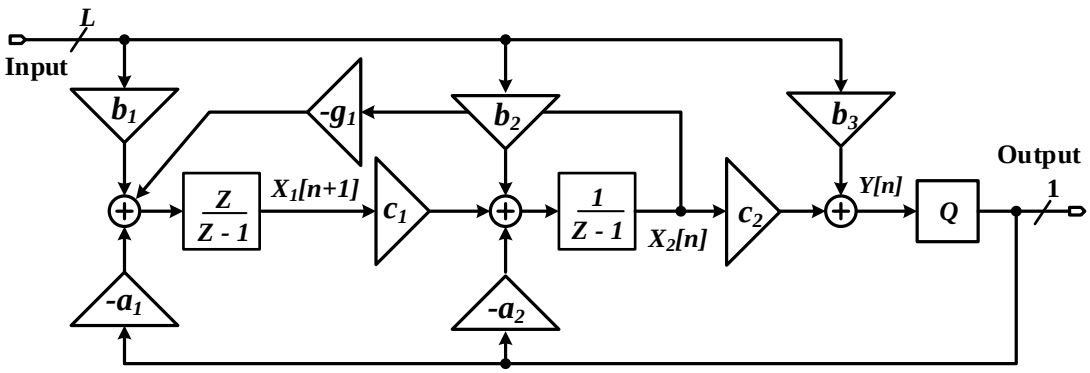


Figure 5.9: Schematic of a 3^{rd}-order, 1-bit Delta-Sigma modulator with CRFB topology

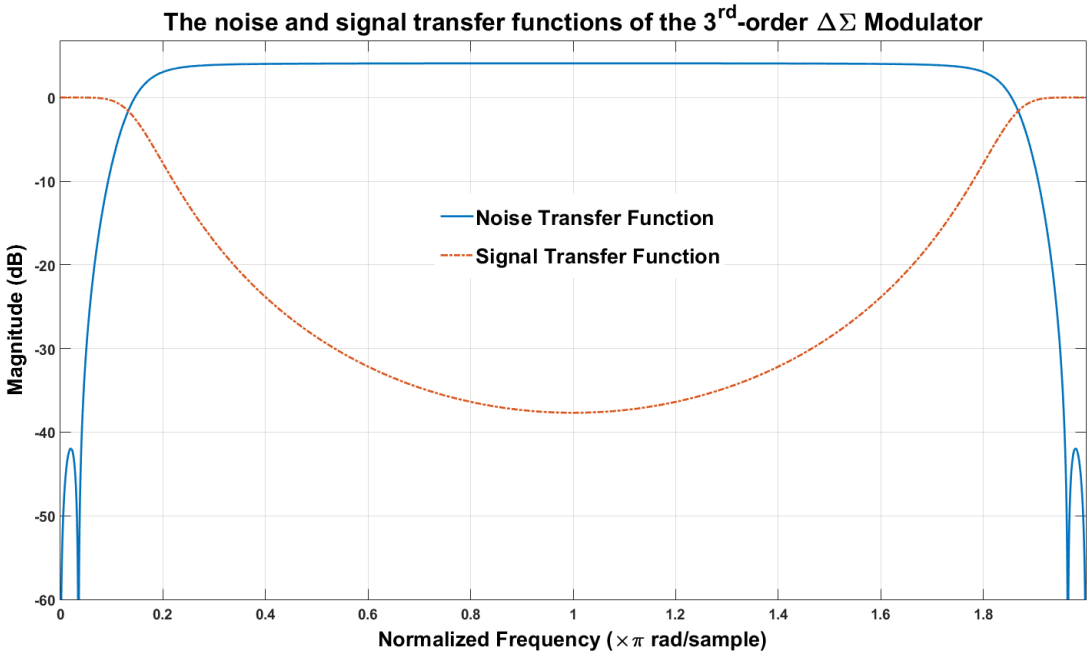


Figure 5.10: Noise and signal tranfer functions of the 3^{rd}-order, 1-bit Delta-Sigma modulator with CRFB topology

5.2.5 FIR DAC In Three Modes

Coefficients are designed based on mask requirements. Four transmit masks for each mode of 802.11ac and an additional mask for the 802.11ad standard require five sets of coefficients. In the case of 802.11ac, optimization was performed to utilize one set of coefficients for more than one mode. This is based on the SNR of the delta-sigma modulator output and the spectral mask requirements. For the 802.11ad, the transmit mask and EVM performance of different filter types at different lengths were simulated.

802.11ad Mode

FIR filter can be designed with windowing method. The basic idea of this method is that a desired brick-wall filter in frequency domain can be generated by using an infinitely long SINC shaped impulse response in time domain. As this is practically impossible to implement, the length of the SINC function has to be truncated. This results in filter whose frequency response has a transition band with a fast roll-off, but with ripples in the passband. The reason for this behavior is because of multiplication of the SINC function by a rectangular window during truncation.

A better approach is to use a window function which prioritizes some parameter—either passband ripple, stopband ripple or transition band. A Kaiser-Bessel window function has a parameter to trade-off transition band with stopband ripple. This gives the designer a degree of freedom.

Initially the 802.11ad filters was designed based on Kaiser-Bessel window function. The results obtained were a good approximation of the minimum filter length required to achieve the stopband attentuation desired. Then the EVM performance of the designed FIR DACs were compared with the standard requirements. In the case of 802.11ad, the simulated EVM of the designed filter was within a small margin of the standard requirement (-15dB for $\frac{\pi}{2}$-QPSK) even at high filter orders. A large EVM contribution from our blocks puts stringent design requirements on remaining analog circuits of the transmitter. Hence, the Kaiser-Bessel function has to be replaced.

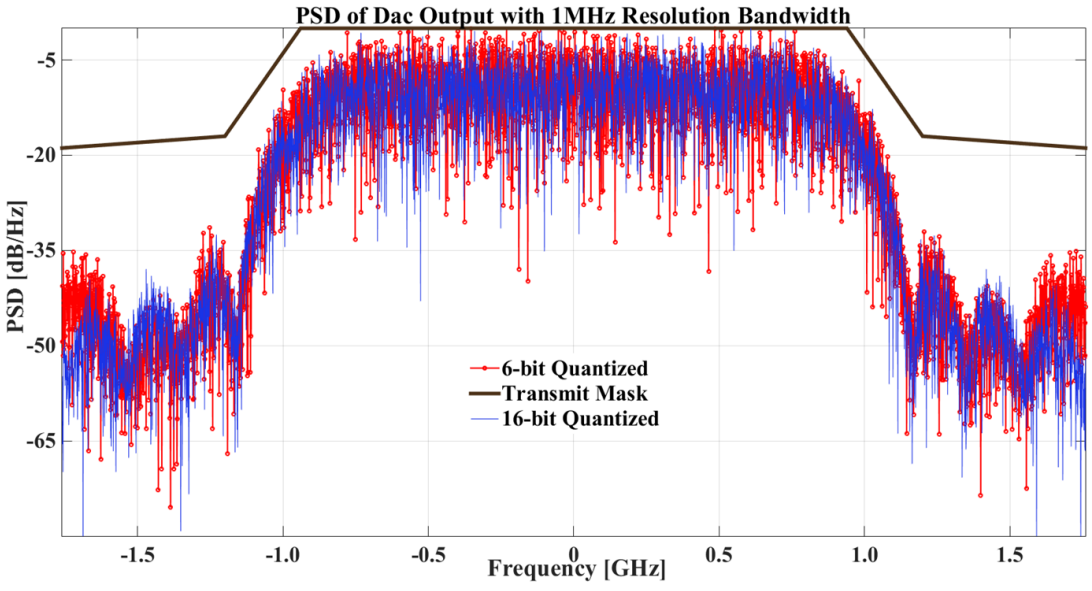


Figure 5.11: The output of the 802.11ad FIR DAC for 6-bit quantized and 16-bit quantized coefficients. The output fulfills the transmit mask requirements with more than 15dB margin.

Since the receive filter for EVM measurement is specified to be an RRC filter with a roll-off factor

of 0.25 [Int+14], it was only right to design the transmit filter with an RRC filter too. The EVM that resulted with the matched filter approach, -52 dB, was found to be a great improve to the methods tried previously.

A simulated FIR DAC response in the 802.11ad mode is shown in Figure 5.11. The coefficients of the 802.11ad filter are quantized to 6-bit and they are compared with the ideal coefficients, shown with 16-bit quantization. As can be seen, the output of the FIR DAC respects the spectrum mask requirements with a large margin.

802.11ac Mode

The delta-sigma modulator coefficients can be reconfigured for each mode of the 802.11ac. It operates with the OSR values shown in Table 5.2. The purpose of the FIR DAC transfer function is to cancel the high pass noise shape coming from the delta-sigma modulator. A single filter transfer function can be used for 20 MHz, 40 MHz, and 80 MHz modes and still fulfill the transmit mask requirements of each of the three modes.

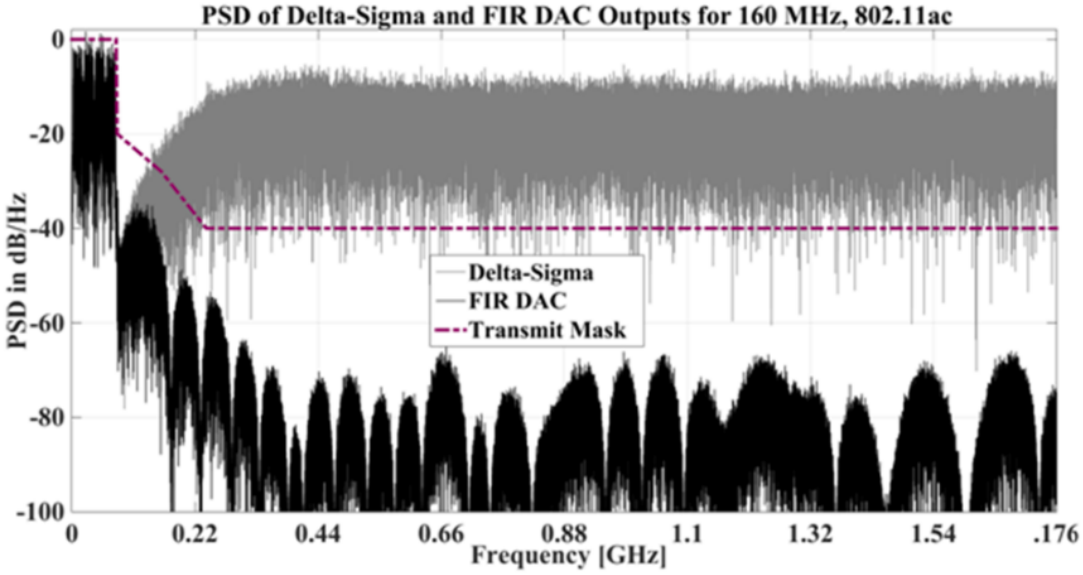


Figure 5.12: The FIR DAC filter roll-off cancels the rising quantization noise from the ΔΣ-modulator output in the 160MHz mode of the 802.11ac

For the 160 MHz mode, a different filter is designed. The main reason is the clipping of the subcarriers at the edge of the passband corrupts the EVM when a lower cut-off frequency is used. When the 160 MHz filter is used for the other lower channel bandwidth modes, the quantization noise raises above the transmit mask before it is canceled by the FIR DAC.

A 60 dBr stopband rejection is required of the 160 MHz filter. This requirement applies only at the

frequencies where transmit mask plateaus ($\frac{3}{2}f_s$ in Figure 5.1a). For frequencies before $\frac{3}{2}f_s$, the filter need only cancel the delta-sigma modulator shaped noise to less than the mask requirements. To take advantage of this fact, the filters are designed based on an equiripple method with decaying stopband. It has the advantage from equiripple method of having low ripple passband. A stopband that decays by $\frac{1}{f^N}$ avoids the problem of using a long equiripple filter to address the stopband requirements that exist at $\frac{3}{2}f_s$ but not necessarily earlier frequencies. The passband ripple is set to less than 0.5 dB, the filter order is 63 in both the 160 MHz and the combined 20 MHz, 40 MHz and 80 MHz modes. Since the filters has symmetrical impulse response, they have linear phase responses.

The response of the FIR DAC and the delta-sigma modulator in the 160 MHz mode of the 802.11ac are shown in Figure 5.12. It can be seen that the rising quantization noise at the output of the modulator is canceled by the decaying stopband of the FIR DAC response to less than the requirements of the transmit mask. The margin between the stopband and the transmit mask is large because the stopband rejection value is designed considering standard coexistence.

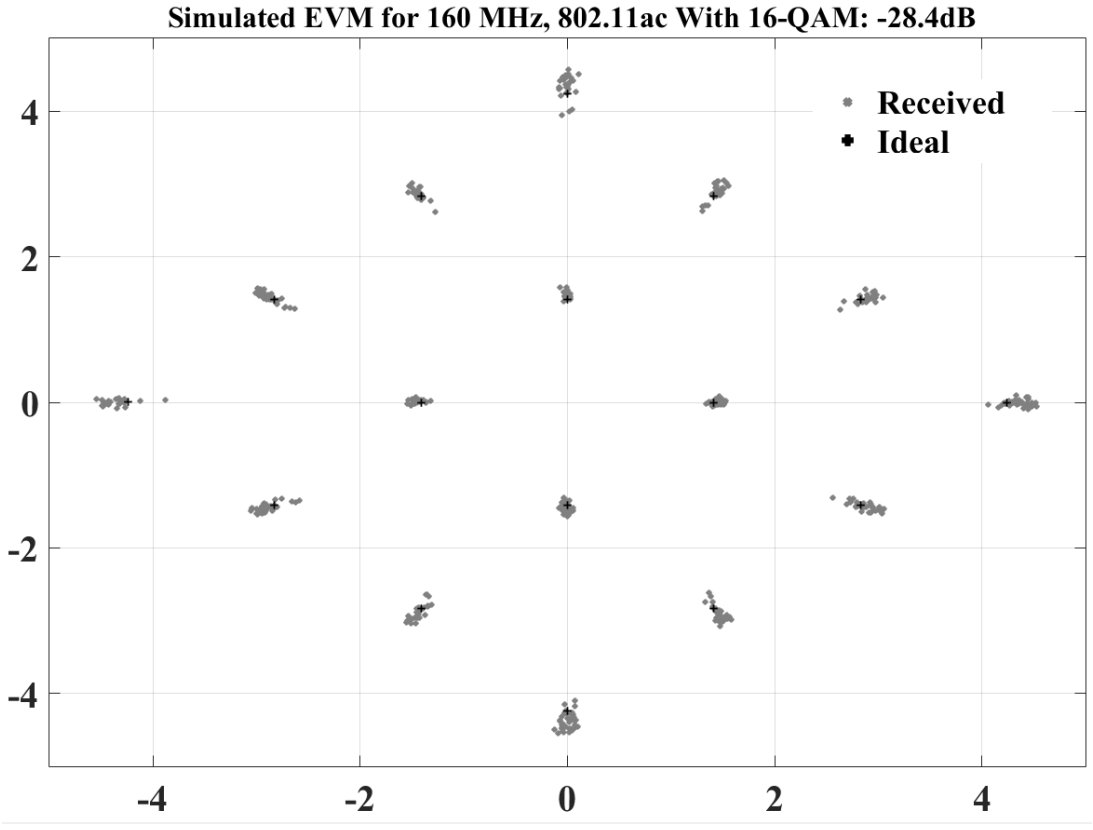


Figure 5.13: Simulated EVM with 16-QAM modulation in the 160MHz mode of the 802.11ac

The EVM of the 160 MHz 802.11ac mode FIR DAC was simulated using Matlab®, and the result for 16-QAM is shown in Figure 5.13. The results compared with the standard requirement leaves a

12dB margin for the subsequent analog blocks of the transmitter. The results for the other modes of the 802.11ac is in [GFK16a]. The EVM simulation method is discussed in Appendix-2.

5.3 From Transfer Function to Circuit Parameters

A configurable FIR DAC is implemented for the 160 MHz 802.11ac and the 802.11ad modes. The circuit level discussions are the subject of Chapter 6. In this section, the system level results obtained are further developed in order to arrive at a thorough multi-standard FIR DAC specification. The discussion include filter coefficient quantization, and choices concerning the FIR DAC performance along the lines of the discussion in Chapter 4.

5.3.1 Coefficient Quantization

The designed 16^{th}-order 802.11ad filter transfer function with ideal and finite coefficient resolutions is shown in Figure 5.11. Filters with arbitrary valued coefficients are prone to process gradient mismatches, require custom design and layout of coefficients, and have large current source count. Coefficient quantization simplifies the design and allows flexible reconfiguration. Nonetheless, coefficient quantization limits the achievable stopband attenuation level of the filter. The coefficients are quantized to 6-bit. It is interesting to see the degradation due to quantization effects. In the 802.11ad standard, the adjacent channel starts at an offset of 1.22 GHz from the channel center. Quantization with less than 6-bit introduces leakage of up to 15 dB [GFK15].

The 20/40/80 MHz mode of the 802.11ac filter design benefits from a higher SNR resulting from the higher OSR of the respective bandwidths at the $\Delta\Sigma$ modulator. Hence, 6-bit quantized coefficients meet the requirements of each mode associated with this filter. For the 160-MHz coefficient set, a ratio of 2^8 exists between the biggest center tap coefficient and the smallest. This is done to reach a higher stopband rejection. This ratio, also called coefficient spread, becomes 2^6 for the 802.11ad and the 20/40/80-MHz cases. Figure 5.15a has the quantized coefficient transfer functions in one plot.

5.3.2 Multi-standard FIR DAC Specifications

As discussed in Chapter 4, the standard deviation of coefficient mismatch can be set to the maximum tolerable stopband value of the transfer function. In the 160 MHz 802.11ac mode, the coefficient values were simulated with a 1.7% standard deviation, and the resulting transfer function is in Figure 5.14. The simulation assumed all the unit elements realizing a coefficient have an independent Gaussian mismatch as discussed in Chapter 4.

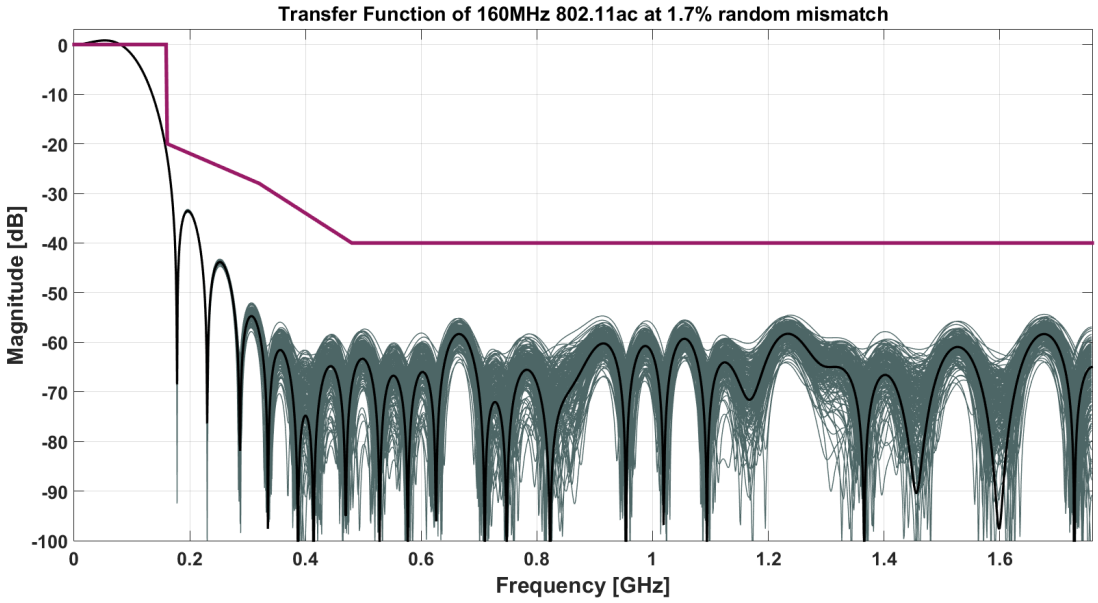
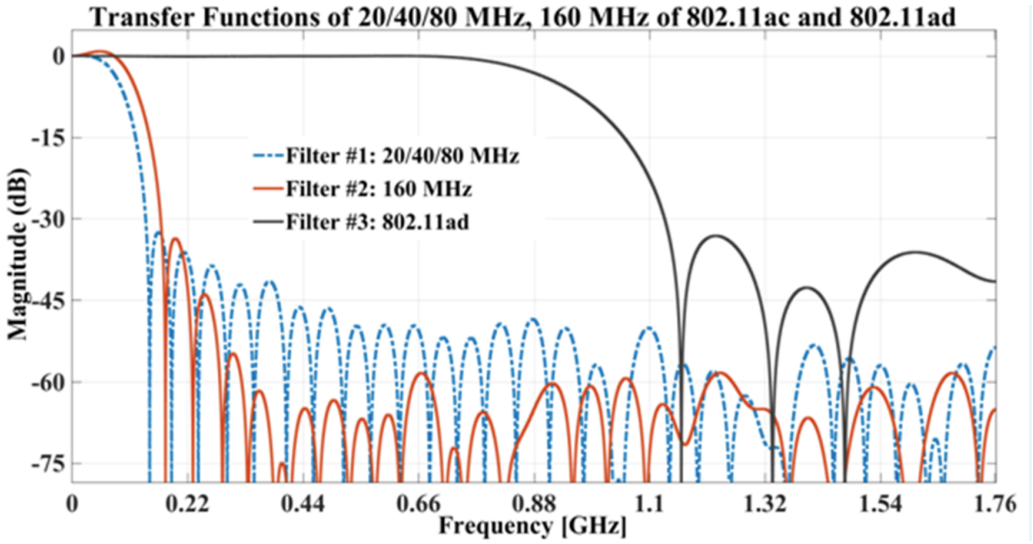


Figure 5.14: The transfer function of the 160MHz of the 802.11ac mode with a unit coefficient mismatch of 1.7% standard deviation.

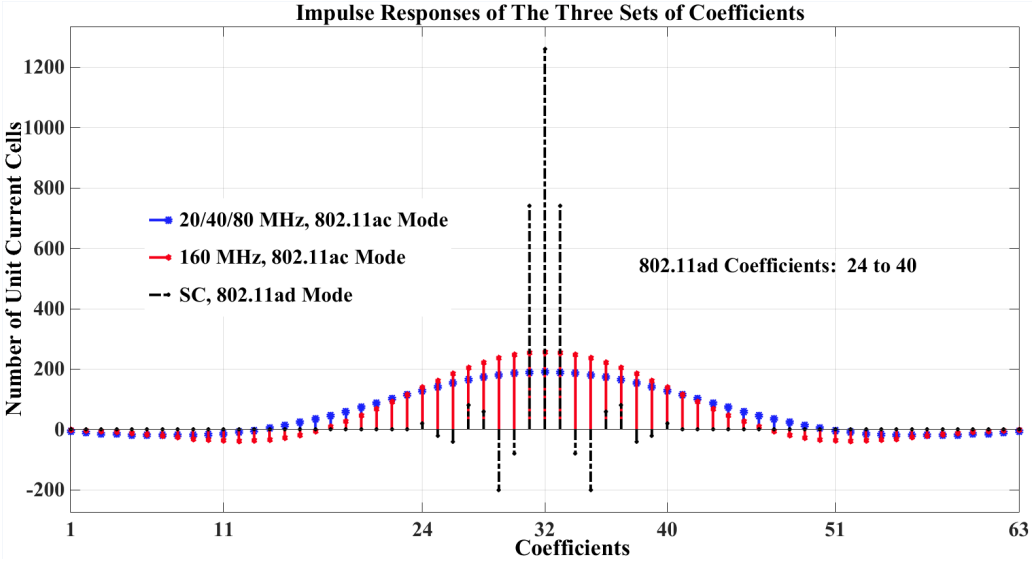
A 1.7% standard deviation introduces almost 3dB increase from the maximum stopband level desired. While it is possible to go further with smaller mismatch requirement, it comes at the cost of area of the current source transistor implementing a coefficient. This is, then, the first design choice to be made when proceeding to FIR DAC implementation.

To implement the two quantized coefficients, those of 160 MHz 802.11ac and 802.11ad, in one FIR DAC circuit, one set of coefficients must be represented by the other. Since the 802.11ac mode has the highest mismatch requirement, the 802.11ad coefficients has to be constructed from it. The 802.11ac coefficients are composed of unit elements, as in unary implementation, with specified mismatch requirements. Then the 802.11ad coefficients has to be integer multiples of these unit coefficients so that they will be constructed using simple analog circuit addition and subtraction. It is important to mention that when each set of coefficients are quantized, each coefficient of a particular set is represented as an integer multiple of a unit coefficient of that coefficient set. Therefore, it should be understood that the 802.11ac and 802.11ad coefficients are quantized by 8-bit and 6-bit, respectively, and their center taps would be 2^8 and 2^6 times the unit coefficients respectively.

The choice of ratio between one set of coefficient and another of a configurable FIR DAC circuit can be made by equating the DC-sum of their coefficients. It is as if equating the full-scale current, in a current steering implementation, of the two coefficient sets. The original sum of the 802.11ad coefficients is 187 11ad-unit coefficients and those of 160 MHz 802.11ac are 4974 11ac-unit coefficients. A ratio of



(a)



(b)

Figure 5.15: The transfer functions and impulse responses of the 20/40/80 MHz, 160 MHz of the 802.11ac and the LP SC 802.11ad mode. The samples in the impulse responses are scaled according to the number of unit coefficient elements required to implement each coefficient.

twenty between the two unit coefficients results in 3740 11ac-unit coefficients for 802.11ad mode, and 4974 11ac-unit coefficients for the 802.11ac mode. Therefore, a maximum of 3740 unit coefficients can be shared between the two modes. Figure 5.15b illustrates the coefficients values relative to the unit coefficients of the combined multi-standard FIR DAC.

All the coefficients of the 802.11ad mode may not be obtained by addition and subtraction of the 802.11ac coefficients. In this case, some unit coefficients are added for fine-tuning the sums or difference

‡ I_{unit} is unit coefficient current § Current-Steering Architecture Assumed

Table 5.3: Summary of the specifications of the multi-standard FIR DAC

Parameter	802.11ac mode	802.11ad mode
Clock Speed	f_s	f_s
Bandwidth	$\frac{f_s}{22}$	$\frac{f_s}{2}$
Unit Coefficient Mismatch, σ_u	1.7%	1.7%
Coefficient Spread	2^8	2^6
Load Resistance §	R_{load}	R_{load}
Full-Scale Swing ‡	$4974 I_{unit} R_{load}$	$3804 I_{unit} R_{load}$
Number of UCC Only in	1246	76
Number of UCC Shared	98% of 802.11ad used in 802.11ac	

to make them equal to the actual 802.11ad values.

The specifications of the multi-standard FIR DAC are summarized in Table 5.3. The parameters can used as a starting point of a multi-standard FIR DAC circuit design. Clearly, the FIR DAC has a single sample rate for the two modes. However, the bandwidth of the 802.11ac mode is smaller than the 802.11ad mode. However, the stringent mismatch requirement in the 802.11ac mode is consisent with the requried higher stopband rejection in this mode. The output of the two modes are taken at the same nodes. Their load resistors are also the same. Only their output swing is scaled according to their number of unit coefficients.

5.4 Summary and Conclusions

In this chapter, a multi-standard transmitter architecture based on a LPF FIR DAC structure is validated on system level. The specific parametric values for each DSP block of each mode of the transmitter are presented. Further, the response of each block for an 160 MHz OFDM signal are included.

The multi-mode FIR DAC specification that is developed at the end of the chapter will be an input to the next chapter. The coefficients of the multi-mode FIR DAC implemented in Chapter 6 will be the same as those discussed in this chapter. However, a high pass FIR DAC delay line is used for implementation of the circuit. The transistor level implementation of the FIR DAC depends on the coefficient values developed here in this chapter.

Chapter 6

Design and Implementation of A Configurable Transmitter Baseband in CMOS 28nm FDSOI

The configurable semi-digital FIR DAC part of the proposed transmitter baseband architecture was fabricated using STMicroelectronics CMOS 28nm FDSOI. In the previous chapter, the discussion was mainly system level validation using MATLAB® based simulation results. In this chapter, transistor level discussions of the circuits used for implementing the explained system, and some layout related issues are explored.

It starts from the a brief introduction of the specification drawn in the previous chapter for the configurable FIR DAC. While the implementation is based on the direct form FIR filter structure discussed, there are some challenges in placement of UCCs. The placement method followed in the implementation of the FIR DAC chip is explained by comparing it to those in traditional multi-bit DACs. Part of this discussion is also part of a published work in [GFK16b]. The next section explores circuit blocks of the implemented chip. A brief discussion of circuit operation, design, and layout related issues is included.

6.1 From System Level to Floorplan

The FIR DAC works in two modes. The 802.11ac mode, which from now on refers to the 160 MHz channel bandwidth, and the LPSC 802.11ad. The impulse responses of these two modes are presented in Chapter 5. The 802.11ac mode has 63 coefficients with 8-bit quantization, and the 802.11ad mode has 17 coefficients with 6-bit quantization. The direct-form FIR filter structure discussed in Chapter 4 is used to implement both impulse responses. In this section, the changes to the normal FIR structure when it is operating in the two standards is explained. The explanation is based on Figure 6.1.

There are 63 delay cells as is expected in the 802.11ac mode. The output of these delay cells are taken to drive the UCCs. The total number of UCCs are placed as one current source and an indication

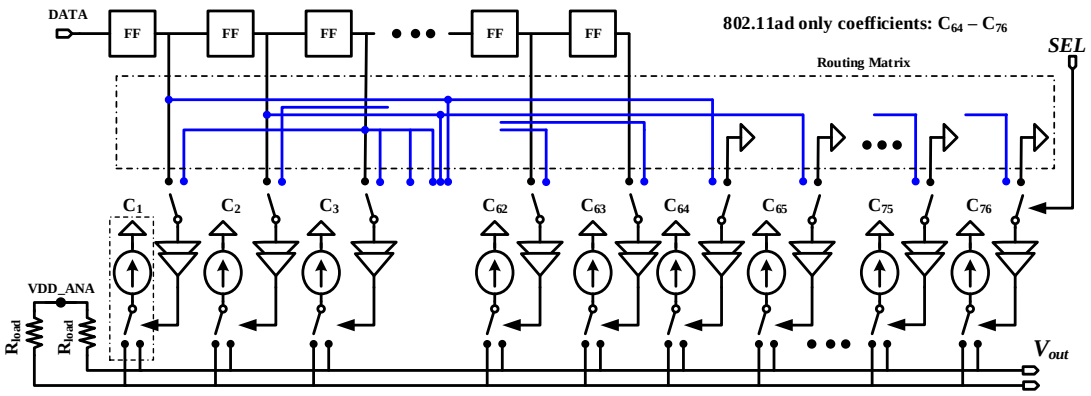


Figure 6.1: FIR DAC block diagram

of their values is placed using their coefficient number ($C_1 to C_{63}$). In the 802.11ac mode, coefficients $C_{64} to C_{76}$ does not contribute to the output.

In the 802.11ad mode, the mode selection signal, SEL, switches the input of the drivers to the second input, in blue in Figure 6.1. All of these inputs are taken from the outputs of the first 17 delay cells. This is consistent with the length of the 802.11ad impulse response. Some of the 17 outputs of the first 17 delay cells are inputs to more than one driver. In other words, that particular tap is driving the sum of the 802.11ac coefficients which correspond to all the drivers connected to that tap. The *RoutingMatrix* is discussed later in the next section. Coefficients $C_{64} to C_{76}$ are small valued coefficients which are added to the summed coefficients of the 17 taps to arrive at the exact coefficient values of the 802.11ad.

6.2 Mismatch Errors and Layout Floorplan

FIR DAC performance is highly dependent on the accuracy of its coefficients. Coefficient accuracy is in turn dependent on the absolute and relative accuracy of the method used to implement the coefficient. For example, the FIR DAC is realized using a current-steering DAC structure where current sources are used for implementing the coefficients. Accuracy, in this case, depends on the random errors that are independently defined by the characteristics of the current source implementing a particular coefficient; and the systematic errors across the array of current sources which contribute a relativistic inaccuracy to that particular coefficient.

MOS transistor mismatch errors are classified as random errors and systematic errors. Random errors are uncorrelated errors that are specific to a particular device. They are defined by technological constants, the area a device occupies and the biasing conditions [Pel+89]. The systematic errors are a combination of first order linear errors and higher order errors. The linear errors are caused mainly by

IR drop along a ground line, oxide thickness gradients, doping gradients; and the main contributors to the higher order errors are thermal gradients, oxide stress, etc [CG00]. It can be understood that the systematic errors are there because of the distance between two or more devices. There is a short enough distance at which the systematic errors are insignificant; or their values are less than the random errors and can be neglected. One design strategy is, then, to make the systematic errors smaller than the random errors regardless of distance.

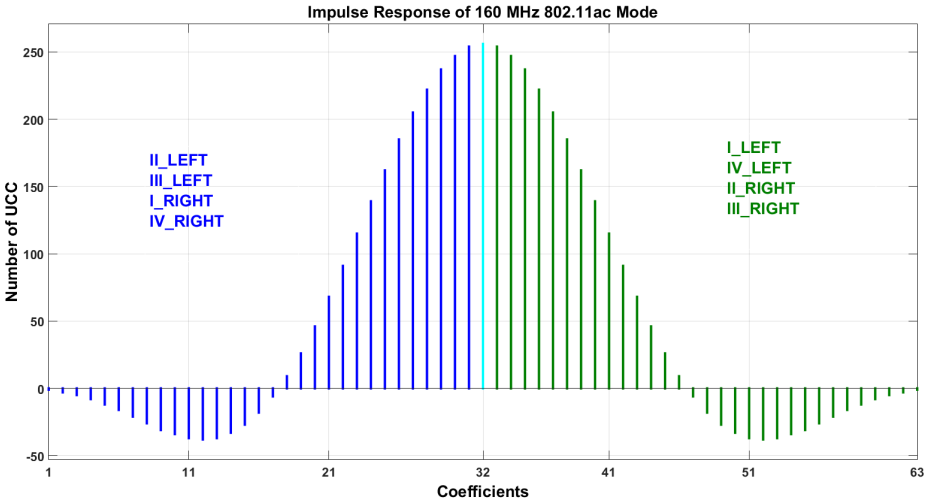
The random errors can be tackled by sizing the area of the current sources according to the standard deviation required. The bigger a MOS transistor is the lower its random mismatch errors. However, this contributes to the systematic mismatch errors by making the chip large. Some of the systematic errors such as the IR drop along the ground line can be minimized by using power and ground distribution grid for the chip and wide ground lines. However, for large number of devices this results in a significant increase in the total area of the chip. A more effective solution is to place the devices in an array and target the mismatch errors with a systematic placement or switching scheme that results in the cancellation of gradients effects and minimization of higher order errors. This is the solution used in many high resolution current-steering DAC implementation [BSS04]. Unfortunately, this solution is not effective for a current-steering FIR DAC with long filter lengths.

6.2.1 Pseudo-Double Centroid Placement Method

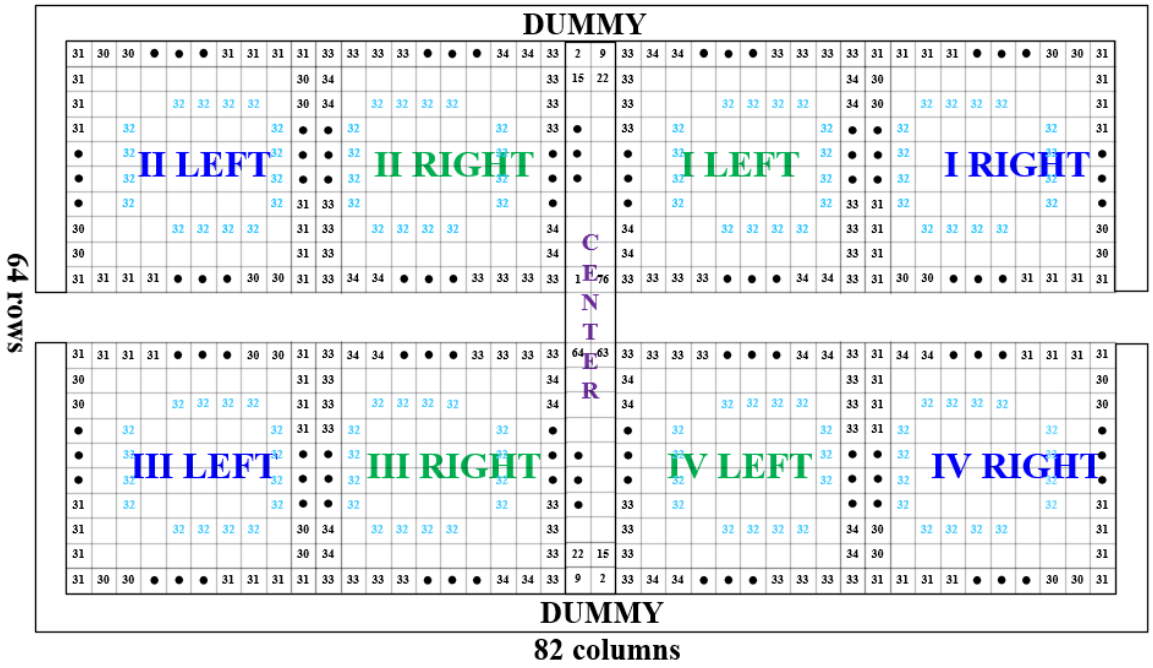
Unit current cell layout in many high resolution DACs is divided into two or, maybe three, transistor array blocks. The switching parts are placed in one array and the current source transistors in a different array [BSS04]. Some of the reasons are the following: to minimize the current source array area, to separate the switching and the current source devices, reduce wiring capacitance between switch and cascode transistors [PS10].

One reason that makes the adoption of the aforementioned method possible is the symmetrical power of two weights present in a conventional multi-bit DAC. Since weights are implemented by scaling the width of the current source transistor, total current is divided evenly into each current source transistor. The errors that occur due to distance can be dealt with effectively if the current source elements are placed in one array. If some of the weights were not power of two, each current source transistor element would carry different current. Error reduction mechanisms such as switching schemes would not be effective. If the non-power-of-two weights are few, they can be implemented as lumped elements. Dummy elements can be used to compensate for any spatial asymmetry that results. However, if all the weights are random, non-power-of-two, dummy elements are the solution.

Another enabling reason for the adoption of that method is because of the relatively reduced number



(a)



(b)

Figure 6.2: A Pseudo double common-centroid placement for UCC fo FIR DAC coefficients. The blue shaded coefficients in the left of the impulse response are placed in the outer sections of each quadrant, and those in green inside. The unmatched center tap is placed in all quadrants.

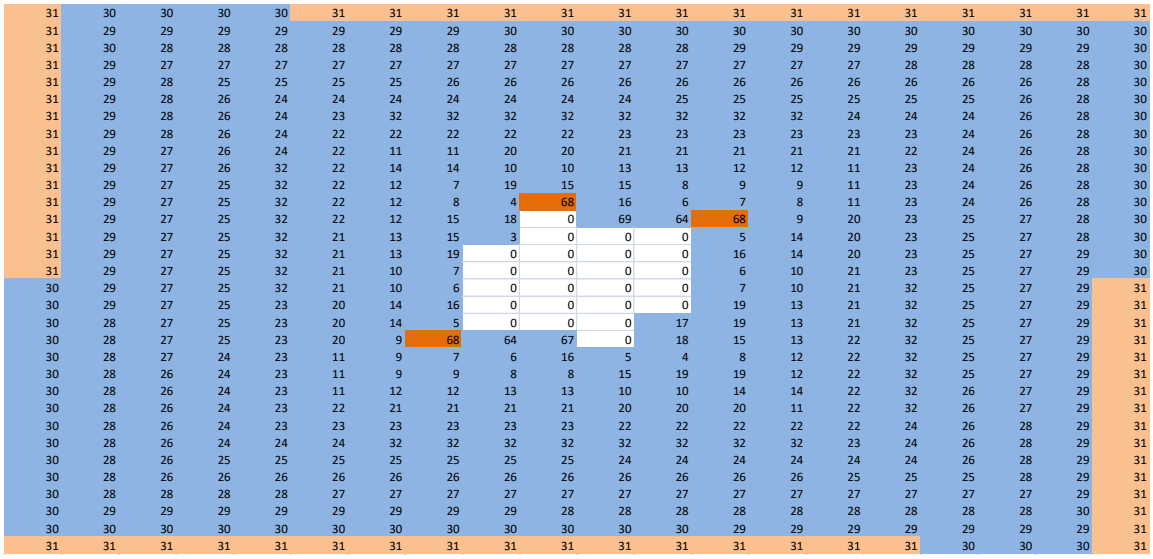
of routing required from the switch array block to the current source array block. For instance, an 8-6 segmented 14-bit DAC has 255x16 unit current sources in unary implementation [Van+99]. These number of current sources are close to those number of unit current cells, 4974, that could have implemented the 802.11ac mode in this FIR DAC. Here, an assumption is made that the smallest coefficient of the FIR DAC is not divided into power of two units. Otherwise, the number of unit current source transistors

would be 4974x16. In the example, the distinct number of signals routed from the switch array block to the current source array are only eight. This reduced number allows for employing a switching scheme where the current sources that share the same routing signal can be dispersed as desired. Nonetheless, in the FIR DAC case, this number would have been 63—equal to the number of filter taps. If the current sources are as dispered as a particular switching scheme may demand them to be, then the complexity and speed penalities corresponding to routing 63 signals from a switch array block to a current source array block would be immense. To put it in perspective, if a 64x68 matrix is used for the current source array as the switching scheme in this example [Dev+04], twelve out of the 63 coefficients of the 802.11ac would have one unit current source in each column and also in each row. That is there would have been at least twelve interconnects in each column since there are twelve coefficients whose values are greater than or equal to 68. The amount of parasitic capacitance mainly due to sidewall capacitance between parallel routing metals would significantly affect the output impedance of those current sources, Equation (4.21) in Chapter 4. Therefore, the idea of placing the current sources in a block separate from the switching blocks was dropped.

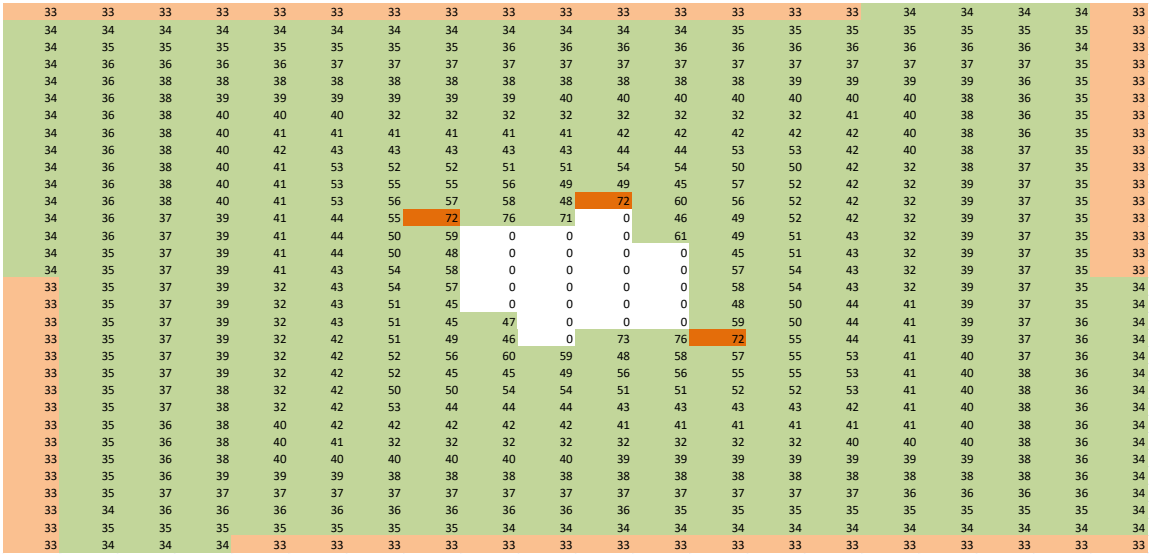
To target high speed operation, the placement method for FIR DAC has to be such that the whole unit current cell is placed as if it was a unit current source transistor. The unit current cell, also UCC, contains the digital latch and analog current source that implements a unit coefficient. The unit coefficient is a value which can be combined to arrive at all other coefficients only using addition or subtraction. In a placement method where the UCC is placed as one unit element in an array, the analog signals within one UCC are routed short distance. The only analog signals which will be routed long distance are the output signals of the FIR DAC. Digital signals from the drivers to the UCC are routed vertically or horizontally, but long distance. Now instead of long distance routing of current source analog signals, it is digital signals that drive the switches which will be routed long distance.

The only problem to high speed operation with this placement method increased time constant due to parasitic capacitance and wire resistance. The digital signals are routed in parallel in the array, so resulting parasitic capacitance between them contributes to increase of time constant and signal may be degraded due to crosstalk. These problems can be tackled with careful choice of metals, shielding and wire sizing.

Other placement methods which were explored to be utilized for FIR DACs are those that are used in switched-capacitor filters. These filters have capacitors whose ratios are random, not power of two as traditional multi-bit DAC weights. The switched capacitor filters can also be long. These characteristics of switched-capacitor filters makes their placement method interesting enough for adoption in FIR DACs. There are many placement methods that are designed for capacitor arrays where linear and quadratic mismatch errors are cancelled even when the values of the capacitors and their ratios are random [SP15].



(a)



(b)

Figure 6.3: The placement of the UCCs in **II_LEFT** and **II_RIGHT** of the UCC array. Two coefficients, C_{31} and C_{33}, equidistant from the center tap, C_{32}, of the 802.11ac impulse response are highlighted. Two fine-tuning 802.11ad only coefficients, C_{68} and C_{72}, are also highlighted. They are also equidistant from the center tap, C_{70}, of the fine-tuning coefficient set.

Nevertheless, the main limitation in adopting these techniques to FIR DAC implementation is the fact that a UCC has nine terminals that has to be routed, unlike two for unit capacitors. Thus, randomly dispersing the UCCs as per the capacitor array placement method dictates does not work. Therefore, a more simpler placement method based on centroid scheme was employed.

A big contribution to systematic errors comes from the first two orders — linear and quadratic.

If the diagonals of the device array are assumed to be aligned with the axes of the systematic errors, mathematically, the errors for a device implemented as one unit can be expressed as follows:

$$\epsilon(x,y) = \epsilon_{lin}(x,y) + \epsilon_{quad}(x,y) \tag{6.1}$$

$$\epsilon_{lin}(x,y) = k_{l,x}x + k_{l,y}y \tag{6.2}$$

$$\epsilon_{quad}(x,y) = k_{q,x}(x^2) + k_{q,y}(y^2) \tag{6.3}$$

$$k_q = k_{q,x}cos(\theta), \quad and \quad k_q = k_{q,y}sin(\theta) \tag{6.4}$$

k_x and k_y are gradient error constants in the x and y directions respectively, and $k_{q,x}$ and $k_{q,y}$ are constant in the x and y directions of the quadratic error, and θ is the angle the axes of the error makes with the x-axis.

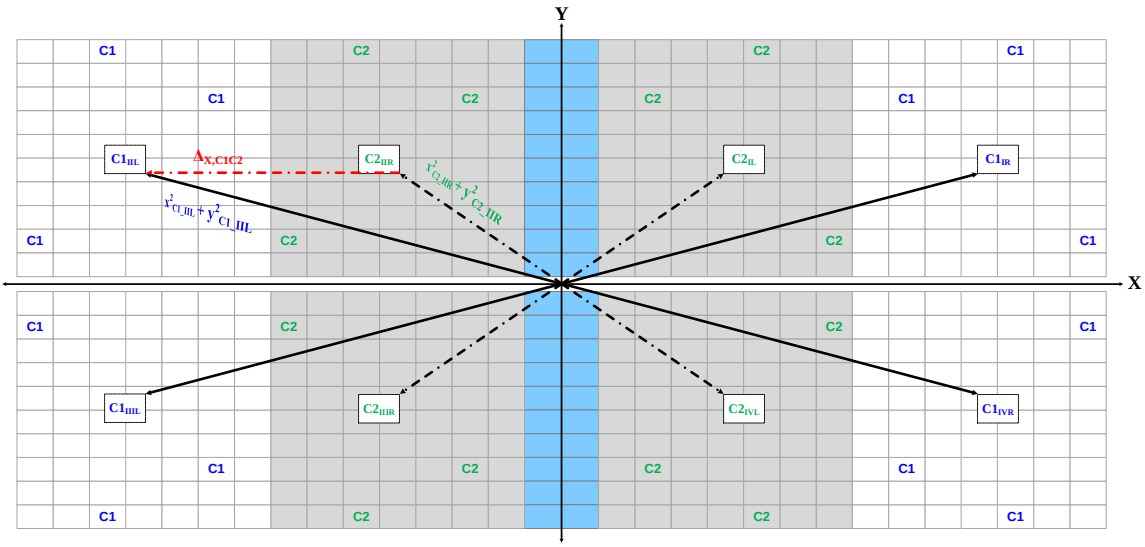


Figure 6.4: Systematic error differences between even valued coefficients left and right of the center tap

In a common-centroid scheme, one device is divided in four units which are placed in each quadrant. Clearly, the linear errors of the device are canceled, but not the quadratic errors. The strategy is to equalize the quadratic errors of all the devices. The best strategy for that is double common-centroid as shown in Figure 6.2. In this scheme, all the devices with more than four unit elements have at least one unit element in each quadrant. For those that have a multiple of four, the quotient are placed in each quadrant in a common-centroid scheme around the center of each quadrant, and the remainder in the center of the UCC array. The units elements of the devices with less than four unit elements including the remainders of those devices represented by more than four units are placed symmetrically around the center of UCC array, i.e. in the **CENTER**. This scheme approximates the net quadratic error of each device to be equal to the value if the devices were placed as a single device at the center each quadrant.

Let N_i be the number of UCCs required to implement a coefficient C_i, where $1 \leqslant i \leqslant N_{tap}$, and N_{tap} is the number of taps of the filter.

$$N_i = 4Q_i + R_i \tag{6.5}$$

Q_i are number of UCCs of C_i placed in each quadrant, and R_i are placed in the **CENTER** of the UCC array. Q_i of each quadrant are placed in a common-centroid configuration within that quadrant.

Since the impulse response is symmetrical about the center coefficient, the UCCs that belong to the coefficients that are in the left of the impluse response, in Figure 6.2, are placed in the left parts of each quadrant. Those in the right are mirrored horizontally from those in the left. Quadrant-I is quadrant-II mirrored horizontally, and quadrants III and IV are copied from II and I by mirroring them vertically. The center coefficients of this odd-numbered impulse response appears in all quadrants in both **LEFT** and **RIGHT**. Because of the fact that the placement in each quadrant is not strictly common-centroid, it is called pseudo double common-centroid. A more thorough common-centroid placement method could be used for the Q_is in each quadrant using methods reported in [SP15]. However, since coefficients with units in one quadrant have also units in other quadrants, the linear parts of their systematic errors are generally canceled. Moreover, the other placement methods come with additional costs in routing area and complexity.

The linear and quadratic components of the systematic errors are reduced by this method. For coefficients that has $Q_i \geqslant 4$, the center of their net quadratic error will be at each section of the quadrant. For example, quadratic errors for two hypothetical coefficients, C_1 and C_2, with 12 UCCs each in the four quadrants of the UCC array and positioned as the coefficients C_{68} and C_{72} are shown in Figure 6.4. The figure is scaled with focus on the center of each quadrant so that it fits the page with good visibility. The axis of the quadratic error are assumed to be aligned with the X and Y axis. The three UCCs of C_1 and C_2 in each quadrant have a quadratic error of:

$$\epsilon_{quad,C1,i} = k_q(x^2_{C1,i} + y^2_{C1,i}) \tag{6.6}$$

$$\epsilon_{quad,C2,i} = k_{q,x}(x^2_{C2,i} + k_{q,y}y^2_{C2,i}) \tag{6.7}$$

and the total error for C_1 and C_2 in all the four quadrants can approximated as:

$$\epsilon_{quad,C1} \approx 4\Big(3(k_{q,x}x^2_{C1,IIL} + k_{q,y}y^2_{C1,IIL})\Big) \tag{6.8}$$

$$\epsilon_{quad,C2} \approx 4\Big(3(k_{q,x}x^2_{C2,IIR} + k_{q,y}y^2_{C2,IIR})\Big) \tag{6.9}$$

Thus, the net resultant quadratic error for a coefficient is proportional to the distance between the center of a section of a quadrant and the center of the array. This creates a difference between the

coefficients in the right side of the impulse response and those in the left as those in the right are placed near the center. For C_1 and C_2, this difference can approximated as:

$$\epsilon_{quad,C1} \approx 4\Big(3\big(k_{q,x}\Delta^2_{X,C1C2}\big)\Big) \tag{6.10}$$

Besides, there is also quadratic error difference between coefficients with $Q_i \geqslant 4$ and the small-valued coefficients that has $Q_i < 4$. The latter has all their UCCs in the **CENTER**, so their quadratic error is expected to be relatively much smaller. Besides, those coefficients that are around the center of the impulse response have the highest because of they are implemented with higher number of UCCs. For example, the quadratic error difference between the coefficients C_1 and C_2 and the coefficients C_{31} and C_{33} highlighted in Figure 6.3 can be approximated as:

$$\epsilon_{quad,C1C31} \approx 4\Big(k_{q,x}(63x^2_{C1,IIL} - 3x^2_{C31,IIL}) + k_{q,y}(63y^2_{C1,IIL} - 3y^2_{C31,IIL})\Big) \tag{6.11}$$

$$\epsilon_{quad,C2C33} \approx 4\Big(k_{q,x}(63x^2_{C2,IIR} - 3x^2_{C33,IIR}) + k_{q,y}(63y^2_{C2,IIR} - 3y^2_{C33,IIR})\Big) \tag{6.12}$$

This estimate can be used in the design of the UCC. The effect of the error on the transfer function can be simulated by incorporating this relative error in to the value of each coefficient. Since each coefficient experience different error magnitude, it is preferable to simulate the transfer function with this non-uniform error distribution. However, it is also possible to design the UCCs for a random error which is large enough to accommodate the quadratic error.

One advantage of the placement method is, then, to distribute the UCCs of the highest coefficients around each quadrant so that the cumulative quadratic error of a big coefficient is a sum of the errors that belong to the UCCs near the center of the array, this error is relatively close to zero, and those far away from the center of the quadrant. This way the total sum is reduced.

This advantage is obtained while still canceling the major contributor of the systematic errors—the linear part. The fact that the UCCs of a coefficient are distributed around the array is also a positive feature of this method.

6.2.2 Layout Floorplan

The layout floorplan of the FIR DAC is shown in Figure 6.5. The single bit input data pass vertically to the UCC array, the clock is supplied horizontally from the left using a clock tree and the outputs are summed with a similar output tree in the right. The digital **Delay Line** outputs are fed to the **Routing Matrix** which is a matrix of interconnects that enables the UCCs to be driven by the digital data outputs from one or more taps of the delay line. The routed matrix of interconnects are inputs to the **Mode Selection**

block which basically selects the data out of the delay line. This is done using a mode selection SEL input. The **DATA DRIVERS** are inserted to compensate for the speed degradation that may result from routing the data to the latches in the UCC array. At the center is the UCC array where the UCCs of the coefficients are placed according to the method discussed in subsection 6.2.1. At the center of the UCC array are the biasing circuits for each section of the four quadrants. The biasing circuits are divided into two parts—**Global** and **Local**. The **Global** circuits at the center of the the chip (**GCM** block) mirror the input reference current and are supplied with a separate voltage supply. The supply, VDD_BIAS and the reference current are fed to chip from the bottom side as shown in Figure 6.5 and 6.7.

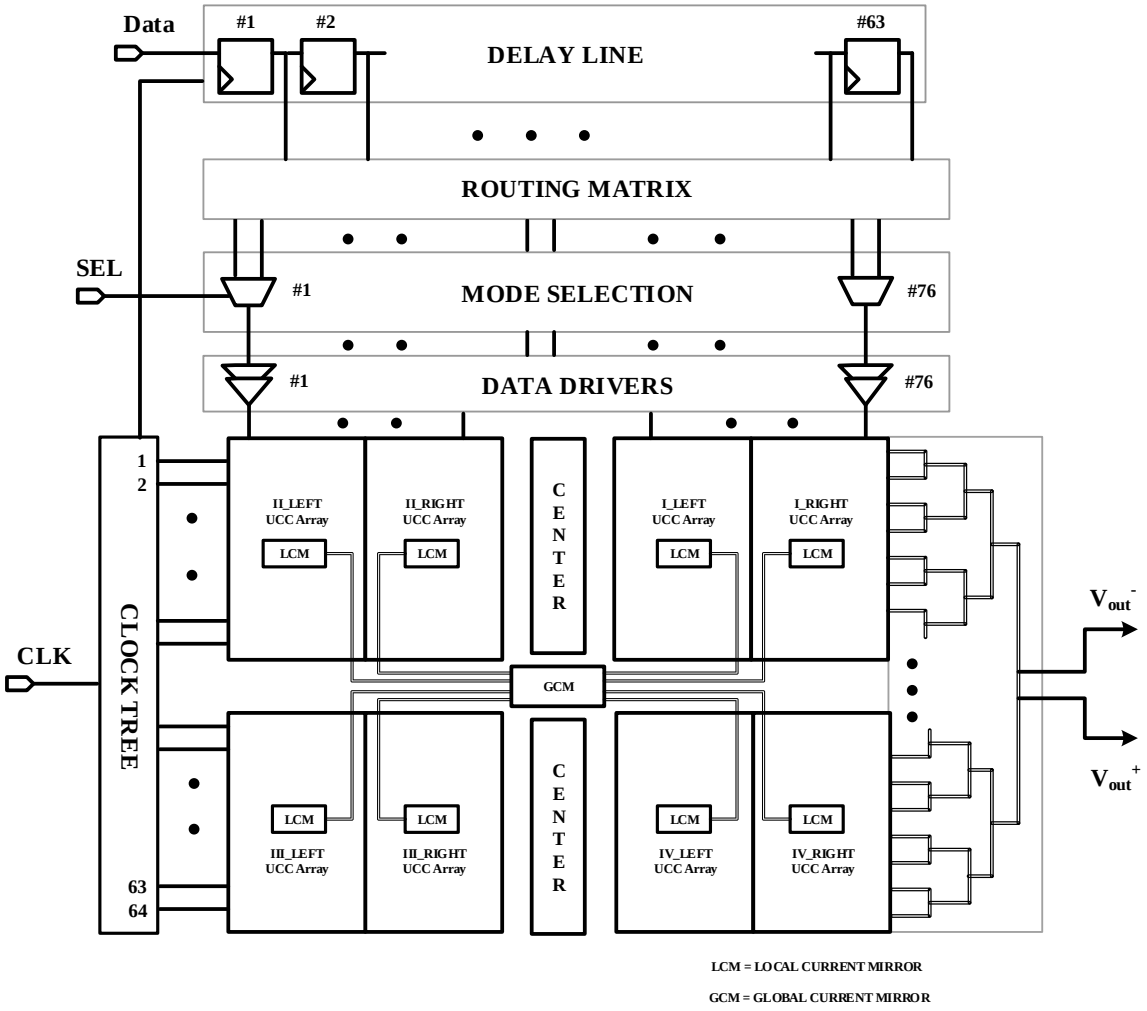


Figure 6.5: FIR DAC floorplan. The current mirrors are local and global—LCM and GCM. The data is propagated from the top starting from 63-flip-flop delay line, to 76-multiplexers mode selection, then to 76 drivers. The clock tree has 64-rows and the output is obtained from differential outputs of a 64-row tree.

There is a common supply voltage, VDD_{DIG}, to all circuits except the biasing circuits. The supply to

the biasing circuits is VDD_{BIAS}, and the reasons for this are explained in 6.3.7. The common VDD_{DIG} is routed along with the ground line using a distribution grid. The grid lines pass through each one of the 64 rows and 82 columns of the UCC array. This density is maintained also on the clock tree, and vertically up to the *DelayLine*. The empty space outside the circuit blocks is filled with decoupling capacitors.

In the UCC array, two high speed analog outputs, power and ground lines, high speed digital clock and data lines, an asynchronous mode selection signal, and two current mirror biases are routed—a total of nine distinct signals. The clock is routed using thick top metal in one side, and the two outputs and two bias current signals in the other side of the UCC. The data lines are propagated vertically on one side and the mode selection SEL signal on the other as shown in Figure 6.20.

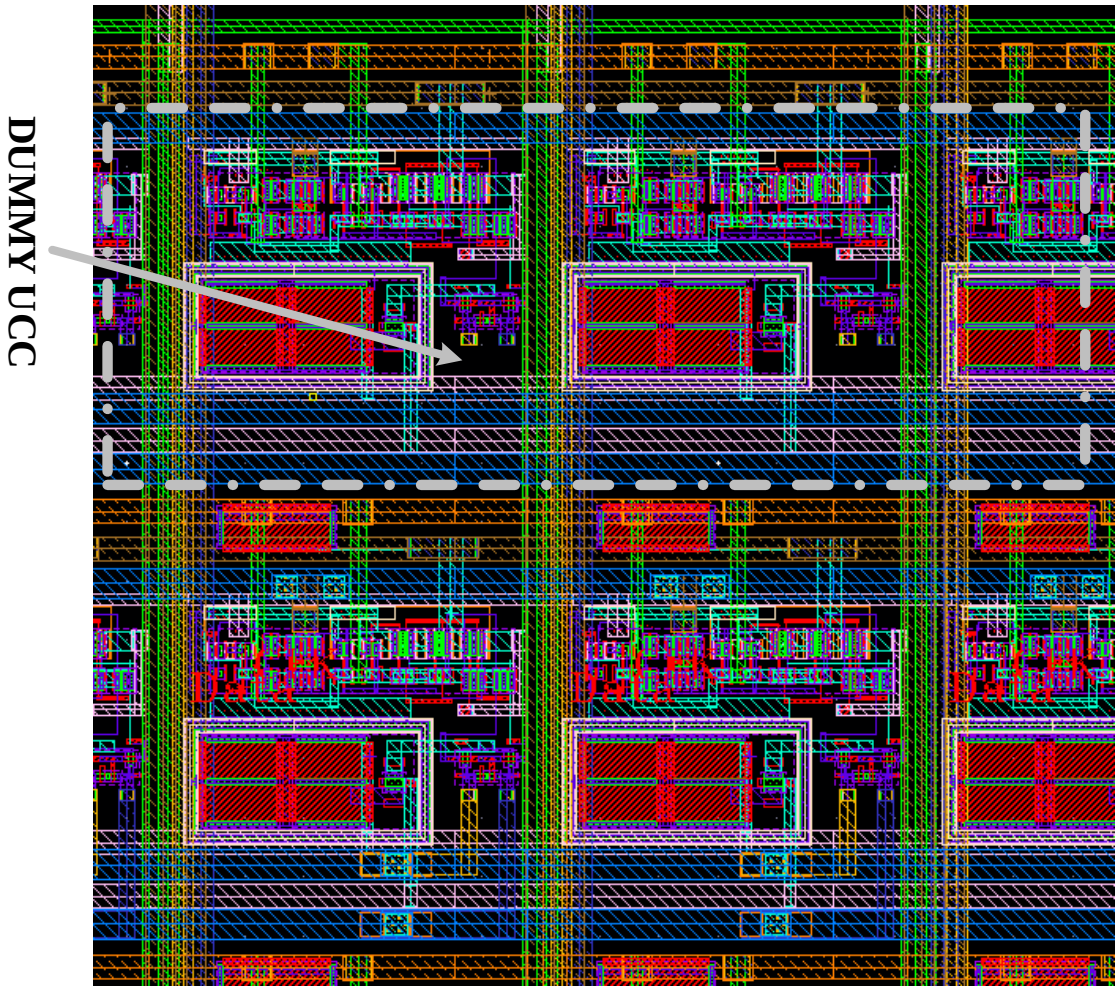


Figure 6.6: A section of the UCC array. Dummy UCCs surround the edge of the array as shown. The data, clock, output, bias and select signal lines of the UCC are routed such that the array area is exactly the sum of the areas of the UCCs.

Design rules require for some distance between power and ground lines. A decoupling capacitor is

placed in this gap to stabilize the supply voltage on each UCC. There are six UCC layout variants. They are those that are turned-on only in 802.11ac, only in 802.11ad and those that are shared. To keep the global UCC array structure stable, positive and negative coefficient variants are prepared for each of the three UCC types mentioned.

The mode selection SEL signal was optimized to turn-off the UCC if it is not operating in the selected mode. The SEL signal is also used to: select data inputs in the multiplexers of the mode selection block, set the input of the non-selected multiplexers to ground, and to turn-on and turn-off UCCs.

The digital lines from the output of the $DATADRIVERS$ are routed to the columns where their corresponding UCCs are accessible. There are two data lines in the first column, three in the second column, increasingly towards the middle of a section of a quadrant. This is because most the of UCC in the middle belong to a coefficient with small number of Q_i (the number of UCC that belong to a coefficient in one quadrant). As a result, there are more parallel data lines, up to eight, in the middle of a section of each quadrant. For this reason, the data lines in the middle are more loaded with sidewall parasitic capacitance than those data lines on the left and right side of the a section of a quadrant of the UCC array. However, with respect to total parasitic capacitance looking from the output of their respective drivers, the data lines in the middle feed to only a few UCCs and experience smallest input capacitance loading. On the other hand, those at the edge are driving up to 16 UCCs in one section of a quadrant, and experience more loading. This, nevertheless, has been discussed more precisely in subsection 6.3.4.

Since it is a custom layout, careful column by column optimization was done to decrease the number of data lines routed vertically. For example, horizontally propagating data lines using a free metal layer to UCC that belong to the same coefficient. In the UCC layout, the nearby analog signals in one side of the UCCs, the two outputs and two biasing signals, are separated by some horizontal gap and vertically by using different metal layers. The fringe capacitances that resulted were minimal.

6.3 Design and Layout of Each Block

The circuit blocks are briefly introduced in subsection 6.2.2 when discussing the floorplan. In this subsection, the circuit topology used, and design strategies followed in each circuit block are discussed.

6.3.1 Digital Delay Line

The outputs of the digital delay line are taken through the routing matrix to the input of the Mode Selection block. Depending on the mode, the output can drive up to seven multiplexers. In the 802.11ac mode, the outputs of each of the flip-flops of the delay line are connected one-to-one with the inputs of the

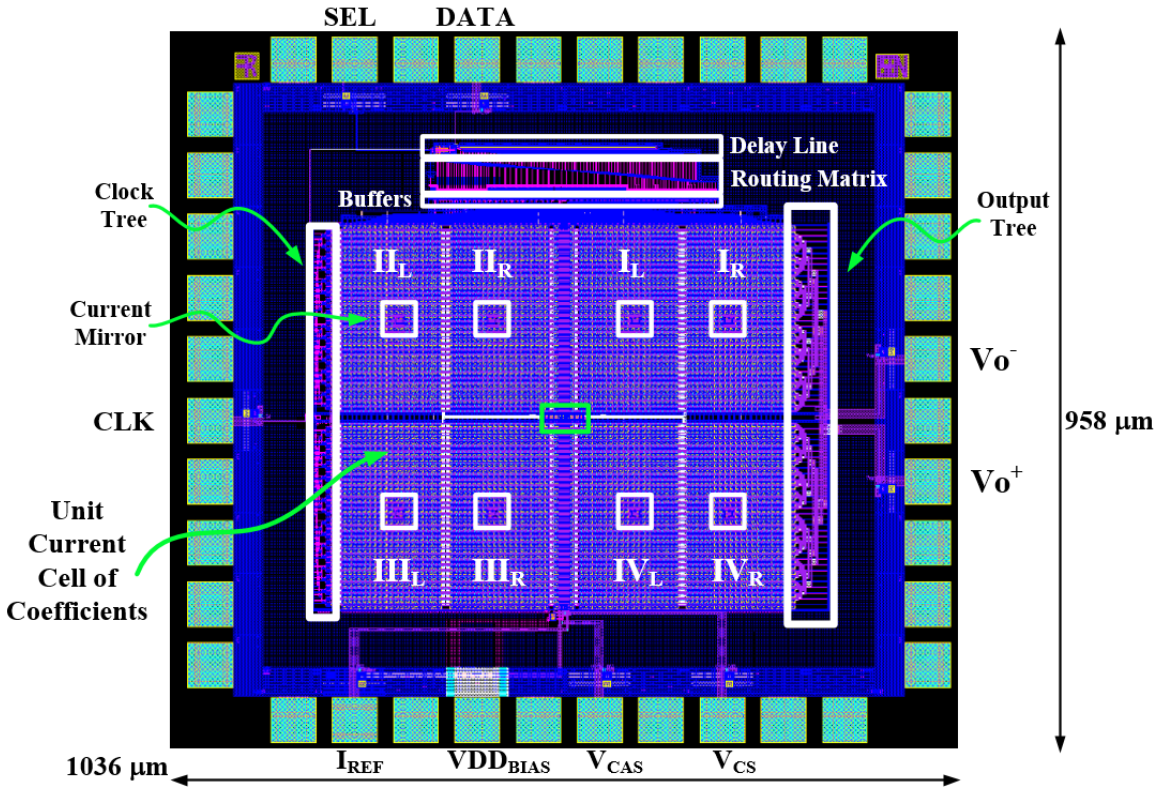


Figure 6.7: FIKRDAC Layout

multiplexers of the mode selection. However, in the 802.11ad mode, where smaller number of outputs, 17, of a shorter delay line are driving the same number of multiplexers, the flip-flops may experience a fan-in up to seven. Thus, the flip-flops are designed for the maximum load.

To reduce clocking timing errors, and the added area and power consumption needed for complementary clocking, the delay line is based on a TPSC flip-flops. Although only a single output is needed, the clock loading for the positive-edge triggered differential semi-static flip-flops, shown in Figure 6.8, is minimized and, hence, have the lowest power consumption [YS97]. Moreover, they can be implemented without additional circuitry, only a low power single-to-complementary buffer-inverter combo is needed, Figure 6.19.

The first stage is an CVSL-based circuit which evaluates the differential inputs when the clock is low. These outputs are forwarded to the output of the second stage when the clock goes high. The inverters hold the outputs steady. There is a chance a *HIGH* data input can go to second stage before the clock goes low in the PMOS transistor, but the outputs do not change before the NMOS is clocked by a rising edge.

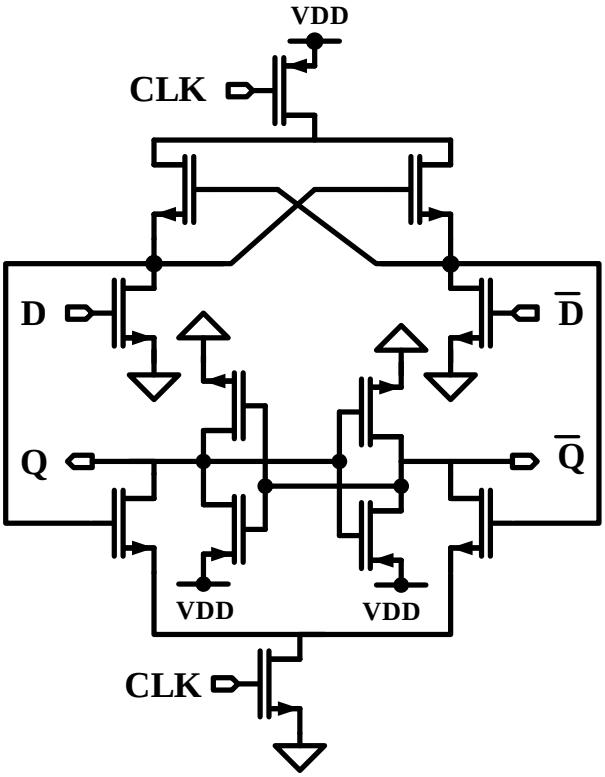


Figure 6.8: A semi-static Flip-Flop for the delay line of the FIR DAC

6.3.2 Mode Selection

In the 802.11ac mode, the mode selection block is a line of multiplexers with as many multiplexers as there are flip-flops in the delay line. There is a one-to-one matching between the delay line outputs and the mode selection inputs. In the 802.11ad mode, these line of multiplexers are driven by a shorter delay line, 17. Since the coefficients of the 802.11ad are only approximated when the 802.11ac coefficients are combined, additional coefficients are needed for fine-tuning. The inputs to these additional coefficients still come from the delay line but they operate only in the 802.11ad mode. Hence, similar to the multiplexers corresponding to the coefficients working only in the 802.11ac mode, one of their inputs are tied to the ground.

The multiplexers are designed based on a transmission gate logic to transfer both high and low values effectively as shown in Figure 6.9. Input and output inverters are inserted to balance loading experienced by the outputs of the delay line and the inputs of the data drivers respectively.

6.3.3 Routing Matrix

The routing matrix is the main block which enables configurability of the FIR DAC. The function of this matrix is to route delay line outputs to multiple coefficients so that a new set of coefficients can be

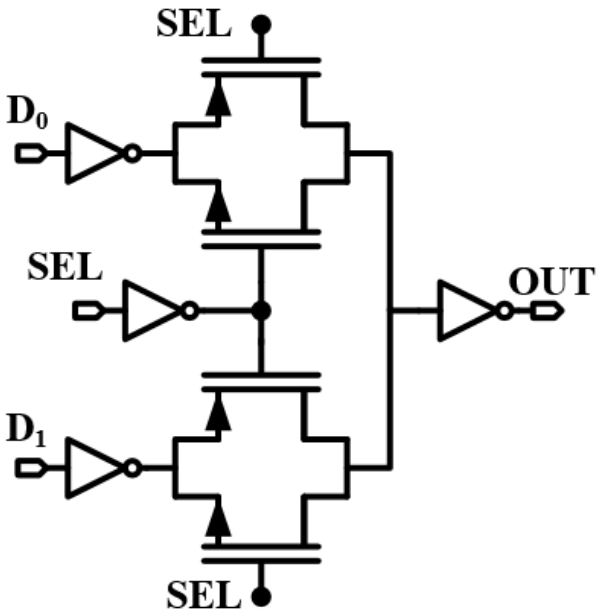


Figure 6.9: A 2-by-1 multiplexer for mode selection

created. In the 802.11ac mode, the coefficients match one-to-one with the delay line outputs according to the filter impulse response of 802.11ac in chapter 5. In the 802.11ad mode, they have to be routed according to a summation table.

The delay line of 802.11ad is created from the first 17 flip-flops in the delay line of 802.11ac. The remaining flip-flops can be turned-off for power saving. Below each of the 17 outputs are the the taps which are driven by these same outputs. For example, The output of the first flip-flop drives both the 18^{th} tap; likewise, the output of the third drives taps 1, 3, 15, and 17. Coefficients from 64 to 76 are added for fine-tuning the coefficient values of the 802.11ad. Here they are being driven by one of the 17 outputs of the 802.11ad mode delay line. Their inputs are grounded in 802.11ac mode.

Table 6.1: Weights of the 802.11ad mode fine-tuning coefficients

Taps	64	65	66	67	68	69	70	71	72	73	74	75	76
Values	11	-2	-1	5	14	4	2	4	14	5	-1	-2	11

At the output of the mode selection, there are 76 data values. Each one of the first 63 values drive some number of UCC as defined in the impulse response, the remaining 13 values drive UCC as defined in Table 6.1. The UCC array occupies large area. Routing the outputs of the mode selection block directly to the UCC inputs incurs significant speed reduction. Therefore, data drivers are inserted to drive both the total UCC input impedance and to compensate speed losses due to routing.

WiGig Taps use first 17 delays and they are created from the following taps of WiFi. Each of the 17 taps below, first 17 taps of WiFi, are routed to those in the same column

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
18	16	1	21	20	7	2	23	30	35	55	50	44	43	47	48	46
		3			10	4	25	31	36	56	51			49		
		15			11	5	28	32	39	59	52			61		
		17			12	8	29	33	41	60	53			63		
					13	9		34		62	54					
					14						57					
64	65	66	67	68			69	70	71			72	73	74	75	76

Figure 6.10: This shows how the coefficients of 802.11ad are created from 802.11ac. The number at the top indicate taps of the 802.11ad. Each tap is drives the taps 802.11ac taps listed below it and the taps for fine-tuning from 64–76.

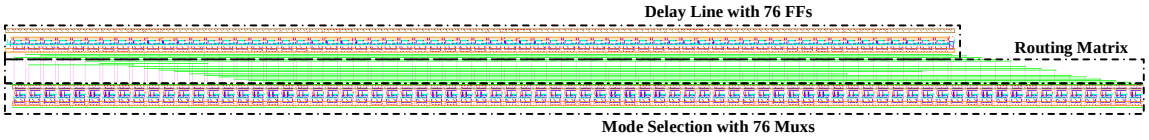


Figure 6.11: The layout of the digital delay line, routing matrix and the mode selection blocks. One of the inputs of the Muxs is directly connected to the flip-flops whereas the other is connected according to the matrix shown above in the table.

6.3.4 Data Drivers

The input data to the FIR DAC are sampled first time at the flip-flops of the delay line, and they are synchronized again at the latches that drive the differential switches of the UCCs. Thus, there are two set of paths between the arrival of the data at the input of the *DelayLine* and at the differential switches of the UCCs. The data time delay between the delay line and the latches has to be less than one clock period minus the hold time required at the flip-flops and the setup time required at the latches. To ensure the data arrives ahead of the clock edge, drivers are inserted between the mode selection and the UCC array. The delay from the output of the delay line to the driver is a small fraction of the period of the clock. However, the delay from the output of the drivers to the input of the latches may not be within the expected margin.

Bandwidth Limitation

The design of data drivers depends on the total load of each data line. For smaller number of UCCs and when the input capacitance of the UCCs, C_{UCC}, is such that the total input capacitance defines the time constant, tapered buffer design which only considers the capacitance as a load can be followed to arrive at to size the drivers. Parity in time delay for each data line can then be reached by sacrificing some area and power consumption by choosing drivers with equal number of stages for even the data lines with smaller number of UCCs.

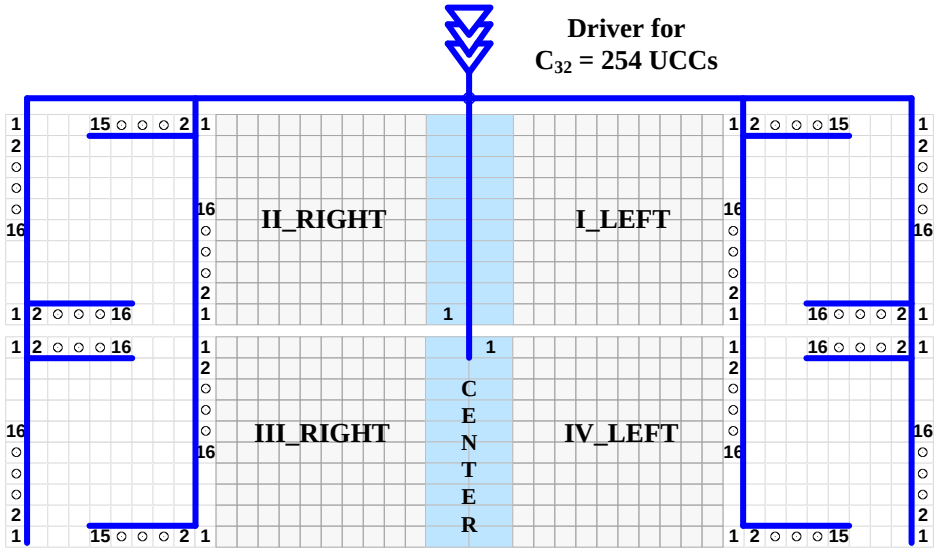


Figure 6.12: The placement of 254 UCCs of coefficient 32 and a depiction of the routing of the data line from driver to the UCCs

Nevertheless, in some cases, the data lines on the left and right edges of a section of a quadrant drive a high number of UCCs. This is because the UCCs that belong to the biggest coefficients in the impulse response of the FIR DAC are placed in the outer edges of the quadrants with the UCCs that belong to the smallest coefficients in the middle of the quadrants. This is done to equalize the quadratic errors of the randomly-valued coefficients. These data lines normally drive up to 256 UCCs, for example, for the center tap. On the other hand, when there is a long RC interconnect in such a way that the $\tau_{rc} > \tau_{driver}$, the equivalent load impedance of the wires should be calculated. The driver has to be designed to make sure the required data rate, and the required bandwidth of the system can be met.

To further explain the point above, Figure 6.12 shows the routing from the output of the driver for coefficient 32 in the 802.11ac impulse response, which is realized with 254 UCCs. The UCCs, as expected, are in common-centroid configuration with two remainders in the center. Each UCC has different RC interconnect delay between itself and the driver. This is clearly shown in Figure 6.13. The

RC segments are represented by an equivalent impedance. The UCC in one location are represented by a box whose equivalent circuit is shown to the right. The model for N number of UCCs has N number of input capacitances and $N-1$ RC segments between them. The equivalent circuit of the rest of the quadrants is the same as that of the first quadrant.

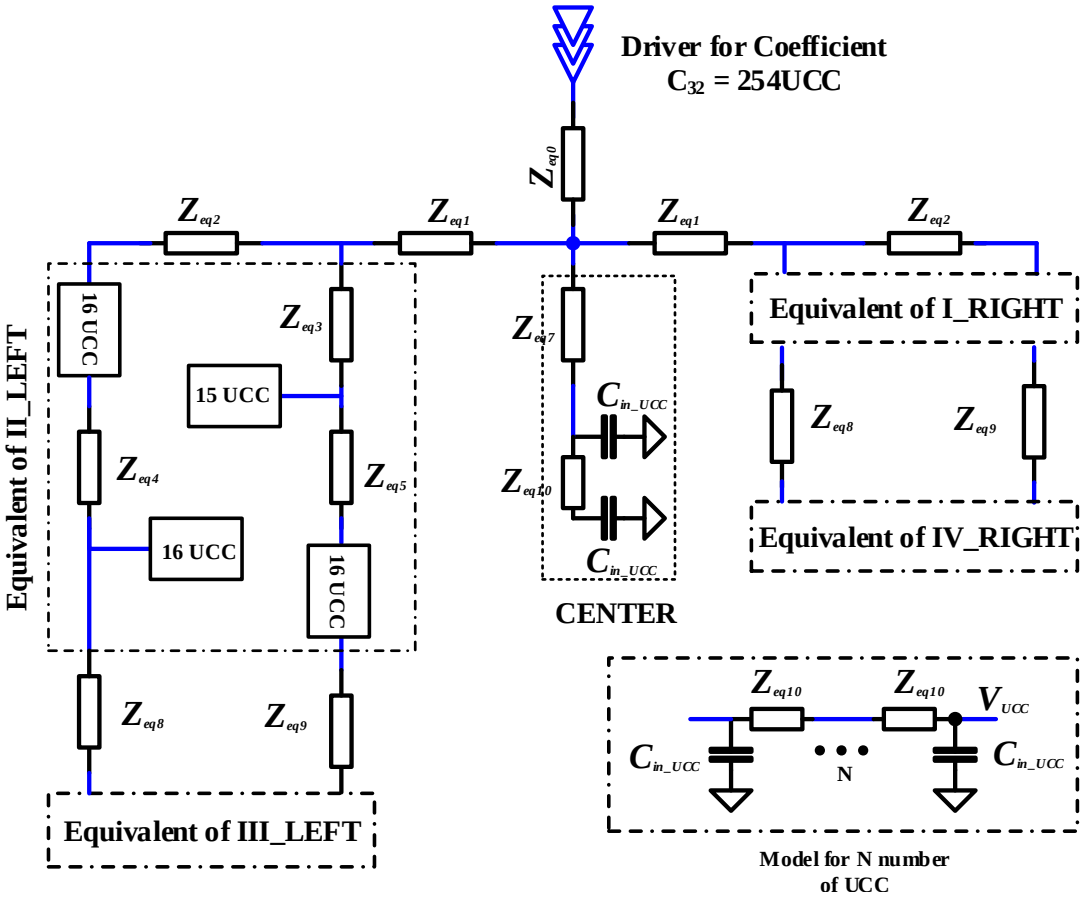


Figure 6.13: Model of equivalent impedance of routed data lines for coefficient 32 with 254 UCCs

All the latches of all the UCCs are clocked with the same signal. The delay difference between the clock edges at two different latches of the 254 UCCs is insignificant; or it is expected to be corrected by the binary tree of the output network. As a result, it is only enough to estimated the worst delay from the driver to one of the latches of the 254 UCCs. The UCCs placed furthest away from the driver are the obvious candidates. To find the worst delay, the total RC interconnect between the driver and the UCC of interest has to be modeled.

A simple *RC* lumped wire model from the driver output to the input of the UCC of interest may not give us an accurate estimation of the delay—tends to be pessimistic [RCN03]. Hence, unnecessary over design of wire widths, usage of higher metals while not needed could result. Common approximation for a distributed wire model are shown in Figure 6.14. A distributed wire model with the Π-model

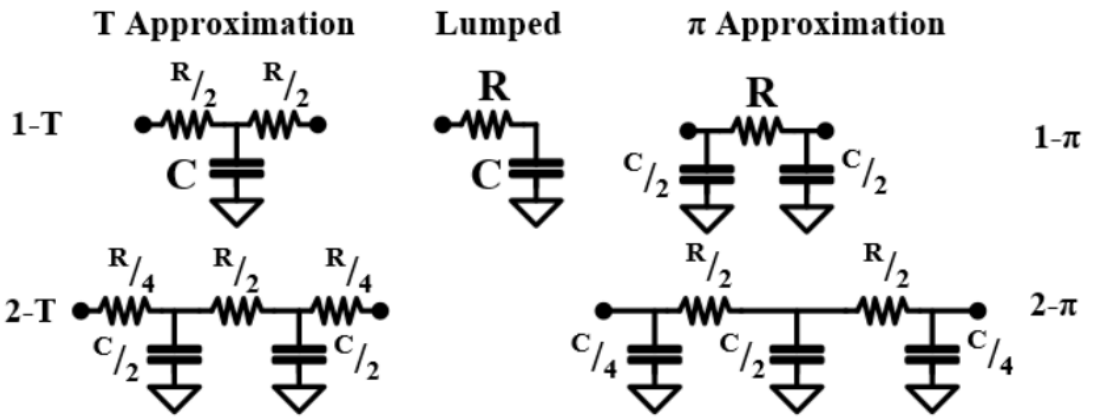


Figure 6.14: RC interconnect models that can be used for fast, less accurate estimation of delay

approximation results in a more accurate, compared with the lumped model, delay estimation. However, the amount of calculation required to estimate the component values could be complex even for a few interconnects. An elaborate wire model may consider metal-to-substrate capacitance, metal-to-metal fringe capacitance, overlap cap, routing resistance, via resistance, etc. In advanced technologies where there are up to ten metal levels, and in a dense layout, this may not be an easy feat.

One formula which gives a practical delay estimation for an RC network with simpler calculations is the Elmore delay formula. The formula assumes a network with one source node where there are no resistive loops and all the capacitors are between a node and ground [RCN03]. Although it is a first-order approximation, its simpler calculation makes it attractive.

Depending on the complexity of the coefficients, the RC segments in Figure 6.13 can be replaced with lumped model of the approximation in Figure 6.14. The Elmore delay from a source S, the driver, to node i, one of the UCCs, is given as [RCN03]:

$$\tau_{si} = \sum_{k=1}^{N} C_k R_{ik}. \tag{6.13}$$

Where k is a capacitive node in the circuit, and N is the number of nodes. There is a possiblity that the formula can result in large errors. However, it is predicted to work better when the node of interest is farther from the source [ADK01].

It is interesting to derive some quantitative expression for bandwidth limitation calculation using the pseudo double common-centroid UCC array placement. It is observed that the RC interconnect associated with the biggest coefficient results in higher time constants. The biggest coefficients are placed in the perimeter of the sections of the quadrants. A driver for a coefficient whose value is almost equal to the biggest coefficient, the center tap in a symmetrical FIR DAC impulse response, requires four data line routing. Two lines in the left and right side of a section of a quadrant, and two in the other. A

fifth for the center if it has a remainder after division by four.

The value of the coefficient can be approximated to 2^B, B is quantization bits. Out of four data lines routed to four quadrants, $\frac{2^B}{4}$ UCCs are connected to one. Considering Figure 6.13, each one-fourth of $\frac{2^B}{4}$ are placed in one location feeding from a tap from this line. The RC segment between the UCC in each group is neglected. The Elmore delay from the driver output to the furthest UCC along the data line in the left-end of the figure can be calculated as a sum of:

$$\tau_{si} \geq \frac{2^B}{4}C_{in\_UCC}R_1 + \frac{2^B}{4}C_{in\_UCC}R_2 + \frac{2^B}{4}C_{in\_UCC}R_3 + (\frac{2^B}{4} - 1)R_4 + C_{in\_UCC}R_{total\_line} \tag{6.14}$$

Where R_1, R_2, R_3, and R_4 are resistive approximation of $Z_{eq0} + Z_{eq1} + Z_{eq2}$, $Z_{eq0} + Z_{eq1} + Z_{eq2} + Z_{eq4}$, $Z_{eq0} + Z_{eq1} + Z_{eq2} + Z_{eq4} + Z_{eq8}$, and $Z_{eq0} + Z_{eq1} + Z_{eq2} + 2Z_{eq4} + Z_{eq8}$. R_{total_line} can be approximated as a sum of: $Z_{eq0} + 2Z_{eq1} + Z_{eq2} + 2Z_{eq4} + Z_{eq8}$ because the RC segment between two UCCs of the same group is neglected. This leads to

$$\tau_{si} \geq \frac{2^B}{4}C_{in\_UCC}(R_1 + R_2 + R_3 + R_4 + R_{total\_line}) \tag{6.15}$$

$$\tau_{si} \geq \frac{2^B}{4}C_{in\_UCC}(4(Z_{eq0} + Z_{eq1} + Z_{eq2} + Z_{eq4}) + 2Z_{eq8}) \tag{6.16}$$

If Z_{eq8} RC segment is close in length as the other segments, $4(Z_{eq0} + Z_{eq1} + Z_{eq2} + Z_{eq4}) + 2Z_{eq8}$ can be approximated to be around $3.5R_{total\_line}$. Then the maximum time constant of this particular line is given as:

$$\tau_{si} \geq 3.5\frac{2^B}{4}R_{total\_line}C_{in\_UCC} \tag{6.17}$$

For example, to achieve a bandwidth of 3.52 GHz with 8-bit quantized coefficient and with C_{in_UCC} of around 400 fF, the left-end data line has to be $\leq 1.3K\Omega$. This can be difficult to fulfill, so it is advisable to use non-shared data lines to a group of UCCs when possible.

The data drivers have a fan-out of four and range from two stage to five stage. A more square layout is obtained by breaking down the longest stages into layers as shown in Figure 6.15. After the final layout of the UCC array, the wire resistance and capacitance were again estimated, and the widths of the wires were changed and choices of adjacent metals changed adjusted in some cases to shorten time delay.

6.3.5 Clock Tree and Output Tree

Two circuit blocks in the chip require clocking. They are the digital delay line, and the synchronizing latches in the UCC array. Due to its size, the clock in the UCC array is distributed with the help of a

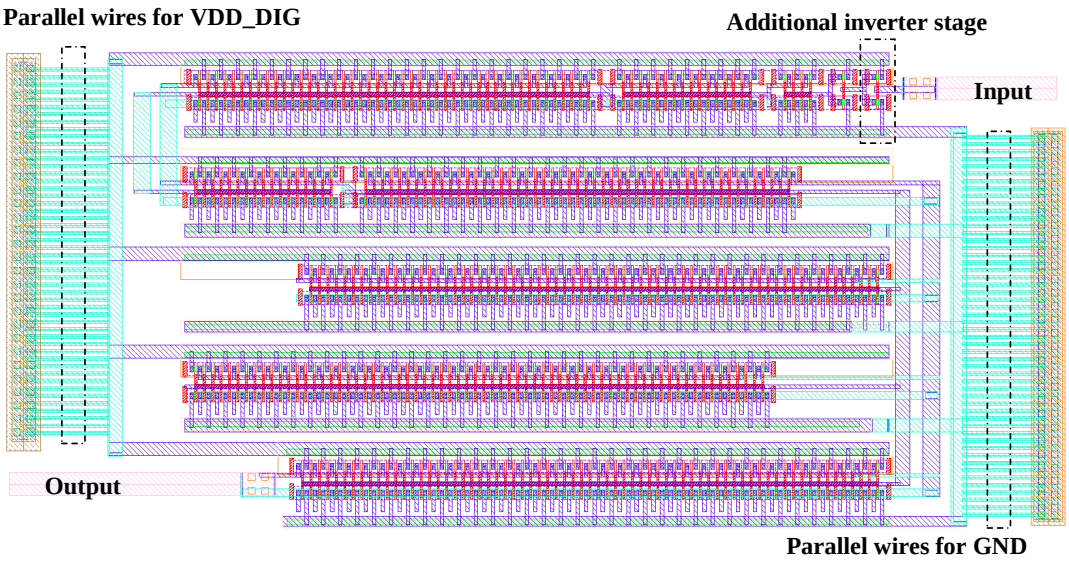


Figure 6.15: The layout view of the a five-stage driver used for the biggest coefficients in the center of the 802.11ac impulse response. Additional stage inserted not to invert the data. Supply connected using parallel thin wires to ensure low current density.

binary clock tree. The delay line occupies SMALLER area compared to the array. No clock tree is used for the delay line. The clock is supplied with a single metal running across all 63 flip-flops in the delay line. The delay from the clock at the PAD output to the delay line and to that of the clock tree output are equalized by using identical structures. The clock to the digital delay lien is driven by a seven stage buffer whose sizing is equal to a single *leaf* of the binary clock tree as shown in Figure 6.18. To maintain equal loading at each stage of buffer for the delay line, dummy inverters which have the same sizing as their counterparts in the binary clock tree are used.

The UCC array is arranged by taking the clock distribution into consideration into 64 equally-spaced rows. A top metal is used to route the clock signal along each row from the output of the tree to decrease the capacitance to adjacent metals and to the substrate. The output clock signal of all the 64 rows is shorted with a top metal spine. This is done to reduce timing differences between rows.

The binary clock has seven stages. Each buffer stage is designed at a fan-out of four. The layout is such that the loading at the nodes of a stage are the same; for example, equal width, length and level of wires, and same size of vias.

Although the final clock signal at the output of the binary tree is distributed with a low capacitance top metal routing, there are still timing differences among the UCCs along a single row. Practically, the UCCs to the side of the clock tree are clocked earlier than those farthest in the right. That is the output of those in the left will appear earlier. To balance this difference, a similar binary tree is used for summing

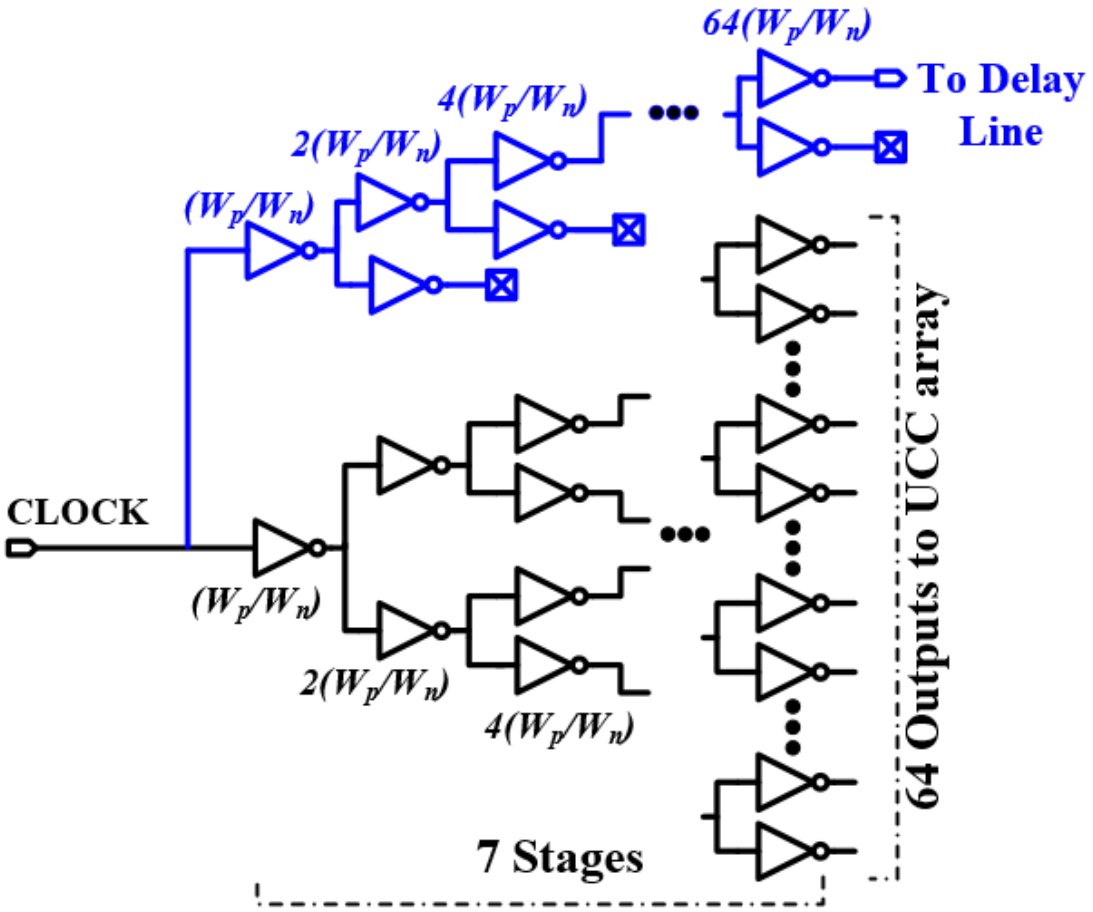


Figure 6.16: The clock is distributed with a seven stage clock tree to the UCC array, and a single leaf of this tree to the delay line. The inverters in the tree are sized have a fan out of 4. This is kept in the inverter chain to the delay line using dummy inverters.

the outputs.

6.3.6 Unit Current Cell

The UCC comprises both the digital and analog current source in one block. A single-ended data is its input. A circuit consisting of a transmission gate and an inverter create the signal for differential switching of the current source. The PMOS and NMOS transistors of the transmission gate are sized in the same ratio as those of the inverter. The differential signals are clocked using a steep transition latch [Lin+09]. The output of the latches drive the differential switches of the current source. Off-chip loads resistors are used.

Since the data is routed a long distance, a synchronizing latch is added. Each UCC has a synchronizing latch. Some power and area savings could be obtained by sharing one latch for a number of UCC,

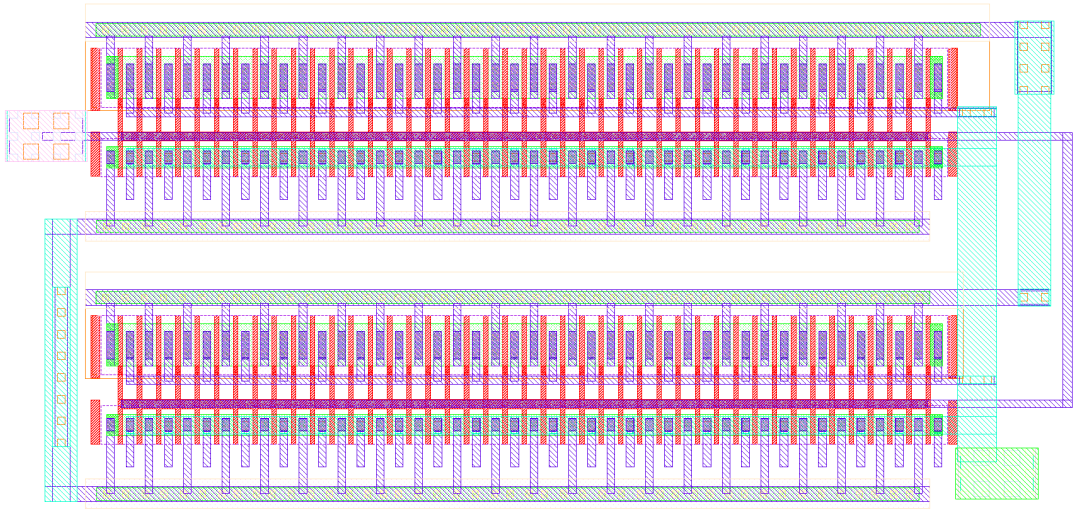


Figure 6.17: The layout view of the final stage buffers of the clock tree. Each PMOS and NMOS are sized 2^6 times the first stage transistors. The fingers are arranged as such so that the clock tree outputs of each of the 64 rows are routed straight to the UCC array with short wires and with minimum distance between the rows of the UCC array.

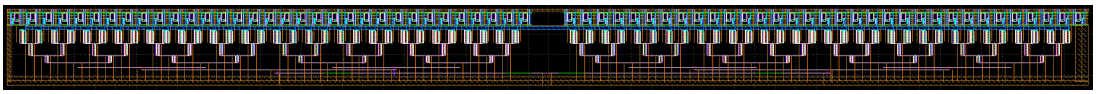


Figure 6.18: The layout view of the clock tree

i.e. data out of one latch to drive switches of multiple current sources that belong a coefficient. The disadvantage in this case is the errors that are incurred due to small timing differences in the switching of the current source of the different UCCs being driven by one latch. This errors depend on the layout and sizing of the latch and the UCCs, but the hard task of placing UCCs in different locations to mitigate mismatch and sharing an equidistant latch for all of them remains. To decrease SFDR degradation due distortion caused by timing differences, the latches of a UCC are placed as close as possible to the differential switches.

One of the advantages of the selected latch is the fact that the output of the latches intersect below the middle point of the signals. By following the latches with inverters, the outputs which control the switches are crossing above the middle point This prevents the possibility of the NMOS differential switches turning off simultaneously. It also guarantees the current never is interrupted as the controls signals allow smooth transition of current from one branch to the other. The crossing point is also set high enough so that the common source node fluctuation is minimized [Bas+98].

The latch was sized so as to decrease its contribution to the total local timing error of the FIR DAC.

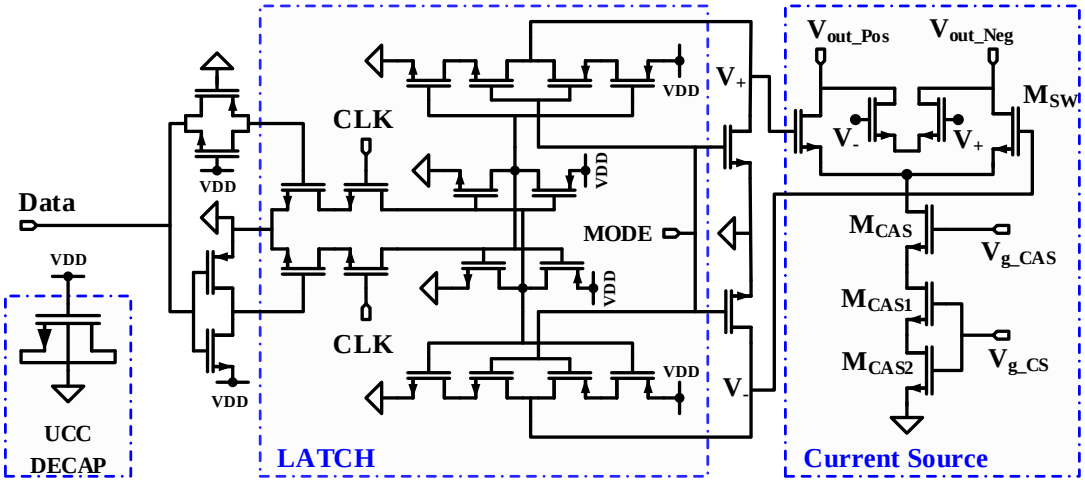


Figure 6.19: Transistor level schematic of a Unit Current Cell which works in 802.11ac mode and is controlled by SEL signal to turn-off in 802.11ad

The following expression for SDR due to random local timing errors is used in the simulation [DRL06]:

$$SDR = \frac{N}{(8 f_{sig} f_s \sigma^2)} \tag{6.18}$$

where N is the number of unary elements in the 802.11ac or 802.11ad modes of the FIR DAC, f_{sig} is the data bandwidth, f_s is clock rate and σ is the standard deviation of the random timing errors. Contribution to the spread of the timing errors is calculated from mismatch of clocked transistors using capacitive loading, biasing current and technological parameters. Similar approach was used to estimate and consider the error that can be contributed due to capacitive loading difference between the gates of the differential switches of the UCC and the final driving tri-state inverters' output load capacitance. The tri-state inverters are sized taking the timing errors, and the high crossing control signals for the differential switches into consideration [TG06].

A combo of tri-state inverters and input grounding is used to turn-off the UCC when it is not part of the operating mode impulse response. This mechanism ensures that the differential switches stay turned-off. The same signal as the mode selection signal is the input to the tri-state buffers. Therefore, the signal that selects a standard in the *ModeSelection* block all turns off unused UCCs of the other mode. These arrangement does not change the high-crossing output expected of the tri-state inverters.

The back-to-back inverters are sized small, and they help in reducing the clock feedthrough to the output [BSS04]. The gate-to-drain charge feedthrough in the differential switches introduces distortion in the outputs. Different methods to mitigate this problem: one is to add a cascode transistor on top of the switches. This method does not suit advanced CMOS nodes as it requires higher analog voltage

supply. It is also possible to lower the swing of the control signals. This method negatively affects the maximum speed at which the UCC can operate [CG07]. A method preferred here is to add two dummy switches with floating sources and are driven opposite to the switches with the same complementary control signals. If they are sized the same as the switches, the problem of charge feedthrough is reduced [LCD00].

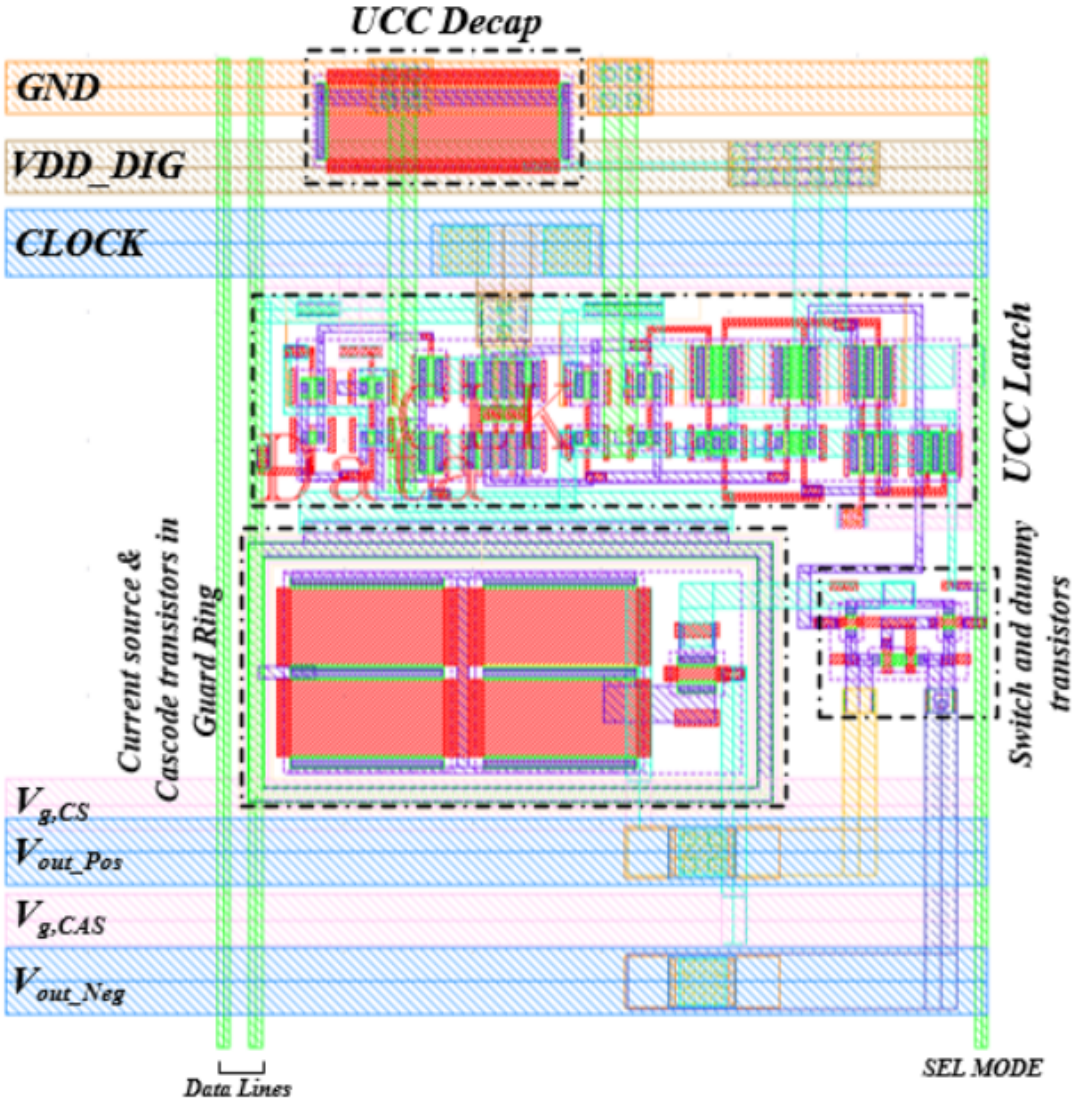


Figure 6.20: The layout view of a unit current cell used in both modes.

The overdrive voltage and size of the current source transistor are designed to meet the random mismatch requirement as given by Equation (4.13) in Chapter 4. That is the drain voltage of the current source transistor, M_{CS}, is set to $V_{OV} + V_{tol}$ higher than the overdrive voltage. V_{tol} is a to ensure saturation operation. To operate the cascode transistor in saturation region, the common source node of the switch transistors has to be at least $2V_{OV} + 2V_{tol}$. The unit current is set by the dynamic range required at the

output as explain at the end of Chapter 4. Large number of UCCs, 4974 in the 802.11ac mode, sum up to a large output swing. This takes big part of the voltage headroom in a low voltage supply operation of the UCC. To ensure saturation region operation of the differential switch transistors

$$VDD_{ANA} - N_{unit}R_{load}I_{unit} \geqslant 3V_{OV} + 3V_{tol}. \tag{6.19}$$

The effect of data dependent output impedance on the dynamic performance of the FIR DAC is already discussed in chapter 4. To ensure high output impedance up to higher frequencies, minimizing unnecessary interconnects during layout of the UCC is important. The contribution of the parasitic capacitances due to interconnect is minimum in this implementation. That means the output impedance will stay flat up to higher frequencies, but the actual values depends on the sizing and biasing of the transistors. This was set through simulation in Cadence® and MATLAB® by tweaking the biasing voltages and sizes of the transistors.

To obtain a more square layout of the current source transistor, it is realized using two identical transistors in series. The current source and cascode transistors are placed inside a guard ring. To stabilize the supply voltage of the UCC, a NMOS decap is connected in the gap between VDD and GND planes.

6.3.7 Biasing circuits

For best dynamic performance of the UCC, the current mirror needs to target ideal requirements. The relationship between SFDR of UCC and output impedance is already stated in Chapter 4. Ideally, a current mirror should also have low input resistance. Technological limits such as supply voltage also limit the input and output voltage swings a particular topology of a current mirror can offer. These practical parameters can be used from the selection of the circuit topology to its sizing.

Although supply voltage limit in advanced CMOS nodes discourages use of cascoding, the high speed operation targeted requires high output impedance, and cascode current mirrors generally fulfill that requirement. A classic cascode current mirror circuit is shown in Figure 6.21a. It offers high output resistance and low input resistance given by the equation (6.20).

$$r_{out} = (g_{mCS} + g_{mCAS})r_{oCAS} + 1)r_{oCS} + r_{oCAS} \tag{6.20}$$

$$r_{in} \approx r_{o1} \tag{6.21}$$

However, it has a high minimum output voltage which eats away on the possible load voltage swing of the UCC. An alternative is to use two simple current mirroring biases as shown in Figure 6.22. It solves the problem of high minimum output voltage by lowering it to $2V_{OV}$ and still maintains high

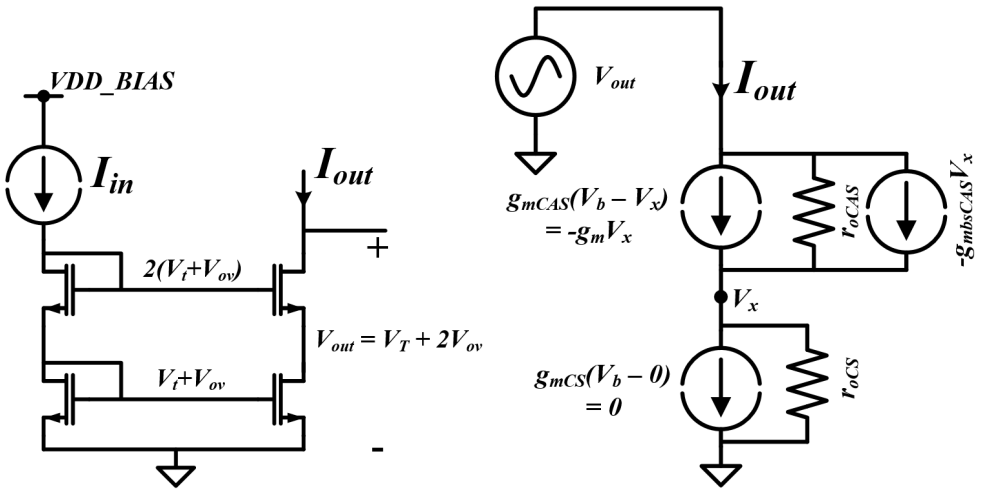


Figure 6.21: A simple Cascode current mirror and small signal analysis of its output resistance

output impedance. However, the current gain of such an approach suffers due to effect of drain-source voltage difference of M_{CS} and M_1 on the output current [Bak10].

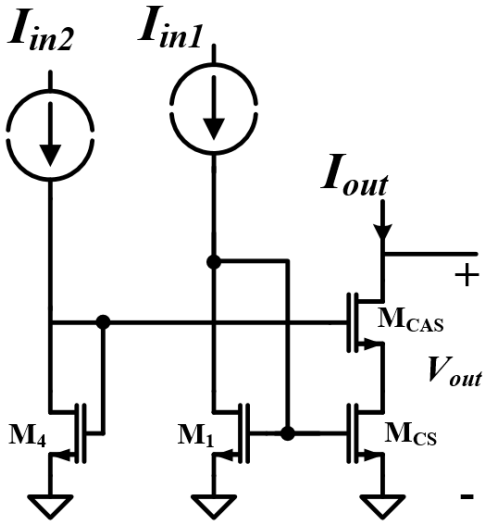


Figure 6.22: Cascode current mirror biased with two branches

The circuit used in this implementation is shown in Figure 6.23. It offers the same output resistance that is derived in (6.20). By adding transistor M_2, the problem of drain-source voltage stability is solved, and in turn the systematic gain error. The origin of M_3 is understood by studying the single input reference current configuration of this circuit[Gra01]. In a single reference current case, transistors M_4 and M_3, as a single transistor, are connected on top of M_2. Gates of M_{CS} and M_{CAS} are biased from drains of M_2 and M_3 respectively. The gate voltage levels M_{CAS} and M_{CS} in Figure 6.21a have a difference of

$V_T + V_{OV}$. To cut the gate voltage of M_{CAS} to one overdrive voltage more than that of M_{CS}, transistor M_3 is used. This is because transistor M_4 forces M_3 into triode region operation. This can be easily shown as follows. The gate and drain of transistor M_4 are tied and it operates in active region. Thus,

$$V_{G4} - V_{S4} - VT > 0. \tag{6.22}$$

Assuming the threshold voltages of both transistors are equal to V_T, replacing V_{G4} by V_{G3}, and V_{S4} by V_{D3},

$$V_{G3} - VT > V_{D3}, \tag{6.23}$$

$$V_{G3} - VT - V_{S3} > V_{D3} - V_{S3}. \tag{6.24}$$

As a result, V_{DS} of M_3 is normally one V_T lower than gate voltage of V_4.

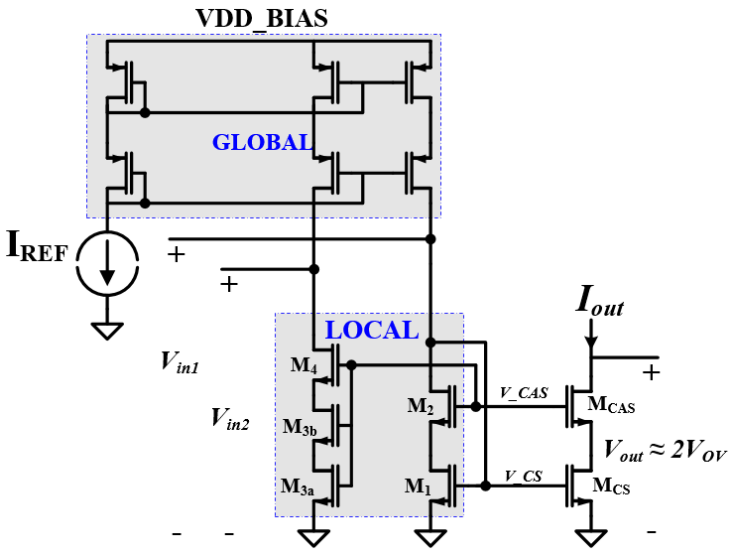


Figure 6.23: Sooch cascode current mirror for local and global biasing

In a two input reference currents configuration of Figure 6.23, its purpose is to bias the source of M_4. It is also useful to note that the aspect ratio of M_3 is a fraction of the sizes of the other transistors(M_1, M_2, M_4) which have identical sizes. This can introduce some non-uniformity in the layout. In this implementation M_3 is replaced with two gate-shorted transistors M_{3b} and M_{3a} whose length should effectively add.

With some assumptions of equal threshold voltages, an approximate size of M_3 can be calculated. Both are working in triode, then their input drain current can be approximated by this equation

$$I_{in1} = \frac{K}{2}\left(\frac{W}{L}\right)_{3b}\left(2(V_{GS3b} - V_T)V_{DS3b} - V_{DS3b}^2\right) = \frac{K}{2}\left(\frac{W}{L}\right)_{3a}\left(2(V_{GS3a} - V_T)V_{DS3a} - V_{DS3a}^2\right) \tag{6.25}$$

K is a technological constant.

$$2(V_{GS\,3b} - V_T)V_{DS\,3b} - V_{DS\,3b}^2 = 2(V_{GS\,3a} - V_T)V_{DS\,3a} - V_{DS\,2}^2 \tag{6.26}$$

If we make further assumption that drain-source voltage of M_{3b} is V_{OV}, and that of M_{3a} to be $\frac{V_{OV}}{2}$, (6.26) leads to

$$2(V_G - \tfrac{V_{OV}}{2} - V_T)V_{OV} - V_{OV}^2 = 2(V_G - V_T)\tfrac{V_{OV}}{2} - \tfrac{V_{OV}^2}{4} \tag{6.27}$$

$$V_G - V_T = \tfrac{7V_{OV}}{4} \tag{6.28}$$

Another equation can be derived from the drain currents of M_4 and M_{3b} as follows:

$$I_{in1} = \tfrac{K}{2}\left(\tfrac{W}{L}\right)_4\left(V_{GS\,4} - V_T\right)^2 = \tfrac{K}{2}\left(\tfrac{W}{L}\right)_{3b}\left(2(V_{GS\,3b} - V_T)V_{DS\,3b} - V_{DS\,3b}^2\right) \tag{6.29}$$

The ratio of transistor M_4 to M_3 can then be written as:

$$\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_{3b}} = \frac{2(V_{GS\,3b}-V_T)V_{DS\,3} - V_{DS\,3b}^2}{\left(V_{GS\,4}-V_T\right)^2} \tag{6.30}$$

Equating (6.28) and (6.29) and substituting the previous assumption on the drain-source voltages of M_{3a} and M_{3b} and , the ratio can be simplified to

$$\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_{3b}} = \frac{2\left(\frac{7V_{OV}}{4} - \frac{V_{OV}}{2}\right)\frac{3V_{OV}}{2} - \frac{V_{OV}^2}{4}}{\left(\frac{7V_{OV}}{4} - V_{OV}\right)^2} \tag{6.31}$$

$$\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_{3b}} \approx 6. \tag{6.32}$$

While the design is robust with respect to output resistance, input resistances, and minimum output votage, the input voltages of this configuration proposed in this implementation are higher compared to those in Figure 6.21a and Figure 6.22. As a result, it is important to calculate the minimum input voltage for both branches so that the minimum supply voltage can be known. This helps in determining the suitability of this configuration for low voltage operation.

$$V_{in1,min} = V_{GS\,4} + V_{DS\,3b} + V_{DS\,3a} \geqslant V_T + V_{OV} + V_{OV} + \tfrac{V_{OV}}{2} \geqslant V_T + \tfrac{5V_{OV}}{2} \tag{6.33}$$

$$V_{in2,min} = V_{GS\,1} \geqslant V_T + V_{OV} \tag{6.34}$$

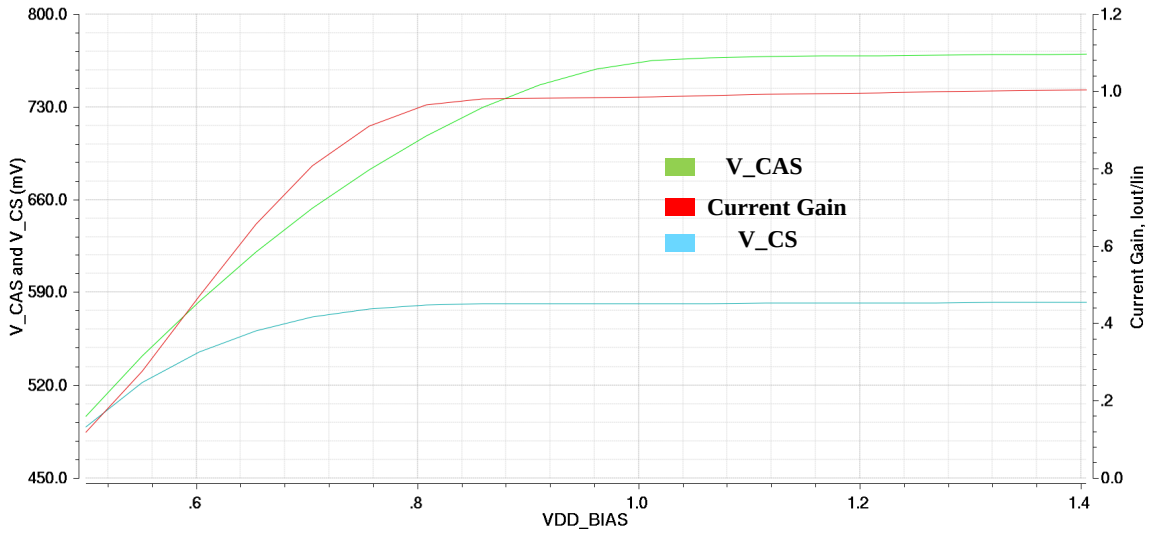


Figure 6.24: A simulation of minimum bias VDD that ensures flat current gain

The trade-off to the robustness and flexibility offered by the configuration in 6.23 is that the required supply voltage is high. It is interesting, then, to determine how low the supply voltage can become. In this implementation, only one reference current is used. To create a robust mirroring of this reference current to the two branches, a cascode circuit is used as shown in Figure 6.23.

$$V_{DD\_BIAS,min} = max(V_{in1,min}, V_{in2,min}) + 2(V_T + V_{OV}) = 3V_T + \frac{9V_{OV}}{2} \tag{6.35}$$

To support this theoretical calculation, a simulation of the circuit shown is done in CMOS 28nm FDSOI. The result can be seen in Figure 6.24.

6.4 Summary and Conclusions

In this chapter, the system-level results of a configurable FIR DAC from the previous chapter were used to design the circuit blocks of the FIR DAC. A thorough discussion starting from the floorplan to the circuit blocks of the DAC has been provided. A pseudo-double common centroid placement method for current steering FIR DAC architectures is introduced. The strength and weakness of this placement method based on its resilience to systematic mismatch errors is also discussed. The layout floorplan of the FIR DAC chip is detailed.

Besides, the different challenges faced during circuit design of each block are examined. Layout level discussion are included as needed to clarify the approaches followed. In the next chapter, a report of measurement of the designed circuit is included.

Chapter 7

Measurement Results of FIR DAC Prototype

A configurable high pass FIR DAC was fabricated in ST 28nm FDSOI with a 10 metal layer CMOS process. The chip is fully custom designed, and occupies an active area of $0.84mm^2$. The chip micrograph is shown in Figure 7.1. Due to metal filling, the circuit blocks are not visible. It has a $4x10$ PAD ring.

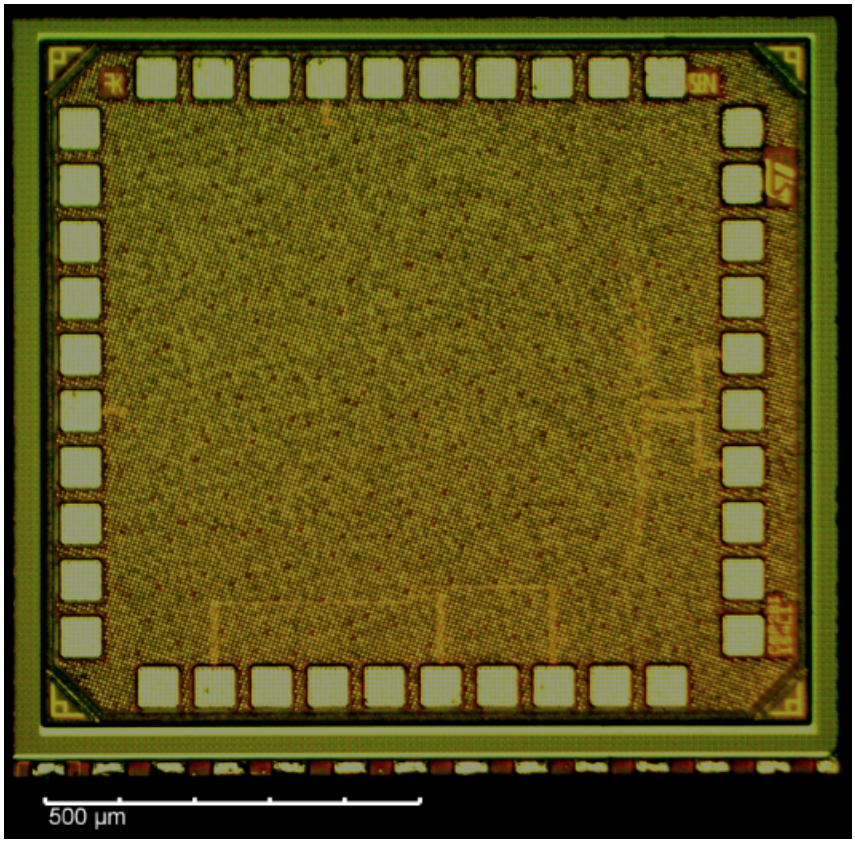


Figure 7.1: Configurable FIR DAC prototype die micrograph. It is fabricated in ST 28nm CMOS FDSOI.

To characterize the prototype FIR DAC circuit, it was first packaged in a QFN40 plastic open cavity package. Then a test PCB was designed using Altium® PCB designer. The package has small leads and only in its underneath. An efficient and reliable way to solder the package is to use an automatic or a

semi-automatic machine. The JFP Microtechnic® PP7 semi automatic pick and place die bonder was used for soldering the packaged die to the PCB at the right temperature gradient.

This chapter begins with the experimental setup section. Any specific choices with the designed PCB, or the instruments and connectors used are discussed in this section. The prototype FIR DAC is characterized using different inputs. Thus, the transmitter setup in Matlab® from which the input data is generated is also explained. In the next section, the actual measurement results for the two modes of operation of the FIR DAC are discussed separately. Discrepancies between theoretical or simulated results and the measured results are also presented in the same section. Finally, the chapter is closed with a last section which compares the obtained results to other works in the same area.

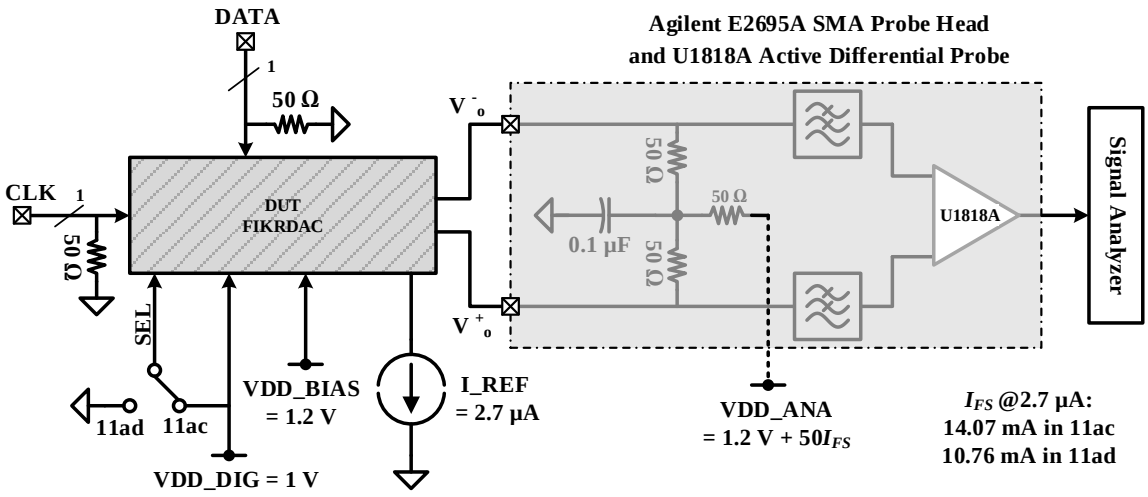
7.1 Experimental Setup

The designed circuit is that of a high pass FIR DAC that implements two impulse responses. The prototype chip in Figure 7.1 has eleven distinct PADs. The rest of the PADs are used for VDD_{DIG} and GND to lower IR drop. Two of the inputs: $DATA$ and $CLOCK$ are high speed digital; one is static DC input: SEL; four are current reference and voltage supplies: I_{REF},VDD_{DIG}, VDD_{BIAS},GND, and VDD_{ANA}; two are analog high speed outputs: $VOUT_{POS}$, and $VOUT_{NEG}$; and two are DC outputs: $VOUT_{CAS}$, and $VOUT_{CS}$.

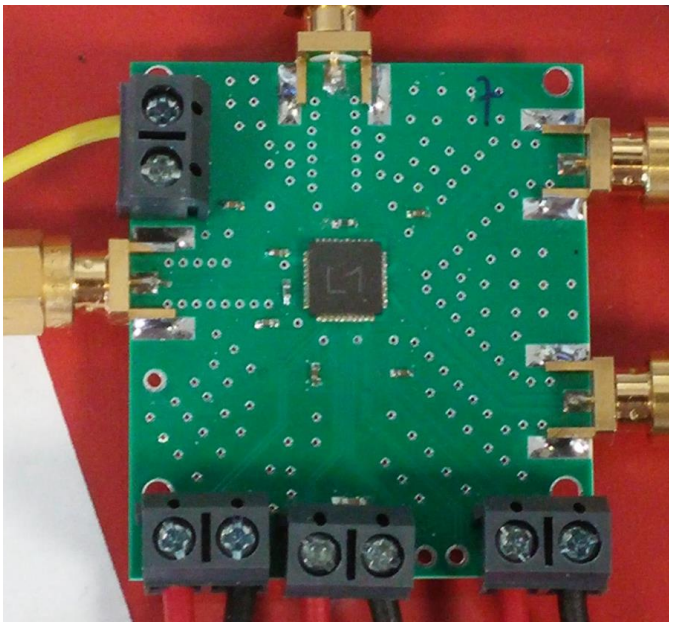
7.1.1 PCB Design

The SEL input is switched $HIGH$ for the impulse response of the 160 MHz 802.11ac, and it is LOW for that of IEEE 802.11ad. It can be supplied from VDD_{DIG} and GND. The $DATA$ input takes 1-bit digital data with the $HIGH$ value set at VDD_{DIG} and the LOW value set at GND. The clock is also a digital input, set on the same levels. Since both $DATA$ and $CLOCK$ have on-chip input drivers, the $CLOCK$ input can also be driven with a sinusoidal waveform and a DC offset. For standard 802.11ac measurement, the $DATA$ is first generated in Matlab® and then transferred to a Data Timing Generator. The supply inputs are all within a range of any standard source meter, so they are directly connected on the board. The differential outputs have to be connected to load resistors.

The chip was packaged in QFN40 plastic package using standard wirebond techniques. The PCB was separately designed using standard FR4 material in two layers. The instrument-generated high speed inputs are connected using SMAs, so a 50Ω track from the SMAs was terminated with 50Ω SMD resistors close to the package pads of $CLOCK$ and $DATA$ as shown in a circuit depiction in Figure 7.2a. Stabilizing capacitors are connected to VDD_{DIG} and VDD_{BIAS}. The rest of the inputs are connected using screw connected power connectors.



(a)



(b)

Figure 7.2: Schematic of test board and the test board with the packaged die on board. The high speed input and outputs are connected with SMAs, and power connectors were used for the static signals.

The analog outputs were initially designed to be connected to 25Ω load resistors. The initial solution was to use a transformer. However, the available bandpass baluns were not suitable for low frequency measurement. Besides, directly connecting the outputs to probes was found to be less susceptible to noise. The final measurement was carried out using 50Ω load resistors from probes. The analog outputs were directly connected to an oscilloscope and spectrum analyzer using Agilent E2695A differential SMA probe head and Agilent U1818A active differential probe. The probe head has a bandwidth of around 7 GHz which is above the expected maximum output frequency. The circuit of the probes is

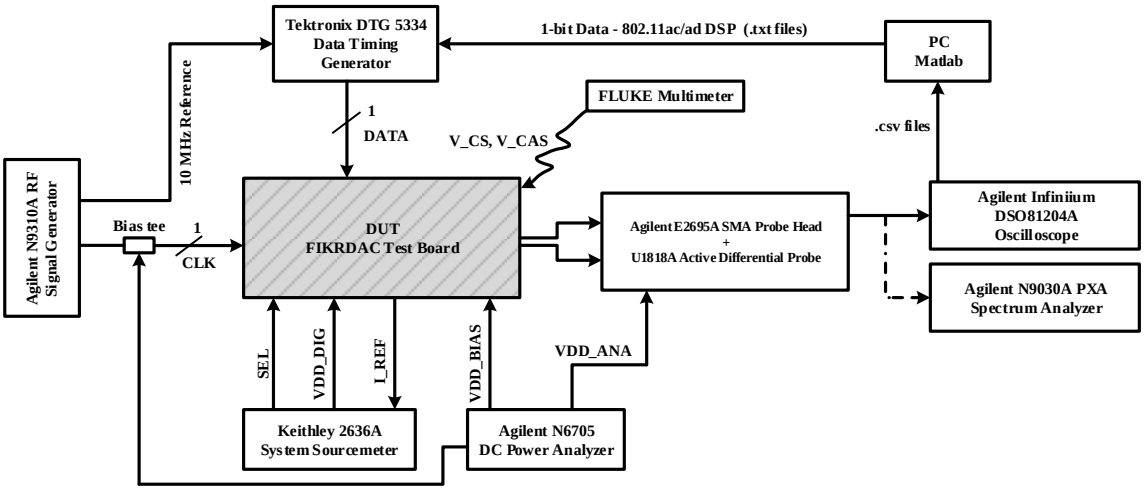


Figure 7.3: Instruments used in the measurement Setup

shown in Figure 7.2a.

There is an internal 50Ω resistor that connects the analog supply voltage to the common point of the load resistors. To account for the voltage drop in this resistor, the analog supply voltage is increased by 50 times the full-scale current as indicated in the figure. The full-scale current is different in the two modes because of the difference in the total number of UCCs. To keep the drain-source voltage of the switch transistors of the UCCs to within the safety limit, the analog supply voltage in the 802.11ad mode was lowered by about 150 mV.

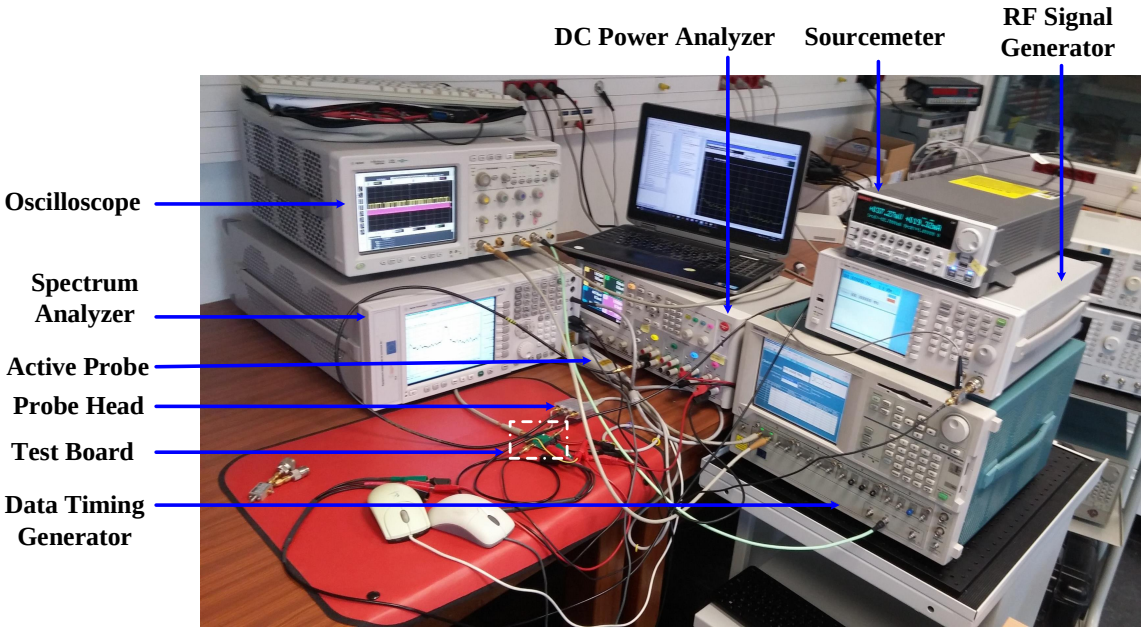


Figure 7.4: The test bench

7.1.2 Input Data Generation

For measurements involving random data, the *CLOCK* and *DATA* inputs were taken directly from Tektronix DTG5334 data timing generator. However, for measurement with modulated signals, the input data in the 802.11ac mode was imported to the data timing generator as a text file from a computer. The transmitter architecture used to generate the data is shown in Figure 7.5. The DTG can take at once, without repitition, a pattern file of $64e^6$ length of 1-bit values. The length of the 1-bit baseband data from the 802.11ac waveform generator oversampled by 22 is below this value. Hence, no special synchronization was needed between signal analyzers and data generators.

The circuit was clocked with a sinusoidal waveform from an RF signal generator with a DC Bias Tee connection as shown in Figure 7.3. This arrangement permits for better control to compensate any cable and termination losses from instrument to the chip. Also in this arrangement, the DTG was provided with a 10 MHz external reference from the RF signal generator.

A Keithley 2636A accurate sourcemeter was used for supplying the digital supply voltage and the reference current. Additional DC supply was used to provide the analog supply voltage, the bias supply voltage for the current mirrors, and for the Bias tee. Output signal analysis was carried out with Agilent Infiniium DSO81204A oscilloscope and N9030A spectrum analyzer. A picture of the test bench is shown in Figure 7.4.

Transmitter Model in Matlab®

For 802.11ac measurements, a BPF FIR DAC transmitter architecture was assumed. The block diagram of the transmitter in Matlab® is shown in Figure 7.5. The input to this function is taken from an IEEE 802.11ac waveform generator interface. This matlab interface was used to generate complex 160 MHz, 802.11ac signals in VHT single transmitter mode.

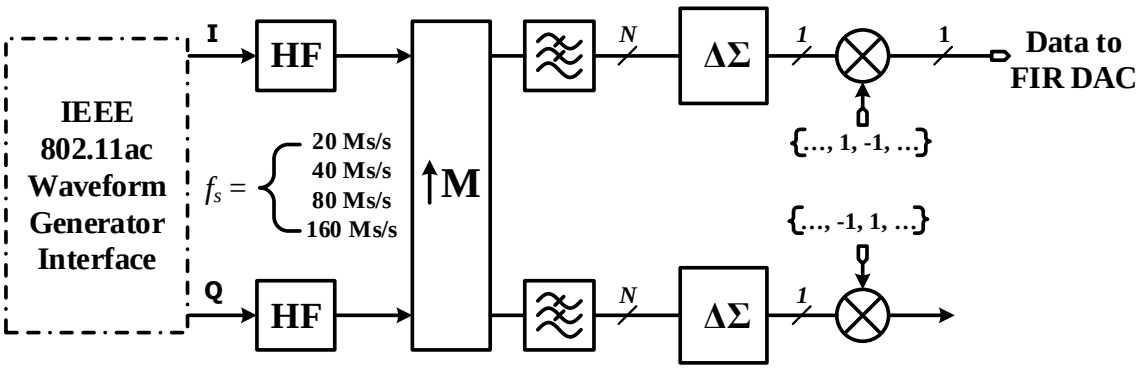
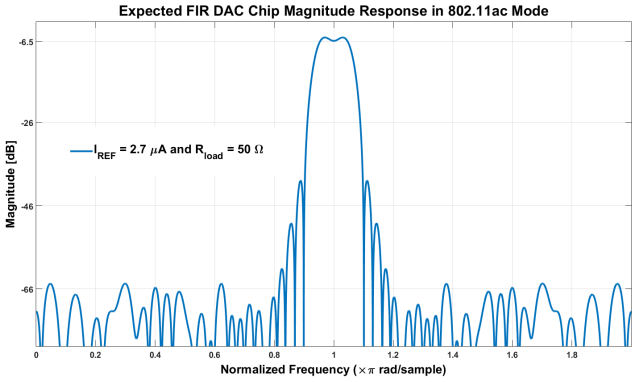
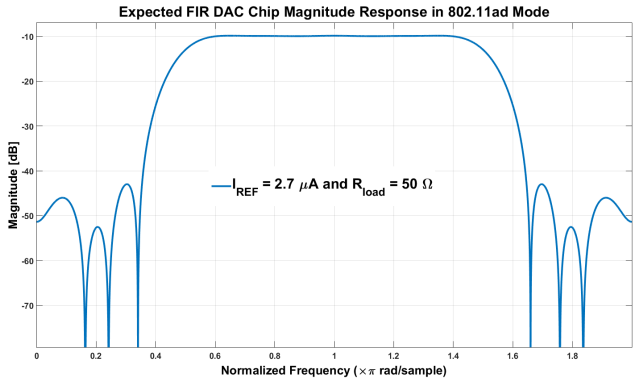


Figure 7.5: The transmitter architecture used to generate 802.11ac data for the chip characterization

The transmitter function implements half-band filter and resampler blocks for oversampling. Then the data is converted to 1-bit using a low pass delta-sigma modulator. A complex mixer is used for frequency translating the data to $\frac{f_s}{2}$. The 1-bit input sequence is loaded on the data timing generator as an input to the FIR DAC chip.



(a)



(b)

Figure 7.6: Transfer functions of the 802.11ac and 802.11ad modes with reference current 2.7μA and load resistance of 50Ω. The passband is expected to be attentuated by around 6.5 dB and 10 dB in the 802.11ac and 802.11ad modes respectively.

The complex baseband data of a IEEE 802.11ad is not windowed. Only oversampling by a factor of two is needed before the data is frequency translated to $\frac{f_s}{2}$. To simplify the test of this mode of the FIR DAC, non-oversampled PRBS data at the same rate as the clock was used.

7.2 Measured Results

The expected transfer functions for the two modes are recalled in Figure 7.6. The coefficient values of the two transfer functions are adjusted to the reference current and load resistors used in the measurement.

The unit coefficient is equivalent to a drop of 2.7 μA on a 50 Ω load, and the current values for the rest of the coefficients are an integer multiples of I_{REF} on the same load. The passband of the magnitude responses experience a drop of 6.5 dB and 10 dB, compared to the a 0 dB gain full-scale values, for the 802.11ac and 802.11ad modes respectively. The reason this value of reference current was selected is to adjust the DC bias conditions to the load resistors of the output differential probes. High reference current results in the triode operation of the switch transistors of the UCC for the analog supply voltage indicated in Figure 7.2a. In cases where a different value of reference current is used, for different reasons, it will be indicated. However, the figures should help as a reference at this value of current.

The FIR DAC was characterized for its performance as a standalone filter and as a FIR DAC as part of a transmitter in each mode of operation. In the 802.11ac mode, actual 802.11ac modulated signal was used to test the chip for wideband operation with different MCSs. Then PRBS input data was used to characterize the FIR DAC as a filter. Single-tone signals were also used to check the dynamic performance of the FIR DAC, and they are included in the last parts of 802.11ac sub-sections.

7.2.1 Biasing Circuits

The first sub-section is measurement of the wide-swing biasing circuits used in the FIR DAC. A detailed analysis of the circuits in transistor level of abstraction is already included in Chapter 6. During measurement, the operation of the mirroring circuits at different parts of the FIR DAC chip was tested by varying the biasing voltage.

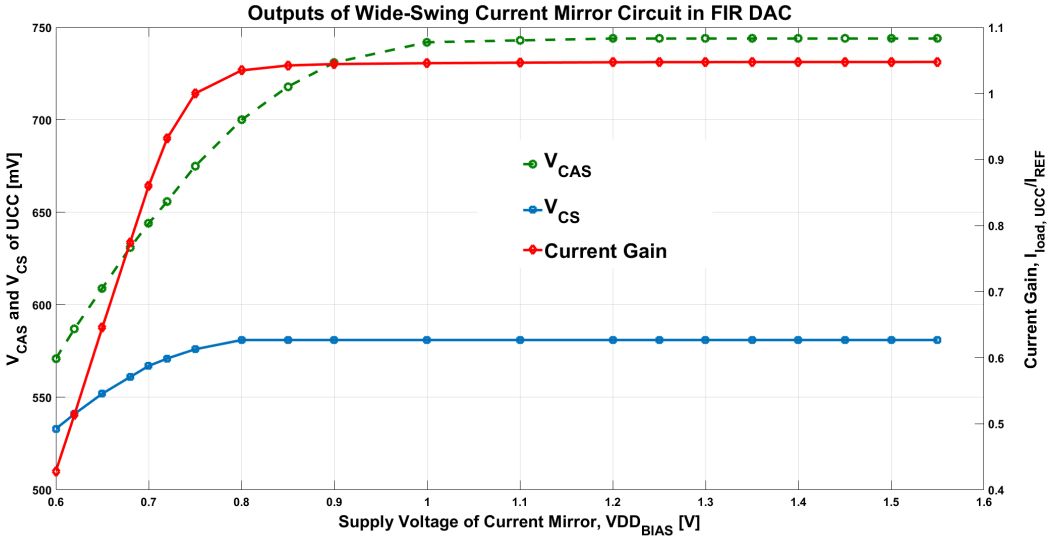


Figure 7.7: The biasing voltages of the current source of the UCC, and the current gain, $\frac{I_{UCC}}{I_{REF}}$, for different values of the biasing voltage supply. The current gain plat

There were wide-swing mirroring circuits in each of the quadrants of the UCC array. An additional replica circuit was used to generate the UCC current source biasing voltages—V_{CAS} and V_{CS}—for testing purposes. The measurement shown in Figure 7.7 is the values of these output UCC bias voltages.

As their name suggests, V_{CS} is the gate bias voltage of the current source transistor and V_{CAS} is the gate bias voltage of the cascode transistor of the current source of the UCC. The current flow is mainly controlled by V_{CS}. This value also sets the overdrive voltage which is critical to the value of random current source transistor threshold voltage mismatch used in design. Both voltages set the DC bias, output impedance of the cascode current source. Thus, it is important the circuit works where both the bias voltages are stable.

The current gain is estimated by dividing the measured total current flow in analog supply voltage to the product of the total number of UCCs in the 802.11ac, 4974, and the reference current, 2.7 μA. This measurement is independent of input signal type and clock frequency.

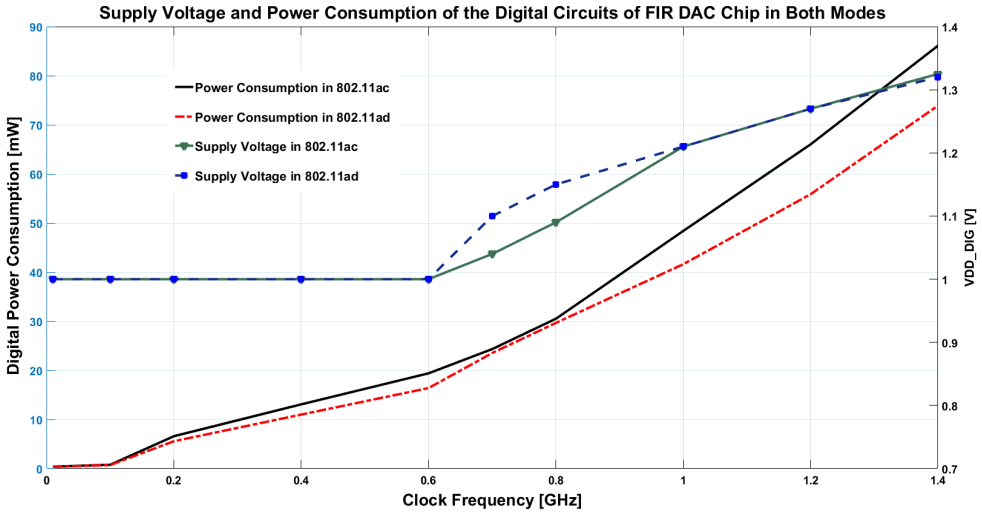


Figure 7.8: Power consumption of the digital circuits, supplied by VDD_{DIG}, of the FIR DAC chip at different clock frequencies in the 802.11ac mode and in the 802.11ad modes.

The result as can be seen in Figure 7.7 closely follows the transistor level simulation plot at the end of Chapter 6. The bias supply voltage, VDD_{BIAS}, is selected, as expected, at values where the current gain plateaus and the bias voltages are stable.

7.2.2 Power Consumption

The total power consumption of the chip in each mode of the FIR DAC chip is obtained by summing the power consumption of the digital circuits, which are supplied by VDD_{DIG}, the static current sources,

which are supplied by VDD_{ANA}, and the biasing circuits, whose supply is VDD_{BIAS}.

The digital part of the power consumption changes with frequency of the clock. In order to find the maximum average power consumption, the chip was run at the highest input bandwidth, up to $\frac{f_s}{2}$, at different clock frequencies. A PRBS input which has a pattern cycle period of $2^{23} - 1$ and a mark density of $\frac{1}{2}$ was employed as an input. The measured power consumption and supply voltages for the two modes of the chip up to 1.4 GHz clock frequency is plotted in Figure 7.8. As explained in sub-section 7.2.3 in this chapter, the digital circuit were run at higher supply voltages after 650 MHz. The value of the digital supply voltage is taken where no significant change in the current consumption of the digital circuits was observed. The circuit was run up to a maximum value of 1.325 V in 1.4 GHz as shown in Figure 7.8.

Table 7.1: Power Consumption of the FIR DAC chip in two modes

Part	Mode	Current	Voltage	Power Consumption
Digital Circuits at 600 MHz	802.11ac	19.4 mA	1 V	19.4 mW
	802.11ad	16.4 mA	1 V	16.4 mW
Digital Circuits at 1.4 GHz	802.11ac	65 mA	1.325 V	86.13 mW
	802.11ad	56 mA	1.32 V	73.92 mW
Analog Circuits	802.11ac	14.07 mA	1.2 V *	16.88 mW
	802.11ad	10.76 mA	1.2 V	12.91 mW
Biasing Circuits	802.11ac	51.3 μA †	1.2 V	61.56 μW
	802.11ad	51.3 μA	1.2 V	61.56 μW
Total Power Consumption at 600 MHz	802.11ac	**36.34 mW**		
	802.11ad	**29.37 mW**		
Total Power Consumption at 1.4 GHz	802.11ac	**103.07 mW**		
	802.11ad	**86.89 mW**		

As expected the power consumption of the digital circuits in the 802.11ad mode is lower owing to the smaller number of UCCs in this mode. It is also true that the consumption increases linearly with frequency: first in the 100 MHz to 600 MHz range for a constant VDD_{DIG} of 1 V, and then beyond 650 MHz. The effect of the small incremental changes in the digital supply voltage beyond 650 MHz is more pronounced in the 802.11ad power consumption.

Similarly, the consumption of the analog current sources is higher in the 802.11ad mode than the 802.11ac mode. It shows a proportional increase, independent of the clock frequency or type of input signal, due to the fact that the number of unit current sources in the 802.11ac mode are approximately 1.3 times those in 802.11ad mode. The results are shown in Table 7.1. Although the power consumption

* Actually, ≈ 1.9 V including IR-drop in 50Ω common mode resistor † For a 2.7 μA reference current

contribution from the biasing circuits is minimal, their power consumption is also tabulated in Table 7.1. The power consumption of the biasing circuits are the same for the two modes.

The table also contains total power consumptions for both the 802.11ac and the 802.11ad modes. Two results at two clock frequencies, 600 MHz and 1.4 GHz, are shown to put the change in the digital supply voltage in perspective.

Finally, when the measured power consumption at 1.4 GHz is compared with the simulated values, it has almost doubled. For example, a total power consumption of 115 mW from a 1 V digital supply was simulated in the 802.11ac mode at 3.52 GHz clock frequency. If the power consumption contribution from the digital circuits was adjusted to 1 V assuming the same current is drawn, as with the 1.325 V supply, at 1.4 GHz, the consumption would still be higher by around 50% compared to the simulated value. Similar comparisons can be made in the 802.11ad mode.

7.2.3 IEEE 802.11ac Mode

In this sub-section, sub-GHz clock frequencies were used to test the FIR DAC. The tests with clock frequency beyond 650 MHz are included in the last part. The data driver circuits of the FIR DAC were not operating at the GHz speeds for a digital supply voltage of 1 V. This was ascertained by observing the time domain output signals at near 1 GHz clock frequencies where some of the outputs values was achieving expected swing albeit at lower update rate during a test with known input sequences. The simulation results showed functionality up to 3.52 GHz with a PRBS $DATA$ at a digital supply voltage of 1 V. The possible source of this problem is increased capacitive loading on the outputs of the $DATA\ DRIVERS$ than what was expected during chip simulation. This could have resulted from less accurate models. Moreover, the transistor flavor used for the implementation of the digital circuits might not have the expected high frequency functionality. This problem was remedied by increasing the digital supply voltage up to 1.325 V depending the clock frequency.

Performance of the DAC for a Wideband Modulated $DATA$

In this mode, the bandwidth of the filter is set to $\frac{f_{CLK}}{22}$. The output of the FIR DAC for a QPSK modulated OFDM 802.11ac signal at a clock frequency of 600 MHz is shown in Figure 7.9. The signal is generated with a frequency plan of 3.52 GHz at the FIR DAC using Matlab®. Thus, the bandwidth of the actual measured signals is approximately 27.3 MHz.

As explained in Chapter 5, the raising quantization noise is canceled by the roll-off in the filter transition band. The quantization noise is reduced by almost 40 dB for the 600 MHz clock frequency. Besides, it can be seen that the ripple in the desired band has changed due to the NRZ clocking used in

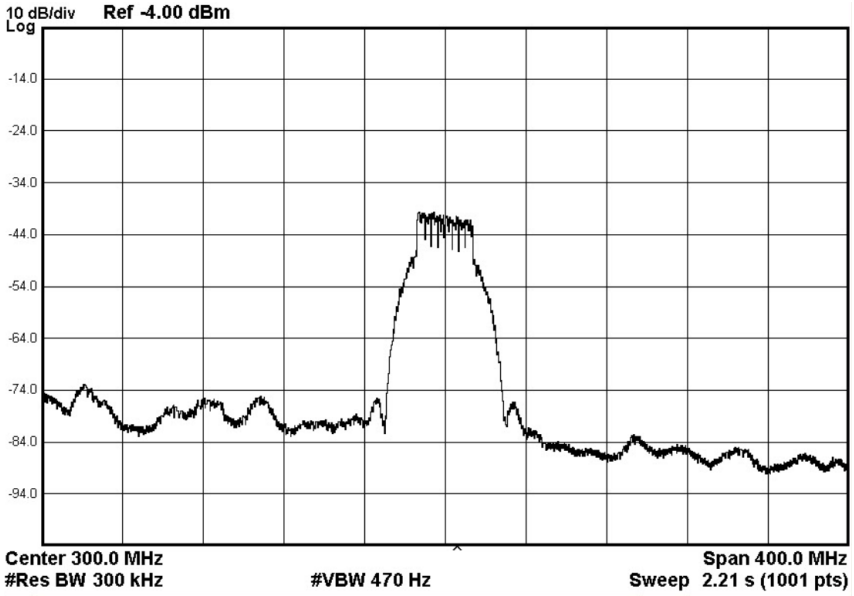


Figure 7.9: Output of the FIR DAC for a ΔΣ input in the 802.11ac mode. It is measured at a clock frequency of 600 MHz.

the FIR DAC. The output of the FIR DAC experience a $\frac{sin(x)}{x}$ attenuation across the desired band. This introduces a ripple in the passband which degrades the desired spectral flatness. The smaller the desired bandwidth, the smaller the ripple due to the holding nature of the clock. The effect of this for a bandwidth of 27.3 MHz at a 600 MHz clock is about 1.6 dB as can be seen in Figure 7.9.

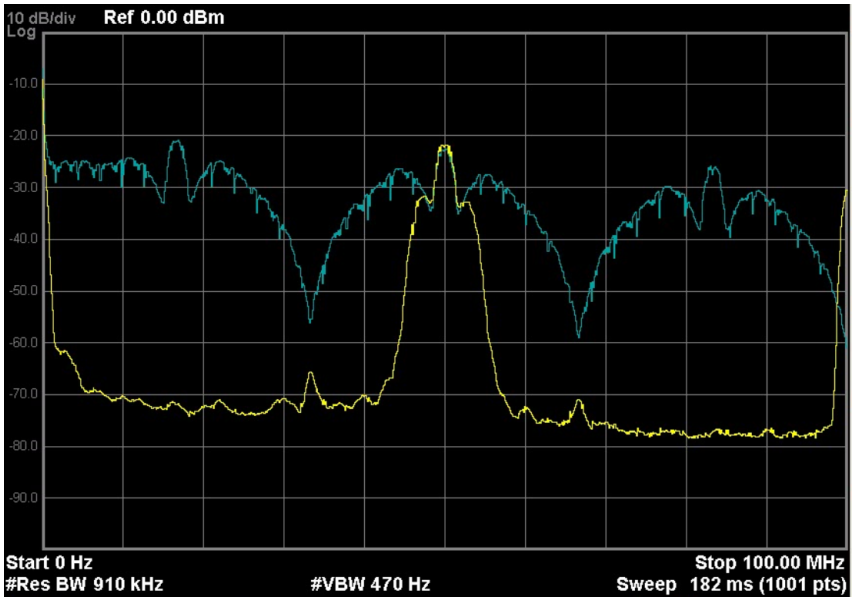


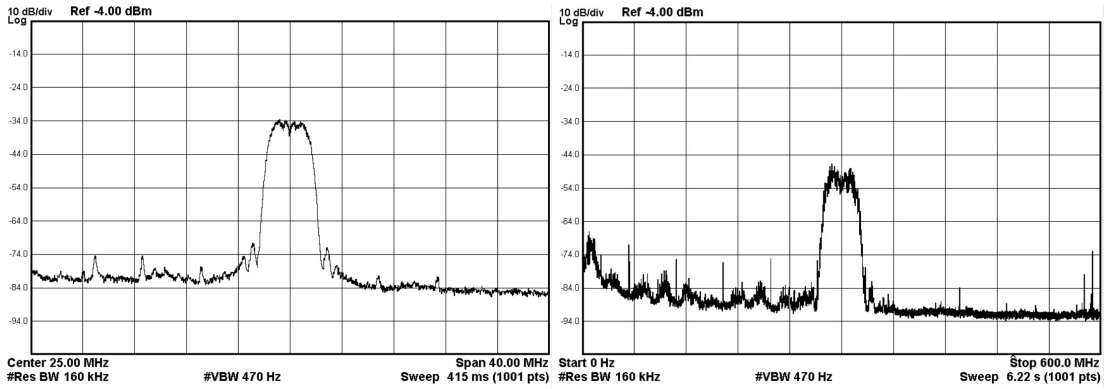
Figure 7.10: Output of the FIR DAC for a thrice oversampled ΔΣ input in the 802.11ac mode. It is measured at a clock frequency of 100 MHz.

To further demonstrate the functionality for modulated signals, the chip is tested with a smaller bandwidth ΔΣ modulator output. The same modulated signal from the first test is oversampled by three at the output of the ΔΣ modulator and frequency translated with the transmitter model shown in Figure 7.5.

The FIR DAC is expected to have a bandwidth of 4.54 MHz output at 100 MHz clock. However, the input is only $\frac{1}{3}$ at 1.51 MHz. The filter attenuates the images as can be seen in Figure 7.10 with the ΔΣ modulator input superimposed on the output. Besides, a power level of -18 dBm is reached with a reference current of 3.2 μA. The input is plotted by DC blocking the Matlab®-generated pattern.

Characterization as a Filter with PRBS *DATA*

The FIR DAC 802.11ac mode was further characterized with a 1-bit PRBS data which has a pattern cycle period of $2^{23} - 1$ and a mark density of $\frac{1}{2}$. The data is generated using a Tektronix® DTG 5334 data timing generator. The test was carried out at different clock frequencies.



(a) (b)

Figure 7.11: Filtered output at 50 MHz and 600 MHz clock of a PRBS input generated from the DTG

The output for a 600 MHz clock is shown in Figure 7.11. Normally, an attenuation close to 55 dB at $0.6f_s$ is expected. However, due to device mismatch reducing the effect of the small-valued coefficients on the transfer function, the filter attenuates by only 40 dB.

This test can be used to characterize the dynamics of the transfer function of the FIR DAC with clock frequency. A transfer function is defined by its passband ripple, stopband rejection and the width of the transition band. This PRBS input can be used to observe how one or all of these parameters of the transfer function are affected.

The supply voltages and the reference current are fixed at the values shown in Figure 7.2a. The input is data is clocked at a ratio of $\frac{1}{11}$ of the FIR DAC update rate. This odd multiple of the OSR, 22, is selected so that the desired band at $\frac{f_s}{2}$ is always flat across different update rates of the FIR DAC. During

measurement of the output, the resolution bandwidth is scaled proportional to the update rate of the FIR DAC to exclude any reading differences.

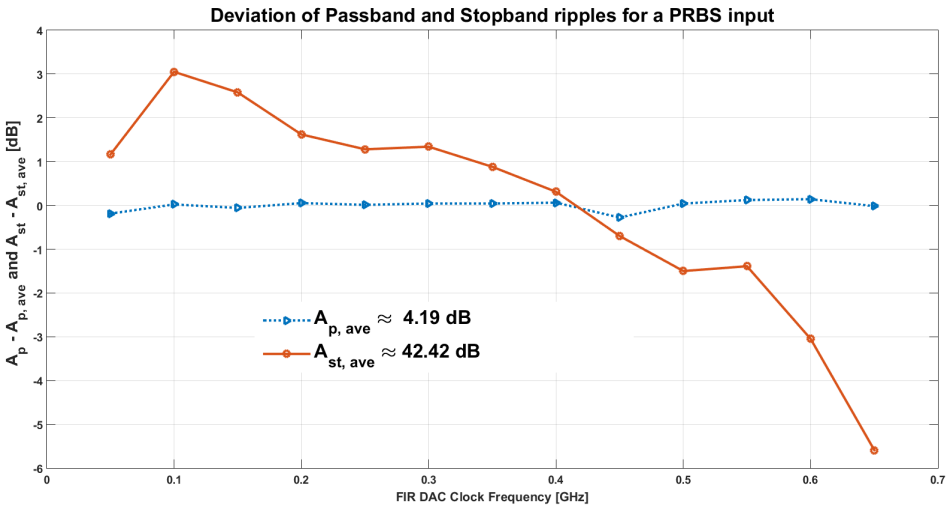


Figure 7.12: Passband AND Stopband ripple deviations for a PRBS input in the 802.11ac mode

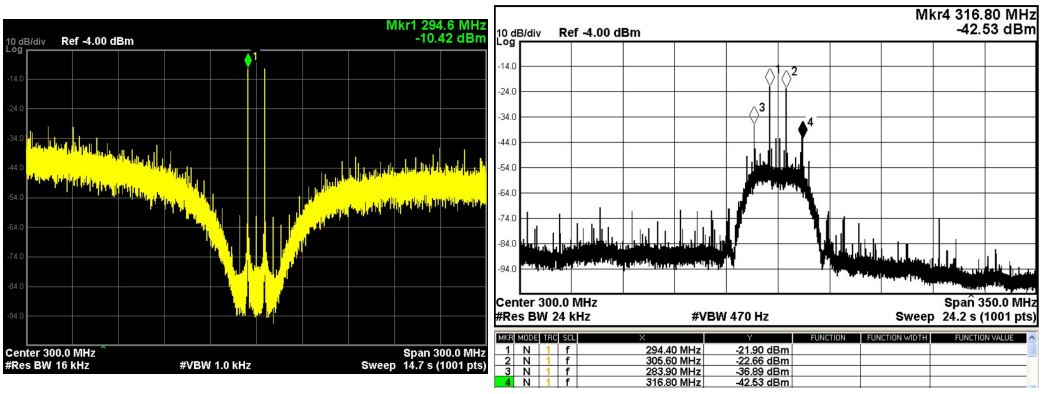
The output PRBS passband and stopband ripples were recorded from 50 MHz to 650 MHz update rates, clock frequencies of the FIR DAC. The change of these ripple from their mean values are shown in Figure 7.12. It can be observed that the passband ripple across a wide range of update rates stay flat whereas the stopband ripple varies by almost 9 dB.

The change in the stopband ripple was caused by slow decrease in the power of the passband when the clock frequency of the FIR DAC increases. The actual stopband power stays constant, only the rejection changed. This can be expected as the static parameters, those that cause change in coefficient values, are constant. The result in Figure 7.12 is then an indication of the failure of the output node of the current sources of the FIR DAC to charge and discharge fast enough to achieve the maximum output swing at each cycle of the clock.

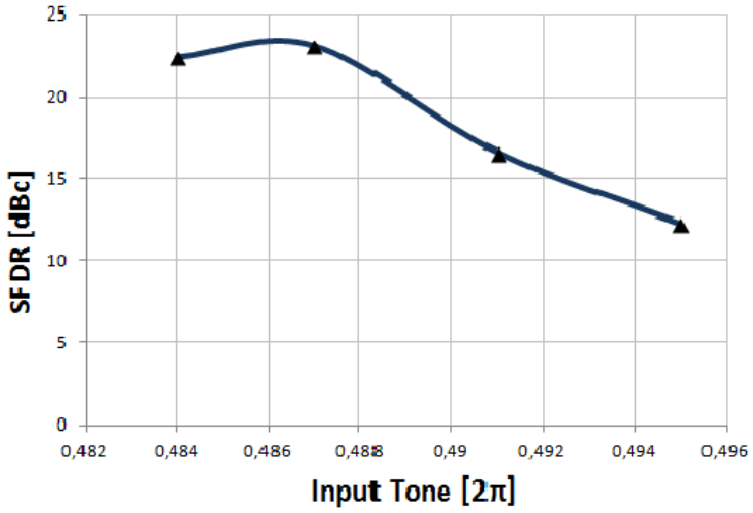
Characterization of Dynamic Performance

It is customary to use single tones sinusoidal waves for DAC dynamic performance measurement. The signals can be filtered to a degree where the noise floor of the input sinusoid is not higher than the noise floor of the spectrum analyzer. While it is fairly straightforward to do that when the input is multi-bit, it becomes harder to generate 1-bit test signals. This is because a $\Delta\Sigma$ modulator has to be used for converting the multi-bit low noise single-tone signal to a stream of 1-bit input data. The SNR of the 1-bit data depends on the SNR of the modulator used. For our case, only a 3^{rd}-order modulator was used, i.e.

a theoretical maximum SNR of 53 dB. This degrades the output spectrum due to additional mixing of the unneeded tones in the passband of the modulator output.



(a) (b)



(c)

Figure 7.13: The signal used as an input for this experiment, b) The measured plot, and c) SFDR in dBc in the bandwidth of the FIR DAC for a clock frequency of 600 MHz.

A measurement result for a 600 MHz clock shows the SFDR in the bandwidth of the filter, $(\frac{f_s}{2} - \frac{f_s}{22})$ to $(\frac{f_s}{2} + \frac{f_s}{22})$, is approximately around 15 dBc in the first Nyquist zone, and almost 20 dBc in the second. The difference is due to ZOH response. The value of the SFDR across the bandwidth is not different from the one shown for a 32 MHz baseband sinusoid. In Figure 7.13c, SFDR with four different input tones is plotted for a 600 MHz clock frequency. It shows the SFDR further degrades by almost 10 dB across the filter bandwidth.

7.2.4 IEEE 802.11ad Mode

In this mode, the bandwidth of the filter was set to $\frac{f_{CLK}}{2}$ by connecting the SEL input to ground. The setup from Figure 7.2a is also used here except the analog supply voltage is decreased to 1.6 V. This is because the full-scale output current decreases in this mode and the switch transistors of the current sources in the UCCs has to be protected from drain-to-source over-voltage.

To test the chip as a DAC in the 802.11ad, the 1-bit input data has to be upsampled by two as indicated in the transmitter architecture discussed in Chapter 5. For the high pass FIR DAC circuit implemented in this work, the input has to be mixed and upconverted so that the center of its bandwidth lies at $\frac{f_s}{2}$. For a truly random signal, this process does not change the frequency characteristics of the signal. Hence, a PRBS signal clocked at the update rate of the FIR DAC is employed for characterizing the chip in this mode of operation.

Characterization of Channelization of PRBS *DATA*

A measurement is conducted to show the filtering characteristics in this mode. The measurement result in Figure 7.14 was carried out at 200 MHz clock frequency and the same speed PRBS input data from the data timing generator.

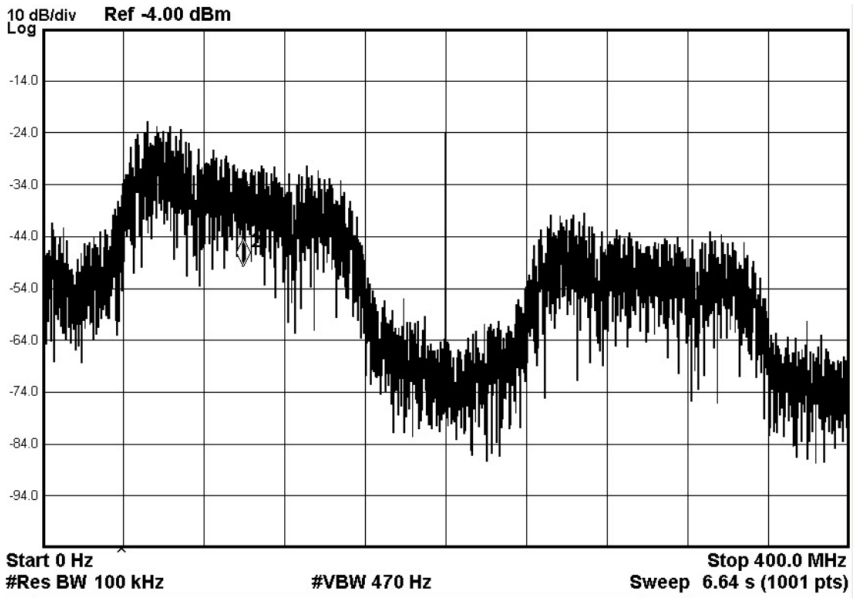


Figure 7.14: Filtered output at 200 MHz clock in the 802.11ad mode for a PRBS input generated from the DTG

As can be seen, the broadband response of the FIR DAC in this mode is observed. However, the effect of the $\frac{sin(x)}{x}$ response of the clock is more pronounced in this mode than in 802.11ac. The passband

ripple increases by around 10 dB due to only the ZOH behavior of the clock.

The large clock feedthrough observed in Figure 7.14 normally should be at a level which is a fraction of the maximum output swing. In this case, it tends to be on the same power as the frequency components in the passband of the FIR DAC.

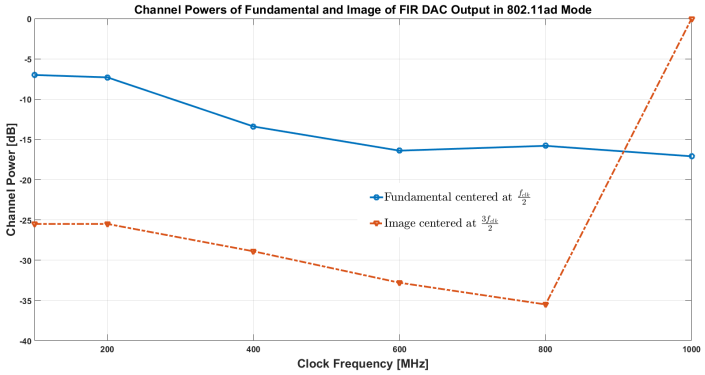


Figure 7.15: Filtered output at 200 MHz clock in the 802.11ad mode for a PRBS input generated from the DTG

Tests even at more than 1 GHz clock frequency has been done, the response degrades further with the added problems observed during measurement of the 802.11ac mode. The measured channel powers of the fundamental and the first image output is shown in Figure 7.15. Although the 802.11ad have higher channel power at the same clock frequency than the 802.11ac, given its broadband operation, the performance is limited to a maximum clock frequency of 1.4 GHz. This is observed by increasing the digital supply voltage up to 1.55 V.

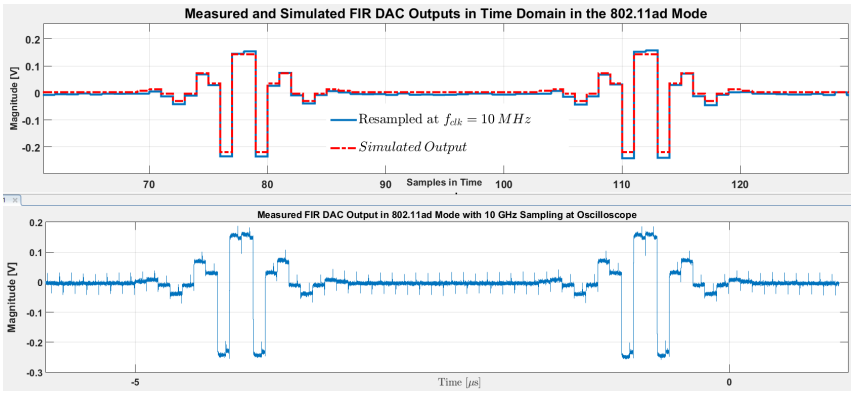


Figure 7.16: Time domain measurement for an input sequence at a clock frequency of 10 MHz.

To mitigate the problem of ZOH, other DAC responses can be used. An RZ-clocked DAC has a flatter response near $\frac{f_s}{2}$ than an NRZ one as discussed in Chapter 4. Unfortunately, this case was not

tested in this implementation.

Another mechanism is to select the output at the first image. One reason for this is that there is less passband ripple at around $1.5f_s$ as the NRZ response of the FIR DAC plateaus at the middle of the first side lobe. Another advantage for selecting this image is to obtain a higher carrier frequency for transmission. However, this comes at a cost. One disadvantage is that output has a large power reduction as the lobes of the $\frac{sin(x)}{x}$ response of the FIR DAC decrease by more than 10 dB at around $1.5f_s$.

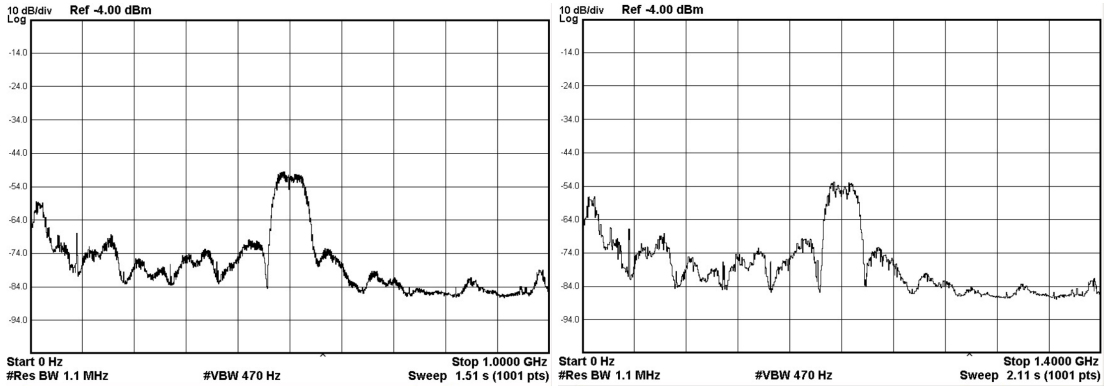
Characterization of Impulse Response with Known Sequence

The 802.11ad mode unit coefficient is scaled 20 times the 802.11ac mode unit coefficient. For this reason the impulse response of the 802.11ad have bigger sized coefficients, and it is easier to measure even with low reference current values. Since this measurement is strictly about the coefficient sizes, it is measured at lower clock frequencies to avoid effect of high frequency dynamic errors.

The output of the FIR DAC in the 802.11ad mode for a repetitive 34 sample sequence, given as:

$$Data = \Big\{1, 1, 0, 0, \ldots, 0, 0\Big\} \tag{7.1}$$

is shown in Figure 7.16. The simulated resulted, from Matlab, is shown in red. The measured result is shown in the second plot. The oscilloscope samples this input at 10 GHz. The superimposed plot at the top is obtained by downsampling the measured data points fro 10 GHz to the clock frequency of 10 MHz. As can be seen, the measured data trace almost exactly as the simulated one; they have equal peak-to-peak voltages, and also their periods are the same. This shows that the static part of the FIR DAC is working as expected at least at 10 MHz clock frequency.



(a) (b)

Figure 7.17: Filtered output at 1 GHz and 1.4 GHz clock frequencies of a PRBS input generated from the DTG

7.2.5 Characterization of the FIR DAC for f_{CLK} beyond 600 MHz

Tests were carried out with increased digital supply voltage. In the 802.11ac mode, PRBS data was used to check the output power performance of the chip at 1 GHz and 1.4 GHz. As can be seen in Figure 7.17, the output swing of the UCC drops fast as the update rate increases. For a 1 GHz clock rate, the power spectral density is barely crossing -54 dBm/1.1 MHz.

Decreasing the input bandwidth does improve the filtering performance of the chip. In Figure 7.18, the output power reaches a -44 dBm/3 MHz spectral density across the bandwidth.

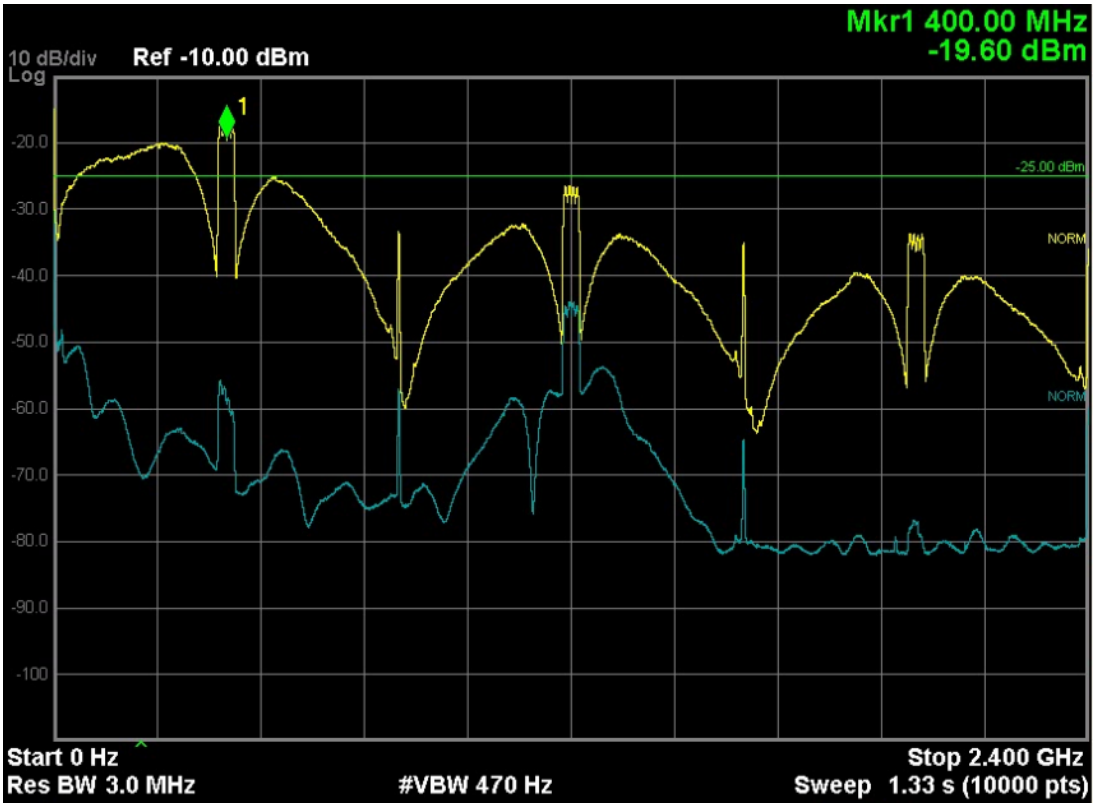


Figure 7.18: Output of the FIR DAC for a thrice oversampled ΔΣ input in the 802.11ac mode. It is measured at a clock frequency of 2.4 GHz. The input digital pattern *DATA* from the data timing generator is shown in yellow, and the measured output in blue.

Measurement with ΔΣ output as the input *DATA* to the FIR DAC were carried out by increasing the digital supply voltage further up to 1.55 V. Figure 7.19 shows the channel power, ACPR and alternate CPR across different clock frequencies for this type of input. We can see that the standard requirement of 11 dBc ACPR is barely fulfilled almost at all frequencies. However, the alternate CPR requirement of 27 dBc for a 160 MHz channel is only met up to around 1 GHz clock frequency. It must be noted that, though, the measured channel bandwidth is less than 160 MHz. A maximum channel power of -14 dBm

is obtained at sub-100 MHz clock frequencies.

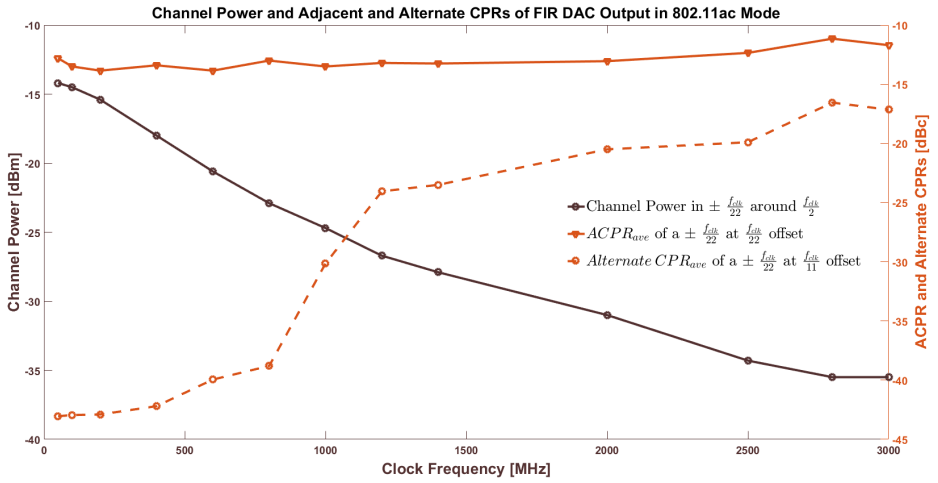


Figure 7.19: Channel power, ACPR, and alternate CPR measurements across different clock frequencies for a ΔΣ output pattern as an input to the FIR DAC in the 802.11ac mode.

The out-of-band profile of the FIR DAC in the 802.11ac mode with he same ΔΣ input data is plotted in Figure 7.20. Two plots of out-of-band attenuation from baseband to $\frac{f_s}{2}$ and from $\frac{f_s}{2}$ to f_s are shown. The third plot indicates the difference between these two plots to quantify the effect of ZOH holding on the out-of-band performance across different clock frequencies. Although its effect on the passband is less significant, it can be seen that the out-of-band profile experiences up to 14 dB difference between the fundamental and images stop bands.

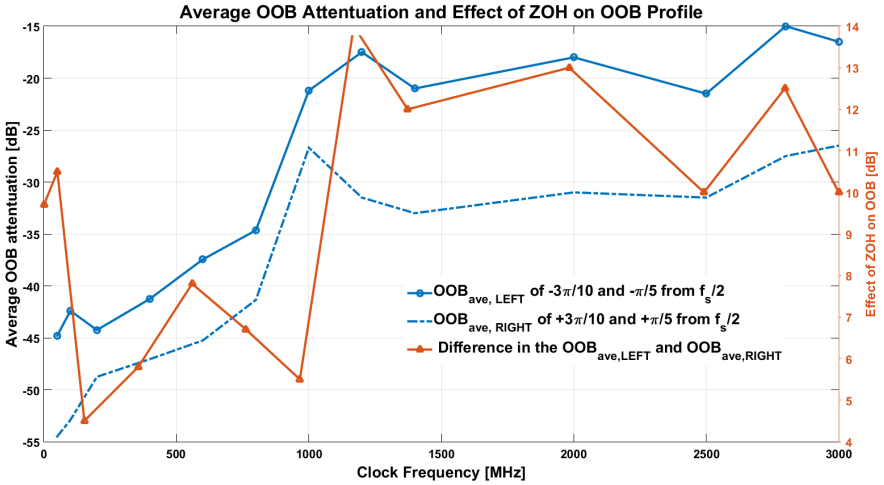


Figure 7.20: Out-of-band profile of the fundamental and image stop bands measured at two points for a ΔΣ output signal as an input. The effect of ZOH clocking on these two stop bands is also shown.

7.2.6 Comparison with the State of the Art

In this subsection, the performance of the test chip is compared with other digital-to-RF converters targeting low power all-digital wireless transmitters. Some of the interesting differences are tabulated in Table 7.2.

Table 7.2: Comparison with the state of the art in digital-to-RF converters of all-digital transmitters

REF.	Tech.	Type of DAC	Mode	Max. BW [MHz]	Max. f_s [MHz]	Max. f_{out} [MHz]	Max. P_{out} [dBm]	P_{Cons} ‡ [mW]
[Ala+14]	65nm CMOS	RF DAC	—	154.1	3500	2400	22.8	—
[Tal+08]	0.25μm CMOS	FIR RF DAC	—	15	250	1062	-5.4	122
[McC+15]	130nm SiGe CMOS	TI $\Delta\Sigma$ RF DAC	BP	50	2000	510	-4.5	55
			HP			990	-7.5	
This Work	**28nm CMOS FDSOI**	**HP FIR DAC**	**11ac**	**136**	**3000**	**1500**	**3.93**	**103.07** §
			11ad	**700**	**1400**	**700**	**1.61**	**86.89** §

It can be seen that, the work outperforms in processing wideband signals, up to 700 MHz in the 802.11ad mode. This bandwidth is measured with a clock frequency of 1.4 GHz. In the 802.11ac mode, higher clock frequency, a maximum of 3 GHz, are reached by increasing the digital supply voltage. However, due to the medium bandwidth targeted with this mode, the input signal bandwidth is limited to 136 MHz.

The advantage of the high pass FIR DAC structure over the LPF and BPF structures is its ability to achieve higher carrier frequency for the same clock speed. A maximum output carrier frequency of 1.5 GHz in the 802.11ac mode and 700 MHz in the 802.11ad mode.

The output power is reported for the full-scale current at a 50 Ω output load network. The output swing is improved compared with what is reported in the other works with an exception to the value reported in [Ala+14] where a combining output network is used to reach a peak output power of 22.8 dBm.

Although this work is expected to take advantage of technology scaling to lower the power consumption, it suffers from increased number of UCCs. This is mainly due to the targeted out-of-band noise profile of -60 dBr required up to 4974 UCCs. The power consumption values in the table are at a clock frequency of 1.4 GHz. The power consumption for measurements with a wideband OFDM input signal

§ $f_{CLK} = 1.4GHz$ ‡ P_{Cons} = Total power consumption

tend to plateau when the clock frequency increases to its maximum value of 3 GHz.

Table 7.3: Performance summary of the configurable FIR DAC

Parameter	**802.11ac mode**	**802.11ad mode**
Bandwidth	$\frac{f_s}{22}$	$\frac{f_s}{2}$
Maximum Output Carrier Frequency	1500 MHz	700 MHz
Maximum Measured Input BW	136 MHz	700 MHz
Full-Scale Output Current, I_{REF} = 2.7μA	14.07 mA	10.76 mA
Power Consumption at 1.4 GHz	103.07 mW	86.89 mW
Total Number of UCCs	4974	3804
Clock Speeds, f_s	$10MHz \leqslant f_s \leqslant 3GHz$	$10MHz \leqslant f_s \leqslant 1.4GHz$
Supply Voltages	VDD_{DIG} VDD_{BIAS} VDD_{ANA} 0.6 to 1.55 V 1.2 V 1.2 V	
Hardware Sharing	98% 802.11ad UCCs used in 802.11ac	
Maximum Stopband Rejection	55 dB in 802.11ac mode	
Output Load Network	50 Ω differential probes	
Clock and Data Input	Single-ended, 50 Ω to ground	
Die Packaging	QFN40 plastic package	
Active Circuit Area	0.83 mm^2	
Transistors Used	Regular V_{th}	
Technology	28nm CMOS FDSOI	

7.3 Conclusions

A summary of the measurement results of the FIR DAC chip is presented in Table 7.3. The maximum input bandwidth for 802.11ac mode is at a clock frequency of 1.4 GHz for a PRBS input shown in Figure 7.17b. It would have strengthened the claim to present EVM results, but it has not been possible to carry out these measurements so far. For the 802.11ad, the maximum input bandwidth is at 600 MHz clock frequency. Nonetheless, the circuit can operate in the 802.11ac mode up to clock speeds of 2.4 GHz starting at a 1.325 V digital supply voltage. Further tests at higher supply voltages were not carried out at the moment. The chip has also functionality up to 1.4 GHz in the 802.11ad starting at a digital supply voltage of 1.325 V.

In the 802.11ac mode, results are obtained at digital supply voltage as low as 0.6 V. As expected,

this happens when the data and clock signal levels are scaled to the corresponding VDD_{DIG} level and at frequencies below 100 MHz. Further tests with varying digital supply voltage were not possible at this moment.

One observation common to all cases of measurement was the robustness of the circuit to delay difference between the $CLOCK$ and $DATA$ signals. The delay could be varied up to 5 ns with the data timing generator. The circuit was tested with a $\Delta\Sigma$ modulator output signal where the input $DATA$ was delayed, sweepingly, from 0 ns upto $\frac{1}{2f_s}$. The circuit was able to deliver expected output even when the input pattern was run for a fixed number of loops. The reason for this is the robustness of the digital delay line against set-up time errors.

There are many conclusions that can be drawn for the measurements presented in this chapter. Despite the fact that the measurement results differ from the theoretically expected results, the validity of the configurable FIR DAC concept is shown. The concept of digitally switching unit current sources and summing them in analog to implement a DAC with different filtering behavior is validated.

While the static part of the FIR DAC circuit has worked reliably. The expected parametric results in the dynamic parts of the circuit were not obtained. Common to both modes is the failure in high clock frequency. The contribution of technology maturity is not to be underestimated, but there are also some improvements that should have been made in circuit implementation that could have decreased the noise level observed in the single-tone measurements results.

The next chapter will include some recommendations for improving the performance of configurable, high speed, high resolution FIR DACs.

Chapter 8

Conclusions and Future Directions

Conclusions

This work provides theoretical analysis, simulation-based validation of FIR DAC based circuits and transmitter architectures. Besides, a prototype chip is measured to validate the use of FIR DAC for multi-standard transmitter implementation. The circuit is tested to work up to a clock frequency of 3 GHz in the medium bandwidth mode while consuming a power consumption of 108.9 mW. It is also characterized in the wide bandwidth mode up to a clock frequency of 1.4 GHz while consuming 86.89 mW of power.

Future Directions

Some recommendations are listed below to improve the multi-mode FIR DAC circuit to achieve a state-of-the-art performance at multi-GHz digital-to-RF conversion.

- As discussed in Chapter 6, the data drivers were placed on one-side of the UCC array. A discussion was included on the possible bandwidth limitation that could result due to parasitic loading. To solve this problem, another set of data driver can be inserted in the middle of the UCC array. There will not be a significant increase in power consumption as the load is divided. Similar technique can be followed for the clock. Additional set of driver can be inserted in the $CENTER$ of the UCC array to balance the delay between two UCC at each end of the clock line.

- As mentioned in the Chapter 7, the output of the HP FIR DAC suffered from the ZOH nature of the clocking used. To improve this, the FIR DAC UCC can be redesigned for an RZ implementation, or better yet other types of implementation which have a peak at around $\frac{f_s}{2}$.

- The FIR DAC circuit area can be improved by designing a UCC which exploits the symmetry that exists in a linear-phase FIR filter impulse response. The obvious method is to use some decoding logic to reuse the same UCC. The way this works is that the UCC is turned-off when the two coefficients have opposite data values and works normally for the other two cases. To turn-off the

UCC, the current source or the two switches can be turned-off. Thus, there will be two control signals for each tap. However, this can affect the speed that can be reached and, more importantly, distortion may be caused due to mismatches on the timing of turn-off and operation of UCC.

To decrease this distortion, an easier way is to redesign the UCC to have three switches to smoothly transfer I_{UCC} into two output and one additional redundant branches for the possible combination values of two taps i.e. -2, 0, and 2. However, still two control signals are needed.

- The clock and data signals are on metal layers four and ten respectively. This prevents cross-talk. However, to separate them, the placement method has to change. A new placement which maintains the strengths of the pseudo-double common centroid placement method, but separates the digital and analog grounds, crossing of digital signals among other things can bring improvement.

- There are works at multi-GHz frequencies that embedded filtering in a DAC. However, the FIR DAC structure is yet to be reported at those frequencies. Had there been one, it would have been a good reference for comparing a 1-bit, N-tap digital-to-RF processor performance against a traditional L-bit, 1-tap DAC. Transistor level simulation of the work reported in [GFK15] showed promising results. A demonstrator chip of the system-level findings in that paper could provide the reference work to appraise the strengths and weakness of the FIR DAC approach.

- A final recommendation is on the general FIR DAC structure. It would be interesting to quantitatively compare the three structures presented in Chapter 4: L-bit, N-tap; 1-bit, N-tap; and L-bit, 1-tap.

Appendix

.1 Transmitter Chain Simulation in Matlab

The matlab code given here is used for simulation of the transmitter chain in Chapter five. The function is also used improved for generating the patterns used in the test of the prototype FIR DAC chip in Chapter seven.

There may be some codes here and there that are mistakenly commented or some values which were chosen for some particular frequency plan, but generally the code can be easily improved to be used for a DSP of transmitter chain simulation.

Unfortunately, the other codes that has been written for each block of the transmitter are not included here. Hopefully, they will available somewhere sometime.

.1.1 IEEE 802.11ac Transmitter Baseband

```
function [SigAnalogOut, ACPR, SpecFlat] =  TxModel_THESIS(SigType, Fs, Order, NTFGain, QBits, topo
% function [SigAnalogOut] =  TxModel(SigType, Fs, Order, NTFGain, QBits, topo, Coeff)
%%
%   Test case - [SigAnalogOut, SigDelSigOut] = TxModelWiFi(real(SigWiFi)/max(real(SigWiFi)), [], 8
%   Modified to [SigAnalogOut, ACPR, SpecFlat] = TxModelWiFi(real(SigWiFi), [], 160e6, 11, 1/(11*8
%   For EVM simulation: [SigAnalogOut, ACPR, SpecFlat] = TxModelWiFi([], [], 160e6, 11, 1/(11*80)
%   Generate a Signal with the input characteristics
%   SigIn = TestSignals(SigType, 50, 1, Fsig, Fs);
%   Fsig = [];      % was useful when generating input signal within this function for single-tone
%%#########################################################################################################
close all;
Fs_Original = Fs;
Fs = 320e6;                             % After HBF, Frequency of operation is 320MHz mode
OSR = 11;
OSRDS = 11*Fs/(1*Fs_Original);          % Fixed for Fs = 320MHz * 11 = 2*1.76GHz, WiGig Fs
GrpDelay_DS = 5;                        % 6 for optimized CRFB, 170 for CIFB and others
FIRDLY = grpdelay(Coeff);
FIRDLY = ceil(max(FIRDLY(1:22)));
N_OFDM = 12;                            % OFDM BITS = 3 + 0.5*log2(512/3*(M-1)), M is constellatin

```

```
%% Scale Input to amplitude of maximum delta-sigma SNR
AmpFS = 0.9;                                % what if the quantizer full scale were 2, 0, -2?
SigInReal = (real(SigType).*AmpFS)./max(abs(SigType));
SigInImag = (imag(SigType).*AmpFS)./max(abs(SigType));
% SigInReal = real(SigType);
% SigInImag = imag(SigType);
%% Quantize to N_OFDM bits
SigInRealQuant = round(SigInReal/max(abs(SigInReal)) * (2^(N_OFDM)-1));
SigInRealNBit = SigInRealQuant*(max(abs(SigInReal))/max(abs(SigInRealQuant)));
SigInImagQuant = round(SigInImag/max(abs(SigInImag)) * (2^(N_OFDM)-1));
SigInImagNBit = SigInImagQuant*(max(abs(SigInImag))/max(abs(SigInImagQuant)));
%%

%% Interpolation for 20MHz, 40MHz and 80MHz using half-band filters
if ismember(Fs_Original, [20e6, 40e6, 80e6, 160e6])
    [SigInRealHF, SigInImagHF] = InterpolateTo320(SigInRealNBit, Fs_Original, SigInImagNBit);
%     [SigInRealHF, SigInImagHF] = InterpolateTo320(SigInReal, Fs_Original, SigInImag);
end
%% Quantize to N_OFDM bits
% [SigInRealHF,B] = interp(SigInRealHF,OSR);
% BNor = B/sum(B);
% SigInRealHF = filter(BNor,1,[SigInRealHF,zeros(1,grpdelay(BNor))]);
% SigInRealHF = SigInRealHF(grpdelay(BNor)+1:end);
SigInRealQuant = round(SigInRealHF/max(abs(SigInRealHF)) * (2^(N_OFDM)-1));
SigInRealHFNBit = SigInRealQuant*(max(abs(SigInRealHF))/max(abs(SigInRealQuant)));
%% Quantize to N_OFDM bits
SigInImagQuant = round(SigInImagHF/max(abs(SigInImagHF)) * (2^(N_OFDM)-1));
SigInImagHFNBit = SigInImagQuant*(max(abs(SigInImagHF))/max(abs(SigInImagQuant)));
%%
%%
%% Interpolate
% [SigShapedR, ~] = OverSample(SigInReal, OSR);     % Zero-Order-Hold
ZOH = ones(1,OSR);
SigInRealUP = upsample(SigInRealHFNBit,OSR);
% SigInRealUP = upsample(SigInRealHF,OSR);
SigShapedR = filter(ZOH,1,[SigInRealUP,zeros(1,ceil((OSR-1)/2))]);
% Zero-Order-Hold delay compensation
SigShapedR = SigShapedR(ceil((OSR-1)/2)+1:end);
%%
%% Delta Sigma Modulator with Delay Compensation
FuncDelSig.OSR = OSRDS;       % OSR decreases -> SNR decreases, but -> delta-sigma NTF curve is fu
```

```
61  FuncDelSig.Fs = Fs * OSR; FuncDelSig.Name='DeltaSigma'; FuncDelSig.Order = Order; FuncDelSig.topo
62  SigShapedR = [SigShapedR,zeros(1,GrpDelay_DS)];
63  [SigDelSigOutR] = DeltaSigma3rdOrder(SigShapedR, FuncDelSig);
64  SigDelSigOutR = SigDelSigOutR(GrpDelay_DS+1:end);
65  PlotFrequencyResponse(SigDelSigOutR, 3.52e9);
66  %% Semidigital FIR DAC
67  SigAnalogOutR = filter(Coeff,1,[SigDelSigOutR,zeros(1,FIRDLY)]);
68  SigAnalogOutR = SigAnalogOutR(FIRDLY+1:end);
69  %% For Q-part
70  % if isempty(SigType)
71  %     [SigShapedQ, ~] = OverSample(SigInImag, OSR);     % Zero-Order-Hold
72  %% ZOH phase compensation ZOH = [1, 1, 1, ...OSR times, 1]; grpdelay = (osr-1)/2;
73  SigInImagUP = upsample(SigInImagHFNBit,OSR);
74  % SigInImagUP = upsample(SigInImagHF,OSR);
75  SigShapedQ = filter(ZOH,1,[SigInImagUP,zeros(1,ceil((OSR-1)/2))]);
    % Zero-Order-Hold delay compensation
76  SigShapedQ = SigShapedQ(ceil((OSR-1)/2)+1:end);
77  %% Delta Sigma Modulator with Delay Compensation
78  SigShapedQ = [SigShapedQ,zeros(1,GrpDelay_DS)];
79  [SigDelSigOutQ] = DeltaSigma3rdOrder(SigShapedQ, FuncDelSig);
80  SigDelSigOutQ = SigDelSigOutQ(GrpDelay_DS+1:end);
81  PlotFrequencyResponse(SigDelSigOutQ, 3.52e9);
82  %%
83  SigAnalogOutQ = filter(Coeff,1,[SigDelSigOutQ,zeros(1,FIRDLY)]);
84  SigAnalogOutQ = SigAnalogOutQ(FIRDLY+1:end);
85  %% Scale Back to Original Magnitudes
86  SigAnalogOut.R = (SigAnalogOutR./AmpFS).*max(abs(SigType));
87  SigAnalogOut.Q = (SigAnalogOutQ./AmpFS).*max(abs(SigType));
88  % SigAnalogOut.R = SigAnalogOutR;
89  % SigAnalogOut.Q = SigAnalogOutQ;
90  %% ACPR simulation
91  [ACPR.QInter, ~, ~] = ACPRTest(SigShapedQ, ACPRPara);
92  [ACPR.QDelSig, ~, ~] = ACPRTest(SigDelSigOutQ, ACPRPara);
93  [ACPR.QSemi, ~, ~] = ACPRTest(SigAnalogOut.Q, ACPRPara);
94  %% SPECTRAL FLATNESS
95  [SpecFlat.Q] = SpectralFlatnessTxWiFi(SigAnalogOutQ, Fs_Original, OSR);
96  % else
97  %% ACPR Simulation Input Data
98  [ACPR.RInter, MainChPowerR, AdjChPowerR] = ACPRTest(SigShapedR, ACPRPara); %#ok
99  [ACPR.RDelSig, MainChPowerR, AdjChPowerR] = ACPRTest(SigDelSigOutR, ACPRPara); %#ok
100 [ACPR.RSemi, MainChPowerR, AdjChPowerR] = ACPRTest(SigAnalogOut.R, ACPRPara); %#ok
```

```
%%
[SpecFlat.R] = SpectralFlatnessTxWiFi(SigAnalogOutR, Fs_Original, OSR);
%% Output of three blocks on the same plot
% ScaleTXPower(SigAnalogOut.R, Fs_Original);     % Includes out-of-band noise profile
close all;
figure(1);
dBFactor =  30;                 % +30 for dBm
FreqFactor = 1e6;               % 1e6 for /MHz
% dBFactor =  0;                % +0 for dB
% FreqFactor = 1;               % 1 for Hz
[Pxx, Fxx] = pwelch(SigDelSigOutR,rectwin(length(SigDelSigOutR)),[],length(SigDelSigOutR),Fs*OSR,
plot(Fxx,10*log10(Pxx.*FreqFactor)+dBFactor,'LineWidth',1.5,'Color',[.1 .1 .9])
hold on;
[Pxx, Fxx] = pwelch(SigShapedR,rectwin(length(SigShapedR)),[],length(SigShapedR),Fs*OSR,'onesided
plot(Fxx,10*log10(Pxx.*FreqFactor)+dBFactor,'LineWidth',1.5,'Color',[.1 .9 .1])
hold on;
[Pxx, Fxx] = pwelch(SigAnalogOut.R,rectwin(length(SigAnalogOut.R)),[],length(SigAnalogOut.R),Fs*OS
% PxxMax(1) = max(10*log10(Pxx(length(Fxx)/2 + 1 : length(Fxx)/2 + length(Pxx)/(2*OSR)).*FreqFacto
% For centered plotting ... max for transmit mask taken over some Fbb samples range in dBm/MHz
% PxxMax(1) = max(10*log10(Pxx(1:length(Fxx)/(2*OSR))));
% For twosided plotting
PxxMax(1) = max(10*log10(Pxx(1 : length(Fxx)/2 + length(Pxx)/(2*OSR)).*FreqFactor)+dBFactor);
% For onesided
% if gt(PxxMax(1),1) || lt(PxxMax(1),-1)
% Scale power to set peak dB/Hz or dBm/MHz at 0
% Pxx = ((10^(-1*dBFactor/10))/(FreqFactor*max(Pxx))).*Pxx;
% PxxMax(1) = max(10*log10(Pxx(length(Fxx)/2 + 1 : length(Fxx)/2 + length(Pxx)/(2*OSR)).*FreqFacto
% end
%% Transmit Mask
if le(Fs_Original, 160e6)
    % TxMaskVector = [0, 9e6, 11e6, 20e6, 30e6, Fs-30e6, Fs-20e6, Fs-11e6, Fs-9e6, Fs; PxxMax(1),
PxxMax(1)]; %ieee802.11ac-20MHz Mask ... for twosided plotting
    TxMaskVector = [0, (Fs_Original/(2*1e6) - 1)*1e6, (Fs_Original/(2*1e6) + 1)*1e6, Fs_Original,
    plot(TxMaskVector(1,:), TxMaskVector(2,:), 'LineWidth',4,'Color',[.6 .1 .4]);
    axis([0 1.76e9 PxxMax(1)-130 PxxMax(1)+10])
% PlotFrequencyResponse(SigAnalogOut, OSR*Fs);
end
xlabel('Sampling frequency');
if FreqFactor==1e6 && dBFactor==30
    ylabel('PSD in dBm/MHz');
elseif FreqFactor==1 && dBFactor==30
```

```
137         ylabel('PSD in dBm/Hz');
138     else
139         ylabel('PSD in dB/Hz');
140     end
141     title('PSD of transmitted signal at Output of the WiFi Tx')
142     % legend('Delta-Sigma', 'Interpolation Filter', 'FIR DAC','Location','NorthEastOutside');
143     legend('Delta-Sigma', 'FIR DAC','Transmit Mask','Location','NorthEast');
144     end
```

.1.2 IEEE 802.11ad Transmitter Baseband

The 802.11ad transmitter is has a simple architecture with only an oversampling by two DSP block before the FIR DAC. Therefore, it is not included.

.2 EVM Simulation

.2.1 Code for EVM Simulation of 802.11ac

```
function [ SigRx, EVM, MER ] = EVMWiFi_THESIS( Coeff, Fs)
%EVMWiFi Simulates an OFDM system in WiFi IEEE802.11ac standard
%   Some blocks are not included to simlify the OFDM system for easy EVM estimation in the WiFi Tx
%   All channel bandwidths are can be simulated by choosing the right Fs.
%
%% Constants variables
SEL = 1+log2(Fs/20e6);
OSR = 11 * 320e6/Fs;                % oversampling by 11 in ZOH and x320/Fs in HBF
NcpALL = [16,32,64,128];            % Guard Interval 1/4*3.2us = 0.8us*Nsc/3.2us= or 0.8us*Fs = Sa
NscALL = [64,128,256,512];          % Total number of subcarriers for Fs
% NdscALL = [56,114,242,484];         % Number of data and pilot subcarriers
NdscALL = [56,114,242,468];
Ncp = NcpALL(SEL);
Ndsc = NdscALL(SEL);
Nsc = NscALL(SEL);
N = 16;                     % 16-PSK/16-QAM with N = 16
Nsym = 1;                   % Number of Symbols
Nsam = Ndsc*Nsym;           % Random data for simulation = integer multiple of Ndsc
%% Create Signals for each block output
SigZP = zeros(Nsc,Nsym);                % Zero padding Nsc-Ndsc = subcarriers
SigIFFT = zeros(Nsc, Nsym);
SigFFT = zeros(Nsc, Nsym);
SigGI = zeros(Nsc+Ncp, Nsym);
SigOFDMRx = zeros(Nsc+Ncp, Nsym);
SigGIRx = zeros(Nsc, Nsym);
SigRx = zeros(Ndsc, Nsym);
SigRf = zeros(OSR*(Nsc+Ncp), Nsym);
%% Constellation Mapper
PhOff = pi/4;
% hModulator = comm.PSKModulator(N, 'PhaseOffset', PhOff, 'BitInput', false);
hModulator = comm.RectangularQAMModulator(N, 'PhaseOffset', PhOff, 'BitInput', false);
SigRand = randi([0,N-1], Nsam, 1);
SigIdeal = step(hModulator, transpose(linspace(0,N-1, N)));
SigMapped = step(hModulator, SigRand);          % Output of constellation mapper
%% Serial to Parallel Converter
SigMapped = reshape(SigMapped, Ndsc, Nsym);
for i=1:Nsym
    % map the data to the data subcarriers
```

```
39      if eq(SEL, 1)
40          SigZP(3:30, i) = SigMapped(1:28, i);       %% position of pilot and data subcarriers is not
41          SigZP(35:62, i) = SigMapped(29:56, i);
42      elseif eq(SEL, 2)
43          SigZP(4:60, i) = SigMapped(1:57, i);              %% position of pilot and data subcarriers
44          SigZP(69:125, i) = SigMapped(58:114, i);
45      elseif eq(SEL, 3)
46          SigZP(4:124, i) = SigMapped(1:121, i);
    %% position of pilot and data subcarriers is not exact
47          SigZP(133:253, i) = SigMapped(122:242, i);
48      else
49          % position of pilot and data subcarriers is exact  for the 160 MHz
50          % mode
51          SigZP(5:23, i) = SigMapped(1:19, i); SigZP(24, i) = 1;
52          SigZP(25:51, i) = SigMapped(20:46, i); SigZP(52, i) = 1;
53          SigZP(53:87, i) = SigMapped(47:81, i); SigZP(88, i) = 1;
54          SigZP(89:115, i) = SigMapped(82:108, i); SigZP(116, i) = -1;
55          SigZP(117:125, i) = SigMapped(109:117, i); %%% DC = 3sc
56          SigZP(129:137, i) = SigMapped(118:126, i); SigZP(138, i) = -1;
57          SigZP(139:165, i) = SigMapped(127:153, i); SigZP(166, i) = 1;
58          SigZP(167:201, i) = SigMapped(154:188, i); SigZP(202, i) = 1;
59          SigZP(203:229, i) = SigMapped(189:215, i); SigZP(230, i) = 1;
60          SigZP(231:249, i) = SigMapped(216:234, i); %%%%%%%%%%%%%%%% DC = 11sc
61          SigZP(261:279, i) = SigMapped(235:253, i); SigZP(280, i) = 1;
62          SigZP(282:308, i) = SigMapped(254:280, i); SigZP(309, i) = 1;
63          SigZP(310:344, i) = SigMapped(281:315, i); SigZP(345, i) = 1;
64          SigZP(346:372, i) = SigMapped(316:342, i); SigZP(373, i) = -1;
65          SigZP(374:382, i) = SigMapped(343:351, i); %%% DC = 3sc
66          SigZP(386:394, i) = SigMapped(352:360, i); SigZP(395, i) = -1;
67          SigZP(397:423, i) = SigMapped(361:387, i); SigZP(424, i) = 1;
68          SigZP(425:459, i) = SigMapped(388:422, i); SigZP(460, i) = 1;
69          SigZP(461:487, i) = SigMapped(423:449, i); SigZP(488, i) = 1;
70          SigZP(489:507, i) = SigMapped(450:468, i);
71      end
72      %% IFFT
73      SigIFFT(:,i) = Nsc.*ifft(SigZP(:,i), Nsc);
74      %% Guard Interval (GI) Insertion using Cyclic Prefix
75      SigGI(:,i) = [SigIFFT(end-(Ncp-1):end, i);SigIFFT(1:end,i)];
76      %% Call WiFi Tx Model
77      [SigAnalogOut] = TxModel(transpose(SigGI(:,i)), Fs, 3, 1.6, 1, 'CRFB',  Coeff);
78      SigRf(:,i) = SigAnalogOut.R + 1j.*SigAnalogOut.Q; % create the complex output
```

```
79      % Downsample
80      SigDn = downsample(SigRf(:,i), OSR);        % OSR for Fs mode
81      SigOFDMRx(:,i) = SigDn;
82      %% GI Removal
83      SigGIRx(:,i) = SigOFDMRx(Ncp+1:Nsc+Ncp,i);
84      %% FFT
85      SigFFT(:,i) = 1/Nsc .*fft(SigGIRx(:,i),Nsc);
86      %% Removal of zero-padding
87      if eq(SEL,1)
88          SigRx(1:28,i) = SigFFT(3:30,i);
89          SigRx(29:56,i) = SigFFT(35:62,i);
90      elseif eq(SEL,2)
91          SigRx(1:57,i) = SigFFT(4:60,i);
92          SigRx(58:114,i) = SigFFT(69:125,i);
93      elseif eq(SEL,3)
94          SigRx(1:121,i) = SigFFT(4:124,i);
95          SigRx(122:242,i) = SigFFT(133:253,i);
96      else
97          % Exact Position of pilot and data subcarriers for the 160 MHz mode
98          SigRx(1:19, i) = SigFFT(5:23, i);
99          SigRx(20:46, i) = SigFFT(25:51, i);
100         SigRx(47:81, i) = SigFFT(53:87, i);
101         SigRx(82:108, i) = SigFFT(89:115, i);
102         SigRx(109:117, i) = SigFFT(117:125, i);
103         SigRx(118:126, i) = SigFFT(129:137, i);
104         SigRx(127:153, i) = SigFFT(139:165, i);
105         SigRx(154:188, i) = SigFFT(167:201, i);
106         SigRx(189:215, i) = SigFFT(203:229, i);
107         SigRx(216:234, i) = SigFFT(231:249, i);
108         SigRx(235:253, i) = SigFFT(261:279, i);
109         SigRx(254:280, i) = SigFFT(282:308, i);
110         SigRx(281:315, i) = SigFFT(310:344, i);
111         SigRx(316:342, i) = SigFFT(346:372, i);
112         SigRx(343:351, i) = SigFFT(374:382, i);
113         SigRx(352:360, i) = SigFFT(386:394, i);
114         SigRx(361:387, i) = SigFFT(397:423, i);
115         SigRx(388:422, i) = SigFFT(425:459, i);
116         SigRx(423:449, i) = SigFFT(461:487, i);
117         SigRx(450:468, i) = SigFFT(489:507, i);
118     end
119 end
```

```
120 %% Parallel to Serial Converter
121 SigRx = transpose(SigRx);
122 SigMapped = transpose(SigMapped);
123 %% Scatterplot and EVM Estimation
124 close all;
125 Pavg = sum( (real(SigIdeal(:))).^2 + (imag(SigIdeal(:))).^2 )/N;
    % Average power of ideal constellation
126 Vavg = sum( sqrt((real(SigIdeal(:))).^2 + (imag(SigIdeal(:))).^2) )/N;
    % Average Amplitude of ideal constellation
127 for k=1:Nsym
128     %% EVM Calculation
129     Ierr = real(SigRx(k,:)) - real(SigMapped(k,:));
130     Qerr = imag(SigRx(k,:)) - imag(SigMapped(k,:));
131     Verr = sum(sqrt(Ierr.^2 + Qerr.^2))/Ndsc;
    % average Amplitude of error constellation
132     EVM.SyV(k) = 20*log10( Verr / Vavg );
    % EVM
133 %     EVM.SyLin(k) = sqrt( Verr / Vavg );
134     %% Modulation Error Ratio
135     Perr = sum(Ierr.^2 + Qerr.^2);
    % power of error constellation
136     Psig = sum( (real(SigMapped(k,:))).^2 + (imag(SigMapped(k,:))).^2 );
    % power of signal constellation
137     MER.SydB(k) = 10*log10( Psig / Perr );
    % MER(k) = 10*log10(Psig/Perr)
138     %% Plotting per symbol
139     scatter(real(SigRx(k,:)), imag(SigRx(k,:)), 2, [.2 .6 .9], 'LineWidth', 4);
    % downsampled
140     hold on;
141     scatter(real(SigMapped(k,:)),imag(SigMapped(k,:)), 3, [.2 .1 0.1], 'LineWidth', 5);
    % ideal
142     hold on;
143 end
144 for n=1:Ndsc
145     %% Relative Constellation Error (RCE) calculation ... EVM per subcarrier
146     Ierr = real(SigRx(:,n)) - real(SigMapped(:,n));
147     Qerr = imag(SigRx(:,n)) - imag(SigMapped(:,n));
148     Perr = sum(Ierr.^2 + Qerr.^2)/Nsym;
149     EVM.ScdB(n) = 10*log10( Perr / Pavg );
150 end
151 % EVM.SyLinAver = 20*log10(mean(EVM.SyLin));
```

```
152 EVM.SydBVolAvg = mean(EVM.SyV);          % average of EVM of symbols
153 MER.Avg = mean(MER.SydB);                 % Mean of Modulation Error Ratio
154 EVM.ScdBAvg = mean(EVM.ScdB);            % average of EVM of subcarriers
155
156 %% Spectral Flatness
157 if eq(SEL,1)
158     Eavg = mean(mean(abs(SigRx(:,1:16)).^2));
159 end
160 end
```

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List of Publications

Journal

- **F. T. Gebreyohannes, A. Frappe, and A. Kaiser, "A Configurable Transmitter Architecture for IEEE 802.11ac and 802.11ad Standards,"** ***IEEE Trans. Circuits Syst. II Express Briefs*****, vol. 63, no. 1, pp. 9–13, Jan. 2016.**

Conferences

- **F. T. Gebreyohannes, A. Frappe, and A. Kaiser, "Semi-digital FIR DAC for low power single carrier IEEE 802.11ad 60 GHz transmitter," in** ***New Circuits and Systems Conference (NEWCAS), 2015 IEEE 13th International*****, 2015, pp. 1–4.**
- **F. T. Gebreyohannes, A. Frappe, and A. Kaiser, "Multi-standard Semi-digital FIR DAC: A Design Procedure," in** ***2016 IEEE MTT-S International Wireless Symposium (IWS)*****, Mar. 2016, pp. 1–4.**
- **"Next Generation of Wireless Access: Disruptive Transceivers," in 2016 IEEE MTT-S International Wireless Symposium (IWS) Workshop (co-author of one of the workshop papers)**

Lecture Presentations

- **"A Configurable Transmitter Architecture for IEEE 802.11ac and 802.11ad Standards," in** ***IEEE International Symposium of Circuits and Systems (ISCAS)*****, Montreal, 2016**
- **"Semi-digital FIR DAC for Low Power Single Carrier IEEE 802.11ad 60GHz Transmitter," in** ***Journées Nationales du Réseau Doctoral en Micro-nanoélectronique (JNRDM)*****, Bordeaux, 2015**

Master's Thesis

- **"Design of Ultra-Low Power Wake-Up Receiver in 130nm CMOS Technology," Department of Electrical Engineering, Linkoping University, Sweden, 2012**

Abstract en Français

La prolifération des standards de communication sans fil, spécifiques aux applications, a abouti à la multiplication des standards et des dispositifs pour un seul scénario utilisateur daujourd'hui. Par conséquent, le domaine de la recherche dans les multi-standard, les systèmes multi-bandes, architectures, et circuits a été un thème populaire. La perspective est d'avoir des dispositifs qui peuvent être adaptés aux différents réseaux tout en offrant d'excellentes fonctionnalités sur les différentes technologies d'accès radio.

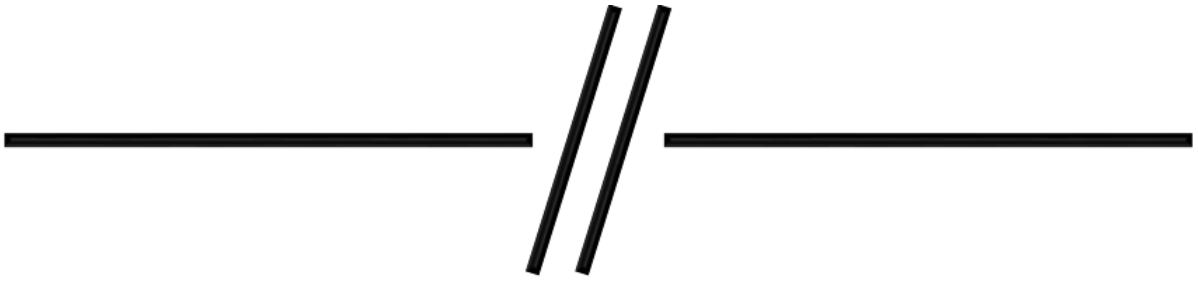
Les architectures d'émetteurs configurables ciblant les cas d'utilisation complémentaires des multistandards multi-Gb/s WiFi-WiGig ont été étudiés. Des approches novatrices basées sur des DAC FIR semi-numériques configurables à grande vitesse sont proposées et publiés dans une revue internationale. Dans ces architectures, le masque émetteur et les exigences de linéarité sont respectées, car le FIR DAC à un seul bit est linéaire et combine dans sa fonctionnalité à la fois la conversion numérique-analogique et le filtrage du bruit. Un modulateur delta-sigma peut être utilisé pour la conversion de résolution de sorte que les signaux en bande de base avec une large gamme de bandes passantes et de résolutions sont traités.

Les DAC de FIR nécessitent des filtres longs avec des coefficients de résolution élevés pour atteindre des niveaux d'atténuation de stopband satisfaisants aux exigences de bruit hors bande. Normalement, cela limite le fonctionnement multi-standard à grande vitesse et se traduit par une grande surface de silicium et un layout complexe. Dans ce travail, les techniques de conception de circuits sont développées de sorte qu'un élément de circuit unitaire réalisant un coefficient d'une fonction de transfert peut être réutilisé dans la réalisation d'un coefficient d'une autre fonction de transfert. Cette capacité multimodale de partage du matériel du FIR DAC est maximisée par optimisation du coefficient au niveau du système.

Le travail propose également des topologies qui exploitent le traitement du signal numérique sur des nœuds avancés pour mettre enœuvre la modulation en quadrature tout en réalisant la conversion, la conversion numérique-analogique, filtrage d'image et la quantification dans un bloc FIR DAC à bande passante configurable. Une puce prototype de filtre passe-haut FIR DAC qui peut être configuré pour le fonctionnement de l'IEEE 802.11ac et l'IEEE 802.11ad a été mise en œuvre sur une technologie CMOS 28nm FDSOI de STMicroelectronics. Le test De cette puce a démontré la validité des architectures d'émetteur proposées. Le prototype de puce peut traiter des signaux OFDM de bande passante aussi larges que 136 MHz à une fréquence d'horloge de 3 GHz et atteint une fréquence porteuse de sortie de 1.5 GHz en mode 802.11ac. Il peut également canaliser des signaux SC aléatoires aussi larges que 700

MHz à une fréquence d'horloge de 1.4 GHz et atteint une fréquence porteuse de sortie de 700 MHz. La puce a une consommation totale de 103.07 mW dans les modes 802.11ac et 86.89 mW dans les modes 802.11ad à une fréquence d'horloge de 1.4 GHz. Il est fourni avec trois alimentations de tension séparées: les circuits numériques fonctionnent de 0.6 V à 1.55 V, le réseau de sortie analogique nécessite une alimentation de 1.2 V et les circuits de polarisation sont fournis avec une tension séparée de 1.2 V.

Mots-clés: *Convertisseurs numérique–analogique, MOS complémentaires, Ondes millimétriques, Radio-Émetteurs et transmission, Filtrage du signal, Multi-bandes, Multi-standard, IEEE 802.11ac, IEEE 802.11ad*



Abstract

The vision of research on multi-standard and multi-band wireless communication systems, architectures, and circuits has been to develop devices which can hop seamlessly from one network to the other while delivering excellent functionality in different radio access technologies.

This work proposes a transmitter architecture based on FIR DACs able to work with very dissimilar high data rate standards for wireless communications at 5 GHz and 60 GHz, namely WiFi (802.11ac) and WiGig (802.11ad). FIR DACs require long filters with high resolution coefficients to meet high out-of-band noise attenuation. Normally, this limits speed and results in large area. In this work, circuit techniques are developed so that a unit circuit elements can be assembled to realize programmable transfer functions. The work also proposes topologies that exploit digital signal processing in advanced technology nodes to implement up-conversion, digital-to-analog conversion and image and quantization filtering in one configurable FIR DAC block.

A prototype high pass FIR DAC chip which can be configured for processing IEEE 802.11ac and IEEE 802.11ad signals was implemented in ST 28nm CMOS FDSOI technology. Experimental results demonstrate the potential of the proposed transmitter architecture. The prototype chip can process baseband signals as wide as 63.63 MHz and 300 MHz at a clock frequency of 1.4 GHz while consuming 103.07 mW in the 802.11ac mode and 86.89 mW in the 802.11ad mode.

Résumé

La recherche dans le domaine des communications multi-standards et multi-bandes vise des architectures et circuits pouvant s'adapter parfaitement aux différents réseaux tout en offrant d'excellentes fonctionnalités sur les différentes technologies d'accès radio.

Ce travail propose une architecture de transmetteur radio utilisant des FIRDAC capable de supporter des standards haut débit à 5 GHz et 60 GHz ayant des caractéristiques très différentes. Il s'agit ici des standards WiFI (802.11ac) et WiGig(802.11ad). Les FIRDAC nécessitent des filtres longs avec des coefficients de résolution élevés pour atteindre des niveaux d'atténuation dans la bande coupée satisfaisants aux exigences de bruit hors bande. Normalement, cela limite la vitesse et se traduit par une grande surface de silicium. Dans ce travail, une approche programmable de la fonction de transfert à partir de cellules DAC unitaire est introduite.

Une puce prototype de passe-haut FIRDAC qui peut être configuré pour le fonctionnement des standards l'IEEE 802.11ac et l'IEEE 802.11ad a été mise en œuvre sur une technologie CMOS 28nm FDSOI de STMicroelectronics. Le test de cette puce a démontré la validité des architectures d'émetteur proposées. La puce prototype peut traiter des signaux avec des bande utiles aussi larges que 63.63 MHz et 300 MHz à une fréquence d'horloge de 1.4 GHz avec une consommation de 103.07 mW dans le 802.11ac et 86.89 mW dans le mode 802.11ad.