

# UNIVERSITE LILLE 1 SCIENCES ET TECHNOLOGIES

École doctorale : Sciences pour l'ingénieur  
Institut d'Electronique, de Microélectronique et de Nanotechnologie

## THÈSE

Présentée par

**Maciej HARAS**

Pour obtenir le grade de

Docteur de l'Université

Spécialité Micro et Nano Technologies, Acoustique et Télécommunications

## **Thermoélectricité non-conventionnelle basée sur les technologies silicium en film minces**

Soutenue le 7 Janvier 2016 devant le jury composé de :

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# List of symbols and abbreviations

<b>AC</b>	Alternate Current	<b>IPO</b>	In-Plane Overlap
<b>a-Si</b>	amorphous Silicon	$j_n$	Electron's current density ( $A/m^2$ )
<b>B</b>	Magnetic induction (T)	$j_p$	Hole's current density ( $A/m^2$ )
<b>Box</b>	Thin layer of electric insulator under the active thin-film layer	$k_B$	Boltzmann's constant $k_B=1.3806\times 10^{-23}$ (J/K) $k_B=8.6173\times 10^{-5}$ (eV/K)
<b>bpm</b>	beats per minute	<b>L</b>	Distance between heater and sensor (m)
<b>Btu</b>	British thermal unit	<b>L.ext</b>	External sensor's length (m)
<b>C</b>	Electric capacitance (F)	<b>L.int</b>	Internal sensor's length (m)
$C_n$	Heat capacity	$L_0$	Lorentz factor $L_0=2.443\times 10^{-8}$ ( $V^2/K^2$ )
<b>CMOS</b>	Complementary Metal Oxide Semiconductor	$L_e$	Mean free path for electrons (m)
<b>c-Si</b>	crystalline Silicon	<b>LED</b>	Light-Emitting Diode
<b>DARPA</b>	Defence Advanced Research Projects Agency	$L_H$	Heating serpentine length (m)
<b>DC</b>	Direct Current	$L_{ph}$	Mean free path for phonons (m)
<b>E</b>	electric field strength (V/m)	$m_0$	Reduced mass of the H-atom $m_0=9.1093\times 10^{-31}$ (kg)
$e^-$	electron	$m_e$	Effective mass for electron (kg)
$E_C$	Conduction band energy (eV)	$m_h$	Effective mass for hole (kg)
$E_{Fn}$	Electrons Fermi level (eV)	<b>MEMS</b>	Micro-Electro-Mechanical Systems
$E_{Fp}$	Holes Fermi level (eV)	<b>MOSFET</b>	Metal Oxide Semiconductor Field Effect Transistor
$E_G$	Bandgap energy (eV)	<b>MIBK</b>	Methyl Isobutyl Ketone resist developer
$E_i$	Intrinsic energy (eV)	<b>m-s</b>	metal-semiconductor junction
$e_{ind}$	Electromagnetically induced potential (V)	$n$	Electrons concentration ( $cm^{-3}$ )
<b>ELL</b>	ELLipsometry	$N_A$	Acceptor doping concentration ( $cm^{-3}$ )
$E_t$	Trap energy level (eV)	$N_C$	Effective density of states in the conduction band ( $cm^{-3}$ )
$E_V$	Valence band energy (eV)	$N_D$	Donor doping concentration ( $cm^{-3}$ )
$f$	frequency (Hz)	<b>NEMS</b>	Nano-Electro-Mechanical Systems
$F_{Cz}$	Electrostatic force (N)	$n_i$	Intrinsic concentration ( $cm^{-3}$ )
<b>FDSOI</b>	Fully Depleted Silicon On Insulator	$N_V$	Effective density of states in the valence band ( $cm^{-3}$ )
<b>FFT</b>	Fast Fourier Transform	<b>OP</b>	Out-of Plane
<b>GNP</b>	Gross National Product	<b>P</b>	Power (W)
<b>GND</b>	Electrical ground	$p$	Holes concentration ( $cm^{-3}$ )
<b>G-R</b>	Recombination rate ( $cm^{-3}\cdot s^{-1}$ )	$P_{el}$	Electric power (W)
<b>GPS</b>	Global Positioning System	<b>PF</b>	Power Factor ( $W/m/K^2$ )
<b>GSM</b>	Global System for Mobile Communications	<b>PGEC</b>	Phonon Glass/Electron Crystal
$H$	Volumetric heat generation ( $W/m^3$ )	$P_H$	Electric power applied to the heater (W)
$h$	Planck's constant $h=6.6260\times 10^{-34}$ (J·s)	<b>PVDF</b>	Polyvinylidene fluoride
$h^+$	hole	<b>PZT</b>	Lead Zirconate Titanate
<b>IEC</b>	International Electrotechnical Commission	$q$	Electric charge $q=1.6021\times 10^{-19}$ (C)
<b>IoT</b>	Internet of Things	<b>Q</b>	Heat flux ( $W/cm^3$ ) or fixed electric charge (C)
<b>IPA</b>	IsoPropyl Alcohol	<b>RF</b>	Radio Frequency
<b>IPGC</b>	In-Plane Gap Closing	<b>RFID</b>	Radio Frequency Identification

<b>RIE</b>	<b>Reactive Ion Etching</b>	<b>VMU</b>	<b>Voltage Measurement Unit</b>
<b><math>R_{n\text{-type}}</math></b>	Electrical resistance of n-type material ( $\Omega$ )	<b><math>V_N</math></b>	Thermally built-in voltage in n-type material (V)
<b><math>R_{p\text{-type}}</math></b>	Electrical resistance of p-type material ( $\Omega$ )	<b><math>V_P</math></b>	Thermally built-in voltage in p-type material (V)
<b><i>rpm</i></b>	rotations <b>p</b> er <b>m</b> inute	<b><math>V_S</math></b>	Voltage applied to sensor (V)
<b>RTG</b>	<b>Radioisotope Thermoelectric Generator</b>	<b><math>v_s</math></b>	Sound velocity (m/s)
<b><math>R_{TOT}</math></b>	Total thermoelectric generator resistance ( $\Omega$ )	<b><math>V_{tot}</math></b>	Total potential barrier in pn junction (V)
<b>S</b>	Thermopower (V/K)	<b>W</b>	Width of suspended membrane (m)
<b><math>s_{el}</math></b>	Cross-sectional surface for electric current ( $m^2$ )	<b><math>W_{Pt}</math></b>	Platinum width (m)
<b>SEM</b>	<b>Scanning Electron Microscopy</b>	<b><math>zT</math></b>	Non-dimensional figure-of-merit (-)
<b>SMU</b>	<b>Source Monitor Unit</b>	<b>ZCS</b>	<b>Zero Current Switching</b>
<b><math>S_n</math></b>	Thermopower in n-type material (V/K)	<b>ZVS</b>	<b>Zero Voltage Switching</b>
<b><math>S_p</math></b>	Thermopower in p-type material (V/K)	<b><math>\Phi</math></b>	Magnetic flux (Wb)
<b>SOI</b>	<b>Silicon On Insulator</b>	<b><math>\alpha_{Pt}</math></b>	Temperature coefficient of the electrical resistivity ( $K^{-1}$ )
<b>SRH</b>	<b>Shockley-Read-Hall</b> recombination model	<b><math>\phi</math></b>	Applied electric potential ( <i>in Coulomb's gauge</i> ) (V)
<b>STC</b>	<b>Standard Test Conditions</b>	<b><math>\phi_{FP}</math></b>	Holes quasi-Fermi level (eV)
<b>SThM</b>	<b>Scanning Thermal Microscopy</b>	<b><math>\phi_{Fn}</math></b>	Electrons quasi-Fermi level (eV)
<b><math>t</math></b>	Thickness of suspended membrane (m)	<b><math>\eta</math></b>	Efficiency (-)
<b>T</b>	Temperature (K)	<b><math>\kappa</math></b>	Total thermal conductivity (W/m/K)
<b><math>T_{CHUCK}</math></b>	Chuck's temperature (K)	<b><math>\kappa_{bulk}</math></b>	Thermal conductivity for bulk material (W/m/K)
<b><math>T_{COLD}</math></b>	Cold temperature (K)	<b><math>\kappa_{el}</math></b>	Electronic thermal conductivity (W/m/K)
<b>TEG</b>	<b>ThermoElectric Generator</b>	<b><math>\kappa_{film}</math></b>	Thermal conductivity for thin-film material (W/m/K)
<b><math>T_H</math></b>	Heater's temperature (K)	<b><math>\kappa_l</math></b>	Lattice thermal conductivity (W/m/K)
<b><math>T_{HOT}</math></b>	Hot temperature (K)	<b><math>\mu_p</math></b>	Holes mobility ( $m^2/V/s$ )
<b>time</b>	Time (s)	<b><math>\mu_n</math></b>	Electrons mobility ( $m^2/V/s$ )
<b>toe</b>	tonne of <b>oil e</b> quivalent $1toe=11.6MW\cdot h$	<b><math>\rho_{cont}</math></b>	specific contact resistance ( $\Omega\cdot cm^2$ )
<b><math>t_{Pt}</math></b>	Platinum thickness (m)	<b><math>\rho_{Pt}</math></b>	Platinum electrical resistivity ( $\Omega\cdot cm$ )
<b><math>T_S</math></b>	Sensor's temperature (K)	<b><math>\sigma_n</math></b>	Electrical conductivity for n-type material ( $1/\Omega/m$ )
<b>V</b>	Electric potential or voltage (V)	<b><math>\sigma_p</math></b>	Electrical conductivity for p-type material ( $1/\Omega/m$ )
<b><math>V_0</math></b>	Built-in <i>pn</i> junction potential (V)	<b><math>\tau_n, \tau_p</math></b>	Electron and hole carrier life time respectively (s)
<b><math>V_A</math></b>	Anode voltage (V)	<b><math>\omega</math></b>	Angular speed (rad/s)
<b><math>V_H</math></b>	Voltage applied to heater (V)		

# General Introduction

The semiconductor industry is in continuous expansion since 1960. In 2015, this branch is worth over 347 billions dollars [\[Semiconductor Industry Association, 2015\]](#). The constant growth of this market required and developed numerous innovative applications of electron devices with rising performance and density constantly reducing the manufacturing costs. For more than fifty years the technological effort was dominated by a downscaling trend defined by the 'Moore law' [\[Moore, 1977\]](#). However, as minimal dimensions of electron devices is approaching the atomic limit, down scaling is no longer possible, economically and technologically. The 'Moore law' proves to be much more difficult to achieve [\[Moore, 2003\]](#).

As a result of the 'Moore law' saturation in Complementary Metal Oxide Semiconductor (**CMOS**), the industry research effort was focused on the modification of downscaling trend which resulted in the 'More Moore law'. In parallel the 'More than Moore' approach emerged. It describes a technological trend where numerous additional functionalities are integrated on the same chip e.g. microsystems, energy harvesting and storage, mechanical flexibility, sensors or actuators. Multifunctionality of single chip requires integration of numerous embedded systems into a single package or chip.

With the rapidly growing market of mobile devices, the need of reliable and compact energy source is become critical. Extension of the device operation time requires more effective energy storage and/or unconventional source of power. Self supplied device must embed a source of power able to transform input energy e.g. heat [\[Goldsmid, 2010\]](#), light [\[Di Piazza, 2013\]](#), vibrations [\[Erturk, 2011\]](#), radio frequencies [\[Greene, 2014\]](#) etc. into electric energy able to totally cover component needs.

Urged by the worldwide increasing demand in energy, constrained by the limited reserves of fossil fuel and faced by the problem of global climate change, all innovative solutions contributing to improve the sustainability of energy production are playing a strategic role. Despite the effort in inventing conversion techniques able to produce energy in more efficient and durable way, a lot of energy is lost. Among all energies produced worldwide, heat represents the highest wastes, around half of input energy being dissipated to atmosphere as a waste heat. In this context the energy represented by heat losses is extremely important and converting them into useful energy will contribute to wiser, durable, economic usage of fossil fuels.

Work presented here focuses on the thermoelectric energy harvesting. Thermoelectricity converts heat into electric current in direct, silent, vibrationless and reliable way. However, it requires materials with antagonistic properties: high crystal-like electrical conductivity ( $\sigma$ ) and low glass-like thermal conductivity ( $\kappa$ ). For more than 30-years, this requirement resulted in the development of harmful, complex, expensive and industrially incompatible materials e.g.  **$\text{Bi}_2\text{Te}_3$** ,  **$\text{PbTe}$**  or  **$\text{Sb}_2\text{Te}_3$** . Recent developments of micro- and nano-technologies offered new possibilities to reduce  $\kappa$  with minor impact on  $\sigma$ . This approach enables transforming simple, cheap, harmless and **CMOS** compatible materials namely: Silicon (**Si**), Germanium (**Ge**), and Silicon-Germanium ( **$\text{Si}_x\text{Ge}_{1-x}$** ), into technologically and economically attractive thermoelectric materials. The material transition from conventional **CMOS** incompatible, to unconventional **CMOS** compatible will significantly contribute in popularization of thermoelectricity on the market.

This manuscript is organized in four chapters. The first chapter presents the urgent necessity to provide power from unconventional environmentally friendly sources before the complete depletion of natural reserves in fossil fuels. Afterwards, evaluation of main energy losses in the world is provided, emphasizing the heat losses. This puts in evidence the strategic importance of waste energy recovering. The second chapter reviews most popular techniques to transform waste energy into electric current. Each harvesting approach is evaluated taking into account output power density and voltage. The aim of this chapter is not only to review the state-of-the-art literature but also to present the many possibilities to harvest energy. The third chapter focuses on performance modelling of **ThermoElectric Generator (TEG)** in different unconventional arrangements based on **Si**, **Ge** or **Si<sub>x</sub>Ge<sub>1-x</sub>** benchmarking with well established **Bi<sub>2</sub>Te<sub>3</sub>**. Performance analysis leads to conclusion that **CMOS** compatible materials are competitive with conventional thermoelectrics (**Bi<sub>2</sub>Te<sub>3</sub>**) unless their high bulk  $\kappa$  is reduced. The fourth and final chapter presents the technological part of this thesis including the design, fabrication and characterization of micrometer measurement platform for  $\kappa$  measurements in thin-film **Si**.

This document is concluded by a synthesized summary highlighting the most important results. The emphasis is put on (i) high harvesting performance of **CMOS** compatible materials, (ii) fabrication procedures and (iii) experimental confirmation of size induced  $\kappa$  reduction in thin-film silicon. Possible future directions of this research are also discussed.

## Chapter 1

This chapter presents the situation of energy in the world. The economical and industrial growth is directly relying on energy supply. At the beginning of this chapter the evolution of primary energy consumption since 1960 is studied. In the last fifty years, the consumption of primary energy almost tripled, each year the global consumption of this energy is rising by 2.5%, however this growth is faster since the last 5 years. This is an indicator of the rapid world industrial.

Particular attention is devoted to electric energy in the world. This energy exhibits an annual mean growth by over 3%. Around  $\frac{3}{4}$  of global electricity is produced from fossils fuels, which natural reserves are expected to run out in the next 50 years. Thus, alternative sources of energy will play a strategic role. Since the last 30 years, the production of electricity by renewable sources is rising by 3.6% annually and nowadays around 20% of electricity comes from renewable sources. Despite rising investments in the field of renewable sources of energy, there is still a lot of progress to be done to replace completely fossil fuels before their exhaustion.

A way to increase the production of energy without increasing the consumption of fossil fuels is to harvest it from waste energy. In this chapter the evaluation of losses while producing and distributing electricity is presented. This estimation shows that in electric industry more energy is lost than delivered to consumers.

Most of the energy losses related to human activities are heat losses. Waste heat is estimated from 20% to 50% of input energy and negligibly small amount of those losses is recovered. Recovering heat losses generated in the United States with the efficiency of only 8% would cover total annual electricity consumption of European Union. This shows the quantity of energy which is lost, and underlines also the importance of energy production from wasted energy.

Finally, the development and diversification of energy production techniques improves stability and ensures the continuous growth of world economy. Waste energy harvesting offers the possibility to improve the independence of fossils fuels and simultaneously

preserves natural environment since emission of gases responsible for gashouse effect is reduced.

## Chapter 2

Urged by the growing demand in energy, faced by the problem of global climate change and constrained by the limited reserves of fossils fuel a big effort is currently done to develop alternative energy sources. This chapter presents a brief review of the concept of energy production from waste energy. In function of input waste energy different scavenging methods can be used. The quantity and variety of energy wastes worldwide compel to develop adapted harvesting methods. The aim of this chapter is to give a general perspective on the capabilities and performance of different harvesting methods. Energy scavenging methods reviewed below enable recovering almost all types of waste energy, thus the importance of the harvesters is very high.

## Chapter 3

This chapter presents the innovative trends in thermoelectricity on the material and topological level. A comprehensive and compact comparative study of the thermoelectric harvesting capabilities for different materials focusing on **CMOS** compatible materials is provided. Thermoelectric capabilities are simulated based on the doping- and temperature-dependent modelling of carrier concentrations ( $n$ ,  $p$ ,  $n_i$ ,  $N_C$ ,  $N_V$ ), mobilities ( $\mu_{n,p}$ ), Seebeck coefficients ( $S_{n,p}$ ) and electrical conductivities ( $\sigma_{n,p}$ ). Constructed model evaluates the theoretical limit of harvested electric power without referring to the thermal conductivity ( $\kappa$ ) and assuming temperature drop across **ThermoElectric Generator (TEG)** to be constant ( $\Delta T = \text{const.}$ ). Firstly, the model is used upon insulated media to confront it with experimental data. Secondly, electrical performance of **CMOS** compatible **TEGs** is modelled and compared with harvesting capabilities of **Bi<sub>2</sub>Te<sub>3</sub>**-based generator. Different unconventional architectures of **TEGs** are investigated to put in evidence the impact of topology on the performance. Thirdly, the analysis is completed by studying **TEG** conversion efficiency ( $\eta$ ) considering the size-induced  $\kappa$  reduction. Comparative studies of the harvested power density put the **CMOS** compatible materials in competitive position compared with conventional thermoelectrics. Comparable harvested power density level for classic thermoelectrics and **CMOS** compatible materials shows a big potential of the latter in thermoelectricity. Reduction of  $\kappa$  improves  $\eta$  up to 10× over efficiency for **TEG** based on bulk material. Finally, studies put in evidence the fact that thermoelectric effect is more efficient harvesting mechanism than the thermal generation of free carriers in the  $pn$  junction.

Dual development of **TEG** both on material and topological level is incomparably contributing making the thermoelectric conversion more popular on the market and can launch the époque of **CMOS**-based **TEGs**.

## Chapter 4

This chapter presents technological input of this work including the concept of the proposed device, the design, the fabrication, the characterization and finally results evaluation. Among numerous thermal conductivity ( $\kappa$ ) characterization methods electro-thermal method was chosen due to its simplicity on methodological and equipment level maintaining high measurement accuracy. However, this method requires topology featuring (i) as low as possible thermal leakages, (ii) linear temperature distribution along characterized material and (iii) as precise as possible temperature sensitivity enabling  $\kappa$  determination at lowest possible temperature drop. Those requirements are significantly

influencing the layout of the device which is included while creating the tape out. Device fabrication requires technological methods *e.g.* dry and wet etching, evaporation or material growth and deposition. Proposed topology is fabricated upon the **Silicon On Insulator (SOI)** wafer with active Silicon (**Si**) layer thickness of 68nm. After the fabrication the complete characterization is performed giving mean  $\kappa$  value of 57W/m/K which represents 3-fold reduction over  $\kappa$  for bulk **Si**. The measured  $\kappa$  follows the empirical law with satisfying precision and it is dependent only on the thickness of the characterized membrane. Designed, fabricated and characterized device proves experimentally the size induced  $\kappa$  reduction in **Si**. Size-induced  $\kappa$  reduction opens new applications of **CMOS** compatible materials especially as environmentally friendly, cheap and industrially compatible thermoelectrics.



# Chapter 1: Energy in the world

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## 1.1 Introduction

Energy is one of the basic scalar physical quantity. It describes the ability of a physical system to do work on the other physical system [Hewitt, 2006]. Within this general definition all known types of energies are comprised *e.g.* potential, kinetic, electric, thermal, chemical or nuclear *etc.* With rising performance of modern industry the energy starts to play a strategic role in social and industrial development. Modern society is in constantly rising demand of numerous types of energies. Thus, the energy is not only a physical quantity with complicated definition but it is also correlated to social and industrial development.

### 1.1.1 Overall primary energy consumption in the world

Maintaining the societies and households in operation, is a task which demands some input energy. This energy has to be produced in various and geographically dislocated sites and delivered to a consumer. According to [British Petroleum, 2014] we can observe constant growth of consumed primary energy<sup>1</sup> during last decades. Since the sixties consumption of primary energy exhibits average annual rise of 2.5%. This evolution of the primary energy consumption is depicted in Fig. 1-1:

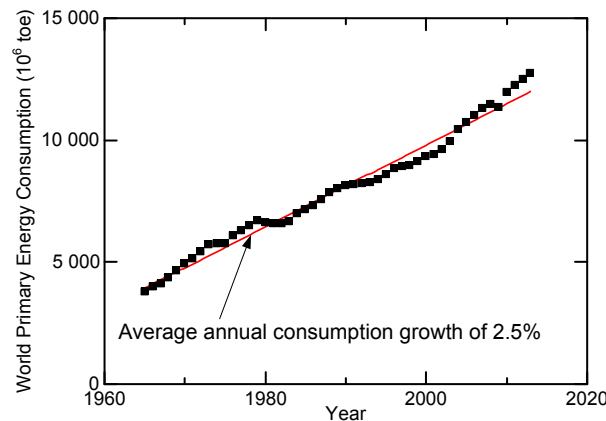


Fig. 1-1 World primary energy consumption in the last 40 years [British Petroleum, 2014].

The primary energy comprises all types of input energies consumed by industry and society *e.g.* coal to produce heat and electricity, petrol to supply all vehicles, energy of wind and sun transformed to electricity or heat, *etc.* The unit to express primary energy is **toe (tonnes of oil equivalent)**<sup>2</sup>. When analyzing Fig. 1-1 it is visible that over last forty years the energy consumption almost tripled. Such a significant growth is a result of economic and industrial development but also by constantly rising world population.

<sup>1</sup> Primary energy is the energy found in nature and this energy has not been transformed or converted. To this type of energy we can include raw fuels (oil, coal) and such types of energy which are received as system input energy.

<sup>2</sup> **toe (tonnes of oil equivalent)** is the quantity of energy which is released when burning one tonne of hypothetical crude oil with heating value of 29300kJ/kg for coal and 10000kJ/kg for oil. Conversion ration between tonne of oil equivalent and electric energy can be expressed as follows:  $1toe = 11.6MW \cdot h$

### 1.1.2 Electric energy - the world situation

As previously mentioned, one of the components included in primary energy is electric energy which is in the scope of this thesis. Following part of this thesis is focused only on the electric energy.

The electric energy generation is an image of world economic situation. Fig. 1-2 shows the evolution of gross and renewable<sup>3</sup> electricity production in the global scale.

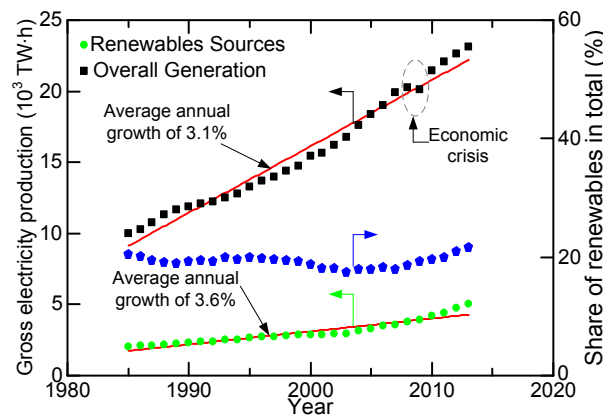


Fig. 1-2 History of total world and renewable electricity generation based on [\[British Petroleum, 2014\]](#)

Electric energy is so close, so present and irreplaceable in ordinary life that it can be an indicator of quality of life. In 2010, the serious financial crisis began causing a significant recession in all industrial branches. This financial crisis is reproduced on Fig. 1-2 by reduction of electricity generation corresponding to the year when crisis began.

In average, world electricity generation rises by 3.1% per year and electricity generation from renewable sources increases slightly faster by 3.6% annually. Despite slightly higher development of renewable sources, the share of energy produced by renewable sources in overall electricity production stays around 20%. As depicted in Fig. 1-2, over the last decade the amount of energy produced from renewable sources exhibits an increased growth.

The importance of renewable sources is accentuated mainly by the natural environment preservation and the fact that global reserves of fossil fuels are limited. Total world proved oil reserves are sufficient to cover only 53 years of global production according to [\[Benes, 2015\]](#) and [\[British Petroleum, 2014\]](#). This situation obliges to find alternative sources of energy able replacing the oil. The same conclusion can be done for others fossil fuels (*e.g. oil, gas or nuclear*). Thus, during the last decade we could observe an increase of investments in the field of renewable sources of energy. Also, numerous research groups around the globe are working in the field of alternative sources of energy seeking for completely new or developing the existing devices converting renewable energy.

To encourage investments in renewable sources of energy some juristic acts *e.g.* United States of America Renewable Portfolio Standard or **E**uropean **U**nion directive 2009/28/EC [\[EU, 2009\]](#), were adopted. The **EU** directive defines the target share of renewable sources of energy in the overall energy production, for each member country,

<sup>3</sup> Renewable sources of energy include energy (re)converted from: water, wind, geothermal, solar and biomass.

this target has to be achieved by the end of 2020. This policy is efficient because during the 2013 there were nearly 195 billions € of investments on renewable sources of energy in the world and this number is constantly and rapidly rising *e.g.* in the 2004 the cost of the investments in renewables was around 30 billions € [REN21, 2014], less than  $\frac{1}{6}$  of actual investments in the field.

On this ground the importance of renewable sources of energy is not only matter of juristic acts or preservation of natural environment but essentially it is a way to ensure the constant industrial development and economical growth when global reserves of fossil fuels will run out.

### 1.1.2.1 Macro scale renewable sources of energy

In 2013, 22.2% of global electric energy was provided by the renewable sources [REN21, 2014]. The “green” electric energy in 2013 was  $E_{RENEW}=5134.2$  TW·h (*global electric energy produced in 2013 is  $E_{2013}=23127$  TW·h*) which is comparable with total electric energy generated in Europe and Eurasia ( $E_{EU+EA}=5234.1$  TW·h) [British Petroleum, 2014] and [REN21, 2014]. Despite increasing production of “green” electric energy there is still need to improve the world independence on fossil. Mainly renewable electricity is produced by:

- Hydro generation
- Wind turbines
- Biomass
- Solar panels
- Geothermal
- Concentrators of Solar Thermal Power (CSP)
- Ocean and sea flows energy harvesters

Electricity production of above mentioned sources of energy is detailed in Fig. 1-3.

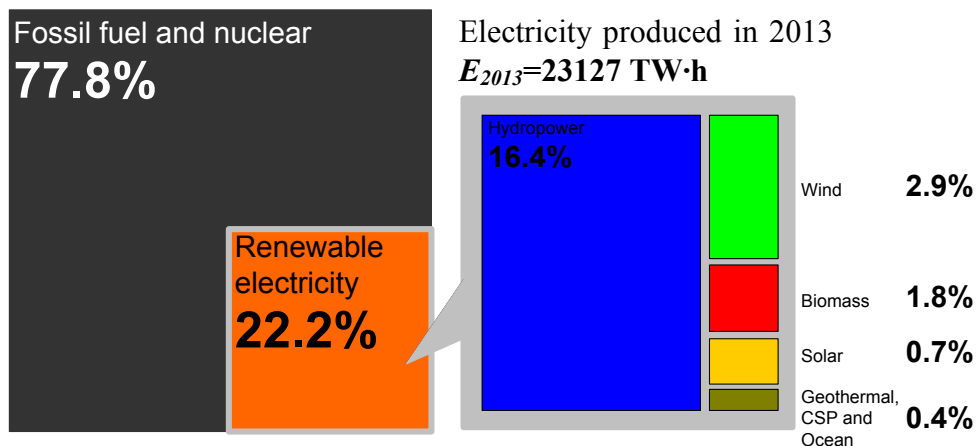


Fig. 1-3 World global electric energy production at the end of 2013 detailing the production from renewable sources based on [REN21, 2014]

Fig. 1-3 presents precisely the electricity production from different renewable sources. The most important part of “green” electric energy is produced by hydraulic power plants followed by the production provided by wind mills, the biomass combustion and the photovoltaic panels. The electricity produced using those four conversions represents 98.2% of total electricity generation in renewable sources.

It is worth noting that natural reserves of non-renewable as well as renewable sources are limited. The renewable sources of energy have also their limits imposed by global resources in *e.g.* sunlight or wind.

**Table 1-1 Global resources in renewable energy and the energy currently available**

Energy	Global resources (TW)	Currently available (TW)	Percentage of used global resources (%)
Wind	1700 <sup>a</sup>	0.318 <sup>b</sup>	0.187
Geothermal	45 <sup>a</sup>	0.012 <sup>b</sup>	0.027
Hydroelectric	1.9 <sup>a</sup>	0.432 <sup>c</sup>	22.7
Solar Photovoltaic	6500 <sup>a</sup>	0.139 <sup>b</sup>	0.021
Concentrators of Solar Thermal Power (CSP)	4600 <sup>a</sup>	0.0025 <sup>b</sup>	0.001

<sup>a</sup> Data based on [\[Jacobson, 2011\]](#)

<sup>b</sup> Data based on [\[REN21, 2014\]](#)

<sup>c</sup> Data based on [\[British Petroleum, 2014\]](#)

Table 1-1 presents the estimate of the global resources in different renewable energy types and the energy which is converted actually. Worth noting is the fact that renewable sources are providing big reserves and currently only small amount of the global resources is used. The energy produced by hydraulic power plants represents almost  $\frac{1}{5}$  of available global resources and still this is the resource the most used among all renewable sources. Other sources of “green” energy are using less than 1% of available earth resources, especially the energy provided by sunlight and geothermal represents resources almost unused by current energy production. The alternative sources of energy can compensate and in long term replace the use of the fossil fuels. The goal is to develop energetically and costly-efficient generators able to produce energy from desired input.

One of the most important disadvantage of the abovementioned “green” sources is their huge financial weight. As a result only countries with strong economy can develop and install this type of electric supply. This deficiency is limiting the realizations only to the richest zones and not to the places where the input renewable energy is the most present *e.g.* highest insolation or average wind speed per annum.

### 1.1.3 Concept of waste energy harvesting

With accelerating industrial growth, the necessity of efficient power conversion is needed much more than ever before. Unfortunately, all known conversion types and industrial processes exhibits efficiencies lower than unity, thus the presence of energy losses on each energy conversion step is unavoidable. To reduce those losses, more efficient machines and processes should to be used. Another way to reduce losses is to use them as input to produce additional energy. The concept of energy production from waste energy is receiving more and more attention recently [\[Harb, 2011\]](#), [\[Harne, 2013\]](#), [\[Matiko, 2014\]](#) and [\[Radousky, 2012\]](#) thanks to the development of nano- and micro-technology which allows miniaturization of the harvesters, making them easy to install.

The exploding number of electric and electronic equipments requires significant power supply. Sometimes providing supply by wires is problematic due to lack of place, necessity to destroy already existing constructions or due to long distance [\[Atkinson, 2013\]](#).

Powering devices without wires significantly facilitates mounting, installation modifications and device use. Energetically-autonomous devices are big application opportunity for energy harvesters. In the age of omnipresent internet people can communicate, control and monitor the objects remotely. Communications recently entered a new era where data is exchanged directly between objects with no human participation. Direct communication between machines is called the **Internet of Things (IoT)** [Gorlatova, 2010]. In the most general case **IoT** system is equipped with sensors and captors which are transferring the information to a master unit which is controlling all system basing on provided information, as illustrated in Fig. 1-4. Good example of the **IoT** system is intelligent building [McLelland, 1988] depicted in Fig. 1-5. Such a building is equipped in sensors which are monitoring important functional parameters *e.g.* air temperature or humidity, light density, presence of people *etc.* Data are transferred to steering unit which takes a decision to turn on/off the radiator, lamp or activate an alarm. Number of sensors needed to completely take control over dwelling is high. Currently, each sensor has to be wired which rises the system cost and hinders further modifications.



Fig. 1-4 Schematic illustration of communication chain in the system of **Internet of Things**

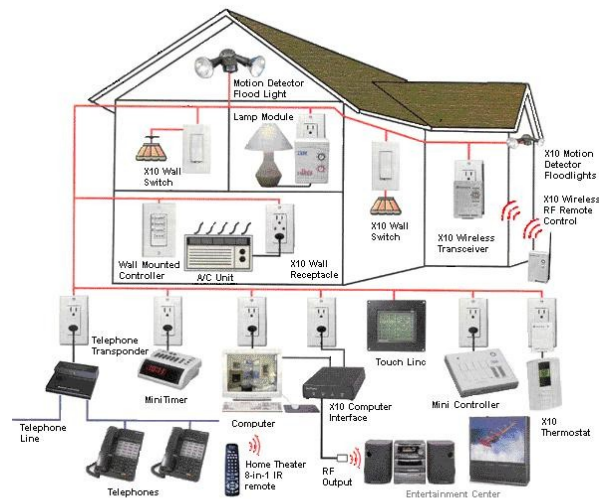


Fig. 1-5 Example of installation in the intelligent building



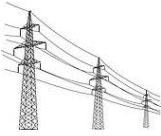

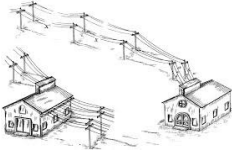
Worth noting is the fact that control over intelligent dwelling can be realized with omission of the human decision. Moreover, the system cost can be significantly reduced when using energy-autonomous sensors or captors, but this requires supply provided by energy harvesters. Knowing that **IoT** market size was \$1.7 trillion in 2013 and is estimated \$7.1 trillion in 2020 [Press, 2014], possibility to use energy harvesters in **IoT** systems is a big opportunity to popularize the harvesters on the market.

To make the harvesters attractive enough input waste energy provided. In the following two estimates are provided: (i) energy losses in electricity production, transformation and distribution and (ii) the estimation of waste heat.

#### 1.1.3.1 Waste energy when producing, transforming and distributing electricity

Table 1-2 is presenting the chain of electric energy production, transformation and distribution emphasizing the typical conversion efficiency on each step of the chain.

**Table 1-2 Typical efficiencies of electricity production, transformation and distribution**

Chain step	Efficiency	Fraction of input energy lost	Energy available at the end of the step
 Conventional nuclear, coal- or gas-fired power plant	33%-48% <sup>a</sup> <i>Mean: 40,5%</i>	52%-67% <i>Mean: 59,5%</i>	33%-48%
 Voltage transformation for high voltage lines	83%-98% <sup>b</sup> <i>Mean: 90,5%</i>	2%-17% <i>Mean: 9,5%</i>	27%-47%
 Electricity distribution in high voltage lines	90%-98% <sup>c,d</sup> <i>Mean: 94%</i>	2%-10% <i>Mean: 6%</i>	24%-46%
 Voltage lowering to domestic level	75%-90% <sup>c</sup> <i>Mean: 82,5%</i>	10%-25% <i>Mean: 17,5%</i>	18%-41%
 Low voltage distribution	90%-98% <sup>c,d</sup> <i>Mean: 94%</i>	2%-10% <i>Mean: 6%</i>	16%-40%

<sup>a</sup> Based on [White, 1992]

<sup>b</sup> Based on [Flanagan, 1993]

<sup>c</sup> Based on [Hase, 2013]

<sup>d</sup> Statistics by International energy agency <http://www.iea.org/statistics/> page access on the 21/01/2015

<sup>e</sup> Based on [McLyman, 2011]

The conclusion arising from Table 1-2 is that only 16% to 40% of input energy is delivered to the consumer as electric energy. This conclusion underlines the importance of recovering waste energy. Worth noting is the fact that overall losses in electricity production and distribution are dominated by the losses which occurs when generating the electricity (*coal fired, nuclear or gas power plants*), around 60% of input energy is lost in power plant. The efficiency of electric power plant is mainly imposed by the maximal possible efficiency of thermodynamic cycles (*usually Rankine cycle is used with theoretical maximal Carnot efficiency of 63%*), other losses such as heat losses, turbine and pump losses are also lowering overall efficiency of power plant but in minor way.

To better illustrate the presence of the losses when producing and distributing electric energy Fig. 1-6 is provided. In contrary to Table 1-2 the numbers are based on real production and consumption in 2007 [International Energy Agency, 2008].

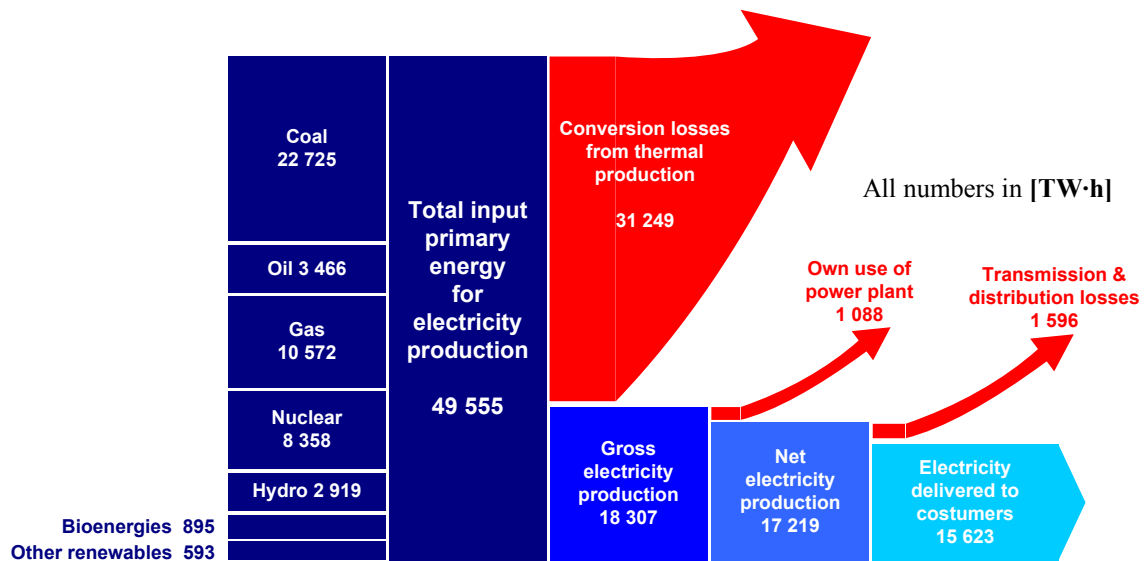


Fig. 1-6 Energy flow in global electric system in 2007 based on [\[International Energy Agency, 2008\]](#)

Fig. 1-6 presents clearly that the electricity is mainly produced in the nuclear, coal- and gas-fired power plants which are presenting low conversion efficiencies. It is also presented that in 2007 around 31.5% of the input energy was delivered to costumers as electric energy.

In the electric energy production and distribution chain the losses occurs mainly in the form of heat which is dissipated to the atmosphere, the other losses *e.g.* transmitting leakage losses, magnetic losses in transformers or losses due to corona discharge in high-voltage lines are playing secondary role. Fig. 1-6 and Table 1-2 are both leading to the conclusion that the amount of waste energy in global electric system is very high. Transforming waste heat energy formed in global electric system into additional electricity with efficiency of 4-5% (*common efficiency of thermoelectric generators*) will produce half of the annual electricity consumed in all **EU**. Knowing that heat losses are the most important when generating and distributing electricity, in the following the quantification of them is provided.

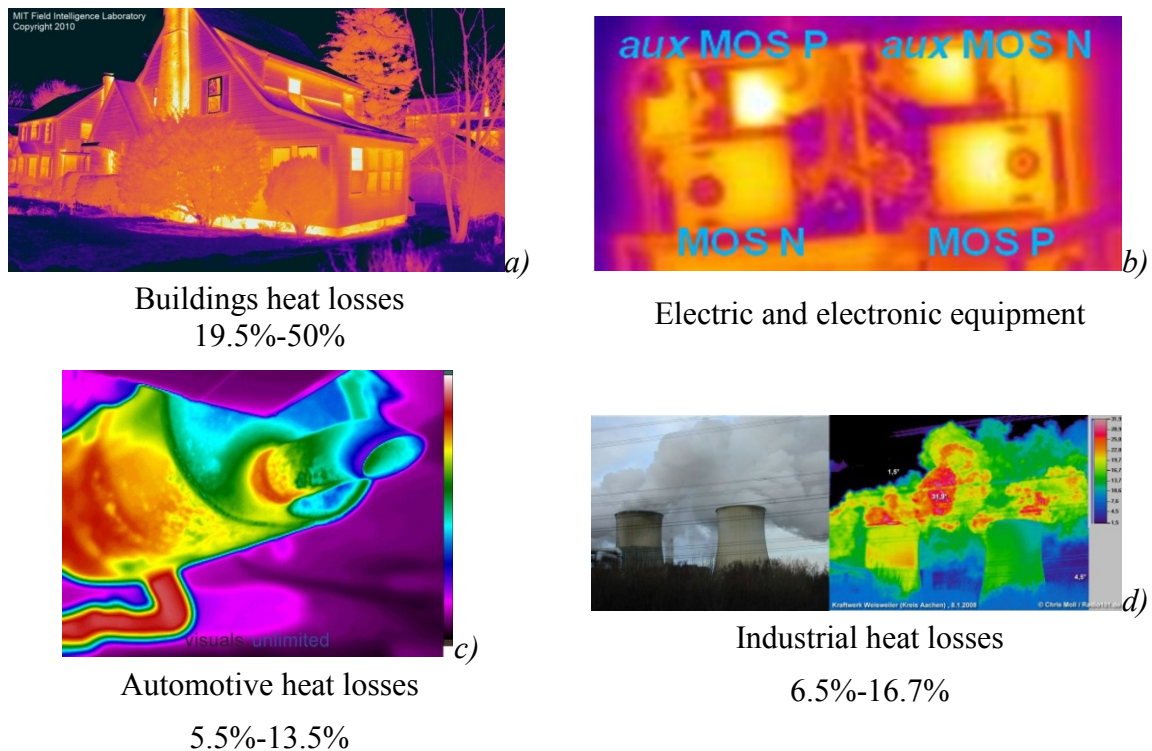
### 1.1.3.2 Evaluation of waste heat at global scale

Following [\[Cook, 1971\]](#) at least 50% of input energy is lost in the form of waste heat. More recent report estimated that only in **USA** the waste heat represents 20%-50% of input energy and that even 470 TW·h/year ( $1.6 \times 10^{15}$  Btu<sup>4</sup>/yr) can be recovered [\[Energetics, 2004\]](#). There is a lack of data for other counties, thus it is difficult to estimate global mean value of waste heat. But it can be assumed that half of heat produced globally is released to atmosphere as a waste heat.

In ordinary life there are a lot of heat sources which are not used. Four main heat dissipation means are presented in following pictures.

<sup>4</sup> British Thermal Unit (Btu) represents an amount of energy sufficient to cool or to heat one pound of water (0.453 kg) by one degree Fahrenheit ( $\approx 0.55^\circ\text{C}$ )





**Fig. 1-7 Main waste heat producers the percentage numbers are presenting the share of heat losses for corresponding branch in overall primary energy consumption**

- Massachusetts Institute of Technology (MIT) Field Intelligence Laboratory (2010)
- M.Haras "Low conductive noise power inverter based on CMOS technology" (2008)
- Visuals Unlimited, Inc.(2011)
- Photo by Chris Moll of Weisweiler power plant near Aachen, Germany

Fig. 1-7 depicts infrared photos representative of the four areas responsible for the majority of waste heat. The percentage below the photos corresponds to share of primary energy released as waste heat for corresponding branch [Energetics, 2004]. Surprisingly, buildings are dissipating the most heat while industry, operating with significantly higher power, exhibits lower heat losses. The reason of this are: (i) more frequent modernization and investments in industry than in buildings and (ii) continually improved standards imposed by the normative documents which have to be fulfilled. Domestic heat losses are mainly caused by: (i) insufficient building thermal insulation, (ii) poorly efficient central heating systems and (iii) consumers life style. While in industry the reduction of heat losses can be driven rather easily by the regulation laws or technical norms taking into account the economical weight of modernization. On the contrary, reduction of domestic heat losses is much more difficult since it requires changing individual behaviours and societal trends. Changing people's minds is a long and slow process.

There is a lack of heat losses estimation formed in electronic or electric equipments since the exact number of those devices is not determined and the efficiency of such equipments is difficult to evaluate. The number of computers, mobile phones or digital cameras increases rapidly, all of them consisting in microprocessors, microcontrollers and others electronic devices all dissipating heat. The heat flux that can be produced by processors is highly non-uniform both spatially and temporary and can be as high as  $300 \text{ W/cm}^2$  depending on workload [Chowdhury, 2009] which is huge value of heat dissipated from relatively small areas. Imagining the quantity of microprocessors in use globally leads to the conclusion that heat losses in electronic and electric equipment are very high.

### 1.1.3.3 *Waste energy as indicator of richness*

As previously mentioned, the installation of renewable sources requires very large economical investment with long term of amortization. Thus the big drawback of the renewable sources is that only rich countries can invest in this branch. Table 1-3 compares the electric and heat losses with **Gross National Product (GNP)** per capita.

**Table 1-3 Gross national product and energy losses for given countries. Data for 2012 based on statistics provided by International Energy Agency**

	Bulgaria	Russia	EU-28	Switzerland	South Korea	Japan
<b>GPD/capita [\$ /capita]</b>	<b>4 630</b>	<b>6 834</b>	<b>28 802</b>	<b>55 460</b>	<b>21 564</b>	<b>36 804</b>
<b>Heat produced [TJ]</b>	<b>57 824</b>	<b>6 407 559</b>	<b>2 496 851</b>	<b>18 366</b>	<b>219 508</b>	<b>23 355</b>
<b>Heat losses</b>	<b>28.6%</b>	<b>19.1%</b>	<b>18.8%</b>	<b>8%</b>	<b>5.1%</b>	<b>3.8%</b>
<b>Electricity produced [TW·h]</b>	<b>47.329</b>	<b>1 070.734</b>	<b>3 295.430</b>	<b>69.866</b>	<b>534.618</b>	<b>1 034.305</b>
<b>Electricity lost</b>	<b>41.2%</b>	<b>30.9%</b>	<b>15.1%</b>	<b>15.6%</b>	<b>9.9%</b>	<b>10.8%</b>
<b>Losses totally</b>	<b>69.8%</b>	<b>50%</b>	<b>33.9%</b>	<b>23.6%</b>	<b>15%</b>	<b>14.6%</b>

Based on statistics provided by International Energy Agency (<http://www.iea.org/statistics/>) for 2012

The national product per capita is the indicator of the economical health for a given country. Table 1-3 compares countries with high **GNP/capita** with countries with low **GNP/capita**. The rich countries are wasting less energy than the countries with modest national product per capita. The countries which are the leaders in the world economy such as Japan, South Korea or Switzerland exhibit low energy losses from 14.6% for Japan to 23.6% for Switzerland. This number is much lower than losses which occur in Bulgaria 69.8%, or Russia with 50%. The reason for this situation is the number of investments in modernization or construction of the power plants able to produce energy more efficiently. In addition, the mentality of the habitants and their ability to change their life style in terms to contribute to energy savings. Strong economy and cooperative, well-informed society can significantly reduce energy losses as we can observe for the Asian countries.

### 1.1.3.4 *Household waste energy*

Previously described national losses also happen in the households. Domestic losses are significant and as showed previously only small amount of them is recovered. The identification and evaluation of waste energy in the average household is presented in the following. The households are supplied in diverse energies: electricity, hot/cold water, heat, water flow. The percentage of the lost energy is depending on installation quality, modernity and on the usage style.

According to data provided by The Joint Research Centre<sup>5</sup> in 2012 the residential sector in **EU** is responsible for consuming 26.65% of total annual energy [[JRC, 2012](#)]. The household energy consumption can be spitted into four main fields.

<sup>5</sup> Joint Research Centre <http://iet.jrc.ec.europa.eu/energyefficiency/sites/energyefficiency/files/energy-efficiency-status-report-2012.pdf> from the 12 February 2015

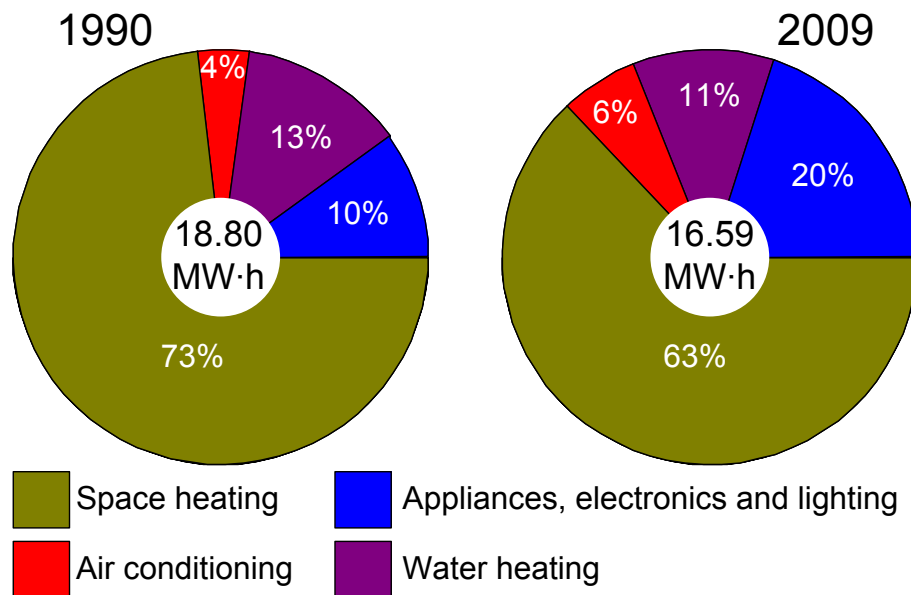


Fig. 1-8 Evolution of energy consumption in houses on the interval of 19 years. The annual total energy consumption per dwelling in the centre [\[Eurostat, 2014\]](#)

Fig. 1-8 illustrates the average composition of the domestic consumption in 1990 and 2009 in the **EU** [\[Eurostat, 2014\]](#). Over 20 years the way how the energy is consumed changed, the biggest change is observed for the space heating and supplying the electronic equipment and lightning. The reduction of energy needed for household heating can be explained by: (i) the climate warming, (ii) significant improvements in the thermal insulation and (iii) more efficient heating devices. On the other hand the increase of energy consumption supplying the electronics and lightning devices is observed. Such a situation is caused by the continually rising quantity of electronic equipments installed in households and their intense usage.

Electronic and lightning equipment exhibits high efficiency usually up to 95% [\[Musiał, 1998\]](#), thus the losses in those devices are relatively low. However, the devices dedicated to produce heat presents, in general, low efficiency e.g. water heaters common efficiency 75%-83% [\[Energy.gov, 2015\]](#), fireplace 15%-80% [\[Wikipedia, 2014\]](#), convection radiators 50% (*best case*). In 2009 the amount of energy for the space heating in residential sector in all **EU-28**<sup>6</sup> dwellings was 2132.2 TW·h (*10.4 MW·h/dwelling/year*) but half of this energy is lost which represents the 1066.1 TW·h (*5.2 MW·h/dwelling/year*) [\[Eurostat, 2014\]](#). Recovering totally heat losses formed in residential sector in the **EU-28** countries would cover the electricity needs of all **EU-28** industrial sector (*966.312 TW·h in 2009* [\[Eurostat, 2013\]](#)). This conclusion underlines the quantity of energy lost and the importance of energy recovering.

Main part of the energy is consumed for space heating, and this is the energy the most difficult to conserve inside the household due to numerous leakages (*ventilation, floor, window or wall losses*) are illustrated in Fig. 1-9a. According to [\[Brett, 2005\]](#) the heat losses can reach even 50% of total energy consecrated to house heating, Fig. 1-9b illustrates the time evolution of average heat loss per dwelling in United Kingdom [\[Palmer, 2013\]](#).

<sup>6</sup> EU-28 is designator used for 28 states countries of European Union: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, United Kingdom

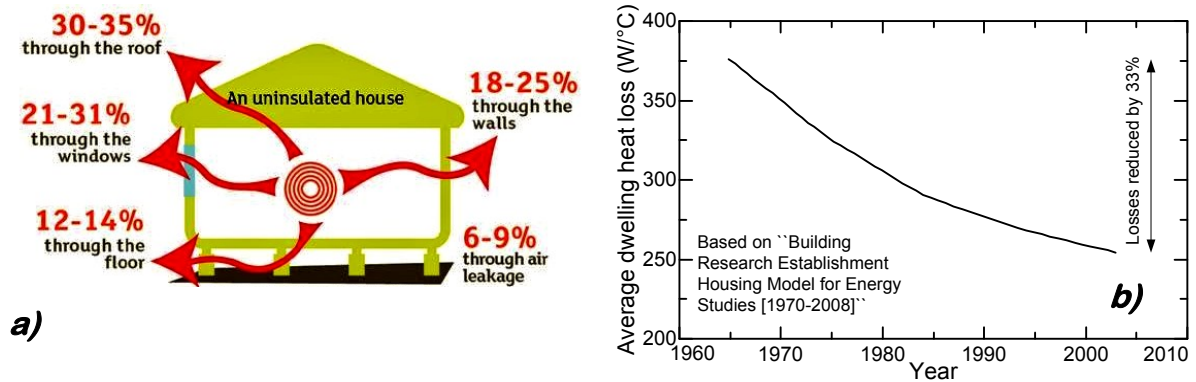


Fig. 1-9 Domestic heat losses a) the percentage of heat losses for given leakage path; b) average heat loss per dwelling over past years [Palmer, 2013]

The example of Great Britain depicted in Fig. 1-9b illustrates clearly the significant improvement in heat consumption effectiveness. Over last 40 years the heat losses has been reduced by  $\frac{1}{3}$  but still the average heat losses states for around  $250\text{W}/^\circ\text{C}$  per dwelling which is significant amount of energy. Total suppression of the domestic heat losses is impossible, because of the household architecture and the need to ventilate. However, those losses can be used as a source to produce additional energy *e.g.* electric energy thought thermoelectric effect. Such a solution would additionally improve the heat effectiveness due to regenerative use of the losses.

Domestic heat is not the sole energy with practical possibility to harvest from, the residential activity offers a lot of diverse possibilities to produce additional energy from renewable or waste energy. Thanks to development of micro- and nano-fabrication technologies it is now possible to mount the harvesters almost everywhere.

Fig. 1-10 illustrates the possibilities of energy harvesting in dwellings. The variety and efficiency of domestic equipment enables the production of energy from wastes or renewable energy. The additional energy which can be produced is indicated as the power densities for a given harvester type. However, the quantity and availability of power is not the most important, but the fact that this energy, in most cases, is uselessly lost. The omnipresence of energy that can be harvested, allows diversification of the energy consumption, improves the independency on energy, reduces the consumption of primary energy and finally contributes to reduction of gases responsible for the greenhouse effect. Power densities available for current energy harvesters are not sufficient to cover significant part of total energy consumed in household. However, their usage opens new opportunities especially in light of increasing rapidly number of installed sensors. Energy-autonomous equipments are possible thanks to the employment of energy harvesters, the use of such equipments simplify the installation and make the installation easy to modify. In the age of increasing importance and presence of electronic devices the possibility of alternative, simple and selfsupply is very interesting.

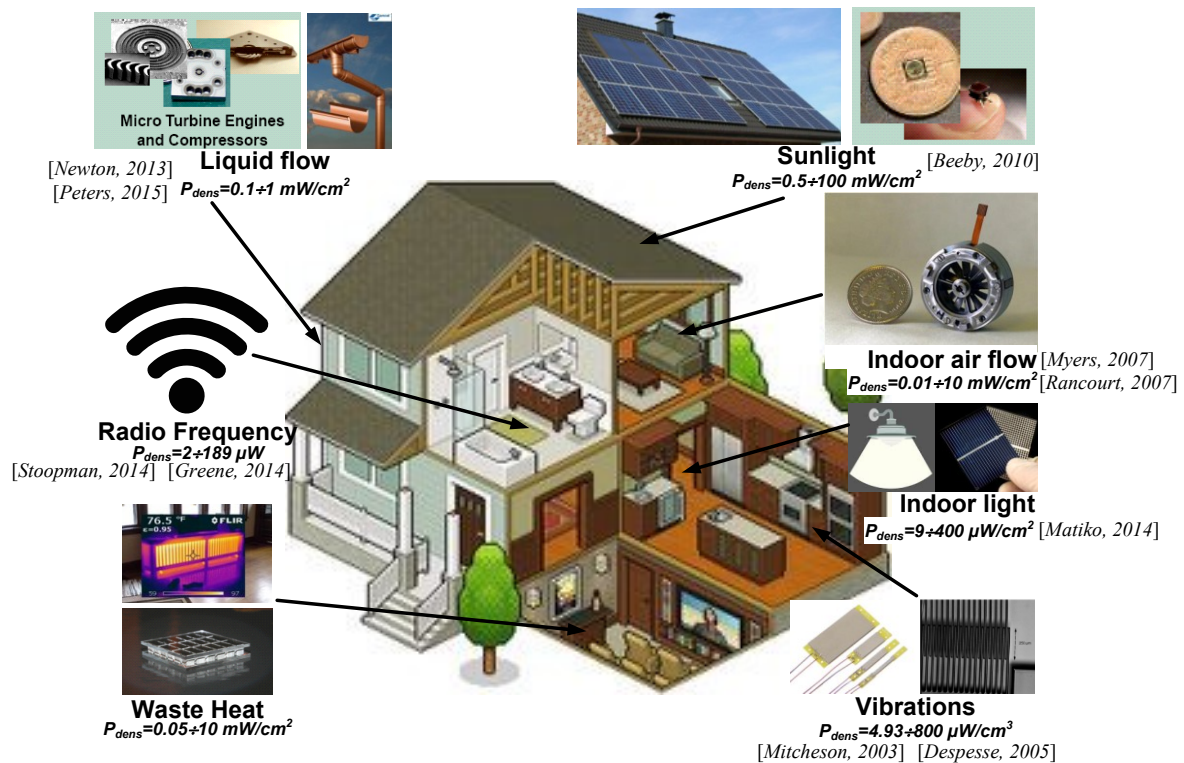


Fig. 1-10 Chosen energy harvesters possibilities with corresponding provided power density range for given harvester in domestic environment [Beeby, 2010], [Myers, 2007], [Rancourt, 2007], [Matiko, 2014], [Mitcheson, 2003], [Despesse, 2005], [Stoopman, 2014], [Greene, 2014], [Newton, 2013], [Peters, 2015]

### 1.1.3.5 Energy from the human body

Good example of omnipresence of energy and expanding possibilities of additional energy from waste is the idea to use human body as source of energy. The estimation of harvesting capabilities of human body is depicted in Fig. 1-11 [Starner, 2004].

Table 1-4 presents the human body power demand to perform given activity [Morton, 1953]. Worth noting is the fact that the highest powers are needed for activities related with movement and displacement, other activities are demanding significantly lower power. The activities which are requiring high power are more interesting from the harvesting point of view because eventual losses created during such activity are higher, it is more likely that harvester will operate with higher input powers for those activities.

Fig. 1-11 depicts waste energy which can be observed in human body. It is presented that all activities related with movement are offering significant energy losses. Worth noting is also the fact that for different activities the waste energy has different character. Those differences in source energy type and availability constrain the physical effect used to harvest and the generator's output power. Energy harvesting from human body is based mainly on recovering from body heat and movement in general. Some applications will be presented in the following.

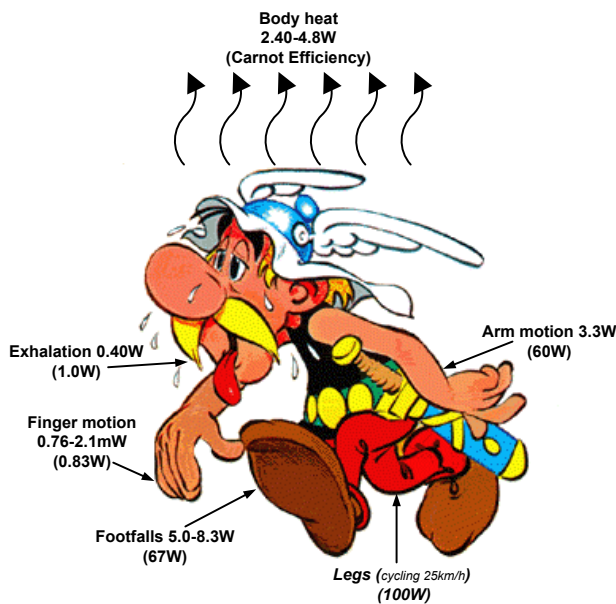


Fig. 1-11 Average available energy from different human activities [Starnier, 2004]

Table 1-4 Body power needed for chosen activities [Morton, 1953]

Activity	Energy	
	Kcal/h	Watts
Sleeping	70	81
Lying quietly	80	93
Sitting	100	116
Standing at ease		
Conversation	110	128
Eating meal		
Strolling		
Driving car	140	163
Playing piano		
Housekeeping	150	175
Carpentry	230	268
Hiking, 6km/h	350	407
Swimming	500	582
Mountain climbing	600	698
Long distance run	900	1 048
Sprinting	1 400	1 630

### 1.1.3.6 Energy from vehicles

At the end of 2010 the global number of vehicles in operation was over 1.015 billions [Sousanis, 2011]. The quantity of vehicles in use rises annually by 3.6% in average. Most of the cars are with internal combustion engine propulsion, while the fully electric car represents less than 2% of the global market [Shahan, 2014]. Vehicles driven by the combustion engine are responsible of around 12% of total  $\text{CO}_2$  emission in European Union [EU, 2015]. The policy of the EU council is promoting the vehicles with small  $\text{CO}_2$  emission.  $\text{CO}_2$  emission targets are 175g  $\text{CO}_2/\text{km}$  in 2014 and 135g  $\text{CO}_2/\text{km}$  in 2020 [EU, 2014]. To accelerate the modernization in EU vehicles exceeding the limits will be penalised e.g. 20€ per gram of exceeding  $\text{CO}_2$  from 2012 and 95€ per gram of exceeding  $\text{CO}_2$  starting from 2020.

The idea of energy harvesting in cars is not a new concept, since the apparition of electric propulsion the concept of regenerative braking was proposed [Szumanowski, 2013]. The regenerative braking allows decelerating the vehicle by switching the electric motor into electric generator. Such braking allows converting the vehicle inertia into electric energy. However, this solution is possible only in vehicles equipped with electric propulsion. For vehicles with combustion engines the energy harvesting is much more difficult and innovative concept. In vehicles with combustion engine propulsion, only around  $\frac{1}{4}$  of input energy is transformed into movement, this is illustrated in Fig. 1-12. Resting  $\frac{3}{4}$  of energy is lost mainly in the form of heat.

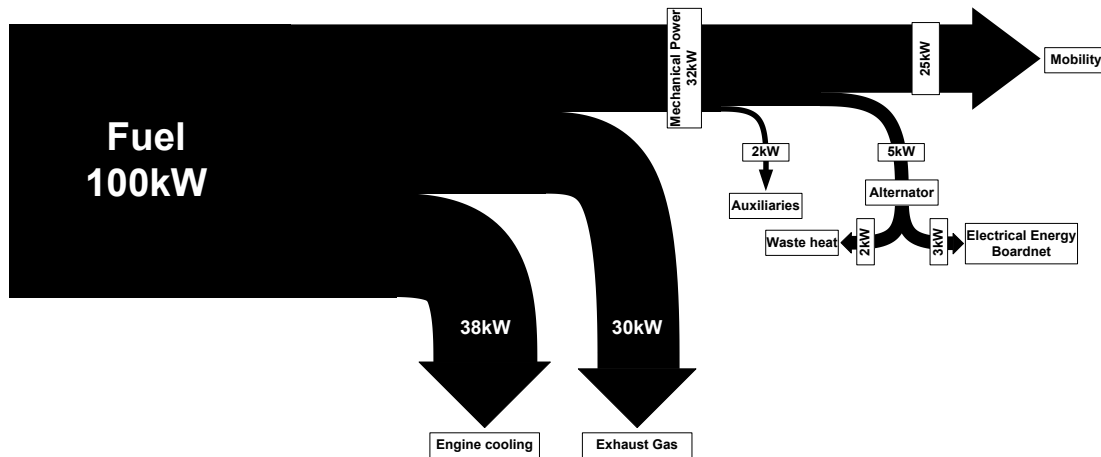


Fig. 1-12 Sankey diagram for diesel light duty truck

Modern cars are becoming more and more sophisticated, complicated and automated. The systems adopted in the vehicles are helping the driver decision or more recently start to replace the driver. Fig. 1-13 illustrates the quantity of used sensors and electronic systems installed in a car.

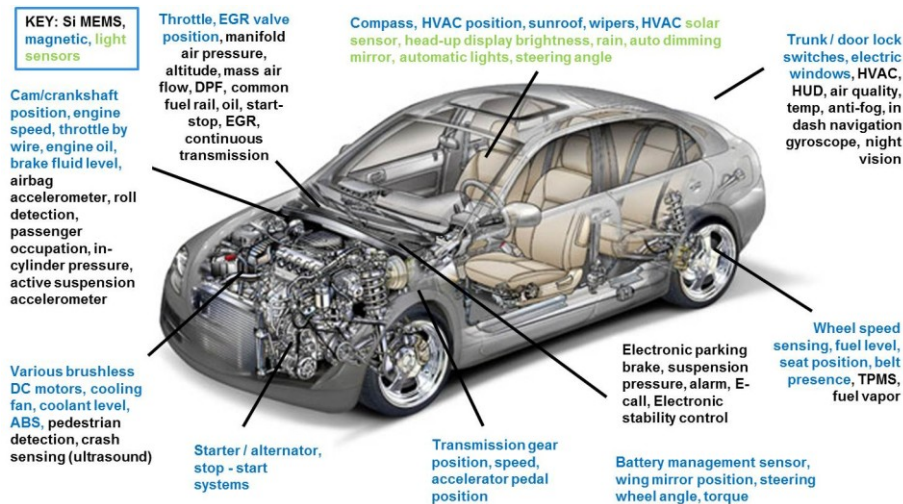


Fig. 1-13 Chosen examples of electronic sensors and systems installed in modern cars distinguishing the Si MEMS, magnetic and light sensors ©IHS Inc. [Lipman-Sidense, 2013](#)

Because of extremely limited car volume the systems are installed in a very dense way, making wiring difficult, expensive and defective. Powering the electric and electronic devices autonomously can simplify the construction, boost the life-time of the car and reduce the fuel consumption by reducing load power extracted from the alternator. Such large quantity of electronic equipment requires high electric power for supply. A detailed table of electric load for typical light duty truck is presented in Table 1-5.

Table 1-5 List of onboard vehicle's electric equipment and power [Miller, 2006]

Engine Management	Power (W)	Multimedia & HVAC	Power (W)	Body Electrical	Power (W)
Fuel Pump & Injection	135	High-end audio sys.	300	Power windows (4)	560
Ignition System	60	Navigation and GPS	150	Power door locks (4)	200
Electr. Throttle System	60	Driver information display	30	Wipers & washers	140
Sensors & Actuators	110	Cabin climate valves	75	Heater backlight	500
Solenoids & Relays	20	Blower motor + ECU	370	Power seats	460
<b>Subtotal Engine</b>	<b>385</b>	<b>Subtotal Cabin Systems</b>	<b>925</b>	<b>Sub. body systems</b>	<b>1860</b>
Chassis Electrification	Power (W)	Lightning (Exterior & Interior)	Power (W)		
Electr. assistance steering	300	Headlamps (2)	120		
ABS brake system	200	Running/park lights (4)	130		
Air suspension valves	50	Turn signal lamps	130		
Air compressor	500	Centre high mount stop	65		
<b>Subtotal Engine</b>	<b>1050</b>	Back-up, interior, licence	45		
		<b>Subtotal Cabin Systems</b>	<b>490</b>	<b>Total Electric/Electronic</b>	<b>4710</b>

Table 1-5 lists the power needed to supply onboard equipment installed in a car. Using all equipment simultaneously requires almost 5kW of power from the battery or the alternator. Knowing that the breaking torque in alternator depends mainly on the output generator's electric power [Patrick, 1997], reduction of the alternator's electric load will reduce the energy needed to drive the alternator thus will reduce the fuel consumption.

Studying Fig. 1-12 lead to conclude that the total wasted energy is higher than energy transformed to mobility. Those wastes are mainly in the form of the heat formed in the engine, the exhaust system and the alternator. The waste heat represents at least 32% of input energy in diesel engine. Thus, in vehicles, the most interesting energy to harvest from is the heat which can be converted into additional electric energy to relief the alternator. Converting the heat into electricity with reasonable and achievable nowadays efficiency of 4-5% can produce significant electric power, for light-duty truck Fig. 1-12 from 1.3kW to 1.6kW. This power can cover all electrical needs of vehicle's lightning and chassis electrification (Table 1-5). Moreover, according to Fiat Research Centre<sup>7</sup> such additional electric power offers **CO<sub>2</sub>** reduction from 10% to 27%.

The vehicles are offering also the possibility to transform the vibrations into additional electric energy. The quantity of energy possible to harvest from vibrations is difficult to estimate. However, harvesters reported in the literature are exhibiting sufficient output power for micro consumption devices such as sensors or captors.

<sup>7</sup> Fiat Research Centre waste heat recovering project (<http://www.crf.it/en-US/Aree/Systems/Pages/Sistemiriuilizzocaloescarto.aspx>) accessed on the 24 February 2015



## 1.2 Chapter summary

This chapter gives an estimation of energy losses at a global scale. Surprisingly, the energy losses are higher than the usable output energy. In other words globally more energy is lost than it is consumed. This shocking observation is amplified by the fact that global energy system is running on limited reserved of fossil fuels. To preserve the economical growth and social progress alternative supplying sources have to be developed before complete depletion of natural reserves in fossil fuels. However, today around 20% of global energy comes from the renewable sources, which is far too low.

To better understand where and how the energy is lost the main energy losses are identified. According to numerous reports and publications most of energy losses are released as heat. Global energy situation can be improved by managing dual action. Firstly, reducing energy losses will result in more wised energy production. Secondly, producing energy from wastes since their presence is unavoidable. In this chapter few potential sources in domestic, automotive and biological environment are presented, emphasizing the estimation of power possible to recover.

Being aware of the quantity and character of energy losses it is now time to introduce the manner how to recover those losses.



## Chapter 2: Energy from waste: a bird's eye view

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Urged by the growing demand in energy, faced by the problem of global climate change and constrained by the limited reserves of fossils fuel a big effort is currently done to develop alternative energy sources. This chapter presents a brief review of the concept of energy production from waste energy. In function of input waste energy different scavenging methods can be used. The quantity and variety of energy wastes worldwide compel to develop adapted harvesting methods. The aim of this chapter is to give a general perspective on the capabilities and performance of different harvesting methods. Energy scavenging methods reviewed below enable recovering almost all types of waste energy, thus the importance of the harvesters is very high.

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## 2.1 Introduction

After reading the first chapter, more realistic perspective on energy losses, their importance and quantity is achieved. In this chapter the most popular recovering methods to produce energy from waste are presented. Production of energy from waste is urged by the worldwide increasing demand in energy, constrained by the limited reserves of fossil fuel and faced by the problem of global climate change. Thus significant research efforts are currently being pursued to improve sustainability of energy production modes.

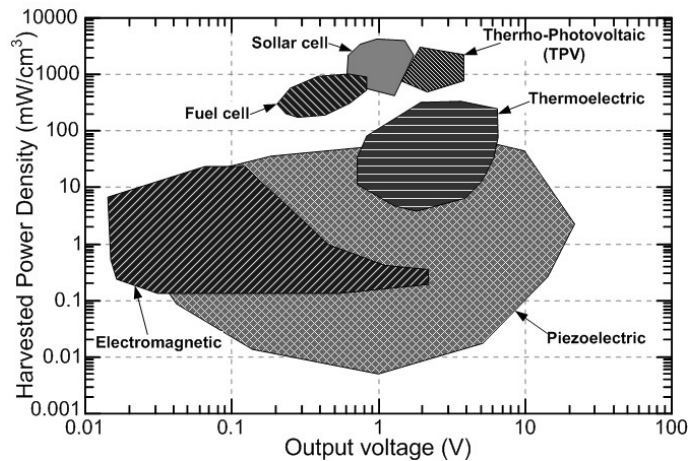


Fig. 2-1 Comparison of harvesting power density and output voltage for different harvesting techniques [Cook-Chennault, 2008]

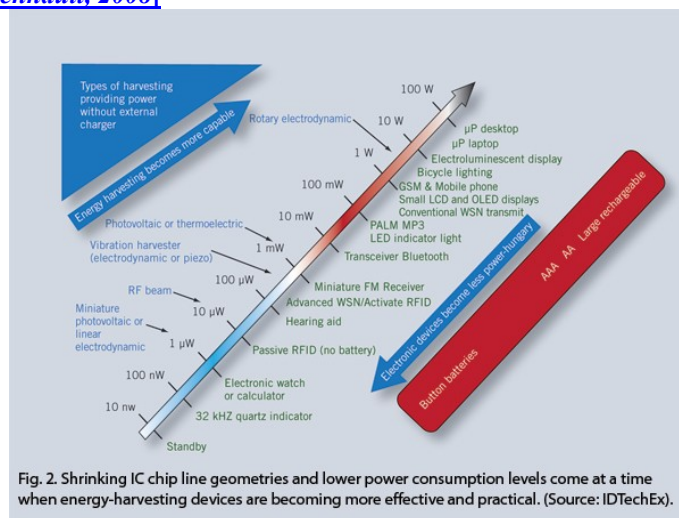


Fig. 2-2 Harvested power for different scavenging technologies and corresponding electric power consumption for given devices technologies [Allan, 2012]

Harvesting method depends on the input waste energy type. Fig. 2-1 depicts the comparison of different harvesting methods, it is presented that depending on energy harvesting approach the generator performance are not the same. The variety of wasted energy types requires different topologies, modes of operation, harvesting method and thus the generator parameters are different. Fig. 2-1 shows clearly the range of power densities and output voltages for various harvesters, the widest range in voltage as well as in power density is provided by piezoelectric and electromagnetic generators which are converting mechanical energy. Thus it can be concluded that energy scavenging from mechanical energy represents the biggest family among energy harvesters. The second group of waste

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energy converters uses thermoelectric effect. Finally, the generators with highest power densities are novel topologies of Thermo-Photovoltaic, solar and fuel cells. In the modern world the quantity of electricity consuming devices is very high. Modern electronic devices with rapid market grow (*cellular phones, sensors, wrist watches etc.*) generally have a micro-power consumption. Fig. 2-2 matches the common nominal power for chosen device with the nominal power available from harvester. This illustrates covered range of power by multiple harvesting technologies and possible application devices. Energy scavenging can contribute in alternative powering of numerous devices allowing:

- the life-time extension,
- battery size reduction,
- wireless supplying,
- fully autonomous devices

Devices enabling the above mentioned properties are very important in industrial and domestic environment. From the industrial perspective, the alternative/autonomous powering enables the electric installation simplification is a highly valuable property. Domestically, the harvesting technologies are more important due to their contribution in reducing energy consumption. Taking into account the wide range of possible output power from different harvesting technologies and the huge diversity of devices, it can be concluded that energy scavenging technologies are simultaneously fulfilling the ecological (*renewable source of energy*), technological (*for some harvesters the fabrication is cheap and simple*) and economical (*contribution to life-time extension*) demands expected from alternative green sources of energy. Recent growth of interest in developing efficient energy scavenging techniques is underlining the importance and hope offered by the energy production from wastes.

The aim of this chapter is to present a bird eye view on waste energy harvesting methods emphasizing the mechanical, thermal, light and electromagnetic energy harvesting.

## 2.2 Energy harvesting from mechanical energy

Harvesting from mechanical energy is a very interesting topic which inspired a lot of scientific groups around the world. Harvesting from mechanical energy is the most popular way to produce energy from wastes. Fig. 2-1 shows that the mechanical energy harvesting (*e.g. piezoelectric, electromagnetic*) offers the widest range in output power and voltage, harvesting from mechanical energy is the biggest group among all known energy harvesters. The input energy for those harvesters is kinetic energy, the energy which includes liquid or gas flow, vibrations, human activity and pressure variations (*e.g. changes of atmospheric or noise pressure*) [Roundy, 2004]. Few examples of vibrations sources are listed in Table 2-1, the omnipresence of those sources is very attractive.

**Table 2-1 Few examples of potential vibration sources distinguishing their appearance** [Roundy, 2003]

	Human body	Transportation	Infrastructure	Industry
Vibration source	Breathing, blood flow/pressure, walking, talking, arm motion, jogging exhalation, heart work, articulation, muscles contractions, etc.	Aircraft, automobile, train, tires, track, peddles, brakes, engine, turbine, shock absorbers, suspension system, etc.	Bridges, roads, tunnels, house structure bending, water/gas pipes, control switches, etc.	Motors, compressors, chillers, fans, pumps, cutting, dicing, pneumatic hammer, etc.

Different parameters of input mechanical energy (*e.g. frequency, vibration amplitude, acceleration, kinetic energy*) impose the use of adapted harvesters for chosen type of input energy. Gas or liquid flow kinetic energy increases cubically with the speed of the flow [Weimer, 2006]. However, machinery, human activity or transportation contributes to low-level vibrations with frequencies from 1Hz to 200Hz and acceleration amplitudes from  $1\text{m/s}^2$  to  $15\text{ m/s}^2$  [Penella-López, 2011]. Table 2-2 presents the sources of vibrations and corresponding acceleration and peak frequency.

**Table 2-2 Acceleration of peak frequency for different vibration sources** [Kong, 2014], [Matiko, 2014]

Vibration source	Acceleration ( $\text{m/s}^2$ )	Peak frequency $f_{\text{peak}}$ (Hz)
Car engine	12.0	200
Heal pressing while walking	7.0-12.0	1.2
Base of 3-axis machine tool	10.0	70
Blender casing	6.4	121
Clothes dryer	3.5	121
Car instrument panel	3.0	13
Small microwave oven	2.5	121
Vents in office building	0.2-1.5	60
CD on notebook computer	0.6	75
Central heating boiler	$6.08 \times 10^{-2}$	121
Microwave	2.17	132

Continuation Table 2-2 Acceleration of peak frequency for different vibration sources [Kong, 2014], [Matiko, 2014]

Vibration source	Acceleration (m/s <sup>2</sup> )	Peak frequency $f_{\text{peak}}$ (Hz)
Washing machine	$7.62 \times 10^{-2}$	108
Tumble dryer	0.28	50
Freezer	$3.56 \times 10^{-2}$	116

Table 2-2 points out the large range of accelerations and peak frequencies for chosen sources of vibration. In Table 2-2 the list of possible vibration sources is reduced only to most interesting examples, the omnipresence of available vibrations is definitively great advantage of energy harvesting from mechanical energy.

Depending on used physical effect we can distinguish piezoelectric, electrostatic or electromagnetic energy harvesters [Kim, 2011]. The reported efficiencies for piezoelectric harvesters are from 0.5% (for polyvinylidene fluoride **PVDF**) to 20% (for lead zirconate titanate **PZT**) [Shenck, 2001]; 0.32% for electrostatic [Mitcheson, 2008] and 6% for electromagnetic harvesters respectively [Beeby, 2010].

All of mentioned types of those generators are producing alternative electric energy (e.g. piezoelectric material is producing positive or negative voltage when compressed or stretched). This is problematic especially for micro power harvesters because the generator has to be equipped with rectification unit, the presence of this rectifier is lowering overall efficiency of the harvester [Ottman, 2002]. Moreover, to adapt output voltage to desired value two conversions are needed first **AC-to-DC** conversion on the output of harvester and second **DC-to-DC** to control and maintain the output voltage value [Kong, 2010], [Lefevre, 2007-a]. The schematic representation of energy harvesting system with the use of electrostatic, electromagnetic or piezoelectric harvester is depicted in Fig. 2-3.

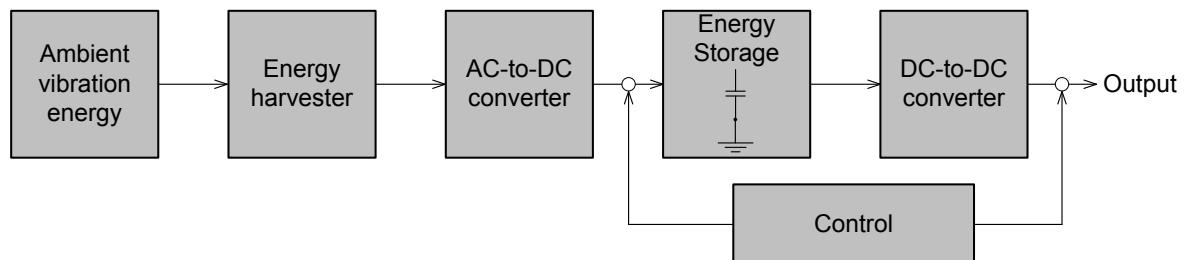


Fig. 2-3 Schematic representation of energy harvesting system with the use of piezoelectric, electrostatic or electromagnetic harvester [Erturk, 2011]

The intermediate stages between energy harvester and output are usually complex for efficiency optimization. Thus, innovative ultra-efficient converters and control system have to be used such as resonant converters [Guan, 2007], operation in discontinuous mode [Ottman, 2003] non linear control algorithms [Guyomar, 2005].

In the following a detailed description of harvesting methods based on mechanical energy is presented.

## 2.2.1 Piezoelectric energy harvesting

### 2.2.1.1 *Basics*

The piezoelectric effect was discovered in 1880 by Jacques and Pierre Curie [[Schils, 2012](#)]. This effect was observed in tourmaline, topaz, calamine, and quartz but not in amorphous materials. The first application of this effect was the ultrasonic submarine detector constructed in France in 1917 [[Katzir, 2012](#)].

Direct piezoelectric effect transforms mechanical stress into electrical charge. This occurs when dipoles of the material are changing polarization because of mechanical stress applied to material.

Since the discovery, huge improvements in piezoelectric materials were obtained. This market of piezoelectric devices was estimated to \$14.3 billion in 2010. The use of piezoelectric materials is very large from well known high voltage generation in lighters to even infertility treatment [[Baltaci, 2010](#)]. Mainly piezoelectrics are used as sound sensors [[Manbachi, 2011](#)], to construct the Atomic Force Microscopes [[European Space Mechanisms & Tribology Symposium, 2001](#)], noise and vibrations attenuators [[Nandi, 2012](#)], piezoelectric motors [[Inaba, 1987](#)] and recently as energy harvesters. This effect is reversible, a mechanical deformation is obtained by applying an electric potential to the material [[Briscoe, 2014](#)]. The reverse piezoelectric effect is very useful in various diagnostic applications *e.g.* wrist blood pressure or hear beat rate monitoring [[Li, 2011](#)] it is also used to detect fatigue cracks in materials [[Sohn, 2010](#)] *e.g.* wind turbines rotor blades [[Taylor, 2014](#)]. The reversibility of the piezoelectric effect is a very important advantage which offers the possibility to use one device to produce vibrations or electricity depending on applied energy, in other words, the same device can be used as a source and a detector of mechanical vibrations.

### 2.2.1.2 *Energy harvesting from walk*

The first application in which piezoelectric material was used as an energy harvester was the concept of powering battlefield equipment by piezoelectric generators embedded in the soldiers' boots. Following [[Starnner, 1996](#)] walk represents 67W of energy for person with 68kg of weight, this is an important amount of available power. Taking into account the efficiencies of piezoelectric harvesters available at that time, the output power was 1-2W from continuous walking. Since the electronic battery charger wasn't efficient enough and the walking comfort was dramatically reduced, the harvester hasn't been accepted as standard soldier's equipment.

Recently the **DARPA**<sup>8</sup> restarted this project improving the electrical battery charger circuit and the soldiers comfort Fig. 2-4 [[Howells, 2008](#)]. Generator output power is around 100mW, enough to supply a cellular phone and geolocalization system based on **GPS**<sup>9</sup>.

<sup>8</sup> **DARPA** - Defence Advanced Research Projects Agency the agency in charge of strategic research for US Army, founded in 1958. It is one of the biggest agency in US Department of Defence with annual budget of \$2.4 billions

<sup>9</sup> **GPS** - Global Positioning System the system used to define the geographical (*longitude and latitude*) position of a user. It uses 31 satellites which are covering all earth, only 3 are necessary to unequivocally localize the user. **GPS** was financed by the US Department of Defence and had only military use nowadays it is one of the most popular tool in truism or travelling.



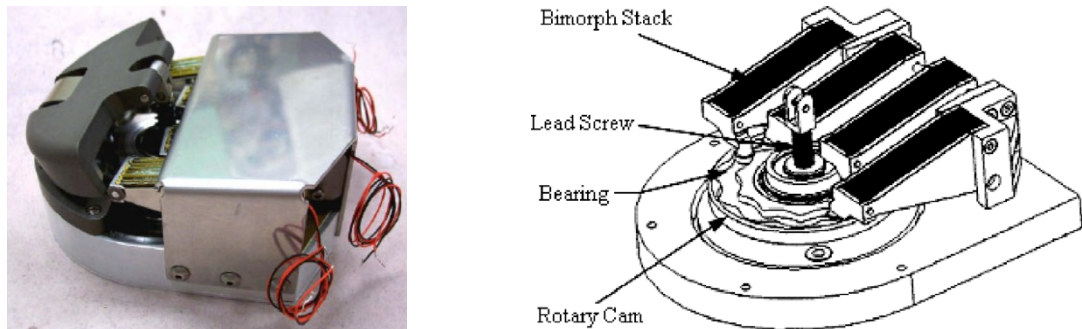


Fig. 2-4 Prototype photo and idea figure of heel piezoelectric energy harvester [Howells, 2009]

High power offered by human walk attracted also civil institution of American giant in sportswear branch Nike®. The company will soon commercialize a shoe capable to communicate with an iPod or a smart phone Fig. 2-5a. The shoe is equipped with piezoelectric generators, voltage boosting block and **WiFi** communication unit. A dedicated communication protocol has been implemented and the data including speed, **GPS** position, number of steps or estimation of burned calories is sent from the shoe to a smart phone. Owing to the use of dedicated applications it is possible to prepare adapted training plan or to control progress of the runner. Other example of piezoelectric energy harvesting is depicted in Fig. 2-5b, based on [Shenck, 2001]. This prototype is equipped with **PZT** energy harvester placed in shoes sole. The harvester is capable of delivering an average power of  $\langle P \rangle = 8.4 \text{ mW}$  at average output voltage of  $\langle V \rangle = 44 \text{ mV}$  from brisk-walking. This is sufficient to supply **Radio Frequency Identification (RFID)** unit which communicates the 12-bit wireless identification code number and actual position of runner.



Fig. 2-5 a) Nike+® shoes for running with piezoelectric generator installed in shoe's heel, b) prototype shoes with piezoelectric harvester and **RFID** electronic circuit [Shenck, 2001]

### 2.2.1.3 Energy harvesting from vehicles

In modern society, we are observing continuous rise of cars quantity. Moreover, modern vehicles are consuming much more electric power than a decade ago. This situation is explained with the development of electronic automotive equipment *e.g.* **CD** player, integrated **GPS** navigation, onboard computer, sensors, camera *etc.* Energy of all onboard equipment has to be produced in alternator or battery, however rising onboard power consumption makes it difficult to supply all receivers simultaneously.

The use of piezoelectric harvesters to convert vehicle vibrations into useful electric energy is a very interesting concept. This additional electric energy can reduce the fuel consumption or simplify the wiring owing to the use of sensor autonomous supply.

But is there enough vibration in vehicles to harvest from, and how much power can be scavenged? The vehicle vibrations have higher frequency than vibrations offered by human walk. Cars are rich in vibrations sources *e.g.* engine block, absorbers, suspension *etc.* An

example of harvesting method from car absorbers is presented in Fig. 2-6 [Zuo, 2013]. Car weight of 1680kg equipped with shock absorber on each wheel produces around 250W when driving at 60km/h.

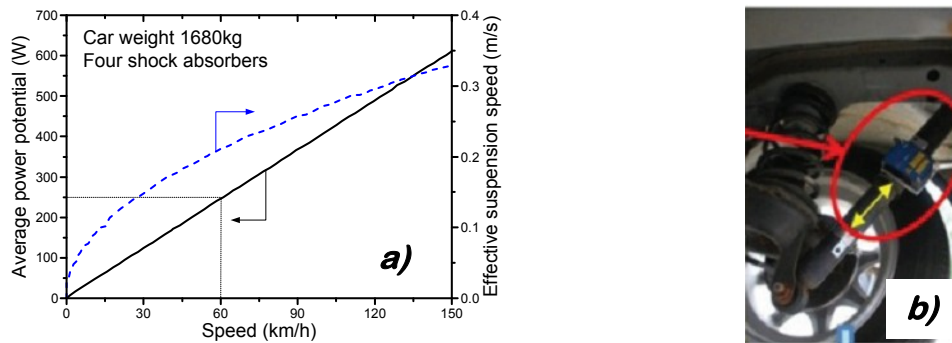


Fig. 2-6 a) Average power potential and effective suspension speed system versus car speed. b) the installation of the measurement device on shock absorber of the rear wheel.

Note that overall electrical requirements of onboard equipment and systems installed in car requires from 2.5kW to 5kW [Miller, 2006]. Thus harvested power from vibrations is significant able to cover 5.5%-11% of overall electric consumption. Result depicted in Fig. 2-6a shows harvesting capabilities of a generator installed on the only one shock absorber. Thus, overall harvested power for a car is more or less four times bigger than this plotted in Fig. 2-6a.

#### 2.2.1.4 Summary of harvesters based on piezoelectric effect

Piezoelectric harvesters are receiving huge interest around the world. Their popularity arises from (i) simple construction, (ii) relatively low price and (iii) significant output power. However, their drawbacks are difficulty to fabricate them using industrial **CMOS** techniques and the character of output energy (*voltage with very high peak values*). Output voltage imposes the necessity to use sophisticated converters, lowering the overall system efficiency. Table 2-3 lists a few examples of piezoelectric harvesters reported in literature.

Table 2-3 Summary of reported piezoelectric harvesters and their parameters

$f$ (Hz)	Excitation ( $m/s^2$ )	Mass (g)	Volume ( $cm^3$ )	$P$ ( $\mu W$ )	Power density ( $\mu W/cm^3$ )	Material	Reference
0.5	N/A	1.2	0.101	0.25	2.47	PZT-5H	[Elvin, 2006]
1.1	N/A	N/A	25	8400	336	PZT dimorph	[Shenck, 2001]
100	72.7	0.96	0.20	35.5	16.3	PZT	[Ng, 2005]
120	2.5	9.2	1	375	375	PZT	[Roundy, 2003]
120	0.98	N/A	N/A	500	N/A	PMNZT	[Jeong, 2008]
13.9	106	N/A	$27 \times 10^{-6}$	1	$37.04 \times 10^3$	PZT	[Jeon, 2005]
1500	3.92	$9 \times 10^{-4}$	0.005	0.03	60	AlN	[Marzencki, 2008]
230	9.8	N/A	N/A	0.27	N/A	PZT	[Kok, 2008]
40	2.5	52.2	4.8	1700	700	PZT	[Roundy, 2005]
462.5	19.6	N/A	N/A	2.15	N/A	PZT	[Shen, 2008]

Continuation Table 2-3 Summary of reported piezoelectric harvesters and their parameters

$f$ (Hz)	Excitation ( $m/s^2$ )	Mass (g)	Volume ( $cm^3$ )	$P$ ( $\mu W$ )	Power density ( $\mu W/cm^3$ )	Material	Reference
50	N/A	N/A	9	180	20	PZT	[Tanaka, 2005]
56	N/A	228	113	$1 \times 10^5$	2650	P1-89 PZT	[Lefevre, 2007-b]
608	9.8	0.0016	0.0006	2.16	3600	PZT	[Fang, 2006]
67	4	2.8	0.987	240	243.1	Screen-printed PZT	[Zhu, 2009]
7000	N/A	N/A	N/A	1600	N/A	PZT-PIC255	[Lu, 2004]
80	2.3	0.8	0.128	2.1	16.4	Screen-printed PZT	[White, 2001]

Studying Table 2-3 leads to the conclusion that the most popular piezoelectric material used for harvesting is **PZT**. Secondly, the piezoelectric harvesters are extremely adjustable to operating conditions the realizable solutions can cover very wide range of vibration frequencies from low frequencies *e.g.* walking person to high vibration frequencies from vibrating machines. Also, the harvested power density range is wide, from few to several thousands of  $\mu W/cm^3$ .

## 2.2.2 Electrostatic energy harvesting

### 2.2.2.1 Basics

Electrostatic interaction between different materials is known since antiquity. However, the storage of electric charge became extremely important with the discovery of electric current and development of electricity usage.

The use of electrostatics to harvest energy is a rather recent discovery. The principle of operation in electrostatic energy harvesters, relies on the use of mechanical forces to perform work against the attraction of oppositely charged capacitor's plates; thus those generators can be considered as mechanically variable capacitors whose plates are vibrated by the movement of the vibration source.

Fig. 2-7 depicts different operating mode of electrostatic energy harvesters. Among those generators we can distinguish two fundamental operation modes: switched and continuous. In the continuous mode harvester is permanently connected to the load. This solution has significant drawbacks firstly the electrical receiver is exposed to high voltages produced by harvester while operating and secondly the harvester has to be permanently biased by internal voltage, thus this solution is rarely used. The switch mode uses electronic switches to modify the generator's external connections depending on the harvester operation state. Within this operation mode the harvester can work with fixed charge or fixed potential [Mitcheson, 2008].

Considering parallel plate structure of variable capacitor, the capacitance can be changed by changing plate's overlap or by changing the distance between the plates Fig. 2-8. When the gap between the plates is increased the electric field strength  $\mathbf{E}$  is decreasing and this force the charge  $\mathbf{Q}$  to be taken from the plates and transferred to an external load. In case of plate's overlap change the electric field strength  $\mathbf{E}$  is constant but the volume of the field changes, this causes the current  $\mathbf{i}$  to flow towards the load. In fixed potential mode

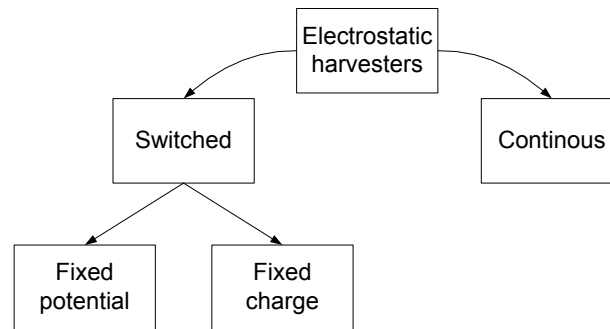


Fig. 2-7 Electrostatic energy harvesters different operation modes [Mitcheson, 2008]

of operation the harvester output voltage  $V$  is constant and the stored electric charge  $q(\text{time})$  is variable Fig. 2-8a, on the contrary, fixed charge operation mode has constant charge  $Q$  and a variable harvester output voltage  $V(\text{time})$  Fig. 2-8b.

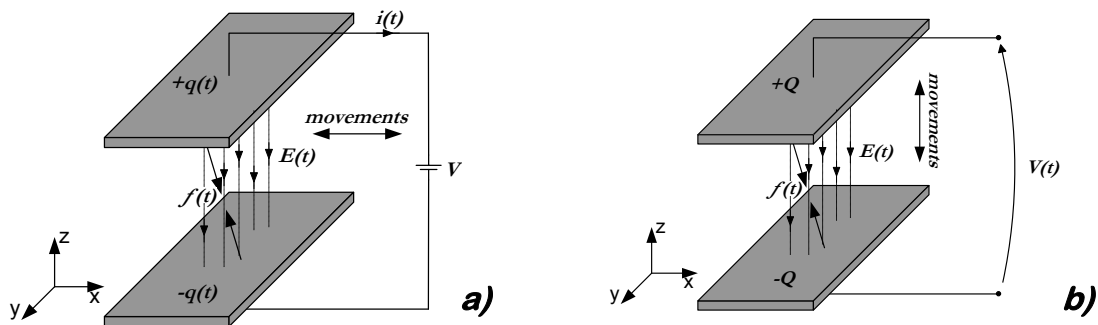


Fig. 2-8 Electrostatic energy harvester operating with a) fixed potential b) fixed charge

Regardless the operation mode, the mechanical work executed in harvester is always against the attractive electrostatic force, this work is transformed into electrical energy. The charge and potential ( $V$ ) are coupled by the electrical capacity ( $C$ ) Eq. 2-1 and energy ( $E$ ) stored in capacitor depends on capacitance and potential Eq. 2-2. Electrostatic force ( $F_C$ ) upon which the work is done depends on the potential and the capacitance change along the movement axis, Eq. 2-3 describes the electrostatic force component along  $z$ -axis.

$$Q = C \cdot V \quad \text{Eq. 2-1}$$

$$E = \frac{C \cdot V^2}{2} \quad \text{Eq. 2-2}$$

$$F_{Cz} = \frac{V^2}{2} \cdot \frac{dC}{dz} \quad \text{Eq. 2-3}$$

Despite rather new concepts of energy harvesting, many different harvesting topologies are possible, some examples are showed in Fig. 2-9.

The difference between the harvesting structures depicted in Fig. 2-9 firstly relies on the relative movement direction between stator and vibrating parts. Secondly, it relies on the topology according to Fig. 2-9 two main structures can be distinguished, first with flat capacitor plates (Fig. 2-9a-d) and comb-like capacitor plates (Fig. 2-9e-f). To maximize the generator capacitance the comb-like plates are preferred because their surface is higher than for flat plates. As a result, the topologies Fig. 2-9e-f are much more popular in practical realizations.

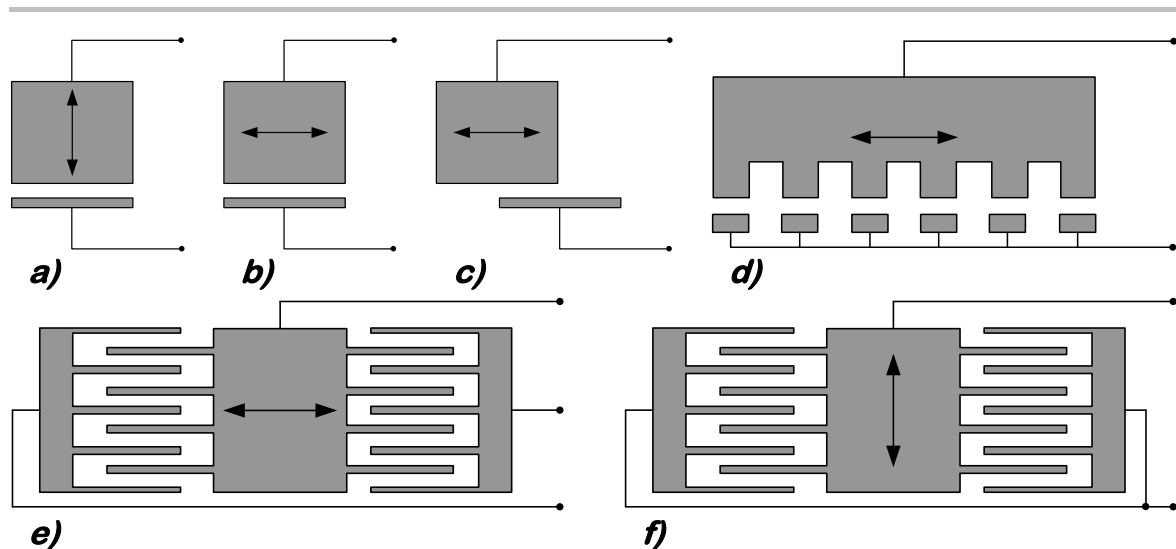


Fig. 2-9 Topologies of kinetic energy electrostatic harvesters. Double arrow shows the vibration direction a) out-of-plane gap closing; OP b),c) and d) in-plane overlap varying IPO; e) in-plane overlap varying; f) in-plane gap closing IPCG

#### 2.2.2.2 Energy from variable capacitance

Fabrication of electrostatic harvester was reported in [Amirtharajah, 2000] and [Meninger, 2001]. The particularity of this device is the small dimensionality and the compatibility with **CMOS** technology.

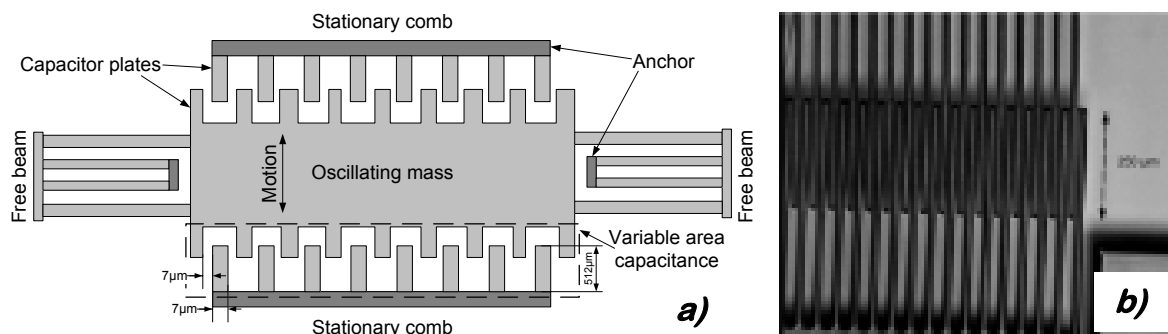


Fig. 2-10 Electrostatic energy harvester a) side view, b) SEM photo on capacitor plates [Meninger, 2001]

Principle of operation for those harvesters relies on the change of electrical charge stored in the capacitor. Fig. 2-10a depicts the side view of this generator. In contrary to piezoelectric generators an external polarization voltage has to be applied in those types of harvesters. The central part of harvester is mechanically suspended allowing only vertical movements and attenuate as much as possible movements in lateral direction. The capacitor plates in form of fingers are installed in central oscillating mass and in stationary comb. When vibrations occur the fingers of the oscillating mass are sliding in between the fingers of the stationary comb, leading to a variation of the capacitor surface. When the capacity is at its maximum value the electric charge stored in the capacitor is transferred to the external battery. Detection when the capacitor should be discharged involves the use of complicated control system. On Fig. 2-10b the picture of capacitor plates is shown. To ensure good capacitive coupling between the oscillating mass and the stationary comb the distance between the fingers has to be as small as possible. In this application the distance is  $7\mu\text{m}$  with the finger's length of  $512\mu\text{m}$ . The small dimensionality of this harvester explains the necessity to use precise methods of nano- and micro-fabrication.

The harvester has to be equipped with: (i) advanced control system responsible for determination of discharge instance, (ii) voltage boosting unit and (iii) system which controls the battery charging. All this additional circuitry has a significant impact on overall system efficiency. The harvester internal load presents significant power Table 2-4:

**Table 2-4 Internal load in harvesting system based on electrostatic generator [Amirtharajah, 2000]**

Unit name	Power ( $\mu$ W)
Total harvester output power	8.66
Discharge instance controller	0.50
Switch losses in controller	3.87
System output power	4.29

Table 2-4 shows that the power consumed in the control unit represents half of total energy harvested in electrostatic generator. The significant internal load and necessity of external polarization are the biggest drawbacks of those harvesters. However, the energy can be harvested from very wide range of vibration frequencies, high internal impedance of the harvester makes it ideal voltage source. Available output power is sufficient to supply some micro-power consumption devices and finally fabrication of this type of generator is compatible with **CMOS** technology which is industrial cost effective production method.

Despite the advantages of those harvesters, this solution still represents the smallest group among mechanical energy harvesters. There is still a need to improve the controller in such a way to reduce the internal power consumption. On account of the advantages, electrostatic harvesters are a promising solution for **CMOS**-compatible, low cost, micro scale energy scavengers.

### 2.2.2.3 Energy from heart

One of the interesting and innovative project which uses electrostatic energy harvester is the vibration recovery from heart beats. Number of heart beats per minute depends on various factors (*e.g. age, life-style, organism load, etc.*) however the average beat rate per minute of human heart is 72bpm<sup>10</sup> (1.2Hz) [Hall, 2011]. Each heart movement represents some quantity of energy, the goal is to use heart movements to transform into electricity which finally is used to supply heart monitoring device or pacemaker. Owing to this alternative way to supply monitoring device the battery size mounted in patient's body can be reduced. Moreover, the monitoring of heart work can be realized observing the quantity of energy harvested during a given time. When the harvested energy is lower than an alert level this can signify that the heart is slowing down and a medical examination is required.

Progress in medical sciences is very long due to numerous obligatory tests before first application to human body. Till now, this concept was carried out on the goat heart [Tashiro, 2000]. The authors measured how much energy represents the working heart by installing an accelerometer on the wall of goat's heart.

<sup>10</sup> bpm – Beats per minute. Number of heart's beats during 1 minute. Physical effort temporary increases the heart's beat rate but decreases bpm while resting. Thus professional athletes have usually resting bpm value largely under average from 50-60bpm. Making heart to increase bpm is in most cases good for heart's health.

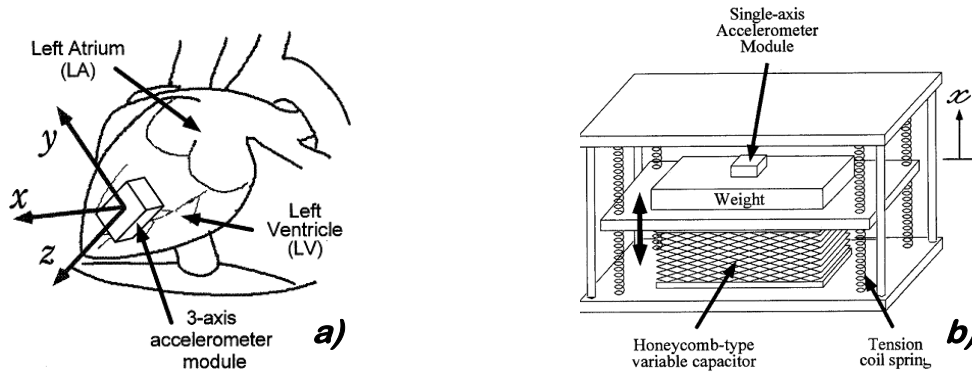


Fig. 2-11a) Accelerometer installation on the heart's wall b) electrostatic energy harvester with ultralow resonance frequency  $f_t=4.76\text{Hz}$  design to harvest energy from heart's beats [Tashiro, 2000]

The measurements of heart harvesting capabilities resulted in conclusion that the goat beat rate ( $96\text{bmp}\approx 1.6\text{Hz}$ ) is significantly higher than the human rate. The **FFT** (**F**ast **F**ourier **T**ransform) analysis of hear beats was also investigated concluding that surprisingly the 3<sup>rd</sup> harmonics represents the highest accelerations in  $xyz$  directions. Thus, the vibrations with frequency corresponding to 3<sup>rd</sup> harmonics are carrying the highest energy. In consequence, the harvester was designed in such a way to reach the resonant frequency of  $f_t=4.76\text{Hz}$  very close to 3<sup>rd</sup> harmonics frequency.

The harvester is equipped in an adapted topology of honeycomb capacitor, which ensures high mechanical flexibility and long lifetime. The weight of the harvester  $m=640\text{g}$  and the capacitance change during one cycle  $C_{MAX}=110\text{nF}$   $C_{MIN}=30\text{nF}$  delivers  $E=12.5\mu\text{J}$  of energy per cycle. Operating with frequency of  $f_t=4.76\text{Hz}$  it produces  $P_{OUT}=59.5\mu\text{W}$ . The output power depends on the load resistance, as previously mentioned, the electrostatic harvesters have very high internal impedances. Thus when the load resistance rises the harvester performance is rising as well due to the impedance matching Table 2-5.

Table 2-5 Harvesting capabilities for different load resistances [Tashiro, 2000]

Load resistance ( $M\Omega$ )	Output voltage (V)	Output power ( $\mu\text{W}$ )
0.20	1.14	6.5
0.50	4.00	32
1.00	7.60	58
2.00	13.9	97

This innovative and futurist concept of alternative power supply for pacemakers is still in the stage of medical tests. There is a high possibility that it will soon be commercialized.

#### 2.2.2.4 Summary

The electrostatic harvesters are representing one of the smallest group among all harvesters converting from mechanical energy. The possibility to fabricate them using **CMOS** technologies is an important advantage. Table 2-6 lists the parameters of a few electrostatic harvesters reported in the literature. Worth noting is the fact that those harvesters have not as high power density as other harvesters types *e.g.* piezoelectric or electromagnetic. The electrostatic harvesters can harvest energy from low and high frequencies vibrations, which is an advantage. Like for the other kinetic energy harvesters the output power is maximized when input vibrations have a frequency close to the harvester resonant frequency. Thus, usually the mass of the generator is inversely

proportional to the vibration frequency. The electrostatic harvesters are the generators which are most likely to be miniaturized. As a result of the development of lithography and etching techniques it is now possible to fabricate capacitors with very good control of the distance between the plates. However, their significant drawback is the necessity to externally polarize the capacitor. This deficiency is limiting the autonomy of the device since it has to be installed along with a voltage source capable of pre-charging the harvester capacitance.

**Table 2-6 Summary of electrostatic kinetic energy harvesters**

$f$ (Hz)	Excitation ( $m/s^2$ )	Mass (g)	Volume ( $cm^3$ )	$P$ ( $\mu W$ )	Power density ( $\mu W/cm^3$ )	Type	Reference
2	3.92	N/A	N/A	40	N/A	IPGC	[Naruse, 2009]
6	1	780	N/A	36	N/A	OP	[Tashiro, 2002]
10	3.9	N/A	0.80	6	7.5	IPO	[Arakawa, 2004]
30	50	0.1	0.75	3.7	4.93	N/A	[Mitcheson, 2003]
50	8.8	104	1.80	1052	584.44	IPGC	[Despesse, 2005]
50	576.6	54	50	17.98	0.359	OP	[Lo, 2008]
500	9.8	N/A	N/A	5	N/A	OP	[Sterken, 2007]
1000	1.96	N/A	N/A	4.28	7.9	IPO	[Kuehne, 2006]
1300	127.4	$642 \times 10^{-6}$	N/A	3.5	N/A	IPO	[Hoffmann, 2009]
1560	82.32	N/A	N/A	1.8	N/A	OP	[Yen, 2006]
2520	N/A	N/A	0.075	8	106.66	IPO	[Meninger, 2001]
743	N/A	0.7	0.6	$7.4 \times 10^{-6}$	$1.23 \times 10^{-3}$	OP	[Mizuno, 2003]

OP: out-of plane

IPO: in-plane overlap

IPGC: in-plane gap closing

Table 2-6 compares few examples of electrostatic harvesters, emphasizing the topology of the device. The different harvester structures allow to generate the energy from vibrations in lateral or vertical direction. The use of interdigitated structure of capacitor (e.g. Fig. 2-9e and Fig. 2-9f) boosts the capacitance due to the higher capacitor plate surface. This solution significantly improves the output power density because the harvester capacitance is significantly raised without big impact on its volume.

## 2.2.3 Electromagnetic energy harvesting

### 2.2.3.1 Basics

Since its discovery in 1831 by Michael Faraday [Feynman, 2011], electromagnetic induction become the most popular way to produce electric energy. Electric generators are producing electricity on the level of a few watts (e.g. brushless DC motors in domestic wind turbines) [Vukosavic, 2013] or of few hundred megawatts (synchronous turbo- or hydro-generators) [Sen, 2013] and are using electromagnetism to convert the mechanical rotation of a rotor into electric energy. Progress in high-performance permanent magnets and multiturn macroscale coils allowed the simplification and miniaturization of electromagnetic generators. However, micro-scale systems are still difficult to achieve



mainly because of poor properties of planar magnets, limited number of turns available in planar coils and finally due to small relative velocity between magnet and coil.

The electromagnetic micro-scale harvester is one of the largest group among all known energy harvesters as depicted in Fig. 2-1. The reason for this is: (i) well-established technique background, (ii) well reported physics of electrical power generation and (iii) progress in coil and magnet fabrication which is improving stator-rotor electromagnetic coupling. However, those generators are facing complicated fabrication problems (*moving parts, shaft bearings, coil fabrication or magnet installation*) and this significantly rises the fabrication costs.

The physics of this effect relies on the induction of electric potential in a magnetic coil when exposed to alternative magnetic field. The induced electric potential ( $e_{ind}$ ) can be calculated using Eq. 2-4 [Chapman, 2005]:

$$e_{ind} = -N \cdot \frac{d\Phi}{dt} \quad \text{Eq. 2-4}$$

$$e_{ind} = (\vec{v} \times \vec{B}) \bullet \vec{l} \quad \text{Eq. 2-5}$$

where  $\Phi$  is the magnetic flux passing through one turn of the coil with  $N$  turns. The general case equation Eq. 2-4 can be simplified, when considering the wire with length  $l$ , moving at speed  $v$  in magnetic field of induction  $B$ . Induced potential can be calculated using Eq. 2-5. Eq. 2-5 describes the physics of electric energy production in generators. The generator is equipped with two mechanically decoupled windings on the rotor and on the stator Fig. 2-12a [Krause, 2012], [Lipo, 2012]. The magnetic field is excited using a **DC** current flow in a rotor winding or using instead a permanent magnet placed on the rotor. When the shaft of the machine is driven with angular speed  $\omega$  (*propulsed by e.g. vapour turbine, wind, water flow etc.*), the lines of magnetic field are crossing the winding placed in stator and this induces the electric potential  $e_{ind}$  in stator winding Fig. 2-12b.

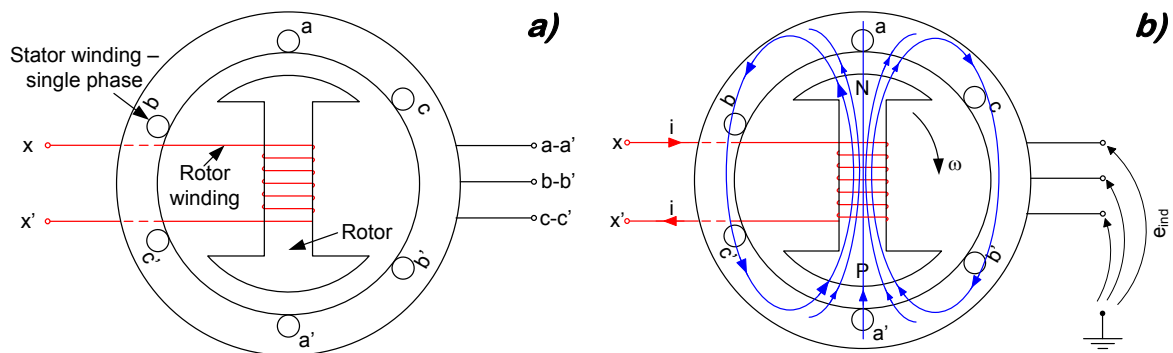


Fig. 2-12a) Synchronous machine placement of rotor and stator windings b) generative operation mode – induction of  $e_{ind}$  in stator winding

The vast majority of electric energy is produced in such a way. The practical realization of a generator is costly and precise operation Fig. 2-13. Although the rotor winding can be replaced by a permanent magnet, the stator winding has to be realized precisely. The quality of this stator winding plays a very important role in the phase shift between induced voltages in each phase and in the amplitude of induced voltage. The prize of the machine is mainly imposed by the stator fabrication [Pyrhonen, 2013].

Fabrication of electric machines at macro scale is well established, known and practiced procedure. However, realizing a micro-scale machine is a new concept. The miniaturization of electrical machines is mainly possible due to two important reasons. Firstly development of efficient permanent magnets allowed replacing the rotor windings with magnets [Gieras, 2010], [Szumanowski, 2013]. Secondly, the development of electronics allowed implementing efficient machine control techniques and this enables reduction of machine's size keeping similar performance [Herman, 2014], [Mohan, 2014], [Santos Jr., 2015] and [Weidauer, 2014].

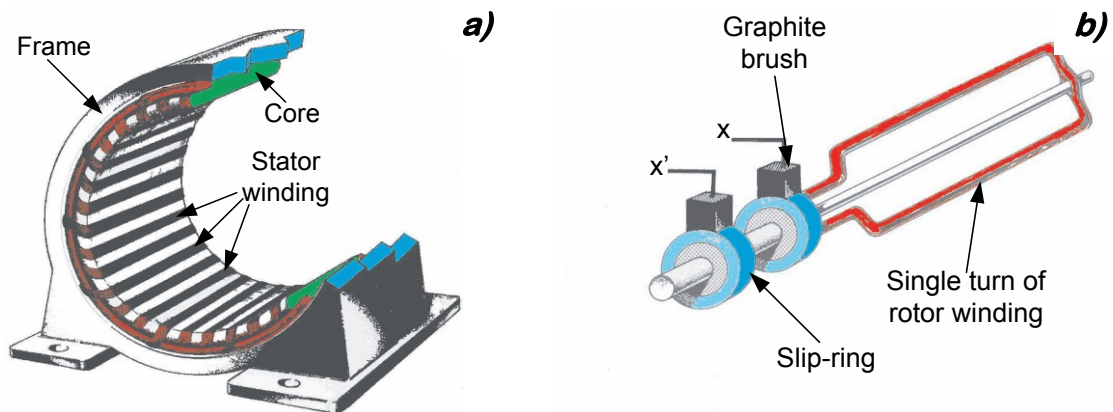


Fig. 2-13 Practical realization of a) stator winding and b) rotor winding in synchronous machine [Veltman, 2007]

The following part presents applications of electromagnetic energy harvesters with the use of micro- or mili-scale electric generators.

### 2.2.3.2 Energy for watch

The first historical use of electromagnetic harvester is reported in a patent [Hayakawa, 1989] by Seiko Epson Co. The patent describes the self supplied wrist watch by the use of self-winding electromagnetic generator Fig. 2-14.

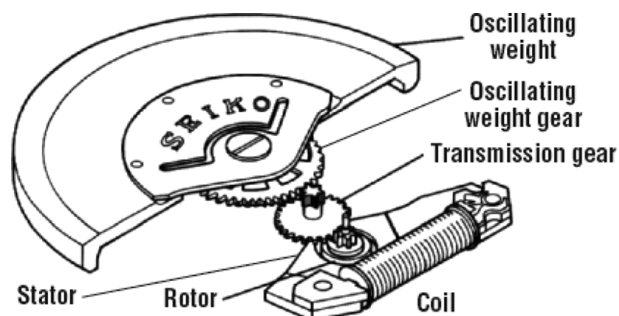


Fig. 2-14 Concept view of self-powered wristwatch with the use of electromagnetic generator [Hayakawa, 1989]

This concept relies on the use of rotating flywheel which is driving the rotor of electromagnetic generator through transmission gear. The generator uses permanent magnet as excitation. The quartz digital wristwatch requires from  $20\mu\text{W}$  to  $40\mu\text{W}$  and this generator concept produces enough energy to cover totally the needs of wristwatch.

## 2.2.4 Energy from indoor wind

Development of electronic devices, control techniques and permanent magnet technology allowed the miniaturization of electric machines. Owing to this miniaturization it is now possible to install them almost everywhere.

As a result of above mentioned size reduction a very interesting concept to produce electric energy from indoor airflows [Howey, 2011] was proposed. The principle of operation is equivalent to well-known wind turbines used at macro-scale. Power of airflow or wind can be calculated using Eq. 2-6 [Weimer, 2006]:

$$P = \frac{1}{2} \cdot \rho \cdot A \cdot V^3 \quad \text{Eq. 2-6}$$

$$P = \frac{1}{2} \cdot C_p \cdot \rho \cdot A \cdot V^3 \quad \text{Eq. 2-7}$$

where  $P$  is harvested power,  $\rho$  is the air density  $A$  is the sweep area of the wing turbine blade and  $V$  is the wind speed. Power produced in wind mill follows Eq. 2-7. The maximal theoretical value of  $C_p=16/27$  is called the Betz limit [Betz, 1927], only large scale wind turbines with very high mechanical-to-electrical conversion efficiency can approach this limit. However, small wind turbines have significantly reduced  $C_p$  because their leakages and losses are playing much important role. Fig. 2-15 depicts the performance of some reported micro-scale wind turbines.

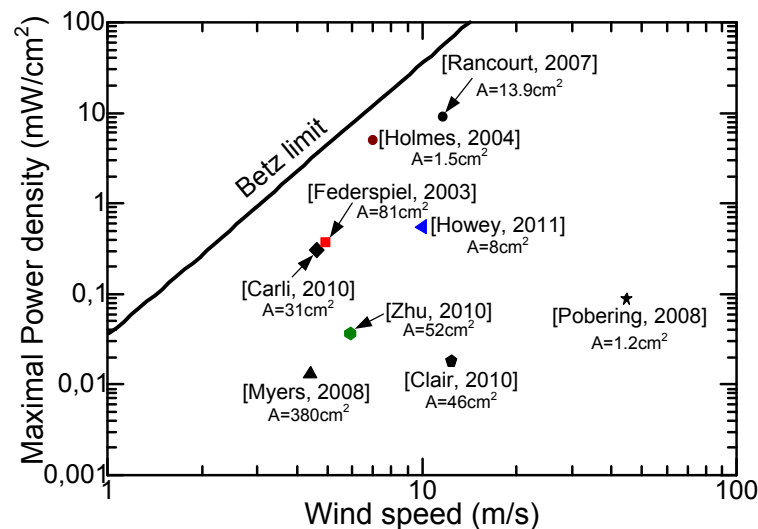


Fig. 2-15 Maximal value of harvested power density versus wind speed for reported in literature micro-scale wind turbines. The harvester surface placed under the reference.

Studying Fig. 2-15 leads to the conclusion that indoor airflows allow to produce significant power on the order of few hundreds mW. According to [Matiko, 2014] the airflow with a speed from 1 to 10m/s represents from 0.9 to 324mW of electrical **DC** power. Those wind turbines can be installed in the air conditioning or/and ventilating systems where airflows are very high. Table 2-7 evaluates the **DC** power from domestically available fans.

**Table 2-7 Domestically available sources of air flow and the maximal harvested power [Matiko, 2014]**

Air source model	Air speed at 0cm from fan (m/s)	Estimated DC power (mW)
Air flow <sup>®</sup>	10.50	324.1
Dunham-Bush 21-240B	6.10	63.6
Daikin—unit 1	3.30	10.1
Rear notebook fan 120mm	1.50	0.9
Front notebook fan 120mm	2.00	2.2

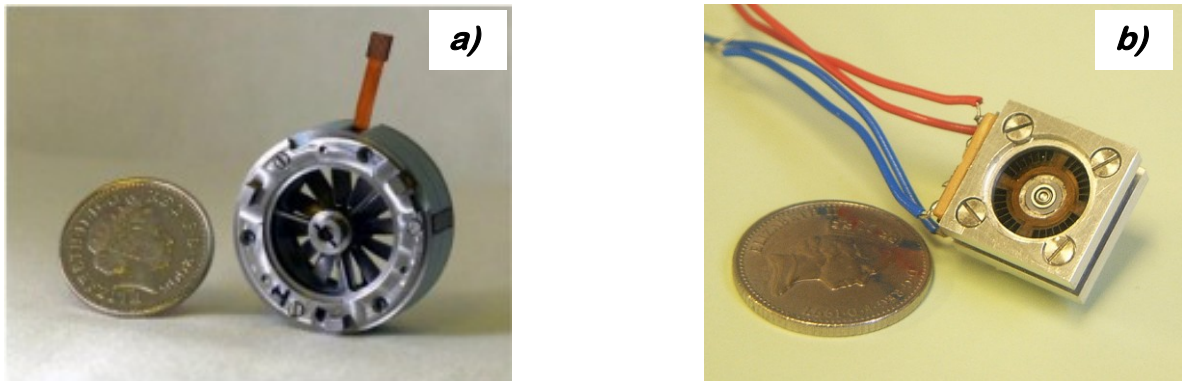


Fig. 2-16a) Micro wind turbine to harvest from domestic airflows turbine diameter  $\phi=3.2\text{cm}$  blades surface  $A=8\text{cm}^2$  [Howey, 2011], b) The smallest reported wind turbine. External dimensions  $18\times 18\times 9\text{mm}$  blades surface  $A=1.5\text{cm}^2$  [Holmes, 2004]

Fig. 2-16a and b show the examples of micro-scale generator dedicated to energy harvesting from indoor airflows. The harvesting from indoor airflows is possible because of very low friction losses in bearings and owing to the use of permanent magnets. Full composition of micro-scale wind generator is presented in Fig. 2-17a.

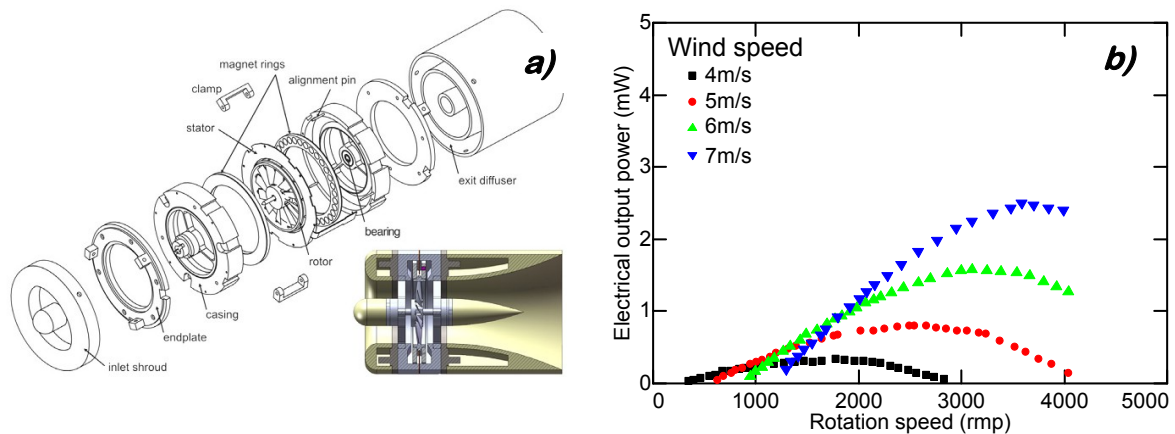


Fig. 2-17 a) The exploded and cross-sectional view on micro-scale wind mill b) generator output power in function of shaft rotation speed for different wind speeds [Howey, 2011]

As shown in Fig. 2-17a the generator has complicated structure, with a lot of parts to assemble. In micro-scale the most problematic is fabrication of good quality bearings with extremely low friction losses and to ensure as small as possible air gap between rotor and stator. However, the harvested gross output power is high Fig. 2-17b, up to 3mW for 7m/s of wind speed. Worth noting is the very high rotation speed of the shaft, this demonstrates that the friction losses are significantly reduced in this generator.

One of the smallest wind turbine reported in the literature is showed in Fig. 2-16b [Holmes, 2004]. This generator has external dimensions of  $18\times 18\times 9\text{mm}$  and area of blades

$A=1.5\text{cm}^2$ . The rotation speed of this turbine can be as high as 140 000rpm and it can produce maximal power of 8mW when wind speed is 7.4m/s.

#### 2.2.4.1 Summary

To summarize the electromagnetic harvesters Table 2-8 provides some examples reported in the literature.

**Table 2-8 Summary of electromagnetic kinetic energy harvesters**

$f$ (Hz)	Excitation ( $\text{m/s}^2$ )	Mass (g)	Volume ( $\text{cm}^3$ )	$P$ ( $\mu\text{W}$ )	Power density ( $\mu\text{W}/\text{cm}^3$ )	Material	Reference
25	N/A	15.6	2.000	3.97	1.98	Styrene	[Kulah, 2008]
50	0.589	N/A	0.570	58.00	101.75	BeCu	[Torah, 2008]
52	0.589	0.66	0.150	46.00	306.67	BeCu	[Beeby, 2007]
60	N/A	0.22	1.00	100	100	Silicon	[Li, 2000]
84	7.8	25	0.800	3500	4375.00	Cu	[Saha, 2006]
85	1.96	0.14	7.30	830	114	NdFeB	[Lee, 2003]
100	N/A	0.03	0.04	1.44	40	Si+Cu	[Huang, 2007]
110	95.5	N/A	1.000	830	830.00	Cu	[Ching, 2001]
280	10	N/A	0.315	17.20	153.20	Ni	[Wang, 2009]
322	2.7	N/A	0.840	180	214.30	Steel	[Glynn-Jones, 2004]
322	N/A	0.50	0.24	530	2208	Cu	[El-hami, 2001]
350	3	0.44	0.06	2.85	47.5	Steel	[Beeby, 2006]
700	N/A	0.54	2.10	$4 \times 10^{-4}$	$0.2 \times 10^{-3}$	N/A	[Mizuno, 2003]
1615	3.92	N/A	0.100	0.104	1.04	Silicon	[Koukharenko, 2006]
4400	382	0.0023	0.054	0.30	5.55	GaAs Poly	[Williams, 2001]
9500	9.81	0.03	0.10	0.02	0.21	Si+Cu	[Beeby, 2005]

Table 2-8 presents the list of electromagnetic harvesters which are harvesting energy from vibrations. Worth noting is the fact that those generators are realisable for low-frequency and high-frequency harvesting, the range of operation frequencies is from 25Hz to 4.4kHz. Harvested power density follows the wide range of operation frequencies, the reported power densities are comprised between around  $1\mu\text{W}/\text{cm}^3$  and  $4\text{mW}/\text{cm}^3$ . Such a big dispersion of available parameters in those harvesters is caused by different construction materials, vibration parameters, oscillatory mass and harvester size.

However, it is important to note that the electromagnetic harvesters are one of the most complicated and difficult to fabricate. This is due to fabrication issues of magnetic coil and necessity to control the fabrication of thin gaps between the coil and the exciter of magnetic field. Moreover, since the principle of operation of those harvesters relies on the exciter movement in reference to the coil the mechanical phenomena such as fatigue, noise, self-vibration are occurring and it is limiting the generator's lifetime.

## 2.3 Energy from Radio Frequency waves

The wireless energy transmission dates to the experiments of Heinrich Hertz in the 1880s, those experiments proved the Maxwell electromagnetism theory [Feynman, 2011]. Wireless energy transmission was used in the late 1950s [Brown, 1984] for applications in solar power satellites [Glaser, 1968] and microwave powered aircrafts [Brown, 1969]. Recently the concept of wireless power transfer regained interest due to increasing sources of **Radio Frequency (RF)** in the world. The interest was ignited by the short-range (less than 2m) **Radio Frequency IDentification (RFID)** devices used in industry, science and medical environment. Such devices are running on the frequency bands of 0.9, 2.4 and 5.8 GHz or higher [European Radiocommunications Committee, 2011], [Federal Communications Commission, 2015] or [ARIB, 2003]. With increasing frequencies the wavelength becomes small enough to enable the fabrication of miniature **Wireless Autonomous Transducers System (WATS)** [Fruehauf, 2000], [Inman, 2006] and [Mattelaer, 2006]. The importance of **RF** energy harvesting arises from the possibility to supply these systems from **RF** waves.

Exploding quantity of communication devices able to operate in wireless mode requires a big quantity of equipment able to provide the electromagnetic waves ensuring communications. In modern environment there are a lot of examples of radiating devices used in ordinary life situations, Fig. 2-18 presents a few of them:



Fig. 2-18 Chosen examples of radiating sources

Fig. 2-18 shows chosen examples of radiating sources working in surrounding environment, the omnipresence of various electromagnetic waves opens an opportunity for energy scavenging. The density of received **RF** power depends significantly on emitter-receiver distance, communication frequency, environment (*urban, industrial, rural etc.*) and conditions (*air humidity, number of obstacles to cross etc.*). Measured **RF** peak power densities from **GSM900** (935-960MHz) network for different environments is presented in Fig. 2-19a The highest **RF** power density is observed in urban zones where the density of radiating devices (*e.g. WiFi hotspots or GSM*) is the highest, for small distances the power density can be as high as  $15\text{mW/m}^2$ . The smallest **RF** power density is measured in rural zones around  $1\mu\text{W/m}^2$  as shown in Fig. 2-19a, due to small number of radiating devices. The instantaneous value of **RF** power density was measured in an urban zone in the city of

Tours in France. Average daily value of **RF** power density equals  $-12\text{dBm}/\text{m}^2$  ( $35.5\mu\text{W}/\text{m}^2$ ) Fig. 2-19b [Bouchouicha, 2010].

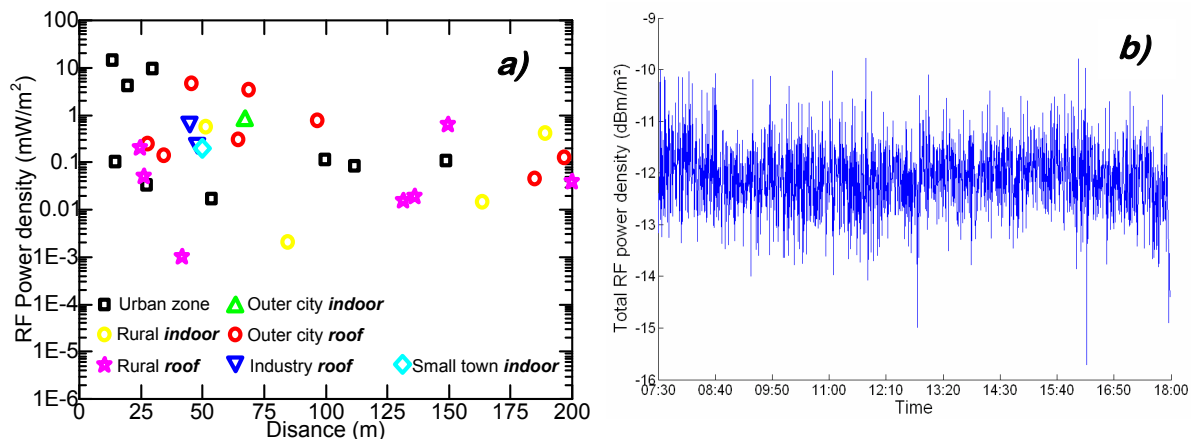


Fig. 2-19 a) Radio frequency (**RF**) peak power density from GSM900 (935-960MHz) network measured in different places emphasizing the placement of measurement unit [Visser, 2008], b) total **RF** power density against time measured in urban zone [Bouchouicha, 2010]

Fig. 2-19b depicts the character of radiating waves in time domain, it is shown that the total **RF** power has a high dispersion of instantaneous values. This character of **RF** radiation is one of the biggest disadvantages of this energy harvesting method. The value of available energy changes each instant and harvesting the power from a continually changing source is problematic and requires extremely fast harvesting devices. Despite the omnipresence of radio frequency waves, the big drawback of this method is the strong dependency on: (i) distance and communication conditions, (ii) number of obstacles, (iii) weather, (iv) air humidity. Fig. 2-20 depicts the harvested **DC** power from **WiFi** hot spot against the distance [Duangsuwan, 2009].

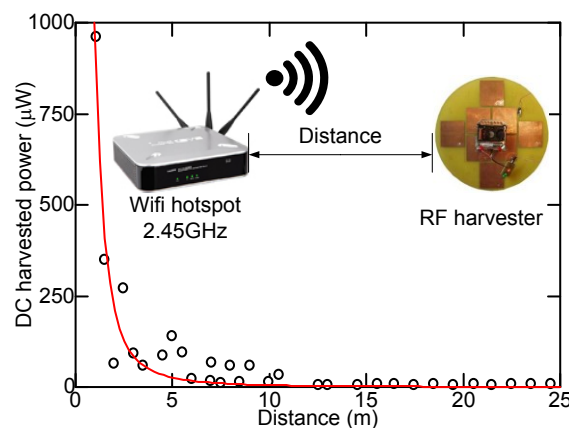


Fig. 2-20 Harvested power from **WiFi** hotspot with 10W broad-beam antenna and transition frequency of 2.45GHz against the distance measured in an office corridor [Duangsuwan, 2009].

Fig. 2-20 shows clearly that the distance dependence of **RF** power is very strong. Placing the harvester as close as possible to the emitting source boosts harvested power, however in some situations such placement is problematic.

Despite rather low available power densities, comparing with other harvesting possibilities, this method of harvesting is very comfortable and promising. Mainly due to the omnipresence of **RF** waves but also owing to continually increasing quantity of emitting devices. The rising number of **RF** emitters makes the waves cover the area with higher density and as a result of that the generator can harvest higher power.

### 2.3.1 Basics

As mentioned before, **RF** energy harvesting is the most interesting to be implemented in **GSM900** (890.0 - 915.0 MHz) and **GSM1800** (1805.2-1879.8 MHz) and in **WiFi** networks (2.4 GHz). The choice of those three systems is not random, they are very popular and thus covering almost all territory with very high density in urban zones. Moreover, the operation frequencies for those systems are high enough enabling the miniaturization of receiving antennas, the main part of the harvester. High operating frequency enables also the signal propagation in ambient air, on the other hand the communication range is inversely proportional to operation frequency [Paul, 2011].

Converting **RF** waves into electric energy relies in electromagnetic coupling between emitting device and harvester. The harvester is tuned in such way to achieve impedance matching and thus to boost the harvested power. The **RF** power received by the harvester has very high frequency as presented already in Fig. 2-19b and a rectification has to be performed. Subsequently, the voltage is boosted in the converter unit, and afterwards the harvested energy is stored in a capacitor or a battery. This conversion chain is depicted in Fig. 2-21 [Visser, 2013].

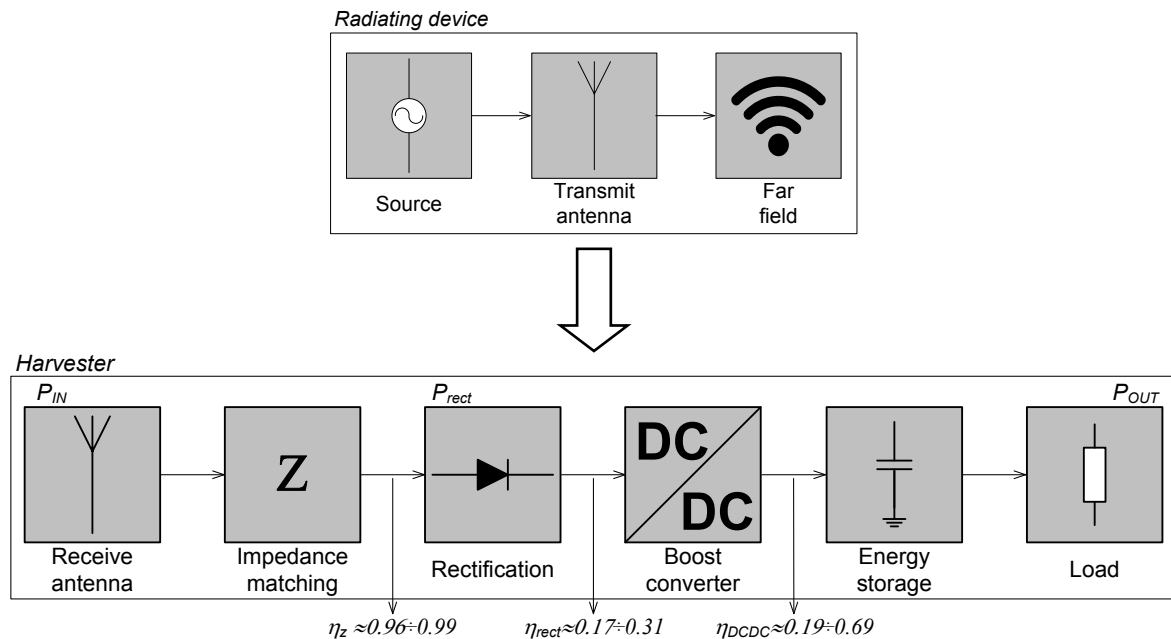


Fig. 2-21 Conversion chain of **RF** harvester emphasizing the efficiency of impedance matching  $\eta_z$ , rectification  $\eta_{rect}$  and boost converter  $\eta_{DCDC}$  units [Visser, 2013]

Fig. 2-21 illustrates the conversion chain of energy harvesting from **RF** waves. Each unit in the chain lowers the overall harvester efficiency. The blocks responsible for the highest losses are: (i) rectifier  $\eta_{rect} \approx 17\% \div 31\%$ , (ii) boost converter  $\eta_{DCDC} \approx 19\% \div 69\%$  and (iii) impedance matching unit  $\eta_z \approx 96\% \div 99\%$ . Overall conversion efficiency for the rectenna<sup>11</sup> [Torrey, 1980] is  $\eta_{TOT} \approx 3.2\% \div 21\%$  [Visser, 2013]. Referring to the reported efficiencies of harvester inner systems it can be concluded that the losses are mainly formed in rectification unit and **DC-to-DC** boosting converter. Efficiencies of those units can be improved by using **ZVS**<sup>12</sup> and/or **ZCS**<sup>13</sup> switching techniques. However, with such

<sup>11</sup> Rectenna describes receiving antenna, impedance matching unit, rectification unit and boosting converter.

<sup>12</sup> **ZVS** – Zero Voltage Switching is the switching strategy which allows elimination of turning-on losses. This switching requires a modified topology of the converter allowing to achieve the resonance during the



high input signal frequency to rectify, implementation of those techniques is problematic. Secondly, harvester efficiency is strongly dependent on the input power, when the input power rises, the conversion efficiency is also rising. The explanation of this situation relies in the fact that the relative effect of generator imperfections and leakages is more important as the input power is low.

As conclusion it can be noted that **RF** energy harvesting is a kind of electromagnetic harvesting described in the section 2.2.3 but using very high frequencies. For those operation frequencies the signal propagates in ambient air without necessity of physical connection between emitter and receiver (*e.g. wires or cables*).

### 2.3.2 Wirelessly supplied wall clock

**RF** energy harvesters is one of the youngest group among all known harvesters it has been employed in the 1950s and significantly improved in 1970s but those applications were of military use and not widely accessible. Recent progress in wireless communication systems and their fast growth on the market lead to ordinary civil solutions.

One of the examples that **RF** harvesters can become domestic alternative power suppliers is to power the wall clock by **RF** energy coming from **WiFi** network [Theeuwes, 2007]. The rectenna of the harvester is tuned to be the most efficient at 2.45GHz frequency which is the nominal value for wireless hotspots. The fabricated harvester is presented in Fig. 2-22:

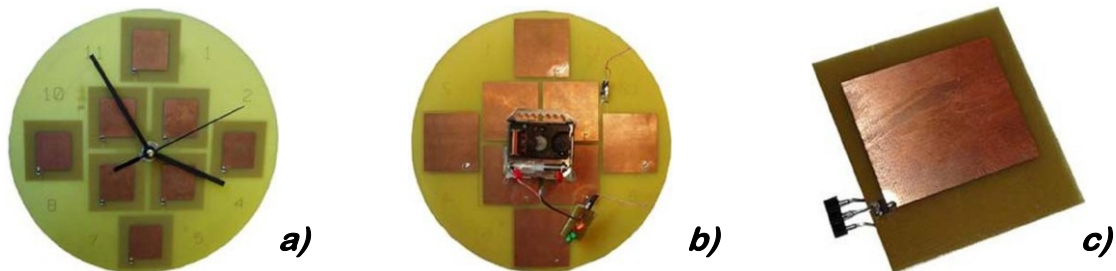


Fig. 2-22 Wirelessly powered wall clock equipped with **RF** energy harvester scavenging energy from 2.45GHz **WiFi** network a) front view b) back view c) photo of single rectenna [Theeuwes, 2007]

The reported **RF** harvester consists of eight rectennas connected in series to boost the output voltage. On account of the use of impedance matching and fast low leakage Schottky diode (*diode reference HSMS-2852*) the overall harvester efficiency is as high as 51% (*for input power level of 0dBm 1mW*), which is a high result for this type of harvester. Building the system dedicated to work with very high frequencies is a difficult task because when working at high frequencies the system becomes more sensitive on imperfections and leakages. Thus the used devices and design quality plays crucial role. The harvester is able to cover totally all energetic requirements of the clock up to 6m of distance from the radiating source of 100mW (*20dBm*).

The main designing problem in those solutions is the big significance of parasitic capacitance and inductance of used components. When converting the signals with very

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operation cycle. The **ZVS** contributes in reduction of switching losses formed in the switch and in reduction of electromagnetic perturbation in both conduction and emitting type [Rashid, 2011]

<sup>13</sup> **ZCS** – Zero Current Switching is the technique allowing elimination of switching losses when turning off and reduction of the losses when turning on. As **ZVS** this technique requires the resonance in the converter topology, as a result of this technique the parasitic energy stored in the switch's capacitance is discharged and due to that the switch can be turned off with zero current [Mohan, 2012].

high nominal frequency and rich in harmonics the component and circuit parasitic can cause a failure of operation.

### 2.3.2.1 Air humidity and temperature from **RF** supply

A very interesting example of completely autonomous measurement system is reported in [Visser, 2012]. The wireless **RF** harvester supplies the commercially available wireless sensor node measuring temperature and humidity and transmitting measured values with interval of 45sec at frequency of 433MHz.

The power required to supply the sensor and communication unit was measured to be  $55\mu\text{W}$ . However, the input power has to be magnified by the power lost in the conversion units (e.g. in this solution the boost converter uses  $17.9\mu\text{W}$ ). Taking into account the losses formed in the harvester the input power has to be at least  $73\mu\text{W}$ . The harvester cooperates with standard frequency used by **WiFi** hotspots 2.45GHz. The packaging of **RF** generator and the sensor is showed on Fig. 2-23a, the device is compact and encapsulated in relatively small chassis which facilitates the mounting.

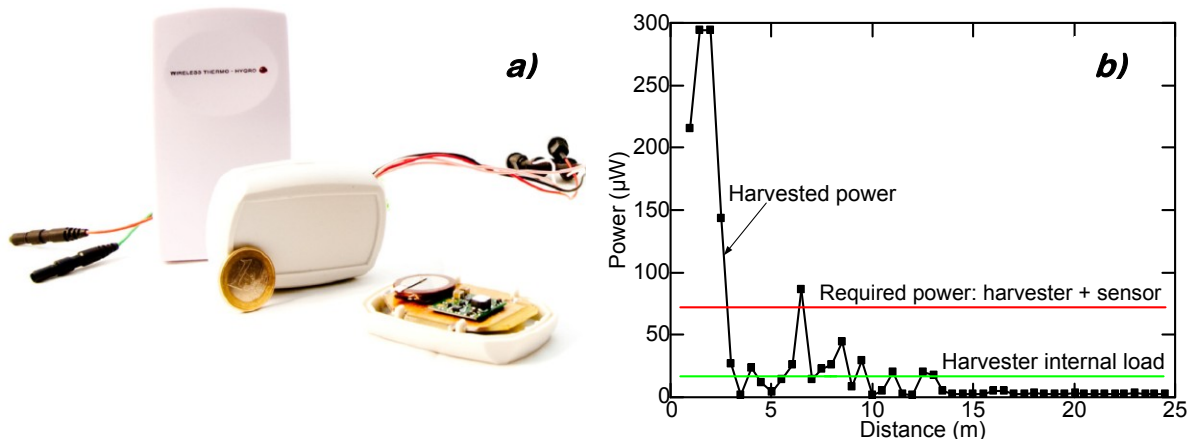


Fig. 2-23 a) Packaging of wireless sensor node measuring the temperature and humidity and communicating the values through connection at 433MHz. The sensor node is supplied by integrated 2.45GHz **RF** energy harvester, b) the harvested power versus distance from radiating source emphasizing the power requirement of the harvester and the sensor node [Visser, 2012]

Fig. 2-23b depicts the harvested power versus distance from radiating source, the red line shows the power requirement of complete system while green line presents the power lost in the harvester. When the harvester power is higher than the limit marked by the red line the system is energetically autonomous and all power requirements are covered by **RF** waves. Placing the harvester up to 5m from the radiating source will ensure scavenging sufficient power to maintain all system functional.

This example of autonomous sensor is very interesting especially in light of the rising popularity of intelligent buildings or exploding applications based on **IoT** (see 1.1.3).

### 2.3.3 Summary

**Radio Frequency** energy harvesting is quite new concept of energy production from ambient **RF** waves. This energy scavenging method stayed almost unemployed since the first application of microwave energy transport in the 1950s. With the explosion of wireless communication devices based on **GSM** or **WiFi** networks the presence and density of microwaves in the ambient air is rapidly rising. Because of the omnipresence of

dense **RF** waves especially in urban zones the **RF** energy scavenging receives regained interest. The main advantages of this harvesting method are: quiet and vibrationless operation and comfortable (*no cable connections, the placement of harvester everywhere but close enough to radiating source*) production of additional energy. However, the **RF** energy harvesters are unpopular on the market mainly due to: (i) small achievable harvested power (ii) high dependency on communication conditions (*obstacle number, air parameters*) (iii) necessity to use sophisticated converters structures able to operate at very high frequencies and (iv) sensitivity to the component and circuitry parasitics.

Despite their disadvantages, the increase of wireless communication devices is pushing forward the development of **RF** harvesters. This harvesting solution is commercialized but the number of producers is very small. Taking into consideration the quantity of research and investments, the expansion of **RF** harvesters is a matter of time.

Table 2-9 lists few examples reported in literature of **RF** energy harvesters with respect to the used frequency band, the input and output power and the distance between harvester and radiating device.

**Table 2-9 Review of Radio Frequency harvesters**

$f$ (MHz)	Network	Input Power (W)	Range (m)	Output Power <sup>†</sup> ( $\mu$ W)	Reference
902-928	GSM900	4	15	5.5	[Le, 2008]
868	GSM900	1.78	25	2.3	[Stoopman, 2013]
868	GSM900	1.78	27	2	[Stoopman, 2014]
915	RFID	3	5	189	[Greene, 2014]
915	RFID	1	4.3	134.9	[Sample, 2008]
866	RFID	3.2	4.8	39.8	[De Donno, 2013]
900 & $2.45 \times 10^3$	GSM900 & WiFi	$50 \times 10^{-3}$	1	100	[Masotti, 2013]
$2.45 \times 10^3$	WiFi	$50 \times 10^{-3}$	2	32	[Lui, 2012]
$2.45 \times 10^3$	WiFi	10	7	73	[Visser, 2012]
$2.45 \times 10^3$	WiFi	$100 \times 10^{-3}$	6	N/A	[Theeuwes, 2007]
$2 \times 10^3 \div 18 \times 10^3$		$0.25 \times 10^{-6} \div 2.5 \times 10^{-3}$	N/A	$2 \times 10^{-9} \div 450 \times 10^{-3}$	[Hagerty, 2004]

<sup>†</sup>minimal required power to make the system operational (*harvester RF-to-DC circuitry*)

Comparing the parameters of **RF** harvesters is problematic because there is no existing measurement procedure which could be adopted when characterizing the harvesters. The lack of characterization standard results in the situation that each reported harvester was measured under different conditions. However, with the help of the Table 2-9, it can be noted that the harvested power depends on the used frequency band, the **GSM900 & RFID** band is transferring higher power than **WiFi** band. Secondly, the output power is strongly affected by the distance between the source of radiation and the harvester.

To summarize this section it can be noted that the **RF** harvesting is a branch of energy scavenging under very high development. The advantages offered by this type of additional energy production are attracting a lot of researchers and industrial investors, thus numerous commercialisations of autonomous devices powered wirelessly through the microwaves are expected very soon. Moreover, the **RF** energy harvesting offers same

advantages like photovoltaic or thermoelectric (*silence, vibrationless and reliable operation*) energy scavenging and adding the liberty of harvester's mounting place within the range of operation. The improvement of **RF-to-DC** harvester circuitry to boost the efficiency, and the development of rectennas with optimised capturing efficiency will allow the **RF** harvester to explode on the market.

## 2.4 Energy from light

The photovoltaic effect was discovered by Edmond Becquerel in 1839. He wrote in the “*Les Comptes Rendus de l’Académie des Sciences*” this observation:

*“[...] the production of an electric current when two plates of platinum or gold diving in an acid, neutral, or alkaline solution are exposed in an uneven way to solar radiation.[...]”*

This effect remained without practical application for very long time, but with the development of electronics and semiconductor technology it became one of the most popular and most frequently used.

The energy provided by the light is one of the densest among all renewable energy as shown in Table 2-10. The light is omnipresent and delivers interestingly high power per surface especially in the case of a sunlight exposition. Despite modest efficiencies of solar cells the harvested power is high enough to offer energetic autonomy for the low-consumption devices e.g. calculators or wrist watches. At macro scale the photovoltaic panels can cover non-negligible part of total dwelling electricity consumption.

**Table 2-10 Power densities for different harvesting methods** [[Raghunathan, 2005](#)]

<i>Energy harvesting technology</i>	<i>Power per volume of total system (<math>\mu\text{W}/\text{cm}^2</math>)</i>
<b>Photovoltaics (outdoors, <math>\eta=15\%</math> cell, insolation <math>100\text{mW}/\text{cm}^2</math>)</b>	<b><math>15 \times 10^3</math></b>
<b>Photovoltaics (indoors, <math>\eta=6\%</math> cell, insolation <math>0.5\text{mW}/\text{cm}^2</math>)</b>	<b>30</b>
<b>Piezoelectric (heel shoe generator)</b>	<b>330</b>
<b>Vibration (small microwave oven)</b>	<b>116</b>
<b>Thermoelectric (<math>\Delta T=10^\circ\text{C}</math>)</b>	<b>40</b>
<b>Acoustic noise (100dB)</b>	<b>0.96</b>

Light represents huge natural reserves which are not enough used, only 0.021% is actually used (*Table 1-1*). Direct conversion of light into electric energy is possible using the photovoltaic effect. This significantly simplifies the converter topology and boosts the overall system efficiency due to the absence of intermediate conversions. Further advantage of those devices is the absence of moving parts making the photovoltaic generator vibrationless, silent and reliable. Moreover, the output energy parameters are convenient for further storage, thus the control and auxiliary circuits are significantly simplified. Advantages of those generators can explain the popularity of photovoltaic devices. The global trend of installed photovoltaic devices shows a rapid increase of generated power after the year of 2005 Fig. 2-24a [[Earth Policy Institute, 2010](#)]. The top three countries with the highest production in photovoltaics include China, Germany and Japan, respectively.

Current worldwide installed power in solar cells globally is around 139GW [[REN21, 2014](#)] and the record installed power growth of almost 30% was achieved in 2013. Those investments are the result of the combination of source advantages already described and module price shown in Fig. 2-24b [[Karkatsoulis, 2014](#)] and [[Fraunhofer ISE, 2014](#)]. Worth noting is the fact that the rapid increase of power produced in

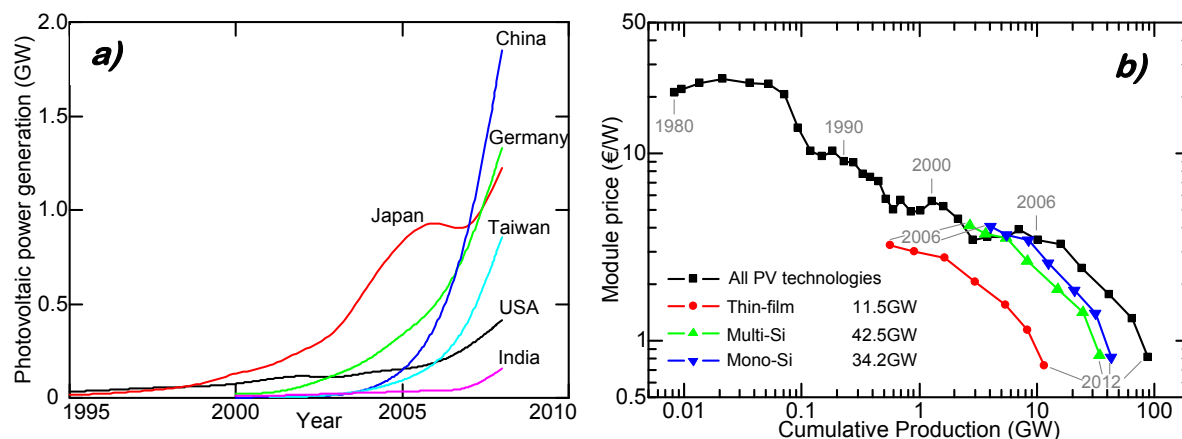


Fig. 2-24 a) The annual photovoltaic production for top six countries [Earth Policy Institute, 2010], b) Module price versus power generation for different fabrication technologies [Karkatsoulis, 2014] and [Fraunhofer ISE, 2014]

photovoltaic modules Fig. 2-24a, which can be remarked around the year 2005, matches perfectly with the arrival of new cost effective fabrication technologies Fig. 2-24b. When the explosion of photovoltaic power production occurred the module cost was about 3€/W. Fig. 2-24b depicts the price evolution since 1980. In the 80s the price of photovoltaics was dominated by expensive technology resulting in low cumulated power at that time. Development of new technologies in the first decade of  $XXI^{st}$  century resulted in (i) cost reduction and (ii) popularization of solar modules on the market which is indicated by the significant rise of generated power in photovoltaic modules. At the end of 2012 a Watt of electric energy generated from a light had a cost around 0.7€, but in the 80s this cost was almost 20€. The technology development and the governmental actions promoting the renewable sources of energy [EU, 2009] resulted in over 95% price drop since the arrival of photovoltaics on the market.

In light of those arguments it is clear that photovoltaic energy harvesting is one of the most powerful and popular renewable source of energy in the world, with global energy production of 139GW<sup>14</sup> in 2013.

This section is organized in such a way to give to a reader general perspective on the photovoltaic energy harvesting. Starting with physical basics, passing through some interesting and non-mainstream solar cell applications and finishing by summarizing few reported photovoltaic harvesters.

### 2.4.1 Basics

Conversion of light into electric energy is realized by  $pn$  junctions which are encapsulated to expose the junction to the light. Light influences the semiconductor  $pn$  junction and generates electron-hole pairs, which are forming the output current and provide the electrical power to the external load [Opolski, 2002].

Fig. 2-25a presents the band diagram for  $pn$  junction which is exposed to the light. Photon energy  $h\nu$  which arrives to the junction excites the electron-holes pairs within the depletion zone. The light energy transferred to the carriers is high enough to cause the carrier excitation to the conduction band for electrons and valence band for holes.

<sup>14</sup> This power is equivalent to electric capacity of France 132GW or Canada 135GW at the end of 2012 [EIA, 2012].

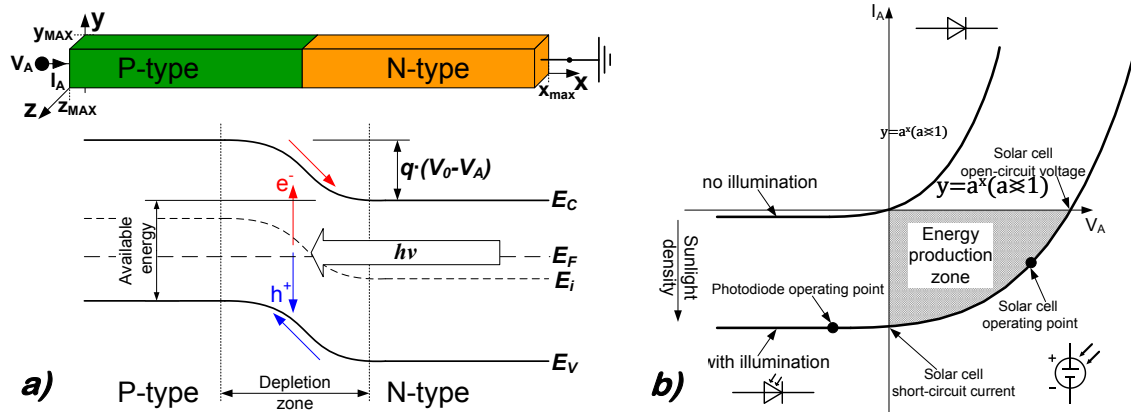


Fig. 2-25a) Band diagram for solar cell in  $pn$  junction exposed to the light [Hennel, 2003], b)  $IV$  characteristics for  $pn$  junction with and without exposure to light, distinguishing the electrical symbol for corresponding operation zones [Opolski, 2002]

Afterwards, excited carriers are separated away from depletion zone owing to the carrier drift (*electrons are flowing towards  $n$ -type semiconductors while holes are travelling to  $p$ -type*). This forms the flow of charged carriers which can be considered as photovoltaic module output current. The photovoltaic modules are fabricated in such a way to limit the carrier recombination, the passage of excited carriers from conduction/valence band to less energetic states with emission of photon. The carriers which are serving as output current have to remain in valence/conduction band without losing the energy provided by the light.

Connecting together  $p$ -type and  $n$ -type semiconductors results in creation of a built-in potential  $V_0$ . To cross this barrier the carrier has to be provided with energy higher than the barrier energy. The built in potential depends on temperature  $T$  and doping parameters such as donor ( $N_D$ ), acceptor ( $N_A$ ) and intrinsic ( $n_i$ ) concentrations Eq. 2-8 [Neamen, 2003].

$$V_0 = \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \quad \text{Eq. 2-8}$$

$$V_{tot} = V_0 + |V_A| \quad \text{Eq. 2-9}$$

$$I_A = I_0 \cdot \left( e^{\frac{q \cdot V_A}{k_B \cdot T}} - 1 \right) - I_L \quad \text{Eq. 2-10}$$

The energy barrier across  $pn$  junction can be modulated by externally applied anode voltage ( $V_A$ ). Negative  $V_A$  puts the junction into blocking state and the total potential barrier  $V_{tot}$  across the junction is magnified by  $V_A$  Eq. 2-9. In this state the carriers have to overcome a high energy barrier and the current is very low. Opposite situation occurs when  $V_A$  is positive, in this case the junction is in conducting state because the energy barrier is reduced and carriers flow between the regions.

The operating modes of  $pn$  junction are presented graphically on the  $IV$  characteristics Fig. 2-25b for a junction without illumination. The characteristics placed in 3<sup>rd</sup> quadrant shows the reverse polarization of the diode, the current is very small for negative values of  $V_A$ . Part of characteristics in the 1<sup>st</sup> quadrant shows the forward polarization,  $V_A$  and  $I_A$  are flowing through the diode, in this state the diode is in conducting state. This characteristics can be described by diode equation Eq. 2-10 for  $I_L=0$  ( $I_L$  is the illumination current).

Influence of light on the diode behaviour is depicted in Fig. 2-25b. The light energy delivered to the junction moves the characteristics towards higher reverse currents when the diode is reversely biased. Diode characteristics is shifted by the value of  $I_L$  towards higher reverse current values as described by Eq. 2-10. In other words, the reverse current  $I_A$  when  $V_A < 0$  is proportional to the density of the incident light. The exposure to the light forms a zone in 4<sup>th</sup> quadrant, which doesn't exist in the case without illumination. Within this zone  $V_A$  and  $I_A$  have opposite signs and the power is produced, the junction operates as photovoltaic cell.

Worth noting is the fact that when forward polarization is high enough, the current will become positive and in such a case the diode will act as normal diode in conduction state. When the junction operates as solar cell it is externally polarized in forward direction but the current flows in opposite direction to the applied bias [Kitai, 2011]. From this description arises second requirement for solar cells, the junctions dedicated to act as photovoltaic device should have high reverse current value when reversely polarized.

The solar cell output power can be also boosted when minimizing the barrier  $q \cdot (V_0 - V)$  this will facilitate the drift of excited carriers from depletion zone. However, if  $q \cdot (V_0 - V)$  is too small the carriers recombination is reinforced and their drift from depletion zone won't be efficient, this will reduce the output current.

Good solar cell should have as small as possible recombination rate within the depletion zone and potential barrier between  $p$ -type and  $n$ -type semiconductors. However, the reverse current should be maximized. Simultaneous fulfilment of those requirements is impossible, thus a trade-off has to be found.

Output voltage and current for single  $pn$  junction working in photovoltaic range is very small. Thus to harvest considerable power the single junctions has to be connected in series to rise-up the output voltage and in-parallel to boost the output current.

The photovoltaic devices are very popular solution to produce renewable energy on the micro-scale (e.g. *the supply for wrist watches or calculators*) and on the macro-scale (e.g. *photovoltaic cars, boats, dwellings etc.*).

## 2.4.2 Energy for watch

In this section I can't omit one of the most popular and every-day application of photovoltaics, which are the wrist watches or calculators solar cells. This solution is extending significantly the life-time of the battery and covers total energy consumption when light density is high enough. The first wrist watch powered by the light was commercialized by Seiko<sup>®</sup> in 1978 in the **LCD** alarm clock A156-5000<sup>15</sup> Fig. 2-26a. At that time the price of photovoltaic devices was very high around 20€/W (see Fig. 2-24b), thus at the beginning this solution did not received enthusiastic welcoming. With development of fabrication technologies which popularized the solar cells nowadays the market is full of small consumption electronic devices supplied from light.

Solar cells are sources of energy with almost perfect parameters adaptation for supplying devices such as watches or calculators. Firstly, the photovoltaic devices provide direct current to the output thus the cell can be coupled directly to the load (*omission of voltage adaptation unit e.g. filtering or rectification*). Secondly, devices such as calculator

<sup>15</sup> <http://www.seikodigitalwatches.com/SEIKO4.htm>



or watch are consuming low power, this makes it easier to integrate the solar cell in the device because its dimensions are not large.

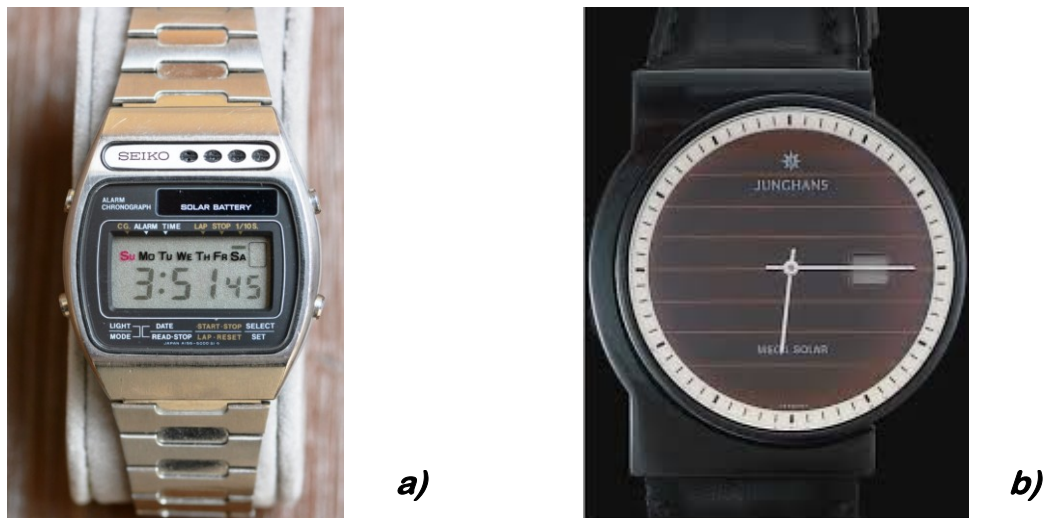


Fig. 2-26 a) First application of solar cell for powering wrist watch by Seiko<sup>®</sup> A156-5000 commercialized in 1978, b) wrist watch with photovoltaic dial-plate with possibility for radio communication on multiple frequency ranges by Junghans<sup>®</sup> Mega Solar commercialized in 2014.

Fig. 2-26 shows clearly the development of solar cells in electronics (*emphasizing the development in supplying wrist watches*). Now the watches can integrate multiple functionalities like: wireless communication, geographical localization *etc.* and all can be powered by photovoltaic device. The modern solar cells are efficient enough to cover all power requirements, however the watches are equipped with batteries to ensure the operation when light is absent.

### 2.4.3 Photovoltaics for road safety

In 2013, a total of 25 938 human beings were lost in traffic accidents [[Brandstaetter, 2012](#)] and motorbike users fatalities states for 18% of total number mortalities on the roads.

Solar energy harvesting can be used to improve safety on the roads especially for drivers who are using motorbikes. Commercialized jackets dedicated for motorbike riders are equipped in **LED** diodes which are doubling the light signals of the bike Fig. 2-27. Supplying for those **LED** diodes is provided from two sources, firstly from the motorbike battery through the electrical connection, secondly from the photovoltaic cells. To repeat same signals as the motorbike the information about the used lights has to be transferred to the jacket, thus the jacket and the bike has to be equipped with a wireless communication unit.

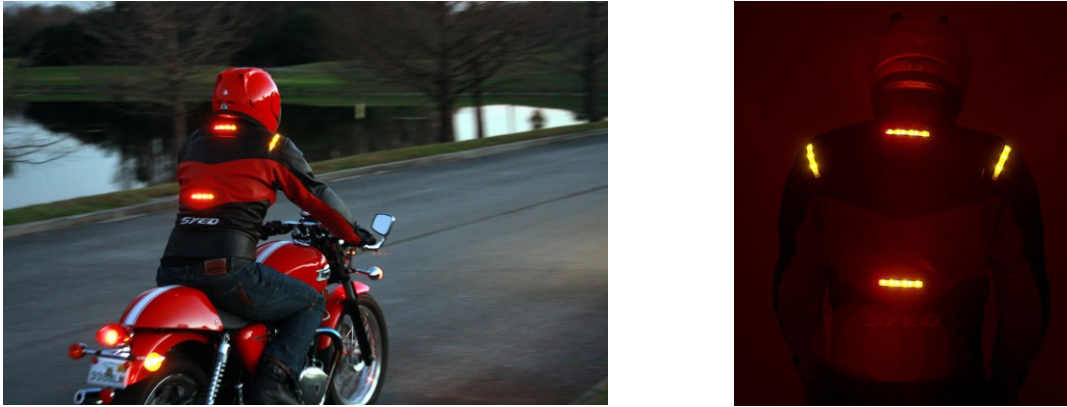


Fig. 2-27 Motorbike jacket with *LED* signalization doubling the intentions of the rider. The jacket can wirelessly communicate with the bike to determine the signalization state, powering through a battery or through solar cells are available. Commercialized by Impulse Jackets

The most interesting and innovative parameter of this solution is the integration of mechanical flexibility into the photovoltaic device. The flexibility allows the mounting on curved surfaces, enables the body movement and makes the jacket more comfortable.

#### 2.4.4 Energy for buildings

The households and offices are all equipped with artificial lighting with interesting luminous flux densities. On the market there are a lot of companies which are proposing photovoltaic devices dedicated for converting indoor light into electric energy. The energy available from the indoor and outdoor light is listed in Table 2-11.

Table 2-11 The comparison of power density available from indoor and outdoor lightning conditions [SCHOTT®, 2006]

<i>Illumination level</i> (lx)	<i>Source</i>	<i>Indoor specification cell</i> <i>Power density</i> ( $\mu\text{W}/\text{cm}^2$ )	<i>Outdoor specification cell</i> <i>Power density</i> ( $\mu\text{W}/\text{cm}^2$ )
100	Fluorescent light	2.9	N/A
200	Fluorescent light	6.1	N/A
1000	Fluorescent light	34	N/A
12500	Natural sunlight	N/A	480
125000	Natural sunlight	7100	6380

According to Table 2-11 the light energy can be harvested from both outdoor and indoor light. Solar cells dedicated to convert artificial indoor light are offering slightly higher power than same cells at the same illumination level. This is the reason of different cells design, the indoor cells are usually fabricated in crystalline-Silicon (**c-Si**) thus can convert the energy from wider spectrum of wavelengths than the solar panels design to cooperate with natural sunlight made from amorphous-Silicon (**a-Si**). This situation is graphically illustrated in Fig. 2-28.

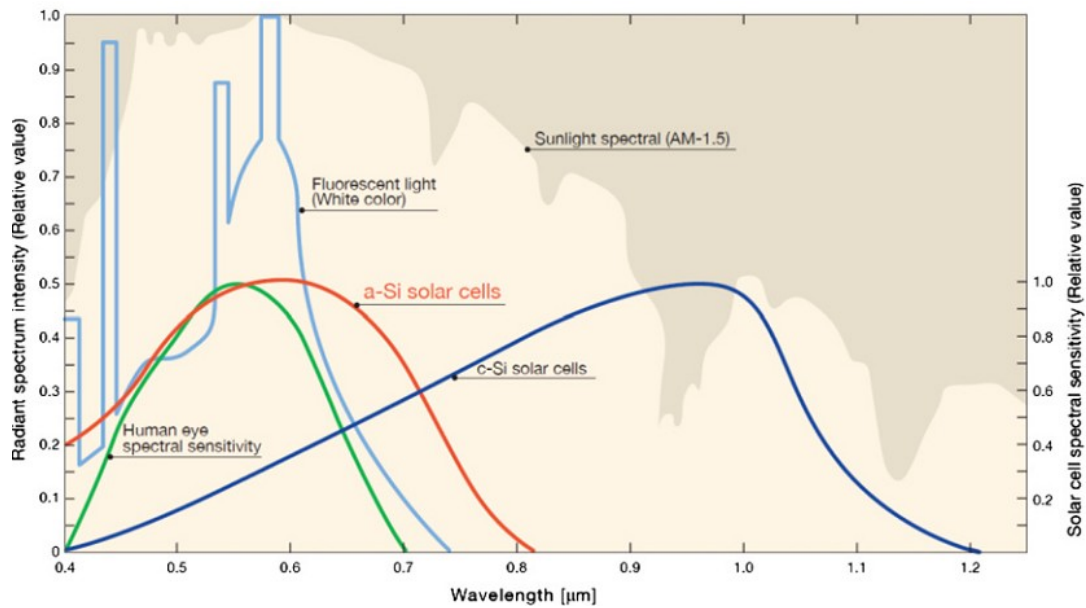


Fig. 2-28 Solar cell spectral sensitivity versus wavelength emphasizing the fabrication technology of the cell and light sources sunlight and fluorescent light

The dwelling and office lightning offer sufficient density to produce additional energy. This harvested power has been measured in different places in households and offices and it is listed in Table 2-12.

Table 2-12 Light measurements in different indoor locations measured in Southampton from 1 to 4 June 2012 and Warsaw on the 24 and 25 January 2011 [Matiko, 2014]

Location	Type	Measurement location	Illumination level (lx)	Cell output power ( $\mu\text{W}$ )	Power density ( $\mu\text{W}/\text{cm}^3$ )
Southampton	Residential	Living room	370	110	38
		Kitchen	300	87	30
		Bedroom	100	25	9
		Bathroom	110	28	10
		Living area	200	56	19
		Living area near windows	3700	1149	399
Warsaw	Office	Single office	800	244	85
		Single office near windows	2400	743	258
		Large open office	2200	681	236
		Corridor	450	134	47

Table 2-12 lists the available power in the residential and office lighting conditions. Installing solar cells in those places enables the production of electric energy with sufficient power for supplying the micro-consumption devices such as wall-clocks, sensors, etc.

### 2.4.5 Summary

Photovoltaic energy harvesting is definitely one of the most popular and developed way to produce electricity from renewable energy. Advantages of energy production from light like silence, absence of vibrations, long life-time and direct conversion are attracting investments and drives research. However, the character of photovoltaic energy harvesters makes it highly dependent on hazardous conditions especially weather and on the mounting place. As a result, the solar devices may not guarantee production of sufficient power continuously. In practice, this results in the necessity to couple photovoltaic cells with batteries making the device powered either from light or from battery depending on lighting conditions.

Various fabrication technologies available for solar panels enabled both the price reduction and parameter diversity. One of the most remarkable technological achievement is the integration of mechanical flexibility into the panels. This particularity enables numerous applications especially in textile industry with commercialization of photovoltaic clothes. In household/office light energy harvesting the investments are encouraged by the support of governmental programs which are promoting alternative sources of energy. In industrial environment the photovoltaic devices states for simplification of installation enabling remote supply. The progress observed in photovoltaic devices is remarkable in each life and industry domain, this explains why this group of harvesters is the largest and the most popular so far. Moreover, photovoltaic devices are applicable in the ranges of output power from micro- to macro- scale. This particularity enables the realization of photovoltaic power plants *e.g.* Arizona power plant with annual production of 3101 GW·h in 2014<sup>16</sup>. Using the same phenomena devices such as wrist watch solar batteries with nominal output power of few hundreds  $\mu\text{W}$  can be fabricated.

Making an exhaustive review of photovoltaic devices is a difficult task because in order to give representative image of state-of-the-art the risk of omission is very high. However, in Table 2-13 the list of few most interesting and innovative application is presented emphasizing on the fabrication technology. The measurement conditions for all devices listed in Table 2-13 are identical. Manufacturers are characterizing their devices using **Standard Test Conditions (STC)** imposed by **International Electrotechnical Commission (IEC)**. According to standards [[IEC 61215, 2005](#)] and [[IEC 61646, 2008](#)] all **c-Si** and thin-film photovoltaic devices have to be characterized under **STC** protocol. **STC** requires the use of sunlight with illumination of  $1000\text{W}/\text{m}^2$  ( $\sim 115\,000\text{ lx}$ ); with solar spectrum AM 1.5 which represents the sun energy provided during clear sky when sun is at  $41.8^\circ$  and ambient temperature of  $25^\circ\text{C}$  [[Labouret, 2010](#)]. This test standard allows comparing different solar panels at same working conditions and simulates the average working conditions for photovoltaic devices transforming energy from the sun.

<sup>16</sup> Data based on monthly report provided by US Energy Information Agency <http://www.eia.gov/electricity/monthly/> for December 2014 accessed on the 15<sup>th</sup> of February 2015

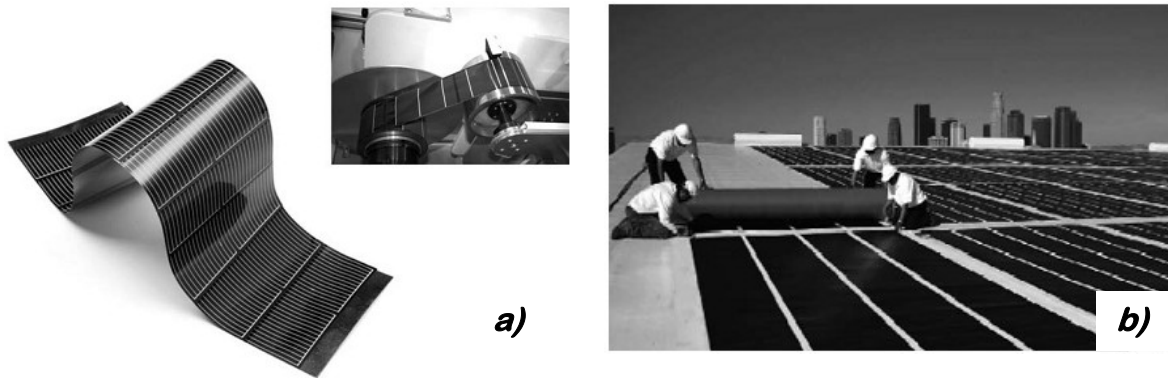
Table 2-13 Summary of photovoltaic devices, characterized under standard test conditions (STC).

Efficiency (%)	Surface (cm $\times$ cm)	$P_{MAX}$ (W)	Power density (mW/cm $^2$ )	Type	Manufacturer	Tech.
7	96 $\times$ 99	67	7.05	a-Si <sup>a)</sup> single junction	Kaneka	Thin-Film
6.2 $\div$ 6.5	110.8 $\times$ 130.8	90 $\div$ 95	6.21 $\div$ 6.55	a-Si <sup>a)</sup> single junction	Schott Solar	
5.5 $\div$ 6.5	110 $\times$ 130	79 $\div$ 94	5.52 $\div$ 6.57	a-Si <sup>a)</sup> single junction	Invectux	
7.3 $\div$ 9	110 $\times$ 130	105 $\div$ 130	7.34 $\div$ 9.09	Micromorph <sup>b)</sup> Si	Invectux	
7.9	100 $\times$ 160	127	7.5	a-Si <sup>a)</sup> double junction	XsunX	
8.5	112.9 $\times$ 93.4	90	8.53	Micromorph <sup>b)</sup> Si	Sharp	
6 $\div$ 7.2	125.8 $\times$ 65.8	50 $\div$ 60	6 $\div$ 7.25	CuInSe $_2$	Sulfur Cell	
7.9 $\div$ 9	120 $\times$ 60	55 $\div$ 65	7.63 $\div$ 9.03	CdTe	First Solar	
7.9	100 $\times$ 160	127	7.5	a-Si <sup>a)</sup> double junction	XsunX	
8.5	112.9 $\times$ 93.4	90	8.53	Micromorph <sup>b)</sup> Si	Sharp	
6 $\div$ 7.2	125.8 $\times$ 65.8	50 $\div$ 60	6 $\div$ 7.25	CuInSe $_2$	Sulfur Cell	
7.9 $\div$ 9	120 $\times$ 60	55 $\div$ 65	7.63 $\div$ 9.03	CdTe	First Solar	
13 $\div$ 14.1	131.8 $\times$ 99.4	170 $\div$ 185	12.97 $\div$ 14.12	Mono-Si	Sharp	Crystalline Silicon
12.9 $\div$ 14.5	158 $\times$ 80.8	165 $\div$ 185	12.92 $\div$ 14.49	Mono-Si	Suntech	
19.3	155.9 $\times$ 104.6	315	19.32	Mono-Si back contact	Sunpower	
14.1	150 $\times$ 99	210	14.14	Poly-Si	Kyocera	
13 $\div$ 14.7	148 $\times$ 99	190 $\div$ 215	12.96 $\div$ 14.67	Poly-Si	Heckert Solar	
12.6	574.5 $\times$ 49.4	300	10.57	CdS+Cu(In,Ga)Se $_2$ on plastic	Global Solar	Flexible
4	66.4 $\times$ 218.5	60	4.14	a-Si <sup>a)</sup> on plastic	Power Film	
3.5	27 $\times$ 32.5	3.08	3.51	a-Si <sup>a)</sup> on plastic	Flexsolarcells	

<sup>a)</sup>a-Si – amorphous Silicon

<sup>b)</sup>Micromorph Si – this is the mix of amorphous and microcrystalline Silicon

Table 2-13 shows only a few of solar cells available on the market. However, when comparing different fabrication technologies it can be concluded that the efficiency of the module depends on the technology. Thin-film and flexible cells are presenting the lowest efficiencies while **c-Si** technology is the most efficient. Efficiency of crystalline materials is due to their good electrical properties. Amorphous materials have significantly lower carrier's mobilities due to structural defects, this makes them less conductive electrically. Worth noting is the increasing number of flexible cells and their variety. The material used by Global Solar<sup>®</sup> exhibits the most interesting efficiency, and the fabrication technology is equally innovative. The solar cells are fabricated using "roll-to-roll" technology which allows the production of the devices in the rolls like paper Fig. 2-29a.



**Fig. 2-29** a) Flexible solar cell fabricated in “roll-to-roll” technology by Global Solar; b) Flexible solar panels installation on the roof [\[Labouret, 2010\]](#)

Mechanical flexibility significantly simplifies the installation of the solar cells, *e.g.* solar panel can be just unrolled and glued to the roof surface Fig. 2-29b.

To conclude this section it has to be underlined that the energy production from the light is definitely the largest and the most commercialized harvesting method. Devices with the power rates from micro- to giga-watts can be supplied by photovoltaic devices. Moreover, the significant advantages like silent, vibrationless and reliable work are also gathering a lot of enthusiasts. For several years solar devices were so expensive that this solution remained unattractive but with the adoption of promoting laws *e.g.* renewable energy law (*feed-in tariff*) the price has significantly decreased. Moreover, efforts in the development of photovoltaic devices resulted in the apparition of multiple fabrication technologies. The modern solar cells are presenting low production costs, adjustable dimensionality and can be mechanically flexible, this will surely cause the further expansion of photovoltaics on the market.

## 2.5 Energy from heat

At last but not at least, this section will be dedicated to electricity production from heat sources. In the following section the history, theory and state-of-the-art of thermoelectricity will be presented.

### 2.5.1 History and future

#### 2.5.1.1 Discovery and early stage development

The beginning of this conversion arises from discovery of the thermoelectric effect which was discovered in 1823 by Estonian-German researcher Thomas Johann Seebeck Fig. 2-30a [Velmre, 2010]. Thus, in the literature, this effect is also called the Seebeck effect. Thomas Seebeck investigated also the photoelasticity of the glass [Aben, 2007] and is a father of colour photography owing to his description how light interacts with silver chlorine (**AgCl**) [Chisholm, 1911]. He recorded the solar spectrum in 1810 in the solution of **AgCl** well before the first colour picture [Eder, 1978].

Demonstration of the thermoelectric effect was observed by the deflection of a magnetic needle when one end of the bismuth-copper (**Bi-Cu**) thermocouple placed under the needle was heated Fig. 2-30b. This demonstration showed that there has to be thermally-built electrical potential in the **Bi-Cu** thermocouple which interacts with magnetic field of the needle resulting in the deflection. Seebeck observed that the deflection angle of the magnetic needle depends on the temperature difference across the thermocouple and its composition. He noted also that to observe a deflection dissimilar metals have to be used in the thermocouple.

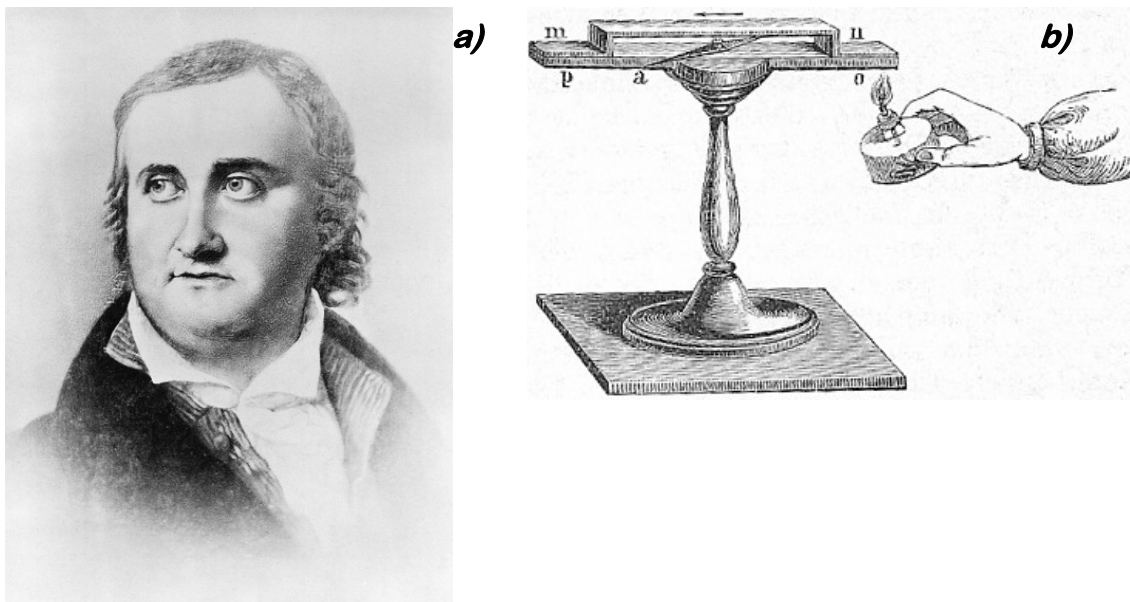


Fig. 2-30 a) Thomas Johann Seebeck (1770-1831), b) Historical instrument from 1840s called "Seebeck's rectangle" for demonstration of thermoelectric effect *op* – strip made from bismuth Bi; *nm* – metallic rod made from copper Cu; *a* – magnetic needle

At the beginning, Seebeck was convinced that had discovered new thermally excited type of magnetic interaction, thus he called his discovery *thermomagnetism* [Seebeck, 1826]. Further studies showed the electric nature of the phenomena and this is why nowadays this discovery is known as thermoelectric effect.

One of the most spectacular and famous employment of thermoelectric effect on its early stage was its use as stable source of voltage in Ohm's experiments. At that time the batteries were instable which was the reason of large incertitude on electrical resistance measurements made by Ohm. The improvement of the measurement accuracy was achieved by the use of thermoelectric effect as a stable voltage source Fig. 2-31a [Ohm, 1825].

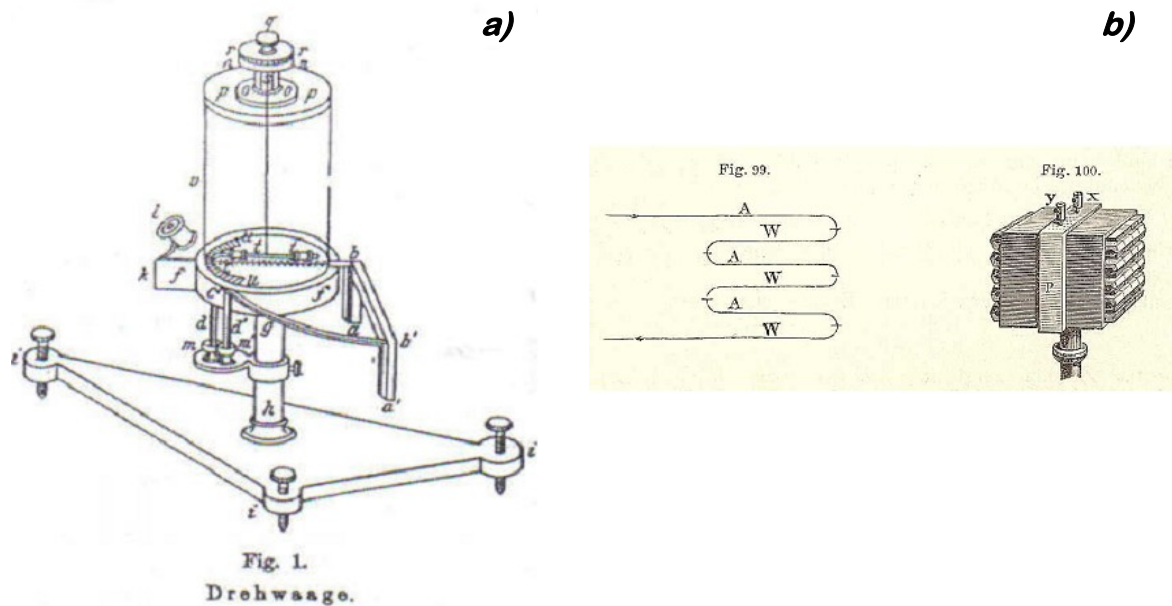


Fig. 2-31 a) Device designed by Ohm for measurement of electrical resistance with the use of thermoelectric effect as precise and stable source of electric voltage [Ohm, 1825], b) first thermopile ever used for temperature measurements, constructed by J. Fourier and H. Oersted in 1823

Preparing my thesis in France I can not omit French participation in early stage thermoelectricity developments. French scientist J. Fourier together with H. Oersted built in the 1823 the first thermopile Fig. 2-31b. This device was dedicated to precise temperature measurements, and was composed of six antimony/bismuth thermocouples connected in series [Finn, 1980].

### 2.5.1.2 Popularization and industrial expansion

However, the thermoelectric effect remained for long time a phenomenon without significant practical use. This situation changed when humanity started to control the radioactive decay. This reaction is used as source of high temperature and the heat is than transformed into electricity. Such a device is called **Radioisotope Thermoelectric Generator (RTG)** and is the earliest commercialized application of the Seebeck effect. The **RTGs** are used as power supply in sophisticated devices where the energy source cannot be replaced frequently. The first **RTG** were installed in the 1950s in Russia as a supply of offshore lighthouses or navigation stations, until now there are at least 1000 **RTGs** still operational in Russia [Alimov, 2005].

In 1960s USA lunched the first space mission powered by a **RTG**, since then a lot of spacecrafts were supplied through the thermoelectric effect including missions Pioneer 10



and Pioneer 11 Fig. 2-32a in 1964 and Voyager 1 and Voyager 2 in 1977 or famous mission Apollo 13 in 1970. Thermoelectricity still plays a very important role in space conquest since recent robot vehicle “Curiosity”<sup>17</sup> Fig. 2-32b is powered by **RTG**. Space exploration is the flagship application of thermoelectricity.

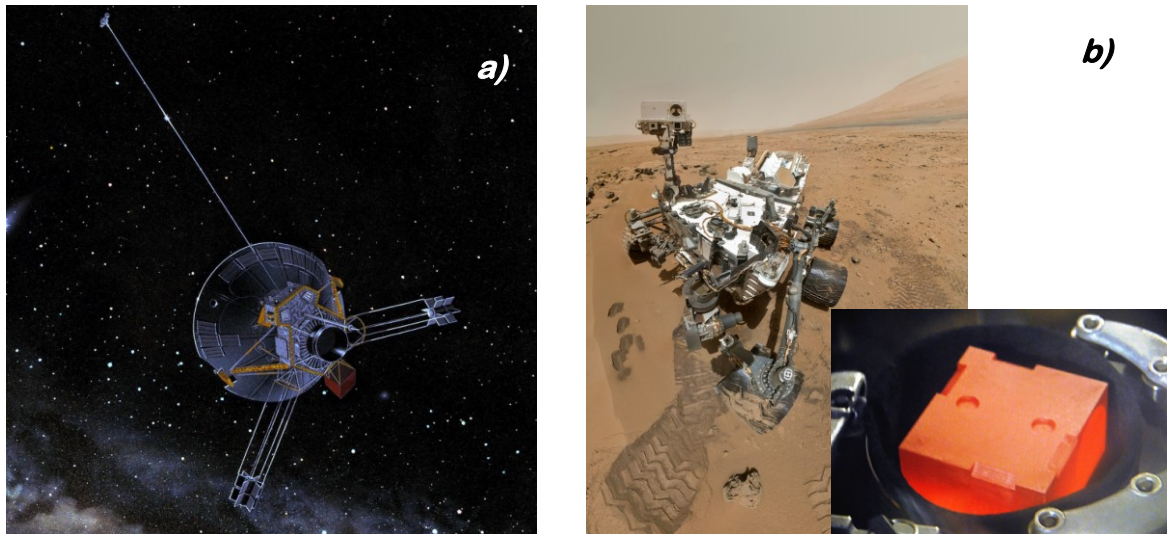


Fig. 2-32 a) Pioneer 10 & 11 the first spacecraft mission equipped with **RTG** launched in 1972 and 1973 respectively, b) Curiosity “selfie” from Mars the most recent application of thermoelectric power supply in space mission launched on November 26, 2012. Inset picture presents the polonium-238 placed in the graphite crucible the heat source of installed **RTG**.

In “Curiosity” the **RTG** is showed on the inset in Fig. 2-32b, the heat produced in the generator is obtained by decay reaction of polonium-238 dioxide. The 4.8kg of polonium-238 is capable of delivering enough heat to produce 2.5kW·h of electrical energy daily with continuous power of 100W (photovoltaic generator can produce on the surface of the Mars 0.58kW·h daily). The life-time of this **RTG** is estimated for 14 years and it can work continuously regardless the weather conditions and the presence of light [Misra, 2006].

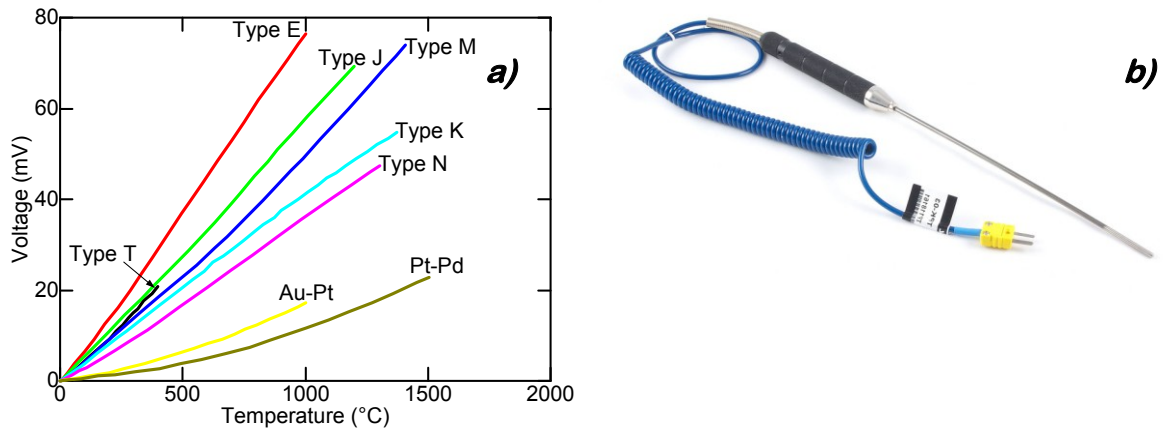
For a very long time, thermoelectric effect was used in very complicated and sophisticated applications. It remained unused in ordinary life or even unavailable on the market for a long time since its discovery. Early stage demonstration of the Seebeck effect showed two main application fields. Firstly, the thermoelectric effect can be used as a thermally controlled voltage source exhibiting high stability, purity (*lack of harmonics*) and short response time, as used in an experiment proposed by Ohm. Secondly, it can be used for temperature measurements. When applying the temperature to the thermocouple the thermally-built voltage is proportional to temperature. This second application family enabled popularization on the civil market.

### 2.5.1.3 Thermoelectricity in the future

Thermocouples dedicated to temperature measurement are available on the market since last 60 years. Nowadays this type of temperature measurement largely dominates the market and it is the main application of the thermoelectric effect. The big advantage of this type of measurement is that it does not require a voltage supply. Moreover, the

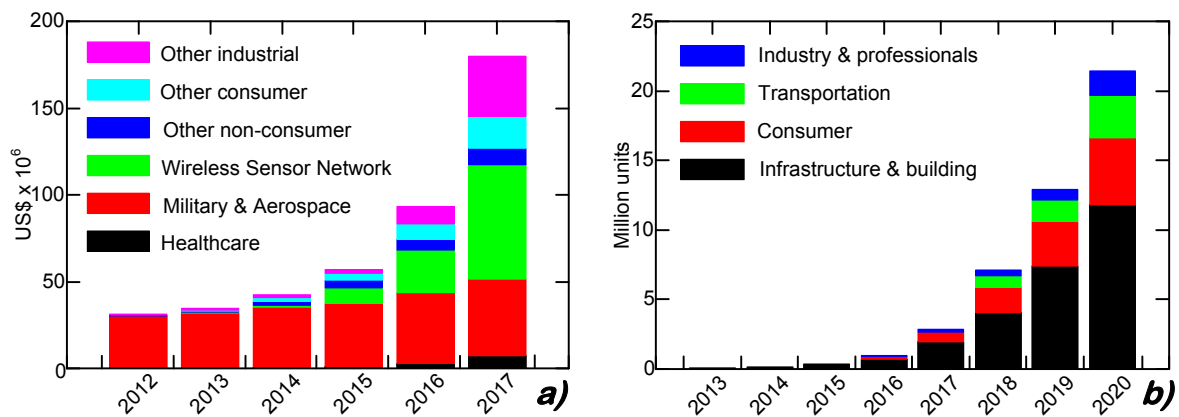
<sup>17</sup> Curiosity – the most advanced and expensive robot vehicle which is exploring Mars surface since the 6<sup>th</sup> of August 2012. It is powered by the solar cells and for emergency supply the RTG is installed. Equipped with the most sophisticated devices such as cameras, communication systems and especially innovative propulsion system. The total weight is 900kg, the cost 2.5 billion \$. Data from NASA Jet Propulsion Laboratory <http://www.jpl.nasa.gov/missions/mars-science-laboratory-curiosity-rover-msl/> accessed on the 2015-09-17

temperature difference converted to voltage through the Seebeck effect can be measured with high precision. Thermocouple should be fabricated in such a way to ensure the linear dependence of the voltage over temperature. On the market there are a lot of different types of thermocouples with specific voltage-temperature characteristics and regarding this relation the most linear behaviour over measured range of temperature should be chosen. Since the first use of thermoelectric effect to measure temperature by J. Fourier many different types of thermocouples were developed Fig. 2-33a presents the voltage-temperature characteristics for different thermocouples types.



**Fig. 2-33 a) Voltage-temperature characteristics for different thermocouples types, b) practical realization of commercially available thermocouple type K 3108-1 - TPK-03 temperature range from  $-50^{\circ}\text{C}$  to  $+700^{\circ}\text{C}$  with tolerance of  $\pm 0.75^{\circ}\text{C}$**

This brief historical review of the thermoelectric effect will be concluded with forecasts for thermoelectricity. As an indication of the industrial branch “health” is the amount of investments and the evolution of financial investments. The market forecast for thermoelectric generators is depicted in Fig. 2-34a [Happich, 2014].



**Fig. 2-34 a) Market forecast for thermoelectric generators industry, b) Quantity of sub-watt thermoelectric generators sold in various branches**

Market expansion of thermoelectric generators are rather optimistic, in 2012 the thermoelectric generators market had around 30M\$ of turnover, with market extremely focused on the military and aerospace branch. In 2017 the financial turnover in thermoelectric generators will be over five times bigger. Moreover, the composition of the main consumers will also change. The most important consumer for thermoelectric generators will be the industry of wireless sensors. Considering that from 2012 to 2017 the thermoelectric market will be multiplied by five allows to conclude that thermoelectricity is one of the most rapidly growing branch of alternative power sources. This conclusion is confirmed by Fig. 2-34b where the market forecast for sub-watt thermoelectric generators

is presented emphasizing the application branch. The figure is scaled in the quantity of devices previewed to be used in respective branch. Worth noting is the fact that the most important outlet for those type of harvesters will be infrastructure and buildings. This correlates with the conclusion raised from Fig. 2-34a, knowing the concept of intelligent building and internet of things described previously in section 1.1.3. Both illustrations in Fig. 2-34 are giving very optimistic perspective for development of thermoelectric harvesting on the market. Energy scavenging from heat is very attractive because at least half of the heat produced globally is lost (*see section 1.1.3.2*). Possibility to transform waste heat into useful energy is a very important and interesting. The importance of this conversion is confirmed by (i) the quantity of lost heat, (ii) the necessity to find new alternative sources of energy and urged (iii) by developing climate warming caused by the emission of gasses responsible for greenhouse effect. Moreover, the thermoelectric energy harvesting produces electric energy with very convenient specification (*stable, constant, without harmonics*), which fits perfectly with the needs of numerous devices.

Regarding the history of thermoelectricity it can be noted that from magnetic needle deflection in 1823 observed by T. Seebeck to the space vehicle “Curiosity”, thermoelectricity has enormously changed. For very long time the use of this phenomena stayed inaccessible in ordinary-life situations but since the last decade a massive popularization and commercialization of thermoelectric devices is observed.

In the following section the focus will be put on physics and basics of thermoelectric effect to better understand the rising popularity of such devices.

## 2.5.2 Theoretical background of thermoelectric effect

This section is dedicated to explain the physical background of the Seebeck effect. The main advantages and challenges of this conversion will be highlighted with putting special accentuation on the **CMOS** compatible material in thermoelectricity.

The effect discovered by T. Seebeck in 1823 relies on the formation of thermally induced electric potential difference. The value of the voltage is proportional to the temperature difference across the material and depends on the material parameters.

But why the temperature difference causes the voltage formation?

To give an answer to this question we have to look on the material as the gathering of the charged carriers. Those carriers can be positively or negatively charged and they are called holes ( $h^+$ ) or electrons ( $e^-$ ), respectively. When considering the material without temperature and voltage difference across it as shown in Fig. 2-35a, the distribution of the carriers is uniform<sup>18</sup>, and the material remains in electrical neutrality, this situation is presented in Fig. 2-35b [[Sze, 2007](#)].

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<sup>18</sup> The carriers distribution is uniform when the doping concentration is equal for each position in the material.

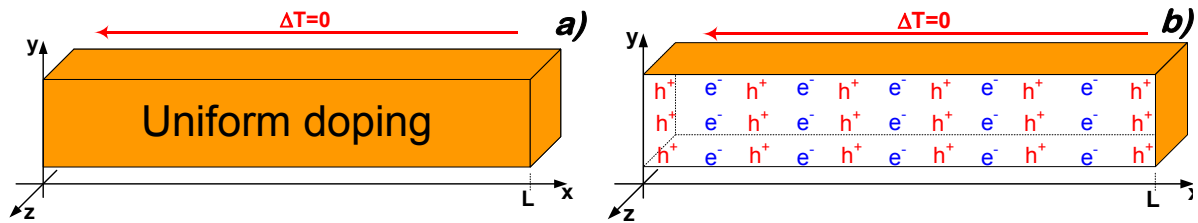


Fig. 2-35a) Thermally and electrically unbiased rod with length  $L$ , uniform doping, b) inner electron and hole distribution in thermally and electrically unbiased material

However, the charged carriers are always in motion, they are vibrating, entering in collisions and exchanging energy. When the material is not electrically biased and/or when the quantity of charged carriers is too small the movement of the carriers is random, unorganized with no privileged direction. Thus we can say that the overall electrical material charge is neutral in average.

The above described situation changes when the material is exposed to a temperature gradient. The temperature represents the average kinetic energy of the carriers, thus the carriers in higher temperatures regions are posses higher energy. This higher energy is manifested in larger carrier vibrations amplitude at the hot site. Because of higher energy and larger vibration amplitude the carriers from hotter site are migrating towards colder region of the material. But the temperature difference is not sufficient condition for creation of voltage difference through the Seebeck effect. If the density of positively and negatively charged carriers is equal the thermally induced carrier migration will not create the difference of potential. To observe the voltage difference across the material when applying the temperature gradient across it, one type of carriers has to be dominant (e.g.  $h^+$  has to be much more numerous than  $e^-$  or in the contrary, the quantity of  $e^-$  has to be higher than  $h^+$ ) the dominant carrier is called majority carrier. Appearance of those two conditions will create the voltage difference when the material is exposed to the temperature difference. Both situations for dominant  $h^+$  or  $e^-$  are presented in Fig. 2-36 [Grundmann, 2010].

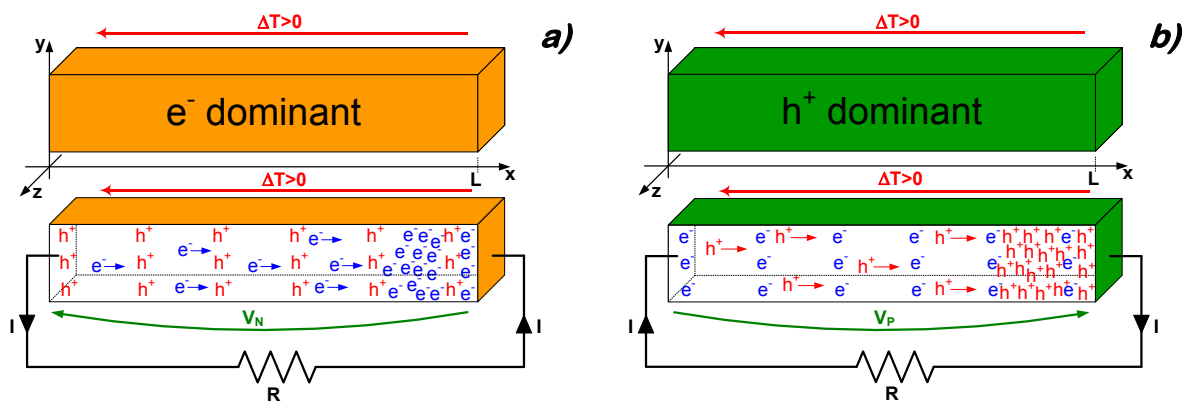


Fig. 2-36 Thermally induced charged carriers migration in material with a) electrons ( $e^-$ ) dominated transport; b) holes ( $h^+$ ) dominated transport

Important to note is the fact that depending on the majority carriers character the thermally induced voltage has opposite sense for same temperature gradient direction. This particularity results in opposite sign of the Seebeck coefficients for the  $n$ - and  $p$ -type semiconductors and is very important from a practical point of view, as will be explained more clearly later on.

At steady state the temperature difference across the material is resulting in the carrier migration towards the colder zone of the material. This unequal carrier density along the

temperature gradient forms the difference of electrical potential  $V_N$  or  $V_P$  (Fig. 2-36). The thermally built voltage can be calculated following:

$$V_N = - \int_{T_{COLD}}^{T_{HOT}} S_n(T) dT \quad \text{Eq. 2-11}$$

$$V_P = - \int_{T_{COLD}}^{T_{HOT}} S_p(T) dT \quad \text{Eq. 2-12}$$

Eq. 2-11 and Eq. 2-12 show perfectly the dual condition character of the Seebeck effect. Both  $V_N$  and  $V_P$  voltages are depending on the temperature and material parameter presented by the Seebeck coefficient (also called the thermopower)  $S_n$  (V/K) for material with dominant electrons concentration and  $S_p$  (V/K) with dominant holes concentration. Formation of  $V_N$  and  $V_P$  due to the application of temperature difference along the material is displacing the  $I$ - $V$  characteristics of semiconducting rods Fig. 2-37:

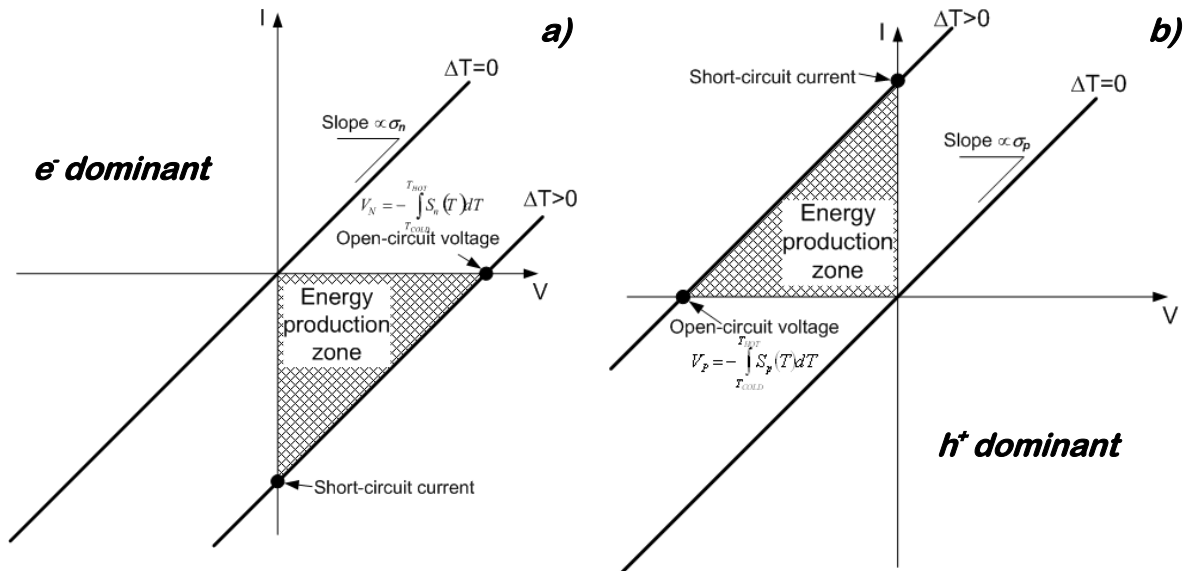


Fig. 2-37  $I$ - $V$  characteristics for semiconductor with applied temperature gradient along the rod a) rod with dominant electron concentration b) rod with dominant hole concentration

According to Fig. 2-37 it is clear to remark the presence of the zone where the product  $I \cdot V < 0$ . Within those zones the current and voltage has opposite signs and the rod is delivering power to the external load. The  $I$ - $V$  characteristics depicted in Fig. 2-37 are showing comparable device behaviour to photovoltaics Fig. 2-25b. Heat for thermoelectric devices has the same role as light in solar cells. Worth noting is the fact that for thermoelectric generators without  $pn$  junction the  $I$ - $V$  characteristics is linear. The intersection points are imposed by two material parameters. Calculating the integral in the Eq. 2-11 or Eq. 2-12 helps to find the open-circuit voltage for given  $T_{HOT}$ ,  $T_{COLD}$  and thermopower, this gives the intersection point with voltage's axis. The second intersection point is imposed by the slope of the characteristics which depends on the electrical conductivity  $\sigma_n$  or  $\sigma_p$  for  $e^-$  dominant or  $h^+$  dominant case, respectively.

Increasing the energy production zone depicted in Fig. 2-37 can be achieved in both ways. Firstly, for given material the energy production zone will be enlarged when it is imposed to higher temperature difference. However, the adoption of such solution is usually not possible in practice due to imposed temperature difference value. Secondly, the

material parameters can be optimised enabling the enlargement of the zone. From Fig. 2-37 it can be concluded that the energy production zone will be larger for materials with high short-circuit current thus the materials exhibiting the high values of  $\sigma_n$  or  $\sigma_p$  will be privileged. Secondly, to enlarge the energy production zone the open-circuit voltage should be increased, this requires materials with high thermopower values  $S_n$  or  $S_p$ . This explanation leads to conclusion that in thermoelectric effect the material plays the crucial part. In the following the special emphasize will be put on the material properties boosting the thermoelectric performance.

### 2.5.2.1 Material challenges in thermoelectric harvesting

Thermoelectric energy harvesting requires the materials which are integrating three antagonistic parameters. Firstly, good thermoelectric material should have high crystal-like electrical conductivity  $\sigma$  (1/ $\Omega$ /m). Secondly, it should manifest a low glass-like thermal conductivity  $\kappa$  (W/m/K) ( $\kappa$  is the sum of a lattice  $\kappa_l$  and an electrical  $\kappa_{el}$  components). Thirdly, it should have as high as possible Seebeck coefficient  $S_n$  or  $S_p$  (V/K) [Slack, 1995]. Material thermoelectric performance is compared using the non-dimensional-figure-of-merit ( $zT$ ) [Rowe, 1978]:

$$zT = \frac{\sigma \cdot S^2}{\kappa} \cdot T = \frac{\sigma \cdot S^2}{\kappa_{el} + \kappa_l} \cdot T \quad \text{Eq. 2-13}$$

Eq. 2-13 defines the non-dimensional-figure-of-merit for thermoelectric material. It has to be underlined that  $zT$  is proportional to the material parameters related to  $\sigma$  describing the quality of electronic transport and  $S_n$  or  $S_p$  are defining the ability to produce electric voltage from applied heat. In the same time  $zT$  is inversely proportional to the quantity which defines the quality of thermal transport  $\kappa$ .  $zT$  value as a function of temperature is depicted in Fig. 2-38a for different materials. For majority of materials,  $zT$  present a bell-shaped curve. Such a shape of  $zT$  over temperature is caused by the antagonistic dependence of  $\sigma$ ,  $\kappa$  and  $S$  on temperature.  $zT$  is very important in thermoelectricity because the maximal generator efficiency  $\eta$  only depends on  $zT$  and the cold and hot temperatures across the harvester Eq. 2-14 [Min, 2007]:

$$\eta = \frac{P_{el}}{|Q|} = \left(1 - \frac{T_{COLD}}{T_{HOT}}\right) \cdot \frac{\sqrt{1+zT} - 1}{\sqrt{1+zT} + \frac{T_{COLD}}{T_{HOT}}} \quad \text{Eq. 2-14}$$

$$\eta_{Carnot} = 1 - \frac{T_{COLD}}{T_{HOT}} \quad \text{Eq. 2-15}$$

Eq. 2-14 presents the theoretical conversion efficiency of thermoelectric generator. The most general definition of the efficiency is the ratio between the input heat flux  $Q$  and the output electric power density  $P_{el}$ . This relation can be expanded to the more detailed form which depends on the temperature and  $zT$ . In Eq. 2-14 the Carnot efficiency (Eq. 2-15) is multiplied by the material dependent component. The thermoelectric conversion as every thermodynamic process is subject to the Carnot limit [Invernizzi, 2013].

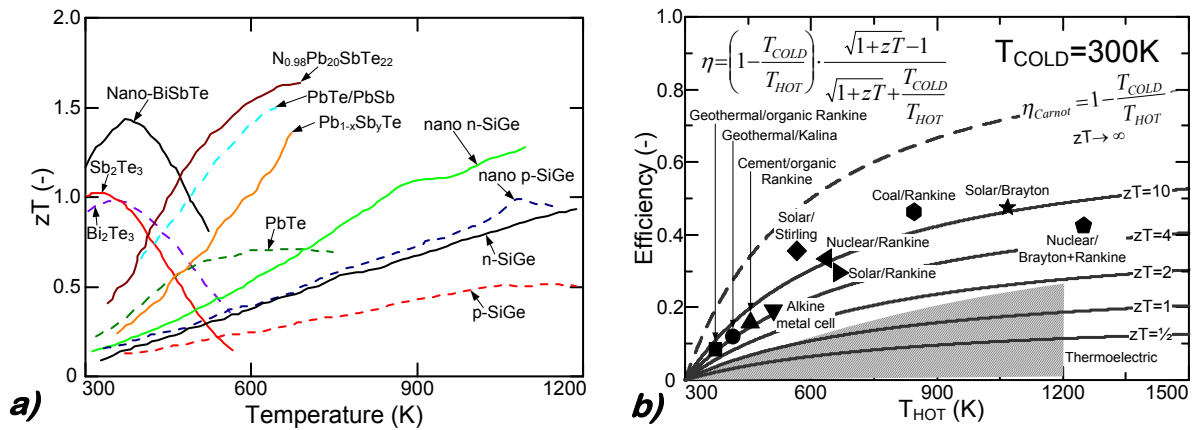


Fig. 2-38a) Dimensionless-figure-of-merit for chosen materials versus temperature [Carmo, 2010], [Minnich, 2009] and [Snyder, 2008], b) The conversion efficiency for different  $zT$  values versus temperature; dots are pointing the common efficiency for conventional energy conversion engines working using different energy cycles the marked zone corresponds to attainable currently thermogenerator's efficiencies [Vining, 2009] and [Volz, 2009]

Fig. 2-38b shows the conversion efficiency as a function of hot temperature for different  $zT$  values,  $\eta$  is calculated using Eq. 2-14. The highlighted zone corresponds to the attainable efficiencies in the state-of-the-art thermoelectricity. To benchmark the markers are pointing the common efficiency of widely known thermodynamic conversions types.

The Seebeck effect occurs in all materials: metals, insulators and semiconductors. However, for some among them this effect is so small that it is impossible to observe it. In electrical insulators the Seebeck effect is extremely strong due to their high value of  $S$ , on the other hand metals have extremely poor thermopower and thus the thermoelectric effect is very difficult to observe.

As already explained, thermoelectric energy harvesting couples three material properties describing heat ( $\kappa$ ) and current ( $\sigma$ ) conductions and the Seebeck effect ( $S$ ). To increase the harvester efficiency  $\eta$  Eq. 2-14 the  $zT$  Eq. 2-13 value should be as high as possible. To maximize value of the  $zT$  Eq. 2-13 a compromise between insulators with high  $S$  and metals with high  $\sigma$  and  $\kappa$  has to be done. The solution is to use the semiconductors with poorer thermopower and electrical properties. But putting all together in Eq. 2-13 results in the optimal  $zT$  value. Fig. 2-39 shows the  $S$ ,  $\kappa$  and  $\sigma$  over wide range of carrier concentration including different material types. It is presented that the maximal value of  $zT$  is achieved when using semiconductors with carrier density around  $10^{19} \text{ cm}^{-3}$  [Gardner, 1994].

Fig. 2-39 surprisingly shows that high Seebeck coefficient or electrical conductivity is not enough to achieve good performance in thermoelectric harvesting. Good thermoelectric material should assemble as high as possible thermopower and electrical conductivity simultaneously maintaining as low as possible thermal conductivity. In other words good material for thermoelectric energy harvesting should behave as crystal for electron transport and as glass for heat transport, shortly phonon glass/electron crystal (PGEC) [Slack, 1995]. The concept of those materials will be explained in more detailed way in the following. Studying the Fig. 2-39 leads to the conclusion that finding materials which are good electric conductors (high  $\sigma$ ) with strong thermopower (high  $S$ ) and good heat insulators (low  $\kappa$ ) is a very difficult task since those material parameters present antagonistic behaviours.

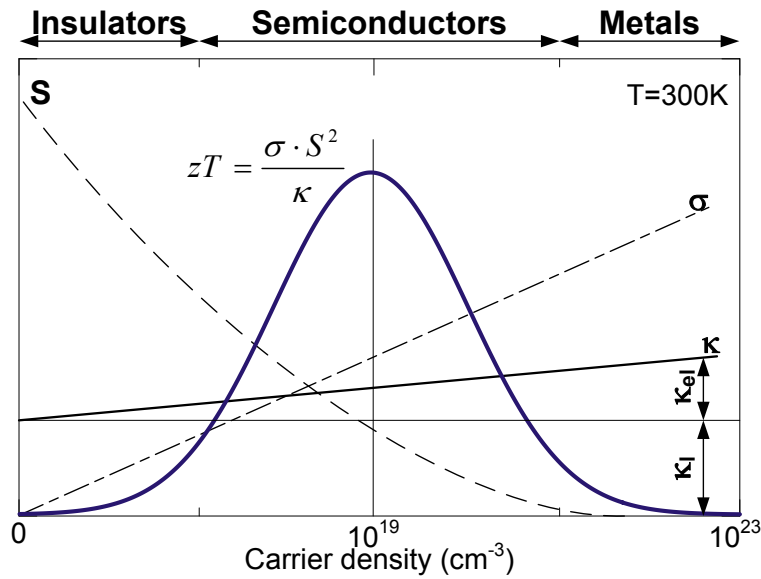


Fig. 2-39 Thermopower ( $S$ ), electrical conductivity ( $\sigma$ ) and thermal conductivity ( $\kappa$ ) versus carrier density [Gardner, 1994].

Dual character of thermoelectric effect requires controlling, tuning and adapting heat and electric transport properties. To achieve good crystal-like electronic transport and low glass-like or amorphous-like heat transport, the way how the electric current and heat are propagating through material has to be identified.

#### 2.5.2.1.1 Electric transport

Electric current is flowing in the material through charged carriers denoted as  $e^-$  and  $h^+$  for electrons and holes, respectively. To participate in electronic transport  $e^-$  or  $h^+$  have to be excited across the energy gap ( $E_G$ ). Lower  $E_G$  results in lower energy required for carrier excitation to the conduction state. In semiconductors manifesting the highest value of  $zT$  (see Fig. 2-39), the electronic transport is covered by  $e^-$  in conduction band and by  $h^+$  in valence band. Nevertheless, both carrier types have to be excited across the energy gap to participate in the conduction, the quantity of the excited carriers is very important for the  $\sigma$  of the material. To improve the  $zT$   $\sigma$  should be as high as possible, Eq. 2-16 estimates  $\sigma$  in semiconductors using the Boltzmann constant  $k_B=1.3806 \times 10^{-23}$  (J/K) =  $8.6173 \times 10^{-5}$  (eV/K), energy band gap  $E_G$  (eV) and temperature  $T$  (K).

$$\sigma(T) \approx \sigma_0 \cdot \exp\left[-\frac{E_G(T)}{k_B \cdot T}\right] \quad \text{Eq. 2-16}$$

$$\begin{cases} \sigma_p(T) = q \cdot \mu_p(T) \cdot p(T) \\ \sigma_n(T) = q \cdot \mu_n(T) \cdot n(T) \end{cases} \quad \text{Eq. 2-17}$$

Eq. 2-16 shows two possibilities to maximize  $\sigma$ . Firstly, the material should have small  $E_G$  to easily excite the carriers across the gap. Secondly, the carriers should present high mobility which will improve the value of  $\sigma_0$ . According to [Mahan, 1997] the good thermoelectric material should have  $E_G \approx 10 \cdot (k_B \cdot T)$  or 0.25eV at  $T=300K$  remaining high carrier mobilities  $\mu_p$  and  $\mu_n$  at least at the level of  $\mu \approx 2000$  cm<sup>2</sup>/V/s.



In semiconductors, the electrical conductivity significantly depends on doping character following Eq. 2-17. The electrical conductivity depends on the hole  $p$  ( $\text{cm}^{-3}$ ) or electron  $n$  ( $\text{cm}^{-3}$ ) concentrations, the mobilities  $\mu_p$  and  $\mu_n$  and  $q=1.602 \times 10^{-19}$  (C) state for elementary charge. The particularity offered by the semiconductors is the possibility to modulate  $\sigma_n$  and  $\sigma_p$  in very wide range when varying the carriers concentration. Fig. 2-40 presents  $\sigma_n$  and  $\sigma_p$  for Silicon (**Si**) and Germanium (**Ge**), “foundation stone” materials in **CMOS**<sup>19</sup> manufacturing technology.

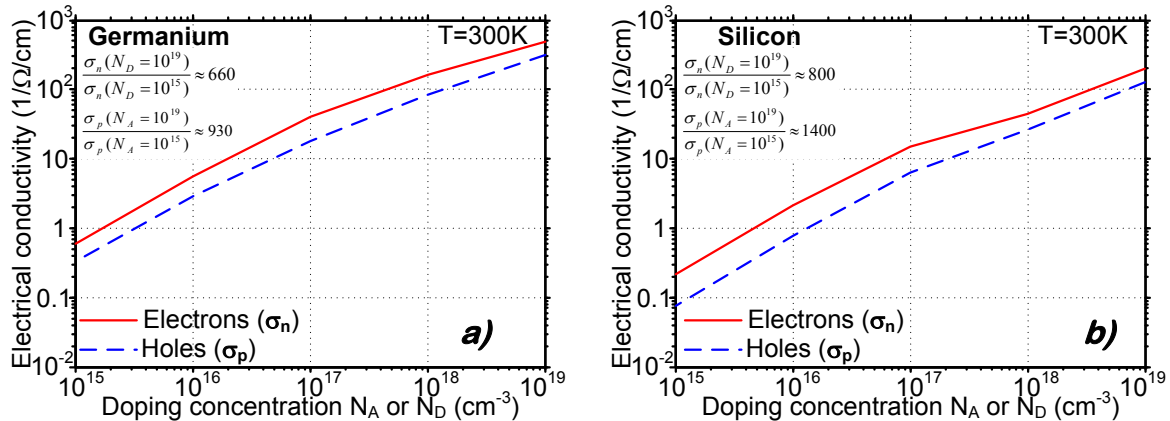


Fig. 2-40 Electrical conductivity at  $T=300\text{K}$  versus doping concentration for a) Germanium and, b) Silicon. In both cases the Arora mobility model was used [Arora, 1982]

Fig. 2-40 shows the possible  $\sigma$  modulation range for both materials when varying the doping concentration. It is depicted that both **Si** and **Ge** have several hundreds higher electrical conductivity for high doping concentration than when lightly doped. This particularity enables the possibility to use the material with optimised, fitted to application value of  $\sigma$ , it will be proved that such particularity is crucial in thermoelectric energy harvesting. In semiconductors, the modulation of electrical transport parameters has minor influence on thermal transport properties. This is very convenient when designing the thermoelectric generator.

#### 2.5.2.1.2 Heat transport

Heat transport mechanism differs significantly from the electronic transport. The heat is propagating through the material using two modes. Dominant propagation mode uses quantized vibrations of the lattice, called phonons, while second mode uses charged carriers such as electrons or holes to propagate [Ziman, 2001]. This dual heat propagation is visible in decomposition of thermal conductivity  $\kappa$  into two components, the dominant phononic  $\kappa_l$  and the negligible electronic  $\kappa_{el}$ . The components are presenting different behaviours over carrier concentration (see Fig. 2-39).  $\kappa_l$  is independent on the carrier concentration while  $\kappa_{el}$  exhibits linear dependence on the carrier density. This linear dependence of  $\kappa_{el}$  can be explained by the increasing number of electrons or holes participating in charge and heat transport simultaneously. Thus,  $\kappa_{el}$  and  $\sigma$  are presenting a linear dependence on carrier density (see Fig. 2-39). Total thermal conductivity  $\kappa$  is the sum of two components Eq. 2-18,  $\kappa_l$  and  $\kappa_{el}$  which can be calculated using Eq. 2-19 and Eq. 2-20 respectively:

<sup>19</sup> **CMOS** (**C**omplementary **M**etal **O**xide **S**emiconductor) – the most popular and frequently used industrial fabrication technology. Most important industrial manufacturers are running on this technology while fabricating their products. Great majority of devices available on the market are fabricated using **CMOS**.

$$\kappa = \kappa_l + \kappa_{el} \quad \text{Eq. 2-18}$$

$$\kappa_l = \frac{1}{3} \cdot L_{ph} \cdot C_h \cdot v_s \quad \text{Eq. 2-19}$$

$$\kappa_{el} = L_0 \cdot \sigma \cdot T \quad \text{Eq. 2-20}$$

where  $L_{ph}$  is an average mean free path for phonons (m),  $C_h$  is heat capacity (J/m<sup>3</sup>/K),  $v_s$  is sound velocity (m/s) and  $L_0=2.443 \times 10^{-8}$  (V<sup>2</sup>/K<sup>2</sup>) is the Lorentz factor. In semiconductors  $\kappa_{el}$  plays negligible role over  $\kappa_l$  which is proved in Table 2-14 reporting thermal conductivity values for given semiconductors.

Referring to the Table 2-14 it can be concluded that heat is transported mainly by the phonons. Moreover, depending on the electrical conductivity for material and the doping concentration level, the contribution of  $\kappa_{el}$  in total  $\kappa$  is comprised between 60% for extremely high doping concentration levels in **Sb<sub>2</sub>Te<sub>3</sub>** material and fraction of percents for lightly doped **Si**. In the case of **Sb<sub>2</sub>Te<sub>3</sub>**  $\kappa_{el}$  is so high due to the high carrier mobilities  $\mu_p \approx 313$  (cm<sup>2</sup>/V/s) at  $T=300$ K and doping level of  $p=10.6 \times 10^{19}$  (cm<sup>-3</sup>) [Skrabek, 1995]. The doping character has slight influence on the thermal conductivity value. Studying the data for **Bi<sub>2</sub>Te<sub>3</sub>** in Table 2-14 for *p*-type and *n*-type doping it can be remarked that the *n*-type material has slightly higher  $\kappa_{el}$  and total  $\kappa$ . It is caused by the fact that electrons (**e<sup>-</sup>**) have higher mobility than holes (**h<sup>+</sup>**).

**Table 2-14 Thermal conductivities components for different materials at T=300K**

Material	Doping concentration	$\kappa_l$	$\kappa_{el} = L_0 \cdot \sigma \cdot T$	$\kappa = \kappa_l + \kappa_{el}$	$\kappa_{el}/\kappa$	Reference
	$\times 10^{19}(\text{cm}^{-3})$	(W/m/K)	(W/m/K)	(W/m/K)		
n-Si	1	155.88	0.12	156	0.08%	[Glassbrenner, 1964]
n-Ge	1	59.65	0.35	60	0.58%	
Si <sub>0.7</sub> Ge <sub>0.3</sub>	3.5	0.9	0.27	1.12	0.19	[Slack, 1991]
n-PbTe	1.6	2.4	1.1	3.5	0.31	[Koh, 2009]
InAs	N/A	30	1.5	31.5	0.05	[Da Rosa, 2009]
InSb	N/A	16	1	17	0.06	
n-Bi <sub>2</sub> Te <sub>3</sub>	1.9	1.41	0.51	1.92	0.27	[Skrabek, 1995]
p-Bi <sub>2</sub> Te <sub>3</sub>	2.0	1.35	0.38	1.73	0.22	
p-Sb <sub>2</sub> Te <sub>3</sub>	10.6	0.60	0.86	1.46	0.59	

Worth considering is the material with  $\kappa_l = \kappa_{el}$  in such case the  $zT$  (Eq. 2-13) can be simplified into Eq. 2-21:

$$zT = \frac{\sigma \cdot S_{(n,p)}^2}{2\kappa_{el}} \cdot T \quad \text{Eq. 2-21}$$

Substituting Eq. 2-20 into the Eq. 2-21 leads to  $zT$  formula for material with equal electronic and phononic contributions of thermal conductivity Eq. 2-22:

$$zT = \frac{S^2}{2 \cdot L_0} \quad \text{Eq. 2-22}$$

$zT$  defined by Eq. 2-22 differs significantly from the general definition in Eq. 2-13. Firstly, the  $zT$  for material with equal  $\kappa_l$  and  $\kappa_{el}$  is independent on temperature. Secondly, the only material variable influencing  $zT$  is the Seebeck coefficient  $S_n$  or  $S_p$  depending on the doping character.  $\kappa_l = \kappa_{el}$  is the condition describing the heat conduction in the theoretical material known as **PGEC** [Slack, 1995]. Interestingly, the  $zT$  formula for **PGEC** (Eq. 2-22) is obtained by modifying only the heat transport properties. In the following, Fig. 2-41 depicts the  $zT$  for **PGEC** material as a function of carrier concentration [Slack, 1995].

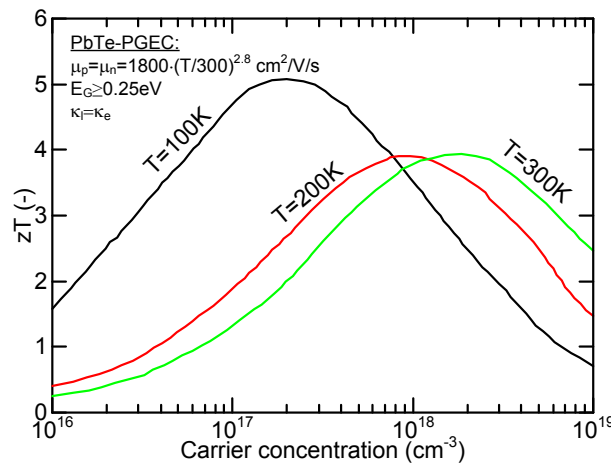


Fig. 2-41 Dimensionless-figure-of-merit for PGEC material versus doping concentration. The material parameters are based on the PbTe except the mobility, energy band gap and the  $\kappa_l = \kappa_{el}$  [Slack, 1995].

Comparing the  $zT$  values depicted in Fig. 2-41 with the values showed in Fig. 2-38a it is visible that suppressing the phononic contribution of thermal conductivity to the electronic level ( $\kappa_l = \kappa_{el}$ ) is significantly improving  $zT$ . **PbTe** with altered thermal transport parameters  $\kappa_l = \kappa_{el}$ , reduced energy band gap to the level of  $E_G = 10 \cdot k_B \cdot T$  and maintained carrier mobility on high level resulted in  $zT$  improvement of around 8-times comparing with the maximal value of  $zT$  for realistic **PbTe**. This significant improvement is mainly achieved by altering thermal transport properties.  $E_G$  and carrier mobility are improving the value of the  $S_{(n,p)}$  but in overall  $zT$  improvement their contribution is less important than the influence of  $\kappa_l$  and  $\kappa_{el}$  equality.

### 2.5.2.1.3 The Seebeck coefficient

The thermopower  $S$  (V/K) is parameter which describes the presence of the Seebeck effect in the given material. The definition of the Seebeck coefficient is the electric potential occurring on the extremities of a material when it is exposed to the temperature difference [Rowe, 1995]. This definition is mathematically represented by Eq. 2-23. However, this direct definition does not take into consideration the material band structure or the material type, making the application of the Eq. 2-23 impossible for some materials. The sign of the  $S$  depends mainly on the electronic conduction parameters of the material. Depending on the material band structure  $S$  can be positive or negative. As presented in Fig. 2-39 the thermopower decreases with increasing carrier concentration resulting in very low absolute value of the thermopower for metals and high values for insulators. General formula allowing determination of the Seebeck coefficient in all materials is very

complicated and thus rarely used in engineer's calculations. However, it has been proved that the  $\mathbf{S}$  can be approximated with satisfying precision basing on  $\sigma$ . Coupling between  $\mathbf{S}$  and  $\sigma$  increases the difficulty to boost  $\mathbf{zT}$ , because of the contrary behaviour of  $\mathbf{S}$  and  $\sigma$  over the doping concentration (look Fig. 2-39). Calculation of the theoretical value of the Seebeck coefficient in metals or degenerate semiconductors<sup>20</sup> is usually performed using simplified formula known as the Mott relation Eq. 2-24 [Cutler, 1969].

$$S = \frac{\Delta V}{\Delta T} \Big|_{\Delta T \rightarrow 0} \quad \text{Eq. 2-23}$$

$$S = \frac{\pi^2 \cdot k_B^2}{3 \cdot q} \cdot T \cdot \left. \frac{d \ln[\sigma(E)]}{dE} \right|_{E=E_F} \quad \text{Eq. 2-24}$$

Eq. 2-24 explains the low values of thermopower in metals and degenerate semiconductors. Derivative of  $\sigma(E)$  with respect to energy at the Fermi level has small value for metals. Seebeck coefficients for different metals are listed in Table 2-15.

**Table 2-15 Seebeck coefficient in metals at T=300K [Rowe, 1995]**

<i>Symbol</i>	<i>S</i> ( $\mu\text{V/K}$ )	<i>Symbol</i>	<i>S</i> ( $\mu\text{V/K}$ )	<i>Symbol</i>	<i>S</i> ( $\mu\text{V/K}$ )	<i>Symbol</i>	<i>S</i> ( $\mu\text{V/K}$ )
Ag	1.51	Eu	24.50	Nb	-0.44	Sr	1.10
Al	-1.66	Fe	15.00	Nd	-2.30	Ta	-1.90
Au	1.94	Gd	-1.60	Ni	-19.50	Tb	-1.00
Ba	12.10	Hf	5.50	Np	-3.10	Th	-3.20
Be	1.70	Ho	-1.60	Os	-4.40	Ti	9.10
Ca	10.30	In	1.68	Pb	-1.05	Tl	0.30
Cd	2.55	Ir	0.86	Pd	-10.70	Tm	1.90
Ce	6.20	K	-13.70	Rb	-10.00	U	7.10
Co	-30.80	La	1.70	Re	-5.90	V	0.23
Cr	21.80	Lu	-4.30	Rh	0.60	W	0.90
Cs	-0.90	Mg	-1.46	Ru	-1.40	Y	-0.70
Cu	1.83	Mn	-9.80	Sc	-19.00	Yb	30.00
Dy	-1.80	Mo	5.60	Sm	1.20	Zn	2.40
Er	-0.10	Na	-6.30	Sn	-1.00	Zr	8.90

Surprisingly, thermopower in metals listed in Table 2-15 attains positive and negative values. Despite the purely electron conduction (*n-type conduction*) in metals, for some of them the thermopower has positive sign. The explanation for this can be found in Eq. 2-24. The derivative of  $\sigma(E)$  with respect to energy at Fermi level can be positive or negative. It is positive when the  $\sigma(E)$  depends more on the electrons with higher energy than  $E_F$ , and

<sup>20</sup> Degenerate semiconductor is the semiconductor with very high doping concentration level this causes more metallic than semiconductor behaviour. Semiconductor is degenerate when the distance of Fermi level  $E_F$  from the valence (for *p-type*) or conduction (for *n-type*) band edge has to be smaller than  $3k_B T$ .

negative in the opposite situation [Dugdale, 1995]. Regardless of the sign of the thermopower it has to be noted that the absolute value of the Seebeck coefficient in metals is very small, largely lower than  $100\mu\text{V/K}$ . This makes metals not adapted and rarely used in thermoelectric energy harvesting.

In semiconductors thermopower has different character due to different energy band structure. The basic definition of the thermopower in semiconductors is presented by the Eq. 2-25. Possible dual conduction type in semiconductors involving the doping character (*donor p-type or acceptor n-type*) and conduction type (*hole conduction p-type or electron conduction n-type*) results in dual definition of the Seebeck coefficient,  $S_n$  is valid in *n*-type semiconductors while  $S_p$  holds in *p*-type semiconductors [Rowe, 1995].

$$\begin{cases} S_n = \frac{1}{q} \frac{dE_{Fn}}{dT} \\ S_p = \frac{1}{q} \frac{dE_{Fp}}{dT} \end{cases} \quad \text{Eq. 2-25}$$

Nevertheless the doping type, the general definition of thermopower in semiconductors relies on the derivative of electron ( $E_{Fn}$ ) or holes ( $E_{Fp}$ ) Fermi levels with respect to temperature Eq. 2-25. Calculating the derivative in Eq. 2-25 results in simplified form of thermopower in semiconductors:

$$\begin{cases} S_n = -\frac{k_B}{q} \cdot \left[ \frac{5}{2} + \ln\left(\frac{N_C}{n}\right) + P_{\mu n} \right] \\ S_p = \frac{k_B}{q} \cdot \left[ \frac{5}{2} + \ln\left(\frac{N_V}{p}\right) + P_{\mu p} \right] \end{cases} \quad \text{Eq. 2-26}$$

Investigating Eq. 2-26 leads to conclusion that both  $S_n$  and  $S_p$  are depending mainly on density of states in conduction  $N_C$  and valence  $N_V$  band and the electrons  $n$  and holes  $p$  concentration. The coefficients  $P_{\mu p}$  and  $P_{\mu n}$  are describing how the temperature is influencing the carriers mobility. For Silicon  $P_{\mu p}$  and  $P_{\mu n}$  are in the range between -1 and 2 [Silvaco, 2012]. Worth noting is the fact that the thermopower depends mainly on the majority carriers concentration, the minority carriers are playing negligible role. Eq. 2-26 is the simplified form which omits the effect of phonon drag important in low temperature and low doping levels. The dual character of the thermopower in *n*-type and *p*-type semiconductor results in opposite sign of thermopower: negative for  $S_n$  and positive for  $S_p$ . Table 2-16 is presenting few values of thermopower for chosen bulk semiconductors:

Table 2-16 The maximal value of the Seebeck coefficient for bulk conventional semiconductors

<i>Symbol</i>	$\rho$ ( $\Omega\text{m}$ )	$S_{MAX}$ ( $\mu\text{V/K}$ )	<i>Reference</i>	<i>Symbol</i>	$\rho$ ( $\Omega\text{m}$ )	$S_{MAX}$ ( $\mu\text{V/K}$ )	<i>Reference</i>
n-Si	$2.5 \times 10^{-5}$	-300	[Geballe, 1955]	n-PbTe	$5 \times 10^{-3}$	-273	[Danko, 1962]
p-Si	$6.4 \times 10^{-5}$	500		p-PbTe	$8 \times 10^{-3}$	298	
n-Ge	0.17	-1070	[Freud, 1965]	n-Si <sub>0.7</sub> Ge <sub>0.3</sub>	$4.8 \times 10^{-5}$	-350	[Dismukes, 1964]
p-Ge	0.105	1060		p-Si <sub>0.7</sub> Ge <sub>0.3</sub>	$3.19 \times 10^{-5}$	240	
n-Bi <sub>2</sub> Te <sub>3</sub>	$8.2 \times 10^{-6}$	-210	[Heikes, 1961]	n-InAs	$2.0 \times 10^{-5}$	-180	[Hockings, 1966]
p-Bi <sub>2</sub> Te <sub>3</sub>	$1.2 \times 10^{-5}$	190		p-InAs	$2.0 \times 10^{-5}$	200	
p-TAGS <sup>†</sup>	$1.25 \times 10^{-3}$	200	[Rowe, 1995]	p-Sb <sub>2</sub> Te <sub>3</sub>	$5.0 \times 10^{-6}$	130	[Goldsmid, 1960]

<sup>†</sup>TAGS – composition of Te/Sb/Ge/Ag largely used in thermoelectricity

Table 2-16 presents the maximal value of the thermopower for the most conventional bulk semiconductors used in thermoelectricity. Analyzing Table 2-16 leads to the conclusion that the thermopower in semiconductors significantly exceeds the values measured in metals listed in Table 2-15. Moreover, the dependence of thermopower on the sample resistivity is visible. Thermopower and electrical resistivity are exhibiting proportional relation, the thermopower is higher for highly resistive materials (*materials with low doping concentration*). Table 2-16 lists the maximal value of the thermopower regardless the temperature for which the  $S_{MAX}$  is attained. However, when studying Fig. 2-38a the maximal value of  $zT$  occurs at different temperatures for given material. It can be concluded that the maximal performance of thermoelectric material depends on numerous factors, the temperature difference, electric and heat transport properties. The choice of the material for thermoelectric energy harvesting is multi-conditional where numerous possible solutions are possible.

#### 2.5.2.1.4 Summary

Referring to the previous brief review on the requirements for materials dedicated for thermoelectric energy harvesting it can be concluded that semiconductors are largely outperforming other materials as it was already graphically presented in Fig. 2-39. To understand this situation three main advantageous properties of semiconductors should be reminded:

- Character of heat transport in semiconductors is decomposed into two main contributions. Dominant part of heat is propagating using phonons and less important part uses charged carriers to propagate. This particular property indicates that heat transport is very well decoupled from electronic transport. Offering an opportunity to independently alternate heat transport properties with minor impact on the electric properties of the material.
- The current uses the charged carriers to propagate through the semiconductor, the transport properties can be modulated in very wide range by varying the doping concentration. Increasing carrier concentration results in the rise of electrical conductivity  $\sigma$  and reduction of Seebeck coefficient  $S$ . The carrier concentration can be altered in rather simple way by choosing doping concentration. This possibility enables to fit the carrier concentration in such a way to achieve the highest performance.
- The thermopower  $S$  in semiconductor has higher absolute values than in metals.  $S$  is inversely proportional to doping concentration enabling possibility to create voltage source (*with very high internal resistance*) rather easily when using lightly doped semiconductors.

However, big challenge is the interdependence of  $S$  and  $\sigma$  on doping concentration. This interdependence is significantly increasing the optimization difficulty. Moreover, to achieve  $\sigma$ ,  $\kappa$  and  $S$  on the satisfying levels allowing the improvement of  $zT$  value (*see Eq. 2-13*) lead to the use of sophisticated, harmful, complex, incompatible with industrial fabrication technologies *e.g.* **CMOS** and expensive materials.  $zT$  for some of them is depicted in Fig. 2-38a. Requirements for material dedicated for thermoelectric energy scavenging were hindering the spread applications on the market, to spatial [\[Rowe, 1991\]](#), medical [\[Francioso, 2011\]](#), automotive [\[Yang, 2006\]](#) and sophisticated industrial [\[Nenninger, 2011\]](#) use. Popularization of thermoelectricity on the market is possible through the material cost reduction. To achieve the goal two strategies can be adopted:

- the quest for new thermoelectric material which exhibits satisfying performance under low fabrication costs
- the use of industrial massive production which will reduce the unit cost of the thermo-generator.

The first possibility is focused on the material fabrication exhibiting the properties close to **PGEC** (*phonon-glass/electron crystal*) see section 2.5.2.1. The development of the material engineering together with the use of nano- and micro-technologies allowed the fabrication of new materials with improved thermoelectric properties. Among numerous innovations especially skutterudites and clathrates are the most promising.

Both skutterudites and clathrates are presenting significant reduction of lattice thermal conductivity ( $\kappa_l$ ). Reduction of  $\kappa_l$  is realized by placing big and heavy atom inside the “cage” as illustrated in Fig. 2-42. Distinguishing skutterudites and clathrates can be done analyzing the “cage” topology. Clathrates have the crystalline topology of the “cage” [Nolas, 2001] while skutterudites not. The placement of big metallic atoms inside the “cage” results in creation of phonon scattering centres while cage is responsible for electrical properties. As a result of this approach  $zT=1.4$  was reported for both *n*-type  $\text{LaFe}_3\text{CoSb}_{12}$  and *p*-type  $\text{CeFe}_3\text{CoSb}_{12}$  skutterudite above 1200K [Fleurial, 1996]. For clathrate topology depicted in Fig. 2-42b the maximal estimated value of  $zT=1.7$  at 800K was reported in [Kuznetsov, 2000]. Both skutterudites and clathrates are promising thermoelectric materials with numerous research actually ongoing around the world. However, the industrial application of them is very difficult due to the use of expensive fabrication technologies and/or rare and costly materials.

Materials based on bulk **Bi**, **Te**, **Sb** or **Pb** are the most popular on the thermoelectric market. However, since their discovery and commercialization their parameters have not been significantly improved causing progress stagnation in commercially available thermoelectric devices. Improvement of the bulk material fabrication technologies can improve the performance but in insufficient way. Thus, the innovation in the industrialized thermoelectric materials relies on the change of their properties by using mainly nanostructurization of industrially compatible materials [Rowe, 2012]. Heat and electric transport properties are very well decoupled in semiconductors and the nanostructurization enables reduction of the heat transport properties without altering electric properties (*this approach will be more precisely described in the next chapter*). Other possibilities are also used, the fabrication of heterostructures and superlattice enables the significant improvement of thermoelectric properties. The actual maximal value of  $zT \approx 2.4 @ 300\text{K}$  was reported in superlattice material composed from  $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ , since so far this is the most efficient thermoelectric *p*-type material [Venkatasubramanian, 2001].

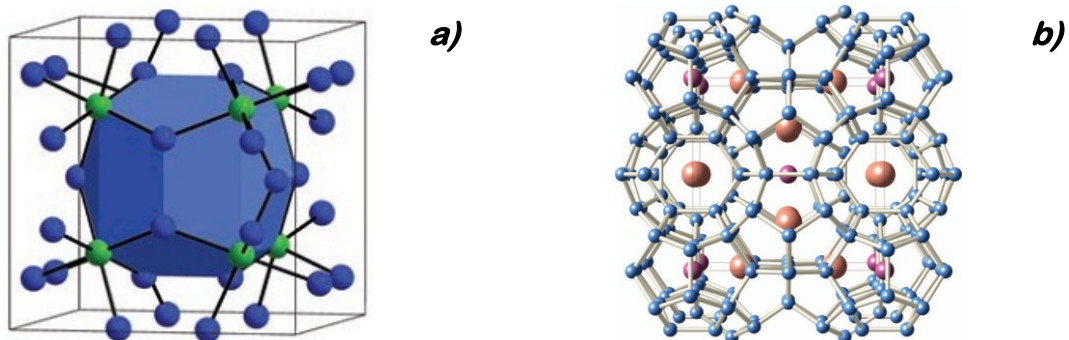


Fig. 2-42 a) Schematic illustration of a  $\text{CoSb}_3$ -type skutterudite crystal, b) the example of clathrate crystal, the cage has crystalline form atoms showed on blue the guest atoms are showed on red.

This thesis manuscript is too short to make detailed review of all  $zT$  improvements possibilities. Table 2-17 compares thermoelectric parameters for few chosen bulk semiconductors:

**Table 2-17 Summary of thermoelectric performance for chosen bulk materials**

<i>Material</i>	$zT_{MAX}$	<i>T range</i>	$S @ zT_{MAX}$	$\sigma @ zT_{MAX}$	$\kappa @ zT_{MAX}$	<i>Reference</i>
	(-)	(K)	( $\mu V/K$ )	( $1/\Omega/m$ )	( $W/m/K$ )	
n-Si	0.06	800-1200	-382	$1.05 \times 10^4$	30.61	Own calculations
p-Si	0.03	800-1200	345	$0.59 \times 10^4$	29.81	
n-Ge	0.13	800-1200	-253	$4.31 \times 10^4$	17.61	
p-Ge	0.03	800-1200	202	$1.39 \times 10^4$		
n-Si <sub>0.3</sub> Ge <sub>0.7</sub>	0.89	800-1200	-289	$5.08 \times 10^4$	4.77	
p-Si <sub>0.3</sub> Ge <sub>0.7</sub>	0.6	800-1200	234	$5.44 \times 10^4$	4.49	
n-Bi <sub>2</sub> Te <sub>3</sub>	1.02	300-500	-240	$10 \times 10^4$	2.02	
p-Bi <sub>2</sub> Te <sub>3</sub>	0.93	300-500	162	$18 \times 10^4$	2.06	
p-Sb <sub>2</sub> Te <sub>3</sub>	1.13	300-500	115	$30.96 \times 10^4$	1.63	
n-PbTe	0.6	350-550	-244	$12.98 \times 10^4$	5.18	
TAGS-85	1.23	500-800	190	$8 \times 10^4$	1.6	

Table 2-17 presents the thermoelectric performance for given materials. Presented materials, except bulk **Si** and bulk **Ge**, are conventional and industrialized thermoelectrics. Studying Table 2-17 leads to conclusion that the choice of thermoelectric material is not simple, to maximize the generator performance the  $zT$  value has to be as high as possible. Knowing that the material parameters are depending on the temperature the  $zT$  maximal value depends also on the temperature. Thus the choice of the material dedicated to thermoelectric generation is complex, with multiple possible solutions, however one of the important criteria is the optimal working temperature range. Additionally, it is worth noting that the range of  $zT$  values is very wide, the values are comprised between 0.03 and 1.23. In general, for given material the  $zT$  values are slightly lower for *p*-type doping. This is the result of lower electrical conductivity and thermopower for *p*-type doping. Interestingly the value of figure of merit for bulk **Si** and bulk **Ge** are extremely small compared to other materials in Table 2-17. Despite huge industrial popularity of **Si** and **Ge** this deficiency explains their unpopularity in thermoelectricity.

Focusing on the industrialization of thermoelectric devices an important criterion is the fabrication technology. The most popular and frequently used technology in electron devices industry is the **CMOS** (**C**omplementary **M**etal-**O**xide **S**emiconductor) technology. This technology fabricates significant majority of electronic components such as *e.g.* transistors,  $\mu$ -processors, **MEMS/NEMS**<sup>21</sup> *etc.* However, **CMOS** technology accepts only **Si**, **Ge** or **Si<sub>x</sub>Ge<sub>1-x</sub>** for a technological material since machines, production lines and fabrication procedures are only compatible with them. Unfortunately, among the **CMOS**

<sup>21</sup> **MEMS** **M**icro-**E**lectro-**M**echanical **S**ystems – it is big family of devices also called micro-machines. Some applications are including: accelerometers, gyroscopes, inertial measurement units, microphones, resonators, radio frequency devices, pressure sensors, fluid acceleration measurement unit, kinetic energy harvesters *etc.*

**NEMS** **N**ano-**E**lectro-**M**echanical **S**ystems – the same concept as **MEMS** but with nanometric dimensionality



compatible materials only  $\text{Si}_x\text{Ge}_{1-x}$  is used in thermoelectricity as material dedicated for high-temperature energy harvesting. Fabrication of **CMOS** compatible thermoelectric generators will contribute to:

- popularization of thermoelectric energy harvesting on the market,
- reduction of fabrication costs,
- preservation of natural environment by using of environmentally friendly materials,
- full integration of the thermoelectric devices on chip reducing the parasitics.

According to [Tritt, 2008] the  $n$ -type and  $p$ -type bulk materials with  $zT \geq 4$  each and low fabrication costs will be the 'Holy Grail' for thermoelectricity. This threshold of  $zT \approx 4$  will enable the popularization of thermoelectric energy harvesting on the market because the generator will be comparably efficient to the thermodynamic engines running on the Rankine cycle (see Fig. 2-38b). As it was already described, material with  $zT \approx 4$  or higher is possible when the electronic and phononic contributions of thermal conductivity are equal ( $\kappa_F = \kappa_{el}$ ) maintaining the electronic transport properties at the highest possible level. Such material is not yet available and thus the thermoelectric conversion cannot overcome the popularization issues. Investigating maximal  $zT$  value versus year of the material discovery depicted in Fig. 2-43 it is easy to note that the optimisation of  $zT$  is very difficult task. Firstly, for more than three decades the maximal value of  $zT$  was below unity. Secondly, Fig. 2-43 illustrates another interesting thing, focusing only on the last decade it can be concluded that the number of reported efficient thermoelectric materials is significantly increasing.

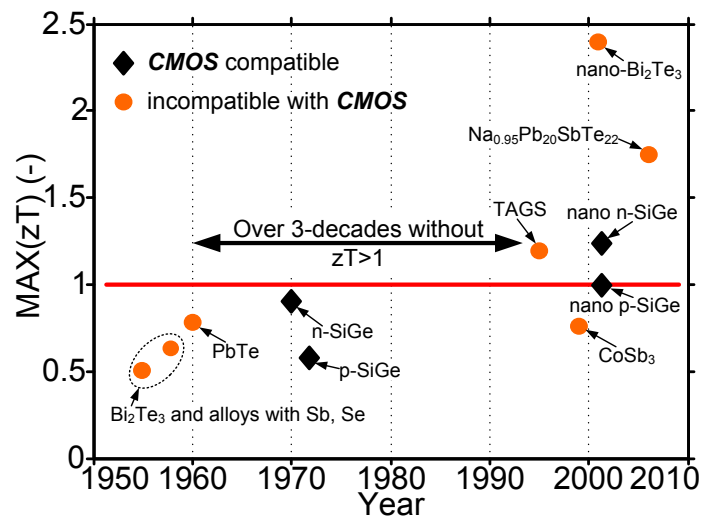


Fig. 2-43 History of the thermoelectric dimensionless figure of merit  $zT$ , black diamond markers are materials compatible with CMOS technologies [Majumdar, 2004]

Since 2001 reported by [Venkatasubramanian, 2001]  $zT$  value of over 2 remains unbeatable. Referring to the popularization threshold ( $zT \geq 4$ ) determined by [Tritt, 2008] it has to be remarked that current state-of-the-art is far away from this goal. Moreover, in general the most efficient thermoelectric materials are costly to fabricate. Mainly due to the use of expensive materials and/or because of the material nanostructurization.

In the following the highlight of the conventional approach for thermoelectric devices is presented.

### 2.5.2.2 Thermoelectric generation the conventional approach

Putting together theoretical background of the thermoelectric conversion and being aware of material requirements, it is now time to present conventional approach for energy harvesting using thermoelectric effect.

As previously mentioned, semiconductors are the most adapted materials to be used in the thermoelectric energy harvesting. Semiconductors are compromising three thermoelectrically important material parameters  $\sigma$ ,  $S$ , and  $\kappa$ . This results in the highest value of  $zT$  comparing with metals and insulators (see Fig. 2-39). It has to be underlined that owing to different doping character, thermoelectric properties of  $p$ -type and  $n$ -type semiconductors are different. The property of very high practical importance is dependence of thermally built-in voltage on the doping character (see Fig. 2-36). For identically imposed temperature along the semiconductor rod the voltage has opposite direction for  $n$ - and  $p$ -doping. This particularity has very high importance when constructing the **ThermoElectric Generator (TEG)** which is illustrated in Fig. 2-44.

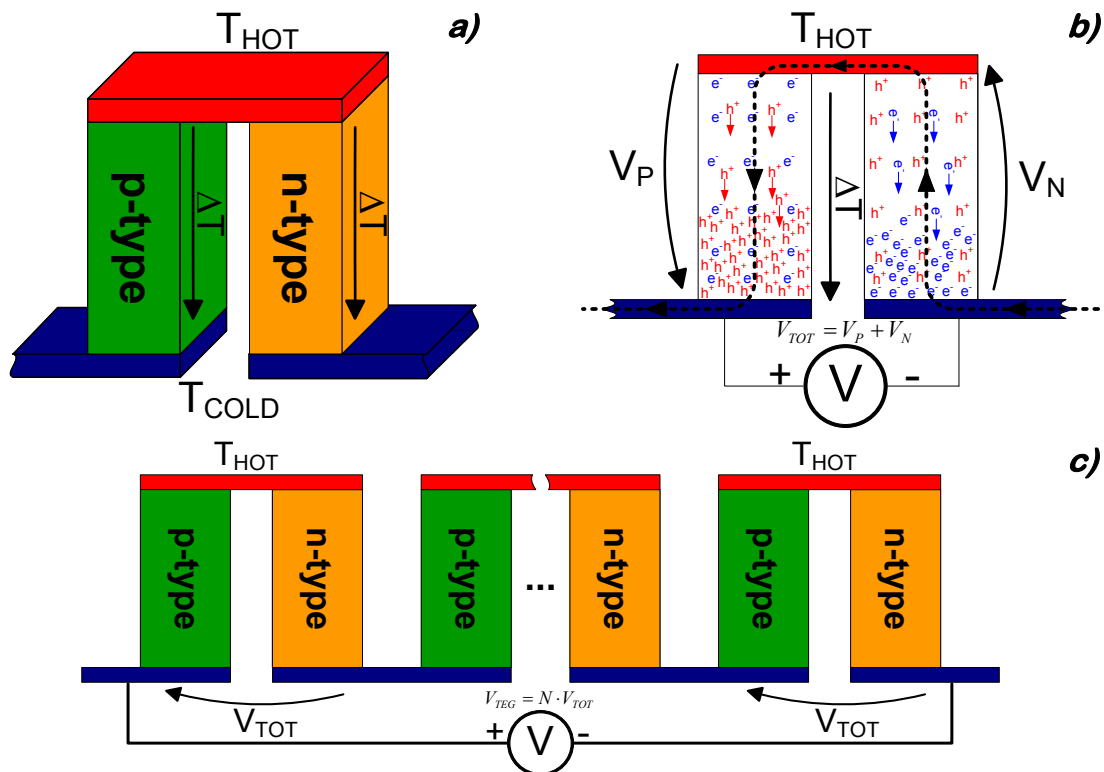


Fig. 2-44 a)  $\pi$ -type thermo-couple topology thermoelectric device,  $n$ -type and  $p$ -type rods encapsulated between hot and cold plates, electrical series connection, thermal parallel connection, b) thermally induced carrier separation results in output voltage addition, c) side view on the thermo-couple's interconnections in the thermoelectric generator

Fig. 2-44 presents a conventional  $\pi$ -type topology of **TEG**. The semiconducting rods from Fig. 2-36 are placed between thermally and electrically conducting plates, one of the plates has higher temperature. As a result of that connection the Seebeck effect occurs separately in each of the rods. In thermoelectric effect the majority carriers are flowing towards lower temperature, results in the voltage formation in opposite directions Fig. 2-44b. Because of that the total output voltage  $V_{TOT}$  is the sum of the two contributing voltages  $V_N$  formed in  $n$ -type rod and  $V_P$  formed in  $p$ -type rod as described by the Eq. 2-27. **TEG** output voltage is improved due to the use of semiconductors with different doping character. Moreover, when studying this topology from thermal point of view, it

can be remarked that both  $n$ -type and  $p$ -type rods are submitted to the same thermal conditions, are both placed between the same difference of temperature  $\Delta T$  as shown in Fig. 2-44a. Thus, thermally the rods are connected in parallel. However, to consider the electrical configuration the current path has to be determined. Dashed line in Fig. 2-44b illustrates the current path through the generator, it is easy to conclude that the rods are electrically connected in series. Merging together electrical series and thermal parallel connection largely simplifies the topology and improves the output voltage. This mixed connection type is easily achieved through the use of opposite doping types. The  $\pi$ -type thermoelectric generator topology is the most popular, the majority of industrially fabricated generators are based on this topology. However, the drawbacks of it are: (i) relatively low topology filling which is the ratio of cross-sectional surface of the semiconductors to the total in-plane surface of the generator, (ii) the necessity to use relatively long semiconductors rods to ensure good thermal insulation between hot and cold plates and (iii) impossibility to fabricate such topology integrating mechanical flexibility into the generator due to the destructive influence of mechanical bending of the rods which causes the detachment of the semiconductors from the plates.

$$V_{TOT} = V_P + V_N \quad \text{Eq. 2-27}$$

$$V_{TEG} = N \cdot V_{TOT} \quad \text{Eq. 2-28}$$

$$V_{TEG} = N \cdot \Delta T \cdot (S_P - S_N) \quad \text{Eq. 2-29}$$

Considering the values of Seebeck coefficients for conventional bulk semiconductors listed in Table 2-16 and Table 2-17 leads to conclude that single thermo-couple will not be able to generate significant output voltage. To overcome this difficulty, in practice the complete thermoelectric generator consists in several thermo-couples connected electrically in series, as it is presented on the side view of Fig. 2-44c. Connecting  $N$  thermo-couples as presented in Fig. 2-44c multiplies  $N$ -times the output voltage from single thermo-couple forming the thermoelectric generator output voltage  $V_{TEG}$  as described by Eq. 2-28. Assuming  $T_{HOT}$  and the  $T_{COLD}$  to be constant and neglecting the dependence of both thermopowers  $S_N$  and  $S_P$  on the temperature simplifies the integrals in Eq. 2-11 and Eq. 2-12. Under such assumptions Eq. 2-28 can be rewritten by substituting the simplified form of Eq. 2-11 and Eq. 2-12, the  $V_{TEG}$  can be calculated using the thermopowers of used semiconductors following Eq. 2-29.

### 2.5.3 Summary

In this section the focus is put on the energy conversion using thermoelectric effect. Starting from the historical background (*see section 2.5.1*), passing through the basic theory of thermoelectric effect (*see section 2.5.2*), evaluating of the material requirements (*see section 2.5.2.1*) and ending on the description of conventional thermo-generator topology (*see section 2.5.2.2*).

Regarding the advantages of thermoelectric energy production (*see section 2.5.1.2*), development of the new materials (*see section 2.5.2.1.4*) and the quantity of possible application on the market (*see section 2.5.1.2 and 2.5.1.3*) it is understandable that in the field of thermoelectricity significant progress has been achieved. To indicate the thermoelectricity development, the number of commercialized solutions, founded

companies and market forecast (see Fig. 2-34) can be used. Actually on the market there are many examples of companies which are fabricating **TEGs**, Table 2-18 compares the performance of few of them.

Studying Table 2-18 it is evident to note that the thermoelectric industry exhibits very high diversity. However, on the market mainly the application dedicated for harvesting from middle- or room temperature range are available. Thus most of listed devices use the **Bi-Te** alloys as material. Sophisticated and dedicated solutions are designed and sold directly between the manufacturer and the client omitting the internet or press announcement and/or without detailed performance and cost specification. Generally the manufacturers are protecting the information referring to the number of thermocouples, price of the module and used material composition.

The spread market offer is manifested comparing generator price and output power density. Referring to the price per watt it has to be noted that one watt of harvested electricity costs from 2.41\$/W to even 350\$/W. Such wide interval is mainly caused by (i) different manufacturing technologies, (ii) production scale and (iii) material processing costs. The material itself represents major share in overall price of the device. The micro-generators based on thin-film materials have high cost per watt. This is mainly due to small harvested power and high generator fabrication costs.

When studying power density for commercialized generators it has to be noted that the power per volume unit is comprised between fractions of  $W/cm^3$  and over  $20W/cm^3$ . The harvested power density is mainly depending on the used material and the generator working conditions e.g. temperature drop across **TEG**. For **Bi-Te** alloys the maximal commercialized power density equals  $3.8W/cm^3$ , produced in thin-film form.

Regarding on the market of thermoelectric generators we can observe progressing trend. The market divides the producers on the companies which are fabricating conventional bulk-type thermoelectric generators, and on the producers fabricating nano-structured materials such as thin-films, clathrates or skutterudites. The fabrication of such materials is possible when using sophisticated and costly technology. Commercialization of the generators based on thin-film materials enabled micro-energy harvesting. The overall cost of such generators is rather small <5\$ [[Habbe, 2011](#)] which encourages the potential clients. Such micro-harvesters are dedicated to sensors supplying with possibility of wireless communication (*this concept was briefly described in the section 1.1.3*).

**Table 2-18 Chosen available on market thermoelectric generators with corresponding parameters**

<i>Manufacturer</i>	<i>Model</i>	$T_{HOT}$	$T_{COLD}$	<i>Number of thermocouples</i>	$Power^\dagger$	<i>Voltage</i>	$Price^\S$	<i>Dimensions</i> <small>Length×Width×Thickness</small>	<i>Power density</i>	<i>Material</i>
		(K)	(K)		(W)	(V)	(\$/W)	(mm×mm×mm)	(W/cm <sup>3</sup> )	
Crystal Ltd.	G-127-10-05-L2	423	323	127	4.06	2.87	4.84	30×34×2.8	1.42	Bi-Te
Custom Thermoelectric	2411G-7L31-15CX1	573	303	N/A	21.6	7.2	2.41	56×56×4.45	1.55	Bi-Te
HiCOOLTEC	TEG-19-1810	463	338	N/A	8.8	4.2	N/A	56×56×4.7	0.60	N/A
Hi-Z	HZ-20	500	300	71	19	2.38	5.75	75×75×5.08	0.66	Bi-Te
HotBlock OnBoard	Nemo	853	353	N/A	3.6±5%	2.6±5%	N/A	20×24×7.1	1.056	Si based alloy
Kryotherm	TGM-127-1.0-0.8	423	323	127	1.38	1.83	24.6	30×30×3.1	0.49	N/A
Laird	eTEG-PG24	400	300	N/A	90×10 <sup>-3</sup>	0.85	~170	3.39×2.05×0.56	23.13	N/A*
Marlow Industries	TG12-8	523	323	N/A	7.95	5.25	5.67	17.6×15.8×3.53	0.82	N/A
Micr°Pelt	MPG-D751	330	300	540	14×10 <sup>-3</sup>	2.25	~350	4.248×3.364×1.09	0.9	Bi-Te*
Nextreame	N <sub>x</sub> 2	423	303	16	0.174	0.235	N/A	5×6×0.7	8.29	N/A
TEC	TEG1-PB-12611-6.0	623	303	N/A	21.7	4.6	4.42	56×56×8	0.86	Pb-Bi-Te
Tellurex	G3-56-0419	573	303	N/A	19.3	4.2	5.7	56×56×5	1.23	N/A
EURECA	TEG1-9.1-9.9-0.8	500	200	N/A	0.8	5.4	N/A	9.1×9.9×2.3	3.86	Bi-Te*
Wellen Tech.	TEG-10-60	423	303	60	2.4	2.35	N/A	50×50×4.5	0.21	N/A

<sup>†</sup>Output power at matched load condition (*maximal generator efficiency*)

<sup>§</sup>shipping cost not included

\*Thin-film material

After reading this section it can be underlined that the thermoelectricity is entering in completely new age. Owing to: (i) development new and more efficient materials, (ii) use of nano- and micro- fabrication technologies and (iii) cost reduction. It is now possible to produce small, efficient and competitively cheap **TEGs**. The thermoelectricity is expanding on the market marking the transition from devices reserved for sophisticated spatial/military use (*as it was mainly in the late 60s*) to popular, ordinary, easily available and renewable energy source for the medical, domestic, industrial *etc.* use. The expansion of this branch of industry is confirmed by the market (*see Fig. 2-34*), ensuring manufacturers about continually rising demand on such devices.

However, the thermoelectric harvesting hasn't been yet tamed. To become more attractive and popular, thermoelectricity has to find a material with parameters close to **PGEC** (*see section 2.5.2.1 and paragraph 2.5.2.1.2*). Current state-of-the-art proposes the materials which significantly differ from the expected 'Holy Grail' (*see section 2.5.2.1.4*) material. Thus there is still a lot of work to place thermoelectricity on the appropriate degree of dignity.

## 2.6 Chapter Summary


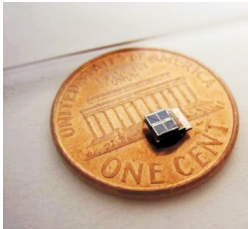
In this chapter a bird's eye view on the energy harvesting methods was presented. The diversity and richness of energy waste in the world allows to produce additional energy from mechanical (*subchapter 2.2*), electromagnetic waves (*subchapter 2.3*), light (*subchapter 2.4*) and thermal waste (*subchapter 2.5*). Each of listed harvesting methods offers advantages and defects. It is crucial to underline that at least part of the global energy waste can be recovered. The opportunity of transforming energy losses into useful energy becomes extremely important in light of: (i) growing energy consumption, (ii) rising world population and (iii) limited fossils fuels resources (*which was highlighted in the Chapter 1*).

After the lecture of this chapter it can be concluded that the energy is everywhere (*humanity is consuming at the very most half of the input primary energy, other half is lost*). Fig. 2-1 illustrates clearly that the covered power density and output voltage range is very large for different harvesting methods.


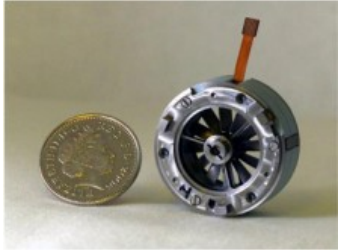
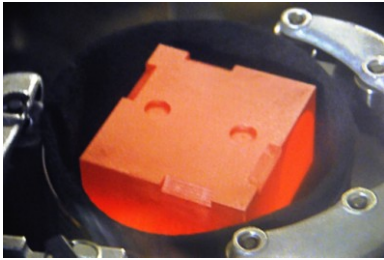
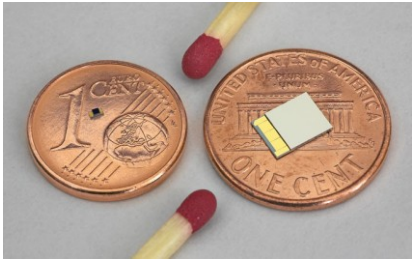
Taking into account abovementioned arguments it can be concluded that humanity is entering in the age of energy production from wastes. Since long time it is possible to produce renewable energy in macro scale, but since last decade new concepts of energy harvesting on micro and nano-scale are possible. Energy scavenging on micro-scale is inspired by the renewable energy sources on macro-scale Table 2-19.

Studying the Table 2-19 lead to conclude that using the same physical effect the produced power can be scaled in mega-watts or nano-watts. Scaling down the energy harvesters enables: (i) easy installation without changing the landscape, (ii) spreading the alternative sources of energy due to attractive cost reduction, (iii) energetic autonomy of the micro-power devices and (iv) covering the power requirements for micro-consumption devices which number is significantly increasing.

**Table 2-19 Comparison macro- and micro-scale energy harvesting methods**

<i>Energy Type</i>	<i>Macro scale</i>	<i>Micro-scale</i>
<b>Solar</b>		
	<p>“Desert Light” California solar power plant 1 540 hectares, 550MW of power [<a href="#">Sanburn, 2015</a>]</p>	<p>Solar cell with integrated pressure monitor 1.5mm<sup>3</sup> of volume, 80.6nW of power [<a href="#">Chen, 2011</a>]</p>

Continuation Table 2-19 Comparison macro- and micro-scale energy harvesting methods

Energy Type	Macro scale	Micro-scale
Wind	 <p>ST10 wind turbine output power 10MW, rotor diameter 164m [<a href="#">Power Technology, 2014</a>]</p>	 <p>Indoor air flow turbine power 3mW, diameter 3.2cm [<a href="#">Howey, 2011</a>]</p>
Thermal	 <p>Radioactive Thermo-Electric Generator used on the mission to Mars, delivered power 2.5kW·h daily continuous power 100W [<a href="#">Misra, 2006</a>]</p>	 <p>MPG-D751 micro-scale thermoelectric generators power of 14mW @ <math>\Delta T=30K</math>, the volume of 15.44mm<sup>3</sup> [<a href="#">Micropelt GmbH, 2008</a>]</p>

One of the most important difference between micro- and macro-scale renewable sources of energy is the fact that when using micro-scale harvesters the total energy autonomy of the system can be achieved. The energy autonomy cannot be achieved considering macro-scale power system.

As already mentioned the energy production from waste is crucial and strategic to maintain social and economical growth. In light of this argument it can be concluded that globally we are entering into the age of energy production from wastes. On the development of energetically and economically efficient energy harvesting method relies the global energetic stability of the future world. Future years will give an answer to this question: "Have we started the energy harvest time?"





# Chapter 3: Innovative thermoelectrics – Modelling and simulations

This chapter presents the innovative trends in thermoelectricity on the material and topological level. A comprehensive and compact comparative study of the thermoelectric harvesting capabilities for different materials focusing on **CMOS** compatible materials is provided. Thermoelectric capabilities are simulated based on the doping- and temperature-dependent modelling of carrier concentrations ( $n$ ,  $p$ ,  $n_i$ ,  $N_C$ ,  $N_V$ ), mobilities ( $\mu_{n,p}$ ), Seebeck coefficients ( $S_{n,p}$ ) and electrical conductivities ( $\sigma_{n,p}$ ). Constructed model evaluates the theoretical limit of harvested electric power without referring to the thermal conductivity ( $\kappa$ ) and assuming temperature drop across **ThermoElectric Generator (TEG)** to be constant ( $\Delta T = const.$ ). Firstly, the model is used upon insulated media to confront it with experimental data. Secondly, electrical performance of **CMOS** compatible **TEGs** is modelled and compared with harvesting capabilities of **Bi<sub>2</sub>Te<sub>3</sub>**-based generator. Different unconventional architectures of **TEGs** are investigated to put in evidence the impact of topology on the performance. Thirdly, the analysis is completed by studying **TEG** conversion efficiency ( $\eta$ ) considering the size-induced  $\kappa$  reduction. Comparative studies of the harvested power density put the **CMOS** compatible materials in competitive position compared with conventional thermoelectrics. Comparable harvested power density level for classic thermoelectrics and **CMOS** compatible materials shows a big potential of the latter in thermoelectricity. Reduction of  $\kappa$  improves  $\eta$  up to 10× over efficiency for **TEG** based on bulk material. Finally, studies put in evidence the fact that thermoelectric effect is more efficient harvesting mechanism than the thermal generation of free carriers in the *pn* junction.

Dual development of **TEG** both on material and topological level is incomparably contributing making the thermoelectric conversion more popular on the market and can launch the époque of **CMOS**-based **TEGs**.

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### 3.1 Introduction

In the previous chapter, a general view on the energy harvesting techniques has been presented. A brief description of the innovations in the field of thermoelectricity was highlighted (2.5.2.1.4) emphasizing only the novelties at the material level. However, progress in thermoelectricity can be achieved by adopting dual action:

- use of economically and thermoelectrically efficient materials
- thermoelectric generator topology improvement

On the material level **CMOS** materials can thermoelectrically harvest comparable power to conventional thermoelectrics. However, their high  $\kappa$  is precluding their usage in thermoelectricity. Thanks to recent development in the nano- and micro-technology the possibility to alter thermal transport properties with minor impact on electrical properties is technologically feasible. This enables fabrication of harmless, cheap, industrially compatible and reliable thermoelectric devices based on **CMOS** compatible materials.

On the topological level recent innovation relies on the thermoelectric generator topologies in lateral configuration which are enabling the size induced  $\kappa$  reduction. Moreover, the lateral topologies are privileged industrially due to ease of fabrication and packaging. The performance evaluation showed that **CMOS** compatible thermoelectric generators can harvest comparable power level to conventional thermoelectric materials and topologies. However, the performance comparability can be achieved only when the  $\kappa$  reduction is achieved in **CMOS** compatible materials.

The merging of material and topological engineering contribute significantly in commercialization of **CMOS**-compatible thermoelectric devices which may be the ‘Holy Grail’ for popularization of thermoelectricity on the market. This chapter evaluates the performance of **CMOS** compatible materials in thermoelectricity in non-conventional thin-film based **TEGs** topologies.

### 3.2 **CMOS** thermoelectric materials

As previously described, the **CMOS** industry implements the most popular fabrication technique in digital industry (2.5.2.1.4). This method allows manufacturing electron devices massively and cheaply. However, this fabrication technology requires well defined materials based on compatibility and performance criteria. The foundation stones for **CMOS** technology are **Si**, **Ge**, or compounds of them **Si<sub>x</sub>Ge<sub>1-x</sub>** [Burghartz, 2013]. Those materials are offering a satisfactory compromise between the cost and performance. **Si** and **Ge** are the materials offering good electrical properties. However, in the field of thermoelectricity only the **Si<sub>x</sub>Ge<sub>1-x</sub>** is used, for high temperature conversion, owing to its low thermal conductivity ( $\kappa$ ). Both bulk **Si** and bulk **Ge** presents too high  $\kappa$ . Reducing  $\kappa$  in **CMOS** compatible materials will enable:

- cheap,
- massive production and
- harmless and environmentally friendly thermoelectric devices.



Table 3-1 reports the unit price of the minerals frequently used in thermoelectricity. It has to be underlined that in thermoelectricity often (*two or more*) minerals are used. Thus, the cost of the final thermoelectric compound is much higher than the simple addition of two contributing mineral's prices.

**Table 3-1 Reported on market cost of thermoelectric materials**

<i>Material</i>	<i>Cost</i> (\$/kg)	<i>Reference</i>
Si	2.16	
Ge	1 900	
Bi	25.11	<a href="#">[USGS, 2015]</a>
Sb	9.50	
Te	117	
Pb	2.36	

Table 3-2 presents the hazard pictograms for given material. Conventional thermoelectric materials are responsible for numerous environmental and biological threats. On the other hand, materials used in **CMOS** technology are relatively safe in use.

**Table 3-2 Chemical hazard labels corresponding to given material**

<i>Conventional thermoelectrics</i>	<i>CMOS compatible</i>	<i>Reference</i>
<p><b>Bi; Te; Sb; Pb</b></p> 	<p><b>Si; Ge and Si<sub>x</sub>Ge<sub>1-x</sub></b></p> 	<p>Globally Harmonized System of Classification and Labeling of Chemicals</p>

Encouraged by this promising possibility, in the following the focus will be put on the analysis of the electrical and thermal properties of **Si**, **Ge** and **Si<sub>x</sub>Ge<sub>1-x</sub>**.

### 3.2.1 Electrical properties simulations

To evaluate the electrical capabilities of **CMOS** compatible materials in thermoelectricity, analytic models have been established. The model simulates a semiconducting rods (Fig. 3-1) taking into account the impact of local lattice temperature (**T**) and doping concentrations (**N<sub>A</sub>** or **N<sub>D</sub>**) on the electric transport properties.

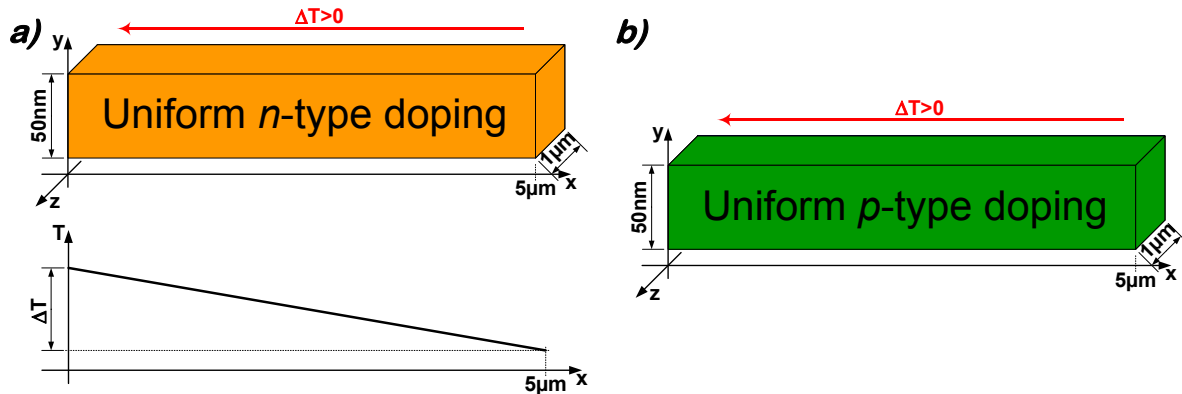


Fig. 3-1 Definition of simulated properties of a semiconducting rod emphasizing dimensions and temperature profile, a) *n*-type doping, b) *p*-type doping

Focusing on the material's electric properties for thermoelectric conversion, the essential importance is put on the electrical conductivity ( $\sigma$ ) and on the thermopower (**S**) while the non-dimensional-figure-of-merit ( $zT$ ) depends on them (see Eq. 2-13). To evaluate the variation of  $\sigma$ , and **S**, realistic calculations of carrier concentrations have to be performed. As mentioned in the previous chapter the considered material parameters are strongly dependent on **N<sub>A</sub>** or **N<sub>D</sub>**, holes (**p**) and electrons (**n**) and intrinsic (**n<sub>i</sub>**) concentrations. The complexity of the model is increased due to dependence of all parameters with the local temperature.

The model assumes a linear temperature profile across the material, defined as follows  $T(x=0)=T_{HOT}$  and  $T(x=5\mu m)=T_{COLD}$  as shown in Fig. 3-1a. The linear temperature distribution can be assumed for small  $\Delta T=T_{HOT}-T_{COLD}$ .  $\kappa$  is temperature dependent making the **T** distribution along the material non-linear. In more precise modelling, the non-linearity of local **T** has to be included in the model.

The mathematical background of the model relies on the assumption that the semiconductor is not degenerated (for definition look 2.5.2.1.3). Basing on this assumption the equilibrium concentrations relationships can be employed [Pierret, 1996] [Sze, 2007]. The equilibrium carriers concentration relationships are based on the Fermi-Dirac distribution function which allows determining the carriers concentrations when the charge neutrality condition is respected.

It has to be noted that all modelled thermal and doping dependent material's parameters responsible for electrical properties are calculated locally following the *x*-axis in the Fig. 3-1. This approach enables modelling the variation of material's parameters as a function of local temperature.

In the following of this section, the comprehensive description of the mathematical background of the model is presented.

## 3.2.1.1 Modelling the band gap

The departure point to determine carrier's concentrations is the calculation of the band gap taking into consideration the thermally and doping induced band gap narrowing. The band gap energy ( $E_G$ ) is dependent on the temperature and the doping concentration. To simulate thermal dependence of the band gap ( $E_{GTherm}$ ), Eq. 3-1 is used [Varshni, 1967]. The temperature is not the sole parameter altering the value of  $E_G$ . When doping is greater than  $10^{18} \text{cm}^{-3}$ , experimental data show that  $E_G$  becomes doping dependent [Slotboom, 1977]. As the doping level increases the valence bands energy is raised and conduction band energy is lowered by approximately the same value ( $\Delta E_{GN}$ ). The doping induced band energy narrowing is analytically described using Eq. 3-2 [Slotboom, 1976]. The final formula for band gap energy which takes into account thermally and doping induced narrowing is normalize by Eq. 3-3.

$$E_{GTherm}(T) = E_G(0) - \frac{\alpha \cdot T^2}{T + \beta} \quad \text{Eq. 3-1}$$

$$\Delta E_{GN}(N_{(A,D)}) = A \cdot \left\{ \ln\left(\frac{N_{(A,D)}}{N_0}\right) + \sqrt{\ln\left(\frac{N_{(A,D)}}{N_0}\right)^2 + C} \right\} \quad \text{Eq. 3-2}$$

$$E_G(T, N_{(A,D)}) = E_{GTherm}(T) - \Delta E_{GN}(N_{(A,D)}) \quad \text{Eq. 3-3}$$

where

- $E_G(0)$  Band gap energy at T=0K (eV)
- $\alpha; \beta$  Fitting parameters defined to obtain the best model's agreement with experiments
- $m_e; m_h$  effective mass for electrons and holes respectively (kg)
- $N_{(A,D)}$  Doping concentration  $N_A$  for acceptor and  $N_D$  for donor respectively
- $A, C, N_0$  Model constants

For  $E_G(T, N_{(A,D)})$  following constant values are used:

**Table 3-3 Band gap narrowing parameters for Silicon and Germanium**

Material	Si	Ge	Reference
$E_G(0)$ [eV]	1.17	0.663	
$\alpha$ [ $K^{-1}$ ]	$4.73 \times 10^{-4}$	$4.774 \times 10^{-4}$	[Grundmann, 2010], [Hennel, 2003], [O'Donnell, 1991], [Pierret, 1987], [Sze, 2007], [Varshni, 1967]
$\beta$ [K]	636	235	
$A$ [V]	$9.0 \times 10^{-3}$		
$N_0$ [ $\text{cm}^{-3}$ ]	$1.0 \times 10^{17}$		[de Graaff, 1986], [de Graaff, 1987], [Klaassen, 1990], [Klaassen, 1992], [Slotboom, 1976], [Silvaco, 2012]
$C$	0.5		

Worth noting is the fact that temperature has bigger influence on  $E_G$  than doping. Fig. 3-2 illustrates the band gap in **Si** and **Ge** considering the above described effects. The band gap exhibits 18% and 33% reduction over a 800K temperature span in **Si** and **Ge**, respectively. While doping impact on  $E_G$  reduces the gap by 10% in **Si** and by 12% in **Ge**. Interestingly, as previously signalled, the  $E_G$  narrowing caused by the doping concentrations  $N_A$  or  $N_D$  is significant only for the doping levels above  $10^{18} \text{cm}^{-3}$ . In Fig. 3-2 doping induced band gap narrowing is visible only when the doping level is  $10^{19} \text{cm}^{-3}$ .

while for  $10^{15}\text{cm}^{-3}$   $E_G$  can be sufficiently modelled considering only the temperature dependent component  $E_{GTherm}$  Eq. 3-1.

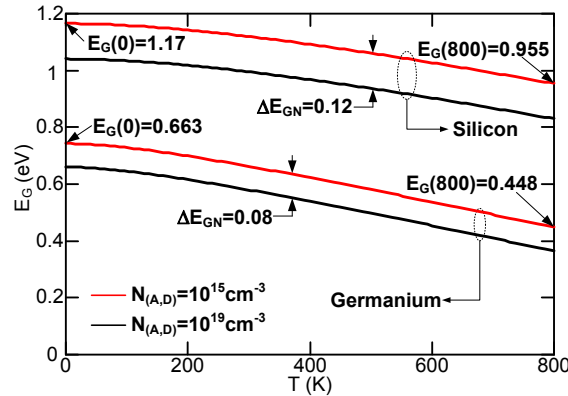


Fig. 3-2 Silicon and Germanium band gap versus temperature. Red line for lightly doped and black line for heavily doped case.

The accurate modeling of  $E_G$  is very important to calculate realistically the carriers concentrations  $p$  and  $n$  and the intrinsic  $n_i$  concentration. The mentioned concentrations are playing key role to evaluate the thermoelectric performance because the electric transport is significantly dependent on them. Moreover, the thermopower is also a function of the carrier concentrations. Thus, the accurate and realistic modelling of the band gap energy is fundamental for realistic modelling of  $\sigma$  and  $S$ .

$E_G$  modelling in  $\text{Si}_x\text{Ge}_{1-x}$  is a much more complicated task, due to a completely different material structure. The interaction between the  $\text{Si}$  and the  $\text{Ge}$  introduces a deformation of the band energies edges making a  $E_G$  model very difficult to construct. The complexity of the model is additionally increased by the presence of mechanical strain in the  $\text{Si}_x\text{Ge}_{1-x}$  caused by the different  $\text{Si}$  and  $\text{Ge}$  lattice constants. Moreover,  $\text{Si}$  and  $\text{Ge}$  are very well reported in the literature compared with  $\text{Si}_x\text{Ge}_{1-x}$ . Mentioned restrictions are listed to present the complexity and the difficulty to build the analytical model for  $\text{Si}_x\text{Ge}_{1-x}$ . Insufficient reported data and analytic models are resulting in the fact that the thermoelectric modelling for  $\text{Si}_x\text{Ge}_{1-x}$  can be completely realized only for  $x=70\%$ . Secondly, lack of temperature dependent modelling of the material parameters is limiting the usage of this model only to temperatures around room temperature. Evaluation of thermoelectric capabilities for  $\text{Si}_x\text{Ge}_{1-x}$  at higher temperatures increases the error.

$\text{Si}_x\text{Ge}_{1-x}$  is the material which properties are depending on the temperature  $T$  and carrier concentrations  $n$  and  $p$  like it is for  $\text{Si}$  and  $\text{Ge}$ . However,  $\text{Si}_x\text{Ge}_{1-x}$  has one more variable influencing all material properties which is the composition  $x$ . Instead of having doping- and temperature-dependent model, for  $\text{Si}_x\text{Ge}_{1-x}$  the model should depend on composition,  $T$  and doping concentration. The  $E_G$  dependence on the composition is depicted in Fig. 3-3a [Braunstein, 1958]. It is visible that the room-temperature  $E_G$  of  $\text{Si}_x\text{Ge}_{1-x}$  is significantly dependent on the  $\text{Si}$  content. For  $\text{Ge}$ -like materials, the  $E_G$  value is close to pure  $\text{Ge}$  and, in contrary, when the material is  $\text{Si}$ -like the  $E_G$  approaches to the  $E_G$  in pure  $\text{Si}$ . The room-temperature  $E_G$  in  $\text{Si}_{70\%}\text{Ge}_{30\%}$  is 0.96eV. As mentioned previously,  $E_G$  in  $\text{Si}_x\text{Ge}_{1-x}$  depends also on the temperature  $T$ . Fig. 3-3b shows the thermally induced band gap bending for different compositions. The closest composition to

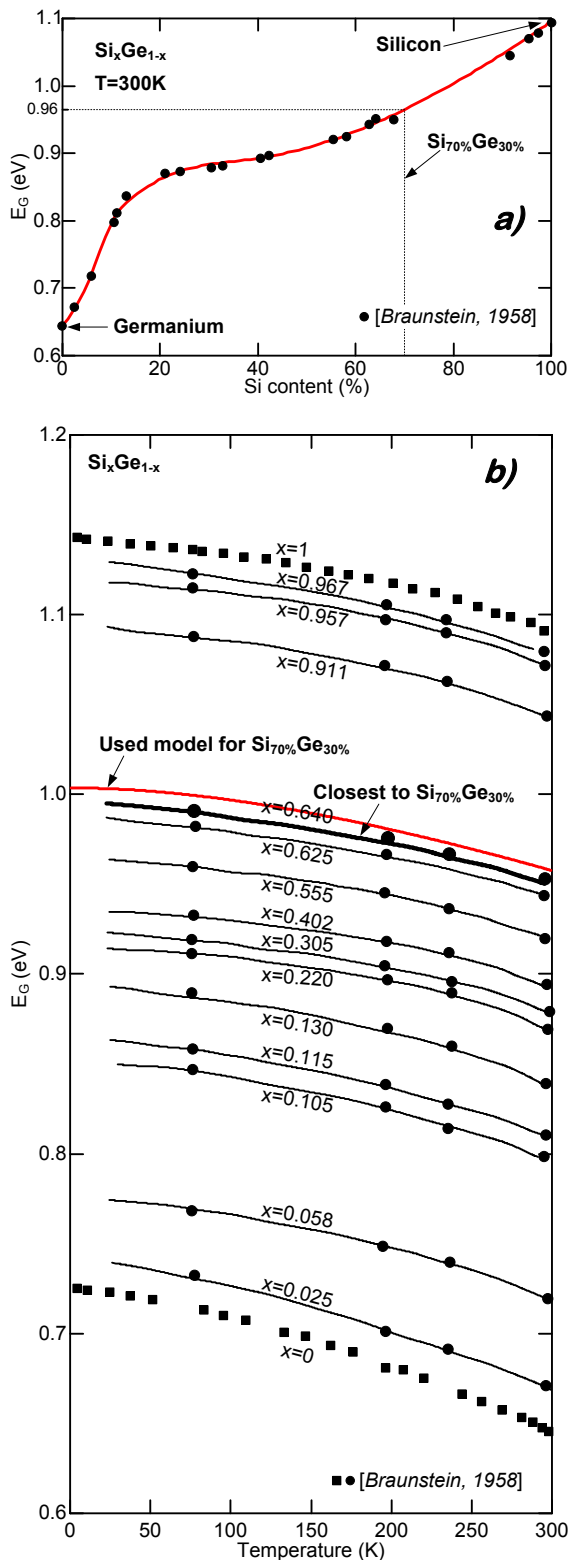


Fig. 3-3 a) Energy band gap at  $T=300\text{K}$  in  $\text{Si}_x\text{Ge}_{1-x}$  for different Silicon contents, b) Temperature dependence of  $E_G$  in  $\text{Si}_x\text{Ge}_{1-x}$  for different  $x$  values

$\text{Si}_{70\%}\text{Ge}_{30\%}$  is highlighted. Fig. 3-3b reveals that  $E_G$  is rising when the  $\text{Si}$  content is increasing. Interestingly, when analyzing the data plotted in Fig. 3-3b leads to the conclusion that the temperature alters  $E_G$  in a comparable way for all reported  $x$  values. As it was already observed for  $\text{Si}$  and  $\text{Ge}$  (compare with Fig. 3-2), the  $E_G$  value is decreasing with increasing temperature for  $\text{Si}_x\text{Ge}_{1-x}$ .

To calculate analytically  $E_G$  in  $\text{Si}_x\text{Ge}_{1-x}$  taking into consideration the local lattice temperature  $T$  and composition  $x$ , Eq. 3-4 is used [Lang, 1985]. The model requires the calculation of the composition dependent variables, following Eq. 3-5 to Eq. 3-7. It has to be underlined that the model presented in Eq. 3-4 fits only with  $\text{Si}_x\text{Ge}_{1-x}$  for  $0.65 \leq x < 0.755$ . For compositions beyond this range a different  $E_G(x)$  formula has to be used. The comparison of the used model with the experimental data is given in Fig. 3-3b in red continuous line. It can be remarked that the model is calculating the  $E_G$  with good precision. The composition and the temperature induced impact on  $E_G$  is reflected in analytically calculated  $E_G$ . However, the model described by Eq. 3-4 is independent on doping concentration in contrast to the band gap narrowing models for  $\text{Si}$  and  $\text{Ge}$  described previously (see Eq. 3-2). Thus, when modelling thermoelectric performance of  $\text{Si}_x\text{Ge}_{1-x}$ ,  $E_G$  is independent on the doping concentration. Knowing that  $E_G$  in  $\text{Si}_x\text{Ge}_{1-x}$  is limited between the  $E_G$  for pure  $\text{Ge}$  and  $\text{Si}$  and the thermally induced  $E_G$  reduction has same behaviour like in  $\text{Ge}$  and  $\text{Si}$  it can be assumed here that doping induced band gap narrowing in  $\text{Si}_x\text{Ge}_{1-x}$  is comprised between 10% for high  $\text{Si}$ -like  $\text{Si}_x\text{Ge}_{1-x}$  and 12% for  $\text{Ge}$ -like  $\text{Si}_x\text{Ge}_{1-x}$ .

$$E_G(T, x) = E_G(x) + E_{G\alpha}(x) \cdot \left[ \frac{300^2}{300 + E_{G\beta}(x)} - \frac{T^2}{T + E_{G\beta}(x)} \right] \quad \text{Eq. 3-4}$$

with:

$$E_G(x) = 0.945 - 0.714 \cdot (0.755 - x) \text{ and } 0.65 \leq x < 0.755 \quad \text{Eq. 3-5}$$

$$E_{G\alpha}(x) = [4.73 + 0.04 \cdot (1 - x)] \times 10^{-4} \quad \text{Eq. 3-6}$$

$$E_{G\beta}(x) = 636 - 401 \cdot (1 - x) \quad \text{Eq. 3-7}$$

### 3.2.1.1 Modelling carrier concentrations

The carrier concentrations have a significant impact on the electronic transport properties and on the Seebeck coefficient. Thus, accurate modelling of the carrier concentrations has high importance when evaluating the performance of thermo-generator while it indirectly alters the numerator in the  $\mathbf{zT}$  formula (see Eq. 2-13). In the following, the modelling of the carrier concentrations will be presented.

The concentrations modelling departure point is the calculation of effective density of states in conduction  $\mathbf{N}_C$  and valence  $\mathbf{N}_V$  bands Eq. 3-8. Afterwards,  $\mathbf{N}_C$ ,  $\mathbf{N}_V$  and  $\mathbf{E}_G$  Eq. 3-3 are used to calculate the intrinsic concentration  $\mathbf{n}_i$  Eq. 3-9. Finally,  $\mathbf{E}_G$  Eq. 3-3,  $\mathbf{N}_{(C,V)}$  Eq. 3-8,  $\mathbf{n}_i$  Eq. 3-9 are directly or indirectly used to calculate the hole  $\mathbf{p}$  and electron  $\mathbf{n}$  concentrations following Eq. 3-10 or Eq. 3-11. The  $\mathbf{N}_A$  and  $\mathbf{N}_D$  variables are acceptor ( $p$ -type) and donor ( $n$ -type) doping concentrations, respectively. When considering  $n$ -type doped material, Eq. 3-10 is used because  $\mathbf{n}$  are majority carriers and  $\mathbf{p}$  minority carriers. Oppositely, in  $p$ -type doping minor are the electrons  $\mathbf{n}$  and major are the holes  $\mathbf{p}$  and Eq. 3-11 is used.

$$\begin{cases} N_C(T) = 2 \cdot \left( \frac{2 \cdot \pi \cdot k_B \cdot T \cdot m_e}{h^2} \right)^{3/2} \\ N_V(T) = 2 \cdot \left( \frac{2 \cdot \pi \cdot k_B \cdot T \cdot m_h}{h^2} \right)^{3/2} \end{cases} \quad \text{Eq. 3-8}$$

$$n_i(T, N_{(A,D)}) = \sqrt{N_C(T) \cdot N_V(T)} \cdot e^{-\frac{E_G(T, N_{(A,D)})}{2k_B T}} \quad \text{Eq. 3-9}$$

$$\begin{cases} n(T, N_D) = \frac{N_D}{2} + \sqrt{\frac{N_D^2}{4} + n_i^2(T)} \\ p(T) = \frac{n_i^2(T)}{n(T)} \end{cases} \quad \text{Eq. 3-10}$$

$$\begin{cases} p(T, N_A) = \frac{N_A}{2} + \sqrt{\frac{N_A^2}{4} + n_i^2(T)} \\ n(T) = \frac{n_i^2(T)}{p(T)} \end{cases} \quad \text{Eq. 3-11}$$



where

$N_A; N_D$	Acceptor and donor concentrations respectively ( $\text{cm}^{-3}$ )
$N_C; N_V$	Density of states in conduction and valence bands respectively ( $\text{cm}^{-3}$ )
$m_e; m_h$	effective mass for electrons and holes respectively (kg)
$E_G$	Energy band gap (eV)
$k_B$	Boltzmann constant $k_B=1.3806 \times 10^{-23} (\text{J/K})=8.6173 \times 10^{-5} (\text{eV/K})$
$h$	Planck's constant $h=6.6260 \times 10^{-34} (\text{J}\cdot\text{s})$
$n_i$	Intrinsic concentration ( $\text{cm}^{-3}$ )
$T$	Temperature (K)
$q$	Magnitude of electronic charge $q=1.6021 \times 10^{-19} (\text{C})$
$n$	Electron concentration ( $\text{cm}^{-3}$ )
$p$	Hole concentration ( $\text{cm}^{-3}$ )

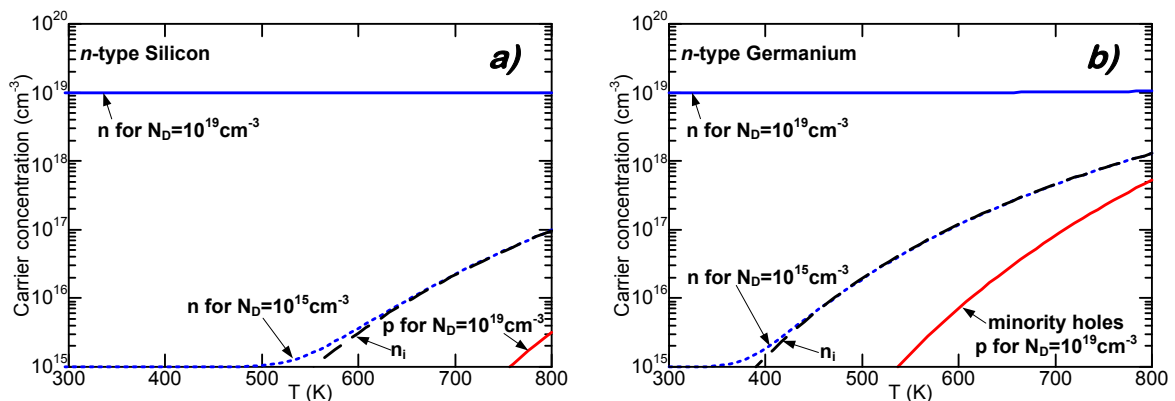
For effective electrons and holes masses the following values are used:

**Table 3-4 Effective carrier mass in Silicon and Germanium used in calculations**

Effective mass	Silicon	Germanium	Reference
Electrons ( $m_e$ )	$1.08 \cdot m_0$	$0.55 \cdot m_0$	<a href="#">[Madelung, 2004]</a>
Holes ( $m_h$ )	$0.81 \cdot m_0$	$0.37 \cdot m_0$	

$m_0=9.10938215 \times 10^{-31}$  (kg) states for the free electron rest mass

The carrier concentrations  $n$ ,  $p$  in Eq. 3-10 and Eq. 3-11 exhibit dual dependence firstly on the temperature and secondly on the doping level. This is visible on Fig. 3-4 where  $n$  and  $p$  are plotted against local temperature  $T$  for  $n$ -doped **Si** and **Ge** for two doping levels  $10^{15} \text{cm}^{-3}$  and  $10^{19} \text{cm}^{-3}$ . The majority carrier concentration (blue line) is exhibiting different behaviour against temperature for light and heavy doping. For doping level of  $10^{19} \text{cm}^{-3}$  the majority carrier concentration  $n$  is almost constant over temperature. When considering the  $n$  concentration for  $N_D=10^{15} \text{cm}^{-3}$ , it can be observed that the concentration remains constant and equal to  $N_D$  until a certain temperature above which  $n$  starts to rise. The rising of  $n$  follows the intrinsic concentration  $n_i$ . In other words, starting from certain temperature the carrier concentrations are governed by the  $T$  and not by the doping level. For  $N_D=10^{15} \text{cm}^{-3}$  **Si** becomes intrinsic when  $T$  is higher than  $\sim 550\text{K}$  while **Ge** marks this transition for temperature  $\sim 400\text{K}$ . When a semiconductor is intrinsic, all concentrations are equal to  $n_i$  and there are no major or minor carriers ( $n=p=n_i$ ).



**Fig. 3-4** Carrier and intrinsic (black dashed line) concentrations against temperature, a) N-type Silicon carriers concentration (blue line) for  $N_D=10^{19} \text{cm}^{-3}$  and  $N_D=10^{15} \text{cm}^{-3}$  (blue dotted line), hole concentration (red line), b) N-type Germanium's carriers concentration (blue line) for  $N_D=10^{19} \text{cm}^{-3}$  and  $N_D=10^{15} \text{cm}^{-3}$  (blue dotted line), hole concentration (red line)

Fig. 3-4 also depicts the minority carrier concentration (*red line*) for heavy donor doping  $N_D=10^{19}\text{cm}^{-3}$ . Firstly, it can be observed that the minority carrier concentration is dramatically smaller than  $N_D$ . Secondly, the temperature affects the minority carrier concentration in a more significant way compared with the majority carriers. Same observations can be made when changing the doping character from *n*-type to *p*-type, however in such case majority carrier is represented by  $p$  and minor carrier concentration is  $n$ . Consideration of the influence of minority carriers on the thermoelectric properties of the material is pointless. The contribution of minority carriers in the electric transport and the Seebeck coefficient is negligibly small. Thus to simplify and clarify the model, in the following only majority carriers for a given material will be taken into consideration.

Focusing now on the carrier concentration modelling in  $\text{Si}_x\text{Ge}_{1-x}$ , it has to be noted that the concentration model is much more simplified compared with modelling for  $\text{Si}$  or  $\text{Ge}$ . The big difficulty in the calculations is the determination of the effective carrier masses due to deformation of the conduction and the valence bands. Thus, to calculate the effective densities of states simplified formulas are used [Silvaco, 2012]:

$$\begin{cases} N_C(x) = 2.8 \times 10^{19} - 1.76 \times 10^{19} \cdot (1-x) \\ N_V(x) = 1.04 \times 10^{19} - 4.4 \times 10^{18} \cdot (1-x) \end{cases} \quad \text{Eq. 3-12}$$

When investigating Eq. 3-12 it can be observed that the effective densities of states in conduction  $N_C$  and valence  $N_V$  bands are taken independent on temperature.

Eq. 3-4 for  $E_C(T,x)$  with Eq. 3-12 for  $N_C(x)$  and  $N_V(x)$  enables the calculation of carrier concentrations  $n_i$ ,  $n$  and  $p$  which is done following the same relationships used for  $\text{Si}$  and  $\text{Ge}$  Eq. 3-9, Eq. 3-10 and Eq. 3-11. The illustration of  $n_i$ ,  $n$  and  $p$  variations with temperature are presented in Fig. 3-5:

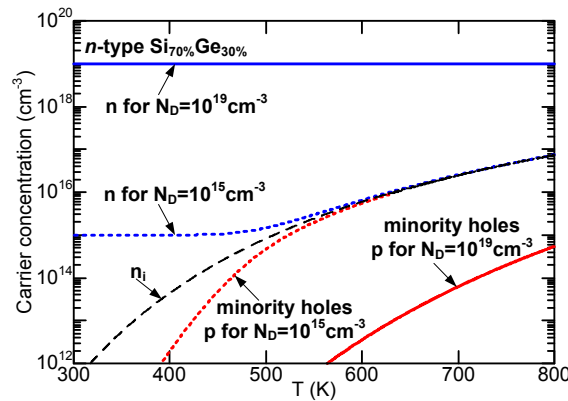


Fig. 3-5 Carrier and intrinsic concentrations (*black dashed line*) for *n*-type  $\text{Si}_{70\%}\text{Ge}_{30\%}$  doped to the level of  $10^{19}\text{cm}^{-3}$  (*continuous lines*) and  $10^{15}\text{cm}^{-3}$  (*dotted lines*)

Fig. 3-5 shows the temperature dependence of the carrier concentrations for *n*-type  $\text{Si}_{70\%}\text{Ge}_{30\%}$  heavily  $10^{19}\text{cm}^{-3}$  and lightly  $10^{15}\text{cm}^{-3}$  doped. Comparing Fig. 3-5 with Fig. 3-4 it can be observed that the shape and the temperature impact on the concentrations are comparable with  $\text{Si}$  or  $\text{Ge}$ . It is an encouraging observation when realizing that  $\text{Si}_{70\%}\text{Ge}_{30\%}$  is constructed from pure  $\text{Si}$  and  $\text{Ge}$  which concentrations are presenting more or less comparable behaviour for different temperatures. However, when studying lightly doped  $\text{Si}_{70\%}\text{Ge}_{30\%}$ , it is observable that the material starts to act as intrinsic ( $n=p=n_i$ ) for temperatures around  $T_i \approx 550\text{K}$  which is higher than for pure  $\text{Ge}$  ( $T_i \approx 400\text{K}$ ) and slightly less than for pure  $\text{Si}$  ( $T_i \approx 550\text{K}$ ). This observation leads to the conclusion that the properties of  $\text{Si}_{70\%}\text{Ge}_{30\%}$  are comprised between two limits defined by pure  $\text{Si}$  and pure  $\text{Ge}$ . The

domination of **Si** in the composition pushes the overall properties of **Si<sub>70%</sub>Ge<sub>30%</sub>** closer towards the **Si** limit.

The calculation of **n**, **p** opens possibility for modelling of **σ** and **S** which will be described in the following.

### 3.2.1.2 Electrical conductivity

**σ** is analytically calculated following Eq. 2-17. Essentially, **σ** depends on the carrier concentrations and carrier mobilities **μ<sub>n</sub>** and **μ<sub>p</sub>**, all being dependent on the temperature and the doping level. After calculating realistically the carrier concentration, to simulate **σ** the carrier motilities have to be correctly and precisely modelled. In the literature, there are many different analytical models which are approximating experimental data. However, in this case the model which depends on doping concentrations **N<sub>A</sub>** or **N<sub>D</sub>** and local lattice temperature **T** has to be chosen. Thus, despite the numerous publications and experiments concerning **Si** and **Ge**, the construction of temperature- and doping-dependent model is very difficult to achieve. The chosen carrier mobility model for **Si** is the Arora model [Arora, 1982] Eq. 3-13:

$$\left\{ \begin{array}{l} \mu_n(N_D, T) = \mu_{\min} \cdot \left(\frac{T}{300}\right)^\alpha + \frac{\mu_{\max} \cdot \left(\frac{T}{300}\right)^\beta}{1 + \frac{N_D}{N_{ref} \cdot \left(\frac{T}{300}\right)^\gamma}} \\ \mu_p(N_A, T) = \mu_{\min} \cdot \left(\frac{T}{300}\right)^\alpha + \frac{\mu_{\max} \cdot \left(\frac{T}{300}\right)^\beta}{1 + \frac{N_A}{N_{ref} \cdot \left(\frac{T}{300}\right)^\gamma}} \end{array} \right. \quad \text{Eq. 3-13}$$

In Eq. 3-13 following parameters values are used:

**Table 3-5 Parameters values for modelling Silicon's carrier mobilities [Arora, 1982] and [Silvaco, 2012]**

Material	Target Eq. 3-13	$\mu_{\max}$ ( $\text{cm}^2/\text{V/s}$ )	$\mu_{\min}$ ( $\text{cm}^2/\text{V/s}$ )	$N_{ref}$ ( $\text{cm}^{-3}$ )	$\alpha$	$\beta$	$\gamma$	Reference
n-type Si	$\mu_n(N_D, T)$	88	1252	$1.432 \times 10^{17}$	-0.57	-2.33	2.546	[Arora, 1982], [Silvaco, 2012]
p-type Si	$\mu_p(N_A, T)$	54.3	407	$2.67 \times 10^{17}$				

**μ<sub>n</sub>** and **μ<sub>p</sub>** in **Ge** follow analytic low-field mobility model [Thomas, 1967] and [Selberherr, 1984] Eq. 3-14:

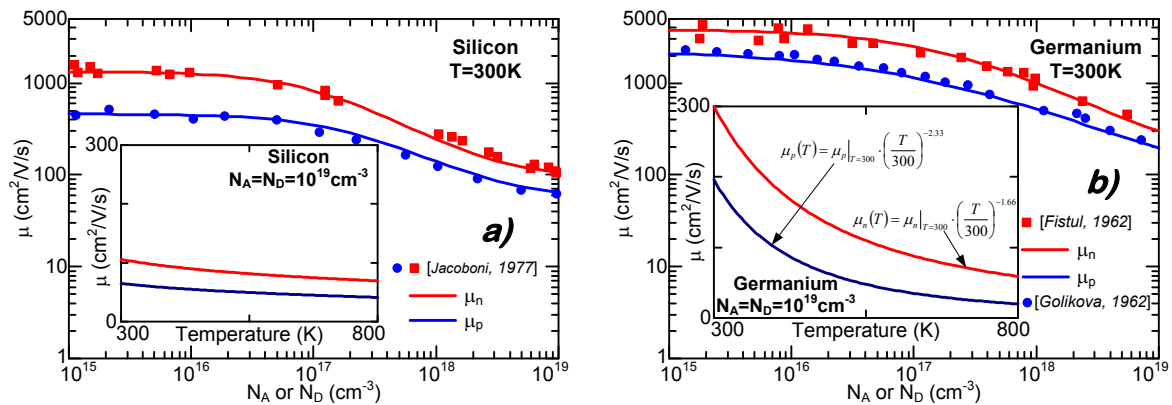
$$\left\{ \begin{array}{l} \mu_n(N_D, T) = \left(\frac{T}{300}\right)^{-1.66} \cdot \left[ \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left[\frac{N_D}{N_{ref}}\right]^\alpha} \right] \\ \mu_p(N_A, T) = \left(\frac{T}{300}\right)^{-2.33} \cdot \left[ \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left[\frac{N_A}{N_{ref}}\right]^\alpha} \right] \end{array} \right. \quad \text{Eq. 3-14}$$

In Eq. 3-14 following parameters values are used:

**Table 3-6 Parameters values for analytic model of Germanium's carrier mobilities**

Material	Target Eq. 3-14	$\mu_{max}$ ( $cm^2/V/s$ )	$\mu_{min}$ ( $cm^2/V/s$ )	$N_{ref}$ ( $cm^{-3}$ )	$\alpha$	Reference
n-type Ge	$\mu_n(N_D, T)$	3850	100±20	$2.16 \times 10^{17}$	0.75	[Fistul, 1962], [Fistul, 1964]
p-type Ge	$\mu_p(N_A, T)$	2250	40±5	$1.00 \times 10^{17}$	0.56	[Golikova, 1962], [Trumbore, 1958]

Eq. 3-13 and Eq. 3-14 are graphically presented on Fig. 3-6.  $\mu_n$  and  $\mu_p$  for **Si** and **Ge** are plotted against the doping concentration and against local lattice temperature  $T$  (*insert plot*). For both considered materials the precision of the model is evaluated using experimental data. For **Si** the measurement data are from [Jacoboni, 1977] while for **Ge** the data are retrieved from [Fistul, 1962] for n-type **Ge** and from [Golikova, 1962] for p-type **Ge**.



**Fig. 3-6** Holes (blue line) and electrons (red line) mobilities versus doping concentration, insert plot shows mobility versus temperature for  $N_A=N_D=10^{19}cm^{-3}$  for a) Silicon experimental data after [Jacoboni, 1977] and b) Germanium experimental data after  $\mu_n$  after [Fistul, 1962]  $\mu_p$  after [Golikova, 1962]

The first observation arising from Fig. 3-6 is that the carrier mobility in **Ge** significantly outperforms the mobility in **Si**. This explains the superiority of electrical conductivity  $\sigma$  in **Ge** over **Si** (see Fig. 2-40). Secondly, studying Fig. 3-6 it can be noticed that the carrier mobility is decreasing for rising doping concentrations  $N_A$  or  $N_D$ . Such behaviour is caused by rising carrier density for increasing doping concentration, the carriers are becoming more and more scattered by the doping atoms inside the material. Thirdly,  $\mu_n$  and  $\mu_p$  in **Ge** and **Si** are both temperature dependent and this dependency is depicted in insert plot in Fig. 3-6. For both materials the mobilities are decreasing with a rising temperature. This inverse relationship between the mobility and the temperature can be explained by the overall increase of carriers scattering with increasing temperature. Due to the rising quantity of carrier-to-carrier collisions, carriers have lower mobilities. However, it is observable that the mobilities in **Ge** are more temperature dependent than in **Si**. This is the result of lower hole and electron effective masses (see Table 3-4) in **Ge** than in **Si**. Carriers with low mass are easily thermally excited and prone to scattering. As previously explained the carrier's vibrations have reducing influence on the carrier mobilities.

Focusing now on the mobilities in **Si<sub>x</sub>Ge<sub>1-x</sub>**, it has to be remarked that the mobilities are composition- temperature- and doping-dependent. However, as previously signalled the

lack of analytical modelling for  $\text{Si}_x\text{Ge}_{1-x}$  is significantly increasing the difficulty of the modelling. According to [Slack, 1991] the temperature- and composition-dependent mobility model follows the Eq. 3-15.

$$\mu_{n,p}^{-1}(x, T) = \mu_0^{-1} + \mu_g^{-1} \cdot \left(\frac{T}{300}\right)^e + \mu_a^{-1} \cdot 4x \cdot (1-x) \cdot \left(\frac{T}{300}\right)^e \quad \text{Eq. 3-15}$$

The model variables are experimentally determined following [Dismukes, 1964] and are listed in Table 3-7. Eq. 3-15 presents the temperature- and composition-dependent approximation of electron and holes mobilities, however the model does not take directly into account the impact of the doping concentration on the carrier mobilities. The doping dependence is introduced indirectly by the variable  $\mu_0$  which does not depend on the composition  $x$  nor on the temperature  $T$ .  $\mu_g$  is the mobility component which is temperature-dependent while  $\mu_a$  is the composition-dependent contribution.

Table 3-7 Measurement of mobility in  $\text{Si}_x\text{Ge}_{1-x}$  [Dismukes, 1964]

Material	$x$	$\mu_0$ ( $\text{cm}^2/\text{V/s}$ )	$\mu_a$ ( $\text{cm}^2/\text{V/s}$ )	$\mu_g$ ( $\text{cm}^2/\text{V/s}$ )	$e^a)$	$\epsilon^b)$	Reference
n-type $\text{Si}_x\text{Ge}_{1-x}$	28%	77.2	160	125	-1.2	0.8	[Dismukes, 1964]
p-type $\text{Si}_x\text{Ge}_{1-x}$	29.8%	139		143	-1.314		

a) following [Slack, 1991]

b) after [Glicksman, 1958]

The illustration of the model defined by Eq. 3-15 is depicted in Fig. 3-7. Fig. 3-7 shows that the carrier mobilities in  $\text{Si}_x\text{Ge}_{1-x}$  for  $\text{Si}$ -like compositions have more or less the same behaviour for different doping concentrations Fig. 3-7a and temperatures Fig. 3-7b.  $\mu_n$  and  $\mu_p$  are both decreasing when  $N_A$  or  $N_D$  increase, which is depicted in Fig. 3-7a. Same impact on mobility is occurring in pure  $\text{Si}$  Fig. 3-6a and  $\text{Ge}$  Fig. 3-6b. However, the mobilities values are significantly lower for  $\text{Si}_{70\%}\text{Ge}_{30\%}$  than in  $\text{Si}$  and  $\text{Ge}$ . Such situation can be explained by different lattice constants of  $\text{Ge}$  and  $\text{Si}$ , joining together  $\text{Si}$  and  $\text{Ge}$  is creating scattering centres at the junction layer thus, the carrier mobility is significantly lower. Focusing on the temperature impact on the mobilities Fig. 3-7b it can be observed that the mobility is inversely proportional to the temperature as it was revealed for  $\text{Ge}$  or  $\text{Si}$ . But the temperature impact is less significant than in pure  $\text{Ge}$  or pure  $\text{Si}$ .

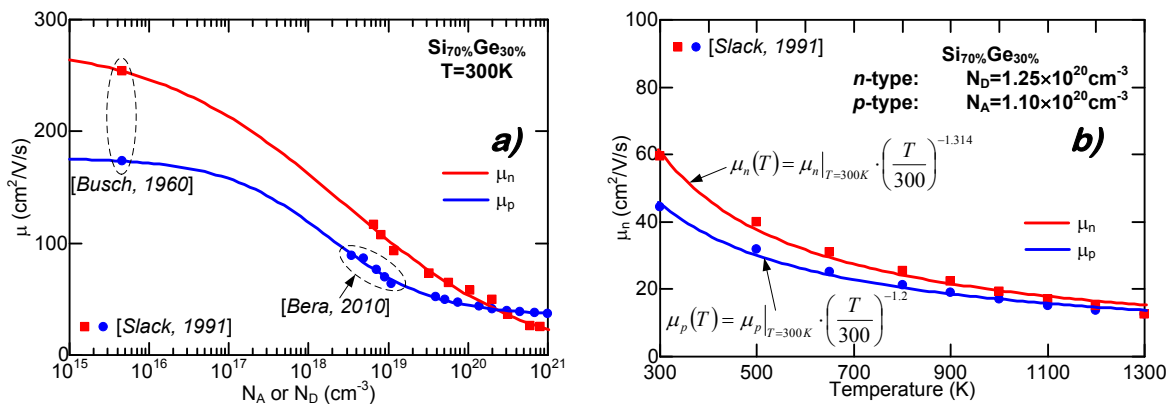


Fig. 3-7 The mobility in  $\text{Si}_{70\%}\text{Ge}_{30\%}$  a) the room-temperature electron and hole mobility versus doping concentration experimental data after [Bera, 2010], [Busch, 1960] and [Slack, 1991], b) electron and hole mobility versus temperature for fixed doping concentration [Slack, 1991]

Eq. 3-15 is describing the mobility in  $\text{Si}_x\text{Ge}_{1-x}$  alloys depending on the temperature, doping and composition  $x$ . When we investigate the mobilities in **Si** Fig. 3-6a and **Ge** Fig. 3-6b it can be remarked that both of those materials are exhibiting significantly different mobilities levels with higher mobility in **Ge**. This observation leads intuitively to conclusion that in  $\text{Si}_x\text{Ge}_{1-x}$  the mobility can have **Ge**-like or **Si**-like values depending on the  $x$ . The mobility in  $\text{Si}_x\text{Ge}_{1-x}$  for different **Si** contents was measured by [Amith, 1965], [Busch, 1960] and [Glicksman, 1958], the results of their experimental work are depicted in Fig. 3-8:

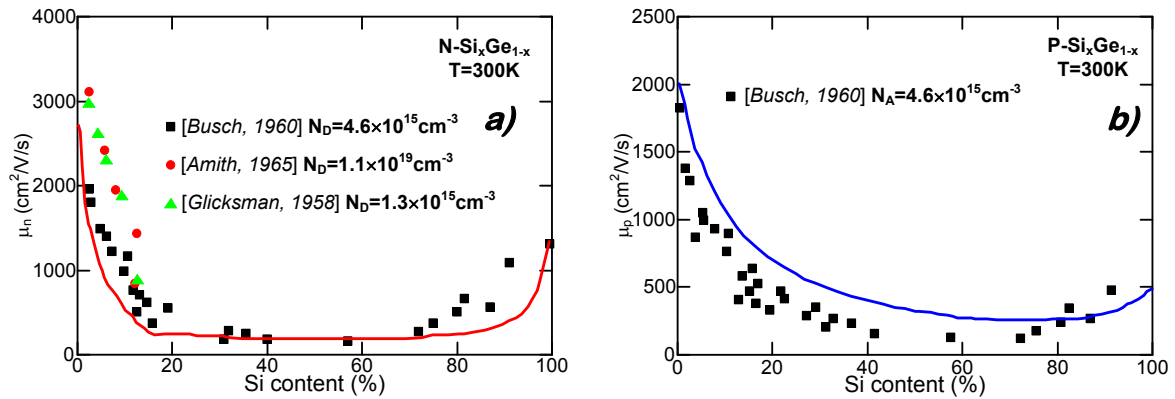


Fig. 3-8 Room-temperature mobility versus Si-content in  $\text{Si}_x\text{Ge}_{1-x}$  in a) *n*-type  $\text{Si}_x\text{Ge}_{1-x}$  for different doping concentrations, b) lightly doped *p*-type  $\text{Si}_x\text{Ge}_{1-x}$

Fig. 3-8 shows that the alloy composition has a significant impact on the carrier mobility. Both  $\mu_n$  and  $\mu_p$  are presenting **Ge**-like high mobilities when **Si**-content is lower than 20%. For increasing **Si**-content the mobility is stabilised and when the **Si**-content is higher than ~80% the  $\mu_n$  and  $\mu_p$  are increasing to attain **Si**-like mobility. Classifying the parameters regarding their influence on the mobility, it can be noted that the composition  $x$  influences the most the mobility, afterwards the doping concentration while temperature has the least impact. Thus, the correct definition of  $x$  and  $N_A$  or  $N_D$  is much more important than the precise determination of temperature difference across the material.

The doping and temperature dependent mobility and carrier concentration modelling enables the accurate simulation of the electrical conductivity  $\sigma$  in **Si**, **Ge** and  $\text{Si}_x\text{Ge}_{1-x}$  following Eq. 2-17.  $\sigma$  is one of the key material parameters influencing the thermoelectric capabilities of the material according to the formula of  $zT$  Eq. 2-13. The room temperature  $\sigma$  for **Si** and **Ge** was presented in Fig. 2-40. To compare the electric transport properties of **CMOS** compatible materials with conventional thermoelectric materials represented by  $\text{Bi}_2\text{Te}_3$ , Fig. 3-9 is given. In light of previously described electrical transport requirements for good thermoelectric material (see 2.5.2.1.1) when studying Fig. 3-9 it can be noted that both **Si** and **Ge** are competitive comparing to  $\text{Bi}_2\text{Te}_3$ .

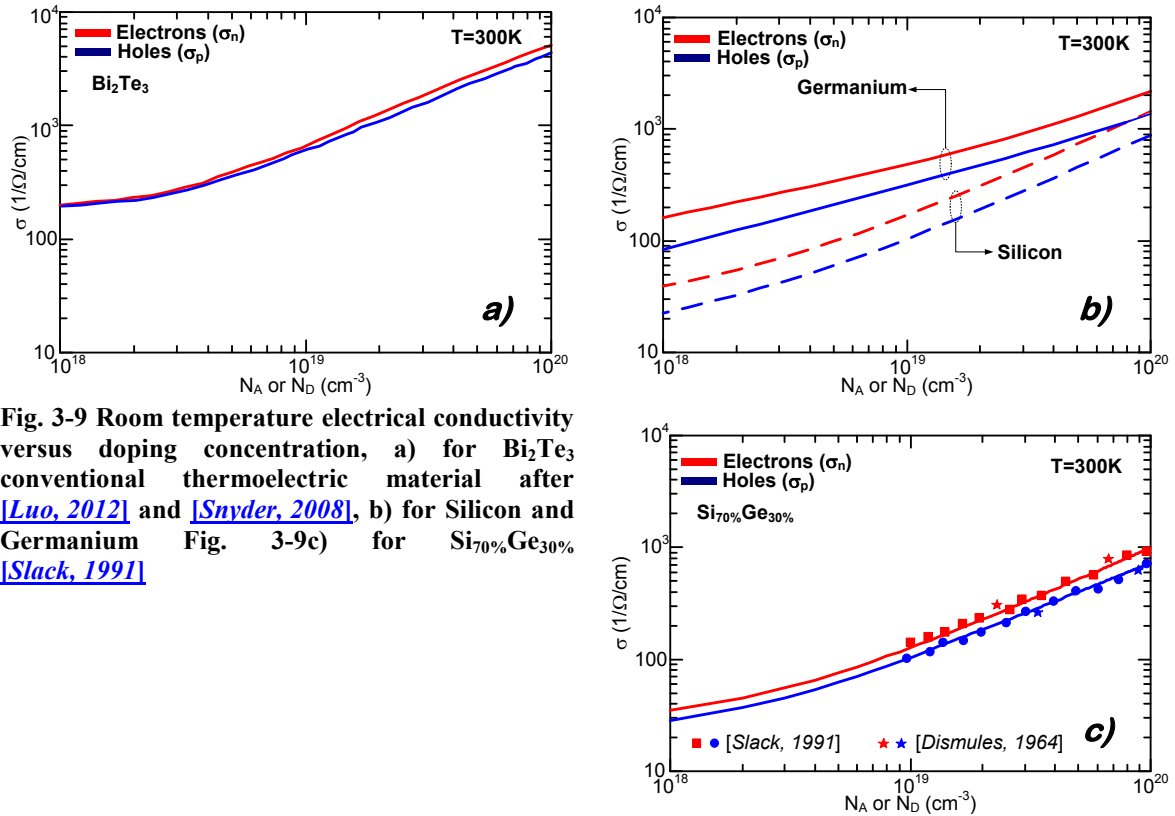


Fig. 3-9 Room temperature electrical conductivity versus doping concentration, a) for  $\text{Bi}_2\text{Te}_3$  conventional thermoelectric material after [Luo, 2012] and [Snyder, 2008], b) for Silicon and Germanium Fig. 3-9c) for  $\text{Si}_{70\%}\text{Ge}_{30\%}$  [Slack, 1991]

From Fig. 3-9, it can be remarked that the  $\text{Bi}_2\text{Te}_3$  electrical conductivity is slightly higher [Luo, 2012] and [Snyder, 2008] than for  $\text{Si}$  and  $\text{Ge}$  [Pierret, 1996]. However, the difference in  $\sigma$  values for compared materials is not drastic. For all materials,  $\sigma$  remains in the comparable order of magnitude. However, when focusing on  $\sigma$  for  $\text{Si}_{70\%}\text{Ge}_{30\%}$  Fig. 3-9c it is worth noting that the level of the electrical conductivity is lower than for pure  $\text{Si}$  or  $\text{Ge}$ . The explanation of this situation was already delivered when comparing the mobilities.  $\sigma$  for different doping concentrations in  $\text{Si}_{70\%}\text{Ge}_{30\%}$  has more  $\text{Si}$ -like shape which is due to dominant  $\text{Si}$  composition in the alloy. Despite slightly lower  $\sigma$  in  $\text{CMOS}$  compatible materials, the material cost and the possibility to use the industrial fabrication techniques must not be omitted.

### 3.2.1.3 Seebeck coefficient

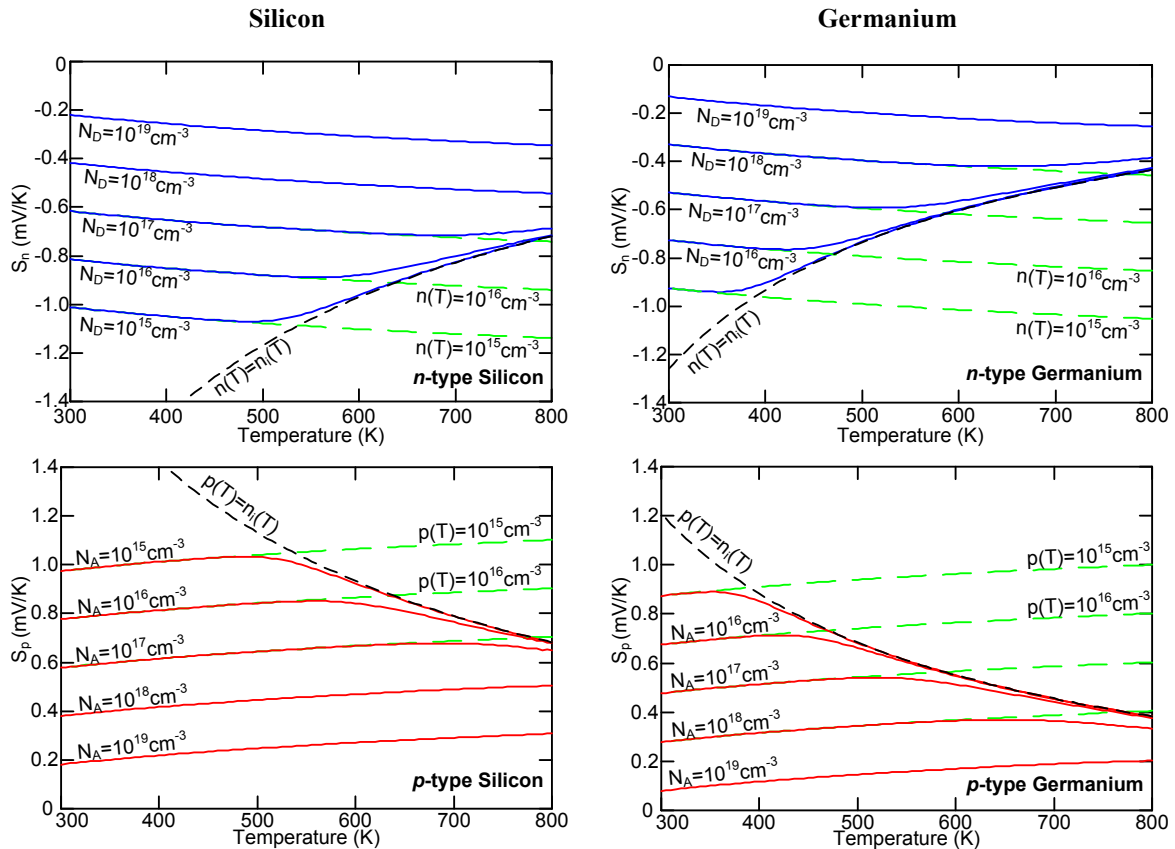
The Seebeck coefficient or thermopower ( $\mathbf{S}$ ) defines the force of the Seebeck effect which occurs in the given material.  $\mathbf{S}$  is expressed in Volt per Kelvin (V/K). The physics and meaning of this effect was briefly described in previous chapter (see 2.5.2.1.3). In this section, the thermopower in  $\text{CMOS}$  compatible material will be investigated and benchmarked with the conventional thermoelectric material.

The thermopower  $\mathbf{S}$  is defined using Eq. 2-26 and it is positive for  $p$ -type doping and negative for  $n$ -type doping. In most cases, the coefficients  $P_{\mu p}$  and  $P_{\mu n}$  are fixed to -1 which simplifies the Eq. 2-26 to the following form:

$$\begin{cases} S_n(T, N_D) = -\frac{k_B}{q} \cdot \left[ \frac{3}{2} + \ln\left(\frac{N_C(T)}{n(T, N_D)}\right) \right] \\ S_p(T, N_A) = \frac{k_B}{q} \cdot \left[ \frac{3}{2} + \ln\left(\frac{N_V(T)}{p(T, N_A)}\right) \right] \end{cases} \quad \text{Eq. 3-16}$$

Eq. 3-16 explains the inversely proportional behaviour of  $S_n$  and  $S_p$  over the carrier concentration. In the natural logarithm, the numerator (*effective density of states in conduction  $N_C$  and valence  $N_V$  Eq. 3-8*) is independent of doping and carrier concentrations, while the denominator (*hole  $p$  or electron  $n$  concentration Eq. 3-10 or Eq. 3-11*) depends on doping concentration. Thus, for lightly doped semiconductors this natural logarithm has higher values than for heavy doping.

Including the equations from Eq. 3-8 to Eq. 3-11 into the calculations of the thermopower Eq. 3-16 for **Si** and **Ge** enables the calculation of  $S_n$  and  $S_p$  with respect to the local lattice temperature and the doping concentration  $N_A$  or  $N_D$ . Fig. 3-10 presents the Seebeck coefficient in **Si** and **Ge** for different doping levels:



**Fig. 3-10** Thermopower in Si and Ge versus temperature for different doping concentrations. *Blue continuous line for n-type doping. Red continuous line for p-type doping. Green dashed line assuming carrier and doping concentrations equality and temperature independence. Black dashed line thermopower in intrinsic semiconductor.*

Fig. 3-10 graphically illustrates Eq. 3-16 taking into account the local lattice temperature  $T$  impact on the carrier concentrations  $p(T)$  and  $n(T)$ , effective densities of states  $N_C(T)$  and  $N_V(T)$ . Red continuous lines are presenting  $p$ -type thermopower  $S_p$  while blue continuous lines are showing the  $n$ -type thermopower  $S_n$ . As previously mentioned both  $S_p$  and  $S_n$  are exhibiting higher absolute values for lightly doped materials while

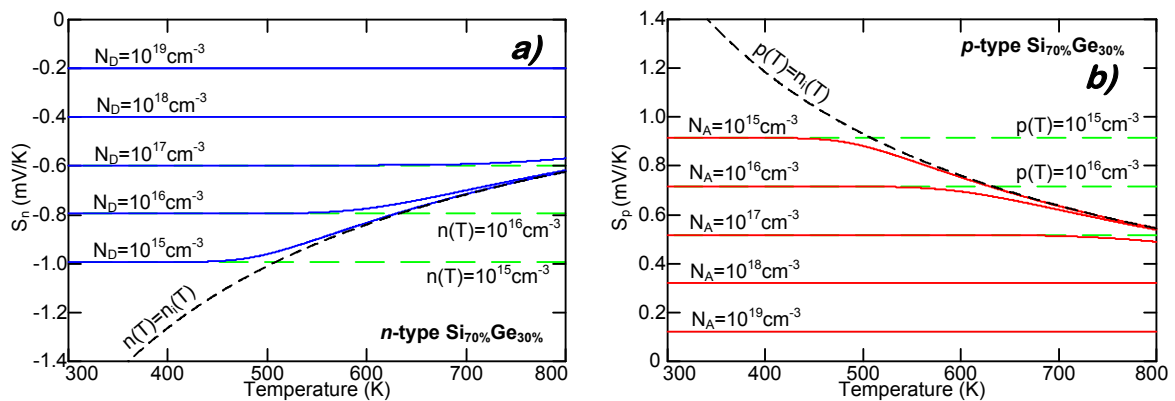


heavy doping results in small absolute value of  $S_p$  and  $S_n$ . For both materials and doping types the thermopower are presenting comparable behaviour. With rising temperature the absolute value of  $S_p$  and  $S_n$  is rising till a certain  $T$  above which the thermopower is decreasing, this is especially visible for lightly doped materials. This phenomenon can be explained by the fact that for lower temperatures  $S_p$  and  $S_n$  are dominated by the value of  $N_V$  and  $N_C$  which are exhibiting  $T^{3/2}$  dependence over the temperature. When temperature rises the carrier concentrations  $p$  and  $n$  can be dominated by intrinsic carrier concentration ( $n_i$ ) which is rising with temperature. When  $n_i$  starts to be higher than doping concentrations  $N_A$  or  $N_D$  the thermopower absolute value decreases. In this regime the semiconductor can be considered as intrinsic and in Eq. 3-16  $p$  or  $n$  can be replaced by  $n_i$ . The intrinsic thermopower limit is illustrated in Fig. 3-10 by a black dashed line. It has to be underlined that the intrinsic limit can be achieved for lower temperatures when  $N_A$  or  $N_D$  are small (*light doping*) than for heavily doped semiconductors.

When  $T$  is small enough to fulfil the condition  $p(T) \gg n_i(T)$  or  $n(T) \gg n_i(T)$  the formula Eq. 3-16 can be approximated with very good agreement by replacing carrier concentrations  $p$  or  $n$  by doping concentrations  $N_A$  or  $N_D$ , respectively. This significantly simplifies the calculations because the thermopower can be determined without referring to the carrier concentrations.  $S_p$  and  $S_n$  based on this approximation is presented graphically in Fig. 3-10 by the green dashed line.

Another interesting fact is the comparison of  $|S_n|$  and  $S_p$  for the same material. For **Si** and **Ge** thermopower in  $p$ -type material is slightly lower than for  $n$ -type material for the same temperature and doping concentration. Such situation can be explained using Table 3-4. The effective mass for electron  $m_e$  is higher than the effective mass for holes  $m_h$ . This results in a higher value of  $N_C$  over  $N_V$  and thus in the range of temperatures where the semiconductor is not intrinsic the  $|S_n|$  is slightly higher than  $S_p$ .

Focusing now on the thermopower in **Si<sub>70%</sub>Ge<sub>30%</sub>**, thanks to the modelling of the carrier concentration, the thermopower can be calculated following Eq. 3-12. The illustration of  $S_n$  and  $S_p$  in **Si<sub>70%</sub>Ge<sub>30%</sub>** is presented in Fig. 3-11.



**Fig. 3-11 Thermopower in **Si<sub>70%</sub>Ge<sub>30%</sub>** versus temperature for different doping concentrations. Continuous lines consider thermal impact on carrier concentrations; green dashed line the carrier concentration replaced by the doping concentration and independent on the temperature; black line the thermopower in intrinsic **Si<sub>70%</sub>Ge<sub>30%</sub>** a) *n*-type **Si<sub>70%</sub>Ge<sub>30%</sub>** b) *p*-type **Si<sub>70%</sub>Ge<sub>30%</sub>****

Fig. 3-11 illustrates the thermopower behaviour over temperature for different *n*- and *p*-type doping levels. At first glance when comparing Fig. 3-11 with Fig. 3-10, it can be remarked that the  $S_n$  and  $S_p$  are exhibiting comparable behaviour over the considered range of temperature. However, when focusing more on details, important differences can be noticed. In **Si<sub>70%</sub>Ge<sub>30%</sub>** for lower temperatures than the intrinsic limit, it can be

observed that both  $S_n$  and  $S_p$  are constant over the temperature. In the corresponding temperature range for **Si** and **Ge**,  $|S_n|$  and  $S_p$  are rising (compare with Fig. 3-10). This situation is the result of more precise modelling of  $N_C$  and  $N_V$  in **Si** and **Ge** which are considered as temperature dependent (see Eq. 3-8) while in  $\text{Si}_x\text{Ge}_{1-x}$  only composition dependence is considered according to Eq. 3-12. The omission of the temperature impact on the  $N_C$  and  $N_V$  result in a relatively low error when operating temperatures are close to room temperature. In contrast, the error increases with temperature difference ( $\Delta T$ ) across the material. For high temperatures for which the  $n_i(T)=p(T)$  or  $n(T)$ ,  $|S_n|$  and  $S_p$  are dominated by the intrinsic concentration and thus start to decay. For light doping this reduction of thermopower occurs for lower temperatures, while for the doping level above  $10^{17}\text{cm}^{-3}$  this reduction is not visible in the considered temperature range. Moreover, when comparing the  $S_n$  and  $S_p$  in  $\text{Si}_{70\%}\text{Ge}_{30\%}$  with their corresponding counterparts for **Si** or **Ge**, it can be remarked that the thermopower value in  $\text{Si}_{70\%}\text{Ge}_{30\%}$  is lower than in pure **Si** and higher than in pure **Ge**.

To benchmark  $S_p$  and  $S_n$  in **Si**, **Ge** and  $\text{Si}_{70\%}\text{Ge}_{30\%}$  with conventional thermoelectric material represented by the  $\text{Bi}_2\text{Te}_3$  [Luo, 2012] Fig. 3-12 is provided:

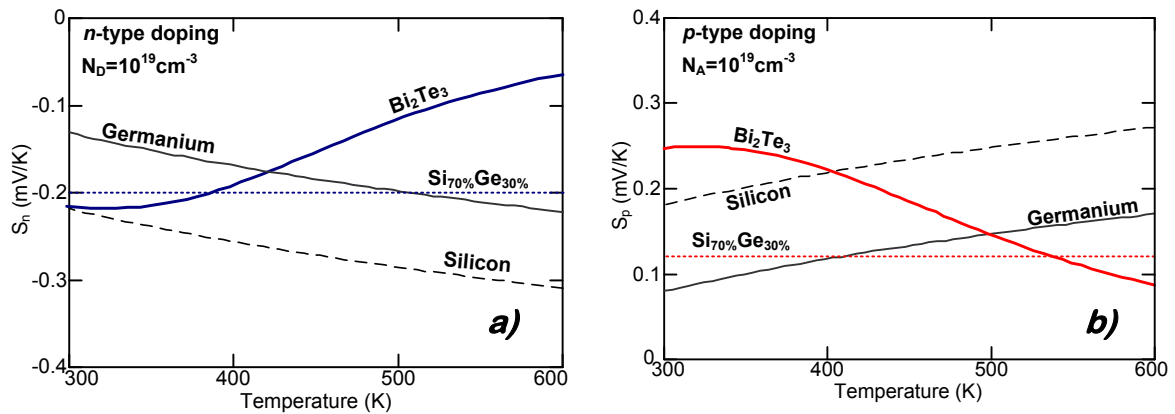


Fig. 3-12 Thermopower versus temperature for  $\text{Bi}_2\text{Te}_3$  [Luo, 2012], Silicon, Germanium and  $\text{Si}_{70\%}\text{Ge}_{30\%}$ , a)  $n$ -type concentration  $N_D=10^{19}\text{cm}^{-3}$ , b)  $p$ -type concentration  $N_A=10^{19}\text{cm}^{-3}$

Compared materials are heavily doped to a level of  $N_A=N_D=10^{19}\text{cm}^{-3}$ . Investigating Fig. 3-12a it is worth noting that **Si** has higher absolute value of thermopower than  $\text{Bi}_2\text{Te}_3$  within all the considered temperature range. When comparing  $|S_n|$  in **Ge** with  $|S_n|$  in  $\text{Bi}_2\text{Te}_3$ , it can be remarked that  $\text{Bi}_2\text{Te}_3$  has a higher value near-room temperature but for temperatures higher than  $\sim 420\text{K}$   $n$ -type **Ge** thermopower is higher.  $|S_n|$  in  $\text{Si}_{70\%}\text{Ge}_{30\%}$  is lower than in  $\text{Bi}_2\text{Te}_3$  for temperatures lower than 400K. But for higher temperatures the thermopower in  $\text{Bi}_2\text{Te}_3$  has a lower value. More or less, the same observation can be done when studying Fig. 3-12b, with the exception that for temperatures near 300K  $p$ -type  $\text{Bi}_2\text{Te}_3$  has higher  $S_p$  than **Si** and **Ge**. With rising temperature,  $|S_n|$  and  $S_p$  in  $\text{Bi}_2\text{Te}_3$  are decreasing because the material becomes intrinsic.  $\text{Bi}_2\text{Te}_3$  is the material which is dedicated for near-room temperature thermoelectric conversion for which the maximal value of  $zT$  near room temperature is observed (see Fig. 2-38a).

General conclusion which arises from Fig. 3-12 is the fact that  $|S_n|$  and  $S_p$  for **Si** and **Ge** are comparable with the thermopower available in  $\text{Bi}_2\text{Te}_3$ . This means that **CMOS** compatible materials represented by **Si** and **Ge** are offering comparable performance as far as thermopower is considered. Such conclusion is advantageous for **Si** and **Ge** when considering their price (Table 3-1), environmental and biological danger (Table 3-2) and their compatibility with the digital industry.

## 3.2.1.4 Analysis of the power factor

The evaluation of thermoelectric materials can be achieved in numerous different ways. Firstly, comparing their  $\mathbf{zT}$  values for a given temperature (see Fig. 2-38a). Choosing the material with the highest  $\mathbf{zT}$  value for given temperature results in the maximal thermoelectric generator efficiency  $\eta$  (according to Eq. 2-14).

Another key parameter to compare materials from the thermoelectric point of view is to consider the **Power Factor (PF)**. The **PF** value evaluates materials considering only the electrical properties: the thermopower ( $\mathbf{S}$ ) and electrical conductivity ( $\sigma$ ) regardless of the heat transport properties defined by thermal conductivity ( $\kappa$ ). The **PF** is defined as follows [Wang, 2013] Eq. 3-17:

$$\begin{cases} PF_n(T, N_D) = S_n^2(T, N_D) \cdot \sigma_n(T, N_D) \\ PF_p(T, N_A) = S_p^2(T, N_A) \cdot \sigma_p(T, N_A) \end{cases} \quad \text{Eq. 3-17}$$

Good thermoelectric material should have as high as possible **PF**. According to Eq. 3-17, the **PF** is proportional to  $\mathbf{S}^2$  and  $\sigma$ . Maximizing thermopower value magnifies the value of thermally-induced electric potential, the generator output voltage is rising with rising  $\mathbf{S}$  for fixed temperature difference across the generator (following Eq. 2-11 and Eq. 2-12). Increasing  $\sigma$  results in a reduction of the internal generator resistance and for a given temperature difference across the generator, the output harvested current is higher. **PF** multiplies the parameter responsible for the output voltage  $\mathbf{S}$  by the parameter responsible for the output current  $\sigma$ . Multiplying current by voltage gives, in turn, the power and this is the meaning of the **Power Factor**.

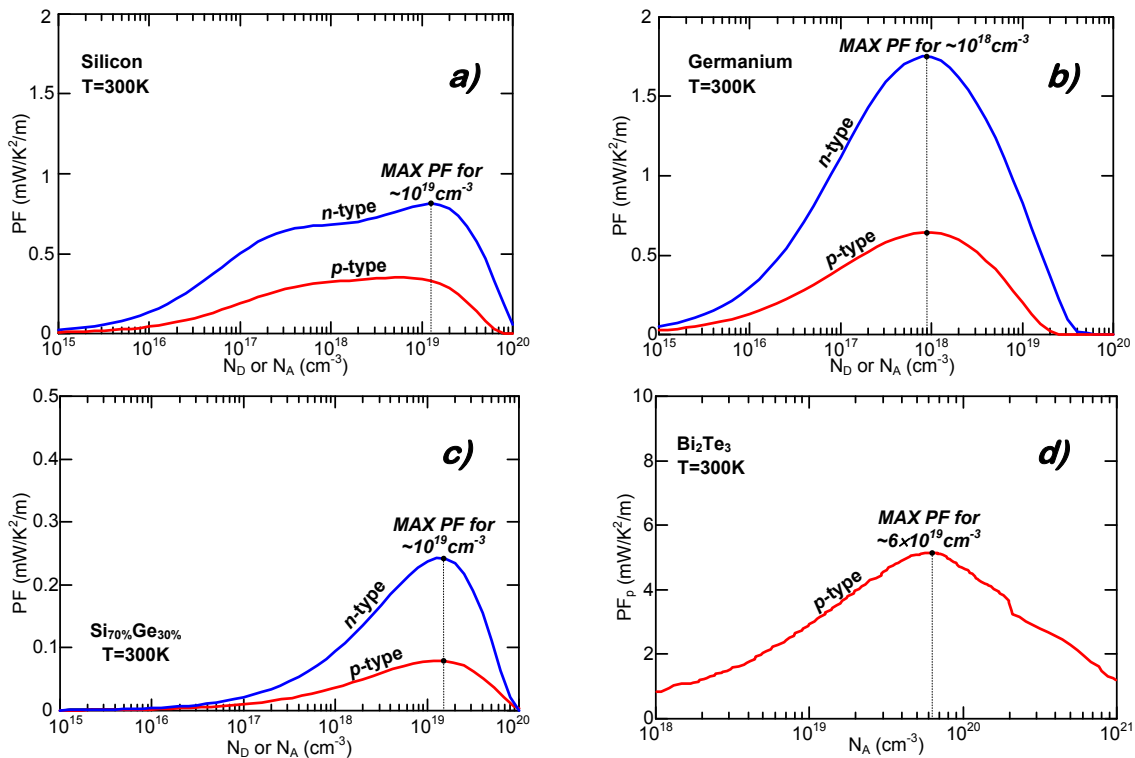


Fig. 3-13 Power factor versus doping concentration comparison for a) Silicon, b) Germanium, c) Si<sub>70%</sub>Ge<sub>30%</sub> and d) p-type Bi<sub>2</sub>Te<sub>3</sub> [Snyder, 2008]

Choosing material with the highest **PF** will result in the selection of the material which can deliver the highest power to the load for a given temperature difference.

However, it does not mean that this material will efficiently harvest energy. The **PF** describes the electrical capabilities of a given material in thermoelectric energy harvesting.

Consolidating together  $\sigma$  and **S** for **CMOS** materials and for **Bi<sub>2</sub>Te<sub>3</sub>**, described previously, enables the comparison of the **PF** depicted in Fig. 3-13. Data are for room temperature which is optimal temperature for **Bi<sub>2</sub>Te<sub>3</sub>**, as previously described in Table 2-17. **Si**, **Ge** and **Si<sub>x</sub>Ge<sub>1-x</sub>** are the most efficient at high temperatures differences (*see Table 2-17*), thus at room temperature their performance is reduced.

Fig. 3-13a, Fig. 3-13b and Fig. 3-13c reveals that *n*-type doping offers higher **PF** than *p*-type doped materials. This situation is caused by higher  $\sigma_n$  and **S<sub>n</sub>** values comparing with their *p*-type counterparts. Moreover, the **PF** for **Ge** has a significantly higher maximal value than **Si** which indicates that for an optimal doping concentration **Ge** will generate higher power for the given  $\Delta T$  than **Si**. The outperformance of **Ge** over **Si** is essentially achieved by the significantly higher electrical conductivity in **Ge** for the same doping concentration (*see Fig. 2-40*). The **PF** in **Si<sub>70%</sub>Ge<sub>30%</sub>** has smaller values than in **Si** and **Ge** with a maximal value for doping around  $\sim 10^{19} \text{cm}^{-3}$ . However, it has to be underlined that due to simplified modelling of material parameters (*especially N<sub>V</sub> and N<sub>C</sub>*) for **Si<sub>70%</sub>Ge<sub>30%</sub>** the presented **PF** is also affected by this approximation. Nevertheless, the **PF** value in **Si<sub>70%</sub>Ge<sub>30%</sub>** indicates that among **CMOS** compatible materials, **Si<sub>70%</sub>Ge<sub>30%</sub>** will generate the lowest electrical power for the same temperature difference. The low value of **PF** in **Si<sub>70%</sub>Ge<sub>30%</sub>** is the result of low  $\sigma$  caused by the lattice constants mismatch and the associated strain at the lattice level which lowers significantly the carrier mobilities. Moreover, as outlined previously the investigated temperature is not the optimal for **CMOS** compatible materials, which results in rather low **PF** values compared with **Bi<sub>2</sub>Te<sub>3</sub>**.

**PF** is especially used during the generator design and allows choosing doping concentration for which the harvested power is maximal. This is possible because the thermal conductivity  $\kappa$  is almost independent on the doping concentration (*see 2.5.2.1.2*). Fig. 3-13a, Fig. 3-13b, Fig. 3-13c and Fig. 3-13d are depicting the **PF** versus doping concentration for **Si**, **Ge**, **Si<sub>70%</sub>Ge<sub>30%</sub>** and **Bi<sub>2</sub>Te<sub>3</sub>** [[Snyder, 2008](#)] respectively. From Fig. 3-13, it is possible to determine the doping concentration for which the **PF** is maximal. This concentration should be then used when designing the thermo-generator to boost the harvested power. Maximal value of **PF** is achieved when using doping concentrations of  $\sim 10^{19} \text{cm}^{-3}$  for **Si** and **Si<sub>x</sub>Ge<sub>1-x</sub>**,  $\sim 10^{18} \text{cm}^{-3}$  for **Ge** and  $\sim 6 \times 10^{19} \text{cm}^{-3}$  when using **Bi<sub>2</sub>Te<sub>3</sub>**.

Comparing the **PF** values achieved by **CMOS** compatible materials and by conventional **Bi<sub>2</sub>Te<sub>3</sub>**, it can be observed that **Bi<sub>2</sub>Te<sub>3</sub>** exhibits significantly higher **PF** values than **CMOS** materials. This observation can be surprising especially in light of comparison of  $\sigma$  and **S** values presented previously. The superiority of **Bi<sub>2</sub>Te<sub>3</sub>** over **Si** and **Ge** is achieved firstly through higher  $\sigma$  in **Bi<sub>2</sub>Te<sub>3</sub>** (*see Fig. 3-9*). Secondly the **PF** factor is calculated using  $\sigma$  and **S** values for room temperature and as mentioned already near room temperature performance of **Bi<sub>2</sub>Te<sub>3</sub>** is higher than for the **CMOS** compatible counterpart.

The observation of higher **PF** in **Bi<sub>2</sub>Te<sub>3</sub>** leads to the conclusion that this material will be more productive electrically for **T<sub>HOT</sub>** around 300K. However, the low **PF** in **CMOS** compatible materials can be compensated by the attractive cost, harmlessness and industrial compatibility.

## 3.2.1.5 Thermal conductivity

## 3.2.1.5.1 Bulk material

The overall thermoelectric generator harvesting capabilities are depending on the electrical transport described by  $\sigma$ , the Seebeck coefficient ( $S$ ) and thermal transport described by the thermal conductivity ( $\kappa$ ). Previously,  $\sigma$  and  $S$  modelling was presented, in this section the focus will be put on the thermal conductivity.

The thermal conductivity is defined using the Eq. 2-18. The total  $\kappa$  is the sum of two contributions namely, lattice  $\kappa_l$  Eq. 2-19 and electronic  $\kappa_{el}$  Eq. 2-20 components. The decomposition of  $\kappa$  into two contributions shows that the heat can be transported by the lattice vibrations (*phonons*) ( $\kappa_l$ ) and by the charged carriers ( $\kappa_{el}$ ). However, for semiconductors the significant majority of the heat is transported by the lattice (see Table 2-14). This shows that the heat and electric transport properties are well decoupled.  $\kappa$  depends on the temperature and this dependence is depicted in Fig. 3-14a:

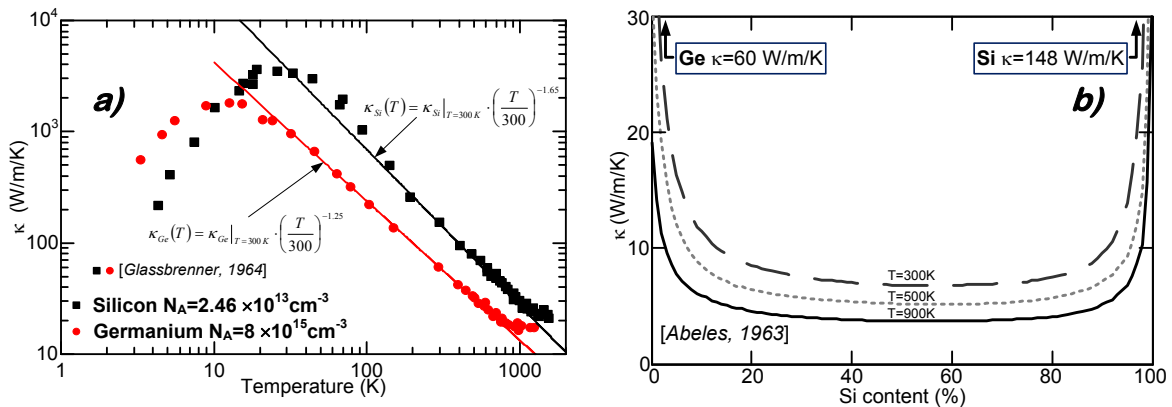


Fig. 3-14 a) Experimental total thermal conductivity in Silicon (black markers) and Germanium (red markers) against temperature [Glassbrenner, 1964], b) Thermal conductivity in  $\text{Si}_x\text{Ge}_{1-x}$  for different Silicon content [Abeles, 1963]

Fig. 3-14a shows the variation of  $\kappa$  over a wide range of temperatures for **Si** and **Ge**. For very low temperatures,  $\kappa$  is rising with increasing temperature and afterwards for temperatures higher than few tens of kelvins,  $\kappa$  starts to decrease for rising temperatures. As it was already described the major part of the heat is transported by the lattice vibrations called the phonons [Ziman, 2001]. In the low temperature range, the material lattice vibrations are very small facilitating the phonons propagation. Thus, the heat is easily transported by phonons across the material resulting in a high  $\kappa$  value. In this range the  $\kappa$  rises with rising temperature. The opposite situation occurs for higher temperatures. In such a case, the material lattice vibrations are high enough to perturb the phonon propagation causing the phonon scattering. This results in  $\kappa$  reduction when the temperature rises. Increasing temperature causes further reduction of  $\kappa$  which can be explained by the increased phonon scattering due to rising lattice vibrations. The range for which  $\kappa$  is decreasing for rising temperatures can be approximated with a satisfying precision using power relationship Eq. 3-18 [Palankovski, 2001].

$$\kappa_{bulk}(T) = \kappa_{bulk}|_{T=300K} \cdot \left(\frac{T}{300}\right)^{\gamma} \quad \text{Eq. 3-18}$$

**Table 3-8 The variable values for temperature dependent model of thermal conductivity in Si and Ge**

<i>Material</i>	$\kappa(T=300K)$ W/m/K	$\gamma$	<i>Reference</i>
Silicon	148	-1.65	<a href="#">[Palankovski, 2001]</a> and <a href="#">[Silvaco, 2012]</a>
Germanium	60	-1.25	

Referring to Fig. 3-14a, it can be observed that  $\kappa$  for **Si** and **Ge** is approximated by the Eq. 3-18 in very wide temperature range. For **Si** the satisfying approximation is achieved from ~50K to ~1000K, and for **Ge** the Eq. 3-18 is acceptable from ~30K to ~900K. Worth noting is the fact that within this wide temperature range  $\kappa$  is approximated using only the room temperature value of  $\kappa$ .

Thermoelectricity requires materials with as low as possible  $\kappa$  to maximize  $zT$  Eq. 2-13.  $\kappa$  in bulk **Si** and **Ge** was for decades the eliminative reason for the use of those materials in thermoelectricity.  $\kappa$  values even for very high temperatures are significantly higher than 10W/m/K which results in drastic reduction of  $zT$  in **Si** and **Ge**. Good electrical transport properties described in previous sections are not sufficient to counterbalance this effect.

Focusing on  $\kappa$  in **Si<sub>x</sub>Ge<sub>1-x</sub>** illustrated in Fig. 3-14b as a function of the **Si** content, it is visible that  $\kappa$  is significantly reduced over a very wide range of **Si** content. For **Si** content between 20% and 80% the room temperature  $\kappa$  is ~8W/m/K which is 18× less than in bulk **Si** and 7.5× less than in bulk **Ge**. This significant and natural  $\kappa$  reduction is introduced by the lattice disorder due to different lattice constants in **Si** and **Ge**. This creates obstacles for phonons propagation in **Si<sub>x</sub>Ge<sub>1-x</sub>**. On the other hand, the same lattice disorder caused the significant reduction of carrier mobilities comparing to bulk **Si** or **Ge** (see Fig. 3-8). Thanks to such high thermal conductivity reduction comparing with bulk **Si** and **Ge**, **Si<sub>x</sub>Ge<sub>1-x</sub>** remains the sole **CMOS** compatible material used in conventional thermoelectric devices.

### 3.2.1.5.2 Reducing the thermal conductivity

Recent progress in nanotechnology revealed the possibility of  $\kappa$  reduction with minor impact on the electrical properties. This reduction relies on the decoupling between thermal and electrical transport in the semiconductors which was highlighted previously (see section 2.5.2.1.4).  $\kappa$  Eq. 2-18 is the sum of two contributions indicating that heat is partly transported by the lattice  $\kappa_l$  Eq. 2-19 and partly by charged carriers  $\kappa_{el}$  Eq. 2-20. In semiconductors  $\kappa_l$  is dominant over  $\kappa_{el}$  (see Table 2-14). The distinction between  $\kappa_l$  and  $\kappa_{el}$  can be done by comparing the mean free paths  $L^{22}$ . For  $\kappa_l$ , the mean free path for phonons  $L_{ph}$  should be compared with mean free path for electrons/holes  $L_e$  determining the  $\kappa_{el}$  component. In bulk **Si**,  $L_{ph} \approx 300\text{nm}$  [\[Marconnet, 2013\]](#) while  $L_e \approx 1...2\text{nm}$ . This huge difference between  $L_{ph}$  and  $L_e$  opens a possibility to alter the propagation of the phonons without changing the propagation of charged carriers.

<sup>22</sup> The mean free path  $L$  is the average distance which can be travelled by the particle (molecule, atom, photon, etc) without any interactions or collisions [\[Carey, 2008\]](#).

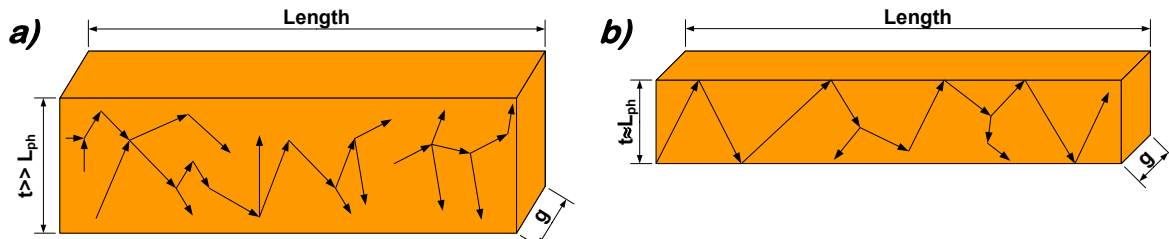


Fig. 3-15 Phonon propagation in the material, a) in bulk materials, b) in nanostructured material

When used material dimensions are significantly bigger than  $L_{ph}$ , the phonon propagation is not altered Fig. 3-15a. In this situation, the surface scattering is playing a negligible role.

The use of modern nanotechnology enables the fabrication of the materials with lower dimensionality than  $L_{ph}$ . In such a case,  $L_{ph}$  is reduced because the phonons are entering in collisions not only with lattice defects but also with the material extremities (*surface scattering*) Fig. 3-15b. Moreover, for decreasing material dimensions, the effects occurring on the boundaries are playing more important. Size-induced reduction of  $L_{ph}$  results in the reduction of the total thermal conductivity.

Looking closer to  $\kappa$  in **Si**, it can be observed that at room temperature around 85% of the  $\kappa$  value is contributed by the phonons with free path in the range of 0.04...40 $\mu$ m [Dechaumphai, 2012] Fig. 3-16a. Interestingly,  $\kappa$  reduction in **Si** is observable for phonons with  $L_{ph}$  lower than 1000 $\mu$ m but below 100 $\mu$ m this reduction is accentuated. Worth noting is the fact that at low temperatures,  $\kappa$  builds up by phonons with a higher mean free path than in high temperature Fig. 3-16a. This thermally-induced  $L_{ph}$  reduction is caused by increasing lattice vibrations which reduce the average distance between the subsequent collisions. The derivative of **Si** room temperature  $\kappa$  with respect to the phonon free path is plotted in Fig. 3-16b. This curve shows in a different light the contribution of phonons with different  $L_{ph}$  to the total thermal conductivity. Interestingly, the phonons with free paths below 1.5 $\mu$ m are representing half of total  $\kappa$  in bulk **Si**, which means that great majority of heat is transported by the phonons with free paths lower than 10 $\mu$ m. The surface below the curve in Fig. 3-16b for all  $L_{ph}$  is the  $\kappa$  component for bulk **Si**.

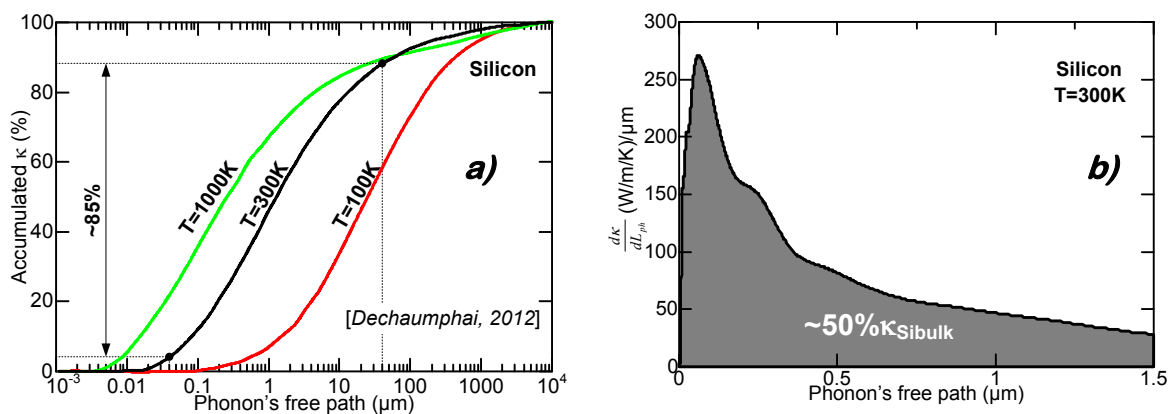


Fig. 3-16 Thermal conductivity in Silicon a) Accumulated Silicon  $\kappa$  over wide range of phonon's free path for different temperatures [Dechaumphai, 2012], b) Derivative of the Silicon room temperature  $\kappa$  with respect to the phonon's free path plotted against phonon's free path

$\kappa$  for the materials with a given thickness ( $t$ ) follows Eq. 3-19 [Sondheimer, 1952]:

$$\kappa_{film}(T, t, L_{ph}) = \kappa_{bulk}(T) \cdot F(t, L_{ph}) \quad \text{Eq. 3-19}$$

where:

$$F(t, L_{ph}) = 1 - \frac{3}{2} \cdot \frac{t}{L_{ph}} \int_1^{\infty} \left( \frac{1}{z^3} - \frac{1}{z^5} \right) \cdot \left[ 1 - \exp\left( -\frac{t}{L_{ph}} \cdot z \right) \right] dz \quad \text{Eq. 3-20}$$

Eq. 3-20 allows calculating the correction coefficient for materials with thickness  $t$  lower than  $L_{ph}$ . Substituting Eq. 3-18 into Eq. 3-19 also takes into consideration the  $\kappa$  dependence on the temperature.

The described concept of size-induced thermal conductivity reduction was experimentally confirmed for several **Si** thicknesses [Asheghi, 1997], [Asheghi, 2002], [Haras, 2014-a], [Ju, 2005], [Liu, 2005], [Tang, 2010] and [Yu, 2010] which is presented graphically in Fig. 3-17a and compared with analytical model [Sondheimer, 1952]:

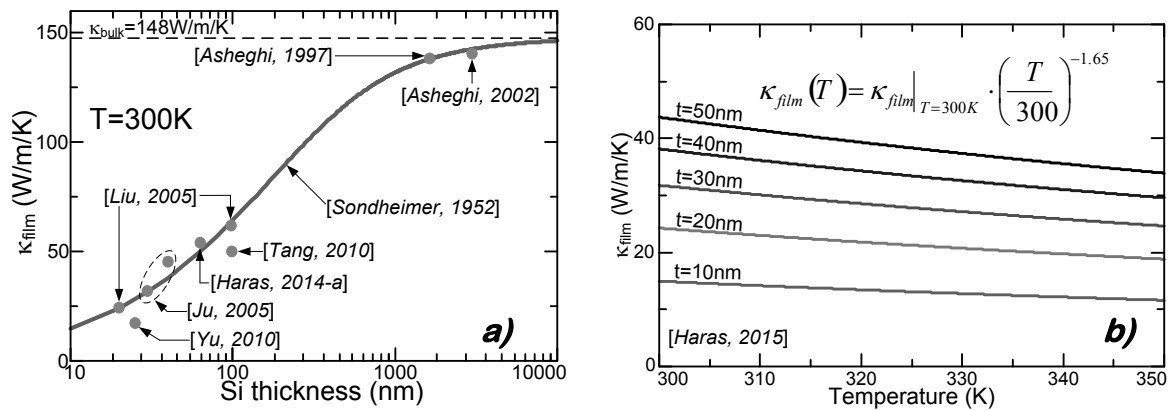


Fig. 3-17 Thermal conductivity reduction in Silicon; a) Silicon thermal conductivity versus thickness, b) Temperature impact on thermal conductivity for different Silicon thicknesses  $t$  [Haras, 2015] following Eq. 3-17 [Palankovski, 2001]

The first conclusion arising from this plot is the fact that the **Si** thermal conductivity reduction has been confirmed experimentally. Secondly, the analytical model Eq. 3-19 follows the experimental data with good precision when parameters values  $L_{ph}=300\text{nm}$   $\kappa_{bulk}=148\text{W/m/K}$  are used. Fig. 3-17b reveals the temperature dependence of  $\kappa$  calculated using Eq. 3-19. It is assumed that  $\kappa$  in thin-film **Si** exhibits the same behaviour with the temperature as bulk **Si**. The main reason for adopting this assumption is the lack of experimental data pertaining to thin-film **Si** for temperatures higher than 300K. However, this assumption is justified when small variations of temperature around 300K are under consideration. Fig. 3-17b shows that the temperature difference of  $\Delta T=50\text{K}$  over the room temperature causes a  $\kappa$  reduction of 30% regardless of the **Si** thickness.

The described  $\kappa$  reduction does not alter significantly the electrical properties, due to the large difference between  $L_{ph}$  and  $L_e$ . This is confirmed by  $\sigma$  measurements in the 22nm thick **Si** membrane [Yu, 2010]<sup>23</sup> presented in Fig. 3-18a.

<sup>23</sup> In this article  $\sigma$  versus temperature is reported for 22nm **Si** thick membrane with mesh of cylindrical holes. The  $\sigma$  values were corrected by the volume represented by the holes to obtain the  $\sigma$  in plain thin-film **Si** membrane.



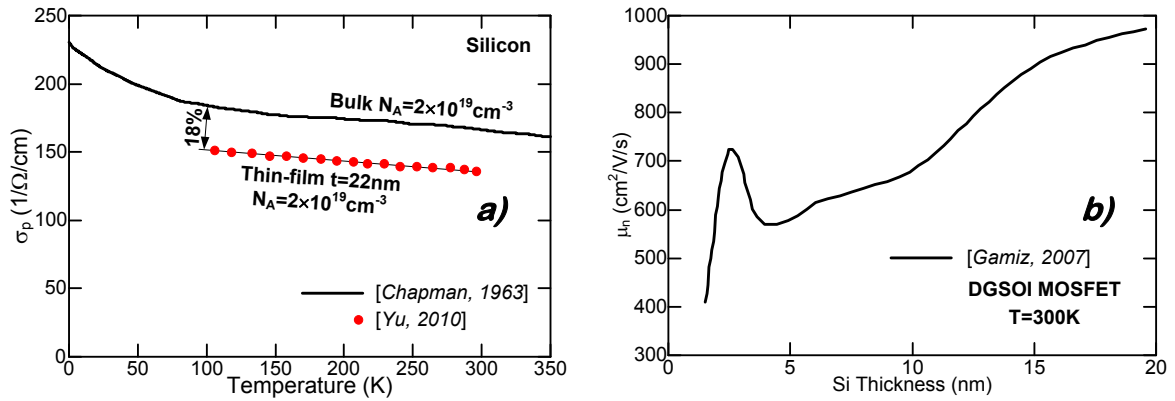


Fig. 3-18 a) Electrical conductivity in *p*-type Silicon versus temperature for bulk material [Chapman, 1963] and 22nm thick membrane [Yu, 2010], b) Low field electron mobility versus Silicon thickness in DGSOI MOSFET [Gamiz, 2007]

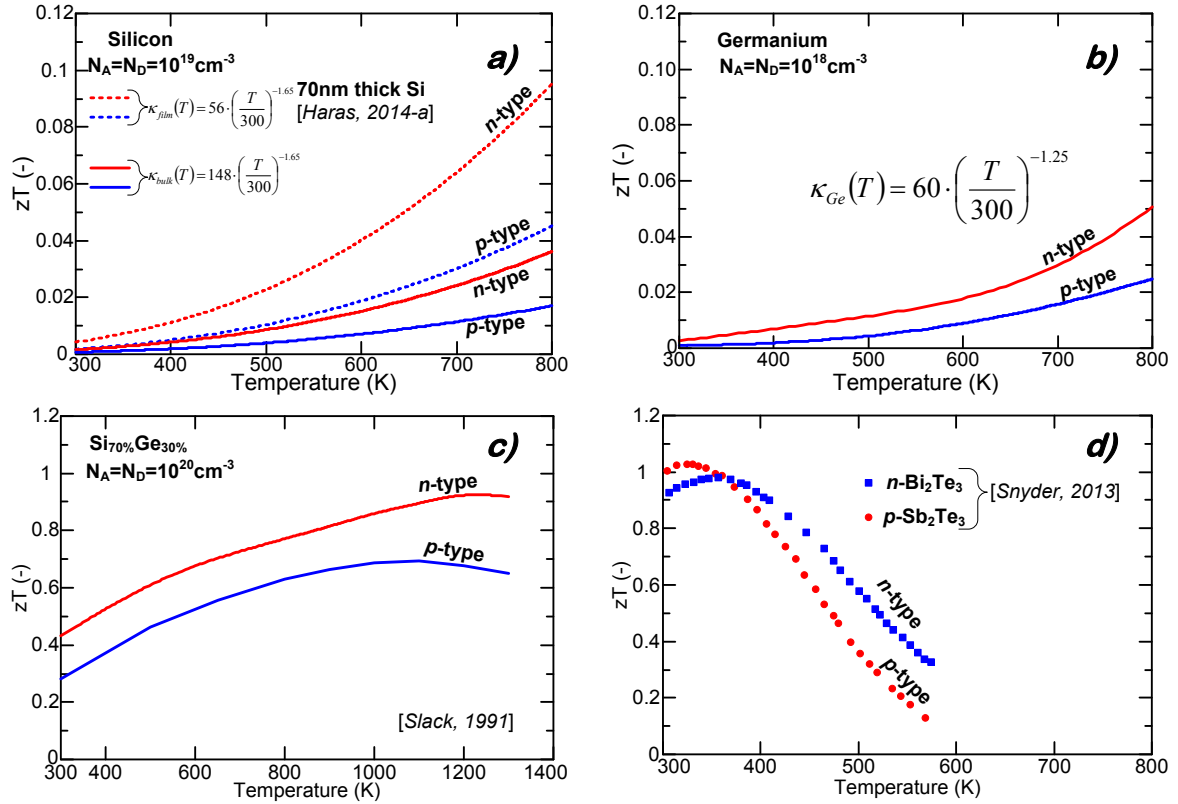
Studying Fig. 3-18a leads to the conclusion that the reduction of **Si** thickness to 22nm causes the suppression of  $\sigma$  by only 18% compared with bulk  $\sigma$  for the same doping concentration. This 18% reduction can be a result of the size-induced carrier mobility reduction reported in [Gamiz, 2007] and [Uchida, 2006] Fig. 3-18b. Analyzing Fig. 3-18b it can be observed that for **Si** thickness of around 20nm  $\mu_n$  starts to decay. The mobility in 22nm thick **Si** is not reported, however it can be assumed that the slight reduction occurs also for this thickness. Fig. 3-18b reports the size induced electron mobility reduction while Fig. 3-18a shows the  $\sigma$  reduction in *p*-type **Si**. The comparison of two types of carriers is justified here because the hole mobility is also affected by the thickness. Because of lack of reported data the plot concerning electrons is used.  $\kappa$  for 22nm thick **Si** equals  $\sim 25 \text{ W/m/K}$  meaning that  $\kappa$  is reduced  $\sim 600\%$  compared with bulk. This observation proves that  $\kappa$  in **Si** is very well decoupled from electrical properties.

The possibility of  $\kappa$  reduction with minor impact on  $\sigma$  or **S** is the way to improve **zT** (see Eq. 2-13). However, the fabrication of the thermo-generators based on the thin-films is often complicated and involves sophisticated procedure. Moreover, the use of thin-films is making the thermoelectric generator much more fragile mechanically and sensitive to vibrations, shocks *etc.* than its bulk counterpart. This obliges to reinforce the mechanical protection of the thermoelectric generator which is not always easy or feasible. Despite the mechanical issues introduced by thin-films, the possibility to use semiconductors with high bulk  $\kappa$  e.g. **Si** or **Ge** in the thermoelectricity is a very interesting possibility. Especially in light of already described material orientations of **CMOS** industry, the concept of  $\kappa$  reduction in **CMOS** compatible materials is very important. Using the effect of size induced  $\kappa$  reduction, the number of possible applications of **Si**, **Ge** and **Si<sub>x</sub>Ge<sub>1-x</sub>** rises significantly and the offer of the electron devices manufacturers can be expanded.

### 3.2.1.6 **zT** and efficiency investigation

The constructed analytic model of the thermoelectric parameters allows investigating the theoretical **zT** in **Si**, **Ge** and **Si<sub>70%</sub>Ge<sub>30%</sub>**. To relevantly evaluate **zT** for **CMOS** compatible materials, the optimal doping concentration was used to maximize the **zT** value. Hence, optimal doping concentration is chosen considering the maximal value of the power factor (see section 3.2.1.4). For **Si** and **Si<sub>x</sub>Ge<sub>1-x</sub>**, the maximal value of **PF** is achieved for doping concentrations  $N_A = N_D = 10^{19} \text{ cm}^{-3}$  (see Fig. 3-13a and Fig. 3-13c), while for **Ge** the **PF** has a maximal value at  $N_A = N_D = 10^{18} \text{ cm}^{-3}$  (see Fig. 3-13b). To benchmark **zT** for **CMOS** compatible materials with the conventional thermoelectric

materials,  $zT$  for  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$  is presented following the data reported in [Snyder, 2008]. The choice of  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$  is not random because those materials are the most popular when constructing thermoelectric generator for near room temperature energy harvesting. The  $zT$  comparison is presented in Fig. 3-19:



**Fig. 3-19** Non-dimensional-figure-of-merit at optimal doping concentration versus temperature for a) Silicon, b) Germanium, c)  $\text{Si}_{70\%}\text{Ge}_{30\%}$  [Slack, 1991] and d)  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$  [Snyder, 2008]

At first glance, comparing  $zT$  for bulk **Si** Fig. 3-19a (*continuous lines*) with bulk **Ge** Fig. 3-19b it is visible that, for both materials,  $zT$  is very low, especially near room temperature. This is the direct reason why pure bulk **Si** and **Ge** are not used in thermoelectricity. For a wide temperature range,  $zT$  for both materials is significantly lower than 0.1. Secondly,  $zT$  in bulk **Ge** is slightly higher than in bulk **Si**. This is the result of a lower thermal conductivity and higher  $\sigma$  in bulk **Ge**. This conclusion was already revealed when comparing the **PF** in **Si** and **Ge** (compare Fig. 3-13a with Fig. 3-13b). The model takes into account the local temperature and doping level impact on the thermoelectric parameters. With rising temperature,  $\kappa$  is decreasing as illustrated in Fig. 3-14a for **Si** and for **Ge**. The temperature induced  $\kappa$  reduction should improve  $zT$  for rising temperatures but this is compensated by the temperature impact on **S** and  $\sigma$  which are reduced when temperature rises. In Fig. 3-19a and Fig. 3-19b,  $zT$  is rising with temperature which means that  $\kappa$  is decreasing more significantly than **S** and  $\sigma$ . Regardless of the  $zT$  behaviour over the temperature range, the values of  $zT$  for **Si** and **Ge** are precluding their usage in the thermoelectricity in the bulk form. Knowing that electrical performance of **Si** and **Ge** is comparable with conventional thermoelectric materials (compare Fig. 3-13a and Fig. 3-13b with Fig. 3-13d). The main reason for such a low  $zT$  is the very high  $\kappa$  for bulk **Si** and **Ge**. Thus previously described concept of phonon scattering enhancement by the reduction of material dimensionality is a big opportunity to boost  $zT$ . Encouraged by this opportunity  $zT$  for 70nm thick **Si** membrane with  $\kappa=57\pm 7.5\text{W/m/K}$  [Haras, 2014-a] is depicted in Fig. 3-19a (*dashed lines*). At first glance,

the significant  $zT$  improvement between bulk and thin-film **Si** is visible. **Si** thinning reduced  $\kappa$  and as consequence  $zT$  is improved around 2.5-times over bulk  $zT$ .

The sole **CMOS** compatible material used in thermoelectricity is  $\text{Si}_x\text{Ge}_{1-x}$ . When analyzing  $zT$  versus temperature for  $\text{Si}_{70\%}\text{Ge}_{30\%}$  Fig. 3-19c it can be noted that  $zT$  has a maximal value in the range of 1000-1200K, and that maximal  $zT$  is around 0.9 for *n*-type and 0.7 for *p*-type. This is comparable with the capabilities represented by the  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$  plotted in Fig. 3-19d, but the temperature for which the maximal  $zT$  is achieved is around 300K.

$zT$  for **CMOS** compatible materials confirms what was previously discussed. That **Si**, **Ge** and  $\text{Si}_x\text{Ge}_{1-x}$  are the materials dedicated for high temperature thermoelectric conversion (see Table 2-17). Their use at lower temperatures is practically justified in the situation when their high bulk  $\kappa$  can be reduced as much as possible.

Substituting the  $zT$  values from the Fig. 3-19 into Eq. 2-14 and assuming that the  $T_{\text{COLD}}=300\text{K}$  and is maintained constant, the material thermoelectric efficiency  $\eta$  can be calculated as showed in Fig. 3-20.

Analyzing the continuous lines in Fig. 3-20a and Fig. 3-20b it is visible that bulk **Ge** slightly outperforms bulk **Si**. However, for both bulk **Si** and **Ge**, the theoretical efficiencies are very small approaching in the best case to  $\eta=1\%$  for  $\Delta T=500\text{K}$ . The reason of such a small  $\eta$  at high  $\Delta T$  across the material was previously described. Mainly, it is caused by the too high thermal conductivities in bulk **Si** and **Ge**. When using thinned **Si** (dashed lines Fig. 3-20a) the efficiency is significantly improved. A **Si** membrane with a thickness of 70nm has higher theoretical efficiency than bulk **Ge** which exhibits around 3-times higher  $\sigma$  for the same doping concentration. Despite  $\kappa$  reduction,  $\eta$  in 70nm thick **Si** remains rather low  $\sim 2.2\%$  for  $\Delta T=500\text{K}$ . However, further thinning of the **Si** is technologically realisable. A **Si** membrane with a thickness of 9nm was reported [Chávez-Ángel, 2014] with a thermal conductivity of  $\kappa_{\text{film}}=9\pm 2\text{W/m/K}$ . Using **Si** with such  $\kappa$  will result in efficiency improvement of 16.5-times over bulk **Si** efficiency. This amounts to  $\eta\approx 6.6\%$  and  $\eta\approx 13.2\%$  at  $\Delta T=500\text{K}$  and for *p*-type and *n*-type **Si**, respectively. Such  $\eta$  is comparable or better than for conventional thermoelectric materials. The size-induced  $\kappa$  reduction is a promising possibility to enable the **Si**- or **Ge**-based thermoelectricity.

Focusing now on Fig. 3-20c and Fig. 3-20d, it can be observed that  $\text{Si}_{70\%}\text{Ge}_{30\%}$  has a significantly higher  $\eta$  than  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$ . Such situation is caused by the assumption that  $T_{\text{COLD}}$  is maintained constant. In  $\text{Si}_{70\%}\text{Ge}_{30\%}$ , the peak efficiency occurs at very high  $\Delta T$  which means that the Carnot efficiency is higher than at lower  $\Delta T$ . The theoretical efficiency of the material is calculated using Eq. 2-14 where the Carnot efficiency is multiplied by the  $zT$  dependent component. However, when considering only the temperature range around 300-400K, it can be concluded that the  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$  are the most efficient among all presented materials. This conclusion proves why  $n\text{-Bi}_2\text{Te}_3$  and  $p\text{-Sb}_2\text{Te}_3$  are the most popular thermocouple composition for thermoelectric harvesting near the room-temperature.

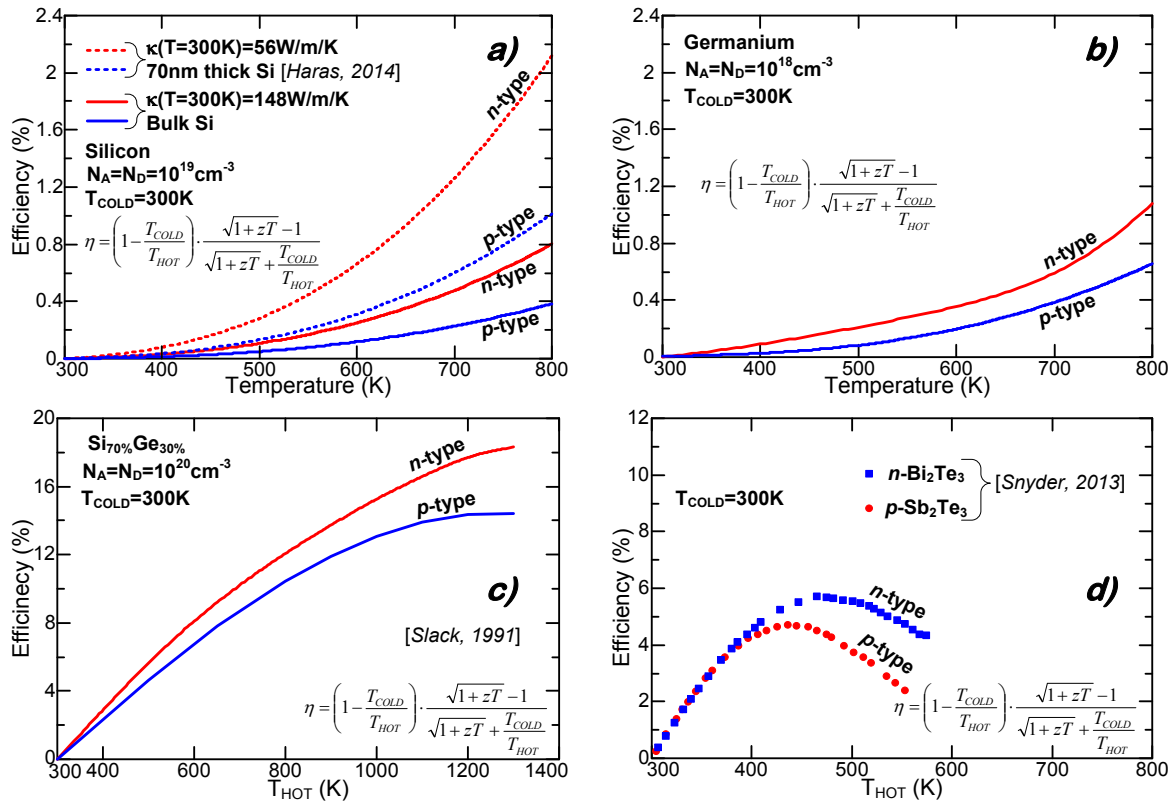


Fig. 3-20 Best case theoretical efficiency versus temperature for a) Silicon, b) Germanium; c)  $Si_{70\%}Ge_{30\%}$  [Slack, 1991] and d)  $n-Bi_2Te_3$  and  $p-Sb_2Te_3$  [Snyder, 2008]

The use of **Si** and **Ge** is possible in thermoelectricity providing that the thermal conductivity can be significantly reduced. Previously described possibility for  $\kappa$  reduction in **Si** enables the significant improvement of the efficiency. In such situation, **Si** can be considered as a material with comparable harvesting capabilities to conventional materials, with the following additional advantages: (i) price reduction, (ii) industrial compatibility, (iii) natural environment preservation and (iv) harmlessness. There is lack of reported data concerning the  $\kappa$  reduction in **Ge**. However, in **Ge** the  $\kappa$  reduction is much more difficult to achieve compared with **Si** due to a very small value of  $L_{ph} \approx 10nm$ . Such a small value of  $L_{ph}$  forces to use extremely thin **Ge** membranes, and in this case the size induced mobility reduction will occur reducing  $\sigma$ .

The size induced phonon scattering enhancement in  $Si_xGe_{1-x}$  was not yet confirmed experimentally. However, knowing that mainly  $Si_xGe_{1-x}$  alloys used in industry are with  $x$  values above 70% gives hope that the further  $\kappa$  reduction in  $Si_xGe_{1-x}$  is feasible as it is experimentally proved for **Si**. The additional  $\kappa$  reduction in  $Si_xGe_{1-x}$  will surely contribute in popularization of **CMOS** compatible thermoelectricity, as well.

### 3.3 Topological non-conventional approach

After evaluating the thermoelectric performance of **CMOS** compatible materials, the focus will be put on the harvesting capabilities simulation of the complete thermoelectric generator (**TEG**). As described at the beginning of this chapter, the improvement of the harvesting effectiveness can be realized through material improvement and/or by the development of innovative generator structures. This section focuses on the description of innovative thermoelectric generators topologies and on the presentation of their performance.

For practical reasons, the **TEGs** are fabricated using *n*-type and *p*-type materials connected electrically in series and thermally in parallel. The *pn* junction is shorted by the metallic strap. Such topology allows boosting the output voltage because the thermally built-in Seebeck voltages in *n*-type and *p*-type leg are added. The most conventional structure of the thermoelectric generator was described previously and is depicted in Fig. 3-21. This topology, also called  $\pi$ -type, is convenient when using bulk materials, mainly because it requires rather high material stiffness to support mechanically the mass of the top metallic clamps. Moreover, this topology is vertical and the height of a single leg is much bigger than the cross-sectional surface. This particularity privileges fabrication of the thermocouples separately.

In **CMOS** technology, the gain interest is put on the use of planar structures based on very thin materials. The most recent **MOSFET** fabrication technology **FDSOI**<sup>24</sup> also called “silicon on nothing” [Jurczak, 1999], [Jurczak, 2000], [Pretet, 2004], [Skotnicki, 2008] is using wafers with 7nm thick active **Si** layer. The composition of the **SOI** wafers is privileging the lateral structures because the ratio between vertical and lateral dimensions of the material responsible for current transport is very small. In other words, when using **SOI** wafers, the current is flowing through the thin-film **Si** horizontally consistent with a planar topology of the device.

The first planar **TEG** was proposed by [Nurnus, 2003] which was published without causing big attention at that time. However, with recent discovery of size induced  $\kappa$  reduction in **CMOS** compatible materials (described in the section 3.2.1.5.2), this topology has attained a renewed interest. The example of the lateral structure evaluated in this thesis is depicted in Fig. 3-22 [Haras, 2014-b]. The planar topology favours the use of the materials with a small height to surface ratio, enabling the device fabrication using very thin materials. Thanks to the use of the very thin materials, this topology enables the integration of mechanical flexibility into the topology. This property is very important because mechanical flexibility opens a new range of applications not possible without this property *e.g.* clothes, hot pipes *etc.* The thermoelectric generator should have as high as possible thermal resistance to maintain the  $\Delta T$  across it. To maximize the thermal resistance, the long semiconducting legs should be used in the thermoelectric generators [Bierschenk, 2008]. The planar topology facilitates the use of long semiconducting legs without changing the generator height, a feature that is impossible to achieve in the  $\pi$ -type topology. Moreover, by means of such topology, it is possible to fabricate final device without the necessity of generator leg separation for performing the assembly or metallic

<sup>24</sup>**FDSOI** – Fully Depleted Silicon On Insulator the type of **SOI** wafer with extremely thin buried oxide layer under active **Si** layer. This wafer is industrially used for fabricating the planar **MOSFET** topology. **FDSOI** is also the name of the planar **MOSFET** fabrication technology.

interconnections. Planar generators also feature a smaller thickness than  $\pi$ -type topologies for the same length of semiconducting legs. This particularity may bring the generator easier to mount on the workplace or enable mounting in locations with very compact and dense infrastructure *e.g.* cars, space crafts *etc.*

Another topological innovation in thermoelectricity is the concept of large area  $pn$  junctions [[Span, 2005](#)] as shown in Fig. 3-23. This generator topology is very simple compared with traditional  $\pi$ -type or planar topology. The large area  $pn$  junction consists in two oppositely doped materials, the temperature gradient being applied along the  $pn$  junction. Near the cold side, the metallic contacts are placed to harvest the energy. The big advantage of such a topology is the fact that it can be fabricated with a very large surface compared with  $\pi$ -type generators. Secondly, by means of the thin-film materials, it is possible to integrate the  $\kappa$  reduction and mechanical flexibility into the topology. Thirdly, it is theoretically possible to harvest energy using two independent effects: the Seebeck effect and the free carrier thermal generation within the depletion zone of the  $pn$  junction. The variation of the material composition along the temperature gradient allows controlling the temperature distribution in the material. Thus, when a material with high  $\kappa$  is placed near the hot temperature, *e.g.* **Si**, the temperature drop is reduced while placing the low  $\kappa$  material near the cold temperature *e.g.* **Si<sub>x</sub>Ge<sub>1-x</sub>** will induce high temperature drop near  $T_{COLD}$ . By implementing a variation of the material composition, there is a possibility to control the temperature gradient along the generator with possibility to expand the zone where the thermal generation is highest [[Wagner, 2007](#)]. Moreover, the thermal generation of free carriers can be enhanced by introducing the structural defects into the material.

The planar equivalent for large area  $pn$  junctions is depicted in Fig. 3-24. The operation principle is the same as for large area  $pn$  junctions. Additionally, this topology allows reducing the height of the generator making it easier to install.

Topology	Equivalent circuit	Description
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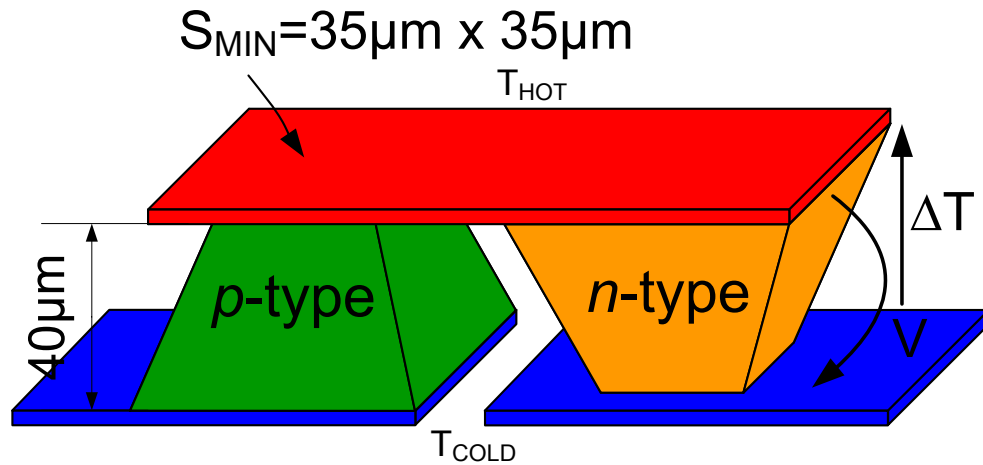
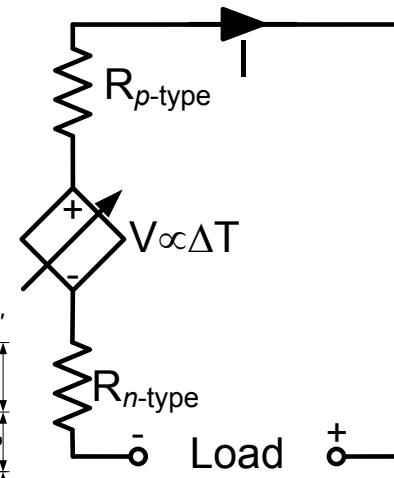


Fig. 3-21 Conventional  $\pi$ -type topology of thermoelectric generator [Micropelt GmbH, 2008]



- The semiconductors are sandwiched between hot and cold metallic plates
- The  $pn$  junction is shorted by metallic strap
- The equivalent circuit consists in series connection of two  $p$ -type and  $n$ -type rod internal resistances

The dimensions based on D-751 generator [Micropelt GmbH, 2008]

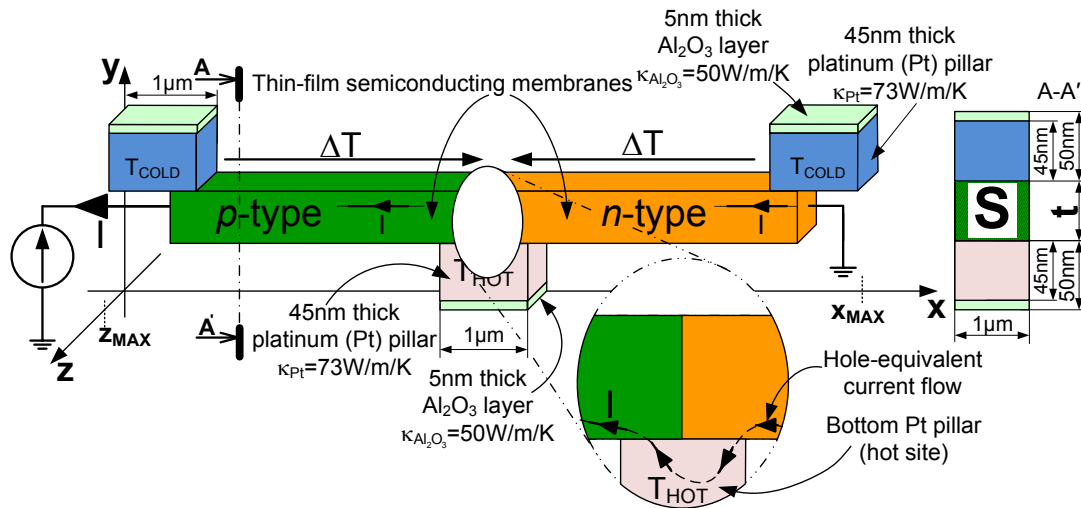


Fig. 3-22 Lateral thin-film thermoelectric generator

- Planar  $\pi$ -type structure
- The  $pn$  junction shorted by metallic contact
- Opposite temperature direction in the semiconducting legs
- Topology adapted for the use of the thin-film materials
- The legs length adjusts the thermal resistance without changing the generator's height
- Feasible in mechanically flexible version
- Reduced generator height – easy to mount

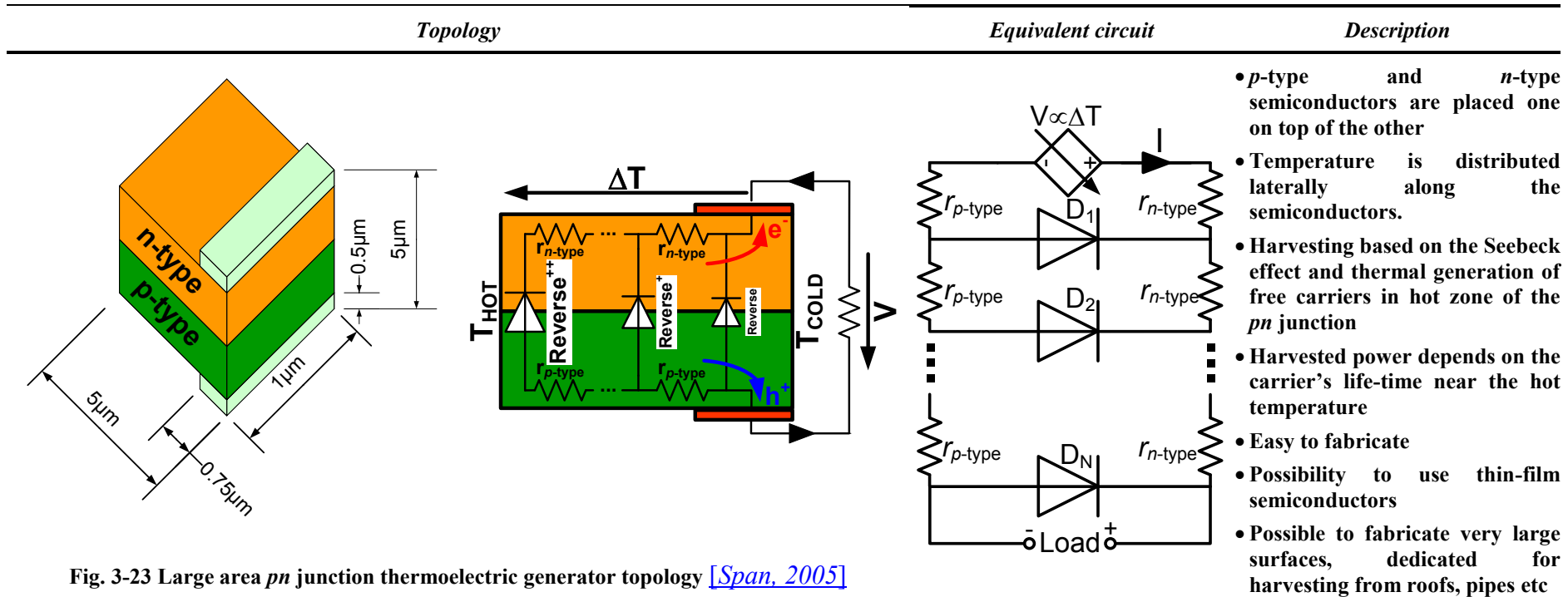


Fig. 3-23 Large area *pn* junction thermoelectric generator topology [Span, 2005]

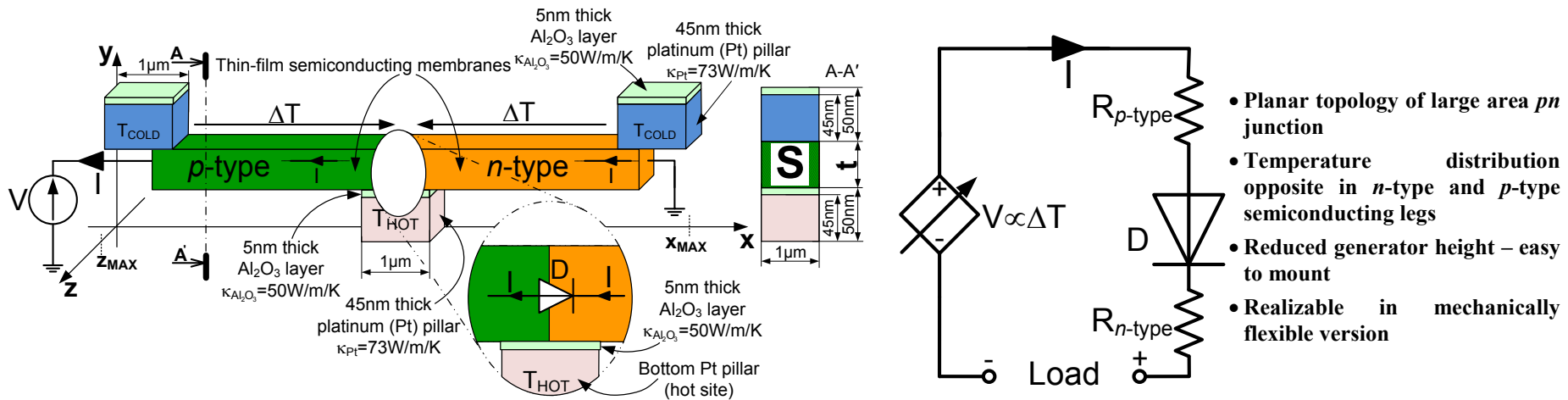


Fig. 3-24 Lateral thermovoltic thermoelectric generator



From the electrical analysis of the presented topologies, the described structures can be divided into two groups. The first composed from the classic  $\pi$ -type generator (Fig. 3-21) and lateral thermoelectric generator (Fig. 3-22) can be represented by temperature controlled voltage source of internal resistance  $R_{p\text{-type}}+R_{n\text{-type}}$  as it is presented on the electrical equivalent circuit. The shorting of the  $pn$  junction results in the electric series connection of two internal resistances of the  $p$ -type and  $n$ -type rods.

The second group is formed from large area  $pn$  junction (Fig. 3-23) and a lateral thermovoltaic generator (Fig. 3-24). In both of those structures, the electric current path goes through the  $pn$  junction. In the topology depicted in Fig. 3-23, the diode is spatially distributed upon a temperature gradient, which means that the electric equivalent circuit consists in a series combination of diodes submitted to different thermal work conditions. Thus, the electric equivalent circuit consists in distributed parallel connected diodes sandwiched between distributed electrical resistances of  $p$ -type and  $n$ -type semiconducting rods. The particularity of this group is that the harvested current is the reverse current of each contributing diode. The equivalent electric circuit for the lateral thermovoltaic generator (Fig. 3-24) differs from the electric representation of large area  $pn$  junction. The difference comes from the assumption that the  $pn$  junction is maintained at a constant temperature. This assumption is close to reality considering that the metallic contact under the  $pn$  junction is much wider than the width of the depletion zone formed in the  $pn$  junction. Like for large area  $pn$  junction, the harvested current in those generators flows in reverse direction through the diode. The diode resistance in reverse direction is very high resulting in a very high overall resistance of the generator.

### 3.3.1 Electrical performance evaluation of the **TEG** – the model

In section 3.2.1, the analytical modelling of the material thermoelectric parameters was described. However, materials were considered as absolute independent media (look Fig. 3-1). In this section, the electrical modelling of **TEG** as a complete device is presented. The **TEG** simulations are performed only on a single thermocouple. In practical implementations, the complete thermoelectric device consists in numerous thermocouples electrically arranged in series and thermally associated in parallel in terms the output voltage to the operational level of few volts as it is depicted in Fig. 2-44c.

#### 3.3.1.1 Modelling of **TEG** with shorted $pn$ junction

The current path in  $\pi$ -type generator is depicted in Fig. 2-44b and for lateral thin-film generator in Fig. 3-22. The current densities are calculated using a non-isothermal drift-diffusion model [Wachutka, 1990] Eq. 3-21. Eq. 3-21 is the transformation of the classical drift-diffusion model assuming that the material temperature is not constant. In this case, the thermoelectric effect occurs (see section 2.5.1.1), this model therefore includes the appearance of the thermoelectric effect in the current continuity equations. The variations of the quasi-Fermi levels ( $\phi_{Fn}$ ,  $\phi_{Fp}$ ) (Eq. 3-22) the thermopower coefficients ( $S_n$ ,  $S_p$ ) (Eq. 3-16), the electrical conductivities ( $\sigma_n$ ,  $\sigma_p$ ) Eq. 2-17, the carrier mobilities ( $\mu_n$ ,  $\mu_p$ ), the concentrations ( $n$ ,  $p$  and  $n_i$ ) and the effective density of states in the conduction ( $N_C$ ) and in the valence ( $N_V$ ) bands are implicitly considered as dependent on the local lattice temperature ( $T$ ) and on doping concentrations ( $N_A$  or  $N_D$ ). The detailed description, results presentation and of the used analytic models can be found in:

- Section 3.2 the modelling of electron, holes, intrinsic concentrations  $n$ ,  $p$ ,  $n_i$
- Section 3.2.1.2 the modelling of electrical conductivity  $\sigma_n$  and  $\sigma_p$
- Section 3.2.1.3 the modelling of thermopower  $S_n$  and  $S_p$

The component parameters enable the calculation of the current densities in thermoelectric generator following Eq. 3-21.

$$\begin{cases} \vec{j}_n(T) = -\sigma_n(T) \cdot [\vec{\nabla} \phi_{Fn}(T) - S_n(T) \cdot \vec{\nabla} T] \\ \vec{j}_p(T) = -\sigma_p(T) \cdot [\vec{\nabla} \phi_{Fp}(T) - S_p(T) \cdot \vec{\nabla} T] \end{cases} \quad \text{Eq. 3-21}$$

with:

$$\begin{cases} \phi_{Fn}(T) = \varphi - \frac{k_B \cdot T}{q} \ln\left(\frac{n(T)}{n_i(T)}\right) \\ \phi_{Fp}(T) = \varphi + \frac{k_B \cdot T}{q} \ln\left(\frac{p(T)}{n_i(T)}\right) \end{cases} \quad \text{Eq. 3-22}$$

$$\begin{cases} \sigma_n(T) = q \cdot \mu_n(T) \cdot n(T) \\ \sigma_p(T) = q \cdot \mu_p(T) \cdot p(T) \end{cases} \quad \text{Eq. 2-17}$$

$$\begin{cases} S_n(T) = -\frac{k_B}{q} \cdot \left[ \frac{3}{2} + \ln\left(\frac{N_c(T)}{n(T)}\right) \right] \\ S_p(T) = \frac{k_B}{q} \cdot \left[ \frac{3}{2} + \ln\left(\frac{N_v(T)}{p(T)}\right) \right] \end{cases} \quad \text{Eq. 3-16}$$

where

$\phi_{Fn}; \phi_{Fp}$  Quasi Fermi levels for electrons and holes respectively (V)  
 $\varphi$  Applied electric potential (in Coulomb's gauge)

It is worth noting that the current density described by the Eq. 3-21 is independent of the thermal conductivity ( $\kappa$ ).

To obtain comparable thermal working conditions for all simulated materials and generators topologies, the  $\Delta T$  across the generator is considered to be constant.

$$T_{HOT} - T_{COLD} = const.$$

In practice **TEGs** are installed on the hot source while the temperature drop across the generator is achieved by natural convection on the cold surface, which means that the colder surface does not have fixed temperature condition.

The theoretical current-voltage **IV** characteristic for conventional  $\pi$ -type **TEG** can be obtained by adding the **IV** characteristics depicted in Fig. 2-37a for  $n$ -type rod to that of Fig. 2-37b  $p$ -type rod. The complexity of the used model is graphically presented in Fig. 3-25 emphasizing the associated physics.

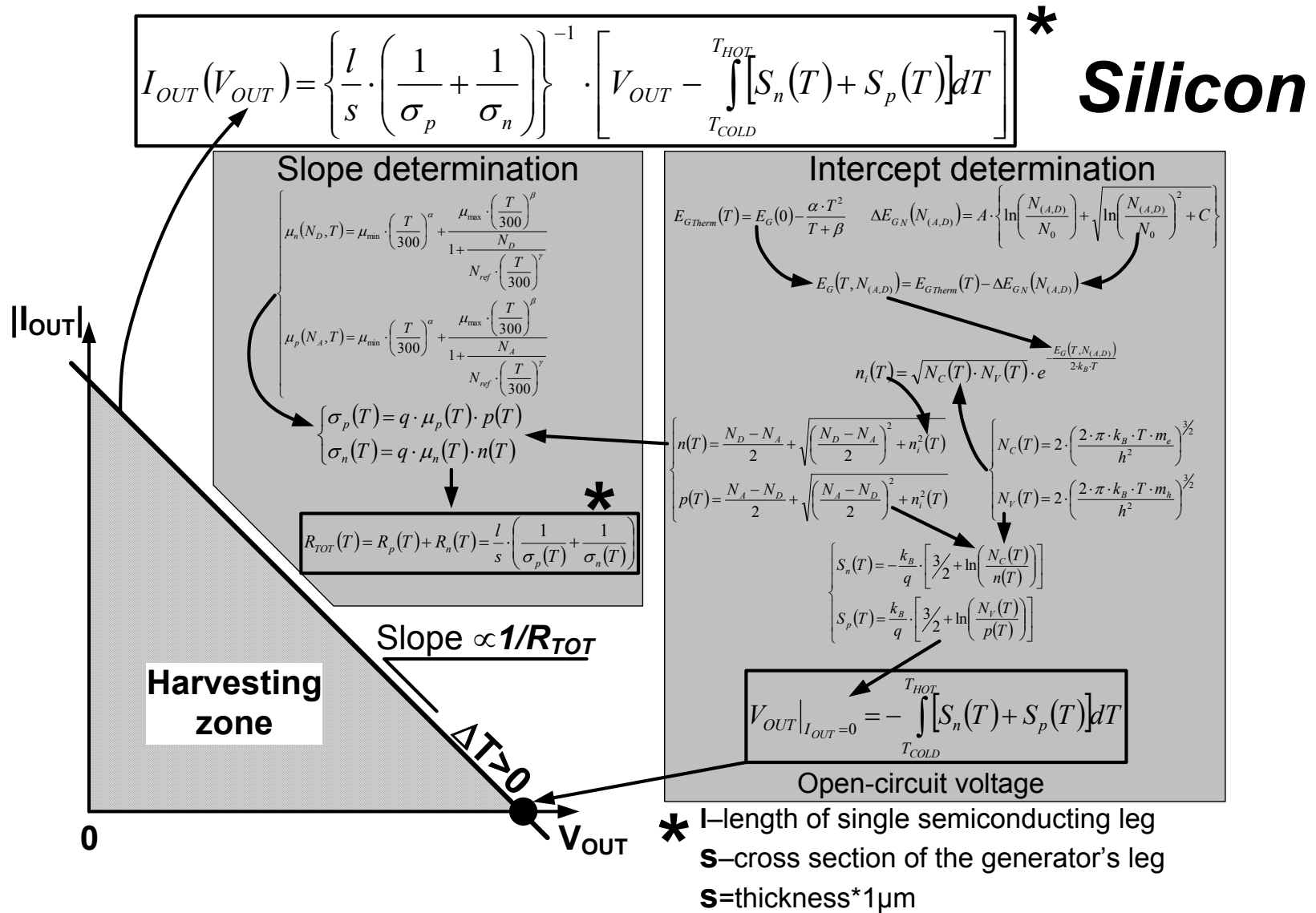


Fig. 3-25 Graphical determination of current-voltage characteristics for Silicon based  $\pi$ -type thermoelectric generators [\[Haras, 2014-b\]](#)

Fig. 3-25 illustrates the ***IV*** characteristics of the thermoelectric generator with shorted *pn* junction (*graphically presented in Fig. 3-21 or Fig. 3-22*). Those generators have a linear ***IV*** characteristic. Fig. 3-25 shows only that part of the ***IV*** characteristics where the generator is the source of electrical energy (*it is 4<sup>th</sup> quadrant, but for clarity rison the absolute value of the current is depicted  $|I_{out}|$* ). To unequivocally determine this characteristics two strategies are possible:

- Determination of two points belonging to the characteristics. Convenient in determining the short circuit current and open circuit voltage.
- Determination of one point belonging to the characteristics and the characteristic slope.

The modelling of the ***IV*** characteristics is performed using the second option.

Fig. 3-25 reveals the complexity and number of material parameters involved in the physical effects taken into consideration to realistically evaluate the electrical capabilities of ***TEGs***. Studying Fig. 3-25 leads to the conclusion that the ***IV*** characteristics formula is determined in two steps. In the first one, the open-circuit voltage is calculated considering the thermal- and doping-induced band gap narrowing, the carrier concentrations and the thermopower.

The slope determination is based on the electrical conductivity  $\sigma$  modelling involving the temperature- and the doping- impact on the (i) carrier mobilities  $\mu_p$  and  $\mu_n$ , (ii) carrier concentrations  $n$ ,  $p$ , the conductivities together with dimensionality of the generator legs allow calculating the total internal resistance  $R_{TOT}$  of the ***TEG***. The slope of the ***IV*** characteristics is the inverse value of the  $R_{TOT}$ .

Fig. 3-25 presents the modelling procedure for thermo-generators with shorted *pn* junction shows the calculations for ***Si***. For other modelled materials ***Ge*** and ***Si<sub>x</sub>Ge<sub>1-x</sub>*** different models have to be employed. However, the calculation procedure is the same for all modelled materials.

### 3.3.1.2 *Modelling thermo-generators with pn junction*

The electrical modelling of the structures with *pn* junctions is much more complicated than for conventional topologies. The difficulty in constructing the analytic model of the topologies like large area *pn* junction or lateral thermovoltaic generator is the presence of diode in the structure. Thus, in contrary to topologies without *pn* junction, for those types of thermo-generators, the modelling is performed using the Atlas<sup>®</sup> simulation environment, a product of Silvaco Inc.

### 3.4 Evaluation of the thermoelectric harvesting capabilities

In this section, the harvesting capability of the investigated structures is presented. Firstly, the results for generators with shorted  $pn$  junction will be discussed and analysed, followed by the evaluation of the electrical performance of  $pn$  junction-based generators.

#### 3.4.1 Energy harvesting in generators with shorted $pn$ junction

Using the calculation procedure depicted in Fig. 3-25 enables the evaluation of the electrical behaviour for the topologies presented in Fig. 3-21 or Fig. 3-22. However, it has to be underlined that theoretically the harvesting performance of the  $\pi$ -type (Fig. 3-21) and of the lateral thin-film thermoelectric generator (Fig. 3-22) are identical when using the same materials, submitted to the same  $\Delta T$  and with equal semiconducting leg dimensions. In other words, there is no topological impact on the theoretical harvested power density when considering the  $\pi$ -type and lateral thin-film topology. This observation is the result of the assumption that  $T_{HOT}-T_{COLD}=const.$  which means that the electric behaviour is independent of the thermal conductivity  $\kappa$ . Knowing that the electricity produced in  $\pi$ -type generator (Fig. 3-21) and lateral thin-film **TEG** (Fig. 3-22) is equal, the results obtained only in the lateral topology Fig. 3-22, with semiconducting material thickness of  $t=50\text{nm}$ , will be presented in the following. The choice of this thickness is not random. This thickness is close to the **Si** thickness in **SOI** wafers used in the technological part of this thesis. Moreover, the **Si** thickness of  $t=50\text{nm}$  also benefits from the size induced  $\kappa$  reduction (described in the section 3.2.1.5.2) which will improve the **TEG** efficiency.

One of the most important parasitic parameter in the **TEG** topology is the contact resistance between the metallic contact and the semiconductor. In **TEG** based on bulk materials, this contact resistance plays a negligible role. However, when the active material dimensions are very small, the role of the contact resistance is crucial. The metal-semiconductor (**m-s**) specific contact resistivity ( $\rho_{cont}$ ) is significantly dependent on the doping level of the semiconductor. For heavily doped semiconductors, the **m-s** contact features an ohmic character while for lightly doped semiconductors the contact exhibits a Schottky behaviour as presented in Fig. 3-26.

This important parasitic parameter represented by  $\rho_{cont}$  can have different electric behaviours. Regardless of the electric character the metal-semiconductor contact resistance it always reduces the harvesting capabilities of the **TEG**. In Fig. 3-26a the contact is ohmic due to the heavy doping of the semiconductor. These parasitic contact resistances are added to the internal **TEG** resistance represented by  $R_{p-type}$  and  $R_{n-type}$ . For lightly doped semiconductors (Fig. 3-26b) the electric behaviour of the **TEG** is altered by the presence of the two Schottky junctions formed at the **m-s** contacts. In addition, the harvested current is flowing through the Schottky diodes in reverse direction (Fig. 3-26b). When the **TEG** is delivering power to the load, the Schottky diodes are in the blocking state. This means that the **TEG** internal resistance is significantly increased by the resistance of Schottky diode in reverse mode.

For the same thermoelectric material and  $\Delta T$  across, the **TEG** higher current will be harvested when heavy doping is used. Semiconductors are less resistive at heavy doping and the **m-s** contact resistance is also less resistive than Schottky contacts.

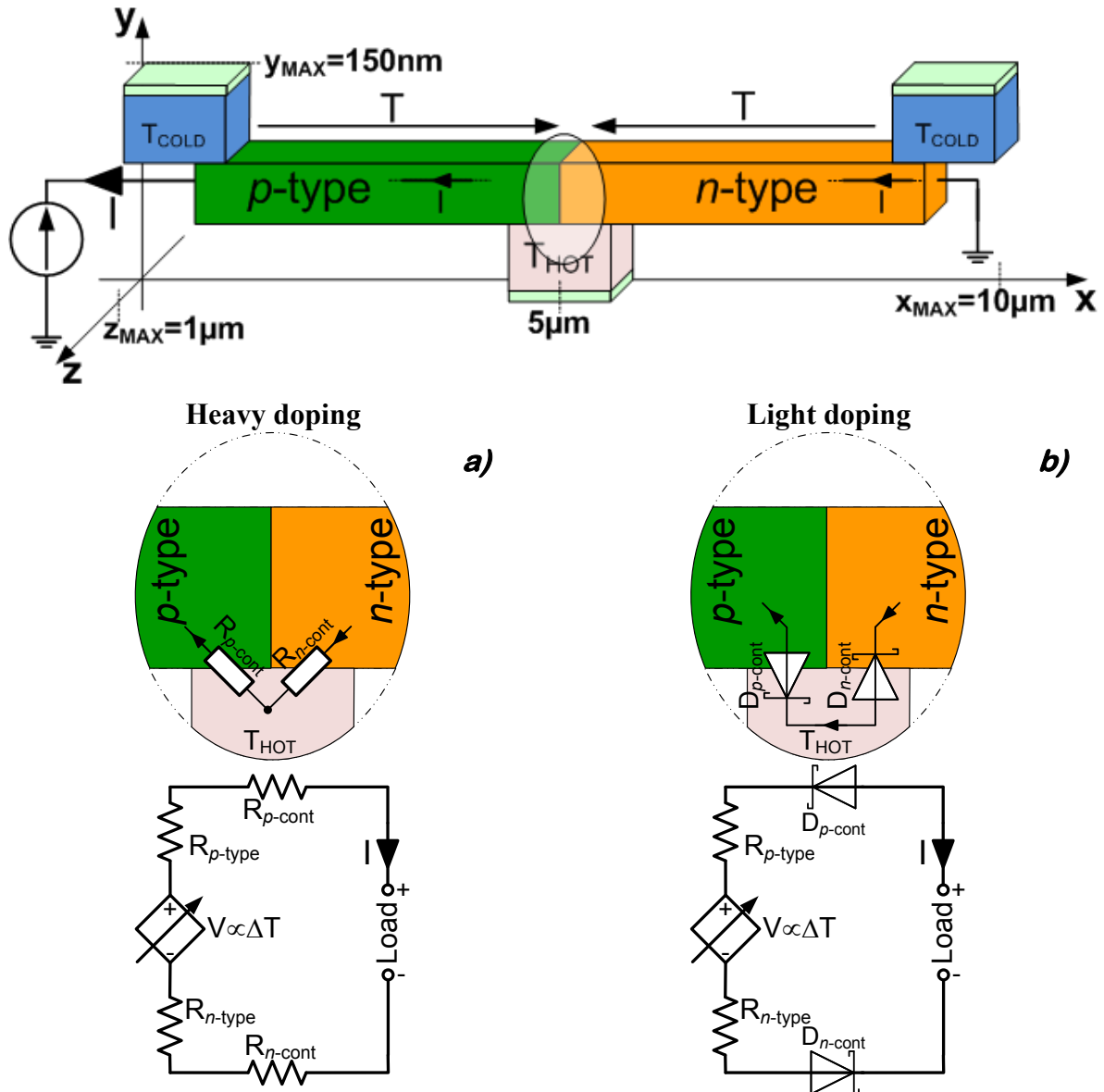


Fig. 3-26 Doping dependent metal-semiconductor contact resistance a) Ohmic contact for heavily doped semiconductors, b) Schottky contact for lightly doped semiconductors

Boosting the *TEG* performance requires the smallest possible  $\rho_{cont}$ . In digital industry the minimisation of the *m-s* contact resistance has been largely studied. For *Si* it is obtained through the introduction of thin layer of *Pt*- or *Ni*-based silicides at the junction between the *Si* and metallic contact. Thanks to this solution, the  $\rho_{cont}$  for doping level of  $N_A=N_D=10^{19}\text{cm}^{-3}$  is lowered to the level of  $\rho_{cont}=5\times 10^{-7}\Omega\cdot\text{cm}^2$  [Stavitski, 2008]. This value of  $\rho_{cont}$  is used for the modelling of *Si*-based and *Si<sub>x</sub>Ge<sub>1-x</sub>*-based *TEG* performance. Although the contact resistance to *n*-type *Ge* has remained problematic for a long time due to the strong Fermi level pinning close to the valence band, recent studies have reported that this effect is spectacularly overcome by inserting a dielectric layer between the *Ge* and metal [Lin, 2012]. Thus for this reason when modelling *Ge*-based *TEGs*, the specific contact resistance is assumed to be  $\rho_{cont}=5\times 10^{-7}\Omega\cdot\text{cm}^2$ .

Focusing on  $\rho_{cont}$  in *Bi<sub>2</sub>Te<sub>3</sub>*, the most popular thermoelectric material for low  $\Delta T$  conversion, the situation differs from *CMOS* compatible materials. The most common values of  $\rho_{cont}$  are comprised between  $1.45\times 10^{-7}\Omega\cdot\text{cm}^2$  [Venkatasubramanian, 2001] for

the very best-case situation and  $10^{-5}\Omega\cdot\text{cm}^2$  [da Silva, 2002] when standard techniques for contact realization are used.

The following of this section is organised as follows: firstly, the complete studies of **Si**-based lateral thin-film **TEG** will be presented followed by the comparison with other **CMOS** compatible materials. The benchmarking with **Bi<sub>2</sub>Te<sub>3</sub>** will also be presented.

### 3.4.1.1 Evaluation of thin-film Si-based TEG

The harvesting capabilities of the **Si**-based lateral thermoelectric generator are evaluated using the previously described procedure and models. The following results are presenting the performance of the generator only in the generator zone (Fig. 3-25). The studied **TEG** dimensions are identical for the lightly and heavily doped options and are depicted in Fig. 3-26. **Si** thickness is fixed to  $t=50\text{nm}$ . Fig. 3-27 presents the harvesting capabilities of the heavily and lightly doped **Si**-based lateral thermoelectric generator for different temperatures gradients across the generator.

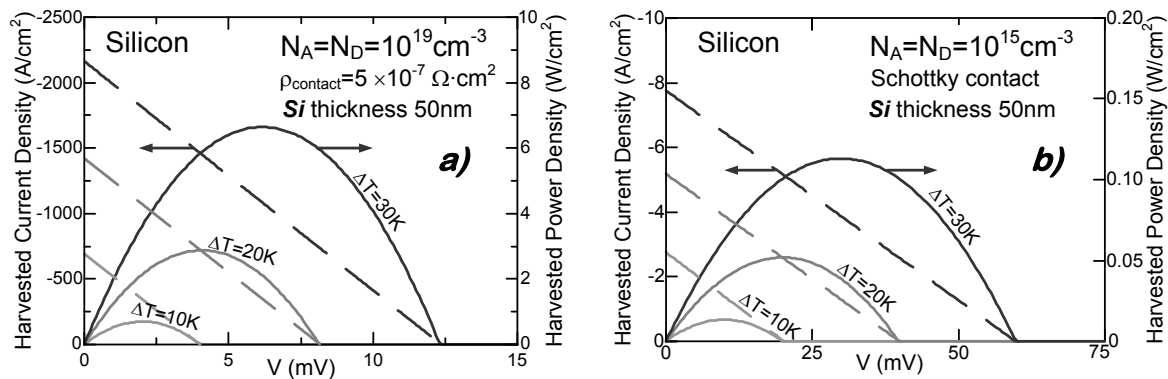


Fig. 3-27 Harvested current and power densities versus output voltage for Si-based thermoelectric generator converting from different temperature differences, a) heavily doped generator with ohmic metal-semiconductor contacts, b) lightly doped generator with Schottky contacts

Studying the harvesting performance illustrated in Fig. 3-27, it can be concluded that heavily doped generator outperforms the lightly doped counterpart. The high internal resistance of the lightly doped semiconductors together with the impact of the Schottky contacts is significantly limiting the harvested current density. However, the generator with a doping level of  $10^{15}\text{cm}^{-3}$  has higher open-circuit voltage for given  $\Delta T$ . This is the result of higher absolute value of thermopower in lightly doped semiconductor (see Fig. 3-10). In both doping level cases, the generators are exhibiting linear **IV** characteristics which confirms the shorting of the **pn** junction in this topology.

Focusing on the harvested power density, it can be remarked that for both doping levels, the harvested power has a parabolic shape. For a given  $\Delta T$ , the maximal power is attained half of the open circuit voltage which indicates that the **TEG** output power is dependent on the load resistance. For  $\Delta T=30\text{K}$ , the heavily doped generator is able to harvest  $7\text{W}/\text{cm}^2$  while lightly doped generator only  $0.12\text{W}/\text{cm}^2$ . The difference of the harvested power levels is the consequence of a higher internal **TEG** resistance and different **m-s** contacts character (*ohmic or Schottky diode*). It has to be underlined that the harvested power density calculated using this model presents the theoretical limit for **Si** and that it is calculated regardless of the variations of the thermal conductivity. However, the current and power density depicted in Fig. 3-27a is presenting **Si** under a new light. The theoretical electric capabilities of **Si** are confirming the good electric parameters of the **Si**, putting it in competitive position with the conventional thermoelectric materials.

Analyzing the equivalent circuit of the investigated **TEG** it can be remarked that for **DC** work conditions, the generator can be represented by the resistances only. Using the Thevenin theorem in the equivalent circuit depicted in Fig. 3-26a, the  $R_{load}$  for which the maximal power is extracted can be calculated. The maximum harvested power density occurs when  $R_{load}$  is equal to the internal resistance of the generator  $R_{TOT}=R_{n-type}+R_{n-cont}+R_{p-type}+R_{p-cont}$ , this is depicted in Fig. 3-28. Such particular load resistance value  $R_{load}=R_{TOT}$  is also well known as impedance matching [Bierschenk, 2008], [Heikes, 1961], [Leonov, 2009], [Lineykin, 2004], [Perez-Marin, 2014], [Rowe, 1995] or [Strasser, 2002].

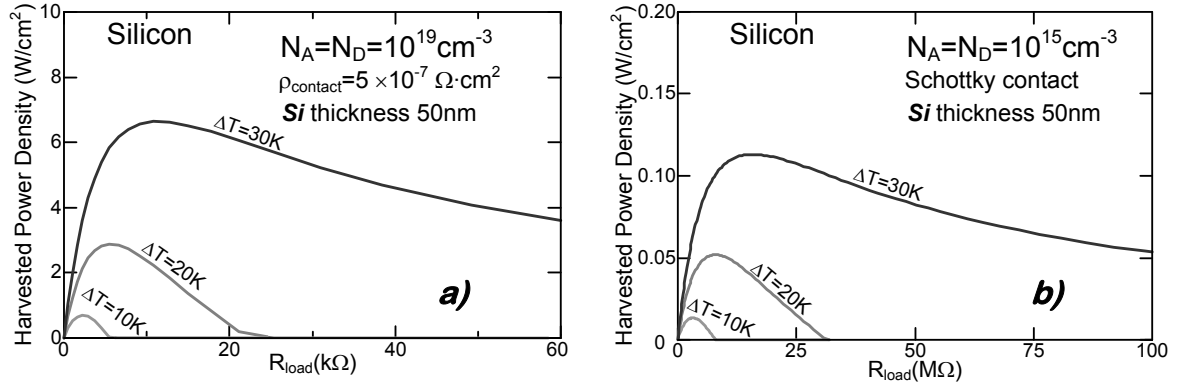


Fig. 3-28 Harvested power density versus load resistance for different temperatures, a) heavily doped generator with ohmic metal-semiconductor contacts, b) lightly doped generator with Schottky contacts

Focusing on Fig. 3-28, it can be remarked at first glance that  $R_{load}$  for heavily doped Fig. 3-28a and lightly doped Fig. 3-28b **TEGs** have different orders of magnitude. Knowing that the maximum power occurs when the  $R_{load}=R_{TOT}$ , the scaling of  $R_{load}$  in Fig. 3-28 presents directly the fact that the lightly doped generator has a significantly higher  $R_{TOT}$  than the heavily doped one. Moreover, with increasing  $\Delta T$ , the shift of optimal  $R_{load}$  value is observed towards higher values for higher  $\Delta T$ . This is mainly caused by the electrical conductivity  $\sigma$  dependence on the temperature  $T$ . Thus, rising  $\Delta T$  makes the **TEG** more resistive  $R_{TOT}$  and the optimal  $R_{load}$  are rising due to the mobility reduction.

#### 3.4.1.1.1 Thermoelectric conversion efficiency using silicon

Merging together the electrical harvesting capabilities showed in Fig. 3-28 with described size-induced thermal conductivity reduction in **Si** Fig. 3-17, enables the calculation of the efficiency ( $\eta$ ) of the **TEG** following Eq. 2-14. The heat flux  $\mathbf{Q}$  depends on the thermal conductivity  $\kappa$  and temperature  $T$  following the Fourier law Eq. 3-23:

$$\vec{Q}(T) = -\kappa(T) \cdot \vec{\nabla}T \quad \text{Eq. 3-23}$$

The efficiency for **Si**-based lateral topology for different active material thicknesses is depicted in Fig. 3-29 [Haras, 2015].

Referring to Fig. 3-29, the first remark is that  $\eta$  is rising with decreasing **Si** thickness. For  $t=10\text{nm}$ ,  $\eta$  is drastically improved 10-times over the efficiency attained for bulk **Si**. However, when focusing on the high  $\Delta T$  across the generator and the efficiency level, it has to be admitted that the thin-film and bulk **Si** are offering rather poor thermoelectric efficiencies. The solution for this problem can be the use of **Si<sub>x</sub>Ge<sub>1-x</sub>** alloys where the bulk  $\kappa$  is naturally reduced over wide range of **Si** contents ( $x$ ) (see Fig. 3-14b). Another possibility is to additionally reduce  $\kappa$ . The successive reduction of  $\kappa$  has been reported experimentally in phononic crystals structures (the network of holes patterned in thin-film



material) e.g. [Yu, 2010], [Tang, 2010], [Hopkins, 2011], [Kim, 2012]. Integrating phononic crystals in a thin-film **Si** can reduce  $\kappa$  100-times over its bulk value. Meaning that  $\eta$  in nanostructured **Si** can outperform its counterpart in the conventional materials.

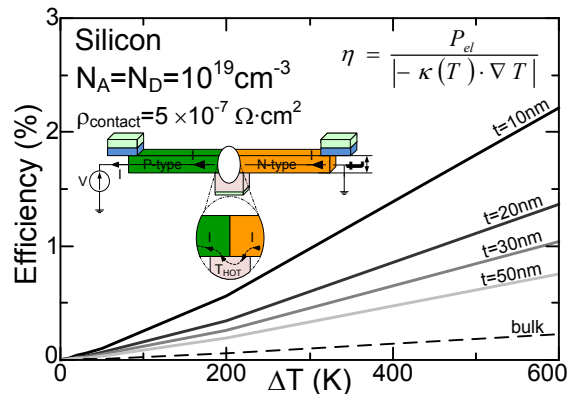
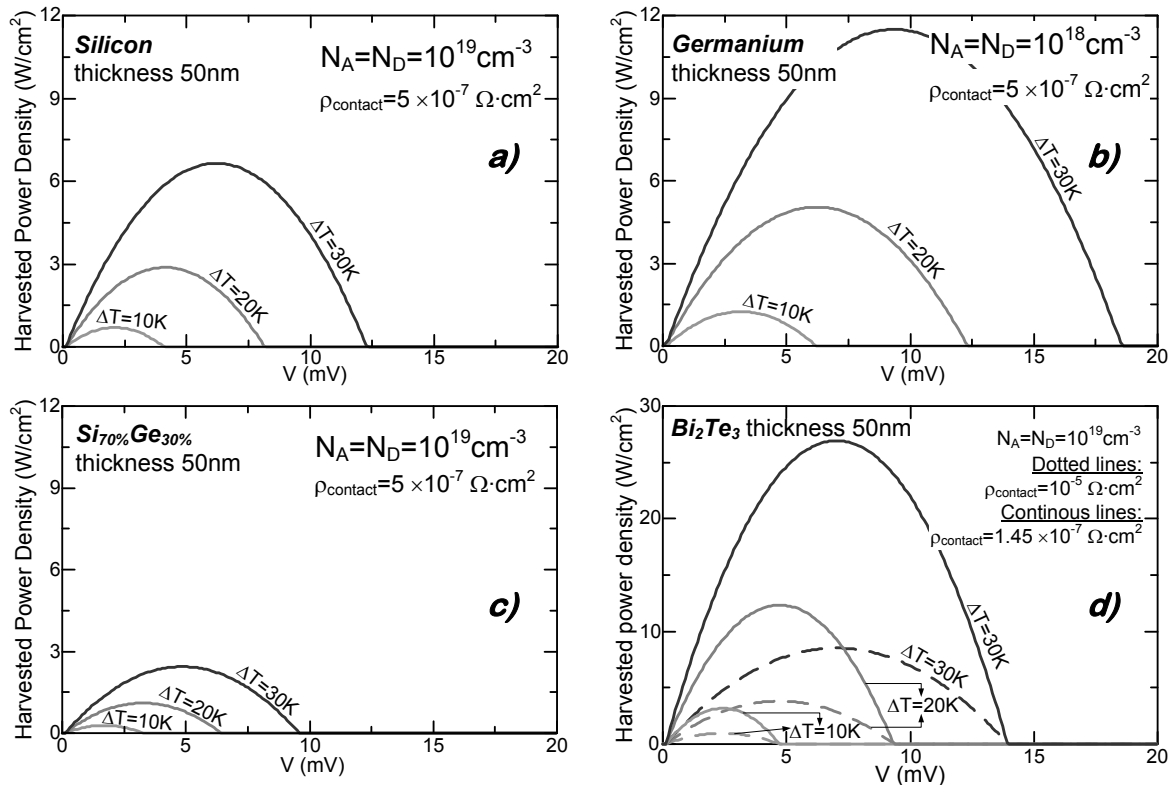


Fig. 3-29 Theoretical conversion efficiency of Si-based thermoelectric generator for different active material thickness  $t$  [Haras, 2015].

### 3.4.1.2 Harvesting capabilities: a comparison

After the accurate comparison of the harvesting performance in **Si**-based **TEG**, it is now possible to compare the thermoelectric capabilities of different materials. Knowing that harvesting is much more productive when using heavily doped semiconductors, only the heavily doped **TEGs** will be investigated in the following. Compared **TEGs** are based on materials with optimal doping level for which the maximal power factor (**PF**) is achieved. For **Si** and **Si<sub>x</sub>Ge<sub>1-x</sub>**,  $N_A=N_D=10^{19}\text{cm}^{-3}$  (see Fig. 3-13a and Fig. 3-13c), for **Ge**  $N_A=N_D=10^{18}\text{cm}^{-3}$  (see Fig. 3-13b) and the benchmark material **Bi<sub>2</sub>Te<sub>3</sub>** is doped to  $N_A=N_D=10^{19}\text{cm}^{-3}$  (see Fig. 3-13d).

Fig. 3-30 presents the harvested power densities for **Si**-, **Ge**-, **Si<sub>70%</sub>Ge<sub>30%</sub>**- and **Bi<sub>2</sub>Te<sub>3</sub>**-based lateral thin-film generators with an active material thickness of  $t=50\text{nm}$ . Focusing on the performance of **CMOS** compatible materials at a fixed  $\Delta T=30\text{K}$  across the generator, it can be concluded that **Ge** has the highest harvested power density around  $11\text{W}/\text{cm}^2$  Fig. 3-30b, followed by the **Si** with  $7\text{W}/\text{cm}^2$  Fig. 3-30a and the lowest harvested power is extracted from **Si<sub>70%</sub>Ge<sub>30%</sub>** around  $3\text{W}/\text{cm}^2$  Fig. 3-30c. The high performance of **Ge** is the result of very high electrical conductivity  $\sigma$  (look Fig. 2-40) and thermopower **S** (look Fig. 3-10). It is very important to note that **Ge** has well defined peak value of **PF** (look Fig. 3-13b) which means that when using a different doping level than  $10^{18}\text{cm}^{-3}$ , the harvested power density is radically reduced, making **Ge** the less attractive. Concerning **Si<sub>70%</sub>Ge<sub>30%</sub>**, it has to be underlined that despite the lowest harvested power density it will offer the highest conversion efficiency due to the natural reduction of  $\kappa$  which, in bulk **Si<sub>x</sub>Ge<sub>1-x</sub>**, is significantly lower than in nanostructured **Si** or **Ge**. The lowest harvested power density in **Si<sub>70%</sub>Ge<sub>30%</sub>** is the result of reduced carrier mobilities (see Fig. 3-8) compared with pure **Si** or **Ge** due to the presence of strain and defects in the lattice. Harvested power density extracted from **Bi<sub>2</sub>Te<sub>3</sub>**-based **TEG** Fig. 3-30d clearly shows the impact of the contact resistance on the **TEG** performance. When conventional technologies for contact fabrication are used, the maximal harvested power density for  $\Delta T=30\text{K}$  is around  $10\text{W}/\text{cm}^2$ . This value is almost tripled when modern sophisticated and efficient contact fabrication methods are used. It can be assumed that the performance of commercial **Bi<sub>2</sub>Te<sub>3</sub>**-based **TEGs** are comprised between the dotted and continuous lines depicted in Fig. 3-30d.



**Fig. 3-30** Harvested power density versus output voltage at different temperature differences extracted from the lateral thin-film thermoelectric generator based on: a) Silicon, b) Germanium, c)  $\text{Si}_{70\%}\text{Ge}_{30\%}$  analytical model based on [Dismukes, 1964] and [Slack, 1991], d)  $\text{Bi}_2\text{Te}_3$  analytical model based on [Luo, 2012]

The outcome and conclusion drawn from Fig. 3-30 is that **CMOS** compatible materials (especially **Si** and **Ge**) are offering comparable power density level to conventionally processed  **$\text{Bi}_2\text{Te}_3$** -based **TEG**. This conclusion puts **CMOS** compatible materials in competitive position with traditional thermoelectric materials offering simultaneously the (i) harmlessness, (ii) cost reduction and (iii) industrial compatibility. However, the analysis depicted in Fig. 3-30 does not consider the impact of  $\kappa$  on the harvesting capabilities. The performance comparability between **CMOS** compatible materials and  **$\text{Bi}_2\text{Te}_3$**  is only theoretical unless high  $\kappa$  in **CMOS** compatible materials is reduced. The electrical parameters ( $\sigma$  and **S**) of **CMOS** materials together with the size induced  $\kappa$  reduction offer new possibility to popularize thermoelectricity on the market.

### 3.4.2 Energy harvesting in generators with *pn* junction

The analysis of the generators based on *pn* junctions is much more complicated than for the previously presented **TEGs**. This is due to the presence of *pn* junctions in the topology of the **TEG** and the physical effects associated to the operating mode. The topologies of large area *pn* junction (Fig. 3-23) and thermovoltaic generator (Fig. 3-24) are modelled using the Silvaco Inc. Atlas<sup>®</sup> TCAD simulation environment.

As mentioned previously the presence of *pn* junction gives the possibility to generate electrical energy using two independent physical effects:

- The thermoelectric effect,
- The thermal generation of free carriers within the depletion zone of *pn* junctions.

The modelling of the thermoelectric effect is similar to the previously described model. The thermal generation of free carriers is modelled using the **Shockley-Read-Hall (SRH) Generation-Recombination (G-R)** model [Shockley, 1952] Eq. 3-24. The calculation of the **G-R** rate requires the knowledge of the Fermi energy level Eq. 3-26, conduction band ( $E_C$ ), valence band ( $E_V$ ) Eq. 3-27 and intrinsic ( $E_i$ ) Eq. 3-28 energy levels. The first energy to determine is the Fermi energy for the electrons ( $E_{Fn}$ ) and the holes ( $E_{Fp}$ ), which is calculated transforming the general definition of thermopower Eq. 2-25. The determination of  $E_C$  and  $E_V$  is established referring on the  $E_{Fn}$  and  $E_{Fp}$ .

The equations from Eq. 3-25 to Eq. 3-28 contribute directly or indirectly in the calculation of the generation-recombination rate (**G-R**) Eq. 3-24.

$$G - R = \frac{p(T) \cdot n(T) - n_i^2(T)}{\tau_p \cdot \left[ n(T) + n_i(T) \cdot \exp\left(\frac{E_t - E_i(T)}{k_B \cdot T}\right) \right] + \tau_n \cdot \left[ p(T) + n_i(T) \cdot \exp\left(\frac{E_i(T) - E_t}{k_B \cdot T}\right) \right]} \quad \text{Eq. 3-24}$$

With:

$$\begin{cases} \tau_p = \tau_{p0} \cdot \left(\frac{T}{300}\right)^{\alpha_p} \\ \tau_n = \tau_{n0} \cdot \left(\frac{T}{300}\right)^{\alpha_n} \end{cases} \quad \text{Eq. 3-25}$$

$$\begin{cases} E_{Fn}(T) = q \cdot \int_T S_n(T) dT \\ E_{Fp}(T) = q \cdot \int_T S_p(T) dT \end{cases} \quad \text{Eq. 3-26}$$

$$\begin{cases} E_c(T) = E_{Fn}(T) - \frac{k_B}{q} \cdot \ln\left(\frac{n(T)}{N_C(T)}\right) \\ E_v(T) = E_{Fp}(T) + \frac{k_B}{q} \cdot \ln\left(\frac{p(T)}{N_V(T)}\right) \end{cases} \quad \text{Eq. 3-27}$$

$$E_i(T) = \frac{E_c(T) + E_v(T)}{2} - \frac{k_B \cdot T}{2 \cdot q} \cdot \ln\left(\frac{N_C(T)}{N_V(T)}\right) \quad \text{Eq. 3-28}$$

where:

<b>G-R</b>	Recombination rate ( $\text{cm}^{-3} \cdot \text{s}^{-1}$ )
$E_t$	Trap energy level (eV)
$E_i$	Intrinsic energy level (eV)
$\tau_n, \tau_p$	Electron and hole carrier life time respectively (s)
$n_i$	Intrinsic concentration ( $\text{cm}^{-3}$ )
$n; p$	Electron and hole concentration respectively ( $\text{cm}^{-3}$ )
$E_C, E_V$	Conduction and valence band energies
$E_{Fp}, E_{Fn}$	Fermi energy level for holes and electrons respectively (eV)
$N_C, N_V$	Density of states in conduction and valence bands respectively ( $\text{cm}^{-3}$ )
$k_B$	Boltzmann constant
$T$	Temperature (K)
$q$	Magnitude of electronic charge ( $1.6 \cdot 10^{-19}$ C)

**G-R** describes the number of electron/holes pairs per unit of time excited from lower energetic states to the conduction/valence band. When **G-R** is positive the dominant generation of free holes and electrons occurs, thus the number of free carriers contributing

to current transport is increased. For negative **G-R**, the recombination is dominant and the inverse situation occurs, because carriers are trapped to recombine in a lower energy state. This short definition shows that generation-recombination processes are mainly affecting the electrical conductivity  $\sigma$  and thermopower **S** by altering the hole (**p**) and electron (**n**) concentrations. The inspection of Eq. 3-24 shows that **G-R** depends on the material parameters represented by  $E_t$ ,  $\tau_p$  and  $\tau_n$ .  $E_t$  is the trap energy level, resulting from the presence of crystal defects. Due to the traps, it is easier for the carrier to cross the band gap energy  $E_G$ . Placing  $E_t$  in the middle of the band gap creates the most efficient generation-recombination centre. The hole and electron life times, ( $\tau_p$ ) and ( $\tau_n$ ) respectively, are defining the efficiency of the **G-R** mechanism. The carrier life-times also reflect the order/disorder in the atomic material's structure. For instance, material without defects features the very long  $\tau_p$  and  $\tau_n$  are of crystalline materials.

The zone where generation-recombination plays a major role is the depletion zone of the *pn* junction. When the *pn* junction is formed from heavily doped *p*-region and *n*-region the depletion zone width is very small. The opposite situation occurs when using lightly doped *n*-type and *p*-type semiconductors. To increase the number of thermally generated carriers, the depletion zone should be as wide as possible. This is possible when using lightly doped *n*-type and *p*-type regions. However, in such case the internal **TEG** resistance is large which results in significant reduction of the harvested current. The antagonist behaviour between the enhancement of the thermal **G-R** of free carriers and electrical conductivity significantly increases the complexity of optimisation.

In this section only the results for the **Si**-based large area *pn* junctions and for the **Si**-based thermovoltaic generator will be presented, compared and discussed.

#### 3.4.2.1 Harvesting capabilities of large area *pn* junction

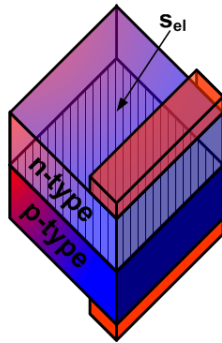
The large area *pn* junction harvested power density is significantly dependent on the generation-recombination rate. **G-R** in Eq. 3-24 is boosted when small  $\tau_n$  and  $\tau_p$  (*materials with high lattice defects densities*) and low doping level is used.

The topology associated to the large area *pn* junction design has different cross-sectional surfaces for heat and current transport as depicted in Fig. 3-31. Using the cross-section surface  $s_{el}$  presented in Fig. 3-31a enables the calculation of the harvested power density Fig. 3-32.

At first glance, the analysis of Fig. 3-32 reveals that the harvested power density is very small compared to the previously described lateral thin-film **TEG** topology (*refer to Fig. 3-27*). For a high  $\Delta T=200K$ , the maximum harvested power density is around  $0.4W/cm^2$  and  $0.27 \times 10^{-3}W/cm^2$  for lightly doped and heavily doped semiconductors, respectively. Moreover the lightly doped generator Fig. 3-32a has significantly higher harvested power density than heavily doped generator Fig. 3-32b. This confirms that the width of the depletion zone plays an important role in the harvesting capabilities of this **TEG** configuration. To benchmark the simulation model with experimental data the comparison of the harvested power density reported in [*Span, 2005*] is performed in Fig. 3-32a. The experimentally characterized large area *pn* junction is  $s_{el}=2cm \times 80\mu m$  and the output power amounts to  $P_e=1.22mW$  at  $\Delta T=205K$ . **Si** has a doping level of  $N_A=N_D=10^{16}cm^{-3}$ , no information about carrier life-time is provided. Despite the slight differences in  $\Delta T$  and doping level, it can be concluded that the measured and simulated

peak power are on the same order of magnitude which confirms the small harvesting capabilities of thermo-generators based on this principle of operation.

Active material cross-section for current



Active material cross-section for heat

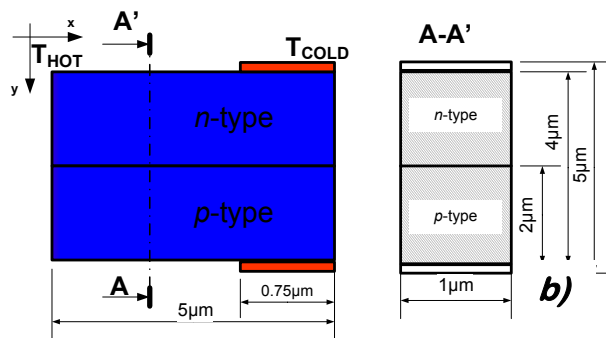


Fig. 3-31 Identification of cross-section surface of active material when transporting, a) current, b) heat

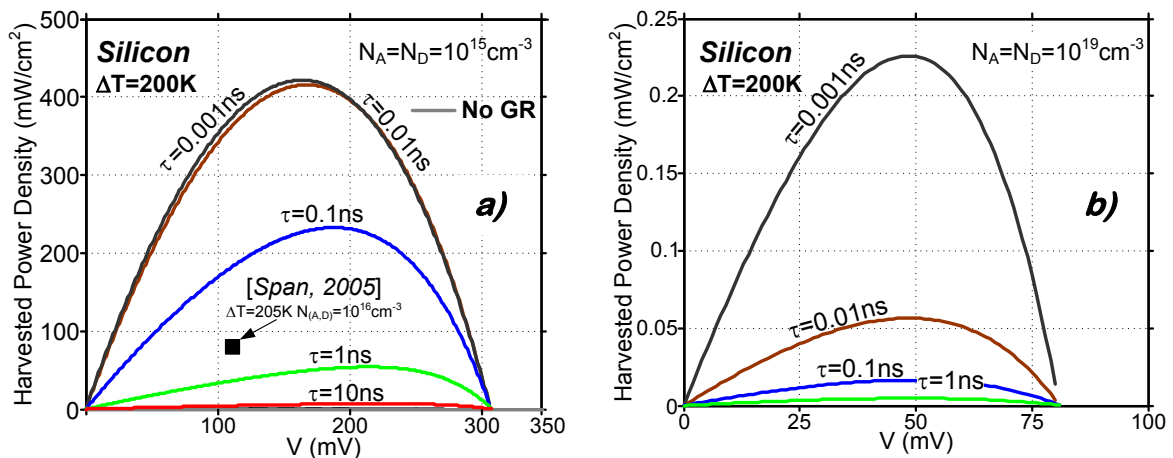


Fig. 3-32 Harvested power density versus output voltage for different carrier life-times a) doping level of  $10^{15} \text{cm}^{-3}$ , b) doping level of  $10^{19} \text{cm}^{-3}$

Compared with the harvested power density for different carrier life times, it is visible that when the carrier life time decreases, the harvested power increases. This is caused by the fact that when  $\tau_p$  and  $\tau_n$  are short this represents high density of structural defects which are facilitating the generation-recombination processes. Moreover, for **TEG** simulated without **SRH** generation-recombination model, the harvested power density is negligible as shown in Fig. 3-32a. This observation allows to conclude that power density depicted in Fig. 3-32 totally comes from the thermally generated free carriers within the depletion zone. The power provided by thermoelectric effect is negligibly small compared with the power produced by the **SRH** process.

From the analysis of the harvested power density level at  $\Delta T=200\text{K}$  (Fig. 3-32), it can be concluded that the **TEG** efficiency is very poor. Calculating the efficiency of the **TEG** requires the information about the heat flux  $\mathbf{Q} = -\kappa(T) \cdot \nabla T$  Eq. 3-23 which is calculated from the knowledge of the temperature gradient Fig. 3-31b (along the  $x$ -axis).  $\mathbf{Q}$  is calculated taking into account the dependency of  $\kappa$  on the local lattice temperature following Eq. 3-18 and assuming that the  $T_{HOT}$  and  $T_{COLD}$  are constant. The large area  $pn$  junction efficiency for  $\Delta T=200\text{K}$  is illustrated in Fig. 3-33:

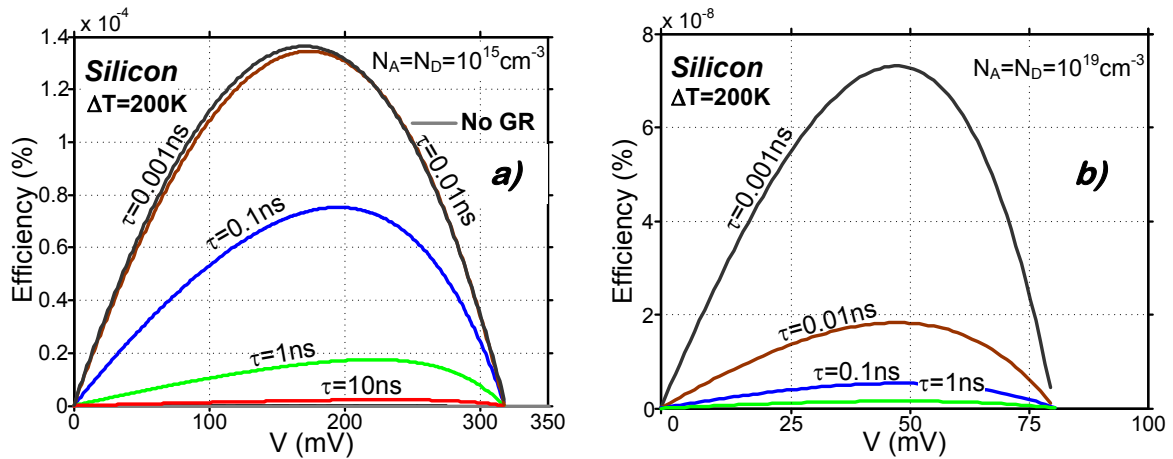


Fig. 3-33 Efficiency of large area  $pn$  junction for  $\Delta T=200\text{K}$ , different carrier life-times and a) lightly doped Silicon, b) heavily doped Silicon

The calculated efficiency depicted in Fig. 3-33 confirms that the harvesting performance of the large area  $pn$  junction topology is very poor. The lightly doped **TEG** features conversion efficiency  $10^4$  higher than its heavily doped counterpart. However, regardless of this observation, it is clear to note that the conversion efficiency level for the large area  $pn$  junction topology is placing this type of **TEG** in a disadvantageous position compared with the conventional  $\pi$ -type or lateral thin-film **TEG** topologies.

### 3.4.2.2 Harvesting capabilities of thermovoltaic generator

Fig. 3-34 presents the dimensional design of the modelled thermovoltaic generator topology. To obtain a full comparison between both the lateral thin-film thermoelectric generator and the thermovoltaic generator are taken with equal dimensions.

Taking into account the dimensions of the **TEG** illustrated in Fig. 3-34, it has to be remarked that due to the localized source of heat directly below the  $pn$  junction and the small thickness of the active material ( $t=50\text{nm}$ ), the diode can be considered as operating in isothermal conditions. Distinguishing this topology from the topology of large area  $pn$  junction depicted in Fig. 3-23.

Due to the presence of the  $pn$  junction the **IV** characteristics of the generator is not linear contrary to the case of the lateral thin-film thermoelectric generator (look Fig. 3-27). Fig. 3-35 presents the **IV** characteristics of thermovoltaic generator.

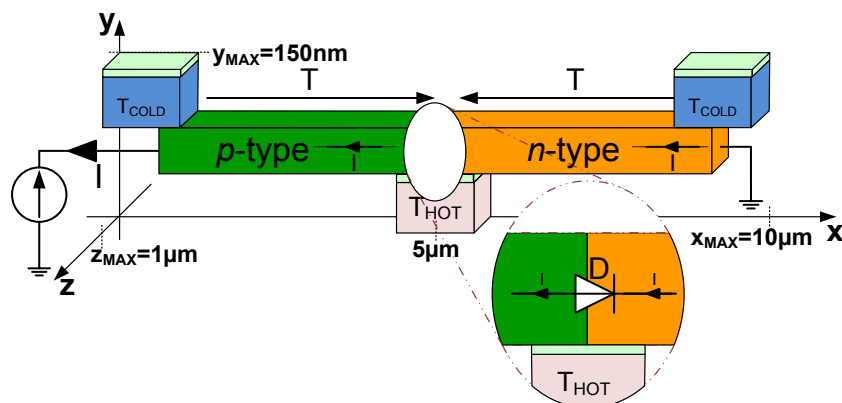


Fig. 3-34 Schematic representation of thermovoltaic generator with active material thickness of 50nm

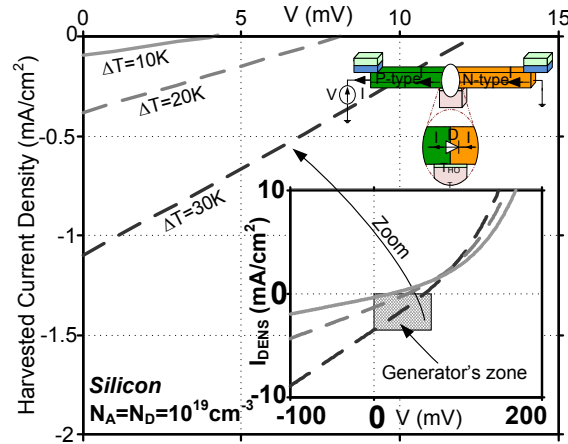


Fig. 3-35 *IV* characteristics for the thermovoltaic generator in the 4<sup>th</sup> quadrant and zoom-out to capture the complete characteristics

In the inset of Fig. 3-35 the complete characteristics of the thermovoltaic generator taken at several  $\Delta T$  are illustrated. The *IV* characteristic is non-linear and has shape comparable to diode. The application of the temperature under the *pn* junction displaces the *IV* characteristics towards higher absolute values of the reverse current (*negative current values*). This behaviour is comparable to photovoltaic diode (*compare with Fig. 2-25*). The increase of thermally induced reverse current creates a generator zone where the current and the voltage have opposite sign. Within this zone, the energy is extracted from the generator and delivered to the load. Comparing current density in Fig. 3-35 and in Fig. 3-27a for both heavily doped *TEGs*, it can be remarked that the thermovoltaic generator delivers a significantly lower harvested current density for the same  $\Delta T$ . This is the consequence of the fact that the harvested current in the topology of thermovoltaic generator is the reverse current of the diode.

Based on the above analysis, it is clear that when the *pn* junction is present in the *TEG* topology, the harvesting capabilities are significantly dependent on the generation-recombination conditions. Fig. 3-36 depicts the *IV* characteristics and the power density for  $\Delta T = 30K$  for different carrier life times.

From the impact of the doping concentration on the harvesting performance, it can be concluded that for lightly doped *TEG* the harvested current and power densities are outperforming the heavily doped generator. The explanation of this fact relies on the free carriers thermal generation enhancement when using light doping caused by the extension of the depletion zone width. The influence of the carrier life-time exhibits same behaviour as already observed for large area *pn* junction. For the short life-times the harvesting performance are increased.

The peak harvested power density for lightly doped generator equals  $\sim 280 \mu W/cm^2$  and is attained for  $\tau_n = \tau_p = 1ps$ . For the heavily doped generator, the peak harvested power is  $\sim 3.5 \mu W/cm^2$  also delivered when *TEG* has  $\tau_n = \tau_p = 1ps$ . Comparing these results with those of the lateral thin-film topology (*look Fig. 3-27*), it is clear that thermovoltaic generator can offer less power for same  $\Delta T$ . However, this topology is more productive than the design based on large area *pn* junction. This is caused by isothermal working conditions for the *pn* junction. The junction is not distributed over all range of  $\Delta T$  applied to the *TEG*. Studying Fig. 3-36 more precisely, it can be observed that the output voltage for the weakly doped generator Fig. 3-36b is significantly higher than for the heavily doped Fig. 3-36a. This recalls to the definition of the thermopower  $S_n$  and  $S_p$  which has a higher absolute value for light doping (*look Fig. 3-10*).

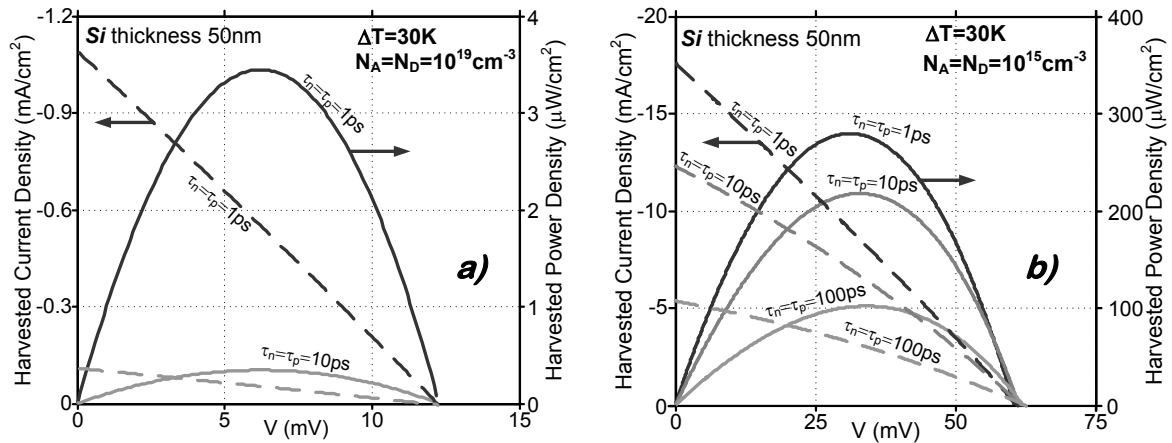


Fig. 3-36 *IV* and harvested power density for thermovoltaic generator with  $\Delta T=30K$  and different carrier life-time active material: a) lightly doped, b) heavily doped.

Contrary to the conventional **TEG** topology in this case (and to the case of large area *pn* junction), the generator performance is not dominated by electrical conductivity  $\sigma$  but by thermal generation-recombination. The generator can deliver higher power to the load when the conditions for high positive **G-R** Eq. 3-24 are fulfilled.

In the topology of thermovoltaic **TEG**, the temperature gradient can be applied in two different ways. The temperature gradient can be applied as presented in Fig. 3-34, where **T<sub>HOT</sub>** is directly placed under the *pn* junction. Opposite situation is also possible by placing **T<sub>COLD</sub>** under the *pn* junction and **T<sub>HOT</sub>** at the semiconducting rods extremities. This slight difference will impact the generator behaviour in a significant way, which is illustrated on the Fig. 3-37.

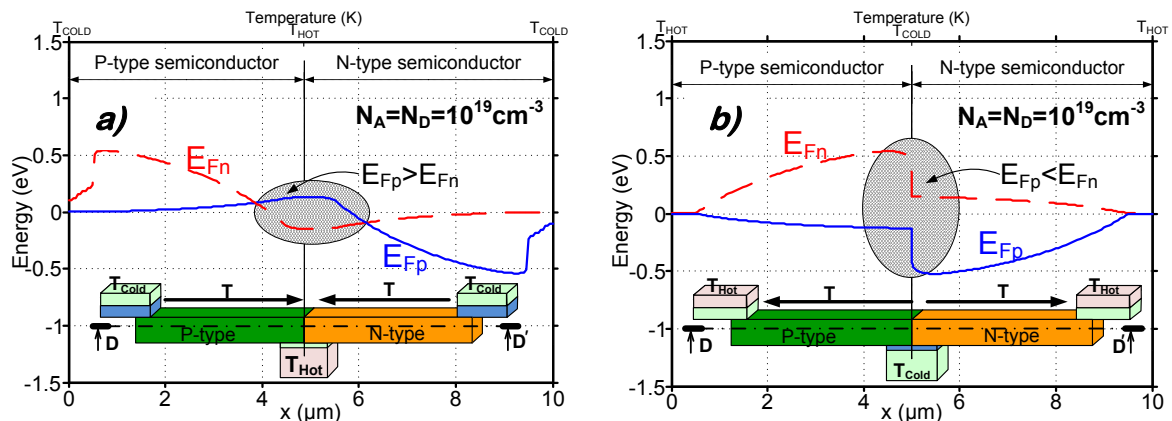


Fig. 3-37 Fermi energies for electrons  $E_{Fn}$  and holes  $E_{Fp}$  along D-D' cutline for opposite thermal gradient direction in thermovoltaic generator: a) Hot temperature under the *pn* junction, b) cold temperature under the *pn* junction

Placing the **T<sub>HOT</sub>** under the *pn* junction results in a hole quasi-Fermi energy above the quasi-Fermi energy for electrons  $E_{Fp} > E_{Fn}$  at the junction as shown in Fig. 3-37a. The opposite situation occurs when the **T<sub>COLD</sub>** is applied directly under the *pn* junction Fig. 3-37b. Referring to the basic diode physics [Grundmann, 2010], [Neamen, 2003], [Opolski, 2002], [Pierret, 1996] or [Sze, 2007] when the diode is in blocking state, within the depletion zone  $E_{Fp} > E_{Fn}$ , while when inside the depletion zone the  $E_{Fp} < E_{Fn}$  the diode is in conduction state. Fig. 3-37a) presents the thermally induced retardation of diode conduction state when the **T<sub>HOT</sub>** is placed directly under the *pn* junction. In other words, the diode is pushed deeper into the reverse state. Fig. 3-37b illustrates the acceleration of the diode conduction state meaning that the diode is pushed in anticipation towards the



conduction state. This situation reflects on the  $IV$  characteristic which is graphically represented in Fig. 3-38.

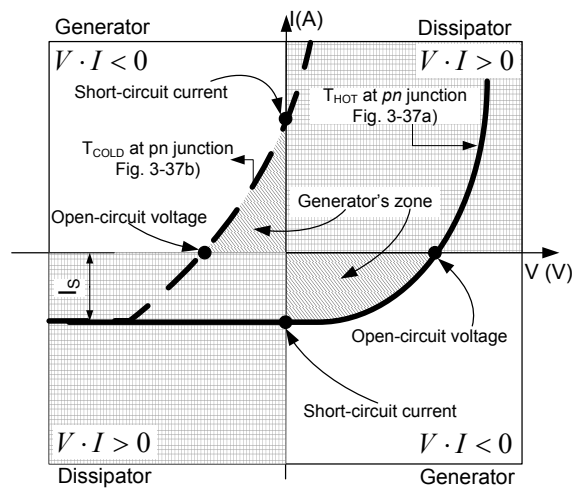


Fig. 3-38 Sketch of  $IV$  characteristic for thermovoltaic generator when  $T_{HOT}$  under  $pn$  junction (continuous line) and  $T_{COLD}$  under  $pn$  junction (dashed line)

Fig. 3-38 illustrates graphically the thermally induced acceleration (dashed line) and retardation (continuous line) of the diode conduction state. Interestingly, when the conduction state is accelerated the generator's zone is pushed to the 2<sup>nd</sup> quadrant, while in the case of retardation of conduction state creates the generator zone in the 4<sup>th</sup> quadrant.

The above described retardation of the diode conduction state occurs also in the large area  $pn$  junction by placing the junction situated at high temperature deeper in reverse mode than the junction closer to the  $T_{COLD}$  (see Fig. 3-23).

### 3.5 Summary and conclusions

In this chapter, the evaluation of the thermoelectric capabilities of **CMOS** compatible materials was presented. The enhancement of harvesting performance can be achieved through the optimisation of the thermoelectric material (*described in section 3.2*) or the thermoelectric generator topology (*described in section 3.3*).

Firstly, the evaluation of the thermal ( $\kappa$ ), electrical ( $\sigma$ ) conductivities and thermopower ( $S$ ) has been performed at the material level (*see Fig. 3-1*). The accurate temperature and doping dependent modelling for the energy band gap ( $E_G$ ), electron, holes and intrinsic concentrations ( $n$ ,  $p$  and  $n_i$ ), electrons and holes mobilities ( $\mu_n$  and  $\mu_p$ ) enables the calculation of  $\sigma$  and  $S$ . Comparison of  $\sigma$  and  $S$  in **CMOS** compatible materials with  $\text{Bi}_2\text{Te}_3$  put **CMOS** materials in the competitive position with respect to  $\text{Bi}_2\text{Te}_3$ . However, due to the high  $\kappa$  in **Si** and **Ge**, their thermoelectric performance is significantly reduced to the level which precludes their usage in thermoelectricity. The described size-induced reduction of  $\kappa$  (*see section 3.2.1.5.2*) enables competitive, cheap, harmless and industrially compatible **ThermoElectric Generators (TEGs)** fabrication.

The innovation at the topological level is described in section 3.3. Starting with the introduction of the conventional **TEG** topology (*Fig. 3-21*), the non-conventional topologies are subsequently presented. Because the **CMOS** industry favours the planar configurations, the topologies of lateral **TEGs** are proposed: (i) the lateral thin-film topology (*Fig. 3-22*) and (ii) the thermovoltaic generator topology (*Fig. 3-24*). At the first glance, those structures are identical with however a significant difference of insulation at the  $pn$  junction. For the thin-film thermoelectric generator (*Fig. 3-22*) the junction is shorted and the topology can be considered as the lateral equivalent of  $\pi$ -type generator. In the topology of thermovoltaic generator (*Fig. 3-24*), the  $pn$  junction is insulated from the metallic contact resulting in the presence of the  $pn$  junction in the **TEG** topology. Both structures enable the possibility to use thin-film materials that feature an additional size-induced  $\kappa$  reduction. Another innovative topology of **TEG** is investigated and depicted in *Fig. 3-23*. The big advantage of this topology is very simple composition. This topology requires only two oppositely doped semiconductors with two metallic contacts placed near cold temperature for extracting the energy from the **TEG** towards the load. Moreover, **TEGs** depicted in *Fig. 3-23* and *Fig. 3-24* can harvest energy based on the thermoelectric effect and on the thermal generation of free carriers within depletion zone of the junction.

The evaluation of the harvesting capabilities of the non-conventional topologies is discussed in section 3.4. The **TEGs** are simulated based on the models described in section 3.2. *Fig. 3-25* illustrates the used modelling procedure to simulate the performance of the **TEG** with a shorted  $pn$  junction. The accurate performance evaluation of the large area  $pn$  junction *Fig. 3-23* and the thermovoltaic generator *Fig. 3-24* requires the addition of generation-recombination processes modelling. The **SRH** generation-recombination model is used for different carrier life times to reflect realistically the harvesting performance. Concerning  $\pi$ -type and lateral thin-film **TEGs**, the performance evaluation is performed only for the lateral generator because the theoretical electric behaviour is identical in both structures. In all cases, the comparison of electrical harvesting capabilities is performed regardless of  $\kappa$  and assuming that  $T_{\text{COLD}}$  and  $T_{\text{HOT}}$  are constant. By means of this assumption, the analysis can be performed based only on  $\sigma$  and  $S$  for investigated materials.

The harvesting capabilities of the **Si**-, **Ge**-, **Si<sub>70%</sub>Ge<sub>30%</sub>**- and **Bi<sub>2</sub>Te<sub>3</sub>**-based lateral thin-film **TEG** are presented (see section 3.4.1.2). The impact of the doping concentration on the **Si**-based **TEG** performance is presented (see section 3.4.1.1), leading to the conclusion that heavy doping delivers more energy to the load. To make the simulation more realistic, the contact resistance between the metal and the semiconductor is considered. In the simulation, technologically achievable values of the specific contact resistances are used. The peak harvested power densities versus  $\Delta T$  for different materials in lateral thin-film **TEG** topology is depicted in Fig. 3-39.

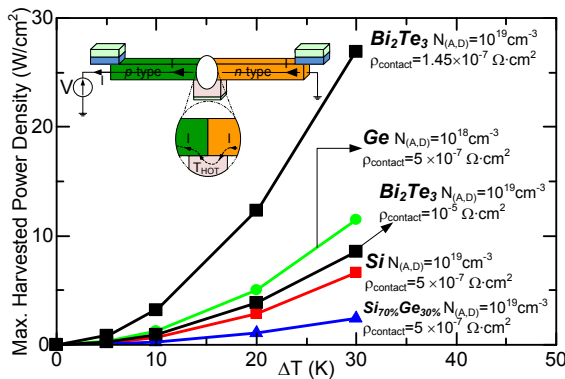


Fig. 3-39 Peak harvested power density versus  $\Delta T$  for different temperature extracted from lateral thin-film topology [Haras, 2014-b]

Based on Fig. 3-39, the peak harvested power density for  $\Delta T=30\text{K}$  are  $\sim 11\text{W}/\text{cm}^2$  for **Ge**  $\sim 7\text{W}/\text{cm}^2$  for **Si**,  $\sim 3\text{W}/\text{cm}^2$  for **Si<sub>70%</sub>Ge<sub>30%</sub>** and for **Bi<sub>2</sub>Te<sub>3</sub>** the power density is comprised between  $\sim 10\text{W}/\text{cm}^2$  and  $\sim 28\text{W}/\text{cm}^2$ . Comparing the harvested power density of **CMOS** compatible materials with **Bi<sub>2</sub>Te<sub>3</sub>** leads to the conclusion that the harvested power is significantly affected by the contact resistance. For conventional contact fabrication techniques the **Bi<sub>2</sub>Te<sub>3</sub>** is outperformed by **Ge**. When the contact resistance is reduced **Bi<sub>2</sub>Te<sub>3</sub>** offers the highest power density. However, it has to be underlined that the harvesting capabilities of **CMOS** compatible materials are in the same order of magnitude as **Bi<sub>2</sub>Te<sub>3</sub>**. This observation is putting **CMOS** compatible materials in competitive position with the conventional thermoelectric materials. Moreover, the harvesting capabilities of **CMOS** compatible materials is simulated in the range of  $\Delta T$  which is not optimal. This is another argument that shows the interest of **CMOS** materials.

The analysis of the harvesting capabilities of large area *pn* junction topology Fig. 3-23 (described in the section 3.4.2.1) leads to completely different conclusions. In this structure the *p*-type and *n*-type materials are in direct contact to form a *pn* junction in the **TEG** structure (see equivalent circuit Fig. 3-23). The harvested current flows through the diode in reverse direction which makes the internal **TEG** resistance very high. Moreover, the mechanism used to harvest the energy is different and the energy is produced by thermal generation of free carriers within the depletion zone of the *pn* junction. The different harvesting effect causes completely different electric behaviour compared with lateral thin-film **TEG** described previously. Contrary to the lateral thin-film generator, the large area *pn* junction is more efficient for light doping (see Fig. 3-32). It is due to the width extension of the depletion zone where free carriers are thermally generated. Secondly, the large area *pn* junction has higher harvesting capabilities for materials with short carrier life times, as expected. The large area *pn* junction **TEG** topology is more efficient for lightly doped materials with high density of energy states in the bandgap. This is in complete opposition with the lateral thin-film **TEG** topology which produces more energy when heavily doped and when using a defect free material.

The third studied topology is the lateral thermovoltaic **TEG** Fig. 3-24. This topology constitutes a slight transformation of the lateral thin-film **TEG** Fig. 3-22. The difference between Fig. 3-24 and Fig. 3-22 is the electrical insulation of the *pn* junction from the metallic contact located under the junction which forces the harvested current to flow through the diode in reverse direction. The difference between large area *pn* junction and

the thermovoltaic generator lies in the fact that in the latter the  $pn$  junction can be considered as working in isothermal condition while for large area  $pn$  junction the temperature is distributed along the junction. The harvesting capabilities of the thermovoltaic generator are evaluated and presented on the Fig. 3-36. Thermovoltaic and large area  $pn$  junction topologies have a lot of similarities. Firstly, both are more efficient when lightly doped, secondly both are producing more energy when based on the material with short carrier life time. Benchmarking the performance of thermovoltaic generator with the lateral thin-film **TEG** (compare Fig. 3-27 with Fig. 3-36), it is clear to conclude that lateral thin-film generator outperforms the thermovoltaic topology.

In the topology of thermovoltaic generator the temperature has an impact on the  $pn$  junction behaviour. The temperature can be applied to the generator in two different ways placing the  $T_{HOT}$  under the  $pn$  junction and  $T_{COLD}$  at the extremities or inversely. Depending on the temperature gradient direction along the generator, the diode conduction state can be accelerated (when the  $T_{COLD}$  is placed under the junction Fig. 3-37b) or retarded (when the  $T_{HOT}$  is placed under the  $pn$  junction Fig. 3-37a). The temperature impact on the diode behaviour is illustrated in Fig. 3-38. This observation proves that the diode is pushed “deeper” in the reverse state when it is maintained at higher temperature.

To close this chapter few bullet points are underlined:

- **CMOS** compatible materials have competitive or outperforming electrical performance compared with conventional  $Bi_2Te_3$  making them attractive thanks to their price, harmlessness, availability and industrial compatibility
- The size-induced  $\kappa$  reduction opens a possibility to employ the high bulk  $\kappa$  materials like **CMOS** compatible materials for thermoelectric conversion
- On the topological level, the architecture with diodes (*the Schottky metal-semiconductor contacts or the direct connection of n-type and p-type materials*) are less efficient due to the higher **TEG** internal resistance
- Energy harvesting based on thermal generation of free carriers within the depletion zone is less efficient than harvesting based on the thermoelectric effect
- The merging of two harvesting effects (*thermoelectric and thermal generation of free carriers*) in one single **TEG** topology is impossible, because both effects require antagonistic working conditions.

# Chapter 4: Measurement platform – design, fabrication and characterization

This chapter presents technological input of this work including the concept of the proposed device, the design, the fabrication, the characterization and finally results evaluation. Among numerous thermal conductivity ( $\kappa$ ) characterization methods electro-thermal method was chosen due to its simplicity on methodological and equipment level maintaining high measurement accuracy. However, this method requires topology featuring (i) as low as possible thermal leakages, (ii) linear temperature distribution along characterized material and (iii) as precise as possible temperature sensitivity enabling  $\kappa$  determination at lowest possible temperature drop. Those requirements are significantly influencing the layout of the device which is included while creating the tape out. Device fabrication requires technological methods *e.g.* dry and wet etching, evaporation or material growth and deposition. Proposed topology is fabricated upon the **Silicon On Insulator (SOI)** wafer with active Silicon (**Si**) layer thickness of 68nm. After the fabrication the complete characterization is performed giving mean  $\kappa$  value of 57W/m/K which represents 3-fold reduction over  $\kappa$  for bulk **Si**. The measured  $\kappa$  follows the empirical law with satisfying precision and it is dependent only on the thickness of the characterized membrane. Designed, fabricated and characterized device proves experimentally the size induced  $\kappa$  reduction in **Si**. Size-induced  $\kappa$  reduction opens new applications of **CMOS** compatible materials especially as environmentally friendly, cheap and industrially compatible thermoelectrics.

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## 4.1 Introduction

After the theoretical performance evaluation of **Silicon (Si)**, **Germanium (Ge)**, and **Silicon-Germanium ( $\text{Si}_x\text{Ge}_{1-x}$ )** for  $x=70\%$  in thermoelectricity, this chapter describes the technological input of this project. In the practical part, the design, fabrication and characterization of a thin-film micrometer platform for thermoelectric measurements is proposed. The platform is dedicated to measurement of the thermal conductivity ( $\kappa$ ) in the thin-film materials. The fabrication and characterization accuracy is evaluated on a thin-film **Si** membrane. Due to **Si** size reduction,  $\kappa$  exhibits reduction over a bulk value (*this effect was described in the section 3.2.1.5.1*). In thermoelectricity, there are three important parameters: thermopower (**S**), electrical conductivity ( $\sigma$ ) and  $\kappa$ . Among them,  $\kappa$  is the most difficult to determine and to optimize. **S** and  $\sigma$  are relatively easy to measure using well established electrical characterization methods. Optimization of **S** (*see Fig. 3-10*) and  $\sigma$  (*see Fig. 2-40*) can be realized also in rather easy way by varying the doping concentration. However, optimizing and determining  $\kappa$  is not trivial. It requires establishing the device topology, characterization method, procedure and conditions.

Thermal measurements are the source of the numerous difficulties especially due to the precise identification and evaluation of the thermal paths and heat leakages existing in the device. Moreover, thermal transport is following a completely different propagation physics than electronic transport [[Ziman, 2001](#)] which is also increasing the difficulty of the thermal characterization. The material thermal properties are always vitiated by an error mainly due to difficulties related to heat convection losses [[Jiji, 2006](#)], radiation losses [[Lienhard, 2011](#)] and the imprecise determination of the injected heat power. For these reason the thermal characterization has usually a lower precision than the electric measurements. The inaccuracy of thermal measurements is present when characterizing bulk materials. When the characterization is performed on thin-film materials, the impact of all leakages and parasitical parameters is significantly amplified. Thus, the thermal characterization of the nanostructured thin-film materials is a challenging task.

It was already described that in digital industry thin-film **Si** layers are largely used for device fabrication. **SOI** technology is facilitating the fabrication of thin-film channels **MOSFET** transistors assuring simultaneous electrical insulation between the channel and the substrate. Moreover, **CMOS** technologies which are relying on thin-film **Si** layers have been successively developed due to their high performance and fabrication efficiency. The minimal **Si** thickness currently industrially used is around 6nm. Although, the electrical characterization of thin-film **Si** is well established in literature, there is still a big lack of data regarding the thermal properties of **Si**, **Ge** and especially  $\text{Si}_x\text{Ge}_{1-x}$ . Thus the thermal characterization of **CMOS** compatible materials in the form of thin-film is very important scientifically and has high technological impact.

In the literature, there are some examples of devices dedicated to thin-film material  $\kappa$  characterization. In general, regardless the topology and thickness of the characterized material, the most popular measurement methods can be divided into three groups:

- non-contact methods *e.g.* Raman spectroscopy [[Abel, 2007](#)], [[Lysenko, 1999](#)], [[Piscanec, 2003](#)]
- contact methods *e.g.* scanning thermal microscopy [[Gomès, 2007](#)], [[Gomès, 2015](#)] *etc.*

- electro-thermal characterization *e.g.* **DC** thermal coupling [[Hopkins, 2011](#)], [[Kim, 2012](#)], [[Yu, 2010](#)], [[Shi, 2003](#)], [[Tang, 2010](#)] or  $3\omega$  method [[Ftouni, 2012](#)], [[Sikora, 2012](#)] *etc.*

The method used in this thesis is based on the **DC** electro-thermal characterization. This method was chosen because:

- it has simple theoretical background compared to other available methods
- the device fabricated dedicated for this method can be easily transformed into thermoelectric generator (**TEG**)
- Required measurement equipment is standard, without sophisticated or specially dedicated equipment needed

Thus, this method of  $\kappa$  extraction and results will be presented in the following.

#### 4.1.1 Electro-thermal $\kappa$ measurement method

The characterization of nanostructured materials requires the use of specific dedicated methods. The material with very small thickness cannot be measured using the same procedures as for bulk materials. Moreover, the measurement techniques and conditions when characterizing the nanostructured materials have to be much more sensitive and accurate than procedures adopted when working with bulk materials. In nanostructures, the parasitic parameters, losses, measurement errors and noise are much significant than for bulk structures.

Among the difficulties associated to the characterization of  $\kappa$  is the precise determination of the temperature (**T**) distribution along the heat flow (**Q**) propagation line. **T** distribution is described by the heat diffusion equation Eq. 4-1 [[Lienhard, 2011](#)]. Local temperature at different positions in the material can be found using Eq. 4-1. When analyzing the general heat diffusion equation in three dimensions Eq. 4-1:

$$C \cdot \frac{\partial T}{\partial \text{time}} = \nabla(\kappa \cdot \nabla T) + H \quad \text{Eq. 4-1}$$

$$0 = \nabla(\kappa \cdot \nabla T) + H \quad \text{Eq. 4-2}$$

where:

<b>C</b>	Heat capacity per unit volume (J/K/kg)
<b><math>\kappa</math></b>	Thermal conductivity (W/m/K)
<b>H</b>	Volumetric heat generation (W/m <sup>3</sup> )
<b>T</b>	Local lattice temperature (K)
<b>time</b>	Time (s)

It can be remarked that heat flow Eq. 4-1 is multi-dependent on material's parameters (**C** and  **$\kappa$** ), material dimensions ( **$\nabla$** ) and time (**time**). Solving Eq. 4-1 represents a significant level of difficulty especially when considering the three dimensional non-stationary system. For that reasons, the device topology and measurement technique is adapted in such a way to introduce important simplifications in Eq. 4-1. Firstly, when considering a thermal steady-state, Eq. 4-1 can be simplified in the form written in Eq. 4-2. Secondly, device topologies are designed in such a way to privilege the heat flux propagation only in one direction which largely simplifies Eq. 4-2 from a three-dimensional to a one-dimensional problem. Thirdly, Eq. 4-2 includes some difficulties in

the form of the gradient  $\nabla$  which mathematically is easy to calculate but in this case is complicating the analysis. Getting rid of the differentials requires the linearization of Eq. 4-2 which in practice is achieved by considering a linear  $T$  distribution along the characterized material and by performing the  $\kappa$  measurement only for small temperature drop along the characterized material. Moreover,  $\kappa$  measurements are very often realized in vacuum to eliminate the convection losses [Jiji, 2006] which, in nanometric structures, can play a significant role. The elimination of convection losses simplifies the analysis of the measurement errors only to radiative heat losses. Owing to that, the analysis and calculation of the  $T$  distribution along the characterized sample is significantly simplified considering a one-dimensional configuration, accurate when measurements are performed in vacuum and easy to realize.

The electro-thermal  $\kappa$  measurement method is one of the oldest and probably most frequently used among all  $\kappa$  measurement procedures. The literature reports many cases of  $\kappa$  determination with different device configuration. Fig. 4-1 presents the most common devices topologies dedicated to electro-thermal measurement of  $\kappa$ :

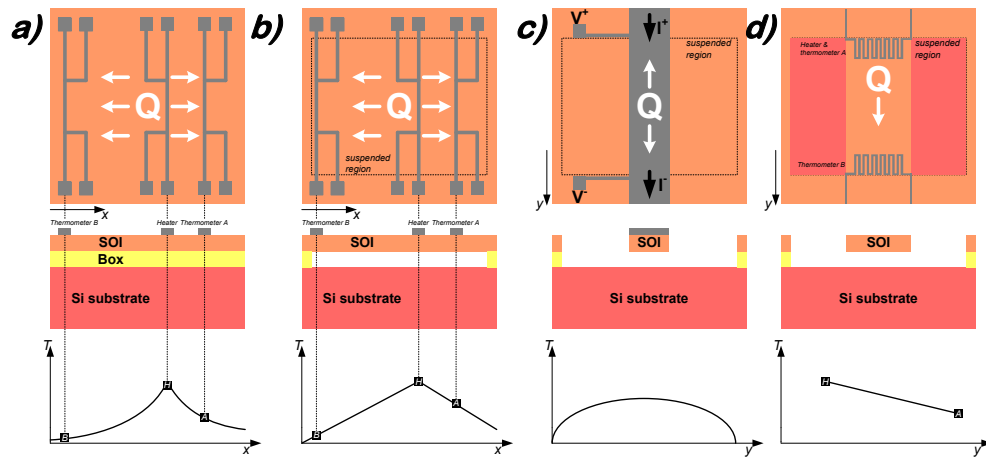


Fig. 4-1 Different device configuration for electro-thermal thin-film  $Si$   $\kappa$  measurement method emphasizing the cross-sectional view and temperature gradient following the  $Q$  propagation line a) not suspended on-substrate steady-state joule heating topology [Asheghi, 1997], [Asheghi, 1998], [Ju, 2005], b) suspended on-substrate steady-state joule heating topology [Asheghi, 2002], [Hao, 2006], [Kim, 2012], [Song, 2004], [Sverdrup, 2001], c) suspended heater bridge topology [Liu, 2005], [Liu, 2006], d) suspended heater-thermometer topology [Yu, 2010], [Tang, 2010]

To measure  $\kappa$ , the temperature distribution along the direction of heat propagation has to be determined. For measurement devices where the characterized material is not suspended Fig. 4-1a [Asheghi, 1997], [Asheghi, 1998] and [Ju, 2005], the  $T$  distribution is therefore not linear due to the fact that  $Q$  is evacuated from the **SOI** membrane through the **Box**<sup>25</sup> and the **Si** substrate. For this reason,  $\kappa$  measurements are more complicated, less precise and more dependent on the device topology. Releasing the **SOI** from the **Si** substrate and the **Box** as depicted in Fig. 4-1b [Asheghi, 2002], [Hao, 2006], [Kim, 2012], [Song, 2004], [Sverdrup, 2001] makes the  $T$  distribution linear along the measured **Si** layer. This largely simplifies the determination of the  $\kappa$  and makes the measurement more precise. In the topology depicted in Fig. 4-1d [Yu, 2010], [Tang, 2010] thanks to the perfect device symmetry, the measurement of  $\kappa$  can be realized based only on the  $T$  measurement from one thermometer, the heating element being also used as thermometer. The device

<sup>25</sup> **Box** – in the **Si** based **SOI** wafers it is the layer of thermal  $SiO_2$  (in most of cases the dry  $SiO_2$  is used grown using thermal oxydation) with very well defined and controlled thickness sandwiched between the top thin-film layer of **Si** and the wafer's **Si** substrate



topology depicted in Fig. 4-1c [Liu, 2005], [Liu, 2006] differs slightly from the previous topologies. A metallization is realized on the suspended thin-film. The current flowing through the bridge is heating the thin-film material non-uniformly due to the suspension. The temperature distribution along the propagation of  $\mathbf{Q}$  has a parabolic shape with a maximal value in the middle of suspended membrane. The measurement of the current and voltage drop in the metallic bridge together with the dimensionality of the system provide sufficient information to calculate  $\kappa$ .

In all cases, the idea of electro-thermal  $\kappa$  measurement method relies on a principle of Joule heating [Alexander, 2013] for sourcing  $\mathbf{Q}$ . Heat flow is generated in the metallic heater by passing a current through it. To determine the  $\mathbf{T}$  drop along the material, the thermometer element measures the local material temperature at a well known distance ( $\mathbf{L}$ ) from the heater. For measurement performed in vacuum  $\mathbf{T}$  distribution is linear along the material and the electric power applied to the heater ( $\mathbf{P}_H$ ) can be considered as heat power. Using those assumptions  $\kappa$  can be calculated following Eq. 4-3 for the topology depicted in Fig. 4-1b [Asheghi, 2002] or Eq. 4-4 for topology depicted in Fig. 4-1d:

$$\kappa = \frac{1}{2} \frac{P_H}{T_H - T_{(A,B)}} \cdot \frac{L_{(A,B)}}{W \cdot t} \quad \text{Eq. 4-3}$$

$$\kappa = \frac{P_H}{T_H - T_{(A,B)}} \cdot \frac{L_{(A,B)}}{W \cdot t} \quad \text{Eq. 4-4}$$

where:

$P_H$	Heater electric power (W)
$T_H$	Heater temperature (K)
$T_{(A,B)}$	Temperature measured in <b>A</b> or <b>B</b> position (K)
$L_{(A,B)}$	Distance between heater and thermometer <b>A</b> or thermometer <b>B</b> (m)
$W$	Width of the measured thin-film material (m)
$t$	Thickness of the measured thin-film material (m)

It is worth noting that Eq. 4-3 and Eq. 4-4 can only be applied to suspended structures depicted in Fig. 4-1b or Fig. 4-1d for which the  $\mathbf{T}$  distribution is linear. When the structure is not thermally insulated from the **Si** substrate as depicted in Fig. 4-1a, retrieving  $\kappa$  is more complicated and resorts to a more complex analysis of the local  $\mathbf{T}$  value along  $\mathbf{Q}$  propagation. Example of  $\kappa$  measurement using this topology is reported in [Asheghi, 1997].

The reason that makes the electro-thermal method so popular among all  $\kappa$  determination methods is the use of easily accessible and precise electric equipment. Heat is generated through the Joule effect by passing current. Temperature is determined indirectly measuring the voltage drop long the heating element (Fig. 4-1c) or resistance shift caused by the temperature change (Fig. 4-1a; Fig. 4-1b and Fig. 4-1d). In all cases,  $\kappa$  is determined relying on the electronic equipment which can precisely measure and/or apply the current, voltage or power. This particularity is not true when using other methods where the equipment accuracy is not at the same level as for electronic equipment. However, the disadvantage of this method is the indirect determination of the thermometers temperatures  $T_A$  or  $T_B$ . Usually, it is measured by the resistance shift due to the temperature change. Thus, thermometers have to be designed from materials with stable properties over the varying range of temperature.

## 4.2 Designing the device

To accurately measure  $\kappa$  in **Si** thin-film, a special micrometer measurement platform was designed. The top view of the full cell is depicted in Fig. 4-2:

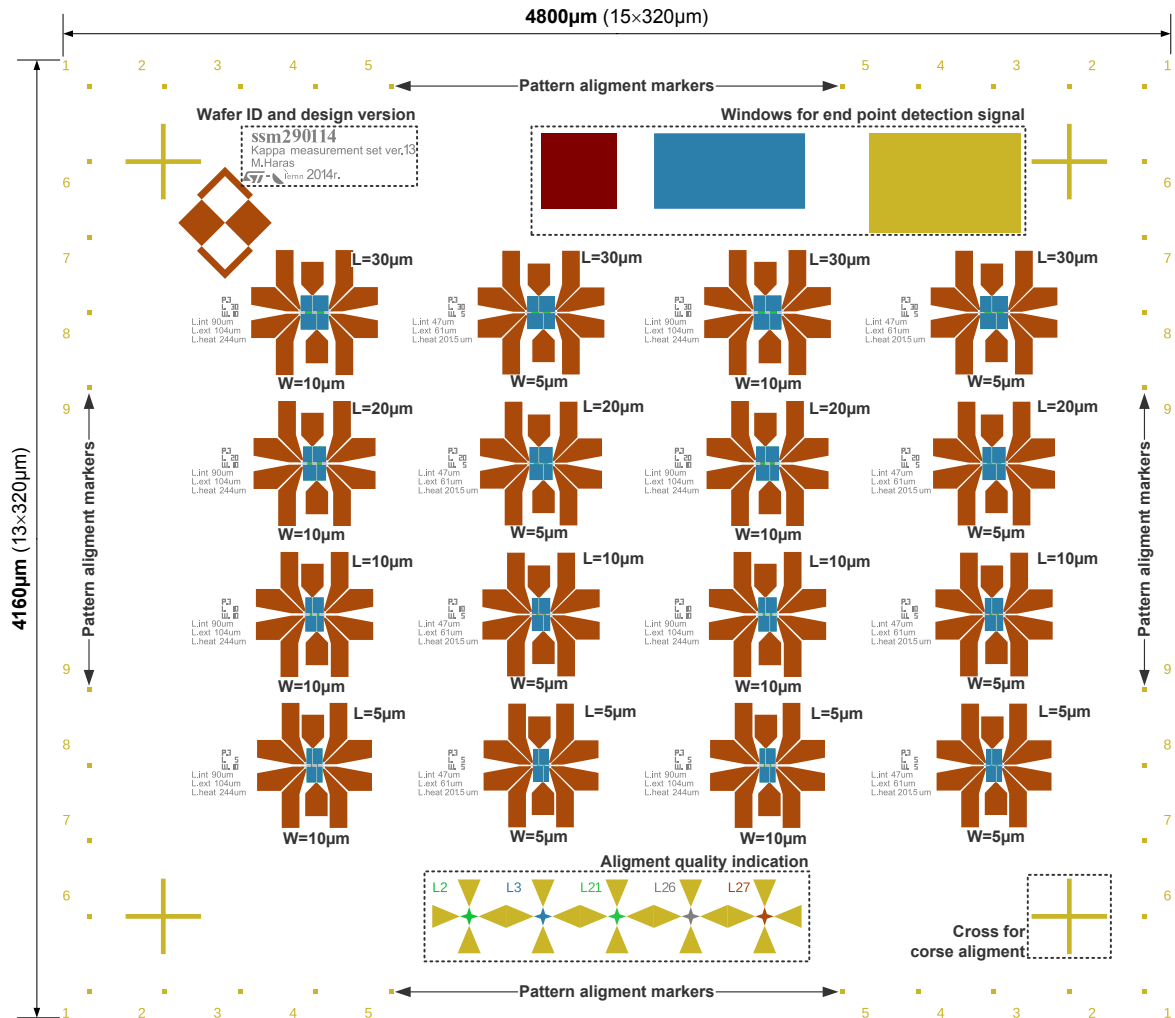


Fig. 4-2 Top view of the designed and fabricated cell emphasizing external dimensions and chosen technologically important cell components; L and W labels near the constituent devices states for length and width of the single **Si** membrane

Fig. 4-2 shows the top view of the fabricated cell which contains 16 devices, however 8 among them are repeated. The distinguishing parameters are the membrane **L**ength and **W**idth. The devices are arranged in four columns starting from the left the **W**=10µm; 5µm; 10µm; 5µm. There are also four lines starting on the bottom-most line **L**=5µm, 10µm, 20µm and 30µm for the top-most line.

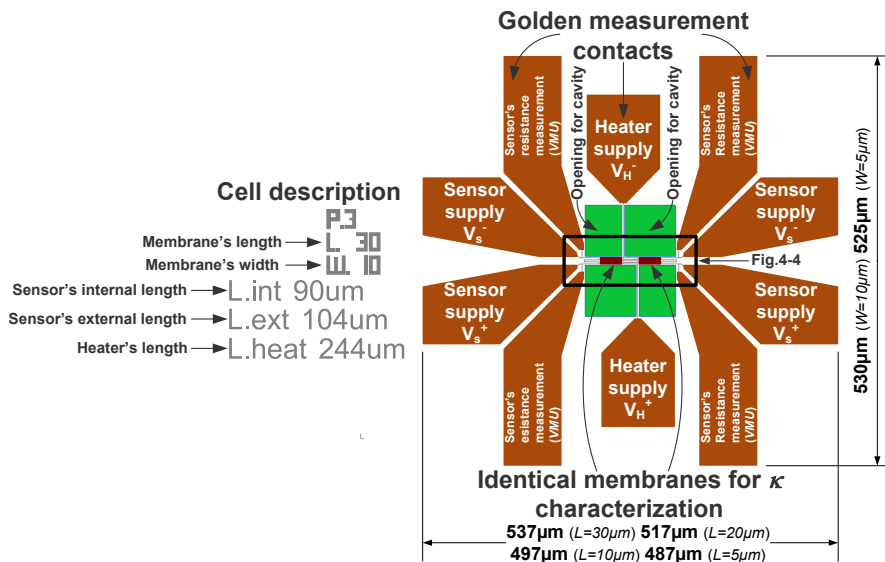
The external cell dimensions are 4160µm×4800µm. Because of technological reasons, the cell external dimensions should be composed from the finite number of the 320µm×320µm squares. This corresponds to the exposure field when performing the lithography, the machine executing this operation is capable of exposing the design within the exposure field without displacing the wafer stage. Moreover, to achieve the highest precision the most critical part of the device has to be placed in the middle of the exposure field. Fig. 4-2 presents the placement of the important cell components such as alignment

markers, windows for end point detection signals or the design and wafer **ID**. The alignment markers are the small squares (*the used size was  $8\mu\text{m}\times 8\mu\text{m}$  or  $20\mu\text{m}\times 20\mu\text{m}$* ) at well specified coordinates.

To ensure that the relative position between the different layers will correspond to the design the lithography machine detects the markers and based on their real positions the exposure is performed. The relative positioning between different layers is maintained regardless of the human induced displacement of the wafer when charging it into the machine. To check the quality of the alignment, indicators are placed (*big crosses situated in the bottom part of the cell*) for each layer separately. When the alignment is not precise the small internal cross is not in the centre of the zone defined by four triangles. This means that the step should be repeated because the placement of the exposed layer does not correspond to the design. The alignment accuracy of the lithography e-beam equipment is 30nm. This standard misalignment can be significantly reduced when using four markers per cell as it is the case in the design depicted in Fig. 4-2.

The second technologically important elements in the cell are the windows dedicated for the end point detection while performing the **Reactive Ion Etching (RIE)**. Thanks to the windows, it is possible to measure the end point signal which indicates the progress of the **RIE**. This allows to stop the etching at a precisely defined time.

To distinguish the design, process flow version and wafer **ID** after the wafer is cleaved each cell is labelled. This is presented in the upper left corner in the Fig. 4-2. This labelling is performed in the material which remains unchanged or altered by the fabrication techniques or chemicals used during fabrication. At the end of the fabrication, the labelling remains visible and readable which is very important for the technical documentation of the project.



**Fig. 4-3 View of the single device emphasizing the most important dimensions and describing the most important device parts**

After presenting complete cell, this section focuses on the single device which is depicted in Fig. 4-3. At first glance, it can be noted that most of the area in the device structure is occupied by the metallic contacts. The measurement contacts have to be big enough to facilitate the placement of the measurement needles enabling the characterization. It can also be remarked that the device consists in one heater placed in the central part of the topology and two identical symmetrically placed sensors. This means that the designed topology is symmetrical with respect to **x** and **y** axis. The symmetry

largely contributes to simplify the heat transport analysis in the device. Analyzing the number of contacts per heater and sensor, it can be remarked that the heater is supplied using two contacts ( $V_H^+$  and  $V_H^-$ ), while each of the sensors has four contacts. The accurate resistance measurement is performed using a four-point-probes measurement technique [Schroder, 2006]. This method requires two contacts to force the current ( $V_S^+$  and  $V_S^-$ ) and two additional contacts to measure precisely the voltage drop using Voltage Measurement Unit (VMU). The measurement contacts are fabricated in gold (Au) due to its very high  $\sigma$  and low hardness. The use of the four-point probe method makes it possible to determine the sensor resistance very high precision. The device external dimensions are dependent on  $L$  and  $W$  as shown in Fig. 4-3. Each device in the cell is labelled with the membrane dimensions  $L$ ,  $W$  and length of the heating element ( $L_H$ ) and sensor. The sensor length is splitted into two values that specify the distance between the sensor supply contacts ( $L_{ext}$ ) and the sensor length between the contacts dedicated to VMU ( $L_{int}$ ). The precise length identification is very important when the heater or sensor  $\sigma$  has to be determined. Fig. 4-4 shows a zoom on the central part of this topology:

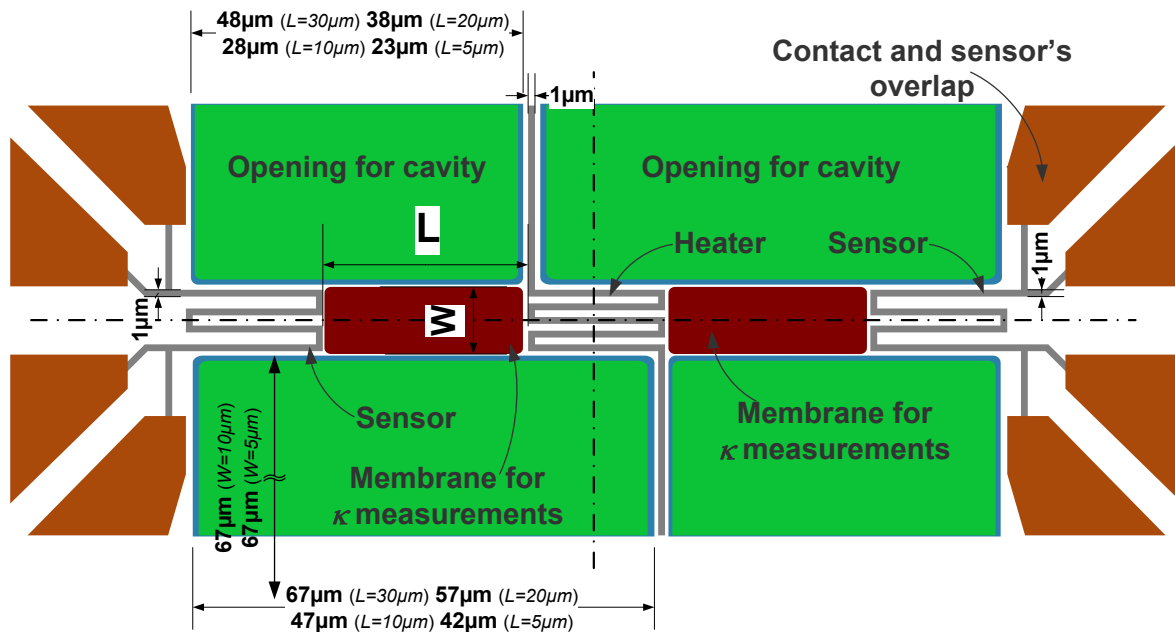


Fig. 4-4 The view on the thin-film Si  $\kappa$  measurement device specifying most important dimensions and topological components

Owing to device symmetry, the identical sensors are put in the same thermal conditions and only one sensor can be measured. The characterized thin-film material is placed between openings for cavities (*the yellow and blue rectangles*). The cavities are enabling the fabrication of the thermal insulation of the SOI membrane from the Box and the Si substrate. In this condition, a linear  $T$  distribution between the heater and the sensors can be assumed (look Fig. 4-1b or Fig. 4-1d). The cavities length is imposed by  $L$ , however the cavity width is the compromise between:

- Good thermal insulation between the membrane and the extrinsic region (*the thermal resistance rises with the cavity dimensions*)
- The temperature profile along the heater has a parabolic shape, but the  $T$  distribution deviates from the parabolic law while  $L_H$  increases
- Rising the cavity dimensions,  $L_H$  increases making the membrane less resistant mechanically. This opens the possibility of crack formation in the membrane

In this topology the cavity has a width of  $67\mu\text{m}$  (*the cavity is not shown completely due to the zooming*). To generate the heat directly on the membrane, the heater is fabricated as a serpentine. The heater serpentine is dense on the membrane to localize the heat generation on the membrane. Referring to the sensor shape the, it can be noticed that the length of the sensor is localized on the membrane. This is done to obtain the higher sensor sensibility. In all cases the sensor and heater cross-sectional dimensions are (*width* $\times$ *thickness*)  $1\mu\text{m}\times 30\text{nm}$ .

Proposed device accumulates the properties of the topologies depicted in Fig. 4-1b and Fig. 4-1d. However, as distinct from Fig. 4-1b and Fig. 4-1d in the proposed structure two sensors are placed symmetrically referring to heater and both heater and sensors have serpentine shape. Moreover, in contrary to the Fig. 4-1d proposed topology uses separated heater and sensor elements. The heater is not designed to be used as thermometer.

Fig. 4-2 to Fig. 4-4 present the design of the proposed device. It is worth noting that this device consists in some differently fabricated parts which all together are forming the  $\kappa$  measurement platform. The inner “parts” of the device are fabricated differently and to distinguish them the layers are used. Table 4-1 links the colour code used in the design with the technological process attributed to the given layer. Analyzing Table 4-1, it can be remarked that the layers are used only when performing **RIE** process or metallization by evaporation. However, the complete process flow contains much more fabrication techniques and processes.

**Table 4-1 Layer colour code and description emphasizing the order of fabrication and attributed technological process**




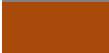


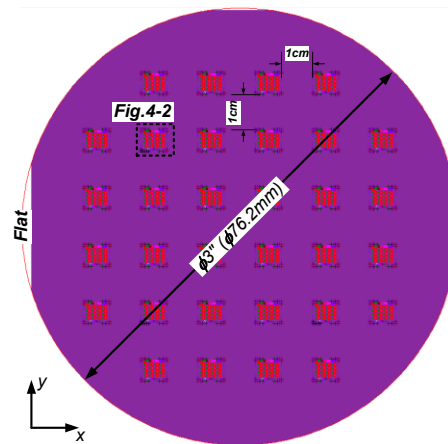
Colour	Layer number	Description	STEP number (Fig. 4-6)	Processing technology
	16	Alignment markers	2a	RIE
	3	Openings for cavities	2b	
	26	Platinum metallization	4	Evaporation
	27	Gold metallization	5	
	21	$\text{Si}_x\text{N}_y$ removal from the membrane	6	RIE
	2	Si substrate exposure at bottom of the cavity	7	

Fig. 4-5 presents the view on a full  $\phi 3$  inches ( $\phi 76.2\text{mm}$ ) wafer on which 32 cells are integrated with a 1cm spacing in  $x$  and  $y$  directions. As it was previously described, a single cell consists in 16 devices (*8 different devices*) meaning that on a full 3 inches wafer 512 devices are available for  $\kappa$  measurement of thin-film **Si**.



**Fig. 4-5 Top view on the full 3 inches SOI wafer with the cell arrangement and spacing**

The spacing between the cells is set to 1cm to facilitate the cleaving of the full wafer into separate samples. This distance is sufficiently comfortable for manual cleaving using a diamond probe. To increase the number of fabricated cells on the full wafer, the spacing between the cells can be significantly reduced.

### 4.3 Fabricating the device

Generally all technical projects, regardless the application or domain, have dual form. Firstly, the project has the technical concept where the placement, arrangement, dimensionality *etc.* are precised (*e.g. technical drawing, layout, electrical schema,...*). Secondly, the full technical project has to include the fabrication procedure, which specifies how fabricate or install designed device (*e.g. fabrication techniques, recipes, installation requirements,...*). In the field of electron devices this project duality is manifested by the layout which defines the size, placement and dimensionality of the device and on the other hand by the process flow. The latter is defining the fabrication procedure specifying used manufacturing techniques. After precise description of the design now the focus will be put on the fabrication procedure.

Device fabrication requires the execution of the sequence of technological steps. Firstly, the complete process flow will be presented emphasizing the link between the designed layout and the corresponding technological steps. The full process flow of micrometer platform for  $\kappa$  measurements is depicted in Fig. 4-6. Pictures taken using **Scanning Electron Microscopy (SEM)** show the sample after the realization of the corresponding step.

Fig. 4-6 presents the full fabrication procedure of the micrometer platform for  $\kappa$  measurements based on thin-film materials. However, it has to be underlined that some steps with minor importance are not depicted for simplification and clarity reasons. Mainly the omitted steps are concerning the cleaning of the wafer and the realization of the alignment marks prior to cavity etching (**STEP 2**).

The process flow consists in nine main steps for releasing the **SOI** membrane from the **Box** and **Si** substrate and fabricating the local integrated platform dedicated to  $\kappa$  measurement.

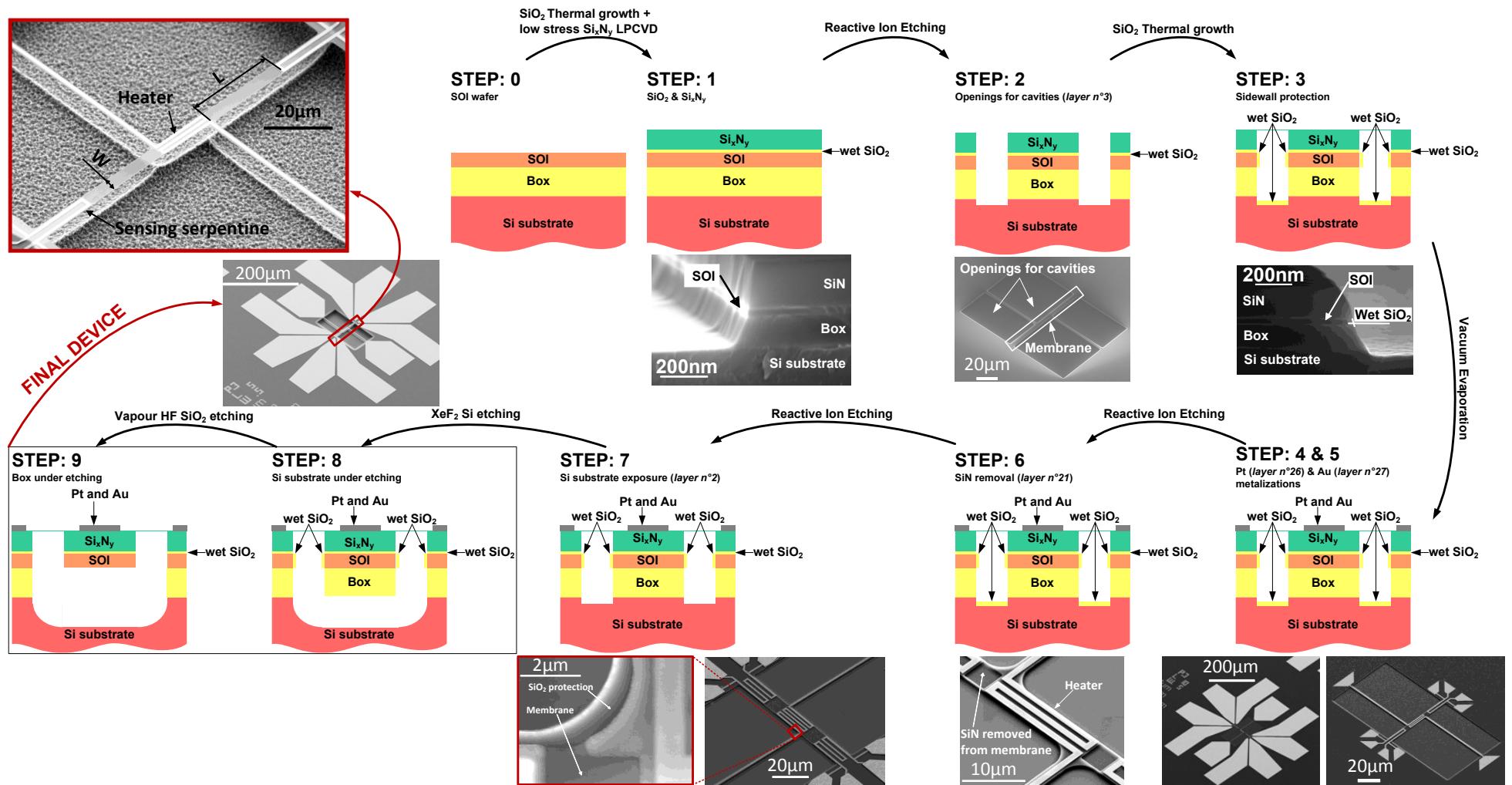


Fig. 4-6 Full process flow of the micrometer measurement platform for  $\kappa$  measurements in thin-film silicon. SEM photos presented below the cross-sectional sketches are presenting the sample after realization of the corresponding step. Specification of layer number is provided when the technological step corresponds to the layer in designed layout. The used manufacturing techniques are indicated over the arrows between the contributing steps.



### 4.3.1 STEP 0 – SOI wafer

The departure point of this technological work is the **SOI** wafer. A wafer with a 68nm thick **SOI** layer and 145nm **Box** was used. However, the proposed fabrication procedure is compatible with different **SOI** and **Box** thicknesses or even different than **Si** thin-film materials. In such a case the etching times should be adjusted to obtain identical result. All the following measurements are corresponding to the 68/145 **SOI** wafer with precise specification described in Table 4-2:

**Table 4-2 Used wafer technical specification**

<i>Parameter</i>	<i>Unit</i>	<i>Value</i>
<b>Full wafer diameter</b>	<b>Inch (mm)</b>	<b>3" (76.2)</b>
<b>SOI thickness</b>	<b>nm</b>	<b>68.53<sup>+0.55</sup><sub>-0.49</sub></b>
<b>Box thickness</b>	<b>nm</b>	<b>146.53<sup>+3.09</sup><sub>-1.21</sub></b>
<b>Wafer thickness</b>	<b>µm</b>	<b>780-800</b>
<b>Orientation</b>		<b>100</b>
<b>SOI resistivity</b>	<b>Ω·cm</b>	<b>14-18.9</b>
<b>Doping type</b>		<b>p</b>
<b>Doped with</b>		<b>Boron</b>
<b>Carrier concentration</b>	<b>cm<sup>-3</sup></b>	<b>(0.7-1)×10<sup>15</sup></b>
<b>Manufacturer</b>		<b>SOITEC®</b>
<b>Price*</b>	<b>€/wafer</b>	<b>~111</b>

\*Academic price. The sold wafer diameter is  $\phi 300\text{mm}$  which is cut in 9  $\phi 76.2\text{mm}$  wafers. Price of a single  $\phi 300\text{mm}$  wafer is around 1000€.

To evaluate the quality of the used wafer, the thickness of the **SOI** and **Box** layers are checked using ellipsometry (**ELL**). The full wafer mapping is depicted in Fig. 4-7. To achieve high mapping resolution, 49 measurements are performed.

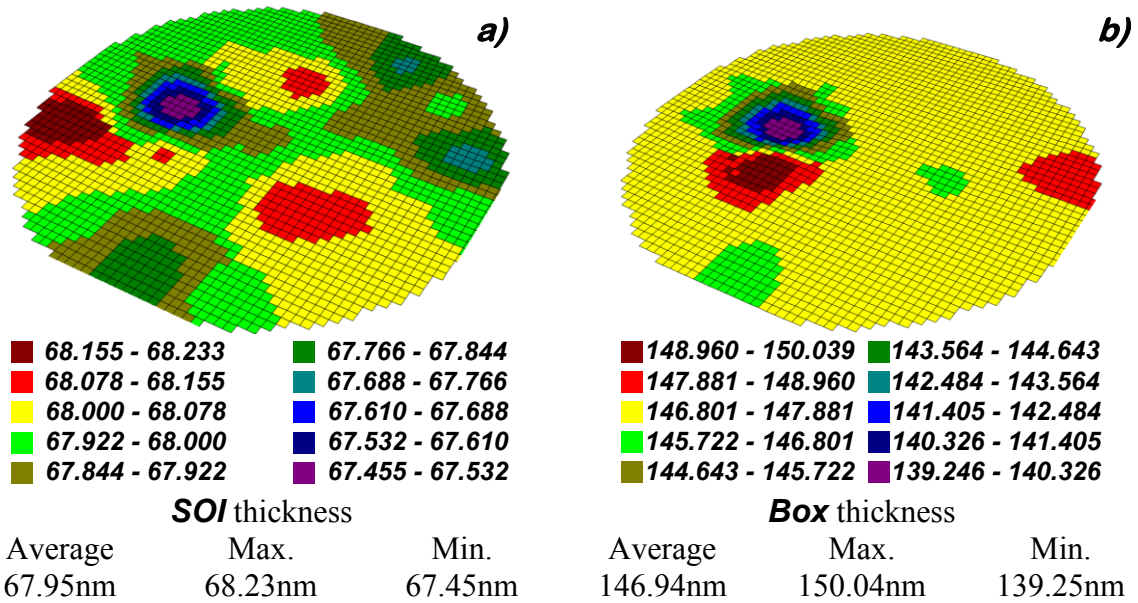


Fig. 4-7 Full wafer *SOI* and *Box* thicknesses 49 points mapping emphasizing the thickness dispersion a) *SOI* thickness mapping; b) *Box* thickness mapping

From Fig. 4-7 and Table 4-2, it can be concluded that the thickness of used *SOI* wafer is very well controlled and has small dispersion around the nominal value. This is very important because the assumption that all membranes fabricated upon this wafer have same *Si* thickness can be justified.

Before starting the process flow the wafer is cleaned using the procedure detailed in Table 4-3:

Table 4-3 Pre-processing wafer cleaning

<i>No.</i>	<i>Product</i>	<i>Temperature</i> (°C)	<i>Duration</i> (min)	<i>Target material</i>
0-1	Remover PG or SVC14	65	min. 120	Wafer protection resist striping
0-2	Acetone	~35-40	10-15	Trace of the Remover PG or SVC14
0-3	Iso-propanol ( <i>IPA</i> )	Room	3-5	
0-4	700W $\mu$ -wave $O_2$ plasma	~130	30	Organic residues
0-5	30ml 95% $H_2SO_4$ + 10ml 30% $H_2O_2$	Room	10	
0-6	5% HF	Room	2	Native $SiO_2$

#### 4.3.2 STEP 1 – $SiO_2$ thermal growth and $Si_xN_y$ deposition

**STEP 1** is performed directly after wafer cleaning to avoid the formation of the native oxide on the *SOI* layer which is exposed to air after  $SiO_2$  wet etching in *Hydro-Fluoric* (*HF*) acid. Thus directly after wafer cleaning, the silicon dioxide is thermally grown. The desired thickness of  $SiO_2$  is 12nm which requires the recipe summarized in Table 4-4:

Table 4-4 Thermal oxide growth procedure

Process stage	Duration (min)	Temperature (°C)	Gas composition	Gas flow dm <sup>3</sup> /min
Wafer introduction		500		
Heating	35	from 500 to 850	N <sub>2</sub>	2.0
Filling-up with Oxygen	10	850	O <sub>2</sub>	1.5
Oxide growth	6	850	O <sub>2</sub> H <sub>2</sub>	1.5 2.5
Filling-up with Oxygen	15	850	O <sub>2</sub>	1.5
Cooling	Inertia	from 850 to 500	N <sub>2</sub>	2.0

Analyzing the **SiO<sub>2</sub>** growth procedure presented in Table 4-4, it can be noted that this step is realized in 3 actions. The wafer is introduced into the oven preheated to 500°C and filled up with nitrogen (**N<sub>2</sub>**). Afterwards, a heating ramp of 10°C/min rises the oven temperature to the final value of 850°C. The heating ramp reduces the thermally induced mechanical stress. When the thermal conditions are stabilized, the oxygen (**O<sub>2</sub>**) is introduced into the tube with a flow of 1.5dm<sup>3</sup>/min for 10 min. The aim of this step is to initiate the thermal oxidation with a uniform layer of dry **SiO<sub>2</sub>**. Afterwards the main **SiO<sub>2</sub>** growing step starts by introducing **O<sub>2</sub>** and hydrogen (**H<sub>2</sub>**) with the flow rate of 1.5dm<sup>3</sup>/min and 2.5dm<sup>3</sup>/min respectively. The growth duration is 6min. After the main growth step, **O<sub>2</sub>** is introduced to the tube with a flow rate of 1.5dm<sup>3</sup>/min for 15min. The reason of this step is to ensure that the tube is completely purged of **H<sub>2</sub>**. To finalize the process, the temperature has inertial decrease with nitrogen flow of 2dm<sup>3</sup>/min.

The **SiO<sub>2</sub>** plays the role of sacrificial layer in this process flow. This layer allows to stop the **RIE** process of **Si<sub>x</sub>N<sub>y</sub>** performed in **STEP 6**. Moreover, this thin **SiO<sub>2</sub>** layer also protects the **SOI** against etching by **XeF<sub>2</sub>** gas when the **Si** substrate is under etched (**STEP 8**).

To isolate the metallic components of the device from the characterized **Si** membrane, and to increase the mechanical strength of the suspended membrane 100nm thick **Silicon-Nitride (Si<sub>x</sub>N<sub>y</sub>)** is deposited using **LPCVD**. **LPCVD** is used because it enables the deposition of low stress **Si<sub>x</sub>N<sub>y</sub>**. A low stress material is required in this design to avoid mechanical bending.

The deposition of the silicon nitride is realized following the recipe specified in Table 4-5. Firstly, the wafer is introduced into preheated oven at 350°C. While heating with the rate of ~7°C/min, gas evacuation is performed so when reaching the final temperature of 800°C the pressure in oven is between 5 and 20mTorr. Afterwards, ammoniac (**NH<sub>3</sub>**) purging is performed for 10min with the flow rate of 10cm<sup>3</sup>/min and a pressure of 100mTorr is maintained inside the oven. The aim of this purging is to completely fill the oven with **NH<sub>3</sub>** before performing the deposition. **Si<sub>x</sub>N<sub>y</sub>** is subsequently deposited by reaction of **NH<sub>3</sub>** with **SiH<sub>2</sub>Cl<sub>2</sub>** under flow rate of 10 and 20cm<sup>3</sup>/min respectively. The deposition time is 40 min. The final step corresponds to **SiH<sub>2</sub>Cl<sub>2</sub>** and **NH<sub>3</sub>** purging. Reduction of thermally induced mechanical stress is achieved by limiting cooling ramp to not exceed -7°C/min.

Table 4-5 Low stress  $\text{Si}_x\text{N}_y$  deposition procedure using LPCVD

Process stage	Duration (min)	Temperature (°C)	Pressure (mTorr)	Gas composition	Gas flow $\text{cm}^3/\text{min}$
Wafer introduction		350			
Heating	60	from 350 to 800	5-20		
Ammoniac purging	10	800	100	$\text{NH}_3$	10
$\text{Si}_x\text{N}_y$ deposition	40	800	100	$\text{SiH}_2\text{Cl}_2$	20
				$\text{NH}_3$	10
Ammoniac purging	15	800	100	$\text{NH}_3$	10
Cooling	60	from 800 to 350			

The desired  $\text{Si}_x\text{N}_y$  thickness is 100nm which referring to Table 4-5 gives a theoretical deposition rate of 2.5nm/min.

To evaluate the thickness of the  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$ , *ELL* mapping was performed as presented in Fig. 4-8. Analyzing Fig. 4-8a it can be remarked that the  $\text{SiO}_2$  layer has a higher thickness dispersion than the previously characterized *SOI* or *Box* thicknesses (refer to Fig. 4-7). However, it has to be underlined the dispersion of few nm around the desired value is not a problem for the process procedure. Focusing now on  $\text{Si}_x\text{N}_y$  for which the mapping is depicted in Fig. 4-8b, it can be remarked that the real thickness of  $\text{Si}_x\text{N}_y$  is slightly lower than the desired 100nm. It can be remarked that the  $\text{Si}_x\text{N}_y$  thickness has a lower dispersion around the mean value.

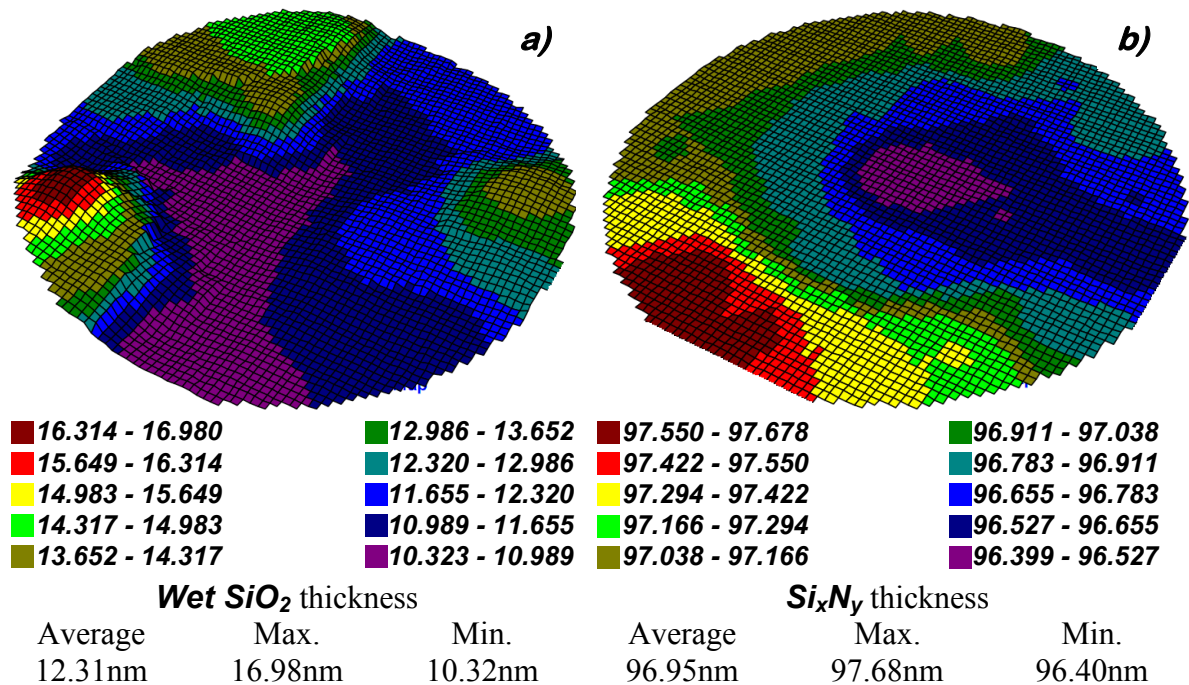


Fig. 4-8 Full wafer  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_y$  thicknesses 49 points mapping emphasizing the thickness dispersion  
a)  $\text{SiO}_2$  thickness mapping; b)  $\text{Si}_x\text{N}_y$  thickness mapping

As previously mentioned the material residual stress has to be as small as possible. For the grown wet **SiO<sub>2</sub>** and **LPCVD Si<sub>x</sub>N<sub>y</sub>**, the residual stress is reported in Table 4-6.

**Table 4-6** Characterized residual stress for selected deposited or grown materials (data from IEMN clean room database)

<i>Material</i>	<i>Stress</i> (MPa)	<i>Stress type</i>
Wet SiO <sub>2</sub>	-0.10	Compressive
Dry SiO <sub>2</sub>	-56.44	
Low stress Si <sub>x</sub> N <sub>y</sub>	29.40	Tensile
Stoichiometric Si <sub>3</sub> N <sub>4</sub>	622.40	

From data presented in Table 4-6, it can be remarked that wet **SiO<sub>2</sub>** and **Si<sub>x</sub>N<sub>y</sub>** have the smallest absolute value of the residual stress among all presented materials. When the materials with small residual stress are used the possible structure bending due to stress relaxation is significantly reduced. Focusing one more time on Table 4-6 it is worth noting that **SiO<sub>2</sub>** and **Si<sub>x</sub>N<sub>y</sub>** have different stress type. **SiO<sub>2</sub>** features compressive stress while **Si<sub>x</sub>N<sub>y</sub>** exhibits tensile stress. The opposite nature of stress is here an advantage because of compensation. Thus the resultant stress of the stack composed of **Si<sub>x</sub>N<sub>y</sub>** and **SiO<sub>2</sub>** is lower than for **Si<sub>x</sub>N<sub>y</sub>** only.

#### 4.3.2.1 Alignment markers and **STEP 2** – openings of cavities

Although the fabrication of alignments marks is not included in Fig. 4-6, it is performed just before **STEP 2** in a very similar way. Only one distinguishing difference can be highlighted between the fabrication of alignment marks and the opening of the cavities (**STEP 2**). In this section, the alignment markers and the procedure of cavities opening is described.

The fabrication of alignment marks is achieved using electronic beam lithography with a positive resist (**PMMA**)<sup>26</sup>. The resist spin coating procedure is described in Table 4-7. Spin-coating consists in seven inner actions. The spin-coating procedure listed in the Table 4-7 results in the uniform ~1.8µm thick layer of the EL13%-MAA8.5 resist. The resist layer thickness was characterized using a profile measurement gauge Fig. 4-9. Thick resist layer is used to ensure that the resist will remain during the long etching steps used for structure alignment marks and cavities.

<sup>26</sup> **PMMA** - Poly(Methyl MethAcrylate) also known as acrylic glass. Widely used in various industrial branches, in semiconductor research and industry it is used as a base for positive electron lithography resists. The advantage of **PMMA** resist is their high resolution

Table 4-7 Resist spin-coating procedure

No.	Process	Specification	Description
2-1	Micro-wave oxygen plasma cleaning	Power	700W
		O <sub>2</sub> flow	525cm <sup>3</sup> /min
		Duration	15min
2-2	Pre-coating heating on heating plate	Temperature	80°C
		Duration	1-2min
2-3	Cooling the wafer to room temperature	Duration	1-2min
2-4	Spin-coating	Resist ID	EL13%-MAA 8.5
		Speed	1000rpm
		Acceleration	1000rpm/s
		Duration	12s
2-5	Post spin-coating annealing on heating plate	T <sub>START</sub>	80°C
		T <sub>END</sub>	180°C
		Speed	7-10°C/min
2-6	Post spin-coating annealing on heating plate	Temperature	180°C
		Duration	10min
2-7	Cooling the wafer to the room temperature	Duration	1-2min

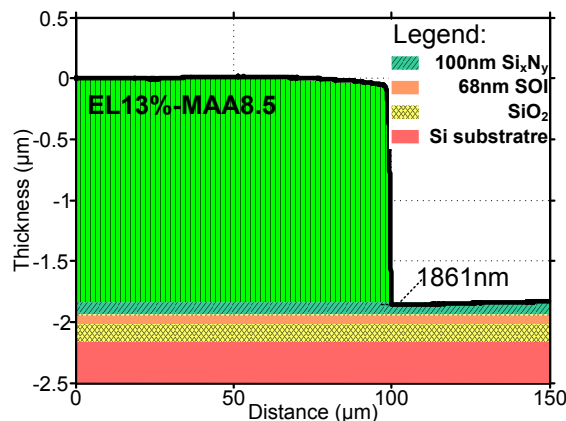


Fig. 4-9 Resist thickness measurement spin-coated using the recipe given in Table 4-7

The lithography process is subsequently performed as detailed in Table 4-8.

Table 4-8 Lithography description for alignment markers exposure (*same exposure parameters are used for cavities*)

<i>No.</i>	<i>Process</i>	<i>Specification</i>	
2-8	Lithography exposure	Dose	450 $\mu$ C/cm <sup>2</sup>
		Current	25nA
		Beam step size	25nm
		Alignment markers layer n°16	
		Exposed layer	OR Cavities openings layer n°3

After electron beam exposure, resist is developed as summarized in Table 4-9.

Table 4-9 Development procedure

<i>No.</i>	<i>Process</i>	<i>Specification</i>	
2-9	Development	Development	30ml MIBK+60ml IPA
		Duration	60s
		Agitation	100-130rpm
2-10	Post development treatment	Iso-propanol ( <i>IPA</i> ) rinse	30sec
		Nitrogen dry blow	Till the wafer is dry

After development, the next step consists in etching alignment markers and cavities using **Reactive Ion Etching (RIE)**. Etching recipe is detailed in Table 4-10. When etching the alignments markers, very deep etching is required to facilitate the marker localization during the lithography exposure. Deep markers can be easily localized by the lithography machine because it uses an electron beam contrast method to localize the marker. When performing the etching of the cavities, the etching is completed when the **Box** is etched exposing the top surface of the **Si** handler. Short etching time reduces **SOI** lateral etching that must be avoided. For this reason the etching of alignment markers and of cavities cannot be performed at the same time and has to be realized in two separate steps.

Table 4-10 Alignment markers and openings for cavities etching procedure

No.	Process	Target material(s)	Specification	Description	
2-11	Etching	100nm $\text{Si}_x\text{N}_y$ ; 12nm wet $\text{SiO}_2$ ; 68nm $\text{SOI}$	Power	30W	Recipe for 100nm thick $\text{Si}_x\text{N}_y$ ; 12nm thick wet $\text{SiO}_2$ and 68nm $\text{SOI}$ etching
			$\text{SF}_6$ flow	$10\text{cm}^3/\text{min}$	
			Ar flow	$10\text{cm}^3/\text{min}$	
			Pressure	10mTorr	
			Strike	50/0/5	
		145nm $\text{SiO}_2$ (Box)	Power	100W	Recipe for 145nm thick $\text{SiO}_2$ (Box) etching
			$\text{CF}_4$ flow	$40\text{cm}^3/\text{min}$	
			$\text{N}_2$ flow	$40\text{cm}^3/\text{min}$	
			$\text{O}_2$ flow	$5\text{cm}^3/\text{min}$	
			Pressure	10mTorr	
			Strike	50/0/9	
		$\text{Si}$ substrate	Power	30W	Recipe for $\text{Si}$ substrate over etching. <i>Performed only for alignment markers etching.</i>
			$\text{SF}_6$ flow	$10\text{cm}^3/\text{min}$	
			Ar flow	$10\text{cm}^3/\text{min}$	
			Pressure	10mTorr	
			Strike	50/0/5	
2-12	Resist stripping	EL13%-MAA8.5	Duration	Min. 2h	Resist stripping from the wafer using Remover PG preheated to 65°C.
			Product	Remover PG@65°C	
			Rinsing	Acethone+IPA	
			Drying	Nitrogen dry blow	

The etching procedure detailed in Table 4-10 allows fabricating the alignment markers and the openings for the cavities. A part of this recipe is also used when  $\text{Si}_x\text{N}_y$  is removed from the membrane (**STEP 6**) and for wet  $\text{SiO}_2$  etching from the cavity bottom to expose the  $\text{Si}$  substrate (**STEP 7**).

During the etching of the alignment markers and of the cavities, the end point detection signal is measured which enables precise control over the etching process allowing to change the etching recipe according to the target material or stopping the etching when needed (e.g. when the **Box** is completely etched through). Knowing the thickness of each layer of the stack to etch (depicted in Fig. 4-7 and Fig. 4-8) and the end point detection signal, it is also possible to calculate the etching rate. Fig. 4-10 presents the end point detection signal, etched profile characterization and the **SEM** pictures of the etched alignment markers (Fig. 4-10a,b and c) and the cavities (Fig. 4-10d,e and f).



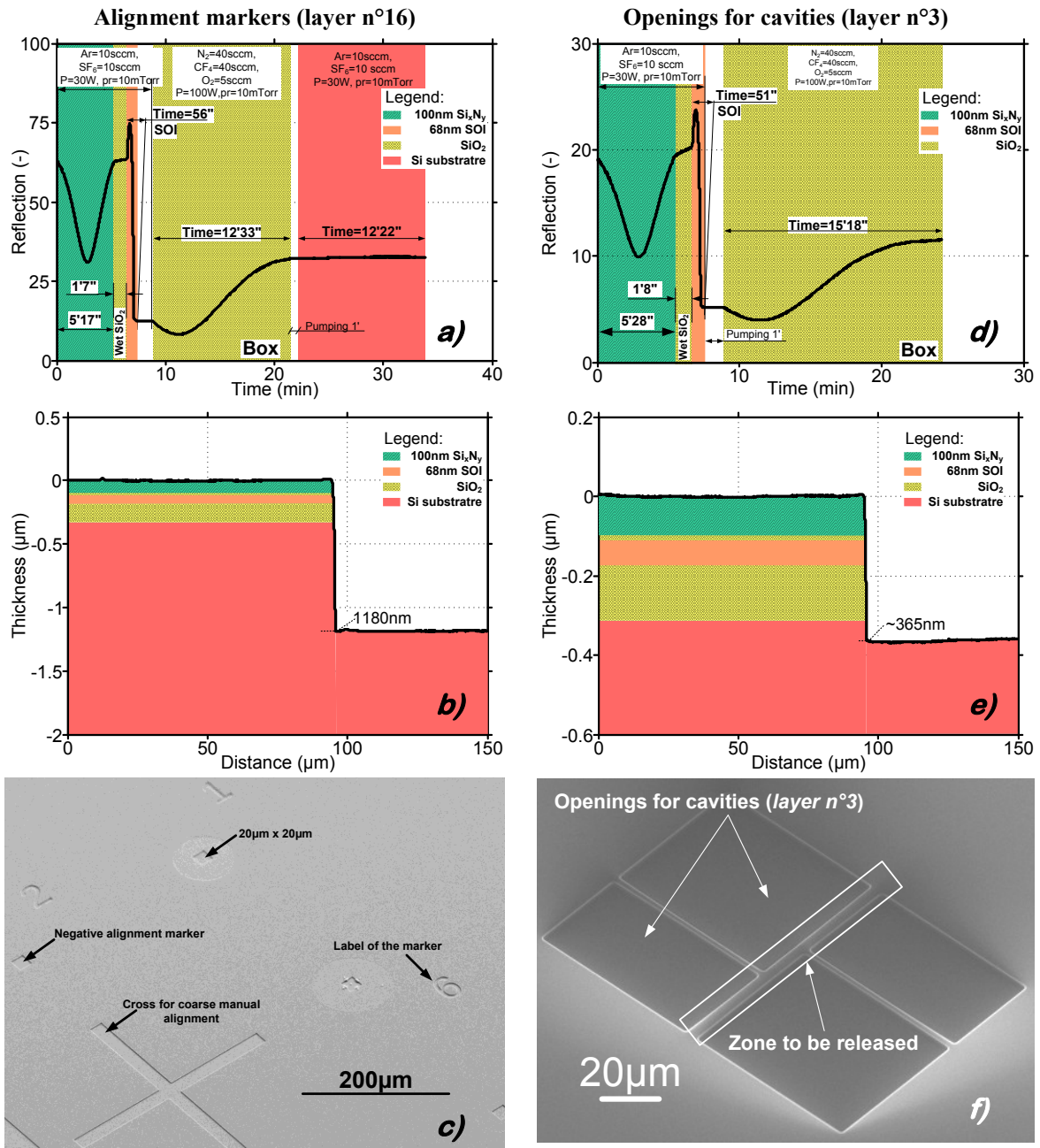


Fig. 4-10 End point detection signal, profile measurement and SEM picture of alignment markers a) to c) respectively. End point detection signal, profile measurement and SEM photo for cavities openings d) to f) respectively.

Comparing the end point detection signals when etching alignment markers (Fig. 4-10a) and when etching openings for the cavities (Fig. 4-10d), it can be remarked that both measured end point signals have the same shape. However, the measured reflection signal is not the same in both cases. The **Y**-axis in the Fig. 4-10a and Fig. 4-10d has a relative scale and depends largely on the **RIE** chamber state. Thus it is not possible to reproduce exactly the same conditions for separately performed etchings. The crucial information arising from the Fig. 4-10a and Fig. 4-10d is the shape of the signal and the time at characteristics points of the signal. The shape of the signal indicates which layer of the stack is being etched (*the colour backgrounds are indicating the part of the end point detection signal which corresponds to the given material*). Knowing the thickness of each layer of the stack and the corresponding etching time, it is possible to calculate the etching rate which is presented in the Table 4-11:

Table 4-11 Etching rates for used etching recipes and etched materials

<i>Material</i>	<i>Thickness</i>	<i>Average etching time</i>	<i>Etching rate</i>	<i>Etching recipe</i>
	(nm)	(min sec)	(nm/min)	
Low stress Si <sub>x</sub> N <sub>y</sub>	96.95 <sup>+0.73</sup> <sub>-0.55</sub>	5'22"	18.065 <sup>+0.14</sup> <sub>-0.10</sub>	SF <sub>6</sub> =10cm <sup>3</sup> /min; Ar=10cm <sup>3</sup> /min; pr=10mTorr; P=30W
Wet SiO <sub>2</sub>	12.31 <sup>+4.67</sup> <sub>-1.99</sub>	1'7"30	10.94 <sup>+4.15</sup> <sub>-1.77</sub>	
SOI (Si)	67.95 <sup>+0.28</sup> <sub>-0.50</sub>	57"30	70.90 <sup>+0.29</sup> <sub>-0.52</sub>	
Si substrate	855.68	12"22	69.19	
EL13%-MAA8.5	1800 <sup>+50</sup> <sub>-50</sub>	39'41"	45.36 <sup>+1.26</sup> <sub>-1.26</sub>	
SiO <sub>2</sub> (Box)	146.94 <sup>+3.10</sup> <sub>-7.69</sub>	13'55"	10.56 <sup>+0.22</sup> <sub>-0.55</sub>	CF <sub>4</sub> =40cm <sup>3</sup> /min; N <sub>2</sub> =40cm <sup>3</sup> /min; O <sub>2</sub> =5cm <sup>3</sup> /min; pr=10mTorr; P=100W
Si substrate	40.68	3'30"	11.62	

The above table presents the etching rates calculated based on the **ELL** thickness measurements (depicted in Fig. 4-7 and Fig. 4-8) and the etching times retrieved from the end point detection signal. The etching rates are presented for different materials and etching recipes. Comparing the **Si** etching rates for different recipes, it can be remarked that the recipe based on the **SF<sub>6</sub>** is etching **Si** much faster than when using **CF<sub>4</sub>**. Moreover, focusing now on the **SiO<sub>2</sub>** etching rate for the presented recipes, it can be pointed out that the etching rate is comparable when using **CF<sub>4</sub>** or **SF<sub>6</sub>**. There are two reasons why during **Box** etching the recipe is switched from a **SF<sub>6</sub>** chemistry (used to etch **Si<sub>x</sub>N<sub>y</sub>**, **SOI** and wet **SiO<sub>2</sub>**) to **CF<sub>4</sub>** chemistry. Firstly, the recipe based on the **CF<sub>4</sub>** gives more vertical **Box** sidewalls, which is desired. Secondly, when using the recipe based on the **SF<sub>6</sub>** for **Box** etching the sidewalls of the **SOI** which are exposed to **SF<sub>6</sub>** are being laterally etched. This results in unacceptable lateral etching of the **SOI** layer. To reduce this effect the chemistry transition is required when etching **Box**. Fig. 4-11 compares the cross-sectional view on **SOI** wafer etched using only recipe based on the **SF<sub>6</sub>** and using composite chemistry for **Box** etching Fig. 4-11b. Comparing the etching quality presented on the Fig. 4-11, it can be concluded that using only the etching recipe based on the **SF<sub>6</sub>** and **Ar** results in unacceptable lateral etching of **SOI**. However, when etching the alignment markers, a long **Si** substrate over etching is performed to achieve as deep as possible markers. During **Si** substrate etching the **SF<sub>6</sub>** and **Ar** are used as etchants, the **Si** substrate etching is very long 12min22sec (see Fig. 4-10a), thus the lateral etching of the **SOI** occurs. However, for the alignment marks quality, the above described **SOI** lateral etching is not critical and thus does not cause any difficulty for their localization during the lithography.

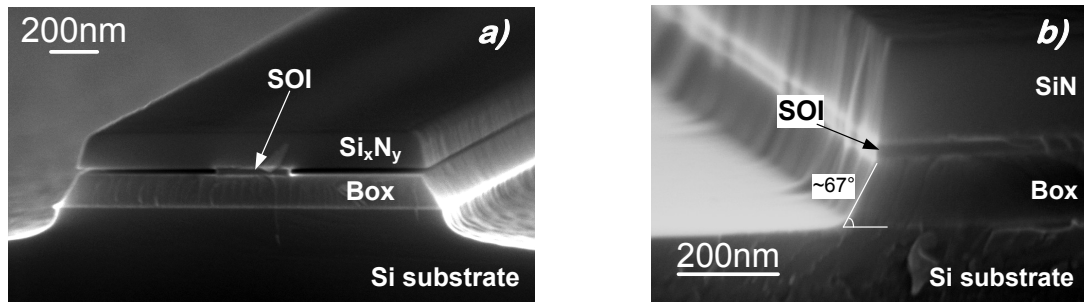


Fig. 4-11 Sidewalls of *SOI* wafer with  $\text{Si}_x\text{N}_y$  etched a) using only  $\text{SF}_6$  and Ar for etching all materials, b) using  $\text{CF}_4$ ,  $\text{N}_2$ ,  $\text{O}_2$  when etching Box and  $\text{SF}_6$ , Ar for  $\text{Si}_x\text{N}_y$ , wet  $\text{SiO}_2$  etching

### 4.3.3 STEP 3 – sidewall protection

After performing the cavities etching, the *SOI* sidewalls are not anymore covered as it is clearly shown in Fig. 4-11. To protect the *SOI* from the chemical attack which can occur during the following technological steps, wet  $\text{SiO}_2$  is grown only at places where the *Si* is exposed (*sidewalls of the SOI and the bottom of the cavities*). Just before the  $\text{SiO}_2$  growth, the wafer is immersed in the 5% *HF* acid for 1min. The same as previously described wet  $\text{SiO}_2$  fabrication procedure is used (see Table 4-4). The result of the wet  $\text{SiO}_2$  growth on the sidewall of the *SOI* is presented in Fig. 4-12:

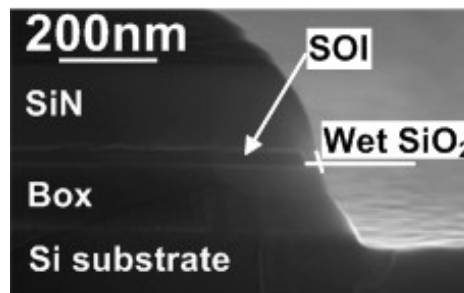


Fig. 4-12 The *SOI* sidewall protection fabricated using wet  $\text{SiO}_2$  thermal growth

This protection is required before **STEP 8**. However, it is impossible and prohibited to thermally grow  $\text{SiO}_2$  on wafers where metal layers are already present. The reasons are twofold: (i) firstly, the metal will contaminate the oven used for thermal oxide growth and (ii) secondly, the temperature used in the process of thermal growth ( $850^\circ\text{C}$ ) will result in possible metal melting and vaporization. Due to those technological reasons, the *SOI* protection has to be performed before the metallization.

### 4.3.4 STEP 4 and STEP 5 – platinum and gold metallization

The parts of the layout which are used as heating and sensing elements are made of platinum (**Pt**) tracks and the measurement pads are fabricated in gold (**Au**).

The metal tracks used in this device to generate the heat and to measure the temperature (see Fig. 4-4) as well as all devices (see Fig. 4-3) and cell label (see Fig. 4-2) are made in **Pt**. For  $\kappa$  measurements **Pt** is used because its electrical conductivity ( $\sigma$ ) exhibits a linear dependence on temperature [Powell, 1962], [Moore, 1973]. Moreover, the linear dependence of  $\sigma$  on the temperature occurs also in the thin-film **Pt** layers [Zhang, 2005]. Owing to this property, **Pt** is very often used for temperature measurements

e.g. thermistors. In this case the linear dependence of  $\sigma$  on the temperature largely simplifies the measurement procedure.

**Pt** tracks integration is performed using the following procedure. Firstly, the positive tone EL13%-MAA8.5 resist is spin coated on the wafer according to procedure specified in the Table 4-7. Electron beam lithography is subsequently performed according to the details listed in Table 4-12:

**Table 4-12 Lithography exposure specification for platinum metallization layer n°26**

No.	Process	Specification	
		Dose	450 $\mu$ C/cm <sup>2</sup>
4-1	Lithography exposure	Current	10nA
		Beam step size	10nm
		Exposed layer	Platinum metallization layer n°26

The metallization is performed by evaporation. This technique enables the deposition of very thin layers of metals, desired **Pt** thickness is 30nm.

It is worth noting that prior to metal evaporation, an argon (**Ar**) etching step is implemented to increase metal adhesion onto the host substrate. Owing to that **Ar** etching the risk of metal peel-off from the wafer is reduced. The evaporation covers completely the wafer with the metal. However, only in the exposed and developed places the metal is in direct contact with the wafer, otherwise the metal is deposited on the remaining resist. Removing the resist will also remove all metal deposited on it, only the metallic structures deposited directly on the wafer will remain. This process is called lift-off and is detailed in Table 4-13:

**Table 4-13 Lift-off procedure specification**

No.	Process	Target material(s)	Specification		Description
			Duration	Min. 2h	
2-4	Lift-off	EL13%- MAA8.5	Product	Remover PG@65°C	Lift-off using Remover PG preheated to 65°C.
			Rinsing	Acethone+IPA	
			Drying	Nitrogen dry blow	

Fig. 4-13a shows the **SEM** picture of the device, after performing **Pt** metallization. The **Pt** elements are well defined and have no defects, simultaneously the cavities opening are visible. The heater and the sensors fabricated in **Pt** are connected to gold (**Au**) measurement contact (*fabricated in the next step*) through the pads as shown in Fig. 4-13a. Fig. 4-13b shows the profile measurement of the evaporated **Pt** layer that matches the desired thickness of 30nm.

When **Pt** metallization is completed, the subsequent **Au** metallization is realized. The **Au** is used to structure pads for contacting the measurement probes. Pure **Au** is chosen for measurement pads because it is very soft material with 188–245 MPa of hardness in Brinell scale [Shackelford, 2000]. Owing to that the measurement probe-pad contact resistance is reduced by low interface resistance.

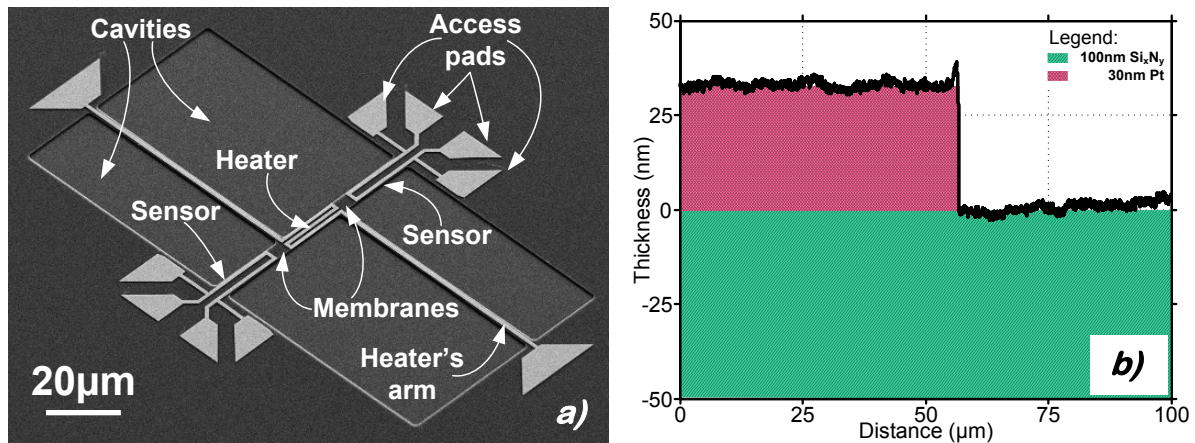


Fig. 4-13 Platinum metallization characterization a) SEM photo detailing the fabricated parts of the device, b) Platinum profile measurement characterizing the *Pt* evaporated thickness

The **Au** metallization is performed in similar way to above described **Pt** metallization. Firstly, the spin coating is realized according to specifications detailed in Table 4-7. Afterwards, the lithography of layer n°27 is performed using the parameters listed in Table 4-14. The measurement pads are the biggest part of the designed device (*see Fig. 4-3*), using low exposure current and precise beam step size will result in very long exposure time. To avoid it the current and beam step size are raised, in contrast to the lithography exposure for **Pt** elements where a precise exposure is needed.

Table 4-14 Lithography exposure specification for gold metallization layer n°27

No.	Process	Specification	
4-5	Lithography exposure	Dose	450µC/cm <sup>2</sup>
		Current	50nA
		Beam step size	25nm
		Exposed layer	Gold metallization layer n°27

After the lithography the development is performed according to the specification detailed in the Table 4-9. Consequently, **Au** is evaporated on the wafer using the sequence specified in the Table 4-15:

Table 4-15 Specification of the gold metallization

No.	Process	Specification	
4-6	Pre-evaporation Argon etching	Energy	200eV
		Time	2min
4-7	Chrome adhesion layer evaporation	Thickness	15nm
4-8	Gold evaporation	Thickness	250nm

According to Table 4-15 a thin 15nm adhesion layer of chrome (**Cr**) is evaporated after the **Ar** etching. The adhesion layer is used to avoid the peeling-of the **Au**. The **Cr** layer also serves as a barrier to avoid **Au** out diffusion towards silicon. After evaporation the lift-off is performed according to the same procedure as for **Pt** (*look Table 4-13*).

After performing the lift-off, **Au** contact pads are transferred onto the wafer and are ready for use. Fig. 4-14a shows the **SEM** photo of the full cell. It is visible that the measurement pads are well defined and that no peel-off occurred. Evaluation of the evaporated **Au** thickness is checked by a stylus profilometer as depicted in Fig. 4-14b.

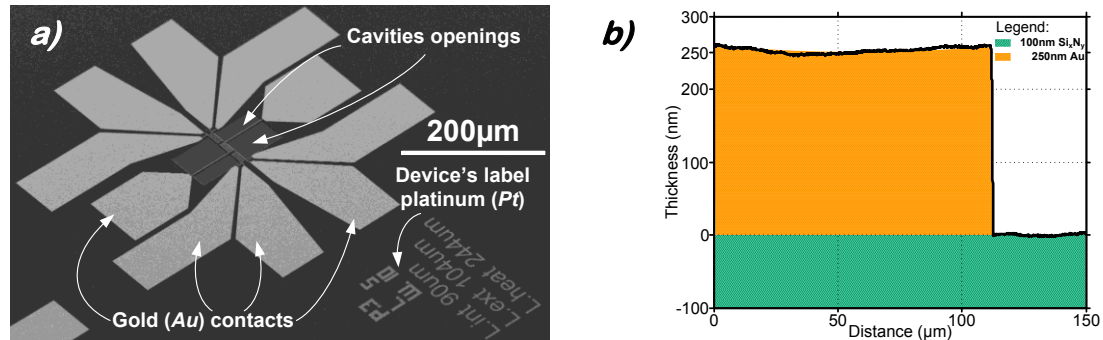


Fig. 4-14 Gold metallization characterization a) SEM photo detailing the fabricated parts of the device; b) Gold profile measurement characterizing the **Au** evaporated thickness

#### 4.3.5 STEP 6 – $\text{Si}_x\text{N}_y$ removal from the membrane

To favour heat transfer along the **SOI** membrane, the top  $\text{Si}_x\text{N}_y$  has to be selectively removed between the sensor and the heater. Owing to the removal of  $\text{Si}_x\text{N}_y$  from the **SOI** membrane,  $\kappa$  measurement is more precise. In other words the temperature rise measured by the sensor derives totally from  $\kappa$  of the characterized **Si** membrane.

$\text{Si}_x\text{N}_y$  removal from the membrane is performed using **RIE**. To define the regions where  $\text{Si}_x\text{N}_y$  has to be removed, the following sequence of technological operations is required. Firstly, the resist is spin-coated according to the procedure detailed in Table 4-7. Afterwards, the lithography is performed using following exposure parameters:

Table 4-16 Lithography exposure specification for  $\text{Si}_x\text{N}_y$  removal from the membrane layer n°21

No.	Process	Specification	
6-1	Lithography exposure	Dose	450µC/cm <sup>2</sup>
		Current	20nA
		Beam step size	10nm
		Exposed layer	$\text{Si}_x\text{N}_y$ removal from the membrane layer n°21

After the lithography exposure, the wafer is developed according to the recipe detailed in Table 4-9. The etching recipe (*gas composition, power, pressure etc.*) is identical to the previously used when fabricating of the alignment markers or openings of cavities. The used etching recipe is detailed in Table 4-10, and is based on the **SF<sub>6</sub>** and **Ar** chemistry. The wafer stack is prepared in such a way that the top-most material is  $\text{Si}_x\text{N}_y$  with wet **SiO<sub>2</sub>** underneath. This layer of thermally grown **SiO<sub>2</sub>** is crucial in this step because it is used as an etch-stop sacrificed layer. Due to this layer, it is possible to etch completely the  $\text{Si}_x\text{N}_y$  without damaging the **SOI** membrane because of this wet **SiO<sub>2</sub>** protection. Referring to Table 4-11, the etching rates of the **SF<sub>6</sub>/Ar** chemistry are 18.04nm/min and 10.94nm/min for  $\text{Si}_x\text{N}_y$  and **SiO<sub>2</sub>**, respectively. Thus,  $\text{Si}_x\text{N}_y$  is etched slightly faster than wet **SiO<sub>2</sub>** when **SF<sub>6</sub>** and **Ar** plasma etching is used. This is a desired situation to slightly over-etch  $\text{Si}_x\text{N}_y$ . The progress of  $\text{Si}_x\text{N}_y$  etching is measured using a end-point detection

signal. When  $\text{Si}_x\text{N}_y$  is etched and the  $\text{SiO}_2$  is exposed to the plasma the end-point signal shows a transition from a pseudo-sinusoidal to a linear shape as shown in Fig. 4-15a. This indicates that over-etching is started. To avoid the complete etching of wet  $\text{SiO}_2$  layer the over-etching cannot be too long. After **RIE**, the resist protecting the wafer from the plasma action is stripped using the procedure detailed in Table 4-10. Analyzing the profile measurement of  $\text{Si}_x\text{N}_y$  after resist stripping (depicted in Fig. 4-15b) it can be concluded that this layer is completely removed without damaging the **SOI** membrane.

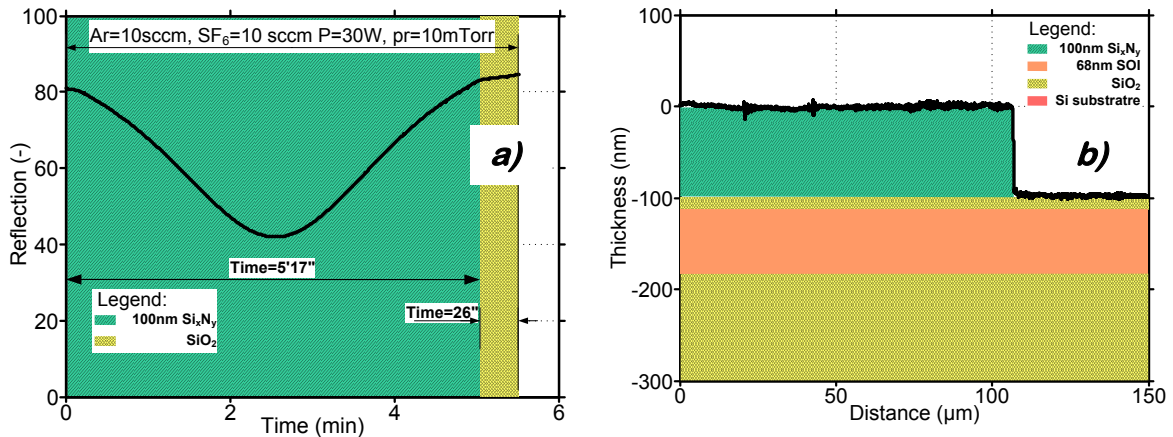


Fig. 4-15  $\text{Si}_x\text{N}_y$  etching from the membrane a) End-point detection signal measured during the etching sinusoidal and linear character marks the transition between  $\text{Si}_x\text{N}_y$  and wet  $\text{SiO}_2$ , b) profile measurement of 100nm thick  $\text{Si}_x\text{N}_y$  etched from the membrane.

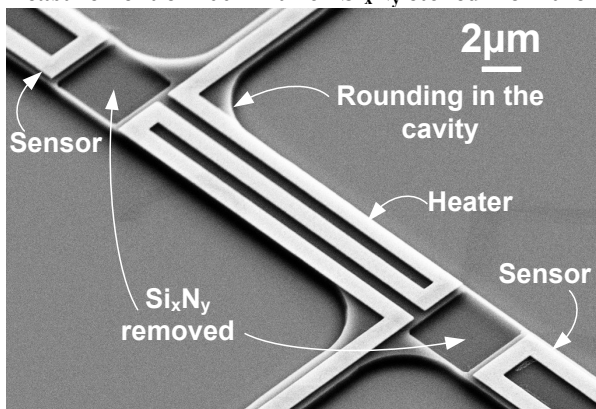


Fig. 4-16 SEM photo presenting the  $\text{Si}_x\text{N}_y$  removed from the membranes upon which the  $\kappa$  measurements will be performed. In between the heater and the sensors fabricated in **Pt** the removal of  $\text{Si}_x\text{N}_y$  is realized.

Finally, to complete the analysis of this technological step the **SEM** photo is provided in Fig. 4-16 which shows a zoom on two membranes with removed  $\text{Si}_x\text{N}_y$ .

The  $\text{Si}_x\text{N}_y$  removal from the membrane is one of the most difficult steps in the process flow because it is easily possible to destroy the **SOI** membrane when performing a too long etching. Conversely, a too short etching will not remove completely  $\text{Si}_x\text{N}_y$  which will create a parasitic thermal path between heater and sensor.

#### 4.3.6 STEP 7 – **Si** substrate exposure

In **STEP 3**, the sidewall protection fabricated using a 12nm thick wet  $\text{SiO}_2$  growth was performed (according to the fabrication procedure detailed in Table 4-4). The silicon dioxide is growing where the **Si** is exposed to the oxidizing agents. Thus, the wet  $\text{SiO}_2$  is grown on the sidewalls of the **SOI** and at the bottom of the cavities. The etching of the **Si** substrate in the cavities is possible only when the **Si** is exposed, thus the  $\text{SiO}_2$  has to be selectively removed only from the cavities without suppressing the wet  $\text{SiO}_2$  used as a sidewall protection of the **SOI**. To achieve this goal, a lithography step is realized to define the zones where the wet  $\text{SiO}_2$  will be exposed to the etching process. Simultaneously the

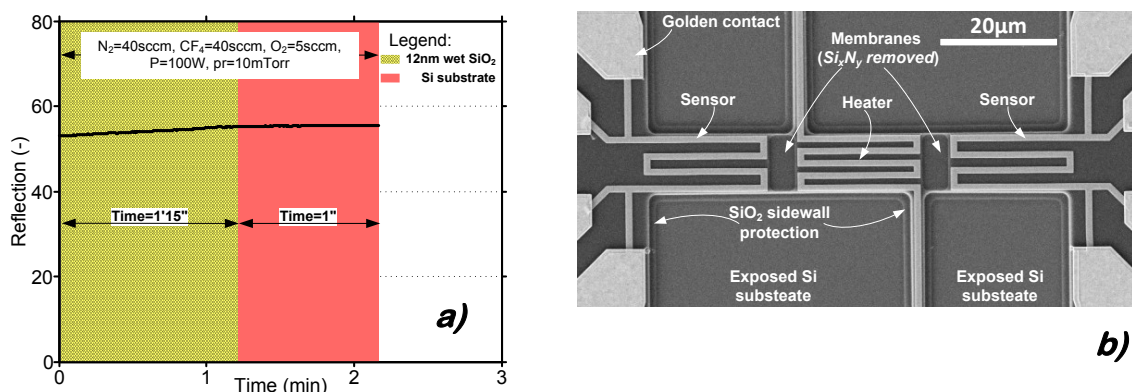
exposed layer is protecting the sidewalls protections of the **SOI** from the etching process. In such case only the **SiO<sub>2</sub>** placed on the bottom of the cavities will be exposed to the etching.

To integrate the exposed layer into the device the lithography process is needed. Lithography is possible only when the electro-sensitive resist is spin-coated on the wafer. The spin coating procedure is detailed in Table 4-7. After spin coating, the lithography exposure is realized following the procedure detailed in Table 4-17. When the lithography is completed, the development of the wafer is performed according to the specification listed in Table 4-9.

**Table 4-17 Lithography exposure specification for SiO<sub>2</sub> removal from the cavities layer n°2**

No.	Process	Specification	
		Dose	450 $\mu$ C/cm <sup>2</sup>
7-1	Lithography exposure	Current	25nA
		Beam step size	25nm
		Exposed layer	Sidewall protection layer n°2

The selective **SiO<sub>2</sub>** removal from the cavities is realized using **RIE**. The etching recipe is the same as for the **Box** etching when fabricating the alignment markers or the cavities. The etching procedure is based on a **CF<sub>4</sub>**, **N<sub>2</sub>** and **O<sub>2</sub>** chemistry. The details of the etching procedure are listed in Table 4-10. Referring to the end-point detection signals acquired for alignment markers (see Fig. 4-10a) or for the opening for the cavities (see Fig. 4-10d), it can be remarked that the etching rate when using **CF<sub>4</sub>**, **N<sub>2</sub>** and **O<sub>2</sub>** is around 10.5nm/min (see Table 4-11). Thus to etch 12nm thick wet **SiO<sub>2</sub>**, the etching time should be slightly longer than 1min. However, to achieve a good **Si** substrate exposure without the residues of silicon dioxide, the etching time can be extended. For fabricating this device, the etching time was two times longer than the aforementioned theoretical time. Using the extended etching time is not an issue in this step because the etching itself is short (around 2min15sec) and all important components are protected by the resist which is capable to withstand long etchings. When the etching is completed, the remaining resist is stripped following the specification detailed in sub-step 2-12 in Table 4-10.



**Fig. 4-17 SiO<sub>2</sub> etching from the cavity a) End-point detection signal measurement during the SiO<sub>2</sub> etching, b) SEM photo presenting the SiO<sub>2</sub> sidewall protection and exposed Si substrate in the cavities emphasizing the structural components of the proposed device**



Analyzing the end-point detection signal depicted in Fig. 4-17a it can be remarked that the signal is quasi-linearly rising when wet **SiO<sub>2</sub>** is etched. The constant value of the signal indicates that the **Si** substrate is reached. According to Fig. 4-17a, the wet **SiO<sub>2</sub>** etching time is 1'15" and the **Si** substrate over-etching is 1min. It can therefore be assumed that the **SiO<sub>2</sub>** is completely etched at the bottom of the cavities. The structural analysis after the **SiO<sub>2</sub>** etching from the cavities is illustrated in Fig. 4-17b. It can be noted that in the central parts of the cavities, the **Si** substrate is exposed while near the cavity borders the internal rectangle is visible which represents the **SiO<sub>2</sub>** sidewall protection.

#### 4.3.7 STEP 8 – **Si** substrate under etching

**STEP 8** has to be performed as quickly as possible after the **SiO<sub>2</sub>** removal from the cavity to reduce the formation of a native **SiO<sub>2</sub>**. After completion of the **SiO<sub>2</sub>** etching in the cavities, the **Si** substrate can be under-etched to release the membrane composed of **SOI** and **Box** stack. Releasing the **SOI-Box** membrane from the **Si** substrate requires an isotropic<sup>27</sup> etching procedure. During this step the **SOI-Box** membrane is released from the substrate. The theoretical thickness of this membrane is 68nm+146nm. Thus the etching has to be very soft mechanically and should not create any mechanical stress on the suspended membrane during etching. The most common procedures for **Si** etching are the wet etching techniques using preheated **KOH**<sup>28</sup> [Canavese, 2007], [Divan, 1999], [Palik, 1991], [Tanaka, 2004] or **TMAH**<sup>29</sup> [Liebert, 2002], [Powell, 2001], [Yang, 2005], [Tabata, 1992] solutions. However, neither **KOH** nor **TMAH** can offer the isotropic etching because the etching rate depends significantly on the crystalline orientation of **Si**. However, the use of wet **KOH** or **TMAH** etching for the release of thin-film membranes has been adopted by several groups [Cuffe, 2012], [Ftouni, 2012], [Sikora, 2012], [Shi, 2003], [Moser, 2012] etc. When wet etching is used to suspend **SOI-Box** membranes, backside etching has to be performed and the top **SOI** layer has to be protected against the etchant. The complete removal of the **Si** substrate with the thickness of several hundreds μm requires very long etching time. However, it has to be underlined that wet etching procedures can be destructive for the suspended ultra-thin membranes. Care must be taken when rinsing the wafer after etching, because of the stiction and capillary forces released while removing the wafer from the etchant solution. Nitrogen blow while drying the wafer is another critical step. Those effects are less important when the released layers are thick. To avoid the destruction of the suspended membranes due to the use of liquid solutions, a gaseous etchant can be used. In such a case **Si** can be etched using **XeF<sub>2</sub>**<sup>30</sup> in gaseous phase [Brazzle, 2004], [Winters, 1979], [Williams, 2003]. **XeF<sub>2</sub>** etching technique was adopted by numerous groups [Boukai, 2008], [Hopkins, 2011], [Kim, 2012], [Yu, 2010], [Tang, 2010] mainly because of isotropic etching, the mechanical

<sup>27</sup> Isotropic etching – the etching with identical etching rate in all directions. The etched material is removed by the etchant in the same quantity vertically and laterally [Williams, 2003]

<sup>28</sup> **KOH** - Potassium hydroxide: inorganic liquid solution used to anisotropic wet **Si** etching. The use of **KOH** is significantly hindered in modern nono-technology due to lower etching rates compared to **TMAH**.

<sup>29</sup> **TMAH** - Tetramethylammonium hydroxide: this is the liquid solution based on the **KOH** dedicated to etch **Si**. The etching rate is significantly dependent on the crystalline direction of the **Si** thus the etchant TMAH is not offering isotropic etching despite it is wet etching.

<sup>30</sup> **XeF<sub>2</sub>** - Xenon difluoride: the powerful fluorinating agent used as isotropic **Si** etchant. **XeF<sub>2</sub>** reacts with the **Si** in the following way [Brazzle, 2004]:  $2XeF_2(g) + Si \rightarrow 2Xe(g) + SiF_4(g)$

It is important to note that the etching reaction products are purely volatile which is indicated by (g) and can be easily evacuated. As a result no passivation occurs on the wafer.

stress reduction and the fantastic etching selectivity. The later allows adopting this etching procedure without using additional masks.

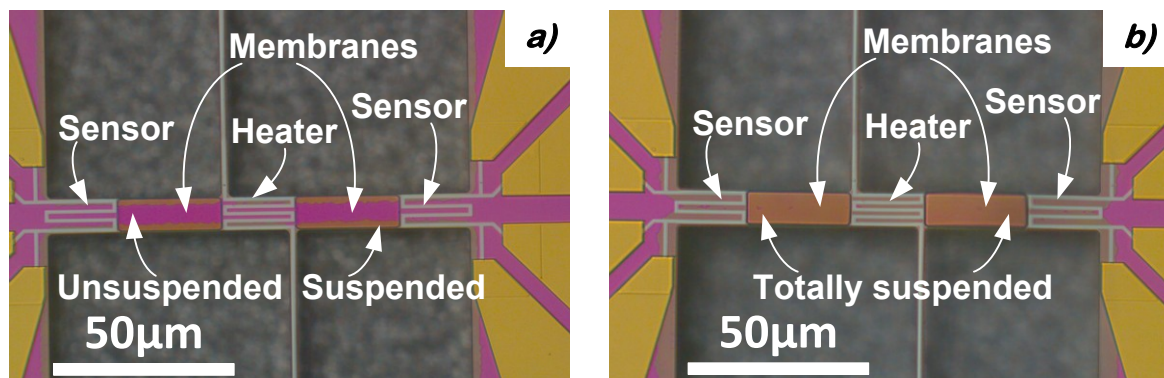
Device fabricated during this thesis was released from the **Si** substrate using dry **XeF<sub>2</sub>** etching. Etching is performed in cycles according to the specification listed in Table 4-18:

**Table 4-18 Si substrate under etching using XeF<sub>2</sub> in gaseous phase**

No.	Process	Specification	
		XeF <sub>2</sub> pressure	3.0 Torr
		Pump out pressure	0.8 Torr
		Single cycle duration	10s
8-1	Si substrate under etching	Number of cycles till complete suspension ( $W=10\mu\text{m}$ )	4
		Operating mode	Advanced normal
		Exposed layer	No layer exposed
		Calculated average etch rate	$\sim 1.25\mu\text{m}/\text{cycle}$

From Table 4-18, it can be remarked that etching using **XeF<sub>2</sub>** has completely different character than the previously used **RIE** methods. **XeF<sub>2</sub>** etching is realized in cycles. The etching chamber is filled up with the reactive gas under a pressure of 3.0 Torr and the etching reaction between the **XeF<sub>2</sub>** and **Si** lasts 10sec. Afterwards, unreacted **XeF<sub>2</sub>** together with the bi-products of the etching reaction (**Xe** and **SiF<sub>4</sub>**) are pumped out from the etching chamber. At the end of the pump out step, the chamber is filled up with the **N<sub>2</sub>**. The number of etching cycles depends on the **Si** volume to be etched (*assuming that the etching is perfectly isotropic*). To reach full suspension Silicon under the **SOI/Box** stack of the membrane must be completely eliminated over a distance equal to width (**W**) of the membrane (*see Fig. 4-4*). Naturally etching occurs from both sides of the membrane where the cavities are placed.

The etching by **XeF<sub>2</sub>** gives non-uniform etching rate per cycle. For cycles at the beginning of the etching, the removal rate is smaller than for the cycles at the end of the etching. This is caused by the presence of thin layer of native **SiO<sub>2</sub>** before introducing the wafer to the etching chamber in **STEP 8**. Between **STEP 7** and **STEP 8** **Si** is exposed to the ambient air leading to native **SiO<sub>2</sub>** growth. **XeF<sub>2</sub>** cycles at the beginning of the etching step have to cross this thin native **SiO<sub>2</sub>** layer before reaching **Si**. The formation of native



**Fig. 4-18 Si substrate under etching using XeF<sub>2</sub> in gaseous phase to release the membrane with  $W=10\mu\text{m}$ , a) Not completely suspended SOI-Box membrane after performing 2 cycles of XeF<sub>2</sub> etching, b) Completely released SOI-Box membrane after performing 4 cycles of XeF<sub>2</sub> etching**

$\text{SiO}_2$  on  $\text{Si}$  in the cavities requires use of adequate number of etching cycles. A too small number of etching cycles results in an incomplete suspension of the membrane as graphically presented in Fig. 4-18a. The unreleased part of the membrane features a different colour than the borders of the membrane which are suspended. When the cycle number is increased a complete suspension is achieved as showed in Fig. 4-18b. The fact that the etching rate is not constant during etching necessitates several iterations.

The suspension of the membrane releases residual material built up in the  $\text{Si}_x\text{N}_y$ , wet  $\text{SiO}_2$ ,  $\text{SOI}$  and  $\text{Box}$  layers. It results that the suspended membrane and cavity borders can be sagged in a metastable state upwards or downwards. The membrane bending is the source of significant mechanical problems for the designed structure. The stress can be localized in sharp corners of the design which favours the formation of cracks. To avoid this problem, all layers dedicated for etching processes (layer n°2, layer n°3 and layer n°21) have rounded corners with radius of  $R=0.5\mu\text{m}$ .

The above described phenomenon was observed in the early stage of this project where the openings for the cavities (layer n°3) were shaped as perfect rectangles with right angles in each corner. Such a situation resulted in the stress concentration and crack formation in the corners of the cavity as presented in Fig. 4-19.

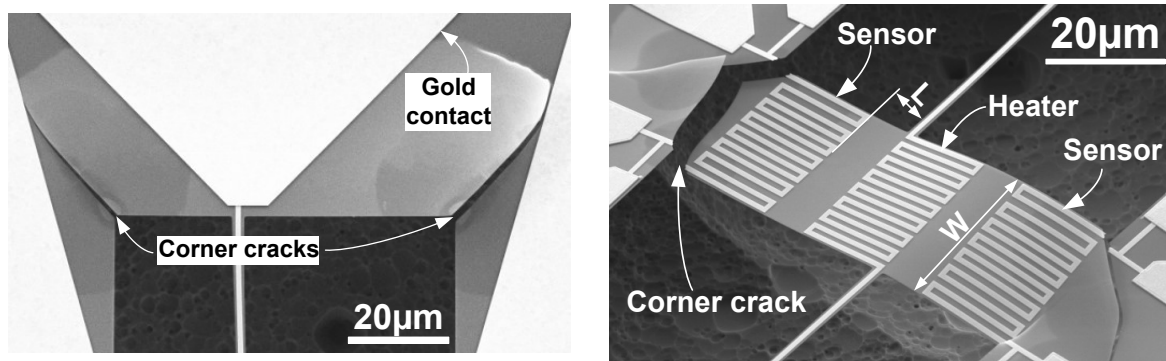
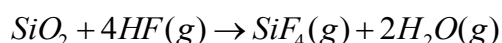


Fig. 4-19 Destructive corner cracks formation due to the stress concentration in the right angle in the cavities corners

Rounding the corners of the cavities distributes the stress on a larger surface in such a way that the corner cracks are avoided as shown in Fig. 4-18b. When  $\text{XeF}_2$  is performed to achieve complete suspension of the  $\text{SOI-Box}$  membrane the sample can be processed in the following step, which completes the process flow.

#### 4.3.8 STEP 9 – $\text{Box}$ under etching

The device fabrication is completed with  $\text{Box}$  etching from the membrane. This process can be realized using wet techniques by immersing the wafer in **HydroFluoric (HF)** acid. However, because of already discussed problems with stiction, capillary forces and nitrogen sample drying, the wet etching can be destructive for the suspended membranes. Thus dry etching of  $\text{SiO}_2$  using a vapour  $\text{HF}$  method [Bois, 2001], [Zhao, 2015]. Owing to the adoption of this technique, the mechanical stress occurring during etching is significantly reduced while the etching is performed in a low pressure environment. Moreover, as a result of the dry etching no rinse is needed after etching to remove a reactive solution or to dry the sample with nitrogen. The mechanism of  $\text{SiO}_2$  etching using  $\text{HF}$  gas ( $g$ ) is described by the following reaction [Zhao, 2015]:



**SiO<sub>2</sub>** reacts with **HF** and all the bi-products of this reaction are volatile which allows evacuating them easily from the etching chamber.

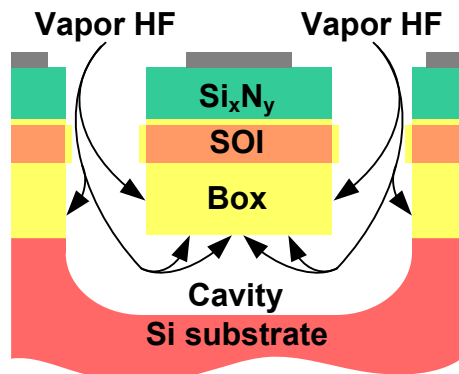
**HF** etching in the case under consideration is used to remove the remaining **SiO<sub>2</sub>** layers (*fabricated in the **STEP°1***) and on bottom of **SOI** (145nm thick **Box** layer). The etching is performed using the specifications detailed in Table 4-19:

**Table 4-19 Specifications of SiO<sub>2</sub> etching using vapour HF method**

No.	Process	Specification	
9-1	Pre-etching heating on heating plate	Temperature	260°C
		Duration	2min
9-2	Box under etching	HF flow	350 cm <sup>3</sup> /min
		C <sub>2</sub> H <sub>5</sub> OH flow	350 cm <sup>3</sup> /min
		N <sub>2</sub> flow	1250 cm <sup>3</sup> /min
		Single cycle duration	7min
		Number of cycles	1
		Etch rate*	37.4nm/min
9-3	Post-etching heating on heating plate	Exposed layer	No layer exposed
		Temperature	260°C
		Duration	2min

\*data from IEMN clean room database

Referring to Table 4-19, it can be remarked at first glance that the vapor **HF** etching sequence requires three sub-steps. Firstly, the sample is heated on the heating plate. This step is required to evaporate remaining residues of **IPA**, acetone or deionised water. Secondly, the sample is introduced in the etching chamber, and the vapour **HF** etching is performed. The etching is performed in cycles. After the completion of one cycle, **HF** is pumped out from the etching chamber (*if there is more than one etching cycles in the etching recipe*). Afterwards, the etching chamber is refilled with vapour **HF**. According to Table 4-19, only one etching cycle is used with duration of 7min. The theoretical etching rate of this recipe is 37.4nm/min which means that nearly 282nm of **SiO<sub>2</sub>** can theoretically be etched. During this etching, the most important layer to remove is the 145nm thick **Box**



**Fig. 4-20** Box etching using vapor HF. The **Box** is etched from the sides and from the bottom

located directly under the **SOI** membrane. The used etching recipe is thus much longer than the theoretical time needed to strictly remove the **Box**. Such a long etching is adopted because:

- **Box** is not well exposed to **HF**: the cavity has to be filled up with **HF** to react with the **Box** from the bottom and from the sides (*see Fig. 4-20*)
- The use of a single cycle means that the **HF** concentration decreases during etching (*till the SiO<sub>2</sub> is totally etched*). Thus the etching rate at the beginning is higher than at the end of the cycle. Etching time extension ensures that **SiO<sub>2</sub>** is totally removed despite a decreasing etching rate.

**HF** in gaseous phase is slightly altering and etching  $\text{Si}_x\text{N}_y$  (this etching does not occur for **HF** in liquid form). The etching time has therefore been optimized to achieve complete etching of  $\text{SiO}_2$  and to avoid additional etching of the  $\text{Si}_x\text{N}_y$  layer. After **HF** etching, the  $\text{Si}_x\text{N}_y$  layer is covered with white passivation layer which disappears when the sample is annealed. Etching is completed after sample annealing on the heating plate with temperature  $260^\circ\text{C}$  for 2min.

After **HF** etching no  $\text{SiO}_2$  remains neither on top nor on the bottom of the **SOI** membrane. The fabrication of **Si** suspended membrane is crucial for the accuracy of  $\kappa$  measurement because all heat generated in the heater can be transferred towards the sensors passing only through the suspended thin-film **Si** membrane. In other words,  $\text{Si}_x\text{N}_y$  removal from the membrane, **Si** substrate and the  $\text{SiO}_2$  under etching are limiting heater-sensor thermal coupling only to suspended **Si** membrane from which  $\kappa$  will be determined.

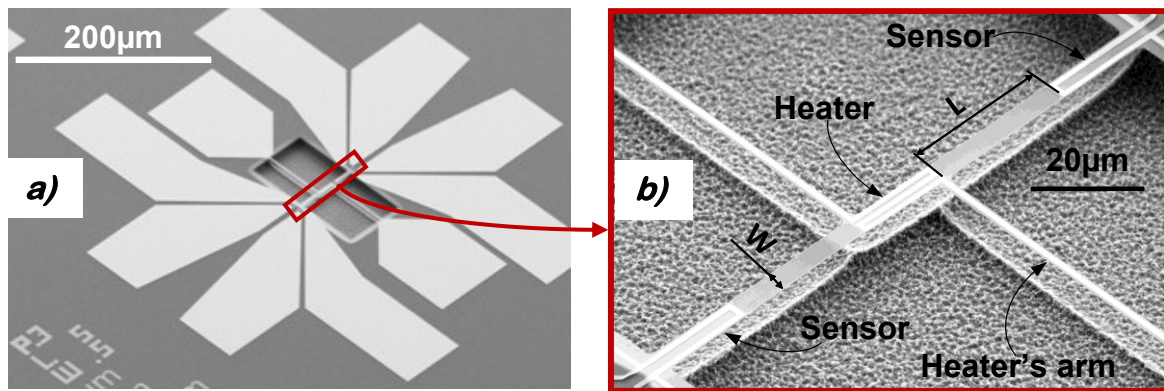


Fig. 4-21 Micrometer platform for  $\kappa$  measurement in thin-film **Si**, a) complete view on the device, b) zoom on the **Si** membrane

Vapour **HF** etching terminates the process flow. The device dedicated to  $\kappa$  determination in thin-film **Si** is showed on the pictures in Fig. 4-21. It can be remarked that the  $t=68\text{nm}$  thick **Si** membrane is suspended and thermal insulation between the suspended membrane and the substrate is confirmed. The distance between the **Si** membrane and the bottom of the cavity is at least equal to  $10\mu\text{m}$ . Comparing the depth of the cavity with the thickness of the suspended membrane ( $t=68\text{nm}$ ), it can be assumed that there is no heat losses from the membrane towards the **Si** substrate. Moreover, even if  $\text{Si}_x\text{N}_y$  is lightly etched when vapor **HF** is used, none of the device components (*heater, sensors or golden contacts*) are detached from the  $\text{Si}_x\text{N}_y$  underlayer. The **Pt** and **Au** metallization are not altered or deformed. Using dry etching techniques, ( $\text{XeF}_2$  and vapor **HF**), the membrane is not altered by the mechanical strains and stresses occurring when liquid etchants are used. However, the residual tensile stress in low stress  $\text{Si}_x\text{N}_y$  ( $29.4\text{MPa}$  look Table 4-6) tightens the suspended membrane. Thus neither upwards nor downwards membrane's bending occurs. This is an advantageous situation because the membrane is straight. Low stress  $\text{Si}_x\text{N}_y$  does not break the suspended thin-film but is sufficient to stretch the membrane making it flat.

On the fabricated wafer, the suspended membranes have  $W=5\mu\text{m}$  or  $W=10\mu\text{m}$  respectively, and separating distance between heater and sensor are  $L=5, 10, 20$  and  $30\mu\text{m}$  as shown in Fig. 4-2. The variation of  $L$  and  $W$  allows measuring  $\kappa$  for different dimensions and makes it possible to evaluate the impact of the membrane dimensions on the measured  $\kappa$  values.

After the description of the fabrication sequence, the following of this chapter describes the extraction of  $\kappa$  on 68 thick **Si** membranes.

## 4.4 Characterizing the device

The characterization method adopted in this project is based on electro-thermal approach. However, the proposed topology allows using other techniques to determine  $\kappa$  e.g. **SThM** or Raman spectroscopy. Because of the rectangular shape and of multiple materials (**Si<sub>x</sub>N<sub>y</sub>**, **Pt** and **SiO<sub>2</sub>**) present on the suspended **Si** membrane, the Raman spectroscopy results can be difficult to analyze but the measurement is feasible if the analysis is consolidated by an accurate model. **SThM** can also be made on the proposed topology but as in the case of Raman spectroscopy, multiple materials used in the stack makes the analysis complicated. This device is designed for the electro-thermal method which is the most comfortable and maybe the most accurate. The measurement principle, the description of the characterization protocol and the measured results will be discussed in the following sections.

### 4.4.1 Principle of the electro-thermal method to measure $\kappa$

The method is based on the assumption that the electrical power generated in the heater ( $P_H$ ) is totally transformed to the heat flow ( $Q$ ) through the Joule effect. Due to the high thermal insulation of the suspended membrane and reduction of the heat convection losses by performing the measurements in vacuum the  $P_H=Q$  relationship can be reasonably assumed. The heat flow  $Q$  generated in the heater is transferred to the suspended membrane as shown in Fig. 4-22. Because the heater-sensor thermal coupling only takes place through the suspended membrane,  $Q$  is exclusively directed to sensors. The membrane is symmetrical and the generated power in the central part of the membrane is divided into two identical contributions  $Q/2$  flowing towards each of the sensors located at opposite ends of the characterized membrane (Fig. 4-22). Transferred power alters the sensor resistance because of the local temperature raise. Knowing what are heater ( $T_H$ ) and sensor ( $T_S$ ) temperatures, the electrical power applied to the heater ( $P_H$ ), the width ( $W$ ), length ( $L$ ) and thickness ( $t$ ) of the membrane,  $\kappa$  can be determined using the Eq. 4-5:

$$\kappa = \frac{1}{2} \frac{P_H}{T_H - T_S} \cdot \frac{L}{W \cdot t} \quad \text{Eq. 4-5}$$

where:

$\kappa$	Thermal conductivity of the material with the thickness $t$ (W/m/K)
$P_H$	Heater electric power (W)
$T_H$	Heater temperature (K)
$T_S$	Sensor temperature (K)
$L$	Distance between heater and the sensor (m)
$W$	Width of the measured thin-film material (m)
$t$	Thickness of the measured thin-film material (m)

According to Eq. 4-5, the determination of  $\kappa$  requires the knowledge of  $T_H$  and  $T_S$  or of the temperature drop ( $\Delta T$ ) along the membrane. The determination of  $T_H$  and  $T_S$  is realized indirectly by the measurement of the heater and sensor electrical resistances at different temperatures. Both the heater and the sensor are made of **Pt** which exhibits a linear dependence between the electrical resistance and the temperature over a very wide temperature range.

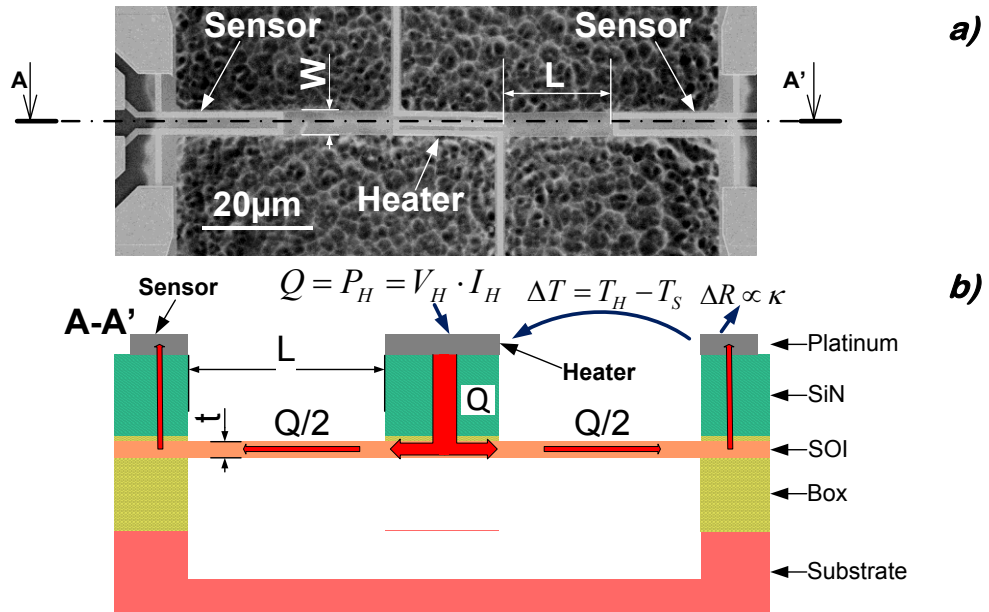


Fig. 4-22 Principle of electro-thermal  $\kappa$  measurement, a) Top view on the suspended membrane emphasizing the heater, the sensors, length ( $L$ ) and width ( $W$ ) of the membrane, b) Cross-sectional side view through the device along the A-A' cutline in the a)

Determination of  $T_S$  and  $T_H$  is possible based on the calibration of the sensor and heater performed before the  $\kappa$  measurement. The calibration of the *Pt* serpentes will be described in the following of this chapter.

#### 4.4.2 Measurement and calibration conditions

As mentioned before  $\kappa$  measurements as well as the heater and sensor calibrations are performed in vacuum. For this reason the heat convection which is the most important heat leakage mechanism, becomes negligible and the hypothesis that  $P_H=Q$  is close to reality. The characterized sample is placed in the vacuum chamber with four-point probe capabilities and equipped with the thermally controlled chuck. The chamber is pumped out to a pressure of  $p_r=3.5 \times 10^{-6}$  Torr ( $4.65 \times 10^{-6}$  mbar). The measurement setup is shown in Fig. 4-23a. Fig. 4-23b shows the placement of the sample in the vacuum chamber.

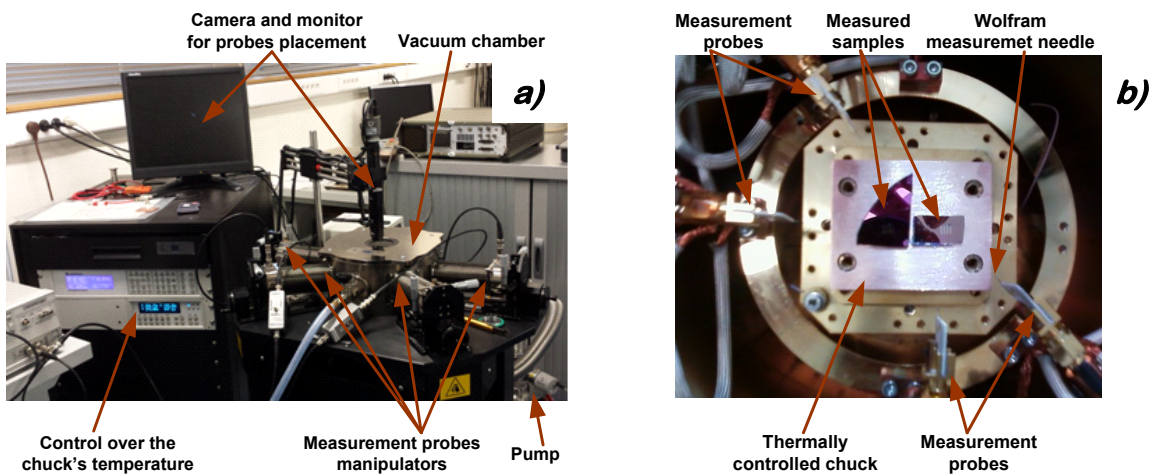


Fig. 4-23 a) Measurement set used during  $\kappa$  determination in thin film *Si* membranes, b) Characterized sample placement upon the thermally controlled chuck inside the vacuum chamber

The measurement probes are connected to an Agilent 4155C<sup>®</sup> semiconductor parameter analyzer which in this configuration is used as a precise voltage source and current, voltage measurement unit. Depending on the configuration ( *$\kappa$  measurement or calibration*) different measurement channels are used. The thermal chuck control allows setting and measuring the temperature with very high precision down to 0.001°C. The used measurement probes are all **DC** type with tungsten needles with a tip radius of  $R=25\mu\text{m}$ . The measurement equipment description is summarized in Table 4-20:

**Table 4-20 Measurement set equipment and conditions specification**

<i>Criteria</i>	<i>Unit</i>	<i>Value</i>			
Chamber pressure	mbar	Average		Minimal	Maximal
		$4.65 \times 10^{-6}$		$3.8 \times 10^{-6}$	$5.5 \times 10^{-6}$
Used chuck temperature range	°C	From ambient to 80			
Chuck temperature measurement precision	°C	0.001			
Chuck cheating/cooling technique		Electrical heating / unbounded cooling			
Number of used probes	unit	4			
Probes type		Direct Current			
Needle's material		Tungsten			
Needle's tip radius	$\mu\text{m}$	25			
Measurement probes configuration		Calibration		$\kappa$ measurement	
		Four-point probes resistance measurement		Two probes sensor and two probes heater resistance measurement	
Measurement device type		HP4155C			
Measurement cable type		Calibration		$\kappa$ measurement	
		2 triaxial 2 coaxial cables		4 triaxial cables ( <i>outer ground not connected</i> )	
Measurement cable length	m	Coaxial		Triaxial	
		1.5		3	0.3
		Coaxial		Triaxial	
Specific cable resistance	$\Omega/\text{m}$	Conductor	$160 \times 10^{-3}$	Inner conductor	$25 \times 10^{-3}$
		Screen	$15 \times 10^{-3}$	Inner screen	$12 \times 10^{-3}$

Table 4-20 does not specify the parameters of all equipments used in the experiments. The less important devices such as coaxial-biaxial connectors and their parasitic resistances are not included. However, their influence on the measurement precision is very low as well as the parasitic resistance of the cables.



### 4.4.3 Calibrations

As mentioned previously, the  $\kappa$  measurement requires the value of  $T_H$  and  $T_S$  which are found indirectly through the heater and sensor resistance measurement during the calibration steps. It is recalled here that the fabricated cells (see Fig. 4-2) feature only two widths  $W=5\mu\text{m}$  and  $10\mu\text{m}$  which impose different lengths of **Pt** metallization both for the heater and the sensors. Thus at least one heater and sensor calibration should be performed for each  $W$ . The distance between the heater and sensor does not influence the serpentine dimensionality and their theoretical resistance for the same  $W$  but different  $L$  is identical. In the following section, the serpentine calibration procedure is described.

#### 4.4.3.1 Sensor calibration

The sensor calibration involves the measurement of the **Pt** electrical resistivity ( $\rho_{Pt}$ ) using a four-point technique for different chuck temperatures ( $T_{CHUCK}$ ). The wiring configuration used during this calibration is depicted in Fig. 4-24a. From this figure it is visible that the sensor is supplied by **SMU**<sup>31</sup> units which are simultaneously used to measure the current. However, the voltage drop along the sensor is measured using **VMU**<sup>32</sup> units by extracting the difference  $VMU_1-VMU_2$ . The **VMU** unit is used because it has a significantly higher accuracy when measuring a voltage compared to a **SMU**.  $\rho_{Pt}$  is determined knowing the voltage drop across the sensor serpentine ( $VMU_1-VMU_2$ ), the current flowing via the sensor (measured by **SMU**) and the sensor dimensions. The measured is performed when thermal steady state is achieved to get a characterized sample with a uniform and constant temperature equal to  $T_{CHUCK}$ . A low sensor voltage  $V_S=10\text{mV}$  is applied to the sensor for 10s, followed by the calculation of the average value of  $\rho_{Pt}$ . When the measurement is completed,  $T_{CHUCK}$  is changed and after the system reaches another thermal steady state condition, the subsequent 10 seconds  $\rho_{Pt}$  measurement is repeated. The detailed specification for this calibration is listed in Table 4-21.

Fig. 4-24b and Fig. 4-24c presents the measured  $\rho_{Pt}$  versus  $T_{CHUCK}$  for membranes with  $W=10\mu\text{m}$  and  $W=5\mu\text{m}$ , respectively. At first glance, it can be remarked that for both characterized  $W$  values,  $\rho_{Pt}$  exhibits a linear dependency over the considered temperature range this is an expected and desired behaviour. Secondly, the measured platinum resistivity for  $W=5\mu\text{m}$  and  $W=10\mu\text{m}$  have almost the same values, which is also expectable keeping in mind that the resistivity is a parameter describing a material (**Pt**) property regardless of the dimensionality. The characteristics depicted in Fig. 4-24b and Fig. 4-24c are used to determine the temperature coefficient of the electrical resistivity  $\alpha_{Pt}=0.002242^\circ\text{C}^{-1}$ . The reported  $\alpha_{Pt}$  value for bulk **Pt** is  $\alpha_{Pt}=0.003927^\circ\text{C}^{-1}$  [Giancoli, 2008] or [Serway, 1998], which is higher than the measured  $\alpha_{Pt}$  of a 30nm thick evaporated **Pt** layer. The difference between the bulk and thin-film **Pt** can be explained by the different production method and the material morphology. This explains the reason why  $\alpha_{Pt}$  has to be characterized accurately and why the bulk value is not relevant. Comparing Fig. 4-24b and Fig. 4-24c, it can be remarked that  $\alpha_{Pt}$  slightly differs: it is slightly lower for membranes with  $W=5\mu\text{m}$ . However, it has to be underlined that the

<sup>31</sup> **SMU** – Source Monitor Unit HP4155C provides four **SMUs** which are programmable current or voltage sources. When the voltage source is specified the output current is measured.

<sup>32</sup> **VMU** – Voltage Measurement Unit in HP4155C two units are available. For voltage measurements the **VMU** has significantly higher precision than **SMU**

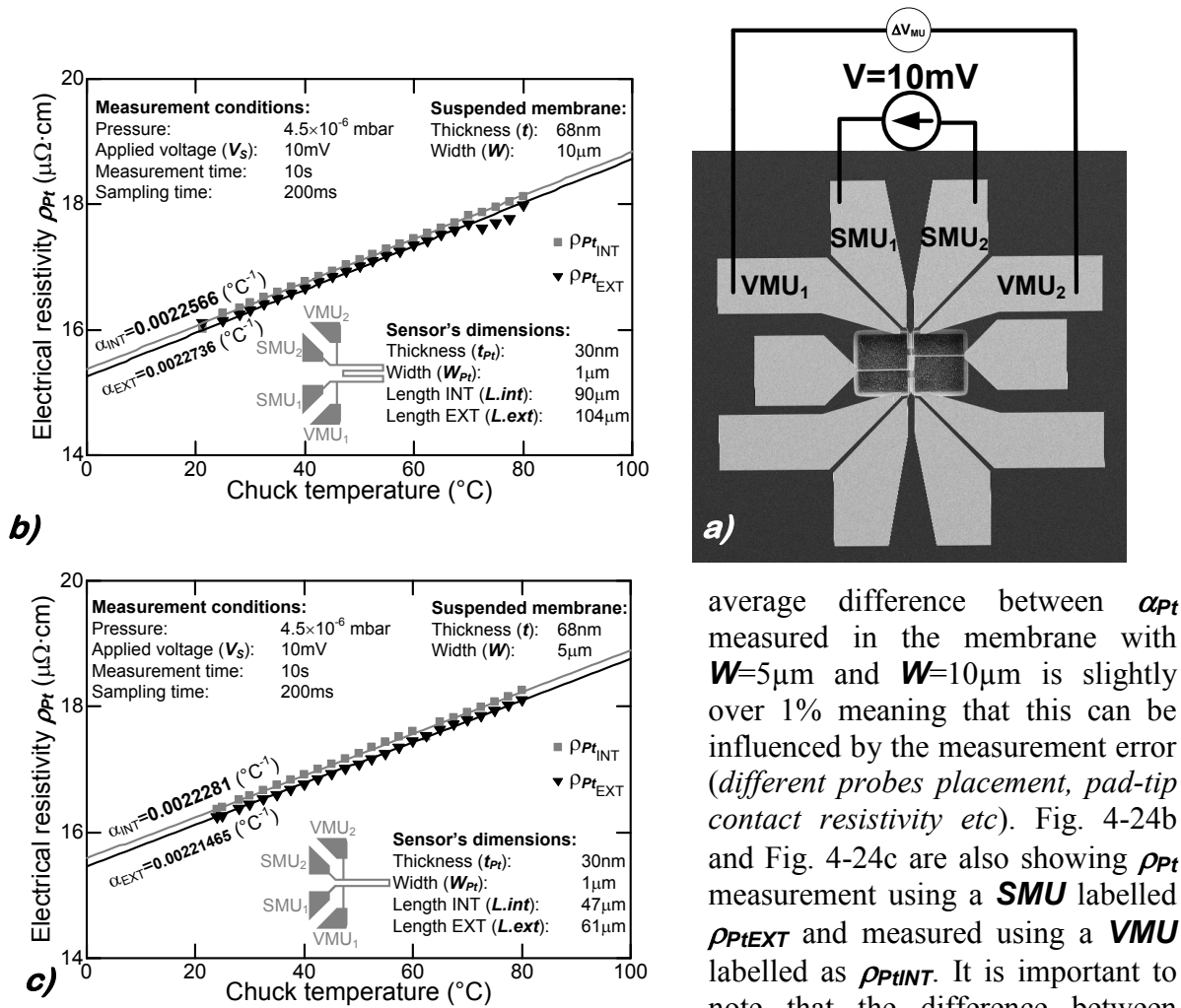
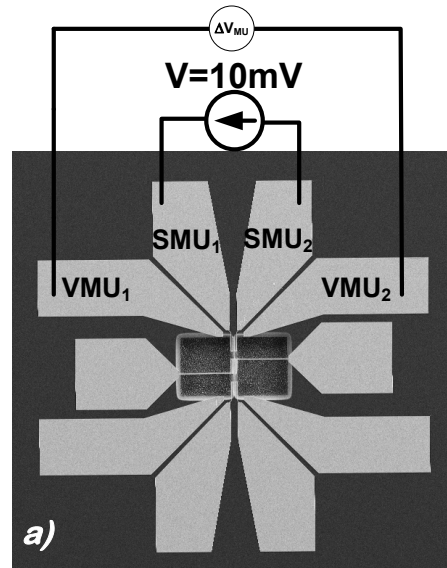


Fig. 4-24 Thermally induced  $\rho_{Pt}$  shift measured in the sensors, a) wiring diagram emphasizing the channels placement on the device, b)  $\rho_{Pt}$  versus chuck temperature measured in the sensor in the suspended membrane with  $W=10\mu\text{m}$ , c)  $\rho_{Pt}$  versus chuck temperature measured in the sensor in the suspended membrane with  $W=10\mu\text{m}$

the average  $\alpha_{INT}$  is calculated based on the measurements acquired for  $W=5\mu\text{m}$  Fig. 4-24c and  $W=10\mu\text{m}$  Fig. 4-24b. Finally,  $\alpha_{Pt}=0.002242^{\circ}\text{C}^{-1}$  is used to determine the  $T_H$ .

The characteristics depicted in Fig. 4-24b and Fig. 4-24c are also used to determine  $T_S$  for evaluating  $\kappa$ . Based on Fig. 4-24b or Fig. 4-24c it is possible to identify  $T_S$  by measuring  $\rho_{Pt}$ . Thus, the results presented on the Fig. 4-24b and Fig. 4-24c can be considered as the sensor calibration.



average difference between  $\alpha_{Pt}$  measured in the membrane with  $W=5\mu\text{m}$  and  $W=10\mu\text{m}$  is slightly over 1% meaning that this can be influenced by the measurement error (*different probes placement, pad-tip contact resistivity etc*). Fig. 4-24b and Fig. 4-24c are also showing  $\rho_{Pt}$  measurement using a **SMU** labelled  $\rho_{PtEXT}$  and measured using a **VMU** labelled as  $\rho_{PtINT}$ . It is important to note that the difference between  $\rho_{PtEXT}$  and  $\rho_{PtINT}$  is very small. However, knowing that **VMU** has 10-times higher accuracy than **SMU**,  $\alpha_{Pt}$  is calculated based on measurements acquired by the **VMU**. In the further calibration step

Table 4-21 Measurement specification for characterizing the temperature impact on the platinum electrical resistivity

<i>Criteria</i>	<i>Unit</i>	<i>Value</i>		
Sensor dimensions	$\mu\text{m}$	Width ( $W_{Pt}$ )	1	
		Length	47 ( <i>L.int</i> )	(W=5 $\mu\text{m}$ )
			67 ( <i>L.ext</i> )	
			90 ( <i>L.int</i> )	(W=10 $\mu\text{m}$ )
			104 ( <i>L.ext</i> )	
Thickness ( $t_{Pt}$ )	$30 \times 10^{-3}$			
Membrane's width ( $W$ )	$\mu\text{m}$	5		
		10		
Chuck temperatures ( $T_{CHUCK}$ )	$^{\circ}\text{C}$	ambient; 25 $\rightarrow$ 80 step $5^{\circ}\text{C}$		
Measurement probes configuration		Four-point probe resistivity measurement		
Used measurement channels		Two <b>SMU</b> channels as voltage source and current meter, and two <b>VMU</b> channels for voltage drop measurement		
Voltage value ( $V_S$ )	V	$10 \times 10^{-3}$		
Measurement mode		SAMPLING		
Integration mode		MEDIUM		
Sampling time	s	$200 \times 10^{-3}$		
Final time	s	10		
Minimal measurement accuracy*		<b>VMU</b>	$\pm 0.2 \mu\text{V}$	
		<b>SMU</b>	$\pm 1 \text{nA}$ for current $\pm 2 \mu\text{V}$ for voltage	

\*Data based on the HP4155C user's manual

#### 4.4.3.2 Heater calibration

The heater calibration differs significantly from the previously described measurement. When calibrating the heater,  $T_{CHUCK}$  is maintained constant while the voltage applied to the heater ( $V_H$ ) is swept. For each  $V_H$  value, the  $Pt$  electrical resistivity ( $\rho_{Pt}$ ) is measured. In contrast with previous measurements, the applied  $V_H$  is here high enough to cause a thermally induced  $\rho_{Pt}$  change due to Joule heating.  $\rho_{Pt}$  is measured as previously with a four-point probe configuration. The wiring diagram is shown in Fig. 4-25a. After the system reaches the thermal steady-state,  $\rho_{Pt}$  is measured for a given  $V_H$ . Thus each  $V_H$  is maintained for 10 seconds to stabilize the thermal conditions and after the hold time ( $t_{hold}$ ),  $\rho_{Pt}$  is measured. The applied heater voltage is depicted in Fig. 4-25b. It is important to note that in this case, the heater is connected to only two measurement pads which makes necessary to place **SMU** and **VMU** probes on the same contacts. Thus, the measurement should give theoretically the same  $\rho_{Pt}$  measured by **VMU** and **SMU**. In other words the adoption of a four-point probe measurement in this case is identical to a two-

point probes measurement. However, the **VMU** unit keeps its accuracy advantage over the **SMU**. The detailed configuration of the measurement setup is listed in Table 4-22.

**Table 4-22 Measurement specification for characterizing the Joule heating impact on the platinum electrical resistivity**

<i>Criteria</i>	<i>Unit</i>	<i>Value</i>
<b>Heater dimensions</b>	$\mu\text{m}$	<b>Width (<math>W_{Pt}</math>)</b>
		<b>Length</b>
		<b>Thickness (<math>t_{Pt}</math>)</b>
		<b>Membrane's width (<math>W</math>)</b>
<b>Chuck temperature (<math>T_{CHUCK}</math>)</b>	$^{\circ}\text{C}$	
<b>Measurement probes configuration</b>		
<b>Used measurement channels</b>		
<b>Measurement mode</b>		
<b>Integration mode</b>		
<b><math>V_H</math> initial value</b>	<b>V</b>	
<b>Step</b>	<b>V</b>	
<b>Final value</b>	<b>V</b>	
<b>Hold time</b>	<b>s</b>	
<b>Minimal measurement accuracy *</b>		

\*Data based on the HP4155C user's manual

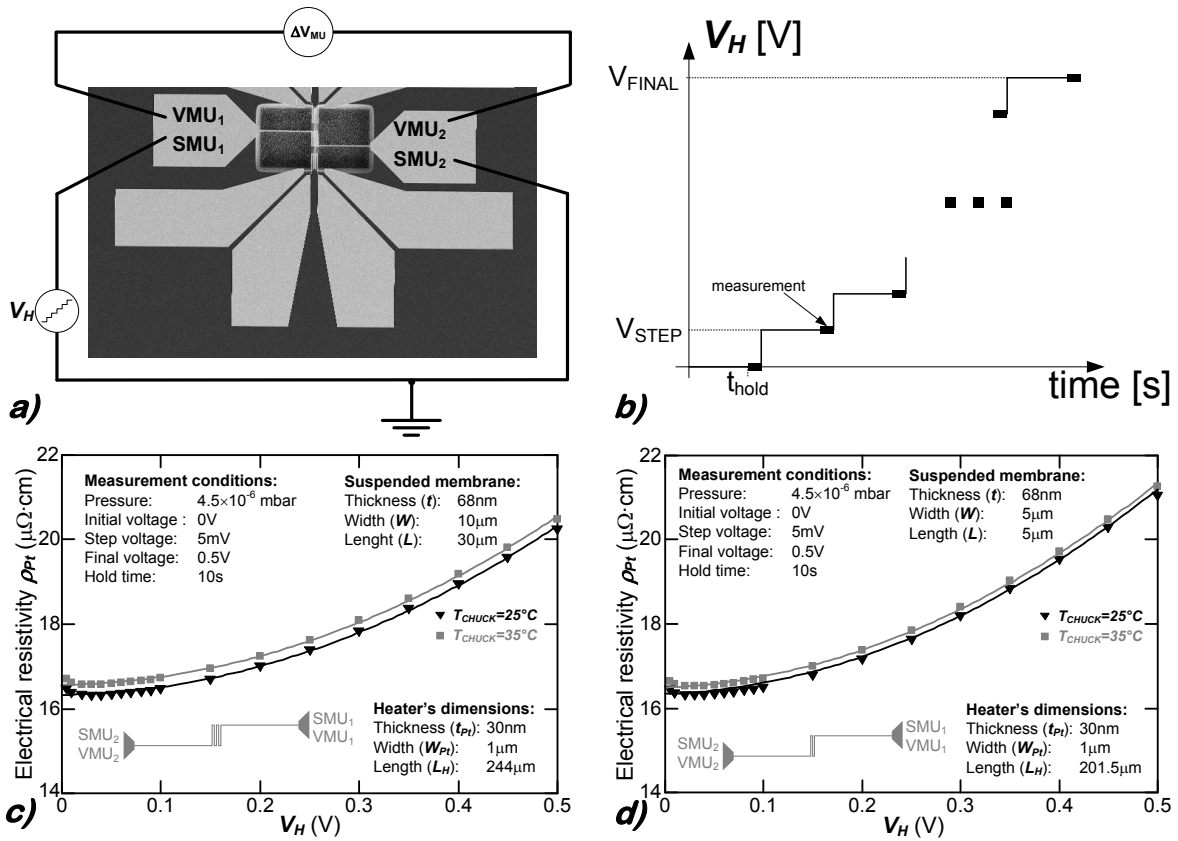


Fig. 4-25 Characterization of impact of Joule heating on  $\rho_{Pt}$  for fixed  $T_{CHUCK}$ , a) wiring schema emphasizing the measurement channels placement on the characterized device, b) Sketch of the voltage applied to heater  $V_H$  c) The electrical resistivity  $\rho_{Pt}$  versus  $V_H$  for two chuck temperatures and membrane width  $W=10\mu\text{m}$  and length  $L=30\mu\text{m}$ , d) The  $\rho_{Pt}$  versus  $V_H$  for two chuck temperatures and membrane width  $W=5\mu\text{m}$  and length  $L=5\mu\text{m}$

$\rho_{Pt}$  measurements versus  $V_H$  for  $T_{CHUCK}=25$  and  $35^\circ\text{C}$  are depicted in Fig. 4-25c for the membrane with  $W=10\mu\text{m}$  and  $L=30\mu\text{m}$  (the widest and the longest membrane in the cell) and in Fig. 4-25d for the membrane with  $W=5\mu\text{m}$  and  $L=5\mu\text{m}$  (the narrowest and the shortest membrane in the cell). At first glance, it is visible that  $\rho_{Pt}$  follows a parabolic dependency with  $V_H$ . The explanation for such behaviour is the Joule power released in the heater resistance. The relationship coupling the electrical power, voltage and resistance has the following form [Schultz, 2011]:

$$P = \frac{V^2}{R} \Rightarrow P_H = \frac{V_H^2}{\rho_{Pt} \cdot \frac{L_H}{W_{Pt} \cdot t_{Pt}}} \quad \text{Eq. 4-6}$$

where:

$P$	Electrical power (W)
$V$	Applied voltage (V)
$R$	Electrical resistance ( $\Omega$ )
$\rho_{Pt}$	Electrical resistivity ( $\Omega\cdot\text{cm}$ )
$V_H$	Voltage applied to heater (V)
$L_H$	Heating serpentine length (m) (for $W=10\mu\text{m}$ $L_H=244\mu\text{m}$ ; for $W=5\mu\text{m}$ $L_H=201.5\mu\text{m}$ )
$W_{Pt}$	Heating serpentine width (m) ( $W_H=1\mu\text{m}$ )
$t_{Pt}$	Heating serpentine thickness (m) ( $t_H=30\text{nm}$ )

Eq. 4-6 presents the well known relationship that describes the dissipated power in the resistor when **DC** voltage is used. From the analysis of Eq. 4-6, it can be remarked that the power (**P**) released as heat in the resistor (**R**) depends on the square of the applied voltage (**V**). This means that a slight change of **V** causes a bigger change in **P**, causing a temperature rise in the resistor. Finally, the temperature change also leads to a variation of the resistance value. Referring to the serpentine, the dissipation of a higher power **P<sub>H</sub>** in the heater causes a more pronounced thermally induced change in  $\rho_{Pt}$ . Comparing Fig. 4-25c and Fig. 4-25d it can be remarked that the  $\rho_{Pt}$  variations with **V<sub>H</sub>** are smaller for **W**=10 $\mu$ m and **L**=30 $\mu$ m membrane than for its **W**=**L**=5 $\mu$ m counterpart. This is caused by the fact that for the same **V<sub>H</sub>**, the dissipated power in the heater placed on the narrowest membrane **W**=5 $\mu$ m is higher because the heater is shorter (**L<sub>H</sub>**=201.5 $\mu$ m) compared with **W**=10 $\mu$ m (**L<sub>H</sub>**=244 $\mu$ m).

From the inspection of Fig. 4-25c or Fig. 4-25d, a repetitive trend can be noticed. When the reference temperature of the chuck is higher the measured  $\rho_{Pt}$  exhibits a higher value. Thus  $\rho_{Pt}(V_H)$  for **T<sub>H</sub>**=35 $^{\circ}$ C lies above its counterpart at **T<sub>H</sub>**=25 $^{\circ}$ C. This behaviour was already observed in the Fig. 4-24b and Fig. 4-24c. **Pt** exhibits a positive  $\alpha_{Pt}$  meaning that the resistivity rises with rising temperature. When **V<sub>H</sub>** is small the initial value of  $\rho_{Pt}$  depends mostly on **T<sub>CHUCK</sub>**, while **V<sub>H</sub>** raises the Joule heating occurs causing parabolic character of the  $\rho_{Pt}(V_H)$  characteristics. Worth noting is the fact that in membrane with **W**=5 $\mu$ m the  $\rho_{Pt}$  exhibits higher change with **V<sub>H</sub>** than in the membrane with **W**=10 $\mu$ m. This means that Joule effect is more pronounced in the membrane with **W**=5 $\mu$ m because of shorter heater length **L<sub>H</sub>**=201.5 $\mu$ m.

Evaluation of Joule effect in the heater serpentine terminates the device calibration. However, based on the above presented measurements determination of **T<sub>H</sub>** as a function of **V<sub>H</sub>** is possible and will be explained in the following section.

#### 4.4.3.3 Determination of the heater temperature **T<sub>H</sub>** for a given heater voltage **V<sub>H</sub>**

Knowing that the **Pt** electrical resistivity exhibits a linear dependence with temperature Fig. 4-24c, Eq. 4-7 can be used to determine  $\rho_{Pt}$  at temperature **T**≠**T<sub>0</sub>** (**T<sub>0</sub>** being considered as the reference temperature)[Serway, 1998]. Transforming Eq. 4-7 to calculate the temperature for an applied voltage **V**≠**V<sub>0</sub>** (**V<sub>0</sub>** being considered as reference voltage), Eq. 4-8 is obtained. Both Eq. 4-7 and Eq. 4-8 are based on the assumption that the temperature induces a linear change in resistivity, which is the case for **Pt**. Hence, the reference temperature is **T<sub>CHUCK</sub>**. Thus rewriting Eq. 4-8 using annotations which corresponds to this topology Eq. 4-9 is obtained.

$$\rho_{Pt}(T) = \rho_{Pt}(T_0) \cdot [1 + \alpha_{Pt} \cdot (T - T_0)] \quad \text{Eq. 4-7}$$

$$T(V) = T_0 + \frac{\left( \frac{\rho_{Pt}(V)}{\rho_{Pt}(V_0)} - 1 \right)}{\alpha_{Pt}} \quad \text{Eq. 4-8}$$

$$T_H(V_H) = T_{CHUCK} + \frac{\left( \frac{\rho_{Pt}(V_H)}{\rho_{Pt}(V_H=0)} - 1 \right)}{\alpha_{Pt}} \quad \text{Eq. 4-9}$$

Based on the previous characterizations  $\alpha_{Pt}=0.002242^{\circ}\text{C}^{-1}$  (see Fig. 4-24c and Fig. 4-24d) and  $\rho_{Pt}(V_H)$  (see Fig. 4-25c) and Fig. 4-25d) are used in Eq. 4-9. Heater temperature ( $T_H$ ) versus heater voltage ( $V_H$ ), following Eq. 4-9, is depicted in Fig. 4-26.

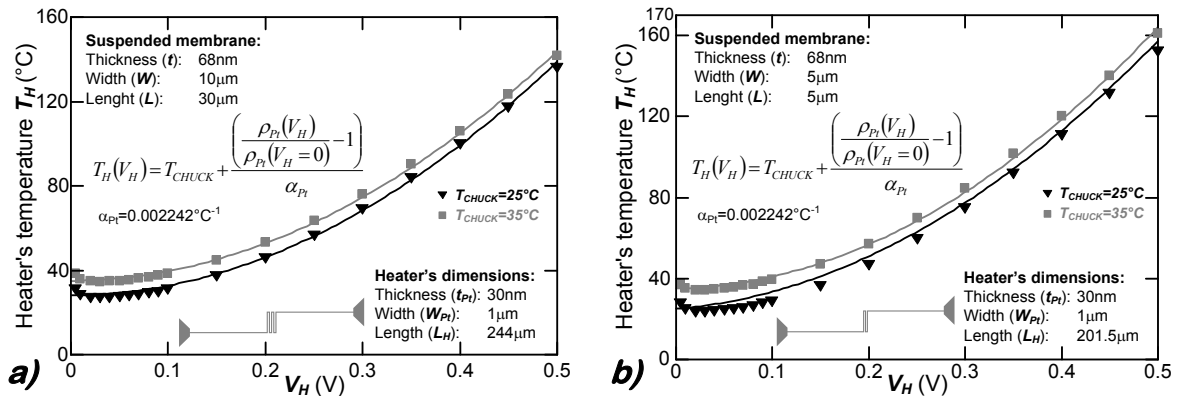


Fig. 4-26 Heater temperature ( $T_H$ ) versus heater voltage ( $V_H$ ) a) a membrane with  $W=10\mu\text{m}$  and  $L=30\mu\text{m}$ , b) a membrane with  $W=5\mu\text{m}$  and  $L=5\mu\text{m}$

Comparing the characteristics depicted in Fig. 4-26, it is worth noting that  $T_H$  reaches very high values for  $V_H=0.5\text{V}$ . For  $W=5\mu\text{m}$ ,  $T_H=160^{\circ}\text{C}$  Fig. 4-26b ( $\sim 135^{\circ}\text{C}$  above  $T_{CHUCK}$ ) and for  $W=10\mu\text{m}$   $T_H=140^{\circ}\text{C}$  as shown in Fig. 4-26a ( $\sim 115^{\circ}\text{C}$  above  $T_{CHUCK}$ ). The  $T_H$  rise is more pronounced for the membrane with  $W=5\mu\text{m}$ . It is because the higher electrical power released in the less resistive heater ( $L_H=201.5\mu\text{m}$  for  $W=5\mu\text{m}$ ) causes a higher  $T_H$  rise.

The characteristics graphically presented in Fig. 4-26 show the  $T_H(V_H)$  relationship. Using Fig. 4-24, it is possible to determine  $T_S$  based on the measured sensor electrical resistivity. Thus to perform the  $\kappa$  measurement the calibrations depicted in Fig. 4-24 and Fig. 4-26 are required. After calibrating the sensing and heating serpentes,  $\kappa$  measurement can be readily extracted. It is the scope of the following section.

#### 4.4.4 Thermal conductivity measurements

After performing the serpentine calibration to be able to determine  $T_S$  and  $T_H$ ,  $\kappa$  measurement can be performed. The  $\kappa$  characterization in thin-film **Si** membranes relies on the thermal coupling between the heater and the sensor. Hence, the focus will be put on the practical implementation of this measurement.

The  $\kappa$  measurement is performed in thermal steady state with  $T_{CHUCK}$  stabilized and controlled during data collection. The determination of  $\kappa$  consists in two previously described calibrations performed simultaneously on the same membrane. The  $\kappa$  measurement specifications are detailed in Table 4-23.

Table 4-23 Measurement specification for  $\kappa$  measurement in thin-film Si membrane

<i>Criteria</i>	<i>Unit</i>	<i>Value</i>	
Suspended membrane dimensions	$\mu\text{m}$	Width ( $W$ )	5 and 10
		Length ( $L$ )	5; 10; 20 and 30
		Thickness ( $t$ )	$68 \times 10^{-3}$
Platinum serpentine dimensions	$\mu\text{m}$	Width ( $W_{Pt}$ )	1
		Thickness ( $t_{Pt}$ )	$3 \times 10^{-2}$
Heater dimensions	$\mu\text{m}$	Length	201.5 ( $W=5\mu\text{m}$ )
			244 ( $W=10\mu\text{m}$ )
Sensor dimensions	$\mu\text{m}$	Length	47 ( $L.int$ )
			67 ( $L.ext$ )
			90 ( $L.int$ )
			104 ( $L.ext$ )
Chuck temperature ( $T_{CHUCK}$ )	$^{\circ}\text{C}$	25, 30 and 35	
Measurement probes configuration	Two probes on heater and two probes on sensor		
Used measurement channels	4x <b>SMU</b> channels as voltage sources and current meters		
Measurement mode	$V_H$ voltage SWEEP		
Integration mode	MEDIUM		
$V_H$ initial value	V	0	
Step	V	$5 \times 10^{-3}$	
Final value	V	0.5	
Hold time	s	10	
Sensor voltage	V	$10^{-2}$ constant during the measurement	
Minimal measurement accuracy*		<b>SMU</b>	$\pm 1\text{nA}$ for current $\pm 2\mu\text{V}$ for voltage

\*Data based on the HP4155C user's manual

The sensor resistivity is measured using a two-point probe configuration with a very small voltage applied to the sensor to avoid  $\rho_{Pt}$  change caused by Joule heating. Simultaneously,  $V_H$  is applied to the heating serpentine using two probes. The wiring diagram used for  $\kappa$  determination is depicted in Fig. 4-27a. The  $V_H$  shape is depicted in Fig. 4-25b. From Fig. 4-27a, it can be remarked that only **SMU** units are in use during this measurement. This is imposed by the limited number of available measurement probes and manipulators associated to the vacuum chamber (Fig. 4-23). The voltage has to be applied to the heater and to the sensor simultaneously which imposes the necessity to use the **SMU** units. For that reason the measurement accuracy is lowered because none of the **VMU** units can be used.



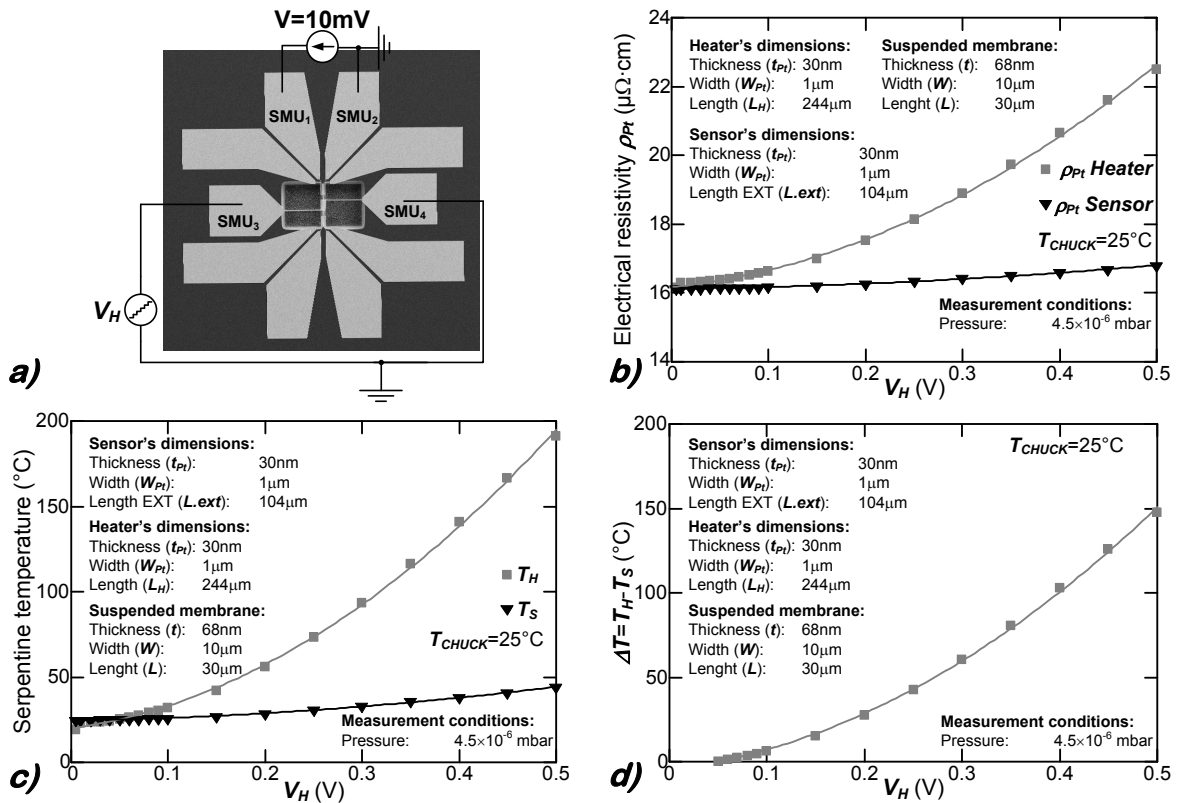


Fig. 4-27 Heater-sensor thermal coupling evaluation for a thin-film **Si** membrane with length  $L=30\mu\text{m}$  and width  $W=10\mu\text{m}$  Fig. 4-27a) wiring diagram used during the  $\kappa$  measurement, b) Heater and sensor electrical resistivity versus voltage applied to the heater for  $T_{CHUCK}=25^{\circ}\text{C}$ , c) Heater and sensor temperatures versus voltage applied to the heater for  $T_{CHUCK}=25^{\circ}\text{C}$ , d) Temperature drop along the membrane versus voltage applied to heater.

The proposed device ensures that thermal coupling between the heater and the sensor only takes place through the suspended **Si** membrane. The heater-sensor thermal coupling has been experimentally measured. The results are presented in Fig. 4-27b and Fig. 4-27c. When  $V_H$  applied to the heater rises, Joule heating occurs which can be observed by the rising of  $\rho_{Pt}$  Heater according a parabolic law (see Fig. 4-27b). The same trend, but less pronounced, is observed on the sensor site. Fig. 4-27b proves that there is a thermal coupling between the heater and the sensor, because the constant voltage applied to the sensor during the measurements is too small ( $10\text{mV}$ ) to induce a resistivity change in the sensor. Fig. 4-27b shows that sensor resistivity exhibits a parabolic variation as well as  $\rho_{Pt}$  Heater this means that the heater thermally influences the sensor. Another interesting point to note is the fact that for a very low  $V_H$ , the heater and sensor electrical resistivity are almost identical. Such an observation confirms that when the Joule heating is negligibly small the sensor and heater are placed in identical thermal conditions. In other words  $T_H=T_S$  for very low  $V_H$  values. Fig. 4-27c presents the sensor and heater temperature versus voltage applied to heater  $V_H$ . Analyzing Fig. 4-27c it can be observed that  $T_H$  is much higher than  $T_S$ . Secondly, the rise of  $T_H$  leads to a  $T_S$  increase. Fig. 4-27c puts more light on the heater-sensor thermal coupling. It is visible that for a rising  $V_H$  the temperature  $T_H$  rises as well due to the Joule effect. However, the rise of  $T_S$  is less pronounced. Fig. 4-27d presents the temperature drop along the characterized membrane as a function of  $V_H$ . It is worth noting that  $\Delta T$  rises to  $\sim 150^{\circ}\text{C}$  when  $V_H=0.5\text{V}$ .  $\Delta T$  between the heater and the sensor it therefore very huge for a distanced of only  $30\mu\text{m}$ . Moreover,  $\Delta T$  starts to rise around  $V_H \approx 0.05\text{V}$  but is close to zero for lower  $V_H$ . This observation gives some information about the sensitivity of the sensor. When the heat power injected in the

membrane is small (*low*  $V_H$ ) the  $\rho_{Pt}$  **Sensor** change is not significant enough to be measured with the adopted measurement strategy. When  $V_H$  increases above the threshold value, the released heat power causes measurable  $\rho_{Pt}$  **Sensor** change. Based on data reported in Fig. 4-27c, knowing the exact electrical power released by the heater ( $P_H$ ) and referring to the characterized **Si** membrane dimensions: length ( $L$ ), width ( $W$ ) and thickness ( $t$ ),  $\kappa$  can be calculated using Eq. 4-5. Fig. 4-28 presents  $\kappa$  of a  $t=68\text{nm}$  thick **Si** membrane with the largest ( $W=10\mu\text{m}$  and  $L=30\mu\text{m}$ ) and the smallest ( $W=5\mu\text{m}$  and  $L=5\mu\text{m}$ ) area.  $L$  indicates the quality of the thermal coupling between the heater and the sensor. For small  $L$ , the heater-sensor thermal connection is the strongest. Neglecting possible 3D edge effects  $\kappa$  should be the same regardless  $W$  and  $L$  of the characterized membrane.

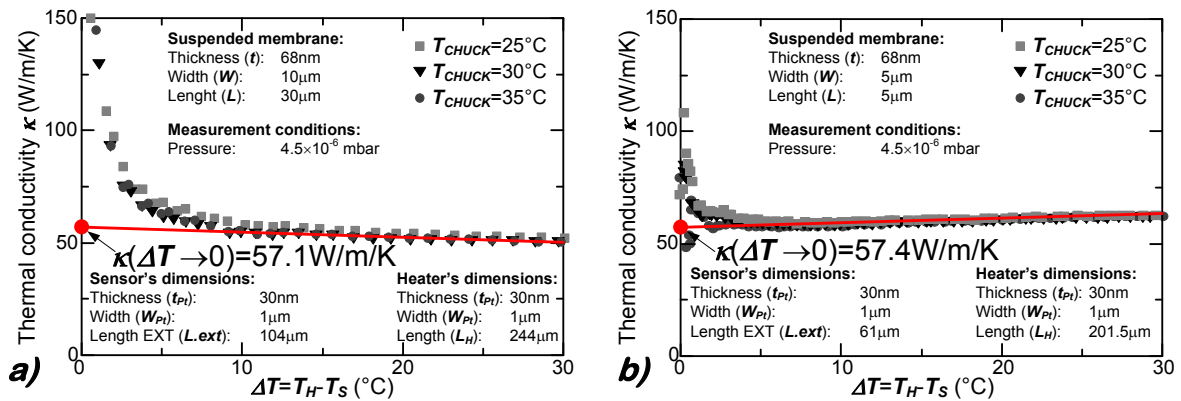


Fig. 4-28 Thermal conductivity versus temperature drop along  $t=68\text{nm}$  thick **Si** membrane a) Length  $L=30\mu\text{m}$ , Width  $W=10\mu\text{m}$ , b) Length  $L=5\mu\text{m}$ , Width  $W=5\mu\text{m}$  [Haras, 2014-a]

Before analyzing Fig. 4-28 some theoretical background be highlighted (*extended explanation is in the section 4.1.1*). Analyzing the heat diffusion law (*Fourier's law*) for thermal steady state in Eq. 4-2, it can be noted that it presents  $\kappa$  as a parameter describing the heat transport quality. Practical determination of  $\kappa$  requires assumptions enabling the simplification of Eq. 4-2. Firstly, instead of analyzing the heat propagation in all directions ( $x$ ,  $y$  and  $z$ ), the device is designed in such a way to favour heat transport along only one axis. Secondly, the **SOI** suspension and measurement in vacuum enables the linearization of Eq. 4-2. For small heater-sensor temperature differences ( $\Delta T$ ) further simplification of Eq. 4-2 can be achieved by replacing ( $\nabla T$ ) by ( $\Delta T/L$ ) where  $L$  is the distance between heater and sensor. The temperature gradient linearization is justified when  $\Delta T \rightarrow 0$  under this condition  $\kappa$  should be determined for as low as possible  $\Delta T$  along the membrane.

Fig. 4-28 plots the measured  $\kappa$  against the  $\Delta T$  along the membrane. To accurately determine  $\kappa$  the linear extrapolation at  $\Delta T \rightarrow 0$  is plotted indicating the value of  $\kappa(\Delta T=0)$ . Inspecting data depicted in Fig. 4-28 it can be remarked that for small  $\Delta T$  across the membrane the measurement gives a diverging  $\kappa$  value. This is caused by the limited sensor sensitivity which is further amplified by the first-order derivative approximation  $\Delta T/L$ . When  $\Delta T$  is small, the released heat power is too small to cause a measurable sensor electrical resistivity change. When  $\Delta T$  becomes higher,  $\kappa$  stabilize and enables  $\kappa$  determination by linear extrapolation at  $\Delta T \rightarrow 0$ . When the distance between the heater and the sensor is small (*Fig. 4-28b*), the zone where the sensor lacks of sensitivity decays faster than for long membranes (*Fig. 4-28a*). This observation confirms that for the smaller  $L$  the thermal coupling between heater and sensor is stronger. As a consequence, a smaller  $P_H$  is needed to cause a measurable sensor resistivity change. However, the main conclusion arising from Fig. 4-28 is that  $\kappa$  values extracted for a membrane with  $L=30\mu\text{m}$  and

$W=10\mu\text{m}$  and for membrane with  $L=5\mu\text{m}$  and  $W=5\mu\text{m}$  closely match. This means that the  $\kappa$  measurement is not affected neither by the length ( $L$ ) nor by the width ( $W$ ) of the membrane. This results in somewhat expectable knowing that both  $L$  and  $W$  are much bigger than the phonon mean free path ( $L_{ph}\approx 300\text{nm}$  for **Si**) (see section 3.2.1.5.2 and Fig. 3-16). This means that the heat transport is only affected by the thickness of the suspended membrane ( $t$ ) and not perturbed by dominated edge effects. The obtained  $\kappa$  value for 68nm thick **Si** is almost 3-times smaller than its bulk counterpart ( $\kappa_{bulk}=148\text{W/m/K}$ ). The previously described size-induced **Si** thermal conductivity reduction (see section 3.2.1.5.2 and Fig. 3-17) is therefore experimentally confirmed.

The results presented in Fig. 4-28 are completing the characterization of the proposed device. In the following the accuracy evaluation of the measured  $\kappa$  and the identification of measurement errors will be discussed.

#### 4.4.4.1 Thermal conductivity measurement accuracy and quality

To evaluate the quality of the measured  $\kappa\approx 57\text{W/m/K}$  for a 68nm thick **Si**, Fig. 4-29 can be used (see also Fig. 3-17). In Fig. 4-29 the mean value of the measured  $\kappa$  extracted

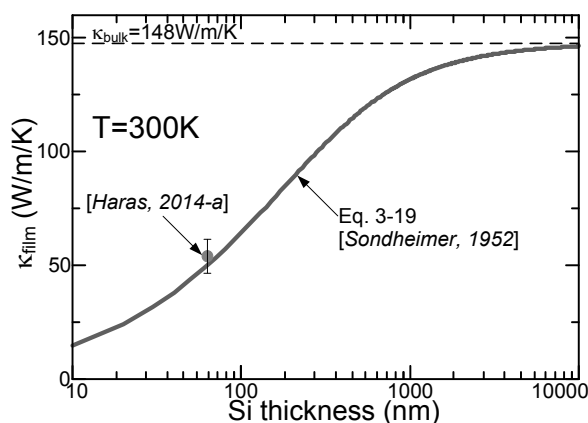


Fig. 4-29 Mean value of the measured  $\kappa$  in all membranes plotted against the **Si** thickness

from all suspended **Si** membranes is presented. To evaluate the accuracy of the measurement the theoretical law describing  $\kappa$  reduction for different thicknesses is plotted [Sondheimer, 1952]. It can be noted that the theoretical model of the  $\kappa$  reduction in **Si** is very close to the experimental data measured using this device. In Fig. 3-17 more experimental data are presented which are confirming the theoretical model. The good agreement of the measured data with theoretical model indicates that the influence of the measurement errors is not

dominant. However, despite the minor impact of measurement errors, the main error sources will be identified in the following.

The errors occurring during the measurement can be divided into three main groups:

- **Equipment** – this group is formed by the inaccuracy of the used measurement equipment (*measurement cables resistance, tip-pad contact resistance and the accuracy of the measurement device*). Those errors are very small and well determined. The most difficult parasitic parameters to estimate is the contact resistance between the measurement needle and the pad. This contact parasitic resistance is influencing the measurement only for  $\kappa$  measurements. When performing the heater or sensor calibrations the contact resistance is eliminated from the calibrations by using **VMU**.
- **Heat leakage** –thermally induced heat leakages associated to the device geometry and the architecture can cause thermal losses. Fig. 4-30a presents the top view of the measurement platform indicating the main thermal paths where heat leakage occurs without passing through the suspended membrane.

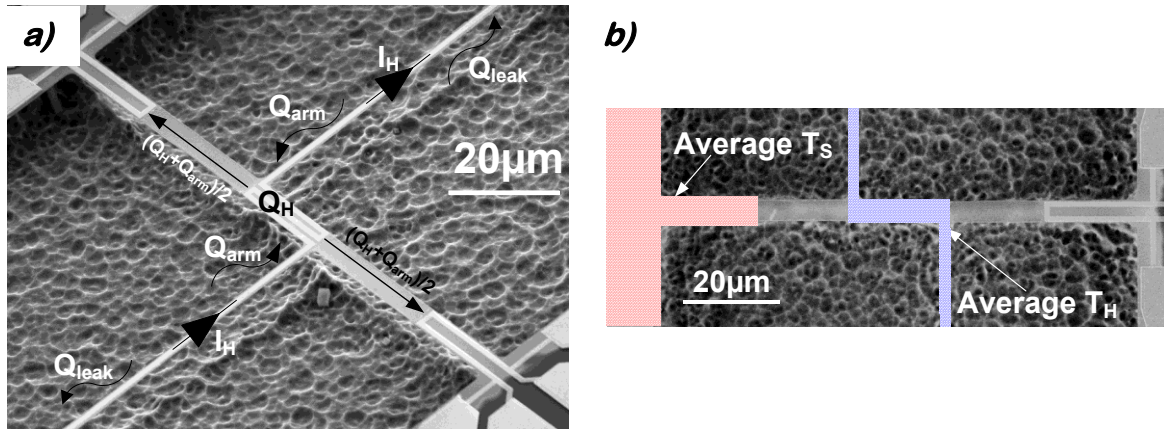


Fig. 4-30 a) Graphical identification of topologically induced heat leakages in the measurement platform, b) top view on the suspended membrane emphasizing the sensor and heater parts which are influencing the temperature determination

Analyzing Fig. 4-30a it can be remarked that the main heat leakage path is formed by the heater arms. This lost heat flux can flow towards the substrate instead of being transferred to the membrane. This is lowering the real heat power transferred to the suspended membrane by the fraction of power which escapes towards the **Si** substrate through the heater arms.

- **Method** – the electro-thermal method requires a vacuum chamber to give repetitive and accurate results. However, despite using the vacuum radiative losses are present. Moreover, the method assumes that the heater temperature  $T_H$  on the membrane is uniform which is not true. The heater has smaller temperature near the membrane borders while in the middle  $T_H$  is higher.  $T_H$  and  $T_S$  are estimated indirectly using electrical resistivity measurements which means that the average  $T_H$  and  $T_S$  are used in the  $\kappa$  determination. This problem is graphically presented in Fig. 4-30b. Thus  $T_H$  and  $T_S$  are not strictly the temperatures of the membrane on the heater and sensor borders, respectively.  $T_H$  and  $T_S$  can also be influenced by the temperature of the **Pt** paths and **Au** contacts. This observation leads to conclude that the real on-membrane value of  $T_H$  and  $T_S$  is higher than the extracted value based on the electrical resistivity measurement. Moreover, the heater and the sensor are affected by this phenomenon unequally. The sensor is much shorter than the heater. Large **Au** contacts are also located near the sensor meaning that their influence on  $T_S$  measurement is more important.

The exact calculation of the measurement errors (*especially methodological and topological*) is very difficult. Based on the good agreement of measurement data with the theoretical model, it can be concluded that the above-described errors are playing a minor role. However, more precise error investigation should be performed when measuring  $\kappa$  for the material with an ultra-low  $\kappa$  e.g. **Si<sub>x</sub>Ge<sub>1-x</sub>**. The natural reduction of  $\kappa$  in **Si<sub>x</sub>Ge<sub>1-x</sub>** coupled to size induced  $\kappa$  reduction when using a thin-film result in a very low  $\kappa$  ( $\sim 3W/m/K$  when assuming the same 3-fold reduction for the thickness of  $68nm$ ). In such a situation, all parasites and heat leakages can badly impact the measurement leading to a wrong  $\kappa$  value.

## 4.5 Summary and conclusions

This chapter has presented the practical part of this project which involves the design, the fabrication and the characterization of an integrated micrometer measurement platform dedicated to  $\kappa$  measurements in thin-film materials.

In the first part, a brief description of existing  $\kappa$  characterization methods has been provided. The measurement approach used in this project is based on an electro-thermal method. This method imposes certain requirements to the design and the layout to obtain accurate results. The  $\kappa$  measurement in thin film material can easily be affected by misleading due to the amplified influence of all parasitics in the structures with micro-nanometer dimensions. Firstly, to ensure a precise  $\kappa$  measurement, the material which is characterized has to be thermally insulated from the surrounding environment (*the wafer*). Secondly to obtain a uniform temperature on the characterized membrane, long heating elements should be employed. Finally, the designed device should provide the highest possible sensibility to determine  $\kappa$  at the lowest possible  $\Delta T$  along the characterized material. Taking into account the above described criteria, a topology of the  $\kappa$  measurement platform in thin-film materials has been proposed (*Fig. 4-3*). Different membrane dimensions have been realized enabling the averaging of the measured  $\kappa$  for different membrane lengths ( $L$ ) and widths ( $W$ ). After completing the design step, a complete processing route has been developed to lead to measurement devices.

The second part of this chapter has described how the integrated platform is realized from a technological perspective. All important technological processes and corresponding parameters have been detailed in this part. The detailed process flow has been described in section 4.3. The device was fabricated on a **SOI** wafer with a 68nm thick active layer and a 145nm thick **Box** layer. Suspending the **SOI** membrane from the **Si** substrate releases all residual mechanical stresses build up in the various layers that can be destructive for the device. The mechanical relaxation has been taken into consideration at the design and fabrication level by adopting two particular arrangements. Firstly, the design should be prepared in such a way to avoid concentration of the mechanical stress in one place. Thus all the corners in the device were rounded to avoid cracks formation (*see Fig. 4-19*). At the fabrication level, only materials with low residual stress were selected for deposition (low stress **Si<sub>x</sub>N<sub>y</sub>**) or growth (wet **SiO<sub>2</sub>**) on the wafer (*Table 4-6*). *Fig. 4-21* presents the completed measurement platform for  $\kappa$  measurements. The fabricated device ensures the thermal insulation of the characterized membrane from the substrate. The heating element is placed in the center of the membrane and is electrically supplied via long arms (*length of single arm is  $\sim 70\mu\text{m}$* ). This is estimated to provide uniform temperature distribution on the characterized membrane and increase the thermal resistance between the membrane and the surrounding wafer. After fabricating the device, the  $\kappa$  characterization has been performed.

Characterization of  $\kappa$  in a 68 nm thick **Si** layer is detailed in section 4.4. The chosen electro-thermal method requires the measurement in vacuum which significantly reduces the convection losses and improves the accuracy. The idea of this measurement method is described in the section 4.4.1. The adopted  $\kappa$  measurement method uses electrical resistivity as an indicator of temperature. The heating and sensing serpentes are fabricated in **Pt** which exhibits linear dependence of the electrical resistivity with temperature (*Fig. 4-24c*). The heating power is delivered to the membrane through the

Joule effect occurring in the heating serpentine. The performance of the heater is evaluated before performing  $\kappa$  measurement (Fig. 4-25). For that reason, both the heater and sensor have been accurately calibrated. Using heater-sensor thermal coupling through the suspended **Si** membrane, the power released in the heater essentially flows towards sensors through the membrane.  $\kappa$  (see Eq. 4-5) of the membrane basically depends on the injected heat power, the temperature difference between the heater and the sensor and on the membrane dimensions. The measured  $\kappa$  for the membrane with the smallest and the largest width (**W**) and length (**L**) is presented in Fig. 4-28. It can be remarked that the measured  $\kappa$  is reproducible for different chuck temperatures and is independent of **W** and **L**. For low values of the temperature drop along the membrane, the measurement gives scattered  $\kappa$  values, which is caused by the limited sensor sensibility. When the temperature drop rises, the injected heat power is high enough to cause a measurable resistivity change of the sensor. The extrapolation to the measurement gives the  $\kappa$  value for  $\Delta T \rightarrow 0$ . The measured  $\kappa$  for 68nm thick **Si** follows with good precision the theoretical model Fig. 4-29. Accuracy of the model was confirmed by numerous experimental data as shown in Fig. 3-17.

To conclude this chapter, the main bullet points can be highlighted:

- The complete device creation chain involving the concept, design, fabrication and characterization has been realized
- The  $\kappa$  electro-thermal measurement method has been selected and the device architecture compatible with the method requirements has been designed
- Fabricating this device requires deposition and thermal growth techniques, dry and wet etching and metallization as well as high accuracy lithography
- Suspending the **Si** from the substrate releases the residual mechanical stress which has to be taken into consideration when designing the device
- The electro-thermal method requires the temperature drop along the membrane which is provided by measuring the electrical resistivity of the **Pt** serpentes
- Thermal conductivity measurement of 68nm thick **Si** is  $\sim 57\text{W/m/K}$  which is 3-fold reduction compared with bulk  $\kappa$  in **Si**
- The extracted value of  $\kappa$  in thin-film **Si** is independent of the membrane dimension (*apart thickness*) and follows the theoretical model with good agreement

# Conclusions

The work reported in this manuscript can be divided into a theoretical part where the performance evaluation of **CMOS** compatible materials, namely **Silicon (Si)**, **Germanium (Ge)** and **Silicon-Germanium (Si<sub>x</sub>Ge<sub>1-x</sub>)**, was presented and in a technological part where the design, fabrication and characterization of the device dedicated to thermal conductivity ( $\kappa$ ) measurements thin-films materials was reported. To synthesize this manuscript the most important conclusions and observations are highlighted hence in after:

1. The accurate temperature-, composition- and doping-dependent modelling enabled the optimisation on the material and topological level:
  - a. Optimal doping concentrations were determined by the analysis of the **Power Factor (PF)**:  $10^{18}\text{cm}^{-3}$  for **Ge** and  $10^{19}\text{cm}^{-3}$  for **Si** and **Si<sub>x</sub>Ge<sub>1-x</sub>**,
  - b. The comparative studies of different **ThermoElectric Generator (TEG)** topologies led to the conclusion that the electric harvesting capabilities are dominated by the electrical conductivity  $\sigma$ . The device with shorted *pn* junction is largely outperforming the **TEGs** with the *pn* junction,
  - c. A lateral topology of **TEG** was proposed. The topology enables (i) the use of thin-film active material that reduces  $\kappa$ , (ii) the integration of mechanical flexibility, (iii) topological adaptation for fabrication in digital industry (*planar geometry*) and (iv) facilitates mounting
  - d. Maximal harvested power density at  $\Delta T=30\text{K}$  and optimal doping concentration is  $12\text{W}/\text{cm}^2$  for **Ge**-,  $7\text{W}/\text{cm}^2$  for **Si**- and  $4\text{W}/\text{cm}^2$  for **Si<sub>x</sub>Ge<sub>1-x</sub>**-based lateral thermoelectric generator. Putting **CMOS** materials in competitive position with their conventional counterparts.
2. The design, fabrication and characterization of a micrometer measurement platform for  $\kappa$  characterization constitutes the technological outcome of this work:
  - a. The electro-thermal  $\kappa$  characterization method requirements are fulfilled at the design and metrology levels and led to a simple approach and accurate measurements,
  - b. The fabrication is realized using **SOI** wafer. The thin-film **Si** is released through the use of (i) low pressure etching techniques, (ii) low residual stress stack materials and (iii) layout design to spread the mechanical relaxation to avoid structure damage,
  - c. Measurements in vacuum determined  $\kappa=57\pm 7.5\text{W}/\text{m}/\text{K}$  in a 68nm thick **Si** membrane. This result is in agreement with the theoretical model and the size induced  $\kappa$  reduction is experimentally confirmed,
3. Good electrical properties and possibility of  $\kappa$  reduction in **CMOS** materials creates a new branch of industrially compatible, harmless, costly attractive and simple thermoelectrics. Recovering heat losses formed in electron devices may be realized through **CMOS** compatible thermoelectrics as very attractive, innovative and convenient energy harvesting method.

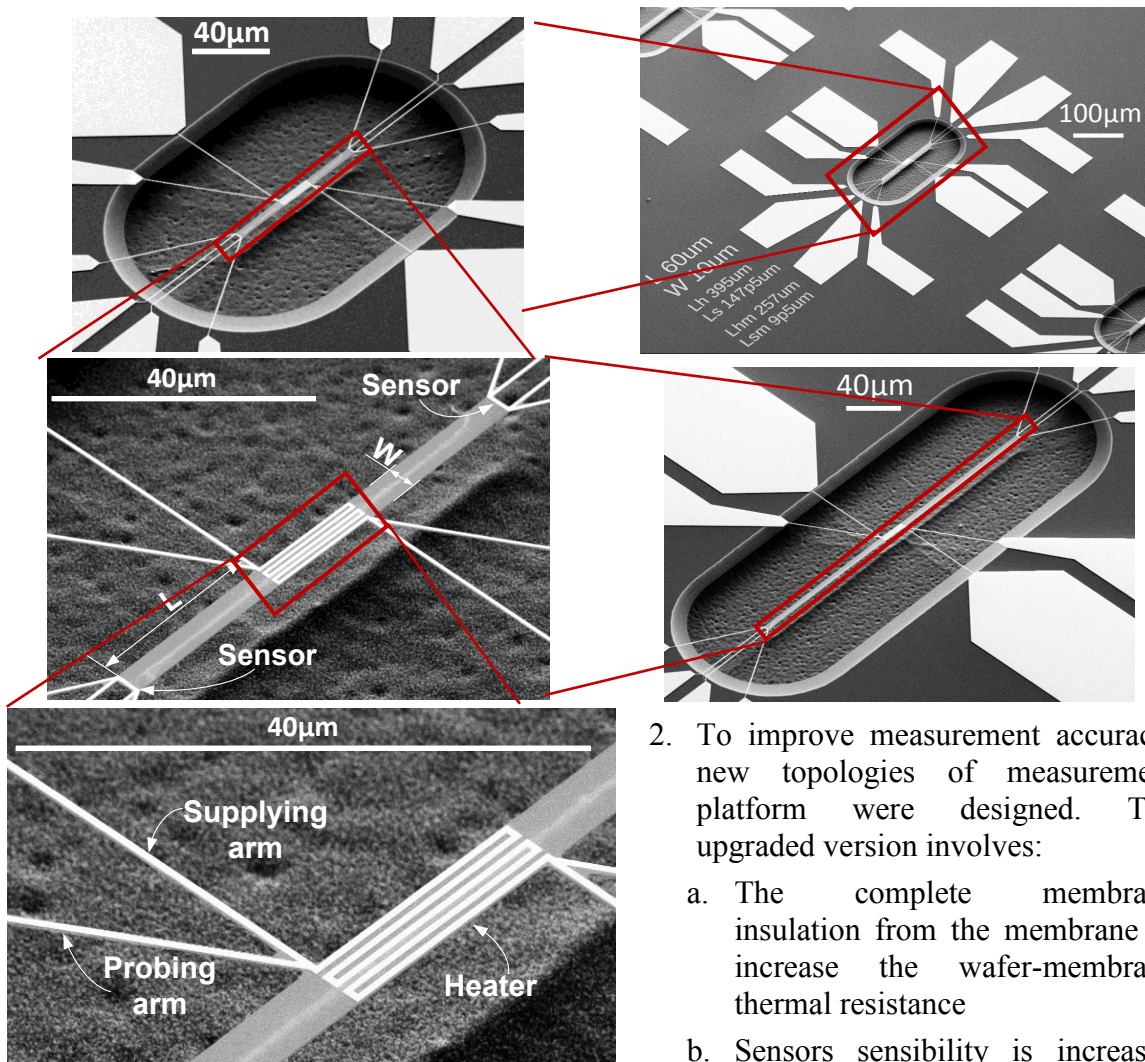




# Perspectives

## Short Term:

1. Established design, fabrication and measurement procedures open possibility to characterize  $\kappa$  for:
  - a. different **Si** thicknesses demonstrating additional  $\kappa$  reduction in ultra-thin **Si** layers
  - b. thin-film **Si<sub>x</sub>Ge<sub>1-x</sub>** determining if the natural reduction of  $\kappa$  can be accumulated with the size induced  $\kappa$  reduction
  - c.  $\kappa$  measurements for different **Si<sub>x</sub>Ge<sub>1-x</sub>** thicknesses would contribute to establish the theoretical model linking  $\kappa$  with **Si<sub>x</sub>Ge<sub>1-x</sub>** thickness

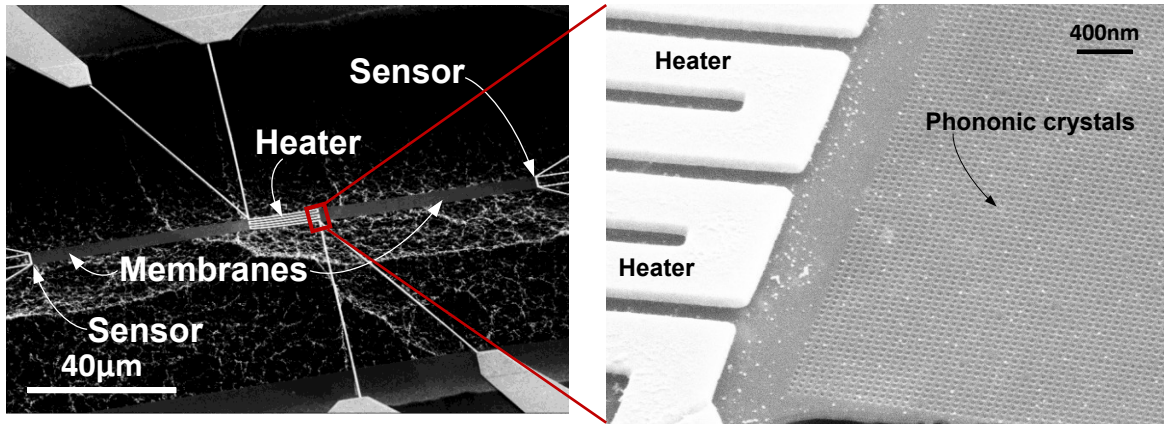


2. To improve measurement accuracy, new topologies of measurement platform were designed. The upgraded version involves:
  - a. The complete membrane insulation from the membrane to increase the wafer-membrane thermal resistance
  - b. Sensors sensibility is increased

thanks to the complete membrane suspension enabling  $\kappa$  determination at lower heater-sensor temperature drop which is more precise

- c. Four-point probe  $\rho_{PH}$  measurement possible on the heating serpentine allowing precise determination of the  $T_H$  temperature
- d. Significantly enlarged cavities are additionally increasing the thermal resistance between the membrane and the wafer

3. Elimination of 12nm thick wet **SiO<sub>2</sub>** grown on top of **SOI** will increase the accuracy of  $\kappa$  measurements by improving thermal transport between the heater and the membrane
4. Measurement of  $\kappa$  in the membranes with integrated phononic crystals and experimental demonstration of further  $\kappa$  reduction in membranes with integrated phononic crystals



5. Experimental evaluation of harvesting capabilities of **CMOS** compatible materials may be realized using the fabricated architecture for  $\kappa$  measurements

#### Medium to Long Term:

1. Fabrication of industrially compatible **TEG** based on **Si**, or **Si<sub>x</sub>Ge<sub>1-x</sub>** as active material
2. Evaluation of harvested power from monolithically integrated **TEG** when used with commercially available micro-controller, micro-processor or power transistor
3. Evaluation of cooling capabilities (*Peltier effect*) of **TEG** monolithically integrated with **CMOS** devices

## Chapter 5: L'Énergie dans le monde

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La consommation d'énergie en croissance continue, l'épuisement des réserves naturelles en minéraux fossiles, le développement technologique en galop et l'augmentation de l'effet de serre sont les défis qui poussent l'humanité à trouver des sources d'énergie innovatrices. L'indépendance énergétique de minéraux fossiles peut être augmentée par l'utilisation d'avantage les sources d'énergie renouvelables et par la conversion d'énergie perdue en énergie utile. La capacité mondiale en énergie renouvelable est très faiblement utilisée, la même conclusion peut être faite concernant la récupération d'énergie de perte. Cette situation donne la possibilité d'agir à l'échelle macro et micro pour rendre l'énergétique mondiale plus diverse, « verte », stable et rentable. Le concept de la production d'énergie à partir des pertes ouvre également la possibilité d'utiliser complètement de nouvelles sources d'énergie (*courant d'air, les vibrations ou le corps humain*). La transition d'énergie conventionnelle polluante et fossile à l'énergie « verte » et renouvelable est nécessaire du point de vue écologique, économique et sociétal, les pertes d'énergie pouvant jouer le rôle principal rendant alors cette transition possible.

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## 5.1 Introduction

L'énergie en général est un moyen qui assure le développement continu économique, technologique et social. Nous sommes incapables de construire sans une certaine portion d'énergie initiale. La croissance de la population mondiale et le développement industriel fait augmenter la consommation de l'énergie dans le monde. Actuellement, la plupart de l'énergie produite mondialement est fabriquée à partir de matières non-renouvelables (*charbon, pétrole, gaz, nucléaire, etc.*) qui ont des réserves limitées (*les réserves globales en pétrole seront totalement consommées d'ici 53 ans [Benes, 2015]*). Pour assurer la qualité de vie et la croissance économique, l'humanité doit trouver un autre moyen de production d'énergie : (i) respectueux envers l'environnement, (ii) efficace et (iii) non-épuisable. Pour cela, il y a beaucoup de recherches sur le développement de nouvelles sources d'énergie renouvelable dite « verte ».

Ce chapitre est centré sur la consommation et les pertes à l'énergie sur échelle mondiale en prenant l'énergie électrique comme exemple de la situation énergétique mondiale.

### 5.1.1 Énergie électrique d'un point de vue globale

L'énergie électrique est la propulsion pour beaucoup des industrielles et ménages elle est omniprésente dans la vie quotidienne. Le graphique ci-dessous présente la consommation mondiale de l'énergie électrique de ces trente dernières années :

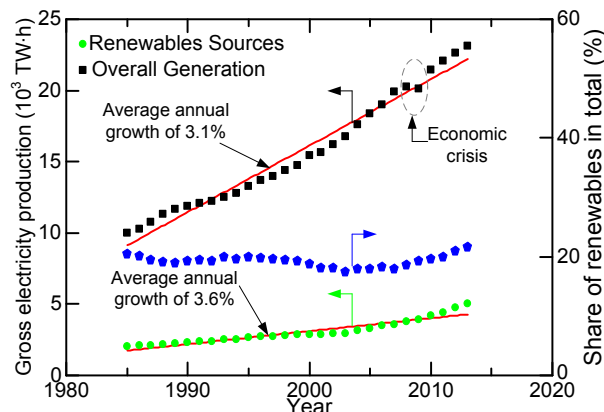


Fig. 5-1 L'histoire de la consommation globale d'électricité [British Petroleum, 2014]

Faisant l'analyse de la consommation électrique mondiale présentée Fig. 5-1 on peut constater que la consommation d'énergie électrique a presque triplé ces trente dernières années (*points noirs sur la Fig. 5-1*) la consommation d'électricité augmente en moyenne de 3% chaque année. D'autre part la part des sources renouvelables dans la production totale est plus ou moins stable, elle varie autour de 20% (*points bleus sur Fig. 5-1*). Le graphique Fig. 5-1 présente également une tendance positive sur l'échelle globale : la production d'énergie « verte » a une croissance la plus rapide (3.6% en moyenne par an) que la production totale (3.1% en moyenne par an). Grâce à ce phénomène la part de l'énergie renouvelable augmente, surtout depuis ces dix dernières années. Fig. 5-1 confirme aussi notre « addiction » aux matériaux énergétiques non-renouvelables car ~80% de l'électricité produite dans le monde provient de ces ressources. Pour nous libérer de

cette dépendance, il faut encore beaucoup de recherche, de travail industriel et surtout un changement de mentalité, il faut que les nations utilisent l'énergie dans manière plus responsable en limitant le gaspillage.

Pour rendre notre système électrique plus « vert » deux actions pouvant être adoptées :

- L'augmentation de la production d'énergie électrique en provenance de sources renouvelables
- Production de l'électricité à partir des pertes énergétiques (*la chaleur, les ondes électromagnétiques, les vibrations mécaniques etc.*)

La première méthode est surtout adoptée à l'échelle macro en utilisant les ressources naturelles d'énergie renouvelable (*le vent, l'eau, lumière du soleil*). La deuxième méthode ouvre la possibilité de produire l'énergie additionnelle pour les applications micro-énergétiques. Par la suite, ces deux moyens seront présentés brièvement.

#### 5.1.1.1 L'énergie renouvelable à l'échelle macro

À l'échelle macro une façon d'augmenter la stabilité et l'indépendance énergétique mondiale vis-à-vis des sources non-renouvelables est de produire l'électricité dans des centrales convertissant l'énergie primaire renouvelable. La figure Fig. 5-2 présente le pourcentage des différentes sources d'énergie électrique en détaillant les sources d'énergie renouvelables.

On peut remarquer que ~20% de l'énergie « verte » qui était produite en 2013 provient surtout de l'hydraulique (16.4%) et de l'éolien (2.9%).

L'énergie électrique renouvelable est produite en

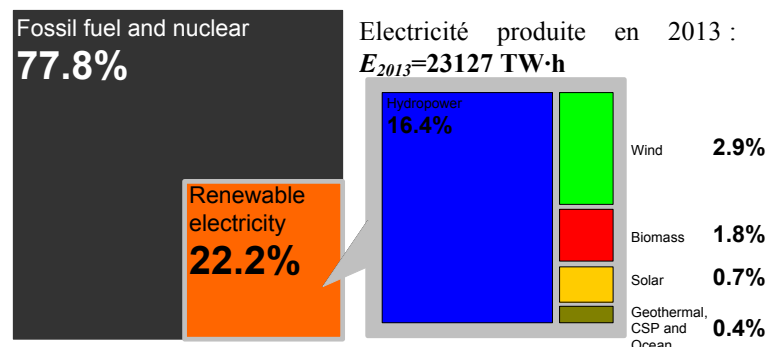


Fig. 5-2 La composition d'énergie électrique en 2013 [\[REN21, 2014\]](#)

utilisant différents générateurs offrant la possibilité de diversifier la production électrique en utilisant différents effets physiques. Cette propriété est très importante concernant la stabilité du système électrique mondiale.

Encore plus important est la question suivante : combien y a-t-il d'énergie « verte » dans les réserves naturelles. Car étonnamment la capacité en énergie renouvelable n'est pas infinie, l'énergie « verte » est limitée par la surface disponible, l'efficacité des convertisseurs actuels, etc. Tab. 5-1 présente les ressources globales disponibles et utilisées pour différentes sources d'énergie renouvelable. Tab. 5-1 démontre que le taux d'utilisation des réserves naturelles en énergie « verte » est très faible, en générale l'énergie la plus utilisée est l'énergie hydraulique (*avec 22.7%*). La plupart des sources sont utilisées de manière négligeable, ce qui veut dire que notre planète offre beaucoup plus d'énergie renouvelable telle nous convertissons actuellement. En 2014, l'humanité avait besoin de 2.85TW d'électricité (*~25000 TW·h d'énergie électrique*), en comparant cette puissance avec la puissance fournie par les différentes sources d'énergie « verte », Tab. 5-1 permet de conclure que la géothermie seule est capable de couvrir tous les besoins énergétiques mondiaux durant plusieurs années. Autrement dit, la transition de l'énergie « conventionnelle » basée sur les matériaux non-renouvelables (*gasoil, charbon ou nucléaire*) à l'énergie « innovatrice » basée sur la transformation de l'énergie primaire

renouvelable est possible et nécessaire, car notre planète nous offre une capacité exceptionnelle en énergie renouvelable, et est nécessaire pour assurer le développement, le progrès et la stabilité de notre civilisation.

**Tab. 5-1 Les ressources globales d'énergie renouvelable disponibles et utilisées**

Énergie	Ressources globales (TW)	Ressources (TW)	Pourcentage de ressources globales utilisées (%)
Vent	1700 <sup>a</sup>	0.318 <sup>b</sup>	0.187
Géothermie	45 <sup>a</sup>	0.012 <sup>b</sup>	0.027
Hydroélectrique	1.9 <sup>a</sup>	0.432 <sup>c</sup>	22.7
Panneau solaires et photovoltaïques	6500 <sup>a</sup>	0.139 <sup>b</sup>	0.021
Solaire thermique à concentration	4600 <sup>a</sup>	0.0025 <sup>b</sup>	0.001

<sup>a</sup> Données basées sur [\[Jacobson, 2011\]](#)

<sup>b</sup> Données basées sur [\[REN21, 2014\]](#)

<sup>c</sup> Données basées sur [\[British Petroleum, 2014\]](#)

### 5.1.1.2 L'énergie renouvelable à l'échelle micro

L'idée de produire l'énergie additionnelle renouvelable à l'échelle micro est un concept récent, qui s'est développé grâce (i) aux progrès dans le domaine de la nano- et micro-électronique permettant la miniaturisation des appareils électroniques, (ii) aux découvertes et développements de nouveaux matériaux électroniques et (iii) à la croissance rapide de nombre appareils électroniques en usage. Les progrès des méthodes technologiques permettent d'intégrer le générateur d'énergie directement dans l'appareil, la technologie rendant également possible la fabrication et le traitement des matériaux à la plus petite échelle. Le développement et les découvertes de nouveaux matériaux élargissent la gamme, les paramètres et réduit les coûts de l'électronique du futur. Et finalement le nombre des appareils électroniques en usage a fait croître la quantité d'énergie nécessaire consommée par l'équipement électronique. En général, les besoins énergétiques des appareils électroniques sont très faibles, de ce fait la puissance du générateur ne doit pas être grande. En plus, sachant que les appareils mobiles sont équipés en batterie, l'installation des générateurs intégrés peut augmenter l'autonomie de l'appareil.

Le concept de production d'électricité à partir des pertes d'énergie intéresse beaucoup de chercheurs [\[Harb, 2011\]](#), [\[Harne, 2013\]](#) ou [\[Matiko, 2014\]](#), etc. Cette idée innovatrice utilise les rejets d'énergie pour produire de l'énergie électrique. Le concept est révolutionnaire car il peut résoudre les problèmes d'alimentation des appareils à faible consommation. En plus, les systèmes électroniques actuels utilisent un grand nombre de capteurs et actionneurs, les câbles d'alimentation sont parfois plus chers que l'appareil. En utilisant l'énergie des pertes pour alimenter le capteur on peut obtenir un capteur énergétiquement autonome sans utiliser de câbles.

Pour savoir si cette idée est justifiée il faut quantifier les pertes énergétiques. On peut évaluer les pertes d'énergie en faisant l'analyse du graphique Fig. 5-3.

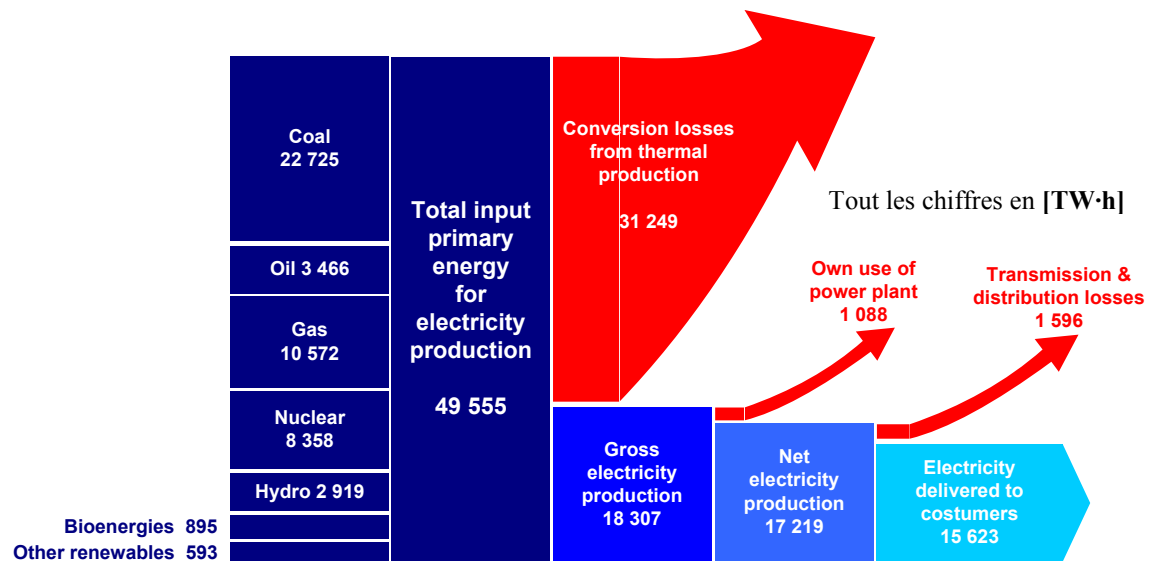


Fig. 5-3 Le flux d'énergie électrique dans le système mondial en 2007 tout les nombres en [TW·h] [International Energy Agency, 2008]

On peut alors remarquer que la quantité de pertes dans la chaîne de production et la distribution d'énergie électrique est très grande, seulement 31.5% d'énergie initiale est consommée. Alors ~70% d'énergie primaire est perdue. Cette conclusion montre l'importance et le potentiel dans la conversion de pertes d'énergie en énergie utile.

Dans la vie quotidienne on peut remarquer que les pertes d'énergie sont omniprésentes mais, parmi ces énergies, la plus gaspillée est la chaleur. L'énergie thermique est très difficile à conserver de plus, la chaleur est souvent le rejet de beaucoup des procédés industriels, elle accompagne le transport du courant électrique et est dissipée par tous les composant électroniques (*le  $\mu$ -processeur peut dissiper un flux de chaleur l'ordre de  $300W/cm^2$*  [Chowdhury, 2009]). Aux États-Unis toutes ces pertes de chaleur sont estimées à 470TW·h/an [Energetics, 2004], ce qui représente la consommation annuel d'énergie électrique de la Pologne et l'Italie réunies [British Petroleum, 2014]. Selon les études menées par [Cook, 1971], au moins 50% d'énergie primaire est perdue sous forme de chaleur, de ce fait ces pertes seraient très intéressantes à récupérer.

Le concept de production d'énergie à partir de pertes (ang. *Waste Energy Harvesting*) n'est pas seulement limité à la production d'énergie à partir de la chaleur dissipée. Dans notre vie quotidienne, on peut trouver beaucoup des énergies qui sont gaspillés, la graphique Fig. 5-4 présente quelques exemples de récupération d'énergie perdue.

Sachant que le développement technologique, surtout en micro- et nanotechnologie, permet la miniaturisation des appareils facilitent l'installation des récupérateurs d'énergie. Cette miniaturisation avec le concept de récupération des pertes d'énergie permet d'envisager la récupération à partir de nouvelles sources d'énergie. Dans ce cas on peut considérer le corps humain comme une source d'énergie avec un potentiel présenté Fig. 5-5. De plus le tableau Tab. 5-2 présente l'énergie consommée par le corps humain. En utilisant le même raisonnement, la récupération d'énergie peut être effectuée par de multiples appareils par exemple : les voitures, l'usine, etc. La quantité de pertes est tellement grande qu'en utilisant seulement les pertes, on pourrait limiter l'utilisation des ressources naturelles de la Terre au strict minimum.

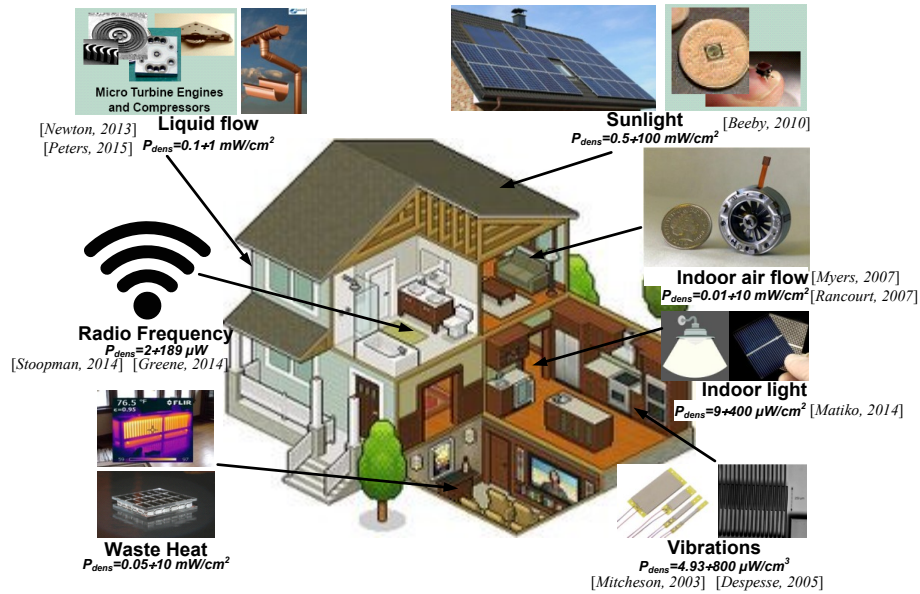


Fig. 5-4 Récupération d'énergie dans environnement domestique avec la densité de puissance correspondante [Beeby, 2010], [Myers, 2007], [Rancourt, 2007] [Matiko, 2014], [Mitcheson, 2003], [Despesse, 2005], [Stoopman, 2014], [Greene, 2014], [Newton, 2013], [Peters, 2015]

Les figures Fig. 5-3, Fig. 5-4 et Fig. 5-5 quantifient des pertes et permettent de conclure que la puissance perdue est au moins comparable à la puissance finale délivrée. Le concept d'utilisation de l'énergie de pertes permet d'utiliser de nouvelles sources d'énergie (comme le corps humain, le flux de l'air, les vibrations etc.). Tous cela amplifie l'importance énergétique de l'énergie gaspillée dans la stabilité et la diversification du système électrique mondial.

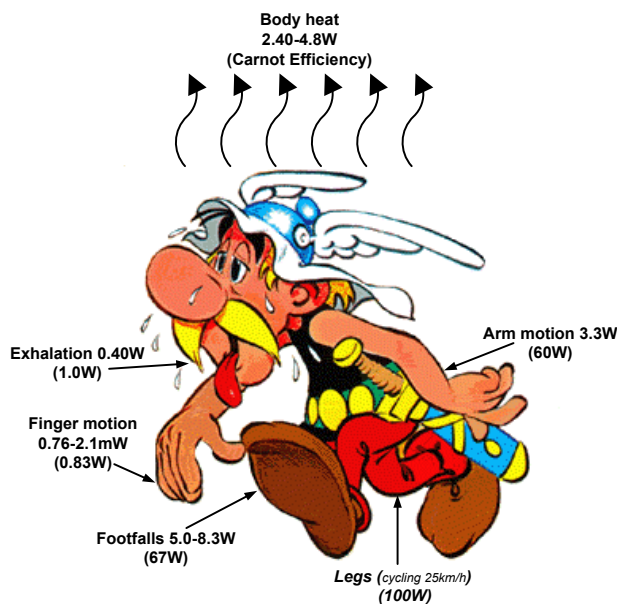


Fig. 5-5 La puissance fournit par le corps humain [Starner, 2004]

Tab. 5-2 La liste des énergies nécessaires au le corps humain pour effectuer certaines actions [Morton, 1953]

Activité	Énergie	
	Kcal/h	Watts
Sommeil	70	81
Allongé tranquillement	80	93
Assis	100	116
Debout à l'aise		
Conversation	110	128
Manger		
Ambulant		
Conduire la voiture	140	163
Jeu piano		
Faire les ménages	150	175
Charpenterie	230	268
Marcher, 6km/h	350	407
Nager	500	582
Grimper en montagnes	600	698
Courir longue distance	900	1 048
Sprint	1 400	1 630

Il y a encore un avantage majeur dans la production d'électricité à partir des pertes, c'est la compatibilité avec les systèmes électroniques. Comme mentionné précédemment l'électronique actuelle utilise beaucoup d'appareils à faible consommation. En utilisant ce



concept, on peut rendre certains appareils complètement autonomes et indépendants énergétiquement. Cette perspective est très intéressante dans l'industrie notamment l'internet des objets Fig. 5-6 (ang. *Internet of Things IoT*) [Gorlatova, 2010] grâce à l'auto-alimentation des appareils pouvant être simplifiée et moins coûteuse. La même tendance peut être remarquée dans le système de bâtiment intelligent Fig. 5-7 (ang. *intelligent building*) [Mclelland, 1988] qui utilise beaucoup de capteurs les pertes utilisées pour alimenter les capteurs offrent la simplification de système le rendent plus attractif économiquement (*pas de câblage nécessaire*).



Fig. 5-6 L'internet des objets

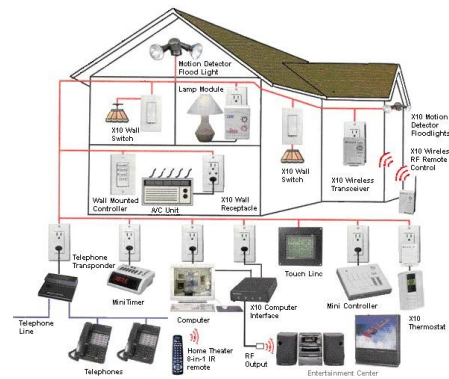


Fig. 5-7 L'exemple d'un bâtiment intelligent

## 5.2 Conclusions

Ce chapitre résume la situation énergétique à l'échelle mondiale en insistant sur les contraintes et les défis dans le système électrique. La stabilité d'un système réclame de nouvelles sources d'énergie permettant à la fois de rendre le système indépendant des matériaux fossiles et de contribuer au développement durable. Pour faire face à cette demande et assurer le développement constant sociétal et industriel, deux actions peuvent être adoptées. À l'échelle macroscopique, l'utilisation des sources renouvelables d'énergie (*vent, lumière solaire, l'eau, géothermie etc.*) doit être augmentée en sachant que la Terre offre des réserves considérables en énergie « verte ». À l'échelle microscopique, les pertes d'énergie peuvent être utilisées pour générer de l'énergie utile.

Le concept de production d'énergie à partir des pertes reçoit récemment beaucoup d'attention pour les raisons suivantes : (i) la puissance des pertes est comparable avec la puissance finale délivrée et les pertes sous différentes formes sont omniprésentes , (ii) l'augmentation de l'autonomie énergétique des appareils électroniques, (iii) la simplification de la topologie d'un système électronique, (iv) la contribution à la diversification et au développement durable en rendent possible la fabrication de systèmes autonomes.

Le concept d'alimenter les appareils à partir de pertes d'énergie rend possible d'utilisation de nouvelles sources d'énergie comme le corps humain, le courant d'air ou les vibrations etc. Les pertes seront la source d'énergie du futur en recouvrant les pertes, on sera capable de faire face aux consommations énergétiques en hausse continue, les réserves de minéraux fossiles en épuisement et réchauffement climatique.

# Chapter 6: L'énergie depuis les pertes – la perspective

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Les différentes formes de pertes nous obligent à choisir la méthode de récupération qui offre le plus grand rendement. Ce chapitre présente différentes méthodes de recouvrement d'énergie gaspillée en soulignant la conversion thermoélectrique. La thermoélectricité possède des avantages très demandés dans l'industrie des semi-conducteurs, mais elle est rarement utilisée, car elle souffre d'un manque des matériaux efficaces thermoélectriquement et économiquement. La solution doit proposer un matériau rentable, non-polluant, simple, performant et compatible avec la production à grande échelle. L'industrie numérique est basée sur le silicium (**Si**), le germanium (**Ge**) et le silicium-germanium (**Si<sub>x</sub>Ge<sub>1-x</sub>**) mais leurs usages en thermoélectricité est impossible à cause de la conductivités thermiques ( $\kappa$ ) trop élevées. Ce chapitre présente la possibilité de rendre **Si** attractif dans le domaine de la thermoélectricité grâce à la réduction de  $\kappa$  obtenue par la nanostructuration. Le concept de la réduction de  $\kappa$  dans **Si** peut encourager la popularisation de la thermoélectricité.

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## 6.1 Introduction

La production d'énergie à partir des pertes contient beaucoup de méthodes permettant cette conversion. La Fig. 5-4 présente quelques exemples de différentes pertes suffisantes pour être transformées en énergie électrique (*la chaleur, les vibrations, les ondes électromagnétiques, le courant d'air etc.*). Chaque type de pertes demande une méthode de conversion adaptée. La méthode de conversion impose la topologie, les dimensions minimales, le rendement et la puissance du générateur. La Fig. 6-1a présente la densité de puissance typique est présentée pour différentes méthodes de récupération d'énergie.

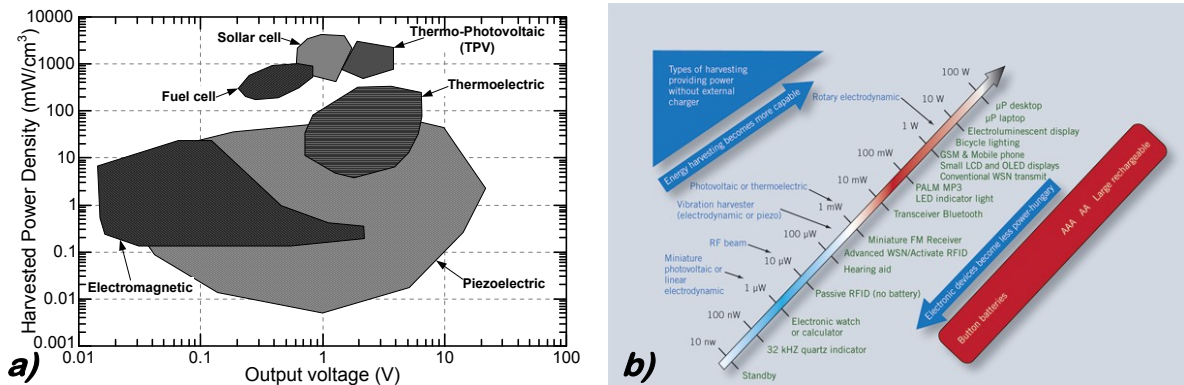


Fig. 6-1 a) La densité de puissance typique fournie pour différentes méthodes de récupération d'énergie [Cook-Chennault, 2008]; b) puissance nominale de différents appareils électroniques avec la méthode de récupération capable de les alimenter

Les exemples des appareils et les générateurs correspondant sont présentés sur la Fig. 6-1b. En analysant les Fig. 6-1a et Fig. 6-1b on peut constater que ces méthodes de conversion offrent différentes puissances de sortie, et que l'intervalle de puissances de sortie est très vaste (*de  $\sim 1\text{mW}/\text{cm}^3$  à  $\sim 10\text{kW}/\text{cm}^3$* ). Dans ces limites la plupart des appareils électroniques peuvent être alimentés. Dans le domaine de l'électronique mobile la prolongation de la période entre les rechargements de la batterie a permis d'augmenter l'autonomie énergétique des appareils. Considérant la quantité des pertes thermiques, l'omniprésence et la puissance, on peut dire que la production d'énergie a une importance stratégique pour l'électronique à basse consommation.

Cette thèse est consacrée à la production d'énergie à partir de chaleur dissipée. Les autres méthodes de récupération sont décrites dans la version anglaise de ce mémoire. Sachant que l'énergie thermique est la plus gaspillée dans le monde (*la moitié de chaleur est gaspillée*), la récupération de cette énergie est très importante. En même temps, la présence des pertes de chaleur est très marquée dans tous les appareils électroniques et, pour cette raison, la thermoélectricité est la méthode privilégiée pour les appareils électroniques. La densité de puissance typique pour les convertisseurs thermoélectriques (Fig. 6-1a) est comprise entre quelques unités et plusieurs centaines de  $\text{W}/\text{cm}^3$ . Cette plage de puissance de sortie couvre les besoins de la plupart des appareils électroniques, simultanément la tension de sortie est adaptée à l'électronique moderne. Les générateurs thermoélectriques offrent encore plus d'avantages comme : (i) la conversion directe ; (ii) l'absence des vibrations ; (iii) le travail silencieux ; (iv) la durée de vie très longue. Grâce à ces avantages, les générateurs thermoélectriques attirent surtout l'attention de l'industrie des semi-conducteurs. Dans la suite de ce mémoire, plus de détails concernant la thermoélectricité seront fournis.

## 6.2 Bases de la thermoélectricité

L'effet thermoélectrique a été découvert en 1821 par T. J. Seebeck [Velmre, 2010], mais il est resté inutilisé pendant ~150 ans. Grâce à leur robustesse les générateurs thermoélectriques ont trouvé « un emploi » dans l'industrie spatial. Ensuite, à cause de son coût élevé, la thermoélectricité est restée impopulaire. Actuellement, on observe le retour vers la thermoélectricité grâce au développement des nano- et micro-technologies permettant de moduler les propriétés des matériaux à l'échelle atomique (*d'ici deux ans les investissements en thermoélectricité vont tripler, Fig. 6-2a [Happich, 2014]*).

La conversion thermoélectrique est une conversion directe, c'est-à-dire que la chaleur est directement (*sans étapes intermédiaires*) transformée en électricité. L'effet thermoélectrique est basé sur la séparation de charges électriques provoquée thermiquement [Goldsmid, 2010]. Cette séparation de charge électrique crée la différence de potentiel donc la tension de sortie. Pour augmenter la tension de sortie la topologie dite  $\pi$  est utilisée (Fig. 6-2b) [Rowe, 1995]. Cette topologie fait que les deux barreaux sont électriquement connecté en série (*ligne en pointilles marque le courant*) et thermiquement en parallèle (*la chute de température est marquée avec  $\Delta T$* ). La mise en série rend possible l'augmentation de la tension de sortie, la mise en parallèle assure que les deux « colonnes » du générateur sont soumises aux mêmes conditions thermiques.

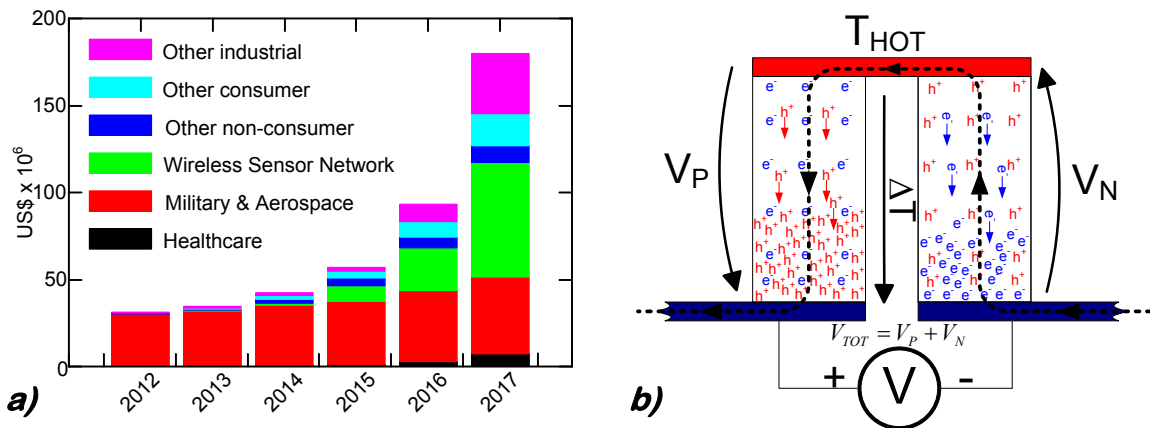


Fig. 6-2a) Prévision économique de la thermoélectricité ; b) Topologie conventionnelle de type  $\pi$  d'un thermogénérateur

La thermoélectricité est la conversion directe réalisée par les matériaux donc il est au centre de cette conversion. Pour comparer les performances thermoélectriques des différents matériaux la figure de mérite monodimensionnel ( $zT$ ) est utilisé Eq. 6-1 [Rowe, 1978].

Un bon matériau thermoélectrique a le  $zT$  le plus grand possible, alors la thermoélectricité demande des matériaux avec une conductivité électrique ( $\sigma$ ) et un coefficient de Seebeck ( $S$ ) très grands, et une conductivité thermique ( $\kappa$ ) très faible. Les conductions thermique et électrique sont

$$zT = \frac{\sigma \cdot S^2}{\kappa} \cdot T = \frac{\sigma \cdot S^2}{\kappa_{el} + \kappa_l} \cdot T \quad \text{Eq. 6-1}$$

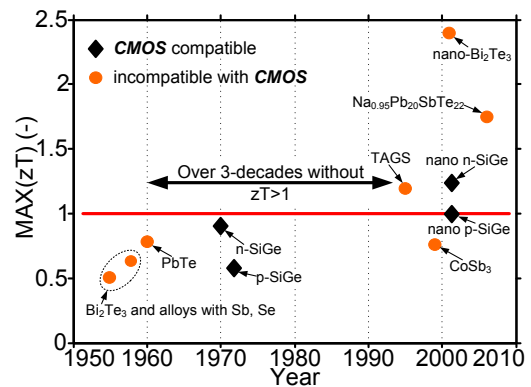


Fig. 6-3 La valeur maximale de  $zT$  en fonction de l'année de découverte

couplé or il n'y a pas de matériau qui soit à la fois isolant thermique et conducteur électrique. C'est pour cette raison que l'optimisation de  $zT$  est très difficile, et que pendant plus que 30 ans, la valeur maximale de  $zT$  est restée inférieure à 1 Fig. 6-3 [Majumdar, 2004]. La Fig. 6-4a présente les valeurs de  $zT$  en fonction de la température ( $T$ ) pour différents matériaux. On peut remarquer que la plupart des matériaux utilisés dans la thermoélectricité sont polluants, nocifs, chers, incompatibles avec la production massive industrielle (ex. **CMOS**) et complexes, ce sont les raisons de son impopularité.

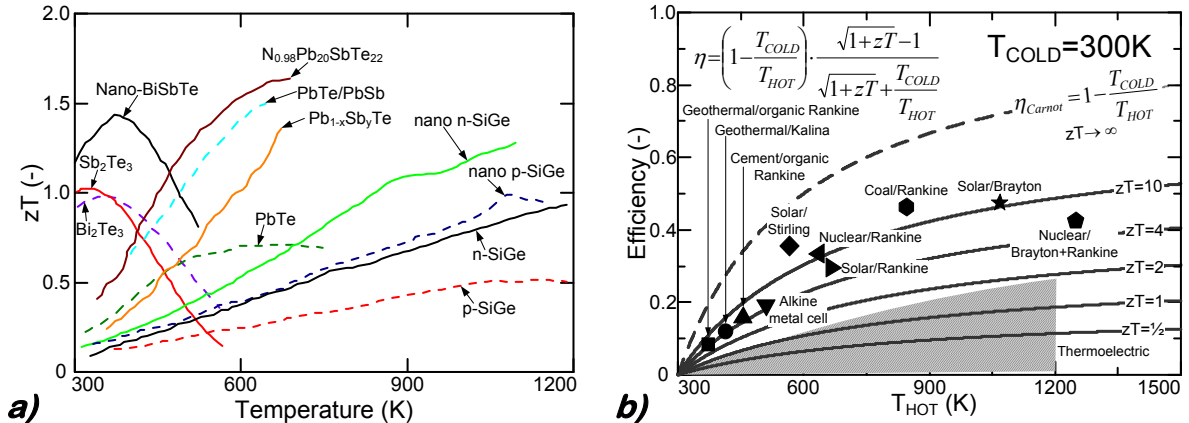


Fig. 6-4 a) Valeurs de  $zT$  en fonction de la température pour différents matériaux [Carmo, 2010], [Minnich, 2009] [Snyder, 2008]; b) le rendement thermoélectrique pour différentes valeurs de  $zT$

Le  $zT$  est très important car le rendement de la conversion ( $\eta$ ) dépend du  $zT$ . La Fig. 6-4b donne des informations supplémentaires concernant l'efficacité thermoélectrique. Premièrement, on peut dire que le rendement croît pour  $zT$  et  $T_{HOT}-T_{COLD}$  croissants, la zone couverte par la thermoélectricité actuelle est marquée. On peut constater que les rendements thermoélectriques sont assez modestes, pour les solutions commercialisées le rendement typique est de 3 à 8%. Fig. 6-4b permet de positionner la thermoélectricité par rapport aux autres conversions. On peut remarquer que la thermoélectricité est moins efficace que les autres conversions. Cela est dû à un manque des matériaux thermoélectriquement efficaces.

La popularisation de cette conversion sur le marché doit se réaliser par l'optimisation/la découverte des matériaux thermoélectriques à bas coût, compatibles avec la production massive et respectueuse envers l'environnement naturel. Selon [Tritt, 2008], les matériaux massifs, pas chers et avec  $zT \geq 4$  sera le « Saint Graal » qui popularisera la thermoélectricité. Actuellement, la valeur maximale de  $zT$  reportée est  $\sim 2$  [Venkatasubramanian, 2001]. En regardant la Fig. 6-4a, on peut dire que l'état de l'art actuel est loin de  $zT \approx 4$  empêchant la popularisation de la thermoélectricité.

Les exigences matérielles imposées par la thermoélectricité font que ni les métaux ( $\kappa$  trop élevé) ni les isolateurs ( $\sigma$  trop faible) ne peuvent être utilisés dans ce domaine. Entre les métaux et les isolants on a les semi-conducteurs qui offrent un compromis entre  $\kappa$  et  $\sigma$ . De ce fait le  $zT$  est maximal Fig. 6-5. Cette particularité explique pourquoi la plupart des matériaux thermoélectriques sont les semi-

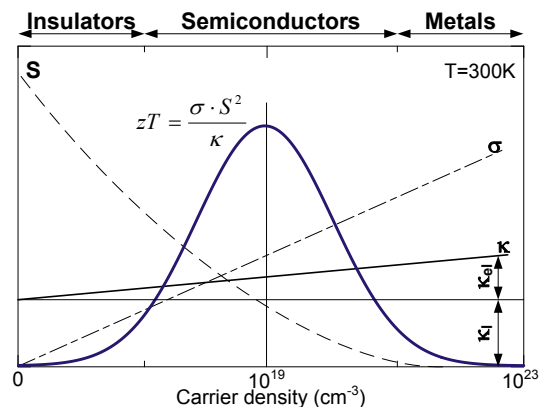


Fig. 6-5 Valeurs de  $zT$  en fonction de la densité de porteurs [Gardner, 1994]

conducteurs. En plus cela peut être un avantage si on considère la possibilité d'intégration de l'appareil thermoélectrique avec l'équipement électronique. Dans ce cas-là le générateur peut être fabriqué dans la même usine en utilisant le même matériau pour fabriquer le générateur et l'appareil électronique. Cette compatibilité industrielle est très intéressante si on veut rendre la thermoélectricité plus attractive économiquement. L'industrie numérique impose des matériaux compatibles avec la technologie **CMOS** : silicium (**Si**), Germanium (**Ge**) ou Silicium-Germanium (**Si<sub>x</sub>Ge<sub>1-x</sub>**).

Actuellement, seul **Si<sub>x</sub>Ge<sub>1-x</sub>** est utilisé dans la thermoélectricité grâce à la  $\kappa$  naturellement réduite Fig. 6-6a, le **Si** et **Ge** seuls ont une  $\kappa$  trop élevée, éliminant leur usage dans ce domaine. La nanotechnologie moderne offre la possibilité de réduire la  $\kappa$  sans altérer le  $\sigma$  et le **S**. Cette possibilité est particulièrement intéressante pour transformer **Si** ou **Ge** en matériaux thermoélectriques, performants, simples, facilement accessibles, non-nocifs et industriellement compatibles. L'idée de la réduction de  $\kappa$  utilise le découplage entre le transport thermique  $\kappa_l$  et électrique  $\kappa_e$  dans les semi-conducteurs. La chaleur est transporté par les vibrations de structure cristalline de matériau dit les phonons [Ziman, 2001] et le courant électrique utilise les électrons ou les trous pour la propagation [Grundmann, 2010]. Grâce à la nanotechnologie il est possible d'empêcher le transport des phonons réduisant  $\kappa_l$  sans perturber la propagation des électrons ou des trous. L'atténuation de transport thermique est obtenue par amincissement de matériau. Fig. 6-6b présente la  $\kappa$  de **Si** en fonction de l'épaisseur de **Si**. On peut remarquer que la  $\kappa$  diminue avec l'épaisseur de **Si**.

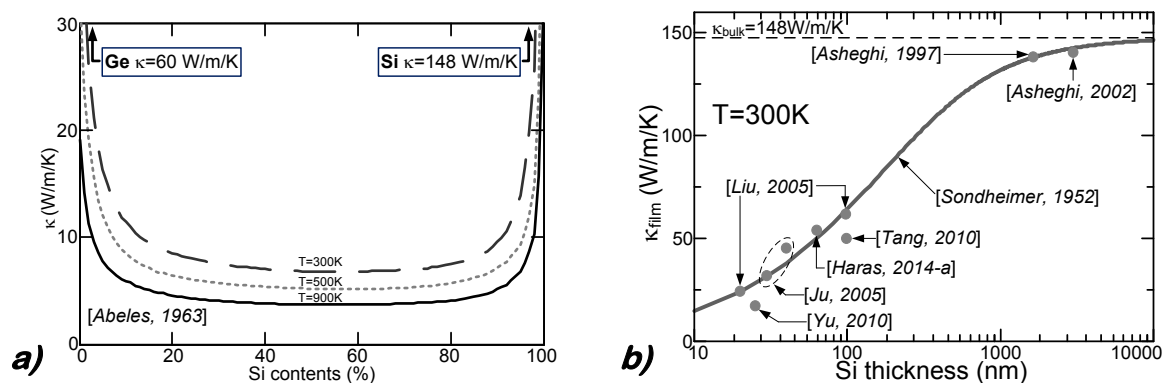


Fig. 6-6 a) La conductivité thermique de **Si<sub>x</sub>Ge<sub>1-x</sub>** en fonction de composition [Abeles, 1963]; b) la réduction de la conductivité thermique dans le **Si** quand l'amincissement de **Si** est utilisée

Cette thèse utilise l'effet de confinement sur la  $\kappa$  de **Si** pour améliorer les performances thermoélectriques. Grâce à cette réduction, la popularisation de la conversion thermoélectrique compatible avec la technologie **CMOS** peut être envisagée.

### 6.3 Conclusions

Ce chapitre présente les différentes méthodes de récupération d'énergie gaspillée en insistant sur la thermoélectricité. Malgré ses nombreux avantages, la thermoélectricité n'est pas populaire à cause des matériaux (i) coûteux, (ii) complexes, (iii) nocifs et (iv) incompatibles industriellement. Cette thèse propose une solution pour la populariser en utilisant **Si**, **Ge** ou **Si<sub>x</sub>Ge<sub>1-x</sub>** nanostructurés comme les thermoélectriques. Des multiples recherches confirment la réduction de  $\kappa$  dans **Si** quand une couche mince de **Si** est utilisée. La réduction de  $\kappa$  sans modification sur les  $\sigma$  et **S** est une perspective prometteuse et innovatrice pour faire sortir la thermoélectricité de l'ombre.

## Chapter 7: Thermoélectricité innovatrice

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Pour innover la thermoélectricité, deux possibilités peuvent être envisagées. Premièrement par l'optimisation des paramètres à l'échelle des matériaux, deuxièmement par le développement des topologies innovantes et performantes. Ce chapitre présente les études concernant les performances des matériaux **CMOS** dans la thermoélectricité. Les bonnes propriétés électriques des matériaux **CMOS** résultent d'une densité de puissance comparable avec les matériaux conventionnels. Grâce à l'utilisation de couche minces la  $\kappa$  peut être réduite. Alors les obstacles éliminant l'utilisation de matériaux **CMOS** ne sont pas insurmontables. L'utilisation de couches minces améliore 10-fois le rendement d'un générateur. La thermoélectricité compatible avec la filière **CMOS** utilisera des matériaux nanostructurés sous forme de couches minces. La thermoélectricité **CMOS** offrira une réduction des coûts, préservera l'environnement et pourra être produite massivement. L'explosion de la thermoélectricité sur le marché sera accélérée avec l'aide de l'industrie **CMOS**. C'est pour cette raison que l'optimisation électrique, thermique et topologique doit être effectuée pour rendre les matériaux **CMOS** attractifs dans le domaine de la thermoélectricité.

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## 7.1 Introduction

L'innovation dans la thermoélectricité peut se réaliser en adoptant deux actions :

- L'amélioration des propriétés des matériaux
- L'optimisation de la topologie du générateur

Cette thèse utilise des matériaux compatibles avec la technologie **CMOS** (**Si**, **Ge** et **Si<sub>x</sub>Ge<sub>1-x</sub>**). Parmi ces matériaux, seul **Si<sub>x</sub>Ge<sub>1-x</sub>** est utilisé comme thermoélectrique, le **Si** et le **Ge** ont une trop grande  $\kappa$  éliminant leur usage dans ce domaine. La réduction de  $\kappa$  est obtenue par l'amincissement du matériau provoquant ainsi l'atténuation de transport de chaleur sans perturber le transport de courant.

La deuxième possibilité innove la thermoélectricité en proposant des topologies non-conventionnelles de générateurs permettant d'augmenter la puissance de sortie, d'intégrer la flexibilité mécanique ou de fabriquer le générateur en consommant moins de matériaux.

L'innovation proposée dans cette thèse utilise les deux moyens. Premièrement les matériaux nanostructurés sont utilisés et arrangés dans la topologie innovatrice non-conventionnelle d'un générateur. Ce chapitre compare et évalue les performances thermoélectriques des matériaux compatibles avec la technologie **CMOS** avec le matériau thermoélectrique conventionnel. De plus, des études comparatives sont réalisées permettant ainsi de choisir la meilleure configuration topologique.

## 7.2 Optimisation du matériau

Pour maximiser les performances énergétiques d'un générateur thermoélectrique, les propriétés du matériau réalisant la conversion doivent être optimisées. Pour une conversion thermoélectrique performante, le coefficient de Seebeck (**S**) et la conductivité électrique ( $\sigma$ ) doivent être les plus grands possibles en gardant la conductivité thermique ( $\kappa$ ) la plus faible possible, cette situation augmentera la valeur de **zT** Eq. 6-1. Les semi-conducteurs ont la valeur de **zT** la plus grande comparée aux métaux et isolants Fig. 6-5. Les propriétés électrique des semi-conducteurs  $\sigma$  et **S** sont dominées par la densité de dopants, alors pour choisir la densité de porteurs optimale, le facteur de puissance (**PF**) est utilisé (*ang. Power Factor PF*) Eq. 7-1. Dans la version étendue de ce mémoire, la description complète de modèle est fournie. Grâce au modèle numérique, la modélisation de  $\sigma$  et **S** pour **Si**, **Ge** et **Si<sub>x</sub>Ge<sub>1-x</sub>** est réalisée, ces modèles rendent possible le calcul de **PF** en fonction de densité de dopants, présenté dans la Fig. 7-1. En faisant l'analyse de Fig. 7-1, on peut remarquer que **PF** est maximal quand la densité de dopants est de  $10^{19}\text{cm}^{-3}$  pour **Si** et **Si<sub>x</sub>Ge<sub>1-x</sub>**,  $10^{18}\text{cm}^{-3}$  pour **Ge**. Le générateur thermoélectrique basé sur ces matériaux sera le plus performant quand le niveau des dopants correspondant à valeur maximale de **PF** sera utilisé. Pour faire la comparaison entre les matériaux **CMOS** et le matériau conventionnel la valeur de **PF** calculée pour **Bi<sub>2</sub>Te<sub>3</sub>** de type **p** est présentée sur Fig. 7-1d. Les résultats présentés dans le Fig. 7-1 ouvrent la possibilité d'optimiser électriquement les matériaux (*car le **PF** prend en compte seulement  $\sigma$  et **S***). Mais pour obtenir une optimisation complète le transport thermique doit être étudié.

$$PF = \sigma \cdot S^2 \quad \text{Eq. 7-1}$$



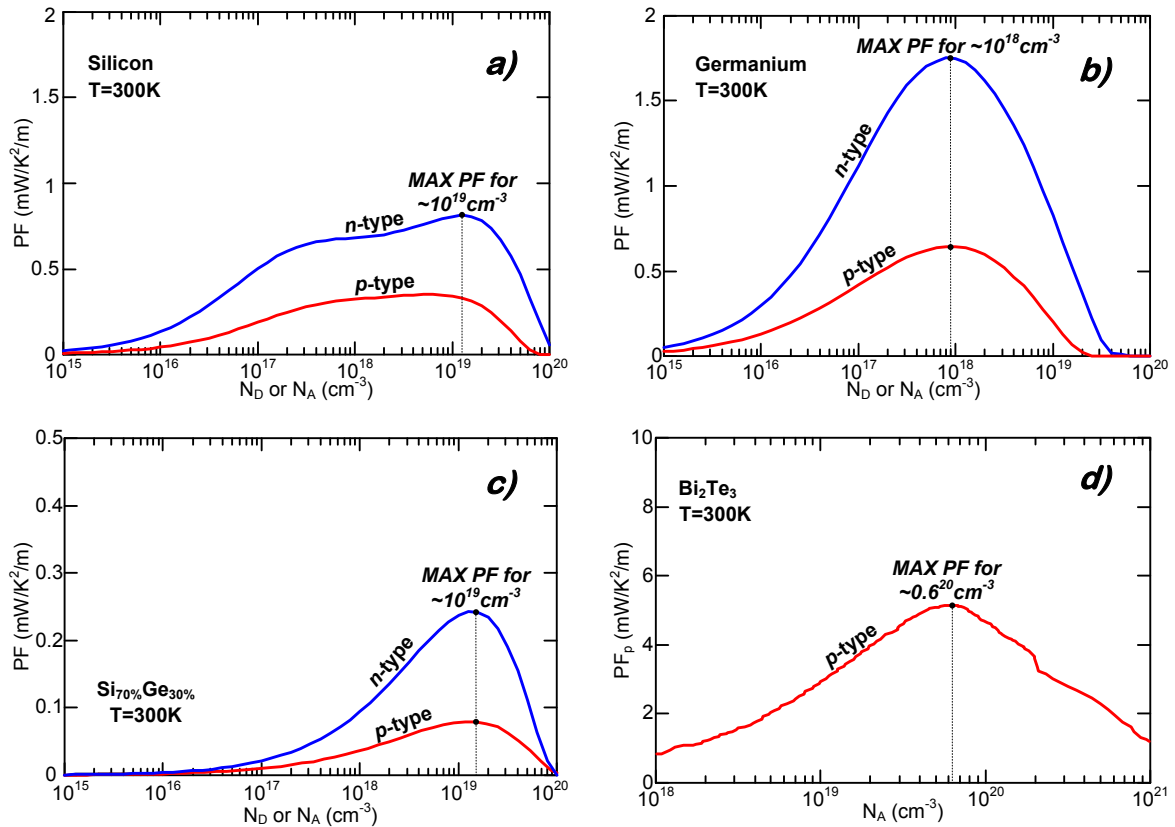


Fig. 7-1 Le facteur de puissance en fonction de la densité de dopant pour a) Silicium; b) Germanium; c) Si<sub>70%</sub>Ge<sub>30%</sub> et d) Bi<sub>2</sub>Te<sub>3</sub> type p [Snyder, 2008]

Comme signalé précédemment, l'adaptation de  $\kappa$  dans les matériaux **CMOS** pour les applications thermoélectriques est obtenue par amincissement comme présenté dans les cas de **Si** Fig. 6-6b. La thermoélectricité demande donc l'optimisation thermique (*obtenue par l'amincissement*) et électrique (*réalisée par utilisation de densité de dopants optimale*).

### 7.3 Innovation topologique

Dans le domaine de la thermoélectricité, il y a quelques exemples de différentes topologies de générateurs mais la plus populaire est la topologie dit  $\pi$  Fig. 6-2b. Sachant que la topologie conventionnelle est adaptée pour les matériaux massifs, la structure adaptée à l'utilisation de couches minces doit être choisie. Dans la version étendue de ce mémoire, la présentation de toutes les topologies et leurs performances sont présentes. Dans ce résumé, seule la topologie la plus performante sera présentée. Les études comparatives des performances des différentes topologies ont révélé que les générateurs avec la jonction *pn* sont moins performants. En court-circuitant la jonction, la résistance interne d'un générateur est fortement réduite permettant de passer plus de courant pour la même tension de sortie. De plus, la topologie doit assurer la possibilité d'utiliser la couche mince de matériau pour profiter de la réduction de  $\kappa$  présenté précédemment. La Fig. 7-2 présente la topologie d'un générateur planaire à couche mince avec épaisseur  $t$ . La jonction *pn* est court-circuitée par le contact métallique et aucun courant ne passe par la jonction.

Le générateur proposé est aussi plus adapté pour la fabrication sur la plaque **SOI**. Grâce à la topologie latérale, le matériau actif est plus efficacement utilisé (*la plaque SOI privilégiée les structures latérales*).

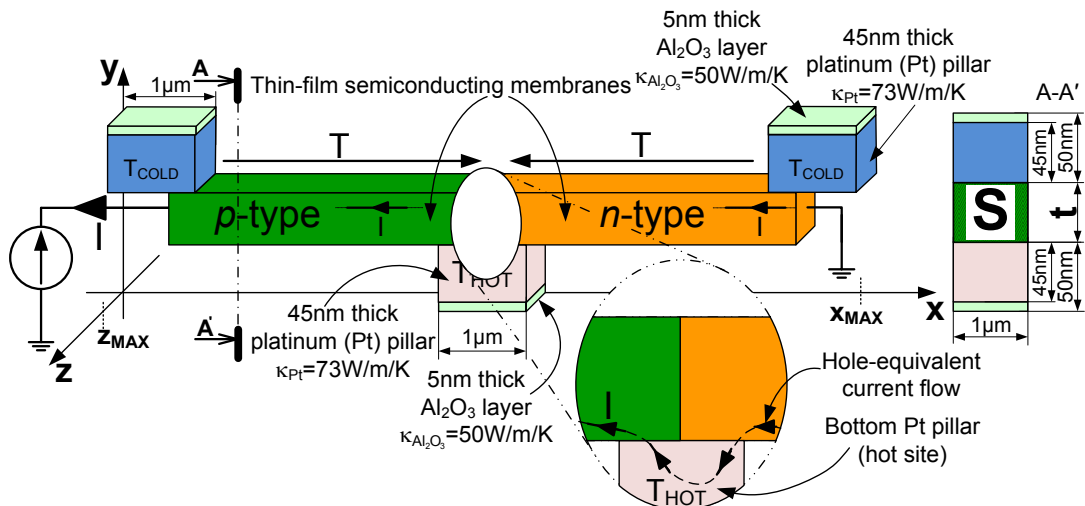


Fig. 7-2 Le générateur thermoélectrique planaire

L'évaluation de la puissance de sortie est possible grâce à un modèle numérique permettant de calculer les paramètres comme  $S$  ou  $\sigma$  en fonction de la densité des dopages et la température locale de réseaux pour les différents matériaux. La construction détaillée de ce modèle est présente dans la version étendue de ce mémoire. En supposant que la différence de température à travers un générateur est fixée, le calcul de puissance de sortie peut être effectué sans tenu compte de la  $\kappa$  du matériau.

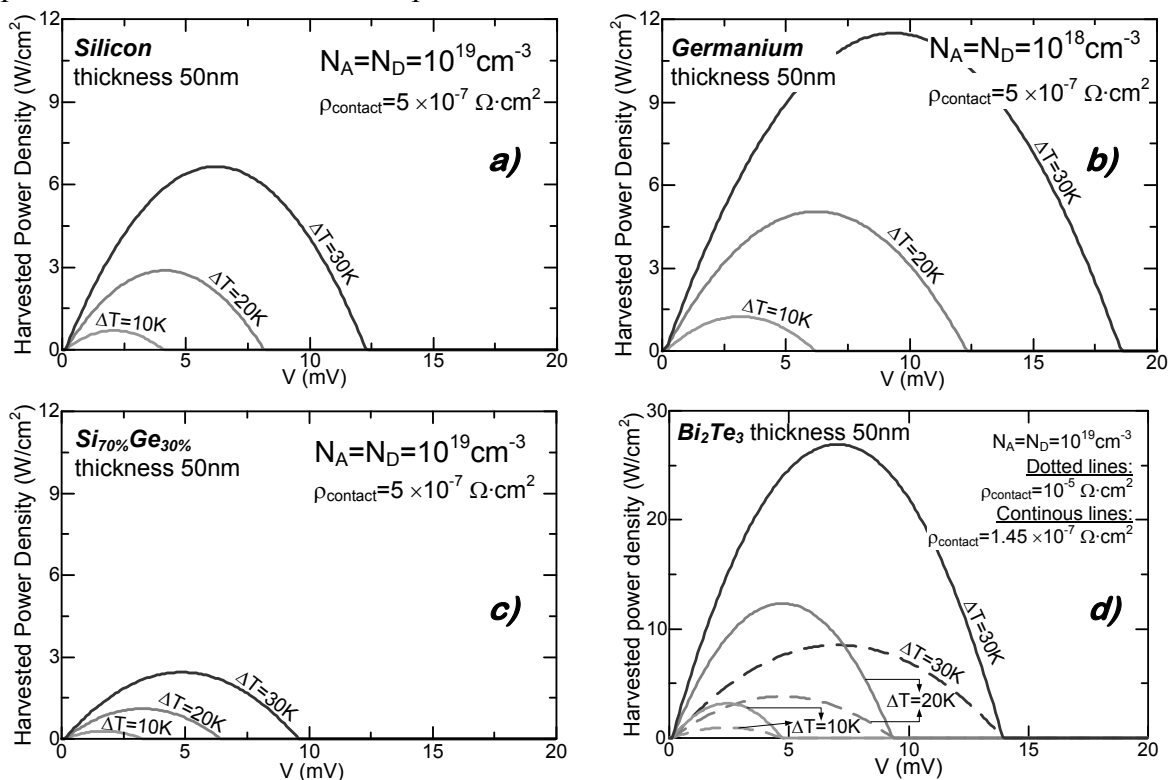


Fig. 7-3 La densité de puissance versus la tension de sortie pour différentes chûtes de températures pour la topologie latérale utilisant: a) Silicium; b) Germanium; c)  $\text{Si}_{70\%}\text{Ge}_{30\%}$  modèle analytique [Dismukes, 1964] et [Slack, 1991]; d)  $\text{Bi}_2\text{Te}_3$  modèle analytique [Luo, 2012]

La densité de puissance produite par le générateur en fonction de la tension de sortie est présentée dans la Fig. 7-3 [Haras, 2014-b]. L'analyse est faite pour le niveau de dopage optimale (densité de dopage pour laquelle  $PF$  est maximal Fig. 7-1) En analysant les performances des matériaux **CMOS**, on peut conclure que la puissance offerte est très

intéressante. Les performances d'un générateur sont dominées par la résistance interne du générateur. Cette résistance est constituée de résistances des semi-conducteurs et résistances de contacts semi-conducteur-métal. Plus la résistance de contact est grande, plus la puissance produite pour le matériau et  $\Delta T$  donné est petite. Pour les matériaux **CMOS**, la densité de puissance est inférieure à celle du **Bi<sub>2</sub>Te<sub>3</sub>** mais elle reste dans le même ordre de grandeur. En plus, la température autour de 300K n'est pas optimale pour les matériaux **CMOS** alors leurs performances ne sont pas maximales. La densité de puissance inférieure pour les matériaux **CMOS** est compensée par la possibilité de la production à grande échelle, sans pollution et à coût réduit.

Connaissant les performances électriques Fig. 7-3 et la  $\kappa$  Fig. 6-6b, l'analyse des performances peut être complétée par le calcul du rendement d'un générateur basé sur le **Si** Fig. 7-4 [Haras, 2015]. On peut alors remarquer que le rendement du générateur croît avec le  $\Delta T$  et l'épaisseur de **Si** diminuant. Quand l'épaisseur de **Si** est de 10nm, le rendement du générateur est 10 fois plus grand qu'avec le **Si** massif. Malgré cela l'efficacité de **Si** n'est pas très élevée ( $\sim 2\%$  pour  $\Delta T=600K$ ). Pour obtenir une augmentation de rendement, la  $\kappa$  peut être réduite en intégrant la couche mince avec les cristaux phononiques. Dans ce cas la  $\kappa$  est réduite d'une décade additionnelle. Le rendement maximal est alors de 20% pour l'épaisseur  $t=10\text{nm}$ .

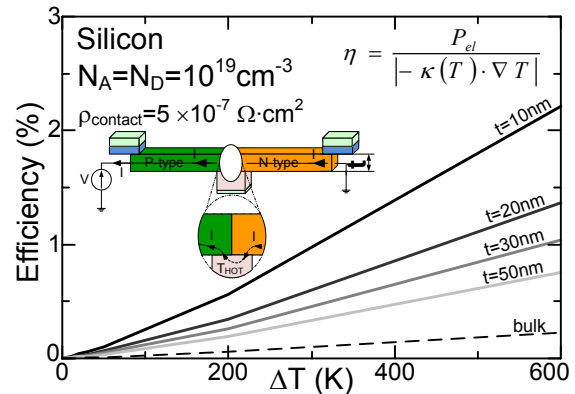


Fig. 7-4 Le rendement d'un générateur en fonction de température pour différents épaisseurs  $t$  de **Si** [Haras, 2015]

## 7.4 Conclusions

Ce chapitre présente l'analyse comparatrice des matériaux et des topologies dans la production d'énergie en utilisant l'effet thermoélectrique. L'accentuation est mise sur les performances des matériaux **CMOS**. La thermoélectricité peut être innovée en optimisant les matériaux et/ou les topologies. Dans ce projet, l'amélioration des performances thermoélectriques est réalisée au niveau de matériau (*réduction de  $\kappa$  par l'amincissement*) et de la topologie (*la topologie planaire moins gaspillant avec les plaques **SOI***). Les simulations ont montré que les matériaux **CMOS** sont très attractifs comme les matériaux thermoélectriques en produisant une densité de puissance comparable avec le matériau conventionnel **Bi<sub>2</sub>Te<sub>3</sub>** et offrant au même temps la compatibilité industrielle, la réduction du coût et la préservation de l'environnement.

La réduction de  $\kappa$  obtenue en diminuant l'épaisseur est la raison pour laquelle l'efficacité du générateur est améliorée. Pour le **Si** de 10nm, le rendement est 10 fois plus grand que pour le **Si** massif. Une réduction de  $\kappa$  encore plus importante peut être obtenue en intégrant la couche mince avec les cristaux phononiques, cette fusion pourrait donner un rendement de 20% (*record absolu dans la thermoélectricité actuelle*).

## Chapter 8: Thermoélectricité en pratique

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Dans la partie pratique de ce projet, le design, la fabrication et la caractérisation d'une plateforme micrométrique pour les mesures thermoélectriques dans la couche mince sont réalisés. Grâce à ce dispositif, la détermination de la  $\kappa$  est possible, la méthode de mesure utilisée est la méthode électrothermique. Les prescriptions topologiques imposées par la méthode sont : (i) l'isolation thermique du matériau caractérisé et (ii) l'élimination des pertes convectives. Ces demandes sont respectées soit au niveau topologique du dispositif soit par les conditions de mesure. L'application de la méthode électrothermique sur la plateforme proposée donne la valeur  $\kappa=57\pm 7.5\text{W/m/K}$ . Le résultat obtenu est confirmé par le modèle théorique avec bonne précision. La réduction de la conductivité thermique dans la couche mince de **Si** est expérimentalement observée et confirmée.

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## 8.1 Introduction

Ce chapitre est consacré à la présentation de la partie technologique de cette thèse. Le travail technologique est constitué (i) du projet du masque d'un appareil ; (ii) de la fabrication technologique ; (iii) de la caractérisation et (iv) de l'évaluation des résultats. Toutes ces étapes seront présentées brièvement, la version anglaise de cette thèse donne une description plus détaillée. Le but de cette partie est de fabriquer et caractériser l'appareil permettant de mesurer la conductivité thermique ( $\kappa$ ) dans les matériaux sous la forme de couche minces, les travaux sont réalisés sur la couche mince de silicium (**Si**).

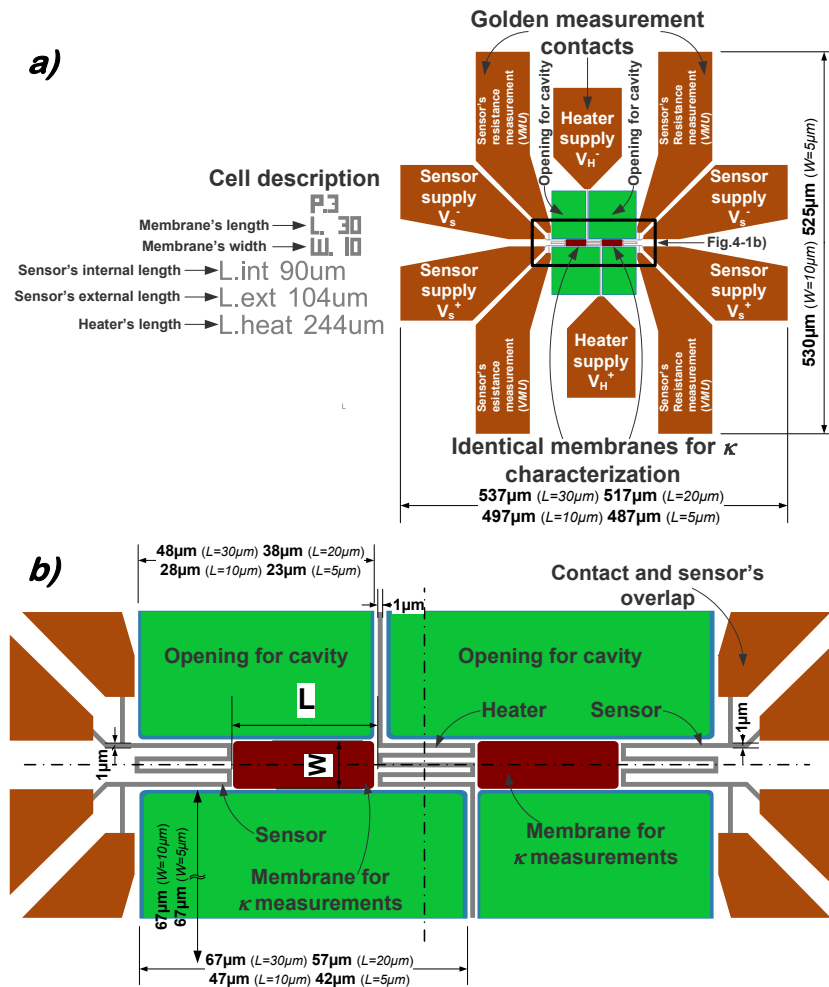
La caractérisation thermique des matériaux pose toujours beaucoup des problèmes car elle est très exigeante au niveau de l'architecture de l'appareil et de la procédure de mesure. Pour mesurer la  $\kappa$  précisément la plateforme de caractérisation doit isoler thermiquement le matériau caractérisé en réduisant les fuites thermiques. En plus, la topologie de l'appareil doit privilégier la propagation de la chaleur dans une direction, pour simplifier la détermination et augmenter la précision de la  $\kappa$ . Toutes ces exigences doivent être considérées au niveau de ce projet. Les méthodes de caractérisation sont :

- méthodes sans contact *e.g.* la spectroscopie Raman [[Abel, 2007](#)], [[Lysenko, 1999](#)], [[Piscanec, 2003](#)] etc.
- méthodes de contact *e.g.* microscopie thermique à balayage, [[Gomès, 2007](#)], [[Gomès, 2015](#)] etc.
- la caractérisation électrothermique *e.g.* en utilisant les signaux continus **DC** [[Hopkins, 2011](#)], [[Kim, 2012](#)], [[Yu, 2010](#)], [[Shi, 2003](#)], [[Tang, 2010](#)] ou  $3\omega$  méthode utilisent les signaux alternatifs [[Ftouni, 2012](#)], [[Sikora, 2012](#)] etc.

Cette thèse utilise la méthode électrothermique car (i) la méthode est simple du point de vue théorique ; (ii) la topologie dédiée pour cette méthode peut être facilement transformée en générateur thermoélectrique (**TEG**) ; (iii) l'équipement de mesure est classique, il n'y a pas besoin d'appareils de mesure très sophistiqués ; (iv) les paramètres mesurés sont les signaux électriques, leur détermination est donc très précise.

## 8.2 Le projet

D'abord, le design de la plateforme est réalisé en respectant les données de mesure. Le projet définit l'emplacement des objets, les dimensions et leur positionnement relatif. La Fig. 8-1 présente la plateforme désignée pour déterminer la  $\kappa$  de couche mince. La Fig. 8-1a présente la vue de dessous du dispositif complet. On peut remarquer que les contacts métalliques d'or occupent une surface importante sur la plateforme. Ces contacts sont prévus pour connecter les pointes de mesure avec la structure permettant la caractérisation de  $\kappa$ . La couche mince est située dans la partie centrale du dispositif, la  $\kappa$  de cette couche sera déterminé durant les mesures. Au premier regard on peut remarquer une certaine symétrie simplifiant le design et par conséquent la métrologie de l'appareil. Chaque dispositif est étiqueté en précisant les dimensions importantes pour la mesure. L'étiquette est fabriquée en matériau résistant aux produits chimiques utilisés pendant la fabrication pour que l'identification du dispositif soit toujours possible. La Fig. 8-1b présente une vue agrandie de la partie centrale. La membrane



**Fig. 8-1 a)** Vue de dessus sur la plateforme désignée en précisant les dimensions et les « composants » plus importants ; **b)** vue de la partie centrale de la plateforme précisant les dimensions et les objets importantes pour la mesure

pour laquelle la  $\kappa$  sera déterminé est située entre le serpentin chauffante (*ang. heater*) et le serpentin de la détection thermique (*ang. sensor*). Les membranes sont fabriquées en variant les dimensions : la largeur ( $W$ ) et longueur ( $L$ ). La cellule complète contient 16 dispositifs, avec  $W=5 \mu\text{m}$  et  $L=\{5 ; 10 ; 20 ; 30\} \mu\text{m}$  et avec  $W=10 \mu\text{m}$  et  $L=\{5 ; 10 ; 20 ; 30\} \mu\text{m}$ . La fabrication des membranes avec  $L$  et  $W$  différentes permet de caractériser l'influence des dimensions sur la  $\kappa$ . La membrane est entourée d'ouvertures pour les cavités qui permettront de suspendre la membrane et la détacher du substrat pendant la fabrication. Pour assurer le bon contact électrique entre les serpentins et la partie en or, les contacts sont fabriqués de telle manière que l'or est déposé dans une petite partie de la serpentine.

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### 8.3 Fabrication

Quand l'étape de conception est terminée l'échantillon peut être fabriqué, la description comment réaliser ce projet technologiquement sera présentée dans cette partie. En général tous les projets techniques ont deux « faces ». Première « face » est le design où les dimensions, l'emplacement des composants mais surtout l'idée du dispositif sont définis. La deuxième « face » c'est la recette de fabrication (*ang. process flow*) précisant les méthodes technologiques, les produits chimiques et la séquence des actions à effectuer pour réaliser le dispositif. Dans cette partie la recette de fabrication sera présentée. La Fig. 8-2 présente la séquence de fabrication pour réaliser le dispositif proposé. Les méthodes technologiques utilisées sont précisées. La photographie du **M**icroscope **É**lectronique à **B**alayage (**MEB**) située à l'intérieur présente l'appareil à la fin de procédure de fabrication. Pour fabriquer cet appareil une séquence de neuf actions doit être réalisée. Le point de

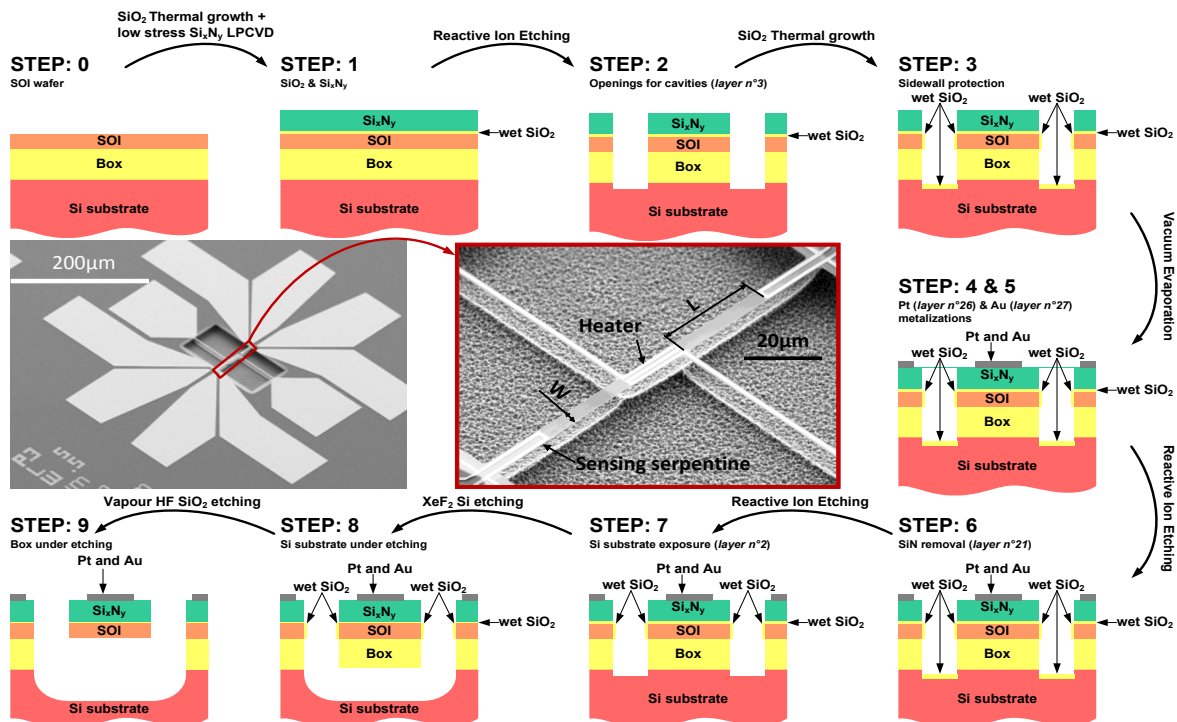


Fig. 8-2 La procédure de fabrication pour la plateforme des mesures thermoelectriques dans les matériaux à couche-mince [Haras, 2014-a]

départ, c'est la plaque **SOI** (*Silicium sur isolateur*). Sur la plaque l'oxyde de silicium humide (**wet SiO<sub>2</sub>**) croît et le nitrure de silicium à faible contrainte (**Si<sub>x</sub>N<sub>y</sub>**) est déposé (**STEP 1**). Le **wet SiO<sub>2</sub>** sert alors de couche d'arrêt protégeant le **SOI** contre les attaques chimiques. Le **Si<sub>x</sub>N<sub>y</sub>** est utilisé pour renforcer mécaniquement la structure et isoler électriquement le **SOI**. Ensuite les ouvertures des cavités sont gravées en utilisant une gravure ionique réactive (**Reactive Ion Etching RIE**). Ces ouvertures permettront de détacher la membrane du substrat. Pour protéger les flancs de **SOI**, la protection de **wet SiO<sub>2</sub>** est fabriquée en utilisant la croissance thermique (**STEP 3**). Consécutivement, les deux métallisations sont effectuées, la première en platine (**Pt**) (**STEP 4**) et la deuxième en or (**Au**) (**STEP 5**). Le **Pt** est utilisé pour former tous les serpentins et l'étiquetage des dispositifs. Le **Pt** a été choisi car la température influence linéairement sur ses propriétés électriques. Grâce à cette linéarité, la procédure de mesure est simplifiée. Les contacts de mesure sont faits en **Au** car ce métal dans sa forme pure est très tendre permettant à la pointe de mesure de s'immerger dans **Au**. Grâce à ce phénomène, la résistance parasite entre le contact et la pointe est réduite. Après les métallisations, le **Si<sub>x</sub>N<sub>y</sub>** est gravé de membrane (**STEP 6**). Grâce à la couche d'arrêt il est possible de graver totalement **Si<sub>x</sub>N<sub>y</sub>** sans endommager **SOI**. Après le **wet SiO<sub>2</sub>**, fabriqué à l'étape **STEP 3** est sélectivement gravé jusqu'au fond des cavités pour exposer le substrat de **Si** (**STEP 7**). L'exposition de substrat de **Si** permet l'attaque chimique de substrat. En utilisant le gaz **XeF<sub>2</sub>**, la gravure sélective du substrat est réalisée (**STEP 8**). Grâce à cette gravure, la membrane **SOI** et **Box** est détachée de substrat. Pour terminer la fabrication, la couche de **Box** est gravée en utilisant l'acide fluorhydrique (**HF**) sous sa forme gazeuse (**STEP 9**). Les deux dernières étapes sont réalisées en utilisant le gaz pour graver les matériaux. Ce choix a été fait car la contrainte et la pression mécanique sont réduites, permettant ainsi de détacher la membrane du substrat et du **Box**. Les photos de l'appareil à la fin de la production sont présentées dans la Fig. 8-2. On peut voir que la membrane est suspendue et que les serpentins fabriqués en **Pt** ne sont pas abimés.

## 8.4 Caractérisation

Après la fabrication la  $\kappa$  de la couche mince de **Si** peut être mesurée. La  $\kappa$  peut être mesurée dans cette topologie en suivant la méthode décrite Fig. 8-3. Cette méthode est basée sur l'hypothèse que la puissance électrique ( $P_H$ ) dissipée dans le serpentin chauffant situé dans la partie centrale de la membrane est totalement transformée en flux de chaleur ( $Q$ ) alors  $P_H=Q$ . Pour s'approcher de cette hypothèse, la mesure doit être effectuée sous vide, permettant de réduire les pertes de chaleur par convection. Le  $Q$  Fig. 8-3 produit dans le serpentin chauffant est divisé en deux parties complètement identiques grâce à la symétrie du dispositif. Alors le  $Q/2$  est transporté vers chaque thermomètre via la membrane suspendue. Quand le  $Q/2$  arrive vers le thermomètre, sa température ( $T_S$ ) augmente en fonction du  $\kappa$  de la membrane. Pour déterminer la  $\kappa$  de la membrane on doit connaître : la puissance  $P_H$ , les températures du serpentine chauffant ( $T_H$ ) et du thermomètre ( $T_S$ ) ainsi que les dimensions de la membrane  $W$ ,  $L$  et  $t$ . La  $\kappa$  est calculée en utilisant la formule Eq. 8-1, la détermination de  $\kappa$  est possible quand les températures  $T_H$  et  $T_S$  sont connues. La mesure des températures se fait indirectement en mesurant le changement de la résistivité électrique du serpentin.

Le calcul de  $\kappa$  présenté par Eq. 8-1 fait quelques simplifications. D'abord le profil de température dans la membrane est supposé linéaire. Le thème  $\nabla T$  dans la loi de la diffusion de la chaleur est remplacé par le thème  $(T_H-T_S)/L$ . Pour respecter l'hypothèse que le  $\nabla T$  est linéaire, la membrane est détachée du substrat éliminant la fuite de chaleur par le substrat. En plus, la mesure est effectuée sous vide en réduisant ainsi les pertes convectives de la chaleur depuis la membrane. L'isolation thermique de la membrane et la mesure sous vide justifient l'hypothèse de  $\nabla T$  linéaire dans la membrane. Alors l'exécution de cette mesure sous vide permet de remplacer  $\nabla T$  par  $(T_H-T_S)/L$  et de considérer la puissance électrique  $P_H$  égale à flux de chaleur  $Q$ . Comme signalé dans Eq. 8-1, les valeurs de  $T_H$  et  $T_S$  doivent être connues, la mesure des températures est faite indirectement en mesurant la résistivité électrique du serpentin. Pour relier la résistivité avec la température, les mesures de calibration sont effectuées avant de déterminer  $\kappa$ . Par la suite, la procédure de calibration des serpents est présentée.

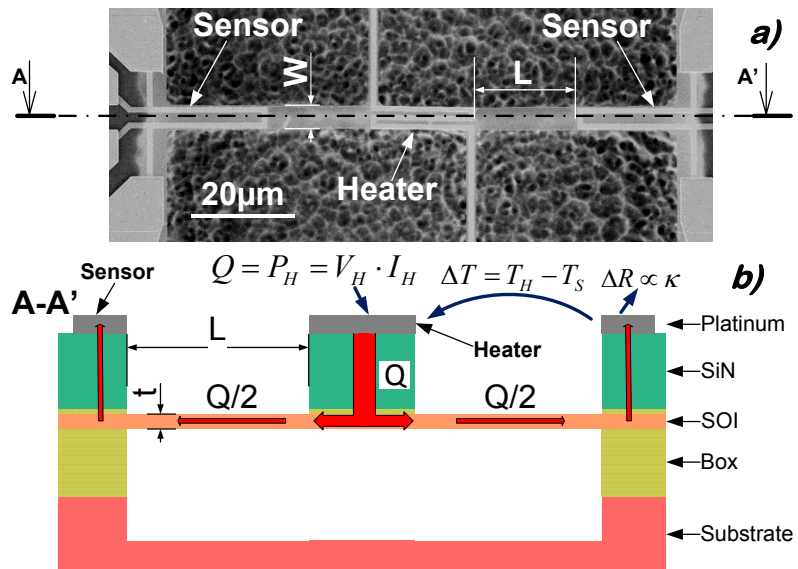


Fig. 8-3 La méthode électrothermique pour déterminer  $\kappa$  dans couche avec épaisseur  $t$ ; a) vue de dessus sur la membrane de longueur ( $L$ ) et largeur ( $W$ ); b) la section coupe suivant la ligne A-A' dans la Fig. 8-3a)

$$\kappa = \frac{1}{2} \frac{P_H}{T_H - T_S} \cdot \frac{L}{W \cdot t} \quad \text{Eq. 8-1}$$



### 8.4.1 Calibration du serpentín de détection thermique

Pour déterminer la température  $T_S$  utilisée dans Eq. 8-1, la calibration du serpentín de détection thermique doit être effectuée. La méthode électrothermique détermine la température  $T_S$  indirectement en mesurant la résistivité électrique pour différentes températures. Les serpentíns de cette plateforme sont fabriqués en **Pt** qui présente une dépendance linéaire entre la résistivité et la température. Grâce à cette linéarité, la mesure de  $\kappa$  est plus simple. Les calibrations et la détermination de  $\kappa$  est faite dans la chambre à vide pour réduire les pertes convectives de chaleur afin de rendre l'analyse plus précise et plus simple. En plus, l'échantillon est placé sur une plaque chauffante avec la possibilité de contrôler sa température très précisément. La température de la plaque chauffante est utilisée comme température de référence ( $T_{CHUCK}$ ).

Pour calibrer le serpentín de détection thermique, la résistivité du platine ( $\rho_{Pt}$ ) est mesurée pour différentes températures  $T_{CHUCK}$ . Pour éviter l'échauffement par l'effet Joule la mesure de  $\rho_{Pt}$  est exécutée en utilisant une très faible tension de mesure, la  $\rho_{Pt}$  est mesurée utilisant le montage dit quatre-pointes permettant de déterminer  $\rho_{Pt}$  avec une très grande précision. La Fig. 8-4 présente les résultats de calibration obtenues dans le serpentín de détection dans la membrane avec  $W=10\mu\text{m}$ . La Fig. 8-4

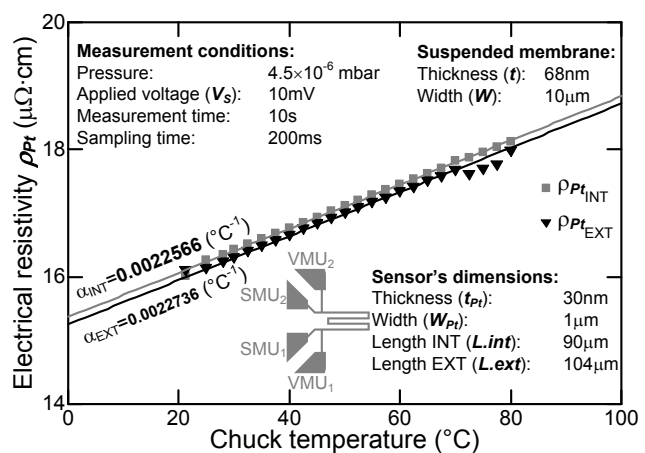


Fig. 8-4 Résistivité de la platine en fonction de la température de référence

confirme la dépendance linéaire entre la  $\rho_{Pt}$  et la température signalée précédemment. Grâce à la caractéristique présentée Fig. 8-4, le coefficient thermique de la résistivité électrique ( $\alpha_{Pt}$ ) a pu être déterminé. La valeur moyenne de  $\alpha_{Pt}=0.002242^\circ\text{C}^{-1}$  est extraite grâce aux calibrations et cette valeur sera utilisée pour estimer  $T_H$ . La Fig. 8-4 achève la calibration du serpentín de la détection thermique. Par la suite, le serpentín chauffant doit être calibré.

### 8.4.2 Calibration du serpentín chauffant

Pour évaluer l'influence de l'effet Joule sur la  $\rho_{Pt}$  du serpentín chauffant, la mesure en balayant la tension appliquée ( $V_H$ ) pour la  $T_{CHUCK}$  constant et stabilisée est exécutée. Cette mesure donne des informations sur des variation de  $\rho_{Pt}$  en fonction de la  $T_H$  qui augmente à cause de l'effet Joule. Les résultats de cette caractérisation sont présentés sur la Fig. 8-5 pour le serpentín chauffant dans la membrane avec  $W=10\mu\text{m}$  et deux  $T_{CHUCK}$  différents. Quand la tension  $V_H$  augmente, l'effet Joule devient plus important et la

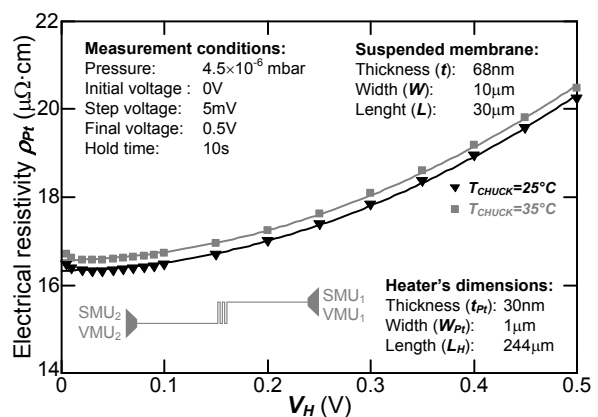


Fig. 8-5 Résistivité de Pt ( $\rho_{Pt}$ ) en fonction de la tension  $V_H$  pour  $T_H$  fixe

$T_H$  commence à monter, provoquant le changement de  $\rho_{Pt}$ . La relation entre  $\rho_{Pt}$  et  $V_H$  est parabolique qui est directement lié avec la relation entre la résistance électrique et la puissance. Comparant la Fig. 8-4 pour  $T_{CHUCK}=25^\circ\text{C}$  ou  $35^\circ\text{C}$  avec la Fig. 8-5 pour de faibles tensions  $V_H$ , on peut remarquer que la valeur  $\rho_{Pt}$  est comparable. Cette observation confirme que le comportement parabolique sur la Fig. 8-5 pour les tensions  $V_H$  plus importantes est strictement provoqué par l'effet de Joule.

La calibration du serpentin chauffant est finalisée en faisant la relation entre  $T_H$  et  $V_H$ . Pour trouver cette relation, la valeur de  $\alpha_{Pt}$  obtenue lors de la calibration précédente (Fig. 8-4) est utilisée. Sachant que la résistance de  $Pt$  change de manière linéaire avec la température, on peut calculer  $T_H$  en fonction de  $V_H$  en utilisant Eq. 8-2. La Fig. 8-6 présente l'interprétation graphique de Eq. 8-2. Analysant la Fig. 8-6, on peut remarquer que  $T_H$  peut avoir des valeurs très élevées quand la tension  $V_H$  est importante. Sachant que les dimensions du serpentin chauffant sont micro- et nanométriques on peut conclure que quand  $T_H$  est très grand, le serpentin chauffant produit un flux thermique très important. Cette caractérisation termine l'étape de calibration. En utilisant la Fig. 8-4,  $T_S$  peut être déterminée en mesurant la  $\rho_{Pt}$ , et en utilisant la Fig. 8-6 la  $T_H$  est connue pour la tension  $V_H$  donnée. Maintenant la mesure de  $\kappa$  peut être réalisée.

$$T_H(V_H) = T_{CHUCK} + \frac{\left( \frac{\rho_{Pt}(V_H)}{\rho_{Pt}(V_H=0)} - 1 \right)}{\alpha_{Pt}} \quad \text{Eq. 8-2}$$

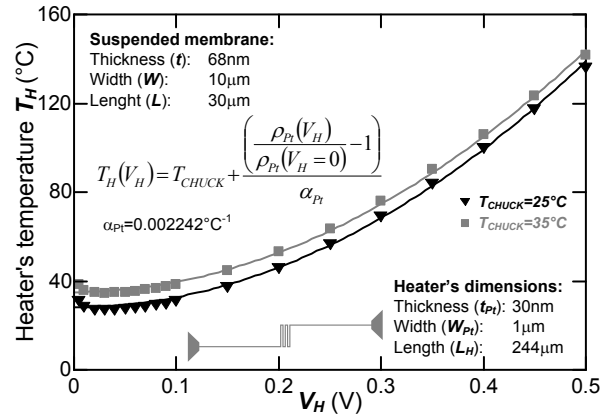


Fig. 8-6 La température du serpentin chauffant en fonction de la tension  $V_H$  pour la membrane avec  $W=10\mu\text{m}$  pour différentes températures  $T_{CHUCK}$

#### 8.4.3 Mesure de la $\kappa$

La mesure de la  $\kappa$  est quasi identique aux calibrations effectuées précédemment. Quand  $\kappa$  est mesurée, la tension appliquée au serpentin chauffant ( $V_H$ ) est balayée la mesure de  $\rho_{Pt}$  pour le serpentin de détection thermique est exécutée. Dans cette configuration, le changement de  $\rho_{Pt}$  dans le serpentin de détection thermique est provoqué par l'échauffement du serpentin chauffant, comme expliqué sur Fig. 8-3. Grâce aux calibrations (Fig. 8-4 déterminant  $T_S$  et Fig. 8-5 déterminant  $T_H$ ), on est capable de déterminer la chute de température sur la membrane en mesurant  $\rho_{Pt}$  pour deux serpentins. La Fig. 8-7 présente la  $\kappa$  mesurée dans deux membranes la première de dimensions  $W=10\mu\text{m}$  et  $L=30\mu\text{m}$  Fig. 8-7a et la deuxième pour la membrane de dimensions  $W=L=5\mu\text{m}$  Fig. 8-7b. La  $\kappa$  déterminée par cette méthode est présentée en Fig. 8-7. La valeur moyenne de la  $\kappa$  mesurée dans toutes les membranes de  $Si$  d'une épaisseur de 68nm est  $\kappa=57\pm 7.5\text{W/m/K}$ . On peut constater que, malgré les différents  $L$  et  $W$  pour les deux membranes, la valeur de la  $\kappa$  mesurée est presque identique. Cette observation permet de conclure que la  $\kappa$  n'est dépendante ni de  $W$  ni de  $L$ . Sachant que la  $\kappa$  pour le  $Si$  massif est  $\kappa_{bulk}=148\text{W/m/K}$  pour la couche mince de  $Si$  avec l'épaisseur de 68nm, la  $\kappa$  est réduite presque 3 fois comparée au  $Si$  massif. Alors la réduction de la  $\kappa$  présentée dans la Fig. 6-6b est ici confirmée expérimentalement. En analysant la Fig. 8-7 on peut remarquer le

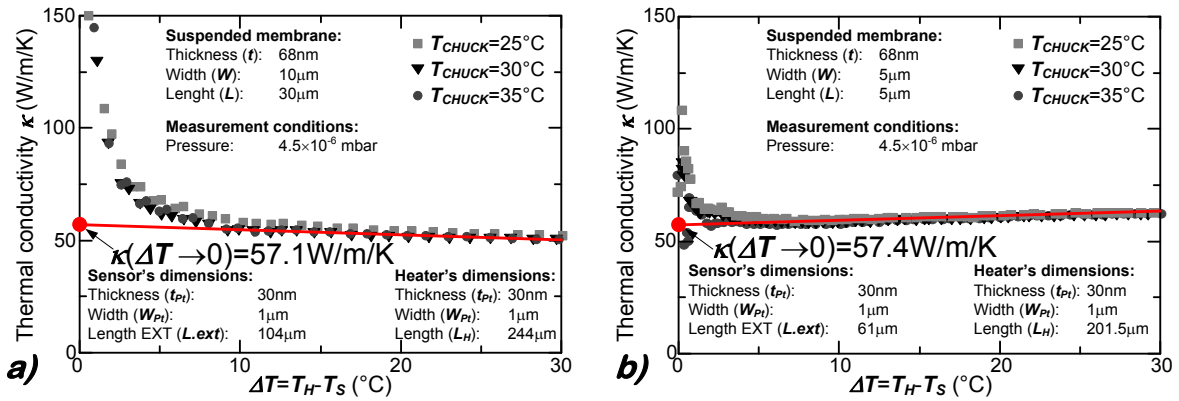


Fig. 8-7 La conductivité thermique en fonction de la différence de température sur la membrane pour *Si* d'épaisseur 68nm a) Longueur  $L=30\mu\text{m}$ , Largeur  $W=10\mu\text{m}$ ; b) Longueur  $L=5\mu\text{m}$ , Largeur  $W=5\mu\text{m}$  [Haras, 2014-a]

même comportement des données expérimentales. Pour des faibles  $T_H - T_S$ , la mesure donne des valeurs aléatoires de  $\kappa$  liée à la sensibilité du serpentin de détection thermique. Quand la puissance injectée  $P_H$  est faible elle n'est pas capable de chauffer le serpentin de détection thermique pour obtenir un changement de  $\rho_{Pt}$  mesurable. Alors, quand la différence  $T_H - T_S$  est faible, les valeurs de  $\kappa$  ne sont pas correctes. On peut aussi remarquer que cette zone, où les valeurs de  $\kappa$  sont aléatoires, est beaucoup moins importante pour la membrane courte  $L=5\mu\text{m}$ . C'est le couplage thermique qui est inversement proportionnel à la distance  $L$  pour les membranes courtes. La puissance injectée  $P_H$  peut être moins importante pour provoquer un changement de  $\rho_{Pt}$  mesurable.

## 8.5 Conclusions

Ce chapitre présente le design, le procédé de fabrication et la caractérisation d'une plateforme micrométrique permettant la détermination de la  $\kappa$  dans la couche. Le design proposé est dédié pour mesurer la  $\kappa$  en utilisant la méthode électrothermique. La fabrication de cette plateforme utilise différentes techniques comme : la croissance thermique, le dépôt à faible pression, la gravure sèche et humide et l'évaporation. Le design et la procédure de fabrication sont confirmés en réalisant l'appareil sur une plaque **SOI** avec une couche active de **Si** d'épaisseur 68nm.

L'appareil fabriqué est ensuite caractérisé en utilisant la méthode électrothermique. Grâce à la grande isolation thermique de la membrane caractérisée et l'exécution de la mesure sous vide, la chute de température sur la membrane est linéaire et la puissance électrique est totalement transformée en chaleur par effet Joule. Cette hypothèse permet de mesurer  $\kappa$  simplement, efficacement et précisément. La valeur de  $\kappa$  dans la couche mince de **Si** est  $\kappa=57\pm 7.5\text{W/m/K}$ , qui est diminuée d'un facteur 3 comparé au  $\kappa$  pour **Si** massif. La Fig. 8-8 compare le résultat avec le modèle théorique, on peut remarquer que l'accord entre l'expriment et la théorie est satisfaisant.

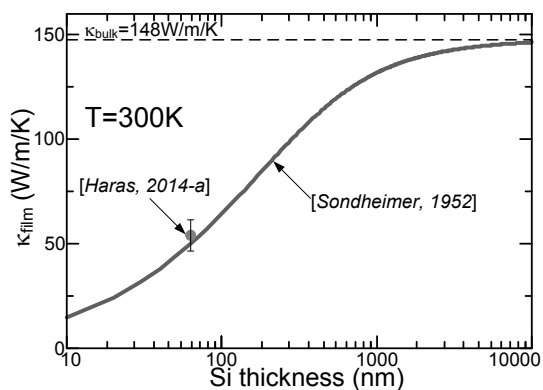


Fig. 8-8 La valeur moyenne de la  $\kappa$  mesurée dans toutes les membranes caractérisées

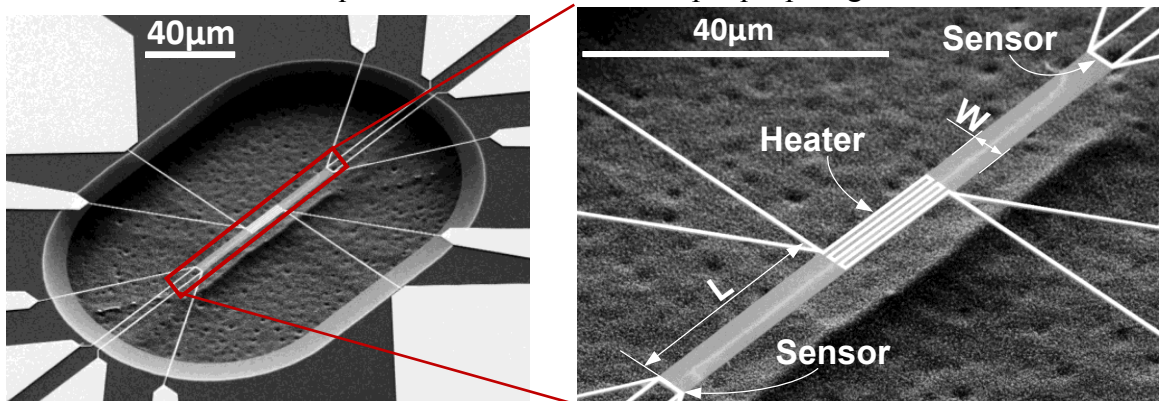
# Conclusions

Le travail effectué peut être divisé en deux parties : une partie théorique où l'évaluation de matériaux compatibles avec la technologie **CMOS** : **Silicium (Si)**, **Germanium (Ge)** and **Silicium-Germanium ( $Si_xGe_{1-x}$ )** est présentée et une partie technologique où le design, la fabrication et la caractérisation permettant la mesure de la conductivité thermique ( $\kappa$ ) dans les matériaux sous forme de couche mince est présentée. Pour synthétiser ce mémoire, les conclusions les plus importantes seront soulignées :

1. Le modèle dépendant de la température, de la composition et du dopage permet l'optimisation aux niveaux du matériau et de la topologie :
  - a. Les concentrations des dopages optimales déterminées en analysant le facteur de puissance (**PF**) sont :  $10^{18}\text{cm}^{-3}$  pour **Ge** et  $10^{19}\text{cm}^{-3}$  pour **Si** et  **$Si_xGe_{1-x}$** ,
  - b. Les études comparatives pour différentes topologies ont montré que la capacité de récupération d'énergie est dominée par  $\sigma$ . Les topologies avec la jonction *pn* court-circuité sont significativement plus performantes que les topologies avec la jonction *pn*.
  - c. La topologie latérale d'un générateur a été proposée. La topologie permet : (i) l'usage des matériaux actifs sous la forme de couches minces intégrant la réduction de  $\kappa$ , (ii) l'intégration de la flexibilité mécanique, (iii) l'adaptation topologique pour la fabrication industrielle (*la topologie planaire*) et (iv) le montage simplifié,
  - d. La densité de puissance maximale pour  $\Delta T=30\text{K}$  et la densité de dopants optimale est  $12\text{W}/\text{cm}^2$  pour **Ge**,  $7\text{W}/\text{cm}^2$  pour **Si** et  $4\text{W}/\text{cm}^2$  pour  **$Si_xGe_{1-x}$** , présentant les matériaux **CMOS** comme compétitifs vis-à-vis des matériaux thermoélectriques conventionnels.
2. Le design, la fabrication et la caractérisation d'une plateforme micrométrique pour les mesures de  $\kappa$  représente la partie technologique de ce travail :
  - a. La topologie du dispositif et les conditions de mesure simplifient et rendent la mesure plus précise,
  - b. La fabrication est effectuée sur plaque **SOI**. La couche mince de **Si** est suspendue grâce aux (i) méthodes de gravure sèche, (ii) à l'utilisation des matériaux à basse contrainte mécanique et (iii) le design permettant de distribuer la contrainte mécanique sur la surface,
  - c. Les mesures sous vide ont donné la valeur de  $\kappa=57\pm 7.5\text{W}/\text{m}/\text{K}$  pour la membrane de **Si** 68nm d'épaisseur, cette valeur est confirmée par le modèle théorique.
3. Les bonnes propriétés électriques avec la possibilité de réduction de  $\kappa$  pour les matériaux **CMOS** créeront la thermoélectricité : (i) industriellement compatible, (ii) économiquement attractive, (iii) non-polluante et (iv) simple. La quantité de pertes thermiques et les appareils électroniques en usage rendent la thermoélectricité très attractive et innovante pour la récupération d'énergie.

# Perspectives

1. Le projet, le procédé de fabrication et les mesures ouvrent la possibilité de caractériser  $\kappa$  pour :
  - a. **Si** avec différentes épaisseurs pour mettre en évidence la réduction de  $\kappa$  dans les couches ultraminces
  - b. Les couches minces de **Si<sub>x</sub>Ge<sub>1-x</sub>** pour déterminer si la réduction naturelle de  $\kappa$  peut être cumulée avec la réduction provenant des couches minces
  - c. Les mesures pour différentes épaisseurs de membranes **Si<sub>x</sub>Ge<sub>1-x</sub>** permettent de construire le modèle théorique couplant la  $\kappa$  avec l'épaisseur
2. Pour améliorer la précision de la mesure, une nouvelle topologie est proposée, les modifications majeures contiennent :
  - a. L'isolation complète entre la membrane et la plaque pour augmenter la résistance thermique entre la membrane et la plaque
  - b. La sensibilité du serpentin de détection thermique est amplifiée grâce à la suspension complète de la membrane permettant de déterminer  $\kappa$  avec plus grande précision
  - c.  $\rho_{Pt}$  du serpentin chauffant peut être déterminée en utilisant quatre pointes afin de permettre la caractérisation du  $T_H$  plus précisément
  - d. La taille des cavités est largement augmentée pour rendre la résistance thermique entre la membrane et la plaque plus grande



3. La gravure de **Si<sub>x</sub>N<sub>y</sub>** (**STEP 6**) utilise la couche mince de **SiO<sub>2</sub>** comme couche d'arrêt pendant la gravure en vapeur **HF** (**STEP 9**), ce **SiO<sub>2</sub>** peut être sous gravé, isolant thermiquement le serpentin chauffant de la membrane, pour éliminer ce problème :
  - a. **Si<sub>x</sub>N<sub>y</sub>** est déposé directement sur la couche de **SOI** et **STEP 6** n'est pas exécuté,
  - b. La détermination de  $\kappa$  du **Si** demande la mesure du  $\kappa$  pour **Si<sub>x</sub>N<sub>y</sub>**
  - c.  $\kappa$  du **Si** peut être extraite en utilisant le diviseur thermique de **Si<sub>x</sub>N<sub>y</sub>-Si**



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# Scientific production

## Journals:

1. **M. Haras**, V. Lacatena, F. Morini, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Thermoelectric energy conversion: How good can silicon be?,” *Materials Letters*, vol. 157, pp. 193–196, Oct. 2015, doi: [10.1016/j.matlet.2015.05.012](https://doi.org/10.1016/j.matlet.2015.05.012).
2. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Toward quantitative modeling of silicon phononic thermocrystals,” *Applied Physics Letters*, vol. 106, no. 11, p. 114104, Mar. 2015, doi: [10.1063/1.4915619](https://doi.org/10.1063/1.4915619).
3. **M. Haras**, V. Lacatena, F. Morini, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Fabrication of Integrated Micrometer Platform for Thermoelectric Measurements,” in *Electron Devices Meeting (IEDM), 2014 IEEE International*, San Francisco, 2014, pp. 8.5.212–8.5.215, doi: [10.1109/IEDM.2014.7047012](https://doi.org/10.1109/IEDM.2014.7047012).
4. **M. Haras**, V. Lacatena, S. Monfray, J.-F. Robillard, T. Skotnicki and E. Dubois “Unconventional Thin-Film Thermoelectric Converters: Structure, Simulation, and Comparative Study,” *Journal of Electronic Materials*, vol. 43, no. 6, pp. 2109–2114, Jun. 2014, doi: [10.1007/s11664-014-2982-z](https://doi.org/10.1007/s11664-014-2982-z).
5. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Phononic engineering of silicon using ‘dots on the fly’ e-beam lithography and plasma etching,” *Microelectronic Engineering*, vol. 121, pp. 131–134, Jun. 2014, doi: [10.1016/j.mee.2014.04.034](https://doi.org/10.1016/j.mee.2014.04.034).
6. M. Turzynski, **M. Haras**, G. Kostro and P. Musznicki “A wide-band modeling of DC-DC two-transistor flyback converter.,” in *Industrial Electronics (ISIE), 2011 IEEE International Symposium on*, 2011, pp. 113–118, doi: [10.1109/ISIE.2011.5984142](https://doi.org/10.1109/ISIE.2011.5984142).

## International conferences:

1. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki, E. Dubois, M. Massoud, P.-O. Chapuis, J.-M. Bluet and A. Scibetta “Thermal conductivity reduction in fully suspended and periodically patterned membranes measured by electro-thermal method,” presented at the 2015 (*MRS Fall Meeting*), Boston, Massachusetts, USA, November 29-December 4, 2015.
2. J.-F. Robillard, V. Lacatena, **M. Haras**, F. Morini, V. Giorgis, H. Ftouni and E. Dubois “Unconventional approaches for thermoelectric energy harvesting,” presented at the Hot nanostructures: thermal transport and radiation at the nanoscale workshop (*CECAM2015*), Mainz, Germany, September 30-October 2, 2015.
3. J.-F. Robillard, V. Lacatena, **M. Haras**, A. Scibetta, S. Monfray, T. Skotnicki and E. Dubois “Thermal conductivity of periodic nano-holes structures etched in silicon membranes,” presented at the 2015 (*E-MRS Fall Meeting*), Warsaw, Poland, September 15-18, 2015.
4. M. Massoud, V. Lacatena, **M. Haras**, P.-O. Chapuis, J.-M. Bluet, J.-F. Robillard and E. Dubois “Effective thermal conductivity of nanophononic membrane strips investigate by scanning thermal microscopy and Raman thermometry,” presented at the 15<sup>th</sup> International Conference on Phonon Scattering in Condensed Matter (*Phonons2015*), Nottingham, United Kingdom, July 12-17, 2015.
5. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Reduced Thermal Conductivity of Periodically Nanostructured Silicon: a Quantitative Molecular Dynamics Study,” presented at the 3<sup>rd</sup> International Conference on Phononic Crystals/Metamaterials, Phonon Transport and Phonon Coupling (*Phononics2015*), Paris, France, May 31–June 5, 2015.
6. **M. Haras**, V. Lacatena, F. Morini, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Fabrication of Integrated Micrometer Platform for Thermoelectric Measurements,” presented at the 60<sup>th</sup> IEEE International Electron Devices Meeting (*IEDM2014*), San Francisco, California, USA, December 15-17, 2014.
7. **M. Haras**, V. Lacatena, F. Morini, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois [*Invited*] “How good silicon for thermoelectric conversion?,” presented at the 17<sup>th</sup> International Symposium on the Physics of Semiconductors and Applications (*ISPSA2014*), Jeju, South Korea, December 7-11, 2014.
8. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Reduction of thermal conductivity in silicon thin film membranes by phononic engineering,” presented at the *Eurotherm* seminar, Lyon, France, October 15-17, 2014.

9. J.-F. Robillard, V. Lacatena, **M. Haras**, S. Monfray, T. Skotnicki and E. Dubois “Silicon Thermoelectrics: A Non-conventional Approach Based on Thin-film Phononic Engineering,” presented at the International Symposium on the CMOS Emerging Technologies Research (*CMOSETR2014*), Grenoble, France, July 6-8, 2014.
10. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois [*Invited*] “Efficient reduction of thermal conductivity in silicon using phononic-engineered membranes,” presented at the 2014 Spring Conference of the European Materials Research Society (*E-MRS Spring Meeting*), Lille, France, May 27-29, 2014.
11. **M. Haras**, V. Lacatena, S. Monfray, J.-F. Robillard, T. Skotnicki and E. Dubois “Integrated measurement platform for thermal conductivity measurements in thin-film crystalline Silicon and Silicon-Germanium,” presented at the 2014 Spring Conference of the European Materials Research Society (*E-MRS Spring Meeting*), Lille, France, May 27-29, 2014.
12. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Phononic Engineering of Silicon using ‘Dots on the fly’ e-beam lithography and plasma etching,” presented at the 39<sup>th</sup> International Conference on Micro and Nano Engineering (*MNE2013*), London, UK, September 16–19, 2013.
13. **M. Haras**, V. Lacatena, S. Monfray, J.-F. Robillard, T. Skotnicki and E. Dubois “Non-conventional thin-film thermoelectric converters: structure, simulation and comparative study,” presented at the 32<sup>nd</sup> International Conference on Thermoelectrics (*ICT2013*), Kobe, Japan, 30 June – 4 July 2013.
14. M. Turzynski, **M. Haras**, G. Kostro and P. Musznicki “A wide-band modeling of DC-DC two-transistor flyback converter,” presented at the IEEE 20<sup>th</sup> International Symposium on Industrial Electronics (*ISIE2011*), Gdańsk, Poland, June 27-30, 2011.

**National conference:**

1. V. Lacatena, **M. Haras**, J.-F. Robillard, S. Monfray, T. Skotnicki and E. Dubois “Phononic crystals patterning by e-beam lithography” dots on the fly” methodology for integration into thermoelectric energy converters” presented at the 17<sup>èmes</sup> Journées Nationales du Réseau Doctoral en Micro-Nanoélectronique, (*JNRDM2014*), Lille, France, May 26-28, 2014

**Award:**

1. 2<sup>nd</sup> prize for the best thesis at Lille Catholic University, Edition 2014



# Non-conventional thermoelectrics based on thin-film silicon technologies

Thermoelectricity converts heat into electric energy in a silent, direct, vibrationless and reliable way. In light of limited reserves in fossil fuels, increasing greenhouse effect and constantly rising worldwide demand in energy, recovering heat losses can be a solution. Good thermoelectric material integrates antagonistic properties: high crystal-like electrical ( $\sigma$ ) and low glass-like thermal ( $\kappa$ ) conductivities. Conventional thermoelectricity uses materials that are harmful, complex, expensive and incompatible with mainstream fabrication technologies *e.g.* **CMOS** making thermoelectricity unpopular.

In contrast, **CMOS** materials, namely **Silicon (Si)**, **Germanium (Ge)** and **Silicon-Germanium ( $\text{Si}_x\text{Ge}_{1-x}$ )**, are simple, easy-to-get, cheap and industrially compatible offering a high electrical conductivity ( $\sigma$ ). However, their usage in thermoelectricity is hindered due to a prohibitive thermal conductivity ( $\kappa$ ). Recent progress in nano- and micro-fabrication opened new possibilities to reduce  $\kappa$  with minor impact on  $\sigma$ . This opportunity enables fabrication of **CMOS** compatible **ThermoElectric Generators (TEGs)** enabling massive production and cost reduction which can popularize **TEGs** on the market.

Our modelling approach place **Si**, **Ge** and  **$\text{Si}_x\text{Ge}_{1-x}$**  in a competitive position compared with conventional thermoelectrics providing that their high bulk  $\kappa$  can be substantially reduced. Within the framework of this thesis, a 3-fold size induced  $\kappa$  reduction in **Si** is experimentally obtained based on a micrometer measurement platform that has been designed, fabricated and characterized in this work.

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Keywords: energy harvesting, **SOI**, **CMOS**, semiconductor modelling, micro-fabrication, material engineering

## Thermoélectricité non-conventionnelle basée sur les technologies silicium en films minces

La thermoélectricité convertit fidèlement l'énergie thermique en énergie électrique de manière directe, silencieusement et sans vibrations. Dans le contexte des réserves limitées en énergies fossiles, de l'effet de serre et de besoin énergétiques mondiaux en hausse, la récupération d'énergie thermique dissipée peut être une solution d'appoint. Un bon matériau thermoélectrique intègre des propriétés antagonistes : haute conductivité électrique ( $\sigma$ ) et faible conductivité thermique ( $\kappa$ ). La thermoélectricité conventionnelle utilise des matériaux nocifs, complexes, coûteux et incompatibles avec des techniques de fabrication massive *ex.* **CMOS** rendant la thermoélectricité peu populaire sur le marché.

En revanche, les matériaux **CMOS**, à savoir le silicium (**Si**), le germanium (**Ge**) et le silicium-germanium ( **$\text{Si}_x\text{Ge}_{1-x}$** ), sont simples, facilement approvisionnables et industriellement compatibles. Ils offrent une excellente conductivité électrique ( $\sigma$ ) mais leur utilisation dans la thermoélectricité est limitée par une conductivité thermique ( $\kappa$ ) trop élevée. Les progrès récents dans les domaines de micro et nano-fabrication permettent de réduire  $\kappa$  sans affecter  $\sigma$ . Cela permet de fabriquer des générateurs thermoélectriques (**TEG**) compatibles **CMOS**, tout en gardant une production massive réduisant le coût.

Les simulations présentées placent **Si**, **Ge** et  **$\text{Si}_x\text{Ge}_{1-x}$**  dans une position compétitive par rapport aux matériaux thermoélectriques conventionnels, à condition de réduire substantiellement  $\kappa$ . Une réduction de la conductivité thermique d'un facteur 3 a été expérimentalement démontrée dans des membranes de **Si** intégrées au sein d'une plateforme micrométrique conçue, fabriquée et caractérisée dans le cadre de cette thèse.

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Mots-clés : récupération d'énergie, SOI, CMOS, modélisation des semi-conducteurs, micro-fabrication, ingénierie des matériaux