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Electronic Properties of Coupled Semiconductor Nanocrystals and Carbon Nanotubes

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Electronic Properties of Coupled Semiconductor Nanocrystals and Carbon Nanotubes

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To my mother

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Abstract

We study the electronic properties of coupled semiconductor nanocrystals and carbon nanotubes. We report measurements of single electron transfers between single CdSe colloidal nanocrystal coupled to a carbon nanotube field effect transistor at room temperature in ambient conditions. The measurements consist of nanotube current level monitoring as a function of time for fixed gate voltage. We observe a sequence of *high* - *low* currents (random telegraph signal) on time scales up to several seconds with *ms* sampling time. We attribute the two level current fluctuations to the transfer of single electron onto the nanocrystal. The probability of the occupation time τ at the *high* or *low* current state follows a power law of the form $P(\tau) \sim \tau^{-\alpha}$ where exponent α lies between 1.5 and 4 (typically close to 2.8). The observation suggests that the two-level current switching is similar to the fluorescence intermittency (optical blinking) observed in individual quantum dots. The spectroscopic analysis of the devices based on coupled semiconductor nanocrystals and carbon nanotubes is consistent with the charging of nanocrystal defect states with a charging energy of E_c ~ 200 meV. The approach developed here enables to probe the trap state dynamics in quantum dots in ambient air and room temperature from a purely electrical approach, and therefore to better understand the physics at hand in (opto)electronic devices based on quantum dots.

Résumé

Ce travail de thèse décrit les propriétés électroniques de nanodispositifs couplés entre transistors à nanotubes de carbone (CNTFETs) et nanocristaux semiconducteurs colloïdaux CdSe/ZnS individuels en régime de détection de charge unique à température ambiante. Les transferts de charges élémentaires entre nanotubes et nanocristaux sont mis en évidence par les fluctuations temporelles du courant des transistors à tension de grille fixée, et font apparaître un signal à deux niveaux (bruit télégraphique ou RTS), observé sur des échelles de temps entre 1s et 0.1 ms. Les temps d'occupation τ des niveaux de courant suivent une loi de puissance $P(\tau) \sim \tau^{-\alpha}$ où l'exposant α varie entre 1.5 et 4 (typiquement proche de 2.8). Cette observation suggère que les fluctuations de charges observées sont à la base des phénomènes de "clignotement optique" des nanocristaux colloïdaux étudiés. L'analyse spectroscopique des dispositifs permet d'attribuer ce clignotement à des pièges dans la bande interdite des nanocristaux, avec une énergie de chargement E_c de l'ordre de 200 meV. L'approche présentée dans ce travail peut être étendue à des mesures électro-optiques, et donc permettre une meilleure compréhension des phénomènes physiques contrôlant les propriétés optoélectroniques de nanodispositifs à base de nanocristaux semiconducteurs.

Introduction

This Ph.D. thesis was completed under the joint doctorate according to cotutelle agreement between Université des Sciences et Technologies de Lille (USTL) and Faculty of Physics, Warsaw University of Technology in Poland (WUT).

The aim of this work was to make use of the unique carbon nanotubes (CNTs) properties in single electron detection performed during the measurements of electronic properties of single quantum dots (QDs). The aim of the work was divided between two Universities. First part was realized at the USTL in the Institute d'Electronique, de Microélectronique et de Nanotechnologie, where the nanodevices based on carbon nanotubes and quantum dots were fabricated. The second part was realized at WUT, where the devices were characterized. Both aims were achieved successfully and further studies on single electron transfer between single quantum dots and carbon nanotube based transistor was realized.

This manuscript contains four chapters. The first chapter provides a general introduction to the theory of carbon nanotube field effect transistors (CNTFETs), with the description of fundamental properties of CNTs, analysis of the switching mechanism and characteristics of single-CNTFETs and efforts towards device integration. The second chapter is an introduction to the theory of semiconductor QDs. Its first part is enclosed with a short bibliography on quantum confinement in semiconductors, the QD synthesis, and description of core-shell QDs. Its second part reports about the confocal luminescence experiments and the electrical measurements revealing optical blinking of semiconductor QDs, a two-state system intermittency, in which the light emission from a QD is switched on and off by the fluctuation of the charge occupation of a single electronic state. Section 2.3 provides a short state of art on the electronic properties of devices coupling QDs and CNTs.

A methodology of device preparation and characterization is introduced in Chapter 3. Essentially, a nanodevice is composed of a single CNT coupled to a QD under investigation. Such a hybrid structure allows to manipulate single electrons in a nanoparticle in a controllable way. Finally, Chapter 4 contains a description of the experiments made during this PhD, followed by discussion and conclusions.

Contents

Chapter 1

Introduction to carbon nanotube field effect transistors

The field of the electronics has undergone in the last decades great progress with many benefits in the field of computing or communications, which affect every aspect of our modern lives. Advanced lithography instruments provide the ability to create incessantly smaller electronic devices. One of the finest examples of miniaturized devices is silicon-based field effect transistors (FETs), which have led to denser and faster integrated circuits.[1] However, fundamental scientific and technological limitations will not enable to build better performing silicon devices below a certain size. Thus, researchers have taken considerable efforts to develop alternative device technologies based on low nanomaterials with low dimensionalities such as, for example, single-walled carbon nanotubes (SWCNTs) acting as one-dimensional semiconducting or metallic channels with adaptable electrical-transport properties. Carbon nanotube field effect transistors (CNTFETs) made from semiconducting SWCNTs have been demonstrated with nearly optimal and highly tunable properties.

The next paragraphs of this introduction chapter contain a description of fundamental properties of carbon nanotubes (CNTs), the analysis of their switching mechanism, the characteristics of single-CNTFETs and the efforts made so far towards device integration. The following description is not exhaustive and it is only a guide to help to understand the final chapters of this work. For more detailed information the reader may refer to following authors: Tobias Dürkop form the University of Maryland in his review on carbon nanotubes high mobility[2] and Phaedon Avouris from IBM Research Division in publications on nanotube-based electronics circuits.[3,4,5]

1.1 Carbon nanotubes

The first observation of CNTs is attributed to Sumio Iijima. In 1991, the Japanese scientist has published the first high resolution TEM images of "Helical microtubules of graphitic carbon",[6] and thus he introduced carbon nanotubes to the scientific world. Since then, carbon nanotubes have attracted great interest as they offer unique properties with a wide range of potential applications.

1.1.1 Structural and electronic properties

Carbon nanotubes are members of the fullerene structural families of carbon (see Figure 1.1). They owe their name due to their long and hollow structure (a tube) formed from single layer(s) of hexagonally arranged carbon atoms (graphene). The structure of these nanomaterials is quasi-dimensional. The length-to-diameter ratio of CNTs could be very high, even up to 132 000 000:1,[7] which is much larger than for any other known material.

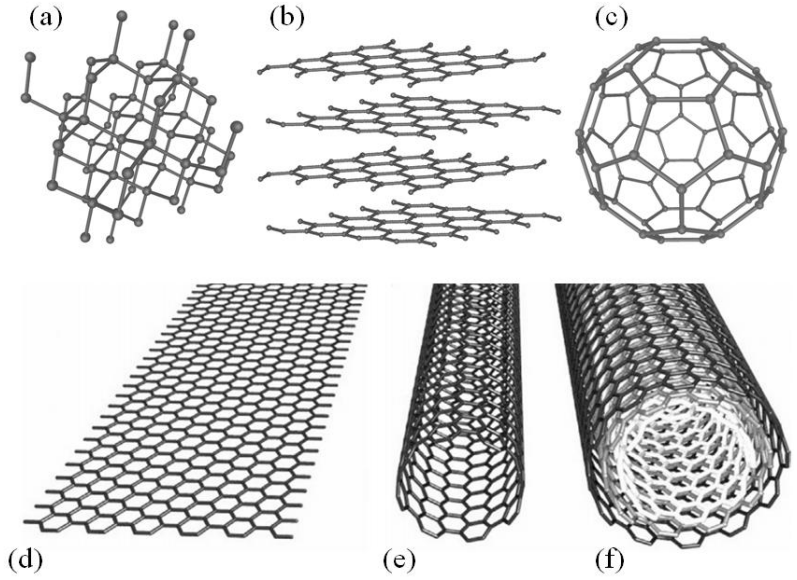

Figure 1.1 *Fullerene structural families. (a-f) Crystal structure of a few carbon allotropes: (a) Diamond, (b) Graphite, (c) Fullerene - C_{60}, (d) Graphene, (e) SWCNT, (f) multi-walled CNT. Adapted from*[8,9]

From a structural point of view, carbon nanotubes either correspond to single-walled nanotubes (SWCNTs) and multi-walled nanotubes (MWCNTs). The first one is, as described above, a tube with just one wall (layer). MWCNTs consist of multiple concentric tubes, as shown in Figure 1f. The distance between each concentric layer in MWCNTs is similar to the distance between each graphene layer in highly oriented pyrolitic graphite, which is around $0.34\,nm$. Because of the complexity of their structure (mostly leading to a metallic

behaviour) and the fact that MWCNTs often appear with structural defects, SWNTs have much better performance and are more suitable for transistor applications.[10,11,12] Therefore, in this work only single-walled carbon nanotubes have been considered, and the abbreviation of CNTs will only refer to single walled carbon nanotubes throughout the rest of the manuscript.

The best way to describe the structure of a CNT is to start with a single layer of graphene. Figure 1.2a presents the schematics of the hexagonal planar lattice with an indication of how to cut a narrow strip out from the graphene sheet in a given direction in order to roll it up to the form of a cylinder. One of the most striking property of CNTs is that the structure of CNTs (including their metallic or semiconducting character) depends on this chosen direction. The vector defining the CNT circumference is given by equation: $\vec{C} = n\vec{a}_1 + m\vec{a}_2$, where $\vec{a}_1$ and $\vec{a}_2$ are the unit vectors of the hexagonal planar lattice and the numbers m and n are called the chirality indexes. Note that m and n precisely determine and describe the structure. For example, CNTs with indices $m = n$ are called armchair, those with $n = 0$ zigzag and other tubes are chiral (see Figure 1.2b). The chirality indexes can used to determine the diameter of a CNT from the following equation:

$$d_{CNT} = \frac{\sqrt{3}a_{C-C}\sqrt{m^2+nm+n^2}}{\pi}, \tag{1.1}$$

where $a_{C-C} = 1.421$ Å is the nearest neighbor distance between carbon atoms.[13]

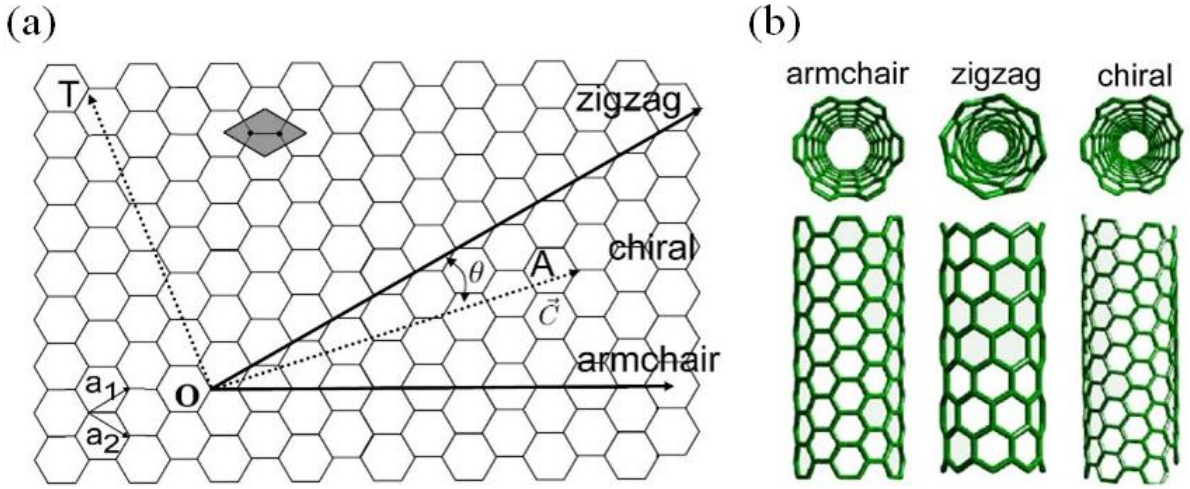

Figure 1.2 S*tructure of CNTs. (a) Hexagonal structure of graphene with its unit cell (gray rhombus) and base vectors. The* $\vec{C}$ *vector defines the circumference of the CNT and* $\theta = \arctan\left(\frac{\sqrt{3}m}{m+2n}\right)$ *represents its chiral angle. The solid lines indicate the circumferences of a zigzag and an armchair CNT, and the dashed lines of a chiral CNT (vectors OT and OA). (b) Examples of the three types of CNTs. Adapted from*[14]

The electronic structure of carbon nanotubes can be obtained from the electronic structure of graphene. It turns out that by using a tight binding scheme, the variation of the energy as a function of the wave vector can be describe by the following formula:

$$E(\vec{k}) = \pm\gamma_0\sqrt{1 + 4cos\left(k_\perp \frac{\sqrt{3}a_{C-C}}{2}\right)cos\left(k_\parallel \frac{\sqrt{3}a_{C-C}}{2}\right) + 4cos^2\left(k_\perp \frac{\sqrt{3}a_{C-C}}{2}\right)}, \qquad (1.2)$$

where $\gamma_0 \sim 3\ eV$ is the bond energy between carbon atoms. A positive sign in the equation 1.2 refers to the conduction band, while a negative sign refers to the valence band. The bands are in contact when $E = 0$ and the contact points are located at the vertices of the hexagons forming the reciprocal lattice. The way to determine the band structure of a CNT is to use periodic boundary conditions along the nanotube edges, starting from the graphene band structure. The new wave vector has two components, a longitudinal one and perpendicular one (with respect to the circumference of the nanotube):

$$\vec{k} = A\overrightarrow{k_\parallel} + B\overrightarrow{k_\perp}. \qquad (1.3)$$

From the fact that the CNT length is much bigger than its diameter it can be assumed that the wave vector along the nanotube axis can take random real values. In contrary, in a perpendicular axis direction, the wave vector is quantized. Compared to the reciprocal graphene lattice, the allowed states lay on parallel lines along the $\overrightarrow{k_\parallel}$ direction separated by value of $2/d$ (see Figure 1.3).

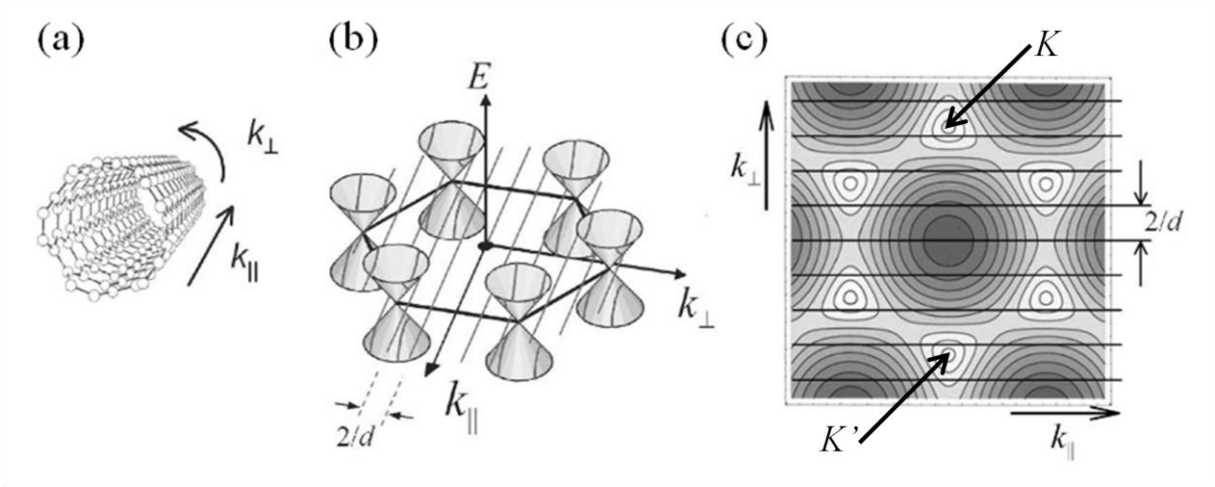

Figure 1.3 *Electronic properties of CNTs. (a) Diagram of a CNT with marked directions of $k_\perp$ and $k_\parallel$ wave vectors. (b) Band structure of graphene determined by equation 1.2 in a conical representation. The wave vectors $k_\parallel$ are indicated by lines, separated by $2/d$. (c) The $E(\vec{k})$ conduction band mapped to the first Brillouin zone with allowed $k_\parallel$ indicated by horizontal lines and marked K points. Adapted from*[8]

The CNT band structure is formed by the intersection of the $\overrightarrow{k_\perp}$ values and the $E(\vec{k})$ surface. If at least one allowed $\overrightarrow{k_\perp}$ line crosses the K or K' points in the first Brillouin zone it indicates that the nanotube is metallic (Figure 1.4a). In other cases an energy gap appears in the band structure and the carbon nanotube is semiconducting (Figure 1.4b). It can be proven that if the chirality indices meet the condition $n - m = 3l$, where l is the integer, the $\overrightarrow{k_\perp}$ line crosses the K or K' point. In case when $n - m = 3l \pm 1$, the CNT is semiconducting.[15]

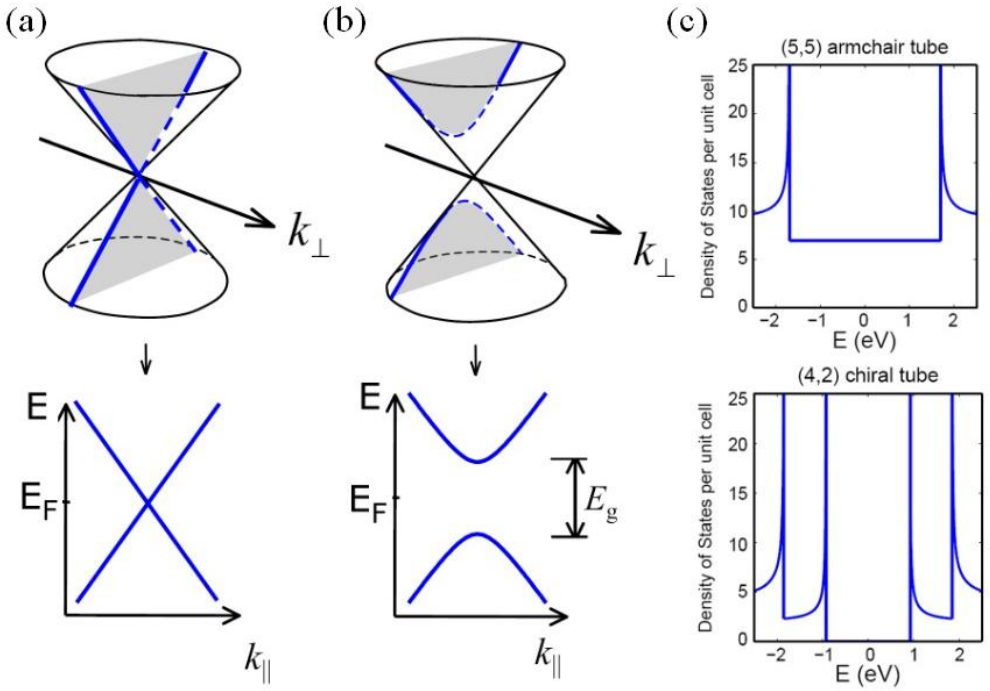

Figure 1.4 *Band structure of CNTs. Conical band structure with allowed wave vector of (a) metallic and (b) semiconducting CNT. (c) Density of states for a (5,5) metallic and a (4,2) semiconducting CNT. Adapted from*[8]

The density of states (DOS) is another important feature affecting electronic properties of carbon nanotubes. Figure 1.4c presents an example of the density of states for (5,5) metallic and (4,2) semiconducting CNT. One can observe the sharp peaks called van Hove singularities which are characteristic of 1D systems.[16] With the parabolic band approximation, the DOS function is $\sim 1/\sqrt{E}$. For metallic nanotubes, the DOS near the Fermi level is approximately constant and for semiconducting nanotubes, the DOS is equal to zero, forming a band gap. It should be noted that van Hove singularities exist for the energy for which the corresponding subband has the minimum. In the case of CNTs with similar diameters, chiral nanotubes have more peaks than the armchair. The local density of states can be determined experimentally by STM spectroscopy.[17]

1.1.2 Carbon nanotube synthesis and dispersion

The three main and most common methods used in the synthesis of CNTs are: arc discharge, laser ablation and chemical vapor deposition (CVD).

The first MWNTs have been noticed in the material created after an arc discharge experiment.[6] An electrical discharge can be induced by applying a high voltage between two graphite rods, which creates a plasma of carbon molecules. MWCNTs and SWNTs can be formed by this process if the rods contain metal catalyst such as nickel, iron or cobalt.[18] In the laser ablation method a high energy pulsed laser is used to irradiate a carbon target containing Ni and Co instead of an electrical discharge to create the plasma for the CNT growth.[19] These two methods are often used to produce CNTs, however with the drawback that they form bundles of CNTs with mixed undesired structures formed by carbon or metal particles.

Nowadays, the production of CNTs is mostly done using CVD methods. The main advantage of CVD, with respect to our work, is that it gives the possibility to grow CNTs directly at a specific position on a given substrate, which is very helpful in the fabrication of devices based on single CNTs. A disadvantage of CVD will be of course that this technique produces both semiconducting and (in our work, unwanted) metallic nanotubes, which need to be sorted out by electrical characterization. In practice, during the CVD process, a substrate is prepared from a layer of metal catalyst nanoparticles, generally Ni, Co,[20] Fe, or a combination of these elements.[21] The diameters of CNTs grown from such catalysts depend to the size of the original metal particles, which can be controlled *e.g.* when starting from patterned metallic layers. The substrate is preheated to around $700°C$, and the growth of nanotubes is done in a reactor with a flow of two gases: a process gas like ammonia, nitrogen or hydrogen and a gas containing the carbon element like acetylene, ethylene or methane. The nanotubes grow from the sites of metal catalysts, where the carbon-containing gas is dissociated. The metal catalyst particles are located after growth either at the apex of the grown CNTs, or at the CNT bottom.[22] In our work we used CNTs from a growth process via a catalytic CVD technique using pure methane (CH_4) as the carbon source.[23] The procedure of catalyst growth is described in chapter 3 (see **3.1.2 CNTs deposition and growth** section).

Unfortunately, a complete control of the nanotube growth process is not possible using the above mentioned synthesis methods. Consequently, the growth of CNTs is more or less non-selective with respect to chirality and diameter distribution.[24] This is a major issue, as the use of nanotubes in various advanced electronic applications requires carbon nanotubes with specific diameters and chirality, and, in particular, in our case, to use only semiconducting

rather than metallic nanotubes. A lot of efforts have been spent on the development of more selective methods for CNTs synthesis and also on the development of dispersion and sorting techniques. The Hersam Research Group at Northwestern University has developed a technology known as density gradient ultracentrifugation (DGU)[25] for separating carbon nanotubes by their optical and electronic properties. A company (NanoIntegris) was established to commercialize this technology.[26] The DGU process can be described as follows: the unsorted CNT material is placed in an aqueous solution containing a combination of surfactants (surface active reagents). Surfactants adhere selectively to CNTs of different species. This process helps to enhance the effective density difference between them (Figure 1.5a). The obtained solution is then centrifuged under a high centrifugal field. The CNTs covered with surfactants migrate during the spinning process to their isopycnic (same density) point in the density gradient. Once semiconducting CNTs are spatially separated from the metallic ones, they can be isolated using established fractionation techniques (Figure 1.5b). The collected semiconducting CNTs can then be 'dried' in the form of a powder, which can be later be used in the same way as the nanotube powder obtained from arc-discharge and laser ablation methods, by a further dispersion into organic solvents.

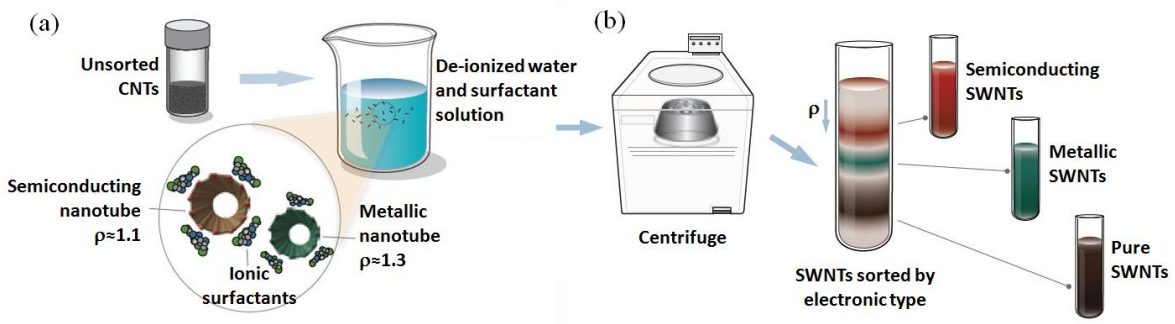

Figure 1.5 *Scheme of processing flow for the NanoIntegris technology for separating CNTs by their optical and electronic properties. (a) CNTs dispersed in aqueous solution using a combination of surfactants. (b) Separated CNTs after centrifugation process. Adapted from*[26]

To do this, the most commonly used method to disperse CNTs is ultrasonication in an organic solvent.[27,28] Bahr et al.[29] described the solubility of small diameter SWNTs in organic solvents including 1,2-Dichlorobenzene. It was suggested that impurities (amorphous carbon and metal catalysts) take part in the dispersion of SWNTs. The nanotube purification process may in a reversed way modify their solubility properties. Koshio et al.[30] reported that the ultrasonication of SWNTs in a monochlorobenzene solution of poly(methyl methacrylate) followed by a filtration step is an effective way to purify SWNTs. It was also found that SWNTs react chemically with the organic liquids during ultrasonication. Niyogi et al. studied

the nature of SWNT-organic solvent interaction that is responsible for the stabilization of ultrasonicated dispersions.[27]

1.2 Transistors based on carbon nanotubes

Since the first observation of carbon nanotubes in 1991, scientists have taken a lot of effort to use this unique material in electronics. This mission is particularly important, because further scaling of classical silicon based field effect transistors will be ultimately limited by top-down fabrication technology and silicon intrinsic electronic performances. Using CNTs with diameters of ~1 nm instead of silicon-based field effect devices would reduce the dimensions of transistors and thus increase the packing of integrated circuits.

One of the first field effect transistors with a single semiconducting CNT channel (CNTFET) was introduced in 1998 by Tans *et al.* at Delft University of Technology.[31] The nanotube was placed on top of an oxidized silicon substrate with predefined platinum contacts. In such a device geometry, the current flow through the nanotube, and the bottom side of the sample works as an electrostatic gate that can be used for current modulation. The performance of the first CNTFETs was far from ideal, with a large contact resistance, low drain current and low conductance. Many techniques were introduced in order to improve their electrical characteristics. For example: the use of low work-function metal contact as compared to CNTs work function;[32] the annealing of contacts in order to alter the nanotube–metal bond; the reduction of the thickness of the dielectric layer; the use of new transistor geometries. Figure 1.6 shows schematically three different CNTFET geometries: back gate geometries with CNT deposited on top of the metal contacts (a),[33] CNT covered with metal contacts (b)[34] and a top gated CNTFET (c).[35]

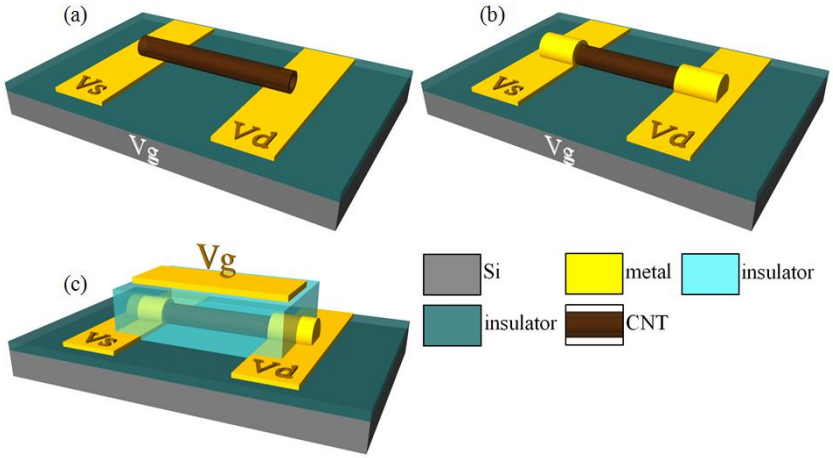

Figure 1.6 *Different geometries of CNTFETs. Back gate geometries with (a) CNT deposited on top of the metal contacts and (b) CNT covered with metal contacts; (c) FET geometry with a CNT covered with metal contacts together with a top gate modulation. Adapted from*[33,34,35]

1.2.1 Electrical switching of carbon nanotube field effect transistors

Nowadays, field effect transistors (FETs) are based on silicon, and operate by switching between on and off states. Semiconducting CNTs can also be switched on and off and are hence suitable materials for FET applications.4 Two models were developed to explain the operation of CNTFETs: a classical MOSFET model and a Schottky barrier field effect transistor model.[36] In the first model for the p-type CNTFET, the inversion layer is induced by applying negative gate potential (V_g), and the potential difference between the source (S) and drain (D) electrodes causes the current flow – the transistor is switched on. The V_g adjustment influences the carrier (holes) concentration and thereby the transistor resistance. The transistor is switched off when the depletion layer is formed upon application of an appropriate V_g. In the case of a CNTFET with Schottky barriers, the transistor operation is based on the modulation of the potential barriers at the metal-nanotube junction. Since the CNT is connected from one side to the source electrode and at the other side to the drain, one have to consider two Schottky barriers. The Schottky barrier height depends on the CNT and connecting metal work functions respectively, on the CNT band-gap, and on chemical bonds which can be formed at the tube-metal interface. The transistor current flow is blocked when the barrier at the junction is high. In the case of a p-type CNTFET, by applying a negative V_g, the barrier width is reduced and carriers (holes) can tunnel through it, or if they have sufficient energy - greater than the height of the barrier - they can flow from metal to the

nanotube. Figure 1.7 presents the case of an ambipolar transistor, for which Schottky barriers becomes thin enough to allow the injection of either electrons or holes (depending on the sign of the back-gate bias), or of both carriers at the same time.[37,38,39] The insets of Figure 1.7 show the influence of V_g on the character of carriers.

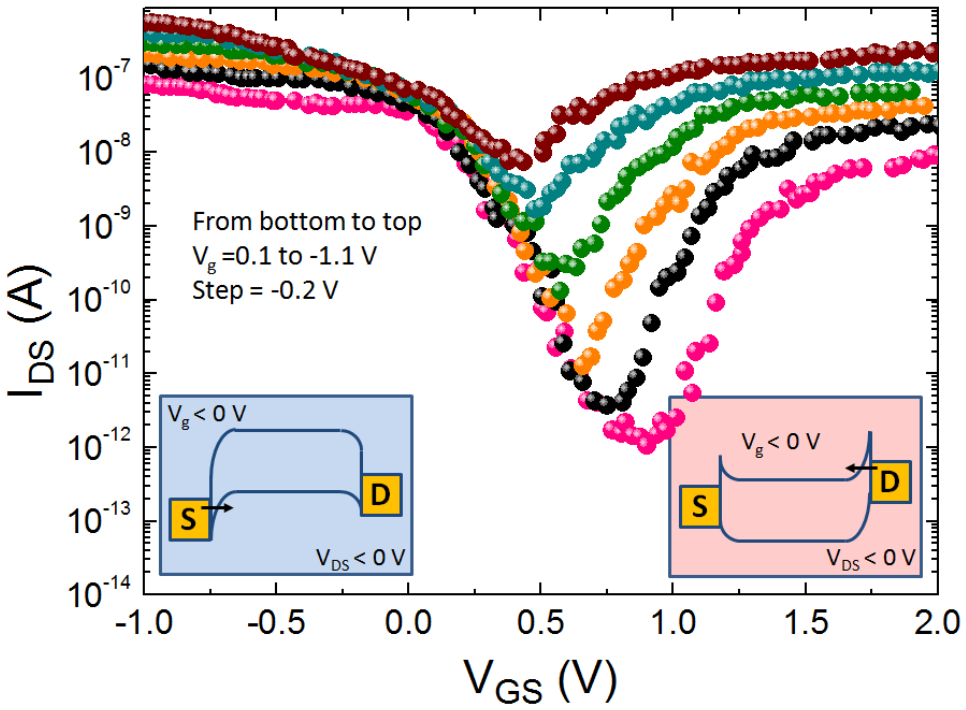

Figure 1.7 *Transport characteristics of an ambipolar CNTFET. Left inset: schematics of the band structure of a p-type CNTFET* ($V_g < 0$). *Right inset: schematic of the band structure of a n-type CNTFET* ($V_g > 0$). *Adapted from*[4]

The CNTFET characteristics, for both the on and off states, depends on Schottky barriers.4 The inverse sub-threshold slope defined as $Sl = \left(d \log_{10} I/dV_g\right)^{-1}$, and is a key parameter to understand this regime. For traditional silicon based MOSFETs with ohmic contacts, at room temperature conditions, the slope is limited by thermionic emission and equals $Sl \approx k_B T/q$, *i.e.* around $60\, meV$ per decade. In case of transistor with Schottky barriers, with oxide thickness less than $10\, nm$, the transport dominates and Sl is much higher, $\sim 100 - 150\, meV$ per decade. The ratio between the on and off currents is also an important parameter for transistors since in logic applications the I_{on}/I_{off} ratio should be greater than 10^4 . Unipolar CNTFETs can exhibit I_{on}/I_{off} ratios between $10^5 - 10^7$.

1.2.2 Electronic transport in carbon nanotube field effect transistors

Scattering on structural defects and lattice vibrations strongly affects the electronic transport in CNTs.4 In a one dimensional (1D) object, only forward and backward carrier motion is allowed. Also what needs to be considered is the interaction between three dimensional (3D) metal electrodes and the CNT.[40,41] The electron confinement in the CNT leads to a discrete contact resistance R_Q. For instance, in the case of metallic CNT one finds $R_Q = \frac{h}{2*2e^2} = 6.45\ \mathrm{k\Omega}$, where the factor 2 in the denominator corresponds to the degeneracy of the (two) bands that carry the current through the nanotube.

The contact resistance can also stem from the resistance due to the presence of Schottky barriers at metal–CNT junction (see previous paragraph), and to parasitic resistance effects due to non-ideal contacts. If the transport in the CNT is ballistic, by definition no carrier scattering and energy dissipation takes place in the CNT, which leads, ultimately to a minimum resistance value equal to R_Q. The parameters which determine if a CNT is a ballistic conductor are the nanotube length ($\leq 100\ nm$), the lack of structural defects, the temperature and the amplitude of the CNT channel electrical bias.

The CNT intrinsic (quantum) capacitance C_Q is related to its density of states. If the nanotube is part of a transistor, it also exhibits electrostatic capacitances which arise from its coupling to surrounding conductors and depend on the device geometry and dielectric structure. In a planar MOSFET, the capacitance C_G due to the electrostatic coupling with the gate scales as $C_G \approx 1/t_{ins}$, where t_{ins} is the thickness of the gate insulator. In the case of a FET based on a single CNT, the device geometry (cylinder-plane capacitance) leads to a weaker dependency of C_G with respect to the thickness of the gate insulator $C_G \approx 1/ln(t_{ins})$. The series capacitance (C_{total}) between C_Q and C_G can then be derived from equation: $1/C_{total} = 1/C_G + 1/C_Q$, and therefore the smaller capacitance dominates (usually C_G).

The transport properties of CNTs are determined by inelastic scattering since elastic scattering in CNTs is weak. For semiconducting CNTs, only low-energy acoustic phonons can efficiently scatter the electrons at low excitation (i.e. temperature and bias), and therefore the temperature dependence of the carrier mobility is inversed at low temperature.[42,43] Due to the one-dimensional band-structure, only a fraction of phonons can participate in the scattering close to the zone center and zone boundaries. Therefore, even at room temperature, in CNTs the low-field mobility is very high.[44] The electron–acoustic–phonon coupling in

CNTs is very weak and the optical phonon energy is large ($\sim 200\, meV$), that is why the carrier mobility of nanotubes is high.[45]

The carrier scattering by the radial breathing mode (RBM) is important in the low bias regime. The energy of RBM phonons is inversely proportional to the nanotube diameter[46] and comparable to the thermal energy of electrons in CNTs with diameters $d_{CNT} = 1.5 - 2.0\, nm$. Electrons can be accelerated up to the RBM energy thermally and/or by applying source-drain bias of a few $V cm^{-1}$.

The van Hove singularities in the CNTs density of states are finally also responsible for the non-monotonic dependence of the mobility with respect to band filling.[42,44,47] By applying the gate potential the band gets filled so the mobility increases because of the reduction of available final (scattered) states. The mobility is then again lowered down when an additional scattering channel opens once the Fermi level reaches a higher-energy 1D subband. The carrier mobility in CNT depends on the diameter quadratically because of the inverse diameter dependence of the effective mass and of the amplitude of the electron–phonon coupling.[42]

In a CNT, the optical phonons contract and elongate the C–C bond length and lead to a strong modulation of the electronic structure which explains why the optical phonon scattering is very strong in this material. The energy of electrons must be larger than the optical phonon energy to emit an optical phonon. These scattering processes were observed first in metallic nanotubes[48,49,50] and later in semiconducting nanotubes.[51] In metallic CNTs, the observed current was saturating at about $25\, \mu A$ because of the short optical phonon mean-free path, of the order of $10 - 20\, nm$, whereas in semiconducting CNTs, a velocity saturation was observed[51] in agreement with earlier theoretical predictions. [51,52]

1.2.3 Performance of carbon nanotube field effect transistors

Here, a short discussion about the performance of CNTFETs is given by raising a question whether CNTFETs can replace silicon MOSFETs with respect to the ITRS (International Technology Roadmap for Semiconductors) roadmap.[53] In 2002, Wind *et al.*[54] proposed a comparison between top gated CNTFETs and two state-of-the-art silicon MOSFETs. The first type is a 15 nm gate length MOSFET built on bulk Si reported by Yu et al.,[55] and the second - a 50 nm gate length device reported by Chau et al.,[56] built using silicon-on-insulator (SOI) technology. The table 1.1 presents the comparison of transistor performances.

	p-type CNTFET	Si p-type MOSFET Yu et al.	Si p-type MOSFET Chau et al.
Gate length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
$V_{th}(V)$	-0.5	~(-0.1)	~(-0.2)
$I_{on}(\mu A/\mu m)$ $(V_{DS} = V_G - V_t \approx -1V)$	2100	265	650
$I_{off}(nA/\mu m)$	150	< 500	9
Subthreshold slope (mV/dec)	130	~100	70
Transconductance $(\mu S/\mu m)$	2321	975	650

Table 1.1 *Performance comparison of field effect transistors: a 260 nm long top gate p-type CNTFET, a 15 nm bulk Si p-type MOSFET (Yu et al.), and a 50 nm SOI p-type MOSFET (Chau et al.). Adapted from*[54]

The top gate CNTFET prepared by Wind *et al.* proved to be capable of approximately three to four times higher drive current per unit (I_{on}~$2100\ \mu A/\mu m$) width than the Si p-type MOSFETs at a gate overdrive around 1 V, with approximately two to four times higher transconductance (g_m~$2321\ \mu S/\mu m$). The comparison is especially impressive since both the channel length and gate oxide thicknesses are significantly larger for the CNFET than for the silicon devices. Wind *et al.* assumed further progress can be made in CNTFET device performance via reductions in gate dielectric thickness and/or higher dielectric constant materials, along with reductions in gate length. In addition, a high $g_m$value directly increases the cutoff frequency ($f_{cutoff} = g_m/2\pi C_G$). The predicted values of f_{cutoff} for CNTFETs are of the order of THz[57] while for MOSFETs it is around 180 GHz.[58] Regarding the state of the art, in 2007, Louarn et al.[59] presented direct measured $30\ GHz$ cutoff frequency for a nanotube transistor and in year 2008, Zhong et al.[60] present a terahertz detection in the time domain using a CNTFET.

1.3 Nonvolatile memories based on carbon nanotubes

The current flowing through a CNT can be gated by single electrons, which is the starting point in making transistors with ultra-low power consumption. Also the perspective is to use individual electrons spin degree of freedom to make quantum bits for use in quantum computers. Further, one of the many CNT applications related with charge sensing and

controlling the CNT device environment is memory device. The aims at developing non-volatile memories would be their low power character, as well as a high-frequency operation. At this point in the development of CNT-based applications, this paragraph is devoted to memories based on electrical properties of CNTs.

Flash memory (developed from EEPROM - Electrically Erasable Programmable Read Only Memory) is a type of nonvolatile memory that can be electrically erased and reprogrammed. The information in flash memory devices is stored using a network of transistors called cells. Each cell consists of a control gate and a floating gate separated by a thin layer of an insulating oxide. When a voltage is applied to the cell, electrons build up as negative electric charge in the floating gate enabling to hold one bit of information.

The pioneering work on logic circuits composed of single-nanotube field-effect transistors was done by A. Bachtold et al.[61] The group was studying the nonconventional screening of charge along the one-dimensional nanotubes.

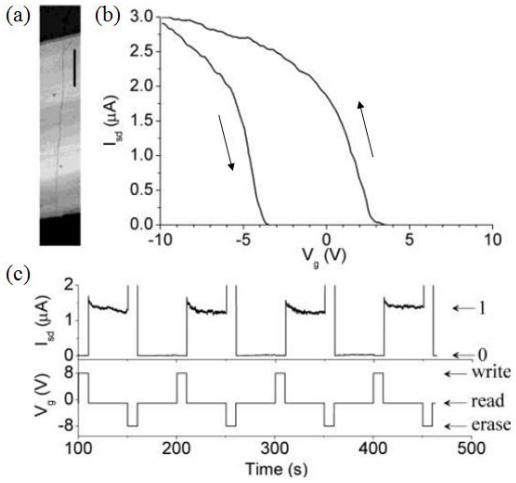

Figure 1.8 *(a) AFM image of CNTFET, scale bar is 1 μm. (b) Transfer characteristic of the device measured at room temperature. The arrows are indicating the gate voltage sweep direction and a pronounced hysteresis is observed. (c) Four read/write cycles of the CNT memory. The memory state was read at -1 V, and written with pulses of ±8 V. Adapted from*[62]

M. S. Fuhrer et al.[62] presented a non-volatile memory based on semiconductor SWNT with diameter ~ 2.7 nm and length ~ 4.8 μm (Figure 1.8). In this cell, charges are stored by application of a few volts across the silicon oxide between the nanotube and the silicon substrate back-gate. The charge is then detected by threshold shift of the CNTFET. Discrete configurations of charges corresponding to rearrangement of a single or few electrons are then detected, as a result of the high mobility of the nanotube transistor.

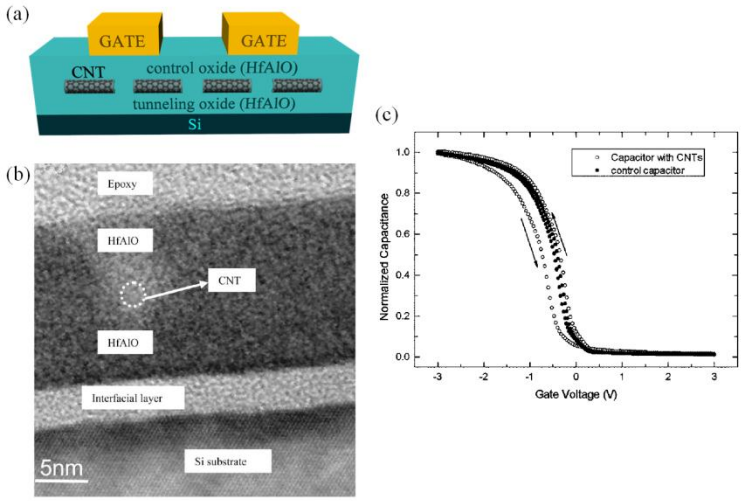

Figure 1.9 *(a) Scheme of the HfAlO/CNTs/HfAlO/Si MOS memory device. (b) High resolution TEM image of CNTs embedded in HfAlO control and tunneling layers. (c) Transfer characteristics of the CNT-based MOS memory devices and the control sample. Adapted from*[63]

Lu et al.[63] created HfAlO/CNTs/HfAlO/Si flash memory device using a CNT as the floating gate. The charge-retention characteristics of the device were determined by measuring its capacitance as a function of the gate voltage (Figure 1.9). The memory effect of the structure was mainly attributed to holes, since negative charge (electrons) writing into the CNTs proved more difficult. A long charge retention time (>10^4 s) was observed.

Ganguly et al.[64] introduced a nonvolatile memory structure using metal nanocrystals (NCs) as the floating gate of a CNTFET. The gate electrode was used to regulate the charging and discharging of the metal NCs from the channel. Each charged NC imposes an extra local potential on the CNT channel, and hence alters its electrical conduction, with sensitivity down to the detection of single electron levels (Figure 1.10).

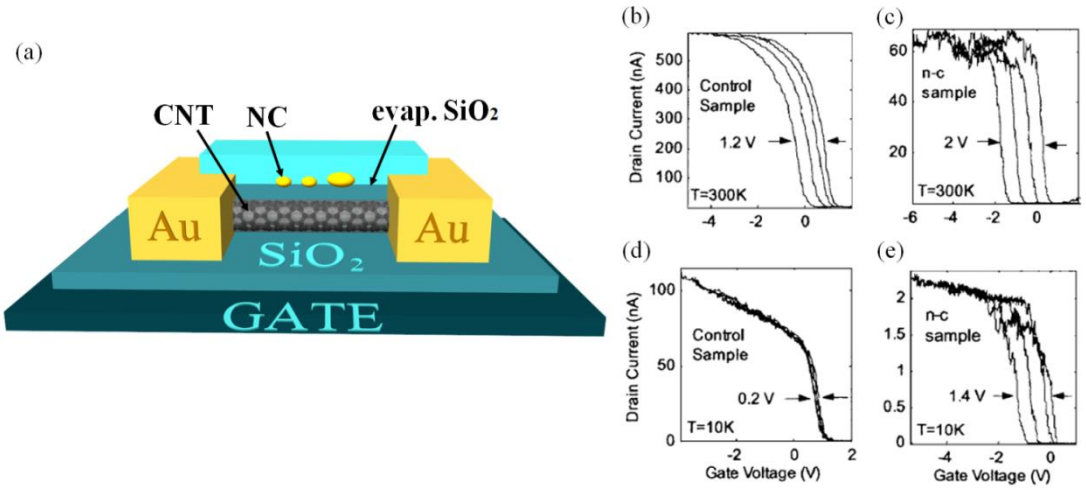

Figure 1.10 *(a) Cross section illustration of memory device based on CNT. (b-e) Transfer characteristics (b) without NC at T=300 K and (c) with NC at T=300 K, (d) without NC and (e) with NC at T=10 K. Adapted from*[64]

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Chapter 2

Semiconductor nanocrystals

The history of low-dimensional semiconductor structures began in 1974, when almost simultaneously, IBM[1] and Bell Laboratories[2] presented the first semiconductor quantum wells. The number of spatial dimensions of the structure is effectively reduced to two as a result of reduced spatial carrier motion in the direction perpendicular to the plane of the quantum well. Further developments in semiconductor nanofabrication technologies allowed producing quantum wires,[3] in which the degree of freedom of charge carrier motions has been reduced to one. The total carrier confinement in all three spatial dimensions was obtained in quantum dots (QDs). The first person to use the term quantum dot, related to zero-dimensional semiconductor nanocrystal, was Mark Reed[4] from Texas Instruments. Initially, QDs have been produced from the quantum wells. The electron confinement in directions parallel to the plane of the quantum well was achieved by applying appropriate voltages to the electrodes disposed in the near vicinity of quantum well.[5] In 1981, Alexey Ekimov discovered QDs in a glass matrix[6] and then in 1985 NCs were fabricated in the form of colloidal solutions by Louis E. Brus.[7] The smallest diameters of first fabricated dots were about 30 *nm*.

QDs attract much attention because they can link the gap between the bulk and molecular levels and lead to broad range of applications *e.g.* in electronics and optoelectronics. There is also a considerable cognitive aspect associated with the possibility of discovering the meanders of quantum mechanics on a new physical object - an artificial atom.

2.1 Basics of semiconductor nanocrystals

The following paragraph provides a general introduction to the theory of QDs, a short description of quantum confinement in semiconductors, QDs synthesis, and a description of a core-shell QDs. Hereafter the term *semiconductor nanocrystals* (NCs) and *quantum dots* will be used interchangeably.

2.1.1 Quantum confinement in semiconductors

Three-directional (3D) semiconductors can be classified by their composition-dependent band gap energy (E_g), where E_g is the minimum energy required to excite an electron from the ground state of the valence band into the vacant conduction band (Figure 2.1a)[8], for instance under optical excitation. So, if the energy of an absorbed photon is greater than E_g, this process leaves a hole in the valence band. The lowest energy state of the created interacting electron-hole pair, is known as an *exciton*. The exciton can be annihilated if the electron relaxes back to the valence band and a photon may be emitted in this process, which is called *radiative recombination*. The exciton has a size defined by its Bohr radius (a_B), which can vary from 1 nm to more than 100 nm depending on the semiconductor material. If the size of a nanocrystal is smaller than a_B, the exciton energy increases, which defines the transition between the bulk crystal properties and the quantum confinement regime. This leads to absorption and fluorescence spectra which is size-dependent. Figure 2.1b illustrates this effect for quasi-spherical cadmium selenide (CdSe) nanocrystals, showing that the fluorescence and absorption of NCs can be tuned by the size of the nanocrystal. CdSe NCs can be tuned to emit fluorescent light in the full visible spectrum range.

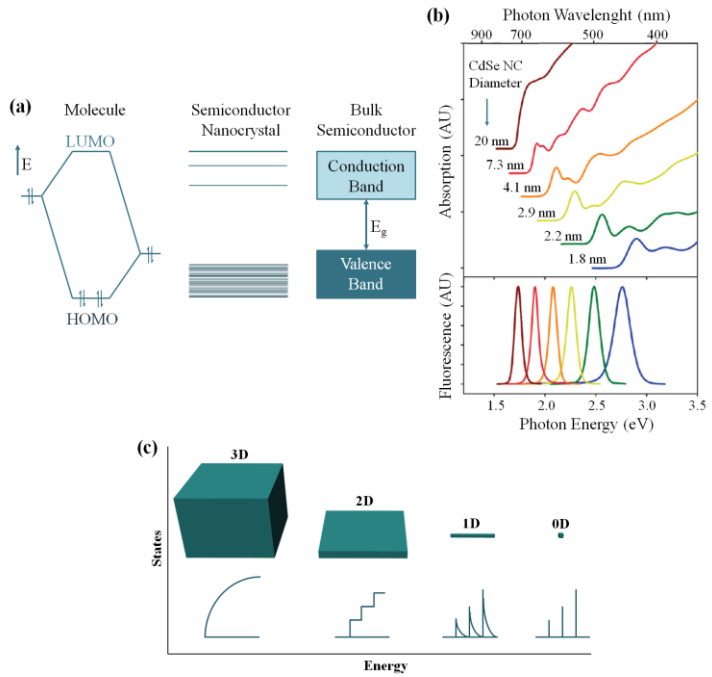

Figure 2.1 *Quantum confinement in semiconductors. (a) Schematics of the electronic energy states in a semiconductor showing the transition from nanocrystals and 3D crystals. (b) Absorption and fluorescence spectra of CdSe nanocrystals (AU - arbitrary units). (c) DOS scheme for one band of a semiconductor structure of 3, 2, 1, and 0 dimensions. Adapted from*[8,9]

There are several possibilities to confine electronic levels in semiconductors, and various types of NCs exist. Figure 2.2 shows examples of objects from which zero-dimensional quantum confinement properties can be observed: single molecules,[10] metallic nanoparticles,[11] semiconductor self-assembled quantum dots or nanocrystals,[12] lateral or vertical dots in semiconductor heterostructures,[13] semiconducting nanowires[14] and carbon nanotubes.[15]

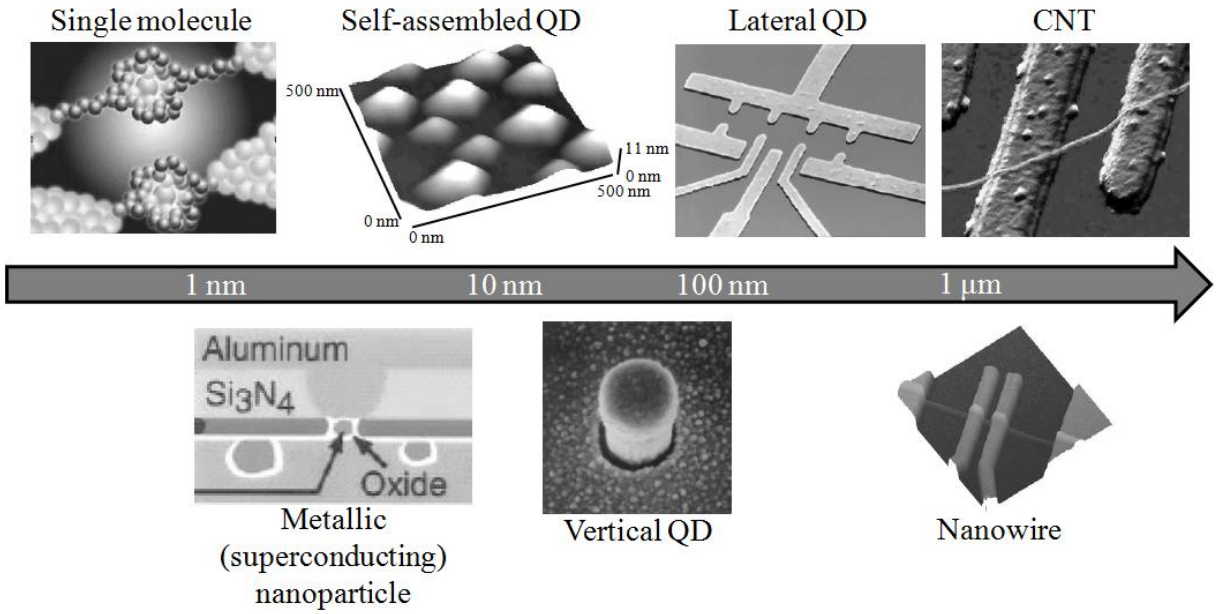

Figure 2.2 *Examples of different systems with a variety of sizes and aspect ratios behaving as quantum dots. Adapted from*[15]

2.1.2 Quantum dot synthesis

The great interest around quantum dots began in 1983, following Louis Brus observation. He was investigating organic redox reactions taking place on the surfaces of photoexcited semiconductors. To do this, he used colloidal semiconductors (in aqueous solution) to obtain higher surface area for the reactions.[16] He observed that the band gap was experimentally varying as a function of the particle size. Through this discovery, researchers began to understand that nanocrystals can be highly important for micro and optoelectronics.

Nowadays nanocrystals are commonly fabricated as colloids or as epitaxial structures grown on solid crystalline substrates. Epitaxial nanocrystals can be prepared with a wide range of shapes and sizes in regular patterns. The advantage of this method is that nanocrystals can by directly integrated in devices. However, solution phase techniques

provide exceptional control over size, monodispersity and shape; their low price, in comparison with the epitaxial method, is also one of their advantages.

In this work, we used colloidal nanocrystals synthesized from metal organic precursors[17] and solvents, as illustrated in Figure 2.3. The metal organic precursors decompose upon heating, and form monomers which allow nucleating the nanocrystals. The synthesis temperature must be high enough to allow for rearrangement and annealing of atoms, but low enough to favor crystal growth. Another critical parameter is the concentration of monomers, leading to two different growth regimes ("defocusing" and “focusing” regimes) from which the size distribution of the grown nanocrystals can be optimized. The great advantage of colloidal synthesis is that large quantities of different types of semiconductor NCs can be fabricated, which is promising for commercial applications.

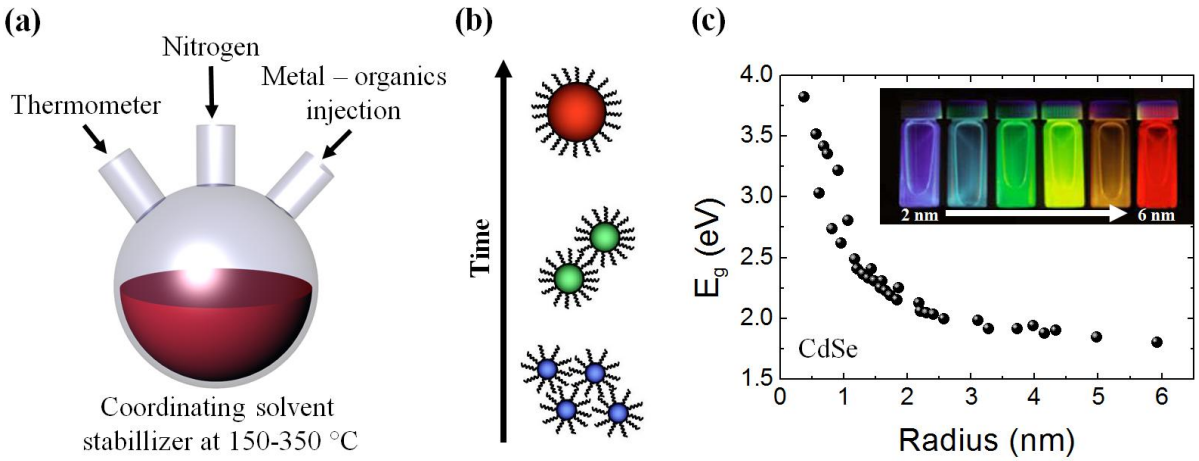

Figure 2.3 *Colloidal nanocrystal synthesis. (a) Schematics of synthesis process. The growth of nanocrystals occurs after the injection of metal and chalcogenide precursors into a hot solvent. (b) Illustration of the control of the nanocrystal size from the growth time. (c) Experimental effective bandgap of CdSe nanocrystals as a function of their radius. Adapted from*[18, 19]

2.1.3 Core-shell QDs

Due to the small particle size, the surface to volume ratio of NCs is relatively high. The atoms on the nanocrystal surface are not bonded completely with the crystal lattice. This way crystalline periodicity is distorted and can form one or more "dangling orbital" sticking out from each atom of the NC surface. Interactions between the NC surface atoms and the surrounding molecules can also significantly affect their optical properties.8

Nanocrystals exhibit in general facets (see Figure 2.4a-c for illustration), each of the facets containing unpassivated orbitals corresponding to surface states.[20,21] If the energy level

of surface states fall within the semiconductor band gap, they can lead to charge carrier trapping at the quantum dot surface. This trapping reduces the overlap between electrons and holes, and favors the probability of nonradiative with respect to radiative relaxation events.

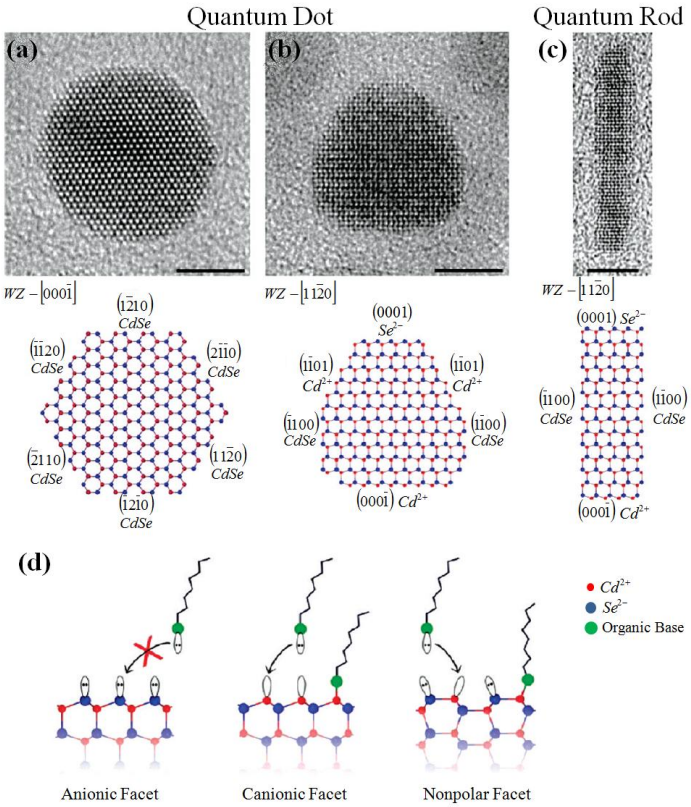

Figure 2.4 *An example of surface properties of CdSe nanocrystals. (a), (b) and (c) TEM images of NCs with different shapes*[22] *(scale bars are 5 nm) together with atomic models. (d) the terminal dangling orbitals on each type of facet. Adapted from*8

To enhance the fluorescence of NCs and reduce the influence of surface states, semiconductor nanocrystals can be coated with an insulating inorganic shell. This process passivates the surface bonds, and adds a material acting as an energy barrier around the nanocrystal. The electronic wave-functions of the nanocrystal charge carriers therefore become concentrated at the nanocrystal core, and do not overlap with its surface,[23, 24] thus reducing the influence of surface defects onto the fluorescence efficiency. In this work, we used CdSe/ZnS nanocrystals commercially acquired from MKNano, which still exhibit blinking properties (see hereafter).

2.2 Blinking of single QD

The phenomenon known as "optical blinking" is a two-level intermittency in which the fluorescence of a quantum dot is observed to be switched *on* and *off* as a function of time. Early approaches have attributed optical blinking to the fluctuation of the charge occupation of the NC, in which fluorescence of an electrically neutral quantum dot is switched off in the case of a charged NC.[25] This phenomenon is on the one hand extremely puzzling, and on the other hand technologically important while using NCs as light sources. It has therefore become a very active research topic, and has been mostly investigated from optical measurements[26, 27]. In addition, electrical behaviors with on/off states attributed to optical blinking were experimentally observed.[28] We present here below a short overview of the optical and electronic blinking properties colloidal NCs.

2.2.1 Confocal luminescence experiments

Time-dependent blinking or luminescence intermittency is illustrated in Figure 2.5. It has been observed on time scales ranging from microseconds to minutes, which fall much above the time scales corresponding from the quantum dynamics of excitons (in the range of picoseconds to nanoseconds).[29] Interestingly, blinking effect has been observed on a large variety of nanocrystals, ranging from II–VI (CdSe, CdTe) materials, silicon nanocrystals, self-assembled semiconductor InP quantum dots, and even for color centers in nanodiamonds.[29,30]

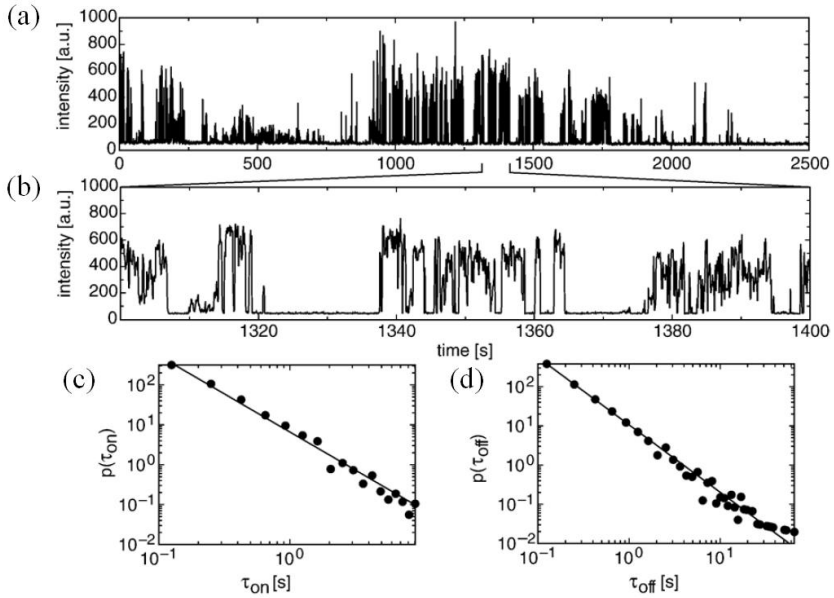

Figure 2.5 *Time resolved luminescence experiments. (a) Luminescence intermittency of a single CdSe/ZnS in polystyrene showing a clear random telegraph pattern. (b) Zoom in on the time trace presented in graph (a). (c-d) Distributions of on- and off-times followed by power-laws Adapted from*[29]

Nirmal *et al.*[31] have observed for the first time blinking of single CdSe colloids capped with a ZnS shell (and surfactant molecules such as trioctylphosphine oxide) which had been spin-coated onto silicon dioxide substrates. A sequence of active luminescence (*on* state) and inactive luminescence (*off* state, no optical emission) equivalent to random telegraph signals has been observed, with *on* and *off* state durations ranging from ms to several $100\ s$. The observed *on*- and *off*-time probability distribution (τ) shows, in general, a power-law statistics: $f(\tau) \propto \tau^{-\alpha}$, with power-law exponents α in the range between 1.1. and 2.2 (the exponents may vary upon the detection threshold and binning time of the experimental set-up due to the divergence of the power-law).[32] The shortest binning times are in usual limited to ms due to CCD optical detectors (see the examples shown in Figure 2.5), but Verberk et al.[33] used an autocorrelation techniques pointing towards blinking times down to the excited state lifetime of $30\ ns$. Figure 2.6 presents two examples of sub-millisecond power-law dependencies.

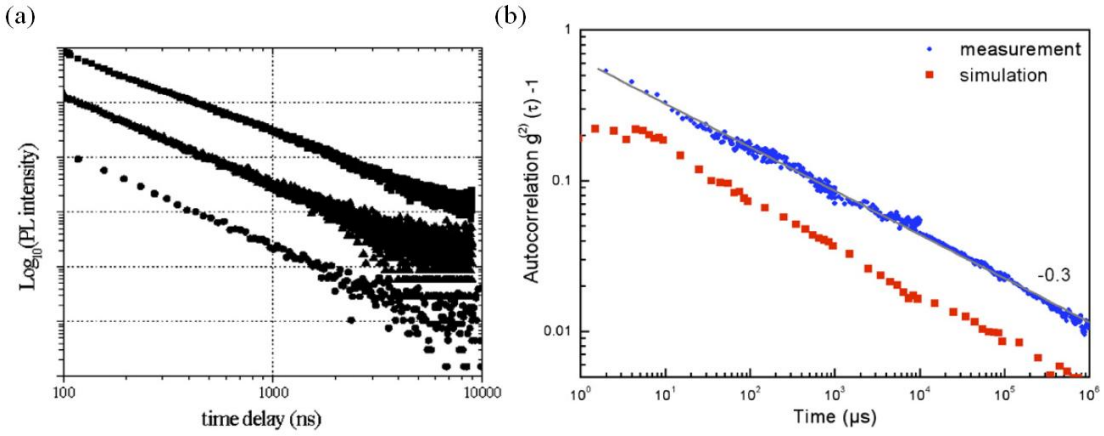

Figure 2.6 *Power law statistics (a) Time-correlated single-photon counting experiments of NCs ensembles with the detection time of* $\sim 100\ ns$. *(b) Autocorrelation function of the luminescence intensity of an individual CdS NC* [33] *followed by power law from 1 s down to ~1μs. Adapted from* [29]

The blinking of semiconductor nanocrystals was assigned in early models[34] to the photoejection (photoionization), most likely of an electron because of its more extended wave function, thus implying that the NC charged state would be associated with a positive charge. This has been observed experimentally for the first time in 1999 by Krauss and Brus[35] who performed electrostatic force microscopy to detect the electrostatic blinking of the charge state of CdSe nanocrystals at a low time scale (typically of the order of a few minutes) and its switching between a neutral and a positively charged (+e) state. The presence of a charge in the NC efficiently introduces non-radiative Auger processes[29] which can predominate over the radiative optical process, and thus quench the NC fluorescence. According to trap models, the

ejected charge tunnels back and forth between the nanocrystal and trap sites giving rise to the observed power-law behaviors.

Figure 2.7a presents a schematics of this 'conventional' blinking mechanism, more recently referred to as *A-type* blinking by Galland *et al.*[36] The *on* and *off* times correspond to a neutral and a charged nanocrystal, respectively. The *on* state fluorescence is associated with the radiative recombination of the neutral exciton, X^0 (see Figure 2.7) with a dynamics characterized by a mono-exponential decay ($15-30\ ns$ in CdSe nanocrystals).[37,38,39] The *off* state is dominated by a faster and non-radiative process involving a charged exciton X^-. This model agrees with the fluorescence behaviors observed in experiments,[37,38,40] corresponding either to actual blinking (Figure 2.7c) in which the fluorescence signal is analogous to random telegraph signal, or to flickering, if the two states are averaged during the data acquisition bin times.

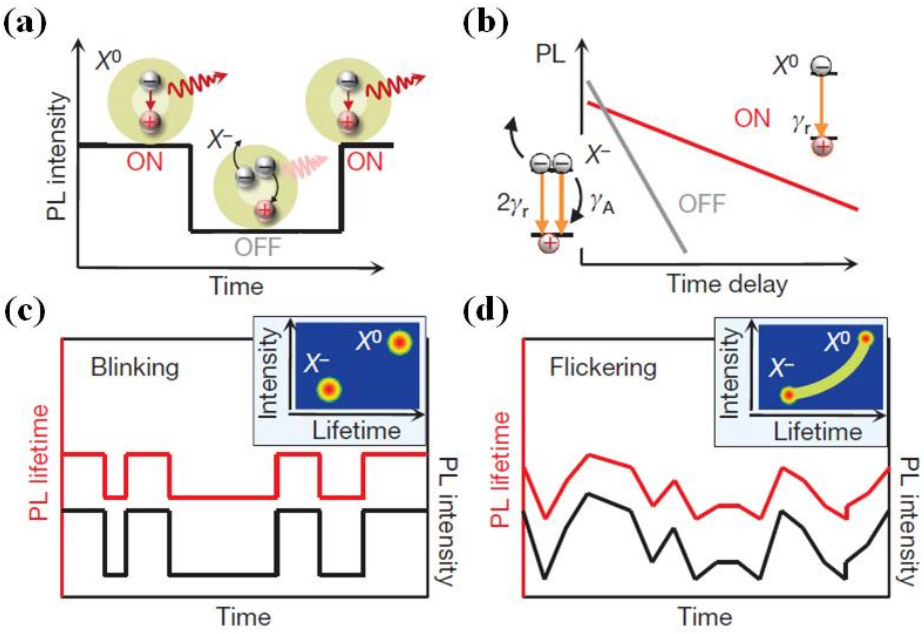

Figure 2.7 *Blinking behavior of individual NCs. A-type blinking and flickering models. (a) The conventional blinking model, in which on and off states correspond to a neutral nanocrystal (X^0) and a charged nanocrystal (X^-), respectively. (b) Scheme of the on and off photoluminescence decays in a logarithmic representation. The time traces observed for blinking and flickering are shown in (c) and (d). Adapted from*[36]

2.2.2 Electrical intermittency of single QDs

Random telegraph signal phenomena have been observed in electrical experiments on single quantum dots, in line with the above mentioned work by Krauss and Brus using electrostatic force microscopy on CdSe NCs. These effects are in general related to trap state

effects. An electrical current intermittency could be, for instance, detected only in case of single NC (the effect was not observed in ensembles of NCs).[41,42] The study of local charging dynamics on the surface of a colloidal nanorod (NR) was presented by Steinberg *et al.*[28] Figure 2.8a shows a typical example of a multistable $I(V)$ curve, taken at temperature 4.2 K. During the experiment, current versus time traces were measured at the fixed gate voltage, in analogy with the luminescence experiments.[43] An example of observed $I(t)$ trace measured at $V_{SD} = 0.36\ V$ is presented in the inset to Figure 2.8b, showing the current multistability.

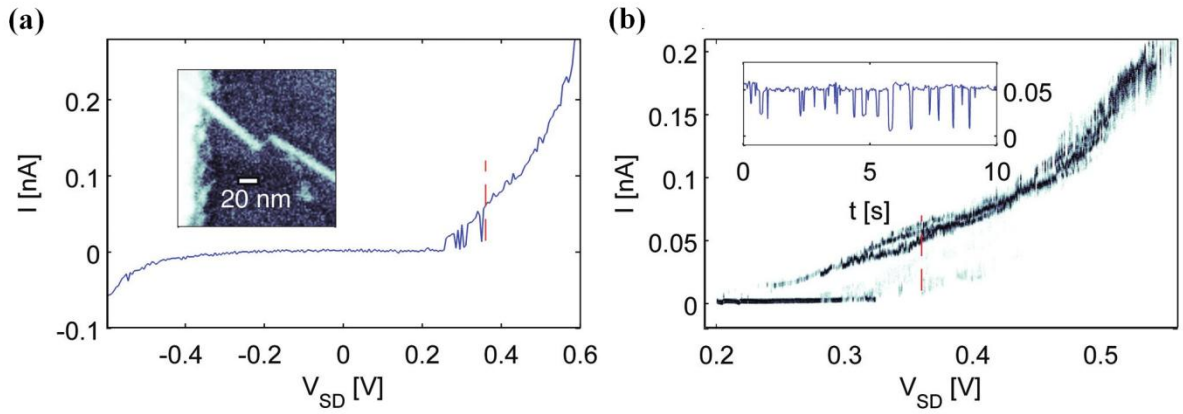

Figure 2.8 *Electrical current switching in single nanorods. (a) Transport characteristics showing the current fluctuations at T= 4.2 K. The dotted red vertical line marks the voltage where the data in the inset to (b) is taken. Inset: AFM image of the NR, connected to the tungsten electrodes. The bright region on the left is the Au electrode. (b) Normalized transport characteristic extracted at each voltage from a* 45 *s long time-domain signal with sampling resolution of* 23 *ms. Inset: Time domain signal at* $V_{SD} = 0.36\ V$ *(marked by a vertical red dashed line), exhibiting current switching between several levels. Adapted from*[28]

Steinberg *et al.* explained the current fluctuations with charging and discharging dynamics of several surface traps. Such an explanation was quantitatively established in case of bistable current traces (see Figure 2.9a), where the probability for the time t spent at the $high$ or low current state followed an exponential dependence $exp(-t/\tau_{H,L})$ (Figure 2.9c-d). This behavior was then modeled by charging dynamics of a single surface trap.

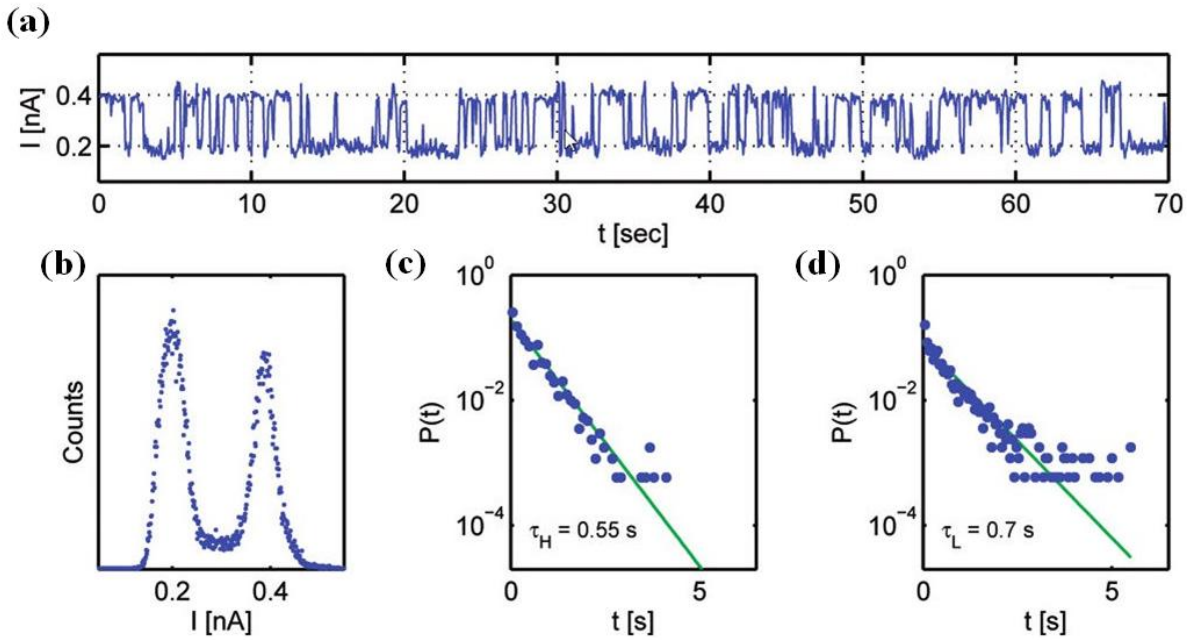

Figure 2.9 *Current statistics. (a) $I(t)$ characteristics at $T = 4.2\ K$ and $V_{SD} = 0.2\ V$. The sampling time is $55\ ms$. (b) Corresponding current histogram. (c-d) Probability densities of the high (H) and low (L) current states. Adapted from*[28]

2.3 Electronic properties of coupled QDs and CNTs

In the field of electronics, noise is treated as a random fluctuation in an electrical signal, a characteristic of all electronic circuits.[44] While noise is generally unwanted, it can be used as an important tool in nanoelectronics. In traditional MOSFETs, the current noise power spectrum at low frequency follows a $1/f$ law (Figure 2.10a). Generally, the $1/f$ noise is understood as the superposition of random events of single-charge trapping and de-trapping from the oxide defects situated close to the semiconductor channel.[45,46] In a submicrometer MOSFETs, only a few traps exist, and a discrete switching of the current between two (or more) levels under constant bias conditions can be observed.[47] These fluctuations are known as a random telegraph signal (RTS) or random telegraph noise. They have been also observed in systems based on semiconductor nanocrystals[28,48] and in CNTFETs.[49,50] Such a noise gives rise to a Lorentzian distribution in the current noise power spectrum (Figure 2.10b).

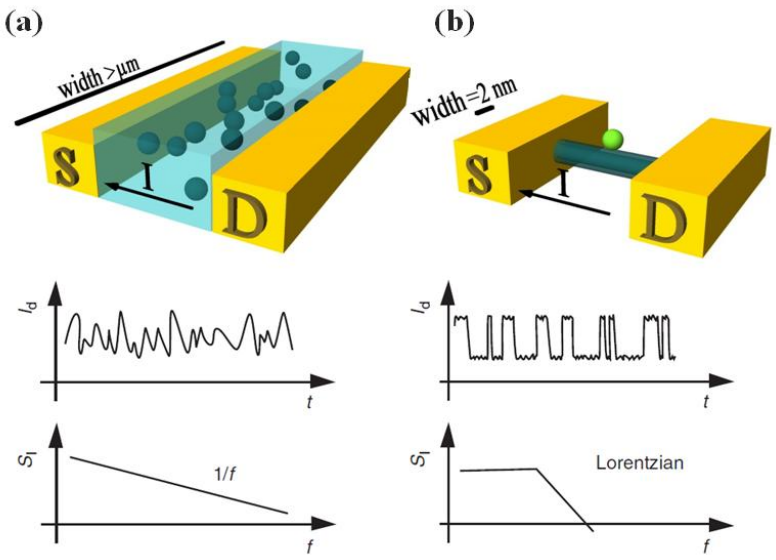

Figure 2.10 *Noise in nanotransistors. Scheme of a conventional MOSFET (a) and CNTFET (b) with examples of time-dependent current fluctuations and the corresponding power spectrum noise (plotted below). Defects are shown as balls and gate oxide with semi-transparent blue color. Adapted from*[47]

CNTFETs can be used as electrometers with single-electron resolution.[49] These advantages have been used for example for sensing of chemical gas[51] and biological probes.[52]

The detection of stored charges in a gold NC with diameter of 30 nm using CNTFET was shown by Marty et al.[53] The CNTFETs used in the experiment were fabricated by self-assembly with the top gate electrode to increase the gate coupling (Figure 2.11a). The nanocrystal distance from the tube was estimated to be around 10 nm. Below 120 K, the field effect was exhibiting steps that became hysteretic below 60 K (Figure 2.11b). These steps were interpreted as direct measurements of the charge transfer that occurs between the carbon nanotube and the gold nanocrystals. However, the precise number of electrons involved in the charge transfer could not be measured.

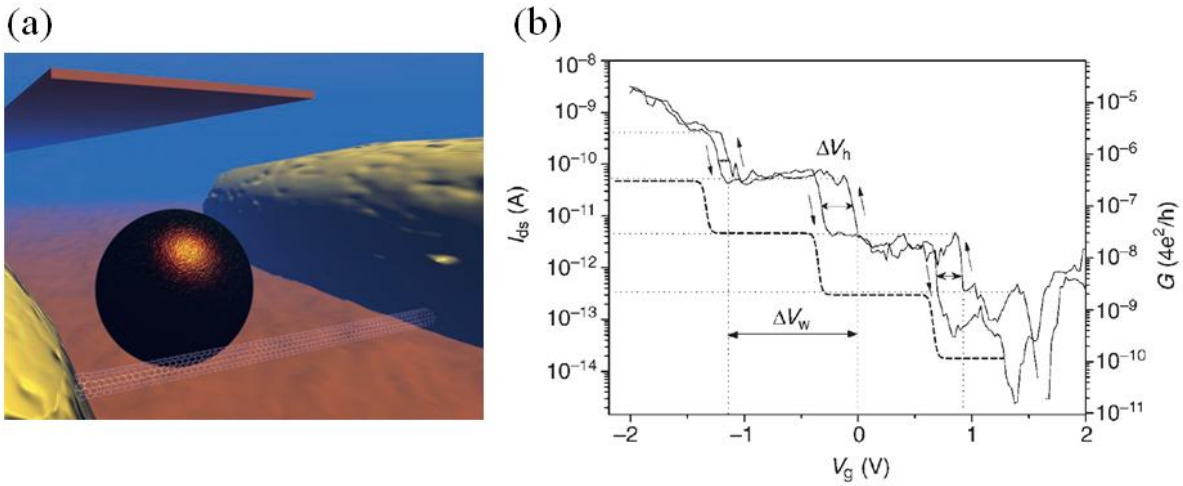

Figure 2.11 *Single electron memories. (a) The 3D diagram of the device based on a CNT with connected Au nanoparticle. A gate electrode was deposited on top to increase the gate coupling. (b) Transfer characteristics of a CNTFET after nanoparticle deposition, recorded at* $T = 2K$. *The charge transfer occurs at regularly spaced gate voltages separated by* ΔV_W *and charging/discharging of the trap occurs at a gate voltages separated by* ΔV_h. *Adapted from*[53]

A rather similar work was presented by Grüneis et al.[54], however with a gold nanocrystal brought in near contact with the nanotube and with a CNTFET operated from its back gate (Figure 2.12a). The transfer of electrons onto the particle was detected by monitoring the conductance of the nanotube (G_{tube}) while sweeping the gate voltage V_G from -4 to -1 V. Grüneis et al. observed tens of abrupt conductance jumps (marked by vertical red bars presented in Figure 2.12a) that indicate individual electron transfers from the nanotube into the particle. The stochastic nature of the electron transfer was inferred from the fact that as the measurement was repeated, conductance jumps appeared at different gate voltages (Figure 2.12b). However, it was possible to observe a reproducible shift in V_G value corresponding to a transfer of an electron on to a nanoparticle located a few nanometers from the nanotube.

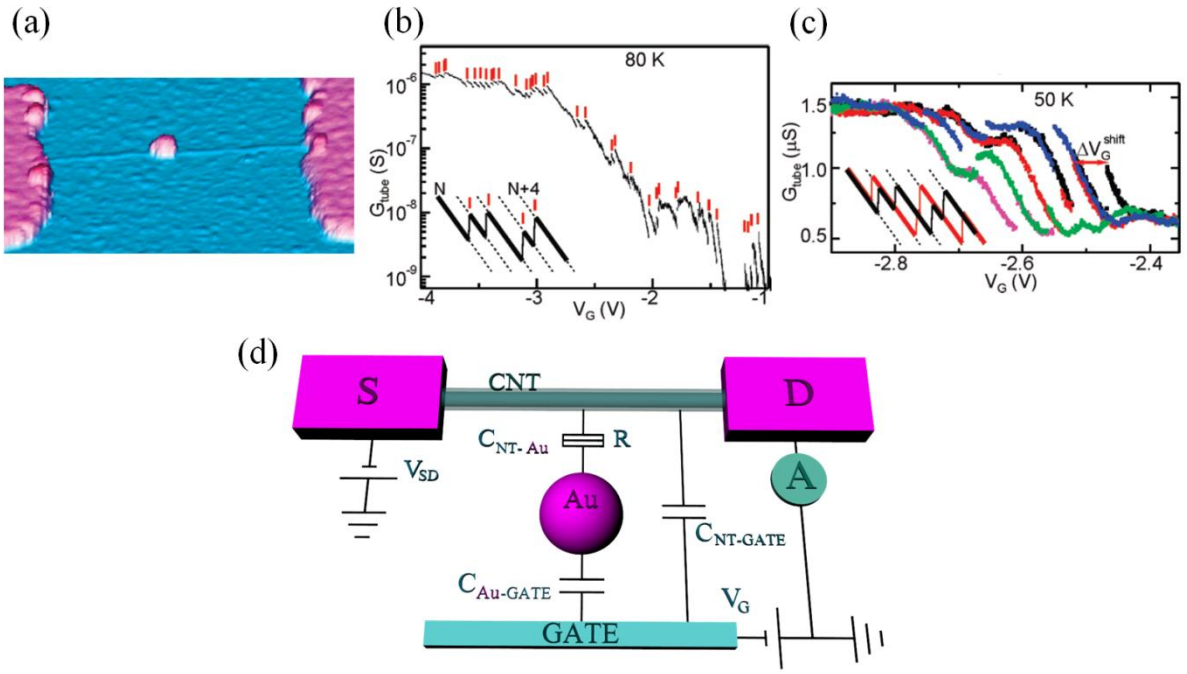

Figure 2.12 *Single electron detection. (a) AFM image of an Au nanoparticle placed on top of a CNTFET channel. (b) Tube conductance as a function of gate voltage V_G.Vertical red bars indicate conductance jumps. The inset shows the relation between $G_{tube}(V_G)$ and the number of electrons in the gold particle. (c) $G_{tube}(V_G)$ characteristics. Each color corresponds to a different measurement. Jumps appear at different V_G values as a result of the stochastic nature of the electron transfer. (d) The equivalent electrical circuit of a nanocrystal-nanotube device. Individual electrons tunnel between the quantum dot and the nanotube through the tunnel resistance R. Adapted from*[54]

Grüneis *et al.* have shown how a method of single-electron detection can be used to derive the separation in energy between the electron states of the particle. Figure 2.13 shows schematics of the potentials in the nanotube and the Au nanocrystal as the gate potential is swept down. Grüneis explained the mechanism as follows: each time an empty energy level of the particle matches the electrochemical potential of the tube, an electron is transferred onto the particle (Figure 2.13c), which is detected by the nanotube transistor. To add an electron to the particle, the Coulomb charging energy E_c is required:

$$E_c = e^2/\left(C_{tube-Au} + C_{Au-gate}\right), \tag{2.1}$$

and ΔE (the level spacing):

$$E_{ad} = E_c + \Delta E, \tag{2.2}$$

(represented by a gap in Figure 2.13a). By reducing the gate potential E_G proportional to $-eV_G$, the potential of the gold nanocrystal E_{Au} decreases according to Kirchhoff's laws. When the electrochemical potential of CNT matches the upper energy of the Coulomb gap in

the particle (Figure 2.13c), an electron can be transferred from the CNT onto the NC, and the electron number N in the particle is increased by 1. This changes E_{Au} by the amount E_c (see Figure 2.13d), which blocks the transfer of the next electron. The transfer rate was slow enough to prevent the last charge from tunneling out of the NC by continuously sweeping down the gate potential.

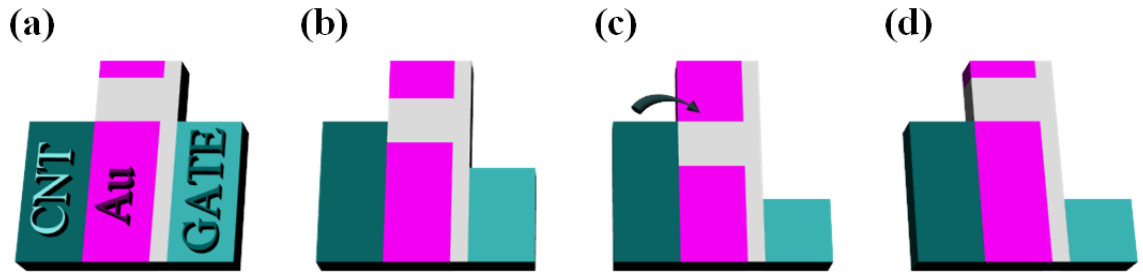

Figure 2.13 *Schematics of the potentials in CNT and the Au NC. The gate potential is swept down from (a) to (c). In this process, each time an empty energy level of the Au NC matches the electrochemical potential of the CNT (c), an electron is transferred onto the NC, which shifts its energy levels (d). Adapted from*[54]

The time-dependent electron transfers was also analyzed. To do so, the gate voltage was set at a fixed value while measuring the tube conductance (Figure 2.14). At $50\ K$, the tube conductance was fluctuating between two values on a time scale. Grüneis attributed the two-level fluctuations to an electron jumping back and forth into the gold particle as a result of thermal excitation and thus changing the number of electrons between N and $N + 1$. After increasing the temperature to$150\ K$, the tube conductance was found to fluctuate between three levels, explained as N, $N + 1$, and $N + 2$ (Figure 2.14b). The scheme of the mechanism is shown in the insets of Figure 2.14.

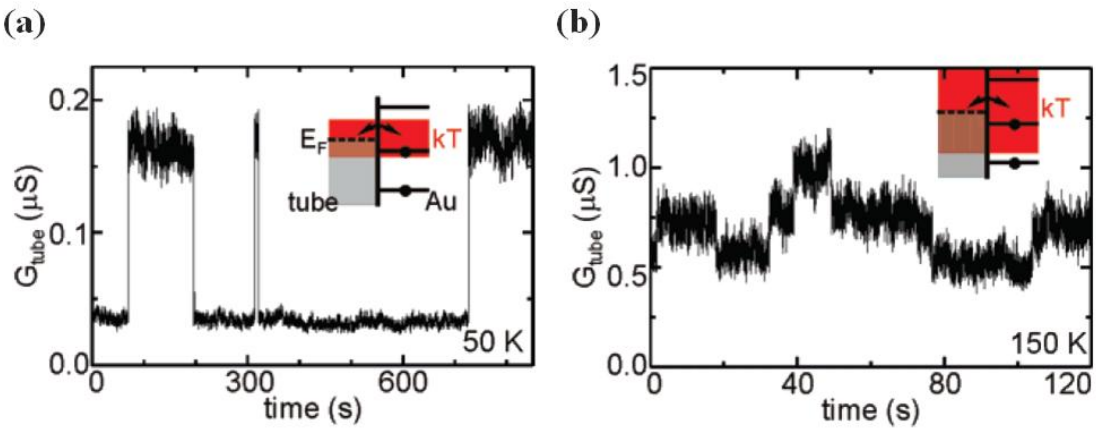

Figure 2.14 *Electron detection. (a) $G_{tube}(t)$ characteristics at* 50 *K, with two current level fluctuation ($V_g = -1.35\ V$). (b) $G_{tube}(t)$ for $V_g = -1.2\ V$ at* 150 *K with three levels. Insets: scheme of energy levels in the CNT and in the Au NC for different numbers N of electrons (the thermal energy shown in red). Adapted from*[54]

Zdrojek et al.[55] proposed a similar approach to investigate single-electron electric effects and the charging spectrum of colloidal semiconducting CdSe NCs. The spectrum of nanocrystals was examined by looking at V_G^{shift} (the amount that $G_{tube}(V_G)$ shifts along the V_G axis, see Figure 2.15b-c). V_G^{shift} is proportional to the energy required to add one electron:

$$V_G^{shift} = \beta E_{ad}, \tag{2.3}$$

where β is the lever arm between the back gate potential and the electrostatic potential on the dot, for the operation of the CNTFET:

$$\beta = \frac{C_{CdSe-tube}}{e(C_{tube-gate}+C_{CdSe-gate})}. \tag{2.4}$$

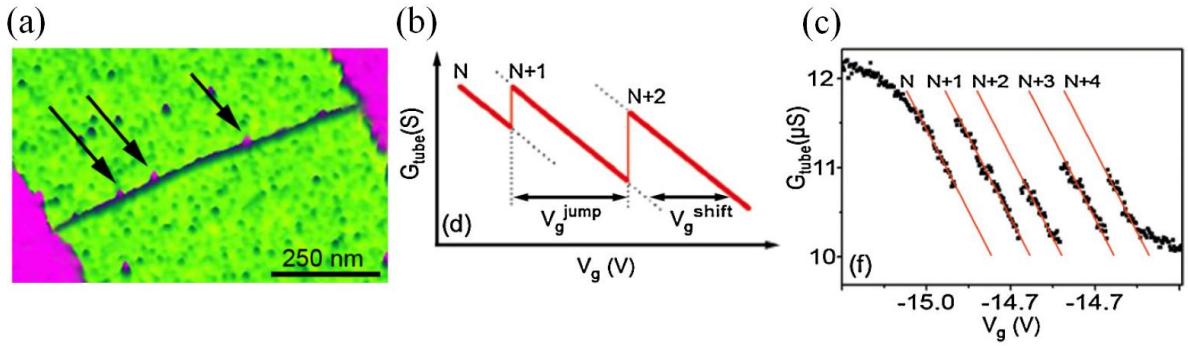

Figure 2.14 *Electron counting spectroscopy. (a) AFM image of a device with a CNT decorated with three CdSe NCs (labeled by arrows). (b) Schematic of $G_{tube}(V_G)$ curve. (c) Tube conductance as a function of V_G at T = 60K. Each shift of $G_{tube}(V_G)$ is attributed to a single electron transfer. Adapted from*[55]

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Chapter 3

Fabrication of nanodevices based on CNTs and NCs

This chapter describes in details all mentioned steps that end up with fabrication of a back-gated CNTFET coupled with individual NCs. The fabrication includes multiple nanofabrication steps. One ideally starts with depositing purely semiconducting CNTs with a predetermined length and diameter, in selected areas of a sample. Transistors are then fabricated using electron-beam lithography. The deposition of nanocrystals along the nanotubes is then perform, which still remains a challenging task[1,2,3,4].

3.1 Fabrication of back-gated CNTFETs

Figure 3.1 shows an AFM image of a back-gated CNTFET. In this paragraph we present all the steps in the process of CNTFET fabrication, namely: marker fabrication, CNT deposition and growth, CNT localization with respect to markers and contact fabrication.

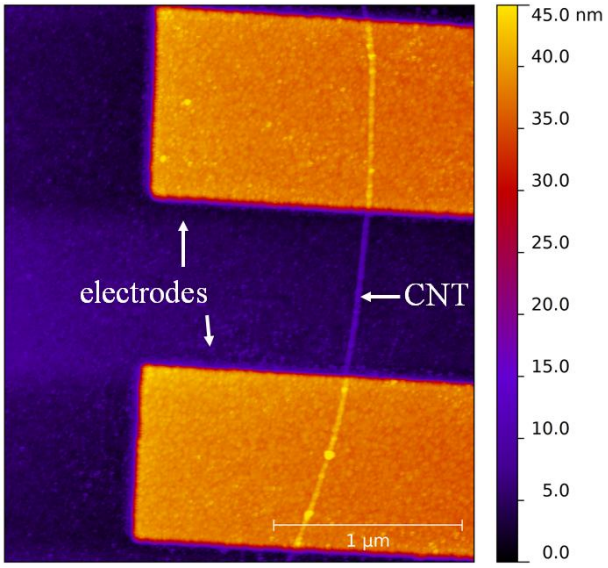

Figure 3.1 *AFM topography image of CNTFET which was fabricated from a semiconducting nanotube grown by chemical vapour deposition on a 1 µm thick SiO_2 layer (blue area). The source and drain electrodes correspond to the orange areas in the topography image.*

3.1.1 Markers fabrication

Two sets of alignment markers are used during sample fabrication: electron beam lithography markers (e-beam markers) and atomic force microscopy markers (AFM markers). E-beam markers are critical in maintaining overlay accuracy throughout a lithography process flow using alignment steps; AFM markers enable the localization of individual CNT. Both sets of markers can be patterned during one lithography step (Figure 3.2 and 3.3e). In this work, for all fabricated samples, we used p-type silicon substrates with thermally grown oxides of thickness is $\sim 300\ nm$ or $\sim 1\ \mu m$. The clean silicon wafers were first coated with a double layer of e-beam resist. The first, thicker bottom layer is more sensitive to e-beam exposure and serves as separator ensuring a proper lift-off. In this work we used EL 13% (MAA, 8.5) dissolved in ethyl lactate. The second, top layer of resist (PMMA 3% 495K dissolved in anisole) is less sensitive to e-beam and serves as an actual mask for metal evaporation. A pattern is written in the double resist layer by a beam of electrons using VISTEC EBPG 5000 Plus system. The e-beam locally breaks PMMA bonds and the typical dose used was 370 $\mu C/cm^2$.

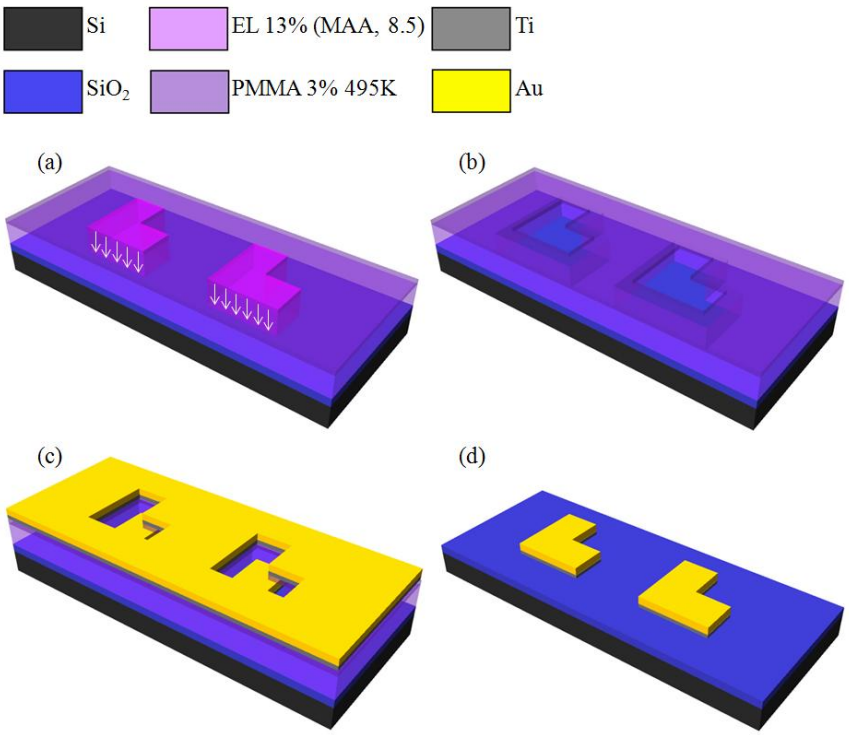

Figure 3.2 *Scheme of processing flow for the fabrication of markers. (a) A double layer of MAA/PMMA is placed on a silica surface; a pattern of marker matrices is irradiated with e-beam. (b) After development, an opening is left in the PMMA. (c) Metal is evaporated. (d) The remaining resist is removed during lift-off process resulting in patterned surface with metal markers at the predesigned positions.*

The next step is the development process in which the e-beam exposed PMMA is removed from the substrate. The sample is immersed in a developer containing a one part of methyl isobutyl ketone (MIBK) and two parts of iso-propyl alcohol (IPA). Then the sample is metallized using an e-beam evaporator with the two layers of metal. Applying a double metal layer provides better metal adhesion to the substrate, for this we were using 5 nm thick Ti as a sticking layer and 45 nm of Au. After metallization, the next step is the lift-off process during which the unexposed resist and excess metal is removed from the substrate. Samples were heated in SVC® remover for around 30 min at 70°C. After lift-off, the substrate is rinsed with acetone and IPA in order to remove residues of metal and PMMA.

3.1.2 CNTs deposition and growth

In this work, two types of CNTs samples were used for transistor fabrication. For the first type, CNTs were deposited from organic solutions. For the second type of samples nanotubes were grown by chemical vapor deposition (CVD) directly on the SiO_2 substrates.

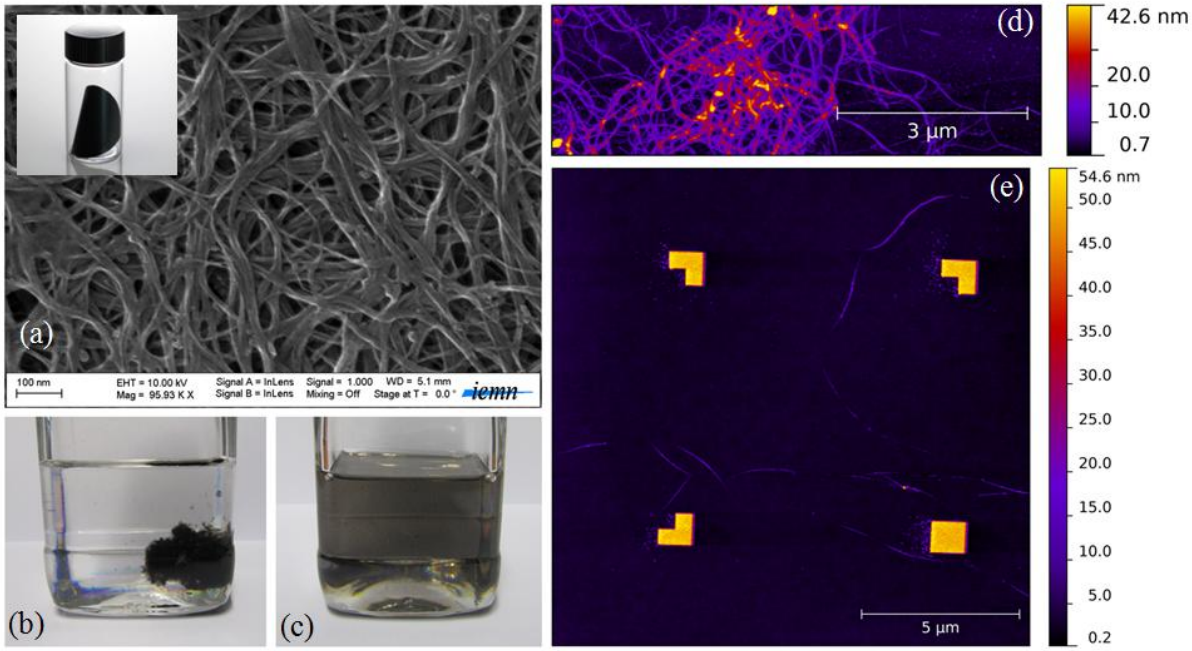

Figure 3.3 *CNT deposition. (a) SEM image of the NanoIntegris SWNT material. The insets show the powder of semiconducting IsoNanotubes (99%) from NanoIntegris used for experiments. (b) SWNT "cake" in DCB and IPA solution after soft sonication. (c) SWNT solution in DCB and IPA after horn sonication. (d-e) AFM images of SWNTs deposited on SiO_2 after for (d) 5 min and (e) 30 min horn sonication.*

For the first method a surfactant-eliminated powder of semiconducting IsoNanotubes (99%) purchased from NanoIntegris was used (Figure 3.3a). The use of these samples is very convenient on one hand, since the goal is to fabricate CNTFETs with semiconductor channel. On the other hand, the dispersion of powder samples has proven to be difficult (see **Chapter**

1.1.2 Carbon nanotube synthesis and dispersion). The list of organic solvents tested during ultrasonic SWCNTs dispersion was as follows: ethanol, N-Methyl-pyrrolidone (NMP), methanol, aceton, chloroform, dichloromethane, 1,2-Dichlorobenzen (DCB), isopropanol (IPA). DCB with a few droplets of IPA turned out to be the best solvent for dispersing CNTs from NanoIntegris.[5] A small amount of CNT powder ($\sim 0.1\, mg$) is placed in a bottle containing 17 ml of DCB/IPA and sonicated until the initial CNT material ("cake") is visibly dissolved (Figure 4.3b-c). Sonication time is typically $\sim 30\, min$ to 1 hour in a 46 kHz bath sonicator (LEO Ultrasonic Cleaner). To suspend individual CNTs in the solvent (*i.e.*, to exfoliate the CNT bundles), additional 24 kHz horn sonication (UP400S) for $\sim 15\, min$ is used. Then a few droplets of the obtained solution are placed on a substrate and blown-dried with nitrogen. At the end, CNTs are left in random positions on the substrate as shown in Figure 3.3e.

The above-described method is slower in comparison with the entire CVD technological process, but there is very high probability that all nanotubes are semiconducting. Unfortunately, we encountered some difficulties during dispersion process. While imaging CNTs from NanoIntegris placed on silicon substrate, we observed a coating of uneven thickness along the nanotubes surfaces. Because of this coating layer it is harder to make good contact to deposited CNTs (during the fabrication process we usually chose the clean part of the nanotubes in order to make better quality contacts). The attempts to identify and to remove the excess material and purify the nanotubes from a thermal treatment are described in **Annex A: Thermal analysis of nanotubes**, but they did not prove to be successful. Figure 3.4 presents the AFM images of the two kinds of CNTs used in this work, for sake of comparison.

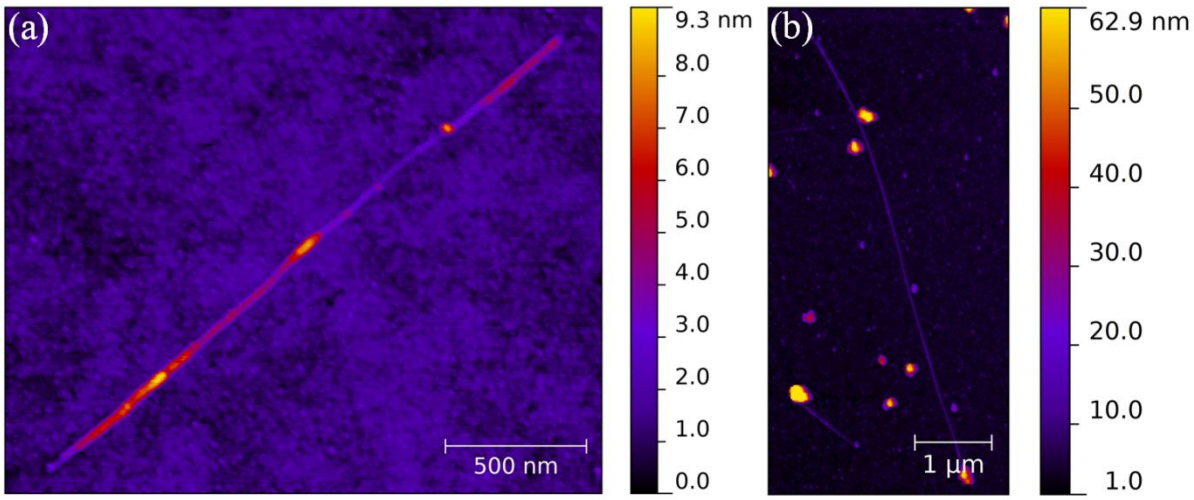

Figure 3.4 *AFM images of SWNTs (a) from NanoIntegris, coated with extraneous material and (b) grown by CVD using pure methane (CH_4) as the carbon source.*

The second type of samples was high-quality CNTs grown by catalytic CVD (CCVD) using methane (CH_4) as the carbon source.[6] A schematic of the thermal CCVD system is shown in figure 3.5a. The partially home-made system is based on a modified Lindberg/BlueM furnace, which consists of one inch diameter quartz reaction tube in between two heating coils. The system allows maintaining a stable temperature up to 1100 °C in central part of the tube (where the sample is kept during the growth process). The growth process involves thermal decomposition of methane over a SiO_2 substrate with previously prepared catalysts. The catalysts were prepared using the following ingredients (from Sigma Aldrich): 80 mg of iron ($Fe(NO_3)_3$ nonahydrate), 4 mg of bis(acetylacetonato)dioxomolybdenum(VI), 60mg of aluminum oxide, all in 60 ml of methanol (HPLC). All components were mixed together and ultrasonicated for one hour before further use. At the end, 10 µl of the catalyst solution was drop casted on the substrate and dried using a nitrogen flow. Directly after catalysts deposition samples were introduced into the furnace.

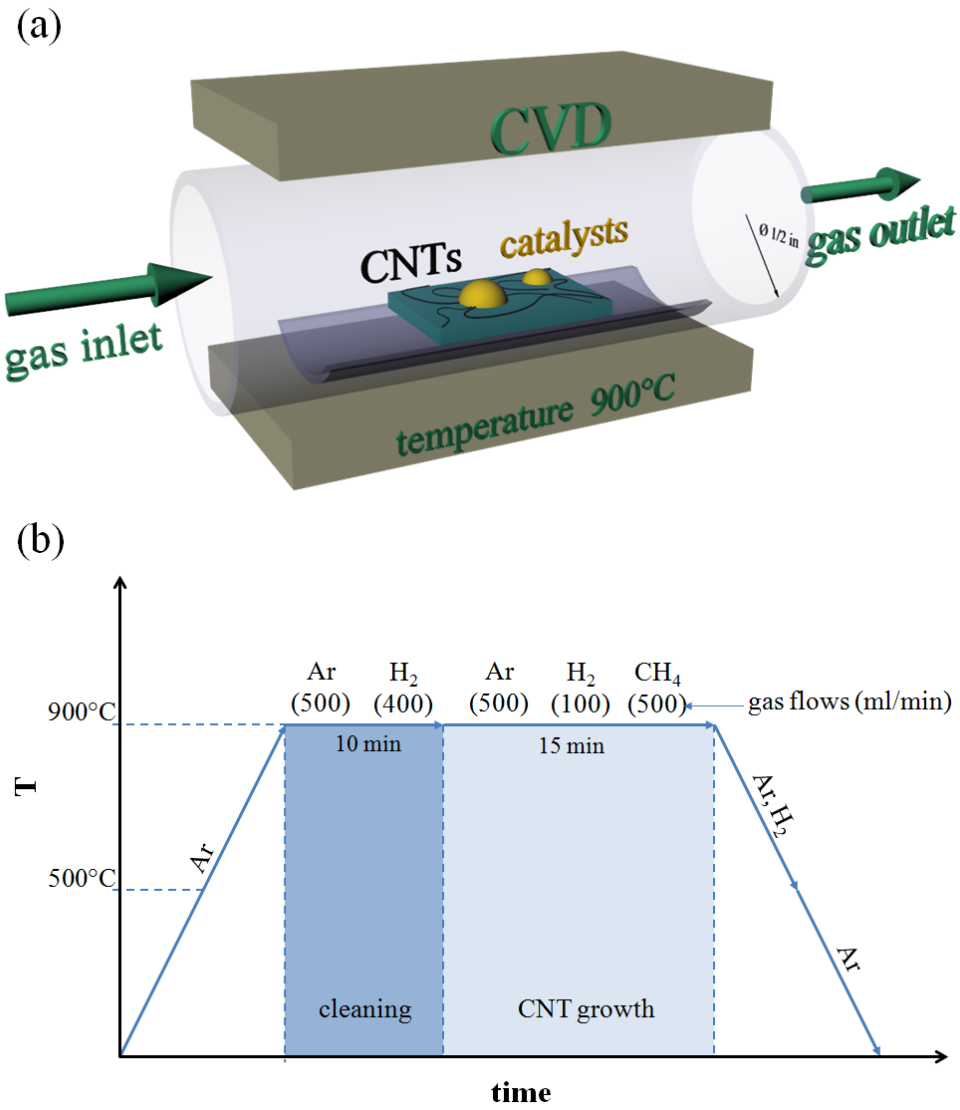

Figure 3.5 *CNTs grown by CCVD. (a) Schematic of CCVD setup using methane as the carbon feeding gas. (b) Scheme of growth procedure showing the timing, gas flow rates and temperature.*

Figure 3.5b illustrates a typical growth procedure involving an initial preheating step under an argon atmosphere (500 ml/min) up to the growth temperature followed by a 10 min annealing under an argon and hydrogen atmosphere (500 and 400 ml/min, respectively). Methane was then introduced into the gas stream for 15 min at a fixed flow rate of 500 ml/min. Simultaneously, the flow rate for argon and hydrogen was fixed to 500 and 100 ml/min, respectively. The growth temperature was set to a fixed value for a given process (*e.g.*, 900 °C). The procedure is then finished with a cooling step, and at 500 °C, the hydrogen feed was switched off. The diagram shown in Figure 3.5b is a graphical representation of the growth procedure using a target temperature of 900 °C.

3.1.3 CNT localization and contact fabrication

After the CNT deposition or growth, nanotubes that are appropriate for further experiments are chosen, localized and imaged using AFM. AFM images were acquired using an ambient-air AFM (Dimension 3100, Bruker Nano). Only straight segments of nanotubes located on clean areas are used for contact fabrication. Figure 3.6 presents the layout of a substrate with the AFM markers, with superimposed AFM image of deposited CNT as a help in designing the electrodes.

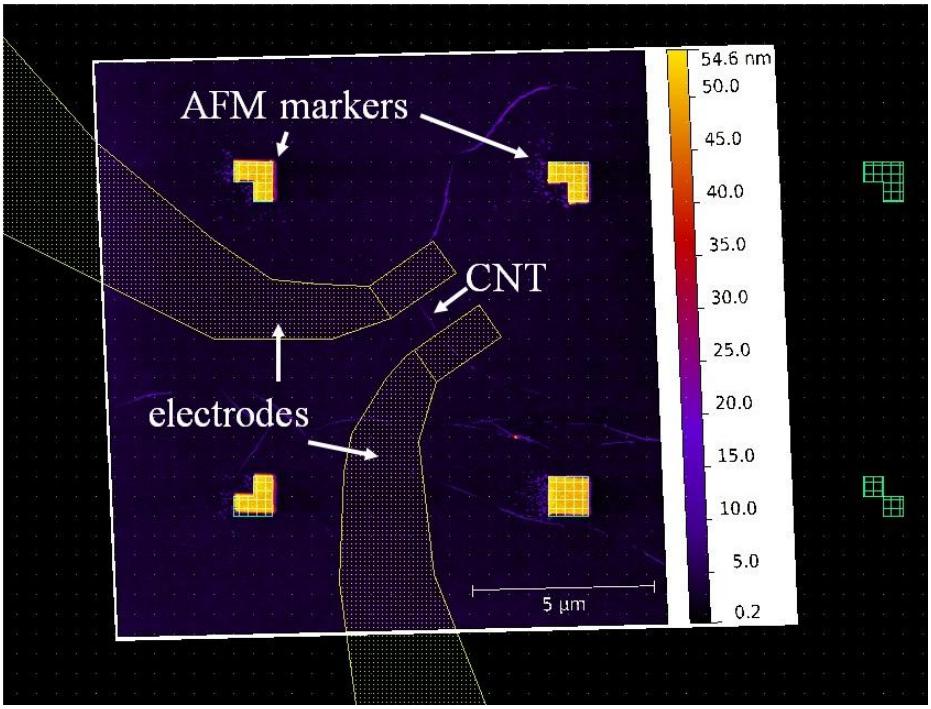

Figure 3.6 *Electrode design. Layout of a substrate with the AFM markers, with superimposed AFM image of deposited CNT as a help for designing electrodes for EBL process.*

Figure 3.7 shows a step-by-step schematics of the fabrication of metal contacts. In the first step, a two-layer electron sensitive resist is deposited (like in the case of markers fabrication) followed by the e-beam exposure in order to write the electrode patterns, and finished by metal evaporation on the sample surface and lift-off. The metal sequence for the electrode contact is: Ti/Au (5/45 nm). All devices of this work have been contacted with top electrodes and gated by the doped silicon substrate back-side.

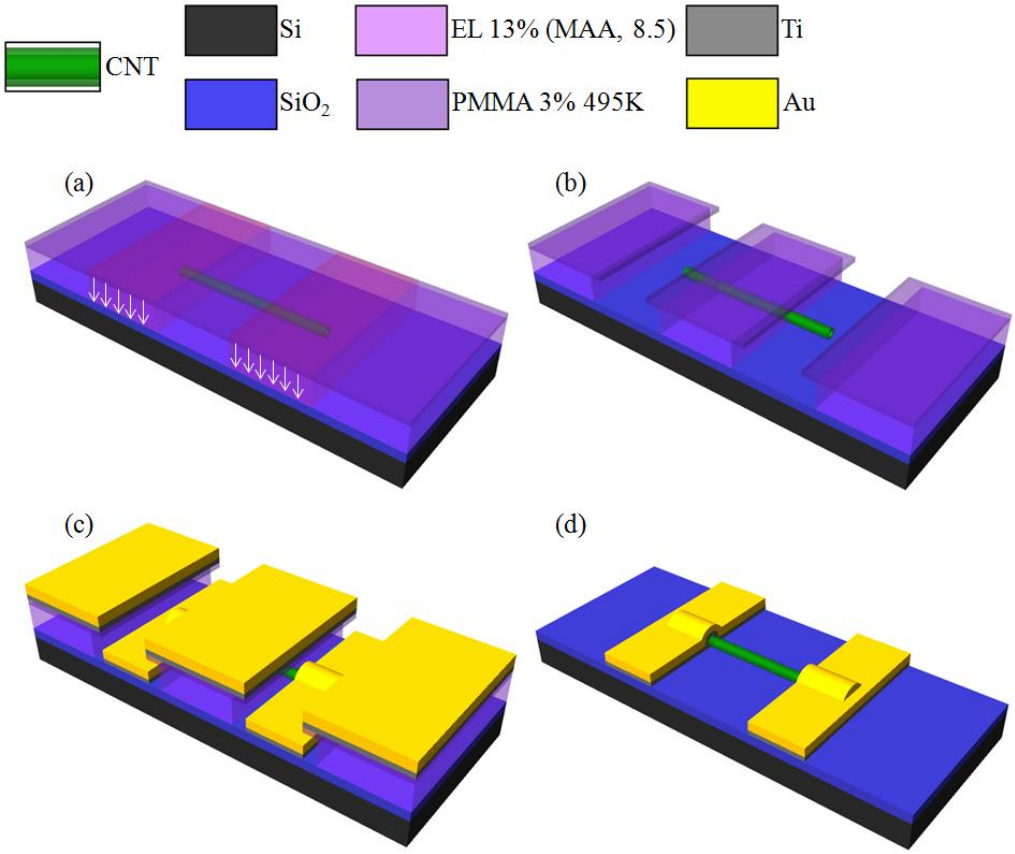

Figure 3.7 *Scheme of whole processing flow for the fabrication of CNTFETs. (a) Sample surface with deposited CNT covered with double layer of organic resist, predesigned pattern is irradiated with a beam of electrons. (b) After development, an opening is left in the resist. (c) Metal is evaporated on top of the substrate. (d) The remaining resist is removed and the metal is left at the predesigned positions*.

3.2 Characterization of CNTFETs

All of the type of samples prepared (*i.e.* either from a Nanointegris suspension, or from the CVD method), were electrically characterized in order to initially check the type of tube conductivity (metallic or semiconducting) and/or the quality of contacts. For further experiments only semiconducting devices are chosen that have also reasonable *on* state current level. All experiments were performed at room temperature in ambient conditions, using a measuring set-up described in the next paragraph.

3.2.1 Principle of electrical measurements

Two electrical systems were used to measure the CNT devices. Figure 3.8a shows a schematic configuration for measuring a CNTFET. In the setup used in this work, a source measure unit (SMU) is connected to the drain terminal and another SMU unit is connected to the back gate terminal (back side of the substrate, here silicon). A SMU allows to source and

measure both current and voltage. The source of the CNTFET is grounded. Using this setup one can change the drain voltage and measure the drain current as a function of the gate voltage. It is also possible to measure the drain current as a function of the gate voltage at a constant drain voltage.

The electrical measurements were also performed by contacting the metal electrodes connected to the CNTs with micromanipulators in a probe station (Figure 3.8b). The probe station is shielded and triaxial cables are used to connect the devices to the measurement equipment to ensure a minimum electrical noise. For the CNTFETs, a Signatone H-100 Probe Station is used with the devices exposed to air during measurement. The devices were characterized using a DAQ system built with: sensor, DAQ device (NI BNC-2090), pre-amplifier (Ithaco) and computer with the acquisition software (LabView).

In both case to avoid damaging the device, it is important to limit the compliance current of the voltage source to about 1 μA.

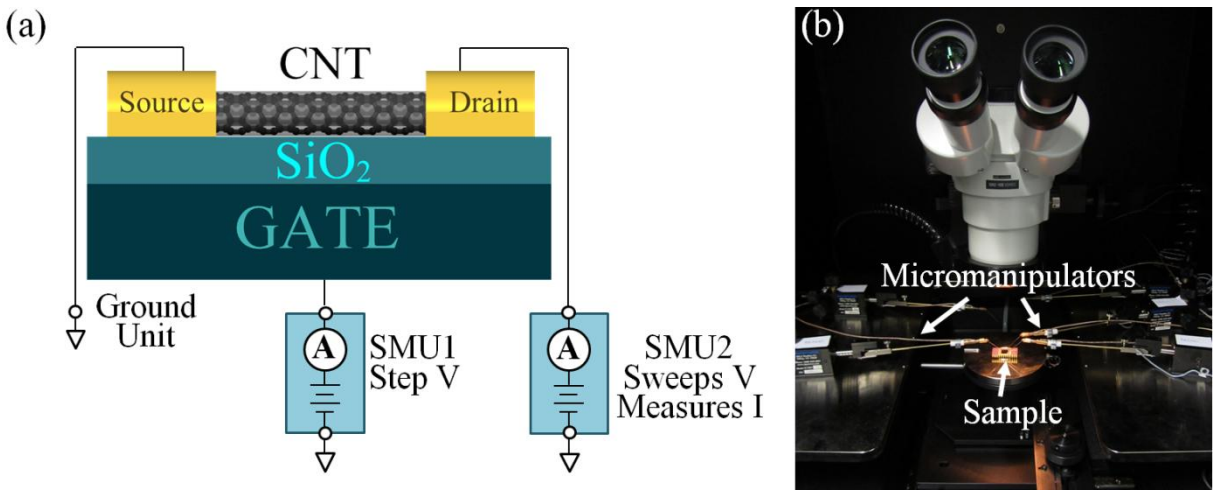

Figure 3.8 *Current-voltage measurements. (a) Circuit diagram for measuring I(V) characteristics of a CNTFET. (b) Photography of the experimental setup. Three micromanipulators are connected respectively to the drain electrode, the source and gate located on the circuit board with the CNTFET sample from one side and from the other side to a semiconductor analyzer - a DAQ system built with: sensor, DAQ device (NI BNC-2090) and computer with the acquisition software.*

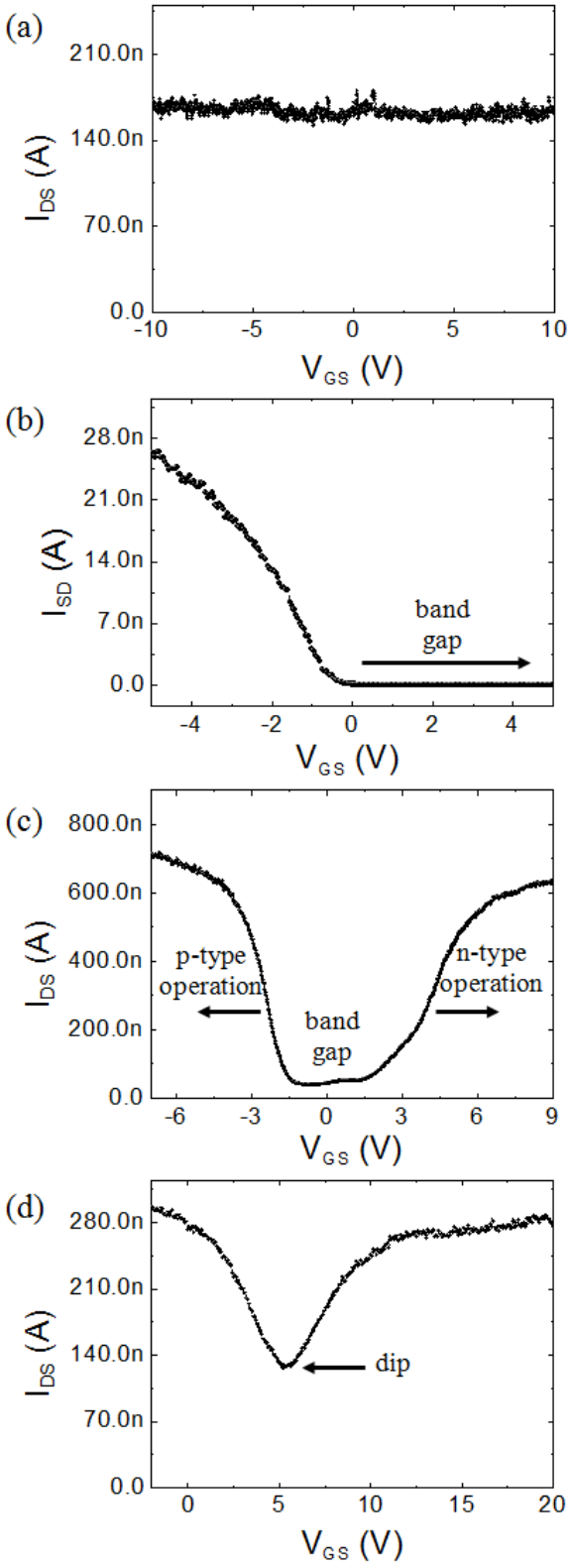

Figure 3.9 *Examples of electrical measurements on devices made from CCVD grown nanotubes at* $V_{DS} = 100\ mV$. *(a) Device characteristics typical for metallic CNT. (b) Semiconducting CNTFET characteristic showing p-type behavior. The device turns off for* $V_{GS} > 0$. *(c) Characteristics of an ambipolar CNTFET with operation in the p-type, band gap and n-type regions. The device conducts at* $V_{GS} = 0$ *and the n-type region is slightly less conductive than the p-type region. (d) Characteristic of device with small –bandgap. The conductance at* $V_{GS} > 0$ *is slightly lower than at* $V_{GS} < 0$.

3.2.2 Transport characterization

The characterization method of all the devices is as follows: a small bias V_{SD} (typically $100\ mV$) is applied to the source, and the I_{DS} current is measured at the drain while sweeping the gate voltage V_{GS}. The examples of conducted measurements for back-gate CNTFETs are presented in Figure 3.9a-d. An example of typical $I_{DS}(V_{GS})$ characteristic for a metallic nanotube is presented in Figure 3.9a, where one can see a constant electrical current with respect to V_{GS}. It should be mentioned that most of the fabricated CNTFETs were found to be *p*-type and the example of $I_{DS}(V_{GS})$ characteristic is shown in Figure 3.9b. We have also observed characteristics typical for ambipolar device (Figure 3.9c) and for device with a small band gap (Figure 3.9d). In this last case one can see that the device does not switch off completely. Such a behavior is attributed to a quasi-metallic CNT with a deformation, structural defect or a large diameter.[7]

3.3 QD deposition

CdSe/ZnS NCs with measured diameters of 4 and 6 nm and an absorption peak at 500 and 620 nm respectively, were purchased from MKNano (product references: MKN-CdSe/ZnS-T500 and MKN-CdSe/ZnS-T620). The core–shell type CdSe/ZnS QDs were prepared by using a colloidal method, and the detailed synthetic procedure for the core–shell QDs was described in **Chapter 2, 2.1.2 Quantum dot synthesis** section. Nanocrystals were drop-casted from the as-received colloidal dispersion in toluene. AFM was used to ensure for the presence of single or few NCs along the nanotubes (Figure 3.10).

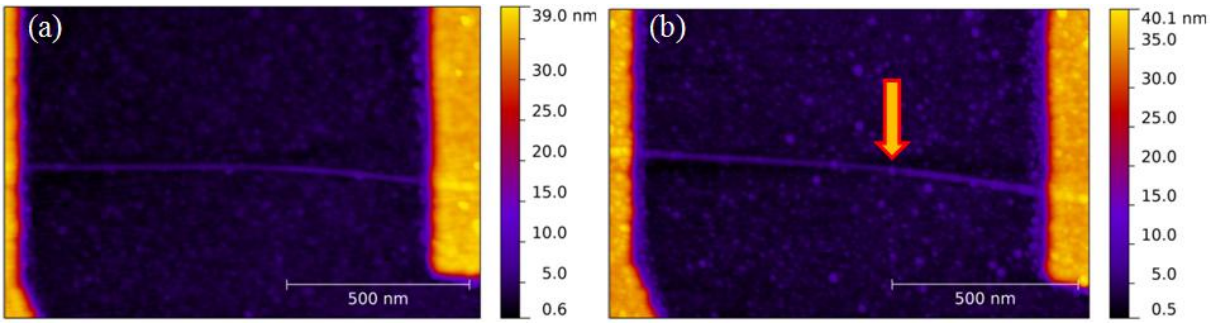

Figure 3.10 *AFM image of CNTFET before (a) and after (b) colloidal CdSe/ZnS nanocrystals deposition.QD diameter ~ 4nm.*

3.3.1 Fluorescence experiments

The optical blinking of the colloidal nanocrystals was verified in two configurations: for NCs deposited on SiO_2 and NCs deposited directly on carbon nanotubes (in the same way as in the case of experiment shown in Chapter 4). In the first case a CdSe/ZnS NCs (6 nm in diameter) were deposited onto a bare SiO_2 layer, whereas the second sample consisted of 4 nm CdSe/ZnS NCs deposited onto a NanoIntegris carbon nanotube carpet (the fabrication details are available elsewhere[8]). A sketch of the two samples is shown in Figure 3.11a and d.

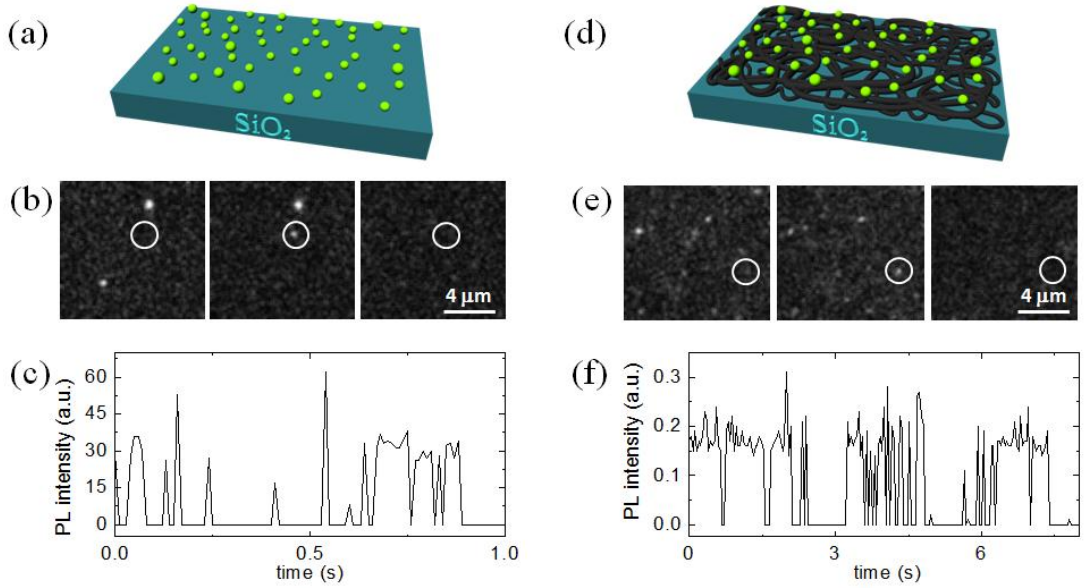

Figure 3.11 *Schematics of the samples used for fluorescence experiments, with (a) 6 nm CdSe/ZnS NCs deposited onto SiO_2 and (b) 4 nm CdSe/ZnS NCs deposited onto a NanoIntegris nanotube carpet. (b) and (e) Fluorescence images showing the NC blinking (a highlighted NC is shown in each case for sake of illustration). (c) and (f) Examples of fluorescence time traces for each sample.*

Optical images were acquired by M. Popoff at Institut de Biologie de Lille, on a Zeiss Elyra P1 inverted optical microscope equipped with a high-speed EMCCD Andor Xion camera (Ref. DU-897D-CSO-#BV-461). The samples were placed on glass-bottom dishes (WillCo-dish, WillCo Wells B.V.) and imaged at 300 K. For each sample, more than 400 frames were acquired. The laser excitation wavelength was 561 nm (although excitation could also be achieved with a laser at 488 nm). A long-pass filter (Zeiss LP570) was used to filter the excitation light and to collect the photons emitted by the blinking dots. The exposure time was 6 ms for the first sample (with a reduced image size of 64×64 pixels) and 40 ms for the second sample (512×512 pixels). The NC blinking is illustrated from a set of three fluorescence images (Figure 3.11b and e for the first and second samples, respectively). The image analysis was performed using ImageJ software (http://imagej.nih.gov/ij/). The mean

intensity of a dot was extracted using the particle detection algorithm on a region of interest for each frame. An illustration of the recorded fluorescence time traces is shown in Figure 3.11c and f.

3.4 Issues in the nanofabrication of coupled QD-CNTFET devices

In the above sections we presented the process, enhanced in design and in precision, of the fabrication of functional nanodevices based on CNTs. To illustrate difficulties in nanofabrication we encountered, below we show most critical issues that we have overcome.

One of the issues is the purity of used samples (both the substrate and the CNTs). The presence of any contaminants in the vicinity of CNTFET channel would cause tube current switching. One of the reasons of substrate contamination was bad surface protection during silicon wafer dicing process, which was made in order to receive smaller samples, manageable for further fabrication steps. The solution to this problem was to coat the silicon wafer with a thick PMMA protective layer (typical thicknesses $> 1\mu m$). After dicing, samples were sonicated for 10 min in acetone and then in IPA. Also to remove the contaminant molecules of resists, cleaning solvent residues - they were further cleaned in UVO-Cleaner® (model 42). The absorption of short-wavelength UV radiation excites and/or dissociates the organic contaminants in photo-sensitized oxidation process.[9] Figure 3.12 presents the AFM image of sample surface before (a) and after (b) UVO cleaning process (typical time of sample exposure ~ 10 min). One can see that the method proved to be an effective and fortunately non-invasive for the carbon tubes[10] yet it did not help to remove the uneven coating from the tubes surface.

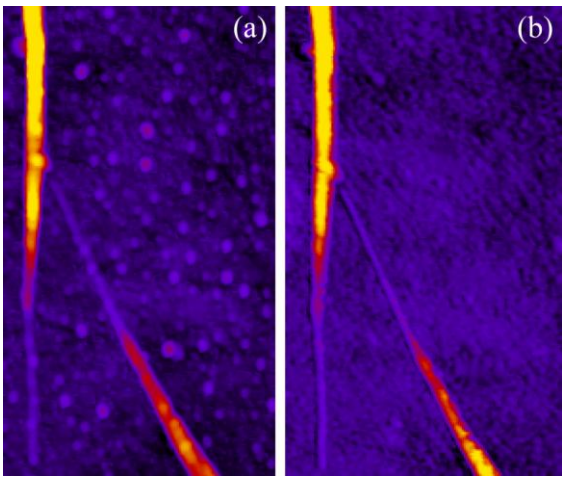

Figure 3.12 *Purity of the substrate and carbon nanotubes. (a) AFM image of contaminated surface with IsoNanotubes (99%) purchased from NanoIntegris, before UVO cleaning. (b) AFM image of the surface*

cleaned using the UVO method. The topography image z-scale was set to 15 nm to enhance the topographic features in the vicinity of the CNTs.

The adjustment of the duration of different processes during nanodevice fabrication was also problematic. Figure 3.13a shows the AFM image of the deformed contact electrodes. The deformation was formed after e-beam lithography step, while immersing the sample in developer (MIBK/IPA) few seconds longer than the regular time. The exposed resist was removed from the substrate, but solvent proved to be sufficiently strong to enlarge the interface.

Figure 3.13b presents the AFM image of CNT connected to electrodes after failed lift-off process. The sample was removed from the SVC® solvent too early, so the unexposed resist and excess metal was not completely removed.

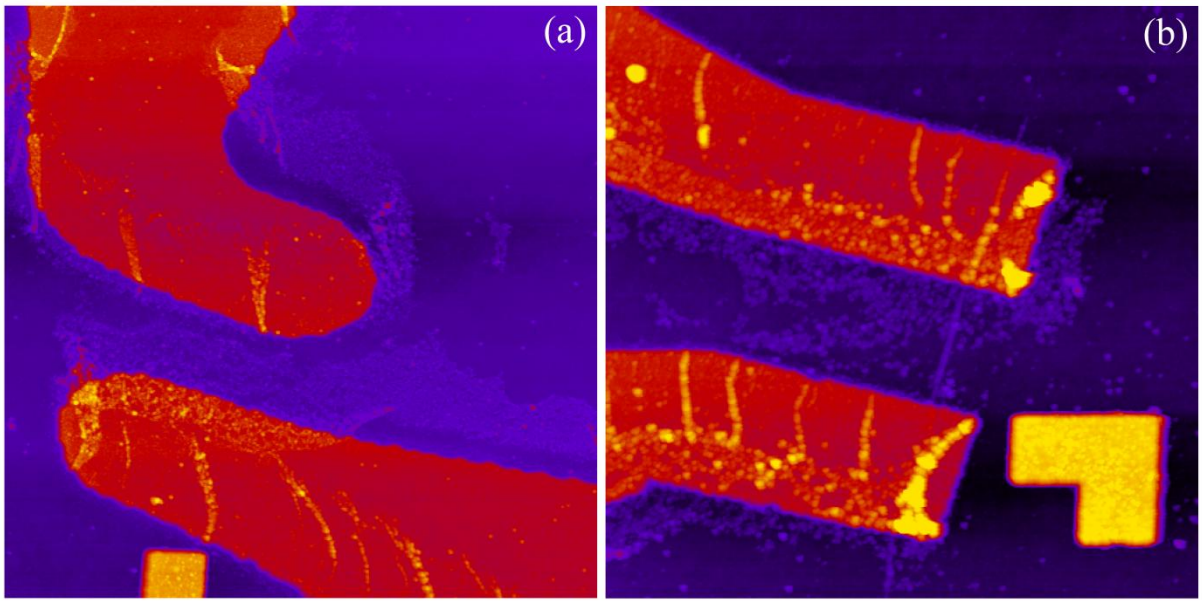

Figure 3.13 *Sample development and lift-off. (a) AFM image of deformed electrodes contacted to CNT. The deformation was formed while immersing the sample in developer few seconds longer than the regular time. (b) AFM image of CNT connected to electrodes after failed lift-off process. The sample was removed from the SVC® solvent too early, so the unexposed resist and excess metal was not completely removed.*

As was mentioned before, the electrodes were designed individually for each fabricated CNTFET. Unfortunately from all contacted nanotubes per sample, only approximately one-fourth were properly connected to electrodes. Figure 3.14 shows two unsuccessful attempts of connecting CNTs, (a) in case when too many tubes were contacted to electrodes and (b) in case when, as a result of poor e-beam marker positioning, no tube was connected.

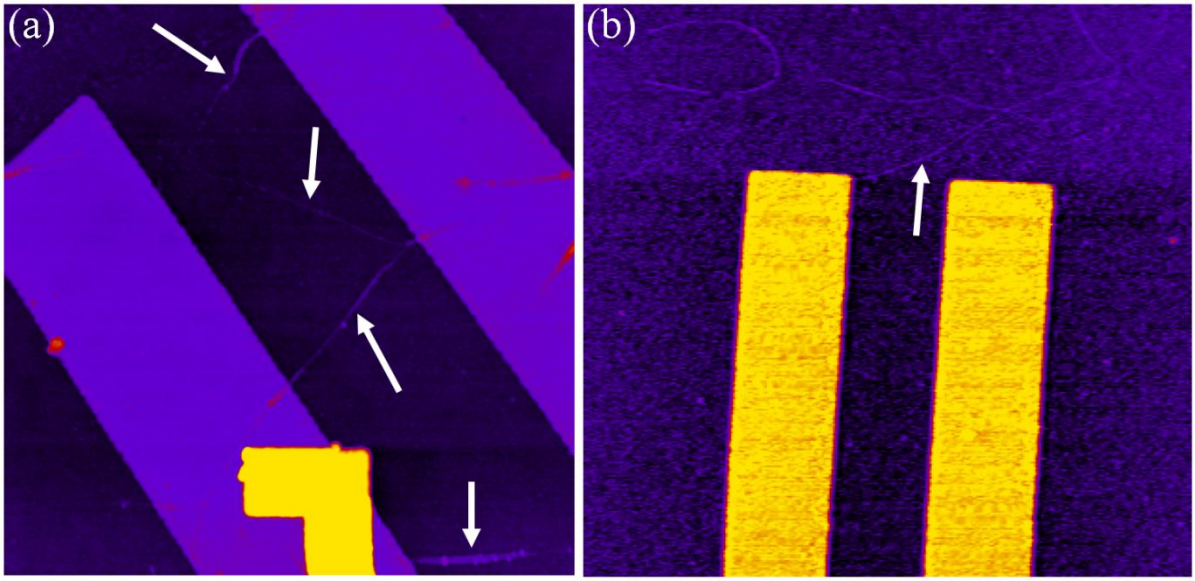

Figure 3.14 *CNTs localization and contacts fabrication. (a) AFM image of metal electrodes contacted to four instead of one individual CNT. (b) AFM image of CNT connected to just one electrode as a result of poor e-beam marker positioning.*

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Chapter 4

Charge blinking statistics of semiconductor nanocrystals revealed by carbon nanotube single charge sensors

In this chapter, we investigate the charge fluctuation dynamics of individual CdSe/ZnS semiconductor NCs using CNTFETs as single charge sensors. CNTFET devices have already been investigated at low temperature to demonstrate and detect single charging events in metallic NCs[1,2] and to probe the charging spectrum of semiconductor NCs.[3] In addition, they have also been used as few-electron/single-electron charge sensors at room temperature in ambient air[4] and, very recently, in a liquid environment.[5] In the present work, to study the charge fluctuation dynamics of individual semiconductor NCs, we probed individual semiconductor NCs attached to CNTFETs with a sub-microsecond time resolution and with single-charge sensitivity at room temperature. Electrical blinking manifests as a pronounced random telegraph signal (RTS) associated with upper and lower current levels through the CNTFET devices. The RTS analysis shows clear power law temporal statistics of upper and lower current states (i.e., statistics varying as $\tau^{-\alpha}$, with α in the range of $\approx 1-3$) and a Lorentzian current noise power spectrum. The spectroscopic analysis of the coupled NC-CNTFET devices shows that the electrical blinking is due to the charging of the NC defect states with a measured charging energy of $E_c \geq 200\, meV$. This origin of the electrical blinking suggests that the power-law statistics of optical blinking is governed by the population statistics of the underlying NC trap states.

4.1 Coupled nanocrystal - nanotube field-effect transistor devices

Samples were fabricated using standard nanofabrication techniques (see **Chapter 3**). We worked both with *(i)* single-walled carbon nanotubes directly grown by chemical vapour deposition on oxidized silicon substrates and with *(ii)* commercial semiconducting nanotubes (99 % pure semiconducting single-walled carbon nanotubes, NanoIntegris). Atomic force

microscopy (AFM) images and electrical characteristics of the CNTFETs were systematically measured prior to and after deposition of semiconducting nanocrystals to ensure the deposition of individual semiconducting NCs along the CNTFET channels. To guarantee that the observed power-law electrical blinking statistics did not depend on the CNTFET device fabrication, we also studied two types of devices, labeled **Device A** and **Device B** hereafter, which were fabricated using two different approaches (Figure 4.1).

Device A consisted of a CNTFET constructed from single-walled nanotubes grown by chemical vapour deposition on a $1\,\mu m$ thick SiO_2 layer thermally grown from a p-type degenerately doped silicon wafer. Source and drain contacts were deposited by Ti ($5\,nm$) / Au ($45\,nm$) metal evaporation, and a CNTFET channel of $\approx 1\,\mu m$ length was defined. CdSe/ZnS NCs with $4\,nm$ outer diameter (purchased from MKNano) were subsequently deposited by being dropcast onto the fabricated CNTFET.

Device B consisted of a CNTFET constructed from commercial semiconducting nanotubes (purchased from NanoIntegris) deposited from a dichlorobenzen suspension onto a thermally oxidized silicon wafer. This device exhibits geometry similar to that of Device A, except for the difference in the SiO_2 thickness ($300\,nm$ thick thermal dioxide) and the deposited NC size (CdSe/ZnS NCs with measured $5\,nm$ outer diameter, purchased from MKNano).

4.2 Device characterization and random telegraph signal

The typical devices (including the CNTFET wiring) are sketched in Figure 4.1a. AFM images of Device A and B are provided in Figure 4.1b-c respectively. The upper panels present topography images before NCs deposition and bottom panels – after deposition. The images show the presence of an isolated NC adsorbed along the CNTFET channel, as a result of the NC deposition process (see the white arrow as a guide to the eye). A careful check shows that observable features along the CNTFET channel after NC deposition either *(i)* already occur at the very same position along the nanotube in the AFM picture before NC deposition; or *(ii)* have been slightly moved along the nanotube during the drop-casting NC deposition process.

The methods of devices characterization are described in **Chapter 3**, **3.2 Characterization of CNTFETs** section.

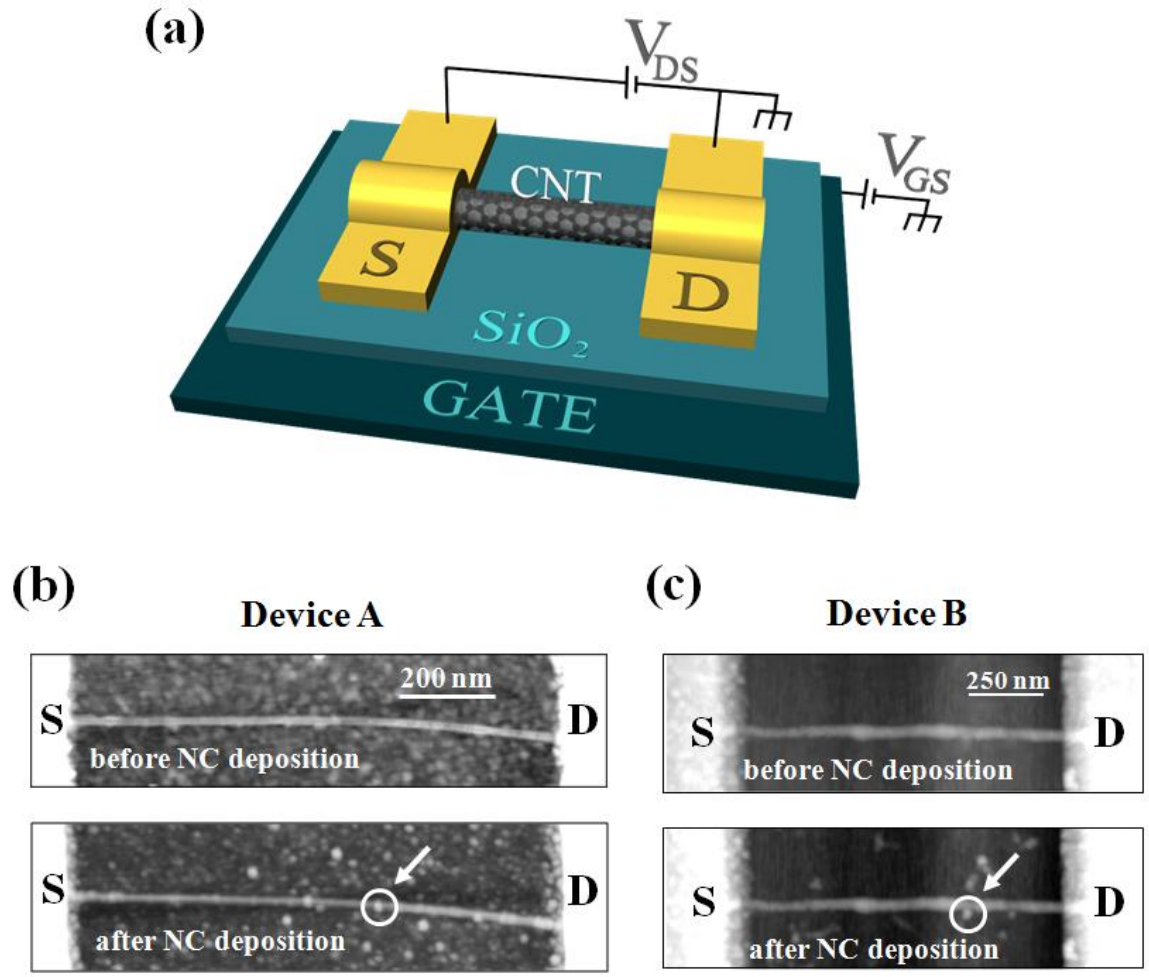

Figure 4.1 *Coupled nanocrystal - nanotube field-effect transistor devices. (a) Schematics of CNTFETs fabricated on a SiO_2 layer grown on a doped silicon wafer acting as a back-gate. A bias V_{DS} is applied between source (S) and drain (D) contacts. The current through the nanotube I_{DS} is probed as a function of the back-gate bias V_{GS}. (b) AFM topography images of Device A, built from a semiconducting nanotube grown by CVD on a 1 μm thick SiO_2 layer before (top panel) and after (bottom panel) NC deposition (here 4 nm outer diameter CdSe/ZnS NCs, see text). (c) AFM images of Device B constructed from commercial semiconducting nanotubes (purchased from NanoIntegris) deposited from a dichlorobenzene suspension onto a thermally oxidized silicon wafer (the layer thickness is 300 nm). The highlighted feature corresponds to a NC (height 5nm) identified after the deposition process. The topography image z-scale was set to 15 nm so as to enhance topographic features in the vicinity of the CNTFET channel. Source and drain contacts therefore correspond to the saturated S and D white areas in topography images.*

The electrical characteristics $I_{DS}(V_{GS})$ of Device A before and after NC deposition are shown in Figure 4.2a. Unlike previously published experiments at low temperature,[2,3] which reveal a series of individual jumps in the $I_{DS}(V_{GS})$ characteristics ("hole per hole" charging of the NC during the back-gate bias sweep), such jumps are not clearly observed here. This lack of observed jumps is a consequence of our devices operating at room temperature and in ambient air, whereas previous experiments have been performed at temperatures much smaller than the dot interlevel spacing (i.e., for $k_B T \ll \Delta E$, in which $\Delta E \approx$ 25-50 meV[3]

accounts for the electrostatic and quantum confinement energies) and were performed in vacuum.

The main feature observable in the electrical characteristics is a "flattening" of the $I_{DS}(V_{GS})$ curve after a NC is attached to the device (i.e., a gradual decrease of the current level with increased negative back-gate bias V_{GS}), as shown in Figure 4.2a. This feature is typical of coupled NC-CNTFET devices and is the global result of charge transfer from the CNTFET to its environment upon the application of a back-gate after NC deposition.[3] An increased noise (Figure 4.2a) is also visible in the $I_{DS}(V_{GS})$ characteristics after NC deposition compared to the characteristics prior to NC deposition. To isolate this effect, current vs. time $I_{DS}(t)$ data were recorded at fixed V_{GS} and are shown in Figure 4.2b. The data clearly indicate that NCs induce a pronounced random telegraph noise in the CNTFET current, where higher (H) and lower (L) current levels (with mean values of $3.6\,nA$ and $1.5\,nA$, respectively) can unambiguously be identified at fixed gate bias. The two-level intermittency between the H and L levels corresponds to the semiconductor NC carrying N and $N+1$ charges, and is unambiguously revealed by the histogram of the current levels in the $I_{DS}(t)$ data, as shown in Figure 4.2c. This RTS signal can be used to study the "electrical blinking" of the NCs using the CNTFETs as charge detectors.

A similar behaviour is observed for Device B, as shown in Figure 4.3. Device B topography is shown in Figure 4.1c, where the circled area corresponds to a NC (measured height $\approx 5\,nm$) identified after the deposition of CdSe/ZnS NCs. The transfer characteristics $I_{DS}(V_{GS})$ of the device before and after NC deposition are shown in Figure 4.3a for a source-drain bias $V_{DS} = 150\,mV$. A very similar flattening effect in the $I_{DS}(V_{GS})$ is observed compared to that observed for Device A. We also recorded the back-and-forth back-gate bias sweeps for the $I_{DS}(V_{GS})$, showing an increased hysteresis in the presence of the NC along the CNTFET channel. This effect is not expected from a purely reversible NC charging effect, but may be due to charge exchange processes with slow time-scale dynamics at the NC/SiO_2 substrate interface[6] upon changes in the gate bias V_{GS}. Current time traces $I_{DS}(t)$, shown in Figure 4.3b after the NC deposition ($V_{DS} = 150\,mV$, $V_{GS} = -8\,V$) display a pronounced RTS after the NC deposition, similar to Device A, with lower (L) and higher (H) current levels of $0.8\,nA$ and $1.5\,nA$, respectively. The corresponding histogram is shown in Figure 4.3c.

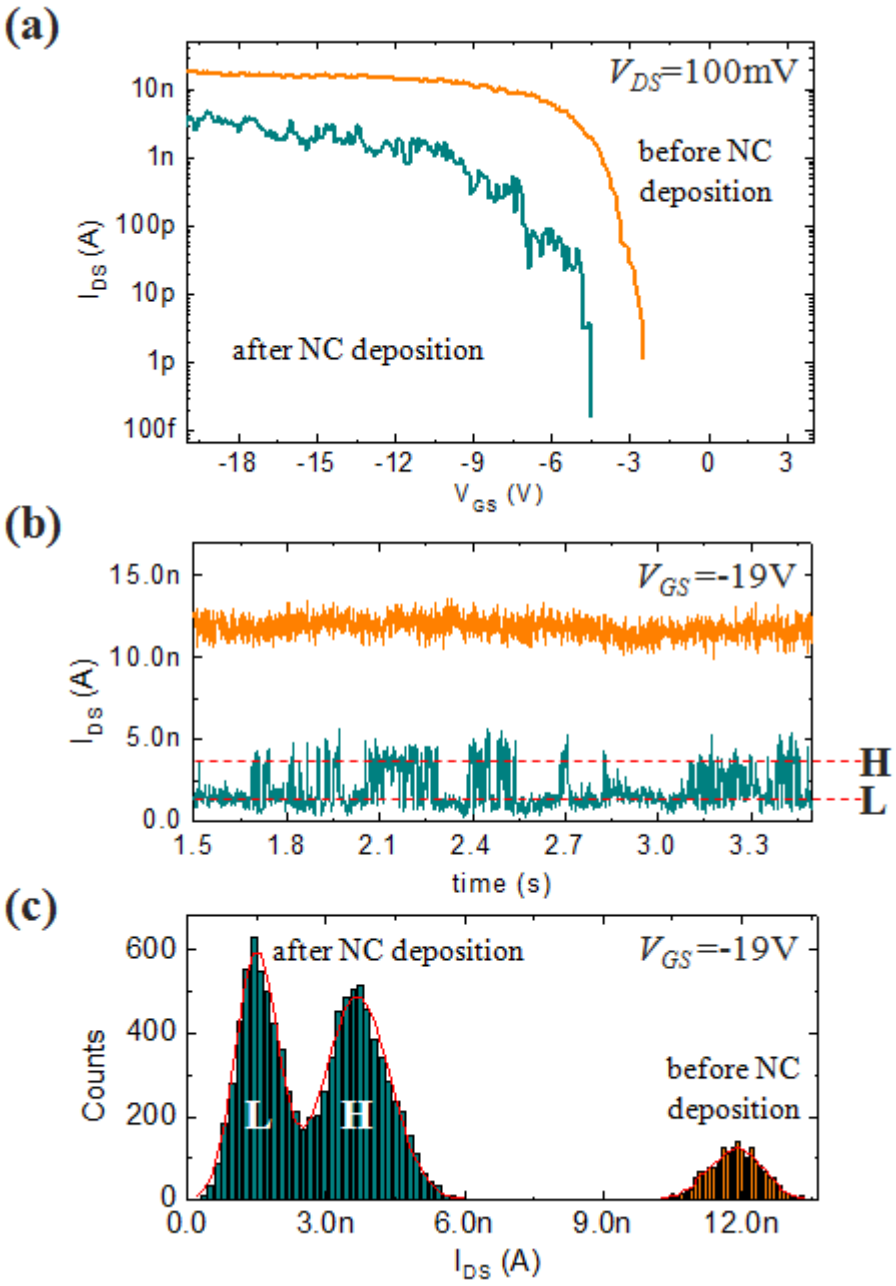

Figure 4.2 *Characterization of Device A. (a) Transfer characteristics $I_{DS}(V_{GS})$ of the CNTFET before (orange) and after (blue) NC deposition. (b) Current time trace $I_{DS}(t)$, recorded at fixed V_{GS}, before (orange) and after (blue) NC deposition. The NC deposition induced a pronounced intermittency between two current levels labeled H (high) and L (low). (c) Corresponding current histograms before and after NC deposition. The current histogram probed before NC deposition is also shown for the sake of comparison.*

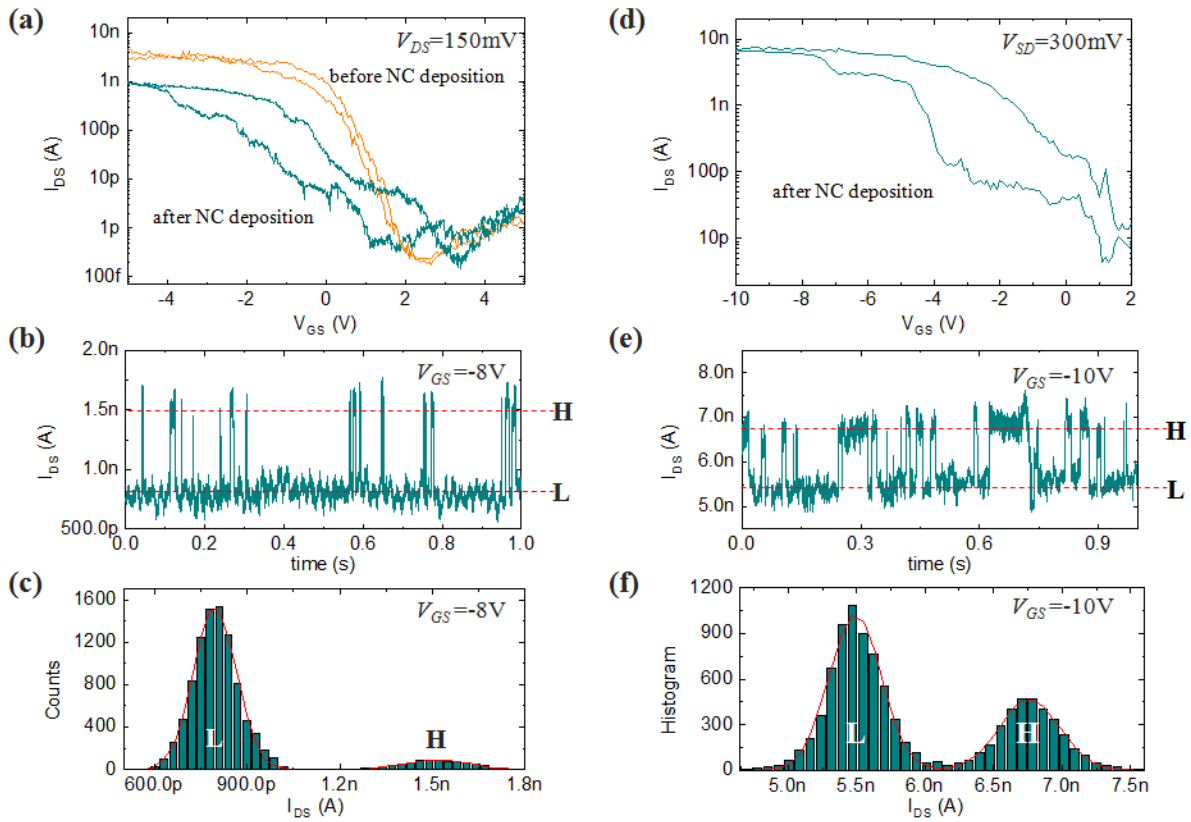

Figure 4.3 *Characterization of Device B. (a) and (d) Transfer characteristics $I_{DS}(V_{GS})$ of the CNTFET (here, in dry atmosphere) before (orange) and after (blue) NC deposition, using V_{DS} = 150 mV and V_{DS} = 300 mV respectively. The hysteresis upper branches correspond to gate bias sweeps towards negative V_{GS}. (b) and (e) Current signal plotted as a function of time $I_{DS}(t)$, at fixed V_{GS} = -8 V and V_{GS} = -10 V after NC deposition, showing two current levels (L and H). The graph also contains here a parasitic current oscillation at 50 Hz. (c) and (d) Current histograms after the NC deposition, corresponding to the graph of $I_{DS}(t)$ shown in (b) and (e) respectively.*

4.3 Nanocrystal charge power-law blinking statistics

To gain insight into the statistics of the charge jumps, we measured the $I_{DS}(t)$ time traces of the devices using a recording bin time of $\tau_{min} = 1\ ms$ and a total integration time of $\tau_{max} = 5\ s$ for Device A and $\tau_{min} = 0.1\ ms$ and $\tau_{max} = 1\ s$ for Device B to explore NC charging dynamics on shorter time scales. An example of raw experimental $I_{DS}(t)$ traces are shown in Figure 4.4a for Device A and 4.5a for Device B. Idealized time traces were also computed (Figure 4.4b and 4.5b for Device A and B respectively), where the introduction of a threshold enables the transformation of the experimental $I_{DS}(t)$ traces into a pure RTS signal between L and H levels with amplitudes 0 and 1, respectively. The current peaks were fitted and a minimum between the fitted curves was the value of L and H separation. From the idealized time traces, we derive the statistics of the levels L and H, which are plotted as a function of the event duration in Figure 4.4c and 4.5c. This plot shows a clear power-law

behavior for the NC charging events (probabilities $P_{L,H}(\tau)$ for the high/low events proportional to $\tau_{L,H}^{-\alpha_{L,H}}$). The associated measured exponents are $\alpha_L = 1.3 \pm 0.3$, $\alpha_H = 2.1 \pm 0.3$ (Device A), and $\alpha_L = 3.1 \pm 0.4$, $\alpha_H = 1.3 \pm 0.4$ (Device B). The average times spent on the levels *L* and *H* are provided in Figure 4.4c and 4.5c, but will not be further analyzed because they depend on the bin time τ_{min} and total integration time τ_{max} for power-law behaviour. The α values may also depend, to a smaller extent, on τ_{min} and τ_{max}. These effects have been previously studied.[7,8,9,10] However, our purpose here is to clearly demonstrate the existence of power-law behaviours in the charging dynamics of NCs - as shown in Figure 4.4c and 4.5c - rather than to provide a refined measurement of the α coefficients.

Furthermore, we computed the power spectrum noise (in A^2/Hz) from the $I_{DS}(t)$ time traces for Devices A and B, which are shown in Figure 4.4d and 4.5d. The power spectra of current time traces were obtained numerically, using OriginPro 8.1 software application for data analysis, starting from the real-time experimental data. This approach is common in characterizations of the RTS arising in field-effect transistors with small (sub-μm) dimensions[11,12] as well as for RTS in CNTFETs at low temperatures.[13] This approach has also been used to characterize the power-law exponents at hand in blinking experiments.[14] Here, we observe for both samples a clear Lorentzian shape for the current trace power spectrum, i.e., a saturation plateau below the corner frequency f_c and a $1/f^2$ slope (slope -2 in the logarithmic representation of Figure 4.4d and 4.5d). We extract from these graphs the RTS corner frequency f_c from a Lorentzian fit to the current trace power spectrum. This yields $f_c = 5\,Hz$ for Device A and $f_c = 48\,Hz$ for Device B. The corner frequencies differ significantly, but they are also related to the average times $\langle\tau_{L,H}\rangle$ spent on each of the levels *L* and *H* and therefore depend both on $\alpha_{L,H}$ and on the choice of the bin time τ_{min} and maximum integration times τ_{max}.7'8'9'[10] However, the observation of such a clear Lorentzian spectrum from electrical experiments is striking compared, e.g., to nanowire field-effect transistor devices with an RTS caused by a few oxide traps,[12] for which the Lorentzian shape of the RTS power spectrum appears as a deviation from or shoulder to the dominant $1/f$ background noise. We associate this effect with the large amplitude of the RTS observed in our experiments (up to a factor 2 between the *L* and *H* current levels) compared to the work of Ref [12] (i.e., less than 10% difference between the *L* and *H* current levels, at most) and to CNTFET for which RTS has been observed in the absence of quantum dots (see **Annex B: Analysis of RTS in CNTFETs**).

An example of statistical analysis of the RTS noise for Device A before QD deposition is shown in Figure 4.6, where the current noise power spectrum follows the $1/f$ law (Figure 4.6b).

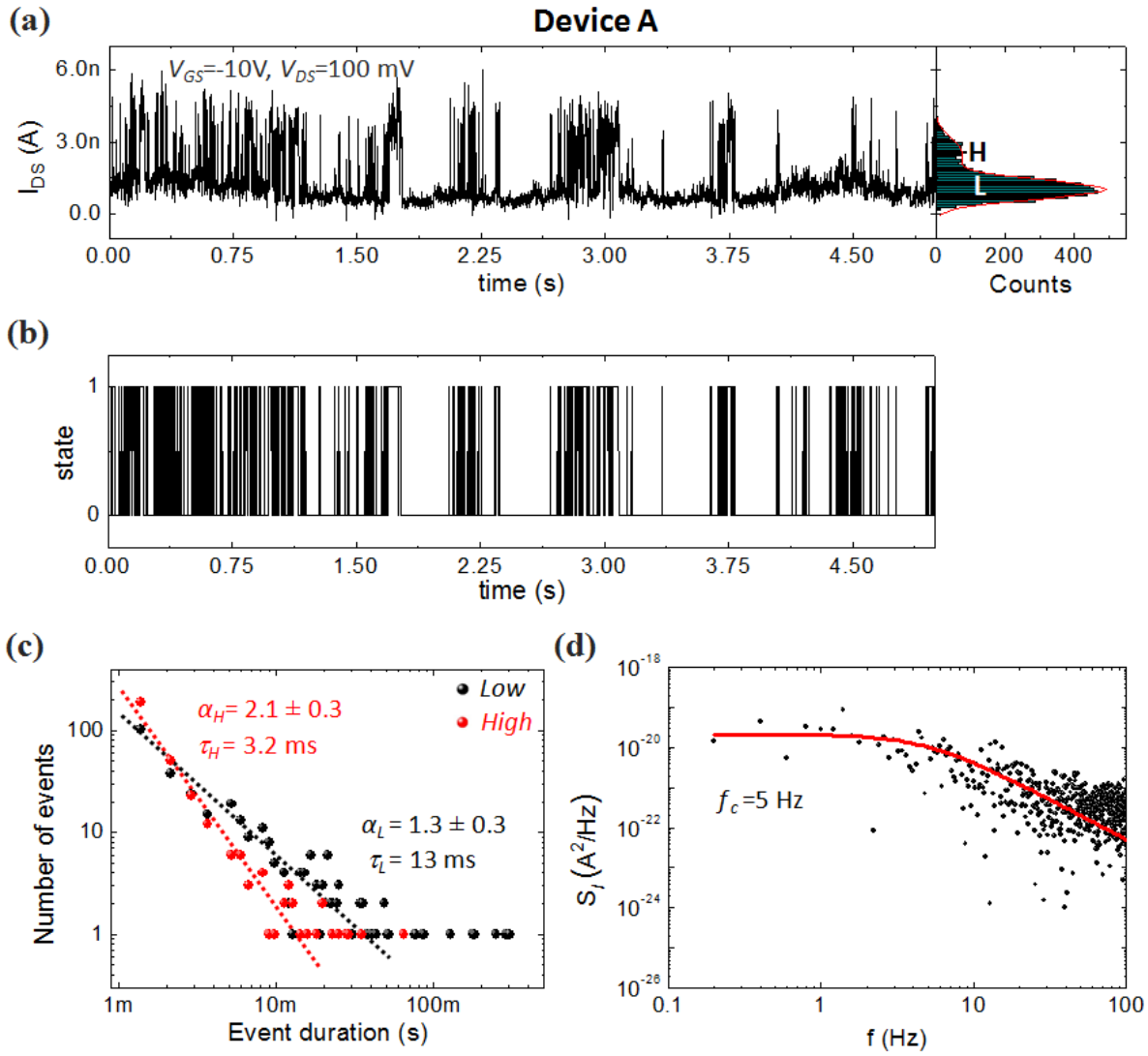

Figure 4.4 *Statistical analysis of the RTS noise for Device A. (a) Experimental time traces of the current I_{DS}, recorded at fixed gate bias (V_{GS} = -19 V and V_{GS} = -10 V for Devices A and B, respectively). Current histograms are provided to show the separation between the L and H levels. Time bin and integration times are respectively τ_{min}=1 ms and τ_{max}=5 s. (b) Idealized time traces, where the introduction of a threshold enables the transformation of the experimental $I_{DS}(t)$ traces into a pure RTS signal between L and H levels with amplitudes 0 and 1, respectively. (c) Statistical analysis of the time spent in the L and H levels, showing power-law behaviours (see text). (d) Power spectra of the experimental $I_{DS}(t)$ time traces, showing lorentzian shapes with well-defined corner frequencies f_c and $1/f^2$ slopes (the red lines are lorentzian fits to experimental data).*

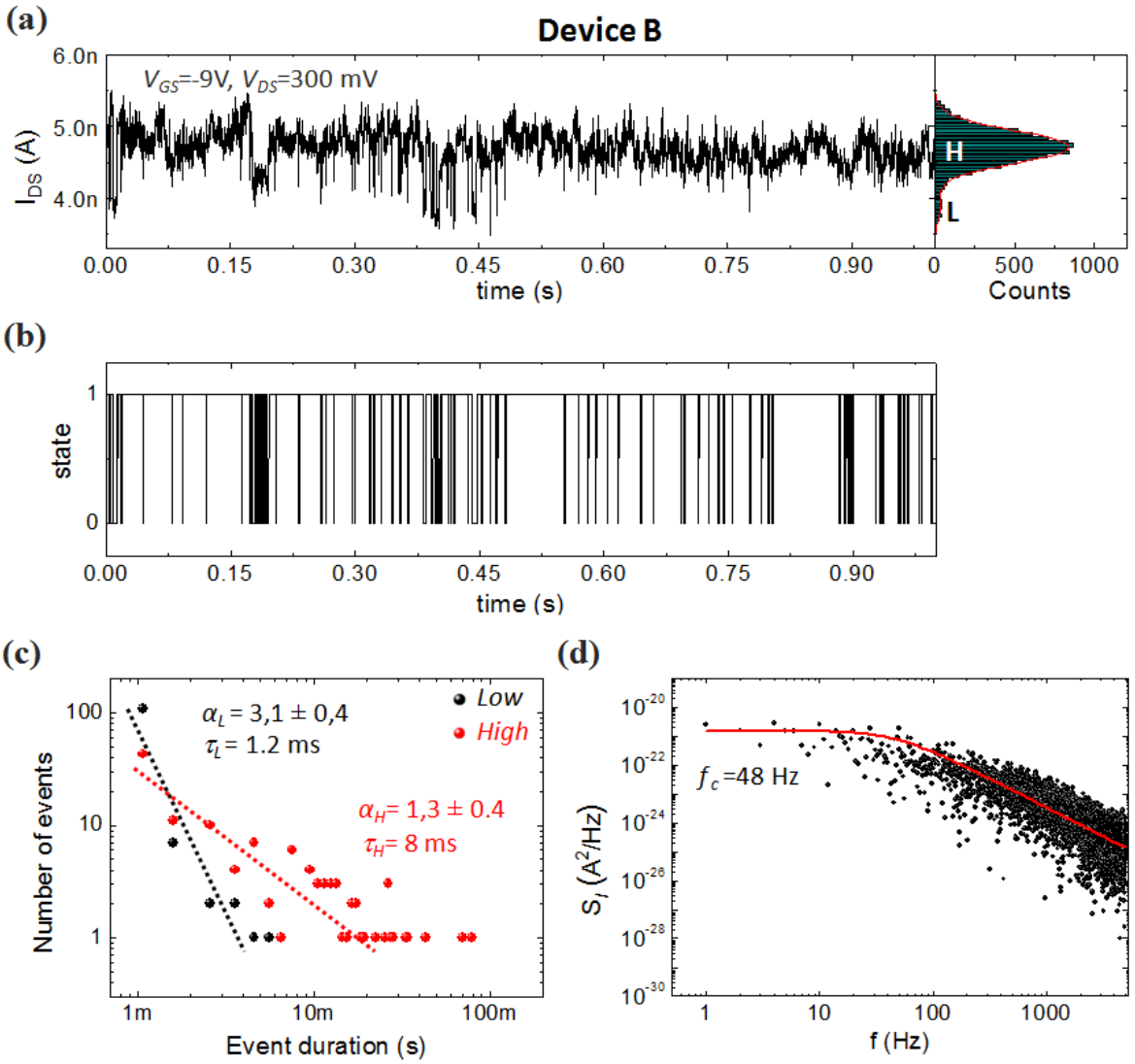

Figure 4.5 *Statistical analysis of the RTS noise for Device B. (a) Experimental time trace of the current I_{DS}, recorded at fixed gate bias (V_{GS} = -9 V). Current histograms are provided to show the separation between the L and H levels. Time bin and integration times are respectively τ_{min}=0.1 ms and τ_{max}=1 s. (b) Idealized time trace, where the introduction of a threshold enables the transformation of the experimental traces into a pure RTS signal between L and H levels with amplitudes 0 and 1, respectively. (c) Statistical analysis of the time spent in the L and H levels, showing power-law behaviours. (d) Power spectra of the experimental $I_{DS}(t)$ time traces, showing a lorentzian shape with well-defined corner frequency f_c and $1/f^2$ slope (the red line is a lorentzian fit to experimental data).*

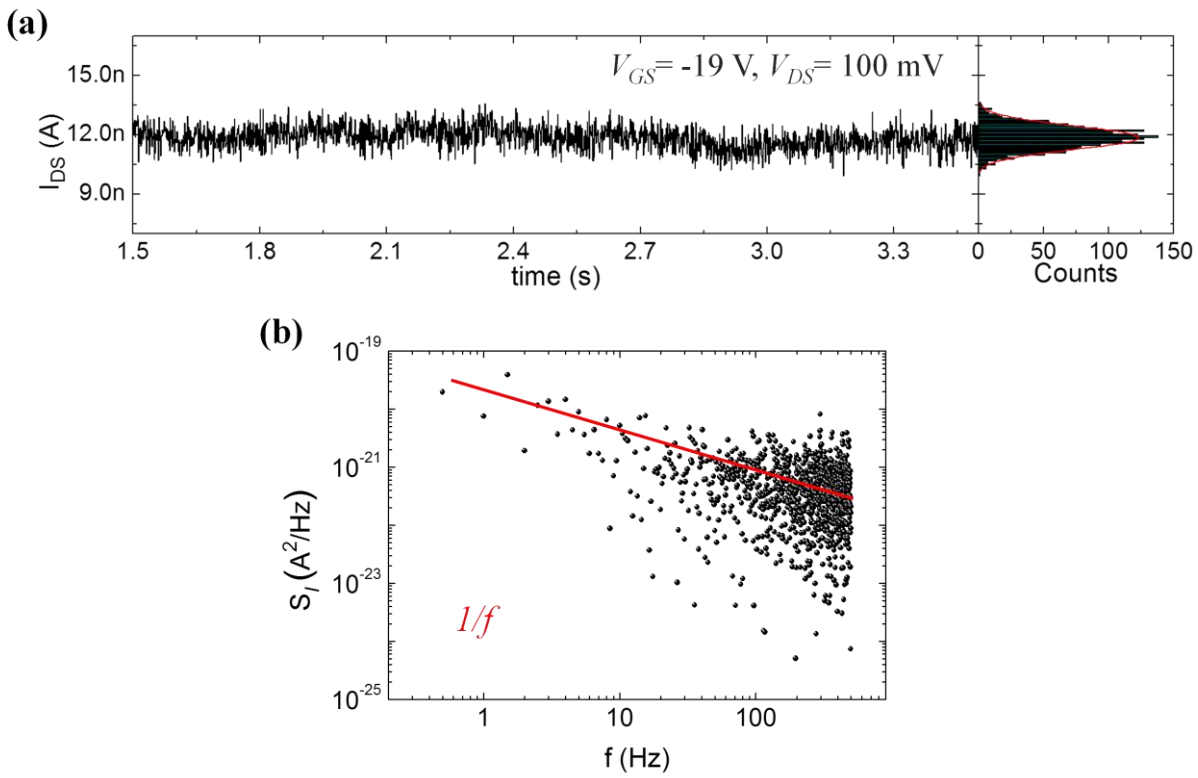

Figure 4.6 *Statistical analysis of the RTS noise for Device A before QD deposition. (a) Experimental time trace of the current I_{DS}, recorded at fixed gate bias (V_{GS} = -19). Current histogram is provided to show one current level. Time bin and integration times are respectively τ_{min}=0.1 ms and τ_{max}=5 s. (b) Power spectrum of the experimental $I_{DS}(t)$ time trace, showing $1/f$ slope (the red line is $1/f$ fit to experimental data).*

The observation of a power-law behaviour is consistent with the optical blinking of similar CdSe NCs capped with ZnS, as observed from fluorescence experiments,[7] or for different colloidal NCs.[8,14,15] We experimentally verified that the NCs used in this work exhibited fluorescence blinking (see **Chapter 3**, **3.3.2 Fluorescence experiments** section) either on insulators or when deposited onto a dense carbon nanotube layer.[16] Notably, however, electrical blinking in our work was observed in the dark. Only the NC electrostatic charge state is indeed probed here, in the absence of optical excitation, which separates electrostatic issues from the optical processes associated with NC blinking.[15] These experiments are, to our knowledge, the first demonstration of electrostatic experiments in which a power-law statistical distribution of the NC charge state is observed. Indeed, pioneering work probing single charge fluctuations of CdSe NCs by electrostatic force microscopy[17] suffered from intrinsic bandwidth limitations and could not reveal NC blinking statistics. Previous experiments based on single charge detection using CNTFETs were neither focused on NC blinking nor on the statistical aspects of charge fluctuations.[3,5] Finally, recent work has focused on current blinking in the transport through colloidal dots, either

from transport measurements using static electrodes[18] in the case of CdSe/CdS NCs or using conductive AFM in the case of PbS or PbSe dots.[19] Such measurements revealed ON and OFF current states with power-law statistics or a Lorentzian power spectrum, but did not demonstrate experimentally the fluctuation statistics of the single charge state involved in their interpretation.

4.4 NC-CNTFET spectroscopic analysis: Trap-state charging energy

To further assess the physical mechanisms associated with the NC electrostatic blinking, we performed a spectroscopic analysis of the devices to measure the charging energy E_c associated with the RTS (see **Chapter 2**, **2.3 Electronic properties of coupled QDs and CNTs** section). In Figure 4.7, we show the RTS properties of Device A probed as a function of the CNTFET back-gate, which is varied by ΔV_{GS} steps of 2 or 3 V. Such large ΔV_{GS} steps were chosen to explore the full V_{GS} range of the device in which the RTS could be observed (see the discussion hereafter). The observed RTS histograms are presented in Figure 4.7 (the insets illustrate the associated current jump events over a reduced time range) for V_{GS} values where the RTS could be observed. We verified that the RTS could not be identified beyond the V_{GS} range of Figure 4.7 in the recording conditions. Figure 4.7 shows that the RTS definitely varied upon changes to the back-gate bias, although a monotonous trend for the relative histogram weights of the L and H current levels was not observed. This effect likely arises because the steps in ΔV_{GS} induce shifts of the NC electrostatic potential larger than the NC charging energy. This effect can also be explained, in part, by the fact that the application of a sudden change in V_{GS} can alter the global device gating properties;[2] alternatively, it can be explained by the presence of different trap centers in the charging process for different V_{GS} (see the discussion hereafter).

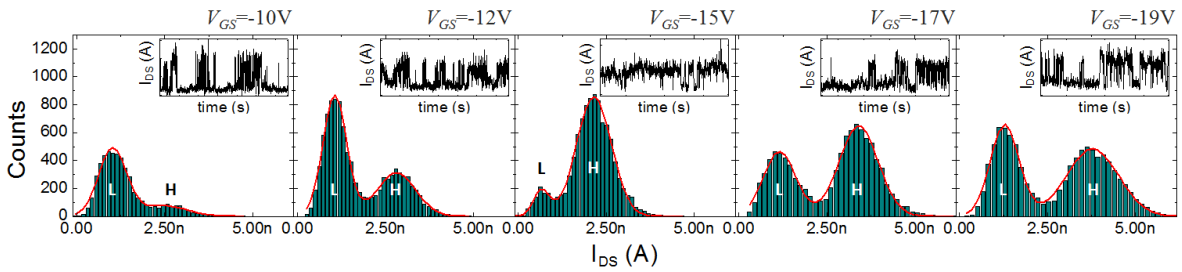

Figure 4.7 *Device A. (a) Histograms of I_{DS} current levels recorded as a function of the back-gate bias V_{GS}. The device current was recorded for each plot using a recording bin time τ_{min}=1 ms . The total recording time is τ_{max}= 5 s (V_{GS} = -10 V) or τ_{max} = 10 s (V_{GS} = -12 V to -19 V). Insets show the RTS of the current traces.*

To estimate the NC charging properties from the RTS data in Figure 4.7, we followed the approach used to model the RTS induced by trap states in early sub-µm Si FET devices.[20] This approach relates the ratio between the trap capture and emission times to the trap charging energy. This model describes the statistics of the trap center in equilibrium with the Fermi level of the electronic device channel (see the schematics in Figure 4.8a). This model can be adapted here to compute the energy difference between the NC electronic state with energy E_T involved in the RTS process, and the local Fermi level E_F in the CNTFET, from the average times spent on the L and H current levels,

$$\frac{\langle \tau_L \rangle}{\langle \tau_H \rangle} = exp\left[\frac{E_T - E_F}{k_B T}\right]. \quad (4.1)$$

We used this equation and the average times $\langle \tau_L \rangle$ and $\langle \tau_H \rangle$ derived from the RTS plots in Figure 4.6 to analyze the variations of $E_T - E_F$ when the back-gate bias V_{GS} was swept in Device A. Results (at room temperature T=300K) are shown in table 4.1.

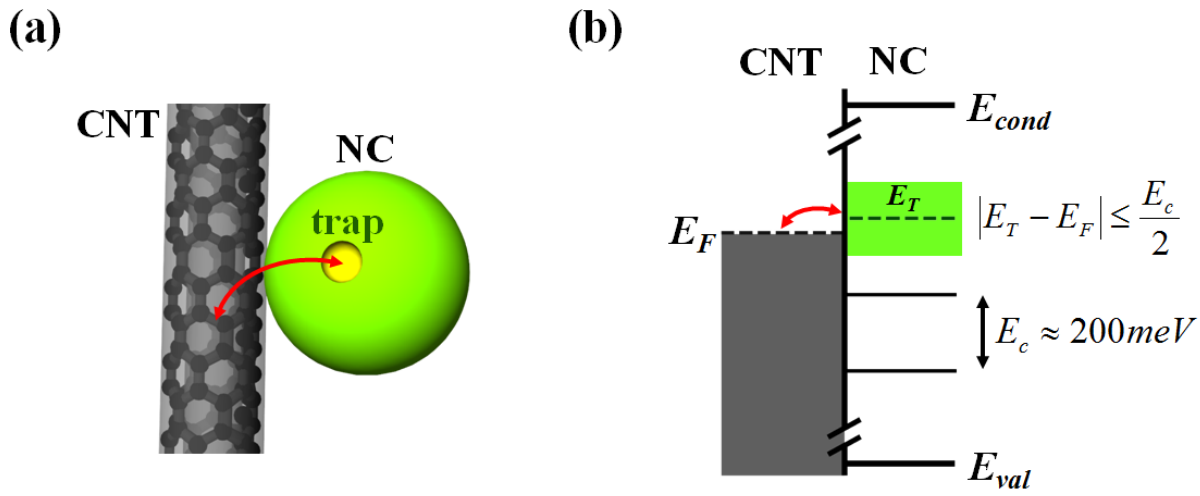

Figure 4.8 *(a) Schematics of the charge transfer between the CNTFET and the NC trap. (b) Energy diagram showing charge transfers between the CNTFET (treated as a metal electrode) and NC band-gap traps with charging energy E_c. E_{cond} and E_{val} refer to the NC conduction and valence bands, respectively. In this picture, we only take into account the trap electrostatic charging energy E_c by assuming that the energy difference between trap levels ΔE_T stays small as compared to E_c ($\Delta E_T \ll E_c$, see text).*

The trap charging energy shows a large dispersion with positive and negative values and a maximum absolute value of $|E_T - E_F|_{max} \approx 70\ meV$. To explain these variations, we propose that the RTS is due to the charging of a NC band-gap trap with energy E_T, in equilibrium with the CNTFET channel (here, in a metallic representation) with local Fermi level E_F. The charging process is illustrated in Figure 4.8a together with a simplified energy diagram provided in Figure 4.8b, in which we consider that the trap charging energy E_c is

much larger than the energy difference ΔE_T between two different traps (this quantity is therefore not represented in Figure 4.8b). This leads to a simple picture of energy levels organized in the form of a "ladder" separated by E_c ($E_c \gg \Delta E_T$ prevents the simultaneous charging of several traps). In this most simple picture, the energy mismatch between E_F and E_T is necessarily limited by $E_c/2$, as shown in Figure 4.8b. Using the measured value of $|E_T - E_F|_{max} \approx 70\, meV$, this yields $E_c \geq 2|E_T - E_F|_{max} \approx 140\, meV$. Such a value is large compared to the charging energy already observed in the case of metal NCs ($E_c \approx 5\, meV$)2 or to that reported for CdSe NCs of similar size ($E_c \approx 20 - 40\, meV$).3 It is, however, consistent with the charging of NC band-gap trap states and is furthermore in agreement with our observation of two-level RTS at $300\ K$.

V_{GS}	$\langle\tau_L\rangle/\langle\tau_H\rangle$	$2(E_T - E_F)$	$\Delta V_{GS}(L-H)$	$e\Delta V_{GS}(L-H)/\beta$
-10 V	16.00	**144 meV**	0.80 V	**215 meV**
-12 V	0.90	**-6 meV**	0.83 V	**225 meV**
-15 V	1.80	**30 meV**	0.80 V	**215 meV**
-17 V	0.14	**-100 meV**	1.00 V	**270 meV**
-19 V	0.47	**-38 meV**	1.00 V	**270 meV**

Table 4.1 *Analysis of the RTS noise in Device A at room temperature (T=300K). The table shows the operation back-gate bias V_{GS}, the ratio between the average times $\langle\tau_L\rangle$ and $\langle\tau_H\rangle$ (data from Figure 4) and the trap energy with respect to the CNTFET Fermi level $E_T - E_F$ (see text); the back-gate voltage difference between the current levels I_L and I_H associated with the L and H states (obtained from the transfer characteristics of Device A without NC) and the corresponding charging energy obtained using the lever arm β = 3.7 taken from Ref.* 3

To support this claim, we estimated E_c using an alternative method. We consider for each gate voltage V_{GS} the values of the L and H average current levels, as extracted from the histograms in Figure 4.7. We then use the CNTFET characteristics of Device A prior to NC deposition to estimate the back gate voltage shift $\Delta V_{GS}(L-H)$ corresponding to the switch between the two current values. Raw values of $\Delta V_{GS}(L-H)$ are presented in table 4.1 and exhibit relatively stable values in the range of $0.8\, V - 1\, V$. These values, however, refer to the voltage applied to the CNTFET back-gate, which is related to the real NC electrostatic energy by a lever arm β. This lever arm has been estimated as $\beta = 3.7$ in a previous work3 for a CNTFET device geometry (i.e., channel length and oxide thickness, see **Chapter 2**, **2.4**

Electronic properties of coupled QDs and CNTs section) similar to that of Device A. We therefore extract the NC charging energy as $e\Delta V_{GS}(L-H)/\beta$, as provided in table 4.1. Remarkably, these values are rather constant (in the $215-270\,meV$ range) as a function of V_{GS} and remain above the $140\,meV$ value extracted from the maximum value of $E_T - E_F$ in the RTS analysis. This result is fully consistent with the fact that $E_c \geq 2|E_T - E_F|_{max}$ in the trap-charging RTS model. It is also consistent with the fact that the measured $E_T - E_F$ values shown in table 4.1 were randomly observed to be positive or negative, which is a consequence of the fact that the back-gate bias steps applied to the device $e\Delta V_{GS}(L-H)/\beta$ are larger than E_c. These results support our model of a two-level RTS associated with the population of NC band-gap traps with charging energy $E_c \approx 200\,meV$ for Device A.

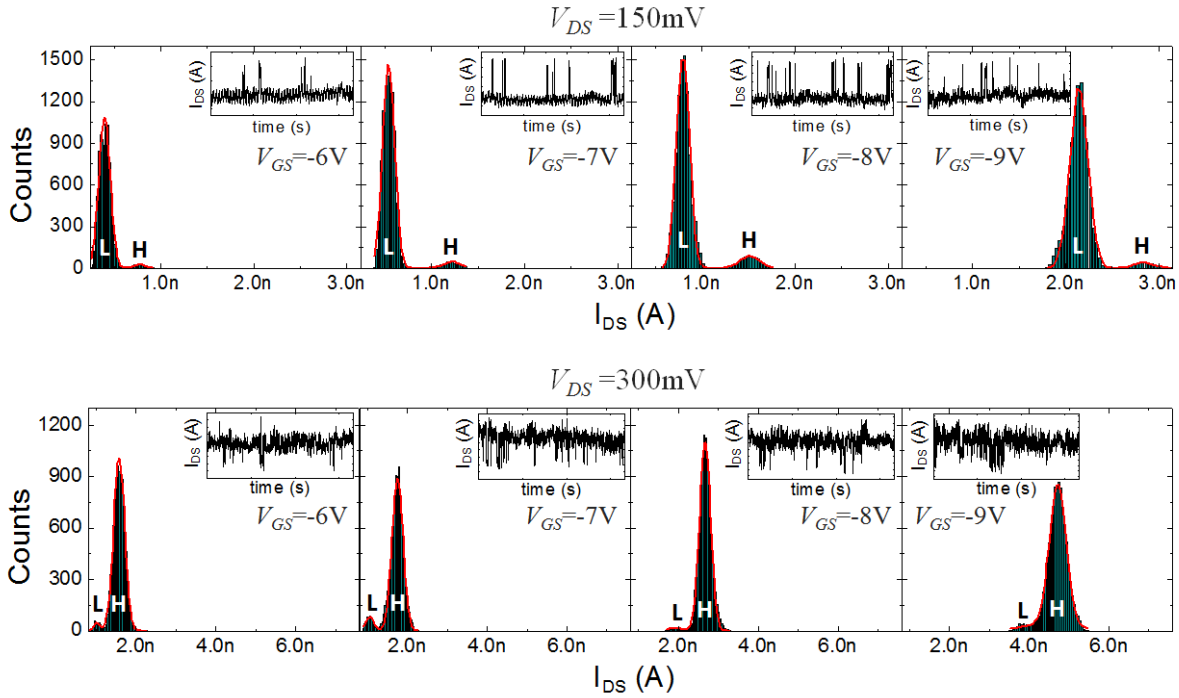

Figure 4.9 *Device B. Histograms of I_{DS} current levels recorded as a function of the back-gate bias V_{GS}, plotted (top) for a source drain bias V_{DS} = 150 mV and (bottom) for V_{DS} = 300 mV. The device current traces have been recorded for each plot using a recording bin time τ_{min}= 0.1 ms and a total recording time τ_{max}= 1 s. Insets illustrate the RTS of current traces over a 1 s duration.*

The same methodology is now applied to Device B, for which histograms of the current traces are shown in Figure 4.9 for $V_{DS} = 150\,mV$ (top) and V_{GS} varied by steps of $1\,V$. The data are shown in the V_{GS} range for which RTS could be observed under the measurement conditions. We used a recording bin time $\tau_{min} = 0.1\,ms$ and total recording time $\tau_{max} = 1\,s$. For each V_{GS} value, the drain bias was switched to $V_{DS} = 300\,mV$; the corresponding data are shown in Figure 4.9 (bottom). The behaviour of Device B differs substantially from that of Device A because the histograms appear as strongly peaked on the L peak only for

$V_{DS} = 150\ mV$, irrespective of the back-gate bias V_{GS}. However, the histograms are strongly peaked on the H peak for $V_{DS} = 300\ mV$. In both cases, the back-gate action is almost insignificant, which suggests a non-equilibrium population of the electronic state responsible for the observed RTS (see the discussion hereafter). The previous analysis using equation (4.1) should therefore be handled with care. However, as shown in table 4.2, we computed the same data as for Device A to determine the effective charging energy at hand in the blinking process observed in Device B. The results show values of $2|E_T - E_F|$ in the $120 - 200\ meV$ range. Similarly as for Device A, we also estimated the back-gate voltage shift $\Delta V_{GS}(L - H)$ corresponding to the jump in current levels between the H and L states from the device transfer characteristics $I_{DS}(V_{GS})$ obtained for $V_{DS} = 150\ mV$ (data from Figure 4.3a) or $V_{DS} = 300\ mV$ (data from Figure 4.3d). This analysis provides an average value for $\Delta V_{GS}(L - H)$ of $\approx 670\ mV$. However, to interpret this value in terms of the NC charging energy, we need to use a lever arm β' (not β) because of the smaller oxide thickness ($300\ nm$ for Device B compared to $1\ \mu m$ for Device A). In the absence of existing data in the literature for this device geometry, we compute β' as a function of: $\beta' = (C_A/C_B)\beta$, where C_A and C_B refer to the nanotube / back-gate capacitance for Devices A and B, respectively. We thus obtain $\beta' = \beta/(1.25 \pm 0.1) = 2.95 \pm 0.25$ (using measured nanotube diameters of $2\ nm$ and $3 \pm 1\ nm$, respectively, for Devices A and B), which gives the measured charging energy $e\Delta V_{GS}(L - H)/\beta'$ listed in table 4.2. An average charging energy $E_c \approx 225\ meV$ can be deduced, which satisfies $E_c \geq 2|E_T - E_F|_{max}$.

We therefore obtain a similar picture as for Device A, where the RTS can be understood as the charging of a trap with charging energy in the $\approx 200\ meV$ range. However, the trap charging here is not activated by the device back-gate bias V_{GS} but rather by a change of V_{DS}. We attribute this behaviour to an out-of-equilibrium trap state population, in contrast with Device A, whereas the observed change as a function of V_{DS} may tentatively be assigned to the trap charging by hot carriers from the CNTFET channel under increased V_{DS} values.

V_{GS}	$\langle\tau_L\rangle/\langle\tau_H\rangle$	$2(E_T - E_F)$	$\Delta V_{GS}(L-H)$	$e\Delta V_{GS}(L-H)/\beta'$
-6 V	40	**190 meV**	0.48 V	**160 meV**
-7 V	22	**160 meV**	0.75 V	**250 meV**
-8 V	11	**126 meV**	0.82 V	**280 meV**
-9 V	82	**172 meV**	0.77 V	**260 meV**
-6 V	0.042	**-164 meV**	0.55 V	**185 meV**
-7 V	0.079	**-132 meV**	0.60 V	**200 meV**
-8 V	0.020	**-200 meV**	0.62 V	**210 meV**
-9 V	0.066	**-140 meV**	0.79 V	**270 meV**

Table 4.2 *Analysis of the RTS noise in Device B at room temperature (T=300K). The tables refer to V_{DS} =150 mV (top) and V_{DS} =300 mV (bottom). The table shows the operation back-gate bias V_{GS}, the ratio between the average times $\langle\tau_L\rangle$ and $\langle\tau_H\rangle$ (data from Figure 4.9) and the corresponding $E_T - E_F$ value as derived from Eq. 1 (see text); the back-gate voltage difference between the current levels associated with the L and H states (obtained from the transfer characteristics of Device B without NC in Figure 2) and the corresponding charging energy obtained using the lever arm β' = 2.95 (see text).*

More generally, our analysis is focused on the attribution of the RTS to trap states, which is consistent with the following arguments. First, and in contrast with the NC spectroscopy previously performed using CNTFETs at low temperature,[3] we do not observe single charge events out of a back-gate bias "gap" corresponding to the NC band-gap , but rather within a given range of V_{GS} values, with amplitude of $9\,V$ (Device A) and $3\,V$ (Device B). Both amplitudes, when normalized by the lever arm β, fall within the expected band-gap of the CdSe/ZnS NCs derived from the absorption peak at $500\,nm$ (Device A) and $620\,nm$ (Device B). Second, the value of the NC charging energy estimated in our work for the two samples and two methods was observed to be close to $200\,meV$. This value is large compared to the charging energy associated with NC quantum levels[3] ($40-50\,meV$ at most, including quantum confinement and Coulomb effects), which underscores the fact that, in our work, the NC charging is not due to the charging of the NC valence-band quantum levels. Finally, the charging mechanism observed is likely close to the trap charging observed from scanning-tunneling spectroscopy experiments on CdSe/ZnS NCs,[21] in which a trap charging energy of $65\,meV$ has been observed. Notably, this value has been measured for a NC in the gap between a metal tip and an Au substrate. This metallic environment may explain the smaller

trap charging energy as compared to our work, in which the NCs were inserted into an electronic device constructed on an insulating layer.

Discussion

We finally discuss in the following our results on a more general basis, and in view of future developments. This covers the aspects of NC trap state spectroscopy and the link of our results with NC blinking experiments and optical spectroscopy. As for the spectroscopy of NC trap states, our electrostatic results indicate that NC trap states are energetically distributed within the NC bandgap, but this analysis should be extended in order to determine the actual trap energy distribution. Hence, we determined in the case of Device A that the RTS associated with traps occurs within a back-gate bias range $\Delta V_{GS} = 9\,V$, corresponding to a $2.4\,eV$ NC energy range using the lever arm $\beta = 3.7$ for Device A. This range is remarkably close to the NC band-gap as deduced from the NC absorption peak at $500\,nm$. Our measurements are thus consistent for Device A with a picture in which traps would be energetically distributed over the whole NC band-gap (in that case, the NC band edges can also be deduced from the charge spectroscopy). This picture is however different for Device B, for which traps are observed on a reduced energy range of $\Delta V_{GS} \approx 3\,V$ ($\approx 1\,eV$ NC energy range, using a lever arm $\beta' = 2.9$ adapted to the oxide thickness for Device B). This value is smaller than the expected NC band-gap, suggesting that traps are localized over a reduced band of energies within the band-gap, in agreement with typical photoluminescence experiments.[22] One cannot so far position here this band of energy with respect to the NC conduction valence and conduction band edges. One way to circumvent this using CNTFET charge detectors would be to lower the device temperature, as done in previous work,3 and to probe the onset of single electron jumps associated with the charging of the NC conduction and valence electronic states. Such an analysis is however restricted to low temperatures due to the much reduced charging energies ($E_c \approx 20 - 40\,meV$) associated with these states, which cannot be observed at room temperature. A second aspect would be the determination of the donor or acceptor character of the trap states within the band-gap. Here again, further developments are required, since experiments using CNTFET as charge sensors only provide measurement of relative changes in the NC charge state (i.e. detecting jumps between N and $N + 1$ elementary charges), but not of its absolute charge state N. This type of identification would be likely possible by coupling CNTFET charge sensing with e.g. charge or potential sensing from scanning-probe microscopy, either by Kelvin probe force microscopy or, similarly, by electrostatic force microscopy. The latter technique has been used originally to probe the blinking of a NC from its charge state compared to an HOPG substrate;[17] the former technique has been more recently used to probe the electrostatics of CNTFETs in presence of

few electron charge spots at the vicinity of the device channel, and could be readily extended to probe coupled CNTFET-NC devices such as those of our work. One would here probe directly the electrostatic potential or charge state of a blinking NC with respect to the CNTFET channel potential, and thus provide an intrinsic reference for the NC charge state. It should be noted however that scanning-probe techniques have intrinsic bandwidth limitations, especially while preserving the charge detection sensitivity better than the elementary charge in air at $300K$.[17] This is why we primarily used CNTFETs in our work rather than scanning-probe techniques, to enable single charge detection with a sub-millisecond time resolution to record the NC charge blinking statistics.

Beyond the pure spectroscopic point of view, our work which has evidenced power-law statistics for the NC trap electrostatic charging also points out the role of time fluctuation of trapping centers or fluctuations in the transfer rates towards trapping centers, in line with recent developments in the explanation of the power-law statistics observed in the case of optical blinking.[22,23] This issue might be significant here, and consistent with the fact that in our experiments it was not possible to isolate and tune the L and H statistical weigths accross a given quantum level E_T from the back-gate bias V_{GS}, although other effects such as the CNTFET hysteresis may play also some role. However, this observation likely indicates a role for multiple trap states with fluctuating charging rates, which could be the case e.g. for surface states[24] for which fluctuations in charging by tunneling from the CNTFET channel can be easily envisaged. On a more general level, the coupling of electrostatic and optical experiments, for instance by directly combining NC trap state spectroscopy using nanoscale charge detectors and individual NC fluorescence dynamics would be most interesting, since excitonic issues such as e.g. multiple exciton recombination in NCs seem closely related to their electrostatics.[25]

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Conclusions and perspectives

The aim of this work was to study the electronic properties of coupled semiconductor nanocrystals and carbon nanotubes. For this purpose we experimentally studied single electron transfer through CdSe/ZnS colloidal nanocrystal coupled to a carbon nanotube field effect transistor at room temperature in ambient conditions.

The CNTFETs were fabricated by means of standard nanofabrication techniques. CNTs were directly deposited from organic solution or grown by chemical vapor deposition method on top of a two sets of doped Si wafers, with $300\ nm$ and $1\ \mu m$ thermal SiO_2 layer, respectively. Single CNT was contacted to Ti/Au electrode patterned by electron beam lithography. The NCs were placed along CNT directly from the colloid suspension and were found to be preferentially adsorbed onto nanotubes.

We have observed the charge blinking behaviour of CdSe/ZnS NCs on the basis of their coupling with CNTFETs used as single charge-sensitive electrometers. The random telegraph signal associated with electrical blinking exhibits characteristics typical of optical blinking, *i.e.*, power-law temporal statistics ($\tau^{-\alpha}$, with α in the range of $\approx 1-3$) and a Lorentzian current noise power spectrum. We performed a spectroscopic analysis of the coupled NC-CNTFET devices, showing either a thermal activation or an out-of-equilibrium population of NC trap states, with a measured charging energy of $E_c \geq 200\ meV$, which is attributed to trap states within the NC band-gap. This observation confirms the recently proposed B-type optical blinking mechanism for colloidal semiconductor nanocrystals based on NC trap state population within the NC band-gap.

This work offers the possibility of more sophisticated studies by, *e.g.*, directly combining NC trap state spectroscopy using nanoscale charge detectors and individual NC fluorescence dynamics. The perspectives would be to combine the time-resolved fluorescence and electrostatic experiments using CNTFETs coupled to individual NCs and to perform the measurements at lower temperatures to improve the spectroscopy.

Annex A

Thermal analysis of nanotubes

This annex is related to **Chapter 3**, subsection **3.1.2 CNTs deposition and growth**, where the methods of CNTFETs fabrication are presented. Here we focus on showing the attempts of identification and purification of the excess material coating semiconducting IsoNanotubes (99%) purchased from NanoIntegris using different analytical techniques: Raman spectroscopy and thermogravimetry analysis (TGA) coupled with mass spectrometry (MS). The analysis was acquired together with Djamila Hourlier at IEMN.

TGA is a technique which allows to continuously measure changes in weight resulting from chemical or physical transformations which occur during sample heating. Materials can be analyzed in various environments (vacuum, inert, reducing and oxidizing atmospheres). Two important types of information can be learned: the percentage of weight loss (% $\Delta M/M_0$) and the onset temperature decomposition, which provides data about the chemical composition and structure of the samples.

Our experiments on Nanointegris nanotubes were conducted under a dynamic gas atmosphere at a flow rate of 80 cm^3/min, with a heating rate of 10°C/min. We have used two types of samples: a powder of 99 % pure semiconducting SWNTs (**S21-067**) and the mixture of semiconducting and metallic tubes (**P12E17**). Table A.1 shows the protocol development. Samples were systematically characterized with Raman spectroscopy before and after heat treatment. A confocal microRaman spectrometer (Horiba-Jobin Yvon, LabRam HR) was used to acquire Raman spectra with 473nm excitation laser, and a 100x objective.

Materials	Experiment TGA/MS	Masse used (mg)	Remarks
Mixture of CNTs (P12E17)	3% H_2/Ar	14	
	20% O_2/He	11	The oxidation has been done on the heat treated CNT sample under H_2
	inert He	31	
Semiconducting CNTs (S21-067)	3% H_2/Ar	5	

Table A.1 *Protocol development. TGA experiments were performed under a dynamic gas atmosphere at a flow rate of 80 cm^3/min, with the heating rate of 10°C/min. Samples (purchased from NanoIntegris) were used: powder of 99 % pure semiconducting SWNTs (S21-067) and the mixture of semiconducting and metallic tubes (P12E17).*

Figures A.1 and A.2 illustrate the thermal behavior of P12E17 sample in an inert atmosphere and in oxygen, respectively. It should be noted that there were no significant differences in the TGA patterns between inert (Helium) and reducing atmospheres (3% H_2 in Argon). On heating from room temperature to 500°C, the SWNTs under inert atmosphere (Helium) exhibit a mass loss of ~24% (Fig A.1), while those pre-treated under H_2 (3% H_2 in Argon) and then after annealed under oxidizing atmosphere (20% O_2 in Helium) show a loss less than 2% (Fig A.2). The mass loss is accompanied by the emergence of complex volatile mixture of components, which are carried out of the TGA furnace through a heated capillary into the quadripole mass spectrometer. The decomposition occurs at different steps as pointed out by the various peaks for the same M/z (Figure A.1). The gases evolved contain H_2 at M/z = 2, water at M/z = 18, CO_2 at M/z = 44, 28, and hydrocarbon molecules C_xH_y at 15, 27, 28, 43. All these volatile species can be related to the decomposition of the surfactant added in the aqueous solution containing CNTs. As we do not know the exact formula of the surfactants used by Nanointegris, it is difficult to assign all the M/z observed during the heat treatment.

Under oxygen atmosphere, the combustion of pre-treated CNTs startet around 450 °C and ended at 700°C, the CNTs were burnt. The main gases evolved are H_2O, CO_2 and CO.

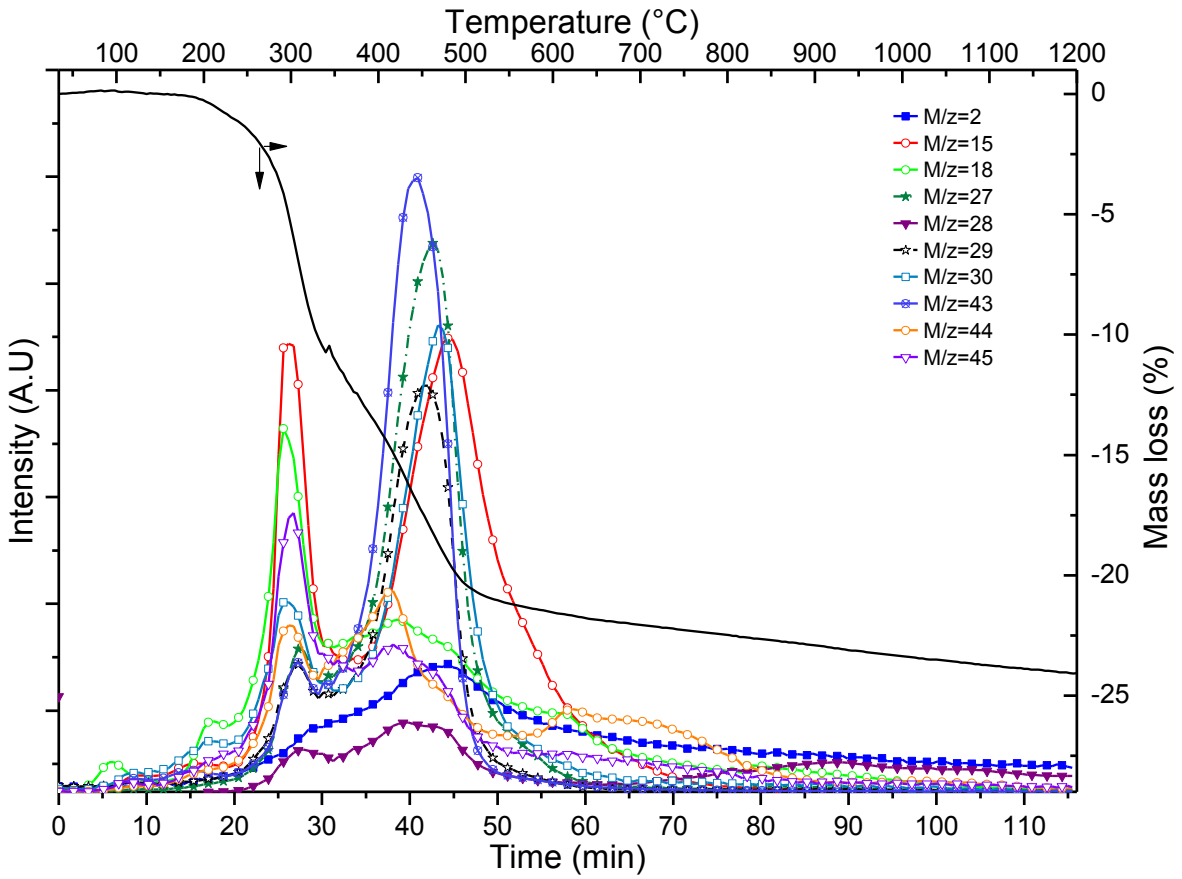

Figure A.1 *Thermogravimetry coupled with mass spectrometry analysis of sample P12-E17 heat treated under helium atmosphere.*

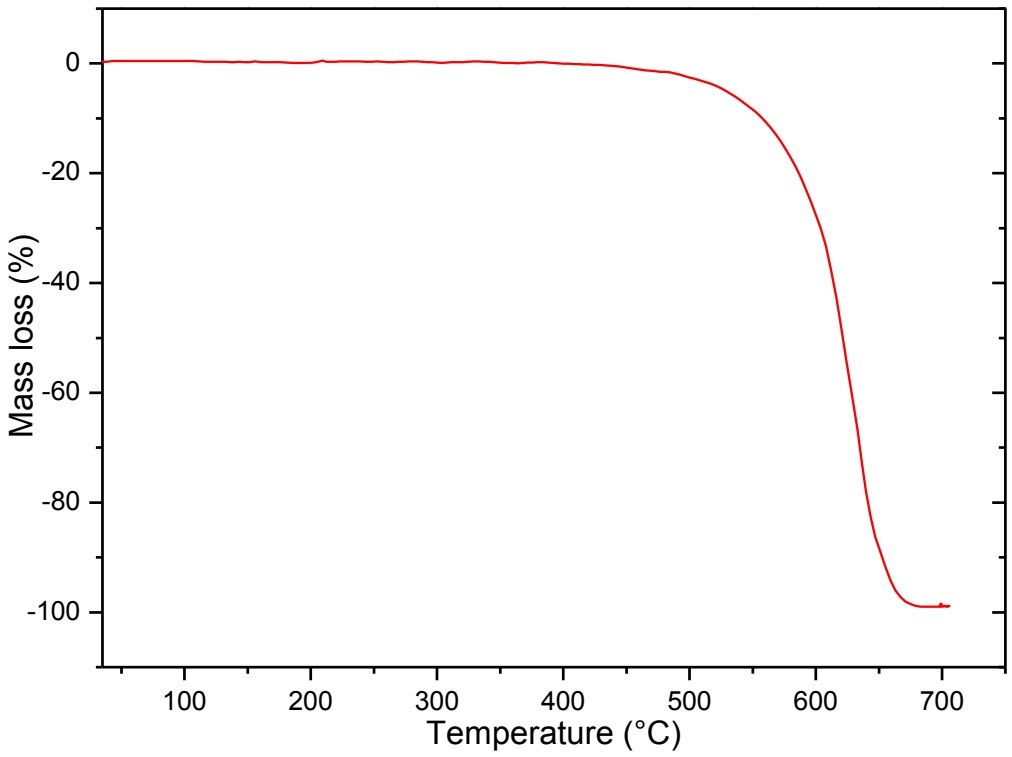

Figure A.2 *Thermogravimetry analysis of sample P12-E17 heat treated under 20% O_2/He atmosphere. P12-E17 was initially heat treated under H_2 at 600 °C.*

Raman spectroscopy analysis were conducted on the two types of samples and indicates that the characteristics of pure semiconducting and the mixture of SWNTs are very similar (Figure A.3 and A.4). In addition we did not observe any difference between characteristics before and after heat treatment (up to 1200°C in Helium). Four distinguishable peaks at: 1350 cm^{-1} (D peak shown in the insets of Figure A.3, 4), 1552 cm^{-1} (Gm peak), 1567 cm^{-1}, and 1590 cm^{-1}, were observed which are also reported in Ref [1]. Raman-active modes between 1500 and 1600 cm^{-1} are associated with the tangential displacement C–C bond stretching motions of CNTs (GM band).[2] The mode at 1350 cm^{-1} (D band) is observed in CNTs with defects.

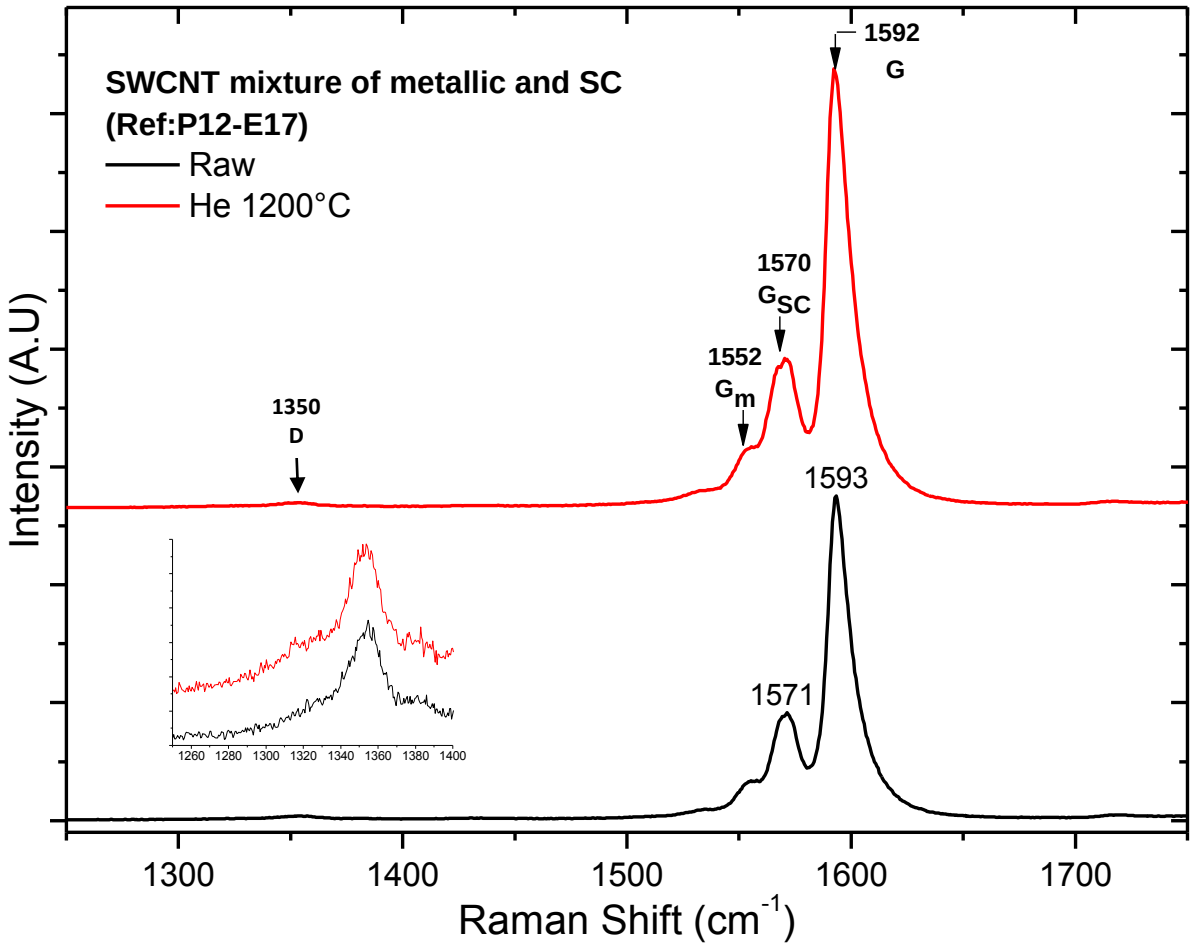

Figure A.3 *A normalized Raman spectra made before (black plot) and after (red plot) TGA experiment conducted on sample P12E17 and measured at room temperature.*

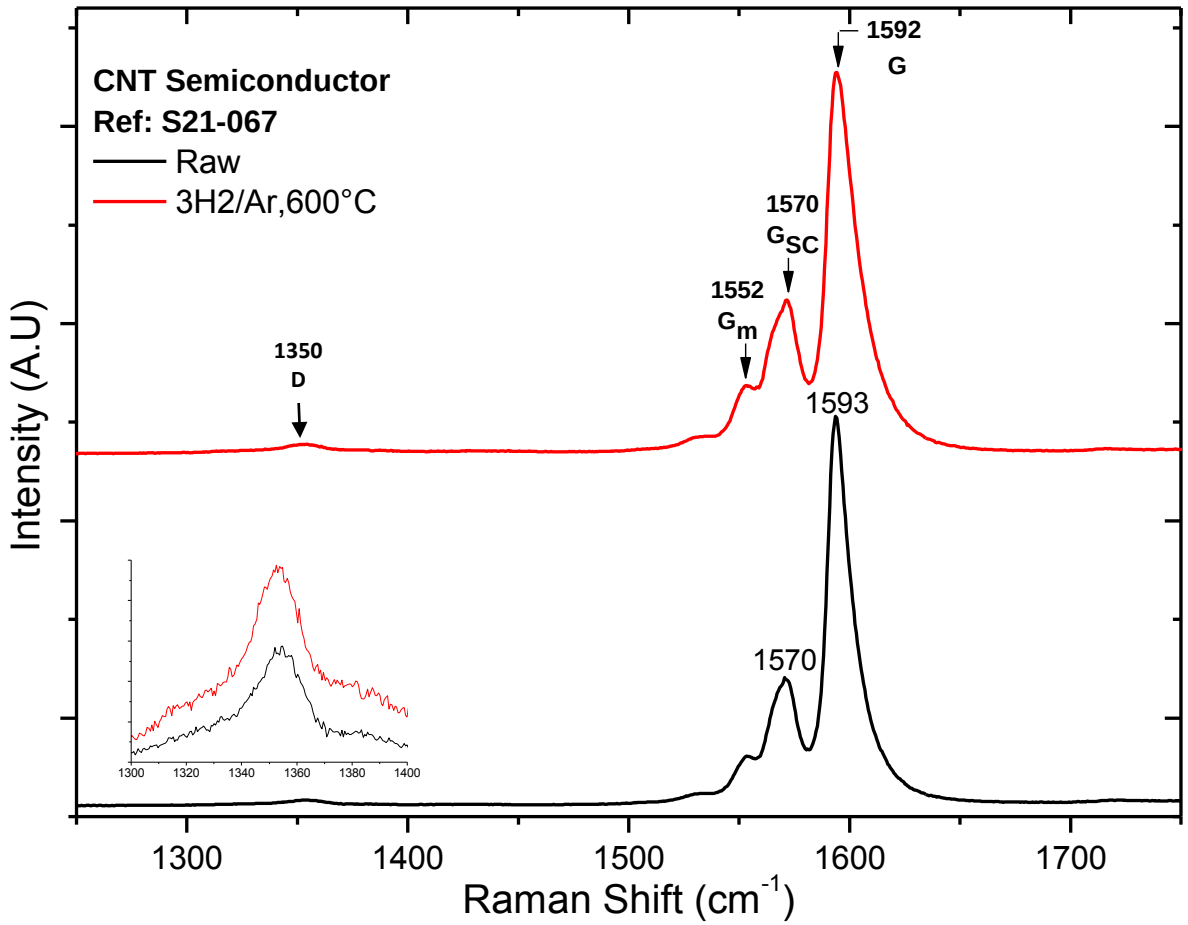

Figure A.4 *A normalized Raman spectra made before (black plot) and after (red plot) TGA experiment conducted on sample S21-067 measured at room temperature.*

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Annex B

Analysis of RTS in CNTFETs

This annex is related to **Chapter 4**, where the results of our work are presented. Here we focus on showing the results of experiments conducted on a specific CNTFET for which RTS has been observed in the absence of quantum dots. It should be noted that the device shown in this Annex is the only case where two-level current switching has been observed without a quantum dot attached to the CNTFET. Such a behavior has been reported previously in the literature and attributed to charge trapping like oxide defects or adsorbed molecules in the vicinity of the CNTFET.[1]

The CNTFET was fabricated by means of standard nanofabrication techniques (see **Chapter 3**), using commercial semiconducting nanotube (99 % pure semiconducting SWNT, NanoIntegris) deposited on a $1\,\mu m$ thick SiO_2 layer thermally grown from a p-type degenerately doped silicon wafer. Source and drain contacts were deposited by Ti ($5\,nm$) / Au ($45\,nm$) metal evaporation, and a CNTFET channel of $1\,\mu m$ length was defined.

Figure B.1a shows an AFM image of the device revealing the presence of contamination adsorbed along the CNTFET channel. We suspect that the excess material consists of residuals of resist, as a result of a failed lift-off process (see **Chapter 3, 3.4 Issues in the nanofabrication of coupled QD-CNTFET devices** section). Measurements of electrical transport were made under ambient conditions and the $I_{DS}(V_{GS})$ characteristic is shown in figure B.1b. Current vs. time $I_{DS}(t)$ data were recorded at fixed V_{GS} and are shown in Figure B.1c. We observe RTS in $I_{DS}(t)$ with *H* and *L* current levels with mean values of $168\,nA$ and $155\,nA$, respectively. It should be noted that the signal value, in comparison with the RTS signals reported for Device A and B, is much weaker (11 % of the average current). The two-level intermittency between the *H* and *L* levels is revealed by the histogram of the current levels in the $I_{DS}(t)$ data, as shown in figure B.1d. We have also reported an individual case of the time-domain $I_{DS}(t)$ trace demonstrating that the current switches between three distinct (multiple) levels (figure B.2).

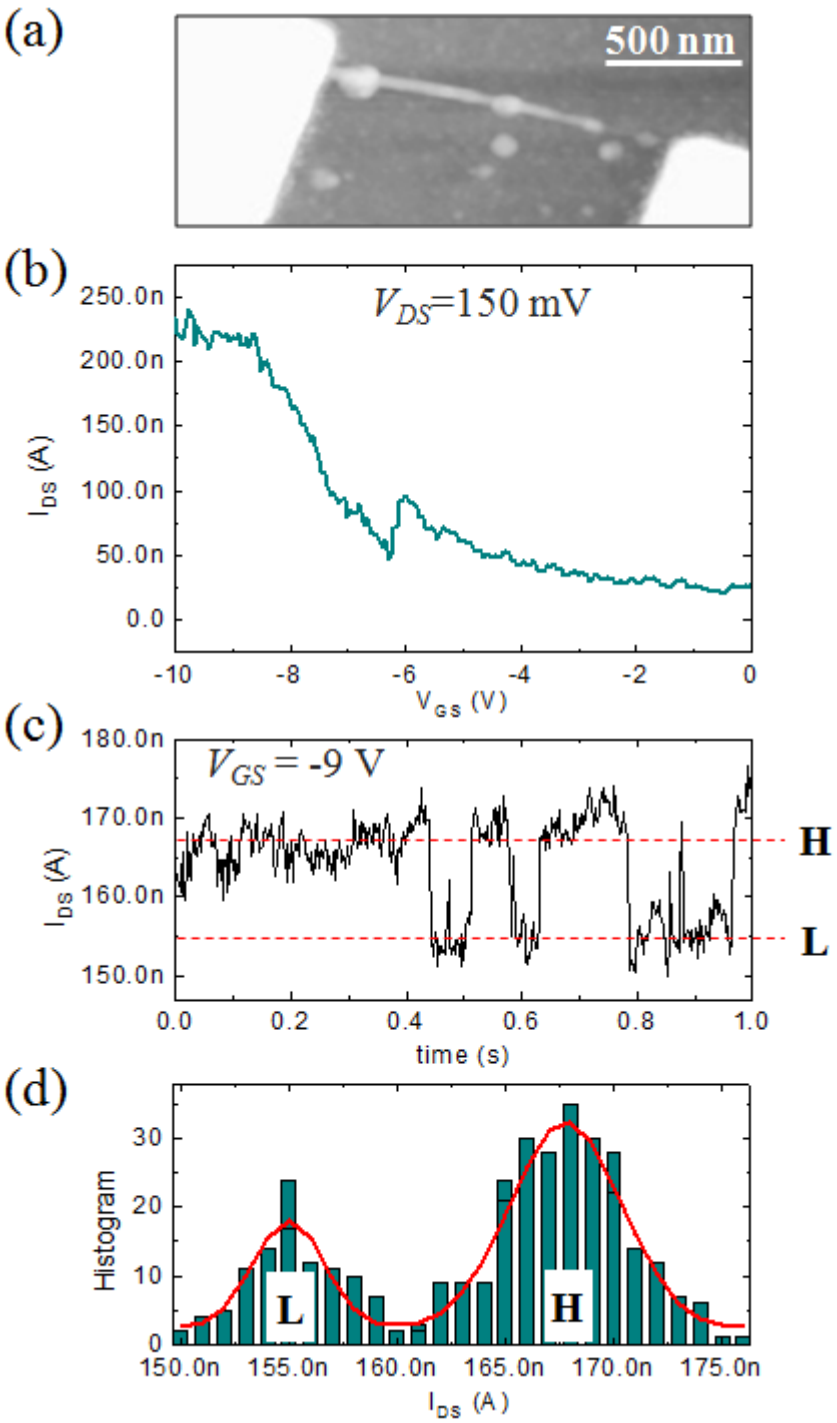

Figure B.1 *Random telegraph signal. (a) AFM image of CNTFET with contaminant molecules adsorbed along the nanotube identified after failed lift-off process. The image z-scale is 45 nm. (b) Transfer characteristics $I_{DS}(V_{GS})$ of the CNTFET (here, under dry atmosphere) V_{DS} = 150 mV. (c) Current signal plotted as a function of time $I_{DS}(t)$ at fixed V_{GS} = -9 V; the signal shows two current levels (L and H). (d) Current histograms corresponding to the graph of $I_{DS}(t)$ shown in (c).*

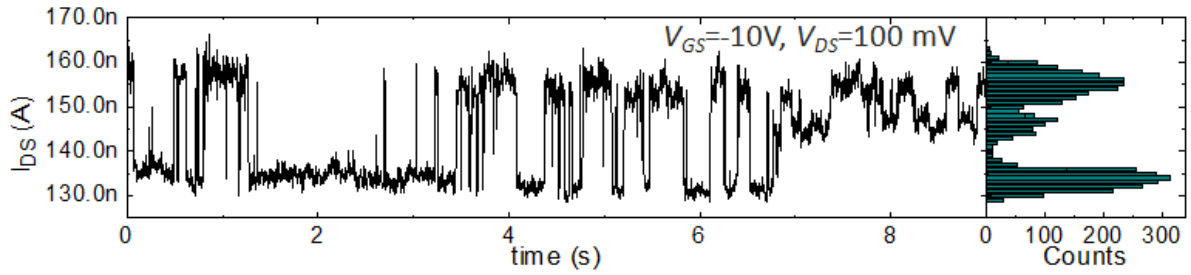

Figure B.2 *Experimental time trace of the current I_{DS}, recorded at fixed gate bias (V_{GS} = -10 V). The current histogram is provided to show the separation between (at least) three levels. Time bin and integration times are respectively τ_{min}=2 ms and τ_{max}=9 s.*

Focusing on the two-level RTS on figure B.1, we have estimated the charging energy E_c associated with the RTS using the two methods described in **Chapter 4**, section **4.4 NC-CNTFET spectroscopic analysis: Trap-state charging energy**. The RTS properties of device were probed as a function of the CNTFET back-gate, by varying V_{GS} from $0\,V$ up to $-20\,V$ with steps of $1\,V$. The observed RTS histograms are presented in figure B.3 (the insets illustrate the associated current jump events) for two V_{GS} values where the RTS could be observed.

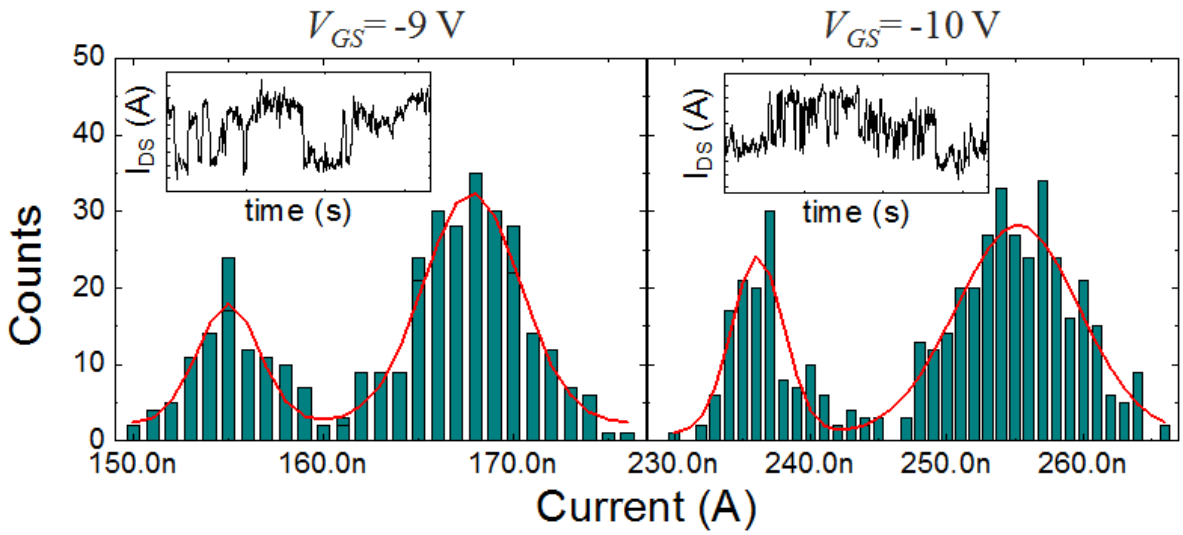

Figure B.3 *Histograms of I_{DS} current levels recorded as a function of the back-gate bias V_{GS}. The device current was recorded for each plot using a recording bin time τ_{min}=2 ms. The total recording time is τ_{max}=1s. Insets show the RTS of the current traces.*

We computed the same data as for Device A to determine the effective charging energy at hand in the charging process observed in device described here above. The results show values of $2|E_T - E_F| \approx 40\ meV$. Similarly as for Device A, we also estimated the back-gate voltage shift $\Delta V_{GS}(L-H)$ corresponding to the jump in current levels between the H and L states from the device transfer characteristics $I_{DS}(V_{GS})$ obtained for $V_{DS} = 150\ mV$ (data from figure B.1b). This analysis provides an average value for $\Delta V_{GS}(L-H)$ of $\approx 150\ mV$,

corresponding to a charging energy $E_c \approx 40\,meV$ can be deduced, which satisfies $E_c \geq 2|E_T - E_F|$, using the lever arm β =0.37 for the CNTFET device geometry. We therefore obtain a different result as for Devices A or B, for which the RTS can be understood as the charging of a trap with $E_c \approx 200\,meV$ and $E_c \approx 225\,meV$, respectively, which shows that the identified RTS stems from traps of nature as compared to Devices A and B.

V_{GS}	$\langle\tau_L\rangle/\langle\tau_H\rangle$	$2(E_T - E_F)$	$\Delta V_{GS}(L-H)$	$e\Delta V_{GS}(L-H)/\beta$
-9 V	0.48	**-38 meV**	0.20 V	**43 meV**
-10 V	2.05	**37 meV**	0.10 V	**27 meV**

Table B.1 *Analysis of the RTS noise. The table shows the operation back-gate bias V_{GS}, the ratio between the average times $\langle\tau_L\rangle$ and $\langle\tau_H\rangle$ and the trap energy with respect to the CNTFET Fermi level $E_T - E_F$; the back-gate voltage difference between the current levels I_L and I_H associated with the L and H states (obtained from the transfer characteristics of device) and the corresponding charging energy obtained using the lever arm β = 3.7 taken from Ref.* [2]

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[2] Zdrojek, M., Esplandiu, M .J., Barreiro, A. & Bachtold, A. Electron counting spectroscopy of CdSe quantum dots. *Phys. Rev. Lett.* **102**, 226804 (2009).

List of publications and communications

Articles:

- *Determination of the electromechanical properties of self assembled Au nanocrystal arrays for force sensing applications*; M. Biaye *et al.*, in preparation

- *Charge blinking of semiconductor nanocrystals probed by carbon nanotube single electron sensor;* E. Zbydniewska, A. Dużyńska, M. Popoff, D. Hourlier, S. Lenfant, J. Judek, M. Zdrojek, T. Melin; *Nano Letters* 2015 (10) pp 6349–6356. doi:10.1021/acs.nanolett.5b01338

- *Synthesis of Carbon Nanotubes from Propane;* M. Zdrojek, J. Sobieski, A. Dużyńska, E. Zbydniewska, W. Strupinski, J. Ratajczak, J. Judek; *Chemical Vapor Deposition* (2015), doi: 10.1002/cvde.201404329

Conferences:

- IEMN Department Days; April 23-24, 2015, poster: *Charge blinking statistics of semiconductor nanocrystals revealed by carbon nanotube single charge sensors;* E. Zbydniewska, A. Duzynska, M. Popoff, D. Hourlier, S. Lenfant, J. Judek, M. Zdrojek, T. Mélin
- E-MRS 2014 Fall Meeting; September15-19, 2014, poster: *Single electron manipulation at room temperature in coupled colloidal quantum dots and carbon nanotubes*; E. Zbydniewska, M. Zdrojek, J. Judek, T. Mélin
- Annual Meeting GDR-I GNT “Graphene and Nanotubes” Science and Applications Ecully (Lyon), January 23-27, 2012
- HERODOT Cargese summer school “Heterogeneous Quantum Rod and Quantum Dot Nanomaterials”, April 4-15, 2011