N° d'ordre : 42328

THÈSE

Présentée à l'Université de Lille 1
École Doctorale Sciences pour l'Ingénieur

Institut d'Électronique, de Microélectronique et de Nanotechnologie

Pour obtenir le grade de :

DOCTEUR DE L'UNIVERSITE

Spécialité : MICRO ET NANOTECHNOLOGIES, ACOUSTIQUE ET TELECOMMUNICATIONS

Par

Julien BORREL

INNOVATIVE CONTACT TECHNOLOGY FOR CMOS FDSOI 10 NM AND BELOW

Soutenue le 03 Mars 2017 devant le jury composé de :

M. Siegfried Mantl, Professeur, Julich Forschungszentrum, Julich	Rapporteur
M. Athanasios Dimoulas, Directeur de recherche, NCSR Demokritos, Athènes	Rapporteur
M. Raphael Clerc, Professeur, Institut d'Optique, Saint Etienne	Examinateur
Mme. Maryline Bawedin, Maître de conférences, IMEP-LAHC, Grenoble	Examinateur
M. Louis Hutin, Ingénieur de recherche, CEA-LETI, Grenoble	Co-encadrant de thèse
Mme. Magali Grégoire, Ingénieur R&D, STMicroelectronics, Crolles	Co-encadrant de thèse
M. Emmanuel Dubois, Directeur de recherche CNRS, IEMN, Villeneuve d'Ascq	Directeur de thèse

“*The man who goes farthest is generally the one who is willing to do and dare. The sure-thing boat never gets far from shore.*”

Dale Carnegie

Acknowledgments

My doctoral research was performed from 2014 to 2017 and took place between the Leti research institute of the French Alternative Energies and Atomic Energy Commission (CEA) in Grenoble, STMicroelectronics in Crolles and the Institute of Electronics, Microelectronics and Nanotechnology (IEMN) in Lille.

I would like to address my first thanks to all the people who have helped me during my PhD to elaborate experiments and to perform them. The semi-industrial and industrial environments of respectively CEA-LETI and STMicroelectronics obviously offer an exceptional framework, allowing developing disruptive devices using avant-garde manufacturing equipments. Nevertheless, interacting with such environments also requires a significant level of expertise in various types of areas from the premises of stand-alone process developments to the final electrical characterization of manufactured devices. Such an expertise has been provided to me during these three years in both CEA-LETI and STMicroelectronics and I am glad I was able to learn from these experts such an extensive amount of invaluable knowledge.

I wish to express my thankfulness to the Laboratory of Logic Component Integration (LICL) of the CEA/LETI and the metal process development group of STMicroelectronics. Both groups have welcomed me and helped me achieving my PhD in the best conditions I could have wished for. A lot of support was given to me, allowing me to blossom in both LETI and STMicroelectronics environments.

My deepest gratitude goes to my supervisors Louis Hutin (CEA) and Magali Grégoire (STM) and my PhD director Emmanuel Dubois (IEMN). Always providing me food for thought in the technical and scientific fields, they allowed me to step back from my work and to grasp a broader vision of my project. Their experience and ability to communicate results took a huge part in my success to produce a high number of articles and abstracts.

I would like to particularly thank Louis who speaks English better than I speak French. I had the chance to travel a lot, being systematically accepted to all the conferences I applied to, and I truly believed that this is directly linked to his communication skills and his rigor. He also supported me in a daily basis, even in the times of doubt when my motivation or my sense of legitimacy were challenged. Without him, I would not have been able to perform the same amount of work with the same degree of quality.

My thoughts also goes to all the others students. Without them, this journey would not have been the same. I would specially thank Mathilde, Heimanu, Luca, Alex, Julien, Jose and Lina to whom I wish the best. Thanks to them, I know that I will keep with me great memories of these three years. I am going to miss them a lot.

Finally, I would like to thank my family and my family in law who have supported me during these three years and particularly my wife Elodie who has been here for me in all the situations, dealing with my highs and my lows and sharing my joys and my pains.

Table of Contents

List of Acronyms 10

Physical Values 12

Chapter I: MOSFETs miniaturization: expectations and limits 13

Introduction to Chapter I 15

I.1 Operative principle of MOSFET for digital logic 16

I.1.1 Basic ideal MOSFET operations...16

I.1.2 Actual electrical behavior..17

I.1.3 Parasitic elements in a real MOSFET 22

I.1.4 Device performance 25

I.2 MOS scaling..27

I.2.1 Costs reduction and performance improvement...............................27

I.2.2 Scaling limitations 29

I.2.3 Next node generations challenges 32

I.3 Ideal contact theory 35

I.4 Real contact case...39

I.4.1 Interface states...39

I.4.2 Fermi Level Pinning...41

I.5 Contact resistivity optimization 42

I.5.1 Space charge region width reduction 43

I.5.2 Effective SBH reduction via FLP mitigation 44

I.5.3 Effective SBH reduction via dipole engineering.................................49

I.6 Chapter conclusion...54

I.7 Thesis Objectives 55

I.8 References 56

Chapter II: MIS contacts modeling and simulation 63

Introduction to Chapter II 65

II.1 Analytical algorithm presentation..66

II.1.1 Fermi Level Pinning 67

II.1.2 1-D band edge diagram evaluation 75

II.1.3 J-V characteristics generation 80

II.2 Stand-alone contact J-V characteristics 90

II.2.1 Zero-barrier contact case 90

II.2.2 MIS contacts simulations 91

II.2.3 Partial conclusions 101

II.3 Impact on devices performance...103

II.3.1 DC impact...103

II.3.2 AC impact...108

II.4 Chapter conclusions...116

II.5 References..118

Chapter III: Implementation and physico-chemical characterization of ultra-thin dielectrics 121

Introduction to Chapter III 123

III.1 Deviation from ideal process flow..124

III.1.1 Control of the substrate surface oxidation 124

III.1.2 MIS contacts instability 126

III.2 Experimental results 133

III.2.1 Indirect TiOx implementation by scavenging 134

III.2.2 ALD based high-k implementations..141

III.2.3 CVD based high-k implementations..149

III.3 Chapter conclusions 152

III.4 References 154

Chapter IV: Electrical characterization of MIS contacts 157

Introduction to Chapter IV.... 159

IV.1 Conventional contact characterization....160

IV.1.1 Specific contact resistivity 160

IV.1.2 Schottky barrier height....161

IV.2 Conventional test structures....163

IV.2.1 Back contact measurement....163

IV.2.2 Transmission Line Model (TLM) 167

IV.2.3 Cross Bridge Kelvin Resistor (CBKR)....171

IV.2.4 Summary of the section....177

IV.3 MIS contacts integration....178

IV.3.1 Substrate characteristics....178

IV.3.2 Dielectric characteristics....180

IV.3.3 Expected materials parameters....182

IV.3.4 Structures layout 182

IV.4 Experimental results 184

IV.4.1 TLM measurements 184

IV.4.2 CBKR measurements....190

IV.5 Discussions....202

IV.5.1 Obtaining contact signature I-V characteristics with CBKR 202

IV.5.2 The TiN/TiO_2/Si case....203

IV.6 Chapter conclusions 206

IV.7 References 208

Chapter V: General conclusions.... 211

V.1 Impact of MIS contacts on advanced MOSFETs nodes....214

V.2 Practical ultra-thin dielectric implementation 215

V.3 Effective electrical properties of MIS contacts 215

V.4 Prospects 216

V.5 References 218

List of Acronyms

AC: Alternating Current

ALD: Atomic Layer Deposition

ARXPS: Angle Resolved X-ray Photoelectron Spectroscopy

BEOL: Back End Of Line

BGE: Band Gap Energy

BOX: Buried OXide

CBO: Conduction Band Offset

CBKR: Cross Bridge Kelvin Resistor

CMOS: Complementary Metal Oxide Semiconductor

CNL: Charge Neutrality Level

CPP: Contacted Poly Pitch

CVD: Chemical Vapor Deposition

DC: Direct Current

DIBL: Drain Induced Barrier Lowering

DIGS: Default-Induced Gap Sates

EELS: Electron Energy Loss Spectroscopy

EOT: Equivalent Oxide Thickness

FDSOI: Fully Depleted Silicon On Insulator

FE: Field Emission

FLP: Fermi Level Pinning

HAADF: High-Angle Annular Dark-Field

HK: High-K

IC: Integrated Circuit

ITRS: International Technology Roadmap for Semiconductor

MIGS: Metal-Induced Gap States

TEMAH: Tetrakis(EthylMethylAmino)Hafnium

MIIS: Metal Insulator Insulator Semiconductor

MIS: Metal Insulator Semiconductor

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor

MS: Metal Semiconductor

NMOS: “N” Metal-Oxide-Semiconductor

PMOS: “P” Metal-Oxide-Semiconductor

POCO: POly COntact

PVD: Physical Vapor Deposition

RC: Resistance Capacitance

RO: Ring Oscillator

RTA: Rapid Thermal Annealing

SBH: Schottky Barrier Height

SC1: Standard Clean 1

SC2: Standard Clean 2

SCE: Short Channel Effects

SCR: Space Charge Region

SD: Source Drain

SOI: Silicon On Insulator

SPICE: Simulation Program with Integrated Circuit Emphasis

SS: Subthreshold Swing

STEM: Scanning Transmission Electron Microscope

TCAD: Technology Computer Aided Design

TE: Thermionic Emission

TFE: Thermionic Field Emission

TEM: Transmission Electron Microscope

TLM: Transmission Line Model

TMA: TriMethylAluminium

TOF-SIMS: Time Of Flight Secondary Ion Mass Spectrometry

TWKB: Transmission Wentzel-Kramers-Brillouin

UHV: Ultra High Vacuum

VBO: Valence Band Offset

XPS: X-ray Photoelectron Spectrosco

Physical Values

Notation	Name	Value
ε_0	Vacuum permittivity	8.85×10^{-12} F.m^{-1}
$\hbar$	Reduced Planck constant	1.054×10^{-34} J.s
m_0	Electron rest mass	9.11×10^{-31} kg
n_i	Intrinsic carrier concentration of Si	1×10^{10} cm^{-3}
q	Elementary charge	1.6×10^{-19} C

Chapter I
MOSFETs miniaturization: expectations and limits

Introduction to Chapter I 15
I.1 Operative principle of MOSFET for digital logic 16
I.1.1 Basic ideal MOSFET operations 16
I.1.2 Actual electrical behavior 17
I.1.3 Parasitic elements in a real MOSFET 22
I.1.4 Device performance 25
I.2 MOS scaling 27
I.2.1 Costs reduction and performance improvement 27
I.2.2 Scaling limitations 29
I.2.3 Next node generations challenges 32
I.3 Ideal contact theory 35
I.4 Real contact case 39
I.4.1 Interface states 39
I.4.2 Fermi Level Pinning 41
I.5 Contact resistivity optimization 42
I.5.1 Space charge region width reduction 43
I.5.2 Effective SBH reduction via FLP mitigation 44
I.5.3 Effective SBH reduction via dipole engineering 49
I.6 Chapter conclusion 54
I.7 Thesis Objectives 55
I.8 References 56

Introduction to Chapter I

The purpose of this chapter is to present the basic theory of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) electrical behavior and the principles of its functioning. The main general concepts and parameters of the field are introduced.

The first part is dedicated to the geometric description of the device itself as well as its functioning. Starting from a description of the MOSFET as an ideal switch, more realistic elements are then added step by step leading to an accurate representation of its modes of operation.

The second part focuses on the miniaturization trend observed in the microelectronic devices from its original formulation to its practical implementation. The issues arising from reaching ultra-aggressively scaled devices are also presented.

Finally, the last three sections are an introduction of the thesis work presented in this manuscript: tackling the contact resistance issue. These parts will be respectively dedicated to present the theory behind the contact resistance, to introduce the phenomena occurring at the real metal/semiconductor interfaces and finally to present the state-of-the-art concerning contact resistance engineering.

I.1 Operative principle of MOSFET for digital logic

In this part, the basic electrical behavior of a MOSFET is described. The first section focuses on the ideal operation of such device in order to give a quick overview of the main transfer characteristics and equations. In the second and third section, limitations arising from the MOSFET switching physics in itself as well as its practical integration are discussed. Finally the last section presents notions of dynamical performance evaluation.

I.1.1 Basic ideal MOSFET operations

As its name suggests, the fundamental stack of any MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) is composed of three main elements. The first is a semiconductor (e. g. Si, Ge, InGaAs) where a current of electric carriers can take place. These carriers travel between two reservoirs called source and drain via a path called channel. The state of this channel, open or closed, is controlled by a field effect [*Lilienfeld_1925*]. This field arises from the bias of an element called gate which consists in a metallic electrode separated from the channel by a dielectric layer called gate oxide.

Depending on the dopants introduced in the source and drain, the current carriers flowing in the channel can be electrons (the MOSFET is referred to as NMOS because electron carry an Negative charge) or quasiparticles equivalent to a lack of electrons called holes (the MOSFET is referred to as PMOS for Positive charge).

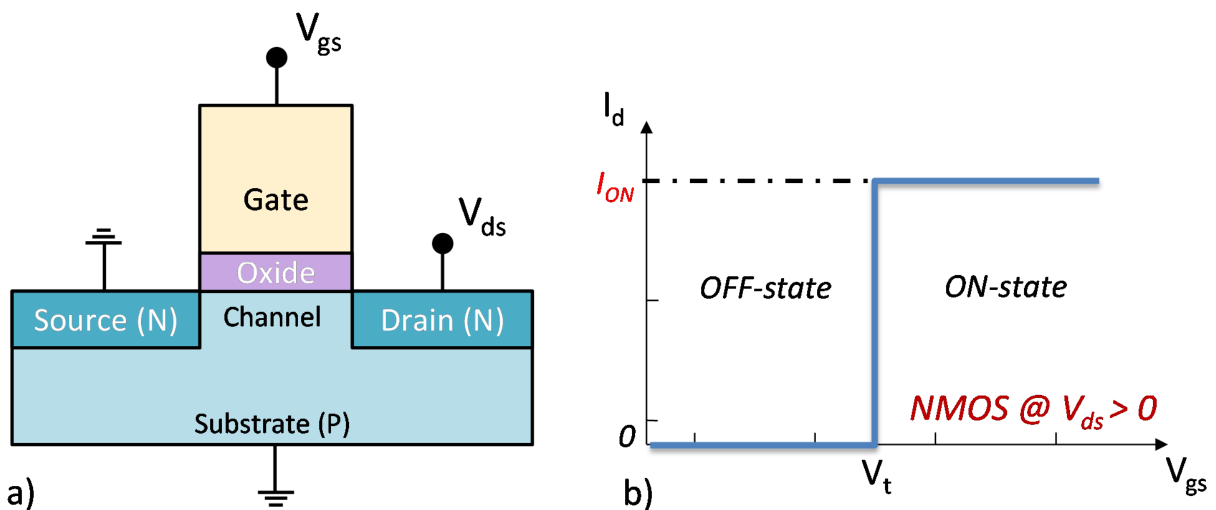


Figure I-1 : (a) Schematic of a traditional bulk NMOS; (b) Ideal I_d-V_{gs} curve of a NMOS when biasing the drain with a positive voltage.

The relative position of the MOSFET main elements is illustrated in Figure I-1 (a) in the case of a bulk NMOS. The gate bias required to actuate the MOSFET depend on its nature i.e. NMOS or PMOS.

As presented for the NMOS in Figure I-1 (a) while the source and drain are n-type semiconductor the substrate is p-type. In order to allow flowing electrons from one reservoir to the other, a sine qua non condition is to induce a sufficient amount of electrons in the channel region which then become the majority carriers at the top surface of the p-type substrate. This can be done by using the field of the gate. The gate acts as the switch of the transistor and has to be positively biased in the case of a NMOS. Moreover, the amount of electrons attracted in the channel has to overcome the amount of holes initially present in the p-type substrate. One can distinguish a typical value of the gate bias called threshold voltage and noted V_t where this transition occurs. The ideal curve of the drain current as a function of the gate-to-source bias (I_d - V_{gs}) of a NMOS is presented in Figure I-1 (b) and illustrates the transition from the OFF-state to the ON-state occurring when V_{gs} equals V_t.

Similar considerations can be adapted to a PMOS which mainly differs from the fact that instead of actuating the device with positive biases, negative ones have to be applied. Therefore, PMOS and NMOS are two switches with dual operating modes and can be used together as elementary elements for digital gates and circuits. Thus this paradigm is called CMOS standing for Complementary Metal Oxide Semiconductor.

I.1.2 Actual electrical behavior

I.1.2.a Current leakage and subthreshold slope

The model proposed above presents the MOSFET as an ideal switch actuated by the gate bias. Nevertheless, the functioning of such device is not perfect:

- The transition from the OFF-state to the ON-state is not as steep as introduced before in Figure I-1. The slope of the I_d-V_{gs} around V_t is not infinite but has a limited value.
- In the OFF-state ($V_{gs} < V_t$) the current flowing from the source to the drain is not zero. This current is called leakage current and is responsible for energy consumption even in the OFF-state.

When applying a bias V_{ds}, the density of electrons is larger in the drain than in the source. Thus, even when the gate is biased below the threshold voltage V_t, a diffusion current occurs in the channel because of the gradient of reservoir majority carriers between the source and the drain. The diffusion current density occurring in the channel for a NMOS device is described by Equation (I-1).

$$j_{diff} = -qD_n \frac{dn(x)}{dx} \quad \text{(I-1)}$$

where the x axis is taken along the channel, *n(x)* is the density of electrons and D_n is a diffusion constant which is a characteristics of the semiconductor material.

Integrating Equation (I-1) in the channel and considering that the variation of the electron density is linear, Equation (I-2) can be obtained.

$$I_d = qAD_n \frac{n(0) - n(L_g)}{L_g} \quad \text{(I-2)}$$

where *n(0)* and $n(L_g)$ are respectively the density of electrons in the source and the drain and *A* is the cross-sectional area of the current flow.

According to [*Sze_1981*], the two densities mentioned above can be found using Equations (I-3) and (I-4) where φ_s referred to the surface potential inside the channel.

$$n(0) = n_0 e^{\frac{q\varphi_s}{kT}} \quad \text{(I-3)}$$

$$n(L_g) = n_0 e^{\frac{q(\varphi_s - V_{ds})}{kT}} \quad \text{(I-4)}$$

Then by including Equations (I-3) and (I-4) in Equation (I-2), the drain current is described by Equation (I-5).

$$I_d = q\frac{A}{L_g} D_n n_0 e^{\frac{q\varphi_s}{kT}} (1 - e^{-\frac{qV_{ds}}{kT}}) \quad \text{(I-5)}$$

In this equation, one can see that the current is exponentially proportional to the surface potential. In order to investigate the subthreshold regime, the link between this surface potential and the gate voltage has to be established. Based on Figure I-1, this calculus can be easily summed up by a capacitive divider as shown in Figure I-2.

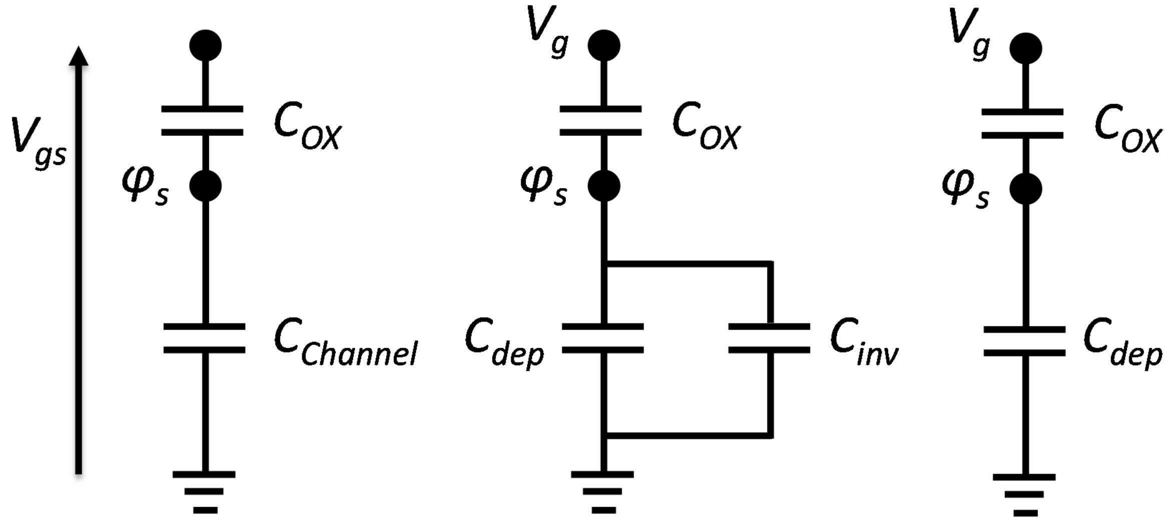


Figure I-2: Capacitive divider used to evaluate the link between the surface potential and the gate voltage. $C_{channel}$ is composed by C_{dep} and C_{inv} in parallel, the latter being negligible compared to the former when the gate voltage is lower than the onset of inversion.

Because the gate is biased below the threshold voltage the density of electrons in the channel is low compared to the density of ionized dopants. In this condition, the capacitance due to the inversion layer can be neglected compared to the depletion capacitance. By applying the capacitive divider to this situation, one can obtain Equation (I-6).

$$\varphi_s = V_{gs}\frac{C_{ox}}{C_{ox}+C_{dep}} = \frac{V_{gs}}{\eta} \quad \text{(I-6)}$$

With

$$\eta = \frac{C_{ox}+C_{dep}}{C_{ox}} \quad \text{(I-7)}$$

Combining Equations (I-5) and (I-6), the drain current I_d becomes:

$$I_d = q\frac{A}{L_g}D_n n_0 e^{\frac{qV_{gs}}{kT\eta}}(1-e^{-\frac{qV_{ds}}{kT}}) \quad \text{(I-8)}$$

As mentioned previously, the transition from the OFF-state to the ON-state cannot be considered infinitely steep and then the definition of V_t as the V_{gs} at which the transition occurs is inaccurate. In experimental studies, the most accurate method to extract V_t is the transconductance peak or double-derivative method [*Simoen_1996*]. Defining the transconductance g_m according to Equation (I-9), V_t is defined as the gate voltage V_{gs} corresponding to the maximum of the $\partial g_m/\partial V_{gs}$ curve.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad \text{(I-9)}$$

Considering this definition of the threshold voltage, the associated threshold current I_t is defined by Equation (I-10):

$$I_t = q\frac{A}{L_g}D_n n_0 e^{\frac{qV_t}{kT\eta}}(1 - e^{-\frac{qV_{ds}}{kT}}) \quad \text{(I-10)}$$

Thus one can rewrite Equation (I-8) and obtain (I-11).

$$I_d = I_t e^{\frac{q}{kT}\times\frac{(V_{gs}-V_t)}{\eta}} \quad \text{(I-11)}$$

The two investigated parameters, i.e. the leakage current and the subthreshold slope, can be obtained using the expression of I_d in Equation (I-11).

As presented in this equation, the drain current is an exponential function of the gate bias in the subthreshold mode. Thus, when plotting I_d as a function of V_{gs} in a logarithmic scale, the representative curve is a straight line. The slope of this curve is called the “subthreshold slope” and its opposite the subthreshold swing (noted SS). The latter can be evaluated by deriving Equation (I-11) leading to (I-12).

Moreover, the I_{OFF} can be evaluated when considering $V_{gs} = 0$ in Equation (I-11) leading to Equation (I-13).

$$SS = \frac{dV_{gs}}{dlog(I_d)} = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{dep}}{C_{ox}}\right) \quad \text{(I-12)}$$

$$I_{OFF} = I_t e^{-\frac{q\,V_t}{kT\,\eta}} = I_t e^{-\frac{V_t}{SS\,ln(10)}} \quad \text{(I-13)}$$

One can see that the subthreshold swing appears to be a key parameter to evaluate the static performance of a more realistic transistor. Indeed reducing the leakage current and ensuring at the same

time an ultra-steep switch from the OFF-state to the ON-state can be achieved by approaching the SS value to zero (thus tending towards an ideal switch).

Nevertheless, based on Equation (I-12), the SS lower limit is obtained when $C_{dep} = C_{ox}$ and reaches $\frac{kT}{q}\ln(10)$ which corresponds to 60 mV.dec^{-1} at 300K.

I.1.2.b Drain bias dependence

While the gate acts as the switch of the MOSFET and control the presence or the absence of charge carriers in the channel, making these carriers flow is controlled by the bias of the drain. Depending on the magnitude of this bias, two regimes can be distinguished: the ohmic and saturation modes. Considering a long channel model, these two regimes can be described as follow.

In the former, I_d is noted $I_{d,lin}$ and is almost linearly proportional to V_{ds} at low V_{ds} as shown in Equation (I-14).

$$I_{d,lin} = \mu_{eff} C_{ox} \frac{W}{L_g}\left(\left(V_{gs} - V_t\right)V_{ds} - \frac{V_{ds}^2}{2}\right) \tag{I-14}$$

where μ_{eff} is the charge carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area, $W$is the gate width and L_g is the gate length.

When V_{ds} is increased and reached the value $V_{ds,sat} = V_{gs} - V_t$, the transistor passes to the saturation mode which can be described as follow: since the effective bias seen by the part of the channel close to the drain is V_{gd}, as the bias on the drain is increased, the actual voltage difference between the drain and the gate is reduced. When V_{ds} finally reaches $V_{ds,sat}$, V_{gd} is lower than V_t. If the drain is biased at higher voltages, the carriers continue to be accelerated but the channel is pinched-off close to the drain. In this regime, the drive current I_d obtained from this trade-off is constant with V_{ds} as described in Equation (I-15).

$$I_{d,sat} = \mu_{eff} C_{ox} \frac{W}{2L_g} V_{ds,sat}^2 \tag{I-15}$$

Typical I_d-V_{gs} and I_d-V_{ds} curves of a NMOS are presented in Figure I-3 (a) and (b). In Figure I-3 (a) one can see that the actual electrical response of a MOSFET is far from the expected ideal one. These non-idealities arise from the founding principles of the MOSFETs in itself meaning that such a type of

devices is theoretically unable to present an ideal steeper switching profile. Additionally to these theoretical limitations, transistors present also parasitic elements arising from their practical implementation which limit even more the functioning.

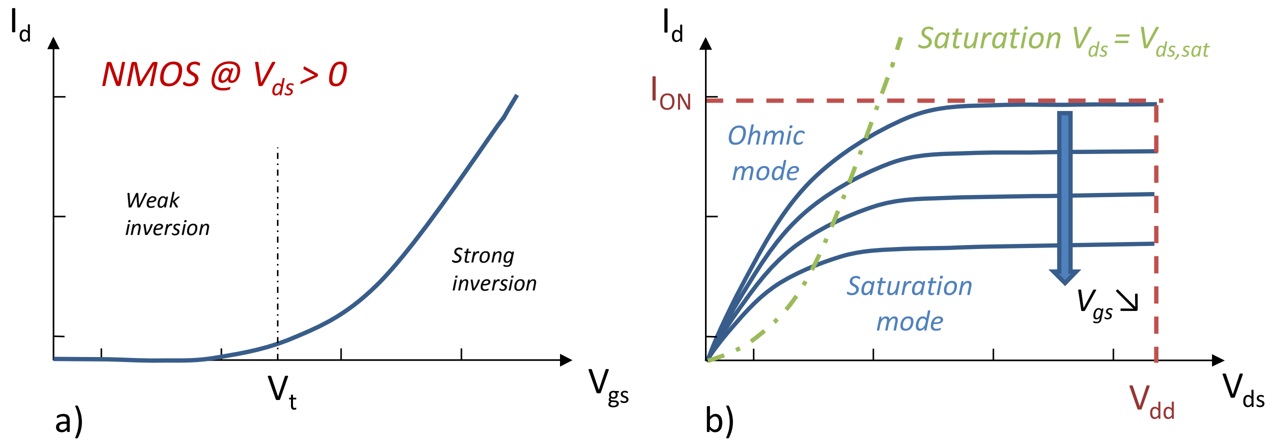


Figure I-3: Typical (a) I_d-V_{gs} and (b) I_d-V_{ds} curve for a NMOS.

I.1.3 Parasitic elements in a real MOSFET

In this section, parasitic elements arising from the integration of MOSFETs are described. Although they are not taken into account in the model previously presented, these additional contributions have a significant impact on the devices performances in both static (DC) and time-dependent (AC) regimes.

I.1.3.a Access resistance

The previous description of the transistor assumes that the source and drain are perfectly conducting elements and that no interface effects occurs between them and the channel. In real devices, several parasitic resistances have to be considered and then alter the previous model. According to [*Ng_1986*], the components to consider are four in number and are represented in Figure I-4:

- R_{co} stands for contact resistance and arises from the interface between the contact metal and the source/drain semiconductor. Although its origin and expression will be extensively discussed in sections I.3 and I.4, R_{co} can be approximated by Equation (I-16).

$$R_{co} = \rho_c / W_c L_c \tag{I-16}$$

where ρ_c is the contact specific resistivity, W_c its width and L_c its length. While the resistivity depends only on the nature of the metal/semiconductor interface (materials, cleaning treatment, doping concentration, etc.), W_c and L_c only refer to geometrical parameters. Thus, for a given interface the contact resistance varies with its size.

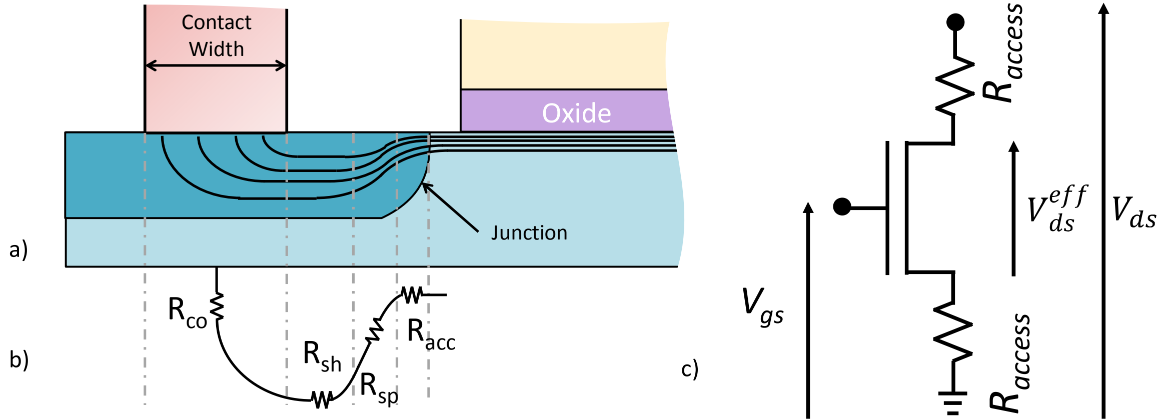


Figure I-4: (a) Schematic diagram of the source/drain region showing the current path and (b) representation of the associated components of resistance. (c) Schematic MOSFET circuit showing access resistances noted R_{access}.

- R_{sh} refers to the sheet resistance of the source and drain semiconductors. Usually, in order to reduce this component and to ensure the thermal stability of the metal/semiconductor interface, an intermetallic compound is intentionally formed at the source/drain surfaces prior to metallization. When the source and drain are based on silicon, this process is called silicidation.
- The last two resistances are R_{sp} and R_{acc} defined as the spreading and accumulation resistances. They are gate-voltage dependent [*Ng_1986*]. On the one hand, when the current reaches the end of the source and drain regions and the field lines are constricted in a smaller area. This phenomenon is referred to as crowding effect and induces the resistance R_{sp}. On the other hand, at the metallurgic junctions (source/channel and channel/drain interfaces), the concentration of carriers abruptly varies leading to a modification of the transport properties. This leads to the apparition of the resistance R_{acc}.

All this components are often treated as a single parasitic contribution called access resistance and referred to as R_{access} as defined in Equation (I-17).

$$R_{access} = R_{co} + R_{sh} + R_{sp} + R_{acc} \quad \text{(I-17)}$$

Being in series with the channel these parasitic resistive components may have a significant impact on the transistor electrical behavior. Indeed when biasing a transistor, a part of the applied voltage drops in the source and the drain due to their associated access resistance. This leads in turn to a lower effective bias applied on the channel. As shown in Figure I-4 (c), this effective bias can be noted V_{ds}^{eff} and can be found solving (I-18).

$$V_{ds}^{eff} = V_{ds} - (R_{s,access} + R_{d,access}) \times I_{ds} \qquad \text{(I-18)}$$

It is worth noting that this problem is self-consistent since finding V_{ds}^{eff} require knowing I_{ds} which is itself a function of V_{ds}^{eff}.

I.1.3.b Stray capacitances

As for the resistive aspect, a MOSFET presents some parasitic capacitive elements which will degrade its performance. While the resistive ones have an impact in both the static and the dynamic regimes, the stray capacitances mostly degrade the dynamic performance.

The MOSFET schematic including these parasitic capacitances is shown in Figure I-5. Therefore, the total capacitance of the gate $C_{g,tot}$ is described by Equation (I-19).

$$C_{g,tot} = C_{gc} + 2 \times C_{if} + 2 \times C_{ov} + 2 \times C_{of} + 2 \times C_{spacer} \qquad \text{(I-19)}$$

C_{if} and C_{ov} are respectively the inner-fringe and overlap capacitances and represent the capacitive effect between the gate and the source/drain through respectively the gate oxide and the channel, and only the gate oxide. While C_{if} has a remote effect, C_{ov} has a direct coupling but only occurs when the gate overlaps the source/drain. For their part, C_{of} and C_{spacer} are called outer-fringe and spacer capacitances. They are capacitive couplings occurring through the spacer between the gate and respectively the source/drain and the metallic plug.

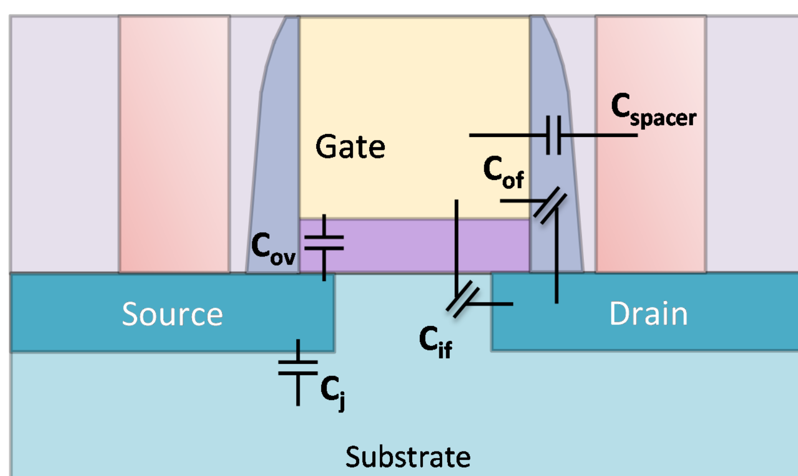


Figure I-5: Schematic of a MOSFET presenting the main parasitic capacitors.

While C_{gc} is the actuation capacitance used to switch the state of the channel, the other capacitors have no operative interest but increase the overall capacitance of the devices. Thus when a MOSFET is working, a part of the energy required to dynamically switch its state is wasted due to theses capacitors.

I.1.4 Device performance

As mentioned previously, the digital gates and circuits are based on the simultaneous use of PMOS and NMOS devices. One of the most basic element in a digital circuit is a CMOS inverter. This elementary brick is only composed by a NMOS and a PMOS having the same bias on their gate and sharing their drains (as shown in Figure I-6 (a)). Analyzing the performance of this elementary component allows to explain the behavior of more complex structures such as NOR and NAND gates. In particular the intrinsic delay of the inverter is a key parameter in dynamic regime.

As presented in Figure I-6 (b) and (c), when V_{in} is set at the supply voltage of the circuit (noted V_{dd}), the NMOS is in its ON-state and can thus be assimilated to finite resistance while the PMOS is in its OFF-state and can be assimilated to an open switch. Then, the output of the inverter is set to 0 V. On the contrary, when V_{in} is s*et at* 0 V the NMOS and PMOS are respectively in their OFF- and ON-state and thus V_{out} is set to V_{dd}. While one of them is used as a pull-up (output to V_{dd}), the other is used as a pull-down (output to GND) with always exactly one of them in its ON-state.

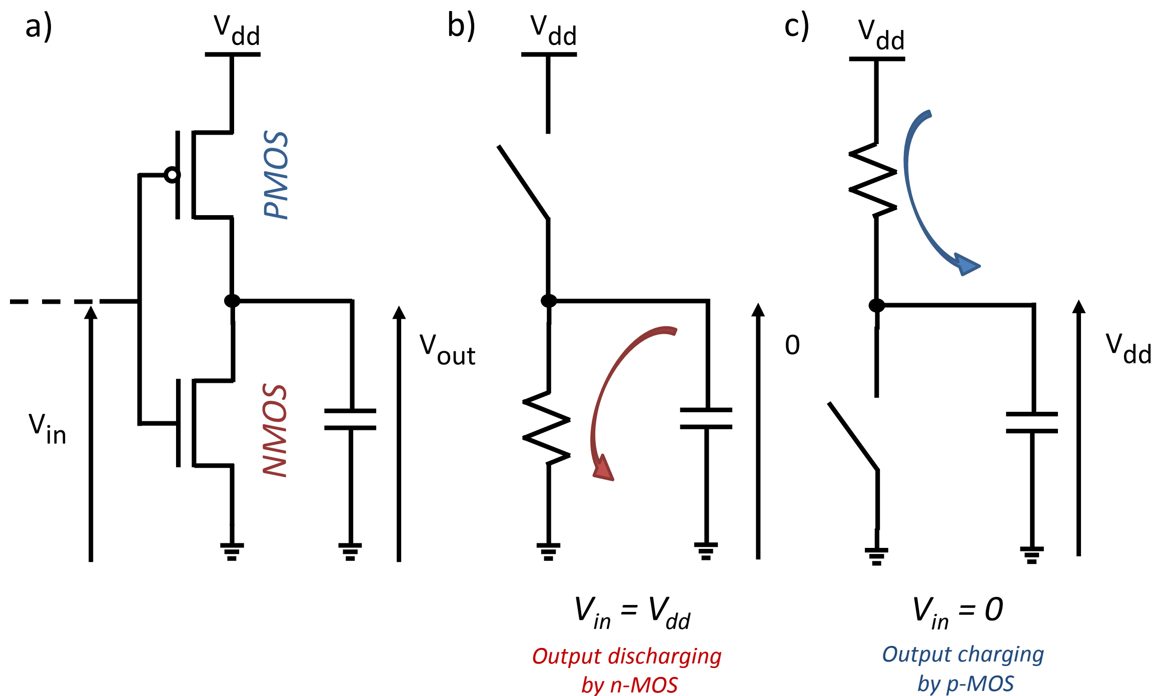


Figure I-6: (a) Static CMOS inverter where V_{dd} stands for supply voltage; (b) and (c) Model for respectively high and low input. In (b) and (c) the arrows represent the direction of the current.

The description above allows to understand the basic response of an inverter from a static point of view. Nevertheless, the transfer of the bias from the input to the output is not instantaneous and presents a transient signal. Indeed, the next stage is often itself composed by transistors. As introduced in Figure I-6, transferring a bias to the input of the next stage basically consists in charging the gate capacitance of a transistor at the considered bias through the channel resistance of the previous stage. Assuming, that the transistors continuously operate in saturation, the typical delay is approximated by Equation (I-20).

$$\tau_{int} = \frac{C_{g,tot} V_{dd}}{I_{d,sat}} = C_{g,tot} R_{ON} \quad \text{(I-20)}$$

With

$$R_{ON} = V_{dd}/I_{d,sat} \quad \text{(I-21)}$$

According to this simple model, it appears that the delay of an inverter increase with $C_{g,tot}$ and R_{ON}. While a part of these parameters is due to the functioning of the MOSFET and cannot be reduced such as C_{gc}, another part is mainly due to parasitic elements and strongly depends on the device geometry and implementation.

I.2 MOS scaling

For decades, one of the driving force of the microelectronics industry has been to reduce the dimensions of the transistor leading to an increase of the transistors density per chip and thus reducing the manufacturing price per transistor [*Moore_1965*]. Beyond the economical benefit, it was also shown that such a reduction of dimensions would lead to a gain in terms of device performance [*Dennard_1974*].

In this section, while the first part will be dedicated to the main concepts of transistor scaling as well as the expected performance improvements, the second part will focus on the limitations of such scaling.

I.2.1 Costs reduction and performance improvement

As introduced previously, for many years the industry has been focusing on following the law predicted in 1965 by Gordon Moore [*Moore_1965*]. This law stipulates that in order to reduce the cost per transistor, and thus the cost to manufacture products, the number of transistors per unit area should be increased. Doing so implies introducing new technology enablers and funding research and development groups and then leads to an increase of the cost of a given wafer. Nevertheless, the density of transistors in this same wafer being increased the actual cost per transistor in reduced.

Even being just a prediction and not a physical law, this trend has been observed for decades. In 2014, this same trend was still presented as relevant and achievable for next generation transistors as shown in Figure I-7 [*Bohr_2014*].

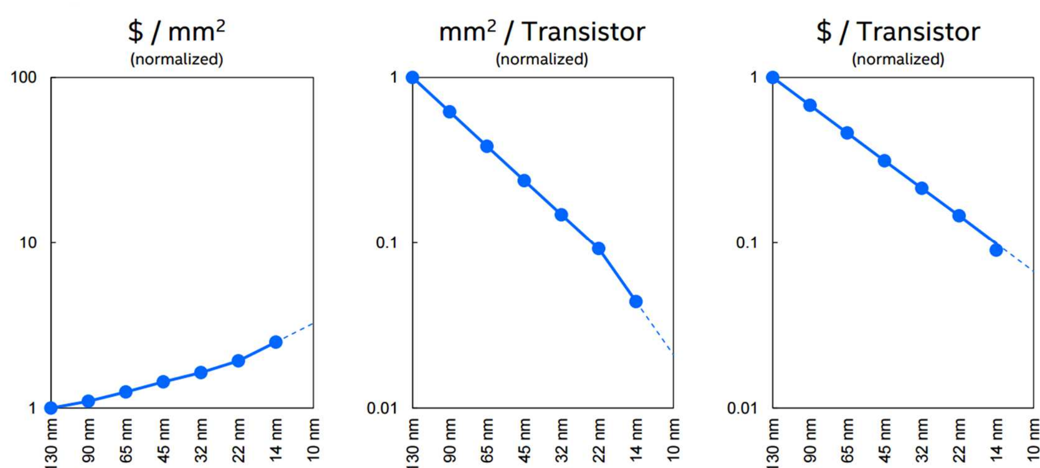


Figure I-7: Illustration of the reduction of the cost per transistor if following the scaling policy [Bohr_2014]

Practically, Moore's law predicts that the density of transistors on a chip has to double every two years to minimize manufacturing costs. Stated in another way, it means that the surface of a transistor has to be divided by two from one generation to the next one. Considering that the surface S^n of a transistor of the generation n is approximately given by its width W^n multiplied by its Contact Poly Pitch (noted CPP^n) as presented in Figure I-8, one can obtain $\{S^{n+1}, W^{n+1}, CPP^{n+1}\}$ from Equation (I-22) for the next node generation $n+1$.

$$S^{n+1} = \frac{S^n}{2} = \frac{W^n \times CPP^n}{2} = \frac{\sqrt{2}}{2} W^n \times \frac{\sqrt{2}}{2} CPP^n = W^{n+1} \times CPP^{n+1} \qquad \text{(I-22)}$$

From this equation, it appears that in order to reduce the area by a factor two, both the W^n and the CPP^n must be reduced by a factor ~0.7.

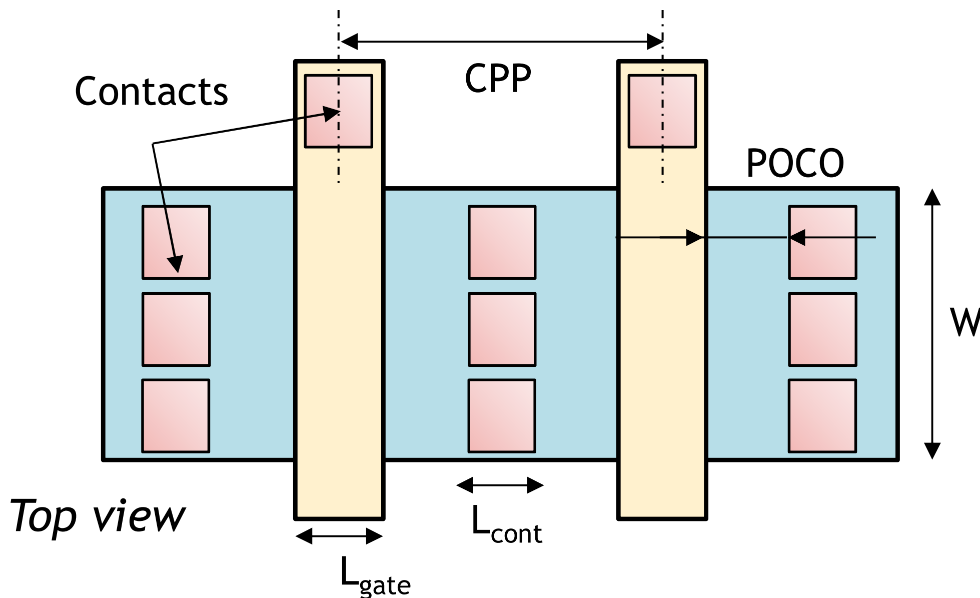


Figure I-8: Top view of two MOSFETs in series.

Besides presenting a financial interest, scaling the devices also present a real interest in terms of performance and energy consumption. The Dennard's law (named after Robert Dennard who wrote its founding paper) states that if one manages to scale all the dimensions of a transistor by a scaling factor named $1/\kappa$ thus all the electric quantities will scale with it [*Dennard_1974*]. Indeed, if the gate length and width are scaled by a factor $1/\kappa$ thus the R_{ON} can be considered as constant for a given set of materials. Thus dividing the bias by κ leads to a current also reduced by κ. If one roughly defines the power per device by Equation (I-23) and the delay by (I-24):

$$P = UI \tag{I-23}$$

$$\tau = RC = \frac{UC}{I} \tag{I-24}$$

then this power is multiplied by a scaling factor $1/\kappa^2$ and the delay by a factor $1/\kappa$. All these scaling changes are summed up in Table I-1. It is worth noting that dividing the power of a device by κ^2 while increasing the density by κ^2 actually leads to power density per unit of area constant with the scaling. This assertion is very important since it ensures no overheating due to device scaling.

Table I-1: Changes in integrated circuit performance which follow from scaling the circuit dimensions [Dennard_1974]

Parameter's Name	Parameter's Value	Scaling Factor
Device dimension	t_{ox}, L_g, W	1/κ
Doping concentration	N_d, N_a	κ
Voltage	U	1/κ
Current	I	1/κ
Capacitance	$C \approx \varepsilon W L_g / t_{ox}$	1/κ
Delay time / circuit	$\tau \approx UC/I$	1/κ
Power dissipation / circuit	UI	$1/\kappa^2$
Power density / area	UI/WL_g	1

Nevertheless, these Moore's and Dennard's laws were predicted during an era referred to as the "happy scaling years" where transistors were very large by today's standards. At this time, reducing the gate length was not a threat for the transistor functioning and the parasitic elements were negligible compared to the other device parameters. These years are now over and the improvements due to the classical scaling have reached saturation.

I.2.2 Scaling limitations

As we reached ultra-scaled devices, the parasitic elements presented in section I.1.3 become prevalent. Additionally, phenomena called short channel effects, appeared at the end of the happy scaling era, are becoming more and more predominant.

I.2.2.a Gate length reduction

In order to follow Moore's law and then to scale the CPP by a factor 0.7 from a node generation to another, the gate length has been reduced more and more aggressively over the past half century going from 10µm in 1971 to 22nm in 2014 (resp. [*Mueller_2006*] and [*Auth_2012*]). Nevertheless, for the latest generations scaling this length was not trivial since new phenomena appeared.

Indeed, as the gate length reaches the same order of magnitude as the depletion-layer widths of the source and drain junctions, these regions begin to overlap. Parasitic effects called Short Channel Effects (referred to as SCE) appear and lessen the electrostatic control of the channel by the gate [*Yau_1974*]. As presented in Figure I-9 for a NMOS, even if no bias is applied on the gate and the drain, the energy barrier in the channel is modified. Thus the gate loses a part of its electrostatic control on the channel leading in turn to threshold voltage reduction. This effect is often called itself Short Channel Effect even if this term gathers other phenomena. Moreover, the source and drain energy profiles being no longer independent, when a bias is applied to the drain an additional reduction of the channel barrier occurs and the threshold voltage is again reduced [*Troutman_1979*]. This second short channel effect is called Drain Induced Barrier Lowering (noted DIBL).

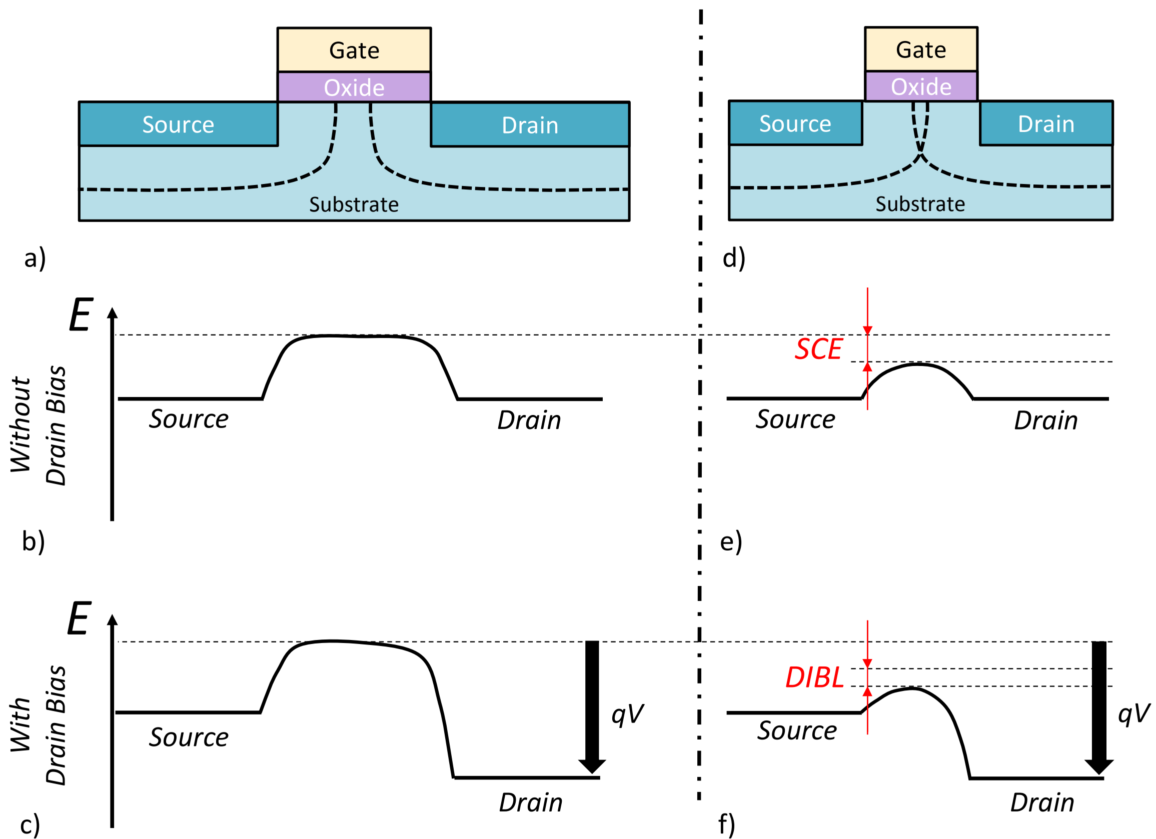


Figure I-9: Schematic of (a) a long-channel and (d) a short-channel MOSFET representing the depletion regions (dashed lines). The associated energetic diagram is plotted (b,e) without and (d,f) with drain bias.

The two phenomena discussed above lead to an I_{OFF} increase and a threshold bias roll-off. Therefore they mainly have an impact on the OFF-state and on the switching of the advanced nodes.

I.2.2.b Parasitic increase issue

Additionally to these short-channel phenomena another limitation of the scaling arises from the parasitic elements. Indeed as we scale the devices, the parasitic resistances and capacitances which were negligible for long-channel transistors become prevalent.

As presented previously, reducing the gate length L_g is limited since SCE and DIBL occur altering the electrostatic control of the channel. Thus in order to keep reducing the *CPP*, other dimensions have been recently reduced such as the *POCO* or the contact length L_{con} (see Figure I-8). Nevertheless, this approach also presents its own drawbacks.

Indeed, while reducing *POCO* would increase C_{spacer} (Figure I-5), reducing the contact length would increase the contact resistance R_{co} (Figure I-4) if the interface stays the same (Equation (I-16)). The example of the contact resistance is addressed in Figure I-10. As shown in this figure, reducing *CPP* while keeping a specific contact resistivity ρ_c of 10^{-8} Ω cm² would make the contact resistance R_{co} a major contribution of the total access resistance R_{access}.

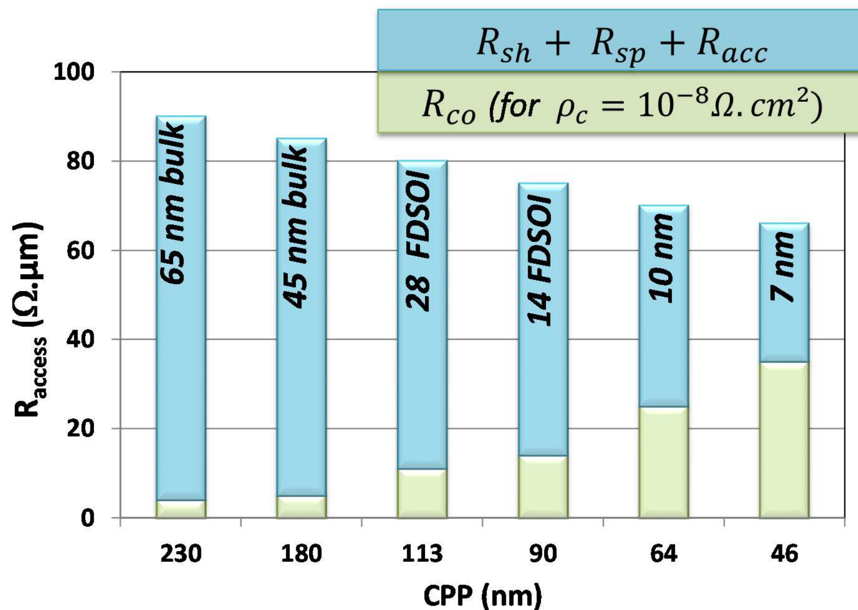


Figure I-10: Access resistance as a function of the Contact Poly Pitch singling out the contribution of the contact resistance [Hutin_2014]

I.2.3 Next node generations challenges

As presented before, the reduction of dimensions of the elementary nodes involves new challenges. New device architectures as well as innovative materials and processes have been proposed over the past 15 years in order to perpetuate a good electrostatic control of the channel ON and OFF states while reducing the parasitic resistance and capacitance contributions.

I.2.3.a Ensuring a good electrostatic control

Due to the preponderance of the short channel effects, new architectures have been adopted since the 32 nm node as alternatives to the Si-bulk MOSFET: the FinFET (Fin Field Effect Transistor) [*Hisamoto_1998*] and the FDSOI (Fully Depleted Silicon On Insulator) [*Colinge_1989*]. While the FinFET is a 3D device, the FDSOI remains a planar architecture. In both cases, the channel is no more doped with the complementary polarity of the transistor (P for NMOS and N for PMOS) but remains intrinsic. Even if the FinFET is mentioned in the following since it represents the leading candidate for advanced nodes, FDSOI transistor is more extensively described and has been used as elementary device in this thesis work due to its interest increase.

❖ FinFET

First introduced in mass production by Intel at the 22 nm node, this architecture is now widely used by most of the foundries; TSMC for its 16 nm and Samsung and Global Foundries for their 14nm. More recently a second generation of industrial FinFET was presented for the 14nm node of Intel [*Natarajan_2014*].

Being non-planar, the FinFET of Figure I-11 is represented in 3D in order to grasp the main features of this architecture. As one can notice that the operative part of the semiconductor (the source, the channel and the drain) has a high aspect ratio and is called *fin*. One transistor is composed of several fins with common source, drain and gate in order to ensure a high ON-state current. The channels are separated the one from another by a buried oxide.

The main advantage of this architecture is that the gate follows the topography of the fin. While in planar architecture only the top surface of the channel is perfectly controlled by the gate, in FinFET presenting thin fin almost all the channel is in the vicinity of the gate oxide and thus the whole fin is well controlled.

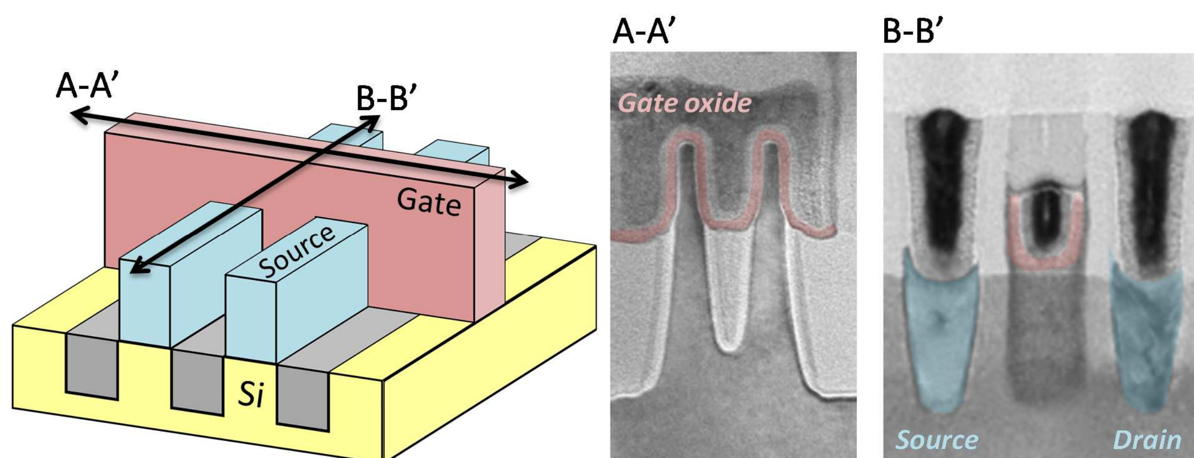


Figure I-11: 3D scheme of a FinFET and the corresponding cross sections A-A' and B-B' from [Natarajan_2014] (the scale are not precise in the original publication)

❖ FDSOI

This architecture has been mainly developed in the STMicroelectronics/CEA-LETI ecosystem during the past decade but begins to attract attention because of its relative simplicity compared to FinFET [*Gwennap_2016*]. Indeed, being planar, this architecture is more similar to the conventional bulk MOSFET than the FinFET. More recently, Global Foundries has announced the launch of a 22 nm node on a FDSOI platform.

The main characteristic of this architecture leans on the introduction of Silicon On Insulator (SOI) substrate which features a thin silicon top layer on top of a Buried Oxide (BOX). For ultra-thin SOI the channel is fully depleted and the transistor is called Fully Depleted Silicon On Insulator (FDSOI).

The principle of this architecture is similar than that of the FinFET: since it is ultra-thin (less than 10 nm), the whole depth of the channel is effectively controlled by the gate. However, FDSOI presents its own advantages and drawbacks. As shown in Figure I-12, the active zone is separate from the bulk substrate by the BOX thus avoiding one of the leakage current contribution. Moreover, this BOX can be used as a back gate. Even without back biasing the device, integrating a ground plane under the BOX with a doping specie opposed to the source and drain allow to increase the threshold voltage [*Fenouillet_2009*]. Thus using different ground planes on the same chip allows to implement multi V_t technology [*Weber_2010*]. In addition, a bias can be applied on this back gate and also modifies the threshold voltage of the devices.

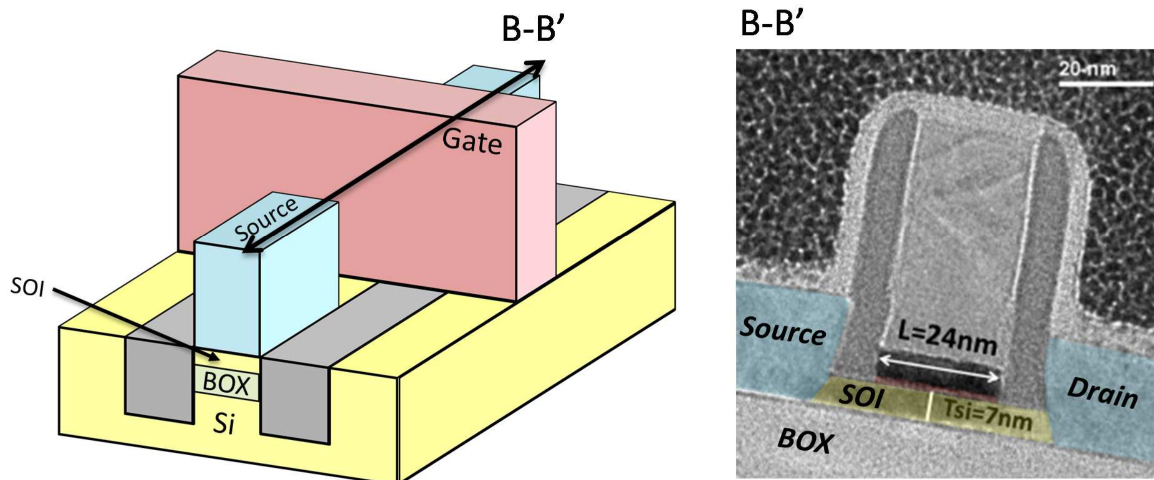


Figure I-12: 3D scheme of a FDSOI and the corresponding B-B' cross section from [Planes_2012]

I.2.3.b Parasitic contributions in new architectures

As presented previously in Equation (I-20), an increase in both parasitic capacitances and resistances would lead to an inverter delay increase and by extrapolation to a degradation of the circuits performance.

Therefore, in order to maintain device performance for reduced MOSFET dimensions, key technology and design enablers have to be identified. Trying to analyze the evolution of the market and to plan and control the technological needs of IC production, the International Technology Roadmap for Semiconductors (ITRS) has been periodically released over the past 20 years. In the issue of 2013 [*ITRS_2013*], the problematic of contact resistivity reduction was discussed and the target of 10^{-9} Ω cm² was mentioned as a key objective for next nodes device performance.

In this work, the parasitic contribution of the contact resistance is addressed. The two next sections are entirely dedicated to introducing the theory of an ideal contact as well as presenting phenomena occurring at real metal/semiconductor junctions. Finally, the state-of-the-art associated to the non-alloyed contact engineering is presented which represents the core of this thesis work.

I.3 Ideal contact theory

In this section, the different contributions of the contact resistivity are presented for the more intuitive case of an n-type semiconductor.

When a metal and an n-type semiconductor are brought together, a transfer of electrons occurs at the interface in order to reach an electrostatic equilibrium. The direction and the magnitude of the electron flow is determined by the difference between the metal work function (Φ_m) and that of the semiconductor (Φ_{sc}). One can distinguish two cases as explained in Figure I-13:

- If $\Phi_m > \Phi_{sc}$, the electrons flow from the semiconductor into the metal. This regime is called "depletion" since it induces a reduction of the density of carriers at the semiconductor surface. This flow of electrons generates a negative charge at the metal surface, counterbalanced by a positive charge in the semiconductor due to the presence of non-compensated ionized donor impurities.
- If $\Phi_{sc} > \Phi_m$, the electrons flow from the metal into the semiconductor. This regime is called "accumulation" since an excess of carrier is observed in the semiconductor. Therefore a negative charge (respectively positive) appears in the semiconductor (respectively in the metal).

In both cases, the zone of the semiconductor where the state of charge is different from a stand-alone semiconductor is referred to as Space Charge Region (hereinafter noted SCR). According to Gauss law these charges induce an electric potential and thus a built-in electric field which counters the electrons flow leading to an equilibrium. The two regimes are represented in Figure I-13 (b) and (c).

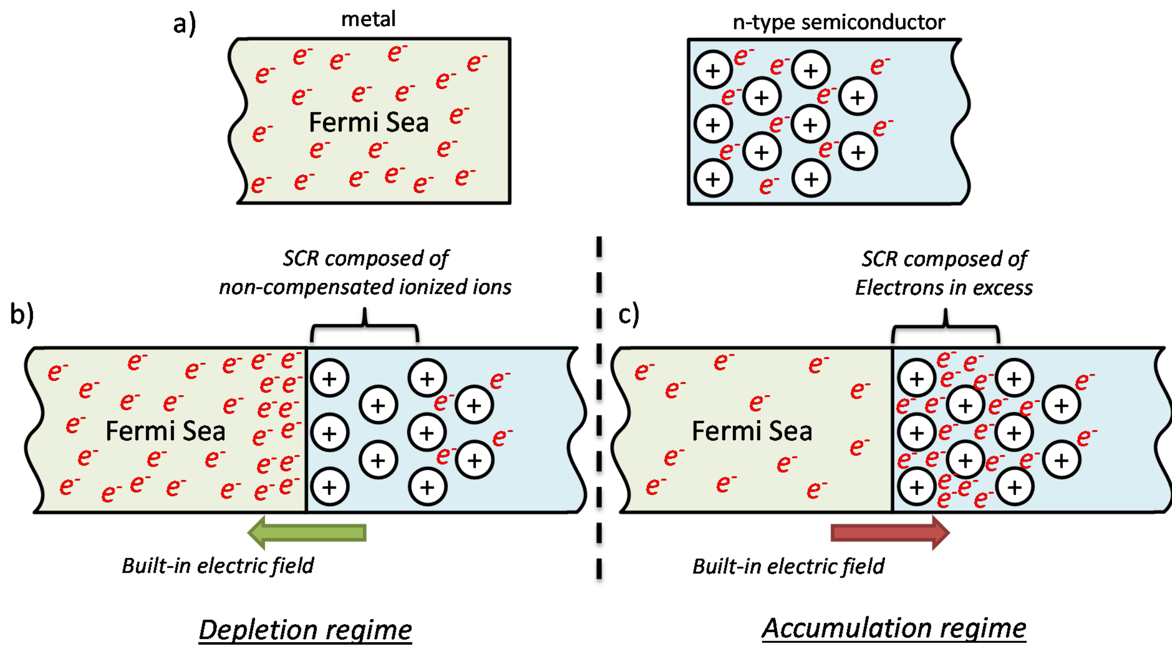


Figure I-13: (a) Reference case. (b) Depletion and (c) accumulation regime equilibria occurring when bringing a metal in contact with a n-type semiconductor

The surface charge modification and the induced electric potential generation have a strong impact on the electrostatic landscape of the semiconductor and thus on its energy band edge diagram. As presented in Figure I-14 (a) and (b), a bending of the energy band whose magnitude and sense depend on the difference between the metal and the semiconductor workfunctions appears in the SCR. In this figure, E_C, E_V and E_F respectively refer to the conduction and the valence bands of energy and the Fermi level.

The bending occurring in the SCR has a significant impact on the way the contact reacts to an electric bias; thus the cases $\Phi_m > \Phi_{sc}$ and $\Phi_{sc} > \Phi_m$ have antipodal behaviors.

As one can notice in Figure I-14 (c) and (d) which both represent the case of $\Phi_m > \Phi_{sc}$, when biasing the semiconductor the electrons have to go through the energetic barrier induced by the bending of the band diagram. While this barrier is always impeding the current when applying a negative bias on the metal, it can be overcome when applying a positive one. The contact response to an external electric bias is thus strongly asymmetric and one can define a reverse and a forward bias. This type of contact is often found highly resistive and is called Schottky.

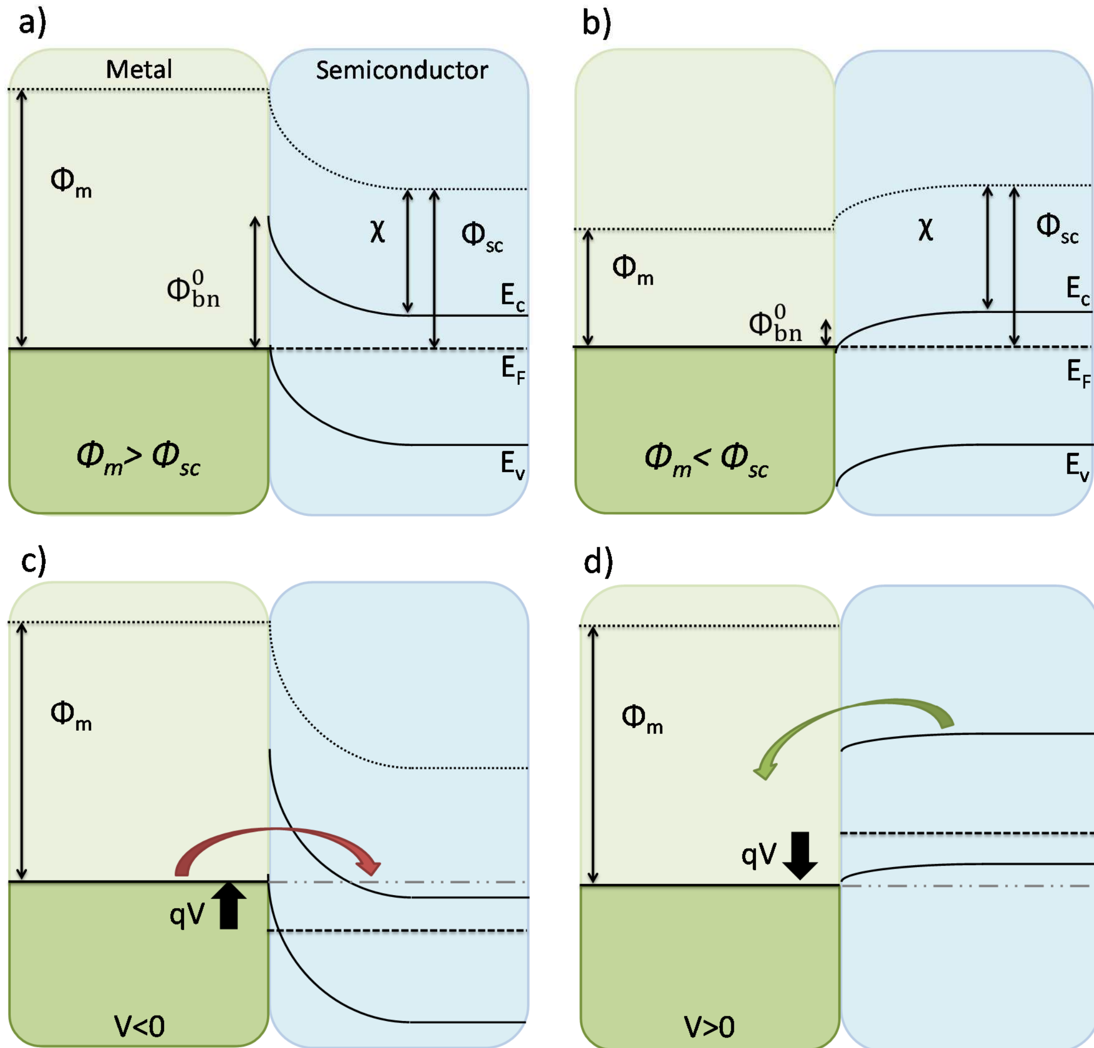


Figure I-14: Simplified band diagram of a metal/n-type semiconductor contact in (a) depletion and (b) accumulation regimes ; (c) and (d) represent the $\Phi_m > \Phi_{sc}$ *case under respectively a negative and a positive bias.*

On the contrary, in the case of $\Phi_{sc} > \Phi_m$ the electrons do not encounter any barrier whatever the bias is. Therefore the contact response to an external electric bias is linear and symmetrical. This type of contact is often found highly conductive and is called Ohmic. The typical shape of the current density as a function of the applied bias is represented for both types of contacts in Figure I-15 by only considering the thermionic theory. Even being simplified, this theory gives a first glimpse at the contact I-V characteristic asymmetric behavior by only considering the electrons flowing above the barrier but not through it (for detailed theory see Chapter II).

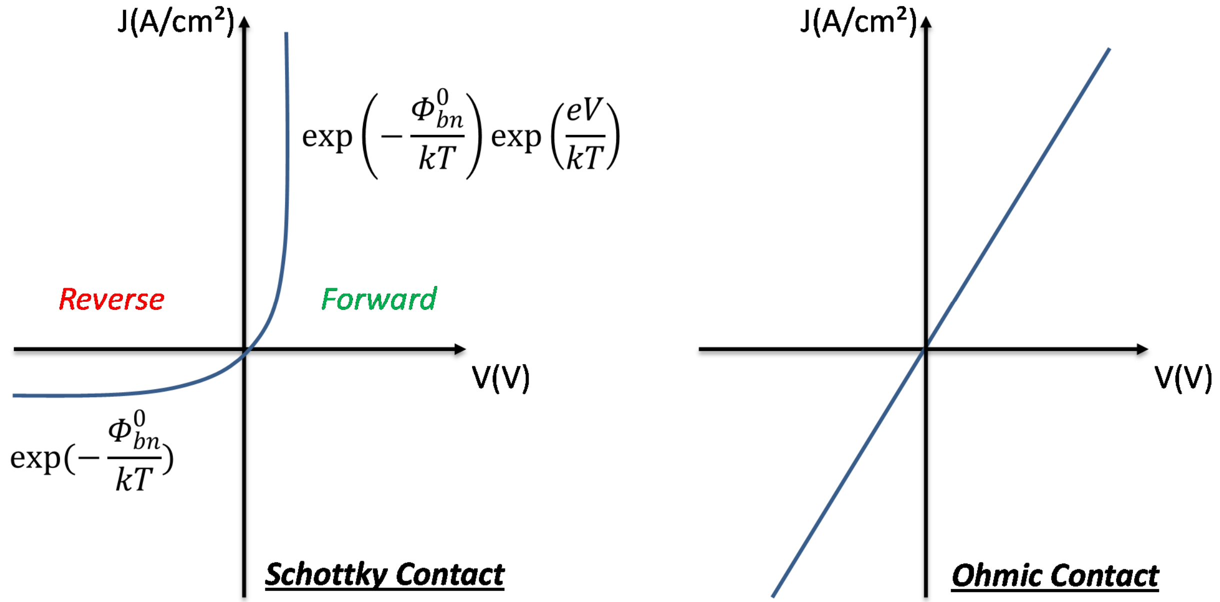


Figure I-15: Schematic of the current density as function of the contact bias for (left) Schottky and (right) Ohmic contacts when considering thermionic emission.

The height of the barrier induced by the band bending at the metal/semiconductor interface, called Schottky Barrier Height (SBH), is thus one of the major parameters to consider when trying to optimize a contact. Being noted Φ_{bn}^{0} in the following, one can determine this SBH from the simplified band diagram of Figure I-14 and obtain Equation (I-25).

$$\Phi_{bn}^{0} = \Phi_{m} - \Phi_{sc} \tag{I-25}$$

Proposed by Schottky [*Schottky_1940*], this theory implies that the electrical behavior of a contact can be totally tuned by choosing a metal with an adapted workfunction when trying to connect a given semiconductor. Following this theory, a high work-function metal would induce a large Schottky barrier on n-type semiconductor whereas a low work-function metal would lead to a small one.

A similar reasoning can be applied to a p-type semiconductor although the majority carriers to consider are holes. In this case, an Ohmic contact is obtained if the workfunction is high compared to the valence band of the semiconductor i.e. $\Phi_m > \Phi_{sc} + E_g$ while a Schottky one results from implementing a contact with a low workfunction metal i.e. $\Phi_m < \Phi_{sc} + E_g$.

Figure I-16 represents the gap of common semiconductors as well as the workfunction of several common metals. Following Schottky's ideal theory, implementing ohmic contacts should be easily addressed by selecting adapted metal workfunctions.

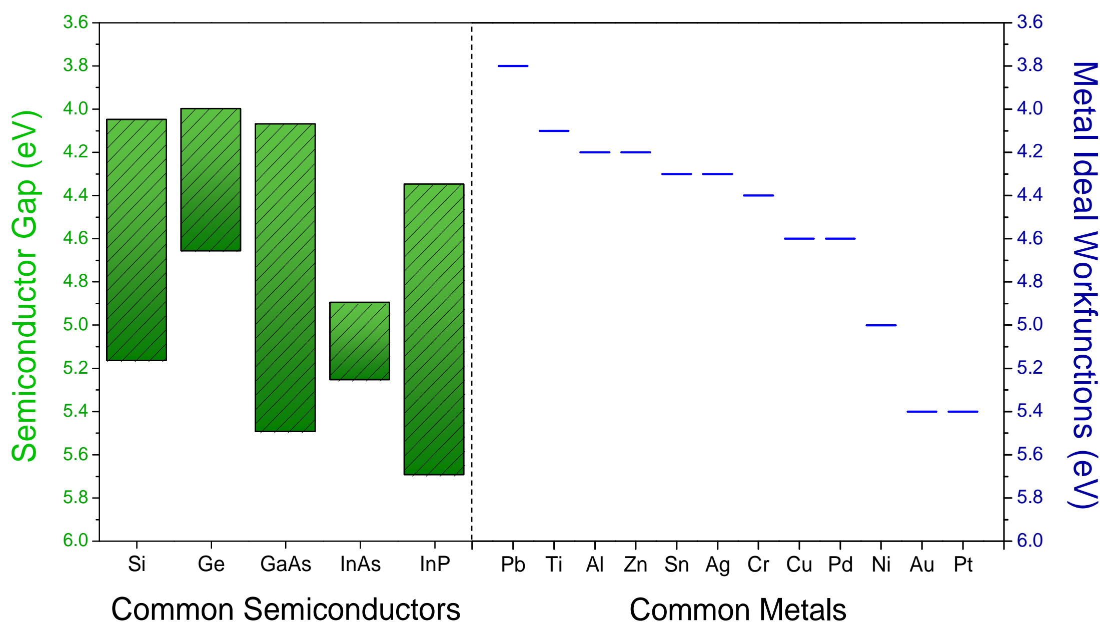


Figure I-16: Various metallizations and their corresponding ideal metal workfunction [Kulwicky_1991]

I.4 Real contact case

In a real metal/semiconductor contact, such a simplified theory cannot be considered. The band diagram as presented in Figure I-14 is actually strongly modified by energetic states generated at the interface.

I.4.1 Interface states

A metal/semiconductor junction being far from ideal, parasitic electrostatic defects distributed within the forbidden gap of the semiconductor appear at the interface. Several interface states origins have been proposed during the last forty years but no real consensus has been reached so far.

As proposed by Rowe in 1975 [*Rowe_1975*], the two main interface defects are Default-Induced Gap States also called intrinsic interface states (noted DIGS in the following) and Metal-Induced Gap States also called extrinsic interface states (noted MIGS in the following).

I.4.1.a Default-Induced Gap States

The evaluation of the properties of a semiconductor (e.g. its electronic affinity and forbidden gap of energy) often relies on considering a perfect crystal with an infinite lattice. When considering the surface of a semiconductor or its interface with another material this assumption is no longer true.

Therefore, the properties found for a bulk material cannot be applied in such a case. As presented in Figure I-17, all those surface imperfections, dangling bonds and foreign adatoms induce symmetry and periodicity breakings in the crystal. These defaults thus induce states of energy which are not taken in account in the bulk semiconductor theory. Those additional states can have their energy level in the forbidden gap of the semiconductor and are referred to as Default-Induced Gap States [*Bardeen_1947*].

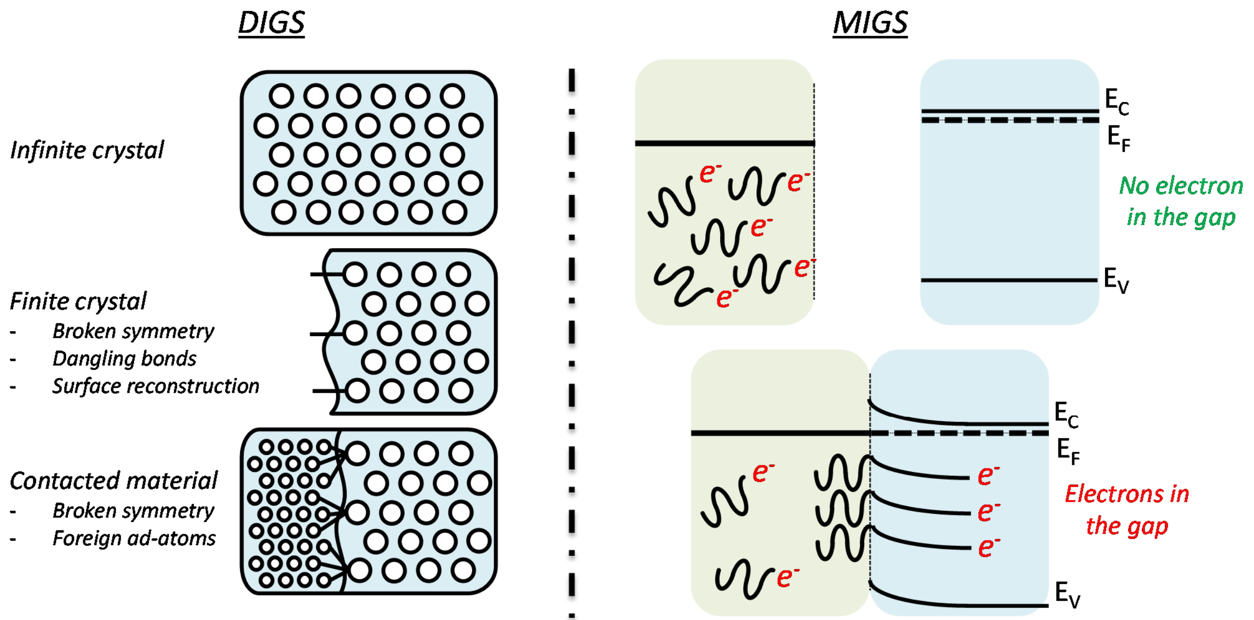


Figure I-17: DIGS and MIGS representations

Therefore these states can be observed on a bare semiconductor surface and their density should be modified by other materials deposition. Nevertheless, the induced modification mechanism is not clear and depends on the considered surface. According to Rowe [*Rowe_1975*], DIGS of a Ge(111) and Ge(100) are totally removed by metallization induced chemical bondings while DIGS of an Ge(110) seem to be insensitive to the metal overlayers.

I.4.1.b Metal-Induced Gap States

In order to explain the interface states origin at a Metal/Semiconductor (MS) interface without considering only defects, Hein proposed in 1965 a new theory based on the wave mechanics [*Hein_1965*]. The electrons in the metal can be considered as free and described by plane waves. When the metal is deposited on a semiconductor, these plane waves can penetrate in the conduction and valence bands as Bloch waves but also in the forbidden gap of energy. As shown in Figure I-17, in this range of energy, the plane waves can only penetrate by tunneling and act as evanescent waves. Therefore, they

only have significant amplitude in a few atomic layers from the interface (≈ 8 Å [*Hein_1965*], ≈ 3 Å [*Tersoff_1984*]). Additional states are thus generated only on several atomic layers and form a continuum of states in the band gap. They are called the Metal-Induced Gap States. According to Rowe, MIGSs should be the major source of gap states after a metallization since the major part of intrinsic states have been removed by chemical bonding [*Rowe_1975*].

I.4.2 Fermi Level Pinning

In this section, the notion of effective metal workfunction is introduced but a more detailed theoretical presentation of the energy band diagram calculation and its modification due to parasitic surface states is given in Chapter II.

Due to the presence of these interface states, the ideal model of M-S contacts is no longer relevant to describe real interfaces and SBHs are in practice found different from the theoretical predictions. Interestingly these effective SBHs are nearly independent from the metal workfunctions and are pinned around a given value depending on the considered semiconductor [*Bardeen_1947*]. This phenomenon is referred to as Fermi Level Pinning (noted FLP).

In 1947, Bardeen calculated that an interface states density $N_{it} = 10^{13} cm^{-2} eV^{-1}$ leads to a total pinning of the Fermi Level [*Bardeen_1947*]. At that time, such a density of interface states was quite common and DIGS seemed to be a good explanation for FLP. However, nowadays the interface quality having improved, interface states densities about $10^{10} cm^{-2} eV^{-1}$ are reached but the M-S contacts still present FLP. Thus DIGS theory is not sufficient to predict a high density of interface states. On the other hand, a study carried out by Hasegawa *et al.* [*Hasegawa_1999*] shows that the SBH depends also on the metal deposition conditions which cannot be explained by the MIGS model.

In practice in order to maintain the formalism of Schottky's theory, the effective SBH is often translated into an effective metal workfunction as shown in Equation (I-26).

$$\Phi_{bn}^{eff} = \Phi_m^{eff} - \Phi_{sc} \qquad \text{(I-26)}$$

The FLP is thus represented by the effective behavior of the metals when contacted to the semiconductor. As presented for the case of Si in Figure I-18, the actual control of the effective metal workfunction can be far from expected. Instead of having the possibility to control workfunction between

3 and 6 eV, the effective metal workfunction appear to be pinned around 4.7 eV, i.e. a midgap value, with only small variations around this point [*Nishimura_2008*].

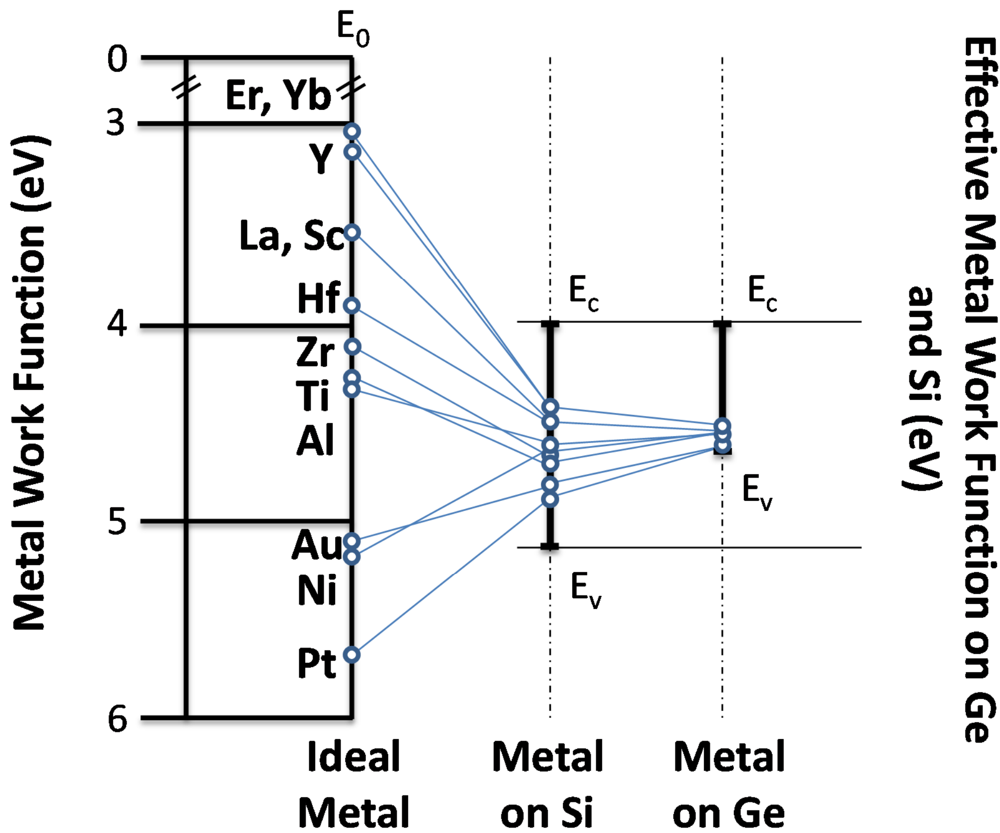


Figure I-18: Effective metal workfunction as a function of their ideal values for common metals when contacted to Si (adapted from [Nishimura_2008]).

Considering the energies of the conduction and valence bands of Si to be respectively 4.05 and 5.17 eV, contacts made on n- or p-Si in practice result in non-ohmic highly resistive junctions. Similarly, still in Figure I-18, the effective metal workfunctions on Ge are found to be really close to its valence band. Thus contacts to p-type and n-type Ge respectively result in ohmic and Schottky junctions.

I.5 Contact resistivity optimization

The FLP thus represents one of the major stumble blocks for future CMOS scaling since it prevents from reducing the contact resistivity and then leads to an increase of the contact resistance when reducing its area.

In order to tackle this issue, two paradigms are conceivable. Indeed, a rough approximation of the contact resistivity ρ_c is given by Equation (I-27) with K and ρ_{c0} two constants experimentally determined and N the doping concentration.

$$\rho_c = \rho_{c0}\exp[\frac{K\Phi_{bn}^{eff}}{\sqrt{N}}] \quad \text{(I-27)}$$

Then reducing the contact resistivity can be achieved by decreasing the effective SBH of the junction or by increasing the doping concentration.

I.5.1 Space charge region width reduction

When considering the transport theory in a contact, the simple model of thermionic emission (electron passing above the barrier) is not fully adequate since it does not encompass the quantum tunneling probability across the barrier. To do so, one has to involve Field and Thermionic Field Emissions (resp. FE and TFE) which are fully described in Chapter II. Basically, these theories, based on quantum tunnelling probability, assert that for sufficiently thin space charge region the major contribution to the transport is due to the electron tunneling through the barrier [*Padovani_1966*].

Referring to the space charge region width as W_{SCR}, Equation (I-28) gives its dependence on Φ_{bn}^{eff} and the doping concentration.

$$W_{SCR} = \sqrt{\frac{2\varepsilon}{q} \times \frac{\Phi_{bn}^{eff}}{N}} \quad \text{(I-28)}$$

Where ε is the dielectric constant (or relative permittivity) of the semiconductor and q is the elementary charge of the electron.

Increasing the doping concentration could thus lead to reducing the width of the space charge region while keeping the SBH constant. Nevertheless, reducing the contact resistivity using this approach requires to reach an ultra-high doping level at the interface. In some cases in order to ensure good transport properties despite a high SBH, the doping concentration has to reach values around its solubility limit in the considered semiconductor. Even being theoretically predicted, the solubility limit remains in practice difficult to achieve using conventional annealing processes and the actual electrically active dopant concentrations are lower than this value. For example, considering a midgap FLP in Si and thus a SBH about 0.55 eV and assuming an electrically active Arsenic concentration limit of 2×10^{20} cm^{-3}

[*Thompson_1998*], ρ_c is limited to about $1 \times 10^{-7} \Omega.\mathrm{cm}^2$, so that reaching the ITRS target is not achievable.

However, metastable configurations where the electrically active dopant concentration is close to the solubility limit can be obtained at ultra-high temperature using pulsed laser annealing [*Plummer_2001*]. Being metastable, the obtained system is very sensible to subsequent annealing steps such as silicide formation. Thus allowing a 2D uniform surface annealing, the pulsed laser would also be used to form the silicide since it is expected to provide locally higher temperatures without damaging the underlying layers [*Huet_2014*].

Recently, combining dopant activation by pulsed laser annealing with Ge amorphization of the source and drain prior to the silicidation, the record-low ρ_c of 1.5×10^{-9} $\Omega.\mathrm{cm}^2$ was reported [*Yu_2015*].

I.5.2 Effective SBH reduction via FLP mitigation

Recently, it was shown that a counter-intuitive approach aiming at reducing the FLP could consist in inserting a thin dielectrics at the interface between the metal and the semiconductor [*Connelly_2004*].

I.5.2.a MIS Contacts

The actual resistance of such contacts, called MIS (Metal/Insulator/Semiconductor), arises from a tradeoff between the SBH reduction through FLP mitigation and the tunnel resistance induced by the insertion itself.

The former, i.e. reducing the FLP, is still not well understood. Nevertheless, several mechanisms have been proposed to explain this effect and all seem to point out an interface states density decrease. In the following, the MIGS reduction model is mainly discussed and is extensively described in Chapter II. As presented in Figure I-19 (a), according to this model the insertion acts as an additional barrier which the plane waves of the metal have to cross in order to penetrate the semiconductor. Therefore, the density of metal plane waves actually going across the entire dielectric and penetrating the semiconductor forbidden gap of energy is lower than for a direct contact on semiconductor i.e. the density of MIGS is reduced [*Connelly_2004*]. Intuitively, the propensity of the insertion to screen the plane waves from the metal is linked to its thickness. The thicker the insertion, the lower the density of MIGS is. Moreover, for a given dielectric thickness, the attenuation of the MIGS density is proportional to the Band Gap of Energy (BGE) of the insertion.

Nevertheless, as presented in Figure I-19, as the insertion acts as a barrier for the parasitic plane waves responsible for the MIGS, it also acts as a barrier for the electrons responsible for current

conduction. For a given insertion thickness, the induced tunnel resistance for electrons (resp. holes) is related to the offset between the conduction (resp. valence) band of the dielectrics and that of the semiconductor. These parameters, presented in Figure I-20, are referred to as Conduction and Valence Band Offsets (noted CBO and VBO) and roughly speaking the higher they are, the higher the tunnel resistance per unit length is.

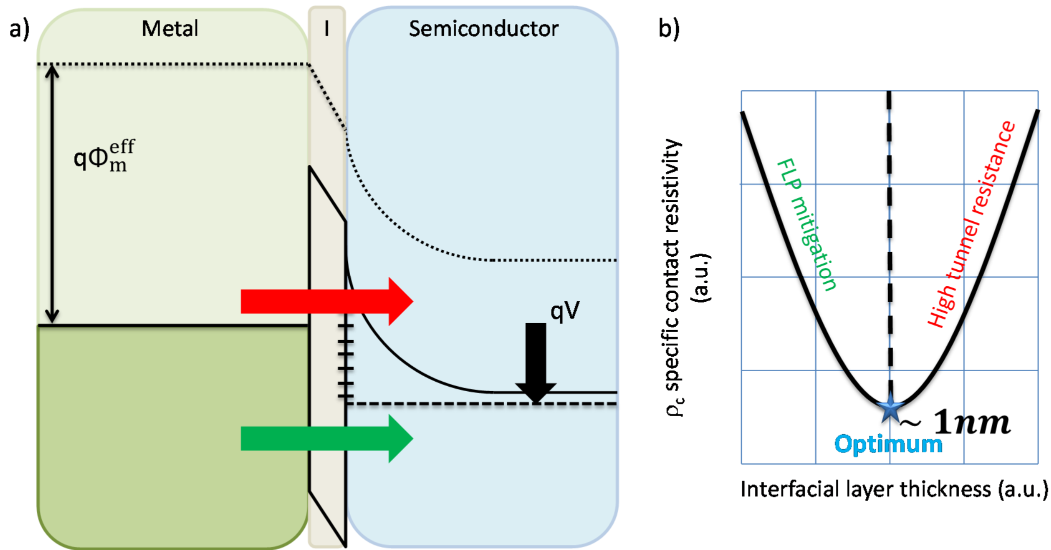


Figure I-19: (a) The band diagram shows that gap states face a larger minimum barrier than do free carrier states, and thus are more rapidly attenuated, allowing free carriers to tunnel while blocking the MIGS. (b) The optimum insulator thickness is where the gap states are effectively blocked while free carrier tunneling is still sufficient [Connelly_2004].

Finally, the total resistance is thus due to the tradeoff between those two contributions. As presented in Figure I-19 (b), the resistance as a function of the insertion thickness is a typical U-shape curve and the optimum thickness is obtained by finding the best compromise between the FLP mitigation and the induced tunnel resistance.

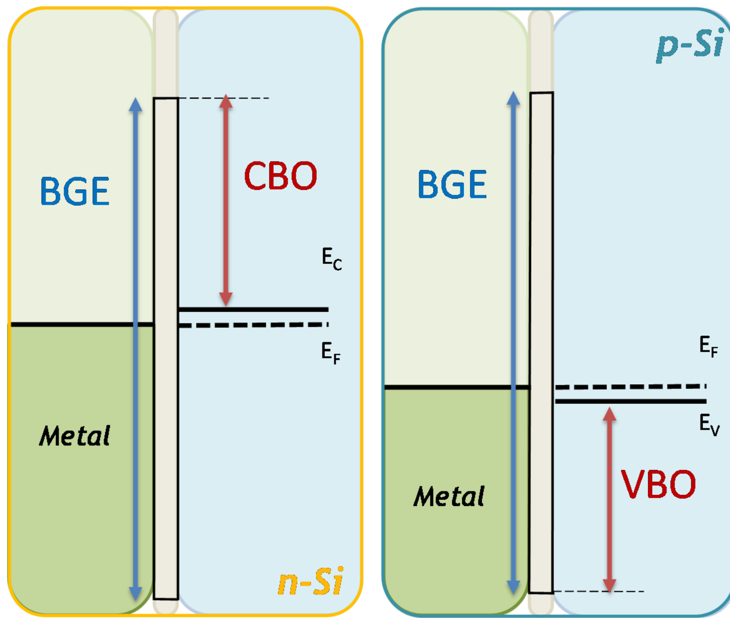


Figure I-20: MIS contact simplified band diagram illustrating the notions of Conduction and Valence band offsets respectively relevant when addressing n- and p-type semiconductors.

I.5.2.b State-of-the-art

Since 2004, many materials and deposition approaches have been reported. A summary of experimentally demonstrated MIS insertions is presented in Table I-2.

Table I-2: Experimental work on MIS structure. The dielectrics in blue present a low band offset compared to the semiconductor.

Semiconductor	Interface Layer	References
Si	Si_3N_4	Connelly_2004; Connelly_2006
	TiO_2	Agrawal_2014
	LaO_x; TiO_x; ZrO_x	Majumdar_2014
Ge	Ge_3N_4	Lieten_2008
	GeO_x; AlO_x	Nishimura_2008
	SiN	Kobayashi_2009
	MgO	Lee_2010; Zhou_2010
	Al_2O_3; TiO_2	Lin_2011; Lin_2012
	ZnO	Manik_2012
	TiO_2	Tsui_2013
	TiO_2/n^+Si	Menghini_2016
GeSn	$GeSnO_x$	Chen_2016
GaAs	SiN	Hu_2008 ; Hu_2009
	Al_2O_3	Hu_2010 ; Hu_2011''
InGaAs	Al_2O_3	Hu_2010
GaSb	TiO_2	Yuan_2011
MoS_2	Ta_2O_5	Lee_2016

Although those studies were mainly focusing on contact performance enhancement, some of them bring important physical considerations on both FLP origins and its mitigation mechanisms.

❖ Performance achievements

The contact enhancement can be seen from 2 main perspectives: evaluating its effective SBH or its electrical transport properties.

- *SBH reduction*

Using MIS contact approach, large SBH reductions have been observed. Being the firsts to propose the insertion of a dielectric, Connelly *et al.* reported a SBH reduction of 0.25 eV using Si_3N_4 between Mg and n-Si [*Connelly_2006*]. Nishimura *et al.* demonstrated similar results on Ge and obtained high SBH reduction of 0.41 eV in the Al/GeO_x/n-Ge system [*Nishimura_2008*]. The first results on III-V were introduced by Hu *et al.* who achieved a SBH reduction of 0.51 eV at the Er/n-GaAs interface [*Hu_2008*].

- *Contact resistivity reduction*

Although studying the effective SBH reflects the FLP mitigation, it does not give an indication on the actual contact resistivity which also includes the insertion-induced tunnel resistance. Studying this actual overall contact resistivity has led the community to focus on low band offsets dielectrics.

Indeed, the latest studies on MIS contacts aimed at reducing the tunnel resistance induced by the dielectric insertion. Lin *et al*. found that the current density of an Al/Al_2O_3/Ge stack is substantially affected by the dielectric thickness while in an Al/TiO_2/Ge stack the injected current remains high and almost constant when increasing the insertion thickness as shown in Figure I-21 [*Lin_2011*]. Doing so the highest reported SBH reduction value of 0.515eV was found to be associated with an increase of the injected current density at a bias voltage of 0.1 V by about 900 times. In 2012, Manik *et al.* worked on Ti/n-Ge junctions and managed to reduce again the dielectric-insertion-induced barrier by using doped ZnO as an interfacial layer [*Manik_2012*].

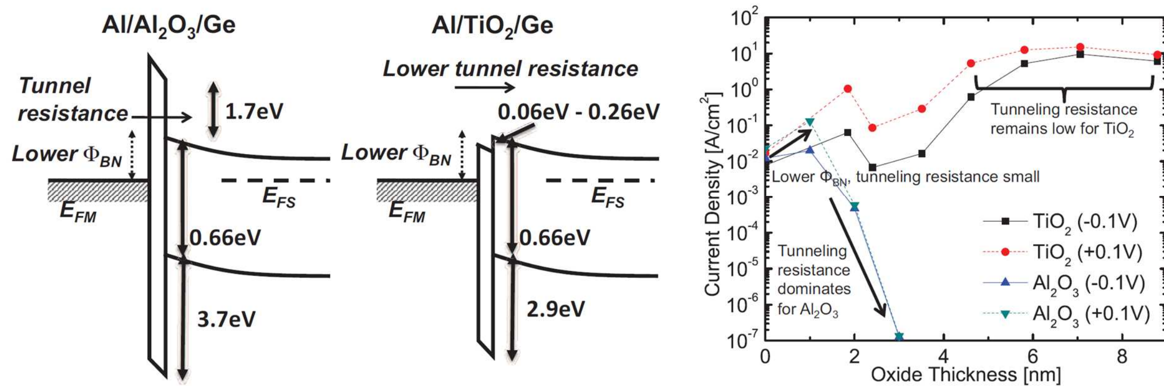


Figure I-21: (left) Band diagram comparison between high and low workfunction metals and (right) their respective impact on the current density at an Al/Ge interface [Lin_2011].

❖ Physical considerations

- *Investigation on the FLP origin*

On top of having a real interest in terms of contact performance, the study of MIS contacts can also help to identify the contribution of both the DIGS and the MIGS in the FLP. In 2010, Zhou *et al.* found that the FLP at the Fe/n-Ge interface was further reduced when using sulfur passivation of the Ge prior to Fe deposition than when inserting MgO between the two elements Fe and Ge [*Zhou_2010*]. The sulfur passivation was obtained by using aqueous $(NH_4)_2S$ and was supposed to act on the dangling bonds of the Ge. This seems to support that the surface states due to native defects at the Ge, which can be considered as DIGS, play a prevalent role in the FLP compare to MIGS.

- *Pinning at another value*

In 2012, Lin *et al.* presented a specific contact resistance study as a function of the oxide thickness in metal/TiO_2/n-Ge stacks where the top electrodes were Al, Pt and Ti [*Lin_2012*]. For all metals, the insertion of TiO_2 reduced the contact resistance. For Pt, which has an ideal metal workfunction that lies below the Ge valence band edge, Fermi-level depinning should actually increase the specific resistivity for n-Ge substrate. The opposite behavior being observed, the reduction of the contact resistance is more likely attributed to electric charges or dipoles at the metal/TiO_2 interface which effectively pin the metal Fermi level closer to the Ge conduction band edge rather than Fermi level depinning by interfaces state reduction.

I.5.3 Effective SBH reduction via dipole engineering

Recently a new way to act on the SBH has been investigated in the context of CMOS technology gate stack engineering. Working mainly on Si, it has been found that dipoles formation at a high-k/SiO_2 interface can lead to dramatic gate stack SBH shift [*Kamimuta_2007*].

I.5.3.a MIIS Contacts

Studies trying to adapt this method of SBH engineering in the frame of contact resistivity reduction were performed and are gathered in blue in Table I-3. In the following, such contacts are referred to as Metal Insulator/Insulator/Semiconductor (MIIS) contacts.

Table I-3: Experimental work on SBH engineering. The references in blue focus on MIIS contact applications.

Semiconductor	Interface Layer 1	Interface Layer 2	References
Si	SiO_2	HfLaOx	Yamamoto_2007
		HfO_2, Y_2O_3, Al_2O_3	Kamimuta_2007
		HfO_2, Al_2O_3	Iwamoto_2008
		HfO_2, Y_2O_3, Al_2O_3, La_2O_3	Kita_2008
			Coss_2009, Coss_2011
		AlOx, LaOx	Wang_2010
		HfO_2, La_2O_3	Charbonnier_2010
		HfO_2	Leroux_2013
		La_2O_3	Ang_2012
GaAs	TiO_2	HfO_2, Al_2O_3	Hu_2011’

Physical origins of such interfacial dipoles are not clear and several theories have been suggested. The most accepted theory was proposed by Kita and Toriumi [*Kita_2008*] and attributes the dipole formation to the difference of the dielectrics oxygen surface density (σ) at the interface. This difference should induce an oxygen transfer from the higher-σ to the lower-σ oxide. This transfer in a form of an O^{2-} is compensated by an oxygen vacancy Vo^{2+} and leads to the dipole creation as shown in Figure I-22.

A second theory, proposed by Kirsch *et al.* [*Kirsch_2008*], asserts that the interface dipole arises from the polarization of the interface chemical bonds and thus is proportional to the electronegativity difference between the components of these bonds. Some results of [*Kirsch_2008*] are in direct contradiction with the oxygen vacancy theory.

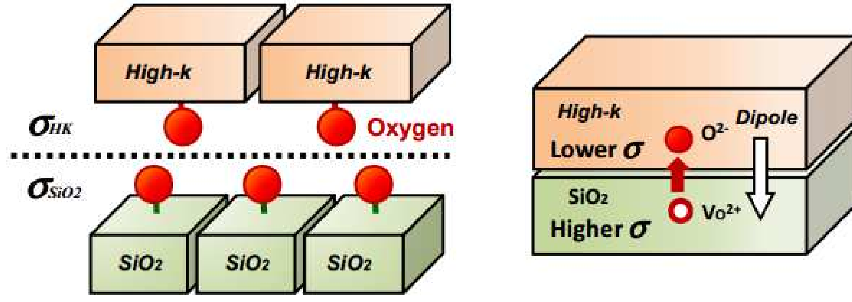


Figure I-22: Illustration of Kita and Toriumi's model for dipole generation. Under the difference between the surface oxygen densities of the two dielectric, transfer of O^{2-} occurs and creates a dipole [Kita_2008].

I.5.3.b State-of-the-art

❖ Gate stack studies

In order to clarify the contribution of the interfacial dipoles, studies were performed by Leroux *et al.* in 2010 and 2013 in TiN/HfO_2/SiO_2/Si stacks presenting various thicknesses of each dielectric [*Charbonnier_2010, Leroux_2013*].

Voltage drops attributed to dipoles, interface charges or bulk charges were considered in this study. The contribution of the charges at the interface between two materials noted mat_1 and mat_2 was calculated using Eqaution (I-29).

$$V = \frac{Q_{mat1/mat2}}{\varepsilon_{mat2}} \times t_{mat2} \tag{I-29}$$

where $Q_{mat1/mat2}$ is the density of charges per surface unit at the interface between mat_1 and mat_2, ε_{mat2} is the dielectric constant of mat_2 and t_{mat2} is the thickness of mat_2.

Similarly, the contribution of the bulk charges of a material noted mat_1 was calculated using Equation (I-30).

$$V = \frac{1}{\varepsilon_{mat1}} \times \int \rho_{mat1}(t)\, tdt \tag{I-30}$$

where $\rho_{mat1}(t)$ is the density of charges per volume unit at the depth t in mat_1.

Applying Equations (I-29) and (I-30) to the TiN/HfO_2/SiO_2/Si stacks, it was possible to link all these voltage drops to the flat band voltage (V_{FB}) and Equation (I-31) was obtained.

$$V_{FB} = \Phi_m - \Phi_{sc} - \delta V1 - \frac{Q_{Si/SiO2}}{\varepsilon_{SiO2}} \times t_{SiO2} - \frac{1}{\varepsilon_{SiO2}} \times \int \rho_{SiO2}(t)\, tdt - \delta V2 - \frac{Q_{SiO2/Hfo2}}{\varepsilon_{Hfo2}} \times t_{Hfo2} - \frac{1}{\varepsilon_{Hfo2}} \times \int \rho_{Hfo2}(t)\, tdt \quad \text{(I-31)}$$

where $\delta V1$ and $\delta V2$ are the interfacial dipoles, $Q_{Si/SiO2}$ and $Q_{SiO2/Hfo2}$ are the interfacial fixed charge densities per surface unit and ρ_{SiO2} and ρ_{Hfo2} are the densities of bulk charge per volume unit respectively in the SiO_2 and the HfO_2.

Using structures presenting a bevel of SiO_2, the dependence of V_{FB} as a function of the thickness of SiO_2 for different thicknesses of HfO_2 layers was measured and shown in Figure I-23 (a).

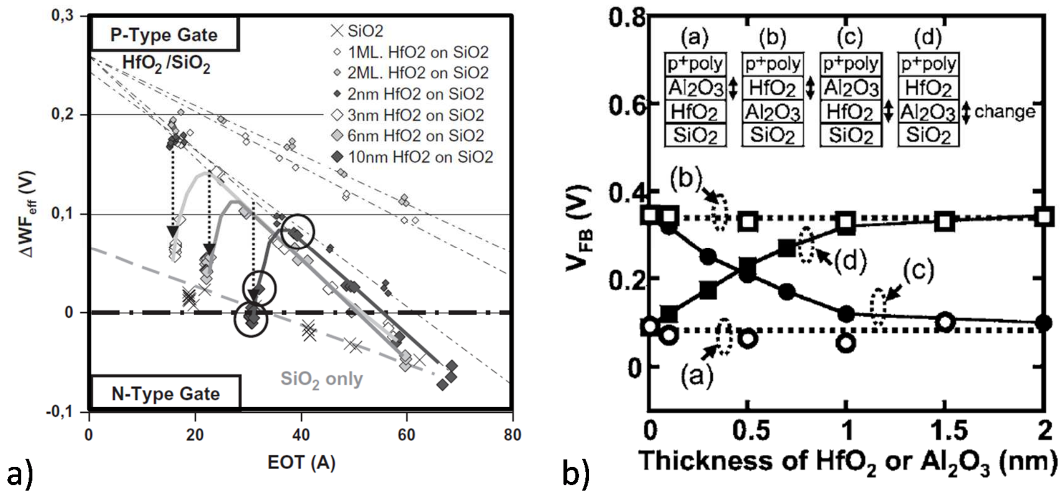


Figure I-23: Investigation of the interfacial charges, interfacial dipoles and bulk charges in dielectric multi-layers using (a) a bevel of SiO2 [Leroux_2013] and (b) three-layers stack with variable thickness [Iwamoto_2008]

The linear dependence of V_{FB} with SiO_2 thickness indicates that there is no bulk charge in this dielectric layer. Moreover the independence of the shift with the HfO_2 thickness at zero EOT (Equivalent Thickness Oxide) implies the presence of a dipole at one interface of the stack and the absence of any isolated fixed charge at HfO_2/SiO_2 interface or any bulk charge in the HfO_2 since any of them would lead to increasing shifts when HfO_2 thickness increases.

Investigating this aspect, Iwamoto *et al.* [*Iwamoto_2008*] studied various bilayer-high-k-dielectrics-based stacks. As shown in Figure I-23 (b), the V_{FB} shift only occurs when the thickness of the bottom high-k dielectric layer is changed indicating that the high-k/SiO_2 interface contribution is

dominant in the dipole formation. Moreover, the independence of V_{FB} saturation regarding the high-k thickness in Figure I-23 (b) also indicates that this V_{FB} shift is not due to the fixed bulk charges in the high-k.

Thus, these two studies seem to be in agreement with the fact that only the high-k/SiO_2 interface participates to the SBH engineering via the generation of interfacial dipoles.

❖ MIIS contacts

More recently, the work on dielectric-dipole-mitigated Schottky Barrier Height in gate stacks has been the origin of first studies of contact resistance reduction [Coss_2009 - Coss_2011'] [Hu_2011']. In these studies, dielectric bi-layer insertions were used in metal/semiconductor contacts in order to both unpin the Fermi level in the semiconductor and reduce the SBH by forming a dipole at the dielectric/dielectric interface.

The first study of Coss *et al.* [*Coss_2009*] consisted in comparing TaN/LaO_x/SiO_2/Si and TaN/AlO_x/SiO_2/Si contacts for both n- and p-type Si. It was found that the AlO_x insertion reduces the SBH on a p-type Si while increasing it on an n-type Si. The opposite observation was made for the LaO_x insertion. The results for a p-type substrate are presented in Figure I-24 (a).

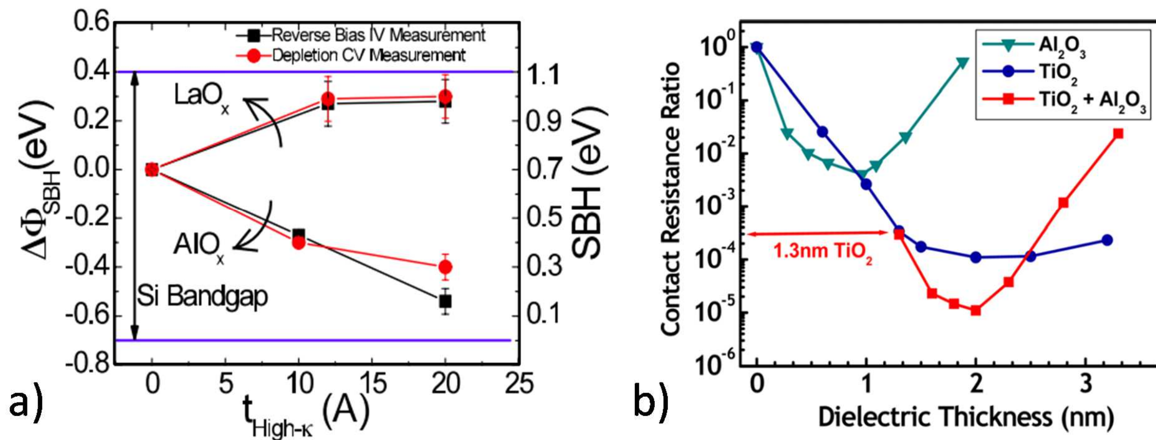


Figure I-24: (a) SBH modification induced by LaOx and AlOx layers on p-Si [Coss_2011] and (b) contact resistance modification induced by Al2O3, TiO2 or Al2O3 + TiO2 layers on GaAs [Hu_2011].

Presenting the same metallization, the ability to reduce the SBH in both n- and p-Si by just changing the high-k dielectric was attributed to dipole generation. Moreover the obtained dipole orientations are in good agreement with the dipole orientation predicted by Kita and Toriumi [*Kita_2008*]. In 2011, 40nm p-FinFETs with novel contacts were fabricated and shown to have reduced

parasitic specific contact resistivity compared to the control devices [*Coss_2011*]. A reduction of $10\ \Omega.cm^2$ was evaluated by statistical analysis and was probably due to a SBH reduction of 100 meV.

As shown in Figure I-24 (b), by comparing MIIS $Al/Al_2O_3/TiO_2$/n-GaAs and MIS Al/TiO_2/n-GaAs, Hu *et al.* observed that inserting 7 Å of Al_2O_3 additionally to a TiO_2 leads to an extra contact resistance reduction *[Hu_2011].* This enhanced bell curve was attributed to a dipole formation at the interface between the two high-k dielectrics.

Even not explicitly introduced by Kita and Toriumi's theory [*Kita_2008*] the dipole formation at the high-k/high-k interface should be in agreement with their model. Indeed, according to this model a dipole should be present between two oxides as long as they do not have the same oxygen atoms areal density. Nevertheless, before this study all the stacks were based on dipole formed at high-k/SiO_2 interfaces (such as LaO_x/SiO_2 or AlO_x/SiO_2) and interfaces between two high-k dielectrics were found to present no dipole (such as Al_2O_3/HfO_2 in [*Iwamoto_2008*] as mentioned above).

I.6 Chapter conclusion

In this chapter, key notions of CMOS technology are introduced. The tendency of miniaturization is also evoked in order to understand the limitations induced by the MOSFET parasitic elements.

In this framework, the importance of reducing the contact resistivity in order to maintain future nodes performances is emphasized. More particularly, the issues occurring at the metal/semiconductor contacts are presented in contrast with the ideal model.

The theory of effective Schottky Barrier Height reduction based on layer or bi-layer insertions is exposed as well as the state-of-the-art of this field. According to some studies, it appears that despite the tunnel barrier induced by the dielectric insertion an optimum configuration can be found in which the overall contact resistivity is lower.

I.7 Thesis Objectives

Most of the studies presented in the Chapter I were performed in a non-industrial environment and were more focused on achieving a proof of concept rather than implementing MIS or MIIS contacts in existing manufactured products with all their constraints.

Consequently, no attention has been so far dedicated to the efficacy of the dielectric insertion as a function of the doping concentration of the addressed semiconductor. Studies based on relatively low doped substrates exhibit high dielectric insertion efficacy whereas doping concentration needs to be high is most of the manufactured products. Additionally, when processing wafers containing both NMOS and PMOS, contacts to n- and p-type semiconductor as to be performed. Therefore the solution chosen to address the contact resistivity reduction has to be efficient on both polarities of substrate and should not lead to an extensive process complexity. However, most of the studies presented in the state-of-the-art focused on stand-alone contact optimization with no insight on co-integration.

Therefore, the work of this thesis consists in:

- Analyzing the optimal co-integration scheme of MIS contacts on n- and p-type semiconductors presenting relatively high doping concentration.
- Evaluating the impact such contacts have on advanced MOSFETs nodes.
- Implementing a MIS contact module in an industrial or semi-industrial environment using the materials commonly found in advanced microelectronics.
- Gauging the effective electrical properties of MIS contacts.

I.8 References

Ang_2012 **K. W. Ang, K. Majumdar, K. Matthews, C. D. Young, C. Kenney, C. Hobbs, P. D. Kirsch, R. Jammy, R. D. Clark, S. Consiglio, K. Tapily, Y. Trickett, G. Nakamura, C. S. Wajda, G. J. Leusnik, M. Rodgers and S. C. Gausepohl**; *Effective Schottky Barrier Height Modulation using Dielectric Dipoles for Source/Drain Specific Contact Resistivity Improvement*; IEEE International Electron Devices Meeting; 2012

Auth_2012 **C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki and K. Mistry**; *A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors*; Symposium on VLSI Technology; 2012

Bardeen_1947 **J. Bardeen**; *Surface States and Rectification at a Metal Semi-Conductor Contact*; Physical Review, Vol. 71; 1947

Bohr_2014 **M. Bohr**; *14 nm Process Technology: Opening New Horizons*; Intel Developer Forum; 2014

Charbonnier_2010 **M. Charbonnier, C. Leroux, V. Cosnier, P. Besson, E. Martinez, N. Benedetto, C. Licitra, N. Rochat, C. Gaumer, K. Kaja, G. Ghibaudo, F. Martin and G. Reimbold**; *Measurement of Dipoles/Roll-Off/Work Functions by Coupling CV and IPE and Study of their Dependence on Fabrication Process*; IEEE Transactions On Electron Devices, Vol. 57; 2010

Colinge_1989 **J.-P. Colinge;** *Thin-Film SOI Technology: The Solution to Many Submicron CMOS Problems;* IEEE International Electron Devices Meeting; 1989

Connelly_2004 **D. Connelly, C. Faulkner, D. E. Grupp and J. S. Harris**; *A New Route to Zero Barrier Metal Source/Drain MOSFET*; IEEE Transactions On Nanotechnology, Vol. 3; 2004

Connelly_2006 **D. Connelly, C. Faulkner, P. A. Clifton and D. E. Grupp**; *Fermi Level Depinning for Low Barrier Schottky Source/Drain transistors;* Applied Physics Letters, Vol. 88; 2006

Coss_2009 **B. E. Coss, W.-Y. Loh, J. Oh, G. Smith, C. Smith, H. Adhikari, B. Sassman, S. Parthasarathy, J. Barnett, P. Majhi, R. M. Wallace, J. Kim and R. Jammy**; *CMOS*

Band-Edge Schottky Barrier Height Using Dielectric-Dipole Mitigated (DDM) Metal/Si for Source/Drain Contact Resistance Reduction; Symposium on VLSI Technology; 2009

Coss_2009' **B. E. Coss, W.-Y. Loh, R. M. Wallace, J. Kim, P. Majhi and R. Jammy**.; *Near Band Edge Schottky Barrier Height Modulation Using High-Dielectric Dipole Tuning Mechanism*; Applied Physics Letters, Vol. 95; 2009

Coss_2011 **B. E. Coss, C. Smith, W.-Y. Loh, P. Majhi, R. M. Wallace, J. Kim and R. Jammy**; *Contact Resistance Reduction to FinFET Source/Drain Using Novel Dielectric Dipole Schottky Barrier Height Modulation Tuning*; IEEE Electron Device Letters, Vol. 32; 2011

Coss_2011' **B. E. Coss, W.-Y. Loh, H. C. Floresca, M. J. Kim, P. Majhi, R. M. Wallace, J. Kim and R. Jammy**; *Dielectric Dipole Mitigated Schottky Barrier Height Tuning Using Atomic Layer Deposited Aluminum Oxide for Contact Resistance Reduction*; Applied Physics Letters, Vol. 99; 2011

Dennard_1974 **R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous and A. LeBlanc;** *Design of Ion-Implanted MOSFET's with Very Small Physicla Dimensions;* IEEE Journal of Solid-State Circuits, Vol. sc-9; 1974

Fenouillet_2009 **C. Fenouillet-Beranger, S. Denorme, P. Perreau, C. Buj, O. Faynot, F. Andrieu, L. Tosti, S. Barnola, T. Salvetat, X. Garros, M. Cassé, F. Allain, N. Loubet, L. Pham-Nguyen, E. Deloffre, M. Gros-Jean, R. Beneyton, C. Laviron, M. Marin, C. Leyris, S. Haendler, F. Leverd, P. Gouraud, P. Scheiblin, L. Clement, R. Pantel, S. Deleonibus and T. Skotnicki**; *FDSOI devices with thin BOX and ground plane integration for 32 nm node and below*; Solid-Sate Electronics, Vol. 53; 2009

Gwennap_2016 **L. Gwennap**; *FD-SOI Offers Alternative to FinFET*; Microprocessor report, The Linley Group; 2016

Hasegawa_1999 **H. Hasegawa**; *Fermi Level Pinning and Schottky Barrier Height Control at Metal-Semiconductor Interfaces of InP and Related Materials*; Japanese Journal of Applied Physics, Vol. 38; 1999

Heine_1965 **V. Heine**; *Theory of Surface States*; Physical Review, Vol. 138; 1965

Hisamoto_1998 **D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu;** *A Folded-channel MOSFET for Deep-sub-tenth Micron Era;* IEEE International Electron Devices Meeting; 1998

Hu_2008 **J. Hu, D. Choi, J. S. Harris, K. Saraswat and H.-S. P. Wong**; *Fermi Level Depinning of GaAs Ohmic Contacts*, Device Research Conference; 2008

Hu_2009 **J. Hu, X. Guan, D. Choi, J. S. Harris, K. Saraswat and H.-S. P. Wong**; *Fermi Level Depinning for the Design of III-V FET Source/Drain Contact;* VLSI TSA; 2009

Hu_2010 **J. Hu, K. Saraswat and H.-S. P. Wong**; *Metal/III-V Schottky Barrier Height Tuning for Design of Nonalloyed III-V Field-Effect Transistor Source/Drain Contacts*; Journal of Applied Physics, Vol. 107; 2010

Hu_2011 **J. Hu, K. Saraswat and H.-S. P. Wong**; *Experimental Demonstration of $In_{0.53}Ga_{0.47}As$ Field Effect Transistors with Scalable Nonalloyed Source/Drain Contacts*; Applied Physics Letters, Vol. 98; 2011

Hu_2011' **J. Hu, K. Saraswat and H.-S. P. Wong**; *Metal/III-V Effective Barrier Height Tuning Using Atomic Layer Deposition of High-k/High-K bilayer Interfaces*; Applied Physics Letters, Vol. 99; 2011

Hu_2011'' **J. Hu, A. Nainani, Y. Sun, K. Saraswat and H.-S. P. Wong**; *Impact of Fixed Charges on Metal-Insulator-Semiconductor Barrier Height Reduction*; Applied Physics Letters, Vol. 99; 2011

Huet_2014 **K. Huet, I. Toqué-Tresonne, F. Mazzamuto, T. Emeraud and H. Besaucèle**; Laser Thermal Annealing: *A low thermal budget solution for advanced structures and new materials*; International Workshop on Junction Technology; 2014

Hutin_2014 **L. Hutin, O. Rozeau, V. Carron, J.-M. Hartmann, L. Grenouillet, J. Borrel, F. Nemouchi, S. Barraud, C. Le Royer, Y. Morand, C. Plantier, P. Batude, C. Fenouillet-Béranger, H. Boutry, T. Ernst and M. Vinet**; *Junction Technology Outlook for Sub-28nm FDSOI CMOS*; International Workshop on Junction Technology; 2014

ITRS_2013 "International Technology Roadmap for Semiconductor (ITRS)"; 2013

Iwamoto_2008 **K. Iwamoto, Y. Kamimuta, A. Ogawa, Y. Watanabe, S. Migita, W. Mizubayashi, Y. Morita, M. Takahashi, H. Ota, T. Nabatame and A. Toriumi**; *Experimental Evidence for the Flatband Voltage Shift of High-k Metal-Oxide-Semiconductor Devices due to the Dipole Formation at the High-k SiO_2 Interface*; Applied Physics Letter, Vol.92; 2008

Kamimuta_2007 **Y. Kamimuta, K. Iwamoto, Y. Nunoshige, A. Hirano, W. Mizubayashi, Y. Watanabe, S. Migita, A. Ogawa, H. Ota, T. Nabatame and A. Toriumi**; *Comprehensive Study of V_{fb} Shift in High-k CMOS – Dipole Formation, Fermi-level Pinning and Oxygen Vacancy Effect*; IEEE International Electron Devices Meeting; 2007

Kirsch_2008 **P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker,**

H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H.-H. Tseng, R. Jammy, T. S. Boscke, D. J. Lichtenwalner, J. S. Jur and A. I. Kingon; *Dipole Model Explaining High-k/Metal Gate Field Effect Transistor Threshold Voltage Tuning*; Applied Physics Letters, Vol. 92; 2008

Kita_2008 **K. Kita and A. Toriumi**; *Intrinsic Origin of Electric Dipoles Formed at High-k/SiO_2 Interface;* IEEE International Electron Devices Meeting; 2008

Kobayashi_2009 **M. Kobayashi, A. Kinoshita, K. Saraswat, H. S. P. Wong and Y. Nishi**; *Fermi Level Depinning in Metal/Ge Schottky Junction For Metal Source/Drain Ge Metal-Oxide-Semiconductor Field-Effect-Transistor Application*; Journal of Applied Physics, Vol. 105; 2009

Kulwicky_1991 **B. M. Kulwicky**; *Humidity Sensors,* Journal of the American Ceramic Society, Vol. 74; 1991

Leroux_2013 **C. Leroux, S. Baudot, M. Charbonnier, A. Van Der Geest, P. Caubet, A. Toffoli, P. Blaise, G. Ghibaudo, F. Martin and G. Reimbold**; *Investigating Doping Effects on High-k Metal Gate Stack for Effective Work Function Engineering*; Solid-State Electronics, Vol. 88; 2013

Lieten_2008 **R. R. Lieten, S. Degroote, M. Kujik and G Borghs**; *Ohmic Contact Formation on n-type Ge*; Applied Physics Letters, Vol. 92, 022106; 2008

Lilienfeld_1925 **J. E. Lilienfeld;** *Method and Apparatus for Controlling Electric Currents*; US Patent No. 1,745,175; Filed October 22, 1925 in Canada and October 8, 1926 in US; Patented January 28, 1930

Lin_2011 **J. Y. J. Lin, A. M. Roy, A. Nainani, Y. Sun and K. C. Saraswat**; *Increase in Current Density for Metal Contacts to n-Germanium by Inserting TiO_2 Interfacial Layer to Reduce Schottky Barrier Height*; Applied Physics Letters, Vol. 98; 2011

Lin_2012 **J. Y. J. Lin, A. M. Roy and K. C. Saraswat**; *Reduction in Specific Contact Resistivity to n^+ Ge Using TiO_2 Interfacial Layer*; IEEE Electron Device Letters, Vol. 33; 2012

Manik_2012 **P. P. Manik, R. K. Mishra, V. P. Kishore, P. Ray, A. Nainani, Y.-C. Huang, M. C. Abraham, U. Ganguly and S. Lodha**; *Fermi-Level Unpinning and Low Resistivity Contacts to N-Type Ge with a thin ZnO interfacial layer*; Applied Physics Letters, Vol. 101; 2012

Moore_1965 **G. E. Moore**; *Cramming more components onto integrated circuits;* Electronics Magazine, Vol. 38; 1965

Mueller_2006 **S. Mueller**; *Microprocessor Types and Specifications*; Upgrading and Repairing PCs, 17th Edition; 2006

Natarajan_2014 **S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang and K. Zhang**; *A 14nm Logic Technology Featuring 2nd-Generation FinFET, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 m² SRAM cell size*; IEEE International Electron Devices Meeting; 2014

Ng_1986 **K. K. Ng and W. T. Lynch**; *Analysis of the Gate-Voltage-Dependent Series Resistance of MOSFET's;* IEEE Transactions on Electron Devices, Vol. 33; 1986

Nishimura_2008 **T. Nishimura, K. Kita and A. Toriumi**; *A Significant Shift of Schottky Barrier Heights at Strongly Pinned Metal/Germanium Interface by Inserting an Ultra-Thin Insulating Film*; Applied Physics Express, Vol. 1; 2008

Padovani_1966 **F. A. Padovani and R. Stratton;** *Field and Thermionic-Field Emission in Schottky Barriers*; Solid-States Electronics, Vol. 9; 1966

Plummer_2001 **J. D. Plummer and P. B. Griffin;** *Material and Process Limits in Silicon VLSI Technology;* Proceedings of the IEEE, Vol. 89; 2001

Rowe_1975 **J. E. Rowe, S. B. Christman and G. Margaritondo**; *Metal-Induced Surface during Schottky Barrier Formation on Si, Ge, and GaAs*; Physical Review Letters, Vol. 35; 1975

Schottky_ 1940 **W. Schottky**; *Abbweichungen vom ohmschen gesetz in halbleitern*; Phy. Z., 41:570; 1940

Simoen_1996 **E. Simoen, C. Claeys and J. Martino;** *Parameter Extraction of MOSFETs Operated at Low Temperature;* Journal de Physique IV Colloque; 1996

Sze_1981 **S. M. Sze**; *Physics of Semiconductor Devices*, 2nd edition; 1981

Tersoff_1984 **J. Tersoff**; *Schottky Barrier Height and the Continuum of Gap States*; Physical Review Letters, Vol. 52; 1984

Thompson_1998 **S. Thompson, P. Packan, T. Ghani, M. Stettler, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang and M. Bohr;** *Source/Drain Extension Scaling for 0.1 µm and Below Channel Length MOSFETs;* Symposium on VLSI Technology; 1998

Troutman_1979 **R. R. Troutman ;** *VLSI Limitations from Drain-Induced Barrier Lowering*; IEEE Journal of Solid-State Circuits, Vol. 14; 1979

Weber_2010 **O. Weber, F. Andrieu, J. Mazurier, M. Casse, X. Garros, C. Leroux, F. Martin, P. Perreau, C. Fenouillet-Beranger, S. Barnola, R. Gassilloud, C. Arvet, O. Thomas, J-P. Noel, O. Rozeau, M-A. Jaud, T. Poiroux, D. Lafond, A. Toffoli, F. Allain, C. Tabone, L. Tosti, L. Brevard, P. Lehnen, U. Weber, P.K. Baumann, O. Boissiere, W. Schwarzenbach, K. Bourdelle, B-Y Nguyen, F. Breuf, T. Skotnicki and O. Faynot**; *Work-function Engineering in Gate First Technology for Multi-V T Dual-Gate FDSOI CMOS on UTBOX*; IEEE International Electron Devices Meeting; 2010

Yamamoto_2007 **Y. Yamamoto, K. Kita, K. Kyuno and A. Toriumi**; *Study of La-Induced Flat Band Voltage Shift in Metal/$HfLaO_x$/SiO_2/Si Capacitors*; Japanese Journal of Applied Physics, Vol. 46; 2007

Yau_1974 **L. D. Yau;** *A Simple Theory To Predict Threshold Voltage Of Short-Channel IGFET's;* Solid-State Electronics, Vol. 17; 1974

Yu_2015 **H. Yu, M. Schaekers, E. Rosseel, A. Peter, J.-G. Lee, W.-B. Song, S. Demuynck, T. Chiarella, L-Å.Ragnarsson, S. Kubicek, J. Everaert, N. Horiguchi, K. Barla, D. Kim, N. Collaert, A. V. -Y. Thean, K. De Meyer**; *1.5<10-9 W.cm² Contact Resistivity on Highly Doped Si:P Using Ge Pre-Amorphization and Ti Silicidation*; IEEE International Electron Devices Meeting; 2015

Zhou_2010 **Y. Zhou, W. Han, Y. Wang, F. Xiu, J. Zou, R. K. Kawakami, K. L . Wang**; *Investigating the Origin of Fermi Level Pinning in Ge Schottky Junctions using Epitaxially Grown Ultrathin MgO films*; Applied Physics Letters, Vol. 96; 2010

Chapter II
MIS contacts modeling and simulation

Introduction to Chapter II 65
II.1 Analytical algorithm presentation 66
II.1.1 Fermi Level Pinning 67
II.1.2 1-D band edge diagram evaluation 75
II.1.3 J-V characteristics generation 80
II.2 Stand-alone contact J-V characteristics 90
II.2.1 Zero-barrier contact case 90
II.2.2 MIS contacts simulations 91
II.2.3 Partial conclusions 101
II.3 Impact on devices performance 103
II.3.1 DC impact 103
II.3.2 AC impact 108
II.4 Chapter conclusions 116
II.5 References 118

Introduction to Chapter II

As presented in Chapter I, according to recent academic researches Metal/Insulator/ Semiconductor (MIS) contacts are potential candidates to ensure reduction of access resistance for future CMOS technology nodes. Nevertheless, those studies were focused on stand-alone contact current-bias characteristics with no insight on neither the actual impact of such contacts on aggressively scaled devices, nor constraints in terms of n- and p-MOSFETs co-integration. Moreover, all the studies so far were performed in the static regime (DC) while it seems to be relevant for digital applications to evaluate the impact on time-dependent MOSFET performance (AC) when using MIS contacts.

In this chapter, modeling and simulation are used to identify the dielectric interlayers of interest in the framework of MIS contacts. After presenting the algorithm used in the analytical simulation, the intrinsic current-voltage characteristics of stand-alone contacts are generated. Then the impact of this MIS module is evaluated on MOSFETs in both DC and AC regimes.

The stand-alone contact part follows on highly standard works on solid-state physics [*Sze_1981, Mönch_1990* and *Mönch_1994*] but also on a more recent study developed in [*Gupta_2013*] focusing on MIS contacts on Ge. The third part, however, dealing with the impact on devices performance, is believed to be unprecedented.

II.1 Analytical algorithm presentation

The three parts of this section are dedicated to the modeling of the contacts. For the sake of simplicity these parts follow the algorithm of Figure II-1.

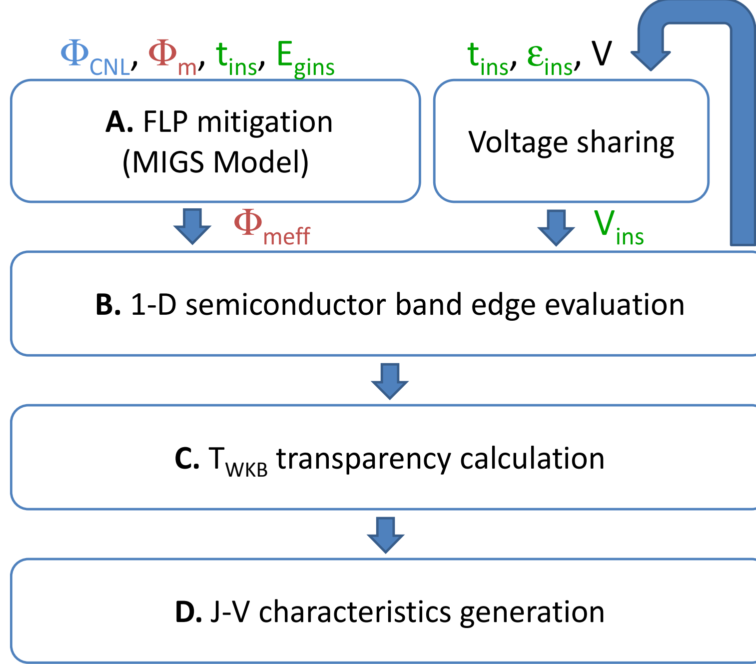


Figure II-1: Algorithm used for J-V calculations. The Metal Induced Gap States (MIGS) attenuation-based Fermi Level Pinning (FLP) alleviation and the Schottky Barrier Height (SBH) image force lowering are considered.

In this figure, the parameters above the boxes are the main physical values used as inputs for the simulations. Φ_{CNL}, Φ_m and E_{gins} stand for the charge neutrality level, the metal workfunction and the energy band gap of the dielectric insertion, respectively. As explained in section II.1.1.a, they are the main electrostatic parameters used to calculate the effective metal workfunction Φ_{meff}. t_{ins} and ε_{ins} are theoretical properties of the dielectrics and take part in the voltage sharing module (section II.1.2.b) and the tunneling probability calculation (section II.1.3.d).

After an extensive description of the physics of the Fermi Level Pinning (FLP) in the first sub-section, the second one is dedicated to its impact on the 1-D band-edge diagram of Metal/Semiconductors (MS) and Metal/Insulator/Semiconductor contacts (MIS). Models of interface electric transport are then presented in the third sub-section including thermionic, thermionic-field and field emissions theories as well as the Wentzel-Kramers-Brillouin approximation (T_{WKB}). The latter is then used to generate I-V characteristics of contacts as a function of the dielectric interlayer nature and thickness.

II.1.1 Fermi Level Pinning

As mentioned in Chapter I, the actual contact between a metal and a semiconductor is far from being ideal since it presents interface states which are not taken into account in the ideal Schottky's theory. These states have a major impact on the formation of the Schottky barrier and lead to consider an effective metal workfunction rather than an ideal one [*Freeouf_1981*].

In this section, the module used to calculate the effective metal workfunction as a function of the density of gap states is presented for the case on an n-type semiconductor.

II.1.1.a Effective metal workfunction expression

The typical physical quantity used to describe the gap states distribution is the Charge Neutrality Level noted CNL in the following and referred to as Φ_0 or Φ_{CNL} depending on the convention (see Figure II-2 (a) and (c)).

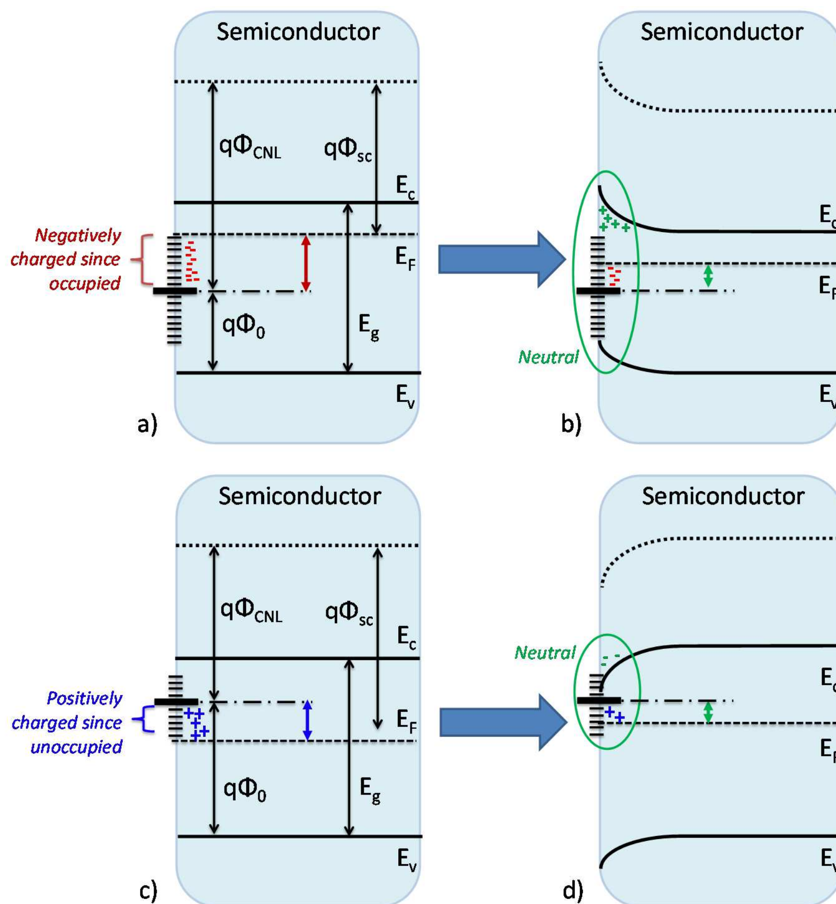


Figure II-2: Band-edge diagram illustrating the concept of charge neutrality level. The Fermi level at the surface is different from the bulk one since it tends to minimize the surface charge.

According to Tersoff, the CNL is an intrinsic property of the semiconductor. If describing the states in the gap of the semiconductor as a linear combination of valence and conduction Bloch states, then the CNL corresponds to the energy level where the gap states cross over from the valence- to the conduction-band dominated character [*Tersoff_1984*]. This level of energy is called the branching point.

The surface states above the CNL are acceptor-like (neutral if unoccupied and negatively charge if occupied) while the surface states below this level are donor-like (neutral if occupied and positively charge if unoccupied) [*Cowley_1965*]. Therefore, if Φ_0 is below the bulk Fermi level as in Figure II-2 (a), a global negative charge appears at the interface due to the occupied acceptor-like interface states. In order to counterbalance this negative charge, the Fermi level of the surface gets further away from the conduction band, generating more uncompensated positive ions. This leads to an expanding of the SCR and the band bending is increased bringing the Fermi level closer to Φ_0 (Figure II-2 (b)). Reciprocally, if Φ_0 is superior to the Fermi level (Figure II-2 (c)) a positive surface charge appears, the accumulation region expands bringing the Fermi level closer to Φ_0 at the surface as in Figure II-2 (d).

In both cases, the surface states tend to reduce the gap between the charge neutrality level and the Fermi level. In the extreme cases, when the surface states density is very high, the Fermi level is pinned around the charge neutrality level. This phenomenon is referred to as the Fermi Level Pinning (FLP).

When contacting a metal and a semiconductor, a charge transfer at the interface should also be accounted for. At equilibrium, the total charge of the semiconductor surface (the surface states plus the depletion region charges) is equal to the opposite of the charge on the surface of the metal.

This problem has been intensively studied over the years. The most common way to evaluate the impact of these charges has been to use the double-layer model [*Monch_1994*] also called the fixed-separation model [*Tung_2001*]. In this model, the net charge resulting from the gap states is assumed to be positioned at a fixed fictitious distance δ away from the metal. In this configuration, Gauss's law allows expressing the potential across the interfacial layer, leading to Equation (II-1) [*Sze_1981*].

$$\Phi_m - \Phi_{sc} - \Phi_{bn}^{eff} = \sqrt{\frac{2qN_d\delta^2}{\varepsilon_{sc}}\left(\Phi_{bn}^0 - \frac{kT}{q}\right)} - \frac{qD_{it}\delta}{\varepsilon_{sc}}\left(E_g - q\Phi_{bn}^{eff} - q\Phi_0\right) \qquad \text{(II-1)}$$

where Φ_m is the metal workfunction, Φ_{sc} is the semiconductor workfunction, ε_{sc} is the permittivity of the semiconductor, Φ_{bn}^{eff} is the effective Schottky barrier for the electrons, N_d is the donor impurities concentration, D_{it} is the interface states density and δ is the fictitious interfacial layer thickness.

One can introduce the quantities:

$$c_1 = \sqrt{\frac{2qN_d\delta^2}{\varepsilon_{sc}}} \; ; \; c_2 = \frac{qD_{it}\delta}{\varepsilon_{sc}} \; ; \; c_3 = \frac{\varepsilon_{sc}}{\varepsilon_{sc}+q^2D_{it}\delta} \qquad \text{(II-2)}$$

Considering N_d between 10^{18} and 10^{20} at.cm^{-3} compared to standards of microelectronic devices, ε_{sc} around 10^{-11} F.m^{-1} for silicon and D_{it} between 10^{14} and 10^{18} eV^{-1}.m^{-2}, c_1 can be neglected compared to c_2. The SBH can then be expressed by Equation (II-3).

$$\Phi_{bn}^{eff} = c_3(\Phi_m - \Phi_{sc}) + (1 - c_3)(\frac{E_g}{q} - \Phi_0) \qquad \text{(II-3)}$$

The quantity c_3 is frequently referred to as the “slope parameter” noted *S* and can also be defined as in Equation (II-4) [*Cowley_1965*].

$$S = \frac{d\Phi_m^{eff}}{d\Phi_m} \qquad \text{(II-4)}$$

It is representative of the controllability of the SBH level by the choice of the metal on a scale from 0 to 1. In an ideal contact when $D_{it} \to 0$, $S \to 1$ and the SBH is perfectly modulated by the metal work-function. In a totally pinned contact when $D_{it} \to \infty$, $S \to 0$ and the SBH is independent of the metal work-function.

As mentioned in Chapter I, instead of considering the contribution of both the ideal metal work function and the interface states, another way to express the Fermi level pinning using the fixed-separation model is to consider an effective metal work function as in Equation (II-5).

$$\Phi_m^{eff} = S\Phi_m + (1 - S)\Phi_{CNL} \qquad \text{(II-5)}$$

Using the previous definition of Φ_m^{eff}, Equation (II-6) is obtained.

$$\Phi_{bn}^{eff} = \Phi_m^{eff} - \Phi_{sc} \qquad \text{(II-6)}$$

The diagram from [*Nishimura_2008*] presented in Figure I-18 for the Si case can thus be plotted in another form using the concept of slope parameter as shown in Figure II-3.

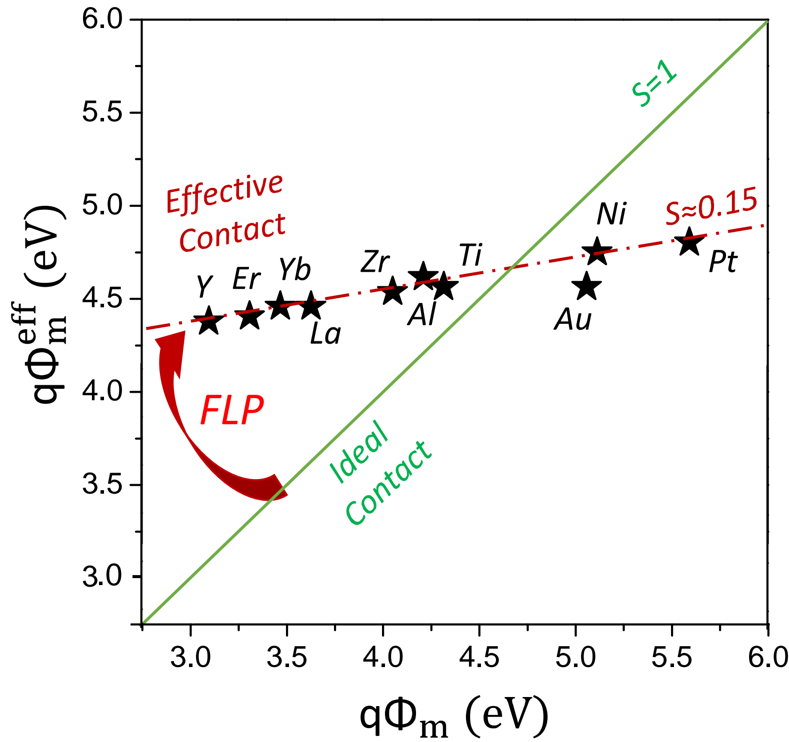


Figure II-3: Effective metal workfunction as a function of the ideal one from [Nishimura_2008]

As an illustration, the charge neutrality level Φ_0 of Ge has been located at 0.09 eV above the valence band and associated to a slope parameter S of 0.05 in [*Dimoulas_2006*]. These values confirm a strong FLP on Ge leading to effective metal workfunctions independent from the ideal ones and almost aligned to the valence band of Ge.

Except the density of interface states, all the parameters of this model are known when considering a given metal/semiconductor or metal/insulator/semiconductor system. Thus, this model allows calculating the effective metal workfunction as a function of the interface states density.

II.1.1.b Interface states density calculation

A way of evaluating the density of gap states at metal/semiconductor contacts was described initially by Mönch [*Mönch_1990*]. The main assumption of this model is to consider the Metal Induced Gap States (MIGS) as the main origin of the interface states. More recently, it was extended to MIS contacts on Ge in [*Gupta_2013*].

According to this model, the density of MIGS at the Metal/Semiconductor (MS) interface is given by Equation (II-7).

$$D_{MIGS}^{0} = \frac{2}{\pi a_{sc}^{2} E_g} \qquad \text{(II-7)}$$

where a_{sc} is the lattice parameter of the semiconductor contacted to the metal and E_g is its energy bandgap. Based on a penetration of electrons of the metal in the adjacent material as evanescent waves, the density of MIGS is expected to fall off exponentially with a decay length δ_{sc} given by Equation (II-8).

$$\delta_{sc} = \frac{h^2}{2\pi m_0 a_{sc} E_g} \qquad \text{(II-8)}$$

where m_0 is the free electron mass and h is Planck's constant. The density of MIGS at a distance *t* from the interface is then given by Equation (II-9).

$$D_{MIGS}(t) = D_{MIGS}^{0} e^{-\frac{t}{\delta_{sc}}} \qquad \text{(II-9)}$$

When the metal is directly contacted to the semiconductor, the density of MIGS at the MS interface can be evaluated by applying Equation (II-7) with the parameters of the considered semiconductor in II. 2. This value can thus be used to evaluate the slope parameter according to Equation (II-10).

$$S = \frac{\varepsilon_{sc}}{\varepsilon_{sc} + q^2 \delta D_{it}} = \frac{\varepsilon_{sc}}{\varepsilon_{sc} + q^2 \delta D_{MIGS}^{0}} \qquad \text{(II-10)}$$

One has to note that this expression is appropriate for a metal/semiconductor interface if only considering the MIGS as the source of the interface states. This expression is thus modified by the insertion of a dielectric.

II.1.1.c Impact of the dielectric insertion

Adding an Insertion Layer (noted IL below) between the metal and the semiconductor of a contact has two main effects: Equation (II-1) resulting from the resolution of the Gauss's law at the interface is modified and the actual density of MIGS in the semiconductor is reduced i.e. D_{it} is not equal to D_{MIGS}^{0} anymore.

Indeed, solving Gauss's law at the interface considering an interlayer presenting a thickness t_{IL} leads to a slope parameter S given by Equation (II-11).

$$S = \frac{\varepsilon_0(\varepsilon_{IL} \times \varepsilon_{sc})}{\varepsilon_0(\varepsilon_{IL} \times \varepsilon_{sc}) + q^2 D_{it} \times (\delta_{sc}\varepsilon_{IL} + t_{IL}\varepsilon_{sc})} \quad \text{(II-11)}$$

Additionally, as illustrated in Figure II-4 (a) and (b), the dielectric acts as a barrier for the electrons of the metal. The electrons propagate in the dielectric as evanescent waves, their amplitude drops and the probability for them to reach the semiconductor is lessened. Then the MIGS density observed at the semiconductor interface is reduced.

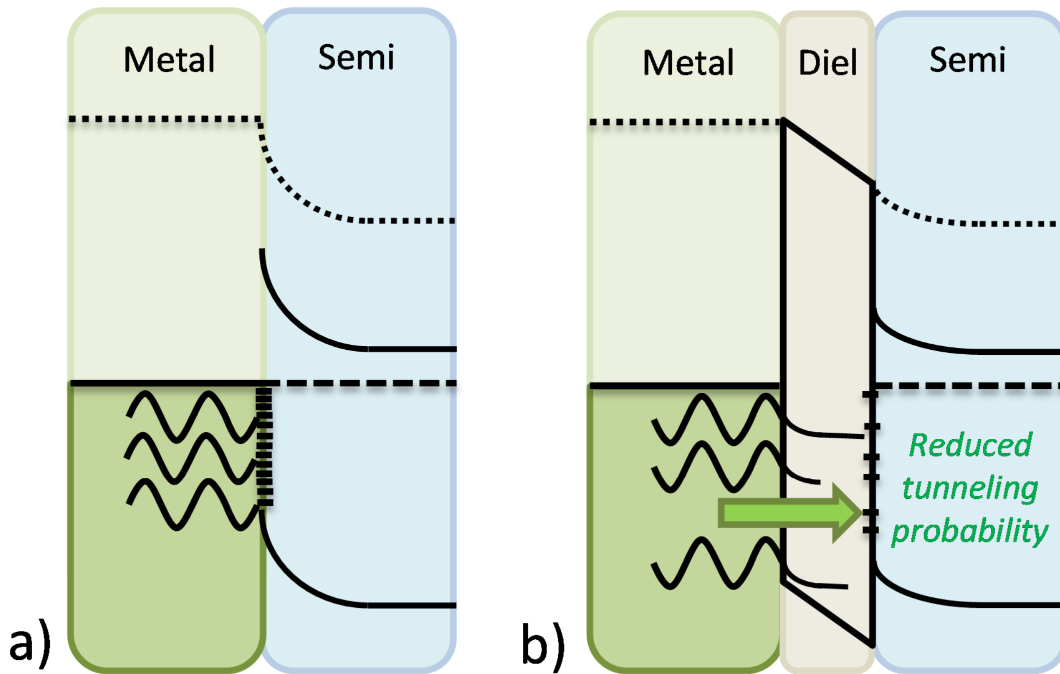
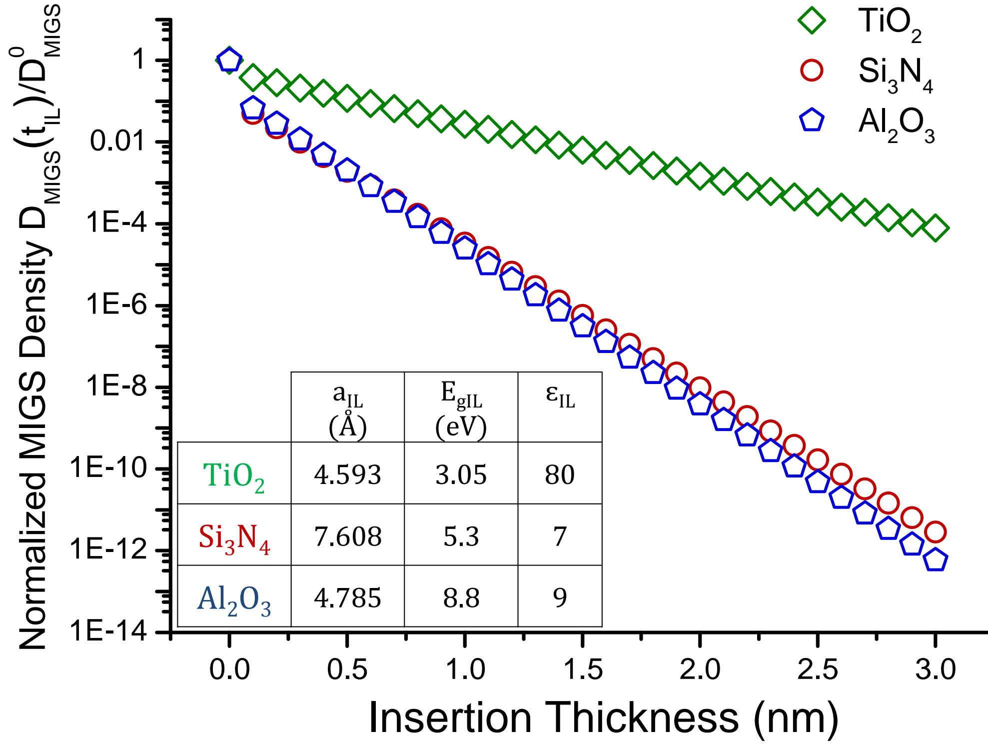


Figure II-4: (a) and (b) scheme of the energetic band edge diagram illustrating the role of barrier played by the dielectric.

Therefore, the actual density remaining at the insulator/semiconductor interface can be obtained by calculating the decay length of the insertion δ_{IL} using Equation (II-8) and substituting the dielectric insertion thickness t_{IL} in Equation (II-9). As an example, this model was used to evaluate the density of MIGS at the Si surface as a function of the dielectric thickness in the cases of TiO_2, Si_3N_4 and Al_2O_3 insertion. The results are shown in Figure II-5.



	a_{IL} (Å)	E_{gIL} (eV)	ε_{IL}
TiO_2	4.593	3.05	80
Si_3N_4	7.608	5.3	7
Al_2O_3	4.785	8.8	9

Figure II-5: Normalized calculated MIGS density at the surface of silicon for various dielectrics.

As illustrated by this figure, a discontinuity is observed at 0 nm. This value actually corresponds to a metal/semiconductor contact with no insertion between these two materials. Thus, passing from 0 to even 1 Å corresponds to a major change i.e. introducing the dielectric. This discontinuity is mathematically expressed in Equation (II-7), since changing the materials at the contact with the metal leads to a modification of D^0_{MIGS}.

Moreover, it appears that the Al_2O_3 and Si_3N_4 curves feature a steeper slope than that of the TiO_2. This difference arises from the disparity between the decay lengths of the considered materials. According to Equation (II-8), this characteristic length is inversely proportional to the product of the lattice parameter of a material times its gap of energy. Applying the calculation to the considered dielectrics leads for example to decay length around three times higher for the TiO_2 than the Al_2O_3.

Finally, the slope parameter to consider in a MIS contact is given in Equation (II-12).

$$S = \frac{\varepsilon_0(\varepsilon_{IL} \times \varepsilon_{sc})}{\varepsilon_0(\varepsilon_{IL} \times \varepsilon_{sc}) + q^2 D_{MIGS}(t_{IL}) \times (\delta_{sc}\varepsilon_{IL} + t_{IL}\varepsilon_{sc})} \qquad \text{(II-12)}$$

One can notice in this expression that D_{it} is not equal to D^0_{MIGS} anymore, but to $D_{MIGS}(t_{IL})$ which represents the density of MIGS having managed to go through the entire insertion.

The variation of S as a function of the density of MIGS is plotted in Figure II-6.

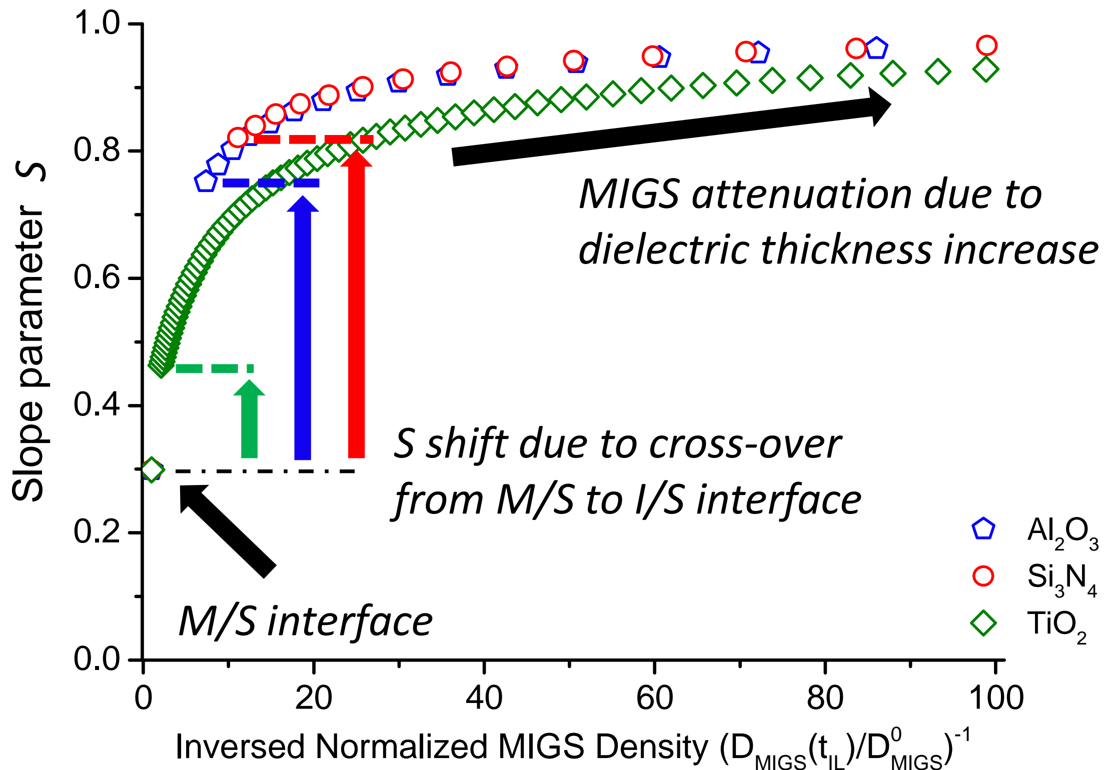


Figure II-6: Slope parameter S as a function of the inversed normalized MIGS density for Al_2O_3, Si_3N_4 and TiO_2 insertion layer.

As described previously, in Figure II-6, a first drop is observed when passing from a zero to a non-zero thick insertion corresponding to a change of the interface nature itself (MS to IS). This shift is inversely proportional to the decay length and leads to an almost direct depinning in the case of Si_3N_4 (slope parameter above 0.8 at ultra-thin insertion). Then one can see that when the remaining density of MIGS is only 1% of the initial value then the slope parameter S is close to the unity. Nevertheless, reaching this value is not achieved at the same thickness for all the dielectrics: around 3 Å for Al_2O_3 and Si_3N_4 and around 14 Å for TiO_2.

II.1.2 1-D band edge diagram evaluation

In this section the case of n-type Si is presented but similar developments can be extended to p-type Si and other semiconductors.

II.1.2.a The image force

Having expressed the slope parameter and thus the effective metal workfunction as a function of the insertion nature and thickness, the simulation can be used to generate the energy band-edge diagram.

A first refinement to consider in order to generate a Schottky barrier profile as realistic as possible is the image force or Schottky effect [*Fowler_1928*]. This effect arises from the exchange of charges between the metal and the semiconductor and is thus induced by a workfunction difference or an external bias. In this configuration, it can be shown that the electric field E_I created by an approaching carrier in the semiconductor at a distance x from the interface attracts a particle with an opposite charge being at a distance –x from the interface (Figure II-7).

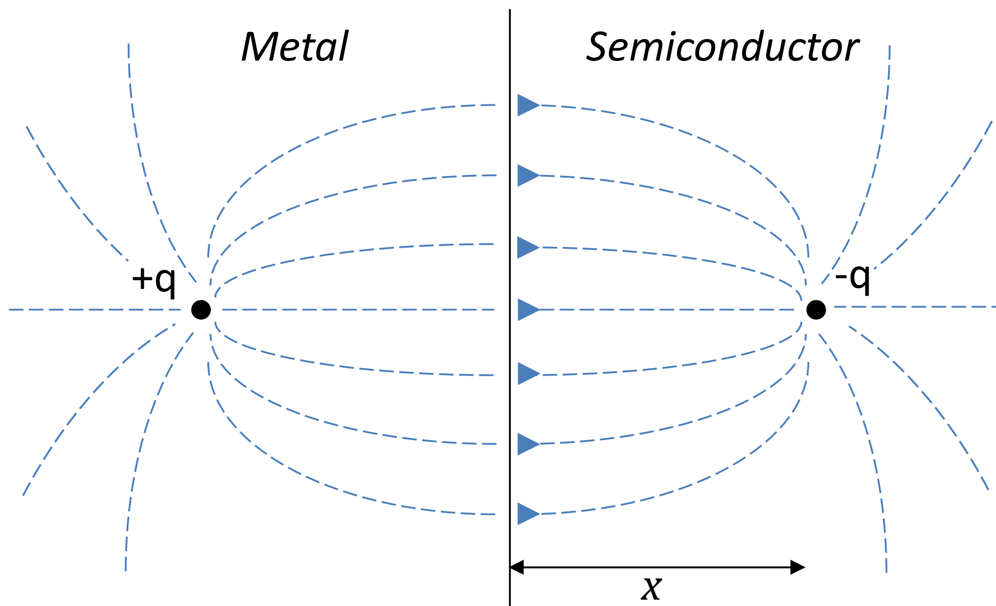


Figure II-7: Schematic of the electric field lines corresponding of two equal but opposite charges.

The electrostatic force between these two charges is given by Equation (II-13) and correspond to the potential in Equation (II-14).

$$F(x) = qE_I(x) = \frac{-q^2}{4\pi\varepsilon_{Si}(2x)^2} \quad \text{(II-13)}$$

$$\phi_I(X) = -\int_X^{\infty} E_I(x)dx = \frac{q}{16\pi\varepsilon_{Si}x} \quad \text{(II-14)}$$

Where $F(x)$ is the electrostatic force, $E_I(x)$ is the electrostatic field and $\phi_I(X)$ is the electrostatic potential. This induced potential needs to be added to the potential of the semiconductor i.e. to its band-edge diagram. Therefore the typical barrier modification occurring at the interface is pictured in Figure II-8.

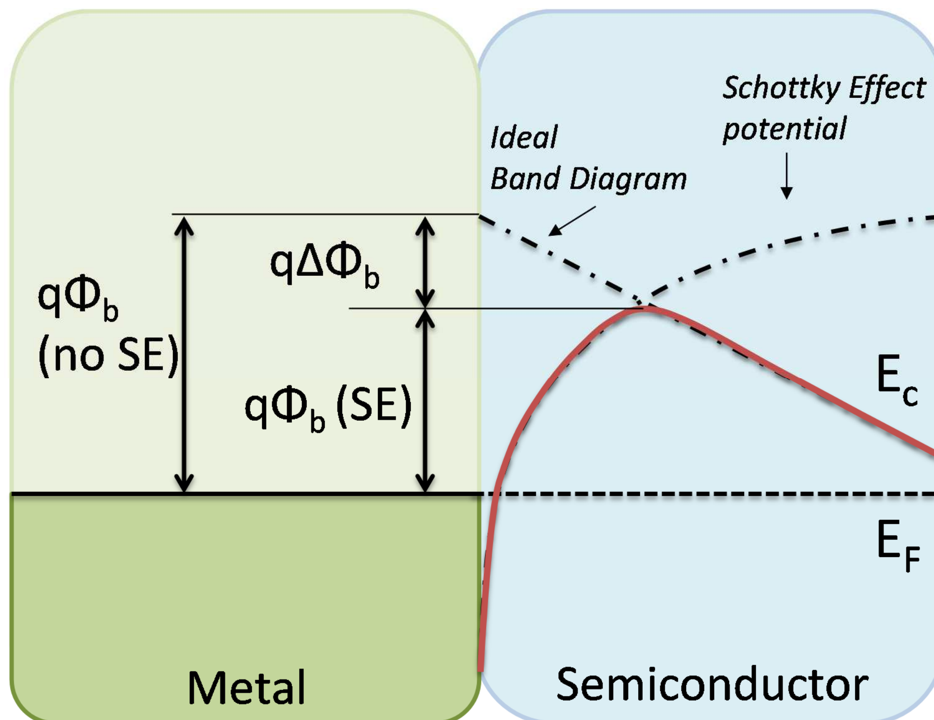


Figure II-8: Barrier lowering at a metal/semiconductor Interface due to image force. The initial barrier is assumed triangular.

One can see in this figure that the principal effect of the image force is to reduce the barrier at the interface. The magnitude of this correction is often negligible compared to the height of the barrier itself and thus have a small impact on the forward current. Nevertheless, the reverse current roughly having an exponential dependency with the SBH even a small variation has to be taken into account.

This mathematical model is however an approximate way to treat the Schottky effect. Indeed, as formulated in Equation (II-13), the carriers are considered as point charges and their electrostatic potentials are treated in a classical way. Nevertheless, some studies [*Harstein_1978*] have pointed out that such a problem should be treated with the quantum mechanics. In this paradigm, the carriers do not have a precise position *x* but have a probability $|\Psi(r,t)|^2$ to be observed at the distance *r* at a given time *t*. The image force potential induced by this charge at a distance *r'* is expressed in Equation (II-15).

$$F(r') = \int_{-\infty}^{0} \frac{q^2|\Psi(r,t)|^2}{2\varepsilon(r-r')} dr \qquad \text{(II-15)}$$

For electrons having their energy below the top of the barrier, the wave packet of the semiconductor are still considered as plane wave but the probability to find a carrier in the barrier is not $|\Psi(r,t)|^2$ but $TR|\Psi(r,t)|^2$, where *TR* is the probability of transmission. Therefore, for a carrier in the barrier, the Equation (II-15) leads to Equation (II-16).

$$F(r') = \int_{-\infty}^{0} \frac{q^2 TR|\Psi(r,t)|^2}{2\varepsilon(r-r')} dr \qquad \text{(II-16)}$$

This equation implies that the potential generated by a carrier depends on the probability of transmission - thus on the barrier's shape - and leads to a modification of the potential of the barrier. This problem is thus self-consistent and can be solved by iterative simulations [*Hutin_2010*].

II.1.2.b The voltage sharing issue

In order to be able to link the simulated band diagram with transport properties, its evaluation has to encompass the bias voltage. To do so, the effective potential difference $\Delta\phi^{eff}$ is defined using Equation (II-17). This physical value corresponds to the actual difference between the vacuum level of the two materials once having including the FLP and the applied bias.

$$\Delta\phi^{eff}(V) = \phi_m^{eff} - \phi_{Si} - V \qquad \text{(II-17)}$$

In this equation, the convention is that the bias voltage is applied on the metal and the ground is set on the Si.

This overall effective contact potential leads to a voltage sharing between the dielectric insertion and the semiconductor as shown in Figure II-9.

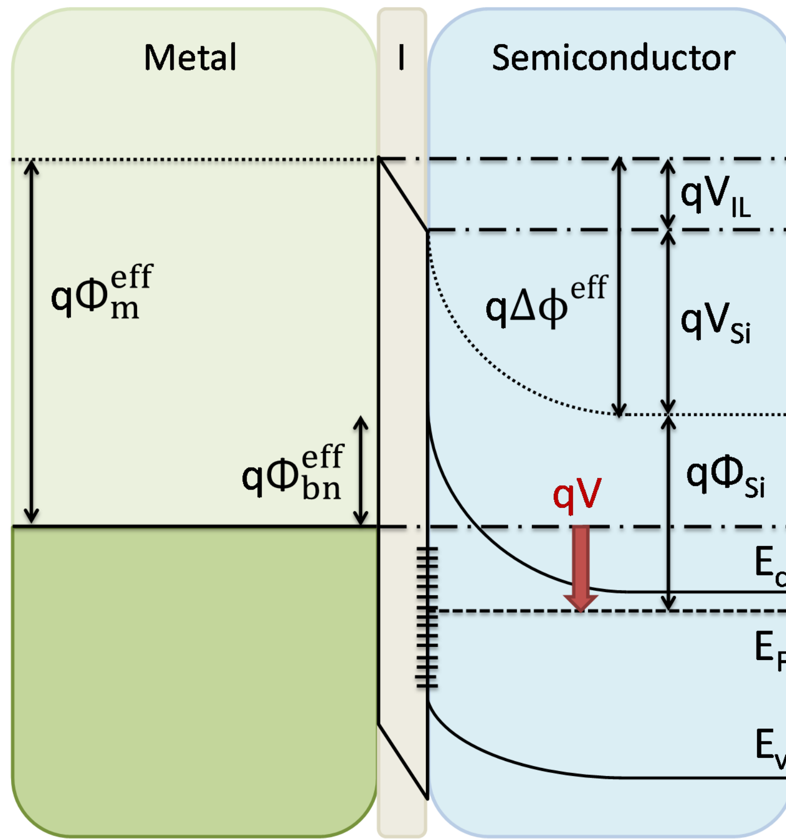


Figure II-9: Band diagram showing the different physical quantities used in the voltage sharing module.

As one can see from this figure:

$$\Delta\phi^{eff}(V) = \phi_m^{eff} - \phi_{Si} - V = V_{Si} + V_{IL} \quad \text{(II-18)}$$

Nevertheless, solving the voltage sharing of Equation (II-18) is not straightforward. Indeed, the part of the applied bias which drops in the Si causes the occurrence of a charge at the IL/S interface which in turn establishes a voltage drop within the interlayer. Therefore, V_{Si} and V_{IL} are linked by the system of Equations (II-19).

$$\begin{cases} V_{Si} = \Delta\phi^{eff}(V) - V_{IL} \\ V_{IL} = \dfrac{t_{IL}}{\varepsilon_{IL}} Q_{Si} \\ Q_{Si} = F(V_{Si}) \end{cases} \quad \text{(II-19)}$$

The surface charge Q_{Si} can be obtained by solving Poisson's equation [*Sze_1981*] and appears to be related to the voltage drop in Si via the *F* function presented in Equation (II-20).

$$F(V_{Si}) = \frac{\sqrt{2}\varepsilon_{IL} kT}{qL_{Debye}} \sqrt{\frac{{n_i}^2}{{N_d}^2}\left[e^{\frac{q(V_{Si})}{kT}} - \frac{q(V_{Si})}{kT} - 1\right] + \left[e^{-\frac{q(V_{Si})}{kT}} + \frac{q(V_{Si})}{kT} - 1\right]} \quad \text{(II-20)}$$

where L_{Debye} is the Debye length, n_i is the intrinsic carrier concentration and N_d is the doping concentration. The typical charge versus Si bias is plotted in Figure II-10 (a).

The problem represented by the system of Equations (II-19) is self-consistent and can be solved using a proper simulation module. Solving the voltage sharing gives the actual voltage drop in the dielectric layer, the surface charge density in Si and finally the resulting surface potential in Si. An illustration of such a voltage sharing is given in Figure II-10 (b) in the case of an Al_2O_3 insertion.

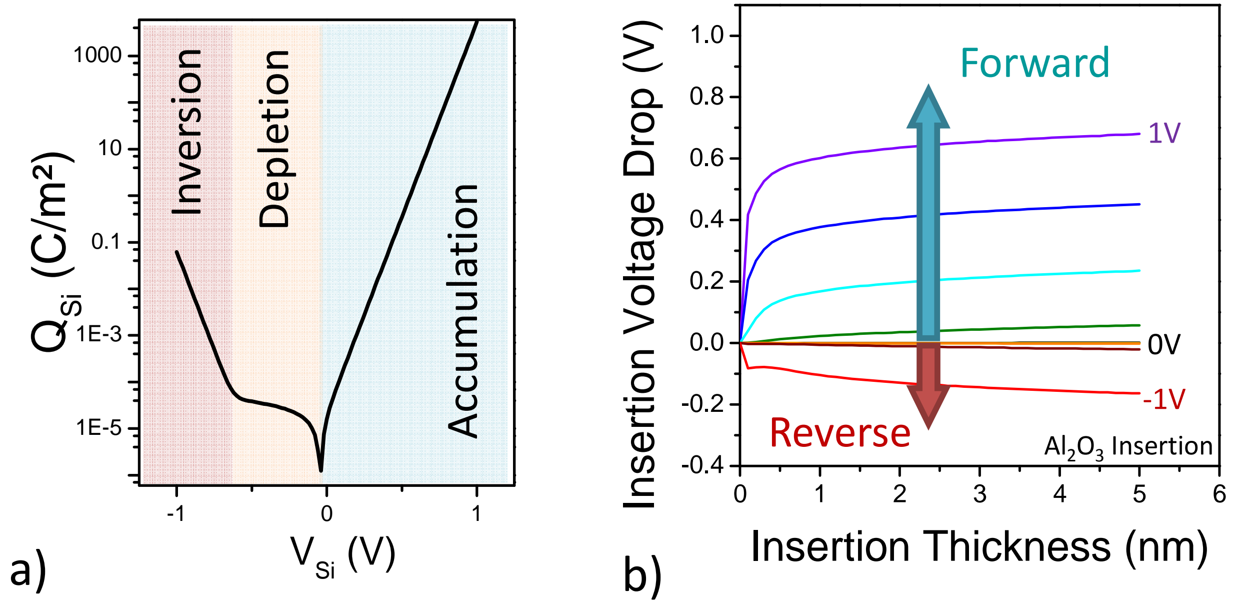


Figure II-10: (a) Evolution of the charge at the surface of the semiconductor as a function of its surface potential and (b) resulting insertion voltage drop as a function of the insertion thickness in the case of Al_2O_3. In these figures, the bias is applied on the metal and the ground on the semiconductor.

As one can see in Figure II-10 (a), the dependency of the semiconductor surface charge upon the bias is strongly asymmetrical. The surface charge in the forward regime is several order of magnitude higher than that of the reverse regime if considering a similar magnitude of bias. Being directly linked to this surface charge, the bias drop occurring in the insertion is dramatically different when biasing the contact in forward or in reverse as shown in Figure II-10 (b) in the case of Al_2O_3.

II.1.3 J-V characteristics generation

The two previous sections explained how to calculate the Fermi level pinning at MS and MIS interfaces, and thus led to evaluating the effective SBH as a function of the insertion layer nature and thickness. Adding a module to include the image force, all the needed inputs to generate the 1-D band-edge profile of the contact as a function of the applied contact bias, the dielectric thickness and the doping concentration in the semiconductor are known.

Combining this generated 1-D band structure of the contact with theories of interface transport, it is possible to evaluate the current across MS and MIS contacts. These theories are presented in the following.

II.1.3.a Main transport theories at MS interfaces

As succinctly mentioned in Chapter I, several mechanisms are traditionally considered at a metal/semiconductor interface:

- **Thermionic Emission (TE)**, the carriers are emitted above the Schottky barrier. This mechanism mainly occurs in moderately doped semiconductors (under 10^{18} at.cm^{-3}).
- **Field and Thermionic-Field Emission (resp. FE and TFE)**, the carriers are emitted through the barrier. These mechanisms more specifically occur in highly doped semiconductors (degenerate). While FE is a pure tunneling process, TFE is tunneling of thermally excited carriers which thus see a thinner barrier than in the case of pure FE.

The decomposition of the interfacial current into the three contributions listed before is represented in Figure II-11 for both the forward and the reverse regimes in the case of a degenerated n-type semiconductor.

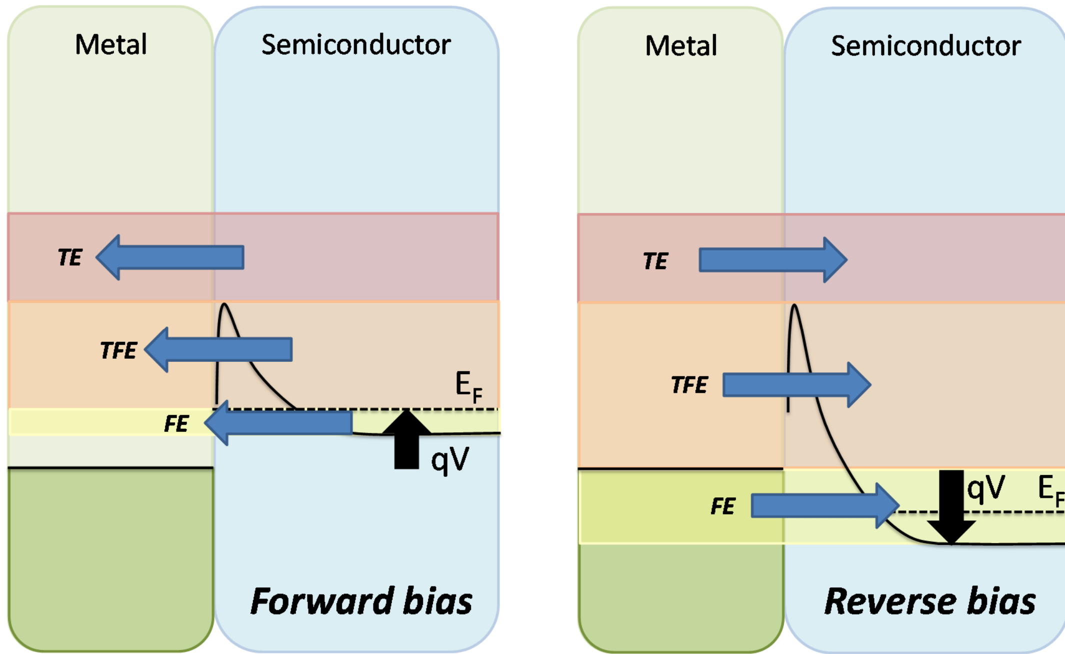


Figure II-11: Contribution of the three main mechanisms to the interfacial current under forward and reverse bias.

❖ Thermionic Emission

This model was one of the first theory used to analytically describe the emission occurring at the metal/semiconductor interface. Presented by Bethe [*Bethe_1942*], it is supposed that the carriers are emitted above the barrier and that a negligible amount of tunneling occurs through this barrier. This model relies on several assumptions:

- The SBH is much larger than *kT/q* i.e. 26 meV at 300K.
- The net current is the sum of the current flowing from the metal to the semiconductor and the one flowing from the semiconductor to the metal.
- There is no collision between electrons nor reflection at the interface.

The current density flowing from the semiconductor to the metal results from integrating the concentration of electron having energy larger than the top of the barrier and moving towards the barrier as in Equation (II-21).

$$J(V) = \int_{Ec+\Phi_{bn}^{eff}}^{+\infty} q v_x g_c(E)\, F(E) dE \qquad \text{(II-21)}$$

where v_x is the velocity of the carriers, $g_c(E)$ is the density of states and *F(E)* is the Fermi Dirac distribution. Assuming a parabolic distribution in the conduction band, solving this integral in the

direction "semiconductor towards metal" gives the corresponding current noted as $J_{S\to M}(V)$ and given by Equation (II-22) (a full description of the demonstration can be found in *[Sze_1981]*).

$$J_{S\to M}(V) = A^* T^2 \exp\left(-\frac{q\Phi_{bn}^{eff}}{kT}\right) \exp\left(\frac{qV}{kT}\right) \quad \text{(II-22)}$$

In this equation, A^* is called the Richardson constant for thermionic emission and is defined by Equation (II-23).

$$A^* = \frac{4\pi m^* k^2}{h^3} \quad \text{(II-23)}$$

where m^* is the electron effective mass in the semiconductor.

One can see in Equation (II-22) that the density of thermionic current depends exponentially on the difference between the applied bias and the effective barrier. When the magnitude of the bias is lower than that of the barrier, the semiconductor still presents a depletion zone and almost no current crosses the interface. However when the applied bias allows to reach the flat band or the accumulation regime, the barrier which was on the path disappears and the current increases exponentially.

A similar expression can be found for the current flowing from the metal to the semiconductor and is presented in Equation (II-24). Nevertheless, in this direction the barrier height seen by the carriers remains the same and does not depend from the bias applied to the contact. Therefore the current is constant as shown in Equation (II-24).

$$J_{M\to S}(V) = -A^* T^2\, exp\left(-\frac{q\Phi_{bn}^{eff}}{kT}\right) \quad \text{(II-24)}$$

Finally by applying the assumption that the total current is the sum of the two contributions, one can obtain Equation (II-25).

$$J_n(V) = \left[A^* T^2\, exp\left(-\frac{q\Phi_{bn}^{eff}}{kT}\right)\right].\left[exp\left(\frac{qV}{kT}\right) - 1\right] \quad \text{(II-25)}$$

At the time it was proposed, this model was very attractive to address the contact resistivity issue. The major considered parameter was the Schottky barrier and its link with the resistivity was straightforwardly obtained by deriving the current around zero with respect to the bias.

However, experimental data have shown to present excess currents compared to the ones predicted by this model, and especially for degenerate semiconductors [*Padovani_1966*]. Thus new models of interface barrier crossing have to be considered.

❖ Thermionic-Field and Field Emissions

As a matter of fact, the J-V characteristics obtained experimentally do not present a constant ultra-low reverse current as predicted by the thermionic emission. According to Padovani and Stratton [*Padovani_1966*], when considering highly doped semiconductors the barrier is thin enough for the carrier to tunnel through it.

In order to take into account this additional contribution, the notion of tunnelling or transmission probability *TR(E)* is introduced. Keeping the Richardson constant convention, this probability can be used to calculate the tunnelling current density as in Equations (II-26) and (II-27).

$$J_{S\to M}(V) = \frac{A^*T^2}{kT} \int_{E_c}^{Ec+\Phi_{bn}^{eff}} f_S(E,V).TR(E,V).[1 - f_M(E,V)]dE \qquad \text{(II-26)}$$

$$J_{M\to S}(V) = \frac{A^*T^2}{kT} \int_{E_c}^{Ec+\Phi_{bn}^{eff}} f_M(E,V).TR(E,V).[1 - f_S(E,V)]dE \qquad \text{(II-27)}$$

One can see from Equation (II-26) that the current density from the semiconductor to the metal can be obtained by multiplying the tunneling probability *TR(E,V)* across the barrier by the occupation probability in the semiconductor $f_S(E,V)$ and the vacancy probability in the metal $[1 - f_M(E,V)]$, and summing on the relevant energy interval.

Similarly the current density from the metal to the semiconductor can be obtained with the same calculation but swapping the occupation and vacancy probabilities as shown in Equation (II-27).

The full demonstration of this calculation and the resulting expression for currents across the MS interface when considering the Tunneling-Field and Field Emissions can be found in [*Padovani_1966*].

❖ Characteristic energy E_{00}

These three mechanisms are co-existing and correspond to a specific range of energy. Depending on the doping and the temperature, the apportionment of the magnitude of these mechanisms varies. The characteristic energy E_{00} representative of this repartition is given in Equation (II-28).

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_d}{m_T^* \varepsilon_s}} \quad \text{(II-28)}$$

where m_T^* is the tunnelling effective mass of the majority carriers, ħ is the reduced Planck constant and N_d the doping concentration. According to Padovani and Stratton [*Padovani_1966*], a rough criterion to discriminate the dominant transport mechanism consists in comparing E_{00} with kT.

- If $E_{00} << kT$, the TE regime is dominant
- If $E_{00} \approx kT$, the TFE regime is dominant
- If $E_{00} >> kT$, the FE regime is dominant

II.1.3.b Interfacial layer tunneling

As evoked before, inserting an interlayer dielectric generates a modification of the band edge diagram since it induces i) a FLP mitigation and ii) a voltage drop sharing between the semiconductor and the dielectric.

Additionally the interlayer also generates an extra tunnel barrier that the carriers have to cross. Thus in order to simulate transport in MIS structures, a simple model was proposed in 1967 [*Schewchun_1967*]. This model consists in modulating the current crossing the barrier found using the previous models by a transmission probability. This transmission is mathematically expressed as an exponential decay of the current as a function of the dielectric thickness as shown in Equation (II-29).

$$T(\delta) = exp(-\sqrt{\zeta}\delta) \quad \text{(II-29)}$$

ζ is given in m^{-2} and represents the barrier induced by the insertion (defined in Chapter I as CBO for electrons and VBO for holes) and δ is the dielectric thickness in Å.

Then if noting $J_{w/o\ ins}$ the current without insertion and J_{ins} the current with the insertion one can obtain Equation (II-33).

$$J_{ins}(V) = J_{w/o\ ins}(V)\ exp(-\sqrt{\zeta}\delta) \quad \text{(II-30)}$$

II.1.3.c Limitations of the main transport theories

The previous models used to describe the different transport mechanisms lean on extensive approximations in order to be easily implemented with a very low computation time. Nevertheless, some of these approximations seem not compatible with the system we tried to simulate:

- **The criterion E_{00} less or greater than kT does not take into account the bias applied on the contact.** Thus, the apportionment of the different mechanisms of conduction is only meaningful at zero bias.
- **The mathematical approximations for thermionic emission are made for high barrier compared to kT** while we tried to obtain very low barrier contact. Moreover, it seems that this restriction is not straightforward since the current taking place above the barrier would reasonably by a major contribution in the case of an ultra-low barrier.
- **Only the height and the width of the barrier are taken into account** but never its shape while the actual energy band diagram presents a polynomial bending.
- **The barrier in the insertion is taken into account in Equation (II-29) by the given value ζ.** However under biasing, the barrier of energy does not stay rectangular but features a triangular shape. Thus, its actual barrier is not constant along the direction perpendicular to the interface.
- **Due to the barrier lowering, the rough criterion consisting in comparing E_{00} with kT seems not to work properly for degenerate semiconductors**. Indeed, according to Equation (II-28), increasing the doping concentration tends to an E_{00} increase and thus should lead to the predominance of the Field Emission. Nevertheless, due to the image force lowering, the effective SBH cannot be considered as a constant value. Since its value is lowered as the doping concentration increases, the contribution of the Thermionic Emission also increases [*Hutin_2010*].

II.1.3.d Wentzel-Kramers-Brillouin approximation (T_{WKB})

Therefore, a T_{WKB} approach was considered in order to be as precise as possible even if suffering from a very high computation time. To do so, Equations (II-26) and (II-27) were considered but the tunneling probability $TR(E,V)$ was not simplified depending on the transport mechanism but calculated using the T_{WKB} approximation. Named after Wentzel, Kramers and Brillouin, this method consists in considering a tunneling probability according to Equation (II-31).

$$TR(E,V) = exp\left[-2\int_{x1(E,V)}^{x2(E,V)}\sqrt{\frac{2m^*}{\hbar^2}(E_c(x,V)-E)dx}\right] \quad \text{(II-31)}$$

x1 and *x2* are the turning points and correspond for each given energy to the boundaries between which tunneling occurs. An illustration of these points is given in Figure II-12. One can see in this figure that a carrier evolving at a given energy *E*, encounters at each *x* between *x1* and *x2* a potential barrier with a height of $E_c(x,V) - E$. Then the total barrier for each energy is obtained by integrating the elementary height between the two turning points.

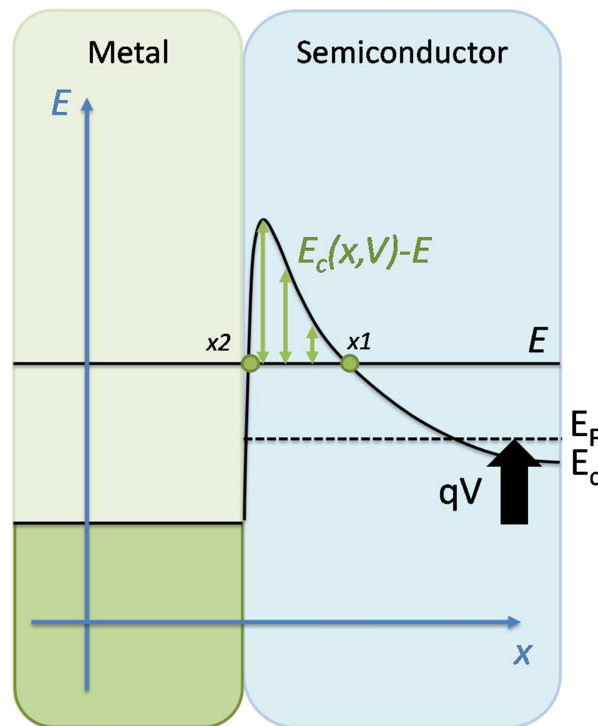


Figure II-12: Illustration of the notion of turning points for an N-type semiconductor.

Equation (II-31) can be applied to all the barriers carriers encounter. Thus for a given energy, they could have to cross the dielectric and/or the depletion region. These two cases have been treated separately by splitting the total transparency in two spatial domains corresponding to each material and by considering proper tunneling masses m_* leading to Equations (II-32) and (II-33) [*Sze_1981*]. The resulting transparency is given by the product of the tunneling probabilities as shown in Equation (II-34) and illustrated in Figure II-13.

$$T_{WKB}^{IL}(E,V) = \begin{cases} e^{-2\int_{IL}\sqrt{\frac{2m_*^{IL}\,(E_C^{IL}(V,x)-E)}{\hbar^2}}dx} & ,if\ E < E_C^{IL}(V,x) \\ 1 & ,if\ E \geqslant E_C^{IL}(V,x) \end{cases} \quad \text{(II-32)}$$

$$T_{WKB}^{Si}(E,V) = \begin{cases} e^{-2\int_{IL}\sqrt{\frac{2m_*^{Si}\,(E_C^{IL}(V,x)-E)}{\hbar^2}}dx} & ,if\ E < E_C^{Si}(V,x) \\ 1 & ,if\ E \geqslant E_C^{Si}(V,x) \end{cases} \quad \text{(II-33)}$$

$$T_{WKB}^{Tot}(E,V) = T_{WKB}^{IL}(E,V) \times T_{WKB}^{Si}(E,V) \quad \text{(II-34)}$$

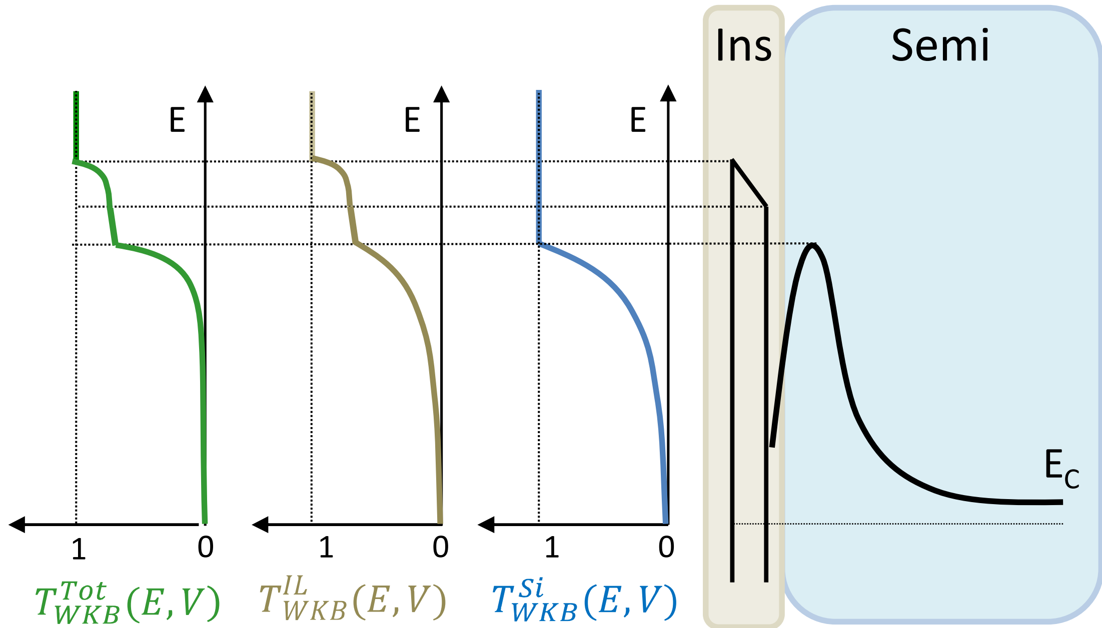


Figure II-13: Schematic of the tunneling probabilities of each domain and the resulting total one.

II.1.3.e J-V Characteristics calculation

Combining Equations (II-26), (II-27) and the T_{WKB} approximation leads to Equation (II-35) which allows a calculation of the current density as a function of the applied bias.

$$J(V) = \frac{A^*T}{k}\int_{-\infty}^{+\infty} T_{WKB}^{Tot}(E,V)(f_{Si}(E,V) - f_{Met}(E,V))dE \quad \text{(II-35)}$$

Therefore the goal of this algorithm is to generate J-V characteristics as a function of the contact parameters such as the doping concentration, the dielectric insertion thickness and nature and the metallization. In order to link the generated electric transport characteristics, the contact resistivity can be obtained using Equation (II-36).

$$\rho_c(V) = \left\{\frac{dJ(V)}{dV}\right\}^{-1} \quad \text{(II-36)}$$

It is worth noting that this value is not *a priori* considered constant since depending on the inputs the resulting contact can be found non-linear and thus its resistivity would be a function of the bias.

In order to evaluate the relevance of our simulations, the contact resistivity of silicon-based insertion-free contact was evaluated as a function of the substrate doping concentration and the effective metal workfunction. The results are plotted in Figure II-14 along with experimental measurements of a PtSi/n-Si contact taken from [*Stavitsky_2008*].

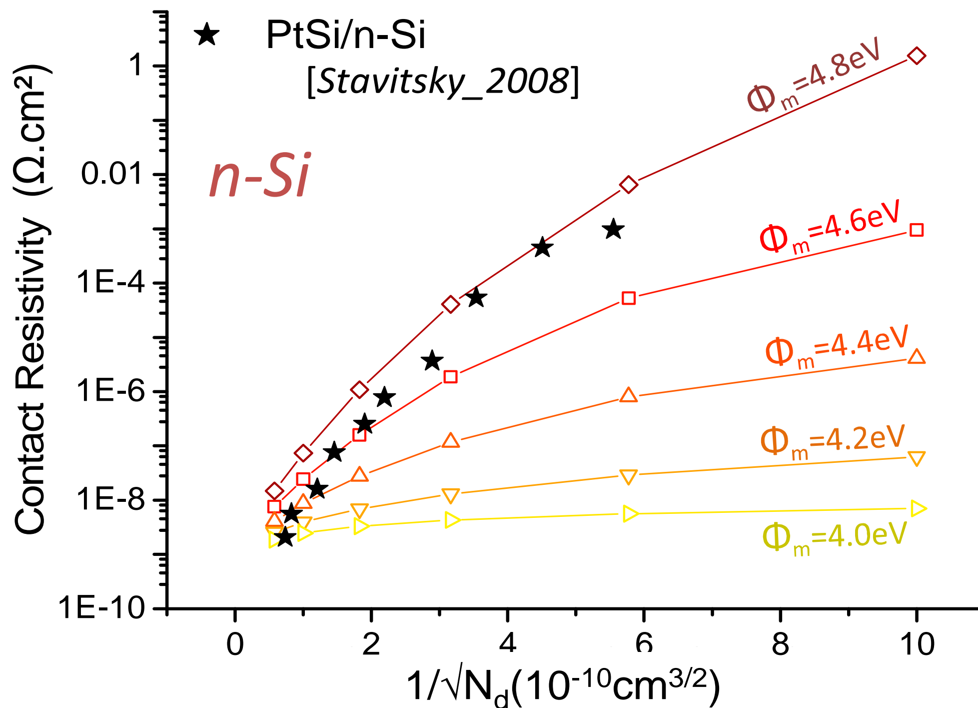


Figure II-14: Contact resistivity to n-Si as a function of the doping concentration for (colored) simulated system presenting various metal work functions for an extraction bias of 1V; and (black stars) experimental PtSi/n-Si system [Stavitsky_2008].

The PtSi metal workfunction varying between 4.8 and 5.1 eV depending on the fabrication process conditions [*Niranjan_2006*], simulated results seem consistent with the experimental values.

II.2 Stand-alone contact J-V characteristics

Following the algorithm of Figure II-1 and implementing all the calculations presented in the previous section allow to generate MS and MIS contacts current density as a function of the doping concentration of the substrate, the dielectric nature, the dielectric thickness and the metallization.

II.2.1 Zero-barrier contact case

The ideal case of zero barrier contact without insertion was first simulated using the algorithm. The doping concentration was considered equal to 10^{20} at.cm^{-3}, the ideal metal work function was set to match the conduction band of Si and the slope parameter S was set to 1 (no FLP). The results obtained for a forward biasing are presented in Figure II-15.

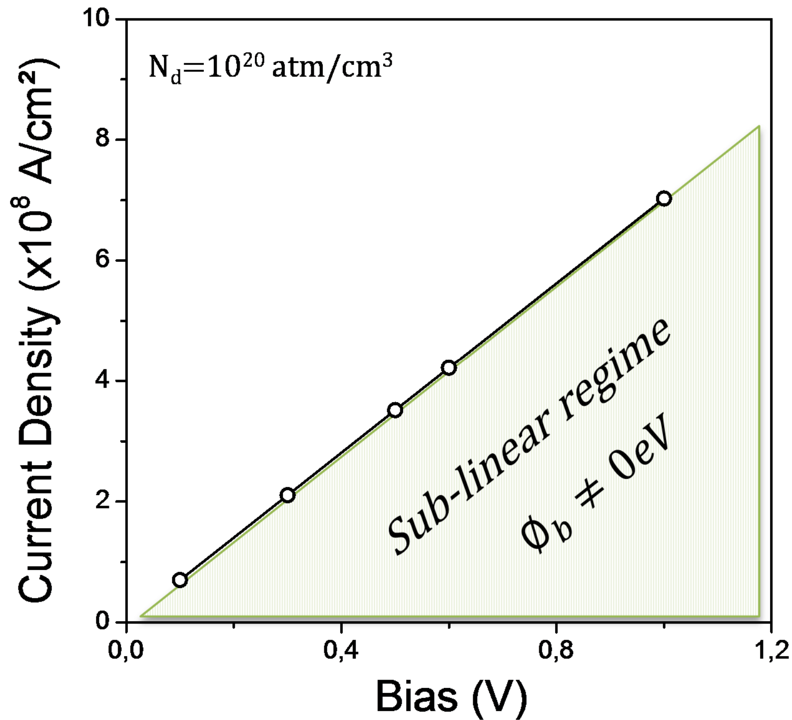


Figure II-15: Forward current density as a function of the bias voltage for an unpinned metal based contact without any insertion.

As expected for a zero-barrier contact the resulting current density versus bias characteristic is linear. By taking the inverse of the slope one can access the contact resistivity. In this case, the value was found to be equal to 1.42 x 10^{-9} Ω.cm².

As shown in Equation (II-36), the same value can be found by simplifying the supply function difference by a rectangular function equal to 1 between the Fermi level of the metal and that of Si and equal to zero otherwise; and by assuming a $T_{WKB}(E,V)$ value of 1 due to the lack of barrier.

$$J(V) = \frac{A^{*}T}{k}\int_{-\infty}^{+\infty} T_{WKB}^{Tot}(E,V)\big(f_{Si}(E,V) - f_{Met}(E,V)\big)dE$$

$$\text{If } \Phi_{bn}^{eff} = 0 \Rightarrow T_{WKB}^{Tot}(E,V) = 1 \qquad \text{(II-37)}$$

$$\Rightarrow J(V) = \frac{A^{*}T}{qk} \times V$$

$$\Rightarrow \rho_c(V) = \left\{\frac{dJ(V)}{dV}\right\}^{-1} = \frac{qk}{A^{*}T} = 1.42 \times 10^{-9}\ \Omega.cm^2$$

This contact resistivity corresponding to a zero-barrier contact can be considered as the ultimate achievable limit for a real contact between a metal and a semiconductor. Therefore, using this simplified model, the ITRS targeted value of ρ_c equal to 10^{-9} Ω.cm² appears to be the fundamental limit value of the contact resistivity scaling for silicon material.

However, it has to be noted that using full band ballistic quantum transport approach, the intrinsic lower limit of contact resistivity with 10^{20} at.cm^{-3} doped n-Si was actually found to be around 2 x 10^{-10} Ω.cm² [*Maassen_2013*].

II.2.2 MIS contacts simulations

Aiming at finding realistic solutions in an industrial clean room environment, standard dielectric insertions (Al_2O_3, Si_3N_4 and TiO_2) and capping metallizations (Zr, Ti and Pt) were considered. The main parameters of these materials used for the simulations are presented in Table II-1 (partially found in [Gupta_2013]).

Table II-1: Main parameters used in current simulations for common materials [Gupta_2013].

Dielectric	Band gap E_g (eV)	Relative permittivity ε_{IL}	Relative mass m^*	Conduction band offset $\Delta E_c/Si$ (eV)	Valence band offset $\Delta E_v/Si$ (eV)
SiO_2	9	3.9	0.3	3.5	4.4
Al_2O_3	8.8	9	0.2	2.8	4.9
Si_3N_4	5.3	7	0.2	1.9	1.8
TiO_2	3.05	80	0.3	-0.06	2.01

Metal	Ideal workfunction (eV)
Zr	4
Ti	4.33
Pt	5

II.2.2.a Doping concentration impact

A first simulation study was dedicated to evaluate the influence of the substrate doping concentration on the properties of a given M, I and S combination. The I-V calculation algorithm was applied for a Ti/TiO_2/Si contact. The insertion thickness was varied between 0 and 10 Å and the n-Si doping concentrations of N_d=10^{18}, 10^{19}, and 10^{20} at.cm^{-3} were considered.

The current amplification factor as defined in Equation (II-38) was calculated as a function of the dielectric thickness, considering the three doping concentrations and a bias of -0.1 eV. The results are plotted in Figure II-16.

$$Current\ Amplification\ Factor(t_{TiO_2}) = \frac{Current\ of\ Ti/TiO_2(t_{TiO_2})/Si\ contact}{Current\ of\ Ti/Si\ contact} \quad \text{(II-38)}$$

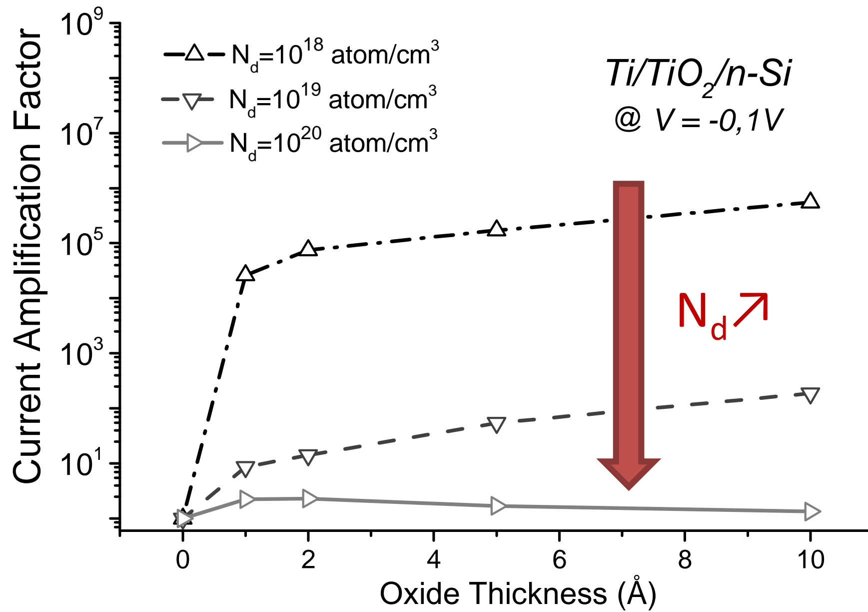


Figure II-16: Current amplification factor at -0.1V versus the insertion-free case as a function of the TiO_2 interlayer thickness for various dopant concentrations.

It appears that while the current is multiplied by a factor of 10^6 when inserting a 1 nm thick TiO_2 layer between the Ti metallization and a 10^{18} at.cm^{-3} n-doped Si, the amplification factor drops down to unity on a 10^{20} at.cm^{-3} doped Si.

This significant degradation of the current amplification factor is mainly due to the difference of transport mechanisms occurring at the interface between a lowly doped Si based contact and a highly doped one.

- At low doping concentration, the space charge region extends on a significant width and the carrier emission in the reverse forward is nearly purely thermionic. Thus the initial resistance (without insertion) is prominent and considering this model of emission, it is exponentially related to the barrier height (please refer to the Equation (II-25)). Consequently, the tunnelling resistance induced as the dielectric thickness increases is of the same order of magnitude of the initial interfacial resistance, and even a slight modification of the SBH can result in a large reverse-bias current enhancement.
- On the contrary, at high doping concentration, the interface barrier is extremely thin and the electric transport is a mix between FE, TFE and TE mechanisms. The initial interface resistance is low compared to that of the previous case. Thus reducing the SBH has less impact on the

interface resistance and the tunnelling resistance induced by the dielectric is no longer compensated. The expected current gain is then more modest.

These considerations are summarized in Figure II-17.

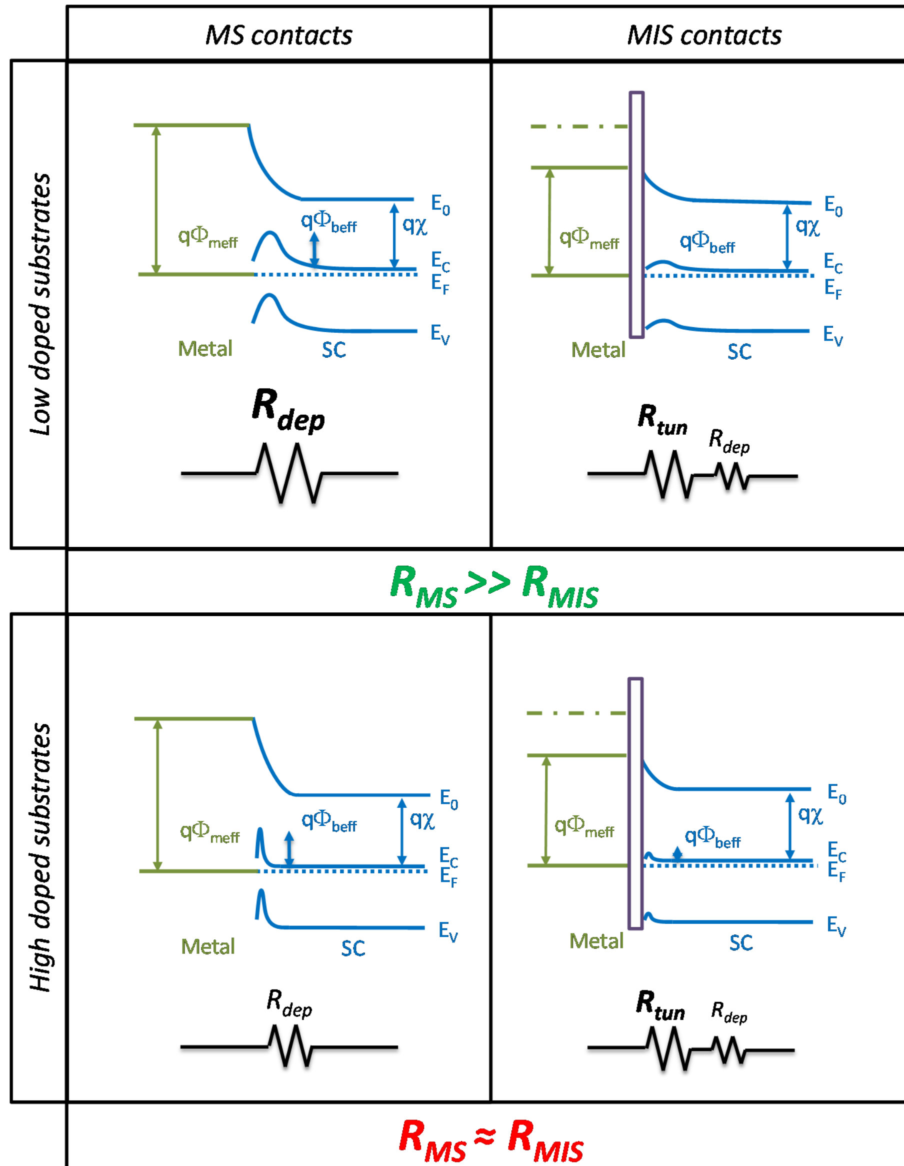


Figure II-17: Schematics aiming at explaining the dependency of the insertion efficacy as a function of the substrate doping concentration

This notion is of prime importance since it means that some results of the state-of-the art showing massive gains due to the use of MIS contacts on low doped substrates cannot be transposed straightforwardly on a high doping substrates. As an illustration, FLP mitigation at the Al/n-GaSb was carried out by introducing Al_2O_3 and TiO_2 insertions in [*Yuan_2011*]. The substrate being lightly doped

with a carrier concentration of ~10^{17} at.cm^{-3}, the current of the contact was amplified by a factor of 10^4 when inserting a TiO_2 layer. As spectacular as this improvement may seem, contacts for advanced CMOS devices will realistically be made on degenerately doped source and drain in order to meet the industrial requirements. In other words, MIS contacts in such devices lead to a lower enhancement.

II.2.2.b Dielectric thickness optima

Simulations were then performed at doping concentrations of 10^{20} at.cm^{-3} for both n- and p-type Si in order to be representative of industrial devices. Since MIS contacts are believed to be an alternative to ultra-high implantation, no higher doping concentration was considered.

The usual barrier deposited prior to metallization being TiN/Ti [*Kamgar_1989*], J-V plots were generated for Ti/Si interfaces as presented in Figure II-18 (a) and (b). The reference cases of perfectly linear ohmic contacts with $\rho_c=10^{-7}$ Ω.cm², $\rho_c=10^{-8}$ Ω.cm² and $\rho_c=10^{-9}$ Ω.cm² are also plotted along in these figures in shades of grey.

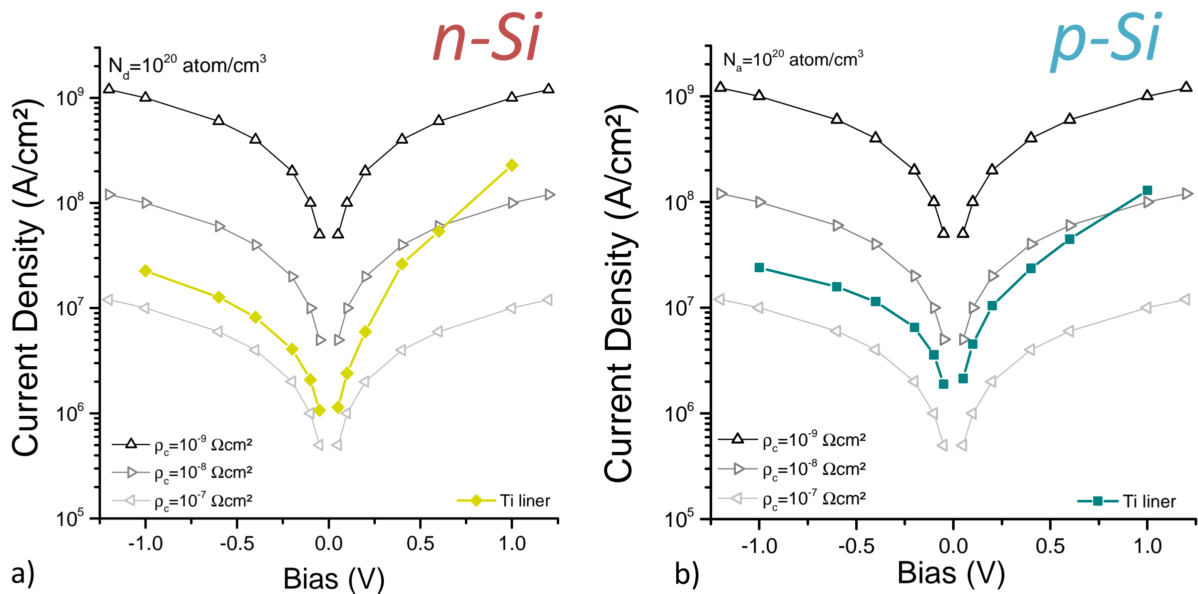


Figure II-18: J-V characteristics of Ti liner contact on (a) n-Si and (b) p-Si compared with ohmic references of $\rho_c=10^{-7}$, $\rho_c=10^{-8}$ and $\rho_c=10^{-9}$ Ω.cm². The workfunction of Ti is considered equal to 4.33 eV and no intermixing with Si is assumed for the simulations.

One can notice that the Ti liner contacts are slightly better on p-type Si due to the FLP being closer to the valence band (Figure I-18). If compared with the reference linear contacts, the Ti metallization appears to have performance slightly above $\rho_c=10^{-7}$ Ω.cm² case in the reverse regime and closer to $\rho_c=10^{-8}$ Ω.cm² one in forward.

As presented in Chapter I and particularity in the Table I-2, Al_2O_3 and TiO_2 have been intensively investigated so far in the state-of the-art. As reported in Table II-1, these dielectrics have highly different parameters. Thus, trying to quantify the impact of the dielectric properties on the transport, simulations were run for those insertions. For simulations, the thickness of the dielectrics were taken equals to 3, 5 and 10 Å and the top electrode was kept in Ti. The results are presented in Figure II-19.

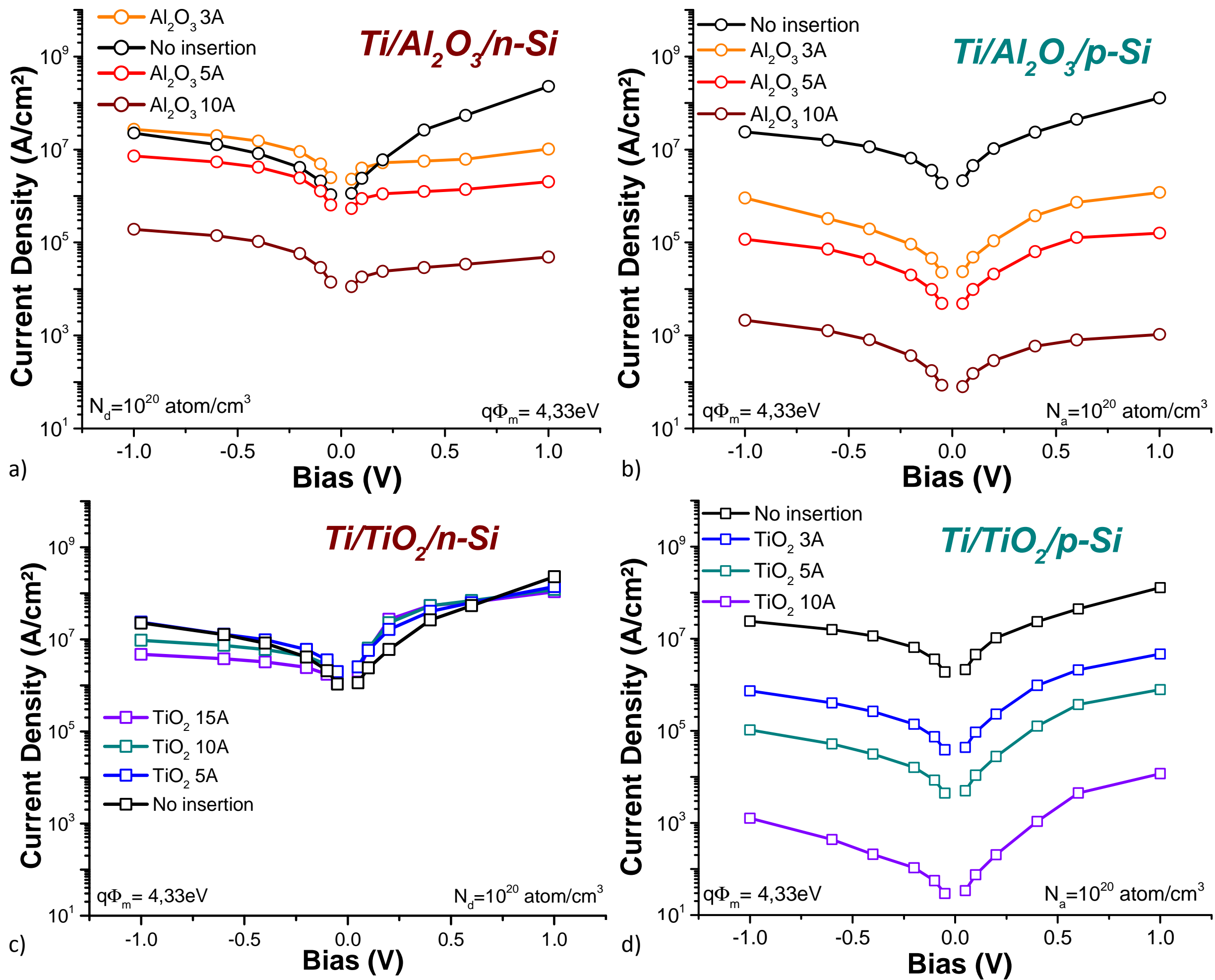


Figure II-19: J-V characteristics of Ti-contacts on (a) Al_2O_3/n-Si, (b) Al_2O_3/p-Si, (c) TiO_2/n-Si and (d) TiO_2/p-Si stacks.

It appears that inserting an Al_2O_3 layer strongly degrades the current density on both n- and p-Si (Figure II-19 (a) and (b)). However, the degradation of the current at a given thickness and bias is higher on p-Si than on n-Si and even a slight enhancement can be observed for the n-type case if keeping an insertion as thin as 3Å. While the current on p-Si is also degraded using TiO_2 insertions, a slight improvement is observed around 0 V on n-Si for a thickness insertion of 5 Å. In Figure II-19 (c), due to

this absence of dramatic degradation, the thickness of TiO_2 was increased above the 10 Å limit set for the other configurations.

These results come from two main origins. First, the dissimilarity between the VBO and CBO of both TiO_2 and Al_2O_3 (Table II-1) participate to the different observed behaviors. Considering basically that the T_{WKB} approximation leads to an exponential variation of the tunnelling barrier opacity as a function of its height, even a small difference in the inputs can lead to a considerable change in the outputs. The VBO and CBO of the Al_2O_3 being respectively equal to 4.9 and 2.8 eV explain the observed degradation of the current density. Similarly, due to the parameters of TiO_2 (VBO of 2.01 eV and CBO of -0.06 eV), only improvement on n-Si is observed.

Secondly, the MIS approach leads to a FLP reduction. Then, as the thickness of the dielectric is increased, the effective work function of the metal tends toward its ideal workfunction. Here, the considered metallization being Ti, an n-type metal, the FLP mitigation leads to the lessening of the effective work function and then to a degradation of the contacts made on p-type.

In order to find an optimal configuration of contact on p-type substrates, the Ti metallization was replaced by Pt due to its appropriate workfunction of 5 eV [*Niranjan_2006*]. Based on this value this metal is considered as p-type and should lead to a SBH reduction on p-Si as the FLP is reduced. The cases of TiO_2 and Si_3N_4 insertions were simulated, the former to keep the same dielectric as the one used on n-Si, the latter to reduce slightly the VBO (1.8 eV instead of 2.01 eV). The results are respectively presented in Figure II-20 (a) and (b).

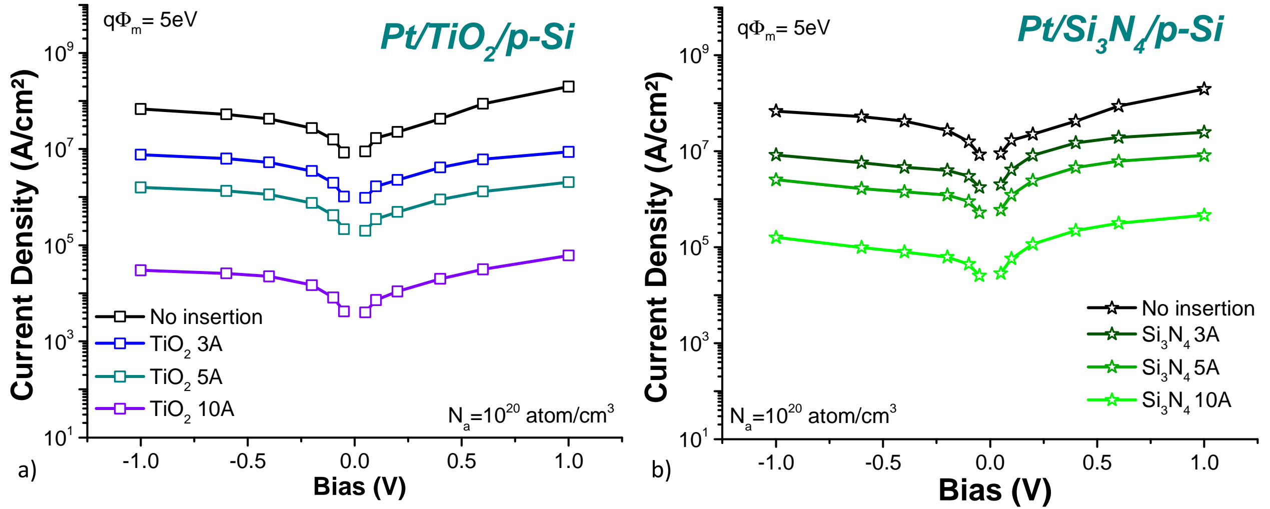


Figure II-20: J-V characteristics of Pt-contacts on p-Si presenting (a) TiO_2 and (b) Si_3N_4 insertions.

These results show a clear degradation of the current density for both configurations whereas the metallization has been changed in order to obtain a reduction of the SBH on p-Si. This suggests that the tunnel barrier induced by the dielectric insertions has a prevailing impact on the contact electric transport compared to the SBH.

Finally, in order to fully benefit from the FLP reduction, a n-type metallization was considered on n-Si substrate, namely, Zr. Considering the results of Figure II-19 (c), TiO_2 was kept as an insertion of choice for n-Si based contacts. Results are displayed in Figure II-21.

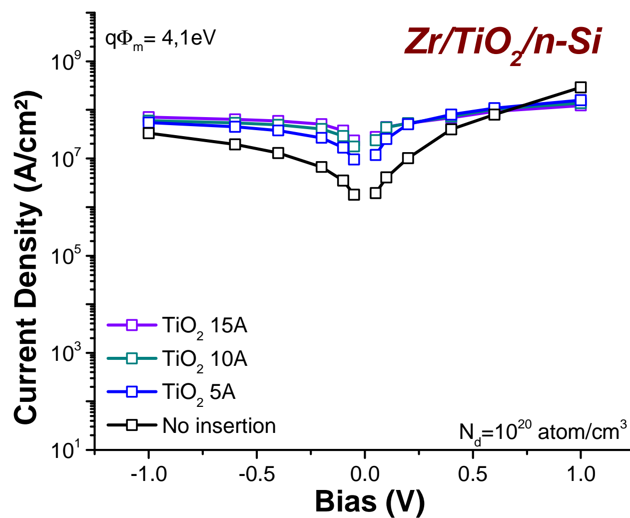


Figure II-21: J-V characteristics of Zr-contacts on n-Si presenting TiO_2 insertions.

While results of Ti/TiO_2/n-Si contacts just feature a slight increase of the current density for a TiO_2 insertion below 5 Å, Zr/TiO_2/n-Si contacts present a large improvement up until 15 Å, with no further increase observed above this value. Combining a dielectric featuring an ultra-low CBO and an n-type metal, this configuration appears to be the best configuration to contact n-Si.

The optimal configurations corresponding to each combination of metal and dielectric were added to the Ti-liner reference and the ideal ohmic cases and are plotted in Figure II-22 [*Borrel_2016*].

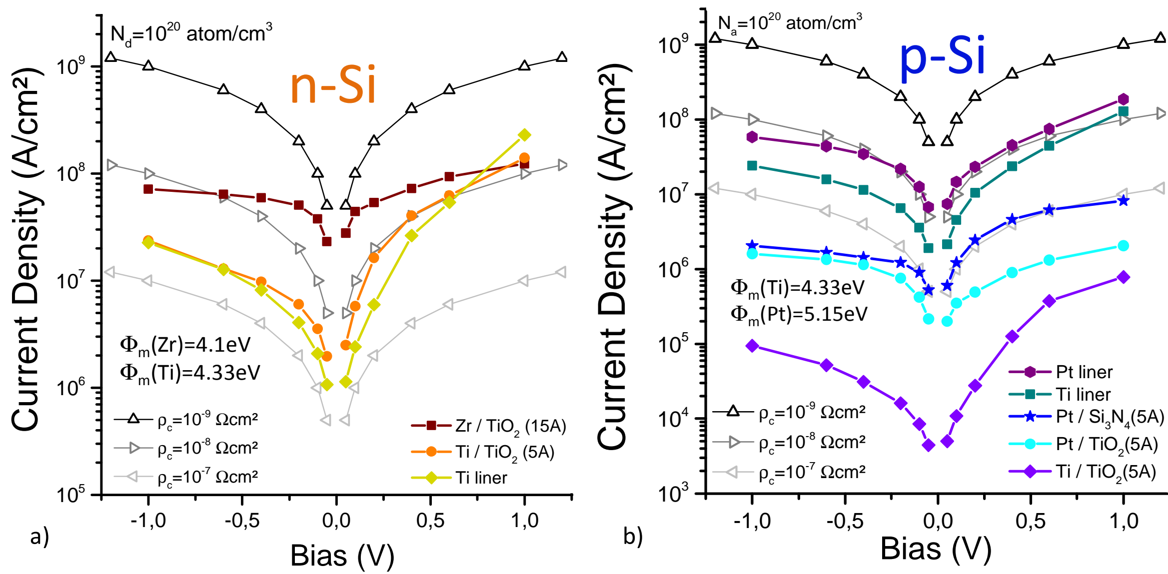


Figure II-22: J-V characteristics for (a) n-type based contacts presenting Ti and Zr metallizations with TiO_2 interlayer and (b) p-type based contacts presenting Ti and Pt metallizations with various interlayer natures and thicknesses. The scales of the two figures are different [Borrel_2016].

By looking between -1 V and 1 V, it appears that only the Zr/TiO_2/n-Si contact presents performance significantly better than the 10^{-8} Ω.cm² case but fails to reach the targeted 10^{-9} Ω.cm² one. Concerning the p-Si, no optimal insertions was found when simulating TiO_2, Si_3N_4 and Al_2O_3 dielectrics. If considering parameters found in [*Gupta_2013, Robertson_2002*] and represented in Figure II-23, it seems that the issue of contacting p-Si with a MIS approach can be extended to a lot of other dielectrics.

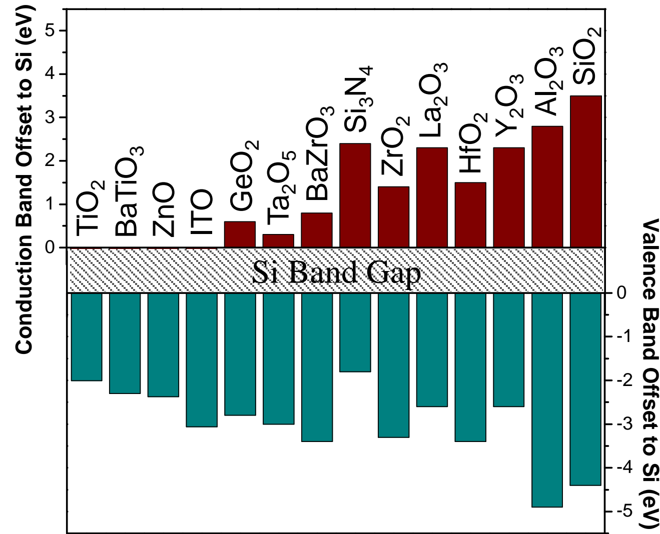


Figure II-23: Conduction and Valence Band Offsets to Si of various dielectric [Gupta_2013, Robertson_2002].

However, the current density simulated in the case of a Pt liner contact comes out to be higher than that of the Ti liner reference (Figure II-22 (b)). Despite a non-mitigated FLP, the 0.82 eV difference between Ti and Pt nominal workfunctions induces a non-negligible effective workfunctions difference between these two metallizations. The resulting effective SBH is consequently lowered, leading in turn to a significant increase in current density.

Finally, by looking at Figure II-22 (a) and (b), the optimal co-integration configuration emerging from the analytical simulations is Pt/p-Si and Zr/TiO_2(15Å)/n-Si.

II.2.2.c Dielectric induced non-linearities

It is worth noting that inserting a dielectric layer between the metal and the semiconductor not only acts on the contact conductivity but also on its symmetry. As explained in Figure II-10, when applying a positive bias to the metal, the Si being in the accumulation regime features a significant surface charge. Then considering the system of Equations (II-19) i.e. the self-consistent voltage sharing between the Si and the dielectric, this surface charge results in an extensive voltage drop in the dielectric (Figure II-10).

Consequently, the actual bias seen by the Si which is responsible for the band bending and the carrier injection is found to be only a fraction of the applied bias. Notably, the Pt/TiO_2(5Å)/p-Si contact features a forward current lower that its reverse one. To our knowledge, this can only occur in MIS contacts.

Therefore, one can notice that neither associating contact resistivities with MIS contacts nor comparing these contacts with linear references is straightforward. As a matter of fact, some contacts may appear to perform poorly at first glance on a [-1V;+1V] interval, yet feature very low resistivity at low biases.

For example, Zr/TiO_2(15Å)/n-Si contact has a conductivity close to the $\rho_c=10^{-8}$ Ω.cm² reference at +1V while it appears to be closer to the 10^{-9} Ω.cm² ideal ohmic contact around 0 V. Similarly, considering the case of a Ti/TiO_2/n-Si contact, the current amplification factor as a function of the thickness was plotted in Figure II-24 for different contact biases.

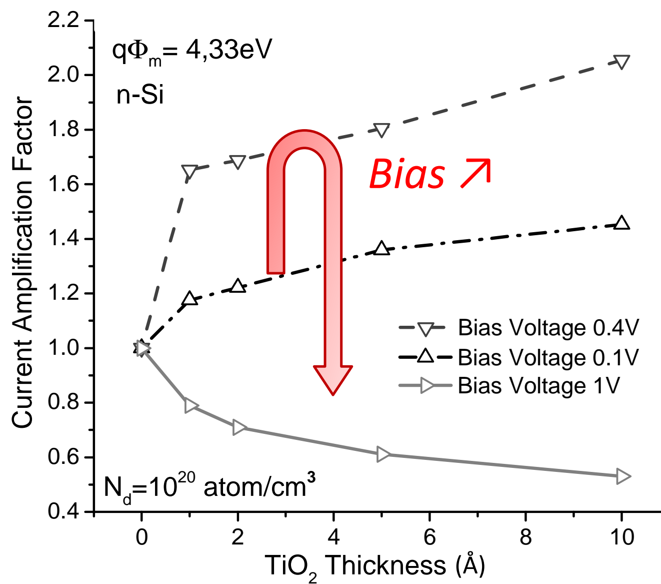


Figure II-24: Current amplification factor as a function of the TiO2 interlayer thickness at three different bias voltages.

The current amplification factor of this contact has no trivial variation with the applied bias. While an insertion of 10 Å ensures a 2 times current amplification at 0.4 V, it also makes it lower by almost a factor 2 at 1V.

For this reason, it seems that associating a given contact resistivity to such non-linear non-symmetric contacts is a sensitive problem.

II.2.3 Partial conclusions

In section II.2, using the 1-D analytical algorithm, MIS contacts J-V characteristics were generated. From analyzing the transport properties of such contacts, several main conclusions can be drawn.

Firstly, when considering a zero-barrier contact, the contact resistivity value is found around 10^{-9} Ω.cm². This case can be seen as the ultimate achievable limit for a real contact between a metal and a semiconductor due to the absence of barrier. Therefore it is legitimate to consider the ITRS targeted value of ρ_c equal to 10^{-9} Ω.cm² as the fundamental limit value of the contact resistivity scaling for silicon material. Even if more complex models (such as ab initio full band calculation [*Maassen_2013*]) found this limit slightly above 10^{-10} Ω.cm², it seems that the room for improvement when it comes to contact resistivity lowering is narrow.

Secondly, the current amplification factor induced by a dielectric insertion is found highly dependent on the doping concentration of the semiconductor. More precisely, the enhancement generated by an insertion appears significantly degraded when contacting a highly doped semiconductor. Therefore, some improvements found in the state-of-the-art may seem spectacular but are actually performed on lowly doped semiconductors. Contacts for advanced CMOS devices will however realistically be made on highly doped source and drain in order to meet the industrial requirements. In other words, MIS contacts in such devices lead to a modest enhancement.

Thirdly, the different combinations of dielectrics and capping metals used in the study point out the lack of suitable insertions to address the p-Si case (using theoretical valence band offsets). Moreover, it also appears that working in the barrier lowering paradigm, as opposed to the barrier narrowing one, implies to address n- and p-type semiconductor polarities respectively with n- and p-type capping metals. Thus, it finally comes out that the optimal configuration consists in a dual-insertions dual-metallizations scheme which is far from simple from a process flow point of view.

Finally, the MIS contacts feature non-linear non-symmetrical J-V characteristics. Therefore, when plotting MIS J-V characteristics with that of ideal ohmic references in order to compare them is not straightforward. As a matter of fact, some contacts may appear to perform poorly at first glance on a [-1V;+1V] interval, yet feature very low resistivity at low biases. For this reason, it seems that associating a given contact resistivity to such non-linear non-symmetrical contacts is a sensitive problem.

II.3 Impact on devices performance

This section addresses the impact of MIS contacts on MOSFETs in both DC and AC regimes. While the former is assessed from I_d-V_{ds} characteristics of transistors flanked by MIS junctions, the latter involves evaluating the intrinsic delay on simulated ring oscillators circuits.

II.3.1 DC impact

As stated previously, in the majority of cases the junctions J-V characteristics are neither perfectly linear nor symmetrical in a [-1V,+1V] range of bias. For this reason, the contact resistivity of such contacts cannot be considered constant and has to be extracted as the function of the bias.

Nevertheless, the extraction bias has to be been chosen as close as possible to the bias used when contacts are plugged to a transistor. Indeed, if extracting the resistivity at an arbitrary bias, e.g. 1 V, could lead to significant discrepancies between the extracted resistivity and the one effectively resulting from the operative contact biasing.

As presented in Figure II-25, the effective operative contact bias to consider arises from solving the voltage sharing between contacts and MOSFET when applying a supply voltage V_{dd} as V_{ds}.

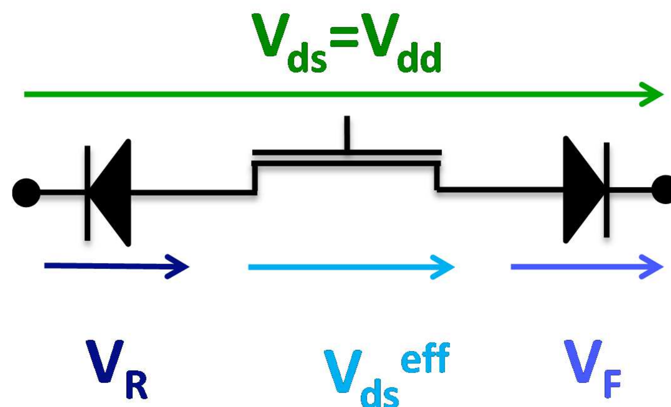


Figure II-25: Voltage sharing between the MOSFET and its contacts when applying V_{dd}. V_{ds}^{eff} is the effective supply voltage biasing the transistor block

Moreover, as illustrated in this figure the two contacts are in a back-to-back configuration meaning that while one of them is biased in the forward regime the other one is necessarily biased in the reverse regime. In the case of non-symmetrical contacts, the operative bias is thus even harder to define since each contact have a different effective bias when applying V_{dd} on the MOSFET. Therefore this

problem boils down to treating two back-to-back diodes and one resistor in series which is a self-consistent problem and can be solved using numerical simulation.

Toward this goal, compact models were built using elementary SPICE components i.e. resistors and diodes in order to reproduce the electrical behavior of all the analytically-calculated MIS diodes J-V characteristics of section II.2. The current density was converted in a current using the projected contact dimensions on active areas for future generations of 10 nm node MOSFETs i.e. 130 nm by 30 nm. As an example the SPICE compact model fit performed for the Ti/TiO_2(5Å)/n-Si is presented in Figure II-26.

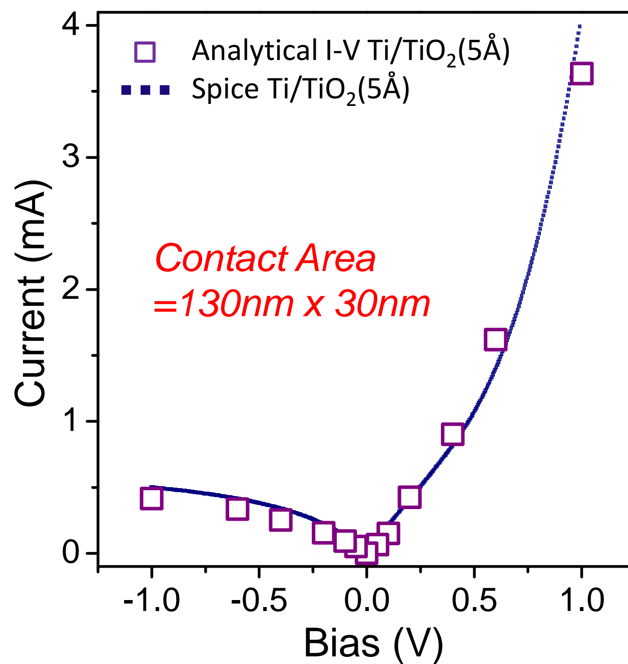


Figure II-26: Overlays of I-V characteristics obtained with analytical 1-D modelling and I-V characteristics reconstructed by combining elementary SPICE components.

The contacts modelled by SPICE were then plugged on each side of 10FDSOI p- and n-MOSFET SPICE blocks developed in STMicroelectronics. The resulting I_d-V_{ds} at V_{gs}=0.7V are presented in Figure II-27 and compared to MOSFETs which are simulated including linear contacts with resistivity respectively equal to $\rho_c=10^{-7}$ Ω.cm², $\rho_c=10^{-8}$ Ω.cm² and $\rho_c=10^{-9}$ Ω.cm².

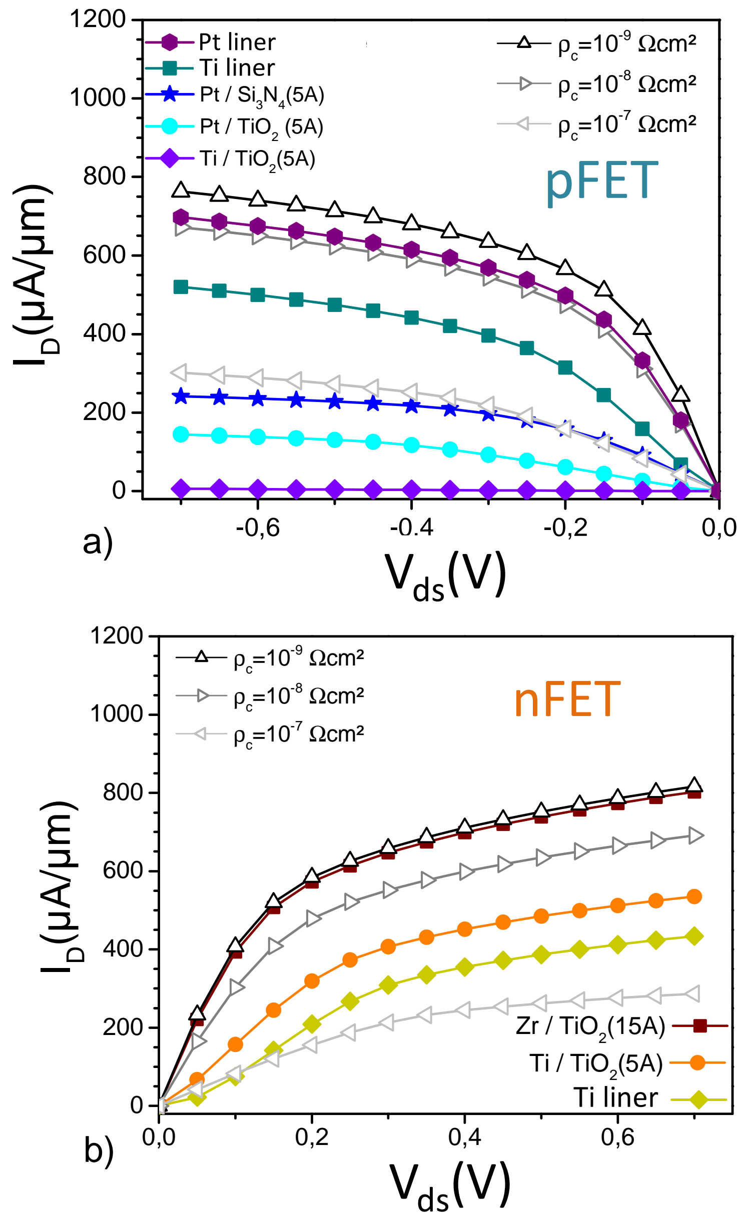


Figure II-27 : Simulated drain current as a function of V_{ds} for ohmic and MIS contacts assuming $q\Phi m(Zr)=4.1$ eV, $q\Phi m(Ti)=4.33$ eV and $q\Phi m(Pt)=5$ eV for scaled (a) p-MOSFET and (b) n-MOSFET (Lg=18 nm, W=130 nm)

Whereas the comparison of the studied contacts performance with the ohmic references was not immediate by looking to the J-V characteristics on [-1V;+1V] range, considering their impact on I_d-V_{ds} ensures a proper ranking of the different MIS junctions with the references. It appears that the optimal contact configurations as Pt/p-Si and Zr/TiO_2(15Å)/n-Si perform respectively slightly above the 10^{-8} Ω.cm² and below the 10^{-9} Ω.cm² ideal contacts.

These results obtained on n-FETs suggest that the effective contact resistivity value recommended by the ITRS can be approached using the MIS contact strategy. Nevertheless, p-FETs performance suffer from the lack of low VBO dielectrics and judging solely from the impact on static output current, it seems that the equivalent contact resistivity on p-FETs is capped around 10^{-8} Ω.cm².

Again, it is worth noting that the near-equivalence in term of DC performance between the Zr/TiO_2(15Å)/n-Si and the 10^{-9} Ω.cm² could easily have been missed by merely looking at J-V curves on an extended [-V_{dd};+V_{dd}] interval. Indeed, the effective biases across each contact at V_{dd} equal 0.7V were plotted against V_{gs} for a Ti insertion-free contact, Ti/TiO_2 and Zr/TiO_2 MIS junctions in Figure II-28 and appear to vary by one decade depending on the considered contact.

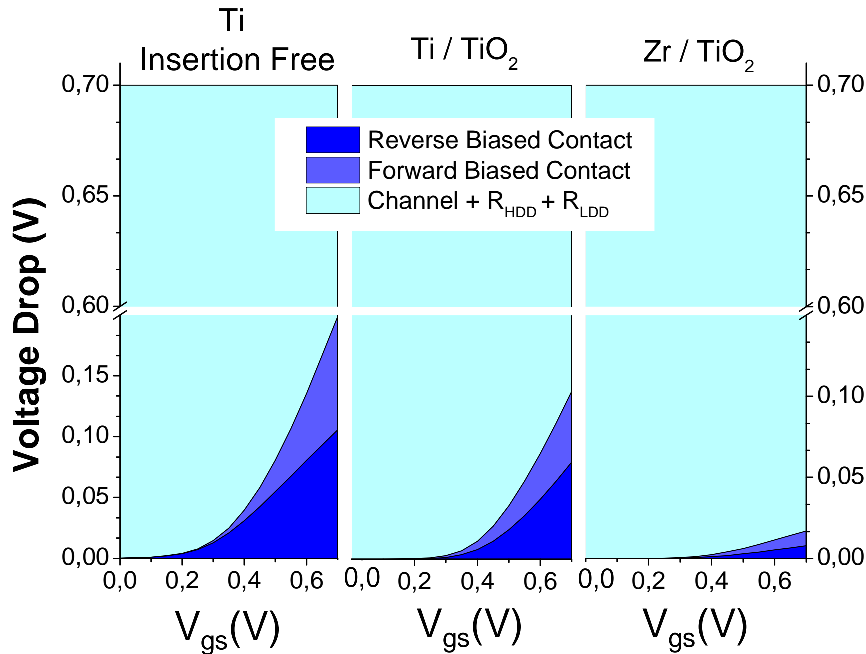


Figure II-28: Sharing of V_{ds} voltage between the contacts and the transistor block for insertion free contact, Ti/TiO_2(5Å) and Zr/TiO_2(15Å) MIS contacts.

In the ON-State (V_{gs}=V_{dd}) the total parasitic voltage drop is measured at 198 mV for the reference configuration, whereas the Ti/TiO_2(5Å) bilayer adsorbs 102 mV and the Zr/TiO_2(15Å) stack only 17 mV.

Moreover, SPICE simulations allow to extract the bias at each node of the circuit and then to know exactly the voltage drop occurring in the reverse biased contact, the forward biased one and the inner MOSFET. One can see in Figure II-28, that whereas the respective contribution of the forward and reverse contacts are equal in the case of Zr/TiO_2(5Å) combination, they differ in the cases of the insertion

free and the Ti/TiO_2(5Å) contacts. This difference can be seen in Figure II-22 (a). Indeed, in this figure one can see that the J-V characteristics is much more symmetrical in the case of Zr/TiO_2(5Å) based MIS contact than in the cases of the other two contacts. Therefore when plugged to a transistor and thus in a back-to-back configuration, the voltage drop is balanced in the case of Zr/TiO_2(5Å) i.e. the reverse contact and the forward one have the same contribution, whereas it is unbalanced in the cases of the insertion free and the Ti/TiO_2(5Å) contacts.

II.3.2 Impact on AC performance

The DC characteristics improvement relying on equivalent contact resistivity reduction is a first figure of merit which can be used to evaluate the suitability of a MIS contact. Nevertheless, as stated previously the equivalent resistivity has to be considered at the actual operative contact bias since the I-V characteristics of the majority of MIS contacts are neither perfectly linear nor symmetrical. Already important in the static study, this assertion is even more relevant in the time-dependent regime since the applied bias V_{app} is no longer constant and periodically varies between *0* and $+V_{dd}$.

Moreover, a non-conformal dielectric insertion also results in what can be modeled by a capacitor (C_{MIS}) in parallel with the contact diode (R_{MIS}) as shown in Figure II-29 *[Borrel_2015']*. A non-conformal dielectric can typically results from using Physical Vapor Deposition (PVD) techniques.

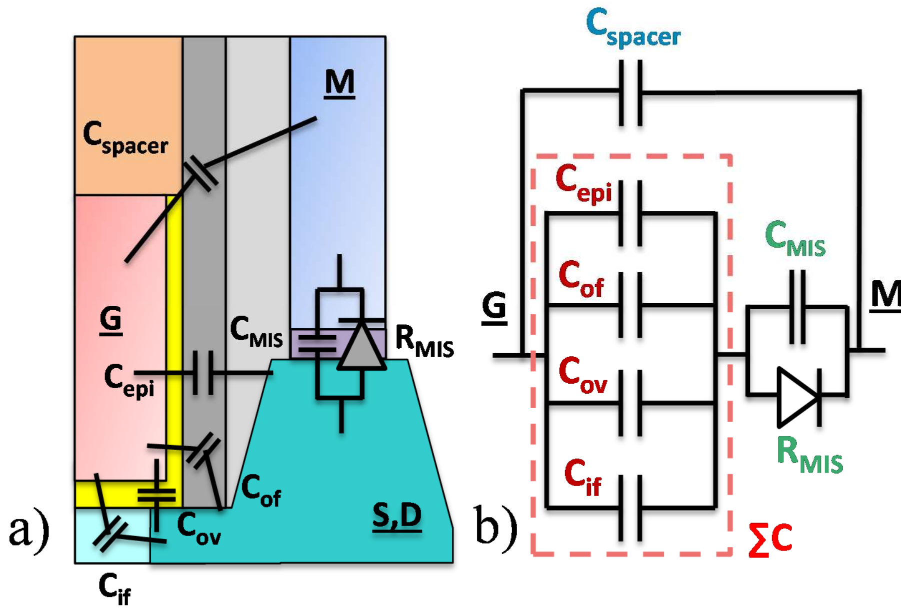


Figure II-29: (a) Structure of a transistor presenting the usual parasitic capacitances and the one induced by the dielectric insertion. (b) Equivalent electric block diagram for non-conformal dielectric deposition.

As seen in Chapter I, the typical figure of merit often used in the ITRS is reminded here in Equation (II-39). In this approximation, the delay of a transistor charging the gate of another transistor depends on both R_{ON} and $C_{g,tot}$.

$$\tau_{int} = \frac{C_{g,tot}V_{dd}}{I_{d,sat}} = C_{g,tot}R_{ON} \qquad \text{(II-39)}$$

Therefore, though irrelevant in DC regime, C_{MIS} may have a significant impact on the dynamic response of a transistor featuring MIS contacts. It should be noted that the considered MIS contacts being

based on ultrathin high-k dielectric insertions, the resulting capacitors are substantial i.e. their impact is expected to be considerable.

II.3.2.a Ring oscillator frequency

Consequently, studying the effect of the MIS contacts on the 10nm node AC performance was achieved through evaluating its influence on the delay of inverter composed with such MOSFETs.

This gauging was performed using ring oscillators, noted R.Os in the following. Indeed, the frequency of an oscillator can be calculated as in Equation (II-40) [*Mandal_2010*].

$$f_0 = \frac{1}{2N\tau_{int}} \quad \text{(II-40)}$$

where *N* is the number of stages of the R. O. (here 7) and τ_{int} is the delay of each stage. Then knowing the variation of the frequency of a R.O. gives access to the delay of one stage, which is representative of the resistive and capacitive elements induced by the MIS contact. The ranking of the junctions was performed by correlating the R.Os frequency with the type of contacts flanking the MOSFETs of the inverters.

From this perspective, ring oscillators were implemented using SPICE simulation. As illustrated in Figure II-30 (a), inverters based on p- and n-MOSFETs flanked by MS or MIS contacts were generated using the SPICE blocks defined previously. 7-stages R.Os were implemented with various combinations of dielectric insertions and metallizations (see Figure II-30 (b)). Finally the frequency of R.Os oscillations was extracted for each combination. The oscillations of the reference case of Ti liner contact on both n- and p-FETs is represented in Figure II-30 (c) along with the optimal case of a Pt liner contact on p-FET and a Zr/TiO_2 MIS contact on n-FET.

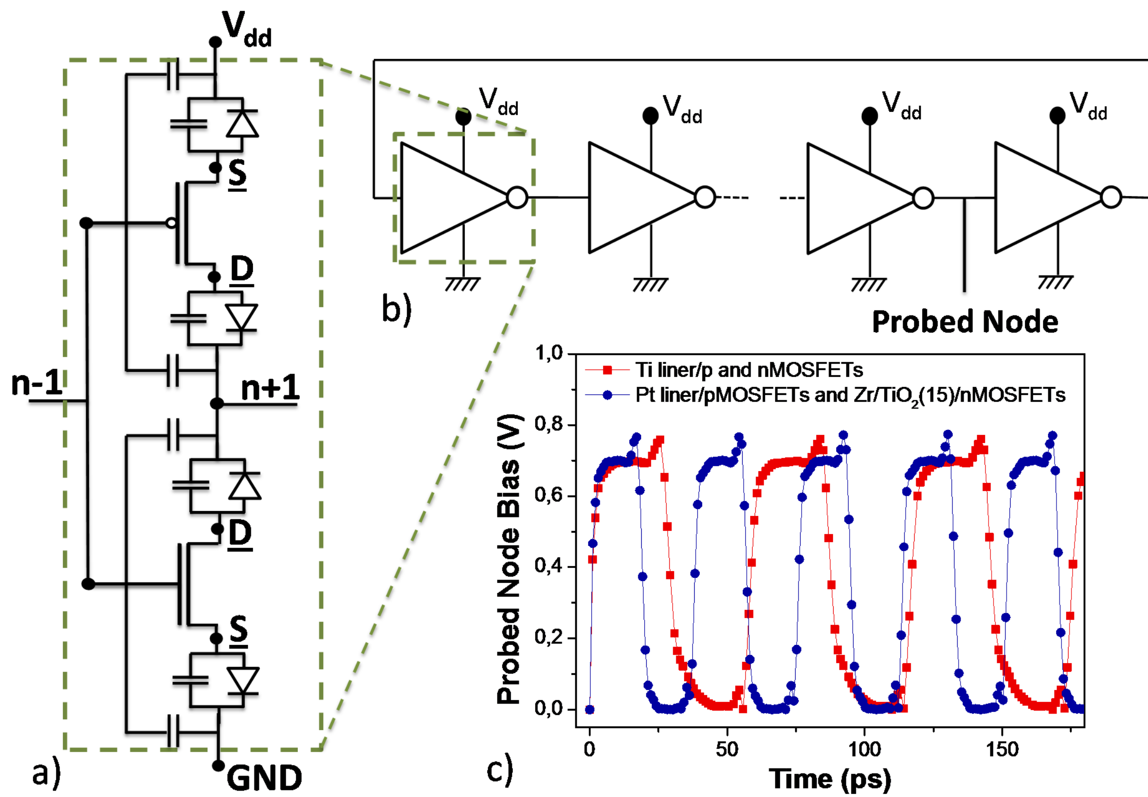


Figure II-30: (a) Elementary inverter presenting MIS contacts. (b) 7 stages ring oscillators were simulated. (c) Resulting probed node bias as a function of the time for Ti liner and MIS contacts optimal configurations at V_{dd}=0.7 V.

In order to compare the time-dependent results with the DC ones, the different configurations of n- and p-type Si based MS and MIS contacts are the same as the ones presented in Figure II-22 and Figure II-27. The R.O. oscillation frequencies are presented in Figure II-31 for the considered combinations of contacts along with that of R.Os composed by p- and n-MOSFETs flanked by $\rho_c=10^{-7}$ Ω.cm², $\rho_c=10^{-8}$ Ω.cm² and $\rho_c=10^{-9}$ Ω.cm² ohmic contacts [*Borrel_2016*].

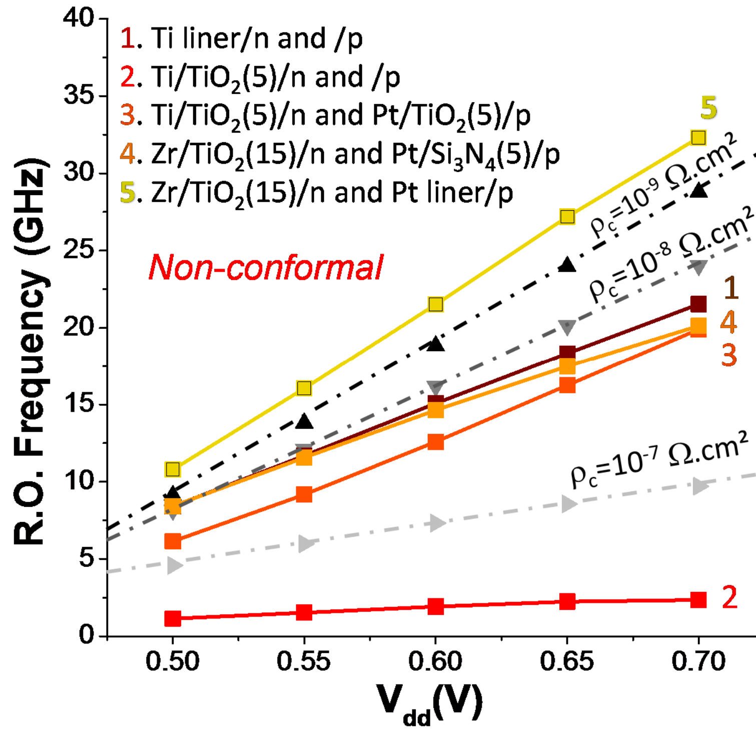


Figure II-31: Oscillation frequency of the R.Os as a function of V_{dd} for different combinations of MIS and MS contacts [Borrel_2016].

The reference case of insertion-free Ti contacts on both p- and n-FETs performs in the AC regime slightly below the $\rho_c=10^{-8}$ Ω.cm² ideal case. Since these contacts do not present any insertion, there is no additional capacitive contribution to consider. Therefore the AC and DC results are in concordance.

As presented in the previous section, p-FETs performance suffering from the lack of low VBO dielectrics, all the combinations of contacts involving an insertion on the p-FETs feature poor oscillation frequency. Thus, a single-insertion single-metallization scheme cannot be considered. Finally, the optimal configuration was found to be the same as in DC i.e. the combination of Pt/p-Si and Zr/TiO_2(15Å)/n-Si.

It is interesting to note that while it could not perform as well as the 10^{-9} Ω.cm² limit in DC, this configuration outperforms it in the dynamic regime. Therefore, the non-conformal insertion implemented in the n-FETs contacts which was initially chosen to optimize the contact resistivity seems to feature an additional impedance reduction in the AC regime.

II.3.2.b Contact complex impedance

Sacrificing some degree of accuracy for the sake of qualitative understanding, notional contacts made of an ideally linear resistor in parallel with a capacitor were connected to p- and n-MOSFETs. Those RC blocks were not fitted on analytically simulated MIS contacts as before. Instead, the R and C parameters were considered arbitrarily tunable and unrelated. Delays of R.Os based on 10FDSOI plugged with these contacts are plotted in Figure II-32.

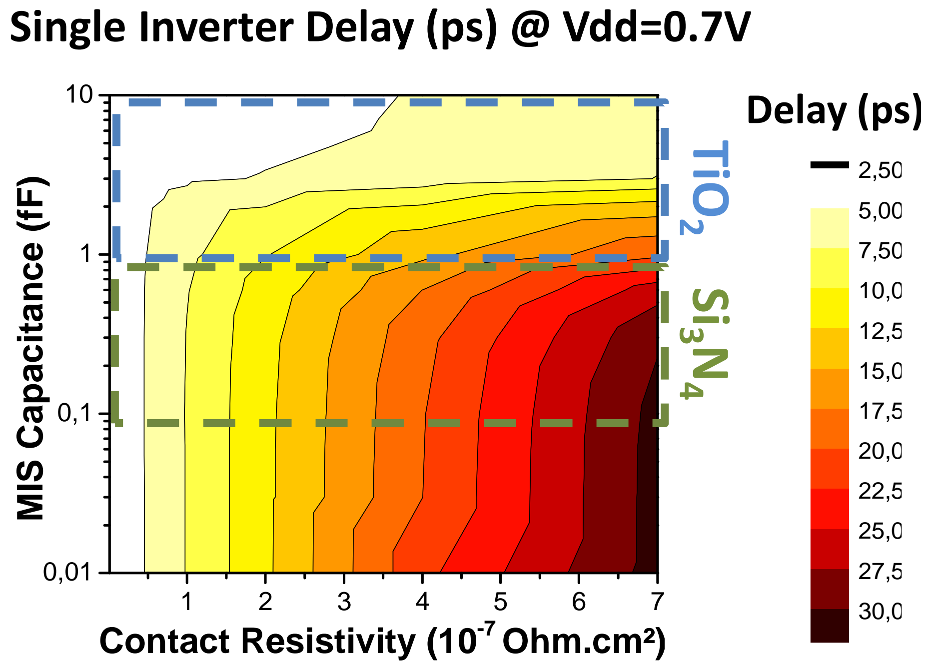


Figure II-32: Delay of a single inverter vs contact resistivity and MIS capacitance in the notional case of a non-conformal insertion based MIS contact presenting ohmic I-V characteristic.

In order to highlight the effect of the capacitance, the range of the resistance was intentionally chosen higher compared to the intrinsic MOSFET resistance and thus to the ITRS target of $\rho_c=10^{-9}$ $\Omega.cm^2$. Doing so, the R.Os delay is dominated by the contact impedance if no capacitance is added to the contact. Moreover, to grasp the impact of common dielectric insertions, the range of capacitance of TiO_2 and Si_3N_4 insertions have been added to Figure II-32. The thickness of the layers was considered between 1 Å and 1 nm.

Results of Figure II-32 suggest that for a given resistance, increasing the contact capacitance reduces the inverter delay. As a matter of fact, the complex impedance of a contact composed by a capacitor in parallel with a resistor is expressed in following Equation (II-41).

$$Z_{eq} = \frac{R}{1 + jRC\omega} \tag{II-41}$$

where R is the equivalent resistivity of the contact, C is its capacitance and ω is the frequency of the applied bias. It is worth noting that the complex impedance is equivalent to R if ω=0 i.e. if the transistor is used in DC regime.

The magnitude of this complex impedance i.e. its modulus is therefore expressed by Equation (II-42).

$$|Z_{eq}| = \sqrt{\frac{R^2}{1 + R^2C^2\omega^2}} \tag{II-42}$$

Therefore, the capacitance primarily acts as a shunt capacitor reducing the conduction path impedance in the AC regime. For a given frequency, if the resistance is non-negligible, this modulus tends to $|Z_{eq}| \approx \sqrt{\frac{1}{C^2\omega^2}}$. Then a low capacitance will lead to high impedance while a high capacitance will lead to a low impedance.

Nevertheless, the single inverter delay was calculated using independently varying R and C. This configuration could not occur in practice since the variation of either the resistance or the capacitance of a MIS contact leads to the variation of its counterpart. Moreover the dielectric layer necessarily introduces current-voltage non-linearity which is not taken in account in this ideal case.

II.3.2.c Conformal dielectric insertion

Aiming at investigating all the foreseeable integration schemes, the case of a conformal deposition of the dielectric insertion was simulated. Conformal deposition can typically be obtained using Atomic Layer Deposition (ALD) or Chemical Vapor Deposition (CVD). Then an additive sidewall capacitance ($C_{MIS,\ side}$) in series with the spacer one (C_{spacer}) is present as shown in Figure II-33.

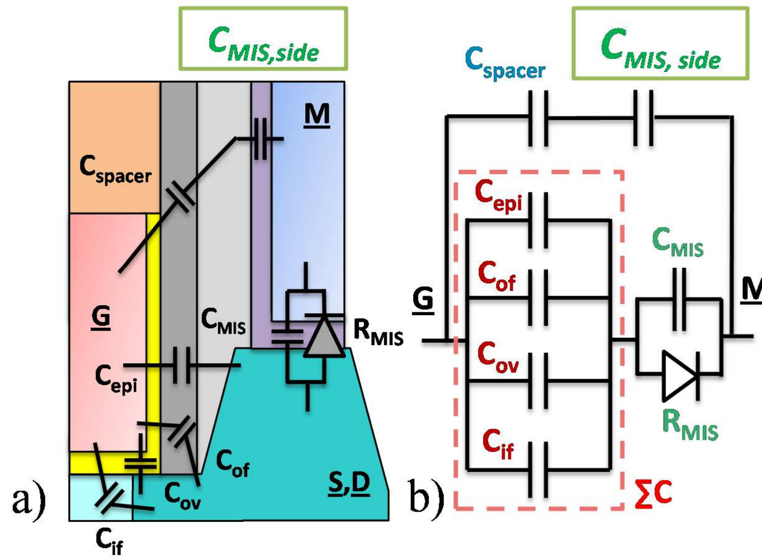


Figure II-33: (a) Structure of a transistor presenting the usual parasitic capacitances and the ones induced by the conformal dielectric insertion. (b) Equivalent electric block diagram for conformal dielectric deposition.

For similar reasons that C_{MIS} is expected to be large i.e. the considered MIS contacts are based on ultrathin high-k dielectric insertions, $C_{MIS,\ side}$ is also expected to be extensive. Nevertheless, being in series with C_{spacer}, its high value will results in a poor impact on the R.Os frequency. The modified R.O. oscillation frequencies are presented in Figure II-34.

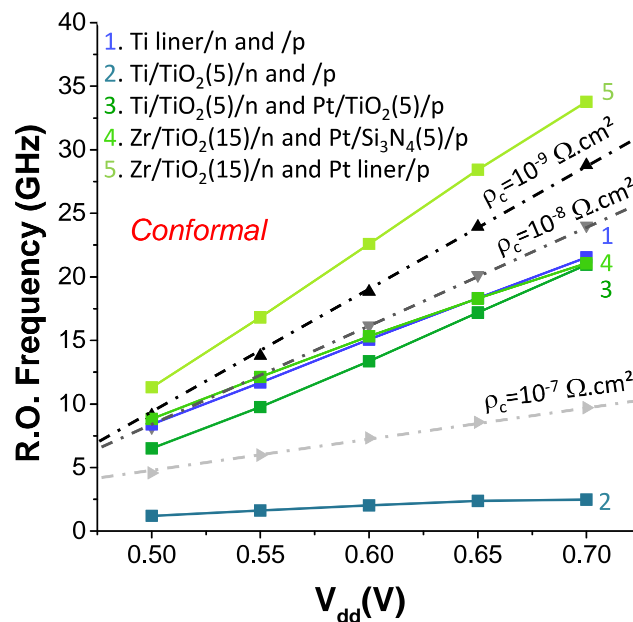


Figure II-34: 7 stages R.O. oscillation frequency as a function of the supply voltage for conformal dielectric insertions.

Featuring the same ranking of the different contacts configurations as in the non-conformal case, a slight gain is observed when using a conformal deposition. The net effect is equivalent to slightly lowering the lateral parasitic C_{spacer} for little to no penalty on the DC current flow.

A summary of all the single inverter delays versus integration scheme and type of deposition is shown in Table II-2.

Table II-2: Single inverter delay extracted from the ring oscillator frequency as a function of the contacts used to plug the transistors. The color code refers to the conduction efficiency of the contact.

	Contacts		Single Inverter Delay (ps) @V_{dd}=0.7V		Conformal vs. Non-Conformal Gain
	p-side	n-side	Non-Conformal	Conformal	
Ohmic	1e-7	1e-7	7.357		
Single MIS	Pt/TiO_2(5Å)	Ti/TiO_2(5Å)	3.589	3.407	5.1%
Dual MIS	Pt/Si_3N_4(5Å)	Zr/TiO_2(15Å)	3.549	3.389	4.5%
Reference	Ti liner	Ti liner	3.319		
Ohmic	1e-8	1e-8	2.973		
Ohmic	1e-9	1e-9	2.481		
Hybrid	Pt liner	Zr/TiO_2(15Å)	2.210	2.116	4.3%

In this table, the first column refers to the type of integration: "Ohmic" stands for contacts made of ideal ohmic contacts; "Single MIS" and "Dual MIS" corresponds to MIS contacts on both p and nFETs using same or different dielectrics to address the two polarities respectively. Finally "Hybrid" refers to the case in which one polarity features a MS contact while the other a MIS one.

II.4 Chapter conclusions

In this chapter, the study of the MIS contacts effective impact on aggressively scaled transistor DC and AC performance is carried out.

In the first part, performing 1-D analytical modeling of MS and MIS it is shown that no optimal single-insertion single-metallization co-integration on n- & p-Si can be found. This issue arises from two main origins. On the one hand, the basic idea of using MIS contacts being to mitigate the Fermi level pinning, the effective metal work function tends to the ideal one. Then, in order to induce a low Schottky barrier height on respectively n- and p-Si, the chosen metallization has to be an n- and p-metal, respectively. Therefore a single-metallization scheme cannot be considered in order to address simultaneously both polarities. On the other hand, the tunneling resistance induced by a given dielectric is not the same for the electrons and the holes. While the resistance seen by the former is proportional to the dielectric conduction band offset to the Si, the one seen by the latter is linked to the valence band offset. Considering dielectric properties from the state-of-the-art, it seems not possible to find an insertion inducing a low tunneling resistance for both types of carriers and, even more, it appears that no insertion can lead to an improved contact on p-Si. Finally, the optimal configuration is found to be a dual-"insertion" (resp. low CBO insertion and no insertion) and a dual-metallization (resp. n- and p-metals). Based on the generated I-V characteristics, this configuration would be Zr/TiO_2/n-Si and Pt/p-Si.

In the second part, evaluating the impact of MS and MIS contact on the MOSFETs DC performance, the optimal contact on p-Si is found to be roughly performing above ideal 10^{-8} Ω.cm² ohmic contact while the optimal MIS junctions on n-type Si was equivalent to a 10^{-9} Ω.cm² ohmic contact. Complementarily, in the third part, we highlight that the shunt capacitor induced by a dielectric insertion on the conduction path has a significant impact on AC performance, allowing an extra improvement beyond the 10^{-9} Ω.cm² ideal case.

In conclusion, even though the implementation of the optimal integration scheme remains non-trivial, the study of AC regime response implies a reassessment of the initial projections on the possible impact of MIS contacts obtained by only considering the DC impact.

In this Chapter, the considered dielectrics are assumed ideal and presenting their theoretical properties (e.g. valence and conduction band offsets, crystallinity...). The FLP mitigation is attributed to the MIGS attenuation without considering DIGS and thus any defects.

Nevertheless, in reality, the dielectric actual properties can appear very far from ideal:

- The different parameters of the dielectrics used to perform the simulations are set at their theoretical value. When considering real experimentally implemented ultra-thin dielectrics,

these physical quantities do not rely on bulk properties but often arise from non-crystalline phenomena.

- When working in the MIS contacts paradigm, the thickness of the considered insertions is typically in sub-nanometer range. At this scale, even a small density of defects cannot be neglected. Then, depending on the process conditions of the dielectric fabrication, it can be foreseen that the DIGS might have a significant impact on the FLP mitigation as well as on the transport properties.
- Moreover, still based on considering the sub-nanometer scale of the dielectric thickness, it is reasonable to suspect that the interactions occurring at the different interfaces (M/I and I/S) might also have a non-negligible incidence on the resulting stack.

Therefore this study of the MIS contacts would not have been complete without practical implementation of such junctions as well as their experimental characterization.

In this context, while the next chapter will be dedicated to present the deposition techniques, the different implemented dielectrics and their resulting physical and chemical properties, the fourth chapter will deal with the electrical characterization of the resulting MIS contacts encompassing all the experimental deviations.

II.5 References

Bethe_1942	**H. A. Bethe;** MIT Radiation Lab Report, No. 43-12; 1942
Borrel_2015	**J. Borrel, L. Hutin, O. Rozeau, P. Batude, T. Poiroux, F. Nemouchi and M. Vinet**; *Considerations for Efficient Contact Resistivity Reduction via Fermi Level Depinning - Impact of MIS Contacts on 10nm Node nMOSFET DC Characteristics*; Symposium on VLSI Technology; 2015
Borrel_2015'	**J. Borrel, L. Hutin, O. Rozeau, M.-A. Jaud, S. Martinie, E. Dubois, M. Vinet**; *At 10nm node, what is the AC impact of dielectric insertions in contact initially meant to decrease the DC contact resistivity?* ; IEEE Semiconductor Interface Specialists Conference; 2015
Borrel_2016	**J. Borrel, L. Hutin, O. Rozeau, M.-A. Jaud, S. Martinie, M. Gregoire, E. Dubois and M. Vinet**; *Modelling of Fermi Level Pinning Alleviation with MIS Contacts – n- & p-MOSFETs Co-Integration Considerations – Part 1 & 2;* IEEE Transactions on Electron Devices, Vol. 63; 2016
Cowley_1965	**A. M. Cowley and S. M. Sze**; *Surface States and Barrier Height of Metal-Semiconductor Systems*; Journal of Applied Physics, Vol. 36; 1965
Dimoulas_2006	**A. Dimoulas, P. Tsipas, A. Sotiropoulus and E. K. Evangelou**; *Fermi-level pinning and charge neutrality level in germanium*; Applied Physics Letters, Vol. 89; 2006
Freeouf_1981	**J. L. Freeouf and J. M. Woodall**; *Schottky barriers: An effective work function model*; Applied Physics Letters, Vol. 39; 1981
Fowler_1928	**R. H. Fowler and L. Nordheim**; *Electron Emission in Intense Fields*; Proceedings of the Royal Society of London, Series A, Containing Papers of a Mathematical and Physical Character, Vol. 119; 1928
Gupta_2013	**S. Gupta, P. P. Manik, R. K. Mishra, A. Nainani, M. C. Abraham and S. Lodha;** *Contact resistivity reduction through interfacial layer doping in metal-interfacial layer-semiconductor contacts*; Journal of Applied Physics, Vol. 113; 2013
Harstein_1978	**A. Hartstein and Z. A. Weinberg**; *On the nature of the image force in quantum mechanics with application to photon assisted tunneling and photoemission*; Journal of Physics C: Solid State Physics, Vol. 11; 1978
Hutin_2010	**L. Hutin**; *Etude des transistors MOSFET à barrière Schottky, à canal Silicium et Germanium sur couches minces*; Ph. D. Thesis, Grenoble University; 2010

Kamgar_1989 **A. Kamgar, R. V. Knoell, F. A. Baiocchi, K. J. Orlowsky, K. P. Cheung and R. Liu;** *Impact of Al Melting on Diode Integrity*; IEEE VLSI Multilevel Interconnection Conference; 1989

Maassen_2013 **J. Maassen, C. Jeong, A. Baraskar, M. Rodwell, and M. Lundstrom;** *Full band calculations of the intrinsic lower limit of contact resistivity;* Applied Physics Letters, Vol. 102; 2013

Mandal_2010 **M. K. Mandal and B. C. Sarkar**; *Ring Oscillators: Characteristics and Applications*; Indian Journal of Pure an Applied Physics, Vol. 48; 2010

Mönch_1990 **W. Monch;** *On the physics of metal-semiconductor interfaces*; Reports on Progress in Physics, Vol. 53; 1990

Mönch_1994 **W. Monch;** *Metal-semiconductor contacts: electronics properties*; Surface Science Vol. 299-300; 1994

Niranjan_2006 **M. K. Niranjan, S. Zollner, L. Kleinman and A. A. Demkov**; *Theoretical Investigation of PtSi surface Energies and Work Functions;* Physical Review B, Vol. 73; 2006

Nishimura_2008 **T. Nishimura, K. Kita and A. Toriumi**; *A Significant Shift of Schottky Barrier Heights at Strongly Pinned Metal/Germanium Interface by Inserting an Ultra-Thin Insulating Film*; Applied Physics Express, Vol. 1; 2008

Padovani_1966 **F. A. Padovani and R. Stratton**; *Field and Thermionic-Field Emission in Schottky Barrier*; Solid-State Electronics, Vol. 9; 1966

Robertson_2002 **J. Robertson**; *Band structures and band offsets of high K dielectrics on Si*; Applied Surface Science Vol. 190; 2002

Shewchun_1967 **J. Shewchun, A. Waxman and G. Warfield**; *Tunneling in MIS structures – I Theory*; Solid-State Electronics, Vol. 10; 1967

Stavitsky_2008 **N. Stavitsky, M. J. H. van Dal, A. Lauwers, C. Vrancken, A. Y. Kovalin and R. A. M. Wolters;** *Systematic TLM Measurements of NiSi and PtSi Specific Contact Resistance to n- and p-Type Si in a Broad Doping Range;* Electron Device Letters, Vol. 29; 2008

Sze_1981 **S. M. Sze**; *Physics of Semiconductor Devices*, 2nd edition; 1981

Tersoff_1984 **J. Tersoff**; *Schottky Barrier Height and the Continuum of Gap States"; Physical Review Letters*, Vol. 52; 1984

Tung_2001 **T. Tung**; *Formation of an Electric Dipole at Metal Semiconductor Interfaces*; Physical Review B, Vol. 64; 2001

Yuan_2011 **Z. Yuan, A. Nainani, Y. Sun, J.-Y. Jason Lin, P. Pianetta and K. C. Saraswat**; Schottky *Barrier Height Reduction for Metal/n-GaSb Contact by Inserting TiO_2 Interfacial Layer with Low Tunneling Resistance*; Applied Physics Letters, Vol. 98; 2011

Chapter III
Implementation and physico-chemical characterization of ultra-thin dielectrics

Introduction to Chapter III 123

III.1 Deviation from ideal process flow 124

III.1.1 Control of the substrate surface oxidation 124

III.1.2 MIS contacts instability 126

III.2 Experimental results 133

III.2.1 Indirect TiO_x implementation by scavenging 134

III.2.2 ALD based high-k implementations 141

III.2.3 CVD based high-k implementations 149

III.3 Chapter conclusions 152

III.4 References 154

Introduction to Chapter III

In the previous chapter, simulation was presented as a first approach used to screen the potential candidates for MIS contacts application from a theoretical point of view. Whereas using modeling allowed to gather fundamental understanding of such contacts, DC and AC SPICE simulations enabled to link stand-alone contact I-V characteristics with their impact on MOSFETs performance. Nevertheless, modeling and simulations are based on assumptions which can be overly simplistic as discussed in the conclusions of the previous chapter.

In Chapter III, practical concerns about ultra-thin dielectric implementation are discussed. In the first part, an overview is dedicated to the different parasitic phenomena suspected to arise during the process of fabrication. In the second part, physico-chemical characterizations are presented for different stacks, with a specific attention to the interactions occurring at the interfaces between materials within the MIS contacts.

III.1 Deviation from ideal process flow

In this first section, the focus is set on parasitic phenomena possibly occurring at the critical steps of the fabrication process.

III.1.1 Control of the substrate surface oxidation

According to the theory of tunneling, one of the major parameters to consider in order to evaluate the dielectric induced tunnel resistance at a given thickness is the Conduction and Valence Band Offsets (resp. CBO and VBO). These values are represented in Figure II.23 and reminded here in Figure III-1.

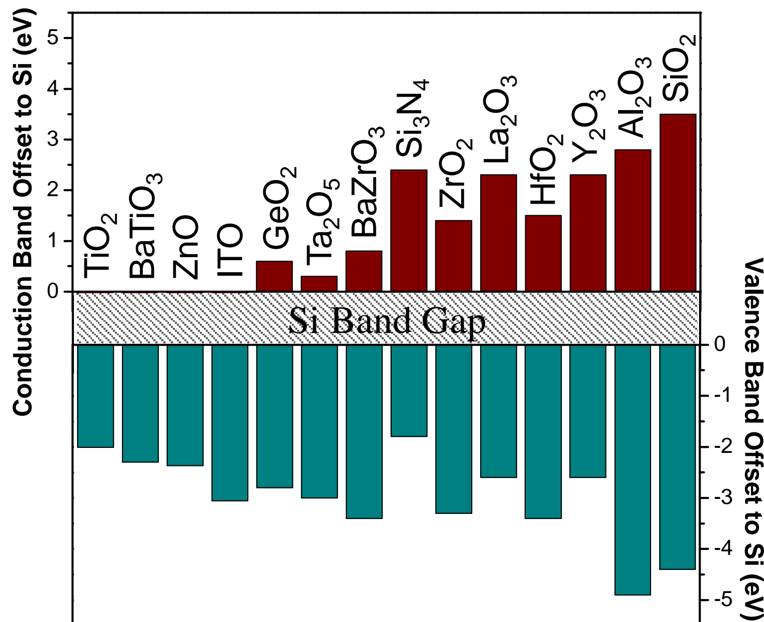


Figure III-1: Conduction and Valence Band Offsets to Si of various dielectric [Gupta_2013, Robertson_2002].

To grasp an idea of the induced tunnel barrier, SiO_2 can be compared to Al_2O_3 since their CBO and VBO values present similar high values. In Chapter II, simulations of Al_2O_3 show significant degradation of the current density of contacts based on this insertion as presented in Figures II-16 (a) and (b). This deterioration appears to be significant even with only a 3 Å thin dielectric (one decade of current less on p-Si presenting a doping concentration of $N_a=10^{20}$ at.cm^{-3}).

Now going back to SiO_2, a small thickness of 3 Å roughly corresponds to the bond length of O-Si-O [*Baur_1977*] meaning only 2 mono layers of substrate oxide. It can be therefore anticipated that even a small regrowth of substrate oxide could lead to dramatic degradation of the MIS contacts properties.

Therefore a particular attention should be paid to controlling the quality of the substrate surface but also to evaluate the thickness of a hypothetical interfacial oxide.

III.1.1.a Substrate passivation prior to insertion deposition

In order to start from the most favorable surface state, the substrates have to be cleaned prior to the dielectric deposition by removing the native oxide and passivated to prevent re-oxidation. HF-last cleaning has been over the years a process of choice to perform the oxide removal on Si. It has been shown [*Chabal_1989*] that this technique generates a passivated substrate surface saturated in Si-H bonds. This passivation ensures a relative stability of the surface and a delay of re-oxidation. When considering the oxide thickness regrowth as a function of time of air exposure in minutes, the growth rate was found to be around 0.2 $nm.decade^{-1}$ [*Mende_1983*].

Thus, in a case of a short queue time between the cleaning of the substrate and the deposition of the dielectric, it seems possible to perform these steps in two different tools without obtaining an important substrate oxide regrowth. Fabricating the samples in industrial and semi-industrial environments, the queue time between processes was not avoidable. Most of the experiments presented in this work were carried out with a maximum delay of 4 hours between the cleaning and the insertion deposition (unless otherwise specified).

III.1.1.b Dielectric deposition induced re-oxidation

Beside oxidation occurring in the environment, the deposition technique used to implement the dielectric on H-passivated Si also plays an important role in the interface quality. Depending on the precursors and on the temperature of process, chemical reactions can occur at the substrate surface introducing new layers formation (such as silicate) or substrate oxide regrowth.

- Chemical Vapor Deposition (CVD)

In 1998, Gilmer *et al.* [*Gilmer_1998*] studied the interface quality resulting from the CVD deposition of a thick TiO_2 layer. The dielectric was implemented in Ultra High Vacuum (UHV) CVD reactor using tetranitratotitanium (TNT) precursor on HF-passivated Si and operating at 280°C. An important amorphous layer of approximately 2 nm in thickness was found at the interface between TiO_2 and Si. Without managing to clearly identify its composition, this layer was assumed to be silicon oxide or Ti-silicate.

Similarly, Al_2O_3 deposition on Si(100) using medium temperature (400°C) CVD was studied [*Klein_1999*]. It was found that implementing a thin film of 3.5 nm actually results in obtaining two

sublayers of approximately 1.7 nm. Using X-ray Photoelectron Spectroscopy (XPS), the interfacial layer close to the substrate was found to consist in Al-O-Si bonds thus considered as an Al-silicate layer.

❖ Atomic Layer Deposition (ALD)

Starting from a stable SiO_2 presenting a thickness of 7 Å, studies [*Damlencourt_2003, Damlencourt_2005*] showed that using ALD of HfO_2 could lead to an increase of the substrate oxide from 7 to 12 Å (using $HfCl_4/H_2O$ precursors at 350°C). In the same time, the thickness of SiO_2 was found to be insensitive to depositions of Al_2O_3 (TMA/H_2O at 300°C).

Nevertheless, a surface presenting hydrogen-terminated silicon is much more reactive than a SiO_2 layer. It was found [*Franck_2003*] that ALD deposition of Al_2O_3 (TMA/H_2O at 300°C) on HF-passivated surface leads to an oxide regrowth of 4 Å. Trying to overcome the substrate oxide regrowth, Ho *et al.* [*Ho_2005*] studied the deposition of HfO_2 using ultra-low temperature ALD i.e. 100°C (TEMAH/D_2O precursors). Using this process, high number of ALD cycles (up to 30) were achieved with no evidence of silicon oxide interfacial layer.

III.1.2 MIS contacts instability

Once the MIS contact stack is implemented, the dielectric shares an interface with both the substrate and the metal. Thus several mechanisms can occurs in the stack and can lead to a transfer of elements from one layer to another. Moreover, during their fabrication, samples undergo parasitic thermal budget which can enhance these mechanisms. Considering the ultra-low thicknesses of the dielectric, these effects can have a significant impact on the composition of the layers and on the actual MIS contact configuration.

III.1.2.a Thermally activated chemical phenomena

The two main mechanisms considered in this work are the diffusion of oxygen and the nucleation of a new oxide phase, both of them eventually occurring to a certain extent through the contact.

❖ Diffusion of oxygen

The mechanism of diffusion of an element occurs when a gradient of concentration of this element is present in a system [*Fick_1855*]. A flux appears flowing from the regions of higher concentration toward the ones with low concentration. This phenomenon is described by the Fick's first law which expresses the flux $\vec{J}$ according to Equation (III-1).

$$\vec{J} = -D\vec{\nabla}C \qquad \text{(III-1)}$$

where D is the diffusion coefficient in $m^2.s^{-1}$ and C is the concentration of the considered element in $mol.m^{-3}$. From this equation, one can notice that the magnitude of the flux is proportional to the gradient of concentration.

Considering the Fick's first law as the driving force for diffusion, the variation of the concentration as a function of time varies following the Fick's second law expressed in Equation (III-2) [*Fick_1855*].

$$\frac{\partial C}{\partial t} = D\Delta C \qquad \text{(III-2)}$$

In solids, the diffusion coefficient D follows an Arrhenius law described in Equation (III-3).

$$D = D_0 e^{-\frac{E_A}{kT}} \qquad \text{(III-3)}$$

where D_0 is the maximal diffusion coefficient in $m^2.s^{-1}$ and E_A is the activation energy in J. This activation energy partially depends on the crystal structure in which the diffusion takes place.

Being based on oxidized insertions, the MIS contacts studied in this thesis work present a strong gradient of oxygen concentration. It is thus expected that a diffusion of this element can occur from the insertion toward the metal and/or the semiconductor. These two materials presenting different crystal structures and thus different activation energy, the oxygen may present an asymmetric diffusion. Moreover, the diffusion being thermally activated, the parasitic thermal budget undergone by the sample during the process of fabrication amplifies this coefficient and thus enhances the different diffusions occurring through the contact.

- Nucleation of new phases

The phenomenon of diffusion is limited by the solid solubility in the host material. At some point it can be energetically favorable for the material to react with the oxygen thus forming a more stable new phase. Metal and semiconductor have the tendency to feature such a chemical reaction leading to oxidation [*Totten_2006*]. This chemical reaction is expressed by Equation (III-4).

$$\frac{2x}{y}Mat + O_2 = \frac{2}{y}Mat_xO_y \qquad \text{(III-4)}$$

where *Mat* is the metal or the semiconductor, *O* is the oxygen and *x* and *y* are integers.

Starting from a notional system under an oxygen pressure p_{O_2} of 1 bar and a temperature of 298K, the standard Gibbs energy of formation can be determined according to Equation (III-5) [*Gibbs_1873*].

$$\Delta G_f^0 = \Delta H_f^0 - T\Delta S_f^0 \qquad \text{(III-5)}$$

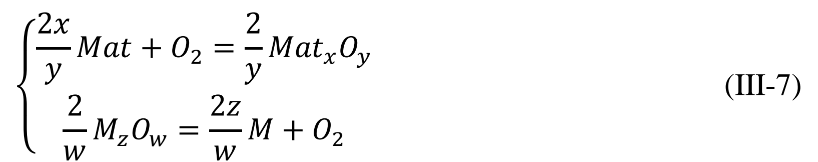
with ΔH_f^0 and ΔS_f^0 respectively the standard enthalpy and the standard entropy of formation. If p_{O_2} differs from 1 bar, the Gibbs energy of formation can be calculated using Equation (III-6).

$$\Delta G_f = \Delta G_f^0 - RTln(p_{O_2}) \qquad \text{(III-6)}$$

with *R* the universal gas constant and *T* the absolute temperature.

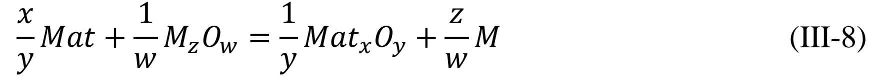
The Gibbs energy represents the driving force of the reaction [*Mellor_1922*]. If ΔG_f^0 is negative, the reaction of Equation (III-4) can take place from the left to the right and the considered material can spontaneously oxidize. If ΔG_f^0 is positive, the oxide phase formation of Equation (III-4) cannot happen. The notion of “possibility” is here of prime importance. If ΔG_f^0 is negative, the reaction can take place but does not necessarily take place. However, if ΔG_f^0 is positive, it is impossible that the oxide phase formation of Equation (III-4) occurs since there is no driving force favoring this reaction.

In this thesis system however, the metal and the substrate are not in contact with air but with a dielectric layer containing oxygen. In order to define the equivalent reaction occurring at one of these interfaces, two reactions, one of oxidation and one of reduction, have to be considered resulting in the system of Equations (III-7).



$$\begin{cases} \frac{2x}{y}Mat + O_2 = \frac{2}{y}Mat_xO_y \\ \frac{2}{w}M_zO_w = \frac{2z}{w}M + O_2 \end{cases} \qquad \text{(III-7)}$$

where Mat is the metal or the semiconductor and M_zO_w is the initial dielectric insertion. Combining the equations of this system leads to the equivalent reaction at one interface:



$$\frac{x}{y}Mat + \frac{1}{w}M_zO_w = \frac{1}{y}Mat_xO_y + \frac{z}{w}M \quad \text{(III-8)}$$

In order to know which oxide is more stable, the standard Gibbs energy of reaction is defined as in Equation (III-9).

$$\begin{aligned} \Delta G_r^0 &= \sum \Delta G_f^0\,(products) - \sum \Delta G_f^0(reactants) \\ &= \frac{1}{y}\Delta G_f^0\left(Mat_xO_y\right) - \frac{1}{w}\Delta G_f^0(M_zO_w) \end{aligned} \quad \text{(III-9)}$$

If ΔG_r^0 is negative, the driving force is favorable to a reaction of Equation (III-8) from the left to the right. It is then possible that Mat gets oxidized to the detriment of M_zO_w which is reduced. If ΔG_r^0 is positive, the reaction of Equation (III-8) cannot happen form the left to the right and the dielectric insertion cannot be reduced.

Thus, knowing the Gibbs energies of formation presented in Equation (III-9) allows a first forecast of potential oxide formation for common metals and the subsequent "stability" of the metal/insulator/semiconductor contact. These values can be found in the literature, as in [Alcock_2000] and [Humpston_2004], and are reported for several common metals in Table III-1.

Table III-1: Gibbs energy of formation in kJ.mol^{-1} corresponding to the oxidation of various common metals [Alcock_2000, Humpston_2004].

Element	Work Function (eV)	Associated Oxide	Gibbs Energy of formation (kJ.mol^{-1})	Gibbs Energy of formation corresponding to 1/2 O_2 (kJ.mol^{-1})
Pb	3.8	PbO	-190	-190
		PbO_2	-210	-105
		Pb_3O_4	-570	-142,5
Ti	4.1	TiO_2	-880	-440
Al	4.2	Al_2O_3	-1580	-526
Zn	4.2	ZnO	-300	-300
Sn	4.3	SnO	-260	-260
		SnO_2	-490	-245
Ag	4.3	Ag_2O_3	-10	-3,3
Cr	4.4	Cr_2O_3	-700	-233,3
Cu	4.6	CuO	-130	-130
		Cu_2O	-150	-150
Pd	4.6	PdO	-221	-221
Ni	5.0	NiO	-235	-235
Au	5.4	Au_2O_3	+50	+50
Pt	5.4	PtO	-221	-221

Nevertheless, evaluating the enthalpy of reaction is just a way to predict which reaction is favorable in terms of driving force. In practice one has also to evaluate the energy needed to nucleate a new phase which represents a barrier of energy to overcome.

According to [*Abraham_1974*], if considering one droplet of radius r of the new phase and noting Δg_f^0 the Gibbs energy of formation per unit volume and σ the surface tension of the interface between the droplet and its surrounding, the Gibbs energy of nucleation is expressed in Equation (III-10).

$$\Delta G^0(r) = \frac{4}{3}\pi r^3 \Delta g_f^0 + 4\pi r^2 \sigma \quad \text{(III-10)}$$

The first term of this equation is a volume term and represents the gain in terms of Gibbs energy when replacing a droplet of the new phase in the initial one. The second term is a surface term and represents the cost of energy at the interface between the two phases. In the case of a negative Δg_f^0 (favorable driving force), the typical curve of $\Delta G^0(r)$ as a function of r is represented in Figure III-2. This curve presents a barrier of energy that the system has to overcome in order for the reaction to effectively occur.

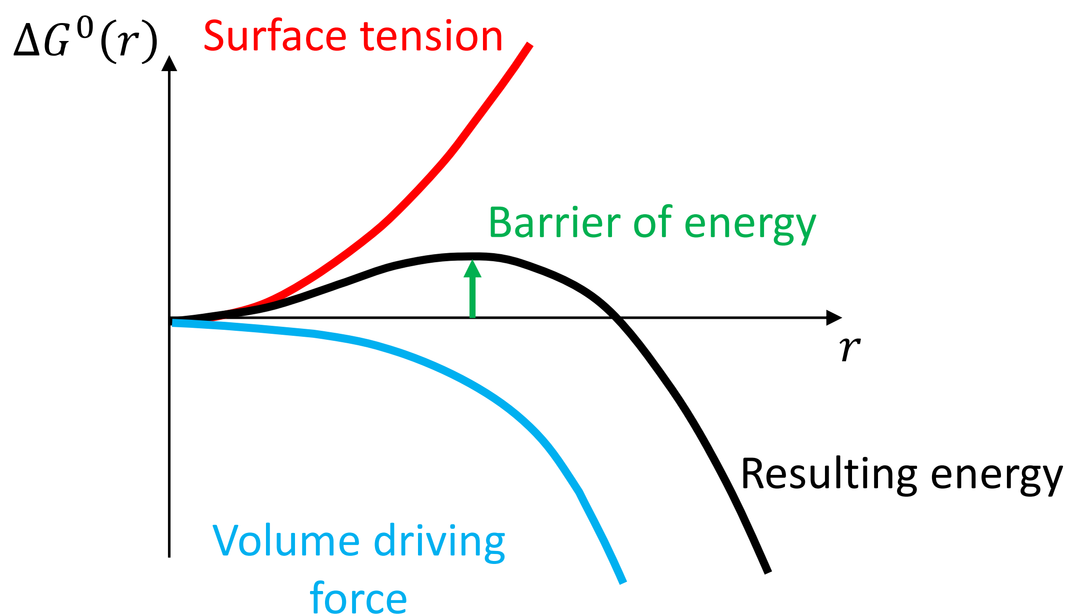


Figure III-2: Typical curve of $\Delta G^0(r)$ as a function of r in the case of a favorable enthalpy of formation per volume unit.

To summarize, the stability of an oxygen-based insertion is governed by the phenomena of diffusion and of new phase nucleation. While the former is only driven by the gradient of oxygen concentration, the latter is based on energetic considerations. The evaluation of the Gibbs energy of formation allows to anticipate which reaction could occur. However, it does not ensure this reaction to actually take place since the barrier of energy induced by the nucleation has to be overcome. Moreover, all the values of Gibbs energy, surface tension and diffusion coefficient can only be found in the literature for the case of bulk materials presenting a defined crystal structure. In the case of this work, the ultra-thin layers are possibly amorphous and these values might be inadequate.

III.1.2.b MIS instability in the state-of-the-art

❖ Oxygen-diffusion-induced substrate re-oxidation

As mentioned earlier, using ultra-low temperature ALD of HfO_2 (TEMAH/D_2O precursors at 100°C), Ho *et al.* [*Ho_2005*] managed to achieve high number of ALD cycles (up to 30) with no evidence of silicon oxide interfacial layer formation. Nevertheless, trying to evaluate the robustness of their stack, post-deposition annealings were performed at various temperatures. It was shown that a 450°C anneal (duration not given) was sufficient to form SiO_2. Ramping up to 700°C led to the regrowth of a 7.2 Å thick silicon dioxide. This oxidation was attributed to the diffusion of oxygen contained in HfO_2 into Si. Before the annealing the hydrogen atoms presents at the HfO_2/Si interface act as a barrier for diffusion.

The annealing removes the remaining hydrogen and allows the excess oxygen contained in the HfO_2 to penetrate the Si leading to the oxidation.

❖ Dielectric degradation by oxygen diffusion

More recently, Yu *et al.* [*Yu_2015*] have studied the stability of TiO_x based MIS contacts as function of the annealing temperature. Using Ti metallization, it was shown that even a moderate post-metal thermal budget, here 370-400°C for several minutes, was enough to deteriorate the insertion. As shown in Figure III-3, this degradation was attributed to the diffusion of oxygen in the top Ti layer and was confirmed by simulation. Figure III-3 (c) shows the resulting Ti layer containing diluted O after a 500°C annealing.

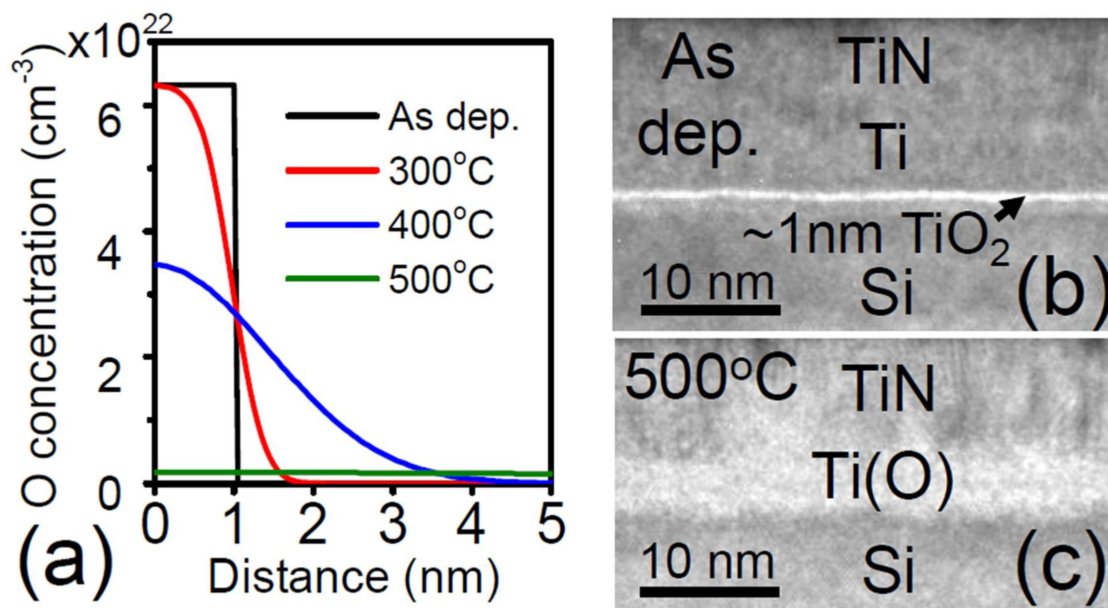


Figure III-3: (a) Simulated O profile in a MIS contact presenting 1 nm ALD TiO_2 after 1 min RTP only considering diffusion of O. (b) and (c) TEM of the corresponding experimental sample respectively before and after annealing [Yu_2015].

Keeping in mind these parasitic phenomena, insertions were implemented in the frame of MIS contacts. HF-last passivation was considered as the required cleaning of the Si surface before dielectric deposition and the queue time between these two steps was kept under 4 hours. Furthermore, these parasitic effects being thermally activated, the process temperatures were kept as low as possible. Unfortunately, a CVD-deposition of W was mandatorily performed at 440°C in the fabrication process. This step occurring after the MIS contact implementation, it might induce modifications of the dielectric insertion. Thus before electrical characterization of the samples, a study of the effective resulting stacks was performed to analyze the possible redistribution of the elements and particularly of the oxygen.

III.2 Experimental results

Three insertions were studied in this work, TiO_2, HfO_2 and Al_2O_3, and can be considered from two points of view.

On the one hand, the dielectrics generate a tunneling barrier that the carriers have to cross to generate the current. According to the VBO and CBO presented in Figure III-1 and as stated in Chapter II, the transmission probability noted T of both holes and electrons across these dielectrics for a given thickness can be sorted as in Equation (III-11).

$$T_{TiO_2} > T_{HfO_2} > T_{Al_2O_3} \quad \text{(III-11)}$$

As presented in Chapter II, the tunnel resistance induced by Al_2O_3 is so large that no optimal thickness was found in a physically achievable range (3 Å when inserting between Ti and n-Si). Thanks to its ultra-low CBO, TiO_2 is however considered as the most promising layer studied in Chapter II and specifically to address n-type Si. Even though it was not studied, reasoning only on the CBO and VBO, HfO_2 can *a priori* be considered as an intermediate candidate.

On the other hand, one has also to consider the stability of these dielectrics when contacted with the substrate and the metal top electrode. As presented in section III.1.2, a first rough image of the dielectric stability can obtained by looking at the Gibbs energy of formation. If considering the values of Table III-1, ΔG_f^0 of the dielectrics can be sorted as in Equation (III-12).

$$-\frac{\Delta G_f^0(Al_2O_3)}{3} > -\frac{\Delta G_f^0(HfO_2)}{2} > -\frac{\Delta G_f^0(TiO_2)}{2} \quad \text{(III-12)}$$

Comparing Equations (III-11) and (III-12), it appears that the stability of the considered dielectrics is ranked in the inverse order than their induced tunnel barrier. Then the process window to find a dielectric both conductive and stable appears to be reduced.

In order to evaluate the actual stability of these dielectrics, experiments were carried out in both STMicroelectronics and LETI clean rooms. In the former, an attempt to implement TiO_2 using an indirect process route was performed by depositing a Ti layer on SiO_2. In the latter, HfO_2 and Al_2O_3 were implemented using Atomic Layer Deposition (ALD), deposition of TiO_2 was performed using Chemical and Physical Vapor Depositions (respectively noted CVD and PVD).

III.2.1 Indirect TiO_x implementation by scavenging

As mentioned in part III.1.2, when implementing a dielectric by conventional deposition, the oxygen contained in the insertion can move away from its original position. This phenomenon is often seen as a detrimental effect since the considered dielectric is the insertion one wants to implement.

Nevertheless, in theory this phenomenon can also be used to create the insertion. Indeed, Ti is well known to be a getter of oxygen i.e. it has the propensity to attract the surrounding oxygen [*Lu_2000*]. Moreover, the Gibbs formation energy of Ti oxide being lower than that of the Si (Table III-1), the reduction of the latter and the oxidation of the former are energetically favorable. Therefore, implementing a layer of Ti on top of a SiO_2 could in theory result in the pumping of the oxygen and is referred to as scavenging [*Ando_2009*].

Additionally, as evoked in the introduction, a usual deposition technique can lead to a substrate re-oxidation. This SiO_2 oxide leads in theory to a dramatic current degradation and a particular attention should be dedicated to tackle this re-oxidation. Using this scavenging-based implementation technique has the advantage to avoid bringing oxygen from an outside source namely from the precursors or from an O_2 plasma. Thus in case of an actual scavenging effect, the resulting substrate oxide can be expected to be thinner than the one observed after a conventional deposition technique.

❖ State-of-the-art

In 1983, Butz *et al.* [*Butz_1983*] observed such reduction of the Si-O bonds at room temperature when depositing 5 Å of Ti on a thermally oxidized Si. Nevertheless, upon a sufficient annealing of 300°C, it was found that these bonds were not stable and that Ti-Si was instead preferentially formed.

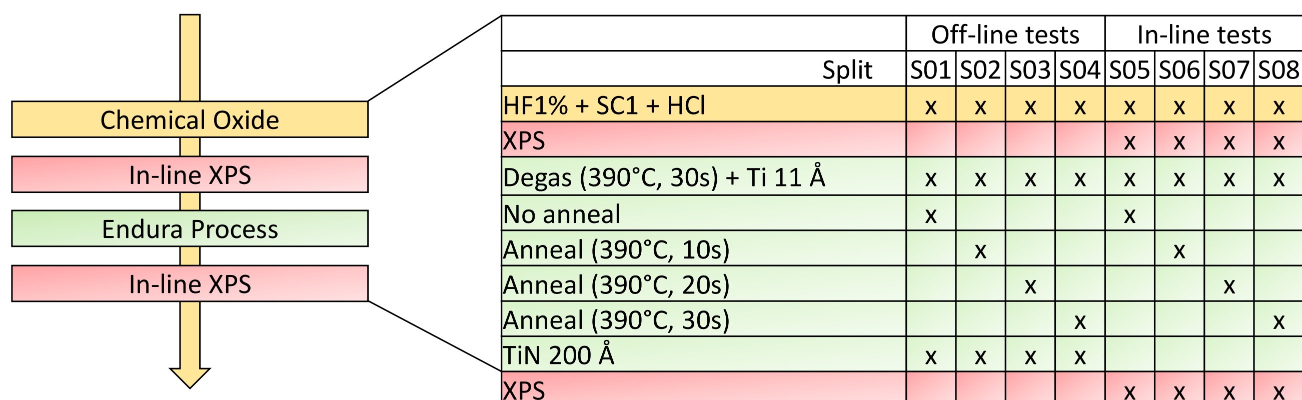
Similarly, in 2010, Oswald [*Oswald_2010*] found that depositing an ultra-thin layers of Ti of various thicknesses on a thick thermal SiO_2 leads to the formation of a Ti oxide layer. Nevertheless, the formation of a Ti_xSi_y layer was observed even at room temperature. Surprisingly this layer was found to be on the top of Ti oxide layer and not at the interface between SiO_2 and TiO_2. For instance, in the case of a Ti deposition of 53 Å, the resulting stack was found to be Ti(18Å)/Ti_xSi_y(22Å)/TiO_x(24Å)/SiO_2.

❖ Process flow

Attempts to implement insertions of TiO_x using scavenging of SiO_2 were performed in STMicroelectronics cleanroom.

In this part, for the sake of simplicity, the description of the process begins at the entrance of the contact module. Nevertheless, planning electrical characterizations of the resulting contact, wafers also

underwent modules of well and S/D implantations. Steps of fabrication occurring in the contact module for scavenging-based TiO_x are presented in Figure III-4.



	Off-line tests				In-line tests			
Split	S01	S02	S03	S04	S05	S06	S07	S08
HF1% + SC1 + HCl	x	x	x	x	x	x	x	x
XPS					x	x	x	x
Degas (390°C, 30s) + Ti 11 Å	x	x	x	x	x	x	x	x
No anneal	x				x			
Anneal (390°C, 10s)		x				x		
Anneal (390°C, 20s)			x				x	
Anneal (390°C, 30s)				x				x
TiN 200 Å	x	x	x	x				
XPS					x	x	x	x

Figure III-4: Process flow restricted to the contact module in the case of the scavenging-based TiO_x.

After having undergone all the steps of implantation, the wafers entered the scavenging module with a chemical cleaning comprising a HF (1%), a SC1 (diluted NH_4OH and H_2O_2) and a HCL cleanings. While the former is used to remove the existing uncontrolled oxide, the 2 other steps eliminate the organic and metallic contaminations and ensure the regrowth of a controlled 9 Å thin chemical SiO_2.

Prior to going through the Ti deposition and annealing steps, a first XPS measure was performed on the in-line tests wafers (S05 to S08) in order to obtain a reference spectrum just after the initial cleaning. This in-situ XPS is based on a monochromated Al Kα source. Its resolution does not allow to separate the two components of the Si2p peak ($Si2p_{1/2}$ and $Si2p_{3/2}$). The results are shown in Figure III-5 (a) et (b) respectively representing the Si2p and the O1s binding energy regions.

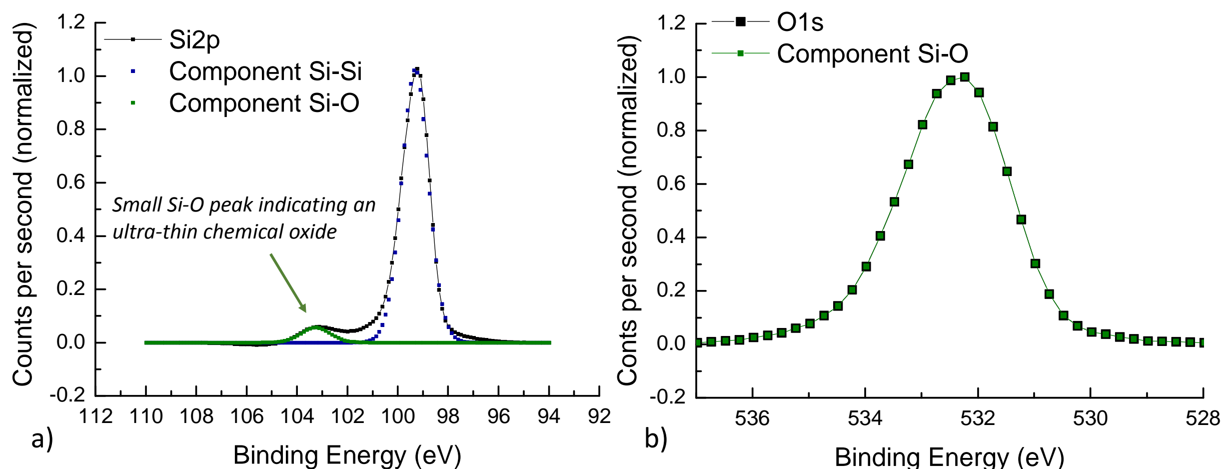


Figure III-5: XPS spectra of (a) Si2p and (b) O1s regions between the chemical cleaning and the Ti deposition.

According to [*Wagner_1979*], the binding energy of the component representative of the Si-Si bonding is considered at 99.3 eV while that of the Si-O at 103.3 eV. These values were thus used to calibrate the binding energies of the measured spectra. In the O1s region, the signal was found centered around 532.3 eV and as expected corresponds to a SiO_2 compound [*Wagner_1979*].

The scavenging module consisted then to deposit a thin Ti layer of 11 Å using RF PVD (Radio Frequency PVD). This deposition had to be preceded by a degassing step (noted Degas in Figure III-4 and performed during 30 s at 390°C) used to volatilize any residual moisture that remained after the pre-clean. After the deposition of Ti, in-situ annealings were performed without vacuum break. These annealings were expected to enhance the reaction of the {Ti,Si,O} system. All of them were performed at 390°C but for various times, 0, 10, 20 and 30 s, as presented in Figure III-4.

The wafers were then split along two routes. The ones dedicated to perform off-line physico-chemical and electrical characterizations (S01 to S04) underwent the full process of the module i.e. they were capped by 200 Å of PVD TiN. The others (S05 to S08) were used to perform in-line XPS measurements of the resulting stack and thus were not capped.

❖ Physico-chemical characterizations

The XPS measurements of wafer S05 obtained after the deposition of Ti are presented in Figure III-6 (c) and (d) and are compared to the results obtained prior to the deposition in (a) and (b).

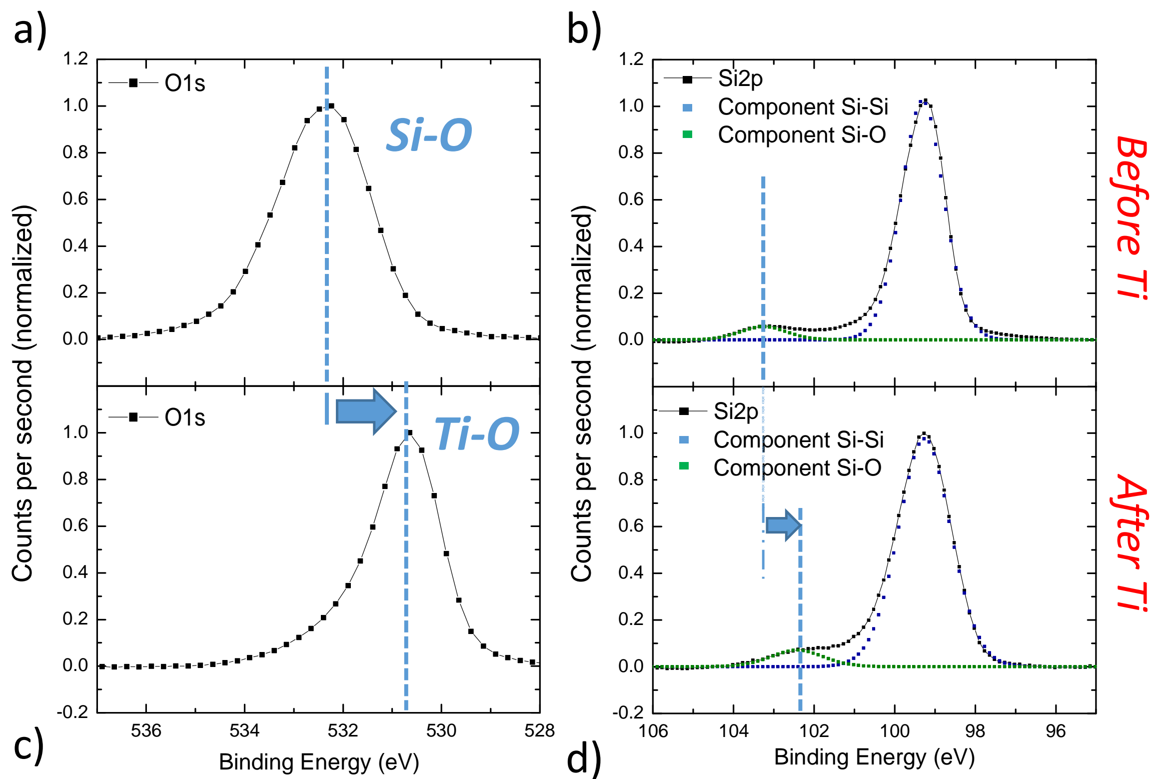


Figure III-6: In-line XPS measurements of S05 (a) (b) before and (c) (d) after Ti deposition.

As shown in Figure III-6 (c), the deposition of Ti induces a shift of -1.7 eV of the O1s core level. Moreover, this core level is not symmetrical and features a shoulder on the higher energy. Such a resulting peak has already been observed by Fulton *et al.* [*Fulton_2002*] and was attributed to the formation of an intermediate Ti-silicate in between the SiO_2 and TiO_2. Nevertheless, this shoulder remains low and the O1s core level seems to be dominated by the TiO_2 signature. Considering the Si2p region (Figure III-6 (d)), the magnitude of the Si-O component appears unmodified by the Ti deposition as expected if the scavenging effect had pumped the oxygen from the SiO_2 layer. However, its position is shifted by -1eV.

Therefore, these observations suggest that the amount of Si-O bonds has not been decreased but that their chemical environment has been modified. According to [*Fulton_2002*] this phenomenon is also a signature of the formation of a Ti-silicate.

In order to study the influence of the thermal budget on the scavenging enhancement, similar XPS measurements were performed on S06, S07 and S08 (resp. anneal lasting 10 s, 20 s and 30 s). This influence was evaluated through the evolution of the Si-O component position and also through its relative intensity compared to the Si-Si signal. Results are plotted along in Figure III-7.

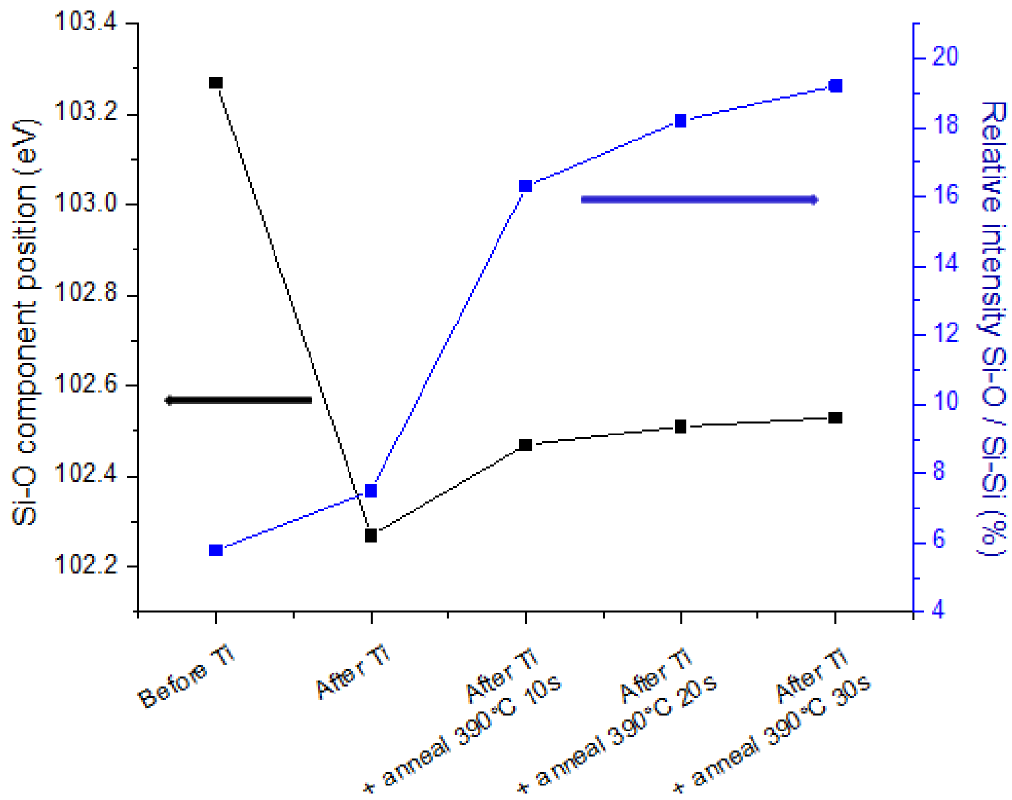


Figure III-7: (black) Evolution of the Si-O binding energy and (blue) relative intensity Si-O / Si-Si as a function of the undergone process split.

As clearly illustrated by this figure, the disappearance of the Si-O component as expected in the case of a successful scavenging process is not observed. On the contrary, Figure III-7 suggests that this component intensity is enhanced by thermal budget. Concerning its position, even if a slight shift toward the higher energies is observed if increasing the annealing time, the Si-O peak remains in the silicate range of binding energy (around 102.5 eV).

XPS gives information about the nature of the bonds. Thus it can be completed by other physical characterizations in order to obtain details about the spatial organization of the elements in the stack. Time Of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) was used to analyze the composition of the thin films. The technique was used on S05 and S08 which represent the most extreme cases in terms of annealing budget i.e. respectively no anneal and 30 s of annealing. An overlay of their depth profiles is presented in Figure III-8.

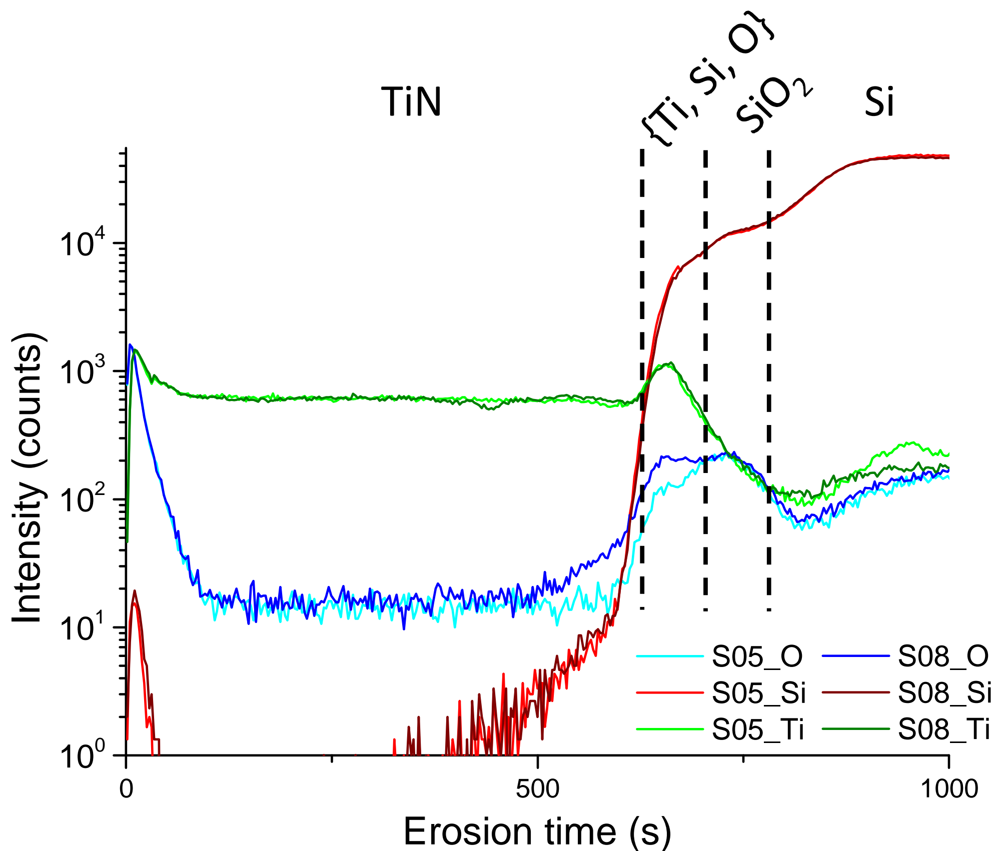


Figure III-8: Overlay of the TOF-SIMS depth profiles of S05 and S08 resp. no anneal and 30 s at 390°C.

This overlay suggests that some Si has already diffused in the Ti layer before the annealing since its spectrum features a small shoulder in this region. This observation seems in agreement with the XPS evidence of silicate formation.

However no diffusion and inter-mixing of Si and Ti occurs during the annealing since their before- and after-thermal-treatment curves are perfectly overlapped. The only major change can be seen on the oxygen curves. Indeed, the concentration of oxygen contained at the Ti layer surface is increased by the annealing whereas no variation can be seen in the SiO_2 region. This implies that the oxygen incorporated in the Ti layer does not come from the SiO_2 but possibly from the residual oxygen of the annealing chamber.

Combining XPS and TOF-SIMS it seems reasonable to elaborate that the scavenging effect does not take place when depositing Ti over SiO_2. Intermixing of the elements occurs and forms a top layer similar to Ti-silicate. Thus the Si-O component seen with XPS is representative of the bonding between Si and O in the silicate. Its increase in term of XPS intensity is not a signature of an increase of SiO_2 but

of oxygen content in the silicate region. This assumption seems confirmed by the TOF SIMS oxygen depth profile.

According to [*Fulton_2002*], titanium silicates are expected to exhibit a large band gap of energy. Thus it seems likely that such a large gap dielectric would induce a significant tunnel barrier for both the electrons and the holes.

III.2.2 ALD based high-k implementation

❖ Preliminary study

Prior to implementing Al_2O_3 and HfO_2 on electrical test structures, a study of their deposition kinetics had to be performed. Indeed, in order to suppress the native oxide on the substrate surface, a HF cleaning is performed prior to ALD deposition. However, such cleaning modifies the state of surface and thus has an impact on the deposition kinetics. As shown by Bender *et al.* [*Bender_2001*], the growth of high-k materials directly on silicon surfaces (i.e. HF-cleaned surfaces) leads to a delay of nucleation. This delay has been attributed to the lack of nucleation sites, namely OH groups, necessary to initiate the ALD growth.

Study of nucleation delay and deposition kinetics of HfO_2 has already been studied in [*Damlencourt_2003, Damlencourt_2005*]. The deposited thickness as a function of the ALD cycle number is plotted in Figure III-9.

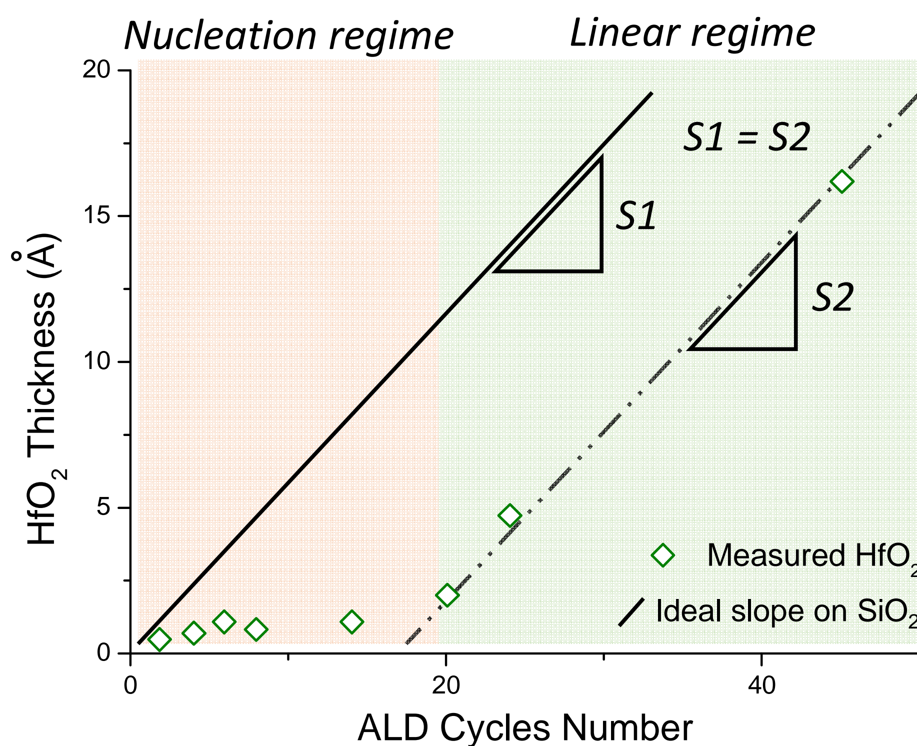


Figure III-9: HfO_2 thickness as a function of the number of ALD cycles on a HF-passivated Si from [Damlencourt_2005].

Similarly to [*Bender_2001*], Damlencourt *et al.* observed a delay when depositing HfO_2 on HF-passivated Si. It was found that after 20 ALD cycles, during which almost no HfO_2 is actually deposited, growth started to recover a classical kinetic. Indeed, the growth rate after this delay of nucleation was found equal to the one obtained on SiO_2 surface.

Working with the same deposition tool and precursors, i.e. Pulsar™ thermal reactor from ASM Microchemistry Ltd with $HfCl_4/H_2O$, these kinetics were considered consistent with experiments preformed in this thesis. Depositions of 15, 20, 25, 30, 35 and 40 cycles were performed in order to obtain HfO_2 layers between 0 and 15 Å.

Trying to obtain information about the nucleation delay and the deposition kinetics of Al_2O_3 on HF-passivated Si, similar experiments were carried out. Starting from a HF-cleaned surface, ALD deposition of Al_2O_3 presenting a variable number of cycles were performed. Pulsar™ reactor from ASM Microchemistry Ltd was used with TMA/H_2O precursors at 300°C. The resulting thickness of Al_2O_3 was measured using Angle Resolved X-ray Photon Electron Spectroscopy (ARXPS). Figure III-10 summarizes the obtained results.

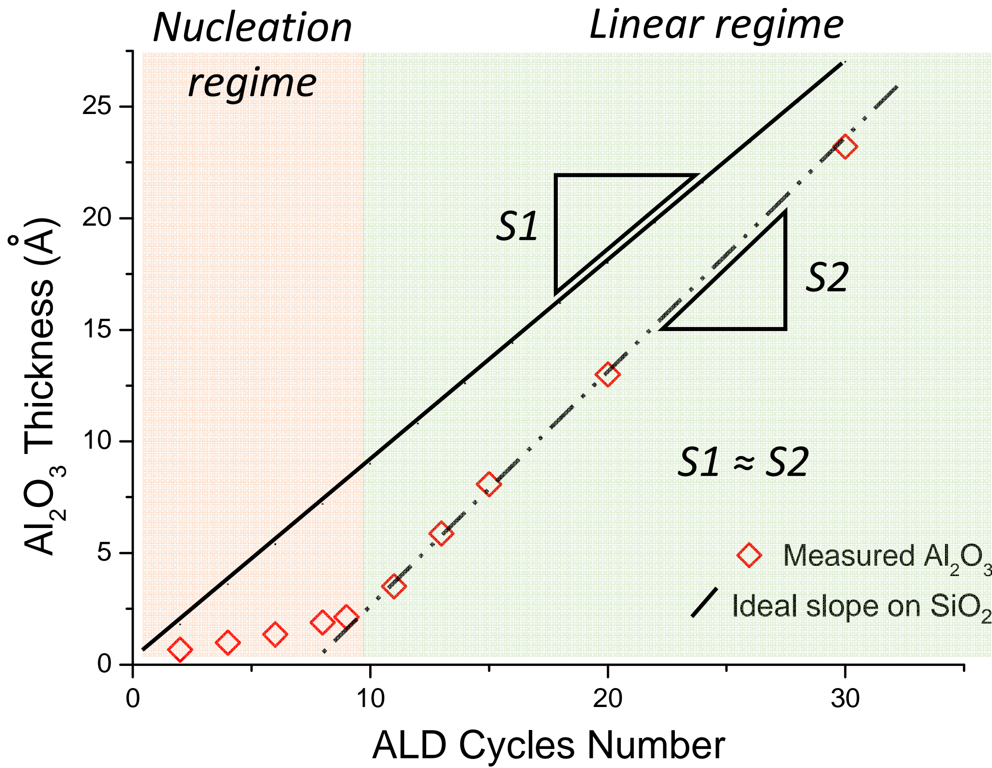


Figure III-10: Al_2O_3 thickness as a function of the number of ALD cycles on HF-cleaned surface.

It appears that similarly to HfO_2, the deposition of Al_2O_3 on HF-passivated Si suffers from a delay of nucleation compared to a growth on SiO_2. Additionally, the growth rate obtained after this nucleation regime is close to the ideal one obtained on SiO_2, here around 1 Å per cycle. Depositions of 4, 8, 12, 16,

18 and 22 cycles were performed in order to obtain Al_2O_3 layers between 0 and 15 Å (thickness range similar to the HfO_2 experiment).

Using ARXPS, the substrate oxide regrowth thickness induced by ALD was also evaluated. This measurement was performed after ALD Al_2O_3 deposition on both thin SiO_2 and HF-last passivated Si. The former being used as a reference case was obtained using a chemical cleaning designed to produce an 8 Å thick substrate oxide. Figure III-11 gathers these results.

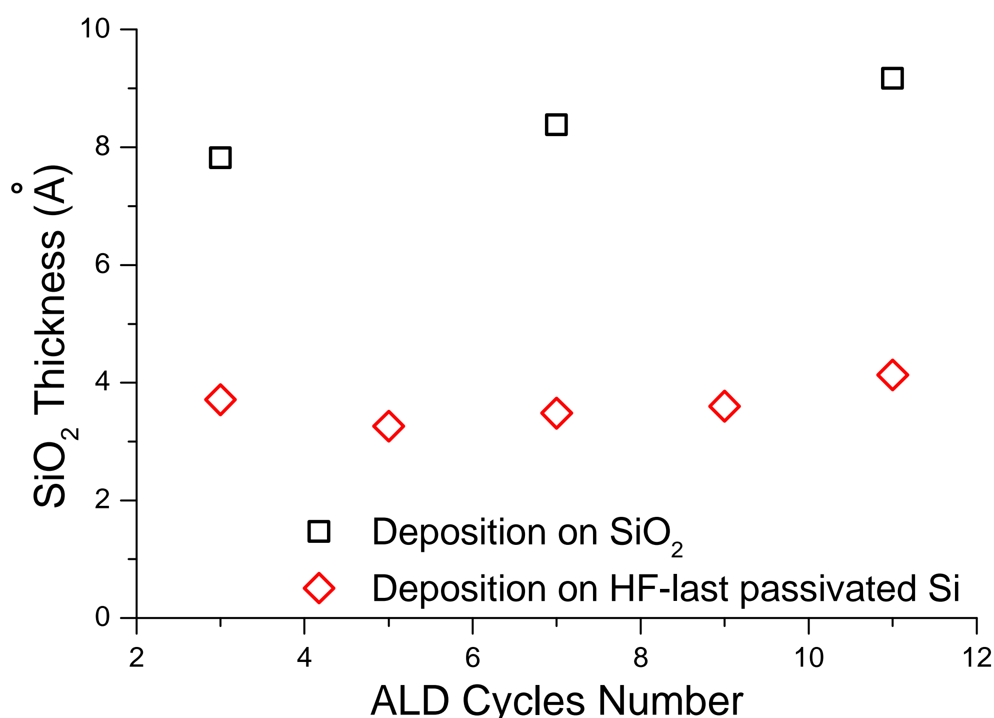


Figure III-11: Substrate oxide thickness measured by ARXPS after ALD deposition on SiO_2 or HF-last passivated Si.

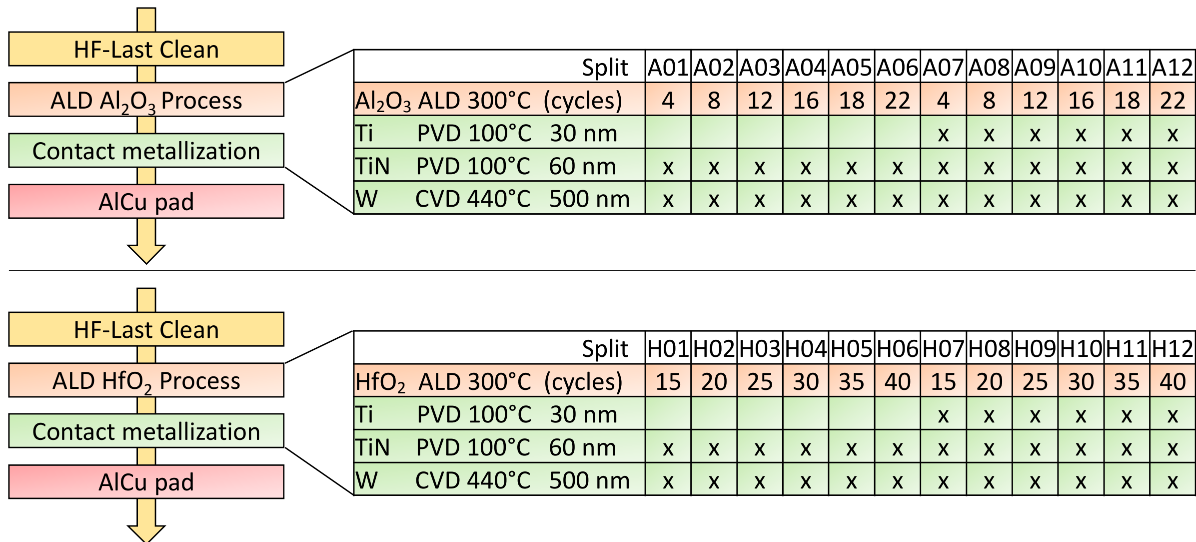
It appears that measurements on the SiO_2 reference case are consistent with the expected value of 8 Å. Nevertheless, this thickness seems to increase with the number of ALD cycles. This observation is in disagreement with [*Damlencourt_2003*] in which the thickness of SiO_2 was found insensitive to the deposition of Al_2O_3 by ALD.

On the HF-passivated surface, similarly to [*Franck_2003*], it was found that ALD deposition of Al_2O_3 using TMA/H_2O at 300°C leads to a SiO_2 thickness around 4 Å. This value was observed even for a low number of ALD cycles and appeared stable over the range of deposited Al_2O_3 thickness. Although this value seems low, as mentioned in the introduction, such a layer could theoretically leads to a huge degradation of performance.

❖ Process flow

In this part, the description of the process begins at the entrance of the contact module for the sake of simplicity. Nevertheless, to make electrical characterizations of the resulting contacts possible, wafers also underwent modules of implantations and test structures patterning.

Including the number of cycles determined in the preliminary study, samples based on the process flow presented in Figure III-12 were fabricated.



Split	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12
Al_2O_3 ALD 300°C (cycles)	4	8	12	16	18	22	4	8	12	16	18	22
Ti PVD 100°C 30 nm							x	x	x	x	x	x
TiN PVD 100°C 60 nm	x	x	x	x	x	x	x	x	x	x	x	x
W CVD 440°C 500 nm	x	x	x	x	x	x	x	x	x	x	x	x

Split	H01	H02	H03	H04	H05	H06	H07	H08	H09	H10	H11	H12
HfO_2 ALD 300°C (cycles)	15	20	25	30	35	40	15	20	25	30	35	40
Ti PVD 100°C 30 nm							x	x	x	x	x	x
TiN PVD 100°C 60 nm	x	x	x	x	x	x	x	x	x	x	x	x
W CVD 440°C 500 nm	x	x	x	x	x	x	x	x	x	x	x	x

Figure III-12: Process flow of the Al_2O_3 and HfO_2 MIS contact module.

HF-last passivation was considered as the required cleaning of the Si surface before dielectric deposition and the queue time between these two steps was kept under 4 hours. ALD deposition was performed at 300°C for both Al_2O_3 and HfO_2.

On some wafers presenting a low number of ALD cycles, the thickness of the dielectric was close to the monoatomic layer. It was thus expected that such a thin layer was not able to act as an efficient barrier for the oxygen contained in the ambient air. Therefore, the queue time between the deposition of the dielectric and that of the metal was also kept below 4 hours in order not to limit the air exposure of the high-k/Si stack.

Since TiN/Ti has been the classical metallization in microelectronics for 30 years [Maeda_1987] and aiming at addressing a system close to the industrial requirements, the same metal was chosen as the top electrode of the MIS contact. However, as presented in Table III-1, Ti is expected to enhance the pumping of the dielectric insertion oxygen. In order to evaluate the impact of such a layer, stacks with and without Ti layers were implemented as detailed in Figure III-12.

No annealing was intentionally applied to the MIS contacts. Nevertheless, some steps require relatively high process temperature. This is the case of the CVD deposition of W which has to be

performed at 440°C. Considering the thermally activated problems mentioned in the introduction, namely the substrate re-oxidation and the scavenging of the dielectric by the top metal, such an annealing may have a significant impact on the resulting spatial distribution of the elements.

In order to probe the actual distribution of the elements, observations of the resulting stacks were performed. The main characterization tool was the Scanning Transmission Electron Microscope (STEM) presenting High-Angle Annular Dark-Field (HAADF) and Electron Energy Loss Spectroscopy (EELS) detectors. TOF-SIMS was also used to perform depth profiling of the elements in presence.

❖ Al_2O_3 based MIS contacts

- *Impact of the Ti layer*

Aiming at probing the samples during their process of fabrication, wafers were taken out of the clean room to perform STEM-HAADF observations. This characterization was performed just before the deposition of W which can be considered as the only process step at high temperature (440°C). Observations were performed on A06 and A12 i.e. Al_2O_3 based MIS contacts respectively without and with Ti layer. Thus it was possible to evaluate the impact of this layer on samples before any thermal budget was applied. The resulting observations are presented in Figure III-13.

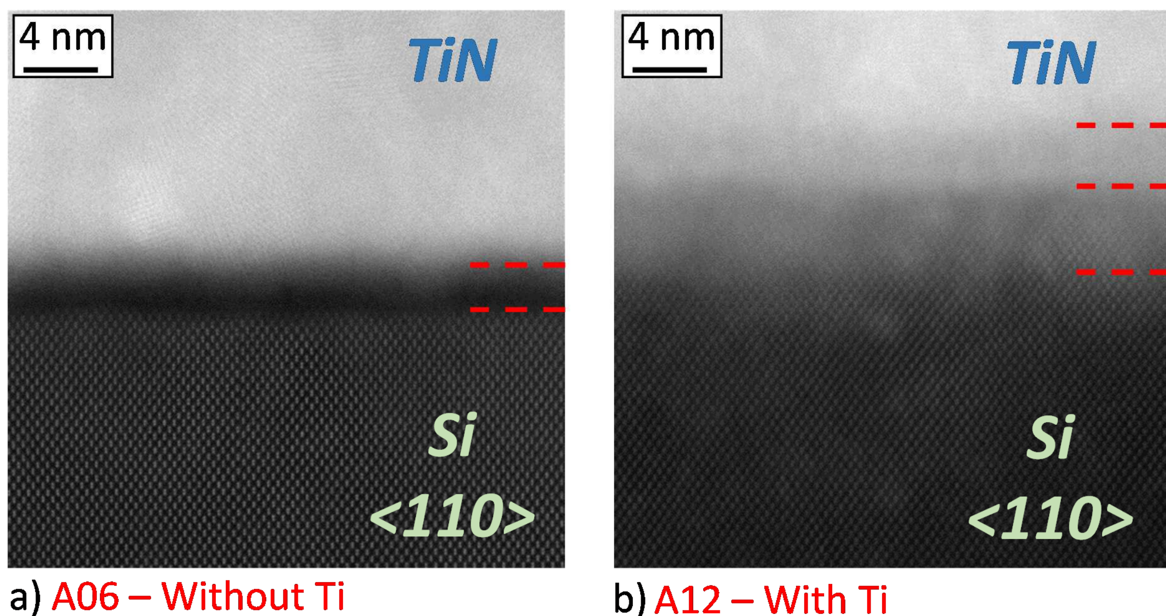


Figure III-13: STEM-HAADF observation of (a) A06 and (b) A12 i.e. Al_2O_3 based contacts resp. without and with Ti.

In STEM-HAADF images, the contrasts are the opposite of the ones of conventional microscopy. Thus the darkest areas can be attributed to the lightest elements or to the least dense layers. Then, it is

often considered as a signature of oxide layers. As shown in Figure III-13 of A06, a sharp dark separation between the Si (arranged layer at the bottom) and the TiN (lighter textured layer at the top) is observed. This layer is assumed to be the Al_2O_3 insertion. Comparatively, in sample A12, no neat boundary is observed and the cross-over from the Si to the TiN is composed of two layers presenting a gradient of shades of grey.

TOF-SIMS profiles were also acquired for these samples in order to find the composition of the different stacks. For the sake of simplicity, only the distribution of Al, O and Si are shown in Figure III-14. While, its part (a) displays the overlay of the A06 and A12 profiles, part (b) only features the Al- and O-components of A12.

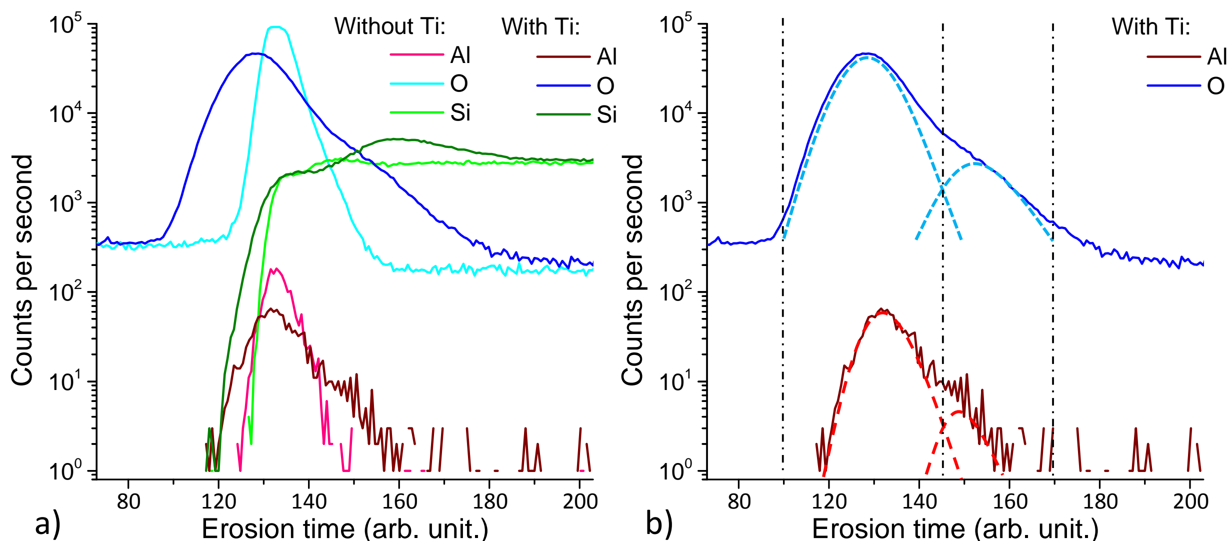


Figure III-14: (a) TOF-SIMS profiles of A06 and A12 i.e. resp. Al_2O_3 based MIS contacts without and with Ti and (b) basic deconvolution diagram of the Al and O components of the Ti-based sample TOF-SIMS profile.

As presented in Figure III-14 (a), TOF-SIMS profiles obtained with and without Ti feature significantly different Al- and O-components. In the case of sample A12, these elements exhibit peaks two times wider than A06 ones with lower maxima. It seems that these spectra can be both deconvoluted into two components having almost the same position as presented in Figure III-14 (b). Then it appears that the initial Al_2O_3 insertion can be separated into two regions.

The TOF-SIMS observations are in agreement with the STEM images. Both indicate that the presence of Ti in the stack induces the dilution of the initial Al_2O_3. The two regions arising from the

deconvolution of the Al- and O-components TOF-SIMS of A12 seem to be legitimately associated with the two layers observed in the STEM images and distinguished by looking at the shades of grey.

- *Impact of the annealing*

Similar observations were performed after the 440°C CVD W deposition in order to evaluate the impact of the thermal budget on the elements distribution. Comparison of the images taken before and after the W deposition is shown in Figure III-15.

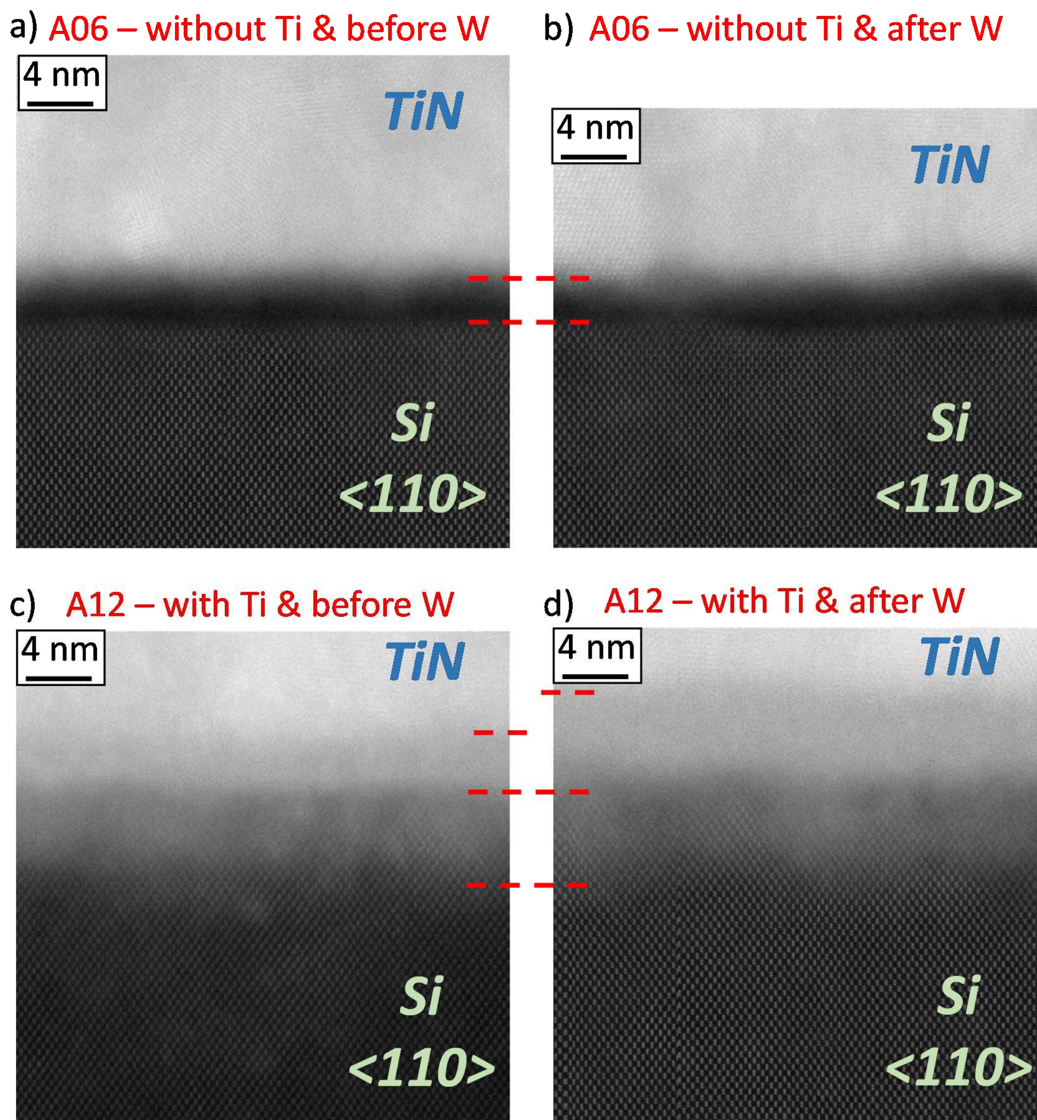


Figure III-15: STEM-HAADF observation of A06 and A12 before and after the 440°C CVD deposition of W.

The stack of A06 seems not modified by the annealing associated to W deposition and the dark region between the Si and Ti is attributed to the Al_2O_3 insertion. However, even though the pictures

corresponding to the A12 samples before and after the W deposition appear similar, the top transition region (at the left of the picture) appears thicker after this process step.

In order to have a more precise idea of the element distribution, the EELS detector was used to probe these 4 samples and the corresponding profiles are displayed in Figure III-16.

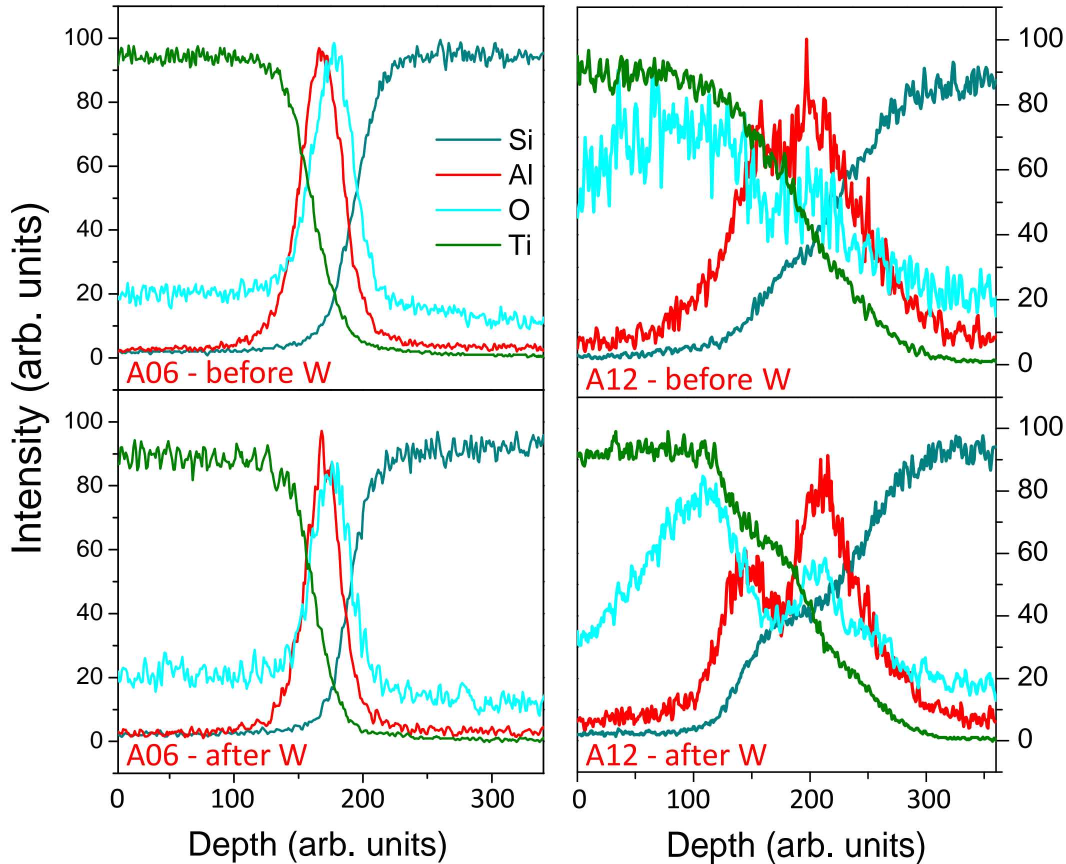


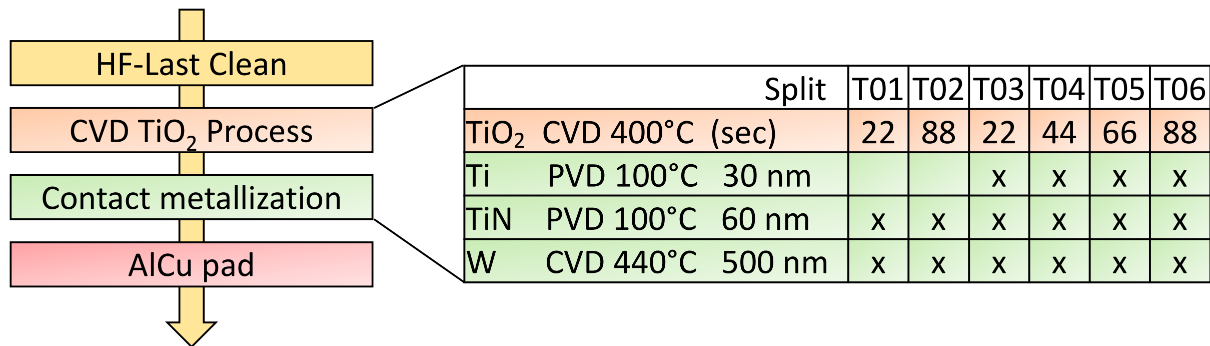
Figure III-16: EELS profiles of A06 and A12 before and after the 440°C CVD deposition of W.

As expected the EELS signal of the sample A06 is not altered by W deposition. Concerning sample A12, the ideal expected stack appears already modified by the deposition of Ti without having undergone the annealing of the W process step. However the EELS signal of A12 suggests that this 440°C annealing extends the evolution of the elements distribution in the case of a Ti capping. As observed in Figure III-16, the initial Al_2O_3 layer seems to result into two sub-layers. Plateaus featured by the Si and Ti signals imply that these sub-layers are ternary systems respectively composed of {Si, Al, O} and {Ti, Al, O}. Moreover the O-component of A12 after annealing spreads significantly over the Ti layer.

III.2.3 CVD based high-k implementation

❖ TiO2 based MIS contacts

In the case of TiO_2, the tunnel resistance induced by the dielectric is assumed to be lower than that of the two other dielectrics. Hence, the maximum thickness of TiO_2 was increased compared to Al_2O_3 and HfO_2. For the CVD-deposited TiO_2 used in this work, the growth rate was assumed to be around 1 Å per 3.66 s. Considering this value, thicknesses of 6, 12, 18 and 24 Å were targeted as displayed in Figure III-17.



Split	T01	T02	T03	T04	T05	T06
TiO_2 CVD 400°C (sec)	22	88	22	44	66	88
Ti PVD 100°C 30 nm			x	x	x	x
TiN PVD 100°C 60 nm	x	x	x	x	x	x
W CVD 440°C 500 nm	x	x	x	x	x	x

Figure III-17: Process flow of the TiO_2 MIS contact module.

Overall considerations about the process flow are similar to the ones presented in the ALD part. An HF-last clean was performed prior to the dielectric insertion disposition and the queue time between these two steps was kept below 4 hours. Titanium being expected to scavenge the insertion, wafers with and without Ti were implemented. However, since the destruction of the TiO_2 insertion by the Ti was already reported in [*Yu_2015*], the insertion stability was only evaluated on sample presenting a TiN metallization and only two wafers were implemented with Ti.

- *Insertion stability*

STEM-HAADF observation of T06 was executed just after the deposition of W. This sample presents TiN metallization and was thus expected to be stable. The resulting observations are presented in Figure III-18.

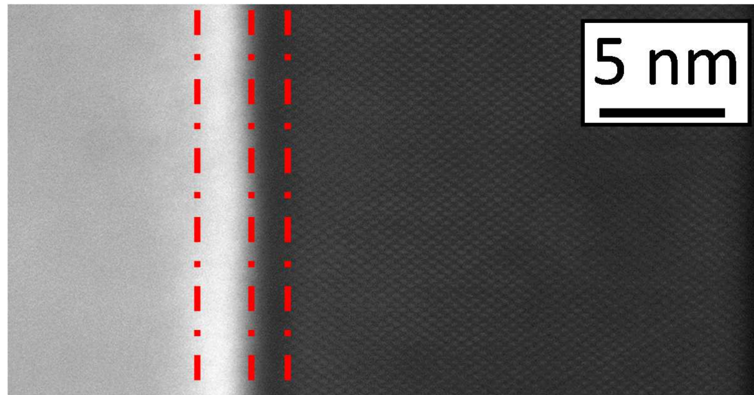


Figure III-18: STEM-HAADF observation of T06 after the 440°C CVD deposition of W.

This picture implies that the interface between TiN and Si can be divided into two different layers: a first one darker than Si and a second one lighter than TiN. In STEM-HAADF, a dark region being attributed to a layer with a low density, the region at the surface of Si could reasonably an oxide layer. In contrast, the region at the interface with TiN being light can be attributed to layer containing metal elements a lack of oxygen and nitrogen.

In order to have a more precise idea of the element distribution, EELS observations was performed on the sample T06 and are exposed in Figure III-19.

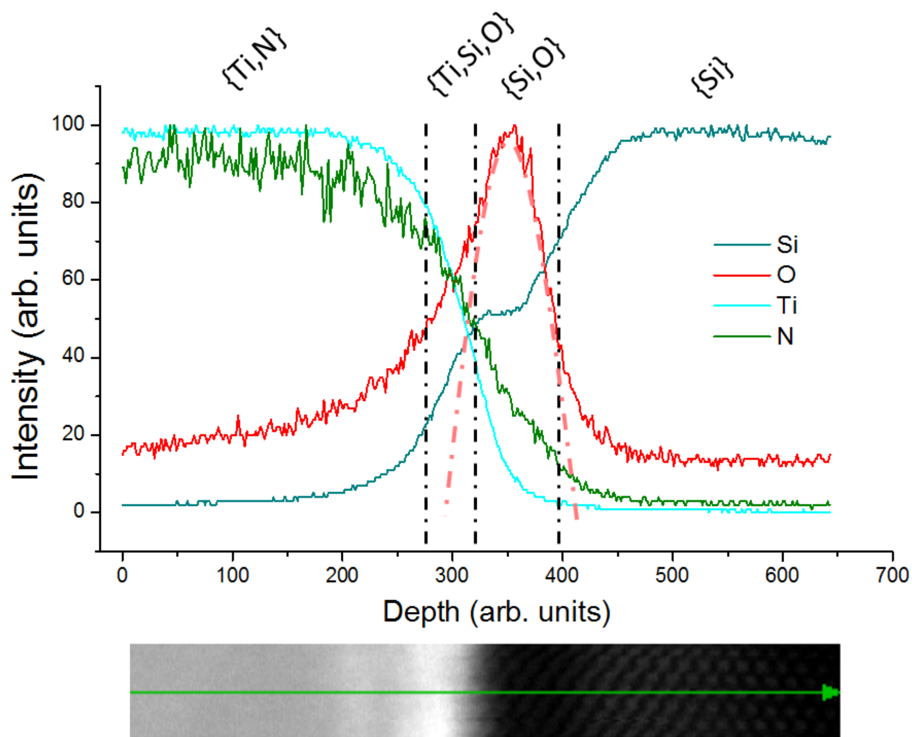


Figure III-19: EELS profiles of T06 after W deposition.

Surprisingly, the spectrum of Ti does not feature any shoulder in the region in which the TiO_2 layer was expected to be. However, the spectra of Si and O feature shapes which tend to indicate an important interface rearrangement. Indeed the O profile cannot be fitted by a single peak as it would be expected in the case of a well-defined TiO_2 layer but features a main peak and a shoulder. Interestingly, this main peak is shifted toward the Si and only the shoulder takes place at the interface with the Ti spectrum. Besides, the Si profile exhibits an important plateau in the interface region. The position of this plateau seems to match with the position of the main peak of the O profile. This suggests the formation of an important SiO_x layer on the surface of the substrate. Finally, the interface between the induced SiO_x and the TiN appears to be composed of Ti, Si and O.

III.3 Chapter conclusions

In Chapter III, dielectrics insertions for MIS contacts are studied through the prism of their practical implementation.

Trying to benefit from STMicroelectronics cleanroom environment, a first pragmatic implementation technique is presented. Based on the scavenging effect, i.e. pumping of oxygen by metal, this experiment aims at fabricating ultra-thin TiO_x layer while using only tools already used in production line. Nevertheless, it finally appears that even if TiO_x formation is thermodynamically favorable, the scavenging effect expected in a Ti/SiO_2 stack is not the prevalent one and other interactions lead to the creation of Ti-silicate layer.

Besides TiO_2, HfO_2 and Al_2O_3 implementations based on traditional deposition techniques are presented, namely, CVD and ALD. The redistribution of the constituent elements actually taking place in the MIS stacks are evaluated as a function of the top metal and the subsequent thermal budget undergone during the process flow. A particular attention is paid to the phenomena of substrate re-oxidation and insertion scavenging. These interactions are believed to be the main source of intermixing issues and MIS stack degradation.

To summarize, it appears that stable ultra-thin dielectric insertions are not easily achieved. Indeed, in this range of thickness, the interface phenomena become prevalent.

Working with the classical metallization used in the IC chips manufacturing industry, namely W/TiN/Ti, the presence of Ti at the vicinity of the dielectric insertion leads to its degradation (if using Al_2O_3 and TiO_2). Moreover, such a scavenging effect is enhanced by any subsequent thermal budget. Thus, being performed at 440°C, the deposition of W is found high enough to amplify elements redistribution through the stack. Even in the case of a low W deposition process, in a full CMOS process, wafers are also submitted to steps required to fabricate the metallic interconnections of metals. These steps are typically performed around 400°C. Then a MIS contact dedicated to CMOS industry should be unaltered by such thermal budget.

Additionally, as demonstrated in Chapter II, in order to enhance the performance of the MIS contacts, the polarity of the metal should match the one of the substrate. Thus in order to address n-type Si, metal with a workfunction even lower than that of Ti should be chosen (in Chapter II, Zr is used for the simulations). Known to be reactive [*Li_2015*], such metals might lead to a higher degradation of the dielectric.

Finally, as presented in the introduction and in the preliminary study of ALD based dielectrics, a regrowth of the substrate oxide seems unavoidable when working at 300°C on a H-passivated surface. This layer has undoubtedly a significant impact on the electrical transport and should be tackled. It appears from the state-of-the-art that such a regrowth reduction was obtained by either working at lower temperature or performing additional surface treatment. The former was achieved by Ho *et al.* [*Ho_2005*] who studied the deposition of HfO_2 using ultra-low temperature ALD i.e. 100°C (TEMAH/D_2O precursors). Using this process, high number of ALD cycles (up to 30) were achieved with no evidence of silicon oxide interfacial layer. The latter was investigated by Damlencourt *et al.* [*Damlencourt_2003*] who performed Cl_2 treatment between the HF-passivation and the dielectric deposition. Doing so, the resulting stacks were found to feature only a 0.26 nm SiO_x regrowth which only corresponds to the bonding length between Si and O.

In the next chapter, the electrical properties of these resulting stacks will be evaluated. Potential deviations from performance predicted by the theory and the simulation will be analyzed and linked to the parasitic chemical interactions presented in Chapter III.

III.4 References

Abraham_1974 **F. F. Abraham**; *Homogeneous nucleation theory; the pretransition theory of vapor condensation*; New York, Academic Press; 1974

Alcock_2000 **C. B. Alcock**; *Thermochemical Processes: Principles and Models*; Butterworth-Heinemann Editions; 2000

Ando_2009 **T. Ando, M. M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber, A. Callegari, D. Lacey, S. Brown, Q. Yang, and V. Narayanan**; *Understanding Mobility Mechanisms in Extremely Scaled HfO_2 (EOT 0.42 nm) Using Remote Interfacial Layer Scavenging Technique and Vt-tuning Dipoles with Gate-First Process*; IEEE International Electron Devices Meeting; 2009

Baur_1977 **W. H. Baur**; *Silicon-Oxygen Bond Lengths, Bridging Angles Si-O--Si and Synthetic Low Tridymite*; Acta Cryst. B33; 1977

Butz_1983 **R. Butz, G. W. Rubloff and P. S. Ho**; *Chemical bonding and reactions at Ti/Si and Ti/Oxygen/Si interfaces*; Journal of Vacuum Science & Technology A, Vol. 1; 1983

Chabal_1989 **Y. J. Chabal, G. S. Higashi, K. Raghavachari and V. A. Burrows**; *Infrared spectroscopy of Si(111) and Si(100) surfaces after HF treatment: Hydrogen termination and surface morphology*; Journal of Vacuum Science & Technology A, Vol. 7; 1989

Damlencourt_2003 **J. –F. Damlencourt, O. Renault, A. Chabli, F. Martin, F. Bedu, M.-N. Séméria**; *Surface treatment for high-quality Al2O3 and HfO2 layers deposited on HF-dipped surface by atomic layer deposition*; Journal of Materials Science: Materials in Electronics 14; 2003

Damlencourt_2005 **J. –F. Damlencourt, O. Renault, F. Martin, M.-N. Séméria, F. Bedu and T. Billon**; *Surface treatment for the atomic layer deposition of HfO_2 on silicon*; Applied Physics Letters, Vol. 86; 2005

Fick_1855 **A. Fick**; *On liquid diffusion*; Journal of Membrane Science, Vol. 100; German original 1855, re-published 1995

Franck_2003 **M. M. Franck and Y. Chabal**; *Nucleation and interface formation mechanisms in atomic layer deposition of gate oxides*; Applied Physics Letters, Vol. 82; 2003

Gibbs_1873 **J. W. Gibbs**; *A Method of Geometrical Representation of the Thermodynamic Properties of Substances by Means of Surfaces;* Transactions of the Connecticut Academy of Arts and Sciences, Vol. 2; 1873

Gilmer_1998 **D. C. Gilmer, D. G. Colombo, C. J. Taylor, J. Roberts, G. Haugstad, S. A. Campbell, H.- S. Kim, G. D. Wilk, M. A. Gribelyuk and W. L. Gladfelter**; *Low Temperature CVD of Crystalline Titanium Dioxide Films Using Tetranitratotitanium (IV)*; Chemical Vapor Deposition, Vol. 4; 1998

Gupta_2013 **S. Gupta, P. P. Manik, R. K. Mishra, A. Nainani, M. C. Abraham and S. Lodha;** *Contact resistivity reduction through interfacial layer doping in metal-interfacial layer-semiconductor contacts*; Journal of Applied Physics, Vol. 113; 2013

Humpston_2004 **G. Humpston and D. M. Jacobson**; *Principles of Soldering*; ASM International Editions; 2004

Klein_1999 **T. M. Klein, D. Niu, W. Li, D. M. Maher, C. C. Hobbs, R. I. Hegde, I. J. R. Baumvol, G. N. Parsons and W. S. Epling**; *Evidence of aluminum silicate formation during chemical vapor deposition of amorphous Al_2O_3 thin films on Si(100)*; Applied Physics Letters, Vol. 75; 1999

Li_2015 **Y. Li**; *Organic Optoelectronic Materials*; Springer; 2015

Lu_2000 **G. Lu, S. L. Bernasek and J. Schwartz** ; *Oxidation of a polycrystalline titanium surface by oxygen and water*; Surface Science, Vol. 458; 2000

Maeda_1987 **T. Maeda, T. Nakayama, S. Shima and J. Matsunaga**; *A Highly Reliable Interconnection for a BF_2^+ -Implanted Junction Utilizing a TiN/Ti Barrier Metal System*; IEEE Transactions on Electron Devices, Vol. 34; 1987

Mellor_1922 **J. W. Mellor**; *A Comprehensive Treatise on Inorganic and Theoretical Chemistry*; Vol. 1, Section Chemical Affinity, pp. 291-93, Longmans; 1922

Mende_1983 **G. Mende, J. Finster, D. Flamm and D. Schulze**; *Oxidation Of Etched Silicon In Air At Room Temperature; Measurements With Ultra-soft X-Ray Photoelectron Spectroscopy (ESCA) And Neutron Activation Analysis*; Surface Science 128; 1983

Oswald_2010 **S. Oswald**; *Growth studies of Ti-based films deposited on Si and SiO_2 using angle-resolved XPS*; Surface and Interface Analysis, Vol.42; 2010

Robertson_2002 **J. Robertson**; *Band structures and band offsets of high K dielectrics on Si*; Applied Surface Science, Vol. 190; 2002

Totten_2006 **G. E. Totten**; *Steel Heat Treatment: Metallurgy and Technologies*; 2nd edition, CRC Press Editions; 2006

Wagner_1979 **C. D. Wagner, W. M. Riggs, L. E. Davis, J. F. Moulder and G. E. Muilenberg**; *Handbook of x-ray photoelectron spectroscopy*; Perkin-Elmer Corporation; 1979

Yu_2015 **H. Yu, M. Schaekers, E. Rosseel, A. Peter, J.-G. Lee, W.-B. Song, S. Demuynck, T. Chiarella, L-Å.Ragnarsson, S. Kubicek, J. Everaert, N. Horiguchi, K. Barla, D. Kim, N. Collaert, A. V. -Y. Thean, K. De Meyer**; *1.5<10-9 W.cm^2 Contact Resistivity on Highly Doped Si:P Using Ge Pre-Amorphization and Ti Silicidation*; IEEE International Electron Devices Meeting; 2015

Chapter IV
Electrical characterization of MIS contacts

Introduction to Chapter IV 159
IV.1 Conventional contact characterization 160
IV.1.1 Specific contact resistivity 160
IV.1.2 Schottky barrier height 161
IV.2 Conventional test structures 163
IV.2.1 Back contact measurement 163
IV.2.2 Transmission Line Model (TLM) 167
IV.2.3 Cross Bridge Kelvin Resistor (CBKR) 171
IV.2.4 Summary of the section 177
IV.3 MIS contacts integration 178
IV.3.1 Substrate characteristics 178
IV.3.2 Dielectric characteristics 180
IV.3.3 Expected materials parameters 182
IV.3.4 Structures layout 182
IV.4 Experimental results 184
IV.4.1 TLM measurements 184
IV.4.2 CBKR measurements 190
IV.5 Discussions 202
IV.5.1 Obtaining contact signature I-V characteristics with CBKR 202
IV.5.2 The TiN/TiO_2/Si case 203
IV.6 Chapter conclusions 206
IV.7 References 208

Introduction to Chapter IV

In the previous chapter, MIS contacts incorporating various dielectrics were studied through the prism of the redistribution of their constituent elements. A particular attention was paid to the phenomena of substrate re-oxidation and insertion scavenging. These interactions were believed to be the main source of intermixing issues and MIS stack degradation.

In Chapter IV, the electrical properties of these resulting stacks are evaluated. In the two first parts, current techniques of characterization and the associated test structures are presented. Some important limitations are outlined. The third part presents the main information about integration, materials and structures required to perform the resistivity extraction. In the fourth part, electrical results of the MIS contacts implemented in this work are reported.

IV.1 Conventional contact characterization

When dealing with Metal/Semiconductor (MS) or Metal/Insulator/Semiconductor (MIS) contacts and trying to characterize them, several figures of merit can be considered. One of the most important is the resistance associated with the interface barrier and called the contact resistance. The magnitude of this resistance depends mostly on the doping concentration near the semiconductor surface and on the effective Schottky Barrier Height (SBH).

However in the case of a significant barrier height and/or a low doping concentration at the interface, the I-V characteristic of a given contact could actually turn out to be non-linear. Thus associating a resistance with such a contact is no longer relevant. In this case, measuring the effective SBH or generating the I-V characteristics allow to grasp the extent of the non-linearity and the amount of forward and reverse currents.

In this section, the main notions used in the state-of-the-art to characterize linear and non-linear contacts are introduced.

IV.1.1 Specific contact resistivity

As introduced in Chapter I, when dealing with the contact resistance R_c, the notion of contact resistivity ρ_c is often used in order to describe the electrical properties of a contact independently of its geometry. Thus, the nature of a contact interface can be defined by its resistivity and the resistance of an actual contact presenting this interface is assumed to be obtained by dividing the resistivity by the surface (Equation (IV-1)).

$$R_c = \frac{\rho_c}{W_c L_c} \tag{IV-1}$$

Experimentally, the notion of "specific" contact resistivity is often considered and defined according to Equation (IV-2) considering V as the bias across the contact and J the current density flowing through it [*Chang_1971*].

$$\rho_c = \left\{\frac{dJ}{dV}\right\}_{V=0}^{-1} \tag{IV-2}$$

Therefore, measuring the resistivity around zero volt gives the specific contact resistivity. If the contact is considered linear, this value is assumed to be consistent at any bias. The Schottky barrier height

being very difficult to extract properly, the specific contact resistivity is often preferred in the state-of-the-art as the figure of merit of choice to define the performance of contacts.

Nevertheless, in the case of a non-linear contact, SBH evaluation and I-V generation cannot be avoided.

IV.1.2 Schottky barrier height

For a long time, the current flowing in Schottky contacts has been attributed to Thermionic Emission (TE) [*Bethe_1942*]. According to this theory, the current is expressed as in Equation (IV-3).

$$I(V) = AA^{*}T^{2}\, exp\left(-\frac{q\Phi_{bn}^{eff}}{kT}\right).\left[exp\left(\frac{qV}{kT}\right)-1\right] \tag{IV-3}$$

Where A is the area of the contact, A^{*} is the Richardson constant, Φ_{bn}^{eff} is the effective SBH and V is the bias. Nevertheless, deviations from the ideal TE theory were observed and attributed to the phenomenon of image force lowering [*Sze_1964*].

In order to fit the experimental results with the TE theory, Equation (IV-3) was modified into Equation (IV-4) introducing a dimensionless parameter η called the ideality factor.

$$I(V) = AA^{*}T^{2}\, exp\left(-\frac{q\Phi_{bn}^{eff}}{kT}\right).\left[exp\left(\frac{qV}{\boldsymbol{\eta} kT}\right)-1\right] \tag{IV-4}$$

Taking the logarithm of the current in the forward regime ($V > 0$), one can obtain Equation (IV-5).

$$\ln I(V) = \ln AA^{*}T^{2} - \frac{q\Phi_{bn}^{eff}}{kT} + \frac{qV}{\eta kT} \tag{IV-5}$$

The ideality factor can thus be calculated using the slope of the straight line of the *ln I vs. V* characteristics. Doing so the ideality factor is expressed according to Equation (IV-6).

$$\eta = \frac{q}{kT}\left(\frac{d(\ln I)}{dV}\right)^{-1} \tag{IV-6}$$

Then, passing the logarithm of the square of the temperature in the left-hand side of Equation (IV-5) leads to Equation (IV-7) .

$$\ln\left(\frac{I_{sat}}{T^2}\right) = \ln AA^* - \frac{q\Phi_{bn}^{eff}}{kT} + \frac{qV}{\eta kT} \quad \text{(IV-7)}$$

Plotting this equation as a function of the inverse of the temperature allows to extract the Richardson constant A^* from the intercept and $\Phi_{bn}^{eff} - V$ from the slope. Such a plot is called a Richardson plot.

Therefore, one can see that there are two ways for characterizing a contact depending on its linearity. If the contact is linear thus only the specific resistivity is required to fully characterize the contact. However if the contact is not linear, more complex experiments have to be performed in order to generate the full I-V characteristics, thus allowing to extract Φ_{bn}^{eff} and η. Both methods require dedicated contact test structures.

IV.2 Conventional test structures

Several structures have reached over the years a general consensus and are often used to extract the specific contact resistivity or the SBH, or even to generate the I-V characteristics of the contacts. The main ones are presented in the following part and are introduced by order of complexity.

IV.2.1 Back contact measurement

❖ Principles

The back contact measurement is one of the simplest methods to implement since it requires only one step of photolithography. As shown in Figure IV-1, it is basically composed of the probed contact (MS or MIS), the substrate and a back contact.

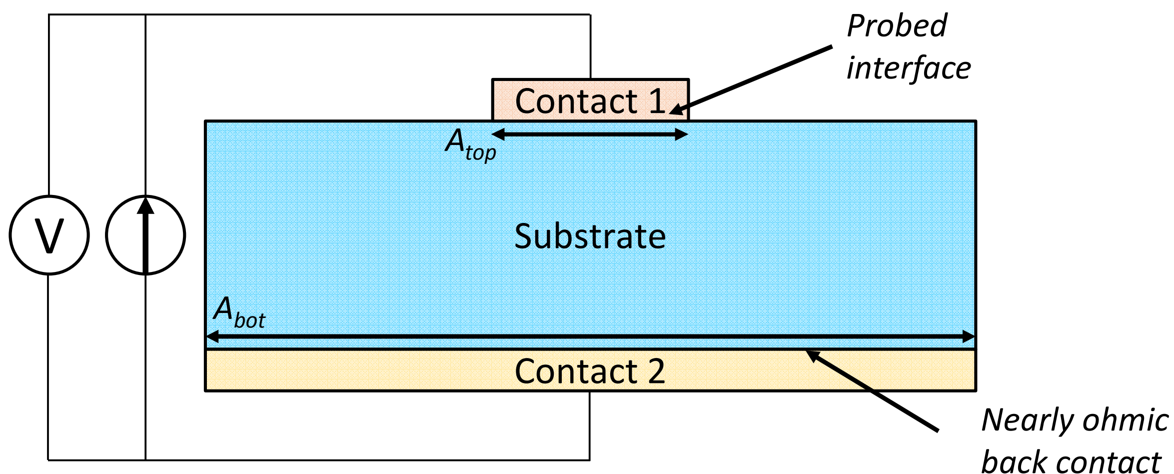


Figure IV-1: Schematic of a back contact measurement.

In order to measure a signal representative of the probed contact, its area A_{top} is small compared to that of the back contact A_{bot}. Additionally, the material composing the back contact is often chosen among the metals having shown in the past a nearly ohmic behavior on the semiconductor substrate.

This method is thus very simple to implement and is often used in the state-of-the-art to generate I-V characteristics. If the requirements presented previously are met, the generated signal is believed to be a signature of the probed contact. One of the most significant illustrations of the contact asymmetry study using the back contact measurement can be found in [*Nishimura_2008*] and is presented in Figure IV-2.

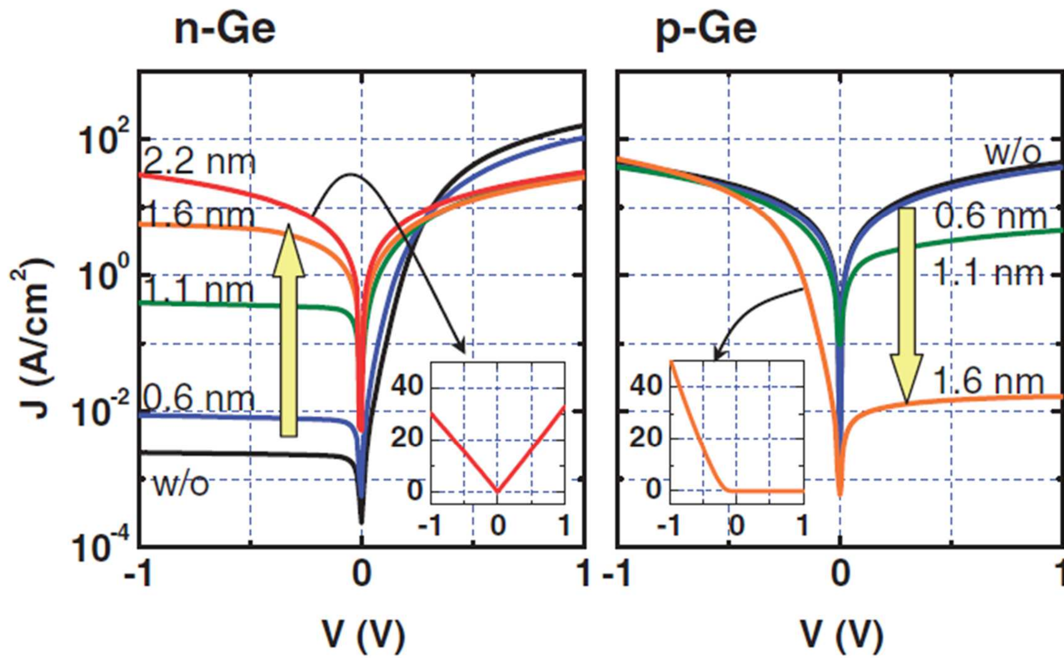


Figure IV-2: J–V characteristics of Al/GeO$_x$/Ge diodes taking from [Nishimura_2008].

In this figure, it appears that the reverse biased current increases on n-Ge and decreases on p-Ge when increasing the thickness of GeO$_x$ as indicated by the yellow arrows. Contacts on n-Ge presenting 2.2 nm of GeO$_x$ are eventually found linear and symmetrical (inset). Such MIS contacts could not have been defined just by associating them a value of resistivity around zero. Additionally, if varying the temperature, this method also allows extracting the ideality factor and the effective SBH using the Richardson plot.

❖ Issues

As powerful and simple as this method might seem, some discrepancies arise when looking at the measured forward saturation current density. Indeed, in Figure IV-2, the highest level of forward current injection is found around 10^2 A.cm^{-2} at 1 V. Using Ohm's law, this value could reasonably be attributed to a contact resistivity of 10^{-2} Ω.cm². It seems that a contact presenting such a poor contact resistivity can hardly be found linear. Whereas the former suggests a high SBH, the latter requires an ultra-low one. Some other studies, such as [*Manik_2012*], associated the same level of saturation current, 10^2 A.cm^{-2} at 1 V, with contact resistivities around 10^{-7} Ω.cm². These resistivities were obtained with other measurements structures and seem not to be consistent with the back contact measurement.

As first discussed by Norde [*Norde_1979*], such difficulties arise if the substrate materials present parasitic resistors comparable to the probed contact resistance.

In [*Werner_1988*], two main discrepancies were observed between an ideal diode behavior and its actual measured I-V characteristics: an enhanced reverse current and lowered forward one. Whereas Figure IV-3 (a) illustrates these discrepancies, Figure IV-3 (b) proposes an equivalent block diagram accounting for the modified levels of current. Both figures are adapted from [*Werner_1988*].

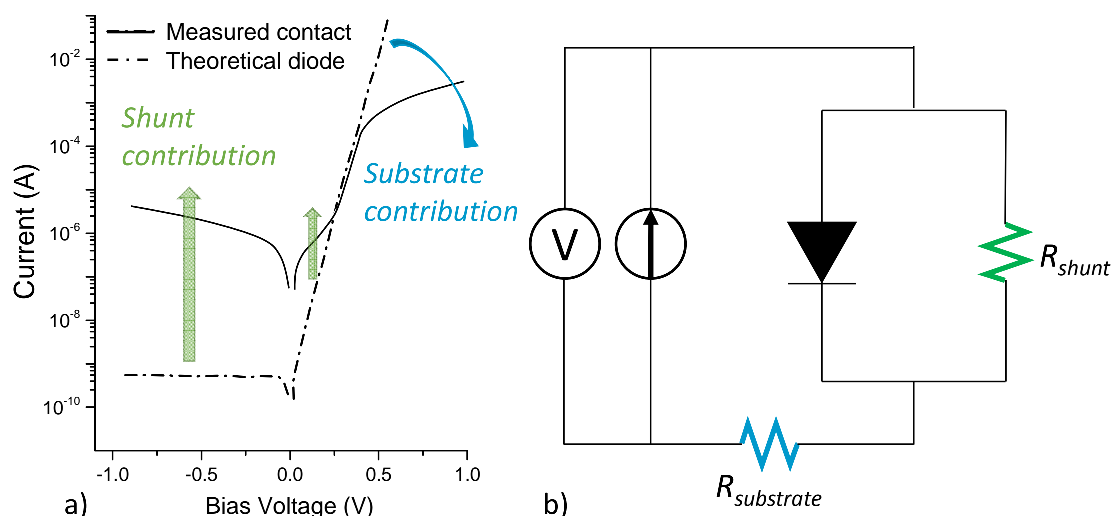


Figure IV-3: (a) Overlay of the theoretical Schottky contact I-V characterisitc and its actual measured one and (b) equivalent block diagram proposed in [Werner_1988] to encompass parasitic effects.

It can be seen from this study that the lowered current in the forward bias region seems to be legitimately attributed to the substrate contribution. However, in this study the reverse current enhancement was attributed to a shunt resistor. This shunt seems to be readily explicable by an actual electrical shunt in the structure. It seems however that this enhanced reverse current is due the transport occurring across the Schottky Barrier at the silicon surface. Since the model used to describe the theoretical diode electrical behavior leans on Thermionic Emission, such a reverse current is not taken into account.

In order to illustrate the discrepancies induced by the back contact method, simulations similar to the ones presented in Chapter II were performed. Contacts consisting of Ti/n-Si and Ti/TiO_2/n-Si were considered. To ensure the efficiency of the TiO_2 insertion at improving the contact resistance, a low doping concentration of $N_d=10^{18}$ at.cm^{-3} was considered.

Stand-alone contacts were first modelled and their I-V characteristics were simulated as if there was no external set-up. Thus the obtained characteristics were considered as intrinsic. These same contacts were then converted in SPICE compact models and plugged into a SPICE-simulated back contact structure. Their I-V characteristics were simulated in this configuration, thus encompassing the external set-up. Thus the obtained characteristics were considered as extrinsic. The results of both configurations are gathered in Figure IV-4.

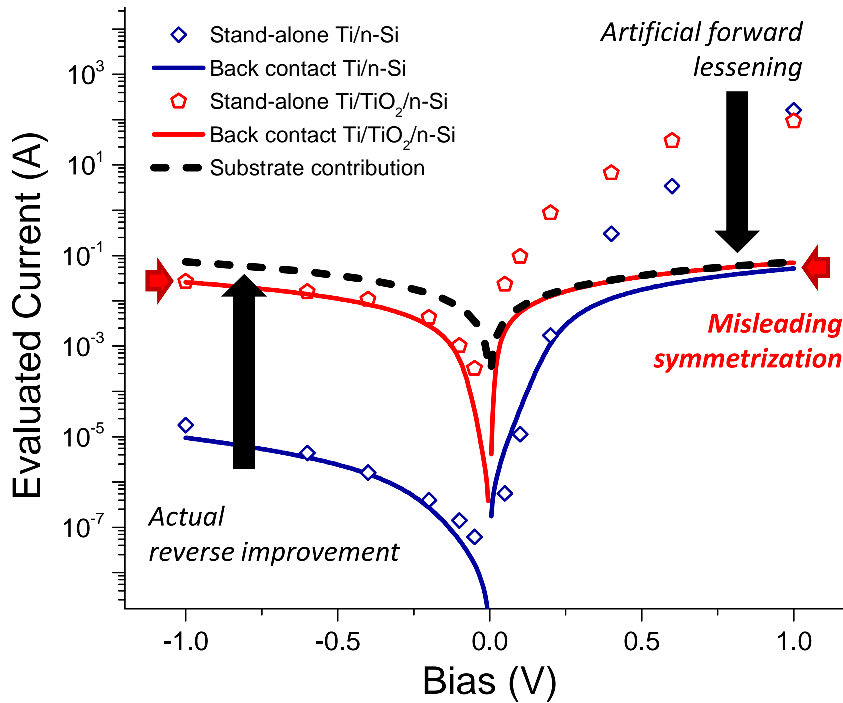


Figure IV-4: Comparison between I-V characteristics of stand-alone Ti/n-Si and Ti/TiO2/n-Si contacts and their corresponding curves measured in a back contact structure.

One can notice that the current is not impacted by the back contact set-up when looking at the reverse biases. However, it appears that the forward current of both contacts saturates around the same value when plugged in the back contact structure losing around 4 orders of magnitude. In Figure IV-4, the contribution of the substrate was added in dashed line. Its level of current in the forward biases region matches the value of saturation of the probed contacts. Thus it seems reasonable to conclude that for a large enough forward bias, the contacts become so conductive that the resistance of the substrate can no longer be neglected. In such a configuration, the measured I-V characteristics become more representative of the substrate than of the probed contacts.

This substrate contribution prevents from evaluating properly the forward current of both contacts and leads to a contact asymmetry undervaluation. Indeed, in the case of a Ti/TiO_2/n-Si contacts, the I-V

appears symmetrical when measured with the back contact while it is actually not the case. Therefore, even if introducing a dielectric layer truly improves the contact symmetry by increasing the reverse current, the measured I-V characteristics could not be interpreted as an evidence of a transition from Schottky to Ohmic behavior.

IV.2.2 Transmission Line Model (TLM)

❖ Principles

Developed by Berger [*Berger 1972*], this method is the most used technique in the state-of-the-art and thus it benefits from a lot of technical documentation.

Essentially, the experimental set-up consists of a series of contacts presenting the configuration one wants to probe, spaced from each other with an increasing pitch (Figure IV-5).

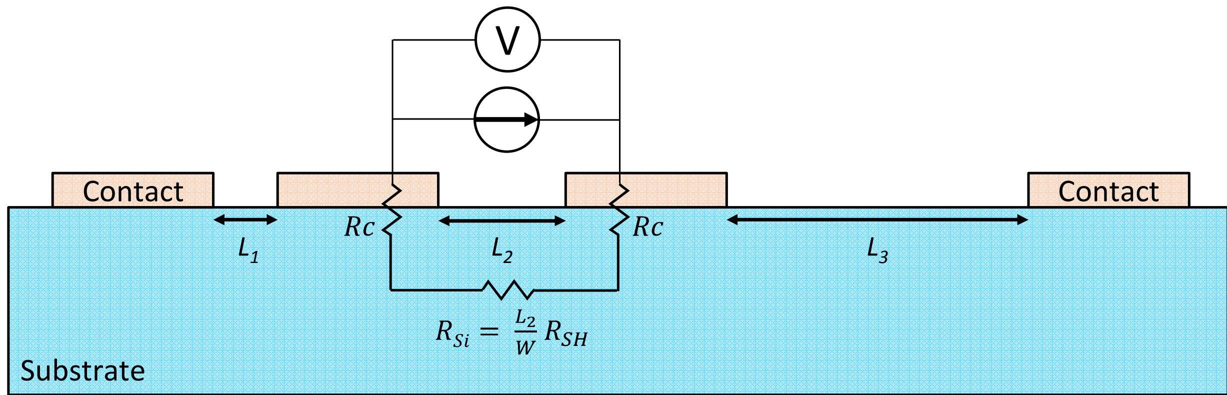


Figure IV-5: Cross section of the TLM measurement. The pitch between two consecutive contacts is not constant.

In such a configuration, at a given length L_i, the measured resistance is given by Equation (IV-8).

$$R_T(L_i) = 2R_C + \frac{L_i}{W} R_{SH} \qquad \text{(IV-8)}$$

Where R_C is the contact resistance one wants to probe, W is the width of the active area and R_{SH} is its sheet resistance in Ohm/□. Thus performing this measurement for each different length allows to plot the total resistance R_T as a function of the space between contacts as in Figure IV-6.

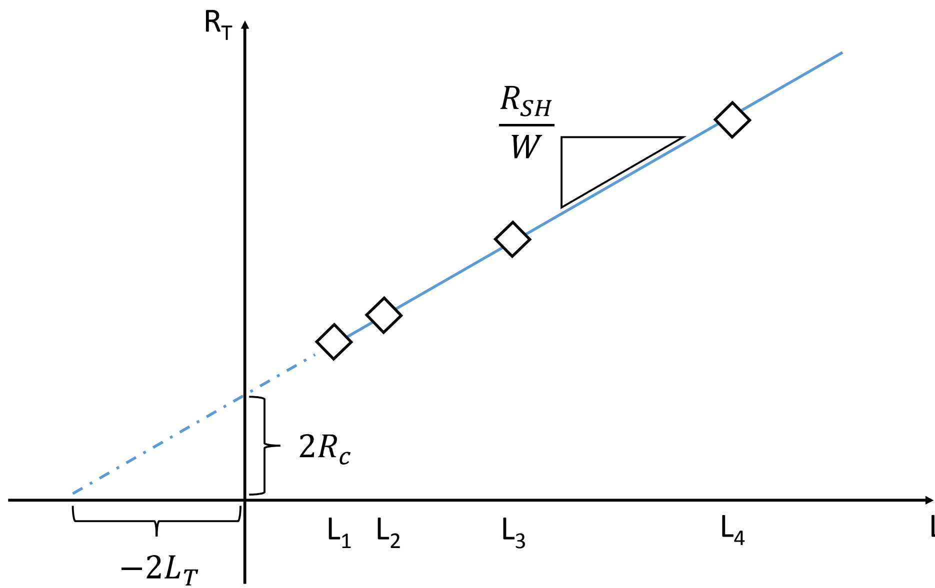


Figure IV-6: Schematic of a R_T versus L characteristics obtained from a TLM measurement. R_{SH}, R_c and L_T are shown on the plot.

Finally, extrapolating the intercept of the curve at *L* equal *0* gives a total resistance equal to twice the contact resistance.

Nevertheless passing from the contact resistance to its resistivity is not as trivial as dividing it by the area of the contact. Indeed as presented in Figure IV-7 (a), the region under the contact can be modelled by a transmission line [*Berger 1972*] (hence the name of transmission line model).

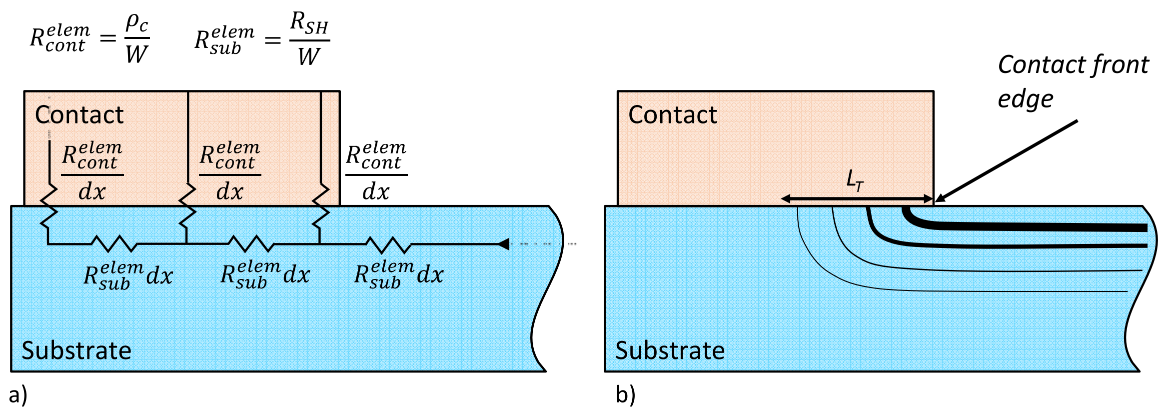


Figure IV-7: Cross section of the region under the contact presenting (a) the equivalent transmission line electric block diagram and (b) a scheme of the current line. The thickness of the lines represents the magnitude of the current density.

In this model, the substrate and the contact surface are divided in elementary segments of length *dx* and width *W*. Each of these elementary substrate and contact portions presents a resistance per length

unit respectively equal to R_{sub}^{elem} and R_{cont}^{elem}. Thus the current flowing toward the contact sees several available paths of conduction. As illustrated in Figure IV-7 (b), following the path of least resistance the current does not flow uniformly in the contact. The current distribution depends on both the sheet resistance of the substrate and the contact resistivity.

If the elementary contribution of the contact is high compared to that of the substrate, then the current will tend to maximize the surface it takes to cross the contact. In extreme cases, the whole surface of the contact is used to propagate the current and the contact resistivity can be found using Equation (IV-9). This configuration is called the electrically short contact limit case.

$$\rho_c = R_c W L_c \tag{IV-9}$$

Inversely, if the elementary contribution of the substrate is high compared to that of the contact, then the current has the tendency to cross the contact interface as close to the contact front edge as possible (Figure IV-7). In this case, the current avoids propagating in the substrate, the density is significant at the front edge of the contact whereas it is negligible at its far edge. In this case, only a portion of the contact is used to propagate the current. The characteristic length in which the current is spread is called the transfer length and is noted L_T. Its definition can be found in Equation (IV-10).

$$L_T = \sqrt{\frac{\rho_c}{R_{SH}}} \tag{IV-10}$$

Experimentally the transfer length can be obtained by extrapolating the intercept of the plotted curve at R_T equal *0* as show in Figure IV-6. Thus the resistivity can be found using Equation (IV-11) and this configuration is called electrically long contact limit case.

$$\rho_c = R_c W L_T \tag{IV-11}$$

In intermediate cases, it can be shown [*Berger_1972*] that the link between the contact resistance and resistivity is expressed by Equation (IV-12).

$$\rho_c = R_c W L_T \tanh\left(\frac{L_c}{L_T}\right) \tag{IV-12}$$

Considering the Taylor series of the hyperbolic tangent, this latest expression accounts for both extreme cases of long and short contact.

From combining Equations (IV-10) and (IV-12), Equation (IV-13) is obtained.

$$\rho_c = R_c W \sqrt{\frac{\rho_c}{R_{SH}}} \tanh\left(L_c \sqrt{\frac{R_{SH}}{\rho_c}} \right) \tag{IV-13}$$

This equation appears to be transcendental and thus cannot be solved easily. Thus it is worth noting that one of the major interests of the TLM method is to allow the evaluation of the transfer length, the sheet resistance and the contact resistance experimentally with almost no ex ante assumption. Knowing these physical values, Equation (IV-12) can used directly.

❖ Issues

First, in some cases, the sheet resistance of the semiconductor layer directly beneath the contact can be modified. For example, such an alteration might be brought by the alloying at the metal-semiconductor interface.

In that case, Figure IV-6 is no longer true and a new model is required [*Reeves_1982*]. According to this model, the transfer length in no longer found using Equation (IV-10) but Equation (IV-14).

$$L_T = \sqrt{\frac{\rho_c}{R_{SK}}} \tag{IV-14}$$

where R_{SK} is the sheet resistance beneath the contact.

In order to address this phenomenon, an additional measurement called "end resistance measurement" should be performed and can be found in [*Reeves_1982*]. In this work, such refinement is not considered since the alloy formation in MIS contacts is expected to be negligible.

Moreover, working with alloyed contacts on III-V, it has been showed in [*Ghegin_2016*] that using the end resistance measurement could lead to inconsistent results such as negative contact resistances.

Besides, as powerful as this method may be, it does not enable to characterize a non-linear contact. Indeed, this method relies on the assumption that the contact resistance is constant. Thus only the contribution of the substrate changes when switching from one spacing to another one. Nevertheless in

the case of a non-linear contact, its resistance varies with the bias applied to the contact. Thus when increasing the spacing, both the voltage drop in the substrate and the contact bias are changing.

Additionally, trying to divert the TLM setup to obtain an I-V signature of the contact is limited. Indeed as presented in Figure IV-8, working at one given spacing results in having two identical diodes in series.

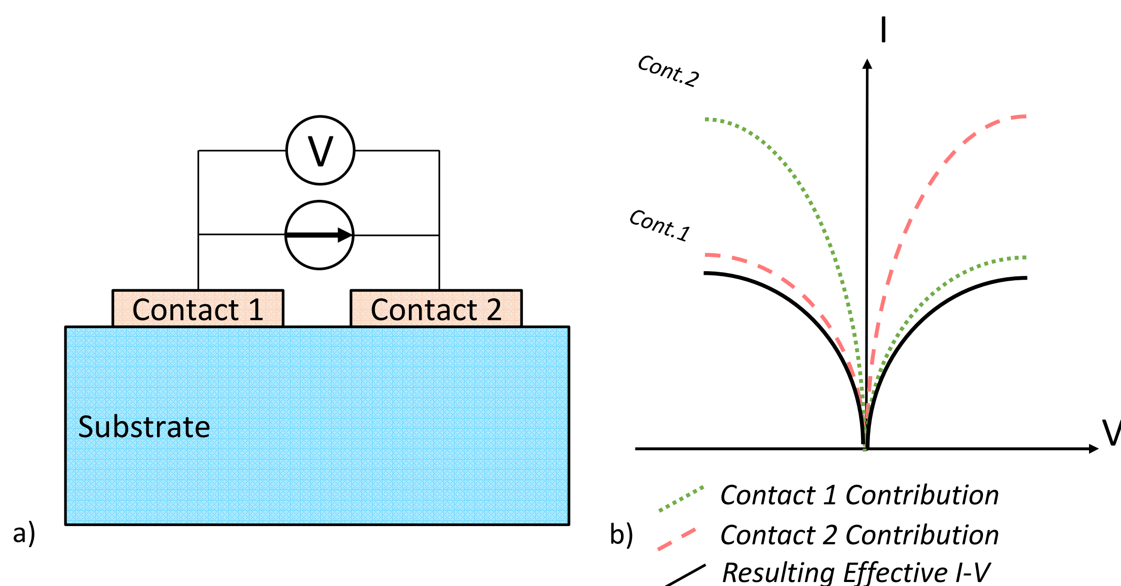


Figure IV-8: (a) Schematic of the TLM measurement on two consecutive pads and (b) sketch of the corresponding I-V characteristics.

In this configuration, the signal is always limited by the diode biased in its reverse regime. Thus, neither the full I-V characteristic of the probed contact nor an information on its asymmetry can be found using this set up.

However, as presented in [*Dubois_2004*], fitting FE, TFE and TE models on the experimental reverse dominated current of this back-to-back configuration allows to extract information about the SBH at the interface.

IV.2.3 Cross Bridge Kelvin Resistor (CBKR)

❖ Principles

Introduced by Proctor *et al.* in 1983 [*Proctor_1983*], the Cross Bridge Kelvin Resistor is the most complicated structure presented in this work.

As shown in Figure IV-9, it cannot be explained by only looking at a cross section but requires 3-D plotting in order to grasp its complexity. Since it is composed of an arm of metallic interconnection

and another of semiconductor separated by a vertical plug, this structure requires at least 3 levels of photolithography.

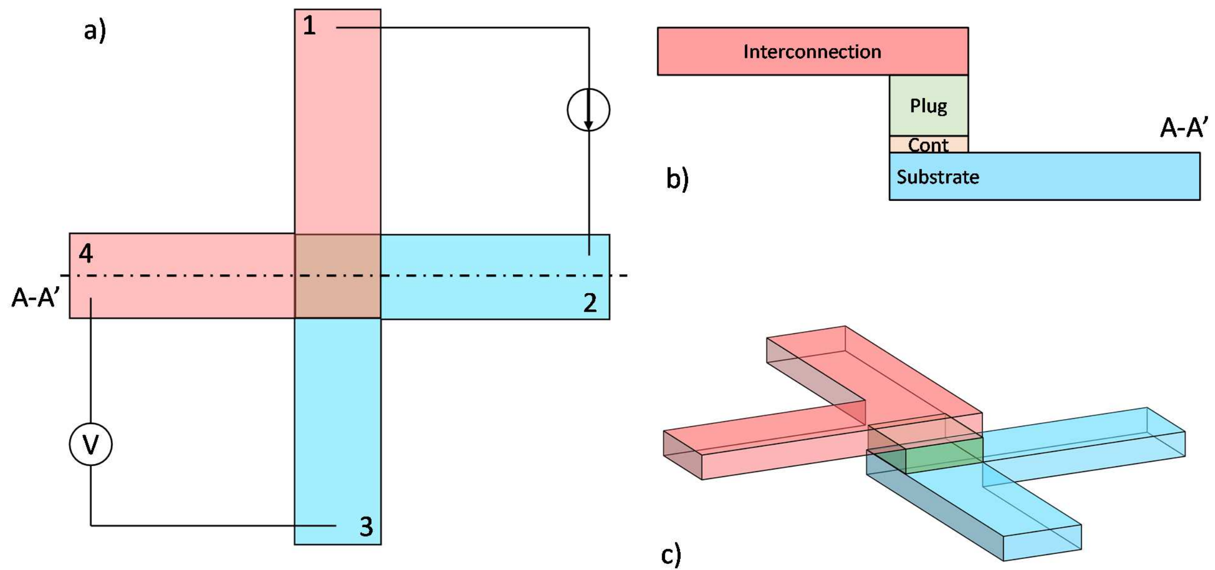


Figure IV-9: (a) Schematic top view of a CBKR structure, (b) cross-section of this structure along the A-A' direction and (c) 3-D view of the CBKR.

The measurement consists in forcing a known current from the semiconductor branch 2 to the metal branch 1 while the voltage is measured between the semiconductor branch 3 and the metal branch 4. In theory and providing that the input resistance of the voltmeter is infinite, only the voltage drop occurring in the central vertical part is actually evaluated and the parasitic resistances of the different branches are not sensed by the measurement. Moreover, the plug being made of metal, its resistance can be neglected compared to the contact resistance [*Proctor_1983*]. Thus the measured resistance R_k is directly assimilated to the contact resistance. In this simple model, called zero dimensional or 0-D, the resistivity can be obtained using Equation (IV-15).

$$R_k = \frac{V_{34}}{I} = \frac{\rho_c}{{L_c}^2} \tag{IV-15}$$

❖ Data treatment

Although the CBKR measurement allows to screen the contribution of the different branches of its structure, the data should not be treated as simply as in the 0-D model. Indeed, whereas it is not always the case, the contact window is considered perfectly aligned with the edges of the top and bottom layers. Moreover, in this model, the current is considered as uniformly spread along the contact.

Therefore, when treating the extracted data so simply, the CBKR-evaluated contact resistivity is often found very different from the ones extracted on the same system but using different structures (TLM for example). Typically, using the 0-D model to treat CBKR data suffers from a lack of accuracy for contact resistivity below 10^{-6} Ω.cm² [*Finetti_1984*]. More complicated models were thus studied and are presented in the following.

- *One-dimensional model (1-D)*

Two main refinements are introduced by the 1-D model. As discussed in the TLM part (IV.2.2), the current does not flow uniformly from the semiconductor to the contact. Besides, a significant underlapped region can be present between the contact and the semiconductor underlying layer represented by δ in Figure IV-10. To account for these major differences from the ideal case, the region under the contact can be modelled by a transmission line block diagram as presented in Figure IV-7. Proposed initially in [*Berger_1972*] to treat the TLM structure, this equivalent block diagram was extended to the CBKR structure by Loh *et al.* [*Loh_1987*].

Considering the position reference presented in Figure IV-10, the potential along the line between *0* and L_c is expressed by Equation (IV-16).

$$V(x) = V_k \frac{\cosh(\frac{x}{L_T})}{\cosh(\frac{L_c}{L_T})} \qquad \text{(IV-16)}$$

where V_k is the total potential dropped across the contact.

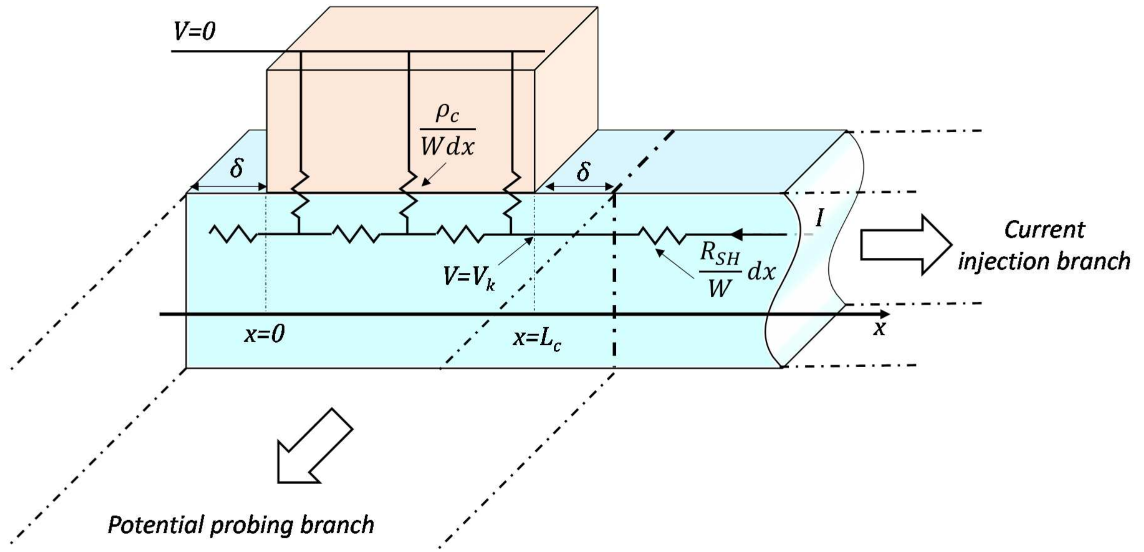


Figure IV-10: Cross-section of the CBKR structure superposed with the one-dimensional transmission line model approximation. The origins of position and electrical potential are also represented.

Thus when probing the voltage drop with the dedicated semiconductor branch, one does not only measure the contact potential V_k but the average potential in this branch over the *range [-δ ; L_c + δ]*. This problem was addressed by Ono *et al.* [*Ono_2002*] who considered the sharing of the potential in the probing branch as expressed in Equations (IV-17), (IV-18) and (IV-19).

$$V(x) = V_k \frac{1}{\cosh(\frac{L_c}{L_T})} \qquad -\delta \leq x \leq 0 \qquad \text{(IV-17)}$$

$$V(x) = V_k \frac{\cosh(\frac{x}{L_T})}{\cosh(\frac{L_c}{L_T})} \qquad 0 \leq x \leq L_c \qquad \text{(IV-18)}$$

$$V(x) = V_k[1 + L_T \tanh\left(\frac{L_c}{L_T}\right)(x - L_c)] \qquad L_c \leq x \leq L_c + \delta \qquad \text{(IV-19)}$$

The current flowing across the contact can thus be expressed as a function of the potential drop across it in Equation (IV-20).

$$I = V_k \frac{W L_T}{\rho_c} \tanh\left(\frac{L_c}{L_T}\right) \tag{IV-20}$$

Therefore, integrating the potential along the probing branch and dividing this average potential by the injected current gives an expression of the measured resistance R_k as a function of the geometrical parameters (Equation (IV-21)).

$$R_k = \frac{\rho_c + L_T R_{sh} \coth\left(\frac{L_c}{L_T}\right) \delta + \frac{R_{sh}}{2} \delta^2 + L_T R_{sh} \frac{1}{\sinh\left(\frac{L_c}{L_T}\right)} \delta}{(L_c + 2\delta) W} \tag{IV-21}$$

One can see from this expression that the measured resistance includes the contact resistance but also the geometrical effect resulting from the misalignment margin between the edges of the contact and the underlying layer.

- *Two-dimensional model (2-D)*

In the 1-D model, the only considered margin is the one along the x-axis as defined in Figure IV-10. Nevertheless, CBKR measurement suffers from a parasitic effect called “lateral current crowding” which may also strongly affect the measurements accuracy [*Finetti_1984*]. As in the 1-D model, the crowding region is characterized by its width δ but this time not only along the current injection branch but also in the perpendicular direction. To illustrate this configuration, the CBKR is here considered from the top view and not from a cross section (Figure IV-11 (b)). For $\delta > 0$, the lateral current flow gives an additional voltage drop that is included in the measured voltage V_k [*Stavitski_2007*].

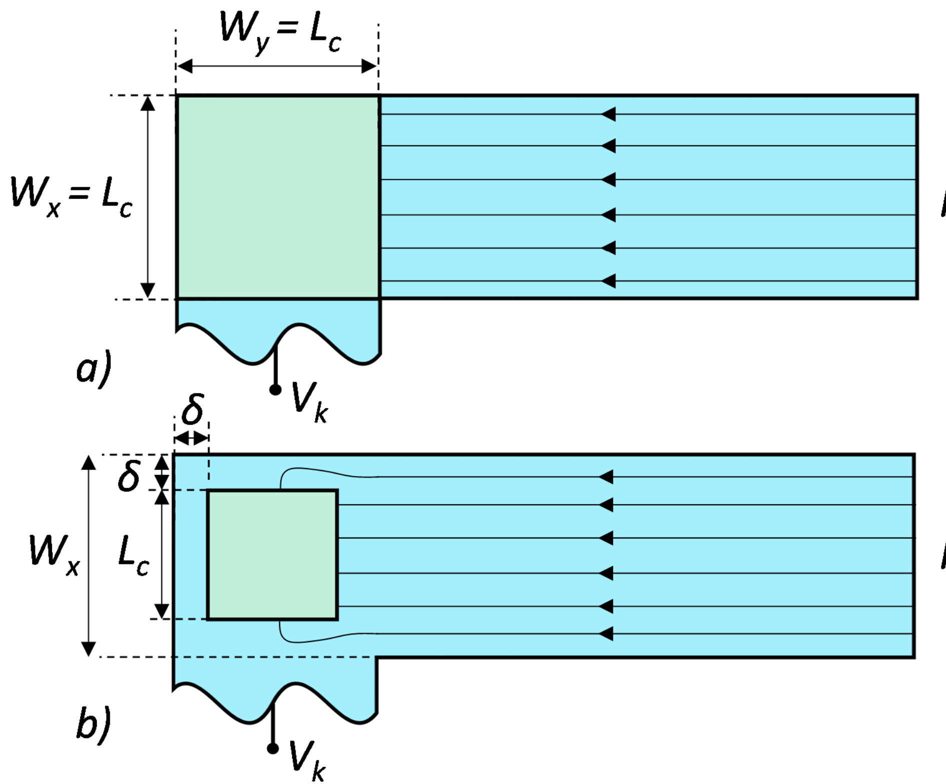


Figure IV-11: Top view of the CBKR structure of (a) an ideal case presenting no alignment margin (b) a realistic case with a margin δ.

In order to take into account this parasitic contribution, the 2D-model was developed by Schreyer and Saraswat [*Schreyer_1986*]. The resistance measured using the CBKR structure is still referred to as R_k and is the sum of the actual contact resistance R_c and the parasitic resistance R_{geom} induced by the current crowding. It was shown in [*Schreyer_1986*] that R_k could be expressed by Equations (IV-22) and (IV-23) .

$$R_k = R_c + R_{geom} \tag{IV-22}$$

$$R_k = \frac{\rho_c}{{L_c}^2} + \frac{4R_{sh}\delta^2}{3W_xW_y}\left[1 + \frac{\delta}{2(W_x - \delta)}\right] \tag{IV-23}$$

❖ Issues

It can be seen from the 1-D and 2-D models that the voltage measured with the probing branch is actually not straightforwardly representative of the voltage actually dropping in the contact. Therefore,

plotting the injected current as a function of the measured voltage does not actually give a signal representative of the contact.

Moreover, one can see from Equations (IV-21) and (IV-23) that knowing the sheet resistance R_{SH} of the semiconductor is required when using the 1-D and 2-D models. However, unlike the TLM measurement, the CBKR structure does not allow to measure this parameter. Therefore, solving these equations imply assuming the value of R_{SH} or using another structure on the same wafer to gain in accuracy.

IV.2.4 Summary of the section

The three main structures used in the state-of-the-art to probe contact have been presented. Although the back contact measurement is easily implemented and theoretically able to provide full I-V of a contact, its output is dramatically impacted by the substrate contribution. In extreme cases, the resulting I-V characteristics is only a signature of the substrate and does not reflect the contact.

TLM and CBKR require higher complexity of fabrication but ensure a better probing of the contact. TLM provides an accurate value of the contact resistivity but fails to supply I-V characteristics. To achieve such characterization, CBKR can be implemented but imply a complex data post-treatment to suppress the parasitic current crowding effects. Additionally, even if the substrate is not probed in series with the contact, its contribution does not allow to obtain the I-V characteristics in a large bias range. Pros and cons of each technique are summarized in Table IV-1.

Table IV-1: Summary of the advantages and disadvantages of each contact probing technique

Technique	Fabrication complexity	Theoretical ability to probe non-linear contact I-V	Impact of the substrate (at low ρ_c)
Back contact	1 level	Full I-V	Total screening
TLM	2 levels	No I-V	No impact
CBKR	3 levels	Reduced-window I-V	Reducing the probing window

IV.3 MIS contacts integration

Before presenting the experimental electrical results, the key information about the integration is presented in this section as long as the main expected properties of the materials. Finally, since they are required in order to use the different resistivity extraction models, the dimensions of the CBKR structures are reported.

IV.3.1 Substrate characteristics

The substrates used in this work consist in Si (30nm)/SiO_2 (145nm)/Si. In the following, both the top Si and the type of wafers will be indifferently referred to as Silicon On Insulator (SOI). The oxide of 145 nm under the SOI is called Burried OXide and noted BOX. The substrate characteristics are detailed in Figure IV-12.

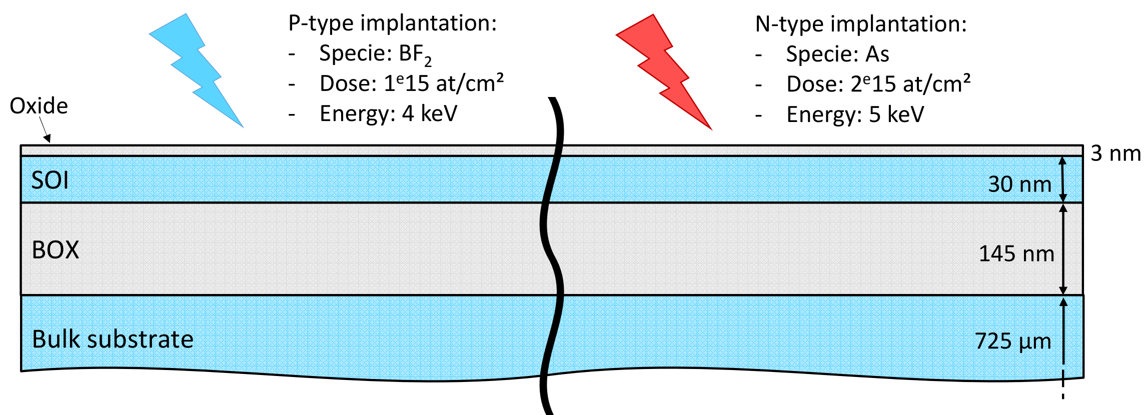


Figure IV-12: Schematic of the substrates used in this work. The conditions of ion implantation are reminded.

These wafers underwent an ion implantation process step in order to modify the conductivity of the top SOI. This implantation was performed through a 3 nm thin top oxide in order to prevent from Si surface damaging. n- and p-type Si were obtained using respectively As and BF_2 implantation. The implantation conditions are detailed in Figure IV-12. Finally the dopants were electrically activated by performing a spike annealing at 1050°C.

S-process TCAD simulation was performed to convert the dose and energy of the implantation into a doping concertation profile of dopants. This profile is plotted in Figure IV-13 as a function of the depth for both p- and n-implantation.

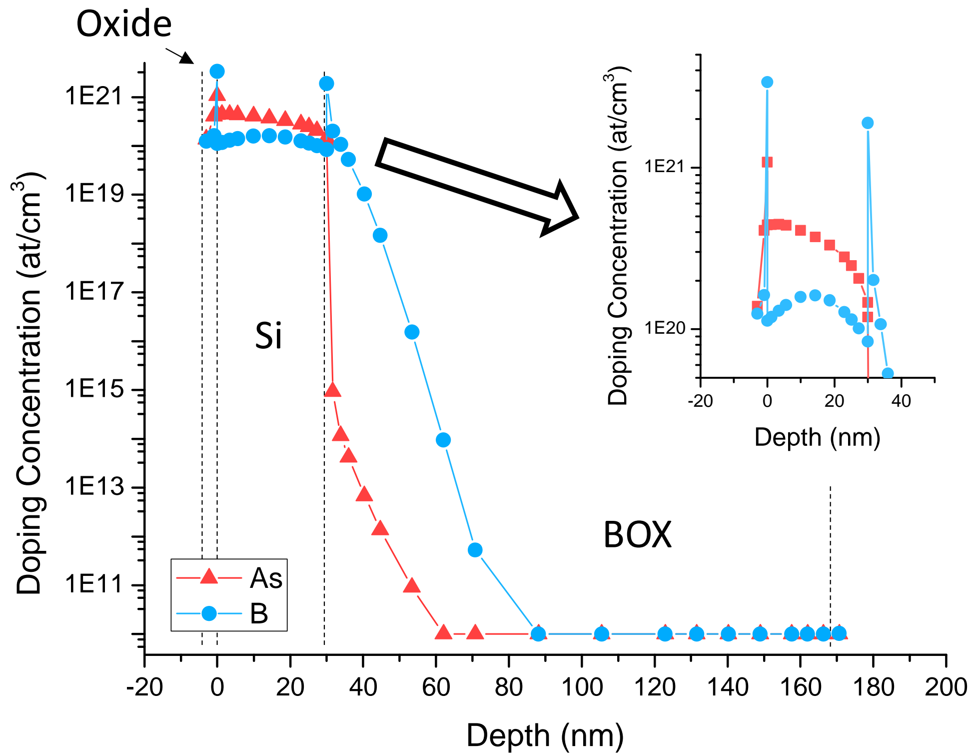


Figure IV-13: Overlay of simulated As and B concentration profiles. Inset: zoom on the SOI region.

According to the simulations, the concentration of B across the p-type Si is found extremely uniform, only varying between 1.0×10^{20} and 1.6×10^{20} at.cm^{-3}. Concerning the As profile in n-Si, the concentration is much less uniform since its value goes from 4.5×10^{20} at the top of the SOI to 1.2×10^{20} at.cm^{-3} at its bottom (inset of Figure IV-13).

As a first approximation, the doping concentration is considered equal to its mean value in the thin film, 1.32×10^{20} and 3.23×10^{20} at.cm^{-3} for B and As respectively. Considering the typical resistivity vs. doping concertation abacus in Figure IV-14 (for example available in [*Jayant Baliga_2010*]), the resistivity of p-Si and n-Si can be approximated around 9.6×10^{-4} and 3.3×10^{-4} Ω.cm. Thus considering a SOI thickness of 30 nm leads to sheet resistance values of respectively 320 and 110 Ω/□ for p- and n-Si respectively.

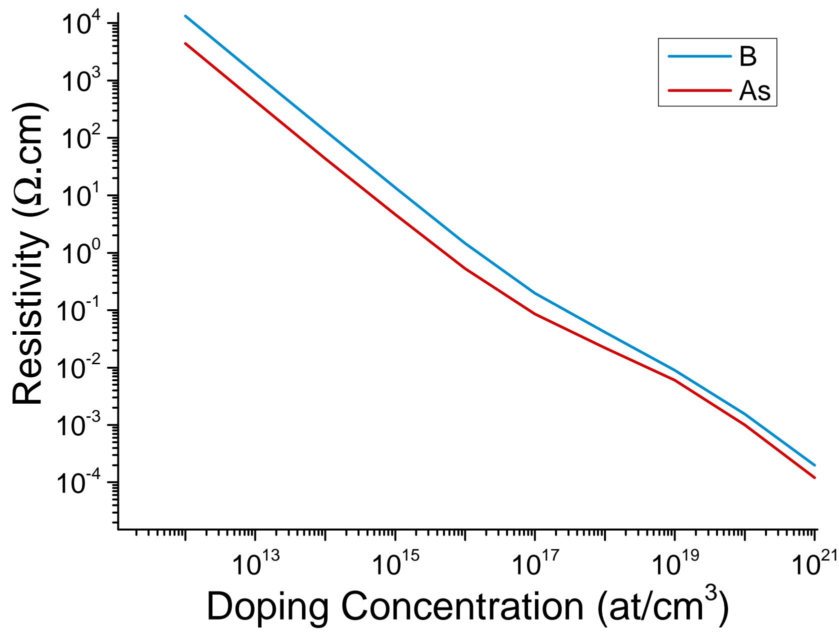


Figure IV-14: Typical plot of the resistivity as a function of the doping concentration [Jayant Baliga_2010].

IV.3.2 Dielectric characteristics

IV.3.2.a Expected thickness

Using the deposition kinetics presented in Chapter III in the cases of ALD Al_2O_3 and HfO_2, the number of ALD cycles were converted in a theoretical deposited thickness. The projected values are given in Table IV-2.

Table IV-2: Projected deposited thickness of Al_2O_3 and HfO_2 based on the kinetics study of Chapter III.

Al_2O_3				
Cycles	4	8	12	16
Thickness (Å)	0.8	1.7	3.8	9

HfO_2						
Cycles	15	20	25	30	35	40
Thickness (Å)	1.3	2.4	5.1	7.9	10.6	13.4

In the case of TiO_2, the tunnel resistance induced by the dielectric is assumed to be lower than that of the two other dielectrics. Hence, the maximum thickness of TiO_2 was increased compared to Al_2O_3

and HfO_2. For the CVD-deposited TiO_2 used in this work, the growth rate was assumed to be around 1 Å per 3.66 sec. Considering this value, thicknesses of 6, 12, 18 and 24 Å were targeted.

IV.3.2.b Expected tunnel barrier

As presented in the previous Chapters, initial guesses about the dielectrics tunnel barrier are based on theoretical Conduction and Valence Band Offsets (CBO and VBO). Although it has already been introduced before, the bar chart gathering the CBO and VBO found in the literature is reminded in Figure IV-15.

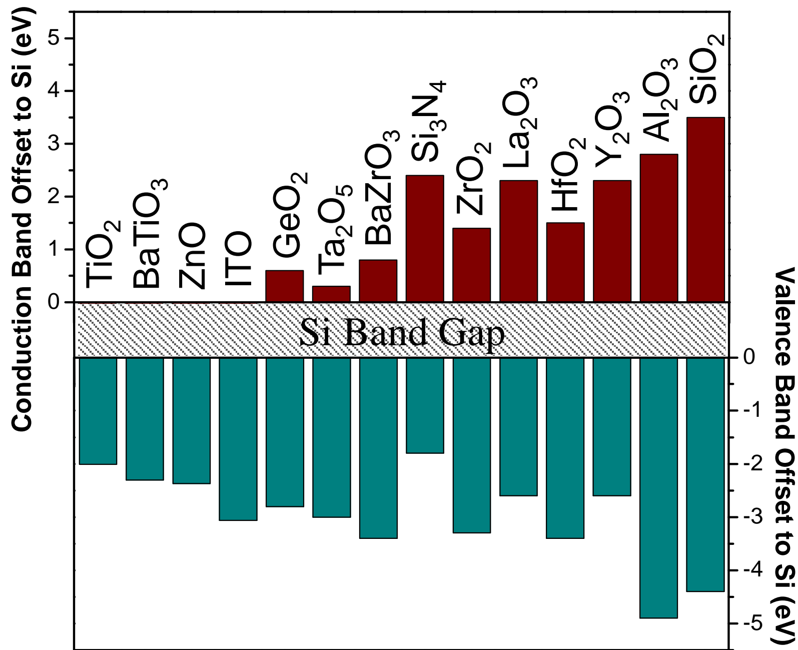


Figure IV-15: Conduction and Valence Band Offsets to Si of various dielectric [Gupta_2013, Robertson_2002].

Considering these VBO and CBO, the transmission probability of both holes and electrons across these dielectrics for a given thickness can be sorted as in Equation (IV-24).

$$T_{TiO_2} > T_{HfO_2} > T_{Al_2O_3} \quad \text{(IV-24)}$$

As presented in Chapter II, the tunnel resistance induced by Al_2O_3 is so large that no optimal thickness was found in a physically achievable range (3 Å when inserting between Ti and n-Si). Thanks to its ultra-low CBO, TiO_2 is however considered as the most promising layer studied in Chapter II, specifically to address n-type Si. Even though it was not studied, reasoning only on the CBO and VBO, HfO_2 can *a priori* be considered as an intermediate candidate.

IV.3.3 Expected materials parameters

In the following, the metal thickness is taken equal regardless of the dielectric insertion to ensure a valid comparison. The common stacks used in this work was TiN(60nm)/Ti(3nm) or TiN(60nm).

IV.3.3.a Ti workfunction

In the state-of-the-art, the value of 4.33 eV is often quoted as the work function of Ti [*Wright_2007*], [*Ramaswamy_2008*]. Ti can thus be considered as an n-type metal and is expected to be a good candidate to contact n-type Si.

IV.3.3.b TiN workfunction

According to the state-of-the-art, determining the workfunction of TiN can however be problematic. Indeed, this physical value depends extensively on the deposition technique, the thickness of the layer and the thermal annealing. In this work, Physical Vapor Deposition (PVD) was used to deposit a 60 nm thick TiN layer. No intentional annealing was performed but the deposition of the capping W layer was performed at 440°C for several minutes.

In [*Matsuhashi_1994*], a workfunction of 4.95 eV and 4.8 eV was found for TiN before and after 400°C annealing respectively. Nevertheless the deposition technique was not mentioned in the study. Coupling both I-V and C-V measurements, a PVD-deposited TiN workfunction was however extracted between 4.4 eV and 4.5 eV in [*Lima_2012*] for a 300 nm thick TiN layer as deposited or submitted to a short annealing at 400°C under forming gas. These conditions were thus close to the one used in this work but the layer was significantly thicker. Finally in [*Lujan_2002*], a workfunction of 4.8 eV was found in the case of a PVD-deposited TiN annealed at 420°C for 30 minutes. Considering these observations, TiN was *a priori* considered as a p-type metal presenting a work function around 4.8 eV. Nevertheless, the possibility to deviate from this figure was kept in mind.

IV.3.4 Structures layout

As presented in sub-section IV.2.3, the dimensions of CBKR are of prime importance since most of the parasitic effects of this structure are induced by the current non-uniformities. This phenomenon, called current crowding, is layout-dependent.

In this work, the CBKR test structures can be divided into two sets as presented in Figure IV-16.

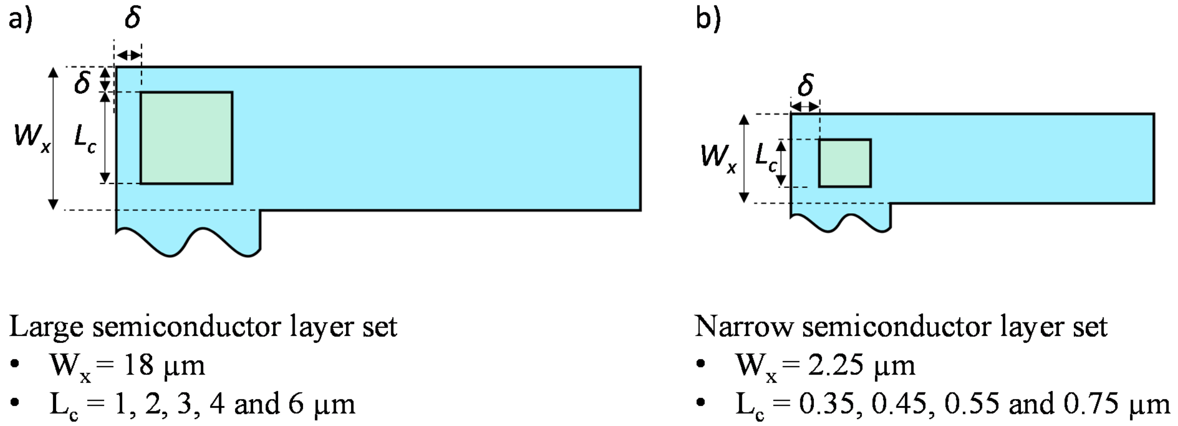


Figure IV-16: Main dimensions of the CBKR structures used in this work.

As noted in this figure, each set is associated to a given semiconductor width W_x, here 18 and 2.25µm, but feature several contact sizes L_c. The underlap parameter δ used as an input in the 1-D and 2-D models is therefore not constant and has to be evaluated for each contact size using Equation (IV-25).

$$\delta = \frac{W_x - L_c}{2} \qquad \text{(IV-25)}$$

Hence, the underlap parameter appears significant for the large semiconductor layer set of CBKR and particularly for the 1 and 2 µm contact. Their δ being equal to 8.5 and 8 µm respectively, important parasitic effects are expected.

IV.4 Experimental results

In this section, the electrical properties of the TiO_2-, HfO_2- and Al_2O_3- implemented MIS contacts were investigated using TLM and CBKR structures fabricated on 200 mm wafers in the clean-room of CEA-LETI. Such characterizations can be considered as the ultimate figure of merit to evaluate an insertion efficacy. First, all the transport properties are evaluated without assuming any theoretical physical parameters such as the band offsets of the dielectrics. Moreover, the measurements are performed on structures presenting processing constraints similar to the ones one would encounter when implementing these contacts on a device. Therefore, the resulting MIS contacts, having undergone parasitic effects such as substrate re-oxidation or metal induced scavenging, closely reflect the performance expected when defining these contacts during a MOSFET fabrication flow.

In the following the contact resistivities of the implemented contacts are first extracted from TLM measurements. As presented in sub-section IV.3.4, considering the dimensions of the CBKR, the parasitic effects are expected to be significant. Thus, the TLM-extracted resistivities being less impacted by these parasitics are used as references. In addition, as presented in section IV.2, TLM measurements allow the extraction of the sheet resistance R_{SH}. This parameter is of prime importance since it is also required to fit the 1-D and 2-D models for CBKR measurements. For these two reasons, first extractions are presented using TLM and followed by the CBKR ones.

IV.4.1 TLM measurements

As explained in sub-section IV.2.2, the resistivity of the sheet under the contact can be modified by the process steps performed during the contact fabrication. In the case of MIS contacts this modification is considered negligible. By extension, as a first approximation the sheet resistance was also considered unaltered in the case of a MS contact not subjected to an intentional silicidation process.

IV.4.1.a Sheet resistance

The sheet resistance of the top SOI was extracted for each batch of wafers. The resulting values are gathered in Table IV-3.

Table IV-3: TLM-extracted sheet resistance as a function of the contact configuration.

Contact configuration	Sheet Resistance (Ω/□)	
	p-Si	n-Si
Reference MS	420	230
Al_2O_3-MIS	420	230
HfO_2-MIS	520	250
TiO_2-MIS	510	225

The first striking observation is that the extracted values are far from the projections performed in sub-section IV.3.1. Indeed, based on the implantation conditions and on TCAD simulations, the sheet resistance was estimated around 320 and 110 Ω/□ respectively for the p-Si and the n-Si. In the cases of the reference metal/Si contacts, whereas an increase of 30% is observed for the p-Si, the sheet resistance of n-Si is more than doubled (+ 109%).

Additionally, the sheet resistance of p-Si appears significantly different from one process to another. As a matter of fact, when the Si of the metal/p-Si reference presents a sheet resistance of 420 Ω/□, the one of the HfO_2-based MIS contacts batch is found around 520 Ω/□.

The variation of the sheet resistance – compared to the expectations but also from one contact configuration to another one - seems hardly explainable by an alteration of the substrate properties induced by the fabrication of the contact itself. Indeed, even if implementing the contact could modify the substrate at the bottom of the contact cavity, it is unlikely that it would induce such a strong change on a large scale. Besides, reasoning in terms of thermal budget, its level remains globally the same regardless of the type of implemented contacts.

Therefore, the variation of sheet resistance might find its origin in a substrate modification during its processing itself. In other words, such an alteration could arise from a change of the thickness of the silicon and/or of its doping concentration. The sheet resistance being inversely proportional to the thickness, a doubled value of R_{SH} would correspond to a thickness divided by two. Such a variation seems unlikely to happen. However, the dependence of R_{SH} on the doping concentration being exponential, it thus seems more likely that the actual doping concentrations are lower than the expected one.

IV.4.1.b MS references

References consisting of direct TiN/Ti and Ti contacts to Si were measured using the TLM technique. No silicidation process was performed intentionally on these reference layers. The results are presented in Table IV-4.

Table IV-4: Contact resistivities of the reference TiN/Ti/Si and Ti/Si contacts extracted using TLM structures.

Process	**Associated resistivity (10^{-8} Ω.cm²)**	
	p-Si	**n-Si**
Reference TiN/Ti/Si	29	3.7
Reference TiN/Si	26	3.1

For each polarity of Si, the contact resistivities are nearly equivalent regardless of the metallization in direct contact with the Si. Only a slight improvement is observed on both p-Si and n-Si when using TiN (respectively -10% and -16% in terms of resistivity).

Considering the difference of ideal metal workfunction of Ti and TiN presented in sub-section IV.3.3, it would have seemed logical to obtain a large increase (resp. decrease) of the contact resistivity on n-Si (resp. p-Si) when passing from Ti to TiN. This lack of variation seems to be consistent with a strong FLP at the metal/Si interface, hence an almost constant effective metal workfunction regardless of the metal.

Also from Table IV-2, it appears that for both metallizations the resistivity on n-Si is one order of magnitude lower than that of p-Si. This effect can find its origin in the difference of SBH for electrons and for holes and/or in the difference of surface doping concentration between the two polarities of silicon. Indeed, an overly simple approximation presented in Equation (IV-26) consists in linking the contact resistivity, the SBH and the doping concentration of surface Si by an exponential law.

$$\rho_c = \rho_{c0} \exp\left[\frac{K\Phi_{bn}^{eff}}{\sqrt{N}}\right] \quad \text{(IV-26)}$$

Thus, if just considering the impact of doping concentration and assuming the values of surface doping concentrations obtained by the TCAD simulations (Figure IV-13), 1.1×10^{20} at.cm^{-3} for p-Si and 4.4×10^{20} at.cm^{-3} for and n-Si, it seems legitimate to find a lower resistivity on n-Si than on p-Si.

However, the FLP is also expected to generate an effective workfunction closer to the valence band than to the conduction band [*Nishimura_2008*]. Therefore, now reasoning in terms of SBH, due to FLP the barrier encountered by holes should be lower than that seen by electrons.

IV.4.1.c MIS contacts

Having no information on either the linearity of the contacts or on their resistivity, TLM extractions have been attempted on all the combinations of capping metals, dielectric insertions and Si polarities (n & p). The results are presented in Figure IV-17 for the combinations for which the TLM extrapolation treatment was possible. The MS references correspond to thicknesses equal to zero.

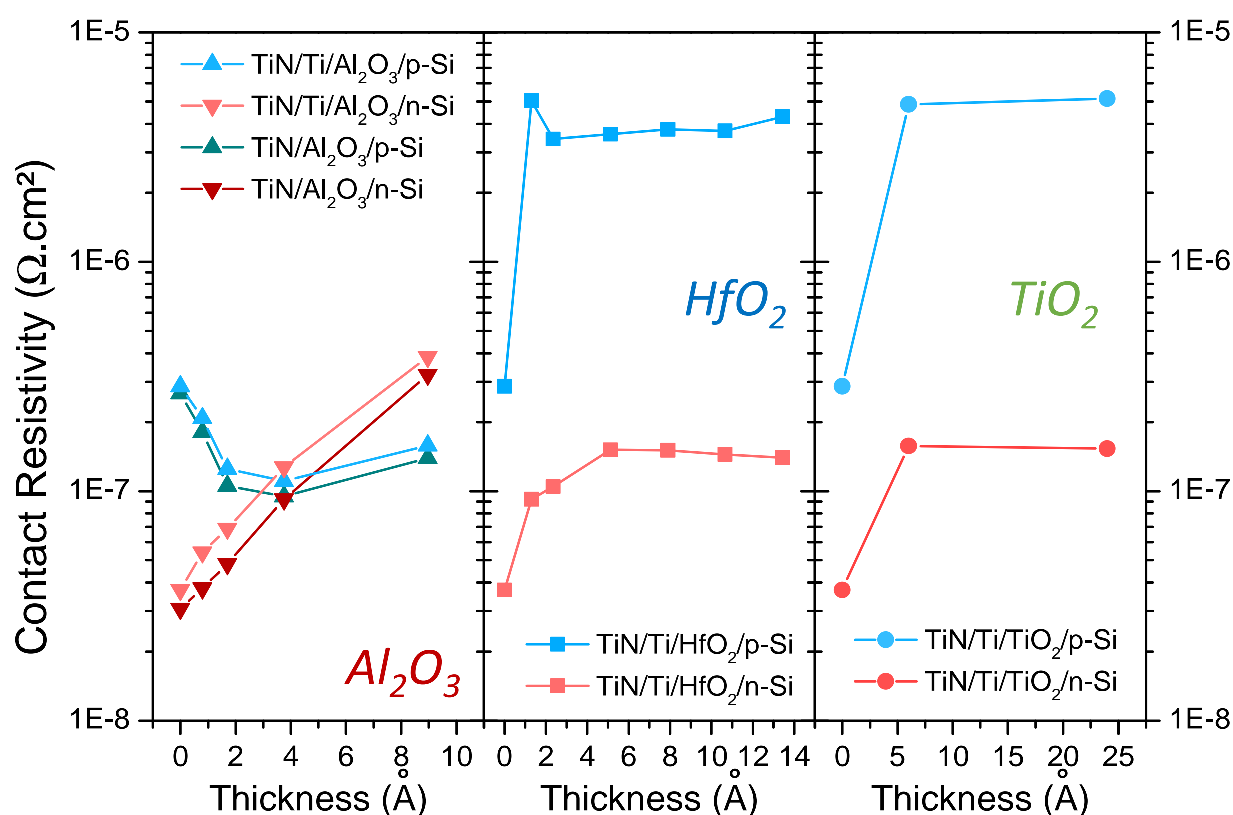


Figure IV-17: TLM extracted contact resistivity as the function of the thickness of Al_2O_3, HfO_2 and TiO_2 in the cases of Ti and TiN metallizations.

❖ TiO_2 and HfO_2 insertions

Presenting similar behavior, the cases of TiO_2 and HfO_2 are treated together. For these dielectrics, only the case of a Ti metallization is commented since it appears that the resistivity extraction was not possible in the case of a direct TiN capping metal.

The performance of the MIS contacts are found significantly degraded compared to the MS ones (thickness equal zero). As previously mentioned, the substrates used for the HfO_2/p-Si and TiO_2/p-Si contacts fabrication feature higher sheet resistance that the ones used for the metal/p-Si references (Table IV-3). Therefore, these substrates might have a lower doping concentration than the reference ones. Since the contact resistivity exponentially depends on this physical value, the significant difference between the references and the HfO_2/p-Si and TiO_2/p-Si contacts in terms of contact resistivity (Figure IV-17) could partially find its origin in a difference of doping concentrations.

Besides, the performance of the contacts based on p-Si is found significantly degraded compared to the ones on n-Si. This seems consistent with the fact that Ti is used as capping metal. Being an n-type metal, in case of FLP mitigation, contacts are expected to be improved on n-Si and degraded on p-Si. Moreover, as presented in Figure IV-15, TiO_2 and HfO_2 feature much higher valence band offsets that conduction ones. Thus, for a given insertion thickness, the induced tunnel resistance is expected to be much higher for holes than for electrons.

However for the same reasons, the observed degradation of performance on n-Si compared to the reference was not foreseen and particularly in the case of TiO_2. Indeed, as presented in Figure IV-15, TiO_2 features no conduction band offset to Si and thus is not believed to induce a tunnel barrier for electrons.

Even if the TiN/Ti/TiO_2/Si stack has not been explicitly characterized in Chapter III, two phenomena could provide a suitable explanation for this unexpected high resistivity. On the one hand, Yu *et. al* [*Yu_2015*] showed that even without performing annealing, implementing a contact to n-Si composed of a 1nm-thick ALD-deposited TiO_2 may lead to significant contact resistivity. This electrical conductivity degradation was found despite a large FLP mitigation, resulting in a low SBH, and was thus attributed to a large CBO of the amorphous TiO_2. On the other hand, still in [*Yu_2015*], it was shown that the oxygen of the insertion should reasonably diffuse in Ti if directly contacted to the TiO_2 layer. In that case, the resulting contact can be assimilated to a MS interface presenting a metal with a highly degraded conductivity.

For these HfO_2 and TiO_2, no optimal MIS contact configuration was found and the resistivity of each MS contact reference remains the lower one.

❖ Al_2O_3 insertions

The case of Al_2O_3-based MIS contacts presents a behavior far different from the HfO_2- and TiO_2-based ones. First, the performance of contacts on p-Si does not feature the same significant degradation. Even more, an improvement is observed and the expected U-shaped curve is obtained with an optimal theoretical thickness of 3.8 Å for both TiN/Ti and TiN metallizations. A degradation is only observed in the case of n-Si substrates.

This observation appears inconsistent with the initial expectations. Indeed, Ti being presumptively considered n-type and TiN p-type, the response of the contact resistivity to the dielectrics thickness increase would be complementary. In other words, whereas contacts on p-Si would be improved with TiN and degraded with Ti, contacts on n-Si would be degraded with TiN and improved with Ti. However, in this work the tendency of the contact resistivity is the same regardless of the metallization type.

This consideration may have two principal explanations. On the one hand, the ideal workfunction of TiN was assumed to be around 4.8 eV meaning closer to a p-type metal. As presented in sections IV.3.3, this value is not a real consensus in the state-of-the-art and discrepancy between the assumed value and the effective one might be the origin of the observed electrical behavior. On the other hand, if assuming that Ti is effectively n-type and TiN p-type, such behavior could be explained by considering that the dielectric does not mitigate the FLP but induces a FLP at another energy in the Si bandgap. Such a result has already been obtained in [*Lin_2012*] when contact resistivity improvement was observed on n-Ge for both Ti and Pt. In this case, Pt is doubtlessly a p-type metal with a high work function and FLP mitigation would lead to contact degradation on n-Ge.

Finally, considering the valence and conduction band offsets of Figure IV-17, Al_2O_3 was expected to feature a significant tunnel resistance for both holes and electrons. Thus, contact degradation was foreseen for both Si polarities regardless of the workfunction attributed to the capping metal.

❖ Optimal configurations

The optimal thicknesses corresponding to each combination are gathered in Table IV-5 along with their associated contact resistivity. The X in the table indicates that the TLM extraction was not possible for the MIS combination. Besides, resistivities in blue were obtained with MIS contacts whereas the ones in red correspond to MS contacts.

Table IV-5: Contact resistivities of the Al_2O_3, HfO_2 and TiO_2 MIS contacts extracted using TLM structures.

Process	Best configuration (Å)		Associated resistivity (10^{-8} Ω .cm²)	
	p-Si	n-Si	p-Si	n-Si
TiN/Ti/Al_2O_3/Si	3.8	0	11	3.7
TiN/Al_2O_3/Si	3.8	0	9.5	3.1
TiN/Ti/HfO_2/Si	0	0	29	3.7
TiN/HfO_2/Si	X	X	X	X
TiN/Ti/TiO_2/Si	0	0	29	3.7
TiN/TiO_2/Si	X	X	X	X

To summarize this sub-section and as highlighted by this table, the main conclusion remains that the ranking of the dielectrics in terms of induced tunnel resistance is far from expected. Indeed, TiO_2 was initially anticipated as the best candidate for MIS contacts but actually results in the most resistive stacks of the study. This phenomenon seems to be attributed to the intermixing of elements occurring in the {Ti, Si, O} set and leading to the destruction of the TiO_2 insertion. On the contrary, an improvement on p-Si was found when using Al_2O_3.

IV.4.2 CBKR measurements

The TLM method, being based on the assumption that the probed contact is linear, does not allow probing all the implemented contacts. Therefore, using CBKR enable the characterization of the nonlinear fabricated contacts. Moreover, for the contacts for which the TLM extraction was possible, it also enables a comparison of the figures obtained by both methods.

As presented in sub-section IV.2.3, the models used to fit the data extracted by CBKR require the knowledge of the sheet resistance of the underlying semiconductor layer. Nevertheless, this structure does not allow its evaluation. Therefore, the values found by TLM measurements and gathered in Table IV-3 are here considered. Prior to treating all the combinations of metals and dielectric and presenting the associated results, a protocol was evaluated on a reference case. Indeed, several models being available in the state-of the art, namely 0-D, 1-D and 2-D, a first test was achieved on the TiN/n-Si case.

IV.4.2.a The TiN/n-Si case

The I-V characteristics of CBKR structures presenting different contact sizes were extracted for the case of TiN/n-Si. The I-Vs corresponding to the large semiconductor layer set are plotted in Figure IV-18.

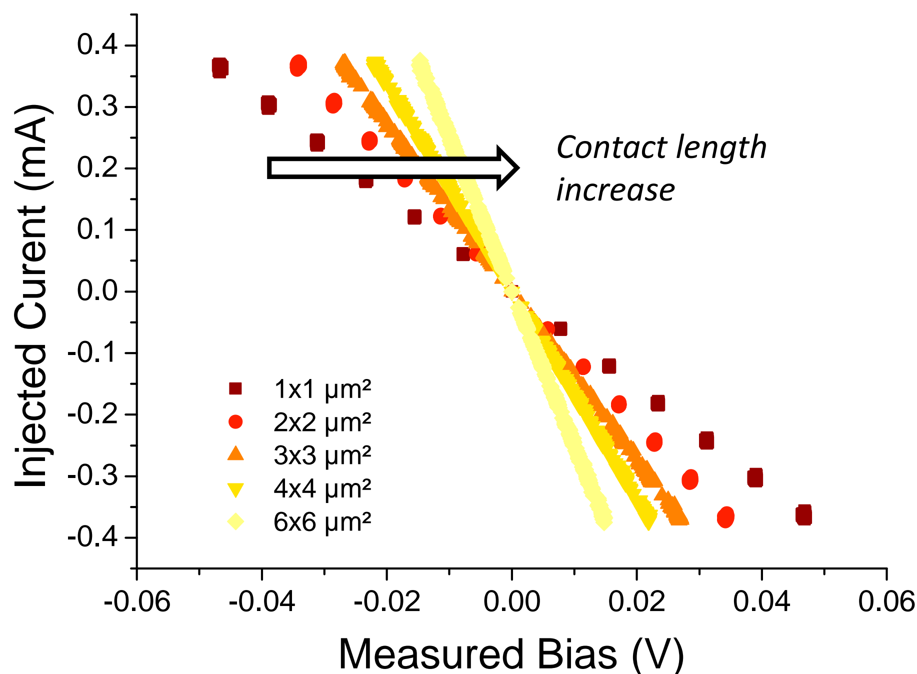


Figure IV-18: I-V characteristics of CBKR structures presenting different contact sizes for the case of TiN/n-Si.

Using the I-V characteristics plotted in Figure IV-18, the resistance of the TiN/n-Si contact was extracted as a function of the contact size. Fitting these extracted values with the CBKR models presented in sub-section IV.2.3 would allow to obtain the corresponding contact resistivity. Nevertheless, several models being available, the data treatment was performed in the other way around in order to discriminate the most effective one.

Indeed, since the TLM extraction was possible on this contact, its contact resistivity and the sheet resistance of the n-Si are known. Therefore, these two values were used as inputs in the 0-D, 1-D and 2-D models and the resulting curves were compared to the experimentally extracted R_k. The overlay is plotted in Figure IV-19 for the three models and for the experimental measurement.

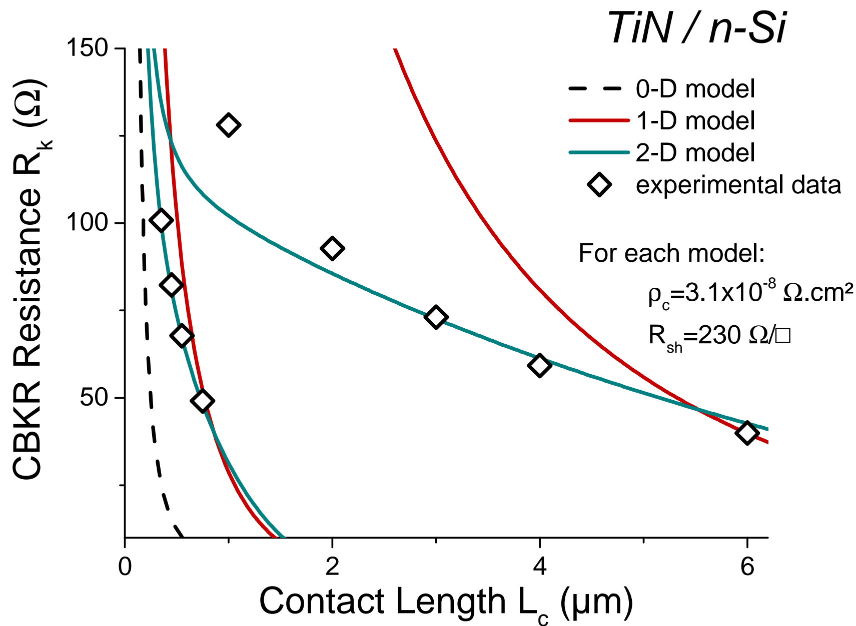


Figure IV-19: CBKR resistance as a function of the contact length. The plot is an overlay of the R_k generated with the 0-D, 1-D and 2-D models and the ones experimentally measured.

It results from this figure that the 0-D and 1-D models are clearly not matching the experimental data when assuming a contact resistivity equal to the one obtained by TLM.

Using the 0-D model, no fit can be obtained even varying the input parameters over a wide range. Indeed, this model cannot feature the difference between the two sets of contacts presented in IV.3.4.

Concerning the 1-D model, a match is only observed for the 0.75 µm and 6 µm contact lengths. A global fit (not shown here) can be obtained varying drastically the inputs of contact resistivity and Si sheet resistance. The values required to obtain an approximate match being considered unrealistic, this model was judged irrelevant.

Only the 2-D model allows an overall overlap with the experimental CBKR measurements when using the values found in TLM. As one can see, the match is particularly conclusive for the "narrow semiconductor layer" set of contacts i.e. 0.35, 0.45, 0.55 and 0.75 µm long contacts and can be even improved if using a ρ_c equal to $3x10^{-8}$ Ω.cm².

For the large semiconductor set, a discrepancy is observed at 1 and 2 µm. Nevertheless, a perfect match can be obtained if the contact resistivity is increased by one order of magnitude i.e. considering a ρ_c equal to $3x10^{-7}$ Ω.cm² as displayed in Figure IV-20.

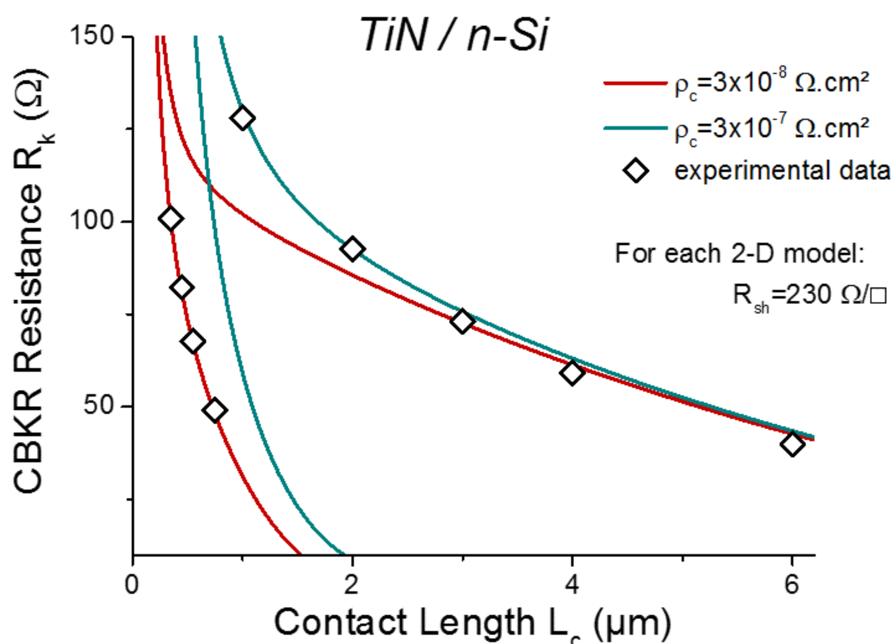


Figure IV-20: CBKR resistance as a function of the contact length. The plot is an overlay of the R_k generated with the same 2-D model but presenting different contact resistivity as input.

From the preliminary test performed on TiN/n-Si reference, only the 2-D model is considered as reliable. By fitting this model separately on both the narrow and the large semiconductor layer sets of CBKR structures, two resistivities can be associated with the probed contact. A discrepancy of one decade was found between these two values in the case of TiN/n-Si.

IV.4.2.b CBKR I-V characteristics generation

I-V characteristics were generated for all the different combinations of dielectrics, capping metals and Si polarities and for all the size of contacts. Due to the large number of resulting curves, all the I-V characteristics are not presented here. However, the results obtained with the TiN/TiO_2/n-Si and TiN/Ti/TiO_2/n-Si are displayed in Figure IV-21 for the sake of illustration.

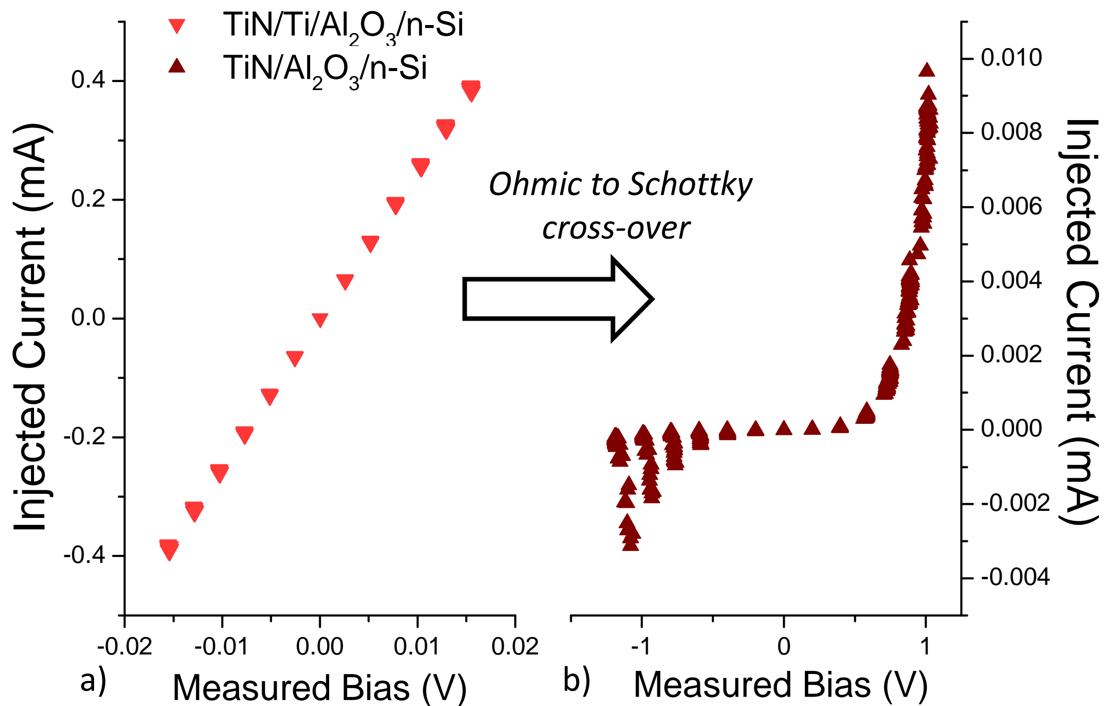


Figure IV-21:CBKR-generated IV-characteristics of TiO_2-based MIS contacts presenting (a) TiN/Ti and (b) TiN metallizations.

It appears that withdrawing the Ti layer at the direct contact with TiO_2 leads to a swing from Ohmic to Schottky behavior. This loss of linearity is reasonably at the origin of the impossibility to probe the TiN/TiO_2/n-Si contact using TLM. Similar observations can be extended to TiN/TiO_2/p-Si but also to TiN/HfO_2/n-Si and TiN/HfO_2/p-Si.

IV.4.2.c CBKR characterization of MS and MIS contacts

In the following, contact resistances are extracted on the CBKR-generated I-V characteristics for all the combination of MS and MIS contacts and the 2-D model is used to extract the contact resistivity from it. As explained in the protocol test performed on the TiN/n-Si, this model is separately fitted on the large and the narrow sets and thus leads to the extraction of two resistivities per contact combination.

❖ Contacts presenting both TLM and CBKR extractions

A comparison between all the TLM and CBKR resistivities is achieved. Since the TLM method is expected to extract a resistivity around zero volts for non-resistive contacts, the CBKR resistances are

also extracted around zero to ensure a consistent comparison. Both TiN/Ti/Al_2O_3/p- & n-Si and TiN/Al_2O_3/p- & n-Si have been considered. However, since both combinations feature almost the same electrical behavior (Figure IV-17), only contacts with Ti are presented for the sake of clarity. Results are plotted in Figure IV-22.

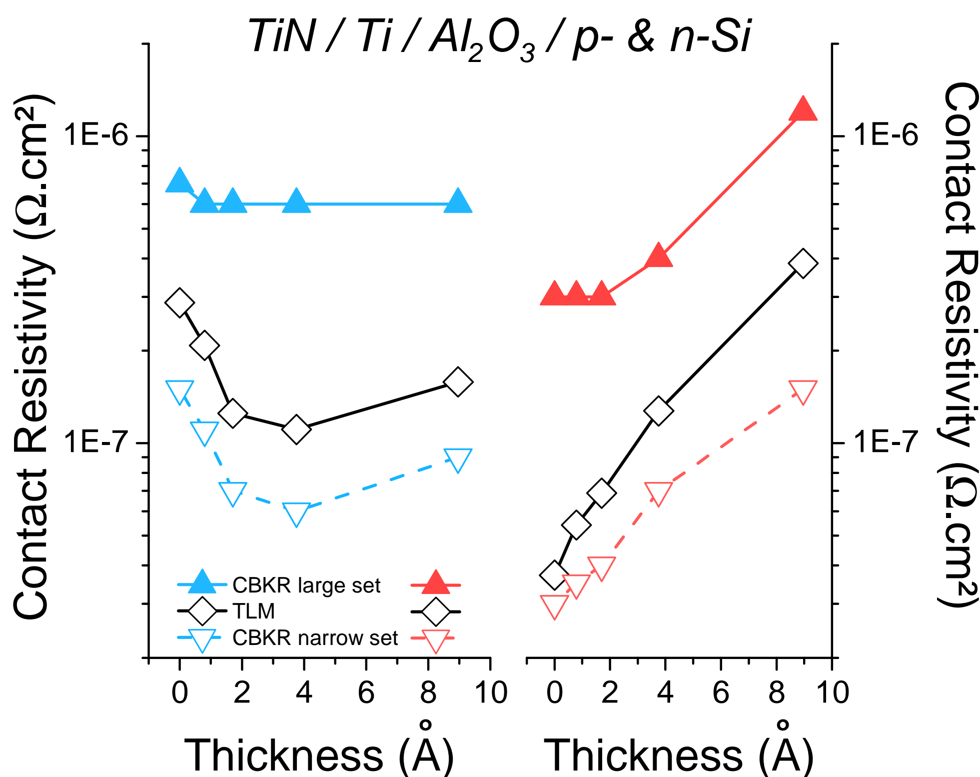


Figure IV-22: Contact resistivity of TiN/Ti/Al_2O_3/p- & n-Si extracted around zero using TLM and 2-D model CBKR (narrow and large sets).

From this figure, it results that the CBKR-extracted resistivities follow the same trend as the TLM-extracted ones. However, values extracted from the narrow set are found below the TLM-extracted ones whereas values extracted from the large set are found above them.

A similar protocol was applied to TiN/Ti/HfO_2/p- & n-Si contacts and the results are reported in Figure IV-23.

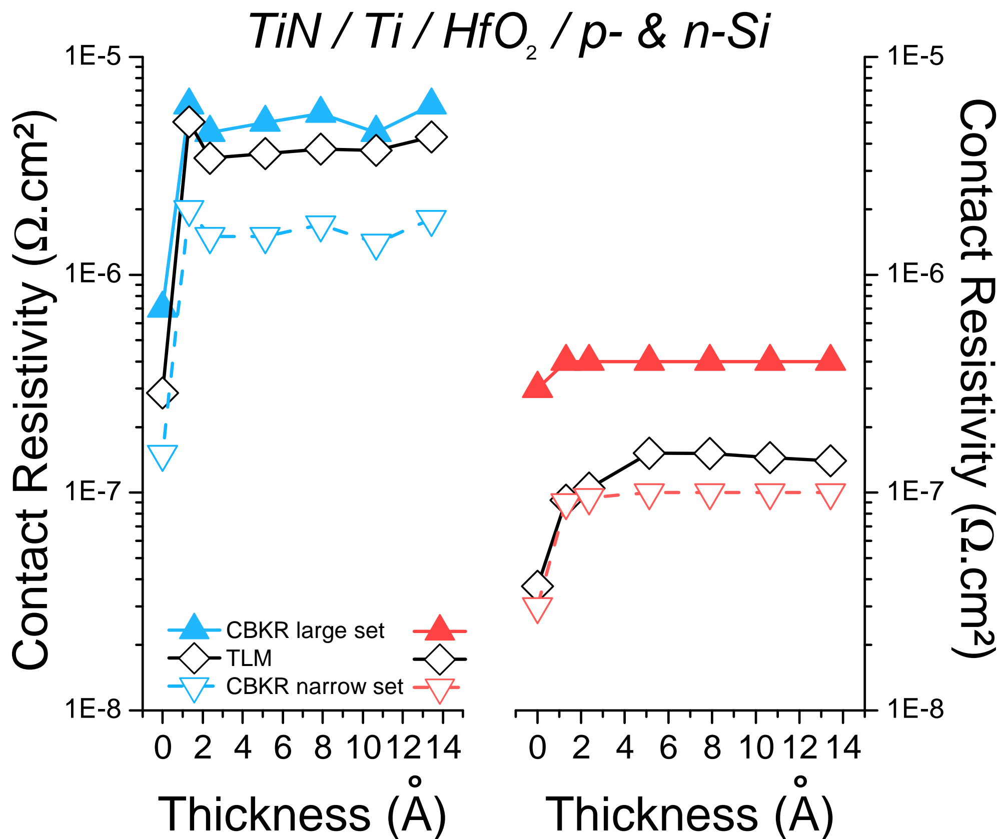


Figure IV-23: Contact resistivity of TiN/Ti/HfO₂/p- & n-Si extracted around zero using TLM and 2-D model CBKR (narrow and large sets).

Similar observations than that of the Al_2O_3-based contacts can be made on ones based on HfO_2. The CBKR-extracted resistivities present the same behavior than that of the TLM-extracted ones and surround them.

The position of the TLM-extracted resistivities relatively to the ones extracted with the narrow and large CBKR sets seems to vary with the magnitude of the resistivity. For example, in the TiN/Ti/HfO_2/p-Si case, the TLM-extracted resistivities appear closer to the large CBKR set extracted ones whereas they are closer to the narrow set extracted ones in the TiN/Ti/HfO_2/n-Si case. Therefore, additional calculations were performed to check this trend.

To measure the relative position of the different resistivities, a coefficient noted α can be defined by Equation (IV-27)

$$\alpha = \frac{\log(\rho_c^{TLM}) - \log(\rho_c^{CBKR,n})}{\log(\rho_c^{CBKR,l}) - \log(\rho_c^{CBKR,n})} \tag{IV-27}$$

where ρ_c^{TLM}, $\rho_c^{CBKR,n}$ and $\rho_c^{CBKR,l}$ are the contact resistivities respectively extracted with the TLM, the narrow set of CBKR and the large set of CBKR.

To graphically visualize the variation of the α parameter, the case of TiN/Ti/Al_2O_3/n-Si is represented in Figure IV-24.

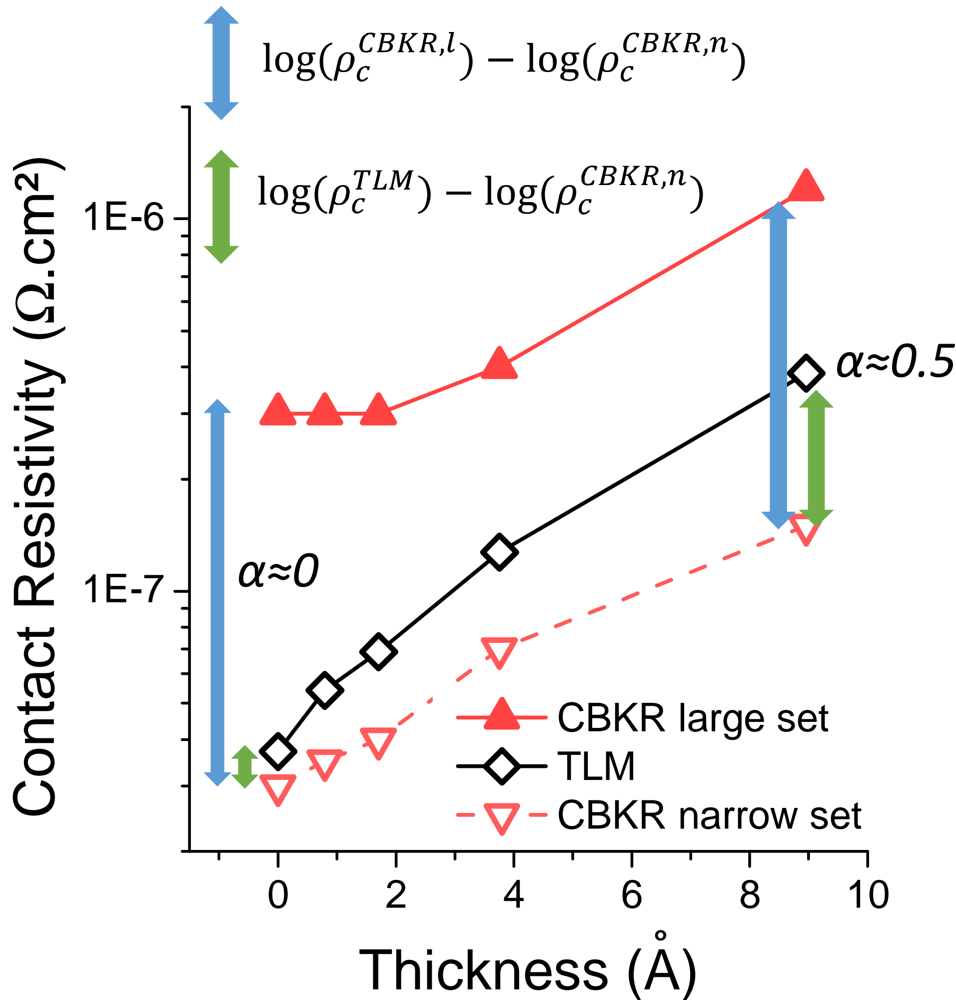


Figure IV-24: Contact resistivity of TiN/Ti/Al_2O_3/ n-Si extracted around zero using TLM and 2-D model CBKR (narrow and large sets).

As illustrated in this figure, the numerator of Equation (IV-27) represents the distance between the resistivity extracted by TLM with the one extracted by the narrow set of CBKR and the denominator represents the distance between the resistivity extracted by the large set of CBKR with the one extracted by the narrow set of CBKR.

Thus, taking this convention, α is a parameter comprised in the [0 ; 1] interval. If α is close to 0, the resistivity extracted by TLM is close to the one extracted by the narrow set of CBKR. If α is close to 1, the resistivity extracted by TLM is close to the one extracted by the large set of CBKR.

In order to verify the previously intuited trend i.e. a correlation between the relative positions of the TLM-extracted resistivities with the magnitude of the resistivity, the α parameter is plotted as a function of the TLM-extracted resistivities in Figure IV-25 for all the MS and MIS combinations.

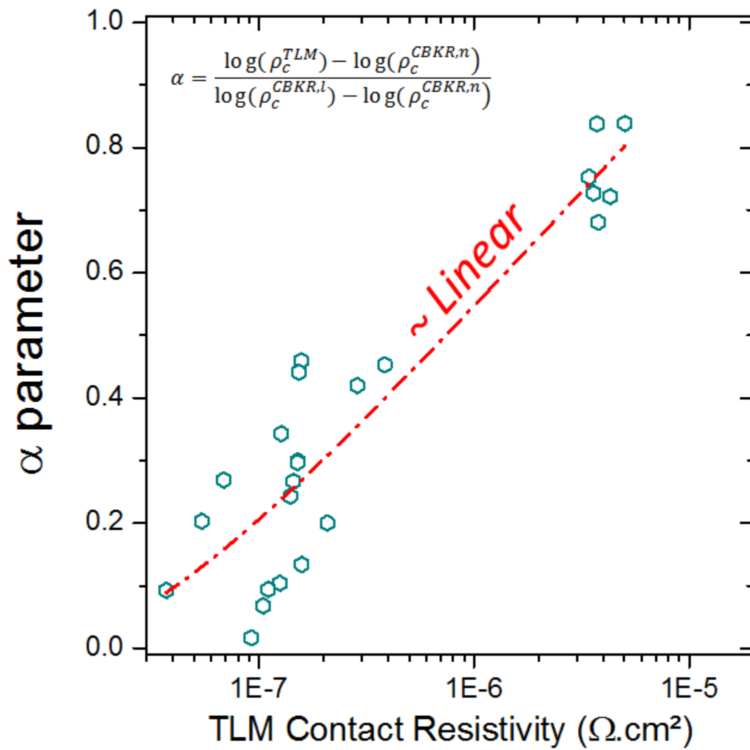


Figure IV-25: α parameter as a function of the TLM-extracted resistivities for all the MS and MIS combinations.

From this plot, it appears that the α parameter indeed varies with the magnitude of the contact resistivity and seems to follow a linear trend when plotted in a semi-log scale.

As mentioned previously, the 2-D model was seemingly considered as the only reliable model to fit the data extracted by CBKR. A significant discrepancy was observed when fitting the large semiconductor layer set and the narrow one. By comparing these value with the TLM-extracted resistivity and studying the α parameter, it results that whereas the narrow set of CBKR turns out to be more suitable to probe low contact resistivities, the large one seems more accurate for the high contact resistivities.

The final protocol consists in:

- giving the priority to the TLM measurement when the linearity of the contact allows it;
- extracting the resistivities around zero using a CBKR measurement if the probed contact is not linear;
- choosing between the narrow and large set extracted resistivities according more trust to the former if the magnitude of the contact resistivity is below 10^{-7} Ω.cm² or to the latter if the resistivity magnitude if above 10^{-6} Ω.cm².

❖ Contacts only presenting CBKR extractions

In view of the previous section, a fitting of the CBKR data is attempted on the contacts for which the TLM extraction was not fruitful, namely, TiN/HfO_2/n & p-Si and TiN/TiO_2/ n & p-Si. Having no preconceived idea on the magnitude of the resistivity of these contacts, both the narrow and large sets of CBKR were used. However, no extraction was experimentally possible with the narrow one.

The results of TiN/HfO_2/ n- & p-Si are displayed in Figure IV-26.

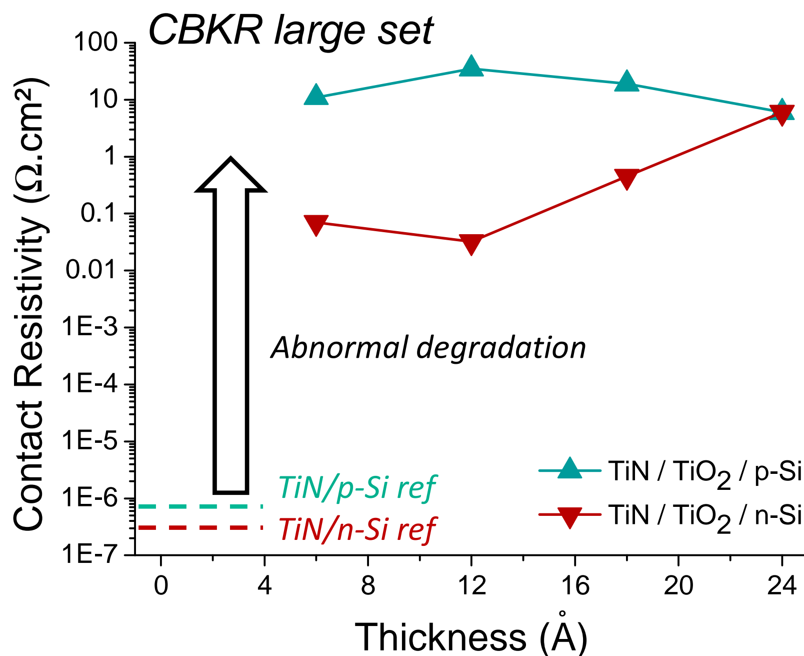


Figure IV-26: Contact resistivity of TiN/TiO_2/p- & n-Si extracted around zero using 2-D model CBKR (large set).

A significant degradation of the contact resistivity is observed for both TiN/TiO_2/p- & n-Si stacks. This high magnitude might explain the impossibility to probe the narrow set of CBKR. In this set, the

contact areas being ultra-small, the resulting contact resistance is dramatically high and the set-up cannot even measure the signal. For example for a 350 nm long contact, its area is 0.1225 µm² and the associated resistance is thus around 10^{10} Ω in the case of the TiN/TiO_2/ p-Si.

This degradation can seemingly be attributed to the formation of a SiO_x layer. Indeed, as observed in Chapter III, an important elements intermixing occurs in the samples initially meant to present a TiO_x insertion. In $TiN/TiO_2/Si$ stacks, although the absence of Ti as capping layer was expected to bring stability, the vicinity of the TiO_2 layer with the Si leads to an important oxygen pumping by the latter.

Besides, the behavior of the resistivity as a function of the theoretical insertion thickness is not straightforward. In the TiN/TiO_2/n-Si case, the U-shaped curve is observed despite the high contact resistivity range. If the global electrical transport properties are driven by an important SiO_x regrowth inducing dramatic degradations, it seems impossible that the FLP mitigation might lead to a noticeable improvement.

Additionally, in the TiN/TiO_2/p-Si case, when plotting the contact resistivity as a function of the theoretical insertion thickness, a bell-curve is observed. This type of curve being not predicted by the MIGS theory, a dedicated section is devoted to this effect in section IV.5.2.

As plotted in Figure IV-26, similar degradation was also obtained on TiN/HfO_2/ n- & p-Si.

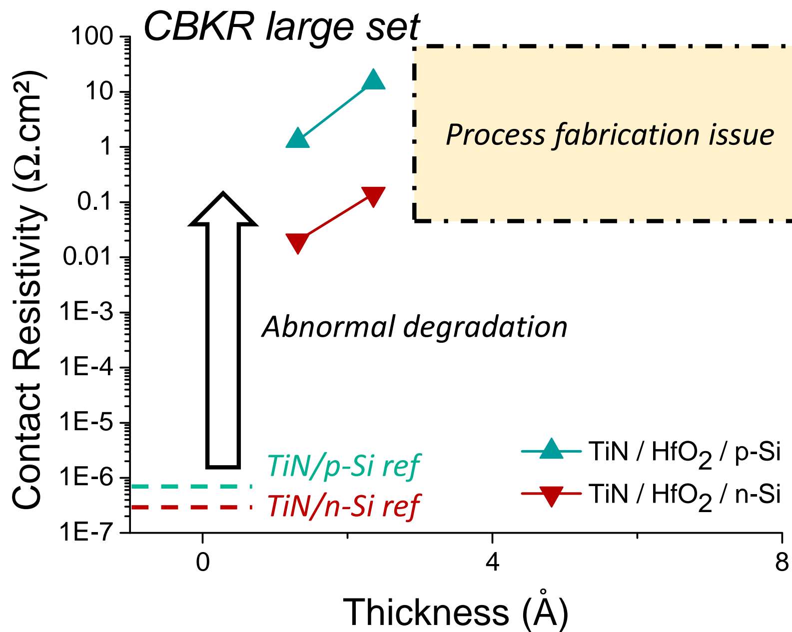


Figure IV-27: Contact resistivity of TiN/TiO_2/p- & n-Si extracted around zero using 2-D model CBKR (large set).

Nevertheless, due to an issue during the process of fabrication of these samples, only two HfO_2 thicknesses are available.

IV.5 Discussions

IV.5.1 Obtaining contact signature I-V characteristics with CBKR

In Figure IV-18, it is worth noting that whereas the bias applied on the whole structure was comprised between -1.2 and 1.2 V, the range of measured bias is only between -0.06 and 0.06 V. If considering the top view of the CBKR structure in Figure IV-28, this significant voltage drop can be attributed to the resistance of the semiconductor branch 2.

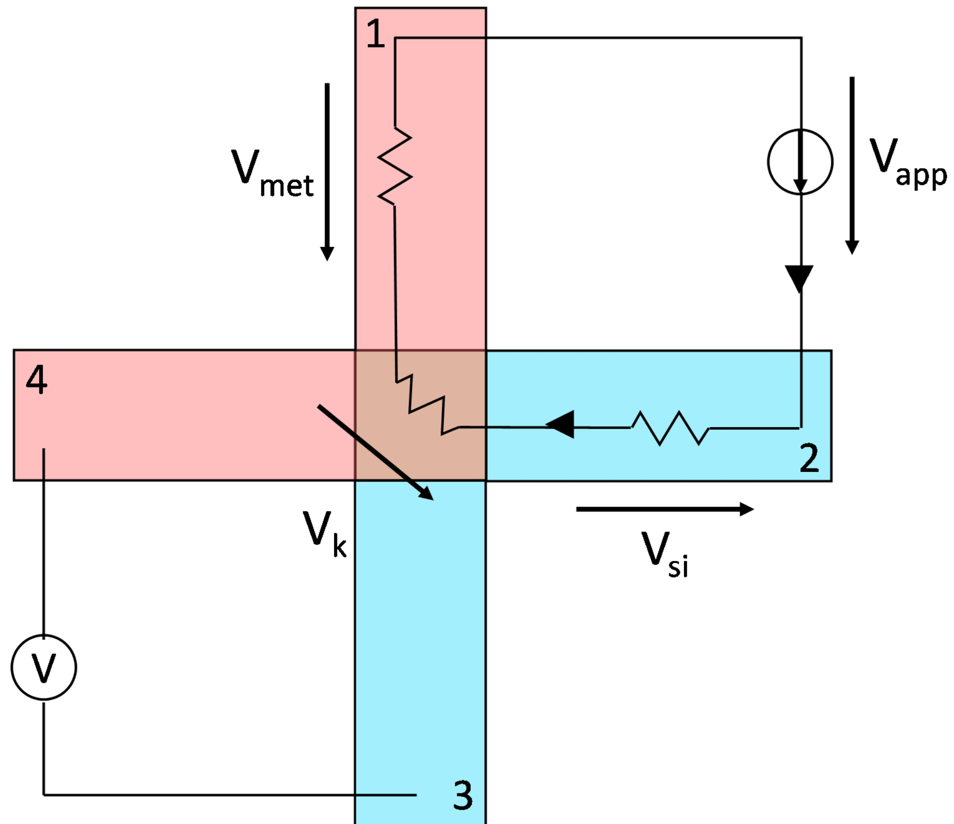


Figure IV-28: Top view of the CBKR structure.

Indeed, even if the contribution of branch 2 is not measured when using the CBKR convention (measurement between 4 and 3), it is still involved in the current injection path. In a case of a contact presenting a low resistivity, Equations (IV-28) and (IV-29) can be obtained.

$$V_{app} \approx R_{Si} \times I_{app} \quad \text{(IV-28)}$$

$$V_{mes} = R_k \times I_{app} \quad \text{(IV-29)}$$

Thus the lower the contact resistivity of the probed contact, the higher the injected current, the higher the voltage drop occurring in the semiconductor branch 2 and then the lower the range of the

measured bias. One of the initial purposes of using CBKR is to obtain the full I-V characteristics of the contact on an extended range in order to visualize a hypothetical non-linearity and/or a non-symmetry. One can see that this seems not achievable due to this parasitic substrate resistance.

IV.5.2 The TiN/TiO_2/Si case

As discussed previously, the behavior of the TiN/TiO_2/Si contact resistivity as a function of the theoretical insertion thickness is not straightforward. In order to underline this trend, the normalized contact resistivity is considered in Figure IV-29.

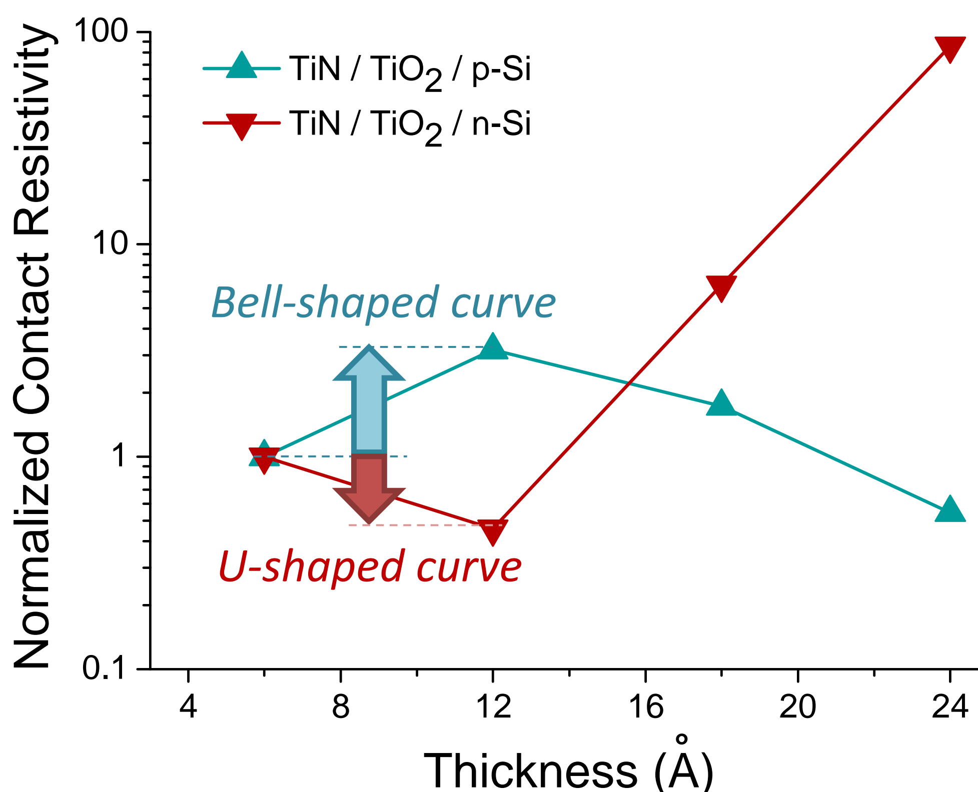


Figure IV-29: Contact resistivity of TiN/TiO_2/n- & p-Si as a function of the dielectric insertion.

While the n-Si based contact resistivity features a classical U-shaped curve, the one based on p-Si follows a bell-shaped curve when increasing the dielectric insertion thickness. Although such a dependence has seldom been reported in the past, similar results can be found in [*Roy_2012*]. In this

study, considering HfO_2 and TiO_2 based contacts, bell-shaped curves were obtained when introducing bulk charges in the dielectric inserted between a p-type metal and n-Ge.

In the simulation module used to evaluate the FLP (presented in Chapter II), its intensity is calculated using an interface charge model initially developed in [*Monch_1990*]. Basically the link between the slope parameter S and the charges is described by Equation (IV-30).

$$S = \frac{d\Phi_m^{eff}}{d\Phi_m} = \frac{\varepsilon_{sc}}{\varepsilon_{sc} + q^2\delta D_{it}} \quad \text{(IV-30)}$$

where Φ_m^{eff} is the effective metal workfunction, Φ_m is the ideal one, ε_{sc} is the permittivity of the considered semiconductor (here Si) and D_{it} is the density of the interface charge.

So far the interface charges were attributed solely to MIGS without considering any fixed charge induced by defects also called Defects Induced Gap States (DIGS). Nevertheless this type of model cannot predict the results obtained in Figure IV-29 and particularly the bell-shaped curve.

As presented in Equation (IV-31), using analytical simulation, charges were introduced at the interface between the dielectric and the substrate in order to account for the DIGS contribution.

$$S = \frac{\varepsilon_{sc}}{\varepsilon_{sc} + q^2\delta(D_{MIGS} + D_{DIGS})} \quad \text{(IV-31)}$$

A notional case was studied considering a metallization presenting an ideal workfunction of 4 eV. The variation of the effective workfunction as a function of the dielectric thickness was generated for different interface charge densities. In Figure IV-30, the effective metal workfunction normalized by its value without dielectric insertion, and thus complete FLP, is plotted as a function of the dielectric thickness for the different DIGS density.

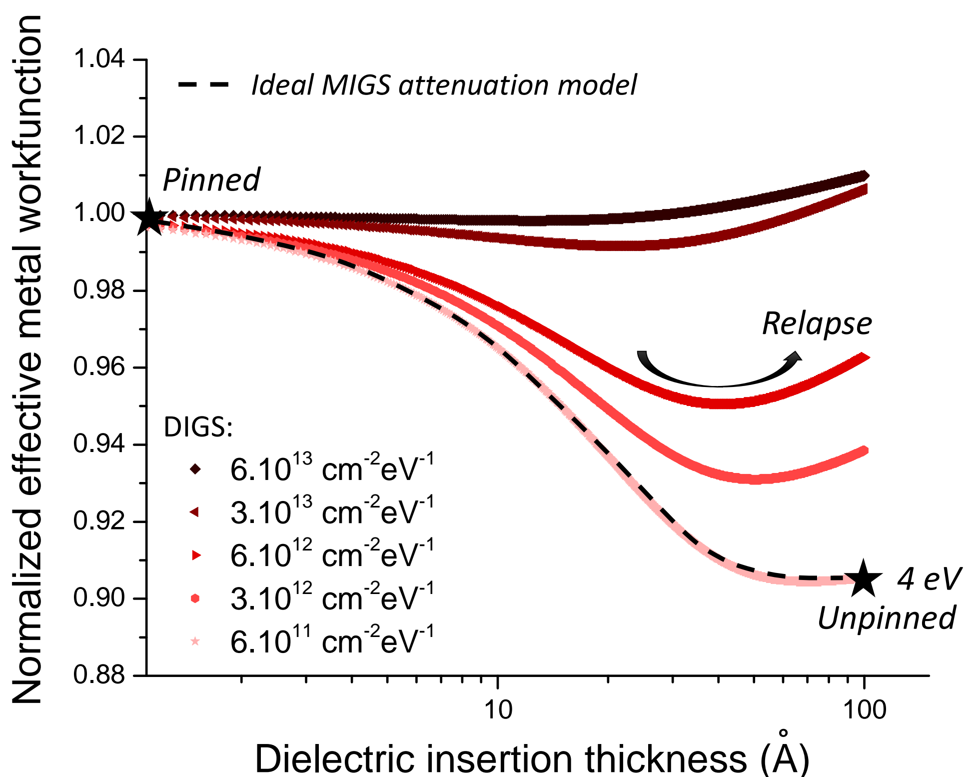


Figure IV-30: Effective metal workfunction as a function of the dielectric insertion considering various DIGS density at the semiconductor/dielectric interface.

Regardless of the DIGS density, the metal always starts from a complete FLP state for ultra-low dielectric thicknesses. One can see that for low DIGS densities, the variation of the effective metal workfunction is close to the trend predicted by an ideal MIGS attenuation model (dashed line). Then for a thick enough dielectric, the FLP is totally mitigated, the effective workfunction tends towards the ideal one (4 eV) making such a contact suitable for n-type Si.

Nevertheless, when the parasitic gap states are dominated by the DIGS rather than the MIGS, one can see that after a first decrease of the effective metal workfunction a relapse is observed. When considering a negligible tunneling resistance in the TiO_2 layer, such a variation would lead to a bell-shaped curve for p-type substrates and thus could explain the experimental results of Figure IV-29.

It seems that the contribution of DIGS and MIGS to the Fermi level pinning has still to be investigated since the ideal MIGS model attenuation fails to explain particular trends like the bell-shaped curve.

IV.6 Chapter conclusions

In Chapter IV, dielectrics insertions for MIS contacts are studied through the prism of their electrical properties.

Transmission Line Model and Cross Bridge Kelvin Resistor measurements are performed in order to probe MS and MIS contacts. Aiming at probing different type of dielectrics, Al_2O_3, HfO_2 and TiO_2 are implemented. As presented in Chapter II, based on theoretical band offsets considerations, whereas Al_2O_3 and HfO_2 are expected to generate significant tunnel resistance for both holes and electrons, TiO_2 seems to be a suitable candidate for MIS applications. However, Chapter III shows that important redistributions of elements might occur in the considered stack and thus that the electrical results could be far from expected.

In this context, direct electrical characterizations can be considered as the ultimate criterion to evaluate an insertion efficacy. First, all the transport properties are evaluated without assuming any theoretical physical parameters such as the band offsets of the dielectrics. Moreover, measurements are performed on structures presenting processing constraints similar to the ones one would encounter when implementing these contacts on a device. Therefore, the resulting MIS contacts, submitted to parasitic effects such as substrate re-oxidation or metal induced scavenging, closely reflect the expected performance when defining these contacts during a MOSFET fabrication flow.

In this work, it is found that the parasitic phenomena such as substrate re-oxidation or insertion degradation lead to a significant discrepancy between the expected performance of a contact and the one it actually presents.

Although TiO_2 is *a priori* a promising dielectrics, it is found that contact based on this dielectric feature poor properties regardless of the metallization. In the case of TiN/Ti metallization, the degradation is attributed to the dilution of the oxygen in the 30 nm thick Ti [*Yu_2015*]. In the TiN/TiO_2/Si contacts, an even higher contact conductivity lessening is observed. As presented in Chapter III, the insertion stability expected with the withdrawal of the Ti capping metal is actually not achieved. The tremendous degradation can thus be attributed to the formation of a SiO_x layer to the detriment of the TiO_2 one.

In terms of electrical properties, the Al_2O_3 is eventually found to be the dielectric presenting the best results. An effective gain compared to the MS reference is obtained on p-Si achieving ρ_c=9.5x10^{-8} Ω.cm².

The electrical results also raise unanswered questions. First, when characterizing Al_2O_3-based contacts, the behaviors of the contact resistivities as a function of the dielectric thickness are nearly equivalent regardless of the metallization in direct contact with the Si. Considering the difference of ideal metal workfunction of Ti and TiN presented in sub-section IV.3.3, it would have seemed logical to obtain a large increase (resp. decrease) of the contact resistivity on n-Si (resp. p-Si) when passing from Ti to TiN when mitigating the FLP. Such behavior could be explained by considering that the dielectric does not alleviate the FLP but induces a FLP at another value [*Lin_2012*].

Additionally, when characterizing TiO_2-based contacts to p-Si, a bell-shaped curve is observed when plotting the contact resistivity as a function of the dielectric insertion thickness. Although such dependence has seldom been reported in the past, similar results can be found in [*Roy_2012*]. Such behavior being not predicted by the classical MIGS model can however be obtained by simulation when introducing DIGS at the dielectric/Si interface.

Therefore it seems that the contributions of DIGS and MIGS to the Fermi level pinning have still to be investigated as well as the mechanisms occurring during FLP mitigation.

IV.7 References

Bethe_1942 **H. A. Bethe;** MIT Radiation Lab Report, No. 43-12; 1942

Berger_1972 **H. H. Berger**; *Models for Contacts to Planar Devices*; Solid-State Electronics, Vol. 15; 1972

Chang_1971 **C. Y. Chang, Y. K. Fang and S. M. Sze**; *Specific Contact Resistance Of Metal-Semiconductor Barriers*; Solid-State Electronics, Vol. 14; 1971

Finetti_1984 **M. Finetti, A. Scorzoni and G. Soncini**; *Lateral Current Crowding Effects on Contact Resistance Measurements in Four Terminal Resistor Test Patterns*; Electron Device Letters, Vol. 5; 1984

Ghegin_2016 **E. Ghegin**; *Development of Si-microelectronics compatible ohmic contacts on III-V surfaces in the frame of Silicon Photonics*; Ph. D. Thesis, Paris Diderot University; 2016

Gupta_2013 **S. Gupta, P. P. Manik, R. K. Mishra, A. Nainani, M. C. Abraham and S. Lodha;** *Contact resistivity reduction through interfacial layer doping in metal-interfacial layer-semiconductor contacts*; Journal of Applied Physics, Vol. 113; 2013

Jayant Baliga_2010 **B Jayant Baliga**; *Advanced Power MOSFET Concepts*; Springer; 2010

Lima_2012 **L. P. B. Lima, J. A. Diniz, I. Doi and J. Godoy Fo**; *Titanium nitride as electrode for MOS technology and Schottky diode: Alternative extraction method of titanium nitride work function*; Microelectronics Engineering, Vol. 92; 2012

Lin_2012 **J.-Y Jason Lin, A. M. Roy and K. C. S**; *Reduction in Specific Contact Resistivity to n+ Ge Using TiO_2 Interfacial Layer*; IEEE Electron Device Letters, Vol. 33; 2012

Loh_1987 **W. M. Loh, S. E. Swirhun, T. A. Schreyer, R. M. Swanson and K. C. Saraswat**; *Modeling and Measurement of Contact Resistances*; Transactions on Electron Devices, Vol. 34; 1987

Lujan_2002 **G. S. Lujan, T. Schram, L. Pantisano, J. C. Hooker, S. Kubicek, E. Rohr, J. Schuhmacher, O. Kilpelä, H. Sprey, S. De Gendt and K. De Meyer**; *Impact of ALCVD and PVD Titanium Nitride Deposition on Metal Gate Capacitors*; 32th European Solid-State Device Research Conference; 2002

Manik_2012 **P. P. Manik, R. K. Mishra, V. P. Kishore, P. Ray, A. Nainani, Y.-C. Huang, M. C. Abraham, U. Ganguly and S. Lodha**; *Fermi-level unpinning and low resistivity*

in contacts to n-type Ge with a thin ZnO interfacial layer; Applied Physics Letters, Vol. 101; 2012

Matsuhashi_1994 **H. Matsuhashi and S. Nishikawa**; *Optimum Electrode Materials for Ta_2O_5 Capacitors for High- and Low-Temperature Processes*; Japanese Journal of Applied Physics, Vol. 33; 1994

Monch_1990 **W. Monch**; *On the physics of metal-semiconductor interfaces*; Reports on Progress in Physics, Vol. 53; 1990

Nishimura_2008 **T. Nishimura, K. Kita and A. Toriumi**; *A Significant Shift of Schottky Barrier Heights at Strongly Pinned Metal/Germanium Interface by Inserting an Ultra-Thin Insulating Film*; Applied Physics Express, Vol. 1; 2008

Ono_2002 **M. Ono, A. Nishiyama and A. Toriumi**; *A simple approach to understanding measurement errors in the cross-bridge Kelvin resistor and a new pattern for measurements of specific contact resistivity*; Solid-States Electronics, Vol. 46; 2002

Proctor_1983 **S. J. Proctor, L. W. Linholm and J. A. Mazer**; *Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity*; Transactions on Electron Devices, Vol. 30; 1983

Ramaswamy_2008 **D. V. N. Ramaswamy**; *Material and Electrical Characterization of TiN/SiO_2 Gate Stacks*; Ph. D. Thesis, Arizona State University; 2008

Reeves_1982 **G. K. Reeves and H. B. Harrison**; *Obtaining the Specific Contact Resistance from Transmission Line Model Measurements*; IEEE Electron Device Letters, Vol. 3; 1982

Robertson_2002 **J. Robertson**; *Band structures and band offsets of high K dielectrics on Si*; Applied Surface Science, Vol. 190; 2002

Roy_2012 **A. M. Roy**; *Tunneling Contacts for Novel Semiconductor Devices*; Thesis, Stanford University; 2012

Schreyer_1986 **T. A. Schreyer and K. C. Saraswat**; *A Two-Dimensional Analytical Model of the Cross-Bridge Kelvin Resistor*; Electron Device Letters, Vol. 7; 1986

Stavitski_2007 **N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, B. K. Boksteen, A. Y. Kovalgin and R. A. M. Wolters**; *Cross-Bridge Kelvin Resistor (CBKR) Structures for Measurement of Low Contact Resistances*; Technology Foundation STW; 2007

Sze_1964 **S. M. Sze, C. R. Crowell, and D. Kahng**; *Photoelectric Determination of the Image Force Dielectric Constant For Hot Electrons in Schottky Barriers*; Journal Of Applied Physics, Vol. 35; 1964

Wright_2007 **J. S. Wright, R. Khanna, L. F. Voss, L. Stafford, B. P. Gila, D. P. Norton, S. J. Pearton, F. Ren and I. Kravchenko**; *Thermally Stable Novel Metal Contacts on Bulk, Single-Crystal n-type ZnO*; ECS transactions, Vol. 6; 2007

Chapter V
General conclusions

V.1 Impact of MIS contacts on advanced MOSFETs nodes 214
V.2 Practical ultra-thin dielectric implementation 215
V.3 Effective electrical properties of MIS contacts 215
V.4 Prospects 216
V.5 References 218

As a consequence of the MOSFET miniaturization trend followed by the industry, parasitic elements are becoming prevalent. In this framework, reducing the contact resistivity appears essential to maintain future nodes performance. Nevertheless, Fermi Level Pinning (FLP) occurring at the metal/semiconductor interface hinders a proper optimization of its electrical properties and leads to significant contact resistivity. According to recent academic research, Metal/Insulator/Semiconductor (MIS) contacts have emerged as potential candidates to ensure the reduction of access resistance for future nodes.

So far, most of the MIS contacts studies were performed in a non-industrial environment and were more aiming at a proof of concept rather than implementing MIS or MIIS contacts in existing manufactured products with all their fabrication constraints.

Consequently, no attention had been so far dedicated to the efficiency of the dielectric insertion as a function of the doping concentration of the addressed semiconductor. Studies based on relatively lowly doped substrates exhibit high dielectric insertion efficacy whereas doping concentration needs to be high in most of the manufactured products.

Additionally, when processing wafers containing both NMOS and PMOS, contacts to n- and p-type semiconductor have to be made. Therefore the solution selected to address the contact resistivity reduction should be fit for both polarities of substrate while preferably not leading to a substantial increase of process complexity. However, most of the studies presented in the state-of-the-art focused on unipolar contacts optimization with no particular insight on co-integration.

Finally, all the studies were performed so far in the static regime while it seems to be relevant for digital applications to evaluate the impact on time-dependent MOSFET performance when using MIS contacts.

Therefore, the work of this thesis consists in:

- Analyzing the optimal co-integration scheme of MIS contacts on n- and p-type semiconductors presenting relatively high doping concentration.
- Evaluating the impact such contacts have on advanced MOSFETs nodes.
- Implementing a MIS contact module in an industrial or semi-industrial environment using materials commonly found in advanced microelectronics.
- Gauging the effective electrical properties of MIS contacts.

V.1 Impact of MIS contacts on advanced MOSFETs nodes

In Chapter II, the study of the MIS contacts effective impact on aggressively scaled transistor DC and AC performance is carried out. Performing 1-D analytical modeling of MS and MIS, it is shown that no optimal single-insertion single-metallization co-integration on n- & p-Si can be found. This issue arises from two main origins.

On the one hand, the basic idea of using MIS contacts being to mitigate the Fermi level pinning, the effective metal work function tends to the ideal one. Then, in order to induce a low Schottky barrier height on n- and p-Si respectively, the chosen metallization has to be an n- and p-metal respectively. Therefore a single-metallization scheme cannot be considered in order to address simultaneously both polarities.

On the other hand, the tunneling resistance induced by a given dielectric is not the same for electrons and holes. While the resistance seen by the former is proportional to the dielectric conduction band offset to Si, the one seen by the latter is linked to the valence band offset. Considering dielectric properties from the state-of-the-art, it seems not possible to find an insertion inducing a low tunneling resistance for both types of carriers. Even more, no insertion is identified in this work as a suitable candidate to improve contact on p-Si. Finally the optimal configuration is found to be a dual-"insertion" (respectively low CBO insertion and no insertion) and a dual-metallization (respectively n- and p-metals). Based on the generated I-V characteristics, this configuration would be Zr/TiO_2/n-Si and Pt/p-Si.

Evaluating the impact of MS and MIS contacts on the MOSFETs DC performance, the optimal contact on p-Si is found to be roughly performing above ideal 10^{-8} Ω.cm² ohmic contact while the optimal MIS junctions on n-type Si is equivalent to a 10^{-9} Ω.cm² ohmic contact.

Finally, it is highlighted that the shunt capacitor induced by a dielectric insertion on the conduction path has a significant impact on time-dependent performance, allowing an extra improvement beyond the 10^{-9} Ω.cm² ideal case.

A simulation strategy is presented as a first approach to screen the potential candidates for MIS contacts application from a theoretical point of view. Whereas using modeling allows to gather fundamental understanding of such contacts, DC and AC SPICE simulations enable to link stand-alone contact I-V characteristics with their impact on MOSFETs performance. Nevertheless, modeling and simulations are based on assumptions and hypotheses which can be overly simplistic.

V.2 Practical ultra-thin dielectric implementation

In Chapter III, it appears that stable ultra-thin dielectric insertions are not easily achieved.

Working with the classical metallization used in the IC chips manufacturing industry, namely W/TiN/Ti, the presence of Ti at the vicinity of the dielectric insertion leads to its degradation (if using Al_2O_3 and TiO_2). Additionally, as demonstrated in Chapter II, in order to enhance the performance of the MIS contacts, the polarity of the metal should match the one of the substrate. Thus in order to address n-type Si, metal with a workfunction even lower than that of the Ti should be chosen (in Chapter II, Zr is used for the simulations). Known to be reactive, such metals might lead to a higher degradation of the dielectric.

Moreover, such a scavenging effect is enhanced by any subsequent thermal budget. In a full CMOS process, the wafers undergone the steps required to fabricate the metal interconnects. These steps are typically performed around 400°C. Then a MIS contact dedicated to CMOS industry should be unaltered by such thermal budget. In this work, the deposition of W is performed at 440°C and is found high enough to enhance the elements redistribution through the stacks.

Finally, as presented in the preliminary study of ALD based dielectrics, a regrowth of the substrate oxide seems unavoidable when working at 300°C on a H-passivated surface. This layer has undoubtedly a significant impact on the electrical transport and should be tackled.

V.3 Effective electrical properties of MIS contacts

In Chapter IV, dielectrics insertions for MIS contacts are studied through the prism of their measured electrical properties.

Transmission Line Model and Cross Bridge Kelvin Resistor measurements are implemented in order to probe MS and MIS contacts. Aiming at probing different type of dielectrics, Al_2O_3, HfO_2 and TiO_2 are implemented. As presented in Chapter II, based on theoretical band offsets considerations, whereas Al_2O_3 and HfO_2 are expected to generate significant tunnel resistance for both holes and electrons, TiO_2 seems to be a suitable candidate for MIS applications. However, Chapter III showed that important redistributions of elements might occur in the considered stacks and thus that the electrical results could be far from expected.

Therefore, direct electrical characterizations can be considered as the ultimate figure of merit to evaluate an insertion efficacy. First, all the transport properties are evaluated without assuming any

theoretical physical parameters such as the band offsets of the dielectrics. Moreover, the measurements are performed on structures presenting processes constraints similar to the ones one would encounter when implementing these contacts on a device. Therefore, the resulting MIS contacts, having undergone parasitic effects such as substrate re-oxidation or metal induced scavenging, closely reflect the performance expected when defining these contacts during a MOSFET fabrication flow.

In this work, it is found that the parasitic phenomena such as substrate re-oxidation or insertion degradation lead to a significant discrepancy between the expected performance of a contact and its effective one.

Although TiO_2 seems *a priori* a promising dielectrics, it is found that contacts based on this dielectric feature poor properties regardless of the metallization. In the case of TiN/Ti metallization, the degradation is attributed to the dilution of the O in the overlaying Ti. In the TiN/TiO_2/Si contacts, an even higher contact conductivity lessening is observed. As presented in Chapter III, the insertion stability expected with the withdrawal of the Ti capping metal is actually not achieved. The tremendous degradation can thus be attributed to the formation of a SiO_x layer to the detriment of the TiO_2 one.

In terms of electrical properties, the Al_2O_3 is eventually found to be the dielectric presenting the best results. An effective gain compared to the MS reference is obtained on p-Si achieving ρ_c=9.5x10^{-8} Ω.cm².

V.4 Prospects

From this work, it appears that MIS contact paradigm might not be the best candidate to address the contact resistance issue occurring in advanced CMOS technology. Due to the high level of dopants activation required in this field, the actual efficiency of such contacts is far from the initially expected one. Thus, remaining of great interest, MIS contacts should be considered for other types of substrates and/or other types of applications. From this perspective, the impact of such contacts should be examined in the framework of contact engineering on **lowly doped substrates such as III-V materials or Ge** typically presenting a doping concertation below 5x10^{19} at.cm^{-3} when using conventional techniques [*Lind_2016*], [*Hsu_2016*]. Besides, as presented in Chapter II, MIS contacts also present a shunt capacitor inducing an extra reduction of their impedance when used in the AC regime. Thus, the impact of using MIS contacts should also be examined in the framework of **CMOS for high radio frequency applications**.

However, even if redefining a more suitable field of application, some issues still have to be addressed in order to make the use of MIS contacts realistic.

First, it seems that the contributions of DIGS and MIGS to the Fermi level pinning have still to be investigated as well as the mechanisms occurring during FLP mitigation. Indeed, the comparison of the actual electric behavior of the probed contacts with their expected one raises some yet unanswered questions. When characterizing Al_2O_3-based contacts, the resistivity as a function of the dielectric thickness is nearly independent from the metallization type in direct contact with Si. Considering the difference of ideal metal workfunction of Ti and TiN, it would have seemed logical to obtain a large increase (resp. decrease) of the contact resistivity on n-Si (resp. p-Si) when passing form Ti to TiN and mitigating the FLP. Such behavior could be explained by considering that **the dielectric does not mitigate the FLP but induces a FLP at a different energy value**. Additionally, when characterizing TiO_2-based contacts to p-Si, a bell-shaped curve is observed when plotting the contact resistivity as a function of the dielectric insertion thickness. Although such behavior is no predicted by the classical MIGS model, similar results can be obtained by simulation when introducing **DIGS at the dielectric/Si interface**.

Finally, the simulation methodology developed in Chapter II underlines the **necessity of insertion bandgap engineering** in order to implement dielectrics presenting low tunnel barrier for current carriers. Since considering conventional dielectrics of the state-of-the-art does not enable finding any suitable candidate for p-type semiconductor, a special attention should be paid to develop insertion featuring low valence band offset to the considered substrate. From this perspective, **types of materials emerging in the CMOS field, such as 2-D materials, should be investigated as insertions for MIS contacts**.

V.5 References

Hsu_2016 **W. Hsu, X. Wang, F. Wen, Y. Wang, A. Dolocan, T. Kim, Emanuel Tutuc and S. K. Banerjee;** *High Phosphorus Dopant Activation in Germanium Using Laser Spike Annealing*; IEEE Electron Device Letters, Vol. 37; 2016

Lind_2016 **A. G. Linda, H. L. Aldridge, C. Hatem, M. E. Law and K. S. Jones**; *Review—Dopant Selection Considerations and Equilibrium Thermal Processing Limits for* n^+-$In_{0.53}Ga_{0.47}As$; Journal of Solid State Science and Technology, Vol. 5; 2016

PUBLICATIONS

1st author

- **Ultra-thin dielectric insertions for contact resistivity lowering in advanced CMOS: Promises and challenges**; J. Borrel, L. Hutin, D. Kava, R. Gassilloud, N. Bernier, Y. Morand, F. Nemouchi, M. Gregoire, E. Dubois and M. Vinet; Japanes Journal of Applied Physics, Vol. 56, 2017
- **Ultra-thin dielectric insertions for contact resistivity lowering in advanced CMOS: promises and challenges**; J. Borrel, L. Hutin, D. Kava, R. Gassilloud, N. Bernier, Y. Morand, F. Nemouchi, M. Gregoire, Emmanuel Dubois and M. Vinet; Japanese Journal of Applied Physics, to be published
- **Modelling of Fermi Level Pinning Alleviation with MIS Contacts – n- & p-MOSFETs Co-Integration Considerations – Part 1 & 2**; J. Borrel, L. Hutin, O. Rozeau, M.-A. Jaud, S. Martinie, M. Gregoire, E. Dubois and M. Vinet; *IEEE Transactions on Electron Devices*, Vol. 63 Issue 9, 201

Co-author

- **Detecting Unintended Schottky Junctions and Their Impact on Tunnel FET Characteristics;** L. Hutin, C. Le Royer, R. P. Oeflein, S. Martinie, J. Borrel, V. Delaye, J.-M. Hartmann, C. Tabone, M. Vinet; *IEEE Transactions on Electron Devices*, Vol. 63, Issue 6, June 2016
- **Investigation of Ambipolar Signature in SiGeOI Homojunction Tunnel FETs;** L. Hutin, .P. Oeflein, J. Borrel, S. Martinie, C. Tabone, C. Le Royer, M. Vinet; *Solid State Electronics*, Vol. 115, 20
- **Ferroelectric Control of Magnetic Domains in Ultra-Thin Cobalt Layers**; Z. Huang, I. Stolichnov, A. Bernand-Mantel, J. Borrel, S. Auffret, G. Gaudin, O. Boulle, S. Pizzini, L. Ranno, L. Herrera Diez, N. Setter; *Applied Physics Letters*, Vol. 103, 2013

CONFERENCES

1st author

- **Considerations on Fermi-Depinning, Dipoles and Oxide Tunneling for Oxygen-based Dielectric Insertions in Advanced CMOS Contacts**; J. Borrel, L. Hutin, H. Grampeix, E. Nolot, E. Ghegin, P. Rodriguez, C. Tabone, F. Allain, J.-P. Barnes, Y. Morand, F. Nemouchi, M. Gregoire, E. Dubois, M. Vinet; *IEEE Silicon Nanoelectronics Workshop*, 2016
- **At 10nm node, what is the AC impact of dielectric insertions in contact initially meant to decrease the DC contact resistivity?**; J. Borrel, L. Hutin, O. Rozeau, M.-A. Jaud, S. Martinie, E. Dubois, M. Vinet; *IEEE Semiconductor Interface Specialists Conference*, 2015
- **Considerations for efficient contact resistivity reduction via Fermi Level depinning - impact of MIS contacts on 10nm node nMOSFET DC characteristics**; J. Borrel, L. Hutin, O. Rozeau, P. Batude, T. Poiroux, F. Nemouchi, M. Vinet*; IEEE Symposium on VLSI Technology*, 2015

Invited

- **Metal/Insulator/Semiconductor Contacts for Ultimately Scaled CMOS Nodes: Projected Benefits and Remaining Challenges**; J. Borrel, L. Hutin, H. Grampeix, E. Nolot, M. Tessaire, G. Rodriguez, Y. Morand, F. Nemouchi, M. Gregoire, E. Dubois, M. Vinet; *International Workshop on Junction Technology*, 2016

Co-author

- **High Performance CMOS FDSOI Devices Activated at Low Temperature**; L. Pasini, P. Batude, J. Lacord, M. Casse, B. Mathieu, B. Sklenard, F. Piegas Luce, J. Micout, F. Mazen, P. Besson, E. Ghegin, J. Borrel, R. Daubriac, L. Hutin, D. Blachier, D. Barge, S. Chhun, A. Cros, J.-P. Barnes, Z. Saghi, V. Delaye, N. Rambal, V. Lapras, J. Mazurier, O. Weber, F. Andrieu, C. Fenouillet-Beranger, Q. Rafhay, G. Ghibaudo, F. Cristiano, M. Haond, F. Bœuf, M. Vinet, *IEEE Symposium on VLSI Technology*, 2016
- **Challenges of 3D VLSI-CoolCube™ process with p-Ge-OI and n-InGaAs-OI for ultimate CMOS nodes**; F. Nemouchi, L. Hutin, H. Boutry, P. Rodriguez, E. Ghegin, J. Borrel, Y. Morand, S. Kerdiles, P. Batude, M. Vinet; *IEEE Silicon Nanoelectronics Workshop*, 2015
- **Junction technology outlook for sub-28nm FDSOI CMOS**; L. Hutin, O. Rozeau, V. Carron, J.-M. Hartmann, L. Grenouillet, J. Borrel, F. Nemouchi, S. Barraud, C. Le Royer, Y. Morand, C. Plantier, P.Batude, C. Fenouillet-Béranger, H. Boutry, T. Ernst, M. Vinet; *International Workshop on Junction Technology*, 2014

DISTINCTION

Nicollian Award – Best Student Paper Award at IEEE SISC 2015