N° d'ordre : 42338

THESE

Présentée à l'Université de Lille 1
École Doctorale Sciences Pour l'Ingénieur

Pour obtenir le grade de :

DOCTEUR DE L'UNIVERSITE

Spécialité : SCIENCES ET TECHNOLOGIES DE L'INFORMATION ET DE LA COMMUNICATION

Par

Chinni Vinay Kumar

"AlGaSb/InAs vertical Tunnel Field Effect Transistors for low power electronics"

Soutenance le 28 mars 2017 devant la commission d'examen

Membres du jury :

M. Rachid Driad	Chef de groupe III-V technologie, Fraunhofer IAF	Rapporteur
M. Bassem Salem	Chargé de recherche CNRS, LTM Grenoble	Rapporteur
Mme Cristell Maneux	Professeur, IMS, Université de Bordeaux	Examinatrice
Mme Virginie Nodjiadjim	Ingénieure de recherche, III-V Lab, Palaiseau	Examinatrice
M. Roland Teissier	Directeur de recherche CNRS, IES, Montpellier	Examinateur
M. Ludovic Desplanque	Maître de Conférences, Université de Lille 1	Co-encadrant
M. Mohammed Zaknoune	Directeur de Recherche, IEMN	Co-directeur
M. Xavier Wallart	Directeur de Recherche, IEMN	Directeur de thèse

ACKNOWLEDGEMENTS

I express my sincere gratitude to **Dr. Ludovic Desplanque**, **Dr. Mohammed Zaknoune**, and **Dr. Xavier Wallart** for their invaluable guidance during the course of my PhD at IEMN. Their limitless patience and unconditional support have made my stay thoroughly enjoyable and cherishable for the rest of my life. In particular, I would always remember the guidance provided by Dr. Desplanque in making me understand the theory of Tunnel FET device, helping in device characterization and providing me epitaxial structures promptly. I am also equally grateful to Dr. Zaknoune, who, using all his experiences, helped me in fabricating the full-length TFET devices, a first of the kind that has been ever developed in the lab. Finally, without the overall guidance and support of Dr. Wallart, I would not have finished my thesis on time.

I also take this opportunity to extend my sincere thanks to technical fraternity of IEMN clean room. Especially, Marc Francois and François Vaurette for training and helping me in lithography, Pascal Tilmant for providing me the necessary training for resists, Christophe Boyaval for training me in using SEM, Laurence Morgenroth for deposition of gate oxide in ALD systems, David Troadec for providing fib-stem images, Christiane Legrand for helping me in using the PECVD and ICP systems, and Dimitri Yareka for training me in using ICP SENTECH system.

I owe special thanks to my dear friends Yoann Leachaux, Matej Pastorek, Sri Saran, Maria Fahed, Alexandre Bucamp, Alain Fadje, Salman Nadar, Mohammad Ridaou, Aurelien, and Mohammad Samnouni for inspiring me and providing me a wonderful atmosphere in IEMN laboratory. Outside the realm of IEMN, I am also grateful to my very good friends Betty, Remi, Gangadhar, Rakibul, Vikram, Diwakar, Satya, Ragavendra and Arun who all supported me emotionally and made my stay in Lille a memorable one.

Last but not the least, I would like to take this opportunity to thank my family for their constant encouragement, love, and sacrifice that had made this work possible.

Résumé

Depuis environ une dizaine d'années, la poursuite de la miniaturisation des dispositifs microélectroniques silicium se heurte au problème de l'augmentation de la densité de puissance consommée dans les dispositifs car la réduction de la tension d'alimentation n'a pas suivi celle des dimensions. Cela est inhérent au mécanisme thermo-ionique d'injection des porteurs dans les transistors de type MOSFET et conduit à envisager un mécanisme d'injection des porteurs différent, basé sur l'effet tunnel. Pour être efficace, ce type d'injection doit s'accompagner de l'introduction de semi-conducteurs III-V à faible masse effective et petite bande interdite. Parmi ces derniers, l'hétérojonction (Al)GaSb/InAs semble prometteuse grâce à la faible masse effective des électrons dans InAs et à la possibilité de passer d'un alignement des bandes de type 'échelon' à 'brisé'.

Ce travail de thèse porte sur la fabrication de transistors à effet tunnel (TFETs) à base d'héterostructures (Al)GaSb/InAs élaborées par épitaxie par jets moléculaires. L'influence des paramètres matériaux et géométriques sur les performances du transistor a été évaluée à l'aide des simulations utilisant le logiciel Silvaco. Un procédé technologique complet de fabrication de diodes et transistors verticaux de taille nanométrique a ensuite été développé et a conduit à la réalisation d'un transistor vertical à effet tunnel sur substrat GaAs. La caractérisation électrique de ce dispositif a révélé un courant dans l'état ON de 433 μA/μm à $V_{DS} = V_{GS} = 0.5$ V. A basse température, une pente sous le seuil de 71 mV/décade et un rapport ON/OFF de 6 décades ont été obtenus. Ce compromis à l'état de l'art entre courant ON et capacité de commutation démontre que le TFET à base de l'hétérojonction (Al)GaSb/InAs pourrait constituer une alternative de choix pour les technologies futures après optimisation de l'empilement de grille.

Abstract

Silicon microelectronics is facing a power consumption crisis for around ten years since the scaling of the supply voltage has not followed that of the transistor dimensions. This is mainly due to the inherent limits of the silicon MOSFETs, based on the thermionic injection mechanism of the carriers. Going to a tunneling injection mechanism is therefore very appealing but, to be efficient, this should go along with the introduction of low effective mass and small bang gap III-V semiconductors. Among them, the (Al)GaSb/InAs heterojunction is very attractive due to the low electron effective mass in InAs and the ability to tune the band alignment from staggered to broken gap which eventually results in large tunneling current densities.

In this PhD work, the fabrication of tunnel field effect transistors (TFETs) based on AlGaSb/InAs heterostructures grown by molecular beam epitaxy is investigated. First the impact of the basic material and geometrical parameters on the device performances has been simulated using Silvaco TCAD software. A complete technological process for the fabrication of nanoscale vertical tunnel diodes and tunneling transistors has then been developed and has led to the achievement of a vertical TFET on a GaAs substrate. The electrical characterization of this device has been carried out exhibiting an ON-current of 433 μA/μm at V_{DS} = V_{GS} = 0.5 V. At low temperature, a subthreshold swing of 71 mV/decade and a 6 decade ON/OFF ratio at 0.1 V are demonstrated. This state-of-the-art trade-off between ON current and switching properties indicates that the (Al)GaSb/InAs TFET may be a valuable solution for beyond CMOS technology after further improvement of the gate stack process.

Table of Contents

List of Figures

Abbreviation List

ALD	Atomic Layer Deposition
BG	Broken-Gap Semiconductor
BGN	Band Gap Narrowing
BTBT	Band-to-Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nano-Tune
CVD	Chemical Vapor Deposition
DC	Direct Current
DOS	Density of States
DI	De-Ionized
EBL	Electron Beam Lithography
EOT	Equivalent Oxide Thickness
FG	Forming Gas
IC	Integrated Circuit
IPA	Isopropyl Alcohol
MBE	Molecular Beam Epitaxy
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NDR	Negative Differential Resistance
NW	Nanowire
PMMA	Poly (Methyl Methacrylate)
PVCR	Peak-to-Valley Current Ratio
RTA	Rapid Thermal Anneal
RIE	Reactive-Ion Etch
SEM	Scanning Electron Microscope
SOI	Silicon-on-Insulator
SRH	Shockley-Read-Hall
SS	Sub-threshold slope
TAT	Trap-Assisted Tunneling
TCAD	Technology Computer-Aided Design

TDD	Threading Dislocation Density
TD	Tunnel diode
TEM	Transmission Electron Microscope
TFET	Tunnel Field-Effect Transistor
WKB	Wentzel-Kramers-Brillouin

Introduction

Historically, the most commonly used transistor in integrated circuits (ICs) is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), based on silicon technology. Complementary MOS (CMOS) circuits use a combination of p-type and n-type MOSFETs to implement digital circuits found in all electronic equipment. The three terminal MOSFET consisting in the gate, drain and source was first fabricated at BELL labs by D. Kahng and M.M. Atalla in 1960 [1] and commercially available in 1964.

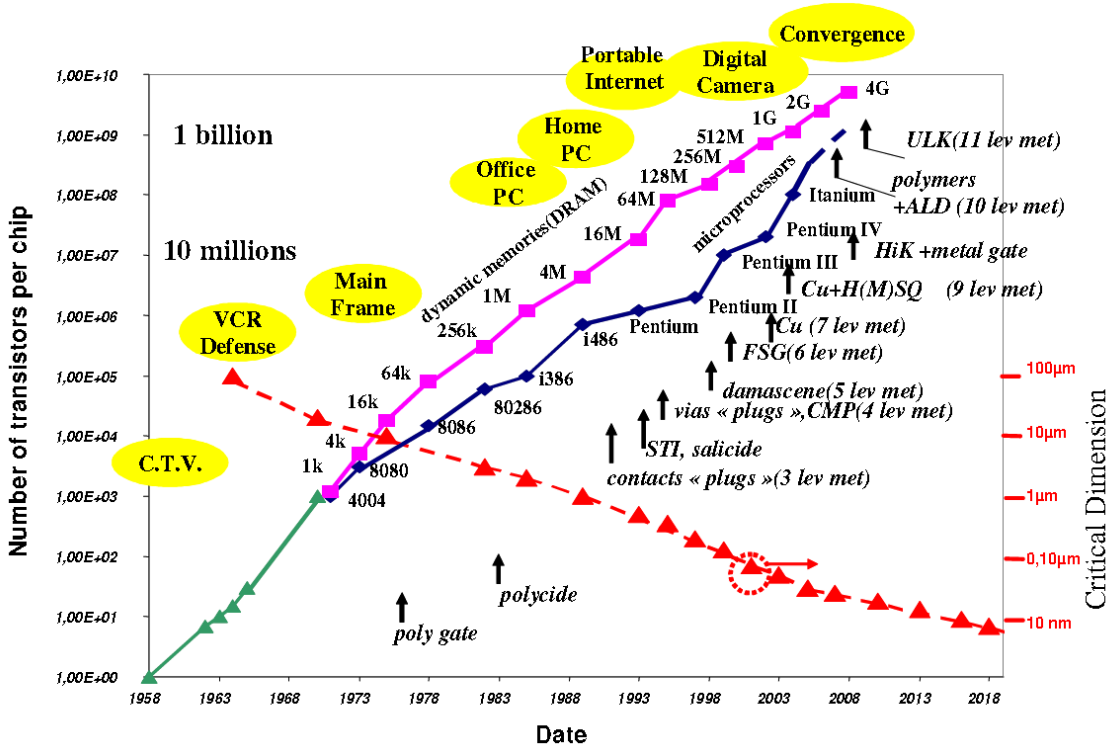


Figure 1: Scaling of transistor over the years following the famous Moore's law, roughly doubling the number of transistors per chip for every 24 months [2].

Scaling of CMOS has achieved an unprecedented success since its invention in 1960 at Bell labs. For more than five decades, MOSFET has been continuously scaled to improve the performances and to add functionalities to the IC. Over the last three decades transistor scaling followed Dennard's voltage scaling principle, which states that all the device dimensions be scaled by 1/k factor while the doping of source and drain regions increased by a factor k [3]. As a result, MOSFET scaling improved the circuit speed and

density along with the addition of more functionalities. With the scaling progressing at an exponential rate, more and more transistors in a given area have been added lowering the manufacturing cost per transistor. Figure 1 shows this trend. However, an emerging problem associated to the scaling of the supply voltage V_{DD} has appeared. The graph in *Figure 2* shows that V_{DD} scaling did not follow the trend of Dennard's scaling law with the technology generation node. Indeed, scaling of V_{DD} and of the threshold voltage V_{TH} have adverse effects (decrease of the gate over drive and on the on-state current, decrease of the Ion/Ioff ratio) due to the carrier transport mechanism based on the thermionic emission principle, leading to limitations of the electrostatic control of the gate over the current flow. This non-scaled V_{DD} leads to the power dissipation problem in the recent technology nodes. One way to address this power consumption problem without sacrificing performance is to increase the switching efficiency, which implies a subthreshold slope (SS) of the device steeper than 60 mV/dec at room temperature, which is a physical limit of the conventional MOSFETs.

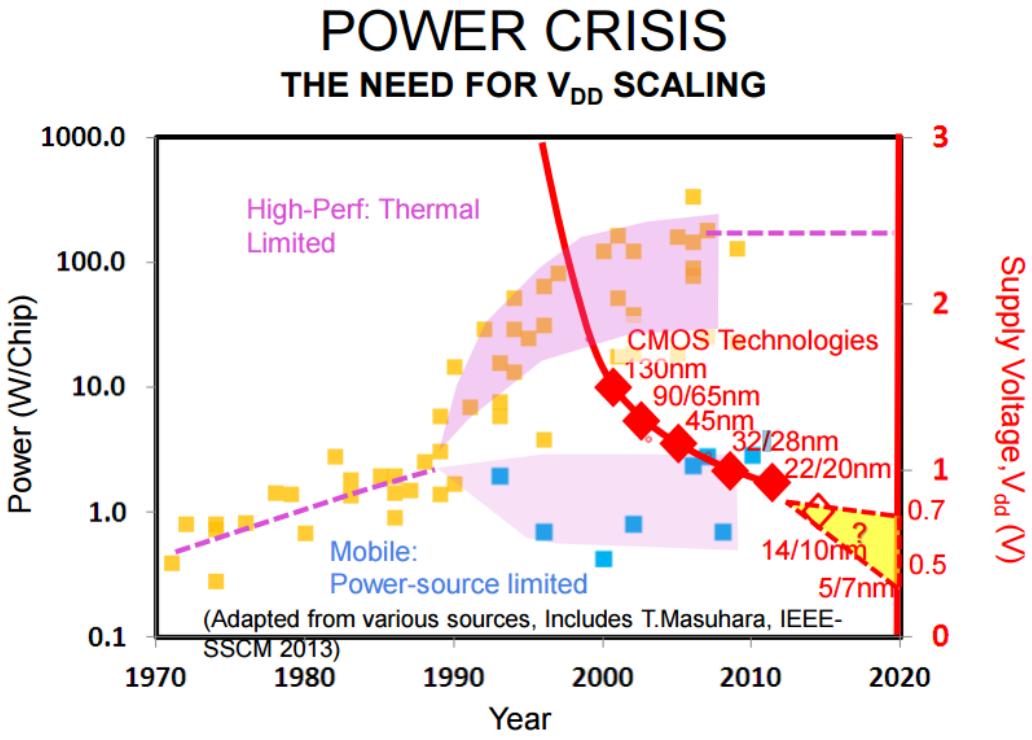


Figure 2: The trend of Power (W/chip) and supply voltage VDD Vs year of a CMOS technology node. (Source: IMEC [4])

There are many alternatives to the MOSFETs to achieve steep SS, which are currently studied. The focus of this work will be on one of them: changing the thermionic injection mechanism of charges into the channel by a tunnel injection mechanism independent of the temperature. This is the working principle of the Tunnel Field Effect Transistor (TFET) in which the carrier transport mechanism is fundamentally different from that in MOSFET and for which a SS lower than 60mV/dec can be expected. The realization of a complete transistor involves many parameters and that is why, as a first step, we will investigate tunnel diodes (TDs) to evaluate material properties.

This manuscript is organized along four chapters.

Chapter 1 provides the motivation for this work, based on the limitations currently being experienced by the MOSFETs in terms of SS. Possible post-MOSFET devices with lower values of swing are discussed and state-of-the-art on the TFETs fabricated within various material systems and architecture is presented. ***At the end we present the main objective of this work, which is to realize a vertical n-TFET in the AlGaSb/InAs material system***.

Chapter 2 presents the operation principles and basic simulation of TFET using the Silvaco software. The parameters such as materials, effective barrier height (E_{beff}) at the tunnel junction, doping variations at source and drain, single and double gate configurations, channel body thickness, effective oxide thickness are varied to get a better insight into the device working.

Chapter 3 details the fabrication process flow for diodes and TFETs that have been developed entirely in the framework of this study.

Chapter 4 discusses the results obtained on the fabricated Tunnel diodes (TDs) and different TFET generations.

Finally, the conclusion suggests some recommendations for future work.

Chapter 1 – Literature review

1.1 Subthreshold Swing of transistor: CMOS limit

The conventional scaling in CMOS technology faced major problems for sub-50nm gate length (L_g), because the operation voltage reduction degrades the sub-threshold leakage current. Figure 3 illustrates that the transition from OFF-state to ON-state is not abrupt and I_{OFF} is not zero in the subthreshold region ($V_{GS} < V_{TH}$). This leads to a leakage or subthreshold current in the OFF-state. In practice, low V_{TH} is desirable to obtain high ON-current while reducing V_{DD}, but high V_{TH} is needed for low OFF-current. This sub-threshold leakage effect slowed down the scaling of the threshold voltage and eventually supply voltage (V_{DD}).

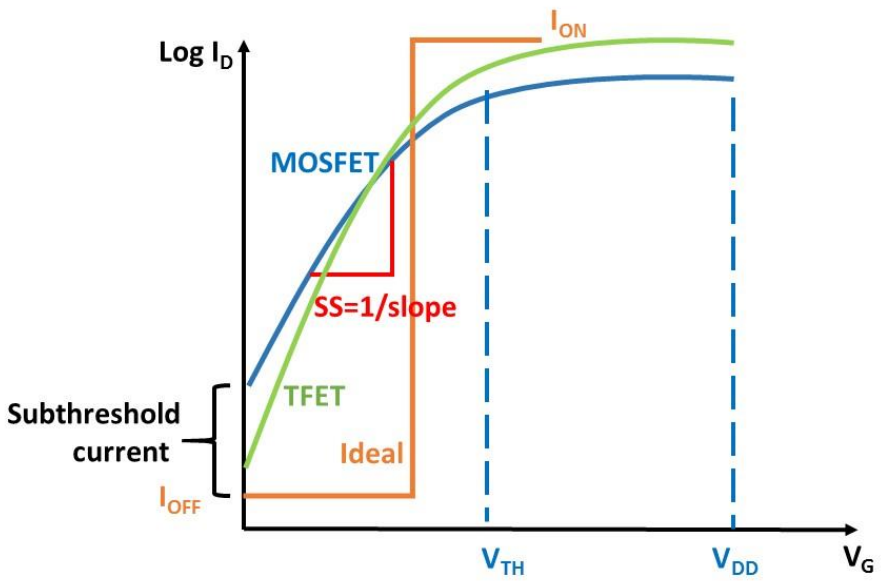


Figure 3: I-V characteristics showing for the MOSFET (blue), TFET (green) in comparison with ideal (orange) I-V characteristics of a transistor.

The subthreshold swing of a MOSFET is defined as the value of the gate voltage (V_G) swing needed for one decade change of the drain current (I_D), usually expressed in millivolts per decade (mV/dec). In Figure 3, the region below the drain current saturation is called subthreshold region. The subthreshold swing (SS) is the inverse of the subthreshold slope of log (I_D) vs V_{GS} and is expressed as [16]:

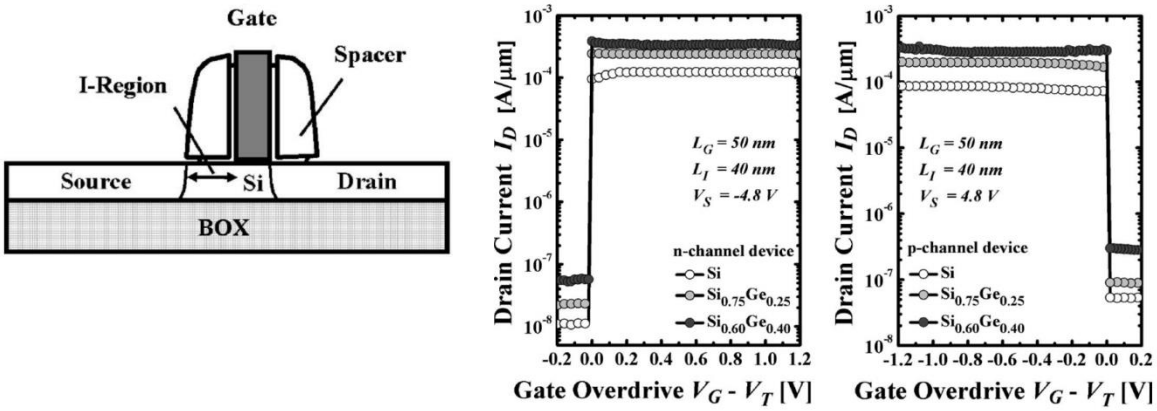
$$SS = \frac{dV_G}{d(log_{10} I_D)} = \ln(10)\frac{k_B T}{q}\left(1 + \frac{C_{dep}}{Cox}\right) \qquad (1.1)$$
$$= \left(\ln(10)\frac{k_B T}{q}\right)(m)$$

where k_B is the Boltzmann constant, T is the temperature, C_{dep} is the depletion capacitance, Cox is the gate oxide capacitance and m is called the body factor. Due to the thermionic nature of the drain current, *SS* is always limited to $2.3k_BT/q$ (=60 mV/decade) at room temperature. Since the *SS* is purely dependent on the transport mechanism of the carriers in the subthreshold regime, achieving steep *SS* lower than 60 mV/decade requires changing the way electrons flow in the device. This is the primary motivation behind Impact-ionization MOSFETS (IMOS), Micro/Nano-Electro-Mechanical FETs (NEMFETs) and Tunnel field effect transistors (TFETs) where the transport mechanism is different from classical silicon based MOSFETs. On the other hand, S. Salahudhin *et al.* [5] proposed a theory on the negative capacitance to increase the surface potential (m<1) in the channel with respect to what is possible in the MOSFET.

1.2 Alternative small Swing devices: Subthreshold slope below 60mV/decade

1.2.1 Impact-ionization MOSFET (I-MOS)

Impact-ionization MOS (I-MOS) is one of the potential electronic device that employs avalanche breakdown to achieve a SS below 10 mV/decade. I-MOS is a gated p^+-i-n^+ structure with a gate partially covering the intrinsic region as shown in Figure 4. Applying a positive gate bias greater than the threshold voltage (Vt) results in an increase of the charge carrier energy. Under the influence of the high electric field the atoms in the lattice are impacted thereby creating more electron-hole pairs. Avalanche breakdown occurs when each carrier produces an electron-hole pair. Since impact-ionization phenomenon is a strong function of the electric field, I-MOS can have a very small subthreshold swing and a high-on current [6].



(a) **(b)**

Figure 4: (a) Schematic of a typical I-MOS structure in which the gate only partially covers the right side of the intrinsic region. (b) Transfer characteristics I_{DS}-V_{GS} of Si and heterostructure SiGe I-MOS with a SS of less than 5 mV/dec for left n-channel I-MOS and right p-channel I-MOS, where source was biased at 4.8V. The above device schematic and characteristics were taken from [7].

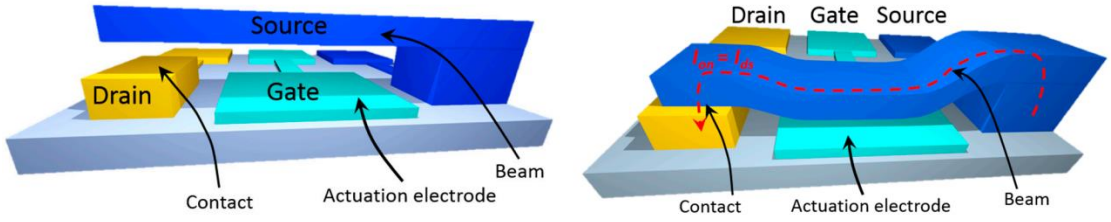
The biggest challenge for the I-MOS is the reduction of the breakdown voltage to enable further scaling of the supply voltage (V_{DD}). Gopalakrishnan *et al.* proposed the use of low band gap materials such as Ge, to lower the breakdown voltage, but experimental demonstration is still lacking [8]. While the supply voltage of 'Si' I-MOS is still higher than for current MOSFETs, Y. Lechaux (Anode group) at IEMN is currently studying III-V based heterojunction I-MOS to lower the supply voltage. Since impact-ionization itself creates hot carriers, this is a matter of concern for repeatability and reliability because hot carriers can go under the gate (into the gate oxide) resulting in threshold voltage shifts and also SS increase of the device. Another major challenge for I-MOS using low band gap materials is the tunneling current.

1.2.2 M/NEMFET (Micro/Nano-Electro-Mechanical FET)

Micro/Nano-electro-mechanical (MEMS/NEMS) relays utilize electrostatic actuation to switch the device from OFF to ON state. The switching behavior is very abrupt and believed to be an excellent choice where the reduction of static power is the main concern. While some MEMS switches are just 2-terminals (2T), which are easy to design

and operate but are limited in terms of applications in circuits, others are 3-terminal (3T) devices. There are many designs available for the 3T relay switch. One of the design is to use a cantilever beam [9] electrostatically "pulled-in" and "pulled-out" as shown in Figure 5 (a). Another possibility is to use a typical MOSFET layout as developed by EPFL. Rhesa *et al.* [10] developed a 4-Terminal (4T) relay to address the shortcomings of 2T and 3T in circuits [11]. In 4T design as shown in Figure 5 (b), the actuated structure is the gate, whose position is controlled by the applied gate-to-body voltage (V_{GB}), as opposed to the gate-to-source (V_{GS}) in the 3T design.

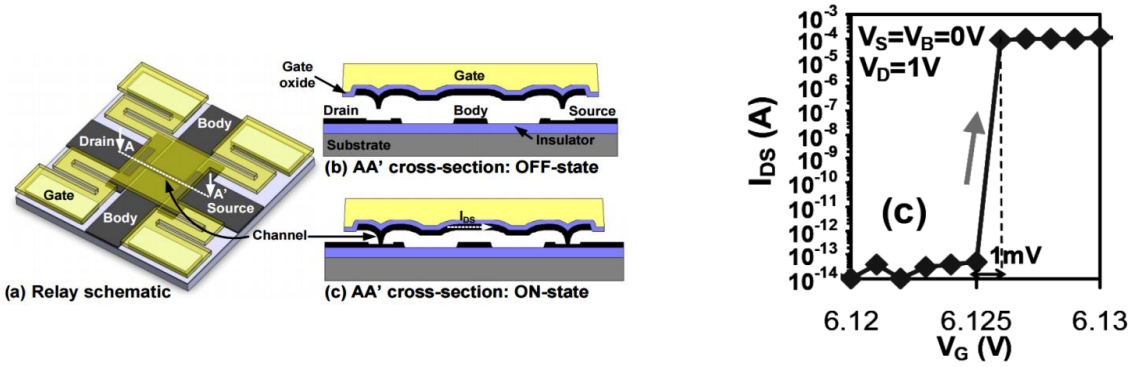
3-Terminal (3T) Relay



OFF STATE **ON STATE**

(a)

4-Terminal (4T) Relay



(b) **(c)**

Figure 5: (a) Schematic showing the operation of cantilever based 3T NEMS switch with source, drain and gate terminals in the OFF state and ON state taken from [9]. *(b) Schematic of 4T relay in OFF and ON states where the gate structure is actuated by V_{GB} and (c) corresponding I_{DS}-V_{GB} of the 4T relay showing SS less than 1mV/decade taken from* [11].

MEMS and NEMS are interesting because of their nearly zero leakage current in the OFF state, abrupt SS and very high I_{ON}. Their main disadvantages include speed and mechanical reliability where millions of switches should be electrostatically operated thousands or millions of times without failure and also high parasitic capacitance at high frequencies [12].

1.2.3 Ferroelectric gate dielectric FET

Another possibility to reduce the subthreshold swing below 60 mV/decade is by using a ferroelectric insulator in place of the conventional gate oxide insulator [5], because a ferroelectric insulator provides an effective negative capacitance (NC) which allows overcoming the Boltzmann limit. The negative capacitance phenomenon can be explained by considering the first term of the equation (1.1), which is denoted as m.

$$m = 1 + \frac{C_{Dep}}{C_{ins}} \qquad (1.2)$$

The body-factor (m) is always larger than 1 in MOSFETs, because of the voltage divider rule in conventional capacitors. Thus SS cannot be less than 60 mV/decade in MOSFETs. However, if 'm' could be made less than one, that will lead to an overall SS less than 60 mV/decade [13]. To achieve this, a negative capacitance insulator (ferroelectric) is connected in series with the semiconductor capacitor as shown in Figure 6. However, these ferroelectric-gate transistors suffer from low field effect mobility and further research has to be conducted [14].

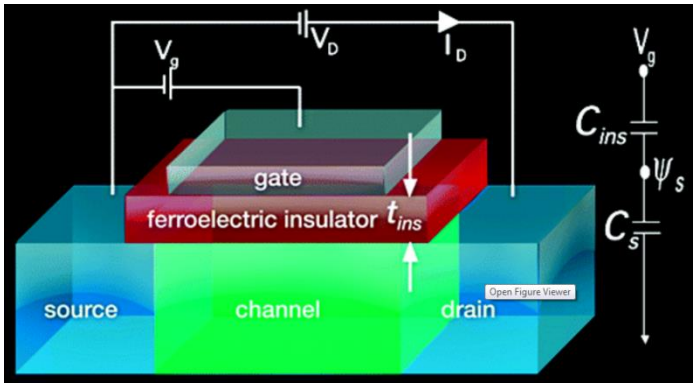


Figure 6: A conventional FET structure with the gate insulator replaced by a ferroelectric insulator, this means channel see a larger voltage than the actual due to the negative capacitance. Next to the FET structure is the schematic showing the insulator (ferroelectric) capacitor and the semiconductor capacitor connected in series like in a MOSFET. The above picture is taken from [5].

1.3 Introduction to the Tunnel Field effect transistor

The tunnel FET also called TFET, is also considered as a potential device for MOSFET replacement for low-power applications. As the carriers tunnel through the barrier, they offer a potential for steep subthreshold swing at a very low OFF state current. Since the tunneling takes place in a very small region of less than 5nm, the gate lengths can be scaled to a distance of tunneling barrier width, which is less than 5nm for III-V materials. The drain current in TFET is independent of the kT/q thermal factor unlike in MOSFET, which makes it possible to achieve subthreshold swing lower than 60 mV/dec.

In theory, TFETs make use of band-to-band-tunneling (BTBT) to establish current flow. BTBT of carriers will occur when a heavily doped p-n junction is polarized under reverse bias and the electric field is high enough of the order of 10^6 V/cm. Under reverse bias, available electrons on the source (p) side tunnel through the narrow barrier and fill the available states in the conduction band of the drain (n) side resulting in a Zener current flow.

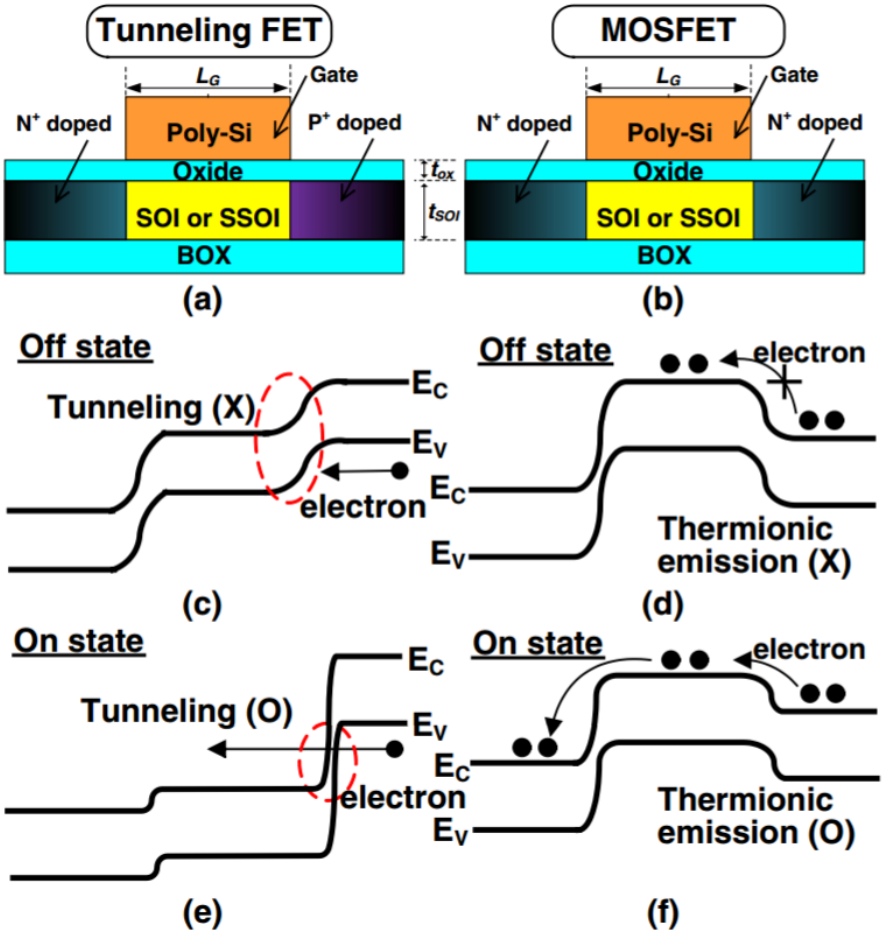


Figure 7: (a), (b) Schematic of a three terminal TFET and MOSFET device structure, (c), (d) Scheme showing the barriers that carriers see for a TFET and MOSFET in Off state and (e),(f) Scheme showing the carrier injection mechanism of a TFET and MOSFET in On state [15].

So, TFETs are gated p^+-i-n^+ diodes operated in reverse bias with a gate aligned with the intrinsic zone. With almost similar 3-terminals like in an nMOSFET, an nTFET consists of a p^+ -region as source, an i-region as channel, and a n^+-region acting as the drain. Like in a MOSFET, the gate voltage (V_{GS}) controls the charge in the channel by modulating the height of the barrier. In MOSFETs, charge carriers go over the barrier, while in TFETs they pass through the barrier as shown in Figure 7. When no V_{GS} is applied, the tunneling barrier width is wide enough to impede carrier tunneling: this is the OFF-state. When a positive V_{GS} is applied on the gate, the intrinsic zone bands are pushed down, and the tunneling

barrier width starts to become thinner, thus allowing the majority charge carriers available on the source side to pass through it towards the empty states in the conduction band of the intrinsic zone. As V_{GS} is further increased, the tunneling probability increases which results in a maximum tunneling current, defining the ON state of the TFET. For nTFET, the majority charge carriers are electrons, with the electrons passing from the p^+ source to the i-channel and drained through the n^+ drain. Conversely, for pTFET, n^+ source allows for injection of holes into the channel. Negative V_{GS} and V_{DS} are applied to turn the pTFET 'ON'.

The principle of operation of a TFET is Zener tunneling. As shown in Figure 7 when a V_{GS} is applied to the gate, the channel bands are pushed down, which reduces the tunneling barrier width and thus allowing the tunneling of carriers from source p+ side to the intrinsic region. The tunneling barrier width is the most important parameter that determines the tunneling current i.e. the drain current of the TFET I_D. The tunneling of electrons is formally understood by the transmission tunneling probability of electron through a potential barrier. Careful examination of Figure 8(a) indicates that the potential barrier is of triangular shape as shown in Figure 8 (b).

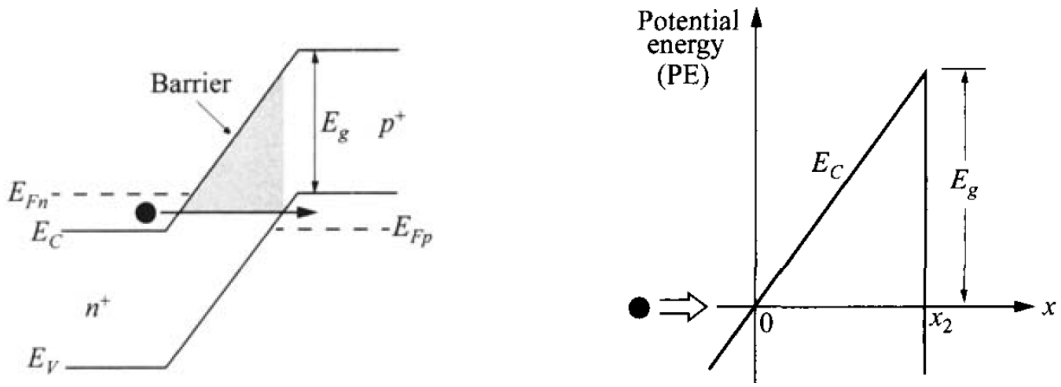


Figure 8: (a) Band-to-band-tunneling mechanism under reverse bias and (b) a triangular potential profile [16].

The transmission tunneling probability across a triangular potential barrier can be analytically solved using the WKB (Wentzel-Kramers-Brillouin) approximation [17], which is obtained as

$$T_t \approx exp - \left(\frac{4\sqrt{2m^*}\, E_g^{\frac{3}{2}}}{3q\hbar\varepsilon} \right) \tag{1.3}$$

where m^* is the effective carrier mass, E_g is the band gap of the material, ε is the electric field at the junction.

Equation 1.3 is a general expression for BTBT transmission. When it comes to the tunneling transistors, I_{BTBT} (I_D) can be obtained with the aid of Figure 9. In a tunneling transistor, at a constant V_D and with the increase/decrease of the gate voltage (V_G), the energetic difference (Δϕ) between the conduction band on one side and the valence band on the other side decreases/increases along with λ, since the slope of the energy bands are changed under the influence of the gate electric field. The electric field (ε) in Eq. 1.3 can be replaced with (Δϕ + Eg)/λ, which gives

$$I_{BTBT} \alpha\, T_t \approx exp - \left(\frac{4\lambda\sqrt{2m^*}\, E_g^{\frac{3}{2}}}{3q\hbar\left(\Delta\phi + E_g\right)} \right) \tag{1.4}$$

$\Delta\phi$ is the energy window over which tunneling takes place, E_g is the band gap of the material, λ is a tunneling screening length and m^* is the effective carrier mass.

From the above equation, two important material parameters allow increasing the transmission tunneling probability: a low carrier effective mass and a small semiconductor bandgap.

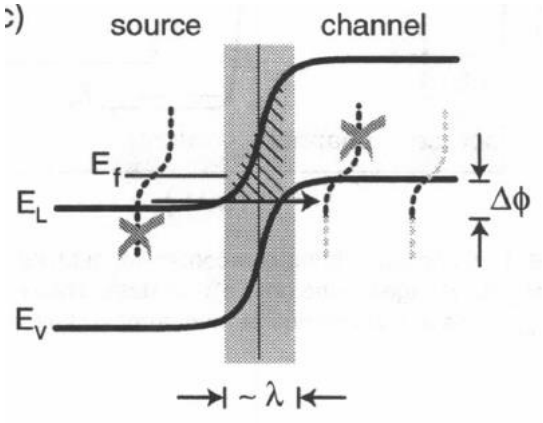


Figure 9: Energy band cross section of a TFET showing a triangular barrier [18].

1.4 TFET State-of-the-art

1.4.1 Material systems

1.4.1a Si/SiGe TFETs

The main objective of the TFET is to outperform CMOS transistors in terms of I_{ON} at low V_{DD} with SS below 60 mV/decade and a large I_{ON}/I_{OFF} ratio. The TFET with sub-60mV/decade on Si was first experimentally demonstrated by Choi *et al.* with an OFF-current in the pA/μm range and an ON-current of 12.1 μA/μm [19]. It has been later showed that BTBT current is significantly enhanced by using strained Si [20] and SiGe [21], because the strain induced heterojunction reduces the band gap. Although significant improvements were seen using band gap engineered Si, SiGe [22], high-k metal gate stack, dopant segregated tunneling junctions [23] and nanowire scaling (NW) to improve electrostatics [24], the ON-current (without degrading the OFF-current) values obtained are far from the desired values compared to MOSFETs. The low ON-current in Si is attributed to the large and indirect band gap, which leads to a wide tunneling barrier for the carriers.

1.4.1b III-V TFETs

Because of the limitation of Si-based TFETs to achieve large drive currents to compete with CMOS, III-V semiconductors have been considered due to their smaller and direct band gaps, low effective-mass and possibility of band alignment engineering to increase BTBT. To date, there have been many III-V combinations investigated using

different architectures. This section reviews the experimental III-V-based TFETs that had been already demonstrated by various groups.

Homo-junction TFETs

Homojunction TFETs consist of a similar semiconductor material for the source, channel and drain. The most experimentally demonstrated III-V homojunction TFET is based on the $In_xGa_{1-x}As$ ternary alloy with 'x' varying from 0.53 to 1 and the corresponding band gap (E_g) from 0.74 eV (x=0.53) to 0.35 eV (x=1). The first $In_{0.53}Ga_{0.47}As$ TFET published by Mookerjea *et al.* with a vertical mesa structure, achieved an ON-current of 20 $\mu A.\mu m^{-1}$ with a minimum SS (SS_{min}) of 150mV per decade [25]. Later Zhao *et al.* improved the ON-current to 50 $\mu A.\mu m^{-1}$ with a SS_{min} around 90mV per decade by inserting an $In_{0.7}Ga_{0.3}As$ (E_g = 0.59 eV) pocket at the source-channel interface [26], [27]. Recently, Noguchi *et al.* [28] and Alian *et al.* [29] achieved a SS of 60 mV per decade on planar InGaAs TFETs, which are the best SS achieved on III-V-based homo-junction TFETs. Table 1 summarizes some of the best experimental results in the literature based on III-V homojunctions.

Table 1: III-V-based homojunction N-TFETs

HOMOJUNCTION N-TFETs						
Ref.	**P^{++}/i**	**architecture**	**High-*k* (EOT nm)**	***I_{ON} ($\mu A/\mu m$)***	***I_{ON}/I_{OFF}***	***SS (mV/dec)***
[25]	$In_{0.53}Ga_{0.47}As$	mesa	Al_2O_3 (2.25nm)	20 *V_{GS}=2.5V; V_{DS}=0.75V*	$>10^3$	153
[28]	$In_{0.53}Ga_{0.47}As$	Planar ('Zn' dopant diffusion)	Al_2O_3 (1.4nm)	10 *V_{GS}=1V; V_{DS}=1V*	$>10^6$	64
[29]	$In_{0.7}Ga_{0.3}As$	Planar ('Zn' dopant diffusion)	Al_2O_3/HfO_2 (1.2nm)	7 *V_{GS}=1.0V; V_{DS}=0.2V*	$>10^6$	60
POCKET HOMOJUNCTION N-TFETs						
[30]	$In_{0.53}Ga_{0.47}As$/ $In_{0.7}Ga_{0.3}As$ (pocket)	mesa	Al_2O_3 (1.45nm)	8 *V_{GS}=1.0V; V_{DS}=0.75V*	$>10^4$	60
[26]	$In_{0.7}Ga_{0.3}As$/ $In_{0.53}Ga_{0.47}As$	mesa	HfO_2 (1.2nm)	50 *V_{GS}=2V; V_{DS}=1.05V*	$>10^4$	93

From the Table 1, it is noteworthy that a thin intrinsic $In_{0.7}Ga_{0.3}As$ as a pocket improves the tunneling probability and also SS compared to the homojunction TFET. Although, III-V homojunction TFETs with pockets exhibit lower SS and higher drive current compared to Si or even SiGe, the drive current has to be further improved to compete with standard CMOS.

Hetero-junction TFETs

Another strategy to further increase the *ON*-current is to use a heterostructure at the tunneling junction. Heterojunction, where the source material is different from the channel and drain, allows for a variety of tunnel barriers to be engineered. There are three types of band alignments possible with the heterojunction: Straddling gap (type I), staggered gap (type II) and broken gap (type III) (Figure 10). Different types of heterojunction TFETs fabricated by various groups are highlighted in Table 2.

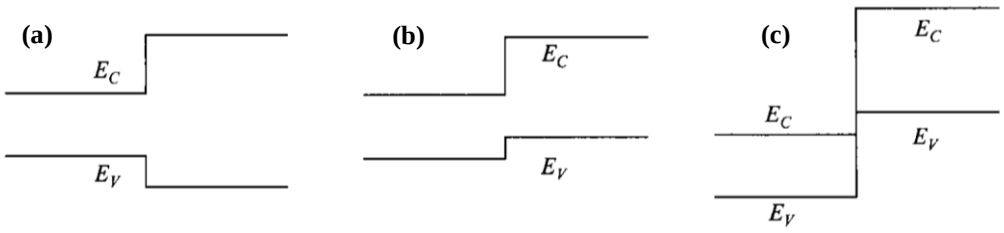


Figure 10: Schematics of heterojunctions. (a) straddling gap (type-I), (b) staggered gap (type-II), and (c) broken gap (type-III).

Table 2: Types of Heterojunction band alignments formed using various material systems

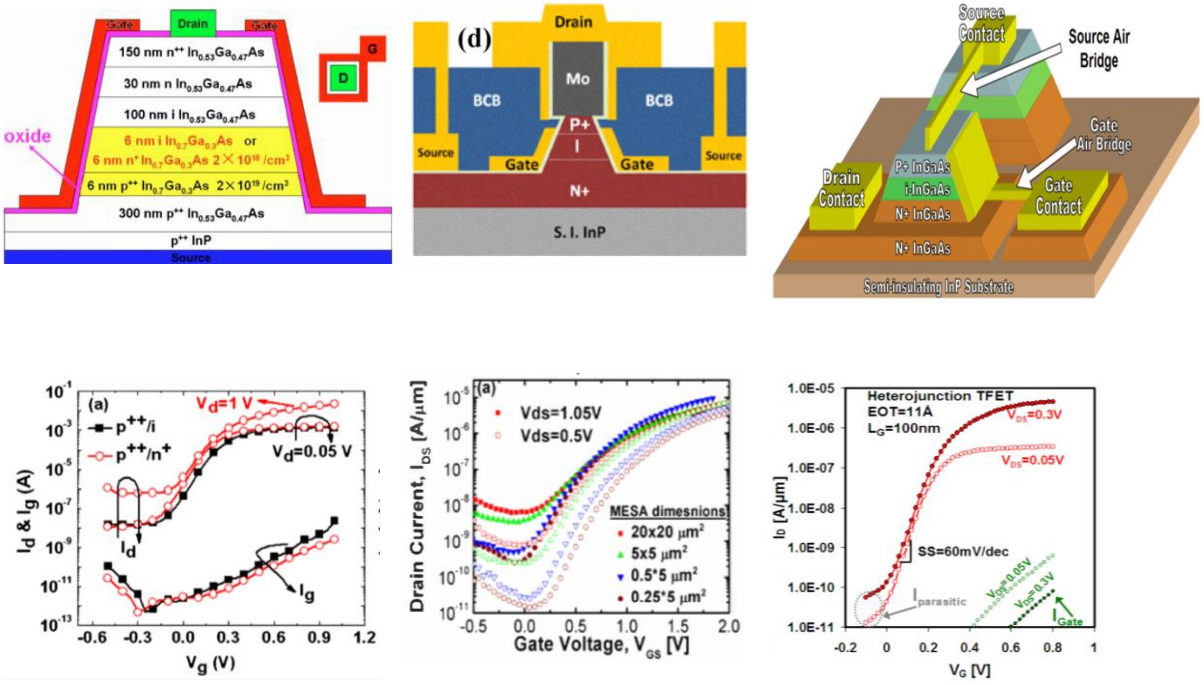
Material system	**Heterojunction type**	**Reference**
$InP/In_{0.53}Ga_{0.47}As$	Straddled	[31]
$GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$	staggered	[32]
$GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$	staggered	[33]
$GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$	staggered	[34], [35]
$GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$	staggered	[36]
$Al_{0.45}Ga_{0.55}Sb/InAs$	staggered	[37]
InAs/Si	staggered	[38], [39], [40]
GaSb/InAs	Broken	[41]

1.4.2 TFET Device architectures

Like for any other device, the electrical characteristics differ widely by the architecture and the fabrication methodologies used for the fabrication of TFETs.

1.4.2a Vertical mesa

Vertical mesa design utilizes dry etching or wet chemical etching [27] or even both to define the channel mesa [25]. A single gate or a two-sided gate is placed on the mesa sidewall as shown in the schematics of Figure 11 to modulate the carriers inside the channel. In the vertical mesa design, the off-state leakage is caused by a Schockley-Read-Hall generation-recombination current, so Mookerjea *et al.* proposed to scale the mesa dimensions to reduce the effect of defects in reverse bias [42].



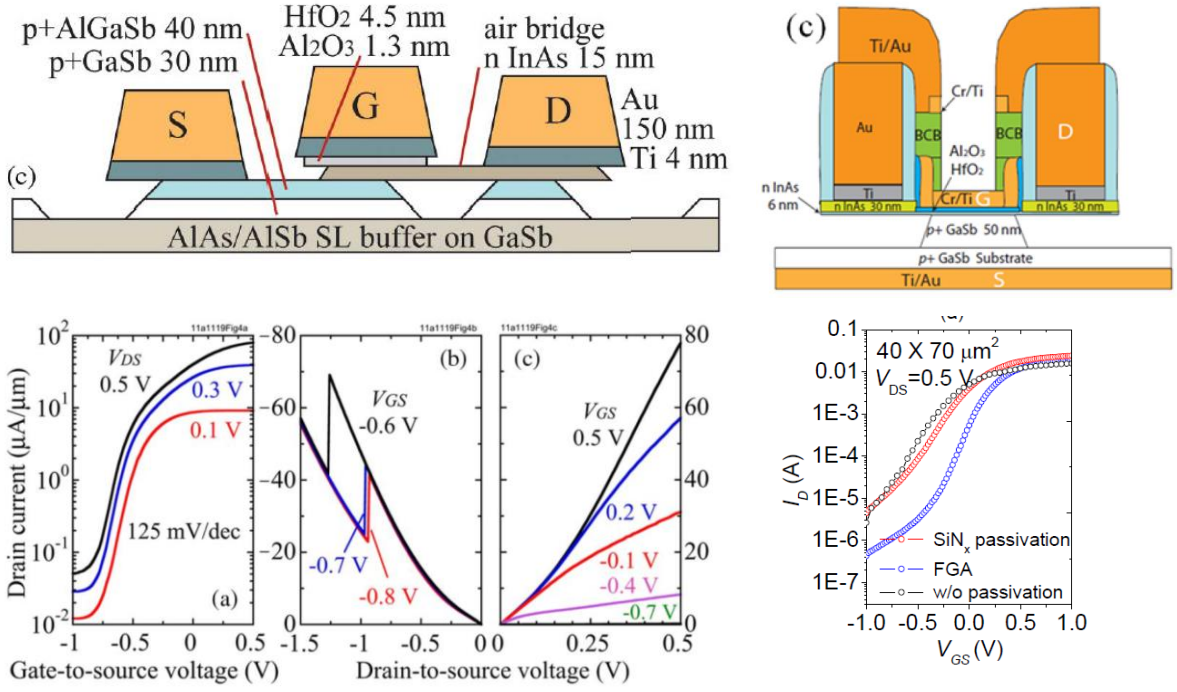
(a) **(b)** **(c)**

Figure 11: Cross-section schematics of a vertical mesa TFET fabricated by (a) the University of Texas [43], *(b)Penn state* [25], *(c) Intel* [30]. *In the vertical mesa TFET, the gate is placed on the channel (i) sidewall of an etched mesa.*

The main challenge for the fabrication of vertical mesa TFETs is to perfectly align the gate on the channel region. The gate overlap or underlap can result in a reduced electrostatic control of the charges in the channel.

1.4.2b TFETs with Tunneling Normal to the Gate

The University of Notre dame demonstrated a TFET with the gate electric field aligned to the tunneling direction. In this design a very thin top epitaxial layer is grown forming the drain and channel. The gate is placed on top of the n^+ drain layer to modulate the tunneling junction. The source is then selectively wet etched to separate the source and the channel forming an air bridge underneath the channel as shown in Figure 12 (a). While the tunneling current maybe enhanced, this design has several disadvantages. There is a significant series resistance inherent to the design [37]. In order to mitigate the series resistance impact, another design named gate recess process (see Figure 12 (b)), demonstrated by Notre dame, involves a higher doped drain layer under the drain contact [41]. This approach achieved a record ON state-current of 180 µA/µm, however the SS is still limited by the interface trap density (D_{it}) at the oxide/semiconductor interface and trap-assisted tunneling (TAT) at the tunneling junction. Moreover, this architecture does not allow easy gate down scaling.



(a) **(b)**

Figure 12: Cross-section schematics of the $Al_xGa_{1-x}Sb$/InAs based TFET fabricated at Notre dame University: (a) Air bridge structure with tunneling in-line with the gate field [37], *(b) another design with heavily doped drain contact* [41].

1.4.2c Nanowire TFETs

The vertical nanowire is an ideal geometry for TFET application since a wrapped gate-all-around (GAA) cylindrical nanowire channel allows the best electrostatic control of the carriers. The cross-section schematic of a recently fabricated vertical nanowire heterojunction TFET is shown in Figure 13. Nanowires are formed either by nanowire-growth assisted by a catalyst [44], [39] or top-down approach using the digital dry etch technique [45].

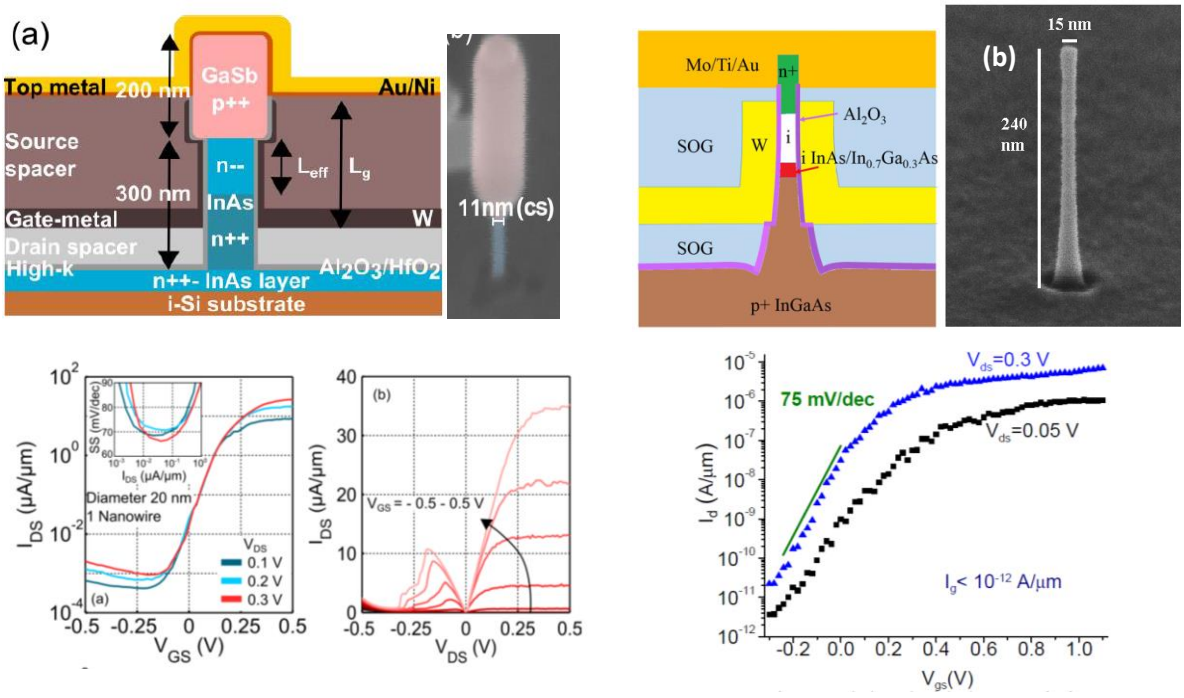
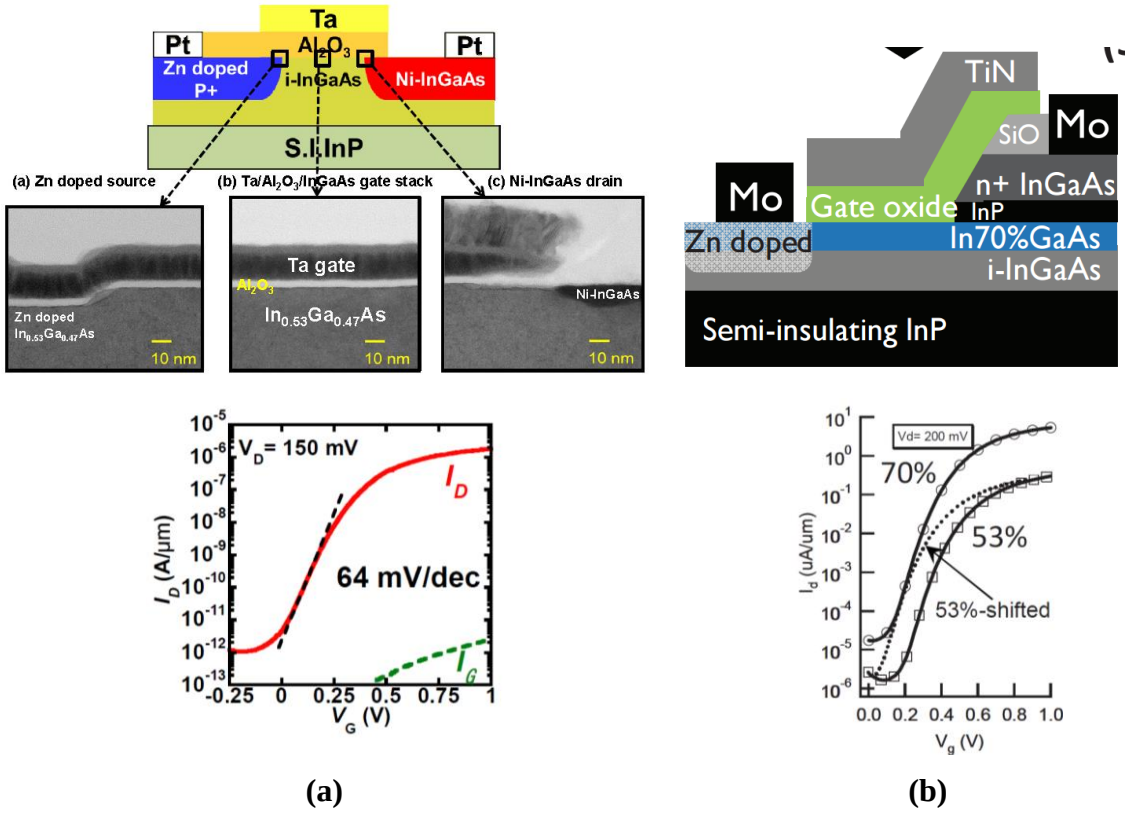


Figure 13: Schematics and a SEM image of a fabricated nanowire processed in (a) bottom-up approach (nanowire growth) [44], *(b) top-down approach (digital dry-etch technique)* [45]. *Very small diameter has been achieved in both cases, but the quality and processing conditions are yet to be optimized.*

Both approaches exhibited an improved SS compared to the vertical mesa architecture because of the aggressively scaled dimensions. But from a manufacturing stand point the digital dry etch approach may be easier than the nanowire growth since the existing plasma tools in the industry can be easily adapted to the dry etch processing.

1.4.2d Lateral TFETs

From a cross-sectional point of view, the lateral TFET architecture is almost similar to the classical MOSFET ones due to its planar nature. For the InGaAs TFET fabricated by Noguchi *et al*. the source (p^+) is formed by Zn-diffusion to form the defect-less p^+/i tunnel junction [28]. With extremely steep doping profiles and a good quality tunneling interface, trap-assisted tunneling (TAT) is reduced which results in a steep SS. Figure 14 shows a schematic of the lateral TFET fabricated at the University of Tokyo and IMEC.



(a) **(b)**

Figure 14: Cross sectional schematic of a lateral TFET with the source regions formed by 'Zn' diffusion developed at (a) the University of Tokyo [28], *(b) IMEC* [29].

1.4.3 Overview of Heterojunction TFETs

Table 3 shows that several heterojunction TFETs achieve a large ON state current over a gate swing of 0.5 V. The large ON state current, however, appeared at the stake of the I_{ON}/I_{OFF} ratio. While the GaSb/InAs (Sb) material system is the best performing so far in terms of high ON state current at V_{DS}=0.5 V, it exhibits an I_{ON}/I_{OFF} ratio less than 10^3 in all

the cases. The absence of steep SS less than 60 mV/dec is noteworthy, except in the work from Tomioka *et al.*[40] and is typically attributed to the high D_{it} at the semiconductor-channel/oxide interface and trap-assisted-tunneling (TAT). Mookerjea *et al*. reported that continued reduction of the mesa area and effective oxide thickness (EOT) can reduce the leakage effects and improve the SS [42]. This statement is confirmed in the case of nanowires: indeed Zhao *et al.* [45] and Memisevic *et al.* [44] fabricated a thin nanowire TFET with a diameter less than 20nm in two different approaches and achieved a SS close to 60 mV per decade. However, the ON state current is lower in this case.

The experimental results show that further EOT and body thickness scaling within the InAs/$Al_xGa_{1-x}Sb$ material system allows for further improvement of the ON state current and lower SS and offers a promising perspective for replacing CMOS.

Table 3: Heterojunction TFETs

HETEOJUNCTION N-TFETs						
Ref.	**P^{++}/i**	**architecture**	**High-*k* (EOT nm)**	***I_{ON} ($\mu A/\mu m$)***	***I_{ON}/I_{OFF}***	***SS_{min} (mV/dec)***
[46]	InP/$In_xGa_{1-x}As$ (x->1.0-0.53)		Al_2O_3/HfO_2 (1.3nm)	20 *V_{GS}=1V; V_{DS}=0.5V*	$>10^6$	93
[47]	$Al_{0.4}Ga_{0.6}Sb$/InAs		Al_2O_3/HfO_2 (1.6nm)	78 *V_{GS}=0.5V; V_{DS}=0.5V*	$>10^3$	125
[41]	GaSb/InAs		Al_2O_3/HfO_2 (1.3nm)	**180** *V_{GS}=0.5V; V_{DS}=0.5V*	$>10^3$	200
[48]	GaSb/AlSb/InAs (quantum well)		10nm-ZrO2	16 *V_{GS}=0.4V; V_{DS}=0.4V*	10^3	194
[34]	$GaAs_{0.35}Sb_{0.65}$/ $In_{0.7}Ga_{0.3}As$ (High HetroJ)	Mesa	Al_2O_3/HfO_2 (1.75nm)	135 *V_{GS}=2.0V; V_{DS}=0.5V*	$>10^4$	169
[49]	$GaAs_{0.18}Sb_{0.82}/In_{0.9}Ga_{0.1}As$	mesa	Al_2O_3/HfO_2 (2nm)	**740** *V_{GS}=2.0V; V_{DS}=0.5V*	10^2	>500
[35]	$GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$	mesa	HfO_2 (1.2nm)	130 *V_{GS}=2.0V; V_{DS}=0.5V*	$>10^5$	105
NANOWIRE HETEROJUNCTION N-TFETs						
		diameter				

[45]	InGaAs/InAs	50nm (top-down approach)	Al_2O_3 (1.2nm)	*0.27* V_{GS}*=0.3V;* V_{DS}*=0.3V*	$>10^2$	75
[50]	GaSb/InAs (Sb)	70nm (bottom-up approach)	Al_2O_3 (1.3nm)	***140*** V_{GS}*=0.3V;* V_{DS}*=0.5V*	10^2	320
[51]	GaSb/InAs	45nm (bottom-up approach)	Al_2O_3/HfO_2 (1.4nm)	*5* V_{GS}*=0.5V;* V_{DS}*=0.5V*	10^2	130
[44]	GaSb/InAs	20nm (bottom-up approach)	Al_2O_3/HfO_2 (1.4nm)	*35* V_{GS}*=0.5V;* V_{DS}*=0.5V*	$>10^2$	68
[40]	Si/InAs	30nm (bottom-up approach)	$Hf_{0.8}Al_{0.2}O_x$ (1.4nm)	*1* V_{GS}*=0.5V;* V_{DS}*=1.0V*	$>10^6$	21

1.4.4 Complementary TFETs

While heterostructure TFETs offer the best alternative possibility for logic applications, the demonstration of low SS p-TFET integration results are lagging. Many challenges exist for the integration of complimentary TFET (C-TFET) on a 'Si' platform. Selective area growth epitaxial technology [52] or nanowire template growth [53] could be possible solutions to realize C-TFET on the same wafer. Recently, Pandey *et al*. demonstrated record performance of n-TFET and p-TFET on the same material system as shown in Figure 15 (a) [54] for the InGaAs/GaAsSb material system. Similar approach has been proposed within the '6.1Å' family in the context of the ANR Samba project (Figure 15(b)).

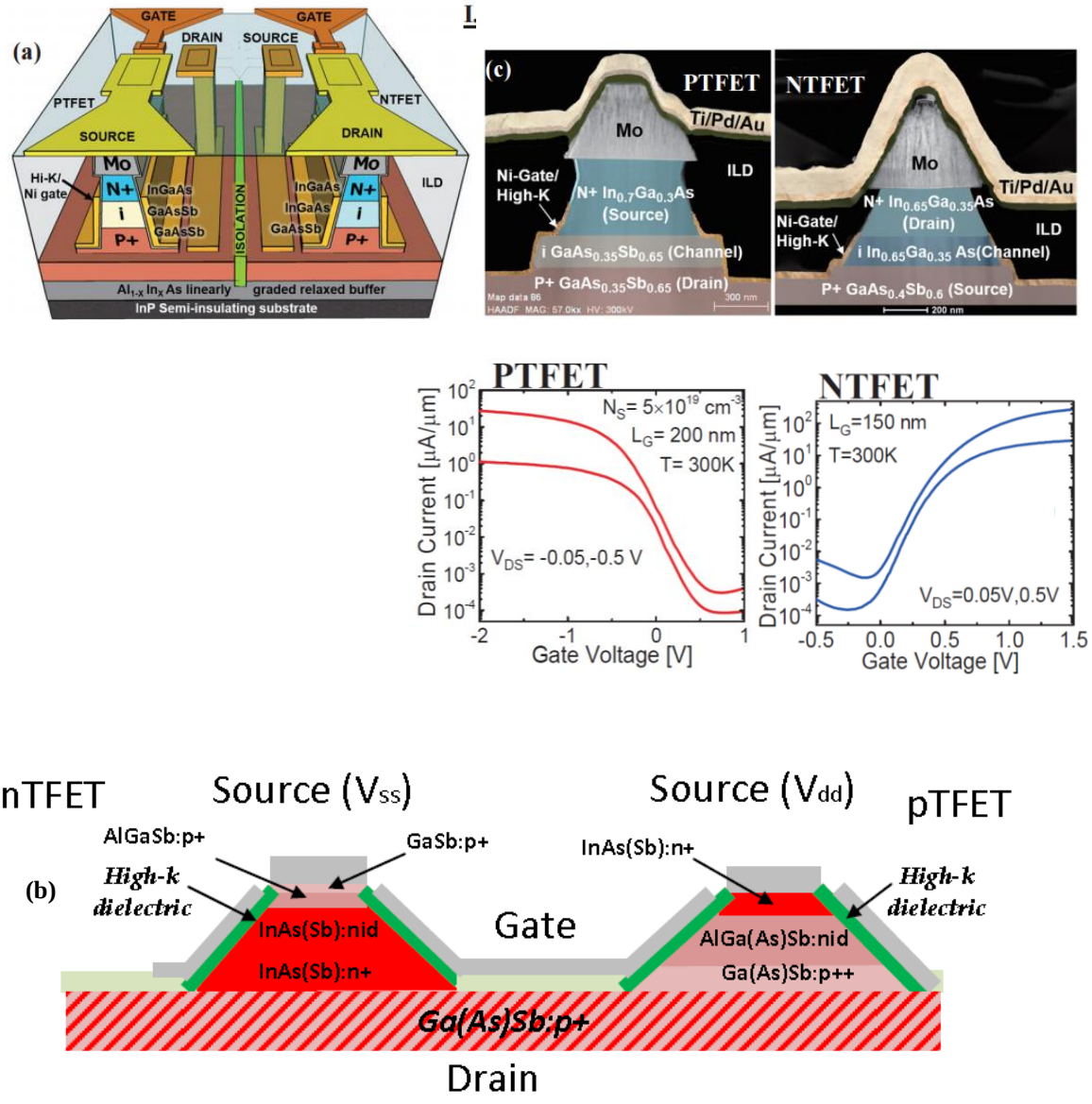


Figure 15: (a) Schematic of a complementary p-TFET and n-TFET on a common metamorphic buffer and TEM image [54]. *(b) Schematic of a C-TFET inverter proposed in the context of the SAMBA project with the selective area epitaxial technology* [52].

1.5. Conclusion

This chapter presented the reasons for searching small swing switches. The most important one is the continuous increase of power consumption in conventional CMOS technology. In this first chapter we have presented the most promising devices that are

widely investigated. Among them, the tunnel field-effect transistor relies on the tunnel injection of carriers through the band gap at the source/channel interface. This mechanism being independent on the operating temperature, the TFET is a potential candidate for ultra-low supply voltage (less than 0.5 V) electronics. The state-of-the art of TFET shows that, although Si or Ge-based devices can achieve a SS lower than 60 mV/dec, the related I_{ON} current is still too low to fulfill the requirements of the CMOS technology. This has led to the use of III-V-based small band gap homojunctions and heterojunctions, which can offer much larger tunneling probabilities.

Considering heterojunction TFETS, high ON currents can be easily achieved in the GaSb/InAs broken gap material system, but this goes along with high OFF currents. For this reason, the (Al)GaSb/InAs(Sb) heterostructure is very attractive as the band offset can be tuned from type II (staggered gap) to type III (broken gap). The results so far on the AlGaSb/InAs material system are based on a lateral architecture. However, to achieve a good electrostatic control, a vertical architecture is highly desirable. Therefore, in this work we will focus on the fabrication of a vertical device with side gates based on the type II (Al)GaSb/InAs material system.

Chapter 2: N-TFET device design and optimization

In the previous chapter, we have explained the working principle of TFETs and compared the experimental results available in the literature. It has been concluded that heterojunction TFETs based on (near) broken gap heterojunctions such as $Al_xGa_{1-x}Sb/InAs$ enhance the tunneling current. In this chapter, we will design and discuss various design parameters about the n-TFET device within the $Al_xGa_{1-x}Sb/InAs$ material system with the help of the Silvaco Atlas simulator.

In this work, we use a Band-to-Band Tunneling (BTBT) model because the drive current in n-TFETs is determined by the amount of carriers that tunnel from the source side (p+) valence band to the channel side (i) conduction band. The BTBT model is based on the Wentzel-Kramers-Brillouin (W.K.B) approximation available in the commercial Silvaco TCAD software [55]. At first, the basic TFET design used in this simulation is explained and the importance of using a heterojunction in terms of high I_{ON}/I_{OFF} ratio is highlighted. The simulation parameters have been separated in two different categories: material properties and device geometry. Finally, we discuss the possible challenges and performance limitations in practical heterojunction TFETs.

The cross sectional n-TFET configuration studied in this chapter is shown in Figure 16. In an n-TFET device, p+ acts as a source, i and n+ act as the channel and drain respectively. In the material engineering section, the influence of the source and drain doping and that of the effective barrier height (E_{beff}) at the junction are presented. In the geometrical engineering section, the gate dielectric and the channel body thickness (W or T_{body}) as well as the channel length (L) and the gate alignment parameters are discussed.

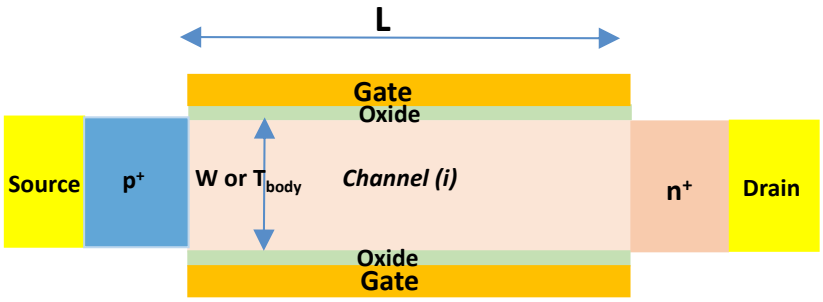


Figure 16: Device schematic of the double gate n-TFET used in this study.

2.1 Simulation framework

In the series of simulations, abrupt doping profiles have been assumed. The model does not take into account the band gap narrowing (BGN) occurring due to degenerate doping [56], quantization effects [57], dislocations/defects at the tunnel junction, D_{it} at oxide-semiconductor interface, work function variations (WFV)[58]. The resulting TCAD simulations should then be considered as useful guides for modeling basic TFET properties, although unable to converge for broken gap heterostructure like the InAs/GaSb structure. Nevertheless, the information and insights are still helpful to understand the device operation and to design the structure.

Due to the electron affinity (EA) values of AlGaSb and InAs chosen in the Silvaco tool, the effective barrier (E_{beff}) height observed at the tunneling interface with respect to the 'Al' composition (x) is different from that reported in the literature. Indeed, Silvaco predicts that $Al_xGa_{1-x}Sb/InAs$ exhibits a staggered band alignment at $x \geq 25\%$ as showed in Figure 17a whereas Lu et al. showed that the staggered band alignment (Figure 17b) occurs for x>45% [59],[60]. Therefore, to avoid any kind of confusion, we consider the effective barrier height (E_{beff}) in the simulations described in this chapter instead of the 'Al' composition. Also, series resistance is not taken in account in our simulations, so we have achieved remarkably high drain current.

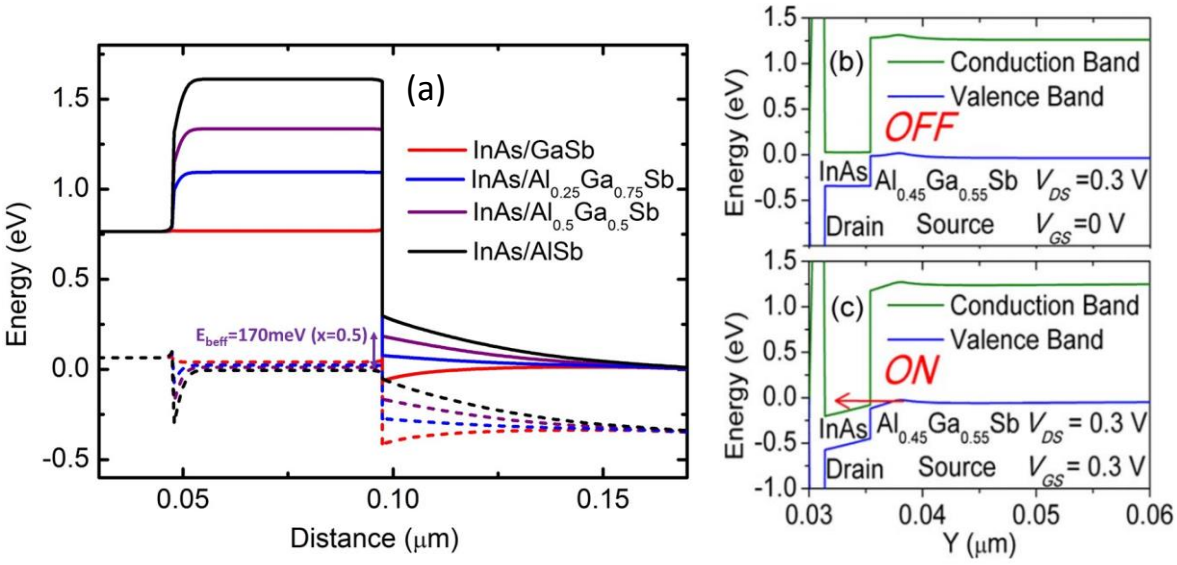


Figure 17: (a) Flat band profiles for the proposed n-TFET for different 'Al' mole fraction of the $Al_XGa_{1-X}Sb$/InAs heterojunction. (b) and (c) Energy band diagrams of the InAs/$Al_{0.45}Ga_{0.55}Sb$ heterojunction (E_{beff} is 40 meV) in the OFF and ON states respectively [60].

2.2 Material Engineering

2.2.1 Comparison of Homojunction and Heterojunction TFETs

The basic device operation is explained from the I_{DS}-V_{DS} output characteristics (Figure 18a) of an InAs homojunction TFET based on the schematics shown before (Figure 15). The energy band profiles along the middle of the channel has been calculated at V_{GS}=0V and at different V_{DS}. At equilibrium (no applied bias) (Figure 18c), the Fermi energy level (E_F) is constant across the junction. Due to the degenerate doping, E_F at equilibrium is above the conduction band in n-type layers and below the valence band in p-type ones.

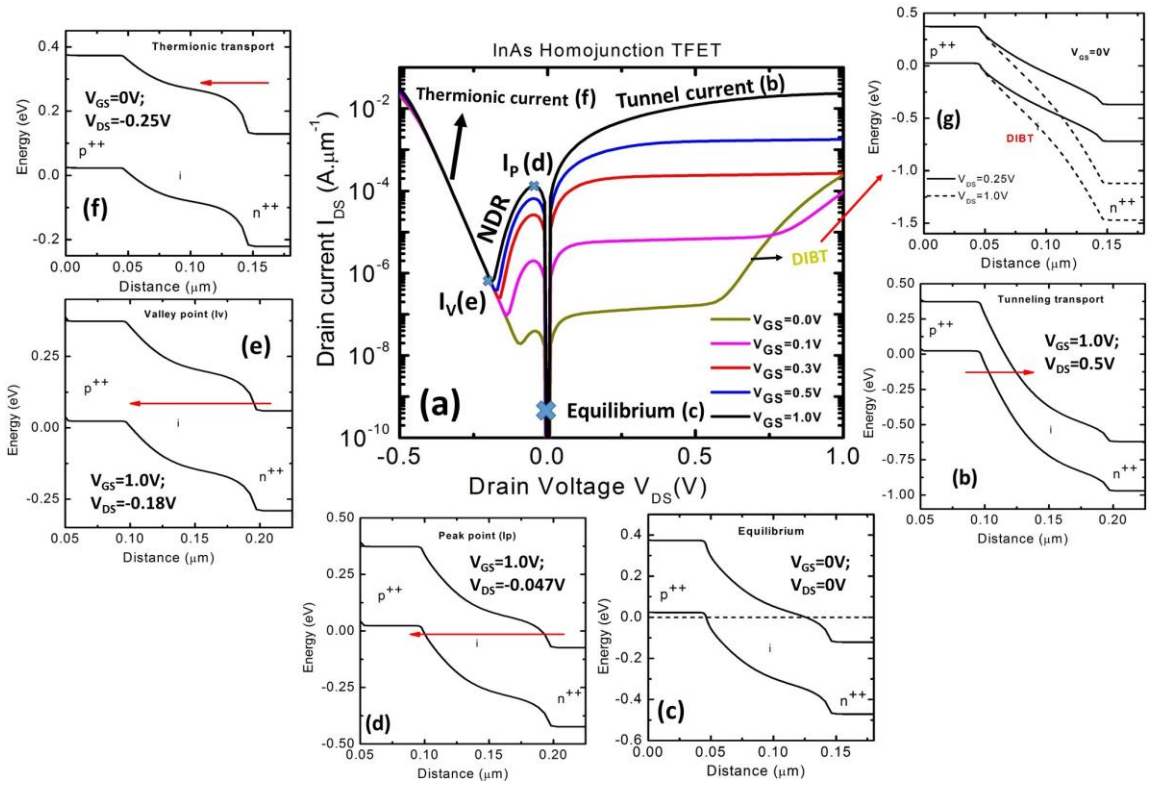


Figure 18: (a) I_D-V_{DS} characteristics, (b) band alignment in reverse bias, (c) equilibrium, (d) peak point (Ip), (e) valley point (Iv), and (f) thermionic diffusion of the InAs homojunction TFET shown in Figure 15.

When a positive V_{DS} bias is applied at the drain terminal, the charge carriers (electrons present in the source terminal) tunnel from the valence band to the channel side conduction band (Figure 18b). Similarly, when a small negative V_{DS} bias is applied, electrons from the n-side conduction band tunnel to the unoccupied states in the p-side (Figure 18d). In the negative bias region, the drain current initially rises to the maximum value known as the peak point (denoted by Ip) and drops to a minimum value known as the valley point (denoted by Iv) when the Fermi level crosses the p-side valence band, giving rise to a Negative Differential Resistance (NDR) region. The NDR phenomenon is considered as the main signature of the tunneling transport in a TFET. By further increasing the negative bias, the diffusion transport of carriers starts to dominate as the barrier for electrons is reduced (Figure 18e). At V_{GS}=0V; V_{DS}=1.0V, the drain current (I_D) also rises sharply with increasing V_{DS}. This is a short channel effect (SCE) called Drain Induced

barrier thinning (DIBT) (Figure 18g). The DIBT effect can be reduced by increasing the channel length/width aspect ratio.

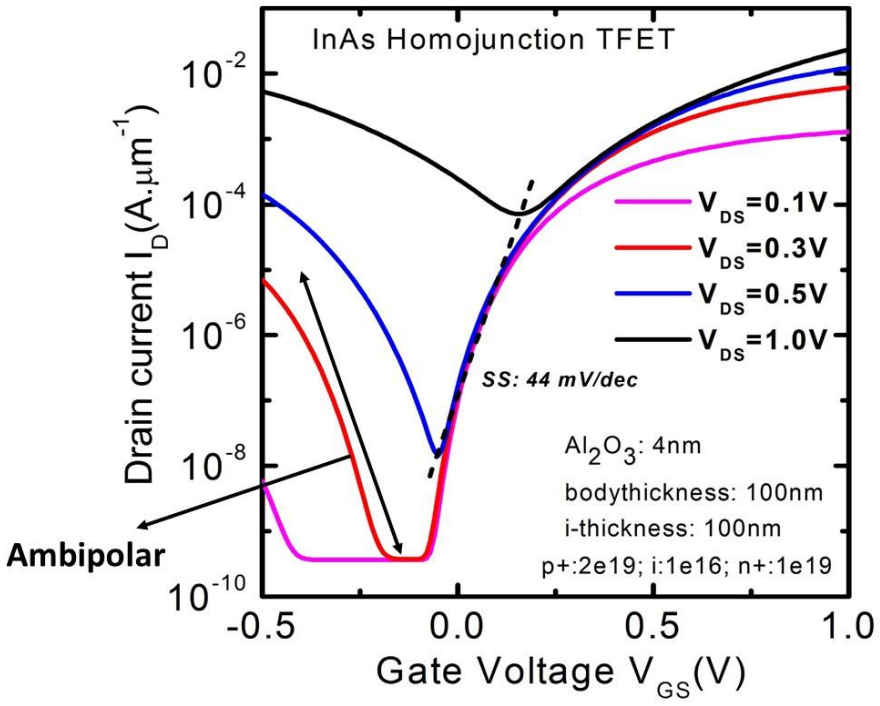


Figure 19: I_D-V_{GS} transfer curve of InAs homojunction TFET at a varying V_{DS}.

Figure 19 shows the I_D-V_{GS} transfer curves of a typical TFET device for different drain-to-source voltages. For I_{OFF}= 15 nA/µm, I_{ON}=1.5 mA/µm at V_{GS}=V_{DS}=0.5V with an $I_{max(VGS=0.5V)}/I_{min(VGS=0V)}$ ratio of over 10^5. The remarkably high magnitude of the ON-currents is achieved as contact resistance and other defects are not considered in our simulation. The SS_{EFF} of this device is 44 mV/decade. At a fixed drain voltage (for example: V_{DS}=0.3V), when the negative gate voltage increases, the drain current (I_D) rises sharply. This is the ambipolar leakage current when tunneling takes place from the channel into the drain side. Figure 20 illustrates the thinning of the tunneling barrier at the channel/drain interface when V_{GS} is increased. Reducing the ambipolar current will be discussed in the later sections of this chapter.

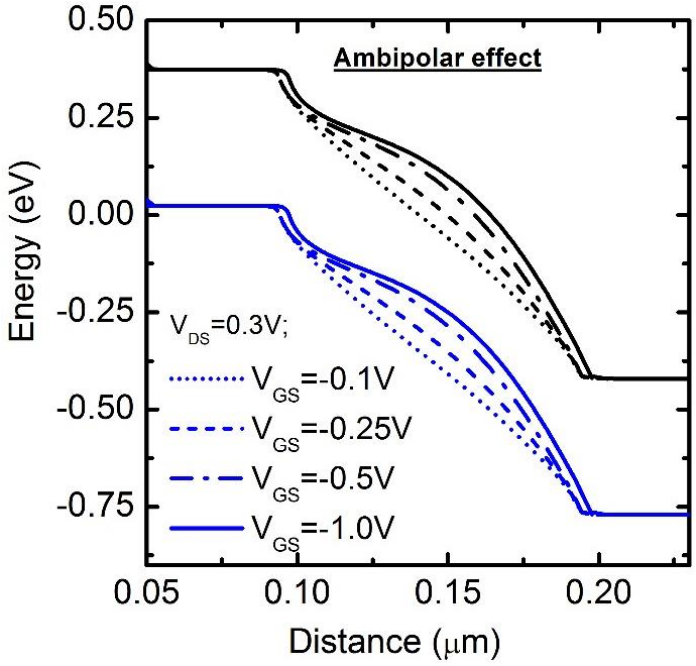


Figure 20: Band profiles showing the ambipolar effect with increasing gate voltage V_{GS}.

Figure 21a shows the I_D-V_{GS} transfer characteristics of an InAs/AlGaSb heterojunction TFET with an E_{beff} of 55 meV and Figure 21b compares it with an InAs homojunction TFET. At V_{GS}=V_{DS}=0.5V, the drain current amounts to 8.5 mA/µm for the InAs/AlGaSb TFET with a SS of 23 mV/decade while it reaches only 1.5 mA/µm with a SS of 44 mV/decade for the InAs homojunction TFET. This large variation in performance is attributed to the large effective barrier (E_{beff}) height in the case of the InAs homojunction TFET.

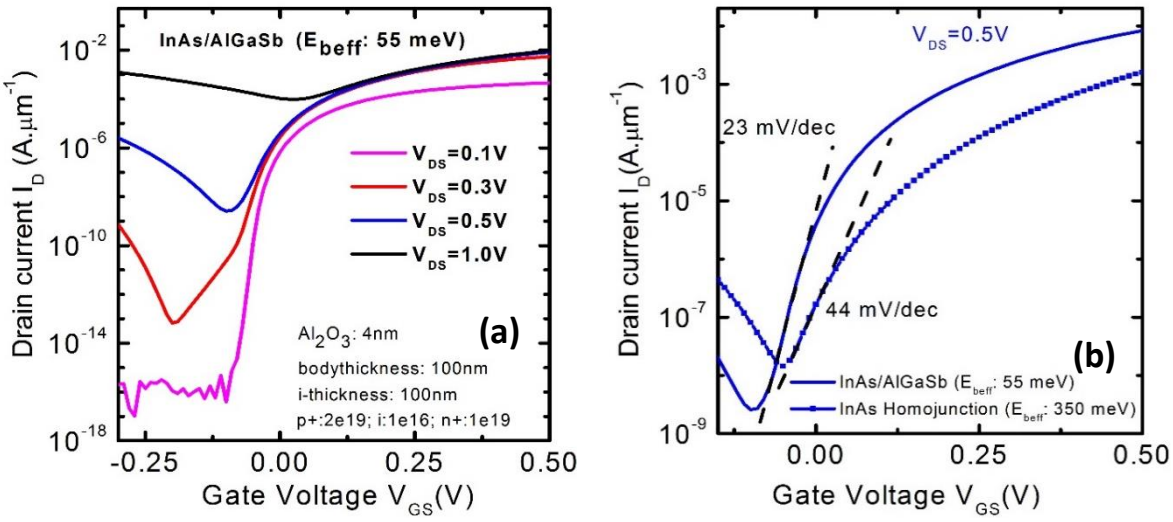


Figure 21: (a) Simulated Drain current (I_D) versus gate voltage (V_{GS}) transfer characteristics of a two-sided gate InAs/AlGaSb Heterojunction TFET with an effective barrier (E_{beff}) height of 55 meV and (b) Comparison showing the difference between a homojunction TFET and a heterojunction TFET and how heterojunction boosts I_{ON}.

2.2.2 Tunneling barrier width ('Al' mole fraction impact in the $Al_xGa_{1-x}Sb/InAs$ system)

An important challenge for TFETs is to realize a sub-60 mV/dec SS while simultaneously achieving a high I_{ON}/I_{OFF} ratio. The material system used at the source/channel interface plays a vital role. The effective barrier height (E_{beff}) at this interface is responsible for the tunnel current density. The objective is to have a high tunneling current while at the same time keeping the off state current as low as possible. With low E_{beff} values at the tunnel junction, higher transmission tunneling probability are obtained, resulting in an increase of I_{ON}. The effective barrier (E_{beff}) height at the interface can be tuned by varying the 'Al' composition in the InAs/(Al)GaSb material system. The impact of the E_{beff} height on the transfer characteristics is shown in Figure 22. I_{ON} is boosted for the device with a E_{beff} height of 55 meV at the tunnel junction. However, it is not the best in terms of smaller SS and maximum I_{ON}/I_{OFF} ratio. This is due to the fact that for a 55 meV E_{beff} height, the ambipolar leakage in the sub-threshold regime masks the sharp switching thereby increasing the SS slope.

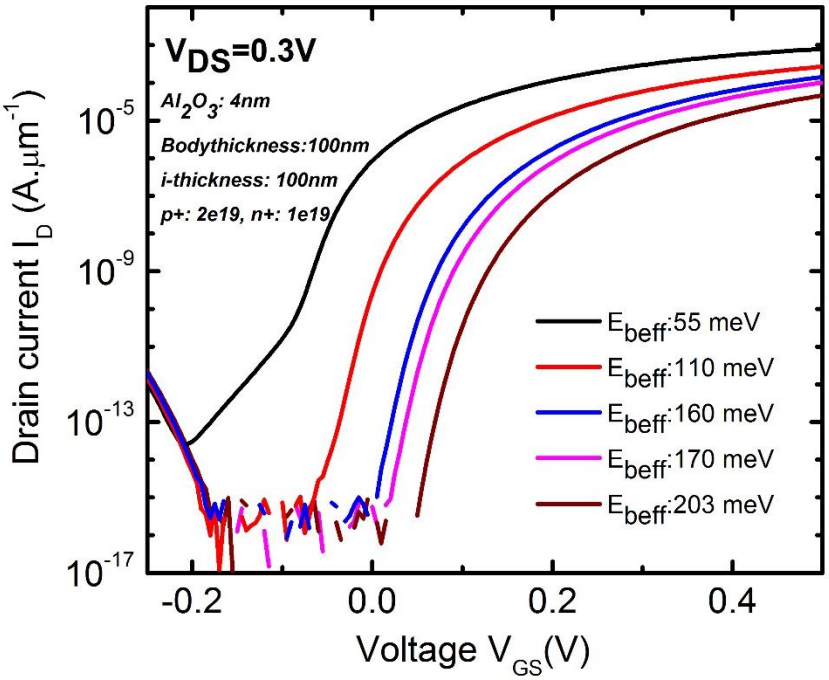


Figure 22: I_D-V_{GS} curve for different effective barrier heights (E_{beff}) at the InAs/$Al_XGa_{1-X}Sb$ heterojunction.

2.2.3 Impact of the source and drain region doping

Doping engineering in the source and drain regions may also be useful to enhance the I_{ON}/I_{OFF} ratio. Figure 23a shows the simulated curves of n-TFETs with varying the source p-doping from 8 x 10^{18} cm^{-3} to 5 x 10^{20} cm^{-3} while keeping the drain n-doping constant at 1 x 10^{18} cm^{-3}. The I_D-V_{DS} characteristics of Figure 23a show that a high source doping of 5 x 10^{20} cm^{-3} is desirable for achieving a high I_{ON}. Increasing the source doping concentration results in a shift of both the conduction (E_c) and the valence (E_v) band edges thus reducing the tunnel length at the junction and leading to an improved transmission probability as shown in Figure 24. High source doping degrades only slightly the SS_{min}, which is below 60 mV/dec in all cases. Its impact on V_{TH} is stronger due to the use of a GaSb/AlGaSb heterojunction at the source side, which shifts the characteristics. Therefore, in order to achieve a low I_{OFF}, a source doping value lower than $5.10^{19}/cm^3$ seems suitable.

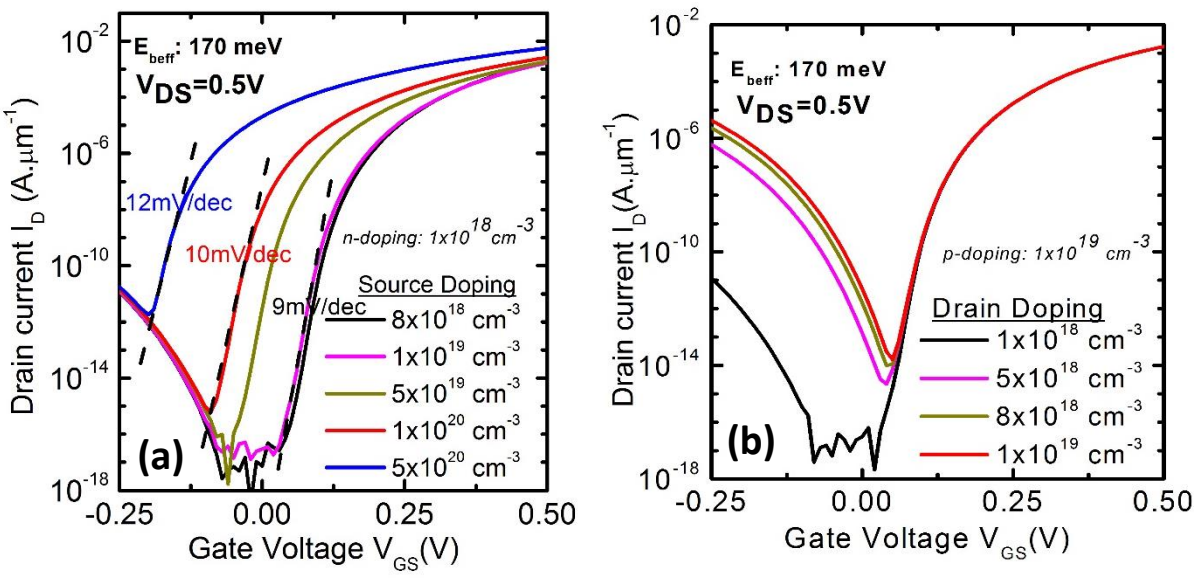


Figure 23: (a) n-TFET simulated I_D-V_{GS} transfer curves for various source doping levels at a constant drain doping of 1 x 10^{18} cm^{-3} and (b) n-TFET simulated I_D-V_{GS} transfer curves for various drain doping levels at a constant source doping of 1 x 10^{19} cm^{-3}.

Figure 23b shows the simulated curves of n-TFETs with different drain doping levels from 1 x 10^{18} cm^{-3} to 1 x 10^{19} cm^{-3} while keeping the source doping constant at 1 x 10^{19} cm^{-3}. From the I_D-V_{GS} characteristics, the I_D is about 1.7 mA/µm at V_{GS}=V_{DS}= 0.5V and is almost the same for all the drain doping concentrations. The effect of the drain doping variation is clearly seen in the off-state region with the suppression of the ambipolar leakage current for a drain doping concentration of 1 x 10^{18} cm^{-3}, in agreement with Seabaugh et al. [61]. Ambipolarity is not a desirable phenomenon at circuit level, as it will increase the static power consumption. When the drain doping is lowered to 1 x 10^{18} cm^{-3}, the ambipolarity is significantly reduced improving the overall I_{ON}(V_{GS}=0.5V)/I_{OFF}(V_{GS}=0V) ratio.

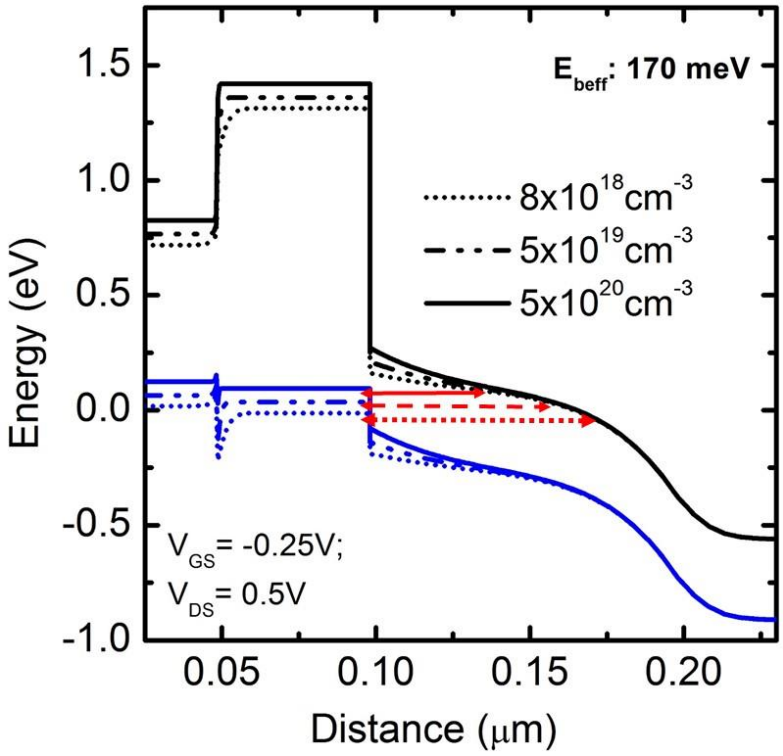


Figure 24: Energy band variations at V_{GS} =-0.25V and V_{DS} = 0.5 V when increasing the source doping level while the drain doping one is kept constant at 1x10^{18} cm^{-3}.

In practice, a low drain doping concentration is desirable but too low values would increase the contact resistance, which affects the overall drain current of the device. In literature, other strategies such as increasing the bandgap at the drain region to reduce/suppress the ambipolar effect have been reported [62]. A doping drain gradient, with a low doping level at the channel-drain junction gradually increasing up to the surface could also help in reducing the ambipolar current without compromising the contact resistance.

2.3 Geometry Engineering

2.3.1 Gate dielectric and thickness

Improvement of the drain current and subthreshold swing can be obtained by a proper choice of the high-k dielectric. Figure 25 shows the effect of the variation of the effective oxide thickness (EOT) on the I_{DS}-V_{GS} characteristics. As a result of increased gate

capacitance with decreasing EOT, SS is reduced from 25 mV/dec for an EOT of 1.73 nm (Al_2O_3 4 nm) to 19 mV/dec for an EOT of 0.15 nm (HfO_2 1 nm). This goes along with a slightly increased drain current. However, most devices in the literature do not reach a sub-60 mV/dec slope due to the high concentration of interface states (D_{it}) at the oxide-semiconductor interface, which reduces the gate's electrostatic control over the channel.

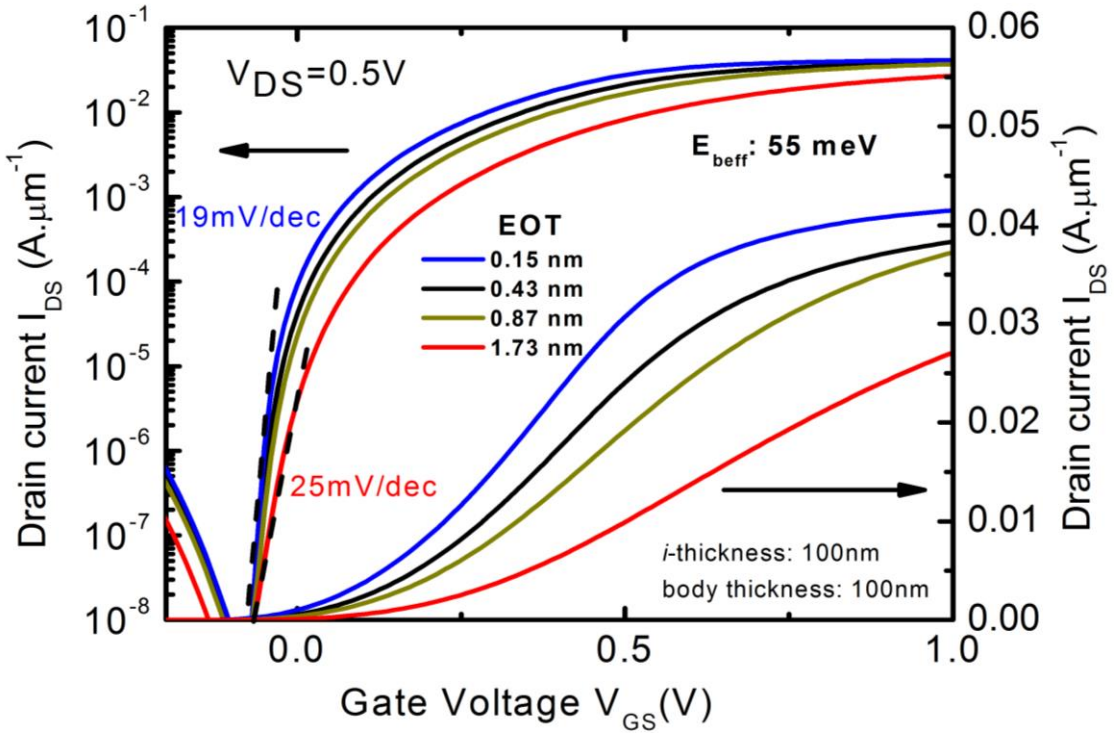


Figure 25: Drain current (I_D) versus gate voltage (V_{GS}) transfer characteristics of a vertical two-sided gate InAs/$Al_{0.25}Ga_{0.75}Sb$ Heterojunction TFET at V_{DS}=0.5V with an effective oxide thickness (EOT) of 0.15 nm, 0.43 nm, 0.87 nm and 1.73 nm respectively. For all the devices the gate is aligned to the intrinsic channel thickness of 100 nm and the body thickness is 100nm.

2.3.2 Single & Double gate

To improve TFET performance, a double gate configuration is appropriate to enhance the electrostatic control compared to a single gate. From Figure 26, the maximum I_D increases by about a factor of 2 when going from single gate to double gate at V_{DS}=V_{GS}=0.5V, with an improvement of the SS from 8mV/decade to 5mV/decade.

However, in the double gate configuration, the electrostatic control depends on the body thickness of the channel and the smallest SS is obtained on the 10 nm thick body device. This is due to a cumulative effect of the electric fields induced by the 2 gates, which improves the electrostatic control over the entire body thickness.

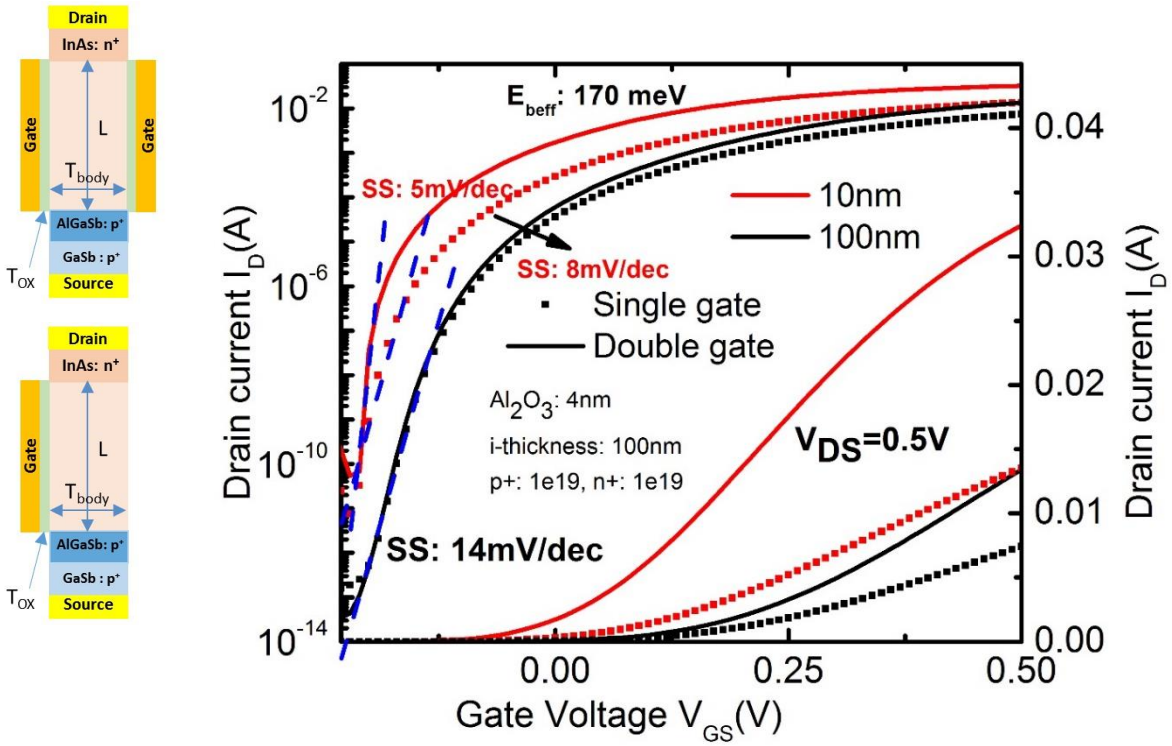


Figure 26: n-TFET simulated I_D-V_{GS} transfer curves of an InAs/AlGaSb (E_{beff}=170 meV) heterojunction TFET comparing the single gate and double gate configurations for two body thickness (T_{body}) of 10 nm and 100 nm.

2.3.3 Body thickness (T_{body})

Figure 27 shows the simulated I_D-V_{GS} transfer characteristics for different body thicknesses. As the body thickness gets thinner, the SS improves from 15mV/decade for a 100nm body thickness to 5 mV/decade for a 10nm one. This is accompanied by an increase of I_{ON} which, for a given V_{DS}, may be attributed to the BTBT rate which is rapidly reduced for large T_{body} due to the lower coupling of the gates [63]. The improvement of the SS_{EFF} for the thin body is due to the strong effect of the two-side gate electrostatics on the channel, resulting in a more uniform electric field within the width of the body.

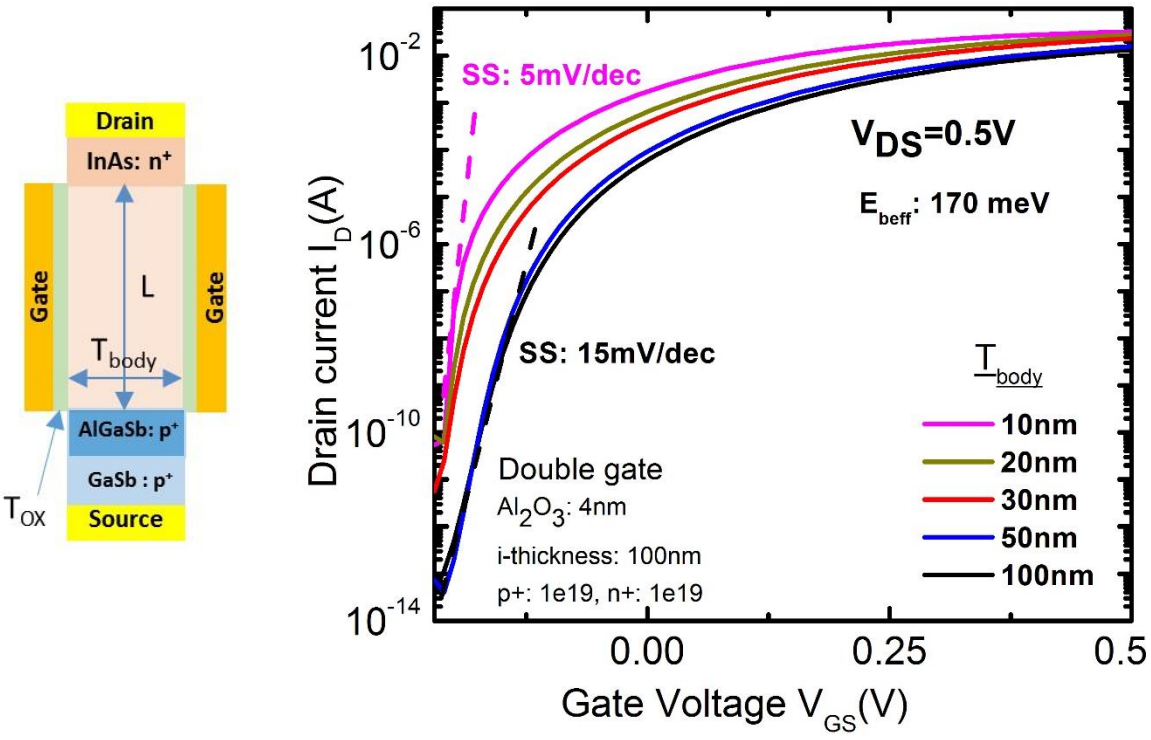


Figure 27: n-TFET simulated I_D-V_{GS} transfer curve for different body thickness (T_{body}) of 10 nm, 20 nm, 30 nm, 50 nm and 100 nm respectively while all other parameters of the devices are kept constant.

To further validate the above understanding, the band diagram across the channel, at 10nm distance from the gate has been plotted for a T_{body} of 100 nm and 20 nm respectively (Figure 28). For a 20 nm thick $T_{body,}$ the gate control is more effective near the junction than for the 100 nm thick $T_{body,}$ which directly affects the tunnel barrier width and in-turn the tunnel current density. Finally, at or below 10nm body thickness, the tunnel current is expected to be much lower if quantum confinement effects are considered as has been already observed by Lu and Padilla *et al.* [64],[65], because the effective band gap of the InAs channel is increased in the presence of confinement.

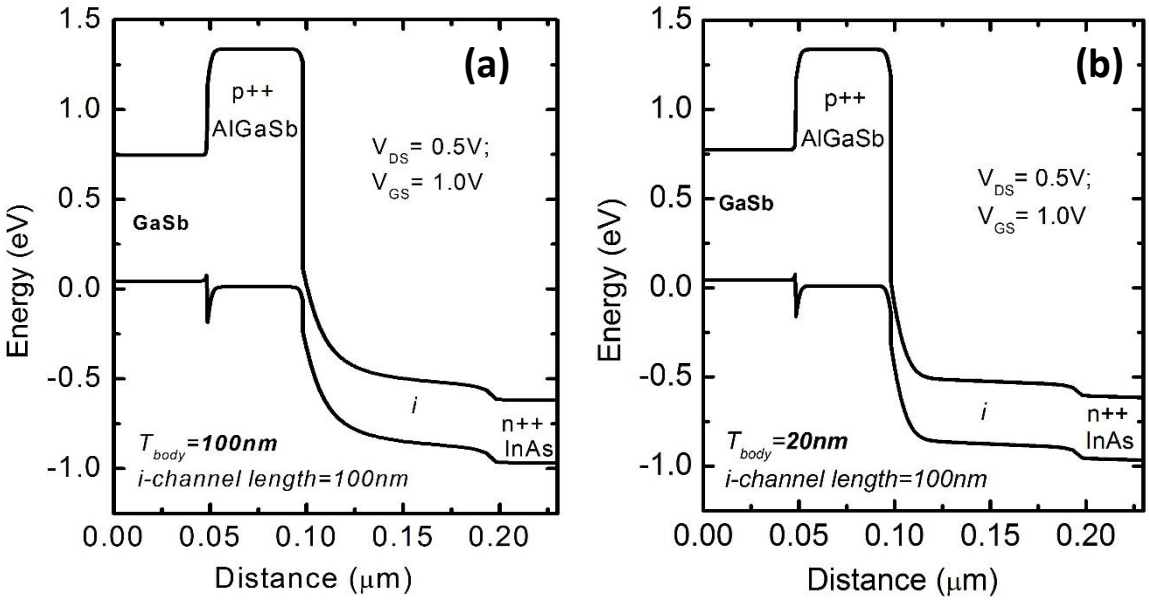


Figure 28: Simulated energy band diagram at V_{GS} = 1 V and V_{DS} = 0.5 V across the channel, 10nm distance from the gate, for a two-sided gate n-TFET with a T_{body} thicknesses of (a) 100 nm and (b) 20 nm respectively.

2.3.4 Intrinsic channel length (L)

As can be seen in Figure 18g there is an increase of the minimum drain current (I_{OFF}) because of short channel effects in the proposed TFET design. One way to suppress this short channel effect is the careful optimization of the drain doping level. Another option is to increase the intrinsic channel length. Figure 29 demonstrates that I_{ON} is independent of the intrinsic channel length (L), but I_{OFF} decreases with L. This behavior is similar to what has been observed in Si TFETs [66]. Shorter channel lengths reduce the tunneling-length between the source and drain further worsening the leakage problem. From Figure 29, Imax $_{(VGS=0.5V)}$/Imin $_{(VGS=0V)}$ improves from $9.5x10^{7}$ for a 80nm channel length to $1.7x10^{12}$ for a 250 nm channel length. In figure 28, the inversion between the 150 and 250 nm curves for negative V_{GS} is due to uncertainties in the simulation for current below 10^{-15}A.μm^{-1}.

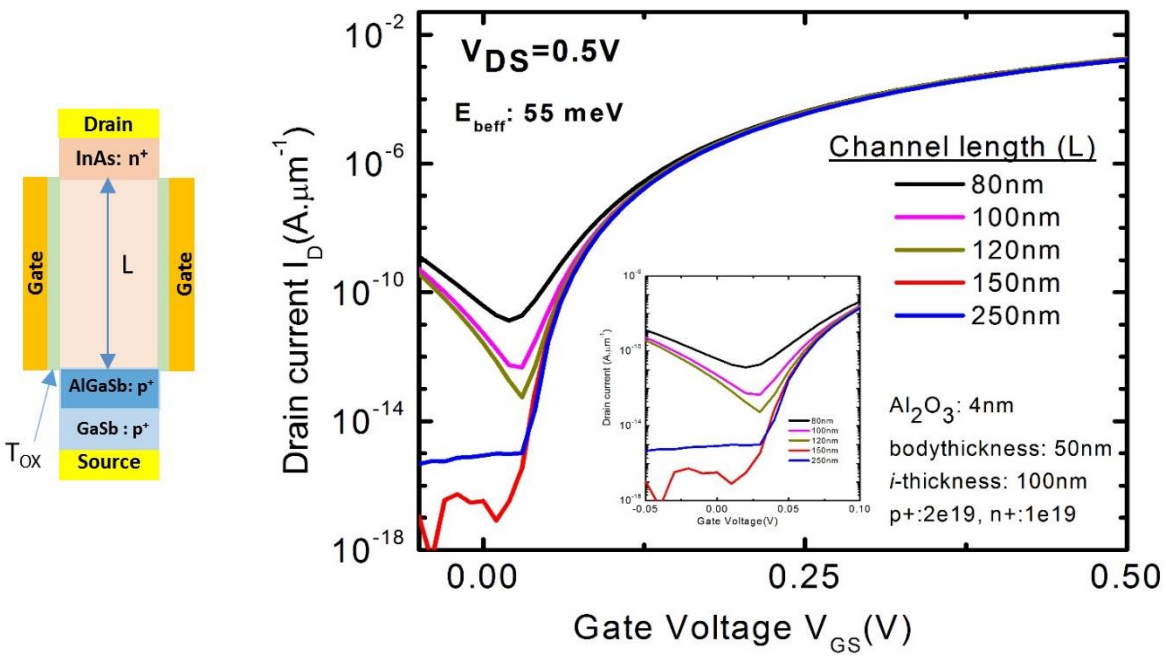


Figure 29: n-TFET simulated I_D-V_{GS} transfer curves of an InAs/AlGaSb (E_{beff}: 55meV) heterojunction TFET showing the influence of the intrinsic channel length.

2.3.5 Gate-Drain overlap

TFETs are ambipolar in nature. This ambipolar behavior can be reduced by the gate alignment with respect to the channel (schematic of the gate alignment to the channel shown in Figure 30). For positive V_{DS}, the electrons that are injected in the channel are driven towards the drain resulting in the ON-state current of the TFET. However, in the OFF-state and at large $V_{DS,}$ the tunnel barrier width at the channel to drain interface decreases affecting I_{OFF} but also SS [67]. Considering a 100nm channel length, the performances of a gate aligned to the channel (0nm curve) with those of a 40nm underlapped gate and those of a 40 nm-overlapped gate are compared in Figure 31. The 40 nm value for the under/overlap is chosen as a typical one to highlight the effect.

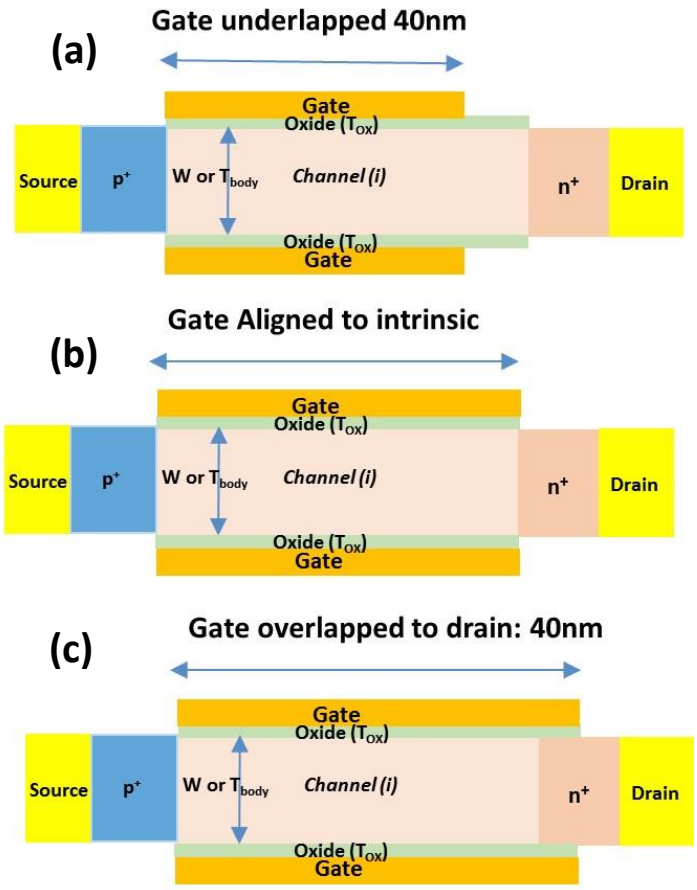


Figure 30: Schematic of (a) 40 nm gate underlapped to channel, (b) gate aligned to channel, and (c) 40 nm gate overlapped to drain.

This evidences that the 40nm underlapped gate device achieves a lower ambipolar current than the device with the gate aligned with the channel. Low I_{OFF} is attributed to the reduced gate induced electric field on the drain-channel junction. Figure 31(b)-Figure 31(d) shows the band profiles for all the gate alignment configurations considering a cutline near the Al_20_3 interface at V_{GS}=-1.0V and V_{DS}=0.5V. The channel/drain tunnel-barrier lengths for the gate-alignment configurations of 0nm, 40nm overlapped and 40nm underlapped are calculated to be 6.7nm, 9nm and 16nm respectively. Since the ambipolar current is inversely proportional to the tunnel-barrier width, the device with a gate underlapped of 40nm exhibits the lowest leakage. Additional advantage of having short gate in TFETs is the reduced parasitic capacitance [68].

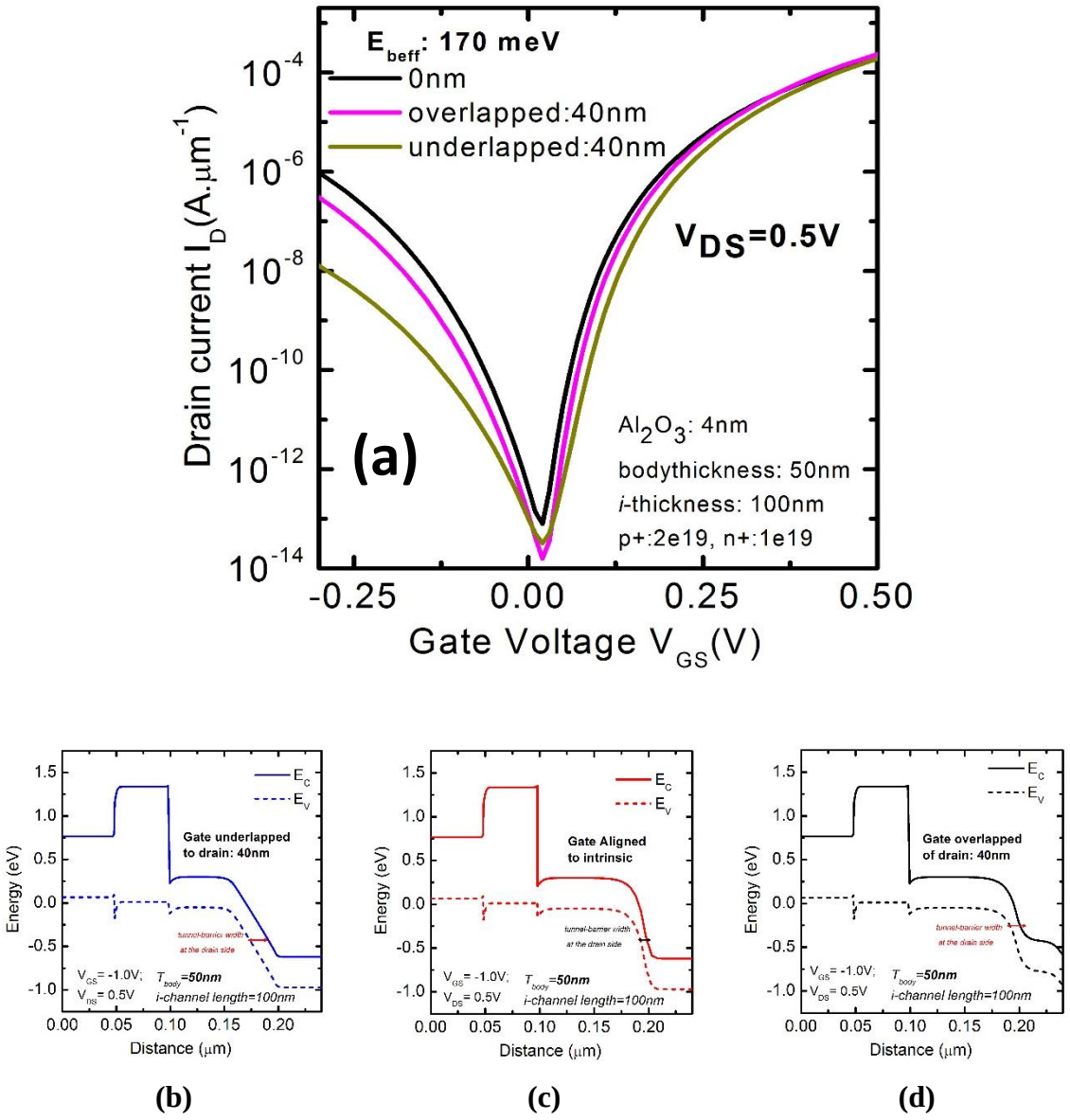


Figure 31: (a) n-TFET simulated I_D-V_{GS} transfer curves of InAs/AlGaSb heterojunction TFET with different gate alignment with the channel, (b)-(d) Impact on the band profiles under the influence of gate induced electric field at the channel-drain junction.

2.4 Beyond simulation

In principle, n-TFET operation relies on BTBT mechanism i.e. carriers tunnel from the valence band on the source side (p+) to the conduction band of the intrinsic channel. The quality of the interface between the source and the channel is the key point to get a

steep SS. In general, I_{ON}, I_{OFF} and SS are limited by material and technological issues, which have been neglected in our simulation and are discussed hereafter.

2.4.1 Material Issues

We mainly focus here on III-V heterostructures keeping in mind that the challenges might be different for TFETs fabricated using indirect band gap materials such as Si or Ge. The main material issues come from non-idealities in epitaxy related to strain relaxation, heavy doping effects and defects at the oxide-semiconductor interface.

From any device point of view, perfectly lattice matched epitaxy is desired to achieve reproducible high performance devices. As the lattice mismatch between layers gets larger, beyond the critical thickness, the associated elastic energy is plastically released via the nucleation of dislocations during the growth as shown in Figure 32.

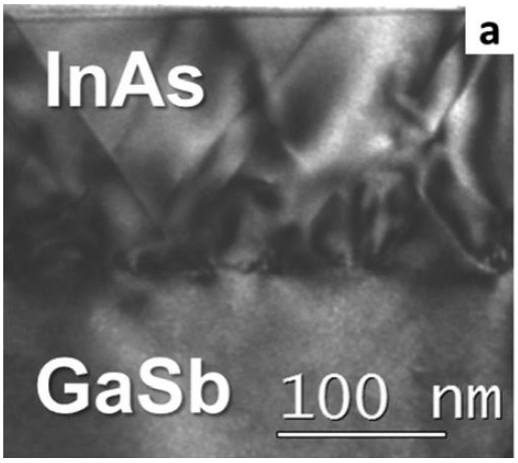


Figure 32: Cross section TEM image of InAs grown on GaSb showing dislocations originating from the interface due to the lattice mismatch between InAs and GaSb. Picture taken from [69].

These dislocation defects at the heterojunction can lead to the trap-assisted-tunneling (TAT) mechanism. Moreover, the defects inside the band gap of the channel lead to the Shockley-Read-Hall (SRH) leakage phenomenon. So far TAT, together with SRH are responsible for the degraded I_{ON}/I_{OFF} ratio and SS in practical TFETs.

SRH has a strong temperature dependence. In the presence of traps, generation-recombination takes place by the absorption of phonon as shown in Figure 33. By using large band gap materials in the channel, carrier recombination can be reduced while at the same time tunneling probability is also reduced.

TAT is a strong electric field dependent leakage mechanism. In the presence of dislocations, which introduce fixed charges at the tunnel junction, the electric field around the fixed charges directly affects the band-alignment and changes the effective tunneling barrier height [70]. Because these defects are electrically active and act as conductive channels, the transport of carriers takes place from source to drain even when there is no applied gate voltage. This indeed increases the excess leakage current and appears in the form of an Off-state current affecting the SS. The path of the carriers in the presence of defects is shown in Figure 33.

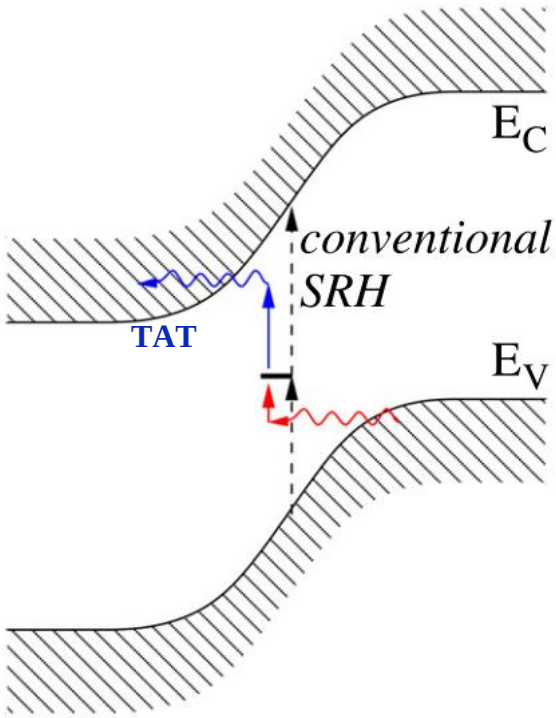


Figure 33: Schematics showing the SRH and TAT leakage mechanisms, taken from [71].

To achieve a high interband tunnel current, heavy doping is required to induce the high electric fields at the junction [72]. Heavy doping is generally associated with tails of

the density-of-states that extend into the band gap referred to as band-tails (schematic in Figure 34). Sharma et al. have proposed recently a new structure named intrinsic-Source Broken-gap TFET to reduce the impact of the band-tails and eventually increase the On-current with the broken band alignment [73].

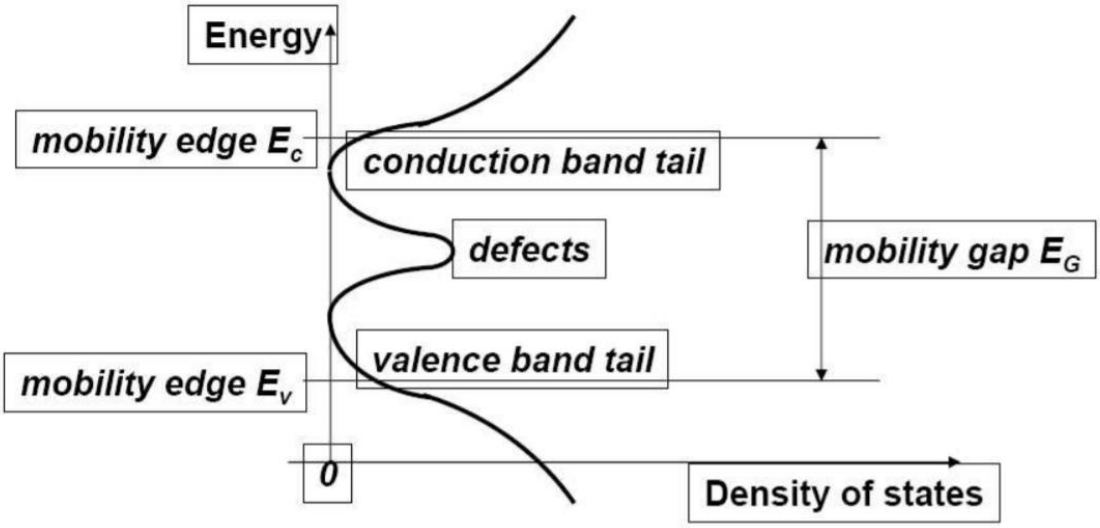


Figure 34: Schematics showing the band-edges and band-tails [74]

Finally, depending on the deposition technique, the use of high-k oxides like Al_2O_3, HfO_2 etc, are susceptible to generate a high interfacial defect density (D_{it}) at the oxide-semiconductor interface [75]. This high D_{it} pins the Fermi level (E_F) within the channel and impedes the gate to modulate the charge efficiently.

2.4.2 Technological Issues

The technological challenges include the formation of low-resistivity ohmic contacts and the achievement of channel widths around 20 nm with a high aspect ratio. Ohmic contacts are very important to achieve a steep SS. On-resistance should be small in order to improve the overall circuit switching speed. But a low doping at the drain side is generally applied for TFET as discussed in section 2.6 to reduce the ambipolarity leakage at the channel-drain junction. However, good ohmic contacts require a heavily doped layer.

One way to circumvent this problem is to use a doping gradient, with a low doping level at the channel-drain junction gradually increasing up to the surface. This idea has been simulated in carbon nanotube FET (CNFET) using a staircase doping technique [76].

Thin channel widths with high aspect ratio is ideal for high performance [77]. But using wet etching, a V-shape profile is obtained in the [110] orientation and a Λ-shape one in the [1-10] orientation. The details of the wet etching and related orientations will be detailed in chapter 3. Simulating all the electrical parameter dependence on the orientation involves complex models and is beyond the scope of this work. In this section, we have mapped the 2D electric field intensity within the V-shaped device (Figure 35a and Figure 35c) and compared it to the electric field map inside a device having a reversed shape (Λ-shape) (Figure 35b and Figure 35d), which are the two different shapes that are obtained after wet etching. The band profiles for ON-state (V_{GS}=0.5V) and OFF-state (V_{GS}=-1V), for both configurations considering a cutline near the Al_20_3 interface and in the middle of the mesa are displayed in Figure 35(e)-(h). In the ON-state, the larger electric field concentration induced by the V-shape leads to a reduced tunneling distance in the middle of the mesa and a more uniform profile along the source channel interface. However, in the OFF-state, the reduced gate induced electric field by the V-shape in the middle of the mesa results in a significant band bending induced by the drain voltage and thus a shorter tunneling distance (DIBT) at the source channel interface. Increasing further the channel thickness or using a dry etching process to obtain a more straight profile could limit this effect. On the other hand, this lower gate influence at the channel to drain interface in the middle of the mesa also enlarges the tunneling distance between channel and drain, minimizing the ambipolar effect. Eventually, one other advantage of the V-shape is the larger area of the drain contact that can improve the series resistance. So, in this thesis work we mainly focus on the realization and comparison of V-shape and Λ-shape mesa profile TFET devices.

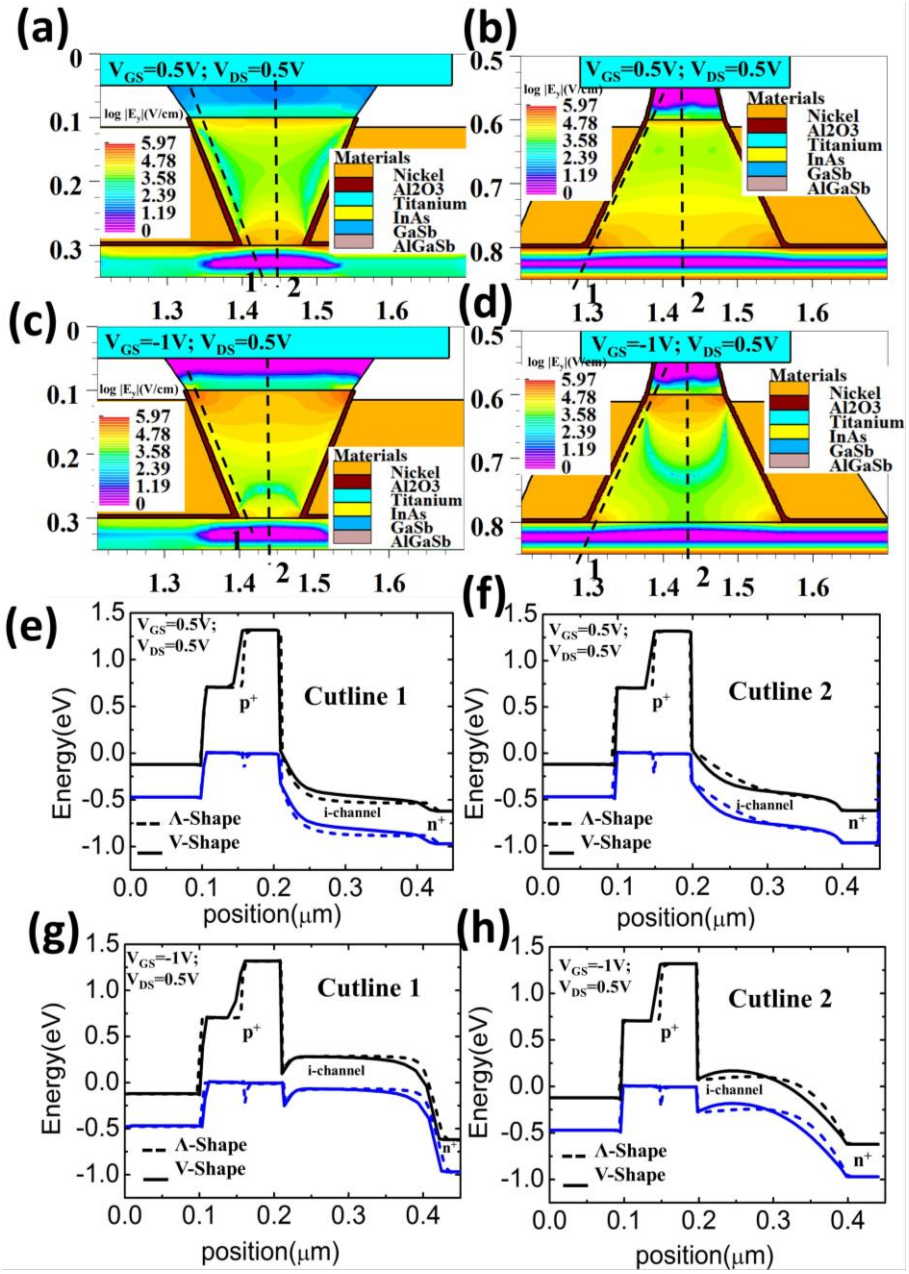


Figure 35:Vertical electric field mapping inside the heterostructure for a V-shaped device at V_{DS}=V_{GS}=0.5V (a) or V_{DS}=0.5V and V_{GS}=-1V (c). Vertical electric field mapping inside the heterostructure for a Λ-shaped device at V_{DS}=V_{GS}=0.5V (b) or V_{DS}=0.5V and V_{GS}=-1V (d). The two shapes are reversed and exhibit a width of 80 nm at respectively the source to channel interface (for the V-shape) or channel to drain interface (for the Λ-shape). The band lines-up resulting from this electric field are extracted along a cutline near the InAs/Al_2O_3 interface (e and g) or along a cutline in the center of the mesa (f and h) for both kind of shape.

Chapter 3: Fabrication process flow of Tunnel diodes and Tunnel FETs

This chapter presents the process flow of n^+-InAs/p^+-$Al_xGa_{1-x}Sb$ Tunnel Diodes (TDs) and TunnelFETs (TFETs) fabricated on GaSb and GaAs substrates. First, the process flow of TDs and TFETs are explained briefly and later each step along with encountered problems is detailed.

3.1 Introduction

It was discussed in chapter 2 that the real challenge in TFETs is to realize a high ON current (I_{ON}) while still maintaining a high I_{ON}/I_{OFF} ratio and a sub-60 mV/dec SS. Growing a n^+-InAs/p^+-$Al_xGa_{1-x}Sb$ heterojunction on a lattice mismatched substrate like GaAs, interface defects and dislocations will enhance the Shockley-Read-Hall generation-recombination (G-R) as well as trap-assisted tunneling resulting in an increase of I_{OFF} [78]. These are parasitic leakage currents, which occur independently of the gate bias. To primarily understand the above-mentioned leakage mechanisms occurring in the epitaxial structure, two-terminal tunnel diodes (TDs) is the simplest way to analyze the behavior.

All samples in this study have been grown using molecular beam epitaxy (MBE). The basic p^+-i-n^+ structure consisting of p^+-$Al_xGa_{1-x}Sb$ and n^+-InAs with a 3nm intrinsic InAs layer has been grown on GaSb and S.I. GaAs substrates for comparison of electrical performance. The schematics of the TDs grown on different substrates are shown in Figure 36a and b. For an InAs epilayer on GaSb substrate, the critical thickness is around 100 nm before relaxation occurs. So in the case of TFET on GaSb substrate (Figure 36c), a 80nm i-InAs channel has been chosen. When transferring the whole structure on a S.I. GaAs substrate and simultaneously increasing the intrinsic channel thickness, the growth has been initiated by an InAs metamorphic buffer as shown in Figure 36d. On S.I. GaAs substrate, the resulting threading dislocation density in the active layers lies in the low $10^8/cm^2$ range [100].

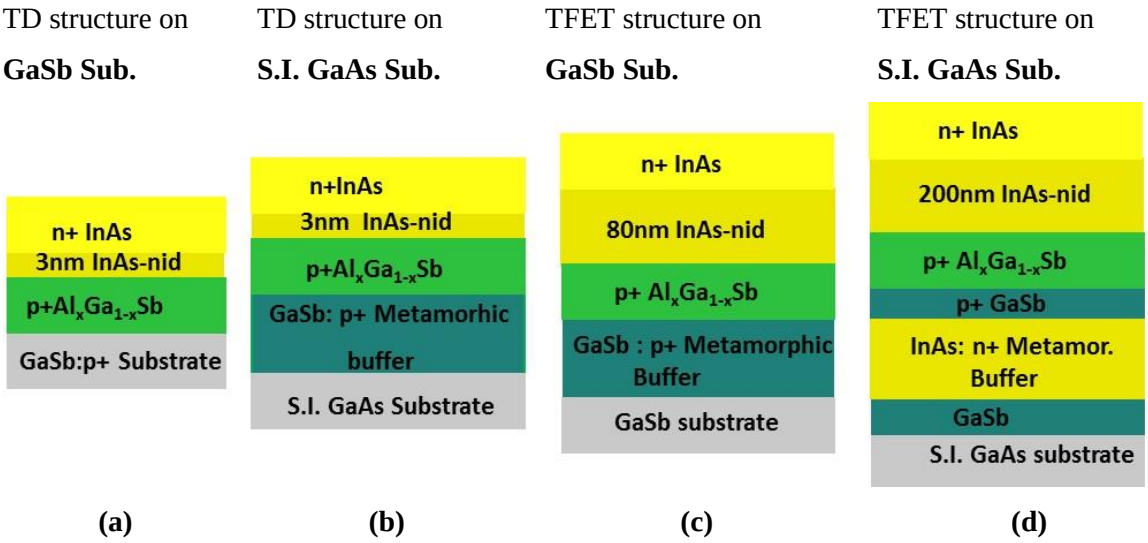


Figure 36: Schematic of the Tunnel Diode and TFET structures used to explain the fabrication process.

3.2 Tunnel Diode processing

3.2.1 Tunnel Diode Mask Layout

Scaling device geometries to very small dimensions will reduce the number of defects present within the device, thereby increasing the peak to valley ratio (PVCR) of a TD [79]. Given this fact, patterning smaller dimensions to as low as 0.15µm is impossible with optical lithography, so the electron beam lithography (EBL) technique is used to pattern these small dimensions.

The mask design for the fabrication of TDs consists in three EBL steps: top contact patterning, top and bottom contact via definition, and top and bottom large contact pads. The top contact, which is referred as the drain contact in TFETs, is patterned with various sizes from 1µm x 4µm down to 0.15µm x 0.15µm to access very small tunnel junctions.

3.2.2 Tunnel Diode Process Flow

The TD process has been developed to study the influence of material properties of the tunnel junction on the electrical characteristics. A tunnel diode is a degenerately doped p-n junction with an i-intrinsic layer sandwiched between p^+ and n^+ forming a p^+-i-n^+

structure. The electrical characteristics of a TD provide information on the peak current density (J_p), valley current density (J_v), peak to valley ratio, which depend on the interface quality of the heterostructure [80]. Absolute conductance data gives information about the subthreshold slope (SS) of a TFET without the need to fabricate the transistor. Since there is no gate-oxide and there are no parasitic leakage paths, hence the SS extracted from the absolute conductance is directly related to the tunnel junction quality [81].

A simple TD process has been implemented to assert the heterojunction quality. In this section, the main fabrication process steps are highlighted. Further details on the process parameters can be found in Appendix I. Figure 37 shows the schematic of the TD process, which consists of a top and bottom contacts. In the first step, the drain contact was defined using EBL with varying drain metal length and width ranging from 1µm x 4µm to 0.25µm x 1µm as described in the mask section. Based on wet chemistry and using the drain contact as a hard mask, InAs (n^+) and InAs (i) were anisotropically etched down to the source layer (p^+). After the wet etching, SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) at 300°C. Contact windows (vias) were opened in SiO_2 by a reactive ion etching (RIE) plasma in the top and bottom contact areas as shown in Figure 37 (e). Since the $Al_xGa_{1-x}Sb$ surface is known to readily oxidize in the environment [82], this AlGaSb layer was wet etched until the GaSb buffer layer in a diluted ammonia solution. Finally metal pads were e-beam evaporated to form the contact on the GaSb buffer and the top contact as shown in Figure 37 (f). Note that the final metal pads were evaporated by tilting the sample to 20° with respect to the metal crucible to make sure the top contacts are properly connected to large contact pads.

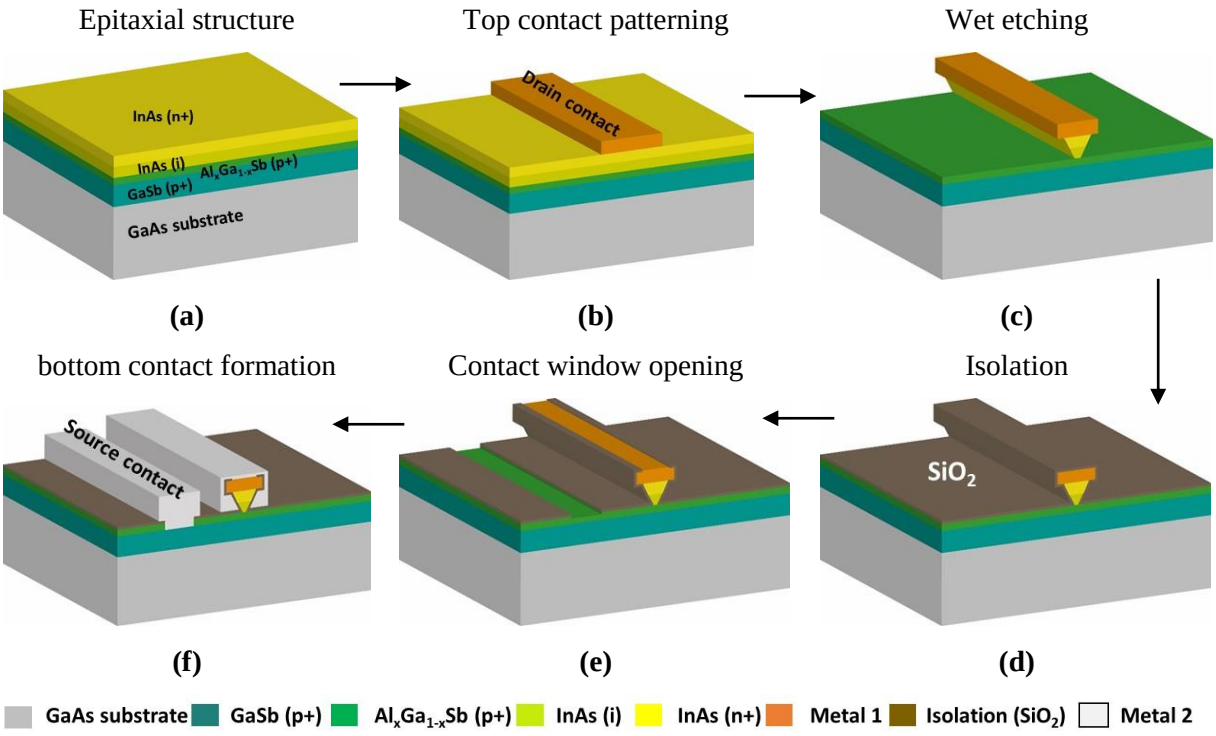


Figure 37: TD process flow cross-sectional schematic. (a) Epitaxial structure. (b) Formation of the top contact. (c) Wet etching of the mesa. (d) Insulating the substrate with SiO_2. (e) Contact window opening (via). (f) Bottom contact formation.

3.3 Tunnel Field Effect Transistor processing

3.3.1 Tunnel Field Effect Transistor Mask layout

With the additional gate terminal, the TFET mask consists of 5 EBL steps to pattern all the three terminals and 2 EBL steps for patterning the final large contact pads. These final contact pads have been designed to be compatible with the RF characterization tool. Similar to the TD mask design, the TFET mask consists in different drain contact sizes to access at very low tunnel junction widths.

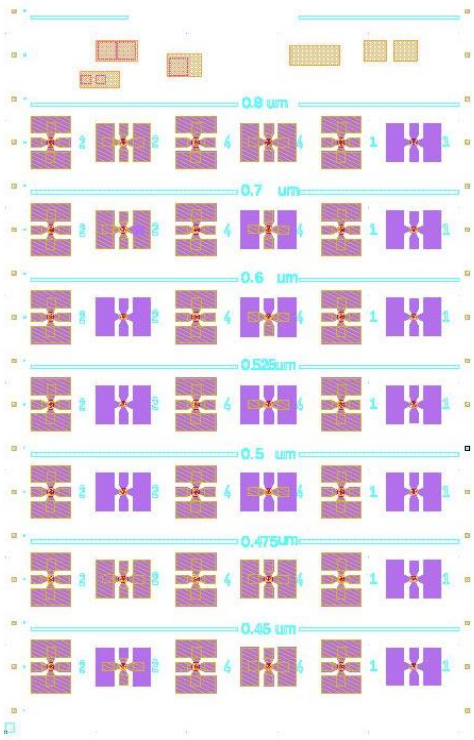
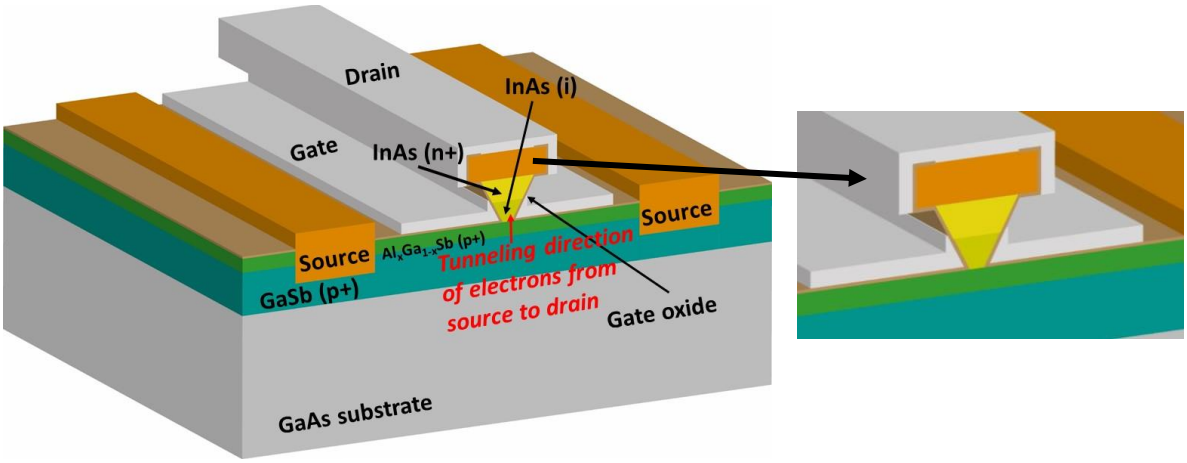


Figure 38: TFET-EBL mask layout. Top view of the mask showing vertical and horizontal devices of different lengths.

3.3.2 Tunnel Field Effect Transistor Process Flow

The TFET fabrication process flow (see Appendix II) is schematically shown in Figure 39 (a) and (b). Drain contacts (Ti/Au/Ti) of sizes varying from 4µm x 1µm down to 1µm x 250nm are fabricated in the [110] and [1-10] directions with respect to the substrate cut as shown in Figure 38. Drain contacts are used as hard masks for the successive anisotropic (phosphoric acid based solution) and selective (citric acid based solution) wet etching of InAs down to the AlGaSb source layer. This leads to different profiles for the mesa in the two different azimuths. A V-shape is obtained in the [110] orientation whereas a Λ-shape is observed in the [1-10] direction. After etching, the sample was treated with dilute HCl to remove the InAs native oxide prior to the deposition of 4nm Al_2O_3 by atomic layer deposition (ALD). Using plasma etching, the oxide layer was removed on top of the drain contact before the Ni gate evaporation. The nickel gate was evaporated by tilting the sample at an angle of 60° with respect to the Ni crucible in order to cover the entire InAs channel. Pd/Ti/Au was evaporated to form the source contact on the GaSb contact layer

after opening the Al_2O_3/AlGaSb source layer with plasma etching. The process was completed by the mesa isolation and the realization of air bridges connecting drain, source and gate to large pads deposited on the GaAs SI substrate.



- Ti/Au/Ti drain contact
- Wet chemical etching of mesa
- 4nm Al_2O_3 deposition
- Dry etching of Al_2O_3 on drain and source
- Two side gate formation
- Source contact formation
- Isolation
- Via opening
- Metal pads formation

Figure 39: TFET cross-sectional schematic and process flow steps.

3.4 Wet Chemical etching

The wet chemical etching to define the channel is the most critical step to fabricate a vertical TFET. An anisotropic wet etching process is used instead of a dry etching process to ensure there is no damage of the channel sidewalls due to the plasma etching process. Since the epitaxial layer design used here consists of an $Al_xGa_{1-x}Sb$/InAs heterojunction, it is important to control the etching process, due to the different physico-chemical reactions of the two materials with the etchant. Hence, a selective etchant that etches only InAs but

not $Al_xGa_{1-x}Sb$ is highly desirable. Therefore, wet etching must be stopped exactly at the InAs/AlGaSb source heterojunction to place a gate metal around the junction. For this channel definition step, different etching chemistries were compared and optimized.

3.4.1 Phosphoric acid based solution

Phosphoric acid (H_3PO_4) and hydrochloric acid (HCl) based etchants have been used in the literature to etch InAs [83]. Hence, a mixture of $H_3PO_4/H_2O_2/H_2O$ (2/1/4) was first studied to find out its feasibility to etch InAs over $Al_xGa_{1-x}Sb$ selectively. A 400nm thick InAs layer grown by MBE over a 50 nm thick $Al_{0.4}Ga_{0.6}Sb$ layer was used as a test sample for this study. Phosphoric acid based solution (PABS) with a volume ratio of [H_3PO_4: H_2O_2: H_2O = 2: 1: 4] was prepared, which resulted in etching 400 nm of InAs in 15 sec. As shown in Figure 40 (a) and (b), PABS etches both InAs and $Al_{0.4}Ga_{0.6}Sb$. The little under etching observed at the InAs/$Al_xGa_{1-x}Sb$ hetero-interface is not suitable for proper gate alignment at the junction [84]. Slight under-etching at the heterojunction of the source ($Al_xGa_{1-x}Sb$) could result in a poor gate control of the carriers in the channel.

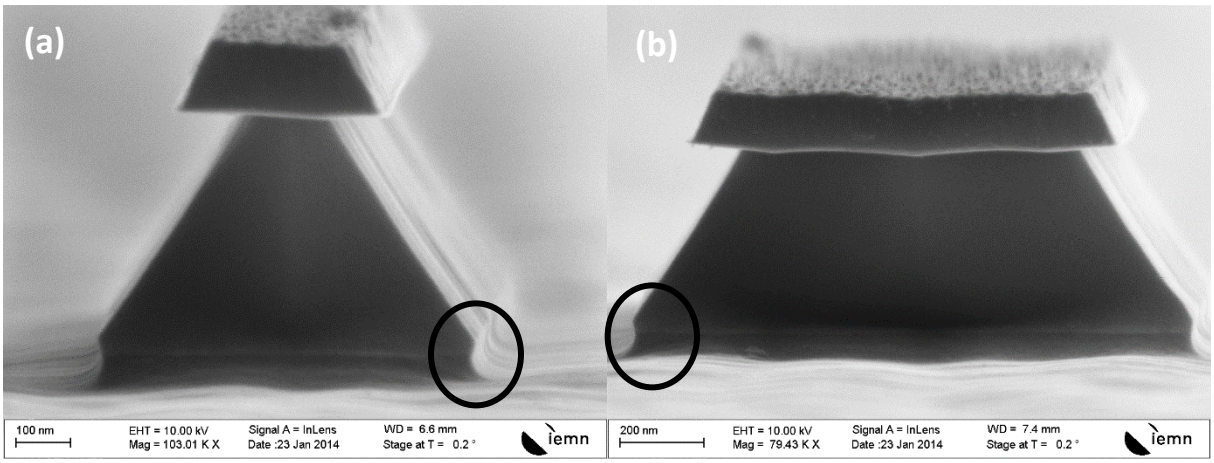


Figure 40: Wet etched mesa profile using PABS solution along the [1-10] direction for a drain contact size of (a) 0.35µm and (b) 1 µm.

3.4.2 Citric acid based solution

Selective wet etching of InAs over $Al_xGa_{1-x}Sb$ with a citric acid-based solution (CABS) has been reported in [85]. CABS was prepared from anhydrous citric acid ($C_6H_8O_7$) powder dissolved in deionized water (DI water) to get 1 mole/liter. 1 ml of hydrogen peroxide (H_2O_2) was added shortly before etching, in a 1 ml citric acid solution. An etch rate value of about 1.4 nm/s was found, very close to those reported by De Salvo *et al.* [86]. It can be seen from Figure 41 that the mesa and $Al_{0.4}Ga_{0.6}Sb$ surfaces are very smooth with no evidence of undercut at the hetero-interface. However, the undercut at the drain metal contact/n^+- InAs junction is large enough and hence, makes it difficult to place a gate over the entire channel. Gate underlapping increases the channel resistance for the carriers and eventually reduces I_{ON} as discussed in chapter 2.

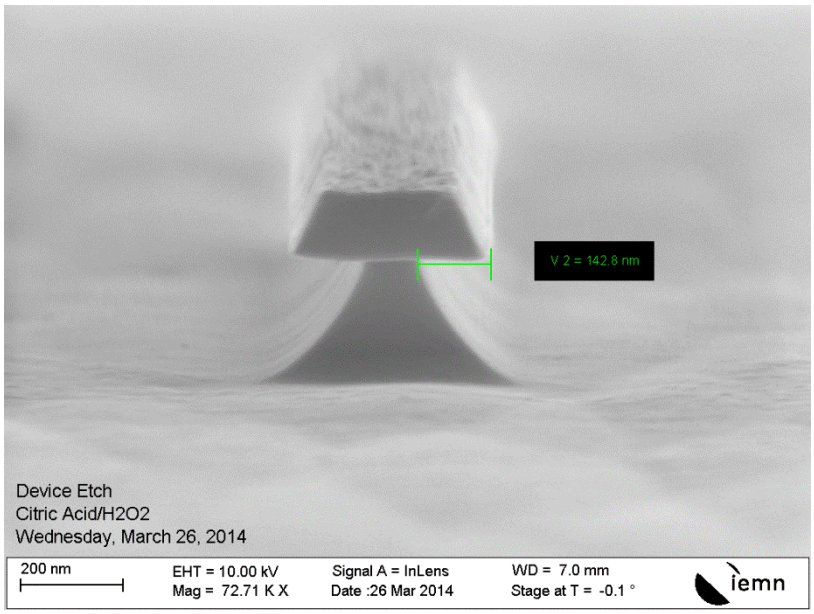
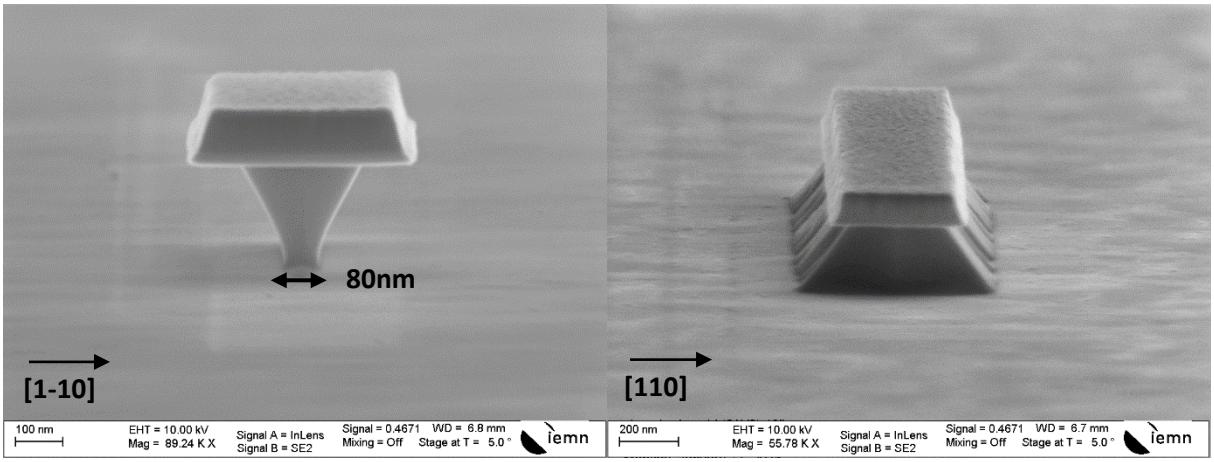


Figure 41: Wet etched mesa profile using CABS solution along the [1-10] direction for a 0.35µm drain contact size.

3.4.3 Phosphoric and Citric acid based solutions

Benefitting from the respective advantages of the two above-mentioned studies, a combination of the two etchants was tried to define the channel mesa.

In the first step a PABS was used to etch InAs until there was 30nm left followed by a second step of CABS used for a soft landing on the $Al_xGa_{1-x}Sb$ layer. PABS solution reduces the under-cut at the drain metal contact/n^+ (InAs) and CABS solution achieves good selectivity over $Al_xGa_{1-x}Sb$. As the wet etching follows the crystalline orientation of the material, the etch rate and the profiles obtained are different for different orientations. Figure 42 (a) and (b) show that the anisotropic wet etch yields V-shape and Λ-shape profiles for the drain metal contact oriented along [110] and [1-10] directions respectively after etching with PABS+CABS solutions.



(a) **(b)**

Figure 42: Wet etched mesa profile using PABS + CABS solutions oriented along (a) [110] and (b) [1-10].

As discussed in the mask design section different drain metal widths have been used to access at the smallest hetero-interface junction possible. Tomioka *et al*. [87] reported a SS value of 25 mV/decade for a nanowire with a diameter of 30 nm, thanks to a very good gate electrostatics. There are several factors like epitaxial layer thickness, drain contact metal width, orientation of the device, etch time and material composition that influence the final hetero-interface junction width. Figure 43 shows some of the profiles obtained for various InAs thickness. TDs (GaSb and S.I. GaAs substrates) require no intrinsic zone and no gate terminal, so the wet etching of InAs results in a foot width of 10nm and a height around 63nm, as shown in Figure 43 (d). The results reported are on structures fabricated

without the need to use critical point drying (CPD). These results show that, scalability is not an issue by using this process to obtain very narrow channel widths down to 10nm.

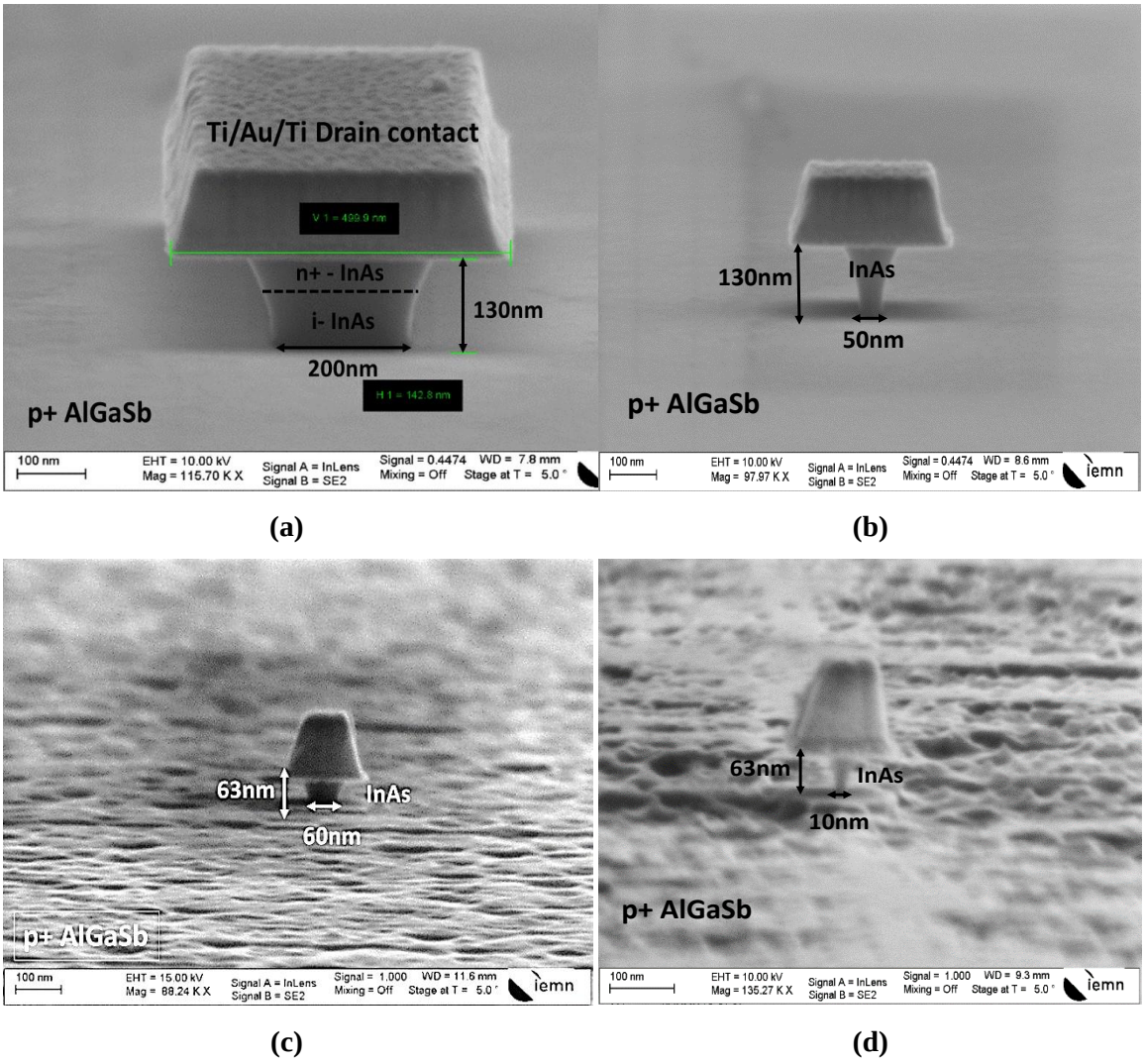


Figure 43: Wet etched mesa profiles obtained on different heterostructuress achieving a tunnel junction width of (a) 200nm (b) 50nm (c) 60 nm (d) 10nm.

3.5 Gate Oxide deposition

A large value of SS in experimental TFET is often due to the high concentration of oxide-semiconductor interface defects (D_{it}) which reduces the gate control over the channel charge [88]. For this purpose, a gate dielectric allowing low D_{it} at the channel semiconductor/oxide interface is highly desirable. Therefore, the sample was first treated with HCl based solution prior to the gate oxide deposition to remove any native oxide,

followed by rinsing in IPA [89]. The IPA beaker containing the sample was then transferred to the ALD chamber (less than 10 min) to avoid any kind of contamination.

The ALD system was first seasoned with Al_2O_3 by running the process recipe for 25 cycles. The sample in the IPA beaker was blow dried with N_2 and loaded in the ALD system. The time between drying and loading was kept below 1 min to reduce the native oxide formation. Deposition of Al_2O_3 has been done by delivering 0.015s Trimethylaluminum (TMA) and 0.025s water vapor (H_2O) pulses into the chamber in alternating cycles. Between TMA pulse and H_2O pulse, N_2 gas is purged to clean the non-stacked atoms from the surface. The schematic of the complete cycle is shown in Figure 44. Both TMA and H_2O were unheated and the liquid source temperature is maintained at 20°C.

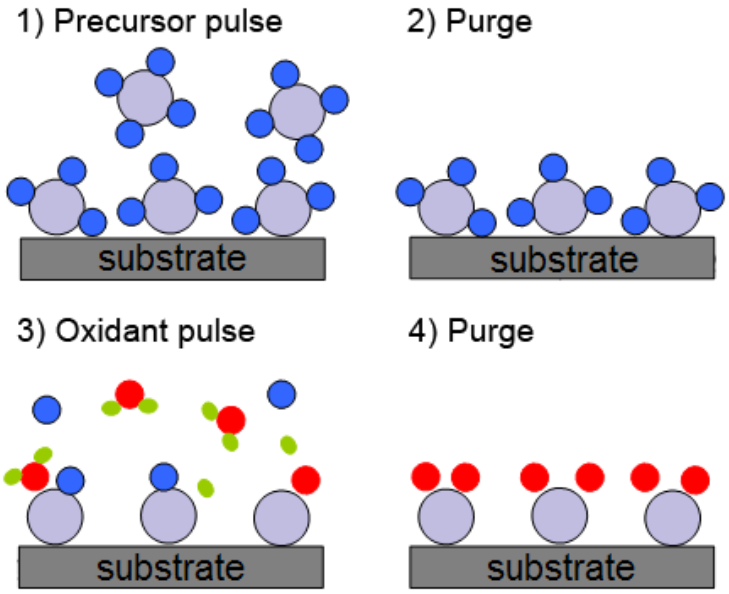


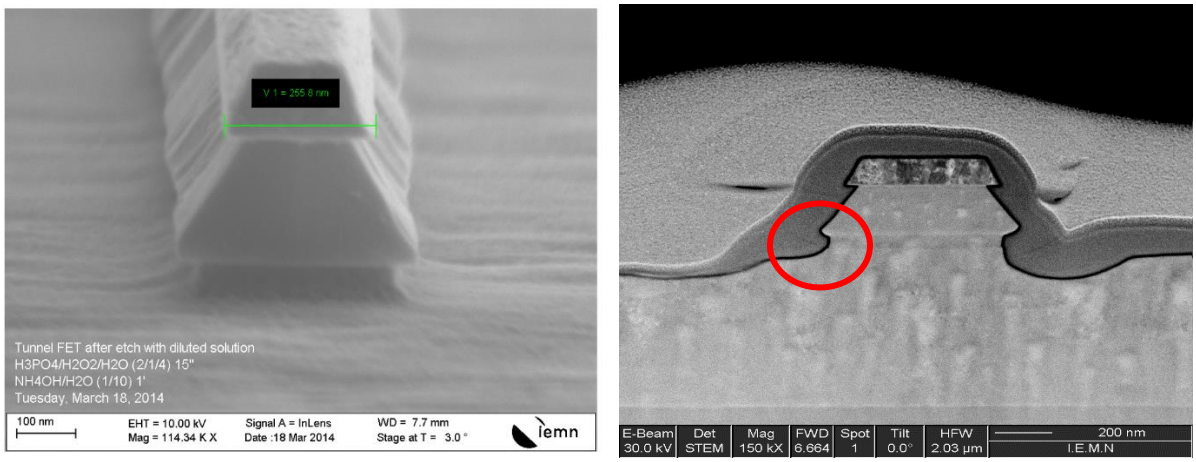
Figure 44: Schematic representation of the atomic layer deposition (ALD) process. By alternating Trimethylaluminum (TMA) and H_2O pulses, thin conformal Al_2O_3 films can be grown with atomic thickness resolution.

For all the samples processed during this work, the substrate temperature was held at 300°C during the oxide film growth, and 40 alternating cycles of TMA and H_2O exposure were completed, resulting in a conformal deposition of 7 nm (TFET-I, see chapter 4) or 4 nm (TFET-II and III, see chapter 4) Al_2O_3 dielectric film as confirmed by ellipsometry.

Since the material system used here is InAs/$Al_xGa_{1-x}Sb$, few pretreatments were investigated to observe the impact of the surface preparation.

3.5.1 Ammonia Treatment

Ammonia sulfide treatment is very popular among III-V materials for sulfur passivation before dielectric deposition [90]. We have first investigated with dilute ammonia, but this leads to an over etching of $Al_xGa_{1-x}Sb$ as shown in Figure 45. The resulting undercut would eventually impact the gate alignment over the hetero-interface.



(a) **(b)**

Figure 45: Dilute ammonia pre-treatment test. (a) SEM image showing the undercut at the tunnel junction. (b) STEM imaging showing the impact of the pre-treatment.

3.5.2 Dilute HCl treatment

Dilute HCl treatment is also well known for InAs surface treatment prior to gate oxide deposition [89]. Figure 46 shows that a smooth surface without under or over etching of $Al_xGa_{1-x}Sb$ is obtained. Therefore, all the TFETs fabricated during this work have been pre-treated with a dilute HCl solution (1:10).

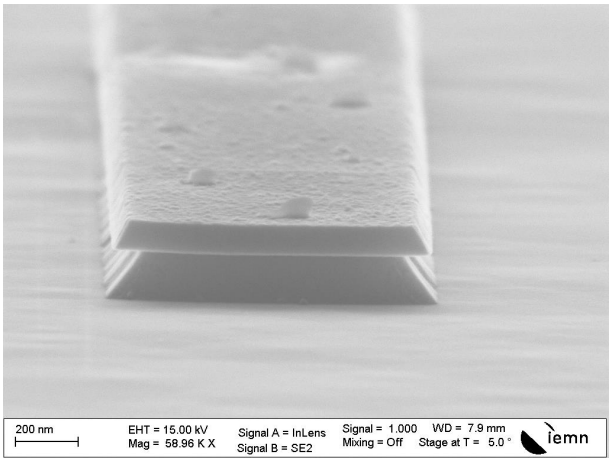


Figure 46: Dilute HCl pre-treatment.

3.6 Dry etching of Oxide on Drain and Source regions

Since the ALD deposition of Al_2O_3 is conformal and distributed on the whole substrate, it is necessary to open this oxide on the drain and source regions to contact them before gate metallization. Although HF-based solution is popular for selective removal of ALD deposited Al_2O_3, the obtained result was unexpected. It can be seen in Figure 47 that the HF solution creeps under the gate and also etches InAs damaging the device. To circumvent this problem, we have adopted a plasma etching process using BCl_3 chemistry to etch 4nm Al_2O_3 using a RIE-ICP tool. This is realized by defining vias through PMMA as shown in Figure 48.

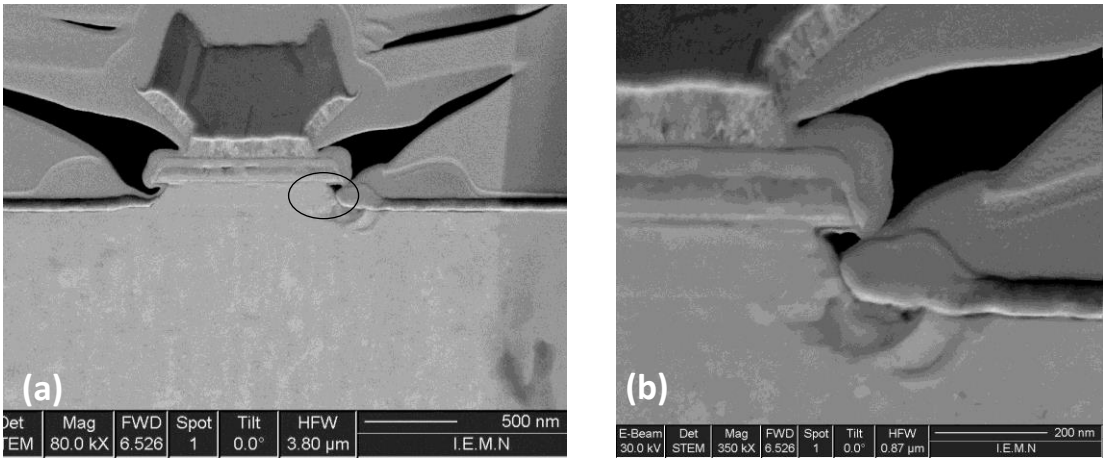


Figure 47: Cross-sectional STEM images showing the impact of using a HF solution to etch Al_2O_3 oxide. (a) Full device and (b) zoom under the gate.

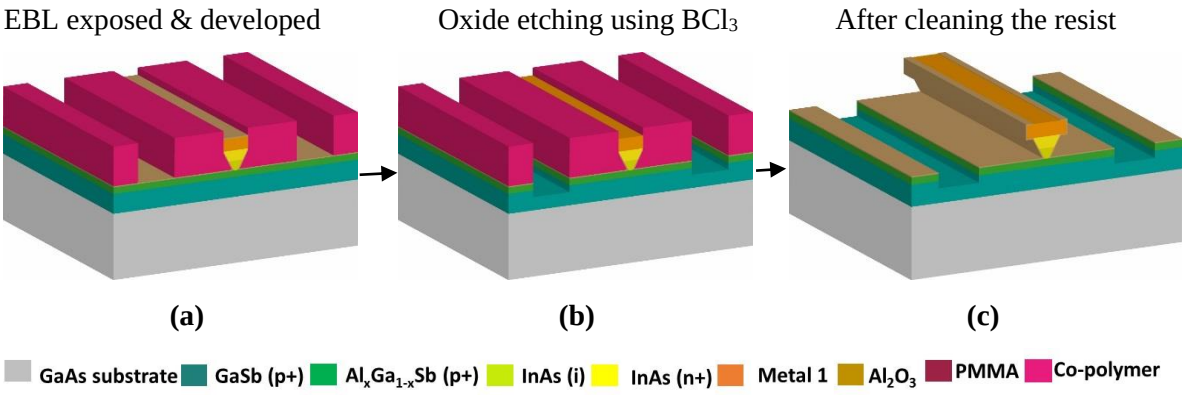


Figure 48: Process flow of window opening on source and drain areas to etch Al_2O_3, defined by Electron beam lithography (EBL). (a) Window opening defined by EBL. (b) Plasma etching using BCl_3. (c) Lift-off.

Interestingly, BCl_3 chemistry also etches 'Sb' based compounds as shown in Figure 49. This is especially advantageous to make contact on the GaSb contact layer because AlGaSb-based compounds quickly oxidize when exposed to air resulting in poor ohmic contacts. Figure 49 reveals that sharp profiles can be achieved by plasma etching. This result indicates that a vertical nanowire kind of profile with high aspect ratio could be obtained and leads to a valuable solution for TFET to switch device abruptly with good electrostatic control over the channel [91].

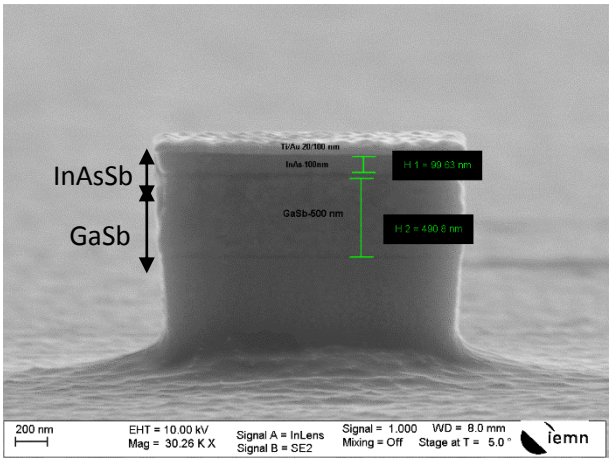
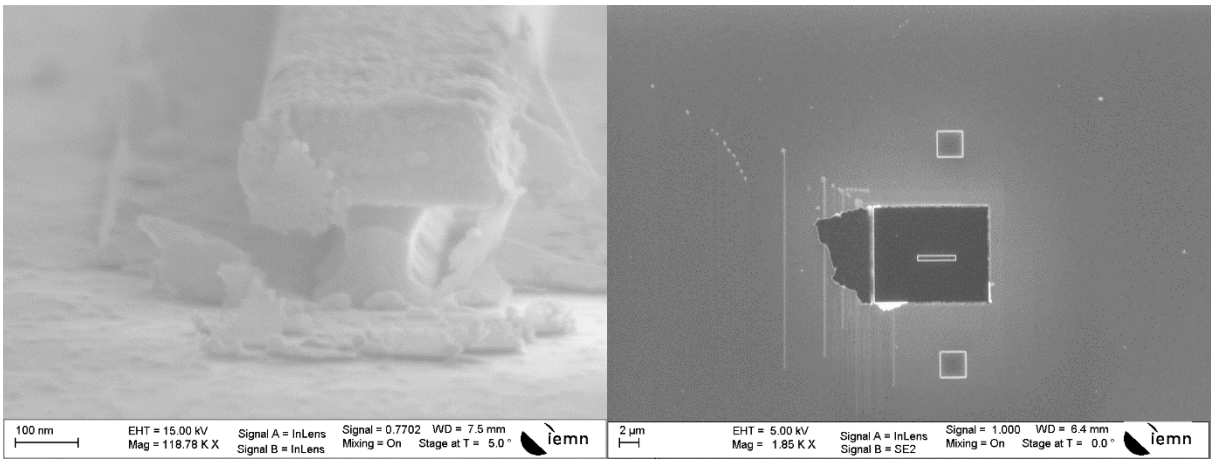


Figure 49: Cross-sectional SEM image showing 'Sb' based material etch using BCl_3 chemistry.

3.7 Gate Patterning

After plasma oxide etching through vias defined by EBL, the next step is the gate patterning. An efficient gate control of the charge in the channel requires gate metal to be placed accurately over the tunnel junction, to ensure abrupt switching.

Contrarily to the Λ-shaped device, the gate metal deposition for the V-shaped device is not straight forward as the junction widths are 25nm – 80nm, which is difficult to access while still covering the entire channel. So, the evaporation of the gate metal for V-shaped devices has been done in multiple steps. To access junction widths as low as 25nm – 80nm, the sample was tilted to 60^0 and rotated continuously with respect to the metal crucible to deposit the metal over the entire channel. However, upon lifting-off, the gate metal was shorted with the drain contact as shown in Figure 50 (a) and (b).



(a) **(b)**

Figure 50: (a) Cross-sectional SEM image showing that the gate metal is shorted with the drain contact when the sample is tilted to 60^0. (b) Top-view SEM image showing the metal residue around the corners of the gate metallization resulted from poor-lift-off process.

It is clear from Figure 50 (b) that metal residue around the gate metallization is due to the insufficient development of the bottom layer of the resist stack (copolymer+PMMA). This result is principally due to the angle necessary for the metallization. Poor lift-off process resulted in shorting of the drain and gate contacts. To avoid this, the bilayer is

treated additionally with methanol/IPA solvent to get an over development of the bottom resist layer as shown in Figure 51 (c). Methanol/IPA solvent is highly selective to develop copolymer without further developing PMMA. Then, the metallization is performed with a 60° tilt angle, to avoid metal deposition on the sidewall of the copolymer as shown in Figure 51 (d).

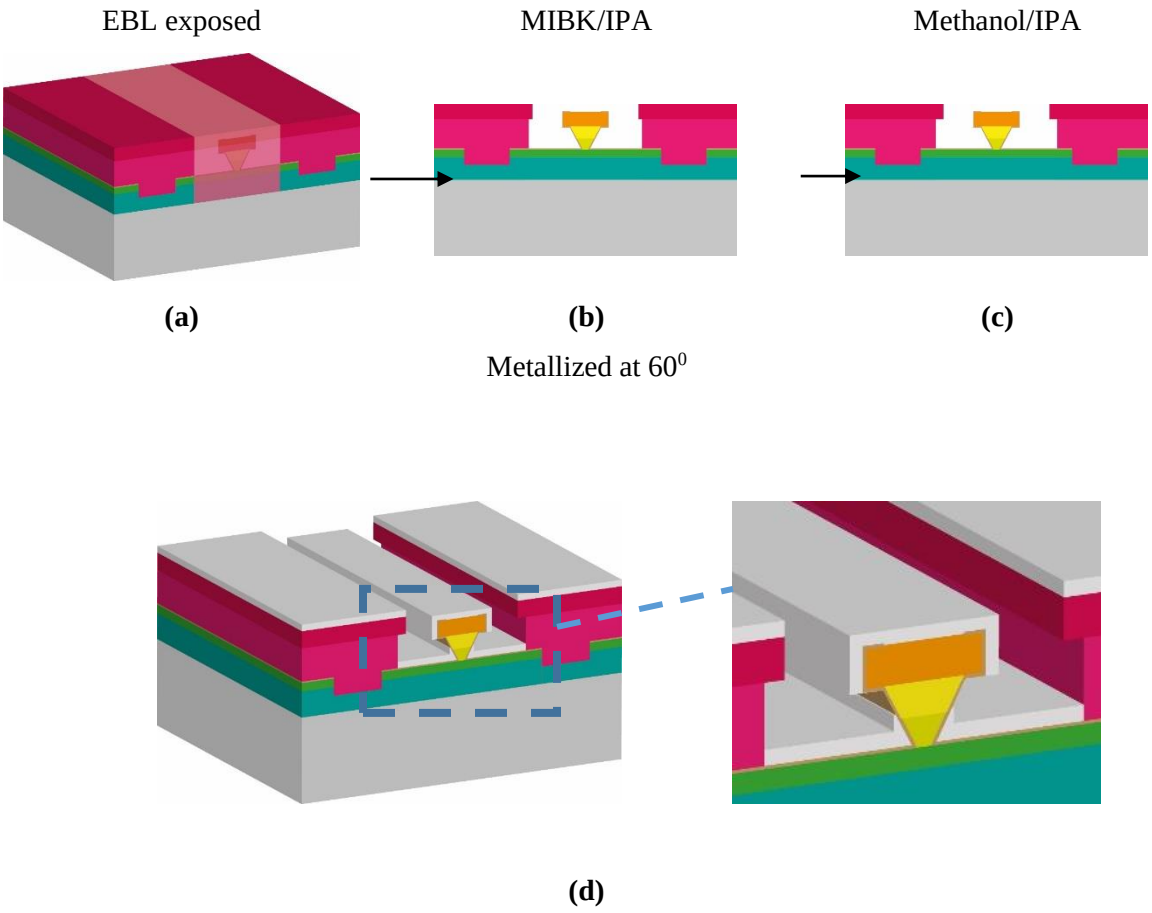


Figure 51: Schematic showing the optimized Process flow to metallize the gate at 60^0. (a) EBL exposure. (b) Resist Development. (c) Methanol/IPA treatment. (d) Metallization with a 60^0 tilt (zoom on the device region).

Figure 52 shows the cross-sectional SEM images of the gate metallization resulting from the optimized lift-off process. It is clear from the SEM picture that there is no shorting

between the gate and drain contacts, and the lift-off process is very appealing as there is no residue around the corners of the gate metallization as shown in Figure 52 (c).

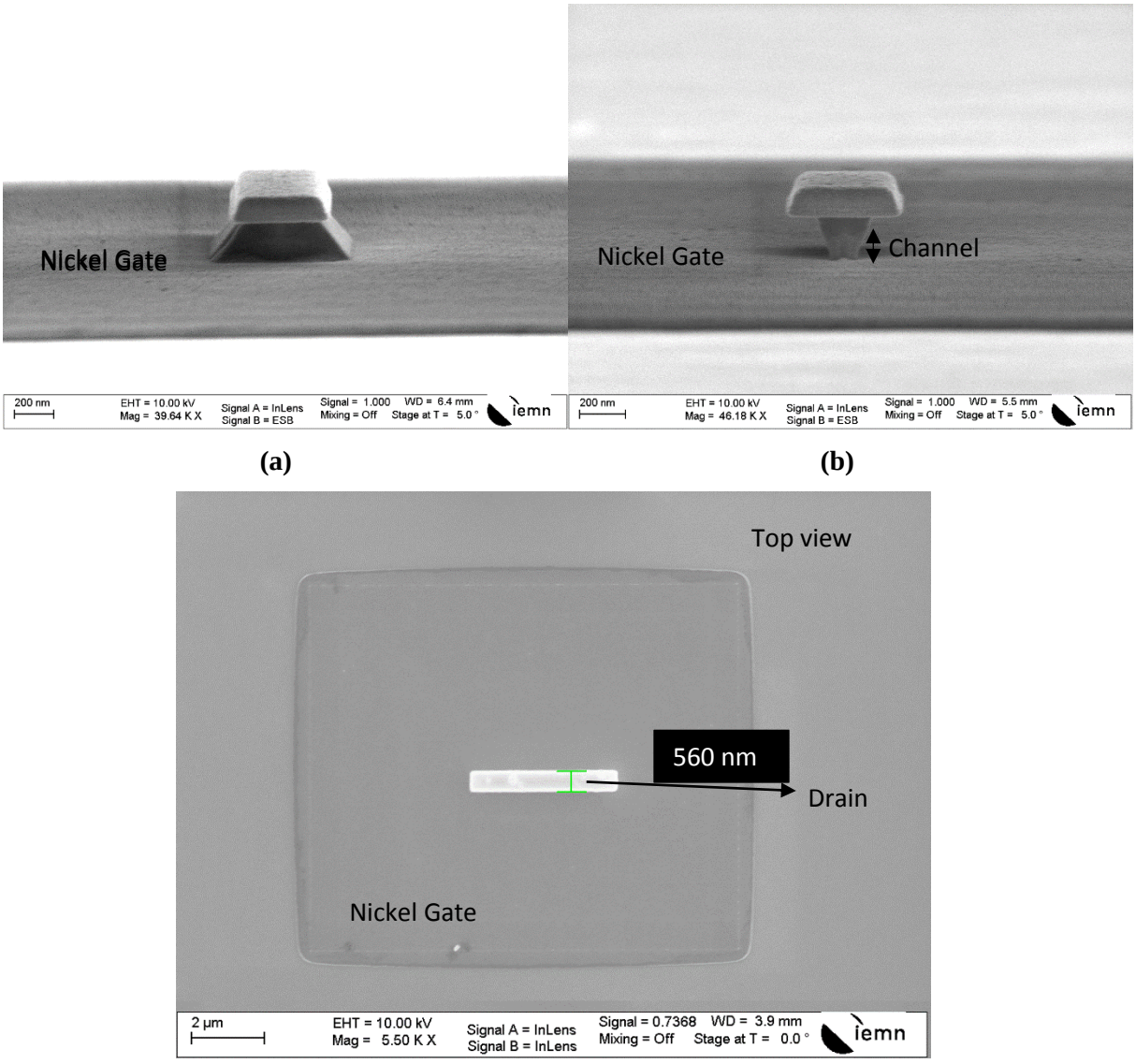


Figure 52: SEM images of gate metallization for devices oriented in (a) [1-10] and (b) [110] and (c) top view showing the gate metallization and drain.

STEM imaging is done to accurately measure the gate overlap and underlap to the channel. Figure 53 (a) and (c) show that for the Λ-shaped device the gate metallization completely overlaps the channel and the n^+ drain. While for the V-shaped device, the gate metallization slightly underlaps the channel (Figure 53 (b) and (d) respectively).

Underlapping of the channel is due to the large under-cut observed at the drain/n^+ interface, which can be engineered to achieve total overlapping of the gate metal over the channel.

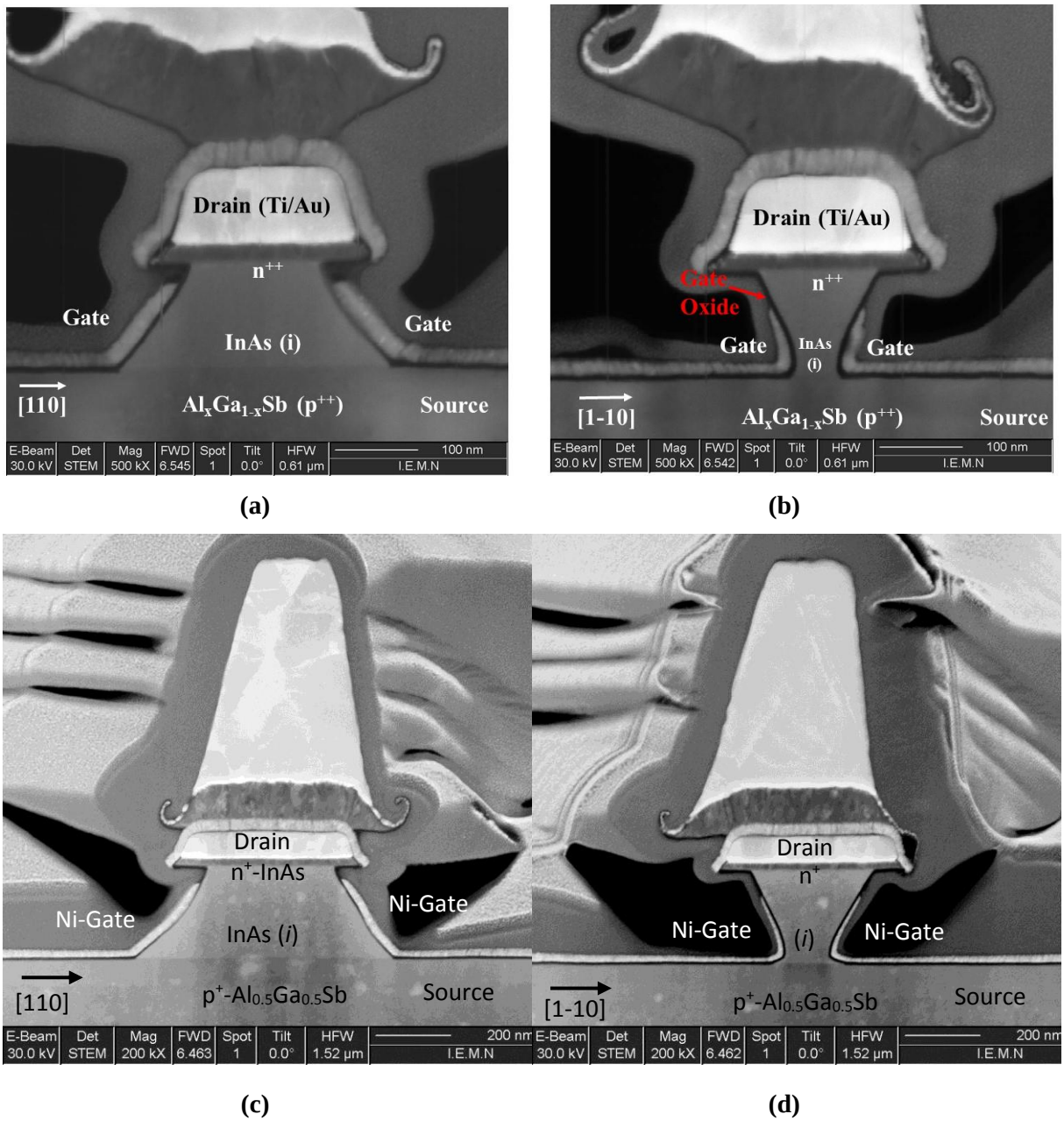


Figure 53: Cross-sectional STEM image of a fabricated vertical TFET device (a), (c) Λ-shape in [1-10] and (b), (d) V-shape in [110] direction.

3.8 Source contact

Normal lift off technique is used to pattern the source contacts. But prior to metal deposition, TDs and TFETs were always treated in chemical solution to wet etch the top surface of the buffer layer to achieve good ohmic contacts. Wet etching solution varies depending on the type of contact layer used to accommodate the mismatch.

For instance, the optimized epitaxy includes an n^+-InAs buffer layer that forms an additional tunnel junction with the p^+-source. Detailed electrical behavior characteristics explaining the impact of the ohmic contact and the influence of the buffer material will be discussed in chapter 4. Figure 54 shows the top view SEM image taken after the source contact formation.

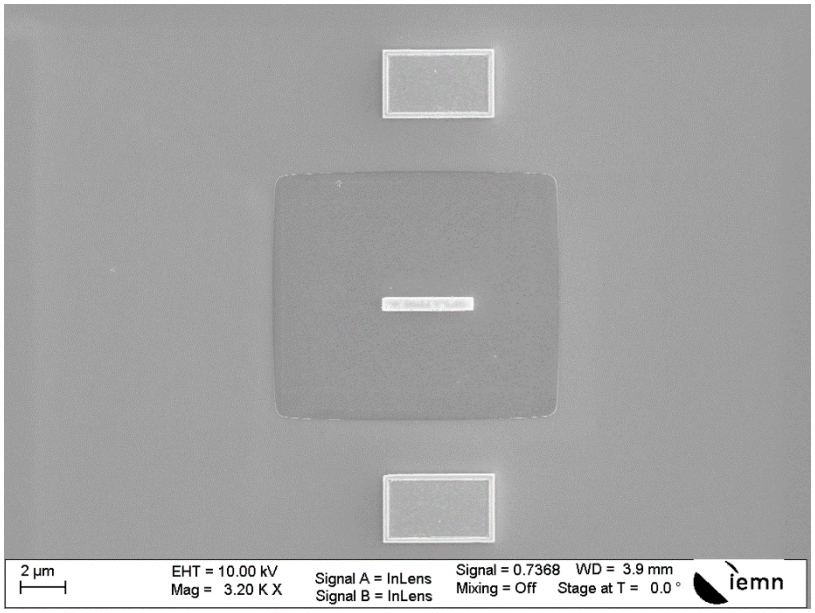


Figure 54: SEM image showing the source contact formation

3.9 Insulation of devices

On semi-insulating substrates, **t**o hinder any leakage current from device to device through the substrate, insulation is done for both tunnel diodes and TFETs. On conductive substrates, SiO_2 deposition is used for contact insulation.

For TDs (on GaSb and S.I. GaAs substrates) grown on GaSb and GaAs substrate, the insulation is done by SiO_2 deposition over the entire substrate using plasma enhanced chemical vapor deposition (PECVD). SiO_2 acts as an interlayer dielectric (ILD) providing insulation between the source contact and drain contacts. Compared to the LPCVD technique, high quality oxide can be deposited at much lower temperatures (300^0C – 400^0C) by PECVD. In our case, 30nm SiO_2 was deposited at 300^0C. After the deposition, vias on top of the drain and source regions are defined by EBL and etched back using reactive ion beam etching (RIE) up to the contacts to prepare the sample for large contact pads.

For TFETs on GaSb (TFET-I will be discussed in chapter 4), insulation with PECVD deposited SiO_2 is not the best solution since the gate metal used is degraded upon high temperature treatment, leading eventually to device failure. That is why for TFETs on GaAs (TFET-II and III discussed in chapter 4), insulation has been done by patterning a negative resist (SAL 601) defined by EBL as a protective mask for etching the buffer layer down to the substrate. Refer to the Appendix I for a detailed process flow on SAL 601. The Al_2O_3 covering the entire surface was first dry plasma etched using BCl_3 chemistry followed by a wet chemical treatment to etch the buffer down to the substrate. When the GaSb buffer was etched with HF and HCl based solutions, the etch time was 3’ and 5’ respectively to etch about 650 nm and the observed undercut was very large as shown in Figure 55 (a) and (b). In order to reduce the large undercut of the GaSb buffer due to the HF and HCl based solutions (Figure 55 (c)), a tartaric acid based solution was used [85]. The etch time of the GaSb layer was also reduced from 5 to 2 mins. Figure 56 shows the mesa insulation performed using tartaric acid based solution.

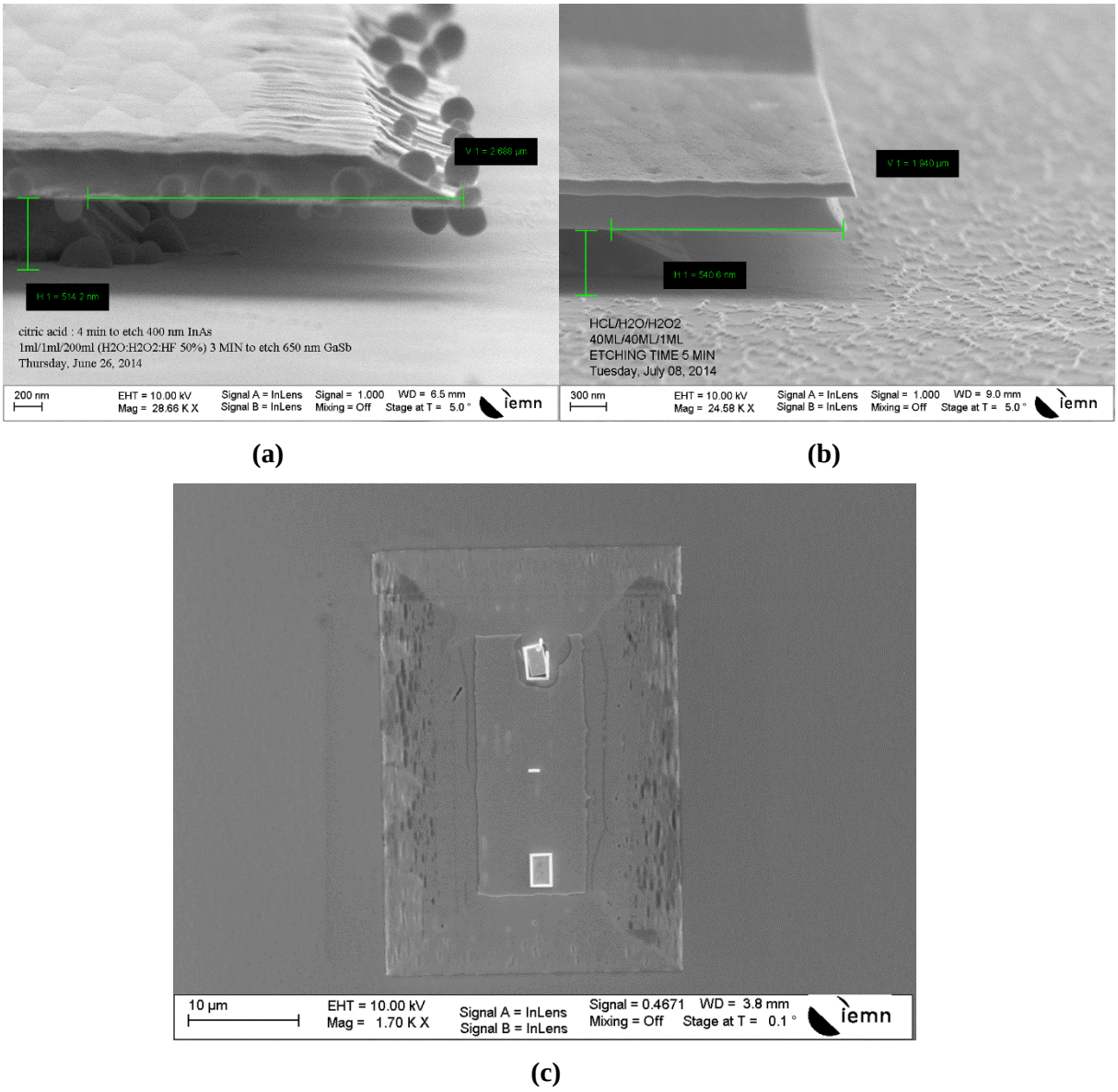


Figure 55: SEM images showing the etching of 650nm GaSb buffer using (a) a HF solution (b) a HCl solution and (c) under etching impact.

It can be seen clearly from Figure 55 (c) that the epitaxial layers (TFET on GaAs-sub with GaSb buffer) are not perfect. Wet etching of the mesa reveals the presence of dislocations in the epilayer. On the mesa sidewall the dislocation density is higher near the GaAs substrate/GaSb buffer interface, as can be observed in figure 54. These dislocations might cause trap assisted tunneling (TAT) thereby increasing the OFF current of the TFET. For TFET-III in chapter 4, an InAs buffer layer was used to avoid relaxation of the thick

InAs channel. Etching of the InAs buffer is almost similar to the wet etching of the channel mesa. The influence of the dislocation density on the electrical characteristics will be discussed in detail in chapter 4.

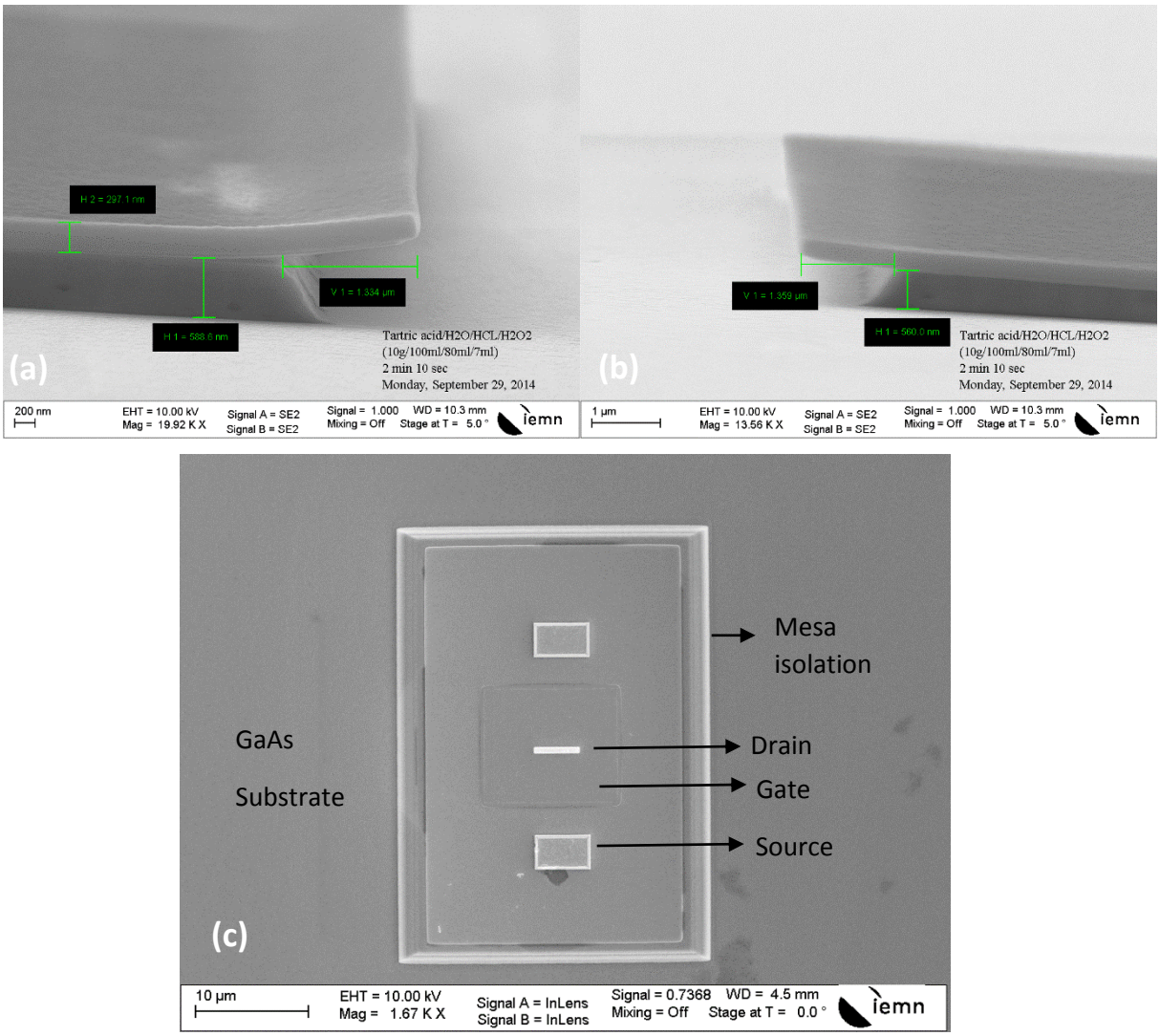


Figure 56: Wet mesa etching of GaSb buffer using a tartaric acid solution. (a), (b) cross section SEM image and (c) top view after mesa isolation.

3.10 Large contact pads

3.10.1 Tunnel Diodes

As described in section 3.1, TD process is kept simple, so after insulation with SiO_2, large openings are defined by EBL and metallization is done by tilting the sample at 20° to avoid disconnection.

3.10.2 Tunnel FETs

For TFETs, as the contacts are small, placing the tips to perform electrical characterization is difficult. Dedicated air bridges are patterned to connect Gate, Drain and Source contacts to the large contact pads simultaneously.

Two resist patterns are needed to finish the air bridges. In the first level, the PMMA resist is patterned, which acts as a supporting layer to allow the bridge resting in air. An additional reflow step at 170^0 C is performed to smooth the corners and sidewalls of the resist. The influence of the reflow of resist can be seen in Figure 57, where the corners of the device were rounded reducing the risks of disconnection.

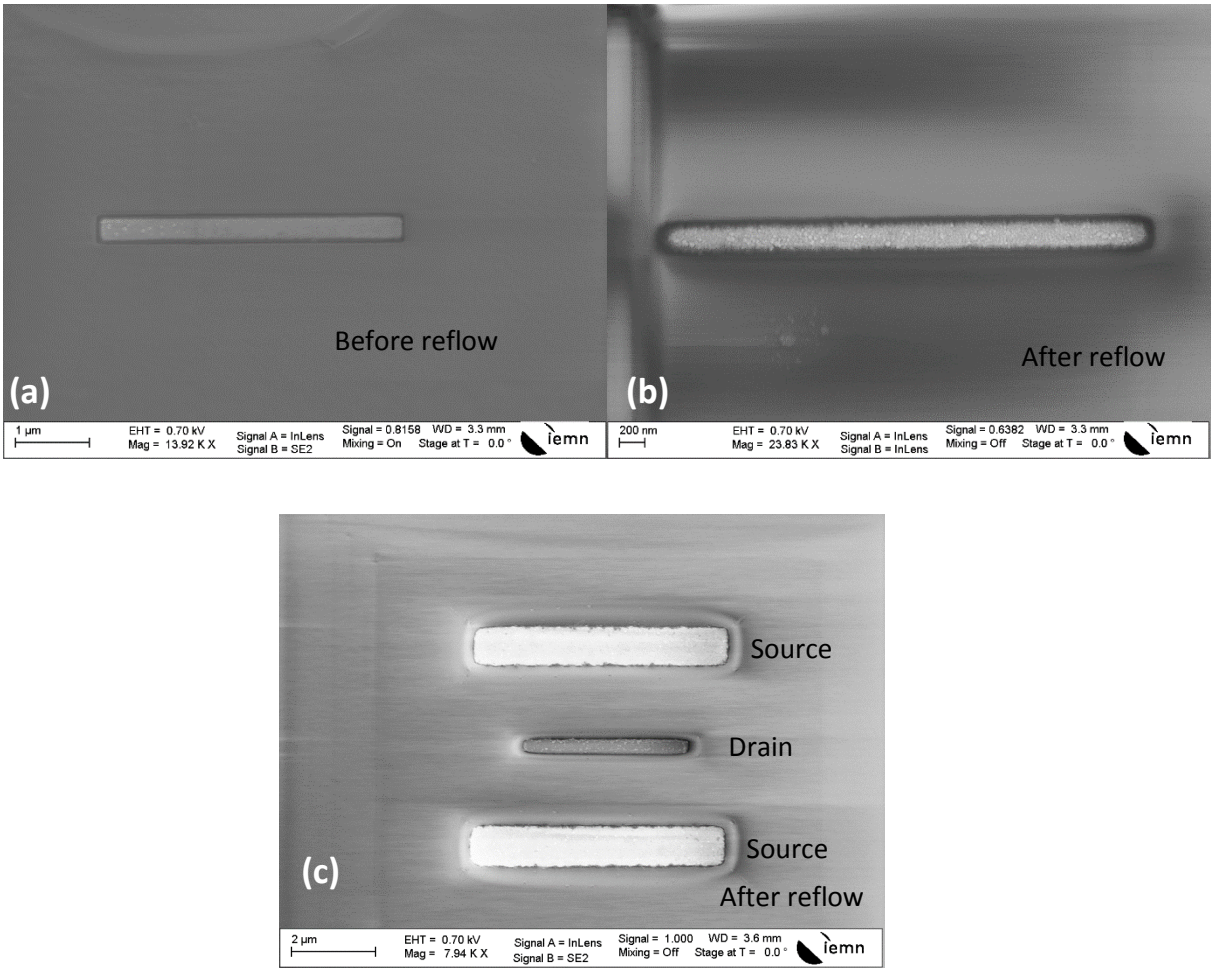
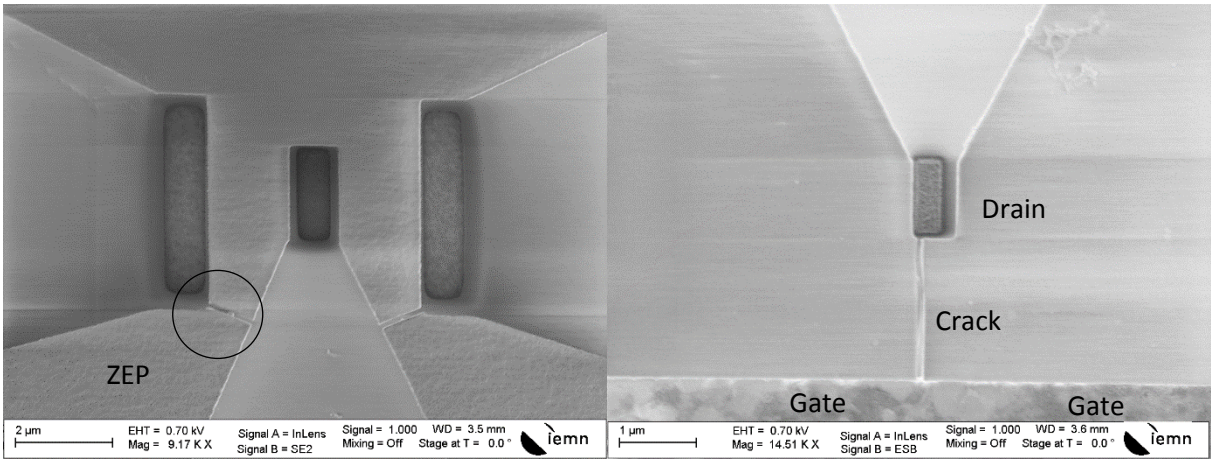


Figure 57: SEM images showing the via opening and post exposure bake to fabricate the air bridges. (a) After the EBL exposure without baking. (b) Round corners obtained after baking at 170^0C. (c) Round corners at source and drain openings.

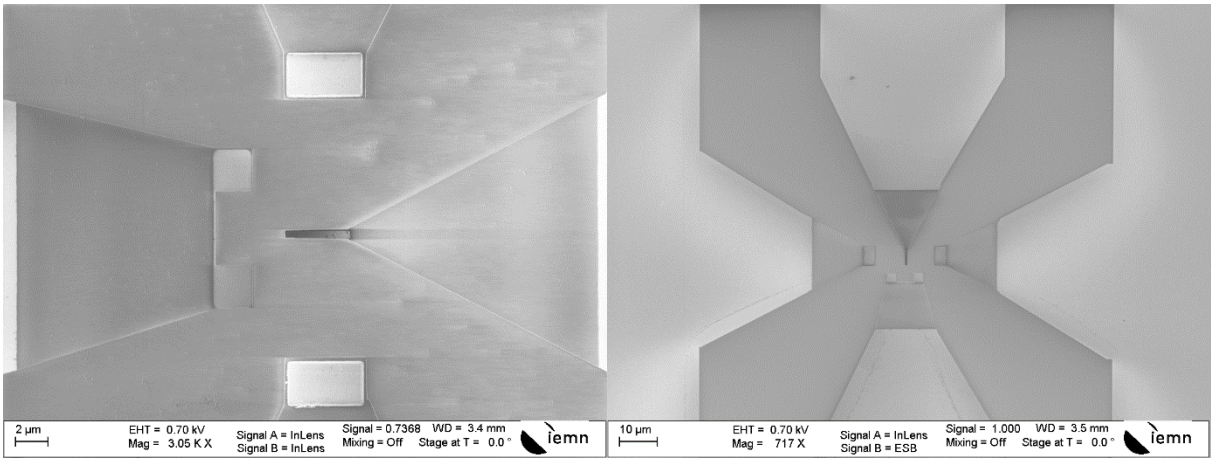
The second resist pattern is the opening for the metallization and is composed of a bi-layer resist stack for lift-off process. The bi-layer stack containing copolymer and ZEP is carefully chosen and the mask design is also optimized. Figure 58 (a) and (b) show that the ZEP in the bi-layer is cracked due to the over dose within short distance, which could result in shorting of the drain, source and gate if metallized. To avoid this problem, the mask design has been changed to increase the distance between the openings, and as a result cracks in ZEP can be avoided.



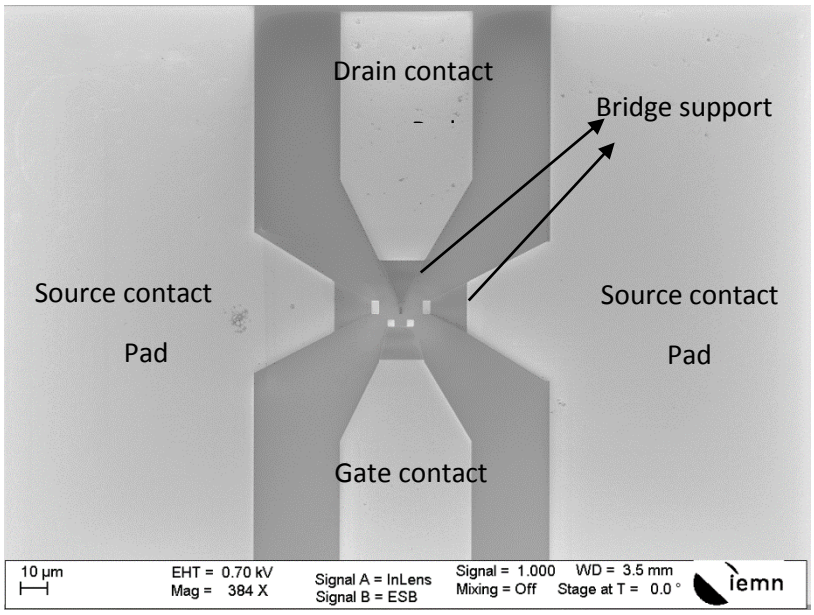
(a) **(b)**

Figure 58: SEM images showing cracks seen after developing ZEP. (a) Cracks obtained between drain and source. (b) Cracks obtained between drain and gate.

It can be seen from Figure 59 that there are no cracks with the optimized mask design and the development is very efficient. The fabrication process ends by metallizing the sample and lifting off. Figure 60 shows the fabricated vertical device with the contact pads connecting via the air-bridge process.



(a) **(b)**



(c)

Figure 59: (a), (b) and (c) SEM images taken after development of the second bridge lithography level. There are no cracks seen in ZEP with the optimized mask design.

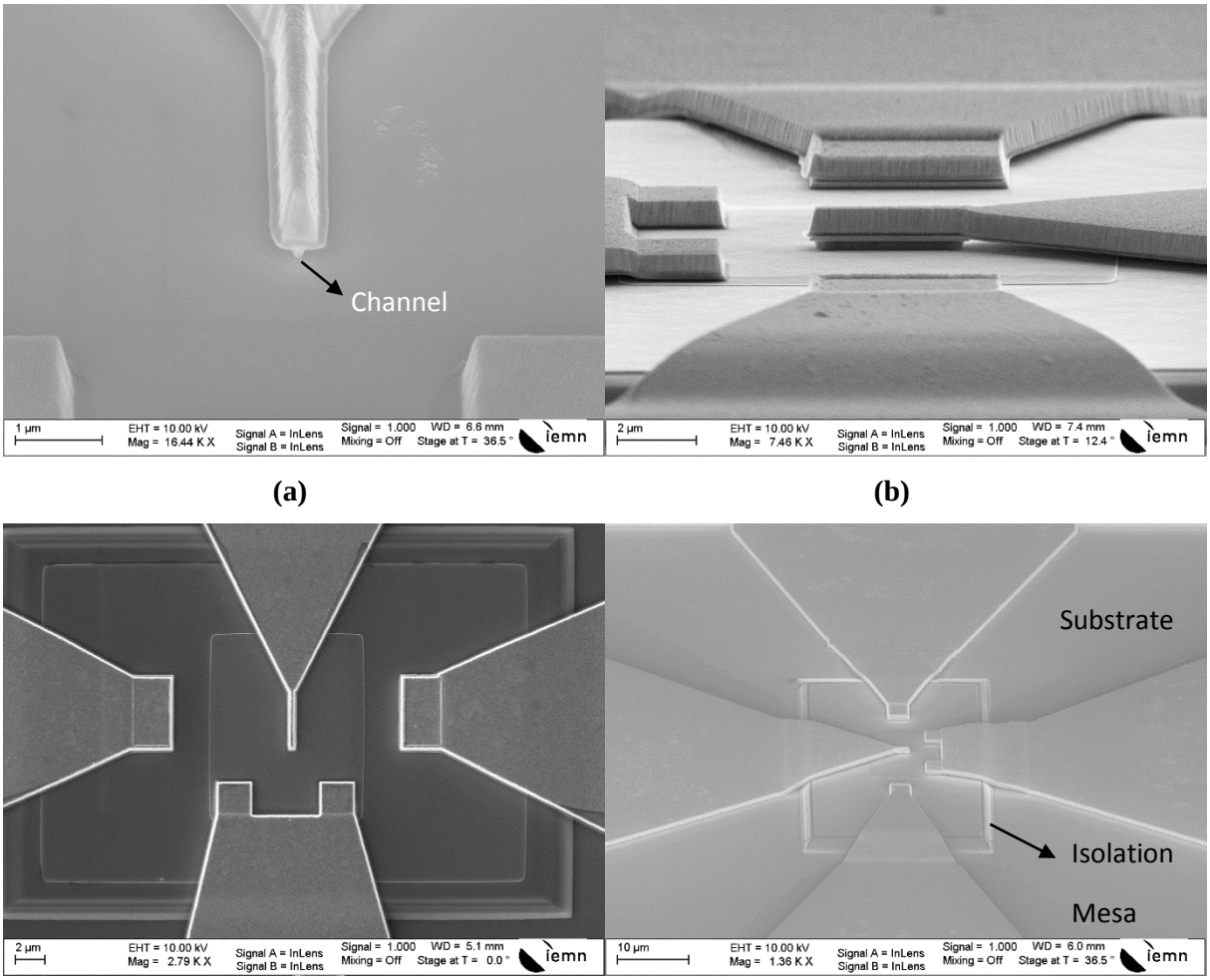


Figure 60: SEM images of (a) channel. (b) Air bridge zoomed at drain contact. (c) Top view of the air-bridge. (d) Tilted view.

Chapter 4: Results and Discussion

4.1 Introduction

In this chapter we present the electrical characterization of tunnel diodes and transistors in the InAs/(Al)GaSb system. We first report the results on the diodes fabricated on a lattice matched GaSb substrate to study the influence of the heterostructure design on the conductance properties of the heterojunction. The extraction of the conductance curves from the diode electrical characteristics has then been helpful to analyze the impact of defects when the diodes are fabricated on a highly mismatched GaAs substrate. From the insights gained from this study, we then present the characterization of different generations of TFET based on this heterojunction.

This chapter is therefore divided in two sections: diodes and TFETs. In each section, we start with describing the epitaxial structure used and the related band diagram generated with the TCAD Silvaco software. To this end we have used a modified value of the electron affinity (EA) in InAs (EA=5.1) to make the band alignments between (Al)GaSb and InAs consistent with the literature and experimental results. With the help of the electrical characteristics, each section details how we have enhanced the performance of the diodes and TFETs. Finally, the results of tunnel diodes and TFETs have been benchmarked separately with the results of the literature.

4.2 Diode Results

In this section we present the electrical results obtained on diodes fabricated using the process detailed in chapter 3. Different tunneling interfaces in the InAs/$Al_xGa_{1-x}Sb$ material system are studied in order to optimize the TFET performance. For this, we target the largest possible ON-conductance with the minimum leakage current and the steepest slope to pass from the ON to OFF state. The peak to valley current ratio is also a useful parameter to compare the quality of similar diodes with different dimensions or substrate.

4.2.1 Interface Optimization

Different InAs/$Al_xGa_{1-X}Sb$ based TDs grown on GaSb substrate have been studied to optimize the heterostructure design and reach the desired properties. We present here four different structures explaining our progression. These epitaxial structures, named TDI, TDII, TDIII and TDIV, and the associated band diagrams are displayed in Figure 61, Figure 62, Figure 63 and Figure 64 respectively. The effective band gap (E_{beff}) at the tunneling interface is progressively increased by moving from TD-I to TD-IV by increasing the Al content in (Al)GaSb. P+ and n+ regions of all the structures were doped with 'Si' with a doping concentration of $1x10^{19}$ cm^{-3} for p-type GaSb and n-type InAs. To minimize the impact of Si dopant in the tunneling process, 3nm-i-InAs and 3nm-i-anode type layer have been introduced before and after the tunneling interface for all the TD structures except for TD-III.

Tunnel Diode: I (TD-I)

57nm	InAs	Si($N_D=10^{19}cm^{-3}$)
3nm	InAs (**nid)**	
3nm	GaSb (**nid)**	
47nm	GaSb	Si($N_A=10^{19}cm^{-3}$)
300nm	GaSb	Si($N_A=2x10^{19}cm^{-3}$)
GaSb Substrate		($N_A=8x10^{18}cm^{-3}$)

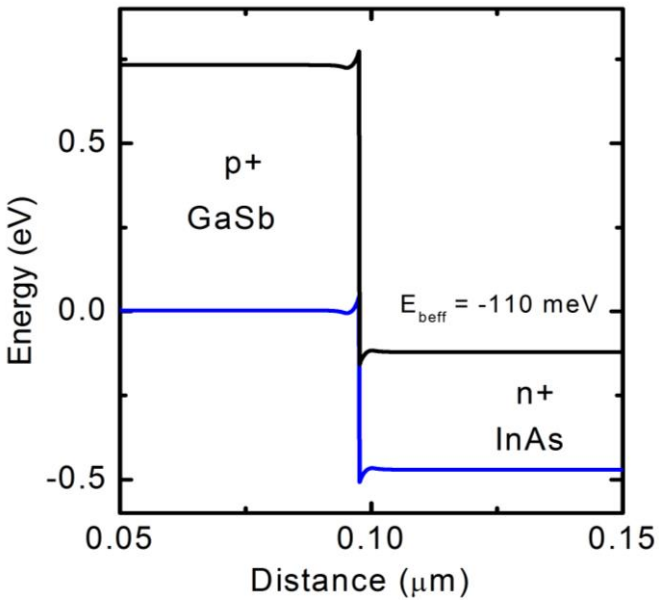


Figure 61: Epitaxial structure and band diagram of TD-I.

The InAs/GaSb forms a type-III broken band alignment at the interface. A valence band offset of 0.47 eV is assumed corresponding to an E_{beff} = -110 meV separation between the InAs conduction and GaSb valence band edges. Due to the broken band alignment, this

material design is thought to be ideal to achieve a large current density for TFET application. However, it is equally important to minimize the OFF state conductance, which is a big challenge with the broken gap alignment at the interface [92]. Therefore, it may be advantageous to insert a thin barrier in between to block the electron flow in the off-state regime.

For TDII, a 3nm-i-$Al_{0.4}Ga_{0.6}Sb$ layer has been inserted between InAs and GaSb. A 40% 'Al' content is chosen to align the 3nm-i-$Al_{0.4}Ga_{0.6}Sb$ valence band and the InAs conduction band edges in an attempt to cut-down the flow of electrons in the off-state regime

Tunnel Diode: II (TD-II)

57nm	InAs	Si($N_D=10^{19}cm^{-3}$)
3nm	InAs (**nid**)	
3nm	$Al_{0.4}Ga_{0.6}Sb$ **(nid)**	
47nm	GaSb	Si($N_A=10^{19}cm^{-3}$)
300nm	GaSb	Si($N_A=2x10^{19}cm^{-3}$)
GaSb Substrate		($N_A=8x10^{18}cm^{-3}$)

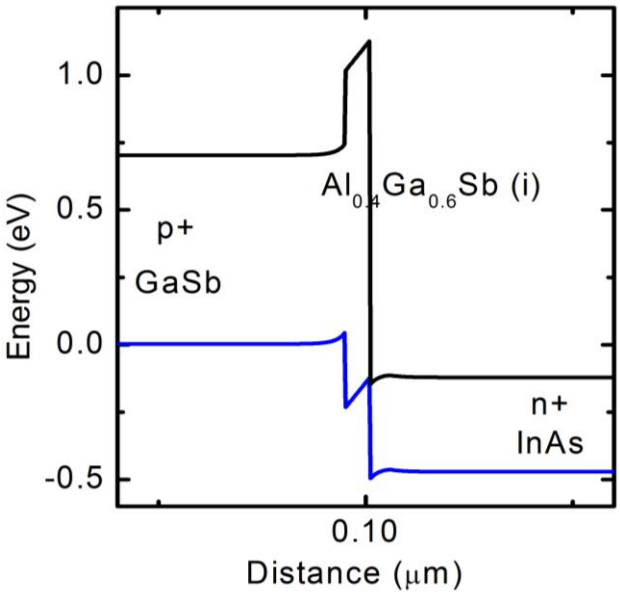


Figure 62: Epitaxial structure and band diagram of TD-II.

To increase further the effective tunneling barrier height (E_{beff}), TDIII is grown with an 'Al' composition of 50%. We get a type-II (staggered) band alignment with an E_{beff} height of 70 meV at the junction. It is evident from Figure 63 that increasing the Al content leads to a valence band edge spike between GaSb and $Al_{0.5}Ga_{0.5}Sb$, which could degrade the electrical performance of the diode. To smooth this offset, we introduce a graded 'Al' composition in TDIV, increasing the Al content from 20% to 60% before the tunneling interface.

Tunnel Diode: III (TD-III)

60nm	InAs	Si($N_D=10^{19}cm^{-3}$)
3nm	InAs (**nid)**	
50nm	$Al_{0.5}Ga_{0.5}Sb$	Si($N_A=10^{19}cm^{-3}$)
300nm	GaSb	Si($N_A=2x10^{19}cm^{-3}$)
	GaSb Substrate	($N_A=8x10^{18}cm^{-3}$)

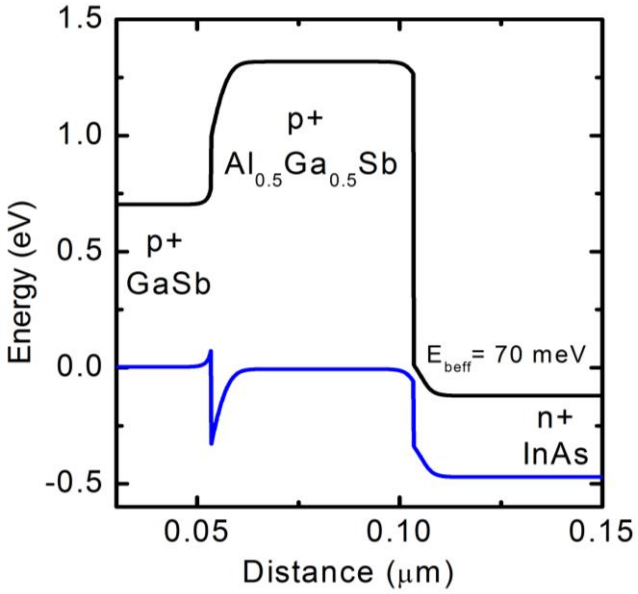


Figure 63: Epitaxial structure and band diagram of TD-III.

Tunnel Diode: IV (TD-IV)

60nm	InAs	Si($N_D=10^{19}cm^{-3}$)
3nm	InAs (**nid)**	
3nm	$Al_{0.6}Ga_{0.4}Sb$ **(nid)**	
47nm	$Al_xGa_{1-x}Sb$ $0.2<X<0.6$	Si($N_A=10^{19}cm^{-3}$)
300nm	GaSb	Si($N_A=2x10^{19}cm^{-3}$)
GaSb Substrate		($N_A=8x10^{18}cm^{-3}$)

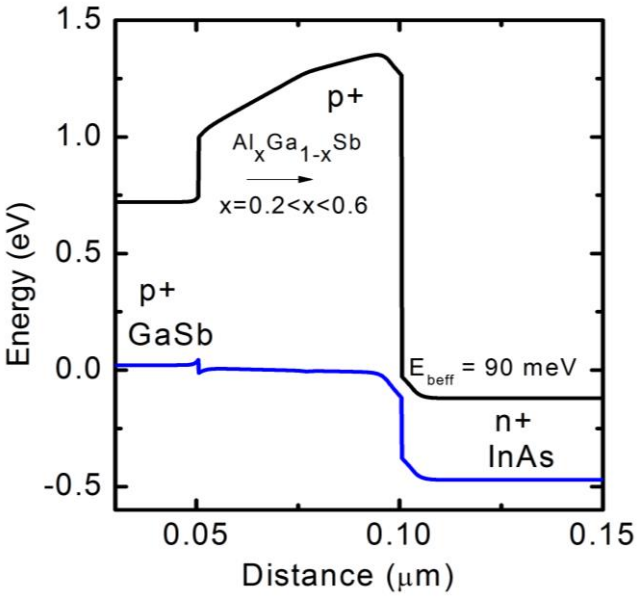


Figure 64: Epitaxial structure and band diagram of TD-IV.

Figure 65 compares the I-V electrical characteristics of the above detailed epitaxial structures. All the curves (Figure 65a) show an Esaki diode behavior. Negative differential resistance (NDR) can be observed for all the TDs, which is a signature of BTBT transport of carriers. As expected, the broken band alignment (TD-I) results in the highest peak current density of 159 $kA.cm^{-2}$ compared to TD-II, TD-III and TD-IV (table I). For the

same size (0.5x1 μm^2) and same orientation of the drain contact, the valley current of TD-II is lower than that of the other designed structures. This can be attributed to the 3nm-intrinsic AlGaSb layer. Comparing TD-I, TD-III and TD-IV, the excess valley current and the peak current gradually decrease with the increase of the effective barrier height (E_{beff}) at the junction (Table 4). This indicates that E_{beff} is the main parameter determining the tunneling properties of the TDs.

The conductance curves for all the TDs are extracted from the I-V characteristics and compared in Figure 65b. It is evident from Figure 65b that there is a major improvement in the steepness of the conductance slope as the E_{beff} height at the interface is tuned from broken to staggered band alignment. Additionally, the minimum conductance decreases significantly for TD-II with the insertion of 3nm-i-$Al_{0.4}Ga_{0.6}Sb$. This is an indication that employing a staggered band alignment at the interface minimizes the off-conductance. However, the on-conductance is much lower in this case because the intrinsic AlGaSb layer fixes the tunneling distance at 3 nm between the valence band of GaSb and the conduction band of InAs whereas for other samples, the tunneling distance can be reduced with the backward voltage. A steep conductance slope of 167 mV/dec is observed for InAs/$Al_{0.5}Ga_{0.5}Sb$ (TD-III) and a better on-conductance is obtained for TD-IV thanks to the smoothing of the valence band edge between GaSb and AlGaSb.

Similar I-V measurements were performed on a wide range of devices varying the tunnel junction area. Figure 65c and Figure 65d show the plot of the peak current (Ip) and valley current (Iv) versus the tunnel junction area. Ip and Iv increase linearly with the junction area indicating a constant tunneling current density while the size is reduced from 4 μm^2 to 0.01 μm^2. Only a small deviation is observed due to process variations over the entire wafer. This indicates that the leakage originating from the sidewalls of the mesa is quite small.

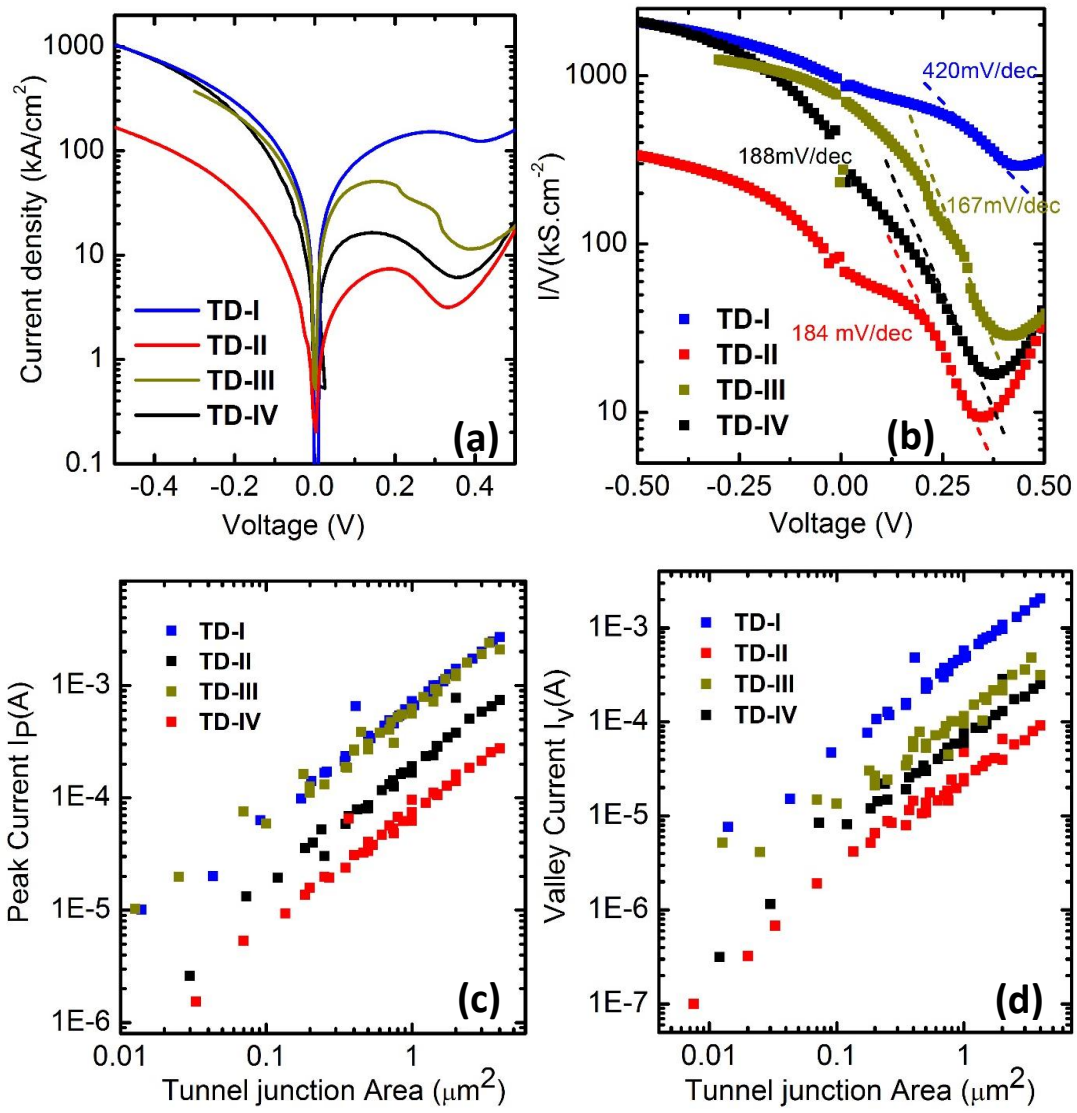


Figure 65: (a) I-V curves showing the difference in peak and valley currents, (b) absolute conductance-voltage curves, measured I_P (c) and I_V (d) versus the tunnel junction area of the epitaxial structures shown in Figure 60-63.

Table 4: Summary of the electrical results for the tunnel diodes fabricated in this study.

Epitaxial Structure	**J_P ($kA.cm^{-2}$)**	**V_P (V)**	**Vv (V)**	**PVCR**	**Max. cond. ($kS.cm^{-2}$)**	**Min. cond. ($kS.cm^{-2}$)**	**ON/ OFF ratio**	**Cond. slope (mV/dec)**
InAs/3nm-i-GaSb/GaSb (TD-I)	159	0.288	0.409	1.35	2192	270	8	420
InAs/3nm-i-$Al_{0.4}Ga_{0.6}Sb$/GaSb (TD-II)	7.6	0.186	0.341	3.07	330	9	37	184
InAs/$Al_{0.5}Ga_{0.5}Sb$ (TD-III)	52	0.17	0.39	4.74	1200	27	44	167
InAs/3nm-i-$Al_{0.6}Ga_{0.4}Sb$/ $Al_xGa_{1-x}Sb$ ($0.2<x<0.6$) (TD-IV)	16	0.15	0.36	2.6	2225	16	139	188

Table 4, summarizes the electrical characteristics of all the TDs used in this study. Table- 4 clearly shows that the transition from type-III to type-II band alignment offers an improvement in conductance steepness. Although the current density of TD-I is the highest, this design is not well suited for TFET applications due to the large minimum conductance and high slope. The TD-III design is more suitable to get minimum conductance slope while TD-IV design exhibits the best trade-off between maximum/minimum conductance and slope.

4.2.2 Comparison of Tunnel diodes with the literature

In this section we compare the conductance properties of the tunnel diodes on different material systems available in the literature. The results in Table 5 show several interesting points. As the band gap of the material changes from indirect band gap (Si) to direct (III-V), TDs show a continuous improvement in terms of maximum conductance. Thanks to the low E_{beff} height at the tunnel junction, the ON-conductance is enhanced significantly while moving from homojunction to heterojunction. From the results GaAs-I, II and InAs-I, II, it is evident that doping does have a large impact on the conductance. Even if a high doping is necessary to obtain a large conductance, the conductance slope drastically increases from 180 mV/dec to 570 mV/dec when the donor concentration in InAs is increased from $3x10^{18}$ to $1x10^{19}$ cm^{-3}. The same phenomenon can be observed in the case of low-doped $In_{0.9}Ga_{0.1}As/GaAs_{0.21}Sb_{0.79}$, in which a minimum conductance slope of 76 mV/dec can be achieved but with only a 4 kS/cm^2 maximum conductance. Therefore, to optimize the TFET performance, it seems more interesting to improve the maximum conductance by using a small effective barrier at the tunneling interface instead of using large band gap materials with degenerate doping. As demonstrated by Agarwal *et al*., this degenerate doping leads to band tails in the band gap that reduce the steepness of the conductance variation [93]. In our case (TD-IV), the trade-off between the on-conductance, the ON/OFF ratio and slope compares rather well with all these results and seems very promising for TFET applications.

Table 5: Summary of the electrical results for TDs using different material systems

Ref.	**Material system**	**N_D (cm^{-3})**	**N_A (cm^{-3})**	**Max. Conduc.**	**Min. conductance**	**ON/OFF ratio**	**Cond. slope (mV/dec)**
[94]	Si	$1x10^{20}$	$1x10^{20}$	20 S/cm^2	0.06 S/cm^2	333	140
[93]	Ge		-	-	-		90
[95]	GaAs-I	$3x10^{19}$	$1x10^{19}$	60 S/cm^2	0.01 S/cm^2	6000	130
[95]	GaAs-II	$3x10^{19}$	$5x10^{19}$	2 kS/cm^2	10 S/cm^2	200	165
[96]	$In_{0.53}Ga_{0.47}As$	$5x10^{19}$	$1x10^{20}$	0.02 mS/ μm	0.7 μS/μm	20	165
[95]	InAs-I	$3x10^{18}$	$1.8x10^{19}$	100 kS/cm^2	10 kS/cm^2	10	180
[95]	InAs-II	$1x10^{19}$	$1.8x10^{19}$	0.7 MS/cm^2	0.2 MS/cm^2	3.5	570
[95]	InAs/ GaSb	$1x10^{19}$ (Si)	$2x10^{19}$ (Be)	40 MS/cm^2	0.56 MS/cm^2	71	-
[97]	InAs/ GaSb	$1x10^{19}$ (Te)	$5x10^{18}$ (Be)	1.3MS/cm^2	220 kS/cm^2	5	268
[98]	InAs/ GaSb	$1x10^{17}$ (Si)	$1x10^{17}$ (Si)	300 kS/cm^2	30 kS/cm^2	10	160
[99]	$In_{0.9}Ga_{0.1}As$/ $GaAs_{0.21}Sb_{0.79}$	$1x10^{17}$ (Si)	$1x10^{17}$ (Si)	4 kS/cm^2	0.04 kS/cm^2	100	76
This study	**InAs/ $Al_{0.6}Ga_{0.6}Sb$ (TD-IV)**	**$1x10^{19}$ (Si)**	**$1x10^{19}$ (Si)**	**2.2 MS/cm^2**	**16 kS/cm^2**	**139**	**188**

4.2.3 Influence of the substrate (GaSb versus GaAs)

In the above-studied structures, the intrinsic zone is very thin (a few nm) which is not the case in a TFET. We have then studied a specific structure with a thicker intrinsic zone. Moreover, in this case we have compared the influence of the substrate, GaSb versus GaAs. To avoid plastic relaxation due to the lattice mismatch between GaSb and InAs, we introduce 9% Sb in InAs so that the InAsSb channel alloy is lattice matched to GaSb. In this way, we are only sensitive to defects coming from the buffer layer and avoid strain relaxation between the channel and source. The epitaxial structure shown in Figure 66 has been grown on both lattice matched GaSb and lattice mismatched GaAs substrates. A

metamorphic buffer has been used for the epitaxy grown on GaAs to accommodate the strain caused by the mismatch. The electrical characteristics shown in Figure 67 compare the I-V performance of TD-V, grown on GaSb (black) and GaAs (pink) substrates. A PVCR of 1.16 can be observed for the epitaxy grown on a GaAs substrate whereas a PVCR of 2.24 is achieved for the epitaxy on a GaSb substrate. This is primarily due to the excess leakage current that can be attributed to the threading dislocation density coming from the large mismatch accommodation between GaSb and the GaAs substrate. In addition, the less steep conductance slope for the device grown on GaAs (Figure 67b) confirms the impact of the metamorphic buffer.

Tunnel Diode: V (TD-V)

50nm	$InAsSb_{0.09}$	Si($N_D=10^{19}cm^{-3}$)
80nm	$InAsSb_{0.09}$ (**nid)**	
50nm	$Al_{0.4}Ga_{0.6}Sb$	Si($N_A=10^{19}cm^{-3}$)
600nm	GaSb	Si($N_A=1x10^{19}cm^{-3}$)
GaSb Substrate		($N_A=8x10^{18}cm^{-3}$)

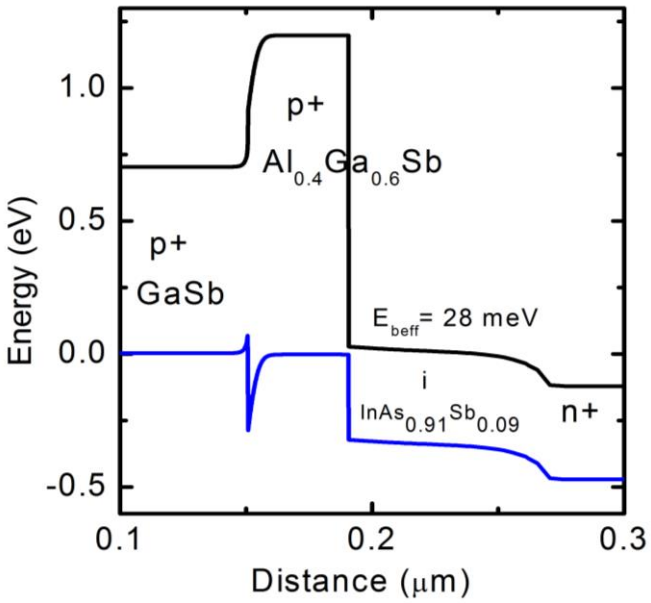


Figure 66: Epitaxial structure of TD-V and its band diagram generated using Silvaco TCAD tool.

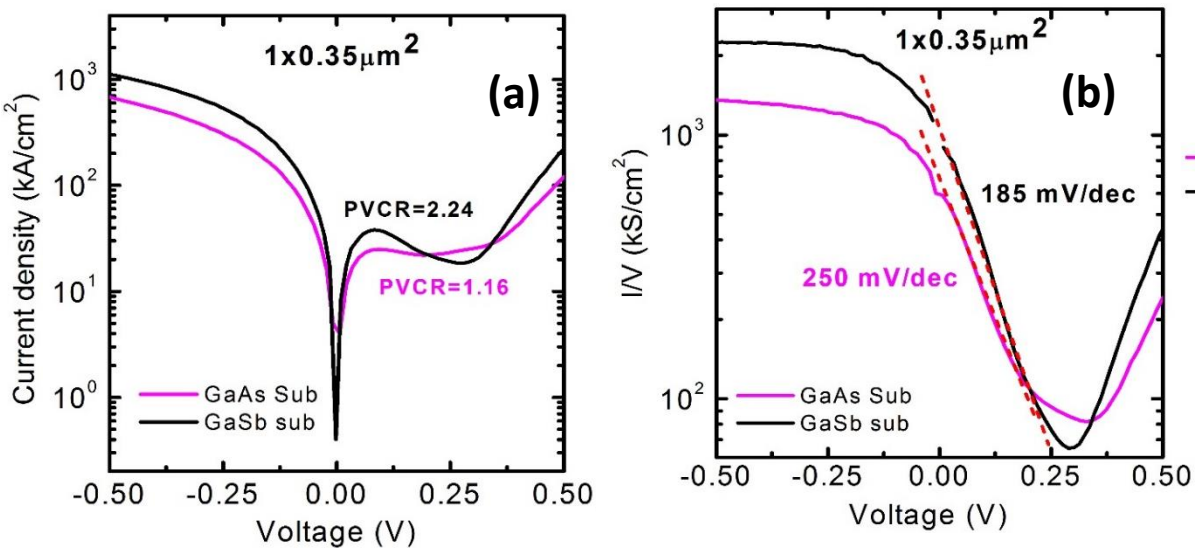


Figure 67: (a) I-V characteristics and (b) conductance slope of TD-V.

4.3 TFET Results

We have developed 3 different generations of TFETs. From generation to generation, the epitaxial structure and technology is changed to increase the overall performance. The improvements were made based on the understanding gained from the I-V characteristics. The layer structure and related I-V characteristics will be detailed for each generation. As we have optimized the technology for diodes and TFETs in parallel, the first transistor (TFET-I, shown in Figure 68) was fabricated using the TD-V layer grown on a GaSb substrate. From generation-I (TFET-I) to generation-II (TFET-II), we show that aggressively scaling the channel width at the interface enhances the gate electrostatic control over the channel. We show from the electrical characteristics of generation-III (TFET-III) that increasing the E_{beff} at the junction and increasing the InAs channel thickness has drastic effects on the performance. Using low temperature measurements, the origin of the different leakage mechanisms are discussed. Finally, the performance of a V-shaped transistor are compared with the results in the literature using staggered band aligned material systems to fabricate TFETs.

TFET-I :

50nm	$InAs_{0.91}Sb_{0.09}$	n++ (Si-1x$10^{19}$$cm^{-3}$)
80nm	$InAs_{0.91}Sb_{0.09}$	**nid**
50nm	$Al_{0.4}Ga_{0.6}Sb$	p++ (Si-1x10^{19} cm^{-3})
600nm	GaSb	p++ (Si-1x10^{19} cm^{-3})
Sub	GaSb(100)	p++ (8x10^{18} cm^{-3})

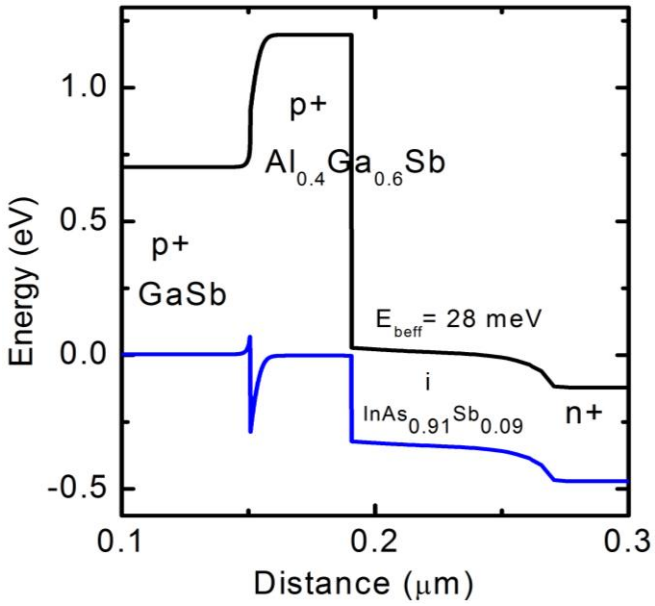


Figure 68: Epitaxial structure and band diagram of TFET-I.

The three TFET structures (Table-6) used in this study were grown and fabricated using the process flow detailed in chapter 3. For TFET-I and TFET-II, the band alignment at the source/channel interface is nearly at the limit from staggered to broken gap with a very low effective barrier (E_{beff}) of 28 meV. The TFET-III structure has an E_{beff} height of 70 meV. All p+ and n+ layers are doped with 'Si' with a doping concentration of 1x10^{19} cm^{-3}.

4.3.1 Electrical results of TFET-I ($InAs_{0.91}Sb_{0.09}/Al_{0.4}Ga_{0.6}Sb$)

Figure 69b displays the output characteristics of the device (size: 0.35x4 μm^2) presented in Figure 69a. As can be seen in backward regime, the NDR evidences a tunnel injection mechanism. The small E_{beff} height at the interface leads to a drain current (I_D) larger than 1200 μA/μm at V_{DS}=0.5V. The small E_{beff} height at the tunnel junction results in a high conductance in both ON and OFF state regimes. Another reason could be that the width of the channel (350 nm) at the junction is so large that the gate cannot control the charge in the center of the channel. Thus, the high conductance together with the poor gate coupling over the channel charge result in a weak variation of I_D. As has been mentioned in chapter 3, PECVD deposited SiO_2 at 300^0 C for 30 min might have degraded the gate stack

quality. Furthermore, the FIB-STEM image in Figure 69a suggests that the gate does not overlap the entire channel which leads to an increased resistance, reducing I_D.

Table 6: Epitaxial structures used in this study to fabricate TFET

Layer name (Sub)	**Buffer (thickness)**	**Heterojunction $n^{++}/i/p^{++}$ (thickness in nm)**	**Doping $n^{++}/i/p^{++}$ (cm^{-3})**	**Expected (E_{beff})**
TFET-I (GaSb)	GaSb (1000nm)	InAsSb/InAsSb/$Al_{0.4}Ga_{0.6}Sb$ (50nm)/(80nm)/(50nm)	$1x10^{19}/1x10^{16}/1x10^{19}$	28 meV
TFET-II (GaAs)	GaSb (600nm)	InAs/InAs/$Al_{0.4}Ga_{0.6}Sb$ (50nm)/(80nm)/(50nm)	$1x10^{19}/1x10^{16}/1x10^{19}$	28 meV
TFET-III (GaAs)	InAs (600nm)	InAs/InAs/$Al_{0.5}Ga_{0.5}Sb$ (50nm)/(200nm)/(50nm)	$1x10^{19}/1x10^{16}/1x10^{19}$	70 meV

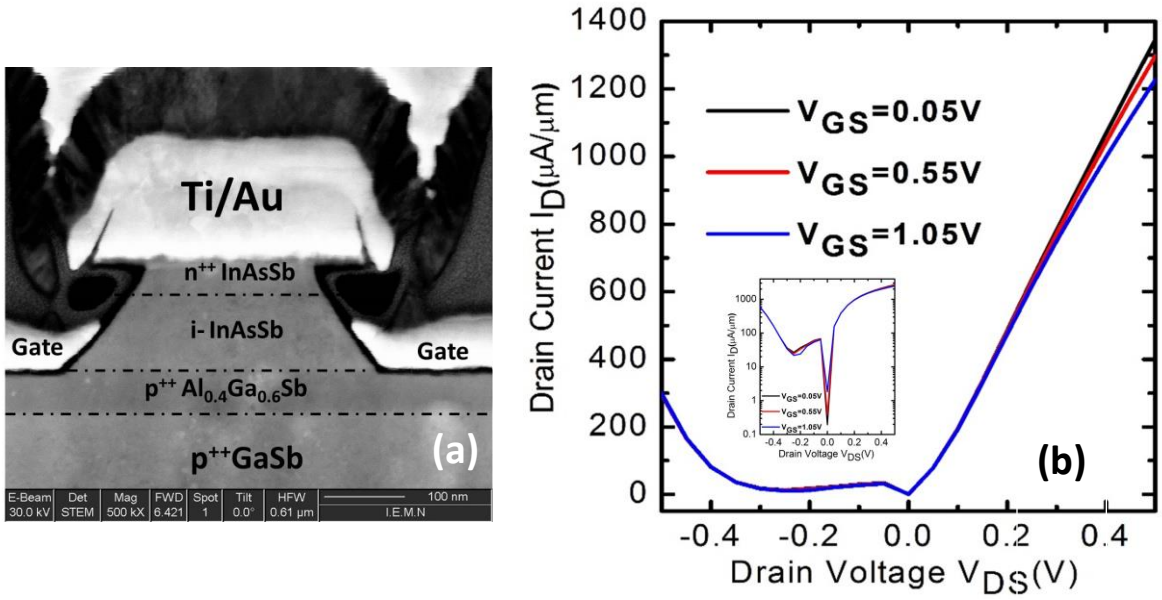


Figure 69: (a) Cross-sectional FIB-STEM image of Λ-shaped device fabricated on TFET-I epitaxial layer and (b) I_{DS}-V_{DS} characteristics of device in (a) at different gate voltages (V_{GS})(Inset: logscale).

4.3.2 Electrical results of TFET-II ($InAs/Al_{0.4}Ga_{0.6}Sb$)

From the observations extracted from the electrical characteristics of TFET-I, $InAs_{0.91}Sb_{0.09}$ has been replaced by InAs for TFET-II (Figure 70) and the structure has been grown on a S.I. GaAs substrate since the insulation of devices made on a conductive GaSb substrate is quite impossible. When using a PECVD SiO_2 layer deposited at 300°C to insulate the contacts from the conductive substrate, the gate metal diffusion eventually degraded the overall gate stack quality as was the case for TFET-I. However, when using S.I. GaAs substrate, the lattice mismatch between GaSb and GaAs (7.8%) leads to the generation of threading dislocations. A 600nm-GaSb metamorphic buffer has been grown on the GaAs substrate before growing the TFET active layers. This epitaxial growth on lattice mismatched substrate has been already optimized by El Kazzi *et al*. at IEMN [100]. The conductive GaSb buffer layer is insulated by dry etching followed by wet etching and large metal pads deposited on the GaAs substrate are connected to the device contacts through air bridges as described in chapter 3.

In addition to that, we used InAs as a channel material to improve the channel/Al_2O_3 interface that reduces the intrinsic doping in the channel. Doping is maintained at the same level with a concentration of $1x10^{19}$ cm^{-3} for both p+ and n+ layers.

TFET-II:

50nm	InAs	n++ (Si-$1x10^{19}$ cm^{-3})
80nm	InAs	**nid**
50nm	$Al_{0.4}Ga_{0.6}Sb$	p++ (Si-$1x10^{19}$ cm^{-3})
600nm	GaSb buffer	p++ (Si-$1x10^{19}$ cm^{-3})
SI-GaAs Substrate (100)		

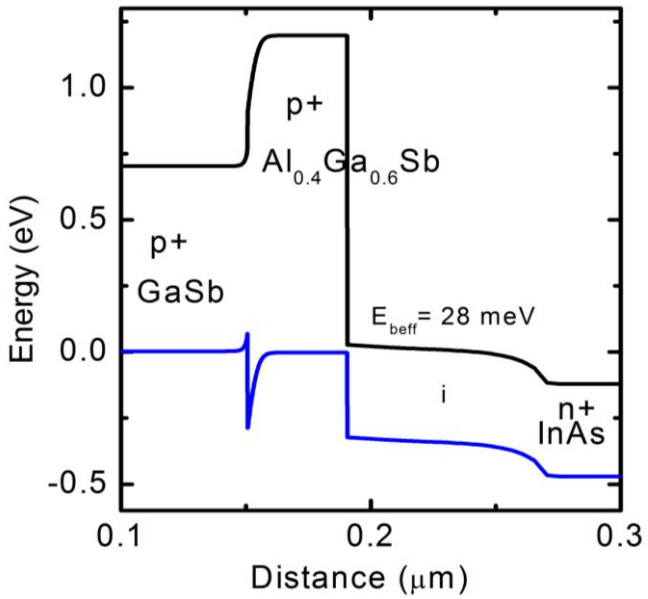


Figure 70: Epitaxial structure and band diagram of TFET-II.

Figure 71 shows the electrical I_{DS}-V_{DS} characteristics of TFET-II for Λ-shaped and V-shaped devices. The insets in Figure 71a and b show the FIB-STEM images of the Λ-shaped and V-shaped devices taken from the same wafer and resulting from the different orientations of the device with respect to the crystallographic azimuths. From the FIB-STEM images, the channel width of the Λ-shaped and V-shaped devices is calculated to be 250 nm and 50 nm respectively. First, the observed NDR at negative V_{DS} is larger than for TFET-I. At V_{DS}=V_{GS}=0.5V, the Λ-shaped and V-shaped devices exhibit a drain current (I_D or I_{ON}) of about 320 μA/μm and 100 μA/μm and an I_{OFF} of about 294 μA/μm and 75 μA/μm respectively. The large I_{ON} for the Λ-shaped device is due to the large tunneling area at the interface. The gate control (Figure 71) is somewhat better for the V-shaped device, probably due to the reduced channel width at the junction.

Note that here no post deposition annealing (PDA) after oxide deposition or post process annealing (PPA) after technology has been performed so far in this process. It has been shown in the literature that forming gas (5% H_2/ 95% N_2) annealing significantly lowers the D_{it} and improves the C-V dispersion curve [101]. Also, PPA annealing can improve the ohmic contact formation, especially for GaSb because it is well known that 'Sb' based compounds are readily oxidized in the environment [102]. This PPA will eventually increase the drain current (I_D).

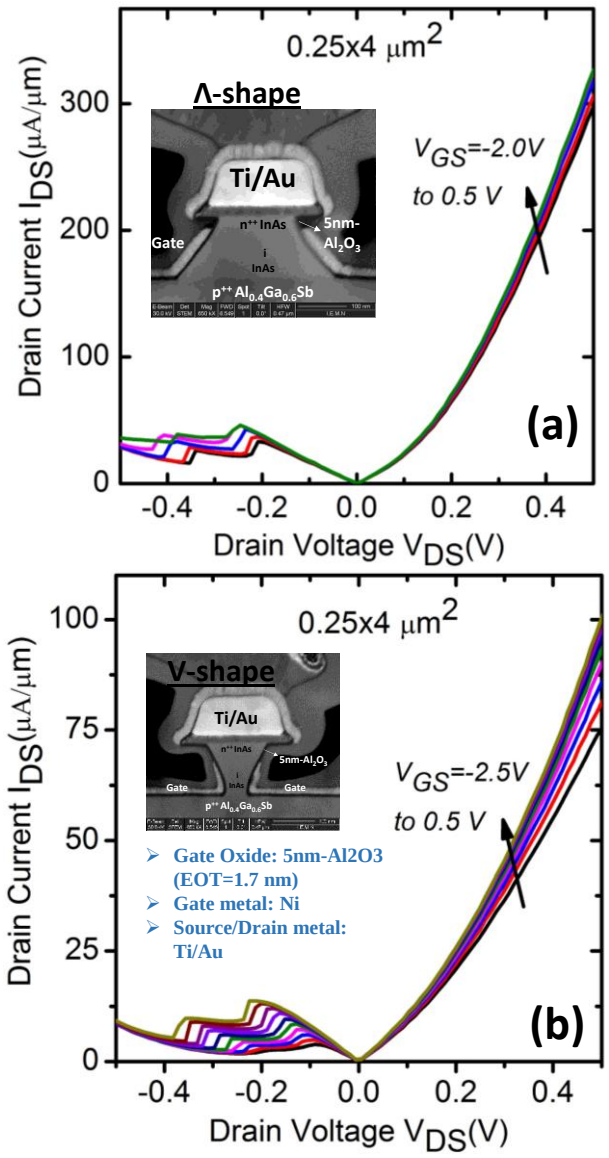


Figure 71: I_{DS}-V_{DS} characteristics of a (a) Λ-shaped device and (b) V-shaped device of area 0.25x4 μm² at different gate voltages (V_{GS}). Inset: FIB-Cross sectional image.

In order to test the impact of an annealing, we have performed PPA at 200 °C in the forming gas for 10 minutes. Figure 72 shows the electrical characteristics of the Λ-shaped and V-shaped devices respectively, for a drain contact area of 0.25x2 μm². A drastic improvement in terms of ON-state and OFF-state currents is visible. For the Λ-shaped device I_{ON} increases from 320 μA/μm to 1180 μA/μm and for the V-shaped device I_{ON} increases from 100 μA/μm to 285 μA/μm. Similarly, for the Λ-shaped device I_{OFF} increases

from 294 μA/μm (V_{GS}=-2.0V) to 585 μA/μm (V_{GS}=-1.5V) and for the V-shaped device I_{OFF} increases from 75 μA/μm (V_{GS}=-2.5V) to 24 μA/μm (V_{GS}=-1.5V). The I_{ON}/I_{OFF} ratio for the Λ-shaped device raises from 1.1 to 2 whereas for the V-shaped one, it raises from 1.3 to 12. The larger I_{ON} value is attributed to a better contact resistance whereas the enhancement of the I_{ON}/I_{OFF} ratio is related to the improvement of the Al_2O_3-InAs interface quality [101]. The I_{ON}/I_{OFF} ratio for Λ-shaped and V-shaped devices after annealing is 2 and 12 respectively. The better I_{ON}/I_{OFF} ratio for the V-shaped device is due to the improved gate efficiency, as the channel width is smaller in this geometry.

Although an I_{ON} current of 285 μA/μm is better than those found in the literature so far on this material system, the I_{ON}/I_{OFF} ratio remains still very poor [103]–[105]. The high I_{OFF} can be due to the small E_{beff} height at the junction and poor gate efficiency contributing to a large OFF-state current. The poor gate control on the channel may contribute to the short channel effect (SCE) called drain induced barrier thinning (DIBT). The other reason could be the problem of mismatch when replacing InAsSb (in TFET-I) by InAs (in TFET-II). The critical thickness of InAs (about 100 nm) is slightly overpassed in TFET-II so InAs is partially relaxed which may cause the formation of defects at the tunneling interface. Furthermore, the pinch-off is difficult to obtain even for the V-shaped device. One way to further boost the performance is to increase the E_{beff} height, which is possible by increasing the 'Al' composition. The other way as described in section 2.3.4, is to increase the channel length to reduce the DIBT.

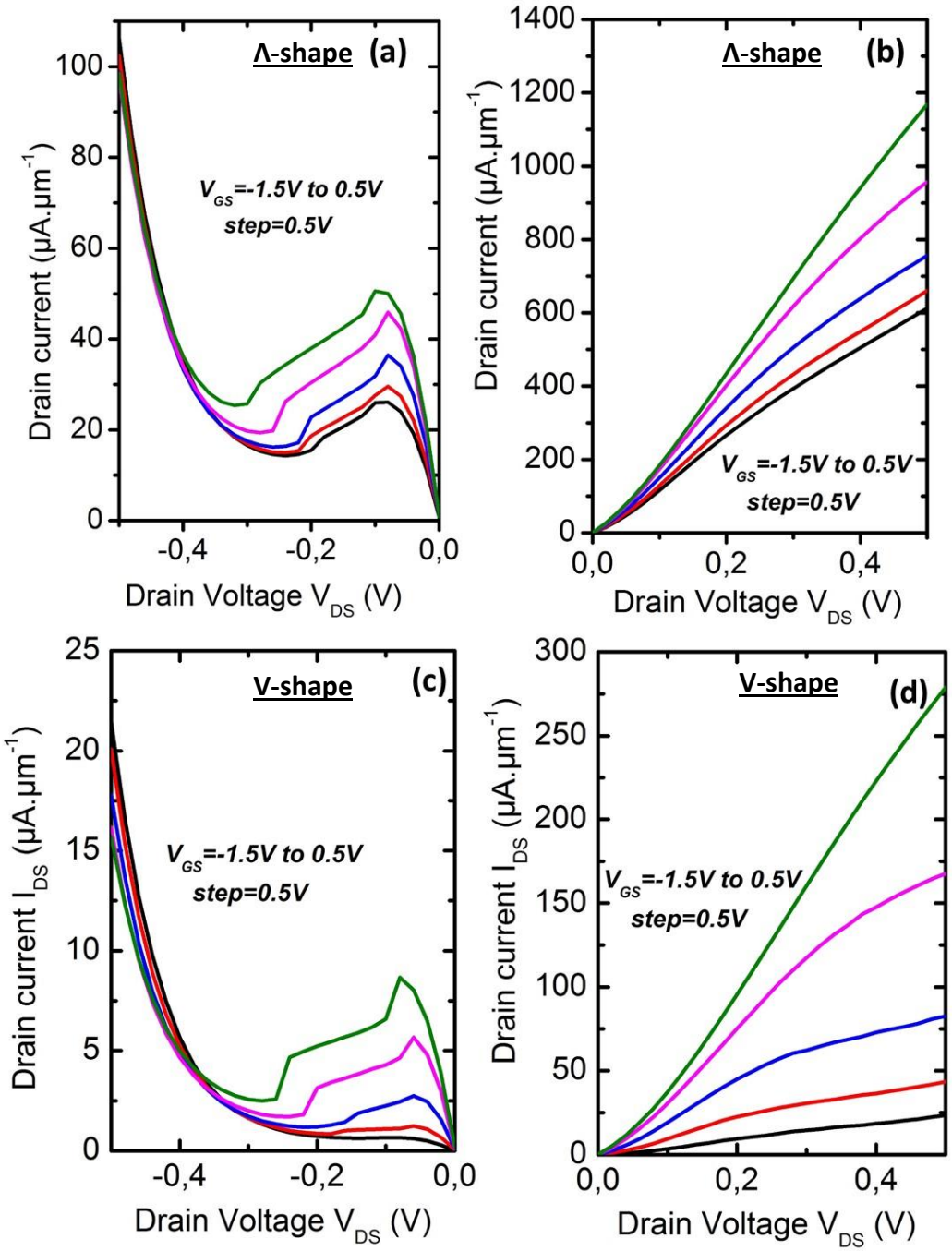


Figure 72: (a), (b) I_{DS}-V_{DS} characteristics of the Λ-shaped device of area 0.25x2 μm^2 and (c), (d) I_{DS}-V_{DS} characteristics of the V-shaped device of area 0.25x2 μm^2.

Table 7: Summary of the electrical results for the tunnel FETs

Layer name (Sub)	**Λ-shape** **I_{ON}** µA/µm (V_{GS}= V_{DS}=V)**;** **I_{OFF}** µA/µm (V_{GS}=V_{DS}=V)**;**	**V-shape** **I_{ON}** µA/µm (V_{GS}= V_{DS}=0.5V)**;** **I_{OFF}** µA/µm (V_{DS}=0.5V)**;**
TFET-I (GaSb)	I_{ON}=1200 µA/µm **(V_{GS}= V_{DS}=0.5V)**	-
TFET-II (GaAs)	I_{ON}=320 µA/µm **(V_{GS}= V_{DS}=0.5V);** I_{OFF}=294 µA/µm **(V_{GS}= -2.0V; V_{DS}=0.5V)**	I_{ON}=100 µA/µm **(V_{GS}= V_{DS}=0.5V);** I_{OFF}=75 µA/µm **(V_{GS}= -2.5V; V_{DS}=0.5V)**
TFET-II (GaAs) ***After annealing***	I_{ON}=1180 µA/µm **(V_{GS}= V_{DS}=0.5V);** I_{OFF}=585 µA/µm **(V_{GS}= -1.5V; V_{DS}=0.5V)**	I_{ON}=285 µA/µm **(V_{GS}= V_{DS}=0.5V);** I_{OFF}=24 µA/µm **(V_{GS}= -1.5V; V_{DS}=0.5V)**

Figure 73 shows the drain current variations with the width of the mesa at the tunneling interface. I_{OFF} (<25 µA/µm) is substantially reduced for a drain contact width of 0.25 µm combined with a V-shape resulting in a width of 50 nm at the tunneling interface. In this configuration, I_{ON}/I_{OFF} is improved and reaches more than one decade. This indicates that further scaling down of the mesa width is necessary to improve the electrostatic control on the tunneling current. Table 7 summarizes the best results obtained in TFET-I and TFET-II (before and after annealing).

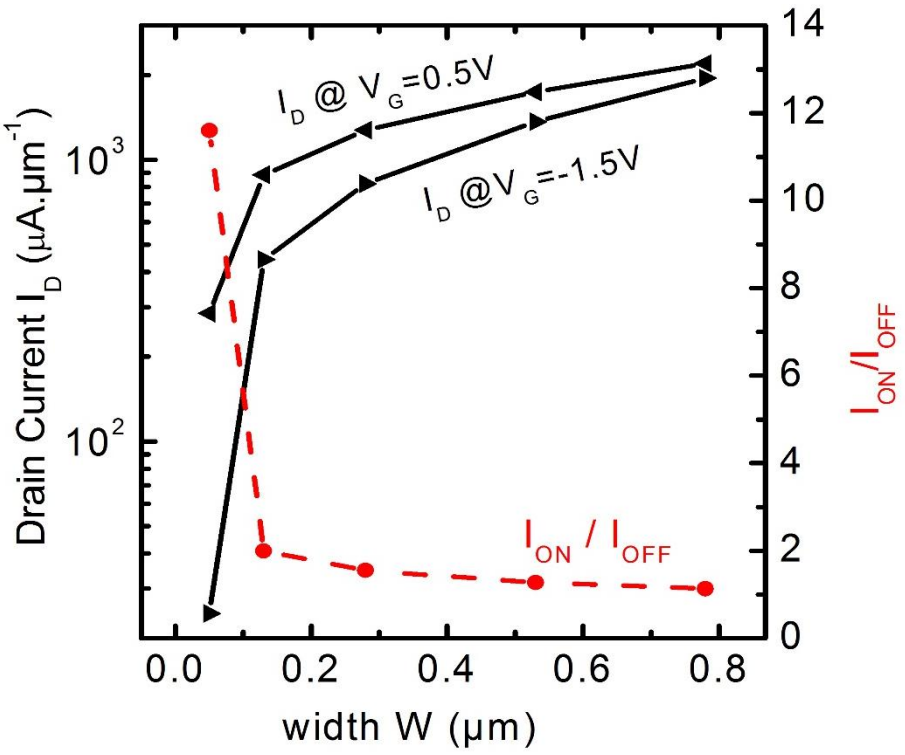


Figure 73: Drain current (I_D) variation with the width of the tunnel junction (black curves, left axis) and resulting ratio between the On state and OFF state currents (red curve, right axis).

4.3.3 Electrical characterization of TFET-III ($InAs/Al_{0.5}Ga_{0.5}Sb$)

Results obtained from TFET-II (table 7) suggest that increasing the effective barrier (E_{beff}) at the tunneling interface by increasing the 'Al' composition reduces the OFF-state current. However, increasing the 'Al' composition also limits the ON-state current because of a larger E_{beff} height and a higher spike in the valence band between GaSb and AlGaSb. From the knowledge gained from the TD-IV results, compositional grading in the source improves the ON-conductance of the device as the valence band edge is smoothened. The epitaxial structure with valence band edge smoothing is shown in Figure 74.

TFET-III:

50nm	InAs	n+ (Si-1x10^{19} cm^{-3})
200nm	InAs	**nid**
50nm	$Al_{0.5}Ga_{0.5}Sb$	p+(Si-1x10^{19} cm^{-3}) (linearly graded 0.2 (bottom)→0.5 (top))
20nm	GaSb	p+ (Si-1x10^{19} cm^{-3})
1µm	InAs	n+ (Si-1x10^{19} cm^{-3})
30 nm GaSb		
S.I.GaAs(100) substrate		

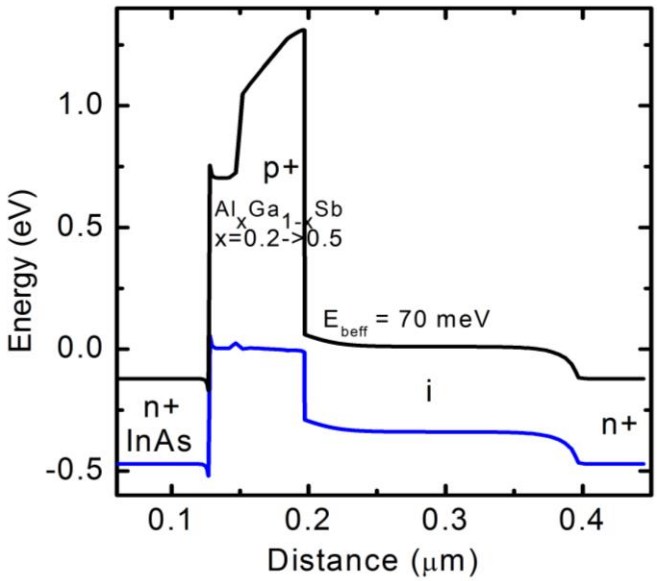


Figure 74: Epitaxial structure and band diagram of TFET-III.

By increasing the 'Al' composition to 50%, E_{beff} at the tunnel junction reaches 70 meV. Furthermore, the InAs channel thickness (nid) has been increased from 80 nm for TFET-II to 200 nm for TFET-III to reduce the short channel effects (SCEs). As this layer is now much thicker than the critical value for plastic deformation of InAs on GaSb, the metamorphic buffer matched to the lattice constant of GaSb (in TFET-II) has been replaced with a buffer lattice matched to InAs and composed of a thin 30 nm not fully relaxed GaSb layer and a 1 µm thick InAs layer in the TFET-III structure. This is now the GaSb/AlGaSb source layer which is compressively strained but with a layer thickness below the critical one for plastic relaxation (<100nm). For the technological process, Pd/Ti/Au was evaporated to form the source ohmic contact on the InAs buffer layer after opening the oxide and AlGaSb/GaSb source layers using dry plasma etching. The high conductance of the InAs:n+/GaSb:p+ broken gap interface (Figure 73) ensures the contact to the GaSb source layer of the transistor [106].

Figure 75 shows the variations of I_{ON} and I_{OFF} when varying the tunnel junction width. Pinching of the device can be achieved when reducing the tunnel junction width. The I_{ON}/I_{OFF} ratio is significantly improved for small widths, reaching 9.84x10^2 for the narrowest mesa width (80nm). This is a significant improvement from what has been observed previously in the case of TFET-II for which the I_{ON}/I_{OFF} ratio is only 12. This

result shows that the scaling of the channel width together with a high aspect ratio is highly beneficial for improving TFET performance.

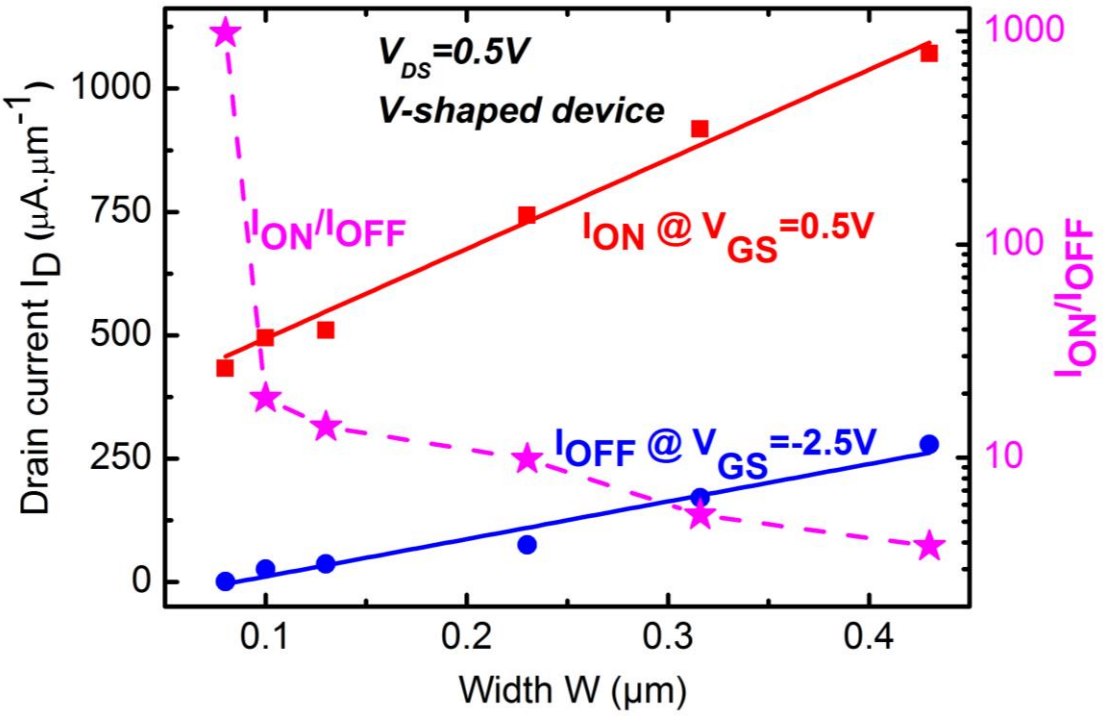


Figure 75: Plot showing the variation of I_{ON} and I_{OFF} w.r.t the width (W) of the tunnel junction for the V-shaped device at V_{DS}=0.5V.

The room temperature characteristics of the narrowest device (W=80nm) are shown in Figure 76. The Esaki diode behavior evidenced by the negative differential resistance (causing some ringing) in backward regime (Figure 76a) confirms a band-to-band tunneling injection mechanism. In forward regime (Figure 76b), the device exhibits a maximum ON-current of 433 µA.µm^{-1} at V_{DS}=V_{GS}=0.5V. The transfer and the transconductance characteristics in Figure 76c and Figure 76d respectively show an I_{ON}(V_{GS}=0.5V)/I_{OFF}(V_{GS}=-2.5V) ratio larger than 9.8x10^2 and a maximum transconductance of about 500 µS/µm for V_{DS}=0.5V. However, a subthreshold slope larger than 500 mV/decade is obtained even for a reduced drain voltage of 0.1V. This result may be due to a high defect density at the InAs/Al_2O_3 interface. As shown by Mookerjea *et al*, a field-enhanced thermal excitation of carriers from these trap states can strongly degrade the slope of the transfer characteristics in the subthreshold regime at room temperature [42].

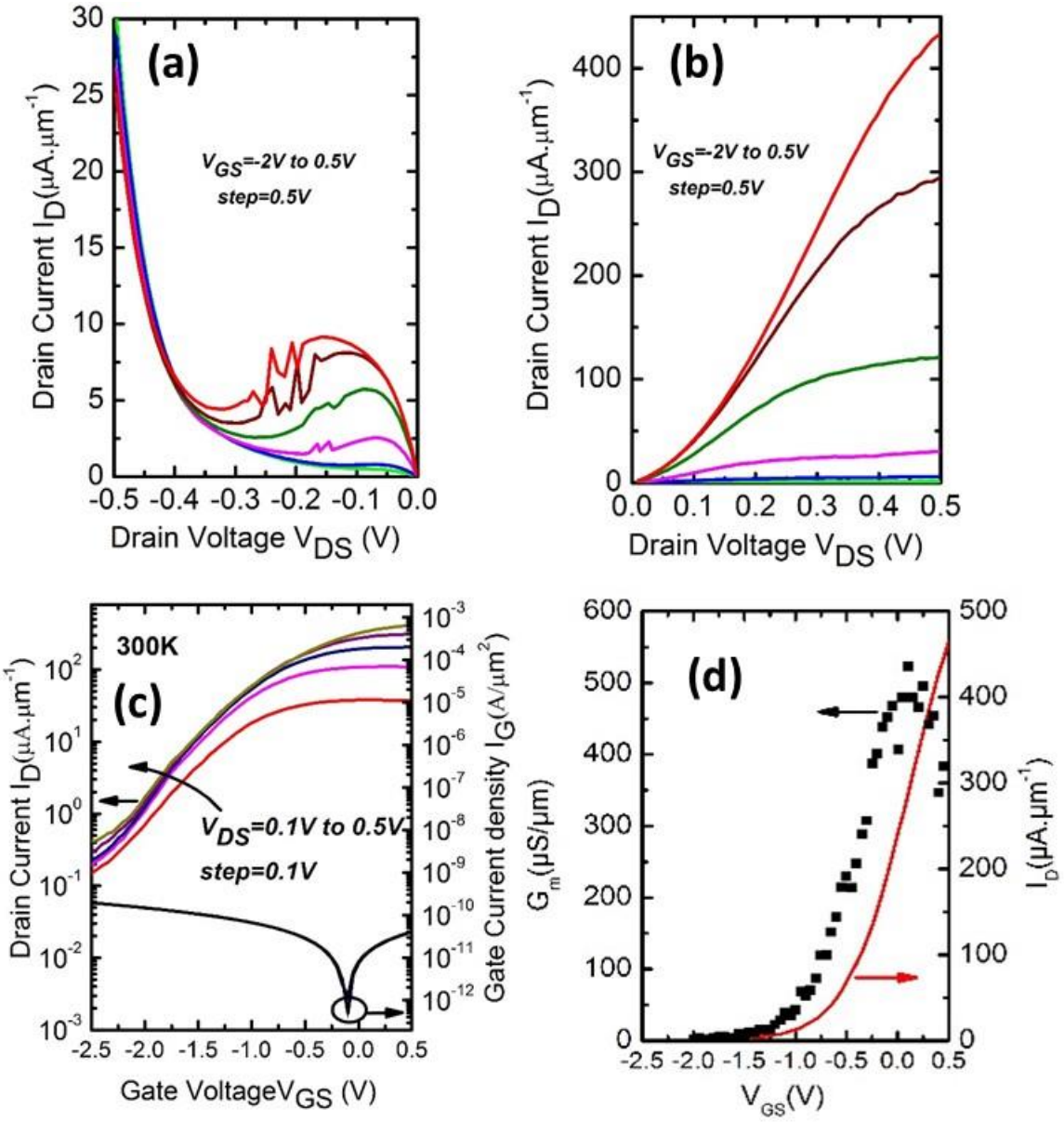


Figure 76: 300K I_{DS}-V_{DS} characteristics of the InAs/AlGaSb V-shape TFET in backward (a) and forward regime (b). (c) Transfer characteristics of the device for different V_{DS} and corresponding gate current density, (d) Transconductance curve for V_{DS}=0.5V (black squares) and transfer characteristics for V_{DS}=0.5V in linear scale (red line).

The TFET performance is also dependent on the density of defects in the gate oxide. In most cases the large storage time of charges by these defects results in an hysteresis effect in the I_D-V_{GS} characteristics [107]. That is indeed what we observe when the gate

voltage (V_{GS}) bias has been swept in two directions with a few minutes between the up and down sweeps (Figure 77). The charge built up by the traps in the oxide results in a shift of 1 V in the threshold voltage (ΔV_T). From this value, the effective fixed oxide charge density in the oxide can be estimated to about $1.1x10^{13}$ $eV^{-1}.cm^{-2}$ [108]. The effective fixed oxide charge density comprises the fixed charges in the oxide and the fixed interface traps between alumina and InAs. Usually, high frequency capacitance measurements are performed to get insight in the origin of the different charge and traps. However, due to the large gate/source overlap (inset Figure 77) in our design, the parasitic capacitance prevents us to perform such measurements.

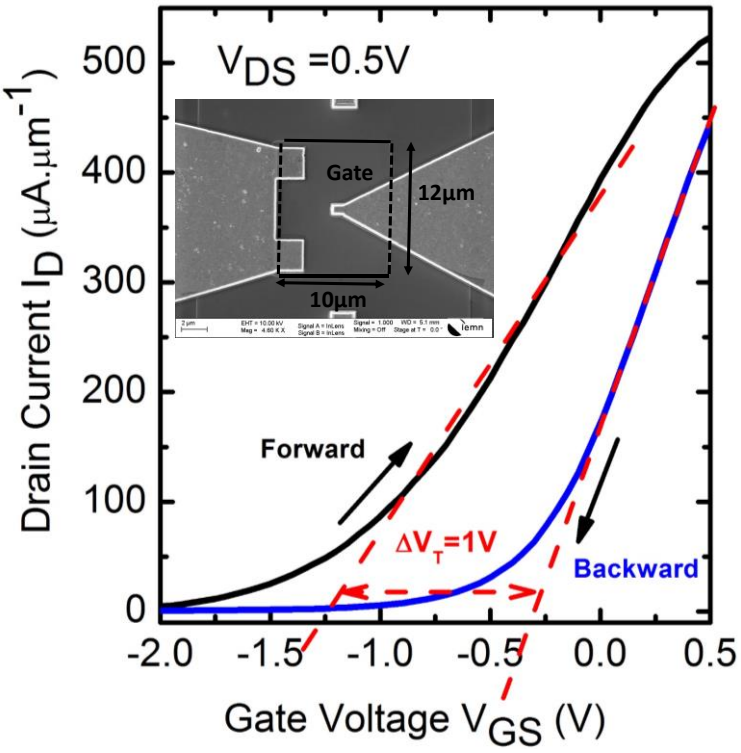


Figure 77: (a) Hysteresis observed in the transfer characteristics for the V-shaped device when the gate voltage is swept in two directions at V_{DS}=0.5V. Inset: Top view SEM image showing the gate/source overlap.

4.3.4 Low temperature measurements for TFET-III

To further understand the influence of traps, we measured the transfer characteristics of the device varying the temperature from 300K to 77K. As can be seen on

Figure 78a showing the results for V_{DS}=0.1V, the subthreshold regime is strongly dependent on the temperature. Whereas the minimum switching slope is larger than 500 mV/decade at room temperature, it is improved to 71 mV/decade at 77K (Figure 78b).

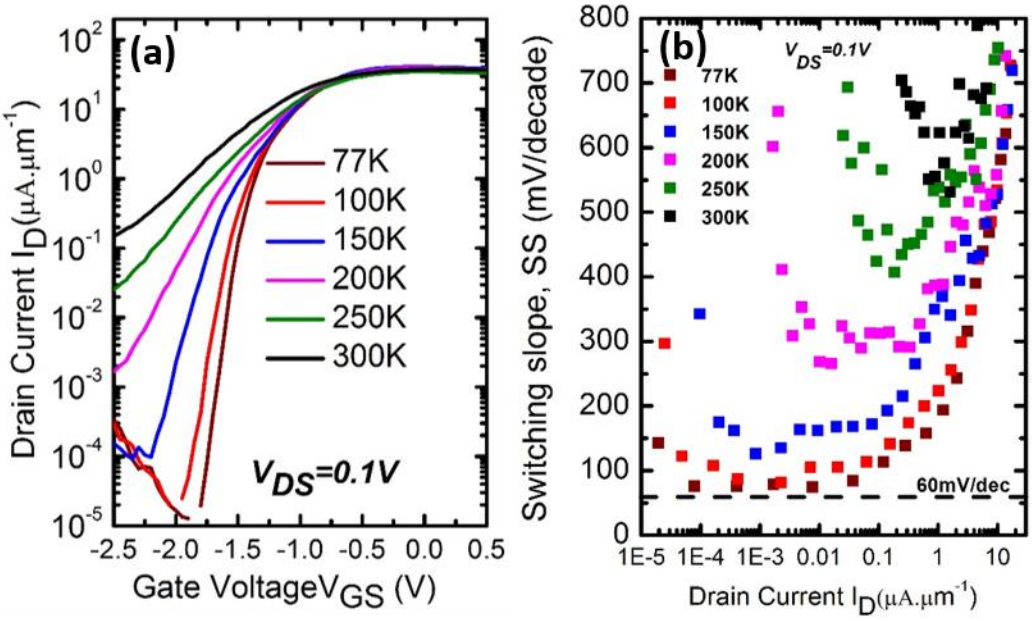


Figure 78: Low temperature characterization of the device: (a) transfer characteristics versus temperature for V_{DS}=0.1V and (b) Subthreshold slope versus drain current extracted from (a).

The Arrhenius plots of Figure 79 evidence the different conduction mechanisms involved for four different V_{GS} corresponding to three different operation modes. For V_{GS}=-2.2 (Figure 79a), whereas the leakage floor is dominated by tunneling at low temperature, a Shockley-Read-Hall (SRH) generation-recombination current prevails when the temperature exceeds 150K. The activation energy that can be deduced from the slope between 300K and 150K is roughly equal to half of the bandgap of InAs (0.17 eV). This means that the thermal activation of traps (probably located at the Al_2O_3/InAs interface) provides a large density of carriers in the InAs channel. The impact of these traps is also confirmed when the variation of the subthreshold current at V_{GS}=-1.8V with the temperature is investigated (Figure 79b). For V_{DS}=0.1V, the linear variation of ln(I_D) vs 1/k_BT evidences a trap-assisted tunneling phenomenon (Poole-Frenkel (PF) mechanism). At larger V_{DS} (0.5V), we observe the same limitation above 200K, but a constant leakage

below 150K expresses a band to band tunneling (BTBT) mechanism. Eventualy, for V_{GS}=-0.5V (Figure 79c) and V_{GS}=0V (Figure 79d), the drain current is independent of the temperature showing a gated BTBT operation.

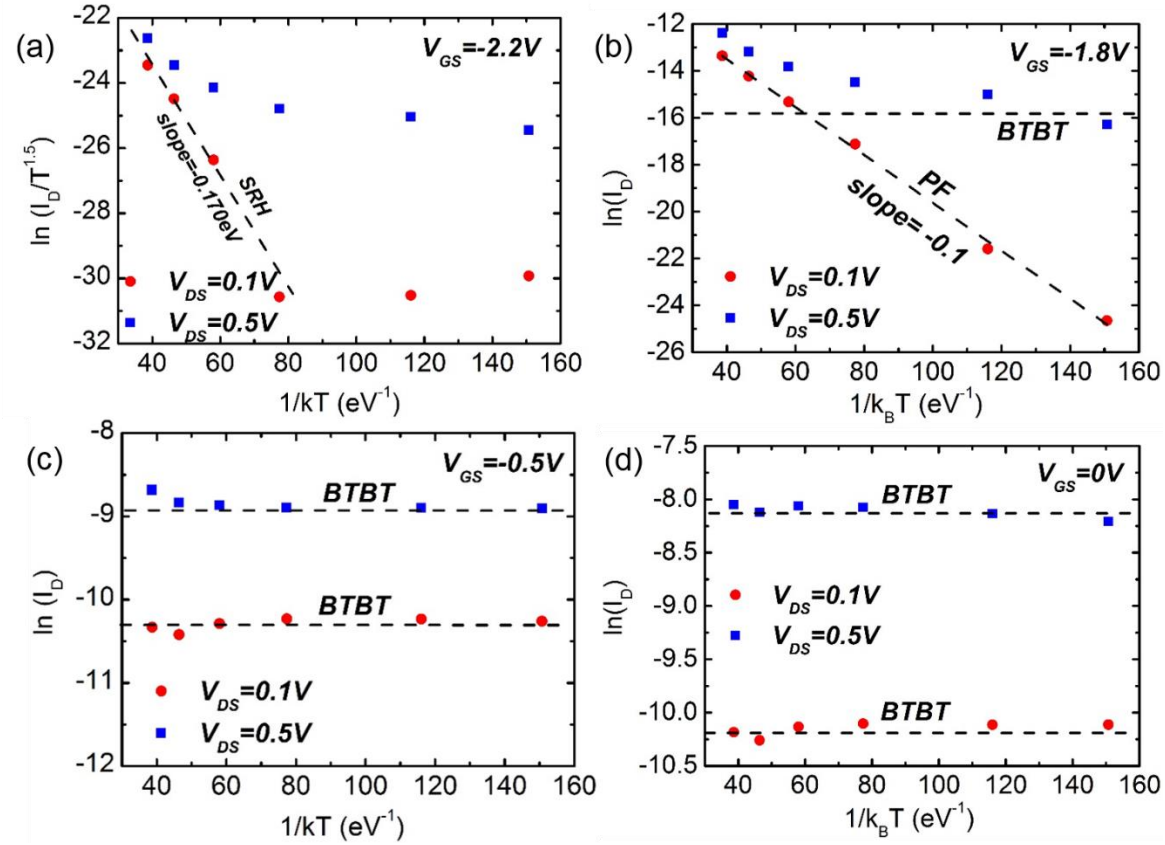


Figure 79 : Arrhenius plot of drain current for V_{GS}=-2.2V showing that the OFF current is dominated at room temperature by a SRH generation-recombination mechanism in InAs (a). For V_{GS}=-1.8V, a Poole-Frenkel (PF) mechanism can be deduced for low V_{DS} (red points) whereas a BTBT phenomenon prevails for large V_{DS} and T<150K (b). For V_{GS}=0.5V (c) and V_{GS}=0V (d), temperature independent drain current evidences a BTBT current domination.

The 77K I_{DS}-V_{DS} characteristics in Figure 80 (backward voltage) reveals a slight improvement of the peak to valley current ratio from 2.23 (RT) to 3.75 (77K) for V_{GS}=0V. This is mainly due to a lower excess current at low temperature as thermally assisted leakage current is reduced. However, in the forward regime, the improvement in the I_{ON}/I_{OFF} ratio is very dependent on the drain voltage whereas the low leakage floor (I_{OFF}<50 pA.µm^{-1}) and a still high ON-current (I_{ON}=40 µA.µm^{-1}) lead to an ON/OFF current ratio

larger than six decades at V_{DS}=0.1V. A little more than three decades are obtained for V_{DS}=0.5V. Considering the 77K transfer characteristic evolution with the drain voltage (Figure 80b), one can observe that the leakage floor for V_{GS} < -2V exhibits a gate voltage dependency characteristic of an ambipolar effect coming from the tunneling at the drain to channel interface. This current corresponds to the temperature independent leakage floor observed on Figure 79a for a temperature below 150K. On the other hand, at V_{GS}=-1.8V (Figure 80b) and for V_{DS}=0.5V, the subthreshold slope is still limited by band to band tunneling at the AlGaSb/InAs interface due to drain induced barrier thinning (DIBT). The 77K DIBT estimated considering the variation of the gate voltage needed to keep a constant drain current at 10^{-7} A/µm while varying the drain voltage from 0.1V to 0.5V is about 1 V/V. At V_{GS}=-2V, the overlap existing between these two phenomena (DIBT and ambipolar tunneling current at the drain to channel interface) indicates that a non-uniform band profile near the AlGaSb/InAs interface probably exists within the width of the channel.

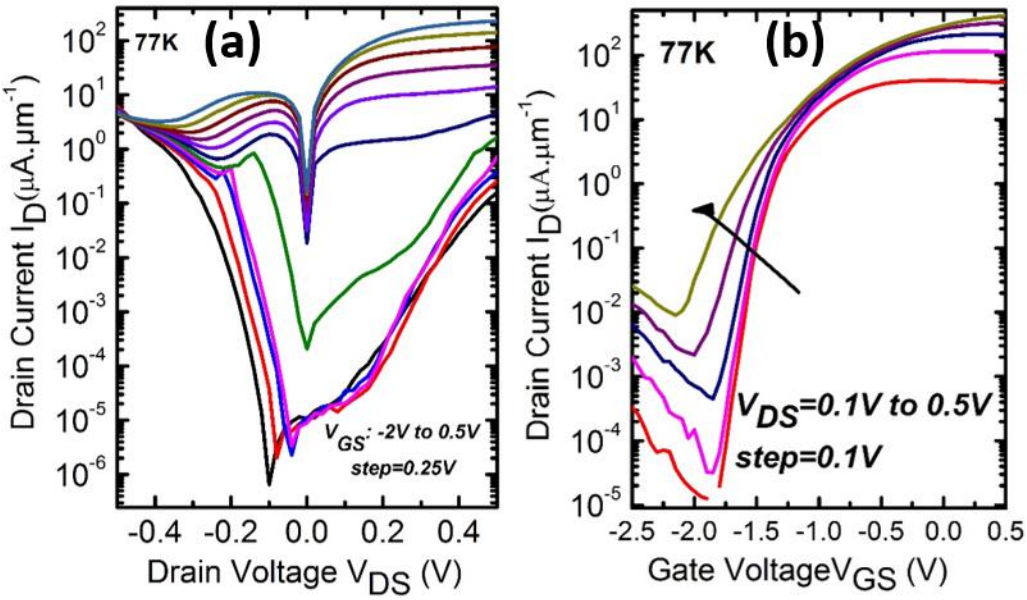


Figure 80: 77K characterization of the device: (a) I_{DS}-V_{DS}, (b) transfer characteristics for V_{DS}=0.1V to 0.5V.

4.4 Benchmarking

A benchmark of our V-shaped n-TFET with other n-TFETs based on near broken heterostructure is proposed in Table 7 and shows a good trade-off between the ON/OFF ratio, maximum ON-current and switching efficiency at low bias. Furthermore, the proposed configuration consisting in a vertical device with side gates makes this solution compatible with a large-scale integration on a CMOS platform. Vertical nanowire with gate all around (GAA) based on InAs/GaSb (broken gap) is attractive in terms of SS_{min}. However growing nanowires on a Si (001) or GaAs (001) substrate is still very challenging.

Table 7: Benchmarking of the V-shaped n-TFET with other broken and near broken heterostructure TFETs available in the literature.

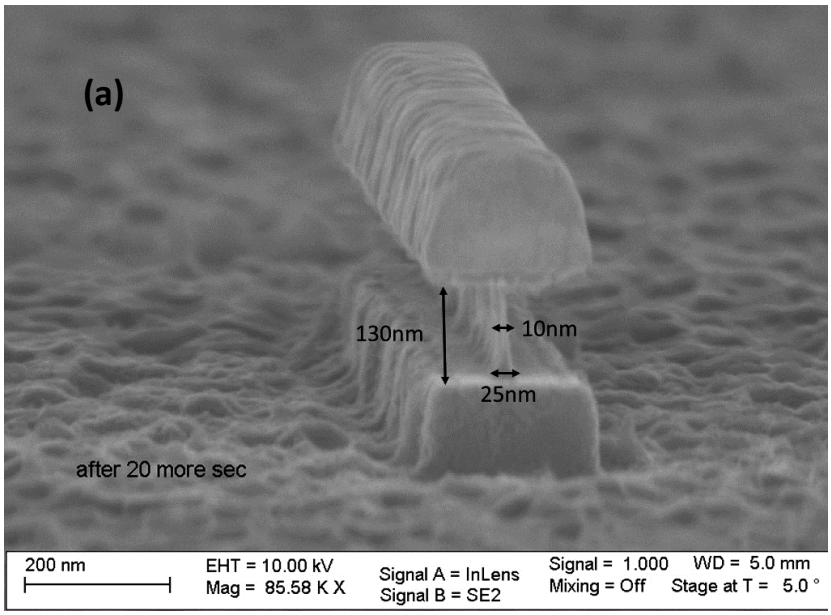
Ref.	**Device type**	**Subs.**	**Materials**	**Body thick. (nm)**	**L_G (nm)**	**EOT (nm)**	**I_{ON} @V_{DS}= 0.5V (µA/µm)**	**I_{ON}/I_{OFF} for V_{DS}=0.5V ($V_{GS(ON)}$ - $V_{GS(OFF)}$)**	**SS_{min} (mV/dec) 300K V_{DS} = 0.5 V**	**SS_{min} (mV/dec) 77K V_{DS}= 0.1V**
[109]	T-shape	GaSb (001)	InAs/GaSb (broken gap)	6	40000	1.3	180	6,000 (1.5V)	200	50
[110]	NW with Ω-gate	GaAs (111)	InAs(Sb)/ GaSb (broken gap)	45	290	1.3	62	143 @ V_{DS}=0.3V (3V)	320	17 @4.2K
[105]	Vertical NW with GAA	Si (111)	InAs/GaSb (broken gap)	20	100	1.4	35	5,000 (1V)	82	NA
[111]	Λ-shape	InP (001)	$In_{0.9}Ga_{0.1}As$/ $GaAs_{0.18}Sb_{0.82}$ (near-broken gap)	600	200	2	740	60 (3V)	>500	150
[112]	Λ-shape	InP (001)	$In_{0.65}Ga_{0.35}As$/ $GaAs_{0.4}Sb_{0.6}$ (highly staggered)	700	150	0.4	110	$1.3X10^5$ (1.5V)	130	NA
This work	**V-shape**	**GaAs (001)**	**InAs/ $Al_{0.5}Ga_{0.5}Sb$ (near-broken)**	**80**	**200**	**1.8**	**433**	**$9.8x10^2$ (3V)**	**530**	**71**

Conclusion and Perspectives

In this thesis an entire fabrication process flow to fabricate tunnel diodes (TDs) and tunnel FETs (TFETs) from (Al)GaSb/InAs heterojunctions has been developed and optimized. The band alignment of this material system can be tuned from broken to staggered gap. Although the process for TD is direct, the process for TFET is quite challenging, especially when the junction widths are within the 25-80nm range. At first, two terminal Esaki tunnel diodes were used to optimize the epitaxial structure. We have shown a strong dependence of the maximum conductance and its variation steepness on the Al composition in the (Al)GaSb/InAs material system. The electrical characterization of $InAs_{0.91}Sb_{0.09}/Al_{0.4}Ga_{0.6}Sb$ and $InAs/Al_{0.4}Ga_{0.6}Sb$ TFETs has shown that aggressively scaling the channel width at the tunneling interface is necessary to enhance the gate electrostatic control over the channel. We show from the electrical characteristics of $InAs/Al_{0.5}Ga_{0.5}Sb$ TFETs that increasing the E_{beff} at the junction and increasing the thickness of the InAs channel layer has a drastic effect on the performance. In this latter case, the vertical architecture together with a V-shaped mesa etching of the InAs channel down to 80 nm at the tunneling interface has been achieved and resulted in a large I_{ON} of 433 µA/um at $V_{DS}=V_{GS}=0.5V$. This is the highest value so far reported in the literature within the $InAs/Al_XGa_{1-X}Sb$ material system. At room temperature, a high trap density in the gate oxide and at the semiconductor/oxide interface degrades the SS value. However, low temperature measurements limiting the influence of traps show a minimum SS of 71 mV/decade together with a 40 $\mu A.\mu m^{-1}$ ON current at V_{DS} = 0.1 V. These results indicate that further improvements of the gate-oxide/semiconductor interface could lead to a valuable solution in terms of ultra-low power logic.

The primary goal of this study was to develop a process flow for TFET fabrication in the (Al)GaSb/InAs system grown on a substrate. Further improvement in device performance in terms of SS and Ion/Ioff ratio at room temperature can be foreseen. For instance, pre- and post-ALD treatments or annealing have not been carried out. In the same way, the rather important DIBT at large V_{DS} could also been reduced by further increasing the gate electrostatic control with a larger aspect ratio between the channel body thickness and the gate length. As described in chapter 3, it is difficult to achieve steep sidewall

profiles with the chemical based wet etching technique defining the mesa width. Hence a dry plasma etch technique for InAs has to be developed. A FIB-STEM image of a TFET based on this dry etching technique is presented in Figure 81 demonstrating the possibility to reach sub-20 nm channel body thickness over more than 100 nm channel length. Large improvement of the gate electrostatic control over the channel could be expected with such a high aspect ratio technology.



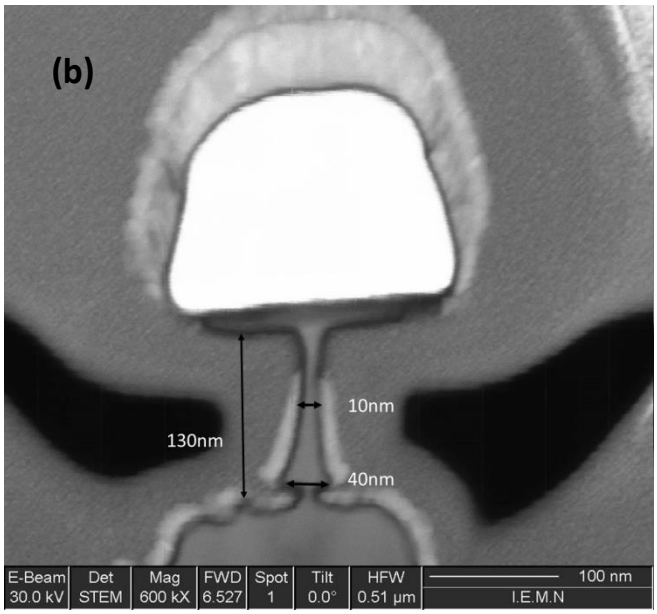


Figure 81: (a) SEM image of 25nm mesa width and (b) FIB-STEM image of 40 nm mesa width defined dry plasma etch technique.

References

[1] D. Kahng, “A Historical Perspective on the Development of MOS Transistors and Related Devices,” no. 7, 1976.

[2] S. Deleonibus, *Electronic device architectures for the nano-CMOS era : from ultimate CMOS scaling to beyond CMOS devices*. Pan Stanford, 2009.

[3] R. H. DENNARD, F. H. GAENSSLEN, H.-N. YU, V. LEO RIDEOVT, E. BASSOUS, and A. R. LEBLANC, “Design of Ion-Implanted MOSFET’s with Very Small Physical Dimensions,” *IEEE Solid-State Circuits Newsl.*, vol. 12, no. 1, pp. 38–50, 2007.

[4] An Steegen, “Pete’s Posts Blog » Blog Archive » What’s down the road for bulk FinFETs.” [Online]. Available: http://semimd.com/petes-posts/2013/10/31/whats-down-the-road-for-bulk-finfets/. [Accessed: 31-Jan-2017].

[5] S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices.,” *Nano Lett.*, vol. 8, no. 2, pp. 405–10, Feb. 2008.

[6] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, “I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q,” in *Digest. International Electron Devices Meeting,* 2002, pp. 289–292.

[7] E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, “Reduction of impact-ionization threshold energies for performance enhancement of complementary impact-ionization metal-oxide-semiconductor transistors,” *Appl. Phys. Lett.*, vol. 91, no. 15, p. 153501, Oct. 2007.

[8] K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer, “Impact Ionization MOS (I-MOS)—Part II: Experimental Results,” *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 77–84, Jan. 2005.

[9] A. Peschot, C. Qian, and T.-J. Liu, “Nanoelectromechanical Switches for Low-Power Digital Computing,” *Micromachines*, vol. 6, no. 8, pp. 1046–1065, Aug. 2015.

[10] N. Abele, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. M. Ionescu, “Suspended-gate MOSFET: bringing new MEMS functionality into solid-state MOS transistor,” in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, 2005, pp. 479–481.

[11] R. Nathanael, V. Pott, H. Kam, J. Jeon, and T.-J. K. Liu, “4-terminal relay technology for complementary logic,” in *2009 IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1–4.

[12] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, and H.-S. P. Wong, “Design Considerations for Complementary Nanoelectromechanical Logic Gates,” in *2007 IEEE International Electron Devices*

Meeting, 2007, pp. 299–302.

[13] A. Islam Khan, D. Bhowmik, P. Yu, S. Joo Kim, X. Pan, R. Ramesh, and S. Salahuddin, "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures," *Appl. Phys. Lett.*, vol. 99, no. 11, p. 113501, Sep. 2011.

[14] H. J. Song, D. Lv, J. B. Wang, B. Li, X. L. Zhong, L. H. Jia, and F. Wang, "Multi-channel ferroelectric-gate field effect transistors with excellent performance based on ZnO nanofibers," *RSC Adv.*, vol. 4, no. 97, pp. 54924–54927, Oct. 2014.

[15] W. Y. Choi and and J. D. P. K. Gopalakrishnan, P. B. Griffin, "Comparative Study of Tunneling Field-Effect Transistors and Metal–Oxide–Semiconductor Field-Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 49, no. 4, p. 04DJ12, Apr. 2010.

[16] "Wiley: Physics of Semiconductor Devices, 3rd Edition - Simon M. Sze, Kwok K. Ng." [Online]. Available: http://eu.wiley.com/WileyCDA/WileyTitle/productCd-0471143235.html. [Accessed: 09-May-2016].

[17] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches.," *Nature*, vol. 479, no. 7373, pp. 329–37, Nov. 2011.

[18] J. Knoch and J. Appenzeller, "A novel concept for field-effect transistors - the tunneling carbon nanotube FET," in *63rd Device Research Conference Digest, 2005. DRC '05.*, 2005, vol. 1, pp. 153–156.

[19] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[20] G. S. Samudra, "Tunneling Field-Effect Transistor: Effect of Strain and Temperature on Tunneling Current," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 981–983, Sep. 2009.

[21] O. M. Nayfeh, J. L. Hoyt, and D. A. Antoniadis, "Strained-Si1-xGex band-to-band tunneling transistors: Impact of tunnel-junction germanium composition and doping concentration on switching behavior," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2264–2269, 2009.

[22] Q. T. Zhao, J. M. Hartmann, and S. Mantl, "An Improved Si Tunnel Field Effect Transistor With a Buried Strained Si1-xGex Source," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1480–1482, Nov. 2011.

[23] K. Jeon, W.-Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, C. Park, C. S. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J. K. Liu, and C. Hu, "Si tunnel transistors with a novel silicided source and 46mV/dec swing," in *2010 Symposium on VLSI Technology*, 2010, pp. 121–122.

[24] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire n-type Tunneling FETs With Low Subthreshold Swing (<=50 mV/decade) at Room Temperature," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 437–439, Apr. 2011.

[25] D. K. Mohata, R. Bijesh, V. Saripalli, T. Mayer, and S. Datta, "Self-aligned gate

nanopillar In0.53Ga0.47As vertical tunnel transistor," in *69th Device Research Conference*, 2011, pp. 203–204.

[26] H. Zhao, N. Goel, J. Huang, Y. Chen, J. Yum, Y. Wang, F. Zhou, F. Xue, and J. Lee, "Factors enhancing In0.7Ga0.3As MOSFETs and tunneling FETs device performance," in *68th Device Research Conference*, 2010, pp. 63–64.

[27] H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, "In0.7Ga0.3As Tunneling Field-Effect Transistors With an Ion 50 uA/um and a subthreshold swing of 86 mV/dec Using HfO2 gate oxide," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1392–1394, Dec. 2010.

[28] M. Noguchi, S. Kim, M. Yokoyama, S. Ji, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, "High Ion/Ioff and low subthreshold slope planar-type InGaAs tunnel FETs with Zn-diffused source junctions," in *2013 IEEE International Electron Devices Meeting*, 2013, p. 28.1.1-28.1.4.

[29] A. Alian, J. Franco, A. Vandooren, Y. Mols, A. Verhulst, S. El Kazzi, R. Rooyackers, D. Verreck, Q. Smets, A. Mocuta, N. Collaert, D. Lin, and A. Thean, "Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, p. 31.7.1-31.7.4.

[30] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," in *2011 International Electron Devices Meeting*, 2011, p. 33.6.1-33.6.4.

[31] G. Zhou, Y. Lu, R. Li, Q. Zhang, W. S. Hwang, Q. Liu, T. Vasen, C. Chen, H. Zhu, J.-M. Kuo, S. Koswatta, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Vertical InGaAs/InP Tunnel FETs With Tunneling Normal to the Gate," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1516–1518, Nov. 2011.

[32] M. Fujimatsu, H. Saito, and Y. Miyamoto, "71 mV/dec of sub-threshold slope in vertical tunnel field-effect transistors with GaAsSb/InGaAs heterostructure," in *2012 International Conference on Indium Phosphide and Related Materials*, 2012, pp. 25–28.

[33] T. Yu, J. T. Teherani, D. A. Antoniadis, and J. L. Hoyt, "In0.53Ga0.47As/GaAs0.5 Sb0.5 Quantum-Well Tunnel-FETs with Tunable Backward Diode Characteristics," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1503–1505, Dec. 2013.

[34] D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan, and S. Datta, "Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio," in *2012 Symposium on VLSI Technology (VLSIT)*, 2012, pp. 53–54.

[35] B. Rajamohanan, R. Pandey, V. Chobpattana, C. Vaz, D. Gundlach, K. P. Cheung, J. Suehle, S. Stemmer, and S. Datta, "0.5 V Supply Voltage Operation of $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ Tunnel FET," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 20–22, Jan. 2015.

[36] D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, "Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300mV logic applications," in *2011 International Electron Devices Meeting*, 2011, p. 33.5.1-33.5.4.

[37] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. Xing, and A. Seabaugh, "AlGaSb/InAs Tunnel Field-Effect Transistor With On-Current of 78 uA/um at 0.5 V," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 363–365, Mar. 2012.

[38] D. Cutaia, K. E. Moselund, M. Borg, H. Schmid, L. Gignac, C. M. Breslin, S. Karg, E. Uccelli, and H. Riel, "Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si Using Selective Epitaxy in Nanotube Templates," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 176–183, May 2015.

[39] H. Riel, K. E. Moselund, C. Bessire, M. T. Bjork, A. Schenk, H. Ghoneim, and H. Schmid, "InAs-Si heterojunction nanowire tunnel diodes and tunnel FETs," in *2012 International Electron Devices Meeting*, 2012, p. 16.6.1-16.6.4.

[40] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III–V nanowire/Si heterojunction," in *2012 Symposium on VLSI Technology (VLSIT)*, 2012, pp. 47–48.

[41] R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, and A. Seabaugh, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 μA/μm at VDS= 0.5 V," in *2012 International Electron Devices Meeting*, 2012, p. 32.6.1-32.6.4.

[42] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-Dependent I-V Characteristics of a Vertical In0.53Ga0.47As Tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010.

[43] H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, F. Xue, and J. C. Lee, "Improving the on-current of In[sub 0.7]Ga[sub 0.3]As tunneling field-effect-transistors by p[sup ++]/n[sup +] tunneling junction," *Appl. Phys. Lett.*, vol. 98, no. 9, p. 93501, Feb. 2011.

[44] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Scaling of Vertical InAs-GaSb Nanowire Tunneling Field-Effect Transistors on Si," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 1–1, 2016.

[45] X. Zhao, A. Vardi, and J. A. del Alamo, "InGaAs/InAs heterojunction vertical nanowire tunnel fets fabricated by a top-down approach," in *2014 IEEE International Electron Devices Meeting*, 2014, p. 25.5.1-25.5.4.

[46] G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "InGaAs/InP Tunnel FETs With a Subthreshold Swing of 93 mV/dec and ION/IOFF Ratio Near 10^6," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 782–784, Jun. 2012.

[47] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. Xing, and A. Seabaugh, "AlGaSb / InAs Tunnel Field-Effect Transistor With On-Current of 78 uA/um at 0.5 V," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 363–365, 2012.

[48] Y. Zeng, C.-I. Kuo, C. Hsu, M. Najmzadeh, A. Sachid, R. Kapadia, C. Yeung, E. Chang, C. Hu, and A. Javey, "Quantum Well InAs/AlSb/GaSb Vertical Tunnel FET With HSQ Mechanical Support," *IEEE Trans. Nanotechnol.*, vol. 14, no. 3, pp. 580–584, May 2015.

[49] R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V Nguyen, D. Gundlach, C. A. Richter, J. Maier, K. Wang, T. Clarke, J. M. Fastenau, D. Loubychev, W. K. Liu, V. Narayanan, and S. Datta, "Demonstration of In0.9Ga0.1As/GaAs0.18Sb0.82 Near Broken-gap Tunnel FET with ION=740μA/μm,. GM=700μS/μm and Gigahertz Switching Performance at VDS=0.5V," in *2013 IEEE International Electron Devices Meeting*, 2013, p. 28.2.1-28.2.4.

[50] A. W. Dey, B. M. Borg, B. Ganjipour, M. Ek, K. A. Dick, E. Lind, C. Thelander, and L.-E. Wernersson, "High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 211–213, Feb. 2013.

[51] E. Lind, E. Memisevic, A. W. Dey, and L.-E. Wernersson, "III-V Heterostructure Nanowire Tunnel FETs," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 96–102, May 2015.

[52] L. Desplanque, M. Fahed, X. Han, V. K. Chinni, D. Troadec, M.-P. Chauvat, P. Ruterana, and X. Wallart, "Influence of nanoscale faceting on the tunneling properties of near broken gap InAs/AlGaSb heterojunctions grown by selective area epitaxy.," *Nanotechnology*, vol. 25, no. 46, p. 465302, 2014.

[53] J. Svensson, A. W. Dey, D. Jacobsson, and L.-E. Wernersson, "III-V Nanowire Complementary Metal-Oxide Semiconductor Transistors Monolithically Integrated on Si.," *Nano Lett.*, vol. 15, no. 12, pp. 7898–904, Dec. 2015.

[54] R. Pandey, H. Madan, H. Liu, V. Chobpattana, M. Barth, B. Rajamohanan, M. J. Hollander, T. Clark, K. Wang, J.-H. Kim, D. Gundlach, K. P. Cheung, J. Suehle, R. Engel-Herbert, S. Stemmer, and S. Datta, "Demonstration of p-type In0.7Ga0.3As/GaAs0.35Sb0.65 and n-type GaAs0.4Sb0.6/In0.65Ga0.35As complimentary Heterojunction Vertical Tunnel FETs for ultra-low power logic," in *2015 Symposium on VLSI Technology (VLSI Technology)*, 2015, pp. T206–T207.

[55] I. Silvaco, "Atlas User's Manual," 2016.

[56] R. Vishnoi and M. J. Kumar, "A Compact Analytical Model for the drain current of a TFET with non-abrupt doping profile incorporating the effect of band-gap narrowing," in *2015 IEEE 15th International Conference on Nanotechnology (IEEE-*

NANO), 2015, pp. 920–923.

[57] J. L. Padilla, F. Gamiz, and A. Godoy, "Impact of Quantum Confinement on Gate Threshold Voltage and Subthreshold Swings in Double-Gate Tunnel FETs," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3205–3211, Dec. 2012.

[58] C.-J. Chen, Y.-N. Chen, M.-L. Fan, V. P.-H. Hu, P. Su, and C.-T. Chuang, "Evaluation of TFET and FinFET devices and 32-Bit CLA circuits considering work function variation and line-edge roughness," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 2325–2328.

[59] Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. D. Chae, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, and P. Fay, "Performance of AlGaSb/InAs TFETs With Gate Electric Field and Tunneling Direction Aligned," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 655–657, May 2012.

[60] Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. D. Chae, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, and P. Fay, "Performance of AlGaSb/InAs TFETs With Gate Electric Field and Tunneling Direction Aligned," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 655–657, May 2012.

[61] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[62] S. Takagi, M. Kim, M. Noguchi, K. Nishi, and M. Takenaka, "Tunneling FET device technologies using III-V and Ge materials," in *2015 Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S)*, 2015, pp. 1–2.

[63] A. Mallik and A. Chattopadhyay, "Drain-Dependence of Tunnel Field-Effect Transistor Characteristics: The Role of the Channel," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4250–4257, Dec. 2011.

[64] J. L. Padilla, F. Gamiz, and A. Godoy, "A Simple Approach to Quantum Confinement in Tunneling Field-Effect Transistors," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1342–1344, Oct. 2012.

[65] Y. Lu, A. Seabaugh, P. Fay, S. J. Koester, S. E. Laux, W. Haensch, and S. O. Koswatta, "Geometry dependent tunnel FET performance - dilemma of electrostatics vs. quantum confinement," in *68th Device Research Conference*, 2010, pp. 17–18.

[66] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the Vertical Tunnel FET With Tunnel Bandgap Modulation and Gate Workfunction Engineering," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 909–917, May 2005.

[67] U. E. Avci and I. A. Young, "Heterojunction TFET Scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length," in *2013 IEEE International Electron Devices Meeting*, 2013, p. 4.3.1-4.3.4.

[68] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Appl. Phys. Lett.*, vol. 91, no. 5, p. 53102, 2007.

[69] R. M. Iutzi and E. A. Fitzgerald, “Microstructure and Band-Edge Steepness of InAs / GaSb Tunnel Diodes.”

[70] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, “Role of InAs and GaAs terminated heterointerfaces at source/channel on the mixed As-Sb staggered gap tunnel field effect transistor structures grown by molecular beam epitaxy,” *J. Appl. Phys.*, vol. 112, no. 2, p. 24306, 2012.

[71] M. Auf der Maur, B. Galler, I. Pietzonka, M. Strassburg, H. Lugauer, and A. Di Carlo, “Trap-assisted tunneling in InGaN/GaN single-quantum-well light-emitting diodes,” *Appl. Phys. Lett.*, vol. 105, no. 13, p. 133504, Sep. 2014.

[72] M. A. Khayer and R. K. Lake, “Drive Currents and Leakage Currents in InSb and InAs Nanowire and Carbon Nanotube Band-to-Band Tunneling FETs,” *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1257–1259, Dec. 2009.

[73] A. Sharma, A. K. Reza, and K. Roy, “Proposal of an Intrinsic-Source Broken-Gap Tunnel FET to Reduce Band-Tail Effects on Subthreshold Swing: A Simulation Study,” *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2597–2602, Jun. 2016.

[74] K. M. A. Rahman, “Nanocrystalline Silicon Solar Cells Deposited via Pulsed PECVD at 150°C Substrate Temperature,” 2010.

[75] L. B. Ruppalt, E. R. Cleveland, J. G. Champlain, S. M. Prokes, J. Brad Boos, D. Park, and B. R. Bennett, “Atomic layer deposition of Al2O3 on GaSb using in situ hydrogen plasma exposure,” *Appl. Phys. Lett.*, vol. 101, no. 23, p. 231601, 2012.

[76] H. Zhou, M. Zhang, and Y. Hao, “Performance Optimization of MOS-Like Carbon Nanotube FETs With Realistic Contacts,” *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3153–3162, Nov. 2010.

[77] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, “Scaling of Vertical InAs–GaSb Nanowire Tunneling Field-Effect Transistors on Si,” *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 549–552, May 2016.

[78] K. Bhatnagar, M. P. Caro, J. S. Rojas-Ramirez, R. Droopad, P. M. Thomas, A. Gaur, M. J. Filmer, and S. L. Rommel, “Integration of broken-gap heterojunction InAs/GaSb Esaki tunnel diodes on silicon,” *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 33, no. 6, p. 62203, 2015.

[79] D. J. Pawlik, “Comprehensive Mapping and Benchmarking of Esaki Diode Performance,” 2013.

[80] R. M. Iutzi, E. A. Fitzgerald, R. M. Iutzi, and E. A. Fitzgerald, “Microstructure and conductance-slope of InAs / GaSb tunnel diodes Microstructure and conductance-slope of InAs / GaSb tunnel diodes,” vol. 234503, no. 2014, 2016.

[81] E. Yablonovitch, “Band-Edge Steepness Obtained from Esaki / Backward Diode Current-Voltage Characteristics,” 2013.

[82] E. R. Cleveland, L. B. Ruppalt, B. R. Bennett, and S. M. Prokes, “Applied Surface

Science Effect of an in situ hydrogen plasma pre-treatment on the reduction of GaSb native oxides prior to atomic layer deposition," *Appl. Surf. Sci.*, vol. 277, pp. 167–175, 2013.

[83] A. R. Clawson, "Guide to references on III-V semiconductor chemical etching," *Mater. Sci. Eng. R Reports*, vol. 31, no. 1–6, pp. 1–438, 2001.

[84] P. T. Fukui and K. Tomioka, "Steep-Slope Tunnel Field-Effect Transistor (FET) using III-V Nanowire on Si," no. V, p. 2012, 2012.

[85] O. Dier, C. Lin, M. Grau, and M.-C. Amann, "Selective and non-selective wet-chemical etchants for GaSb-based materials," *Semicond. Sci. Technol.*, vol. 19, no. 11, pp. 1250–1253, 2004.

[86] G. C. Desalvo, R. Kaspi, and C. A. Bozada, "and InAs for Heterostructure Device Fabrication y ~ L ./," vol. 141, no. 12, pp. 3526–3531, 1994.

[87] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III-V nanowire/Si heterojunction," *Dig. Tech. Pap. - Symp. VLSI Technol.*, no. 2010, pp. 47–48, 2012.

[88] Y. Zhu and M. K. Hudait, "Low-power tunnel field effect transistors using mixed As and Sb based heterostructures," *Nanotechnol. Rev.*, vol. 2, no. 1, pp. 1–43, 2013.

[89] H. D. Trinh, G. Brammertz, E. Y. Chang, S. Member, C. I. Kuo, C. Y. Lu, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, B. T. Tran, K. Kakushima, and H. Iwai, "Electrical Characterization of Al 2 O 3 / n-InAs Metal – Oxide – Semiconductor Capacitors With Various Surface Treatments," vol. 32, no. 6, pp. 752–754, 2011.

[90] D. Y. Petrovykh, "Chemical and electronic properties of sulfur-passivated InAs surfaces," vol. 523, pp. 231–240, 2003.

[91] X. Zhao, A. Vardi, and J. A. Alamo, "InGaAs / InAs Heterojunction Vertical Nanowire Tunnel FETs Fabricated by a Top-down Approach," *IEEE Int. Electron Devices Meet.*, pp. 590–593, 2014.

[92] C.-Y. Hsu, C.-Y. Chang, E. Y. Chang, and C. Hu, "Suppressing Non-Uniform Tunneling in InAs/GaSb TFET With Dual-Metal Gate," *IEEE J. Electron Devices Soc.*, vol. 4, no. 2, pp. 60–65, Mar. 2016.

[93] S. Agarwal and E. Yablonovitch, "Band-Edge Steepness Obtained From Esaki/Backward Diode Current–Voltage Characteristics," *IEEE Trans. Electron Devices*, vol. 61, no. 5, 2014.

[94] P. M. Solomon, J. Jopling, D. J. Frank, C. D'Emic, O. Dokumaci, P. Ronsheim, and W. E. Haensch, "Universal tunneling behavior in technologically relevant P/N junction diodes," *J. Appl. Phys.*, vol. 95, no. 10, p. 5800, 2004.

[95] D. Pawlik, B. Romanczyk, P. Thomas, S. Rommel, M. Edirisooriya, R. Contreras-Guerrero, R. Droopad, W.-Y. Loh, M. H. Wong, K. Majumdar, W.-E. Wang, P. D. Kirsch, and R. Jammy, "Benchmarking and improving III-V Esaki diode performance with a record 2.2 MA/cm^2 peak current density to enhance TFET drive

current," in *2012 International Electron Devices Meeting*, 2012, p. 27.1.1-27.1.3.

[96] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-Dependent I-V Characteristics of a Vertical In0.53Ga0.47As Tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010.

[97] K. Bhatnagar, M. P. Caro, J. S. Rojas-Ramirez, R. Droopad, P. M. Thomas, A. Gaur, M. J. Filmer, and S. L. Rommel, "Integration of broken-gap heterojunction InAs/GaSb Esaki tunnel diodes on silicon," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 33, no. 6, p. 62203, Nov. 2015.

[98] R. M. Iutzi and E. A. Fitzgerald, "Microstructure and conductance-slope of InAs/GaSb tunnel diodes," *J. Appl. Phys.*, vol. 115, no. 23, p. 234503, Jun. 2014.

[99] R. M. Iutzi and E. A. Fitzgerald, "Conductance slope and curvature coefficient of InGaAs/GaAsSb heterojunctions at varying band alignments and its implication on digital and analog applications," *J. Appl. Phys.*, vol. 118, no. 23, p. 235702, Dec. 2015.

[100] Salim El Kazzi, "Croissance épitaxiale d'hétérostructures antimoniées sur substrats fortement désadaptés en maille pour applications aux transistors à effet de champ," University Lille1- science et Technologies, 2012.

[101] Y.-C. Wu, E. Y. Chang, Y.-C. Lin, C.-C. Kei, M. K. Hudait, M. Radosavljevic, Y.-Y. Wong, C.-T. Chang, J.-C. Huang, and S.-H. Tang, "Study of the inversion behaviors of Al2O3/InxGa1−xAs metal–oxide–semiconductor capacitors with different In contents," *Solid. State. Electron.*, vol. 54, no. 1, pp. 37–41, 2010.

[102] R. Li, Y. Lu, S. D. Chae, G. Zhou, Q. Liu, C. Chen, M. Shahriar Rahman, T. Vasen, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. G. Xing, S. Koswatta, and A. Seabaugh, "InAs/AlGaSb heterojunction tunnel field-effect transistor with tunnelling in-line with the gate field," *Phys. status solidi*, vol. 9, no. 2, pp. 389–392, Feb. 2012.

[103] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. Xing, and A. Seabaugh, "AlGaSb/InAs Tunnel Field-Effect Transistor With On-Current of 78 uA/um at 0.5 V," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 363–365, Mar. 2012.

[104] Guangle Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and Huili Xing, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 uA/um at VDS=0.5 V," in *2012 International Electron Devices Meeting*, 2012, p. 32.6.1-32.6.4.

[105] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Scaling of Vertical InAs–GaSb Nanowire Tunneling Field-Effect Transistors on Si," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 549–552, May 2016.

[106] L. Desplanque, M. Fahed, X. Han, V. K. Chinni, D. Troadec, M.-P. Chauvat, P. Ruterana, and X. Wallart, "Influence of nanoscale faceting on the tunneling properties of near broken gap InAs/AlGaSb heterojunctions grown by selective area epitaxy," *Nanotechnology*, vol. 25, no. 46, p. 465302, Nov. 2014.

[107] D. K. Schroder, *Semiconductor material and device characterization*, 3rd editio. IEEE Press, 2006.

[108] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2006.

[109] Guangle Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and Huili Xing, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 uA/um at VDS=0.5 V," in *2012 International Electron Devices Meeting*, 2012, p. 32.6.1-32.6.4.

[110] A. W. Dey, B. M. Borg, B. Ganjipour, M. Ek, K. A. Dick, E. Lind, C. Thelander, and L.-E. Wernersson, "High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 211–213, Feb. 2013.

[111] R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V Nguyen, D. Gundlach, C. A. Richter, J. Maier, K. Wang, T. Clarke, J. M. Fastenau, D. Loubychev, W. K. Liu, V. Narayanan, and S. Datta, "Demonstration of In0.9Ga0.1As/GaAs0.18Sb0.82 near broken-gap tunnel FET with ION=740μA/μm, GM=70μS/μm and gigahertz switching performance at VDs=0.5V," in *2013 IEEE International Electron Devices Meeting*, 2013, p. 28.2.1-28.2.4.

[112] B. Rajamohanan, R. Pandey, V. Chobpattana, C. Vaz, D. Gundlach, K. P. Cheung, J. Suehle, S. Stemmer, and S. Datta, "0.5 V Supply Voltage Operation of In $_{0.65}$ Ga $_{0.35}$ As/GaAs $_{0.4}$ Sb $_{0.6}$ Tunnel FET," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 20–22, Jan. 2015.

Appendix

Appendix I: Diode process

1. Marker & Drain level

1.1 Spin coating of Co-polymer & PMMA	EL 6% (MAA 8.5) Speed=2500;acc=1000;time=12'' PMMA 4% 950K Speed=2500;acc=1000;time=10'' 170°C baking for 3' after each coating
1.2 E-beam Lithography (mask layer 1,2)	Resolution=0.020 ;Current : 20nA ; Dose=220μC/cm^2
1.3 Resist development	MIBK/IPA (70ml/70ml) ≈1'45'' + 3' IPA cleaning
1.4 metal deposition	Ti/Au/Ti : 100/800/100 Å; etch: 1'30''; 150eV
1.5 Metal lift off	SVC-14; RPM=300; TEMP=80°C ≈ 30'

2. Device Mesa Wet etching

*2.1 Deoxydation	HCL/H20 (1/10) TIME: 1min
*2.2 Phosphoric acid	H3PO4/H2O2/H20 (2/1/6) time: 8 Sec
*2.3 Citric acid	Citric acid/H2O (1/1) TIME: 1 MIN

* The above process is used to etch a 200 nm-thick InAs layer. The process is modified according to the epi-layer and its thickness.

3. SiO2 deposition all over the wafer

30 nm at 300° C

4. SiO2 opening of apertures in source and drain pad regions (RIE Dry etch + HF treatment)

4.1 Spin coating of PMMA	PMMA 4% 950K Speed=2500;acc=1000;time=10'' 170°C baking for 3' after each coating
4.2 E-beam Lithography (mask layer 5,13)	Mask layer 13: Resolution=0.010 ;Current : 10nA ; Dose=220μC/cm^2 Mask layer 5 : Resolution=0.025 ;Current : 20nA ; Dose=220μC/cm^2

4.3 Resist development	MIBK/IPA (70ml/70ml) ≈3’ + 3’ IPA cleaning
4.4 Dry etch + HF/H2O(1/4)	RIE dry etch (2’30’’) + 15’’

5. Ammonia/tartric acid treatment 50nm-AlGaSb (≈ 3’) + HF (5%)/H2O (20/80ml) 15’’

6. Metallization for drain & source pads

6.1 Spin coating of PMMA	Copo ARP 33 % Speed=1500;acc=1000;time=12’’ **~6000Å** PMMA 4% 950K Speed=2500;acc=1000;time=10’’ 170°C baking for 3’ after each coating
6.2 E-beam Lithography (mask layer 5,15)	Resolution=0.025 ;Current : 20nA ; Dose=220μC/cm^2
6.3 Resist development	MIBK/IPA (70ml/70ml) ≈3’ + 3’ IPA cleaning + Methanol/ipa (1/3) 3’
6.4 metal deposition	Ti/Au : 1000/2000 Å (tilt 30° rotation) + Au: 3000 Å; Ar etching : 2’; 150eV ;
6.5 Metal lift off	SVC-14; RPM=300; TEMP=80°C ≈ 2 hrs

Appendix II: TFET process

TFET-I **50nm InAs n^+ Si-($1x10^{19}/cm^3$)** **80nm InAs n^+ (intrinsic)** **50nm $Al_{0.4}Ga_{0.6}Sb$ p^+ Si-($1x10^{19}/cm^3$)** **600nm GaSb p^+ Si-($1x10^{19}/cm^3$)** **S.I. GaAs substrate**	**Substrate: GaSb-Sub** **Drain contact: Ti/Au/Ti (20/100/10 nm)** **Gate contact: Ni (80nm)** **Gate Oxide: 7 nm- Al_2O_3** **Source contact: Ti/Au (20/170 nm)**
1. Defining Marker & drain contact 1.1 Spin coating of Co-polymer & PMMA	EL 6% (MAA 8.5); **2000/1000/12''** ≈220 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
1.2 E-beam Lithography	Resolution: 20 nm ; Current: 20nA ; Dose: 220 μC/cm^2
1.3 Resist development	MIBK/IPA (1/1) **≈1'45''** + 3' IPA cleaning
1.4 metal deposition	Ti/Au/Ti : 20/100/10 nm
1.5 Metal lift off	SVC-14; Temp=70°C ≈ **2 hrs**
2. Wet mesa etching 2.1 Wet mesa etching of InAs	HCl/H_2O (1/10) : 1 min $H_3PO_4/H_2O_2/H_2O$ (2/1/6) : 4 sec $C_6H_8O_7/H_2O_2$ (1/1) : 25 sec
3. Gate Oxide deposition 3.1 Pre-treatment	HCl/H_2O (1/10) : 30 sec Stopant: IPA
3.2 Gate oxide deposition	4 nm- Al_2O_3 Thermal mode; temperature: 300^0 C; 40 cycles
4. Contact window opening of Al_2O_3 on drain and source regions (ICP dry plasma etching) 4.1 Spin coating of PMMA	PMMA 4% 950K; **2500/1000/10''**≈220 nm (opening of drain & source contact to etch Al_2O_3)
4.2 E-beam lithography	Resolution: 0.010; Current : 10 nA; Dose = 220μC/cm^2
4.3 Resist development	MIBK/IPA (1/1): **2'** of development time is

	ideal
4.4 Dry plasma etching	To etch 4 nm Al_2O_3 RIE = 50; BCl_3 = 30 sccm; ICP = 200 W; time = **1 '30''**; Pressure = 2m Torr; temp/precision He = 10°C/5 torr
4.5 Cleaning	SVC-14 @ 70 °C for **≈2 hrs**
5. Gate metal patterning 5.1 Spin coating of Co-polymer & PMMA	Copo ARP 33%/ Ethyl lactate (1/0.5) **2600/1000/12''**≈120 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
5.2 E-beam lithography	Resolution: 0.010; Current: 10 nA ; Dose = 220μC/cm^2
5.3 Resist development	MIBK/IPA (1/1) ≈ **1'40''** Methanol/IPA (1/3) ≈ **2'30''**
5.4 Gate metallization	Ni: 80 nm @ 60° tilt; rotation
5.5 Lift-off	SVC-14 @ 70 °C ≈ **10'-20'**
6. Isolation of devices 6.1 30 nm SiO_2 at 300° C by PECVD	
6.2 SiO_2 opening of aperture in source and drain pad regions (RIE Dry etch + HF treatment)	PMMA 4% 950K Speed=2500;acc=1000;time=10'' 170°C baking for 3' after each coating
7. Metallization of drain and source pads 7.1 Spin coating of PMMA	Copo ARP 33 % Speed=1500;acc=1000;time=12'' **~6000Å** PMMA 4% 950K Speed=2500;acc=1000;time=10'' 170°C baking for 3' after each coating

7.2 E-beam Lithography (mask layer 5,15)	Resolution=0.025 ;Current : 20nA ; Dose=220μC/cm^2
7.3 Resist development	MIBK/IPA (70ml/70ml) ≈3’ + 3’ IPA cleaning + Methanol/ipa (1/3) 3’
7.4 metal deposition	Ti/Au : 1000/2000 Å (tilt 30° rotation) + Au: 3000 Å; Ar etching : 2’; 150eV ;
7.5 Metal lift off	SVC-14; RPM=300; TEMP=80°C ≈ 2 hrs

TFET-II **50nm InAs n^+ Si-($1x10^{19}/cm^3$)** **80nm InAs n^+ (intrinsic)** **50nm $Al_{0.4}Ga_{0.6}Sb$ p^+ Si-($1x10^{19}/cm^3$)** **600nm GaSb p^+ Si-($1x10^{19}/cm^3$)** **S.I. GaAs substrate**	**Substrate: GaAs-Sub** **Drain contact: Ti/Au/Ti (20/100/10 nm)** **Gate contact: Ni (80nm)** **Gate Oxide: 4 nm- Al_2O_3** **Source contact: Ti/Au (20/170 nm)**
1. Defining Marker & drain contact 1.1 Spin coating of Co-polymer & PMMA	EL 6% (MAA 8.5); **2000/1000/12''** ≈220 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
1.2 E-beam Lithography	Resolution: 20 nm ; Current: 20nA ; Dose: 220 μC/cm^2
1.3 Resist development	MIBK/IPA (1/1) ≈**1'45''** + 3' IPA cleaning
1.4 metal deposition	Ti/Au/Ti : 20/100/10 nm
1.5 Metal lift off	SVC-14; Temp=70°C ≈ **2 hrs**
2. Wet mesa etching 2.1 Wet mesa etching of InAs	HCl/H_2O (1/10) : 1 min $H_3PO_4/H_2O_2/H_2O$ (2/1/6) : 4 sec $C_6H_8O_7/H_2O_2$ (1/1) : 25 sec
3. Gate Oxide deposition 3.1 Pre-treatment	HCl/H_2O (1/10) : 30 sec Stopant: IPA
3.2 Gate oxide deposition	4 nm- Al_2O_3 Thermal mode; temperature: 300^0 C; 40 cycles
4. Contact window opening of Al_2O_3 on drain and source regions (ICP dry plasma etching) 4.1 Spin coating of PMMA	PMMA 4% 950K; **2500/1000/10''**≈220 nm (opening of drain & source contact to etch Al_2O_3)
4.2 E-beam lithography	Resolution: 0.010; Current : 10 nA; Dose = 220μC/cm^2
4.3 Resist development	MIBK/IPA (1/1): **2'** of development time is ideal

4.4 Dry plasma etching	To etch 4 nm Al_2O_3 RIE = 50; BCl_3 = 30 sccm; ICP = 200 W; time = **1 '30''**; Pressure = 2m Torr; temp/precision He = 10°C/5 torr
4.5 Cleaning	SVC-14 @ 70 °C for **≈2 hrs**
5. Gate metal patterning 5.1 Spin coating of Co-polymer & PMMA	Copo ARP 33%/ Ethyl lactate (1/0.5) **2600/1000/12''**≈120 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
5.2 E-beam lithography	Resolution: 0.010; Current: 10 nA ; Dose = 220μC/cm^2
5.3 Resist development	MIBK/IPA (1/1) ≈ **1'40''** Methanol/IPA (1/3) ≈ **2'30''**
5.4 Gate metallization	Ni: 80 nm @ 60° tilt; rotation
5.5 Lift-off	SVC-14 @ 70 °C ≈ **10'-20'**
6. Source contact patterning 6.1 Spin coating of Co-polymer & PMMA	EL 6% (MAA 8.5); **1500/1000/12''**≈220 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
6.2 E-beam lithography	Resolution: 0.020; Current : 20 nA ; Dose = 220μC/cm^2
6.3 Resist development	MIBK/IPA (1/1) ≈ **1'40''**
6.4 Source contact metallization	Ti/Au : 20/170 nm
6.5 Lift-off	SVC-14 @ 70 °C ≈ **2 hrs**
7. Isolation of devices 7.1 Spin coating of HMDS & SAL601	1. Clean with IPA 2. Dehydration @ 200°C for 10 minutes 3. Blow N2 air for 1 min to cool down 4. Prepare HMDS **3000/1000/12''** 5. Immediately SAL 601 **1500/1000/12''**
7.2 E-beam lithography	Current:100pA ; Dose = 5μC/cm^2
7.3 Resist development	Prebake @ 115 °C for 3 min Development: MF 322 ≈ **1'30''**
7.4 Etching of buffer	**Dry etch**: GaSb Buffer RIE = 50; BCl_3 = 30 sccm; ICP = 200 W;

	time = 1’30’’; Pressure = 2m Torr; temp/precision He = 10°C/5 torr Etch depth: 300 nm **Wet etch**: 1. Tartaric acid = 10 g; DI H2O = 100 ml; 37% HCl = 80 ml; Stirred continuously for 1 hour to cool down to 20° C. 2. Add H_2O_2 =7 ml just before performing etch. Etch rate is ≈ 310-320 nm ≈ **45-50’’** to 310-320 nm
7.5 Cleaning	SVC-14 @ 70 °C for ≈ **2 hrs**
8. 2-Step bridge process for air-bridge Step-1 8.1.1 Spin coating PMMA	PMMA 5 % 950 K; **1750/1000/10’’** ≈ 500nm Baked @ 180 ° C for **1’30’’**
8.1.2 E-beam Lithography	Res: 0.010; current = 10 nA; dose = 250 μC/cm^2 Contact area (large contact region) Res: 0.025; current = 70 nA; dose = 270 μC/cm^2
8.1.3 Resist development	MIBK/IPA (1/1) ≈ **2’**
8.1.4 Reflow	**45’’+15’’** @ 170 ° C
Step-2 8.2.1 Spin coat Copo ARP 33% (2 μm) 8.2.2 spin coat ZEP 520A	**2100/1000/12’’** @ 140 ° C for **2’** to get ≈ 2 μm thick **2500/1000/8’’** @ 140 ° C for **2’** to get ≈ 370 nm thick
8.2.3 E-beam lithography	Device region Res: 0.010; current: 6nA; Dose = 160 μC/cm^2 Large contact region Res: 0.025; current: 40nA; Dose = 160 μC/cm^2
8.2.4 Development	Zn50 for ZEP ≈ **30’’** Etchant stoppant : DI H_2O Methanol/IPA (1/3) ≈ **45’’**stoppant: IPA
8.2.5 Metallization	1000/7000 Å (Ti/Au)
8.2.6 Lift-off	SVC-14 @ 70 °C ≈ **2 hrs**

TFET-III **50nm InAs n^+ Si-($1x10^{19}/cm^3$)** **200nm InAs n^+ (intrinsic)** **50nm $Al_{0.5}Ga_{0.5}Sb$ p^+ Si-($1x10^{19}/cm^3$)** **(Linearly graded 0.2->0.5)** **600nm InAs p^+ Si-($1x10^{19}/cm^3$)** **S.I. GaAs substrate**	**Substrate: GaAs-Sub** **Drain contact: Ti/Au/Ti (20/100/10 nm)** **Gate contact: Ni (80nm)** **Gate Oxide: 4 nm- Al_2O_3** **Source contact: Ti/Au (20/170 nm)**
1. Defining Marker & drain contact 1.1 Spin coating of Co-polymer & PMMA	EL 6% (MAA 8.5); **2000/1000/12''** ≈220 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
1.2 E-beam Lithography	Resolution: 20 nm ; Current: 20nA ; Dose: 220 μC/cm^2
1.3 Resist development	MIBK/IPA (1/1) ≈**1'45''** + 3' IPA cleaning
1.4 metal deposition	Ti/Au/Ti : 20/100/10 nm
1.5 Metal lift off	SVC-14; Temp=70°C ≈ **2 hrs**
2. Wet mesa etching 2.1 Wet mesa etching of InAs	HCl/H_2O (1/10) : 1 min $H_3PO_4/H_2O_2/H_2O$ (2/1/6) : 6 sec $C_6H_8O_7/H_2O_2$ (1/1) : 20 sec
3. Gate Oxide deposition 3.1 Pre-treatment	HCl/H_2O (1/10) : 30 sec Stopant: IPA
3.2 Gate oxide deposition	4 nm- Al_2O_3 Thermal mode; temperature: 300^0 C; 40 cycles
4. Contact window opening of Al_2O_3 on drain and source regions (ICP dry plasma etching) 4.1 Spin coating of PMMA	PMMA 4% 950K; **2500/1000/10''**≈220 nm (opening of drain & source contact to etch Al_2O_3)
4.2 E-beam lithography	Resolution: 0.010; Current : 10 nA; Dose = 220μC/cm^2
4.3 Resist development	MIBK/IPA (1/1): **2'** of development time is ideal
4.4 Dry plasma etching	To etch 4 nm Al_2O_3 RIE = 50; BCl_3 = 30 sccm; ICP = 200 W; time = **1 '30''**;

	Pressure = 2m Torr; temp/precision He = 10°C/5 torr
4.5 Cleaning	SVC-14 @ 70 °C for **≈2 hrs**
5. Gate metal patterning 5.1 Spin coating of Co-polymer & PMMA	Copo ARP 33%/ Ethyl lactate (1/0.5) **2600/1000/12''**≈120 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
5.2 E-beam lithography	Resolution: 0.010; Current: 10 nA ; Dose = 220μC/cm^2
5.3 Resist development	MIBK/IPA (1/1) ≈ **1'40''** Methanol/IPA (1/3) ≈ **2'30''**
5.4 Gate metallization	Ni: 80 nm @ 60° tilt; rotation
5.5 Lift-off	SVC-14 @ 70 °C ≈ **10'-20'**
6. Source contact patterning 6.1 Spin coating of Co-polymer & PMMA	EL 6% (MAA 8.5); **1500/1000/12''**≈220 nm PMMA 4% 950K; **2500/1000/10''**≈220 nm 180°C baking for 3' after each coating
6.2 E-beam lithography	Resolution: 0.020; Current : 20 nA ; Dose = 220μC/cm^2
6.3 Resist development	MIBK/IPA (1/1) ≈ **1'40''**
6.4 Source contact metallization	Ti/Au : 20/170 nm
6.5 Lift-off	SVC-14 @ 70 °C ≈ **2 hrs**
7. Isolation of devices 7.1 Spin coating of HMDS & SAL601	1. Clean with IPA 2. Dehydration @ 200°C for 10 minutes 3. Blow N2 air for 1 min to cool down 4. Prepare HMDS **3000/1000/12''** 5. Immediately SAL 601 **1500/1000/12''**
7.2 E-beam lithography	Current:100pA ; Dose = 5μC/cm^2
7.3 Resist development	Prebake @ 115 °C for 3 min Development: MF 322 ≈ **1'30''**
7.4 Etching of buffer	**Dry etch**: InAs Buffer **Wet etch**: $H_3PO_4/H_2O_2/H_2O$ (2/1/6) : 20 sec $C_6H_8O_7/H_2O_2$ (1/1) : 60 sec

7.5 Cleaning of resist	SVC-14 @ 70 °C for ≈ **2 hrs**
8. 2-Step bridge process for air-bridge Step-1 8.1.1 Spin coating PMMA	 PMMA 5 % 950 K; **1750/1000/10''** ≈ 500nm Baked @ 180 ° C for **1'30''**
8.1.2 E-beam Lithography	Res: 0.010; current = 10 nA; dose = 250 μC/cm^2 Contact area (large contact region) Res: 0.025; current = 70 nA; dose = 270 μC/cm^2
8.1.3 Resist development	MIBK/IPA (1/1) ≈ **2'**
8.1.4 Reflow	**45''+15''** @ 170 ° C
Step-2 8.2.1 Spin coat Copo ARP 33% (2 μm) 8.2.2 spin coat ZEP 520A	 **2100/1000/12''** @ 140 ° C for **2'** to get ≈ 2 μm thick **2500/1000/8''** @ 140 ° C for **2'** to get ≈ 370 nm thick
8.2.3 E-beam lithography	Device region Res: 0.010; current: 6nA; Dose = 160 μC/cm^2 Large contact region Res: 0.025; current: 40nA; Dose = 160 μC/cm^2
8.2.4 Development	Zn50 for ZEP ≈ **30''** Etchant stoppant : DI H_2O Methanol/IPA (1/3) ≈ **45''**stoppant: IPA
8.2.5 Metallization	1000/7000 Å (Ti/Au)
8.2.6 Lift-off	SVC-14 @ 70 °C ≈ **2 hrs**

List of Publications

1. L. Desplanque, M. Fahed, X. Han, **V. K. Chinni**, D. Troadec, M.-P. Chauvat, P. Ruterana, and X. Wallart, "Influence of nanoscale faceting on the tunneling properties of near broken gap InAs/AlGaSb heterojunctions grown by selective area epitaxy," *Nanotechnology*, vol. 25, no. 46, p. 465302, Nov. 2014.

2. **V.K. Chinni**, L. Desplanque, M. Zaknoune and X. Wallart, "V-shaped InAs/$Al_{0.5}Ga_{0.5}Sb$ VerticalTunnel FET on GaAs (001) Substrate with I_{ON}=433 µA.µm^{-1} at V_{DS}= 0.5V," IEEE *Journal of the electron devices society (JEDS)*, Vol. 5, No. 1, January 2017.

International conferences:

1. L. Desplanque, X.L. Han, M. Fahed, **V.K. Chinni**, D. Troadec, M.P. Chauvat, P. Ruterana, X. Wallart, "InAs/AlGaSb Esaki tunnel diodes grown by selective area epitaxy on GaSb (001) substrate," *IPRM 2014*, Montpellier, France, 11-15 May 2014.

2. L. Desplanque, X.L. Han, M. Fahed, **V.K. Chinni**, D. Troadec, M.P. Chauvat, P. Ruterana, X. Wallart, "Selective area epitaxy of InAs/AlGaSb heterostructures on GaSb (001) substrate for tunnel diode applications," *18th MBE 2014*, Flagstaff, AZ, USA, 7-12 September 2014.

3. **V.K. Chinni**, L. Desplanque, M. Zaknoune and X. Wallart, "V-shaped InAs/$Al_{0.5}Ga_{0.5}Sb$ Vertical Tunnel FET on GaAs Substrate," *IPRM 2016*, Toyama, Japan,

26-30 June 2016.

National conferences:

1**. V.K. Chinni**, L. Desplanque, M. Zaknoune and X. Wallart, "InAs based Esaki tunnel diodes," *JNRDM 2014*, Lille, France, 26-28 May 2014.

2. **V.K. Chinni**, M. Zaknoune, C. Coinon, X. Wallart and L. Desplanque,"Fabrication and characterization of InAs/$Al_{0.5}Ga_{0.5}Sb$ vertical tunnel FET on GaAs substrate," *JNMO 2016*, Les Issambres, France, 30 May- 1 June 2016.

3. Y. Lechaux, **V.K. Chinni**, V. Talbo, M. Pastorek, N. Wichmann, S. Bollaert," Fabrication et caractérisation de diodes PIN GaSb pour la réalisation de transistors I-MOSFETs," *JNMO 2016*, Les Issambres, France, 30 May- 1 June 2016.