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Par

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"Fabrication and characterization of III-V MOSFETs for high performance and low power applications"

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Résumé

La réduction de la taille des circuits CMOS vers des dimensions extrêmement petites est telle que son élément constitutif, le MOSFET à base de Silicium, commence à souffrir d'une faible efficacité de puissance. L'une des alternatives qui ne peut être écartée est le concept du transistor MOSFET à base de matériaux III-V. Ses propriétés de transport extraordinaires, apportées par les matériaux III-V, promettent de réduire la tension d'alimentation des circuits CMOS sans réduire leur performance. Cette transition technologique pourrait aboutir non seulement à des circuits CMOS plus petits, plus écologiques mais aussi à des circuits co-intégrés avec des technologies RF.
C'est dans ce contexte que nous présentons, dans ce travail de thèse, la fabrication et la caractérisation des transistors MOSFET Ultra-Thin Body (UTB) à base d'InAs et du transistor FinFET à base d'InAs. La combinaison d'une longueur de grille extrêmement réduite, d'une faible résistance d'accès et d'une mobilité impressionnante dans le canal d'InAs a permis d'obtenir des courants importants (I_{MAX}=2000mA/mm pour L_G=25nm). Egalement, l'utilisation des architectures du canal de type ultra mince et FinFET permet d'obtenir un bon contrôle électrostatique. De plus, une spécificité du procédé technologique présentée dans ce travail est les réalisations des contacts et du canal par une épitaxie par jets moléculaires (MBE) localisée.

Mots-clés: Matériaux III-V, MOSFET, Ultra-Thin Body, Gate-All Around, FinFET, recroissance, MBE, ALD

Abstract

Scaling the size of CMOS circuits to extremely small dimensions gets the semiconductor industry to a point where its cornerstone, Silicon-based MOSFET starts to suffer a poor power efficiency. In the quest for alternative solutions cannot be omitted a concept of III-V MOSFET. Its outstanding transport properties hold a promise of reduced CMOS supply voltage without compromising the performance. This can path a way not only to the smaller, greener electronics but also to more co-integrated RF and CMOS electronics.
In this context, we present fabrication and characterization of Ultra-Thin body InAs MOSFETs and InAs FinFET. Synergy of a deeply scaled gate length, low access resistance and a high mobility of InAs channel enabled to obtain impressively high drain currents (I_{MAX}=2000mA/mm for L_G=25nm). Equally, the introduction of Ultra-Thin body and FinFET channel design provides an improved electrostatic control. A specific feature of the process presented in this work is a fabrication of contacts and channel by localized molecular beam epitaxy MBE epitaxy.

Keywords: III-V Material, MOSFET, Ultra-Thin Body, Gate-All Around, FinFET, regrowth, MBE, ALD

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List of abbreviations

2D	Two dimensional
2DEG	Two Dimensional Electron Gas
3D	Three dimensional
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BOE	Buffer Oxide Etch
BTBT	Band To Band Tunneling
CBO	Conduction Band Gap Offset
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DOS	Density of States
EBL	Electron Beam Lithography
EDX	Electron Diffraction Spectroscopy
EOT	Effective Oxide Thickness
FinFET	Fin shaped Field Effect Transistor
GAA	Gate-All Around
GIDL	Gate Induced Drain Leakage
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HF-LF	High Frequency Low Frequency
HMDS	Hexamethyldisiloxane
HP	High Performance
HRTEM	High Resolution TEM
HSQ	Hydrogen silsesquioxane (resist)
ICP-RIE	Inductively Coupled Plasma RIE
IEMN	Institute of Electronics Microelectronics and Nanotechnology
IPA	Isopropanol
MBE	Molecular Beam Epitaxy
MIBK	Methyl Isobutyl Ketone
MIT	Massachussets Institute of Technology
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconducteur
MOSFET	Metal Oxyde Semiconductor Field Effect Transistor
MugFET	Multiple Gate Field Effect Transistor
NID	Non Intentionally Doped
PDA	Post Deposition Annealing
QW MOSFET	Quantum Well Metal Oxyde Semiconductor Field Effect Transistor
RF	Radio Frequency
RIE	Reactive Ion Etching
RMS	Root Mean Square Roughness
RTA	Rapid Thermal Annealing
SBH	Schottky Barrier Height

SCE	Short Channel Effects
SEM	Scanning Electron Microscopy
SOI	Silicon On Insulator
SS	Subthreshold Swing
TDMAH	Tetrakis-Dimethyl-Amido-Hafnium
TEM	Transmission Electron Microscopy
TLM	Transfer Length Measurement
TMA	Trimethyl-Aluminium
TMAH	Tetramethylammonium hydroxide
ULP	Ultra Low Power
UTB	Ultra-Thin Body
VLS	Vapor Liquid Solid Growth
VLSI	Very Large Scale Integration

General Introduction

1 Power constrained scaling

1.1 Moore's law

During the last 50 years, we have been witnessing an incessant technological advance in microelectronics devices. Fifty years ago, a chip contained only dozens of gates whereas today the number has dramatically increased to several billions. This provided us with immense and complex circuits that are integrated into modern electronic devices. Such a huge progress was governed by Moore's law formulated around 50 years ago. In the article "Cramming More Components onto Integrated Circuits" [1], Gordon Moore made a prediction that the number of transistor per chip would double every 24 months. Hereafter, the entire silicon industry has adopted his theory as a dogma that relentlessly dictates the trend of circuit miniaturization.

The building block of today's logical circuits is Complementary Metal Oxide Semiconductor (CMOS) technology consisting of p and n-type MOSFET transistor. Following Moore's law and a CMOS scaling theory, its dimensions such as gate length, width and oxide thickness are reduced proportionally by a scaling factor (λ) equal to $\sqrt{2}$. Keeping a constant electric field in the channel implicates that a supply voltage (V_{DD}) is reduced along with the MOSFET's dimensions by a factor of λ. This is translated into an increased performance gain, proportional to λ, while the power density remains constant.

1.2 End of Moore's law

However, scaling the CMOS technology below 90 nm gate length is characterized by a difficulty to reduce the device dimensions along with the supply voltage (V_{DD}). Limiting factor starts to be a leakage power density [2][3] (**Figure 1**) that is related to the off-state current. Since the off-state current is exponentially dependent on the threshold voltage, the latter cannot be scaled proportionally with the supply voltage. On the contrary, decrease of the gate overdrive (V_{GS}-V_{TH}) would cause a degradation of the on-state current being related to the

device switching speed. Nevertheless, constant channel voltage scaling affects the active power density that is proportional to V_{DD}^2. In this situation, the active power density increases as λ^2 contrary to the unity in the constant electric field scaling. This would drastically increase the device consumption. Holding the clock frequency constant can only slow the increase of active power density by a factor of λ. In this situation continuing scaling inevitably leads to an increased chip power density. As a consequence, the chip temperature is raised what amplifies the off-state leakage currents. This vicious circle is referred as "Power constrained scaling" and makes the validity of Moore's prediction questionable for next generations of CMOS devices.

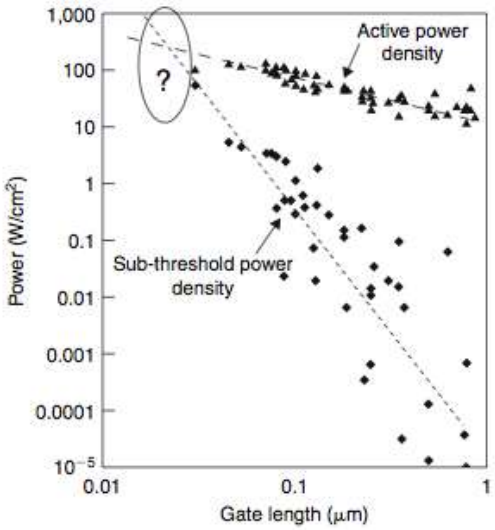


Figure 1: Active power consumption and leakage (subthreshold) power density [4].

To overcome this limitation, novel technological solutions have been successfully introduced over the last decade. Stress engineering introduced for 90nm node allowed to enhance the channel carrier mobility [5]. Problematic oxide scaling was temporarily resolved with a high-k oxide applied in 45 nm node [6]. Also a successor of planar architecture, FinFET concept was introduced for 22nm node [7], followed by a second generation introduced for 14nm node [8].

1.3 Beyond Silicon MOSFET

Beyond the traditional Si MOSFET, multiple concepts of low power devices are available. Among them, we find tunnel FET [9], ferroelectric FET [10], mechanical switch [11]. A characteristic feature of this category of devices is an ability to obtain a smaller subthreshold swing than 60mV/dec reducing thus the off-state leakages.

An alternative approach consists in replacing Si material by III-V high mobility materials. Here electrons can move from source to drain in much higher velocities than in Si MOSFET. Since the current is proportionally dependent on the carrier velocity, these materials have potential to deliver higher on-state current or in other words allow operation at a lower supply voltage. For decades, III-V technology has been successfully applied in High Electron Mobility Transistor (HEMT) and Heterojunction Bipolar Transistor (HBT) where they have shown an excellent dynamic performance and has become an inevitable part of RF applications. However, III-V MOSFET, has still not reached its predicted potential. High-quality III-V/ oxide interface, low access resistance but also an integration on Si substrate are the issues that have to be addressed before III-V materials could be implemented into CMOS circuits.

In this context is presented the thesis that you are holding in your hands. It is organized as follows:

2 Thesis organization

The thesis will guide the reader through concept (**Chapter 1**), fabrication (**Chapter 2**) and finally through electrical characterizations (**Chapter 3**) of a deeply scaled Ultra-Thin body (UTB) III-V MOSFET and FinFET fabricated at Institute of Electronics Microelectronics and Nanotechnology in Lille.

In **Chapter 1,** the theoretical concept of the deeply scaled MOSFET will be given. Specifically, in this chapter will be explained the notions such as mobility, injection velocity, MOSFET ballistic transport and why these are so important for a high-performance MOSFET operation regime. Furthermore, it will be discussed that a proper choice of architecture can diminish the leaky character of a deeply scaled MOSFET. Finally, it will be shown that despite

an early stage of III-V MOSFET development, the concept features interesting on and off-state metrics.

In the next step is presented the experimental part of the work: fabrication and characterization of Ultra-Thin body (UTB) InAs MOSFET and InAs FinFET (**Figure 2**). This work is a continuity of the first and second generation of III-V MOSFETs (**Figure 2**) previously fabricated at the Institute of Electronics Microelectronic and Nanotechnology in Lille (IEMN). Due to a high access resistance, these did not provide high on-state metrics and suffered from a bad scalability. In this situation, an update of architecture and fabrication process was vital to keep up with the technological advance of III-V MOSFET research groups. The most important change in fabrication represents the introduction of a localized Molecular Beam Epitaxy (MBE) realized in a close collaboration with our partner group Epiphy at IEMN. Regarding the architecture, Ultra-thin body (UTB) MOSFET and FinFET design were introduced. The practical part is presented in 2 chapters:

In **chapter 2** are presented building blocks of the fabrication process. In the channel-substrate section are presented epi-layers utilized for Ultra-Thin body (UTB) MOSFET and Gate-All-Around (FinFET) channel design. Description of the high-k oxide deposition is provided in the second section, the gate stack module. Formation of source and drain contacts based on a raised In(Ga)As n+ realized by localized MBE is discussed in the contact module. In the MOSFET and GAA (FinFET) fabrication modules, the reader can find a description of the devices fabrication schemes.

In **chapter 3** are discussed electrical characterizations of selected devices regrouped into 3 (**sub**)-generations of planar UTB InAs MOSFETs and 1 generation of InAs FinFET. The first (**sub**)-generation is characterized by the utilization of a single layer Al_2O_3 high-k oxide. A characteristic feature of the second (**sub**)-generation is the introduction of a bilayer high-k oxide Al_2O_3 + HfO_2. Contrary to the previous (**sub**)-generations utilizing InAs +n S/D contact module, in the third (**sub**)-generation is used InGaAs n+ S/D contact module. Alternative channel architecture based on a suspended InAs channel was used in the last reported device referred as a first FinFET generation.

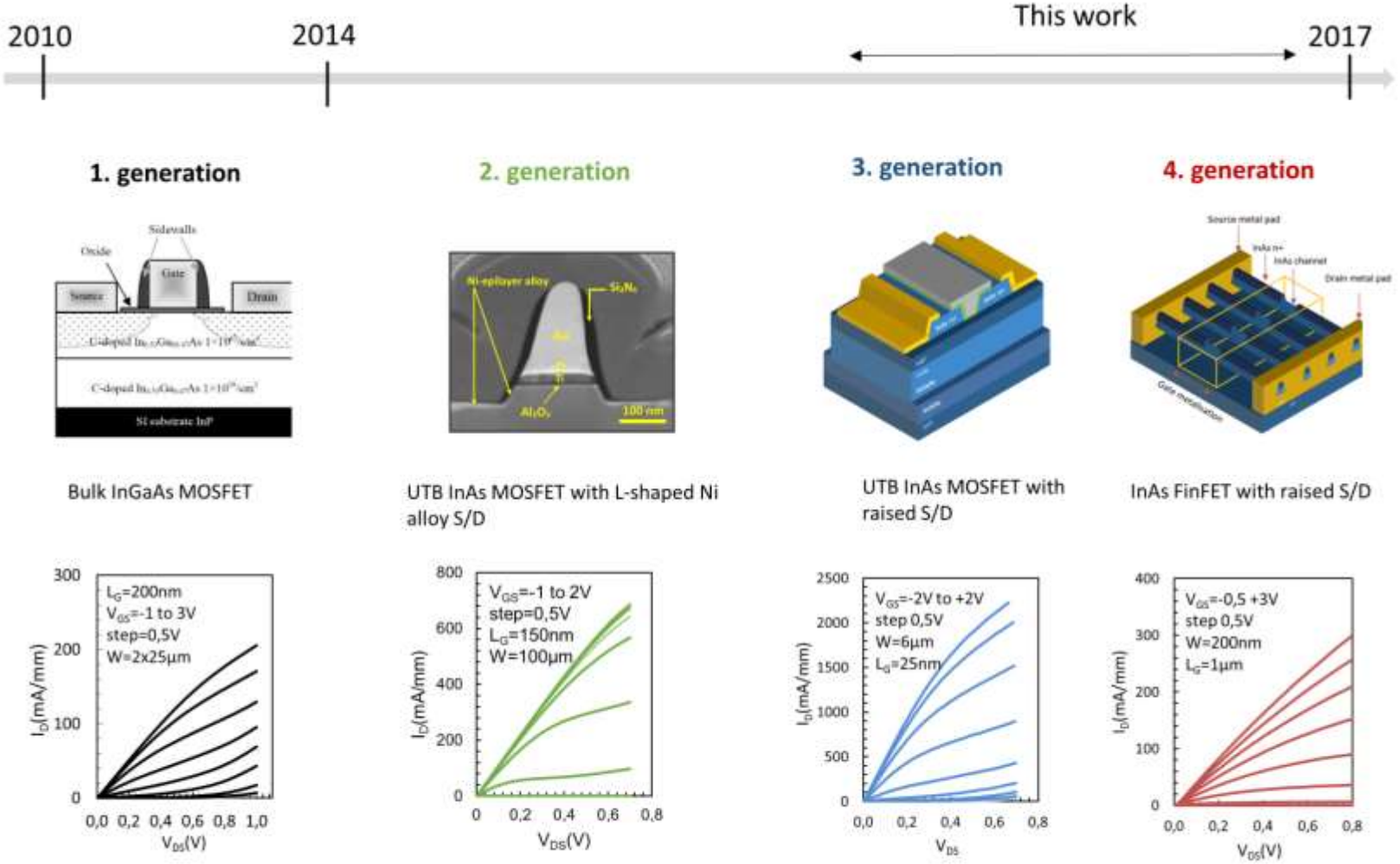


Figure 2: Evolution of III-V MOSFET at Institute of Electronics Microelectronics and Nanotechnology (IEMN) with outlined topology of devices presented in this work.

Chapter 1

1 Introduction

In this chapter, the reader can find the principal guidelines for designing a deeply scaled MOSFET. Firstly, we will explain basic notions such as mobility, carrier velocity and why these gauges are so important for high-performance MOSFETs. Furthermore, we will explain the underlying transport, command and leakage theory of a modern deeply scaled MOSFET that will be put into relation with the channel material and the channel architecture. Based on this, the reader should be capable to evaluate the advantages but also challenges of III-V MOSFET in comparison to a traditional Si MOSFET technology. Finally, the discussed theory is confronted with the current situation of III-V MOSFET. In the last section is presented a brief overview of the state of art experimental III-V MOSFETs and commercial Si MOSFETs.

2 Channel material for high-performance MOSFET

As outlined in the introduction, choice of channel material plays a crucial role in improving the n-MOSFET transport performance. Specifically, we have stated that III-V high mobility materials can deliver higher current for a given drain voltage than Silicon channel. This is enabled by a smaller electron effective mass that is inversely proportional to the carrier effective mobility. The former term reflects primarily existence of a periodical potential in a semiconductor crystal that is characterized by a specific energy dispersion diagram E(k). The role of the effective carrier mass is then to simplify the energy dispersion diagram by attributing to free carriers (electrons and holes) that occupy the conduction and valence band respectively a specific effective mass. This is quite a useful MOSFET gauge enabling to compare carrier velocities but also inversion capacitance with respect to a specific energetic level.

When the semiconductor material is biased, free carriers get into motion acquiring a drift velocity that is inversely proportional to the carrier effective mass.

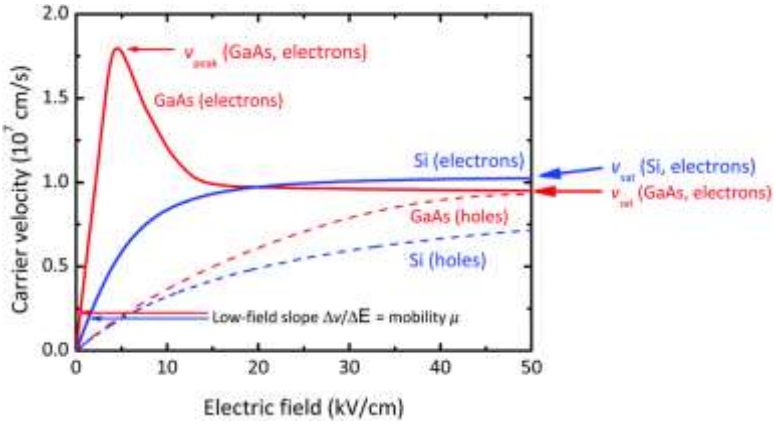


Figure 3: Velocity characteristics of electrons and holes in electric field. The low field slope of carrier velocities in GaAs is lower than the slope in Si material [12].

In **Figure 3** are illustrated GaAs and Si holes and electrons velocities dependency upon electric field. In a low field region (the region where the carrier velocity is linearly dependent upon electric field) GaAs shows a higher slope of v-E function than in Si what basically reflects a fact that light electrons can be accelerated to higher velocities compared to heavier electrons in Si material. Due to an increased carrier scattering with phonons, impurities, and crystal defects, the velocity in both materials is saturated and does not follow a linear dependency on the electric field. Here again, the GaAs attains higher values of maximum peak velocity at lower electric field than Si material. For the sake of clarity, we illustrate v-E function of merely GaAs but similar observation can be applied on the whole family of III-V materials that shows a superior electron drift and higher maximum peak velocities over Si. In this regard, we put ahead namely InAs that we choose as a channel material in this work. This exhibits an effective electron mobility of 40000 $cm^2(Vs)^{-1}$ what is almost 30 times higher than the effective electron mobility reported for Si channel (**Table 1**).

Typically, light carrier, high carrier mobility and high maximum peak velocity are underlying preconditions to reach high on-state currents. Regarding the deeply scaled MOSFET, the device current is related to the injection velocity. Here also, a low effective electron mass is an underlying criterion to obtain a high injection velocity. More on this topic will be discussed in the section explaining the MOSFET transport theory.

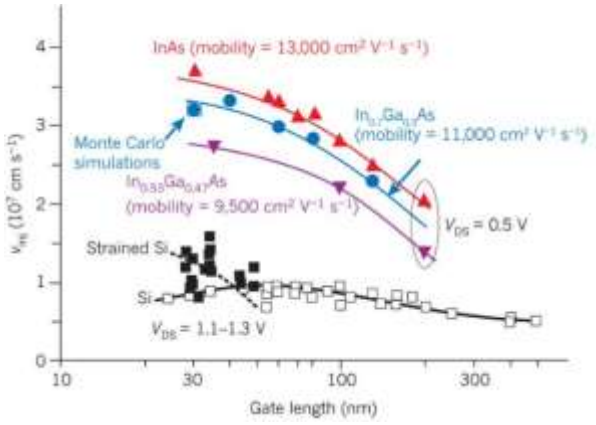


Figure 4: Experimental electron injection velocity extracted from III-V and Si FET devices. Reported mobility in strained Si is two times lower than in In(Ga)As based FETs [13].

In **Figure 4** are illustrated typical injection velocities for III-V and Si FET devices. Transport properties of integrated III-V based FET are superior to MOSFET with strained silicon channel. In particular, injection velocities in InGaAs FET device are 2 times higher than velocities obtained in Si MOSFET. It is worth to note that this was obtained with 0.5V drain voltage compare to 1.3V obtained for Si MOSFET [13].

Regarding alternative material systems providing an outstanding carrier transport it is also worth to mention the graphene channel based FET (**Table 1**) that is explored namely in RF devices [14]. Despite its supreme transport properties, graphene misses a bandgap what induces a high off-state leakage current. Several solutions have been reported [15] trying to open the band gap but none of them has demonstrated a technological readiness. In this view, Graphene is very unlikely to become a material for CMOS logical switches.

Material parameter	IV		III-V			2D
	Si	Ge	InAs	GaAs	$In_{0,53}Ga_{0,47}As$	Graphene
Electron effective mass, m_e	0,19	0,08	0,023	0,063	0,041	N/A
Hole effective mass m_h	0,49	0,33	0,41	0,082	0,45	N/A
Electron mobility ($cm^2 V^{-1}s^{-1}$)	1400	3900	40000	8500	12000	15000
Hole mobility ($cm^2 V^{-1}s^{-1}$)	450	1900	500	400	300	15000
Energy gap (eV)	1,12	0,661	0,354	1,424	0,74	N/A
Lattice constant (A)	5,431	5,658	6,06	5,65	5,8687	2,45
Dielectric constant(ε_r)	11,7	16,2	15,15	12,9	13,9	16-3,3(HF)
Thermal conductivity W cm^{-1} °C^{-1}	1,3	0,58	0,27	0,55	0,05	5

Table 1: Parameters of Si and emerging material systems for FET devices [16][17].

The main advantage of III-V systems over alternative materials is its technological maturity [18]. Today, these are applied in the modern high-performance RF circuits as a part of HBT or HEMT devices.

However, contrary to Si, materials such as InGaAs and InAs require integration on morphologically compatible substrates. Additionally, a narrow band gap InAs substrate would in MOSFET causes a high substrate leakage current. Also, it is not technologically feasible to grow a ternary compound substrate such as InGaAs. Therefore InAs and InGaAs are typically integrated on the conventional III-V substrates such as InP or GaAs [19].

Prior to the introduction of III-V materials in Very Large Scale Integrated Circuits (VLSI), several technological challenges have to be addressed. While the silicon as a channel material features inferior transport properties, it is still considered to be the best substrate material. Silicon has superior mechanical and thermal properties (Thermal conductivity of Si is 5 times higher than in InAs (**Table 1)** and most importantly, a lower price over III-V wafers. Hence, if III-V materials want to conquer VLSI market its ultimate co-integration on Si wafer is inevitable.

Also, a major disadvantage of III-V lies in absence of a quality native oxide [20]. As a result, oxide gate stacks containing III-V semiconductor are prone to a high density of interface traps. Recently introduced Atomic Layer Deposition (ALD) technology enabled to deposit quality high-K dielectrics. Thanks to this technological breakthrough, III-V materials have gained the attention of engineering community as a feasible technology for future CMOS applications.

3 Theory of deeply scaled MOSFET

In this section is presented transport and command theory of a deeply scaled MOSFET. In a classical MOSFET, a gate stack capacitor is composed of metal, oxide and channel semiconductor. In principle, the structure modulates the carrier concentration in the channel. Accordingly, we can distinguish 3 operation regimes: inversion, accumulation and depletion. For n-type MOSFET a positive gate bias will repulse holes and attract negatively charged electrons in a thin layer referred as an inversion layer serving as a conducting path between the source and drain.

3.1 Gate command

Gate stack ability to attract or repulse free carriers is characterized by a channel gate capacitance. For generations of MOSFETs with a thick oxide, the gate capacitance was equal to the insulator (oxide) capacitance. However, this does not hold for a deeply scaled oxide thickness requiring a more complex model accounting namely for the quantization effects. In **Figure 5** is outlined an idealistic equivalent gate capacitance circuit diagram of a deeply scaled III-V Quantum Well (QW or UTB) MOSFET. This is composed of an oxide capacitance (C_{ox}), a density of states capacitance C_{inv}^{DOS} and a centroid capacitance $C_{inv}^{thickness}$ [21][22]. The model does not account for process related parasitic terms such as an interface trap capacitance, oxide border trap capacitance, etc. that for a more realistic model of III-V channel MOSFET devices should not be disregarded. Considering the contribution of the abovementioned capacitances, we can write for the overall gate capacitance:

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_{inv}} = \frac{1}{C_{ox}} + \frac{1}{C_{inv}^{DOS}} + \frac{1}{C_{inv}^{thickness}} \quad (1)$$

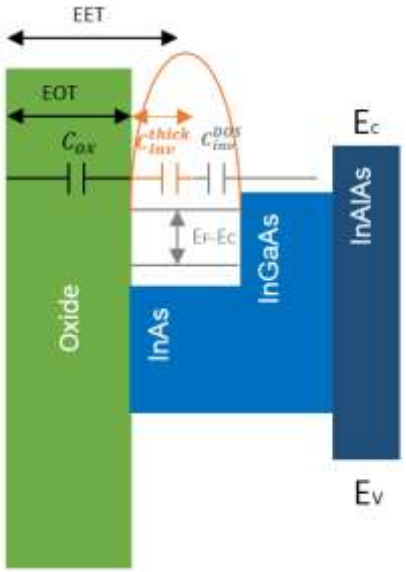


Figure 5: Equivalent gate capacitance circuit diagram of confined InAs quantum well channel. Orange line corresponds to the charge concentration with a characteristic centroid form induced by the quantization effects.

3.1.1 Oxide Capacitance (C_{ox})

The physical significance of the oxide capacitance is quite straightforward. It represents a capacitance of a standard dielectric layer that depends primarily on the oxide thickness and the oxide permittivity. Simply, thinner the oxide thickness, higher is the MOS capacitance and better is the channel electrostatic control. As a result, can be expected lower off-state current and higher on-state current. As a popular benchmark metrics is used Effective Oxide Thickness (EOT). This puts the dielectric constant and the oxide thickness in relation to SiO_2 and is expressed as:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high\ k}} t_{high\ k} \quad (2)$$

3.1.2 Inversion Capacitance (C_{inv})

For a deeply scaled oxide we observe a mismatch between the measured capacitance and the oxide capacitance. This is explained by an inversion capacitance (C_{inv}) that is wired in series with the oxide capacitance. As the oxide thickness becomes extremely thin, the weight of the inversion capacitance in the total channel gate capacitance grows while the weight of the oxide capacitance on the total capacitance is lowered. Consequently, when the oxide capacitance approaches the same order of magnitude as the inversion capacitance, the gain in electrostatic control driven by the oxide thinning is counterbalanced by a growing weight of the inversion capacitance. Accordingly, a larger value of C_{inv} is favorable for a more efficient gate command of an extremely scaled gate stack. Unlike the oxide capacitance, the physical significance of the inversion capacitance is not intuitive. It arises from an electron confinement in the inversion layer of Si MOSFETs [21] or in case of III-V MOSFET [22] from a thin quantum well confinement. In reality, the description of the effect is more complex as the quantification of states is manifested through two different effects. Each of them can be represented by a separate capacitance.

3.1.2.1 Inversion Capacitance: Density of states capacitance (C_{inv}^{DOS})

The carrier confinement in a Two-Dimensional Electron Gas (2DEG) system such as the inversion layer or a quantum well has one major bottleneck. This is a smaller density of states compared to 3D case. Filling the quantum well with carriers is accompanied by a raising Fermi level due to a finite Density of States (DOS) of each subband. Therefore, besides an energy required to create an electric field in the oxide, the creation of 2DEG will require an additional energy to raise the Fermi level. The relation between C_{inv}^{DOS} and $E_f - E_1$ is then formulated as [22]:

$$C_{inv}^{DOS} = \frac{\frac{q^2 m^*}{\pi \hbar^2}}{1 + e^{-\frac{E_f - E_1}{kT}}} \quad (3)$$

Where $\frac{E_f - E_1}{kT}$ is referred as a Fermi reduced energy (η) and can be obtained from $\eta = \ln\left(\exp^{(\frac{N_S}{N_{2D}}} - 1\right)$ and calculated with respect to the carrier concentration N_S. Next, the expression $\frac{m^*}{\pi \hbar^2}$ stands for 2D DOS and is proportional to an electron effective mass. In the following picture is plotted C_{inv}^{DOS} (**Figure 6**) as a function of carrier concentration for a low and high electron effective mass **(3)**.

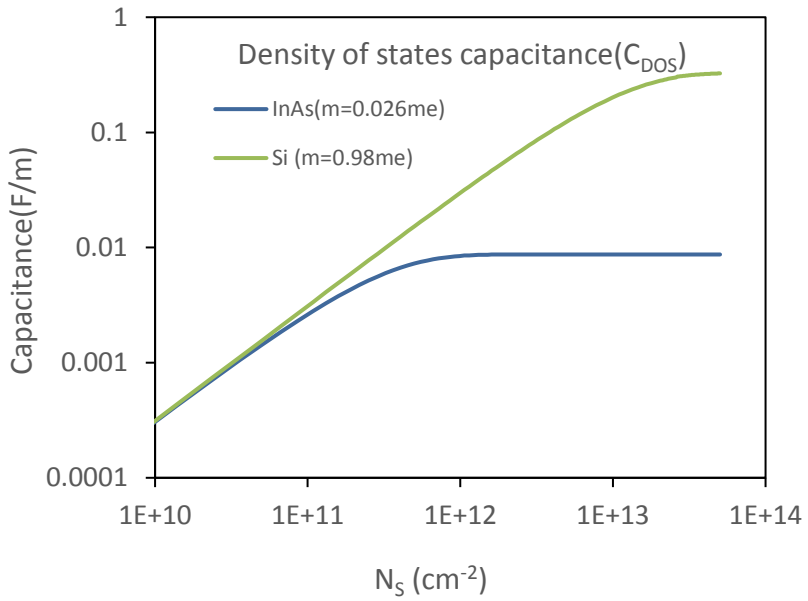


Figure 6: Calculated C_{inv}^{DOS} as a function of sheet charge density for Si and InAs electron transversal effective masses.

In either case, can be noticed that the importance of C_{inv}^{DOS} capacitance arises for a strong inversion region (high N_S) where C_{inv}^{DOS} converges towards $\frac{q^2 m^*}{\pi\hbar}$ and will be lower for a weak inversion (low N_S) where the C_{inv}^{DOS} can be expressed as $\frac{q^2 m^*}{\pi\hbar}\exp\left(\frac{E_f - E_1}{kT}\right)$. Since C_{inv}^{DOS} is proportionally dependent on the electron effective mass, III-V materials such as InAs show a lower C_{inv}^{DOS} than Si channel MOSFET. This implies that III-V channel materials will be more severely touched by the oxide scaling due to a lower C_{inv}^{DOS} compared to Si channel.

3.1.2.2 Inversion Capacitance: Centroid capacitance ($C_{inv}^{thickness}$)

The second term is a centroid capacitance $C_{inv}^{thickness}$. This originates from a non-classical carrier distribution of the inversion charge in the channel. In the inversion layer (QW channel) an average carrier concentration peak referred also as a centroid is shifted from the oxide/SC interface as illustrated in **Figure 5**. As a consequence, carriers are commanded from the metal/oxide interface from the distance EOT to which is added the distance of the centroid in respect to the oxide/semiconductor interface. This is manifested by an additional parasitic component that can be approximated for III-V MOSFET channels by $C_{inv}^{thickness} = \frac{2\varepsilon_{sc}}{t_{QW}}$ and for

Si MOSFET as $\frac{\varepsilon_{sc}}{t_{inversion}}$[21]. Where t_{QW} is a thickness of III-V MOSFET quantum well channel and $t_{inversion}$ is an average thickness of 2DEG in Si MOSFET.

Regarding the impact of the inversion capacitance on MOSFET command, we can conclude that a low effective mass will reduce the DOS being related to the density of states capacitance. The lower density of states capacitance can be understood as a more energy (i.e. voltage) required to generate the same carrier densities in the inversion layer (quantum well) as for the heavier effective mass materials such as Si. In this regard, lower inversion capacitance typical for III-V suffering from a low DOS can reduce the current density and compromise their excellent transport properties. However, MOSFET command is just one aspect of MOSFET operation. The second aspect is the MOSFET transport where III-V channel outmatches Si.

3.2 Transport theory

In a strong inversion regime, the inversion layer serves as a conduction path between the source and drain electrodes. Applied potential difference between source and drain will then generate the drain current. Its magnitude depends on the applied drain voltage. In a typical MOSFET I_D-V_{DS} characteristic, the voltage span is divided into 2 specific voltage spans. The first is referred as a linear zone. Here, the drive current follows a linear dependency on the drive voltage that is expressed as:

$$I_{ON} = \frac{W}{L}\mu C_G(V_{GS} - V_{TH})V_{DS} \quad (4)$$

Where μ stands for the carrier mobility, C_G is the gate capacitance and the W and L are the width and gate length respectively. In this region, transistor is in a so-called ohmic regime and the channel is controlled via both voltages V_{GS} and V_{DS}. Beyond a certain drain voltage level, referred as a saturation voltage, the drain current starts to saturate. It attains a floor level where the slope of the function representing the conductance G_D (variation of the drain current versus V_{DS}) goes towards 0 (ideal FET). Drain current is then modulated only by V_{GS}.

This phenomenon is called saturation and it is a typical MOSFET operation regime. Saturation voltage depends strongly on device architecture as well as on channel material choice. According to dominating mechanism of saturation, we can distinguish 3 saturation models.

3.2.1 Long channel Theory: pinch-off saturation

Increasing V_{DS} causes a strong polarization of the channel zone that is in the proximity of the drain contact. This will lead to a creation of a depletion region that leads to a narrowing of the inversion channel thickness. This is called a pinch-off saturation. The I_{on} current density is then controlled only via gate overdrive following a quadratic dependence $(V_{GS}\text{-}V_{TH})^2$. Then, the drain current can be written as:

$$I_{ON} \approx \frac{W}{2L}\mu C_G (V_{GS} - V_{TH})^2 \qquad (5)$$

The provided model is typically valid for a long gate device and starts to be inaccurate for a large V_{DS}/L_G ratio exceeding the electric field related to the carrier velocity saturation (**Figure 3**).

3.2.2 Intermediately long channel theory: drift velocity saturation

As the channel length is scaled down, while the supply voltage is kept constant a carrier drift velocity saturation may occur. For a constant V_{DS}, the electric field along the channel is inversely proportional to the channel length. Higher longitudinal electric field accelerates carriers to higher drift velocities. Since the channel length is still longer than the carriers mean free path, carriers will lose a part of their energy in interactions with the channel lattice. Carriers dissipate their energy in a form of phonon. Lower kinetic energy of the carriers is then manifested as a reduced drift velocity. When MOSFET with dominating velocity saturation mechanism is biased in the saturation region, the drain current will increase linearly with the gate voltage overdrive $(V_{GS}\text{-}V_{TH})$ as:

$$I_{ON} = WC_G(V_{GS} - V_{TH})v_{sat} \quad (6)$$

Where v_{sat} is the saturation drift velocity.

3.2.3 Deeply scaled MOSFET: ballistic and semi-ballistic transport

While for the drift velocity saturation model the drain current was affected by scattering events along the channel, in a deeply scaled MOSFET with a channel typically reduced to a few mean free path lengths, the probability of carrier collision events is greatly diminished. This is called a semi-ballistic transport and describes the reality of sub 100nm gate length MOSFET [23]. To illustrate this, we consider an ideal ballistic transport with absent channel collisions. Here the electron transition time through the channel is lower than the time necessary for a lattice-carrier interaction. Carrier will then pass through the channel keeping its kinetic energy until it is relaxed in a highly doped drain. Contrary to the drift velocity saturation model, absence of scattering events in the ballistic channel will accelerate charge to high velocities that can overpass the previously mentioned drift velocity saturation. This phenomenon is known as a velocity overshoot [24]. In such system, the saturation current is not limited by the saturation velocity but by a lowest attainable velocity along the channel. And this is the velocity at the point the electron enters the channel. Analytically this can be described with the following relation:

$$I_{ON} = WC_G(V_{GS} - V_{th})v_{average} \quad (7)$$

Where $v_{average}$ represents an average carrier velocity at the point of injection. In absence of backscattering events what is simply an ideal ballistic transport, the average velocity becomes injection velocity and can be written as:

$$v_{injection} = \sqrt{\frac{2kT}{\pi m^*}} \frac{F_{1/2}(\eta)}{F_0(\eta)} \quad (8)$$

That is explained as a multiplied thermal velocity with a portion of Fermi level integrals of zero and ½ order respectively. The expressions of Fermi integrals are calculated with respect to the

Fermi reduced energy (η) that can be obtained from N_S as already discussed in the section Density of states capacitance. The term $F_{1/2}/F_0$ describes an effect of carrier degeneracy in the channel. For a low degeneracy, the $F_{1/2}/F_0$ goes towards unity and the expression can be approximated by $v_{thermal} = \sqrt{\frac{2kT}{\pi m^*}}$.

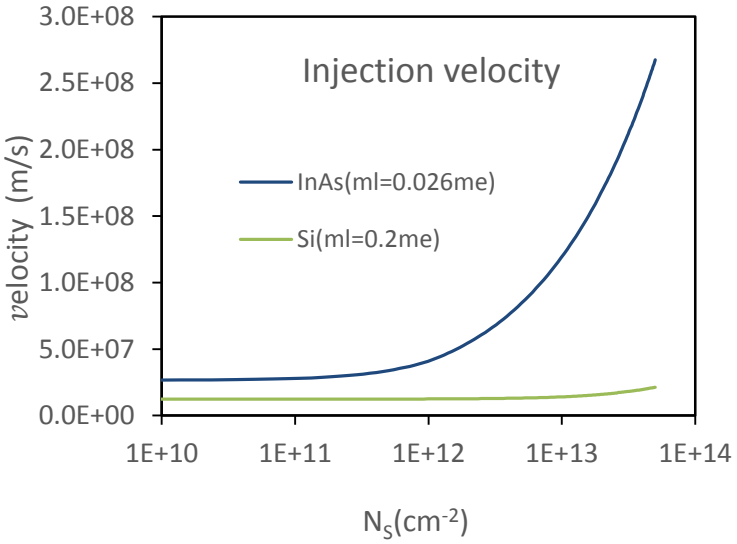


Figure 7: Calculated electron injection velocity as a function of the sheet density for InAs and Si channel.

Considering a more realistic quasi-ballistic model [25] a portion of electrons entering the channel will scatter that is modeled by introducing a backscattering (reflexion) coefficient R. Then the average injection velocity is proportional to injection velocity and backscattering term $\left(\frac{1-R}{1+R}\right)$.

$$v_{average} = v_{injection}\left(\frac{1-R}{1+R}\right) \quad (9)$$

In **Figure 7** is calculated **(8)** injection velocity for InAs and Si ballistic channel MOSFET. We can notice that for a typical carrier density an inversion layer N_s=10^{13} cm^{-2} InAs channel MOSFET exhibits one order of magnitude higher injection velocity than Si channel MOSFET.

We can conclude that relevance of future channel material system will depend on 3 aspects: injection velocity, ballistic transport, gate stack command. In two aspects III-V MOSFET obviously surpasses Si MOSFET. The lower mean free path could reduce scattering events in the channel, bringing it closer to an ideal ballistic transport in comparison to Si MOSFET. In this case, I_{ON} current depends strongly on the injection velocity, where III-V materials have a comparative advantage thanks to their lower electronic masses. To complete, we should also take into consideration the electrostatic aspect that shows to be for III-V materials a challenging issue. Their lower electron efficient mass will lower the available density of states.

4 MOSFET off-state performance

In addition to the drive on state current (I_{ON}), transport in each MOSFET device is inevitably associated with a certain level of parasitic drain current obtained at zero V_{GS} called off-state current (I_{OFF}). Level of the CMOS off-state current will define the area of its application. For instance, permitted I_{OFF} leakage current for High Performance (HP) and Ultra-Low Power (ULP) CMOS applications cannot exceed 100nA/µm and 10pA/µm respectively. In general, to reduce the device consumption while keeping high performance, the trend is to diminish the leakage current as low as possible so as to obtain as highest I_{ON}/I_{OFF} ratio as possible. Or otherwise, for a given I_{ON}/I_{OFF} ratio to obtain as low drive voltage as possible.

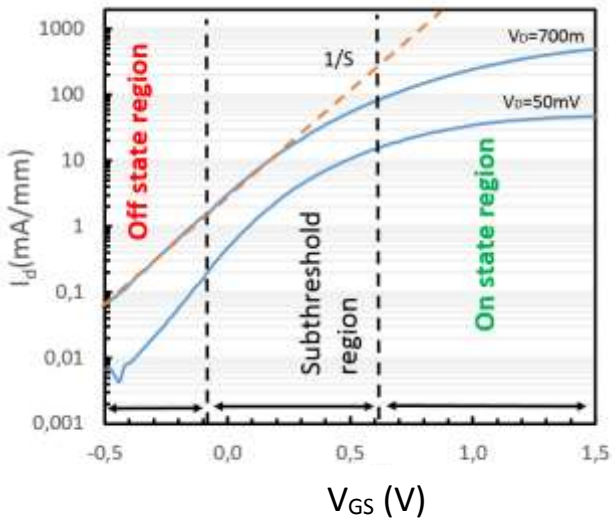


Figure 8: MOSFET transfer (sub-threshold) characteristic with outlined MOSFET operation regions.

A common method to evaluate the leakage current is to analyze a sub-threshold characteristic. This is traced drain current in a logarithmic scale versus gate-source voltage (**Figure 8**). Below the threshold voltage is situated a subthreshold region. Characteristic for this region is a linear dependency of log (I_D) on the gate voltage. Usually, we regard an inverse of log (I_d)-V_G slope referred as a subthreshold swing (SS). This is a useful leakage indicator commonly utilized in CMOS community. In a more physical sense, SS slope reflects a gate stack efficiency to transform the gate voltage variation to the channel surface potential variation. Ideally, we try to obtain as smallest value of SS as possible or otherwise as abrupt shift from on to off-state as possible.

4.1 Idealistic model

In the subthreshold region, the drain current having a thermionic character is related to the surface potential by an exponential function $I_D \sim \exp(\frac{q\varphi}{kT})$ where φ_s is the surface potential. In this region, C_{inv} governed by N_s is negligible in relation to C_{ox}. Then the surface potential variation governed by the applied gate voltage variation and given as $d\varphi_s/dV_G = \frac{C_{ox}}{C_{ox}+C_{dep}+C_{inv}}$ goes towards unity. For an ideal capacitor model this implies that the gate voltage variation in subthreshold region is entirely sensed by the surface potential variation. Then we can say that $d\varphi_s = dV_G$ and write [26]:

$$SS = \frac{dV_{GS}}{dlogI_D} = \frac{dV_{GS}}{d\varphi}\frac{d\varphi_s}{dlogI_D} = \frac{k_b T}{q}\ln(10) = 60\left(\frac{mV}{dec}\right) \quad (10)$$

This is the lowest attainable SS being imposed by the thermionic character of leakage current at temperature T=300K. It should be noted that in the abovementioned expression we do not account for parasitic effects caused for example by the fabrication or by the short channel effects [26].

4.2 Non-idealistic model

As mentioned, in the realistic model the channel command is challenged by non-desired effects that are related either to channel bandgap engineering, channel design, or to the fabrication process. Accordingly, we can distinguish several origins of leakage current that are described in the following:

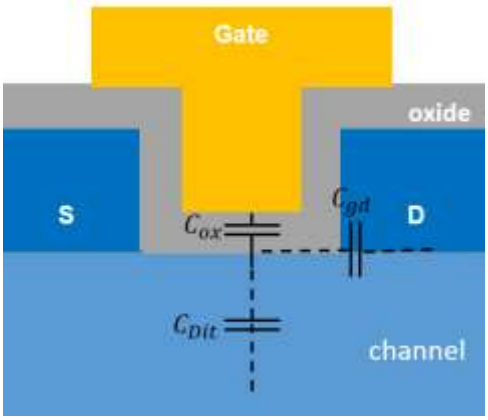


Figure 9: MOSFET capacitance model with outlined parasitic and ideal MOS capacitances

4.2.1 Interface traps

Interface traps situated between oxide and semiconductor channel cause a Fermi level pinning. Consequently, this compromises an efficient surface potential modulation being related to the carrier concentration in the channel. Electrically the impact of interface trap

density (D_{it}) can be explained as a parasitic interface trap capacitance C_{Dit} being wired in series to C_{ox} capacitance (**Figure 9**). The phenomena can be observed on the transfer characteristic as a deteriorated value of SS and as a raised level of the off-state current.

$$\mathrm{SS} = \frac{dV_{GS}}{d\varphi} * \frac{d\varphi}{dlogI_D} = 60\left(\frac{mV}{dec}\right)\left(\frac{C_{ox} + C_{Dit}}{C_{ox}}\right) = 60\left(\frac{mV}{dec}\right)\left(1 + \frac{C_{Dit}}{C_{ox}}\right) \qquad (11)$$

Impact of C_{Dit} on SS is best measured on a long gate MOSFET where the Short Channel Effects (SCE) can be disregarded. Problematics of interface traps is more fully explained in the second chapter.

4.2.2 Tunneling leakages

Beside the oxide-semiconductor traps, there is a second type of leakage. This usually does no impact the level of the subthreshold slope but is manifested as a floor leakage current. This kind of leakage current can have several origins.

4.2.2.1 Gate leakage current

Thinning the oxide to few atomic layers can trigger a high level of oxide tunneling current [27]. This is dominated by a direct tunneling mechanism. Here electrons tunnel through the oxide forbidden energy barrier directly into the channel conduction band. Its probability depends primarily on the oxide thickness, material and potential barrier height. Therefore to keep the oxide leakage current below a reasonable level while continuing scaling down the oxide thickness, it was introduced into semiconductor manufacturing high-k oxides [6] that has higher dielectric constants than silicon dioxide (SiO_2). This enables to shrink the Effective Oxide Thickness (EOT) while maintaining the gate leakage current on a reasonable level.

4.2.2.2 Band to band tunneling

In presence of a high electric field, specifically at drain side can appear a Band-to-Band Tunnel Current (BTBT). This is a consequence of a local energetic diagram bending narrowing the band gap and increasing thus the tunneling probability. This is typically observed in devices

containing material system with small bandgaps such as InAs or InSb. In MOSFET, we can distinguish two main BTBT mechanisms. The first type of BTBT occurs at the channel-drain zone where an important drain electric bending of energy diagram can induce an electron tunneling from the valence band to the conduction band. In this case, the current has a strong dependency on the drain voltage.

The second type of BTBT is typical for devices with a large gate overlap. This partly covers doped source and drain contact zones. Under the overlap a negative gate voltage causes a surface energetic band bending. Consequently, electrons tunnel from the valence band to the conduction band. In this case, generated tunnel current has a strong dependency on the gate voltage given by $V_{GD}=V_{GS}-V_{DS}$. This phenomenon is usually referred as Gate Induced Drain Leakage (GIDL) [28].

In UTB III-V MOSFET (or SOI MOSFET), the second phenomena can be amplified by the channel confinement. Holes as a product of electron-hole tunnel current pile up in the confined channel where they have no possibility to recombine on highly doped impurities. Their positive charge lowers the potential barrier that electrons in the source need to overcome to be injected into the channel. From a transport perspective, a small hole current flowing from drain to confined channel generates a large electron current flowing from source to drain (**Figure 10**). The analogy of the foregoing mechanism can be found in a bipolar junction transistor. Via a small base current is generated a great collector current. That is why this effect is commonly referred as a bipolar gain effect [29].

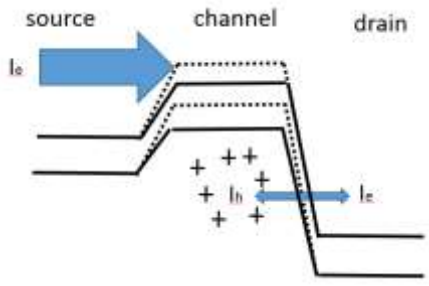


Figure 10: Illustrated leakage mechanism of MOSFET bipolar gain effect

4.2.3 Short channel electrostatic leakages

Furthermore, aggressively scaled gate length can cause large leakage current caused by an unbalanced electrostatic control of the channel. In this case, the source and drain depletion zones control an important portion of the channel producing an important screening of the carriers in the channel. This effect is more pronounced on the drain side due to an applied drain voltage. The extension of the drain depletion is represented through a gate-drain capacitance (C_{GD}) as illustrated in **Figure 9**. If the channel length is inadequately scaled down, the impact of C_{GD} with respect to C_{ox} cannot be overviewed. As a result, in addition to V_{GS} the channel control is corrupted by V_{DS}. In a more physical sense, the electrons in the source contact see a lower potential barrier in the channel, thereby allowing electrons to flow from source to drain. In an extreme case, the source and drain depletion regions merge into a single depletion region and MOSFET operation becomes strongly dependent on the drain voltage. Barrier lowering causes a threshold voltage shift and is expressed by a term called Drain induced barrier lowering (DIBL) given as:

$$DIBL = \frac{V_{th\,1} - V_{th\,2}}{V_{DS\,1} - V_{DS\,2}} \tag{12}$$

This term puts into relation a shift obtained for threshold voltage $V_{th\,1}, V_{th\,2}$ at drain bias $V_{DS\,1}, V_{DS\,2}$ respectively **(12)**. In an ideal case, this shift should be as small as possible. In reality, for an extremely scaled Si FinFET having 14-22 nm gate length, DIBL is typically around (50mV/V - 65mV/V) [8] [30]. Elimination of the Short Channel Effects (SCE) is usually realized adjusting the channel doping level, oxide or via architecture engineering.

5 Architecture consideration

In the section explaining MOSFET transport mechanisms, we have mentioned that in an extremely short channel the probability of scattering events is greatly reduced. Consequently, compared to the long channel, the short ballistic channel can transport a higher current for a given drain voltage. On the other hand, below a certain gate length we have stated that

MOSFET starts to suffer from the Short Channel Effects (SCE), manifested by a raised level of leakage current. So a question arises. How deeply can we scale MOSFET while maintaining its leakage current under control? The answer is strongly depended on the device architecture. This will set the distribution of the gate and drain electrical field across the channel and define thus the device immunity against SCE. In this regard, the channel design has to provide a balance between short and long channel effects. The synergy of the ballisticity and of a good electrostatic control may enable simultaneous supply voltage and gate length scaling without compromising the off-state current. In the following section is provided a brief overview of different architecture concepts and analyzed their suitability for future CMOS node.

5.1 Bulk MOSFET

The so called Bulk MOSFET is a traditional MOSFET design that had been employed in Si industry for almost 40 years. According to a theory of miniaturization formulated by Brews for bulk MOSFET [31] a minimal L_{MIN} is determined as a threshold gate length below which MOSFET strongly suffers from the electrostatic leakage:

$$L_{MIN} = 0.1(T_{ox}X_jX_{DEP}^2)^{\frac{1}{3}} \quad (13)$$

In the bulk technology, the subthreshold leakage control was realized through optimizing 3 parameters: source and drain contact injection depth (X_j) , channel depletion depth (X_{DEP}), and via reduction of the oxide thickness. Common approach to remedy SCE was to increase a channel doping level related to X_{DEP}. Later was introduced a halo doping [32], retrograde channel doping profile [33] helping to reduce carrier scattering on dopants impurities and lastly high-k/metal gate [6]. However, all these innovations reach their limitation at 28nm CMOS technology [34]. Regarding the bulk concept for III-V MOSFET, this was abandoned by a majority of leading research groups before attaining sub 75 nm gate lengths without providing satisfying on and off state metrics. Example of III-V bulk MOSFET is provided in reference [35]. Introduction of a confined channel provides improvement of the channel electrostatic control allowing to design smaller gate lengths.

5.2 Two dimensional MOSFET

As announced, one way to improve the MOSFET scalability is to replace the bulk channel by a thin and confined 2D channel for III-V and Si MOSFET typically referred as Ultra Thin Body channel (UTB).

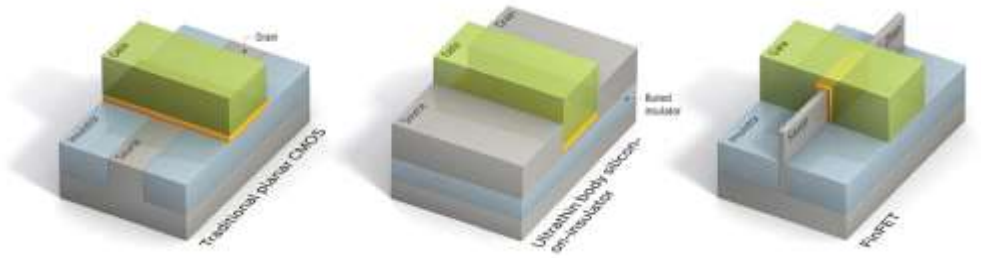


Figure 11: Transition from bulk to 2D and to 3D design. New designs converge towards a better electrostatic control of channel [36].

Confinement of carriers in a small zone situated close to the gate provides a better carrier command. The capacitance coupling between the gate and channel is enhanced, while the capacitance coupling between drain and channel is reduced. Contrary to the bulk device, where X_{dep} was adjusted by the channel doping, here the depletion region is defined to a large extent only by the channel thickness.

For confined channels was introduced a natural scaling length also known as an electrostatic scaling length. It represents an electric field extension from drain into the channel region [37] [38] and is defined as:

$$\lambda_n = \sqrt{\frac{\varepsilon_s}{n\,\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_s}\frac{t_s}{t_{ox}}\right)t_s t_{ox}} \qquad (14)$$

Where *n* is called an effective number of gates. For one gate electrode type of MOSFET such as SOI or UTB MOSFET *n* is equal to 1. The constant λ_n can be understood as a minimum achievable L_G before SCE start to be extremely severe. We recall that a higher penetration of the drain electric field into the channel is explained by a screening of the channel carriers due

to a drain electric field. In this sense, λ_n can be often find in MOSFET literature as a screening length.

$$\alpha = \frac{L_G}{2\lambda_n} \tag{15}$$

A common method to evaluate the scaling potential of a particular MOSFET technology is to put into relation λ with L_G as a ratio α **(15)** and trace the off state metrics such as SS, DIBL versus ratio α (**Figure 12**). Playing with the material parameters, oxide thickness, gate lengths can be tailored a device with specific off state parameters.

5.3 Three dimensional MOSFET

Double-Gate FET, the FinFET and Gate All Around devices belong all to MugFET (Multiple Gate MOSFET) family. Placing additional electrodes around the channel provides a more symmetrical channel electrostatic control compared to the single gate type of MOSFET (**Figure 11**). Ideal channel symmetry can be obtained by a Gate All Around (GAA) MOSFET, where the gate stack is wrapped around the channel nanowire [39]. The expression **(14)** for the double gate MOSFET is then applied with n=2, FinFET n=3 and cylindrical device n=4. Accordingly, λ_n decreases as the gate number increases. Naturally, multi-gate devices start to suffer from the short channel effects (SCE) at a shorter gate length than single-gate MOSFETs [38]

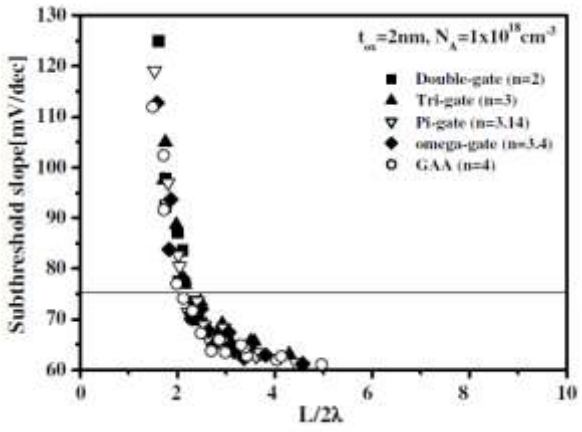


Figure 12: Example of SS versus α for different category of MOSFET designs [38]

All in all, choice of architecture for future CMOS will have a crucial effect on the device scaling potential. Here III-V MOSFET has one major bottleneck. Their higher dielectric constant compared to Si may leads to a higher scaling length **(14)**. Therefore, there is a concern that these devices would suffer from a more pronounced SCE than in Si. In this situation, only way to compete with convenient Si concept of MOSFET is to introduce as much carrier confinement as possible. This can be found in extremely thin Ultra Thin Body, FinFET or Gate-All-Around channel design.

6 Overview of state of art MOSFETs

Contrary to Si MOSFET, III-V MOSFET are still in its exploration phase and to our knowledge, their commercialization has not been demonstrated yet. However, more than a decade of engineering work has provided us with multiple concepts. In many of them, we can find multiple features that were adopted mainly from Si MOSFET and III-V HEMT or HBT. In the following is presented a brief overview of the most important and the most performing devices. They can be divided according to their mode of fabrication but also according to the channel design. A major part of the overview is focused on III-V MOSFET but also a small part is devoted to the best Si MOSFETs.

6.1 Planar UTB (2D) III-V MOSFET

A common feature of the planar UTB (2D) III-V MOSFET is an epi-layer hetero-structure typically composed of a narrow band gap In(Ga)As channel providing the carrier confinement. As announced, this has a beneficial impact on the channel control. Presented device are regrouped into 3 sub-categories differentiated according to the fabrication process such as silicide like MOSFET, MOSFET with raised S/D or III-V recessed gate HEMT.

6.1.1 UTB III-V MOSFETs with alloyed S/D contacts

Several devices whose S/D contacts were formed by an alloyed metal [40][41][42][43][44][45][46] were reported. The technique was adopted from the planar Si MOSFET where it is referred as silicide like method. Its advantage lies in the utilization of a

highly conductive silicide layer that is essentially a metal/semiconductor phase providing a low access resistance. Regarding InAs, InGaAs based silicide like process, several studies have been reported [43][45][46]. Among them, Ni shows the most promising results with a low Schottky barrier between metal and semiconductor and low Ni-III/V alloy sheet resistance [45][46][47]. Ultra-shallow contact scheme for a self-aligned MOSFET with Ni-InAs shows a metal-semiconductor sheet resistance of 97Ωμm [45]. Also, Ni-InGaAs alloy contact scheme with a low Schottky barrier in InGaAs was reported [47].

Excellent results were obtained by Takagi team [42][43] that succeeded to achieve sub 100 nm gate lengths MOSFET integrated on SOI substrate. In **Figure 13** is illustrated a silicide like process for UTB MOSFET. Device with a channel length of 20nm provides a maximum on current I_{max} of 2380mA/mm and maximum transconductance G_m of 1950mS/mm (**Figure 14**). A major bottleneck of the fabrication process is a controllability of lateral and vertical Ni diffusion depth. This can be possibly circumvented via L shape Ni epi-layer alloyed source and drain contact demonstrated at IEMN [44].

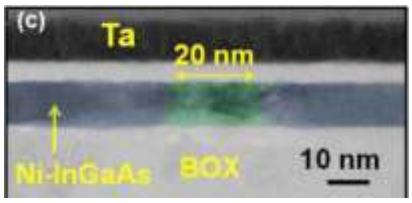


Figure 13: Cross sectional TEM images extremely scaled 20 nm L_G MOSFET with Ni alloyed S/D [42].

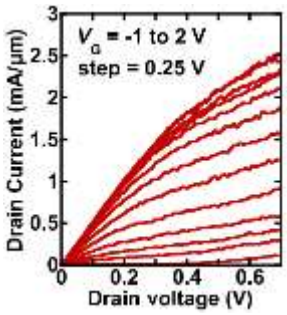


Figure 14: Output characteristic of InAs-OI n-MOSFETs with L_G of 20nm with Ni alloyed S/D [42].

6.1.2 UTB III-V recessed gate MOSFET

Excellent results were obtained also on III-V MOSFET with a HEMT-like process flow [48][49][50][51][52]. The key step is the realization of an aperture through capping layers. This is performed via precise etching control [49][53] leaving the channel ready for a gate stack deposition. In the HEMT industry, this process is often referred as a recessed gate.

In a work [50] a high precision of channel thickness down to 30 nm was reported (**Figure 15**). The device shows a subthreshold swing (SS) of 114mV/dec and transconductance (G_m) of 1420mS/mm at V_D=0.5V. The second reported MOSFET is characterized by a free wet etch recessed gate [49] (**Figure 16**). Device with a gate length of 70nm features low R_{ON} of 206Ω.µm and the maximum transconductance G_m of 2700mS/mm but SS=150mV/dec and DIBL =220mV/V at V_D=0.5V. Device with a record value of transconductance (G_M) of 3450mS/mm at V_{DS}=0.5V that outperforms to our knowledge the best InGaAs HEMT [54] was reported [51]. This work suggests that a highly doped access zone with a high electron concentration shows a better immunity against the effect of electron starvation. In this view, a better channel transport can be obtained using thicker and highly doped access zones.

In the paper [55], the recessed gate III-V MOSFET was demonstrated on SOI substrate. MOSFET with a gate length of 70nm achieves I_{max} equal to 150mA/mm for V_{GS}=0.8V, V_{DS}=0.6V with SS of 140mV/dec and DIBL of 209mV/V [55].

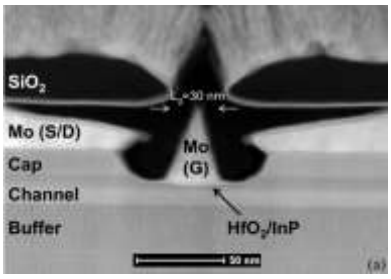


Figure 15: Cross-sectional TEM image of L_G 30nm MOSFET fabricated by recessed gate process [50].

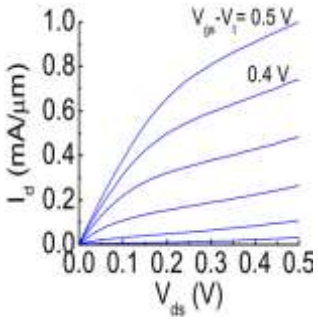


Figure 16: Output characteristic of 20nm L_G MOSFET fabricated by recessed gate process [49]

6.1.3 UTB III-V MOSFETs with selectively raised S/D

The family of devices fabricated by a S/D regrowth has shown a significant improvement over the last few years. Their advantage lays in absence of diffusion or etching steps preventing a possible damage of sensible UTB epi-layer. Also, contacts are typically

highly doped what in a self-aligned fabrication scheme, typically provides a low access resistance.

Pioneer device was demonstrated by Rodwell's group via Molecular Beam Epitaxy (MBE) regrowth of InAs n+ S/D and with a gate first process [56]**.** Another device with MBE InAs n+ S/D but with a gate last process features a low access resistance equal to 305Ωμm. Device with L_G of 40nm achieves a saturation current of 800mA/mm at V_{GS}=1.4V and a low SS of 130mV/dec at V_{DS}=0.1V and DIBL of 400mV/V [57].

The last series of devices reported by the same research group are MOSFETs with Metal Organic Chemical Vapour Epitaxy (MOCVD) selectively raised source and drain [58][59][60][61][62]. Among them, an extremely scaled 12nm gate length device with a well-balanced on and off performance was reported [63] (**Figure 17, Figure 18**). The device demonstrates a high 1800mS/mm transconductance (G_M), low subthreshold swing (SS) of 107mV/dec at V_{DS}=0.5V. The ratio I_{ON}/I_{OFF} is equal to $8.3x10^5$. Characteristic for the device is a heterojunction type of contact enabling to mitigate the tunnel leakage.

Successful integration of MOSFET with raised MOCVD S/D on SOI substrate was reported [62]. Device with a gate length of 20nm presents I_{max} of 1500mA/mm at V_{GS} 1V and a maximum peak trans-conductance (G_m) of 2000mS/mm and an access resistance (R_{access}) of 247Ω.μm, SS of 142mV/dec.

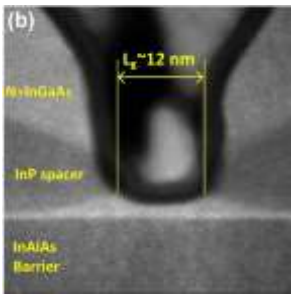


Figure 17: Cross-sectional TEM image of 12nm L_G MOSFET with MOCVD raised S/D [63]

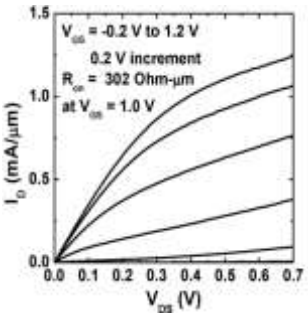


Figure 18: Output characteristic of 12nm L_G MOSFET with MOCVD raised S/D [63]

6.2 State of art III-V FinFET and GAA devices

Planar MOSFET has appeared to be also an excellent platform for studying device physics and more importantly provided ready blocks such as gate modules, contact modules

that were subsequently utilized in more complex 3D III-V devices. As discussed before, 3D channel design provides a better immunity against SCE than 2D planar design [64]. This is translated into a shorter natural scaling length allowing to design smaller gate lengths. Similarly, as we have done for planar 2D III-V MOSFET we differentiate them according to their fabrication scheme.

6.2.1 FinFET and GAA with top-down process

Alike the recess gate category of planar UTB III-V MOSFETs, a top-down category of 3D III-V channel MOSFETs reported in [65][66][67][68][69][70] is characterized by Reactive Ion Etching (RIE) channel patterning. In the study [65], Intel demonstrated the advantage of 3D InGaAs channel over 2D planar architecture. Tri-gate design of 60 nm length channel enabled to diminish SS from 160mV/dec (UTB channel) to 85mV/dec (Tri-gate channel). Next, a device with a small fin width (W_f) of 30nm and with a gate length of 60nm was demonstrated with an extremely low off-state metrics (**Figure 19, Figure 20**). The SS is equal to 77mV/dec(V_{DS}=0.5V), and the DIBL is equal to 10mV/V, while the on-state current attains 400mA/mm (I_{OFF} = 100nA/µm) and the device transconductance (G_M) is 1500mS/mm [67]. Regarding Gate-all-around (GAA) design, a sub 20nm diameter InGaAs channel was reported [69]. Device with a channel diameter (W_D) of 50nm and of a gate length of 80nm achieved a transconductance (G_M) of 730mS/mm and SS of 200mV/dec at V_D=0.5V.

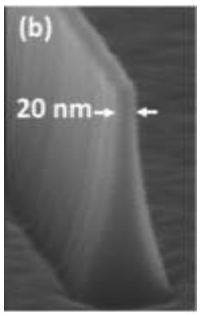


Figure 19: SEM image of stand-alone InGaAs fin patterned by RIE etching [67].

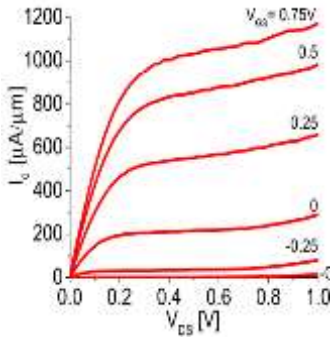


Figure 20: Output characteristic of 30nm L_G nanowire MOSFET patterned by RIE etching. The Fin FET width is equal to 22nm [67].

6.2.2 Fin FET and GAA with bottom-up process

Very much like the planar UTB III-V MOSFETs with selectively raised S/D, 3D channels patterned by bottom-up techniques are characterized by an etch-free fabrication. The first group of devices is formed via Vapor Liquid Solid Growth (VLS) technique (**Figure 21**). This uses a metal particle that guides the channel growth. The technology was successfully demonstrated in III-V MOSFET devices [71][72][73][74]. Device reported in [72] was fabricated on InP substrate with a gate length of 50 nm. It achieves a high transconductance (G_M) of 800 mS/mm (V_{DS}=1V) while the off-state metrics features SS of 100mV/dec and DIBL of 60mV/V at V_{DS}=0.5**.** High transconductance (G_M) attaining 1370mS/mm and a high saturation current of 1340mA/mm at V_{DS}=0.5V were reported for 200 nm gate length device fabricated on SOI substrate [73][74].

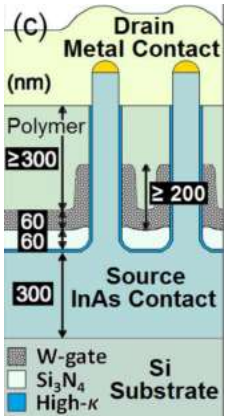


Figure 21: Schematic illustration of vertical InAs Nanowire FET [71].

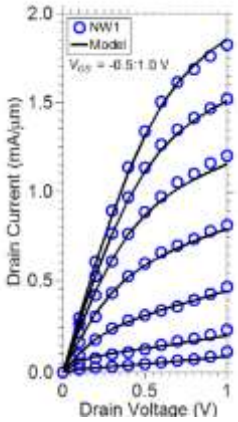


Figure 22: Output characteristics of vertical InAs nanowire with a diameter of 45nm and L_G= 200nm [71].

The second bottom-up technique is based on a selective epitaxy growth. Essentially, this consists in confining the channel growth in a hard mask aperture. In works [75][76], the technique was successfully deployed for fabrication of III-V MugFET and GAA device designs. Excellent on and off state metrics were obtained for a device with a gate length of 75nm and W_F of 90nm (**Figure 23, Figure 24**). The device shows an extremely high on-state current of 650 mA/mm (I_{OFF}=100nA/m) and an extremely high transconductance of 3000mS/mm. Equally, the device provides perfect off-state metrics with SS of 66mV/dec and DIBL of 65 mV/V [76]. Fabrication of a selectively raised MOCVD 3D channel was also achieved on Si

wafer [77]. For a fin width (W_f) of 50nm and a gate length (L_G) of 50nm, the device provides a transconductance (G_m) of 560mS/mm and I_{max}=300 mA/mm.

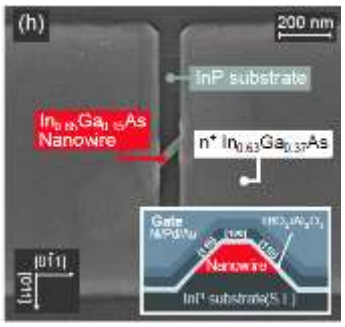


Figure 23: Top-down SEM (a) and cross section (b) illustration of InGaAs GAA MOSFET. Channel and S/D contacts are formed by MOCVD regrowth [76].

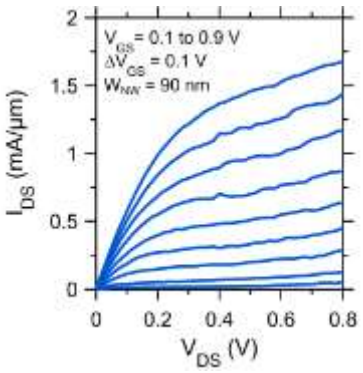


Figure 24: Output characteristics of MOSFET with L_G=75nm and W_f= 90nm. Channel and S/D contacts are formed by MOCVD regrowth [76]

6.2.3 State of art Si MOSFET

During the last 40 years, the conventional Si MOSFET has undergone a considerable technological progress. One of the most important innovation was a shift from planar to 3D design that is deployed in commercial Intel chip well-known as a 22nm and 14nm technology (**Figure 25, Figure 26**). Despite an extremely shrunk gate lengths to 22 nm, the former [30] exhibits SS of 70 mV/dec and DIBL of 50mV/V. Extracting the on-state metrics fixed for 100nA/µm (maximal I_{OFF} current required for high-performance CMOS applications) device provides a high on-state current 1260mA/mm for a drain bias of 0.8V. The oxide EOT is scaled down to 0.9nm. To reduce the access resistance (R_{ACCESS}), contacts S/D are fabricated via selective epitaxy. This allows utilizing a channel strain engineering modulating Si channel transport properties. Second generation 14 nm FinFET (**Figure 25)** provided a 15% better on-state performance than the previous technology. The on-state current defined at 100nA/um attains 1300mA/mm (**Figure 26)** while SS and DIBL are maintained at 65mV/dec and 60 mV/V respectively [8]. Similar concept but fabricated on SOI substrate was reported by IBM [7]. Also, a GAA nanowire design with extremely small diameters of 13nm was achieved for a gate length of 25nm [78]. The device shows 400 mA/mm on-state current and the SS of 85mV/dec and DIBL of 50mV/V.

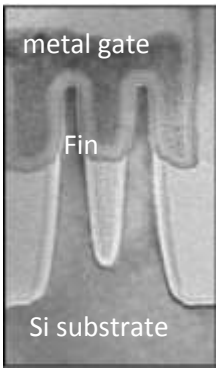


Figure 25: Cross-sectional image of Intel's 14 nm gate length FinFET [8].

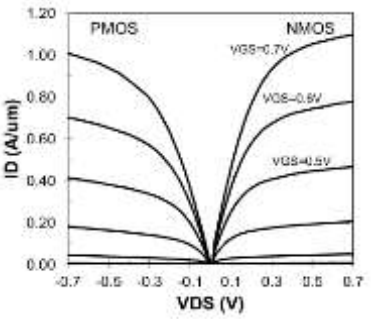


Figure 26: Intel's 14nm I-V characteristics [8].

7 Conclusion

The static on and off state performance of the reported MOSFETs are benchmarked in the (**Figure 27, Figure 28**). We can conclude that device Ultra-thin body (UTB) III-V MOSFETs architecture demonstrated an interesting on and off-state metrics. Among them stands out the work of Rodwell's group that reported outstanding series of devices with selectively raised S/D [61][63]. If we correctly normalize Si FinFET according to their fin periphery, we can say that Rodwell's planar 14-25nm III-V technology delivers comparable on state currents at I_{OFF}=100nA/µm situated between 200 and 500mA/mm what is close to Intel's Si FinFET 14nm technology. Regarding 3D topology, we put ahead namely FinFET devices demonstrated by Lund University with a high on-state current of 650 mA/mm (I_{OFF}=100nA/m) [76] outperforming 14nm Si FinFET MOSFET [8]. These early proof of concepts obtained for III-V planar and 3D MOSFETs are quite encouraging for a further research. It should be noted that to a very large extent this was achieved in conditions of university research labs disposing of limited technological, financial and human resources compared to well-equipped and well-established Si-oriented industry represented by players such as Intel, IBM or Samsung.

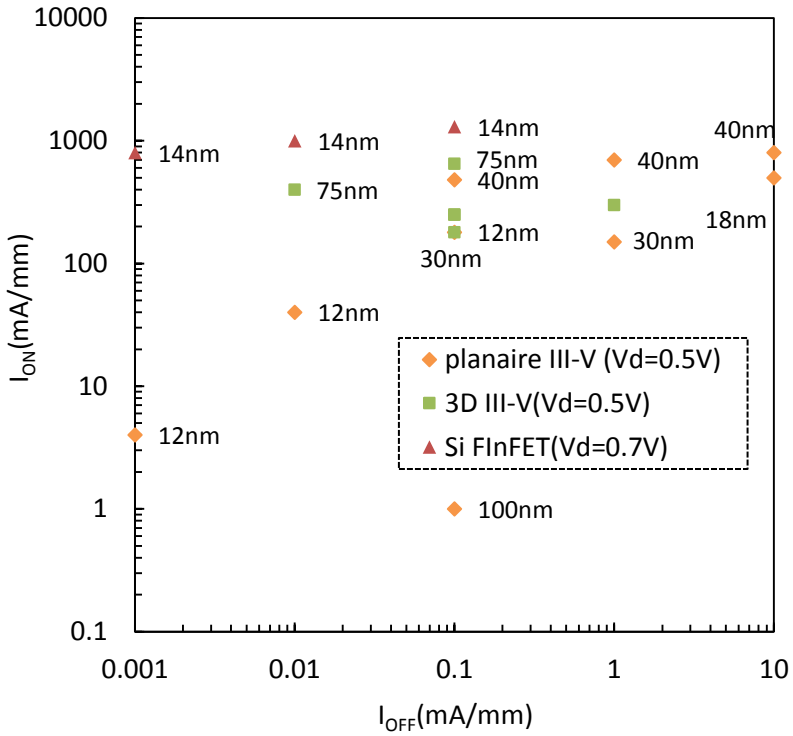


Figure 27: Comparison of I_{on} versus I_{OFF} for the state of art Si and III-V MOSFET with $L_{G<12\text{-}100nm)}$ reported in this work.

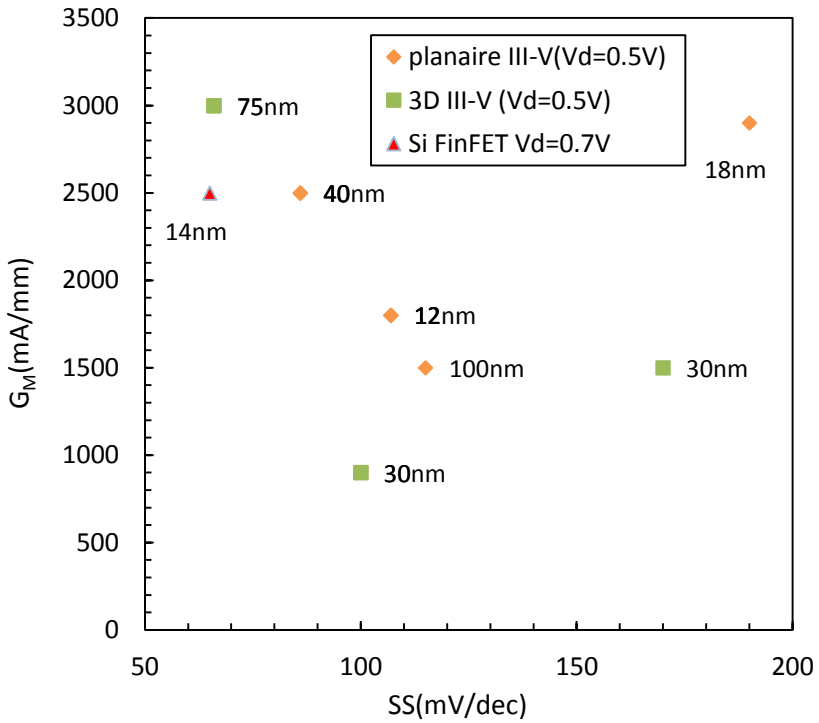


Figure 28: Comparison of G_M versus SS for $L_{G<12\text{-}100nm)}$ for state of art MOSFET reported in this work.

Chapter 2

1 Introduction

Regarding the technological maturity of III-V materials, these are still far behind Silicon that has successfully implemented technologies such as raised source and drain, high-k oxide and has already achieved integration of 3D channel. Therefore, to keep up with such a considerable advancement of Si MOSFET, the introduction of III-V materials will require new material systems and fabrication techniques. These could be inspired by the abovementioned concepts but adapted to III-V material. In this regards, one of the most problematic part that faces III-V MOSFET community is a high-quality oxide deposition on III-V that for the moment limits III-V MOSFET operation. In addition, to take advantage from III-V high conductance channel, the parasitic access resistance needs to be as low as possible. This calls for a self-aligned contact process consisting in forming the source and drain before the gate stack deposition. As a result, the alignment of the gate and contact is achieved independently of the lithography tool precision.

In this chapter, we present the development of a gate last III-V MOSFET fabrication process. This starts with presentation of principal building blocks such as substrate, gate stack and contact module. In the last two sections, the modules are assembled together to form UTB 2D and GAA (or FinFET) 3D III-V channel MOSFET.

2 Channel-substrate module

To date, Silicon is still considered as the most convenient substrate for the CMOS applications. The major reasons are its abundance compared to III-V materials, supreme mechanical properties but also its compatibility with already established VLSI fabrication processes. Therefore, the trend is to integrate III-V material on Si substrate. However, the difference in crystalline structure between Si and III-V may cause a lower quality of integrated

III-V channel. The main reasons are an important difference in thermal coefficients, a high lattice mismatch and also a difference in polarity, leading to the creation of material defects. So as to accommodate the difference in lattice mismatch, several solutions have been reported such as Aspect Ratio Trapping where the dislocations are blocked utilizing selective area epitaxy in apertures of SiO_2 [79]. Another solution consists in progressive stress attenuation by introducing a thick buffer layer also referred as a metamorphic layer [80], direct III-V growth on Silicon [81], or reporting III-V channel from native III-V substrate to Silicon substrate by oxide-oxide bonding known as III-V On Insulator (III-V-O-I) [82] etc. This topic is intensively studied by our partner LETI laboratory that has successfully achieved integration of InGaAs on Silicon substrate. The ultimate goal of our work was to implement their epi-layer for our MOSFET fabrication process. However, at the beginning of this work, a high-quality III-V on Si had not been ready yet. As a temporary solution enabling to develop the device fabrication module was decided to start with a high-quality III-V epi-layers on III-V substrate.

However, integration of InAs channel on III-V wafer is not trivial either. In fact, the common insulating substrates used in III-V technology exhibits a lattice mismatch with InAs. For instance, the lattice mismatch between InAs and InP is 3.2% and between GaAs is 7%. Therefore, it is mandatory to ensure that the experimental InAs channel MOSFET is built on a high-quality epi-layer with a low density of structural defaults. If not, the damaged channel can raise the level of the leakage current but also corrupt the high mobilities of III-V channel. Growth of InAs material on lattice-mismatched III-V substrates was done by Epiphy group at IEMN that has successfully developed 2D InAs epi-layer and 3D InAs nanostructures. These serve as starting substrates in the fabrication process of Ultra Thin Body (UTB) InAs MOSFET (**Figure 29**) and GAA (or FinFET) InAs respectively (**Figure 30**).

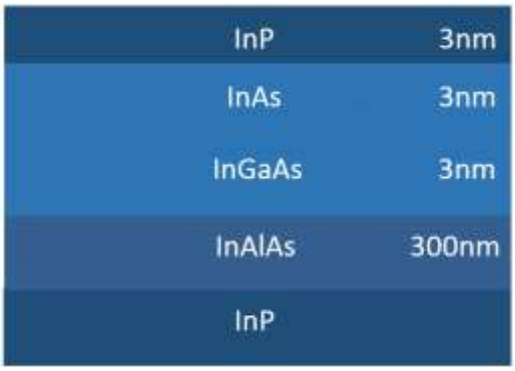


Figure 29: High mobility 2D InAs channel integrated on a lattice mismatched InP substrate.

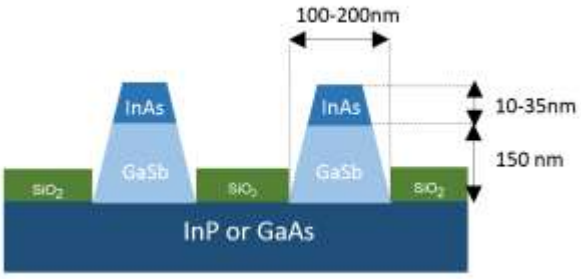


Figure 30: High mobility InAs 3D nanowire integrated on a lattice mismatched InP substrate.

2.1 Ultra Thin Body (UTB) 2D III-V channel

Confined InAs channel was firstly deployed in HEMT devices where it helped to boost the mobilities of InGaAs pseudomorphic channels grown on a lattice mismatched InP with InAlAs buffer [83][84]. Placing a narrow bandgap material in the center of the channel shifted the carriers from InGaAs/InAlAs interface into confined InAs layer where it can take advantage of a higher effective electron mobility. The concept of composite channel InAs/InGaAs with InAlAs buffer grown on InP substrate was later transferred to III-V UTB MOSFET and is also utilized in this work. Contrary to SOI MOSFET where the channel confinement is obtained by placing oxide layers on the top and bottom side of the channel, in 2D UTB composite channel (InAs/InGaAs), the confinement is realized placing a high bandgap semiconductor such as InAlAs below the channel. Since InAs exhibits a large conduction band gap offset (CBO) with respect to InAlAs (0.9eV), this leads to a carrier confinement in InAs quantum well. Moreover, to avoid a strong Fermi-level pinning between the oxide and InAs channel, is introduced a barrier layer InP placed between the InAs channel and the oxide. Carriers are shifted from the oxide/III-V interface which helps to diminish the electron-traps interactions and prevents a deterioration of InAs electron mobility. This architecture is referred as a buried channel MOSFET. Since InAs is grown on lattice-mismatched InP substrate, the InAs layer is strained. Above a critical thickness, the elastic energy is released which could cause the formation of structural defaults that can considerably deteriorate MOSFET transport properties. For the 2D InAs epi-layer systems that were developed and fabricated in our laboratory, the maximal thickness that has to be respected is 3nm.

On the other hand, InAs channel thinning leads to a raised level of the sub conduction energy band. Reduced conduction band offset between the channel subband conduction level and the buffer (barrier) conduction level induces in a physical sense an electron-wave function penetration into InAlAs. This leads to parallel conduction paths through the semi-insulating InAlAs barrier. Another negative effect of the raised sub-conduction band is a lower attainable carrier density in the channel which limits the device on-state performance.

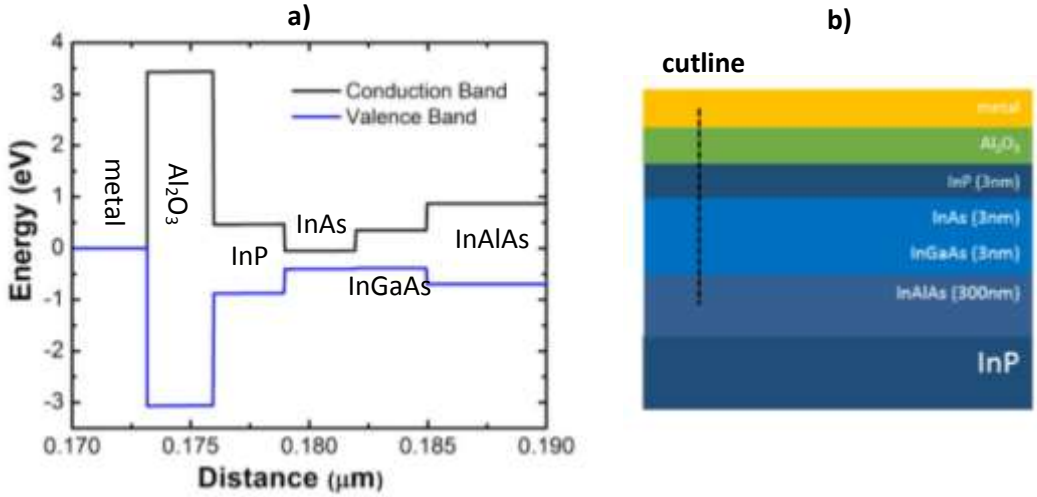


Figure 31: Energy band gap diagram (a) traced across the gate stack and channel heterojunction of the UTB InAs MOSFET (b).

2.2 Gate All Around (GAA) or FinFET 3D III-V channel

Due to the abovementioned limitations of 2D UTB InAs channel, we have attempted to introduce a 3D InAs channel that provides a better electrostatic control without lowering the device on-state current. From the available fabrication schemes utilized for patterning 3D III-V channel was reported MOCVD InAs localized selective regrowth of 3D nanostructures characterized by a defect-free epitaxy on Si substrate [85]. In our laboratory, the selective growth of III-V was studied by Epiphy group that developed MBE selective epitaxy of 3D InAs/GaSb nanoribbons grown on a lattice mismatched GaAs substrate. The selectivity was achieved by forming an extremely thin InAs 10-30nm channel on GaSb in SiO_2 hard mask apertures. The role of the GaSb intermediate layer is to attenuate the high lattice mismatch between InAs channel and InP or GaAs substrate but also to provide a supporting (sacrificial) layer that is selectively removed prior to the oxide deposition. Optimizing the growth

condition they have achieved relaxed and high-quality continuous InAs/GaSb nanoribbons grown on GaAs substrate.

3 Gate stack module

High-k oxide integration on III-V channel is not a trivial issue. Contrary to Si channel, III-V materials have one major drawback, they do not have a high-quality native oxide. As a consequence, the interface between the oxide and the III-V channel is prone to a high density of interface traps (D_{it}). This causes a channel Fermi level pinning preventing an optimal channel conduction band bending. As a result, the transition from depletion to inversion region and vice versa requires a higher gate voltage sweep. From MOSFET perspective, this corresponds to a lower I_{ON}/I_{OFF} ratio, higher consumption, etc. Therefore, the level of defects should be as low as possible. To do so, the formation of a high-quality oxide on III-V is usually accompanied by a passivation technique. In the following section is described the oxide deposition and employed passivation technique utilized for reported MOSFETs process. Lastly, is investigated the impact of MOSFET process related contamination on the MOSCAPs capacitance response.

3.1 ALD deposition

Regarding the oxide deposition techniques for III-V material, Atomic Layer Deposition (ALD) is presently the most reported. The technique was transferred to III-V from the Silicon industry where it enabled to continue the gate capacitance scaling by introducing an extremely scaled dielectric oxide (high-k). In ALD tool, the oxide layer is formed with a high precision which is a key criterion for obtainment of an extremely thin, conform and a large area uniform oxide layers.

In essence, the technique is similar to Chemical Vapour Deposition (CVD), except a high deposition precision that is achieved in ALD by separating the precursor's injection. The reaction that forms one monolayer (cycle) consists of two sequences where each contains a precursor and purge pulse. The former introduces the precursor species that react with the sample surface. Non-reacted precursors species are then evacuated during the purge step. The formation of one monolayer (cycle) is terminated by introducing a second precursor that

reacts with the first precursor (**Figure 32**). The overall thickness of the deposited oxide can be controlled by adjusting the number of the cycles. In this dissertation, we utilize aluminium and hafnium high-k oxides (Al_2O_3 and HfO_2 respectively).

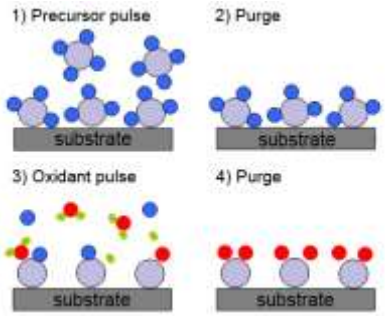


Figure 32: Schematic illustration of the Atomic Layer Deposition (ALD) process.

The former Al_2O_3 is deposited by altering a metallic precursor Trimethyl Aluminium (TMA) that reacts sequentially with an oxidizing precursor H_2O. Residual elements of the reactions are eliminated by nitrogen purges.

The later HfO_2 is deposited using tetrakis-dimethyl-amido-hafnium (TDMAH) that reacts sequentially with the oxidizing precursor H_2O. Residual elements of the reactions are eliminated by Nitrogen purges.

3.2 Oxide defects

In reality, a certain level of defects characterizes the oxide deposition. These are mainly responsible for reduced device efficiency, increasing variability etc. Usually, we distinguish four types of defects that in regards to their position are further divided into two categories. The first category of defects is situated in the oxide volume. Among these are classified fixed charges created during the oxide growth, oxide trapped charges created by carrier injection upon a strongly polarized gate electrode and oxide mobile charges associated with ionic impurities.

Among the bulk defaults are also classed the oxide border traps. These are placed close to the semiconductor oxide interface from where they can interact with the channel carriers.

The most intrusive effect on the device operation has defects lying directly on the semiconductor/oxide interface. These originate from low-quality native oxides typical for III-V materials. Oxide/III-V interfaces are then characterized by unsatisfied dangling bonds and metallic bonds having energy levels lying in the band gap energy. The Fermi level pinning prevents an efficient gate command. So as to quantify the effect of interface traps, it was introduced a Density of interface traps (D_{it}) metrics that represents a quantity of surface interface trap charge expressed in $(eV)^{-1}cm^{-2}$. Multiple of D_{it} and elemental charge q gives an interface capacitance $C_{it}=qD_{it}$ that will be later used in D_{it} extraction models.

3.3 Passivation technique

A great effort was dedicated to resolve the issue of excessively high density of interface states at oxide/III-V interface by studying multiple passivation techniques. These are classified according to the phase of the passivating agent that can be either liquid (chemical) or plasma.

For the former, sulfur ammonium $(NH_4)_2S$ [86] and hydrogen ammonium solutions $(NH_4)OH$ [87] are the most popular species. These are applied before the ALD oxide deposition and their function is to passivate III-V surface dangling bonds. The passivation step is generally preceded by a stripping of the low-quality III-V native oxide realized either in HF [88] or in a low concentrated HCl [89] solutions. Also starting the ALD deposition by a series of TMA precursor pulses was found to be an efficient method for removal of the native oxide [90]. Second passivation approach is to utilize the plasma treatment prior to the oxide deposition. Among these, we cite hydrogen H_2 [91].

Lastly, the passivation of interface defaults may be also performed after the oxide deposition. In the work [92], plasma O_2 is applied after the Al_2O_3 deposition. Oxygen diffusion through the deposited oxide results in a formation of GeOx interlayer lying on the oxide/semiconductor interface that is supposed to reduce the density of interface states and thus improve the MOSCAP capacitance response.

At IEMN, a similar concept was successfully demonstrated for Al_2O_3 on InP and InGaAs material by Alain Bruno Fadjie and Yoann Lechaux [93] utilizing (RF) oxygen plasma coupled with ALD chamber. They proposed a hypothesis that the oxygen plasma creates an interlayer at Al_2O_3/III-V interface preventing the interface re-oxidation. The interface barrier limits diffusion of oxygen species from the oxide into the oxide/semiconductor interface that usually

occurs after the Post-Deposition Annealing (PDA). PDA is necessary to reduce the bulk charge. In **Figure 33** are measured capacitance plotted against the voltage-capacitance without (**Figure 33a**) and with (**Figure 33b**) exposure to plasma O_2 on Al_2O_3/InP MOSCAP (**Figure 36**). Application of the plasma O_2 yields an improved capacitance response. Specifically, it was observed a lower dispersion in accumulation region (V_{GS} between 1V and 3V) as well as a higher dC/dV ratio in a weak depletion region for the entire spectrum of C-V curves. This points to a lowered density of interface states. With optimized plasma exposure parameters D_{it} is of (1-3) x 10^{11} $eV^{-1}cm^{-2}$(extracted by conductance method).

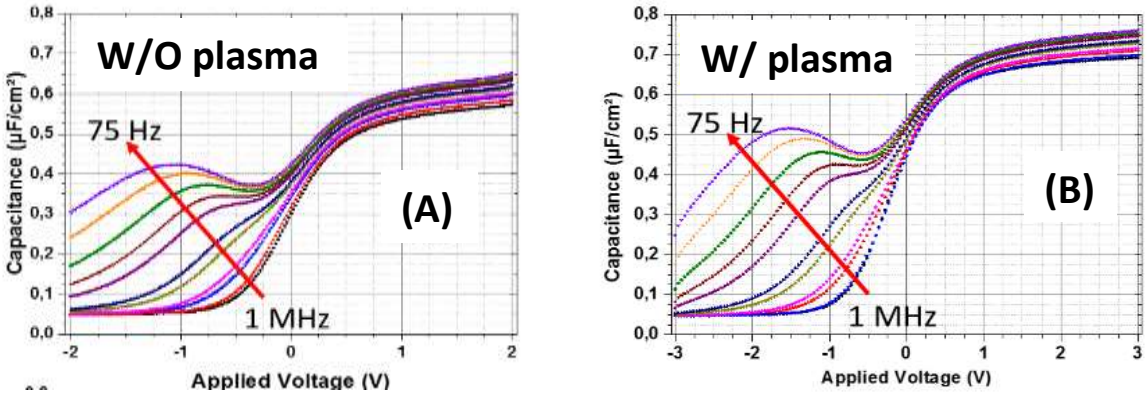


Figure 33: Frequency dispersion of C-V curves measured in frequency range from 75Hz to 1MHz on Al_2O_3/InP MOSCAP without **(a)** and with **(b)** O_2 plasma. Total Al_2O_3 thickness is 8nm (courtesy of Alain Bruno Fadjie)

3.4 Extraction of D_{it}

The extraction of D_{it} is usually realized by means of MOSCAPS capacitance-voltage (C-V) measurement. This consists in applying a direct current (DC) to which is superposed an alternating current (AC) and measuring the circuit impedance. Extraction of D_{it} is then performed applying a specific model's method.

3.4.1 HF-LF method

The principle is based on an assumption that the interface traps cannot follow a signal frequency that is higher than the 1/τ traps time response. Consequently, the contribution of

the interface traps capacitance can be disregarded and a model of high-frequency overall capacitance model **(Figure 34b)** (C_{HF}) can be expressed as:

$$\frac{1}{C_{HF}} = \frac{1}{C_{OX}} + \frac{1}{C_S} \tag{16}$$

Where the C_S is the semiconductor capacitance and C_{OX} is the oxide capacitance. On the contrary, when the applied signal is lower than 1/(carrier lifetime), corresponding to a quasi-static signal, interface traps can follow the applied signal and the model of an overall low-frequency capacitance (**Figure 34a)** becomes (C_{LF}):

$$\frac{1}{C_{LF}} = \frac{1}{C_{OX}} + \frac{1}{C_{it} + C_S} \tag{17}$$

Plotting the capacitance versus voltage, in both cases (**Figure 33**), is observed a distortion of the low-frequency capacitance curve with respect to a high-frequency curve. This phenomenon is referred in literature as a stretch out effect and is assigned to the interface trap response sensed by the low-frequency signal **(17)**. Rearranging the abovementioned terms **(16)**, **(17)** and putting $C_{it}=qD_{it}$, we can calculate D_{it} as:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{LF}/C_{ox}}{1 - C_{LF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1 - C_{HF}/C_{ox}}\right) \tag{18}$$

3.4.2 Conductance method

Beside the capacitance model of the interface charge (C_{it}), the interface traps can be modeled also as a R-C dipole. Indeed, the traps at the oxide semiconductor are characterized by a capturing and emission of carriers that is in principle a loss mechanism expressed by a resistance R_{it}. Expressing the model (**Figure 35a**) by parallel elements G_p and R_p (**Figure 35b**) we can approximate the peak of D_{it} (ω) obtained from the angular dispersion diagram G_p/ω as:

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad (19)$$

By a further simplification of (**Figure 35b**), we obtain a measurement circuit (**Figure 35c**) from which is extracted the parallel transconductance G_p/ω as:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (20)$$

Where G_m and C_m are the measured transconductance and capacitance respectively, ω is the angular frequency.

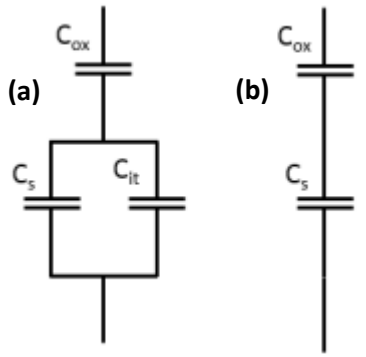


Figure 34: Equivalent circuits models for LF (**a**) and HF (**b**) signals. (HF-LF method)

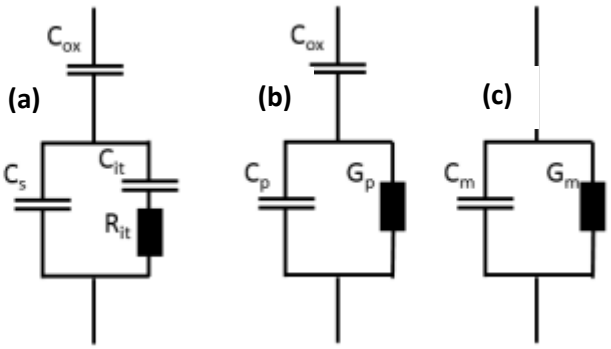


Figure 35: Equivalent circuit model for conductance method (**a**). Simplified circuit (**b**) of equivalent circuit (**a**) and measurement circuit (**c**).

3.5 Effect of MOSFET process related contamination

Fabrication of the MOSFET gate stack reported in this work differs from the originally developed high-k MOSCAPs process (**Figure 33**) developed by Alain Bruno Fadjie and Yoann Lechaux [93]. Initially, this was designated for a gate first fabrication process where the process starts with the gate stack deposition. However, in this dissertation, the MOSFET gate stacks modules are fabricated after the source and drain contacts formation what is referred as a gate last process. This means that, prior to the oxide deposition, the InP epi-layer surface comes into contact with different chemistries that may pollute the surface and thus

undesirably alter the MOSFET electrical response. Namely, this concerns HSQ (Hydrogen Silsesquioxane resist) dummy gate process, thermal annealing in MBE chamber etc. Effect of selected device fabrication treatments was simulated on the following MOSCAPs samples.

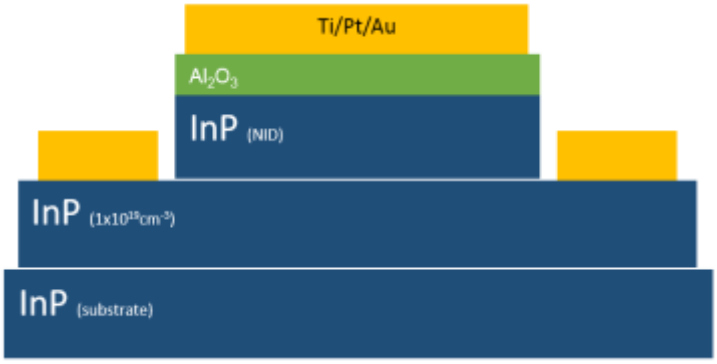


Figure 36: Schematic illustration of the MOSCAP design.

3.5.1 MOSCAP fabrication process

The fabrication process starts with Molecular beam epitaxy (MBE). On InP substrate (001) is grown 300nm highly Si-doped (N^+=1x$10^{19}$$cm^{-3}$) InP providing an ohmic contact and 300nm non-intentionally doped (NID) InP top layer. The epi-layer organic impurities were wiped out in acetone and isopropanol bath. Subsequently, the samples were exposed to the following chemistries:

Sample A: BOE 5 minutes + $(NH_4)_2S$ 10% 10 minutes

Sample B: HSQ process + 5 minutes BOE + 1 minute HCl 10% + 10 minutes $(NH_4)_2S$ 10%

Sample C: HSQ process + thermal annealing (70 minutes 470°C in RTA furnace) + 5 minutes BOE + 1 minute HCl 10% + 10 minutes $(NH_4)_2S$ 10%

Selected treatments contain similar chemistries utilized in the fabrication of the MOSFET gate stack module (More details about the role of each treatment can be found in the MOSFET fabrication module) such as HCl for the native oxide dissolution, $(NH_4)_2S$ for the surface

passivation, BOE (**SAMPLE A**) utilized for elimination of the HSQ dummy gate (**SAMPLE B**), and thermal annealing simulating conditions of In(Ga)As n+ S/D contact regrowth in MBE chamber (**SAMPLE C**). Since the treatments were performed ex-situ, the samples were kept in the IPA bath and dried by Nitrogen until their insertion into the ALD chamber. The oxide deposition starts with 2nm of Al_2O_3 that is formed by a sequence reaction of the organometallic precursor Trimethyl Aluminium (TMA) and the oxidizing agent H_2O, followed by applying in situ 0_2 plasma in Argon atmosphere. The deposition process is completed by adding 2nm of Al_2O_3. Stabilization of oxide is achieved by annealing samples in RTA furnace at 600°C (PDA) in N_2H_2 atmosphere. The gate stack is completed by formation of circular electrodes realized by a selective evaporation of Ni/Au. The highly doped InP layer providing N-type ohmic contact was accessed by carrying out a wet etch of the oxide and InP NiD layer followed by evaporation of Ti/Pt/Au electrode. The process of MOSCAP fabrication was terminated by annealing samples at 350°C in RTA furnace under N_2H_2 forming gas. Illustration of the completed MOSCAP is provided in **Figure 36**.

Effect of BOE treatment: SAMPLE A

The first studied sample contains BOE treatment that is in the MOSFET fabrication utilized for selective removal of HSQ dummy gate. The results of electrical C-V measurements are plotted in **Figure 37(a).**

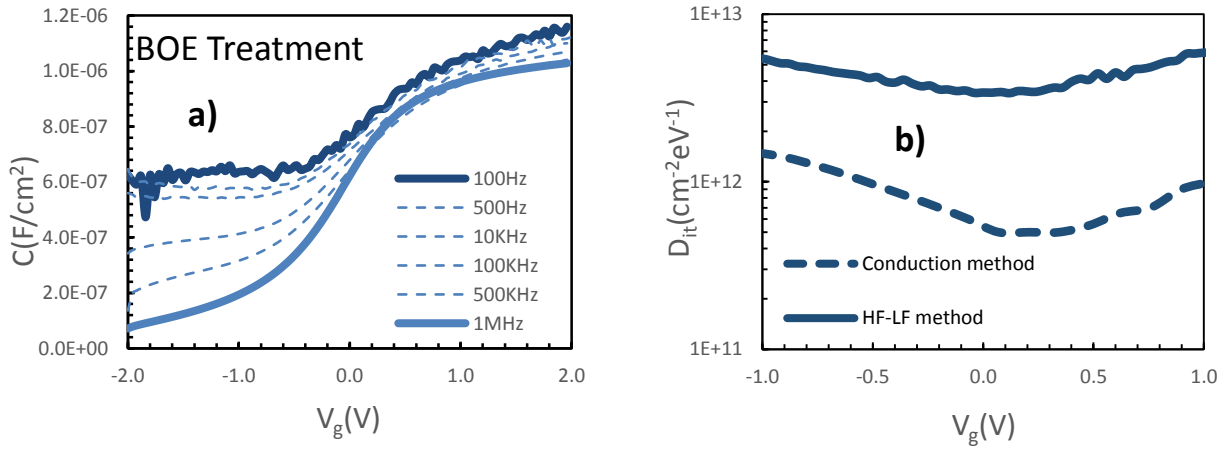


Figure 37: (**Sample A**) C-V frequency dispersion curves. Measured frequency ranges between 100Hz and 1MHz **(a)** and D_{it} versus voltage extracted by conductance and HF-LF methods (**b**)

From the low frequency (LF=100Hz) curve (**Figure 37a**) is determined the peak value of capacitance that attains $1.13x10^{-6}$ F/cm^2. This is lower than expected theoretical $C_{OX}=1.44x10^{-6}$F/cm^2 calculated with ε_r (Al_2O_3) = 6.5. (The relative permittivity of Al_2O_3 was determined in a separate work [94] realized at IEMN by Yoann Lechaux. Extrapolating C_{MAX} measured for different MOSCAP's Al_2O_3 oxide thickness is extracted Al_2O_3 relative permittivity.) The difference can be explained by an inversion capacitance C_{inv}^{DOS} whose effect cannot be disregarded in MOSCAPs containing an extremely thin oxide and a low effective mass semiconductor. For InP layer C_{inv}^{DOS} is equal to $5{,}35x10^{-6}$F/cm^2. Furthermore, the shift between the high frequency (HF=1MHz) and LF curves indicates a presence of the interface and the oxide border traps. In the accumulation region the ratio between HF and LF figure is around 1.12. Sweeping the voltage from inversion to depletion region goes along with a reduction of slope (dC/dV) referred as a "stretch out" effect that is assigned to the interface traps response. In the inversion region the HF curve does not present the capacitance response what is due to a large hole generation time with respect to 1/signal frequency.
Using HF-LF method, extraction from capacitance gives a minimum D_{it} that is equal to $4x10^{12}$(eV)$^{-1}$cm^{-2} (**Figure 37b**). This is higher than D_{it} of $5x10^{11}$(eV)$^{-1}$cm^{-2} obtained by the conductance method (**Figure 37b**). The measured mismatch between the two methods is likewise due to a lack of HF-LF precision attributed to a high border traps density.

We can conclude that MOSCAP treated with BOE (**SAMPLE A**) presents minimum D_{it} $5x10^{11}$eV^{-1}cm^{-2} that is in the same order of magnitude as MOSCAPs utilizing the original gate first recipe (D_{it} of 1 – $3x10^{11}$eV^{-1}cm^{-2}).

Effect of HSQ deposition and effect of thermal annealing: SAMPLE B, C

Effect of HSQ process was investigated on samples B and C. This includes Hexamethyldisiloxane (HMDS) deposition, surface dehydration and finally spin coating of Hydrogen silsesquioxane resist (HSQ) utilized as a dummy gate. This was followed by BOE treatment to remove unexposed HSQ and then by HCl to eliminate InP native oxide. The surface treatment is finished by applying $(NH_4)_2S$ as a surface passivation. For the **sample C**, in addition to the described HSQ process is applied 70 minutes thermal annealing at 470°C in RTA furnace that should simulate conditions in MBE chamber during the In(Ga)As n+ contact epitaxy. The choice was motivated by a work [95] where was discovered that 1 hour annealing

of InGaAs at 500°C surface covered by SiOx deteriorates the MOSFET capacitance response. The C-V measurements are presented in **Figure 38** and **Figure 39** respectively.

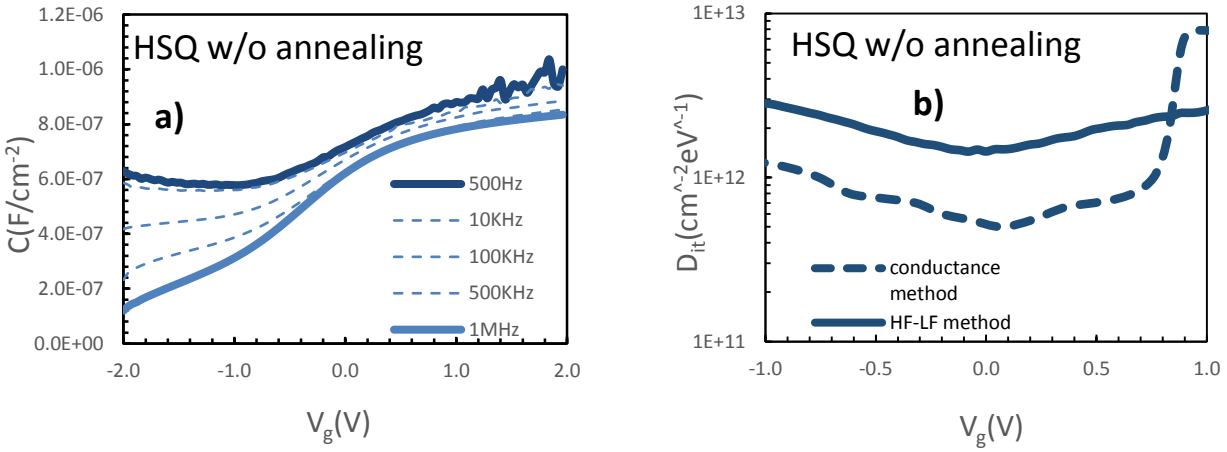


Figure 38: (**Sample B**) C-V frequency dispersion curves. Measured frequency ranges between 500Hz and 1MHz **(a)** and D_{it} versus voltage extracted by conductance and HF-LF methods **(b)**.

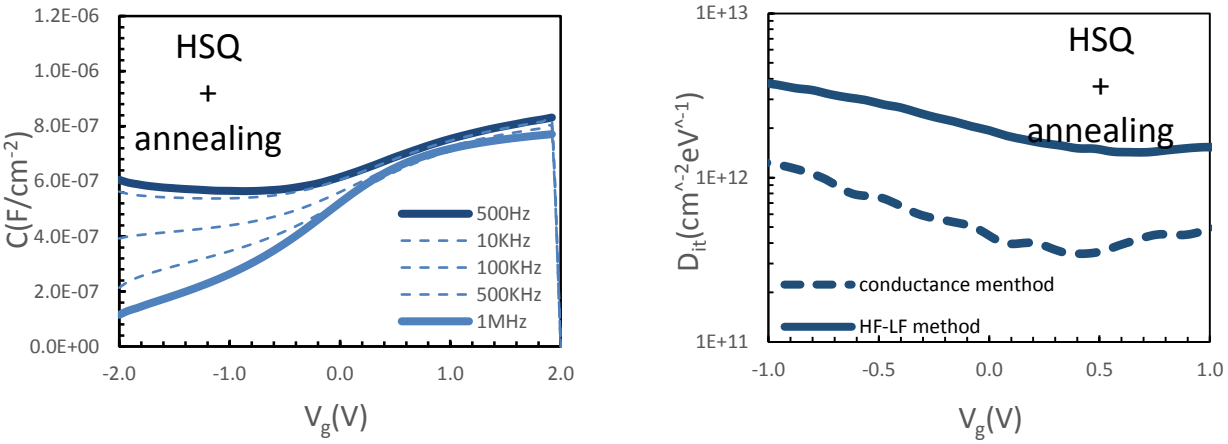


Figure 39: (**Sample C**) C-V frequency dispersion curves. Measured frequency ranges between 500Hz and 1MHz (a) and D_{it} versus voltage extracted by conductance and HF-LF methods.

The value of the maximal measured HF capacitance is 8.35×10^{-7} F/cm^2 and 7.71×10^{-7}F/cm^2 for the HSQ plus without (**Figure 38a**) and with (**Figure 39a**) thermal annealing step respectively that is again lower than the theoretical oxide capacitance. For both samples, HF capacitance curve is shifted with respect to LF figure (stretch out). The distortion is more pronounced with gradually increasing signal frequency. The peak value of the HF capacitance slope dC/dV

obtained in a weak depletion region (transition from inversion to depletion) is $3.45x10^{-7}F/cm^2$ and $3.08x10^{-7}$ F/cm^2 for the sample without (**Figure 38a**) and with (**Figure 39a**) thermal annealing step respectively. In contrast, the sample unexposed to HSQ processing (**Figure 37a**) exhibited a higher slope of HF capacitance $dC/dV=7x10^{-7}F/cm^2$. The sample without annealing step exhibits a minimal peak D_{It} obtained by HF-LF and by conductance method ranging between $1.5x10^{12}eV^{-1}cm^{-2}$ and $5x10^{11}eV^{-1}cm^{-2}$ respectively (**Figure 38b)**. The MOSCAP containing the annealing step presents a minimal D_{it} of $1.4x10^{12}eV^{-1}cm^{-2}$ and $4x10^{11}eV^{-1}cm^{-2}$ extracted by HF-LF and Conductance method respectively (**Figure 39b)**. Comparing the levels of D_{it} obtained by HF-LF method from the sample without HSQ treatment (**Figure 37b**) against the samples exposed to HSQ process (**Figure 38b, Figure 39b**) we can say that these exhibits slightly different values. This can be explained by missing 100Hz measurement for the former and latter MOSCAP due to excessive oxide breakdowns.

Maximal values of extracted D_{it} from all the studied samples are comparable with the state of art gate-last MOSFET process reporting D_{it} of $5x10^{12}eV^{-1}cm^{-2}$ [61] extracted by subthreshold slope method. Also, we can conclude that the annealing step does not have a significant effect on MOSCAP electrical response. Indeed, it is a common technique to protect the semiconductor surface against the thermal damage by a capping layer such as SiO_2 or Al_2O_3. On the contrary, presence of HSQ itself may induce the surface degradation. The MOSCAPS containing the HSQ process (Sample B, C) (**Figure 38a, Figure 39a)** presents a lower slope of HF capacitance (dC/dV) against the sample A (**Figure 37a**) which reveals a slight command degradation.

To clear any doubts about an undesirable impact of the MOSFET process on the gate stack command, digital etching should be used before the oxide deposition to remove a few layers of damaged III-V epi layer. This should have a beneficial impact on the MOSFET command [60].

4 Source and drain contact module

So as to benefit from a high mobility of III-V channel, the source and drain resistance values of MOSFET should be very low. In particular, extremely scaled MOSFETs are concerned. Here, the gate length reduction is followed by an increasing contribution of the access

resistance on the overall MOSFET resistance. Realization of such a contact can be inspired by the already established concepts utilized either in III-V HEMTs or Si MOSFETs.

Dopant implantation is one of the oldest contact technology utilized in MOSFET technology. Its advantage is that the ex-situ doped contacts are formed in a self-aligned manner with respect to the channel. However, dopants require an activation what is typically performed by a thermal annealing that may for certain sorts of semiconductors lead to irreversible material changes. Here are concerned mainly III-V materials that are more sensitive to thermally induced dissociation in comparison to an elemental semiconductor such as Si. Therefore the implantation is not viewed as a viable technique for III-V MOSFET.

Alike the implantation, the silicide like technique involves diffusion of foreign elements into the channel. A thin metal layer is deposited on a wafer, followed by an annealing step that produces diffusion of the metal layer into the epi-layer, thereby forming an alloyed semiconductor/metal phase typically characterized by a low sheet resistivity and by a low contact resistivity. Playing with the metal thickness and with the annealing temperature, modulation of the metal diffusion thickness is achieved. An advantage of the process is its simplicity as the metal deposition can be realized through the gate stack mask providing a self-aligned source and drain contact deposition with respect to the channel. The control of the metal diffusion depth is important, especially for extremely thin channels. Here, the diffusing metal can totally react with the ultra-thin channel semiconductor and limit thus the transfer length between channel semiconductor and the silicide phase. This may result in an increase of the silicide/channel junction resistance leading to a reduced device conductance [96]. Furthermore, the metal diffusion suffers from a bad horizontal resolution what may be problematic especially for extremely small gate lengths.

4.1 Selectively raised source and drain

Unlike contact diffusing techniques, the selective epitaxy is considered to be the least intrusive one. Its main benefit is the contact self-alignment with respect to the channel obtained by utilizing a dielectric hard mask. This permits to precisely define the gate length which is hardly achievable with the abovementioned techniques. Additionally, this can be achieved independently of the dummy gate and gate metal misalignment simply by designing a large gate stack overlap. Due to a precise source and drain definition, it was decided to

fabricate the MOSFET and GAA (or FinFET) contact modules by selective source and drain epitaxy. Illustration of MOSFET model of selectively raised S/D is provided in **Figure 40**.

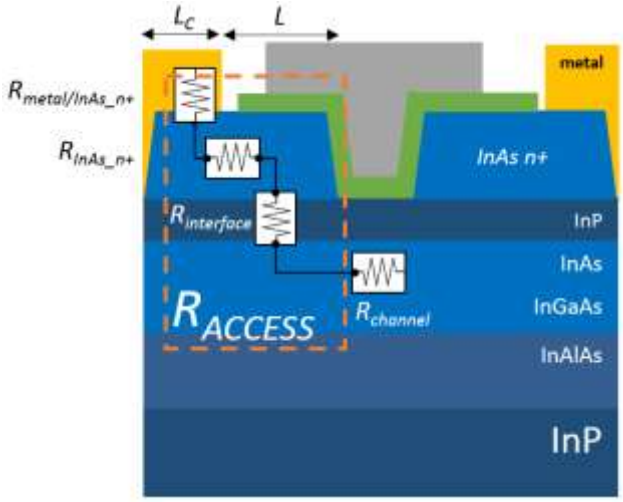


Figure 40: Illustration of MOSFET with raised InAs n+ source and drain. Model of one side access resistance.

Among the epitaxy technique utilized for selective growth, we have chosen Molecular Beam Epitaxy (MBE) installed at IEMN. Its main benefit is a high degree of growth control. On the other hand, a major bottleneck of MBE is a bad selectivity between the hard mask and the semiconductor. Contrary to Metal Organic Chemical Vapor Deposition (MOCVD) where the selective growth is achieved by a different precursor desorption between the hard mask and the semiconductor substrate, in the MBE technique the precursor decomposition is not material sensitive. To achieve the selectivity, it is necessary to optimize the growth conditions and thus achieve a re-evaporation of III elements from the hard mask onto the semiconductor surface. The MBE growths itself with optimization of the growth parameters were realized by Ludovic Desplanque. This was demonstrated for two materials InAs n+ and InGaAs n+. Our contribution consisted in adapting the technique to MOSFET and GAA (FinFET) process. This consisted in hard mask selection and in realization and optimization of associated lithography process as well as studying the impact of the hard mask pattern on the raised contact quality.

4.1.1 Contact uniformity

The raised contact has to present a high degree of surface uniformity. Otherwise, contact deformations, namely at the edges of the gate (access region) may act as a parasite

resistance obscuring the potential of III-V materials to deliver a high on state current. This concerns namely InAs n+ contacts that are grown in this work on InP layer. Due to a high lattice mismatch between InAs and InP, raised InAs n+ contacts are prone to surface deformations. When the growth thickness of InAs on InP exceeds a certain thickness, the elastic energy is relaxed and the growth has 3D character. To circumvent this effect, performing the growth through a small hard mask apertures constituted of HSQ resist enables to obtain a free of defects InAs n+ surface. In the **Figure 41** are compared 2 SEM InAs surfaces recorded after removal from MBE chamber after 150nm InAs regrowth. In **Figure 41a** is displayed in plane InAs n+ realized uniquely through HSQ dummy gate line.

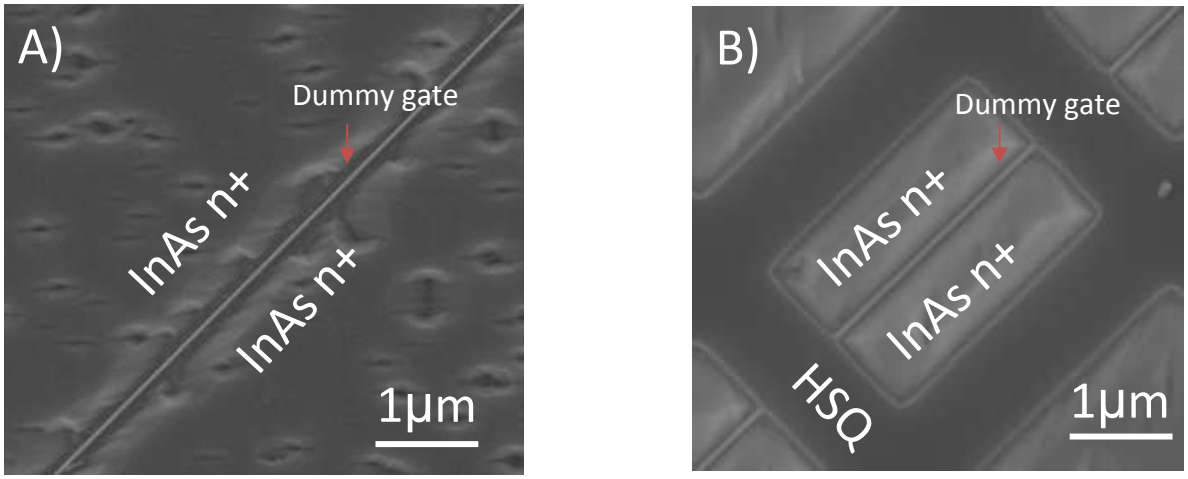


Figure 41: Top-down SEM image of InAs n+ surface recorded after performing MBE growth (a) on a large surface through HSQ dummy gate. The InAs n+ surface is characterized by a low surface uniformity and by an absence of growth in the zone close to the dummy gate. (b) in HSQ 1x3µm apertures. The aperture is completely filled with a high-quality InAs n+.

The SEM image reveals a low InAs n+ surface uniformity. More specifically, this is characterized by defects and also along the zones close to the dummy gate by an absence of InAs material. Lack of InAs n+ material in the device access region increases the overall resistance. In **Figure 41b** is displayed an image of InAs n+ growth in HSQ apertures. An HSQ standing for the dummy gate is put across the HSQ square pattern to create two 1x3 µm HSQ apertures in which the growth is performed in a confined manner, characterized by a noticeable decrease of the surface defects.

4.1.2 Selectivity

Another aspect of the contact fabrication is a growth selectivity between HSQ hard mask pattern and the semiconductor surface. As announced, the MOSFET fabrication process that is reported in this dissertation is realized in a gate last manner. The raised contacts are formed before the gate stack formation which needs to protect the gate area by HSQ hard mask during the MBE contact growth. It is preferable to achieve selective growth uniquely on the semiconductor surface without deposition on the hard mask surface. However, this is hardly achievable in MBE tool. In **Figure 42** is presented an example of a non-selective growth of InGaAs n+. The polycrystalline debris of InGaAs n+ are grown on HSQ surface. It was observed, that even after the HSQ removal, the debris are still presented on the underlying epi-layer surface.

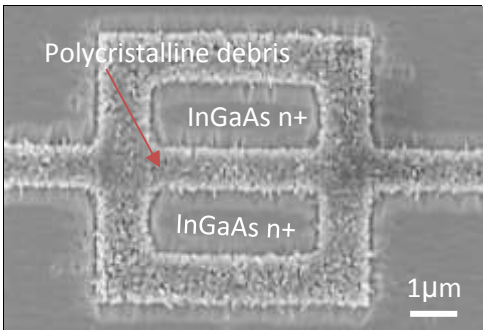


Figure 42: Top down SEM image recorded after InGaAs n+ growth with HSQ hard mask. HSQ surface is covered entirely by polycrystalline debris

One should propose to utilize a resist planarization step and then suppress the debris by a chemical etching. Instead, simplification of the process was brought by a selective MBE growth demonstrated at IEMN by Ludovique Desplanque [97]. Optimizing the MBE growth conditions such as adding an atomic hydrogen flux was achieved a substantial suppression of the debris from HSQ surface for both raised semiconductor InAs n+ and InGaAs n+. Example of an almost debris free HSQ surface is presented in **Figure 43**.

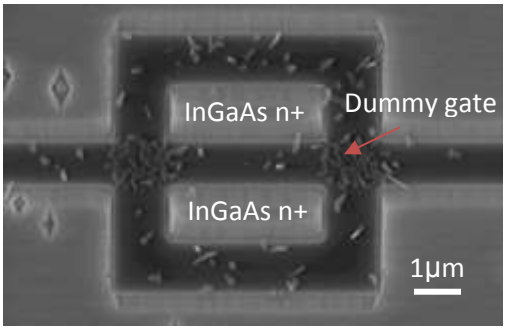


Figure 43: Top down SEM image recorded after InGaAs n+ growth with an almost debris free HSQ surface

4.1.3 Extraction of the contact resistance

As outlined in **Figure 40**, the access resistance of the utilized contact system is composed of 3 elements: a metal/semiconductor contact resistance ($R_{In(Ga)As\ n+/metal}$), sheet resistance of the raised contact ($R_{In(Ga)As\ n+}$), and so-called interface resistance (R_{int}). Sum of the resistances can be extracted by tracing the MOSFET R_{on} as a function of the gate length and then decomposing it into partial resistance components. Whereas the interface resistance is not trivial to obtain, as we will show in the last chapter, the first and second term can be obtained from a Transfer length measurement (TLM).

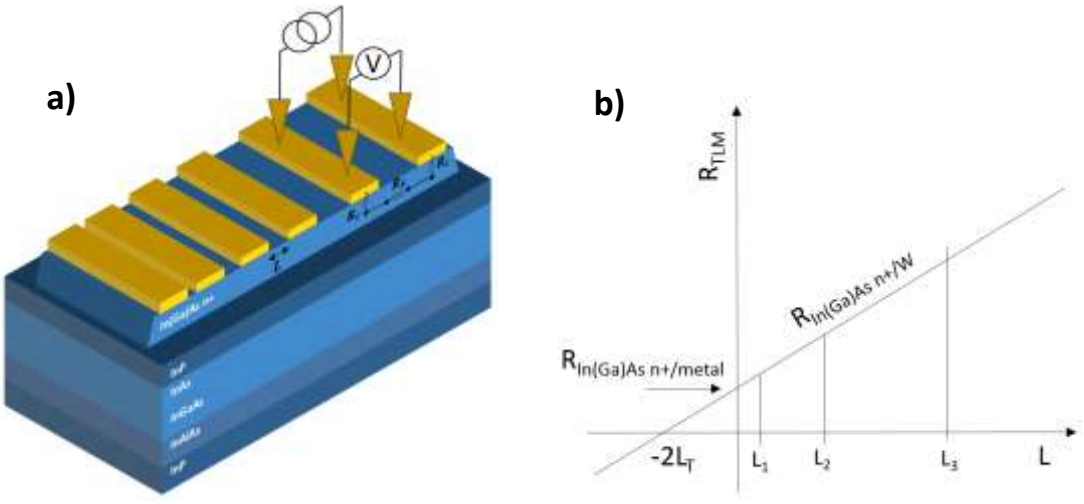


Figure 44: Illustration of a typical TLM structure used in the dissertation for extraction of characteristic resistances of a raised source and drain contact module (a). Traced resistance of TLM structure with outlined elemental resistances.

The design of TLM structure that is utilized in this dissertation to extract characteristic resistance of InAs n+ and InGaAs n+ contact module is illustrated in **Figure 44a**. On In(Ga)As n+ layer grown by MBE on ultra-thin body epi-layer are deposited contact metal pads by thermal evaporation. The metal pads are separated by gaps whose dimensions range from 5 to 20µm. The resistance is measured by a four contact method between each neighbor contacts and displayed as a function of the separation gap. The measured resistance follows a linear evolution that can be mathematically expressed as:

$$R_{\mathrm{TLM}}(L) = R_{In(Ga)As\ n+} L/W + 2R_{In(Ga)As\ n+/metal} \qquad (21)$$

Where L represents the spacing between two neighbor metal pads. Assuming that the conduction through the NID doped epi-layer channel is negligible in comparison to highly doped 1x10^{19}cm^{-3} InAs n+ and InGaAs n+ layer then the contribution of the semiconductor sheet resistance linearly dependent on L is expressed by $R_{In(Ga)As\ n+} L/W$ where $R_{In(Ga)As\ n+}$ is the sheet resistance of the raised source and drain contacts In(Ga)As n+ and can be obtained from the slope of measured R_{TLM}(L).

The function's intercept with y-axis corresponds to a two side metal/semiconductor junction resistance ($R_{In(Ga)As\ n+/metal}$). Assuming that the extrapolated sheet resistance $(R_{In(Ga)As\ n+})$ does not change all along the channel and the maximal distance the current achieves before entering the metal pad (standing for the transfer length L_T) is smaller than the contact length, then we can approximate the contact resistivity as $\rho_{In(Ga)As\ n+/metal} = R_{In(Ga)As\ n+/metal}\ L_T$.

In this work, the TLM extraction structures were placed on the same wafer as the fabricated UTB InAs MOSFETs. Regarding the metal/semiconductor contact resistance ($R_{In(Ga)As\ n+/metal}$), their typical values ranges between 9Ωµm and 29Ωµm for InAs n+ and InGaAs n+ respectively. Higher metal/semiconductor contact resistivity obtained for InGaAs n+ compare to InAs n+ can be attributed to a higher band gap of InGaAs n+ that increases the Schottky barrier height (SBR) presented on the metal/semiconductor interface. In the following table are benchmarked typically reported resistances for MOSFETs utilizing In(Ga)As n+ based contact material systems.

Contact	Doping [cm^{-3}]	Type	$\rho_{In(Ga)As\ n+/metal}$ [$\Omega.\mu m^2$]	$R_{In(Ga)As\ n+/metal}$ [$\Omega.\mu m$]	$R_{In(Ga)As\ n+}$ [Ω/Sq]	Ref
Ti/Pt/Au InGaAs n+	$1x10^{19}$	implantation	N/A	80	128	[98]
Ti/Pt/Au InAs n+	$1x10^{19}$	implantation	N/A	1150	212	[98]
Co-InGaAs n+	$5x10^{19}$	Alloyed	10^5	1100	20	[99]
Pd-InGaAs n+	$2x10^{18}$	Alloyed	10^4	650	77	[100]
Ni-InGaAs n+	$1x10^{19}$	Alloyed	150		20	[101]
Ti/Pd/Au- InGaAs n+	$3,5x10^{19}$	non-alloyed	1	N/A	N/A	[102]
Mo InGaAs n+	$3x10^{19}$	non-alloyed	2-10	0,1 - 0,2	5	[103]
Ti/W-InGaAs n+	$3,5x10^{19}$	non-alloyed	1	N/A	N/A	[102]
Ti/Pt/Au-InAs n+	$1x10^{19}$	non-alloyed	5	9 ± 0.72	14 ± 0.2	This work
Ti/Pt/Au- InGaAs n+	$1x10^{19}$	non-alloyed	23	29 ± 13	38 ± 0.63	This work

Table 2: Benchmarked typically reported resistances for MOSFET with In(Ga)As contact material.

Contact resistances between the metal and InAs n+ and InGaAs n+ semiconductor ($R_{In(Ga)As\ n+/metal}$) reported in this dissertation are lower than the contacts realized at IEMN by implantation (ex-situ doped) of InGaAs [98] and InAs [98]. In particular, the raised InAs n+ (in-situ doped) yields a substantial improvement over implanted InAs n+ (ex-situ doped) contact providing 1150Ωμm [98]. The same can be said about the sheet resistance ($R_{In(Ga)As\ n+}$) that are reduced by around one order of magnitude against the implantation technique.

Benchmarking the metal/semiconductor contact resistivity $\rho_{In(Ga)As\ n+/metal}$ against Ni silicide like contact combined in [101] with a raised InGaAs n+, we can conclude that our material system utilizing a non-alloyed metal stack provides a lower contact resistivity. Similarly, the metal/semiconductor contact resistivity of the whole group of alloyed metal contact shows higher values that varies between $1x10^2$ for Ni-alloy to $1x10^5$ for alloyed Co-InGaAs n+.

The obtained values are in a good agreement with the same category of contact modules characterized by non-alloyed Ti-based metals deposited on doped In(Ga)As n+. A slight difference can be attributed to a surface preparation performed before the metal deposition. Indeed, each preparation technique exhibits a different efficiency in eliminating the native oxide that is generally associated with a parasitic resistance. In this work, we utilize in situ Ar+ plasma, applied prior to the metal evaporation. This was the only in-situ treatment available

in our electron beam evaporation (e-beam) chamber. Therefore, to further reduce the contact resistance, a more advanced technique of native oxide desorption will be required.

5 UTB InAs MOSFET fabrication module

A high-quality epi-layer, low density of interface traps and a low sheet and contact resistance are underlying criteria for building an efficient III-V MOSFET. To do so, one should also ensure that these modules are assembled in a precise and careful way with respect to the deeply scaled dimensions of envisioned MOSFET. In the following section is presented UTB InAs MOSFET fabrication module with selected key fabrication studies.

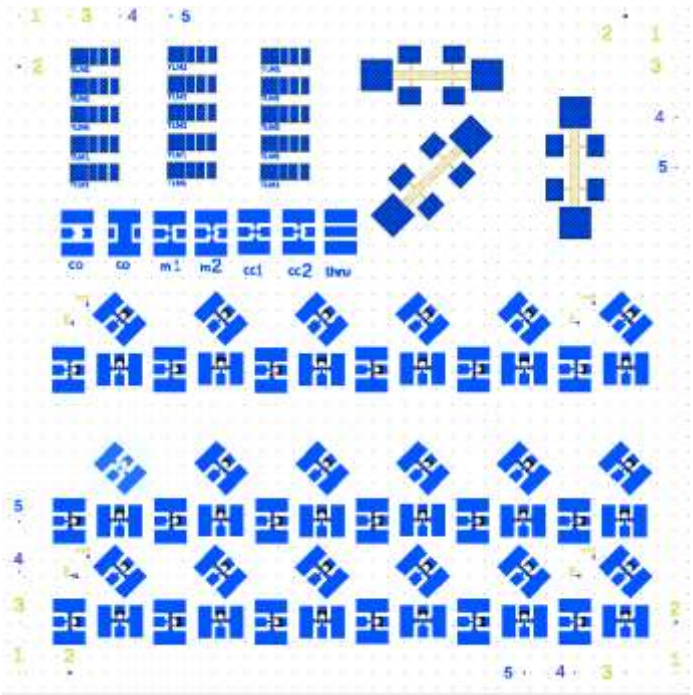


Figure 45: Lithography mask of UTB InAs MOSFET

5.1 Presentation of UTB InAs MOSFET mask

In **Figure 45** is presented MOSFET lithography mask. In order to form nanometric HSQ dummy gate, Electron Beam Lithography (EBL) tool capable to perform a high precision writing

is utilized. For the sake of simplicity, the whole fabrication process is performed exclusively by EBL tool.

The MOSFET measurement structure is composed of 2 gate fingers (**Figure 46**). Width of one finger is set to 3µm (**Figure 47**). Further, the mask contains Transmission line method (TLM) enabling to extract the characteristic resistances of selectively raised module (**Figure 48**). Even though the dissertation was primarily oriented towards optimization of MOSFET's DC performances, a small part was also devoted to RF analysis. Therefore, in the mask were placed structures enabling to carry out a de-embedding of MOSFET parasitic elements (**Figure 49**).

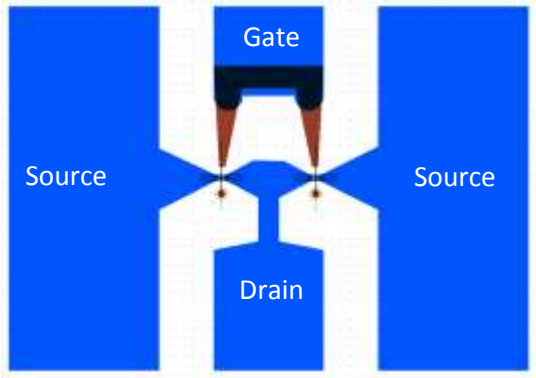


Figure 46: Design of two fingers (MOSFETs) measurement structure.

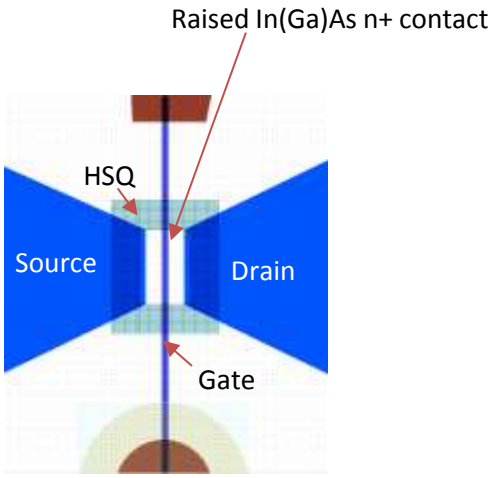


Figure 47: Focus on MOSFET mask design.

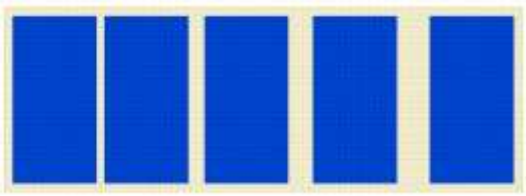


Figure 48: Transmission line measurement structure

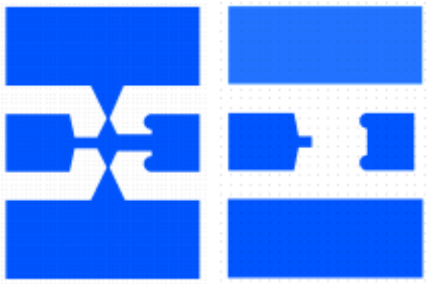


Figure 49: Open and short circuit MOSFET structure utilized for RF de-embedding of parasitic elements.

5.2 UTB InAs MOSFET process flow

The MOSFET process flow is composed of the following fabrication steps:

1. **Surface wafer cleaning**

   The first step consists in cleaning the surface in acetone and Isopropanol bath.

2. **Mark alignment definition**

   Alignment marks were defined by a bilayer COPO/PMMA positive resist that was exposed by EBL tool and followed by a development in Isopropanol and Methyl Isobutyl Ketone (MIBK) solution. The metal stack composed of Ti/Pt is deposited by a thermal evaporation.

3. **HSQ pretreatments**

   Prior to the HSQ spin coating was performed an improvement of the epi-layer adhesion properties.

4. **HSQ definition**

   The HSQ resist is spin coated and exposed by EBL tool. Rapid thermal annealing (RTA) is carried out enabling evaporation of residual solvents from the resist and preventing thus the MBE chamber pollution.

5. **HSQ revelation**

   The revelation of HSQ resist is carried out in TMAH solution. So as to avoid the collapse of the deeply scaled and fragile HSQ structures is performed supercritical drying in CO_2 atmosphere.

6. **MBE In(Ga)As n+ contact regrowth**

   After the transfer into MBE tool, the sample was thermally annealed under atomic hydrogen eliminating the surface native oxides and carbons residues. This was followed by a selective growth of doped InGaAs n+ or InAs n+. The temperature window of In(Ga)As n+ MBE regrowth is between 400°C and 500°C. Typical thickness of the raised contacts reported in this dissertation ranges between 100 and 150nm.

Figure 50 gives an illustration and SEM image recorded after InAs n+ selective regrowth.

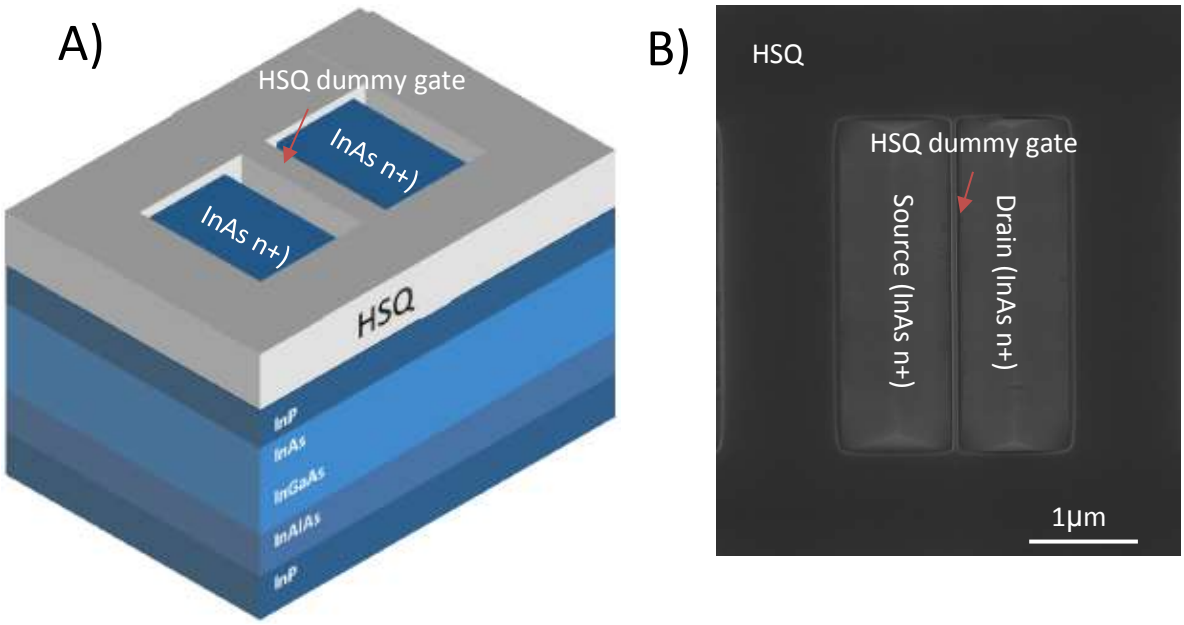


Figure 50: Illustration (**A**) and top-down SEM image of localized selectively raised source and drain contact in HSQ pattern (**B**).

7. HSQ removal

Prior to the oxide deposition, the hard mask pattern (HSQ) was selectively removed in BOE solution leaving the channel ready for the ALD oxide deposition.

8. ALD oxide deposition

After performing the native oxide removal in a low concentrated HCl 10% solution, the surface was passivated in $(NH_4)_2S$ 10% solution. The sample was subsequently transferred in ALD chamber where was deposited high-k oxide of either **1)** single layer Al_2O_3 4nm or **2)** bilayer Al_2O_3 2nm + HfO_2 2nm with a post-deposition oxygen plasma as described in the gate stack module. The temperature window of Al_2O_3 and HfO_2 ALD deposition is between 150°C and 250°C.

9. Gate metal deposition

Gate stack is completed by an electron beam evaporation (e-beam) of Ni/Au or Ti/Pt/Au through a bilayer of COPO/PMMA mask patterned by EBL lithography. **Figure 51** gives an illustration and a SEM image recorded after the gate metal deposition.

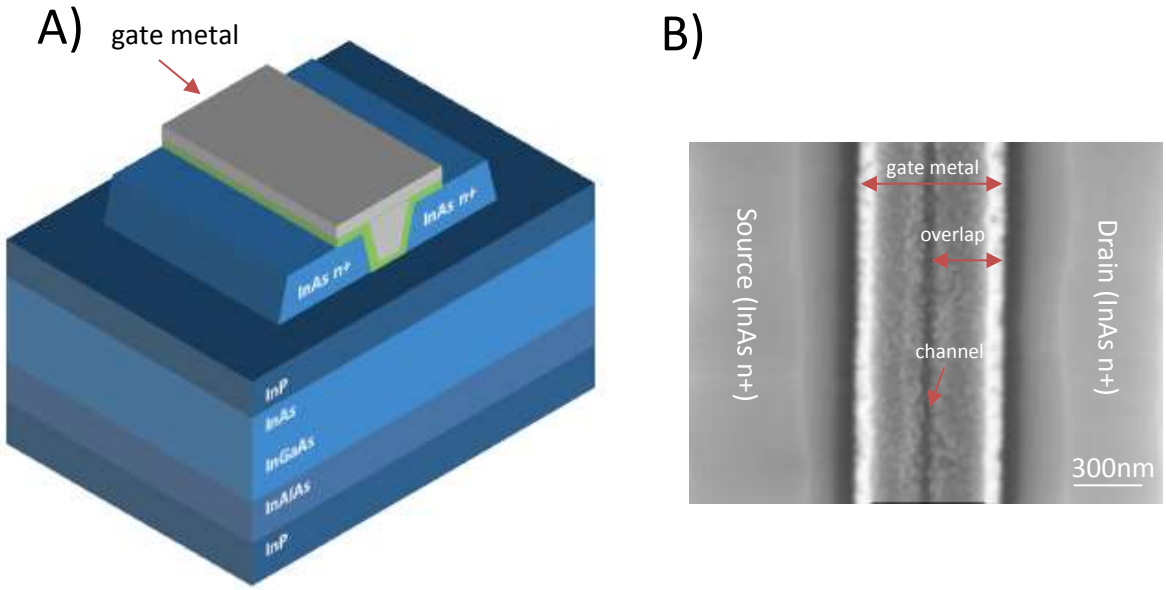


Figure 51: Illustration **(A)** and top-down SEM image of the raised S/D and gate stack recorded **(B)** after the gate metal lift-off.

10. Oxide etching

Oxide in the zones of raised Source and Drain is etched by means of BOE chemistry (used for **single layer oxide Al_2O_3**) or BCl_3 chemistry in Reactive Ion Etching (RIE) tool combined with an Inductively Coupled Plasma (ICP) (used for **bilayer Al_2O_3 + HfO_2**).

11. Source and Drain metal pad evaporation

Formation of metal pads is performed evaporating Ti/Pt/Au through a bilayer resist patterned by EBL lithography.

12. MESA isolation

Electrical isolation of the MOSFET is performed by removing the InP/InAs/InGaAs active layer and a part of InAlAs buffer layer. This was realized by exposing the sample to BOE chemistry (used for single layer **oxide Al_2O_3**) or RIE-ICP under BCl_3 chemistry (utilized for **bilayer Al_2O_3+ HfO_2**) and then by soaking in $H_3PO_4/H_2O_2/H_2O$ solution. The active parts were protected by SAL 601 negative resist mask. **Figure 52** gives an illustration and a SEM picture of cross section of the completed device.

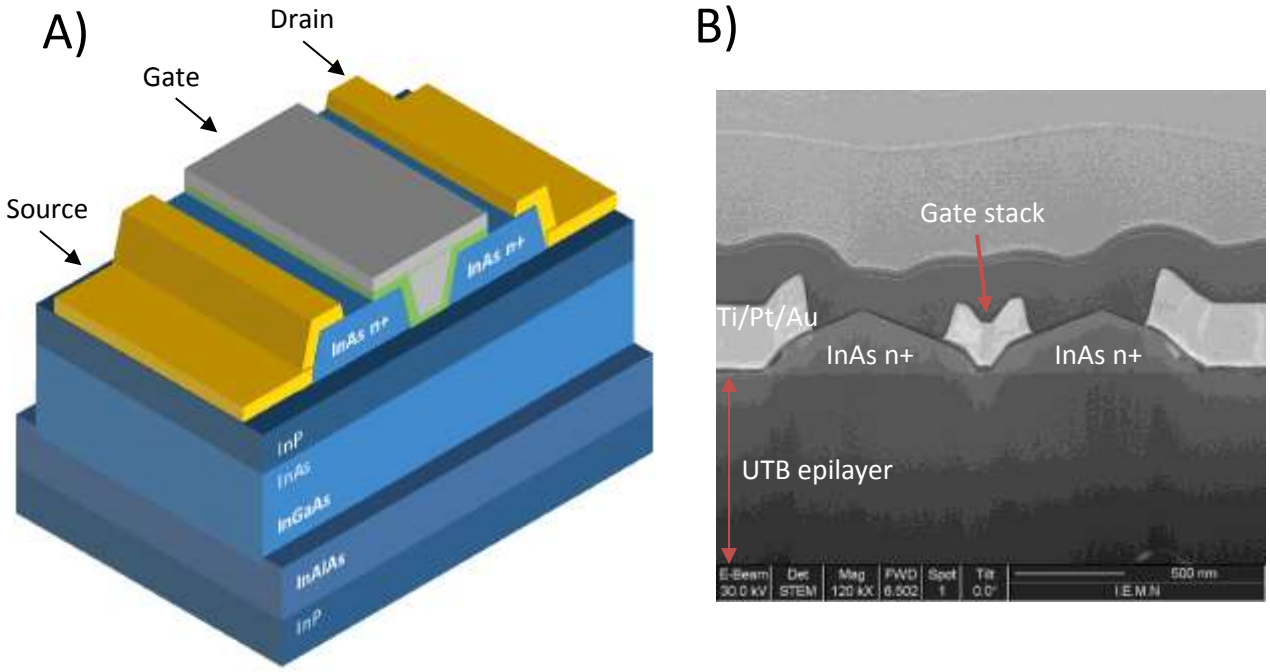


Figure 52: Illustration **(A)** and cross section STEM image **(B)** of the completed UTB InAs MOSFET with selectively raised InAs n+ S/D

5.3 Hard mask patterning

The process of HSQ hard mask required special attention, as the HSQ dummy gate defines the MOSFET gate lengths. Following the scaling principles, this should descend to extremely small nanometric dimensions. However, definition of HSQ nanopatterns on InP substrate was not trivial. Critical points were namely the surface preparation and the mechanical stability. Also to obtain extremely small dimensions, the applied electron dose of EBL lithography needed refinement with respect to InP substrate.

5.3.1 EBL dose determination

Exposition of HSQ by electron beam leads to a modification of the resist morphology. This is manifested as a different development (etching) resistivity in comparison to an unexposed area. To ensure a high-resolution resist patterning, we need to precisely determine the EBL electron dose standing for a number of incident electrons per unit area of exposure. Its unity is given in micro-Coulomb per square centimeter $\mu C/cm^2$. An excessive electron dose is translated into a bigger HSQ size than designed and vice-versa. Example of an overdosed HSQ line is shown in **Figure 53**. The difference between a designed HSQ larger and a real larger is approximately 50nm. Diminishing the dose by around 2000 $\mu C/cm^2$ leads to an optimal HSQ larger (**Figure 54**).

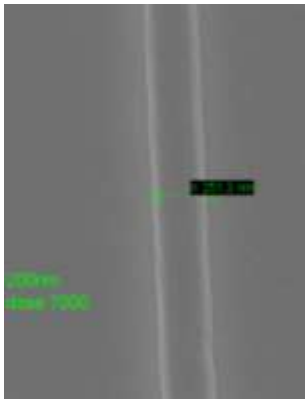


Figure 53: HSQ line exposed by a dose of 7000 $\mu C/cm^2$. The mismatch between a designed and a real thickness is 50nm.

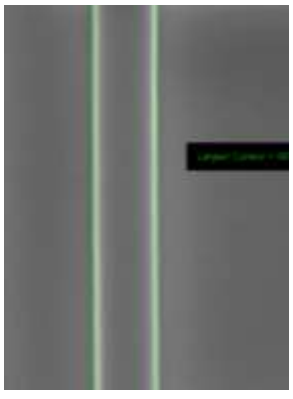


Figure 54: HSQ line exposed by a dose of 4800 $\mu C/cm^2$. The mismatch between a designed and a real thickness is not detectable.

5.3.2 HSQ adhesion

First tests of HSQ (dummy gate) development have revealed a poor adhesion of HSQ nanostructures on InP surface. More specifically, after development in TMAH solution, the majority of HSQ nanostructures have collapsed. In reference to [104], HSQ adhesion properties are strongly related to the substrate surface chemistry that can be modified by a surface preparation. Whereas in case of Si, the surface is covered by a native oxide that is considered to form a stable bond with HSQ, adhesion mechanism of HSQ on III-V materials has not been understood yet. In addition, the adherence promoter Hexamethyl-disilazane (HMDS) is considered inefficient for III-V substrates [105].

Few test were realized to study the HSQ adhesion on InP. The first sample was treated by HF solution. After the development in TMAH solution, the HSQ patterns are visibly detached from the surface (**Figure 55**). While HF is efficient in removing the native oxides, it leaves the InP surface terminated by F species what renders the surface hydrophobic [88]. Another factor that can contribute to the structure collapse is a mechanical stress induced during the drying step [106]. Alternatively, drying from a low surface tension liquid such as IPA can provide some benefits. Finally, using an Ammonium hydroxide based solution and employing a supercritical drying technique provided a suitable result (**Figure 56**). The former is typically applied as a removal of surface organic contamination. The latter enables to reduce the surface tension by replacing the nitrogen drying by a supercritical drying in CO_2 atmosphere leading to a reduced HSQ surface tension.

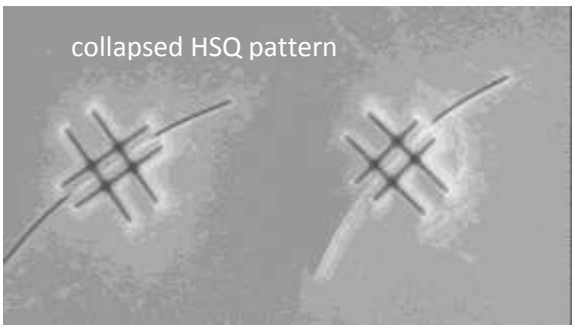


Figure 55: Example of a collapsed HSQ structure after HF treatment and nitrogen drying

Figure 56: Example of a free-standing HSQ structure after Ammonium hydroxide based solution and supercritical drying.

5.4 Impact of selected wet chemical treatments on MOSFET UTB epi layer

During the MOSFET fabrication process, the epi-layer surface was exposed to multiple chemistries that are either cleaning solutions, removal solutions or development solutions. In particular, a special attention should be given to a controllable and a selective removal of the epi-layer native oxide. Otherwise, a high surface roughness may cause an increased level of the oxide/semiconductor interface traps D_{it} and also increase the carrier surface scattering. Therefore, was analyzed an impact of various species utilized during the process namely TMAH, HF, NH_4OH, HCl. In particular, were examined two parameters, the surface roughness and the etched thickness by means of Atomic force microscopy (AFM). To measure the etched thickness was utilized a positive resist that covers the non-exposed area and that serves as a reference plane. After the surface treatment and the resist removal, the measured step between the exposed and unexposed planes provides the etched thickness.

5.4.1 NH_4OH treatment

The first examined treatment was a low concentrated Ammonium hydroxide (NH_4OH) 10% solution typically used as a universal semiconductor surface cleaner. The solution removes the InP native oxide leaving the surface passivated or in other words chemically inactive. In this work, we have discovered that a low concentrated NH_4OH improves the HSQ adhesion on InP surface. After immersing the sample during 1 minute into HCl 10% bath, we obtain the etched thickness of 0.5nm. This can be assigned to a removal of InP native oxide (**Figure 57**) without modifying the surface roughness (**Figure 58).**

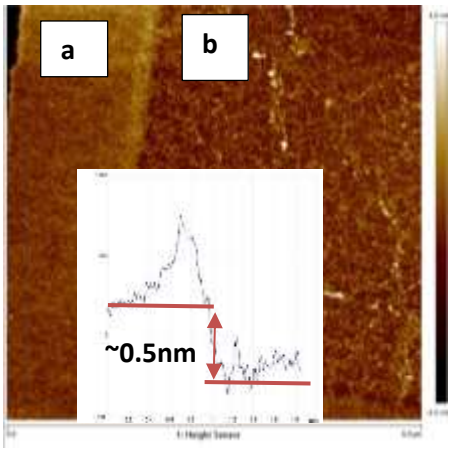


Figure 57: Scanned surface of the masked area (a) and the area exposed (b) to NH_4OH solution. Measured step between (a) and (b) plane is around 0.5nm

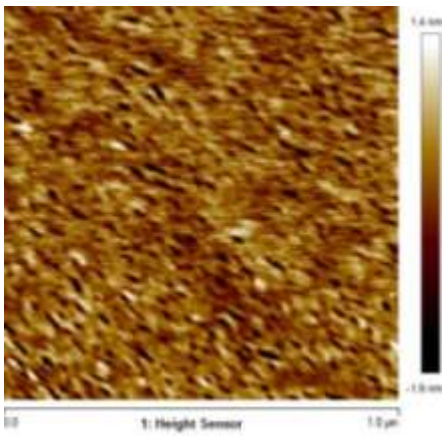


Figure 58: AFM scanned surface exposed to NH_4OH solution. The measured roughness RMS =0,42nm (RMS of virgin epi-layer is 0.48nm)

5.4.2 TMAH treatment

Tetra Methyl Ammonium Hydroxide (TMAH) is usually used in Silicon industry. Regarding III-V material, no reported study on TMAH etching III-V was reported so far. In this work, the TMAH 25% is applied during 1 minute as a hard mask developer stripping the unexposed HSQ resist. The realized test with 25% TMAH applied during 1 minute confirms that TMAH based solution does not react with InP surface. The etch step is undetectable (**Figure 59**) and the surface roughness is not increased either **(Figure 60).**

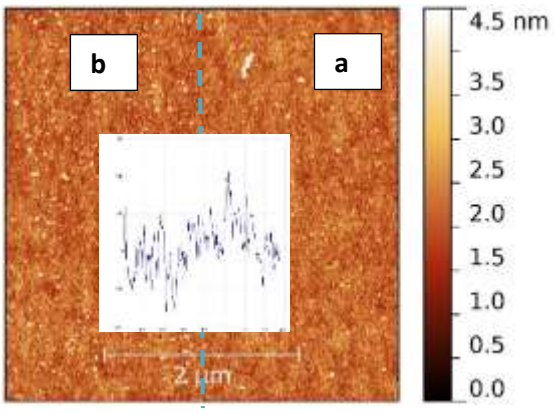


Figure 59: Scanned surface of the masked area (a) and the area exposed to TMAH solution (b).

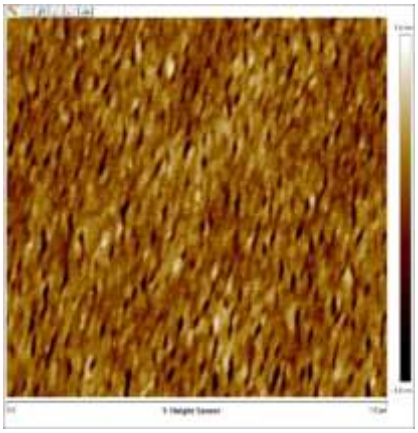


Figure 60: AFM scanned surface exposed to TMAH solution. The measured roughness RMS = 0,35nm (RMS of virgin epi-layer is 0.48nm)

5.4.3 HCl Treatment

The surface of InP is covered by a thin native oxide containing few atomic layers (2-10Å). To obtain a high-quality semiconductor oxide interface, the native oxide needs to be removed prior to the ALD deposition. This is an underlying criterion for obtention of a low EOT and D_{it} oxide deposition. Usually, the native oxide of InP is removed [89] in a low concentrated HCl solution in a selective and controllable manner. The performed test with 10% HCl applied during 1 minute confirms that a sample dipped in a low concentrated HCl removes approximately 1nm of the epi-layer attributed to a dissolution of InP native oxide (**Figure 61**) without roughening the InP surface. (**Figure 62**).

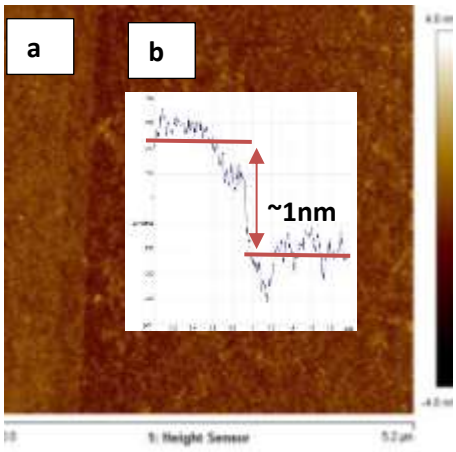


Figure 61: Scanned surface of the masked area (a) and the area exposed to HCl solution (b). Measured step between (a) and (b) plane.

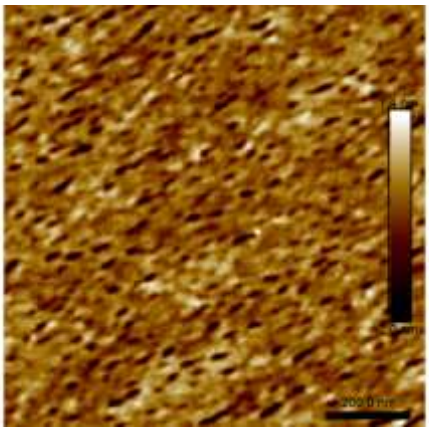
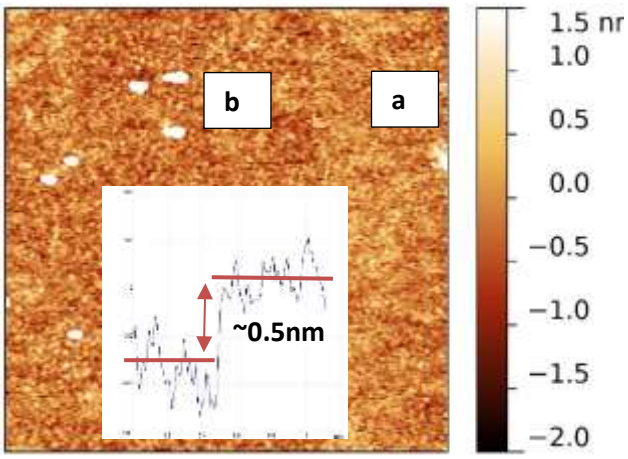


Figure 62: AFM scanned surface exposed to TMAH solution. The measured surface roughness RMS=0,41nm (RMS of virgin epi-layer is 0.48nm)

5.4.4 HF Treatment

Hydrofluoric acid (HF) based solutions are also reported as a remover of InP native oxide [88][107]. In addition to this, HF reacts with the SiO_2. In this work, we utilize the HF-based solution as a remover of HSQ resist. Even though the tested HF concentration and time presented in this study does not correspond exactly to the applied etching time and concentration utilized in the MOSFET process flow, the test can provide a rough idea of HF effects on the epi-layer surface. At low concentrated rates, the estimated etched InP thickness

is around 0.5nm (**Figure 63**) with an undetectable increase of the surface roughness (**Figure 64**).



***F*igure 63**: AFM Scanned surface of the masked area (a) and the area exposed to the HF solution (b). Measured step between (a) and (b) plane.

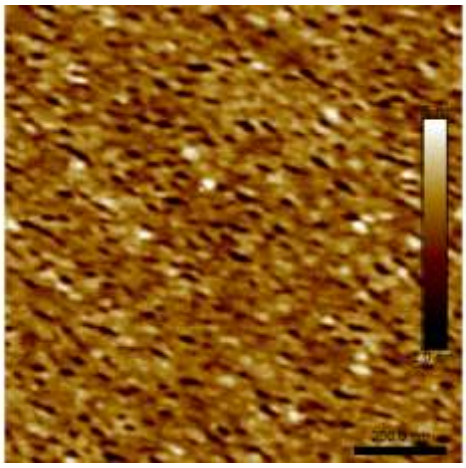


Figure 64: AFM scanned surface exposed to TMAH solution. The measured surface roughness RMS=0,42nm (RMS of virgin epi-layer is 0.48nm)

According to the abovementioned results, we can conclude that the tested chemistries do not damage the epi-layer. The maximal etched thickness ranges between 0 and 1nm what can be attributed to the native oxide dissolution. The tested treatments do not increase the surface roughness either.

6 GAA (FinFET) InAs fabrication module

The second category of device that is presented in this work is a MOSFET using 3D channel topology. Device fabrication is constituted of two selective MBE epitaxy steps: MBE epitaxy of InAs/GaSb channel nano-template and InAs n+ source and drain contacts. The device contains high-k oxide surrounding the channel. Characteristic feature of the fabrication scheme is that it allows to wrap the channel by a metal that is referred as Gate-all around (GAA) topology.

6.1 Presentation of GAA (FinFET) InAs mask

Lithography mask used in the GAA (FinFET) process is presented in **Figure 65**. It contains devices with the following gate lengths: 25nm, 100nm, 200nm and 1µm. Each device is composed of 2 fingers. The fin width is 200nm and each finger contains 37 fins.

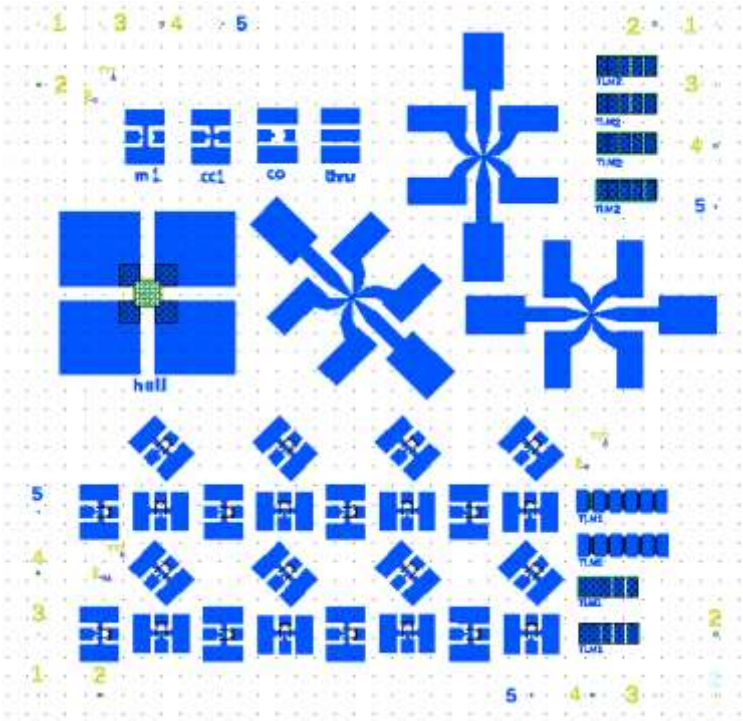


Figure 65: Lithography mask of GAA (FinFET) InAs

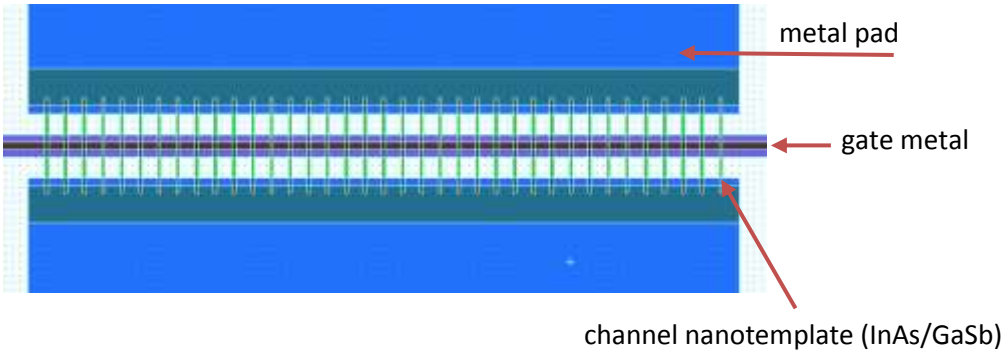


Figure 66: Focus on GAA (FinFET) InAs mask design.

6.2 GAA (FinFET) InAs MOSFET process flow

The device fabrication process flow is described in the following:

1. **Cleaning step**

   The process starts with a removal of surface contamination by immersing the InP substrate into aceton and isopropanol bath.

2. **Silica deposition**

   Silica (SiO_2) is deposited by Plasma enhanced chemical vapor deposition (PECVD). This serves as a hard mask for the first selective MBE growth of GaSb + InAs.

3. **Alignment marks**

   Alignment marks were defined by bilayer COPO/PMMA positive resist exposed by EBL. This was followed by a development in isopropanol (IPA) and Methyl Isobutyl Ketone (MIBK) solution. The metal stack composed of Ti/Pt is deposited by electron beam evaporation.

4. **Hard mask pattern**

   The windows in SiO_2 are then opened by a reactive ion etching (RIE) utilizing PMMA mask that was previously patterned by EBL lithography.

5. **Selective Molecular Epitaxy of GaSb + InAs**

   The sample is transferred into MBE chamber where is carried out InP surface deoxidation followed by a selective growth of 150 nm thick GaSb serving as a sacrificial layer plus InAs 30nm thick channel layer. In **Figure 67** is given an illustration and top-down SEM image recorded after the channel nanotemplate InAs/GaSb epitaxy.

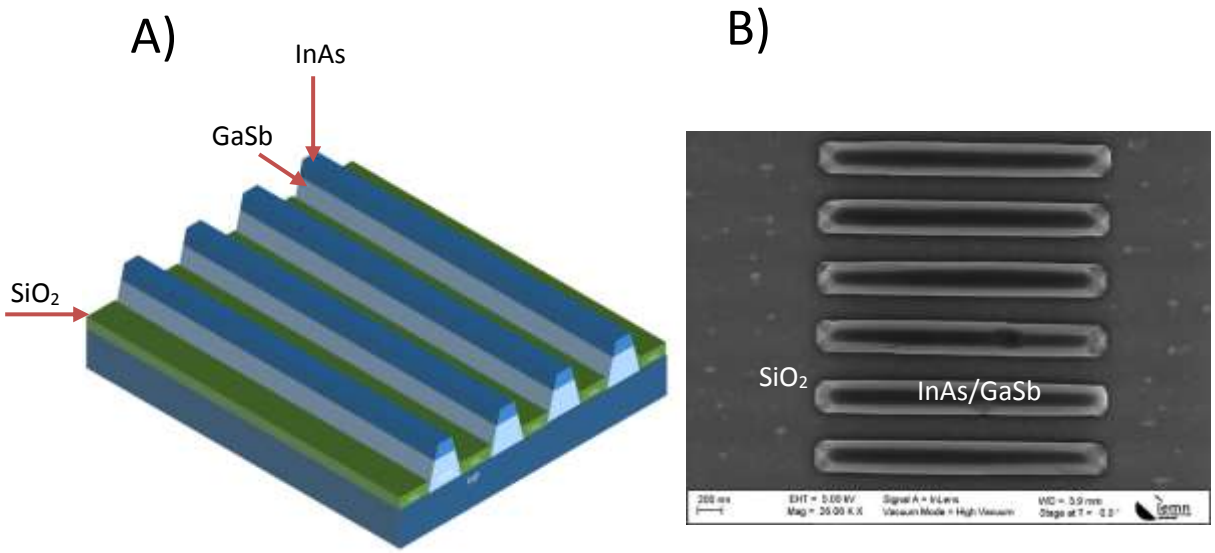


Figure 67: Illustration (A) and top-down SEM image (B) recorded after the MBE of GaSb + InAs channel nanotemplates grown through SiO_2 mask.

6. Second hard mask pattern

HSQ is spin coated and then written by EBL Electron beam lithography. The resist development is carried out in TMAH bath. To avoid the collapse of released InAs wires, the drying is performed in CO_2 atmosphere. Rapid thermal annealing (RTA) is carried out enabling evaporation of residual solvents from the HSQ resist and preventing thus the MBE chamber pollution.

7. MBE contact regrowth

The sample is transferred into MBE chamber where is selectively grown InAs n+ source and drain contact through HSQ hard mask pattern. **Figure 68** gives an illustration and SEM top-down image recorded after the second selective MBE epitaxy of InAs n+.

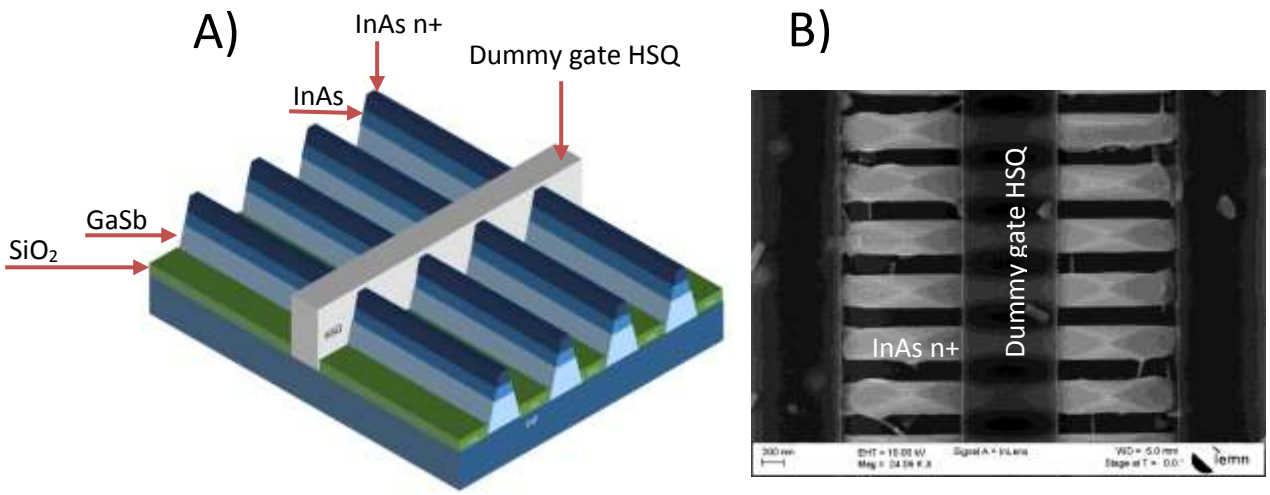


Figure 68: Illustration (A) and top-down SEM image (B) recorded after the second MBE InAs n+ regrowth on InAs channel.

8. HSQ removal

The HSQ dummy gate (hard mask) covering the channel during the growth as well as the first hard mask (SiO_2) is etched away immersing the sample in BOE bath that also partially attacks the sacrificial GaSb layer. To ensure a complete GaSb removal is carried out TEM and SEM inspection of the nanowire profile.

9. Source and Drain metal pad evaporation

Formation of the source and drain metal pads (Ti/Pt/Au) is performed by e-beam evaporation through a bilayer COPO/PMMA resist patterned by EBL lithography.

10. Gate stack deposition

The oxide deposition is preceded by an ex-situ surface passivation, immersing the sample into HCl and $(NH_4)_2S$ solutions. The high-K bilayer oxide Al_2O_3 2nm + HfO_2 3nm are deposited in a conformal manner by Atomic layer deposition (ALD). The temperature window of Al_2O_3 and HfO_2 ALD deposition process is between 150°C and 250°C.

11. Gate metal deposition

The device fabrication is completed by electron beam evaporation (e-beam) of Ni/Au serving as gate stack metal and gate access pad. Illustration and top-down SEM image recorded after the device fabrication is displayed in **Figure 69**.

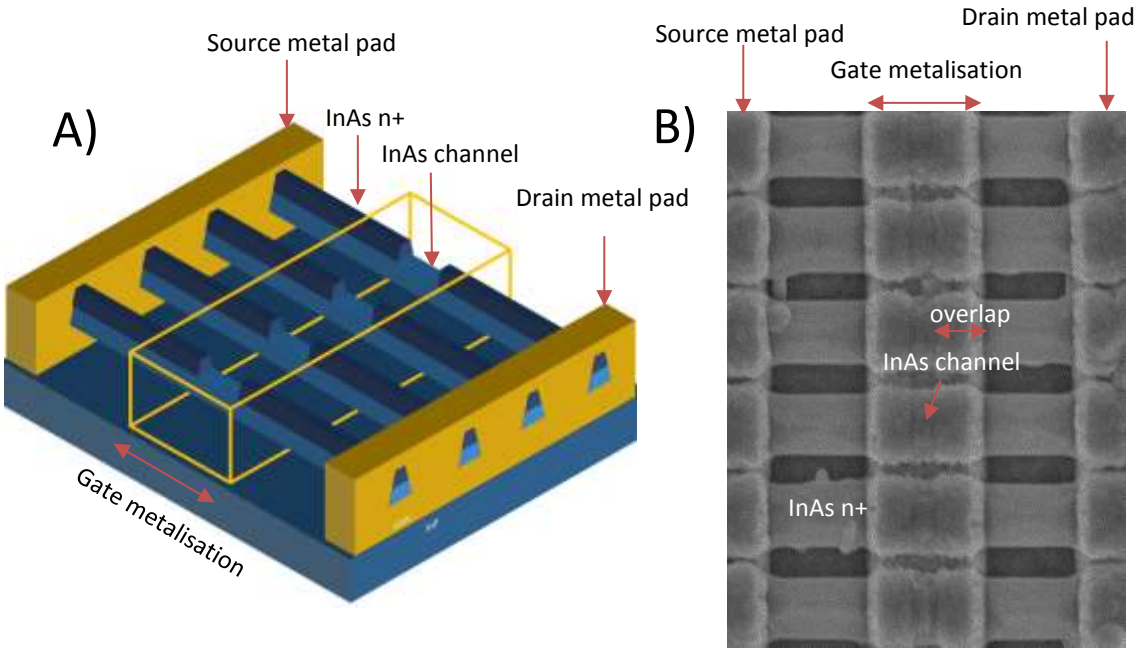


Figure 69: Illustration (**A**) and top-down SEM image (**B**) recorded after source, drain and gate metallization.

6.3 Impact of device orientation on channel and contact uniformity

Building a GAA (FinFET) device with a high-quality InAs channel and InAs n+ source and drain contacts is a precondition for achievement of high performance and reproducible device operation. For instance, defects in InAs channel or in InAs n+ contacts may have a detrimental impact on the device conductance. We have observed that the apparition of surface defects is strongly related to the orientation of the device. In the following section are analyzed SEM images recorded after InAs/GaSb channel and InAs n+ S/D contact epitaxy for the following directions [110], [1-10] and [100].

A) Device oriented along [110] direction

The first selective epitaxy of channel GaSb and InAs nanoribbons in SiO_2 apertures oriented along [110] direction exhibits a homogenous and continuous surface (**Figure 70a**)**.** No degradation is observed after the HSQ development in TMAH solution (**Figure 71a**)**.** Equally, the second epitaxy of InAs n+ contact performed through HSQ hard mask apertures presents a uniform and reproducible 3D shaping (**Figure 72a**).

B) Device oriented along [1-10] direction

Examining InAs/GaSb nanoribbons oriented along [1-10] direction, we can notice a presence of surface defects (**Figure 70b**). By soaking the sample in TMAH solution is removed underlying sacrificial GaSb layer what is followed by a collapse of liberated InAs nanowire (**Figure 71b**). The second epitaxy of InAs n+ S/D is characterized by a non-regular shaping (**Figure 72b**).

C) Device oriented along [100] direction

Device oriented along [100] direction display a continuous and homogenous InAs/GaSb surface (**Figure 70c**). Removal of GaSb in TMAH soak reveals continuous, however, “twisted” shape of InAs channel. (**Figure 71c**) The second epitaxy of InAs n+ contact presents 3D surface shaping (**Figure 72c**).

From the device perspective, the both InAs 3D channel, as well as InAs n+ contact, should display continuous and defect-free surface. In this view, devices oriented along [110] show the least topological imperfections with a continuous and reproducible InAs channel as well as continuous and reproducible InAs n+ selectively raised contacts.

channel InAs/GaSb template

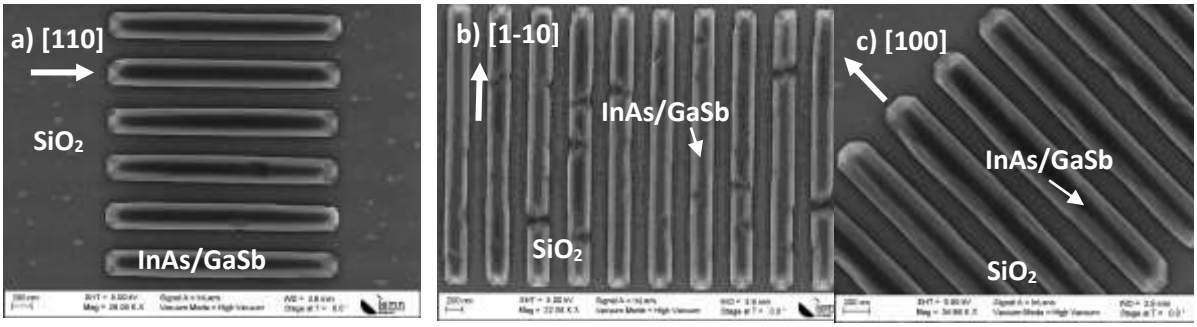


Figure 70: Top down SEM images of InAs/GaSb channel nanotemplate grown in SiO_2 apertures oriented along a) [110] b) [1-10] c) [100] direction.

HSQ dummy gate definition

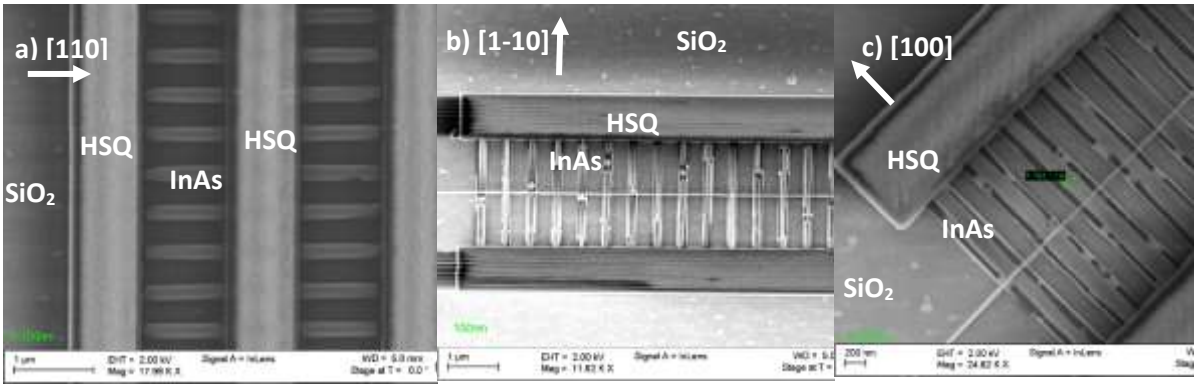


Figure 71: Top-down SEM image recorded after HSQ development in TMAH that partially remove the underlying GaSb layer. Nanoribbons are oriented along a) [110] b) [1-10] c) [100] direction.

raised InAs n+ source and drain

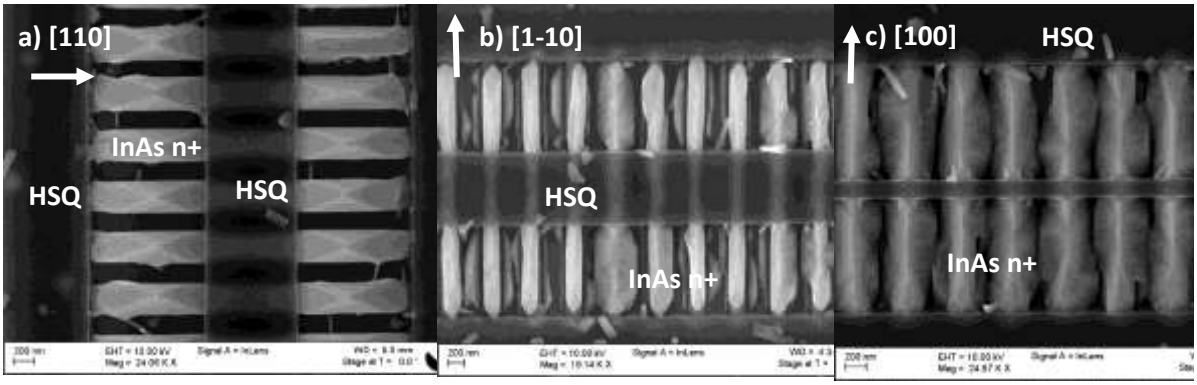


Figure 72: Top down SEM image recorded after MBE selective regrowth of InAs n+ displayed in a) [110] b) [1-10] c) [100] direction.

6.4 Chemical Analysis

Structural and chemical analysis enabling to determine the channel InAs and contact InAs n+ (**Figure 73**) material composition is carried out by means of Transmission Electron Microscopy (TEM) and Electron Diffraction Spectroscopy (EDX) respectively. The extraction of samples from the wafer was carried out by Focus Ion beam (FIB) cut. Discussion of the observation is provided in the following.

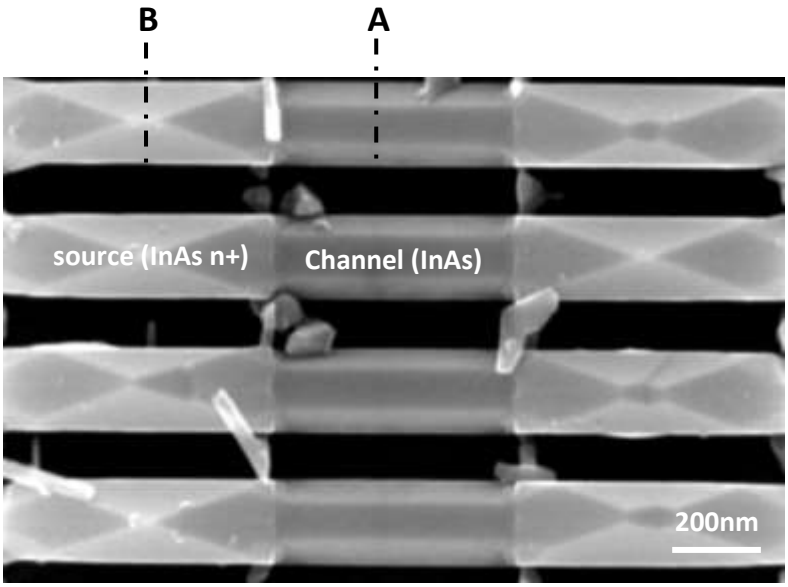


Figure 73: Top-down SEM image of [110] oriented InAs/GaSb nanostructures recorded after HSQ dummy gate removal. Dotted lines **A** and **B** depict InAs channel and InAs n+ contact profiles respectively.

In **Figure 74** is displayed TEM image of InAs channel region (**line A in Figure 73**). We can notice incomplete removal of the sacrificial GaSb. Beside the in-plane InAs channel located on the top of GaSb, the growth of InAs is extended on GaSb facets. A bad resolution disables clear differentiation between InAs channel and GaSb sacrificial layer. Different elements present in the structure were identified utilizing EDX (**Figure 75**). The top layer presents Indium and Arsenide species. We can also notice that InAs layer presents a minor concentration of Antimony and undetectable concentration of Galium. Noticeable oxide concentration situated mainly in a thin layer surrounding InAs channel is a sign of surface oxidation.

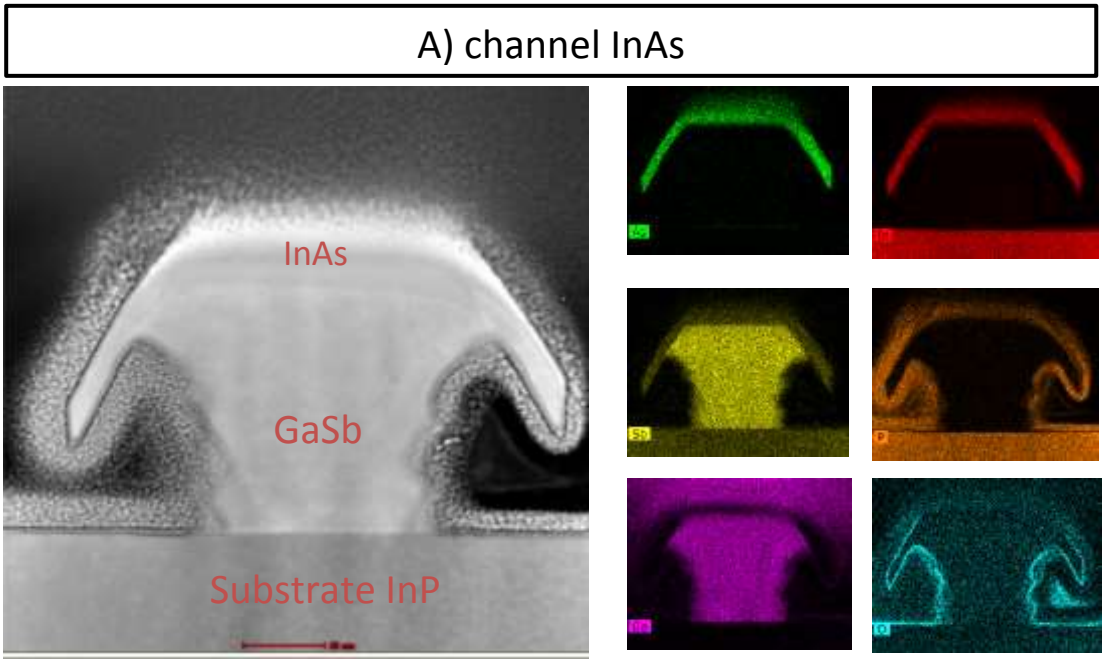


Figure 74: Cross-sectional image of InAs/GaSb channel nanotemplate oriented along [110] direction recorded by TEM (**line A in Figure 73**). **(courtesy of Aurélien Olivier)**

Figure 75: EDX images of cross-sectional InAs/GaSb channel nanotemplate oriented along [110] direction. The color of As, In, Sb, P, Ga and O spectre is green, red, yellow, orange, purple and blue respectively. **(courtesy of Aurélien Olivier)**

Inspecting the region of raised InAs n+ source contact (**line B the Figure 73)** we can notice a 3D faceting of InAs n+ specific for [110] direction (**Figure 76**). Image contrast allows to clearly differentiate between InAs n+ and InAs and precisely determine the InAs channel dimensions. These are 30nm for the center zone and 20nm for the side zones. The peak distance between InAs n+ contact and the in-plane facet of InAs channel is around 140nm. The distance between InAs n+ and InAs channel side facets is around 80nm. To our surprise, InAs n+ occurs below the InAs channel what is confirmed by EDX analysis (**Figure 77**). Beside this, below the InAs channel is still presented GaSb having a triangular shape.

Both images (**Figure 75, Figure 77** reveals presence of residues of sacrificial GaSb layer below InAs channel. These were not completely eliminated during the BOE soak. To pursuit the device fabrication the sample was treated in TMAH that efficiently removed residual of GaSb.

B) raised InAs n+ contact

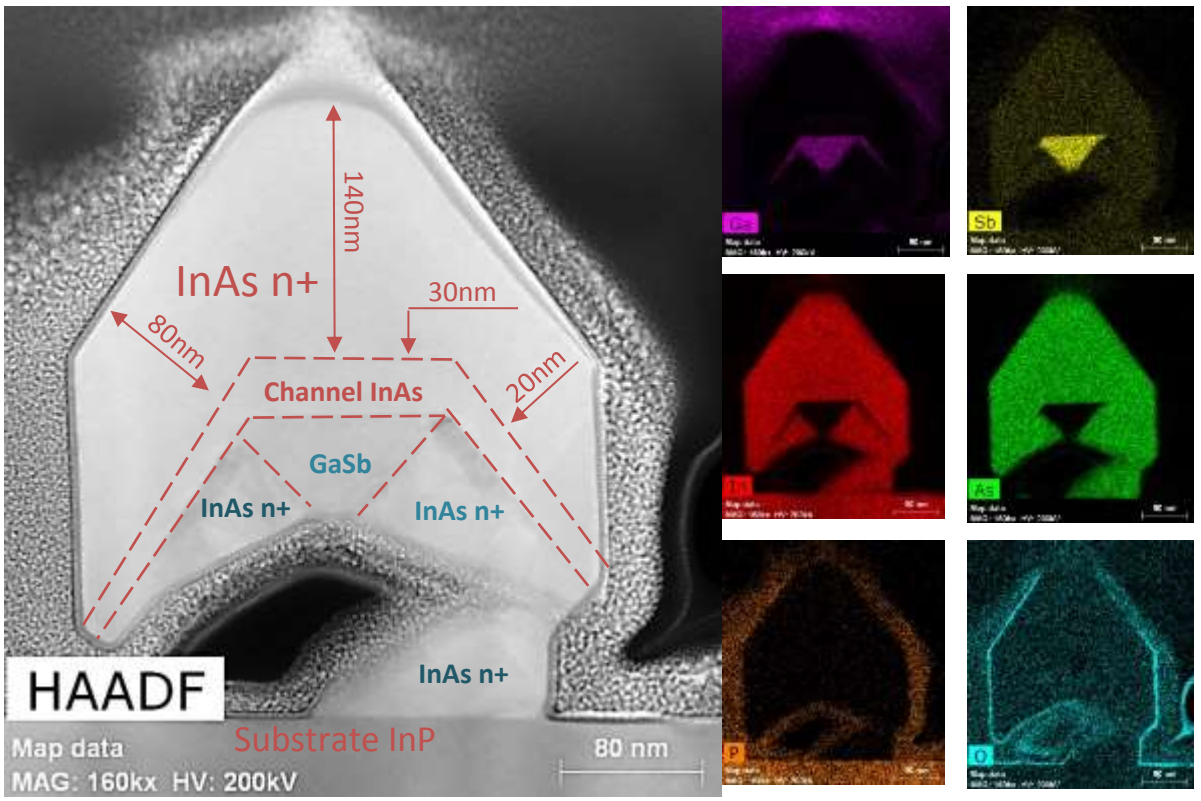


Figure 76: Cross-section HAADF image of the second selective epitaxy of InAs n+ contact oriented along [110] direction. (courtesy of Aurélien Olivier)

Figure 77: Cross section EDX images of the second selective epitaxy of InAs n+ contact oriented along [110] direction. The color of Ga, Sb, In, As, P and O spectre is purple, yellow, red, green, orange and blue respectively. (courtesy of Aurélien Olivier)

7 Conclusion

In this chapter we have described the most important steps of the III-V MOSFET process development. Firstly, we have presented different MOSCAPs that besides the original gate first recipe were exposed to different chemistries utilized during our UTB InAs MOSFET gate last process, including BOE and HSQ process. Extracted Densities of interface traps (D_{it}) are in the same order of magnitude as reported values of state of art III-V MOSFETs.

Furthermore, we have also described the contact fabrication whose cornerstone is the MBE localized selective epitaxy. The technology was successfully integrated into presented MOSFETs process in InAs n+ and InGaAs n+ version. Both are characterized by low contact and sheet resistances values.

Assembled gate stack and the contact module were then introduced into UTB MOSFET fabrication module. One of the most challenging issue was the hard mask adhesion on InP surface. This was resolved by modifying the surface chemistry. Besides, it was confirmed that the MOSFET process flow including various surface treatment does not cause the epi-layer roughening either epi-layer thinning which is one of the main preconditions for obtaining a high-quality oxide deposition. Improvements of the MOSFET fabrication process and design are possible and will be discussed in the last chapter.

In the last section was outlined the fabrication process of GAA (FinFET) InAs that contrary to UTB MOSFET is fabricated by two selective localized epitaxy. In the first study we have shown that the quality of the InAs channel and raised InAs n+ contacts is strongly related to the device orientation. In this regards, devices oriented [110] show the least material imperfections.

Chapter 3

1 Introduction

The main objective of the optimization work is to obtain a small gate length III-V MOSFET with a high-quality high-k oxide, low access resistance, low subthreshold swing, high I_{ON} and high I_{ON}/I_{OFF}. Optimization is illustrated on selected three generations of planar UTB InAs MOSFET and on one generation of FinFET InAs. The fabrication of each generation may slightly differ from the process illustrated in the second chapter (UTB MOSFET and GAA (FinFET) fabrication module) which will be emphasized for the concerned devices.

The methodology of the electrical measurements is as follows. Since the objective of the work is to fabricate a device for low power applications, the drain voltage is kept below 1V. Transfer G_M-V_{GS} and subthreshold characteristics log (I_D)-V_{GS} are measured for two drain voltage levels and that, 0.7V or 0.5V and 50mV or 100mV that are referred throughout this dissertation as a high drain and as a low drain voltage (bias) respectively. To a large extent, extremely scaled gate lengths MOSFETs suffered from the short channel effects. Therefore, to illustrate the leakage currents, the lower limit of measured V_{GS} may descend to -2V and in some exceptional cases to -4V. The upper limit of V_{GS} does not exceed 2V. For all devices are extracted principal electrostatic parameters such as V_{th}, SS and DIBL and these are plotted as a function of L_G. Extraction of the access resistances is performed once for each contact module, InAs n+ and InGaAs n+. Complementary microwave measurements performed on selected MOSFETs and FinFETs are not presented as an integral part of this manuscript and can be found in the **Appendix**.

2 First MOSFET generation

The first presented MOSFET is composed of a gate stack constituted of 4 nm Al_2O_3 high-k oxide plus e-beam evaporated Ti/Pt/Au metal. Besides, the device is formed with 150nm highly doped 1 x 19cm^{-3} InAs n+ source and drain raised contacts achieved in MBE chamber.

Removal of the high-k oxide from InAs n+ contact was performed in BOE solution which was followed by an electron beam evaporation of Ti/Pt/Au source and drain pads. Presented devices are oriented along [1-10] direction. The rest of the process is identical to the process detailed in the second chapter (UTB InAs MOSFET fabrication module). The key specifications of the process are summarized in **Figure 78**.

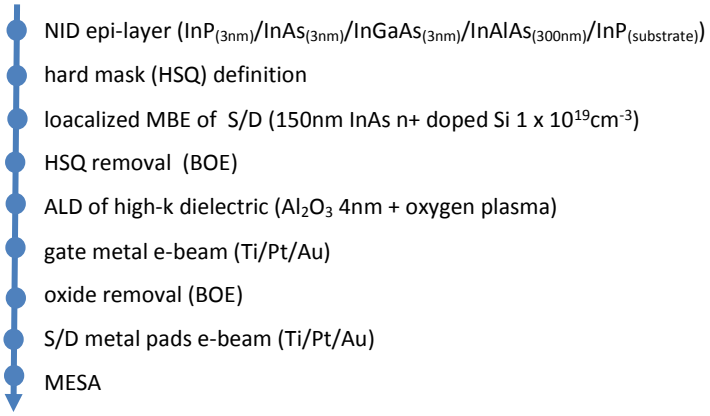


Figure 78: Key specifications of the 1st generation UTB MOSFET process

2.1 Impact of selectively raised S/D InAs n+ design

Since the raised source and drain InAs n+ contact exhibits a lattice mismatch with UTB epi-layer composed of InP substrate, its in-plane MBE growth will be characterized by a high surface roughness. As a result, this could potentially lead to an increase of the access resistance and obscure thus the intrinsic MOSFET performance. The localized growth of InAs n+ in HSQ hard mask apertures has been already discussed in the second chapter, section contact module. It has been observed that the quality of InAs n+ growth is strongly dependent on the HSQ aperture size. By reducing the HSQ aperture size, the quality of raised InAs n+ tends to improve which was found to have an impact on the MOSFET performance. To illustrate this effect, in the following section are compared two MOSFETs realized with different sizes of InAs n+ contact module.

The first studied case is MOSFET with 3x3µm^2 InAs n+ contact module that is characterized by a high surface roughness. **Figure 79a** gives SEM image of InAs n+ S/D raised contacts in 3x3 µm^2 hard mask apertures. The source and drain InAs n+ contacts are separated

by 50nm large HSQ dummy gate. We can notice that the surface of InAs n+ is characterized by a presence of growth defects. Most importantly, zones next to the dummy gate exhibit absence of InAs n+ growth.

Cross-sectional image of MOSFET utilizing the abovementioned contact design is provided in the **Figure 79b**. Due to the absence of InAs n+, the gate length defined as a distance between the edges of InAs n+ source and drain sidewalls exceeds HSQ dummy gate length of 50nm. Consequently, the effective gate length does not depend uniquely upon the resolution of HSQ resist but also on the quality of raised InAs n+ contacts. In addition, a high roughness of InAs n+ (**Figure 79a**) disables a precise gate length definition.

On the other hand, reducing the hard mask aperture to 1x3µm^2 leads to its optimal filling by InAs n+, notably characterized by a suppression of InAs n+ growth gap (**Figure 80a**). Then, InAs n+ S/D contacts are in a perfect alignment with respect to HSQ dummy gate allowing to obtain extremely small and reproducible gate lengths corresponding to the length of the HSQ dummy gate. In **Figure 80b** is presented a cross-sectional image recorded after the MOSFET fabrication. The measured gate length agrees well with HSQ dummy gate length designed to 50nm.

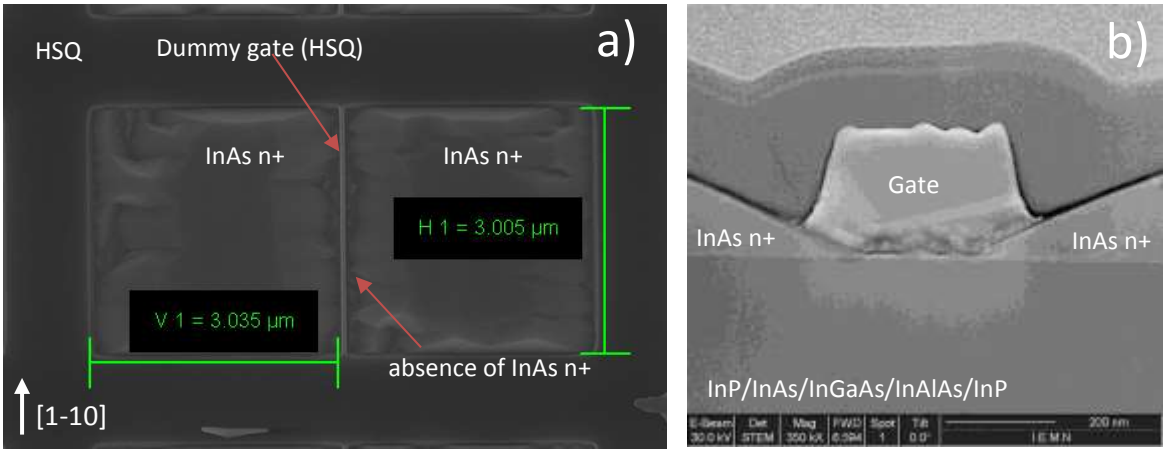


Figure 79: Top-down SEM image of 3x3 µm^2 HSQ apertures in which are selectively raised S/D InAs n+ contacts (**a**). Cross-sectional image of UTB InAs MOSFET realized with 3x3 µm^2 InAs n+ contact module. The gate length exceeds HSQ dummy gate length designed to 50nm (**b**)

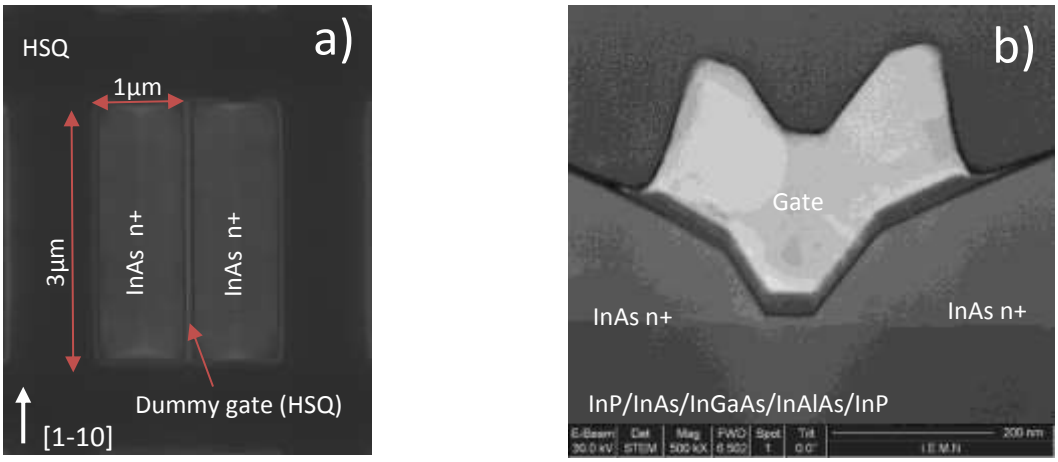


Figure 80: Top-down SEM image of 1x3 µm^2 HSQ apertures in which are selectively raised S/D InAs n+ contacts (**a**). Cross-sectional image of 50nm L_G UTB InAs MOSFET realized with 1x3 µm^2 InAs n+ contact module (**b**)

Electrical measurements of the mentioned MOSFETs are as follows. Analyzing firstly the output characteristics of MOSFET with InAs n+ 3x3µm^2 contact module (**Figure 81**). For a gate voltage (V_{GS}) of 2V and for a drain voltage (V_{DS}) of 0.7V device achieves a maximum on-state current of 360mA/mm. From the transfer characteristic presented in **Figure 82**, the peak transconductance achieves 250 mS/mm and 40mS/mm for V_{DS}=0.7 and 50mV respectively.

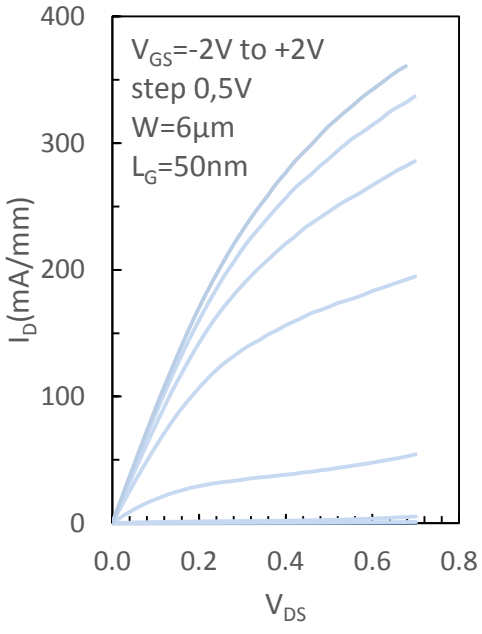


Figure 81: Output characteristics (I_D-V_{DS}) of 50nm L_G MOSFET with 3x3µm^2 InAs n+ contact module.

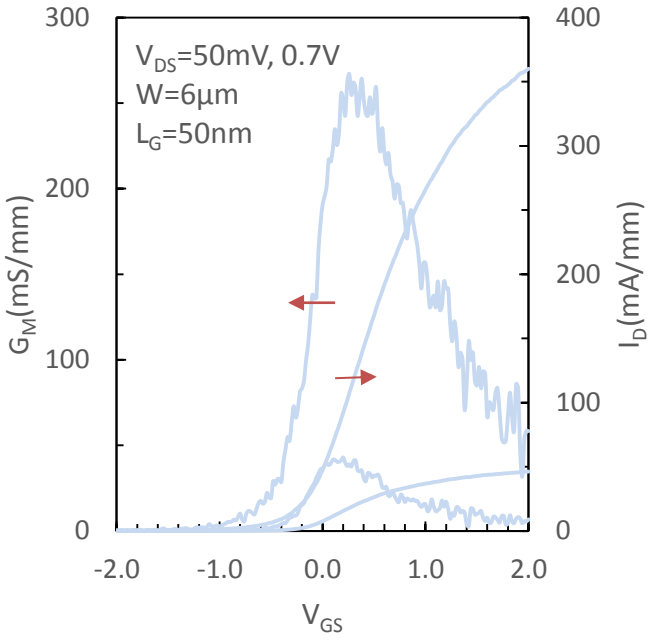


Figure 82: Transfer characteristics (I_D-V_{GS}) of 50nm L_G MOSFET with 3x3µm^2 InAs n+ contact module.

In contrast, a device with 1x3µm^2 InAs n+ contact module displays a high saturation current of 1300mA/mm biasing the device at V_{DS} of 0.7V and V_{GS} of 2V (**Figure 83**). This represents a current gain of 260 percent against 3x3µm^2 contact design. Similarly, the measured maximum transconductance achieves 910mS/mm and 153mS/mm at V_{DS}=0.7V and 50mV respectively (**Figure 84**).

Interpretation of the observed mismatch is as follows. As illustrated in **Figure 79**, the growth gap extends the distance between the source and drain contact InAs n+ that is related to the MOSFET gate length. Since a portion of electrons scatters in the channel a higher gate length will be translated in an increased channel resistance. Consequently, the device performance will be lowered what is observed as reduced on-state metrics. On the other hand, better performance of MOSFET with 1x3µm^2 contact can be attributed to the suppression of the growth gap providing a perfect alignment of InAs n+ sidewalls edges to HSQ dummy gate.

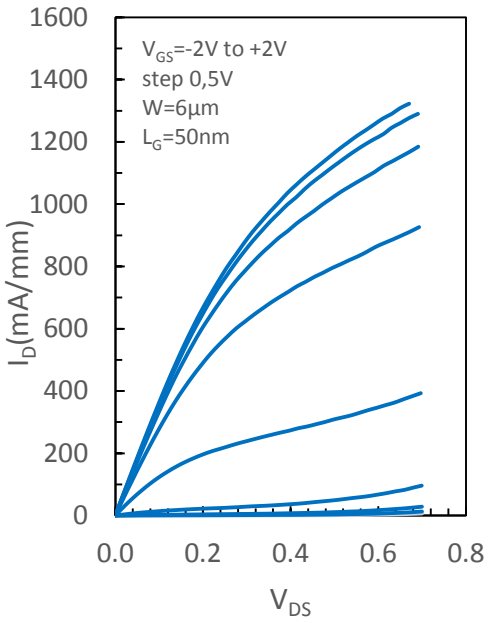


Figure 83: Output characteristics (I_D-V_{DS}) of 50nm L_G MOSFET with 1x3µm^2 InAs n+ contact module.

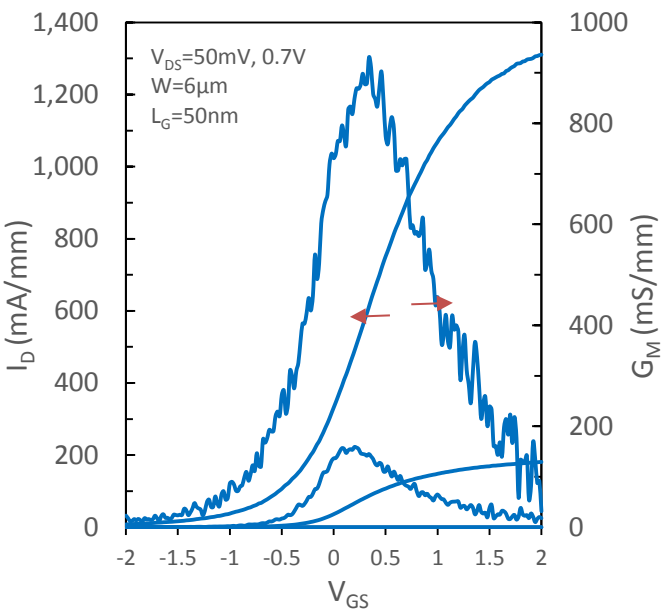


Figure 84: Transfer characteristics (I_D-V_{GS}) of 50nm L_G MOSFET with 1x3µm^2 InAs n+ contact module.

Since our intention is to fabricate a device with an aggressively scaled gate length to few dozens of nanometers, the inaccurate gate length precision, characteristic for MOSFET

with 3x3µm^2 contact module cannot be tolerated. Therefore, for the next analyses are selected uniquely MOSFETs equipped with 1x3 µm^2 InAs n+ contact modules providing a perfect gate length precision as well as satisfyingly high currents.

Analyzing the subthreshold characteristics of 50 nm gate length MOSFET (**Figure 85a**), we extract the lowest drain current (I_{min}) of 9mA/mm at V_{GS}=-2V and V_{DS}=0.7V. The ratio between the highest measured saturation current (I_{max}) and the lowest off-state current is 1.4 x 10^2. Further, the lowest subthreshold swing biasing the device at V_{DS}=0.7 is found 1200mV/dec while at V_{DS}=50mV this diminishes to 760mV/dec. Besides, the device shows a high Drain induced barrier lowering (DIBL) equal to 1400mV/V. Regarding the gate leakage current (**Figure 85a)**, this exhibits two orders of magnitude lower values than I_{min} (obtained at V_D=0.7V). Hence it can be excluded as a cause of the excessive drain leakage current.

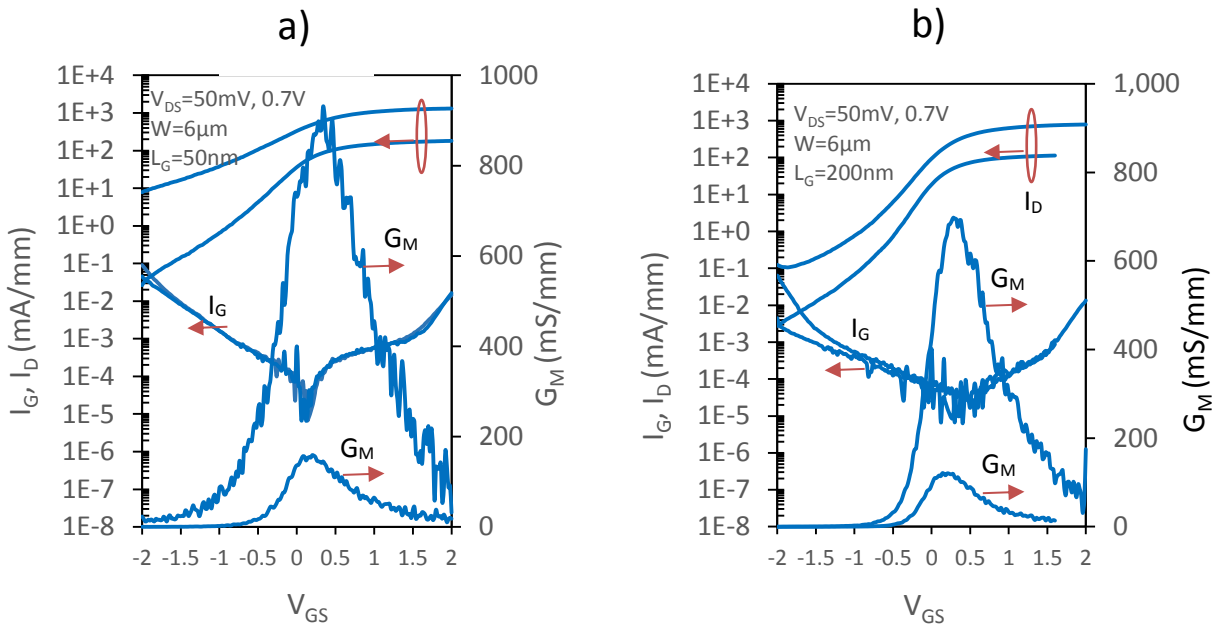


Figure 85: Subthreshold (log (I_D)-V_{GS}) and transconductance characteristics (G_M-V_{GS}) of **50nm** (**a**) and **200nm** (**b**) L_G UTB InAs MOSFET with 1x3µm^2 InAs n+ contact module.

Considering the subthreshold characteristic of 200nm L_G MOSFET plotted in the **Figure 85b,** the most important features are smaller values of minimal SS attaining 320mV/dec and 380mV/dec for V_{DS}=50mV and 0.7V respectively. Also, the difference between the SS obtained for high and low drain bias is lowered. Both features point to a better immunity against the Short Channel Effects against L_G=50nm MOSFET. As a result, a higher I_{max}/I_{min} ratio is obtained, equal to 6 x 10^3 for V_{DS}=0.7V. In terms of the gate current, this remains bellow 3x10^{-1}mA/mm

for 0.7V and alike 50 nm L_G MOSFET its weight in the overall I_D leakage current within voltage span (-1.5V, +2V) can be neglected.

As outlined, a relevant explanation of the improved off-state metrics obtained for 200nm against 50nm L_G MOSFETs is less important **Short Channel Effects (SCE).** In case of an inadequately scaled gate length, the impact of parasitic drain-channel capacitance (C_{GD}) cannot be neglected with respect to C_{OX}. (Detailed description of the MOSFET leakage mechanism is presented in the 1. Chapter: MOSFET off-state performance). This is translated in a diminished channel barrier height modulating the drain leakage current. In essence, the SCE explain the different subthreshold swings obtained for 50nm and 200nm L_G devices for a low drain bias (V_{DS}=50mV). Moreover, biasing the device at higher drain voltage V_{DS}=0.7V may magnify this effect. In this sense, one could argue that the important difference of the subthreshold swings of 50nm L_G MOSFET observed at V_{DS}=0.7 is due to the SCE (**Figure 85a**). However, that is not entirely true especially for the narrow bandgap channel.

Here another relevant leakage mechanism is also a Band to Band Tunneling (BTBT) currents that is in MOSFETs referred as **Gate-Induced Drain Leakage (GIDL)**. This occurs at the edge of the drain contact when the device is biased at high V_{DS} and negative V_{GS}. Since V_{GD}=V_{GS}-V_{DS}, for a given V_{DS}, decrease of V_{GS} increases the reverse voltage V_{GD}. Strong electric field on the drain InAs n+ corner induces an important band bending that triggers a hole-electron leakage tunnel current. Presence of this effect can be observed on 200nm L_G device (**Figure 85b**) where SCE leakage mechanism plays a less important role compared to 50 nm. For 50nm L_G MOSFET, GIDL leakage is logically more obscured by SCE. For 200nm L_G device, the current log(I_D)-V_{GS} does not descend with a constant slope but is slightly bent below V_{GS}=-0.5V.

In addition to this, in case of a confined channel, the BTBT amplifies the SCE what is called **Bipolar Gain Effect (**Hole Induced Barrier Lowering**).** A small hole (**tunnel**) current results in accumulation of holes in the confined UTB channel what pulls down the channel potential barrier generating a high electron leakage (**thermo-ionic**) current from the source to the channel. For a high drain bias, this leakage is presented in the subthreshold region and has the same signature as SCE as it affects the subthreshold swing. In this sense, the increase of the subthreshold wing observed for 50nm L_G MOSFET at a high drain bias (V_{DS}=0.7V) is considered as a coupled BTBT and short channel leakages.

Analyzing the electrostatic parameters extracted from 50nm 100nm and 200nm L_G MOSFETs (**Figure 86**). A characteristic feature of the first generation is an aggressive evolution

of the off-state metrics such as V_{th}, SS, DIBL with the gate length reduction. Namely, the technology presents a high ΔSS (V_{DS}=50mV) = 400mV/dec between 50nm and 200nm gate length devices. This for a small drain biases arises mainly from a bad electrostatic control. Assuming that the impact of the short channel effects is less prominent for 200nm. Then one could argue that the main cause of the high SS measured at a low drain bias is the presence of important D_{it} situated between the high-k oxide and InP semiconductor. This can be calculated by the subthreshold slope method utilizing the following expression:

$$D_{it} = C_{EOT}\left(\frac{SS}{2.3kT} - \frac{1}{q}\right) \quad (22)$$

Assuming that the relative permittivity of Al_2O_3 is 6.5, then the effective oxide thickness (EOT) is 2.4nm. Accordingly, for SS of 320mV/dec calculated D_{it} is $4x10^{13}$ $(eV)^{-1}.cm^{-2}$. This is few orders of magnitude higher than D_{it} extracted from the MOSCAPs by conductance ($3x10^{11}$) and HF-LF ($5x10^{12}$) method presented in the second chapter. The huge disagreement can be attributed either to a different extraction methodology or it is possible that the assumption that the 200nm L_G device is free of short channel effects was not right. To conclude, large subthreshold swing measured at the low drain biases for L_G=200nm points either to a high D_{it} or to a bad electrostatics combined with BTBT.

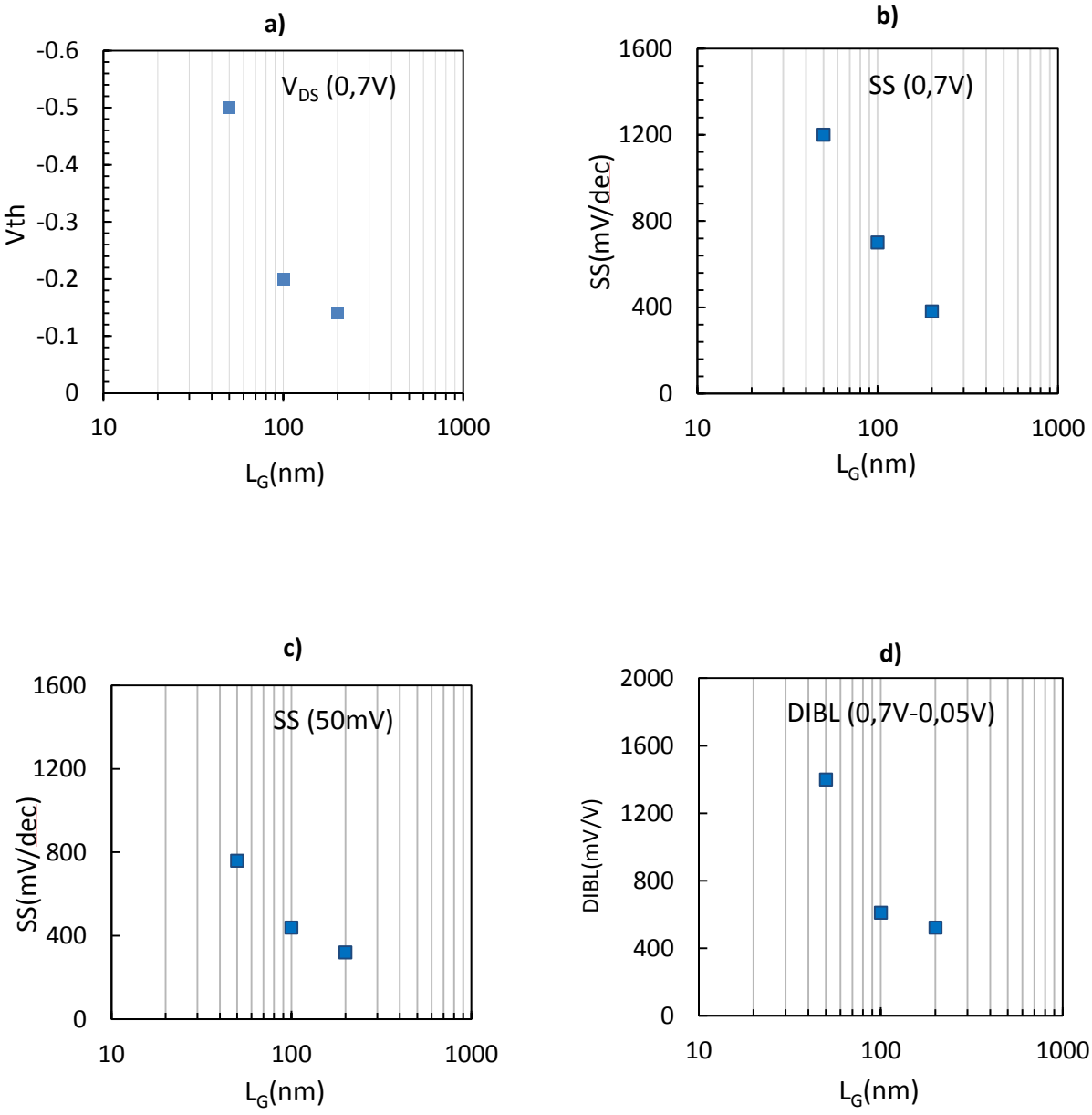


Figure 86: Plotted principal electrostatic parameters of 50, 100 and 200nm L_G MOSFET as a function of L_G. Threshold voltage (V_{DS} = 0.7V) (**a**), Subthreshold swing (V_{DS} = 0.7V) (**b**), Subthreshold swing (V_{DS} = 50mV) (**c**), Drain induced barrier lowering (V_{DS} = 50mV, 0.7V) (**d**).

3 Second MOSFET generation

In pursuit of a better electrostatic control, the second generation of UTB InAs MOSFETs was realized with a new oxide composed of a bilayer oxide Al_2O_3 / HfO_2 (2nm/2nm). Hafnium oxide provides a high dielectric constant which provides lower Effective oxide thickness (EOT). In **Figure 87** are presented examples of capacitance-voltage characteristics obtained from 2 MOSCAPs samples fabricated on InP wafer. The first contains 4nm Al_2O_3 and the second 2nm Al_2O_3 + 2nm HfO_2 oxide. It can be observed that the oxide replacement is followed by an enhancement of the control characterized by an increase of the maximum capacitance. This is explained by a higher dielectric constant of HfO_2. Accordingly, EOT can be calculated for each oxide taking into account the inversion capacitance C_{inv}^{DOS}. We find for the bilayer oxide Al_2O_3 + HfO_2 EOT of 1.9nm which represents a reduction of EOT equal to 0.9nm in comparison to Al_2O_3 4nm oxide (EOT=2.8nm).

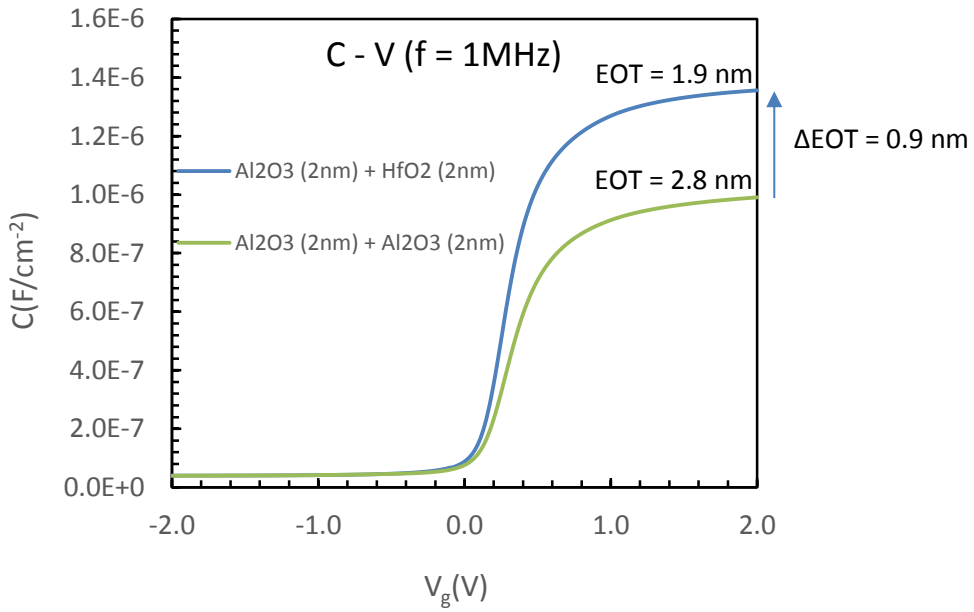


Figure 87: Capacitance-voltage curves (f = 1MHz) of MOSCAPs containing 4nm Al_2O_3 and 2nm Al_2O_3 + 2nm HfO_2 high-k oxides.

Integration of the bilayer oxide Al_2O_3 + HfO_2 into the MOSFET fabrication process is expected to provide an enhanced channel electrostatic integrity. When the gate capacitance increases, the portion of the channel controlled by the drain and source depletion region is

lowered, which should attenuate the previously discussed Short Channel Effects. This was identified as one of the reasons of the high off-state metrics reported for the extremely scaled gate length MOSFET.

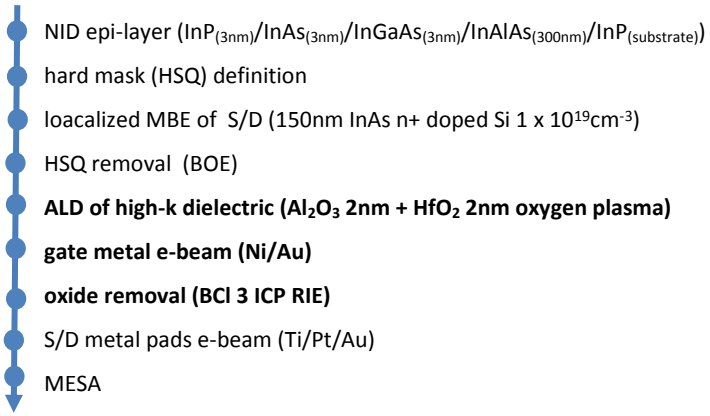


Figure 88: Key specifications of the 2nd generation UTB MOSFET process

Key specification of the fabrication process are provided in **Figure 88**. Further details of the fabrication process can be found in the second chapter (UTB InAs MOSFET fabrication module)

The modification of the gate stack oxide required optimization of the oxide removal from the InAs n+ surface. Prior to the metal pad deposition, oxide covering InAs n+ surface needs to be removed to enable connection between evaporated Ti/Pt/Au and raised InAs n+. However, contrary to Al_2O_3, thermally cured HfO_2 is not dissolved in BOE solution that was utilized in the first generation. Therefore, it was developed a dry etching process utilizing BCl_3 chemistry in ICP-RIE chamber.

Beyond this, the electron beam evaporated Ti/Pt/Au used in the first generation as the gate metal is replaced by an electron beam evaporated Ni/Au that is the most common gate metal stack reported for experimental III-V MOSFET.

Furthermore, the lithography mask was extended to an extremely small L_G =25nm and 1µm MOSFETs. The latter should provide a better approximation of the long channel MOSFET.

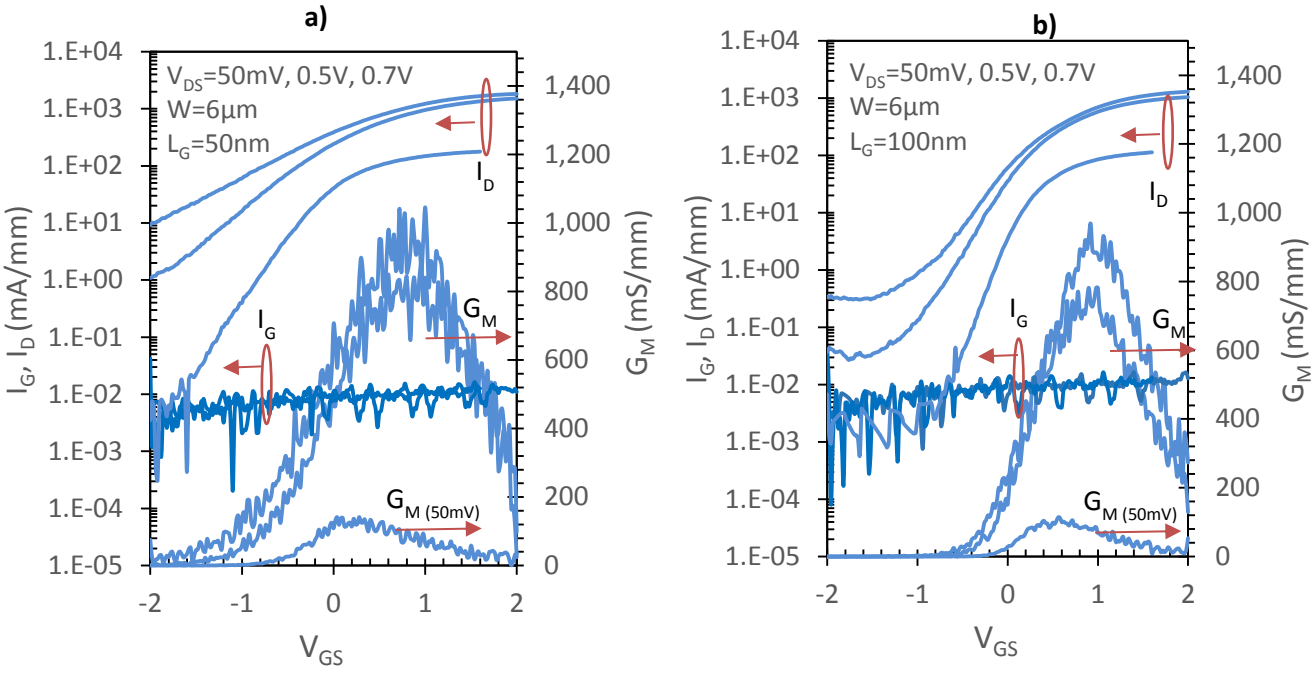


Figure 89: Subthreshold (log (I_D)-V_{GS}) and transconductance characteristics (G_M-V_{GS}) of **50nm (a)** and **100nm (b)** L_G MOSFET.

3.1 Bilayer oxide Al_2O_3 + HfO_2

Analyzing the subthreshold characteristic of 50nm L_G MOSFET depicted in **Figure 89a**. Biasing the device at V_{DS}=0.7V device exhibits a subthreshold swing of 1,2V/dec which is close to the previously reported device equipped with 4nm single layer Al_2O_3. The off-state current at V_{DS}=0.7V displays very similar values of 9mA/mm. Improvement of the electrostatic control is obtained for V_{DS}=50mV where the SS reaches 420mV/dec. As a result, the off-state current is decreased by around one order of magnitude in comparison to 4nm Al_2O_3 MOSFET. Also, the ratio between I_{max}/I_{min} at this drain voltage level presents an improvement of one order of magnitude. For V_{GS} < -1.8V the value of the drain leakage attains a floor level of 6 x 10^{-3}mA/mm which is attributed to a dominating gate leakage current.

Analyzing the subthreshold characteristics of 100nm L_G MOSFET is displayed in the **Figure 89b**. This presents a subthreshold swing of 260mV/dec and 480mV/dec for V_{DS} of 50mV and 0.7V respectively. The device presents off-state currents of 3x10^{-1}mA/mm and 1x10^{-3}mA/mm for V_{DS} 0.7V and 50mV. The values of the off-state current obtained for 100nm L_G MOSFET are comparable with the previously reported 200nm MOSFET equipped with 4nm

Al_2O_3. In this sense, a better scalability strongly suggests a better electrostatic control enabled by a bilayer Al_2O_3+HfO_2 oxide.

On the other hand, replacement of the Al_2O_3 (4nm) oxide by a bilayer of Al_2O_3 (2 nm) + HfO_2 (2 nm) is followed by an increase of the gate leakage by around one order of magnitude within the V_{GS} voltage span of -1V and +1V. Nevertheless, the gate leakage remains still three decades lower than the state of art InGaAs HEMT [108]. In **Figure 90**, the main electrostatics parameters are displayed versus the gate length.

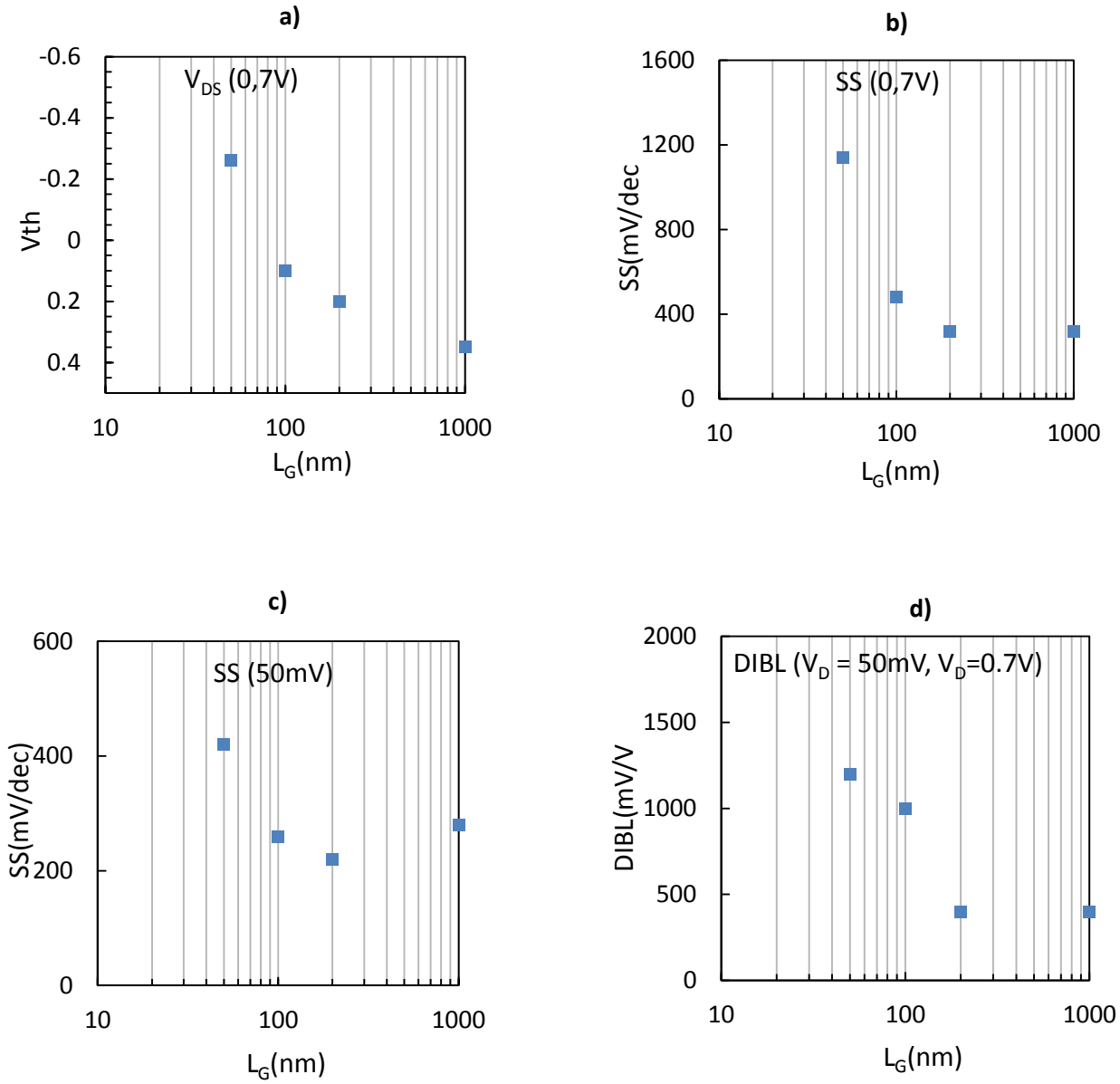


Figure 90: Principal MOSFET electrostatic parameters. Threshold voltage (V_{th}) extracted at V_{DS}=0.7V (**a**), Subthreshold swing (SS) extracted at V_{DS}=0.7V (**b**), Subthreshold swing extracted at V_{DS}=50mV (**c**), drain induced barrier lowering (DIBL) extracted at V_{DS}=50mV and 0.7V (**d**).

3.2 Hybrid device orientation

Besides the [1-10] oriented MOSFETs, on the wafer were placed devices oriented along [110] and [100] directions. Among the studied devices, an important difference was observed for 25nm L_G MOSFETs. Discussion of the observation is provided in the following.

Analyzing first of all the output characteristics of 25nm L_G MOSFET oriented along [1-10] direction (**Figure 91a**). The device shows a high maximal drain current 2000 mA/mm at V_{GS} of 2V and V_{DS} of 0.7V. On the other hand, the device is unable to close the channel even when biased at high negative voltages. The subthreshold characteristics are depicted in **Figure 91b**. The device shows a high SS of 1V/dec at V_{DS}=50mV.

Unlike [1-10] oriented device, the device oriented along [110] direction shows a lower saturation current of 1500mA/mm and a higher off-state current that achieves for V_G=-2V extreme 300mA/mm (**Figure 92a**). Equally, the device displays an important subthreshold swing for both drain biases exceeding 2V/dec what disables a correct extraction of DIBL (**Figure 92b**). Poor switching properties can be most likely classified as a “Punch through” effect that occurs when the drain and source depletion regions merge together causing a strong leakage current. This becomes strongly dependent on the drain voltage leaving the channel control almost insensitive to the gate bias.

Among the studied directions, the device oriented along [100] direction exhibits the best electrical properties. The devices display a high saturation currents of 2300mA/mm measured at V_{GS}=+2V (**Figure 93a**) as well as the best switching characteristics including SS, DIBL (**Figure 93b**). However, these remain still important as SS attains 620mV/dec (V_{DS}=50mV) and DIBL exceeds 2V/V.

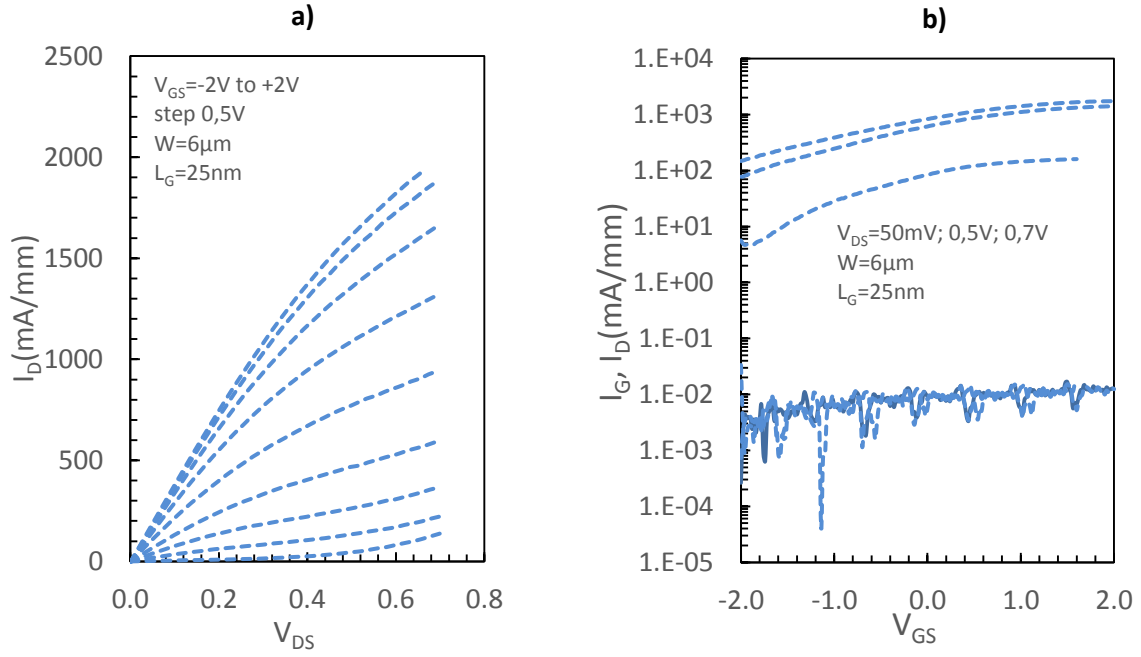


Figure 91: Output characteristics (I_D-V_{DS}) (**a**) and Subthreshold characteristics (log (I_D)-V_{GS}) (**b**) of 25nm L_G MOSFET oriented along [1-10] direction.

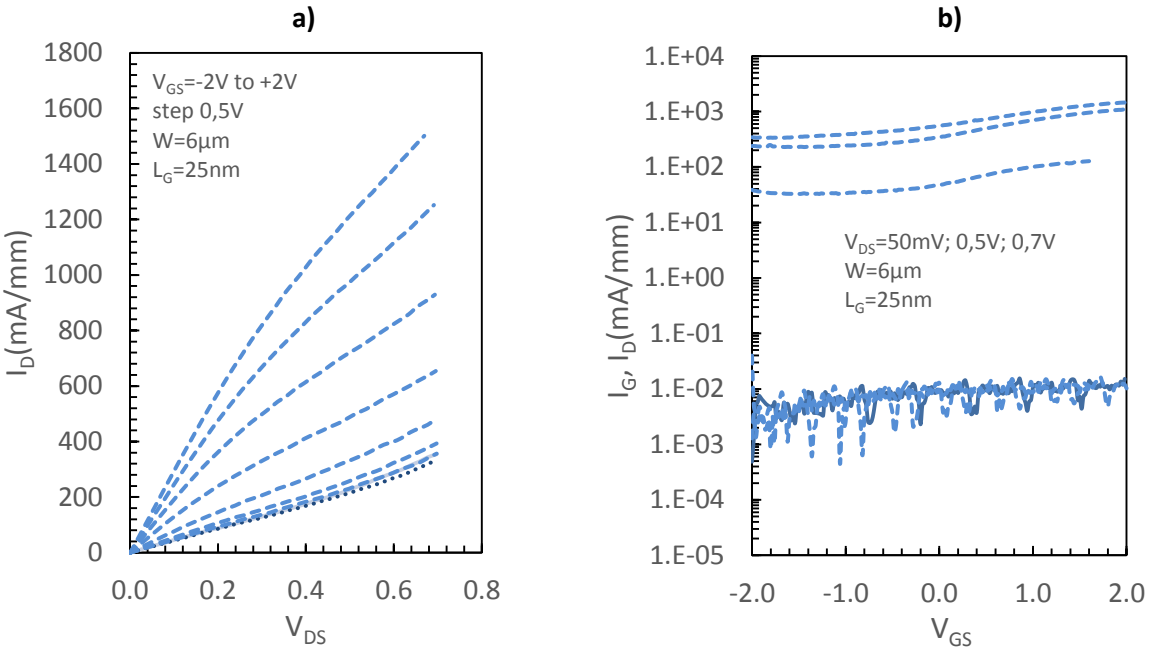


Figure 92: Output characteristics (I_D-V_{DS}) (**a**) and Subthreshold characteristics (log (I_D)-V_{GS}) (**b**) of 25nm L_G MOSFET oriented along [110] direction.

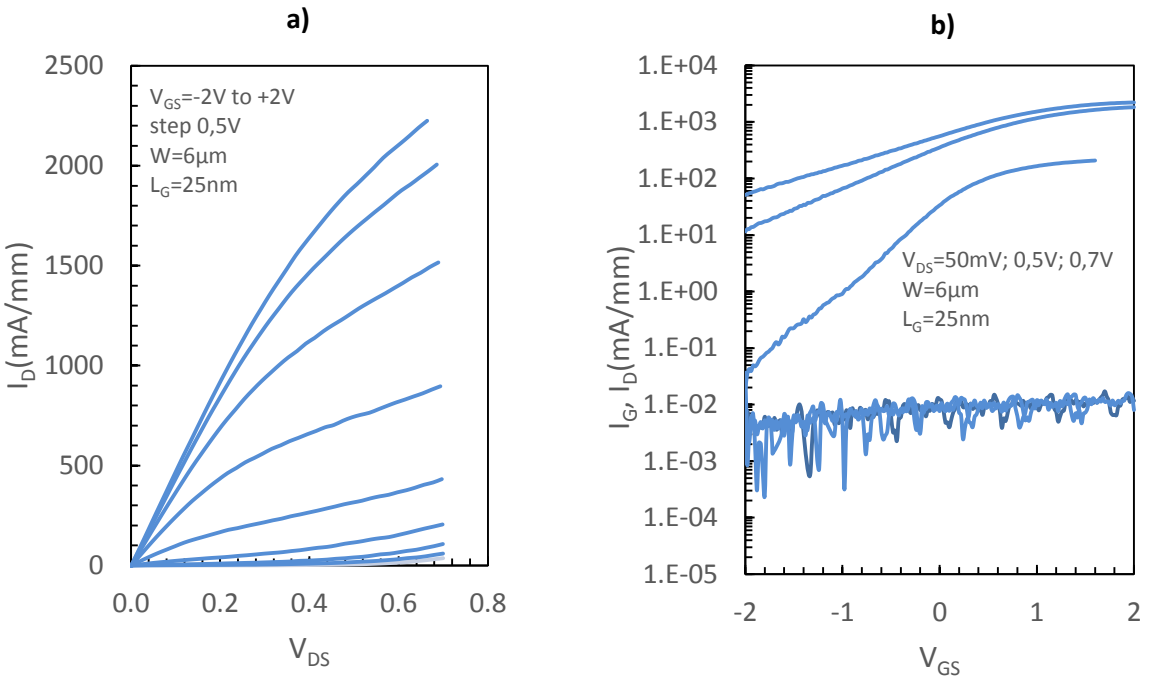


Figure 93: Output characteristics (I_D-V_{DS}) (**a**) and Subthreshold characteristics (log (I_D)-V_{GS}) (**b**) of 25nm L_G MOSFET oriented along [100] direction.

Considering the electrostatic parameters extracted from 25nm, 50nm, 100nm, 200nm and 1µm L_G MOSFETs oriented along the examined directions [100], [1-10] and [110] (**Figure 94**). Scaling down the gate length is accompanied by a rapid increase of SS and DIBL. Among the studied direction, the effect is most prevailing for [110] oriented MOSFET. For instance, the ΔSS (V_{DS}=50mV) of [110] oriented MOSFET is 1300 mV/dec whereas for [100] ΔSS represents only 400mV/dec. The difference of the off state metrics between [100] and [110] oriented MOSFET is observed uniquely for 25nm gate length MOSFET.

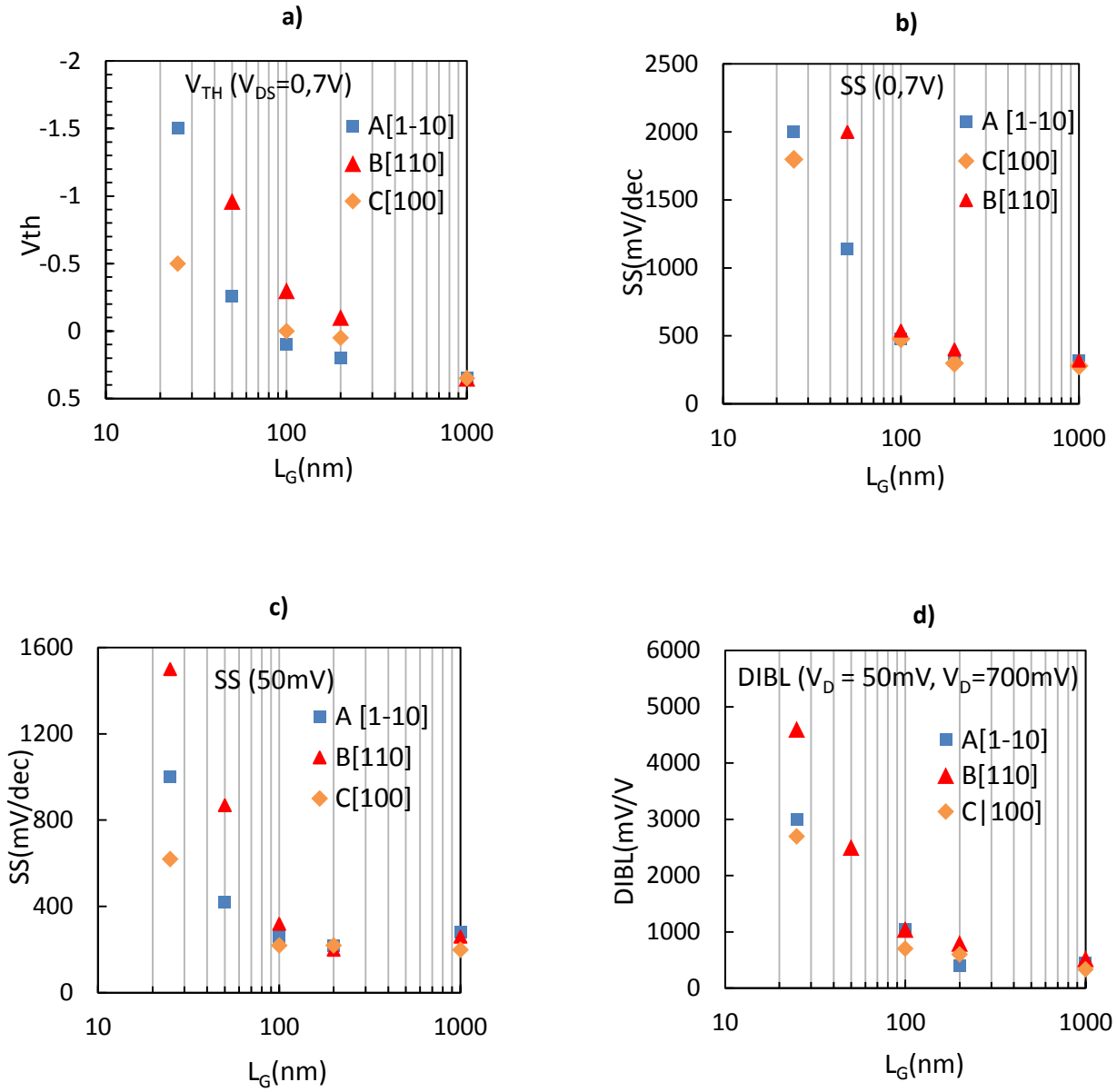


Figure 94: Main MOSFET electrostatic parameters. Threshold voltage (V_{th}) extracted at V_{DS}=0.7V (**a**), Subthreshold swing (SS) extracted at V_{DS}=0.7V (**b**), Subthreshold swing extracted at V_{DS}=50mV(**c**), Drain induced barrier lowering (DIBL) extracted at V_{DS}=50mV and 0.7V (**d**).

Given the complexity of parameters that may have been affected by the hybrid MOSFET orientation, it is not trivial to interpret the observed phenomenon. Nevertheless, one of the relevant explanation may be points to InAs n+ contact module exhibiting a sidewall shaping that is unique for each direction. As illustrated in **Figure 95**, the highest angle between InAs n+ sidewall and the (001) substrate is measured for [110] oriented MOSFET. We remind, that the worst immunity against the short channel effects was observed for the devices oriented along [110] direction. On the other hand, the lowest angle is characterized for [100] oriented MOSFET displaying the best off-state metrics. For the following studies were selected devices oriented uniquely along [100] direction.

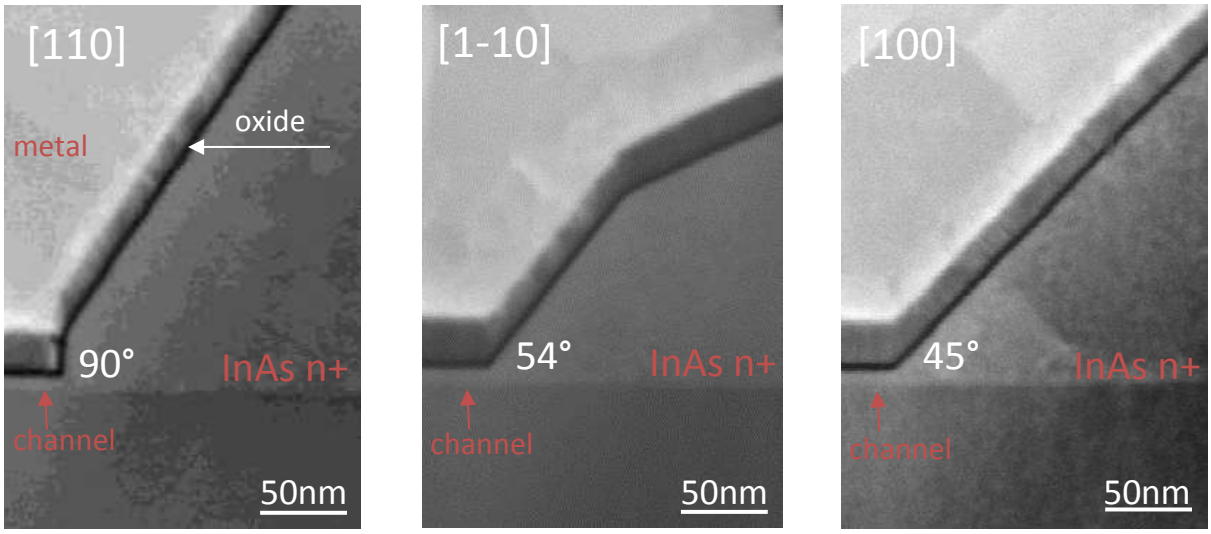


Figure 95: Cross-section STEM images of MOSFETs oriented along [110], |1-10] and [100] direction with depicted InAs n+ sidewall angles.

Regardless of the orientation, the long gate devices (L_G=1µm) present very similar off state metrics (**Figure 94**). The subthreshold swing obtained at 50mV is 200mV/dec. Assuming that the discrepancy between the theoretical value of SS=60mV/dec and the measured SS (V_{DS}=50mV) is caused uniquely by the presence of interface traps. Then, D_{it} can be extracted by the subthreshold slope method and we find for EOT = 1.9nm D_{it} = 2.7 x 10^{13} $eV^{-1}cm^{-2}$. However, this remains one decade higher than D_{it} reported for the state of arts III-V MOSFET as well as D_{it} extracted from the MOSCAPs reported in the second chapter.

3.3 Impact of epi-layer quality

Abnormally high off-state metrics reported for the previous series of MOSFETs may point to a different leakage mechanism rather than an important density of oxide/semiconductor interface traps. It should be reminded that the utilized epi-layer includes InAs channel that is grown in a strain mode. This is characterized by the creation of elastic energy that upon certain conditions such as exceeding InAs critical thickness (3nm) may be released leading thus to a formation of epi-layer material defects**.** Hence**,** it is reasonable to verify the impact of the UTB epi-layer quality on the device performance.

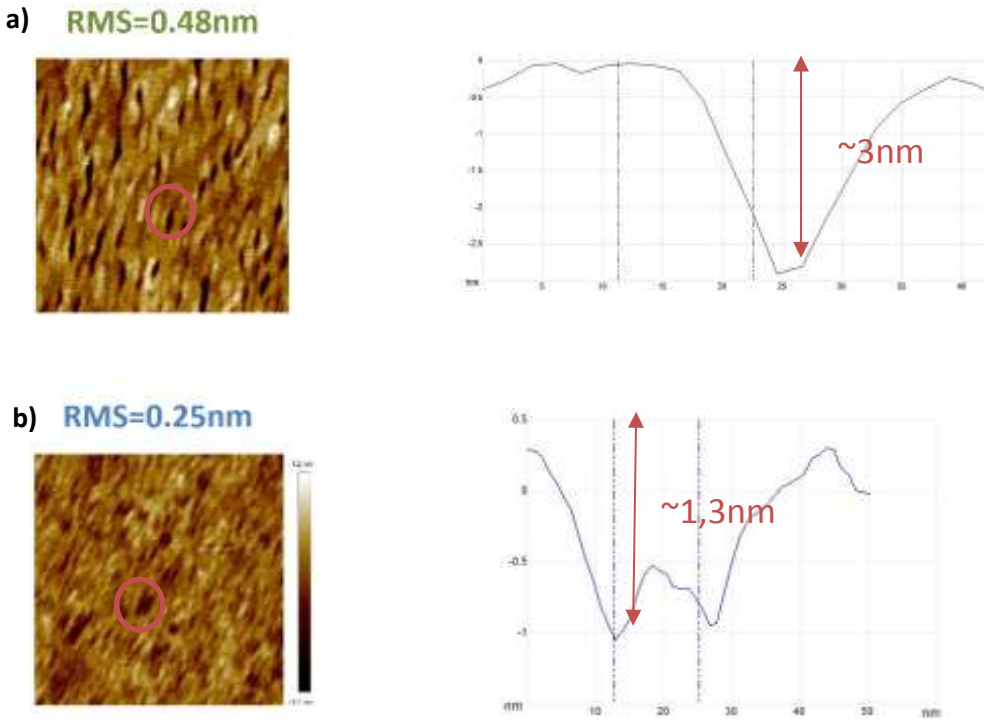


Figure 96: AFM surface scan on epitaxial layer InP/InAs/InGaAs/InAlAs/InP with RMS values **0.48nm** (**a**) and **0.25nm** (**b**). The scanned area is 0.5 x 0.5 µm².

In the (**Figure 96a**) is provided AFM surface scan of the UTB epi layer utilized for the fabrication of the last series of MOSFETs. The root mean square roughness (RMS) is equal to 0.48nm. In addition to this, the surface scan is characterized by a presence of “holes” whose typical diameter and depth is 16nm and 3nm respectively. The latter value may be underestimated due to a limited AFM cantilever geometry that does not allow to scan the

entire defect profile. It should be noted, that RMS value of 0.48nm is higher than those reported for III-V MOSFETs. For instance, epi-layers fabricated by IntelliEpi Inc. utilized in MIT's state of art MOSFETs (del Alamo's group) exhibits RMS = 0.17nm [103].

To remedy this issue, our close collaborator Epiphy group at IEMN optimized the epi-layer growth conditions and fabricated a new epi-layer with an improved RMS roughness of 0.25nm. Its surface scan is presented in the **Figure 96b**. Beside a lower roughness, the surface is characteristic by a reduction of the hole depth to 1.5nm.

The epi-layer was utilized to fabricate a duplicate of the last presented MOSFET. After the device fabrication was performed inspection of the epi-layer profile by means of a high-resolution TEM that is displayed in **Figure 97**. Visual inspection of the channel cross-section confirms a good quality of the new epi-layer. Nevertheless, a clear differentiation between InAs and InP layer seems to be difficult. Estimated thickness of InAs + InP is approximately ~ 5nm what is slightly lower than expected 6nm. Thinning can be attributed to the top InP layer exposure to different chemistries prior to the oxide deposition. (More information on that topic can be found in the second chapter: UTB InAs MOSFET fabrication module: Impact of selected wet chemical treatments on UTB epi-layer)

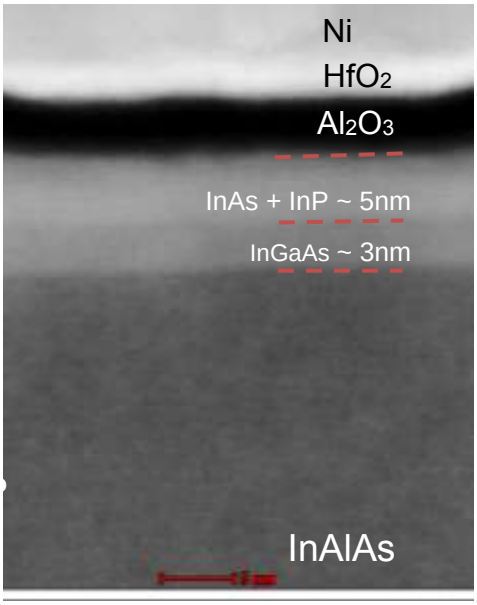


Figure 97: Cross-sectional high resolution TEM image of InP/InAs/ InGaAs/InAlAs/ epi-layers on InP substrate recorded after the device fabrication.

Electrical measurements performed on the MOSFETs are discussed in the following**.** In **Figure 98** are illustrated transfer log (I_D)-V_G characteristics of 100nm L_G MOSFET fabricated on both epi-layers (**RMS=0.48nm and RMS=0.25nm**). Improved epi-layer quality (**RMS = 0.25nm**) results in a lower minimal drain current $8x10^{-2}$mA/mm obtained at V_{DS}=0.5V and V_{GS}=-0.8V. This represents an improvement of 2 decades over MOSFET utilizing epi-layer (**RMS = 0.48nm**). Moreover, the device presents I_{max}/I_{min} ratio of 10^5 for V_{DS} of 0.5V what represents an improvement of one decade. Better electrostatic control can be also illustrated by lowered subthreshold swings that approaches a reasonable level of 100mV/dec and 140mV/dec for V_{DS}=50mV and 0.5V respectively. Further, the device meets the off-state current required for high-performance CMOS applications (I_{OFF}=0.1mA/mm) at V_G=-0.7V. The device provides also ΔV_{TH} shift (V_{DS}=50mV and 0.5V) of 0.15V.

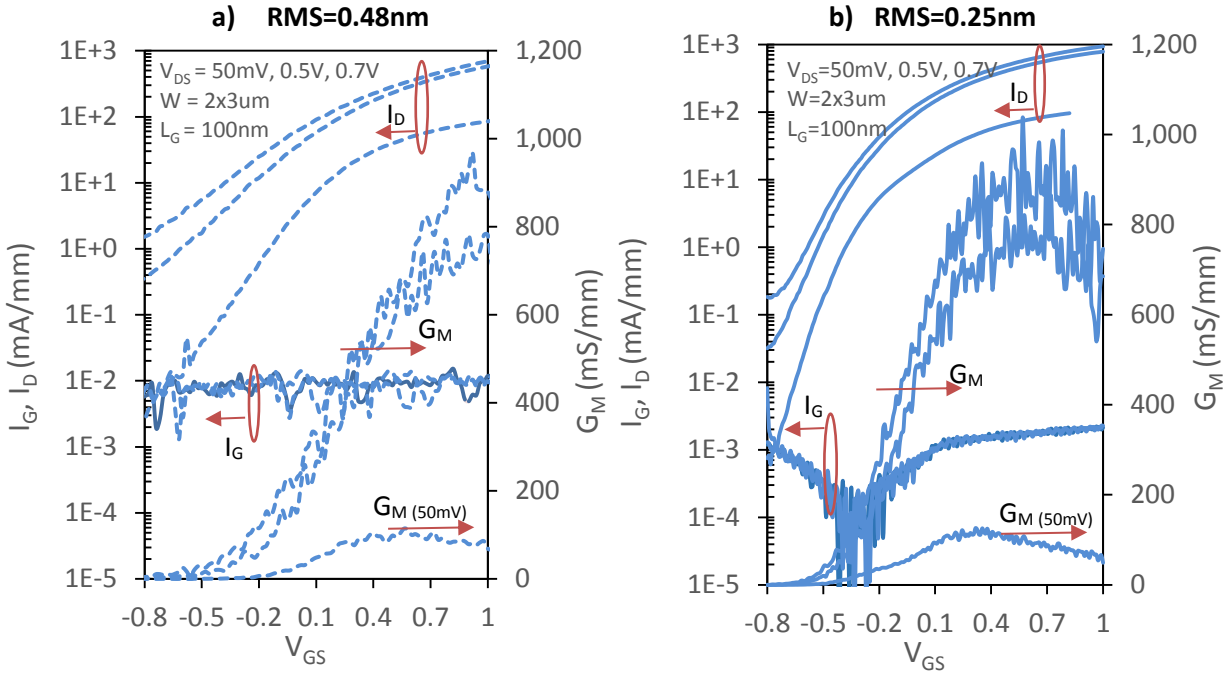


Figure 98: Subthreshold (log (I_D)-V_{GS}) and transconductance characteristics (G_M-V_{GS}) of L_G=100nm MOSFET grown on epi-layer of RMS roughness of **0.48nm (a)** and **0.25nm (b).**

Accordingly, the DIBL is 330mV/V between the drain biases of 50mV and 0.5V what presents a reduction by 400mV/V against MOSFET (**RMS = 0.48nm**). Similar behavior was observed on the whole set of fabricated L_G.

In **Figure 99** are benchmarked principal MOSFET electrostatic parameters as a function of L_G. For the extremely reduced gate length of 25nm was achieved a slight improvement of SS descending from 620mV/dec (**RMS=0.48nm**) to 400mV/dec (**RMS=0.25nm**) at V_{DS}=50mV. The series of MOSFETs (**RMS=0.25nm**) presents a considerable suppression of the short channel effects between L_G of 50nm and 1µm. Regarding MOSFET of 50nm L_G, this provides SS of 200 mV/dec and 130mV/dec for V_{DS}=0.5 and 50mV respectively. These are ones of the lowest values reported in this dissertation. The long gate MOSFETs (L_G=1µm) present low off-state metrics including a low DIBL of 40mV/V (V_{DS}=50mV and 0.5V) but also a low SS (V_{DS}=50mV) of 90mV/dec which represents an improvement of 100mV/dec against MOSFET (**RMS = 0.48nm**).

The smaller leakage of MOSFETs (**RMS = 0.25nm**) strongly points to the improvement of epi-layer quality. It is known that the epi-layer non-idealities such as dislocations are electrically active. These may introduce new energy states within the band gap [109] that from the electrostatic perspective cause the channel Fermi level pinning or BTBT trap-assisted tunneling.

In this situation, one could argue that the reported values of density of interface traps (D_{it}) extracted from 1µm L_G MOSFET **(RMS = 0.48nm)** were to a large extent overestimated as these involved a contribution of the leakage current associated with the epi-layer nonidealities. This as evidenced, affects the subthreshold swing. Supposing now that the subthreshold leakages associated with the epi-layer nonidealities can be neglected, we can calculate again D_{it} from the subthreshold swing of 1µm L_G MOSFET **(RMS = 0.25nm)** and we find for EOT=1.9nm D_{it}= 5.9 x 10^{12} $(eV)^{-1}$ cm^{-2}. This is in a good agreement with the highest D_{it} of 5 x 10^{12} $(eV)^{-1}$ cm^{-2} extracted from the MOSCAPs reported in the second chapter as well as close to a typical D_{it} of 3 x 10^{12} $(eV)^{-1}$ cm^{-2} reported for state of art III-V MOSFETs [61].

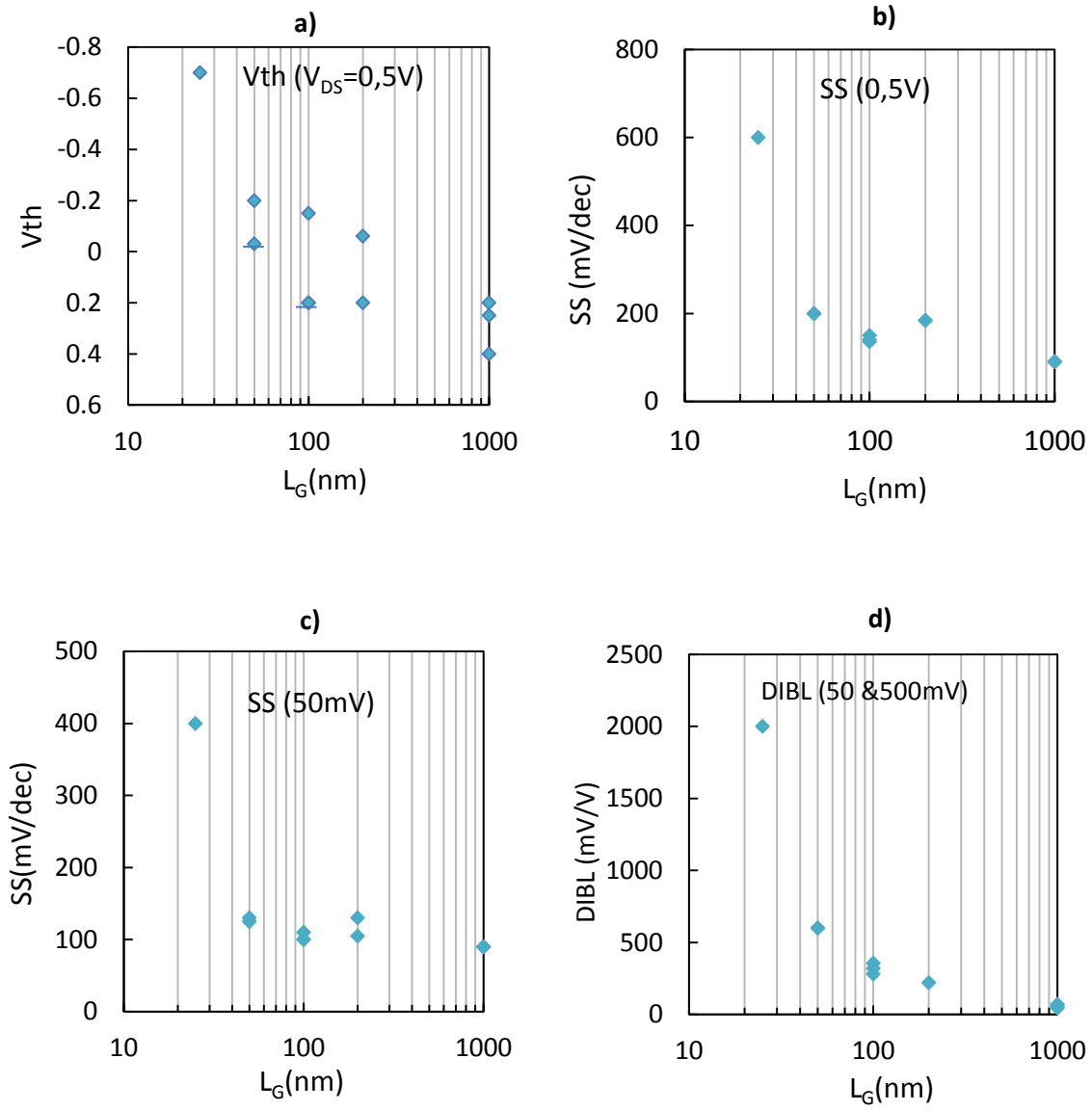


Figure 99: Principal MOSFET (**RMS=0.48nm**) electrostatic parameters. Threshold voltage (V_{th}) extracted at V_{DS}=0.5V (**a**), Subthreshold swing (SS) extracted at V_{DS}=0.5V (**b**), Subthreshold swing extracted at V_{DS}=50mV (**c**), Drain induced barrier lowering (DIBL) extracted at V_{DS}=50mV and 0.5V (**d**).

3.4 Decomposition of UTB InAs MOSFET source and drain InAs n+ access resistance

On the presented device is carried out extraction of the access resistance (R_{ACCESS}) (**Figure 100a), (Figure 100b)**, its decomposition (**Figure 100c)** and presentation of the decomposed elements of R_{ACCESS} **(Figure 100d)**.

The extraction of R_{ON} is carried out driving the device in I_D-V_{DS} linear region (V_{DS}=50mV) while V_{GS} is biased at $V_{GS} = V_{th} + 2V$. The R_{on} is then plotted as a function of L_G (**Figure 100b)**. Extrapolating the curve R_{ON} (L_G) to L_G=0 is determined the intersection with y-axis R_{ON} (L_G=0) giving 2 x R_{ACCESS}.

In the second chapter was mentioned that the resistance model of the contact module is constituted primarily of two elements and that semiconductor resistance ($R_{InAs\ n+}$ (MOSFET)) and the metal/semiconductor junction resistance ($R_{InAs\ n+/metal}$ (MOSFET). These are obtained from Transmission line method **(Figure 100a)**. Since the length of MOSFET metal/InAs n+ contact L_C =220nm is smaller than TLM transfer length L_T=600nm (L_C<L_T), the MOSFET contact resistance ($R_{InAs\ n+/metal}$(MOSFET) has to be recalculated with respect to L_c (MOSFET), L_T(TLM) as [110]:

$$R_{\mathrm{InAs\ n+/metal}}(\mathrm{MOSFET}) = R_{\mathrm{InAs\ n+}}(\mathrm{TLM}).L_{\mathrm{T}}\coth\frac{L_{\mathrm{C}}\ (\mathrm{MOSFET})}{L_{\mathrm{T}}\ (\mathrm{TLM})} \qquad (23)$$

Where the sheet resistance $R_{InAs\ n+}$ (TLM) obtained from TLM is equal to 30Ω/Sq and the metal/semiconductor junction resistance ($R_{InAs\ n+/metal}$ (TLM) is equal to 18Ω.µm. The resistance associated with the carrier transport through raised InAs n+ ($R_{InAs\ n+}$ (MOSFET) is obtained by multiplying the sheet resistance $R_{InAs\ n+}$ (TLM) obtained from TLM with the distance L(MOSFET)=800nm indicated in the picture (**Figure 100a)**. This represents a spacing between the contact metal edge and the channel edge. The contribution of both terms $R_{InAs\ n+}$(MOSFET) and $R_{InAs\ n+/metal}$(MOSFET) is equal to 80Ω.µm what is surprisingly smaller than R_{ACCESS} of 131Ω.µm (**Figure 100b)**. The mismatch of 51Ω.µm is due to the architecture of the channel that extends the access resistance model to a new term that we will call an interface resistance (R_{Int}).

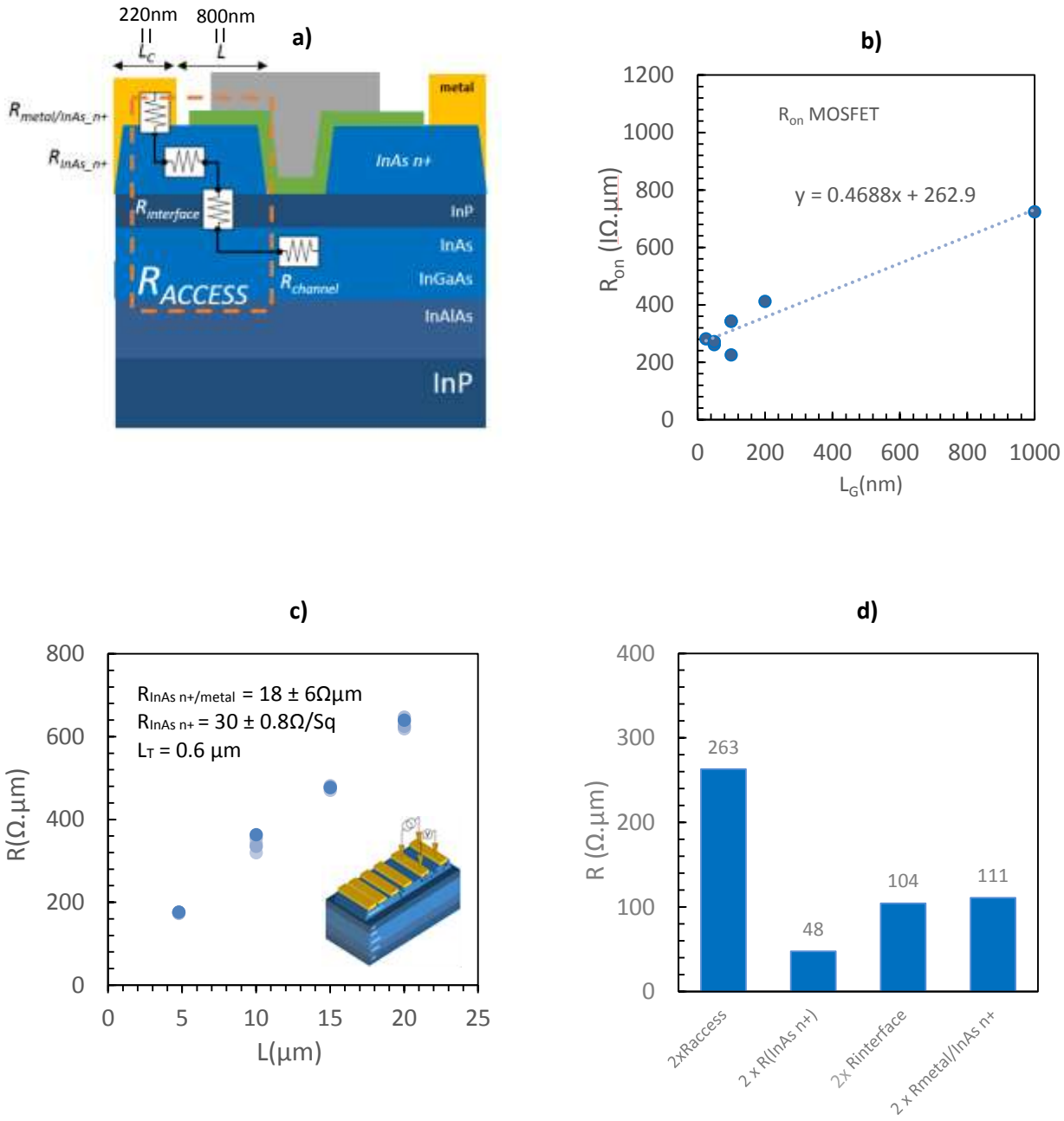


Figure 100: Illustrated model of one side access resistance (**a**) Plotted R_{ON} as a function of L_G. (**b**) Plotted R obtained from the TLM structure (**c**) decomposed elements of the access resistance (**d**).

3.5 Interface and Ballistic resistance

Interface resistance (R_{int}) denotes the contribution of a so-called ballistic resistance and a resistance of InP barrier layer that acts as a potential barrier between InAs n+ contact and InAs channel. In a published work [111] was evidenced that in fact 3nm of InP can be considered quasi-transparent for electrons. Therefore, the interface resistance can be explained merely by the ballistic resistance.

Ballistic or also Landauer resistance has already been reported for SOI MOSFET [112] but also on III-V MOSFET [113]. A common feature of both devices is an ultra-thin-channel (below 10 nm) leading to 2D carriers confinement. It is important to note that the ballistic resistance does not depend on the gate length. The reason why it is called ballistic resistance is that it is easier to put it into evidence on an extremely scaled FET where the diffusive losses are neglected. In a long gate device, the dominance of diffusive losses disables to observe the ballistic resistance. Its physical significance is as follows.

In an extremely thin 2D (UTB or SOI) channel the quantum mechanics effects gain on importance what lowers the density of states being proportional to the carrier sheet concentration. In a language of Landauer formalism, very large number of modes (carrier concentration in the source and drain reservoir) are then conducted by few modes (low carrier concentration in the channel). Then the losses in device conduction due to the channel quantum confinement can be quantitatively explained as [113]:

$$R_B = \frac{2\Phi_T}{v_{t0} q N_S} \frac{F_0(\eta)}{F_{-1/2}(\eta)} \tag{24}$$

Where Φ_T is the thermal voltage, N_s is the sheet carrier concentration, v_{t0} is the thermal velocity, η is the reduced surface potential and F_0 and $F_{-1/2}$ are Blackmore Fermi-Dirac integrals whose ratio accounts for the carrier degeneracy. The effect of R_B is more pronounced for III-V materials than for Si as they are penalized for their low effective mass what diminishes more the carrier sheet concentration and raised thus the R_B. Assuming that $R_B = 2 \times R_{int}$ = 104Ω.µm and utilizing the abovementioned equation, we determine the carrier concentration in the channel 2 x 10^{12} cm^{-2}. To lower the ballistic resistance, one can propose to introduce

beneath the channel a doped n+ plane that increases N_S. For instance, increasing the carrier sheet concentration N_S to 1 x 10^{13} cm^{-2}, the ballistic resistance can be diminished to 60Ω.µm.

4 Third MOSFET generation

The most significant change in the third generation of MOSFET is the introduction of 100nm thick InGaAs n+ contact module raised by MBE. There exists a concern that the growth of InAs n+ contact module being in lattice mismatch with the epi-layer can lead to a presence of channel dislocation that may be electrically active. Except for InGaAs n+ contact module, the fabrication was realized utilizing the same recipe, lithography mask as well as the same epilayer (**RMS=0.25nm**) as reported in the last presented device with InAs n+ contact module. Its key specifications can be found in **Figure 101**.

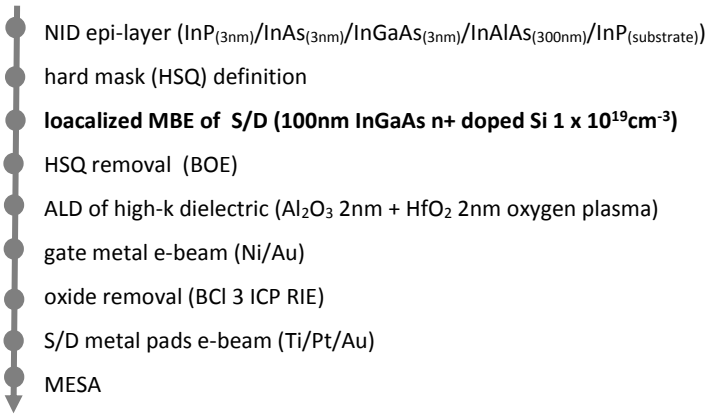


Figure 101: Key specifications of the 3rd generation UTB MOSFET process flow

Examining the electrical performance of the whole set of fabricated gate lengths was discovered that the difference between MOSFET with InAs n+ and MOSFET with InGaAs n+ contact modules is most prominent at 25nm L_G MOSFET. The output characteristics of these devices are compared in **Figure 102**. The device with InGaAs n+ contact module is characterized by a lower maximum current that attains 830mA/mm at (V_{GS}=1V) whereas for InAs n+ the maximum current is 1400mA/mm (V_{GS}=1V).

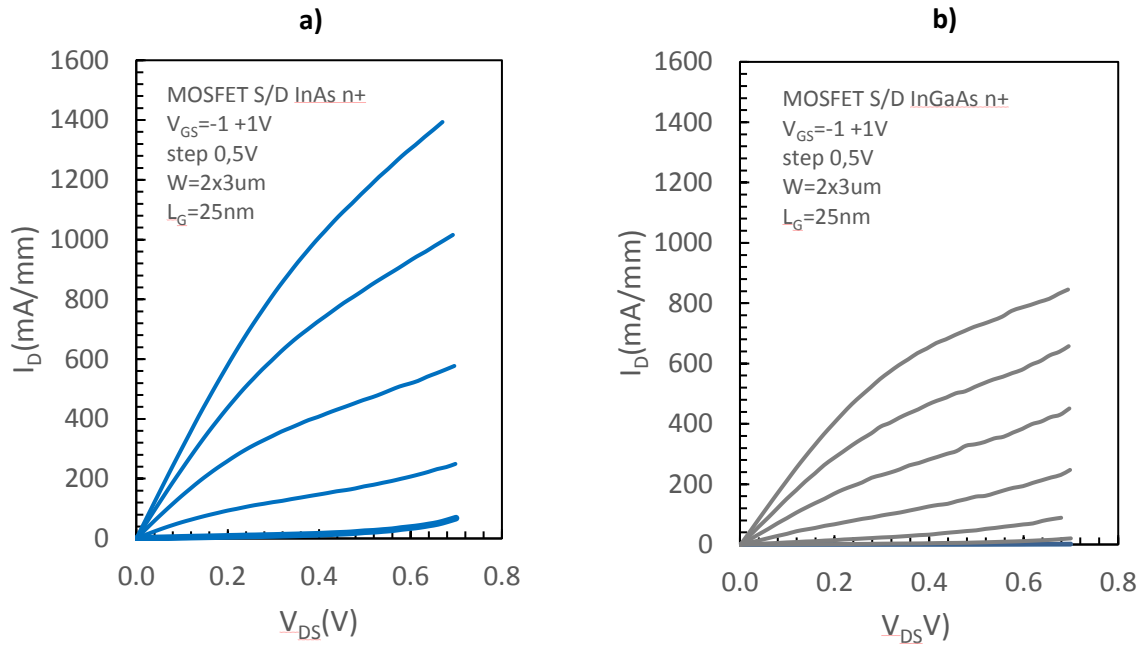


Figure 102: Output characteristics (I_D-V_{DS}) of 25nm L_G UTB InAs MOSFET with InAs n+ **(a)** and InGaAs n+ **(b)** contact module.

4.1 Decomposition of the access resistance of MOSFET with raised S/D InGaAs n+

The explanation can be provided by a higher access resistance whose extraction and decomposition (**Figure 103**) is performed in the same manner as presented for InAs n+ contact module. The extracted metal junction resistance of InGaAs n+ ($R_{InGaAs\ n+/metal}$)(TLM) and the sheet resistance $R_{InGaAs\ n+}$(TLM) is equal to 30Ωµm and 38Ω/Sq respectively. The extracted transfer length (L_T) is 800nm. Extrapolating the MOSFET R_{ON}-L_G curve (**Figure 103b**) is determined an access resistance of 176Ωµm which is higher than the access resistance obtained for MOSFET with InAs n+ contact module. Equally, the decomposition of the access resistance is realized by TLM structure (**Figure 103c)** and recalculated with respect to MOSFET dimensions (**Figure 103a)**. Higher access resistance is due to a more important metal junction resistance of InGaAs n+ ($R_{InGaAs\ n+/metal}$) that is equal to 107Ω.µm (**Figure 103d)** whereas for InAs n+ is only 55Ω.µm **(Figure 100d).**

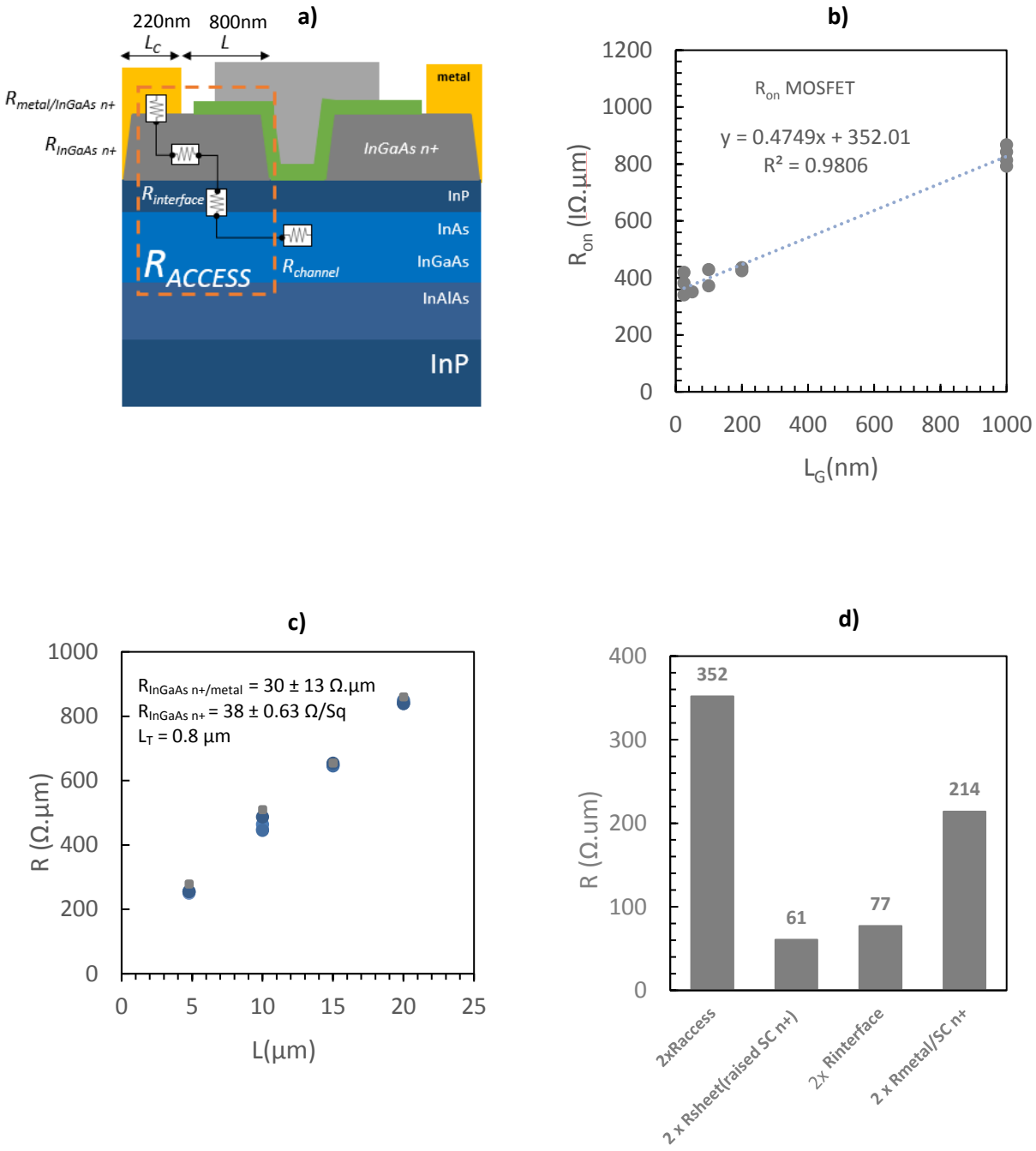


Figure 103: Illustrated model of one side access resistance (**a**) Plotted R_{ON} as a function of L_G. (**b**) Plotted R as a function of the separation gap L obtained from the TLM structure (**c**) decomposed elements of the access resistance (**d**).

Considering the subthreshold characteristics presented in **Figure 104**. MOSFET with InGaAs n+ contact module provides two decades lower subthreshold leakage currents than MOSFET with InAs n+ module. Another feature of the MOSFET with InGaAs n+ contact module

is the lowest measured subthreshold swing of SS=180 mV/dec (V_{DS}=50mV) and SS=220 mV/dec (V_{DS}=0,5V) reported throughout this dissertation for L_G=25nm MOSFET. Also, the device is less susceptible to the tunnel-related leakages than MOSFET with InAs n+ contact module that is visible as a smaller difference between the off-state leakages and subthreshold swings biasing the device at a high (V_{DS}=0.5V) and at a low drain (V_{DS}=50mV) voltage.

Regarding the gate current of 25nm L_G MOSFET (**Figure 104**), this is most probably dominated by In(Ga)As n+/oxide/metal tunnel current due to an important size of the gate stack overlap. In this regards, the difference in the gate leakage signature can be assigned to different tunneling properties of InAs n+/oxide/metal and InGaAs n+/oxide/metal material systems. However, in neither case, does the gate leakage current exceed 0.01mA/mm and therefore can be excluded as a cause of different drain leakage properties.

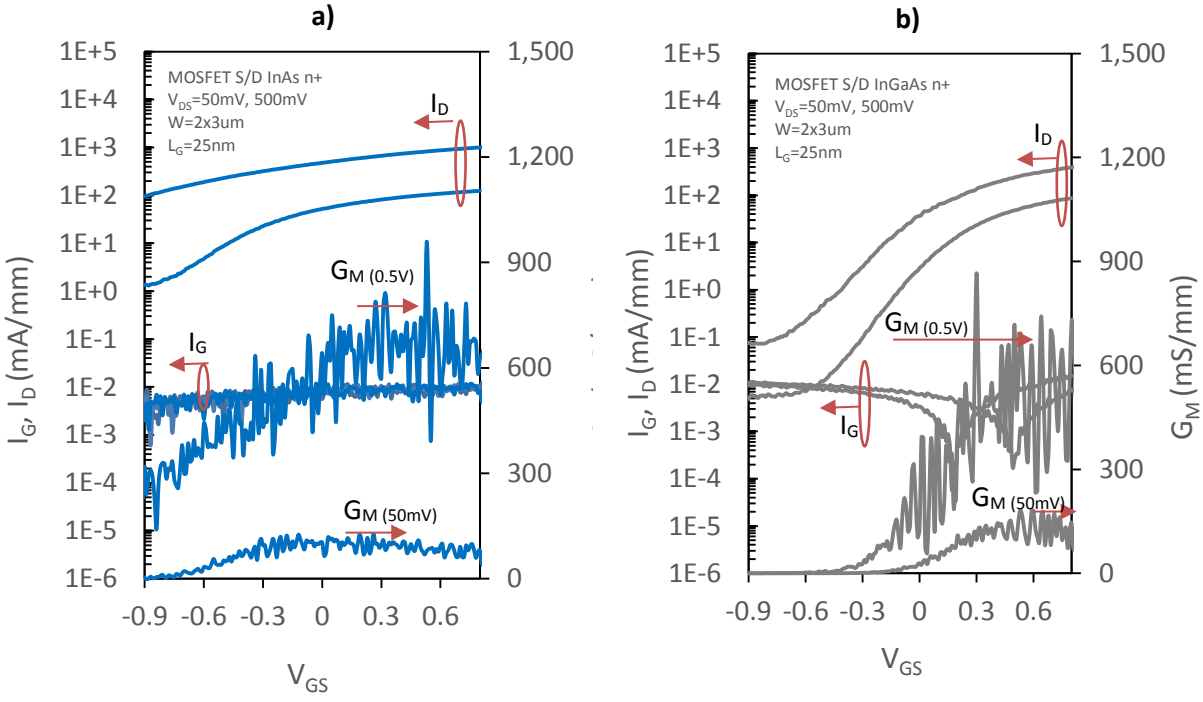


Figure 104: Subthreshold characteristic (I_D-log(V_{GS})) of 25nm L_G UTB InAs MOSFET with InAs n+ (**a**) and InGaAs n+ (**b**) contact module.

One could argue that the lower off-state metrics obtained for InGaAs n+ contact module can be explained by a higher access resistance. For a given extrinsic source drain bias, the higher access resistance lowers the intrinsic drain source voltage. Since $V_{GD}=V_{GS}-V_{DS}$, lower drain source voltage induces a smaller channel-drain band bending. This occurs at the edge of the drain InGaAs n+ contact and causes subthreshold and tunnel leakages. However, this

interpretation does not hold for a small drain bias (V_{DS}=50mV) where this effect can be neglected. Also, it is worth to remind that contrary to InGaAs n+, InAs n+ is lattice unadapted to InP. Presence of the source and drain InAs n+ stressors may cause the damage of the channel epi-layer and alter the leakage response of the deeply scaled 25nm channel MOSFET. Therefore, HRTEM inspection of both channels would be required.

Analyzing the principal electrostatic parameters extracted from the whole set of fabricated gate lengths (**Figure 105**) we can say that except V_{TH} the MOSFET equipped with InGaAs n+ contact technology provides the lowest shift of ΔSS=110mV/dec (V_{DS}=0.5V) and ΔSS~5mV/dec (V_{DS}=0.05V) comparing to a short gate MOSFET (L_G=25nm) and to a long gate MOSFET (L_G=1µm).

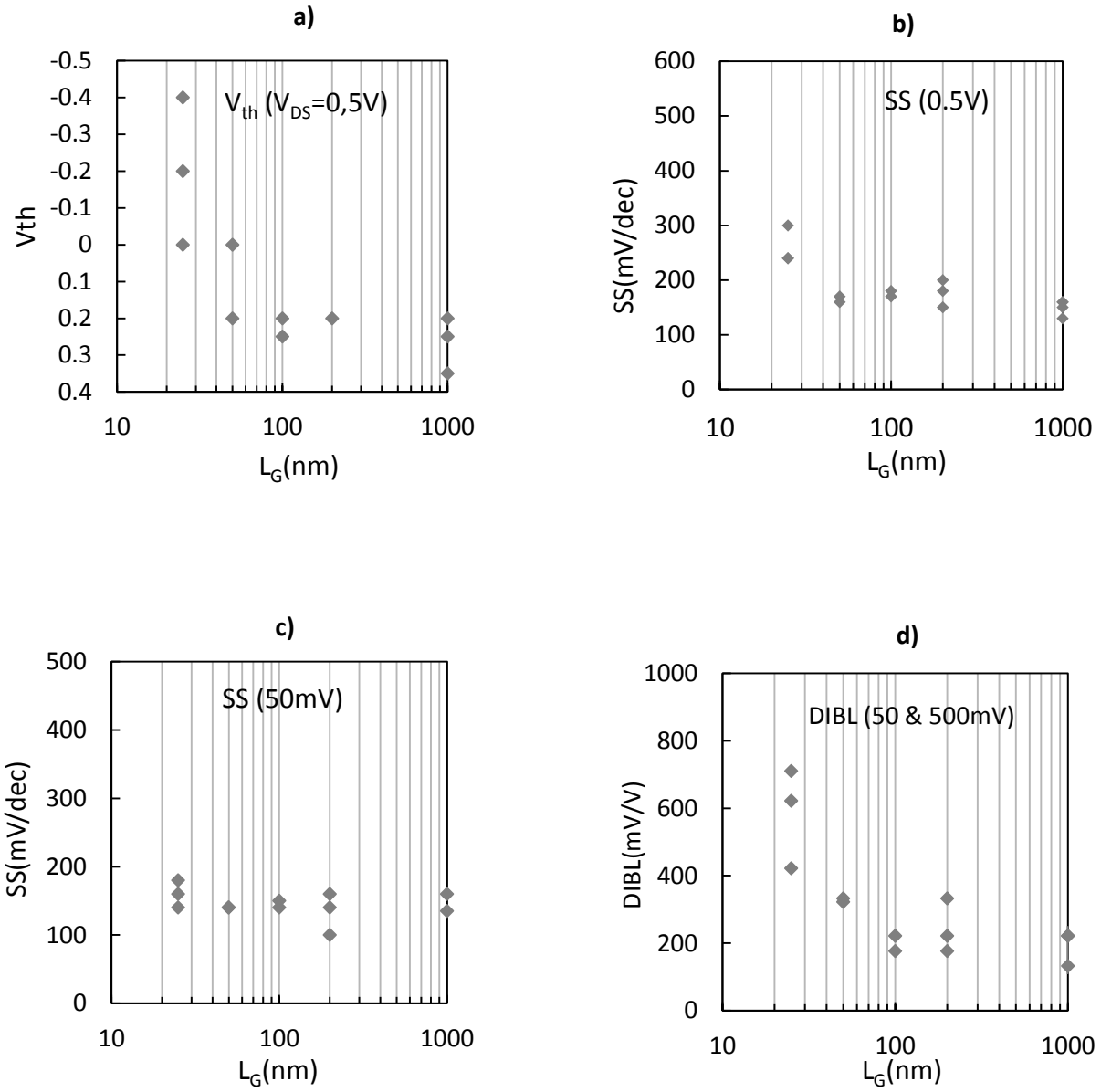


Figure 105: Principal MOSFET electrostatic parameters. Threshold voltage (V_{th}) extracted at V_{DS}=0.5V (**a**), Subthreshold swing (SS) extracted at V_{DS}=0.5V (**b**), Subthreshold swing extracted at V_{DS}=50mV(**c**), Drain induced barrier lowering (DIBL) extracted at V_{DS}=50mV and 0.5V (**d**).

5 First FinFET generation

To further reduce the SCE, one could suggest to scale down the channel thickness of UTB MOSFET. Nevertheless, price to pay is a lower current density and lower carrier mobility. Another key factor that limits the performance of the UTB technology is the gate electrode. This controls only one side of the channel leaving the bottom side floating on a semi-insulating InAlAs layer. In this situation, regardless of the effort that is put into the optimization of the UTB MOSFET oxide or epi-layer, device scaling potential will be still limited by the scaling theory that states, more electrodes is brought to the MOSFET design, better gate length scalability can be expected. Or in other words, lower leakages can be obtained for extremely small gate lengths.

In this situation was prepared transition towards 3D channel design developed in a close collaboration with our partner Epiphy group. Its elaboration was detailed in the second chapter (GAA (FinFET) InAs fabrication module). In contrast to 2D InAs, 3D InAs channel design brings more complexity to the device fabrication. Namely, the fabrication contains two selective epitaxies of InAs. The first consists in growing InAs channel and the second in forming the source and drain contacts of InAs n+. The process is a bottom-up technology.

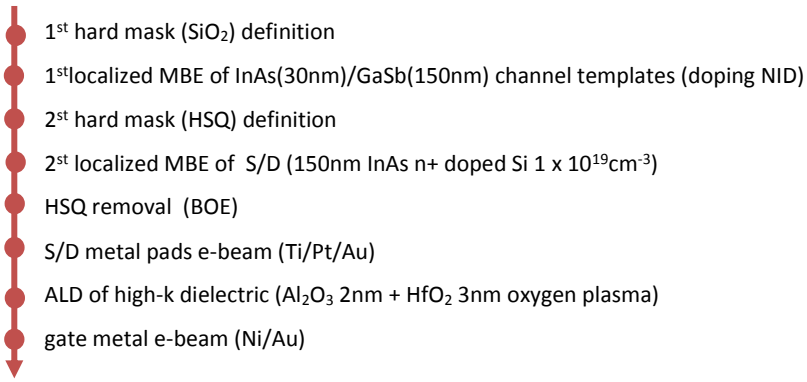


Figure 106: Key specifications of the 1st FinFET generation process

Remaining fabrication steps can differ according to the choice of the gate stack design. Indeed, InAs channel has a 3D shape what makes possible encapsulation of top and bottom InAs channel side by a gate electrode. Encapsulation of the channel is possible by means of conformal ALD technique allowing to deposit the high-k oxide and the gate metal. While the

ALD oxides deposition has been mastered, proved by the abovementioned series of working UTB InAs MOSFET equipped with extremely scaled oxides, ALD deposition of metal layers will require further optimization. The first prototype of GAA InAs realized with a high-k oxide Al_2O_3 (2nm) + HfO_2 (2nm) and Platinum (50nm) was characterized by an extremely high gate leakage current rendering the device dysfunctional.

As a temporary solution was chosen a gate stack deposition procedure already reported in the abovementioned series of planar UTB InAs MOSFET fabrication module. This consists in skipping the Pt deposition step and simplifying the process to Al_2O_3 (2nm) + HfO_2 (3nm) high-k oxide deposition plus an e-beam evaporated (Ni/Au) gate metal. In contrast to ALD of Pt, the latter is not realized in a conform manner. Instead, the evaporated metal is deposited only on one top side of the channel leaving the bottom side of InAs channel without metal deposition. The key specification of the device fabrication process can be found in **Figure 106**. Images recorded by Scanning Electron Microscopy after the device fabrication are presented in **Figure 107**. The InAs channel was grown in SiO_2 hard mask apertures of a larger of 200nm oriented along [110] direction.

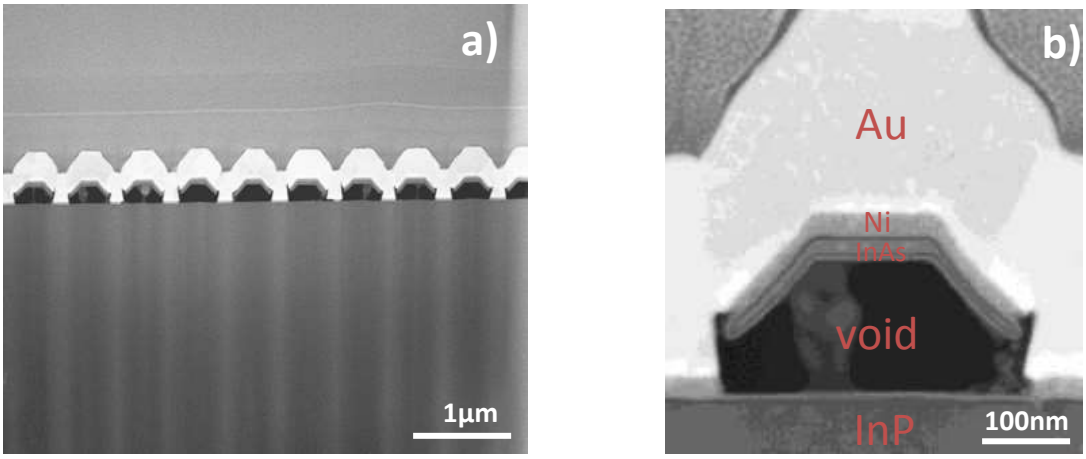


Figure 107: Cross-sectional STEM image of an array (**a**) and general view (**b**) of FinFET InAs channel with Ni/Au metal gate stack oriented along [110] direction.

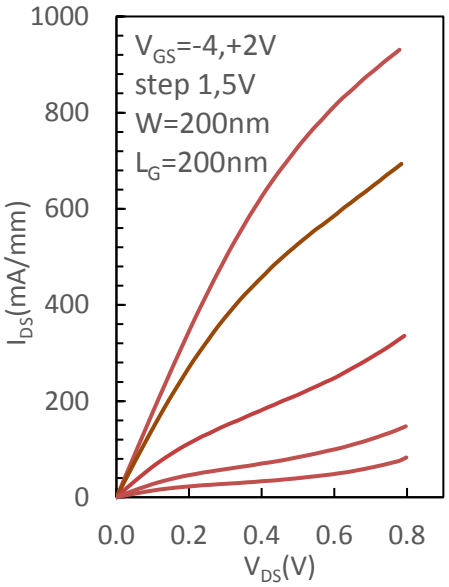


Figure 108: Output characteristics (I_D-V_{DS}) of 200nm L_G device.

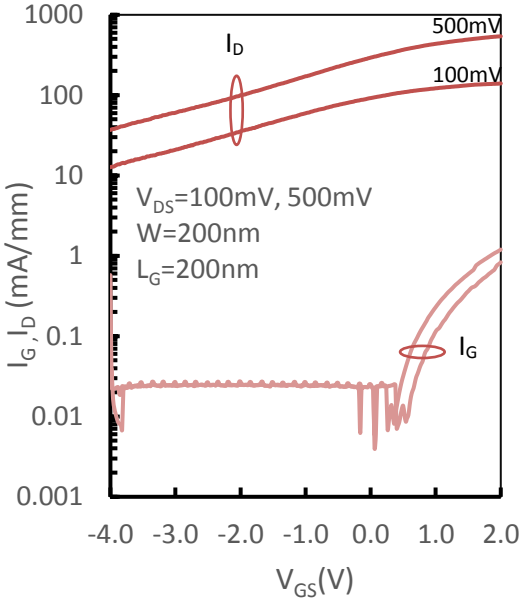


Figure 109: Subthreshold characteristics (log(I_D)-V_{GS}) of 200nm L_G device

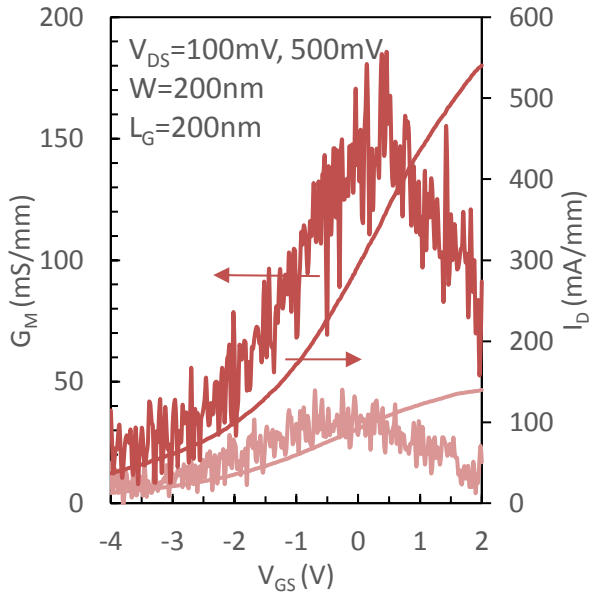


Figure 110: Transfer characteristics (I_D-V_{GS}) of 200nm L_G device.

In the next step, 200nm and 1µm L_G FinFETs were electrically characterized. The FinFET measurement structure consists of an array of 74 fingers of InAs FET. The measured data are normalized to the combined width of 74 fingers. This comprises the contribution of all InAs

sidewalls including in-plane and out-plane InAs sidewalls determined from the TEM scans (**Figure 107b**).

Considering the output characteristics of 200nm L_G presented in **Figure 108**. The device presents a high saturation current of 930mA/mm obtained at V_{GS} equal to 2V. The R_{on} resistance obtained for a high gate voltage of 2V is equal to 730Ω.µm**.** On the other hand, the device is characterized by a strong leakage that is impossible to be suppressed even when driving the device under V_{GS}=-4V. Leakage current at this level exceeds 7mA/mm.

Considering the subthreshold characteristics (log (I_D)-V_{GS}) presented in **Figure 109**, log (I_D) current falls with a slope of 4.5V/dec for V_{DS}=0.1 and 0.5V without attaining a floor level. The high value of SS points to an insufficient electrostatic control. Identical SS extracted at V_{DS} of 0.1V and 0.5V suggest a smaller importance of tunnel-related leakage. In terms of the gate leakage, this exhibits a stable value that oscillates around 0.02mA/mm within the measured gate span (-4V to 0V) and can be considered insignificant in regards to the drain leakage currents. Insufficient electrostatic control is translated into a low transconductance (**Figure 110**). Biasing the device at 0.5V this attains 150mS/mm.

Analyzing the output characteristics of the long gate FinFET (L_G=1µm) depicted in **Figure 111**. The device exhibits a reduction of the saturation currents. For instance, biasing the device at V_{GS}=2V maximum current drops to 200mA/mm which represents a difference of a factor of 4 against 200nm L_G device. This can be explained by a higher channel resistance that is proportional to the gate length.

In spite of the lower drain currents, the device displays a transconductance of 120mS/mm (**Figure 112**) that represents only a slight diminishment in comparison to 200nm L_G device. Examining the subthreshold characteristics plotted in **Figure 113**. It is noticeable that the device presents an insignificant threshold voltage shift of 20mV between 0.5V and 0.1V what corresponds to DIBL of 50mV/V. Biasing the device at V_{DS}= 0.1V and 0.5V we find SS of 110mV/dec. A minimal drain leakage current for V_{DS}=0.5V is 4.86 x 10^{-5} mA/mm providing I_{max}/I_{min} ration 10^6 obtained within the gate voltage span going from -0.6V to 2V. Below -0.3V the drain leakage current attains a floor level given by an increasing importance of the gate leakage current.

Lower values of the off-state metrics against 200 nm L_G device are explained mainly by a stronger immunity against the short channel effects provided by the long channel design. Here, the values of the subthreshold swings are close to the previously reported UTB InAs

MOSFETs (L_G=1µm), however, these remain higher than the theoretical limit of the MOSFET technology.

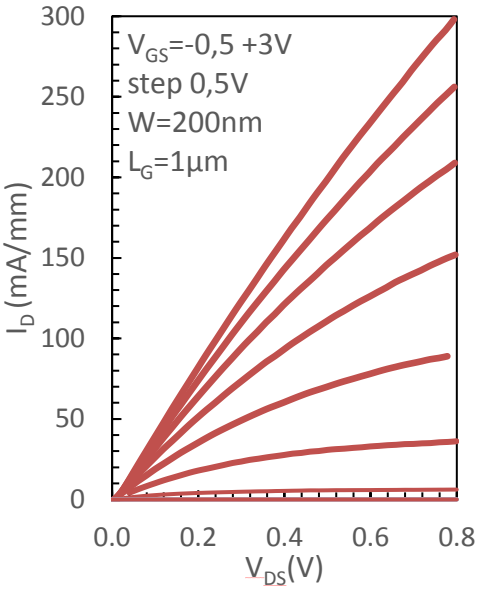


Figure 111: Output characteristics (I_D-V_{DS}) of 1µm L_G device.

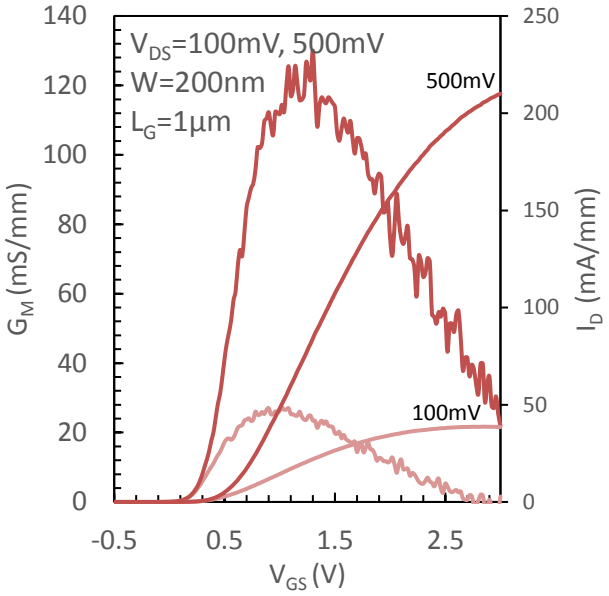


Figure 112: Transfer characteristics (I_D-V_{GS}) of 1µm L_G device.

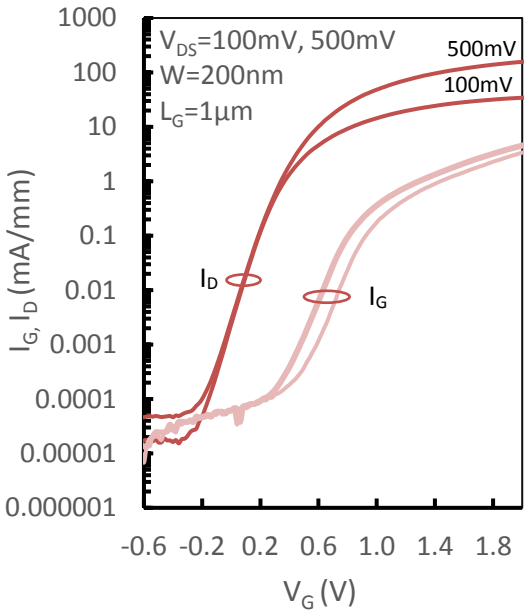


Figure 113: Subthreshold characteristics (log(I_D)-V_{GS}) of 1µm L_G device

Assuming that for a 1µm L_G FinFET the Short Channel Effects play a marginal role. Then the subthreshold swing of 110mV/dec can be interpreted by a presence of a density of interface traps. We recall that the high-k oxide is directly deposited on InAs channel whose oxide interface is usually characterized by a Fermi-level pinning.

Furthermore, high off-state metrics at L_G=200nm suggests important Short Channel Effects. Indeed, the absence of the bottom electrode places the device into the same category of devices as planar UTB InAs MOSFETs. Also, it is worth to remind that the channel thickness of reported UTB InAs MOSFETs was set to 6nm whereas, for proposed FinFET, this is 35nm. Reduction of the channel thickness as well as wrapping the channel all around by a gate electrode can provide an enhanced immunity against the Short Channel Effects.

6 Conclusion

In the last chapter were presented electrical measurements illustrated on selected 3 generations of UTB InAs MOSFET and one generation of FinFET InAs. With an intention to fabricate an extremely small gate length with a good electrostatic control were progressively introduced different design modifications. In the first MOSFET generation was illustrated problematics of the contact size having a crucial impact on the device operation. By reducing the contact size was obtained an improvement of the gate length precision as well as a substantial increase of the on-state current. The second generation of UTB InAs MOSFET realized with a new oxide Al_2O_3 (2nm) + HfO_2 (2nm) and with an improved epi-layer quality yields a substantial improvement in the off state metrics. In the last UTB InAs MOSFET generation was introduced a lattice matched InGaAs n+ contact module. Here, extremely small gate lengths of 25nm present reduction of the on-state metrics, however a substantial improvement in the off state metrics. In the last series of devices was utilized the suspended type of InAs channel intended for future Gate-all-around (GAA) design. Here, the long gate device presents a satisfying on-state and also low off-state metrics. Improvement of the device operation can be achieved by optimizing the gate stack architecture. Wrapping the channel all around by its periphery can provide an enhanced electrostatic control. Also, a channel length scaling to sub 100nm dimensions can provide a quasi-ballistic operation regime characterized by high on-state metrics.

General Conclusion and Perspectives

In the presented work was demonstrated fabrication and characterization of III-V MOSFETs. Dominating part of the work was devoted to the optimization of UTB InAs MOSFET with a planar channel design. Last modification consisted in re-designing the device topology and preparing its ultimate transition towards 3D channel. This was presented as the first generation of InAs FinFET.

Regarding the UTB InAs MOSFET, its low access resistance of 263Ω.µm and 352Ω.µm obtained for InAs n+ and InGaAs n+ contact modules put the device into the state of art III-V MOSFETs whose typical reported value descends to 200Ω.µm (Santa Barbara [59]). This represents an unprecedented progress in comparison to the previous generations of IEMN devices using dopants implantation or Ni-alloy contact technology.

From the scaling perspective, a drastic reduction of the gate length to 25nm was achieved that is considered to operate in a near ballistic regime.

Combination of a deeply scaled gate length, low access resistances enabled to obtain for 25nm L_G MOSFETs high saturation currents achieving 2000mA/mm for V_{GS} of 2V and drain bias of 0.5V.

Besides that, was demonstrated reduction of the off-state metrics. The longest MOSFET channel that is considered to best reflect the value of the D_{it} (density of interface traps) presents the lowest achieved SS_{50mV}= 90mV/dec and $DIBL_{50mV-0,5V}$ of 40mV/V. Extracted values of D_{it}=5.9E^{12} (eV)$^{-1}$cm^{-2} (Subthreshold slope method) agrees with the values of D_{it} extracted from the MOSCAPs (HF-LF method) reported in the second chapter. Also, this value falls within the range of D_{it} = (3-6)E^{12} (eV)$^{-1}$cm^{-2}extracted from the state of art III-V MOSFETs (Santa Barbara [59], Lund university [58] respectively).

In addition to the drastic gate length scaling and satisfying value of D_{it}, a characteristic feature of the reported series of UTB MOSFET was the integration of a thin bilayer dielectric (4nm) Al_2O_3 and HfO_2 providing a smaller EOT of 1.9nm. In addition, a correlation between the epi-layer roughness and the device electrostatic control was reported. The combination of the

improved epi-layer roughness and the scaled EOT thickness enabled to obtain a better immunity against the off state leakages and the short channel effects. In the last reported UTB InAs MOSFETs (3 th, 4th generation), the subthreshold swing (V_{DS}=0.05V) is stable up to 50nm L_G MOSFET. The effect of the reduced off-state metrics was best observed on the extremely small gate lengths. For instance, for L_G=50nm, was reported reduction of SS (V_{DS}=0.05V) from a level of 800mV/dec to 130mV/dec. For MOSFET with 25nm L_G a reduction of SS (V_{DS}=0.05V) from 1.5V/dec to a level of 180mV/dec was obtained.

Also in this work was observed that the deeply scaled 25nm L_G MOSFET with InGaAs n+ contact module exhibited a considerably lower off-state current than the device realized with InAs n+ contact module. We remind that in contrast to InGaAs n+, InAs n+ contact module is lattice mismatched to the InP epi-layer. Therefore, there exists a concern that the InAs n+ contact module induces the channel damage and alter thus the channel leakage response. To correlate the difference in leakage response observed between 3rd and 4th generation with the channel damage, HRTEM inspection of both channels is scheduled by our collaborators (LETI laboratory).

Further improvement of the extremely scaled MOSFET's off state metrics is possible and can be achieved by the following optimization:

The first modification can be realized on the level of the epi-layer. Here, one could propose to introduce p-type doping into InAlAs buffer layer while keeping the channel unintentionally doped. This mitigates the channel drain capacitance coupling and reduces thus the short channel effects. Simulation and device fabrication with the modified epi-layer is the subject of the ongoing work.

To further improve the device scalability, the second suggestion concerns the oxide EOT. Intel has already introduced extremely shrinked high-k oxide for their 22nm technology yielding an extremely small EOT of 0.9nm [114]. In this sense, one could propose to skip Al_2O_3 and utilize uniquely HfO_2 or ZrO_2 single layer providing a higher dielectric constant and a smaller EOT [64].

Lastly can be addressed the problematics of BTBT tunneling current that is important for narrow bandgap materials such as InAs. As proposed by [61], this behavior can be

diminished by increasing the thickness of the wide bandgap barrier introduced between the channel and the raised contact In(Ga)As n+.

Following this strategy, a reduction of the off state metrics can be expected. For instance, assuming that $SS_{0.5V}$ is reduced for 50nm L_G MOSFET (3rd generation) and 25nm L_G MOSFET (4th generation) to 100mV/dec, a substantial improvement of I_{on} by around two orders of magnitude can be expected. This would make both technologies competitive in terms of I_{ON} with extremely scaled state of art Si MOSFETs.

Futhermore, contact scaling would require an optimization of the metal/In(Ga)As n+ contact resistance. For example, reducing the contact dimension below 15nm [13] while maintaining the same level of access resistance would require reduction of metal/InGaAs n+ junction resistivity from 5Ω.µm^2 (InAs n+) and 23Ω.µm^2 (InGaAs n+) to a level below 1Ω.µm^2. This could be achieved by implementing an advanced technique of InAs n+ and InGaAs n+ native oxide desorption or by raising InAs n+, InGaAs n+ doping level beyond 1E^{19} cm^{-3}.

In order to adapt the device for high-frequency applications, the high gate stack overlap has to be removed [58]. In fact, this causes a high parasitic capacitance limiting the device cutoff frequencies. To address this issue, we have developed optimized InGaAs n+ contact design. Cross-section image of the device gate stack with optimized contact module is depicted in the picture (**Figure 114**). After the gate stack formation, InP is selectively removed what reduces the gate-InGaAs n+ capacitance coupling effect.

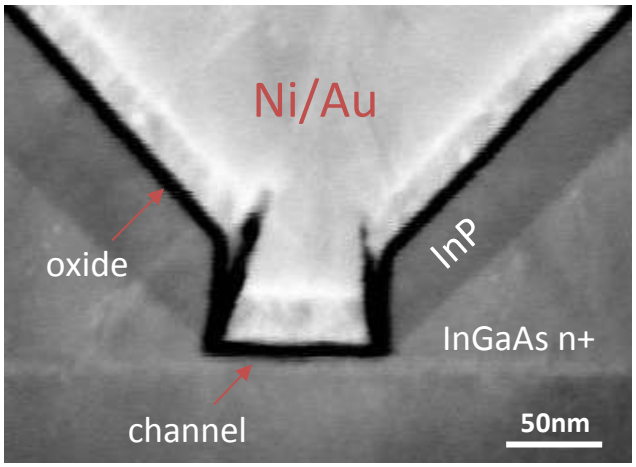


Figure 114: Cross-section STEM image of UTB InAs MOSFET with raised InGaAs n+ contact module adapted for RF applications. Image is recorded before removal of sacrificial InP.

In a search of better electrostatic command, abandon of 2D channel design and transition towards 3D topology seems to be inevitable. This has been partially demonstrated by the first generation of FinFET InAs. However, to fully benefit from its supreme electrostatic properties, several modifications of the FinFET design will be demanded. These concerns primarily the optimization of the channel thickness that needs to be scaled down to enhance the electrostatics. This may be resolved either by optimizing the growth conditions or by utilizing a digital etching to selectively remove few nm of InAs channel. Also, achievement of the Gate All Around design will be conditioned by introduction of ALD metal deposition into the fabrication process.

Appendix

1 Microwave characteristics

In the following are illustrated microwave characteristics performed on selected MOSFETs and FinFETs. Extrapolating the Mason unilateral power gain (*U*) and the current gain ($|H_{21}|^2$) plotted as a function of frequency can be determined the cut-off frequency (f_t) and a maximum oscillation frequency (f_{max}) utilized as a useful metrics in logic and analog circuits respectively (**Figure 115**). Current and Mason gain are calculated from S matrix containing S_{11}, S_{12}, S_{22}, S_{21} parameters.

$$|H_{21}|^2 = \left|\frac{-S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}\right|^2 \quad (25)$$

$$U = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2\left(K\left|\frac{S_{21}}{S_{12}}\right| - R_e\left(\frac{S_{21}}{S_{12}}\right)\right)} \quad (26)$$

To minimize an effect of the parasitic access lines and the contacts pads is perform a so called de-embedding method. This consist in measuring the S matrix of the short and open structures presented on the MOSFET lithography masks (chapter 2). This enables to obtain a de-embedded S matrix free of the parasitic terms. Capacitance of the gate overlap is not de-embedded. Microwave characteristics were measured by vector network analyzer calibrated by LRRM method. Measurements were performed on wafers referred in the dissertation as second UTB InAs MOSFET generation (orientation [100]) and first FinFET InAs generation.

1.1 UTB InAs MOSFET

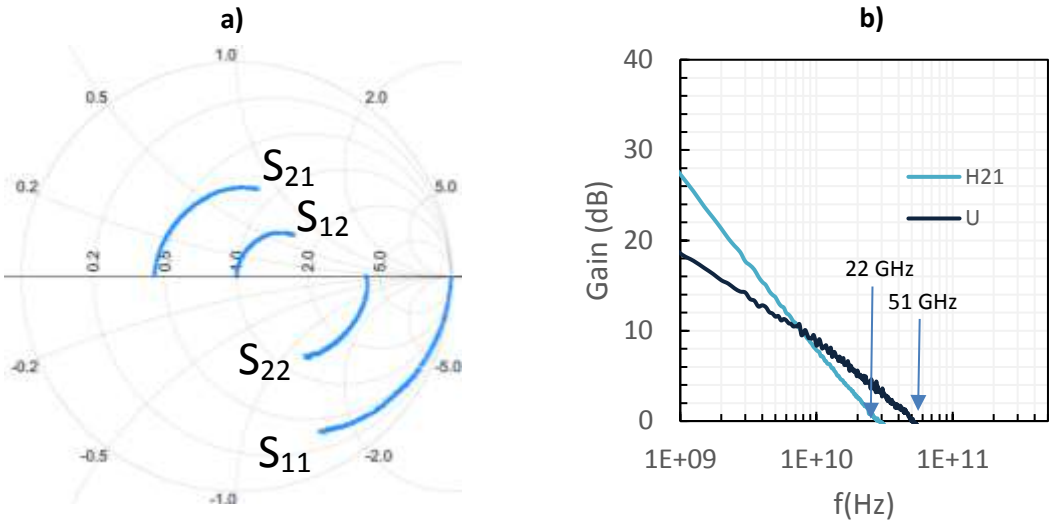


Figure 115: De-embedded S parameters of 25nm L_G MOSFET (**a**). Current ($|H_{21}|^2$) and Mason unilateral power gain (U) of 25nm L_G MOSFET U plotted as function of frequency (**b**). (frequency range from 250MHz to 67GHz, V_{DS} = 0.7V, V_{GS} = max (H_{21}))

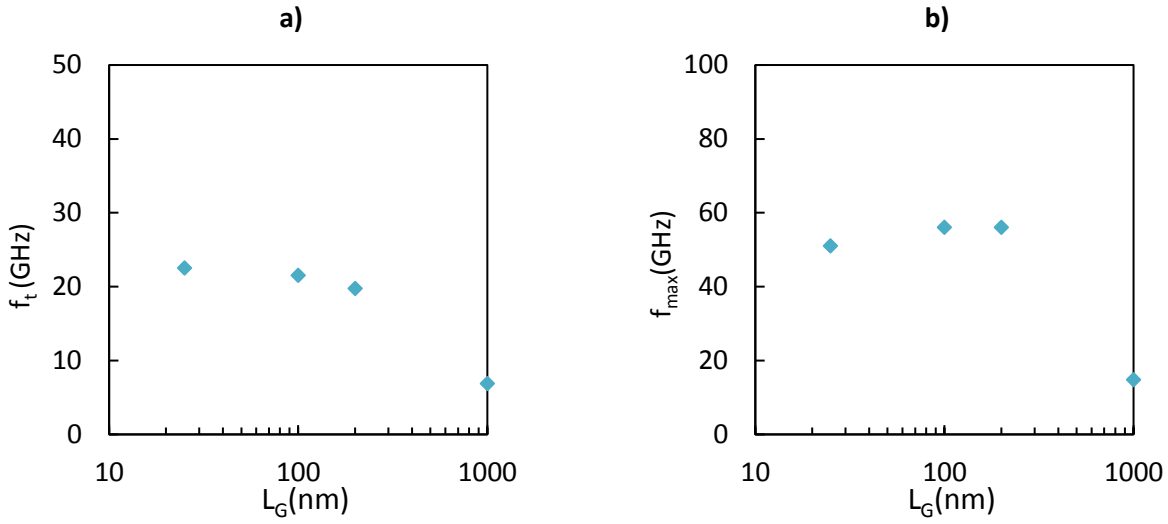


Figure 116: Cut-off frequency f_t displayed as a function of L_G (**a**), maximum oscillation frequency f_{max} displayed as a function of L_G (**b**). (frequency range from 250MHz to 67GHz, V_{DS} = 0.7V, V_{GS} = max (H_{21}))

1.2 FinFET InAs

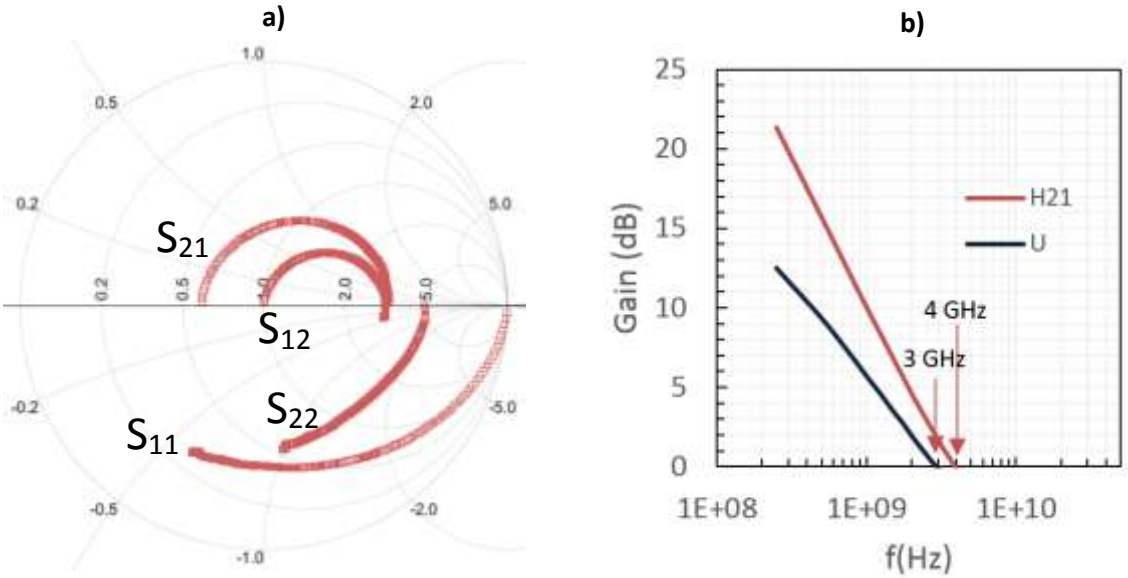


Figure 117: De-embedded S parameters (a). Current ($|H_{21}|^2$) and Mason unilateral power gain (U) of 200nm L_G FinFET (W=100nm) plotted as a function of frequency (b), (frequency range from 250MHz to 67GHz, V_{DS}=1V, V_{GS}=max (H_{21}))

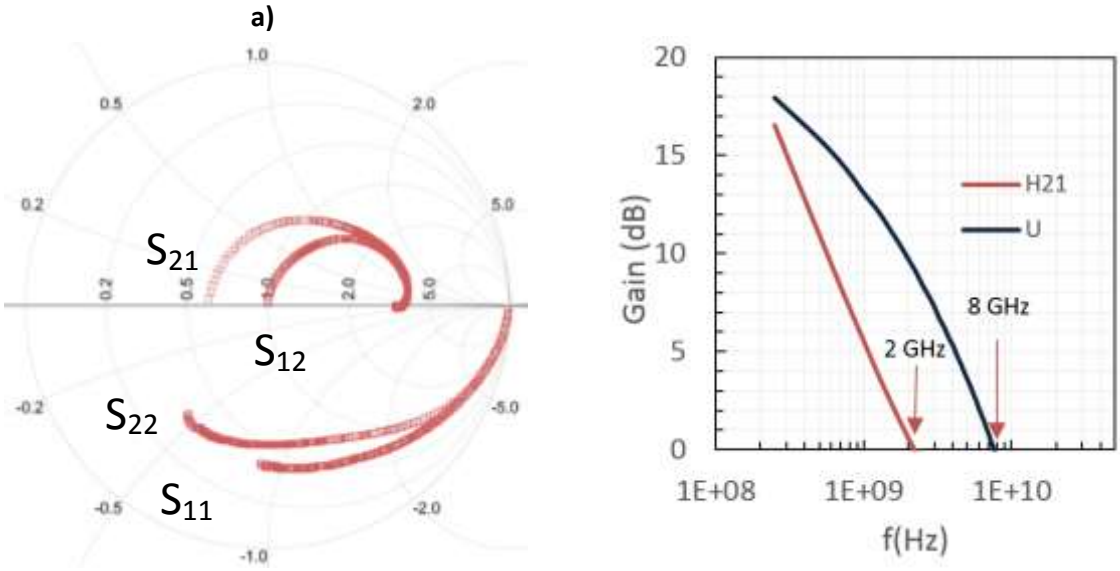


Figure 118: De-embedded S parameters (a). Current ($|H_{21}|^2$) and Mason's unilateral power gain (U) of 1µm L_G FinFET (W=200nm) plotted as a function of frequency (b), (frequency range from 250MHz to 67GHz, V_{DS}=1V, V_{GS}=max (H_{21}))

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List of publications

"Ultra thin body InAs MOSFET with raised InAs n+ S/D by selective MBE" **M. Pastorek**, M. Ridaoui, A. Fadjie, A. Olivier, N. Wichmann, L. Desplanque, X. Wallart, S. Bollaert, Device Research Conference (DRC), IEEE, Notre Dame USA, 25- 28 June, 2017

"Ultra-thin body InAs MOSFET with selectively raised InAs n+ S/D contacts," **M. Pastorek**, N. Wichmann, L. Desplanque, M. Ridaoui, Alain. B. Fadjie, Y. Leachaux, X. Wallart, S. Bollaert, WOCSDICE, Aveiro Portugal, 6-10 juin, 2016

"Static and low frequency noice characterization of ultra thin body InAs MOSFET," T. A. Karatsori, **M. Pastorek**, C. G. Theodorou, A. Fadjie, N. Wichmann, L. Desplanque, X. Wallart, S. Bollaert, C. A. Dimitriadis, G. Gibaudo, International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, IEEE, Greece, 3-5 April, 2017

"Fabrication of InAs in-plane nanowires with raised heavily doped contacts using selective area molecular beam epitaxy,", IEEE, L. Desplanque, **M. Pastorek**, A. Olivier, M. Fahed, N. Wichmann, S. Bollaert, A. Addad and X. Wallart, Berlin Germany, 15-18 Mai,2017

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"Low interface traps density of Al_2O_3 on InP interfaces using post oxygen plasma treatment," Alain B. Fadjie, Y. Lechaux, M. Ridaoui, **M. Pastorek**, N. Wichmann, S. Bollaert, 27th International Conference on Indium Phosphide and Related Materials, IEEE, Santa Barbara USA, june 28, 2015

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"High-Performance Self-Aligned InAs MOSFETs with L-shaped Ni-epilayer alloyed source/drain contact for Future Low-Power RF applications," M. Ridaoui, Alain B. Fadjie, **M. Pastorek**, N. Wichmann, A. Jaoued, H. Maher and S. Bollaert, in 11th European Microwave Integrated Circuits Conference (EuMIC), IEEE, United Kingdom, 3-7 octobre, 2016

"MOSFET III-V : du Transistor Planaire à Couche Mince aux Nanofils à Grille Enrobante," **M. Pastorek**, N. Wichmann, M. Ridaoui, A. Olivier, L. Desplanque, X. Wallart, S. Bollaert, Journées Nationales Microondes, Saint Malo, 16-19 mai, 2017

"Utra-thin body InAs with raised S/D contacts for future high-performance CMOS applications," **M. Pastorek**, N. Wichmann, L. Desplanque, M. Ridaoui, A. Fadjie, Y. Lechaux, X. Wallaert, S. Bollaert, 19ème Journées Nationales du Réseau Doctoral (JNRDM), Toulouse, France, 11-13 Mai, 2016

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