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Realization and characterization of Organic Field Effect Transistors and Nano Floating Gate Memories on rigid and flexible substrates

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List of abbreviations

OFET	Organic Field Effect Transistor
OSCs	Organic Semiconductors
NVM	Nonvolatile Memory
NFGM	Nano-floating Gate Memory
MIS	Metal-Insulator-Semiconductor
HOMO	Highest Occupied Molecular Orbital
LUMO	Lowest Unoccupied Molecular Orbital
S/D	Source/Drain
SAM	Self-assembled Monolayer
PMMA	Polymethylmethacrylate
Au NPs	Gold Nanopaticles
NCs	Nanocrystals
OTS	3-Octadecyltrichlorosilane
rGO	Reduced Graphene Oxide
PFBT	2,3,4,5,6-Pentafluorobenzenethiol
EBL	Electron-Beam Lithography
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
XPS	X-ray Photoelectron Spectroscopy
UPS	UV-Photoelectron Spectroscopy
RMS	Root Mean Square Roughness
W/L	Channel Width /Channel Length
DFG	Double Nano-floating Gate
SFG	Single Nano-floating Gate

List of abbreviations

APTS	3-Aminopropyl)triethoxysilane
P/E	Program/Erase
PC	Parylene C
PVD	Physical Vapor Deposition
CVD	Chemical Vapor Deposition
HSQ	Hydrogen Silsesquioxane
UV-zone	Ultraviolet-Ozone
Ref.	References

List of samples

R_{tot}	Total resistance (Ω)
R_C	Contact resistance (Ω)
R_{ch}	Resistance of channel (Ω)
L	Channel length (μm)
W	Channel width (μm)
μ	Charge carrier mobility ($cm^2V^{-1}s^{-1}$)
C_i	Gate capacitance per unit area (F/cm^2)
V_{GS}	Gate-source voltage (V)
V_{DS}	Source-drain voltage (V)
I_{DS}	Source-drain voltage (A)
I_{on}/I_{off}	Current on–off ratio
θ	Contact angle (°)
V_{Th}	Threshold voltage (V)
ΔV_{Th}	Memory window (V)
S	Subthreshold swing (V/decade)
N_{ss}^{max}	Maximum number of interface states ($cm^{-2}\,eV^{-1}$)
k	Boltzmann constant
T	Absolute temperature (°)
q	Electronic charge (C)
Δn	Number of trapped charges in the Au NPs (and polymer electret)

General introduction

In the various of electrical devices, organic field effect transistor (OFET) have been attracted great attention over the past few years because of a number of merits such as low-cost process, potential to realize large areas, and particularly that they are compatible with flexible plastic circuits. Nowadays, the OFET based nonvolatile memory (NVM) devices. i. e. flash memory, which means the information could be remain stored even when power is disabled, is also one of the most important and fundamental elements in the construction of electronic systems. Generally, the flash memory could be classified in terms of the structures and materials of the charge storage layers, among the many possible device configurations of organic flash memories, tremendous efforts have been devoted to the development of nano-floating gate-based transistor memories (NFGM) towards high performance memory devices (exhibit high speed operation, superior reliability, and to be scaled down), due to its spatially discrete floating-gate elements (nanometer-sized metallic or semiconductor nanoparticles) effectively as a charge trapping site between two dielectric layers (blocking layer and tunneling layer.

Considering the effects of materials and process conditions, the characteristics of the pentacene based NFGM were improved more or less that have been reported. The objective of this work is to develop pentacene based OFET and NFGM devices on flexible substrates. There are mainly three parts involved; (i) Optimization of the OFET that fabricated on conventional Si/SiO_2 substrate; (ii) Improvement of the performances of NFGM based on the results of OFET;(iii) Realization of OFET and NFGM on flexible substrate.

In chapter 1, first, the introduction of the OFET and NFGM is described. Then, the typical high mobility p-type organic semiconductors that are widely used in OFET devices are demonstrated. Based on the widely literatures and the mature fabrication process in our group, the pentacene is chosen as the organic semiconductors in this thesis, thus, the progress of pentacene based OFET and NFGM devices that reported in recent years has been introduced. According to the reports, the self-assembled monolayer (SAM) is presented to optimize the OFET. To fabricate the NFGM, Au nanoparticles (Au NPs) and reduced graphene oxide (rGO) sheets are chosen as the floating gate layers in this work.

In chapter 2, the fabrication processes of our OFET samples on rigid substrates and the analysis instrumentations are described in detail. The physical and electrical properties of different SAM modified pentacene FET devices were performed and discussed, i.e. pentacene

deposited on OTS modified dielectric surfaces, on the PFBT modified source/drain electrodes, and on the cumulative OTS and PFBT modified surfaces. The FET of pentacene deposited on bare SiO_2 was fabricated as a reference. Then, the electrical parameters of the different samples of OFET were summarized and compared. Through the SAM modification, optimized electrical performances were obtained and the charge transport mechanisms were explained.

In chapter 3, the pentacene based single floating gate (SFG) memory (using Au NPs as trap layer) and double floating gate (DFG) memory (using Au NPs and rGO as the lower and upper trap layer, respectively) were fabricated and characterized. The SiO_2 and Al_2O_3 dielectrics were deposited as blocking layer and tunneling layer, respectively. Based on the results of chapter 2, the PFBT was used to modify our memory devices, the performances our NFGM devices with and without PFBT modification were demonstrated and compared. Meanwhile, the effects of rGO sheets and the effects of SAM modification on the NFGM were discussed. Finally, Optimized memory performances including the large memory window of 51 V, the stable retention property more than 10^8 s, and reliable cycling endurance over 1000 cycles were obtained. This further highlights the utility of surface modulations to tune the charge storage/release behaviors in transistor memories.

In chapter 4, first, the performances of pentacene based transistors that fabricated on flexible substrates were presented. The materials used in this transistor are all organics and the fabrication processes are under low temperatures. The operation voltage of the flexible OEFT was deduced compared to the one that fabricated on Si substrate and there was no hysteresis in the I-V measurements, which means the interface traps were well decreased. Then, the NFGM devices were fabricated on flexible substrates and the performances were demonstrated. In particular, the multi-level data storage was achieved from our flexible NFGM, from the bending stability/mechanical stability test, the stable retention property more than 10^5 s, and reliable cycling endurance over 500 cycles were obtained.

In chapter 5, the conclusions of this thesis are summarized and discussed, based on the results of this thesis, the perspective is proposed.

Chapter 1

State of the art

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1.1 Background

Current research on electronic devices have been advancing incredibly fast as much of our life relies on them, the miniaturization and economically applicable are all along great demand for the realization of industrial production. In the various electronic devices, organic field effect transistor (OFET) has been attracted great attention over the past few years because of a number of merits such as low-cost process, potential to realize large areas, and particularly that they are compatible with flexible plastic circuits [1-5]. In the improvement of material performances, since the organic materials used for the OFET fabrication such as the semiconductors, the dielectrics and even the substrates could be deposited at room temperature or relatively at low temperatures. In addition, most of the organic materials are available for deposition in solution, thus the deposition process could be adopted as spin-coating or inkjet-printing that avoid to require a vacuum stage. Otherwise, in the past of years, many organic semiconductors (OSC) have been found high field-effect mobilities (up to 10 $cm^2V^{-1}s^{-1}$ or even higher) that exceed the mobilities (0.5–1.0 $cm^2V^{-1}s^{-1}$) of amorphous silicon, for instance, pentacene, rubrene, and fullerene (C_{60}), the typical OSC used in OFET [6, 7]. As the output current and cut-off frequency are proportional to the mobility, it is essential to obtain high mobility for device applications.

The progress of OSC in mobility and the economy of the fabrication process make OFET has great potential in various real electrical applications based on the industrial manufacturing technology. As a result, for the applications of OFET, they have been expected and proposed to be used as display switches [8], chemical and biological sensors [9, 10], liquid crystals [11], neuromorphic synapses [12, 13], nonvolatile memories [14-16] and so on. In terms of the OFET memory devices, they have the similar geometry as OFET, the difference is that a charge-storing medium like a thin film, or metallic/semiconductive discrete NPs act as floating gate between two dielectric layers for the OFET memory devices [17, 18].

Nowadays, the nonvolatile memory (NVM), which means that the information could be remain stored even when power is disabled, is also one of the most important and fundamental elements in the construction of electronic systems [19-21]. As a conventional NVM, Si-flash memory has been extensively used in mobile storage for a long period of years due to their

massive memory capacity, relatively high density and low fabrication process [22]. Generally, the flash memory could be classified in terms of the structures and materials of the charge storage layers, including conventional floating gate type memory by using a conducting floating gate, nitride-based charge trapping memory [23] and NPs or nanocrystals (NCs) based charge trapping memory (called nano-floating gate memory NFGM) [24], they have the common configuration that the trapping layer assembled between two dielectric layers, which called tunneling layer and blocking layer, respectively. Figure 1.1 shows the device structure of a conventional flash memory cell.

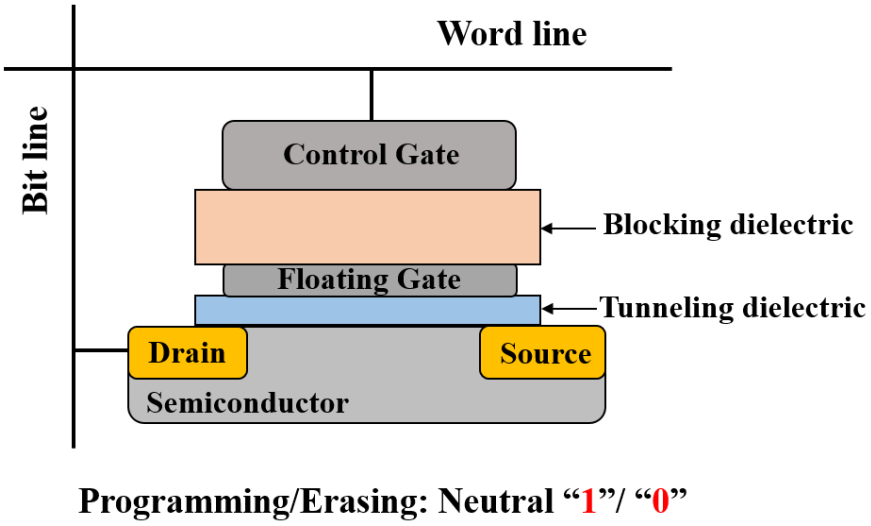


Figure 1.1 Device structure of a conventional flash memory cell.

As portable electronic devices scaling continues, and requirements such as high performance, high density, low power consumption for NVM devices, a lot of challenges have been met for us to optimize the conventional floating gate type flash memory. For example, it is very difficult to reduce the tunneling layer because of the charge loss and stress-induced leakage current [25], and the reduction of the dimensions of the floating gate will decrease the stored electrons/holes, which makes the margin of the electron/hole loss tolerance very narrow [26]. Thus, considering these drawbacks, the emerging flash memory of NFGM type has been proposed and studied. One hand, the NPs (NCs) are discretely assembled between the tunneling layer and the blocking layer that avoid the problem of using a continuous floating gate, on the other hand, the reap levels and trap sites could be effectively controlled and tuned by the work functions and dimensions (size and density) of the NPs [28]. Hence, a tremendous efforts has been devoted to develop NFGM devices in recent decades, it has been considered as a promising

candidate towards high performance flash memory devices that shows large endurance, small size, long retention time, and low power consumption [29, 30]. Among the many possibility applications of NFGM, by using OSC to enable the NFGM, it gives a great opportunity to fulfill the requirements for novel applications targets such as flexible, printable, and low-cost preparation processes [31].

1.2 Overview of organic field-effect transistor (OFET)

1.2.1 Synthesis of organic semiconductors

Organic transistors are metal-insulator-semiconductor (MIS) field-effect transistors (FETs) in which the semiconductor is a conjugated organic material [32]. Generally, the conjugated bands including the sigma (σ)-type bond a pi (π)-type bond, σ-bonds are the strongest in covalent bonds and π-bonds are much weaker than them. In σ-bonds, both bonded atoms give single electron from the s orbital and the two electrons are attached to their nuclei and localized. In π-bonds, the two electrons come from the p orbitals which are far away from their nuclei, and the two electrons are localized as well. Organic semiconductors are conjugated polymers which consist of sp_2–hybridized linear carbon chains. These chains hold a sp_2-$2p_z$ configuration in double bond, overlapping among different sp_2 orbitals forms σ bonds. On the other hand, two p_z orbitals form a less strong covalent bonds called π bonds as shown in figure.1.2 [33].

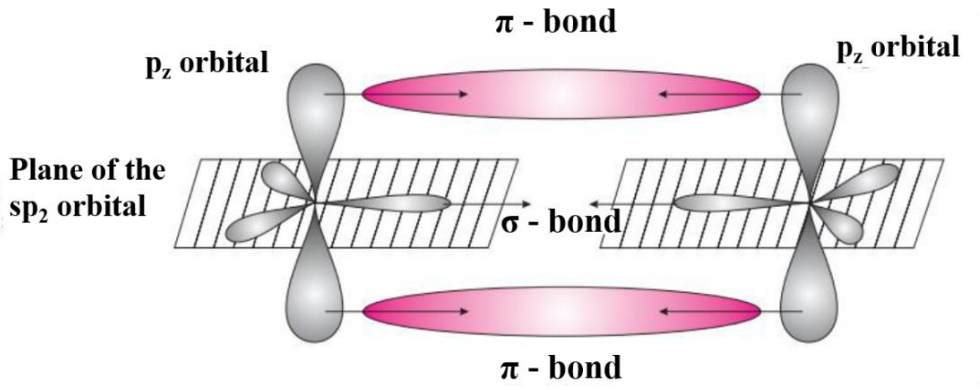


Figure 1.2 Sp_2 hybridization of two carbon atoms. Sp_2 orbitals lie on the same plane and bond into an σ-bond, p_z orbitals are orthogonal to the plane and bond into a π-bond.

For the band diagram of OSCs, as alternating double and single bonds in the conjugated backbone results in a separation of bonding and anti-bonding states, causing the formation of a forbidden energy gap and a spatially delocalized band-like electronic structure. The highest occupied molecular orbital (HOMO) consists of bonding states of the π -orbitals with filled electrons, and is analogous to the valence band in silicon. The lowest unoccupied molecular orbital (LUMO) consists of empty higher energy anti-bonding (π∗) orbitals, and is analogous to the conduction band. The energy difference between the HOMO and LUMO defines the band-gap energy (Eg), as shown in figure 1.3. Eg depends on the chemical structure of the repeating unit, and generally decreases with the number of repeat units in the chain [33]. The Eg of conjugated polymers is typically in the energy range of 1–4 eV. This band-like structure, along with low electronic mobility, is responsible for the semiconducting properties observed in conjugated polymers.

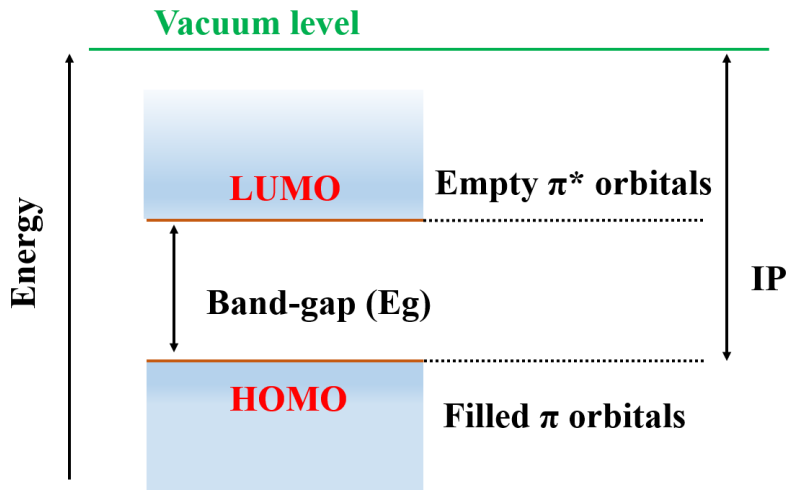


Figure 1.3 Energy band diagram of an organic semiconductor. Abbreviations: IP: ionization potential; LUMO: lowest unoccupied molecular orbital; HOMO: highest occupied molecular orbital.

1.2.2 Structures and operations of OFET

• *Structures*

Generally, the common configurations used for FETs are devised into two different structures, i. e. bottom-gate type and top-gate type, as shown in figure 1.4 [34]. The structure of the device contains the layers of substrate (rigid or flexible), gate electrode, insulator (dielectric), semiconductor, and source and drain electrodes. In addition, because of the different positions of source and drain electrodes, the structures of FET could be identified detail as bottom-gate-bottom-contact (BGBC), bottom-gate-top-contact (BGTC), top-gate-

bottom-contact (TGBC), as well as top-gate-top-contact (TGTC). Briefly, each structure has the merits and drawbacks, the choice of the structure is normally decided by the fabrication processes such as the temperatures, the circumstance conditions, the lithographic masks involved and the materials (metals, dielectrics and semiconductors) that used for the realization of device. In the case of OFETs, the semiconductor is an organic material. The OSCs are the most important materials that are used as the active components for OFET, they can be divided into n-type with electrons transporting and p-type with holes transporting, as well as ambipolar ones with both electrons and holes transporting.

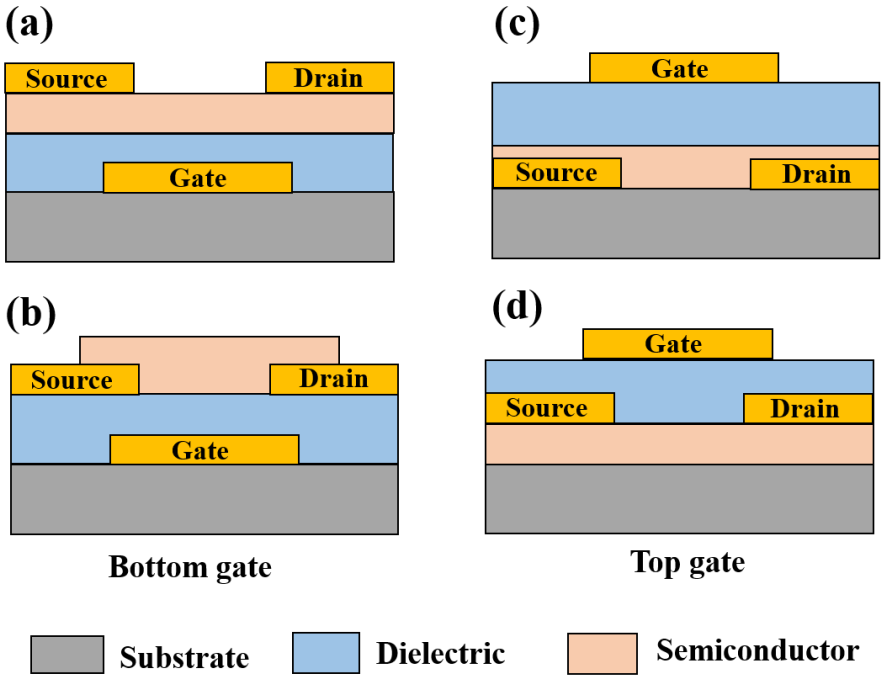


Figure 1.4 Typical device structures of organic field-effect transistors.

• *Operations*

In principle, the electrical characteristic that best to be used to define the OFET is the presence of the electric field that controls and modulates the conductivity of the channel between source and drain electrodes, i. e. the current between source and drain (I_{DS}) [34]. The typical p-type and n-type OFET operations (BGTC structure) are shown in figure 1.5 (a) and (b). The electric field is created by the gate voltage between gate and source (V_{GS}), which is also dependent on the insulator (dielectric) layer. For the different type of semiconductor, a positive or a negative gate voltage will be operated to force the holes or electrons (charges) accumulate at the insulator (dielectric) and semiconductor interfaces. And the density of the

charges is dependent on the V_{GS} and capacitance (C) of the insulator. Figure 1.5 (c) and (d) show the energy-level diagrams along the carriers transport in the channel of p-type and n-type organic transistors, respectively. In p-channel transistors the transfer of negative charges into the semiconductor is blocked due to the large energy difference between the Fermi level of the contact and the LUMO of the semiconductor, and in n-channel transistors the transfer of positive charges is blocked by the energy barrier between the contact and the HOMO of the semiconductor [32].

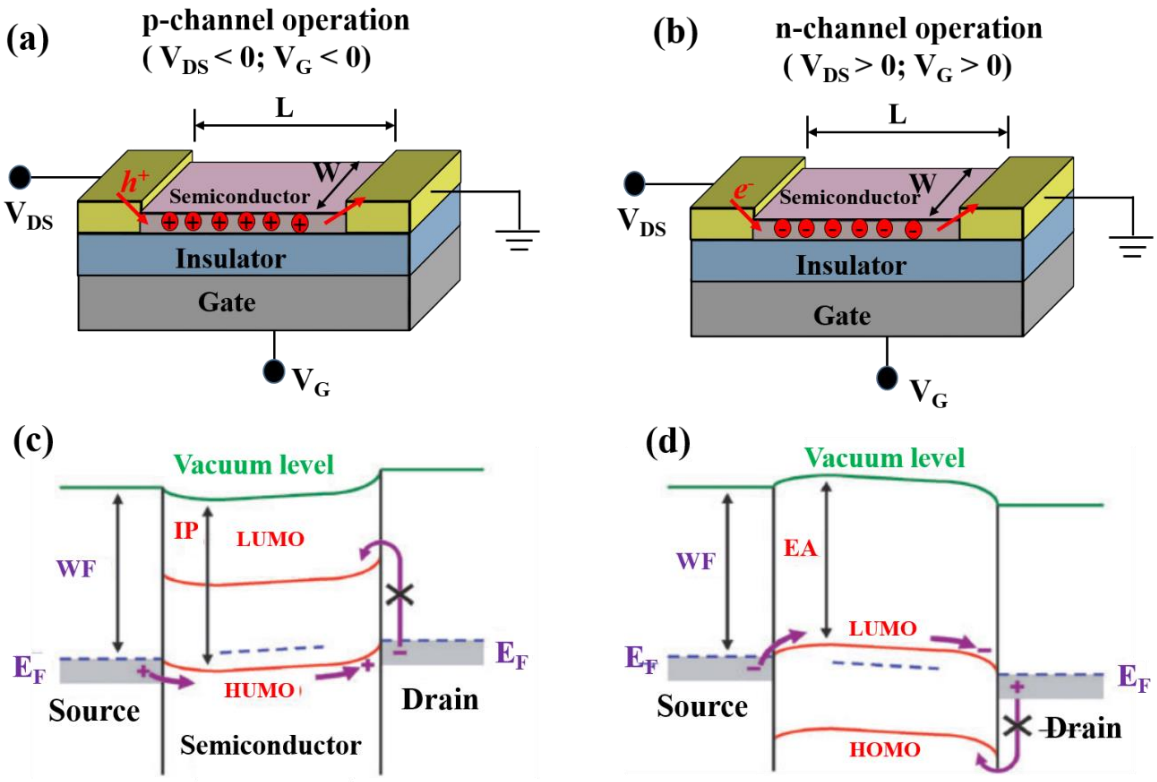


Figure 1.5 Typical operations of (a) p-type and (b) n-type organic field-effect transistors. L, channel length; W, channel width. Energy-level diagrams along the carriers transport in the channel of organic transistors: (c) p-channel transistor, (d) n-channel transistor. Abbreviations: WF: work function; EA: electron affinity; IP: ionization potential; LUMO: lowest unoccupied molecular orbital; HOMO: highest occupied molecular orbital; E_F: Fermi energy level.

1.2.3 Extraction of electrical parameters

The electrical parameters for the OFET are commonly extracted from the typical current-voltage characteristics, which involves static current versus voltage measurements, where output (I_{DS}-V_{DS}, V_{DS} is the voltage between source and drain) and transfer (I_{DS}-V_{GS})

curves can be obtained. As shown in figure 1.6, an example of an n-type device with typical "near"-ideal output and transfer I-V curves.

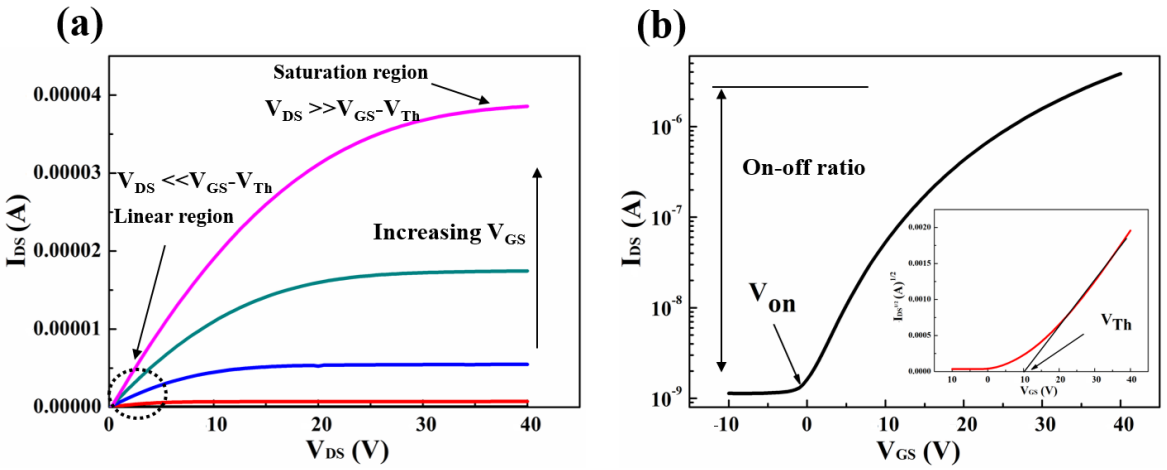


Figure 1.6 Typical (a) output and (b) transfer characteristics of an n-type OFET.

For the output curves that shown in figure 1.6 (a), the characteristic provides a most qualitative information of the effectiveness of channel pinch-off and contact resistance between electrodes and probes of the equipment. As OFET is being seriously assessed for mobility critical applications, it is very important to extract the value of the mobility [6]. As we can see in figure 1.6 (b), when V_{GS}>V_{Th}, a significant density of charges is accumulated in dielectric/semiconductor interface and a large I_{DS} starts flowing, depending on the V_{DS}. This state is designated by On-state and involves a linear current regime at a low V_{DS} and followed by a saturation regime at a higher V_{DS} value, for the two regimes, the I_{DS} varies with the V_{GS} are determined as following:

When V_{DS}<<V_{GS}-V_{Th}, the OFET is in the linear mode, the I_{DS} is ascribed:

$$I_{DS} = C_i \cdot \mu_{linear} \cdot \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (1\text{-}1)$$

where C_i is the gate capacitance per unit area, μ_{liner} the field-effect mobility, W is the channel width, and L the channel length of the device. For V_{DS}<V_{GS}-V_{Th}, the quadratic term is typically neglected.

When V_{DS}>>V_{GS}- V_{Th}, the OFET is in the saturation mode, the I_{DS} is ascribed:

$$I_{DS} = (\frac{W}{2L}) \cdot C_i \cdot \mu_{sat} \cdot (V_{GS} - V_{Th})^2 \quad (1\text{-}2)$$

where μ_{sat} the field-effect mobility.

Based on the equation of (1-2), the μ_{sat} which is extremely relevant to evaluate the performance of OFET is obtained and describes a situation when the channel width W is smaller than length L [35].

$$\mu_{sat} = \frac{2L\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2}{C_i W} \tag{1-3}$$

In general, these electrical parameters not only depend on the nature properties of the materials, but also on the structure of the OFET, and on fabrication technologies that may induce traps. In addition, using the equation (1-3), conservative mobility estimates are preferable even considering some of the high mobility materials exhibit non-idealities in their transfer and output characteristics, but many of the reported high-mobility materials exhibit near ideal transfer characteristics [6, 36, 37].

And from the transfer curves, more electrical analysis are discussed and the relative electrical parameters are defined, the details of the other basic parameters are determined as below:

- Contact resistance (R_{tot}): This parameter is opposed to an intrinsic value in a transistor system refers to the contribution on the total resistance of the channel length (R_{ch}) and the electrodes connections (R_c). Consequently, a small contact resistance is preferable.
- Current on–off ratio (I_{on}/I_{off}): The parameter is a ratio value of the maximum I_{DS} to minimum I_{DS}. It is known that a higher “on” current offers better driving capability, while a lower “off” current results in low leakage current [38]. Consequently, a higher I_{on}/I_{off} ratio value is preferable.
- Threshold voltage (V_{Th}): It is a significate parameter that reflects a significant charge is accumulated close to the dielectric/semiconductor interface, which corresponds to the V_{GS}. By using a linear extrapolation of the I_{DS}-V_{GS} at low V_{DS}, the V_{Th} could be obtained.
- Turn-on voltage (V_{on}): This parameter corresponds to the V_{GS} at which I_{DS} starts to rapidly increase. It is easily visible in the log I_{DS}-V_{GS} curves.
- Subthreshold swing (S): this parameter indicates the V_{GS} required to increase I_{DS} by one decade, as seen in the subthreshold region. It is defined in V/decade:

$$S = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1} \tag{1-4}$$

Normally, a small threshold swing indicates lower power consumption and higher switch speed for the transistor device [38].

With these basic electrical parameters, we can analyze the qualitative performances of the OFET device. For instance, considering the operation of n-type OFET, the positive and negative value of V_{Th} could design the device as enhancement and depletion mode, respectively. The enhancement mode is typically preferable as a gate voltage is not necessary to turn off the device [39].

1.2.4 High mobility p-type organic semiconductors

One of the most important step is to choose an OSC material as the active component. The OSC is the OFET device core element because semiconductor controls charge transport in the FET. That's because the device mobility, which is the key parameter for an OTFT, is an indicator of charge transport efficiency through the semiconductor channel. In the past of years, the organic semiconductor materials that have been most used include both sublimed and solution processed semiconductors such as pentacene, tips-pentacene, fullerene, rubrene. The choice of the semiconductor materials highlight several possibilities to develop integrated circuit technologies based on OFET for various large area, low-cost applications. Generally, Organic semiconductors are generally classified into polymers and small molecules. Polymers have lower performance than small molecules, however, polymers are more susceptible and flexible to various deposition techniques. Oxidation and reduction reactions are used to achieve p-type (electron removal) and n-type (electron addition) doping, respectively. Usually, polymers are doped by oxidation, that's why p-type conductive polymers are more common. Here, some of the typical p-type OSCs are presented as below:

• *P-type small molecular*

In the variety of p-type OSCs, pentacene is one of the well-known p-type small molecular and the promising semiconductors with high mobility that has been widely and intensively used in many years. For example, the OFET built on purified pentacene by using parylene gate dielectric obtained the mobility of 2.2 $cm^2V^{-1}s^{-1}$ [40]. A mobility of 1.4 $cm^2V^{-1}s^{-1}$ was found for the pentacene single crystals by using a SiO_2 gate dielectric that treated with self-assembled monolayer (SAM) [41]. Very recently, a carrier mobility of 4.63 $cm^2V^{-1}s^{-1}$ for the pentacene OFET with $La_{0.850}Nb_{0.150}O_y$ as gate dielectric has been reported [42]. And for the pentacene fabricated with flexible substrate, P. Cosseddu et al [43] found the mobility of

$(5\pm2)\times10^{-2}$ $cm^2V^{-1}s^{-1}$ for the pentacene fabricated on poly(ethylene therephtalate) (PET) substrate and using the parylene as dielectric layer. Kwang H. Lee [44] et al reported a higher mobility of 1.22 $cm^2V^{-1}s^{-1}$ for pentacene based OFET deposited on polyethersulfone (PES) substrate. Furthermore, the OFET based on a bulk and ultrapure single crystal of pentacene was reported to exhibit very high hole mobilities values in the range of 15~40 $cm^2V^{-1}s^{-1}$ at room temperature by using 6,13-pentacenequinone (PQ) as the gate dielectric [45]. Otherwise, rubrene is another p-type small molecular that used extensively in OFET devices, it also has exhibited the optimized charge carrier mobilities as high as ~15 $cm^2V^{-1}s^{-1}$ by a fabrication method of laminating a monolithic elastomeric transistor stamp against the surface of a crystal [46] and the mobility is even maximized to ~43 $cm^2V^{-1}s^{-1}$ [47].

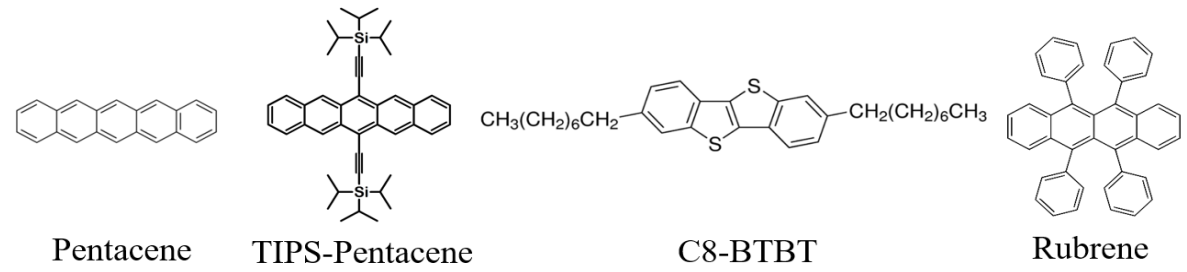
In addition, a functionalized small molecule pentacene, 6,13-bis-(triisopropyl-silylethynyl) (TIPS-pentacene) has been researched widely because of their relatively high field-effect mobility and soluble in many common solvent with solution process ability. The mobility of TIPS-pentacene has been reported as 4.6 $cm^2V^{-1}s^{-1}$ with the shortest π-π stacking distance of 3.04 Å achieved by lattice strain that prepared by a solution-shared technique [48]. And Zhenan Bao et al showed the mobility of Tips-pentacene up to 2.7 $cm^2V^{-1}s^{-1}$ that designed OFET with very small pattern [49]. Jae-Joon Kim et al reported highly crystalline and self-assembled TIPS-Pentacene with maximum mobility of 3.40 $cm^2V^{-1}s^{-1}$ that formed by simple spin-coating [50]. TIPS-pentacene also deposited on flexible PEN substrate and showed a promising performance with a mobility of 0.8 $cm^2V^{-1}s^{-1}$ [51]. Totally, the mobility of TIPS-pentacene based OFET was improved up to 11 $cm^2V^{-1}s^{-1}$ through a "fluid-enhanced crystal engineering" device fabrication approach [52].

In recent years, a small molecule 2,7-dioctyl[1]benzothieno[3,2-b][1]-benzothiophene (C8-BTBT) has attracted much attention since it is ultra-transparency, and with high mobility. A maximum hole mobility values of 31.3 $cm^2V^{-1}s^{-1}$ for C8-BTBT was obtained by printing method [53]. And it even showed mobility values as high as 43 $cm^2V^{-1}s^{-1}$ by using a blended solution with polystyrene [54]. Very recently, the hole mobility of C8-BTBT at room temperature reaches 6.50 $cm^2V^{-1}s^{-1}$ by easy treatment way with UV-ozone exposure on the SiO_2 surface [55].

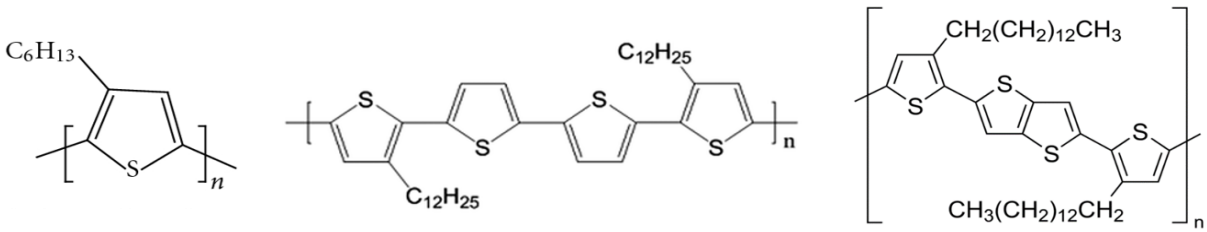
• *P-type polymer semiconductors*

For the OFET fabricated with polymers OSCs, a large effort and several strategies have been developed these years, and several materials with home mobility over 1 $cm^2V^{-1}s^{-1}$ have

been reported [56]. Basically, poly-(3-hexylthiophene) (P3HT) is the benchmark p-type polymeric OSCs for OFET with mobility of 0.1 $cm^2V^{-1}s^{-1}$ [57]. Poly-(3,3-dialkylquaterthiophenes) (PQT) [58], poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b] thiophene) (PBTTT) [59] were introducing functionalized groups into the main chain of polythiophenes, improving the mobility up to $cm^2V^{-1}s^{-1}$. The mobility of co-polymers reported in reference (Ref.) [60] with donor-donor type structure by integrating the advantages of PQT and PBTTT was 4.6 $cm^2V^{-1}s^{-1}$, respectively. However, among the many types of polymers, donor-acceptor type co-polymers dominate the highest mobility in OFET application. Co-polymers based on fused PBTTT derivatives are interesting polymers with mobility up to 10 $cm^2V^{-1}s^{-1}$ [56, 61]. Further improvement of long-range orientation of the polymer chains based donor-acceptor co-polymers obtained much improved mobility, the mobility reached up to 23.7 $cm^2V^{-1}s^{-1}$ in Ref. [62] and 21.3 $cm^2V^{-1}s^{-1}$ in Ref. [63]. Figure 1.7 shows the molecular structures of some typical P-type organic semiconductors with high mobility (a) small molecules (b) polymers.



(a) P-type small molecules



(b) P-type polymers

Figure 1.7 Molecular Structures of some typical P-type organic semiconductors with high mobility (a) small molecules, (b) polymers.

In this part, several p-type representative OSCs are mentioned, much more high mobility of OSCs were reported in detail in the review references of [64]. As using the n-type OSCs in OFET devices, the electrons should be injected into LUMO level of the semiconductor, and most of the values of energy diagrams at the LUMO level are around 4.0 eV, thus, it needs relatively low work function electrodes for better charge injection. However, the electrodes with low work function is not as stable as gold (Au), platinum (Pt) electrodes with high work function in the air, thus we considered to use typical p-type semiconductor. Moreover, pentacene, which is an aromatic hydrocarbon and is shown in figure 1.7, is one of the promising materials with high mobility and has been widely and intensively studied that more than 1000 articles related to pentacene transistors have been reported in scientific journals confirming its considerable importance. The subjects in these reports include device physics, growth, crystallography, electronic transport, dielectrics, surface science and device applications contribute to amount of progression for pentacene FETs [65]. In this thesis, the p-type small molecule of pentacene is preferable to be used for realization out OFET and NFGM devices.

1.2.5 Pentacene based OFET

In previous part, the examples of pentacene with high mobility has been presented. As the pentacene is chose as the semiconductor material in this thesis, here some represents of the performances and the progresses of pentacene based OFETs in the publications are demonstrated. An amount of studied of pentacene FETs has been reported, in attempt to improve the performances of the transistor devices, the research subjects generally include the device physics such as thin films growth, crystallization, dielectrics, interface and surface science and so on.

• *Pentacene thin films*

Pentacene molecule could be deposited on the substrate by vacuum thermal evaporation and solution process [66]. However, pentacene is essentially insoluble in organic solvents at room temperature, and most of the pentacene prepared by vacuum deposition has been reported with high mobility, in this section, the pentacene thin films deposited by thermal are presented. In general, thin films growth modes on substrates are generally classified into three modes: layer-by-layer (Frank–van der Merwe), layer followed by island (Stranski–Krastanov) and island (Volmer–Weber) growth modes [65], as shown in figure 1.8. Normally, for the pentacene growth on a substrate corresponds to the Stranski–Krastanov mode with the following

elementary processes [67]. First, the molecule sublimating from the source with heating, adsorbs and diffuses on the substrate. Then the molecules aggregates on the surface of the substrate and with a critical numbers to form a two-dimensional (2D) island, and gradually form monolayers, the growth mode finally transforms to three-dimensional (3D) as the deposition continue to increase. The thin films growth mode and morphology are greatly related to the conditions of the deposition process (deposition rates, substrate temperature, and kinetic energy of the sublimating molecules) and the substrate surface conditions (dielectrics, surface roughness).

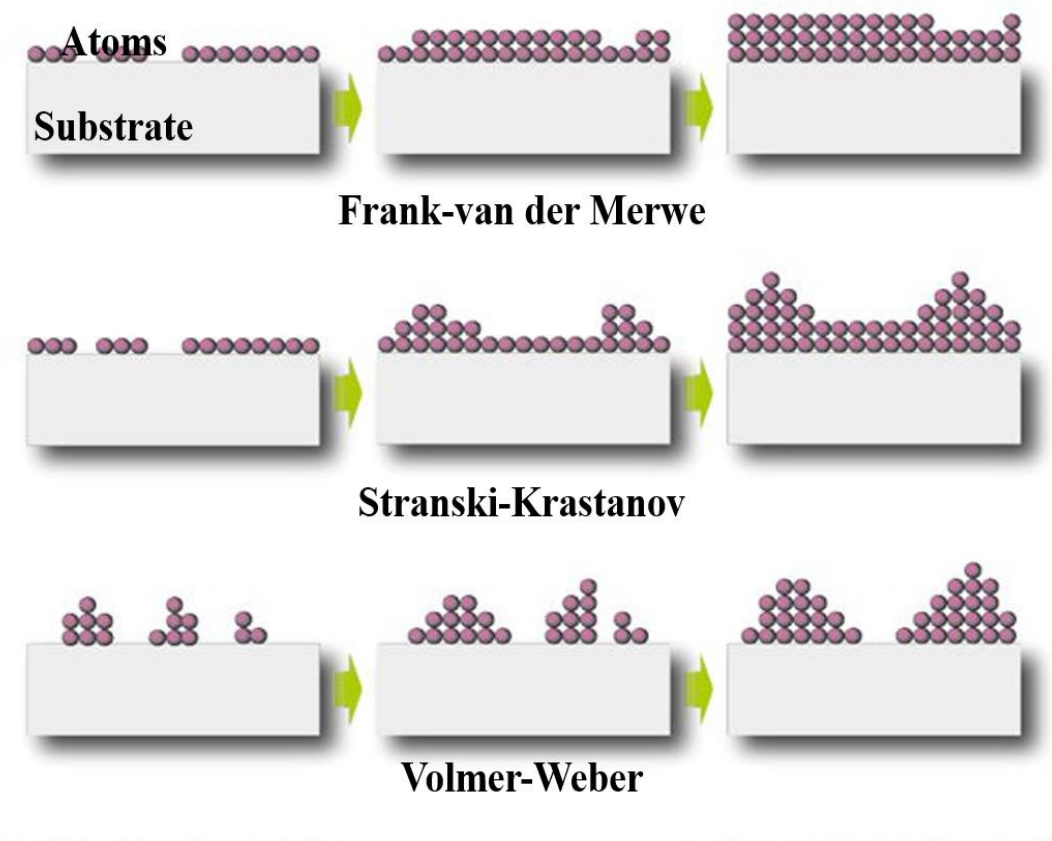


Figure 1.8 Thin films growth modes.

As shown in figure 1.9, the AFM images of 1 nm thick pentacene deposited on a SiO_2 surface [65]. The 2D islands were observed for all the samples with deposition rates are (a) 0.12 nm min^{-1}, (b) 1.2 nm min^{-1} and (c) 12 nm min^{-1}. In the literature of [68], B. Stadlober et al have also reported an extended and quantitative analysis of pentacene with submonolayers (2D islands) were formed on dielectric layers of SiO_2, polymethylmethacrylate (PMMA), poly-4-

vinylphenol (PVP) and PVCi-polyvinylcinnamate under different substrate temperatures. It indicates that the density of the 2D island strongly depends on the deposition rate.

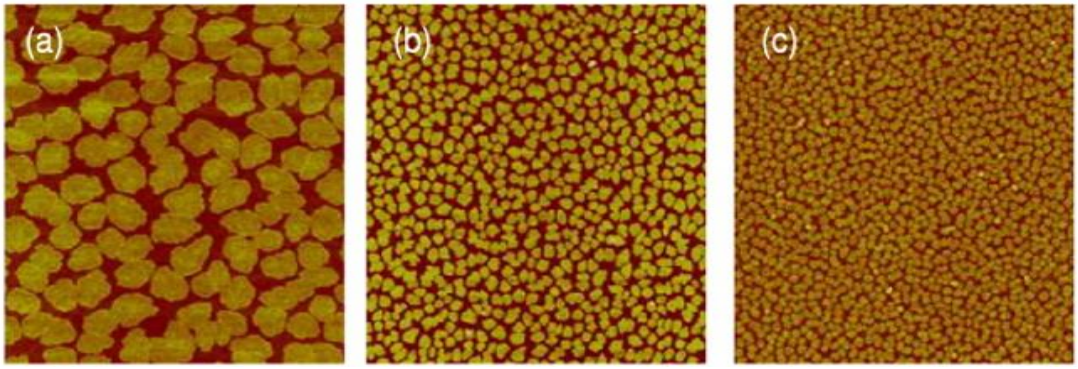


Figure 1.9 AFM of 2D pentacene thin films (thickness 1 nm) deposited on a SiO_2 surface. The AFM image size is 5 μm × 5 μm. The deposition rates are (a) 0.12 nm min^{-1}, (b) 1.2 nm min^{-1} [65].

For the thick pentacene thin films, the density of the 3D crystal grains also depends on the deposition rate, but less than that of the 2D island. This indicates that the 3D grain results from coalescence of small islands. As shown in figure 1.10, B. Stadlober [68] et al also analyzed the dependence of N_{sat} on R at the initial phase of film growth for a large number of 50 nm thick pentacene films grown on SiO_2 at room temperature. The examples for rate-dependent morphology are given which illustrate that multilayer pentacene films are coarse for low deposition rate and fine grained if R is increased significantly beyond 1 nm/min. The determination of the nucleation density in thick films is not as straight forward as for submonolayer films. On the other hand, according to the results that N_{sat} was obtained by counting the number of maxima in the AFM micrographs in Ref. [69], Tejima et al have shown that the grain density does not depend on the nominal thickness of pentacene in the range of 11-46 nm, It indicates that coalescence of 2D islands completes up to 11 nm.

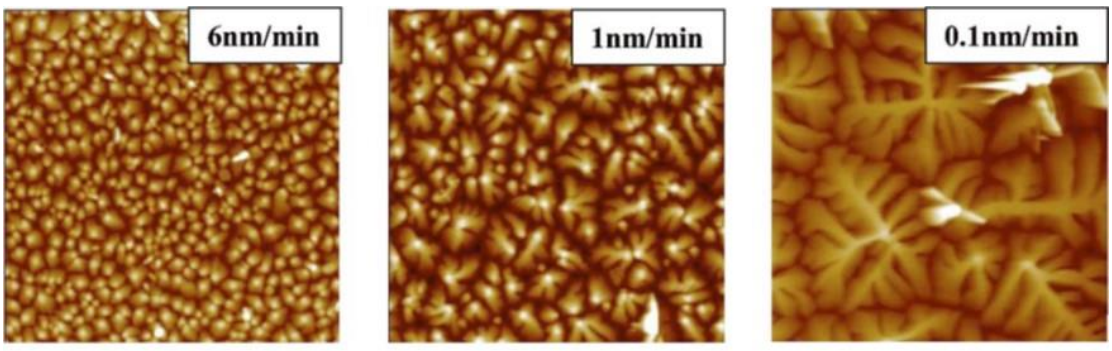


Figure 1.10 Three examples for rate-dependent morphology in thick pentacene films are given in the upper row AFM height micrographs, 5 μm × 5 μm [68].

In addition, another principal condition to influence the growth of pentacene thin films is substrate temperature. In general, grain size increases with substrate temperature, the nucleation density is significantly higher at room temperature than at any other substrate temperature, correlating to the average grain area that is smallest. And the ratio of the bulk phase to the thin-film phase increases with substrate temperature [68, 70].

• *Effects of the Interfaces*

In order to fabricate high-performance OFETs, research efforts have been focused on improving the electrical properties of the semiconductor as well as the gate dielectric and the conducting electrodes. Along with the material properties of each layer in the device, interface properties of the metal-semiconductor and insulator-semiconductor have a strong influence on the device performance [71]. As shown in figure 1.11, during the charge transport in the p-type semiconductor under the operation, one hand, the interface roughness, defects and charges between insulator and OSC and around this region have a strong effect on the carrier life time and the mobility [72]. On the other hand, the contact resistance will affect the carrier movement through the interface and low barrier height contact is needed between the source/drain (S/D) electrode and OSC, especially with the decreasing device dimensions, the contact resistance as a part of the total device resistance will dominate over the channel resistance, and therefore the speed of organic integrated circuits may be limited by the contact resistance, not by the intrinsic carrier mobility of the organic semiconductor [73]. Thus, optimization of the interface is one of the important factors for OFET performance along with the insulator–semiconductor interface.

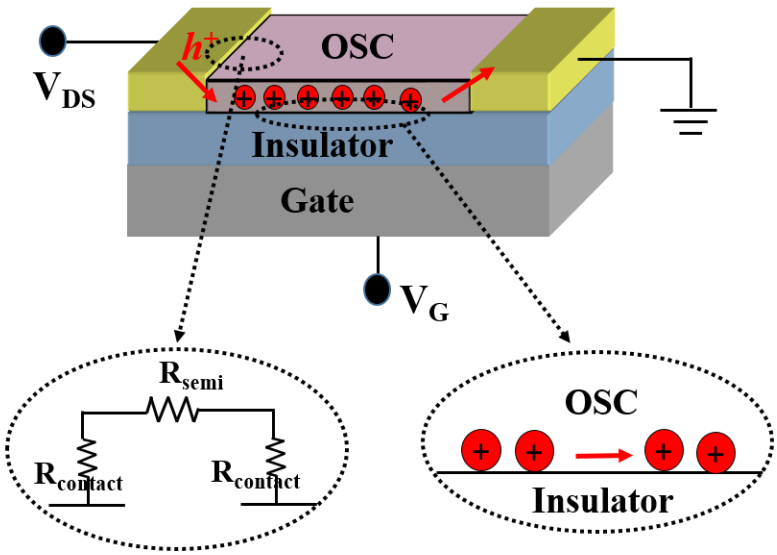


Figure 1.11 Schematic diagram of an organic thin film transistor with metal–semiconductor and insulator-semiconductor interfaces.

The pentacene grain size is significantly affected by the roughness and surface energy of the substrates, for example, the grain size of pentacene that deposited on SiO_2 with different surface roughness decreases with the increasing surface roughness [74]. As the different roughness and surface energy for different dielectrics, the morphology and even the performance of the OFET are quite difference. Yang et al reported that the pentacene deposited on the polymer surface with high surface energy had a large grain [75]. Moreover, pentacene grown on a substrate with low surface energy, such as SiO_2 surface treated with a monolayer of organic chemicals octadecyltrichlorosilane (OTS) has lower surface energy than inorganic SiO_2 surfaces, the pentacene thin films have a significantly smaller grain size than that for an untreated SiO_2 [76].

Otherwise, the charge carrier mobility of pentacene FET is also sensitive to the surface properties of the dielectric layer, since the majority of charge carriers in an OFET are located at the semiconductor-dielectric interface [77]. Normally, the surface properties of the dielectrics could be simply controlled by the modification with a SAM in an OFET. The SAM technique ensues when molecular assemblies are formed spontaneously on the surfaces by adsorption and are then organized into relatively large ordered domains, which is shown in figure 1.12. It enables the fabrication of closely packed, well-ordered and organized multilayer films from oriented monolayers and allow for the immobilization of several functional molecules onto the surfaces [78].

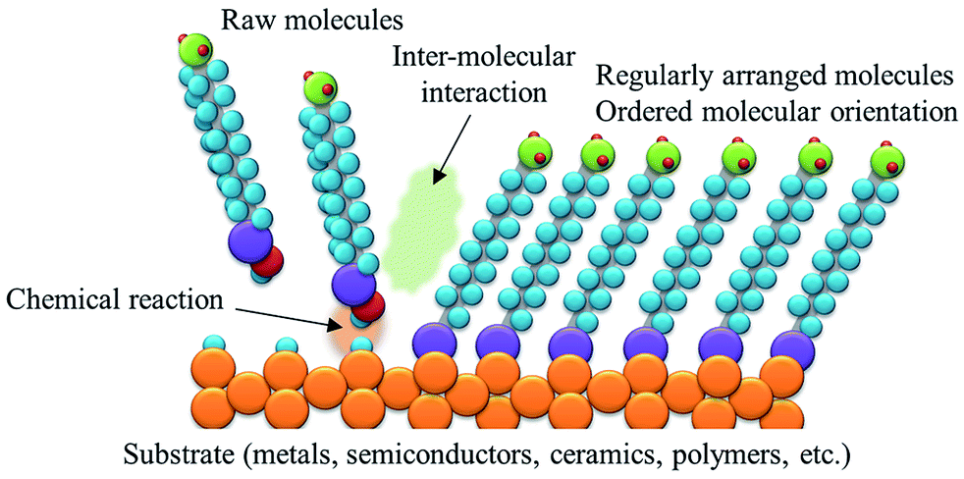


Figure 1.12 A schematic for SAM technique [78].

Figure 1.13 shows TM-AFM topographies for 60-nm-thick pentacene films deposited on HMDS- and OTS-treated surfaces, as well as the I-V characteristics of OFET devices

deposited on (c) HMDS- (d) OTS-treated SiO_2/Si substrates that presented in Ref. [77]. From the analysis TM-AFM topographies corresponding the mobility measurements, by using 60-nm-thick pentacene films in the top contact, the HMDS and OTS-treated samples have a similar vertical conducting path for top contact devices, however, the terrace-like multilayered pentacene films, grown on single crystal-like faceted islands in the first layer i.e. HMDS-treated surface, have shown much higher field-effect mobility of 3.4±0.5 $cm^2V^{-1}s^{-1}$ than those grown on polycrystalline dendritic islands, i.e. on OTS-treated surface with mobility of 0.5±0.15 $cm^2V^{-1}s^{-1}$.

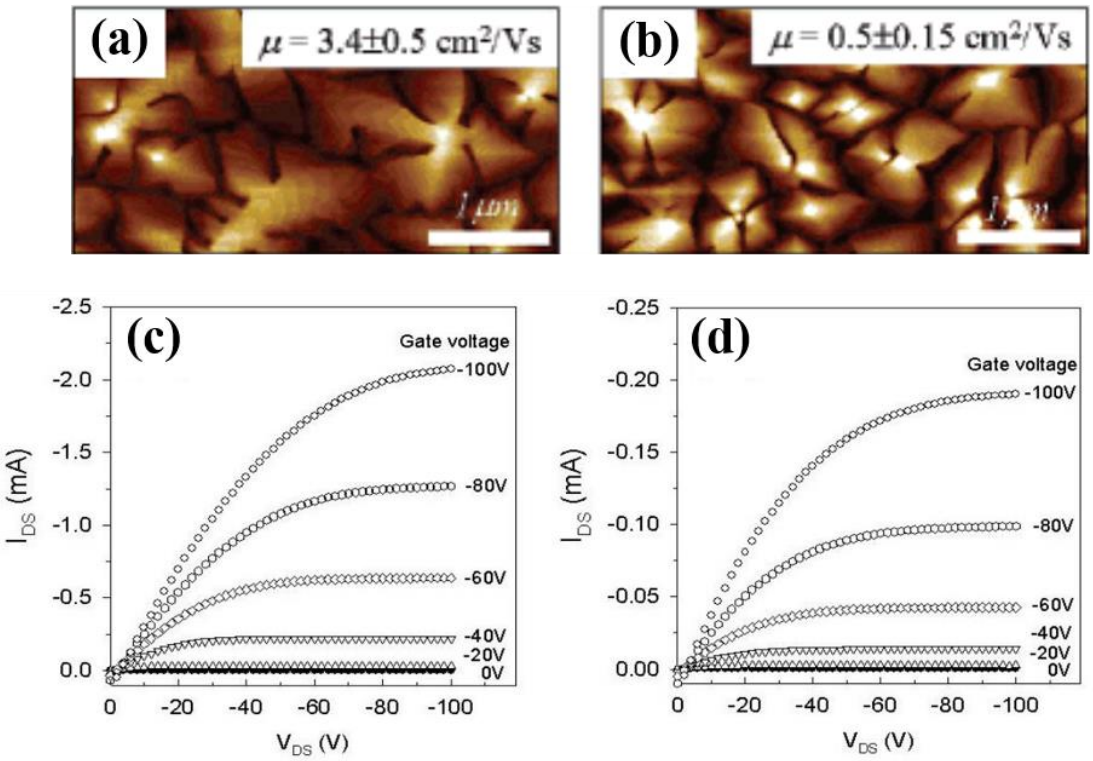


Figure 1.13 TM-AFM topographies of 60-nm-thickpentacene films on (a) HMDS- and (b) OTS-treated SiO_2/Si substrates, I-V characteristics of OTFT devices with 60 nm thick pentacene films deposited on (c) HMDS- (d) OTS-treated SiO_2/Si substrates [77].

In attempt to reduce the power consumption for the OFET devices, typically decreasing the operation voltages is a good way. For existing OFET using conventional SiO_2 gate dielectrics, the operating voltages always exceed 20 V because of the thickness of SiO_2 (200–300 nm) and the high interfacial trap densities. Thus, high dielectric-constant (high-k) materials such as TiO_2, Al_2O_3, and HfO_2 have been utilized to resolve the challenge of low voltage [34], and also using double poly(vinylidene fluoride/trifluoroethylene) [P(VDF-TrFE)]/poly-4-vinyphenol (PVP) (high-k/low-k) polymer[79], as well as using organic–inorganic blend

dielectrics that prepared under lower temperatures and ambient conditions to obtain low operation voltages [80].

• *Pentacene based flexible OFET*

The electronic devices formed on flexible substrates are essentially expected to meet emerging technological demands where silicon-based electronics cannot provide a solution. Examples of active flexible applications include rollable displays, conformable sensors, and wearable computers [81]. As the organic semiconductor and organic dielectrics could be deposited with low temperature and large area, they have the advantages to realize flexible electronics. During these years, the pentacene has been widely studied to realize flexible OFET devices and remains attracted attentions [34, 81-83]. As shown in figure 1.14, the performances of pentacene fabricated on PET substrate and using PMMA and PVP as the dielectric layers. And Very recently, S. Zhou et al also reported the flexible pentacene TFTs were fabricated by depositing the pentacene thin film on the elastic polydimethylsiloxane (PDMS) dielectric layer with PET supporting layer. As a consequence, it motivates us to realize flexible OFET by using pentacene semiconductor in this thesis.

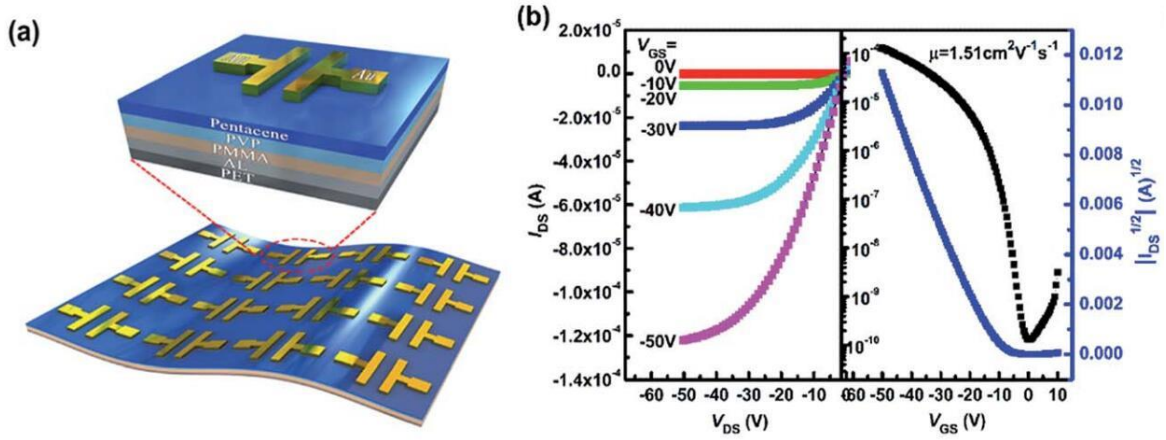


Figure 1.14 (a) The schematic illustration of the pentacene-based flexible OFETs, (b) the representative output and transfer characteristics of flexible pentacene-based OFETs [84].

1.3 Overview of OFET based nano-floating gate memory

1.3.1 Structure and operations

As mentioned in the background, the OFET based nano-floating gate memory has the similar structure as a single organic transistor that a charge-storing medium like NPs or NCs act as floating gate between two dielectric layers [84]. For a conventional floating gate flash memory, because the floating gate is continuous and conductive, all charge stored in the floating gate will be lost if a leakage path appears in the tunneling oxide when the scale is minimized. Thus, discrete nanocrystal memory was proposed first by IBM in 1995 to solve the scaling miniaturization problem, the nanocrystal memory has a two bit per cell storage capability due to its discrete electron storing center, which readily increases the memory density. After that, an amount of NFGM by using discrete NPs were also proposed and studied [85].

For the scaling of NFGM devices to achieve low-voltage, single-electron operation at room temperature, the features of the structure are as follows:

(i) the floating gate dimensions should be small enough to increase the energy level spacing by quantum confinement and the Coulomb blockade;

(ii) a thin tunnel layer is preferable to allow direct tunneling to increase the memory speed;

(iii) the gate oxide has to be thicker to prevent “gate-to-dot” and “dot-to-dot” tunneling;

(iv) the device needs to have low interface state densities to reduce offset charges.

The operation mechanism of organic NFGM is very similar to that of conventional Si-based flash memory devices. Information is stored in the NPs by injecting or rejecting (charge or discharge) charges under applying a suitably strong external electric field is applied to the gate electrode of the memory device, thus followed by a threshold voltage shifts in relation to the memory states called programming and erasing operation (write and erase), respectively. Therefore, the shift value of V_{Th} respect to the applied program/erase bias pulses defines as the memory window. The digital “0” or “1” (“on” state or “off” state) memory status is determined by applying a read voltage to the gate between the program and erase operations to read the corresponding drain current. Note that the read voltage is much lower than the programming voltage.

The program and erase operations are depicted in figure 1.15(a). Figure 1.15(b) and (c) schematically illustrate the energy band mechanisms of the program and erase processes for an n-type NPs memory device based SiO_2 dielectric layer. During the write process, a positive gate

voltage is applied to the control gate to inject electrons rom the channel into the NPs. The application of a reverse bias causes the reverse tunneling of electrons into the channel [85].

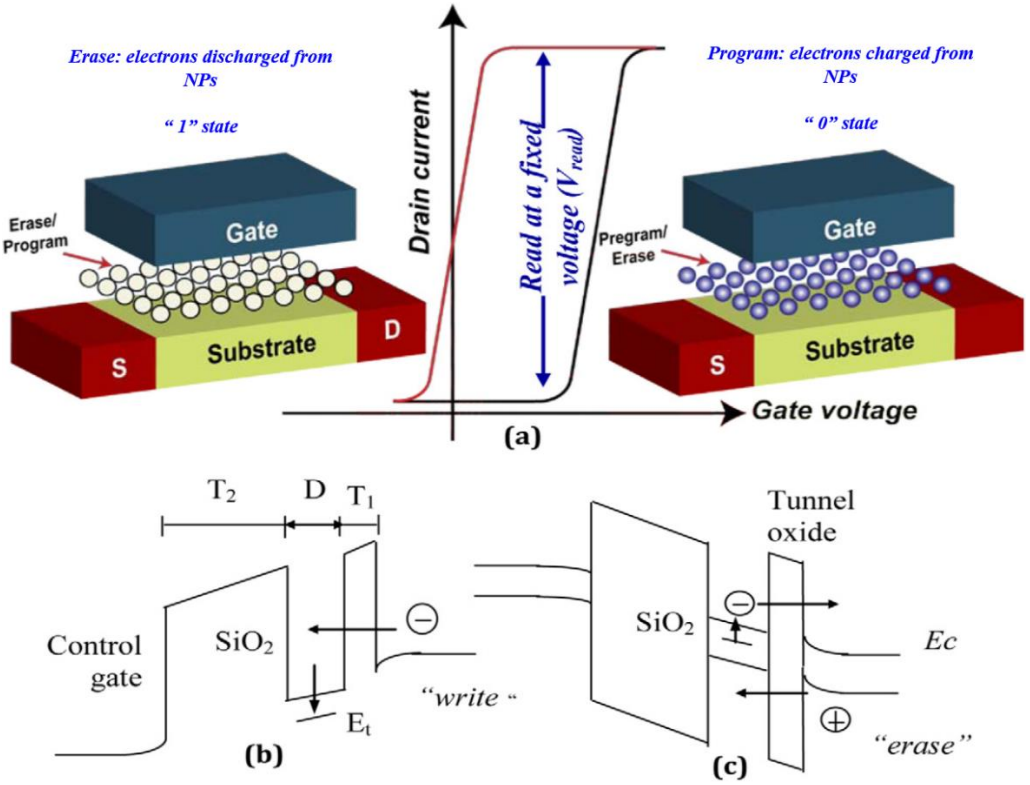


Figure 1.15 (a) Schematic of the program and erase operation in a NFGM device. A schematic band diagram illustrating (b) write and (c) erase processes in a Si based NFGM device [84].

1.3.2 Nano-floating gate layers

The nano-floating gate layer as the key device element in NFGM has been focused all the time during the research. The first formation of nanocrystal-based charge-trapping flash memory devices was reported by Tiwari et al [86], they used Si nanocrystals embedded in the gate oxide as the charge-storage element based on a conventional n-channel metal-oxide-semiconductor transistor, and the Si nanocrystals were synthesized by chemical vapor deposition. Since the early report, considerable progress has been made on the fabrication of nanocrystal-based memory over the years. Currently, for the charge floating gate, varied materials have been investigated to use for the charge-storing medium, for the medium that most commonly used, semiconductive or metallic nanoparticles that have been thermally deposited or chemically assembled [87], nanocomposites (e. g. Polymer/ZnO) [88, 89], carbon-based charge trapping materials (e. g. C60 or graphene) [90, 91].

In the kinds of the charge-storing medium, the metallic nanoparticles are the most widely used floating gate layer as the sample preparation process and easy to control the density of the particles. For example, figure 1.16(a-d) shows the TEM images of various metals NPs, including those of Au, Ag, Cu and Al, as a floating gate layer in NFGM devices that reported in Ref. [87]. The NPs were inserted between the bilayers of various polymer dielectrics (polystyrene (PS)/poly(4-vinyl phenol) (PVP) or PS/poly(methyl methacrylate (PMMA)). The effects of metallic NPs and gate dielectrics were investigated and compared in the literature, and the best performing P(NDI2OD-T2)-based NFGM devices were found as the ones fabricated using PMMA and Au NPs.

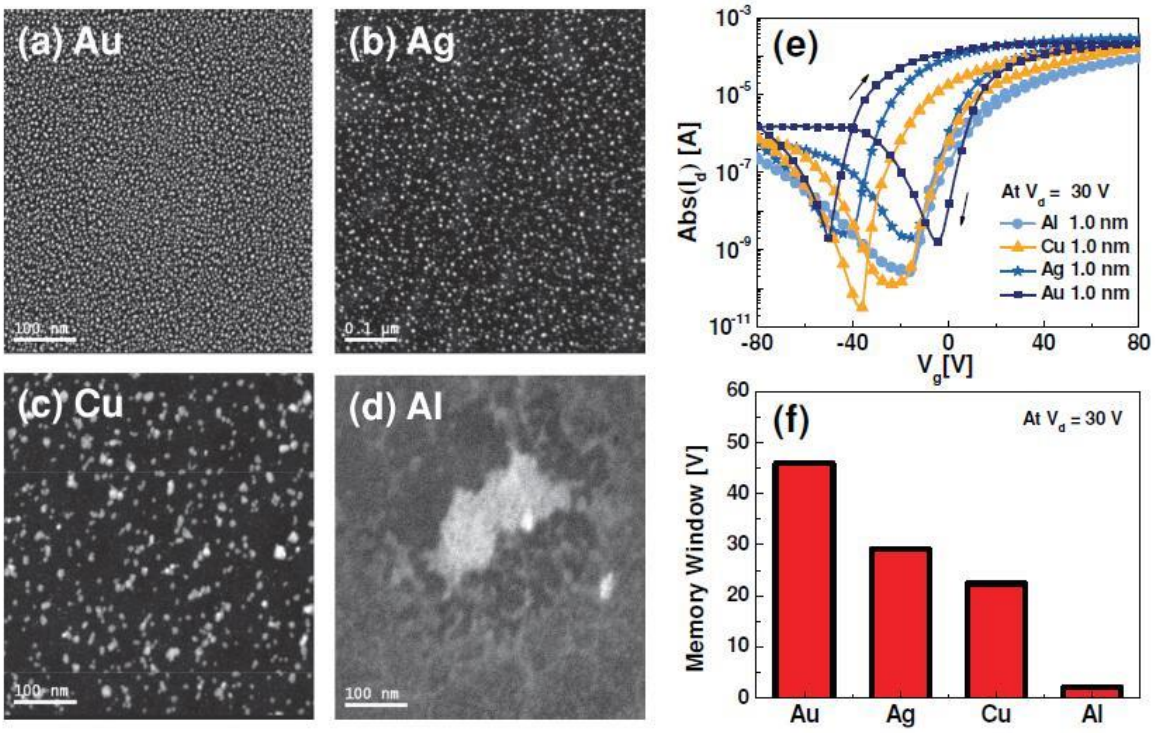


Figure 1.16 (a-d) TEM images of the various thermally deposited metallic NPs (1.0 nm thick deposited): (a) Au, (b) Ag, (c) Cu, and (d) Al. (e) Memory hysteresis loops and (f) corresponding memory windows of the transfer plots, Abs(I_d) vs Vg at Vd=30 V, for the OFETs fabricated with various metallic NPs, i.e., those of Au, Ag, Cu and Al [87].

Furthermore, the 2D nanomaterial of graphene and derivative graphene like graphene oxide and its reduced form (rGO) have been adapted as charge trapping media for more efficient charge trapping but also better compatibility with solution processes. For example, Dai et al developed an organic nano-floating gate memory (NFGM) device using solution-processed graphite nanocrystals as nano-floating gate materials [92]. Mi Jung Lee et al fabricated an n-type charge-trapping memory device with rGO as the charge-trapping layer on the flexible

substrate using all-solution processes [91]. Very Recently, Tae-Wook Kim et al demonstrated a graphene quantum dots (GQD)-based organic NFGM device using pentacene as the organic channel layer and PS as the tunneling layer [93].

Most of organic NFGMs exhibit relatively poor device characteristics along with markedly shorter retention times, therefore, the NFGM with double floating-gate were proposed to optimize the performances of NFGM devices [94-96]. For instance, S. T. Han et al reported a hybrid double floating-gate memory device by utilizing an rGO-sheet monolayer and an Au NP array as upper and lower floating gates, respectively. The rGO acts as buffer layer at the interface between the Au NPs and the pentacene and decreases the surface roughness, consequently enhancing the electrical characteristics of the DFG devices, as shown in figure 1.17 [94]. When keep the density of the Au NPs at ~1.3×10^{11} cm^{-2}, rGO coverage at ~90%, the memory window of the DFG memory reaches the largest value of 1.75 V and retention time is up to 10^5.

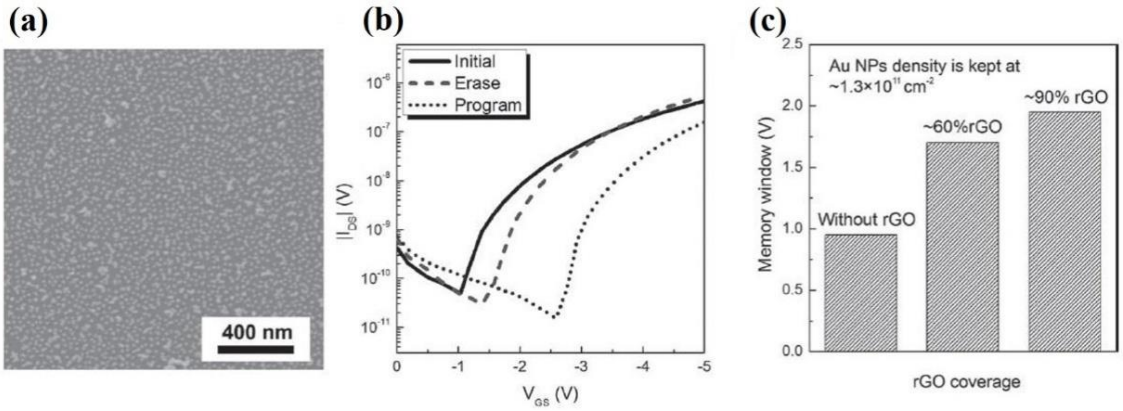


Figure 1.17 (a) SEM image of self-assembled 15 nm Au NP monolayer with a density of around 1.3 $\times10^{11}cm^{-2}$, (b) Transfer characteristics of DFG memory device, (c) Memory window with respect to different densities of rGO while the density of the Au NPs is kept at $\approx1.3\times10^{11}cm^{-2}$ [94].

1.3.3 Pentacene based NFGM

For fabrication of NFGM devices on rigid or flexible substrates, pentacene has been widely selected and studied as the active layer [92-104]. Over the years, many efforts have been devoted to optimizing the floating-gate layers. Besides the floating-gate layers, the blocking and tunneling dielectric layer also has a direct impact on memory performance of floating-gate OFET memory devices [103]. Examples of the research that reported very recently, M. D. Yi et al obtained the improvement of the NFGM devices with high density porous structure of PMMA tunneling layer that was mainly attributed to both the high charge capture and release

efficiency and the high electrical insulating property [103]. Tae-Wook Kim et al used the method that one-step synthesis of Au NPs by simple annealing of the solid phase PAN and an Au salt to fabricate the NFGM and found the excellent performances of the memory, as shown in figure 1.18 [102]. The memory devices exhibited a high on/off ratio (over 10^6), large hysteresis windows (76.7 V), and stable endurance performances (3000 cycles). Otherwise, the multilevel charge storage phenomenon was also found in pentacene based NFGM. The multilevel transistor memories can be utilized to increase the memory capacity without decreasing the size of the device to the nanoscale [98].

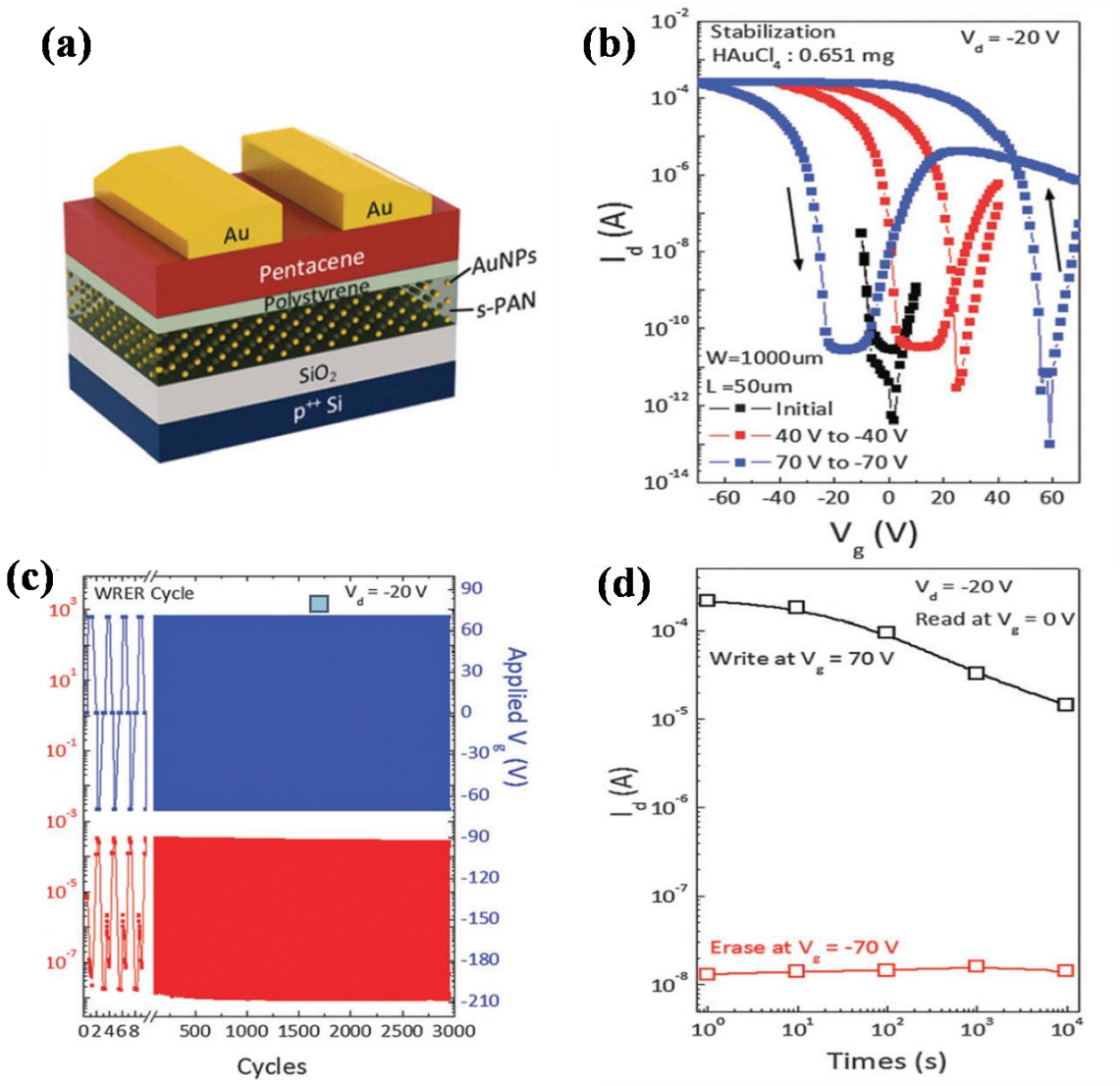


Figure 1.18 (a) The device structure of the memory with p++ Si/SiO_2/Au NPs in PAN/PS/pentacene/Au. (b) Transfer characteristics of NFGM. The transfer curves were measured by a gate double sweep with ranges of ±40 V and ±70 V at V_d =-20 V. (c) Endurance test results of the cyclic write-read-erase-read (W – R – E – R) test. (d) Retention time test results of the written state and erased state [102].

Considering the effects of materials and process conditions, the characteristics of the pentacene based NFGM were improved more or less that have been reported. Table 1-1 shows the summary of key characteristics of pentacene based FET memory devices that reported in the Refs in recent years.

Table 1-1. Summary of key characteristics of pentacene based NFGM devices that reported in the Refs in recent years. (P/E: Program/Erase)

Substrate/ dielectrics	Charge store medium	$V_{P/E}$ (V)	Mobility ($cm^2V^{-1}s^{-1}$)	Memory window (V)	I_{on}/I_{off} (V)	P/E cycles	Retention time (s)	Ref
PES/cross-linked PVP	Au NPs	±90	0.25	10	$>10^2$	700	10^5	[97]
PET/Al_2O_3	Au NPs	±50	-	16.5	3×10^3	1000	$>10^5$	[98]
PET/Al_2O_3	rGO sheets/ Au NPs	±5	0.1	.95	$\sim10^3$	1000	10^5	[94]
Glass/HfO_2	CuPc NPs +N-C_{60}	±5	0.0125	4.2	8.3×10^3	500	10^4	[96]
Si/SiO_2/	Graphene	±80	0.061	~40	10^5	110	$>10^5$	[99]
Si/SiO_2	Ferritin NPs	±100	0.013	>20	10^4	200	10^4 ($>10^7$)	[100]
Si/SiO_2	Au NPs +Pt NPs	±45	0.53	18.7	$>10^5$	600	10^4	[101]
Si/SiO_2	S-PAN +Au NPs	±70	0.809	76.7	$>10^6$	3000	$> 10^4$	[102]
Si/SiO_2/ Porous PMMA	Au NPs	-120 /+80	0.49	43	10^5	300s	10^4	[103]

From the summary of the characteristics of pentacene based NFGM devices that reported in recent years, we can see that most of the pentacene NFGM devices are fabricated on rigid substrates of silicon [96, 99-103], and the tunneling and blocking layers are mainly inorganic dielectrics like SiO_2 and Al_2O_3, which needs relatively high temperature to deposit. For the flexible NFGM [94, 97, 98], only Ref. [97] used organic as the blocking layer, however, the operation voltage is very large (±90 V), the memory window is small, and the current on/off ratio is low. Hence, it signifies to develop new approach to improve the memory performances and the realization of flexible NFGM by using all organic materials are worth to going to research.

1.4 Conclusions

In this chapter, we describe the state of the art of OFET and NFGM and the motivation of this thesis is presented. In detail, the configurations and the operations of the OFET and the NFGM are presented first. Then, the typical high mobility organic semiconductors that used in OFET devices are represented. From the research of widely literatures and the point of commercial applications, the pentacene is chosen as the organic semiconductors to fabricate our OFET and NFGM devices in this thesis. Thus, the progress of pentacene based OFET and NFGM in recent years has been introduced. Finally, from the summery of the recent reports that involved of pentacene NFGM, the Au NPs and rGO sheets are chosen as the floating gate in this work, in addition, the dielectric materials and the structures were mainly taken into consideration for this work and our aim is to obtain high performances of OFET and NFGM on rigid and flexible substrates.

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Chapter 2
Preparation and optimization of organic transistors

Chapter 2 Preparation and optimization of organic transistors

2.1 Introduction

Organic field-effect-transistors (OFET) have been extensively studied in electronic applications due to its advanced advantages, such as low-cost, high integration, flexibility, and compatibility with biosensors [1-5]. However, commercial breakthrough is still ahead with considerable effort in fundamental improved as well as applied research currently undertaken. All these devices have in common organic semiconductor layers with processing a non-vanishing energy gap between occupied and empty electronic states, and must be inevitably realized with a range of metals because of the electrical connection of organic semiconductor to peripheral circuitry [6]. Thus it signifies to control the way of the charge transport between organic and metals. As we all know, the electrical performance of OFET is often measured in terms of the carrier field-effect mobility [7]. The carrier mobility is correlated with the charge transport performance in the dielectric/organic semiconductor device, which could be closely connected with the surface treatment, temperature, material purity, device structure, deposition vacuum conditions and so on [8]. Hence, it's also motivated to analyzing and tuning the way of charge transport between organic and dielectrics.

During recent decades, an important approach of tuning charge transport is proposed by inserting SAMs on the surface of dielectrics or electrodes [9-12]. Charge transport takes place primarily within the first few monolayers at the dielectric/semiconductor [10]. For instance, the hydrophobic nature of 3-octadecyltrichlorosilane (OTS) has been widely used to modify the SiO_2 dielectric surface, results in improvement of the mobility of varies OFETs, which could be explained by the increase of the semiconductor crystallinity, reducing interfacial trap states and planarize the surface [13, 14]. And a number of thiol-based SAMs such as 1-hexadecanethiol [13], 4-fluorothiophenol, and 2,3,4,5,6-pentafluorobenzenethiol (PFBT) [15,16], deposited on the source and drain electrodes of OFETs have demonstrated improvements to the contact resistance and channel transistor performance. Very recently, Tomoharu Kimuraet al [16] directly investigated the local impedance and the potential difference at the electrode-channel interfaces of the OFET using frequency modulation scanning impedance microscopy (FM-SIM) presumed the reduction of the hole trap sites at the

source-channel interfaces by using PFBT-modified OFET. Nevertheless, the hybrid contacts with both SAMs on electrodes and dielectrics are rarely reported, especially the way for explaining the charge transport mechanisms in the two kinds of SAM contacts is expected to explore.

In this chapter, the fabrication process and analysis instrumentations used for our OFET samples are described in detail. The physical and electrical properties of different SAM modified pentacene FET devices were performed and discussed, i.e. pentacene deposited on OTS modified dielectric surfaces, on the PFBT modified source/drain electrodes, and on the cumulative OTS and PFBT modified surfaces. The FET of pentacene deposited on bare SiO_2 was fabricated as a reference. Through the SAM modification, optimized electrical performances were obtained and the charge transport mechanisms were explained, which highlights the utility of surface modulations to tune charge transport in nanoscale materials. The results also support the application of SAM on our memory devices for further research.

2.2 Fabrication of pentacene based OFETs

To obtain the OFET samples in our experiments, the fabrication process is including cleaning the substrate, getting gold electrodes by e-beam lithography, deposition SAM by chemical reaction, as well as deposition pentacene semiconductor by thermal evaporation. The details of the mainly fabrication processes for the four different OFETs samples are described below.

2.2.1 Electron-Beam Lithography technology

As electron-beam lithography (EBL) is one of the crucial technology used for the fabrication of micro- and nano-devices with the merits of mask-free and high resolution. The ideal pattern realization is based on the solubility changeable of polymer resist films after irradiated by a focused beam of electrons. After the irradiation, it enables a selective removal of resist by immersing the sample into a solvent because of the different solubility of the resist exposed/non-exposed by electrons. The transistor devices prepared in our work with bottom contact of Au source and drain electrodes were fabricated by EBL with channel length from 1 μm to 50 μm and channel width 1000 μm, respectively. To prepare the source/drain electrodes for our transistor devices by EBL, the fabrication process is carried out in the yellow light room

and mainly following 7 steps. Figure 2.1 shows the mainly schematic diagrams of e-beam lithography experimental process.

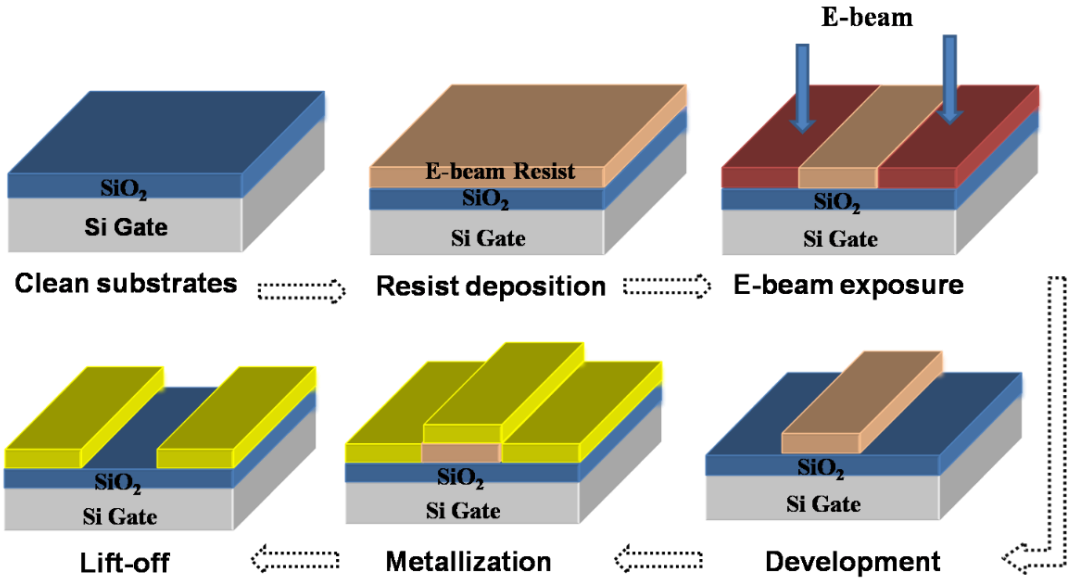

Figure 2.1 The schematic diagram of e-beam lithography experimental process.

Step 1: Designing mask

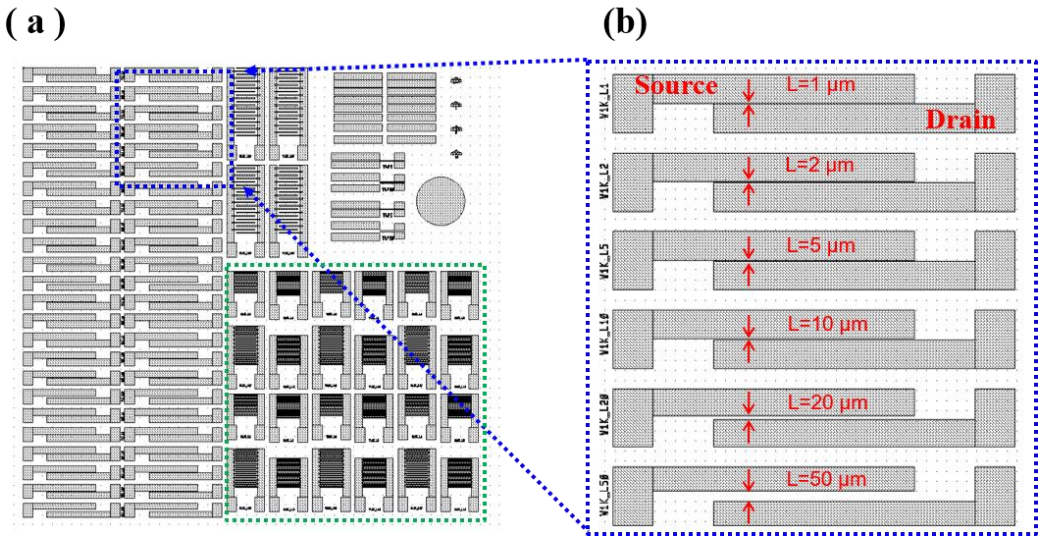

Figure 2.2 (a) Pattern design for the transistors in layout; (b) the image of zoom part of the single transistor design with different gap length.

The geometry of the transistors with different dimensions have been designed by layout software prior to fabrication steps. The pattern designed in layout for the devices is depicted in figure 2.2 (a), there are totally 48 single transistors and a part of integrated transistors. Figure 2

(b) shows the zoom image of the single transistor part designed with different gap length from 1 μm to 50 μm. It is able to calculate the statistics of the transistor parameters, which is further supported the research results of our devices.

Step 2: Cleaning substrates

N-type negative Si (doped by Ph, 380~400μmthick, resistivity of 0.0001-0.0003 Ω·cm) with 200 nm thick dielectric layer of SiO_2 were used as the substrates for all the samples. The substrates were cleaned by sonication in sequential baths of acetone, and isopropanol for 10 min each, dried by blowing N_2 gas (99.9 % purity) at room temperature, then followed with radiation in ultra-violet zone for 25 min.

Step 3: Deposition of resist

Resists are generally a kinds of organic materials with properties tailored for specific applications. In lithography technology, resists are divided in two different types, i.e. negative resist and positive resist. For the negative resist, after development process, the exposed structure is higher than the surrounding due to cross linking of polymer chains; for the positive resist, the exposed structure is deeper than the surrounding due to chopping of polymer chains after development. Normally, resist layers are deposited on the substrate surface by spin-coating method. The type of the resist and the resist layer thickness is crucial for designing the parameters of exposure.

In this work, under the optimization of electrodes fabrication in our previous research, the Copo EL 13% and Poly ethyl-methacrylate (PMMA) 3% 495 K positive resists are used, and the main parameters for the resist deposition process is shown in table 2-1.

Table 2-1 The parameters for deposition resists and the measuring resist layer thickness

Resist	Speed (rpm/min)	Acceleration	Time(s)	Curing	Thickness
Copo EL 13%	3500	1000	12	180 10 min	510 nm
PMMA 3% 495K	3000	1000	8	180 10 min	85nm

Step 4: E-beam exposure

The E-beam exposure step was carried out following the pattern design mask, seen in figure 2.2. Lithography tool VISTEC EBPG5000Plus is used during the process, with a fixed

given power 100 keV and current 50 nA to electrons, the written spot is 10 nm and the term of dose reflects the number of electrons received per unit area is expressed as 380 μC/cm^2.

Step 5: Development

For the process of development after E-beam exposure, the samples were immersed in a mixture of Methyl Isobutyl Ketone (MIBK) and IsoPropylic Alcool (IPA) with a ratio 1:2 for 60 s, subsequently immersed in IPA solution for 60 s to remove the resist exposed by the electrons, finally dried by blowing N_2 gas (99.9 % purity) at room temperature.

Step 6: Metallization

The samples treated after development process were transferred into the metal evaporation instrument. Gold were selected as the source and drain electrodes because of the excellent conductivity and the approximate work function of gold and pentacene semiconductor. A 5 nm thick Titanium was deposited as an adhesion layer. And then 50 nm thick gold were evaporated on the top of the samples.

Step 7: Liff-off

The samples were immersed in the solution of acetone for 8 hours to take off the resist, and the expected device patterns with gold were deposited on the substrates. The optical images of the devices obtained are shown in figure 2.3

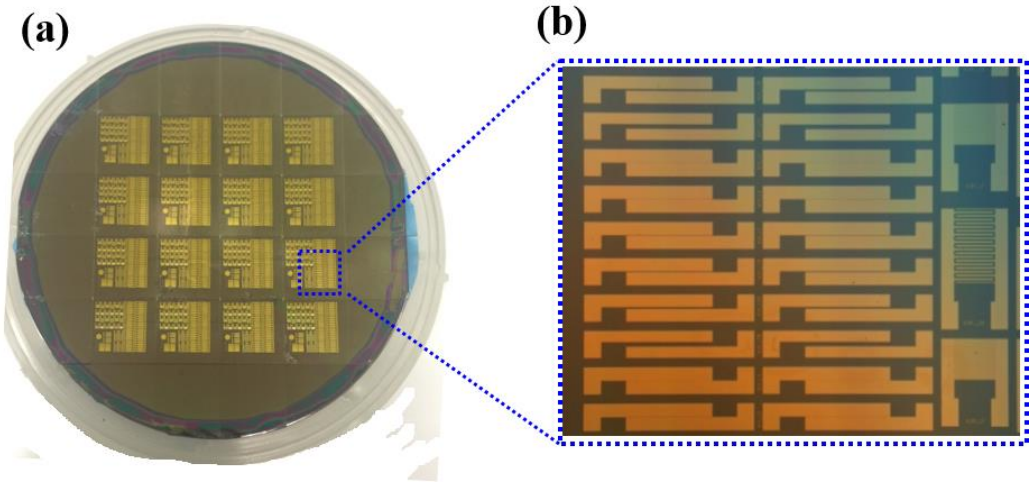

Figure 2.3 (a) The optical images of the fabricated device, (b) the image of zoom part of the single transistor design with different gap length and integrated transistors.

2.2.2 Self-assembled monolayer (SAM) modification

The SAM method deals with the monolayers of organic molecules grafted on solid substrates by chemical reactions in solution. To improve the performances of silicon-based OFETs, OTS SAM treatment on the surface of Si or SiO_2 dielectric and PFBT thiol treatment on gold are widely used and the preparation process has been extensively reported in many years [15-18]. During the preparation process, the sample is immersed in the solution of OTS or PFBT mixed with solvent for some time. It enables bear the functional moiety at the ends i. e. silane (thiol) group chemically reacted to the oxidized (gold) surfaces. However, the ways of deposition such as the properties of the solvent, the sample immersing time, the atmosphere, the exposure time of the sample after SAM treatment could be have some influences on the quality of the monolayers, which further induces to the get different properties of the OFETs [18, 19]. Thus, it signifies to concern the effects of preparation conditions during the SAM fabrication process. Following the previous results from the reverences, the mainly processes for fabricating OTS monolayer in this work is depicted in figure 2.4.

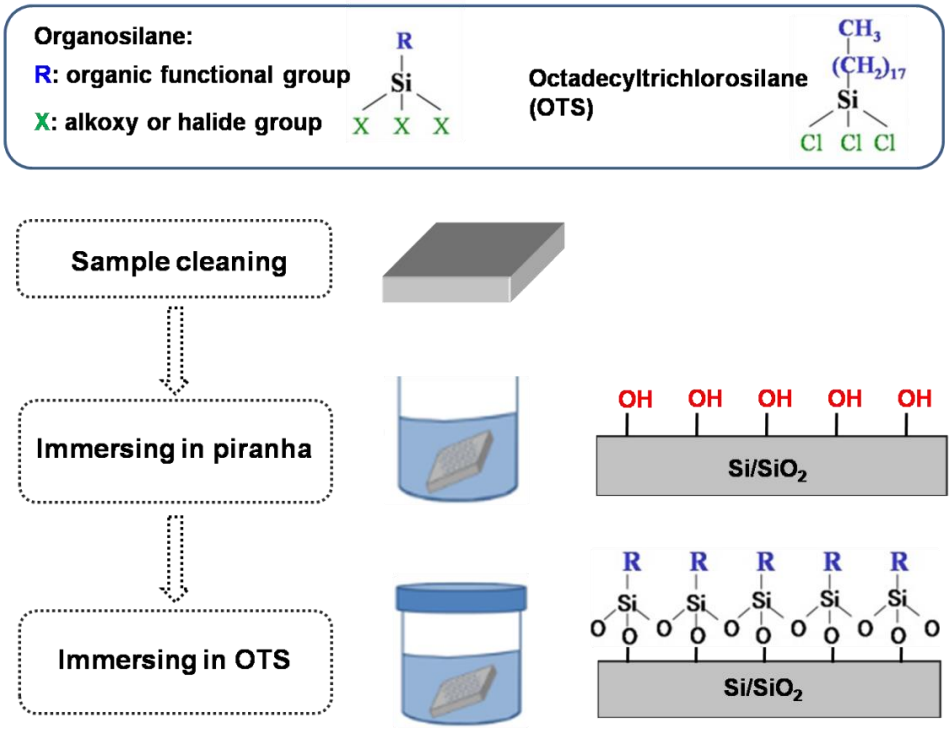

Figure 2.4 The schematic diagram of experimental process for OTS SAM deposition.

First, the sample was cleaned as the same cleaning step described in the part of 1.2.1. Then, the sample was immersed in the piranha solution (mixture of acid sulfuric H_2SO_4 96%

and hydrogen peroxide H_2O_2 with a ratio 1:2) for 15 min to form the hydrophilic surface with functionalized group Si-OH. Finally, the sample was dipped in the solutions of OTS (3-octadecyltrichlorosilane ≥90% with density of 0.984 g/mL at 25 °C, bought from SIGMA-ALDRICH company) mixed in the solvent (Hexane 70% + chloroform $CHCl_3$ 30%) with a ratio 1:10 for 2 hours, the chemical reaction process was done in a N_2 glove box to avoid the influences of water and oxygen. After the dipping process, the sample was cleaned by sonication in sequential baths of dichloromethane CH_2Cl_2 and IPA for 3 min each to remove the molecules.

To prepare PFBT SAM on gold surface, the clean sample was immersed in the solution of PFBT (2,3,4,5,6-Pentafluorothiophenol 97% with density of 1.501 g/mL at 25 °C, bought from SIGMA-ALDEICH company) mixed in the solvent of ethanol with a ration of 1:10 for 20 hours (the immersing time should be more than 18 hours to make sure obtain the PFBT SAM). After the immersing process, the sample was cleaned by sonication in bath of ethanol for 3 min each to remove the molecules. The schematic diagram of experimental process for PFBT is shown in figure 2.5.

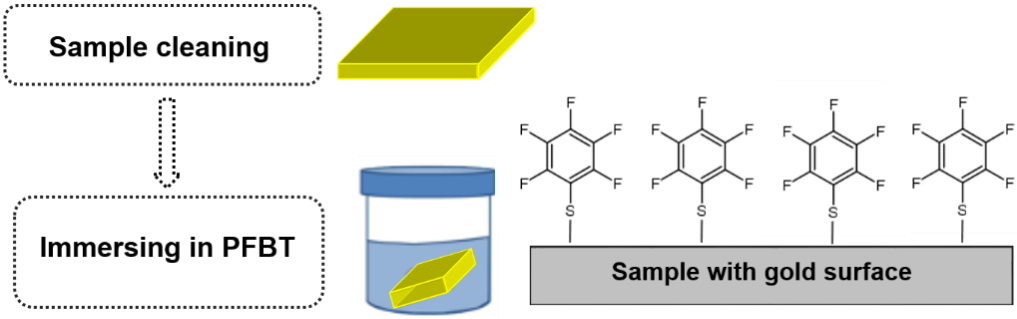

Figure 2.5 The schematic diagram of experimental process for PFBT deposition.

2.2.3 Thermal evaporation

Thermal evaporation is one of the simplest Physical Vapor Deposition (PVD) techniques to prepare semiconductors or metals. Normally, the deposition process is following two steps:

Step 1. Organic/metal materials are heated in a vacuum chamber until there's surface atoms have obtain sufficient energy to release from the surfaces.

Step 2. The atoms released from the origin materials traverse the vacuum chamber and coat a substrate positioned above the evaporating material.

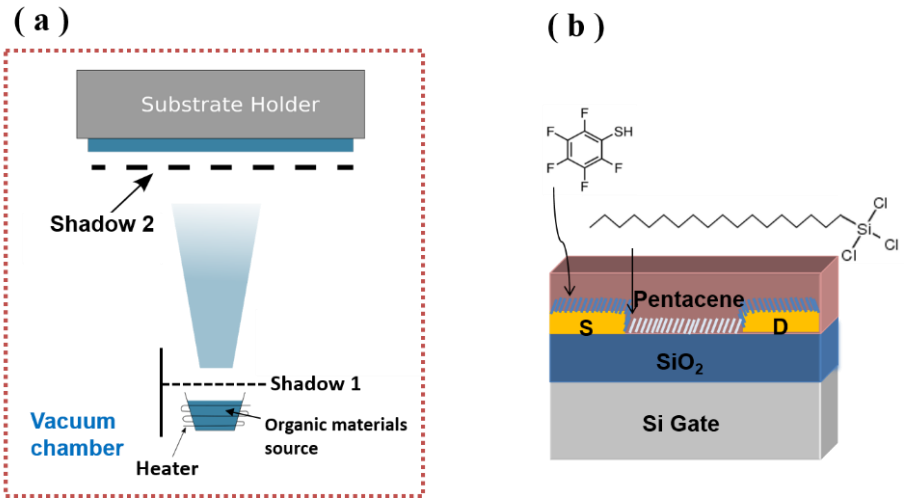

Figure 2.6 (a) The schematic of the thermal deposition chamber structure, (b) the configuration of pentacene FET device treated with OTS and PFBT SAMs

The morphology of pentacene thin films has been widely studied in order to understand its effect on transistor performance. Device performance is believed to decrease once the film becomes greater than a critical thickness. Nucleation of the films is also an important aspect, as grain boundaries can be unfavorable to device performance [20]. During deposition of pentacene, the conditions such as deposition rate, temperature, substrate type, and cleanliness have a strong impact on growth morphology [21]. Based on these considerations, in this work, 30~50 nm thick pentacene was deposited with a deposition rate of 0.1~0.2 Å /s under 2 × 10-6 Torr at source heating temperature of 125 °C. The pentacene material (purity ≥99.9 %) used I this work is bought from SIGMA-ALDRICH Company. The schematic of the thermal deposition chamber structure is shown in figure 2.6(a). Figure 2.6(b) shows the configuration of pentacene OFETs device treated with OTS and PFBT SAMs.

2.3 Instrumentations

In our experiments, the contact angle measurement, ellipsometry, profilometry, atomic force microscopy (AFM), scanning electron microscopy (SEM), x-ray photoelectron spectroscopy (XPS) and UV-photoelectron spectroscopy (UPS) characterization techniques were used to perform the sample's structural properties. The electrical properties were

characterized by Agilent 4156 C Semiconductor Measurement Unit SMU combined with N_2glove box.

2.3.1 Contact angle measurements

The contact angle is used to quantify the wettability of a solid material surface. The unique value of the contact angle could be obtained by a given system of solid, liquid, and vapor at a certain temperature and pressure. The schematic diagram is depicted in figure 2.7. The contact angle is conventionally measured through the liquid-vapor interfaces meets the solid surface, which could be used to reflect the relative strength of solid (S), liquid (L) and gas or vapor (G) molecular interaction, and in further, to perform the surface energy of the solid material. The contact angle is firstly determined by a liquid via the Young equation [22], as depicted in equation (2-1).

$$\gamma_{SG} - \gamma_{SL} - \gamma_{LG}\cos\theta = 0 \tag{2-1}$$

where γ_{SG}, γ_{SL}, and γ_{LG} represent the liquid-vapor, solid-vapor, and solid-liquid interfacial tensions, respectively, and θ is the contact angle.

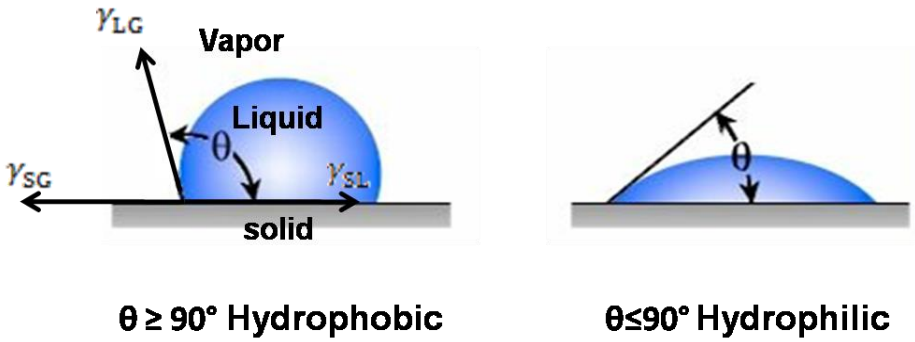

Figure 2.7 The schematic of contact angle with a liquid drop on the solid surface.

Generally, small contact angles (≤90°) correspond to high wettability, means the surface of the solid is hydrophilic, while large contact angles (≥90°) correspond to low wettability, means the surface of the solid is hydrophobic. Normally, the contact angle measuring methods can be classified into two ways: the direct optical method and the indirect force method. The direct optical method is used in our experiments. The ionized water is used to drop on the sample, and the drop contact angle is measured by a high resolution cameras and software to capture and analyze the contact angle result.

2.3.2 Atomic force microscopy

Atomic force microscopy (AFM) is used to analyze the surface morphology of pentacene thin films in this work. AFM method is performed by monitoring the attractive and repulsive forces of atoms between the probe and the surface of sample, which could further image the surface of the materials in three-dimensional detail down to the nanometer scale [23]. Figure 2.8 shows the simple schematic of AFM setup. When doing the measurements, the sample could be moved in the 3D (x, y and z) directions by using a single piezotube, and the probe attached to cantilever could move up and down to response the certain force between the probe and sample. As a consequence, the movement of the cantilever is detected by a photodetector through using a lased spot reflected from the top surface of the cantilever.

In general, the AFM is divided into two imaging mode, i.e. contact mode and non-contact mode. However, both of the two modes have disadvantages, the contact mode could obtain distort image data and damage the sample. And the non-contact mode can be hampered by the contamination. To be sure not damage the sample and also achieve high resolution surface images, the non-contact mode was used for our experiments.

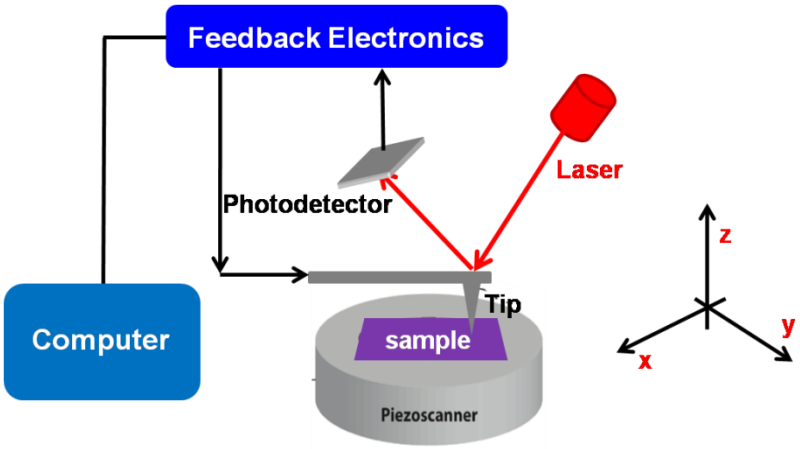

Figure 2.8 The schematic of the AFM setup.

2.3.3 Scanning electron microscopy

Scanning electron microscope (SEM) is a common technique that applied to perform a surface topography image and material composition of a sample by scanning the sample's surface with a focused beam of electrons. The electrons ejected from the electron gun could impact with the atoms in the sample, then producing various signals like x-ray, auger electrons, and secondary electrons and so on that contain information of the sample. The most common

SEM mode is through collecting the secondary electrons by using a special detector and creates the topography image of the sample. It can achieve resolution better than 1 nanometer. The mechanism of the SEM is shown in figure 2.9 and the type of ultra-55 SEM is used in our experiments.

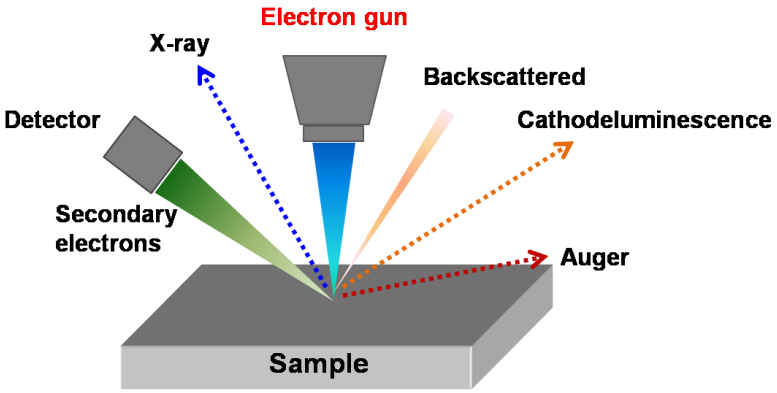

Figure 2.9 The mechanism of the SEM setup.

2.3.4 XPS and UPS

X-ray Photoelectron Spectroscopy (XPS) and UV Photoelectron Spectroscopy (UPS) are techniques to display the elemental, molecular, energetic information of materials. For the physic mechanism of XPS and UPS, XPS uses high energy x-ray photons to excite "core" electrons in the near-surface region, gives the elemental composition of the sample, while UPS uses lower energy photons in the deep UV region to excite valence electrons, further provides estimates for "density of stares", frontier orbital energies (HOMO), and work function. Figure 2.10 shows the different physic mechanisms of XPS and UPS.

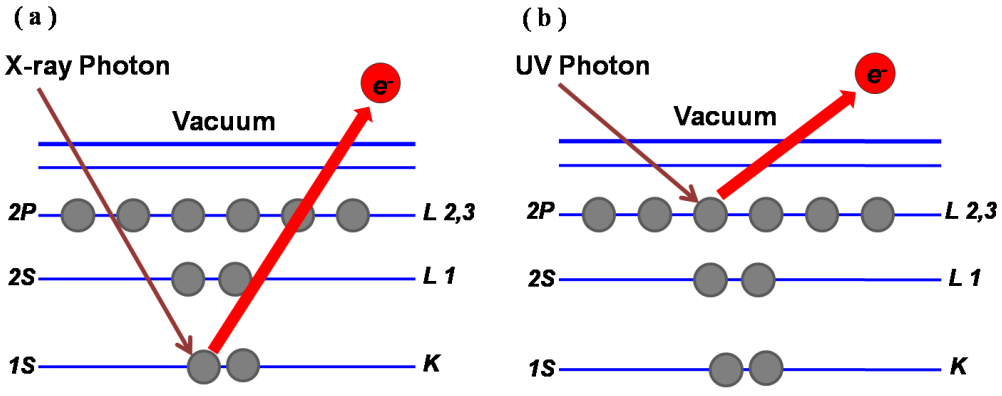

Figure 2.10 The physic mechanisms of (a) XPS and (b) UPS techniques.

2.3.5 Electrical characteristic system

In this work, all the electrical characteristics of the samples were performed by the instrument of Agilent 4156 C Semiconductor Measurement Unit SMU in a glove box under vacuum with the controlled atmosphere (H_2O, O_2 < 0.1 ppm, pressure ~ 5-6 mbar), the schematic of the measurement system is shown in figure 2.11.The Agilent 4156C instrument could apply the extra voltage as big as ±100 V, the limit current is 200 mA. During the measurements, the station and the contact probes could be controlled to change the direction in 3D dimension, and an optical microscopy is used to observe the sample and probes. When the sample is connected with the instrument, LabVIEW and easy expert software is used to measure the electrical properties.

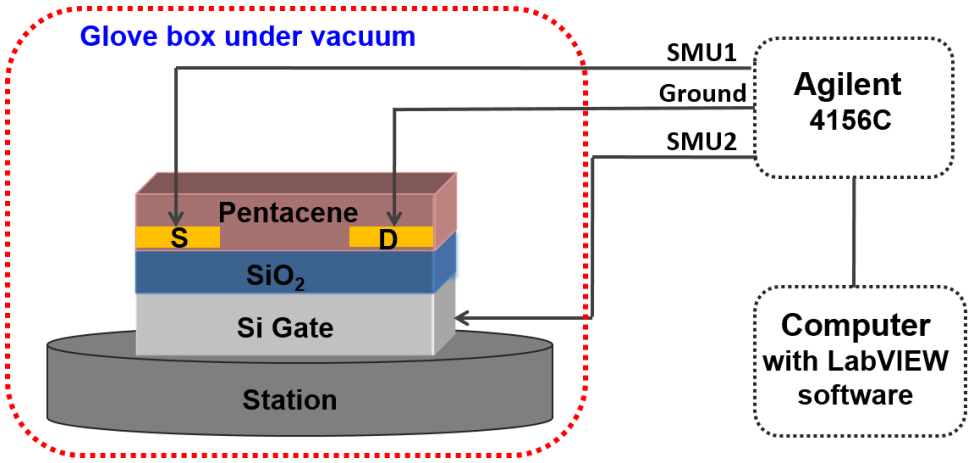

Figure 2.11 The schematic diagram of the electrical characteristic system used in this thesis.

2.4 Characterization

2.4.1 Physical properties

• *Contact angle*

To compare the bare substrate and SAM-modified gate dielectric layer or gold layer in terms of the surface energy, the static contact angles were measured. As shown in figure 2.12, the optical images of contact angles measured on bare SiO_2, SiO_2 treated with OH group, bare gold, gold functionalized PFBT, SiO_2 functionalized OTS, as well as the transistor device with cumulative OTS and PFBT modified surfaces. As a result, we found the clean, bare SiO_2

typically had contact angles between 28° and 35°. The SiO_2 treated with OH group also had contact angles between 25° and 30°. Almost no differences with bare SiO_2. However, the OTS-treated SiO_2 we typically measured contact angles between 90° and 108°, depending on the exact conditions of the OTS treatment. Indicating that the surface energy of OTS-treated SiO_2 is quite lower than the bare SiO_2, which is beneficial to deposit high quality of pentacene thin films [24].

At the same time, the contact angles of clean, bare gold were measured between 65° and 72°. For the PFBT-treated gold sample, we typically measured contact angles were between 80° and 85° (seen in figure 2.12(c) and (d)). The PFBT modified gold surface could change the work function of gold, consequently, decrease the contact resistance during the electric measurements [13]. In order to see the effect of cumulative OTS and PFBT modified device surfaces on the performances, the contact angle was also calculated and found the values between 95° and 110°.

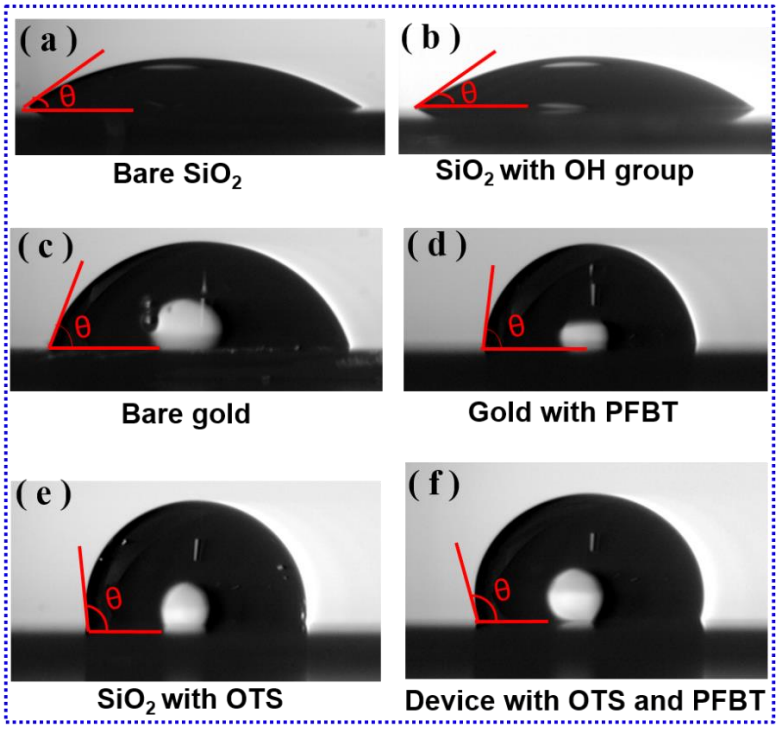

Figure 2.12 Contact angle of (a) clean, bare SiO_2 surface, (b) SiO_2 surface treated with OH group, (c)clean, bare gold surface, (d) PFBT-treated on gold, (e) SiO_2 surface treated with OTS, (f) transistor device with cumulative OTS and PFBT modified surfaces.

The thickness of the SAM were also measured by ellipsometry to further identify the property and the succeed deposition of OTS and PFBT monolayers. The results showed the thickness of OTS on SiO_2 is 15Å to 20 Å and the thickness of PFBT on gold is 8 Å to 9 Å.

Indicating that the OTS and PFBT monolayers were successfully deposited on the surface of samples and without any cluster of molecules.

• *AFM*

As the solid surfaces with and without SAM treatment have efficient influence on the physical structure of the top organic semiconductors, the surface morphologies in 2D and 3D dimensions of the pentacene thin films deposited on bare gold, bare SiO_2, gold functionalized with PFBT, as well as SiO_2 functionalized with OTS were demonstrated and compared by AFM measurements, the images are depicted in figure 2.13. During the measurements, the rout of tips scanned the pentacene semiconductor on the transistor devices is from gold electrode area to channel area.

As can be seen in figure 2.13 (a) and (b), the pentacene deposited on bare gold electrode and bare SiO_2 shows a preferable bulk phase with a root mean square roughness (RMS) 10.5 nm on gold electrode area and 13.2 nm on SiO_2 dielectric, respectively. However, after the SAM modification on the surfaces, seen in figure 2.13 (c) and (d), the pentacene shows a thin film phase with RMS decreased to 7.2 nm on PFBT modified gold electrodes areas and 9.5 nm on OTS modified SiO_2, respectively. Thus, the pentacene deposited on the SAM treated surfaces is more smooth. The 50 nm thick pentacene thin films were measured by profilometry method. Research from Bouchoms et al [25] has verified that the pentacene could present a thin film phase and a bulk phase (triclinic in nature), and the performance of the pentacene based transistor device is believed to decrease once the pentacene film enters the bulk phase [26].

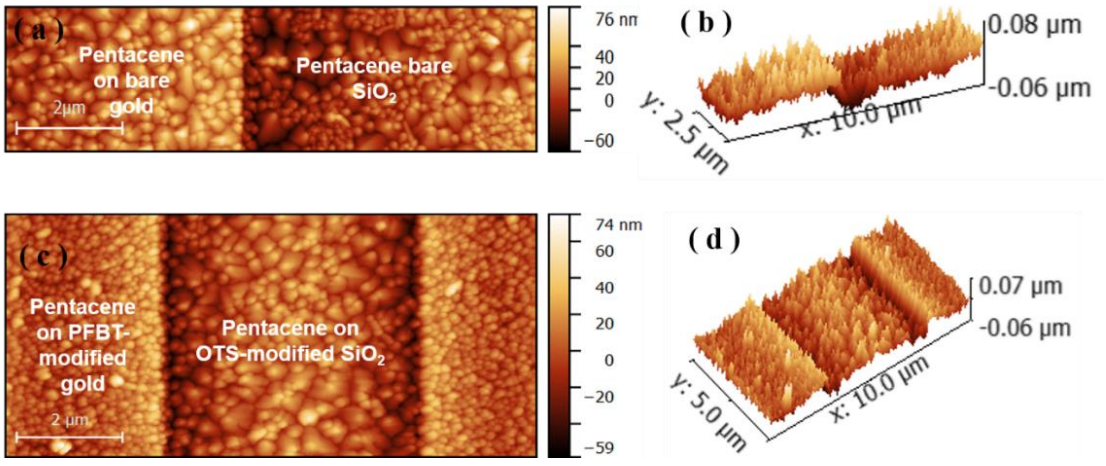

Figure 2.13 AFM of the pentacene on (a) bare gold and bare SiO_2 surfaces in 2D dimension, (b) bare gold and bare SiO_2 surfaces in 3D dimension, (c) OTS and PFBT SAMs modified surfaces in 2D dimension, (d) OTS and PFBT SAMs modified surfaces in 3D dimension.

2.4.2 Electrical properties

• *Transfer characteristics*

All the samples fabricated in our experiments were successfully work as a transistor device, and the electrical properties has been measured under the same circumstance conditions. To compare the characteristics of the sample treated with different type of SAM, the results of the sample with exactly same structures (same channel width and length) were performed. Here, the drain current-gate voltage (I_{DS} - V_{GS}) transfer curves of different SAM modified OFET and the reference OFET (bare SiO_2) channel width 2μm and channel length 1000 μm (W/L=500) are depicted in figure 2.14, where logI_{DS} and $I_{DS}^{1/2}$ is plotted versus V_{GS} at a fixed V_{DS} value of -40 V for all the samples, V_{GS} ranges from +40 V to -40 V. The mobility values of the transistors were calculated in saturation by using equation (1-4) based on Ihantola and Moll's [27] theory about isolated gate field effect transistor.

As expected from the conventional OFET operation, the current flow through the OFETs is strongly influenced by the gate voltage V_{GS}. All of the transfer characteristics of the OFETs prepared here display a subthreshold regime between the switch on voltage and the threshold voltage. From the electrical transfer characteristics, the parameters of carrier mobility, threshold voltage, and subthreshold swing and on/off current ratio were extracted. The electrical performances were electrically characterized and determined in the saturation regime, the electrical parameters of the different samples of OFET were summarized in Table 2-2 (every parameter was extracted by the average of 10 devices).

Table 2-2. Summary of the electrical parameters for different pentacene OFETs

Gate dielectric material	Carrier mobility ($cm^2V^{-1}s^{-1}$)	Threshold Voltage (V)	Subthreshold swing (V/decade)	On/off current ratio
SiO_2	0.03	-10	1.1	$>10^4$
SiO_2+OTS	0.048	-17	1.4	$>10^5$
SiO_2+PFBT	0.301	-12.5	1.6	$>10^6$
SiO_2+OTS+PFBT	0.363	-6	0.9	$>10^6$

For the device fabricated with bare SiO_2 dielectric layer and bare gold electrodes, the carrier mobility is only 0.03 $cm^2V^{-1}s^{-1}$ and the current on/off ratio is 10^4orders of magnitudes.

When the SiO_2 is treated with OTS monolayer, the carrier mobility increases to 0.048 $cm^2V^{-1}s^{-1}$and current on/off ratio is 10^5orders of magnitudes, the optimized performance is consistent with previous researches [13-15]. However, for the device fabricated with the PFBT monolayer modification on the gold electrodes, the carrier mobility sharply increases to 0.301 $cm^2V^{-1}s^{-1}$, which is ten times bigger than the bare $SiO_2$and bare gold sample. And the current on/off ratio is also increased up to 10^6orders of magnitudes. Intriguingly and significantly, the performances of pentacene FET with the hybrid contacts by modification of both OTS and PFBT SAM were enhanced, carrier mobility reached to 0.363 $cm^2V^{-1}s^{-1}$. Finally, a higher mobility up to 0.68 $cm^2V^{-1}s^{-1}$ was obtained of the device with channel length 2 μm and channel width 1000 μm (W/L=500).

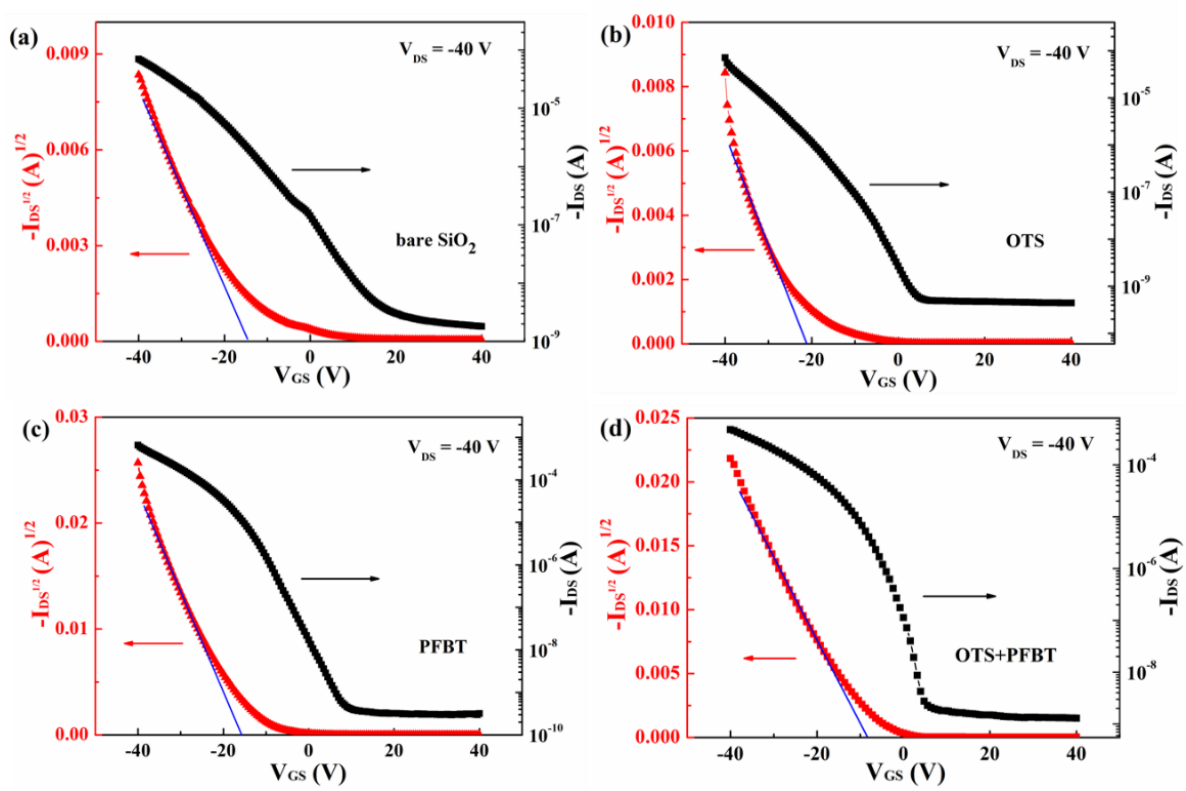

Figure 2.14 The drain current-gate voltage (I_{DS} - V_{GS}) transfer curves of different SAMs modified OFETs and the reference OFETs (bare SiO_2) with channel length 2μm and channel width 1000 μm.

• *Output characteristics*

The output characteristics of the four different samples are also displayed and compared, seen in figure 2.15. All the samples show the pronounced saturation behavior with the measurement parameters V_{GS} =40 V, V_{DS}=40 V. When comparing the low drain voltage part (with red dotted line circle) of the four figures, the transistor devices fabricated with bare SiO_2

is nonlinear property, whereas the devices treated with PFBT has linear property. It further verify the PFBT SAM functionalization lower the contact resistance.

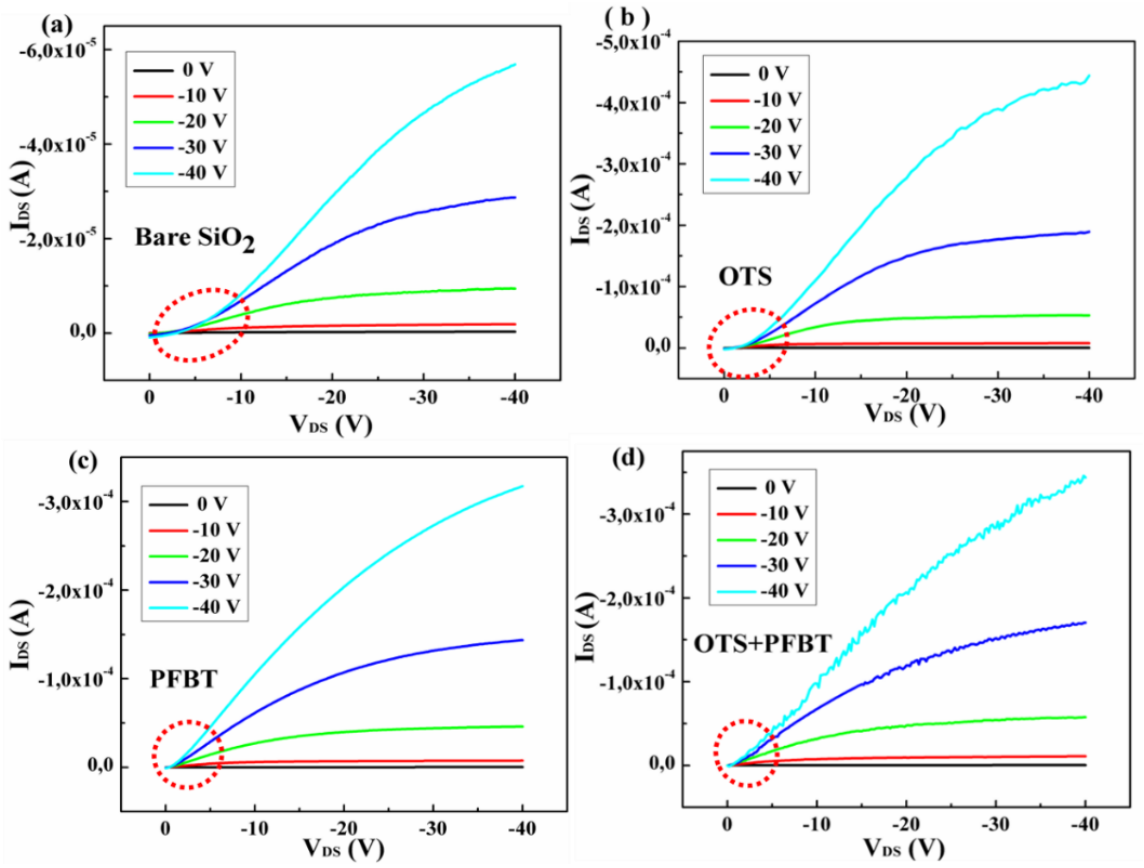

Figure 2.15 The drain current-drain voltage (I_{DS} - V_{GS}) output curves of different SAMs modified OFETs and the reference OFETs (bare SiO_2) with channel length 2μm and channel width 1000 μm.

• *Contact resistance*

The contact resistance as opposed to an intrinsic value in a transistor system refers to the contribution on the total resistance of the channel length and the electrodes connections. The total resistance R_{tot} can be calculated following the equation (2-2) [28].

$$R_{tot} = R_c + R_{ch} = R_c + \frac{L}{WC_i\mu(V_{GS} - V_{DS})} \quad (2\text{-}2)$$

Where R_C is the contact resistance of probes and electrodes, R_{ch} is the resistance of channel length, W/L=channel length/channel width, $\mu$is charge carrier mobility, C_i is insulator capacitance per unit area, V_{GS} and V_{DS} is gate-source voltage and drain-source voltage, respectively.

According to the equation, we can see that the contact resistance could be provided by the linear extrapolation of the total resistance to the zero channel length. Therefore, we used the most common method of transmission model to measure the contact resistances of our samples. The results is shown in figure 2.16. Here, the total device resistance is plotted as a function of the channel length. The resistance of the transistor is decreased with OTS and PFBT modification.

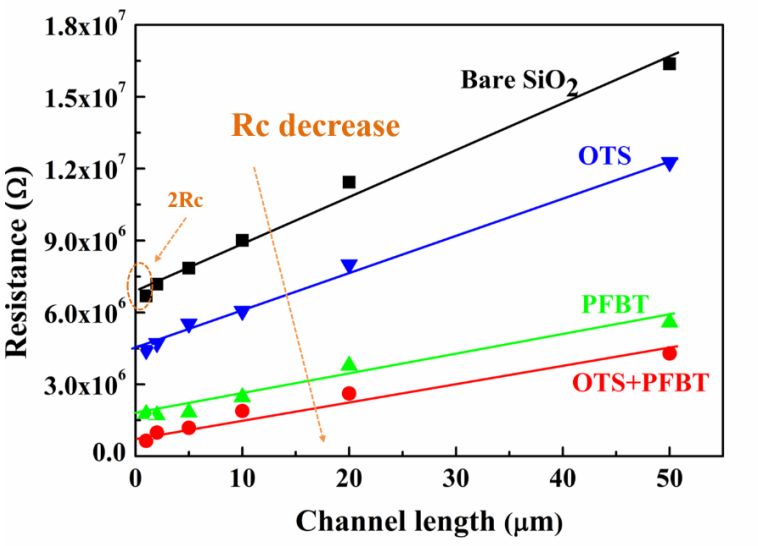

Figure 2.16 The total device resistance is plotted as a function of the channel length.

• *The dependence of the mobility and on/off ratio on the channel length*

The performances of OFETs are strongly correlated the charge carriers injection and the transport in the channel [29, 30]. To better understanding the occurrence charge transport in different SAMs modified pentacene FETs, the mobility and on/off ratio depend on the channel length were described and compared, shown in figure 2.17.

As can be seen in figure 2.17(a), the mobility of OTS modified device is increased with the increase of channel length, here it is proposed that the main occurrence of the charge transport is on the OTS monolayer in the channel. The smaller mobility with the shorter channel could be explained by the existence of significant contact resistance, which further induces to less charge carrier injection. The result tendency is associated with Ref [31]. In contrast, the device with the PFBT modified electrodes and with both OTS and PFBT modification show that the mobility is decreased with the increase of channel length, and the mobility is much higher than the device modified by OTS. The same result was also investigated by Chong-an

Di et al [32]. In this case, the SAM enhance the work function of electrodes is extensively approved during the research [15, 16, 33]. Thus improves the charge injection from the bias and tunes the occurrence of charge transport from the PFBT monolayer to Pentacene or to OTS monolayer. For the current on/off ratio, there is no obvious dependence on the channel length, the current on/off ratio of the devices with the PFBT modified electrodes and with both OTS and PFBT modification is like Gauss distribution, which needs further investigation.

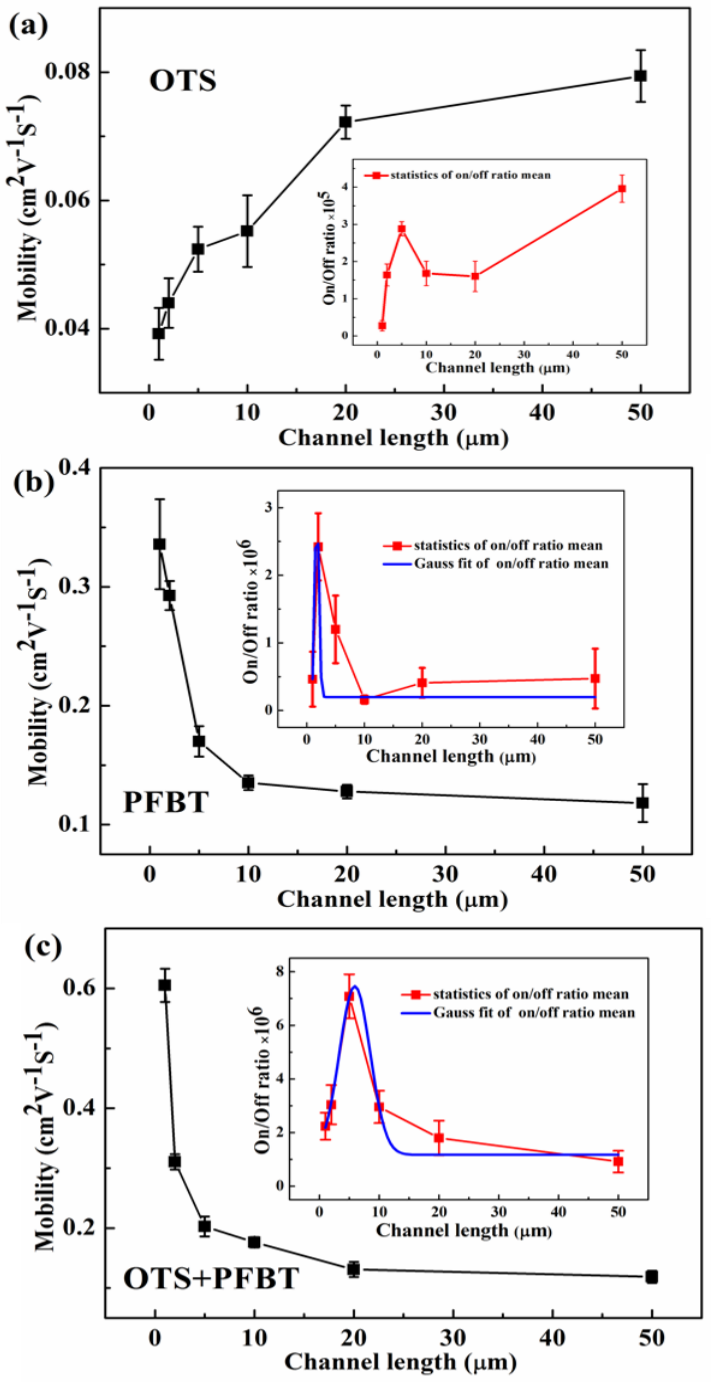

Figure 2.17 The dependence of the mobility and on/off ratio on the channel length with different SAMs modification. (a) OTS-modified, (b) PFBT-modified, (c) OTS and PFBT-modification.

2.4.3 Analysis of physical mechanisms

• *The XPS analysis*

To learn more about the physical mechanisms of the charge transport in these different samples, XPS analysis was used to further directly observe the pentacene interaction with PFBT and OTS monolayers [13]. The XPS general spectra of pentacene deposited on OTS, bare OTS, and pentacene deposited on PFBT, as well as bare PFBT are shown in figure 2.18.From the general spectra, we can see that the OTS and PFBT SAM were successfully grafted and the pentacene thin films was well deposited on the SAM monolayers.

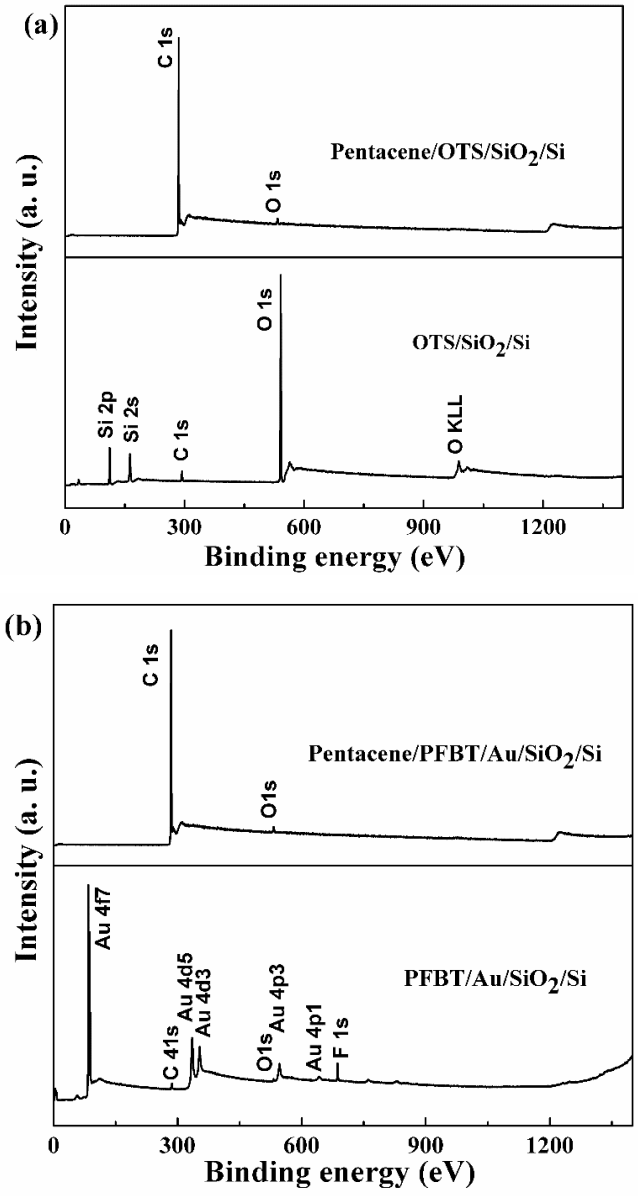

Figure 2.18 The respective general spectra of PFBT, OTS and pentacene on the SAMs. (a) Pentacene on OTS and OTS, (b) Pentacene on PFBT and PFBT.

To analyze the XPS in detail, the respective C1*s* spectra of PFBT, OTS and pentacene on the SAM are displayed in figure 2.19. The C 1*s* peak of OTS in figure 2.19(a) shows the mainly composed C-C bond at 284.7 eV with the atomic area percentage of 96%.However, a small peak at 286.9 eV indicates possibly the oxidation of OTS. The C1*s* peak of pentacene deposited on OTS depicts symmetric shape without shift, implies those of thin-film-phase pentacene formed on a nondipolar interface, where there is negligible electronic interaction between pentacene and the OTS surface. In figure 2.19(b), The C 1*s* peak of PFBT/Au shows the C-C bond and C-F bond at 284.8 eV and 286.7 eV, respectively, indicates the PFBT is well chemisorb on the Au. And the C1*s* peak of pentacene/PFBT/Au shows symmetric shape with a peak centered at 284.4 eV, resembles a thin-film-phase pentacene [13]. It is associated with the AFM measurements. The shift of the C-C peak with 0.4 eV implies the electronic interaction between pentacene and the PFBT thiol surface due to the molecule dipoles with different directions and moments within the PFBT thiol. It means the downward band binding in pentacene along from the interface to the thin film surface [34].

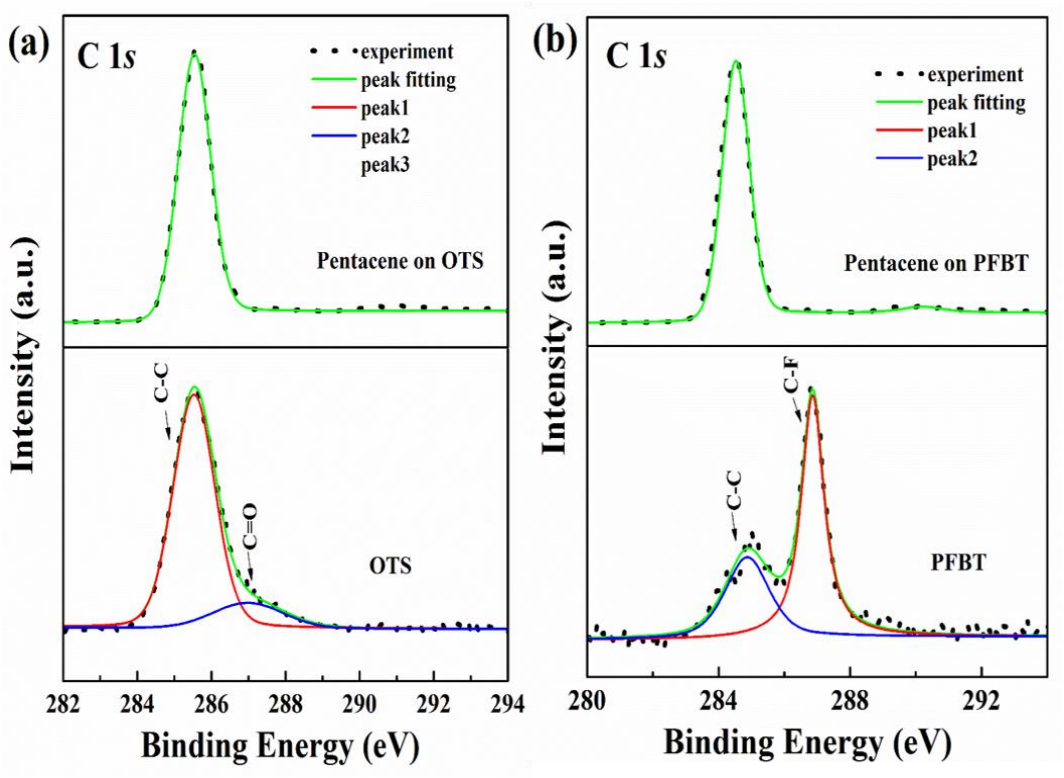

Figure 2.19 The respective C1*s* spectra of PFBT, OTS and pentacene on the SAMs. (a) Pentacene on OTS and OTS, (b) Pentacene on PFBT and PFBT.

In all the samples, the O1s peaks were clear detected, which implies that oxygen was contained. As the oxygen could be the electrons contributions for electrical properties, therefore, the spectra in figure 2.20 compares the O 1*s* peaks of bare OTS, bare PFBT, and pentacene on the SAM.

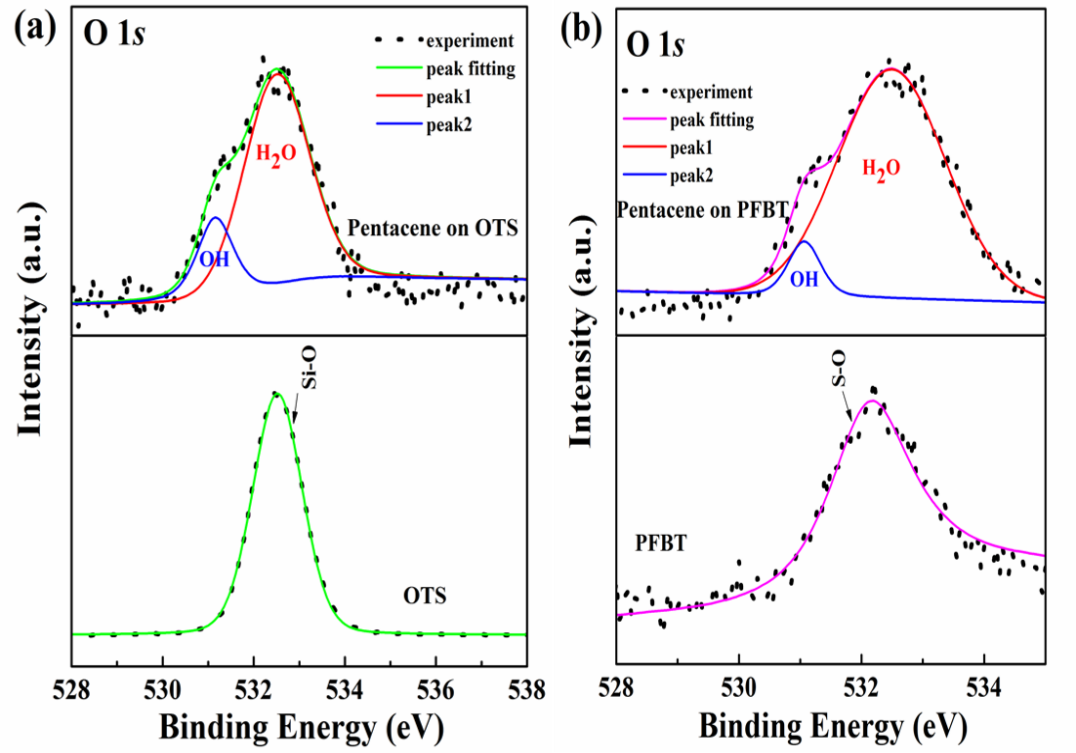

Figure 2.20 The respective O1*s* spectra of PFBT, OTS and pentacene on the SAMs. (a) Pentacene on OTS and OTS, (b) Pentacene on PFBT and PFBT.

The O 1*s* peak at 532.4 eV of OTS in figure2.20 (a) shows strong intensity could be the Si-O bond [35, 36].Whereas without C-O bond observed as in figure 2.20 (a) maybe because of the relatively low intensity inducing the overlapping of the peak. The O 1*s* peak of Pentacene/OTS shows two kinds of oxygen components, could be distinguished as the oxygen in H_2O at 532.3 eV and OH at 531.2 eV moieties [37]. Under experimental conditions in ambient air, H_2O and O_2 are very likely to be present on the surface of the amine-terminated film. Thus, the reactions occur at the film–air interface and influence the intrinsic electrons in the film. From figure 2.20(b), the O1s peak at 532.1 eV with relatively low intensity corresponding to the oxidized sulfur [38]. And Pentacene/PFBT also shows oxygen components in H_2O at 532.5 eV and OH at 531.1 eV. The binding energy shift also indicates the difference in the electronic character of pentacene on OTS and PFBT. As the effect of O_2 on the OFET performance is very small, whereas the chemically absorbed water interacts with

pentacene to form pentacene/$(H_2O)n$ clusters, which can enhance saturate current [38]. Comparing the pentacene deposited on the two kinds of SAMs, the density of the oxygen component of H_2O (O_{H2O}/O_{Total}) is 92.4% in pentacene deposited on PFBT but only 78.9% in pentacene deposited on OTS. Those differences should play an important role on the transport properties of thin films.

• *The UPS analysis*

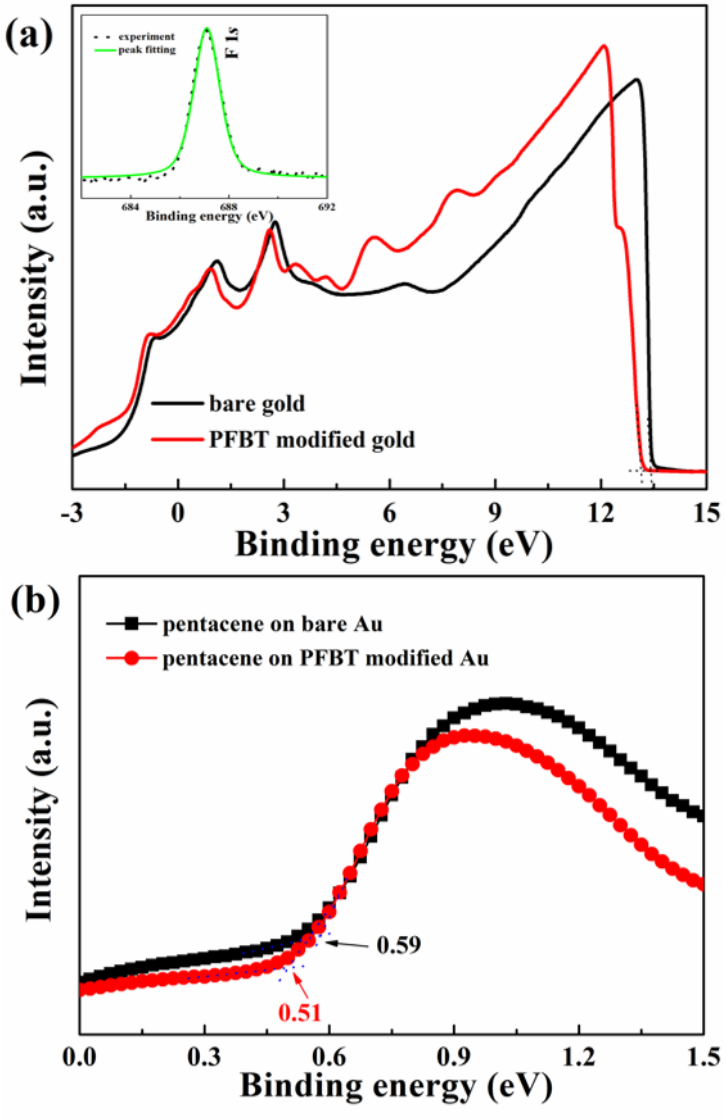

Figure 2.21 (a) UPS He I (21.2 eV) spectra under 3 eV of bare Au and PFBT-modified Au, (b) Focused UPS spectra near HOMO level of pentacene on bared Au and PFBT-modified Au.

As the device fabricated with PFBT SAM obtained excellent performance, we used UPS analysis to get better understanding the charge transport at pentacene/PEBT-modified electrodes interfaces. The UPS results of bare Au the PFBT modified Au are displayed in figure

2.21. The inset of figure 2.21(a) shows the high resolution of XPS spectrum of PFBT modified Au with a clear peak at 687.5 eV associated with F 1s, a clear signature of PFBT molecules [15]. From the UPS spectra, the work function values of bare Au and PFBT modified Au are 4.75 eV and 5.25 eV, respectively. It implies the PFBT-modified Au increase the work function of bare Au, and resulting in a reduction of hole injection barrier into pentacene semiconductor, in good agreement with previous reports [16, 39-41]. The figure 2.21(b) shows the focused UPS spectra near HOMO level of pentacene on bared Au and PFBT modified Au. The different values could be related to the change of crystallinity of pentacene, and inducing the different of holes injection barrier. Therefore, it further affects the charge transport at the Au/pentacene interfaces.

• *The energy diagrams*

The above viewpoints are explained by the energy diagrams of charge transport from Au to pentacene are presented in figure 2.22(a) and figure 2.22(b), respectively.

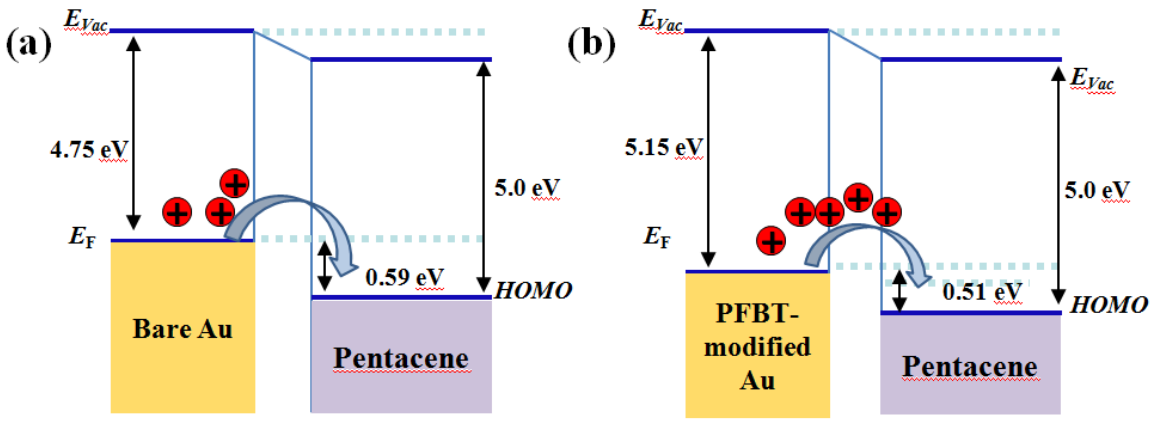

Figure 2.22 Energy diagrams of by the energy diagrams of charge transport from (a) Bare Au to pentacene, (b) PFBT-modified Au to pentacene.

The pentacene band structure in the figure is from Ref. [42]. For the pentacene deposited on bare Au, the HOMO peak is centered at 0.59 eV, indicating the holes injected from bare Au to pentacene under bias should surmount the energy barrier of 0.59 eV. On the contrary, when the pentacene deposited on PFBT modified Au, the spectrum shifts and shows a HOMO peak centered at 0.51 eV, indicating energy barrier at PFBT modified Au/pentacene interface decreases to 0.11 eV. As a consequence, the decreased hole barrier for Au contact to pentacene leads to an improved contact at Au/pentacene interfaces, more holes with rapid increase are

injected into the channel and significantly improve the electrical performance [13]. Thus, the occurrence of the charge transport is different from the OTS modified pentacene transistors.

2.5 Conclusions

In conclusion, first, the mainly technique fabrication processes for realization of our transistor devices and the instrumentations used to analyze the samples have been introduced in detail in this chapter. Then, the electrical performances of different SAMs modified pentacene FET devices i.e. the FETs of pentacene that deposited on bare SiO_2, on OTS modified SiO_2 surfaces, and on PFBT modified Au electrodes surfaces, as well as both the two SAMs modified surfaces were exhibited and compared. With the SAM modification, the optimized electrical results with high mobility 0.68 $cm^2V^{-1}s^{-1}$ and high current on/off ratio $>10^6$ were obtained. In the end, the charge transport mechanisms were discussed in detail by using XPS and UPS analyses. In particular, the improving performance of the organic transistors through tuning the charge transport with hybrid SAM layers suggesting that highlighting the utility of surface modulations and controlling of charge transport of interfaces in nanoscale materials, and the results could be an efficient support our further experiments.

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Chapter 3

Preparation and characterization of NFGM

Chapter 3 Preparation and characterization of NFGM

3.1 Introduction

Memory device is an essential component in many of industrial electronic devices for data processing, storage, and communication [1]. In recent years, nonvolatile transistor organic memories have been extensively studied and expected to be used in commercial industry because of the advanced advantages, such as flexibility, low-cost fabrication, and single transistor structure [2-6]. Among the many possible device configurations of nonvolatile organic memories, tremendous efforts have been devoted to the development of NFGM towards high performance memory devices, due to its spatially discrete floating-gate elements (nanometer-sized metallic or semiconductor nanoparticles) effectively as a charge trapping site between two dielectric layers (blocking layer and tunneling layer) to store and erase the information [7]. Thus, NFGM exhibit high speed operation, superior reliability, and to be scaled down [8-10].

In the past of years, much works have been focused on developing new materials and structures to get higher performances of NFGM devices [11]. For instance, Dong-Yu Kim et al used different kinds of charge trap metallic nanoparticles to obtain larger memory window [12], the authors in Ref. [3, 13] achieved the NFGM with better retention properties by altering gold nanoparticles (Au NPs) and reduced graphene sheets (rGO) sheets as double floating-gate. Wei Huang et al improved the operation current on/off ratio by changing the properties of tunneling layer [14], very recently, Ye Zhou et al deduced the working voltage through tuning the way of storing signals [15]. Nevertheless, all the research reported in the previous is related to modify the trap levels, trap sites, structures, or semiconductors, they have in common the charges stored in the floating-gate all come from the organic semiconductors. As the connection of organic semiconductor to periphel circuitry in electronic device, it processing a non-vanishing energy gap between occupied and empty electronic states electrical and must be inevitably realized with a range of metals [16]. In this regard, it also signifies to tune the way of the charge transport between organics and metals. However, there is few reports concerning about the influence of charge transport at the interface of organic semiconductors/electrodes on the performances of

NFGMs. Hence, it is motivated and expected to explore the new approaches to the optimization of NFGMs.

In chapter 1, we have optimized the performances of pentacene based transistors by modifying the dielectric and electrode surfaces with OTS and PFBT SAM, respectively. Based on the results, in this chapter, the pentacene based single and double NFGM were fabricated and characterized. We used Au NPs and rGO sheets as floating gate to trap charges. SiO_2 and Al_2O_3 dielectrics were deposited as blocking layer and tunneling layer. The performances of single and double NFGM with and without PFBT modification electrodes were demonstrated and compared. Optimized memory performances including the large memory window of 51 V, the stable retention property more than 10^8 s, and reliable cycling endurance over 1000 cycles were obtained. And the effect of rGO sheets and the effects of SAM modification on the NFGM were discussed, which further highlights the utility of surface modulations to tune the charge storage/release behaviors in transistor memories.

3.2 Experimental

In this chapter, we totally fabricated four kinds of memory samples, including single nano-floating gate (SFG) memory by using Au NPs as floating gate, double nano-floating (DFG) memory by using lower Au NPs and upper rGO sheets as hybrid floating gate, SFG memory with PFBT monolayer, and DFG memory with PFBT monolayer.

• ***Fabrication process***

To fabricate the NFGM samples in our experiments, the process mainly includes cleaning the substrate, depositing Au NPs/rGO sheets as floating gate, evaporating Al_2O_3 tunneling layer, getting gold electrodes by e-beam lithography, and deposition PFBT SAM, as well as deposition pentacene semiconductor by thermal evaporation. Compare with the process to fabricate transistors in our experiments, the different steps for realization of NFGM are the deposition of floating gate and tunneling layer. The details to deposit Au NPs and rGO sheets, as well as tunneling layer is described below.

• *Deposition of Au NPs*

In the experiments, the Au NPs was fabricated by self-assembled method. First, the clean substrate was treated with sequential piranha solution and UV ozone to be rich in hydroxyl groups. Then, it was immersed into the solution of (3-Aminopropyl)triethoxysilane (APTS)

(≥98%, 0.946 g/mL at 25 °C, purchased from SIGMA-ALDRICH) mixed in the solvent of methanol for 1 h to form a positive charged SAM, the ratio of APTS to methanol solvent is 1:10, the excess non-reacted molecules were removed by rinsing with methanol and then in isopropanol under sonication. After the functionalization of APTS, the sample was dipped into the negative charged citrate-reduced Au NPs solution (colloidal solution purchased from Sigma Aldrich with the average diameter of the Au NPs10±3 nm,) for more than 2 hours to obtain the lower floating gate layer of Au NPs matrix, the NPs concentration in the solution and the duration time of the reaction were changed to adjust the Au NPs density. The basic strategy to deposit the Au NPs matrix on the SiO_2 surface is schematized in figure 3.1.

Figure 3.2 Schematic representation of the procedures developed for fabricating gold nanoparticles on the substrate in combination with APTS monolayer.

• *Deposition of rGO sheets.*

To prepare rGO sheets the upper floating gate layer, the sample with the layer of Au NPs matrix was first assembled another layer of APTS, then pristine graphene flakes solution (purchased from Graphene Supermarket, with concentration of 1 mg/L, dispersion in ethanol 70% + water 30%, with average flacks thickness of 0.35 nm and average particle size around 550 nm) was drop casted on the sample surface and followed by an annealing process on oven at 80 °C for 5 min, the time for repeating drop was determined the average cover percentage of rGO sheets on the sample surface. The rGO sheets that were used for a second floating gate layer could overcome the problem of obtaining a pair of charge trapping layers along the vertical direction of Au NPs double floating-gate memory devices [3]. The same preparation processes of Au NPs and rGO sheets have been reported in our previous works of Ref. [13, 17].

• *Deposition of Al_2O_3 dielectric layer*

Al_2O_3 dielectric layer with 10 nm thickness was used to be the tunneling layer in our NFGM devices. The Al_2O_3 was deposited by using atomic layer deposition method at the temperature of 300 °C. And the thickness of was verified by ellipsometry. The schematic diagram process of fabricating SFG memory and DFG memory is depicted in figure 3.2.

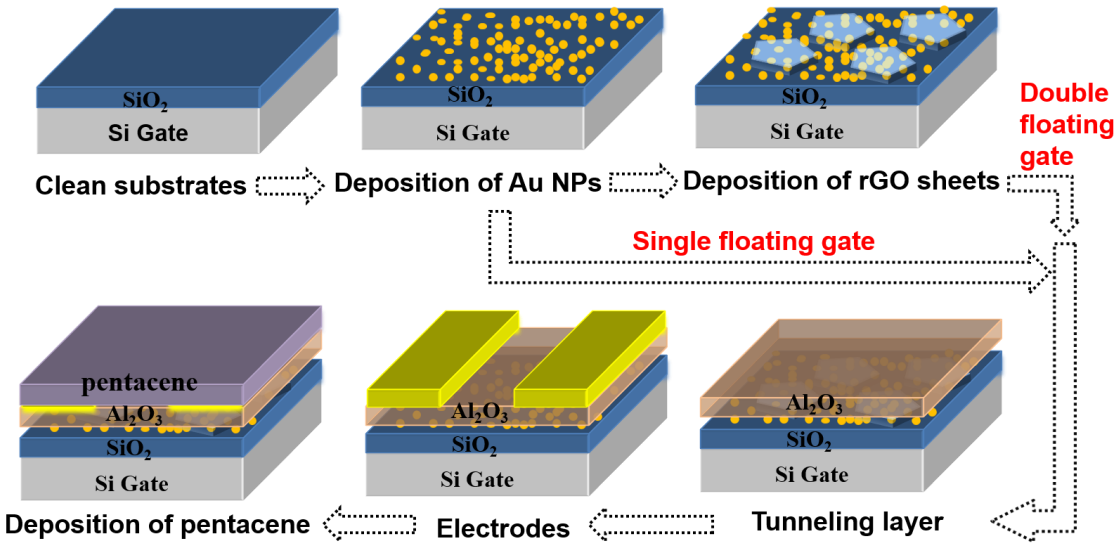

Figure 3.2 The schematic diagram process to prepare single NFGM (using one layer of Au NPs as floating gate) and double NFGM (using lower Au NPs and upper rGO sheets as hybrid double floating gate).

• *Measurements*

• *SEM*

The deposition of Au NPs on the surface of SiO_2 was characterized by SEM, as shown in figure 3.3. The Au NPs are uniform in size and no aggregation is observed due to the electrostatic repulsion between the neighboring Au NPs [18, 19]. For observing the memory properties by using Au NPs as the floating gate, the maximum density of Au NPs should be from 10^{11} to 10^{12} NP/cm^2, which is the repulsive-limited saturation coverage [20]. The device with Au NPs density excess to 10^{12} NP/cm^2 would not exhibit memory properties duo to the short circuit may exist between source and drain [17].

To adjust the density of Au NP in our experiments, we prepared the sample with different duration in the solution of Au NP. The result showed in figure 3.3(a) is the sample treated with duration of 30 min, and we can see that the density of Au NPs was found just ~2.3

$\times 10^{10}$ NP/cm^2. When the duration increased to 1 h, the density of Au NPs was ~2.5$\times 10^{10}$ NP/cm^2, shown in figure 3.3(b). When the duration increased to 2 h, 5 h and 12 h, we found the density of Au NPs was ~1.1$\times 10^{11}$ NP/cm^2, ~1.6$\times 10^{11}$ NP/cm^2 and ~1.8$\times 10^{11}$ NP/cm^2, seen in figure 3.3(c), (d), (e), and the Au NPs were uniformly dispersed on the solid surface without any aggregation, which could limit the flow of charges by electrostatic repulsion between neighboring Au. Thus, the sample immersed in the solution of Au NPs with duration more than 2 h could be used as the floating gate in our memory devices. The zoom of the part of (e) also verified that the radium of the Au NPs is around 10 nm.

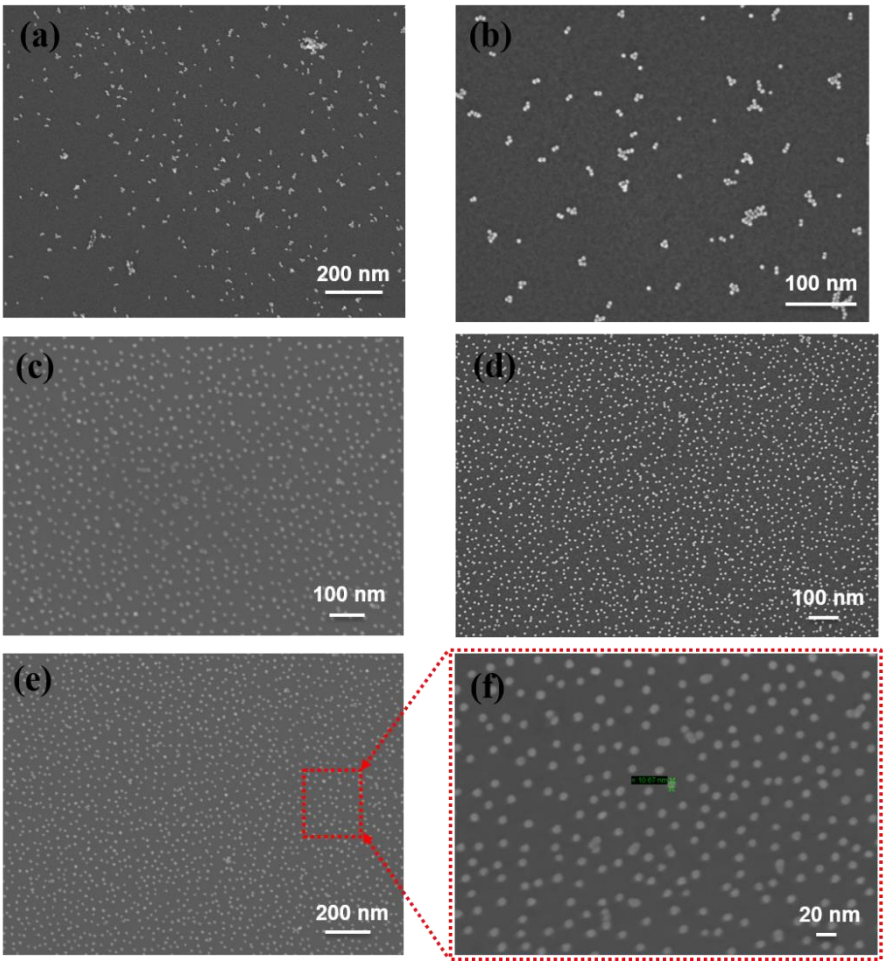

Figure 3.3 The SEM of the Au NPs deposited on functionalizedSiO_2surfaces with different duration time. (a) 30 min, (b) 1 h, (c) 2 h, (d) 5 h, (e) 12 h, (f) zoom of part of (e).

Figure 3.4 shows the SEM images of Au NPs covered with rGO sheets. To control the coverage of rGO sheets, the different drop times of rGO solution and the different annealing ways were carried out in the experiments. As we can see, when rGO solution was dropped 3 times on the sample and then did the annealing process, the percentage of rGO sheets coverage

is less than 30%, shown in figure 3.4(a). When the sample was treated by annealing after each drop of rGO solution and repeated the process for 3 times, the percentage of rGO sheets coverage is less about40%. After increased the drops to 5 times and followed by annealing process, the percentage of rGO sheets coverage is almost 50%, shown in figure 3.4(c). In addition, when the sample was tread by annealing after each drop of rGO solution and repeated the process more than 5 times, we found that the percentage of rGO sheets coverage is more than 60%, seen in figure 3.4(d), (e), (f). Figure 3.4(f) shows the zoom of part of figure 3.4(e) to observe the rGO sheets more clear. However, we found rGO sheets formed some multilayer for all the samples, which may affect the morphology of pentacene semiconductor but could still be an upper floating gate to improve the performances of the memory devices.

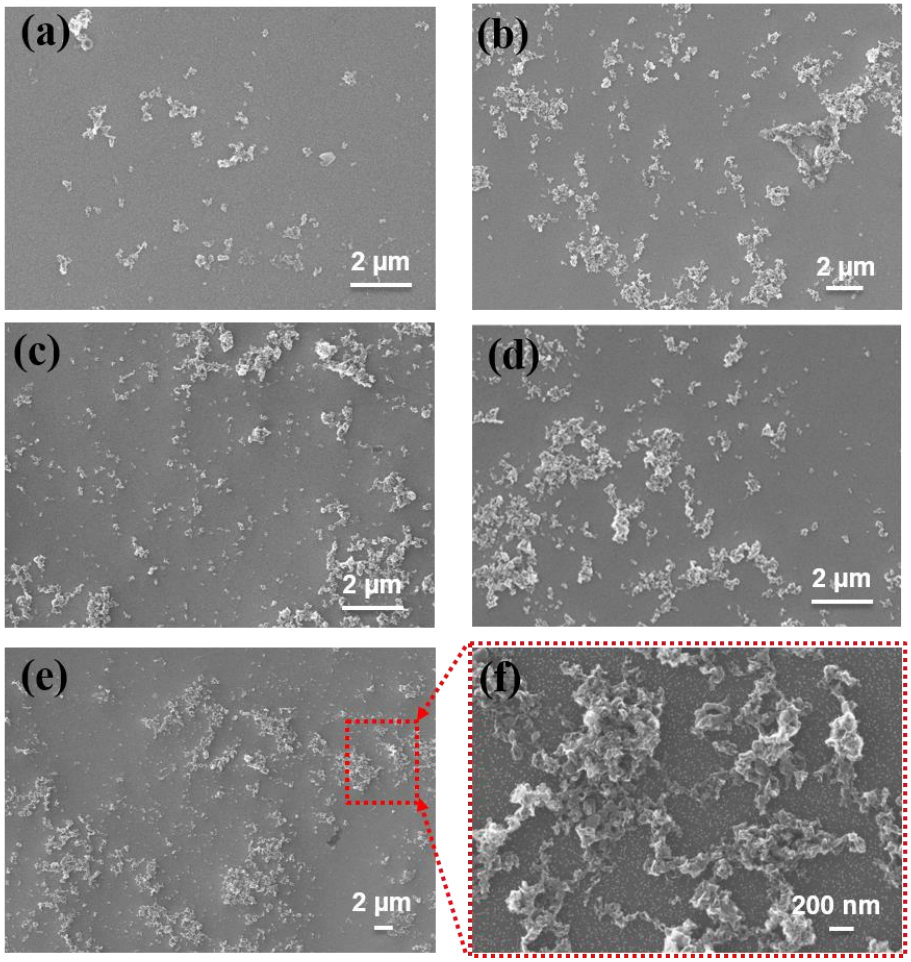

Figure 3.4 The SEM mages of Au NP covered with rGO sheets. (a) with 3 drops of rGO solution followed with annealing, (b)annealing after each drop and repeat for 3 times, (c) with 5 drops of GO solution followed with annealing process, (d) annealing after each drop and repeat for 5 times,(e) annealing after each drop and repeat for 8 times, (f) zoom of part of (e).

• *AFM*

The AFM comparison of pentacene deposited on bare SiO_2, bare gold, OTS modified SiO_2, and PFBT modified gold electrodes has been described in chapter 2.4.1, here, we just characterized the AFM morphology of pentacene thin films deposited on PFBT SAM modified electrodes and bare SiO_2 dielectric for the double NFGM to have a result. Figure 3.5 (a) displays the 3d AFM morphology of pentacene deposited on PFBT SAM modified electrodes and bare SiO_2 dielectric. It scanned from the source to channel gap, as well as to drain with a size of 10 µm×10 µm. The pentacene shows a thin film phase with a root mean square roughness 7.8nm on PFBT modified electrodes areas and 10.8 nm on SiO_2. The clear zoom AFM images of pentacene on electrode and SiO_2 are displayed in figure 3.5(b) and (c), respectively. The 30 nm thick pentacene thin films were measured by profilometry. And compared to the AFM results of transistor with PFBT modification in chapter 2.4.1, the characteristics are almost the same.

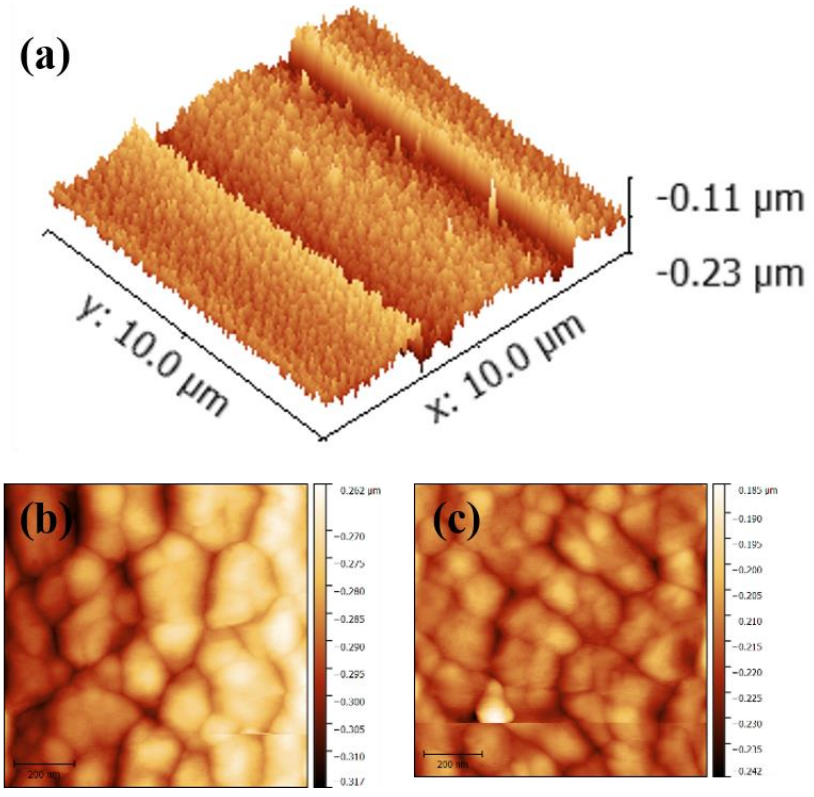

Figure 3.5 (a) The 3d AFM morphology of pentacene deposited on PFBT SAM modified electrodes and bare SiO_2 dielectric, the clear zoom 2d AFM images of pentacene on electrode and SiO_2 are displayed in figure 3.5(b) and (c), respectively.

3.3 The memory electrical properties

3.3.1 The memory performances of SAM modified DFG memory

In order to get the voltage operations for the measurements of our NFGM devices, the NFGM sample with PFBT modification was first used to do the tests. The electrical properties were also characterized with the Agilent 4156C instrument in glove box.

At beginning, the typical transfer and output characteristics of the PFBT SAM modified DFGM memory device were performed and showed in figure 3.6.

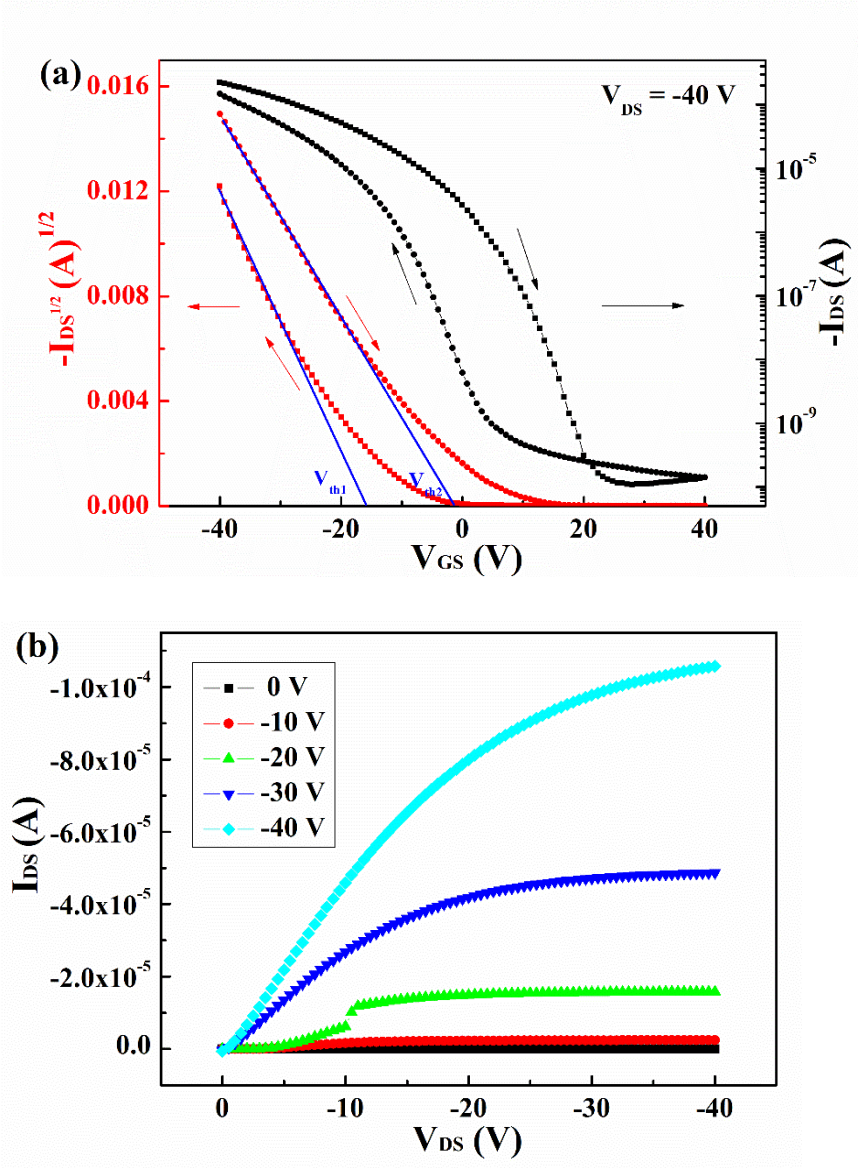

Figure 3.6 The typical (a) transfer with the gate sweep voltage ranges (40 V to -40 V to 40 V) at V_{DS}=-40 V and (b) output characteristics of the PFBT SAM modified double NFGM device.

The measurement operation was carried out as the same as measure a transistor devices. As we can see in figure 3.6(a), during the measurement, the gate sweep voltage ranges (40 V to -40 V to 40 V) at V_{DS}=-40 V, the memory device shows a hysteresis curve with a window about 18 V, which means there is nonnegligible charging or/and discharging of charge carriers occurred in the device system. Figure 3.6(b) shows the typical p-channel output curves respect to the gate bias voltage. The curves performed at the small gate bias part are linear character, indicating that the contact resistance between the electrodes and probes could be very small and associated with the previous reports. Based on the hysteresis characteristic of the device measured as a transistor, we subsequently display the memory performances by changing the operation voltages.

Then, to get more information of gate bias values during the operation of the measurement for NFGM, the bias hysteresis under the application of V_{GS} sweeping ranging from ±30 V to ±100 V with a fixed V_{DS} value of -40 V were carried out and showed in figure 3.7.

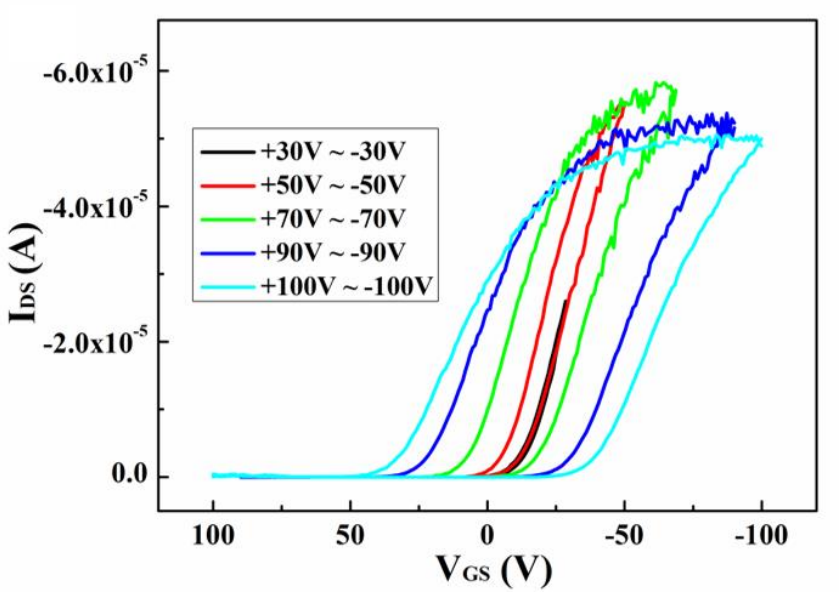

Figure 3.7 The bias hysteresis under the application of VGS sweeping ranging from ±30 V to ±100 V with a fixed V_{DS} value of -40 V.

The large bias hysteresis means the large shifts of the V_{Th}, and the memory window is defined as shift value of V_{Th} respect to the applied program/erase bias pulses [7]. From the result, we can see that when V_{GS} sweeping in the range of +30 V to -30 V, there is no hysteresis observed. With the increase of the gate sweeping voltage, the window of hysteresis engenders

and increases, which means there are more holes are trapped in the floating gate when the gate bias is large. As the reversible bias hysteresis is obviously observed with the application of V_{GS} $\geqslant \pm 70$ V, thus, a sequential programming and erasing operations performed by applying of V_{GS} −90 V and V_{GS} +90 V is determined in our following experiments.

Figure 3.8(a) and (b) show the shift of the I_{DS} under different program/erase (P/E) speed (changes from 10^{-4} s to 10^{1} s) and the change in the extracted value of threshold voltage (memory window) respect to the P/E speed, respectively.

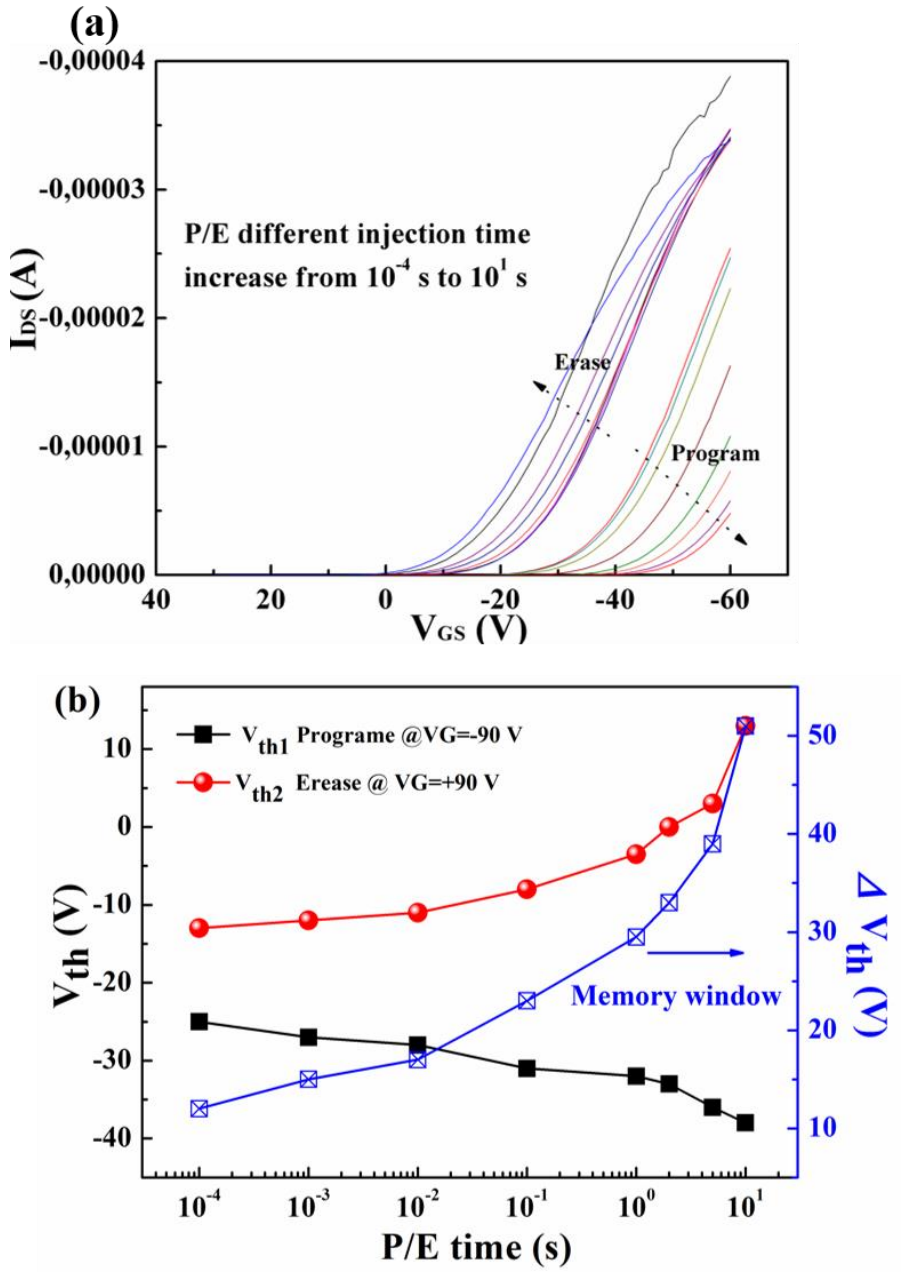

Figure 3.8 (a) the shift of the I_{DS} under different program/erase (P/E) speed (changes from 10^{-4} s to 10^{1} s), (b) the change in the extracted value of threshold voltage (memory window) respect to the P/E speed.

From the results of figure 3.8(a), the phenomena of I_{DS} shifts with the change of P/E speed is observed and the V_{Th} is extracted. Initially, after programming operation with gate bias pulse of -90 V for injection of 10^{-4} s, the value of V_{Th1} is -25 V, and then it shifts to V_{Th2} -13 V after erasing at the gate bias pulse of +90 V for injection 10^{-4} s, thus the memory window is 12 V at this P/E speed. With the increase of P/E injection time, the V_{Th} shifts more away from the initial value and the memory window is increased, it means more holes are trapped in the floating gate. Overall, the memory window increases up to 51 V when the P/E injection time reach up to 10 s. Despite it is not very good to operate long P/E injection time for the application of memory devices, the memory window of our device still could be as large as 12 V even the program/erase operation time is just 10^{-4} s.

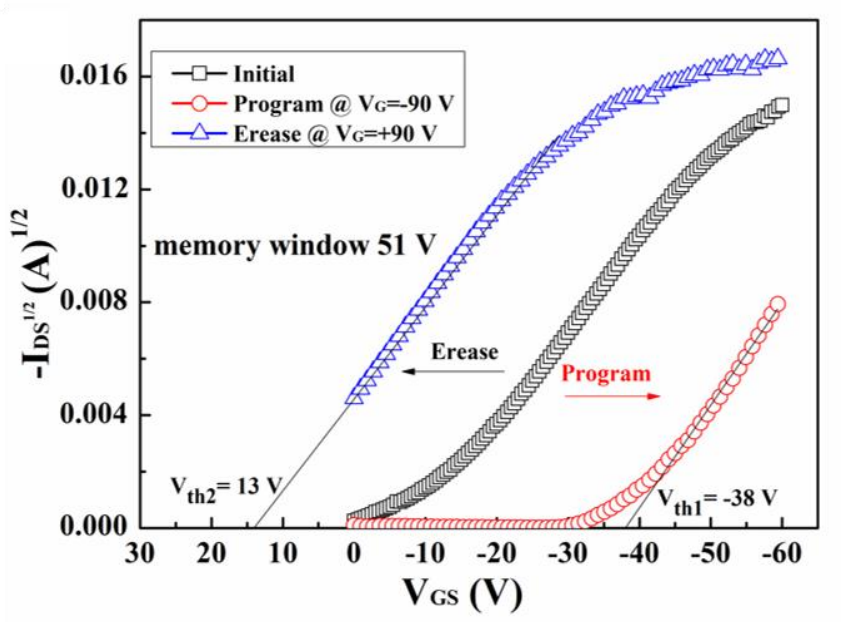

Figure 3.9 Thetypical memory transfer curves of DFG memory with PFBT monolayer, plotted with $(I_{DS})^{1/2}$ versus V_{GS}after gate bias pulses ±90 V for 10 s

The typical memory transfer curves plotted with $(I_{DS})^{1/2}$ versus V_{GS} at gate bias pulses ±90 V for 10 s is displayed in figure 3.9. After obtaining the initial curve (black line) with gate sweep from 0 V to -60 V, a negative voltage -90 V is applied to the bottom gate electrode, the holes could be ejected from the pentacene channel to the floating layers through the thin tunneling layer, and the holes are preferable first charged in the lower floating gate (Au NPs layer) according to the Ref. [21]. In this DFG memory, when the Au NPs getting saturated to trap the holes under the constant programming voltage, the extra holes could be trapped by the upper rGO sheets layer [22]. Therefore, it causes a depletion zone to be formed within the

channel, and results in a lower current during the I_{DS} versus V_{GS} measurement, as a consequence, the transfer curve shifts to the negative bias (red line in figure 3.9), and the shift confirms that the charges are trapped in the floating gate. Then applying the positive voltage +90 V to the bottom gate, the holes stored in the Au NPs would be rejected back to the channel, resulting in a positive V_{Th} shift (blue line).

Generally, the transfer curve should almost shift back to the same position of initial state after erasing operation. But here a lot of difference (the shift of black line to blue line) is found for the device, which means the charge density after the erase process is quite different from the initial state. The explanation for this phenomenon is proposed to be the reason of the increase of charge injection and would be verified in the later discussion.

3.3.2 The effects of rGO sheets

• *Transfer characteristics*

Many works have reported the different memory performances of NFGM devices by using different kinds of floating gate. To study the effects of Au NPs and rGO sheets floating gate on the memory performances in our experiments, the transfer characteristics with $(I_{DS})^{1/2}$ versus V_{GS} of SFG and DFG memory without any SAM modification are presented in figure 3.10. To unconcern the effect of PFBT monolayer on the performances of NFGM here, the performances of memory devices showed in this part are the results of SFG and DFG memory without PFBT monolayer modification.

In figure 3.10, we can see that both of the memory devices show V_{Th} shifts after the program/erase operation, the memory window is 24 V for the SFG memory. And the memory window is increased to 37 V for the DFG memory after assembled the rGO sheets as the upper floating layer. The origin state (black line) in figure 3.10 (a) and (b) is almost at the same stage for the two devices, after program process, the V_{Th} shifts to -21 V for the SFG memory, whereas the V_{Th} shifts to -42 V for the DFG memory, which means more holes are trapped in the floating gate, it further verifies that after the Au NP getting saturated under the constant programming voltage, there may be extra holes are trapped by the upper rGO sheets layer in this DFG memory.

Figure 3.10(c) and (d) show the voltage bias hysteresis under the application of V_{GS} sweeping range of $\pm$30 V to $\pm$90 V. The SFG memory presents narrow memory windows and

the memory window does not further increase obviously even applied a high voltage of V_{GS} ±100 V. On the contrary, the DFG memory presents obviously increased memory windows with the increase of V_{GS}. The large hysteresis loops for the DFG memory prove that these different memory characteristics compared with the SFG memory are mainly resulted from the supplementary of rGO sheets, the charges could be trapped in the Au NPs/rGO sheets hybrid floating gate. The difference results further indicate that the use of only Au NPs as the floating gate in NFGM induces a saturated state under the constant V_{GS} programming voltage, it further explains the necessary of an additional trapping layer for the charges. And these rGO sheets have a high density of states with a semi-metallic band structure that is nearly similar to that of metal NPs, therefore, rGO could produce a lower gate coupling ration and enhance the memory window [23].

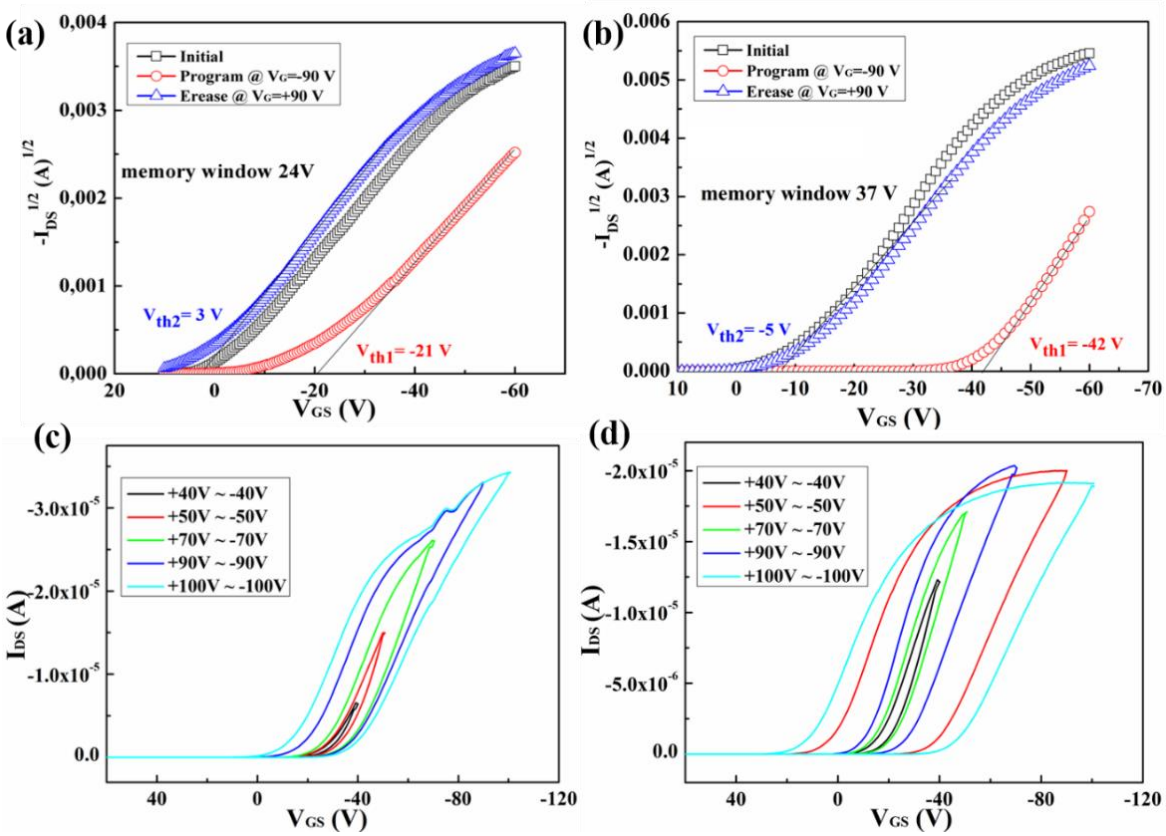

Figure 3.10 The typical memory transfer curves plotted with $(I_{DS})1/2$ versus V_{GS} after gate bias pulses ±90 V for 10 s of (a) SFG and (b) DFG memory, the bias hysteresis under the application of V_{GS} sweeping range of ±30 V to ±90 V of (c) SFG and (d) DFG memory.

• *The retention and endurance characteristics*

The charge endurance and retention capabilities are the important merits for nonvolatile memories. In this part, the endurance and retention properties of our SFG and DFG memories are carried out and compared.

The way of V_{GS} voltage operation to obtain the endurance properties is shown in figure 3.11(a), the endurance properties based on the values of I_{DS} was measured by repeating continuous P/E operations with bias pulse of ±90 V for 1 s. The I_{DS} character of SFG and DFG memory is shown in figure 3.11(b). In each program/erase operation, a reading voltage of V_{GS} -25 V was applied to verify the distinguishable I_{DS} current state (lies in between program V_{Th} and erase V_{Th}) for reliability. As a result, we can see that no degradation and break down were observed for the SFG and DFG memory until repeated P/E 1000 cycles, it indicates that the P/E state is well maintained with the changeable of V_{GS} pulse bias.

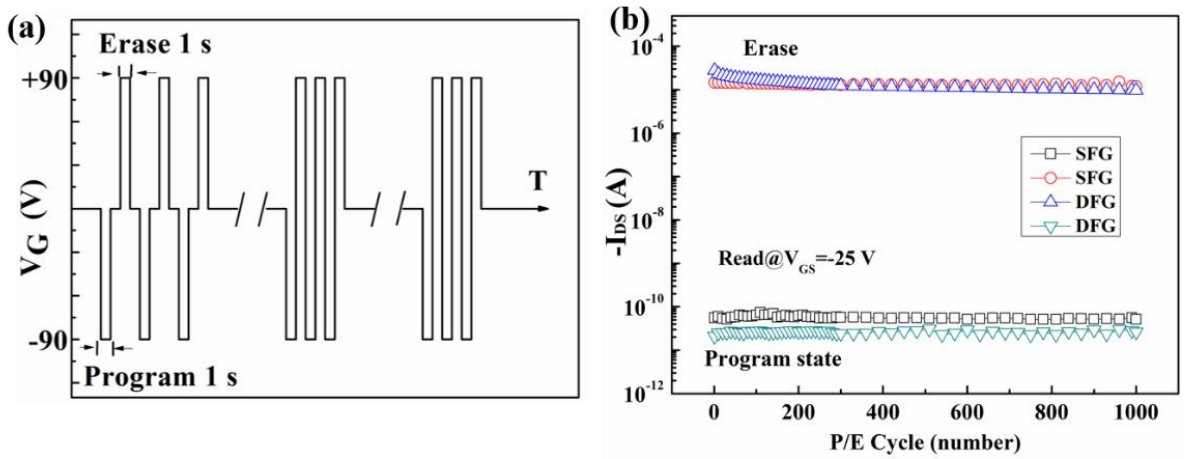

Figure 3.11 (a) The application of P/E bias pulse of repeating +90 V/-90 V for 1 s, (b) the endurance characteristics of the SFG and DFG memory. The I_{DS} values were read at V_{GS}=-25 V.

Figure 3.12(a) shows the way of program/erase (P/E) pules operations to obtain the retention property, the I_{DS} values were read at V_{GS}=-25 V over a time interval of 10 s after the application of P/E bias pulse of +90 V/-90 V.

The retention property based on I_{DS} values of SFG and DFG memory are shown in figure 3.12(b). The SFG memory shows the data retention around 10^5 s, around 60%~70% charge loss is observed at the time with value of 10^4 s. However, DFG memory shows significate longer

data retention time compared to the SFG memory by extrapolation exceed 10^8 s. It confirms that the upper rGO sheets plays a crucial role on the retention property in NFGM devices.

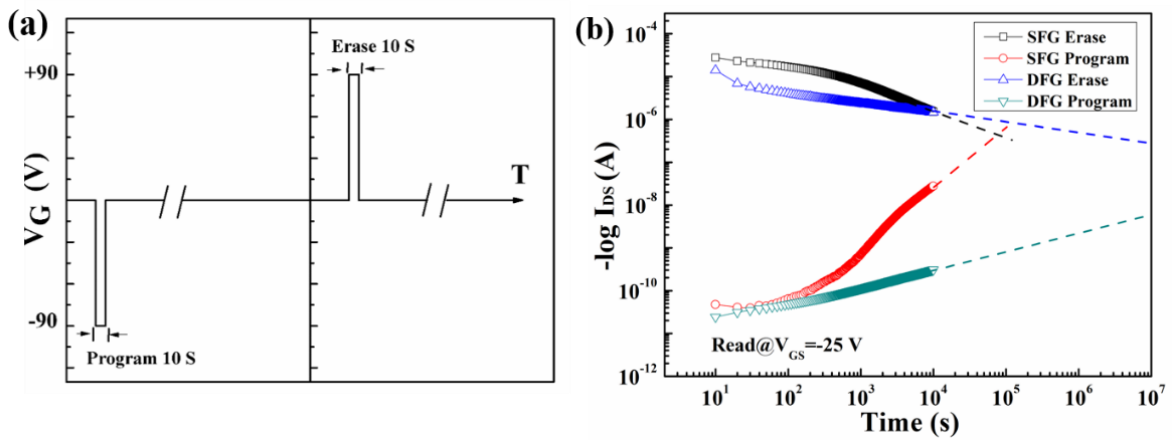

Figure 3.12 (a) The application of P/E bias pulse of +90 V/-90 V for 10 s, (b) the retention characteristics of the SFG and DFG memory. The IDS values were read at V_{GS} =-25 V.

• *The schematic energy diagrams*

The energy band diagram to explain the charge transfer mechanisms in SFG and DFG memory is shown is figure 3.13.

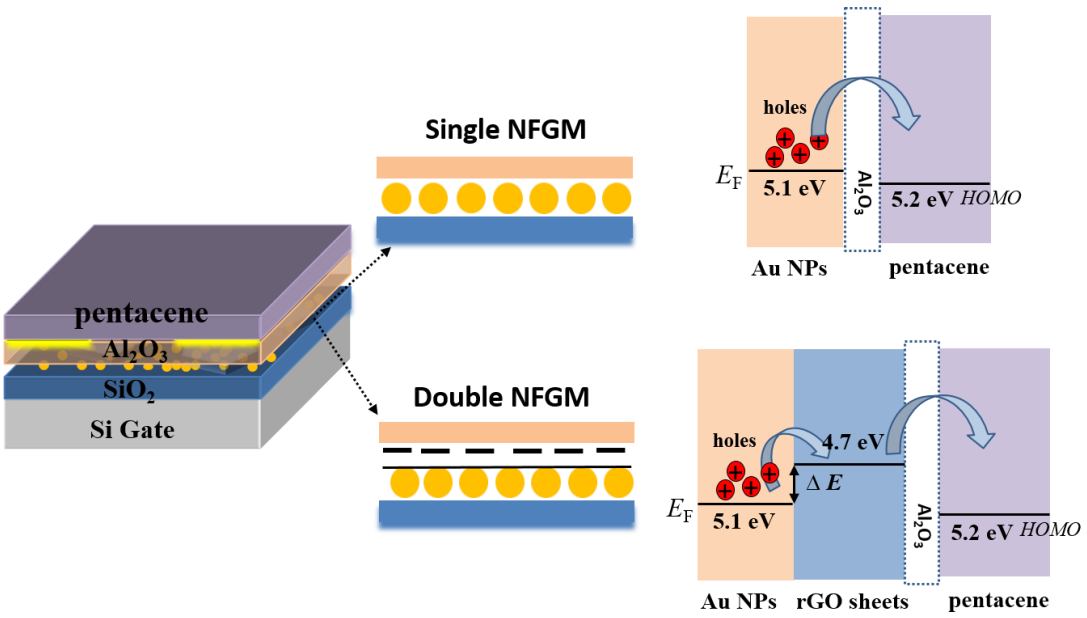

Figure 3.13 The schematic configuration of the NFGM device with SFG and DFG; the energy band diagram of holes release from Au NPs to pentacene during the erase operation for the SFG and DFG memories.

The supplementary of rGO sheets effectively improve the memory window because of the increase of charge traps. And the improvement of retention property of memory is explained by the schematic energy diagrams of the holes transfer after erase operation. Here, it signifies to indicate that during the erase operation, the holes stored in the Au NPs would overcome the energy barrier height induced by the difference Fermi levels between rGO sheets and Au NPs first then transfer back to the channel. In this case, the memory fabricated with rGO sheets and Au NPs double floating gate could perform better retention properties than single floating gate memory.

As shown in figure 3.13, the values of the work function of Au NPs and rGO are from Ref. [3, 24, 25], the HOMO level of pentacene is from Ref. [26]. As the work function of rGO sheets reduced chemically is around 4.7 eV, which is smaller than the work function of Au NPs ~ 5.1 eV, as a result, there is an energy barrier height ΔE exists between the Au NPs and rGO sheets, and the holes in the lower nano-floating gate need to overcome the barrier to transfer back to the channel.

• *The memory window statistic*

We note that the each memory sample fabricated on the Si substrate in our experiment totally including 32 memory elements (as the electrodes are patterned with arrays of 8×4 linear memory with channel length from 1 μm to 50μm and channel width 1000 μm). The frequency distributions of memory window for the SFG and DFG memories were calculated and are displayed in figure 3.14.

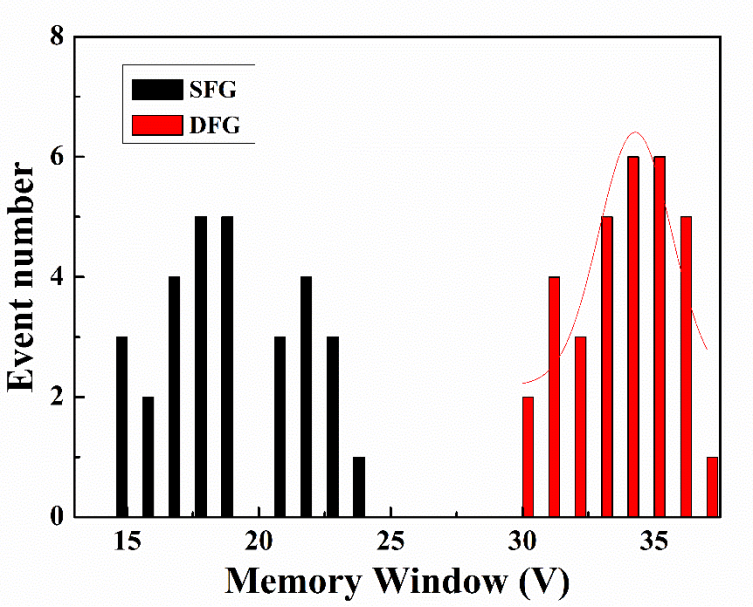

Figure 3.14 The memory window statics of the SFG and DFG memories.

From the statics results, we can see that the functional memory device is 100% for both of the SFG and DFG memories. And the average memory window is 18.8 V for SFG and is 33.6 V for DFG memory. In addition, compare the results of SFG and DFG memory, the decrease of the variability for the memory window is observed in DFG memory, indicating that adding the rGO sheets as the upper floating gate could also keep the charges be trapped/detrapped more stable even in different channel length.

3.3.3 The effects of PFBT SAM

Compared the transfer characteristics of NFGM with and without PFBT monolayer, seen in figure 3.9 and figure 3.10(a) and (b). The erase state for the NFGM without PFBT is almost at the same stage, whereas the erase state of the NFGM with PFBT shifts far away from the initial state (blue line shifts to black line), in this part, the influence of the PFBT monolayer on the performance of our NFGM devices is discussed.

• *Transfer characteristics of SFG with PFBT.*

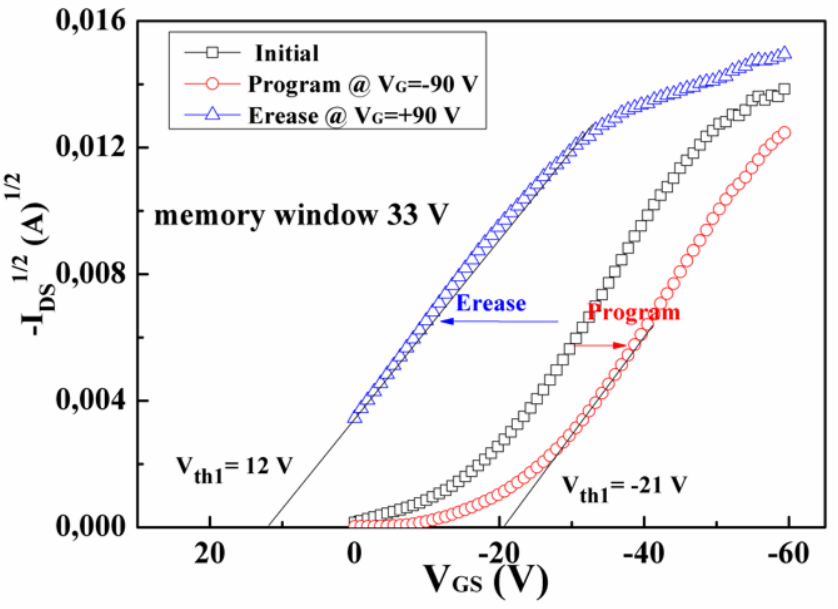

Figure 3.15 The typical memory transfer curves of SFG memory with PFBT monolayer, plotted with $(I_{DS})^{1/2}$ versus V_{GS} after gate bias pulses ±90 V for 10 s.

As the transfer characteristics of SFG and DFG without PFBT, as well as the DFG with PFBT modification has been presented. Here, figure 3.15 displays the transfer curves of SFG with PFBT monolayer. We can see that the performance of this memory device is quite the

same as figure 3.9. After obtaining the initial curve (black line) with gate sweep from 0 V to -60 V, a negative voltage -90 V is applied to the bottom gate electrode, the transfer curve shifts to the negative bias (red line), the charges are trapped in the floating gate. Then applying the positive voltage +90 V to the bottom gate, the holes stored in the Au NPs would be rejected back to the channel, resulting in a positive V_{Th} shift (blue line). However, the blue line also shifts to initial black line, the transfer curves of the SFG with PFBT also implies the PFBT monolayer affects the memory properties

• *The retention characteristics*

To see clearer different I_{DS} characters of the memory devices with and without PFBT modification, the retention properties were carried out and presented in figure 3.16. The I_{DS} values were read (at V_{GS} =-25 V) over a time interval of 10 s after the application of P/E bias pulse of +90 V/-90 V, which is the same operation as previous measurements. The values of the retention time for DFG memories with and without PFBT are determined to be more than 10^8. The program state is almost at the same stage for the two devices, whereas a distinguishable erase state is obviously investigated, which means after the erase operation, the density of the charges released from the Au NPs floating gate back to the semiconductor is different for the two devices.

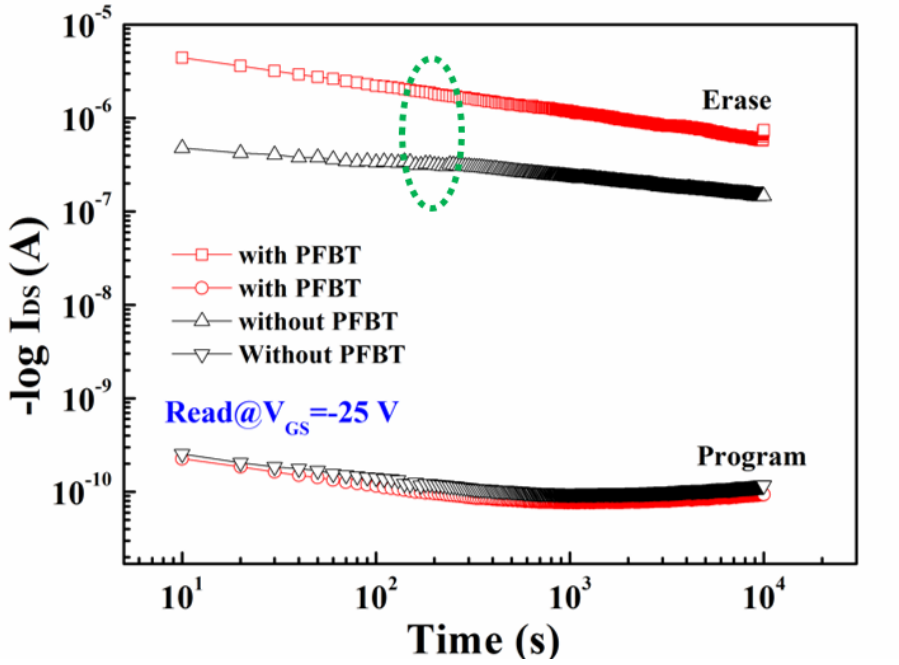

Figure 3.16 The retention characteristics of the SFG and DFG memory.

• *The memory window statistic*

The frequency distributions of memory window for the DFG memories with and without PFBT modification were calculated and are displayed in figure 3.17. From the statics results, the functional memory device is 100% for the two memory samples. And the average memory window is 33.6 V for DFGwithout PFBT and is 48.8 Vfor DFG memory with PFBT. And the decrease of the variability for the memory window is observed for the DFG memory with PFBT modification, thus the PFBT modification also improve the stability of charges trapped/detrapped in the floating gate.

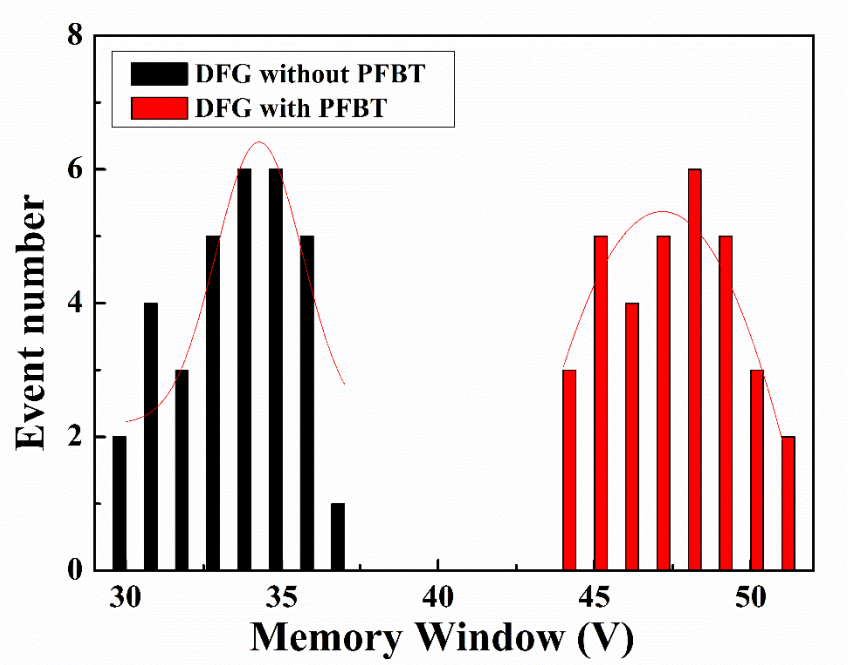

Figure 3.17 The memory window statics of the DFG memory with and without PFBT modification.

• *The XPS and UPS analysis*

The effects of PFBT on the pentacene and electrodes could be directly analyzed by using XPS and UPS. Figure 3.18(a) shows the respective C1*s* spectra of PFBT and pentacene deposited on PFBT, the C 1*s* peak of PFBT/Au shows the C-C bond and C-F bond at 284.8 eV and 286.7 eV, respectively. And the C1*s* peak of pentacene/PFBT/Au shows symmetric shape with a peak centered at 284.4 eV, resembles a thin-film-phase pentacene. The shift of the C-C peak after pentacene deposition with 0.4 eV implies the electronic interaction between pentacene and the PFBT thiol surface due to the molecule dipoles with different directions and moments within the PFBT thiol. In figure 3.18(b), the UPS spectra show the work function values of bare gold and gold with PFBT are 4.73 eV and 5.26 eV, respectively. The Results of

XPS and UPS are associated with the results that depicted in chapter 2.4.3. Thus, in the NFGM device with PFBT modification, more charges from the electrodes injection are trapped in the Au NPs after the programming operation, resulting in the increase of charges released back to the pentacene during the erase operation.

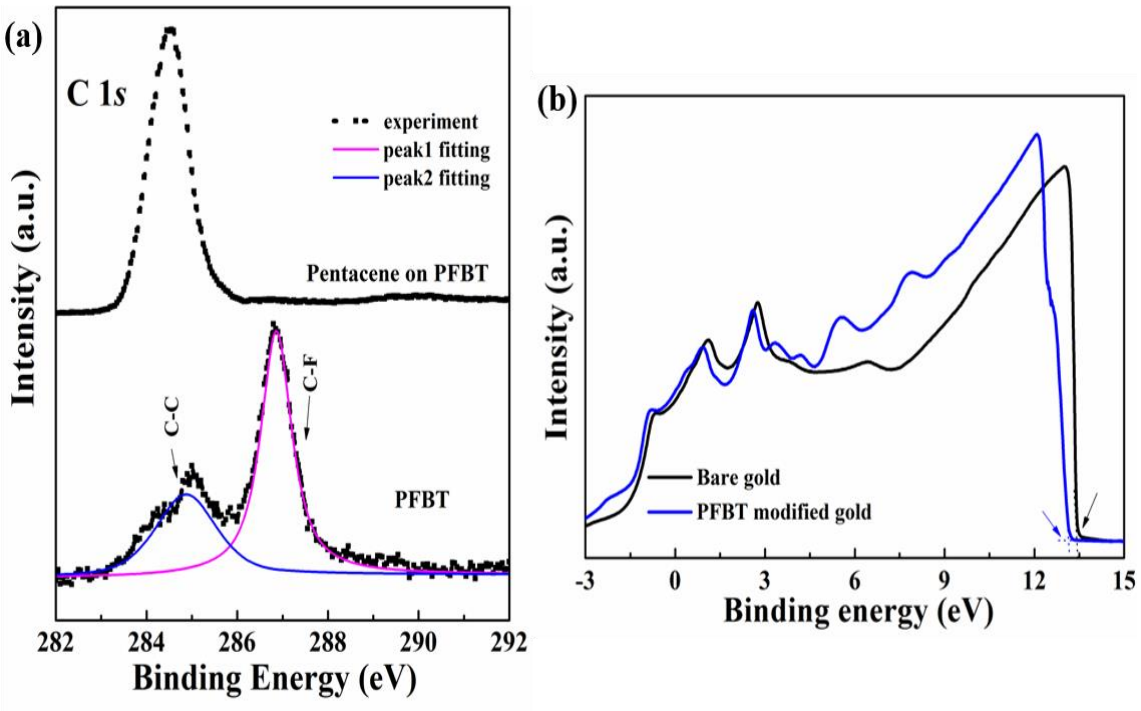

Figure 3.18 (a) The respective C1s spectra of PFBT and pentacene on the PFBT, (b) the UPS He I (21.2 eV) spectra under 3 eV results of bare gold the PFBT-modified gold.

• *The* schematic diagrams of physical mechanisms

From the I_{DS}-V_{GS} and I_{DS}-Time results, we found that the PFBT effectively affect the memory properties in our memory devices, especially after the erase operation, the erase state shifts far away from the initial sate. In addition, to better understand the effect of PFBT monolayer on the performances of NFGM devices. The schematic diagrams of physical mechanisms for the charge transport during the P/E operation in NFGM with PFBT are depicted in figure 3.19. At beginning, an initial transfer curve is measured, when the gate bias pules -90 V was operated, the intrinsic charges in pentacene are rejected to the floating gate and be stored, shown in figure 3.19(a). Then, the programming transfer curve is measured with gate sweep from 0 V to -60 V. during this process, because of the PFBT modification, more charges are injected in the semiconductor and even transfer to the floating gate under the gate voltage, inducing more charges trapped in the floating gate, shown in figure 3.19(b). On the contrary,

when the gate bias pules +90 V was operated for the erasing process, the charges are all released back to the pentacene, shown in figure 3.19(c), resulting in the charge density in pentacene is quite different from the intrinsic state and increased. It further explains the erase state shifts from the initial state in figure 3.9 and figure 3.15.

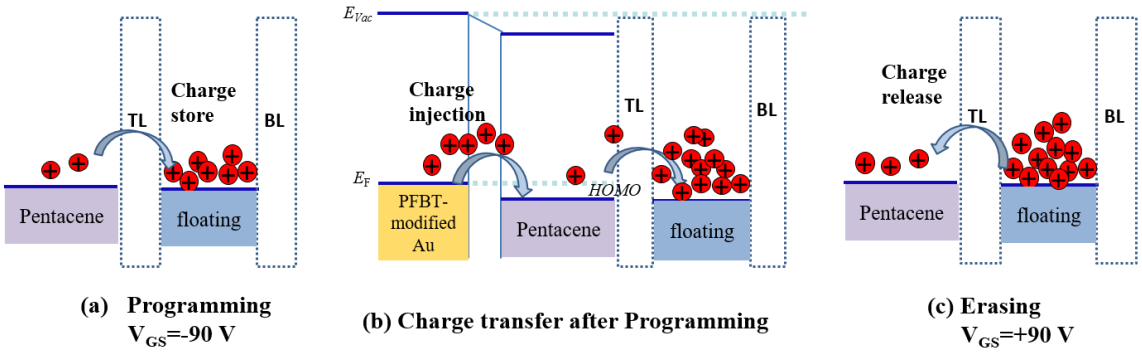

Figure 3.19 The schematic diagrams of physical mechanisms for the charge transport during the P/E operation in NFGM with PFBT.

3.4 The comparison of electrical parameters

To better compare the performances of the different kinds of NFGM devices that fabricated in our experiments, the relative electrical parameters such as memory window, mobility, retention time were extracted from the measurements results.

In the parameters for valuing the property of memory devices, the trapped charge density in the floating gate is a crucial data. In general, the trapped charge density in the NFGM device is simply estimate calculated by the equation of (3-1).

$$Q = C_i \Delta V_{th} \tag{3-1}$$

where C_i is the capacitance per unit area and ΔV_{Th} is the memory window [7, 27]. For our NFGM devices, C_i is measured by capacitance versus voltage (C-V) with the MIS capacitor structure of Au/Pentacene/Al_2O_3(10nm)/SiO_2(200nm)/Si(N-type), and we obtained the value of 2.3×10^{-8} F/cm^2.

Consequently, the electrical parameters extracted from different I-V measurements for the four kinds of memory devices are summarized in table 3-1 for comparison.

Table 3-1. Comparison of the electrical parameters for SFG, DFG with/without PFBT modification.

NFGM	Carrier mobility ($cm^2V^{-1}s^{-1}$)	Memory Window (V)	Trapped charge density (C)	Subthreshold swing (V/decade)	P/E current ratio	retention time (s)
SFG	0.03	24	5.52×10^{-7}	1.6	$>10^4$	$\sim10^5$
SFG with PFBT	0.045	33	7.59×10^{-7}	1.1	$>10^4$	$\sim10^6$
DFG	0.053	37	8.6×10^{-7}	1.2	$>10^4$	$>10^7$
DFG with PFBT	0.23	51	1.19×10^{-6}	0.8	$>10^5$	$>10^8$

From the summery of parameters of our NFGM samples, we found the DFG memory with PFBT modification showed the best performances. Under the P/E operation voltages of -90/+90 V, the memory window was calculated as large as 51 V, the current ratio is $>10^5$, and the retention time is expected to exceed 10^8, it means the properties of the NFGM are enhanced compared to the pentacene based NFGM that reported in rent years (summarized in the table 1-1 in chapter 1). In addition, for the DFG memory that fabricated with rGO sheets and Au NPs, the charge trap density was improved compared the SFG, which is associated with the previous reports [3]. In particular, we used SAM to modify the NFGM devices and found that the SAM modification also plays an important role to improve the performances of NFGM.

3.5 Conclusions

In this chapter, the pentacene based NFGM with/without PFBT monolayer by using Au NPs and rGO sheets as charge trapping layers are successfully fabricated. The performances of SFG (Au NPs as floating gate) and DFG (hybrid Au NPs and rGO sheets as the lower and upper floating gate, respectively) were presented and compared. The memory window, especially the charge retention time were enhanced by assembling the rGO sheets, which due to an energy barrier height ΔE exists between the Au NPs and rGO sheets, In detail, the effect of rGO sheets on the memory properties were well discussed.

Furthermore, the NFGM with and without chemical treating of PFBT SAM were also presented and compared. The NFGM with PFBT exhibits excellent memory performances, including high mobility of 0.23 $cm^2V^{-1}s^{-1}$, the large memory window of 51 V, and the stable retention property more than 10^8 s, as well as reliable cycling endurance over 1000 cycles. The

optimized performances of the NFGM are explained by the increase of charge injection due to the increase of the work function of gold electrodes after the PFBT modification, which further resulting the increase of trapped charge density in Au NPs floating gate. In particular, the results highlight the utility of SAM modulations and controlling of charge transport in the development of transistor memories. However, the P/E operation voltages for our NFGM devices are still quite high, and the fabrication process with EBL is not an economy way for commercial applications. Thus, in the next step of this thesis, we fabricated NFGM with all organic materials on flexible substrate.

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Chapter 4

Preparation and characterization of OFET and NFGM on flexible substrate

Chapter 4 Preparation and characterization of OFET and NFGM on flexible substrate

4.1 Introduction

Due to the merits of organic materials such as mechanical flexibility, solution processability, and light weight characteristics, organic semiconductors and organic dielectrics are essentially expected to meet emerging technological demands that realizing flexible and wearable electronic devices, where silicon-based electronics cannot provide a solution. OFET, as one of the basic elements in various flexible and wearable integrated electronic circuits, has been widely studied and used. It is necessary to improve the performances of flexible OFET including reduction of the operating voltage and leakage current, and improvement of the mechanical characteristics under various bending conditions for devices [1-4]. The electrical performances of the OFET are extremely corresponding to the properties of the organic semiconductors and dielectrics. The dielectrics could affect the growth of the semiconductors, the charge transport, and the stability of the OFET [5, 6]. To achieve the high performances of OFET, many reports have focus on the study of the gate dielectric layers, for example, selection of high-k metal oxide Al_2O_3, TiO_2 [7], passivation of the dielectric surfaces by inserting self-assembled monolayers [8], and deposition of thin polymer/high-k oxide hybrid dielectric layers [9].

Moreover, in order to take the advantage of flexible nature and low cost roll to roll technology of organics, various polymer dielectrics such as Polyvinyl pyrrolidone (PVP), polystyrene (PS), polymethyl methacrylate (PMMA), poly(chloro-p-xylene)-C (Parylene-C) have been extensively used in OFET as the gate dielectrics [10-16]. In the past few years, the investigation of organic dielectrics has become more and more important not only due to their functional applications, but also the decrease of the interfacial trap density between dielectrics and semiconductors [17]. In the various polymer dielectrics, recently, Parylene C (PC) has been reported not only as a gate dielectric [14], but also as water passivation layer for soft devices [18], encapsulation and ultra-thin substrate [19], due to its high dielectric property, uniform thickness, low moisture sorption, stretchable properties, as well as inertness. In addition, the PC could also undergone stander lithography to obtain miniaturized flexible integrated circuit

[20]. Thus, in this work, the PMMA and PC polymeric thin films were selected as the dielectric layers and substrate.

One of the prerequisite for realizing the flexible electronic devices is the use of a thin substrate that can be bent into a small radius. Organic transistors are often fabricated on sheets of polyimide (PI), polyethylene naphthalate (PEN) or polyethylene terephthalate (PET) flexible substrate [15, 21, 22]. Normally, the selection of the flexible substrate is depended by the fabrication process and the applications of the devices.

In this chapter, we mainly presented the pentacene based transistors and memories fabricated on flexible substrates. The insulator polymer PMMA, PC were used as the bilayer gate dielectric layers. The electrodes were deposited by simple thermal deposition. The materials used in this device are all organics and the devices were fabricated with low temperature during the fabrication process. For the I-V characteristics, the operation voltage was deduced and there was no hysteresis observed, which means that the interface traps between the dielectrics and were decreased. Then, the NFGM devices were fabricated on flexible substrates by using the same structure of the flexible transistor and the performances were demonstrated.

4.2 Experimental

4.2.1 Fabrication of flexible OFET

• *Fabrication process*

The fabrication processes of our transistors are presented in figure 4.1. It mainly includes the flowing steps:

- Deposition of 2 μm thick Paylene C on silicon, glass and kapton as the substrate.
- Evaporation of 50 nm gold as the gate electrode.
- Spin-coating PMMA (AR-P 67904 type, 5% PMMA-950 K, soluble in ethyl lactate solvent) by setting the parameters as: velocity of 4000 rpm/min, acceleration of 1000, time of 60 s, curing at 80 °C for 30 min. The thickness was measured by profilometry with ~150 nm.

- Deposition of PC with thin thickness (50 nm, 100 nm, 150 nm, 200 nm) on silicon, glass and kapton as the substrate.
- Evaporation of 50 nm gold as the source and drain electrodes by using patterned mask (with channel length 50 µm, 100 µm, 150 µm, channel width 2000 µm, 5000 µm, 1 cm)
- Deposition of pentacene thin films. 30 nm thick pentacene was deposited by using a thermal evaporator at a deposition rate of 0.1 Å /s, under 2×10^{-6} Torr atmosphere and at a room temperature.

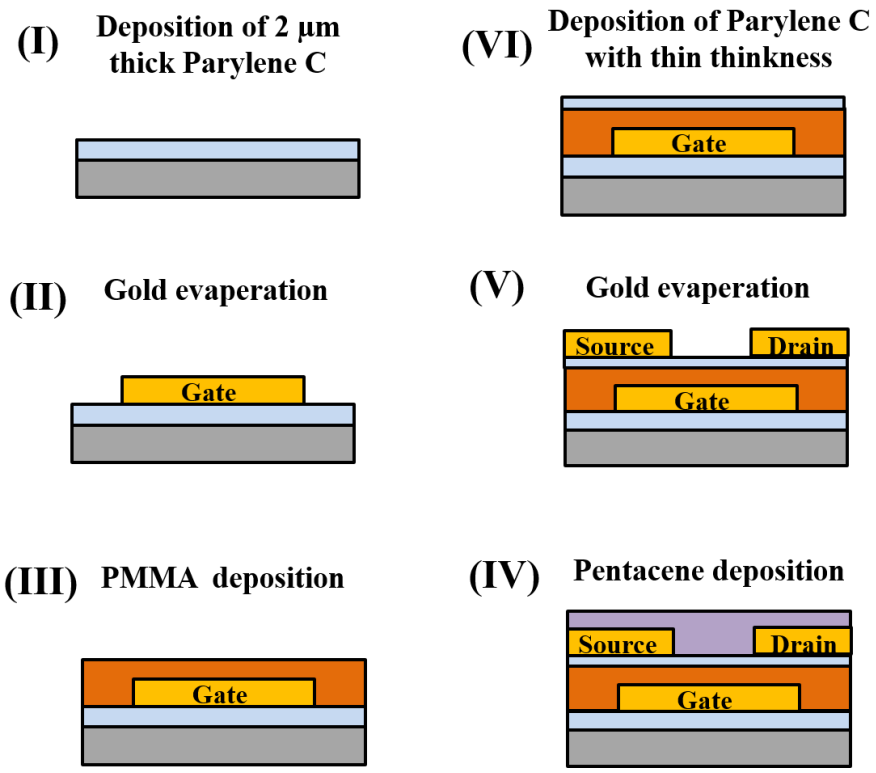

Figure 4.1 The schematic diagram process to fabricate the transistor samples by using Paylene C and PMMA as the gate dielectric layers.

Some of the important informations that involved in the fabrication of the flexible transistors are described below.

• *Synthesis of Parylene C*

The PC was deposited by using a deposition machine of parylene Comelec C20S type. The process of the deposition is a synthetic path for polymer formation, at the same time

it belongs to the category of chemical vapor deposition (CVD), as such, it yields products in a form of conformal solid films depositing at any surface exposed [23]. Figure 4.2 shows Schematic representation of the deposition process of PC with the respective chemical reactions. The dimer pyrolyze at a temperature of 670 °C involves a monomer molecule in its diradical triplet first excited state and then deposit on the surface of the substrate at room temperature. The most unusual feature of the parylene process is the polymerization mechanism compared to the conventional CVD process. A natural consequence of this mechanism is the extraordinary purity of parylene coatings and deposited on the substrate at room temperature, a property of great importance in electronic applications [23].

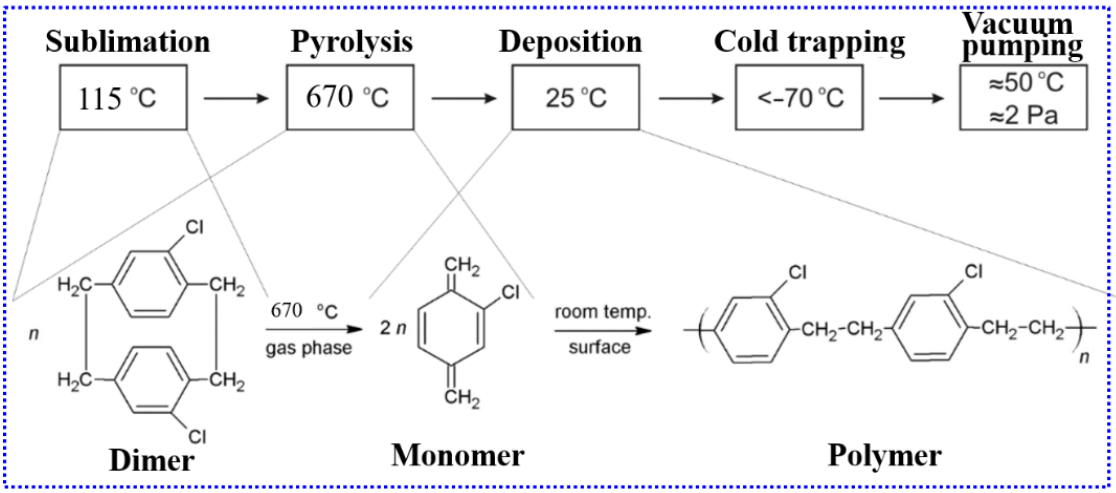

Figure 4.2 Schematic representation of the deposition process of PC with the respective chemical reactions [24].

• *Substrates*

In this chapter, three kinds of adhesion substrates were used for the OFET devices, and 2 μm of PC was deposited on the adhesion substrates first. In attempt to analyze the properties of the PMMA and PC dielectrics easily, the rigid substrates of silicon and glass were used as the references. Then, the polymide film kapton sheet was selected as the flexible substrate. The image of commercial version of kapton and its monomer formulation is presented in figure 4.3. Among the frequently-used flexile substrates, kapton is a polyimide film developed by DuPont in the late 1960s with thermal stability across a wide range of temperatures, from −269 to +400 °C, melting temperature of 410 °C, and high resistivity (10^{17} Ω•cm) that is preferable to be used in the kinds of electric devices, as the thermal property is a crucial

parameter to be considered by engineers during the future fabrication process, for example, to obtain miniaturized flexible integrated circuit combined with lithography technique.

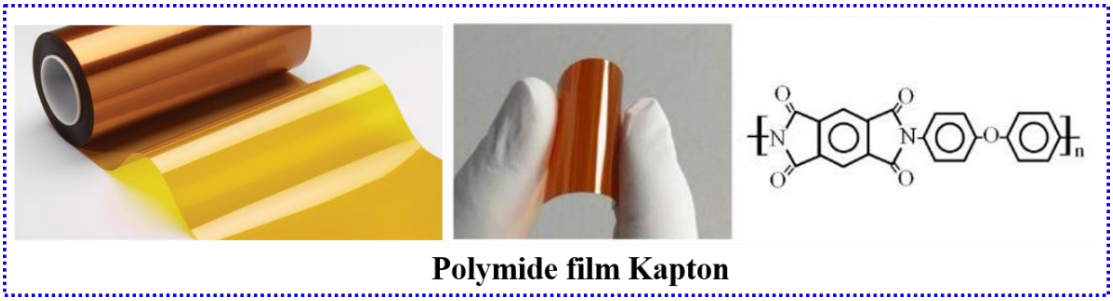

Figure 4.3 Image of the kapton sheet and the mononmer formulation.

The configuration of the pentacene based flexible OFET and the optical images of the transistor samples that fabricated on glass, silicon, and kapton, respectively, are shown in figure 4.4. The transistor devices were fabricated with channel length of 50 µm, 100 µm, and 150 µm, respectively, channel width of 2000 µm, 5000 µm, and 1cm, respectively.

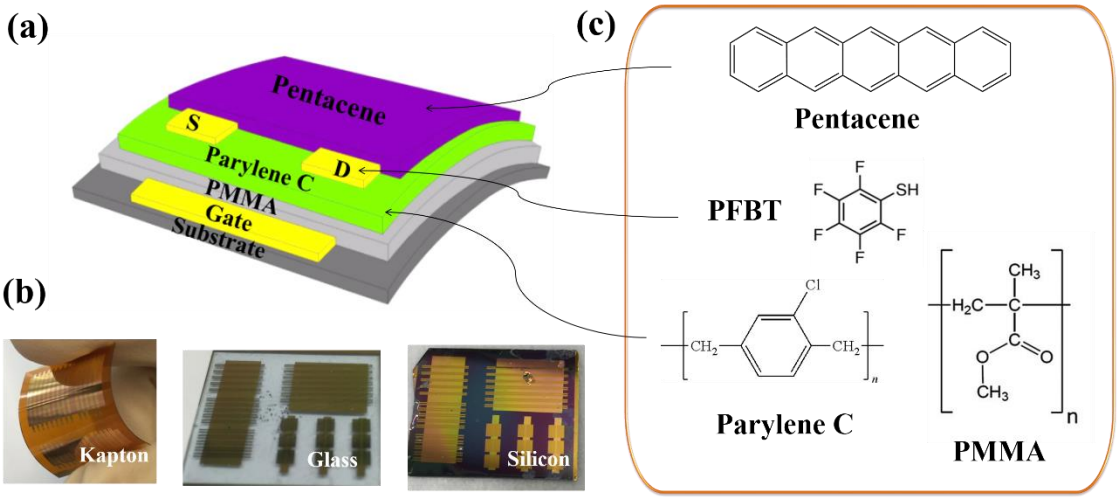

Figure 4.4 (a) The Configuration of the transistor sample on ultra-flexible PC (2 µm), (b) optical images of transistors on kapton, glass and silicon, (c) molecular Structures involved in the devices.

• *Measurements*

• *SEM*

Figure 4.5 shows the Cross-section SEM images of pentacene films thermally evaporated on bare Au and PFBT modified Au on PC 100 nm/PMMA/PC 2 µm. we can see that

the thickness of pentacene is around 30 nm. After the PFBT modification, the pentacene thin films that shown in figure 4.5 (b) are more ordered and the grains are more average, it indicates that the pentacene layers have a relatively smooth surface, and free of major height variations.

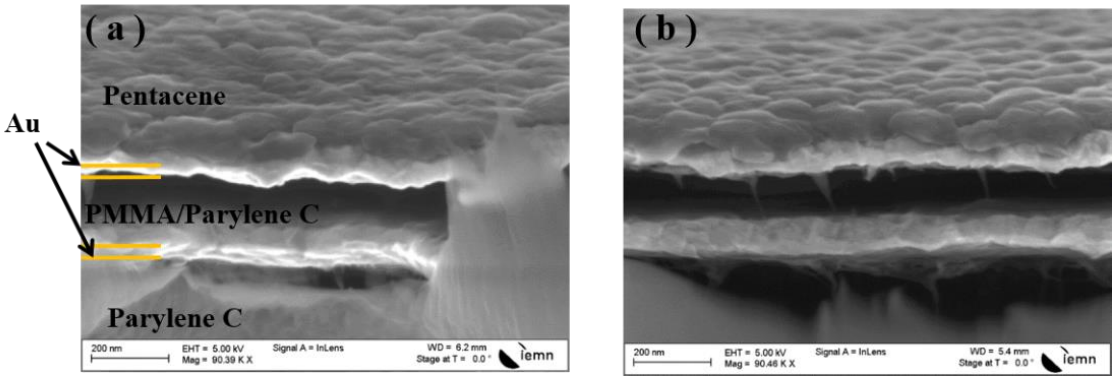

Figure 4.5 The Cross-section SEM images of 30 nm thick pentacene films thermally evaporated on Au/PC/PMMA/PC, (a) Bare-Au, (b) PFBT-modified Au.

• *AFM*

To observe and compare the influence of the substrates on the morphologies of the added organic thin films layers (PC, PMMA, pentacene) that we deposited by CVD, spin-coating, and thermal evaporation methods, we used AFM to characterize the rigid silicon, rigid glass, flexible kapton and the added layers of 2 µm PC and pentacene thin films deposited on these substrates, the morphologies and the values of Root Mean Squared (RMS) roughness are shown in figure 4.6.

The scans were carried out by 5 µm × 5 µm. From the first row of images, we can see that the surface of silicon is very smooth with RMS 0.5 nm, and the kapton shows the relatively higher value of RMS 4.3 nm. However, after the deposition of 2 µm PC thin film, the values of RMS increase and reach to around 4 nm for the three samples compared to the starting substrates, especially for the sample with silicon substrate, the RMS increases a lot, indicating that the RMS may mainly depends on the property of the PC rather than the substrates. Then, as shown in the last row of the images, the addition of pentacene thin films results in a further increase in RMS of 1-2 nm and the pentacene displays individual crystallites of lateral dimensions that observed from the morphologies for the three samples. For comparison, there is not a lot of difference for the active layer of pentacene deposited on the three kinds of substrates after layer by layer deposition. Despite the values of surface roughness are

significantly larger than that of the starting substrates, they are still quite acceptable for completing the device fabrication through deposition of a source–drain gold contact layer.

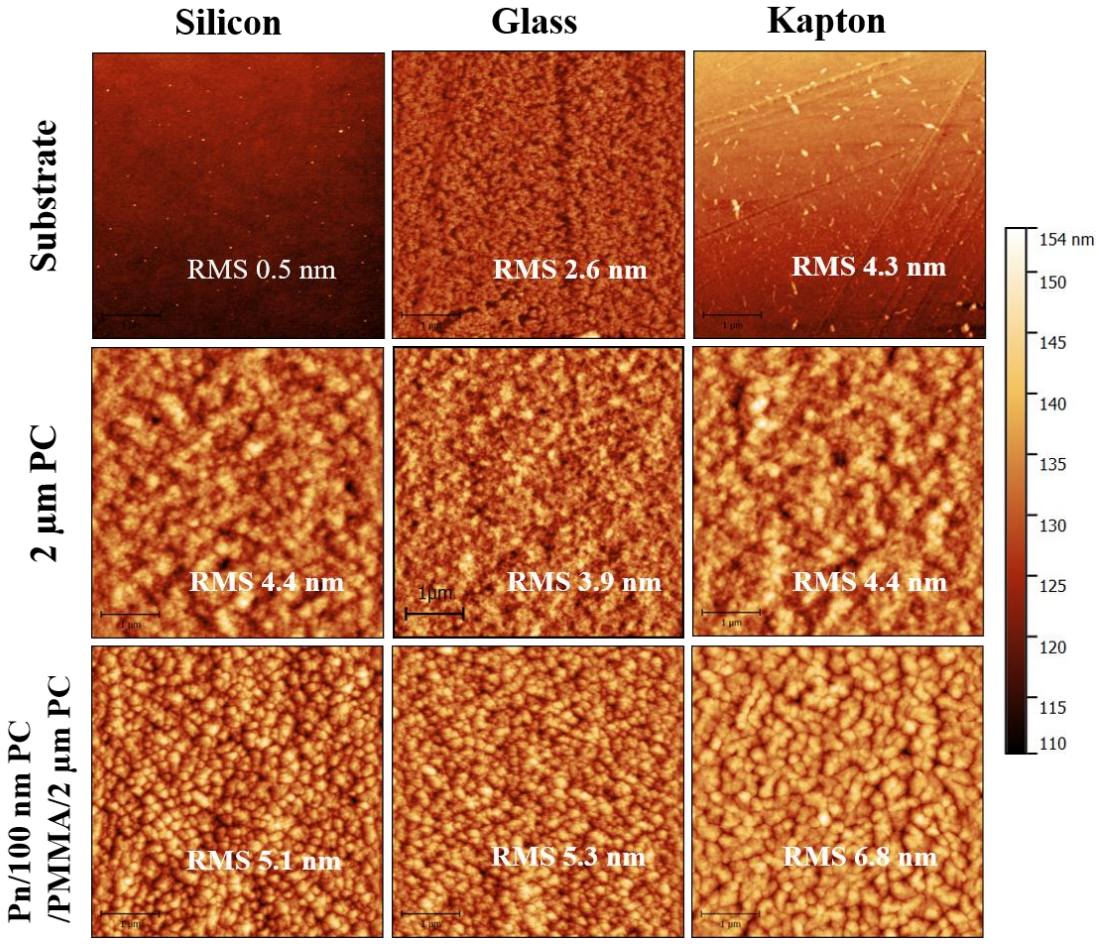

Figure 4.6 AFM scans of rigid silicon, rigid glass, flexible kapton and the thin films deposited on these substrates: 2 µm PC and pentacene (Pn). The vertical color bar indicates the range of surface topology; the average RMS roughness of the starting substrate and after thin film deposition are also indicated.

As we adjusted the thickness of PC dielectric layer to observe the effect of PC on the electrical properties of the our transistor devices, the surface morphologies of the PMMA and different thicknesses of PC thin films were carried out by AFM, the images with 2d and 3d scales are shown in figure 4.7. The thickness of the layers were measured by profilometry. From the AFM images, smooth and compact thin films of PMMA and PC were obtained by spin coating and CVD, respectively. The results revealed that there were no pits and pin holes on the surfaces for our thin films of 160 nm PMMA, 200 nm PC, 150 nm PC as well as 100 nm PC. The only topographic features observed is the hillock of about 2~30 nm large and a peak

to valley distance of about 5~10 nm. Thus, they could be effectively used as the gate dielectric layers.

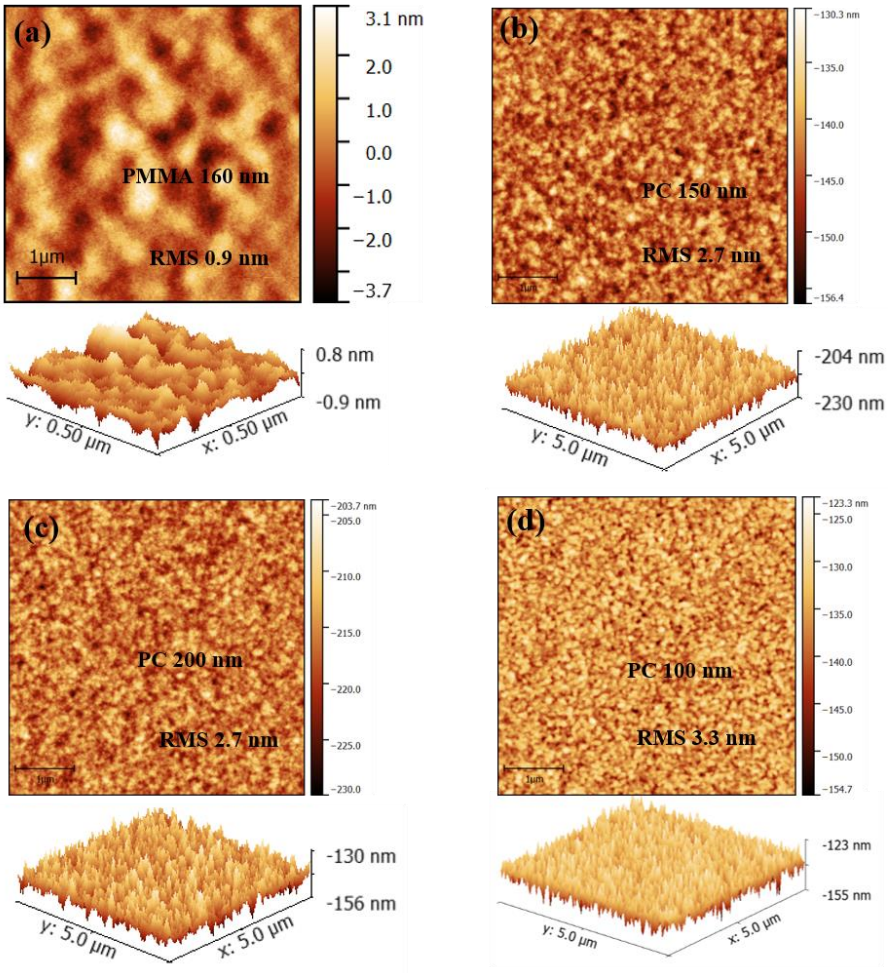

Figure 4.7 AFM scans of (a) PMMA deposited on 2 μm PC/Si by spin coating, PC thin films on Si with thickness of (b) 200 nm, (c) 150 nm and (d) 100 nm.

4.2.2 Fabrication of flexible NFGM

• *Fabrication process*

In this part, for fabricating the flexible NFGM samples, two more steps are needed to be carried out compared to the process of fabricating flexible pentacene transistors, i.e. deposition of Au NPs on the PC/PMMA gate dielectric layers as floating gate, and deposition of a thin layer of Hydrogen Silsesquioxane (HSQ) by using spin-coating as the tunneling dielectric layer.

• *Deposition of Au NPs*

Importantly, here, the method to deposit Au NPs on PC/PMMA dielectric layers is different from the way described in the part 3.2.1. Because of the easier aggregation of Au NPs on the surface of polymer by using solution deposition ways and to avoid the dissolve or damage of organic dielectrics in the solvents such as methanol, ethanol or piranha solution, the sample with structure PC/PMMA/PC(2 μm)/substrate was first directly oxidized by ultraviolet-ozone (UV-zone) treatment to get hydroxyl groups and then placed 3 hours in the presence of vapors of freshly distilled APTS (≥98%, 0.946 g/mL at 25 °C, purchased from SIGMA-ALDRICH) in laboratory glassware at 0.2 Torr to form a positively charged NH_2/NH_3^+-terminated SAM, and then dipped into the negatively charged citrate-reduced Au NPs solution (the average diameter of the Au NPs is 10 nm) for more than 2 h to obtain the floating gate layer of Au NPs matrix. The Au NPs starting solution which supplied by Aldrich was diluted 100 times in toluene solvent. Again, NP concentration in the solution and duration of the reaction were changed to adjust the NP density on the surface. The basic strategy to deposit the Au NPs matrix on the PC surface is the same as schematized in figure 3.2.

• *Deposition of HSQ dielectric layer*

Hydrogen Silsesquioxane (HSQ) was used as the tunneling layer in this flexible memory devices. It is class of inorganic compounds with the chemical formula $[HSiO_{3/2}]n$ and with high stability [25].

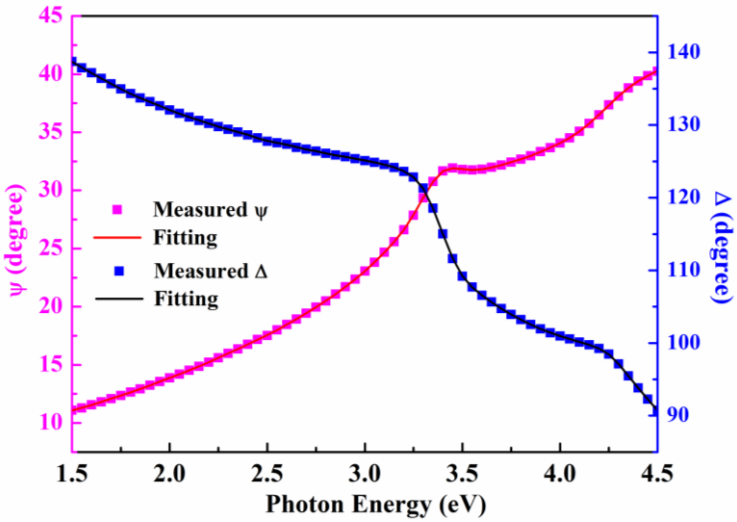

Figure 4.8 Ellipsometer measurement and data fitting for HSQ thickness.

After the construction of the double floating gates, a ~19 nm thick HSQ dielectric layer was deposited by spin coating and annealing at 90 °C for 30 min to form the tunneling oxide. The thickness of HSQ was verified by spectroscopic ellipsometer measurement. As shown in figure 4.8, the Ψ and Δ describe the change in polarization that occurs when the measurement beam interacts with a sample surface causing a change in the outgoing polarization. With the beast fitting, the thickness of HSQ was found to be ~19 nm.

• *Configuration of the NFGM sample on ultra-flexible PC*

After deposition of HSQ, the 50 nm thick source and drain electrodes were fabricated by evaporation with the same mask of our flexible OFET, and 30 nm thick pentacene was deposited by thermal evaporation. The Configuration of the NFGM sample on ultra-flexible PC (2 µm) is depicted in figure 4.9.

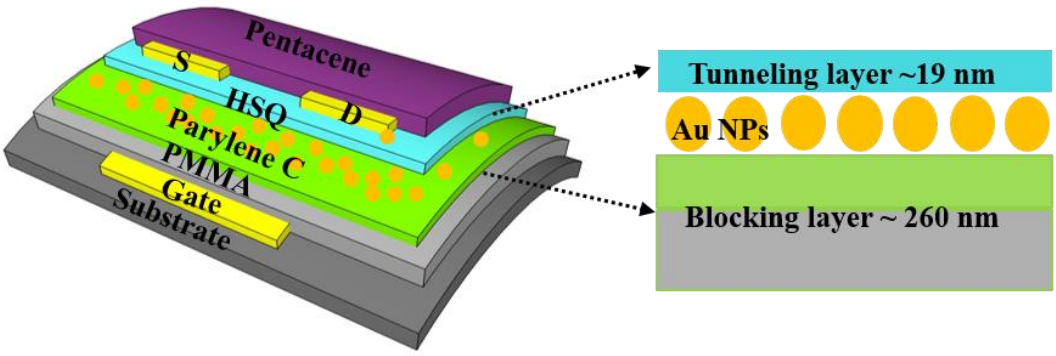

Figure 4.9 The Configuration of the NFGM sample on ultra-flexible PC(2 µm).

• *Measurements*

• *Contact angle*

To deposit Au NPs on the surface of PC dielectric layers, the sample was oxidized by UV-zone treatment to get hydroxyl groups. Figure 4.10 shows the images of water contact-angles and the curves relationship of average contact-angles with different UV-ozone treating periods on clean PC surfaces. No UV-ozone treated PC surface shows a water contact-angle of 92.8°, the surface without UV-ozone treatment hydrophobicity. As the UV-ozone treatment periods increase from zero to 10 minutes, the contact angle decreases from 92.8° to 44.8°. The intrinsic wetting threshold for water is 65° [26, 27], which is also the boundary between hydrophilicity and hydrophobicity, therefore, the surface is assessed as without sufficient hydroxyl groups. Furthermore, a super hydrophilic surface is obtained with a contact angle near

zero. Here, when the UV-ozone treatment period is more than 30 min, the contact angle decreases below to 25.4° and even reaches to 6.6° when the UV-ozone treatment period is 90 min. It is clear that the UV-ozone treatment period has strong effects on the surface energy and surface wettability, and in our experiments, we can see that the surface of PC could obtain sufficient hydroxyl groups (the contact angle decreases below to 30°) after the UV-ozone treatment period is more than 30 min.

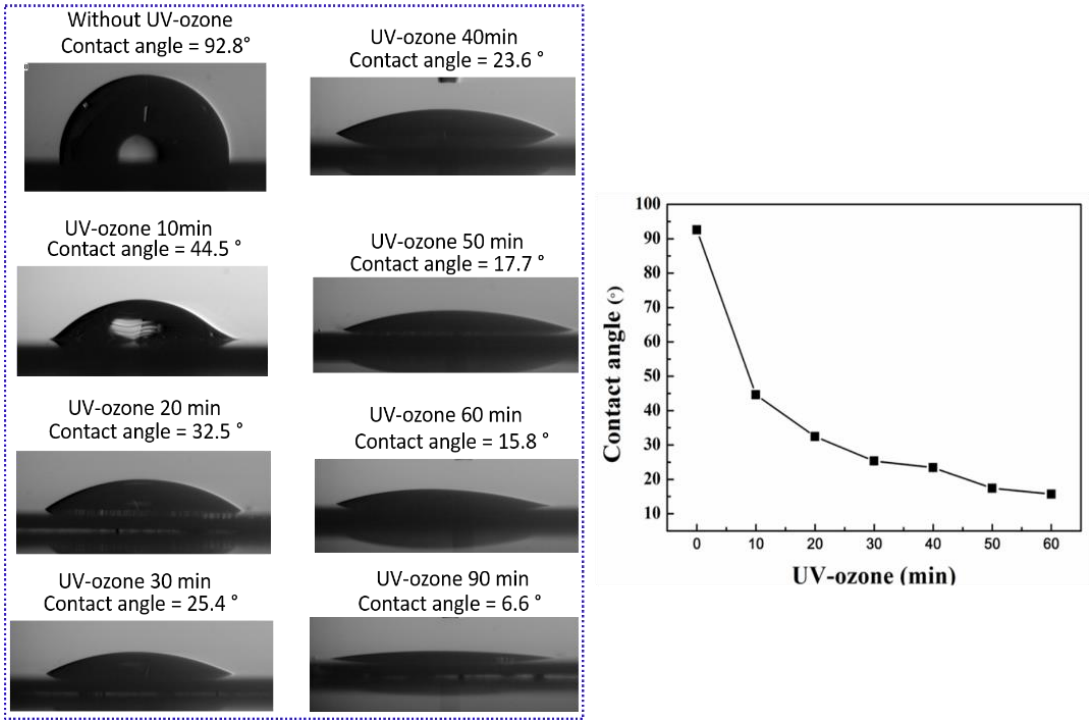

Figure 4.10 The microscope images of contact angle measurements the curves relationship of average contact-angles for the different PC surfaces with different UV-ozone treatment times.

• *SEM*

The deposition of Au NPs on the surface of PC was characterized by SEM, as shown in figure 4.21. At beginning, we used the same way that described in part 3.2.1 to deposit the Au NPs, however, the Au NPs were always aggregated, that we did not find any memory characteristics because of the short circuit between source and drain electrodes. The SEM images of the aggregated Au NPs are shown in figure 4.11 (a) and (b). Thus, we changed another way to deposit the Au NPs, we prepared the APTS by putting the sample in the presence of vapors of freshly distilled APTS in a laboratory glassware and then cleaned well before immersed in the solution of Au NPs. From the SEM images that depicted in figure 4.21 (c) and (d), we can see that he Au NPs are uniform in size and some aggregates is observed in the zoom

images with 20 nm scale. The density of NPs was found ~2.5×10^{11} NP/cm^2 and the radium of the Au NP is around 10 nm.

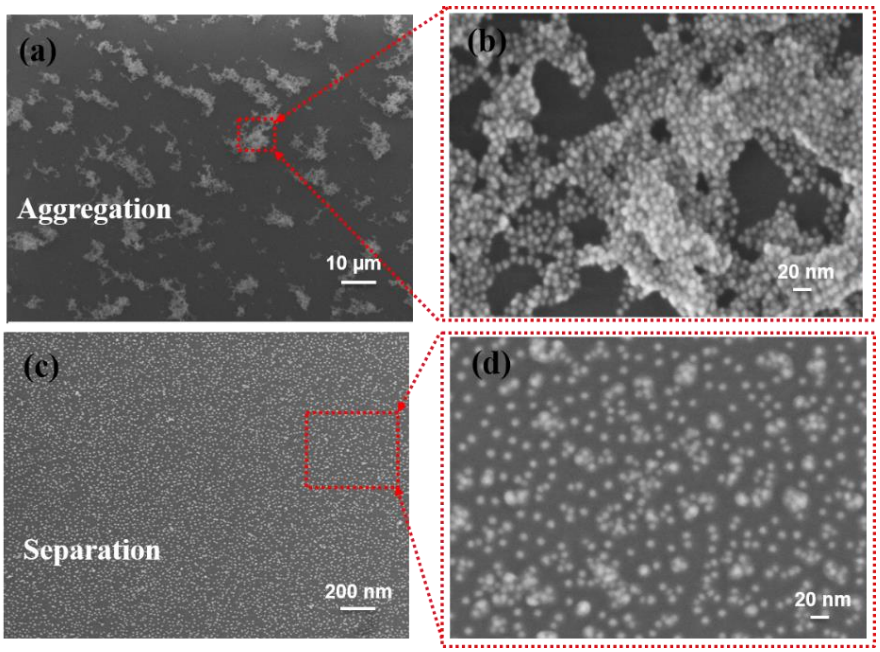

Figure 4.11 The SEM of the Au NP deposited on functionalized PC surfaces. (a) Examples of aggregation NPs, (b) zoom of part of (a), (c) dispersion NPs, (d) zoom of part of (d).

• *AFM*

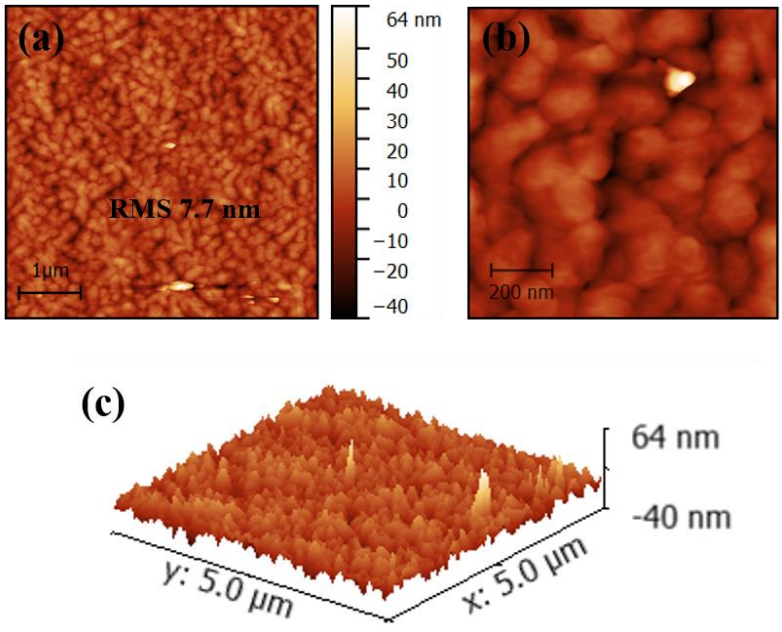

Figure 4.12 (a) AFM scans of pentacene thin films fabricated on kapton substrate with NFGM structure, (b) zoom of part of (a), (c) 3d AFM images.

Figure 4.12 shows the AFM 2d and 3d morphologies of pentacene thin films fabricated on kapton substrate with NFGM structure. In figure 4.12(a), the scans were carried out by 5 μm × 5 μm. we can see that the pentacene thin films show polycrystalline dendritic islands shape with a RMS of 7.7 nm with. The polycrystalline dendritic islands shape could be clear seen in figure 4.12 (b) with zoom scan of 1 μm×1 μm. In addition, the 30 nm thick pentacene thin films were measured by profilometry.

4.3 Characterization of pentacene based OFET

4.3.1 Electrical characteristics

Based on the experiments results of chapter 2 and chapter 3, we also used PFBT to modify our flexible transistor devices. And for comparison and easy to study the properties of the PC/PMMA bilayer polymer dielectrics, the ultra-flexible transistors fabricated on 2 μm PC were deposited on silicon, glass and kapton substrates and the thickness of dielectric layer of PC were adjusted as 50 nm, 100 nm, 150 nm, 200 nm, respectively. Thus, there were totally nine kinds of transistor samples were fabricated.

• *Electrical characteristics of OFET by using single PC or PMMA dielectric*

In this part, before using PC/PMMA bilayer as the gate dielectrics, single layer of PC or PMMA was deposited as the gate dielectric. The structure of the transistors are:

- Pentacene(30 nm)/Au(Source and Drain)/PMMA(350 nm)/Si(Gate)
- Pentacene(30 nm)/Au(Source and Drain)/PC(300 nm)/Si(Gate)

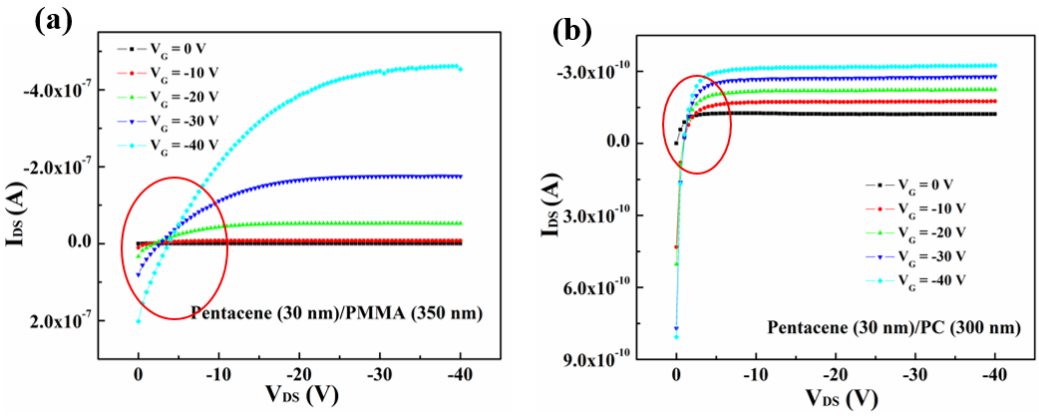

Figure 4.13 Represents of output characteristics of the transistor devices with the same configuration of figure 4.5 by using (a) single PMMA and (b) single PC layer as gate dielectric.

However, when we carried out the transfer and output characteristics, the leakage currents were found very large for these samples with single dielectric layer, as a consequence, these transistor devices performed very poor characteristics, for example, the output characteristics are shown in figure 4.13. Thus, we used PC/PMMA conjugated bilayer as the gate dielectrics because inserting PC polymer dielectric layer in OFET has been reported to effectively enhance the electrical properties of the transistor devices [14, 26].

• *Electrical characteristics of OFET by using PC/PMMA bilayer dielectrics and the effects of the substrate*

Here, all the samples fabricated by using PC/PMMA bilayer dielectrics in our experiments successfully work as transistor devices, and the electrical properties has been measured under the same circumstance conditions that descripted in chapter 2 and chapter 3. To compare the characteristics of the transistor samples fabricated on different substrates, the results of the sample with exactly same structures (same channel width and length, W/L=100) were performed. The drain current-gate voltage (I_{DS} -V_{GS}) transfer curves are depicted in figure 4.14, where logI_{DS} and $I_{DS}^{1/2}$ is plotted versus V_{GS} at a fixed V_{DS} value of -20 V for all the samples, V_{GS} is running from +10 V to – 20 V.

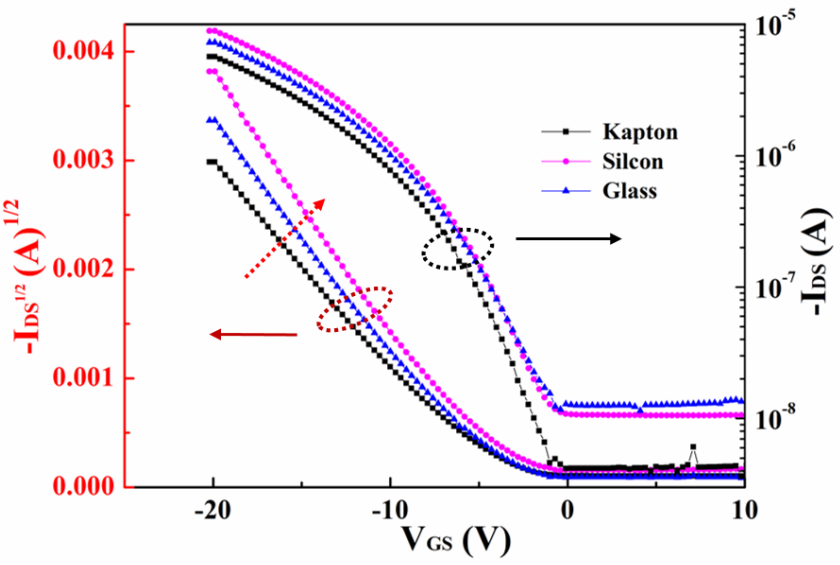

Figure 4.14 The typical transfer curves of the structure of pentacene/PC/PMMA/2 μm PC on kapton, silicon, and glass substrates, respectively, with the gate sweep voltage ranges (from 10 V to -20) at V_{DS}=-20 V.

As expected from the conventional OFET operation, the currents flow through the OFETs for the three kinds of sample are strongly influenced by the gate voltage V_{GS}. All of the transfer characteristics of the OFETs prepared here display a subthreshold regime between the

switch on voltage and the threshold voltage. Compared with the transistor that fabricated by using inorganic SiO_2 as the dielectric layer in chapter 2, the gate operation voltages is decreased. And compared the three samples, the I_{DS} current is relatively better for the device fabricated on silicon substrate, which may due to the more smooth surface of the silicon substrate. The electrical parameters like mobility, threshold voltage, and current on/off ratio were extracted and calculated, which are summarized and presented in table 4-1 for better comparison.

To clearly observe the electrical characteristic of our flexible transistor, figure 4.15 shows the typical transfer curves of the structure of pentacene/PC/PMMA/2 µm PC on kapton with the gate sweep voltage ranges (from 20 V to -20 V to 20 V) at V_{DS}=-20 V. Compared with the transfer curves of the conventional pentacene/SiO_2/Si transistor, the hysteresis (the difference in transfer curves when sweeping V_{GS} back and forth), that is detrimental for the conception of OFETs based circuits, completely disappeared in the case of OFET by using PC/PMMA dielectrics. Which indicates that the charge trapping/detrapping effects at the pentacene/PC dielectric interface are significantly attenuated by using polymeric layer [16, 27]. In further, the transfer performance is stable and the leakage current I_G is low.

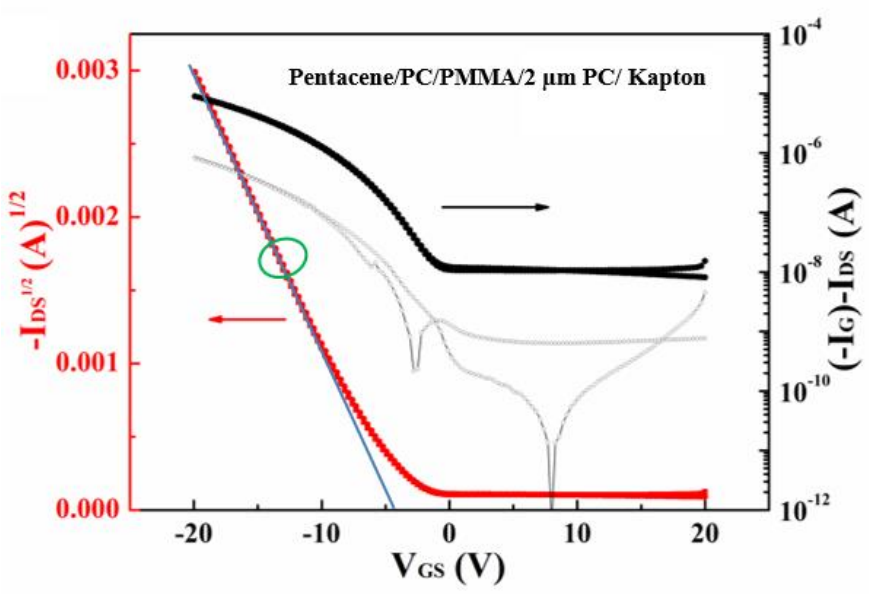

Figure 4.15 The typical transfer curves of the structure of pentacene/PC/PMMA/2 µm PC on kapton with the gate sweep voltage ranges (20 V to -20 V to 20 V) at V_{DS} = -20 V.

The output characteristics for the transistors that fabricated on kapton, silicon, and glass substrates, respectively, are performed in figure 4.16. The output curves for the three kinds of samples typically show good saturation at higher V_{DS} and a clear linear regime at low V_{DS} with

maximum V_{DS} operation voltage of 20 V. On the other hand, the required V_{GS} operating voltage is about -5 V to reach an on-state I_{DS} of 1 μA for the three kinds of samples.

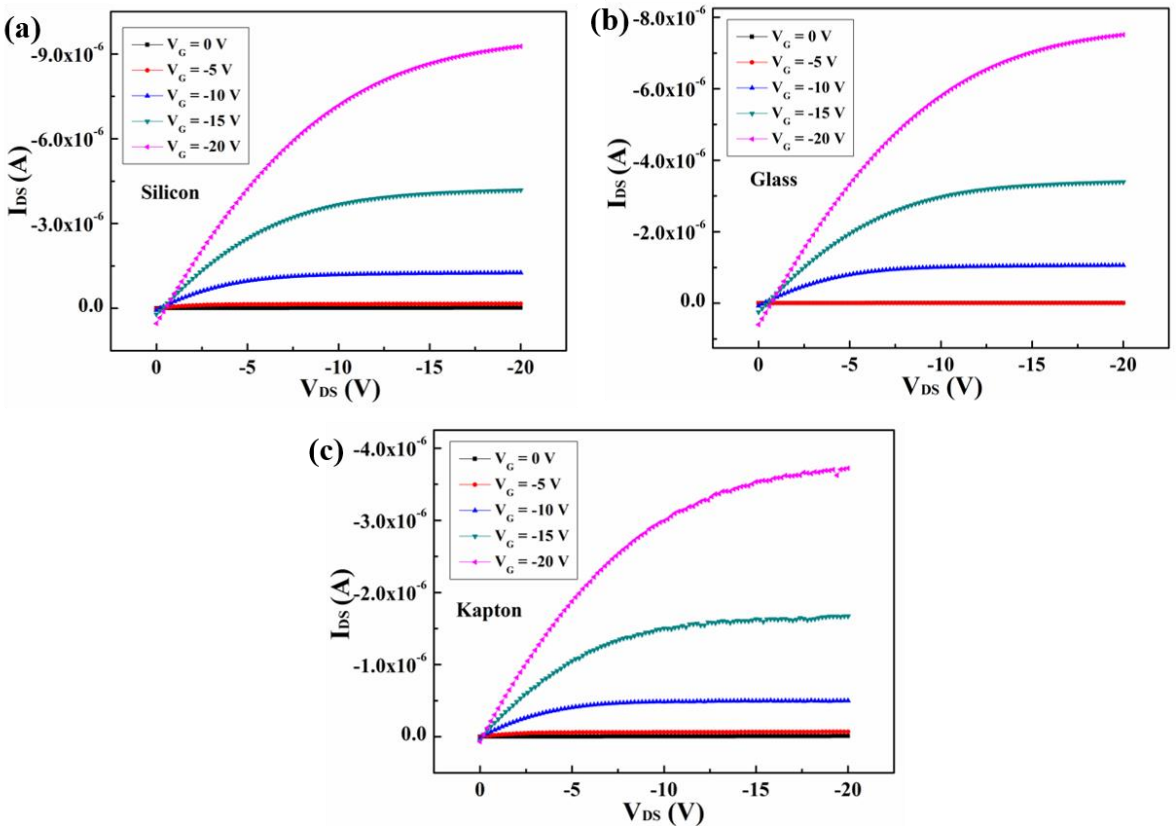

Figure 4.16 The I_{DS} - V_{GS} output curves of different the structure of pentacene/PC/PMMA/2 μm PC on (a) silicon, (b) glass and (c) kapton substrates, respectively.

• *Electrical characteristics of the structure of pentacene/PC/PMMA/2 μm PC/kapton and the effects PC dielectric*

For investigation of the effects of dielectric layers on the performance of the flexible transistor devices, we adjusted the thickness of PC and carried out the electrical properties. Figure 4.17 shows the transfer curves of the structure of pentacene/PC/160 nm PMMA/2 μm PC on kapton with thickness of PC ranges from 50 nm to 200 nm and with/without PFBT SAM treatment. The logI_{DS} and $I_{DS}^{1/2}$ are plotted versus V_{GS} are presented in figure 4.17 (a) and (b), respectively. As we can see, the I_{DS} current is increased with the decrease of the thickness of PC dielectric layer. When the PC decreased to 100 nm, the current on/off ratio reaches to 6.8×10^5, the threshold voltage is -4 V. The sample fabricated with PC 50 nm was not found electrical properties, which may be induced by the low breakdown voltage because of the thin dielectric layer of 160 nm plus 50 nm PC. And with PFBT modification, the I_{DS} current is

increased but not as a lot of improvement as in chapter 2 that the transistor devices were fabricated on silicon substrate, this is maybe because of the kapton flexible substrate was not stretched well in the solution of PFBT.

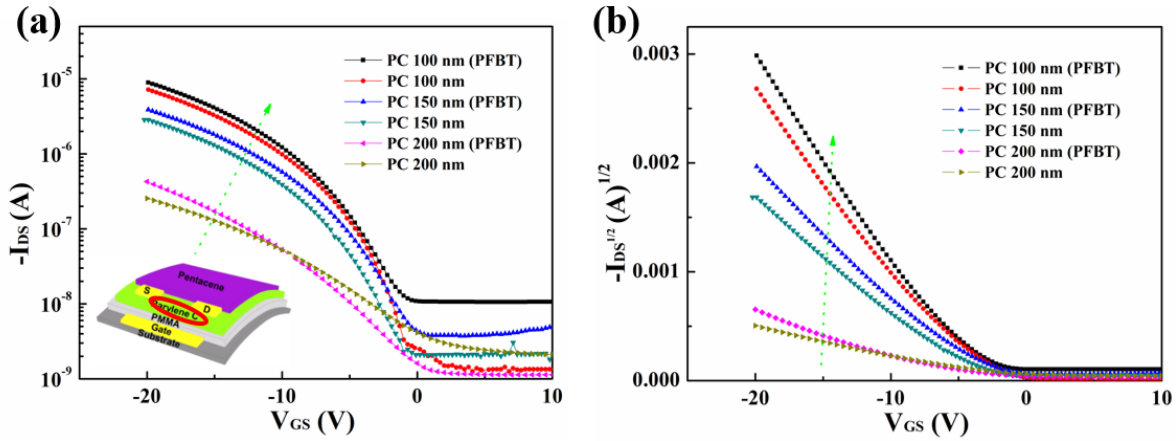

Figure 4.17 The typical transfer curves (a) $\log I_{DS}$-V_{GS} and (b) $I_{DS}^{1/2}$ -V_{GS} of the structure of pentacene/PC/PMMA/2 µm PC on kapton with thickness of PC ranges from 50 nm to 200 nm and with/without PFBT SAM treatment. The gate sweep voltage ranges (20 V to -20 V to 20 V) at V_{DS} = -20 V.

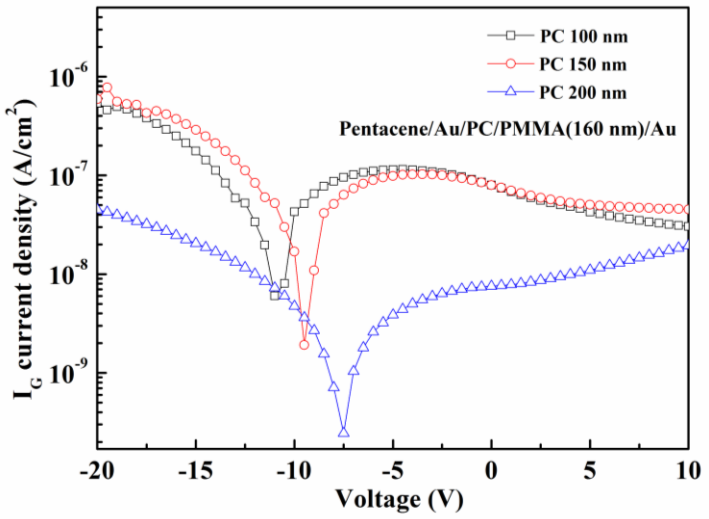

Figure 4.18 The leakage current density of pentacene/PC/PMMA/2 µm PC on kapton with thickness of PC ranges from 50 nm to 200 nm.

A key requirement for a polymer gate dielectric is the ability to form a thin film with good dielectric properties [8, 13]. The thickness of the gate dielectric determines directly the operating voltage of the FET. Figure 4.18 shows the gate leakage current versus the gate bias voltage of the pentacene/Au/PC/PMMA /Au (metal-insulator-semiconductor) MIS with different thickness of PC on ranging from -20 V to 10 V. The leakage current density of the

100 nm and 150 nm PC dielectric layer is 8 μA/cm^2 and 7.5 μA/cm^2 at -20 V, respectively. The leakage current density of the bilayer film was decreased to 0.6 μA/cm^2 at -20 V by increasing the thickness of PC to 200 nm. This small leakage current in the bilayer dielectrics with PC (200)/PMMA (160nm) indicates that the film thickness is slightly increased to 50 nm, effectively reducing the gate leakage current.

Interface traps and gate dielectric surface roughness are important parameters which can contribute to variations in the threshold voltage and mobility FET [28, 29]. In figure 4.6 and figure 4.7, we carried out and compared the surface morphologies of thin films layers. Here, the capacitance-voltage (C-V) and capacitance-frequency (C-F) characteristics of MIS structures have been measured to investigate interface properties, the analysis of C-V and C-F could be used to control threshold voltage and carrier field-effect mobility. MIS capacitors are the two-terminal counterparts of thin film transistors sharing the same basic layer structure. Therefore, to fully understand different physical phenomena in the bulk and at insulator/semiconductor interfaces, a systematic analysis of pentacene/Au/PC/PMMA /Au MIS capacitors has been performed. Depending on the sign of the gate voltage the MIS capacitor can be in one of the three states: accumulation, depletion, and inversion regimes. The total capacitance of the MIS structure can be described by a series connection of two capacitors: the capacitance of the insulator and the capacitance of the semiconductor layer. The total capacitance is given by [31].

$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{Cs} \tag{4-1}$$

where Cs is the semiconductor capacitance and Ci is the insulator capacitance which is given by:

$$C_i = \frac{\varepsilon_0 \varepsilon_{eff}}{t_i} \bullet \mathrm{A} \tag{4-2}$$

where A is the capacitor area, ε_0 is the vacuum permittivity, ε_{eff} is the bilayer insulator (PC and PMMA) dielectric constant and t_i is the insulator thickness (the sum of thickness of PC and PMMA). In accumulation, $Cs \gg Ci$ and the total capacitance is approximately equal to the insulator capacitance.

Figure 4.19 shows the C-V characteristics of the pentacene/Au/PC/PMMA /Au with various PC thickness. The measurements were performed with a small alternating current (AC) signal 20 mV at a frequency of 1 KHz on top of a preselected directing current (DC) voltage. The voltage was swept forward from negative to positive. The accumulation, depletion and

inversion regions are observed for all the MIS samples (the inset of figure 4.19 shows the C-V of PC with 200 nm for better investigation), with the decrease in capacitance in the depletion region due to the variable depletion capacitance of the pentacene active semiconductor layer in series with the PC/PMMA bilayer dielectrics capacitance. At negative voltage of –20 V, it shows maximum capacitance with accumulation of holes at the polymer – metal interface. The capacitance of the accumulation region depends primarily on the PC/PMMA thickness and permittivity, whereas the capacitance in the depletion region is also dependent on the properties of the pentacene semiconductor and interface charge density at the interface with PC. Compared with the three different PC thickness of MIS, the capacitance is improved with the decrease of PC thickness and reaches to 14.5 nF/cm^2 when PC is 100 nm. The dielectric constant ε_{eff} of the bilayer polymer films could be obtained from this capacitance and equation (4-2), thus, the dielectric constants for bilayer dielectrics of PC (100 nm)/PMMA, PC (150 nm)/PMMA, PC (200 nm)/PMMA were calculated to be 3.56, 3.25, and 3.13, respectively. In addition, the flat band voltage (V_{FB}) is -3 V when PC is 100 nm, it shifted in the negative direction when the thickness of PC is increased and increased up to -10 V, which indicates that more positive fixed charges exist in the thicker PC/PMMA bilayer polymer film [32].

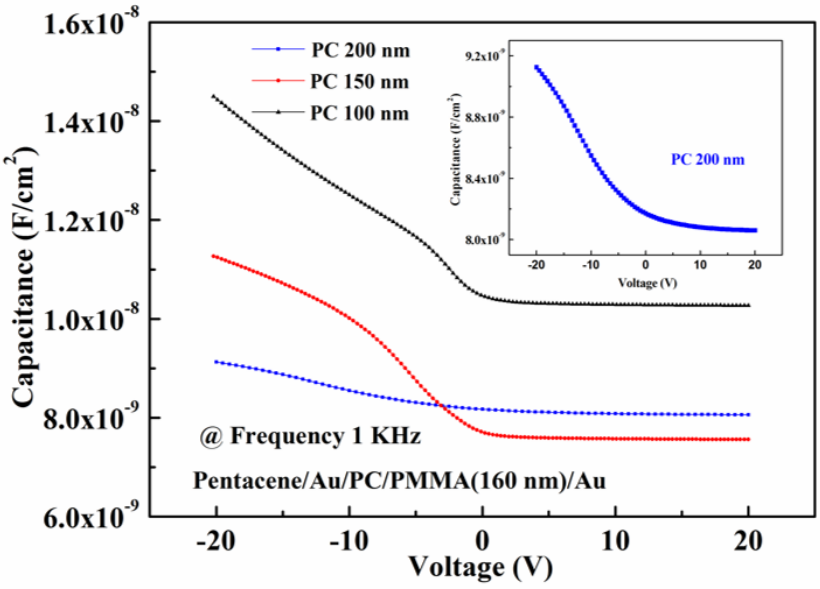

Figure 4.19 The C-V curves of pentacene/PC/PMMA/2 μm PC on kapton with thickness of PC ranges from 100 nm to 200 nm at frequency of 1 KHz.

Figure 4.20 shows the C-F characteristics of the pentacene/Au/PC/PMMA /Au with various PC thickness at AC voltage of 20 mV and DC voltage of 0 V. From the C-F curves, we can see that the three samples all exhibit frequency independent behaviors and it also

presents that the capacitance is improved with the decrease of PC thickness. The dispersion of the capacitance at the low frequency of 20 Hz and high frequency of 10^6 Hz may be due to the critical edge of the frequency measurements range.

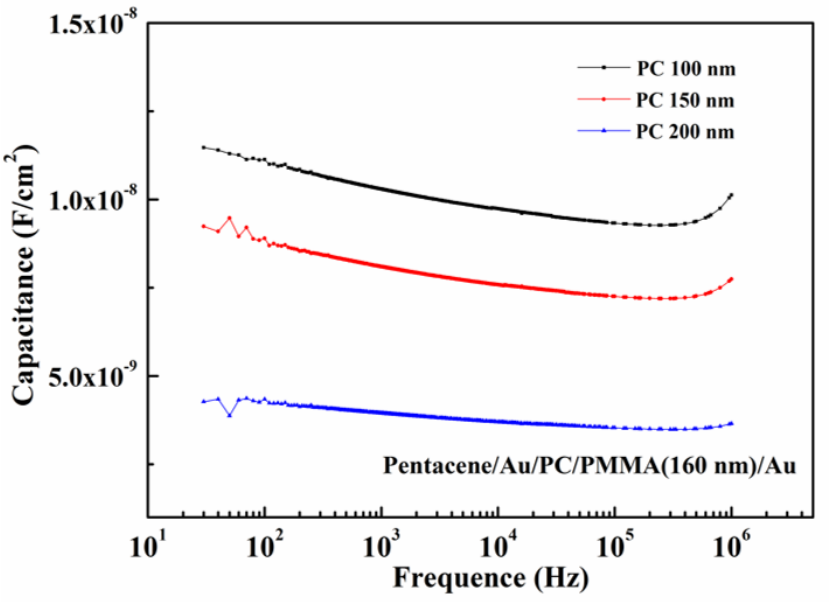

Figure 4.20 The C-F curves of pentacene/PC/PMMA/2 µm PC on kapton with thickness of PC ranges from 100 nm to 200 nm.

The frequency dependence of the measured C-V curves of pentacene/100nm PC /PMMA/2 µm PC on kapton is shown in figure 4.21 (a). The frequency ranges from 100 Hz to 200 KHz. As we can see, the values of capacitance increase with decreasing frequency, the accumulation, depletion and inversion regions are clearly observed with relatively low frequencies. The capacitance decreases in accumulation regime when high frequency is used, while the capacitance in depletion regime remains almost the same. The frequency dependence of C-V characteristics originates from different responses of trapped and mobile charges between the interface region and bulk of the semiconductor [31]. This difference in response to the applied signal is directly related to the different carrier-lifetimes and carrier-generation rates of disordered organic semiconductors [33]. The shallow states respond to high frequency voltages whereas deep and localized states do not respond to those voltages at high frequency. Lower values of the capacitance at higher frequencies indicate that mobile charges do not respond at those high frequencies, behaving similar to fixed or trapped charges. Typically, the capacitance in the accumulation regime has shown a rapid decrease, which indicates that the response of the holes to the gate signal decreases rapidly. In contrast, the depletion capacitance remains almost constant. Frequency dispersion in the transition region between the maximum

and minimum capacitances is due to the presence of interface traps between dielectrics and pentacene. For example, Lindner et al. [34] have shown in their simulation work on MIS C-V characteristics, interface traps can have significant effect on the C-V characteristics. The maximum number of interface traps present can be calculated using Eq. (4-3); assuming that the densities of deep bulk states and interface states are independent of energy [37].

$$N_{ss}^{max} = \left[\frac{S \cdot \log(e)}{KT/q} - 1\right]\frac{C_i}{q} \tag{4-3}$$

where N_{ss}^{max} is the maximum number of interface states, S is subthreshold swing which is calculated by equation (1-1), k is the Boltzmann constant, T is the absolute temperature and q is the electronic charge. Table 4-1 gives all the electrical parameters of the pentacene FETs that fabricated in this chapter. Minimizing the number of charge carrier traps is also important for any OFET, as traps can lead to lower device currents and shifts in the turn-on voltage [15].

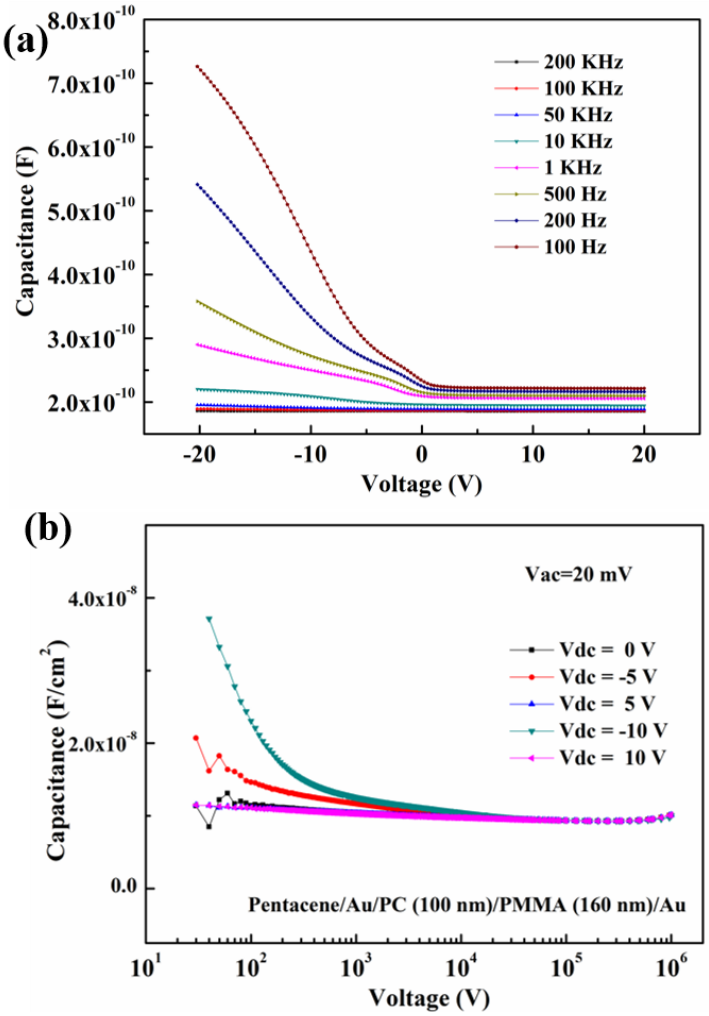

Figure 4.21 (a) The C-V curves with frequency dispersion characteristics and (b) the C-F curves at different bias voltages of pentacene/100nmPC/PMMA/2 µm PC on kapton.

Figure 4.21(b) shows the C-F characteristics (frequency sweep from 20 Hz to 10^6 Hz) of the pentacene/100nm PC /PMMA/2 µm PC on kapton at AC voltage of 20 mV and various DC voltages. At the frequency ranges from 200 Hz to 10^6 Hz, the capacitance remains stable, and the capacitance show frequency independent behaviors. On the other hand, with the change of DC voltages, the capacitances are remains at the same stage. The dispersion of the capacitance at the low frequency of 20 Hz may be due to the critical edge of the frequency measurements range.

• *Electrical characteristics of structure of pentacene/PC/PMMA/2 µm PC/kapton under binding tests*

The flexible transistor with structure of pentacene/PC/PMMA/2 µm PC/kapton is measured under bending tests with radius of 1.4 cm, the transfer and output characteristics are shown in figure 4.22.

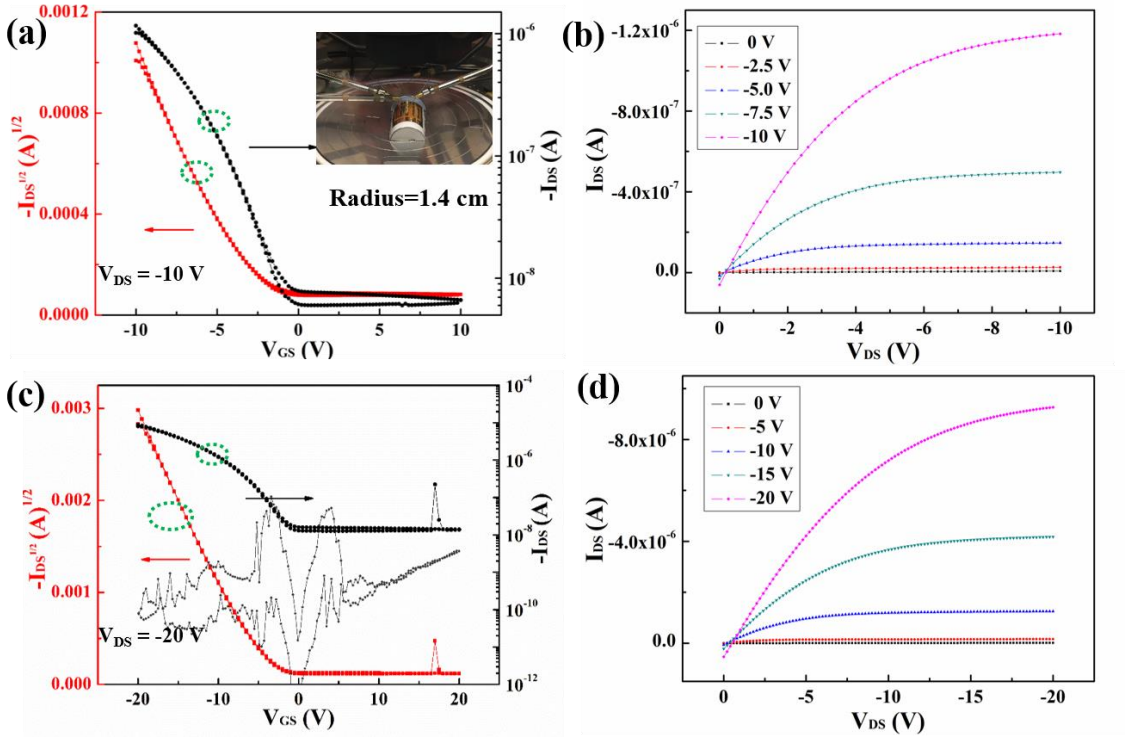

Figure 4.22 The typical transfer and output characteristics of pentacene/PC/PMMA/2 µm PC on kapton under binding test with radius of 1.4 cm.

The results measured with the various gate sweep voltage ranges (from +10 V to -10 V, +20 V to -20 V) show that there is no hysteresis in the case of OFET under binding tests by using PC/PMMA dielectrics, indicating that the charge trapping/detrapping effects at the

pentacene/PC dielectric interface are significantly attenuated. In further, the transfer performance is stable and the output curves for the three sweep voltage ranges typically show good saturation a clear linear regime. The saturation mobility is 0.055 $cm^2V^{-1}s^{-1}$, and the leakage current is relatively low. We can see that the I-V behaviors with binding tests obtained the same state characteristics with flat tests.

4.3.2 Extractions of electrical parameters

From the analysis of the characteristics of the all the transistor devices that fabricated in this chapter, the parameters of carrier mobility, threshold voltage, subthreshold swing, on/off current ratio, as well as interface traps were extracted and calculated, the values were summarized in Table 4-1 (every parameter was extracted by the average of 5 devices).

Table 4-1. Summary of the electrical parameters for different pentacene OFETs

Transistor device	Average mobility (maximum) ($cm^2V^{-1}s^{-1}$)	Threshold Voltage (V)	Subthreshold swing (V/decade)	On/off current ratio	Interface state density • 10^{12} ($cm^{-2}\,eV^{-1}$)
S1	0.0015 (0.0026)	-1	0.3	1.5×10^3	3.12
S2	0.0018 (0.0026)	-0.5	1.3	1.6×10^3	3.1
S3	0.0046 (0.006)	-2	0.9	2.5×10^3	2.89
S4	0.0056 (0.006)	-1.5	0.5	3.3×10^3	2.9
S5	0.056 (0.08)	-4	1.2	2.5×10^5	2.85
S6	0.071 (0.15)	-3	1.1	4.5×10^4	2.83
S7	0.075 (0.1)	-3.8	0.8	5.5×10^3	2.81
S8	0.095 (0.23)	-4	0.6	6×10^3	2.8

For predigestion in the table, the transistors samples are marked as following:

• S1: Pentacene/PC(200 nm)/PMMA/PC(2 μm)/Kapton

- S2: Pentacene/PC(200 nm)/PMMA/PC(2 μm)/Kapton with SAM
- S3: Pentacene/PC(150 nm)/PMMA/PC(2 μm)/Kapton
- S4: Pentacene/PC(150 nm)/PMMA/PC(2 μm)/Kapton with SAM
- S5: Pentacene/PC(100 nm)/PMMA/PC(2 μm)/Kapton
- S6: Pentacene/PC (100 nm)/PMMA/PC(2 μm)/Kapton with SAM
- S7: Pentacene/PC (100 nm)/PMMA/PC(2 μm)/Glass with SAM
- S8: Pentacene/PC(100 nm)/PMMA/PC(2 μm)/Silicon with SAM

From the summary of the electrical parameters for our OFET samples above, we can see that there is no big difference of the performances for the ultra-flexible OFET of Pentacene / PC(100 nm)/PMMA/PC(2 μm) attached on kapton, glass and silicon substrates. With the decrease of the thickness of PC (for the samples of S1, S3, S5), the properties were improved, especially the mobility was increased to 0.056 $cm^2V^{-1}s^{-1}$ for sample S5, which is more than ten times improvement of S1. Compared to the sample with and without PFBT, for example, S1 and S2, the mobility and current on/off ratio were not enhanced a lot. The results indicate the dielectrics have a great effects on the properties of our OFET samples.

4.4 Characterization of pentacene flexible NFGM

4.4.1 The memory electrical properties

- *Transfer characteristics*

To get more information of gate bias values during the operation of the measurement for NFGM, the bias hysteresis of our flexible NFGM devices was measured first and shown in figure 4.23.

Considering the gate operation voltage with sweep +20 V to -20 V for our flexible transistor devices that were analyzed in part 4.3.2, the bias hysteresis measurements were carried out under the application of V_{GS} sweeping ranging from ±10 V to ±40 V with a fixed V_{DS} value of -20 V. The observed reversible hysteresis loop in the current–voltage relationship has two distinct current minima during the forward and reverse traces, and their offset (or the memory window) depends on the initial input V_{GS}. The initial V_{GS}-dependent offset is attributed to the amount of the trapped/detrapped charge carriers in the AuNP floating gate upon

application of the initial input V_{GS}. An application of a negative V_{GS} makes the holes in the pentacene channel to be trapped in the Au NPs, when applying positive V_{GS} above 0 V values, these trapped holes could escape from the Au NPs and gradually reach the pentacene channel, i. e. during reverse sweep (from positive to negative V_{GS} sweep). Thus, with the increase of the gate sweeping voltage, the window of hysteresis engenders and increases, which means there are more holes are trapped in the floating gate when the gate bias is large.

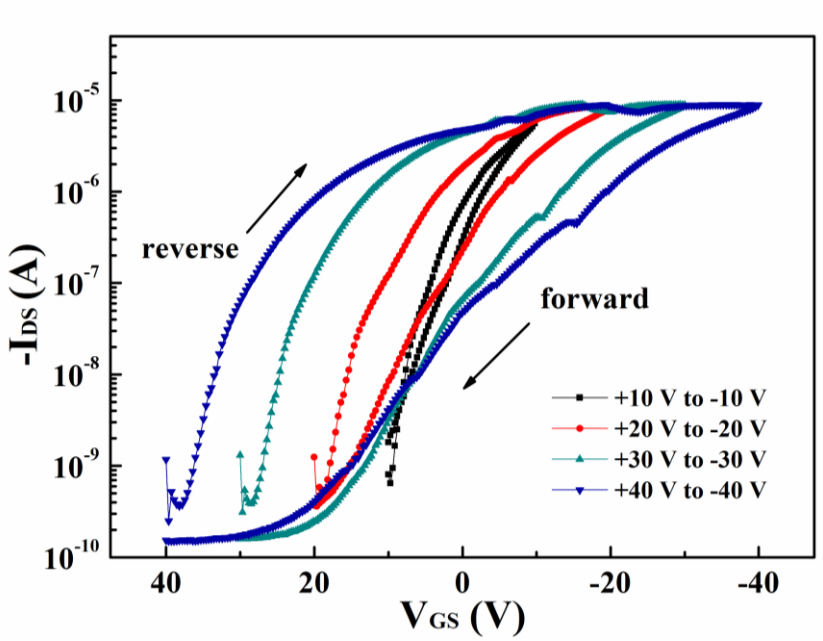

Figure 4.23 The bias hysteresis under the application of V_{GS} sweeping ranging from ±10 V to ±40 V with a fixed V_{DS} value of -20 V.

Figure 4.24 shows the transfer characteristics of the NFGM that measured after the applications of various positive or negative V_{GS} pulses over a short period of time of 1 s. Importantly, the drain current levels at the reading voltage of the flexible NFGM could be controlled systematically by manipulating the number of trapped/released charges between the pentacene channel and the Au NPs. From figure 4.24(a) with $\log I_{DS}$ versus V_{GS}, for better distinguishing the drain current levels under different V_{GS} pulses values, a reading voltage V_{GS} of -6 V was selected in our flexible NFGM devices. The drain current levels at V_{GS} = -6 V increase from 2.6 pA to 0.44 μA, as the pulsed V_{GS} ranges from -40 to +40 V. The clear distinction between different memory states indicated that multi-level data storage could be achieved from our NFGM by using pentacene as a channel material and polymers of PMMA, PC, HSQ as dielectric layers, respectively. The development of multilevel data storage is still in progress, especially in the use of organic-based memories, which can further enhance the memory capacity per unit cell area without reducing the cell size [37, 38].

To observe more clearly of the memory window, figure 4.24 (b) shows the transfer characteristics of the NFGM with linear I_{DS} versus V_{GS}. The memory window is found to be 2.5 V when the V_{GS} pulses are -10 V and +10 V for programing operation and erasing operation, respectively, it increased to 10.7 V with V_{GS} pulses ±20 V. Furthermore, the memory window reaches to 23 V by increasing the V_{GS} operation pulses as ±40 V.

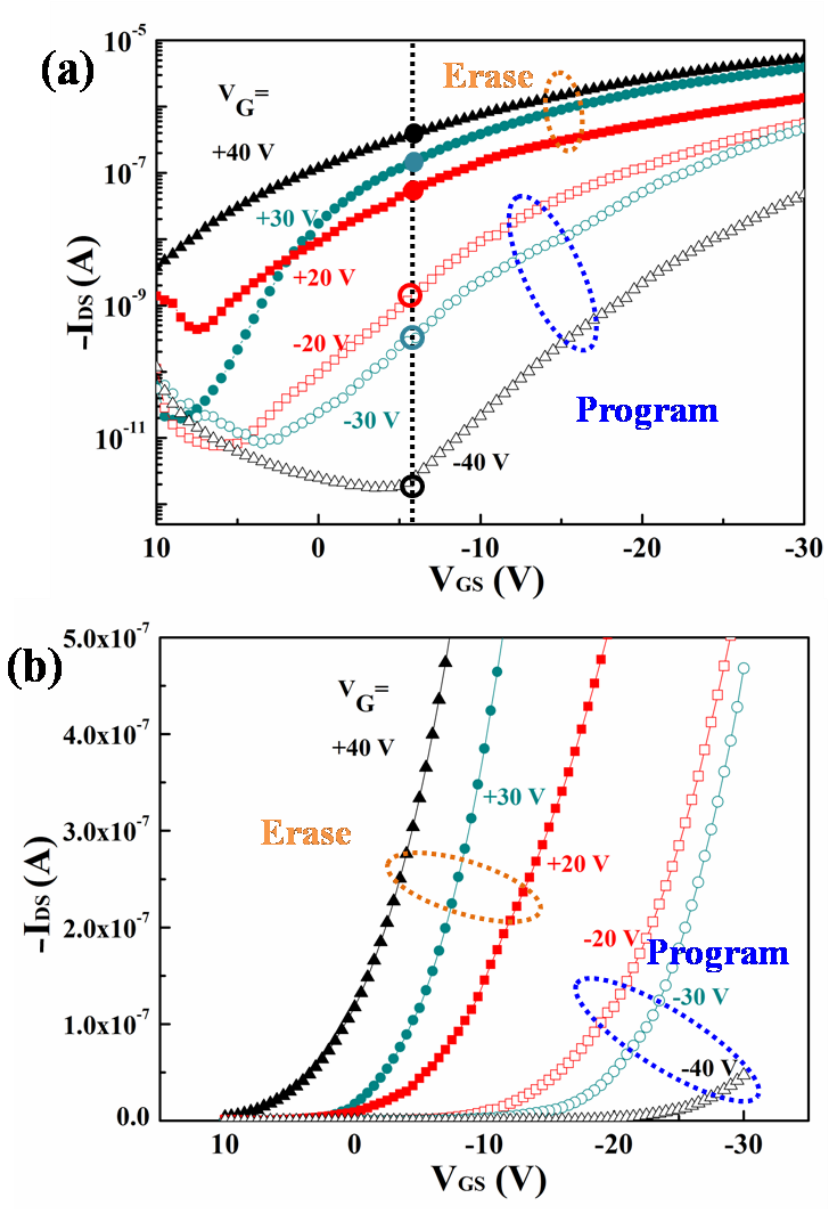

Figure 4.24 I_{DS} Shifts in the transfer curves of the NFGM measured after application of six different pulsed V_{GS} values for 1 s. (a) -log I_{DS} versus V_{GS}, (b) -I_{DS} versus V_{GS}.

In general, increase in applied gate voltage will enhance the probability of tunneling events hence increase the number of trapped/detrapped charge carriers. The observation of saturation region can be explained by the capacitive coupling of charge carriers trapped in each

Au NP [39]. Initially, the charging process is random, however, the capacitive coupling will increase as the number of trapped charge carrier increase, resulting in the enhanced coulomb repulsion. Thus, limited amount of charge carriers are available at certain gate bias and the charging process could continue until the increase in gate bias that governs the deeper level trapping behavior of NPs. In this aspect, multilevel data storage can be realized by utilizing various saturation of programmed/erased state, the same results based pentacene NFGM has been reported in Ref. [40]. In addition, for the structure of our devices, the layer of PC of 100 nm could also act as the polymer electret [41], in previous reports, the energy levels of trapped sites in polymer electret presumably present Gaussian distribution [42, 43]. Therefore, the number of trapped charges in the charge trapping multilevel data storage characteristics obtained by applying different gate voltages suggested that the device possessed nonvolatile write-many-read-many memory behaviors [42-44].

The number of trapped charges in the Au NPs (and polymer electret) (Δn) could be evaluated by using the equation of (4-3).

$$\Delta n = \frac{C\,\Delta V_{th}}{e} \tag{4-3}$$

where C is the capacitance per unit area and ΔV_{th} is the memory window, e is the elemental charge [45]. For our NFGM devices, C is measured by capacitance versus voltage (C-V) with the MIS capacitor structure of Au/Pentacene/HSQ(19nm)/PC(100 nm)/PMMA(260nm)/Au and obtained the value of 2.58×10^{-9} F/cm^2.

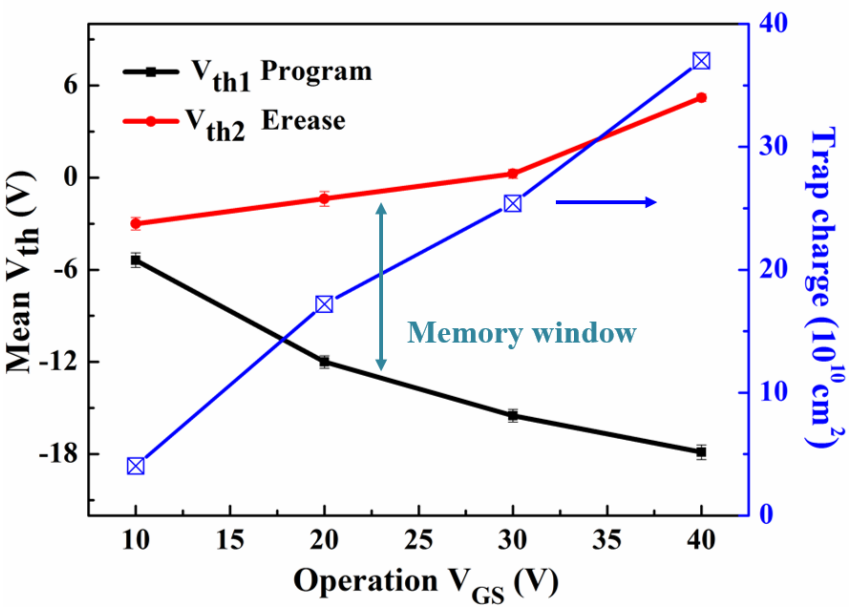

Figure 4.25 Threshold voltages and total number of the trapped charges in the Au NPs as a function of different operation V_{GS}.

Figure 4.25 shows threshold voltages (memory window) and total number of the trapped charges in the Au NPs as a function of different operation V_{GS}. The number of trapped charges increased from 4.03 × 10^{10} cm^{-2} to 3.7 × 10^{11} cm^{-2} as the V_{GS} program/erase increased from ±10 V to ±40 V.

• *The retention and cycling endurance characteristics*

The reliability of the NFGM was examined by measuring the retention time and carrying out cyclic endurance tests. Figure 4.26 presents the retention characteristics of the NFGM under application of various V_{GS}.

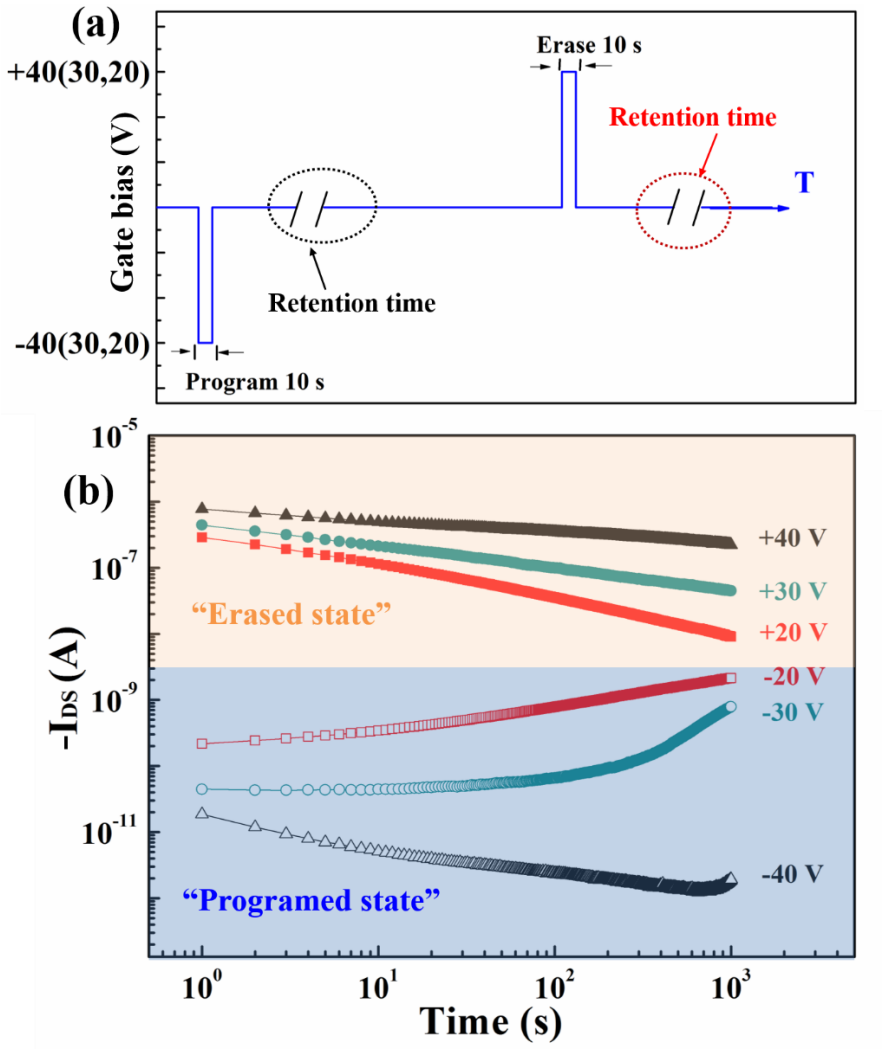

Figure 4.26 (a) The application way of various V_{GS}, (b) the retention characteristics of the flexible NFGM.

The drain current level at each state was monitored over a period of time at V_{GS}= -6 V and V_{DS} =-20 V after the application of -20 V, +20 V, -30 V, +30 V, -40 V and +40 V at the gate for 10 s, as shown in figure 4.26(a). Each programmed and erased state was sustained reasonably up to 10^3 s. When relatively low gate pules of ±20 V and ±30 V operated on the device, a degradation in I_{DS} values was observed for all the data states (programed and erased state), which indicates less trapped charges in the floating gate induced less reliability. When applied gate pules of ±40 V, a slight degradation in I_{DS} values was observed, the I_{DS} current on/off ratio is exceed 10^5 and the retention time is determined to be more than 10^8. Such a good data retention characteristic of the NFGM may be attributed to the 19 nm-thick smooth and pinhole-free HSQ tunneling gate dielectric layer, which reduces the leakage of the trapped charges from the Au NPs to the pentacene channel. Note that the erased state exhibit less distinct storage levels than the programmed state, which could be explained by the reason of eased states are shift back close to the initial state after the erasing operation.

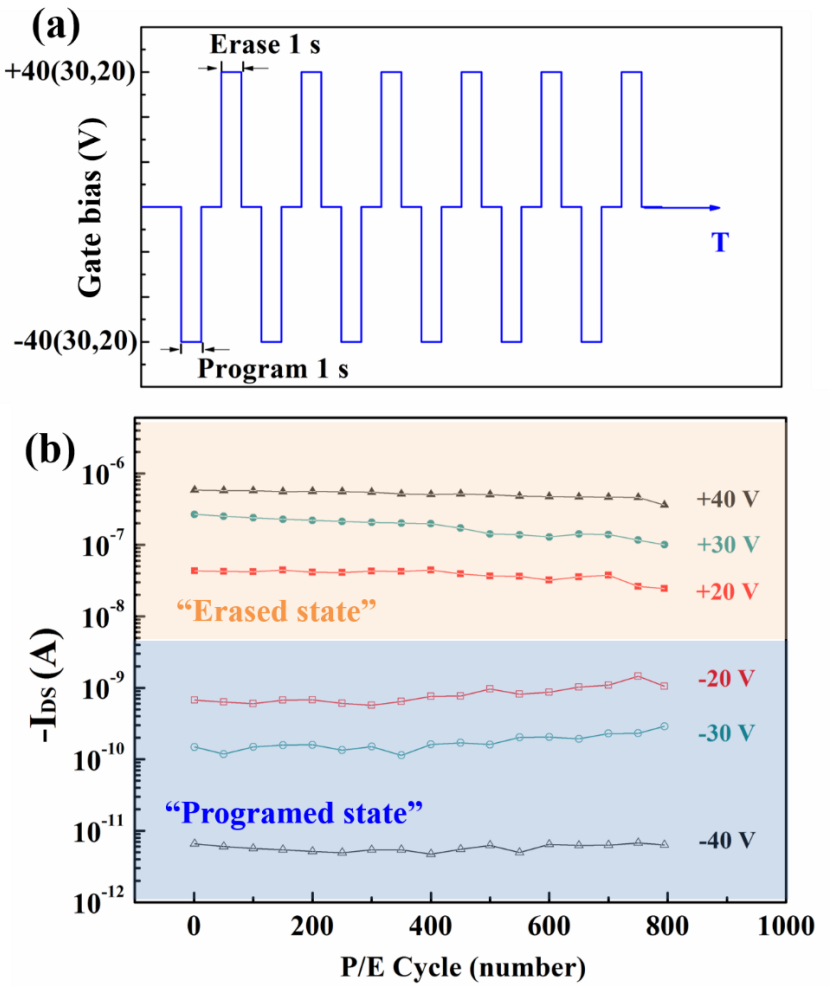

Figure 4.27 (a) The application way of various V_{GS}, (b) The cycling characteristics of the NFGM.

Figure 4.28 presents the drain currents collected as a function of number of continuous programming/erasing cycles. The drain current level at each state was monitored over a period of time at V_{GS} = -6 V and V_{DS} = -20 V after the application of -20 V, +20 V, -30 V, +30 V, -40 V and +40 V at the gate for 1 s. The device exhibits highly reproducible memory behavior with well-separated programmed/erased states for more than 800 cycles without degradation. The results indicate a good endurance property of pour flexible NFGM devices.

• *The dynamic characteristics*

Intriguingly, the dynamic behavior of the NFGM with corresponding current levels under application of various V_{GS} pulse is illustrated in figure 4.28.

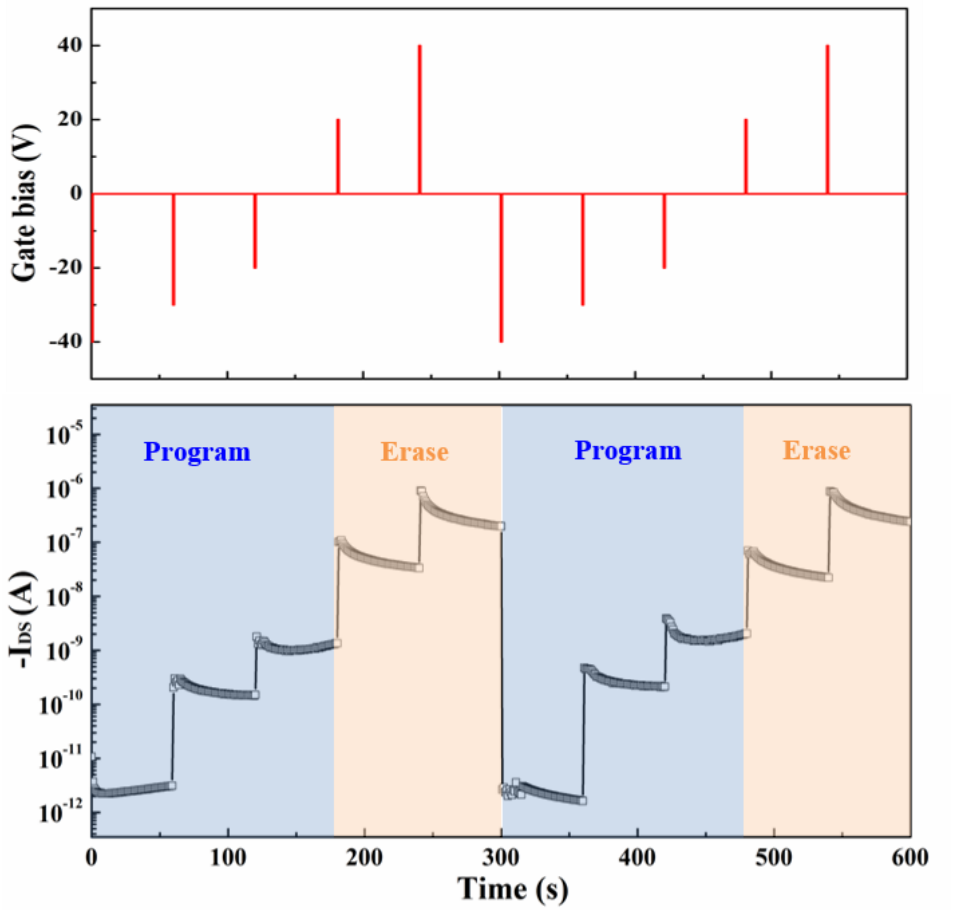

Figure 4.28 The dynamic behavior of the NFGM with corresponding current levels under application of various V_{GS} pulse.

The drain currents were monitored during the application of five different pulsed V_{GS} values with the duration of 1 s. The gate voltages of −20 V, -30 V and -40 V were applied so as

to program a signal (indicated by blue area), while the gate voltages of +20 V and +40 V were applied so as to erase a signal (indicated by orange area) and the current is reading under a small V_{GS} voltage of -6 V for 60 points within each voltage level. Therefore, five well defined data levels are distinguishable with three programed states at current levels ~5×10^{-12} A, ~5×10^{-10} A, ~3×10^{-9} A in conjunction with another two distinct erased states ~1×10^{-7} A, ~1×10^{-6} A, respectively. Each state can be read separately to resemble five levels in a single device. In fact, the extent of storage can be clearly selected depending on the demand of the writing access.

• *The bending characteristics*

Figure 4.29 shows the retention and cycling test for out flexible NFGM under bending conditions.

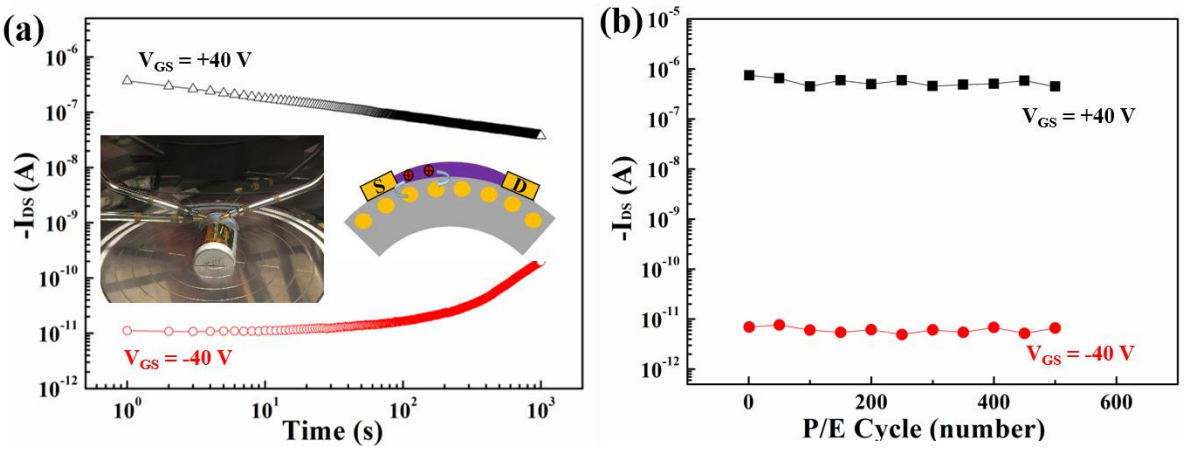

Figure 4.29 The mechanical-stability of the NFGM with corresponding current retention time and cycling tests.

In addition to reliable device operation, the bending stability/mechanical stability is one of the most important parameters to determine the suitability of this device structure for application in flexible electronics. The bending test was carried out by measuring the retention and endurance tests with a radius of curvature of 14 mm. The memory device exhibit retention time larger than 10^3 s with I_{DS} current on/off ratio >10^4 as shown in figure 4.30(a), and almost no degradation in I_{DS} current in both program/erase states after measuring repeatedly for 500 cycles as shown in figure 4.30(b), these observations confirm that our NFGM memory based on Au NPs floating gate and with all organic layers is suitable for flexible electronic memories.

4.4.2 The analysis of mechanisms

To explain the memory characteristics for our flexible NFGM, Figure 4.31 shows the energy band diagrams of a floating gate flash memory transistor at programming mode, storage mode and erasing mode, and the scheme of charge trapping OFET memory based on (i) Au NPs.

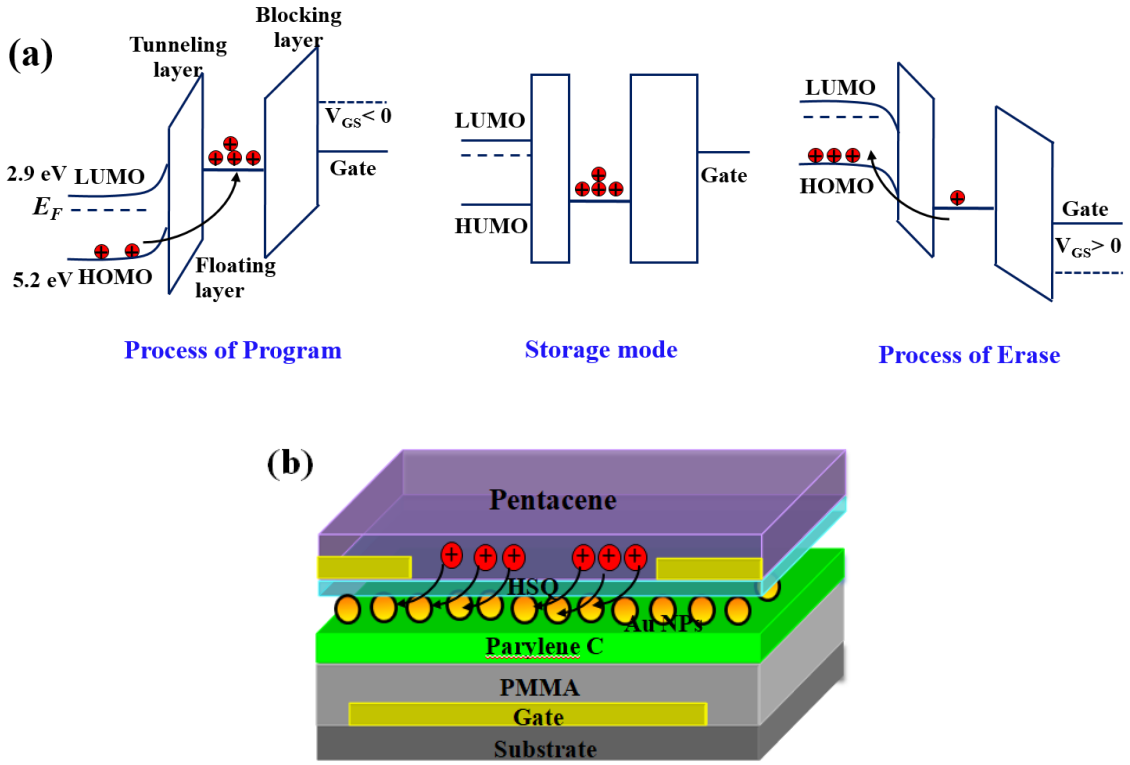

Figure 4.30 (a) Energy band diagrams of a floating gate flash memory transistor at programming mode, storage mode and erasing mode, (b) Scheme of charge trapping OFET memory based on Au NPs.

As we can see in figure 4.31(a), operating mechanism of our flexible memory device can be explained by the equilibrium energy band diagram that corresponds to programming/erasing operations in the reversible hole transport properties. Equilibrium energy band diagram of memory device corresponding to programming operation, erasing operation and storage state are illustrated. With the application of negative bias on the gate electrode, the transfer curve shifts towards negative voltage direction in comparison with the initial state, which confirms that Au NPs act as trapping element of holes [40], the trapped charge carriers which transfer from pentacene screen the gate and manipulate the conduction in the channel. In

order to release the stored charges, the gate should be reversed biased. Figure 4.30(b) illustrates scheme of charge trapping of our flexible NFGM. The charges may be trapped by Au NPs. As the existence of capacitive coupling, multilevel data storage can be realized by utilizing various saturation of programmed/erased state as the increase in gate bias that governs the deeper level trapping behavior of NPs [40].

4.5 Conclusions

In this chapter, the pentacene based flexible OFET and NFGM devices were prepared and characterized. First, for fabricating flexible transistors, the insulator polymers PMMA, PC were selected to be used as the bilayer gate dielectric layers. All the layers were organic materials that deposited under low temperatures and could be transferred on other kinds of substrates, the silicon, glass and kapton substrates were used in this chapter and the characteristics were compared. For the I-V characteristics, the operation voltage was deduced and there was no hysteresis behavior observed, which means the interface traps between the dielectrics and was decreased. The flexible OFET with structure of Pentacene/PC(100 nm)/PMMA/PC(2 μm)/kapton obtained high mobility of 0.08 $cm^2V^{-1}s^{-1}$ and current on/off ratio of 2.5×10^5.

Then, based on the results of flexible OFET, the flexible NFGM devices wither structure of Pentacene/HSQ(19 nm)/Au NPs/PC(100 nm)/PMMA/PC(2 μm)/Kapton were realization the memory performances were demonstrated. The large memory window of 23 V were obtained by application of V_{GS} pulse of $\pm$40 V, the multi-level data storage could be achieved from our flexible NFGM by using pentacene as channel material and polymers of PMMA, PC, HSQ as dielectric layers, respectively, which could be explained the deeper level trapping behavior of NPs under the increase in gate bias. In addition, the bending stability/mechanical stability test confirm that our NFGM memory based on Au NPs floating gate and with all organic layers is suitable for flexible electronic memories.

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Conclusions and perspective

• *Conclusions*

In this thesis, we succeed to fabricate, optimize and characterize the pentacene based OFET and NFGM devices on rigid and flexible substrates.

First, in order to find a way to optimize NFGM devices, among the many possibilities to optimize the OFET, we used OTS and PFBT SAMs to modify the SiO_2 dielectric layer and on gold source/drain electrodes. With SAMs modification, the electrical results with high mobility 0.68 $cm^2V^{-1}s^{-1}$ and high current on/off ratio $>10^6$ were obtained. We compared the results and explained the optimization characteristics by tuning the way of charge transport between pentacene and dielectrics, pentacene and electrodes, respectively. Then, based on the results of the OFET, we fabricated SFG and DFG memory devices, Au NPs and rGO sheets were used as charge trapping layers. The performances of SFG (Au NPs as floating gate) and DFG (hybrid Au NPs and rGO sheets as the lower and upper floating gate, respectively) were presented and compared, and the effect of rGO sheets on the memory properties were well discussed. In particular, we used PFBT SAM to modify our SFG and DFG memory devices. The NFGM with PFBT exhibits excellent memory performances, including high mobility of 0.23 $cm^2V^{-1}s^{-1}$, the large memory window of 51 V, and the stable retention property more than 10^8 s, as well as reliable cycling endurance over 1000 cycles. The optimized performances of the NFGM are explained by the increase of charge injection due to the increase of the work function of gold electrodes after the PFBT modification, which further resulting the increase of trapped charge density in Au NPs floating gate. The consideration about the influence of charge injection at the interface of organic semiconductors/electrodes on the performances of NFGM has not been reported yet, and the results highlight the utility of SAM modulations and controlling of charge transport in the development of transistor memories.

Second, we fabricated pentacene based OFET that fabricated on kapton flexible substrates, and all the layers of the device are organic materials, which could be obtained with simple fabrication processes and under low temperature. The ultra-flexible OFET with structure of the Pentacene/PC(100 nm)/PMMA/P (2 μm) could be attached on many kinds of substrate, in this thesis, the silicon, glass and kapton substrates were used and the characteristics were compared. Compared with the I-V characteristics of pentacene FET that fabricated on conventional SiO_2/Si with lithography technique in this thesis, the operation voltage of our flexible OFET devices was deduced and there was no hysteresis behavior observed, which

means the interface traps between the polymer dielectrics and was decreased. In the end, we found that the flexible OFET with structure of Pentacene/PC(100 nm)/PMMA/PC(2 μm)/Kapton obtained high mobility of 0.08 $cm^2V^{-1}s^{-1}$ and current on/off ratio of 2.5×10^5.

Finally, based on the results of our pentacene flexible OFET, the flexible NFGM devices with structure of Pentacene/HSQ(19 nm)/Au NPs/PC(100 nm)/PMMA/PC(2 μm)/Kapton were realized and the memory performances were demonstrated. The large memory window of 23 V were obtained by application of V_{GS} pulse of $\pm$40 V, and we found the multi-level data storage performances for our flexible NFGM by using pentacene as a channel material and polymers of PMMA, PC, HSQ as dielectric layers, respectively, which could be explained the deeper level trapping behavior of NPs under the increase in gate bias and the energy levels of trapped sites in polymer electrets. In addition, the bending stability/mechanical stability tests confirm that our NFGM memory based on Au NPs floating gate and with all organic layers is suitable for flexible electronic memories.

To our knowledge, these results of our pentacene based flexible OFET and NFGM reach the state of the art for pentacene flexible devices. Furthermore, depositing Au NPs on the surface of polymer PC by using the chemical way has not been reported yet.

• *Perspective*

Based on the experiments results of this work, we highlight the efficient ways to optimize the OFET and fabricate the flexible NFGM by simple fabrication process. However, one of the main prospective for electronic devices is to achieve miniaturization, high performance, integrated circuits. From the process point of view, several orientations are needed:

• Fabrication with lithography techniques that contribute the minimization of the flexible devices in further study.

• Selection of the high-K organic dielectrics to reduce the operation voltages.

• Insert the double floating gate layer to increase the memory window and retention time, for example, the rGO sheets that we used for fabricating the DFG memory on conventional SiO_2 /Si substrate.

List of publications

• *Journals*

1. **S. Li**, D. Guérin, S. Lenfant. K. Lmimouni. Optimization of Pentacene double floating gate memories based on charge injection regulated by SAM functionalization. AIP Advances, 2018, 8, 025110.

2. **S. Li**, D. Guérin, K. Lmimouni. Improving performance of OTFTs by tuning occurrence charge transport on pentacene interaction with hybrid contacts. Microelectronic Engineering, 2018, 195, 62-66.

3. **S. Li**, D. Guérin, K. Lmimouni. All transferred ultra-flexible pentacene field-effect transistors by fabricating with all organic thin film layers. (under redaction)

4. **S. Li**, D. Guérin, K. Lmimouni. Flexible organic nano-floating gate memory with multi-level charge storage by combing charge store in nanoparticles and electrets. (under redaction)

• *Conferences*

5. **S. Li**, D. Guérin, K. Lmimouni. Improving performance of transistor memory by tuning occurrence charge transport on pentacene interaction. Telecom'2017 & 10ème JFMMA, 10-12 may 2017 Rabat, Maroc. (poster)

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Realization and characterization of OFET and NFGM on rigid and flexible substrates

Abstract:

Organic field effect transistor (OFET) and organic based nano-floating gate memory (NFGM) devices are essentially expected to meet emerging technological demands that realizing flexible and wearable electronic devices. The objective of this thesis is to develop and optimize the pentacene based OFET and NFGM on rigid and flexible substrates.

First, self-assembled monolayers (SAMs) were used to optimize the OFET, a high mobility of 0.68 $cm^2V^{-1}s^{-1}$ and current on/off ratio $>10^6$ were obtained. Then, we fabricated single floating gate (SFG) and double floating gate (DFG) memory devices by using gold nanoparticles (Au NPs) and reduced graphene oxide (rGO) sheets as charge trapping layers. In particular, the DFG with PFBT exhibits excellent memory performances, including the large memory window of 51 V, and the stable retention property more than 10^8 s.

Third, we fabricated all organics based OFET and NFGM on kapton flexible substrates with simple fabrication process under low temperature. The large memory window of 23 V was obtained, and the multi-level data storage performance was observed for our flexible NFGM devices. In addition, the bending stability/mechanical stability test present high current on/off ratio $>10^5$, retention time $>10^4$, as well as cycling exceed 500 cycles. Based on the experiments results of this work, we highlight the efficient ways to optimize the OFET and fabricate the high performances of flexible NFGM by simple fabrication process.

Key words: pentacene transistor, memory, gold nanoparticles, self-assembled monolayer, flexible electronics, multi-level storage

Réalisation et caractérisation de transistors à effet de champ organiques OFETs et Mémoires à nano grille flottante sur des substrats rigides et flexibles

Résumé

Depuis la découverte des polymères conducteurs, de nombreuses études ont été menées afin d'utiliser ces nouveaux matériaux semiconducteurs en tant que couche active de composants électroniques. Dans cette thèse nous nous intéressons à deux composants clés de l'électronique organique: Les transistors à effet de champs et les mémoires à nano-grille flottante seront réalisés à la fois sur des substrats rigides et flexibles. Pour l'optimisation de nos dispositifs, nous avons choisi de travailler sur les interfaces.

Tout d'abord, des monocouches auto-assemblées SAMs ont été utilisés pour optimiser les interfaces électrode/SCO et diélectrique/SCO de l'OFET: des mobilités de $0.68 cm^2V^{-1}s^{-1}$ et des rapports on/off $>10^6$ ont été obtenus. Par la suite, nous avons fabriqué des dispositifs de mémoire à simple grille flottante SFG en utilisant les en nanoparticules (NPs) d'or et à double grille flottante DFG en utilisant les NP d'or et des feuillets de graphène comme couches de piégeage de charges. En particulier, les DFG avec PFBT présentent en effet d'excellentes performances (une large fenêtre mémoire de 51V et un temps de rétention stable et de plus de 10^8s).

Ensuite, nous avons fabriqué tous les dispositifs sur des substrats souples en kapton avec des processus de fabrication simples et à basse température. Ces NFGM flexibles ont été caractérisées et leurs performances mesurées (fenêtre mémoire de 23V). Nous avons également mis en évidence un piégeage multi-niveaux dans les NPs. De plus, ces composants ont montré une bonne résistance aux tests de flexibilité et de pliage et une stabilité très satisfaisante (supérieure à 500 cycles).

Mots clés : transistor pentacène, mémoire, nanoparticules d'or, monocouche auto-assemblée, électronique flexible, stockage multi-niveaux