THESE

Présentée à l'Université de Lille
Ecole Doctorale des Sciences pour l'Ingénieur

Institut d'Electronique, de Microélectronique et de nanotechnologies de Lille
STMicroelectronics Crolles

Pour obtenir le grade de :
DOCTEUR DE L'UNIVERSITE

Spécialité: MICRO-NANO SYSTEMES ET CAPTEURS

Par

Thierno Moussa BAH

Développement et caractérisation d'un démonstrateur de générateur thermoélectrique à base de membranes de silicium couplées à de l'ingénierie phononique

Soutenue le 03 Juillet 2019 devant le Jury composé de :

Mr. Olivier BOURGEOIS, *Directeur de Recherche* CNRS, Institut Néel, Grenoble	Président du Jury Rapporteur
Mme. Sylvie HEBERT, *Directrice de Recherche* CNRS, CRISMAT, Caen	Rapporteur
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Thesis Summary:

The lack of reliable, safe and low-cost energy source seems to delay the blooming of the internet of things (IoT) and wireless sensors nodes. Thermoelectric harvesters feature those key advantages. Silicon presents the advantages to be most abundant, less environmental harmful and to benefit from facilities and technological processes for low cost thermoelectric harvesters mass production compared to the conventional materials (bismuth telluride alloys). However, silicon is a poor thermoelectric material due to its high thermal conductivity ($150 W m^{-1} K^{-1}$). The possibility to reduce the thermal conductivity while preserving electrical conductivity and Seebeck coefficient is the key to upgrade silicon as an efficient thermoelectric material. To that end, efforts are oriented towards the phononic part of heat transport, which is the dominant contribution in semiconductors. The researches carried out during this thesis dealt with the integration of phonon engineered silicon membranes into thermoelectric harvester demonstrators and their characterizations with respect to the state of the art. The results demonstrated the feasibility of a silicon based thermoelectric harvester exhibiting performance (from **few µW/cm²** for ΔT~5-10K to **few mW/cm²** for ΔT>100K) sufficient for autonomous sensor nodes' power supplying and comparable performance with the bismuth telluride state of the art harvester according to the harvesters' cooling conditions. Moreover, this thesis demonstrated, in addition to the energy harvesting, the possibility of developing silicon based thermoelectric coolers, opening the way to possible integration of thermoelectric coolers in silicon based micro-electronic devices.

Résumé de la thèse :

L'essor de l'internet des objets (IoT) et des capteurs autonomes et communicants semble être retardé en raison du manque de source d'énergie fiable, sûre et à faible coût. Les récupérateurs d'énergies thermoélectriques présentent ces avantages clés. Le silicium présente les avantages d'être très abondant, moins polluant et de bénéficier d'installations et de procédés technologiques permettant la production en série de récupérateurs d'énergies thermoélectriques à faible coût par rapport aux matériaux conventionnel (alliages de tellure de bismuth). Toutefois, le silicium est un matériau thermoélectrique médiocre en raison de sa conductivité thermique élevée ($150 W m^{-1} K^{-1}$). La possibilité de réduire la conductivité thermique tout en préservant la conductivité électrique et le coefficient Seebeck est la clé pour améliorer le silicium en tant que matériau thermoélectrique efficace. À cette fin, les efforts sont orientés vers la partie phononique du transport de chaleur, qui constitue la contribution dominante dans les semi-conducteurs. Les recherches menées au cours de cette thèse ont porté sur l'intégration des membranes de silicium nanostructurées de réseaux phononiques dans des démonstrateurs de récupérateurs d'énergies thermoélectriques et leur caractérisation au regard de l'état de l'art. Les résultats de ces études ont démontré la faisabilité d'un récupérateur d'énergie thermoélectrique à base de silicium présentant des performances (De **quelques µW/cm²** pour ΔT~5-10K à **quelques mW/cm²** pour ΔT>100K) suffisantes pour l'alimentation en énergie de nœuds de capteurs autonomes et des performances comparables à celles d'un récupérateur (état de l'art) à base de tellure de bismuth en fonction des conditions de refroidissement de ces derniers. De plus, cette thèse a démontré, outre la récupération d'énergie, la possibilité de développer des refroidisseurs thermoélectriques à base de silicium, ouvrant la voie à une possible intégration de refroidisseurs thermoélectriques dans des dispositifs micro-électroniques à base de silicium

General Introduction

The blooming of the so-called Internet of things (IoT) and wireless sensors nodes (WSN) raise the problematic of finding reliable and easily available energy sources. Moreover, according to [Nordrum 2016], this blooming seems to be delayed owing to the lack of reliable, safe and low-cost energy source. Thermoelectric energy harvesting features key advantages of reliability and is complementary to other energy sources. However, its efficiency is intrinsically limited to a few percent around room temperature and usually relies on harmful materials. Indeed, for near room temperature applications the best thermoelectric materials are alloys of bismuth and telluride (rare, expensive and environmentally harmful). These drawbacks of the best thermoelectric material limit currently thermoelectric harvesting to specific applications. Silicon (the most abundant and used semiconductor) can be the key to answer the problematics of cost and environmental impact rose by conventional materials use. However, silicon is a poor thermoelectric material due to its very high thermal conductivity (hundred times higher than bismuth telluride thermal conductivity). Reducing the silicon thermal conductivity became for the two last decades a subject of high interest in the thermoelectric community. The results from this research demonstrated the importance of developing low dimensionality material in order to reduce the silicon thermal conductivity. Indeed, significant silicon thermal conductivity reduction have been demonstrated by using silicon nanowires [Boukai et al. 2008] and thin films patterned with nanoscale holes [Tang et al. 2010] for example. Research also focus on developing silicon based micro thermoelectric harvester demonstrators. Those demonstrators are mainly made of silicon nanowires and thin films. However, those demonstrators do not exhibit sufficient performances to compete with the bismuth telluride state of the art micro thermoelectric harvesters (cf. chapter 1).

The work carried out throughout this thesis aims at studying and developing a silicon based micro thermoelectric harvester demonstrator, sufficiently efficient to power supply autonomous sensors nodes. This work is in the continuity of two previous thesis [Haras 2016; Lacatena 2016] aiming at improving the silicon's thermoelectric properties by reducing its thermal conductivity. By coupling the Si membranes dimension reduction with phononic engineering patterning, the two thesis allowed to reduce the thermal conductivity from 148 W/m/K (bulk silicon) to 34.5 W/m/K [Haras et al. 2016].

The manuscript includes four chapters. The **first** chapter reviews the need of energy harvesting rose by the development and blooming of wireless sensor networks (WSN) by comparing the energy needed to power supply the WSN and the harvestable energy from common energy harvesting techniques. Later, the theory behind thermal energy harvesting, before reviewing key results of micro energy harvesters. The review focuses mainly on silicon thermoelectric properties improvement and its integration into micro thermoelectric harvesters for near room temperature applications. The review focuses also on the best micro-harvesters developed so far for applications near room temperature (even if they are not made of silicon).

The **second** chapter deals with the theoretical study of the silicon based thermoelectric harvester demonstrator developed. This study aims at:

- Estimating the performances that we can expect from such generators
- Determining the optimal dimensions for the demonstrators' realization
- Benchmarking the planar Si based TEG with commercial based thermoelectric harvester
    - Understand the benefits and the drawbacks of the Si based TEG with respect to the commercial one.

Modeling is done by means of FEM (Finite Element Modeling). Analytic models are also developed in order to:

- Check the consistency of the FEM and an analytic model based on thermoelectric equations
- Save computation time, after checking the consistency of FEM and analytic model

The **third** chapter describes the realization process of the phonon engineered silicon membranes based thermoelectric harvester demonstrator. In addition to the harvester demonstrators' realization (main objective of this chapter) elementary devices indispensable, to complete the demonstrators' characterization (thermal conductivity, Seebeck coefficient and electrical conductivity measurement platforms) are also characterized. The chapter presents first the different devices designs, before detailing the different fabrication steps.

The **fourth** and last chapter describes the characterization of the different devices realized during this thesis work and discuss the different results. The chapter is organized in four main parts:

- First, the description of the different characterization protocols: How the measurements are performed on the different devices, under which environment are performed the measurements, the different apparatus needed for the characterizations.
- Second, the chapter focuses in the thermoelectric properties on the different elementary devices (all except the demonstrators) and especially, the impact of the phonon engineering on those thermoelectric properties.
- Third, the harvester demonstrators' characterizations are performed. In this third section (the main one), the demonstrators' characterization methodologies are detailed before focusing on extracting the different thermoelectric performances (thermoelectric voltage, produced electrical power, …) and the performances discussion with respect to the modeling results presented in chapter 2 and the state of the art micro-harvesters' performances.
- Finally, after the problematic of thermoelectric harvesting, the chapter deals with the possibility of using the developed demonstrators as thermoelectric coolers through the investigation of the Peltier effect on the developed demonstrators.

Chapter 1: Silicon based thermoelectric harvesters: Problematics and Challenges

Abstract

This first chapter reviews the need of energy harvesting rose by the development and blooming of wireless sensor networks (WSN) by comparing the energy needed to power supply the WSN and the harvestable energy from common energy harvesting techniques. Later, the theory behind thermal energy harvesting, before reviewing key results of micro energy harvesters. The review focuses mainly on silicon thermoelectric properties improvement and its integration into micro thermoelectric harvesters for near room temperature applications. The review focuses also on the best micro-harvesters developed so far for applications near room temperature (even if they are not made of silicon).

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1.1 Wireless Sensors Networks and power supply

Energy harvesting is a known concept, wind turbines and solar farms are the most common example. In this work, we focus on developing energy harvesters of much lower power scale dedicated to power supply small and autonomous sensors devices capable of monitoring their surrounding environment called wireless sensors nodes.

The final goal of wireless sensor nodes development is to combine them to form a network of sensors capable of monitoring their surroundings and exchange information wirelessly between them, called wireless sensor network (WSN). The smallest dimensions and lower cost of these sensors will generalize their use:

- ***Industrial monitoring:*** WSNs can be used for rare event detection or periodic data collection in industrial environment [Low and Win 2005]. For rare event detection, WSNs will detect and classify unusual events due to failure of machines, processes, security … On the other hand periodic data gathering will aim to monitor and/or control materials flows, machines, processes, manufacturing pollution … WSNs would allow engineers to gather real-time data for a better management of the manufacture.
- ***Smart cities development:*** The perpetual increase of cities' population generates new kind of problems for the cities. Indeed, this increase will generate more and more challenges (e.g traffic jams, energy consumption management, …) [Chourabi et al. 2012]. WSNs use would allow a better management of those cities or megacities by:
    - ***Traffic monitoring:*** Management of transport systems have a direct influence on the cities' economy. A well-managed, easily accessible public transportation is indispensable to attract workers and investors in a city. Urban WSNs can allow a better traffic congestion monitoring by deploying sensors along the road in order to gather real time traffic information and make it available to citizens.
    - ***Infrastructures monitoring and control***: preserving historical patrimonies but also improved the quality of life of citizens implies to invest in roads and buildings health care monitoring and control. The use of WSNs will allow gathering continual and enormous data of these infrastructures' integrity by deploying sensors allowing the monitoring of their stress, deformations and the impact of the pollution for example [Lynch and Loh 2006].
    - ***Waste management:*** The growth of cities goes with the growth of waste. A good waste management policy is indispensable to avoid the development of unsanitary cities. In [Nuortio et al. 2006] it is recommended to use smart containers to detect the level of load and optimize the trucks' route.
    - ***Energy consumption monitoring:*** WSNs can also allow a better energy consumption management by gathering information of energy consumption throughout the city.
- ***Body sensors:*** This is an important and fast growing market for wireless sensor networks. The best application field is in medicine where wearable or implantable sensors can be used for medical treatment. Indeed, sensors able to continuously monitor a patient vitals and alert emergencies if needed can facilitate the patient care [Stojmenović 2005]. Chronically-ill patients can also be helped by WSNs to monitor constantly the biological signs linked to the illness like hypertension, heart disease, diabetes[Martins et al. 2004; Zhang et al. 2016; Darwish and Hassanien 2011; Lee and Chung 2009].

The development of wireless sensor nodes due to the reduction in size and in power consumption of electronic devices raises the question of their power supplying. The first idea will be to use batteries. Indeed, batteries have the advantage to power supply at the desired

voltage. However, batteries can be cumbersome to small sensors and the lifetime of batteries raises the issue of their replacement, which can be expensive if we have many sensors [Zhu and Beeby 2011]. Moreover, the function of many sensors will be to monitor environment where we already have energy sources like heat, vibrations … Making interesting the idea of developing energy harvesters to power supply the sensors from the surrounding environment than using batteries for example. *Vullers et al.* [Vullers et al. 2009] summed up the estimated power consumption and energy autonomy of some electronic devices.

Electronic device	Power consumption	Energy autonomy
Smartphones	1 W	5 h
MP3 Player	50 mW	15 h
Hearing Aid	1 mW	10 days
Wireless sensor node	100 µW	Infinite
Cardiac Pacemaker	50 µW	7 years
Quartz watch	5 µW	5 years

Table 1- 1: common electronic devices power consumption and autonomy [Vullers et al. 2009]

From table 1-1 we notice that a wireless sensor node requires 100µW to run, the question now is what amount of energy can we expect from the different available energy sources? In the same paper [Vullers et al. 2009], Vullers et al. answer the question by the table given hereafter.

Energy sources	Available Power	Harvestable Power
Ambient Light • Indoor • Outdoor	 0.1 $mWcm^{-2}$ 100 $mWcm^{-2}$	 10 μWcm^{-2} 10 $mWcm^{-2}$
Vibration/motion • Human • Industrial	0.5m @ 1Hz, 1ms^{-2} @ 50 Hz 1m @ 5Hz, 10ms^{-2} @ 1 kHz	4 μWcm^{-2} 100 μWcm^{-2}
Thermal Energy • Human • Industrial	 20 $mW.cm^{-2}$ 100 $mWcm^{-2}$	 30 μWcm^{-2} (ΔT~5-10K) 1-10 $mWcm^{-2}$ (ΔT>50K)
• RF / Cell phone	0.3 μWcm^{-2}	0.1 μWcm^{-2}

Table 1- 2: Energy harvesting sources, available power and harvestable power [Vullers et al. 2009]

Choosing the right harvester, will of course depend on the output power of the harvester, but also on the available energy in the sensor's ambient environment. In this thesis, we will not deal with all the different methods of energy harvesting but only with thermal energy harvesting. The table shows that with thermal energy harvesters, wireless sensor nodes can be power supplied.

1.2 Thermoelectric Energy Harvesting

Thermoelectricity is a reversible physical phenomenon allowing the direct conversion of heat into electricity (Seebeck Effect) or the direct conversion of an electrical current into heat (Peltier Effect).

1.2.1 Thermoelectric Effects

Three effects characterize thermoelectricity: the Seebeck Effect, the Peltier Effect and the Thomson Effect. Each effect bears the name of the scientist who discovered it.

1.2.1.1 The Seebeck Effect

Discovered in 1822 by Thomas Seebeck, it consists on the generation of electrical field $\vec{E}$ in response to a thermal gradient $\vec{\nabla}T$ through two electrically different materials, associated electrically in series and thermally in parallel. The relation between these two physical parameters is:

$$\vec{E} = S \cdot \vec{\nabla}T \qquad \textit{equation 1- 1}$$

S [$V \cdot K^{-1}$] being the Seebeck coefficient or thermopower. S depends on the carriers' nature and concentrations. It can be positive or negative depending on the nature of the majority carriers. This is the effect used to develop thermoelectric generators/harvesters.

1.2.1.2 The Peltier Effect

Discovered one decade after the Seebeck effect by Jean Charles Peltier, this effect is the opposite of the Seebeck effect. Indeed, it consists in the absorption or generation of heat q due the propagation of an electrical current j through two electrically different materials, associated electrically in series and thermally in parallel as previously. The relation between the heat exchanged and the current is:

$$q = \pi \cdot j \qquad \textit{equation 1- 2}$$

π [V] being the Peltier coefficient. This effect is used to develop coolers well known as Peltier modules.

1.2.1.3 The Thomson Effect

From the work of William Thomson (Lord Kelvin), this effect combines the two previous effects but this time, we consider just one material. Indeed, when at the same time, an electrical current j and a thermal gradient $\vec{\nabla}T$ propagate through a material, heat is absorbed/generated q by the material. The exchanged heat is expressed as follows as a function of the electrical current and the thermal gradient.

$$q = \beta \cdot j \cdot \Delta T \qquad \textit{equation 1- 3}$$

ΔT and β [VK^{-1}] being respectively the temperature difference between the two ends of the material and the Thomson coefficient.

1.2.2 Thermoelectric properties

Thermoelectric harvesters are made of an assembly of electrically different materials. These materials are associated electrically in series and thermally in parallel. Though Seebeck voltages can be generated using any pair of conducting materials, it took more than one century

before Ioffe [Ioffe et al. 1959] and Goldsmid [Goldsmid et al. 1958] established heavily doped semiconductors as best thermoelectric materials enabling practical use of TE generation. Currently, thermoelectric harvesters are made of *p*-doped and *n*-doped semi-conductors associated electrically in series and thermally in parallel as shown in figure 1-1-

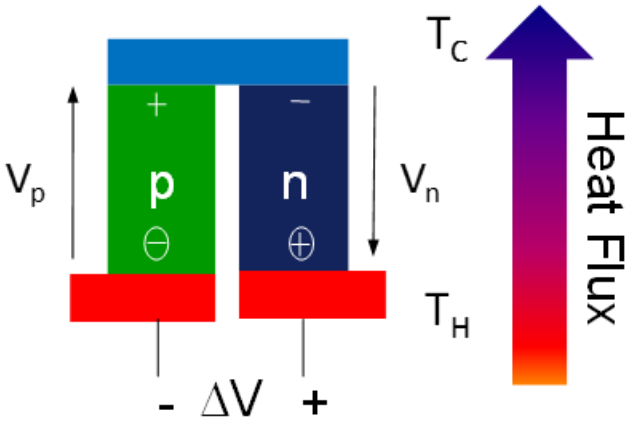


Figure 1- 1: Thermoelectric energy harvesting principle

The efficiency of an ideal thermoelectric harvester is given by η:

$$\eta = (1 - \frac{T_C}{T_H}) \cdot \frac{\sqrt{(1 + zT_m)} - 1}{\sqrt{(1 + zT_m)} + \frac{T_C}{T_H}} \qquad \textit{equation 1- 4}$$

This maximal efficiency is the product of the Carnot efficiency η_C and the efficiency linked to the thermoelectric properties of the materials used to develop the harvester η_{TE}.

$$\eta_C = 1 - \frac{T_C}{T_H} \qquad \textit{equation 1- 5}$$

$$\eta_{TE} = \frac{\sqrt{(1 + zT_m)} - 1}{\sqrt{(1 + zT_m)} + \frac{T_C}{T_H}} \qquad \textit{equation 1- 6}$$

$$zT_m = \frac{(S_p - S_n)^2}{\left(\sqrt{\rho_n \kappa_n} + \sqrt{\rho_p \kappa_p}\right)^2} \times T_m \qquad \textit{equation 1- 7}$$

$$T_m = \frac{T_C + T_H}{2} \qquad \textit{equation 1- 8}$$

T_C, T_H, zT_m being respectively the temperature of cold source (ambient air for example), the temperature of the hot source and the figure of merit of the thermocouple (*p* and *n* doped material association) at the average temperature T_m. The hot and cold source temperature being constant, the leverage to improve the efficiency of the thermoelectric harvester is the maximizing of the figure of merit ZT_m according to equation 1-4. Maximizing the figure of merit consists in choosing or developing materials with high Seebeck coefficient, high electrical conductivity and low thermal conductivity. This is contradictory because in nature a good electrical conductor is also a good thermal conductor.

1.2.2.1 Thermal conductivity

Heat diffuses according to three phenomena, Heat conduction (in solids), convection (in fluids, gas) and thermal radiation (in vacuum and in air). The thermoelectric harvester being made of crystalline materials, the heat will diffuse through thermal conduction according to the Fourier law:

$$\vec{q} = -\kappa \cdot \vec{\nabla} T \qquad \textit{equation 1- 9}$$

In metals, the heat diffuses through the electrons' propagations. The thermal conductivity is given by the Wiedemann-Franz law, which relates the electron thermal conductivity to the material electrical conductivity (equation 1-10). The electronic contribution is related to electrical conductivity through the Lorenz' number L.

$$\kappa_e = \sigma \cdot L \cdot T \qquad \textit{equation 1- 10}$$

On the other hand, in insulating materials, the heat diffuses through the lattice vibrations (phonons). The Debye's relation as presented by equation 1-11 formulates the lattice thermal conductivity in first approximation, the phononic contribution depends on the volumetric specific heat C of the material, the phonons' mean free path Λ and group velocity *v*.

$$\kappa_{ph} = \frac{C \cdot \Lambda \cdot v}{3} \qquad \textit{equation 1- 11}$$

In thermoelectric materials, mostly semiconductors the heat diffuses through both mechanisms. The thermal conductivity is given by equation 8.

$$\kappa = \kappa_e + \kappa_{ph} \qquad \textit{equation 1- 12}$$

1.2.2.2 Seebeck Coefficient

The Seebeck coefficient represents the ability of the material to convert any thermal gradient into an electric field (see section II.1-a). The Seebeck coefficient is defined as follows:

$$S = \frac{\Delta V}{\Delta T}|_{\Delta T \to 0} \qquad \textit{equation 1- 13}$$

From equation1-13, it is difficult to extract a general formula for the Seebeck coefficient calculation. However, Cutler et al in [Cutler and Mott 1969] defined a general formula known as Mott formula, allowing in metals or degenerate semiconductors the calculation of the Seebeck coefficient. This formula is based on the coupling of the Seebeck coefficient with the electrical conductivity.

$$S = \frac{\pi^2 \cdot k_B^2}{3q} \cdot T \cdot \frac{d(\ln[\sigma(E)]}{dE}|_{E=E_F} \qquad \textit{equation 1- 14}$$

k_B, q and E_F being respectively the Boltzmann constant, the electronic charge and the Fermi energy. In [Fritzsche 1971] Fritzsche developed a general expression for semiconductors Seebeck coefficient by :

$$S_n = \frac{k_B}{q} \cdot (\frac{E_c - E_F}{k_B T} + A_n) \qquad \textit{equation 1- 15}$$

$$S_p = \frac{k_B}{q} \cdot (\frac{E_v - E_F}{k_B T} + A_p)$$

E_c, E_v, A_n and A_p being the conduction band energy, the valence band energy and constants depending on the materials. By introducing the carriers' concentration, the Seebeck coefficients are then:

$$S_n = \frac{k_B}{q} \cdot (\ln(\frac{N_C}{n}) + A_n)$$
$$S_p = -\frac{k_B}{q} \cdot (\ln(\frac{N_v}{p}) + A_p)$$

equation 1- 16

N_V and N_C denote the effective density of states in valence and conduction bands, respectively. *p* and *n* denotes the holes and the electrons concentrations.

1.2.2.3 Electrical conductivity

The electrical conductivity is the ability of a material to conduct electricity. This conduction is made through electrons, holes, or both according to the nature of the materials. This electrical conductivity results from the material's electronic lattice and its fermi level. The electrical conductivity $[Sm^{-1}]$ is defined as the product of the carriers' concentrations (*p* or *n*), their mobility μ and the electronic charge q.

$$\sigma_n = \mu_n \cdot n \cdot |q|$$
$$\sigma_p = \mu_p \cdot p \cdot |q|$$

equation 1- 17

Generally, the materials contain electrons and holes, the electrical conductivity is then the sum of the holes and electrons contributions. Moreover, the electrical conductivity is temperature-dependent. Indeed in metals, the temperature increase favorites the electrons' diffusion and the lattice vibration resulting in the mobilities reduction and in semiconductors, the temperature increase favorites an increase of the carries' concentration. In the semiconductors, the carriers' concentration increases exponentially with the band gap energy E_g and the temperature *T*: **exp (-E_g/k_B*T*).**

1.2.3 Materials choice

The materials' choice is critical to realize efficient thermoelectric harvesters. Indeed, as presented in the section II-2, the thermoelectric generator efficiency is function of the Carnot efficiency and mainly of the thermopiles' figure of merit, which is function of the materials' thermoelectric properties (equation 1-7).For a single thermoelectric material, the figure of merit becomes:

$$zT = \frac{\sigma \cdot S^2}{\kappa} \times T$$

equation 1- 18

Best materials will then be materials with the highest electrical conductivity and Seebeck coefficient and the lowest thermal conductivity. Insulators can be the good choice to satisfy criteria of high Seebeck Coefficient and low thermal conductivity, but not the criteria of high electrical conductivity. On the other hand, metals satisfy the criteria of high electrical conductivity but feature a high thermal conductivity. Therefore, the only choice left is the use of semi-conductors and these semiconductors must be highly doped according to Ioffe's works [Ioffe et al. 1959]. The optimum doping level to maximize the material's figure of merit is about($10^{19} cm^{-3}$ (figure 1-2) [Gardner 1994]. Indeed, the Seebeck coefficient decreases

quickly with the carriers' concentration increase (Seebeck coefficient proportional to the logarithm of the carriers' concentration (cf. equation 1-16)).

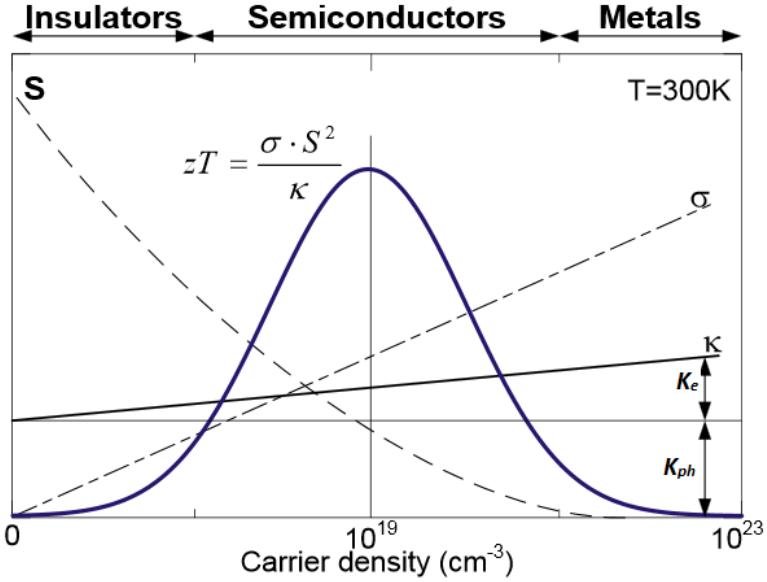


Figure 1- 2: Optimum doping level for thermoelectric applications [Gardner 1994]

In addition to a doping level around $10^{19} cm^{-3}$, a good thermoelectric material must have a band gap close to $10 \cdot k_B T$ at the working temperature T [Mahan 1989]. Indeed, small band gaps favorite carriers' mobility, but too small will favorite negative contribution from the minority carriers on the Seebeck coefficient. According to Tritt [Tritt 2000] good thermoelectric materials must also be multi-valley semiconductors with high crystal structures symmetry to produce equivalent bands in order to avoid the reduction of carriers' mobility by the increase of effective mass. The materials must be composed of elements with low electronegativity differences in order to minimize the carrier scattering by optical phonons, then the reduction of the carrier mobility [Slack 1995].

In addition to good electronic properties, the material's thermal conductivity is also an important parameter for thermoelectric application. In semiconductors, the thermal conductivity features two contributions (see section I.2.a) dominated by the phononic contribution while the electronic plays negligible role [Jin 2014] (cf. figure 1-2). The idea now is to use or develop materials with the lowest phononic contribution to the thermal conductivity. This is achievable by using materials with high phononic scattering frequency (small mean free path) and/or materials presenting low phononic group velocity by using for example materials made of heavy elements, many atoms per unit cell …

Following these guidelines, the majority of state-of-the-art materials are alloys with high carrier concentration [Ioffe et al. 1959]. High carrier concentration enable an improvement of the electrical conductivity while disrupting the phononic heat transport, resulting in a thermal conductivity reduction. These materials are alloys of bulk Bi, Te, Sb and Pb for room and moderate temperature applications and alloys of Si and Ge for high temperature applications as presented in figure 1-3 [Minnich et al. 2009].

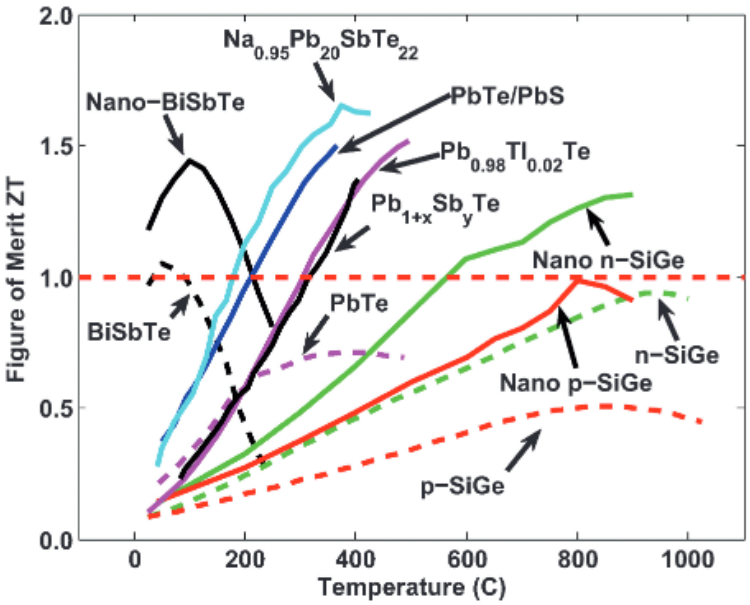


Figure 1- 3: Best thermoelectric materials [Minnich et al. 2009]

Figure 1-3 presents the state of the art (mainly from laboratories) of mostly used materials for thermoelectric harvesting and cooling. The dashes lines represent bulk materials and the solid lines, nanostructured materials. From this figure, we can see clearly that nanostructuring materials improves considerably the thermoelectric efficiency. Indeed, by nanostructuring the materials, the constraints on phonon displacements are accentuate, resulting in a supplementary thermal conduction reduction. In addition to these materials, researches carried out allow the emergence of new promising materials. The panel of thermoelectric materials is wide and keep expanding from organic materials, semiconductors to semimetals, ceramics … They can be monocrystalline, polycrystalline, 3D materials, 2D materials, etc… Hereafter are presented some of these materials.

- ***Skutterudites:*** Skutterudites materials are based on the fact that the unit cell contains empty spaces, which, can be filled by loosely bound atoms known as rattlers [H. Julian Goldsmid 2010]. These rattlers' oscillations induce the thermal conductivity reduction. The general formula of these materials are MX_3 where M is Co, Rh or Ir and X is P, As or Sb. However, they can be encountered as $V_2M_8X_{24}$ where V is the loosely bound atom that can act as dopant. They exhibits a figure of merit close to unity for 500-700K temperature range [Uher 2001].
- ***Half-Heusler***: Heusler alloys are ferromagnetic materials. The best-known Heusler material is Cu_2MnAl, it has a structure in which Cu forms a primitive cubic cell with alternative cells of Mn and Al. The half Heusler structure is the same except that half of the Cu sites are empty. They are stable at high temperature and exhibit good thermoelectric performances after doping. $Ti_{0.5}Zr0.25Hf0.25NiSn$ exhibits a figure of merit of 1-5 at 700K according to Muta et al. [Muta et al. 2006].
- ***Clathrates:*** Intermetallic compounds, they are composed of Si, Ge or Sn with guest atoms in different sites of the crystallographic structure. They are good thermoelectric materials for high temperature applications. For example $Ba_8Ga_{16}Ge_{30}$ presents a figure of merit of 1-3 at 1000K [Hou et al. 2009].
- ***Oxides:*** Oxide materials are interesting for high temperatures applications [Fergus 2012]. Indeed, they are chemically inert and potentiality stable. The most promising materials are cobalt oxide based materials used as p type materials and presenting figure of merit close to unity at temperatures around 870 K [Funahashi et al. 2000].

- ***Organic materials:*** Owing to low thermal conductivities (0.1-1 $Wm^{-1}K^{-1}$) and to the advantages to be printable, flexible and moldable, polymers [Petsagkourakis et al. 2018] are investigated for thermoelectric applications. Indeed, the amorphous morphology and their non-covalent bindings increase the phonons' diffusion and then the material thermal conductivity reduction. However, those same advantages are also drawbacks, since the amorphous structure contributes to reduce their electrical conductivity, limiting the developed generators' performances to few $nWcm^{-2}$. Nevertheless, organometallic polymers use can allow achieving few μWcm^{-2} under tenth of kelvins as temperature difference across the generator [Sun 2012]
- ***Nanostructured materials:*** Nanostructured materials for thermoelectric harvesting have been investigated first by Hicks and Dresselhaus [Hicks and Dresselhaus 1993b; Hicks and Dresselhaus 1993a]. They predicted by their simulations, a significant increase of the figure of merit for bismuth telluride nanowires with respect to the figure of merit of bismuth telluride. Low dimensional materials are used for two purposes. First, to increase the electron quantum-confinement to increase the Seebeck coefficient and second, to use the numerous interfaces (material's borders and/or impurities) to scatter preferentially and strongly the phonons, resulting into a thermal conductivity reduction [Dresselhaus et al. 2007]. Dimensionality reduction is the best example of material thermoelectric improvement by nanostructuration. Indeed, *Mahan and Sofo* demonstrated in [Mahan and Sofo 1996] that narrowest and sharpest will be the energy carriers distribution of a material, better will be the material for thermoelectric applications (cf. figure 1-4). It is important to note, that in this case, purely originates from electronic confinement without taking care of possible phononic impact due to the nano-structure itself.

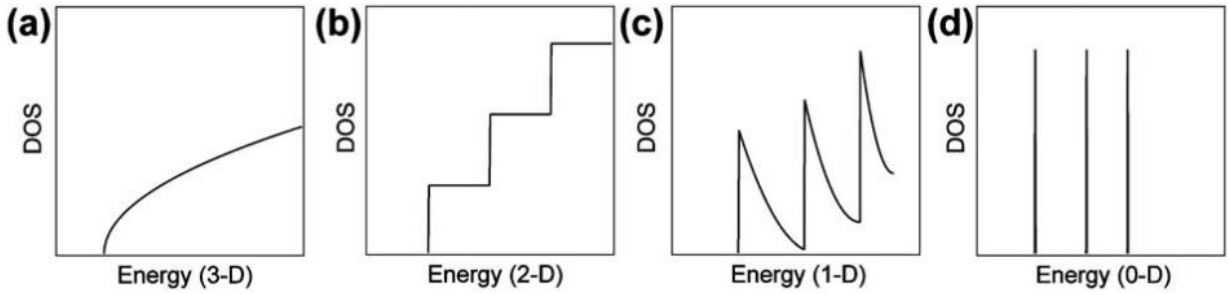


Figure 1- 4: Density of states versus energy for: Bulk material (a), 2D material (b), 1D material (c) and 0D material (d) [R. Szczech et al. 2011]

The development of low dimensionalities materials can be a key to improve the thermoelectric properties of non-conventional materials like silicon and/or silicon germanium for near room temperature applications. 2D material can be thin films or superlattices, 1D can be nanowires development and 1D quantum dots use. In the next section, we focus on the main problematic of this thesis: the use of silicon for thermoelectric harvesters' development.

1.3 Silicon for thermoelectric harvesting

Figure 1-3 tells us that for thermoelectric harvesting, we can use everything except silicon. However, silicon based thermoelectric harvesters development is a topic of high interest in the thermoelectric community. Indeed, Silicon has the advantages to be the most abundant semi-conductor material, to benefit from existing facilities and technological processes for low cost and mass production. Moreover, silicon is less environmentally harmful than most materials used currently. All these advantages make silicon a material of great interest in the thermoelectricity community. However, silicon is not used for thermoelectric harvesting because of its poor thermoelectric properties regarding other materials like Bi_2Te_3. Indeed, the

figure of merit of bulk silicon is at best 0.01at 300K where Bi_2Te_3 exhibits hundred times higher value at same temperature. This gap is mainly explained by their thermal conductivities. At room temperature, for bulk materials, the thermal conductivities of Bi_2Te_3 (~1-5 $Wm^{-1}K^{-1}$) [Goldsmid et al. 1958] and that of Si (~150 $Wm^{-1}K^{-1}$) [Asheghi et al. 1998] are separated by two orders of magnitude. Thermal conductivity reduction is therefore the principal issue to upgrade silicon as an efficient thermoelectric material.

In this chapter, we will discuss the silicon enhancement to an efficient thermoelectric material with respect to bulk silicon, it integration into a thermoelectric harvester and finally present the best state of the art room temperature thermoelectric harvesters.

1.3.1 Silicon enhancement to an efficient thermoelectric material

Silicon thermoelectric properties improvement focuses on developing nanostructured silicon, aiming to reduce the thermal conductivity with minor impact on the electrical conductivity. This is possible thanks to the recent progress in nanotechnology and the decoupling between the electronic and phononic contributions to the thermal conductivity. Indeed, The huge difference between the phonons mean free path ($\sim 200-300\ nm$)[Marconnet et al. 2013] and the electrons mean free path ($few\ nanometers$)[Weber and Gmelin 1991] for bulk silicon and at room temperature, allows the alteration of the phonons transport with minor impact on the electronic carriers. Nanotechnology then permit the realization of materials with dimensionalities lower than the phonons mean free path and/or the inclusion of impurities into the material. In such materials phonons collisions with the material borders and the impurities are favored (cf. figure 1-5).

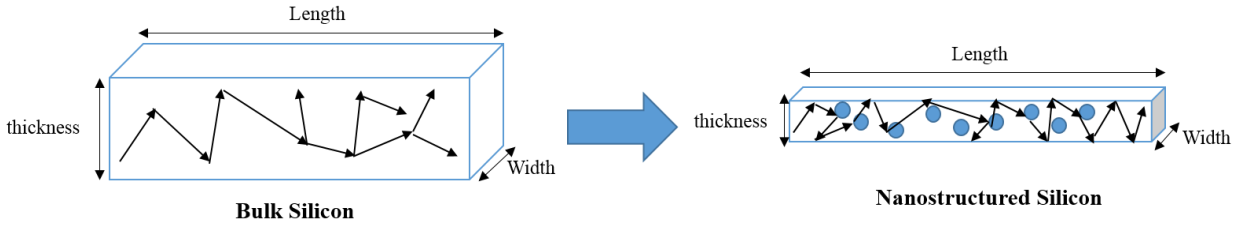


Figure 1- 5: Silicon thermal conductivity reduction methodology

Figure 1-5 shows the mechanism of the phonons scattering in the bulk silicon vs. in the nanostructured silicon. The nanostructuration increases the frequency of the phonons scattering leading by definition to the reduction of the phonons mean free path and then to the phononic contribution to the thermal conductivity, the dominant contribution [Dechaumphai and Chen 2012]. Hereafter, are given the most common nanostructured silicon based materials for thermoelectric harvesting.

1.3.1.1 Nanowires

Nanowires for thermoelectric applications have been investigated theoretically by Hicks and Dresselhaus [Hicks and Dresselhaus 1993]. They investigated the effect of 1D nanostructuration along the different axes on the different thermoelectric properties of bismuth telluride.

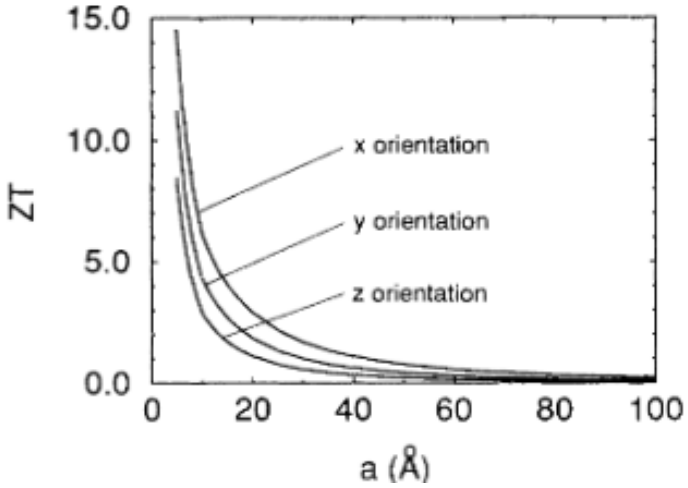


Figure 1- 6: Effect of bismuth telluride nanowires' diameter to the thermoelectric performances [30]

The results show a significant improvement of the figure of merit with the reduction of the wire diameter. The simulations predicted a figure of merit up to 15 for a bismuth telluride nanowire of 0.5nm as diameter.

Concerning silicon nanowires, the principle is the same, by developing silicon nanowires with the smallest possible diameter, the phonons borders scattering and the quantum confinement phenomenon increases, reducing then the thermal conductivity. The decisive experimental proof of thermoelectric properties improvements by silicon nanowires has been presented by Boukai et al. and Hochbaum et al entitled respectively "*Silicon nanowires as efficient thermoelectric materials"* [Boukai et al. 2008] and *"Enhanced thermoelectric performance of rough silicon nanowires"* [Hochbaum et al. 2008] both published in 2008 by nature.

By theoretical and experimental investigation, Boukai et al demonstrate the impact of silicon dimensionality (silicon nanowires) reduction and impurity addition (doping) on the thermal conductivity and the thermoelectric performances. They reported a thermal conductivity reduction up to a factor of 200 (10nm as diameter and 200K) and a figure of merit of one at 200K for a nanowire of 20nm as diameter and doped at $1 \times 10^{19}\ cm^{-3}$ (cf. figure 1-7).

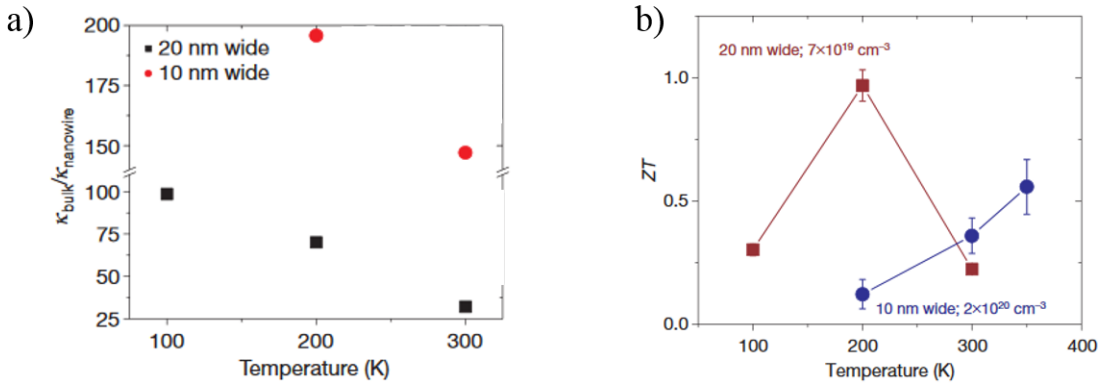


Figure 1- 7: Silicon thermal conductivity reduction (a) and thermoelectric properties enhancement (b) from Boukai et al. work [Boukai et al. 2008]

Hochbaum et al took an interest in the evolution of the different thermoelectric properties from a bulk material to a nanowire. In figure 1-8, is represented the evolution of the thermal conductivity from bulk to 50nm diameter nanowire (Figure 1-8-a) and the power factor and figure of merit values with respect to the temperature for a 52nm (Figure 1-8-b) diameter nanowire. The results depict that the power factor is not significantly affected by the

nanostructuration, while the thermal conductivity is a two order of magnitude lower at 300K (Figure 1-8-a). Finally, it shows that it is possible to achieve a zT of 0.6 at 300K for a silicon nanowire of 52nm diameter (Figure 1-8-b). This result demonstrates that the dimensionality reduction has a bigger impact on the phonon conduction rather than the electronic density of states.

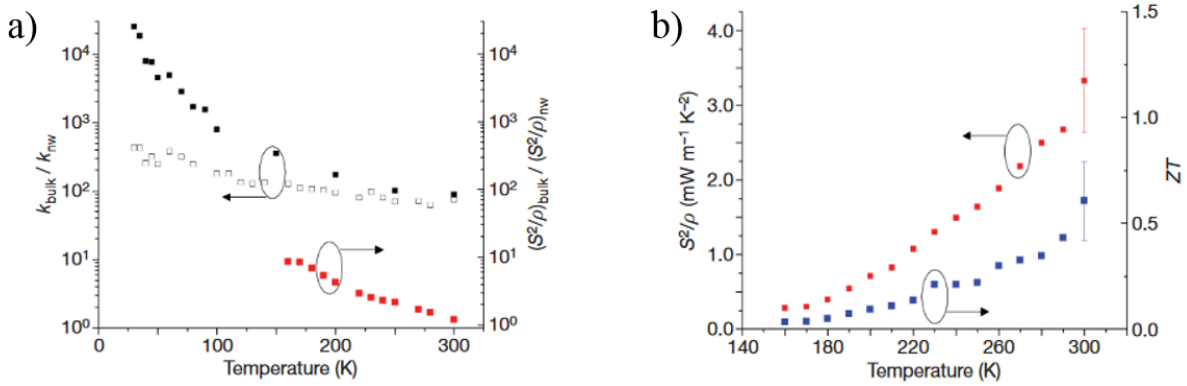


Figure 1- 8: Thermal conductivity reduction by developing a 50nm diameter silicon nanowire, open squares (highly doped silicon), black squares (intrinsic silicon) and the power factor variation (a). Power factor variation and figure of merit of a 52nm diameter silicon nanowire (b).

As a complement to Boukai et Hochbaum works, Lim et al investigated in [Lim et al. 2012] the effect of silicon nanowires surface roughness on the thermal conductivity. The results show a thermal conductivity reduction down to 5 $Wm^{-1}K^{-1}$ The work shows also that the roughness has more impact on thermal conductivity reduction than the wire diameter.

1.3.1.2 Phononic engineering

In 1952, Sondheimer investigated the effect of the thickness reduction on the silicon electrical conductivity [Sondheimer 1952] in thin planar films. The Casimir-Ziman model is the equivalent for phononic transport. Equation 1-19 gives the thin membrane thermal conductivity with respect to bulk:

$$\kappa_{membrane} = \kappa_{bulk}\left(1 - \frac{3(1-p)}{2\delta}\right)\int_1^{\infty}\left(\frac{1}{\xi^3} - \frac{1}{\xi^5}\right)\frac{1-\exp\left(-\frac{t}{\Lambda}\xi\right)}{1-pexp\left(-\frac{t}{\Lambda}\xi\right)}d\xi \qquad \textit{equation 1- 19}$$

where t is the thickness, Λ the phonon mean free path at 300K and p the fraction of phonons specularly reflected at the boundaries. The model developed by Sondheimer for Λ=300nm at 300K and p assumed to be 0 is validated by experimental measurements for several silicon thickness (cf. figure 1-9). Silicon thinning allows for a significant reduction of the thermal conductivity down to ~25 $Wm^{-1}K^{-1}$ for a 20nm thick silicon membrane [Liu and Asheghi 2004] ~9 $Wm^{-1}K^{-1}$ for a 9nm thick silicon membranes [Chávez-Ángel et al. 2014] . This incredible reduction offered by a thickness reduction down to tenths of nanometers, opens the way to the integration of thin silicon film to industrial converters compatible with the CMOS technology.

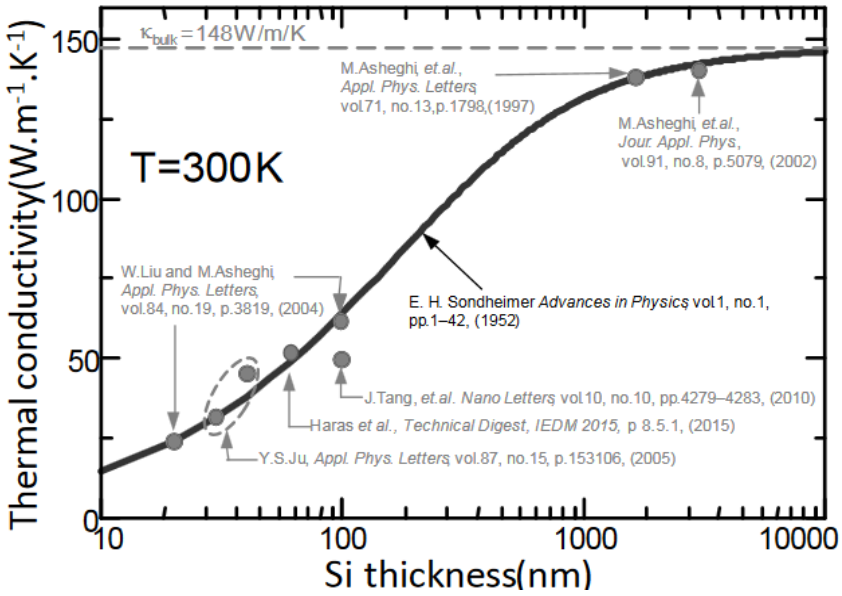


Figure 1- 9: Silicon thermal conductivity versus thickness. The Fuchs-Sondheimer model (line) is used to fit values reported in the literature (circles) [Haras et al. 2016].

The silicon thinning allows a significant reduction of the thermal conductivity but it remains much higher than the bismuth telluride thermal conductivity or amorphous silicon. The amorphous value constitutes a commonly admitted lower limit to the thermal conductivity of any material [Cahill et al. 1992].The key to downscale further the thermal conductivity is to couple the thinning with a phononic engineering solution. This solution consists on patterning the thin film with regular and periodic features. The idea here is to play on the phonons' frequency and wavelength to reduce their contribution to the thermal conductivity [Maldovan 2013]. Indeed, phonons, quantum of lattice vibrations carry sound for frequencies from few Hz to hundreds of GHz and heat for frequencies over hundredth of GHz to hundredth of THz (cf. figure 1-10).

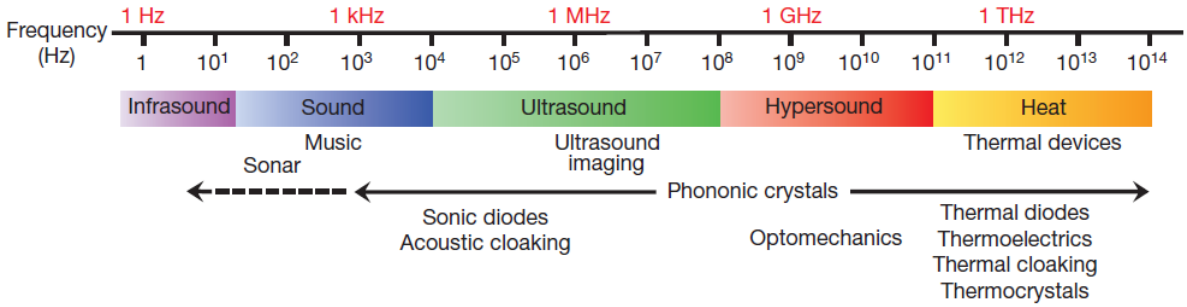


Figure 1- 10: Phononic spectrum [Maldovan 2013]

The heat being carried at high frequency and on short distances, it can be controlled by nanostructuring the thin silicon film (figure 1-11). The network of periodic holes presented in figure 1-11 allows by the nanoscale dimensions of the holes and the pitch between the holes to act like diffuser for THz phonons and then to reduce the thermal conductivity. Such network is called "Phononic Crystal". At room temperature, the phonon coherence length is very short (few nm) such that the transport regime is purely diffusive and the detailed geometry (periodic or not) of the hole pattern has no impact on the thermal conductivity reduction. In that extent, the term "Phononic Crystal" should not be understood here as a media which phonon transmission is coherently impacted by a periodic structure but rather a material maximizing

the diffusion of phonons in order to reduce thermal transport. "Phononic or Phonon Engineering" replaces then the term "Phononic Crystal".

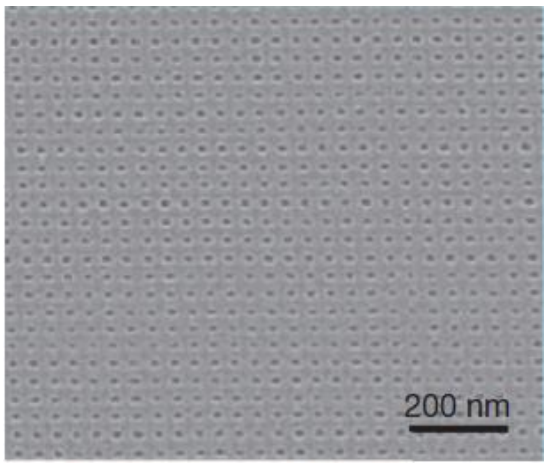
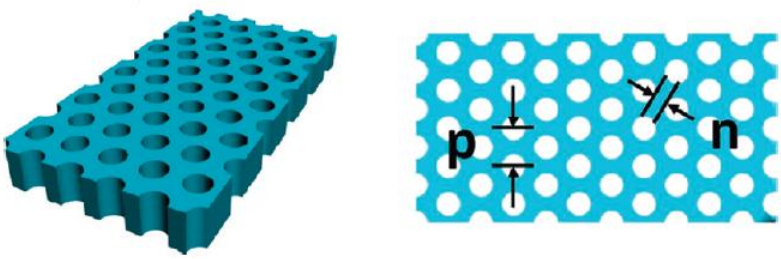


Figure 1- 11: Periodic holes network ("Phononic Engineering") for heat transport management [Maldovan 2013]

Phononic engineering is not just a concept. It has been studied both by theoretical and experimental means. Reference works being, those carried out by *Tang et al.* [Tang et al. 2010], *Yu et al.* [Yu et al. 2010], *Hopkins et al* [Hopkins et al. 2011] and *Dechaumphai and Chen.* [Dechaumphai and Chen 2012]. In [Tang et al. 2010], *Tang et al* investigated the thermal efficiency of a 100nm thick silicon membrane patterned with several phononic engineering pattern as presented in figure 1-12.



	avg. pitch, p (nm)	avg. neck, n (nm)	avg. porosity, φ (%)	κ ($Wm^{-1}K^{-1}$)
nonholey			0	50.9 ± 2.0
nonholey*			0	47.6 ± 1.7
350-pitch	350	152	~35	10.23 ± 0.44
140-pitch	140	59	~35	6.96 ± 0.34
55-pitch	55	23	~35	2.03 ± 0.07
55-pitch*	55	23	~35	1.73 ± 0.06

*Figure 1- 12: Holey silicon geometry and the measured thermal conductivity at 300K [Tang et al. 2010], * denotes doped samples (Boron $5 \cdot 10^{19} cm^{-3}$)*

All the samples presented in Figure 1-12 have the same thickness. Beyond, the benefit of phononic engineering for thermal conductivity reduction, these results show that the pitch and the neck size between holes are key parameters to further reduce the thermal conductivity and thus potentially improve the thermoelectric figure-of-merit. In addition, the doping has an impact on the thermal conductivity. Indeed, by doping we add impurities into the material, which will increase the probability of phononic scattering and reduce the thermal conductivity. Finally, from this work, we can report a thermal conductivity reduction down to $1.73\ to\ 2.03\ Wm^{-1}K^{-1}$, almost close to bismuth telluride thermal conductivity ($1.5\ Wm^{-1}K^{-1}$) and to the amorphous value of silicon ($\sim 1.8\ Wm^{-1}K^{-1}$ [Wada and Kamijoh 1996]). The figure of merits of the doped samples are

consigned in the figure 1-13. We can observe again clearly the benefit of phononic engineering over the plain silicon membrane. Moreover, the largest reduction of the thermal conductivity allows reaching a figure of merit at 300K of 0.4 (at least 40 times higher than the bulk silicon figure of merit).

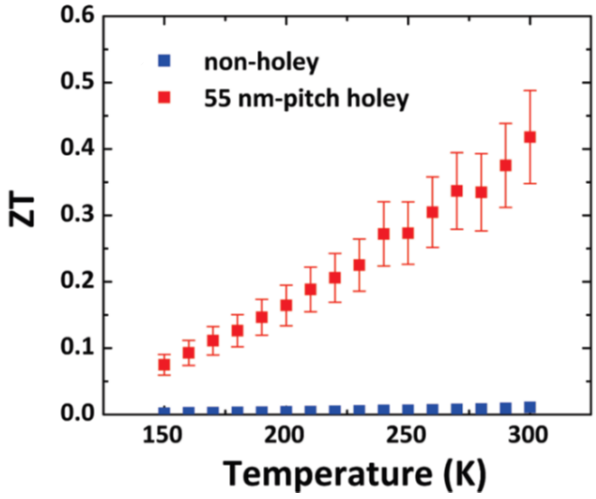


Figure 1- 13: Thermoelectric figure of merit comparison of the plain membrane versus the membrane with phononic engineering (Boron $5 \cdot 10^{19} cm^{-3}$) [Tang et al. 2010].

Yu et al. [Yu et al. 2010] studied the thermal conductivity of silicon thin film (TF), an e-beam lithography device (EBM), silicon nanowire (NWA) and silicon nanomeshes (NM). The samples thicknesses are close from 20 nm for the nanowires to 25nm for the thin films.

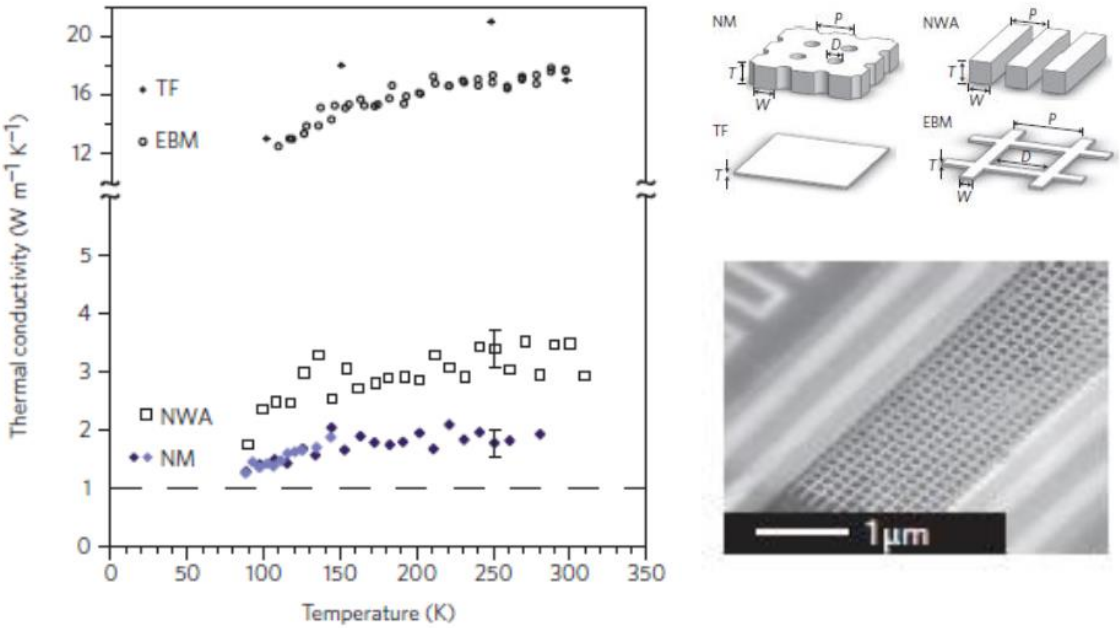


Figure 1- 14: Left: Thermal conductivity measurements on different nanostructures: thin film (TF), electron beam lithography device (EBM), nanowires (NWA) and nanomeshes (NM). Right top: the nanostructures sketch and right bottom: SEM picture of the nanomeshes [Yu et al. 2010].

Silicon nanowires and nanomeshes are the samples exhibiting the lowest thermal conductivities (figure 1-14). The nanomeshes exhibit at 300K a thermal conductivity of $1.8\, Wm^{-1}K^{-1}$, closer to what obtained by *Tang et al.* and the bismuth telluride thermal conductivity.

Both *Yu et al.* and *Tang et al.* achieved a huge thermal conductivity reduction. However, like with the nanowires, beyond the thermal conductivity reduction another concern is to improve or at least to avoid degrading the electrical properties. In this same paper, *Yu et al.* studied the impact of the silicon nanostructuration by phononic engineering (nanomeshes NM) on the electrical conductivity. The result shows a reduction of the electrical conductivity due to phononic engineering, however less important for doping levels close to $10^{19} cm^{-3}$ (cf. figure 1-15). Moreover, compared to the thermal conductivity reduction, the electrical conductivity reduction is less important. These results demonstrate that besides the high thermal conductivity reduction, phononic engineering affects to a lesser extent the electrical conductivity with respect to the bulk's electrical conductivity.

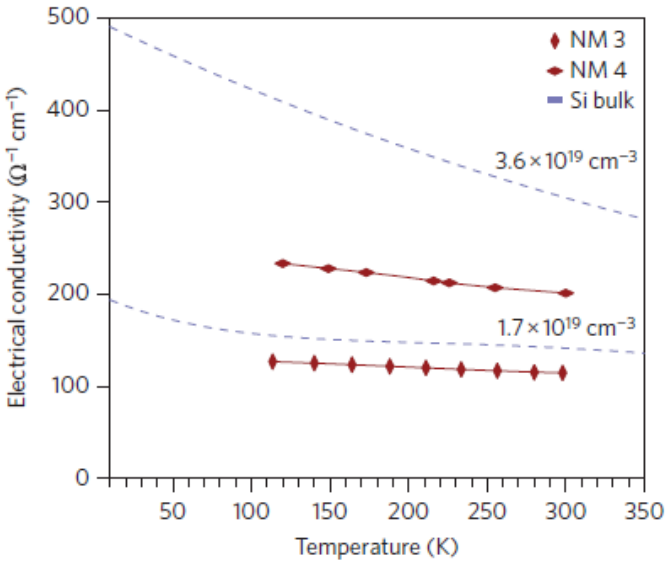


Figure 1- 15: Left: Doped bulk silicon electrical conductivity versus nanomeshes electrical conductivity at the same doping level [Yu et al. 2010]

Hopkins et al. [Hopkins et al. 2011] investigated besides the thermal conductivity reduction thanks to, the thermal transport processes in such microstructure. They achieved a thermal conductivity of 4.81 $Wm^{-1}K^{-1}$ for a 500nm thick phononic membrane with 300nm diameter and 600nm pitch Holes network. It is also argued in this work that the thermal conductivity reduction in these structures is not only due to the incoherent phononic propagation (boundary scattering), but also to the coherent phononic transport.

Dechaumphai and Chen [Dechaumphai and Chen 2012] developed a model based on a partial coherent effect in phononic engineering in order to understand the outstanding thermal conductivity reduction achieved by *Tang et al.* [Tang et al. 2010], *Yu et al.* [Yu et al. 2010] and *Hopkins et al* [Hopkins et al. 2011]**.** They used Boltzmann transport equation (BTE) and finite difference time domain (FDTD) modeling to investigate the experimental findings presented earlier. The modeling is based on wave like or particle like nature of the phonons depending on their mean free path and the characteristic length of the medium in which they propagate. Indeed, if the phonon mean free paths are lower than the medium (here phononic crystal) characteristic length, the phonons are considered as particles and their transport properties are described by the Boltzmann transport equation (BTE). The propagation regime is then considered incoherent. On the other hand, if the phonons mean free paths are higher than the medium characteristic, considered as waves, the finite domain time domain (FDTD) describe them. The propagation mode is not only incoherent (boundary scattering) but also coherent.

In figure 1-16 are presented the BTE model and the developed model to explain the low thermal conductivities observed. From this figure, we can observe that the BTE model itself

cannot explain the lowest thermal conductivities obtained experimentally. However, the model in this paper thanks to the FDTD modeling fits quite well the results from [Tang et al. 2010; Yu et al. 2010], especially for small neck sizes. It confirms also that the neck size is a key parameter to maximize the efficiency of the phononic engineering.

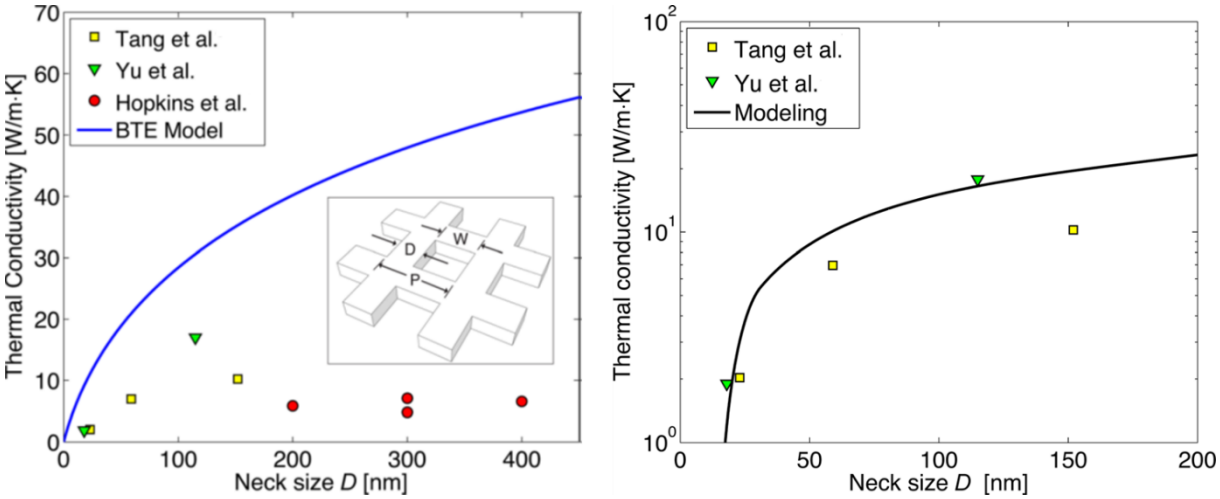


Figure 1- 16: BTE (particles) model versus experimental measurements (left) and the coherent (waves) model developed versus experimental measurements (right) [Dechaumphai and Chen 2012]

The results reported earlier demonstrate that phononic engineering present a huge opportunity to the silicon thermoelectric properties improvement. Indeed, they allow a significant thermal conductivity reduction with minor impact on the electrical conductivity. Figure 1-17 depicts the literature state of the art of thermal conductivity reduction with respect to the Sondheimer model and also our state of the art [Haras et al. 2016] represented by the result of *Haras et al.*

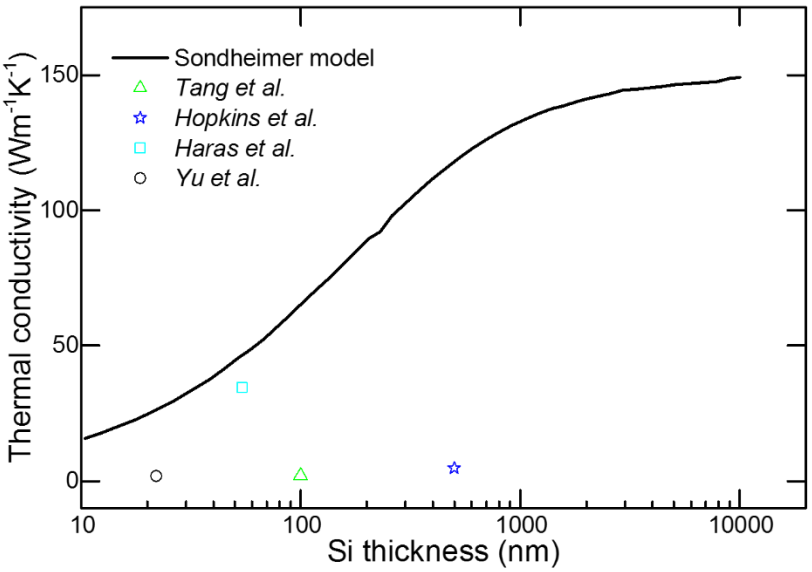


Figure 1- 17: Summary of phononic engineering thermal conductivity reduction with respect to the Sondheimer model

Like silicon nanowires and phononic engineering, Porous silicon and polycrystalline silicon exhibit low thermal conductivities. Indeed, randomly and intertwined pores or polysilicon can permit significant reduction of thermal conductivity down to $0.1\,Wm^{-1}K^{-1}$ [Gesele et al. 1997; He et al. 2011; Marconnet et al. 2012; Song and Chen 2004]. However, these low thermal conductivities are not exploitable for thermoelectric harvesting, since the electrical conductivity is also considerably degraded with respect to bulk single crystal silicon.

1.3.2 Silicon based micro-harvesters state of the art

In addition to silicon thermoelectric properties, the thermoelectric research community investigated the integration of these improved materials into a thermoelectric harvester demonstrator. It is the case of *Ziouche et al.* who developed a planar polysilicon based thermoelectric harvester (cf. figure 1-18) [Ziouche et al. 2017]. The developed thermoelectric harvester, composed of 560 thermocouples exhibits a maximal output power of 12.3 μWcm^{-2} for 2 Wcm^{-2} as input power.

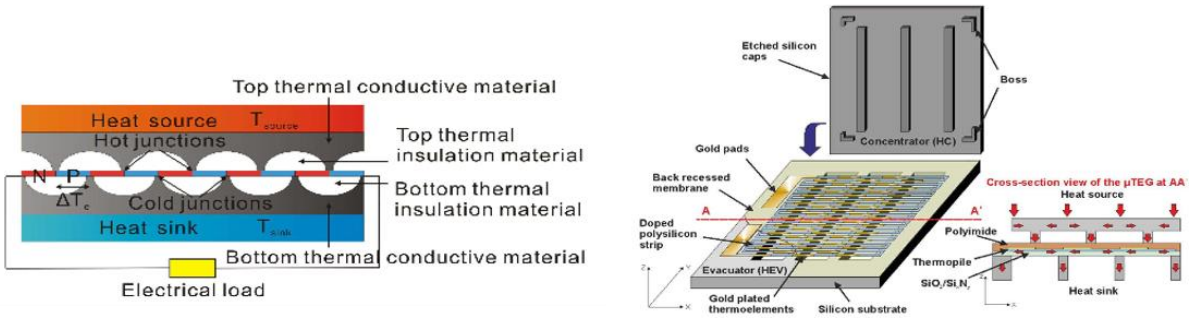


Figure 1- 18: Planar polysilicon thermoelectric harvester [Ziouche et al. 2017]

In the same perspective than *Ziouche et al. Xie et al.* presented in [Xie et al. 2010] a CMOS compatible thermoelectric harvester. The novelty of this work realized before *Ziouche et al.* lies on the void cavities on top and down of the thermoelectric elements (cf. figure 1-19). These cavities aim at a better management of the thermal gradient through the thermoelectric elements by insulating them from the silicon substrate. In this work, it is reported an output power of 1-3µW for a temperature difference across the thermoelectric harvester of 5K and an open-circuit voltage of 16.7V for a square cm TEG.

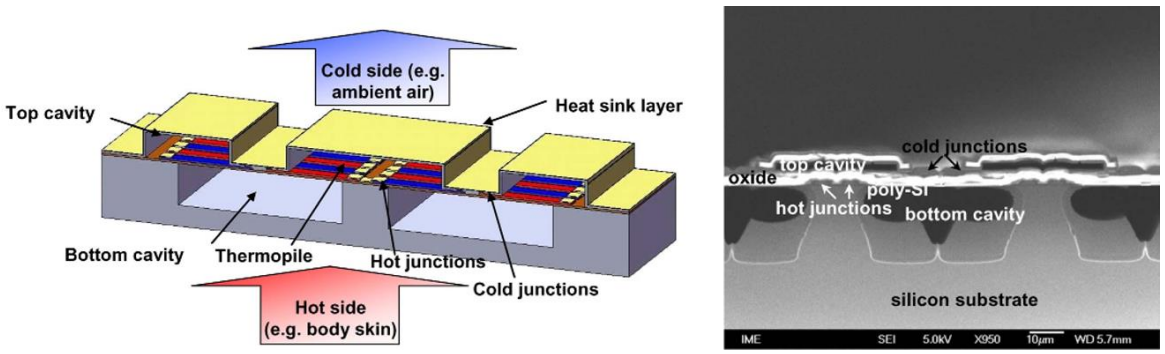


Figure 1- 19: Schematic of the Xie et al. thermoelectric harvester (left) and SEM view of the stacking [Xie et al. 2010]

Perez-Marin et al. [Perez-Marín et al. 2014] also developed a planar-based thermoelectric harvester proof of concept, but this time with single crystal silicon (cf. figure 1-20). Their proof of concept exhibits 4.5 µW/cm^2 under 5K as produced power density. This work is of great interest for us because it is in the same framework of the thesis. Indeed, this thesis aims to develop phonon engineered single crystal planar thermoelectric harvester proof of concept.

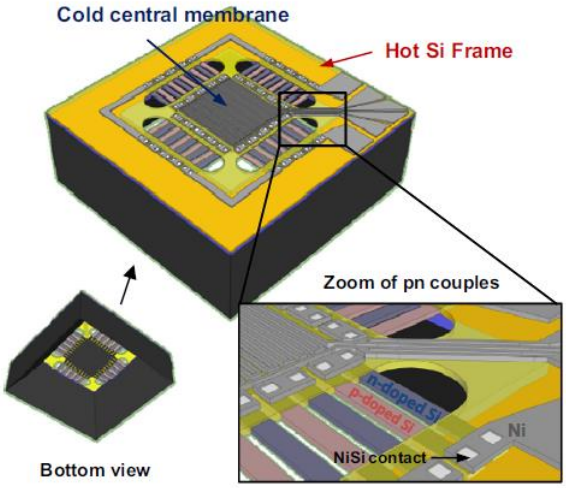


Figure 1- 20: Schematic of the Perez-Marin et al. single crystal planar thermoelectric harvester [Perez-Marín et al. 2014]

Besides planar silicon membranes, silicon nanowires are the other upgrade silicon used for silicon thermoelectric harvesting demonstration. In 2011, *Li et al.* [Li et al. 2011] demonstrated the integration of silicon nanowires into a thermoelectric harvester. Gaps between nanowires are filled with low temperature oxide. The developed thermoelectric harvester exhibits an output power of 1-5 nW at 0.12K for 25mm^2 generator. In 2012, they replaced the low temperature oxide by polyimide, the developed TEG exhibits then an output power of 470nW but for a temperature difference across the generator 70K.

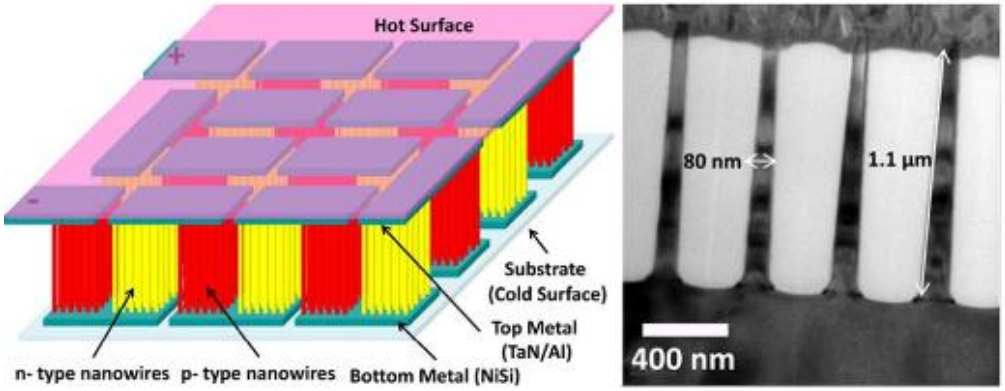


Figure 1- 21: Schematic of the Li et al. thermoelectric harvester (left) and SEM view of the silicon nanowires [Li et al. 2011]

Davila et al. [Dávila et al. 2012] investigated also the integration of silicon nanowires into a thermoelectric harvester demonstrator (Figure 1-22), unlike *Li et al.* the silicon nanowires are integrated in planar architecture. The hot source is simulated by Joule effect thanks to a metallic heat/thermometer. The design is done such a way that the all platform has a low thermal mass, allowing a rapid cooling. With the demonstrator, they manage to harvest 1.5 $mWcm^{-2}$ by providing a temperature difference across the TEG of 300K.

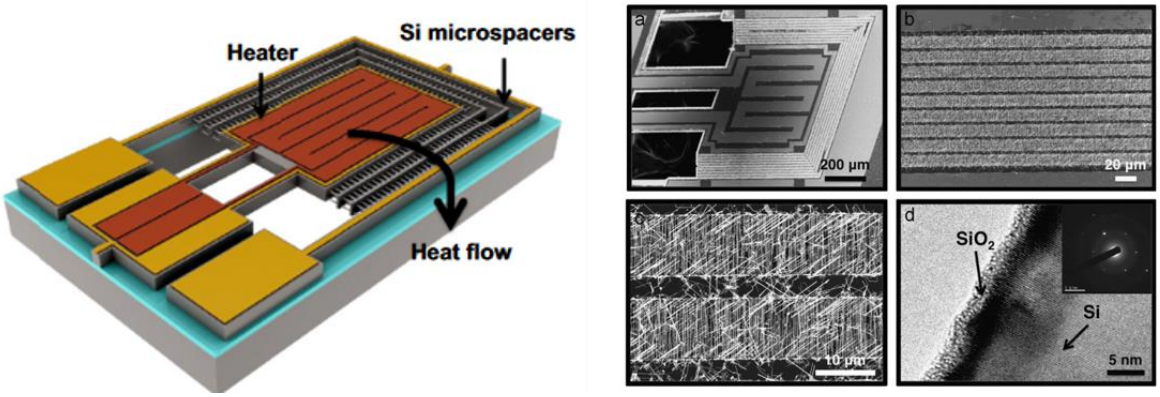


Figure 1- 22: Davila et al. Silicon nanowires based TEG proof of concept. (a) Design of the demonstrator. (b) SEM pictures of the TEG and details [Dávila et al. 2012].

1.3.3 Silicon germanium based micro harvester

Silicon germanium with an intrinsic lower thermal conductivity than silicon is also of interest for the development of near room temperature applications micro thermoelectric harvesters. The best example of silicon germanium use for thermoelectric harvesting is the development of the "radioisotope thermoelectric generator" for space aircrafts. Indeed, Si-Ge has been and is used as thermoelectric material for harvesting the heat produce by the decay of radioactive material in space aircrafts thanks to it good thermoelectric behavior at high temperatures. However, since then, works have been done to develop miniaturized and near room temperature compatible silicon germanium thermoelectric harvesters. This is supported by the works of *Wang et al.* [Wang et al. 2009; Wang et al. 2011]. In the first paper, the authors presented a silicon based thermoelectric harvester for human body applications (figure 1-23). They suspended the thermocouples (like presented earlier) in order to maximize the thermal resistance of the harvester. Secondly, they narrowed the thermoelectric couples also for increasing the thermal resistance but they kept the width of the junction larger as possible in order to reduce the contact resistance at this interface. From this device, they claim for a square cm harvester an average voltage of 12.5V/K and an output power of 26nW/K^2. Moreover, when the harvester is worn on a wrist, it delivers 150mV.

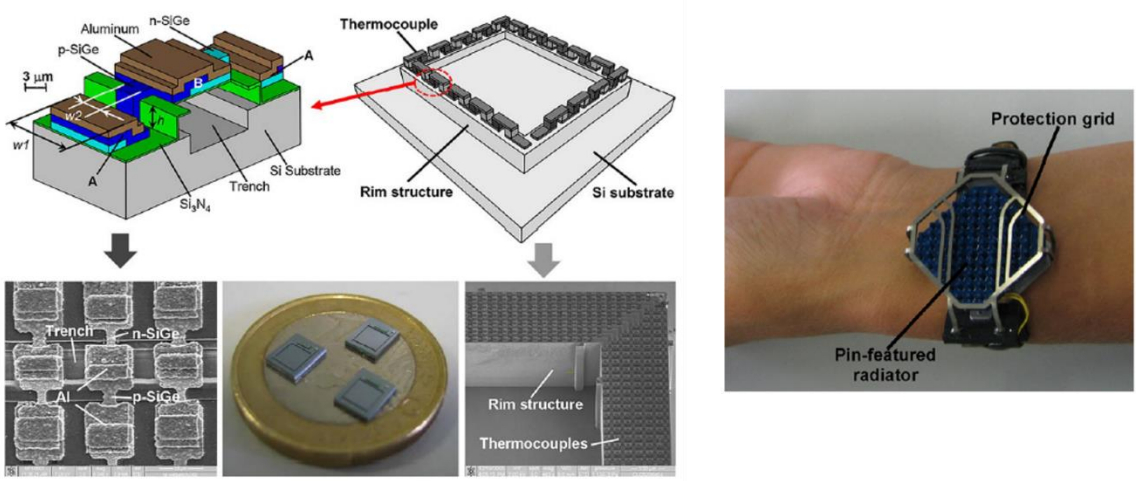


Figure 1- 23: Silicon germanium based thermoelectric harvester for human body applications [Wang et al. 2009]

In the second paper, the authors investigated the integration of in-plane poly silicon germanium and poly silicon into a planar and vertical thermoelectric harvester architecture (Figure 1-24). They claim a maximal open circuit voltage of 95 mV/K and an output power for a load match of 2.34 nW/K^2.

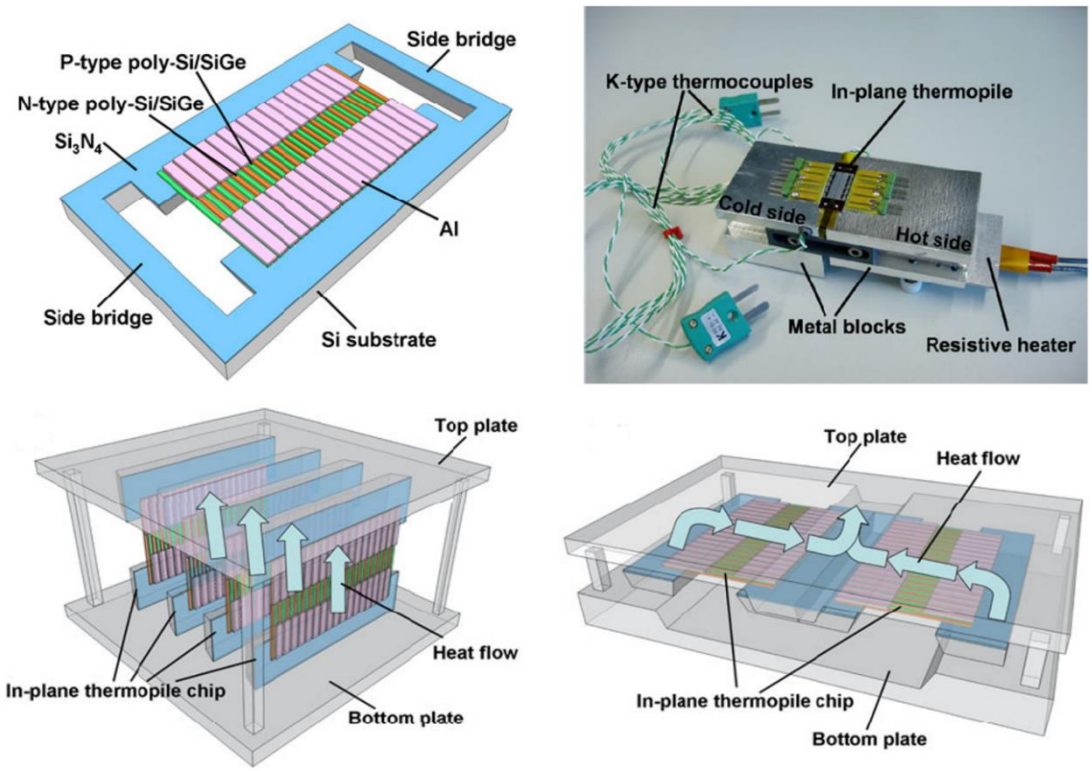


Figure 1- 24: In-plane poly silicon and poly silicon germanium integration into a thermoelectric harvester investigation [Wang et al. 2011]

In addition, to thin films and nanowires use, another way to improve the thermoelectric properties of silicon and silicon germanium for near room temperature applications is the use of quantum dots inclusion (0D material). *Savelli et al.* from CEA LITEN investigated the development and thermoelectric properties characterization of Si-Ge based quantum dots superlattices [Hauser et al. 2012; Savelli et al. 2015]. Figure 1-25 presents the realization process of titanium nano-islands incorporation into Si-Ge layers to form quantum dots superlattices (QDSL).

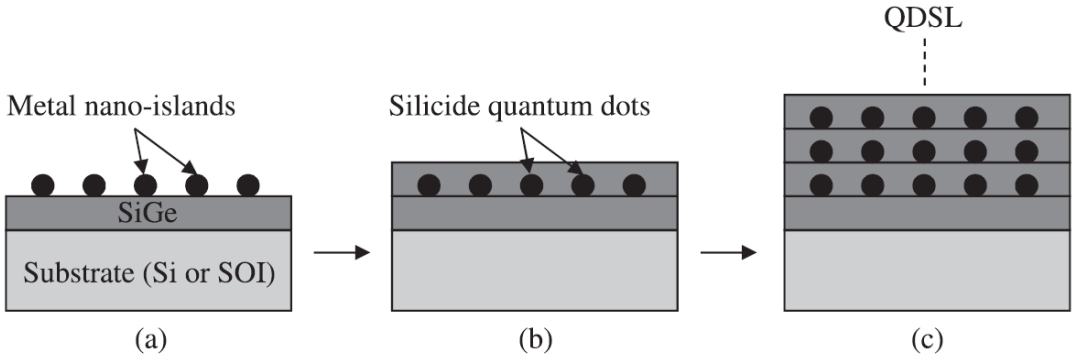


Figure 1- 25: Si-Ge based quantum dots superlattices realization process. (a) Meatal (Ti in this case) nano island growth on Si-Ge thin film, (b) Si-Ge layer deposition to encapsulate the meatal nano island and (c) repetition of steps (a) and (b) to create superlattices of quantum dots [Hauser et al. 2012]

The authors studied the impact of the quantum dots superlattices on the thermoelectric properties with respect to those of the Si-Ge thin films. The study is realized for both monocrystalline and polycrystalline QDSLs.

	Monocrystalline			Polycrystalline		
	n ($10^{19}cm^{-3}$)	μ ($Cm^2V^{-1}s^{-1}$)	κ ($Wm^{-1}K^{-1}$)	n ($10^{19}cm^{-3}$)	μ ($Cm^2V^{-1}s^{-1}$)	κ ($Wm^{-1}K^{-1}$)
QDSL	3.2±0.2	73±5	6.8±0.7	2.8±0.2	18±1	4.6±0.5
Si-Ge ref	3.2±0.2	56±3	8.5±0.8	4.4±0.2	13±1	4.2±0.4

Table 1- 3: comparison of electronic mobility and thermal conductivity for Mono and poly crystalline Ti-QDSL in Si-Ge with respect to Si-Ge thin film properties.

From table 1-3, we can observe modifications of mobilities and thermal conductivities by including nano Ti islands in to silicon germanium thin films. However, we can observe that, the monocrystalline QDSLs exhibit better improvement mainly in terms of thermal conductivity reduction, because in the polycrystalline case, the grain boundaries phonons scattering in the Ti nano islands. To complete the study, the authors investigated the power of the developed QDSLs with respect to that of the Si-Ge thin film. The results presented in figure 1-26 show clearly an improvement of the power (better for the monocrystalline QDSL). This study confirms again the importance of nanostructuring to use non-conventional material for thermoelectric harvesting.

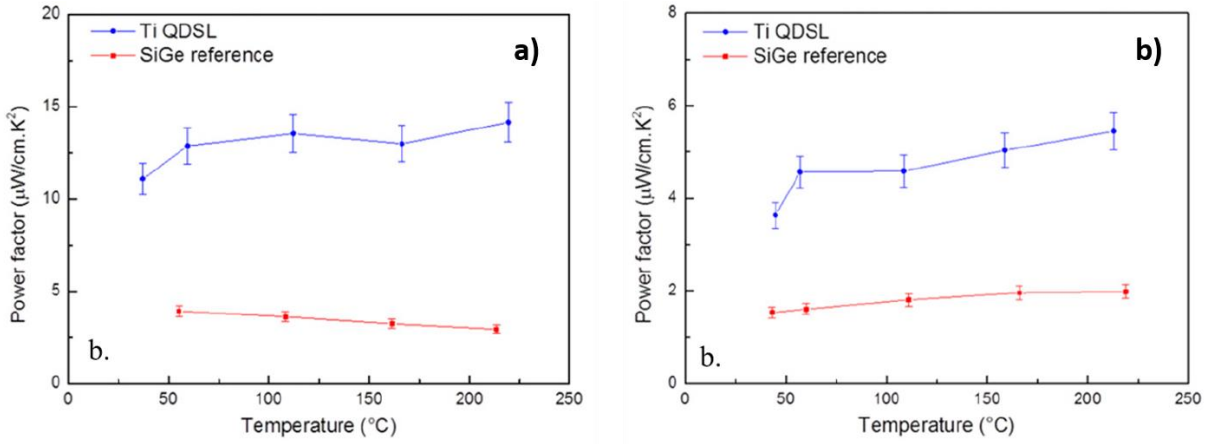


Figure 1- 26: Thermoelectric power factors of monocrystalline QDLS (a) and Polycrystalline QDSL (b) with respect to that of the Si-Ge thin film [Savelli et al. 2015]

1.4 Best micro-harvesters for near room temperature applications

Not surprisingly, the state of the art thermoelectric harvesters for near room temperature applications are made of bismuth telluride alloy (the best thermoelectric material for such temperature range). In 1999, Seiko developed an embedded micro thermoelectric harvester capable of power supplying a wristwatch. This embedded thermoelectric harvester was made of bismuth telluride alloy, chosen for it excellent thermoelectric properties. The microscale thermoelectric harvester was made of 104 thermocouples in vertical architecture (cf. figure 1-27). They estimated a voltage generation of 20mV/K and an output power of 22.5μW. Moreover, they observed that the thermoelectric harvester generates more than what is necessary to power supply the wristwatch, it can also power supply a battery. By this work, Seiko demonstrated the ability of thermoelectric harvesting to power supply everyday life electronic devices.

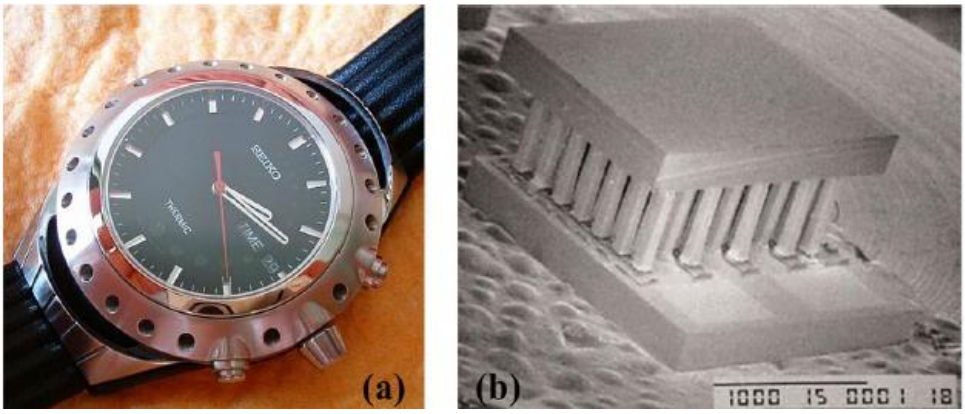


Figure 1- 27: Seiko's wristwatch (a). The embedded thermoelectric harvester developed by Seiko (b) [Kishi et al. 1999]

Since the demonstration of Seiko of the use of thermoelectric harvester to power supply electronic devices, thermoelectric harvesting attracts more interest. In 2003, *Snyder et al.* [Snyder et al. 2003] present Bi, Sb an Te alloy based thermoelectric harvester developed by a MEMS like process (Figure 1-28a). This realization process has the advantages to be simple, low and compatible with batch production, it can therefore participate to reduce the TEG production cost. The same year *Li et al.* [Li et al. 2003] proposed to combine MEMS technology and materials processing in order to develop densely aligned fine scale and high aspect ratio thermocouples (Figure 1-28b). No thermoelectric performances were reported.

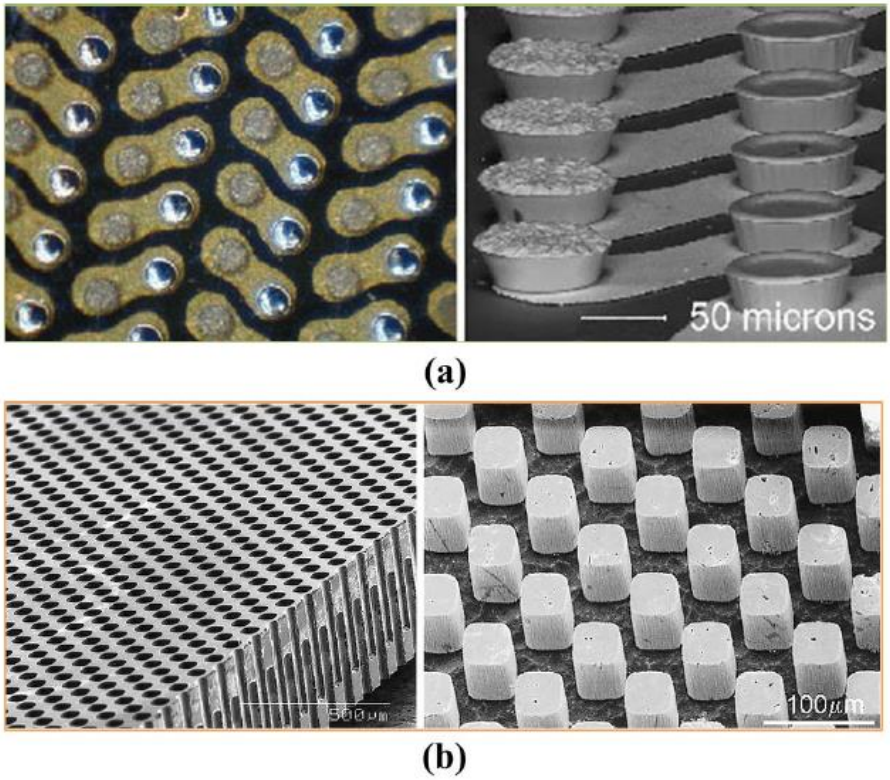


Figure 1- 28: Snyder et al. proposed thermoelectric harvester architecture (a) [Snyder et al. 2003]. Li et al. High aspect ratios and fine-scale thermocouples (b) [Li et al. 2003]

Since Seiko, *Bottner et al.* [Bottner 2002; Bottner et al. 2004; Bottner 2005; Bottner et al. 2007] carried out remarkable works on bismuth telluride based thermoelectric harvester. Indeed, these works proposed the first thermoelectric devices based on bismuth telluride alloys, which can be manufactured with regular thin film and micro technology. Moreover, these works

led to the manufacturing and sale of those considered as the state of the art commercial micro thermoelectric harvesters.

The adventure began in 2002 by the work presented at the 21st international conference on thermoelectricity (ICT) [Bottner 2002]. In this work, the authors discussed the fabrication of bismuth telluride based microscale thermoelectric harvesters and coolers by means of MEMS like process. Indeed, they study the deposition of bismuth telluride layers on silicon substrates by means of physical vapor deposition (PVD), metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) before patterning them with usual MEMS patterning processes. The demonstrator resulting from this work is made of 12 thermocouples occupying 1-12 mm^2.

The work continues with the integration of more thermocouples in the generators. In 2004, they described clearly the realization process of a bismuth telluride based microscale thermoelectric harvester in [Bottner et al. 2004]. Basically, the process is as follows:

- From two-bulk silicon wafer, the thermoelectric materials are deposited (p type on one and n type on the other).
- Both *p* and *n* type thermoelectric material are etched and structured by reactive ion etching.
- *p* and *n* chips are cut from the p and n wafers and associated (a p type chip with its complementary n type chip), forming a thermoelectric generator.

Metallic contact are realized, to firstly associate in series the p and n type materials and secondly to allow the extraction of the thermoelectric performances. Figure 1-29 depicts the association of the p and n chip to form a thermoelectric generator (a), the p or n chip on a full wafer scale (b) and a close up view of p and n chip with the thermoelectric element shape.

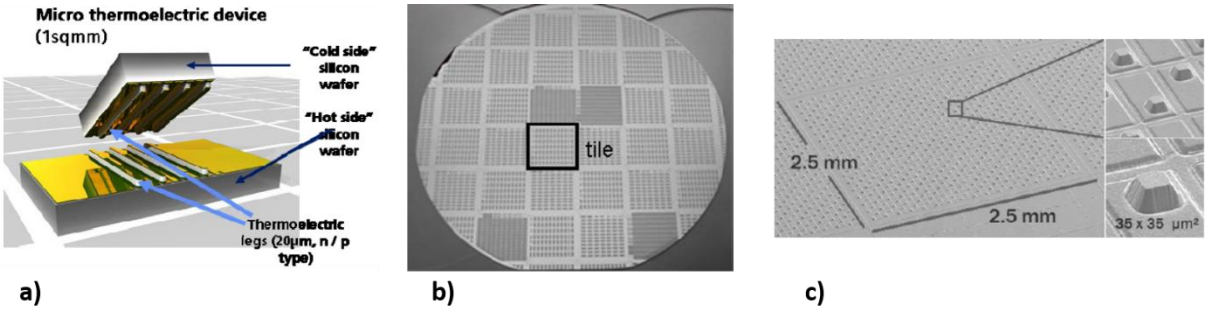


Figure 1- 29: Bottner et al. proposed thermoelectric harvester architecture. (a) Exploded view of the generator, (b) wafer scale view of thermoelectric element and (c) close up view of on cell of the wafer.

In 2005, the authors published the thermoelectric harvester performances [Bottner 2005]. The generator is made of bismuth telluride alloy following the realization process presented earlier. The generator is made of 140 thermocouples associated electrically in series and thermally in parallel, they occupy a surface of 2.5x2.5mm^2. In Figure 1-30 is represented the maximum output power of the 140 thermocouples TEG with respect to the temperature difference across the generator. With such TEG, it is possible to harvest 1-5 mW for a temperature difference of 5K, opening the possibility to power supply autonomous and standalone sensors.

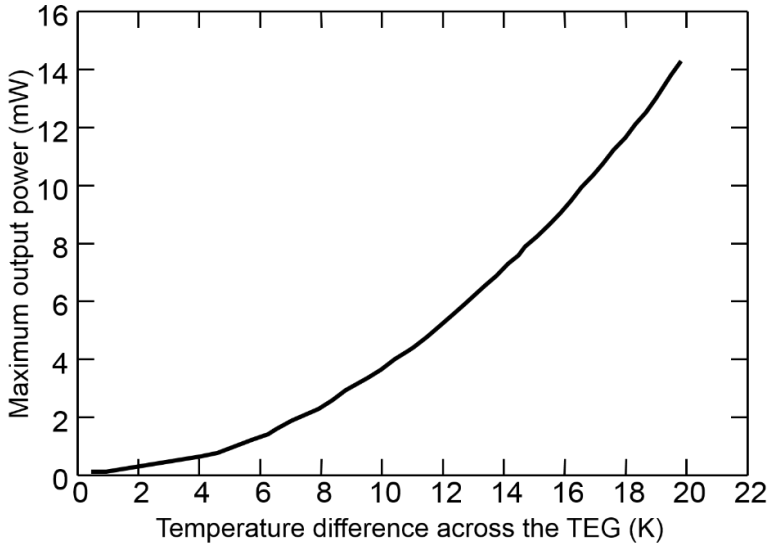


Figure 1- 30: Maximum output power from 2.5x2.5mm² bismuth telluride based thermoelectric harvester. Reproduced from [Bottner 2005]

These performances are obtained for thermoelectric harvester subject to a constant temperature difference (with the help of a high capacity heat sink for example). In the last paper [Bottner et al. 2007] published in 2007, the authors interested in the effect of the generator cooling condition of the performances (Figure 1-31). In the figure "without convection", means cooling with natural convection without heat sink help and "with convection" cooling with natural or forced convection with heat sink help. The results plotted in figure 1-31 shows clearly, that for an optimum running conditions, the generator must be associated to a heavy heat sink and/or with a forced convection situation to help it better manages the thermal gradient.

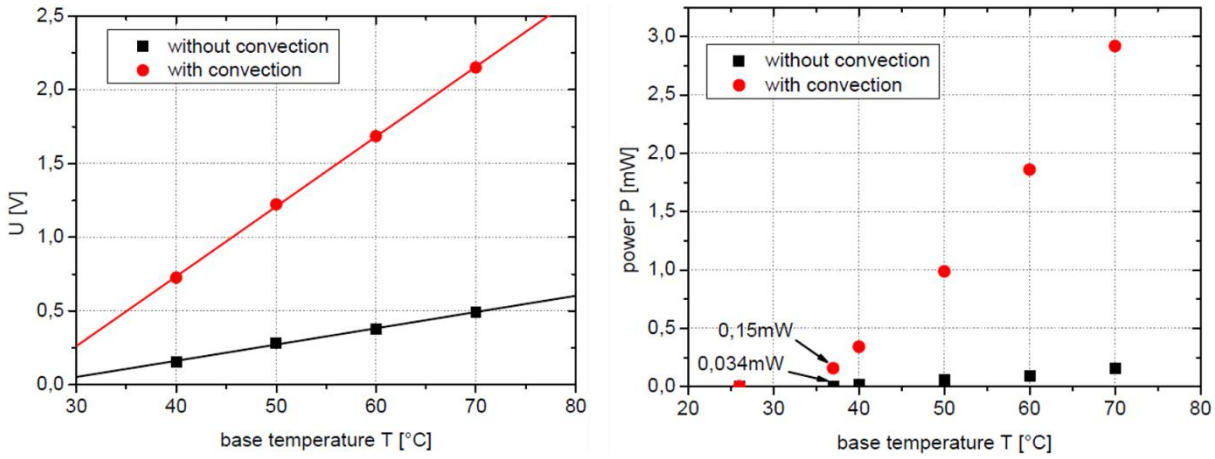


Figure 1- 31: Bismuth telluride based microscale thermoelectric harvester performances under natural convection without heat sink and under convection with heat sink help. Left, the thermoelectric voltage and right the thermoelectric power

The authors developed a technology for manufacturing microscale bismuth telluride thermoelectric harvesters with an integration up to 100 of thermocouples per mm² [Bottner et al. 2007]. The devices microscale dimensions allow their easily incorporation into a setup for converting waste heat into electricity. The performances also exceed amply what is needed to power supply autonomous sensor nodes. Moreover, the developed realization process is compatible with mass production. The excellent performances and the compatibility with mass production encouraged the authors industrialized their prototypes. They then create MicroPelt to commercialize the microscale thermoelectric harvesters as well as coolers from their

researches. The devices commercialized by MicroPelt are considered as state of the microscale thermoelectric generator for our work for three reasons. Firstly, the generators are made of the best thermoelectric material for near room temperature applications. Secondly, the harvested powers are more than enough to power supply autonomous nodes. Finally, the devices are commercialized.

Bismuth telluride is mostly integrated in vertical-architecture thermoelectric harvester. By doing so, bulky materials are used, allowing then to minimize the harvester's electrical resistance but the drawback is then the thermal gradient management (cf. figure 1-31-right). *Tainoff et al.* presented in [Tainoff et al. 2019] the development of a planar bismuth telluride based thermoelectric harvester. They used 300nm thick bismuth telluride membranes deposited on a silicon nitride layer and both suspended for a better thermal insulation (cf. figure 1-32). In this work, the thermopiles are both electrically in series and parallel to increase both current and voltage. After characterization, the harvester exhibits 60nW as produced power for 0.5 cm^2 harvester, then 120nW/cm^2 under 6.8 K of temperature difference across the thermopiles. The performance is lower than that of the harvester from Micropelt because of especially the higher electrical resistance due to the use of 300nm thick membranes.

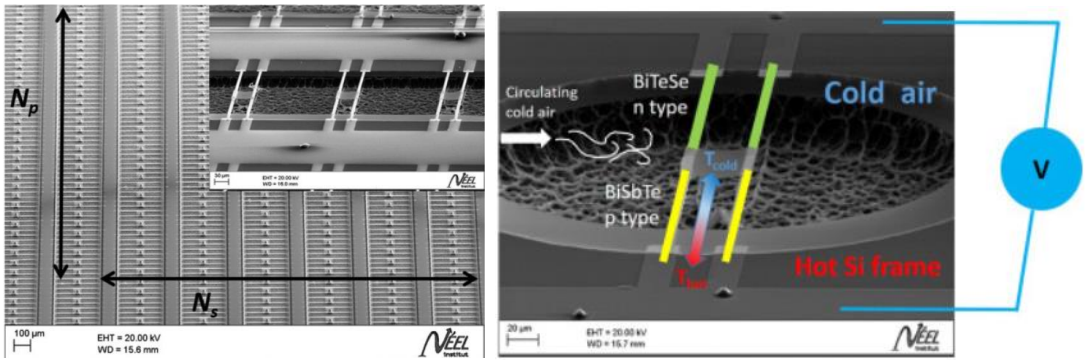


Figure 1- 32: Planar bismuth telluride based microscale thermoelectric. Left: SEM view of some thermocouples and right: focus one thermopile and details of the characterization set-up.

Conclusion

This first chapter dealt with the problematic of energy harvesting technologies development rose by the indispensable [Nordrum 2016] blooming of wireless sensor networks (WSN) and internet of things (IoT). Then, the thesis detailed the theory behind thermoelectric harvesting and reviewed the different methodologies for the silicon thermoelectric properties improvement thanks to its thermal conductivity reduction. Finally, the first chapter reviewed the microscale thermoelectric harvesters' state of the art, with a focus on the silicon (material of interest for this thesis) and bismuth telluride alloys (best thermoelectric materials) based harvesters.

Figure 1-31 sums up the micro-harvesters' performances presented earlier. It is noticeable that the best performances are achieved by Bi-Te based micro-harvesters and the silicon-based micro-harvesters exhibit comparable performances. The Bi-Te's low thermal conductivity allow the use of bulky materials for the harvesters' realization thus allow the development of low electrical resistances harvesters' while the silicon harvesters exhibits higher electrical resistances due to the dimensionality reduction indispensable to reduce their thermal conductivity. The silicon based harvesters' state of the art being made of polysilicon or nanowires, we expect the demonstrators that we will realize to exhibit higher performances because they will be made of single crystal and lager silicon membranes (answer in the fourth chapter).

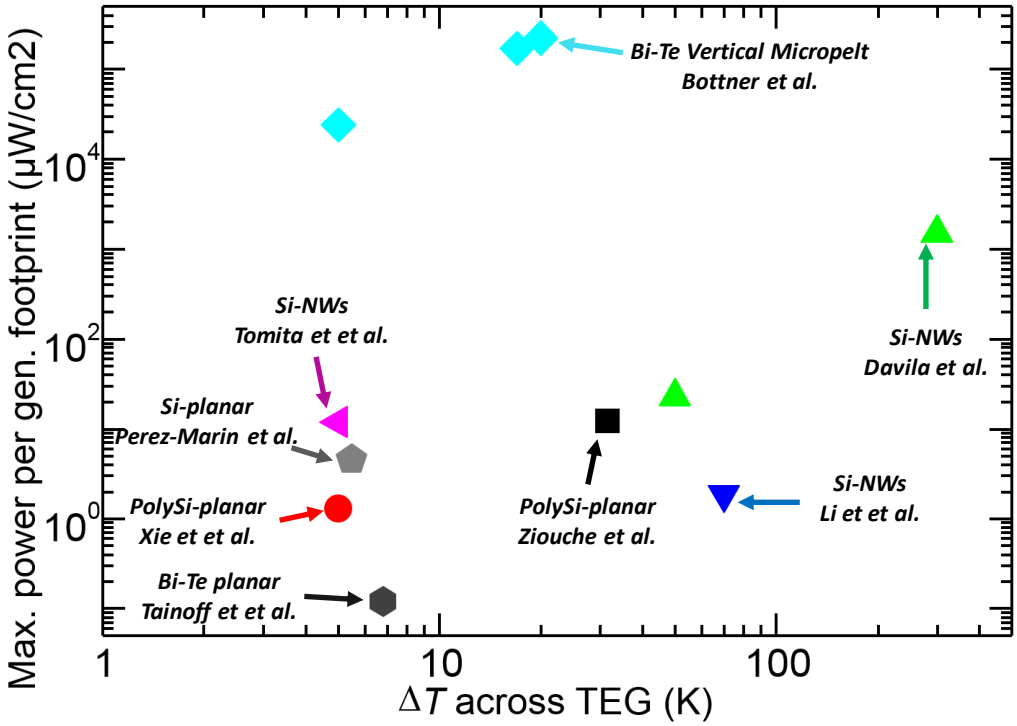


Figure 1- 33: State of the art micro-harvesters' maximum output power per generator footprint with respect to the temperature difference across the generators. [Ziouche et al. 2017; Xie et al. 2010; Dávila et al. 2011; Bottner 2005; Tomita et al. 2018; Li et al. 2011; Perez-Marín et al. 2014]

Chapter 2: Modeling studies of the Si based thermoelectric harvester with respect to a commercial state-of-the-art

Abstract

In the previous chapter, we reviewed the need of energy harvesting solutions rose by the blooming of the so-called Internet-of-Things (IoT) and Wireless Sensor Nodes (WSN), before exposing the issue of silicon based thermoelectric harvesting development. In the previous chapter, we observed also that silicon is very far from being the best material for thermoelectric harvesting. However, thanks to its advantages to be the most common semi-conductor and compatible with **CMOS** technologies, researchers through the world investigate the improvement of the silicon thermoelectric properties. From those researches, we can report noticeable improvement on silicon thermoelectric properties, leading to the development of some demonstrators. Despite the excellent results from those works, the state of the art micro thermoelectric harvester remains, a bismuth telluride based thermoelectric harvester from the company Micropelt.

In this chapter, we will deal with the theoretical study of the silicon based thermoelectric harvester demonstrator that we will develop. This study aims to:

- Estimate the performances that we can expect from such generators
- Determine the optimal dimensions for the demonstrators' realization
- Benchmark our Si based TEG with the commercial based thermoelectric harvester
    - Understand the benefits and the drawbacks of the Si based TEG with respect to the commercial one.

The modeling is done by means of FEM (Finite Element Modeling). Analytic models are also developed in order to:

- Explain the physical observations from the FEM with mathematic relationships
- Carry out quickly the modeling (once analytic and FEM are equivalent) for heavy computations.

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2.1 Silicon TEG modeling

2.1.1 The model

The silicon thermal conductivity (main obstacle to silicon based micro thermoelectric harvester – cf. chapter 1) reduction is done by coupling silicon thinning to phononic engineering (the next chapter deals with the realization process) (figure 2-1).

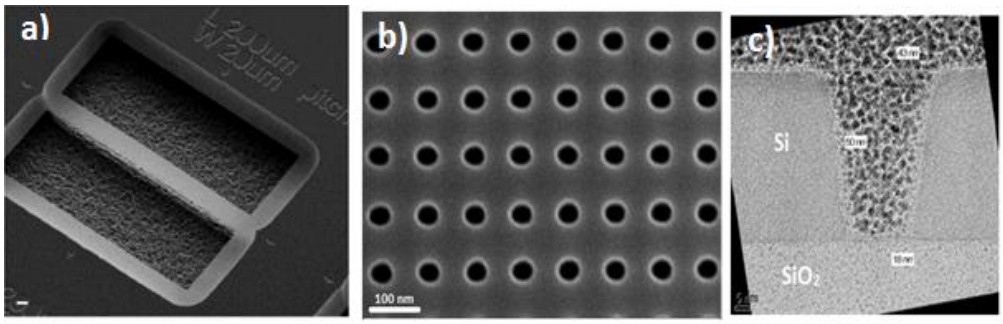

Figure 2- 1: SEM pictures of (a) Silicon thin film coupled to phononic crystal, (b) close up view of the phononic crystal network and (c) TEM cut of phononic hole before membrane suspension.

This thermal conductivity reduction method imposes the development of a planar architecture thermoelectric harvester (cf. figure 2-2) instead of the common vertical architecture. The thermoelectric elements are called membranes in this configuration. Like for the vertical architecture, the TEG is made of *n* and *p* doped membranes electrically in series and thermally in parallel held between two silicon substrates.

In the center of the platform, platinum and silicon nitride layers are deposited respectively to short-circuit the p-n junction and insulate the platinum from the silicon substrate. Both ends of the membranes are anchored to the second silicon substrate for heat dissipation purposes. The heat source is introduced to the center of the platform so that heat is discharged through the membranes to the bulk silicon anchors. The platinum layers are deposited on the ends of the membranes. The current flow is ensured between the *p* and *n* membranes by an electrical shunt in platinum.

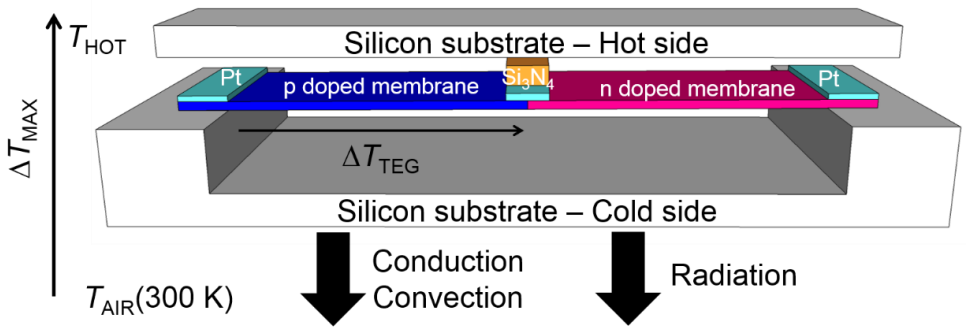

Figure 2- 2: Silicon based thermoelectric generator model and the TEGs modeling conditions

Modeling are performed as follows:

- The hot source is assumed to be at a constant temperature (T_{HOT}) between 300 and 400K
- The heat is routed to the cold substrate by thermal conduction through the silicon membranes till the cold ends which are anchored to the wafer (cf. figure 2-3).
- Vacuum is assumed in the cavity between the two-silicon substrates (no conducto convection). Thermal radiation is also neglected in the cavity due to the small gap.
- Two thermal conductivities are considered :
  - 34.5 $Wm^{-1}K^{-1}$ our last published value [Haras et al. 2016]

- 2.03 $Wm^{-1}K^{-1}$ the lowest value from the literature [Tang et al. 2010]

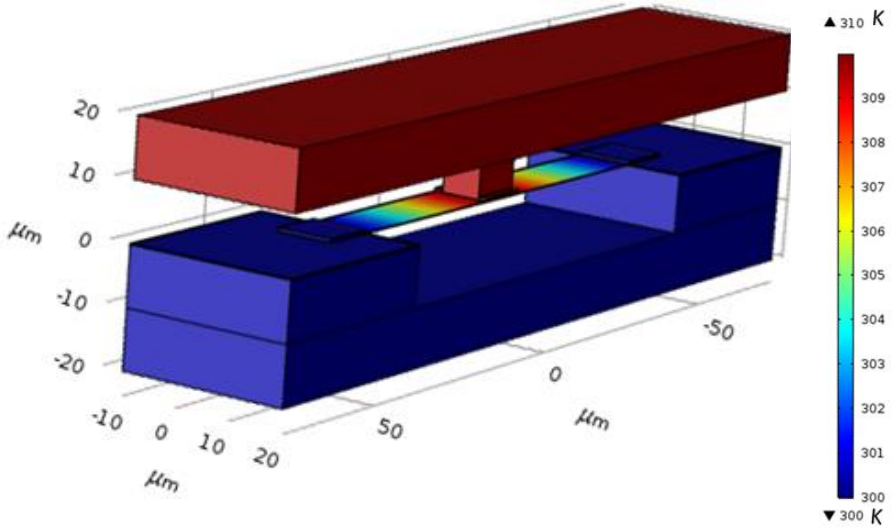

Figure 2- 3: Thermal gradient across the planar Si membranes thermoelectric generator

- Conducto-convective cooling with a transfer rate h is used to model the heat sink with three typical situations (cr. Table 2-1). This conducto convection transfer rate h defines the use or not of a heat sink and the efficiency of that heat sink (if it is used).

h=10Wm^{-2}K^{-1}	***h=100Wm^{-2}K^{-1}***	***h=1000Wm^{-2}K^{-1} and more***
Cooling without heat sink	Cooling with a small capacity heat sink	Cooling with a higher capacity heat sink

Table 2- 1: conducto-convection transfer rate and the physical meaning

2.1.1.1 Thermal conduction

The thermal conduction is the thermal energy transport from hot sources to cold sources of a same medium or of mediums in direct contact. This thermal transport method is typical of heat transfer in solid materials.

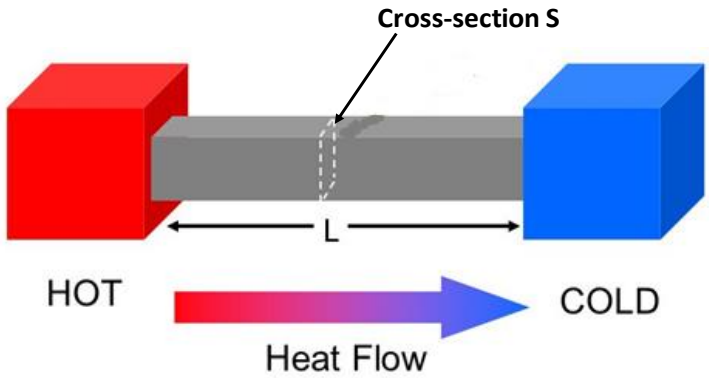

Figure 2- 4: Thermal conduction method

The Fourier law characterizes the heat flux density:

$$\vec{\varphi} = -\kappa \cdot \overrightarrow{grad}(T)$$

$$\varphi(Wm^{-2}) \approx \frac{\kappa \cdot (T_H - T_C)}{L}$$

Equation 2- 1

2.1.1.2 Conducto-convection

Convective heat transfer occurs in fluids. It is due to the movements of molecules within fluids, it takes place through advection and/or diffusion. When, solid medium and fluids at different temperatures are in contact, the heat is transferred both by conduction (from the solid medium to the fluid) and by convection (in the fluid), we then talk about conducto-convection in the fluid.

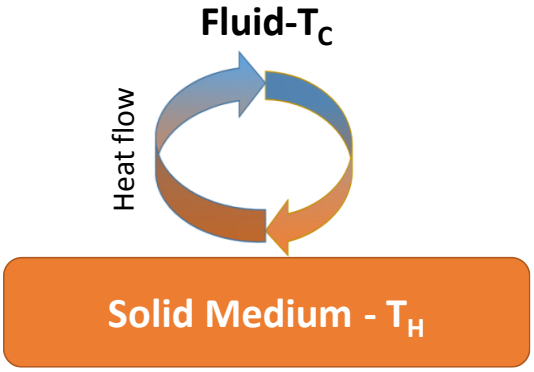

Figure 2- 5: Thermal conducto-convection transfer

The heat flux from a conducto-convection is given by:

$$\varphi(W \cdot m^{-2}) = h \cdot (T_H - T_C)$$

Equation 2- 2

h being the conducto-convection transfer rate.

2.1.1.3 Thermal radiation

The thermal radiation is an electromagnetic radiation produced by thermal motion of charged particles in matter. Any medium with a temperature higher than the absolute zero emits heat in the form of radiation.

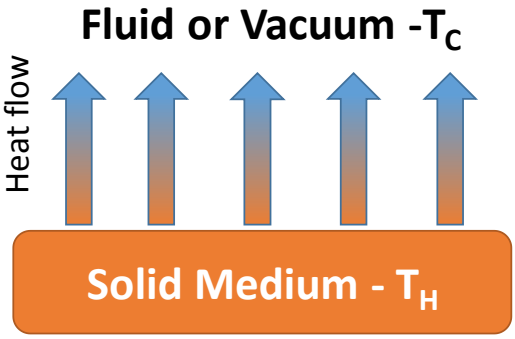

Figure 2- 6: Thermal radiation

The heat flux is given by the Stefan-Boltzmann formula:

$$\varphi(W \cdot m^{-2}) = \varepsilon\sigma \cdot (T_H^4 - T_C^4)$$

Equation 2- 3

ε and σ being respectively the emissivity of the material and the Stefan-Boltzmann constant ($5.67.10^{-8}Wm^{-2}K^{-4}$).

2.1.2 Finite Element Modeling

Finite Element Modeling (FEM) is used and the thermoelectric coupling is based on the coupled resolution of carriers and heat transport equations. The current densities are given by the non-isothermal drift diffusion model [Haras et al. 2014]and transport is assumed to be governed by majority carriers.

$$\overrightarrow{J_\alpha}(T) = \sigma_\alpha(T) \cdot \left[\vec{E} + |S_\alpha(T)| \cdot \vec{\nabla}(T)\right] \qquad \textit{Equation 2- 4}$$

σ_α, S_α and $\vec{E}$ being the electrical conductivity, the Seebeck coefficient and the eventual applied electrical field through the generator.α stands for n or p depending on the doping area.

$$\sigma_\alpha(T) = q.\mu_\alpha(T).\alpha(T)$$

$$S_n(T) = -\frac{k_B}{q} \cdot [1.5 + \ln(\frac{N_C(T)}{n(T)})]$$

$$S_p(T) = \frac{k_B}{q} \cdot [1.5 + \ln(\frac{N_V(T)}{p(T)})]$$

$$n(T) = \frac{N_D}{2} + \sqrt{\frac{N_D^2}{4} + n_i^2(T)} \qquad \textit{Equation 2- 5}$$

$$p(T) = \frac{N_A}{2} + \sqrt{\frac{N_A^2}{4} + n_i^2(T)}$$

$$n_i(T) = \sqrt{N_C(T) \cdot N_V(T)} \cdot \exp(-\frac{E_G(T)}{2 \cdot k_B \cdot T})$$

$$N_C(T) = 2 \cdot \left(\frac{2\pi \cdot k_B \cdot T \cdot m_e}{h^2}\right)^{3/2}$$

$$N_V(T) = 2 \cdot \left(\frac{2\pi \cdot k_B \cdot T \cdot m_h}{h^2}\right)^{3/2}$$

k_B being the Boltzmann constant ($1.38 \cdot 10^{-23}J/K$), q the elementary charge ($1.62 \cdot 10^{-19}C$) and h the Planck constant ($6.62 \cdot 10^{-34}$ m^2kg/s. p(T) and n(T) are the hole and electron densities. $N_V(T)$ and $N_C(T)$ denote the effective density of states in valence and conduction bands, respectively. The doping level in the thermoelectric legs is set to $10^{19}cm^{-3}$ for which the figure-of-merit is optimal [Hao et al. 2010], represented respectively by N_D and N_A for the n and p doped legs. S_p and S_n being the p and n doped Seebeck coefficient, given by the Mott law [Fritzsche 1971] defined in the previous chapter. $E_G(T)$ is the energy gap of the semiconductors. σ_α the electrical conductivities while μ_α are mobilities of the p and n regions respectively given by the Arora model [Arora et al. 1982] as follows :

$$\mu_n(N_D,T) = \mu_{min} \cdot \left(\frac{T}{300}\right)^{\alpha} + \frac{\mu_{max} \cdot \left(\frac{T}{300}\right)^{\beta}}{1 + \frac{N_D}{N_{ref} \cdot \left(\frac{T}{300}\right)^{\gamma}}}$$

Equation 2- 6

$$\mu_p(N_A,T) = \mu_{min} \cdot \left(\frac{T}{300}\right)^{\alpha} + \frac{\mu_{max} \cdot \left(\frac{T}{300}\right)^{\beta}}{1 + \frac{N_A}{N_{ref} \cdot \left(\frac{T}{300}\right)^{\gamma}}}$$

Material	μ_{min} ($cm^2/V/s$)	μ_{max} ($cm^2/V/s$)	N_{ref} (cm^{-3})	α	β	γ
n-type Si	88	1252	$1.432 \cdot 10^{17}$	-0.57	-2.33	2.546
p-type Si	54.3	407	$2.67 \cdot 10^{17}$			

Table 2- 2: silicon maximal and minimal mobilities and coefficients for the Arora model [Arora et al. 1982]

The finite element modeling is performed thanks to the Software "COMSOL Multiphysics". This software allows the modeling by the finite element method (Solving partial derivatives equations), the modeling of physical phenomenon in components or devices.

2.1.3 Equivalent analytic modeling

The Si membranes low dimensions impose the use of a very tight mesh, resulting in the computational time significant increase. So, to the sake of computational time reduction and mainly to the sake of a better understanding of the modeling studies, an analytic model is developed in parallel to the FEM.

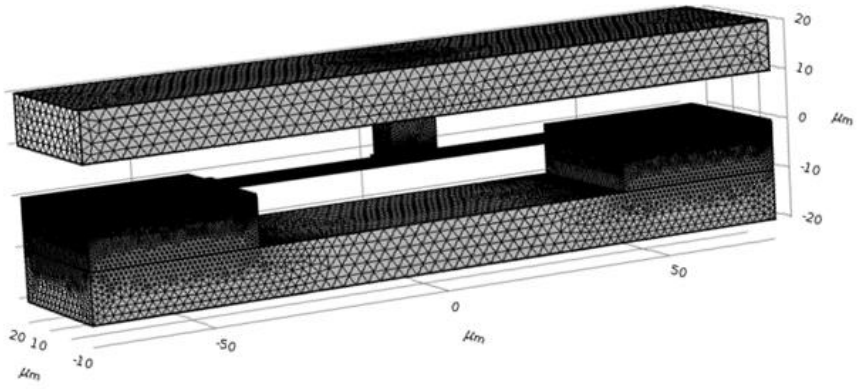

Figure 2- 7: Si membranes thermoelectric generator modeling mesh

The analytic model uses a thermal resistance equivalent circuit (figure 2-8.) to calculate the heat flux propagating across the TEG for a given temperature difference. Then, the maximum output power P_{MAX} is calculated across the thermoelectric legs under the condition of electrical impedance matching.

$$P_{MAX} = \frac{V^2}{4 * R_{el}}$$
$$V = (S_p - S_n) \cdot \Delta T \qquad \textit{Equation 2- 7}$$
$$R_{el} = \sum \frac{\rho_{legs} \times L_{legs}}{A_{legs}} + \sum \frac{\rho_c}{A_c}$$

where V and R_{el} are respectively, the maximum output voltage at the given temperature difference ΔT through the legs and the electrical resistance of the whole TEG. The whole electrical resistance accounts for the legs contribution and the contact resistance as in equation 2-7 with ρ_{legs}, L_{legs}, A_{legs} the electrical resistivity, the length and the cross-section of the legs respectively. A_c and ρ_c are the platinum-legs contact surface and contact resistivity. The hot side of the TEGs is held at a constant temperature. The heat flows from the hot side to the bottom silicon handler by thermal conduction. Heat exchange with ambient air is treated by convection and thermal radiation as shown in Figure 2-2. Because the cold and hot plates are separated by a vacuum gap and due to the relatively weak temperature difference, convective and radiative heat transfers between them are neglected. The simulation conditions are the same for both TEGs. Assuming the conservation of the heat flux, the TEG can be modeled by an assembly of thermal resistances as shown in Figure 2-8. The thermal resistances of the substrates (R_{HOT} and R_{COLD}) are considered as negligible with respect to those of the TEG (R_{TEG}) and convective-radiative exchange with ambient air (R_{AMB}).

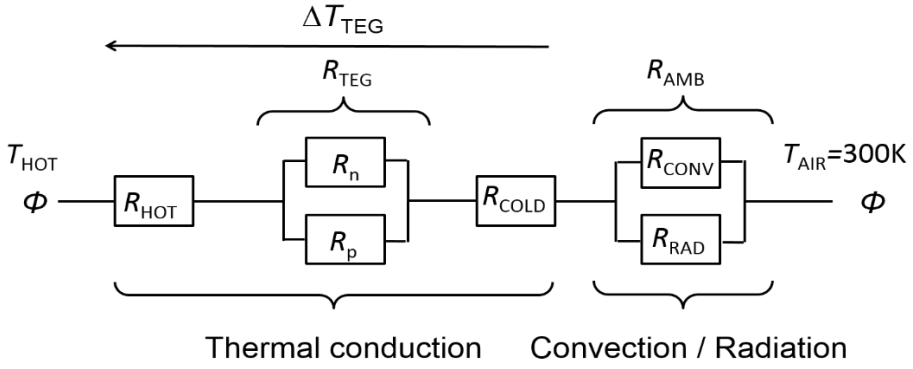

Figure 2- 8: Equivalent analytic model of the thermoelectric generators

Based on this analysis, the effective temperature difference ΔT_{TEG} across the TEG expressed as the following relation gives a function of the maximum available ΔT_{MAX}. ΔT_{MAX} being the difference between the hot plate and ambient air temperatures.

$$\Delta T_{TEG} = \frac{1}{1 + \frac{R_{AMB}}{R_{TEG}}} \times \Delta T_{MAX} \qquad \textit{Equation 2- 8}$$

The hot and cold substrates thermal resistances are neglected compared to the silicon membranes resistances. The high thermal conductivities (150Wm-1 K-1) and the large dimensions of the silicon substrates explain this. The heat being routed from the hot substrate to the cold substrate only by thermal conduction, the TEG thermal resistance is defined as follows:

$$R_{TEG} = R_n // R_p = \frac{L}{(\kappa_n + \kappa_p) \cdot S} \qquad \textit{Equation 2- 9}$$

For the modeling, we assume that the p and n-doped membranes have the same thermal conductivity. The ambient environment influence on the TEG is modeled by the conducto-convection and the thermal radiation in air. The conduction convection is defined by its transfer rate h and the surface subjected to convection S_{CONV}. The equivalent thermal resistance is given by:

$$R_{CONV} = \frac{1}{h \cdot S_{CONV}} \qquad \textit{Equation 2- 10}$$

By working with temperature differences lower than 100K, we assume the linearization of the radiative heat flux as follows:

$$\varphi(Wm^{-2}) = 4\varepsilon\sigma \cdot T_C^3 (T_H - T_C) \qquad \textit{Equation 2- 11}$$

The thermal radiation can then be modeled as a thermal resistance in parallel with the conducto-convective thermal resistance. The radiative thermal resistance is given as follows:

$$R_{rad} = \frac{1}{h_{rad} \cdot S_{CONV}} \qquad \textit{Equation 2- 12}$$

$$h_{rad} = 4\varepsilon\sigma . T_C^3$$

The ambient environment thermal resistance is then expressed as follows:

$$R_{AMB} = R_{CONV} // R_{rad} = \frac{1}{(h_{rad} + h) \cdot S_{CONV}} \qquad \textit{Equation 2- 13}$$

Equations 2-7 and 2-8 show that a good thermoelectric harvester must have first, a higher thermal resistance over the ambient environment to sustain the main part of the heat gradient and maximize the generated voltage. Second, the generator must have the lowest possible electrical resistance in order to maximize the electrical current flow through the generator.

2.1.4 Optimal Si-TEG dimensions

This modeling study aims also to define the optimal dimensions of the silicon membranes in order to harvest the maximum of power from the surrounding heat. In this part, we investigate the influence of the length and the thickness of the silicon membranes on the generators' performances. The modeling is performed for a maximum temperature difference of 30K and in the case of cooling with a small capacity heat sink ($h = 100Wm^{-2}K^{-1}$).

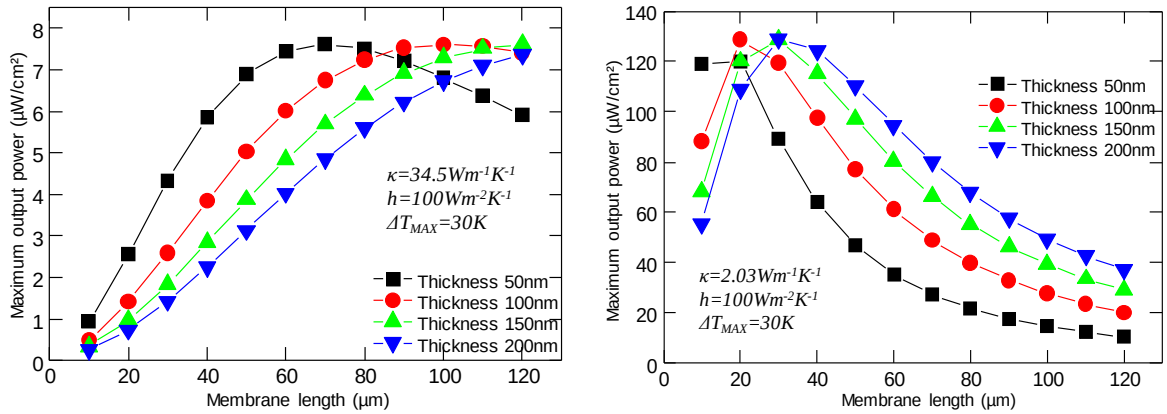

Figure 2- 9: Optimal silicon membranes dimensions investigation for κ_{Si}=34.5 W/m/K (left) and 2.03 W/m/K (right)

Results in figure 2-9 show first, that there is an optimal couple (length, thickness) maximizing the harvested power. Second, the optimal dimensions are given for a tradeoff between high thermal resistance and low electrical resistance (for a given thickness, the tradeoff is obtained in term of the Si membranes length). Indeed, a well-designed thermoelectric harvester is a generator with the highest possible thermal resistance and the lowest possible electrical resistance. Consequently, the optimal dimensions are the dimensions maximizing the electrical conductance and the thermal resistance. The optimal dimensions determined here are used for the demonstrators' realization and their benchmarking with the commercial micro generator. Of course, in practice it will be challenging to have a 200nm thick Si membranes with lower thermal conductivity as obtained by [Tang et al. 2010]. The devices in this thesis will be realized with Si membranes with thicknesses closer to 50nm.

2.2 Commercial micro TEG study

Despite the silicon TEG modeling, this chapter interests in the study of a commercial micro-harvester. Indeed, in addition to the silicon TEG design improvement and the determination of the expected performances from such TEG, it would be interesting to be able to benchmark the Si TEG's expected performances with a state of the art micro harvester and even better if the comparison is done with a commercialized micro-harvester. This benchmarking is realized by means of the finite element method and analytic model developed to confirm the results obtained from the FEM. The principle is basically the same as for the Si TEG modeling except the materials' properties.

2.2.1 Commercial TEG model

The commercial TEG architecture is based on the design presented in [Bottner et al. 2007] and [Bottner 2005] which represents a commercial bismuth telluride based TEG designed by Micropelt. The reported 100µW per thermocouples for a temperature difference of 20K represents state-of-the-art for such miniature converters. The TEG is composed of p and n vertical bismuth telluride legs, 10 µm high, pyramidal shaped with a minimum cross section of $35\times35\mu m^2$ and maximum cross section of $70x70\mu m^2$ (fig 2.3).

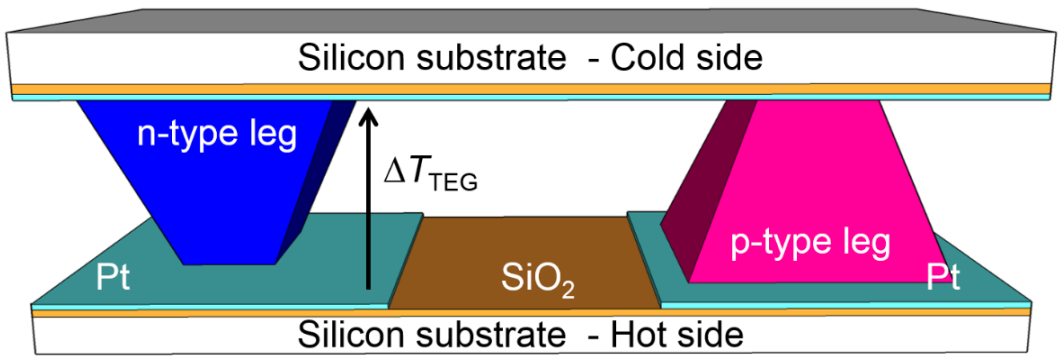

Figure 2- 10: Commercial micro thermoelectric harvester architecture

On each side of the thermoelectric legs, strapping layers of platinum are deposited to ensure electrical continuity while a silicon dioxide layer guarantees insulation from the top and bottom silicon handlers that acts as heat sinks. The cavity between cold and hot surfaces is assumed to be vacuum.

Like for the Si-TEG study, the hot source is assumed to be at constant temperature, the heat is carried from the hot substrate to the cold substrate by thermal conduction and the generator is cooled by thermal conducto-convection and radiation in air. The equivalent analytic model is the same than the analytic model defined for the Si-TEG.

2.2.2 Commercial model validation

Before any modeling study of the commercial micro generator, it is important to make sure that the developed model represents well the commercial micro TEG. To do so, we compared the modeled maximum output power of 140 thermocouples under a fixed temperature difference across the generator with the data from [Bottner 2005] (cf. figure 2-11).

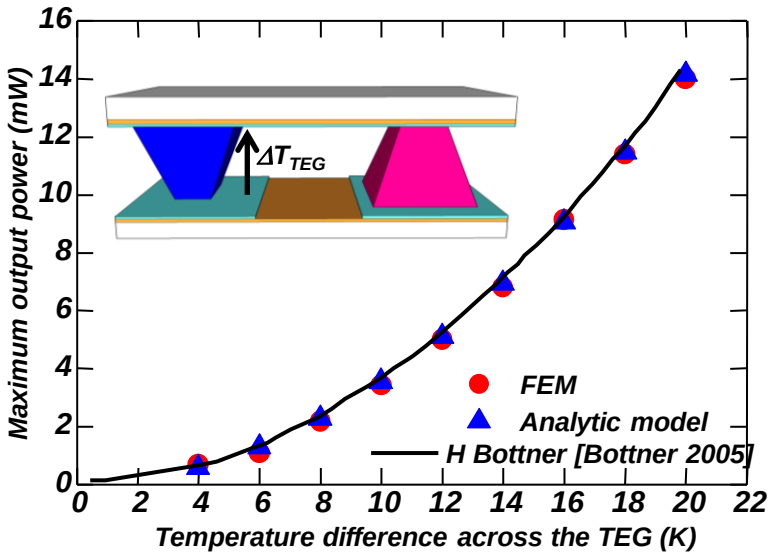

Figure 2- 11: Commercial micro harvester model validation

Both FEM and analytic models fit well the commercial micro TEG data as presented in [Bottner et al. 2007; Bottner 2005]. The commercial micro generator can be studied with the developed models (FEM and analytic) with confidence.

2.2.3 Effect of the cooling conditions on the TEG performances

The commercial micro generator exhibits interesting performances (14mW for 20K of temperature difference across the generator), more than enough to power supply autonomous sensors [Vullers et al. 2009]. The measurements presented by the authors of the commercial TEG are obtained for a fixed temperature difference across the generator (hot and cold substrate at constant temperatures). It is interesting to determine the influence of the cooling with or without heat sink help on the commercial micro generator performances. In figure, 2-12 are presented the maximum output power densities (output power per generator footprint) of commercial micro generator for several available temperature differences and under different cooling conditions.

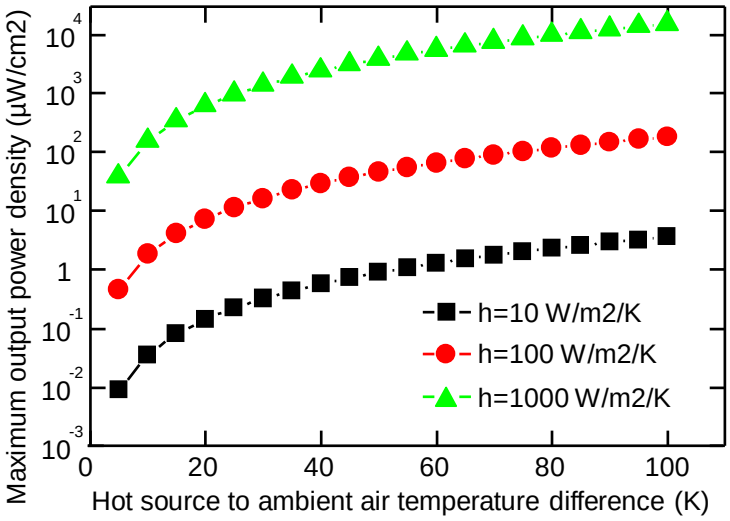

Figure 2- 12: Commercial micro generator performances according to the cooling conditions

Results from this study depict the importance of the use of a higher capacity heat sink to get the best from the commercial micro generator. Indeed, for an available temperature difference of 20K, the generator exhibits a maximal output power density of 0.1 $\mu W cm^{-2}$, barely 6.25 nW, when the generator is cooled by natural convection without any heat sink help. However, by using a heat sink and increasing its cooling capacity, the performances are enhanced to few $mW cm^{-2}$ for higher capacity heat sinks. The poor thermal gradient management of the commercial micro generator explains the poor performances without high capacity heat sink cooling. Indeed, the thermoelectric generator performances are closely dependent on its ability to manage as much as possible the thermal gradient through the thermoelectric legs. Yet, the thermoelectric generator must be more resistive thermally than the ambient environment to ensure a better thermal gradient management through it (equation 2-8). The table 2-3 hereafter presents the thermal resistances of the thermoelectric generator and the ratio between generators' cooling conditions and TEG thermal resistances with respect to the conducto-convection transfer rate (the cooling conditions).

	h=10 $Wm^{-2}K^{-1}$	h=100 $Wm^{-2}K^{-1}$	h=1000 $Wm^{-2}K^{-1}$
R_{TEG} Bi-Te(10^3 K/W)	R_{AMB}/R_{TEG} BiTe		
1.2755	1204.46	168	17.48

Table 2- 3: Thermal resistances of the commercial micro generator and the cold ambient environment for one thermocouple

It shows that:

- Cooled by natural convection without any heat sink help, the generator is a very good thermal conductor compared to the ambient environment (thermal resistances ratio too high). It is then difficult to sustain any thermal gradient across the generator.
- Adding a small capacity heat sink reduces the thermal resistances of the ambient environment with respect to the TEG's resistance and then reduces the heat dissipation from the TEG.
- Increasing the heat sink capacity increases the thermal conduction of the ambient environment, resulting on a better cooling of the generator.

Figure 2-13 highlights better the importance of a heat sink and its cooling capacity to get the best from the commercial micro generator.

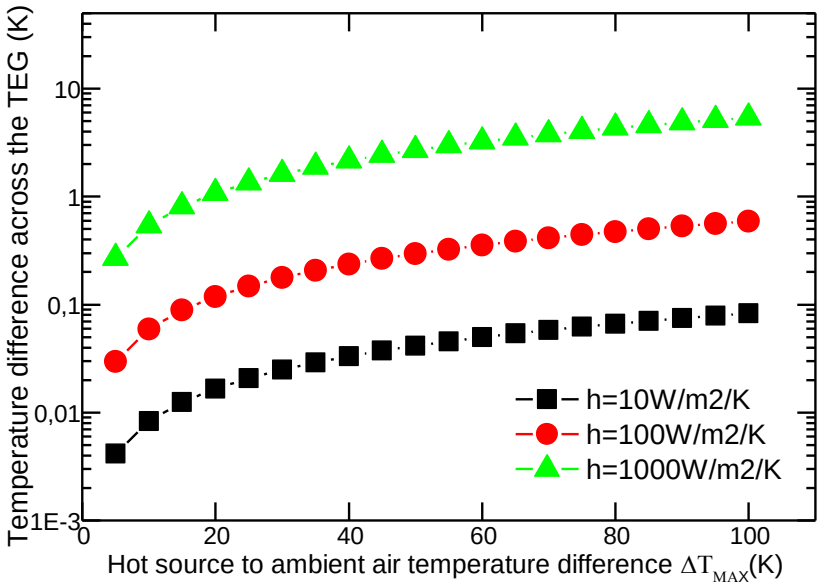

Figure 2- 13: Commercial micro generator thermal gradient management function of the cooling conditions

- Barely 0.1% of the available temperature difference is maintained in the generator when the generator is cooled naturally without any heat sink help. Almost all the heat is lost to the ambient environment.
- The small heat sink capacity improve the thermal gradient management through the generator by reaching about 1% of temperature difference conservation through the generator. Nevertheless, 99% of the heat remains lost to the ambient environment, the generator efficiency remains poor.
- Increasing the heat sink capacity, increases the share of the available temperature difference maintained through the generator and enhances the generator performances.

These observations explain the dimensions of the heat sink compared to the micro generator dimensions provided by Micropelt GmbH.

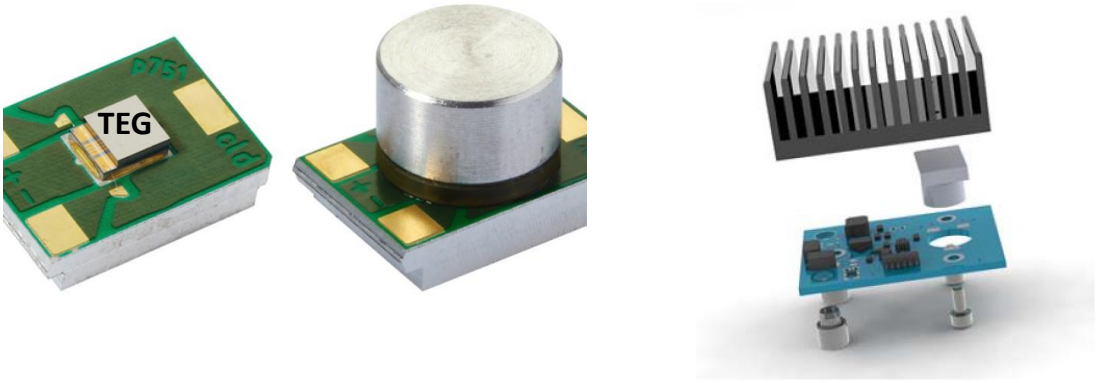

Figure 2- 14: Micropelt thermoelectric module assembly, view on the importance of the heat sink compared to the thermoelectric generator dimensions [MicroPelt GmbH]

2.3 TEGs Benchmarking

The modeling study aims mainly at understanding the possible benefits and drawbacks of our silicon based thermoelectric generator compared to commercial micro harvester. However, before any comparison let us present the expected performances of our developed silicon based TEG.

2.3.1 *Thermal gradient management in the Si planar based TEG*

In the previous part of this chapter, we investigated the performances of the commercial micro harvester with respect to the cooling conditions. This study highlighted the importance of coupling the generator with a high capacity heat sink in order to get the best from it despite the low thermal conductivity of bismuth telluride. In this part, let us focus on the expected performances of Si-based TEG in the same conditions.

As for the commercial micro harvester, we first interest in the thermal gradient management of the planar phononic crystal engineered silicon based generator. The study is performed for both values of thermal conductivities (our last published value and the lowest value predicted by literature). Figure 2-15 reports the thermal gradient management of a Si based TEG with a silicon thermal conductivity of 34.5 $Wm^{-1}K^{-1}$ [Haras et al. 2016].

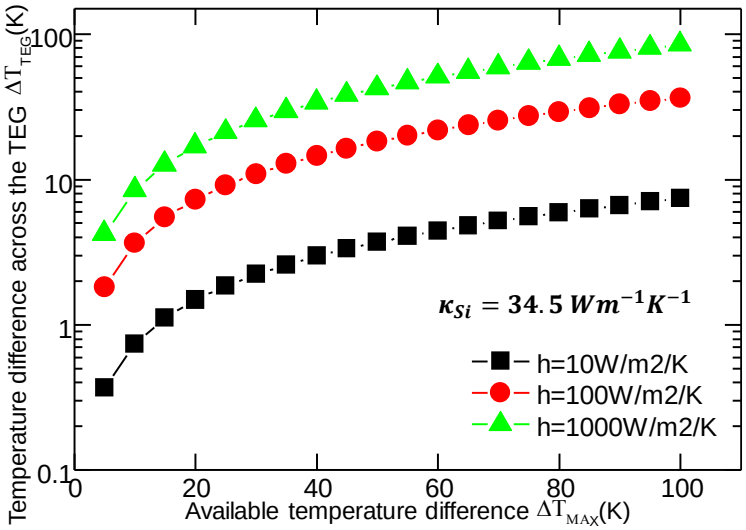

Figure 2- 15: 34.5 W/m/K Silicon phonon engineered generator thermal gradient management function of the cooling conditions

It shows that similarly to the commercial micro generator, the heat sink capacity influences the generator's thermal gradient management. However, this generator manages better the thermal gradient than the commercial micro generator when it is cooled naturally (almost 10% of the available temperature is usable for power generation against 0.1% for the commercial micro generator).

The small dimensions of the silicon membranes (mainly the membranes cross-section) explain this good thermal gradient management behavior despite a larger thermal conductivity. Table 2-4 reports the silicon based TEG thermal resistance and the ambient environment (at the cold side) thermal resistances according to the cooling conditions.

	h=10 $Wm^{-2}K^{-1}$	h=100 $Wm^{-2}K^{-1}$	h=1000 $Wm^{-2}K^{-1}$
R_{TEG} Si (10^6 K/W)	R_{AMB}/R_{TEG} Si		
1.4493	12.5	1.74	0.18
R_{TEG} BiTe (10^3 K/W)	R_{AMB}/R_{TEG} BiTe		
1.2755	1204.46	168	17.48

Table 2- 4: Thermal resistances of the silicon phonon engineered generator and the cold ambient environment for one thermocouple compared to the thermal resistances in BiTe TEG (table 2-3)

Unlike for the bismuth telluride (BiTe) based TEG, the Si planar membranes exhibit higher thermal resistances close to the ambient environment thermal resistances. Allowing then a better thermal gradient management across the Si TEG (even without heat sink help) than across the BiTe TEG.

Downscaling further, the silicon thermal conductivity increases the thermal resistance of the generator, resulting in an improvement of the thermal gradient management through the generator. Figure 2-16 presents the thermal gradient management improvement when the silicon thermal conductivity is reduced to the value predicted by literature [Tang et al. 2010]. The share of the available temperature difference maintained through the generator is more than doubled compare to the use of silicon membranes thermal conductivity from [Haras et al. 2016], reminding that silicon thermal conductivity reduction remains a key factor to improve Si based TEG performances.

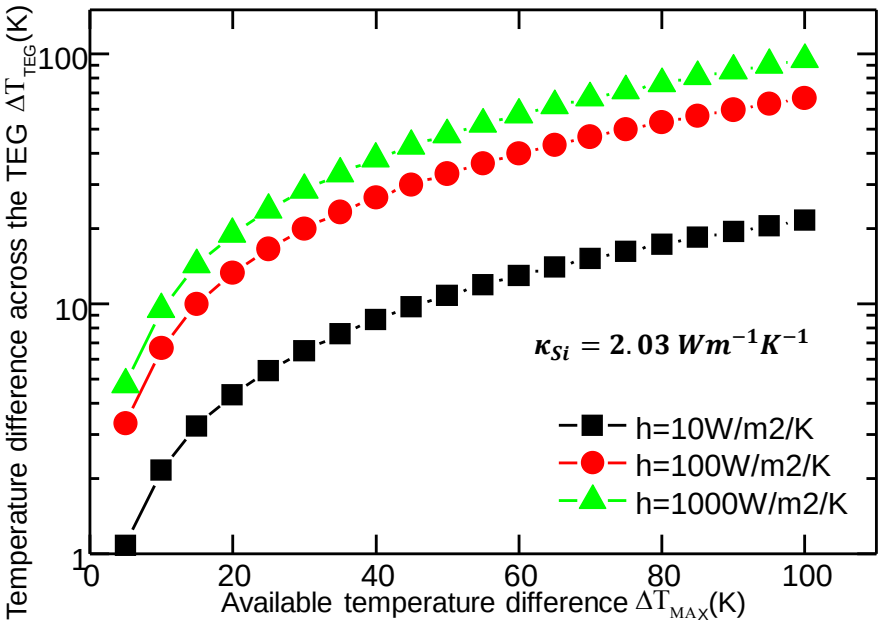

Figure 2- 16: 2.03 W/m/K Silicon phonon engineered generator thermal gradient management function of the cooling conditions

From this study, we can withhold that despite reducing the thermal conductivity of the materials, a good design of the generator in which the material will be embedded is just as important to ensure a good use of the available heat gradient. Therefore, the planar architecture coupled to thermal conductivity reduction seems interesting for silicon based thermoelectric harvester development.

2.3.2 Si based TEG Vs. Commercial micro generator

After showing the interest of coupling silicon thermal conductivity reduction to a planar architecture for a better thermal gradient management through the Si TEG, let us now focus on estimating the performances of such generator with respect to the commercial micro generator. Like previously, the study is done for both values of phononic-engineered silicon membranes thermal conductivity and for three different cooling conditions.

In Figure 2-17 are reported, the expected maximum output power densities according to the available temperature difference in the TEG surrounding of both 34.5 W/m/K Si based and the commercial micro harvester.

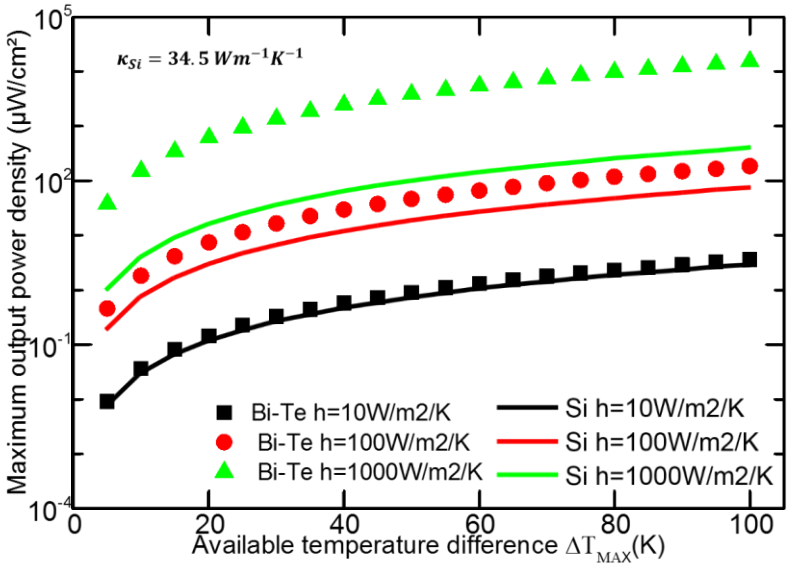

Figure 2- 17: 34.5 W/m/K silicon phonon engineered TEG & the commercial TEG performances benchmarking

First, despite the better intrinsic thermal gradient management of the silicon based TEG, the performances of both generators are comparable when they are cooled without any heat sink help. This can be explained by the fact that in addition to a high thermal resistance a good thermoelectric generator must have a low electrical resistance. In this case, the commercial micro harvester's electrical resistance ($\mathbf{0.214\Omega}$ for one thermocouple) is five order of magnitude lower than that of the Si planar based TEG ($\mathbf{20k\Omega}$ for one thermocouple). Therefore, its high electrical resistance annihilates the good thermal gradient management behavior of the Si based TEG compared to the commercial micro harvester.

By using a heat sink, the thermal gradient management through the commercial micro generator is considerably improved while in the Si based TEG, the improvement is less important and the maximum of temperature difference is quickly reached. The heat sink confers then to the commercial micro TEG better performances compared to the Si based generator.

Downscaling further the phononic engineered silicon thermal conductivity to the literature value [Tang et al. 2010] and using the adequate generator design, the Si planar based TEG performances are considerably enhanced. The Si based TEG outperforms the commercial generator in the case scenario of cooling without heat sink help or with a small capacity heat sink (cf. figure 2-18). Not only has a better thermal gradient management explained these good performances, but also the lowest electrical resistance ($8k\Omega$ for one thermocouple) due to the optimal dimensions for this thermal conductivity (cf. figure 2-9). Nevertheless, despite a silicon thermal conductivity downscaling, a higher capacity heat sink improves hugely the performances of the commercial micro generator, while the Si based TEG performances are slightly increased. Again, the thermal gradient management improvement is more significant for the commercial micro harvester than for the Si based TEG in which the maximum is quickly reached.

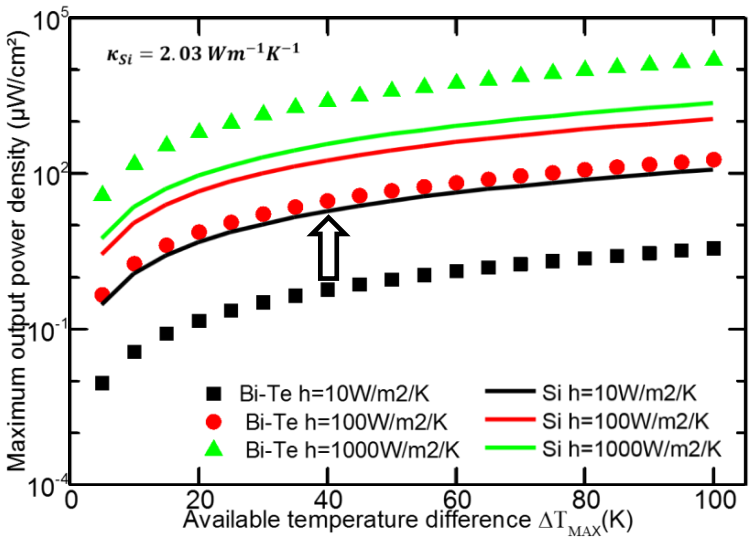

Figure 2- 18: 2.03 W/m/K silicon phonon engineered TEG & the commercial TEG performances benchmarking

Silicon thermal conductivity reduction methodology imposes the development of planar-based thermoelectric harvester. This architecture coupled to a significant thermal conductivity reduction allows a better thermal gradient management through the generator without any heat sink help. However, the low dimensions of the silicon membranes imposed by the thermal conductivity reduction confers a high electrical resistance as well to the generator, limiting the current flow through it. The planar silicon generator is then more interesting for application without any heat sink help and with a small capacity heat sink, if the thermal conductivity is sufficiently low. Nevertheless, when higher capacity heat sinks are used, the commercial micro TEG is better thanks to its very low electrical resistance.

2.3.3 Planar BiTe and Vertical Si: What can we expect?

We presented earlier the benefits and drawbacks of developing planar silicon based thermoelectric generator with respect to the commercial vertical micro harvester. In this part, we focus on the performances of silicon and Bi-Te based TEG in both architectures. We assume the development of suspended bismuth telluride membranes for thermoelectric harvesting. The thermal conductivity remains the thermal conductivity of bulk bismuth telluride (we do not find lower value). This generator will be made of membranes of 20µm long, 10µm wide and 50nm thick, which are the optimal dimensions for a planar TEG for this value of thermal conductivity.

The vertical silicon based TEG is assumed to be developed according to the dimensions of the commercial micro harvester. The dimensions of the thermoelectric legs in this configuration (tenth of micron thick) imposes the use of the bulk silicon thermal conductivity [Sondheimer 1952] (cf. figure 2-19). Silicon planar architecture TEG and the commercial micro harvester complete this study. The two silicon thermal conductivities ($\kappa_1 = 34.5 Wm^{-1}K^{-1}$[Haras et al. 2016] and $\kappa_2 = 2.03 Wm^{-1}K^{-1}$ [Tang et al. 2010]) are modeled. Studies are performed for a constant available temperature difference of 30K and for several cooling conditions.

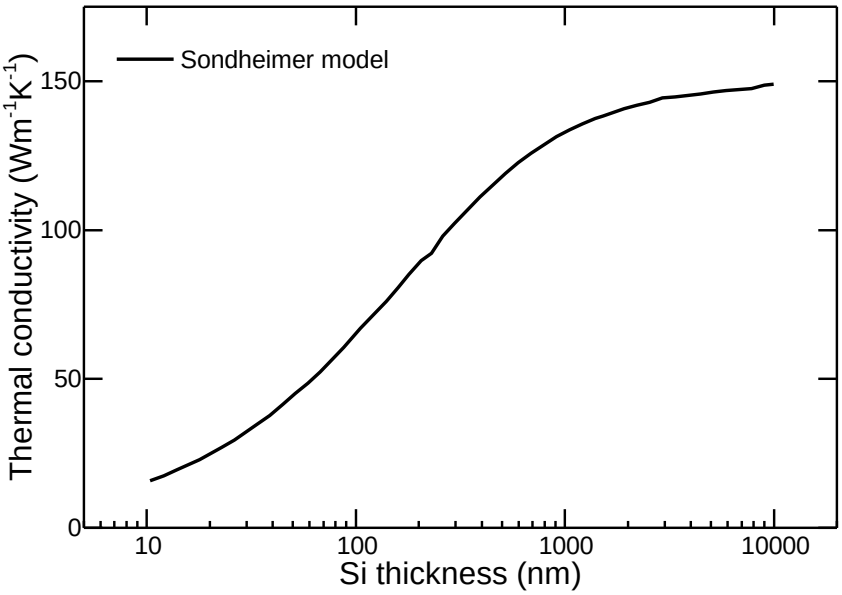

Figure 2- 19: Silicon thermal conductivity dependency to the thickness [Sondheimer 1952]

Figure 2-20 hereafter summaries the maximum output power densities of those different generator configurations according to the cooling conditions. We can observe that:

- First developing a vertical silicon generator like the commercial micro harvester is not of interest.
- Planar architectures are more interesting than vertical architecture when low capacity heat sink is used. This is more significant when the planar harvesters are made of low thermal conductivity materials.
- With planar architectures, performances reach quickly a "plateau", while the commercial micro harvester's performances keep increasing with the heat sink capacity.
- For both planar and vertical architecture, the use of low thermal conductivity materials improves the performances, which confirms the importance of the thermal conductivity reduction.

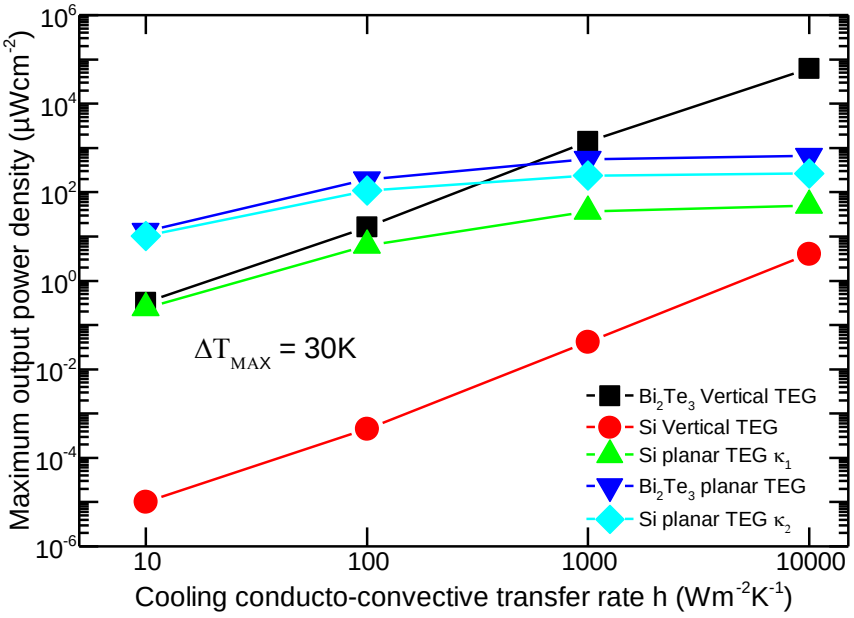

Figure 2- 20: Maximum output power densities of bismuth telluride and Silicon based TEG benchmarking in both TEGs' architectures

A first explanation of the observations done earlier can be the thermal gradient management behavior of those different generators. Figure 2-21 reports the thermal gradient management of the different generators according to the cooling conditions and for an available temperature difference of 30K.

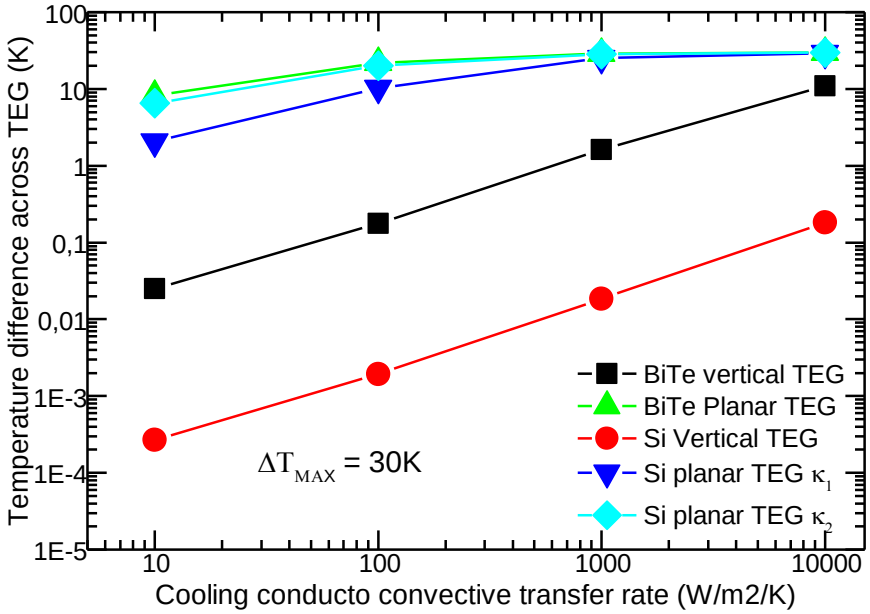

Figure 2- 21: Thermal gradient management of bismuth telluride and Silicon based TEG benchmarking in both TEGs' architectures

This thermal gradient management shows:

- A very bad thermal gradient management across the vertical Si TEG. Indeed, the bulky Si dimensions used for the vertical architecture imposes a high thermal conductivity to the thermoelectric element (cf. figure 2-19). This high thermal conductivity associated to bulky dimensions lead to very low thermal resistance and then a very thermal gradient management.
- Both silicon and bismuth telluride vertical TEGs need higher capacity heat sinks to improve their thermal gradient management. The thermal gradient management is enhanced by increasing the heat sink cooling capacities.
    - Due to its lower thermal conductivity the bismuth telluride TEG, manage better the thermal gradient than the silicon TEG.
    - Due to its higher thermal conductivity, a vertical silicon TEG is more a heat spreader than a harvester. This confirms the non-interest of developing a vertical silicon TEG.
- Planar architectures allow a better thermal gradient management, but by increasing the heat sink capacities, the maximum is quickly reached. The intrinsic high thermal resistances of planar TEGs compared to the cold ambient environment explain this. On the other hand, vertical TEGs are used, the thermal gradient can be improved thanks to the increase of the heat sink capacities and their low intrinsic thermal resistances compared to the cold ambient environment. This thermal gradient improvement coupled to a low electrical resistance increase hugely their performances

Conclusion

This second chapter dealt with the finite element modeling (FEM) of a silicon and a bismuth telluride alloys based thermoelectric harvester. The studied silicon harvester model is made of

planar silicon membranes in the framework of the demonstrators that where realized and studied in the thesis. Regarding the bismuth telluride alloys, the harvester model was realized from a state of the art bismuth telluride harvester [Bottner 2005], realized and commercialized by Micropelt[Micropelt GmbH]. The modeling studies realized for two values of silicon thermal conductivity [Haras et al. 2016] (our last published results) [Tang et al. 2010] (the lowest state of the art value) report:

- A better thermal gradient management across the harvester for the silicon based harvester, despite a higher thermal conductivity
- Comparable (and better with silicon) thermoelectric performances when harvesters are naturally cooled without any heat sink.
- The bismuth telluride harvester remains the best when they are cooled with high capacity heat sink.

The modeling studies highlighted that by combining the two leverages of nanostructuration in order to reduce the thermal conductivity with an innovative in-plane TEG design, there was an improved use of the thermal gradient. Therefore, this lead to a maximized harvested energy even in the absence of bulky heat sinks, which is an advantage in the perspective of miniature energy harvesters. These results open perspectives in the field of autonomous sensor nodes of typical µW consumption with cm^2 sized silicon-based harvesters, based on Si material and compatible with mass production facilities of semiconductor manufacturers.

Chapter 3: Silicon based thermoelectric harvester demonstrators realization

Abstract

This third chapter aims to describe the phonon engineered silicon membranes based thermoelectric harvester demonstrator fabrication process. The main objective is to realize the harvester demonstrators, but also elementary devices indispensable to complete the characterization (thermal conductivity, Seebeck coefficient and electrical conductivity measurement platforms).

First the devices' design is presented, before detailing the fabrication process and finally the presentation of the devices after the realization. The devices are realized on a SOI wafer with a CMOS compatible process, consisting in:

- the patterning of the top layer of the SOI wafer by means of e-beam lithography and Reactive-Ion-Etching (RIE)
- SOI electrical properties modification by mean of ion implantations
- Materials deposition on that top layer by means of Low-Pressure-Chemical-Vapor-Deposition (LPCVD) and e-beam evaporation.
- Thermal insulation of the top layer from the others layer of the SOI by XeF_2 and HF vapor etching.

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3.1 Devices Design

The silicon phonon engineered TEG demonstrators are designed and realized with other devices. Those devices aims to complete the characterizations of the demonstrators and validate some technological process steps. In figure, 3-1 is presented the 2'' wafer containing the different devices.

- The silicon phonon engineered TEG demonstrator (1)
- A "single-thermopile" silicon phonon TEG demonstrator for thermoelectric parameters extraction (2)
- Doping level measurement platforms (3)
- Thermal gradient management devices (4)

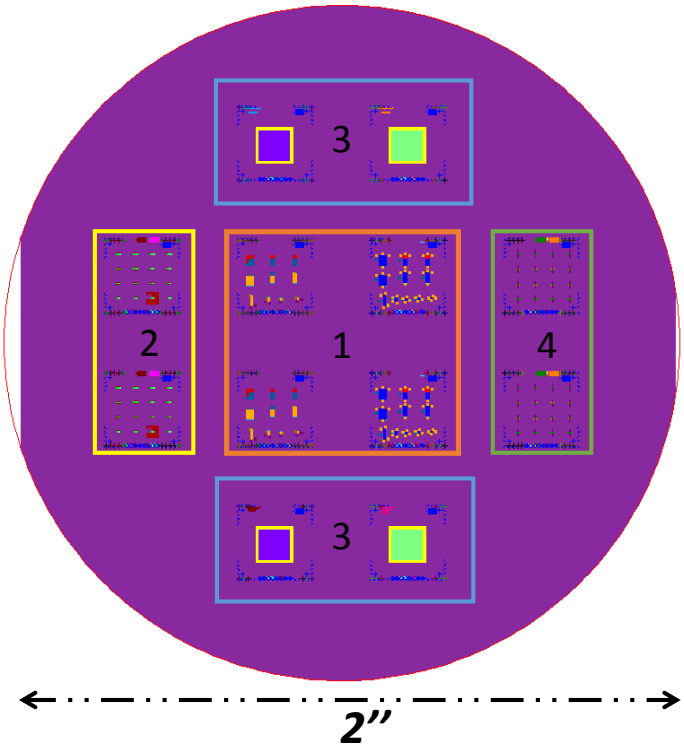


Figure 3- 1: Devices contained on the 2" wafer overview

All the devices are realized on the same wafer, to make sure that the measured thermoelectric properties are well associated to the good demonstrators. This is possible because, the realization processes of all the devices are similar. The non-phonon engineered and phonon engineered versions are designed and realized for all devices (the idea being to study the effect of the phonon engineering on the thermoelectric properties and performances). Before presenting the realization process, the devices designs are described hereafter.

3.1.1 TEGs demonstrators

The wafer contains four cells of TEGs demonstrators, two contains non-phonon engineered silicon membranes and two phonon engineered. Each cell contains several demonstrators made of 5, 10, 25, 50 and 100 thermopiles presented in figure 3-2.

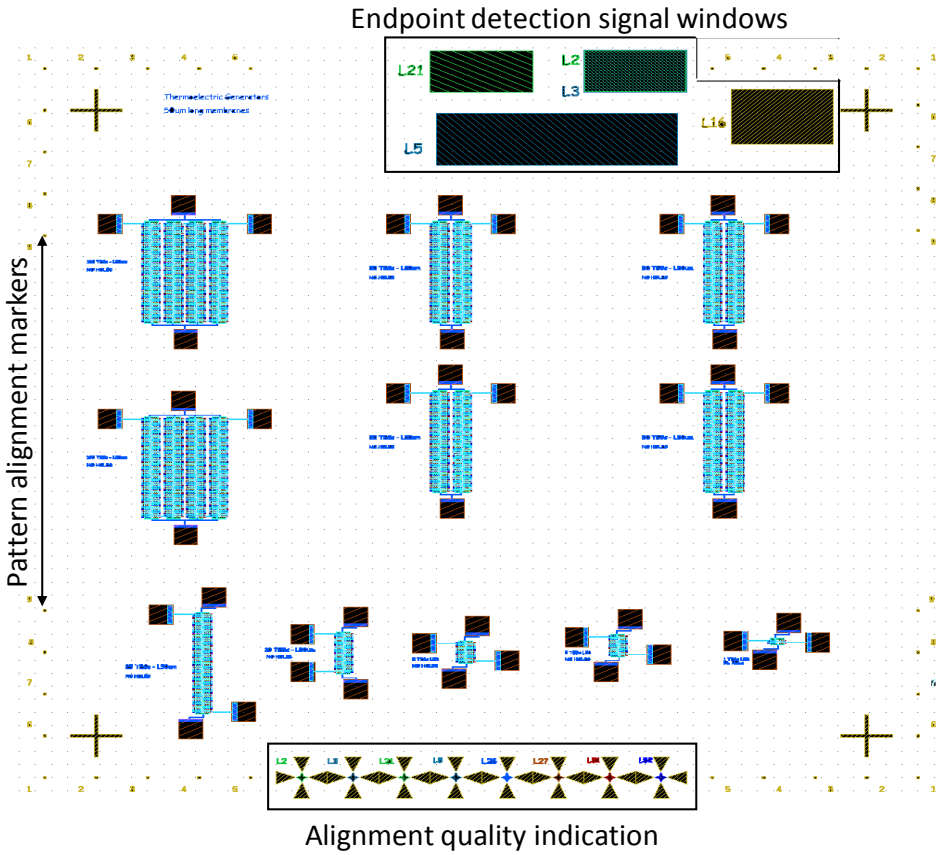


Figure 3- 2: View of one cell containing thermoelectric generator demonstrators.

Demonstrators are made of several thermopiles, associated electrically in series and thermally in parallel. They are contained in a cell of $5760\mu m \times 5760\mu m$. In addition to the devices of interest, the cell contains

- Alignment markers, to allow the precise stacking of the different layers one to another.
- Alignment quality indications, to verify after lithography exposure and development, the good alignment of the written layer.
- Endpoint detection signal windows to control the etching processes.

In the layout software, each layer is associated to a number and a color. These numbers are used to label the endpoint detection windows and the alignment quality indication. The table below summarizes the layers used and the corresponding description. The others devices are also designed following the same layers nomenclature. The cells are identical for all the devices. Figure 3-3 details a planar silicon based TEG demonstrator design.

Layer number	Description
2	Cavities sidewalls protection
3	Cavities openings
5	Phononic crystal patterning
16	Alignment markers
21	SiN removing from membranes
26	PtSi layers
27	Gold layer evaporation
28	Heaters & Labels
51	p doping areas
52	n doping areas

Table 3- 1: Design layers description

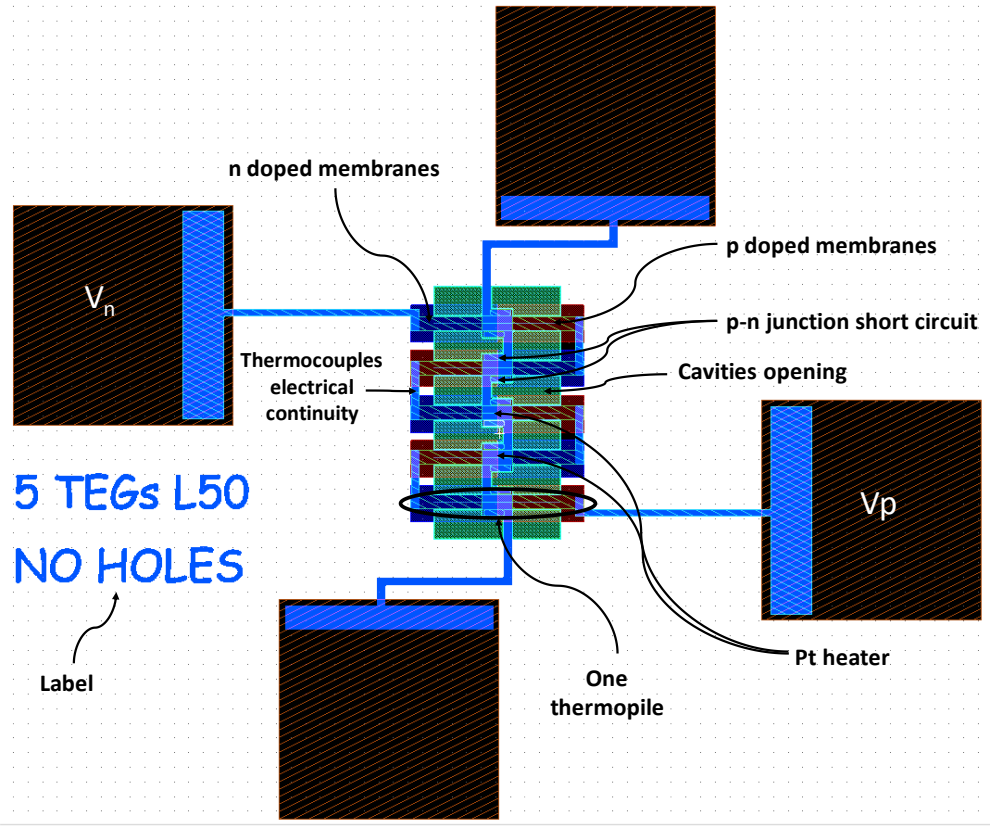


Figure 3- 3: Five thermopiles thermoelectric generator demonstrator.

Each thermopile is made of a pair of p and n doped silicon membranes. The p-n junction is short-circuited by a platinum strap. A platinum strap also ensures the electrical continuity between two thermopiles. Platinum heaters are deposited (cf. figure3-4) at the center of the thermopile in order to simulate by Joule effect the hot source. To make sure that all the Joule effect heat is concentrated in the Pt heater, the heaters are designed to be more resistive than the paths between two heaters. Cavities openings are planned to allow the silicon membranes suspension. Demonstrators are designed according to the modeling results from optimal silicon

membranes investigation (chapter 2). They are then made of 50µm long and 10µm wide silicon membranes.

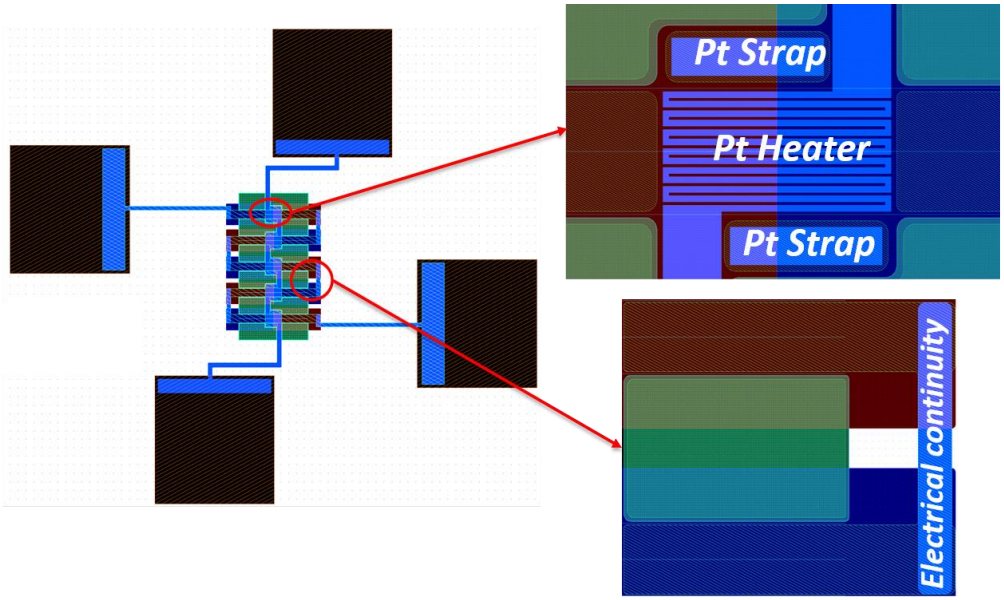


Figure 3- 4: Details of the pn junction short circuit, the Pt heater and the electrical continuity between two thermopiles design

3.1.2 Thermoelectric properties extraction platform

These devices aim to characterize the thermoelectric properties of the phonon-engineered silicon based thermoelectric demonstrators. The wafer contains two identical cells of each device, each cell containing sixteen devices of single thermopile based TEG demonstrators (cf. figure 3-5). The devices are arranged in four columns defining the width of the silicon membranes: 10 µm, 5µm, 5µm and 10µm. There are also arranged in four lines defining the silicon membranes length: 120µm, 90µm, 60µm, 30µm. The different silicon membranes dimensions aims to study the impact of those dimensions on the thermoelectric performances, like studied theoretically in the previous chapter. Finally, like for the TEG demonstrators, some devices are made of phonon-engineered silicon membranes and some are not, in order to study the effect of phonon engineering on thin silicon film thermoelectric properties.

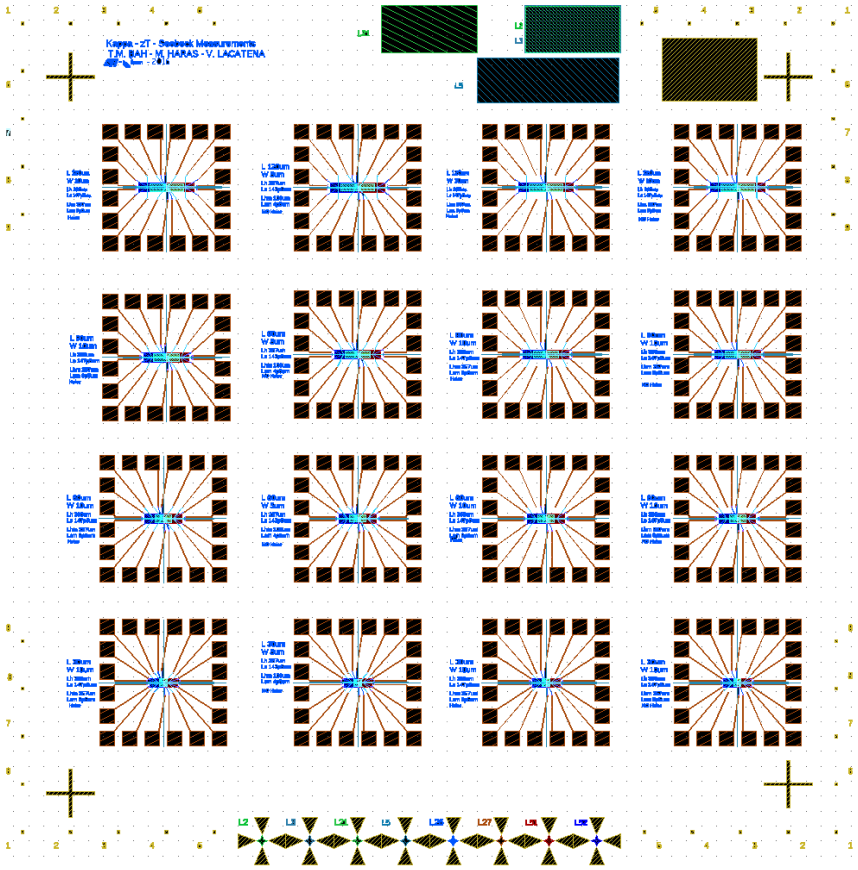


Figure 3- 5: Thermoelectric properties extraction devices design

Figure 3-6 presents a close up view on a thermoelectric properties extraction platform. The device is made of a single thermopile TEG demonstrator, surrounded by a matrix of metallic pads.

- The pads in the center are dedicated to the platinum heater. 4 pads are designed in order to allow a precise determination of the hot source temperature by performing 4 probes measurements.
- At the extremities of the platform, 4 others probes are designed to allow the extraction of cold side temperature. Once the hot and cold side temperature are determined thanks to 4 probes measurements, the silicon membranes thermal conductivity can be extracted.
- The other pads, thanks to a direct contact on the silicon membranes, aims to measure the Seebeck coefficient and the electrical conductivity.

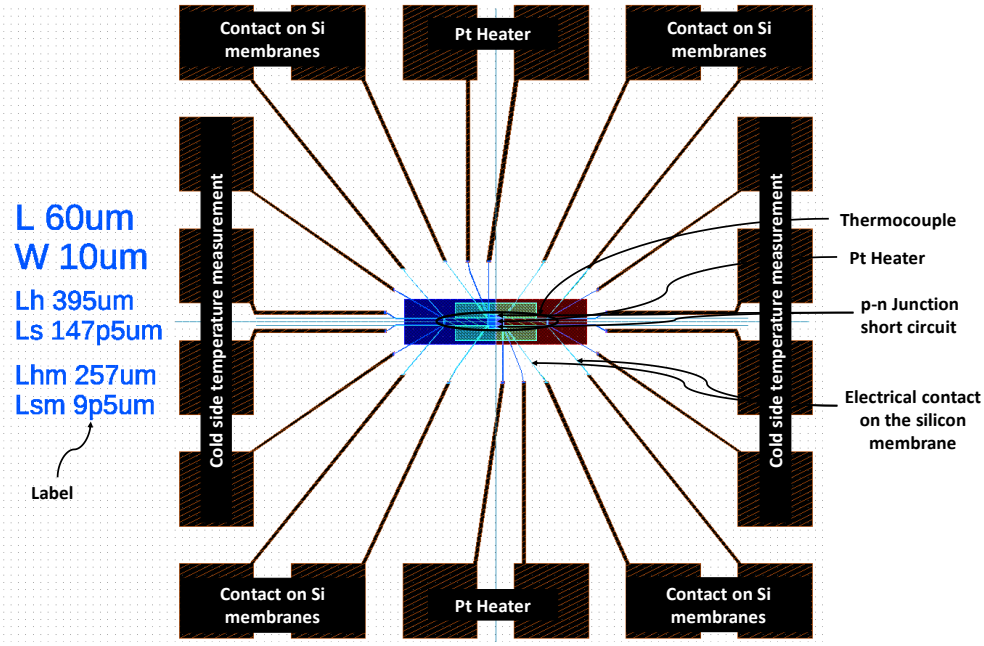


Figure 3- 6: Details of a thermoelectric properties extraction device

3.1.3 Doping level Measurements

The third category of devices are dedicated to allow the measurement of the silicon membranes doping level. The devices consist in 4-probes measurements platform (cf. figure 3-7).

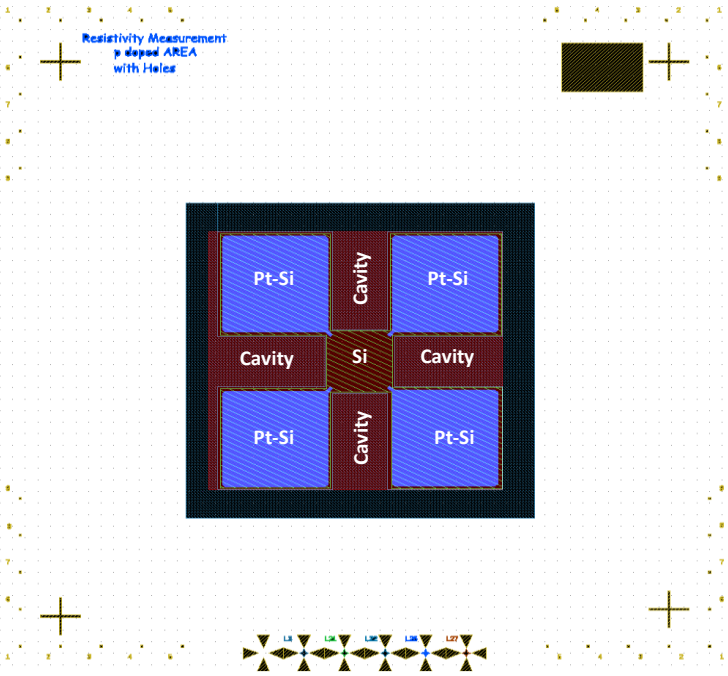


Figure 3- 7: Doping level measurement device

The idea here is to measure the electrical resistivity of a p or n doped silicon layer and to determine the doping level of the Si layer from an abacus. The silicon layer is insulated from the wafer by etching cavities around it. Platinum layers are deposited at the extremities of the Si layer to ensure an electrical contact. The contacts must be as much as possible symmetric and ohmic. Finally, the wafer contains for each doping nature, a silicon phonon engineered

layer and a non-phonon engineered one, in order to allow a first study of the impact of the phononic engineering on the Si sheet resistance and resistivity.

3.1.4 Thermal gradient management devices

The last category of devices on the wafer is dedicated to the silicon membranes thermal conductivity measurements by the 3ω methodology. The wafer contains two cells of sixteen devices (per cell).

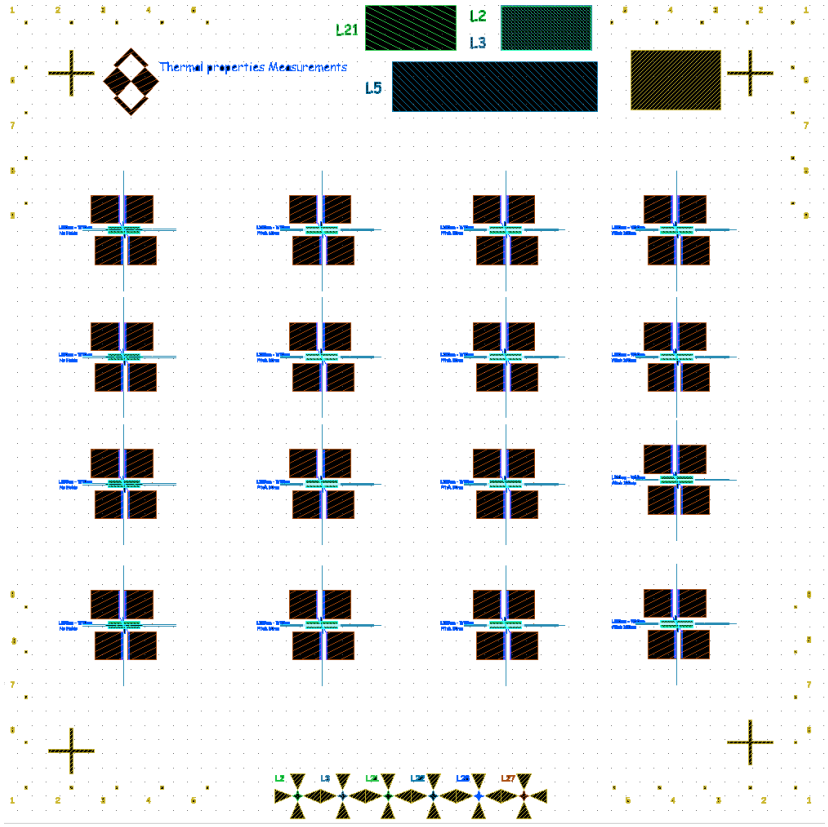


Figure 3- 8: Thermal gradient management devices cell

The devices consist in suspended and non-doped silicon membranes, heated by a platinum heater at the center (cf. figure 3-9). All the devices are made of identical pairs of 120µm long and 10µm wide silicon membranes. However, the sixteen devices in each cell are not identical, the first column contains devices made of non-phonon engineered silicon membranes and three others phonon engineered silicon membranes as follows:

- Second column : phonon engineered silicon membranes, with 60nm as distance between two consecutive holes centers (called pitch)
- Third column : phonon engineered silicon membranes with 80nm as holes pitch
- Fourth column : phonon engineered silicon membranes with 100nm as holes pitch

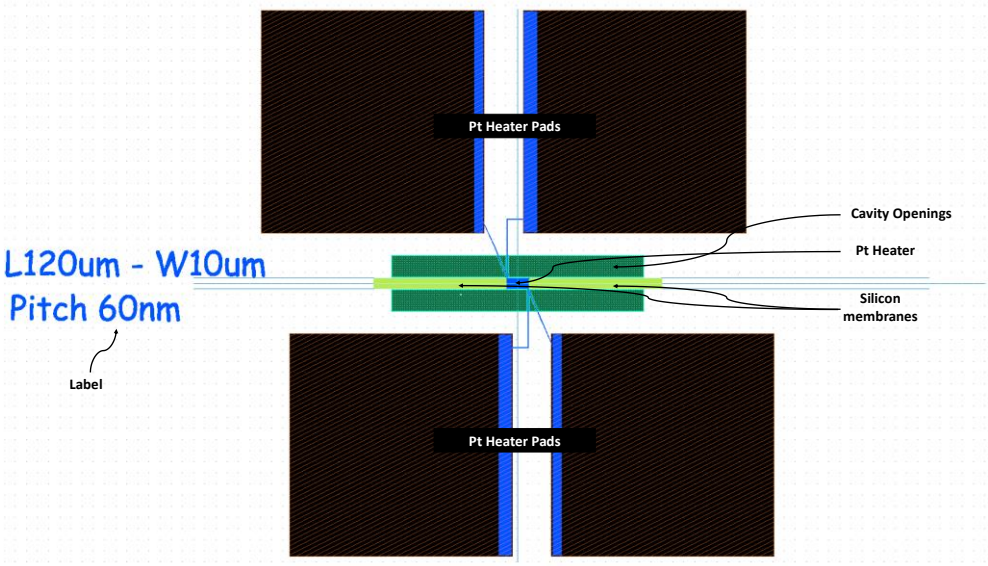
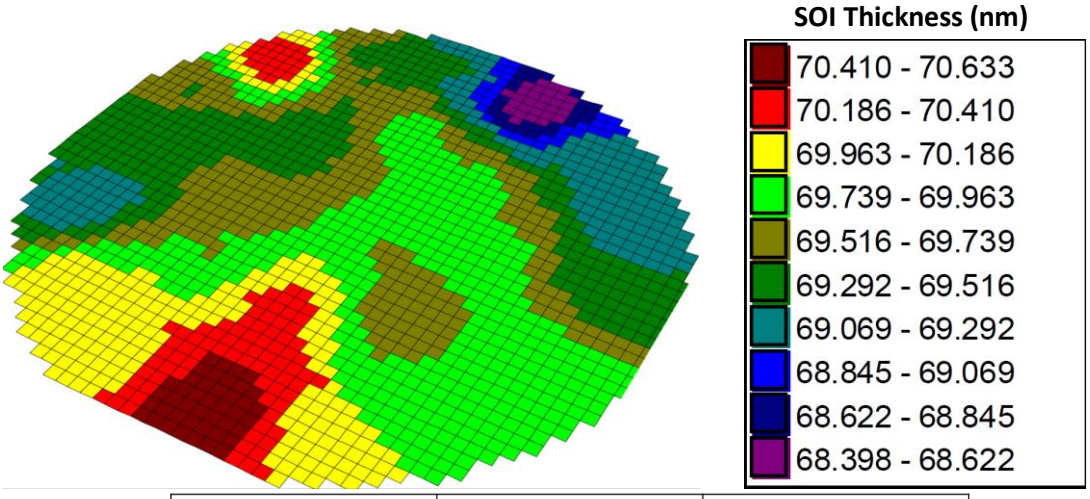


Figure 3- 9: Details of a thermal gradient management device

3.2 Devices Realization

The devices are realized from a SOI wafer from SOITEC. The stack is composed of 70nm (cf. figure 3-10) thick silicon top layer (that we will call SOI), a 145nm thick Buried-Oxide (BOX) layer and 745µm silicon substrate layer.



Average	Minimum	Maximum
69.671 nm	68.398 nm	70.633 nm

Figure 3- 10 : SOI layer thickness mapping by ellipsometer (ELL) measurement

The realization process (figure 3-11) consists in:

- the patterning the top layer of a Silicon-On-Insulator wafer by means of e-beam lithography and Reactive-Ion-Etching (RIE)
- SOI electrical properties modification by mean of ion implantation
- Materials deposition on that top layer by means of Low-Pressure-Chemical-Vapor-Deposition (LPCVD) and e-beam evaporation.
- Thermal insulation of the top layer from the others layer of the SOI by XeF_2 and HF vapor etching.

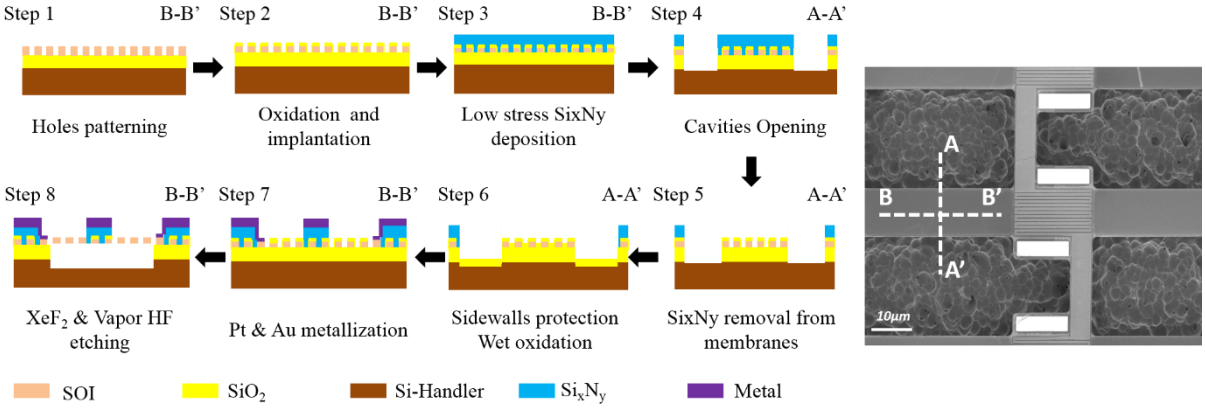


Figure 3- 11: Silicon thermoelectric generator demonstrators' realization process

3.2.1 Wafer cleaning & Alignment markers patterning

First, the 8 inches SOI wafer purchased to SOITEC are cut in to 2 inches wafers. A protective resist layer is coated before cutting, so the first step of the devices realization will be the cleaning of the cut wafers. This cleaning consist on putting the wafers in a Remover PG solution heated at 70°C for 2 hours minimum, followed by acetone and isopropanol (IPA) rinse. The cleaning is then completed with Piranha (solution of H_2SO_4 and H_2O_2) attack for 10 minutes, in order to strip all the organic residuals. Finally, the wafers are immersed in a HF solution for 30 seconds for stripping an eventual silicon oxide layer. The table hereafter summaries this cleaning steps.

Step description	Step parameters
Protective resist stripping	Remover PG @ 70°C for 2 hours minimum Acetone, IPA rinse – N2 blow dry
Organic residuals stripping	H2SO4:H2O2 = 1:1 for 10 min Deionized (DI) water rinse – N2 blow dry
Eventual oxide layer stripping	HF for 30 sec Deionized (DI) water rinse – N2 blow dry

Table 3- 2: Wafers cleaning procedure

Once the wafers cleaned, the next step is the alignment markers patterning to allow the correct superposition of the different layers. The markers are patterned thanks to an electron beam (e-beam) lithography and reactive ion etching. First, the resist spin coating (MMA copolymer from MicroChem diluted in the solvent ethyl lactate (EL13%)), then e-beam lithography and reactive ion etching are performed.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V1000rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 1.8µm
Lithography	Lithography Writing : Dose 450µC/cm2, current : 25nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Etching	SF6/Ar 10sccm/10sccm, 30W 10mTorr : SOI top layer etching (~35sec) CF4/N2/O2 40sccm/40sccm/5sccm, 100W 30mTorr : BOX etching (~15min) SF6/Ar 10sccm/10sccm, 30W 10mTorr : Silicon substrate etching (~10min)
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry

Table 3- 3: Alignment markers patterning recipe

Table 3-3 details the different steps for the alignment markers patterning. The markers must be as deep as possible to allow the correct alignment of the layers by the e-beam machine. To do so, the markers are etched down to the SOI layer (70nm), the box layer (145nm) and few micrometers in the silicon substrate. The etching is monitored by mean of an endpoint detection signal. This is done by monitoring the DC bias potential while holding the RF power constant. The voltage-power relation being related to the chemistry of the plasma, the absence of a plasma contribution form the etched layer implies a change of their relationship. Therefore, when the layer is completely etched the intensity of the spectral lines emitted by the plasma changes. An embedded endpoint detection signal apparatus is provided with the RIE etching. It consists in a camera with a laser driven by a software. The laser is pointed and focalized on a pattern to be etched and by interferometry, it indicates the changes in reflection due to layers etching and the etching rates.

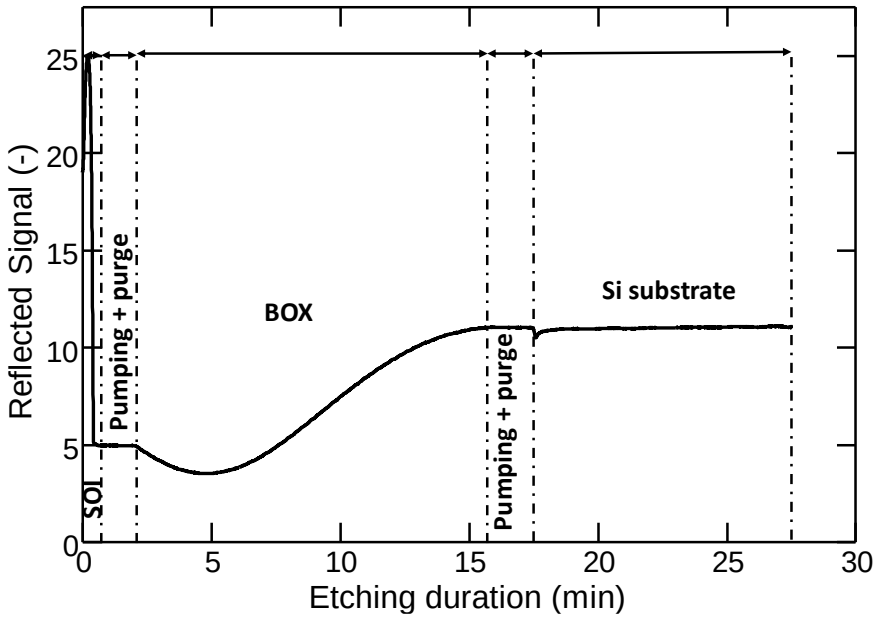


Figure 3- 12: Alignment markers etching endpoint detection signal

3.2.2 Phononic engineering patterning

After, the alignment markers patterning, we highlight now the phononic crystal patterning on the silicon membranes. This step is realized by mean of e-beam lithography and reactive ion etching . For this step, the resist used is the CSAR 62 from AllResist, which has a higher resolution than the MAA copolymer used for the alignment markers. The phononic crystal network can be patterned by mean of two methodologies presented hereafter.

3.2.2.1 Dots on the fly

The dots on the fly methodology [Trasobares et al. 2014; Lacatena et al. 2014]consist in defining the e-beam machine's beam step size (BSS) to the desired phononic crystal network pitch, using a higher current (10nA) and lowering the dose (tenth of µC/cm2) for obtaining regularly spaced network. The "trick" is to draw a sample figure (a square as an example) in order to generate the network at one time. The lower dose aims to generate the pattern only once, but not to provide it the sufficiently high dose and the BSS to perform the desired writing of all feature. The image obtained appears as a "pixelization" of the desired object.

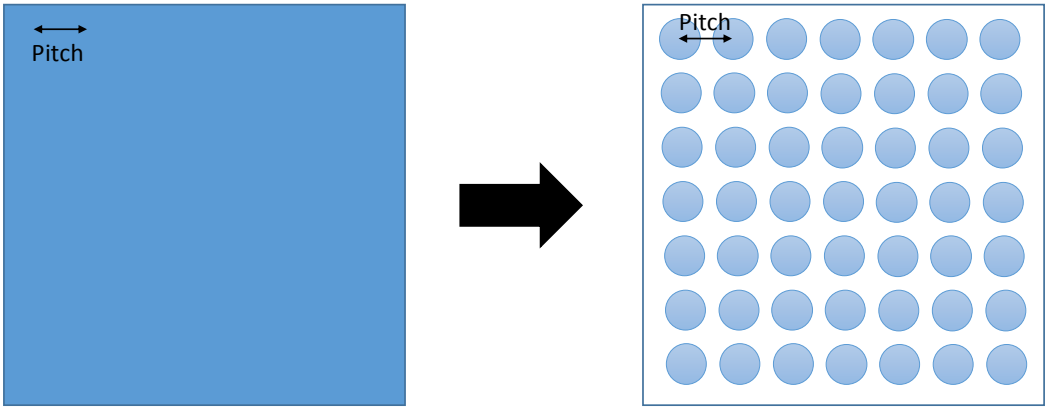


Figure 3- 13: Dots on the fly (dotfs) principle

This methodology has the advantage to allow a fast lithography, due to the time saved from the beam on/off transitions. It is then interesting for patterning large areas. However, the dots-on-the-fly methodology does not allow us to open properly the phononic crystals (cf. figure 3-14).

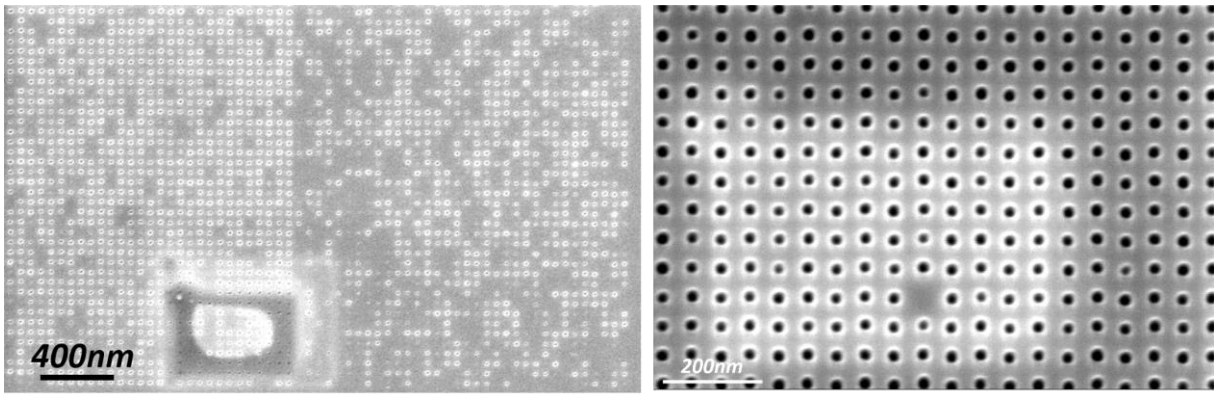


Figure 3- 14: Partially opened phononic crystals networks after dotfs

3.2.2.2 Overdosing method

The second methodology consists in designing a sequence of small squares (2x2 nm^2 – Smallest e-beam machine's BSS) and to overdose (hundredth of mC/cm^2) each square in order to open more than the square dimensions (cf. figure 3-15).

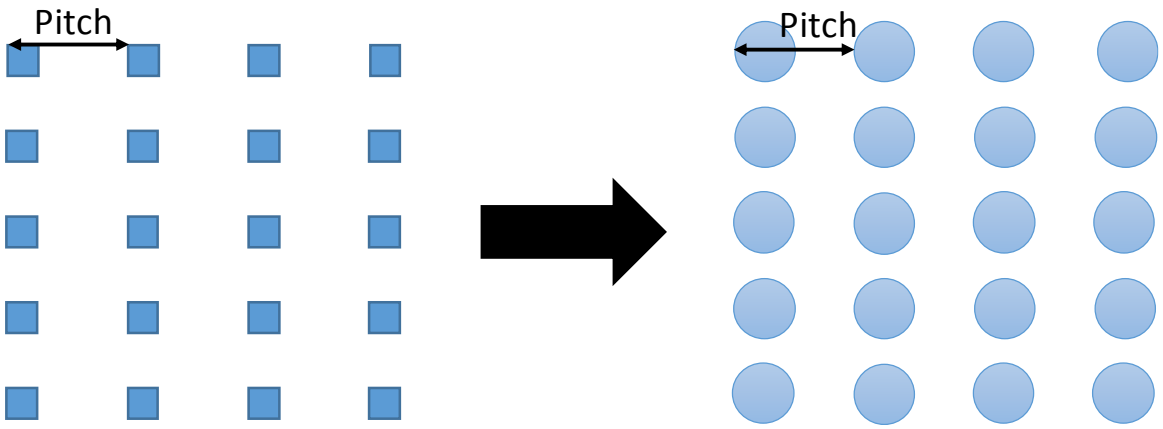


Figure 3- 15: Overdosing methodology principle

The pitch is defined by the design and not by the e-beam machine's BSS anymore. This methodology allows the patterning of different shapes of phononic crystal networks and precise opening of the patterns (cf. figure 3-16). However, exposing the squares, one after the others, increases considerably the lithography times.

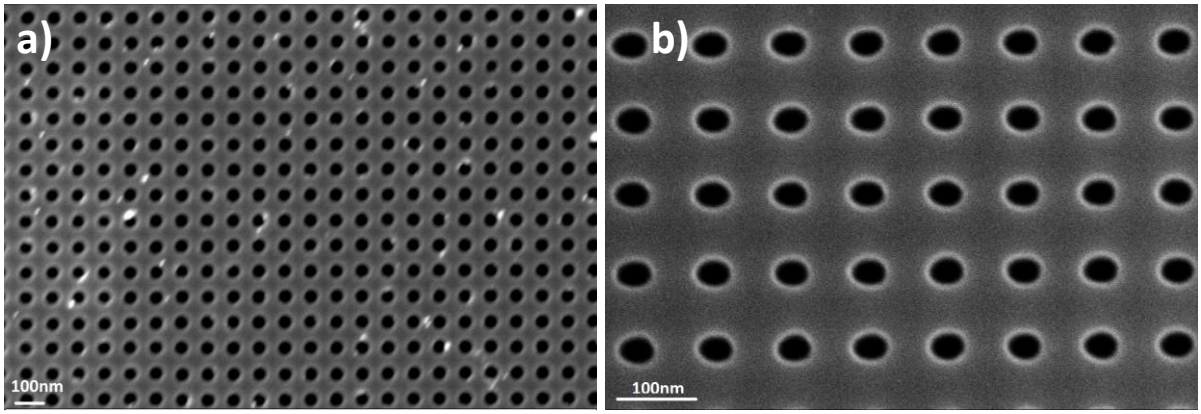


Figure 3- 16: SEM pictures of phononic crystals after realization by overdosing methodology

The overdosing methodology allowing a better patterning precision than the dots-on-the-fly methodology, despite a higher lithography time, the choice to pattern the pores with this methodology is made. The realization process is given in the following table.

Step description	Step parameters
Resist Spin coating	CSAR 62: V3000rpm, A1000rpm/sec, t08sec Baking @ 150°C for 1 min Thickness : ~300nm
Lithography	Lithography Writing : Dose 300mc/cm2, current : 300pA, Resolution 100nm Lithography development : AllResist 600-54 @ 80rpm for 55 sec – IPA rinse for 40sec
Etching	Cl2/Ar 30sscm/10sccm, 30W 10mTorr for 4min
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry

Table 3- 4: Phononic crystals patterning recipe

After the lithography, a Cl_2/Ar RIE etching is performed to open the phononic crystal in the SOI layer. The etching is performed without any endpoint detection signal help, due to the fact that the patterns are too small (tenth of nm) to focalized the laser, and focalizing on a bigger pattern while etching is useless, due to the loading effect (larger patterns are etched faster than the small patterns). However, by determining the exact thickness of SOI etched in small patterns while using an endpoint detection signal on larger patterns, the required etching duration can be calculated. For a 70nm thick SOI, the duration is estimated to 4min. The SEM pictures (figure 3-17) of cleaved holes confirm the holes opening till the box for 4min of Cl2/Ar RIE etching. Moreover, the pictures shows an anisotropic profile of the holes.

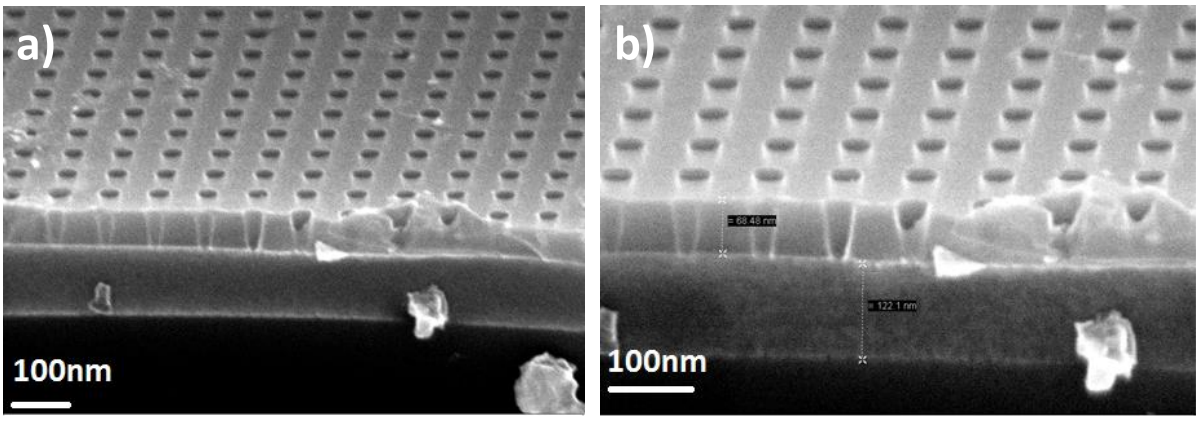


Figure 3- 17: Profile cuts of SOI membranes after the phononic crystals patterning

3.2.3 Ion implantation

This third step aims at developing the thermopiles that will compose the TEG demonstrators. Those thermopiles are realized by doping the SOI layer thanks to ion implantation forming p and n-doped regions. Ion implantation doping consists in accelerating (at low temperatures) ionized impurities with an electric field, in order to give them the necessary energy (keV) to enter the material. Ion implantation offers more flexibility than diffusion for semiconductors' doping. First, ion implantation is performed at room temperature, allowing the use of resist as mask while diffusion is done at high temperatures, limiting the mask choices to silicon oxide or silicon nitride, much harder to strip. Second, ion implantation offers an anisotropic dopant profile and an independent control of the dopant concentration and junction depth (cf. figure 3-18).

Diffusion	Ion implantation
High temperature process → Hard mask (SiO2 or SiN) needed	Low temperature process → Resist can be used as mask
Isotropic dopant profile	Anisotropic dopant profile
Cannot independently control the dopant concentration, junction depth	Can independently control the dopant concentration, junction depth

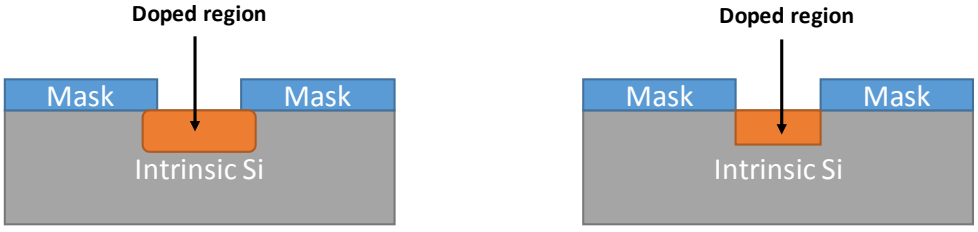


Figure 3- 18: Doping by diffusion and ion implantation comparison

However, ion implantation presents two main drawbacks. First, the ion implantation damages the target's structure. Indeed, all the way into the target, the ions undergo series of collisions, displacing the target's atoms. The effect of those collisions can be amplified by eventual collisions due to the displaced target's atoms until the particles energy becomes too small. Hence, the doped regions can be highly disordered resulting in electronic properties way far from expected. A rapid thermal annealing (RTA, >= 900°C for 5-60 minutes) can repair these damages after implantation [Narayan et al. 1983]. The second drawback concerns the channeling effect. Indeed, in crystalline materials, certain directions allow the ions to propagate

with minor scattering. At first glance, the channeling effect may be interesting, since it minimizes the scattering, thus the target's structures damages. However, the channeling effect brings a deeper dopant profile and random dopant distribution according to the channels [Teranishi et al. 2018], resulting in a non-uniformity of sheet resistance. Hence, it is indispensable to minimize the channeling effect as much as possible. The first solution and most widespread consists in titling the target of a certain angle in order to present a random target structure arrangement (cf. figure 3-19). This random arrangement will increase the probability of ions scattering and then reduces the channeling effect [Teranishi et al. 2018; Cho et al. 1985].

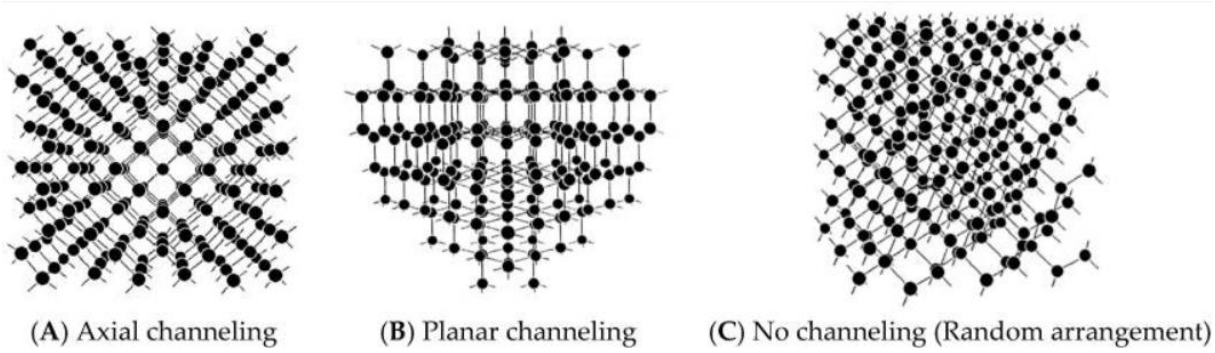


Figure 3- 19: Different appearance of a crystal lattice by the view angle [Teranishi et al. 2018]

Performing ion implantation through an amorphous layer deposited or grew on the target is another proposed solution. Generally, this amorphous layer is a silicon oxide layer. The thicker the silicon dioxide layer, the lower the channeling effect (cf. figure 3-20) [Teranishi et al. 2018]. Those two solutions cannot completely annihilate the channeling effect, especially in high symmetrical structure like silicon, but they will reduce the impact on the ion implantation. Therefore, the first step of ion implantation process is the growth of a silicon oxide layer to act as a screen amorphous layer for reducing the channeling effect during implantation.

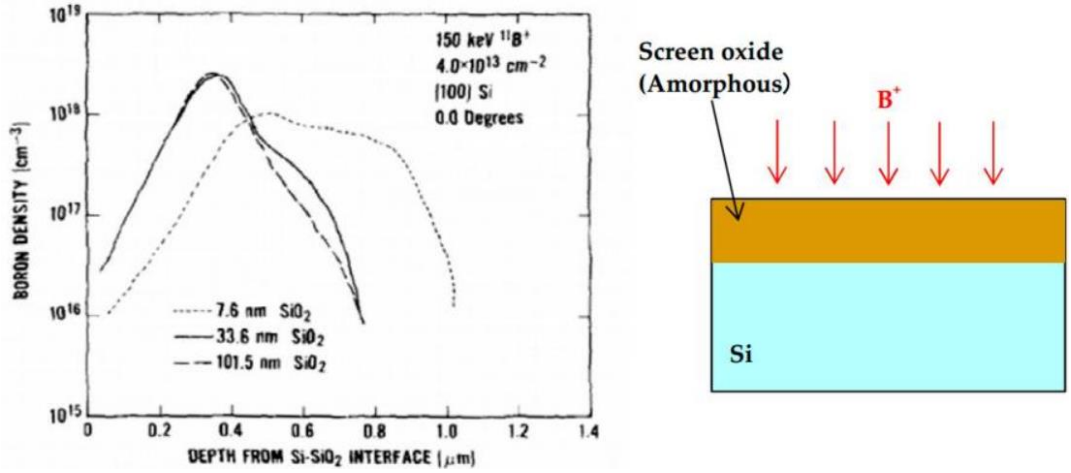


Figure 3- 20: Boron dopant profile with various screen oxide thickness [Teranishi et al. 2018]

3.2.3.1 SOI oxidation

The SOI oxidation will not only serve as screening layer for the ion implantation, but also as protection for the SOI layer from the XeF2 etching, and as sacrificial layer during the reactive ion etching. The oxide is grown (LPCVD) and not deposit (PECVD) to ensure a better tightness to the XeF2 gas. The LPCVD oxidation or thermal oxidation consist in forcing at high temperature (800-1200°C) an oxidizing agent into a wafer and react with it. The oxidizing agent

can be obtained from water vapor (wet oxidation) or molecular oxygen (dry oxidation) according to the following reaction.

$$Si + 2H_2O_{(gas)} \rightarrow SiO_2 + 2H_{2\,(gas)} \text{ (wet oxidation)}$$

$$Si + O_{2\,(gas)} \rightarrow SiO_2 \text{ (dry oxidation)}$$

The thermal oxidation is accompanied by a consumption of the silicon substrate (cf. figure 3-21). About 45% of the grown oxide comes from the silicon substrate. However, this silicon consumption limits the oxide thickness. Indeed, the oxide thickness is not only imposed by its use (protection layer, screen layer …) but also by available silicon and the device applications. In our case, the SOI layer after oxidation should not be too small, due to the risk of increasing the electrical resistance, that will limit the developed generators performances. For this work, we choose to grow 15nm of oxide, reducing then the SOI thickness of less than 10nm.

The dry oxidation is performed because it allowed a good uniformity of growing (cf. figure 3-22) and repeatability. The growth is done at 900°C, for 35 min and under two slm of oxygen according to the oxidation recipe depicted in table 3-5.

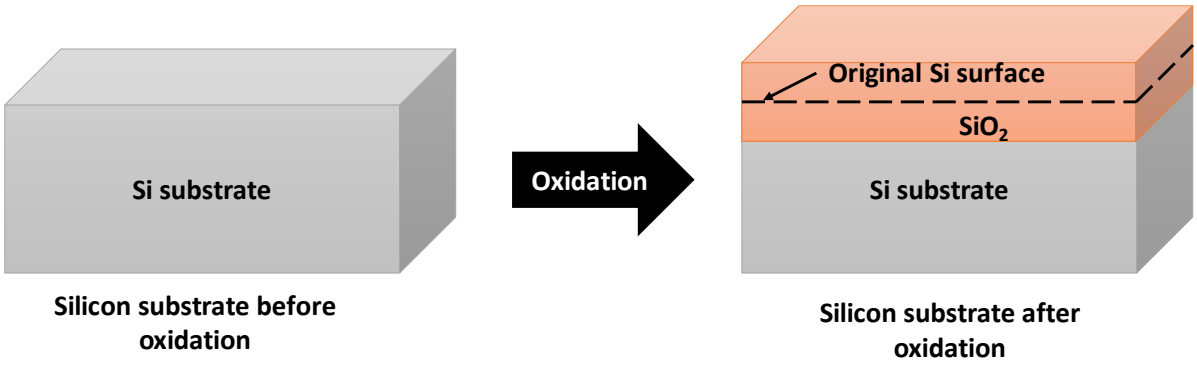


Figure 3- 21: Silicon thermal oxidation principle

Recipe steps	Temperature (°C)	Gas composition	Gas flow (slm)	Duration (min)
Wafer introduction	500			
Heating	500 → 650			20
	650 → 900	N_2/O_2	2/0.2	30
Oxidation	900	O_2	2	35
Cooling	900 → 500			

Table 3- 5: Dry oxidation process

The grown oxide and the remaining SOI layer thicknesses are measured with an ellipsometer and consigned in figure 3-22. The recipe allows the growth of a 13.8 nm thick average oxide with a good uniformity (11.8 – 14.6 nm) for 15 nm as target.

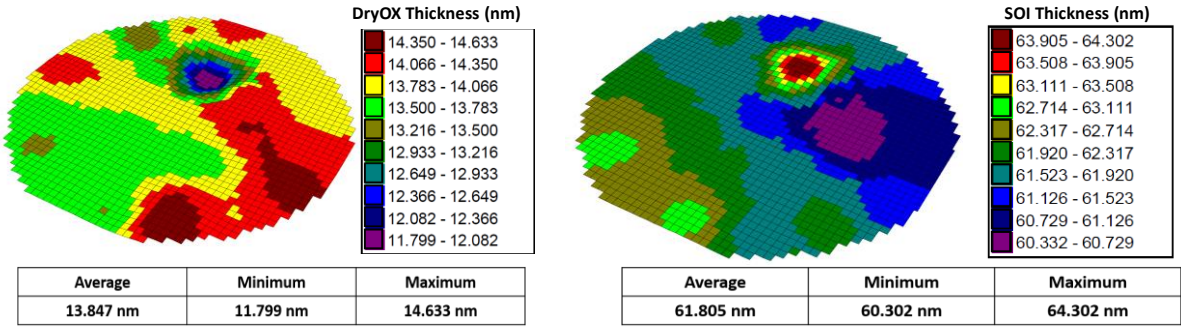


Figure 3- 22: Dry oxide (left) and remaining SOI (right) thicknesses mapping

3.2.3.2 Ion implantation parameters

The oxidation completed, we interest in the ion implantation. First, we must determine the ion implantation parameters (energy, dose and minimal thickness of the mask). The different parameters are obtained thanks to a "Monte-Carlo" like simulation through the software SRIM/TRIM. The software interface is presented figure 3-23, it consists of three parts: the dopant nature and energy definition zone (1), the target's stack definition (2) and the materials composing the stack definition (3). The stacks width are the layers' thicknesses.

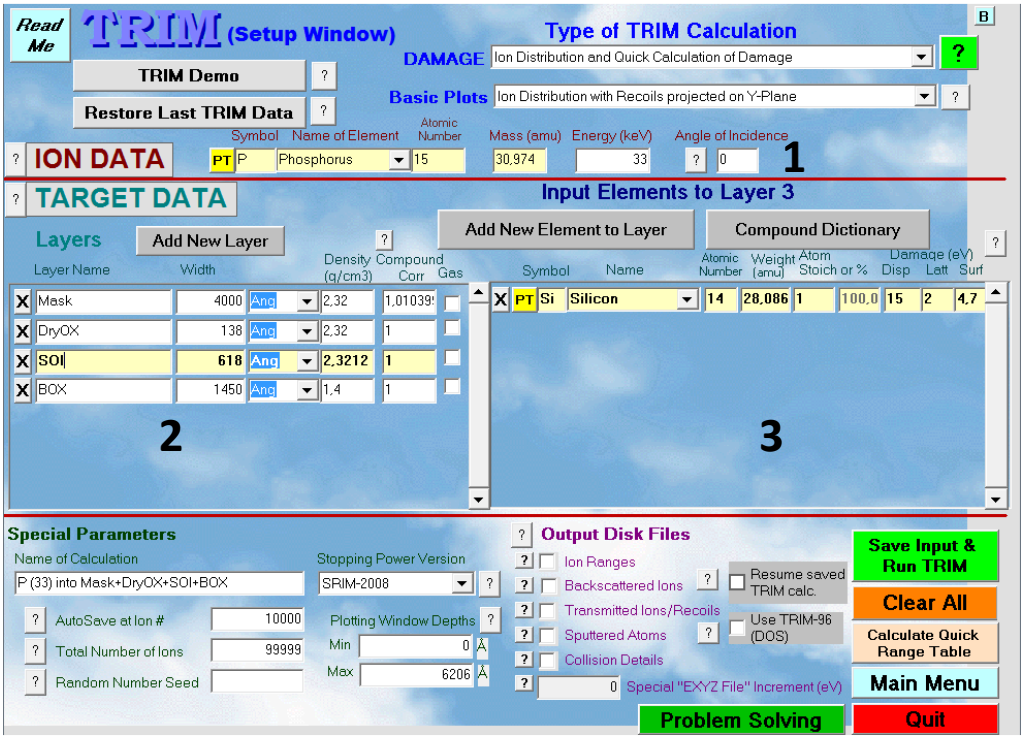


Figure 3- 23: Ion implantation "Monte-Carlo" modeling interface

First, we were interested in finding the optimal dopant energy to allow the maximum of ion to reach the SOI layer and remain into it. Therefore, the modeling is performed without any mask in the stack. The modeling shows that the optimal energies are respectively 12 keV for the boron dopants (p dopants) and 33 keV for the phosphorous dopants (n dopants). Figure 3-24 presents the ions propagation and distribution into the stack. These modeling results also give us the implantation dose corresponding to the desired dopant concentration over the y-axis of the ion distribution. The optimal doping level for a thermoelectric harvester being around

$10^{19} atoms \cdot cm^{-3}$ and considering the ions distribution, the implantation is performed for both p and n dopants at $2 \cdot 10^{14}\ atoms \cdot cm^{-2}$.

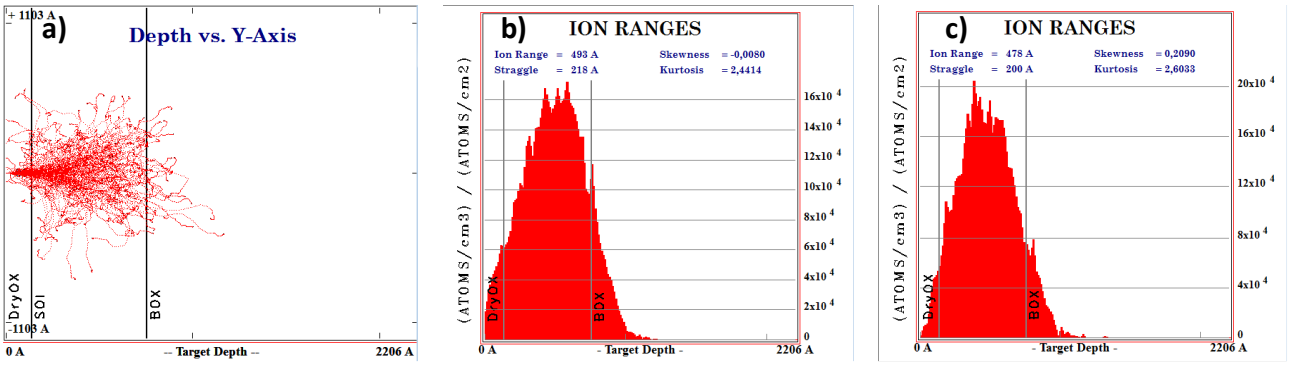


Figure 3- 24: Boron and phosphorous implantation simulation of a silicon layer. Ions propagation into the target stack (a), Ions distribution for a Boron dopant (b) and phosphorous dopant (c)

Once the optimal energies were identified, we were interested in the thickness of the mask allowing a good protection of the regions where we do not want to implant. Ion implantation allowing us to use resist as mask, we investigated the use of a 200nm PMMA resist. The results presented in figure 3-25 shows that the 200nm are more than enough to prevent from the implantation of non-desired areas. Nonetheless, the choice of using the habitual 1.8µm thick MAA8.5EL13 copolymer is done.

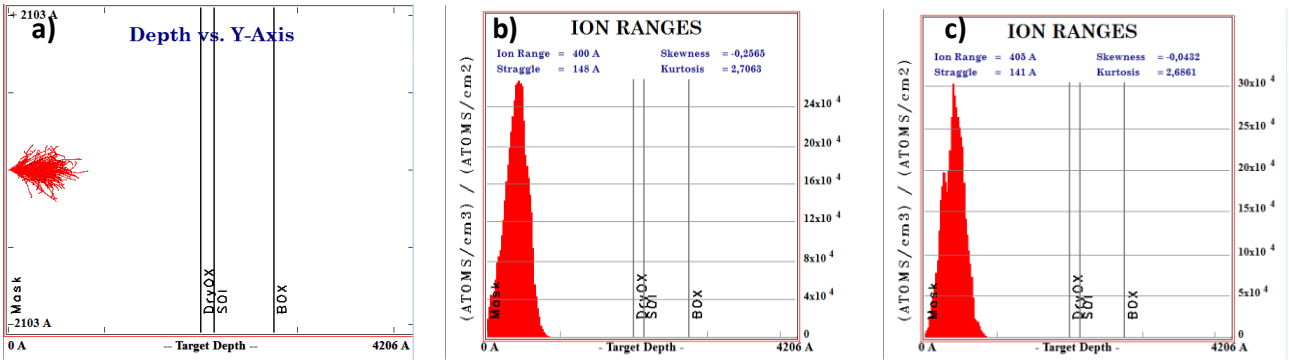


Figure 3- 25: 200nm PMMA resist mask investigation. Ions propagation into the target stack (a), Ions distribution for a 12 keV Boron dopant (b) and 33 keV phosphorous dopant (c)

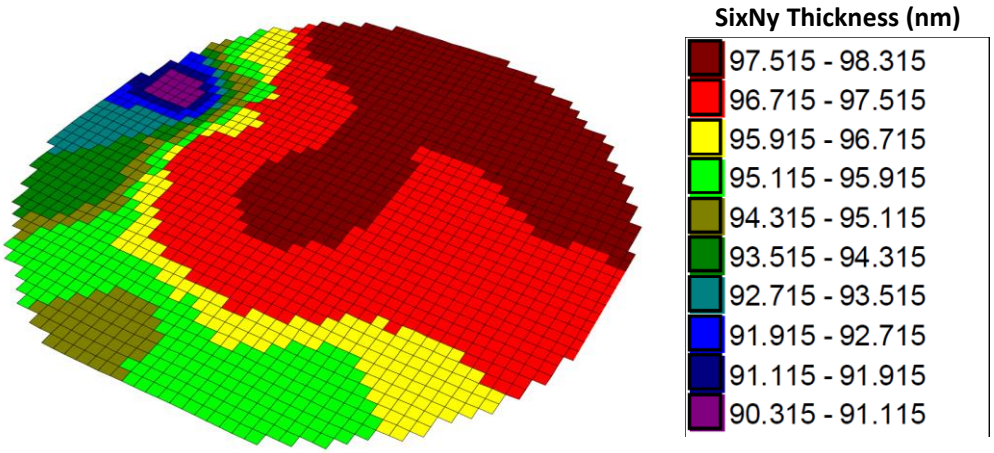
Once the implantation parameters are defined, the p and n doping are performed according to the process flow consigned in table 3-6. An e-beam lithography is realized to expose the regions dedicated to doping. The boron or phosphorous doping is performed at the same time, the resist is stripped, and a rapid thermal annealing (RTA) is performed at 900°C for 5min under a nitrogen (N_2) environment. The operation is repeated for the other nature of dopant.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V1000rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 1.8µm
Lithography	Lithography Writing : Dose 450µC/cm2, current : 25nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Implantation	Boron dopant, Energy: 12keV, Dose: $2 \cdot 10^{14}\ atoms \cdot cm^{-2}$ or Phosphorous dopant, Energy : 33keV, Dose: $2 \cdot 10^{14}\ atoms \cdot cm^{-2}$
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry
Rapid Thermal annealing (RTA)	Annealing @ 900°C for 5min under N_2

Table 3- 6: Ion implantation process flow

3.2.4 Cavities Opening & SiN removing from SOI

Following the ion implantation, a 100 nm thick (cf. figure 3-26) silicon nitride layer is deposited to first isolate the metallic component dedicated to simulate the hot source from the silicon membranes and second, to increase the mechanical strength of the suspended membranes.



Average	Minimum	Maximum
96.482 nm	90.315 nm	98.315 nm

Figure 3- 26: LPCVD SixNy full wafer thickness mapping

The silicon nitride layer is deposited by LPCVD because it ensures the deposition of low-stress silicon nitride layer, indispensable to avoid the mechanical bending of the suspended structures. Two kinds of silicon nitride can be deposited, the stoichiometric Si_3N_4, which is a high stress (622 MPa – internal data) silicon nitride and the non-stoichiometric Si_xN_y with low

stress (29.4 MPa –internal data). Naturally, we choose to deposit the second one according to the recipe defined in table 3-7.

Recipe steps	Temperature (°C)	Pressure (mTorr)	Gas composition	Gas flow (sccm)	Duration (min)
Wafer introduction	350				
Furnace Heating	350 → 800	5-20			60
Ammoniac purge	800	100	NH_3	10	10
Si_XN_Y deposition	800	100	SiH_2Cl_2/NH_3	20/10	32
Ammoniac purge	800	100	NH_3	10	15
Furnace Cooling	800 → 350				60

Table 3- 7: Low stress Si_XN_Y deposition recipe

In order to prepare the silicon membranes suspension at the last steps of the process, access cavities are opened around the silicon membranes (cf. figure 3-27). E-beam lithography writing and a reactive ion etching according to the recipe in the table 3-8 perform the cavities openings.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V1000rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 1.8µm
Lithography	Lithography Writing : Dose 450µC/cm2, current : 25nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Reactive Ion Etching	SF6/Ar 10sccm/10sccm, 30W 10mTorr : Si_XN_Y/SiO_2/SOI top layer etching (~8min) CF4/N2/O2 40sccm/40sccm/5sccm, 100W 30mTorr : BOX etching (~15min)
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry

Table 3- 8: Cavities openings recipe

The recipe is quite similar to the alignment markers patterning recipe, except that the etching is performed through the deposited silicon nitride, the thermal oxide, the thin SOI layer and the BOX down to the silicon substrate. Figure 3-27 represents the etching endpoint detection signal and a SEM views of some opened cavities.

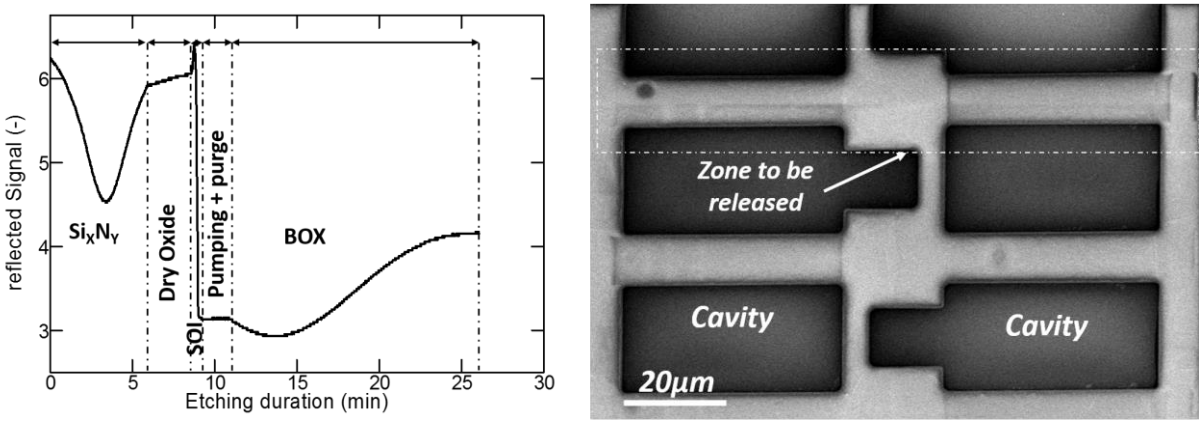


Figure 3- 27: Left: Membranes suspension access cavities etching endpoint signal and right SEM view of some cavities opened for the silicon membranes suspension.

To avoid any eventual parallel conduction channel in the silicon nitride, it must be removed from the silicon membranes. Therefore the silicon nitride is removed from the membranes by another step of e-beam lithography writing and reactive ion etching as summarized in table 3-9. The etching is performed until the endpoint detection signal indicates the complete etching of the silicon nitride and the exposure of the dry oxide to the etchants. The endpoint signal is represented in the figure 3-28.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V1000rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 1.8µm
Lithography	Lithography Writing : Dose 450µC/cm2, current : 25nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Reactive Ion Etching	SF6/Ar 10sccm/10sccm, 30W 10mTorr : Si_XN_Y top layer etching (~6min)
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry

Table 3- 9: Silicon nitride removal from membranes recipe

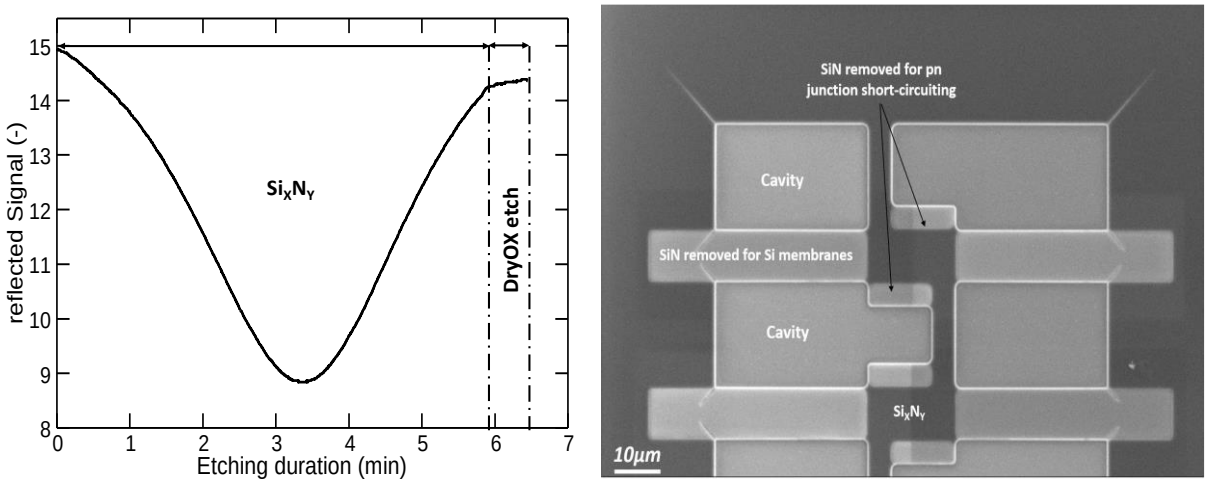


Figure 3- 28: Left: Silicon nitride etching from membranes endpoint signal and right: SEM view of some thermopiles after SiN removal from silicon membranes and areas dedicated to pn junction short-circuit

3.2.5 Metal deposition

The devices metallization is the following step. However, before metallization a drawback of the cavities opening step has to be solved. Indeed, by opening the access cavities, we exposed laterally the SOI layer. This issue has to be faced, to avoid the membranes etching at the XeF_2 etching step. An oxidation is performed according to the recipe presented earlier and before metallization to avoid the furnace contamination. This step called sidewalls protection allows the oxidation of both the lateral exposed SOI layer and the inner surface of the cavities (cf. figure 3-29).

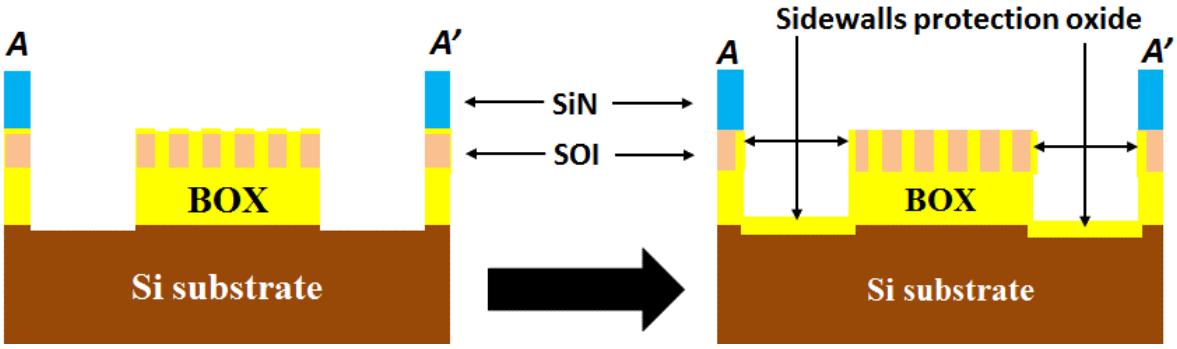


Figure 3- 29: Before (left) and after (right) sidewalls protection oxide growth

Once the SOI sidewalls protection oxide grown, we deal with the devices metallization. This step aims to deposit metals for ensuring the electrical continuity of the thermopiles and the metals for the devices characterizations. The deposition is performed by e-beam lithography and e-beam evaporation. Before metal evaporation, a low power (300 eV) and short (2min) Ar plasma etching step is done to eliminate eventual contaminations on the samples.

3.2.5.1 Platinum metallization

The platinum deposition aims first to realize platinum heaters, emulating by Joule effect the TEGs' hot source. The platinum is also used to realize the "ohmic" contacts on the silicon membranes, indispensable to ensure the electrical continuity between thermopiles and to the devices characterization. An e-beam lithography is realized through the same MAA8.5EL13 copolymer resist, before the evaporation of 30nm of platinum and a rapid thermal annealing (RTA) after the resist stripping. The step process is depicted table 3-10.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V2500rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 800nm
Lithography	Lithography Writing : Dose 500µC/cm2, current : 10nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Platinum evaporation	Buffered Oxide Etchant (BOE 7:1) attack 30sec Ar etching 300eV, 2min - Platinum evaporation : 30nm
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry
Rapid Thermal Annealing (RTA)	Annealing @ 400°C for 2min under 500 sccm of N_2H_2

Table 3- 10: Ohmic contacts realization recipe

Before the metal evaporation, the silicon oxide grown on the silicon membranes must be removed to allow contacting them. This is done by a 45 sec of buffered oxide etchant (BOE) attack just before loading the sample in the evaporation chamber. The BOE is preferred to HF, to avoid the resist embrittlement or destruction. Removing the metal from the area non-devoted to the ohmic contacts is achieved by stripping the resist underneath the metal, then the metal

above also. A reactive-ion-etching step can replace the BOE attack. The BOE attack have the advantage to be fast than the reactive-ion-etching.

The ohmic contacts are realized thanks to a rapid thermal annealing at 400°C, under 500sccm of N_2H_2 and for 2min. this annealing aims to ensure the formation of one unique and less resistive material from Pt and Si called platinum silicide (PtSi). This silicidation occurs according to two reactions: first the diffusion of the platinum into the silicon to form the intermediate compound (Pt_2Si), and finally the diffusion of the silicon into the Pt_2Si to form the final compound (PtSi). These two reactions occur sequentially (no PtSi without Pt_2Si) and they are thermally activated.

Figure 3-3-a, from Larrieu's works [Larrieu et al. 2003], shows that the annealing must be realized at least at 338°C to achieve the complete silicidation of the platinum and the figure b from Breil's works [Breil 2009] shows that around 400°C and for 2min of RTA under N_2H_2, the PtSi sheet resistance varies less and is smaller. Therefore, for this work, the platinum silicidation is performed at 400°C, under N_2H_2 and for 2min. Like for the thermal oxidation, the silicidation is done with consumption of silicon. Indeed, at the end of the process, the PtSi is almost two times thicker than the deposited Pt layer and two-third of that thickness comes from the silicon consumption [Larrieu et al. 2003]. Consequently, for the mechanical resistance of the devices, it is indispensable to avoid the complete consumption of the silicon layer after the silicidation. The choice has been made to deposit only 30nm of Pt on the 60nm of Si. After silicidation, another deposition can be realized on the ohmic contacts to ensure a very good electrical continuity between elements composing the devices.

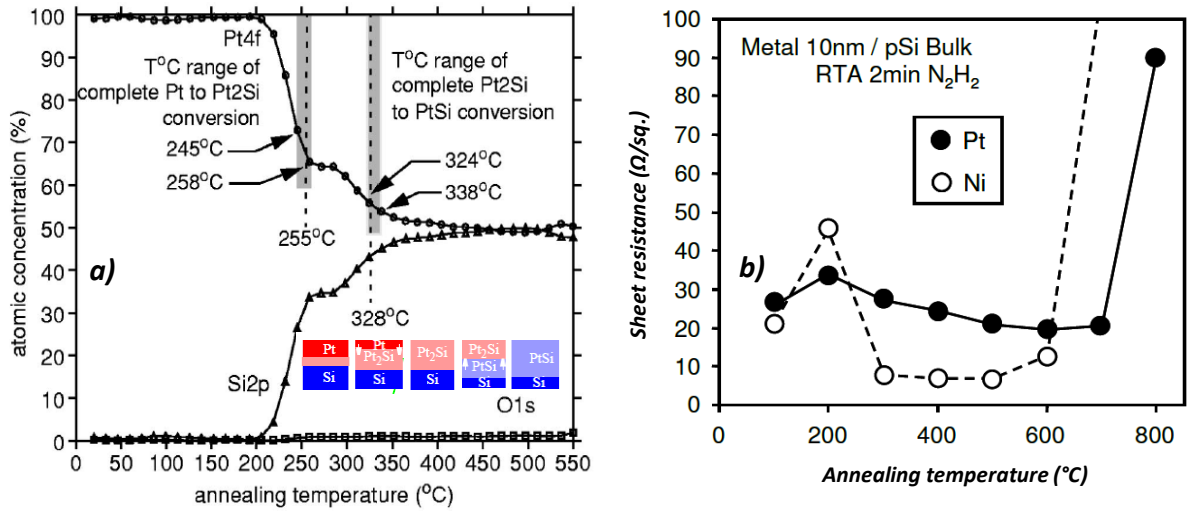


Figure 3- 30: a) Platinum silicide formation mechanism and kinetic [Larrieu et al. 2003] and b) PtSi sheet resistance with respect to the annealing temperature [Breil 2009].

The platinum heaters dedicated to emulate the devices hot sources by Joule effect are realized according to the same recipe except the BOE attack before the 30nm Pt evaporation and the rapid thermal annealing after evaporation (not needed). Figure 3-32 presents the different platinum layers deposited on a TEG's demonstrator.

The electrical continuity between the thermopiles can be performed through two ways:

- First by depositing a Pt layer from one thermopile to another through the intrinsic SOI layer between both thermopiles (cf. figure 3-31-left)
- Second by depositing the metal from on thermopile to another through a silicon nitride layer (cf. figure 3-31-right).

The first way can favor current leakages through the intrinsic SOI while the second can ensure a better insulation of the thermopiles from the rest of the wafer. The measurement results are presented in chapter 4.

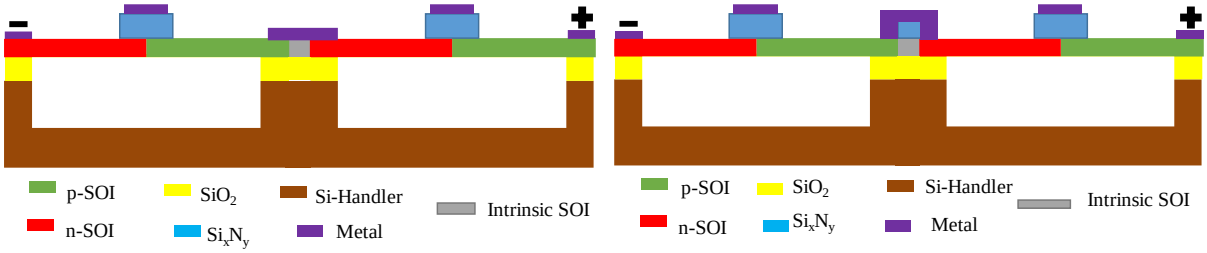


Figure 3- 31: Electrical continuity between thermopiles. Left: Continuity through the intrinsic SOI and right: continuity over a silicon nitride layer deposited on the intrinsic SOI

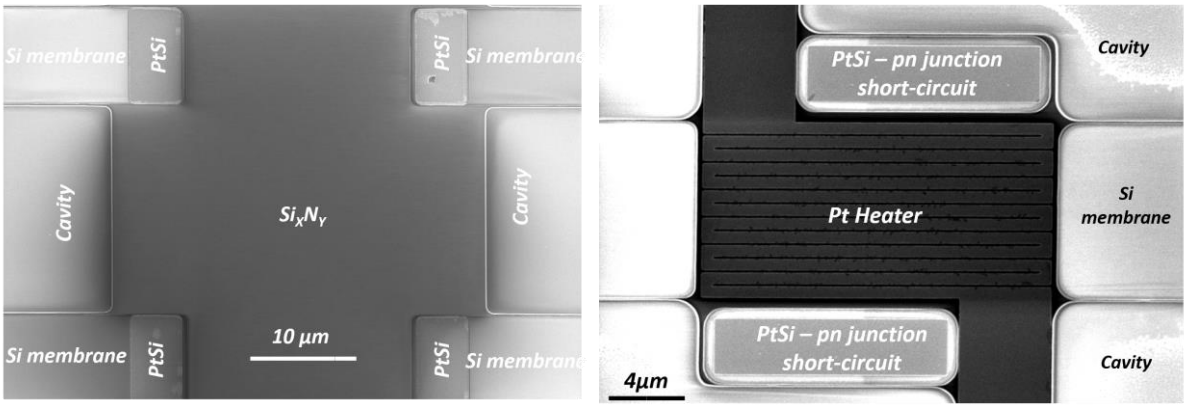


Figure 3- 32: Platinum deposition, left PtSi contacts realization for electrical continuity between thermopiles and right PtSi contacts for the pn junctions short-circuiting and the platinum heater serpentine.

3.2.5.2 Gold metallization

For the sake of thermo-electric measurements, probing pads are required. Gold is chosen, thanks to its softness and ductility. The metal is deposited like the platinum by means of e-beam evaporation. The process (table 3-11) is nearly the same as for the platinum, except the ohmic contact realization and the e-beam lithography parameters.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V1000rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 1.8µm
Lithography	Lithography Writing : Dose 500µC/cm2, current : 50nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Gold evaporation	Ar etching 300eV, 2min – Chromium/Gold evaporation : 125nm/400nm
Resist stripping	Remover PG @ 70°C for 2hours minimum Acetone, IPA rinse – N2 blow dry

Table 3- 11: Gold metallization recipe

Figure 3-33 presents SEM views of the gold metallization of a TEG demonstrator. A layer of chromium is deposited before the gold layer to ensure a better adhesion of the metal on the silicon nitride.

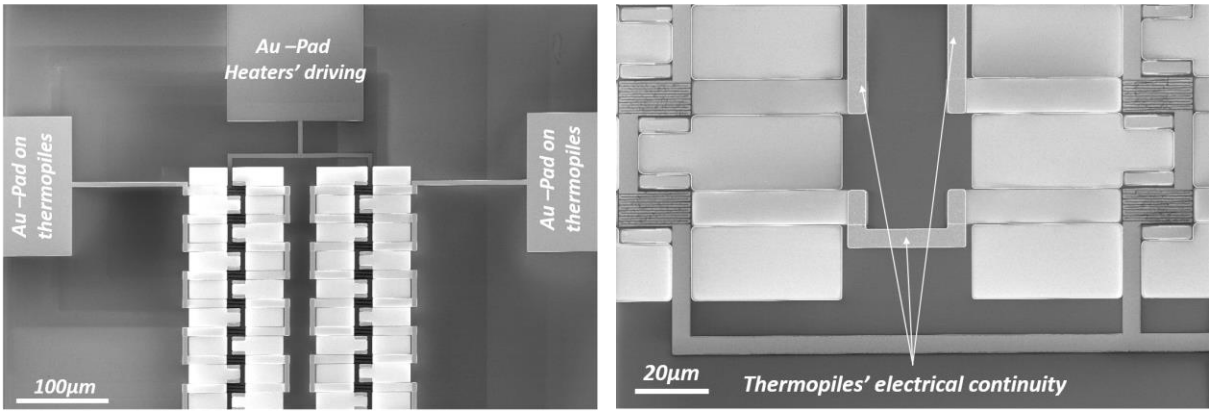


Figure 3- 33: SEM views of TEG demonstrator after Gold deposition. Left: view on some thermopiles and Au pads accesses to drive the Pt heaters and the contacts on the thermopiles, right: close-up view on the electrical continuity between thermopiles

3.2.6 Silicon membranes suspension

The final steps of the devices realization process deal with the silicon membranes thermal insulation from the other layers of the SOI substrate. This is achieved by suspending the silicon membranes. However, before the suspensions, it is necessary to remove the oxide previously grown in the bottom of cavities (cf. figure 3-29) before the metallization steps. For that sake, a last e-beam lithography and reactive ion etching are performed. The following table summarizes the details.

Step description	Step parameters
Resist Spin coating	MAA8.5EL13: V1000rpm, A1000rpm/sec, t12sec Baking @ 180°C for 10 min Thickness : 1.8µm
Lithography	Lithography Writing: Dose 450µC/cm2, current : 25nA, Resolution 25nm Lithography development : MIBK:IPA = 1:2 @ 80rpm for 55 sec – IPA rinse for 40sec
Reactive ion etching	CF4/N2/O2 40sccm/40sccm/5sccm, 100W 30mTorr : Bottom cavities etching (~2.5min)

Table 3- 12: Bottom cavities opening recipe

A reactive ion etching is performed until the complete etching of the oxide present at the bottom of cavities and a slight over-etch of the silicon substrate (cf. figure 3-34) is realized to be sure to remove all the oxide and prepare the XeF_2 etching. The reactive ion etching is preferred to chemical bath (BOE or HF) to avoid etching the grown oxide on the SOI sidewalls. The resist is not stripped after the etching, because it will act as a mask for the XeF_2 vapor etching.

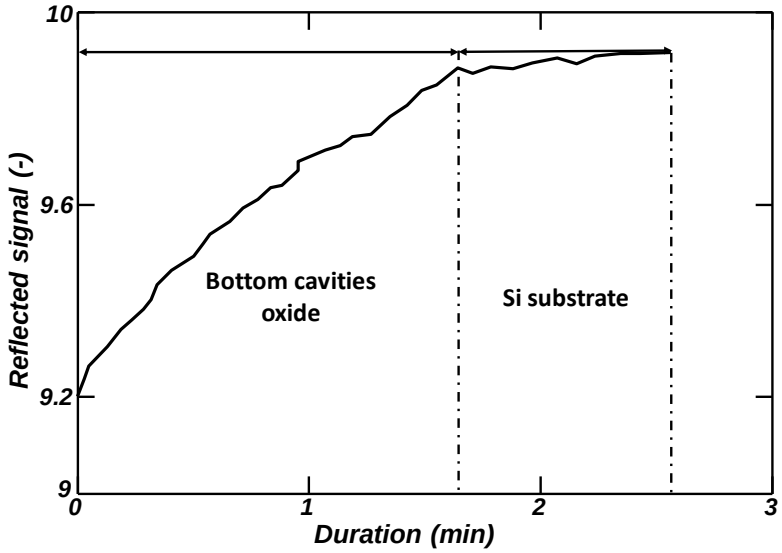


Figure 3- 34: Endpoint detection signal of bottom cavities oxide removal

3.2.6.1 XeF_2 vapor etching

The silicon membranes suspension begins with the releasing of the **SOI-BOX** layers from the silicon handler layer. This releasing consists in etching the silicon substrate under the BOX and the SOI layers. The first idea is to use wet etchant bath such as **KOH** or **TMAH**, however, due to the thin thickness of **SOI-BOX** layers ($\sim 60nm + 145nm$), the stiction issues and capillary forces, dry etching is preferred. This dry etching is performed thanks to gaseous phase of XeF_2. The XeF_2 allows an isotropic etching of the silicon and a very good selectivity to oxide, allowing the use of the SiO_2 as etching mask. However, The BOE bath used before PtSi realization imposes additional precautions (the use of a resist mask plus the oxide). Figure 3-35 presents the XeF_2 etching principle.

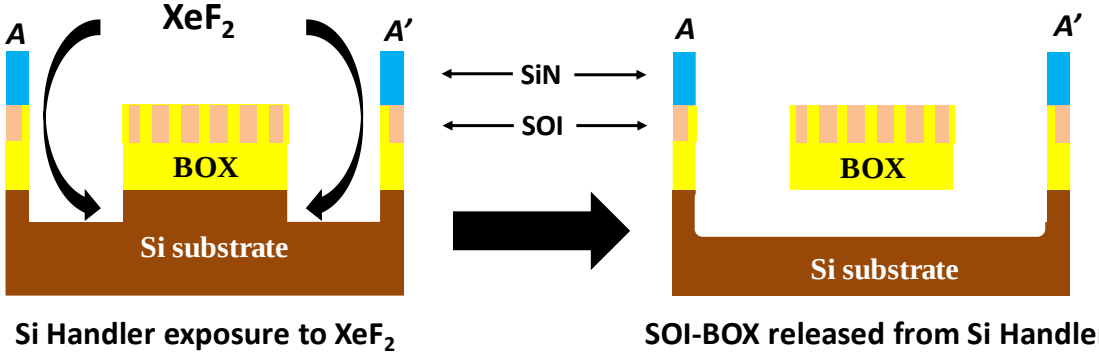


Figure 3- 35: XeF_2 etching process (example of etching of an efficient SiO2 mask).

The XeF_2 etching is performed by cycles. The etching chamber is filled with the etchant gas under 3 Torr and the etching cycle is at last 10sec. When the pump-out pressure (800 mTorr) is reached and for each cycle, the byproducts (**Xe** and **SiF_4**) and the remaining etchants are pumped out of the chamber. The process is repeated until the **SOI-BOX** layers are suspended. Four cycles are needed to completely suspend the **SOI-BOX** layers. Figure 3-36 presents some SEM views of the silicon membranes after the XeF_2 etching. Once the suspension is done, the resist mask is stripped by immersing the samples in an acetone bath (for 2h minimum and at ambient temperature). The samples are afterwards cleaned by IPA and dry by N_2 blow at very low pressure.

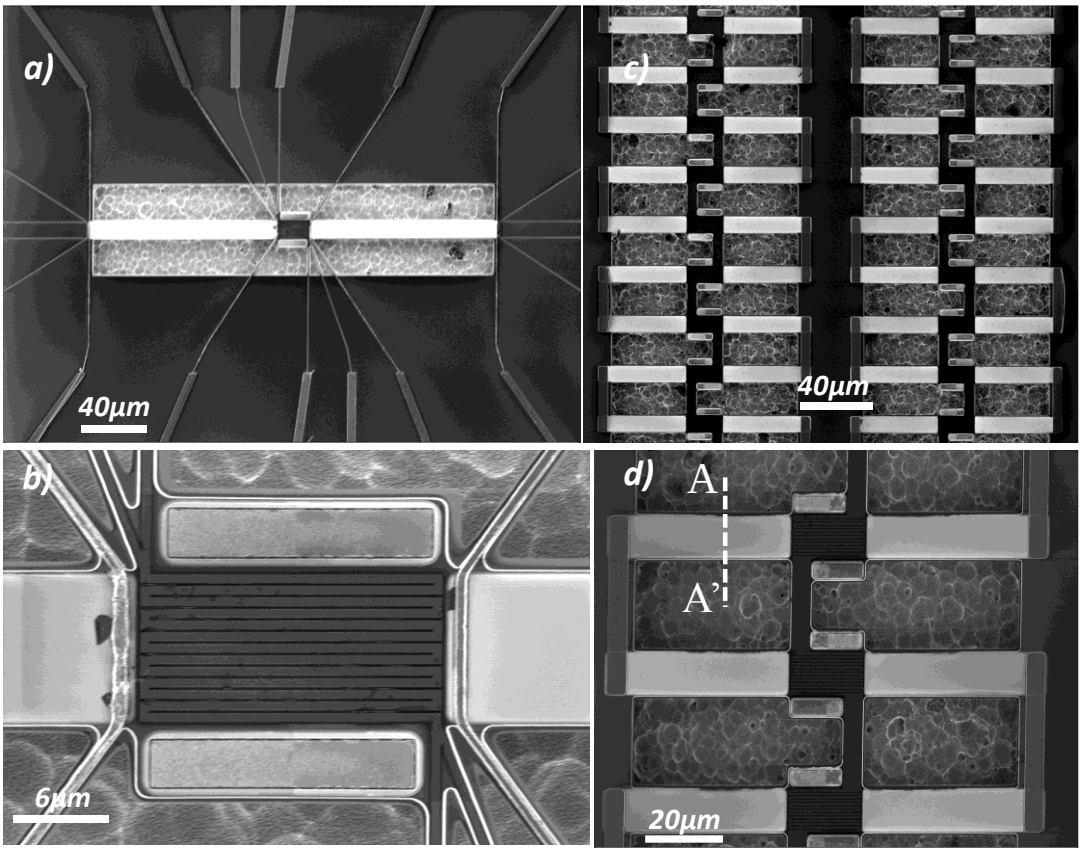


Figure 3- 36: Silicon membranes SEM pictures after XeF_2 etching. a) View of a single thermopile device. b) Focus on the center of that single thermopile (Pt heater, pn junction straps). c) Image of several thermopiles composing a TEG demonstrator. d) Zoom on three of those thermopiles

3.2.6.2 HF Vapor etching

Next step in the silicon membranes thermal insulation is the releasing of **SOI** layer from the BOX. The common way to etch a silicon oxide is to perform a HF etching. Like the previous issue, two possibilities are offered to us: first, a wet HF etching and second, a dry HF etching thanks to the use of a vapor phase HF. The second solution is preferred. In fact, the wet etching presents the disadvantages of increasing the stiction problems and the wet HF favorites the metals' corrosion. The best solution is then vapor HF etching: it provides repeatable, stable etchings and it is compatible with large range of metals. However, the silicon nitride is a critical material during HF vapor etching. Indeed, it can swell and degrade the devices or break the suspended membranes. The solution is to perform a 250°C baking before and after the HF vapor etching for 2min.The HF vapor etching of the silicon oxide reaction given hereafter. The alcohol ionizes the HF vapor and act as catalyst. The 145nm thick oxide and the grown oxide remaining on the silicon membranes are etched during one cycle of 5min, under 190 sccm of HF and 125Torr. Figure 3-37 presents the vapor etching principle of the devices. Figure 3-37 depicts the vapor HF etching principle and figure 3-38 shows some SEM pictures of the silicon membranes after the vapor HF etching.

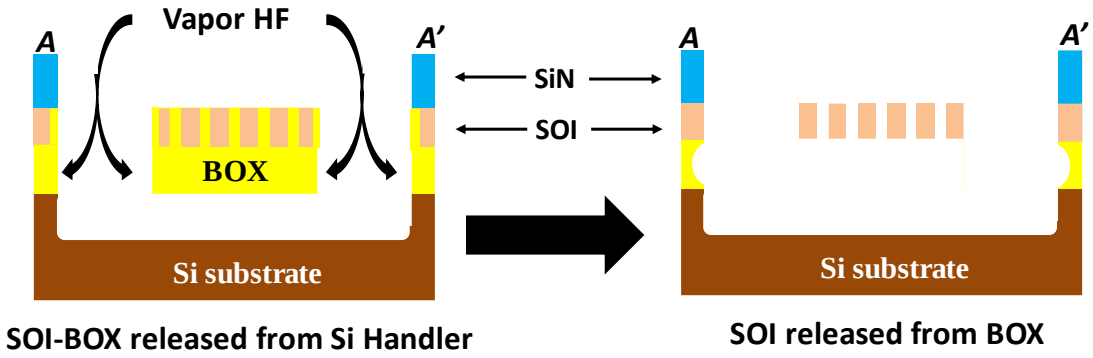


Figure 3- 37: Vapor HF etching principle of the studied devices (view of cut through cavities).

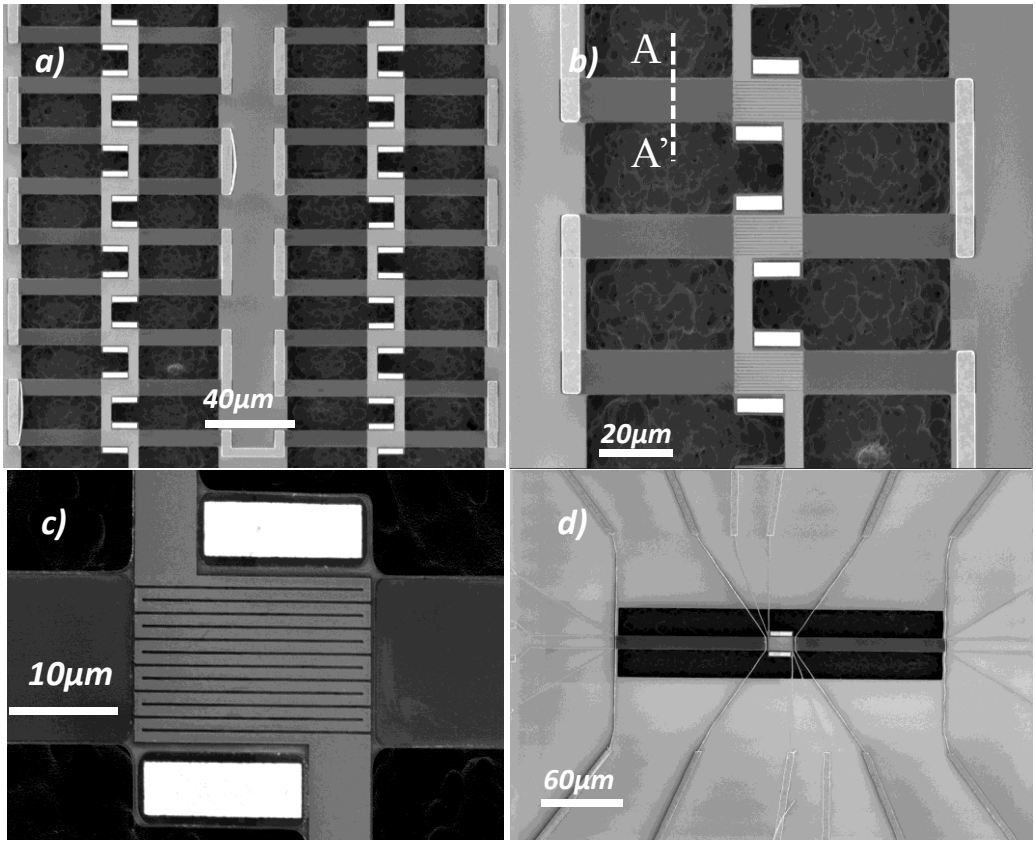


Figure 3- 38: SEM pictures after vapor HF etching. a) SEM pictures of several thermopiles. b) Zoom on three thermopiles. c) Detail of a thermopiles center (Pt heater and pn straps). d) Image of a single thermopile

3.3 The realized devices

The main interest of the carried works is the development and study of a phonon engineered silicon membranes based thermoelectric harvester demonstrator. However, in order to complete the developed demonstrator's characterization, elementary devices allowing the extraction of thermoelectric properties (e.g. the thermal conductivity, the electrical conductivity) are fabricated. Hereafter, we present those different devices.

3.3.1 Electrical conductivity measurements device

The first device (cf. figure 3-39) aims to extract the silicon layer electrical conductivity after the ion implantations and the doping level thanks to the Van Der Pauw methodology. The wafer

contains four cells: two p doped and two n doped. For each doping nature, a version with and without phonon engineered layers is realized. At the center, the silicon doped layer (phonon engineered or not), at the four corner platinum silicide contact for the electrical conductivity measurements by means of four probe resistive measurement. Cavities are etched around the platform to isolate it from the rest of the SOI wafer.

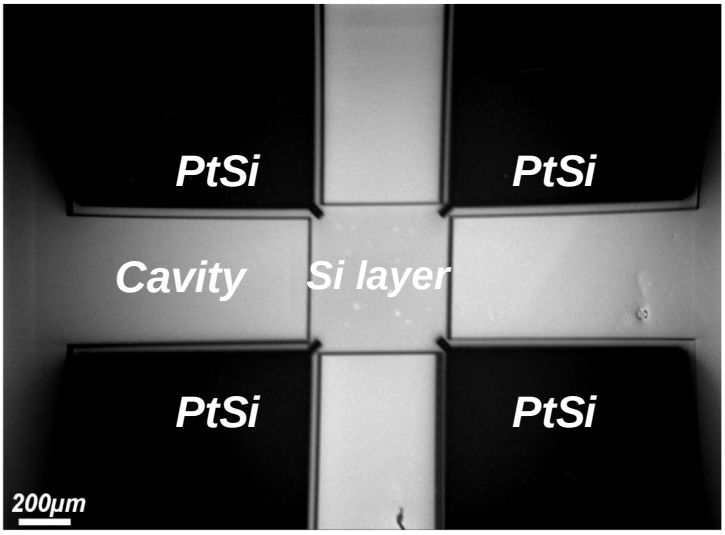


Figure 3- 39: SEM picture of the electrical conductivity measurement device

3.3.2 Thermal gradient management device

This second type of devices (figure 3-40) aims to study the impact of the phonon engineering on non-doped silicon membranes thermal conductivity. The devices are made of pair of suspended silicon membranes (phonon engineered or not). At the center of the platform, a resistive serpentine heater is deposited to emulate by Joule effect the hot source. The extremities are anchored to the SOI substrate. The membranes are all 115µm long, 10µm wide and 60nm thick.

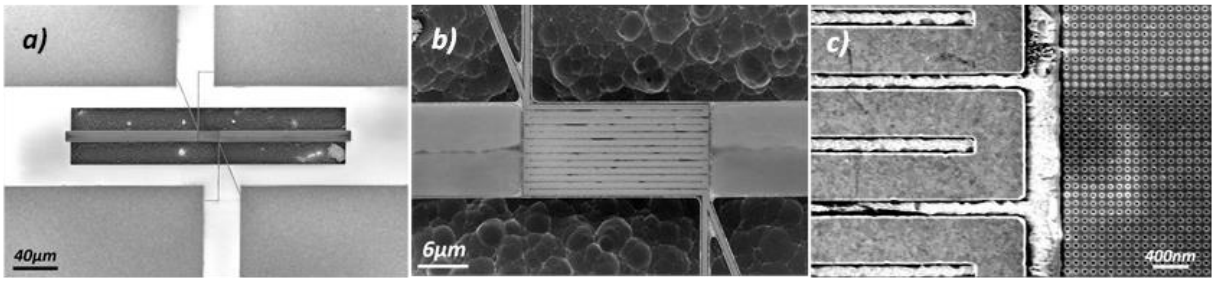


Figure 3- 40: SEM image of the thermal management platform (a). Close-up view of platform's center (b). Platinum resistive heater & detail of phonon engineered lattice (c).

3.3.3 Thermoelectric properties measurements platforms

The third type of devices (cf. figure 3-41) aims to allow the extraction of the silicon membranes thermoelectric properties (electrical conductivity, thermal conductivity and Seebeck coefficient). They are made of one suspended thermopile (p and n-doped membranes, electrically in series and thermally in parallel). It is made of a resistive platinum heater at the center of the thermopiles, four electrical contacts (platinum silicide) on each silicon membranes to allow the electrical conductivity measurements by means of probe resistive measurement also and Seebeck coefficients. Metallic contacts (four probes) at the thermopiles extremities on silicon nitride for cold ends temperature measurements. Unfortunately, the several contacts on the thermopiles weaken them (cf. figure 3-41 c) and d)). In addition, several Pt discontinuity

are observed (cf. figure 3-41 e). Therefore, these devices cannot be characterized with confidence.

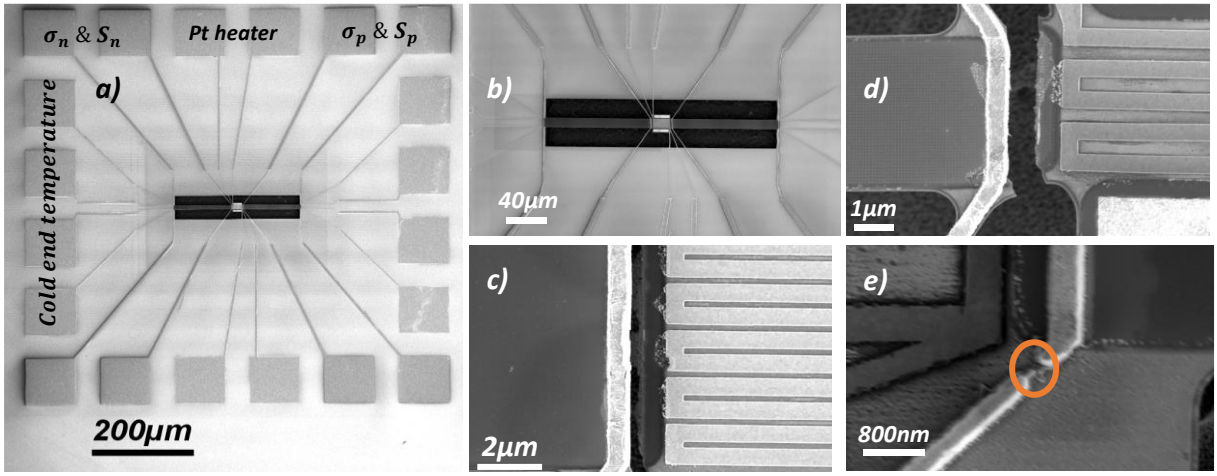


Figure 3- 41: SEM image of the parametric device a). Zoom on the thermopile (b). Focus on the suspended PtSi contacts (c-d) image of the thermopile extremities (e)

3.3.4 Thermoelectric harvester demonstrators

The thermoelectric harvester demonstrators (cf. figure 3-42) are made of an association of a several thermopiles, electrically in series and thermally in parallel. Like for the thermal devices, Joule effect thanks to a resistive platinum serpentine deposited at the center of the thermopiles will simulate the hot sources. The extremities of the thermopiles are anchored to the SOI substrate, allowing a better heat dissipation at the cold ends.

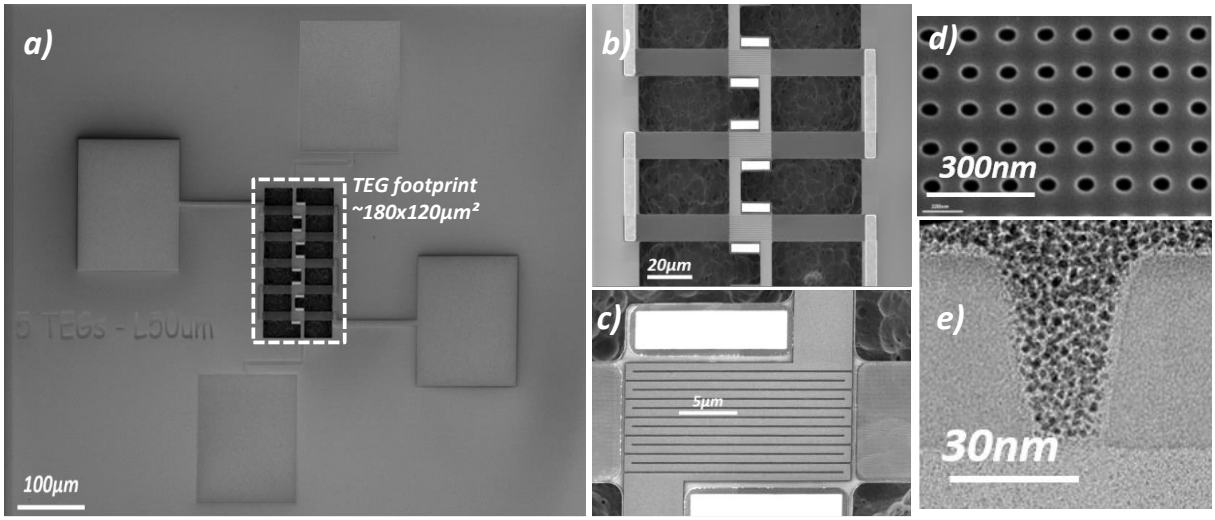


Figure 3- 42: SEM view of 5 thermopiles thermoelectric generator demonstrator (a). Close-up view of some thermopiles and the electrical continuity (b). Platinum heater serpentine (c). Details of phononic crystals (d). TEM cut before suspension of the membranes (e)

Conclusion

This third chapter tackled the silicon harvester demonstrators design (according to the modeling results) and realization. The demonstrators were realized with and without phonon engineering in order to allow the study of the phonon engineering impact on the thermoelectric performances. Moreover, as complement to the demonstrators, three other devices were realized on the same wafer. These devices aimed to allow the study of the phonon engineering on the silicon thermoelectric properties (Seebeck coefficient, thermal conductivity and

electrical conductivity). The devices where realized from a SOI wafer according to a CMOS compatible process whose main steps were:

- The SOI wafer's top layer patterning by means of e-beam lithography and Cl_2/Ar Reactive-Ion-Etching (RIE)
- SOI electrical properties modification by mean of ion implantations
- Materials deposition on that top layer by means of Low-Pressure-Chemical-Vapor-Deposition (LPCVD) and e-beam evaporation.
- Thermal insulation of the top layer from the others layer of the SOI by XeF2 and HF vapor etching.

Table 3-13 reports the thermal conductivities of the main materials used for the development of the silicon thermoelectric harvester demonstrators.

Material	Si membrane [Haras et al. 2016]	SiO_2 [Yamane et al. 2002]	SiN [Ftouni et al. 2015]	Pt [Zhang et al. 2005]
κ (W/m/K)	Plain : ~59 PE : ~34.5	~1.5	~3	~71W/m/K

Table 3- 13: Thermal conductivities of main materials used for the demonstrators realization

Chapter 4: Silicon based thermoelectric harvester demonstrators characterization

Abstract

This last chapter aims at characterizing the different devices realized during this thesis work and discuss the different results. The chapter will be divided in 4 main parts:

- First, the description of the different characterization protocols: How the measurements are performed on the different devices, the measurement conditions, …
- Second, the chapter interest in the thermoelectric properties on the different elementary devices (all except the demonstrators) and especially, the impact of the phonon engineering on those thermoelectric properties.
- Third, the demonstrators' characterizations are performed. In this third section (the main one), the demonstrators' characterization methodologies are detailed before focusing on extracting the different thermoelectric performances (thermoelectric voltage, produced electrical power, …) and the performance discussion with respect to the modeling results presented in chapter 2 and the state of the art micro-harvesters' performance.
- Finally, after the problematic of thermoelectric harvesting, the chapter deals with the possibility of using the developed demonstrators as thermoelectric coolers through the investigation of the Peltier effect.

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4.1 Characterization protocol

The devices' characterizations are performed in four-probe measurements station and with the help of a semiconductor parameter analyzer. However, they are classified in two categories:

- The doping level/electrical conductivity measurement performed in ambient air
- The thermal conductivity/thermoelectric performance measurement performed in vacuum to get rid of heat losses by conducto-convection in air.

4.1.1 Doping level / Electrical conductivity measurement

4.1.1.1 Principle

The doping level estimation consist in the measurement of the electrical conductivity or resistivity of the doped silicon layers and the conversion of that electrical conductivity to a doping level thanks to an abacus [Sze 1981] in figure 4-1. The abacus is based on bulk silicon electrons and holes mobility models with doping levels. The studied layers being thicker than the electrons' mean free path, we assume the same model explains our thin films and bulk silicon.

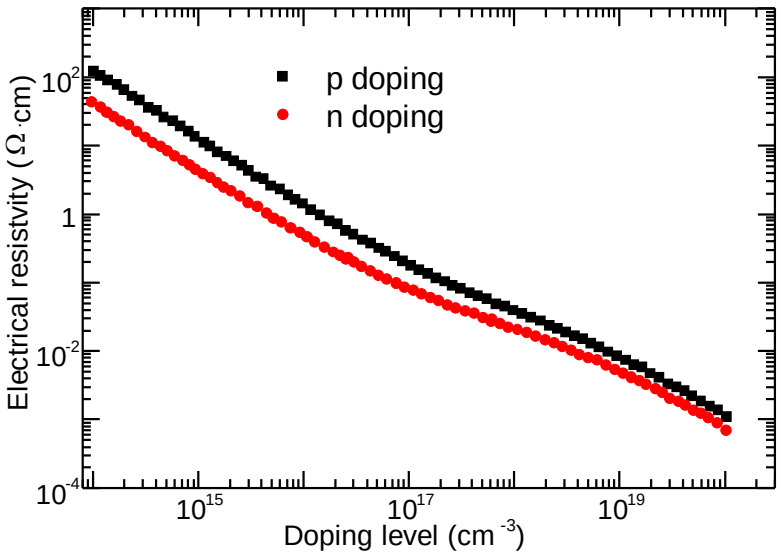

Figure 4- 1: Silicon's electrical resistance versus doping level [Sze 1981]

The electrical conductivity measurement is performed thanks to the "Van Der Pauw (VDP)" method. The VDP method [Van Der Pauw 1958; Ramadan et al. 1994; van der PAUW 1991] is commonly used to measure resistivity and Hall coefficient of a sample. This method has the main advantage to allow the measurement of the average conductivity of any arbitrary shape samples, since it is approximatively two-dimensional (much thinner than wider) thanks to four probes at the samples perimeter. However, for an accurate measurement with the VDP method, the following conditions must be fulfilled:

- Flat shape and uniform thickness
- No isolated holes on the sample
- Homogenous, symmetrical sample
- The electrical contacts must be absolutely at the edge on the sample and arranged symmetrically

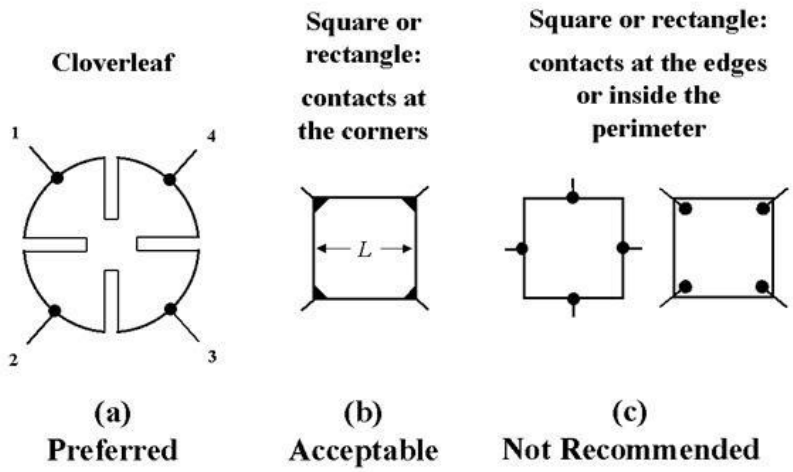

Figure 4- 2: Samples' choice for VDP electrical conductivity measurements

The sample is provided with four contacts at arbitrary places, numbered from 1 to 4 (cf. figure 4-2a). A direct current (DC) is applied from contact 1 to 4 (I_{14}), we then measure the potential difference at the two others contacts (V_{43}) to define the sample's "vertical" resistance: $R_V = \frac{V_{43}}{I_{12}} = \frac{V_{12}}{I_{43}}$. Analogously, the sample's "horizontal" resistance is define as: $R_H = \frac{V_{23}}{I_{14}} = \frac{V_{14}}{I_{23}}$. The electrical resistivity determination relies on the theorem that between R_V and R_H exists the following relation[Van Der Pauw 1958; van der PAUW 1991]:

$$\exp\left(-\frac{\pi \cdot t}{\rho} \cdot R_V\right) + \exp\left(-\frac{\pi \cdot t}{\rho} \cdot R_H\right) = 1 \qquad \textit{Equation 4- 1}$$

Where t and ρ are respectively the sample's thickness and electrical resistivity. The equation resolution is straightforward if the sample possesses a symmetrical line and the contacts disposed symmetrically (figure 4-2 a and b). Indeed, in this situation, the contacts are all equivalent and the "vertical" and "horizontal" resistances too. The electrical resistivity is then defined as:

$$\rho = \frac{\pi \cdot t}{\ln(2)} \cdot R_V = \frac{\pi \cdot t}{\ln(2)} \cdot R_H \qquad \textit{Equation 4- 2}$$

However, if the sample is not symmetrical line and/or the contacts are disposed arbitrarily, solving the equation 4-1 is more difficult. The electrical resistivity is then defined as:

$$\rho = \frac{\pi \cdot t}{\ln(2)} \cdot \frac{R_V + R_H}{2} \cdot f \qquad \textit{Equation 4- 3}$$

f being a form factor, only function of the "vertical" and "horizontal" resistances and given in figure 4-3. The electrical resistivity obtained in this condition is not the most accurate, explaining why it is indispensable as much as possible to design symmetrical measurement platform and dispose the contacts symmetrically (figure 4-2 a or b).

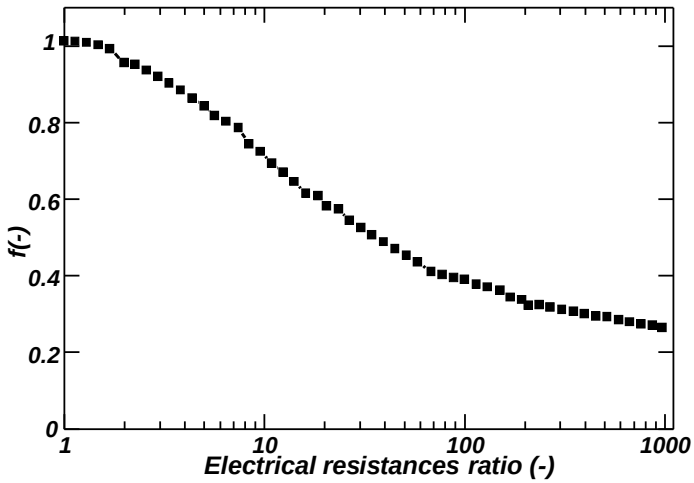

Figure 4- 3: Electrical resistivity correction factor with respect to the "vertical-horizontal" resistances ratio [Van Der Pauw 1958]

4.1.1.2 Measurement conditions

The electrical measurement is performed on a "cloverleaf" architecture platform (figure 4-2a). The interesting layer is at the center of the platform and the electrical contacts at the extremities, disposed symmetrically (cf. section 3.3.1). Measurements are performed in a DC four-probe measurement station. The probes are connected to a HP/Agilent 4155C semiconductor parameter analyzer, used as an accurate voltage source and current or voltage measurement unit. The HP4155C presents four source monitor units (**SMU**) which can be used as voltage source-current measurement unit or current source-voltage measurement unit, two voltage measurement units (**VMU**) only dedicated to voltage measurement and two voltage source unit (**VSU**). The **SMUs** will be used only as voltage source-current measurement units because the **VMUs** allows a better voltage measurement accuracy ($\pm 0.2\mu V$ against $\pm 2\mu V$ and $\pm\, 1nA$ for the **SMUs**). **VMUs** will be used only for potential difference measurements (ddp between two points).

The device is voltage biased on two contacts and on the two other contacts through **SMUs**, the potential difference induced by the current from voltage-biased contacts is measured thanks to **VMUs**. The electrical current in the silicon layer is measured by **SMUs**. This operation is performed for both "vertical" and "horizontal" electrical resistances measurements. Figure 4-4 presents the measurement platform and configurations.

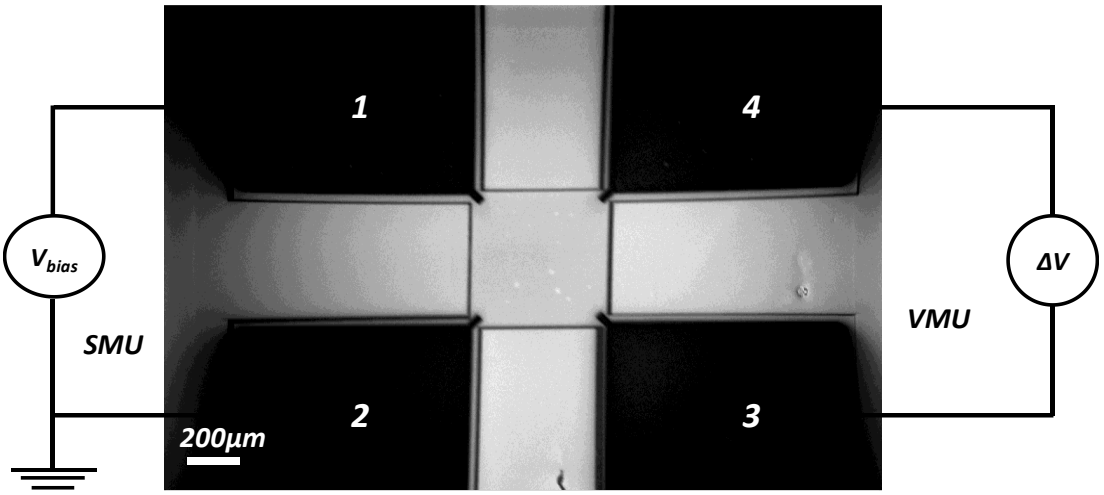

Figure 4- 4 : Electrical conductivity measurement Platform and configuration

4.1.2 Thermal gradient management

4.1.2.1 Principle

The thermal conductivity and thermoelectric performance characterization method is based on an electro-thermal approach. Indeed, the devices' hot sources are simulated by Joule effect thanks to platinum (Pt) resistive serpentines. The electro-thermal method relies on the assumption that the electrical power (**P_H**) generated in the Pt heater is totally converted as an efficient heat flow (**Q_H**). To fulfill this assumption, the top SOI layer is completely suspended to ensure its high thermal insulation from the rest of the wafer and the measurements are performed under vacuum to get rid of the conducto-convection in air. The heat flow (**Q_H**) generated in the Pt heater is transferred to the SOI membranes as presented in figure 4-5 from the center of the platform to the extremities by thermal conduction. The platform being symmetrical, the heat flow is divided in two equal contributions (**$Q_H/2$**) and the membranes. The silicon membranes' thermal conductivity can then be defined in a first approximation by Fourier law as:

$$\kappa = \frac{1}{2} \cdot \frac{Q_H}{(T_H - T_C)} \cdot \frac{L}{w \cdot t} \qquad \textit{Equation 4- 4}$$

T_H, T_C, L, w and t being respectively, the temperature at the hot source (center of the platform), the temperature at the cold ends (platform's extremities), the membranes' length between the platform's center and extremities, the membranes width and the membranes thickness.

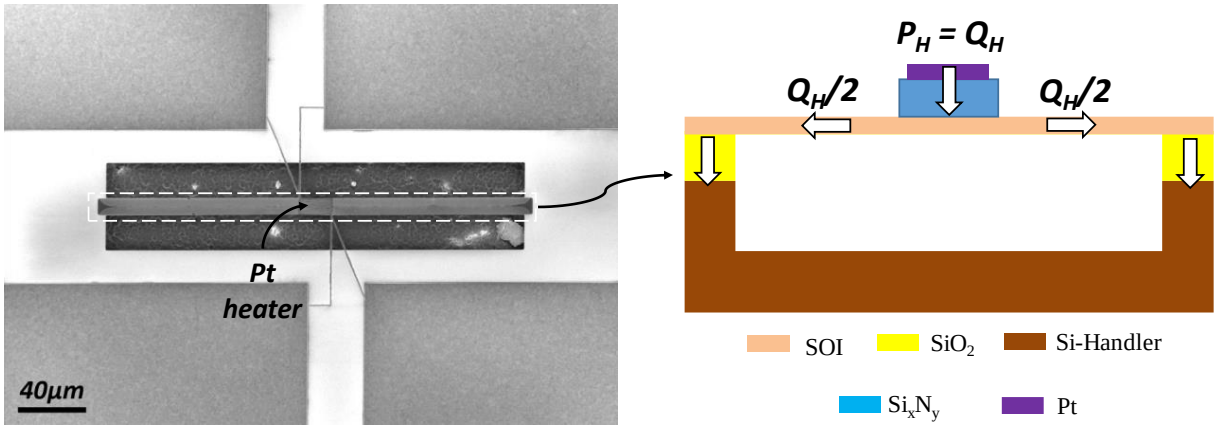

Figure 4- 5: Electro-thermal characterization principle. Left: top view of a suspended platform for thermal gradient management. Right: cross-sectional side view through the device along the membranes

The temperature difference between the center of the platform and its extremities is indispensable to obtain the silicon membranes' thermal conductivity and to fulfill the thermoelectric harvesters' characterization. This temperature difference is linked to the Pt heater serpentine temperature elevation due to the electrical power injected. Indeed, the Pt electrical resistance (resistivity) increases with the temperature due to the carriers' lifetime associated to electron-phonon collisions. The electrical resistance at given temperature T is then defined as follows:

$$R_{Pt}(T) = R_{Pt}(T_0) \cdot (1 + \alpha \cdot \Delta T) \qquad \textit{Equation 4- 5}$$

Where T_0, α and ΔT being respectively, the initial temperature (generally ambient), the platinum's temperature coefficient of resistance (TCR) and the temperature elevation $(T - T_0)$.

4.1.2.2 Characterization conditions

The characterizations are performed in a four probes DC point probes measurement set-up, equipped with a vacuum chamber (down to $4 \cdot 10^{-6}$ Torr). The vacuum allows neglecting the conducto-convection in air, which represents the main source of heat losses. The vacuum chamber is equipped also with temperature-controlled chuck to allow the heating of the sample. Figure 4-6 a presents the measurement set-up and figure 4-6 b the placement of the sample in the chamber. The probes are connected to the HP/Agilent 4155C presented earlier.

The first part of the characterizations is the Pt heater serpentine calibration to extract the TCR α. The methodology consists of varying the chuck's temperature while biasing the heater with a constant voltage (10mV for example). Then, we register the Pt electrical resistance variation with the temperature and extract α thanks to equation 4-5. Second the chuck is maintained at a constant temperature (25°C for example) while the Pt heater is biased with a variable voltage. Knowing α, the electrical resistance increase due to the bias voltage variation is converted into temperature thanks to the equation 4-5 too (T_0 being the chuck's constant temperature).

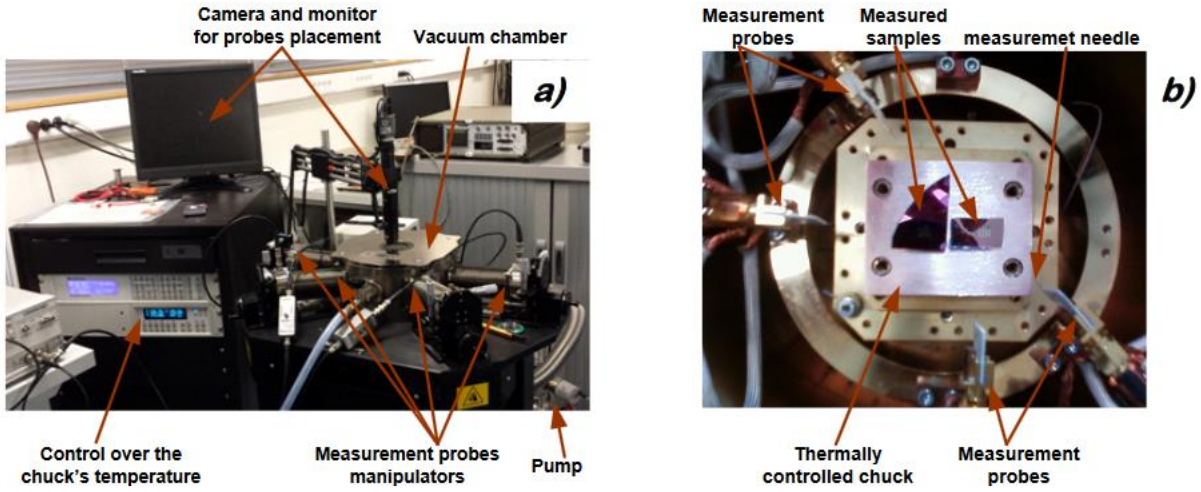

Figure 4- 6: Measurement set-up (a). Detail of the samples in the vacuum chamber (b)

4.2 Thermoelectric properties characterization

4.2.1 Doping level

The doping levels are measured from the devices presented in chap3-II-1 and according to the measurement methodology presented earlier (section I-1) and in figure 4-3. The doping level measurements are performed only on the devices containing plain silicon layer. Indeed, the measurement methodology do not guarantee sufficient accuracy for devices with phononic engineering.

The devices are voltage biased by sweeping from -1V to 1V through two **SMUs** (the output current is measured by the same **SMUs**) in ambient air (no sample heating or vacuum for these measurements). The potential difference (ΔV) induced by the current generated by the bias voltage is sensed by the **VMUs** according to figure 4-4. Each measurement is hold during 10 seconds and the HP4155C integration mode is set to medium for a better measurement accuracy.

Figure 4-7 presents the results of the measurements performed on a 60nm thick plain p-Si layer (left) and n-Si layer (right). The figures present the induced potential difference with respect to the electrical current through the layer for both "horizontal" and "vertical" measurement configurations. A slight shift between "horizontal" and "vertical" electrical resistances is noticed for the p-Si layer ($R_H/R_V \approx 1.2$) and a complete superposition for the n-Si layer ($R_H/R_V \approx 1$). The slight shift can be due to a dissymmetry of the contacts on the p-Si layer. Equation 4-3 allows the p and n electrical resistivity computation, table 4-1 cosigns the results. In the table are also consigned the values of the "geometry factor" f from figure 4-3 with respect to the "horizontal" and "vertical" electrical resistances ratio. The electrical resistivity values reflect doping levels slightly inferior to $1 \cdot 10^{19} cm^{-3}$ (cf. figure 4-1), which was the target.

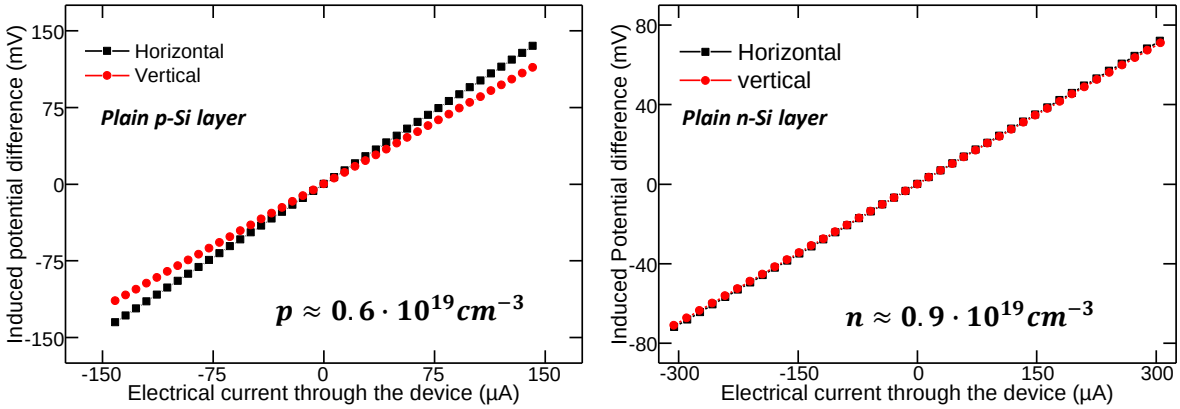

Figure 4- 7: Plain p-Si (left) and n-Si (right) layers' electrical resistances

Si layer	$R_H(\Omega)$	$R_V(\Omega)$	Resistances ratio (-)	f(-)	***ρ(Ω·cm)***	***Doping level (cm^{-3})***
p-doped	956	771	1.2	0.9971	$2.341 \cdot 10^{-2}$	$\sim 0.6 \cdot 10^{19} cm^{-3}$
n-doped	236	233	1	1	$6.377 \cdot 10^{-3}$	$\sim 0.9 \cdot 10^{19} cm^{-3}$

Table 4- 1: 60nm thick plain p-Si and n-Si layers electrical resistivity and doping levels

4.2.2 ***Phononic engineering impact on the electrical conductivity***

Despite the doping levels estimations, the main interest of the electrical conductivity measurement devices is the phononic engineering impact on the silicon membranes' electrical conductivities. In order to allow a confident comparison with non-phonon engineered membranes, designs and characterization of both phonon engineered and non-phonon engineered devices' are identical. Figure 4-8 reports the phonon engineered p-Si (left) and n-Si (right) "horizontal" and "vertical" electrical resistances. The "vertical"/"horizontal" electrical resistances ratio are close to those of the non-phonon-engineered layers. The electrical resistances are doubled when the phonon-engineering lattice patterns the layers (cf. table 4-2).

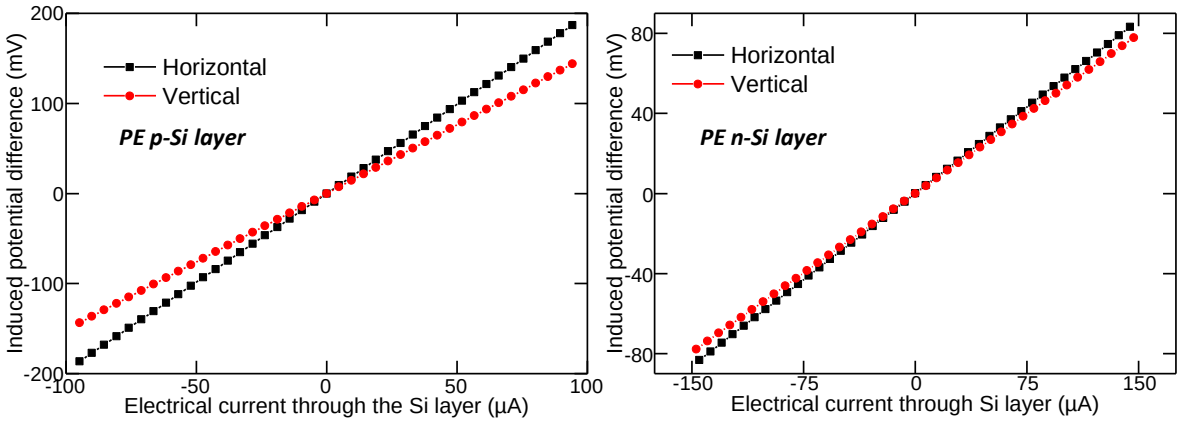

Figure 4- 8: Phonon-engineered p-Si (left) and n-Si (right) layers' electrical resistances

Si layer	$R_H(\Omega)$	$R_V(\Omega)$	Resistances ratio (-)	f(-)
p-doped	~1900	~1500	~1.3	0.9941
n-doped	~576	~530	~1.1	0.9992

Table 4- 2: Phonon-engineered p-Si and n-Si layers' electrical resistances

It was foreseeable that the electrical resistances will increase with the phonon engineering because the phonon engineering is done with material removal for the electronic transport. However, does only the material removal explain this resistances increase? **In other words, does this electrical resistances increase obtained without increase of the electrical resistivity?** This question can be answered by a finite element modeling of plain and PE Si layers like those measured (if yes the FEM will match the measurements). To reflect the PE measured layers, the PE models must have the same porosity than the PE measured layers. The porosity is defined as the total surface occupied by the holes over the plain layer surface, equivalent to the surface occupied by one hole over the surface of a square which side is the phononic lattice pitch. The following relation then gives the porosity and the phononic lattice being made of 40nm diameter holes spaced by a pitch of 100nm, the lattice porosity is about 12.5%

$$\text{porosity} = \frac{\pi d^2}{4 * pitch^2} \qquad \textit{Equation 4- 6}$$

For the FEM study, 60nm thick, 520nm long and wide Si layer is considered (figure 4-9). The PE layer is patterned with a 25 holes lattice of 40nm diameters, 100nm pitches, a porosity of about 12% (close to measured layers). At the four layers' corners and at the edges, Pt pads at deposited to mimic the Van-Der-Pauw methodology. For these studies, we assume that the electrical conductivity is not affected by the phonon-engineering (same electrical conductivity for both plain and PE layers). A constant current (100µA) is injected in the layers through the pad 1, the pad 4 is at the ground and the induced potential difference is measured at the pads 2 and 3.

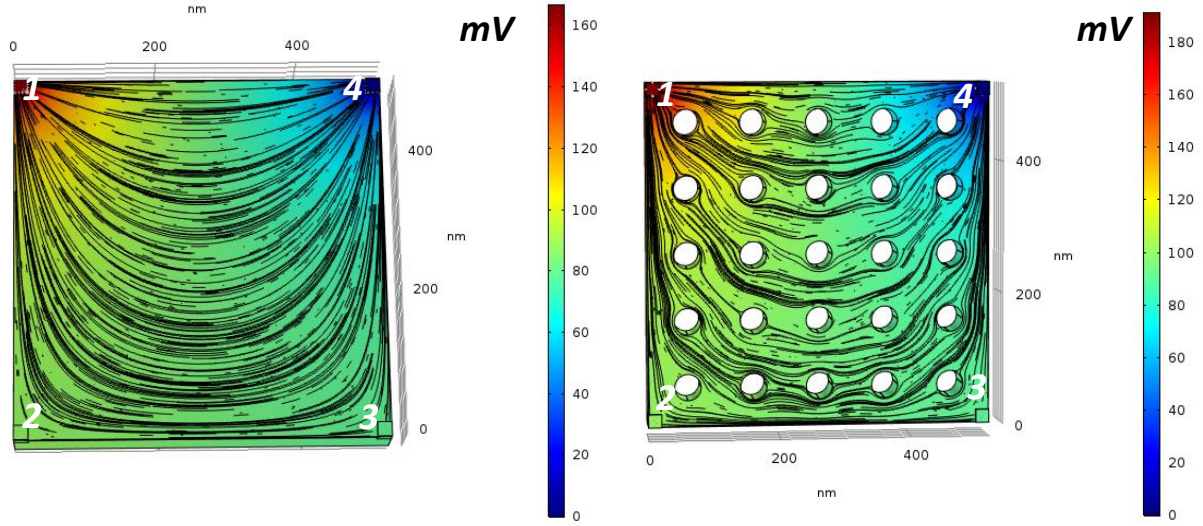

Figure 4- 9: FEM study of PE impact on electrical resistance (Left: plain Si layer. Right: PE Si layer). Voltage mapping on the Si layer for an arbitrary electrical conductivity and the electrical current streams (black)

Table 4-3 reports for both values of electrical resistivity measured earlier, the potential differences induced by the injection of 100µA through the PE and plain silicon layers. As

expected and observed by the measurements, phonon-engineering increases the layers' electrical resistance (increase of the voltage for a same current). However, the increase is less important than observed with the measurements, leading to reject the hypothesis of electrical conductivity conservation with the phonon engineering. Indeed, with the measurements, we observed an electrical resistance increase of about 2-fold while the FEM depicts an increase of barely 1.3-fold, **leaving 1.5-fold that we can assume is due to an increase of electrical resistivity**. The carriers' density of states modification by phonon engineering can explain the electrical conductivity decrease.

$\rho_{Si}(\Omega \cdot cm)$	ΔV_{PE}(mV)	ΔV_{Plain}(mV)	$\Delta V_{PE}/\Delta V_{Plain}(-)$
$6.377 \cdot 10^{-3}$	30.39	23.42	~1.3
$2.341 \cdot 10^{-2}$	109.72	84.58	~1.3

Table 4- 3: FEM study of the PE impact on the electrical resistance

4.2.3 Phononic engineering impact on the temperature gradient management

The devices presented in chap3-III-2 are used to study the impact of the phononic engineering on the thermal gradient management through the silicon membranes. As explained in section I-2, the study is performed under vacuum and according to two steps: the Pt heater serpentine calibration and the phonon engineering impact on the temperature gradient management.

4.2.3.1 Pt heater serpentine calibration

The Pt heater serpentine calibration consists in measuring the Pt heater's electrical resistance increase with the chuck's temperature. The chuck's temperature is varied from $\sim 23°C \; to \sim 65°C$ and for each chuck's temperature value, a four probe electrical resistance measurement is performed on the Pt heater thanks to the HP/Agilent 4155C **SMUs** and **VMUs**. The heater is biased by a constant 10mV at each chuck's temperature on two contacts and the exact voltage drop in the heater is measured through the two other contacts (cf. figure 4-10).

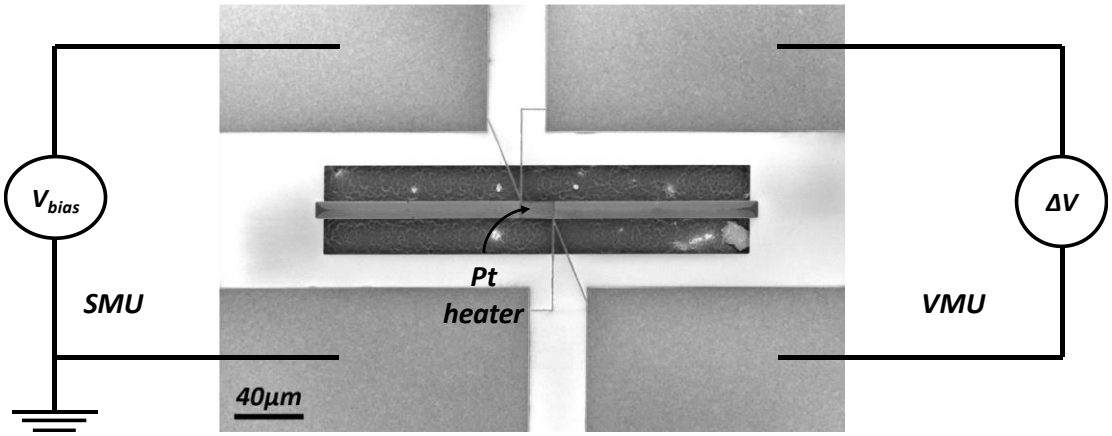

Figure 4- 10: Pt heater electrical resistance measurement for both heater calibration and phonon engineering impact study

As expected the Pt electrical resistance increases with the chuck's temperature, this increase is linear (figure4-11) as predicted by equation 4-5, the TCR α is calculated thanks to that equation and is $\mathbf{2.5 \cdot 10^{-3} K^{-1}}$.

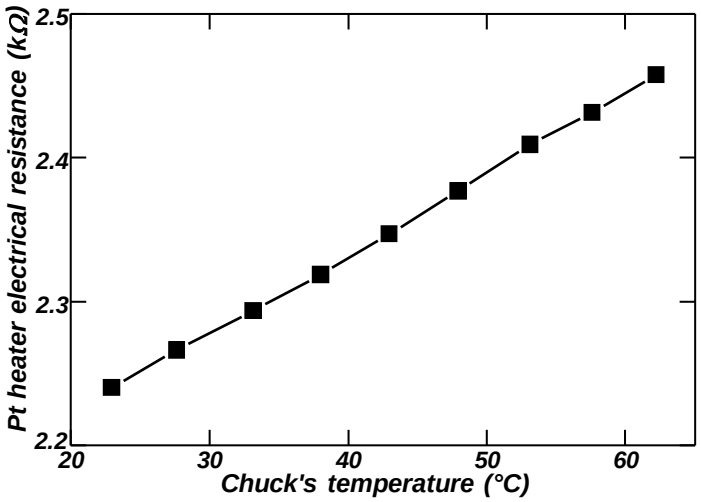

Figure 4- 11: Pt electrical resistance variation with the chuck's temperature

4.2.3.2 Temperature gradient management

The temperature difference across the silicon membranes for the same heating power evaluates the impact of the phononic engineering on the temperature gradient management. Indeed, the devices being identical except the phononic engineering, any gap of temperature difference across the silicon membranes for the same heating power can only be due to the phononic engineering.

The measurements methodology is the opposite of that of the heater calibration. This time, the chuck is maintained at constant temperature (25°C) while the bias voltage (cf. figure 4-11) varies from 50mV to 2V. This voltage bias variation implies the Pt heater's electrical resistance variation (cf. figure4-12 left) and from this resistance variation, the Pt temperature elevation (figure 4-12 right) is calculated thanks to equation 4-5 and the TCR determined earlier.

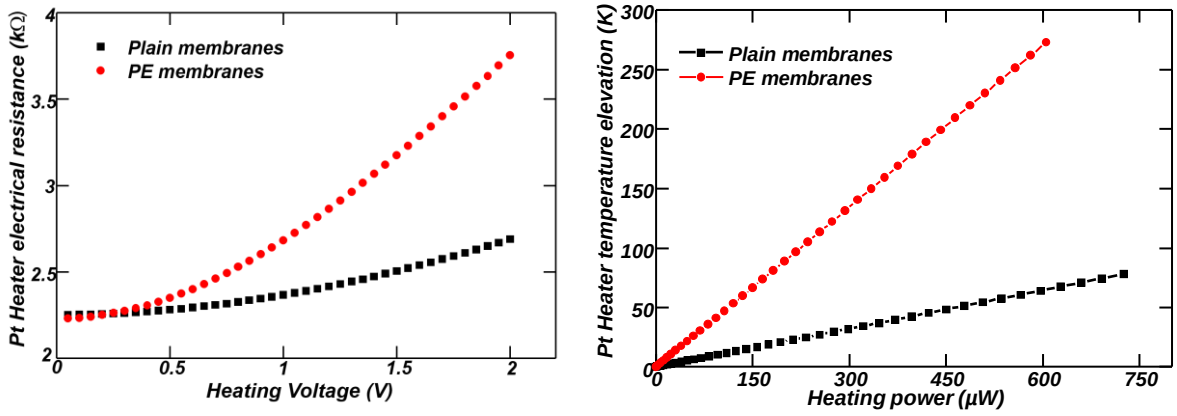

Figure 4- 12: left: Pt heater electrical resistance variation with the heating voltage (bias voltage). Right: Pt heater temperature elevation with the heating power

Figures 4-12 reports both higher electrical resistance variation and temperature elevation for phonon engineered silicon membranes. This reflects an increase of the device's thermal resistance with phonon engineering. This thermal resistance increase is actually only due to the silicon membranes. Indeed, the device can be modeled as an association of thermal resistances (cf. figure 4-13), with the membranes and the heater's access beams resistances in parallel. The access beams being identical for all the devices, the gain of temperature difference is only due to the membranes. In this case, the membranes patterning of holes' lattice of 40nm diameter-

hole and 100nm pitch on a 115µm long and 10µm wide membranes allows the increase of the temperature difference in the structure by a factor 4.5.

The only difference between the devices being the phononic engineering, in a first approximation the thermal resistance can be considered being increase by a factor 4.5 too. However, for a better accuracy, it would have been interesting to be able to quantify the different contributions (especially the access beams contributions) to the thermal gradient. Unfortunately, this design does not allow it and the devices designed to do it turned out broken (cf. figure 3-41). The phononic engineering impact on the temperature gradient is then only characterization done in terms of thermal resistance increase. In [Haras et al. 2016] is presented a complete study of the phononic engineering impact on the thermal gradient across silicon membranes.

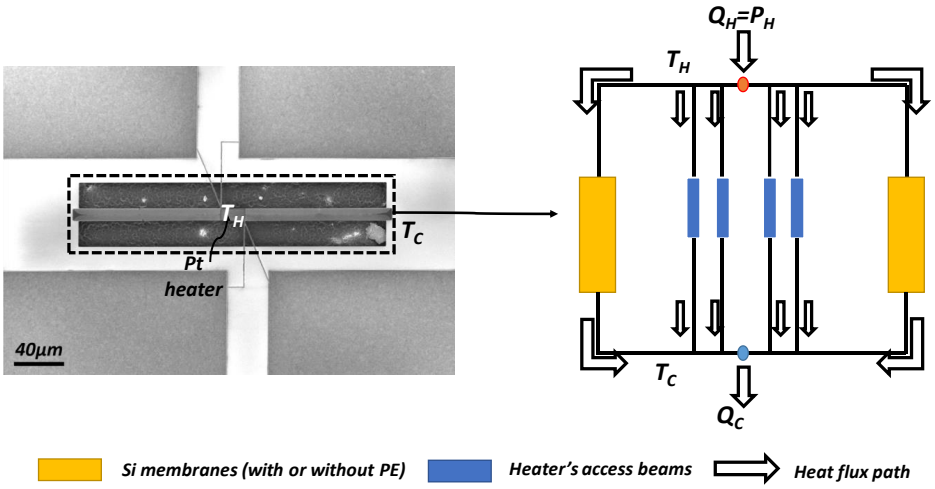

Figure 4- 13: Equivalent thermal resistances' circuit of the thermal gradient management device. Left: SEM picture of the device. Right: the equivalent thermal resistances of the device.

4.3 Thermoelectric harvester demonstrators

This chapter's third part deals with the thermoelectric harvester demonstrators' (cf. section 3.3.4) characterization. The demonstrators are made of several suspended thermopiles associated electrically in series and thermally in parallel (Figure 4-14-a). A silicon nitride layer is deposited between the thermopiles and the Pt heaters in order to reduce the current leakage from the heaters to the thermopiles as much as possible and metallic contact are realized at the ends on the thermopiles to allow the characterization (figure 4-14-b). The thermoelectric harvester like any generator can be modeled as the series association of a voltage source (here function of the temperature difference across the thermopiles) and the thermopiles internal resistance or impedance (figure 4-14-c).

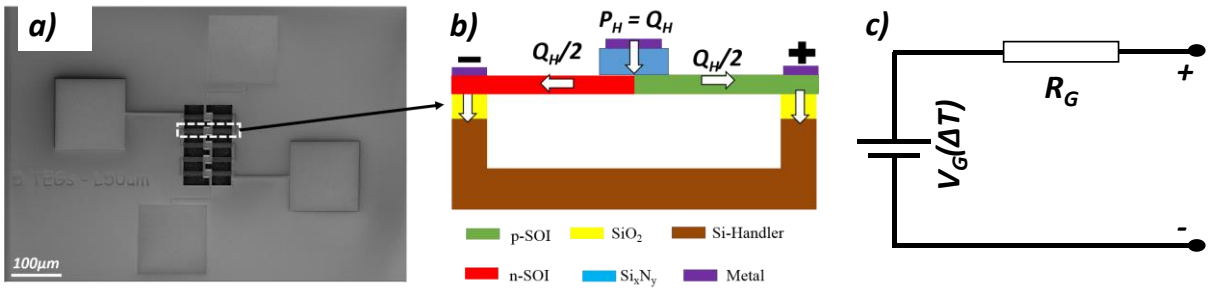

Figure 4- 14: SEM view of a 5-thermopiles demonstrator (a). Cross-sectional side view of a thermopile along the silicon membranes (b) Pt Straps non visible on the cross-section view. The equivalent electrical model of an ideal thermoelectric harvester (c)

During the thesis, several batches were realized, aiming mainly to correct and improve the realization process. Only three of them resulted in devices sufficiently achieved for characterization, the last one being the most successful and the two first being batches with some process improvement to be done. So, in the following are presented first the last realized demonstrators' performance and then the others (first realized) demonstrators' performance and that needed process improvement.

4.3.1 Characterization methodologies

The thermoelectric harvester demonstrators' characterizations are performed under in the apparatus presented in figure 4-6, with the help of the HP/Agilent 4155C and in three phases:

- the Pt heaters calibration like earlier
- The output voltage measurement of the devices under temperature gradient (the Seebeck measurement)
- The demonstrators' current-voltage characterizations of the devices under temperature gradient

4.3.1.1 Pt heaters calibration

The hot sources calibration consists as previously to extract the Pt TCR. The devices being realized on the same wafers and the Pt deposition at the same time, the demonstrators' Pt TCR must be equal or at least close (measurement errors) to the previous obtained TCR. The measurement protocol is the same as previously: the chuck's temperature varies from ambient (23°C) to about 70°C, while a constant voltage (100mV) is applied to the heaters (cf. figure 4-15-left) to sense the effect of the temperature variation on the Pt electrical resistance. Four-probe measurement is not performed, since the heaters are in series and the design is made such a way to make the heaters more resistive than the interconnections. Only the **SMUs** are used at this step and the same **SMUs** used for the voltage bias are used to measure the electrical current and then calculate the electrical resistance. Figure 4-16-right reports the five heaters' (of the considered demonstrator) electrical resistance variation with the chuck's temperature. The electrical resistances increases linearly with the chuck's temperature as expected. As previously, from equation 4-5, the TCR is determined to be of about $\mathbf{2.56.10^{-3}}\ \boldsymbol{K^{-1}}$.

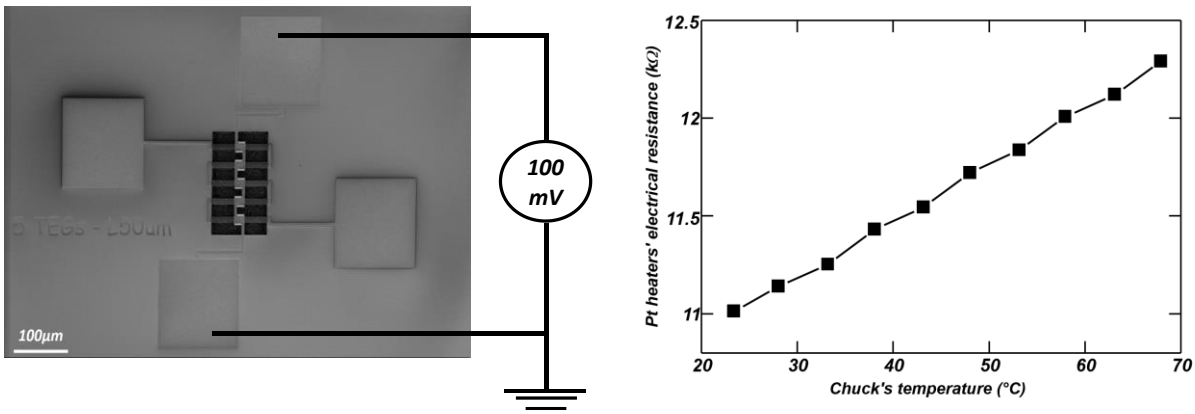

Figure 4- 15: Left: the Pt heaters calibration protocol on a 5-thermopiles demonstrator. Right: the 5-thermopiles demonstrators' Pt heaters' electrical resistances variation with the chuck's temperature

The chuck's temperature is constant (25°C), while the heaters' bias voltage varies to produce several heating temperatures. Since they are strongly coupled to the substrate, the temperature at both ends of the thermopiles is assumed constant and equal to the chuck's temperature. The temperature difference through the demonstrators is then equal to the Pt heaters' temperature elevation due to the bias voltage, calculated thanks to equation 4-5 and the

TCR determined earlier. The next measurements aims to characterize the demonstrators' ability to produce electricity when heated.

4.3.1.2 Seebeck measurement

The first characterization step concerns the measurement of the voltage produced by the demonstrators under thermal gradient. This voltage corresponds to the demonstrators' open-loop voltage. Therefore, the measurements are performed as presented in figure 4-16-letf. While the Pt heaters are biased with a variable voltage ($V_{H\text{-}bias}$), a voltmeter (ΔV) is connected to the thermopiles to sense the voltage ($V_G(\Delta T)$) produced by the temperature difference (ΔT) across the thermopiles. Figure 4-16-right presents the electrical equivalent circuit. The open-loop measurements is mimicked by using a **SMU** "null" current source for the voltage measurement. The voltage is then measured at this high impedance's terminals through a voltage dividing measurement, equivalent to measure the harvester's source voltage. The measured voltage should increase linearly with the temperature (cf. chapter I).

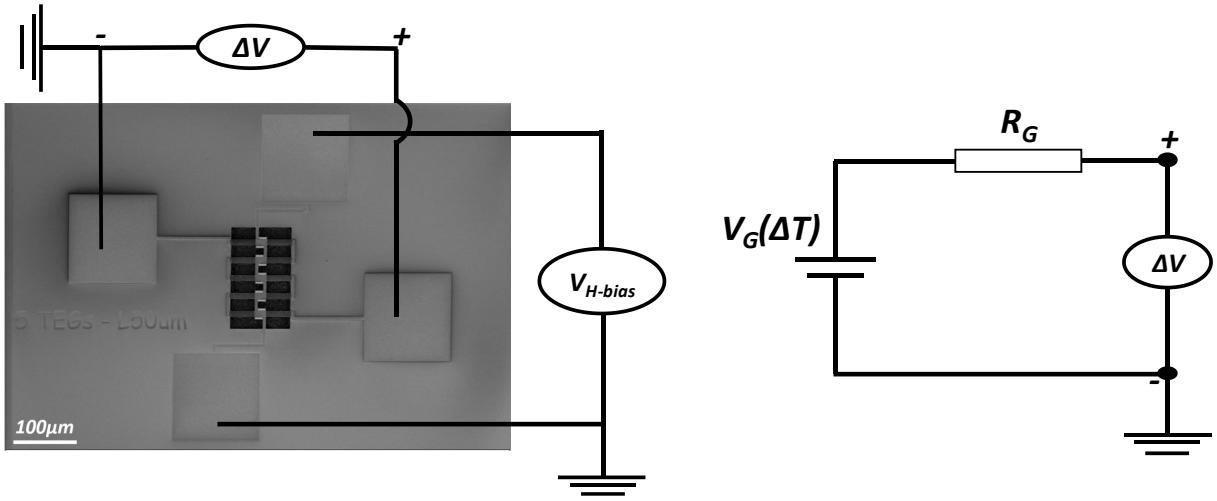

Figure 4- 16: Thermoelectric voltage measurement protocol. Left: the measurement protocol and right: the equivalent electrical circuit

4.3.1.3 Demonstrators' Current-Voltage curves

In addition to the open-circuit voltage measurement, the ability of a thermoelectric harvester to produce electrical power is characterized by its current-voltage with the temperature difference across the thermopiles. Indeed, when the harvester produces electrical power, a shift of the open-circuit voltage and short-circuit current is observed with the increase of the temperature difference across the thermopiles as presented in figure 4-17. Moreover, to qualify the device as a generator, the current-voltage product must be negative. The produced electrical power corresponds to the surface formed by the open-circuit voltage, the short-circuit current. The profile presented in figure 4-17 is based on an ideal (pure resistive) thermoelectric harvester, the principle remains the same if the thermopiles are not purely resistive, only the I(V) curves profile changes.

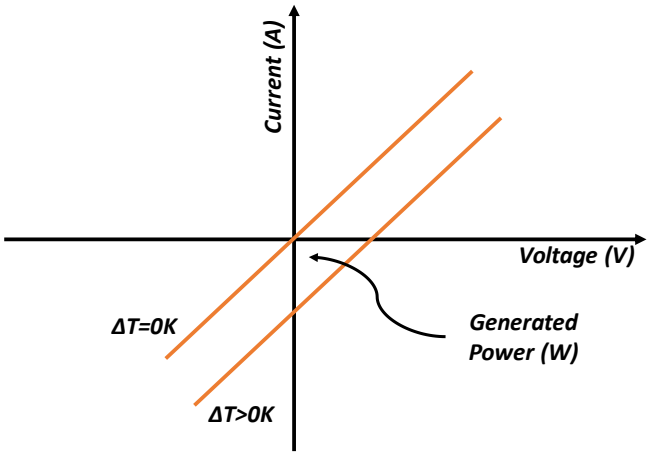

Figure 4- 17: Current-voltage profile of an ideal thermoelectric harvester.

The measurements consist then to apply a voltage sweep to the thermopiles for each Pt heaters' bias voltage (cf. figure 4-18-left). The equivalent electrical circuit (example of an ideal harvester) is presented in figure 4-18-right. From the equivalent circuit, the electrical current through the thermopiles can be expressed with respect to the open-circuit voltage and the thermopiles' sweeping voltage as:

$$I = \frac{V_{G\,bias} - V_G(\Delta T)}{R_G} \qquad \textit{Equation 4- 7}$$

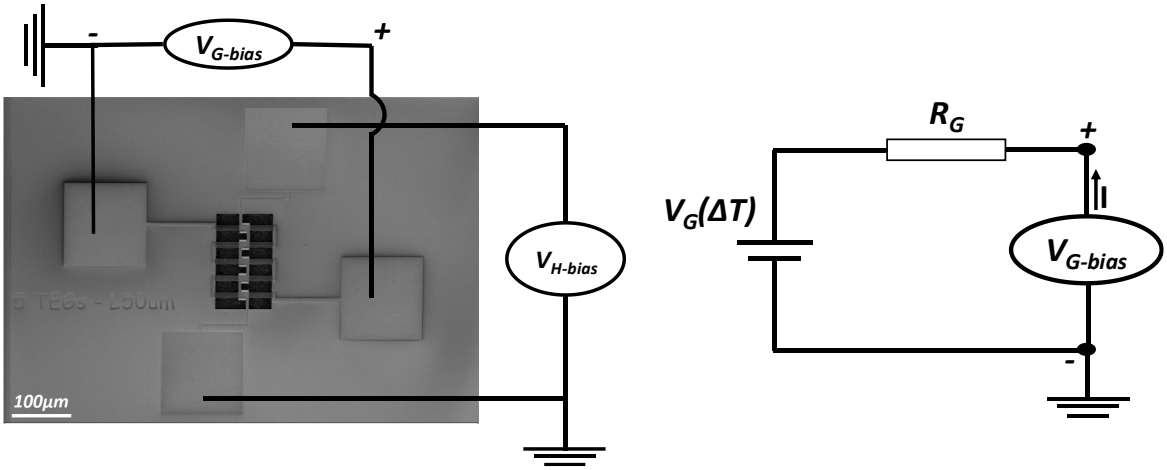

Figure 4- 18: Demonstrators' current-voltage characterization protocol. Left: the measurement protocol and right: the equivalent electrical circuit

4.3.2 Last realized demonstrators' characterizations

The demonstrators presented hereafter are the last realized demonstrators during this thesis. For these demonstrators, the **silicon oxide layer is not removed** before measurement and a metal deposition over silicon nitride layer between thermopiles ensures the thermopiles' electrical continuity.

First, the Pt heaters' calibrations are done, before measuring the dropout voltage due to the Pt heating and the current-voltage characterization according to the temperature difference across the thermopiles. The results presented hereafter are from sample with the silicon membranes embedded in SiO_2 (cf. figure 4-19-right). During the measurements the samples are heated at a constant temperature (25°C) and **without any contrary mention, measurements are performed under vacuum**.

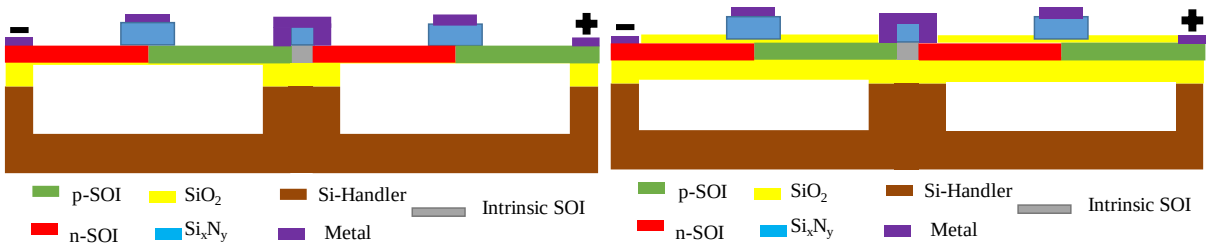

Figure 4- 19: Cross-sectional view of 2 thermopiles demonstrator without (left) and with (right) silicon membranes embedded in silicon oxide layer

4.3.2.1 Demonstrators hot sources calibration

The hot sources being emulated by Joule effect through Pt resistive heaters, it is necessary before any thermoelectric performance characterization to calibrate those Pt heaters. To that sake, a voltage sweep is applied to the Pt heaters and the electrical resistance variation with the sweeping voltage is recorded (figure 4-20-left). The electrical resistance increases quadratically with the heating voltage. From this increase, the Pt serpentines' temperature elevation is calculated thanks to equation 4-5 and the TCR obtained in figure 4-16. Since, the sample is heated at a constant temperature during all the measurements. The temperature difference across the thermopiles is the Pt serpentines' temperature elevation and is presented in figure 4-20-right. We can observe that for a given amount of heat power, the phonon engineered (PE) thermopiles offers a higher temperature difference across the thermopiles and then a better thermal gradient management through the thermopiles as expected.

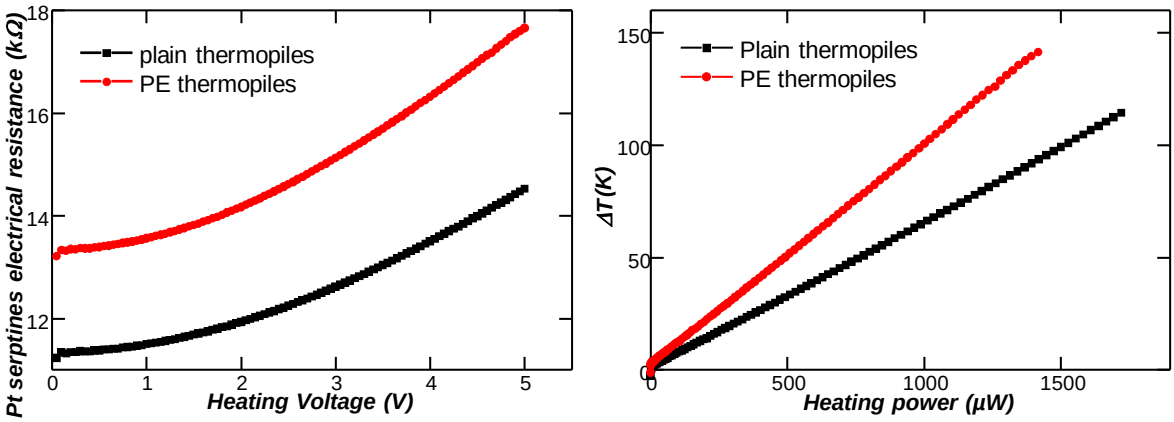

Figure 4- 20: 5 thermopiles' Pt serpentines electrical resistances variation with the heating voltage (left) and the temperature difference across the same TEG according to the heating power (right) (black: plain thermopiles and red: PE thermopiles)

To confirm the Pt serpentines' heating, infrared (IR) imaging is performed. This is done in ambient environment; samples are heated up to a constant temperature (70°C) during the imaging. A constant voltage biases the Pt heaters during all the IR acquisition (figure 4-21-right). The imaging shows indeed a heating of the Pt serpentines when a voltage is applied at their limits. The thermal gradient through the silicon membranes cannot be observed by the IR imaging, because, silicon is transparent to IR waves. However, a temperature difference between the center and the ends of the thermopiles is noticeable.

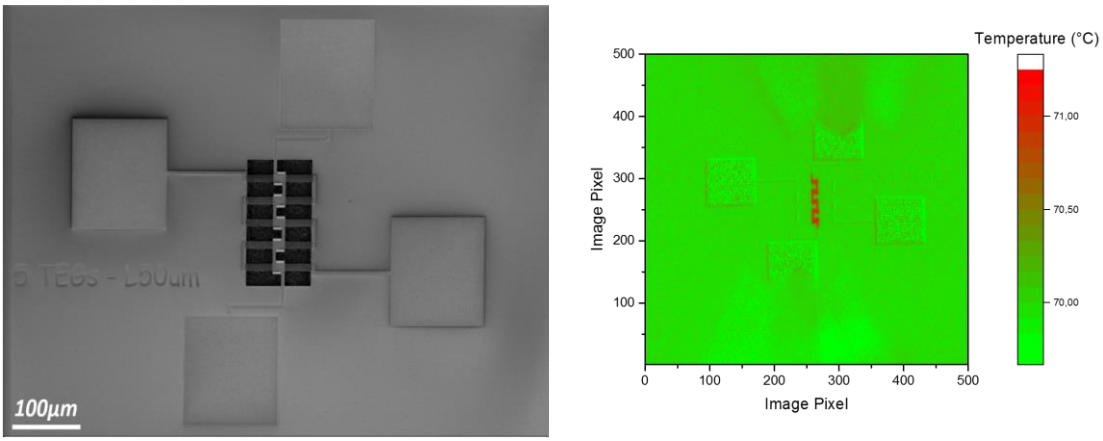

Figure 4- 21: 5 thermopiles demonstrator SEM view (left) and IR imaging after Pt heaters Voltage bias (right)

4.3.2.2 Seebeck coefficient measurements

As explained in the characterization methodologies section (III-1), the first thermoelectric performance of interest is the voltage generated in the thermopiles by the temperature difference across them. The measurement is performed as detailed in figure 4-16 and figure 4-22 reports the output voltage according to the temperature difference across thermopiles obtained from five plain (left) and PE (right) thermopile demonstrators. The output voltage increases "quasi" linearly with the temperature difference and we report respectively **570µV/K, 590µV/K** for the two plain thermopiles and **822µV/K, 840µV/K** for the two PE thermopiles as Seebeck coefficient per thermopile. The Seebeck coefficient seems then to increase with the phonon engineering making the phonon engineering even more interesting for thermoelectric applications. Like the electrical conductivity decrease, the carriers' density of states modification could also explain the modification of the Seebeck coefficient with the phonon engineering. Moreover, a carriers' density of states reduction could explain both the electrical conductivity decrease and Seebeck coefficient increase with the phonon engineering.

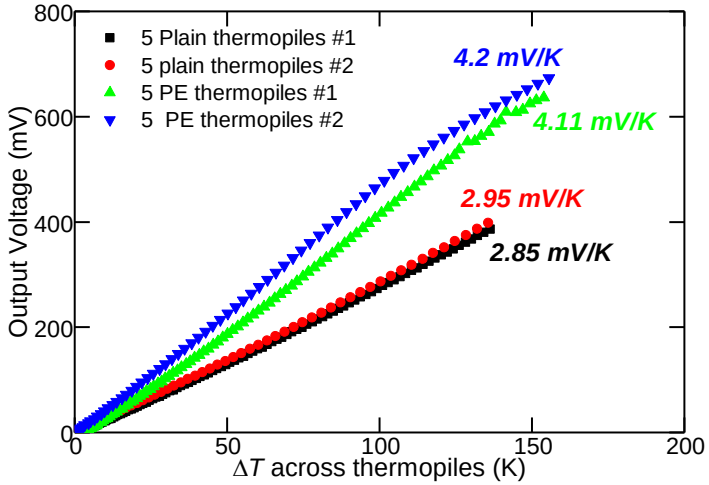

Figure 4- 22: 5 plain thermopiles (black squares & red dots) and 5 PE thermopiles (green & blue triangles) output voltage with respect to the temperature difference across thermopiles

The main drawback of the demonstrators design is the hot sources' mimic by Joule effect through the Pt heaters. Indeed, during the measurements, the electrical current drove in the Pt heaters can leak in the thermopiles and then distort the measurements. Silicon oxide and nitride layers are deposited between the thermopiles and the heaters to make sure that there is no current leakage in the thermopiles (or at least minimize it as much as possible). However, depending on the applied voltage and the number of heaters on the device, current (I) can leak

through the SiO_2 and SiN layers in the thermopiles. When this occurs the measured voltage (V_{out}) is then equal to:

$$V_{out} = V_G(\Delta T) - R_G \cdot I \qquad \textit{Equation 4- 8}$$

So depending on the leakage current direction, the output voltage can be over-estimated or underestimated with respect to the thermoelectric voltage ($V_G(\Delta T)$). So, it is necessary to check the current continuity and conservation in both heaters and thermopiles channels. Figure 4-23 reports the current conservation in both five plain (left) and PE (right) thermopiles' Pt serpentines heaters. There is then, no current leakage from the Pt serpentines' heaters in the thermopiles, the measured output voltage can be considered resulting from the temperature difference induced by the Pt heaters' voltage biasing.

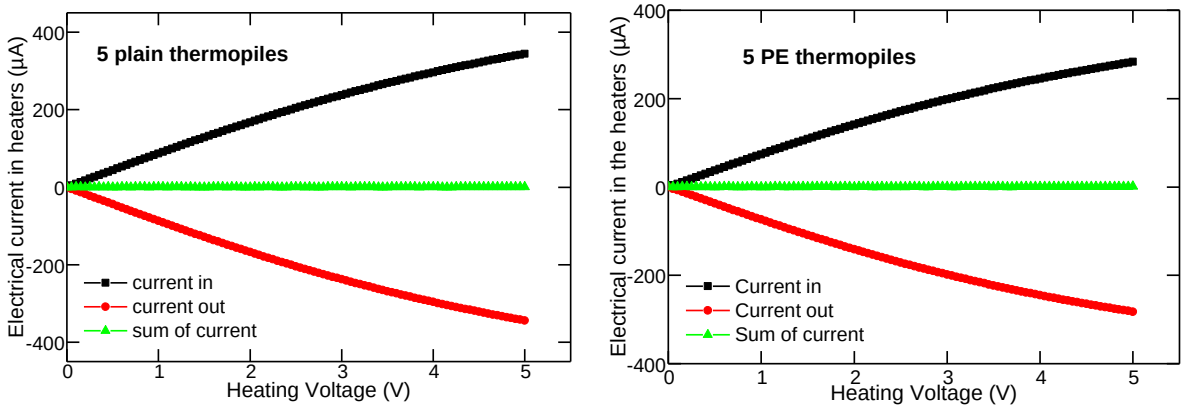

Figure 4- 23: Electrical current in the Pt heaters conservation in 5 plain (left) and 5 PE (right) thermopiles

A focus on the current conservation in the Pt heaters is presented in figure 4-24 according to the heating voltage (left) and the temperature difference across the thermopiles (right). It confirms and highlights the observation made in figure 4-23, namely that the measured output voltage is mostly being from the temperature difference induced by the Pt heaters' voltage bias than from leakage current in the thermopiles. However, figure 4-24 depicts over 4V and 120K more leakage current for the PE thermopiles than the plain thermopiles, what can explain the difference of shape of the output voltage curves (figure 4-22).

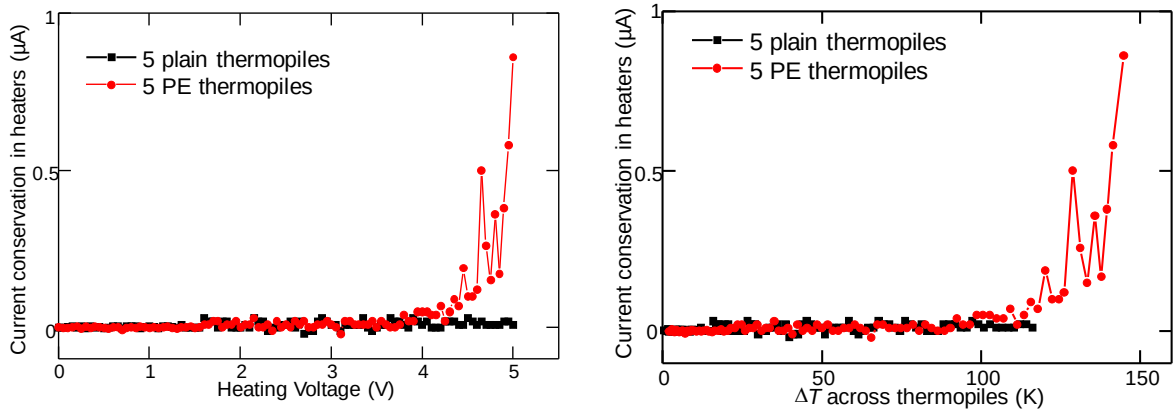

Figure 4- 24: Close-up view on the current conservation in Pt heaters (green curve in figure 4-23) according to the heating voltage (left) and to the temperature difference across the thermopiles (right) for 5 thermopile devices

4.3.2.3 Current-Voltage curves

After the thermoelectric voltage measurement, the second part of the characterization consists in the study of the thermopiles' behavior with the temperature difference across the thermopiles. This second part aims, first, to determine the generator's internal electrical

resistance. Second to demonstrate the electrical power generation according to the temperature difference across the thermopiles and quantifies that generated power. The characterization is performed according to the methodology presented in figure 4-18 and explained in the paragraph above figure 4-18. The characterizations are done first for the plain thermopiles and then repeated to the PE thermopiles

- ***5 Plain thermopiles***

Figure 4-25 reports the current-voltage profile of two "5-plain" thermopiles when no voltage is applied to the platinum heaters (under no temperature gradient). It is noticeable that the current across thermopiles is linked to the voltage through a linear relation, confirming that the *pn* junctions are well short-circuited. The current is equal to:

$$I = \frac{V_{G\,bias}}{R_G} \qquad \textit{Equation 4- 9}$$

V_{Gbias} and R_G being respectively the applied (bias) voltage to the thermopiles and the thermopiles' internal electrical resistance. The 5-plain thermopiles electrical resistances are respectively for the "demonstrator 1": $\mathbf{115\ k\Omega}$ and $\mathbf{156\ k\Omega}$ for the "demonstrator 2". Knowing that the *p* and *n* doped layers electrical resistivity being respectively $\mathbf{2.341 \cdot 10^{-2}\ \Omega cm}$ and $\mathbf{6.377 \cdot 10^{-3}\ \Omega cm}$ and a thermopile being 2x50µm long, 10µm wide and 60nm thick, the theoretical electrical resistance for a "5 plain" thermopiles is about $\mathbf{125\ k\Omega}$. The measured electrical resistances rely with the theoretical electrical resistance within **8%** for the "demonstrator1" and **25%** for the "demonstrator2". The measurements' accuracy and the metal/Si contacts, not taken in account for the theory, can explain these shifts between theory and measurements

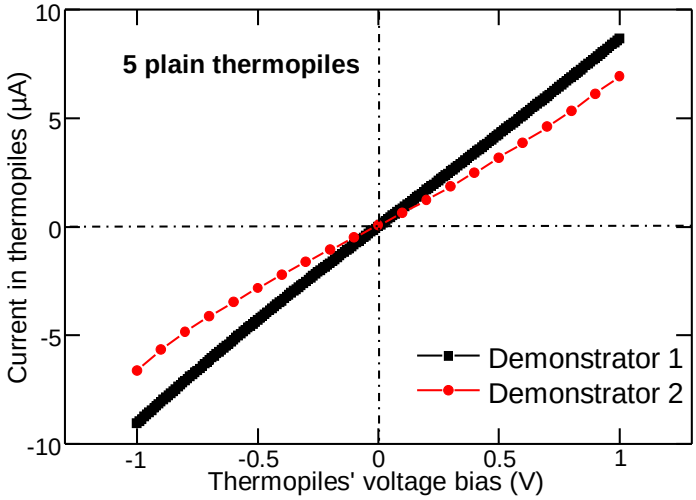

Figure 4- 25: 5 plain thermopiles current-voltage profile when no temperature difference applied to thermopiles

The thermopiles' "ohmic" behavior and the electrical resistances defined, we now focus on the current-voltage behavior with the temperature difference across the thermopiles. Figure 4-26 presents the current-voltage profiles of a "5 plain" thermopiles demonstrator. The figure reports the increase of the open-loop voltage and the short-circuit current, characteristic of a Seebeck effect. Moreover, the negative $I \times V$ product is consistent with a generator regime. Finally, the open-loop voltages correspond to the thermoelectric voltages measured earlier. The current-voltage relation is given by the equation 4-7. It has been already demonstrated that there is no current leak from the Pt heaters to the thermopiles, so the measured current here corresponds well to the thermoelectric generated current.

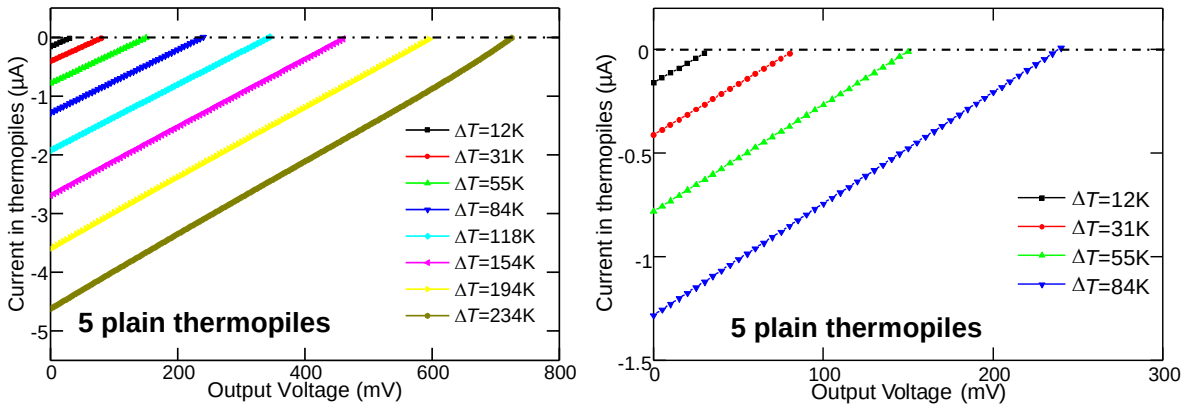

Figure 4- 26: 5 plain thermopiles current-voltage profile according to the temperature difference across the thermopiles. Right: close-up view on small ΔTs

The demonstrator's current-voltage profile with the temperature difference across the thermopiles being consistent with that of a generator, it is now indispensable to quantify the generated power. To that sake, we consider the current-voltage profiles in the generator regime area and multiply that current with the output voltage (V_{Gbias} in the generator regime area). The equation 4-7 becomes then:

$$I \times V = \frac{V_{G\,bias}^2 - V_G(\Delta T) * V_{Gbias}}{R_G} \qquad \textit{Equation 4- 10}$$

The output power is then a quadratic function of the output voltage, null when the output voltage is null or equal to the thermoelectric voltage at the given temperature difference and maximum when the output voltage is equal to the half of the thermoelectric voltage. Figure 4-27 reports the output voltage per generator footprint ($180\mu m \times 120\mu m$) with respect to the output voltage and the temperature difference across the thermopiles. It is noticeable that such demonstrator is able to produce few µW (12K) to mW (234K) per square cm of generator. Such powers are in the range of the energy needed to power supply autonomous senor nodes [Vullers et al. 2009].

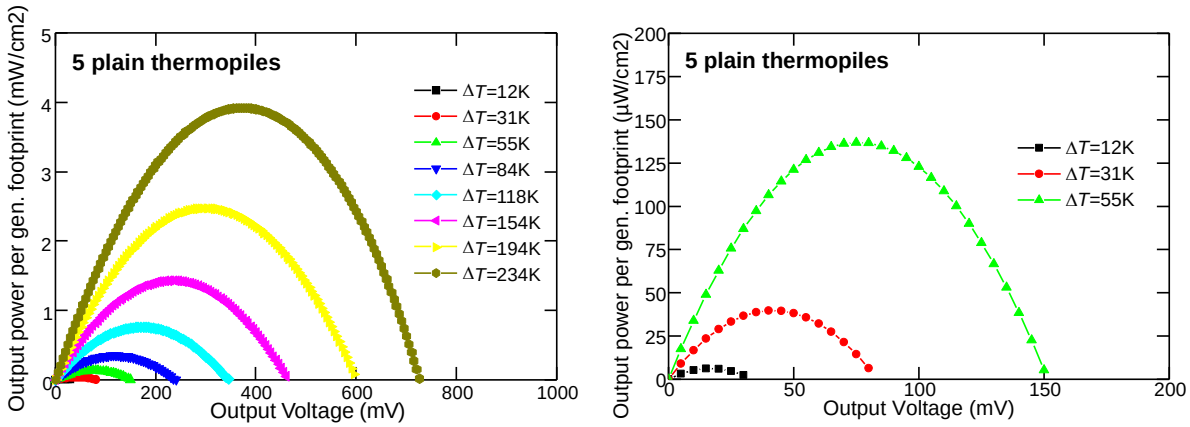

Figure 4- 27: 5 plain thermopiles' output power per generator footprint with respect to the generated voltage and the temperature difference across the thermopiles. Right: close-up view on small ΔTs

- ***5 PE thermopiles***

Let us now focus on the energy production with PE thermopiles. The characterization is performed on demonstrators containing also five thermopiles in order to allow the best and accurate comparison with the plain thermopiles demonstrators. The characterization methodology and steps are the same as for the plain thermopiles. Figure 4-28 presents the

current-voltage profiles of two "5 PE" thermopile demonstrators when no voltage is applied (bias) to Pt heaters, then under no thermal gradient across the thermopiles. The left figure presents measurements done under vacuum and right those done in ambient environment (with conducto-convection in air). Figure 4-28 reports as for the plain thermopile demonstrators that the electrical current varies linearly with the voltage, confirming the well short-circuiting of the *pn* junctions. However, the measurements under vacuum depict a slope change over 0.5V, which can be explained by a possible Peltier or Joule effect or both. Moreover, the measurements performed in ambient environment (with conducto-convection in air) does not show this slope change, confirming heat generation or absorption over 0.5V under vacuum. The 5 PE thermopiles exhibit as electrical resistances respectively under vacuum: $\mathbf{262k\Omega}$ for the "demonstrator1" and for the "demonstrator2" $\mathbf{295k\Omega}$ and in ambient environment $\mathbf{340k\Omega}$. Those electrical resistances are basically, the double of the plain thermopiles' electrical resistances, confirming the results from the section 4.2.2 (cf. table 4-1 & 4-2)

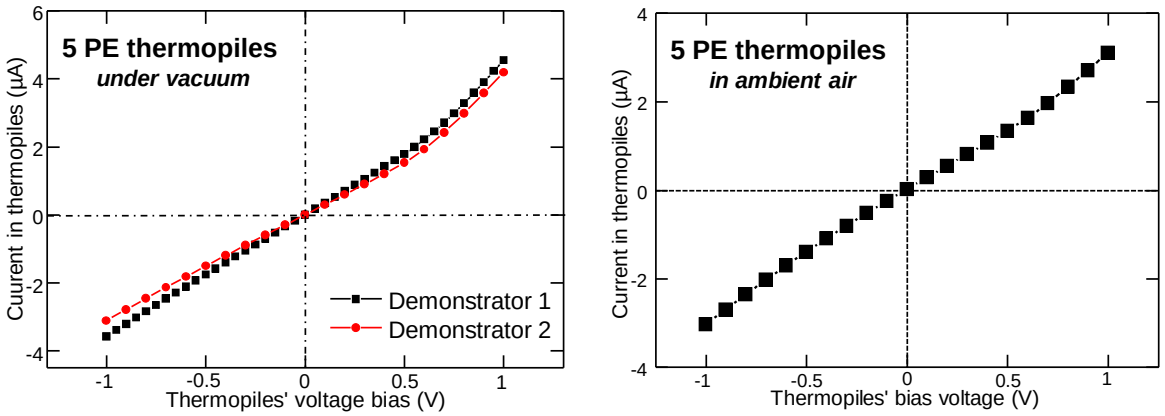

Figure 4- 28: 5 PE thermopiles current-voltage profile when no temperature difference applied to thermopiles. Left: Measurements under vacuum and right: Measurements in ambient environment

Like for the plain thermopiles, the next step is the current-voltage behavior with the temperature difference across the thermopiles. Figure 4-29 consigns that behavior for several temperature differences from 3K to 282K. As previously, the figure reports the open-loop voltage and short-circuit current increase with the temperature and a negative $I \times V$ product confirming a Seebeck effect and power generation. It has also already been demonstrated that there is no current leak from the Pt heaters to the thermopiles, so the current here is only due to the temperature difference across the thermopiles. Moreover, the current-voltage profiles have the same shape than the profile without any temperature difference across the thermopiles, confirming that no additional current is created and that the voltage and current shift is only due to the temperature difference across the thermopiles.

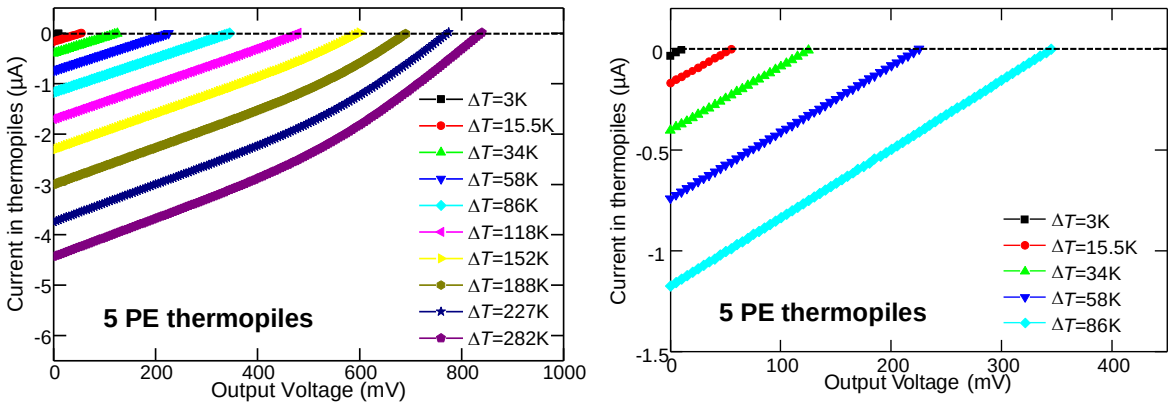

Figure 4- 29: 5 PE thermopiles current-voltage profile according to the temperature difference across the thermopiles. Right: close-up view on small ΔTs

Again, on the same principle as for the plain thermopiles (equation 4-10), the output power per generator footprint according to the generator's output voltage is calculated and presented in figure 4-30. The output power is a quadratic function of the output voltage as expected. In addition, at high temperature differences, the current-voltage slope change is translated by a slight dissymmetry of the quadratic curve. However, the main characteristics remain unchanged: the power is null when the output voltage is null or equal to the open-loop voltage (thermoelectric voltage) and maximum when the output voltage is half of the thermoelectric voltage. The generator exhibits also few µW to mW according to the temperature difference across the thermopiles per square cm in the range for autonomous sensor nodes power supplying [Vullers et al. 2009].

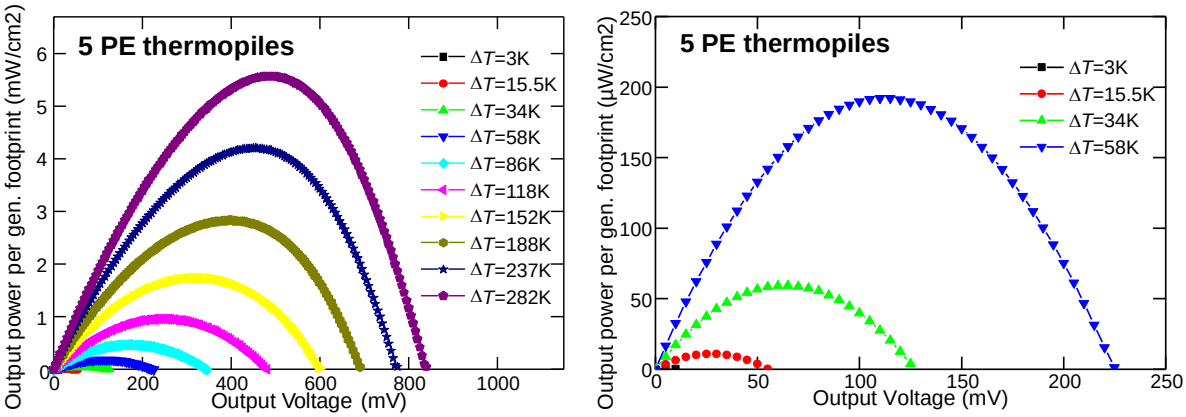

Figure 4- 30: 5 PE thermopiles' output power per generator footprint with respect to the generated voltage and the temperature difference across the thermopiles. Right: close-up view on small ΔTs

4.3.2.4 Phonon engineering TEG performance Vs. Plain TEG performance

Let us sum up the results presented and discussed so far. The phonon engineering (PE) allows:

- A **better thermal gradient management** through the thermopiles thanks to a thermal conductivity reduction by a factor 4.5 (for the best device)
- The silicon membranes' **Seebeck coefficient increases (~830µV/K** per thermopile for PE thermopiles and **~ 580µV/K** per thermopile for plain thermopiles)
- The silicon membranes' **electrical resistance increase by a factor 2** through the reduction of the matter available for electronic transport and electrical resistivity increase.

Finally, integrated into a thermoelectric harvester demonstrator, both PE and plain thermopiles produce comparable power (same order of magnitude). In short, the phonon engineering presents some advantages and drawbacks. Do these advantages overcome the drawbacks? To answer this question, the maximum output power per generators footprint are extracted and compared. First, the comparison is performed according to the temperature difference across the thermopiles (figure 4-31). Figure 4-31 reports comparable performance for the different demonstrators, sometimes a PE demonstrator outperforms a plain demonstrator or vice-versa. This comparison is actually the comparison of the Seebeck coefficient increase to the electrical resistance increase. Indeed, at equal temperature difference (ΔT) across the thermopiles, the maximum output power is only function of the Seebeck coefficient (S) and the electrical resistance (R_G) as presented by equation 4-11. So, the results presented in figure 4-31 depict a compensation of the electrical resistance increase by the Seebeck coefficient increase.

$$P_{MAX} = \frac{V^2}{4 * R_G} = \frac{S^2 * \Delta T^2}{4 * R_G} \qquad \textit{Equation 4- 11}$$

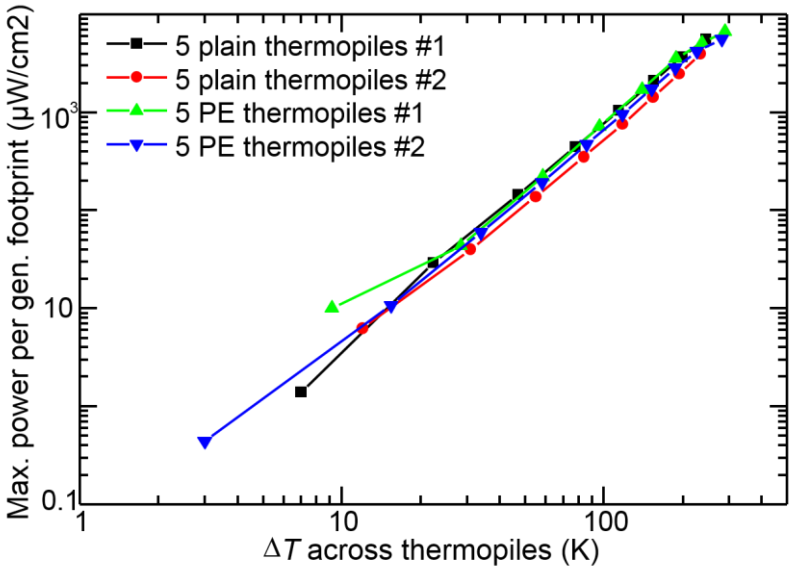

Figure 4- 31: 5 plain and PE thermopiles benchmarking with respect to the temperature difference across the thermopiles

To highlight the main purpose of the phonon engineering, namely its ability to allow a better thermal gradient management through the generator, the comparison is performed this time according to the heating power. That way we study the generators abilities to harvest from the same energy source. In this condition, equation 4-11 becomes:

$$P_{MAX} = \frac{V^2}{4 * R_G} = \frac{S^2 * Q^2 * r_{TEG}^2}{4 * R_G} \qquad \textit{Equation 4- 12}$$
$$\Delta T = Q * r_{TEG}$$

Q and r_{TEG} being respectively the heat power and the generator's thermal resistance. So, in addition to the Seebeck coefficient/electrical resistances, the demonstrators' ability to sustain a thermal gradient are studied. Figure 4-32 reports the maximum output power per generators footprint according to the heating power for several 5 PE and plain thermopile demonstrators. It is clearly noticeable that the PE demonstrators outperforms the plain demonstrators even if

the gain is less than an order of magnitude. The ability to sustain a thermal gradient is then the principle advantage of the phonon engineering of silicon based thermoelectric harvesters' development.

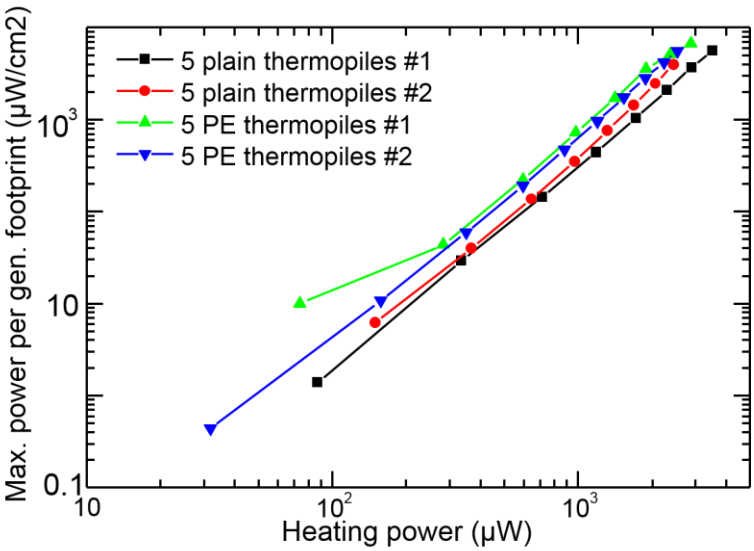

Figure 4- 32: 5 plain and PE thermopiles benchmarking with respect to the heating power

The low gain of power when PE thermopiles are used can be explained by the fact that silicon membranes are embedded into silicon oxide. Indeed, the silicon oxide around silicon membranes can improve the thermal gradient management across silicon membranes. Let us consider the elementary device presented in figure 4-10 with and without silicon oxide around the silicon membranes. Figure 4-33 presents the thermal gradient management across silicon membranes without silicon oxide (left) and with silicon oxide (right). Figure 4-33 shows not only that the silicon oxide allows the increase of membranes thermal resistances [Verdier et al. 2018] but also that it has a bigger impact on the plain silicon membranes than the PE silicon membranes. Therefore, removing the silicon oxide could amplify the power generation gap between PE and plain thermopiles, but also with the optimal silicon oxide thickness around silicon membranes, thicker silicon membranes (lower electrical resistance) based generators could be developed with minor degradation of the thermal gradient management.

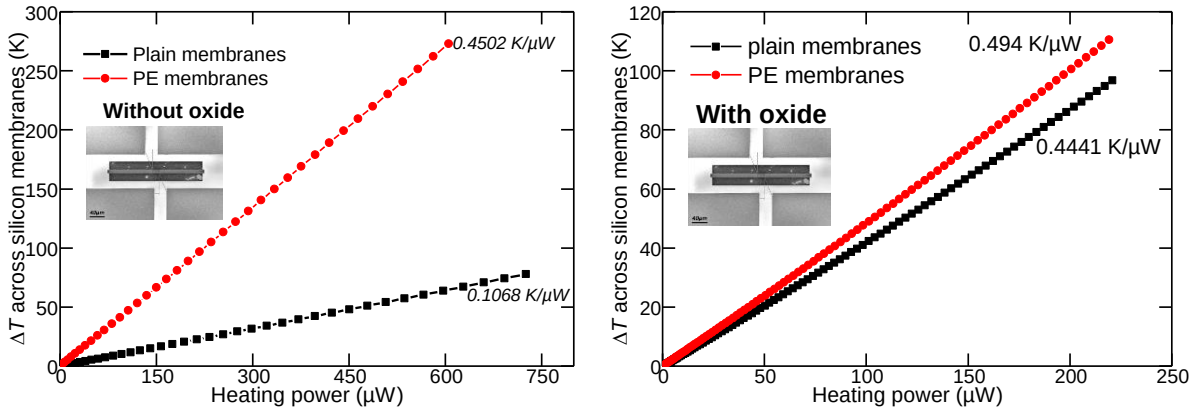

Figure 4- 33: Effect of the silicon oxide on the thermal gradient management across silicon membranes

4.3.3 ***First realized demonstrators***

The demonstrators presented in this section are the first realized demonstrators, the demonstrators used to develop and improve the realization process. For these demonstrators, the realization process was performed until the end (the silicon oxide was systematically

removed). The process improvement concerned mainly the electrical continuity between thermopiles. So two batches were realized (one for each thermopiles' electrical continuity methodology) and presented hereafter.

4.3.3.1 First batch

In the first batch, the demonstrators were made such a way that the continuity between two thermopiles were realized through the intrinsic silicon layer (cf. figure 3-31-left). The demonstrators from this batch exhibit current-voltage profiles similar to profiles with bad contacts between metal and semiconductor and like current propagation through lightly doped silicon (cf. figure 4-34), raising the hypothesis of an eventual current leakage through the intrinsic SOI.

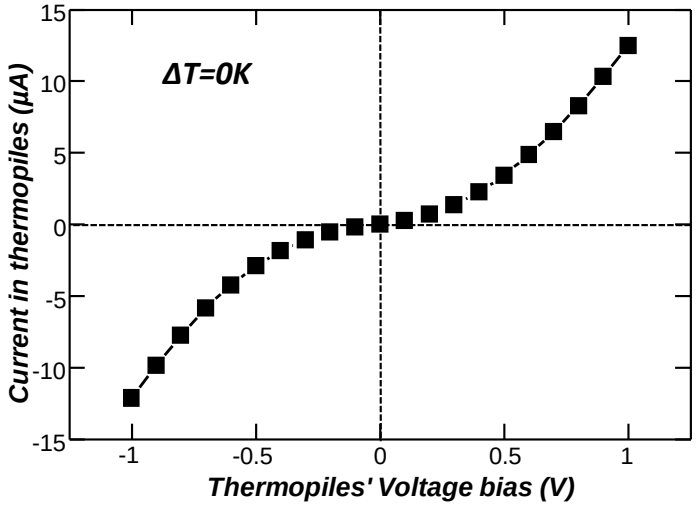

Figure 4- 34: First batch's 50 PE thermopiles current-voltage profiles @ ΔT=0K

However, an open-loop voltage and short-circuit current increase is observed with the temperature difference and the profiles keep the same shapes (cf. figure 4-35 left). The output power per demonstrator footprint is also evaluated (figure 4-35-right). The realized demonstrator exhibits quite high performance (**~2mW/cm^2 @ Δ*T*=46K**) compared to the performance of the last realized demonstrators (**barely hundredth of µW/cm^2 for same Δ*T***), difficult to explain, mainly because of the current-voltage profiles.

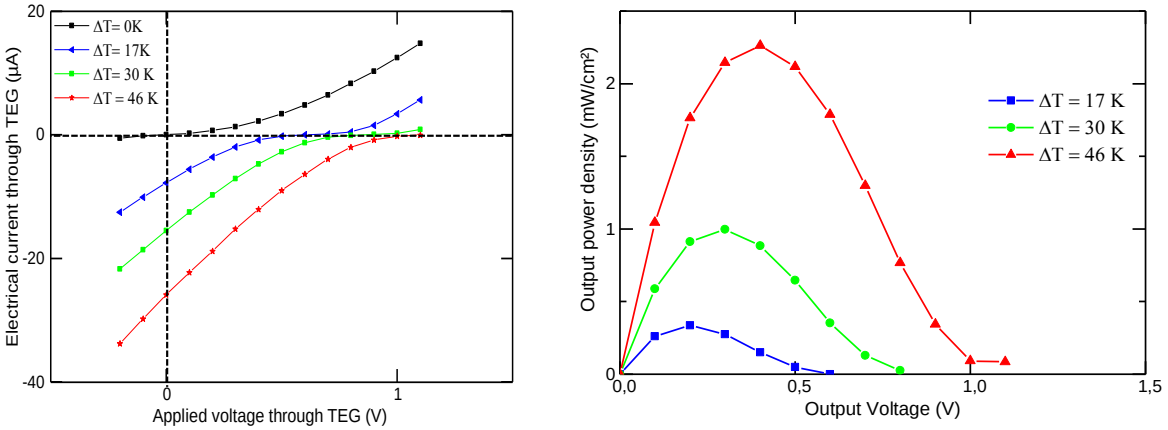

Figure 4- 35: First batch's 50 PE thermopiles current-voltage profiles (left) and output power per demonstrator's footprint according to the temperature difference across thermopiles

4.3.3.2 Second batch

To verify the hypothesis of current leak through the intrinsic SOI, the demonstrators are for this second batch, realized such a way to perform the thermopiles' electrical continuity over a silicon nitride layer (cf. figure 3-31-right). Except the thermopiles' electrical continuity step, the other steps are kept unchanged for a better comparison of the batches. The silicon membranes are then completely suspended (**no oxide left**). After the silicon membranes suspension, the thermopiles present diode like current-voltage profiles (cf. figure 4-36-left), while before suspension the profiles are more close to ohmic profile (figure 4-36-right). The current-voltage profiles have no longer the shapes presented earlier, confirming the possibility of current leak through intrinsic SOI.

However, the current-voltage curve becoming diode like while before suspension it is more close to an ohmic profile, suggest the platinum straps on the *pn* junctions embrittlement. Unfortunately at this step, no measurement was performed before each suspension step (Si substrate etch and oxide removal (cf. section 3.2.6), making impossible to determine when do the Pt straps embrittlement occur. To address this new issue, decision is made to perform characterizations before the oxide removal, explaining why the last realized demonstrators were characterized without the silicon oxide removal. The demonstrators behaving like diodes, it is difficult to produce any energy, **no energy production** was then recorded with these demonstrators.

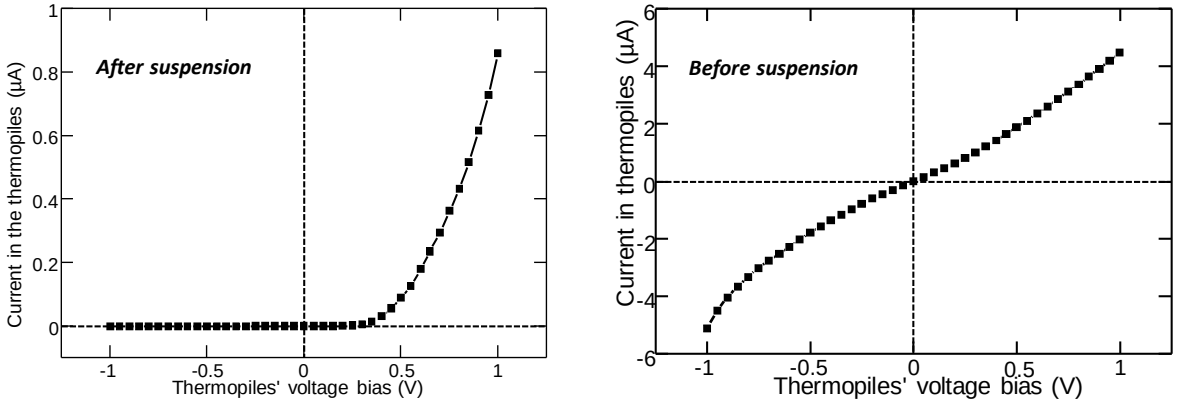

Figure 4- 36: second batch demonstrators' current-voltage profile after (left) and before (right) silicon membranes suspension

4.3.4 Measurements vs. Finite Element Model

In the second chapter, we dealt with the theoretical study of a planar silicon based thermoelectric harvester. It is interesting to compare that study with the measurements performed on the different demonstrators realized during this thesis. Figure 4-37 reports the measured maximum output power density comparison with the results obtained from the finite element modeling. The comparison shows that the measurements basically, matches pretty well with the FEM, except measurements performed on the demonstrator from the first batch. The measurements from the first batch do not match with the model because of its current-voltage profile, not characteristic of an "ideal" thermoelectric harvester. In addition, for the other measurements, the slight shift between measurements and model can be explained by the electrical resistance differences and/or the Seebeck coefficient differences.

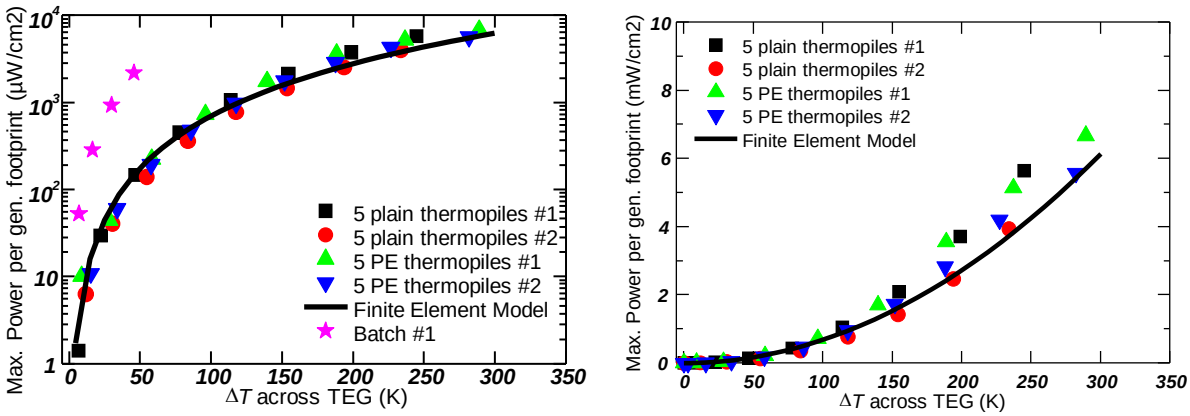

Figure 4- 37: Measured max. Output power compared to FEM according to the temperature difference across the thermopiles. Left: All measurements and right: close-up view on last measurements.

Figure 4-38 presents the measured voltage on five plain and PE thermopiles compared to the output voltage obtained from a finite element modeling of a five silicon based thermopiles according to the temperature difference across the thermopiles. The finite element model is made of plain thermopiles (finite element cannot model the physical effect of the phonon engineering) and the thermoelectric voltage modeled through the Mott-law for the Seebeck coefficient (cf. chapter I).

The measurements on plain thermopiles matches within about **5%** (for the first demonstrator) and **8%** (for the second demonstrator) to the modeling results obtained from the Mott law formula for the Seebeck coefficient. These results validate the Seebeck model used to study the Si thermoelectric harvester in the second chapter. However, the PE thermopiles measurements do not match the model result. This observation was predictable, since the FEM does not allow the modeling of carriers' density of states modification due to the phononic engineering.

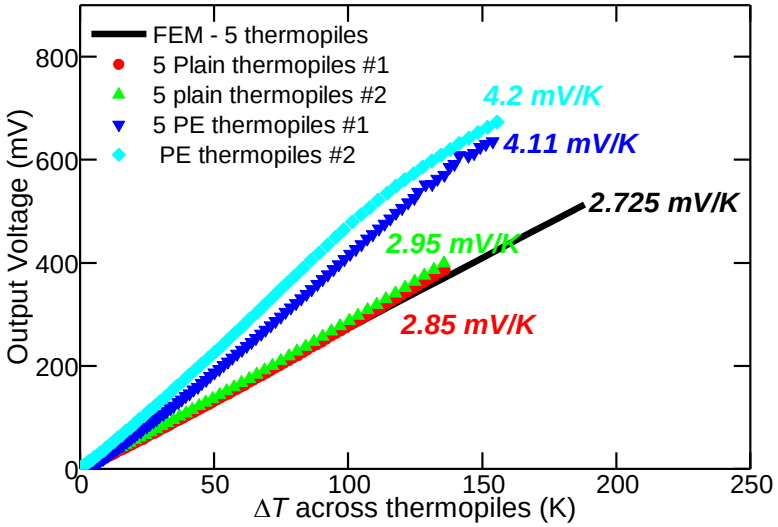

Figure 4- 38: Measured output voltage on 5 plain and PE thermopiles compared to the results from a 5 thermopiles finite-element-model

4.3.5 ***Benchmarking with micro-harvesters state of the art***

The last and most important comparison is made with the state of the art micro-thermoelectric harvesters presented in the first chapter. Indeed, it is interesting to know if the developed devices outperform the existing ones or not and explain why. Figure 4-39 presents

the developed demonstrators' maximum output power densities according to the temperature difference across the thermopiles and with respect to the state of the art micro-harvesters. The state of the art are silicon nanowires based micro-harvesters (*Davila et al.* [Dávila et al. 2011] *Li et al.* [Li et al. 2011] *and Tomita et al.* [Tomita et al. 2018]), planar polysilicon based micro-harvesters (*Ziouche et al.* [Ziouche et al. 2017] and *Xie et al.* [Xie et al. 2010]) and bismuth-telluride based micro-harvester (*Bottner et al.* [Bottner 2005]).

Compared to silicon based thermoelectric micro-harvesters, the developed demonstrators mainly exhibits **better performance** than the state-of-the-art for same temperature differences across the thermopiles. The material crystalline structure and/or the harvesters' architectures can explain this difference of performance. Indeed, a polysilicon and a single crystal do not have the same electrical resistivity. Moreover, the lower dimensions of silicon nanowires can contribute to increase the harvester's electrical resistance. Nevertheless, *Tomita et al.* thanks to the silicon nanowires and the cold end substrate engineering manage to develop Si nanowires (NWs) based harvester exhibiting better performance than the rest of the state of the art.

However, regarding the bismuth telluride based micro-harvester, the developed demonstrators exhibit poor performance compared to the bismuth telluride state of the art. The bismuth telluride micro-harvesters depict performance **four order of magnitude** higher than the developed demonstrators do. Already noted in the chapter 2, this is mainly explained by the gap of electrical resistances: **less than 1Ω** per thermopile for the Bi-Te micro-harvesters against **tenth of kΩ** per thermopile for the developed demonstrators. Indeed, bulk (tenth of µm) Bi-Te exhibiting low thermal conductivity, there is no need to thin the Bi-Te, allowing then the development of harvesters with low electrical resistances in the opposite of our demonstrators. Nevertheless, the modeling works presented in chapter 2 demonstrated that according to the harvesters cooling conditions, the developed demonstrators could **compete and even outperform the Bi-Te micro-harvester state of the art**.

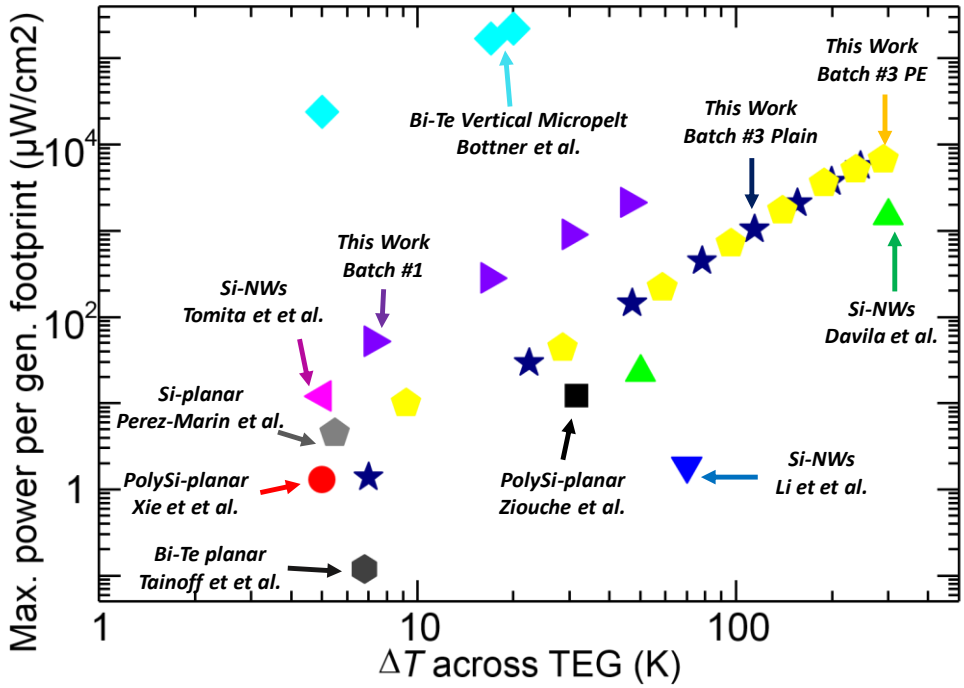

Figure 4- 39: Silicon based thermoelectric harvester demonstrators' performance compared to the state-of-the-art

4.4 Thermoelectric cooling with the same demonstrators?

Developing silicon based thermoelectric coolers is also of interest, since it can allow the integration of coolers into silicon based micro devices for local and efficient cooling. Though the devices were not designed for that sake, we tested the demonstrators in Peltier mode.

4.4.1 Characterizations' principle

The Peltier effect consists in a heat absorption or generation at the thermopiles' junctions due to the thermopiles' biasing. The electrical current direction will define the absorption or generation behavior. For this study, the sample is placed under an IR camera while biasing the thermopiles with a constant voltage as presented in figure 4-40 (first from the *p* end to the *n* end and then from *n* to the *p* end). By doing so, we expect a heat generation at the thermopiles' centers in one electrical current direction and a heat absorption in the other direction. For a better measurement's accuracy, the sample is heated at 75°C during characterization.

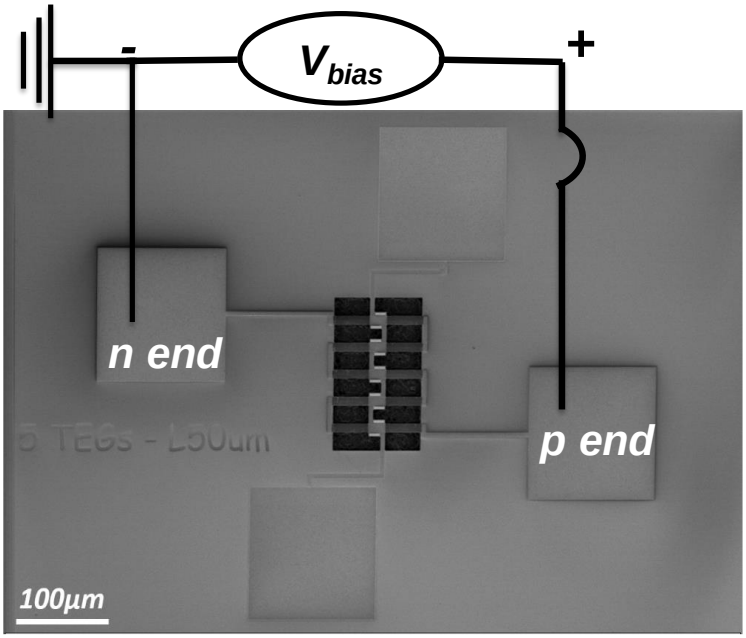

Figure 4- 40: Peltier effect characterizations' principle

4.4.2 Raw IR Imaging

The study is performed on a five plain thermopiles. The thermopiles are voltage biased with 7.5V (almost 95µA and 700µW) according to the scheme presented in figure 4-40 in both current directions (from *p* end to *n* end and from *n* to *p* end). Figure 4-41 presents the raw pictures after biasing the thermopiles with 7.5V for a current flow from *p* to *n* end (left) and from *n* to *p* end (right). From the pictures, we can make two important observations:

- A heat generation at the center of the thermopiles is observed for both current directions. No heat absorption as expected. This first observation can be explained by the Joule effect, indeed, the thermopiles being an assembly of electrical resistances, a current flow across them can generate a heating through the Joule effect.
- The heat generations is more important for a current direction than the other on, leading to conclude that the current flow in the thermopiles generate another effect in addition to the Joule effect. Indeed, the thermopiles being "ohmic" resistances (cf. figure 4-26), for the same voltage bias, the Joule effect must be the same whatever the current direction. The Peltier effect can explain this observation, in fact, we can presume that in addition to the Joule effect, a heat generation/absorption is also present depending on

the current directions, leading to the difference of heating observed in figure 4-41. The pictures should then be processed to get rid of the Joule effect.

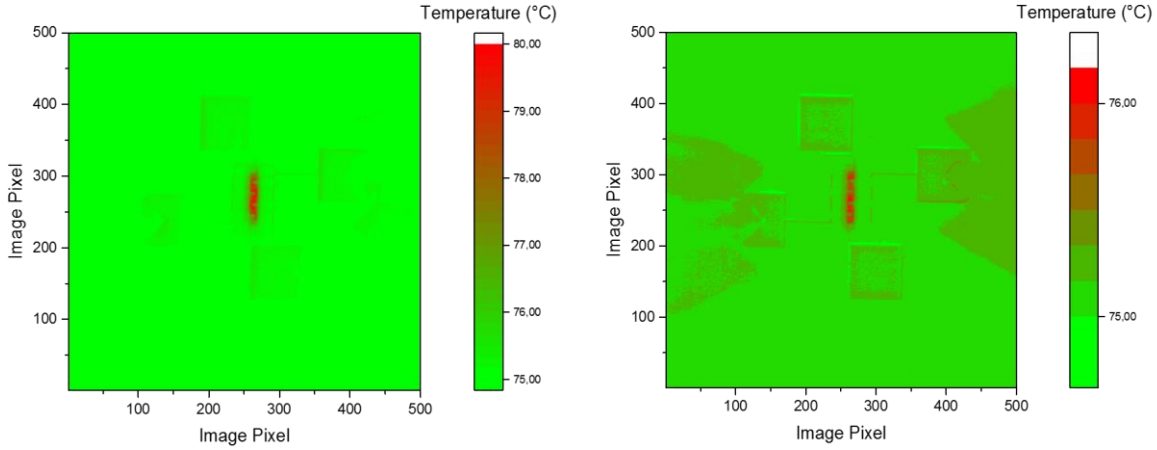

Figure 4- 41: Raw IR pictures on 5 plain thermopiles' biased with 7.5V (~700µW). Left: Electrical current flows from p end to n end and right: electrical current flows though n end to p end.

4.4.3 Peltier effect extraction

The Peltier effect is extracted by processing the pictures such a way to get rid of the Joule effect. First, the hypothesis of the presence of a Peltier effect in addition to the Joule effect implies:

- Left picture (figure 4-41) = Joule effect + Peltier heating
- Right picture (figure 4-41) = Joule effect + Peltier cooling

The Peltier effect are then expressed as:

- Peltier heating = Left picture (figure 4-41) - Joule effect
- Peltier cooling = Right picture (figure 4-41) - Joule effect

The thermopile being biased with the same voltage and especially the same electrical power, it can be assumed that "Peltier heating + Peltier cooling =0", leading to estimate the Joule effect's contribute to (Left picture (figure 4-41) + Right picture (figure 4-41))/2. Figure 4-42 presents the estimated Joule effect's contribution.

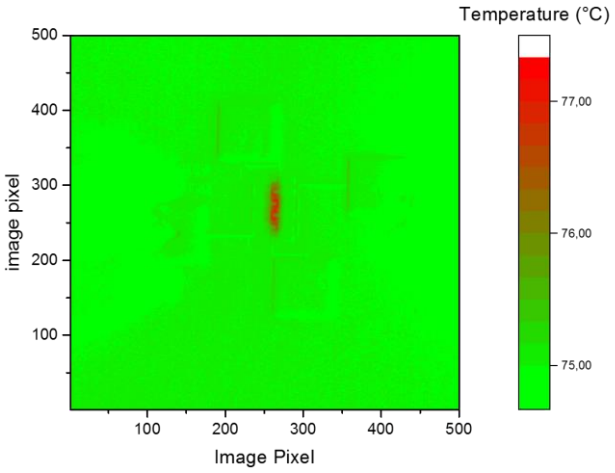

Figure 4- 42: IR image of the estimated Joule effect's contribution

The Joule effect's contribution known, the Peltier effect's contributions are estimated according to the relations presented earlier. Figure 4-43 reports the IR images (Left: current from *p* to *n* end and right: current from *n* to *p* end) free of the Joule effect. The result shows a heat generation when the current flows from the *p* to *n* end and a heat absorption in the current's opposite direction as expected from a Peltier effect. With the developed thermopiles, it is then possible to highlight the Peltier effect and specially to perform thermoelectric cooling. However, the design must be improved in order to dissipate the heat generated by the Joule effect. Indeed, the current design is more dedicated to thermoelectric harvesting by allowing a better thermal gradient management than to thermoelectric cooling. This result is just as important as the thermoelectric harvesting results, in fact, this result can open the way to the integration of thermoelectric cooling in silicon based micro-devices.

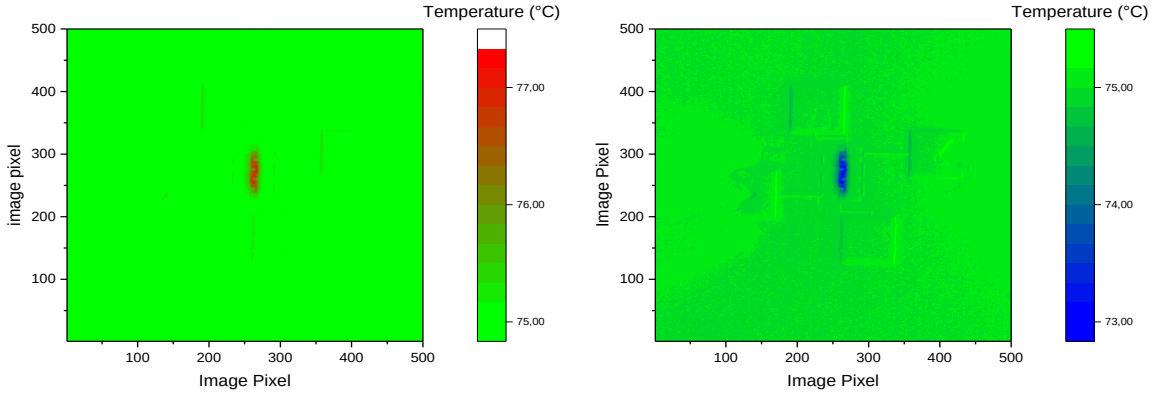

Figure 4- 43: IR images after Joule effect's removal. Left: Electrical current flows from p end to n end and right: electrical current flows though n end to p end.

Conclusion

The **fourth and last part** detailed the characterizations of the different realized devices. Joule effect thanks to Pt resistive serpentine deposited in the center of the thermopiles emulated the hot source on the devices. Therefore, in order to avoid the heat losses in air through the conducto-convection, the thermal measurements were performed under vacuum. The Pt serpentines' electrical resistances exhibited linear variation with the temperature. The heating power was delivered to the silicon membranes through the Joule effect occurring in the Pt heater serpentines. Therefore, it was indispensable before any characterization to accurately calibrate the Pt heaters. Once the heaters calibrated, the devices were characterized. The devices characterizations reported:

- **A better thermal gradient management** through the silicon membranes thanks to the phonon engineering (cf. figure 4-13). This improvement was explained by the increase of the silicon membranes' thermal resistances with the phonon engineering (already demonstrated by previous works [Haras 2016; Lacatena 2016])
- The **increase of the silicon membranes' electrical resistances** with the phonon engineering (cf. section 4.2.2) **by a factor 2**.
- **The increase of the silicon membranes' Seebeck coefficient** thank to the phonon engineering (cf. figure 4-22) **by a factor 1.4**.
- The generation of electrical power with the developed demonstrators, when they were in contact with a heat source (here emulated by Joule effect). The devices generated from **few µW/cm^2** to **few mW/cm^2** according to the temperature difference across the thermopiles and then according to the heating power.

- **Comparable performances for phonon engineering and non-phonon engineered silicon harvester demonstrators for the same temperature difference across the thermopiles** (cf. figure 4-31), reflecting the compensation of the different impacts of the phonon engineering on the silicon membranes thermoelectric properties.
- **Higher thermoelectric performance** for the phonon engineering harvester demonstrators when the study is done according to the heating power (cf. figure 4-32). This result **highlights the importance of the thermal gradient management quality** on the thermoelectric performance.
- **The validation of the FEM studies' results** (cf. figures 4-38 et 4-39), confirming experimentally the conclusions made after the FEM studies, namely, the opportunity of developing low cost mass production thermoelectric harvesters for $\mu W/cm^2$ power consumption autonomous sensor nodes[Vullers et al. 2009].
- **Better performance** of the developed demonstrators compared to the state of the art silicon based micro-harvester at the same temperature. However, when the comparison is done with bismuth telluride micro-harvester as already observed with the FEM studies, the **performance is lower**. Nevertheless, if the thermal gradient would be taken in consideration, the developed demonstrators could exhibit better performances than the bismuth telluride micro-harvester (cf. figure 2-18).
- **The possibility of** using the developed demonstrators for **thermoelectric cooling** applications (cf. figure 4-44). However, as it is, the thermoelectric cooling was masked by a Joule effect due to the silicon membranes' electrical resistances. Therefore, for thermoelectric cooling applications, the thermopiles' design must be improved such a way to allow the Joule effect's heat dissipation.

General Conclusion & Perspectives

This thesis work focused on the study and the development of phonon-engineered silicon based thermoelectric harvester demonstrators, and their study with respect to the state-of-the art of micro-harvesters based on silicon or bismuth telluride alloys.

In the thesis's **first part** presents the problematic of energy harvesting technologies development rose by the indispensable [Nordrum 2016] blooming of wireless sensor networks (WSN) and internet of things (IoT). Then, the thesis detailed the theory behind thermoelectric harvesting and reviewed the different methodologies for the silicon thermoelectric properties improvement thanks to its thermal conductivity reduction. Finally, the first chapter reviewed the microscale thermoelectric harvesters' state of the art, with a focus on the silicon (material of interest for this thesis) and bismuth telluride alloys (best thermoelectric materials) based harvesters.

The second part dealt with the Finite Element Modeling (FEM) of a silicon and a bismuth telluride alloys based thermoelectric harvester. The studied silicon harvester model is made of planar silicon membranes in the framework of the demonstrators that where realized and studied in the thesis. Regarding the bismuth telluride alloys, the harvester model was a state of the art bismuth telluride harvester [Bottner 2005], commercialized by Micropelt[Micropelt GmbH]. The modeling studies realized for two values of silicon thermal conductivity [Haras et al. 2016] (our last published results) [Tang et al. 2010] (the lowest state of the art value) report:

- A better thermal gradient management across the harvester for the silicon based harvester, despite a higher thermal conductivity
- Comparable (and better with silicon) thermoelectric performances when harvesters are naturally cooled without any heat sink.
- The bismuth telluride harvester remains the more efficient when they are cooled with high capacity heat sink.

The modeling studies highlighted that, by combining the two leverages of nanostructuration in order to reduce the thermal conductivity with an innovative in-plane TEG design, there was an improved use of the thermal gradient. Therefore, this lead to a maximized harvested energy even in the absence of bulky heat sinks, which is an advantage in the perspective of miniature energy harvesters. These results open perspectives in the field of autonomous sensor nodes of typical tenth of µW consumption with cm^2-sized harvesters, based on Si material and compatible with mass production facilities of semiconductor manufacturers.

The **third part** tackled the silicon harvester demonstrators design (according to the modeling results) and realization. The demonstrators were realized with and without phonon engineering in order to allow the study of the phonon engineering impact on the thermoelectric performances. Moreover, as complement to the demonstrators, three other devices were realized on the same wafer. These devices aimed to allow the study of the phonon engineering on the silicon thermoelectric properties (Seebeck coefficient, thermal conductivity and electrical conductivity). The devices where realized from a SOI wafer according to a CMOS compatible process whose main steps were:

- The SOI wafer's top layer patterning by means of e-beam lithography and Cl_2/Ar Reactive-Ion-Etching (RIE)
- SOI electrical properties modification by mean of ion implantations
- Materials deposition on that top layer by means of Low-Pressure-Chemical-Vapor-Deposition (LPCVD) and e-beam evaporation.

• Thermal insulation of the top layer from the others layer of the SOI by XeF2 and HF vapor etching.

The **fourth and last part** detailed the characterizations of the different realized devices. Joule effect thanks to Pt resistive serpentine deposited in the center of the thermopiles emulated the hot source on the devices. Therefore, in order to avoid the heat losses in air through the conducto-convection, the thermal measurements were performed under vacuum. The Pt serpentines' electrical resistances exhibited linear variation with the temperature. The heating power was delivered to the silicon membranes through the Joule effect occurring in the Pt heater serpentines. Therefore, it was indispensable before any characterization to accurately calibrate the Pt heaters. Once the heaters calibrated, the devices were characterized. The devices characterizations reported:

- **A better thermal gradient management** through the silicon membranes thanks to the phonon engineering (cf. figure 4-13). This improvement was explained by the increase of the silicon membranes' thermal resistances with the phonon engineering (already demonstrated by previous works [Haras 2016; Lacatena 2016])
- The **increase of the silicon membranes' electrical resistances** with the phonon engineering (cf. section 4.2.2) **by a factor 2**.
- **The increase of the silicon membranes' Seebeck coefficient** thank to the phonon engineering (cf. figure 4-22) **by factor 1.4**.
- The generation of electrical power with the developed demonstrators, when they were in contact with a heat source (here emulated by Joule effect). The devices generated from **few µW/cm^2** to **few mW/cm^2** according to the temperature difference across the thermopiles and then according to the heating power.
- **Comparable performances for phonon engineering and non-phonon engineered silicon harvester demonstrators for the same temperature difference across the thermopiles** (cf. figure 4-31), reflecting the compensation of the different impacts of the phonon engineering on the silicon membranes thermoelectric properties.
- **Higher thermoelectric performances for the phonon engineering harvester demonstrators when the study is done according to the heating power** (cf. figure 4-32). This result highlighted the importance of the thermal gradient management quality on the thermoelectric performances.
- **The validation of the FEM studies' results** (cf. figures 4-38 et 4-39), confirming experimentally the conclusions made after the FEM studies, namely, the opportunity of developing low cost mass production thermoelectric harvesters for µW/cm^2 power consumption autonomous sensor nodes.
- **Better performances** of the developed demonstrators compared to the state of the art silicon based micro-harvester at the same temperature. However, when the comparison is done with the state of the art bismuth telluride micro-harvester as already observed with the FEM studies, the **performances are lower**. Nevertheless, if the thermal gradient would be taken in consideration, the developed demonstrators would have exhibit better performances than the bismuth telluride micro-harvester (cf. figure 2-18).
- **The possibility of** using the developed demonstrators for **thermoelectric cooling** applications (cf. figure 4-44). However, as it is, the thermoelectric cooling was masked by a Joule effect due to the silicon membranes electrical resistances. Therefore, for thermoelectric cooling applications, the thermopiles' design must be improved such a way to allow the Joule effect's heat dissipation.

This thesis allowed the study and the development of phonon engineered silicon based thermoelectric harvester demonstrators exhibiting performances sufficient for autonomous sensor nodes' power supplying [Vullers et al. 2009] and exhibiting comparable performances with the bismuth telluride state of the art harvester [Bottner 2005] according to the harvesters' cooling conditions. Moreover, this thesis demonstrated in addition to the energy harvesting, the possibility of developing silicon based thermoelectric coolers, opening the way to possible integration of thermoelectric coolers in silicon based micro-electronic devices

After the proof of concept demonstration of a silicon based thermoelectric harvester for autonomous sensor nodes, the next logical step is the realization of a **completely encapsulated thermoelectric harvester** from the demonstrators' work. This harvester will have the particularity to no longer have the source emulated by Joule effect. A Si wafer that will act as hot source will replace the Pt resistive heaters. The harvester design will be very close to that of the demonstrators presented in this thesis. However, there will be several challenges to overcome such as:

- The perfect redirection of the heat from the surrounding hot source to the center of the thermopiles (only on the center).
- The silicon membranes encapsulation between hot and cold sources under vacuum to get rid of any eventual conducto-convection between the Si bulk wafers
- The mechanical stress of the device. Indeed, by encapsulating the silicon membranes, they will be subject to more stress than for the current demonstrators.

The development of the encapsulated harvester can also be the chance of investigating the impact of the hot and cold end's silicon substrate engineering on the thermal gradient management through the harvester. Indeed, the investigations focused on the amelioration of the thermal gradient management through the enhancement of the silicon membranes' thermal resistances. What about the heat sources? Could we improve this thermal gradient by modifying the heat sinks? One example can be **the patterning of the silicon substrate such a way to increase the convection surface and then reduce the substrates' thermal resistances with respect to the silicon membranes' thermal resistances.**

Another important point to address is the silicon membranes based thermoelectric harvesters' electrical resistances. Indeed the thesis reported that the main drawback of the silicon based thermoelectric harvester's performance with respect to the bismuth-telluride state of the art harvester is its high electrical resistance. The thermal conductivity reduction methodology imposing the use of thin silicon membranes, this point seems difficult to address. However, the thesis' works demonstrated that embedding the silicon membranes into silicon dioxide helps to improve the thermal gradient through the thermopiles. Therefore, maybe by deepening this observation, **"thicker" silicon membranes based thermoelectric harvester with "lower" electrical resistances could be realized**.

The last opportunity is **the development of a silicon based thermoelectric coolers** from the demonstrators realized during this thesis. Indeed, a thermoelectric cooling proof of concept has been realized, but the proof of concept highlighted the importance of improving the design in order to dissipate the Joule effect masking the thermoelectric cooling. Beyond, the thermoelectric coolers realization, the evaluation of their **integration into silicon based micro-electronic devices would be of great interest.**

Bismuth telluride alloys remain the best materials for thermoelectric harvesters' development. However, with an adequate engineering: thermal conductivity reduction and generators' design, Silicon can be a very good alternative to the bismuth telluride use. Indeed, this thesis and the previous works on the silicon thermal conductivity reduction demonstrated

the feasibility of Si based thermoelectric harvester with performance more than enough to power supply autonomous sensor nodes. Moreover, the optimal phonon engineering design (trade-off between thermal/electrical conductivity reduction and Seebeck coefficient increase) and the silicon membranes embedding in an appropriate silicon oxide layer (optimal layer thickness to maximize the thermal gradient management) could contribute to enhance the Si based thermoelectric harvester's performance.

Scientific Production

Journals:

[BAH19] **T-M. Bah *et al.*** in preparation

[VER18] M. Verdier, D. Lacroix, S. Didenko, J.-F. Robillard, E. Lampin, **T.-M. Bah**, and K. Termentzidis, *"Influence of amorphous layers on the thermal conductivity of phononic crystals", Phys. Rev.* , vol. 97, no. 11, p. 115435, Mar. 2018, doi: 10.1103/PhysRevB.97.115435.

[HAR16] M. Haras, V. Lacatena, **T. M. Bah**, S. Didenko, J.-F. Robillard, S. Monfray, T. Skotnicki, E. Dubois, *"Fabrication of thin-film silicon membranes with phononic crystals for thermal conductivity measurements"*, *IEEE Electron Device Letters*, **37**, 1358-1361 (2016)

Conferences:

[ROB18c] J.-F. Robillard, **T-M. Bah**, S. Didenko, T. Zhu, D. Zhou, J. Yin, E. Dubois, P.-O. Chapuis and S. Monfray, *"Demonstration of low-thermal conductivity silicon nano-patterned membranes as a thermoelectric material",* Nanoscale and Microscale Heat Transfer VI Eurotherm 111, 2-7 Dec, 2018 Levi, Lapland, Finland

[DID18] S. Didenko**, T-M. Bah**, M. Massoud,V. Lacatena, M. Haras, R. Orobtchouk, J. M. Bluet, P O Chapuis, E. Dubois, J.- F. Robillard, *"Artificially-induced anisotropic heat flow in 2D patterned membranes",* Nanoscale and Microscale Heat Transfer VI Eurotherm 111, 2-7 Dec, 2018 Levi, Lapland, Finland

[BAH18b] **T.M. Bah**, S. Didenko, J.F. Robillard, S. Monfray, M. Haras, T. Skotnicki, E. Dubois, *"Demonstration of a Silicon Thin Film, Phonon Engineered Thermoelectric Converter"*, 50th European Solid-State Devices and Materials conference, SSDM 2018, Tokyo, Japan, sept. 09-13 (2018)

[BAH18a] **T.M. Bah**, S. Didenko, J.F. Robillard, S. Monfray, M. Haras, T. Skotnicki, E. Dubois, *"Performance Evaluation of Silicon Based Thermoelectric Generators Interest of Coupling Low Thermal Conductivity Thin Films and a Planar Architecture"*, 48th European Solid-State Device Research Conference, ESSDERC 2018, Dresden, Germany, sept. 03-06 (2018)

[YIN18] J. YIN, T.Q. ZHU, D. ZHOU, **T-M. BAH**, S. DIDENKO, S. GOMES, O. BOURGEOIS, D. PELLERIN, E. DUBOIS, J-F. ROBILLARD, *"Nanometer-scale active thermal devices for thermal microscopy probe calibration"*16èmes Journées de la Matière Condensée, JMC 2018, Grenoble, France, 27-31 août, 2018, 513-513

[ROB18b] [Invited] J-F. ROBILLARD, **T-M. BAH**, D. ZHOU, S. DIDENKO, T.Q ZHU, V. LACATENA, M. HARAS, A. MASSOUD, E. DUBOIS, J-M BLUET, O. CHAPUIS, S. MONFRAY, *"Fabrication and thermal characterization of silicon membranes for integrated thermoelectric converters",* 16èmes Journées de la Matière Condensée, JMC 2018, Grenoble, France, 27-31 août, 2018

[ROB18a] [Invited] J-F. ROBILLARD, **T-M BAH**, S. DIDENKO, D. ZHOU, E. DUBOIS, S. MONFRAY, *"Microwatt silicon thin-films thermoelectric harvesters"* 19th International Symposium on the Physics of Semiconductors and Applications, ISPSA 2018, Jeju, Korea, july 1-5, 2018, paper WeA2-1

[DID17] S. DIDENKO, A-M. MASSOUD, **T-M. BAH**, J-F. ROBILLARD, P-O. CHAPUIS, J-M. BLUET, E. DUBOIS, T. SKOTNICKI *"Thermal conductivity in Si 2D phononic membranes studied by Raman thermometry"* GDRe Workshop on Thermal NanoSciences and NanoEngineering, Villeneuve d'Ascq, France, November, 23-24, 2017,

[BAH17] **T.M. Bah**, S. Didenko, J.F. Robillard, S. Monfray, M. Haras, T. Skotnicki, E. Dubois, *"Planar architecture for thin silicon film based thermoelectric generators"*, European Materials Research Society Fall Meeting, E-MRS Fall 2017, Warsaw, Poland, sept. 18-21 (2017)

Awards:

[UCL18] 3rd prize for the best thesis awarded by the Research Council of Lille Catholic University, 2018 Edition

[E-MRS17] Winner of the "best student presentation award", E-MRS fall meeting, Warsaw Poland 2017

Activities:

[JNTE17] Participation to « journées nationales de la thermoélectricité », Montpellier France, December 2017

[NiPS 17] Participation to "the energy harvesting summer school" organized by the NiPS lab, Gubbio Italy, June 2017

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