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THÈSE

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Convertisseurs thermoïoniques à gap micrométrique : matériaux, conception et fabrication d'un démonstrateur

Soutenue le 17 décembre 2019 devant le jury composé de:

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General Introduction

The efficiency of energy generation is one of the main indicators of the development level of human society. While the technology of massive production of high-quality energy, especially electrical energy, have not been revolutionarily innovated for many decades, the importance of harvesting low-quality energy and converting to high-quality energy are keeping increasing [Petroleum 18]. The Unconventional principles of thermoelectric generation project (UPTEG) funded by the European Research Council focuses on the performance of thermoelectrics, including phononic engineering, thermoelectric generator (TEG) based on Seebeck effect and micro thermionic converters based on thermionic emission. This thesis is one part of the UPTEG project and is focused on Micro-Thermionic Convertor (MTC).

Generally speaking, the performance of thermoelectric energy generators (TEG) has been limited by the difficulty of conciliation between electron-crystal electrical conductivity and phonon-glass thermal properties [Rowe 95]. These are two ambivalent factors ruling the conduction of both electrical and thermal currents. The figure of merit (zT) is a value that represents the trade-off between these ambivalent properties [Kittel 96]. In recent decades, with the microelectronics processes, micro/nanoscale structuration is intensively researched and proved to yield better zT by means of electron and/or phonon confinement.

However, the Micro Thermionic Converter, which is an unconventional thermoelectricity converter based on thermionic effect, has theoretically near zero heat conduction, and an equivalent zT about 10 which is higher than solid-state conversion. At the same time, MTCs have all the great advantages of solid-state convertors. It converts heat in to electric current in direct, silent way, without mechanical movement and in a reliable way. MTCs have a remarkably different compared to TEGs. MTCs consist in a pair of parallel electrodes with high temperature difference separated by a micron scale vacuum gap. Both electrodes are coated with low work function materials, which helps hot electrons evaporate and emit from the hot electrodes' surfaces efficiently.

MTC is one type of Thermoelectric Converter (TC). Despite potentially very high current densities, TC is a technical route abandoned in the 90s' due to several reasons. The complexity in the fabrication of large surface parallel electrodes with micrometer gaps in between was more than difficult at that time. Secondly, it is hard to overcome the problems of thermal losses. Last, the space charge effect in large dimension gaps that originally were supposed to be solved with plasma technology leads to more engineering challenges. However, MTC has become a promising solution, due to the fact that the microfabrication technology has been greatly improved. In recent years, scientific research on Thermionic Energy Converters (TEC) revives.

The field of Thermionic Energy Converters is a huge topic that relates solid-state physics, solid-state chemistry, materials science and thermal engineering. The diversity of academic subjects and complexity of the topic makes it hard, if not impossible, to fully demonstrate in one single thesis. So what is presented here focuses on synthesis and characterization low work function alkali metal oxide material films, thermal-gradient finite element modelling simulation, fabrication of prototype MTCs with careful thermal engineering design and characterization.

The targets in this project that we propose include: explore the renewed approach based on electronic micro fabrication technology; test working state at an easier regime with non-ignited and low space charge; build a reasonable temperature difference between electrode at about 100K; propose an

alternative revolutionary solution to power applications in lower power devices from microwatt to watt range.

This manuscript is organized in four chapters. The first chapter presents the general view of thermionic energy conversion including MTC basics, history, the state-of-the-art and our approach in the frame of the UPTEG project. The second chapter focuses on low work function material coating by two different technologies and film work function characterization with different methods and with different equipment. The third chapter reviews existing models and designs of MTCs compared to the prototype of this project with numerical simulation of thermo-isolation and temperature gradient management. The fourth chapter presents the technological part of this thesis including the device layout design, step-by-step fabrication, setup integration and finally prototype characterization. At last, is the overall conclusion to the unconventional thermoelectricity convertor based on thermo-electronic emission.

Chapter 1

This chapter provides a general view of thermal energy generator/harvester with general review about the motivation for the thermal energy field as a constantly researched topic. At the beginning of this chapter, recent data about global energy consumption is presented. Each year the total consumption is rising, however with limited renewable energy production, the energy crisis needs to be considered seriously. On the other side, thermal energy has a massive potential to be utilized . It is an abundant source and easy accessible, which promises thermal energy generators to a bright future. Then, illustration of the thermionic energy convertor basics, which include its working principles, its structure and its first discovery. Then a history of almost 100 years of conception and innovation of thermionic convertors is studied. Later, the state-of-the-art is reviewed with all recent models and approaches to build efficient MTCs with efforts of different aspects. At last is our approaches in the frame of the UPTEG project with two different material candidates and two coating processes with corresponding device structures.

Chapter 2

With this knowledge, the properties of how MTCs work, a highly efficient emitting material must be integrated at the surface of electrodes. The first section will be a simple introduction to work function. Since the work function is not a characteristic of a bulk material, rather as a property of the surface [Halas 10], what the MTCs really require is a film from several atoms thickness or at most several nanometers. This chapter will then present the development of a system with sound workflow to achieve low work function film deposition and characterization. One of the highlights is to match the work function results of different measurement principles on one single sample. This matching process increases the reliability and repeatability of measurement and can help to avoid the influence of Kelvin Probe surface pollution due to chemical vapor deposition in the chamber.

Particularly, we analyze and compare the performances of two alkali metal oxides: Potassium oxides (K_xO_y) and Cesium oxides (Cs_xO_y). These compounds feature a very low work function lower than 1 eV which are even better than alkali like potassium metal and cesium metal. These elements are also abundant and not particularly dangerous in experimental conditions. In our workflow these alkali material were firstly deposited on highly-doped clean silicon surface to form a thin film. The oxide thin films were characterized by Kelvin Probe, photoemission and thermionic emission measurements. Then X-ray photoelectron spectroscopy and energy-dispersive X-ray spectroscopy were also tested. All the results on the synthesis of these thin films were obtained under high vacuum and controlled temperature.

Chapter 3

Although, in theory, the MTCs has little to no thermal leakages and not like other thermoelectric generator that need to balance between electron-crystal electrical conductivity and phonon-glass thermal properties, thermal leakages also need to be carefully considered in real devices. Furthermore, unlike TEGs, the heat gradient direction of MTCs are perpendicular to the wafer surface. A considerable temperature difference, ideally over 100 degrees, needs build up in less than one-millimeter distance. This is the biggest challenge for the real MTC devices. To meet this demand a layer of both electrical and thermal isolation material is needed in between the electrodes, which at the same time provides structure stability.

This chapter focused on designing possible structures and corresponding parameters for the design of a prototype with maximum efficiency in real experimental conditions. Different finite element analysis were performed to explore the technical indicators for an efficient MTC with acceptable thermal losses and best temperature difference between the two electrodes.

Chapter 4

This chapter presents engineering and technological aspects of this work including design and fabrication of the prototype. As a prototype, the design needs to be harmless, cheap, industrially compatible and reliable based on existing nano/micro-fabrication processes and technology. One of the best solution is to fabricate upon silicon on insulator (SOI) wafer with silicon (Si) layer thickness of 200nm.

After fabricating the electrodes with gaps, we integrate it to our characterization platform before low work function film deposition on electrode surface in-between the vacuum gap. Then the MTC was ready to be tested. The prototype MTC proves that thermo-convertors based on thermo-emissions effect are one environmentally friendly, cheap and industrially compatible generator with much higher potential than other energy harvest devices.

[Petroleum 18] British Petroleum, “BP Statistical Review of World Energy 2018” British Petroleum, 67th annual statistical report on world energy, June 2018

[Rowe 95] D. M. Rowe, CRC Handbook of Thermoelectrics (CRC, Boca Raton, 1995).

[Kittel 96] Charles Kittel, “Introduction to Solid State Physics”.

[Halas 10] Stanislaw Halas, Tomasz Durakiewicz, “Is work function a surface or a bulk property?”, Vacuum, 85, 486-488 (2010)

Introduction Générale

L'efficacité de la production d'énergie est l'un des principaux marqueurs du niveau de développement d'une société humaine. Bien que la technologie de production massive d'énergie de haute qualité, en particulier l'énergie électrique, n'ait pas été révolutionnée depuis de nombreuses décennies, l'importance de la récolte d'énergie de faible qualité et la conversion en énergie de haute qualité est de plus en plus forte [Petroleum 18]. Les principes non conventionnels du projet de production thermoélectrique (UPTEG) financé par le Conseil Européen de la Recherche se concentrent sur les performances thermoélectriques, y compris l'ingénierie phononique, le générateur thermoélectrique (TEG) basé sur l'effet Seebeck et les micro convertisseurs thermiques à base d'émission thermoïnique. Cette thèse est une partie du projet UPTEG et se concentre sur le Convertisseur Micro-Thermoïnique (Micro-Thermionic Converter MTC).

D'une manière générale, la performance du générateur d'énergie thermoélectrique (TEG) est limitée par la difficulté à concilier une conductivité électrique forte, comme celle d'un cristal, et une conductivité thermique faible, comme celle d'un verre [Rowe 95]. Il s'agit de deux facteurs ambivalents qui gouvernent la conduction du courant électrique et thermique. Le Facteur de mérite (zT) est une valeur qui représente le compromis entre ces propriétés ambivalentes [Kittel 96]. Au cours de la dernière décennie, avec les procédés de la microélectronique, la micro/nano structuration est vue comme une voie pour obtenir une amélioration de zT grâce au confinement des électrons et/ou phonons.

Cependant, dans le cas des Convertisseurs Micro Thermoélectroniques, qui sont des convertisseurs non-conventionnels basés sur l'effet thermoïnique, la conduction de chaleur est théoriquement proche de zéro. Cela permet un zT équivalent à environ 10 qui est plus élevé que la conversion à l'état solide. Alors que, dans le même temps, les MTCs ont tous les avantages liés à l'état solide. Ils convertissent la chaleur en courant électrique en directement, silencieusement, sans parties mobiles et de manière fiable. Les MTCs ont un principe remarquablement différent des TEGs. Les MTCs consistent en une paire d'électrodes parallèles avec une différence de température élevée, séparées par un vide à l'échelle du micron. Les deux électrodes sont revêtues de matériaux à faible travail de sortie, ce qui permet aux électrons de s'évaporer de la surface de l'électrode chaude.

Comme les TEGs, le MTC est un type de convertisseur thermoélectrique (TC). En dépit de densités de courant potentiellement très élevées, TC est une voie technique abandonnée dans les années 90 pour plusieurs raisons. La complexité de la fabrication de grandes électrodes parallèles avec des écarts micrométriques était plus que difficile à l'époque. Deuxièmement, il est difficile de surmonter les problèmes de pertes thermiques. Enfin, l'effet de charge spatiale est prépondérant pour les gaps de grande dimension. Ce phénomène était censé être résolu par la technologie de plasma qui conduit à encore plus de défis d'ingénierie. Cependant, le MTC est une solution prometteuse, en raison du fait que la technologie de microfabrication a été grandement améliorée. Ces dernières années, la recherche scientifique sur les convertisseurs énergétiques thermoïniques (TEC) est ravivée.

Le champ des Convertisseur Micro-Thermoïnique est un sujet énorme qui allie physique à l'état solide, chimie à l'état solide, science des matériaux et de l'ingénierie thermique. La diversité du sujet académique et la complexité du sujet rendent difficile, voire impossible, de le traiter pleinement en une seule thèse. Donc, ce qui est présenté ici se concentre sur la synthèse et la caractérisation de faible travail de sortie des films d'oxyde de métal alcalin, simulation de modélisation d'éléments finis à

gradient thermique, prototype de fabrication de MTCs avec une conception d'ingénierie thermique minutieuse et caractérisation des prototypes du MTC.

Les objectifs de ce projet sont notamment: explorer l'approche renouvelée basée sur la technologie de micro-fabrication; tester l'état de fonctionnement à un régime plus facile avec une charge d'espace faible; établir une différence de température raisonnable entre les électrodes d'environ 100K; proposer une solution alternative aux applications de puissance dans les appareils de faible puissance de la gamme microwatt au watt.

Ce manuscrit est organisé en quatre chapitres. Le premier chapitre présente la vision générale de la conversion de l'énergie thermoïnique, y compris les bases de MTC, l'histoire, l'état de l'art et notre approche dans le cadre du projet UPTEG. Le deuxième chapitre se concentre sur le revêtement de matériaux à faible travail de sortie par deux techniques différentes et la caractérisation du travail de sortie de film avec différentes méthodes et avec différents équipements. Le troisième chapitre présente les modèles existants et la conception des MTCs comparés au prototype de ce projet avec une simulation numérique du transfert et de l'isolation thermique et de maintien du gradient de température. Le quatrième chapitre présente la partie technologique de cette thèse, y compris la conception et l'agencement des dispositifs, la fabrication étape par étape, l'intégration et enfin la caractérisation des prototypes.

[Halas 10] Stanislaw Halas, Tomasz Durakiewicz, "Is work function a surface or a bulk property?", Vacuum, 85, 486-488 (2010)

[Kittel 96] Charles Kittel, "Introduction to Solid State Physics". 1996

[Petroleum 18] British Petroleum, "BP Statistical Review of World Energy 2018" British Petroleum, 67th annual statistical report on world energy, June 2018

[Rowe 95] D. M. Rowe, CRC Handbook of Thermoelectrics (CRC, Boca Raton, 1995).

Chapter 1 Thermionic Energy Conversion

This chapter provides a general view of thermal energy generators/harvesters and the motivation for the thermal energy field as a constantly researched topic.
At the beginning of this chapter, recent data about global energy consumption is presented. The total consumption is rising each year, however with limited renewable energy production, the energy crisis need to be considered seriously. On the other side, thermal energy has a huge potential to be utilized with its abundant sources and accessibility, which promise all thermal energy generators to a bright future. Compared to other energy harvesting devices TEC has many advantages, while several challenges remain to be solved.
Later in this chapter, the thermionic energy convertor basics are illustrated, which include its working principles, its structure and its first discovery. The history of almost 100 years of conception and innovation of thermionic convertors is presented. Later, the state-of-the-art is reviewed with all recent models and approaches to build an efficient MTC with efforts of different aspects. At last, our approaches in the frame of the UPTEG project with two different material candidates and two coating processes with corresponded device designs.

1.1 Energy conversion and generation

1.1.1 Energy consumption and electric energy in the world

Energy is not only a basic scalar physical quantity but also the cornerstone of development of human civilization. With the process of understanding and taking advantage of different types of energies, from potential energy, kinetic energy to chemical energy, from thermal energy to electric energy, the human productivity improves together with human society. The modern society, nowadays, is maintained by the enormous energy supply and is in constantly rising demand of all types of energies. The energy consumption rate is a barometer of the human society. According to [Petroleum 2018] a constant growth of consumed primary energy can be observed during last decades. In 2010, a serious financial crisis began causing a significant recession in both industrial branches and the tertiary industry, which is revealed as a global drop in primary energy consumption.

Years after the start of second industrial revolution in the late 19th century, the electrification of industry took place [Nye 90], followed by household electrification at 1920s in cities. With the massive utilization of electricity and electrification the inexpensive production of aluminum, chlorine, sodium hydroxide and magnesium became possible [McNeil 90]. However, around 100 years after electrification, in 2014 the fossil energy production still takes a ratio of 81%. The latest data show, in year 2017, global electricity production reaches 25551.3TWh [REN21 2018], among which 73.5% is generated by fossil fuel and nuclear energy which is known as not renewable sources. On the other side, 26.5% of global electric energy was provided by the renewable sources with an annual increase of 2% compared to 2016. Thanks to the development of photovoltaic power generation and massive construction of wind power farms, year 2017 has the greatest renewable electricity ratio increase during the past decade.

		2013	2014	2015	2016	2017
Global electricity production	TW·h	23457.6	23918.8	24289.5	24930.2	25551.3
Fossil fuel energy and nuclear energy	%	77.9	77.2	76.3	75.5	73.5
Renewable energy	%	22.1	22.8	23.7	24.5	26.5
Hydropower	%	16.4	16.6	16.6	16.6	16.4
Wind	%	2.9	3.1	3.6	4.0	5.6
Biomass	%	1.8	1.8	2.0	2.0	2.2
Solar	%	0.7	0.9	1.2	1.5	1.9
Geothermal, CSP and Ocean	%	0.4	0.4	0.4	0.4	0.4

Table 1.1 Ratios of electricity generation from BP Statistical Review of World Energy 2018

Table 1.1 presents the trend of global energy production by different resource. In between 1980 to 2013, in average, world electricity generation by renewable sources has an increase rate of about 3.6%. This annual increase rate in the closest five recent years is almost 8.2%, which is more than twice the previous rate. Due to the high efficiency of electricity use, compared to other energy consumption methods, electrical energy is surely a better choice. So all the efforts to increase the production of electricity from renewable energy are worthwhile.

On the other side, the typical non-renewable energy, the fossil fuel energy has a much lower efficacy compared to electricity. For instance, most of all modern vehicles operate with internal combustion engines that consume fossil fuel. However, despite the pollution of the internal combustion engine, only one quarter of all input energy is transformed into movement. Figure *1.1* present the energy lost at each stage and resulting in a final efficiency of about 25%. If counting from on wheel power, the efficiency may be even lower. One thing worthy to mention is that even through the absolute efficiency

seems to be a low value, it is not that bad when compared to Carnot efficiency due to the intrinsic limitation of all heat engines.

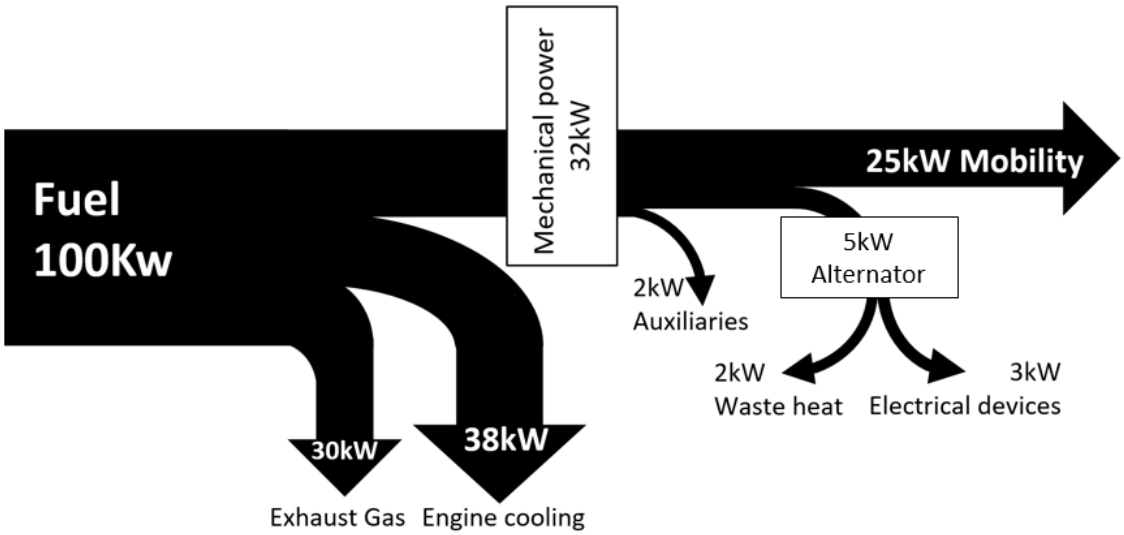

Figure 1.1: Sankey diagram for diesel light duty vehicles.

In European Union, 12% of the total CO_2 emission are generated by internal combustion engine [EU 2015]. Furthermore, more pollution like sulfide, nitrogen oxides NOx (NO and NO_2) and solid micro particles are also not negligible. These widely distributed engines lead to a bigger problem dealing with the pollution. For thermal power electrical stations operated by fossil fuel, the pollution is concentrated and can be well treated by various specific devices and processes, which is not possible for vehicles. The example above tells that electrical energy is a clean and better solution for the human energy demand.

With the conclusion that electricity is among the best energy form for human industry and living, facing a great accelerating of energy consumption, the necessity of efficient power conversion is needed more than ever before. Unfortunately, all known conversion types for electricity power has some defects either products great amount of pollution or dangerous by-products. For some renewable electrical energy production methods, the defects are either high cost or negative impact on natural environment. The idea of energy production from waste energy is thus receiving more and more attention recently [Harb 11], [Harne 13], [Matiko 14] and [Radousky 12].

So from where the energy can be generated? Nowadays, one of the most popular answer is solar energy, which is the ultimate source of fossil fuel energy, hydropower, wind energy etc. Beginning from year 2005, the photovoltaic devices and total power generation by photovoltaic increased rapidly. Thanks to the technology development and the governmental actions, the price of this renewable energy production device has dropped over 95% in a few years, which accounts for the explosive development of this clean energy. In recent years, the industrially produced solar cells have reached a highest efficiency of 21.5%, while the highest efficiency of multi-junction solar cells in laboratory is reported to be 46.0% [Dimroth 14]. However, the character of photovoltaic energy means it is highly dependent on fatal conditions like weather and sunshine direction.

On the other side, when the question is that from where the energy can be harvested? Harvesting from thermal energy is the most promising answer. During the electricity production and transportation about two third of total input primary energy was lost and converted into thermal energy

[International energy agency 2008] and only around 31.5% of the input energy was delivered to consumers as electric energy in 2007. For some more instance, 19.5%-50% of overall primary energy consumption turns into heat losses of dwelling, 6.5%-16.7% of energy consumption in industrial scenario is lost in form of heat. All over the world, a surprisingly high rate of energy is lost in the form of heat. In other words, more energy is lost than it is consumed. So to preserve the economic growth and develop an alternative energy sources is a critical task for all humans before the fossil fuels heading to depleted.

In this report, an unconventional method of energy harvesting and generation will be presented with details. The very first idea of energy harvesting comes from harvesting electrical energy from heat. Thermal energy is what most types of energy ends into. What's more, thermal energy is the most abundant and easily accessible energy form. Therefore, it is one of the best source for energy harvesting. Fortunately, with the development of semi-conductor micro fabrication technology, this unconventional energy harvesting method can be miniaturized and has a promising future.

1.1.2 Conventional Thermal energy generator based on Seebeck effect

Talking about harvesting electrical energy from heat, the first and most popular solution is thermoelectric generator (TEG), which is also named Seebeck generator. As it is named, the TEG has a working principle based on Seebeck effect. A TEG works like any heat engines, with the given thermal input and temperatures at both sides forming a temperature gradient, has an output as electrical potential. The fact that a heat flow passing through material leads to a drift of charge carriers, which consequently result in a voltage difference. Thomas Johann Seebeck firstly discovered this phenomenon [Seebeck 25] [Seebeck 26] in year 1821.

It seems to be a great way to convert energy from heat to electricity and it has been produced for military and aerospace applications for decades. However, it has a low typical efficacy of 5-8%. Note that these devices are reversible and most popular usage is heat pumps. The biggest problem is limited by the development of material science. The performance of thermoelectric generation has been limited by the difficulty of conciliation between electron-crystal electrical conductivity and phonon glass thermal properties [Rowe 95]. In other words, to design thermoelectric generators with good performance, a material with high conductivity and at the same time a low thermal conductivity property is needed.

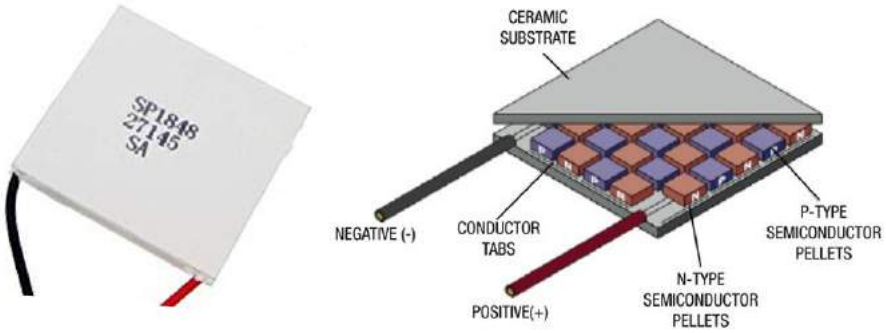

Figure 1.2 (a) Photo of commercial TEG product; (b) Inner structure of TEG module.

Figure *1.2* presents a typical commercial TEG module and its inner structure, which is an array of P-type and N-type semiconductor in series. With the ceramic substrate of different temperature at two

side, a temperature gradient is established along each semiconductor. Charge carriers of different types will drift from hot to cold. With the movement of these carriers, a thermal current and voltage potential are created.

Still, in real case scenarios, the TEG has some engineering defaults that need to be solved: High generator output resistance which is not friendly for low impedance loads as a power supplier; low thermal conductivity which is not a good harvester for heat source as a digital microprocessor; and limited capacity for release cold-side heat to air which add an additional parasitic loss to total output.

Despite the challenges facing TEG, with the advantages of thermoelectric generator, it is still the most popular and wide production device for thermal energy harvester/generator.

1.1.3 Unconventional Micro Thermionic energy Convertor and its structure

In this section is focused on the basic principal of Micro Thermionic energy Convertor. The basic principles are simple, and phenomenas are around us in daily life. As we know when metal is heated to a high enough temperature, the electrons will have higher energy. When electrons have enough energy to overcome the work function barrier, electrons can be emitted from a metal surface. Just like Figure *1.3* presented, in old cathode tube TV, screen shines when electrons hit the fluorescent screen, and these electrons ejected from electron gun are firstly emitted from heated filament. The heated filament has a high enough temperature and electrons can easily escape from filament surface.

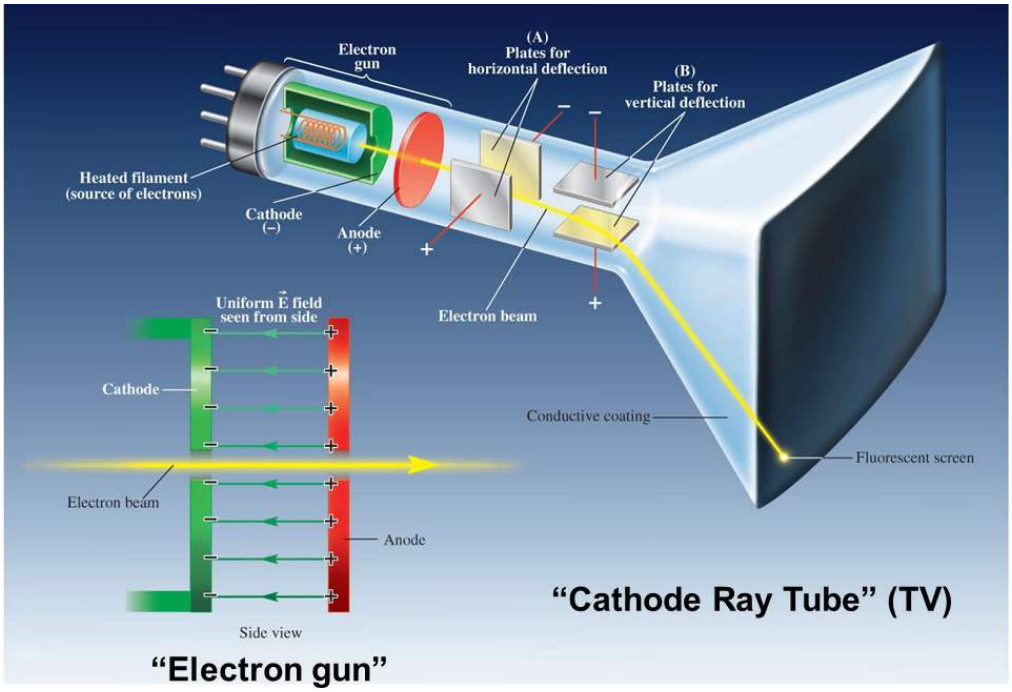

Figure 1.3: Principle of Cathode Ray Tube TV.

The Micro Thermionic energy Converter or MTC works in the same principle as presented in Figure *1.3*. MTC converts thermal energy into electrical energy directly. The basic structure of convertor consists of a high temperature electrode and a low temperature electrode parallel positioned with a vacuum gap separating the two electrodes. This direct energy conversion is based on thermoelectric emission or thermionic emission. Being in contact with heat source, the hot cathode reaches a high temperature, and electrons from this surface get enough energy for extraction and evaporation from the surface of the conductive material. Some electrons will transport through the vacuum gap and arrive at the cold

anode. This phenomenon was firstly demonstrated in 1880 by Thomas Edison. During the experiment to determine the origin of filament breaks inside lamps and the blackening of incandescent lamp bulbs, the thermionic electron emission was observed [Waits 03] [Fleming 96]. Then in 1915, this energy conversion principle was proposed by W. Schlichter [Schlichter 15].

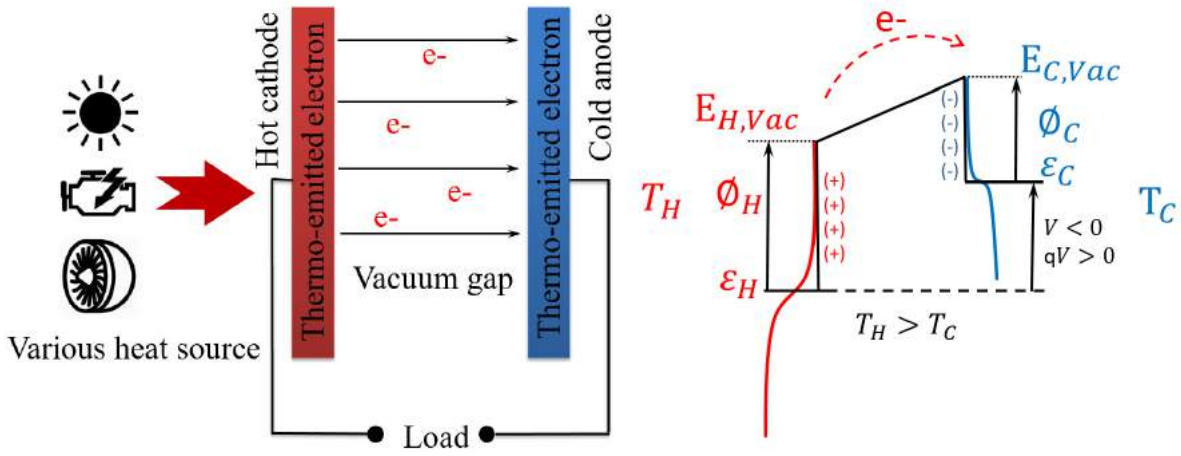

Figure 1.4 (a) Generic architecture of a MTC; (b) Energy diagram of MTC.

Presented in Figure *1.4*(a), the simplest structure of Thermionic energy Converter is constituted by two parallel electrodes facing each other, with thermionic electrons evaporated and emitted from hot electrode to the cold electrode. The thermionic current can then pass through a load connected to the load circuit of the converter. For Micro Thermionic Converter, the "micro" term applies to the vacuum gap distance. MTC with several micrometer large vacuum gap will get best performance. The Figure *1.4*(b) is an energy diagram representing the energy band of hot cathode and cold anode. Firstly, like the architecture diagram these two electrodes are separated by a vacuum gap. Both side of electrodes has its electrical potential and corresponding Fermi level ε. The work function Ø is the property of each electrode surface material. Then the hot cathode is heated by absorbing the heat from any kind of energy source. With the increasing temperature, the electrons have enough energy jump to vacuum level E_{Vac} and some may evaporate from its surface. Some electrons arrive at cold anode and if the circuit is open, potential will consequently build up at the anode. The cathode losing electrons will be positively charged. With negative charge on anode, Fermi level (and thus vacuum level) shifts up, repelling backward electrons. Finally, an equilibrium is reached when the forward and backward currents equalize. The energy band in the gap can be present with a striate line connecting vacuum level of cathode and anode. Detailed research about the size of vacuum gap, corresponding heat loss crossing the gap and final efficiency as a function of gap parameters will be discussed in chapter 3.

With great advantage for MTC energy conversion conception is its simple physical phenomenon. Moreover, without any moving element, MTC is particularly suitable for miniaturization and compatible with all existing MEMS technology. It is not hard to imagine that one day in the close future with sensor and its power supplier all integrated on the same silicon chips, sensors can be easily distributed at more position without the limitation of power supply. Finally yet importantly, theoretically speaking the MTC will reach a high efficiency, which can be as much as 21% at low temperature working condition (T_H=400K T_C=300K). The efficiency of MTC is calculated by the total output divided by total input power. To well understand the efficiency of a heat engine, the efficiency is compared to Carnot limit. Carnot efficiency is the theoretical maximum efficiency for all reversible heat engine at given working condition. 21% total efficiency is 85% of Carnot's limit, which is an efficiency far forward comparing to conventional technologies.

1.1.4 Comparison of two thermal electric convertors

After presenting two thermal energy generators based on different physical phenomena, a simple comparison will be illustrated in this sector. Begin from what these two thermal convertors have in common. First of all, due to the fact that thermal energy is abundant and easily accessible energy, both types of thermal electric convertors have a stupendous potential and a bright future. Secondly, the research and development of a better TEG or MTC are highly depending on material science. For TEGs the need to find a material with low thermal conductivity and high electrical conductivity is essential. This property of materials, in thermoelectric research field, is evaluated by zT, the figure of merit.

$$\mathrm{zT} = \frac{S^2}{\rho\kappa}T = \frac{S^2\sigma}{\kappa_e+\kappa_l}T \qquad \text{Eq 1. 1}$$

The figure zT is a property of material and calculated by Eq 1.1, where S is Seebeck coefficient, ρ is electrical resistivity, σ is electrical conductivity, κ is the thermal conductivity, κ_e is electronic thermal conductivity and κ_l is lattice thermal conductivity and T is cold temperature. The zT value for thermal energy generators can be calculate by the properties of used material. For MTCs, the corresponded zT values is obtained by fitting it efficiency by the same working condition, the T_c. Unlike efficiency, which is a variable value at different working Temperature for a same device, figure of merit zT present the ability of a given material or heat engine to efficiently produce thermoelectric power in all working temperature range.

So why the MTC has a higher zT than TEG? One main difference is the thermal conductivity through the device. For the TEG, heat passes through thermoelectric materials by conductivity. In other words, the thermoelectric material physically connects the heat source and cold heat sink. While the MTC works differently in the case of thermal flow. By eliminating the material between hot energy source and cold electrode, the only heat exchange through the vacuum gap is by radiation. This results in much lower thermal loss and greater efficiency. With zT values, the maximum efficiency at different temperature can be calculated by the following equation.

$$\eta = (1-\frac{T_C}{T_H})\cdot\frac{\sqrt{1+zT}-1}{\sqrt{1+zT}+\frac{T_C}{T_H}} \qquad \text{Eq 1. 2}$$

Figure *1.5* presents, at given cold temperature equal to 300K, thermal engine efficiency for different values of the figure of merit working at different input hot temperature. Generally speaking, the thermal engines nowadays have an equivalent zT value of about 0.7. The refinement of the technology has a possible limit of up to 2. Some of the best efficient geothermal power plants have an equivalent zT of about 4. Furthermore for some nuclear power plant and solar power plant, an equivalent zT of 10 can be possible [Vining 09]. For a MTC with electrode work function at 0.5eV the equivalent figure of merit is about 10. This means that MTC can reach a total thermal efficiency of 50% if it is working at nuclear powered heat source, which is about 1300K.

$$\eta_{Carnot} = 1-\frac{T_\mathrm{C}}{T_\mathrm{H}} \qquad \text{Eq 1. 3}$$

$$\eta_{CN} = 1-\sqrt{\frac{T_\mathrm{C}}{T_\mathrm{H}}} \qquad \text{Eq 1. 4}$$

In Figure *1.5*, two reference solid lines are presented. The back line is Carnot efficiency at given condition, and the red solid line is Chambadal-Novikov efficiency. In the case of vacuum thermionic energy conversion T_C and T_H are temperature corresponding to cold anode and hot cathode. The Carnot efficiency η_{Carnot} is the maximum efficiency possible for reversible engines. The red line

represents the efficiency at maximum power output for all endo-reversible thermal engines. Corresponding equations for Carnot and Chambadal-Novikov efficiency are presented above.

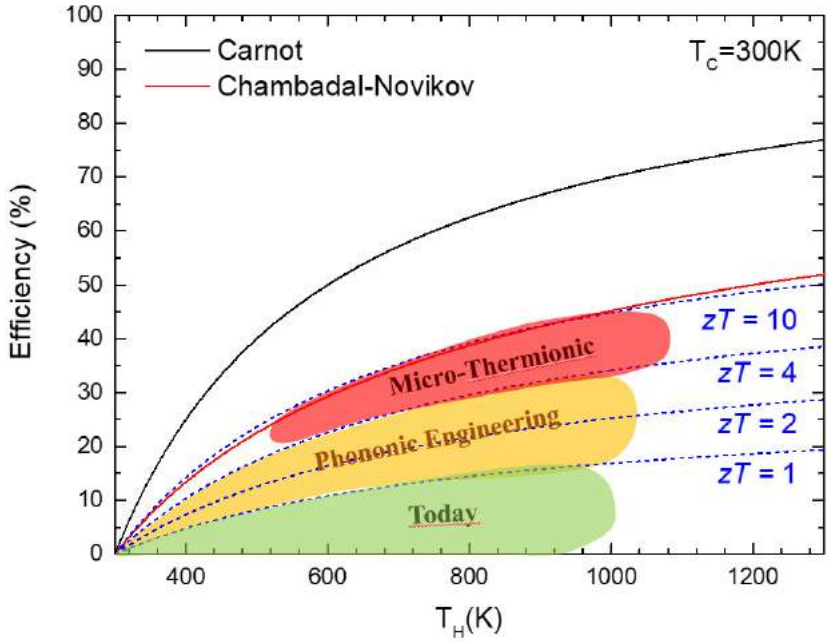

Figure 1.5 At different figure of merit, temperature-efficiency plots.

During the design process of a reliable thermal generator, in order to achieve high efficiency in the system requires extensive engineer design in order to balance between the heat flow through the device and maximizing the temperature gradient across them. For our project, the discussion of efficiency and maximization of temperature gradient will be present in Chapter 3.

What is the difference between these two thermal electrical generators? First, due to different generation principles the 3D structure of TEG is more complicated and need either new material or doping technology with dedicated structure for each cell of semiconductor. The complicated structure means it will meet more challenges when facing thermal stress in operation environment. On the other hands, for MTCs, structure is much simple. The only concern of MTCs' structure is building the temperature gradient and limit heat flow. The second difference in between two types of thermal generators is the geometric direction of studied materials process and the direction of temperature gradient direction. In the case of TEG, the temperature gradient has same direction as material geometric length direction. For MTCs, the low work function coating material on the electrodes' surface are perpendicular to thermal gradient. Due to the fact that the power output of thermal electrical device is proportional to its surface. The fabrication of a massive scale TEG device are much more complicated. On the other side, the surface coating process can usually applied on a bigger surface. Last is the potential of two principles. The Seebeck effect is easy to tackle and consequently lots of TEGs have been commercialized and products for civilian use can be found on the market. The MTCs are much more difficult and far from the process of commercialization, due to the current limitation by space charge effect and the limitation of old mechanical fabrication methods. However with newly developed Micro/Nano-fabrication process in 21 century, MTC has much larger potential to be researched and discovered.

1.1.5 Thermionic energy convertor challenges

Similarly to TEG, the research and development of TEC are limited by material science. In order to make electrons easier to escape from the hot cathode's surface, a lower work function material is necessary. With a material of 0.5eV work function, the equivalent zT can be as high as 10, while with a work function of 1.0eV, the zT value drop to below 1 at less than 1000K working range. Moreover, the corresponding coating process of this low work function material is critical, in order to have a stable and uniform coating on cathode substrate. A stable coating process is critical. The surface will be facing a tough mechanical and thermal condition during working circumstances. In this case, when a high temperature will be applied on one electrode, a thermal stress will be applied on the structure. So a stable coating material and process will contribute greatly in fabrication and increase device stability.

The mechanical structure in between electrode and in micro vacuum gap should be rigid and resist the atmosphere pressure with vacuum inside. In addition, it should be as small as possible with material of minimum thermal conductivity. Other than thermal stress, mechanical fatigue caused by large number of thermal cycles should be taken in to consideration.

1.2 History from 20th century to 21th century, the history and future

Other than challenge of finding a better material with lower work function and improving some engineer stabilization properties, there are many methods to approach a better performance for Thermionic Convertors (TC), including:

- **High particle velocity/grid** [Child 1911] [Langmuir 1913]
- **Arc-mode (ignited mode)/hybrid** [Langmuir 1923] [Schlichter 1915]
- **Plasmatron principle** [Hatsopoulos 1963]
- **Resonance ionization** [Hernqvist 1958] [Lee 2012]
- **Reduce inter-electrode gap** [Kiejna 1979] [Durakiewicz 2001] [Ibragimov 2001]

In this section, history of TCs with different scientific approach at different decades will be presented.

1.2.1 Early research during 20th century

After the first scientific report about the electron emission by Elster and Geitel in 82[Elster 82], and the discovery of Edison effect from Edison' lamps in 1884, the cathode rays were identified by Thomson as negatively charged particles of fundamental importance [Thomson 97] [Thomson 99]. Then, after Stoney had suggested the term electron [Stoney 94] in 1894, Richardson presented an approach that quantified the electron emission current. In 1901, Richardson published the results of his experiments: the current from a heated wire seemed to depend exponentially on the temperature of the wire with a mathematical form similar to the Arrhenius equation. The equation was firstly put forward by Arrhenius in order to describe chemical reaction rate, which is dependent on the absolute temperature.

1.2.1.1 Richardson Equation

Later, the thermal emission law had a mathematical form [Richardson 01][Richardson 03]:

$$J = AA^{*}T^{2}exp\left(-\frac{q\emptyset_s}{kT}\right) \qquad \text{Eq 1. 5}$$

In Eq 1.5, J is the emission current density, T is the temperature of the sample, $\emptyset_s$ is the work function of the metal, *k* is the Boltzmann constant, and AA^{*} is the thermal emission constant. Here *A* a universal constant. The mathematical form of A^{*} is presented in Eq 1.6. The $exp\left(-\frac{q\emptyset_s}{kT}\right)$ represents the Maxwell-Boltzmann distribution. The Arrhenius linear plot with $\frac{1}{T}$ as X axis and $\ln(\frac{J}{T^2})$ as Y axis will present the relationship between absolute temperature and thermionic current presented in Figure *1.6*.

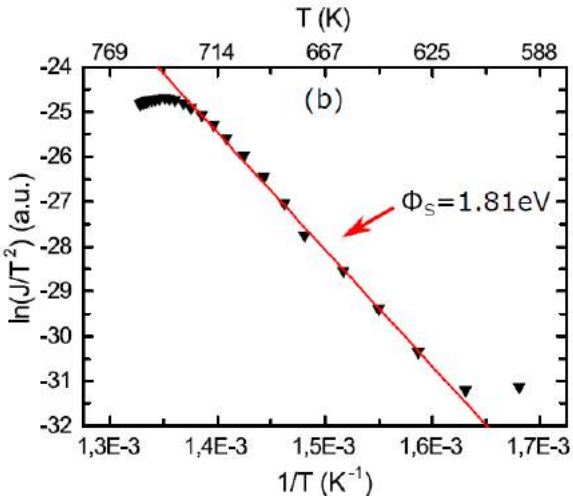

Figure 1.6 Arrhenius linear plot

$$A^{*} = \frac{4\pi mk^{2}e}{h^{3}} = 1.20173 \times 10^{6}\ Am^{-2}K^{-2} \qquad \text{Eq 1. 6}$$

or $$A^{*} = 120\ Acm^{-2}K^{-2} \qquad \text{Eq 1. 7}$$

In these equations, *m* and *e* are the mass and charge of an electron, and *h* is Planck's constant. Eq 1.6 is an approximate theoretical value of Richardson's constant. With the mathematical relation presented by the equation above, the thermoelectric emission was connected to the work function of the emitter cathode. After analyzing experimental data, it was observed that the work function for metals has a linear relationship with temperature.

$$\emptyset = \emptyset_0 + \alpha T \qquad \text{Eq 1. 8}$$

In Eq 1.5 the values of constant α has an order of $10^{-4}eV.K^{-1}$ according to experimental data, and is an order of magnitude smaller with theoretical calculations. [Durakiewica 01][Ibragimow 01]

1.2.1.2 Beginning from 1915, the first proposition by Schlichter

In 1915, with interest in phenomena surrounding glow effect around electrical heated solids, Schlichter studied a process that would "in principle present a possibility to directly convert heat energy to electrical energy as the economical method of such a procedure would be of great technical importance" [Schlichter 15]. In his report, Schlichter described the efficiency of the thermoelectric converter in an equation similar to Carnot efficiency.

$$N_0 = \frac{T_2 - T_1}{T_2} \qquad \text{Eq 1. 9}$$

In Eq 1.6, T_2 is the temperature of the glow-electrode (emitter) and T_1 is the temperature of the counter-electrode (collector). One noticeable thing is that, although the calculated efficiency of thermionic convertor, which is close to Carnot limit, is highly overestimated. In Schlichter first experiment, thermionic energy convertor with platinum electrodes at 1000°C with a reported efficiency of 1.5×10^{-11}. According to the conclusion in his report, the low efficiency magnitude was mainly attributed to radiation losses without addressing the space charge phenomenon. Although the first experimental result is not auspicious, thermionic energy convertor remains to be one of the generator offers maximum efficiency amount all types of energy convertor.

1.2.2 Thermionic development During cold war and thermionic crisis in 1990s (Thermionic Quo Vadis report)

Child and Langmuir firstly described the space charge effect in 1910s. Describing that the saturated thermionic electron emission current building a sufficient electrical field that prevents an electronic charge accumulation adjacent to the emitter boundary [Child 11] [Langmuir 13] [Langmuir 23]. However, in 1955, 40 years after the first proposition by Schlichter, the space charge effect was officially recognized as one of two most limiting factors for Thermionic convertors. In 1958, Hernqvist postulated two key efficiency limitations, including electrode work function difference and inter-electrodes space charge effects presented in Figure *1.7* [Hernqvist 58]. A more detailed discussion of space charge effect can be found in Chapter 3.

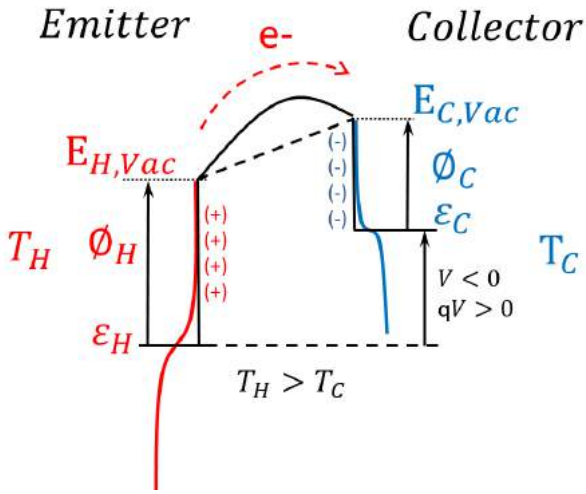

Figure 1.7. Energy diagram of MTC with space charge barrier located in the gap of inter-electrodes.

In order to limit space charge effect, Hernqvist, in his experiment, introduced positive ions, which can be generated through impact ionization for lower cathode temperature of 1200-1500°C in an ignited or arc-mode converter [Hernqvist 63]. In the same year, an ignited cesium converter operating in plasma mode is reported by Hatsopoulos, which lowers the space charge barrier [Hatsopoulos 63]. During the process of investigation of thermionic emission, Hatsopoulos introduced two types of TECs, namely, vacuum TECs(VTECs) and vapor TECs [Hatsopoulos 65].

For vapor TECs, the inter-electrodes space is filled with cesium vapor and space charge effect is neutralized by the positive ions, because cesium is easily ionized. In this case, vapor TECs has a better performance in aspects of implementation and thermal isolation structure design, compared to VTECs.

So early researches were usually focused on the vapor TECs. However, vapor TECs in real case scenarios are facing problems like insufficient positive ions and unfavorable effects of elastic collision in the inter-electrodes space. In one word, due to the limitation of fabrication techniques, most research and development on TECs were focused on vapor TECs in mid to late 20th century.

As we know, electrode work functions are the other main limitations for efficiency of thermionic converters. Efforts to find an alternative method to lower work function were also made in early 20th century. In 1925, Langmuir and Kingdon published a report illustrating the ionization of cesium vapor when a filament is heated to 1200K with a negatively charged cylinder surrounded. The work function of tungsten filament during this process was lowered to 2.69eV, instead of 4.53eV. [Langmuir 25] Further study were also carried out by Wilson in 1966. Thermionic converter with polycrystalline electrode surface and different cesium vapor filling the gap [Wilson 66].

Back to year 1960s, thermionic converters were studied not only for academic research, but also by government and industry. In the early 1960s, U.S. government conducted a program of large-scale thermionic converter focused primarily on solar and nuclear powered systems. While the program failed to produce convincing results and eventually terminated, research on thermionic energy converters were carried on, for example application of laser excitation of cesium atoms for continuous ion generation was also suggested in 1976 by Hansen from NASA [Hanson 76]. Years later, in Soviet Union, two large nuclear reactors equipped with a 5kW power Thermionic energy converter were successfully orbited and operated in space within the TOPAZ program in 1987. This program was abandoned due to budget restriction and political reasons in 1988.

Figure 1.8 Thermionic reactor of TOPAZ II at Kirtland Air Force Base

Then at 1990s, with little advancement of thermionic scientific research and lack of advanced technology and fabrication techniques, the research and development of thermionic converter met a great crisis, which lasted for more than a decade. It became obvious that large scale TEC was a dead-end.

1.2.3 Renewed interest with nanotech and low work function materials on TECs

At the beginning of 21st century, with the great improvement of micro/nanofabrication and material science, the enthusiasm of researching thermionic energy converter is revived. In one way, the study of low work function material has been improved due to massive renovation of micro/nano-fabrication technology, for example Chemical Vapor Deposition (CVD) and nanowire growth. In another way, the second challenge of TECs, to minimize the space charge effect has some break through. Many new methods like using negative electron affinity (NEA) property or incorporate external electric and magnetic fields were proposed recently. Together with the MEMS technology,

which make a closed-spaced micro gap TECs possible to fabricate, TECs as an energy harvester and generator meet its shirley valentine (second wind).

1.3 State of the art

In this section, recent solutions for TECs will be presented in two parts. The first part is focused on work function of electrodes, and the second part is research about minimizing the space charge effect for TECs. These two challenging factors have been the biggest obstacles before the commercialization of TECs.

1.3.1 Limitations of work function and recent solutions

According to thermal emission law by Richardson the work function of the electrodes is one the the most significant factor that affect the efficiency of a TEC. Work function is a parameter of material surface. It defines the amount of energy required for an electron to transit from Fermi level to vacuum level. In other words, it is the minimum amount of energy for an electron to be evaporated from material surface. In the case of a TEC, it is the first barrier for electrons before emitted out of the surface and arrive at inter-electrodes space.

In order to maximize the efficiency of a TEC, both emitter and collector must have a low enough work function. The output voltage and work function of two electrodes will be further discussed in chapter 3.

1.3.1.1 Low work function Materials

Alkali metals, in the field of TECs, are one of the most widely studied materials. They are well known for the low work function characteristics. In early research of 20th century, the alkali metals, especially ionized cesium, were key components for an effective vapor TECs. However, recent research with modern coating technology, alkali metals are regarded as good emitter surface material candidates.

In 2001, work function reduction of platinum was reported by using cesium adsorption method. The work function of platinum dropped from 5.6eV to 1.4eV after the process [Hishinuma 01]. Later, similar cesium adsorption was carried out on semiconductor. And the reduction of work function on silicon was observed [Sinsarp 03].

With the development of advanced coating process, alkaline earth metal can also be deposited on silicon or metal substrate. For example, in one research of thermally isolated low work-function emitter, both barium and barium oxide (BaO) were deposited onto a polycrystalline-silicon carbide substrates, with thin adhesive tungsten layer by Lee's group [Lee 14]. The work function of electrode with barium oxide reached as low as 1.7eV. Similar work function drop was observed on barium coated sample. According to the report, the system with barium oxide was running stable for hours with a temperature of 900-1400K. Other than barium oxide, LaB_6 is a popular material for many types of thermal emission application, which has a work function equals to 2.5eV. The high melting point and low evaporation rate at high temperature makes LaB_6 the best for cathodes in applications like SEM, microwave tubes, electron lithography, electron beam welding, X-ray tubes and so on.

With chemical vapor deposition method, our group has tested different alkali metal film coating techniques, including potassium and cesium. A significant drop was observed on hydrogen-passivated (100) p-type silicon substrate. For silicon substrate with potassium oxide film, the work function dropped from 4.7eV to 1.35eV. For cesium oxide film, the final work function dropped to 1.66eV [Morini 14] [Giorgis 16]. Details about the coating technique, operation and measurement will be presented in Chapter 2.

Not only alkali metal and alkaline earth metal are good candidates for a low work function emitter, diamond film and graphene-based TEC were able to reach a high efficiency. An extremely low work function of 0.9eV was acquired with phosphorus-doped polycrystalline diamond films on metallic substrate. The film was reported stable at sustained temperature of 765°C [Koeck 09]. Moreover, for nitrogen-incorporated, ridged nano diamond films on silicon substrates can achieve a work function of 1.39eV and can sustain a temperature of up to at least 900°C [Paxton 10].

1.3.1.2 Nano structure methods to lower work function

Surface nanostructure is one new method to lower the work function. The newly named field electron emission is an example. In this case, electrons emission is enhanced by a field-effect named electrostatic field. It is normally referred as cold emission, as it occurs at lower temperature compared to planar emitter TECs. A study carried out by Pan and his group producing aligned SiC nanowires (SiCNWs) on stainless steel substrates [Pan 00]. The structure proved to feature a superior field enhancement factor for thermionic emission for given materials and conditions.

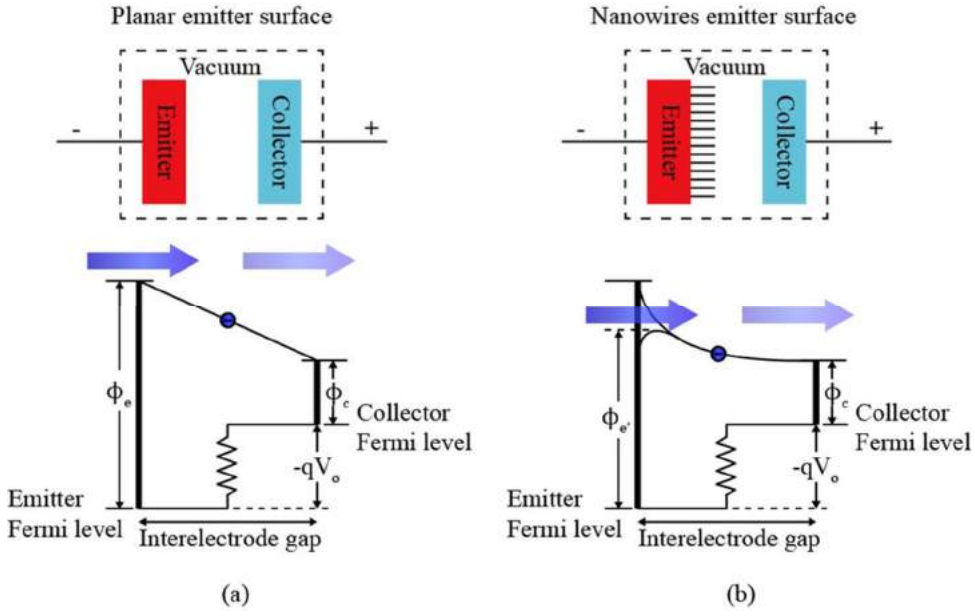

Figure 1.9 Schematic energy diagram of two types of electron emission TEC from (a) planar emitter surface and (b) nanowires emitter surface. [Smith 06] [Kamarul 16]

Figure *1.9* presents two energy diagrams, comparing electron emission from different surfaces. Experimental results prove that the nano-tips make electrons arrive at vacuum level at lower energy cost. This is due to Schottky barrier lowering [Smith 06]. Multiple publications have announced that SiCNWs are compatible with microfabrication techniques, feature good thermal and chemical stability and are thus excellent candidates for high-temperature MEMS devices. The field-enhanced TEC with SiCNWs seems to be another promising solution.

In 2007, Xi and his group reported an experiment, which combines both field emission and BaO/SrO coating for a TEC device. In the experiment, a thin barium strontium oxide uniform coating was successfully deposited on the surfaces of vertically aligned CNTs grown on tungsten ribbons. Although the field enhancement factor was not optimal due to the diameters of nano-tips, the work function of emitter was reduced to 1.9eV with a field enhancement factor of 467 [Jin 07].

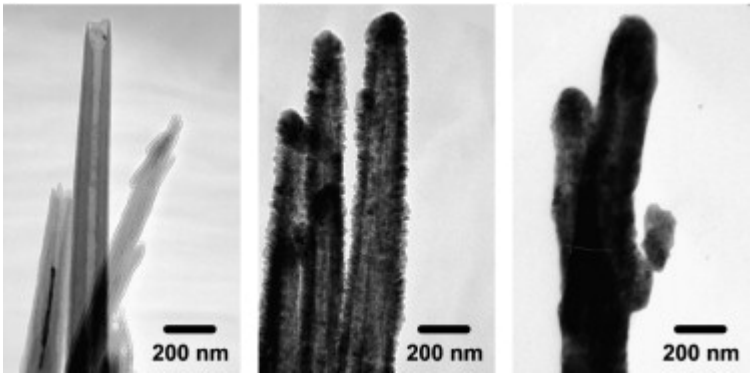

Figure 1.10 (a) TEM image of CNTs before coating. (b) 50 nm coated CNTs. (c) 100 nm barium strontium oxide coated CNTs.

Later, a thermal-assisted electric field was demonstrated and field emission device was fabricated by Cui and his group with barium oxide coating on CNTs [Cui 17]. The calculated results of BaO emitter work function dropped from 1.44eV at room temperature to 0.96eV at 593K.

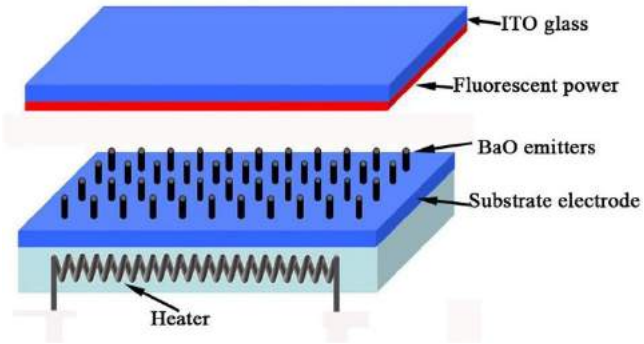

Figure 1.11 Scheme of thermally-assisted field emitter [Cui 17].

Recent research confirms that the thermionic emission current acquired from individual hot CNTs is not following the Richardson-Dushman law [Wei 14] [Wei 10]. Wei and his group claimed that during *in situ* multi-probe measurement, the measured electron emission density is more than one order of magnitude higher than prediction by Richardson's law. In the same time, the Arrhenius plot were found to exhibit an upward bending feature instead of straight lines.

1.3.1.3 Intercalation

Intercalation is a chemistry process where guest molecules or ions are inserted or included into materials with layered structures. The host materials usually has a layered structure like carbon or graphite. Intercalation expands the Van der Walls gap between layers, which needs energy. This energy is supplied by charge transfer in between the host and the guest.

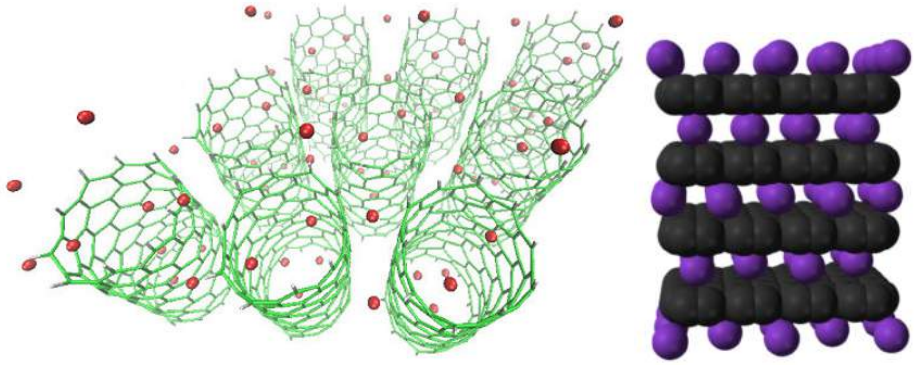

Figure 1.12 (a) Model of intercalation of potassium into single-wall CNTs (b) Model of intercalation of potassium into graphite

Figure *1.12* present two intercalation models with famous intercalation host, the carbon nanotube and graphite. Carbon nanotube (CNT) is another promising nanomaterial. Due to its excellent electrical conductivity and thermal stability. A research by Westover and his group showed that the intercalation of potassium into single-wall and multiwall CNTs resulted in the work function of 2eV for both application [Westover 10]. The work function of pristine CNTs, which has similar value as graphite, is usually about 4-5eV [Ago 99] [Sun 02]. The reduction of work function by intercalation with potassium metal atoms is significant.

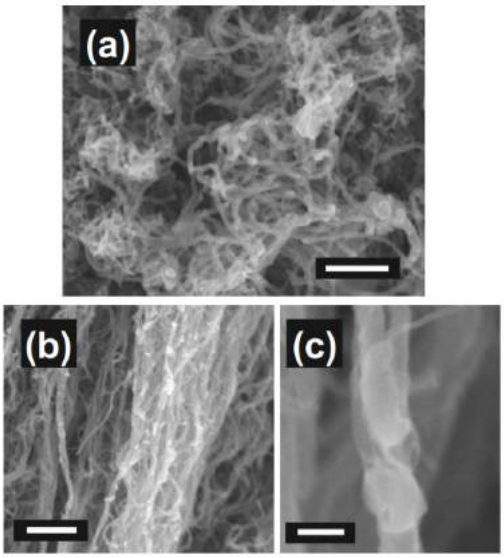

Figure 1.13 FESEM images of K/MWCNTs, showing metal, presumable potassium, inside individual MWCNTs. Scale bars are 500 nm, 1 µm and 100 nm, in (a) (b) and (c), respectively. [Westover 10]

Similar experiment has been tested on different types of graphitic carbon nanofibers (GCNFs). The direct reaction of GCNFs with molten potassium gives potassium/graphitic carbon nanofiber (K/GCNF) intercalates a stoichiometry-controlled potassium loading. Thermionic emission is observed on stage-1 (C_8K; 29 wt% K) K/narrow tubular GCNF intercalate at 300°C. The stage-1 K/herringbone GCNF displayed a work function of 2.2eV and remained thermally stable at the temperatures of up to 1000°C. Compared to the work function of carbon nanotubes, which is about 4.6eV minimum that depends on parameters optimization, a reduction of 2.4eV is achieved. [Michel 08].

1.3.1.4 Photo-enhanced TEC and PETE

Another alternative method to enhance the evaporation of hot electrons is known as Photon-Enhanced Thermionic Emission (PETE). An additional conduction band carrier population created by photoexcitation can enable this new type of electron emission process. PETE, in case of p-type materials, combines photovoltaic and thermionic effects into a single physical process, which takes advantage of both the high per-quanta energy of photons and the available thermal energy due to thermalization and absorption losses [Schwede 10].

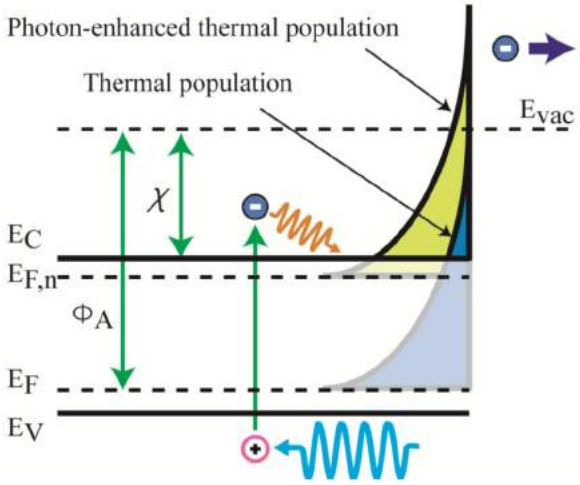

Figure 1.14 Energy diagram of PETE process. Photon-generated electrons increase the conduction-band population, leading to effective work-function decrement and enabling the device to harvest both photon and heat energy. [Lee 14]

The scheme of the PETE process presented in Figure *1.14* consists in three stages. First, electrons in valence band E_V are excited by photons into the conduction band E_C. Second, they rapidly thermalize within the conduction band and diffuse throughout the emitter. Finally, electrons that reach the surface with energies greater than the electron affinity can emit into the vacuum. The PETE process is advantageous especially for p-type emitters compared to thermionic emission from n-type materials due to the larger output voltage. It results that in p-type semiconductors Fermi level is near to valence band and away from conduction band. With the theoretical model of PETE above, a conversion module was fabricated for serving Concentrated Solar Power (CSP) applications and patented in 2012 [Trucchi 15]. This module named ST^2G is a solar thermionic-thermoelectric generator. By involving both thermionic and thermoelectric conversion stages and connected thermally in series, the calculated overall conversion efficiency was claimed to be up to 30% or greater. Although PETE is firstly discovered in a study of concentrated solar power applications [Schwede 10] and is still intensively studied in solar cell utilization to allow electrons carry both the photon energy and the thermal energy. It is considered as an essential improvement in TEC research.

1.3.2 Research and recent solutions for space charge reduction

Space charge effect is a important phenomenon for thermionic emission. The evaporated electrons filling a vacuum space and resulting in a negatively charged cloud and an electric current passing through the vacuum. The first assumption is that the distribution of electrons is even. Then according to Poisson equation, we have:

$$\nabla^2\Psi = -\frac{\rho}{\epsilon_0} \qquad \text{Eq 1. 10}$$

$\epsilon_0$is dielectric constant of vacuum, Ψ is the energy barrier of space charge effect. If ρ is constant (even distribution), Ψ is a parabola. However, due to the fact that thermionic current $\vec{J} = ne\vec{V}$ does not depend on position, while the kinetic energy of electrons change according to the position due to the existence of electoral barrier. So the even distribution assumption is wrong. So, the Poisson equation can be written as:

$$\frac{\partial^2\Psi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_0} \qquad \text{Eq 1. 11}$$

The result of calculation tells that the barrier of space charge effect is a curve shorter and flatter than a parabola.

Since last century, several approaches have been proposed to mitigate the space charge effect. One of the most studied method is vapor TEC. By inserting positively charged ions into the inter-electrodes space, we can neutralize the negative charge created by thermionic current. Unfortunately, this method has drawbacks and been proved less effective in 20th century.

1.3.2.1 Negative electron affinity (NEA)

Negative electron affinity is one other way to avoid the limitation of space charge effect. By using a hydrogen-terminated diamond material with negative electron affinity property [Smith 07], the vacuum level below the conduction band was lowered. This is the alternative way to interact with negative charged thermionic electrodes other than positively charged ions in vapor TEC. Similar to PETEs, electrons in this case receive sufficient energy to be promoted to the conduction band and can escape the surface as the vacuum level is already been lowered below the conduction band by NEA.

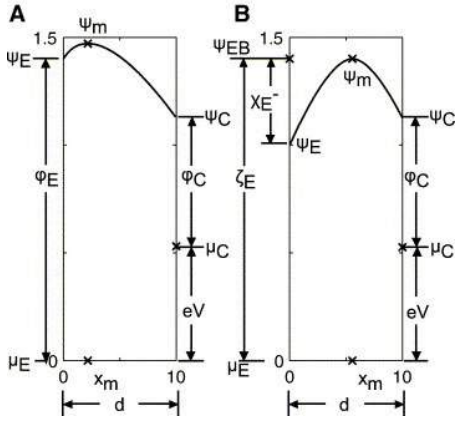

Figure 1.15 (a) Energy diagram of a TEC with conventional emitter operating in the space charge limited model. (b) Energy diagram of a TEC with an NEA emitter operating at the virtual saturation point. Both devices are operating at the same temperatures, has same emitter and collector barrier heights and the same gap dimension with the same output voltage. [Smith 06]

The calculation results are presented in Figure *1.15*, the value and position symbols are defined as follows: the *d* is inter-electrodes dimension, ψ_m and x_m are the value and location of the maximum barrier. For the collector parts, symbols are same with μ_C, φ_C, ψ_C representing the Fermi level, work function and vacuum level, eV is the defined output voltage. For the emitter parts, in conventional emitter symbols are similar with subscripts changed from C to E. In Figure *1.15* (b) for an NEA emitter,

χ_{E-} is the value of NEA, ψ_{EB} is conduction band level *and* ζ_E is the emitter barrier height. By comparing the barrier height between Figure *1.15(a)* and Figure *1.15(b)*, we find that the ψ_m in Figure *1.15(b)* is lower. Due to the lowered vacuum level below the conduction band, every emitted electron has a minimum kinetic energy χ, which is the energy band gap between bottom of conduction band and vacuum level. Comparing to the no NEA emitter, the low kinetic energy electrons are eliminated and consequently the space charge barrier is lowered and the maximum shifted towards collector, as presented in Figure *1.15*. Thanks to the lowered boundary condition at the emitter, the NEA device can outperform the Langmuir device, and in certain sets of parameters it can make a TEC to avoid the space charge limited mode and perform equivalent to an ideal device. [Smith 06]

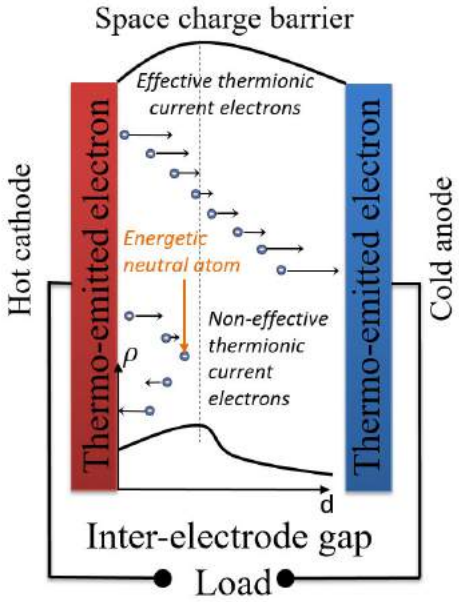

Figure 1.16 Effective thermionic current electron, which arrives at collector and non-effective electron that returns to emission surface. The arrows present the speed and direction of electron movement. Vertical dotted line is the peak position of space charge barrier. The black curve with axes presents the electron density distribution in the inter-electrode gap.

Another benefit of NEA property in case of TECs is that it can be further exploited to filter electrons with possibly lower kinetic energy. The Interstellar Boundary Explorer (IBEX), as an example, is a satellite that detects energetic neutral atoms in space. This filter can minimize the total electrons stay in the gap in given moment and guarantee that most of electrons in the gap are effective thermionic current. This method is promising, because most of space charge barrier is heavily built up by those electrons without enough energy and cannot overcome space charge effect. These low energy thermionic electrons are distributed in between emitter and peak position of space charge barrier, which is presented in Figure *1.16*. If this population of electrons can be filtered from the source, the space charge barrier can be reduced significantly. A calculation has proved that by increasing the value of the NEA, the output current characteristic will approach the ideal mode of TEC, where TEC is not affected by space charge effect [Smith 06].

1.3.2.2 Micro Thermionic electric convertor structure

Due to the limitation of fabrication process in mid-20th century, the closely-spaced TECs failed successful fabrication process and promising results. It has been abandoned as practical devices since the 1960s. However, the method of limiting space charge effect by reducing the inter-electrode space

has revived in the recent years due to advance micro-fabrication processes including photolithography, plasma etching, CVDs etc. The early attempts of micro-gap thermionic converter are reported by Fitzpatrick in 1996. The theory of limiting space charge effect by micro gap is simple and straightforward. The micro dimensioned inter-electrode gap is so small that no space for the travelling electrons to accumulate and build up the anti-emission barrier. The thermionic electrons can reach the collector in short amount of time, which consequently not many electrons stay in the gap in the same moment. Up to now, the micro-gap TEC is one of the most direct and efficient way to eliminate the challenging problem of space charge effect.

Fitzpatrick and his group have managed to control the spacing between the electrodes with a gap spacing of less than $10\mu m$ [Fitzpatrick 96]. Although, problems of near field radiative heat transfer lead to a thermal energy loss and it is hard to build-up high temperature difference within small vacuum gaps if the gap is too narrow [Gerstenmaier 07] [Lee 12]. The Micro-gap Thermionic energy Convertor (MTC) seems to be promising with numerous advantages. For example: MTC has simple structure especially with existing compatible MEMS technology; easy adaption to different low work function materials and corresponding coating processes. In this report, presentation will focus on our efforts in different aspects made for MTC in the frame of ERC project.

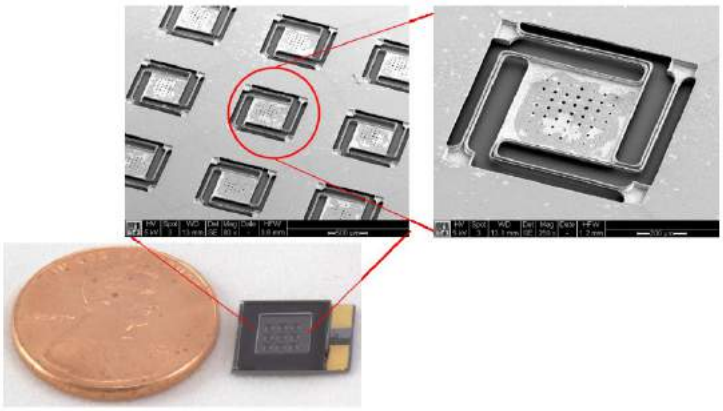

Figure 1.17 Encapsulated die with 3×3 array of TECs. One cent of dollar is shown to indicate scale of whole encapsulation. The inset shows a scanning electron micrograph (45°) of one single TEC element. [Lee 14]

1.3.2.3 Integration of electric and magnetic fields

More work has been made to solve space charge effect for TECs. Another recently announced approach is incorporate TEC with external electric and magnetic fields. The initial idea was reported by Hatsopoulos in 1973 [Hatsopoulos 73]. Two triode TEC configurations were introduced with the propose of both minimizing the space charge and managing the heat transfer between the emitter and the collector.

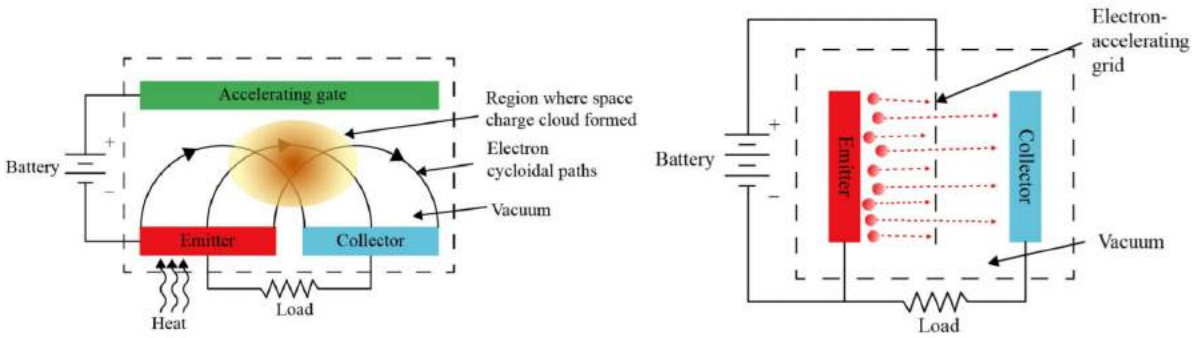

Figure 1.18 Two schematic structure of Hatsopoulos [Hatsopoulos 73] [Kamarul 16]. (a) Magnetic triode TEC, (b) Schematic of an electrostatic triode TEC.

Figure *1.18*(a) is the magnetic triode TEC, with both emitter and collector positioned in a line, the thermionic electrons leave the hot surface and in the help of accelerating gate magnetic field go along a cycloidal paths. The acceleration of these electrons removes them from the originally concentrated area, which implies the suppression of the space charge cloud. Figure *1.18*(b) presents the second configuration, which is an electrostatic triode TEC. In this configuration, electron acceleration grid is placed between the electrodes to accelerate electrons away from the emitter and overcome the peak barrier position. Both of these two schemes were unsuccessful at that time and have the same problem. Most of thermionic electrons will end up in hitting the acceleration gate or positively charged grid, which leads to efficiency loss named leakage current.

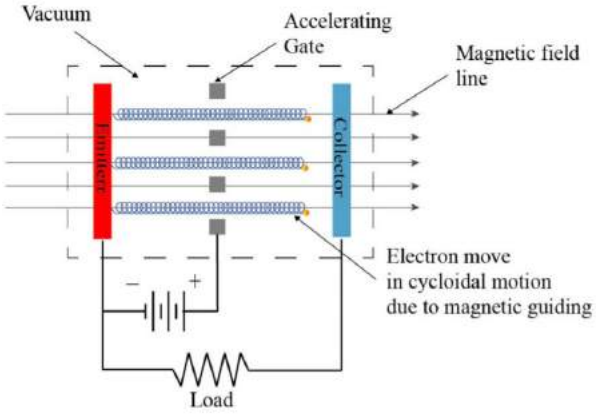

Figure 1.19 schematic of combined magnetic and electrostatic triode TEC. [Meir 13]

Recently a configuration of combining the vacuum magnetic and the electrostatic triode concept has been proposed to eliminate the space charge effect [Meir 13]. Presented in Figure *1.19*, the concept has similar structure as electrostatic triode TEC, and an external magnetic field is applied to keep the electrons from hitting the accelerating gate. A large pair of neodymium magnets was used to force the electron radius of gyration to be smaller than the openings of the gate mesh, so that these electrons could pass through the gate and reach the collector.

Other than the configuration above for vacuum TECs, triode configuration has been studied to reduce the space charge effect in Vapor TECs. A thermionic triode was designed with an auxiliary discharge in a longitudinal magnetic field. This configuration helps separate cesium ions from other thermal electrons using the magnetic field. The second design is neutralized space charge by Cs ions injected from the grid and this grid wires are located between the electrodes [Moyzhes 05].

1.4 Approaches in the frame of the UPTEG project

This UPTEG project is funded by European Research Council. With a simple review about state of art previously, this section is a brief presentation of in which aspect have we made efforts to develop a better micro-gap TEC (MTC). This includes exploration and technique development for a lower work function material based on alkali metal oxide. Analyze the TEC characterization as an energy supplier. Calculations and simulations for a better structure for greater temperature difference. Layout design and experimental design, including integration of the TEC device into exist vacuum platform. Fabrication by available nano/micro-fabrication techniques and I-V characterization in high temperature and high vacuum environment.

1.4.1 Low-work function material candidates

Alkali metals and alkaline metal oxides have the property of low electron binding energy, which have the best potential to reach a lower work function. The work function values of these materials has been proved by both experimental measurement and theoretical calculation, which have the lowest values amount all detected elements. Figure *1.20* presents the work function of these coating candidates with the results of accepted experiment values and calculated values.

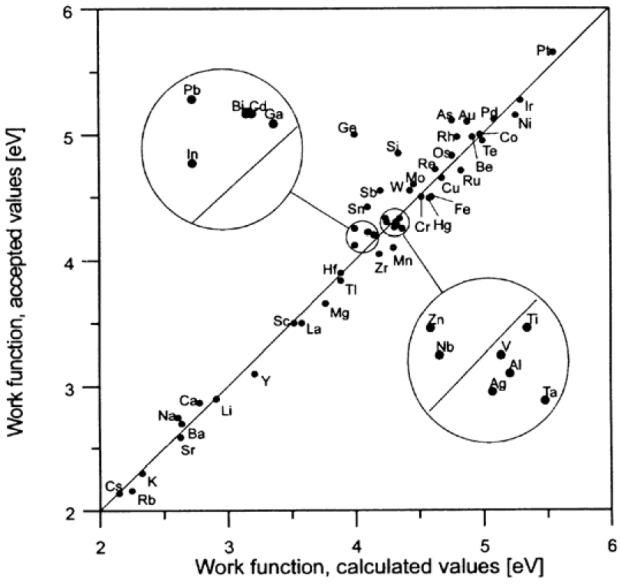

Figure 1.20 Measured work function values vs. calculated by the metallic plasma model proposed by Halas and Durakiewicz [Halas 98], which is a method improved from Brodis's novel approach using ab-initio methods.

Early in 1908, 17 oxides were reported with experimental work function within the range of 2.0 to 4.4eV, in which the lower end of the range is surprisingly low. However, over the entire 20th century, no sound explanation of the low values was proposed for oxides. Despite this, nowadays, the lowering of work function with alkaline oxides and alkali oxides has a great significance in production of negative ions in numerous domains, including spectrometry, catalysis, microelectronics and so on [Wachsmann 91] [Broqvist 04]. One theoretical discussion for alkali and alkaline metal oxide emitter has a lower energy is due to the decrease of the free electron density in the surface layer of oxidized metal [Halas 06]. The second reason lead to a lower work function is the oxides may has larger disorder in the activated layer, which results in larger spacing between atoms on the oxide-vacuum interface.

With experimental data taken from Handbook of thermionic properties, we have a comparison between work function of pure metals and their oxides. From *Table 1.2*, we find that the alkali and alkaline earth metal oxide has lower work function than the pure metal of same element.

Metal	φ (eV)	Oxide	φ (eV)
Li	2.35	Li_2O, Li_2O_2 etc.	Not found
Na	2.28	Na_2O,Na_2O_2 etc.	Not found
K	2.29	K_2O, K_2O_2 etc.	1.54-1.89
Rb	2.26	Rb_2O, Rb_2O_2, Rb_2O_3	Not found
Cs	1.95	Cs_2O, Cs_2O_2	0.99-1.17 [Fomenko 66] 1.33 [Morini 14]
Ca	1.97	CaO	1.7-1.9
Sr	2.15	SrO	1.4-1.6
Ba	2.17	BaO	1.4-1.7

Table 1.2 Work function of pure metal and their oxides (experimental data) [Fomenko 96], work function may change according to different pre-measurement process.

Material	Coating/Doping	Related principle	φ (eV)
Platinum	Cesium	Adsorption	1.4
Metallic	P-doped polycrystalline diamond	Diamond coating	0.9
Stainless steel	SiC nanowires	Nanostructure emitter	1.9
Carbon nanotubes (CNTs)	Barium oxide	Coating on nanostructure	0.96
Single-wall and multiwall CNTs	Potassium	Intercalation	2.0
Graphitic carbon nanofibers	Potassium	intercalation	2.2

Table 1.3 Materials and related technology for lowing the work function of TEC emitters. All the principles are illustrated in section 1.3 of this chapter.

After analyzing the material accessibility and recently developed technology, which presented in *Table 1.3*, the coating element candidates for thermionic emitter in our project is potassium and cesium.

1.4.2 inspiring structure designs lead to our conception

Before the conception of MTC, looking back to recent models and designs is always beneficial. The following two recent models represent two different thoughts in key aspects including structure mechanical support, thermal isolation method and surface coating process. In chapter 3, conception and FEM simulation of a new structure will be presented, which is a better developed design inspired by these following models.

1.4.2.1 U-shape membrane design by Berkeley University

One of the most accomplished designed Micro-gap Thermionic Converter was proposed by Jae Hyung Lee from Berkeley University [Lee 13]. It is a sound technical design from layout to vacuum encapsulation. The suspension arm had a width of 10-30μm, the sidewall height was 30μm and the poly-SiC film was 2μm thick. The etch holes were used in the emitter plate to etch the cavity and suspend the membrane. The distance between suspended SiC membrane and the bottom substrate is

about 10µm. The device was firstly fabricated using 4-inch SOI wafer (40µm device layer, 4µm BOX). Then, since the bonding between the SiC layer and the pyrex glass was not reliable for vacuum bonding, the modified fabrication process was based on SOSOI wafers.

During the stand-alone TEC heating experiment, the Photon-Enhanced Thermionic Emission (PETE) device had a thermionic current was about 280nA when the incident power was about 150nW at zero bias between the emitter and the collector.

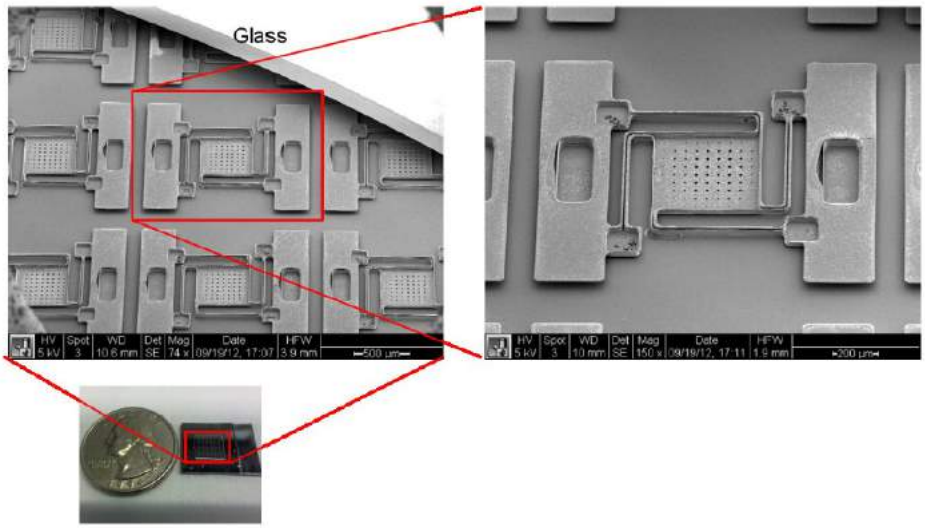

Figure 1.21 Vacuum-encapsulated devise with an array of TECs. A quarter is shown to indicate scale with a SEM image of one single U-shaped TEC element is shown. [Lee 13]

From Figure *1.21,* the suspended projection takes a square shape area of about $900\mu m \times 900\mu m$, and MTC emitter surface is about $500\mu m \times 500\mu m$ ignoring the surface of holes. The effective surface ratio is about 30.1%. The advantage of the U-shape TEC design is with long suspension arms thermal conduction can be limited by the slender and long U-shape arms. The thermal stress is also well managed in this design. However, with emitter on the top side, the only heating method is by laser or light. So, it is usable with concentrated solar beam. In other words, the PETE device is not designed for other heat energy source. With the active area limited it may not suitable for massive industrial fabrication and commercial usage.

1.4.2.2 Emitter and collector stack structure by Tohoku University

One more recent MTC structure was proposed by Remi Yacine Belbachir from Tohoku University [Belbachir 14]. SiC emitter and Pt Collector were stacked on each other with a micro-size gap. The stacked thermionic power generator was placed on a Cu heat sink with the collector side down, which was continuously cooled by water. The SiC emitter was placed under a quartz glass and remotely heated by a lamp heater. The system was placed in side a vacuum chamber where Cs was evaporated using a heating filament. With SiC emitter and Cs evaporation filling inside the vacuum gap, the MTC reached an output power density of 11.5mW/cm^2 has been observed at 830°C. The quantitative thermal loss measurement on the same system proves that in this work, a power conversion efficiency of 3.9×10^{-5} has been obtained.

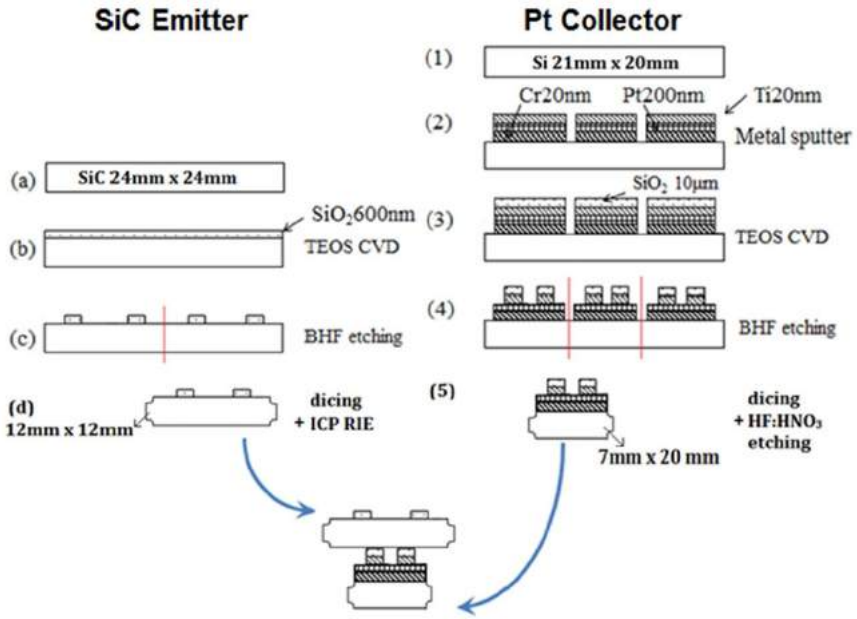

Figure 1.22 Emitter and collector process chart. The emitter and collector surface dimension are indicated and the inter-electrodes gap distance was fixed at about 10μm. [Belbachir 14]

The square section shape SiO_2 has a dimension of $700\mu m \times 700\mu m$ with pillar height of 10μm. On one single $7mm \times 20mm$ collector, there are 56 SiO_2 columns spread in four rows of 14 SiO_2 columns each. The effective surface ratio counting from the collector side is about 80.4%. The surface-pillar structure has much higher effective surface compared to the membrane-arm structure designed for PETE device from Berkeley University. However, as has been reported, it has a value of 2.4K/W thermal resistance which confirming the predominance of the conduction heat loss from the emitter to the collector.

1.4.2.3 Expectation and technical indicators for our design

Learning from recent MTC structures, the goal of prototyping is an efficient MTC compatible with mass production processes and various heat sources. The solution we proposed managed to combine advantages of the two previous models. The structure scheme will be presented in chapter 3. By using pillar support the emitter surface can easily be enlarged and can receive thermal energy from different heat sources. This is a great advantage compared to Belbachir's design. With the vapor etching process and SOI wafer as initial material, the pillar size can be controlled accordingly by distribution of etching holes. This is an advantage from Lee's U-shape micro TEC. However, if the design can real benefit the innovative design remain to be tested.

In chapter 3, before the presenting the fabrication of the prototype, several finite element modelling and numerical simulations will be presented focusing on the thermal conductivity and thermal resistivity of the MTC structures. Hoping that after the simulation, improvement about thermal performance for MTC will lead to a satisfying result. The goal is to establish a temperature difference of 100K in between emitter and collector with the emitter at relatively low temperature, which is about 700K to 1000K.

1.4.3 Proof of concept under vacuum

Facing two main challenges in front of thermionic energy convertors, the work function and space charge effect, the solutions in the frame of this UPTEG project are presented in the previous section of this chapter. So what is the benefit and advantages of these technical routes compared to the state-of-the-art. First, to get a low work function electrode, the silicon substrate is one of the most technical compatible material with modern microelectronics manufacturing process, no matter in laboratory or in factory. Also, it is a simple and direct method to get desirable work function values. What's more, the conductivity of silicon can be easily controlled, while nanostructure materials and intercalation structure solutions may result in low conductivity emitters. The nanowire emitter surface, which will drop the work function, however, will increase the space charge concentrated at the nanowire tip or nanotube top. The current density of nanostructure emitter is lower than planar emitter, due to the effective surface is only located on the tip top not all emitter. A profitable tradeoff between low work function but lower effective area remains unknown. To avoid the impact of space charging, the micro gap thermionic energy convertor is the best choice according to engineering feasibility. The concept of magnetic triode TEC, magnetic field or electron accelerating are attractive and outstanding. However, the amount of pre-development work is enormous to build only a prototype. In addition, the complicated structure is unfriendly to commercial usage, even if a prototype can be successfully developed.

In one word, by using micro gap TEC structure, space charge effect can be eliminated; by use of alkali metal oxides coating through CVD or ALD technique, work function of electrodes can be minimized. Both of these two methods are reported as possible solutions in order to meet the need of a working TEC.

1.4.4 Encapsulation of Micro Thermionic electric convertor

In the field of semiconductor fabrication package is one of the most essential step during the whole process. The plan of MTC prototype packaging is using the technology of wafer-level gold thermos-compression vacuum bonding [Tsau 2003].

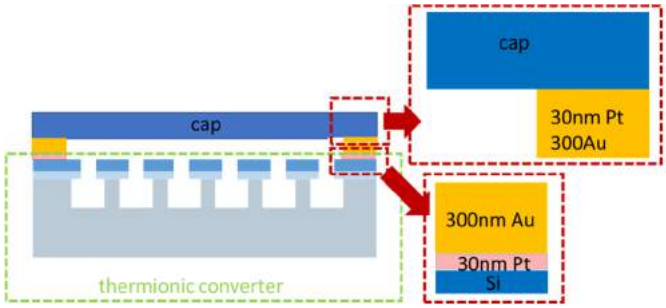

Figure 1.23 Schematic image of the thermionic converter after encapsulation

Thanks to the contribution of ZHOU Di, post-doctoral fellow for this project, a vacuum capsulation process was developed and tested on silicon wafer, which makes the vacuum package of MTC device possible. Also, it can be an alternative design as a radiator on the collector which may be a necessary approach to build up a temperature.

Figure *1.23* presents the section view after a wafer-level bonding for package. The Platinum was used as an adhesive layer in-between gold and silicon surface, while the thicker Au thin film operates as

bonding material to bond two silicon substrates. The whole bonding process will be processed in a vacuum chamber and the square shape bonding contacts will be able to keep the vacuum environment inside the capsulation and maintain micro sided vacuum gap. Further detail will be presented in chapter 4 with all designs layout and photos.

1.5 Chapter summary

Thermal engines which convert energy from heat to electricity directly is a topic that interests many researchers. These types of energy harvester/generator have great potential due to the massive available and easy access thermal resource. The principle of TEC is thermionic effect also known as the Edison effect, which has been studied from early last century. Without any moving parts, the early TEC was designed to be an electrical generator for extra-long duration. Limitation of technology in many aspects lead to a failure when facing various problems like build a micrometer structure, create a high temperature gradient in a high temperature range, etc. Luckily, the field of thermionic research remains to be a vivid topic for scientists. With recent semi-conductor fabrication process and low work function material coating methods makes TEC possible to work in a temperature not that high and close to room temperature (from 300K to 1000K). For the same reason, many possible advance structure of TECs has been proposed with careful design and firm theory support. The renewed interest of the field of TECs will probably bring a stable and efficient TEC out of lab and into the industry world.

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Chapter 2 Low Work Function Material Coating and Characterization

With knowledge of the operation of a MTC, a highly efficient emitting material integrated at the surface of electrodes is really needed. The first section will be a simple introduction for work function. Because the work function is not a characteristic of a bulk material but rather a property the surface [Halas 10], what the MTCs really need is a film from several atoms thickness or at most several nanometers. This chapter will then present the research work and development of a system with sound workflow to achieve low work function film deposition and characterization. One of the highlights is to match the work function results of different measurement principles of one single sample with each other. This matching process increases the reliability and repeatability of measurement and can help to avoid the influence of Kelvin Probe surface pollution due to chemical vapor deposition in the same chamber.

Particularly, we analyse and compare the performances of two alkali metal oxides: Potassium oxides (K_xO_y) and Cesium oxides (Cs_xO_y). These compounds feature a very low work function lower than 1 eV which are even better than alkali like potassium metal and cesium metal. These elements are also abundant and not hazardous in experimental conditions. In our workflow these alkali materials were firstly deposited on highly-doped silicon surface to form a thin film. The oxide thin films were characterized by Kelvin Probe, photoemission and thermionic emission measurements. Then X-ray photoelectron spectroscopy and energy-dispersive X-ray spectroscopy were also tested. All the results on the synthesis of these thin films were obtained under high vacuum and controlled temperature.

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2.2.3 In chamber Characterization

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2.2.4 External chamber characterization

2.1 Introduction

I mentioned in the first chapter that the work function and space charge effect are two main challenges faced by every thermionic energy converter researcher. The chapter 2 will present our approaches to develop low work function materials and the corresponded coating techniques.

This first section will present the study on the nature of the work function. At early 20th century, thanks to the research carried out by Einstein, Richardson, Jentzsch, Debye, Schottky and Langmuir, work function was assumed to be a force, which is the main reason for the barrier at the metal surface. Some early theoretical equation is still used for calculation these days. Then at the end of 20th century the image potential as the main contribution to work function was restored by Brodie then improved by Halas and Durakiewicz with the development of surface physics. In these new theories a distance d from which the image force can be integrated is found from the uncertainty principle and from the length of spontaneous metallic plasma polarization, respectively.

2.1.1 The term of "work function"

Definition and propriety of work function was firstly used in 1923 as an expression in eV describing the necessary energy to get electron out of metal [Dushman 23]. In the past decades, with the development of high vacuum technology and stable metal thin film industrial production technology, work function as a fundamental property of a surface has been examined for most of all elements and many conducting compounds or alloys [Halas 06] [Michaelson 77].

The interpretation of work function defined from photoelectric effect is by Albert Einstein. In 1905, 26 years old Einstein wrote five papers, which changed the foundations of physics and understanding of the Universe. In his paper, trying to deal with radiation and energy properties of light, several phenomena were considered, including photoluminescence, photoelectric effect and gas ionization by ultraviolet light.

At that time, with photoelectric effect already investigated experimentally by Lenard in 1902, Einstein considers this effect as generation of electrons from a cathode by irradiation by light quanta. He assumed that "*every electron leaving a solid has to lose a characteristic work P"*. With Planck's quanta as particles of energy, the first latterly introduces equation $\mathrm{E} = \mathrm{h}\nu$ submitted by Millikan. Therefore, the kinetic energy of leaving electrons is:

$$\frac{1}{2}mv^2 = h\nu - P \qquad \text{Eq 2. 1}$$

From this equation Millikan defined a much more accurate Planck constant than before, which is calculate from the Planck radiation law.

In the last phenomena of gas ionization by ultraviolet light, Einstein introduces the work for ionization of one mole of a gas, $\mathcal{I}$ and later we have the equation:

$$h\nu \cdot N \geq \mathcal{I} \qquad \text{Eq 2. 2}$$

The estimated average ionization energy of air molecules is in fairly good agreement with that determined by mass spectrometry the appearance potential of $O_2{}^+$,$(12.3 \pm 0.3\ \mathrm{V})$. In this study the introduced quanta can be converted to other quanta and can do real work. He defined *works* which later on were called as work function and ionization energy.

Apart from photoelectric effect and ionization, in early years, work function was also defined from thermionic emission in the paper "*on negative radiation from hot platinum*" by Richardson. Starting from the Maxwell-Boltzmann distribution of electron velocity, he found the following law for the saturation current density, which is a value that can be measured from the experiment.

$$j_s = ne\sqrt{\frac{kT}{2\pi m}}\, e^{-\varphi/kT} \qquad \text{Eq 2. 3}$$

Here, Φ is defined as "the work done by a corpuscle in passing through the surface layer", T is the absolute temperature, k is Boltzmann constant, n is the total number of corpuscles per unit volume and m is thier mass. From his law, Richardson could determine both Φ and n for platinum. Then he interprets Φ/e as the discontinuity in the potential at the surface of the metal. Unfortunately, Richardson did not explain the origin of this electric barrier. And not until three decades later, when Max Born using the Fermi-Dirac distribution, the thermionic emission current has its modern look [Born 63].

$$j_s = \frac{4\pi emk^2}{h^3}\, T^2 e^{-\varphi/kT} \qquad \text{Eq 2. 4}$$

Here, the universal constant $\frac{4\pi emk^2}{h^3} = 120A \cdot cm^{-2} \cdot K^{-1}$ is defined by physical constants.

In the history, other than photoelectric effect, ionization and thermionic emission, work functions were studied experimentally and theoretically in some other phenomena where it plays an important role. These phenomena including Schottky effect, semiconductor doping, electronegativity, electric dipole moment and metal surface adsorption.

2.1.2 Work function and Properties

In solid-state physics, the work function is the minimum thermodynamic work needed to remove an electron from a solid to a point in the vacuum immediately outside the solid surface. Or, in other words, it is the minimum energy required to extract the electrons from one electrostatic forces equilibrium position to a given position with potential V_0, when V_0 is one for which the kinetic energy of the electrons is zero.

2.1.2.1 Relation between Fermi level and Vacuum level

The analytical definition of work function is based on the theory of Selon Wigner and Bardeen [Wigner 35]. The work function of is the energy difference between an electrically neutral crystal and a crystal to which an electron has been extracted. Although it is an analytical description, the definition is true only when it is absolute zero and in perfect vacuum condition. So this definition is not very exploitable in experimental situation. Alternatively, the work function is defined as the energy needed for extract an electron from Fermi level to Vacuum level. In this case, the expression can be written:

$$\emptyset = E_0 - E_F \qquad \text{Eq 2. 5}$$

Or, in other presentation:

$$\emptyset = \mathrm{q}V_\mathrm{e} - E_F \qquad \text{Eq 2. 6}$$

This is the only operational definition for experimental measurement. Energy diagram presenting this work function definition can be found in Figure *1.13* and Figure *2.1* below. In the case of intrinsic semiconductor, Fermi level located at almost the middle of energy gap in-between valence band and

conduction band with $E_F = E_i$. This is due to the number of electrons in the conduction band is equal to the number of holes in the valence band.

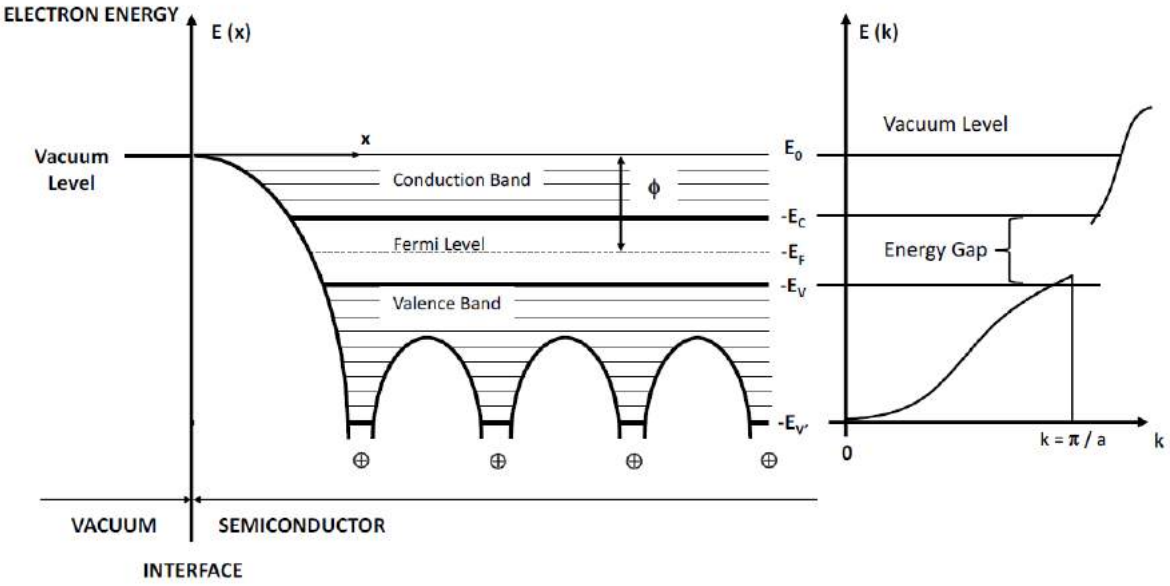

Figure 2.1 energy band diagram of an intrinsic semi-conductor.

2.1.2.2 Relation between work function and semiconductor carrier densities

In the Figure *2.1* conditions, electron number per unit volume is the same as holes in valence band. We have $\mathrm{n} = \mathrm{p} = n_i$. With Fermi-Dirac distribution function $\mathrm{F}(E) = \frac{1}{1+e^{\frac{E-E_F}{kT}}}$, with some approximate simplification of Fermi distribution the electron density n and hole density p :

$$n = N_C exp(-\frac{E_C - E_F}{kT}) \qquad \text{Eq 2. 7}$$

$$p = N_V exp(-\frac{E_F - E_V}{kT}) \qquad \text{Eq 2. 8}$$

$$\mathrm{E}_{F,i} = \frac{E_C + E_V}{2} + \frac{1}{2} k_B T ln(\frac{N_V}{N_C}) \qquad \text{Eq 2. 9}$$

N_V and N_C is the density of states of valence band and conduction band. The work function can be presented:

$$\emptyset = E_0 - E_{F,i} \qquad \text{Eq 2. 10}$$

In doped semiconductors, electron density and hole density are no more equal. For n-type semiconductor, in complete ionization situation, $\mathrm{n} = N_D$.

$$\mathrm{E}_C - \mathrm{E}_{F,n} = k_B T ln(\frac{N_C}{N_D}) \qquad \text{Eq 2. 11}$$

For p-type semiconductor, with $\mathrm{p} = N_A$, we have:

$$\mathrm{E}_{F,p} - \mathrm{E}_V = k_B T ln(\frac{N_V}{N_C}) \quad \text{Eq 2. 12}$$

For intrinsic Silicon (i-type), Fermi level located in between two values above. From Eq 2. 9:

$$\mathrm{E}_i = \frac{E_C+E_V}{2} + \frac{1}{2} k_B T ln(\frac{N_V}{N_C}) = \chi + \frac{E_g}{2} + \frac{1}{2} k_B T ln(\frac{N_V}{N_C}) \quad \text{Eq 2. 13}$$

χ is the electron affinity, E_g is the energy gap between top of valence band and bottom of conduction band. So we can find that donor doping (n doped), the Fermi level gets closer to the conduction band, and the work function decreases; once doped with acceptors (p doped), the Fermi level is closer to valence band, and work function increases. Then the work function can be written as:

$$\emptyset = E_0 - E_{F,n} \text{ or } \emptyset = E_0 - E_{F,p} \quad \text{Eq 2. 14}$$

The *Table 2.1* presents different silicon doping types with its work function. The work function of intrinsic silicon is 4.850 eV.

Type of doping	Resistivity ($\Omega \cdot \mathrm{cm}$)	Doping density ($\mathrm{N} \cdot \mathrm{cm}^{-3}$)	Work function (eV)
N-type/phosphorus	0.02-0.04	1.3×10^{18} – 4×10^{18}	$4.162 - 4.192$
N-type/phosphorus	5-10	1.1×10^{15} – 4.8×10^{15}	$4.343 - 4.364$
Intrinsic Si (i-type)	≤ 100	1.3×10^{10}	4.85
P-type/boron	5-10	8.8×10^{17} – 4×10^{17}	$4.937 - 4.957$
P-type/boron	0.05-0.07	2.4×10^{17} – 1.1×10^{18}	$5.088 - 5.108$

Table 2.1 Work function at 300K, 100 oriented silicon of different doping type and doping intensity.

2.1.2.3 Work function and temperature

Fermi distribution is a function of temperature, the increase of temperature will lead to an increase of high-energy electron probability for both metals and semiconductors. According to the definition of work function, for a given crystallographic direction, the Fermi level varies according to the following equation [Blakemore 85]:

$$\mathrm{E}_F(\mathrm{T}) = \mathrm{E}_{F,0K}(1 - \frac{\pi^2 \cdot {k_b}^2 \cdot T^2}{12 {E_{F,0K}}^2}) \quad \text{Eq 2. 15}$$

However, in all experiments, the maximum change of work function is in the order of milli-electronvolt in a large temperature range, which is almost negligible compared to other phenomena [Blakemore 85] [Burton 76].

2.1.2.4 Work function and crystallographic orientation

Crystallographic orientation is one of the most influential parameter of material work function. The model proposed by Smoluchowski describes the work function of metal surface in two steps. The first step is to consider the Wigner-Seitz cell [Graef 12] as well as all the electrons contained within the metal. The electrons are arranged to minimize the total energy. Then the distribution of the electrons takes place in directions perpendicular to the surface. There are less electrons bound to the metal if the neighboring crystalline cell is absent. As a result, the charge density extends perpendicular to the metal surface to the vacuum level, creating a large surface dipole. The radial charge distribution function of an isolated atom results in the range of electronic charge density reaching the vacuum level.

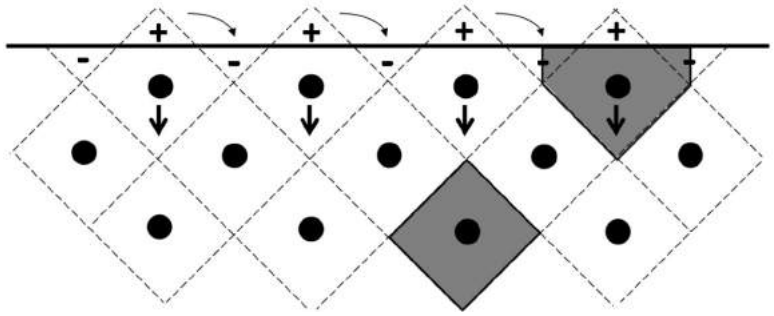

Figure 2.2 Schematic presentation for Smoluchowski model. [Graef 12]

The principle of "Smoluchowski smoothing" is shown schematically in Figure *2.2* with a simple two dimensional cubic lattice. On the surface of the metal, for the first step, the electronic density is reorganized from the Wigner-Seitz cell, represented from dotted line to horizontal line at interface position. Then the redistribution of charges happened, schematized by the dark gray area with square shape inside and reformed shape at the interface. The reformed shape induces a surface dipole depending on the crystallographic orientation and leads to a relaxation phenomenon forcing the atoms to move towards the inside of the crystal lattice by repulsion.

In conclusion, according to Smoluchowski Model, the work function increases if the surface has more dipole induced by charge redistribution. Comparing the direction (100) with (110) in Figure *2.2*, more opposite dipole is created during electronic rearrangement, which leads to a decrease of work function. More real experimental results on many material has confirmed this model [Krahl 77] [Besocke 77].

Element	Plane (hkl)	Ø (eV)	Measurement method
Au	(100)	5.47	Photoelectric effect
	(110)	5.37	
	(111)	5.31	
Cu	(100)	4.59	
	(110)	4.48	
	(111)	4.98	
Si	(100)	4.91	Contact Potential Difference
	(111)	4.60	Photoelectric effect
K	(100)	2.40	Photoelectric effect
	(110)	2.75	
	(111)	2.35	
Cs	(100)	2.30	
	(110)	2.25	
	(111)	1.80	

Table 2.2 Relationship between crystallographic orientation and material work function of different material including metals and semiconductors [Michaelson 77].

Table 2.2 presents for the same material with different crystalline orientation the work function changes. So as a conclusion, as the crystal structure orientation changes the work function so much, for each measurement of the same material, the crystalline orientation should be mentioned if possible.

2.1.3 Conclusion

Work function is the minimum energy necessary for extracting an electron from the Fermi level to vacuum level. This energy is, within a crystal, a function dependent on the crystallographic planes defined by the Miller index (*hkl*). Because of this, the output work is an isotropic quantity.

In reality, the work function is a complicated parameter, which is hard to predict by theory with accuracy. Many factors will change the work function of one same material, including lattice orientation, temperature, doping type, doping level, surface adsorption etc. In general, a higher density crystal face will have high work function. On the other hand, an open lattice and larger atom interval will contribute to get a lower work function for the same materials.

However, work function can be modulated by doping levels and by surface adsorption. Depending on type of doping work function may rise or decrease slightly according to the shift of Fermi level. The adsorption of atoms implies the presence of electrical dipoles on the surface. The larger difference of electronegativity between surface atoms and the adsorbates, the higher dipole will be and the more significant the work function drops.

The adsorption of atoms is a better way to quantify, modulate and minimize work function on given metal surface. At last, the reduction of work function provides a possible method to receive thermoelectric current density in a lower temperature. In another aspect, thermionic current also provides a solution to measure work function by Arrhenius plot, which has an acceptable resolution.

2.2 Experimental Setup

2.2.1 Chemical Vapor Deposition/measurement setup

The setup is composed by two separated compartments: the loading chamber and the deposition/measurement chamber. A manual transfer arm can transport sample module from the loading chamber to the deposition chamber and load the module to the sample holder.

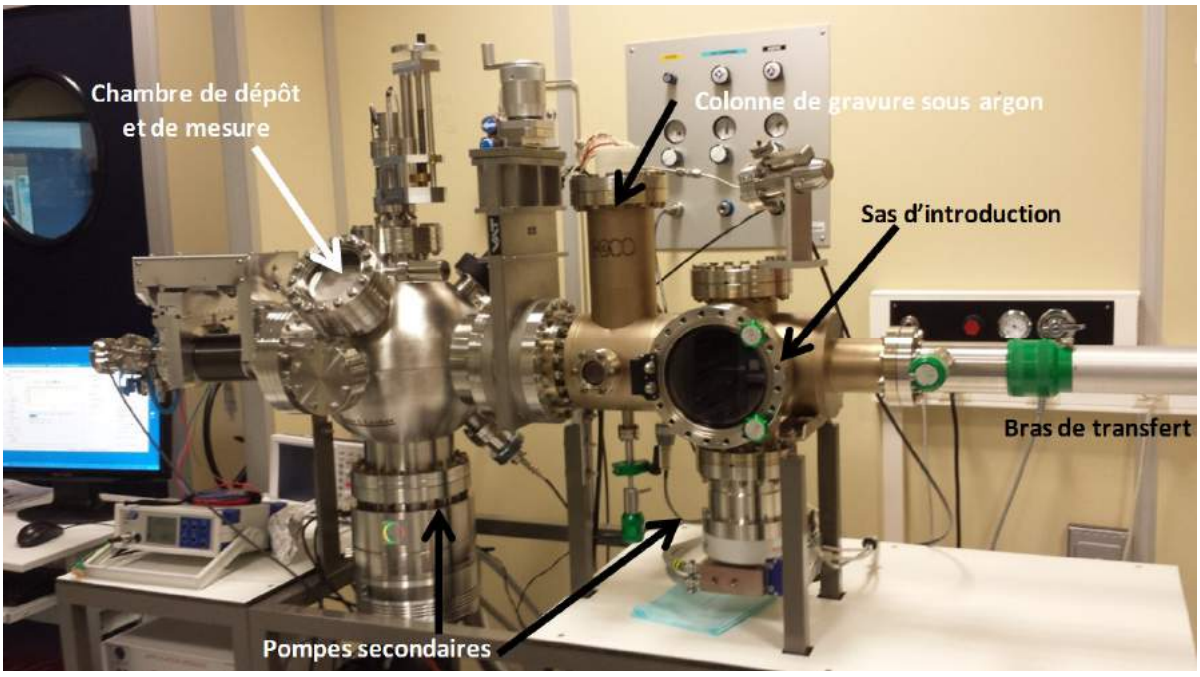

Figure 2.3: photograph of the setup

Figure *2.3* is a global picture of the setup. The two chambers are separated by a gate which can manually operate by the spin handle at the top of the gate. Each chamber is equipped with a series connected pump system. Both systems are composed by a primary pump which is a dry rotary pump and a secondary pump which is a turbo pump. In the right-side smaller loading chamber, the vacuum level can reach the order of 10^{-7} mbar. The left-side bigger deposition/measurement chamber with better performance turbo pump can reach a vacuum level of maximum 10^{-10} mbar.

The loading chamber is built in order not to break the high vacuum level of the deposition/measurement chamber during load or unload processes. This chamber is provided with an argon dry etching system. Therefore, a manual valve regulates the argon supply. As described previously, the vacuum is obtained by the combined action of a primary dry rotary pump Alcatel (5.4 m^3/h) and a secondary water-cooled turbo pump Pfeiffer (210 L/s). Both of primary pump and secondary pump is controlled by a Digital Control Unit by Pfeiffer Vacuum, where all state parameter of turbo pump can be read from the LCD screen of the digital module. An ion gauge measures the chamber pressure. The deposition and measurement chamber has been realized by Kurt J.Lesker company. It consists in a sphere of stainless steel that can accommodate several measurements and deposition tools. The secondary pump providing an ultra-high vacuum is a turbo pump Agilent (700 L/s). An ion gauge measures the chamber pressure.

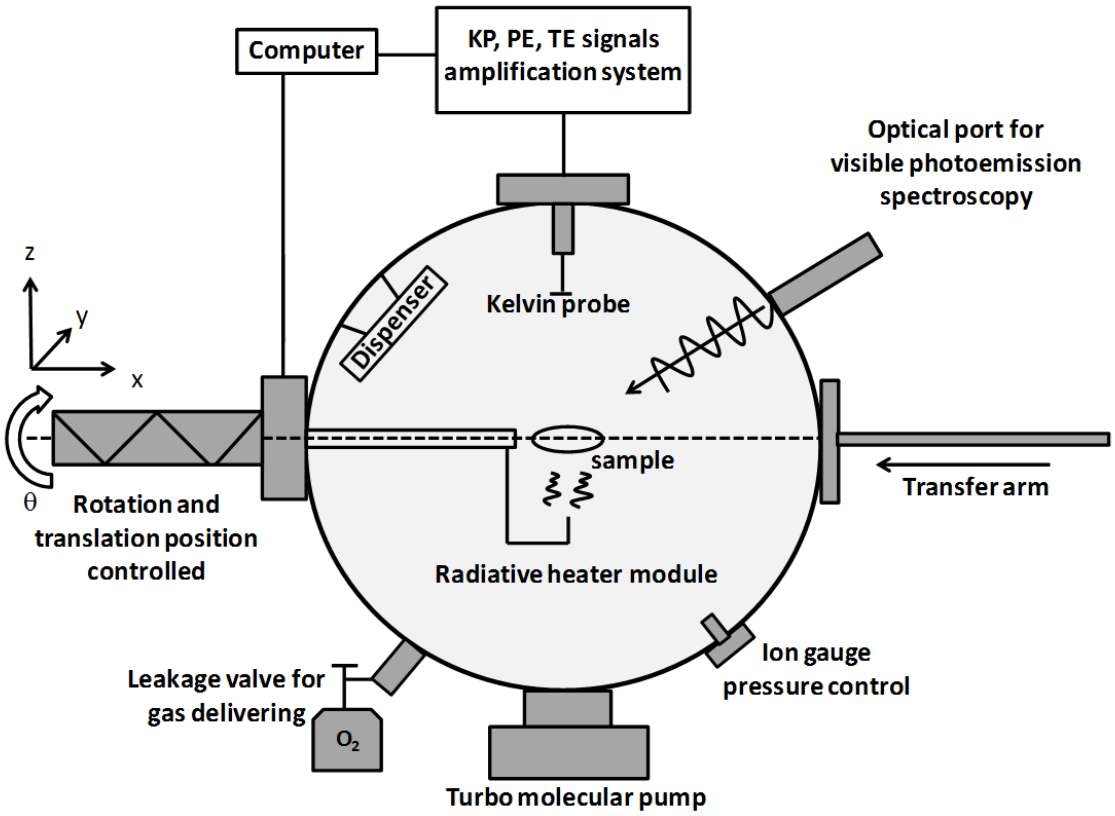

Figure 2.4: Scheme of the deposition and measurement chamber

The deposition/measurement chamber includes a resistive evaporation system, the dispenser, a radiative heater integrated in the sample holder, a Kelvin probe (by KP Technology), and a port for the illumination necessary to the photoemission spectroscopy and a leakage valve for oxygen delivery. The sample holder is in the center of the ultra-high vacuum chamber, which is integrated over a ceramic heater for warming up the sample in order to perform the thermionic measurements. The heating part is insulated from the other components, marking the sample heating through purely radiative method. A temperature sensor is located in the radiator and the sample temperature is calibrated at the

beginning of the project. By knowing the radiator voltage and its current temperature, the temperature of sample can be found accordingly through the calibration table. 16V, 18V and 22V are the commonly used values of voltage applied on the radiator. These represent low, mid and high temperature range for TE measurement.

Figure 2.5: picture of multi-axis manipulator arm including the heating module (left). Schematic representation of the sample holder and transfer arm.

2.2.2 Alkali metal Chemical Vapor Deposition

Before every deposition-characterization work flow, the silicon wafers were first cleaned by Piranha solution for 10 minutes followed by 5% Hydrogen fluoride for 1 minutes with rinsing step after each solution. The aim is to create a clean and hydrophobic surface with H-terminated [*Huba 09*] on top of silicon.

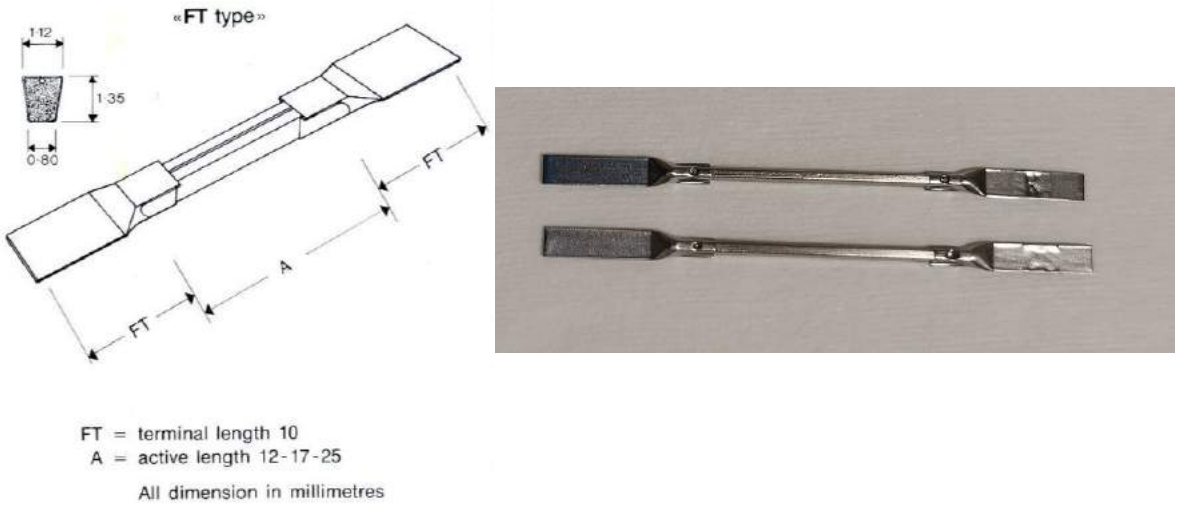

Figure 2.6: (a) schematic of cartridge structure. (b) Cesium and Potassium cartridge image.

The key component in deposition/measurement chamber is SAES cartridges named as the dispenser in Figure *2.4* and presented in Figure *2.6*. It works as a resistive evaporation system under high direct current. During the deposition process the cartridge were firstly positioned close to the sample with the sample facing to it, then heated by a current of 7.5A DC. A vacuum level drop to 10^{-8} mbar can be observed in one minutes. Stabilization of the chamber pressure, then open carefully the oxygen valve at the bottom left side of the chamber to control the pressure at a constant value of 4×10^{-7} mbar. This operation creates a saturating oxygen environment [*Bertel 89*] inside the chamber. Keep adjusting the valve to maintain the pressure for 10 minutes then stop the current of cartridge. During the entire

deposition process, no significant temperature change is observed. After deposition, a film of alkali material can be observed polished and/or colored on the clean pure silicon (100) wafer (p-type Boron doped, resistivity 0.02-0.04 Ω·cm).

2.2.3 In chamber characterization methodology

In our study, we took advantage of a dedicated measurement set-up, which is integrated to the same chamber where alkali thin film were deposited. The workflow of samples characteristics measurement were processed as follow: First, contact potential difference by Kelvin probe, then photoemission measurement followed by thermionic emission measurements.

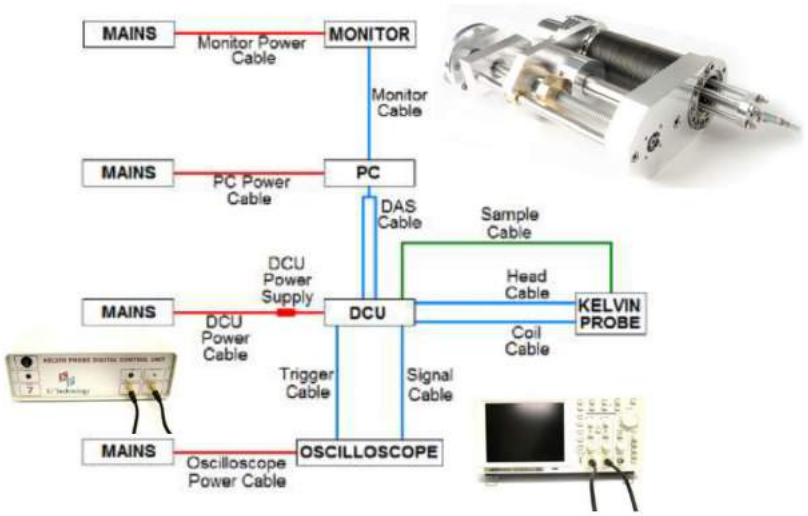

Figure 2.7: Scheme of Kelvin Probe system, the bottom-left image shows the Digital Control Unit (DCU), up-right image is the probe, and the bottom-right is the oscilloscope.

2.2.3.1 Kelvin probe setup and contact potential difference measurement

Kelvin probe is a vibrating electrode device that probes the outermost layers of material of great sensitivity without touching the surface. It was firstly proposed more than one hundred years ago based upon equilibrium of energy and was used to study contact electrification of metals. After decades of development, it became a non-contact, non-destructive vibrating capacitor device which is used to measure the work function of conducting materials or surface potential of semiconducting or insulating surfaces. Nowadays, the technique has a sensitivity resolution of 1-3 meV. [Baikie 14] Kelvin probe measures the work function via an indirect way that is equilibrium not extracting electrons. The Kelvin probe module showed in Figure *2.7* is fully compatible with Ultra-high vacuum and is connected to DCU with a separated amplifier.

When two materials with different Fermi-levels are connected together, they equalize by a flow of electrons from the lower work function to the higher work function. Kelvin probe systems can measure the current, detect the voltage change and it is how Kelvin probes measure work function. With the Kelvin probe system, work function can be measured by the method of Contact Potential Difference short for CPD measurement. CPD measurement makes it possible to determine the relative difference of work function between two materials through the variable capacity constructed by the sample and probe.

Figure *2.8* shows the energy diagrams between the sample and the tip surface. Firstly, position the sample in front of tip at a distance d, before connecting sample and the tip like Figure *2.8*(a). At this position both samples and tip have the same vacuum level, where ϕ_S and ϕ_{Tip} are the work function of sample and the tip, and ε_s and ε_{Tip} represent their Fermi levels.

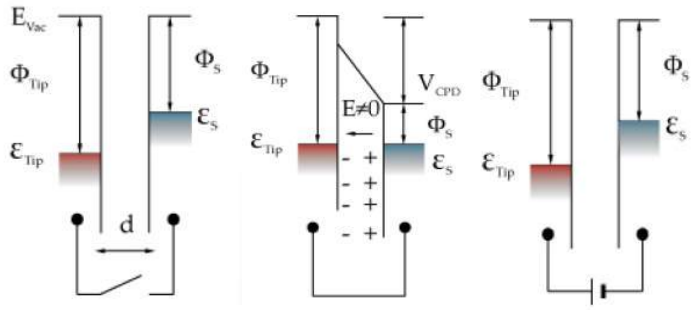

Figure 2.8: Energy diagrams of the sample and the Kelvin probe. (a) Before connection of sample and Kelvin probe. (b) After building an external electrical contact. (c) A voltage added in between sample and Kelvin probe

After connecting sample and the tip, ε_S and ε_{Tip} equalize resulting in a flow of charge. The charge stabilizes and then produces a potential gradient termed as contact potential V_{CPD}. The structure of sample and the tip facing each other create a charged capacitor where two surfaces are charged oppositely. The corresponding energy diagrams are presented on Figure *2.8*(b).

Inclusion of a variable "backing potential" in between sample and the tip at external circuit position permits biasing of the tip or sample. At the unique point where backing potential has the same value and opposite signal as V_{CPD}, a null output signal is obtained. Although this backing potential can be measured directly, it is at a high noise position. With Kelvin probe, the tip can oscillate above the sample, changing the space d and the value of the capacitance as a function of time.

$$\mathrm{d(t)} = d_0 + d_1 \sin(\omega t) \qquad \text{Eq 2. 16}$$

Replacing d(t) in the expression of capacity $\mathrm{C} = \frac{\varepsilon S}{d}$

And we have:

$$\mathrm{C(t)} = \frac{C_0}{1+\frac{d_1}{d_0}\sin(\omega t)} \qquad \text{Eq 2. 17}$$

C_0 is the capacity when tip locate at neutral position d_0.

According to the manual of Kelvin probe system, the signal which is a small current, will first arrive at an amplifier and then be measured by the analysis module. The signal is determined by the surface charge Qs on the probe, where Qs can be expressed by:

$$Q_s = (V_c + V_b)\mathrm{C} \qquad \text{Eq 2. 18}$$

V_c is the voltage difference between probe tip and sample, V_b is the external voltage used to balance the circuit. Therefore, the output current is:

$$\mathrm{i}(t) = \frac{dQ_S}{dt} = \mathrm{G}(V_c + V_b)\frac{dC}{dt} \qquad \text{Eq 2. 19}$$

G is the gain of the amplifier.

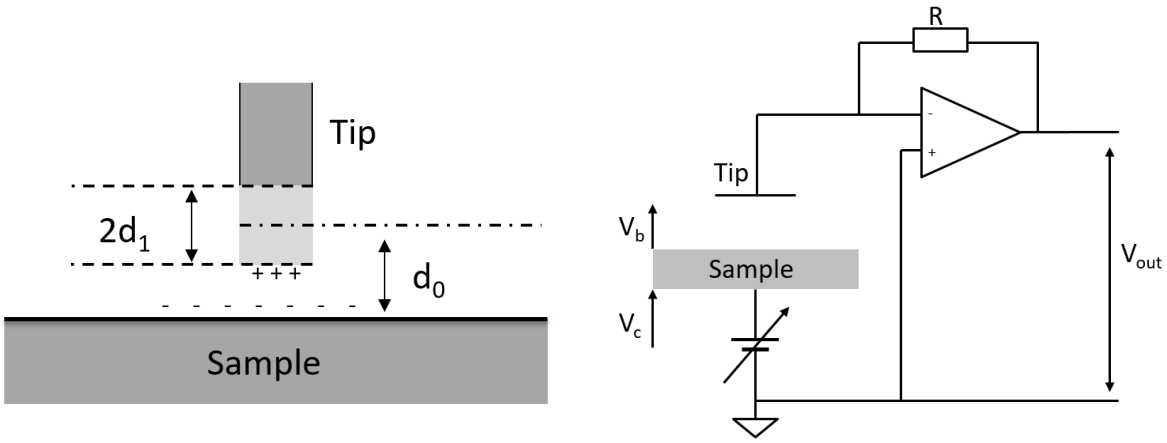

Figure 2.9: (a) The sketch represents the vibrating probe above the sample and defining relative position with amplitude. (b) Sketch of the Kelvin circuit

With the contribution of the oscillatory probe, the peak-to-peak voltage is:

$$V_{ptp} = (V_c + V_b)R_f G C_0 \omega \varepsilon \sin(\omega t + \varphi) \qquad \text{Eq 2. 20}$$

ε is defined by modulation index and Rf is the I/V converter feedback resistance, ω is the angular frequency of vibration, and φ is a phase angle.

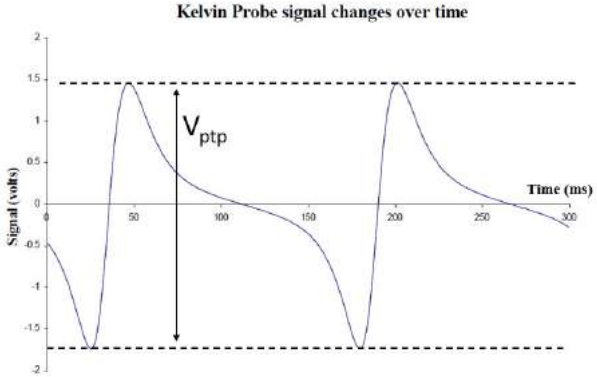

Figure 2.10: (a) Signal output real by oscilloscope. (b) Sketch of the determination of VCPD. [Baikie 91] The gradient is proportional to the tip to sample distance.

The equation $Vptp = (V_c + V_b)R_f G C_0 \omega \varepsilon \sin(\omega t + \varphi)$ Eq 2. 20 tells that in given oscillatory the value of V_b has a linear correlation with V_{ptp} as the blue line showed in Figure *2.10*(b). The intersection position with the abscissa represents the $-V_c$ where the signal output is null. This indirect technique is so called off null measurements. To avoid measuring the backing potential at the null position, an indirect measurement to locate the V_B-V_{ptp} line can help locking the accurate position of V_c without the effect of random noise signal on the CPD measurement. In practical measures, two points far away from the null position are enough to calculate V_c.

2.2.3.2 Direct measurement of work function by photoemission system

In 1930s, the theory of using photoelectric effect to determine the work function proposed by Fowler [Fowler 31] and DuBridge [Dubridge 33]. With the measurement resolution relaying on a monochromator [Crowell 62], photoemission effect is a direct, reliable and repeatable way to

determine the work function. Firstly, the sample is shone with monochromatic light and the photocurrent I_{ph} is harvested by the Kelvin probe, held at a constant distance from the sample. In all PE measurements, the distance is 1.25 cm to avoid inhibiting photoemission by the shadow of the tip. From the theory of Flowler and DuBridge, the expression of photoelectric current density J(hν) is a function of photons' energy:

$$J(h\nu) \propto B(k_B T^2)\left[\frac{(h\nu-\emptyset)^2}{2}+\frac{\pi^2}{6}+\sum_{n=1}^{+\infty}(-1)^n\frac{exp[-n((h\nu-\emptyset))]}{n^2}\right] \qquad \text{Eq 2. 21}$$

At the $h\nu > \emptyset$ condition, the equation 2.21, electrons were emitted successfully under a range of different wavelengths. Then the tip can absorb the electrons to measure the photo current which is proportional to the square of photon energy minus work function:

$$J(h\nu) \propto (h\nu - \emptyset)^2 \qquad \text{Eq 2. 22}$$

Similarly to CPD measurement, finding the $J(h\nu) = 0$ and the ν at limit situation is hard and noisy. A similar off null measurement methods was applied. First measure step-by-step the correspondent photocurrent of different photon energy at maximum range ignoring whether the photon energy were greater or less than work function.

In Figure *2.11* (b) the energy band diagram represents the energy relationship in each step of photoemission effect. A photon of hν energy excites an electron above the vacuum level. With the remaining energy in kinetic form and the help of electric field created by 10 Volt bias on the tip, the electron emitted can finally arrive the at tip surface. Then, the corresponding PE current can be amplified and measured by the Kelvin probe system. Here the 10 V bias on the tip is the maximum voltage allowed by the Kelvin probe setup. A high bias voltage V_b can ensure all the emitted to vacuum level electrons arrive at the tip, which helps increasing the accuracy of measurement. In the optimum condition, work function resolution measurement based on photoemission can be as low as 30-50 meV. [Baikie 14]

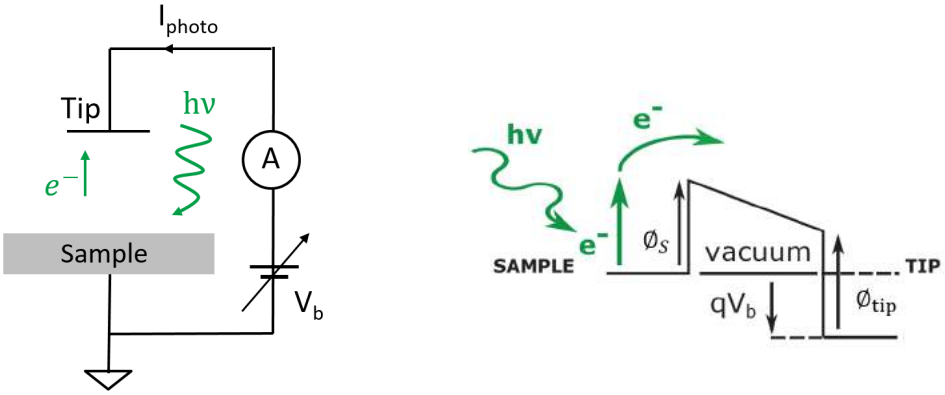

Figure 2.11: (a) Sketch of photoemission circuit. (b) Energy band diagram of photonic emission.

Then, we draw a graph to present the relation between photon energy and square root of photocurrent on Figure *2.12*. In this graph, the measurement results are very linear in the range of 2.15 eV to 2.8 eV. According to Eq 2.22, a linear fitting is performed with the data in selected range. The linear trend can then be extrapolated to photocurrent zero position to determine the work function of the sample. At the zero position, $h\nu = \emptyset_{Sample}$, work function can be acquired.

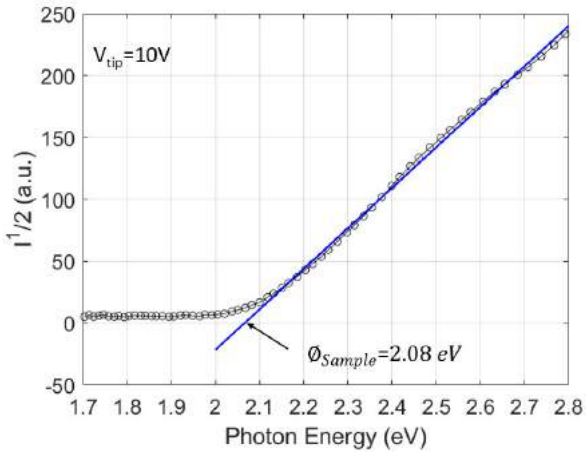

Figure 2.12: Photocurrent measurement at different photon energy and linear fitting for measuring work function.

Based on photoemission effect, measuring the work function of the tip is also feasible [Afanas 07]. From Figure *2.11* (b), the energy band diagram of photonic emission a simple relationship between the energy of incident photons hν, the photoelectron detection voltage V_{onset} and the work function of tip surface $\emptyset_{tip}$.

$$h\nu = \emptyset_{tip} + qV_{onset} \qquad \text{Eq 2. 23}$$

The Figure *2.13* (a) shows the curves of root of photocurrent and tip voltage at different wavelength from 450 nm to 570 nm at an interval of 10 nm. By linear fitting each curve, V_{onset} can be located at abscissa axis for each correspondent photon energy. Later with these onset-voltage values a plot like Figure *2.13* (b) can be created. A second linear fitting with selected points in red lines has an intersection with abscissa axe. This intersection means the V_{onset} equals to zero, while at the same time, the photo-energy value equals the tip work function. In the case of Figure *2.13*(b) the tip work function equals 4.94 eV.

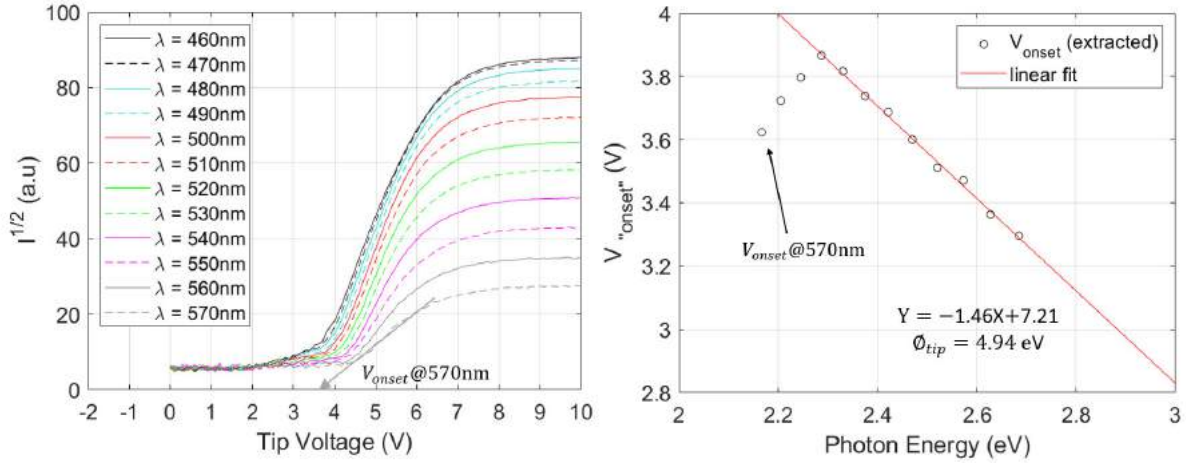

Figure 2.13: (a) $\sqrt{I_{PE}}/V_{tip}$ curve at different wavelength. (b) V_{onset}/Photon Energy and linear fitting plot.

2.2.3.3 Thermo-emission with Kelvin Probe and with Agilent semiconductor parameter analyzer

The Richardson-Dushman equation describes the effect of thermo-emission: electrons will be emitted from surface of high enough temperature. Defining the energy as k_BT, and the energy barrier thermos-emitted electrons need to overcome as Ø, the thermal electrons emitted from the sample surface can be collected at the tip with the help of an electrical field created by positive voltage. The position relation of heating module, the sample and the tip are presented in Figure *2.14* (a). The tip is located 1.25 cm above the sample that is heated by a ceramic radiator. Like in photoemission the current bypass the tip of Kelvin probe can be measured by system. V_b is a tunable voltage applied to the tip. The energy band diagram Figure *2.14* (b) represents the barrier that thermal electrons need to overcome in order to reach vacuum level is $Ø_S$, the positive voltage on the tip is V_b, while the work function of the tip is $Ø_{tip}$.

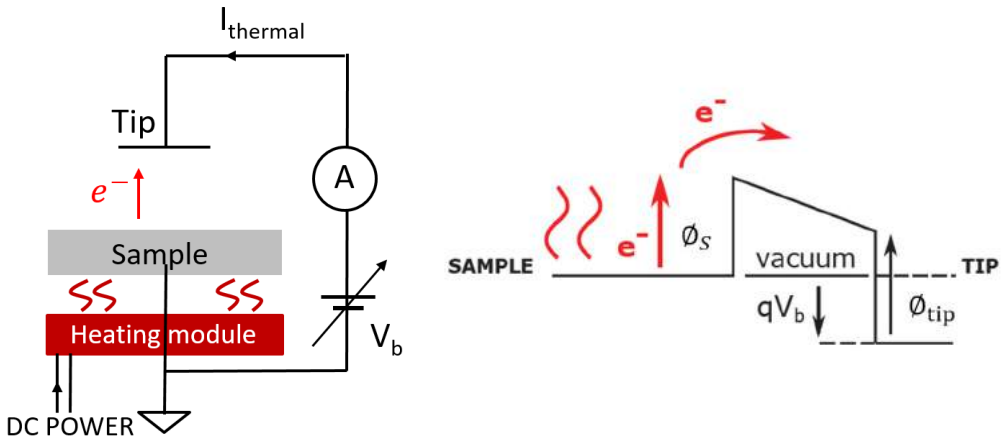

Figure 2.14: (a) Sketch of thermal-emission circuit. (b) Energy band diagram of thermionic emission.

In the saturation regime, a positive voltage was applied on the tip. The total current density is independent from the applied potential due to the saturation regime. The thermal current is represented by the equation:

$$j_{saturation} = AA^*T_s^2 exp\left(-\frac{q\emptyset_s}{k_BT_s}\right) \qquad \text{Eq 2. 24}$$

In the ideal forward emission only situation, when electrons are emitted only from the sample surface and cannot be emitted from the tip surface, according to Richardson's law, the current with voltage applied is:

$$j_{forward} = j_{s\to t} = AA^*T_s^2 exp\left(-\frac{q\emptyset_s+qV_b}{k_BT_s}\right) \qquad \text{Eq 2. 25}$$

Here, T_S is the sample temperature, q = −e, and with knowing work function of the sample, the only parameter that influences the thermal current is the voltage added on the tip which can tuned from -10V to 10V by Kelvin probe module and -20v to 20v by Agilent semiconductor parameter analyzer.

A COMSOL thermal conduction simulation was performed to analyze the tip temperature. (Detail description in chapter 3) The result presents that in ultra-high vacuum environment the radiative heat flow from sample to tip at 1.25 cm distance is low enough to ignore the backward emission. The equation 3.10 presents the total current density considering the backward emission.

$$j_{total} = j_{s\to t} - j_{t\to s} = AA^*T_s^2 exp\left(-\frac{q\emptyset_s+qV_b}{k_BT_s}\right) - AA^*T_t^2 exp\left(-\frac{q\emptyset_t}{k_BT_t}\right) \qquad \text{Eq 2. 26}$$

However, during the experiment, to measure work function of the sample, the focus is located at the saturation thermal current. During the heating of sample, the potential of the tip changes periodically from -10V to 10V. So, by separate the variable T_s^2 of Eq 2.24 with exponential part:

$$\frac{j_{saturation}}{T_s^2} = AA^* exp\left(-\frac{q\emptyset_s}{k_B T_s}\right) \qquad \text{Eq 2. 27}$$

Logarithm both side of equation:

$$\ln\frac{j_{saturation}}{T_s^2} = \ln AA^* - \frac{q\emptyset_s}{k_B T_s} \qquad \text{Eq 2. 28}$$

This form is linear and the corresponding Arrhenius plot is a convenient way to measure the work function. According to the expression the $\ln\frac{j}{T^2}$ is the function of $\frac{1}{T}$ and the gradient is $-\frac{q\emptyset_s}{k_B}$. Thus after fitting the measurement results and with the gradient both work function $\emptyset_s$ and Richardson constant A^* can be defined.

The Kelvin probe module, which is integrated with the Kelvin probe inside our vacuum chamber, is not the only device we used to measure the thermionic current. Agilent semiconductor parameter analyzer is another device available in the laboratory to measure and analyze the characteristics of semiconductor devices. Instead of using DCU units and computer, by connecting Kelvin probe signal to Agilent 4155C allows us to perform both measurement and analysis of measurement results. The Agilent 4155C has four highly accurate source/monitor units, two voltage source units, and two voltage measurement units. It can measure voltage values with a resolution of 1μV and current values with a resolution of 1pA. [4155C user's guide]. This device is generally more accurate and helps us to avoid the offset problem by the amplifier at zero current through DCU measurement.

2.2.4 Ex-situ characterization methodology

In this section, both of the characterization techniques were applied to define the chemical composition of deposited thin film. With the limitation of experimental condition, these characterizations were performed after the sample exposing to atmosphere.

2.2.4.1 Scanning electron microscopy – energy dispersive X-ray analysis

Scanning electron microscope (SEM) is one of the most direct and useful tools in micro-fabrication and characterization. By using a focused beam of electrons, the microscope scans the sample surface in vacuum with better than one nanometer resolution. During the scanning process, various types of signals are produced including secondary electrons, characteristic X-rays, back-scattered electrons and so on. The scanning electron microscope we use (Gemini Ultra 55) is equipped with standard secondary electron detector and back-scattered electron detector to produce high-resolution images of sample surface, the characteristic X-ray detector to measure energy dispersive X-ray spectroscopy. Due to the much focused high-energy electron beam, SEM can produce an image with a considerable depth of field and sometime can produce the under SOI image beneath the Silicon surface at a lower resolution. This feature helps to visually analyses the processes of 3D structure fabrication.

Energy dispersive X-ray analysis the nature of the chemical elements in the sample. It is capable to measure qualitatively and quantitatively the elements presented. Firstly, the electron beam hits the sample and transfer part of its energy to the atoms. Some electrons in the sample atoms use this energy and temporarily transit to a higher energy level called excited state. Then when these electrons leave, the higher energy state and drop to ground state the energy are released in the form of an X-

ray. Figure *2.15* (a) represent the electrons' energy transition of these two steps. This X-ray has energy equal to energy difference between these two energy states. This energy difference is uniquely depending on the atomic number. Consequently, by characterizing the wavelength of X-ray and the help of database of each element, all types of elements that exist in the sample can be identified.

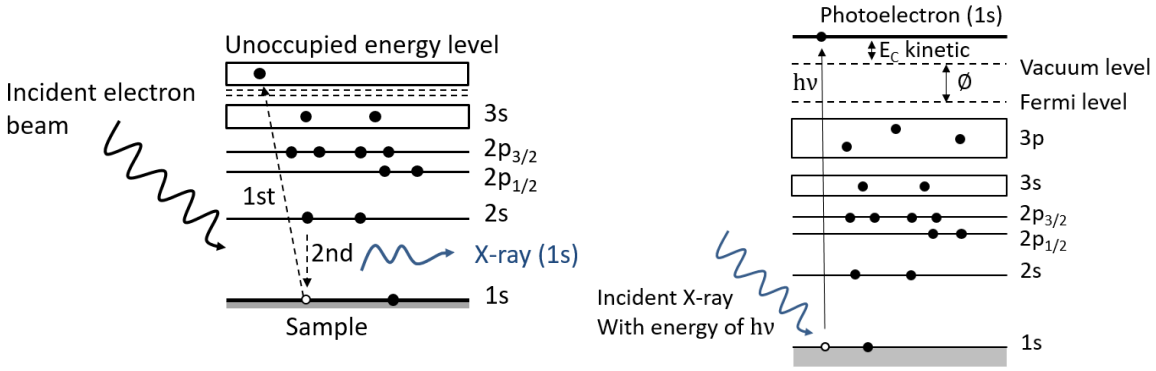

Figure 2.15: (a) Energy band sketch of X-ray generation process in EDX analysis. (b) Photoelectron emission from solid material. White dot indicates the electron position before emission.

2.2.4.2 X-ray photoelectron spectroscopy

The X-ray photoelectron spectroscopy is one of most popular surface-sensitive method to characterize materials qualitatively and quantitatively. By irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and quantity of electrons emitted from the surface. [Siegbahn 56] The results of X-ray photoelectron spectroscopy gives us not only the information of element types and quantity but also chemical information thanks to the bonding states. According to the Figure *2.15* (b), when a photon interacts with an electron elastically, a photoelectron is emitted with kinetic energy of E_C. The photon energy is $\mathrm{h}\nu$. With the work function of sample $\emptyset_s$ and the interacted valence electron has energy E. An equation can be established to represent the energy relationship:

$$E_C = \mathrm{h}\nu - \emptyset_s - E_b \qquad \text{Eq 2. 29}$$

With the selected wavelength, the work function of sample and kinetic energy read from by X-ray photoelectron spectroscopy, we can get the energy difference in-between energy levels, which is a good fingerprint to identify the element. In practice, the sample work function is not needed. With E_C measured and $\mathrm{h}\nu$ known, the spectra is shifted to adjust the energy E_b of carbon which function as a common reference.

The measurements were carried out using a Physical Electronics model 5600 system for which the base pressure is in the low 10^{-10} Torr range. A monochromatic Al Kα X-ray source making a 90° angle with the electrostatic hemispherical analyzer was used for all XPS measurements. The analyzer acceptance angle and pass energy were set to 14° and 12 eV respectively. The analyzed area was 400µm in diameter whereas the electron take-off angle was fixed to 45°. For the sensitivity factors of XPS we used the following reference presented by J.F. Moulder [Moulder 92]. The XPS spectrum is a plot shows the number of electrons detected at the binding energy of detected electrons. The XPS peaks at certain binding energy values directly identify the elements. For the same element, each peak represent a possible electron configuration of the electrons inside atoms. The signal intensity or the number of electrons detected shows the general percentage of correspondent elements. In this way, elements can be quantitatively analyzed.

2.3 Potassium oxide with CVD process

We now apply these characterization methods to the sample, which is a high doped Silicon with potassium oxide film deposited by CVD in the high-vacuum chamber. All the work function measurement processes are performed in the same chamber without significant pressure change and are carried out in few days.

2.3.1 Contact potential difference with Kelvin probe

Potassium deposition and characterization was performed on seven different samples. According to the workflow presented in sector 2.2, CPD measurements were performed right after the CVD deposition process several times with an interval of around 10 minutes. This repetitive measurement after deposition with interval is due to the pressure changes in the chamber. In 20 minutes, in chamber pressure bringing back from 10^{-7} mbar to 10^{-9} mbar after CVD process. During this time, the newly deposited alkali oxide thin film change to a more stable state at high vacuum environment. For all CPD measurements in this project the tip of the Kelvin probe is approached to the sample with great care until the CPD capacity gets targeted sensitivity at the right distance. The CPD signal is shown in Figure *2.10* (a). As the oscillation period ω constant, and the V_{ptp} (peak-to-peak voltage) changes according to distance in-between tip and the sample, to have the same gradient value make the tip keep a stable position during every CPD measurement. Furthermore, in order to precise the sample work function value, for each CPD measurement, an average of 70 times and repetition of 50 points is set to be the standard parameters.

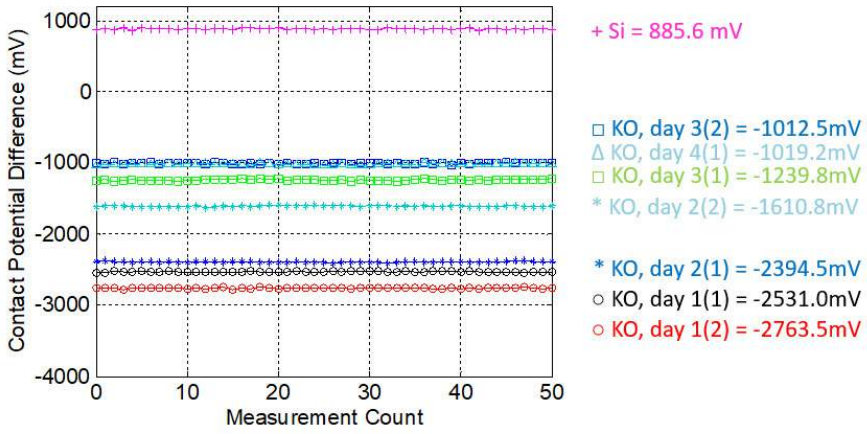

Figure 2.16: CPD measurements plot for clean silicon wafer and potassium oxide thin film at different stages. In-between day 2(1) and day 2(2) an annealing process was carried out.

First, with pure p-doped silicon (100) wafers measurement $\emptyset_{si} = 4.91\text{eV}$ [Holzl 79] [Riviere 69] [Michealson 77], and $\text{CPD} = 0.885\text{mV}$, the tip work function is no more equals to the given value in the manual of Kelvin probe($\emptyset_{tip} = 4.76\text{eV}$). It is highly possible that during the CVD deposition process the potassium vapor filling the chamber and a certain amount of potassium atoms stay on tip surface. Although for a single deposition, the tip surface pollution may not be significant. After tens of cycles of deposition, it lowers the tip work function level compared to its original value. In this particular case, from the result of first CDP measurement on clean silicon wafer, tip work function can be speculate as $\emptyset_{tip} = 4.02\text{eV}$.

The Figure *2.16* tells that the work function of the potassium oxide changes even after the deposition. Especially the value changes significantly right after the deposition when pressure changes and after each thermal emission characterization when temperature changes rapidly. For example, the measurement day1 (1) and measurement day1 (2) have only an interval of 10 minutes with all the configuration of the setup remain untouched. The work function of the sample decreased for around 200mV and this circumstances repeat after each deposition for both potassium and cesium. The newly deposited sample has a work function of 1.26eV. This value rise to 1.63eV before the thermal emission one day later.

In-between the measurement day2 (1) and day2 (2) the thermal emission is carried out. The potassium oxide film changes during the annealing process especially at higher temperature condition. After thermal emission measurement, according to CPD results the work function rise to 2.42eV and remain considerably stable after first annealing. However, these values after thermionic emission measurement are less convincing since the tip is located close to the sample and the evaporation of Potassium may greatly pollute on the tip surface for a certain time.

2.3.2 Photoemission characterization

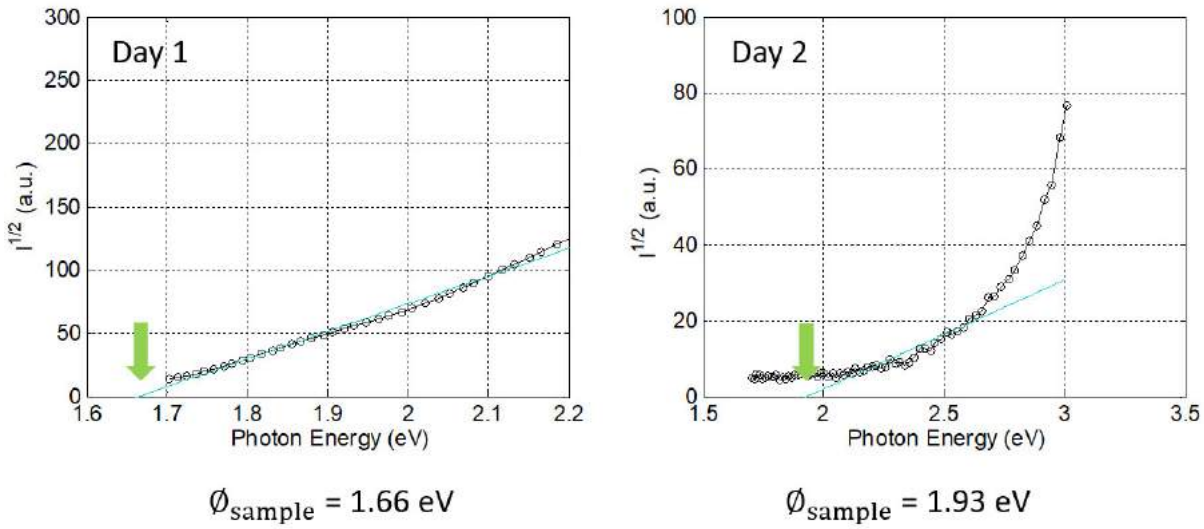

Figure 2.17: Two photoemission plots. (a) PE measurement after deposition, Gain = 1. (b) PE measurement one day later after deposition, Gain = 4.

Figure *2.17* shows two examples of photoemission analysis. The value of the sample work function, evaluated from the plot of $\sqrt{I_{ph}}$ as a function of photon energy, is 1.66eV and 1.93eV. While speculate tip surface work function is about 4eV and corresponding sample work function by CPD is 1.63eV. Due to weak PE signal at the second day, and the higher gain value lead to a higher noise level, the second measurement is less accurate especially at low photon energy range. The day 2 data present much less linear. It may due to two threshold process, which corresponded to two components with similar and slightly different work function. In the case of day 2, the noise level is so high and the PE measurement for characterization tip work function is failed.

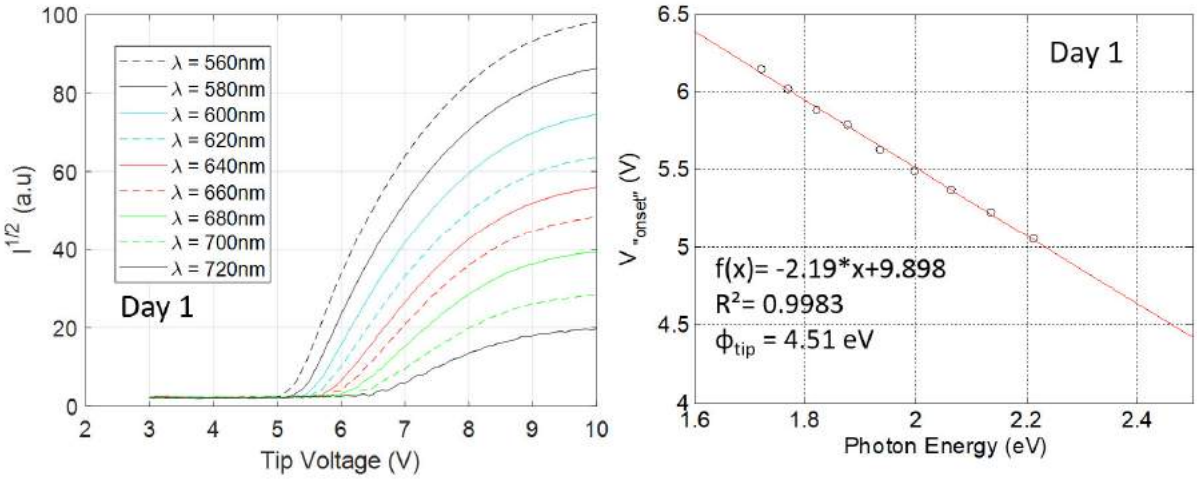

Figure 2.18: PE measurement plot for tip work function at day 1. (a) $\sqrt{I} - V$ plot at various wavelength (b)$V_{onset} - photon\ energy$ and linear fitting plot

By comparing Figure *2.18*(a) and Figure *2.19* (a) we find in weak signal circumstance it is not possible to define V_{onset} values. In some extreme situations, as Figure *2.19* (a) presented, the spectrum is noisy and it the PE tip work function calculation by linear fitting is impossible. The points of V_{onset} in Figure *2.19* (b) is somehow random distributed on the plot, with which a linear fitting is not convincing at all. With only a visible light source and the maximum photon energy $\mathrm{h}\nu$ limited, photocurrent signal is limited and sometimes full of noise. Especially for some higher work function samples, when signal is to week, the amplified signal is full of that data analyses is unreliable. To solve this problem, a wider wavelength range light source, a better amplifier, a higher voltage applied tip are helpful.

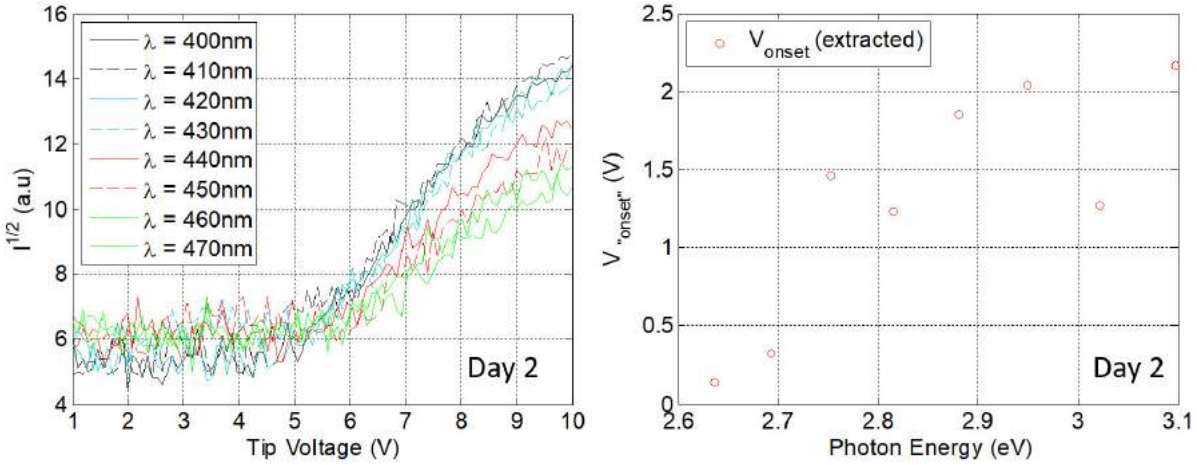

Figure 2.19: PE measurement plot for tip work function at day 2. (a) $\sqrt{I} - V$plot at various wavelength (b) (b)$V_{onset} - photon\ energy$ plot not possible to do linear fitting

2.3.3 Thermionic emission characterization

The thermionic emission measurements were performed heating the sample from 500K to the maximum temperature 850K and stop after the current density began to drop. The analysis is shown in Figure *2.20* (a) and (b). From the first plot, J vs T, it is possible to extract the information about the evolution of the thermionic current density: for the blue line, thermionic current starts increasing at around $\mathrm{T} = 650\mathrm{K}$, and reaches $1.3\mu\mathrm{A}/cm^2$ at 725K, the highest temperature in this experiment. To

extrapolate $\emptyset_{sample}$from the Arrhenius plot Figure *2.20* (b) we fitted the region where the current density dramatically increases with the temperature, from 650K to 720k, obtaining $\emptyset_{sample} = 1.66eV$.

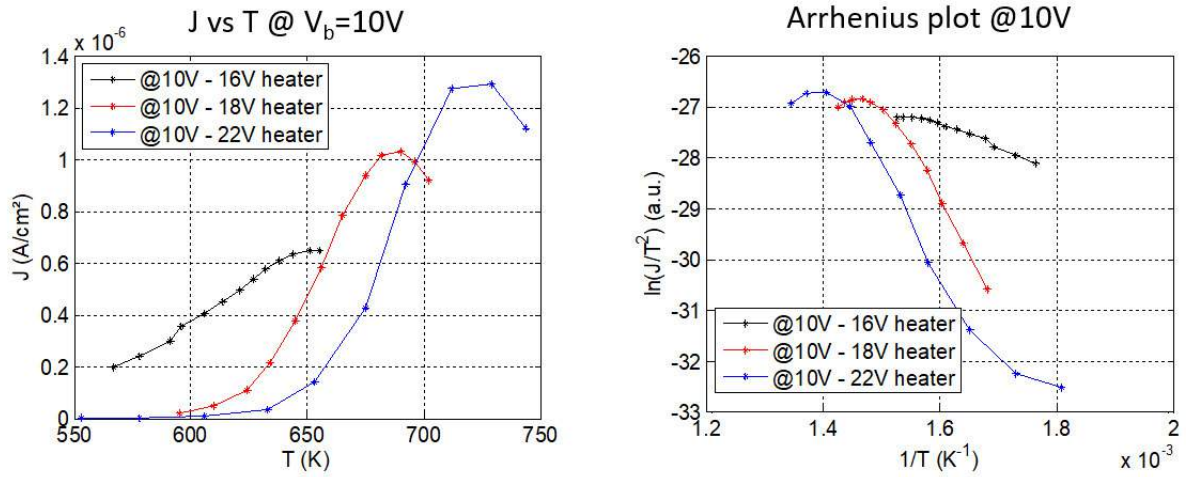

Figure 2.20: TE measurement plots (a) Current density curves at different heating speed. (b) Arrhenius plot for sample work function calculation.

The sample was heated three times with different applied voltages to the radiator and TE measurement was implemented at different temperature range from low to high. From Figure *2.20* (a), a significant thermal current decrease between the first and the second measurement represent the atomic structure of the thin film changes. This phenomenon has also been detected by CPD and PE measurement. At the end of second and third test, a deterioration of the film may occur which may lead to the evaporation of potassium element and rise the work function further. The work function result from these three measurements are 0.39eV 1.65eV 1.66eV.

The work function value 0.39eV may represents a rare potassium oxide which is not stable and/or easy to evaporate at higher than room temperature. This below 1eV alkali metal compound with ultra-low work function was detected several times. Form the next sample fabricated a -4500mV CPD value was measured which represents a similar below 1eV work function result. Same as PE measurement, depends on the way of fitting, a below 1eV work function result with R^2>0.95 can be obtained. Up to now, the conclusion for this ultra-low work function material is that:

- It is a highly possible to be a product by CVD deposition and is not stable at high temperature. More evidence and research is needed to define the existence and process feasibility.
- Other than the first nearly unbelievable value, the 1.65eV 1.66eV are much more convincing and both of the value is in the range of CPD results and PE results. Moreover, compared to the potassium metal work function of 2.29eV, the potassium oxide is a better candidate for thermionic converter electrodes coatings.

2.3.4 XPS spectrum characterization

XPS analysis was performed right after the oxide deposition and after the annealing due to thermionic emission measurement. XPS analyses were carried out using a physical Electronics model 5600 system for which the base pressure is in the low 10^{-10} Torr range. A monochromatic Al Kα X-ray source making a 90 ° angle with the electrostatic hemispherical analyzer was used for all XPS measurements. The analyzer acceptance angle and pass energy were set to 14° and 12 eV respectively. The analyzed area was 400μm in diameter where the electron take-off angle was fixed to 45°. The

collected XPS spectra were fitted by Gaussian-Lorentzian profiles and the oxide composition was determined by standard quantitative analysis using the appropriate sensitivity factors. [Moulder 92]

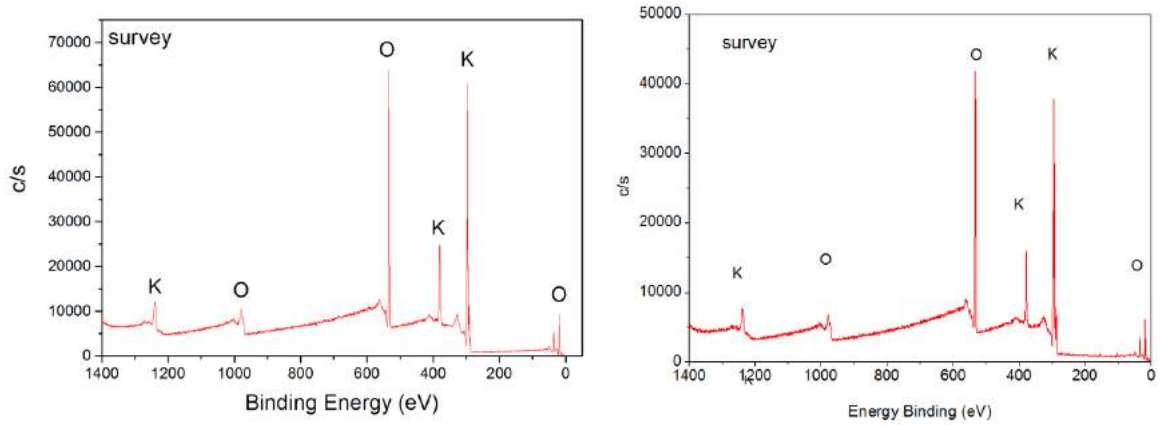

Figure 2.21: XPS spectrum before and after annealing (a) Sample right after CVD deposition (b) Sample after all in-chamber characterizations including a few thermionic emission measurements.

The composition of the obtained thin film of potassium oxide is revealed by XPS analysis presented in Figure 2.22. The XPS spectra of O1s has a peak at 534.26 eV. We interpret this peak as the presence of KO_2, potassium superoxide [Krix 14] [Lamontagne 95]. This interpretation is supported by the presence of the two peaks of K2p, respectively at 296.09 eV and 298.89 eV (Figure *2.22*(b)). The lower peak at 535.79 eV in O1s spectra corresponds a binding of type O-Fx and the element fluorine was introduced due to the silicon wafer cleaning process with HF solution.

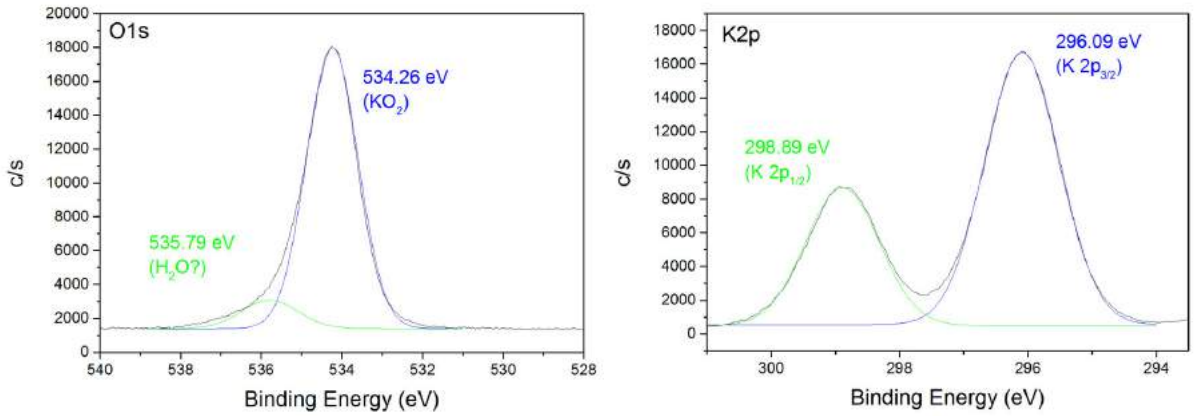

Figure 2.22: XPS complete spectrum right after deposition (a) O1s spectrum, showing a main peak at 534.26 eV; it can be interpreted as the presence of KO2. A second peak at 535.79 eV is present, corresponding to a binding of the type O-Fx. (b) K2p spectrum, confirming the presence of potassium oxide.

On potassium oxide covered samples, if compared before and after annealing, the oxide composition indicated the coating film may containing KO_2, K_2O_2 and K_2O_3. These oxides changes during the annealing process. Both before and after the annealing, the peaks of potassium element content in Figure *2.21* remain position unchanged. A slight decline of peak intensity is observed. We interpret it as the potassium evaporate in to the vacuum along with the reaction of oxides. The result was further confirmed by the presence of potassium oxides [Wu 99]. We conclude that the annealing up to 800K, does not change the elemental composition of the potassium oxide film and will change the compound structures.

2.4 Cesium oxide with CVD process

2.4.1 Contact potential difference with Kelvin probe

Cesium deposition and characterization was performed separately on seventeen different samples during a period of more than one year. Same as potassium characterization, according to the workflow presented in sector 2.1, CPD measurement on cesium deposited samples were first performed right after CVD process. Before deposition, a CPD measurement on p-doped clean silicon wafer (100) was applied as standard workflow. And it usually results from about 650mV to around 1000mV. In this particular sample, the result of silicon work function of 647.2mV as present is Figure *2.23*. The CPD right after deposition drops significantly to -1756mV.

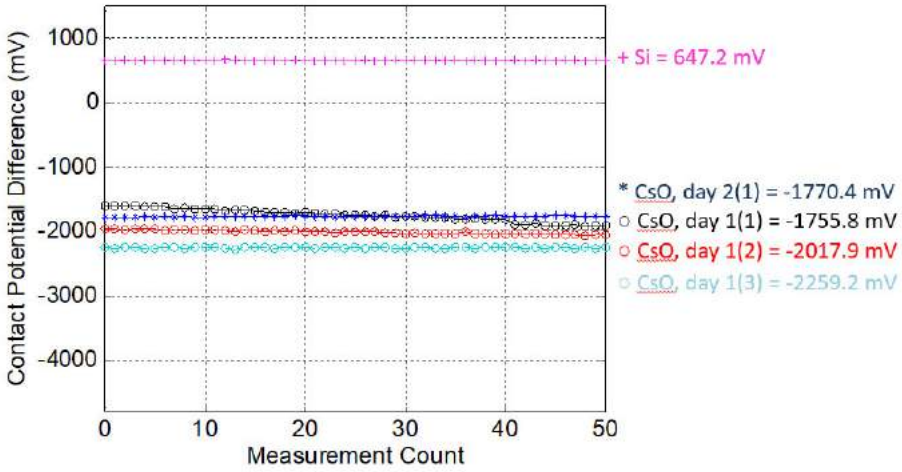

Figure 2.23: Plot of CPD measurement results

Similarly, potassium the CPD measurement repeat several times with 10 minutes interval. Finally, at the end of first day measurement the work function stabilizes at -2259mV. The work function of the cesium sample is 2eV calculated basing on the tip work function.

2.4.2 Photoemission characterization

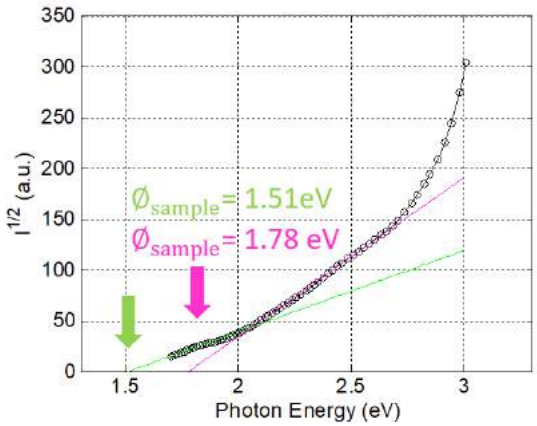

Figure 2 24: PE measurement plot for sample work function

With the same method, we have the value of the sample work function, evaluated from the plot, is 1.51 eV and 1.78 eV. The shape of the $\sqrt{I}$ vs $h\nu$ photoemission curve rarely reduces to a simple linear

curve. However, a two regimes seem to emerge. These two regimes can arise from a compound surface with emission at two different thresholds.

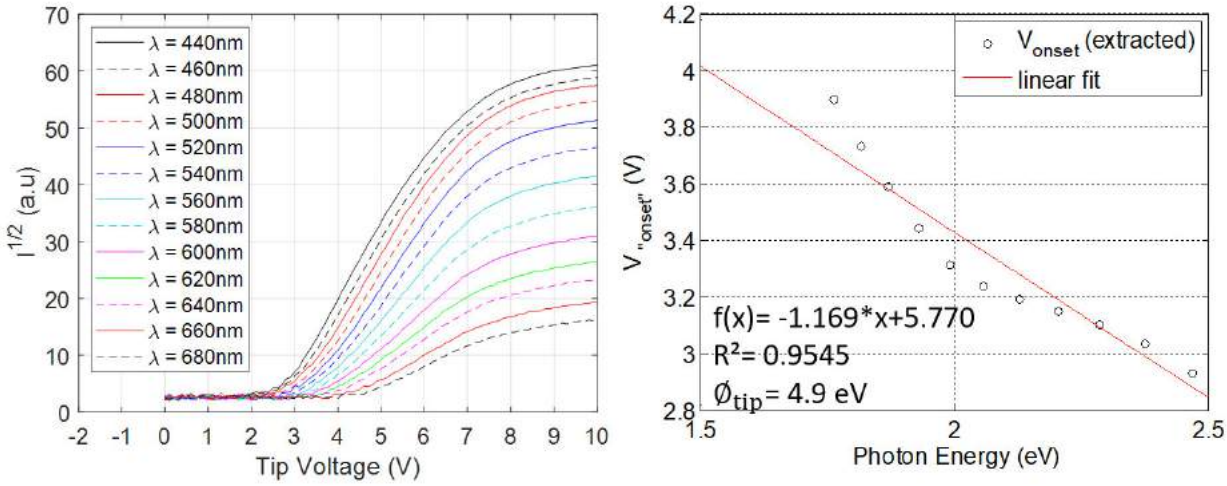

Figure 2.25: PE measurement plot for tip work function (a) $\sqrt{I} - V$ plot at various wavelength (b)$V_{onset} - photon\ energy$ and linear fitting plot

With the help of off null measurement and Eq 2.23, we can do a linear fitting based on the V_{onset} values. The Curve Fitting application module in Matlab can operate linear fitting on every curve of photo current. The intersection of the fitting line and abscissa axis are the V_{onset} value under each wavelength. Then fit one more line in Figure *2.25*(b), the tip work function is found to be 4.9eV.

2.4.3 Thermionic emission characterization

Thermionic emission characterization in this section has an assumption of the tip temperature remain stable at a much lower temperature than the sample. Which means at given distance, 12.5mm between the tip and sample, the temperature difference assumed to be the sample temperature minus room temperature. This assumption will be further studied in chapter 3.

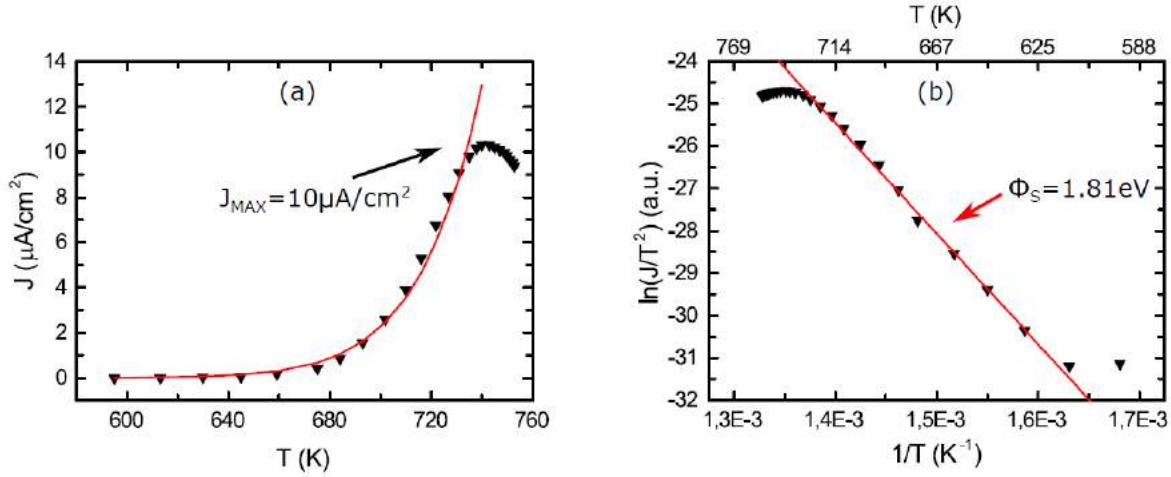

Figure 2.26: Caesium oxide TE experiment. (a) Plot of thermionic current density as a function of the temperature, fitted with Richardson's equation, using values extracted from Arrhenius plot. (b) Arrhenius plot.

Figure 2.26 (a) shows the plot of the current density versus the temperature and the current density Arrhenius plot present in Figure 2.26(b) for a typical Cs samples. The sample work function is evaluated analyzing the latter plot: $\emptyset_{sample} = 1.81\ eV$. The evolution of J is depicted in Figure 2.26(a): the thermionic current density starts increasing at $\mathrm{T} = 680\mathrm{K}$ and reaches its maximum, $10\ \mu\mathrm{A}/cm^2$, at $743\mathrm{K}$. Again, the Richardson's curve (solid line in the same figure) reproduces thes experimental data trend.

It is worth noting that the cesium oxide cover sample presents a critical temperature, $T_C = 750K$, above which the current density decreases. This behavior was observed in each sample, with the critical temperature being between $700\mathrm{K}$ and $800\mathrm{K}$. It is our opinion that the current drop is an indication of a modification in the film structure and composition. [Moulder 92][Dolle 90] In order to study the reversibility of the annealing below T_C, we performed the measurement heating the sample at three different temperatures: 700K, 750 K, 800 K. The sample inertial cooled to room temperature before each temperature ramp. An example of this process, proving the reversibility of the annealing, is depicted in Figure *2.27*: the sample was still emitting current if the temperature of the previous annealing did not exceed T_C.

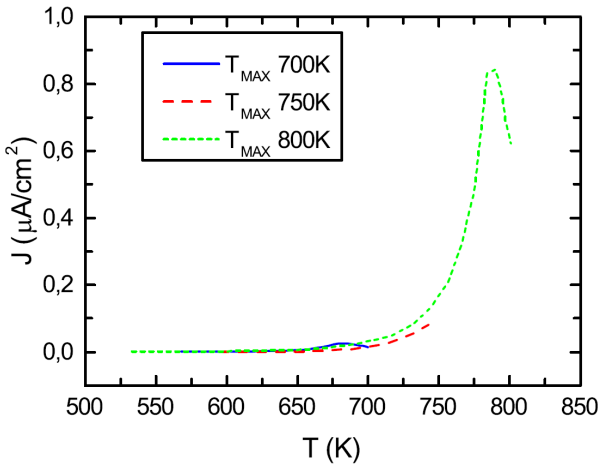

Figure 2.27: Cesium oxide thermionic emission plot. Measurements of current density as a function of temperature with three temperature ramps: 700K, 750K and 800K.

2.4.4 SEM-EDX characterization

Several SEM and EDX were performed trying to find a Cesium oxide film that has higher X-ray signal represent Cesium element compared to other position on the Silicon surface. Although some film-like pattern was found, no significant higher EDX signal showed in the corresponding area. It may be the trace of cesium film after the releasing of cesium element when the sample was exposed in atmosphere. At beginning, a p-doped silicon (100) wafer was cleaned. Then using an aluminum film to cover part of the surface. Transfer the sample into the ultra-high vacuum chamber and performed deposition with standard receipt. From Figure *2.28*(a), we can locate clearly the border of deposited and no-deposited area. Due to the cesium oxide film is thin and fragile, by using stainless steel tweezers, a scratch was manually created with light force. The Figure *2.28*(b) shows the closer view in to the scratch. The scratch pass from left-bottom corner to up-middle at the picture. Then we can find clean silicon surface at the bottom and some residual material nearby.

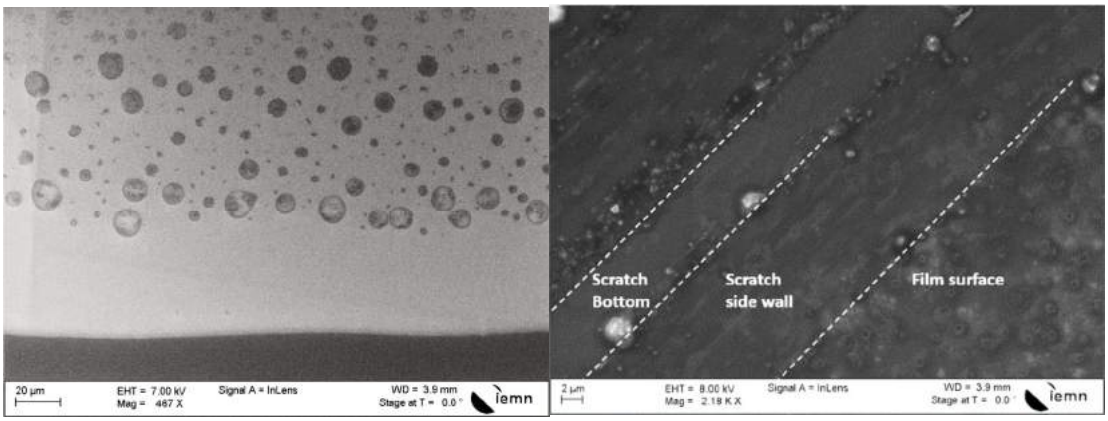

Figure 2.28: (a) SEM photo on the border of cesium deposited (up) and no cesium deposited area. (b) SEM photo on the scratch position.

No significant result from these SEM-EDX analyses from the CVD deposited cesium film. This is due to the unstable material feature at atmosphere and no chemical bond built between silicon subtract and cesium element. A further study based on ALD sample will present great difference.

2.4.5 XPS spectrum characterization

Same as potassium oxide, XPS characterization were also carried out on cesium oxide two times. One for sample right after deposition and another for sample after annealing. By comparing the complete spectrum of both measurements, we conclude that the annealing up to 800K, does not change the elemental composition of the potassium oxide film. Figure *2.29* present right after deposition sample characterization results, including the complete XPS spectrum and three critical spectrum position. In Figure *2.29*(b) O1s spectrum, showing an intense peak at 533.27 eV, interpreted as the presence of SiO2 [Lamontagne 95], and a second peak at 531.81 eV, corresponding to Cs2O2, then the two peaks in Cs3d5 spectra further confirm the presence of Cs_2O_2 [Fakult 10]. The Si spectra at 103.4eV proves the presence of the silicon oxide.

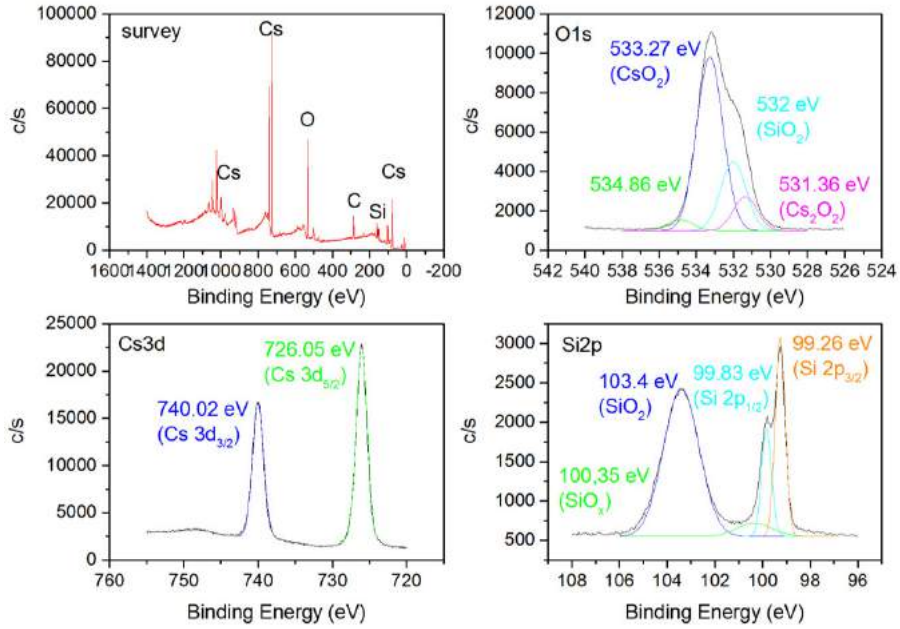

Figure 2.29: XPS spectrums after deposition. (a) Complete XPS spectrum; (b) O1s spectra; (c) Two peaks in Cs3d5 spectra; (d) Si2p spectra.

2.5 Cesium oxide with ALD process

Cesium oxide coating realized by chemical vapor deposition is usually not stable and quite fragile. As the atomic layer deposition are known for its stable film in atomic scale, we have contacted Pr. Mikko Ritala from University of Helsinki and try to cooperate with them to create a film of Cesium Oxide with only few nanometer sicknesses with a stability in high temperature and atmosphere environment. It is known that the chemical vapor deposition methods we used for coating is not suitable for industrial production. On the other side, atomic layer deposition with good conformal ability and sickness control the best methods for this application. Searching for experts in atomic layer deposition, the cooperation with University of Helsinki began. The plan to realize a Cesium Oxide with good stability, the initial coating material is Cs_2CO_3 with or without same kinds of protection. First, the cesium carbonate is stable at room temperature. Then the property of Cs_2CO_3 that will decompose to cesium oxide and carbon dioxide in high temperature is what makes it interesting to our application. In this way, the cesium oxide can be formed inside vacuum chamber in the control of a radiator.

The sample was crystal clean and visually uniform Figure *2.30 (c)*, once it was out of reactive chamber for ALD. Then, by the time pass the color changes and Lines of defects appear. Finally a crystalized irregular pattern formed like Figure *2.30 (b)*. Although it is not as stable as we wanted, the uniform film still stay in atmosphere for a good few minutes which is better than film fabricated by CVD technology.

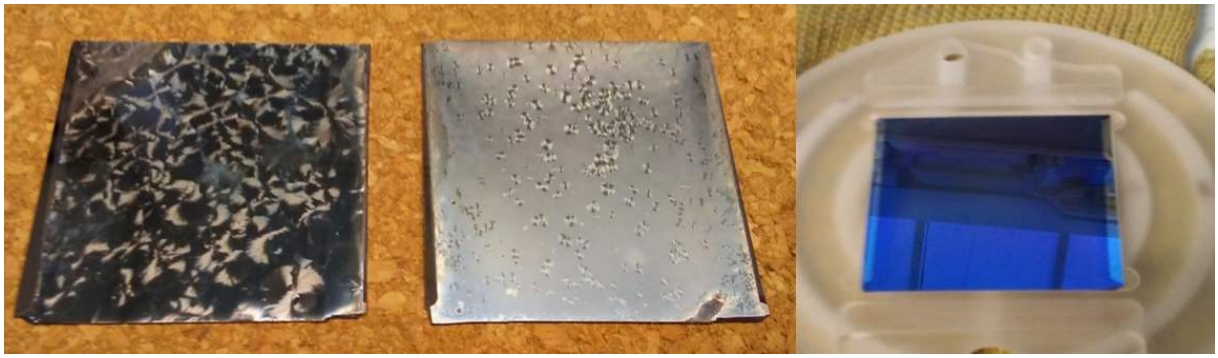

Figure 2.30: Left, sample of Cs2CO3 with a layer of Al2O3 (b) middle, sample of Cs2CO3 without protection (c) right, same sample just out of ALD vacuum chamber

2.5.1 Contact potential difference with Kelvin probe

All the later characterization was carried on the sample received from University of Helsinki. The original ALD material was supposed to be Cs_2CO_3 without Al_2O_3 protection present in Figure *2.30*.

Figure *2.31* shows the results of CPD measurement. The two 'day1' measurement were carried out right after introducing into UHV chamber (result presented in red line) and one hour later (result presented in black line). A thermionic emission test was applied three times from day 2 to day 5. What we expect is due to the annealing of temperature up to 800K, carbon dioxide was released under heat from Cs_2CO_3 and left cesium oxide on the surface. The CPD results proves that the element remain at the surface were cesium oxide which has a lower work function. As cesium oxide has lower work function than original Cs_2CO_3, the CPD value keeps dropping after each annealing process.

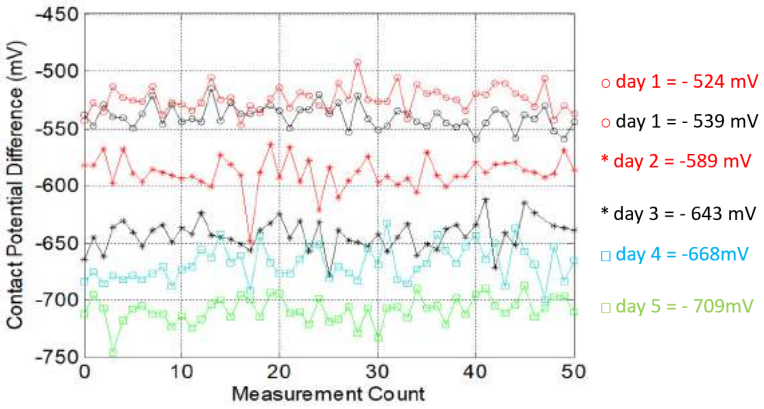

Figure 2.31: CPD measurement plot on Cs2CO3 atomic deposited sample

Then according to our standard workflow, photoemission measurement is applied after CPD measurement. Photoemission failed on atomic layer deposition samples due to no photocurrent detected through the tip and consequently no signal found by the system.

2.5.2 Thermionic emission characterization

Four thermionic emission measurement by Agilent semiconductor parameter analyzer

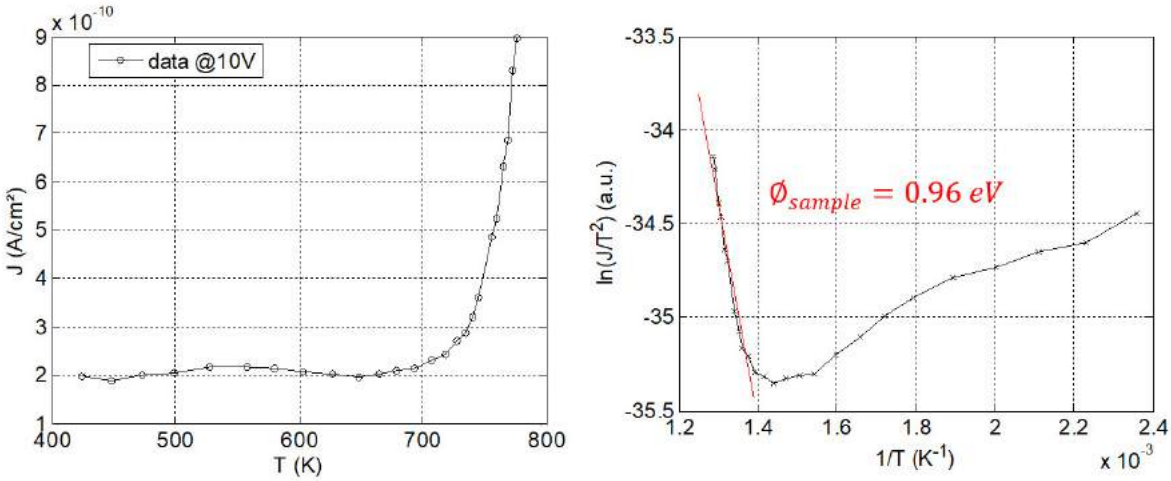

Figure 2.32: ALD Cesium oxide TE experiment. (a) Plot of thermionic current density as a function of the temperature. (b) Arrhenius plot.

With same thermionic emission measurement method, the work function results are $0.96\,eV$, $0.96\,eV$ and 0.996eV.

From Figure *2.33*, we found that thermal current changes greatly during the first TE measurement. Beginning from the end of first TE measurement, the thermionic current are highly identical. Same as the value of work function, these values are fluctuating in a range of less than 0.4eV. According to the thermionic experiment based on CVD deposited sample, this remaining material with lower work function may perform better in high temperature.

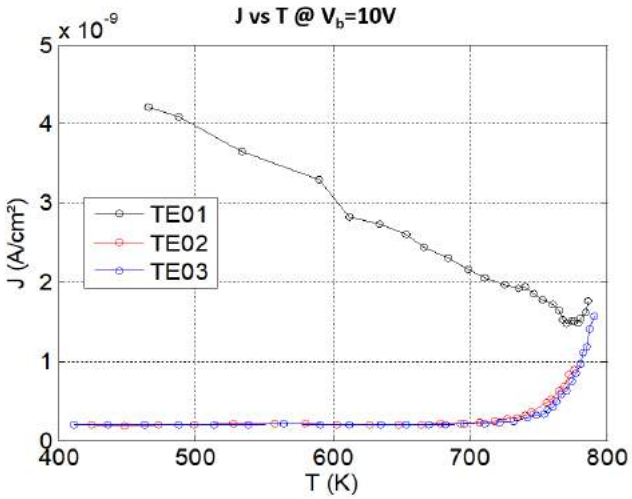

Figure 2.33: ALD Cesium oxide TE experiment.

For both second and third TE measurements, the thermionic current starts increasing after 700K during the heating process and at the maximum temperature of 780K the thermal current still has the same trend. Trying to find the critical temperature T_C like CVD deposited cesium sample, we heat the sample at maximum power for more than one hour and the maximum temperature at 805K, the gradient of thermal current curve keeps increasing. With the radiator power limitation, the maximum temperature is still below the critical temperature which mean this cesium oxide as much better stability.

With lower work function and better stability at high temperature, is it a better material? Investigating the thermionic current plot, we find that the current density at same temperature are 3 order less than the best CVD deposited Cesium sample. At this stage, our opinion is at the given temperature range (below 800K), the ALD cesium may not be a better candidate for MTC.

2.5.3 SEM-EDX analyses

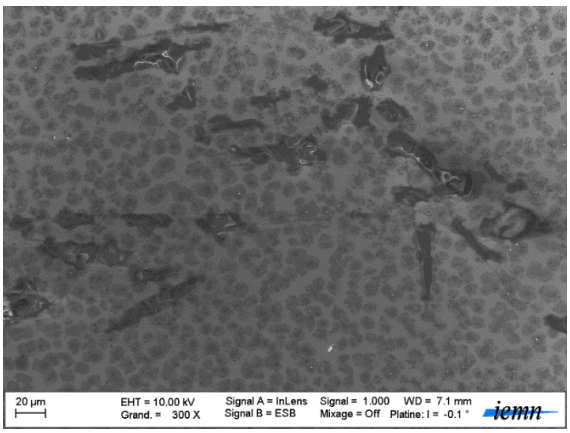

Figure 2.34: SEM image of large-scale view.

After all the in chamber characterization processes, the sample was again exposed to atmosphere, like how it was transported form Helsinki. Then we did a SEM-EDX as usually, hoping that we can find an observable structure under microscope and conformed to be Cesium by EDX signal.

Figure *2.34* present the general surface appearance of the film, which is very inhomogeneous. Few crystallites can be found on the surface and also under the black openings. These may be the crystalized cesium, which are the interest points for EDX measurement. The pattern on flat surface has similar shape compared to the SEM image in Figure *2.28(a)*. In some darker pattern, crystal structures can be found. We interpret it as crystalized cesium. Then by scanning these crystal structure positions, showed in Figure *2.35*, 4 times stronger signal than regular position are presented. Before this, we have tried several time with the CVD deposited cesium sample but no significant result shows a significant increase in cesium element signal. This is the first time that on coating surface crystallites are found and defined as a cesium component.

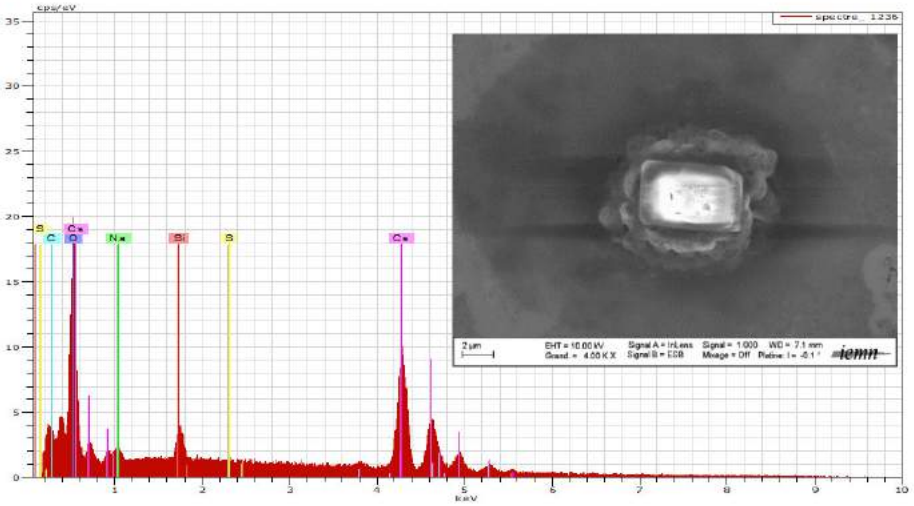

Figure 2.35: SEM image and EDX spectrum at rich cesium element position.

Figure *2.36* present a suspected structure for cesium component. We observe a crystal structure underneath a scratch. However, after investigation, only a feeble X-ray signal corresponded to cesium. This means that like other deposition position little cesium element is distributed here.

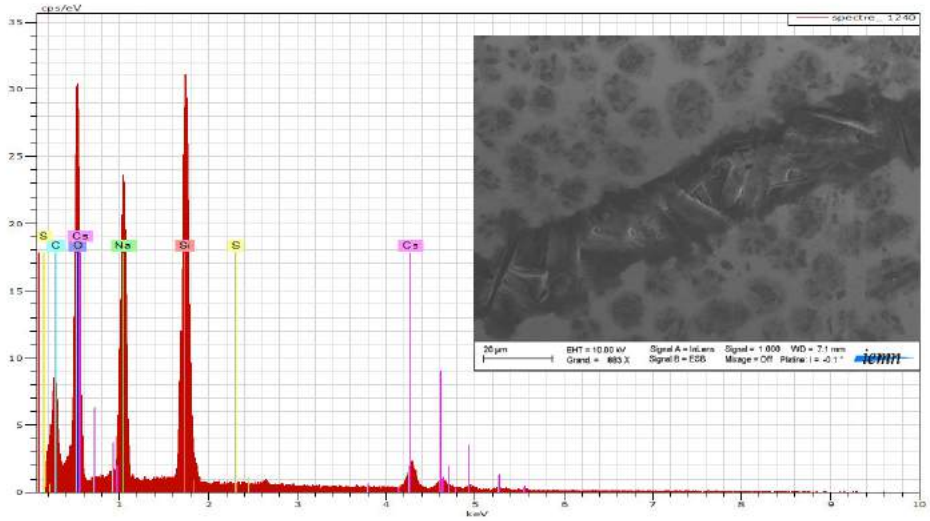

Figure 2.36: SEM image and EDX spectrum at less cesium element position

2.5.4 XPS analyses

Same XPS measurement was carried out on the atomic layer deposition sample presented in Figure *2.37*. The component before annealing was expected to be Cs_2CO_3 and the component after annealing was expected to be some type of cesium oxide. Sodium pollution was found on the ALD sample, this might due to package and transportation process. Cs signal is less important compared to CVD samples, which can be interpreted as the proportion of cesium atoms in Cs_2CO_3 is less than cesium oxide film deposited by CVD. If compared to the XPS measurement result, the signal represent cesium, carbon and oxide changed. Same as CVD samples, cesium signal declined due to some extend of material evaporation during annealing process. The signal intensity of cesium is 15% smaller after annealing presented in Figure *2.37(c) and (d).* In Figure *2.37(b)* the peak of O1s is slightly shifted which indicate a change of neighborhood for the oxygen atoms in components. In Figure *2.37(e),* the C1s peaks changed significantly. This proves that carbon is one of the critical element in the chemical reaction during annealing process, which is what we expected.

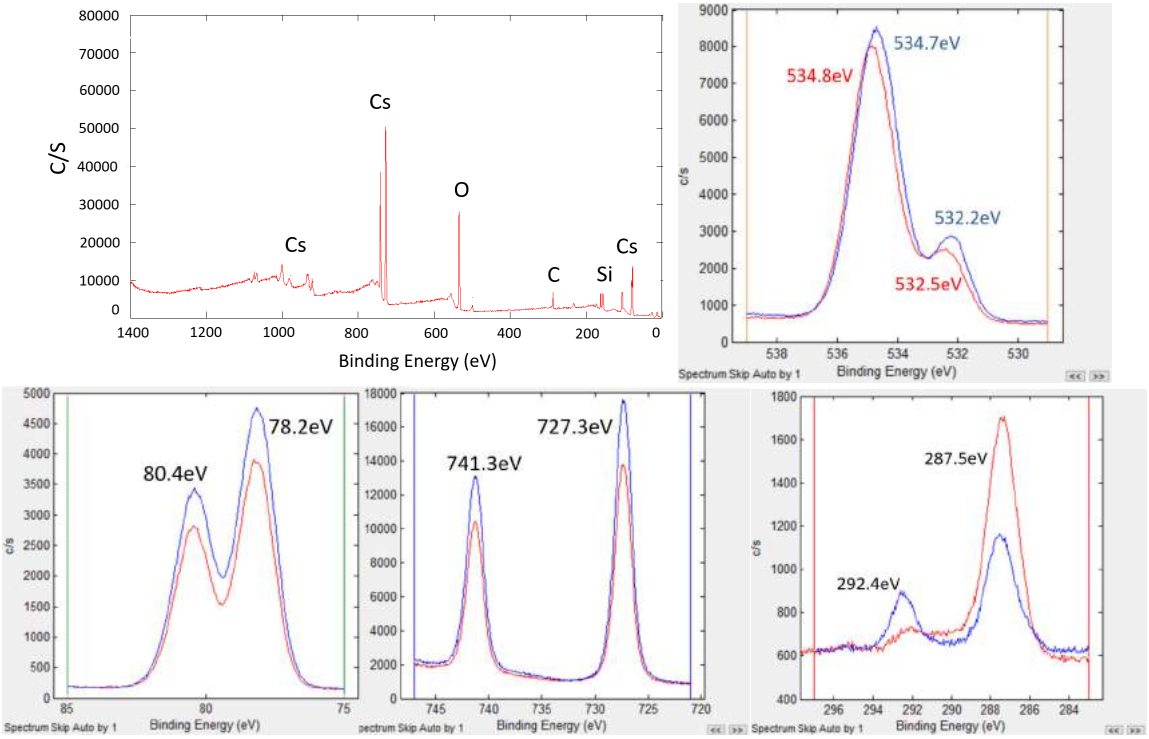

Figure 2.37: XPS spectrums after deposition. (a) Complete XPS spectrum; (b) O1s spectra; (c) Peaks in Cs3d5 spectra and (d) spectra of Cs4d; (e) C1s spectra.

2.6 Chapter summary

The objective of this chapter is to illustrate the principle of work function and present the characterization workflow with results on three different types of samples, including chemical deposited potassium oxide, cesium oxide and atomic layer deposited cesium oxide. In the very beginning of this chapter, as presented, all the CPD measurement are based on the tip work function. The tip work function is a value given in the manual and can be measured by photoemission. In Figure *2.18* and Figure *2.25* we present two typical examples of the analysis. In the first example, the square root of the photocurrent was collected by the Kelvin probe as the voltage V_b varied from +3V to +10V, while the sample was illuminated by monochromatic light in the range λ = 560:720 nm. The intercept

of the linear fit of the slopes of the I-V cures and the χ-axis gave the values of V_0, then plotted in Figure *2.25* (b) as a function of hν. The intercept of the line fitting V_0 points and the energy axis, gave $\emptyset_{tip} = 4.51\text{eV}$. The measurement was performed multiple times during various deposition campaign at different experiment stages, obtaining a mean value for $\emptyset_{tip} = 4.39 \pm 0.62eV$. This value is comparable with the value $\emptyset_{tip} = 4.764\ eV$, given by the Kelvin probe manufacturer.

The deposition and characterization of potassium repeat seven times, and the values of $\emptyset_{sample}$ extracted by the measurements on all the potassium coating experiments are $1.73 \pm 0.16\text{eV}$, for photoemission experiments, and $1.75 \pm 0.28\text{eV}$, for thermionic emission experiments. The results of photoemission and thermionic emission measurements are comparable. The maximum current density was $3.6\ \mu\text{A}/cm^2$ at 799K, harvested by the kelvin probe tip on a potassium oxide covered sample applying $+10\ \text{V}$ to the tip, at the highest temperature reached for that experiment.

With seventeen cesium samples, our conclusion is: the thin film of cesium oxide gave $\emptyset_{sample} = 1.66 \pm 0.27\ eV$, for photoemission experiments, and $\emptyset_{sample} = 1.72 \pm 0.2\ eV$, for thermionic emission experiments. The values are comparable. The highest achieved current density for these samples was $12.8\ \mu\text{A}/cm^2$ at $698\ \text{K}$.

With the sample, fabricated by ALD and from university of Helsinki, we find that the atomic layer deposited material has better stability at high temperature and at atmosphere. Although, for MTC the working temperature with this coating method is much higher than CVD coating processed, it has enough potential to become a good candidate for MTC. The TE measurement result for this material is $\emptyset_{sample} = 0.98 \pm 0.02\ eV$. With ALD cesium oxide sample and by comparing to previously deposited Cesium sample image, we also confirmed the pattern of Cesium oxide film after break the ultrahigh vacuum and reload in to SEM chamber. The EDX signal is a further evidence.

The XPS measurement results that the potassium and cesium were well coated on the sample with CVD in-situ process. Both potassium and cesium oxide are composited by multiple alkali oxide. The confirmation of oxide chemical structures is difficult and unreliable, because changing pressure and temperature may lead to the evaporation or crystallization of the thin film composition. XPS measurements on ALD cesium sample represent a chemical reaction with carbon element as what we expected. It happens during the annealing process and has no significant influence on cesium, which is interpreted based on the little change on cesium XPS signal. By XPS measurement, we confirmed that the annealing up to 800K, does not change the elemental composition of the oxide film. However compound structures will change during the process.

We compared the performance of potassium and cesium oxides film as low work function coating for MTC electrodes. We compared same element cesium with different coating technics and processes. We demonstrated that a low sample work function (< 2 eV) can be achieved for both materials and processed, having similar $\emptyset_{sample}$ values. Therefore, the silicon work function can be decreased by around 3 eV. Moreover, we obtained significant thermionic currents at relatively low temperatures, applying low voltages to the probe/sample system. The XPS study performed on the coated samples was fundamental to demonstrate that cesium oxides composition changes above its critical temperature.

The comparison of the performances of potassium and cesium oxides brought to the conclusion that cesium oxides film is a preferred material for MTC electrodes coating. In the experimental temperature range, cesium oxides provide higher thermionic current at lower temperature, with maximum values of $12.8\ \mu\text{A}/cm^2$ at $698\ \text{K}$, with respect of potassium oxides film, $3.6\ \mu\text{A}/cm^2$ at 799K.

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Chapter 3 Structure, Technical indicators and the Finite Element Method MTC modeling

Although, in theory, the MTC has little to no thermal leakages and not like other thermoelectric generator that need to balance between electron-crystal electrical conductivity and phonon-glass thermal properties, thermal leakages also need to be carefully considered in real devices. Furthermore, not like TEGs, the heat gradient direction of MTCs are perpendicular to the wafer surface. A considerable temperature difference, ideally over 100 degrees, need to be build up over less than ten-micrometer distance. This is the biggest challenge for the real MTC devices. To meet this demand a layer of both electrical and thermal insulation material is needed between electrodes, which at the same time provides structure stability.
This chapter focuses on possible structures and correspondent parameters for the conception of a prototype with maximum efficiency in real experimental conditions. Multiple Finite Element Modeling were performed to explore the technical indicators for an efficient MTC with acceptable amount of thermal leakages and best temperature difference between two electrodes.

3.1 Introduction

In the previous chapter, two promising candidate elements potassium and cesium have been tested and analyzed. A systematical explanation of deposition process and theory of each measurement has been presented, proving that the alkali metal oxide thin film is a good solution for MTC electrodes surface coating. However, like all other thermal energy generator, materials are not the only key point for building a good device. Micro-structure design is the other crucial part. In this chapter, presentation will be focused on the discovering of technical needs for the construction of MTC structure with special attention on the influencing of thermal conduction. These includes:

- Concept a structure with good thermal efficiency and compatibility with Industrial microelectronics manufacturing
- Our approach to a dedicated design
- Simulation for parameters of the very first prototype

In the first section, a review of existing TC and MTC structures will be presented including the analyses of those structures' benefits and limitations, considering the state of arts.

In the second section, models will be built and presentation of this report will focus on MTC parameters in relation with thermal efficiency. Then, within the industrial technology capability of micro fabrication of semiconductors, possible MTC designs will be presented with detailed illustration and commends. Then details of thermal conductivity study with COMSOL multi-physics finite element analysis will be in this section. The FEM began with the thermal emission data acquired from the characterization of alkali metal oxide in the last chapter. The interrelated results proves the reliability of the applied thermal model. Then detailed modeling processes and calculation results provide great help to the perfection of design. This simulation will be a critical step forwarding the conception to a functional prototype.

At the last of this chapter a structure of MTC with all optimized parameters and expected thermal performance with be designed. This structure present will be possible for massive industrial fabrication and with decent thermal efficiency at the same time.

3.2 Theoretical Calculation of Maximizing Efficiency

3.2.1 Forward/backward emission and open loop voltage

After the presentation in chapter 1.4.3 and chapter 2.2.3.3, we know that the thermionic current in an ideal situation can be calculated by the following equation:

$$\mathrm{J} = J_{H\to C} + J_{C\to H};\quad J_{H\to C} = \mathrm{A}T_H^2 \exp\left(-\frac{\Phi_H}{kT_H}\right);\ J_{C\to H} = \mathrm{A}T_C^2 \exp\left(-\frac{\Phi_C}{kT_C}\right) \qquad \text{Eq 3. 12}$$

This equation for the ideal situation represents pure thermo-electronic emission. The net current density is consider as the sum of current density from hot side to cold side and from cold side to hot side. In the equation Φ represent the potential barrier height which is between the vacuum level of current source and the highest barrier in the gap. The space charge effect, which is ignored in the equation, is the key phenomena responsible for the decrease of the current density. This is due to the repulsion of negative charges in the inter-electrode space, which creates a barrier and stops the thermo-emitted electrons with lower kinetic energy from arriving at the other electrode.

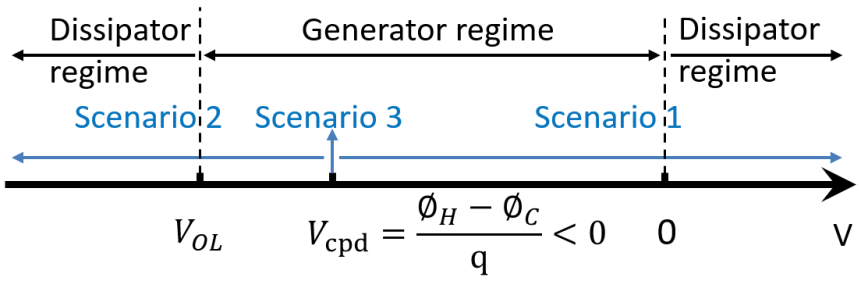

Figure 3.1: Outline of discussion: energy diagram scenarios and MTC working regimes.

The ideal MTC has three possible working scenarios based on vacuum level of electrodes. Presenting in Figure *3.1*, these three working scenarios have been identified together with three thermo-electronic working regimes. The first case corresponds to the emission of a majority current from the hot electrode. In the second case, the MTC has a majority current generated by the cold electrode. The last case is a unique and special scenario, in which the total current equals to zero and vacuum levels of electrodes are position closely with a difference resulted from Fermi-Dirac distribution. The Fermi-Dirac distribution at two different temperatures dominate this vacuum levels miss-alignment, which lead into a dynamic equilibrium. Here we use $\Delta \mathrm{E}$ to represent this energy level misalignment by the electrodes' different temperature.

- For the first scenario, $\mathrm{V} > \frac{\emptyset_H - \emptyset_C}{q}$ and V is the potential difference between two electrodes which is the same as V_b in chapter 2.2. In this case, electrons emitted from hot electrode to cold electrode compose the majority of the thermo-current. Assuming that the work function of both hot electrode and cold electrode is ultra-low and work function of cold electrode is even lower than the hot electrode. We have two energy band diagrams of this working state the Figure 3.2 and Figure 3.3.

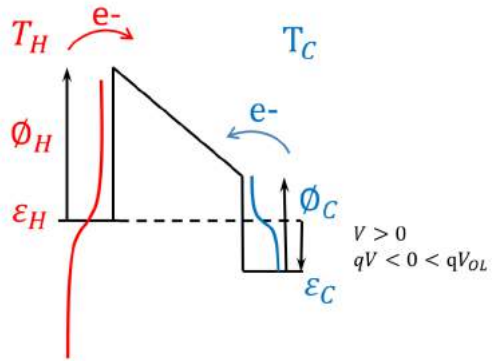

Figure 3.2: Energy band diagram of ideal MTC at $V > 0$ and $V > \frac{\emptyset_H - \emptyset_C}{q}$, when the majority of thermo-current is electrons emitting from hot to cold electrode. (The dissipator regime)

Assuming $\emptyset_H > \emptyset_C$, $\emptyset_H - \emptyset_C$ is a positive value. If V_{OL} represents the open loop voltage of ideal MTC, we have $qV < 0 < qV_{OL}$ and $0 < \mathrm{q}V < \emptyset_H - \emptyset_C < \mathrm{V}_{OL}$ two sub-case. In Figure *3.2*, the ε_H is the Fermi level of hot electrode and ε_C is the Fermi level of cold electrode. The potential difference in between two electrodes is presented by the relative position of these two Fermi levels. The work functions are presented as $\emptyset$ with arrow lines length represent the value of work function. The red and blue curve is the Fermi distribution at different temperatures. With a potential lower the Fermi level of cold electrode, it is obvious that electrons emitted from hot side dominate the thermionic current in this scenario.

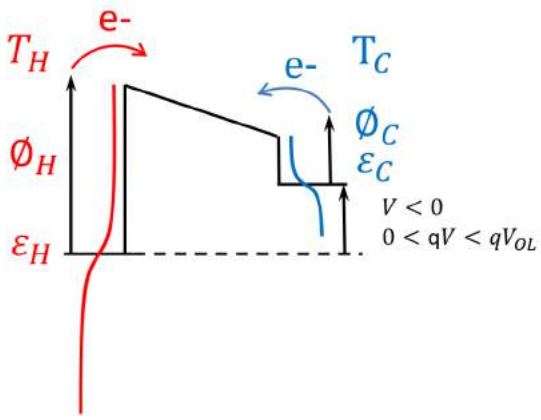

Figure 3.3: Energy band diagram of MTC at $V < 0$ and $V > \frac{\emptyset_H - \emptyset_C}{q}$, when the majority of thermo-current is still electrons emitting from hot to cold electrode. This happens only when $\emptyset_H - \emptyset_C > 0$. (The generator regime)

Same as the previous energy band diagram presented, at $\mathrm{V} < 0$ and $V > \frac{\emptyset_H - \emptyset_C}{q}$ situation, the dominant current is the thermionic current from hot electrode to cold electrode. In both of the two sub-scenarios, the total current between two electrodes is equal to the difference between anode and cathode, which is:

$$J_{total(a)} = j_{H\to C} - j_{C\to H} = \mathrm{A}T_H^2 \exp\left(-\frac{\emptyset_H}{kT_H}\right) - \mathrm{A}T_C^2 \exp\left(-\frac{\emptyset_H - qV}{kT_C}\right) \qquad \text{Eq 3. 13}$$

The $\emptyset_C$ in the second term of Eq 1. 1 is replaced by $\emptyset_H - qV$, because it is the real barrier height electrons need to overcome in order to be emitted from cold to the hot cathode.

- For the second scenario, we have the potential between electrodes $\mathrm{V} < \frac{\emptyset_H - \emptyset_C}{q}$ and the corresponding energy band diagram is the Figure *3.4*.

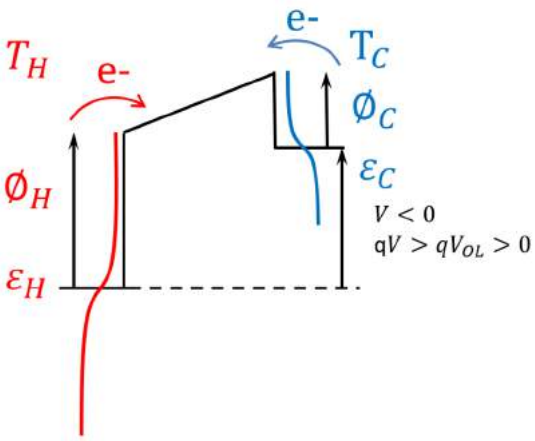

Figure 3.4: Energy band diagram of MTC at $V < 0$ and $V < \frac{\emptyset_H - \emptyset_C}{q}$, when the majority of thermo-current is emitting from cold to hot electrode. (The dissipator regime and generator regime)

In the second scenario, the dominant current is the thermionic current from the cold electrode to hot electrode. The total current can be presented by Eq 3. 14.

$$J_{total(b)} = j_{H\to C} - j_{C\to H} = \mathrm{A}T_H^2 \exp\left(-\frac{\emptyset_C + qV}{kT_H}\right) - \mathrm{A}T_C^2 \exp\left(-\frac{\emptyset_C}{kT_C}\right) \qquad \text{Eq 3. 14}$$

For the same reason mentioned before, the $\emptyset_H$ in the first term is replaced by $\emptyset_C + qV$, which is the effective barrier height.

- For the third and last scenario, the vacuum levels of both electrodes are equal $\mathrm{V} = \mathrm{V}_{cpd}$. However, with the temperature difference in between electrodes it is not a stable state. The Fermi-Dirac distribution tells that the hot surface will always have more electrons with higher energy than vacuum level at the Figure *3.5*(a) circumstance. So the potential will further built up and finally arrived at the open loop condition, when $\mathrm{V} = \mathrm{V}_{OL}$ the energy band diagram is presented as Figure 3.5(b).

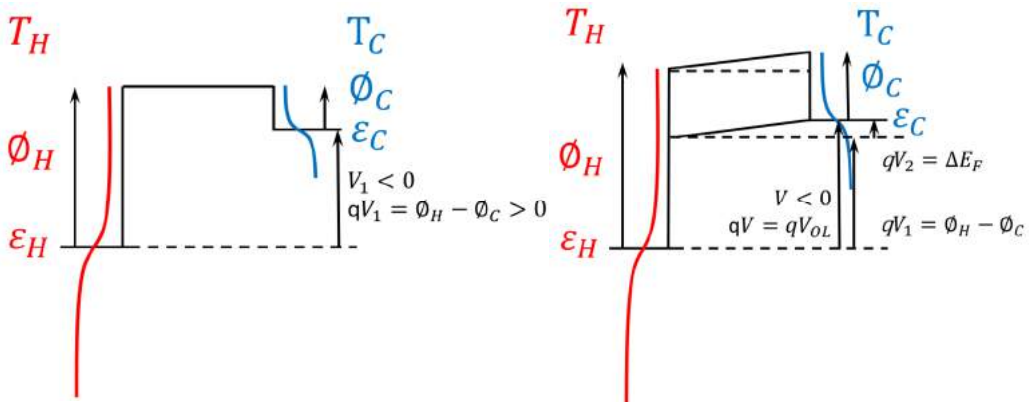

Figure 3.5: Energy band diagram of MTC (a) Vacuum level of both electrodes are aligned, where $V_1 = \frac{\emptyset_H - \emptyset_C}{q}$, (b) At $V = V_{OL}$, when the total thermo-current is equal to zero, MTC reaches a dynamic equilibrium condition.

The open loop voltage V_{OL} is a critical value for all MTCs. To calculate V_{OL} one straight forward method is based on Eq 3. 14 and Figure 3.5(b). The open loop condition represents a dynamic equilibrium condition where $J_{total(b)} = 0$, the $j_{H\to C} = j_{C\to H}$. According to these we have:

$$\mathrm{A}T_H^2 \exp\left(-\frac{\emptyset_C + qV}{kT_H}\right) = \mathrm{A}T_C^2 \exp\left(-\frac{\emptyset_C}{kT_C}\right) \qquad \text{Eq 3. 15}$$

Logarithm of the equation:

$$\ln\left(\frac{T_H^2}{T_C^2}\right) - \frac{\emptyset_C + qV}{kT_H} = -\frac{\emptyset_C}{kT_C} \qquad \text{Eq 3. 16}$$

Reorganize the equation, we have the same open loot voltage V_{OL}:

$$V_{OL} = \frac{2\mathrm{k}T_H}{q} \ln\left(\frac{T_H}{T_C}\right) + \frac{\emptyset_C}{q}\left(\frac{T_H}{T_C} - 1\right) \qquad \text{Eq 3. 17}$$

The calculation method above is based on experiment observation results. To look into the physics behind, a second method to calculate V_{OL} is illustrated below. Firstly, we will take close look at what are the factors that influence the value of open loop voltage. Assuming that the vacuum level of both electrodes are firstly aligned and temperatures are same at two electrodes. So, with the same Fermi distribution, Figure 3.5(a) can be stable if $\mathrm{T}_H = \mathrm{T}_C$. We find V_1 which is same as CPD measurement presented in chapter 2.1.3.1 which is equal to the contact potential difference value V_{CPD} when two electrodes are not connected. It is a value only dependent on the work function difference of anode and cathode. Starting from this state with the process of heating the hot electrode, thermal current

increase and the net current present in a direction from the hot to the cold side. Thermionic electrons in this process arrive at the cold side and build up a potential V_2 showed in Figure 3.5(b). The value of V_2, however, is more complicated. This voltage compensate the Fermi distribution and density of states at different temperature. To further study this value, a deep investigation of Fermi-Dirac distribution is needed. Beginning from equation of Fermi-Dirac distribution:

$$\mathrm{F(E)} = \frac{1}{e^{\frac{E-E_F}{kT}}+1} \qquad \text{Eq 3. 18}$$

Here E_F is Fermi level, k is Boltzmann constant, T is given temperature.

When a quasi-continuum of energies E has an associated density of states $\mathrm{G(E)}$ (the number of states per unit energy range per unit volume/surface), the average number of Fermions per unit energy range per unit space (volume, surface or line) is

$$\mathrm{N(E)} = \mathrm{G(E)F(E)} \qquad \text{Eq 3. 19}$$

Here $\mathrm{N(E)}$ corresponds to the highlighted triangular area with light yellow in the Figure *3.6*. In this case, the surface area represents the quantity of electrons with enough energy to be emitted and arrive to the other electrode at given temperature.

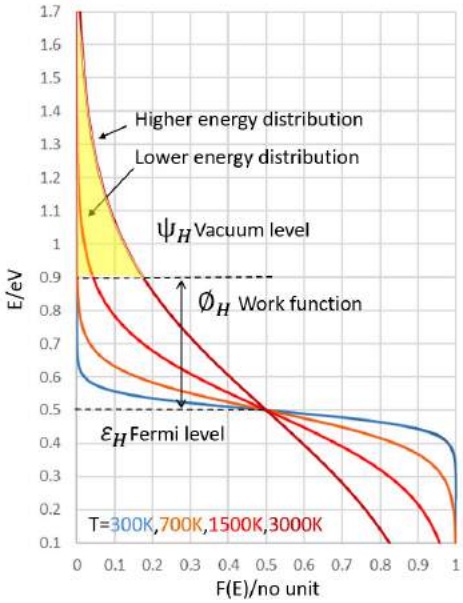

Figure 3.6 Fermi-Dirac distribution at different temperatures from 300K to 3000K. The highlighted area represent the conduction-band population of different temperature.

At $E - E_F > 3kT$, the Fermi distribution can be approximated as:

$$\mathrm{F(E)} = e^{-\frac{E-E_F}{kT}} \qquad \text{Eq 3. 20}$$

At the MTC working situation, $E - E_F > \emptyset \gg 3kT = 0.0771eV$ $(T@298K)$. For a micro gap MTC, the electrons in system can be regarded as free electrons two-dimensional Fermi gas system. The two-dimensional Fermi gas model will be proved fitting the condition later in this section. Then the effective density of states $\sigma(\mathrm{E} - \mathrm{E}_F)$ is the step-function equals to a constant proportional to temperature. With density of states and effective density of states presented below [King 05]:

$$\rho(\mathrm{E}) = \frac{m^*}{\pi h^2}\sigma(E - E_F) \propto E^0 = const. \quad \text{Eq 3. 21}$$

$$\mathrm{G(E)} = \frac{m^*}{\pi h^2}\mathrm{kT} \quad \text{Eq 3. 22}$$

Assuming the open loop voltage is composed by two part, V_1 represents the work function difference with the given working parameter of MTC, including: $T_H, \emptyset_F, T_C, \emptyset_C$. According to Figure 3.5(b) the highest barrier for thermionic electrons from hot cathode is $\emptyset_F + qV_2$, and the barrier for cold anode is $\emptyset_C$. The integration of average number per unit volume/surface in corresponding energy range can be represented following equations Eq 3. 23 and Eq 3. 24:

$$\mathrm{N}_H(\mathrm{E}) = \int_{\emptyset_H+qV_2}^{+\infty} \mathrm{G}\cdot\mathrm{F(E)dE} = (\frac{m^*}{\pi h^2}\mathrm{kT}_H) \times (\mathrm{kT}_H e^{-\frac{\emptyset_H+qV}{\mathrm{kT}_H}}) \quad \text{Eq 3. 23}$$

$$\mathrm{N}_C(\mathrm{E}) = \int_{\emptyset_C}^{+\infty} \mathrm{G}\cdot\mathrm{F(E)dE} = (\frac{m^*}{\pi h^2}\mathrm{kT}_C) \times (\mathrm{kT}_C e^{-\frac{\emptyset_C}{\mathrm{kT}_C}}) \quad \text{Eq 3. 24}$$

In open loop situation, we have

$$\mathrm{N}_H(\mathrm{E}) = \mathrm{N}_c(\mathrm{E}) \quad \text{Eq 3. 25}$$

So Eq 3. 23 and Eq 3. 24 lead to:

$$\mathrm{T}_H{}^2 e^{-\frac{\emptyset_H+qV}{\mathrm{kT}_H}} = \mathrm{T}_C{}^2 e^{-\frac{\emptyset_C}{\mathrm{kT}_C}} \quad \text{Eq 3. 26}$$

Logarithm of the equation:

$$2\mathrm{Ln}\frac{\mathrm{T}_H}{\mathrm{T}_C} - \frac{\emptyset_H+qV}{\mathrm{kT}_H} = -\frac{\emptyset_C}{\mathrm{kT}_C} \quad \text{Eq 3. 27}$$

Reorganize the equation:

$$\mathrm{qV}_2 = 2\mathrm{kT}_H\mathrm{Ln}\frac{\mathrm{T}_H}{\mathrm{T}_C} + \emptyset_C\frac{\mathrm{T}_H}{\mathrm{T}_C} - \emptyset_H \quad \text{Eq 3. 28}$$

So we have open loop voltage $V_{OL} = V_1 + V_2$

$$\mathrm{q}V_{OL} = \emptyset_H - \emptyset_c + 2\mathrm{kT}_H\mathrm{Ln}\frac{\mathrm{T}_H}{\mathrm{T}_C} + \emptyset_C\frac{\mathrm{T}_H}{\mathrm{T}_C} - \emptyset_H = 2\mathrm{k}T_H\ln\left(\frac{T_H}{T_C}\right) + \emptyset_C\left(\frac{T_H}{T_C} - 1\right) \quad \text{Eq 3. 29}$$

By using theory of Fermi-Dirac distribution and effective density of states of free electrons in 2-D Fermi gas, the result of V_{OL} is same as using Richardson's law.

Here is a simple discussion about why the effective density of states is present as 2D Fermi gas model. First of all, the Thermionic electrons are emitted and arrive at the other electrode presenting a thermal current density. The current density has directionality, which is perpendicular to the surface like presented in Figure 3.7(a). The electron emission direction can be decomposed into two vectors, $v_1$which is the projection in the direction of current density and v_2 which is in the surface of emitting electrode. The direction of v_2 in the electrode surface is define by angle θ and length v_2 showed in Figure 3.7. The angle θ wno't influence the energy distribution inside the vacuum gap. So v_1 and v_2 are two independent coordinates in the system. As a result, the average number of thermionic electrons can be fitted in the 2D Fermi gas model.

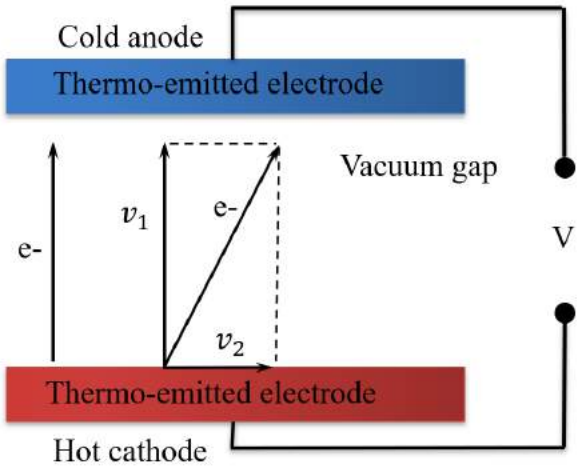

Figure 3.7: Scheme of electrons emission and movement in vacuum gap where v_1 is perpendicular to the electrodes and v_2 is parallel to electrodes. The size of electrodes is assumed infinitely large.

According to Eq 3. 17, the open loop voltage is independent to work function of cathode, $\emptyset_H$. It only depends on the temperature of electrodes and the work function of cold anode. So, which is the key factor to build up a higher open loop voltage? From Eq 3. 17, we find the possible candidates are temperature ratio, hot cathode temperature and work function of cold anode. To increase the temperature ratio makes a greater temperature difference and it may lead to near-field radiation dissipation problem and thermal isolation problem for real device. While keep the temperature ratio and only increase is even less effective as presented in *Figure 3.8*(b). The default hot temperature at 400K and cold temperature set at 300K, hot cathode work function at 0.6eV and cold anode at 0.4eV.

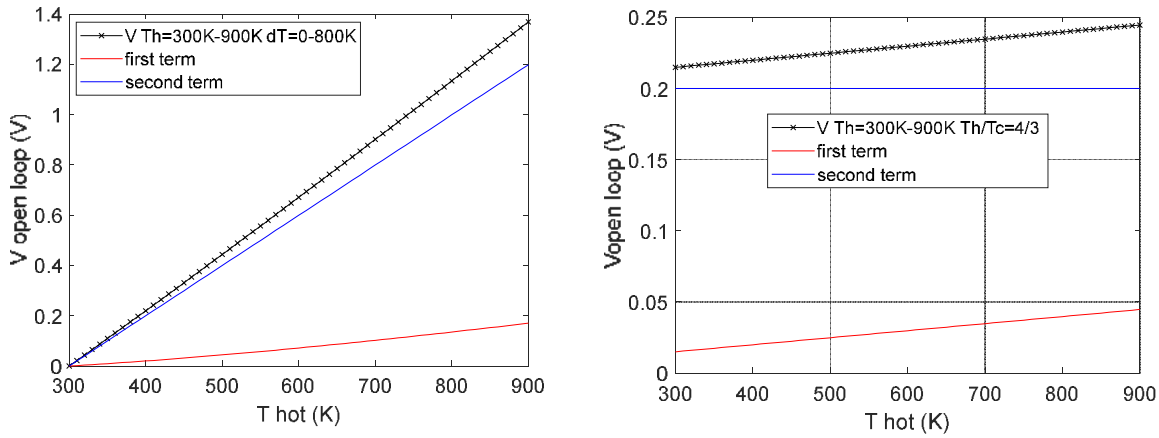

Figure 3.8 (a) Open loop voltage built up with the increase of hot cathode temperature rise and temperature ratio increase. (b) Open loop voltage barely increase with the temperature ratio stay at same level while only increase the hot cathode temperature.

Because the Eq 3. 17 has two terms, from Figure *3.8* and Figure *3.9* the contribution to build open loop voltage by each term are presented. The last and most effective way is to increase cold anode work function. This concludes that to make a real MTC prototype, the ultra-low work function may not be necessary considering the fact that open loop voltage is the maximum voltage a power generator can supply. Here appears a trade off for MTC. With $0 < \emptyset_C \leq \emptyset_H$, $\emptyset_C$ should be as high as possible to increase V_{OL}. But $\emptyset_H$ should remain low to enable high current.

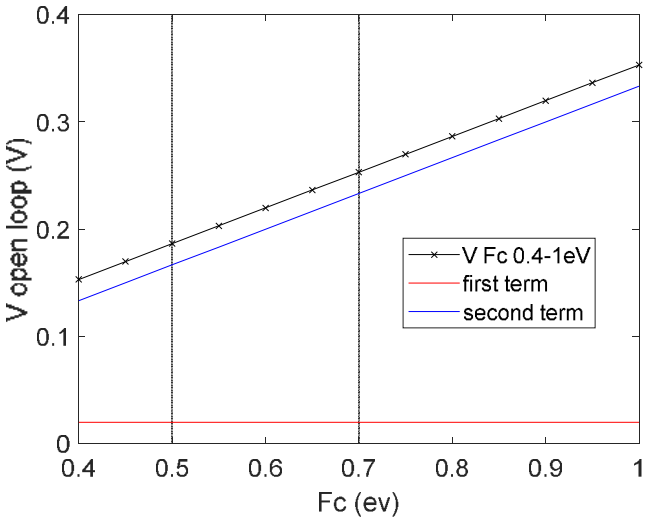

Figure 3.9 Open loop voltage as a function of cold anode work function.

The analyses of open loop voltage above has the boundary condition of $\emptyset_H$ presented below.

$$\emptyset_H \leq 2\mathrm{kT}_H \mathrm{Ln}\frac{\mathrm{T}_H}{\mathrm{T}_C} + \emptyset_C \frac{\mathrm{T}_H}{\mathrm{T}_C} \qquad \text{Eq 3. 30}$$

This means the conclusion is true not only at $0 < \emptyset_C \leq \emptyset_H$, but also work at $0 < \emptyset_H < \emptyset_C$ condition, when $\emptyset_H$ is slightly smaller than $\emptyset_C$. Once $\emptyset_H$ fit in the inequality, the MTC has a generator range no matter how small it is. This value is presented as V_2 in Figure *3.5*(b) and Figure *3.10*. In real MTC fabrication and working scenario, both the hot cathode and cold anode are coated by low work function materials and the heating process leads to a slightly higher work function at hot electrode compared to cold electrode. Therefore, the analyses in this section are always valid in our experiments. So all following discussion are based on assumption of $0 < \emptyset_C \leq \emptyset_H$.

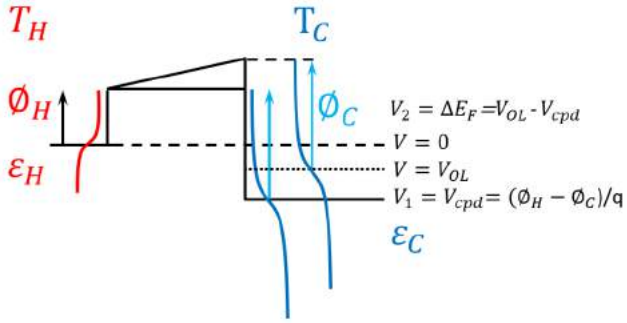

Figure 3.10 Energy diagram illustrating for open loop voltage, CPD and potential zero position, at $0 < \emptyset_H < \emptyset_C$ *condition.*

3.2.2 Ideal power density and efficiency under no space charge condition

At the beginning of previous section, three thermoelectronic emission scenarios have been presented. The first case corresponds to the emission of a dominant current from the hot electrode and the highest barrier is the work function of hot cathodes. The second case assumes that the thermoelectronic current generated by the cold electrode dominating the thermionic current with the highest barrier at the cold side. The last scenario represents a process of equilibrium. Beginning from

$V = (\emptyset_H - \emptyset_C)/\mathrm{q}$ and end into the open loop situation with no net thermal current in between electrodes. The highest barrier remains at the cold side. Analyzing the potential in between electrodes, for these three MTC working scenario, for $V_{OL} \leq \mathrm{V} < 0$, the device works as generator. Otherwise, it works as dissipator like presented in *Figure 3.11*(b). Curves in the plot are based on Eq 3. 13 discussed in the beginning of this section.

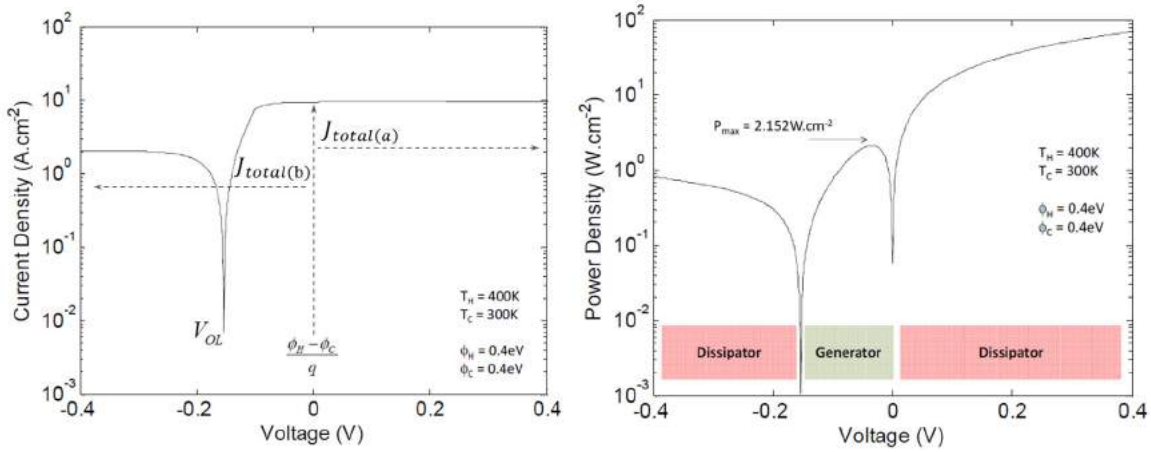

Figure 3.11 (a) current density curve in relation to the voltage between electrodes and open loop voltage. (b) Power density at corresponded voltage and three different working mode of MTC

With the calculation result of ultra-low work function material, the potassium peroxide thin film, Figure *3.11* present at hot electrode temperature equal to 400K and cold electrode remains at room temperature, the current density and power density with the relationship of MTC voltage [Wu99]. Both the cold and hot electrode are made of potassium peroxide thin film with work function equal to 0.4eV [Wu 99] [sonnenberg 69]. These hypothesis values the optimistic parameters which give the best current density results in almost the best performance for all MTC parameters. From Figure *3.11*(a) we know that the current is saturated when output voltage is greater than $\frac{\emptyset_H - \emptyset_C}{q}$. The electrical power density P, which is generated or consumed by the micro thermionic convertor, is defined as:

$$\mathrm{P} = \mathrm{J(V)} \cdot \mathrm{V} \qquad \text{Eq 3. 31}$$

Under the same condition as *Figure 3.11(a)*, the maximum useful electrical power density is higher than $2\mathrm{W.cm^{-2}}$. The corresponding heat flow used by the convertor and transported from one electrode to another electrode can be calculated by the following equation.

$$Q_{e-} = j_{H\to C}(2kT_H + \emptyset_H + qV) - j_{C\to H}(2kT_C + \emptyset_C + qV) \qquad \text{Eq 3. 32}$$

The radiative heat losses in vacuum micro gap between electrodes Q_R can be evaluated by the following equation according to black body radiation described by Stefan-Boltzmann law.

$$Q_R = \sigma_{SB}\varepsilon_0\left(\varepsilon_{rH}{T_H}^4 - \varepsilon_{rC}{T_C}^4\right) \qquad \text{Eq 3. 33}$$

In the equation ε_{rH} and ε_{rC} are the relative emissivity of electrode material. σ_{SB} is the Stefan-Boltzmann constant. The thermionic energy convertor efficiency η can be defined by the ratio between the useful electrical power generated and the total dissipated heat power. The expression is given below:

$$\eta = \frac{P}{Q_R + Q_{e-}} \qquad \text{Eq 3. 34}$$

Similarly, like other thermal engine, the efficiency is a function of hot temperature, cold temperature and the MTC working state, which is only dependent on the output voltage. The result can be compared with the Carnot efficiency given by:

$$\eta_{Carnot} = 1 - \frac{T_C}{T_H} \qquad \text{Eq 3. 35}$$

At the same condition as *Figure 3.11*, a thermoelectric efficiency of 21% is obtained within the power generator voltage range, while the Carnot limit is 25% in this case.

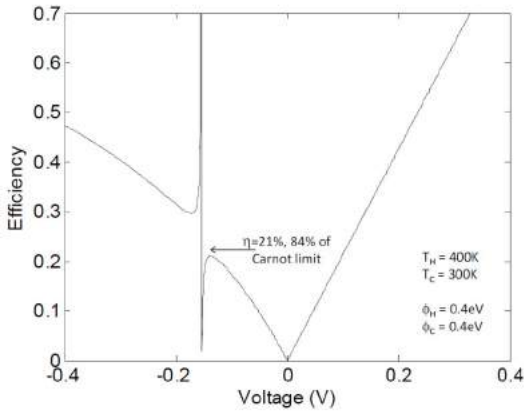

Figure 3. 12 thermoelectric conversion efficiency as a function of output voltage. The maximum efficiency is nearly at 85% of Carnot limit.

From figures above, we find that the peak efficiency appears at output voltage near open loop voltage position. In the current research and develop stage, targeting an MTC prototype with benchmark of Carnot limit is not really a goal. Rather achieving the more attractive working efficiency for MTCs at the maximum power output is preferable. This mean the thermionic energy convertor works at low power output and large voltage output with the best efficiency is a potential feature that may be further studied in future. In order to obtain the best power output possible, the best configuration for MTCs are ultra-low work function at both electrode and working at close to large temperature gradient with output voltage far lower than the open loop voltage.

3.2.3 Space charge effect

The thermionic energy convertor can work in two different modes with the vacuum gap or with a gap filled with ionized cesium steam. The reason to use ionized cesium steam is to neutralizing the space charge and consequently improve the output power. However, it also requires a much higher electrodes temperature ($> 1000\mathrm{k}$) to sustain the Cs vapor, which leads to higher thermal losses. Then our solution is to use vacuum gap thermionic convertor. In operating condition, the gap will be filled with negative charge carried by thermionic electrons and this charge lead to a higher barrier in the gap than at the energy barrier at electrodes. This barrier is named space charge effect, which is a supplementary barrier impedes efficiency.

For instance, the current density at any position x in the gap from zero to d is a stable and same value. So electrons are evenly distributed in the gap. Define ψ as electric potential. Then according to Poisson equation, the solution of $\frac{\partial^2 \psi}{\partial \mathrm{x}^2} = -\frac{\rho}{\varepsilon_0}$ is a parabola with the highest barrier position at $x = x_{\max}$.

$$\mathrm{J} = -en_e \cdot v \qquad \text{Eq 3. 36}$$

However, the simple estimation of electron distribution is not true when considering the result above. The parabola shaped potential barrier will reduce the kinetic energy of electrons at different position. Therefore, the speed of electrons v is a function of position x. This shows that charge density is not a constant and is respect to position. In Eq 3. 37, $n_e$is a function of position x.

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon_0} = -\frac{e^2 n_e(x)}{\varepsilon_0} \qquad \text{Eq 3. 37}$$

Here we have boundary conditions: $\psi(x=0)=0$, and $\psi(x=d)=U=\frac{\emptyset_H-\emptyset_C}{q}$. Then assuming that we have a value K, which is represent the electric field at the cathode. K can be written as $\frac{d\psi}{dx}|_{x=0} \equiv \frac{KU}{d}$ and K is a parameter without unit. It helps to investigate the characteristic of current flow limited by space charge effect at $x=0$. Especially, it allows identifying the maximum potential position. With$\frac{d\psi}{dx}|_{x=0}$ we have $\frac{\partial \mathrm{J(K,U,d)}}{\partial \mathrm{K}}=0$, so $\mathrm{K}=K_m$ and $\mathrm{J}_m(\mathrm{K}_m,\mathrm{U},\mathrm{d})$. Here J_m is the limit current by Child-Langmuir law (three-halves-power law). [Child 11] [Langmuir 13] [Langmuir 23] Discussion above tells that the equation has a fully coupled solution.

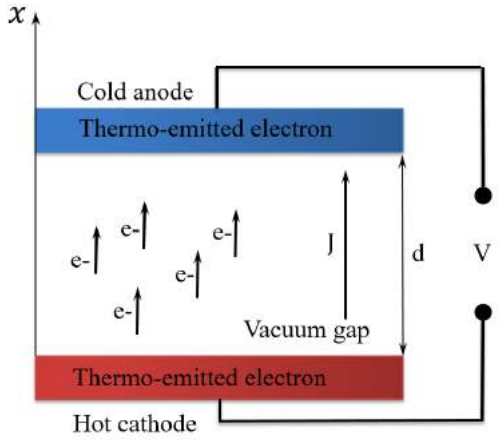

Figure 3.13 Scheme of Child-Langmuir flow: thermionic current density J is limited by the space charge effect with a potential barrier U.

In vacuum gap situation, with the following assumptions valid:

- Electrons travel ballistically between electrodes with no or little scattering.
- In the inter-electrode region, the space charge of any ions is negligible.
- The electrons have zero velocity at the cathode surface.

We have the current density under the influence of space charge effect:

$$\mathrm{J}_L = \frac{4\varepsilon_0}{9}\sqrt{\frac{2q}{m_e}}\cdot\frac{U^{\frac{3}{2}}}{d^2} \qquad \text{Eq 3. 38}$$

Where d is the vacuum gap size as presented in Figure *3.13*, *U* is potential barrier, q is the charge of the electron and m_e is its mass. $\emptyset_H = 0.6eV$, $\emptyset_C = 0.4eV$, $T_H = 400K$, $T_C = 300K$ and $d_1 = 1\mu m, d_2 = 2\mu m, d_3 = 3\mu m$.

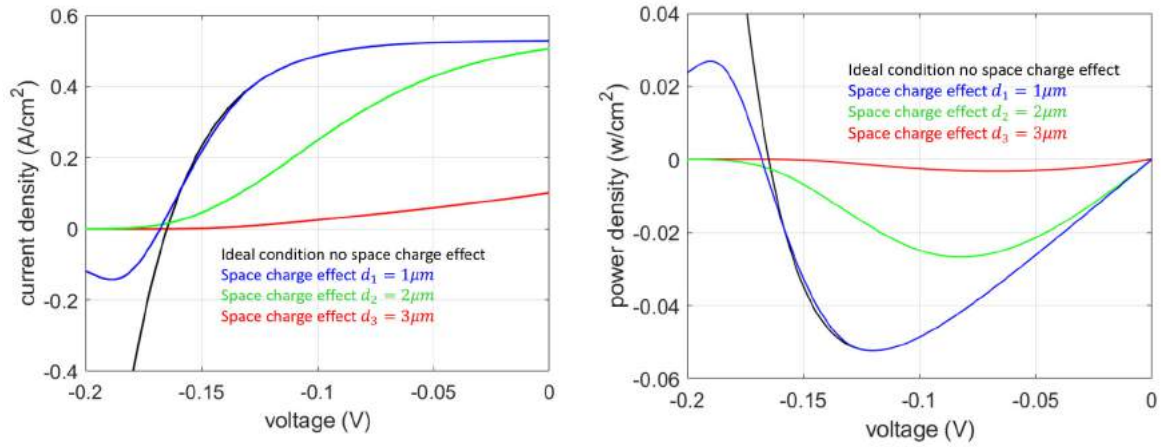

Figure 3.14(a) Influence of space charge effect for current density as a function of gap dimension d. (b) Influence of space charge effect for power density as a function of gap dimension d.

As expected we find that the space charge effect will greatly reduce the output power when the gap dimension are too large. For gap dimension larger than $1\mu m$ the influence is important. [King 04]

In order to better illustrate the influence of space charge effect, the parameters of MTC model are change to: $\emptyset_H = 0.6eV$, $\emptyset_C = 0.4eV$, $T_H = 400K$, $T_C = 300K$ and $d = 2\mu m$. In this case, the forward only curve, ideal curve and space charge curve are well separated in Figure *3.15*. The blue curve represents the thermionic current from hot to cold with assuming no thermal current backward. The red curve takes both forward and backward thermal current in to consideration. At last, the green curve includes the impact of space charge effect.

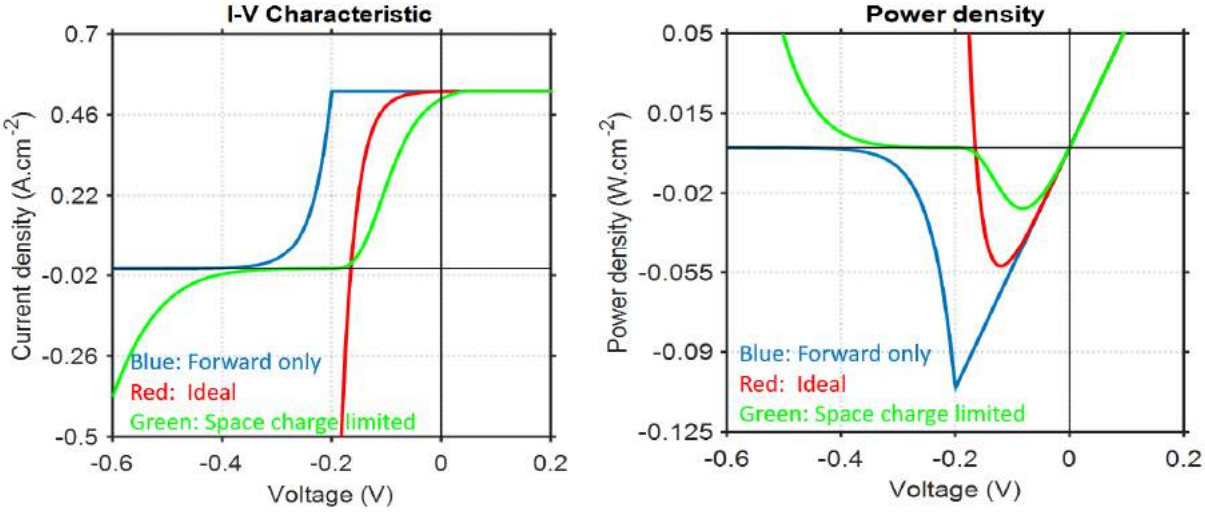

Figure 3.15(a) Comparison between forward only, ideal and space charge effect thermionic current density. (b) Comparison between forward only, ideal and space charge effect thermionic power density.

To overcome this effect, one possible solution without changing de dimension of the gap is use a strong electric field ($500\mathrm{V} \cdot cm^{-1}$). This allow a lower barrier by the Schottky effect.

3.2.4 Ideal gap dimension

After investigating the space charge effect, it is time to find out the ideal gap dimension for given MTC parameters. First, we have the electrical net output power represented as below:

$$\mathrm{P}_{net} = \mathrm{J}_{net}(\mathrm{V} - \mathrm{J}_{net}R) \qquad \text{Eq 3. 39}$$

According to the previous section, the J_{net}, the current density of micro thermionic convertor is limited by the effect of space charge. This effect increases the potential barrier and can be regarded as a local work function for both electrodes. Therefore, the effective work function of hot cathode and cold anode are:

$$\emptyset_{H,net} = \emptyset_H + \psi_H \text{ and } \emptyset_{C,net} = \emptyset_C + \psi_C \qquad \text{Eq 3. 40}$$

Here, ψ_H and ψ_C is the additional barrier height due to space charge effect for corresponding electrodes. Both of them are functions of gap dimension and in the study of net output power, they are the main reason for internal resistance. Figure *3.16* is the energy diagram present the relation between height of space charge barrier ψ and gap distance d.

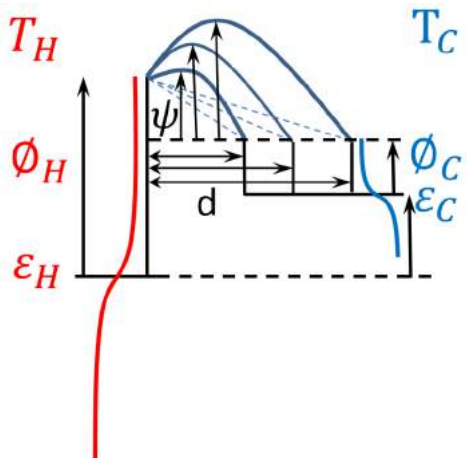

Figure 3.16 Energy diagram illustrate space charge barrier increase as the gap distance increases.

Furthermore, at given gap dimension, the thermal radiative losses can be composed by two parts. The propagative regime Q_{prop} and evanescent regime Q_{evan}. In black body radiation theory, according to Wien's displacement law, at the gap dimension smaller than the peak energy thermal wavelength, the evanescent regime is dominant; otherwise, the propagative regime is dominant. For MTC working temperature less than 1000K. The conclusions are at around and above $1\mu m$ gap dimension range, the radiative thermal losses are stable and not important. Below this range the thermal losses increase rapidly as the gap distance decreases.

$$Q_{total} = \mathrm{Q}_{e-} + \mathrm{Q}_{prop} + \mathrm{Q}_{evan} \qquad \text{Eq 3. 41}$$

So we have final expression of efficiency:

$$\eta_{total}(T_H, T_C, \emptyset_{H,net}, \emptyset_{C,net}, \mathrm{d}) = \frac{\mathrm{P}_{net}}{Q_{total}} = \frac{\mathrm{J}_{net}(\mathrm{V}-\mathrm{J}_{net}R)}{\mathrm{Q}_{e-}+\mathrm{Q}_{prop}+\mathrm{Q}_{evan}} \qquad \text{Eq 3. 42}$$

So, we have the calculation results for electrical efficiency as a function of vacuum gap and different hot temperature as presented in *Figure 3.17.* Although the impact of gap distance is less critical than the effect of temperature difference, for a constant thermal condition, the output power and efficiency are both highly relayed on an optimum gap distance.

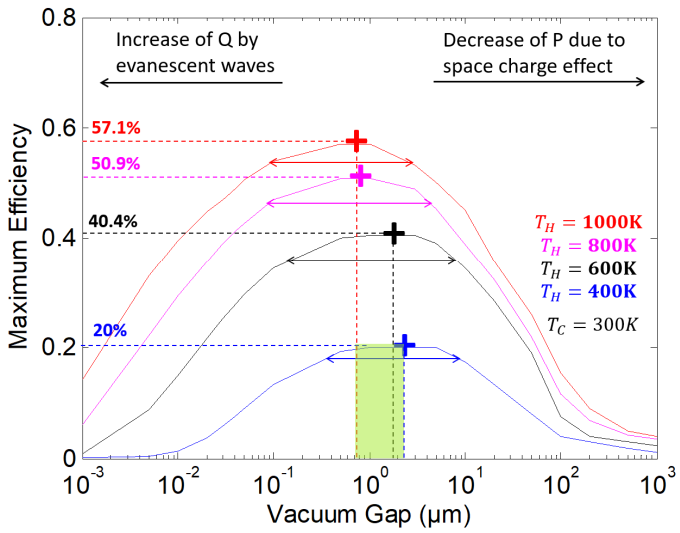

Figure 3.17: Maximum efficiency for micro thermionic convertor as a function of vacuum gap dimension. [Morini 14]

After a theoretical investigation of micro thermionic convertor, here is a short conclusion. Due to the existence of space charge effects the first generation and early exploration about one hundred years ago has failed. *Figure 3.17* presents a maximum thermal electrical convention efficiency range for vacuum gap dimension at different hot electrode's temperature. Within this interval, the thermal energy loss is not important, and the space charge effect is not significant in limiting the output power. The green rectangle represents the best gap size for a large range of hot electrode temperature. The double arrow line shows the 90% of maximum efficiency range at given temperature.

Generally speaking, at the range of 200 nm to 10 μm, the total energy flow is dominated by thermionic emission at the hot cathode temperature ranging from 400 to 1000K. As a conclusion, the maximized efficiency of MTCs has gaps dimension similar to the characteristic wavelength of the thermal radiation of the emitter, which is a function of MTCs' working temperature.

3.3 Thermal Insulation

3.3.1 Introduction

In the last section, the micro vacuum gap thermionic convertor are analyzed in a theoretical ideal way. This section, we will present another alternative approach to further understand and explore the MTC in different given working conditions with the capabilities of COMSOL's heat transfer with surface-to-surface radiation module. By selecting the hot electrode's temperature, we are able to confirm the Alkali metal work function characterization results in chapter 2. In the last chapter, during the thermal emission effect measurement, we assumed that the temperature of Kelvin probe is constant at room temperature, which is not true. Numerical simulations can also test the designs of different layout for future Nano-fabrication processes. In the mechanical domain, a micro size vacuum gap has a pillar structure in between, which will lead to significant thermal energy losses. This part of energy losses and concept a good structure for thermal isolation in between electrodes of MTC are the principle of this section. The processes of numerical simulation are common in pre-prototype investigation, and will provide fabrication indicator for a more precise and real scenario.

3.3.1.1 MTC structure compatible with Chemical Vapor Deposition

One most important factor for Micro-gap Thermionic energy Convertor (MTC) is the vacuum gap dimension. Due to the limitation of fabrication process in last century, this technical route was abandoned at that time. With the modern micro electrical fabrication processes and Silicon On Insulator (SOI) wafer available, the first solution is presented in *Figure 3.18*.

SOI is a technology wildly used in the fabrication of thin-film channels MOSFET transistors. Moreover, COMS technologies which are relying on thin –film Si layers have been successively developed thanks to the high performance and fabrication efficiency of SOI. However, unlike the industrially used Si thickness of around 6nm, the thickness of top Si layer in the fabrication of MTC has no requirement. Box in the figure represent the thermal SiO_2 in the Si based SOI wafers, which in most of cases is the dry SiO_2, located in-between the top thin-film layer of Si and the wafer's Si substrate. In this design, low work function vapor goes through the open holes and arrive at inner side of both emitter and collector during coating process. And during working time, electrons will absorb heat and evaporate from Si subtract of SOI and arrive at the SOI layer.

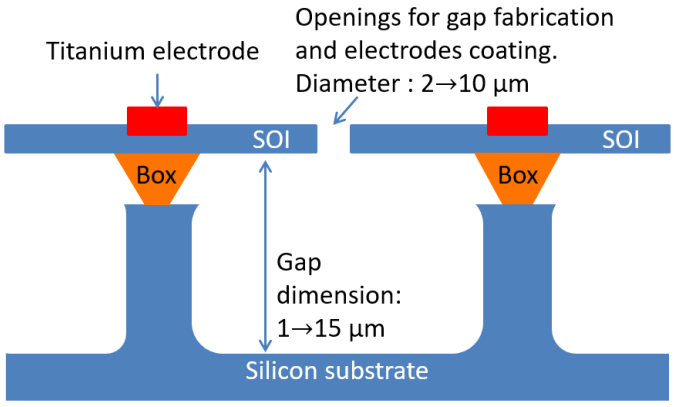

Figure 3.18: Schematic diagram of sectional view of MTC fabricated by SOI wafer.

3.3.1.2 MTC structure compatible with Atomic Layer Deposition

In the second plan, the electrodes of MTC are two separated wafers with Atomic layer deposited low work function coating. Then, two electrodes were bonded together in vacuum and Al_2O_3 as gap spacer with good thermal isolation property. The schematic diagram presented as Figure *3.19*.

ALD is, generally speaking, a subclass of chemical vapor deposition. The majority of ALD reactions use two chemicals. These chemicals react with the surface of substrate one at a time in a sequential, self-limiting manner. The target material is slowly deposited on the substrate after hundreds of this sequential cycle. As a key process in the semiconductor fabrication, ALD technology has some important features. First, it is a very controllable method to produce a film with specified thickness. Second, the growth of different multilayer structures is straightforward. Moreover, the process typically runs at a lower temperature, which is thermochemical preferred and avoid significant thermal stress in other CVD deposited film. Last, generally speaking, the film has a good stability on the substrate, which is a great advantage for the scenario of MTC fabrication.

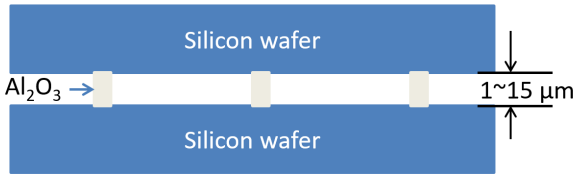

Figure 3.19: Schematic diagram of MTC structure based on ALD and Vacuum bonding technology.

Although with simpler structure and better coating film stability, this plan has a higher demand for engineer development of related device, which is more challenger than the first plan. Thanks to the collaboration with university of Helsinki, ALD coated samples can be characterized, which is presented in chapter 2.

3.3.2 FEM modeling for thermal conductivity of kelvin probe by thermal emission

The very first numerical simulation realized by COMSOL is based on an experiment presented in chapter 2. During the characterization of alkali metal work function, the third methods we used is thermal emission measurement. However, due to the sample high temperature with a close distance to the tip, the radiative heat transfer is unavoidable. Consequently, the tip temperature is no more at initial room temperature. This means that the cold electrodes has a temperature as a function of distance $T_C = f(d)$. By using the heat transfer with surface-to-surface radiation COMSOL module, we are able to calculate the tip temperature.

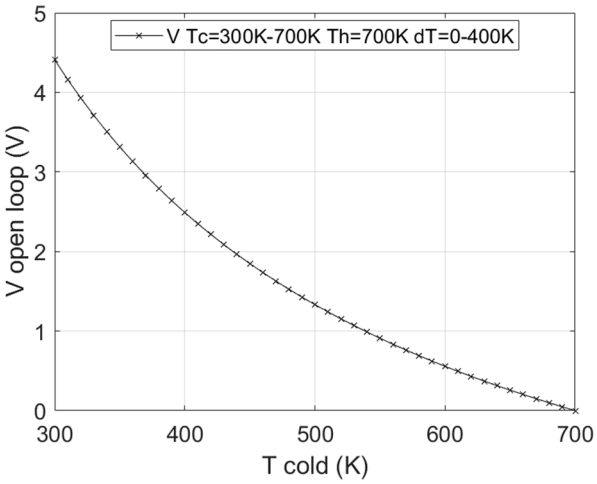

Figure 3.20: The open loop voltage as a function of cold electrode's temperature. Calculation results based on Eq 3.18 of chapter 3.2.

In order to make experimental results and simulation results comparable with each other, the thermal emission experiment is modeled. The hot sample is kept at given temperature controlled by the DC power supply unit. In this case is about 700K. The tip starts to measures thermionic current from a large distance of 40mm from the sample. After each measurement, the tip is moved towards the sample for 2.5mm until reaching a distance of 2.5mm. During this process, the tip is gradually heated up, as distance to the heated sample is decrease. We assume that the hot electrode has stable work function, same as cold electrode and the sample remains at a constant temperature during the whole process. From Eq 3.18 we know that with the increase of temperature at cold electrode and lower temperature difference, the open loop voltage decreases. It is presented in Figure *3.20*.

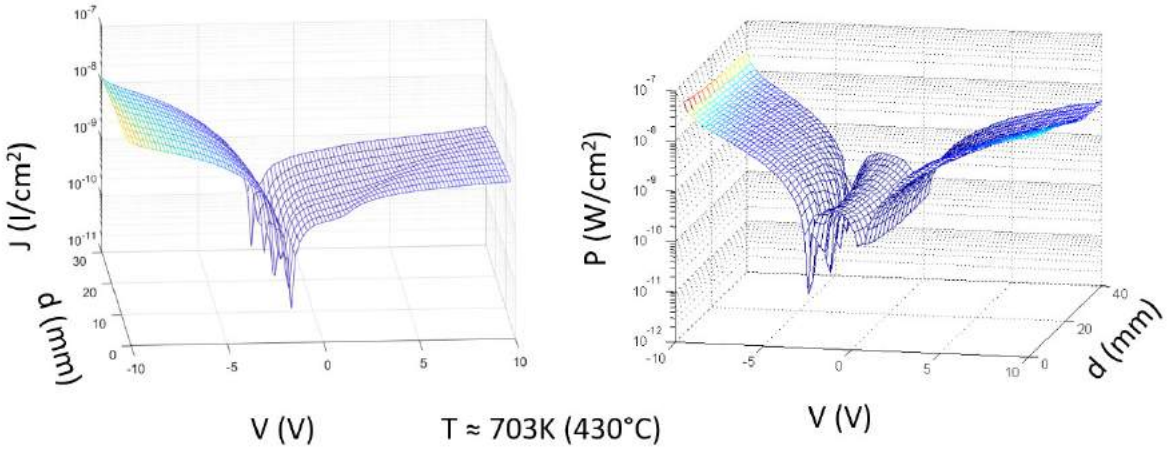

Figure 3.21: Measurement results of modified thermionic emission characterization. (a) Current density plot, (b) power density plot.

Figure *3.21* is the results of tip approach measurement. The open loop voltage decreases after each step and the maximum power output position located at the farthest position. With the above data, a plot presenting the relationship between open loop voltage and tip-sample distance can be present in a 2-d plot. Figure *3.21* shows the trend between open loop voltage and tip-sample distance. Ignoring the first five points that has close distance, all the rest points present a clear increasing relationship.

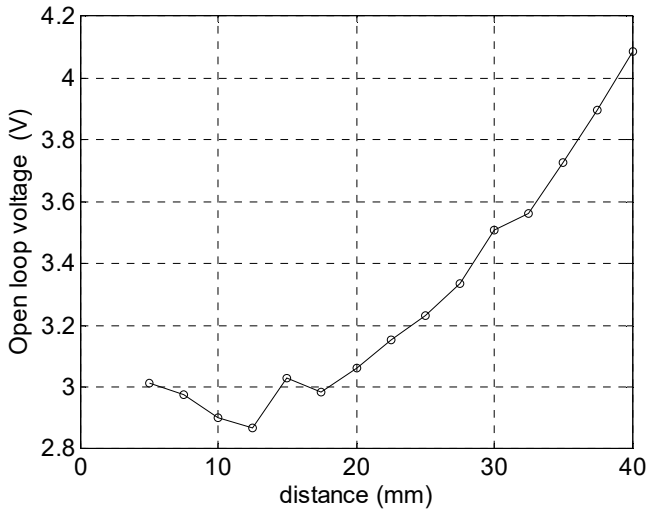

Figure 3.22: Open loop voltage is decided by the temperature difference, which is a function of tip-sample distance.

With the CPD and photoemission measurement, both the sample work function and tip work function at the moment is calculated: $\emptyset_H = 2eV, V_{cpd} = 1.23mV$. (Same process showed in Chapter 2)

The next step is FEM simulation for temperature at the cold electrode. Beginning from model building. The tip-sample model is built in an axis symmetrical way. According to the Kelvin probe manual, the tip has a diameter of 1mm assuming the other side of the tip is in contact with the shell of vacuum chamber, which stays at a default room temperature of 293.15K. The sample with the radiator module is simplified to a cylinder with 1 cm height and 6cm diameter. Due to the heating process, the module bottom side is at 700K as the initial condition. The ambient pressure set at 10^{-9} bar. To calculate the radiative heat transfer, emissivity of all related surface and material are necessary. The emissivity

coefficient ε indicates the radiation of heat from a 'grey body' instead of the black body that has an emissivity coefficient equals to one. According to table.1, emissivity of silicon-related materials at different temperature, at about 700K range for both p-doped and n-doped silicon, the emissivity stays at 0.5 to 0.7.

Emissivity of Silicon-Related Materials **1603**

Table I. Results of Simulations of Emissivity as a Function of Temperature for Wavelengths of Interest for Pyrometry (Doping Concentration, of 10^{17} cm^{-3} for n-Si and p-Si; Thickness, 700 μm)

Temp.	30°C		200°C		500°C		700°C		1000°C	
$\lambda(\mu m)$	n-Si	p-Si	n-Si	p-Si	n-Si	p-Si	n-Si	p-Si	n-Si	p-Si
0.8	0.672	0.672	0.667	0.667	0.657	0.657	0.651	0.651	0.643	0.643
0.9	0.677	0.677	0.673	0.673	0.661	0.661	0.651	0.651	0.635	0.635
1	0.681	0.681	0.678	0.678	0.667	0.667	0.658	0.658	0.644	0.644
1.1	0.282	0.28	0.649	0.649	0.671	0.671	0.663	0.663	0.65	0.65
2.4	0.051	0.076	0.104	0.137	0.385	0.385	0.68	0.68	0.677	0.677
2.7	0.068	0.099	0.116	0.148	0.441	0.441	0.682	0.682	0.679	0.679
3.4	0.08	0.116	0.105	0.141	0.518	0.518	0.684	0.684	0.684	0.684
4.5	0.179	0.24	0.244	0.289	0.61	0.61	0.685	0.685	0.689	0.689
10.6	0.548	0.582	0.602	0.602	0.689	0.689	0.689	0.688	0.692	0.692

Table 3. 1 Emissivity of silicon-related materials at different temperature and for different doping. [Ravindra 01]

The tip is considered as stainless steel, by checking the database of emissivity coefficient, which has a range from 0.54 to 0.63 for steel type 301. By setting all boundary of both tip and sample as diffuse surface and the result is presented in *Figure 3.23*(b).

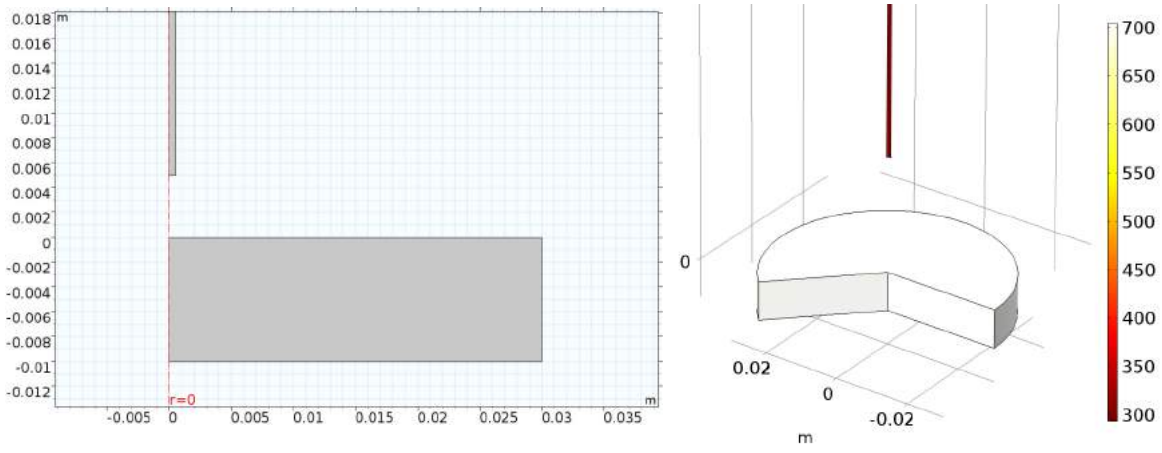

Figure 3.23: (a) axis symmetrical model, (b) 3-d plot of simulation visual result.

After the first simulation, the distance is modified as a variable changing from 5mm to 40mm with a step of 2.5mm. All other parameters kept unchanged. We have the temperature as a function of sample-tip distance plot, presented in *Figure 3.24*.

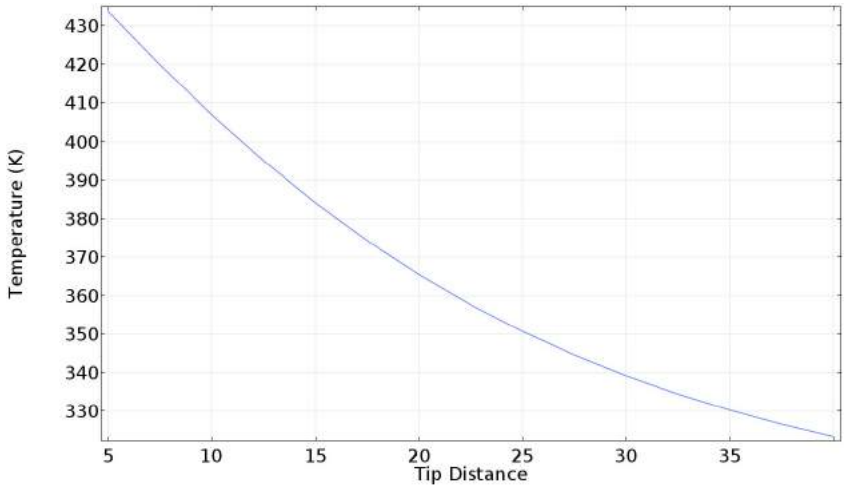

Figure 3.24: Simulated cold electrode's temperature as a function of tip distance.

Eq 3.18 tells that the open loop voltage is a function of two temperatures and cold electrode work function at given condition, which can be present as:

$$V_{OL\,calculated} = \mathrm{F}(T_H, T_C, \emptyset_C) \qquad \text{Eq 3. 43}$$

In order to fully benefit from the numerous open loop voltage values, a fitting of calculated voltage values with the result of simulation are fitted to the measurement voltages presented in Figure *3.25*. Using the linear fitting equation Eq 3.32.

$$V_{OL\,measured} = a\mathrm{F}(T_H, T_C, \emptyset_C) \qquad \text{Eq 3. 44}$$

From previous measurements we have $\emptyset_H = 2eV, V_{cpd} = 1.23mV$. The cold work function is 3.23eV, and we find with $\emptyset_C = 3.23eV$, the theoretical calculated results and the thermal emission measurement results match each other. One thing need emphasize is that the open loop voltage measured results is from the combination of TE measurement results and FEM temperature modeling results. The linear fitting has a good variance $R^2 = 0.92$, when the gradient $a = 0.99$. This is one of the good result, which proves the established thermal modeling has a good compatibility with real experimental scenario.

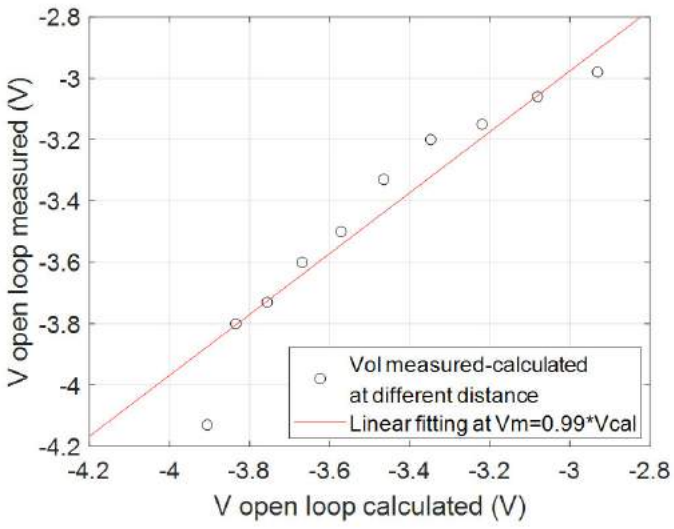

Figure 3.25: Fitting plot between the calculated open loop voltage based on FEM results and the measured results.

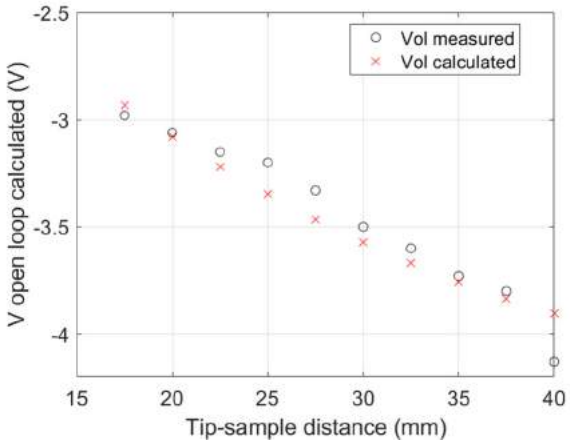

Figure 3.26: Measured and calculated open loop voltage as a function of tip-sample distance.

Comparing Figure *3.26* with Figure *3.20*, with the tip-sample distance proportional to the cold electrode temperature, the curves of open loop voltage are in good agreement.

3.3.3 COMSOL modeling for heat flux through contacts by conduction

The first conception of an MTC with Microelectronics manufacturing processes is based on Silicon On Insulator wafers (SOI) presented in 3.3.1.1. Unlike pure silicon wafers, SOI has three layer of materials. The top layer is silicon with small thickness from tens of nanometer to hundreds of nanometer, which is also named as SOI layer. The second layer is insulator named as box layer, usually silicon dioxide for a thickness larger than first layer. The substrate is silicon, and the total thickness is around 800µm. By using the SOI, we have membrane fabrication process of integrated micrometer platform for thermoelectric measurements [Haras 14]. With the E-beam lithography and two-step isotropic gas etching, a micrometer gap with silica and silicon pillars as mechanical supports can be built. Section view scheme of MTC with micro gap structure is presented in Figure *3.27*. Nanofabrication process and manufacturing details will be present in Chapter 4.

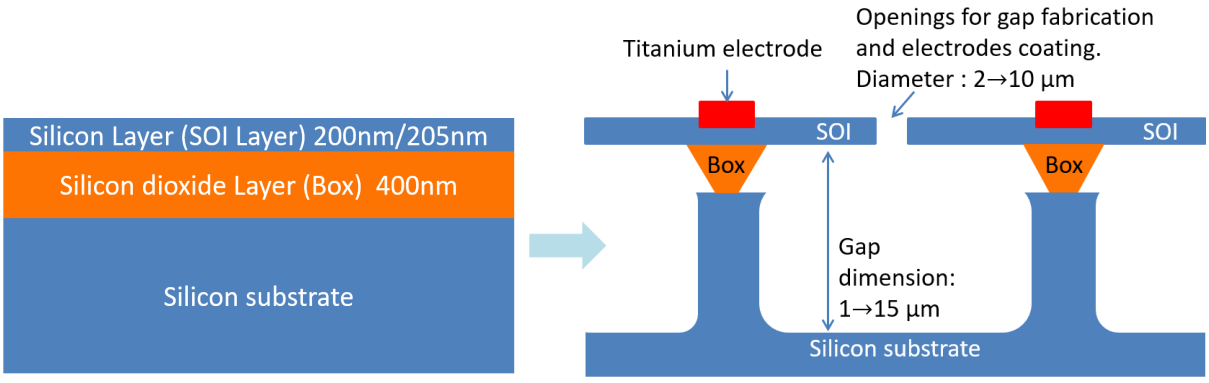

Figure 3.27: MTC conception based on SOI wafer and section view of final MTC structure.

The first simulation is focused on the heat flux through the pillar and the temperature difference between silicon substrate and membrane. Although silica is a good thermal insulator, heat flow through the 400nm thickness silica by heat conduction is not negligible. According to the previous calculation for thermal dissipation, the thermal losses through pillar by heat conduction will be 5 to 6 order greater than radiation heat flux. So to minimize the pillar heat flux is crucial during layout

conception is important. Fortunately, by using the COMSOL numerical simulation heat flow and temperature difference can be calculated, which helps in modifying and improve the design.

First of all, due to the matrix arrangement for cavities openings and the two-step isotropic gas etching, the pillars for final device will have a pattern of matrix same as cavities openings. So for modeling the sample, only one cell of the whole device is enough representative.

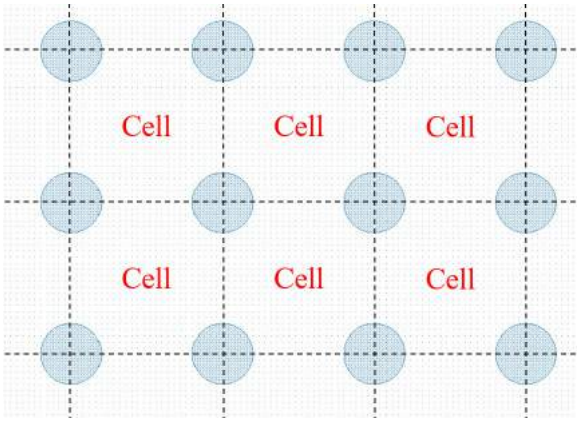

Figure 3.28: Pattern of SOI opening, pillar under SOI lay will located at center of each cell

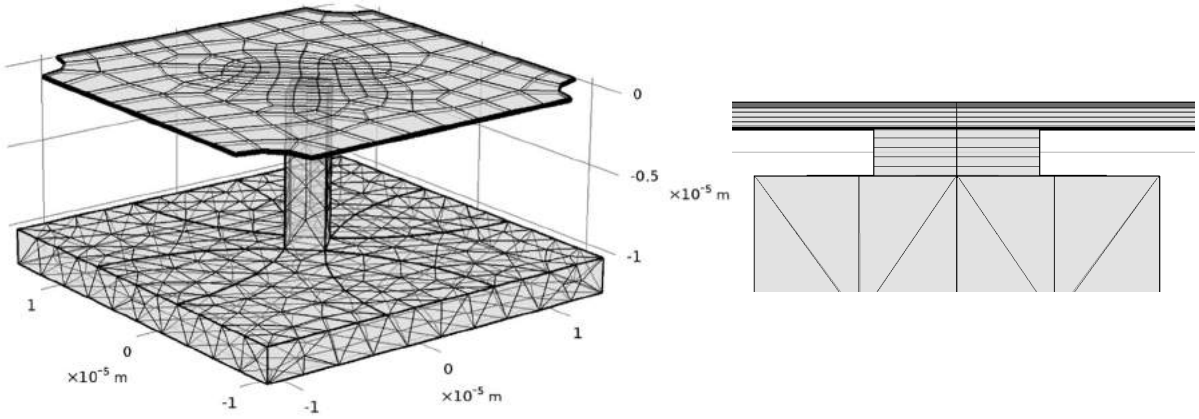

Figure 3.29 (a) The mesh of simulation cell. (b) Details of manually controlled mesh for thin geometry structures.

Then, for the first model, the openings are $3\mu m$ radius circle-shape holes and surface of silica at top of pillar is $1\mu m^2$. The symmetrical cell has a side length of $25\mu m$ and total surface $625\mu m^2$. The gap between SOI layer and cavities bottom has a dimension of $10\mu m$. Same as FEM modeling in previous section, the emissivity of silicon and silicon dioxide are set to 0.7 and 0.79 [Ravindra 01] and all other properties values from the COMSOL library.

With the database of 200/400 SOI, the z-axis dimension are much smaller than two other dimension. So in the mesh process, a special distribution is applied on the SOI layer and BOX layer. Figure *3.29*(b) shows that both layer are manually set to five layers of mesh. This helps to increase calculation efficiency and leads to a more accurate result. Compared to Figure *3.29*(a), the manually controlled layers has a much higher mesh density at z-axis direction.

Figure *3.30*(a) shows the global temperature distribution of the cell model and *Figure 3.30*(b) present the detail temperature gradient from silicon pillar to silica pillar together with temperature of SOI layer. The absolute temperature different is only 3K between top and bottom layer. Most of gradient are located at the silica pillar position, which is caused by much large thermal resistance for silica. The total

heat flux at z component on silica-SOI interface is $1.43 \times 10^{-2}\ W/cm^2$. The radiation thermal flux at top surface of SOI is $1.0 \times 10^{-2}\ W/cm^2$. According to different simulation results, these are two critical values proportional to the corresponding SOI surface.

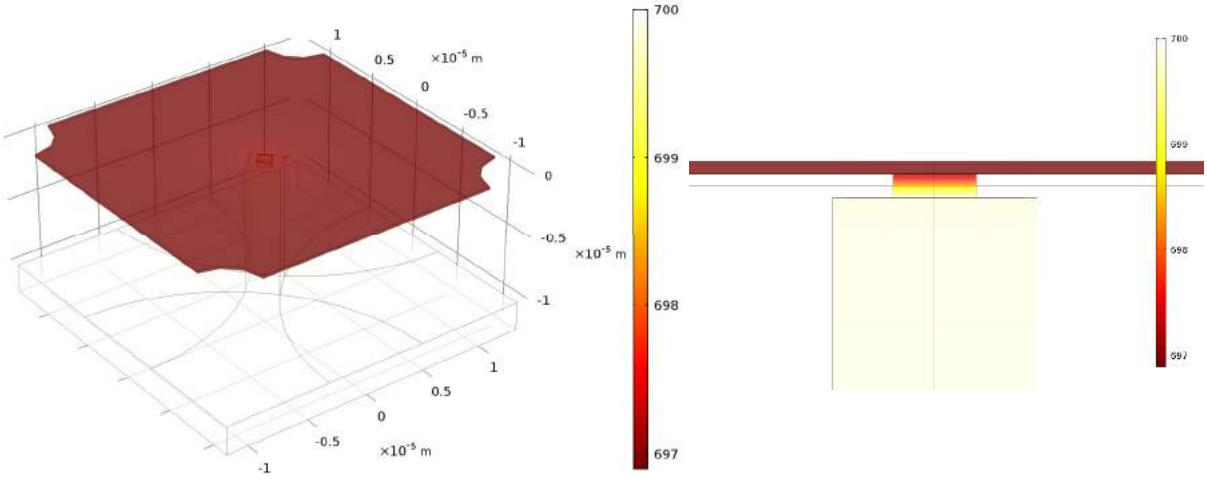

Figure 3.30: (a) Temperature distribution of MTC cell with $1\mu m^2$ *silica pillar surface. (b) Temperature distribution at z direction.*

The next model is for the corner and border of MTC. Same as previous model mesh, the critical position is a much higher mesh density for a more reliable result as presented in Figure *3.31* (a). At the corner MTC has an even less temperature difference at border contact situation. Because the cell has a centrosymmetric property, the following model for center cell will have one quarter of the first cell model, similar to the corner MTC model in Figure *3.31*(b). Due to a larger contacting area and the fact that membrane can hardly diffuse heat to external, the result is 0.04K temperature difference. Both 3K and 0.04K temperature difference are far away from what we expected for MTC devices. Therefore, a method of heat dissipation for SOI and a better layout to control the SOI input thermal conduction from pillars are necessary.

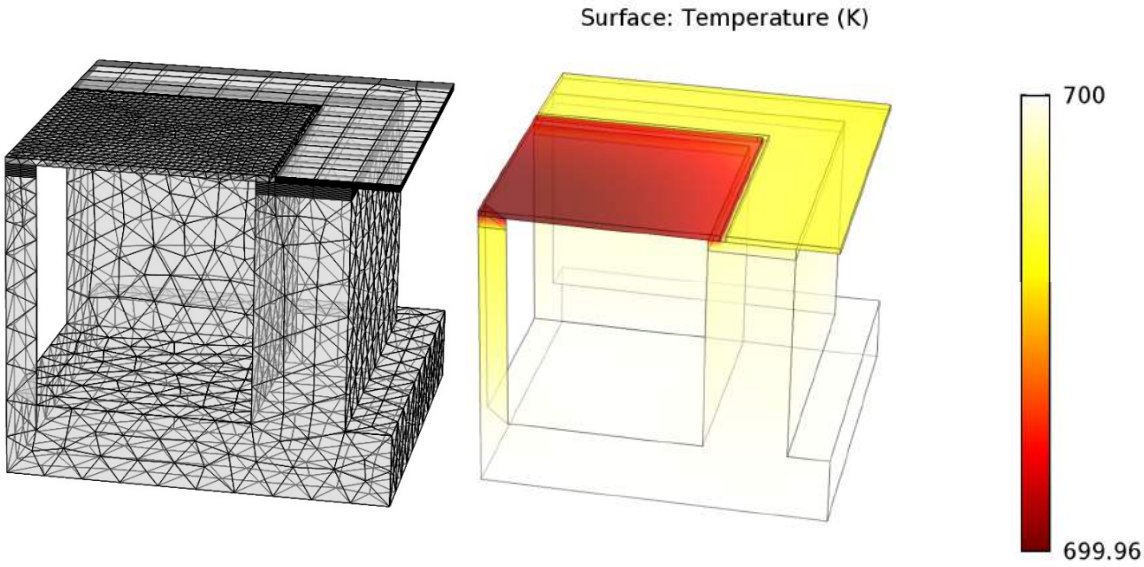

Figure 3.31 (a) Defined mesh layer number for critical position (b) Temperature distribution at the boarder of the MTC membrane.

Both of these two previous result is not satisfying, the pillar and border contacts have great impact to the thermal isolation, which lead to less temperature gradient than necessary. These two structures represent two different ways to support the collector electrode. The first method is to support the membrane in between openings under the membrane, which is like columns in buildings. While the second method is to hold the membrane at the edge position like drum and drum surface. More modeling was made in order to explore a better method to isolate heat and increase the temperature difference.

The third simulation operates in different given temperature with different pillar heights based on the first model. Due to the fact that silicon dioxide is one of the best thermal isolators, the length of silicon dioxide limits the thermal flux greatly. Despite the wafer we have has maximum box layer about 200nm thickness, a simulation with larger thickness range is meaningful. It is because the prototype is aimed to have a design that capable of commercialization. Technically speaking, to fabricate a SOI wafer with 10μm box layer is feasible. One other conclusion is that the symmetry of a single cell of the first model means that the later model can be a fourth or one eighth of the previous surface.

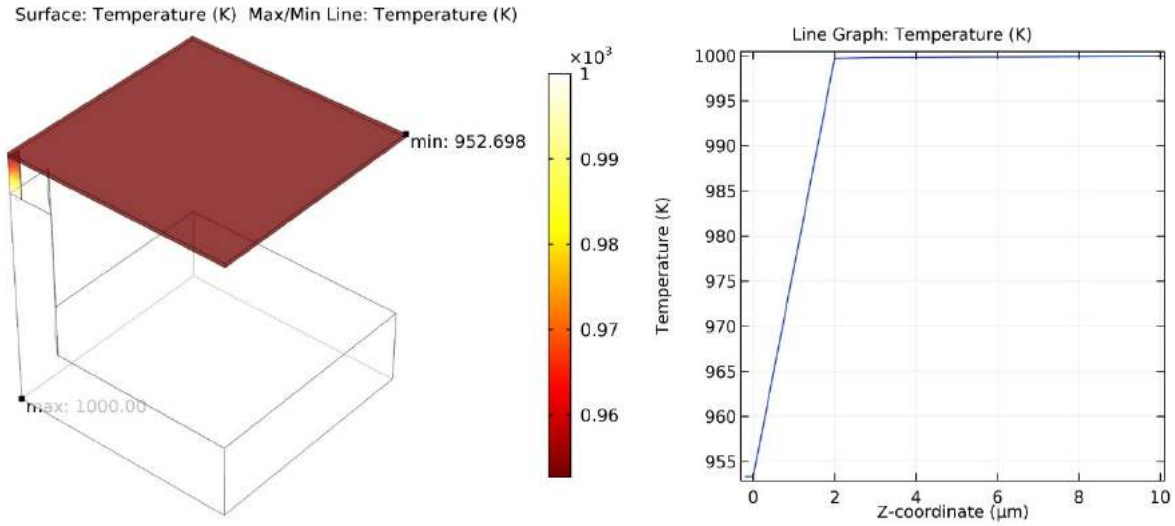

Figure 3.32 (a) Temperature distribution on MTC with 2μm SiO_2 pillar. (b) Temperature curve on Z direction at center of the pillar.

A series of different given emitter temperatures from 700K to 1000K and with different silicon dioxide heights from 400nm to 8μm in same gap distance were simulated. Due to the objective of analyzing the impact of thermal conduction with different SiO_2 thickness, in this simulation, silicon membrane thermal conductivity was set same as bulk silicon. According to the thermal emission experimental experience, the pressure is set to $10E^{-8}\ atm$. Results is presented in

Ambient parameters	*Dimension of SiO2 layer*	*T HOT:*	*700K*	*800K*	*900K*	*1000K*
Pressure: $\rho_{amb} = 10E^{-8}\ atm$	*400nm*	***T COOL:***	*697.1K*	*795.1K*	*892.1K*	*988.1K*
	1μm		*693.3K*	*788.7K*	*882.2K*	*973.6K*
Irradiance: $I_{sn,amb} = 1000[W/m^2]$	*2μm*		*687.3K*	*778.9K*	*867.4K*	*952.7K*
	4μm		*676.4K*	*761.8K*	*842.8K*	*919.4K*
	8μm		*657.9K*	*734.4K*	*805.5K*	*871.7K*

Table 3.2.

Ambient parameters	*Dimension of SiO2 layer*	*T HOT:*	*700K*	*800K*	*900K*	*1000K*

Pressure: $\rho_{amb} = 10E^{-8}\ atm$ Irradiance: $I_{sn,amb} = 1000[W/m^2]$	*400nm*	*T COOL:*	*697.1K*	*795.1K*	*892.1K*	*988.1K*
	1μm		*693.3K*	*788.7K*	*882.2K*	*973.6K*
	2μm		*687.3K*	*778.9K*	*867.4K*	*952.7K*
	4μm		*676.4K*	*761.8K*	*842.8K*	*919.4K*
	8μm		*657.9K*	*734.4K*	*805.5K*	*871.7K*

Table 3.2 Simulation results at different SiO2 thickness at different emitter temperature

This simulation was based on that all other environmental parameters remain unchanged and the pillar section unmodified. Only the height of different material changes with the total pillar height at 10μm. The T COOL presented in

Ambient parameters	*Dimension of SiO2 layer*	*T HOT:*	*700K*	*800K*	*900K*	*1000K*
Pressure: $\rho_{amb} = 10E^{-8}\ atm$ Irradiance: $I_{sn,amb} = 1000[W/m^2]$	*400nm*	*T COOL:*	*697.1K*	*795.1K*	*892.1K*	*988.1K*
	1μm		*693.3K*	*788.7K*	*882.2K*	*973.6K*
	2μm		*687.3K*	*778.9K*	*867.4K*	*952.7K*
	4μm		*676.4K*	*761.8K*	*842.8K*	*919.4K*
	8μm		*657.9K*	*734.4K*	*805.5K*	*871.7K*

Table 3.2 is found at the lowest position on the farthest corner of the membrane on the simulated model same as showed in Figure *3.32*. With the maximum temperature difference on the membrane less than 0.2 degree the chosen axis direction data will present the temperature gradient in between the emitter and collector.

With the gap fixed at 10μm, the SiO_2 pillar at larger height cannot approximate as same section shape at different height, so the calculated cool temperature may be lower than the real scenario with current SiO_2 layer model ($d > 2\mu m$). This is due to isotropic of two-step gas etching beginning from XeF_2 vapor etching then HF vapor etching. After two-step vapor etching process, the large thickness SiO_2 lay turns into a pillar with small bottom section surface and large upper surface. The smallest pillar surface at the bottom is around $1\mu m^2$, which is same as the section surface in model, while the largest surface will lead to a higher collector temperature. From Table 3.2, the biggest temperature difference is about 130 degree, which seems to be as good as we expected. However the results with 400nm SiO_2 layer have a gradient of only about 3 to 12 degree, which is far from satisfying. All the result above proves that the SiO_2 thickness is a key parameter. In our case the thick SiO_2 was not readily available. We will now explore other leverages to increase temperature gradient.

3.3.4 Modeling for capacity of diffuse heat by membrane

Intuitively the alternative solution is improve the capacity of diffusing heat for Silicon membrane. However in vacuum environment, if the membrane can diffuse heat through radiation and overcome the thermal conduction through the pillar? Due to the small membrane surface in last simulation, the 0.2 degree maximum temperature different on previous simulation is not illustrative. To explore this, the next model with a big membrane surface and same SOI parameter 200nm/400nm was designed. The focus of simulation in this section is based on thermal conductivity on silicon membrane with lower thermal conductivity value compared to bulk silicon [Ma 14]. For membrane thickness about 200nm the parameter of thermal conductivity we set was 70W/mK.

Simplifier from the second model, in this simulation, the membrane has a big surface in round shape with border contact of $10\mu m$. Based on 2D axisymmetric module, calculation time can be greatly saved. This model is also capable to analyze the impact of border contact to the membrane temperature at far away position. This help to give a visual image of the heat diffusion capacity for the membrane in

vacuum. With 200nm sickness SOI and 400nm sickness SiO_2, the temperature distribution is presented in Figure *3.33*(a).

Since thermal isolation is a difficult engineering problem for micro-gap thermionic convertor, the target temperature difference is set to 100 degree. From Figure *3.33*(b), the temperature distance plot present the collector surface temperature drops as it is at a farther position. To build up a gradient of 100 degree, in border fully contact situation, the effective membrane should be located at 1.4mm away from its border. The dimension of 1.4mm for a membrane is too large to be efficiently and reliably fabricated. The fully contacted border is not a good design even through the contact dimension diminuend from 10µm to 1µm. At 1µm border contact model, the results barely changes about tens of micrometers at 100 degree temperature difference position.

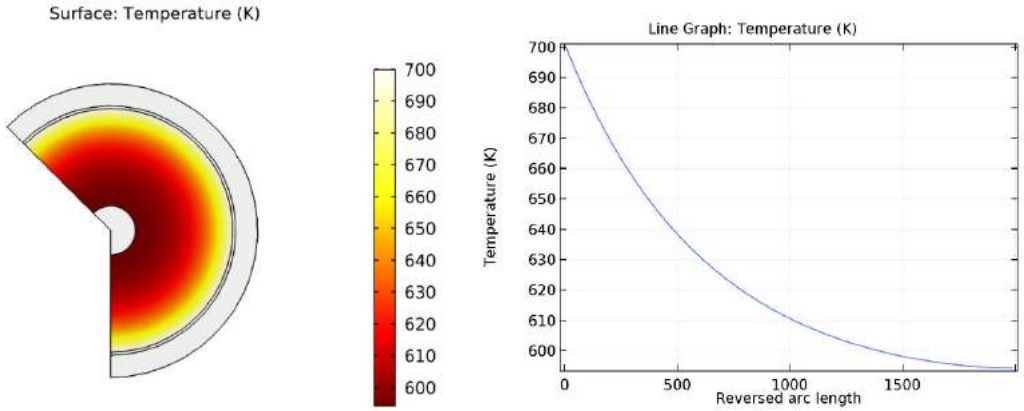

Figure 3.33 (a) Temperature distribution at the membrane surface with emitter temperature at 700K. Calculate range from 700K to below 600K. Membrane only contact the substrate at 700K at the center circle position. (b) The relationship between temperature and position to border distance in micrometer.

Still, these results provide a good result for investigating the diffusive capability of silicon surface in vacuum. Results tell that, at contact position the heat flux is saturated, and the heat transfer is limited by thin film membrane structure. So, one more method to create a larger temperature gradient is to limit the heat flux at close to pillar position. For example, at pillar support model, the upper titanium electrodes should be laid faraway from pillar structure to avoid increasing thermal conductivity on membrane. What's more, at around pillar structure, Phononic pattern of hundred nanometer dimension holes should be distributed to eliminate heat flux through membrane [Haras 16]. Similarly for drum structure and border contact model, these Phononic patterns of nanoscale holes can be distributed at near border position where the thermal flux needs to minimize. In this way, thermal flux from contact position can be limited. [Yu 10]

The previous simulation results tell that with a large enough surface, the collector temperature may be low enough fitting our design. So, the initial design presented Figure *3.28* is modified. By controlling the opening size only, the pillar can be fully etched in some cells and have repetitive etching results by every three cells in both X and Y direction. The modified layout has larger cells separated by doted lines. All the opening holes has slightly larger dimension than those close to pillar position. Changing the distribution of smaller openings can lead to different pillar pattern. So, in the simulation model is larger while the silicon and silicon dioxide pillar remain same. In other words, the ratio of active membrane surface/pillars section surface is magnified.

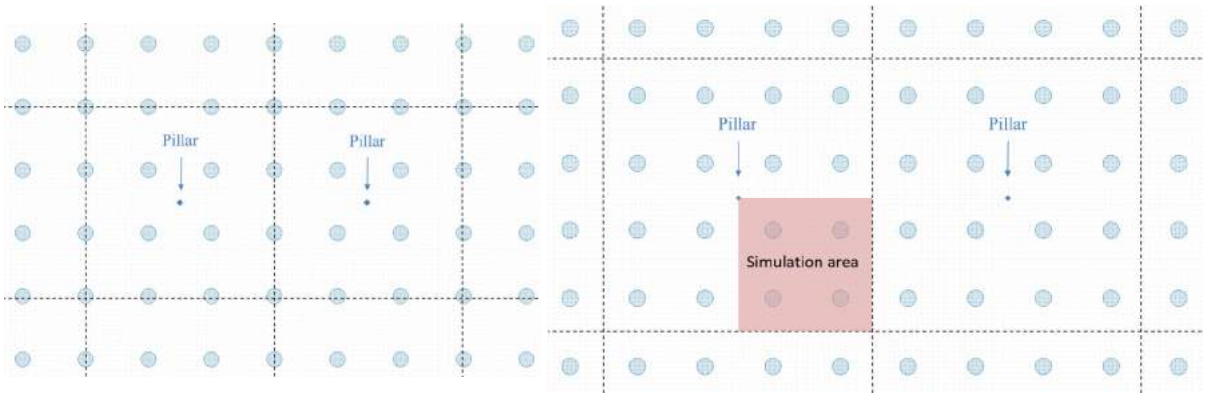

Figure 3.34 Patterns of SOI opening, pillar under SOI lay will not be present in each cell as compared to Figure 3.28. The cell/pillar interval value can range from three to larger number. The left layout has an interval value of 3, the right has an interval value of 4.

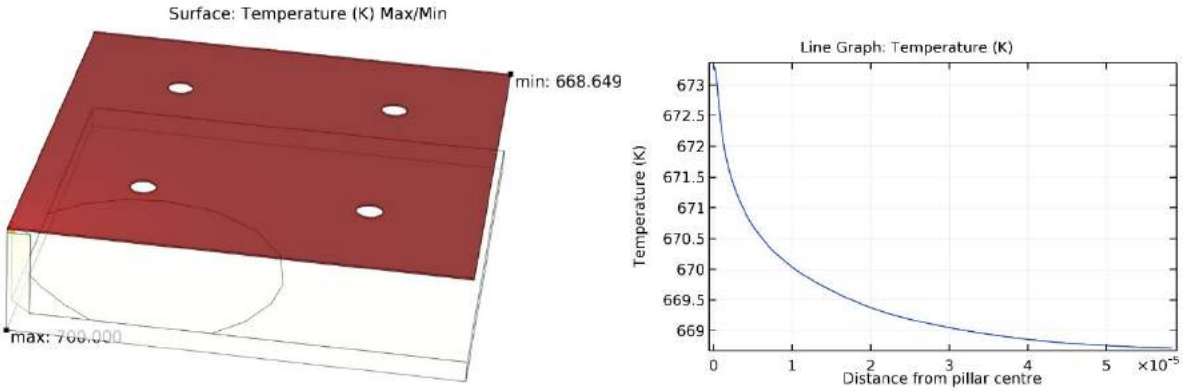

Figure 3.35 (a) Model after modification with interval value 4 with $50\mu m \times 50\mu m$ membrane. (b) Temperature distribution from the pillar center to further position on the top membrane surface. Opening holes position was avoid when printing temperature-radius line graph.

Figure *3.35* (a) presents more than 10 times larger temperature difference than the first model. With a pillar height of 400nm the minimum temperature reaches 668.7K and at 10µm away region greater than 30 degree temperature difference was established. With silicon membrane thermal conductivity corrected from bulk value to the value corresponded to 200nm thickness 2D structure [Marconnet 13][Ma 14], the temperature gradient on the membrane plane was also analyzed. Curve in Figure 3.35(b) presents a significant temperature drop in close to pillar position which means the collectors' temperature is also limited by thin film thermal conductivity. In other words, by limiting thermal conductivity of membrane near pillar position, further temperature drop can be expected. By compared to the curve in Figure *3.33*(b), the temperature reduces is more significantly in this model. This means to limit thermal flux through pillar will lead to further temperature drop on the membrane position far from pillar. A similar calculation of different SiO_2 thickness as presented in

Ambient parameters	*Dimension of SiO2 layer*	*T HOT:*	*700K*	*800K*	*900K*	*1000K*
Pressure: $\rho_{amb} = 10E^{-8}\ atm$	*400nm*	*T COOL:*	*697.1K*	*795.1K*	*892.1K*	*988.1K*
	1µm		*693.3K*	*788.7K*	*882.2K*	*973.6K*
Irradiance: $I_{sn,amb} = 1000[W/m^2]$	*2µm*		*687.3K*	*778.9K*	*867.4K*	*952.7K*
	4µm		*676.4K*	*761.8K*	*842.8K*	*919.4K*
	8µm		*657.9K*	*734.4K*	*805.5K*	*871.7K*

Table 3.2 was applied and result listed in table 3.3.

Ambient parameters	**Dimension of SiO2 layer**	**T HOT:**	700K	800K	900K	1000K
Pressure:$\rho_{amb} = 10E^{-8}\ atm$	400nm	**T COOL:**	668.6K	750.9K	828.9K	903.2K
	1μm		644.5K	717.9K	787.4K	854.1K
Irradiance: $I_{sn,amb} = 1000[W/m^2]$	2μm		618.9K	685.9K	750.3K	813.1K
	4μm		589.9K	652.5K	714.3K	776.0K

Table 3.3 Simulation results at different SiO2 thickness at different emitter temperature

The simulation results are much satisfying compared to results presented in

Ambient parameters	*Dimension of SiO2 layer*	*T HOT:*	*700K*	*800K*	*900K*	*1000K*
Pressure*:* $\rho_{amb} = 10E^{-8}\ atm$	*400nm*	***T COOL:***	*697.1K*	*795.1K*	*892.1K*	*988.1K*
	1μm		*693.3K*	*788.7K*	*882.2K*	*973.6K*
Irradiance*:* $I_{sn,amb} = 1000[W/m^2]$	*2μm*		*687.3K*	*778.9K*	*867.4K*	*952.7K*
	4μm		*676.4K*	*761.8K*	*842.8K*	*919.4K*
	8μm		*657.9K*	*734.4K*	*805.5K*	*871.7K*

Table 3.2. From the table above, we find that models at lower T_{hot} with thicker SiO_2 layer and models with higher T_{hot} have over 100K temperature difference. These temperature differences are what we expect. In addition, we found that with larger SiO_2 pillar height the temperature decrease rate along the membrane is smaller than lower SiO_2 height. For example, at $T_{hot} = 700\text{K}$ the 400nm model has 5K maximum temperature difference on membrane while at 4μm model the difference is only 2K. Similar comparison illustrate that all methods focus on membrane is effective only when it has a higher temperature. So, the effective control of thermal flux through pillar is the most efficient method to drop the membrane temperature, while the limit of the membrane thermal conductivity is only a backup solution for small height SiO_2 pillar model.

As discussed previously, Phononic patterns can be useful in limiting thermal conductivity. Corresponded simulation can be carried out by limiting the thermal conductivity locally near pillar. This simulation is tested on 400nm and 1μm thick SiO_2 MTCs. Assuming with the patterns, a reducing factor of 0.6 is applied on membrane thermal conductivity. The patterned distribution area is $5\mu\text{m} \times 5\mu\text{m}$ square shape located around pillar center in the model.

Dimension of SiO2 layer	***T HOT:***		*700K*	*800K*	*900K*	*1000K*
400nm	*No phononic pattern*	***T COOL:***	*668.6K*	*750.9k*	*828.9K*	*903.2K*
	With phononic pattern		*667.2K*	*748.7K*	*826.11*	*899.8K*
1μm	*No phononic pattern*		*644.5K*	*717.9K*	*787.4K*	*854.1K*
	With phononic pattern		*643.5K*	*716.6K*	*785.9K*	*852.4K*

Table 3.4 Simulation results comparing the effectiveness of phononic pattern on membranes at different SiO2 thickness at different emitter temperature

Dimension of SiO2 layer	***T HOT:***	*700K*	*800K*	*900K*	*1000K*

400nm	*No phononic pattern*	***T COOL:***	*668.6K*	*750.9k*	*828.9K*	*903.2K*
	With phononic pattern		*667.2K*	*748.7K*	*826.11*	*899.8K*
1µm	*No phononic pattern*		*644.5K*	*717.9K*	*787.4K*	*854.1K*
	With phononic pattern		*643.5K*	*716.6K*	*785.9K*	*852.4K*

Table 3.4 presents the contribution for building a temperature gap is not significant. The largest difference appears at 400nm 1000K circumstance with a further temperature drop of 3.4K. After comparison, we found that this method of thermal isolation is relatively effective in small SiO_2 pillar structure and at higher temperature. It is easy to predict that with larger phononic pattern covered area will result in a better temperature gap. However, it will also decrease the effective collector surface, which may not be worthwhile.

The Phononic patterns added on the silicon membrane will significantly increase the difficulty of lithography and overall fabrication difficulty. The patterns will increase the fragility of the membrane, which function as the collector. Although the gain of temperature drop is observed from simulation results, the benefit is minor and leads to a higher risk. It is not an acceptable method with current fabrication techniques in the frame of this work.

3.4 Conclusion

This chapter has discussed the efficiency of MTC. To design an efficient MTC, not only a low work function coating material is needed. A suitable gap dimension and a dedicated thermal isolation structure are necessary. This chapter focuses on the MTC structure and related parameters. In the first part, a conception of open loop voltage is discussed in detail with theoretical analyses. The open loop voltage is the most accessible value during characterization. A derivation of equation of open loop voltage is presented according MTC working principle and final equilibrium state. The results of two sets of values from different route turns agree at the end. The conclusion is a slightly higher work function of collector can be beneficial to rise the open loop voltage. At the same time, it verifies that the FEM model is correctly established. Then as an initial step toward a good MTC layout, in chapter 3.2, the theoretical discussion about all influential factors concludes that at a gap dimension ranging from 200nm to about 10µm will lead to the best efficiency.

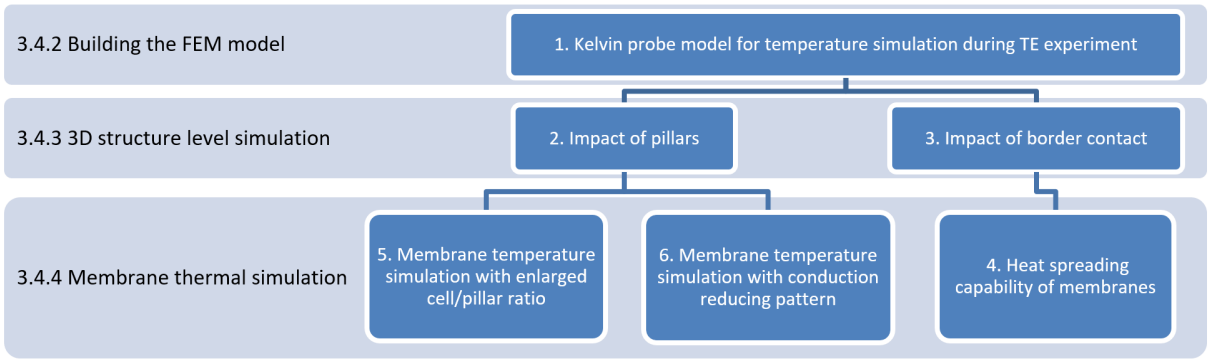

Figure 3.36 Simulation and study route of chapter 3.4

Then at the next section, two state-of-arts models about MTC are presented, which are two most inspiring model leading to our design. From these two recent feasible models, general ideas of how to concept our MTC structure with available equipment and techniques are established. The following

steps remain to be parameters choice and structure detail design. Other than work function and gap distance, among all factors, the most important is to have a large temperature difference between emitter and collector. Based on the goal of high temperature difference, the design is initiated with a numerical simulation. General study route is presented in Figure *3.36*. We start from confirming the simulation result by fitting it into the theory and the experimental results. Section 3.4.1 shows that the simulation results and theory calculation outcome agree with experimental results, which indicate that both the theory and simulation results are consistent. With a first structure, a thermal simulation is also applied based on the real MTC structure with same dimension. Based on the temperature difference results, we found that combining the pillar structure with membrane suspension, a large MTC surface with high effective ratio can be fabricated with existing equipment. A large membrane surface and pillar section surface ratio ($S_{membrane}/S_{pillar}$) will create a good temperature gap. With SOI-200-400nm wafer, a 50-degree temperature difference can be established and the design is compatible with other thicker box layer SOI wafers, which may easily increase the temperature difference to above 100 degree at 800K hot emitter and 2µm box layer. Furthermore, the strategy of apply a conduction reducing pattern on the membrane is discussed. However, it seems to be effective for high temperature anode, which is considered only as a backup plan.

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Chapter 4 Fabrication of micrometer-gap parallel electrodes

This chapter presents engineering and technological aspects of this work including design and fabrication of the prototype. As a prototype, the design need to be harmless, cheap, industrially compatible and reliable based on existing nano/micro-fabrication processes and technology. One of the best solutions is fabricate upon the silicon on insulator (SOI) wafer with Silicon (Si) layer on top and thicker box (silicon dioxide) layer in middle.

After fabricating the electrodes with gaps, we integrate it to our characterization platform before low work function film deposition on electrode surface in-between the vacuum gap. Then, the MTC was ready to be tested. The prototype MTC proves that thermo-convertors based on thermo-emission effect are one environmentally friendly, cheap and industrially compatible generator with much higher potential than other energy harvest devices.

4.1 Introduction

After FEM simulation presented in last chapter, evaluation of thermal isolation for MTCs with different design was made. A pillar/cell ratio over four presented in Figure *3.34* can create difference temperature gap according to simulation at ideal circumstances. Benefit from good thermal resistivity property of silicon dioxide and the reduced thermal conductivity on silicon membrane the target temperature can be create in vacuum condition. Thus, fabricate a MTC device with enough thermal gap in micronized distance vacuum gap is proved feasible (simulated in chapter 3.3).

It was already described that in modern digital industry SOI technology is largely used during fabrication. Multiple advantage of devices fabrication based on SOI technology makes it one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic device, as “extending Moore’s Law”. In our case, using SOI wafer and microelectronic fabrication process means that the prototype has a higher potential to be further modified to fit the commercial needs. In the design of MTC devices, the thin top layer of SOI wafer will be cold electrode that is cathode. The isotropic etching process with the etching cavities interval will control the gap between top SOI layer and silicon substrate. This distance represent the vacuum gap dimension, which is the crucial part of the whole project. Thanks to the reference of membrane fabrication process of integrated micrometer platform for thermoelectric measurements [Haras 14] and multiple processes experiences from our group, the designed fabrication process is successfully carried out. And details will be illustrated later in this chapter.

This chapter describes the technological input of this project. The practical part includes the design, fabrication, integration and characterization of a Micro-gap Thermionic energy Converter. The platform used in low work function coating and characterization are also able to perform measurement of I-V characteristics for MTC devices in vacuum environment. The potential of the MTC device is revealed at the end of this chapter with precise characterization techniques and with dedicated analysis.

4.2 Designing the device

4.2.1 Layout

The first conception of an MTC with Microelectronics manufacturing processes is based on Silicon On Insulator wafers (SOI). Based on the structure needs of MTC and compatibility to chemical vapor deposition process for alkali metal oxide, the device needs a vacuum gap with accessibility from outside. As presented in 3.3.1.1, the structure based on SOI wafer has a membrane structure with matrix apertures. This aperture patterns allow the two steps isotropic etching during structure fabrication and film deposition. The top SOI layer is highly doped into N-type silicon. Titanium metal electrode on to of SOI will further increase the conductivity of the SOI layer. Figure *4.1* is the section view of the device, which will give a general idea of the targeted structure.

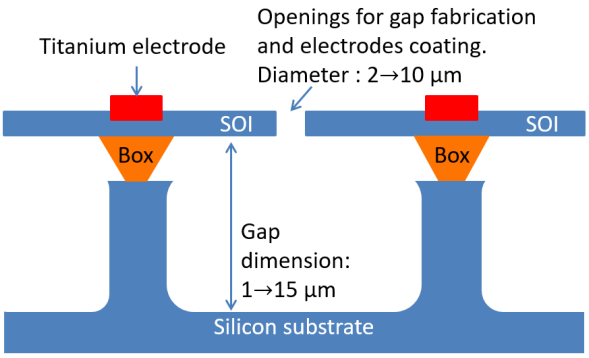


Figure 4.1 Schematic diagram of sectional view of MTC fabricated by SOI wafer.

In the first sample, the layout is designed for exploring the fabrication techniques and searching for best parameters for MTC devices. Targeting to create a vacuum gap at about 10µm size by vapor etching, which is an isotropic etching process. The depth of the gap and the membrane suspension was realized in the same step. So different distance between etching holes and different diameter were tested in the first sample. The sample layout presented in Figure *4.2* is one of the eight samples on the first wafer with etching holes distance of 30µm. Other etching holes distance from 15µm, 20µm to 25µm were also fabricated on the same wafer.

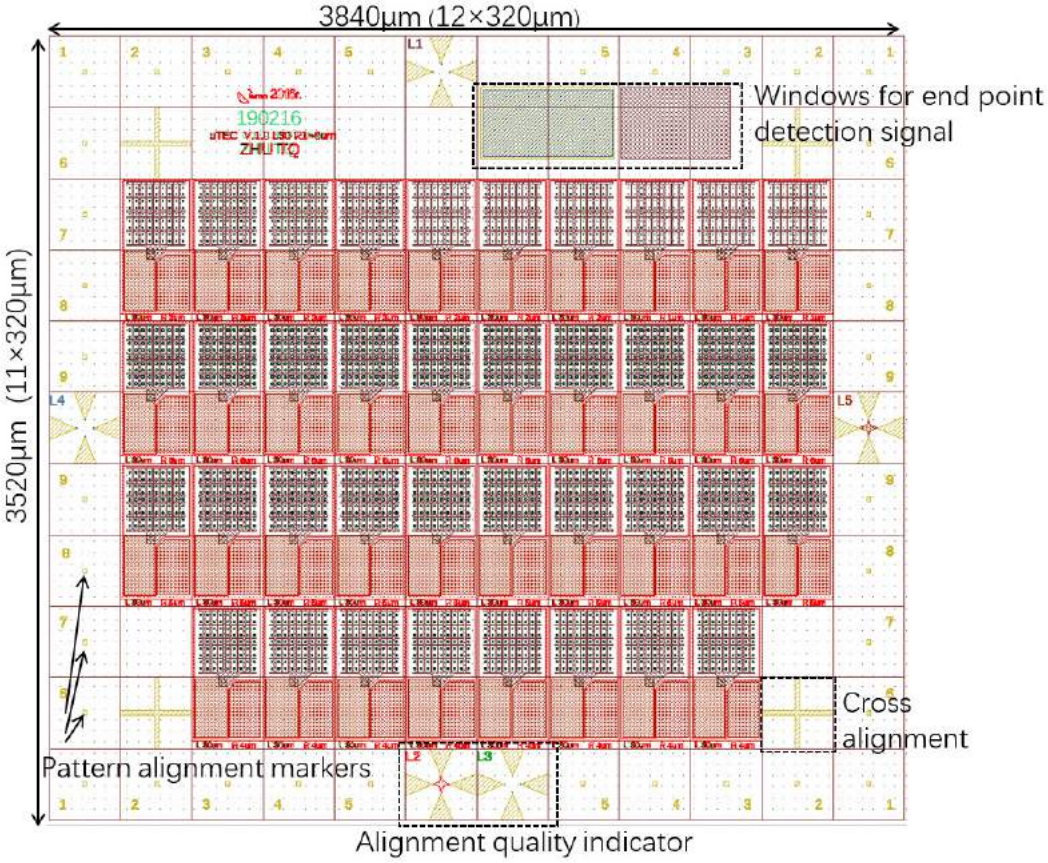


Figure 4.2 shows the top view of the fabricated cell that contains 38 devices. On this sample the distance between open holes are set to 30µm and radius of holes varies from 1µm to 6µm.

The external cell dimensions are 3520µm×3840µm. Because the maximum writing area for e-beam lithography without moving the stage is limited, the cell external dimensions was composed from the finite number of 320µm×320µm or 500µm×500µm squares. Within this range, when doing e-beam

lithography, the machine can execute all the pattern writing process without displacing the wafer stage, which is important to maintain the highest precision. Figure *4.2* is the global view of one whole sample including all the details like optical alignment markers, e-beam lithography alignment markers, windows for endpoint detection signals or the design and layout information. The alignment markers are small squares of 20µm×20µm size and can be identified by e-beam lithography system.

The windows for endpoint detection signal are essential for Reactive Ion Etching (RIE), which helps to control the depth of etching. With laser spot on the window for end point detection, the capture sensor will receive the reflection and measure the intensity of the signal. The intensity of the signal will present like a sinusoidal signal as a function of time and thus, depth of etching. The cycle and amplitude of the signal will tell on which layer the plasma is etching.

One thing need to be aware is that even through all the MTC samples in this report was using e-beam technology to write the pattern, the photolithography can be an alternative method to fabricate the sample. Due to the controlled minimum size of patterns, photolithography can easily replace e-beam lithography during massive fabrication.

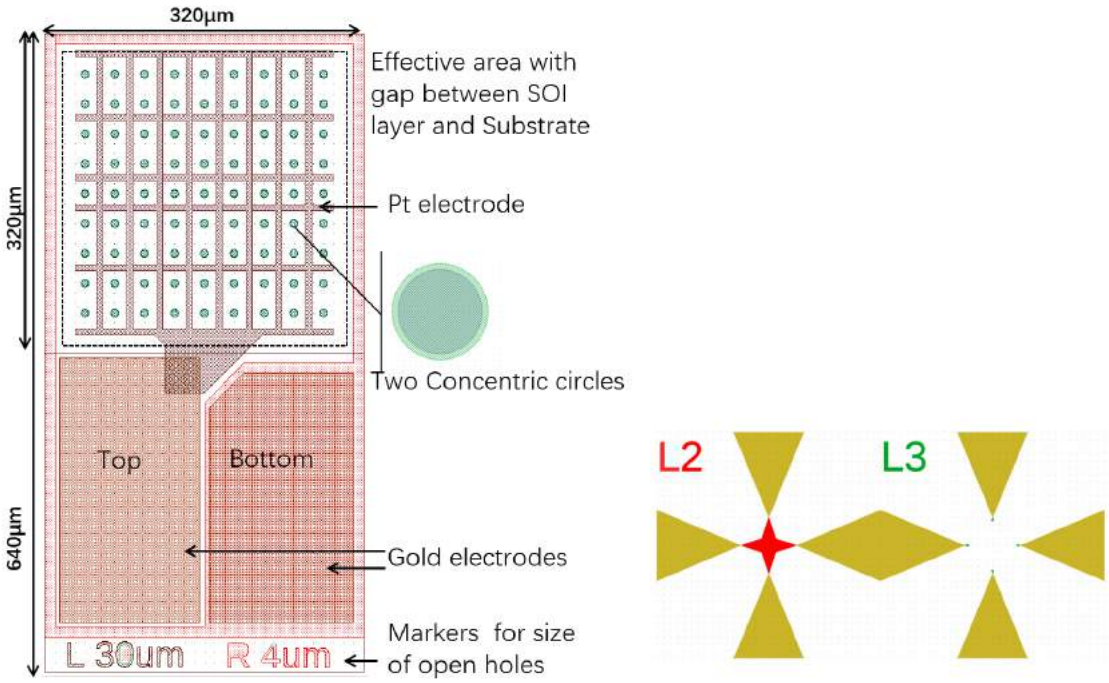


Figure 4.3(a) Single device in the size of two basic fields. (b) Alignment indicators to confirm the alignment quality after develop process.

Figure *4.3*(a) represent one single device that takes two basic cell space on the wafer. The upper cell part is the etching holes and Pt electrode that connected to the collector membrane. The bottom cell is two large electrode pads. The left is collector and the right is etched in to SOI substrate that is connected to emitter. To distinguish the design during SEM or optical microscope, each device was labeled with dimension parameters. More information can be found on the top left corner of each sample. The dotted box is where the membrane will be. And the two concentric circles are critical patterns for membrane suspension process, where the outside circles are etched to substrate, while the inner circles are for opening protection and window for XeF2 etching. All process details will be described in nest section.

To ensure that the relative position between layers corresponds to the design the lithography machine detects the markers and based on their real positions the e-beam exposure is performed. Figure *4.3*(b)

shows two alignment indicators. By comparing the inner parts and outside parts, which are on different layers and realized by different exposures, we can observe the quality of alignment. When the alignment is not precise, the small internal parts will not pointed to the triangles. In this situation, the spin-coating and exposing step should be repeated. The right alignment indicators has much small inner parts, this can help acceleration of e-beam writing process with small current. The alignment accuracy of the lithography equipment is 30nm, however this misalignment value can be further reduced by using four pattern alignment markers per sample, which are shown in Figure *4.2*.

Figure *4.4* illustrates the arrangement of different samples on the 3 inches SOI wafer. Four different designs with eight repetitions each were positioned with a 10mm spacing in x and y direction. As presented each sample design consists of patterns with 5 or 6 different interval between holes. A total of 1216 devices with small effective surface were fabricated in one time. All through on the same sample only several devices will have membrane structure with pillars connecting emitter and collector, enough devices are available for process test and parameter exploration.

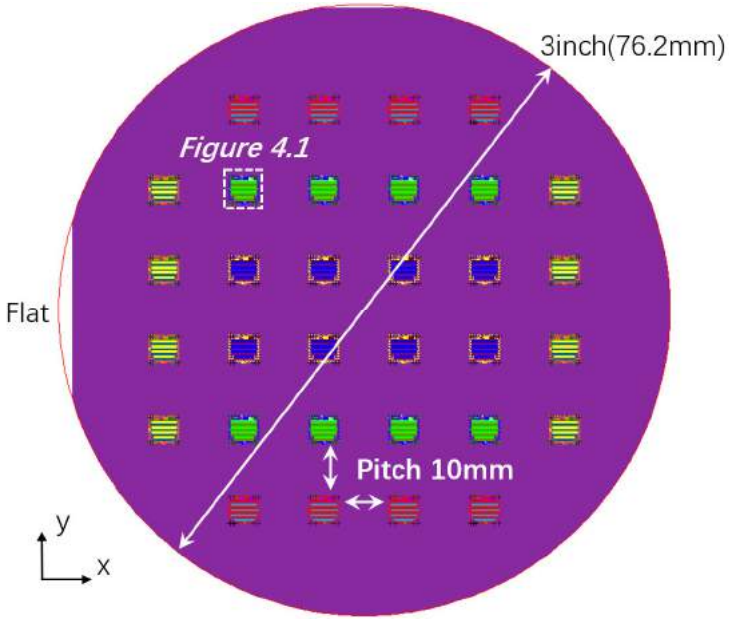


Figure 4.4 Top-down view on the 3 inches SOI wafer with the cell arrangement and spacing.

The spacing between the cells is set to 10mm to facilitate the cleaving of the full wafer into separate samples. Diamond saw or laser cutting will operate this process. This distance is sufficiently for this separating process and further manipulation. Consider the increasing size of MTC surface, less samples may be fabricated on one single wafer to facilitate the integration to the characterization platform.

Color	Etching hole distance	Radius of etching holes
Red	15µm	R 1µm to R 5µm
Green	20µm	R 1µm to R 5µm
Blue	25µm	R 1µm to R 5µm
Yellow	30µm	R 1µm to R 6µm

Table 4.1 Sample layout on the 3 inches SOI wafer.

Color	Etching hole distance	Radius of etching holes

Red	15µm	R 1µm to R 5µm
Green	20µm	R 1µm to R 5µm
Blue	25µm	R 1µm to R 5µm
Yellow	30µm	R 1µm to R 6µm

Table 4.1 presents detailed information about interval distance between two nearby etching holes. On different samples, the radius of etching holes are different, verging from 1µm to 6µm depending on the etching holes' pitch.

4.2.2 Improvements and later version

The tested sample profile takes the size of 18 cells by 18 cells, in which the cell size is 320µm×320µm same as previous samples. The only MTC device takes most space of the sample surface. Thus the total effective area take 16 cells by 15 cells, which without diminishing the etching holes, the total surface is 24.576mm2. Other patterns like alignment markers and electrode pads are positioned at the border and alignment markers were moved away from membrane border. All patterns and characters with sharp corners were changed into smooth rounded shape to avoid concentration of mechanical stress and cracks at sharp edges. The circle shape etching holes in this version has changed to square shape with rounded corner, because the square shape etching cavities will decrease the final pillar section surface.

Figure *4.5* shows the MTC device in detail. The patterns in yellow are alignment markers. Green represents concentric etching cavities shapes. The blue area is covered with Titanium, which pass from the membrane to right gold pad in red color. It is also position under the left gold pad, which function as an adhesion layer between silicon and gold. The pink square is for opening the cavity that will also isolate the SOI layer from the membrane to ensure the electrical isolation. In this graph, in order to present different materials and due to the limitation of resolution, several layers over lapped on each other are not presented in detail.

The bottom right part of Figure *4.5* shows that in different positions the etching cavity has different dimension. The squares aperture above the black doted line have a side length of 6µm while the aperture below has 5µm. This differentiation makes the pillar between emitter (substrate) and collector (SOI layer) formed in expected position, which will minimize the energy lost by thermal conductivity.

Color	Layer number	Description	Step number	Processing technology	Related materials
Yellow	16	Alignment markers	2	RIE	Entire SOI
Green	3	Etching cavities	2	RIE	
Brown	4	Cavities etching cavities	6	RIE	Protection SiO2
Blue	5, 7	Titanium metallization	4 5	Evaporation Fast annealing	Titanium
Red	1	Gold metallization	5	Evaporation	Gold
Pink	6	Membrane and SOI layer isolation	2	RIE	Entire SOI

Table 4.2 links the pattern color with the technological process attributed to the given layer. The reactive ion etching (RIE) and evaporation are two only process that need to be processing on the corresponded layer. However, many more process is contains in the full fabrication like Low Pressure

Chemical Vapor Deposition (LPCVD), annealing and so on. Details about all technological steps will be presented in next section.

Color	Layer number	Description	Step number	Processing technology	Related materials
Yellow	16	Alignment markers	2	RIE	Entire SOI
Green	3	Etching cavities	2	RIE	
Brown	4	Cavities etching cavities	6	RIE	Protection SiO_2
Blue	5, 7	Titanium metallization	4 5	Evaporation Fast annealing	Titanium
Red	1	Gold metallization	5	Evaporation	Gold
Pink	6	Membrane and SOI layer isolation	2	RIE	Entire SOI

Table 4.2 Layer color and Layer number in layout editor. Corresponded process information with related materials.

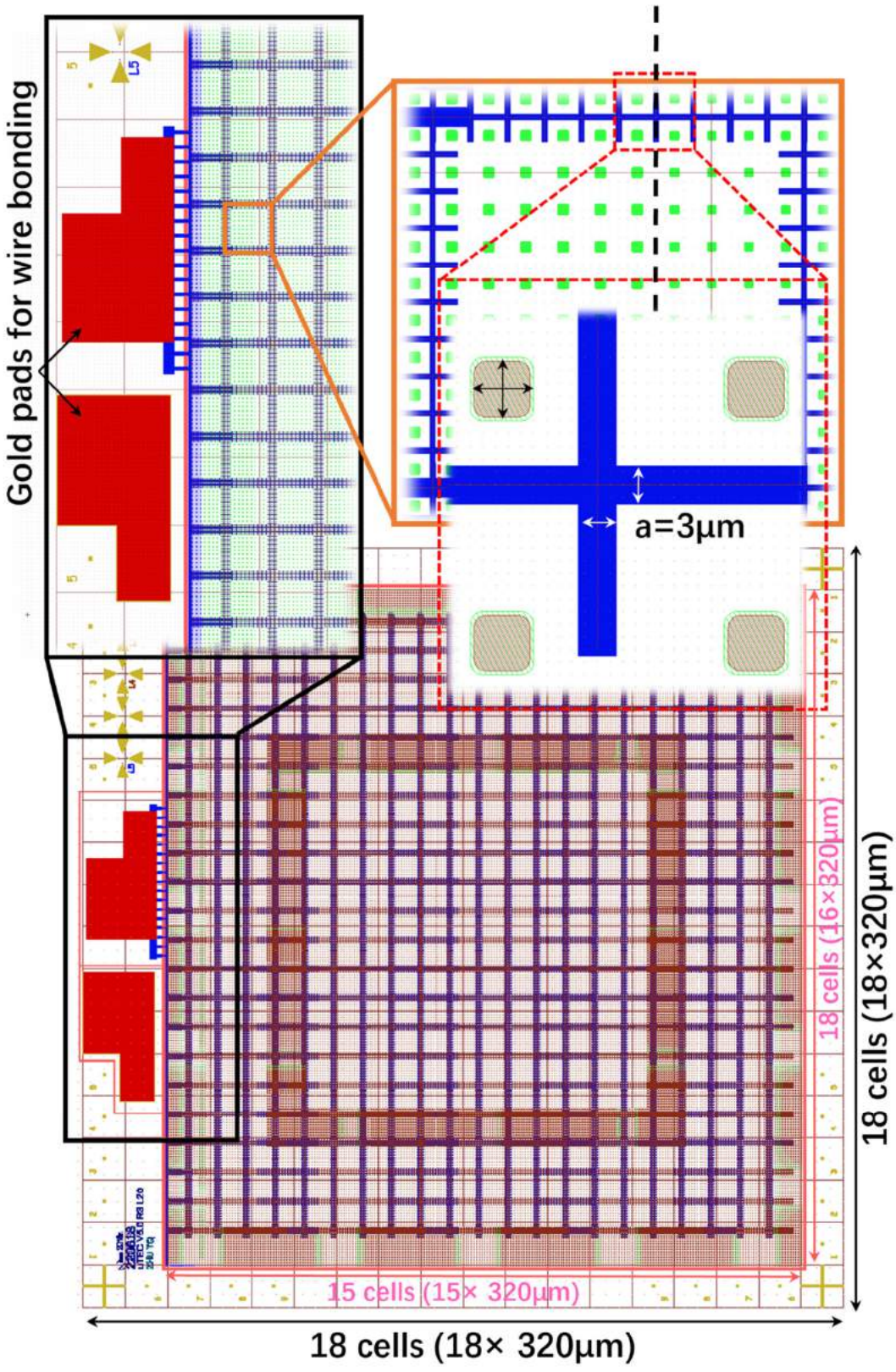


Figure 4.5 One single MTC device with a large membrane surface.

According to

Color	Layer number	Description	Step number	Processing technology	Related materials
Yellow	16	Alignment markers	2	RIE	Entire SOI
Green	3	Etching cavities	2	RIE	
Brown	4	Cavities etching cavities	6	RIE	Protection SiO2
Blue	5, 7	Titanium metallization	4 5	Evaporation Fast annealing	Titanium
Red	1	Gold metallization	5	Evaporation	Gold
Pink	6	Membrane and SOI layer isolation	2	RIE	Entire SOI

Table 4.2, the steps 2, 4, 5, 6 need mask and lithography. In total six lithography steps are operated during the whole process.

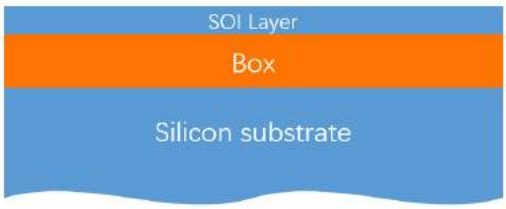
4.3 Process of fabricating the device

The UPTEG project, as all technical project, regardless the domain, have two main parts. First part is theoretical analyze and technical conception. This has been illustrated in the previous chapter in this report. The second part is fabrication processes, which in micro electric project includes not only fabrication, but also integration, characterization, packaging and testing. Among all factors, the layout that defines the size, placement and operation parameter in process flow, is the first key factor. While the second key factor is fabrication procedure, which directly leads to a success or a failure of the device. In this section, the full sequence of technological fabrication steps will be presented.

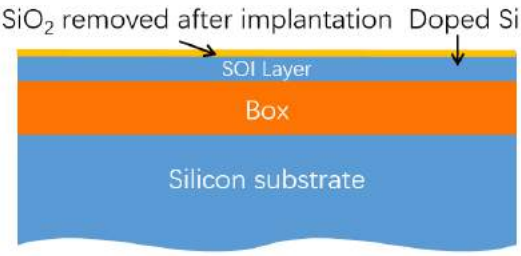
4.3.1 Process Overview

The process flow consists ten steps for suspending the SOI membrane from the Box and Si substrate and create a well-isolated collector both thermally and electrically. Electrodes connecting to emitter and collector with big surface gold pad for wire bonding and the final integration will also be made in these processes.

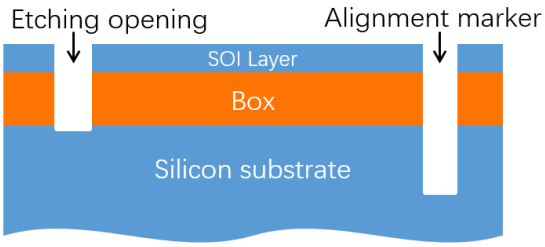
Figure *4.6* presents the full fabrication procedure of the Micrometer vacuum gap Thermionic energy Converter. Some repeated steps with minor importance in certain step are not over depicted for simplification reasons and better coherence.



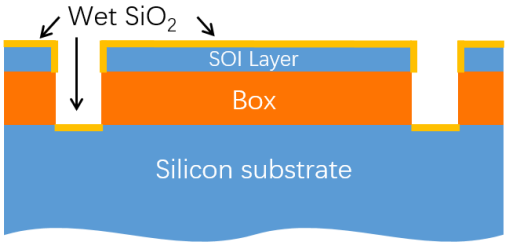
Step 0: Wafer cutting, polishing and cleaning



Step1: LPCVD SiO_2 thermal growth and implantation



Step2: Alignment markers and etching cavities



Step3: Etching openings sidewall protection

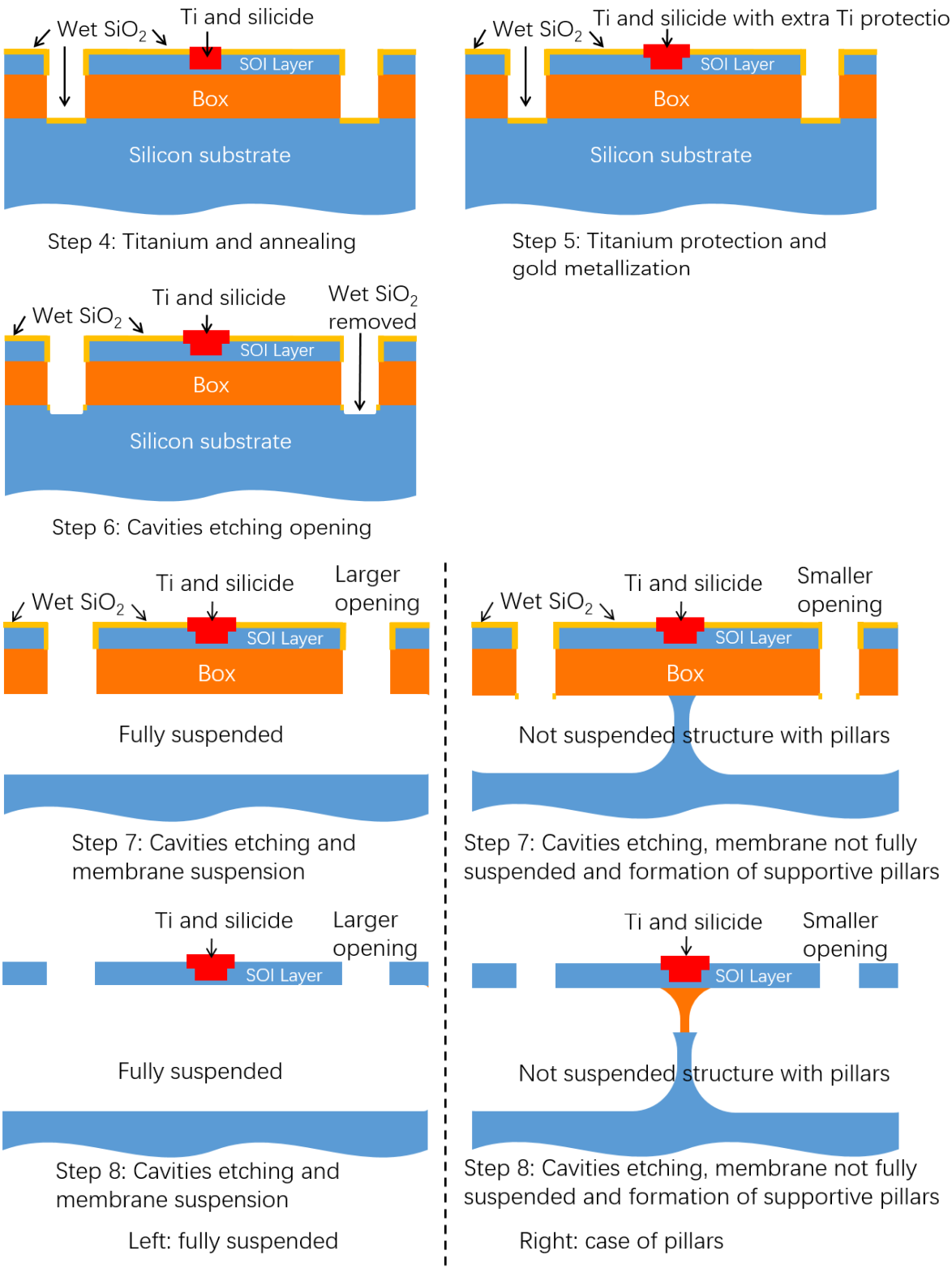


Figure 4.6 Full process flow of the MTC micro fabrication.

4.3.2 Step 0 - SOI wafer

Firstly, the wafer used in this fabrication technological work is SOITEC. The wafer has three layers including 200nm thick SOI layer and 400nm Box. The substrate is 710µm-740µm thick silicon. However,

the following fabrication procedure is compatible with different SOI and Box thicknesses while the preferred thickness of Box layer is ranging from 2µm to 10µm. The only difference in-between different SOI wafers are those etching time, including RIE and two-step vapor etching.

Parameter	Unit	Value
Full wafer diameter	Inch (mm)	3'' (76.2)
SOI thickness	nm	192.5 – 217.5
Box thickness	nm	395 – 405
Wafer thickness	µm	710 – 740
Orientation		100
SOI doping type		P type
SOI doped with		Boron
SOI resistivity	$\Omega \cdot \mathrm{cm}$	8.5 – 11.5

Table 4.3 Abstract from the used wafer datasheet (SOITEC)

The wafer diameter was 200mm, which is cut in four 3-inches wafers for fabrication process and five 1-inch wafers for technological tests. Before laser cutting, the 200mm wafers will be coated with thick photoresist to protect the SOI surface from particle sputtering. The cut wafer has a dimension of Ø76.4-76.5mm slightly larger than 3-inch wafers. Then the 3-inch wafers are sent to Siltronix for edges polishing. Although, diameter will be slightly smaller than before, the smooth border will increase the useable lithography area during spin-coating step.

4.3.3 Step 1 - SiO_2 thermal growth and implantation

According to the analysis of chapter 2.1, the N-type silicon will have lower work function. The first step is phosphorus implantation. The previous photoresist is first removed and the wafer is further cleaned in two steps. It was immersed into so-called piranha solution with 95% H2SO4 and 10% H2O2 in 1:1 ratio. After 10 minutes, rinsing by deionized water for 1 minute. Then by immerge the wafer into 5% HF solution the SiO2 created by previous step can be removed, leaving a clean and hydrophobic surface with Hydrogen-terminated [Huba 09] on top of silicon. This is the same cleaning steps mentioned in chapter 2, before alkali metal oxide characterization.

These processes above will remove all possible organic pollutions right before the Low Pressure Chemical Vapor Deposition (LPCVD). Right after the two-steps cleaning, LPCVD was performed. This is because the formation of the native oxide on the SOI layer is not wanted. The silicon dioxide thermally grown during the LPCVD has a thickness of 12nm, which has several advantages including higher purity, better uniformity, lower defects and better surface coverage properties. The last point is crucial in the later steps to build a protection layer.

Process stage	Time (minutes)	Temperature (°C)	Gas composition	Gas flow rate (dm^3/min)
1.1 Wafer introduction		$0 \rightarrow 500$	N_2	2.0
1.2 Heating	35	$500 \rightarrow 850$	N_2	1.5
1.3 Filling-up with Oxygen	10	850	O_2	1.5
1.4 Oxide growth	6	850	H_2/ O_2	2.5/1.5
1.5 Filling-up with Oxygen	15	850	O_2	1.5
1.6 Cooling	inertial	$850 \rightarrow 500$	N_2	2.0

Table 4.4 recipe of LPCVD for 12nm wet silicon oxide

Process stage	Time (minutes)	Temperature (°C)	Gas composition	Gas flow rate (dm3/min)
1.2 Wafer introduction		$0 \rightarrow 500$	N2	2.0
1.2 Heating	35	$500 \rightarrow 850$	N2	1.5
1.3 Filling-up with Oxygen	10	850	O2	1.5
1.4 Oxide growth	6	850	H2/ O2	2.5/1.5
1.5 Filling-up with Oxygen	15	850	O2	1.5
1.6 Cooling	inertial	$850 \rightarrow 500$	N2	2.0

Table 4.4 presents the growth of a layer of 12nm Silicon oxide by LPCVD. From the table, it can be noted that three main steps are realized. The wafer is introduced into the preheated oven with a temperature of 500°C. During this step, the chamber is purified with nitrogen. Then, the oven is heated and the temperature increases with a ramp of $10°C/\mathrm{min}$. In the second step, the oven remains at 850°C during the whole process. The critical step of oxide growth takes 6 min with an oxygen O2 and hydrogen flow rate of 1.5dm3/min and 2.5dm3/min respectively. The previous and following steps are purification steps. It can avoid gas pollution and improve the stability of thermal growth. At the last step, the temperature has inertial decrease with nitrogen flow of 2dm3/min. In this thermal growth process, the film stress is not an important factor, so the cooling temperature is not specifically controlled.

Comparing the molecular density of SiO2 and Si, the volume of SiO2 is 2.16 times larger than consumed silicon. Volume expansion occurs during silicon thermal oxidation. So, this step consumes about 5nm to 6nm Silicon during the oxidation process. The wet silicon oxide layer has a thickness of 10nm to 15nm reported by the LPCVD oven engineer.

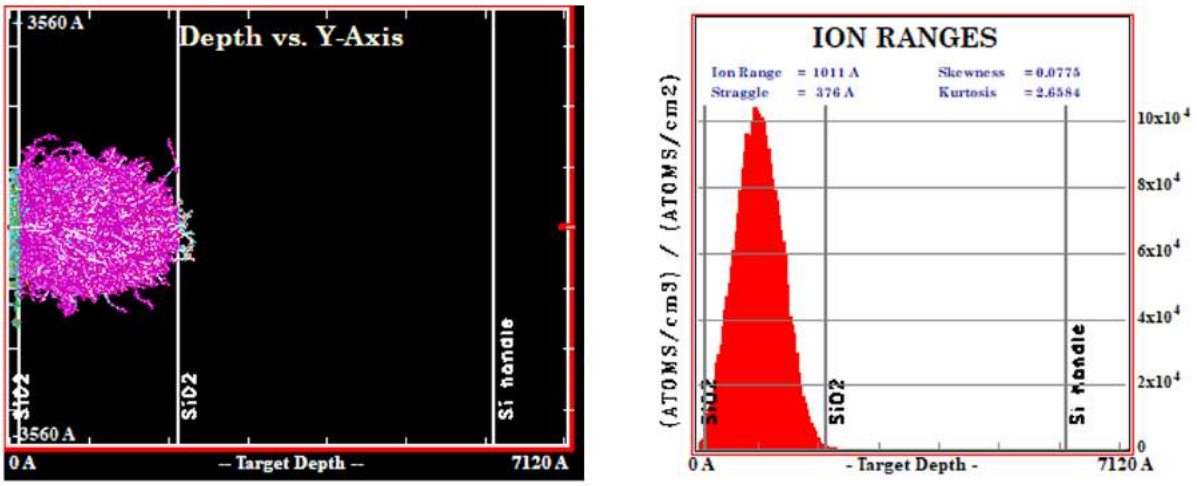


Figure 4.7 Parameters prepared for implantation. (a)Monte Carlo simulation on target wafer to determine doping energy for the target penetration depth. (b) Histogram of expected doping density.

In order to improve the electrical conductivity of silicon membrane collector and lower the Schottky barrier between interface of membrane and top metal electrode, an implantation step is applied at the beginning of the whole process. The expected doping depth is 200nm, from the wafer surface to the bottom of SOI layer. The doping depth, doping energy and doping density can be calculated by SRIM/TRIM software. Doping parameters are test and results presented in Figure *4.7*. The dopant kinetic energy of 70keV and dose of $1.8 \times 10^{14} atom/cm^2$ the implantation is applied to the wafer followed by a fast thermal annealing at 850K for 180 seconds. With this doping concentration, the membrane resistivity is expected to be $0.02\Omega \cdot \mathrm{cm}$. After the implantation, the sample is cleaned by HF solution with same operation processes parameters. This cleaning step is intended to remove the deposited 12nm SiO2, which is the sacrificial layer due to the annealing process.

4.3.4 Step 2 –Alignment marker and etching apertures

The fabrication of alignment markers and etching holes for membrane are two similar steps. The alignment markers are fabricated before the etching apertures. The only difference in-between these two steps are the etching depth. The alignment markers need a depth of more than 1µm in order to be easily found by the e-beam lithography machine, while the etching apertures are only 600nm deep until the surface of silicon handler. The deep alignments markers can be easily localized by the lithography machine in later steps during lithography process based on the electron beam contrast method. The procedure of both alignment marker and etching apertures processes are described in this section.

The fabrication of alignment marks is achieved by using electronic beam lithography resist PMMA (Poly Methyl MethAcrylate know as acrylic glass). The PMMA EL13%-MMA8.5 is a positive resist and for 12s 1000rpm, the spin-coating procedure will leave a uniform 1.8µm thick layer of resist. It is thicker than normal procedure, which is used to ensure that the resist will remain during the long Reactive Ion-Etching step. On 200/400nm SOI wafer, to etch for 1µm distance about 60 minutes are necessary.

No.	Process	Specification		Description
2.1	Micro-wave oxygen plasma cleaning (optional)	Power O_2 FLOW Duration	700W 525cm^2/min 15min	Cleaning all organic residuals and drying the wafer
2.2	Pre-coating heating on heating plate & cooling (optional)	Temperature Duration	80°C 1-2min	Removing organic residuals and drying the wafer
2.3	Spin-coating	Resist ID Speed Acceleration Duration	EL13%-MAA8.5 1000rpm 1000rpm/s 12s	Spin-coating of the electronic resist upon the wafer
2.4	Post spin-coating annealing on heating plate	T_{START} T_{END} Heating Ramp	80°C 180°C $< 10°C/min$	Heating the wafer to dry the resist, avoiding thermal stress.
2.4’	Post spin-coating annealing on heating plate (Alternative)	D_{START} D_{END} Descend speed	10mm 0mm $< 0.5mm/min$	Alternative method to control the heating ramp with integrated wafer support in heating plate.
2.5	Post spin-coating annealing on heating plate	Temperature Duration	180°C 10min	Final annealing, baking the resist to fully remove the resist.
2.6	Cooling the wafer to the room temperature	Duration	1-2min	Inertial cooling. Resist and wafer thermal stress release.

Table 4.5 Resist spin-coating procedure

In

No.	Process	Specification		Description
2.1	Micro-wave oxygen plasma cleaning (optional)	Power O2 FLOW Duration	700W 525cm2/min 15min	Cleaning all organic residuals and drying the wafer

2.2	Pre-coating heating on heating plate & cooling (optional)	Temperature Duration	80°C 1-2min	Removing organic residuals and drying the wafer
2.3	Spin-coating	Resist ID Speed Acceleration Duration	EL13%-MAA8.5 1000rpm 1000rpm/s 12s	Spin-coating of the electronic resist upon the wafer
2.4	Post spin-coating annealing on heating plate	TSTART TEND Heating Ramp	80°C 180°C $< 10°C/min$	Heating the wafer to dry the resist, avoiding thermal stress.
2.4’	Post spin-coating annealing on heating plate (Alternative)	DSTART DEND Descend speed	10mm 0mm $< 0.5mm/min$	Alternative method to control the heating ramp with integrated wafer support in heating plate.
2.5	Post spin-coating annealing on heating plate	Temperature Duration	180°C 10min	Final annealing, baking the resist to fully remove the resist.
2.6	Cooling the wafer to the room temperature	Duration	1-2min	Inertial cooling. Resist and wafer thermal stress release.

Table 4.5 first two steps are optional depending on the previous step and condition of wafer surface at the moment. After upgrading of the spin-coating annealing heating plate, the step 2.4’ is an alternative method to control heating ramp and thermal stress. This step is important because the thermal stress will lead to resist cracks at sharp pattern corners. Noting that for same step on certain samples resist may not be PMMA. For several times, other e-beam lithography resists like UV220 or else, which need less dose and better resistivity against plasma etching are applied as the mask material. However, in the later steps, the only resist is PMMA EL12-MMA8.5 and operation parameters are the same as listed in

No.	Process	Specification		Description
2.1	Micro-wave oxygen plasma cleaning (optional)	Power O2 FLOW Duration	700W 525cm2/min 15min	Cleaning all organic residuals and drying the wafer
2.2	Pre-coating heating on heating plate & cooling (optional)	Temperature Duration	80°C 1-2min	Removing organic residuals and drying the wafer
2.3	Spin-coating	Resist ID Speed Acceleration Duration	EL13%-MAA8.5 1000rpm 1000rpm/s 12s	Spin-coating of the electronic resist upon the wafer
2.4	Post spin-coating annealing on heating plate	TSTART TEND Heating Ramp	80°C 180°C $< 10°C/min$	Heating the wafer to dry the resist, avoiding thermal stress.
2.4’	Post spin-coating annealing on heating plate (Alternative)	DSTART DEND Descend speed	10mm 0mm $< 0.5mm/min$	Alternative method to control the heating ramp with integrated wafer support in heating plate.

2.5	Post spin-coating annealing on heating plate	Temperature Duration	180°C 10min	Final annealing, baking the resist to fully remove the resist.
2.6	Cooling the wafer to the room temperature	Duration	1-2min	Inertial cooling. Resist and wafer thermal stress release.

Table 4.5.

No.	Process	Technical Specifications	
2.7	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	25 to 50nA
		Beam step size	25nm
		Exposed layer	Alignment markers layer (yellow) Etching aperture (green) Membrane and SOI isolation (pink)

Table 4.6 Lithography description for alignment markers exposure (same exposure parameter are used for etching aperture layer, Membrane and SOI isolation layer, etc.). Color referred are corresponded to

Color	Layer number	Description	Step number	Processing technology	Related materials
Yellow	16	Alignment markers	2	RIE	Entire SOI
Green	3	Etching cavities	2	RIE	
Brown	4	Cavities etching cavities	6	RIE	Protection SiO2
Blue	5, 7	Titanium metallization	4 5	Evaporation Fast annealing	Titanium
Red	1	Gold metallization	5	Evaporation	Gold
Pink	6	Membrane and SOI layer isolation	2	RIE	Entire SOI

Table 4.2 and Figure 4.5

The minimum beam step size is 10nm, but a larger 25nm beam step size can accelerate the e-beam writing speed at the cost of lower resolution. Although the etching aperture and isolation layer are draw separately in Layout editor, they are processed in the same step.

After electron beam exposure, resist is developed in MIBK and IPA solution.

No.	Process	Technical Specifications	
2.9	Development	Solution	30ml MIBK + 60ml IPA
		Agitation	100rpm
		Mixing Duration	60 second
		Development Duration	60 second
2.10	Post development treatment	Iso-propanol (IPA) rinse	30 second
		Nitrogen dry blow	As long as needed

Table 4.7 Development procedure for PMMA resist

After development, resist is removed and patterns can be observed by optical microscope. Begin from the second electron beam exposure, by using optical alignment indicators the pattern position can be checked. Once the patterns for Reactive Ion Etching (RIE) are checked, sample is loaded in to Oxford

80plus etching machine. The graphite support is used in this process and the chamber is previously cleaned with suitable recipe (usually O2 plasma). The etching details are listed in

No.	Process	Target materials	Technical specifications	
2.11.1	Etching SOI layer	Silicon	Power	30 W
			SF6 flow	10 cm3/min
			Ar flow	10 cm3/min
			Pressure	10 mTorr
			Strike	50/0/5
2.11.2	Etching Box layer	Silicon oxide	Power	100 W
			CF4 flow	40 cm3/min
			N2 flow	40 cm3/min
			O2 flow	5 cm3/min
			Pressure	10 mTorr
			Strike	50/0/9
2.11.3	Etching substrate	Silicon (Only for alignment markers)	Power	30 W
			SF6 flow	10 cm3/min
			Ar flow	10 cm3/min
			Pressure	10 mTorr
			Strike	50/0/5
2.12	Stripping resist	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C	2H to 3H
			Rinsing Acetone-IPA	5 min each
			Dry by nitrogen blow	Until fully dry
2.12’			Acetone @ Room Temperature	About 10H
2.12’’			SVC or other remover	2H to 3H

Table 4.8.

No.	Process	Target materials	Technical specifications	
2.11.1	Etching SOI layer	Silicon	Power	30 W
			SF_6 flow	10 cm^3/min
			Ar flow	10 cm^3/min
			Pressure	10 mTorr
			Strike	50/0/5
2.11.2	Etching Box layer	Silicon oxide	Power	100 W
			CF_4 flow	40 cm^3/min
			N_2 flow	40 cm^3/min
			O_2 flow	5 cm^3/min
			Pressure	10 mTorr
			Strike	50/0/9
2.11.3	Etching substrate	Silicon (Only for alignment markers)	Power	30 W
			SF_6 flow	10 cm^3/min
			Ar flow	10 cm^3/min
			Pressure	10 mTorr
			Strike	50/0/5
2.12	Stripping resist	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C	2H to 3H
			Rinsing Acetone-IPA	5 min each
			Dry by nitrogen blow	Until fully dry

2.12’	Acetone @ Room Temperature	About 10H
2.12’’	SVC or other remover	2H to 3H

Table 4.8 Alignment markers and etching aperture procedure, RIE etching and resist stripping

To fabricate alignment markers all three sub-steps from 2.11.1 to 2.11.3 are necessary. To build etching opening and isolation pattern, only 2.11.1 and 2.11.2 are needed. During the above etching process, the end point detection signal is measured through small window above the sample with laser. It enables the operator to control the etching process and indicate on which material the plasma is etching. By calibration data of etching speed from previous experiments with the same etching machine and etching parameters, the etching process can be double checked. According to the PhD report of Maciej HARAS, The etching rate on silicon with the presented receipt is about 70nm per minute, and the SiO2 etching rate is 10.5nm per minute. In the experiment, for etching through the SOI layer, takes about 8 minutes and 30 second and about 35 to 40 minutes for BOX layer. The substrate etching process consumes 8 minutes. The extended SOI layer etching time is due to the observation for the change of endpoint signal curve and make sure the Box layer is exposed.

From the optical profilometer characterization result, presented in Figure *4.8*, all the markers have a depth of more than 1µm. It is a depth that is good enough for building an electron signal contrast for machine to recognize.

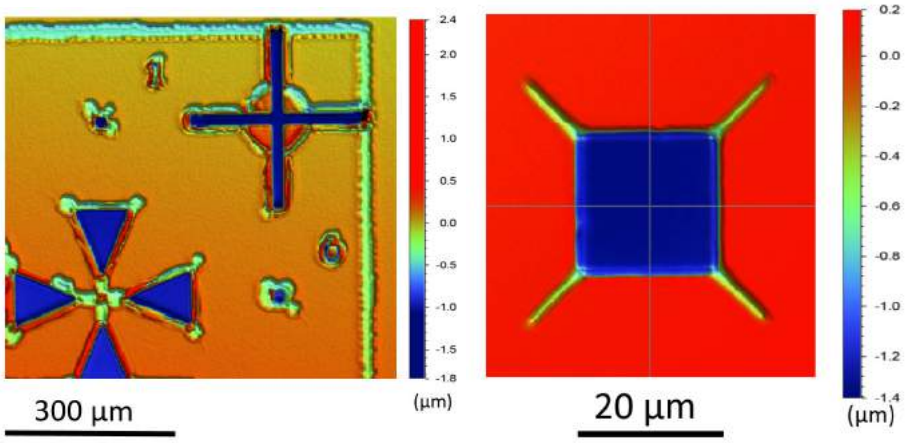


Figure 4.8 (a) Alignment indicator, alignment markers and optical alignment markers. (b) Alignment markers for lithography machine, type “mark20”.

Figure *4.8* presents three patterns for alignment. In Figure *4.8*(a), the bottom left is alignment indicators, upper right is optical alignment markers for pre-alignment before loading the sample into lithography machine and the other two small blue square are alignment marker type “mark20”. The indicators and two alignment markers presented are used. Figure *4.8*(b) presents an unused alignment marker with four corner cracks. These are unwanted patterns, however as the crack are small and the markers are far away from other patterns. The cracks here have no bad consequences. The 20µm square has four R2µm rounded corner has already reduced the length of corner cracks from about 30µm to about 10µm.

4.3.5 Step 3 - Sidewall protection

As presented in the full process plot, the two-steps vapor etching technique consists in Silicon etching and Silicon dioxide etching. Between these, silicon substrate need to be etched firstly due to the top SOI silicon membrane should be protected by silicon dioxide during the first etching process. The LPCVD wet silicon grown has a good sealing property. Therefore, the sidewall protection is design as coating the exposed silicon surface by LPCVD oxidation process. However, what needs to be aware is that the wafer with metal deposited will evaporate metal atoms and pollute the Chemical Vapor Deposition chamber. So sidewall protection is applied after the etching opening step and before metallization.

As presented in the first step, the wafer is cleaned by immersion into 5% HF acid for 1min right before introducing into the deposition chamber. The LPCVD 12nm silicon oxide deposition with same recipe presented in

Process stage	Time (minutes)	Temperature (°C)	Gas composition	Gas flow rate (dm3/min)
1.3 Wafer introduction		$0 \rightarrow 500$	N2	2.0
1.2 Heating	35	$500 \rightarrow 850$	N2	1.5
1.3 Filling-up with Oxygen	10	850	O2	1.5
1.4 Oxide growth	6	850	H2/ O2	2.5/1.5
1.5 Filling-up with Oxygen	15	850	O2	1.5
1.6 Cooling	inertial	$850 \rightarrow 500$	N2	2.0

Table 4.4. The result presented that not only the SOI surface is covered with SiO2, the SOI sidewall, substrate sidewall and etching Cavities etching apertures bottom are also covered with SiO2.

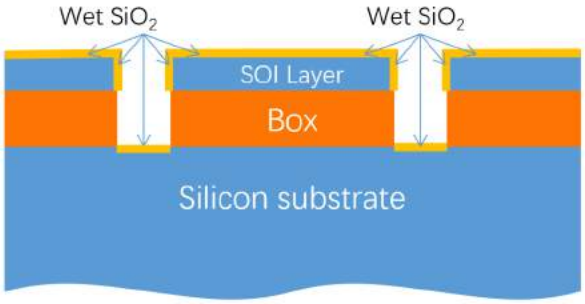


Figure 4.9 illustration of sidewall protection and incensement of volume after oxidation.

4.3.6 Step 4 – Titanium metallization and annealing

This titanium pattern has two functions. The first is to increase the conductivity of the highly doped silicon membrane and connect to the output position of the circuit. The second function is to serve as an adhesive layer between silicon and gold pad preparing for future wire bonding. The initial design used Platinum because the platinum has lower electrical barrier at the silicon-metal interface. However, the Platinum is not a good adhesive layer and the later deposited gold cannot stay on the silicon surface during the bonding process. So the alternative material is Titanium which is a good bonding adhesive candidate for gold pads and by process annealing after deposition, the Schottky barrier is lowered by creating a silicide. In this case, TiSi2 is the product after 750°C.

The Titanium pattern is made using the following procedure. Firstly, the same PMMA positive resist is spin coated on the wafer with same operation parameter and same baking process listed in

No.	Process	Specification		Description
2.1	Micro-wave oxygen plasma cleaning (optional)	Power O2 FLOW Duration	700W 525cm2/min 15min	Cleaning all organic residuals and drying the wafer
2.2	Pre-coating heating on heating plate & cooling (optional)	Temperature Duration	80°C 1-2min	Removing organic residuals and drying the wafer
2.3	Spin-coating	Resist ID Speed Acceleration Duration	EL13%-MAA8.5 1000rpm 1000rpm/s 12s	Spin-coating of the electronic resist upon the wafer
2.4	Post spin-coating annealing on heating plate	TSTART TEND Heating Ramp	80°C 180°C $< 10°C/min$	Heating the wafer to dry the resist, avoiding thermal stress.
2.4'	Post spin-coating annealing on heating plate (Alternative)	DSTART DEND Descend speed	10mm 0mm $< 0.5mm/min$	Alternative method to control the heating ramp with integrated wafer support in heating plate.
2.5	Post spin-coating annealing on heating plate	Temperature Duration	180°C 10min	Final annealing, baking the resist to fully remove the resist.
2.6	Cooling the wafer to the room temperature	Duration	1-2min	Inertial cooling. Resist and wafer thermal stress release.

Table 4.5. After spin-coating, electron beam lithography is subsequently performed. Details listed in

No.	Process	Technical Specifications	
4.1	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	10 to 15nA
		Beam step size	25nm
		Exposed layer	Platinum electrode layer

Table 4.9.

No.	Process	Technical Specifications	
4.1	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	10 to 15nA
		Beam step size	25nm
		Exposed layer	Platinum electrode layer

Table 4.9 Lithography exposure specification for platinum electrode.

Metal	Silicide	Formation Temperature (°C)	Melting point (°C)	Dominant diffusion species	Formation mechanism	Resistivity ($\mu\Omega \cdot cm$)
Ti	$TiSi_2$	700-900	1500	Si	Nucleation	29 – 96
	Co_2Si	300-450	1330	Co	Diffusion	110
Co	CoSi	460-650	1460	Si	Diffusion	147
	$CoSi_2$	650-900	1326	Co	Nucleation	15

Ni	Ni_2Si	200-350	1255	Ni	Diffusion	24
	NiSi	350-750	992		Diffusion	10.5
	$NiSi_2$	790-900	993		Nucleation	34
Pt	Pt_2Si	200-300	1372	Pt	Diffusion	30
	PtSi	300-450	1502	Si	Diffusion	28
Ir	IrSi	400-550		Si	Diffusion	

Table 4.10 Proprieties of Silicide formation, materials frequently used in microelectronic field. [Maex 95] [Baglin 81] [Ottaviani 81] [Zhu 04]

Metal	Silicide	Formation Temperature (°C)	Melting point (°C)	Dominant diffusion species	Formation mechanism	Resistivity ($\mu\Omega \cdot cm$)
Ti	TiSi2	700-900	1500	Si	Nucleation	29 – 96
Co	Co2Si	300-450	1330	Co	Diffusion	110
	CoSi	460-650	1460	Si	Diffusion	147
	CoSi2	650-900	1326	Co	Nucleation	15
Ni	Ni2Si	200-350	1255	Ni	Diffusion	24
	NiSi	350-750	992		Diffusion	10.5
	NiSi2	790-900	993		Nucleation	34
Pt	Pt2Si	200-300	1372	Pt	Diffusion	30
	PtSi	300-450	1502	Si	Diffusion	28
Ir	IrSi	400-550		Si	Diffusion	

Table 4.10 presents several commonly used materials and some correspond parameters. By comparing the resistivity of TiSi2 to the resistivity of highly doped silicon membrane, the metal silicide has much lower resistivity and better conductivity. However, during the formation process, the product of silicide will penetrate in to the silicon surface. The depth of penetration and silicon consummation is presented in Figure *4.10*. With 200nm silicon SOI layer and 60nm thickness Ti, the silicide will not totally penetrate down to the bottom of SOI.

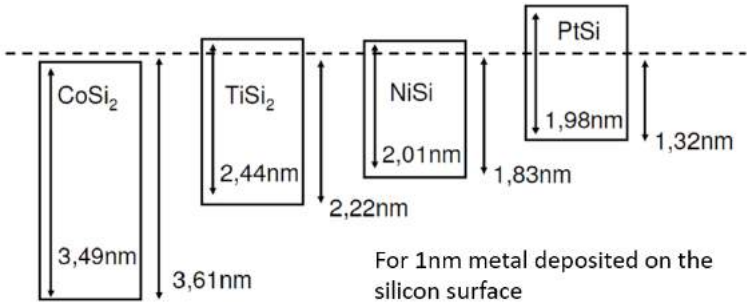


Figure 4.10 Penetration depth of silicide on silicon surface during annealing process [Breil 09]

The metallization is performed by the evaporation and this technique can deposit a very thin layers of metal. The technical parameters are presented in

No.	Process	Material	Specifications	
4.2	Pre-deposition plasma cleaning	Argon	Clean duration	120 Seconds
			Power of plasma	200 eV
4.3	Evaporation	Titanium	Deposit thickness	60 nm
			Evaporation speed	0.1 nm/s
4.4	Lift-off		UV exposure	15 mins (optional)

	PMMA EL13%-MMA8.5	Remover PG @ 65°C	2H to 3H
		Rinsing Acetone-IPA	5 min each
		Nitrogen dry blow	Until totally dry

Table 4.11. The argon etching step is intended to increase metal adhesion onto the host substrate.

No.	Process	Material	Specifications	
4.2	Pre-deposition plasma cleaning	Argon	Clean duration	120 Seconds
			Power of plasma	200 eV
4.3	Evaporation	Titanium	Deposit thickness	60 nm
			Evaporation speed	0.1 nm/s
4.4	Lift-off	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C	2H to 3H
			Rinsing Acetone-IPA	5 min each
			Nitrogen dry blow	Until totally dry

Table 4.11 Evaporation procedure specification. Lift-off procedure specification

The metal is deposited on the whole surface of the 3 inches wafer. After the deposition, removing the resist will also remove metal film at unwanted position, creating a pattern same as lithography. This removing resist process is called lift-off instead of stripping. Parameters are presented in

No.	Process	Material	Specifications	
4.2	Pre-deposition plasma cleaning	Argon	Clean duration	120 Seconds
			Power of plasma	200 eV
4.3	Evaporation	Titanium	Deposit thickness	60 nm
			Evaporation speed	0.1 nm/s
4.4	Lift-off	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C	2H to 3H
			Rinsing Acetone-IPA	5 min each
			Nitrogen dry blow	Until totally dry

Table 4.11 and alternative method are 2.12'' in

No.	Process	Target materials	Technical specifications	
2.11.1	Etching SOI layer	Silicon	Power	30 W
			SF6 flow	10 cm3/min
			Ar flow	10 cm3/min
			Pressure	10 mTorr
			Strike	50/0/5
2.11.2	Etching Box layer	Silicon oxide	Power	100 W
			CF4 flow	40 cm3/min
			N2 flow	40 cm3/min
			O2 flow	5 cm3/min
			Pressure	10 mTorr
			Strike	50/0/9
2.11.3	Etching substrate	Silicon (Only for alignment markers)	Power	30 W
			SF6 flow	10 cm3/min
			Ar flow	10 cm3/min
			Pressure	10 mTorr
			Strike	50/0/5
2.12	Stripping resist	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C	2H to 3H

	Rinsing Acetone-IPA Dry by nitrogen blow	5 min each Until fully dry
2.12’	Acetone @ Room Temperature	About 10H
2.12’’	SVC or other remover	2H to 3H

Table 4.8 by using SVC instead of PG remover.

No.	Process	Specifications			Description
		Duration (s)	Temperature (°C)	N_2H_2 filling speed (sccm)	
4.5	Quick Thermal Annealing	45	25	2000	Purge chamber
		15		500	Test gas valve
		600	25 to 750	500	Heating with PID control
		120	750	500	Annealing
		60		500	Heating off, Inertial cooling
		360		0	Liquid Cooling down

Table 4.12 Jipelec quick thermal annealing procedure specification.

No.	Process	Specifications			Description
		Duration (s)	Temperature (°C)	N2H2 filling speed (sccm)	
4.5	Quick Thermal Annealing	45	25	2000	Purge chamber
		15		500	Test gas valve
		600	25 to 750	500	Heating with PID control
		120	750	500	Annealing
		60		500	Heating off, Inertial cooling
		360		0	Liquid Cooling down

Table 4.12 presents the details of thermal annealing after titanium deposition. Silicide formed during the annealing will increase the thermal conductivity of whole silicon membrane. However, the silicide will lead to some problems. Due to the volume change and silicon penetrated, the protection layer covered on top of SOI surface has some crack on the border of silicide. It can be observed and thus protection process is needed. If not during the XeF2 etching process, the vapor will not only etch silicon substrate from etching cavities but also SOI membrane through these cracks.

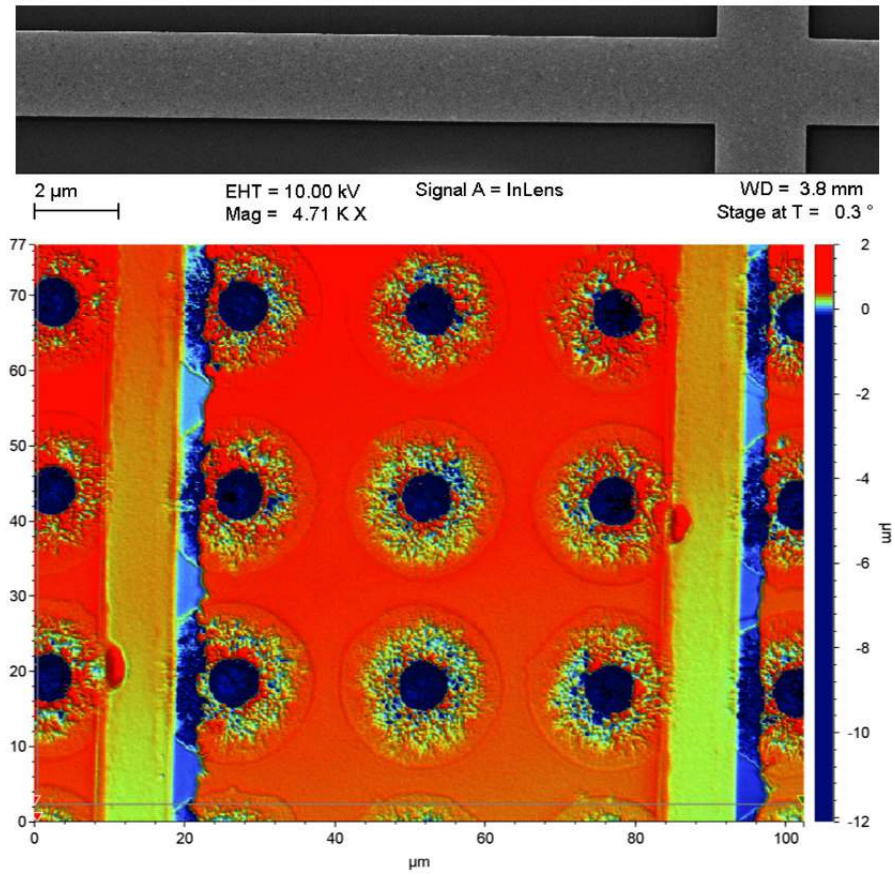


Figure 4.11 (a) SEM image after annealing. (b) Broken membrane after XeF2 vapor etching mapped by optical profilometer.

The darker line beside the Titanium path and membrane breaking from the border of titanium presented in Figure *4.11* is observes in annealed sample while not observed in the sample without annealing process. So if the annealing is applied to the sample, one more layer of protection need be operated especially at near Titanium pattern position to cover the cracks. However, the LPCVD is not possible to apply due to metal pollution to the chamber, which has been discussed earlier. The alternative method is to coat a slightly larger width path with Titanium on the same position to cover the border of Titanium silicide.

4.3.7 Step 5 – Titanium protection and gold metallization

The protection layer titanium is deposited in exactly the same method. For overlapping of 250nm larger width on single side is not enough to protect Si-Ti bordering from XeF2 etching. So the overlapping Ti layer is more than 1 µm larger than the first titanium layer, present in Figure *4.12*. All details are presented in

No.	Process	Technical Specifications	
4.1	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	10 to 15nA
		Beam step size	25nm
		Exposed layer	Platinum electrode layer

Table 4.9 and

No.	Process	Material	Specifications	
4.2	Pre-deposition plasma cleaning	Argon	Clean duration Power of plasma	120 Seconds 200 eV
4.3	Evaporation	Titanium	Deposit thickness Evaporation speed	60 nm 0.1 nm/s
4.4	Lift-off	PMMA EL13%-MMA8.5	UV exposure Remover PG @ 65°C Rinsing Acetone-IPA Nitrogen dry blow	15 mins (optional) 2H to 3H 5 min each Until totally dry

Table 4.11, so the step 5.1 is to repeat the step 4.1 to 4.4.

When Ti protection layer is completed, the subsequent Gold (Au) metallization is operated. The Au is used to create a big pad for the wire bonding. It is one of the best candidate for bonding due to the good contacting property with probes. Furthermore, the wire bonding also uses gold wires and can build a good electrical contact on gold pad. Generally speaking, the metallization is performed in the same way as Titanium. The only different is the deposition thickness, which is 400nm instead of 60nm. Due to its square shape and large surface, the electron beam lithography will apply bigger step size in higher current. The 25nm step size is the highest value allowed for the machine. The spin-coating process for this step remains the same and the lithography exposure parameters are listed in

No.	Process	Technical Specifications	
5.2	Lithography exposure	Dose Current Beam step size Exposed layer	$450\mu C/cm^2$ 50nA 25nm Gold pad layer

Table 4.13.

No.	Process	Technical Specifications	
5.2	Lithography exposure	Dose Current Beam step size Exposed layer	$450\mu C/cm^2$ 50nA 25nm Gold pad layer

Table 4.13 Lithography exposure specification for platinum electrode

Due to the big pad surface, the minimum dose factor for lithography is changed from 0.1 to 1 in the gold pattern writing process. This will avoid underdoping at the center of the gold pad. Noting that the thickness of resist is 1.8µm, which is 4 times larger than the evaporated metal. This will be helpful for lift-off step. The evaporation steps are similar to the previous step with same lift-off process presented in

No.	Process	Material	Specifications	
5.3	Pre-deposition plasma cleaning	Argon	Clean duration Power of plasma	120 Seconds 200 eV
5.4	Evaporation	Gold	Deposit thickness Evaporation speed	400 nm 0.1 nm/s

5.5	Lift-off	PMMA EL13%-MMA8.5	UV exposure Remover PG @ 65°C Or SVC @ 65°C Rinsing Acetone-IPA Nitrogen dry blow	15 mins (optional) 2H to 3H 5 min each Until totally dry

Table 4.14.

No.	Process	Material	Specifications	
5.3	Pre-deposition plasma cleaning	Argon	Clean duration Power of plasma	120 Seconds 200 eV
5.4	Evaporation	Gold	Deposit thickness Evaporation speed	400 nm 0.1 nm/s
5.5	Lift-off	PMMA EL13%-MMA8.5	UV exposure Remover PG @ 65°C Or SVC @ 65°C Rinsing Acetone-IPA Nitrogen dry blow	15 mins (optional) 2H to 3H 5 min each Until totally dry

Table 4.14 Parameters of the gold metalliztion and lift-off.

The thickness of Gold pad is measured by profilometer and the measured thickness is correspond to the design.

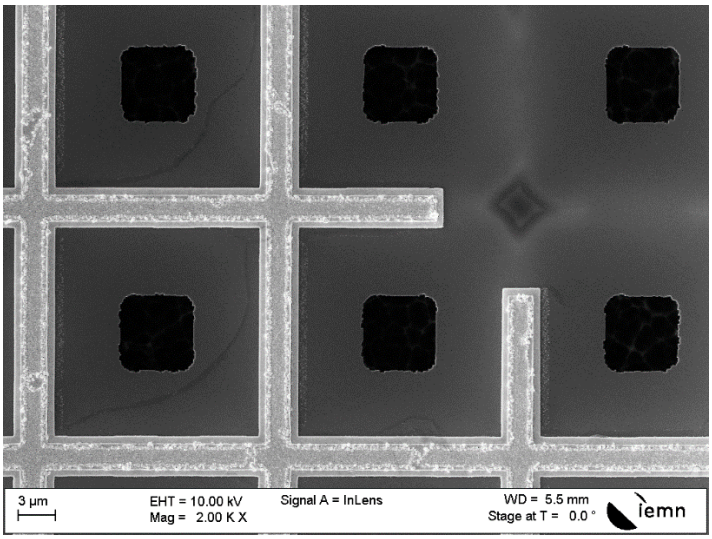


Figure 4.12 The titanium electrode with annealing process is 2µm wide, the second titanium layer is 3µm wide.

4.3.8 Step 6 – Cavities etching apertures

The membrane suspension begins from etching the protection on the etching cavities. The covered Silicon dioxide layer fabricated in step 3 needs to be removed before the XeF2 vapor etching, which expose the Silicon to the etching vapor. The etching of Si will then happen at the exposed surface. The spin-coating process is the same as previously presented, details listed in

No.	Process	Technical Specifications	
2.9	Development	Solution Agitation	30ml MIBK + 60ml IPA 100rpm

2.10	Post development treatment	Mixing Duration Development Duration Iso-propanol (IPA) rinse Nitrogen dry blow	60 second 60 second 30 second As long as needed

Table 4.7 and in

No.	Process	Technical Specifications	
4.1	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	10 to 15nA
		Beam step size	25nm
		Exposed layer	Platinum electrode layer

Table 4.9. After step 6.1 is the electron beam lithography. Specifications are listed in

No.	Process	Technical Specifications	
6.2	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	20nA
		Beam step size	10nm
		Exposed layer	Sidewall protection layer

Table 4.15. With comparatively lower current and thinner resist film, the alignment is easier and have better lithography result. This is a more important lithography step than before.

No.	Process	Technical Specifications	
6.2	Lithography exposure	Dose	$450\mu C/cm^2$
		Current	20nA
		Beam step size	10nm
		Exposed layer	Sidewall protection layer

Table 4.15 Lithography exposure specification for remove protection layer on etching cavities.

The patterns are slightly smaller than the etching cavities in step 2, which can be observed after development in Figure *4.13*. Before the RIE etching process, the result needs to be verified. Because not fully opened patterns will lead to a huge pillar with massive heat losses and failure to build a temperature difference between substrate and membrane for MTC. The wafer after development will be laser cut, with SOI layer facing downside and away from the laser spot. The MTC devices on the same wafer will be separated in small dies in 16mm by 10mm size. For the subsequent steps samples are processed separately or in small groups.

After lithography exposure and development, the SiO2 can be removed by RIE and with the same recipes presented in step 2.11.2. Based on CF4 , N2 and O2 the etching is operated without the endpoint detection. The film to etch is so thin that hardly any signal change can be observed. By the previous etching experience, the etching time is set to 2minutes and 45 second. According to the etching speed calibration, this time is too long and sample is over etched. This longer etching time is useful to compensated the decreased etching rate usually associated to deep and narrow patterns. While the slightly extended etching will not leads to important defect for following steps. The optical profilometer measurement image after stripping is presented in Figure *4.13*. However, in real fabrication process the resist coated for this step will stay on the surface until XF2 vapor etching step (step 7) is finished. So stripping will apply after step 7.

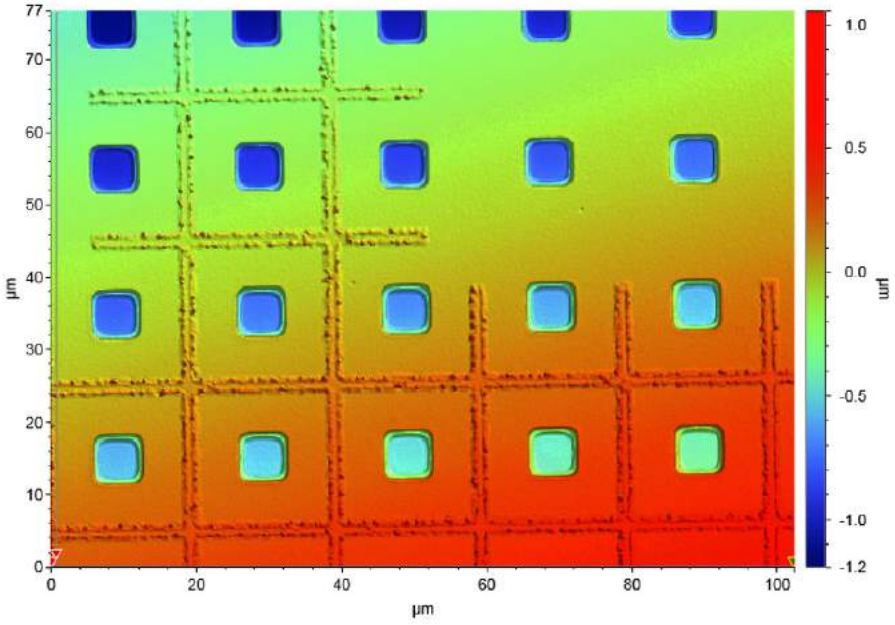


Figure 4.13 Image of optical profilometer measurement.

The etched patterns are inside the pre-etched holes and the step down patter can be easily observed under optical microscope. From Figure *4.13*, we checked that the measured etching depth is much larger than 12nm, so all the etching cavities are well exposed. After RIE, the sample should not be exposed in the atmosphere for a long time, due to Silicon oxidization. Therefore, the RIE step and membrane suspension steps are usually operated with the following steps in the same day.

4.3.9 Step 7 – Membrane suspension

Right after the RIE process, the sample is transported in to XeF2 vapor etching machine. Thanks to the isotropic etching properties of vapor etching, the membrane composed of SOI, Ti and Box can be released from Silicon substrate. Other commonly used vapor etching techniques, are wet etching process for silicon like preheated KOH [Canavese 07] [Divan 99] [Palik 91] [Tanaka 04] or TMAH solutions [Liebert 02] [Powell 01] [Yang 05] [Tabata 92]. These will not provide a stable isotropic etching rate. Another reason these wet etching techniques are not applicable is that the top surface of suspended membranes need further protection and the wet processes are risky to destroy sue to sticky force create during drying procedure.

In this case, to avoid using liquid solutions, the XeF2 vapor etching is the best candidate as a silicon etchant [Brazzle 04] [Winters 79] [Williams 03]. Corresponded chemical formula presented below.

$$2\mathrm{XeF}_2(g) + Si \rightarrow 2Xe(g) + SiF_4(g) \qquad \text{Eq 4. 30}$$

Other than silicon, all substance in reactive equation are in gaseous phase. Due to its unique isotropic etching properties and all reactive products in gaseous phase, this technique was studied and investigated by numerous groups. For us, also benefiting from these properties, the etching procedure can suspend the membrane without using an additional mask or lithography process.

No.	Process	Technical Specifications	
7.1		XeF_2 input pressure	3.0 Torr

	Si substrate etching, suspension of membrane by XeF_2 vapor etching	XeF_2 pump out pressure	0.8 Torr
		etching cycle	6 - 8
		Single cycle etching duration	10 s
		Single cycle operation duration	17 – 19 s
		Operation mode	Advanced normal

Table 4.16 XeF_2 vapor ethcing specification

The XeF2 vapor etching procedure is the most important step among all technical processes. The suspension process will create the micro gap for MTCs. Two critical parameters, the gap distance between emitter and collector and the cross section of pillars are controlled by the etching parameters. Thus, knowing the operating mechanism is important. First of all, the device has two preparing chambers and one etching chamber where the sample is loaded. The input pressure in

No.	Process	Technical Specifications	
7.1	Si substrate etching, suspension of membrane by XeF2 vapor etching	XeF2 input pressure	3.0 Torr
		XeF2 pump out pressure	0.8 Torr
		etching cycle	6 - 8
		Single cycle etching duration	10 s
		Single cycle operation duration	17 – 19 s
		Operation mode	Advanced normal

Table 4.16 control the pressure of XeF2 in preparing chamber. Then after all preparing procedures in the recipe beginning finished, the etching chamber is vacuumed and once the pressure reach pump out pressure one of the etching chamber is connected to preparing chamber. Due to higher pressure in preparing chamber, etching gas will leave the preparing chamber and fill the etching chamber. The single cycle etching duration time controls the connecting time in-between etching chamber and preparing chamber. After certain time, the valve is closed and the etching chamber is evacuated and pumped down to the pump out pressure. Then the second etching cycle begins. This process ensures that the quantity of reactant gas is constant for a given set of parameters. The reaction is limited by the amount of XeF2 and gas pressure. The software interface will tell the whole cycle operation time that is normally from 15 second to 19 second. In the fabrication of MTC devices, the etched dimensions need to be fully controlled in micrometer size. So all influential parameters should be considered. For small exposed etching cavities surface, a lower XeF2 input pressure is set to 3.0 Torr and pump out pressure is set to 0.8 Torr. 0.8 Torr is a pressure can easily reached after only several seconds of pumping. In normal condition, the performance condition of dry vacuum pump in this etching platform will influence the single cycle operation duration by several seconds that is an acceptable range. A lower pump out pressure setting will increase the influence of pump performance status, while a higher pump out pressure setting will reduce the etching efficiency. Therefore, a balance etching setting is important.

After numerous tests and investigation, we find that the first cycle after the loading of sample is less effective and has slower etching speed than the next cycles. The reason is the preparation procedure before the etching that purges the chamber with nitrogen and dilutes the etching gas compared to the cycle intervals in a single process. However, unlike the first cycle, from the second cycle, the chamber is filled with Xenon difluoride with Silicon tetrafluoride with much less dilution.

The expected etching depth and etching range are about 10µm in 6 to 8 cycles. With the etching cavities patterns, the etching speed can be controlled at different position. Due to the cavity structure

with aperture for intake of etchant gas, the isotropic etching has different speed at different cavities. What we find is that the etching speed is slightly larger inside cavities with larger aperture patterns and slower in small-opening cavities. The aperture dimension works as the valve to control the intake gas during etching cycles and thus controls the etching speed. In other words, the small patterns in the previous step works as a “chock” that will limiting the etching reaction in the cavity. Consequently, after several cycles, smaller etching apertures lead to small cavities while larger opening patterns create larger cavities. According to this phonmenon, by controlling the etching cavity patterns in step 6, pillar distribution can be locolised and arranged. The Figure *4.14* present the etching results.

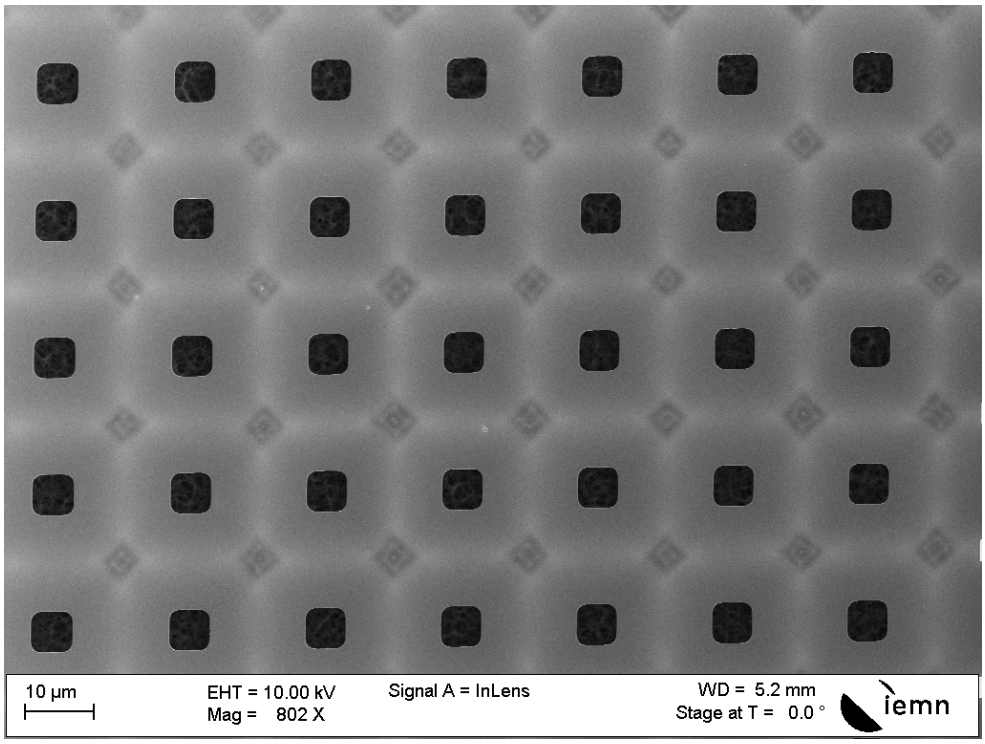


Figure 4.14 SEM image after membrane suspension from silicon substrate. The lighter out border is the result of XeF_2 etching, while the inner border represents the remaining SiO_2 after HF vapor etching.

The structures below the membrane can be observed transparently by both optical microscope and scanning electron microscope. From Figure *4.14*, the nearly square shape pillars can be observed even under metal electrodes. The maximum etch distance that is also the maximum vacuum gap dimension can be easily measured, in addition the pillar section surface can be observed and measured. So after calibration of etching distance for different etching cavities with different numbers of cycles, the etching parameters can be exported. For the best result, the minimum dimension of the pillar is about 1µm to 2µm. In the future, in order to better control the etching progress, a microscope with real time observation on the transparent cover of etching chamber would be greatly helpful.

To avoid Ti-Si border etching, the PMMA resist is removed after this step by Acetone for a long time, usually overnight, at room temperature. Then, the sample is transferred into IPA for Acetone removing during 10 minutes. Due to the fragile membrane, the IPA naturally evaporates with low-pressure nitrogen airflow.

4.3.10 Step 8 –SiO_2 etching to minimize pillars cross-section

The last fabrication step before loading the device into vacuum chamber is Silicon dioxide etching. This process can further minimize the cross-section of pillars with precise control. This is due to the stable and slow etching rate by HF vapor. This dry etching technique has the same isotropic etching property. The mechanism of the vapor etching process can be described by the following chemical equation.

$$SiO_2 + 4HF(g) \rightarrow 2SiF_4(g) + 2H_2O(g) \qquad \text{Eq 4. 2}$$

Thanks to the previous adoption of this technique, the mechanical stress occurring during etching is significantly reduced in low pressure environment [Bois 01] [Zhao 15] [Haras 16]. Similar to previous step, the etching vapor together with two by-products of this reaction are in gaseous phase, which is easy to evacuate.

No.	Process	Technical Specifications	
8.1	Pre-etching heating	Temperature Duration	260°C 2 min
8.2	Box under etching, Oxide removing	HF flow C_2H_5OH flow N_2 flow Single cycle etching duration Number of cycles Operation mode	350 cm^3/min 350 cm^3/min 1250 cm^3/min 16 min 1 Recipe 2

Table 4.17 Parameters of removing oxide and box layer by HF dry vapor etching.

The parameters of etching SiO2 is modified according to the minimum dimension measured after Xenon difluoride etching. This will help in limiting the conductive heat loss through pillar structures. The 16 minutes (960 seconds) etching time corresponds to about 400nm etching thickness for devices with perfect pillar cross-section, where the minimum dimension is about 1µm to 2µm. In this case, the remaining pillars cross-section after HF vapor etching will be about 1µm2 that is ideal size for limiting the heat losses based on FEM modeling in chapter 3. For samples with larger cross-section after previous step, the etching time with HF vapor can be increased for compensation.

The step 8.1, pre-etching heating procedure removes the possible solvent including IPA, acetone or water from the surface. Then, the sample is introduced to the low pressure etching chamber. The etching process also progresses in cycles. However with different equipment configuration and the etching gas is controlled by introduction flow, the etching cycle with long duration remains an effective etching speed all the time. So only one cycle is applied with longer etching time. The procedure in

No.	Process	Technical Specifications	
8.1	Pre-etching heating	Temperature Duration	260°C 2 min
8.2	Box under etching, Oxide removing	HF flow C2H5OH flow N2 flow Single cycle etching duration Number of cycles Operation mode	350 cm3/min 350 cm3/min 1250 cm3/min 16 min 1 Recipe 2

Table 4.17 deletes the post-etching heating step. This is because the sample after etching should be transferred into vacuum chamber in minimum time avoiding oxidation, while the post-etching heating may lead to the oxidation of the exposed silicon surface.

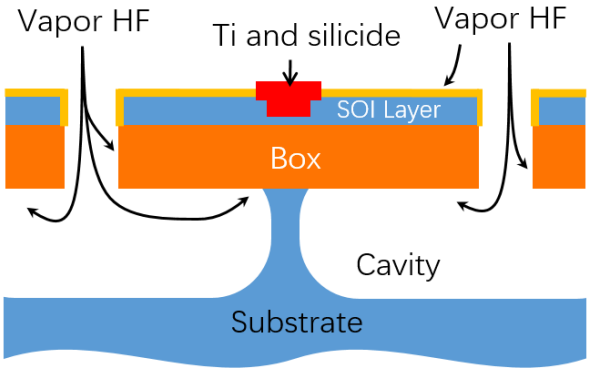


Figure 4.15 schematic diagram for HF vapor etching.

Compared to the etch rate calibrated in cleanroom database, which is 37.4nm/min, the real etching speed is about half of the calibrated value. Reasons are listed as follow: First, the box layer is not well exposed to HF, the small cavity limit the vapor flow through target material surface presented in Figure *4.15*. Second, the single cycle etching process with constant vapor flow means that the gas inside the cavity has less circulation. Furthermore, with the progress of etching, the silicon oxide is far away from the aperture patterns and exposed surface is smaller than initial. Therefore, the etching keeps slowing down during the procedure.

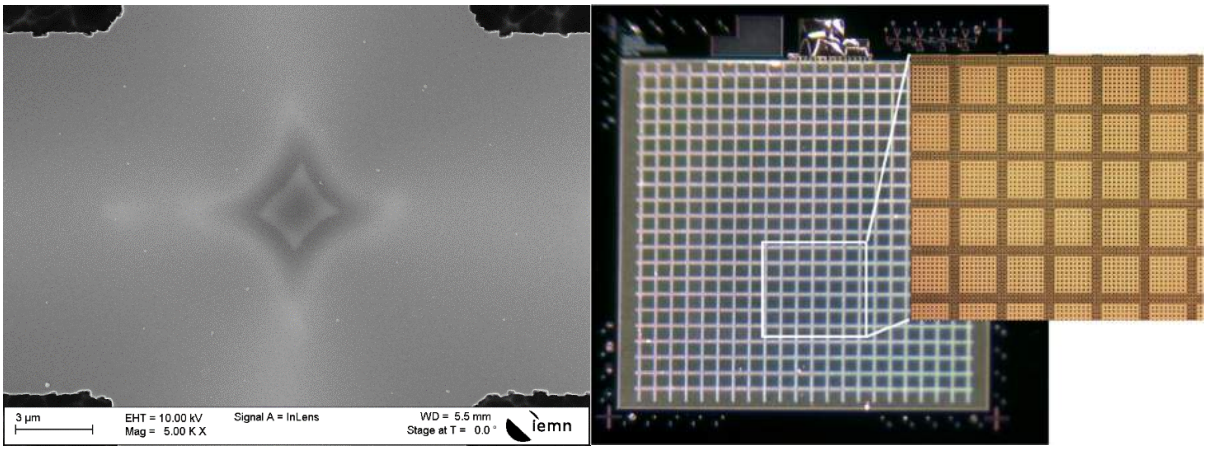


Figure 4.16(a)SEM images of samples for HF vapor etching speed calibration. (b)Optical microscope images with a global view of sample.

Although the HF vapor-etching machine has etching rates calibrated with different recipe each several month and the data shows an etching speed of 459nm per 10 minutes. Due to complex inner structure and small openings, the etching process on the MTC sample is unlike other suspension etching process that has a slower etching rate than normal condition. After etching with recipe 2 for 10 minutes and two cycles, the etching distance is about 650-700nm, which is measured on SEM images. So the etching rate is about 325-350nm per cycles (10 minutes). Compared to XeF2 vapor etching HF vapor etching has slower speed and etching rate is more stable. Therefore, with the HF vapor etching step, a precise control of pillar size is reliable and highly repeatable. The targeted pillar critical size, which is $1\mu m$ at box layer, is a critical parameter for thermal isolation according to the calculation and simulation in chapter 3. The silicon oxide pillar and global view of the MTC sample are presented in Figure *4.16*(a) and Figure *4.16*(b). By opening sidewall protection for SOI membrane, we can observe the expected

silicon dioxide pillar position, which is located at the geometric center of square shape opening presented in Figure *4.17*.

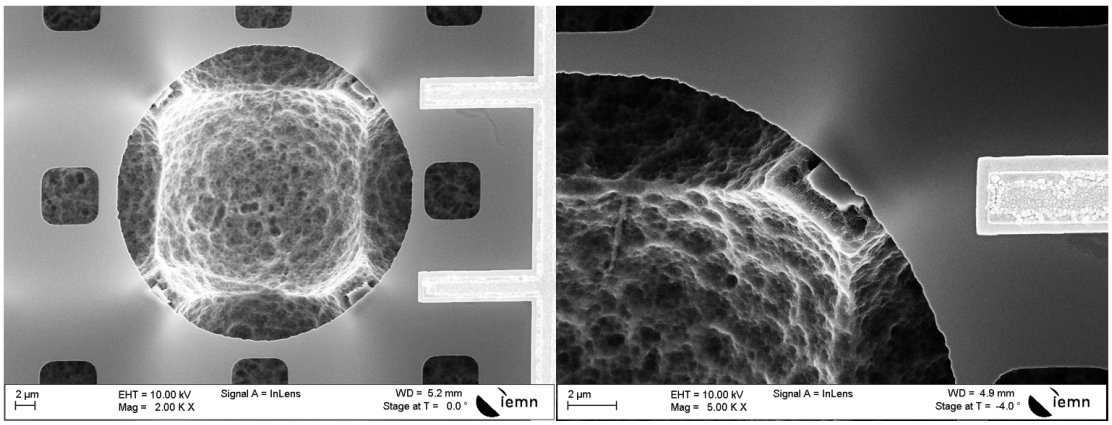


Figure 4.17 SEM images of sample surface after HF vapor etching. (a) The unprotected SOI silicon layer lead to a round opening. (b) Through the opening, the Silicon pillar formed by step 7 and the the silicon dioxide pillar position can be observed.

One thing that needs to be mentioned is that after XeF2 vapor etching, the inner stress of Silicon dioxide will lead to a wavy membrane and the uneven membrane surface will return to flat shape after HF etching, when most of silicon dioxide is removed and the stress on membrane is released. At the end of fabrication process, at the position where SiO2 pillar is entirely removed due to over etching, a wavy surface can be observed by optical microscope. For membrane with evenly distributed SiO2 pillars, it will stay flat with height difference on silicon less than 100nm. Figure *4.18* presents the pillar shape by removing the silicon membrane by reactive ion etching. The SEM image shows that by controlling etching cavity in step 6, the pillar distribution can be organized.

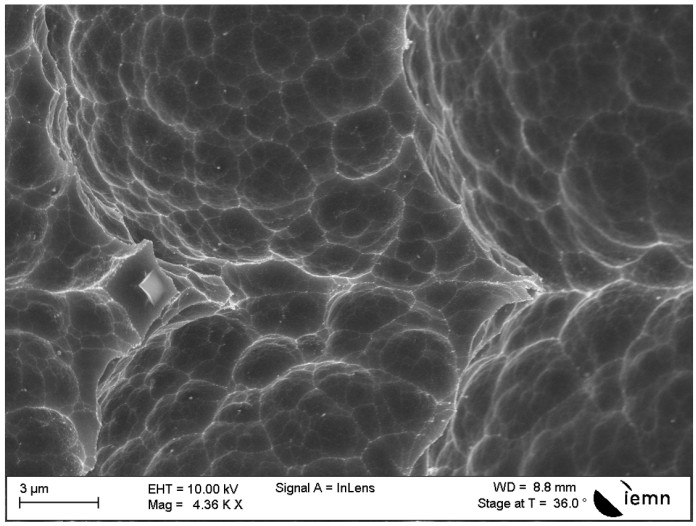


Figure 4.18 SEM images of pillar shape. (left) Pillar with box layer remained, (right) over etched pillar with box layer totally removed.

4.4 Device mounting for characterization

4.4.1 Mounting design for mechanical fixation, electrical insulation and connection

The integration is developed based on a metallic platform for loading the sample into vacuum chamber. As presented in Figure *4.19*. The sample holder has four screws for thin metal clips presented in Figure *4.20* to fasten both SOI sample (MTC device) and holder wafer. Two contact pillars provide electrical accessibility for measurement inside the vacuum chamber. One pillar is equipped with a ceramic isolation ring, while the other pillar without ceramic isolation ring is grounded. The electrical design is to connect the left pillar to the SOI membrane and the grounded pillar connect to the silicon substrate. Then, by the two BNC ports the Agilent semiconductor parameter analyzer can be connected to the MTC device inside the vacuum chamber.

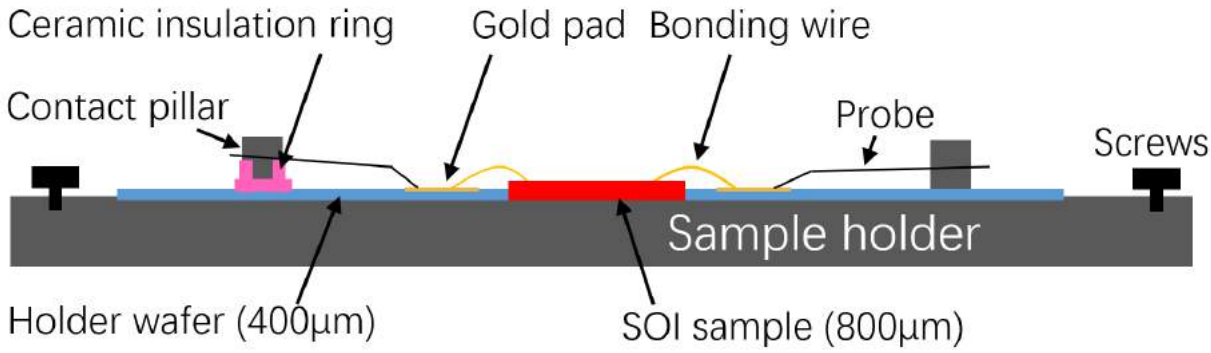


Figure 4.19 Schematic diagram present the layout of the measurement plantfrom in vacuum chamber

As presented in Figure *4.19*, a holder wafer is used in order to build reliable electrical contact from sample dies to BNC connecter. Firstly wire bonding technique connect the sample dies to the large gold pads on holder wafer by gold bonding wires. Than the metal probes fastened by on pillars have solid electrical contact to the large gold pads on the holder wafer and have good electrical contact to pillars at the same time. The pillars on the sample holder function as stands for probes, which is connected to metal pins inside vacuum chamber. Therefore, thermal current from MTC device can pass through the holder wafer to the pillar and finally be measured by the Agilent analyzer by BNC cables.

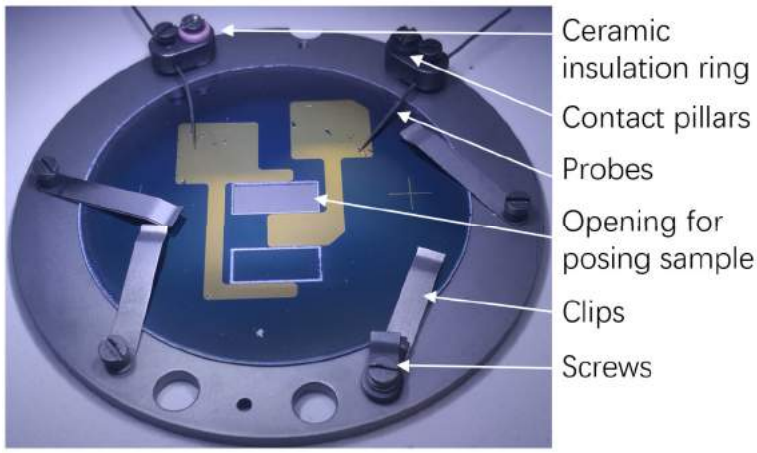


Figure 4.20 Picture of sample holder and holder wafer.

One thing need to be mentioned is that the holder wafer has an opening where the SOI sample can tightly fit. It is a 50mm diameter wafer with thickness of 400µm. The wafer is firstly cut into this dimension by laser cutting technique. Then the Plasma Enhanced Chemical Vapor Deposition is operated coating the silicon surface with 1µm thick silicon dioxide function as an isolation layer. Technique specifications are listed in

No.	Process	Technical Specifications	
9.1	PECVD	Recipe	1.45
		SiH4(5% ds N2) flow	150 sccm
		N2O flow	700 sccm
		HF power	20 W
		Pressure	1 Torr
		Temperature	300°C
		Deposition speed	696 Å/min
		Time	15min

Table 4.18. The database tells that for each 1nm SiO_2 can insulate 1V of electrical potential. Therefore, the insulation thickness is more than enough. Later 60nm Titanium and 400nm Gold are deposited on the holder wafer where are probe contact areas and bonding areas. Technique parameters are presented in

No.	Process	Material	Specifications	
4.2	Pre-deposition plasma cleaning	Argon	Clean duration	120 Seconds
			Power of plasma	200 eV
4.3	Evaporation	Titanium	Deposit thickness	60 nm
			Evaporation speed	0.1 nm/s
4.4	Lift-off	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C	2H to 3H
			Rinsing Acetone-IPA	5 min each
			Nitrogen dry blow	Until totally dry

Table 4.11 and

No.	Process	Material	Specifications	
5.3	Pre-deposition plasma cleaning	Argon	Clean duration	120 Seconds
			Power of plasma	200 eV
5.4	Evaporation	Gold	Deposit thickness	400 nm
			Evaporation speed	0.1 nm/s
5.5	Lift-off	PMMA EL13%-MMA8.5	UV exposure	15 mins (optional)
			Remover PG @ 65°C Or SVC @ 65°C	2H to 3H
			Rinsing Acetone-IPA	5 min each
			Nitrogen dry blow	Until totally dry

Table 4.14. A silicon mechanic mask is used during the metal evaporation process. The patterns on silicon stencil is made from 3 inches silicon wafer with laser cutting technique. The stencil has same diameter as the holder wafers and, by using the notch, alignment can be realized before introducing both wafer into the evaporation chamber.

No.	Process	Technical Specifications	
9.1	PECVD	Recipe	1.45
		SiH_4(5% ds N2) flow	150 sccm
		N_2O flow	700 sccm
		HF power	20 W
		Pressure	1 Torr
		Temperature	300°C

	Deposition speed	696 Å/min
	Time	15min

Table 4.18 Specification of Plasma Enhanced Chemical Vapor Deposition for 1µm SiO_2

According to the layout of MTC devices, the suspended membrane is isolated from this periphery SOI. The SOI wafer used for device fabrication is almost twice thicker than the sample holder wafer, so the holder wafer, SOI layer on the sample and the membrane collector are insulated between each other.

Same as alkali metal characterization, the MTC device is directly contacted to the surface of sample holder. In this condition, the previously calibration of heat process parameter and temperature checking table can be used during the MTC test in next section. This calibration shows the relationship between the temperature of inside radiator and the wafer temperature with direct contact on the sample holder. The ceramic radiator is located under the sample holder inside vacuum chamber presented in chapter 2.2.1. Therefore, with the datasheet of this calibration, the devices' temperature can be measured indirectly.

4.4.2 Tungsten tips and bonding

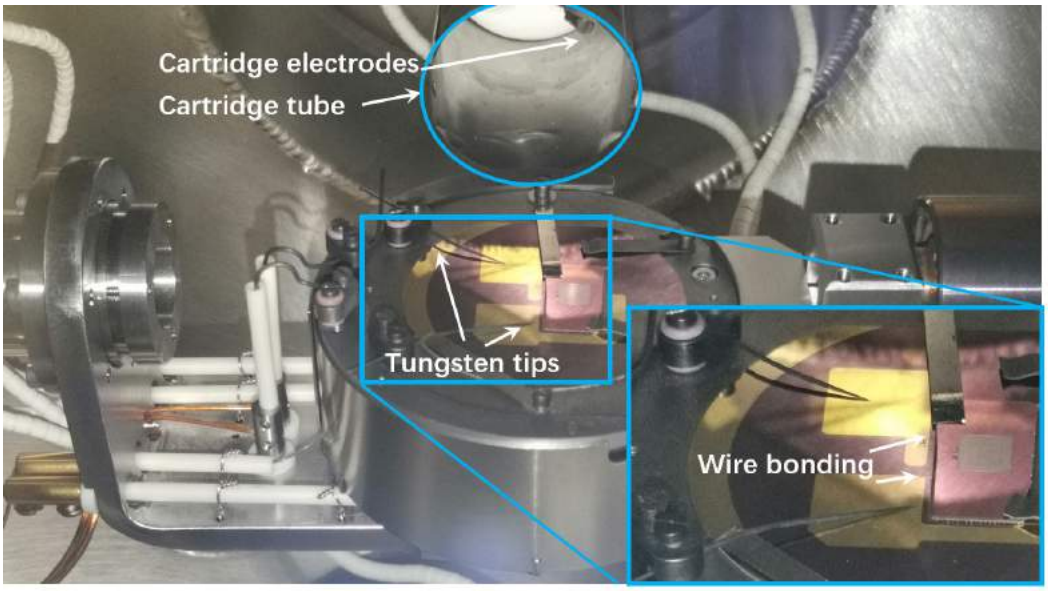


Figure 4.21 view of the sample/ holder wafer/sample holder in vacuum chamber

The SOI sample with suspended membrane is fit in to the sample holder wafer on the sample holder with clips and screws. Then, the electrodes on the SOI sample and gold pads on sample holder wafer are bonded by gold wire using wire-bonding technology. To make sure a good electrical contact between sample electrodes and gold pads, several bonding wires are bonded in parallel. After bonding process, tungsten tips are passed through holes in contact pillar and fixed with pressure between tip and gold pads. This will ensure good electrical connection. Figure *4.21* is the image of transport the sample holder from low vacuum chamber to high vacuum chamber. The sample holder is positioned in the horizontal slot on top of radiator. Once the position is fixed, two metal wires will contact pillars and set good electrical connection with accessibility. At the right side, mechanical arms hold the sample holder can transport it in to the position. The radiator module with horizontal slots in the middle of the image can move in three directions and rotate. By moving upwards can release the sample holder from mechanical arms. Then during the coating process, it will rotate backwards, facing the sample to the cartridge tube.

4.5 Characterization for micro thermionic convertor, analyses and perspectives

After wire bonding and setting the tungsten tips set on the gold contact pad, a simple I-V characterization is applied. The I-V curve present a 10 $\mathrm{K}\Omega$ resistivity after two steps etching suspension processes. The sample before etching, which is measured on probe station present a resistivity of about 1 $\mathrm{K}\Omega$. This is the contact resistance represent a metal short current between high-doped SOI layer and silicon substrate. However, with microscope inspection no metal pieces can be observed hanging from SOI layer into cavity. Profilometer shows similar results. One assumption is that the LPCVD deposited Silicon dioxide layer is not totally covered the exposed silicon substrate, while at the same position, the titanium layer has a thin film formed during the deposition which is not removed after lift-off process. This is the one assumption for large short circuit current between SOI and silicon subtract. Luckily, some electrical insulation problems can be solved by changing the electrode layer design or metal etching at suspected current leaking position. Reactive ions beam etching for example can remove unwanted metal on top or on sidewalls. However, one defect on SOI sidewall during LPCVD silicon dioxide protection layer deposition may result in short current between SOI and silicon substrate. At the defect of sidewall protection position, the opening on SOI will be bigger than normal due to XeF_2 etching and will lead to a silicon dioxide over etching.

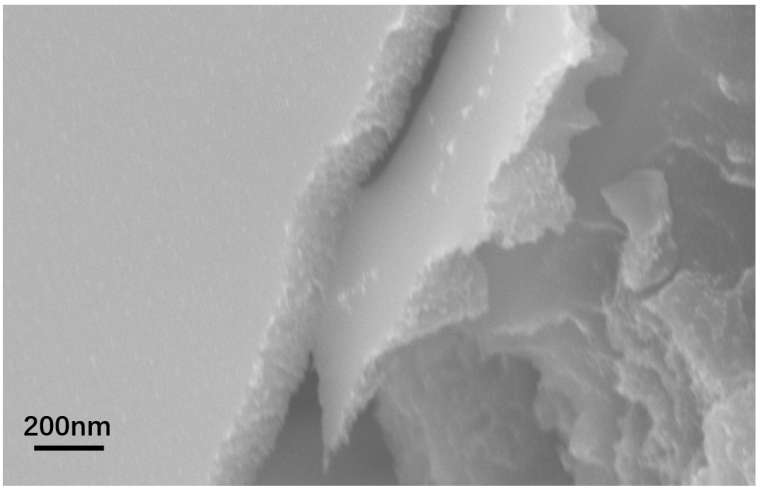


Figure 4.22 SEM images at unexpected larged SOI opening, the top SOI layer is touching the bottom silicon substrate when box layer(silicon dioxide) is totally removed by etching.

For a reference of good electrical isolation, a resistance greater than $10^7\ \Omega$ is the limit for thermionic current measurement. This is due to the magnitude of thermal current characterized in chapter 2 has a magnitude of $\mu\mathrm{A}/cm^2$, while the estimated active membrane surface is about $0.2cm^2$. If consider the massive thermal leakage compared to the ideal vacuum situation and unsatisfied temperature difference between electrodes, the minimum electrical isolation should provide a resistance of $10^9\ \Omega$ considerably. Due to the thermionic current calculated in chapter 3, thermionic convertor is working at the range of nano-ampere to pico-ampere with tens of temperature different at around 700K per Square millimeter. A current leakage of microampere presented on current sample is not acceptable. This leads to the enormous noise for measuring thermionic current. In another way, the surface designed for microelectronic process is too small for thermionic effect measurement and a larger membrane surface will introduce to a high risk of defects. For the same reason, on a big surface of millimeter scale or larger, an uneven vapor etching result will occur which makes unwanted pillars'

dimension distribution. This will lead to an unwanted thermal flow through sample wafer. One possible solution for this is to series connect multiples devices, which have smaller surface and are etched separately with dedicate control. This solution may ends into a structure that likes conventional thermal electric converter based on Seebeck effect.

4.6 Chapter summary

In this chapter presentation focuses on the practical part of approaches to fabricate parallel silicon electrodes. This is the basic structure for the unconventional thermal electric converter. The technical processes are proved feasible and a prototype device structure is build.

In the first part of contents of this chapter, the section 4.2 presents the layouts of initial sample and final sample. The initial sample has small single surface without consideration of thermal flow, which is intended for testing fabrication process. With many process parameters tuned and selected, the second and third sample with much large surface of about 25mm^2 have much less defects. Then, after the end of COMSOL thermal simulation, an unsatisfactory little temperature isolation capability for 400nm silicon dioxide lead to a much more challenge structure demand. The pillar size need to be less than several square micrometer and the pillar spacing should be three times larger than initially designed. The interval value of pillar presented in chapter 3 Figure *3.31* lead to the need of detailed adjustment of apertures and dedicated truing during two-step vapor etching. Moreover, the result of simulation illustrated the need of boarding thermal isolation for membrane. The evolution between first and final sample design represent the further understanding of the demand of thermionic converter device.

In chapter 4.3, technical detail of micro electrical nanofabrication processes are presented. All important technological processes and corresponding parameters have been listed in multiple tables. For some crucial problems, detailed characterization images of different methods are presented. Most of the problems are analyzed and solved with existing technology approaches. The device was fabricated on a SOI wafer with 200nm thick Silicon and a 400nm thick Box layer. The handler is 800µm silicon substrate. Facing the need for good electrical contact between top metal electrode and SOI layer, the silicon is doped with phosphorus. The n-type doping makes electrons from silicon easily transport to titanium and to the measurement circuit. All other efforts are mostly focused on minimizing thermal flow through device to create a better temperature difference between top layer and bottom substrate. Including membrane structure with pillar only support structure, untouched border and suspension electrode pass from membrane to bonding pads. These provide minimum temperature distribution on the membrane and increase the thermal resistance between membrane, surrounding wafer and silicon substrate.

The integration of device into vacuum chamber is detailed in section 4.4. Many possible solutions to increase thermal flow from surface of SOI are concept. However, hardly any approach is feasible considering the difficulty of modification inside ultra-high vacuum chamber. The integration step present is based on existing material and device feature of total vacuum chamber. With device direct contacting sample holder, the existing temperature calibration for alkali metal characterization remain same. The electrical contacts from electrodes on the sample to exterior of vacuum chamber are tested and proves to be reliable. However, with most of time spent on improving thermal isolation capabilities, the electrical isolation problem is unexpected appeared at the end of the fabrication. The initial diagnostic is a film of metal, probably titanium, formed at the unprotected sidewall position. From

other sample with membrane defects, an over etching of silicon dioxide layer may also lead to current leakage, which is observed by SEM.

To conclude this chapter, the main bullet points are: improvement between first and last design, the utilization of accuracy lithography and multiple etching techniques, realization of intended structure with suspending large surface membrane, final structure presented by look through image by SEM with pillar structures.

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Conclusions and Perspectives

Conclusions

All works carried out during this thesis contributed to the study and development of a thermionic electrical device. The work reported in this manuscript can be divided in to three parts. The alkali metal oxide characterization part is presented in chapter 2. In the chapter two possible coating materials features a low work function parameter is presented with different methods of characterization. The chapter 3 focuses on the structure parameter and thermal isolation evaluation for current design. The chapter 4 introduces the layout design and nano-technology fabrication process in detail. To summarize this report, the most important conclusions of each part of work and observations are listed in after:

1. By using Kelvin probe system, CPD measurement, photoemission measurements and thermal emission measurements reveal several important features of potassium oxide and cesium oxide as two potential material with low work function and high thermionic current density. Follow results demonstrate the effectiveness of alkali metal oxides for thermionic energy converter:

    a) Potassium oxide coating by vapor deposition technology gives work function of $1.73 \pm 0.16\text{eV}$, for photoemission experiments, and $1.75 \pm 0.28\text{eV}$, for thermionic emission experiments. The maximum current density was $3.6\ \mu\text{A}/cm^2$ at 799K.

    b) Cesium oxide coating by vapor deposition technology gives $\emptyset_{sample} = 1.66 \pm 0.27\ eV$, for photoemission experiments, and $\emptyset_{sample} = 1.72 \pm 0.2\ eV$, for thermionic emission experiments. The highest achieved current density for these samples was $12.8\ \mu\text{A}/cm^2$ at $698\ \text{K}$.

    c) Cesium oxide coating by ALD technology gives $\emptyset_{sample} = 0.98 \pm 0.02\ eV$. We also confirmed the structure of Cesium oxide film after breaking the ultrahigh vacuum and reloading in to SEM chamber. The SEM image of Cesium oxide film is further confirmed by EDX signal.

2. Theoretical discussion about all influential factors and FEM thermal conduction and emission simulation are carried out. The previously measured cesium oxide work function is confirmed with simulation model. This proves that both the measurement results and simulation model are valid. Later, the FEM results conclude that a gap dimension ranging from 200nm to 10µm will lead to best efficiency for an ideal device without conductive thermal leakage. For existing SOI-200-400nm wafer with ideal fabrication result according to the design, a temperature difference of 50 degree is the maximum. For a hotter emitter and 2µm box layer of silicon oxide, a temperature difference of 100 degree can be reached with less fabrication difficulty. Better design for the SOI opening or phononic pattern can also help in increasing temperature difference between emitter and collector.

3. The design, fabrication, integration and characterization of a thermionic device is presented in the last part. The main bullet points are:

    a) Improvement between first and last design which is a unique way to build a parallel thermal electric electrode by microelectronic process

b) The utilization of accuracy lithography and multiple etching techniques, realization of intended structure with suspending large surface membrane, final structure presented by look through image by SEM with pillar structures. By the end of device fabrication process, in each device the parallel electrodes structure is fabricated with a big membrane surface of $25mm^2$ and little defects. The pillar dimension is limited to $1\sim3\mu m^2$ by two step vapor etching, which maximum limit conductive thermal leakage between emitter and collector in the thermionic device.

Perspectives

Short term:

1. Device problem shooting: Solve current leakage problem by improving layout design or removing possible short circuit metal parts by reactive ions beam etching. Improving process stability reproduce the device with less or no defects. These defects are possible lead to contact between SOI and silicon substrate result in bad thermal and electrical isolation, both of which are crucial to the unconventional thermionic converter.

2. Improving even vapor etching method on larger sample. Find a dedicated control method of XeF_2 etching range by slowing down the etching speed. Simple solutions like making and using a silicon etching support or change etching parameter. Both can decrease etching speed and increase etching cycles/time, which may help in improving even etching and precise etching. Still some sophisticated solutions will have better effects. A better control of etching chamber pressure by adjustable valve can have more stable chamber pressure. A pump with more stable vacuum capacity will also help in precise etching and better repetitive devices.

3. Repeat I-V characterization after alkali metal deposition at high temperature in ultra-high vacuum chamber. With the help of FIB, SEM and EDX the deposition quality and film distribution analyses are needed. With FIB technology, a section view of membrane and cavities can be observed while the membrane remain partly undamaged. Using previously measured work function value to estimate the thermal current. Comparing it with results thermionic power harvested from the device.

Medium to Long term:

1. Material research: Investigation on more alkali materials and searching for lower work function values and better thermal stability. Try to find a molecular structure of Cesium oxide with low work function and can sustain higher temperature. This is a task demand for more chemical knowledge and experiment experience.

2. Increase thermal isolation capability to create better temperature difference. Improving membrane thermal diffusion capability. Furthermore, despite the well developed fabrication techniques and the delicate device structure represented, we wants to try some other strategies. For example, use thick silicon oxide growth and deep etching technique to build electrodes of MTC separately on thin silicon wafers. Then, align them and use wafer-bonding technique to connect electrodes and build the device with robust mechanic structure. This may be a lower cost and better repeatability strategies.

3. Propose a method or structure feature to connect multiple device on a series association. One literature has demonstrated by increasing number of thermoelectric modules does

not impose a weak electrode output work. Therefore, the combination of multiple working device will decreasing the demand for a coating material with low work function. What's more, the thermoelectric module stack will take better usage of thermal gradient and gain better power output in per unit surface.