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Par
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Design and characterization of power detectors in 55-nm BiCMOS technology for 5G and THz applications

Conception et caractérisation de détecteurs de puissance en technologie BiCMOS 55 nm pour les applications 5G et THz

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General introduction

The mobile communication system brings real-time communicating to people in a mobile state without physical transmission line. It has been continuously developing since the cellular communication concept was proposed by Bell Labs in 1970s [1]-[3].
The first generation of mobile communication system (1G) was commercially launched in 1980s. This system adopted analog electronics technology and can only provide low quality voice service, very small system capacity and limited services [4].
In early 1990's, the second generation mobile systems (2G) were rolled out commercially as digital communication systems. The system capacity and quality were significantly improved as compared to (1G) because of its digital nature. Low data rate services (384 Kb/s) were also added in (2G) systems along with voice services [5].
In the 21st century, the third generation mobile systems (3G) were standardized under the coordination of International Telecommunication Union (ITU) [6]. Based on the Code Division Multiplexing Access (CDMA) technology, (3G) systems provided higher data rates, larger bandwidth, and higher system capacity.
Long Term Evolution (LTE) proposed by Third Generation Partnership Project (3GPP) was the initial taste of (4G) networks around 2004 [7]. With the introduction of the orthogonal frequency division multiple access OFDMA and MIMO (multiple-input and multiple-output), (4G) networks provide much higher data rates than (3G) [8], [9].
(5G) is the actual generation of mobile communication technologies. Its initial launch was in 2012 [10], and commercially introduced in 2020. The main (5G) aims are to provide higher data rates, lower latency, seamless coverage, lower power consumption and higher reliable communications [11]. So many researches have been also done to enhance the machine-to-machine (M2M) and Internet of Things (IoT) technologies. These technologies are operated using the (5G) systems. Several ranges of Millimeter-wave (mmW) frequencies are utilized in (5G) systems for back-haul (up to 100 GHz), this allows to provide higher data rate (of at least 1 Gb/s) and lower latency as compared to (4G) [12], however, higher power consumption is required. In addition, the huge number of IoT sensors that will be installed makes it difficult to sustain all batteries [13],[14].

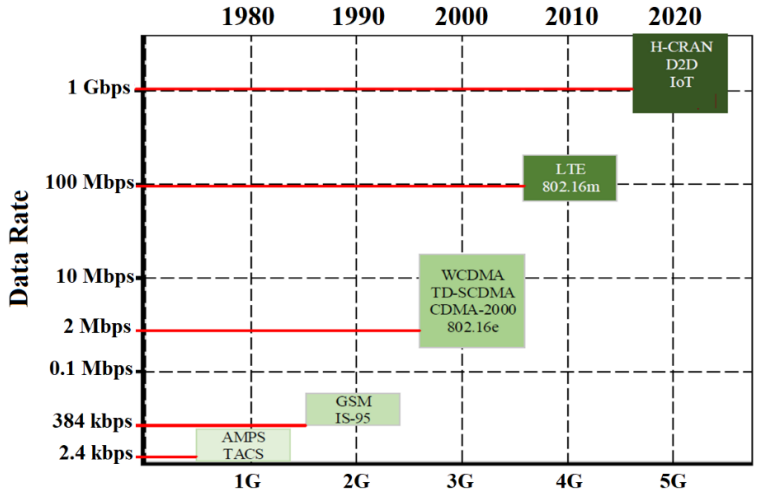


Figure 1 Journey of cellular networks [15].

Moreover working at high frequencies makes the thermal effect an issue requiring more power consumption. For those reasons, the battery life is crucial and considered as one of the biggest hurdles in the development of IoT devices [16]. In this context, several methods are proposed for reducing power consumption [17]. Using envelope tracking technique (ET) could be a promising solution to increase the efficiency of (5G) and IoT devices [18]. As a part of envelope tracking circuit, several power detector topologies (zero bias detectors) are proposed and studied in this thesis. Another detector topology (tunable detector) is also proposed in this thesis, this can be utilized in different 5G applications. These detectors are designed using the SiGe 55-nm BiCMOS technology from STMicroelectronics, in the frequency band (35 – 55) GHz allowing to cover several 5G bands [19].

(6G) is the next generation of mobile communication system which will be commercially launched in 2030. This generation will be able to use higher frequencies than (5G) systems (THz frequencies), providing higher capacity and much lower latency (1 µs latency of communications) [20].

Nowadays, the use of THz waves became more popular. This is because of their interesting properties, and also, the new sophisticated technologies which allow to deal with such high frequencies. THz waves are mainly utilized in high resolution imagining for medical and security applications [21], and also in spectroscopy providing information that other waves cannot [22].

In this thesis, power detectors (using the same technology) dedicated for higher frequency applications (in sub-THz and THz) are also studied. The design and characterization of those detectors have been done for two frequency ranges. The first range is (140-220) GHz in G-band. This detector can be used in integrated power detection for power measurement instrumentations. The second range is (0.45-0.6) THz, where radar and THz imaging systems are forecasted as the main applications.

Very high performances can be obtained when the III-V technologies are utilized to design THz detectors [23]. However, they have high cost and cannot be integrated with the digital (processing) parts on the same silicon chip. The detectors presented in the thesis (based on silicon technology) exhibit very good performances and allow the integration with the digital parts. Therefore, these detectors can be interesting for several reasons:

- Because of the integration capability, these detectors help increasing the compactness and the overall efficiency of power measurement systems at such high frequencies.
- They have low cost.
- They are not available in the market.

The thesis is organized as the following:

The first chapter presents the need of power measurements by explaining the most common applications with some examples at different frequency ranges. The principles of the heat and diode based sensors are also presented, showing the pros and cons for each type.

The second chapter studies the basic diagram of diode based detectors by explaining the function of each block. The detector parameters are discussed in detail, showing their importance depending on the applications, and their effects on each other.

The third chapter presents the extraction of the small signal model of the PN diode (which is under development). Then, the design of tunable detectors (using the extracted model) is presented. The model of the diode is also extracted for several temperatures in order to help to design temperature compensated detector (based on this diode).

The fourth chapter focuses on the design and characterization of zero bias detector, based on MOSFET (NMOS) transistors. Several detector topologies are designed and characterized, dedicated for 5G, IoT and THz applications.

It is worth to mention that, part of this thesis (detectors for 5G applications) has been done in the frame of European project (EURAMET - 16ENG06 ADVENT), which is supported by the European Metrology Program for Innovation and Research (EMPIR). The aim is to calibrate our detectors (at 42 GHz) using a heat based detector (as a reference), which is designed by Laboratoire national de métrologie et d'essais (LNE).

Chapter 1
Power Measurement Applications & Power Sensors

1.1 A brief history of RF and microwave power measurement

From the beginning of the RF and microwave systems, it was necessary to determine the power level in different systems plans (input power, output power, power level in-between the stages, etc.). The power measurement principles were quite primitive compared to nowadays technologies. In the late 1930s, the klystron microwave power tube was used in the early experimental stages of klystron cavity to give a gross indication of power level [24]. Whereas the diode-based detection of the day was not capable to work at such microwave frequencies as the klystron tube.

For the high power systems, set of terminals were being arranged to absorb the power, then, the built-up heat versus time was being measured. With the launch of the crystal technology in the period of the world war II, new types of detectors were initiated based on this technology. Consequently, the detectors became faster, more rugged and performed at higher frequencies. One of the earliest sensing element built in crystal technology had a positive temperature coefficient (PTC); this type of element uses the power substitution methods to produce the readout voltage. The thermistors which have negative temperature coefficient (NTC) were much more rugged, for this reason, they became more dominant compared to PTC elements. The calorimeters were also being used with the thermistors in the early measurements. In the 1960's, the 434A power meter was an oil-flow calorimeter, where the maximum measurable power using this meter was about 10 watt [25]. On the other hand, water flow calorimeters were being used for medium and high power levels.

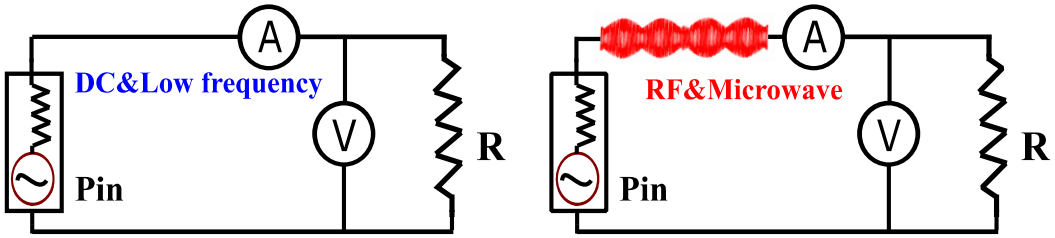
Finally, it is worth to mention that some of the early power sensors are still used nowadays (such as thermistors, calorimeters, diodes …). However, more decent technologies and complex instruments are employed to improve the detection performances.

1.2 Why measuring power ?

Measuring the voltage and current in DC and low frequency systems can be very accurate and simple as in figure 1.1 (a). For a resistive load, the power can be calculated

using the effective current and voltage drop across the load, as in equation 1.1:

$$P = V_{rms}.I_{rms} = \frac{V_{rms}^{\ 2}}{R} = I_{rms}^{\ 2}.R \qquad (1.1)$$



(a) (b)

Figure 1.1 (a) Power measurement at dc and low frequencies, (b) variation of the voltage along transmission line at RF & microwave frequencies.

However, for higher frequencies such as RF and microwave, the propagation wavelength becomes smaller, and so comparable to the dimensions of transmission lines. Because of that, the voltage (and current) varies along transmission lines as in figure 1.1 (b). In addition, signal reflections, standing waves, and impedance mismatch become very significant error sources.

In the following, we can mention two main reasons for which the power measurement is performed (instead of voltage or current) at high frequencies:

1) The power delivered to the load (R) is constant along the lossless transmission line. Therefore, the measured power does not depend on the meter position.
2) Performing voltage or current measurement in waveguide is more complicated.

1.3 Power measurements applications

Measuring the power in most of RF and microwave systems is necessary and sometimes even crucial. There are thousands of unique applications where power measurement is required and helpful. RF power detector is considered as the key element to establish the power measurement. Some of the common applications are mentioned and explained in the following paragraphs.

1.3.1 Proof of design

The designers often need to determine power levels in different system plans, and so verify the validity of their circuits. Amplifiers and couplers circuits are common examples where the input and output power have to be measured. These measurements are useful to determine the power gain of amplifiers, coupling factor and losses in couplers.

1.3.2 Component protection

Two possible effects can be produced when high instantaneous (peak) or steady stat power is applied on a device:

1) Overstressing the device, which causes temporal or permanent modification in their physical characteristics.
2) Causing dielectric breakdown, over-heating and damaging the device.

Even at power levels well below the damage threshold, excessive power can change the performance of the system. This usually happens when the input power level excess the compression point producing a distortion in the output signal. Therefore, power levels are usually measured and controlled in order to keep the systems in proper operating zone and safe conditions.

1.3.3 Power regulation

Power regulation is considered as one of the most important issues to be fulfilled in the RF and microwave systems. For example, in the communication and wireless industries, there are usually a number of regulatory specifications that must be met by any transmitting device. The most common regulatory requirement is to specify the maximum power which may be radiated by the antenna.

Regulated amplifier for radars is another example [26], where accurate power control is required to meet system specifications under operating conditions (temperature and supply voltage variation). The power control loop works as the following:

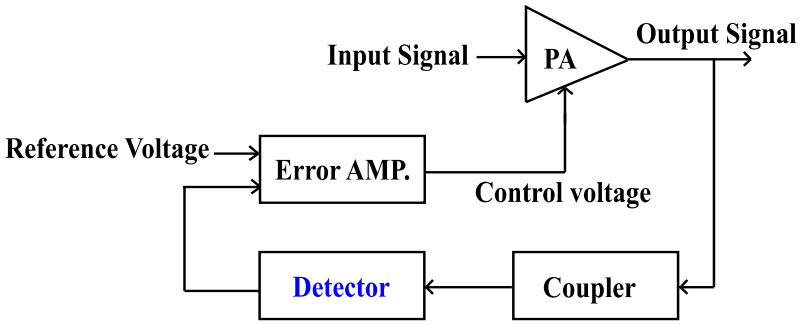


Figure 1.2 Power amplifier control loop for radar system.

The detector read the output power of the PA through the coupler as shown in figure 1.2. The reference voltage (which is set by the controller) is compared to the detector output. Then, the error amplifier reduces the error value in the output signal by changing the control voltage, and so the power gain. In this application, measurement accuracy is the most important parameter that the detector has to fulfill. It is worth to mention that the control loop technique does not depend on frequency, hence it can be used at higher frequencies (at millimeter waves for 5G transmitters).

1.3.4 Measuring or improving of system efficiency

Efficiency is a measure of how well a device (or system) converts one energy source to another. In microwave engineering, we are interested in converting DC to RF power or the opposite.

With the rapid development of wireless communication systems, the demand of higher data rate and larger frequency bandwidth is more and more increased. This can only be achieved by consuming more energy [27]. Therefore, increasing the efficiency of the devices is necessary.

In mobile radio networks, the amplifiers in both cell phones and base stations consume the highest amount of energy comparing to other system parts. (50-80) % of the consumed power in the base station is drained in power amplifier [28]. Moreover, these amplifiers suffer from low efficiencies. Hence, increasing their efficiencies will significantly increase the overall system efficiency and the battery life.

In this thesis, the envelope tracking technique (ET) is forecasted as the application of power detector, where the aim is to improve the efficiency of amplifiers in 5G and IoT systems.

1.3.4.1 Envelope tracking technique (ET)

Traditionally, power amplifiers (PAs) are biased so that there is sufficient DC power at the transistor to supply for peak output RF power. However, when the output level is smaller than the peak value, the extra DC power must be dissipated in the transistor as a heat, since it is not transferred to the RF load. The higher the value of peak to average power ratio (PAPR), the higher is power dissipated in the transistors, thus, lower efficiency is obtained. Figure 1.3 (a) shows the variation of power added efficiency (PAE) with the input power for an amplifier biased by a fixed power supply.

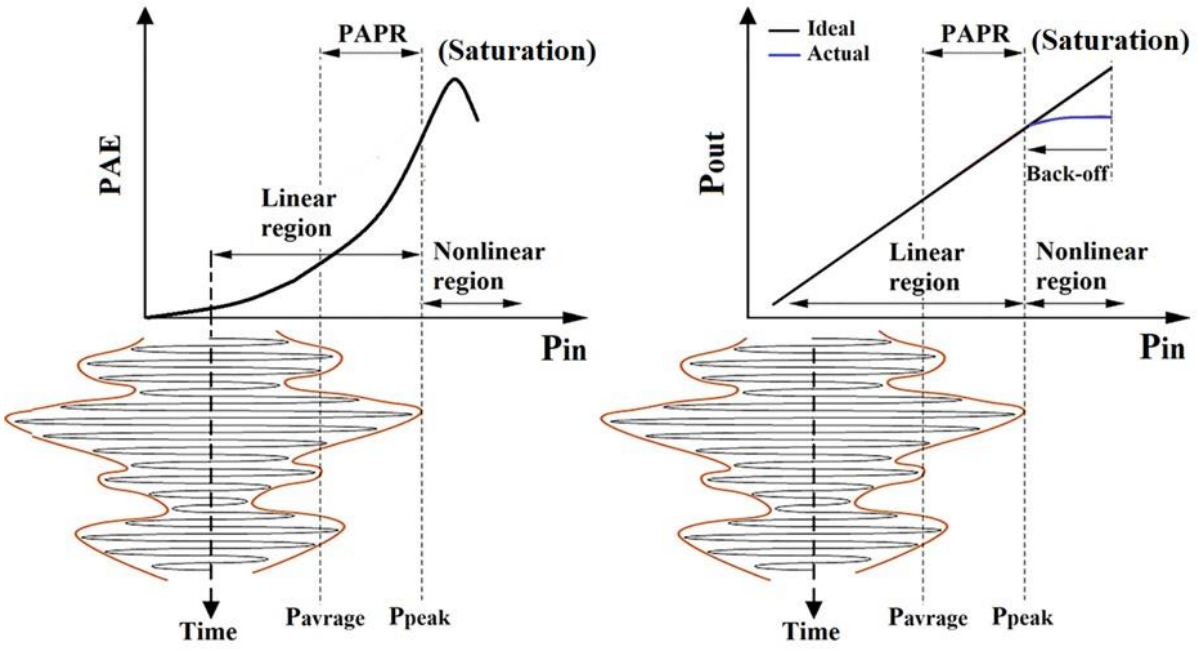


Figure 1.3 (a) The power added efficiency (PAE) versus input power for an amplifier using fixed power supply, (b) the output power versus input power for an amplifier [29] .

As it can be seen, the maximum efficiency is only obtained near the saturation region. Biasing the amplifier by a fixed power supply is usually inefficient, this is because most

of the modern modulated signals (such as OFDM modulation) have high PAPR values [30].

Modulating the power supply level can be a solution to improve the efficiency of an amplifier. This is done by decreasing the supply level when the output level is smaller than the peak value, thus decreasing the dissipated power in the transistors. Figure 1.4 shows the load lines corresponding to two signal input levels when modulated power supply is used. Instead of maintaining the same biasing point for small output level, ET technique decreases the supply voltage ($V_{CE\,High}$ to $V_{CE\,Low}$). Hence, the biasing point is changed allowing for enough load line swing, while decreasing the DC power. It is worth to mention that the gain does not change with the supply voltage, and the last is adjusted to ensure that no extra power is dissipated in the transistor. This technique is used to increase the power efficiency in mmW power amplifier [31].

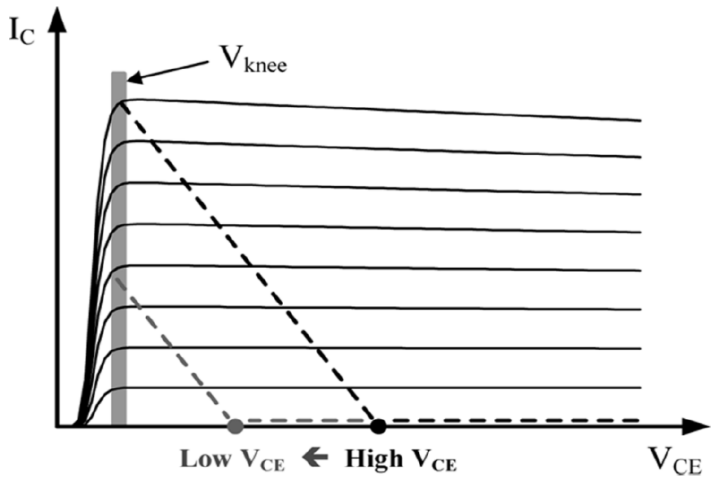


Figure 1.4 Load lines of class-B biased GaAs HBT PA for modulated power supply [32].

Figure 1.5 shows the PAE curves for different supply levels (which follow the variation of the input signal), where the peak efficiency values are obtained for all signal levels (even at low power). In other words, envelope tracking technique makes the efficiency follow its peak values of the swept supply voltage, thus, significant improvement is obtained.

Improving the linearity of amplifiers is another important benefit of using ET technique,

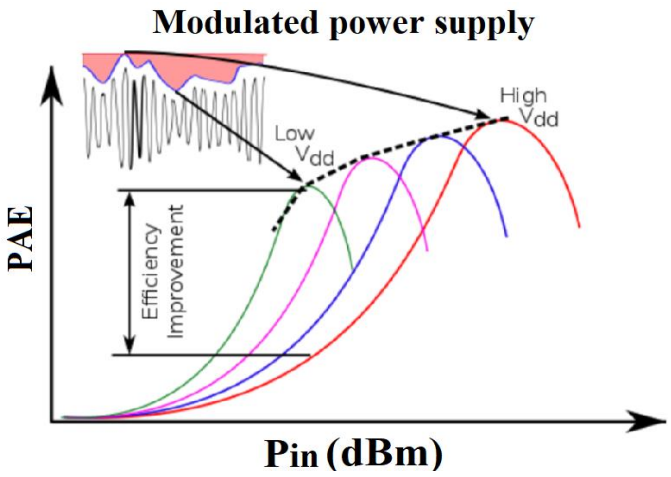


Figure 1.5 The PAE curves for different supply levels (when ET is used).

since it allows following the input signal levels to keep the operating point in the linear region.

Figure 1.6 shows the simple version of envelop tracking diagram. It consists of several stages which are briefly explained in the following:

- **RF coupler**: This coupler is located at the input RF signal. Its main function is to divide the input RF power in two parts in order to feed the envelop detector and the amplifier. The losses and coupling factor of the coupler have to be designed in order to keep the input power - of the detector and amplifier - higher than their noise floors and lower than their compression points. The coupler also has to be matched at the input in order to absorb the maximum of the input RF power.

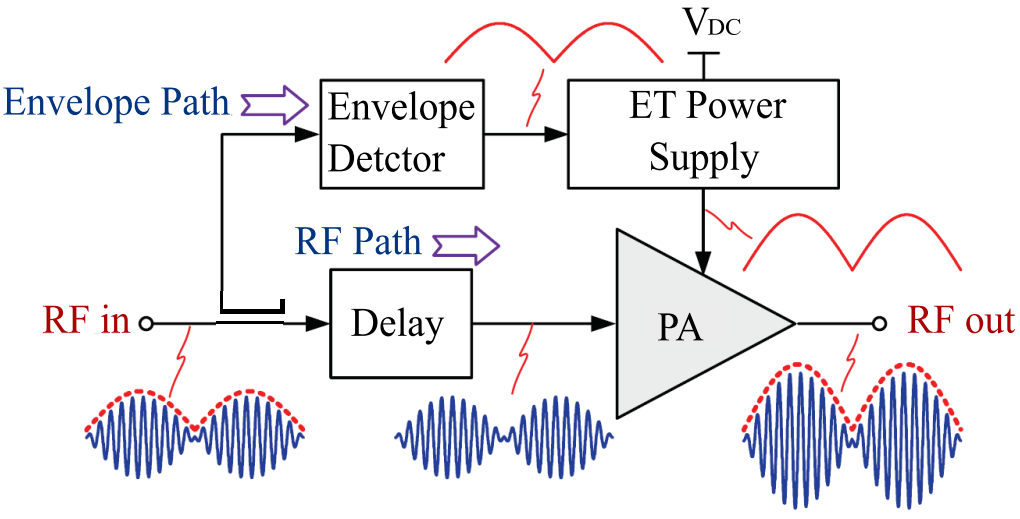


Figure 1.6 Envelope tracking block diagram [33].

- **Envelope detector:** Its function is to extract the envelope (bass band) signal. This signal drives the ET power supply (modulated power supply). The detector has to fulfill two critical parameters: (1) Fast response is required in order to track the envelope variation. For this reason, the heat based detectors are not useful in this application. (2) The power consumption has to be minimum possible in order to take the full benefit of the ET technology.

  The diode based detector dedicated to ET technique is explained in detail in this thesis.
- **ET power supply:** It is a modulated power supply. The output supply level depends on the input control signal (coming from the envelope detector). Hence, it has the same shape as the envelope of RF signal. Some requirements have to be met in the design of ET power supply [34]:
  1) The output bandwidth has to be sufficiently large (typically around two to three times of the envelope signal bandwidth), so it can accurately follow the envelope signal.
  2) The ET power supply must be highly efficient in order to take the full benefit of the ET technology.
  3) Using switch mode power supply (SMPS) offers high efficiency level, however it generates high frequency noise which causes severe issues related to power integrity (PI) and radio frequency interference (RFI) [35]. The larger envelope signal bandwidth, the higher noise level is produced. Therefore, innovative SMPS design is required to ensure low noise level.
  4) Usually, decoupling capacitor is added at the output of power supply in order to eliminate the ripples and noise level. In the case of ET power supply, decoupling capacitor cannot be added since the supply power is not DC (has the shape of RF envelope). This means that ET supply must have very low output impedance to absorb any noise that might appear.
- **Delay:** This stage makes a delay in the RF input signal which is fed to the power amplifier. This compensates the response time of the detector and the ET power supply.

1.3.5 THz power detection

The THz frequencies spectrum is defined in the range 0.1 to 10 THz [36], these waves are located in the area between electronics and photonics fields in the electromagnetic spectrum. THz radiation is characterized by the following unique features:

- It can penetrate through a wide variety of dielectric materials such as fabric, paper, plastic, leather and wood.
- It is non-ionizing and has minimal effects on the human body.
- It is significantly absorbed by water at specific frequencies.
- It is highly reflected by metals.

In the context of THz power detection, terahertz imaging is utilized in many applications, some of them are mentioned in the following.

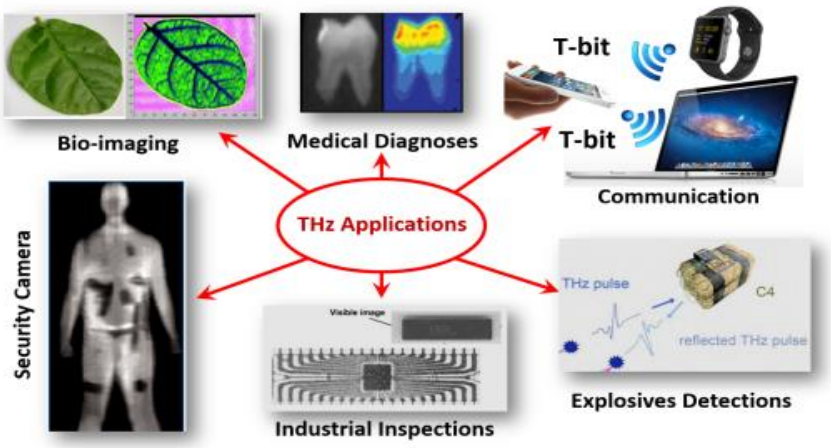


Figure 1.7 Some of THz applications [37].

As previously described, terahertz radiation is sensitive to water and has very low photon energy, those properties make THz imaging suitable for many biomedical applications [21]. The non-ionizing character of THz radiation makes it less harmful to living tissue than X-ray. This is especially interesting for medical applications such as cancer diagnosis [38]. It has been proved that terahertz imaging can replace other diagnostic technologies for imaging the structure of teeth [39]. High water absorption of THz radiation makes it a very useful tool for plant scientists for the inspection of the water in vegetative tissues [40].

In the field of defense and security, it has been shown that THz spectroscopy can be used for the detection of explosive materials, and concealed weapons [22]. THz imaging can also be an alternative to X-ray and non-imaging millimeter-wave systems [41].

In this thesis, integrated THz power detectors are designed using the SiGe 55-nm BiCMOS technology from STMicroelectronics in the frequency ranges (140 – 220) GHz, and (450 – 600) GHz.

Concerning the RF front ends devices, III-V technologies allow better performance comparing to silicon technologies. However, using the low cost BiCMOS technology to build our detectors allows the integration with the digital parts on the same chip. This helps reducing the losses and improving the overall efficiency.

Power detections at such high frequencies require high sensitivity value because of two main issues:

- The losses (in the probes, wave transitions and transmission lines) are relatively high. For example, the insertion loss of 50 Ω microstrip lines in BiCMOS technology from STMicroelectronics is about (3.5 dB/mm) at 500GHz (simulated performance).
- The electromagnetic waves are significantly attenuated by the medium (9 dB/km at 300 GHz for the air, depending of the relative humidity (RH)), thus the received power levels (to be detected) are relatively low.

1.4 Power sensors

There are several technologies available for RF power measurement. One of those technologies uses direct sensing elements, this includes:

- Thermal sensing elements (such as thermistors) to measure the heat effect of RF power.
- Nonlinear devices (such as diodes and transistors) which rectify the RF signal.

Another technology uses indirect methods to quantify the RF power, this includes:

- Tuner receiver which receives the RF signal, then its amplitude component is measured.

- RF sampling, where the RF signal is treated as a baseband signal and directly digitized.

The power sensor has to be chosen following the applications. In the following paragraphs, different types of power measurement are briefly presented, then, different types of direct sensing elements are explained.

1.4.1 Power definition

When voltage signal v(t) is applied on a load Z, current signal i(t) will pass through, and vice versa. The power dissipated (absorbed) in the load is defined in the following equation:

$$P = V_{rms}.I_{rms}.\cos(\phi) \quad (1.2)$$

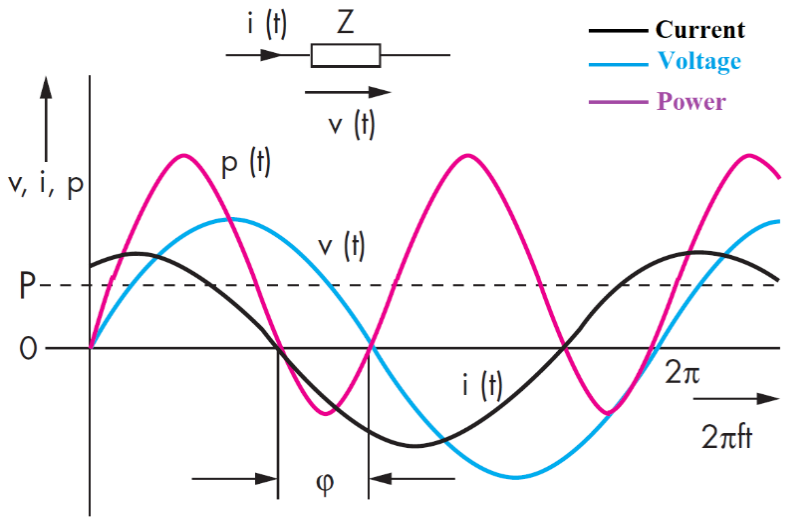


Figure 1.8 The voltage, current and power absorbed in load Z.

Where V_{rms} and I_{rms} are the RMS values of the voltage and current signals over the load, φ represents the phase shift between the voltage and current signals. It is worth to mention that φ is equal to zero for pure resistive load.

The power *P* represented in equation 1.2 is commonly used in the RF and Microwave engineering, it is referred as the true or active power. This power quantity is what would be indicated by a thermal power meter.

1.4.2 Types of power measurement

Figure 1.8 shows the power curve when a simple sinusoidal signal is applied. However, the waveforms are more complex in real applications (depending on the modulation type).

When modulated signals are considered, several definitions of power quantities are more appropriate [42]. In the following, each power quantity is briefly explained:

- The instantaneous power P(t): It represents the actual power of the signal (carrier) at any given time. The detection of this power type is considered as a reproduction of the waveform. A detector with very fast response is required in order to capture the fast variation of the signal carrier.
- The envelope power $P_e(t)$: It represents the actual power of the envelope signal at any given time. The detection of this power type is considered as a reproduction of the envelope signal (baseband signal). A detector with fast response is required in order to capture the variation of the envelope signal.
- The average power P_{avg}: It represents the average value of the envelope power signal $P_e(t)$ over a specified period of time (usually the modulation period). The P_{avg} value is what would be indicated by thermal power meters, therefore, this type of detection is usually referred as true-RMS detector. In this case, the detector does not need to have fast response, since it averages out the power of a waveform for a certain time period.
- The peak envelope power PEP: It represents the highest value of the envelope power signal $P_e(t)$. PEP is an important parameter for specifying transmitters (as explained in 1.3.3). A detector with a fast response is required in order to follow the peaks of the envelope signal.

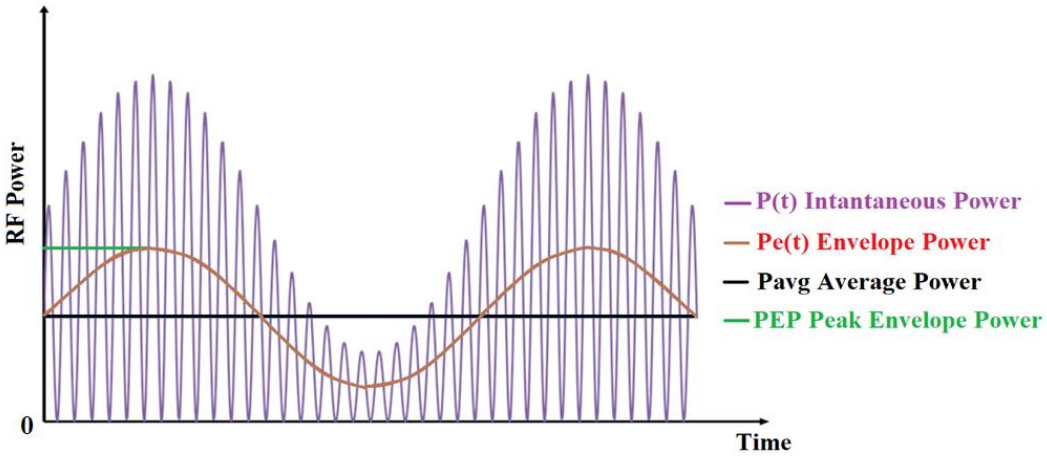


Figure 1.9 Modulated signal with the illustration of several power types.

- The pulse power P_{pulse}: Measuring a signal with high power levels can damage the power sensor. One possible solution is to apply several bursts of the signal (pulsed signal) instead of continuous mode, this can avoid burning out the sensor. Radar system is another application where pulsed signal measurement is required. Such type of measurement can be done by dividing the average power P_{avg} over the duty cycle of the pulses (D). The pulse power averages out all aberrations that can occur due to the pulse modulation, such as overshooting and ringing (as shown in figure 1.10). For this reason, it is called pulse power and not peak or peak pulse power.

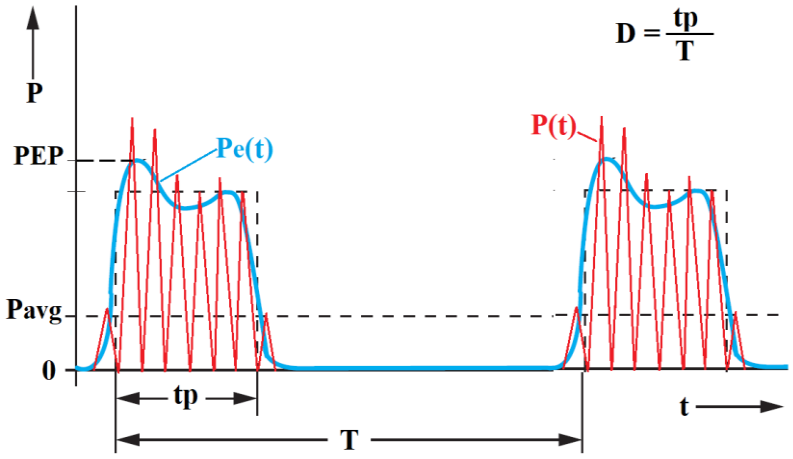


Figure 1.10 Pulsed signal with the illustration of several power types.

As a conclusion, the heat based sensors can only measure the average power P_{avg} since no fast response is required.

1.4.3 Some backgrounds of power detectors

The RF signal power can be directly measured using power sensors and meters as shown in figure 1.11, where the power sensors are considered as the key elements. The function of the sensors is to convert the incoming high frequency power (i.e. RF, microwave, millimeter-wave or even higher) to a DC or low frequency signal. The meters measure (read) the output signal of the sensor, and then, display the result.

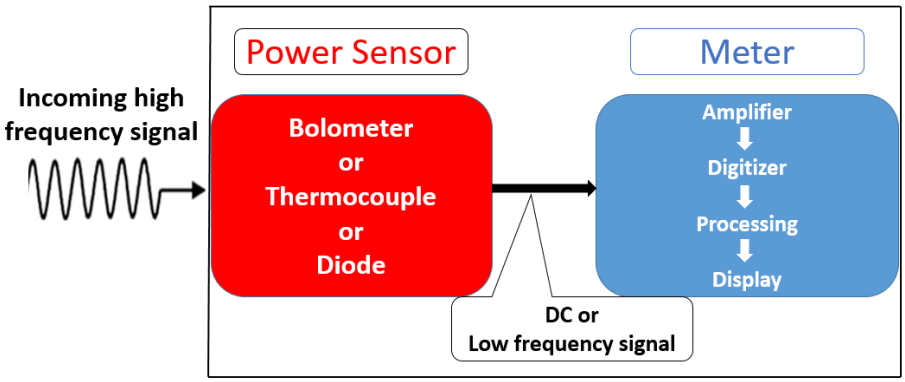


Figure 1.11 Basic block diagram of power detectors.

Two main types available of power sensors:

1) Heat based sensors (bolometers and thermocouples).
2) Diodes (or transistors).

In the following paragraphs, we present the principles of the bolometer, thermocouple, and diode detectors. Since the diode detector is the core of the thesis, it will be explained in detail in the next chapter.

1.4.4 Heat based power detectors

As the name suggests, this type of detectors dissipates the incoming RF power into heat, the resulting temperature rise is somehow measured in order to calculate the RF power.

The heat based RF power sensors are able to measure the true average power as a heat over a period of time, thus, they measure the RF energy which is independent of the waveform. In many cases, this is considered as an advantage comparing to other

detection techniques, where the PAPR can affect the results [43]. These detectors are mainly used as reference power standards, since they are considered to have very low uncertainty in their measurements [24].

Considering the response time, the heat based sensors are not suitable for measuring fast variation or instantaneous signal values due to their slow responses. Those types of measurement are usually done using diode based detectors. The heat based detectors mainly include two types of technologies: bolometers and thermocouples.

1.4.4.1 Bolometers

Bolometers are RF power sensors based on thermistors. These elements have negative temperature coefficient of resistance (NTC), i.e. their resistance values decrease with temperatures [44] (figure 1.12). The thermistor heats up as a result of dissipating RF power, as well as the effect of ambient temperature.

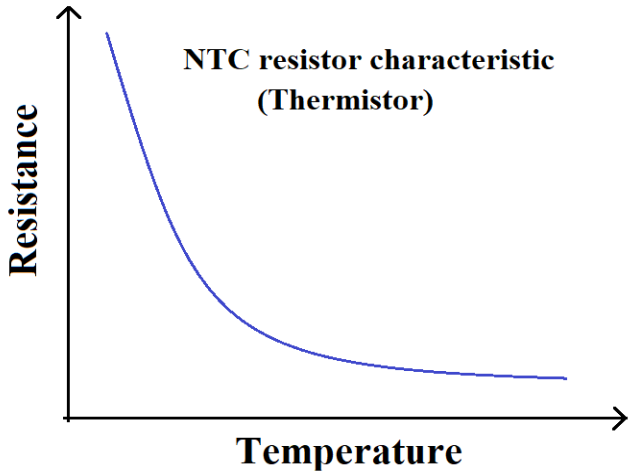


Figure 1.12 Thermistor characteristic with temperature [45].

This type of sensors was one of the first utilized to measure the RF power. In most of modern applications, bolometers are replaced by thermocouple and diode detectors due to their larger dynamic ranges and higher sensitivities.

Nowadays, thermistors are still used as reference power standards in most of national standards, this is because of two main reasons:

1) They are the only present-day sensors which allow DC power substitution measurement techniques. This type of measurement can be done with very low uncertainty [46].
2) There are no weighting errors when RF power is converted into heat.

Thermistor elements can be mounted in coaxial cables or waveguide structures, thus, they can be fed by microwave signals (or even higher frequencies) using the common transmission lines. The sensor circuit has to be designed so that it absorbs the maximum possible of incident power. This can be done by fulfilling the following conditions:

- The impedance of the sensor circuit has to match the impedance of mounting structure.
- The losses in sensor circuits have to be minimum possible. Therefore, low resistivity and dielectric losses within the mounting structure are required. This is important because only the power dissipated in the thermistor is indicated in the power meter.
- The sensor has to be thermally isolated from the environment, hence, it is far less affected by the ambient temperature.

Operating principles:

The most common implementation place of the thermistor is in auto-balancing Wheatstone bridge (as in figure 1.13) using the DC substitution technique [47].
In this case, the thermistor is considered as a temperature measurement device and RF load at the same time. The output of the amplifier is used as a power source to bias the bridge. Because the deferential input voltage of the amplifier is about zero, certain amount of power will be drawn bringing the bridge to the balance stat (i.e. producing *RT* is equal to the other resistors *R)*.
We call the power P_{OFF} is the total power drawn by the balanced bridge (P_{tot}) before applying the RF signal. When the input RF power is injected, the thermistor absorbs this power producing additional heat. Hence, the (*RT*) value tends to be lower, and the bridge is no more balanced. Because of the feedback power source configuration, the power drawn (P_{tot}) is decreased bringing back the bridge to the balance state. We call the later power P_{ON}.

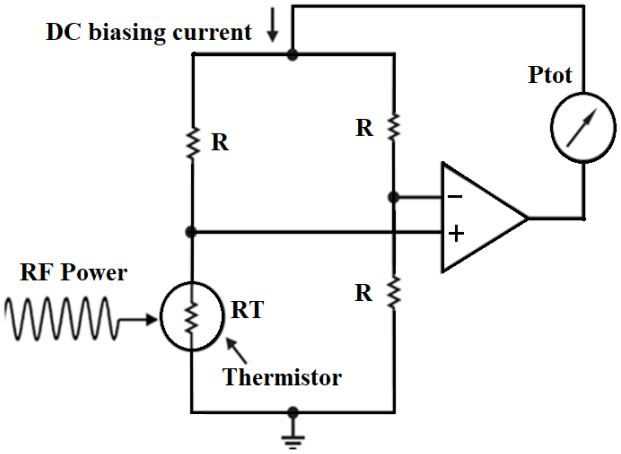


Figure 1.13 Thermistor as RF power detector in Wheatstone bridge configuration [47].

The total power dissipated in the thermistor is due to the incoming RF power and the DC bias. As a result, the incoming RF power can be extracted using the difference ($P_{OFF} - P_{ON}$). This computation is only valid in the ideal case, i.e. all the incoming RF power is absorbed in the thermistor. In practice, there are some existing losses in the input transmission line, the mount structure, and others; correction factor is added to take those facts into account.

It worth to mention that the three resistors (R) are designed to have a negligible temperature coefficient of resistance; otherwise, error of measurement can be produced. To avoid having this error, the bridge is configured with two identical thermistors; where only one thermistor is exposed to the RF power; the second thermistor is used to compensate the variation in ambient temperature.

1.4.4.2 Thermocouple sensors

The working principle of thermocouple sensors is based on Peltier effect. It tells that, dissimilar metals generate a potential due to temperature differences at a hot and a cold sides of the metals as in figure 1.14. The thermocouples have been used as RF power sensors since their introduction in 1974 [48]. In practice, number of thermocouples are electrically connected in series to build the thermopile as shown in the figure 1.15.

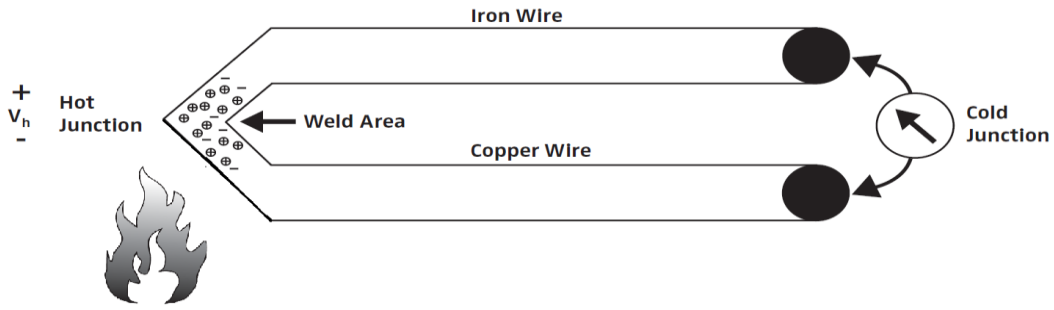


Figure 1.14 Simple thermocouple structure.

This connection can boost up the output voltage, hence, it can be easily amplified and measured by voltmeter. The thermocouples provide three main advantages over the thermistors [49]:

- They exhibit higher sensitivity levels and larger dynamic ranges.
- They are more rugged.
- They exhibit higher performance at high frequency bands. This is because the power sensor is electrically isolated from the RF input circuit, thus, it does not suffer from the problem of the high frequency leakage through the DC bias circuit.

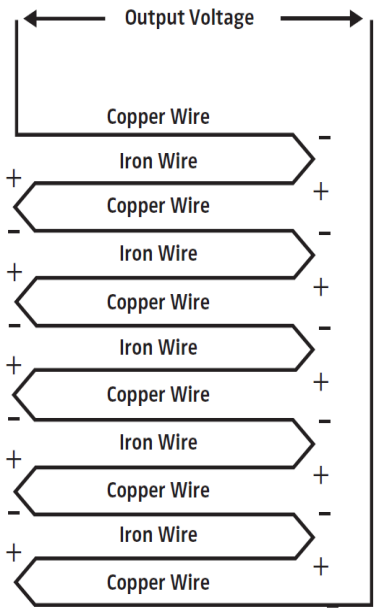


Figure 1.15 Thermocouples are connected in series (thermopile).

Operating principles:

Modern thermocouple sensors are typically designed to be integrated in silicon circuit chip [50]. The incoming RF power is injected and absorbed by an integrated RF load. This load is thermally coupled with the hot junctions of the thermopile (as illustrated in figure 1.16), hence, the heat generated in the load rises up the temperature of the hot junctions. This increase of temperature is quantified by measuring the DC output voltage of the thermopile. This voltage is very linear with input power and has a relatively long time constant due to heat flow delays.

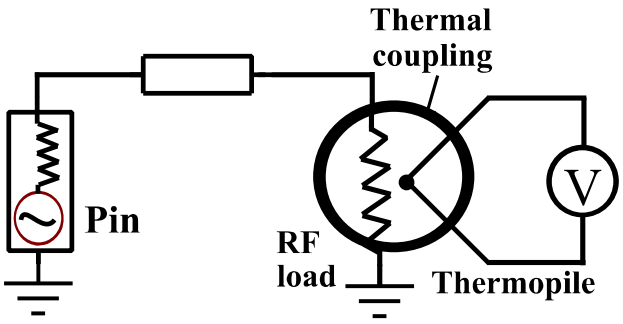


Figure 1.16 Block diagram of thermocouple detector.

1.4.5 Diode based detectors

Since 1900s, diodes have been used as passive devices in most of electronic systems [51]. Their fundamentals and applications have not changed since 1980s. However, their technologies have been continuously developed in order to improve their performances, and allow to operate at higher frequencies. In microwave engineering, the diodes are used in three main applications [52]:

- Rectification: Converting high frequency signal to DC.
- Detection: Demodulating of amplitude-modulated signal.
- Mixing: Shifting (up or down) the frequency of an input RF signal.

The diodes convert high frequency energy to DC (or low frequencies) using their rectification properties; these properties arise due to their nonlinear current-voltage (I-V) characteristic. When diode is used as a power detector, the high frequency signal is directly applied on the diode, and then, the output low frequency signal is measured.

PN, Schottky (SBD) and backward tunnel (BTD) diodes are the main diode types used in the power detection [53]. Usually, the fabrication of BTD is more difficult than SBD, however the BTDs exhibit higher sensitivity values at zero bias with lower value of video resistance, and lower temperature dependence [54].

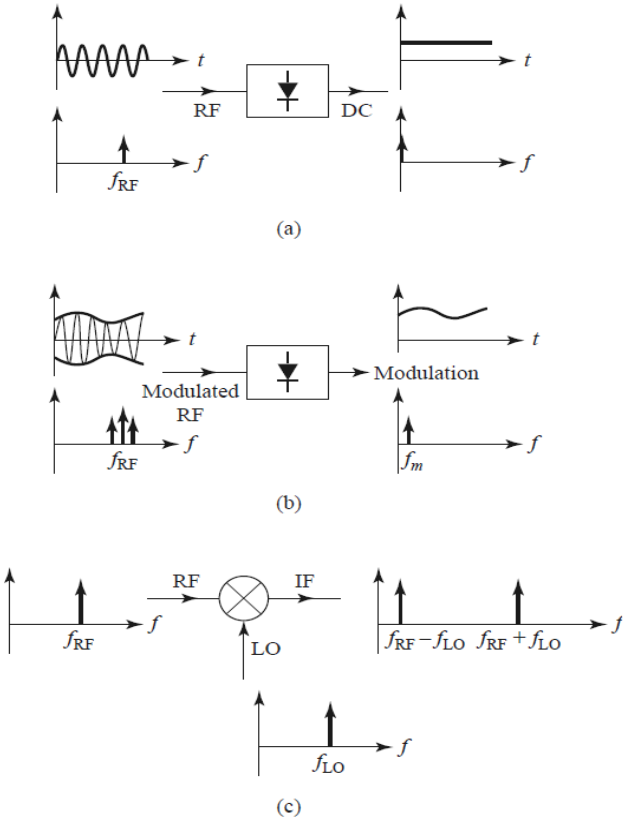


Figure 1.17 Basic diode functions: (a) diode rectifier, (b) diode detector, (c) mixer [52].

Diode based power detectors have two major advantages:

1) They are able to measure very low levels of power (down to -90 dBm).
2) They exhibit fast response, hence, they can track the fast variation of the RF signal.

On the other hand, the diodes sensors are very sensitive to ambient temperature, in addition, they have poor linearity. Therefore, the heat based detectors are still adopted as the transfer standard detectors.

1.5 Conclusion

In this chapter, we showed the importance of the power measurements in several microwave and THz applications. We also showed that the power levels are relatively

low at such high frequencies, this is due to the high losses in the mediums and systems circuitries, therefore, detectors with high sensitivity values are required.

Different types of power measurements were briefly explained, where the required measurement type is determined following the applications.

The heat and diode based detectors were briefly introduced. The heat based detectors are very accurate for true RMS power measurement. However, their response time is slow. Therefore, they are suitable for steady state or continuous wave (CW) signals. In addition, they are often used as reference power standards. The diode based detector can track the fast variations of input signals. However, they suffer from poor linearity and high sensibility to ambient temperature. The table 1.1 shows a direct comparison between those detectors, indicating the better one to be used concerning each parameter.

	Heat based detectors	**Diode based detectors**
Cost		Lower cost
Simplicity		Simpler structure
Accuracy	Most accurate	
Linearity	Best linearity	
Integrity		Easier to be integrated
Response time		Faster response
Sensibility to waveform	Not sensible to signal waveforms	
Sensibility to temperature	Less affected by ambient temperature	
Working bandwidth	Can work at larger frequency band	
Minimum detectable power		Can detect lower level of RF power
Voltage (or Current) Sensitivity		Have higher values of sensitivity

Table 1.1 Comparison between heat and diode based power detectors.

In a nutshell, each type of power sensor has its own strengths and weaknesses following its application.

Chapter 2

Diode Based Detectors

Theory & Parameters

2.1 Introduction

In this chapter, the theory of the diode based power detector will be discussed in detail, since it is the core of this thesis. Following the application, certain detector parameters are more critical than others. The correlations between these parameters will be explained in detail. This will help to develop detectors with optimal specifications, dedicated to certain applications.

2.2 Diode detector principles

RF and microwave signals can be detected using a nonlinear semiconductor device such as diodes or transistors. Figure 2.1 shows the basic configuration of diode based detectors (video receiver), where the diode is utilized to rectify the high frequency signal. This configuration can be more complicated (depending on the topology); for example, several diodes might be utilized (instead of single diode) in order to improve some detection parameters.

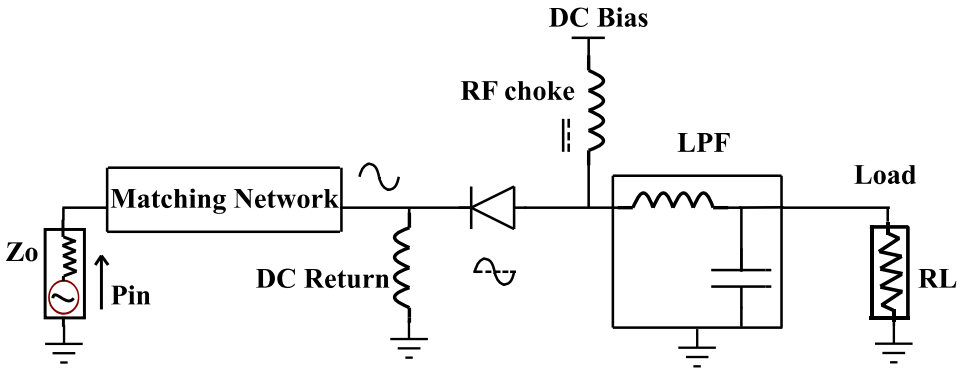


Figure 2.1 Basic diode detector configuration [55].

The function of each block is explained in the following:

- **The RF signal source:** The source can be an antenna, amplifier, or any stage which feeds an available power P_{in}, with an internal impedance Zo. P_{in} is the power to be measured.
- **Matching network:** Usually, the input impedance of detector is not matched with the source impedance Zo. Therefore, matching network is necessary to ensure that

maximum RF power is absorbed in the detector, meanwhile avoiding standing waves which can cause an error of measurement [24].

- **Diode:** (PN or Schottky) diodes or any equivalent device such as diode connected transistors can be employed to rectify the RF signal. The diode is biased using DC power (voltage or current) source to allow operating at a certain DC point. However, some types of diodes (usually Schottky diodes) have low threshold voltages, thus no DC biasing source is required; this type of diodes is called zero bias. The intrinsic equivalent circuit of diode (small signal model) consists of an active part R_j (the junction nonlinear resistor which rectifies the signal), in parallel with parasitic junction capacitance C_j (which is considered as a parasitic capacitance). As well as a series resistance R_s representing the resistance of the active layer [56].

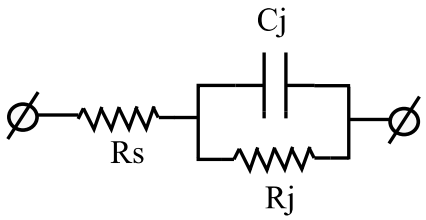


Figure 2.2 The intrinsic small signal model of diode.

- **Choke inductors:** They exhibit high impedance to RF signal and short circuit to DC and low frequency signals. The function of these inductors is to avoid RF short circuit through the DC biasing source (or the ground directly). The DC return choke inductor pulls the cathode potential to the DC ground, providing a closed DC biasing circuit. Figure 2.3 shows the circuit paths for RF and baseband signals.
- **Low pass filter (LPF):** This filter is considered as the key element to correctly follow the variation of the envelope (baseband) signal. The main function of this filter is to determine the bandwidth of the output signals (rectified signals); this bandwidth is called video bandwidth. Depending on the application, there are several LPF topologies which can be used such as RLC (as in figure 2.1) or simple RC filter. The video bandwidth has to be carefully chosen to avoid increasing the noise floor of the detector (more details are explained in paragraph 2.3.6).

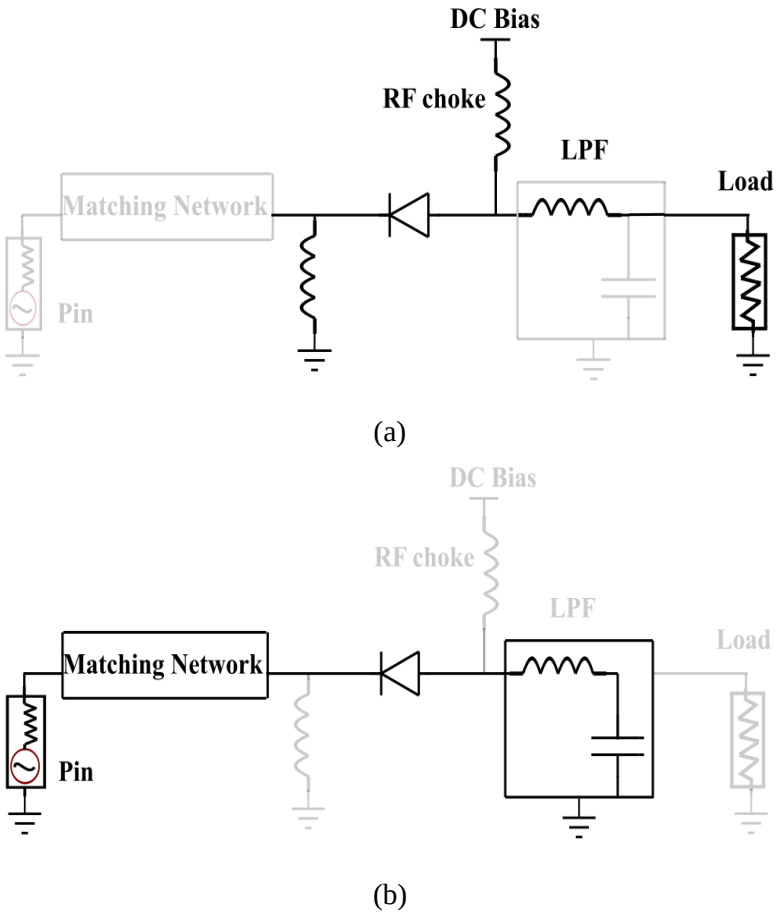


Figure 2.3 The circuit path of: (a) DC and low frequency signals, (b) RF signal.

- **Load (R_L):** The detector drives the load R_L which is connected at its output. Depending on the application, the load can be (1) a simple voltmeter, (2) an amplifier to extract the envelope signal, (3) ADC (analog to digital converter) to allow digital processing of the RF power value, (4) modulated power supply to control the biasing of an amplifier, etc. To avoid loading the detector, the internal impedance value of the diode has to be much smaller (or even negligible) comparing to the load impedance (R_L), hence, the DC biasing current only flows through the diode (more details are explained in 2.3.5).

2.3 Diode detector parameters

To establish the RF power measurement, the detector parameters have to be carefully chosen (or designed). In practice, we cannot obtain an ideal power detector with the best performances in all parameters. Therefore, some detector parameters are usually

sacrificed (or degraded) in order to improve (or make the trade-off with) others. In the following, we explain the theory of those parameters, and the relations between each other.

2.3.1 Bandwidth of interest (Δf)

The bandwidth of interest represents the desired frequency band (of RF signal) which can be measured by the detector. The bandwidth is probably the first parameter to be considered when choosing (or designing) a power detector. To maximize the absorbed power at the input, a matching network (corresponding to the bandwidth of interest) can be added (or integrated) to the detector. This network also rejects the undesired frequencies which can be injected in the detector. A bulky matching network can cause significant losses in the input power (especially at high frequencies), thus, small networks sizes are recommended.

2.3.2 Power consumption (P_D)

As discussed in the paragraph 2.2, some diodes need to be biased in order to operate at a certain DC point (Q). This helps to decrease their high impedances (since high impedance can block the input signal), and enhance their non-linearity of I-V curve (which is poor around 0). Figure 2.4 shows the different regions of I-V diode characteristic, and the static operating point Q. For the detection purpose, the diode has to be biased so the Q point is kept in the nonlinear region. The following equation provides the I-V relation of a diode [57]:

$$I = I_S.(\exp(V / n.V_T) - 1) \tag{2.1}$$

And

$$I_S = A^*.A.T^2 \exp\left(\frac{-q.\phi_B}{K.T}\right) \tag{2.2}$$

Where I , and V are the current and voltage across the junction, n is the ideality factor, I_S is the saturation current, V_T is the thermal voltage (V_T = 26 mV at room temperature), A is the

effective junction area, A^* is the effective Richardson constant, K is the Boltzmann constant, T is the absolute temperature in kelvin, and $\emptyset_B$ is the barrier height with no bias.

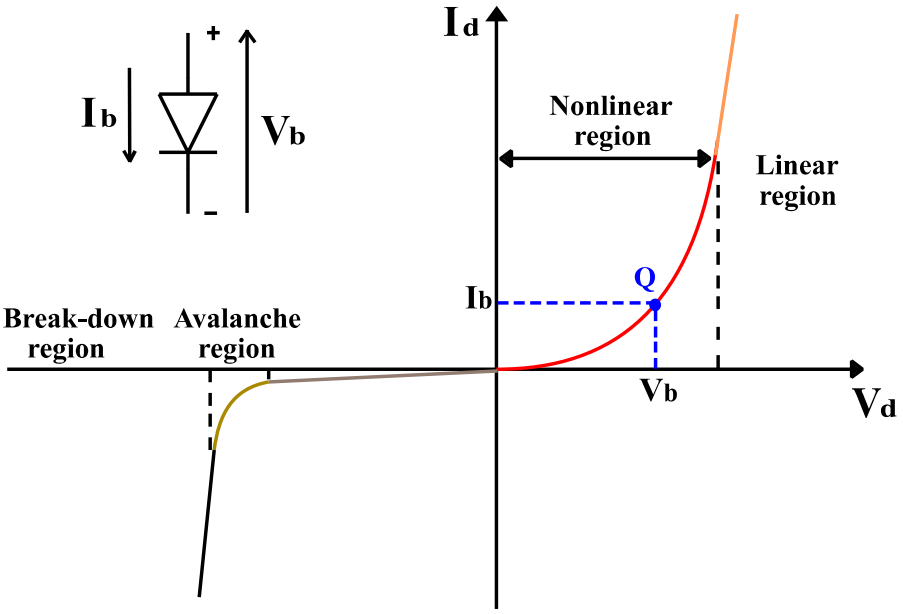


Figure 2.4 I-V characteristic of a diode in different operating regions.

The DC power consumed for biasing the diode is given in the equation 2.3.

$$P_D = V_b \times I_b \qquad (W) \tag{2.3}$$

Where V_b and I_b are the DC voltage and current biasing values. From the equation 2.3, the higher current (or voltage) biasing value, the higher is the power consumption. In some applications, the power consumption is a critical parameter. As an example, the diode detector which is employed to improve an amplifier efficiency (and decrease the overall power consumption as in ET technique in figure 1.6). In this case, using a zero bias diode (where no DC biasing required) can be the optimal solution.

Varying the value of biasing current (or voltage) affects all the detector parameters. This includes power consumption, matching condition, sensitivity value, noise floor, dynamic range and video resistance. All those effects are explained in the next paragraphs.

2.3.3 Voltage or current sensitivity (γ)

The sensitivity is the ability of a detector to convert the input RF signal into DC or low frequency signal. The last corresponds to extract the envelope signal of high frequency signal. In this thesis, we are interested in the voltage sensitivity values, thus, DC current source is required for biasing the diode.

We define (V_{OFF}) as the DC voltage across the diode corresponding to the DC biasing current (I_b); while the voltage (V_{ON}) is the DC voltage across the biased diode (using the same I_b) when the RF power is applied (as illustrated in figure 2.5).

For low level of RF power, the difference voltage ($V_{OFF} - V_{ON}$) is proportional to the applied RF power. The voltage sensitivity (response coefficient in V/W) of a diode can be defined by the equation 2.4.

$$\gamma = \frac{V_{OFF} - V_{ON}}{P_{in}} \qquad (V/W) \qquad (2.4)$$

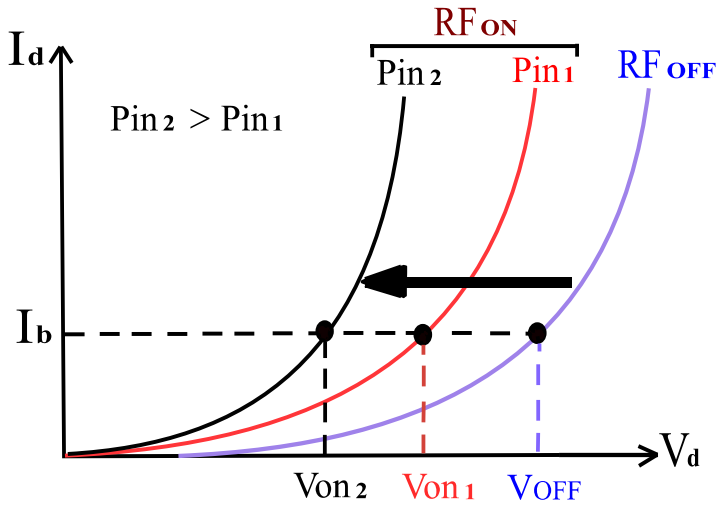


Figure 2.5 I-V curves for three states of input RF power, with a constant biasing current I_b.

In the equation 2.4, P_{in} is the available input power. Higher sensitivity value means that the detector is able to generate higher output DC voltage for lower RF input power. This is considered one of the most important parameters for selecting a power detector. For example, in millimeter and submillimeter waves applications, the level of losses in the overall systems is relatively high and signal levels usually of limited power. Thus,

week levels of RF input power is usually to be measured. In this case, having power detector with high sensitivity value is mandatory.

The sensitivity value depends on several parameters mentioned in the following:

- Physical characteristics of the device: We can mention several characteristics such as doping level of the active layer, and series (access) resistances of the diode. The efficiency of the device increases (and so the sensitivity value) by decreasing the parasitic effects, such as parasitic capacitance with substrate.
- Working frequency: Working at higher frequencies increases the overall losses in the detectors (access lines, connectors …). In addition, the parasitic effects in the diode (such as junction capacitance and capacitances with the substrate) become more dominant. Those issues degrade the detection efficiency and so the sensitivity value.
- Matching condition: If the detector impedance is not matched, part of the input power will be reflected leading to smaller sensitivity value. This is because that the detector only indicate the absorbed power in the diode.
- Diode temperature: Increasing the diode temperature degrades the sensitivity value, this is due to the R_j which becomes less dominant as compared to C_j. In this thesis, we propose a detector with temperature compensation structure; this design helps having a stable detector performance over the temperature (paragraph 4.2.4).
- Diode Size: The intrinsic sensitivity value of the diode (which considers the response of diode as stand-alone device) is proportional to R_j value ($\gamma_{Intrinsic} \propto R_j$) as shown in Annex 1. Smaller diode sizes exhibit higher sensitivity values (for the same biasing condition). This is due to the higher R_j values exhibited by these diodes. Since smaller diode sizes require larger sizes of matching networks, a trade-off between diode and matching network sizes has to be considered.
- Biasing condition: When the biasing current (or voltage) increases, the R_j value becomes smaller, hence, smaller value of sensitivity is produced.
- Load effect: When the detector is loaded by a low impedance value, part of the output voltage will be dropped in the internal diode resistance (R_V), hence, smaller sensitivity value is produced. More details are explained in paragraph 2.3.5.

Varying the sensitivity value affects some other parameters including dynamic range *Dy*, noise floor (NEP) and figure of merit FOM. All those effects are explained in the next paragraphs.

2.3.4 The detector noise floor

The effect of noise is critical to most of RF and microwave systems, because it ultimately limits the system performance. Noise determines the threshold for the minimum signal that can operate the system, and sometimes causes deformations in the useful RF signals.

Concerning the power detectors, noise power can be introduced from the external environment, as well as generated internally by the detector itself and/or by the circuitry. To reduce the effect of external noise, shielding the detectors and their circuitry elements is necessary. The semiconductor devices (diodes and transistors) are the main responsible of generating the internal noise.

Depending on the biasing conditions, several types of noise can be generated in the diode. The main four types of noise are briefly explained in the following.

2.3.4.1 Thermal (Johnson) noise

It is considered as the most basic type of noise, being created by the vibration of bound charges due to the thermal excitation. The thermal motion of carriers creates fluctuating voltage on the terminals of resistive element. The average value of this voltage is null, however the power on its terminals is not zero. The generated noise power in a resistor (R) can be represented by a voltage source in series with the resistor or a current source in parallel with the resistor (as shown in figure 2.6). The equations 2.5 and 2.6 describe the values of those sources [58].

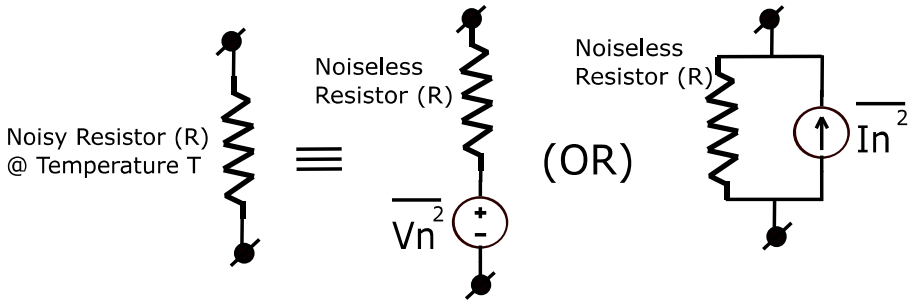


Figure 2.6 The equivalent circuit of noisy resistor (R) at temperature T in voltage and current modes [58].

$$V_n = \sqrt{4.K.T.R}.\sqrt{\Delta f} \quad (V) \tag{2.5}$$

$$I_n = \sqrt{\frac{4.K.T}{R}}\sqrt{\Delta f} \quad (A) \tag{2.6}$$

Where K is the Boltzmann constant, T is the absolute temperature in kelvin, R is the resistor value, and Δf is the frequency bandwidth. The thermal noise power density is independent of frequency, thus, it is considered as white noise.

The source of thermal noise in biased diodes consists of the contribution of (R_S) only. However, in zero bias diodes, two contributions are included (R_j & R_s). This will be explained in detail in paragraph 2.3.4.4.

2.3.4.2 Flicker (1/*f*) noise

This type of noise is dominant in low frequency range, its spectral density function is proportional to 1/*f*. The flicker noise appears when there is a DC biasing current (I_b) passing through the diode. The main cause of this noise is the imperfection of fabrication process [58]. The equation 2.7 represents the noise spectral density function for the Hooge model [59].

$$S_{1/f} = \frac{2000.I^{\alpha}}{f^{C}.N} \tag{2.7}$$

Where N is the number of carriers, α and C are material constants. From the equation 2.7, it can be concluded that $1/f$ noise is more dominant at higher levels of biasing current (I_b) and lower frequencies.

2.3.4.3 Avalanche noise

This type of noise is generated when the diode is reversed biased in the avalanche region. When high electric field is reversely applied on a diode, carriers in the junction gain energies and then they collide with the crystal lattice. If the energy gained between collisions is large enough, then during collision, another pair of carriers (electron and hole) can be generated. This random process is the main cause of the avalanche noise [58]. This type of noise is not concerned in our study, because the diode detectors are operated in forward regime.

2.3.4.4 Shot noise

This type of noise arises because of flowing of vast number of discrete charges which are not totally analogue phenomenon. The continuous flow of these discrete pulses gives rise to almost white noise called shot noise [58].

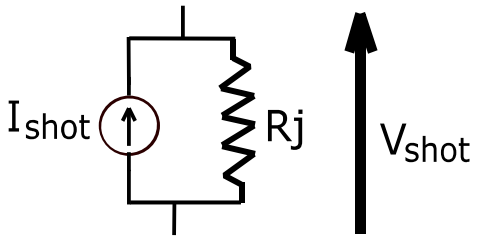


Figure 2.7 The equivalent circuit of shot noise generated in diode junction [58].

The shot noise is generated in the diode junction, its current power density is given in equation 2.8 [58].

$$S_I = 2q(I_b + 2I_S) \qquad (A^2/Hz) \tag{2.8}$$

Where q is the electron charge, I_S is the saturation current, and I_b is the DC biasing current. When a diode is biased by DC current $I_b \gg I_S$, hence we get $S_I = 2q.I_b$. The shot current spectral density is given as $I_{Shot} = \sqrt{S_I} = \sqrt{2q.I_b}$. Hence the generated shot voltage can be given as in equation 2.9:

$$V_{Shot} = I_{Shot} \times R_j = \sqrt{2q.\frac{n.K.T}{q.R_j}} \times R_j = \sqrt{2.n.K.T.R_j} \qquad (\mathrm{V}/\sqrt{Hz}) \tag{2.9}$$

When zero bias diode is used, $I_b = 0$ => $S_I = 4q.I_S$. The shot current spectrum density is given as $I_{Shot} = \sqrt{S_I} = \sqrt{4q.I_S}$. Hence the generated shot voltage can be given as in equation 2.10:

$$V_{Shot} = I_{Shot} \times R_j = \sqrt{4q.\frac{n.K.T}{q.R_j}} \times R_j = \sqrt{4.n.K.T.R_j} \qquad (\mathrm{V}/\sqrt{Hz}) \tag{2.10}$$

It can be noticed that the noise voltage generated in the case of zero bias diode (equation (2.10)) has the nature of thermal noise (V_n in equation (2.5)).

Finally, based on the different noise types discussed above, we can conclude that zero bias diode only generates thermal noise, since no DC current passes through. This can be an advantage of using this type of diodes.

2.3.4.5 Estimation of noise equivalent power (NEP)

The NEP value represents the detector noise floor within a 1 Hz video bandwidth. Thus, it determines the minimum RF power that can be measured by a given detector.

It is desirable to have small NEP value, so the detector is able to measure lower levels of RF power. The NEP formula is given in the equation 2.11 [60].

$$NEP = \frac{V_{noise}}{\gamma} \qquad (W/\sqrt{Hz}) \qquad (2.11)$$

$$P_{in\_\min} = NEP \times \sqrt{BW} = \frac{V_{noise}}{\gamma}.\sqrt{BW} \qquad (W) \qquad (2.12)$$

Where V_{noise} represents the total noise voltage spectrum (V/$\sqrt{Hz}$) generated in the diode, P_{in_min} is the minimum detectable power, and BW is the video bandwidth.
In the case of using biased diode, and if the shot and thermal noises are dominant (usually for modulated signal where flicker noise is eliminated), the NEP relation can be written using the equation (2.9), (2.10) and (2.11) as the following:

$$NEP = \frac{\sqrt{2.n.K.T.(R_j + 2R_S)}}{\gamma} \qquad (W/\sqrt{Hz}) \qquad (2.13)$$

On the other hand, the NEP value of zero bias diode is given in equation (2.14), where the thermal noise is the only source of noise:

$$NEP = \frac{\sqrt{4.n.K.T.R_j}}{\gamma} \qquad (W/\sqrt{Hz}) \qquad (2.14)$$

Since the intrinsic sensitivity is proportional to R_j

$$=> NEP_{Intrinsic}\ \alpha \frac{\sqrt{R_j}}{R_j} \alpha \frac{1}{\sqrt{R_j}}.$$

As a conclusion, maximum value of R_j (and so small diode size) is required for minimum NEP value.

2.3.5 Video resistance (R_V)

The video resistance is defined as the resistance exhibited by the diode in the video (baseband) frequency bandwidth. The diode video resistance is given as in the following:

$$R_V = R_S + R_j \approx R_j = \frac{dV_d}{dI_d} = \frac{n.K.T}{q.(I_S + I_b)} = \frac{n.V_T}{I_S + I_b} \qquad (\Omega) \qquad (2.15)$$

R_S is the series (access) resistance of diode. Usually, when the diode is biased in the nonlinear region, the R_S value is negligible compared to R_j.

From the equation 2.15, R_V varies with:

- Temperature.
- Biasing current for biased diode ($I_b \gg I_S$ => $R_V = \frac{n.V_T}{I_b}$).
- Diode size for zero bias diode ($I_b = 0$ => $R_V = \frac{n.V_T}{I_S}$ => $R_V \propto \frac{1}{A}$ from equation 2.2).

In the baseband frequency, a diode detector can be considered as a video voltage source (V_{det}) with an internal impedance R_V. Figure 2.8 shows the video equivalent circuit for a detector loaded with resistance R_L and smoothing capacitor C_L (forming RC low pass filter). The output voltage V_{Out} for baseband signals is given as in the following:

$$V_{Out} = \frac{Z_{R_L//C_L}}{Z_{R_L//C_L} + R_V} V_{\det} \qquad (V) \qquad (2.16)$$

The equation 2.16 shows the effect of the smoothing capacitor and load resistance on the output voltage. Ideally, it is desirable to obtain $V_{Out} = V_{det}$, i.e. the total output voltage of the detector is delivered to the load. To achieve that, the video resistance has to be much smaller than the load ($R_V \ll Z_{R_L//C_L}$). For high values of R_V, the diode bias (or size) can be adjusted to reduce the R_j value (meanwhile maintaining the trade-off with other parameters).

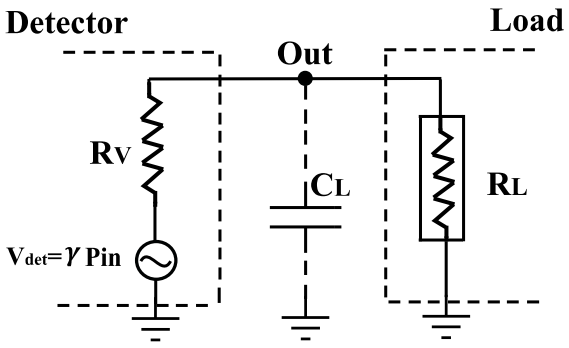


Figure 2.8 The video equivalent circuit of diode detector loaded by resistance R_L with smoothing capacitor C_L.

A detector is considered useful when the voltage degradation is not more than 10% [61]. On the other hand, when the diode is used for wireless energy harvesting (rectenna), the DC rectified power (instead of voltage) has to be delivered to the load R_L. In this case, it is desirable to have $R_V = R_L$ for maximum power deliverance.

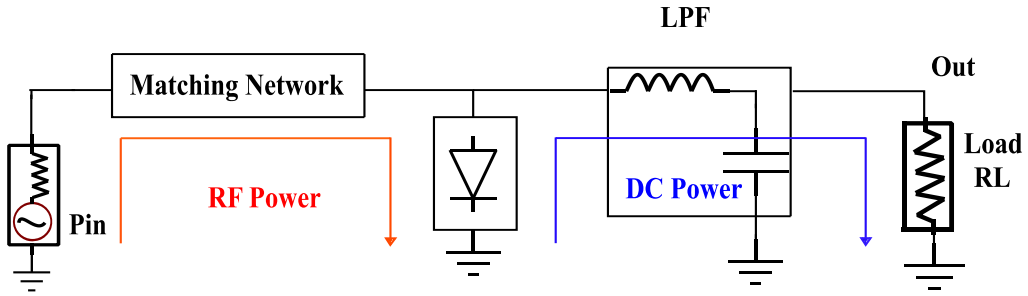


Figure 2.9 The RF and DC power paths in rectenna.

2.3.6 Video bandwidth (*BW*)

As explained in the paragraph 2.2, the video bandwidth is the signal frequency band at the detector output. It is mainly determined by the filter (LPF) connected at the detector output, the video resistance, and the load resistance values.

If an envelope signal with frequency $f_{envelope}$ is required to be detected, the video bandwidth *BW* has to be larger than $f_{envelope}$ in order to correctly follow the variation of the envelope. On the other hand, the *BW* does not have to be very large, so that the minimum detectable power P_{in_min} is maintained as low as possible (equation (2.12)).

Usually, a simple capacitor (C_L) is connected in parallel with the load (R_L) forming RC low pass filter as in figure 2.8. In this case, the video bandwidth is given as in the following:

$$BW = \frac{1}{2\pi . R_T C_L} \qquad (Hz) \qquad (2.17)$$

Where R_T is the equivalent parallel resistance ($R_T = R_V // R_L$). The value of C_L is tuned to obtain the desired video bandwidth, i.e. exhibiting high impedance for envelope signal and low impedance (short circuit) for RF signals.

2.3.7 Dynamic range (*Dy*)

The dynamic range is defined as the range of RF power levels where the detector response is in the linear region (i.e. the output voltage is linear to the applied RF power). As illustrated in figure 2.10 (a), we can distinguish three different behaviors of diode voltage depending on the input power level.

- When the RF power is too low (smaller than P_{in_min}), the signal is imbedded below the noise floor, hence, there is no useful readout value.
- When the input power is increased, the diode voltage becomes proportional to the square of input voltage, i.e. input RF power (P_{in}), so it is called square law region.
- When the input power reaches a certain level called (P_{in_max}) or the compression point, the output voltage is now proportional to the input RF voltage (instead of power), so it is called linear region [47].

The dynamic range can be given as in the equation (2.18).

$$Dy = P_{in\_\max(dBm)} - P_{in\_\min(dBm)} \qquad (\text{dB}) \qquad (2.18)$$

or in linear scale

$$Dy = \frac{P_{in\_\max(\mu W)}}{P_{in\_\min(\mu W)}} \qquad (2.19)$$

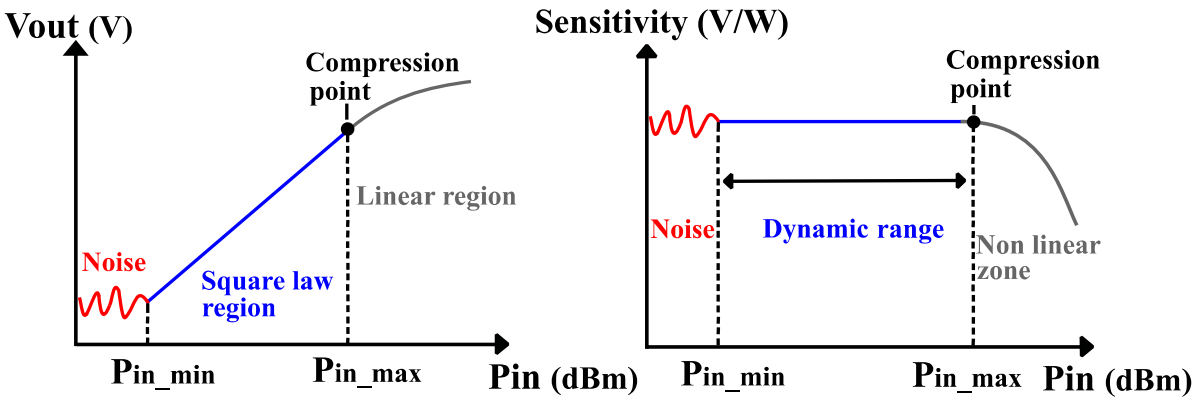


Figure 2.10 (a) The output voltage behavior of diode versus input RF power, (b) the sensitivity curve versus input RF power.

The figure 2.10 (b) represents the sensitivity curve versus the input power showing the dynamic range and the nonlinear zone; this curve is a direct result from the diode voltage behavior with input power.

An attenuator is usually added to the detector circuit reducing the power absorbed in the diode, thus, the compression point occurs at higher level of input power; however the sensitivity value is degraded.

For a given diode and biasing current value, the detection simulation using ADS (explained in paragraph 3.4.4) shows that the product ($const. = P_{in\_max} \times \gamma$) is constant while changing the attenuation factor. This constant (*const.*) value depends on the characteristic of diode device. Based on equations 2.12 and 2.19, we can write the following development.

$$Dy = \frac{P_{in\_\max}}{P_{in\_\min}} \propto \frac{const./\gamma}{\sqrt{R_j.BW/\gamma}} \propto \frac{const.}{\sqrt{R_j}.} \qquad (2.20)$$

The parameter *BW* is considered to be fixed (from the design point of view), since it is determined by the envelope signal frequency.

It can be concluded that the dynamic range is increased as decreasing the R_j value (on the opposite of the sensitivity ($\gamma_{Intrinsic} \propto R_j$)). This can mathematically explain the reason that (*Dy*) and (γ) have opposite behaviors.

2.3.8 Figure of merit (FOM)

The figure of merit FOM is defined as a quantity used to characterize the performance of a detector; it is usually used to make the comparison between the detector performances. There are several criterions to evaluate the performance of detector, the most common FOM is given in the following [55]:

$$FOM = \frac{\gamma}{\sqrt{R_V}} \tag{2.21}$$

In some cases, an attenuator is added to the detector in order increase the dynamic range *Dy*. Hence the sensitivity value (γ) is decreased whereas the video resistance (R_V) is not affected, and so, the FOM is decreased.

In order to qualify the performance of a stand-alone detector (without attenuation effects), we adopt another criterion based on the product ($Dy \times \gamma$) taking the sensitivity and the dynamic range into account:

$$FOM = Dy \times \gamma \qquad \text{(V/W)} \tag{2.22}$$

Where *Dy* is in linear scale (equation 2.19), γ is in V/W.

2.4 Conclusion

In this chapter, the working principles of the basic diode detector were discussed, where the function of each block was briefly explained. In addition, all the detector parameters are explained in detail, showing the effects and the relations between each other. In the following, some conclusions are mentioned:

- It has been shown that when the sensitivity value increases, the dynamic range is decreased, and vice versa.

- For zero bias diode, small intrinsic NEP value can be obtained using a diode with large R_j value (small diode size).
- The video bandwidth BW has to be carefully designed, so the detector is able to track the signal envelope variation, meanwhile keeping low NEP value.
- Varying the diode size affects all the intrinsic parameters. Figure 2.11 summarizes these effects considering zero bias diode.

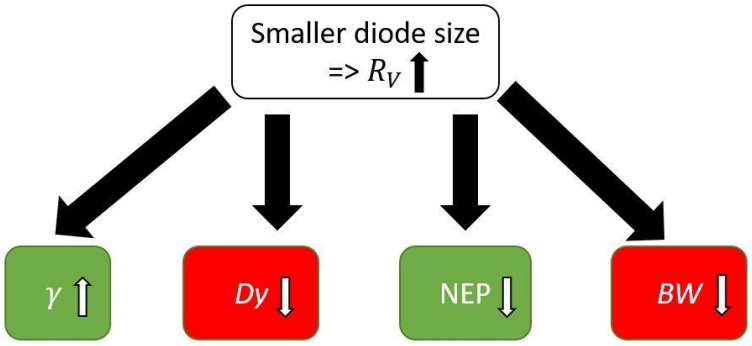


Figure 2.11 The effects of diode size over the intrinsic parameters considering zero bias diode.

Chapter 3

PN Diode Detectors

Design & Characterization

3.1 Introduction

As shown in chapter 1, the RF power detectors are considered as the key blocks in many RF systems. Depending on the applications, there are several detector configurations that might be utilized, such as different diode types and sizes, different circuit topologies, etc.

In this chapter, we will discuss the extraction of the electrical model of PN diode integrated in the SiGe 55-nm BiCMOS technology from STMicroelectronics, since it is a device under development. Subsequently, the design and characterization of detectors based on the same diode will be presented. Finally, the variation of the diode characteristics with temperature is studied, the aim is to help designing a temperature compensated detector.

3.2 The technology SiGe 55-nm BiCMOS

In this paragraph, we briefly present the technology SiGe 55-nm BiCMOS which is used to build our detectors. This technology is dedicated for millimeter wave applications. It provides high system integrity by offering the ability to process the digital and analog signals on the same chip. It is derived from the 65-nm CMOS technology providing the MOSFET and HBT transistors on the same chip. The HBT transistor in this technology can reach the maximum and current cutoff frequencies of 320 GHz and 370 GHz respectively [62].

The structure of the technology 55-nm BiCMOS is composed of 8 metal layers of copper, and the last layer of aluminum as shown in figure 3.1. The layers in the technology are connected using vias, i.e. establishing the connections among different types of components; this includes the elements in the metal layers (capacitors, inductors, ..) and the components in the active zone (transistors, diodes, ..). The metal layers with the vias form the back-end of line (BEOL). The thicknesses of the metal layers are different, the metal 8 offers the thickest layer in order to exhibit lower losses in the inductors and transmission lines. The AP layer is located on the top of metal 8 where the connection with outside circuits is required (such as input and output pads).

In order to protect the circuits, the passivation layer covers the whole circuits structures unless the AP layers keeping the connection with the outside circuits.

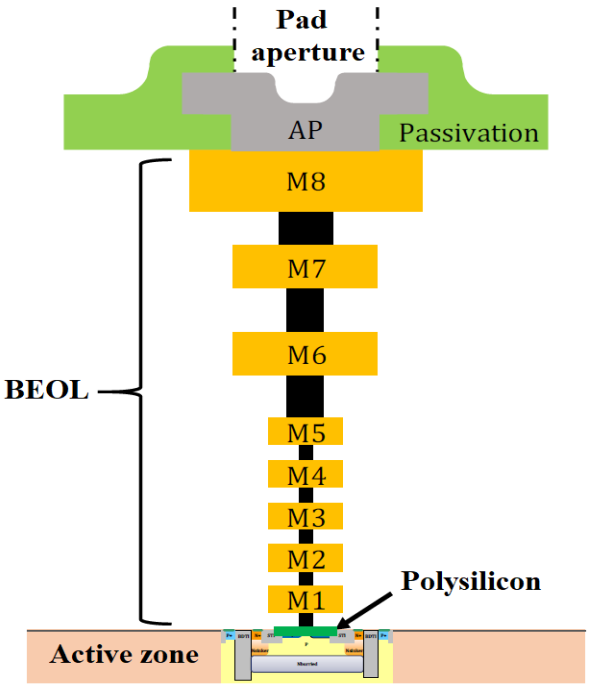


Figure 3.1 The back-end diagram of the 55-nm BiCMOS technology from STMicroelectronics.

3.3 Extraction of the diode parameters

The PN diode used in our detectors is under development, thus, it is not available in the design kit of the technology. In order to represent the diode in the design schematic and estimate its performance, the small signal model and other diode parameters are extracted up to 110 GHz as presented in the following [63].

The test structure used to extract the diode parameters is shown in figure 3.2. It is composed of the diode mounted in 2-ports configuration, connected to dedicated RF pads through access lines on metal level 8 and vias.

The intrinsic small signal model of the diode is presented in paragraph 2.2 figure 2.2. It includes the R_j , C_j representing the junction resistance and capacitance respectively, and R_S representing the series resistance of the active layer.

Figure 3.3 shows the small signal model of the test structure including the intrinsic and extrinsic models.

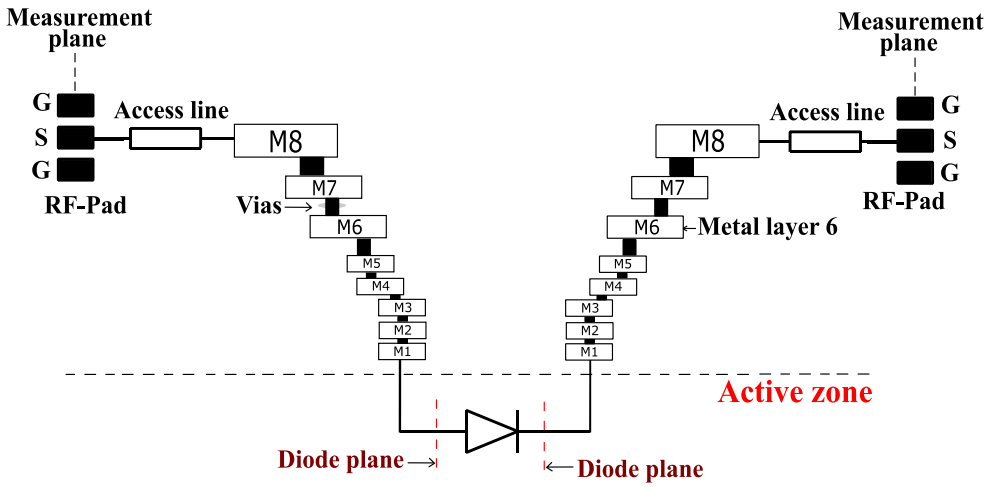


Figure 3.2 The test structure diagram of the diode stand alone.

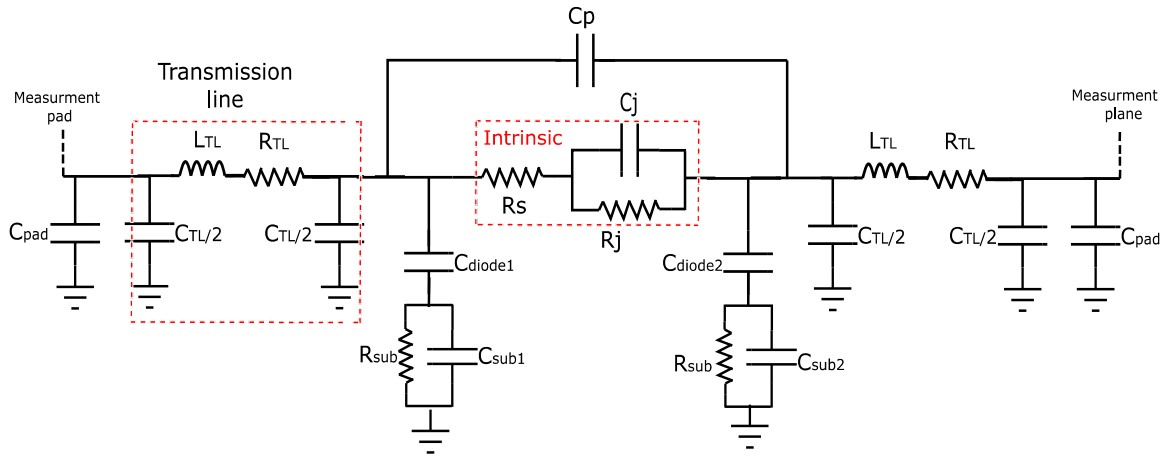


Figure 3.3 The test structure model including the intrinsic and extrinsic elements.

For the extrinsic model, several elements are included:

- C_p represents the anode to cathode capacitance due to back-end structure.
- R_{TL}, L_{TL} and C_{TL} form the equivalent circuit of the access line.
- C_{pad} represents the capacitive effect of the RF pad.
- C_{diode} is the capacitance between the diode and substrate. R_{sub} , C_{sub} are the parallel resistance and capacitance of the substrate respectively.

It is worth to mention that the structure of the back-end access of the diode (in the figure 3.2) is not vertical, this design shape helps to reduce the value of back-end capacitance C_p.

R_j and R_s can be extracted from the I-V characteristic of the diode; where R_j is deducted from the slope of the I-V curve at a given operating point, and R_s can be calculated at any point in the linear zone.

The I-V characteristic curves are measured and shown in figure 3.4 for two different diode sizes (L1N1 and L2N5), the goal is to investigate the effect of the diode size on the detector performance; the relation of this characteristic is given in equation 3.1. Here L1N1 is the diode which has one anode finger with 1µm as finger length, L2N5 is the diode which has five anode fingers with 2µm as finger length. This corresponds to diode junction sizes of 0.34 µm² and 3.4 µm² respectively. The diodes layouts are illustrated in the figure 3.5. Those diodes are

$$I = I_S.(\exp(V / n.V_T) - 1) \tag{3.1}$$

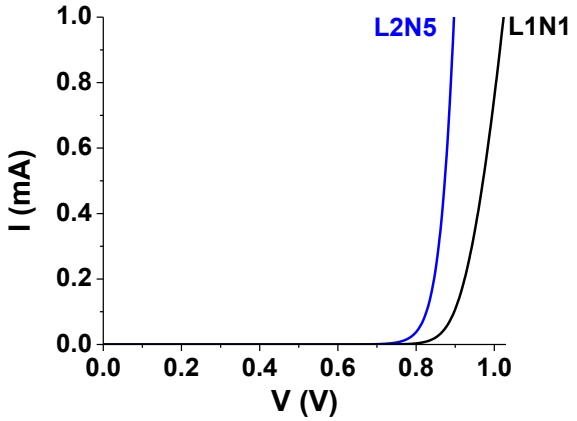


Figure 3.4 The I-V measured curves for L1N1 and L2N5.

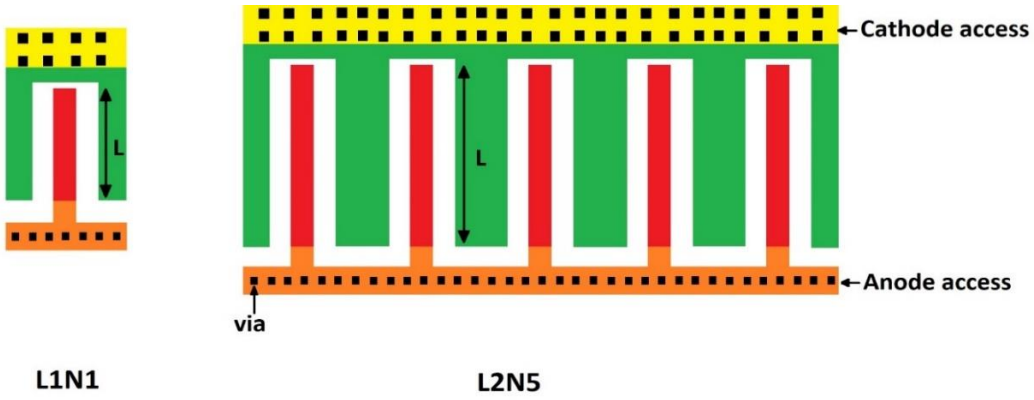


Figure 3.5 The layout illustration of the diodes L1N1 and L2N5.

In order to extract the extrinsic elements values, S parameters measurements of the dummy structures (shown in figure 3.6) were performed from 0.1 to 110 GHz, then, they were transferred into Z and Y parameters.

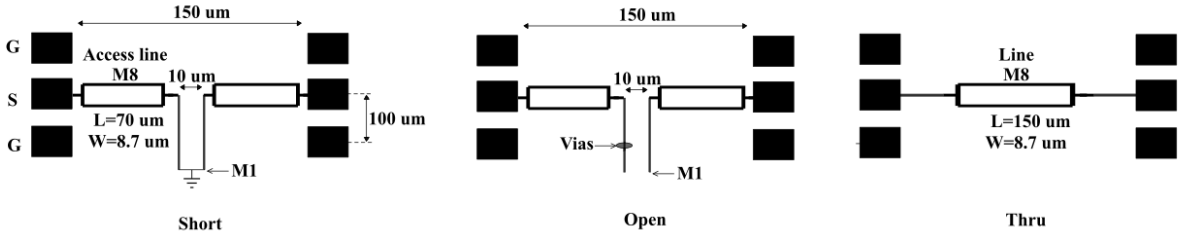


Figure 3.6 The dummy structures diagrams.

The values of C_{pad} and C_p can be extracted using the open structure, this structure can be represented by a Pi network as shown in figure 3.7. At low frequencies (f < 20 GHz), the impedance of C_p is dominant, hence the value of C_p is given as :

$$C_p = \frac{imag.(-Y_{21})}{2.\pi.f} \tag{3.2}$$

The extracted value is C_{Pad} = 3 fF.

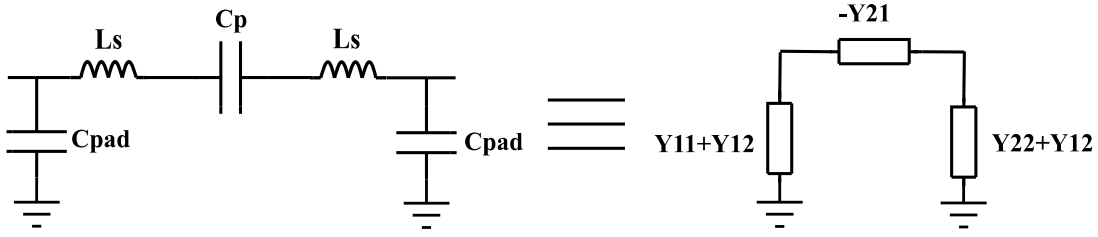


Figure 3.7 The Equivalent Pi network of open structure.

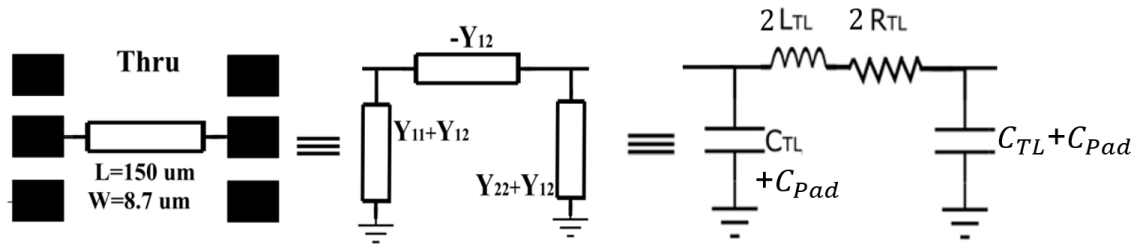
Meanwhile, C_{pad} is calculated at high frequencies (f > 50 GHz) as in the following:

$$C_{Pad} = \frac{imag.(Y_{11}+Y_{12})}{2.\pi.f} = \frac{imag.(Y_{22}+Y_{12})}{2.\pi.f} \tag{3.3}$$

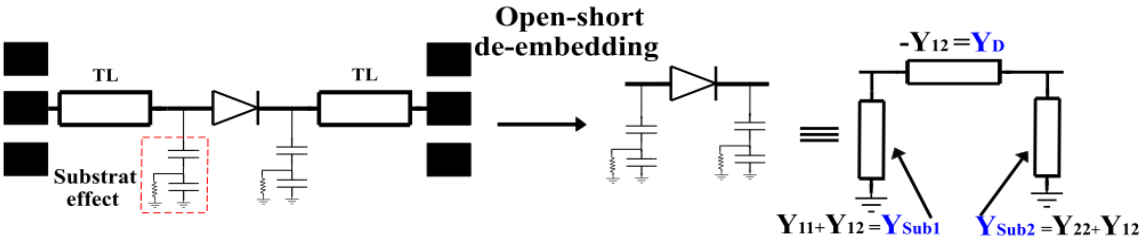
The values of R_{TL}, L_{TL} and C_{TL} can be extracted using the thru structure, this structure can be represented by a Pi network as shown in figure 3.8 (a). R_{TL} and L_{TL} are extracted using the real and imaginary values of $-Y_{12}$, on the other hand, C_{TL} is extracted using the following equation:

$$C_{TL} = \frac{imag.(Y_{11} + Y_{12})}{2.\pi.f} - C_{Pad} \tag{3.4}$$

The extracted values are R_{TL} = 0.4 Ω, L_{TL} = 30 pH, C_{TL} = 10 fF.



(a)



(b)

Figure 3.8 The equivalent Pi network of : (a) thru structure, (b) de-embedded test structure.

In order to extract the junction capacitance C_j, the impedance of the diode Z_D is required (in the diode plane figure 3.2), this can be done as the following:

S parameters measurements of the test structure were performed (for several values of biasing current) from 0.1 to 110 GHz. The open-short de-embedding method [64] is used to remove the effects of the RF-Pads and access lines (figure 3.8 (b)). The de-embedded S parameters are converted into Y parameters. Finally, the diode impedance is extracted as $Z_D = -1/Y_{21}$ considering that the de-embedded structure as a Pi network. The extracted capacitance C_P is very small (1fF), and so it is supposed to be

negligible compared to the diode impedance. Based on this assumption, we can consider that the diode impedance Z_D is represented by the intrinsic model in figure 3.3. The diode impedance Z_D is given in equation 3.5, and C_j can be concluded as the solution of the equation 3.6.

$$Z_D = R_s + \frac{R_j}{1 + w^2 R_j^2 C_j^2} - j\frac{wR_j^2 C_j}{1 + w^2 R_j^2 C_j^2} \tag{3.5}$$

$$(imag(Z_D).w^2.R_j^2).C_j^2 + (w.R_j^2).C_j + imag(Z_D) = 0 \tag{3.6}$$

Where *w* is the angular frequency and *imag(Z_D)* is the imaginary part of the measured impedance of the de-embedded structure. R_j is the junction resistance which is already extracted from the I-V characteristic.

Respecting two conditions: (i) The extraction of the C_j value is done at high frequency, (ii) The value of R_j is high as compared to the impedance of C_j (which is the case of this study), hence C_j can be also deduced using equation 3.7 which gives approximately the same result of the equation 3.6.

$$C_j \approx -\frac{1}{w.imag(Z_D)} \tag{3.7}$$

The C_{diode}, R_{sub} , C_{sub} are also extracted from the de-embedded test structure (figure 3.8 (b)). Based on the measurements, the real part impedance (R_{sub}) has relatively high value (higher than 5 kΩ), and so it is negligible as compared to the substrate capacitances. Consequently, the substrate effect will be represented by one capacitor for each diode side (C_{sub-L} and C_{sub-R}) as the equivalence of two series capacitors (C_{diode} and C_{sub}). The C_{sub-L} and C_{sub-R} values are extracted from $Y_{Sub1}$and Y_{Sub2} respectively (figure 3.8 (b))

Extraction results:

The extracted values of model elements are reported in tables 3.1 and 3.2 for (0.1, 1, 10) µA biasing currents and two sizes of diode (L1N1 and L2N5).

Biasing current I_b (µA)	C_P (fF)	C_{sub-L} (fF)	C_{sub-R} (fF)	R_S (Ω)	R_j (kΩ)	C_j (fF)
0.1	0.7	0.5	5	60	250	2.2
1					24	4.4
10					2.7	15.8

Table 3.1 The extracted model elements values for L1N1.

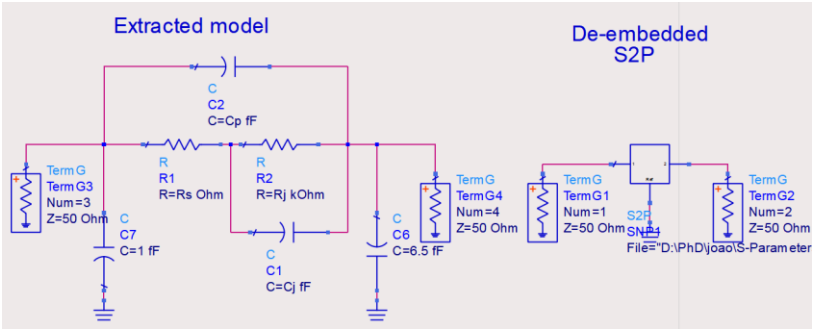
Biasing current I_b (µA)	C_P (fF)	C_{sub-L} (fF)	C_{sub-R} (fF)	R_S (Ω)	R_j (kΩ)	C_j (fF)
0.1	1	1	6.5	18	245	16
1					23	23
10					2.4	45

Table 3.2 The extracted model elements values for L2N5.

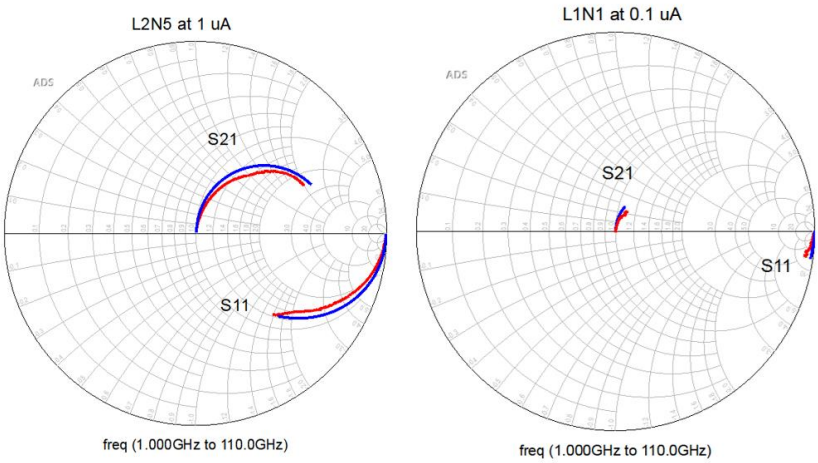
To validate the model, the extracted elements values were used to simulate the extracted model in ADS Keysight® software, where the S-parameters of the de-embedded measurements (S2P box) and the extracted model are compared as illustrated in figure 3.9 (a).

Figure 3.9 (b) shows the comparison results of the S-parameters, where good agreement is obtained over the whole frequency range. This fact confirms our assumptions and validates the proposed model.

Based on the measured I-V curves and the equation 3.1, the *n* and the I_s values are also extracted (and reported in table 3.3) using the same method proposed in [65].



(a)



(b)

Figure 3.9 (a) The schematics of ADS simulation of the extracted model and measurements, (b) comparison of measured and extracted S_{11} and S_{21} of the PN diode for two sizes (L1N1 @ 0.1 µA, and L2N5 @ 1uA).

Diode	n	I_s (A)
L1N1	1.025	5E-20
L2N5	1.027	5E-19

Table 3.3 Extracted ideality factor and saturation current values for L1N1 and L2N5.

3.4 Design of adjustable power detector based on PN diode

With the diversity of the applications provided by 5G and IoT systems, power detectors with different characteristics are required. In this context, we present the design and characterization of two adjustable (tunable) power detectors, based on PN diodes.

The detectors are designed based on two sizes of PN diodes (L1N1 and L2N5), hence, we will name the detector by its diode name. The working frequency band is (35 - 50)

GHz allowing the detectors to cover several 5G bands (37 - 40.5) GHz, (42.5 - 43.5) GHz, (45.5 - 47) GHz and (47.2 - 50.2) GHz [19]. When the value of biasing current is adjusted, all the detector parameters can be tuned. This includes the video resistance (R_V), maximum input RF power (P_{in_max}), voltage sensitivity (γ), and power consumption (P_D). This characteristic makes the detectors suitable for different 5G applications providing adjustable parameters. The objectives are to:

- Design a tunable power detector, suitable for different 5G applications.
- Investigate the effect of the diode size on the detector performance.

The detector circuit schematic is shown in figure 3.10, it consists of three main blocks: (i) N-load circuit, (ii) PN diode, (iii) matching network. In the following, each block circuit is discussed. Subsequently, the simulation of the detectors using ADS Keysight© software is explained.

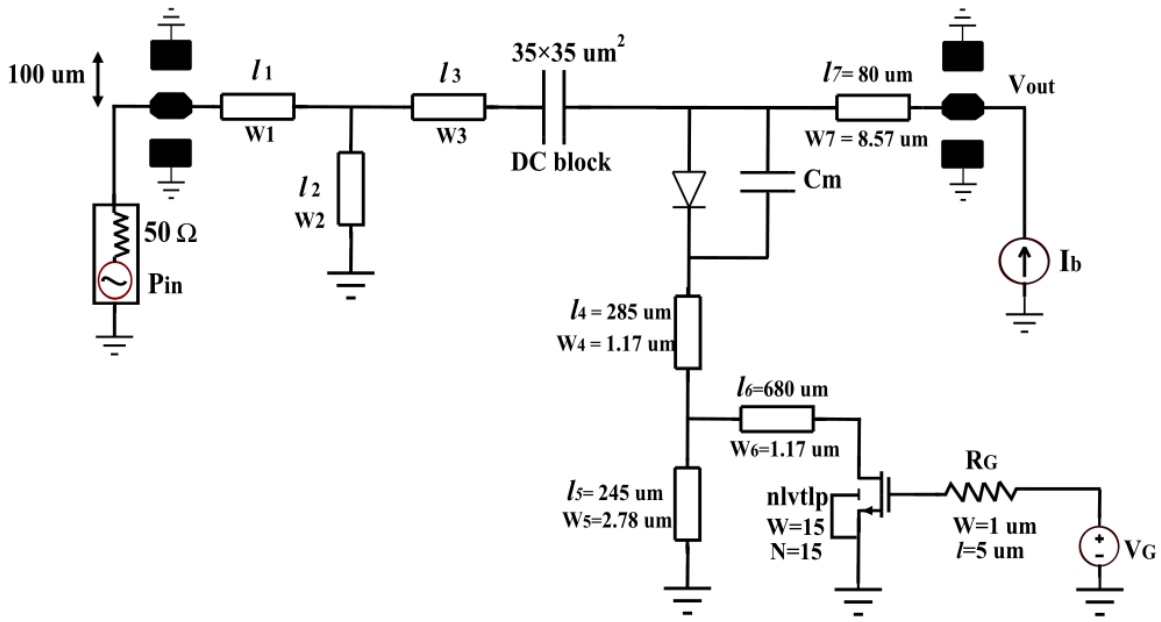


Figure 3.10 The adjustable detector circuit based on PN diode.

3.4.1 N-load circuit

The N-load circuit consists of NMOS transistor with stub network. This circuit is connected in series with the diode in order to absorb (thus attenuate) part of the input RF power. Attenuating the input power allows to maintain the linearity of the diode at higher level of input power (P_{in}>-30 dBm). However, it decreases the sensitivity value.

Hence, the attenuating factor has to be carefully chosen making the best trade-off between sensitivity and linearity. The resistor R_G is a poly silicon resistor of 30 kΩ, it avoids the RF signal leakage to the DC source V_G.

Using Cadence virtuoso software (which provides the design kit of the technology), the elements of the N-load circuit are sized in order to provide the following characteristics:

- the N-load circuit exhibits about 40 Ω as real impedance in series ($real(Z_{load})$) in the frequency bandwidth (35 – 50) GHz, thus, it absorbs a part of input power P_{in}.
- It exhibits an inductive series impedance ($imag(Z_{load}) > 0$) in the frequency bandwidth (35 – 50) GHz, this helps to match the detector by compensating the capacitive effect of the diode.
- It exhibits a short circuit ($Z_{load} = 0$) at DC (via stubs l_4, l_5), thus, no DC power is consumed.
- The NMOS transistor is driven through its gate by a certain DC voltage (V_G), thus no DC power is consumed in this transistor. When the voltage V_G is adjusted, the values of the impedance Z_{load} is varied over the frequency, and so the attenuation factor. Therefore, the flatness of the sensitivity curve over the frequency can be adjusted by controlling the value of V_G. This will be more clarified in the paragraph 3.4.5 (B).

3.4.2 PN diode

The function of the PN diode is to rectify (detect) the input RF power. As we mentioned before, the diode utilized in our design is under development, and does not exist in the design kit of the technology. Therefore, we will use the extracted model and the parameters from paragraph 3.3 in order to represent the diode in the detector simulation. The diodes are biased by a current source (instead of voltage source) to take the benefit of the small variation in the diode model parameters with the temperature (paragraph 3.5).

3.4.3 Matching network

The matching network is represented by the subs l_1, l_2, l_3 (micro-strip transmission lines) and the DC block capacitance (110 fF with the dimensions 35×35 µm MOM capacitance). Adding this network is important to ensure that the maximum RF power is absorbed by the detector, meanwhile avoiding standing waves. In order to design the matching network, the complete detector circuit is simulated in Cadence virtuoso (where the diodes are represented by their extracted small signal models, the N-load circuit is already designed in Cadence). Then, the elements sizes of the matching network circuit are adjusted (tuned) using Cadence virtuoso in order to obtain the desired $|S_{11}|$ values.

It is worth to mention that, the matching networks are designed for wide range of biasing current value (1 nA - 100 µA) enabling the tuning of detectors parameters.
Since the size of the diode L2N5 is ten times larger than the diode L1N1, the stubs dimensions in the matching networks are different, those dimensions are reported in table 3.4.

Diode	l_1 (µm)	l_2 (µm)	l_3 (µm)	w_1 (µm)	w_2 (µm)	w_3 (µm)
L1N1	80	230	180	8.57	1.17	1.17
L2N5	80	220	200	8.57	1.17	1.17

Table 3.4 The stubs dimensions in the matching networks for the detectors L1N1 and L2N5.

3.4.4 Detection simulation in ADS

The large signal model of the diode is required for detection simulation. This model is obtained by replacing the R_j (active part) and C_j by dynamic elements exhibiting their nonlinear behaviors as shown in figure 3.11.
The Symbolically Defined Devices (SDD) box available in ADS software is suitable to represent this behavior for the active part (R_j). Therefore, ADS is chosen (instead of Cadence virtuoso) to execute the detection simulation. The SDD box is defined by the equation 3.1 where the extracted *n* and I_S values are provided from table 3.3.

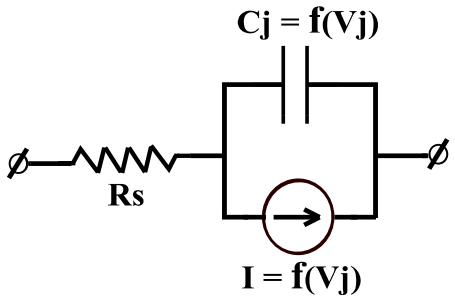


Figure 3.11 The large signal intrinsic model of diode, V_j is the voltage across the junction.

The 50 fF capacitor C_m (20×20 µm MOM capacitance) is connected in parallel with the diode in order to help to match the detector for wider range of biasing currents I_b. This capacitance is assumed to be dominant compared to the variation of the C_j values with input RF power. This assumption will be validated by comparing the simulated to the measured results. Based on the assumption above, the extracted C_j values (from the linear model tables 3.1 and 3.2) are used in the large signal model of the diodes.

The complete circuits of the detectors are simulated in ADS as shown in figure 3.12, where the matching networks and N-load circuit are represented by their extracted equivalent circuits from Cadence virtuoso; the diodes are represented by their large signal models, the RF pads are represented by their equivalent capacitance (25 fF) in parallel with resistance of 1 kΩ representing the dielectric losses at high frequencies.

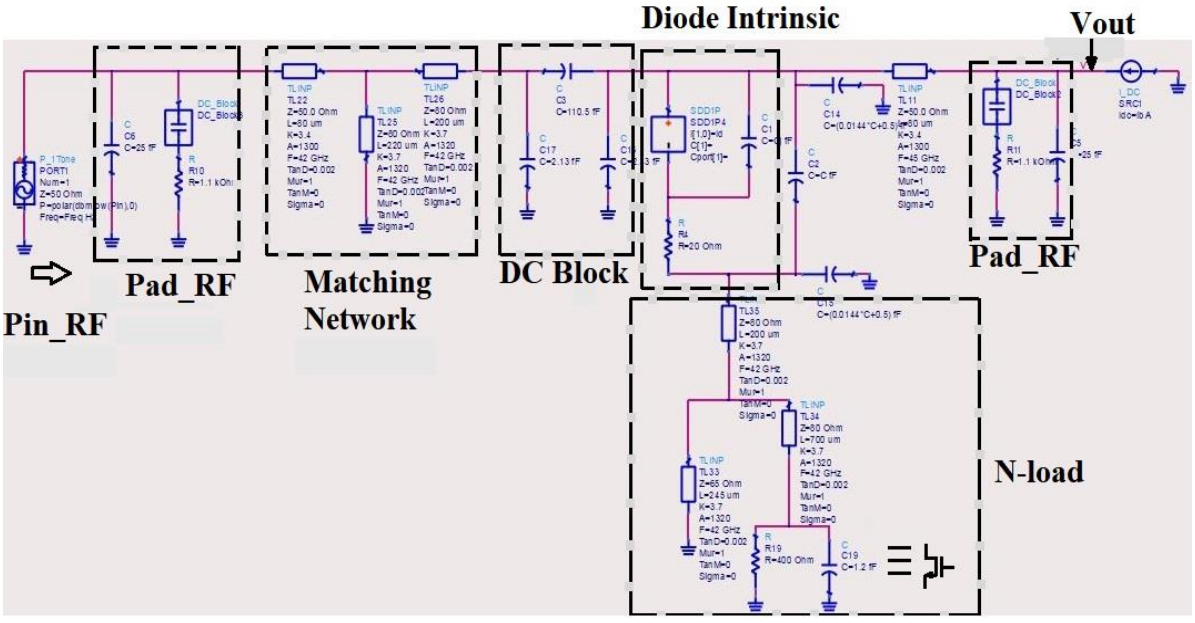


Figure 3.12 The detector schematic simulated in ADS.

As we can see in figure 3.12, the stubs are represented by transmission lines (TLINP), where their characteristic impedances, physical lengths, relative permittivity ε_r, insertion losses and tangent losses are provided. The DC block and C_m capacitors are represented by their body capacitance and two parallel parasitic capacitances. The transistor NMOS is represented by its R_{DS} in parallel with C_{DS} corresponding to two biasing voltages V_G (0.53 V and 0.51 V) for the detectors L1N1 and L2N5 respectively. Finally, the RF pads are represented by their capacitive effect (25 fF) in parallel with resistor of 1 kΩ representing the dielectric loss at high frequencies.

Harmonic balance simulation is used to simulate the output DC voltage (V_{out}) when the input RF power is applied. In addition, matching the detectors for large signal input power (up to -10 dBm) is also verified using large signal S-parameter simulation (LSSP).

3.4.5 Measurement results

The layout of the detectors is shown in figure 3.13, the total area of the detector is 0.17 mm^2 without the pads.

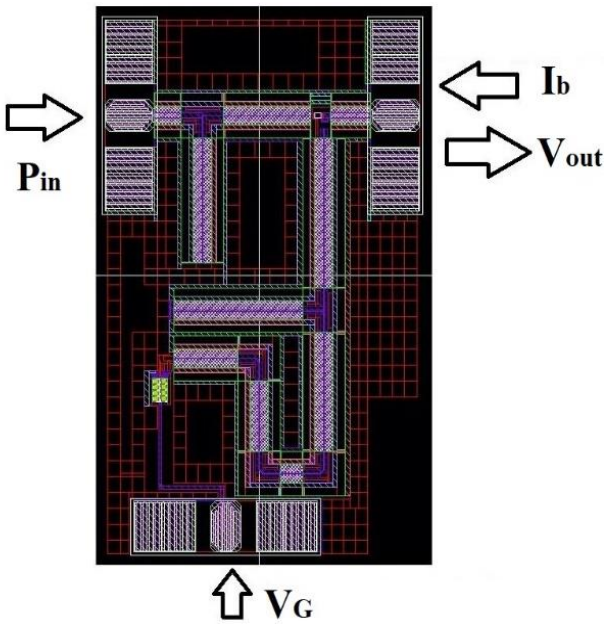


Figure 3.13 The layout of the detectors L1N1 and L2N5.

A. Measurement of the reflection coefficient

Figures 3.14 and 3.15 show the measured and simulated S_{11} curves of the detectors L1N1 and L2N5 respectively. These curves are shown for three values of biasing current I_b. It can be noticed that the detectors L1N1 and L2N5 are matched in the frequency bands (35-50) GHz and (35-48) GHz respectively, where $|S_{11}| \leq$ -8 dB. Some discrepancies (simulation - measurements) are also noticed. In order to investigate the source of these discrepancies, the simulation models of the capacitor (DC block) and the transistor NMOS were verified and validated (by comparing them to the measurements up to 220 GHz). As a conclusion, these discrepancies can be attributed to the effects of: (i) The T structures in the layout design, (ii) the standing waves which can be occurred in the output line (l_7).

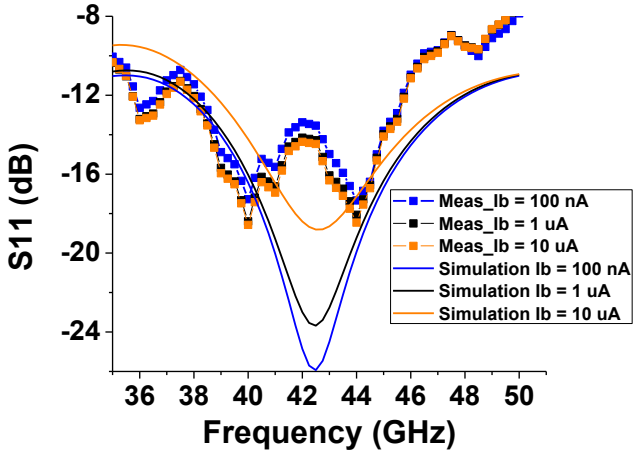


Figure 3.14 The measured and simulated S_{11} for L1N1 detector at P_{in}=-12 dBm.

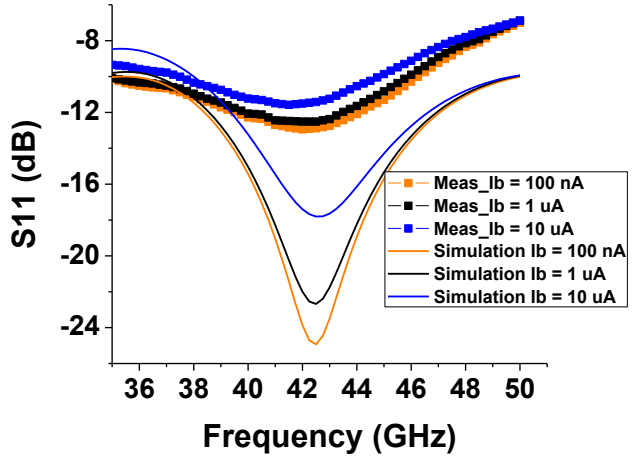
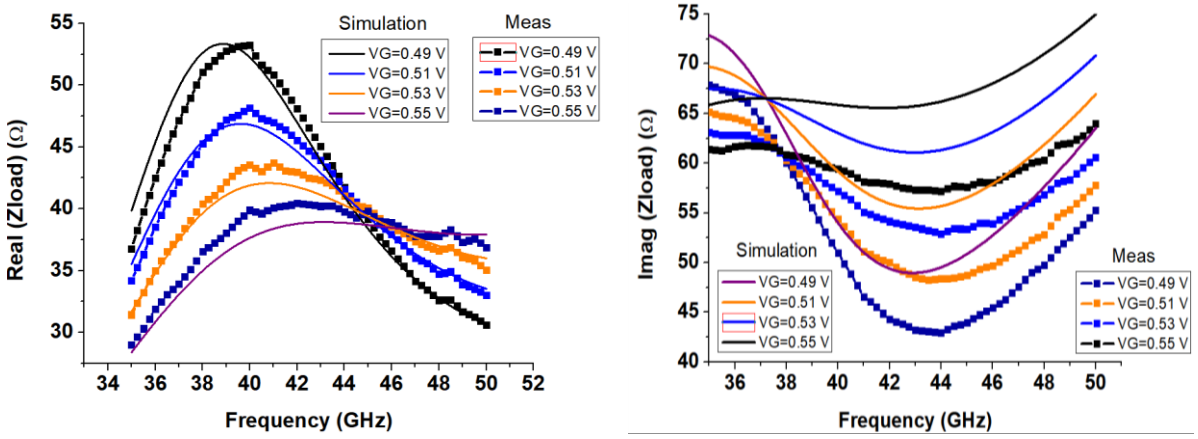


Figure 3.15 The measured and simulated S_{11} for L2N5 detector at P_{in}=-12 dBm.

B. Measurement of the N-load circuit

The S_{11} parameters of the N-load circuit stand alone are extracted (one port configuration) for several values of voltage V_G, then, they are transferred into Z_{11} parameters. The extracted Z_{11} parameters represent the series impedance of the N-load circuit Z_{load} as shown in figure 3.16.



(a) (b)

Figure 3.16 The measured / simulated real and imaginary parts of N-load impedance Z_{load} for several V_G values.

Based on the figure 3.16 (b), the N-load circuit exhibits an inductive impedance ($imag\ (Z_{load}) > 0$) for the whole bandwidth of interest helping to match the detector. In the frequency band (40 - 45) GHz, the slope rate (the decrease) of the N-load impedance over the frequency can be adjusted by controlling the voltage V_G, hence it can adjust the flatness of the sensitivity curve over the frequency band.

C. Measurement of voltage sensitivity γ

The voltage sensitivity of a diode is already defined in the paragraph 2.3.3. Similarly, the voltage sensitivity of detector is given as :

$$\gamma = \frac{V_{OFF} - V_{ON}}{P_{in}} \qquad (V/W) \tag{3.8}$$

In the equation 3.8, the (V_{OFF}) and (V_{ON}) are the DC output voltages of detector when the input RF power (P_{in}) is in the states (OFF) and (ON) respectively.

The block diagram of the setup used in order to extract the voltage sensitivity is shown in figure 3.17. The detector is probed using coplanar Infinity probe i67 [66] at the input (RF side), and a high impedance Cascade (form-factor)-Microtech probe FPX-100X [67] at the output (DC side). A KEITHLEY-2440 DC source meter is used as a current source to bias the detector by a DC current I_b.

In order to measure the DC output voltage (V_{out}), a DC voltmeter Agilent 34461A is connected in parallel with the source meter providing more accurate reading voltage

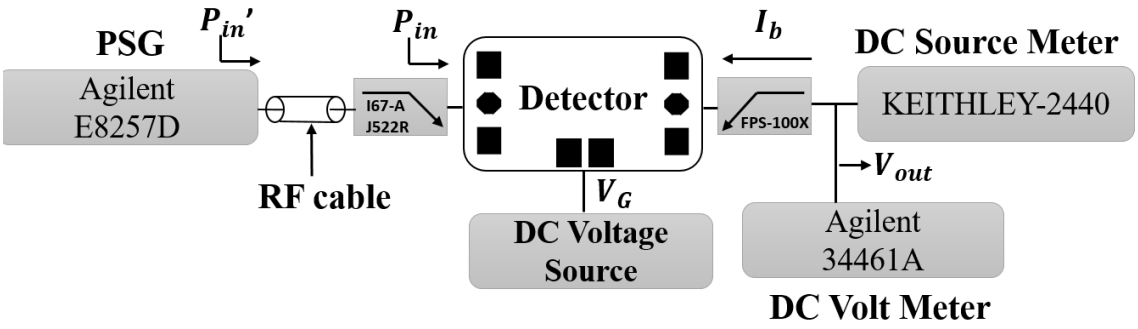


Figure 3.17 Test bench block diagram to extract the voltage sensitivity.

than the source meter. The internal impedance of each of the source meter and voltmeter is about 10 GΩ. DC voltage source is used to drive the N-load circuit providing the voltage V_G through DC needles. The RF power is injected using PSG (Performance Source Generator E8257D) in the frequency band (35-50) GHz, where the input RF power P_{in} is defined at the input pad plane as shown in figure 3.17. In order to shift the reference power plane from P_{in}' to P_{in} , the losses of the RF cable and input probe are subtracted from the PSG injected power. To extract the voltage sensitivty values, the (V_{OFF}) and (V_{ON}) are measured and then applied in the equation 3.8.

Figures 3.18 and 3.19 show the measured and simulated sensitivty curves versus the frequency for L1N1 and L2N5 detectors. The biasing voltages V_G are adjusted to be (0.53 and 0.51) V for the detectors L1N1 and L2N5 respectively, those voltage values allow obtaining flat sensitivity curves over the frequency band of interest.

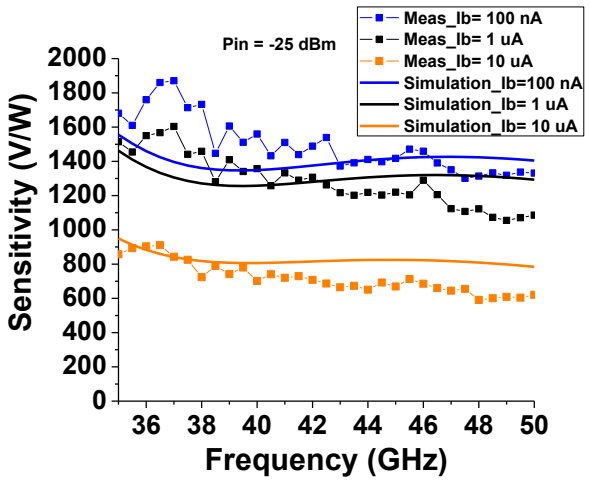


Figure 3.18 The measured and simulated voltage sensitivity curves vs frequency for L1N1 detector at P_{in}= -25 dBm.

From the obtained results, it can be concluded that:

- The sensitivity curves are relativly flat over the frequency band of interest.
- A good agrement is obtaind between the simulation and measurement results.
- The higher the biasing current, the lower is the sensitivity value.

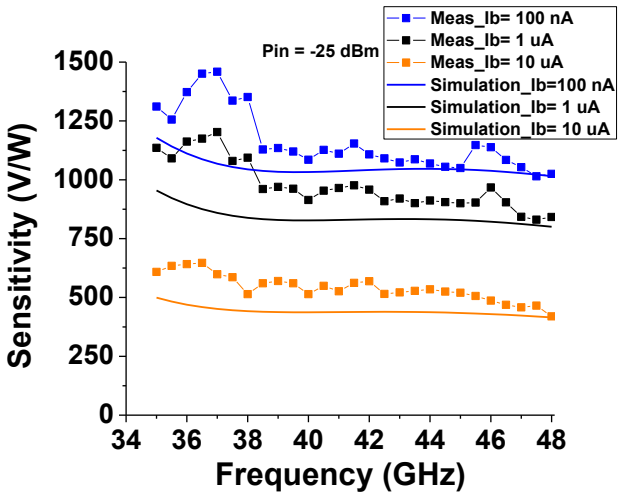


Figure 3.19 The measured and simulated voltage sensitivity curves vs frequency for L2N5 detector at P_{in}= -25 dBm.

Figures 3.20 and 3.21 show the measured and simulated sensitivty curves versus the input power for L1N1 and L2N5 detectors at 42 GHz. From the obtained results, it can be concluded that:

- The lower the sensitivity value, the higher is the compersion point P_{in_max}, where this point is obtained for 10% degradation of the sensitivity value in the linear zone. The P_{in_max} points corresponding to biassing currents (0.1, 1, 10) µA occur at (-20, -18.7, -12) dBm for L1N1, and (-18, -16, -8) dBm for L2N5 respectivily.
- A good agrement is obtained between the simulation and measurement results.

The DC power is only consumed in the diodes, thus the power consumptions (P_D) of the detectors are calculated (for each biasing current) using the I-V characteristics as :

$$P_D = V_{OFF} \times I_b \qquad \text{(W)} \tag{3.9}$$

Since the N-load impedance (Z_{load}) is null at low frequencies, the video resistance values of the detectors R_v are equal to the R_j values of the diodes. Thus, they can be directly concluded using tables 3.1 and 3.2.

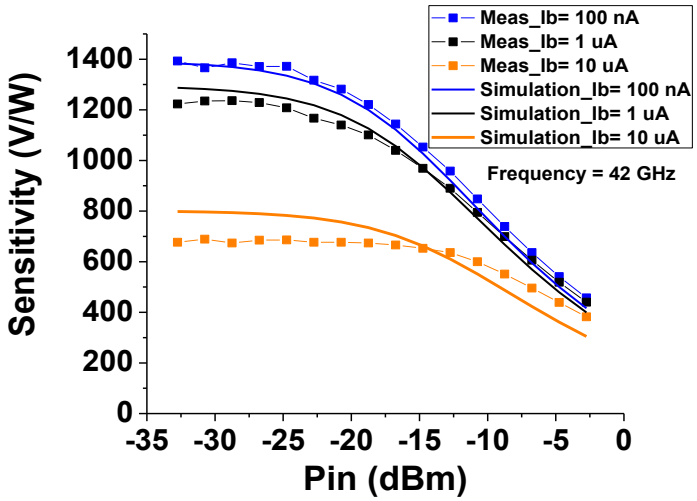


Figure 3.20 The measured and simulated voltage sensitivity curves vs input power for L1N1 detector at 42 GHz.

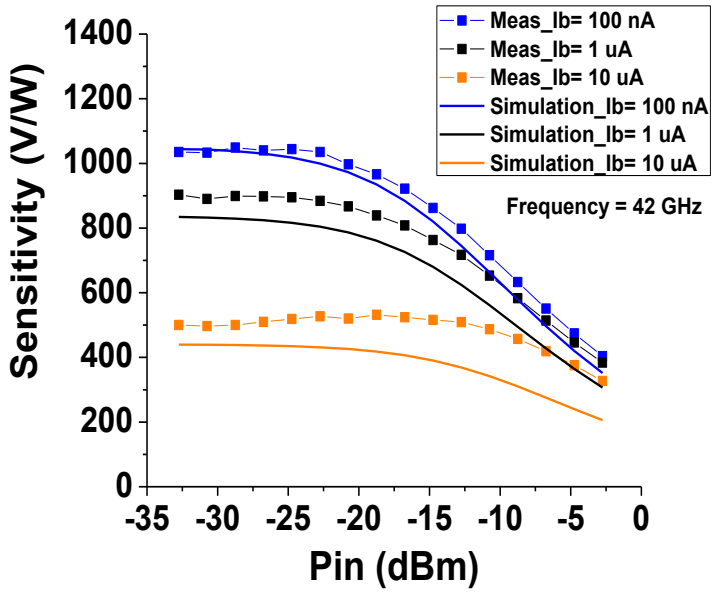


Figure 3.21 The measured and simulated voltage sensitivity curves vs input power for L2N5 detector at 42 GHz.

The tables 3.5 and 3.6 summarize the extracted parameters for the detectors L1N1 and L2N5. It can be concluded that a targeted sensitivity value with lower power consumption can be obtained using larger diode, as the cases of (detector L1N1 biased with I_b= 1 µA) and (detector L2N5 biased with I_b= 0.1 µA). However, the larger diode will exhibit higher video resistance (R_v= 25 kΩ and 250 kΩ for L1N1and L2N5 respectively) reducing the video bandwidth (based on equation 2.17).

The S_{11} measurements show that the detectors are matched over a wide range of current I_b (1 nA - 100 µA), providing simulated sensitivity values (10 - 1500) V/W for the detector L1N1. However, those values were not measured due to the accuracy

I_b (µA)	γ (V/W)	P_{max} (dBm)	R_v (kΩ)	P_D (µW)
0.1	1400	-20	250	0.07
1	1200	-19	25	0.77
10	700	-12	2.5	8.3

Table 3.5 The extracted parameters of the detectors L1N1 for three values of biasing current.

I_b (µA)	γ (V/W)	P_{max} (dBm)	R_v (kΩ)	P_D (µW)
0.1	1150	-18	250	0.06
1	900	-16	25	0.69
10	500	-8	2.5	7.6

Table 3.6 The extracted parameters of the detectors L2N5 for three values of biasing current.

limitation of the source meter and volt meter, hence, the I_b values (0.1, 1, 10) µA were chosen in order to produce measurable sensitivity values. The figure 3.22 shows the S_{11} measurements corresponding to the minimum and maximum biasing currents for L1N1 detector, proving the matching conditions whatever the current is in the range (1 nA, 100 µA).

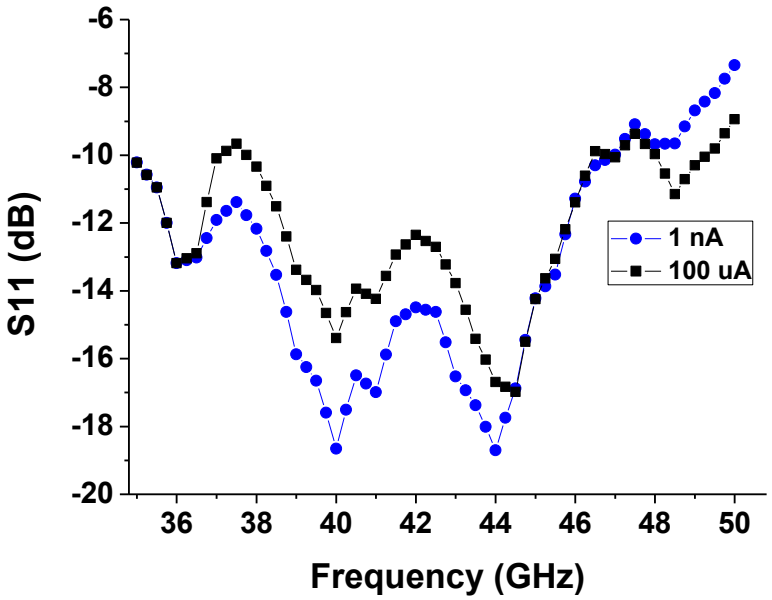


Figure 3.22 The S_{11} measurements for L1N1 detector at 1 nA and 100 µA biasing currents.

3.4.6 Theoretical analysis

Based on the mathematical development presented in Annex 1, the intrinsic sensitivity of diode for low level of input RF power (P_{in} is smaller than the P_{in_max} compression point) can be given in the following equation:

$$\gamma_{Intrinsic} \approx \frac{R_j.X}{2.n\ .V_T} \tag{3.10}$$

X is the ratio between the input injected power and the power absorbed in the junction. Based on the equation (3.10), the sensitivity value can be increased by:

- Increasing the factor X, i.e. the power absorbed in the diode junction.
- Increasing the junction resistance R_j.
- Operating the detector at lower temperature, i.e. keeping the thermal voltage V_T as low as possible.
- Using diode which has ideality factor $n \approx 1$.

The variations of the sensitivity value with the biasing current I_b and diode size are explained based on the equation (3.10) in the following:

- When the diode is biased with higher value of DC current I_b, the R_j value becomes lower, and so lower sensitivity value is produced.
- For the same biasing current I_b, larger diode sizes exhibit higher C_j values, meanwhile, the R_j values do not change (tables 3.1 and 3.2). Therefore, lower power is absorbed in the diode, and lower sensitivity value is produced.

3.5 The thermal behavior of the PN diode

When the ambient temperature is varied, the diode parameters are affected due to their temperature dependency. Hence, the detector performance is deviated, and error of measurements is produced (comparing to the room temperature performance).

In this context, we present a study of the deviation with the temperature of:

- The model of the PN diode.
- The sensitivity value of the same diode (L1N1 stand-alone) at 40 and 45 GHz.

3.5.1 The deviation of the PN model with temperature

Extracting the thermal model of the diode allows simulating the detector for several temperatures, and so, a detector with temperature compensation can be designed.

The same test structure in figure 3.2 (diode L1N1) is used in order to extract the thermal model of the diode and the sensitivity variation with the temperature.

Using the same extraction method in paragraph 3.3, the values of the R_s , R_j , I_s, n and C_j are extracted for three temperatures (25, 60, 100)°C. In addition, the built in potential V_{bi} is extracted for those temperatures. These values are extracted using the I-V curves by making the intercept of the linear zone with the voltage axis [65] as illustrated in figure 3.23.

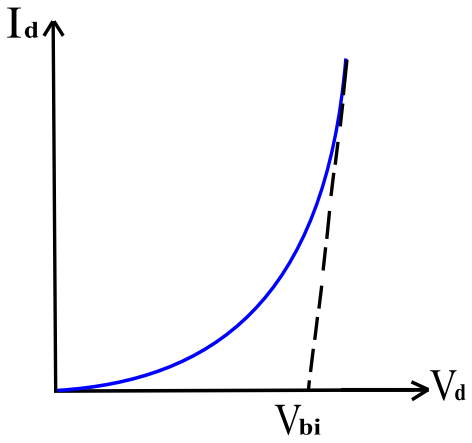


Figure 3.23 The extraction of V_{bi}.

Based on the measurements, the I-V characteristics for three temperatures (25, 60, 100)°C are shown in figure 3.24. The extracted values of the saturation current I_S and the built-in potential V_{bi} are reported in table 3.7. When the temperature increases, the saturation current value is increased, whereas the built-in potential value is decreased. This behavior is well known for diode [68].

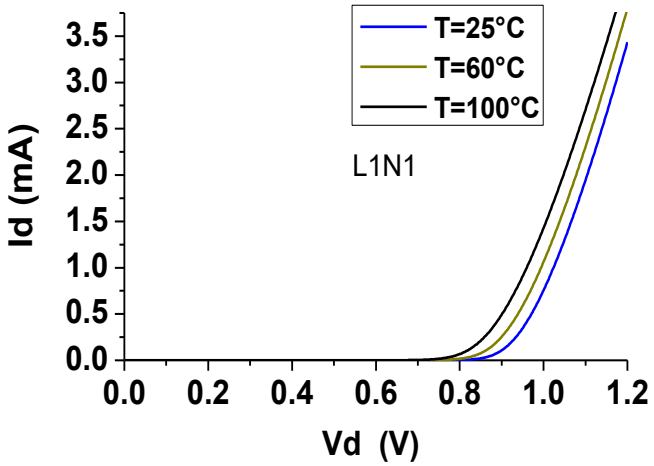


Figure 3.24 The measured I-V curves corresponding to three temperatures for the diode L1N1.

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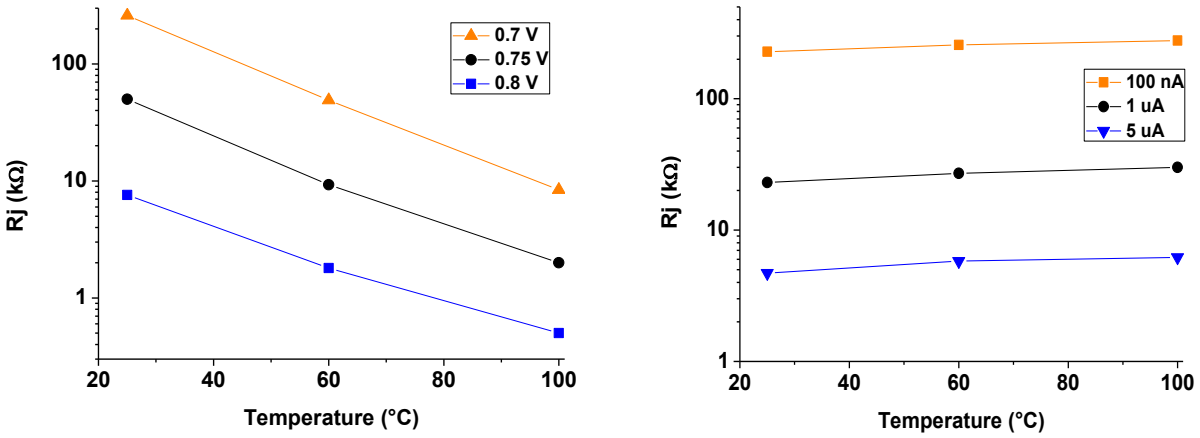
T (°C)	I_s (A)	V_{bi} (V)
25	5E-19	1
60	3E-17	0.96
100	2E-15	0.92

Table 3.7 The extracted saturation current and built-in potential for several temperatures.

The variation of the R_j value with the temperature is plotted in figure 3.25, this variation is also plotted for several biasing voltage and current values.

It can be noticed that the R_j value decreases when the biasing value (current or voltage) is increased. In addition, a significant decrease of R_j value with the temperature is obtained when the diode is biased by a voltage source ($\Delta R_j/\Delta T$= 3.35 Ω/°C). On the contrary, biasing the diode by a current source guaranties a very small variation of R_j value with the temperature ($\Delta R_j/\Delta T$= 0.65 Ω/°C). All these behaviors can be explained using the equation 2.15 from chapter 2:

$$R_j = \frac{n.V_T}{I_b + I_S} \approx \frac{n.V_T}{I_b} = \frac{n.V_T}{I_S.\exp(V_b / n.V_T)} \qquad \text{for} \quad I_b >> I_S$$



(a) (b)

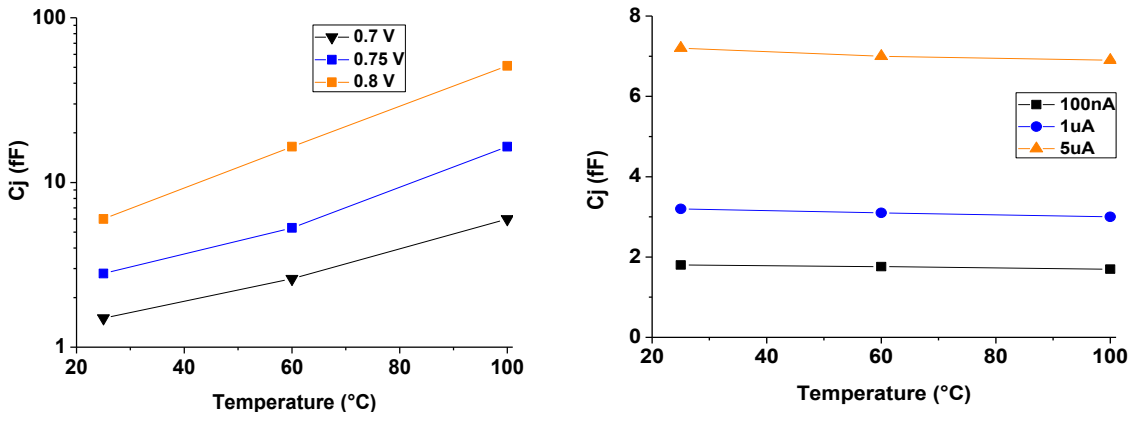
Figure 3.25 The variation of R_j value with temperature for: (a) different biasing voltage values, (b) different biasing current values.

When the diode is biased by a current source, the denominator is constant over the temperature (I_b), thus, a small increase in R_j value is obtained from the V_T increase. However, when the diode is biased by voltage source, a significant increase of the diode current (I_b) is obtained over the temperature corresponding to the same biasing voltage (as shown in figure 3.24). Therefore, a significant decrease of R_j value is obtained with the temperature.

The variation of the C_j value with temperature is extracted and plotted in figure 3.26, this variation is also extracted for several biasing voltage and current values. A significant increase of C_j value with the temperature is obtained when the diode is biased by a voltage source. On the contrary, biasing the diode by a current source guaranties very small variation in C_j value with the temperature. All these behaviors can be explained using the junction capacitance formula [69]:

$$C_j = A_j \sqrt{\frac{N_D.N_A.q..\varepsilon_s}{2(N_A)(V_{bi}-V_b)+N_D}} = A_j \sqrt{\frac{N_D.N_A.q..\varepsilon_s}{2(N_A)(\Delta V)+N_D}} \qquad (3.11)$$

Where N_D, N_A are the concentration of donor and acceptor atoms respectively, ε_s is the dielectric constant of the semiconductor, q is the electron charge, and A_j is the junction

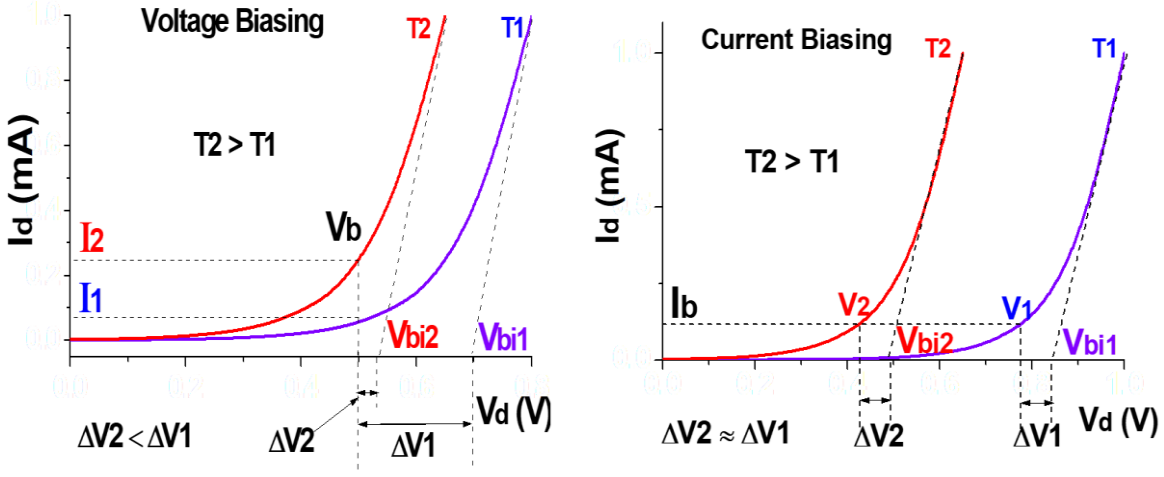


(a) (b)

Figure 3.26 The variation of C_j with temperature for: (a) different biasing voltage values (b) different biasing current values.

area. The equation 3.11 considers the depletion capacitance, whereas the diffusion capacitance is neglected because the diode is biased in weak forward regime.

When the diode is biased by voltage source (V_b), a significant decrease in (ΔV) is obtained with temperature as illustrated in figure 3.27 (a). Therefore, a significant increase in C_j value is obtained with the temperature. However, when the diode is biased by a current source, the (ΔV) is nearly constant with the temperature (as in figure 3.27 (b)), thus, very small variation in C_j value is obtained.



(a) (b)

Figure 3.27 The variation of ΔV for two temperatures in: (a) voltage biasing (b) current biasing.

The R_s and n values were extracted with the temperature; no variation is obtained above 100°C. This can be explained by the fact that the temperature 100°C is not high enough to change the conductivity of the *N*-well layer, where n=1.05 and $R_s = 60\Omega$.

From the study presented above, it can be concluded that the diode model becomes less sensitive to temperature variation when it is biased by a current source. On the other hand, the model and the cutoff frequency of voltage biased diode are strong temperature dependent.

The intrinsic cutoff frequency is calculated using the equation 3.12, and its variation with temperature is shown in figure 3.28. These results also show the capability of this diode to work at submillimeter wave applications.

$$f_{cutoff} = \frac{1}{2\pi . R_S . C_j} \tag{3.12}$$

It is worth to mention that, the tunable detector in the paragraph 3.4 was designed to be biased by a current source to take the benefit of the small deviation in the diode model parameters with the temperature.

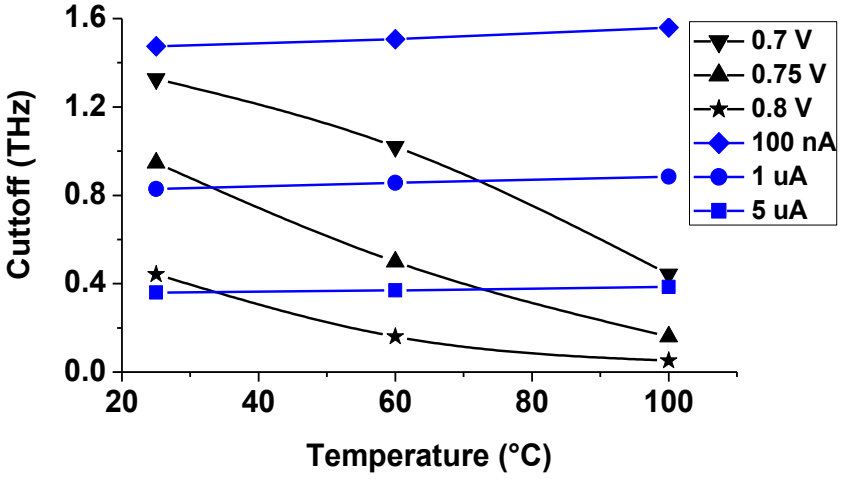


Figure 3.28 The variation of intrinsic cutoff frequency with temperature for different voltage and current biasing values.

3.5.2 The deviation of the sensitivity with temperature

The same diode (L1N1 stand-alone figure 3.2) is used in order to extract the diode voltage sensitivity (γ) over the temperature. The block diagram of the setup used in order to establish this extraction is shown in figure 3.29.

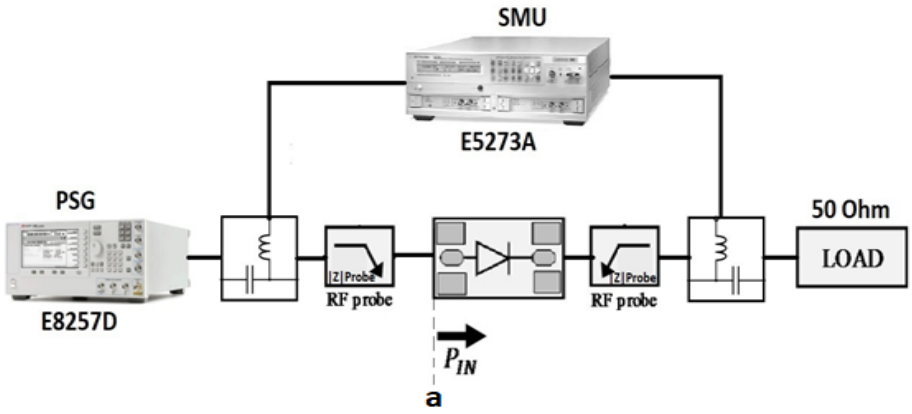


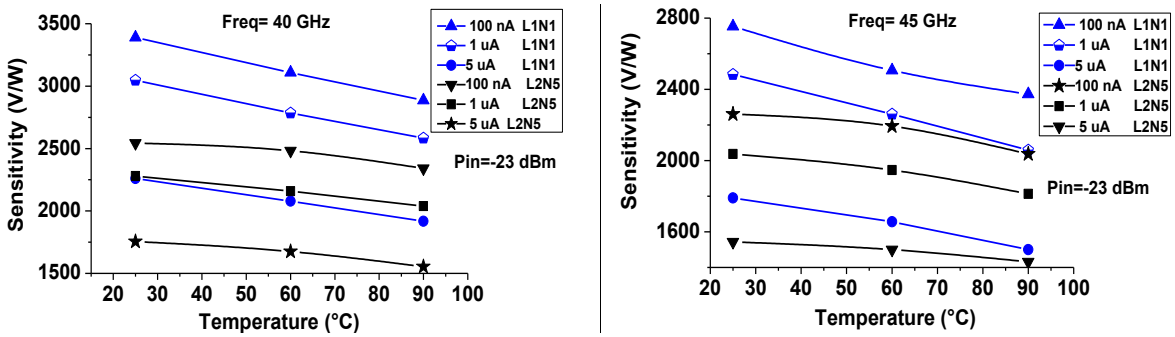
Figure 3.29 Test bench block diagram to extract the voltage sensitivity of the diode L1N1.

The diode is probed using |Z| probes with a coplanar access [70]. A Source/Monitor Unit (SMU) E5273A is used to bias the diode in forward regime by applying DC current I_b (current source), and then the corresponding DC voltage is measured (V_{OFF} or V_{ON}). The internal impedance of the SMU is about 10 GΩ which is much more higher than the video resistance R_j. The RF power is injected using the PSG (Performance Source Generator E8257D) at two frequency values 40 and 45 GHz. Two bias tees are used to separate the DC and RF signal at the input and output of the test structure. The external mmW load of 50 Ω is connected at the output of the test structure to reduce the standing wave on the right probe, and also, to absorb part of the injected RF power allowing to maintain the linearity of the diode at higher level of input power (P_{in}>-30 dBm).

The input power P_{in} is defined at the input pad plane (plane 'a') as shown in figure 3.29. The delivered power to the input of the left probe was measured using power meter, and then the losses of the probe are added in order to shift the reference power plan from the PSG to the plan 'a' by using scalar power de- embedding.

To extract the voltage sensitivty values, the (V_{OFF}) and (V_{ON}) values are measured and then applied in the equation 2.4 from chapter 2.

The voltage sensitivity of the integrated diode is extracted for: (i) two diode sizes (ii) three values of biasing current (iv) three temperatures (v) two frequency values 40 and 45 GHz. These measurements are shown in figure 3.30. The aim of varying all those parameters is to study their effects on the voltage sensitivity.



(a) (b)

Figure 3.30 The extracted voltage sensitivity in function of temperature for several biasing current values, two diode sizes, at -23 dBm: (a) 40 GHz, (b) 45 GHz.

Based on figure 3.30, several conclusions can be mentioned:

- When the temperature increases, the voltage sensitivity value is decreased for all the conditions. This is because that the active part (R_j) becomes less dominant (the increase ratio $\Delta R_j/\Delta T$ is more significant comparing to $\Delta C_j/\Delta T$), hence less power is absorbed in the diode and smaller sensitivity value is produced. This behavior is verified using the detection simulation in ADS (shown in the next paragraph).
- When the frequency of the input power increases, the sensitivity values are decreased. This is due to the effects of the parasitic elements (C_j, C_{sub}, …) which become more dominant at higher frequencies, reducing the power absorbed in the diode. The matching conditions can also affect the sensitivity values over the frequency. This is not the case of this structure, since the $|S_{11}|$ is nearly the same for 40 and 45 GHz.

3.5.3 Simulation / measurement of sensitivity with temperature

The test structure model of the diode L1N1 is simulated in the ADS software (similar

to the simulation explained in paragraph 3.4.4), the schematic used in this simulation is shown in figure 3.31. The S-parameters of the output probe is represented by the S2P box in the simulation. Harmonic balance simulation is used to simulate the output DC voltages (V_{OFF} and V_{ON}), these voltage values are then applied in the equation 2.4 in order to extract the sensitivity values.

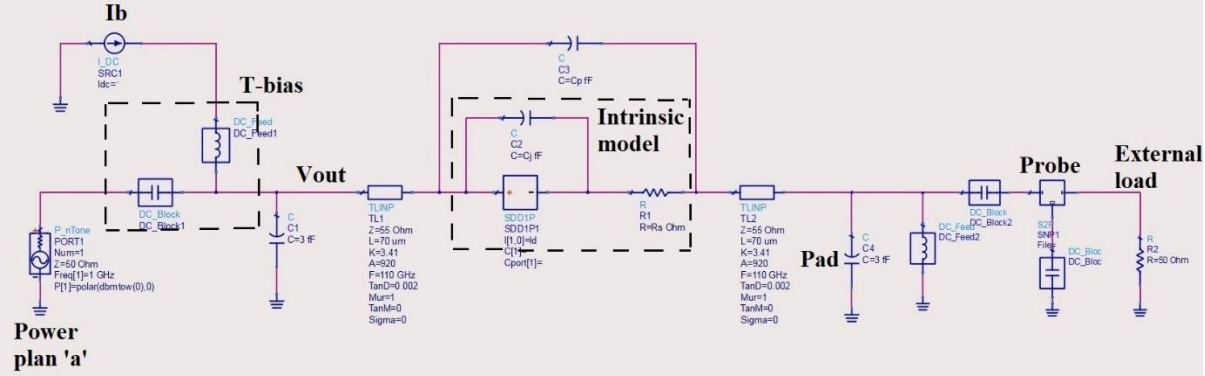


Figure 3.31 The test structure schematic simulated in ADS.

The variation in temperature is represented in the simulation by providing the corresponding values of I_s, V_T in the SDD box, and the C_j values for the junction capacitance.

Figure 3.32 shows the simulated and measured voltage sensitivity for several temperatures, at 1 µA of biasing current, and frequency of 40 GHz. A good agreement

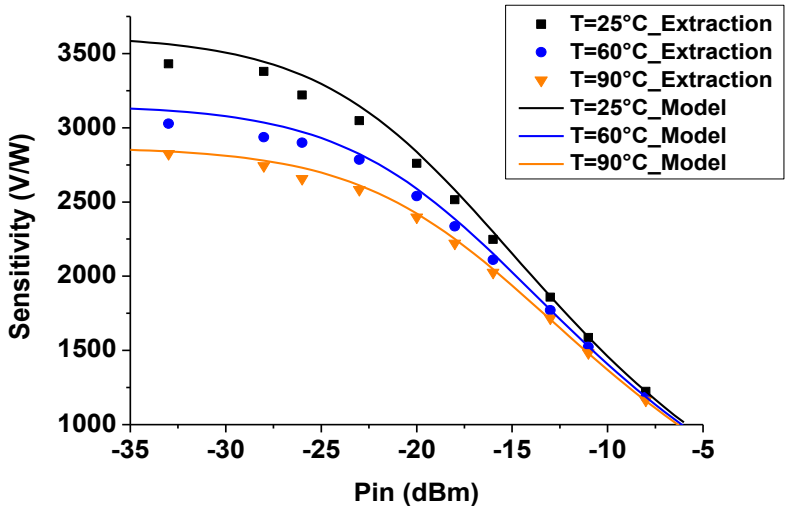


Figure 3.32 The extracted and simulated voltage sensitivity in function of input power for several temperatures at 40 GHz, 1µA biasing current using the diode L1N1.

is obtained between the simulated and extracted voltage sensitivity curves. This fact validates the extracted model and the detection simulation in ADS. The voltage sensitivity value varies between (2800 –3600) V/W corresponding to variation of temperature range (25 - 90)°C.

3.6 State of the art

The performances of the tunable detectors designd in paragraph 3.4 are compared to other recent works in table 3.8, our designs performances are beyond the current state of the art exhibiting very low power consumption with relatively high sensitivity values.

Reference	Technology	Frequency (GHz)	Sensitivity (V/W)	P_D (µW)
[71]	65nm-CMOS (PN diodes)	4-6	3	700
[72]	Commercial mHEMT (Schottky)	50 – 70	500 at 60 GHz	0.7
[73]	250nm-BiCMOS (HBT)	7 -20	-	720
[74]	55nm-BiCMOS	50 - 66	1500	80
This work	55nm-BiCMOS PN diode	35-50 For L1N1	700 1200 1400	8.3 0.77 0.07
		35-48 For L2N5	500 900 1150	7.6 0.69 0.06

Table 3.8 Comparison with other published power detectors for frequencies < 110 GHz.

3.7 Conclusion

In this chapter, the extraction of the PN diode model was presented up to 110 GHz. The comparison between the extracted model and the measurements was made in order to validate this model.

The extracted model was employed to design two tunable power detectors in the frequency band (35 - 50) GHz, based on two diode sizes. Since the parameters of these detectors are tunable, they can be used in different 5G applications. These detectors performances are beyond the current state of the art by exhibiting relatively high sensitivity values with very low power consumption. Using larger diode helps providing a targeted sensitivity value with lower power consumption. Measuring the NEP of those detectors is planned as a future work in order to determine the minimum detectable power.

In the aim of realizing a temperature compensated detector, the thermal model of the diode was extracted, showing the deviations in the diode parameters with the temperature. It has been shown that biasing the detector with current source guaranties small variations in the model as compared to the voltage bias case.

Chapter 4

Zero Bias Detectors

Design & Characterization

4.1 Introduction

In this chapter, the design and characterization of several zero bias detectors will be presented in different frequency bands. This detector type is very practical for the 5G applications, where the power efficiency is required. In the frequency band (38 - 55) GHz, several detector topologies will be discussed based on different NMOS categories in order to compare their performances.

The design of detectors in (140 - 220) GHz and (0.45 - 0.6) THz frequency bands will be also presented. Since those detectors cover large frequency bands, the sensitivity value can significantly vary with the frequency. Therefore, the detectors are designed with frequency compensation; this characteristic makes them more practical since the sensitivity value is independent from the frequency. It is worth to mention that all the detectors in this chapter is designed (simulated) using Cadence virtuoso software, where the models of all circuits elements are provided in the design kit of the technology 55-nm BiCMOS from STMicroelectronics.

4.2 Zero bias detectors for 5G applications

Zero bias detector (ZBD) is a type of power detector that does not require DC biasing source. Therefore, this detector type can be the best solution for the applications that require power efficiency or passive operation. The elimination of the DC power source can often reduce the size, cost, and complexity of the circuitry.

ZBDs are utilized in many applications, such as RF identification (RFID), Internet of Things (IoT), and RF tagging taking the advantage of low cost and zero power consumption.

In the literature, many power detectors are proposed with no power consumption, however, they need DC voltage source (with zero current) for biasing the active elements [75], [76]. These detectors are not practical in a complete passive operation, where no DC source or batteries is provided. For example, many IoT devices do not have internal batteries because of the difficulties of sustain huge number of batteries [77], in addition the effect of self-discharge can empty the battery over time even the

circuit dose not consume power. In this context, we can distinguish the zero bias and zero consumption detectors, where the zero bias detectors offer the great advantage of operating in a complete passive system.

The PN diode used in the adjustable detector (paragraph 3.4) has a relatively high barrier potential (1V for the diode L1N1). Hence, it exhibits very high impedance if no biasing current (or voltage) is applied, and so, it cannot be used as a zero bias diode.

The 55-nm BiCMOS technology offers several categories of NMOS transistors (nlvtlp, nlvtgp, nhpalp) with low threshold voltage V_{th}. In the following, we briefly explain the main characteristics of these transistors:

- nlvtgp (we will name it as GP): It is considered as the standard NMOS transistor of the technology, it is usually used for general purpose high frequency applications.
- nhpalp (we will name it as HPA): This transistor was basically developed for analog applications by offering higher gain and linearity.
- nlvtlp (we will name it as LP): This transistor is suitable for low power and high frequency applications (i.e. millimeter and submillimeter waves applications) .

Since these transistors have low threshold voltages, they can be used in diode connected configuration as zero bias diodes. The diode connected transistor is obtained by connecting the drain to the gate as shown in figure 4.1 (a). This configuration creates a three-terminal device (a diode with a bulk access) out of a four-terminal transistor.

4.2.1 Overview of MOSFET operation regions

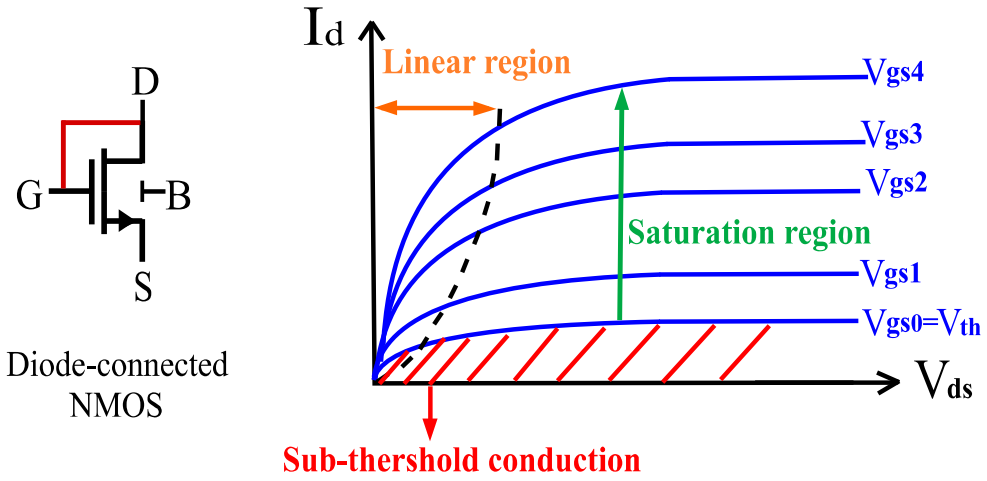
The MOSFET transistor can be operated in three main regions as shown in figure 4.1 (b). In the following, we mention the conditions and the drain current formula for each regime considering NMOS transistor :

- The NMOS operates in the linear region if: $V_{GS} > V_{th}$ & $V_{DS} < V_{GS} - V_{th}$

The drain current is given in the following equation [78]:

$$I_D = \mu_n . C_{OX} . \frac{w}{2L} [2(V_{GS} - V_{th}) V_{DS} - V_{DS}^2] \quad (4.1)$$

Where μ_n is the electron mobility, C_{OX} is the oxide capacitance, the w and L are the width and length of the NMOS channel respectively. In this regime, the transistor acts as an ohmic resistance.



(a) (b)

Figure 4.1 (a) Diode connected NMOS transistor, (b) the output characteristic of NMOS transistor showing different operation regions.

➢ The NMOS operates in the saturation region if: $V_{GS} > V_{th}$ & $V_{DS} \geq V_{GS} - V_{th}$

the drain current is given in the following equation [78]:

$$I_D = \mu_n . C_{OX} . \frac{w}{2L} (V_{GS} - V_{th})^2 \quad (4.2)$$

In this regime, the transistor acts as a current source, where the drain current I_D is nearly constant with the variation of V_{DS} .

➢ The NMOS operates in the sub-conduction mode if: $V_{GS} < V_{th}$

In this case, the drain current does not drop abruptly to zero. The MOSFET transistor is partially conducting for voltages below the threshold voltage. This effect is called subthreshold or weak inversion conduction. The drain current I_D can be given as in the following [79]:

$$I_D \propto \exp\left(\frac{V_{GS}-V_{th}}{n.V_T}\right).\left(1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (4.3)$$

Depending on the biasing conditions, the MOSFET in diode connected configuration can be operated either in sub-threshold or saturation regime. In our designs, we use the MOSFETs as zero bias diodes with low RF input power, thus, they are operated in sub-threshold mode. V_{GS} is equal to V_{DS} representing the voltage across the device (as V_d in a diode), whereas the drain current I_D represents the current passing through the device. In sub-threshold regime, the relation voltage-current of the drain is exponential (i.e. $R_{DS} \propto 1/g_m$) [79]. Therefore, it can be concluded that the behavior of the transistor in this case is similar to a diode.

4.2.2 Zero bias detector based on single NMOS

4.2.2.1 Detector design

Three zero bias detectors are designed based on three categories of NMOS transistor (LP, GP, HPA), we will name the detectors as the transistor name. The aim is to design several detectors using different NMOS categories in order to compare their performances. The working frequency bands of the circuits are located in (38 - 50) GHz allowing the detectors to cover several 5G bands [19].

The detectors circuits consist of three main blocks: (i) attenuator, (ii) diode connected NMOS, (iii) matching network.

The attenuator is used to maintain the linear response at higher levels of RF power; the NMOS transistor is used to rectify the RF input power; the matching network helps to absorb the maximum RF power in the detector.

In the case of zero bias detector, a series resistor (N+ silicided poly 50 Ω resistor) is used to attenuate the input RF power instead of the N-load circuit (which is used in the adjustable detector paragraph 3.4.1) for the following reasons:

- To reduce the detector area and simplify its circuitries.
- No need of saving DC power.
- The degradation of the voltage sensitivity over the bandwidth of interest (30 – 50) GHz in the NMOS transistor is less important than in the PN diode.

The schematics of the detectors GP, LP and HPA are shown in figures 4.2, 4.3 and 4.4 respectively. The matching network is represented by the DC block capacitor (of 110 fF) with the stubs (l1, l2, l3, l4).

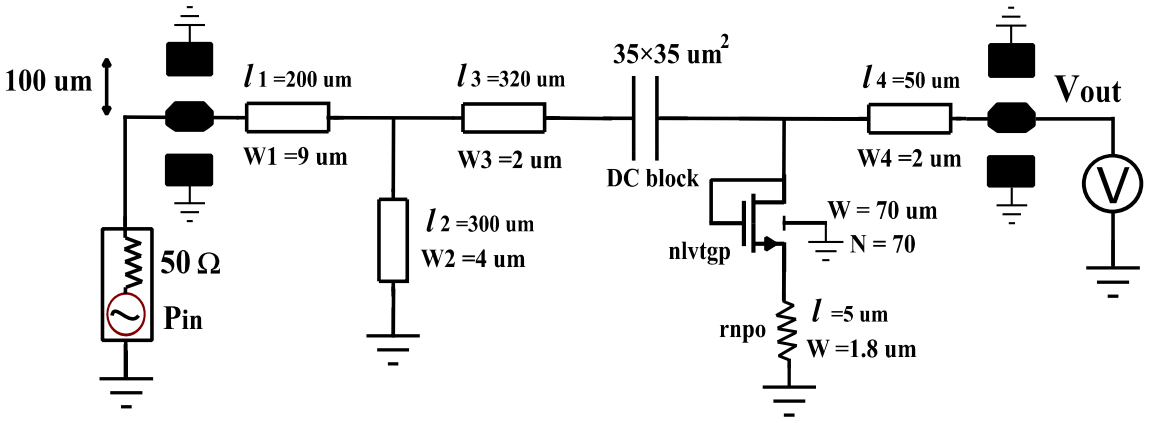


Figure 4.2 The schematic of the detector GP.

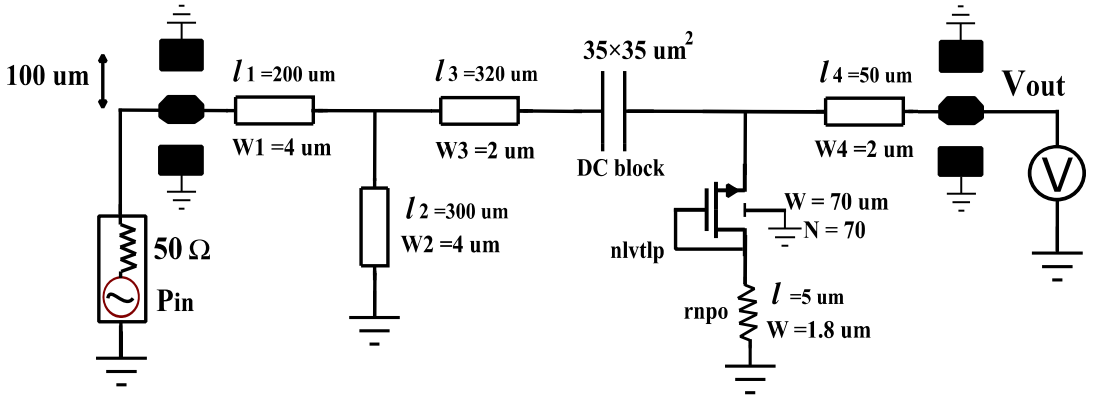


Figure 4.3 The schematic of the detector LP.

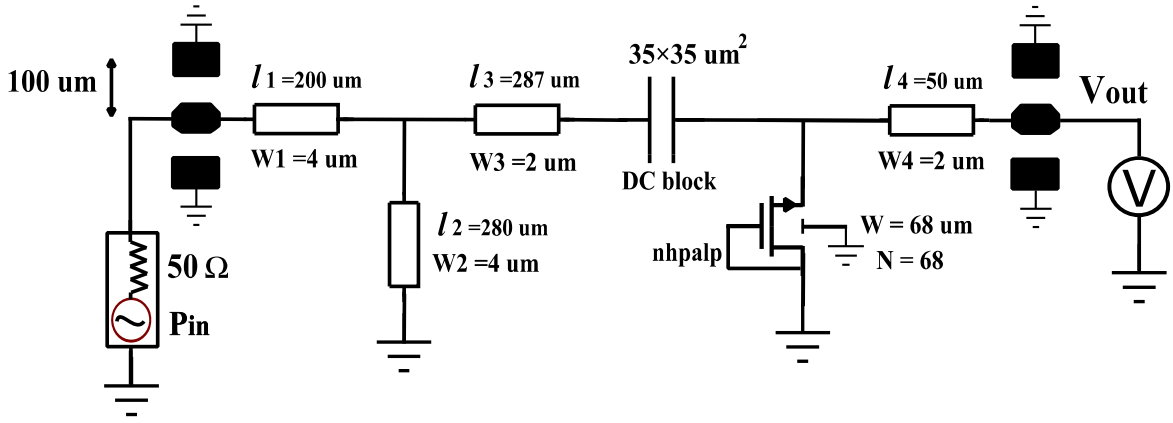
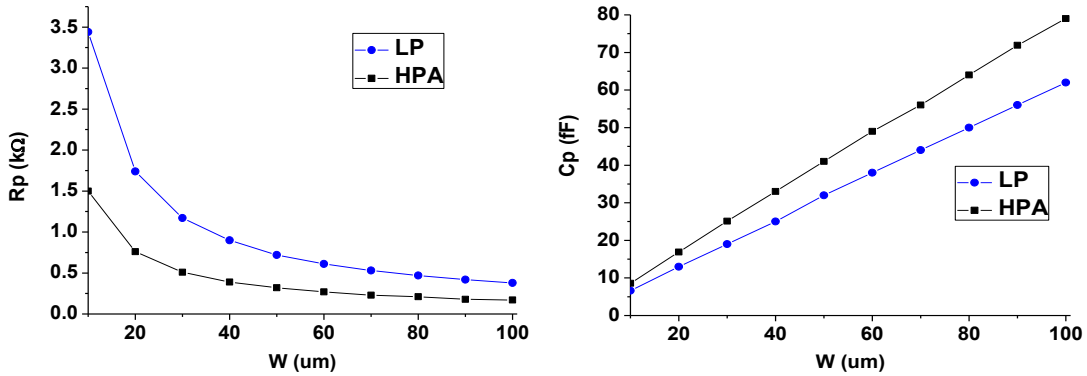


Figure 4.4 The schematic of the detector HPA.

The RF pads are represented by their equivalent shunt capacitors (3 fF as already extracted).

Design procedure:

- The transistors are sized using harmonic balance simulation in order to obtain the desired voltage sensitivity value. The impedance of those transistors for small RF signal can be represented by the channel resistor (R_P) in parallel with the parasitic capacitor (C_P). The R_P in the GP and LP transistors has higher values (less dominant) as compared to the case of HPA transistors. Therefore, adding a series attenuating resistor (R_a) in GP and LP detectors is necessary to help to match the circuit by



(a) (b)

Figure 4.5 The extracted R_P and C_P values (from Cadence) for diode connected NMOS at 42 GHz, for $N = W$.

increasing the real part impedance. Meanwhile, matching the HPA detector is established without R_a. Figure 4.5 shows the extracted R_P and C_P values (from

Cadence) for the diode connected transistors LP and HPA at 42 GHz, where *w* (is the channel width) is equal to number of fingers *N*. The NMOS transistors are sized taking *w* = *N* since their models which are used in the simulation is more reliable in this case.

- Small and large signal S-parameters simulations are executed in order to design the matching network, where the elements of this network are sized to produce the desired $|S_{11}|$ values in the frequency band of interest.

4.2.2.2 Measurement results

The layouts of the zero bias detectors are very similar, this layout is shown in figure 4.6. The detector area is 0.09 mm^2 without the pads.

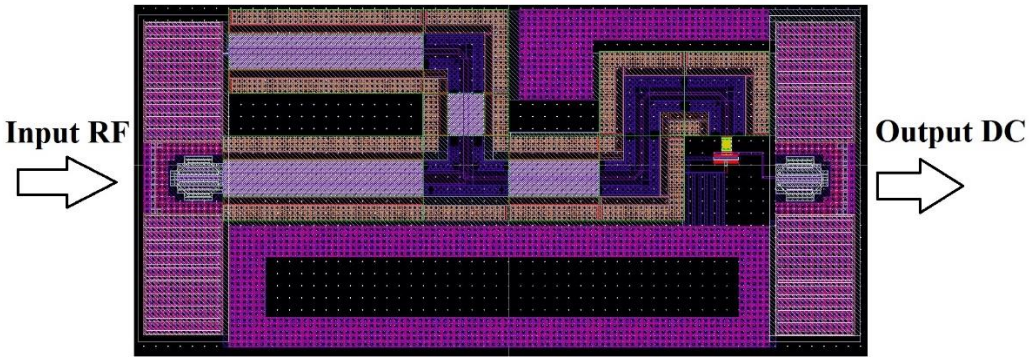


Figure 4.6 The layout of the zero bias detector based on single NMOS.

A. Measurement of the reflection coefficient

Figures 4.7 (a,b,c) show the measured and simulated S_{11} curves of the GP, LP and HPA detectors. These detectors are matched in the frequency bands (38-48), (40-50) and (42-50) GHz respectively, where $|S_{11}| \leq$ -8 dB. The measured S_{11} curves show some shifts in frequency comparing to simulations, thus some deviations in S_{11} values are obtained. These shifts in frequency are attributed to: (i) The T structures in the layout design, (ii) the standing waves which can be occurred in the output line (l_4) (as the case

in the paragraph 3.4.5 A). In order to verify the T structures effects, post layout or electromagnetic simulations will be executed in the future works.

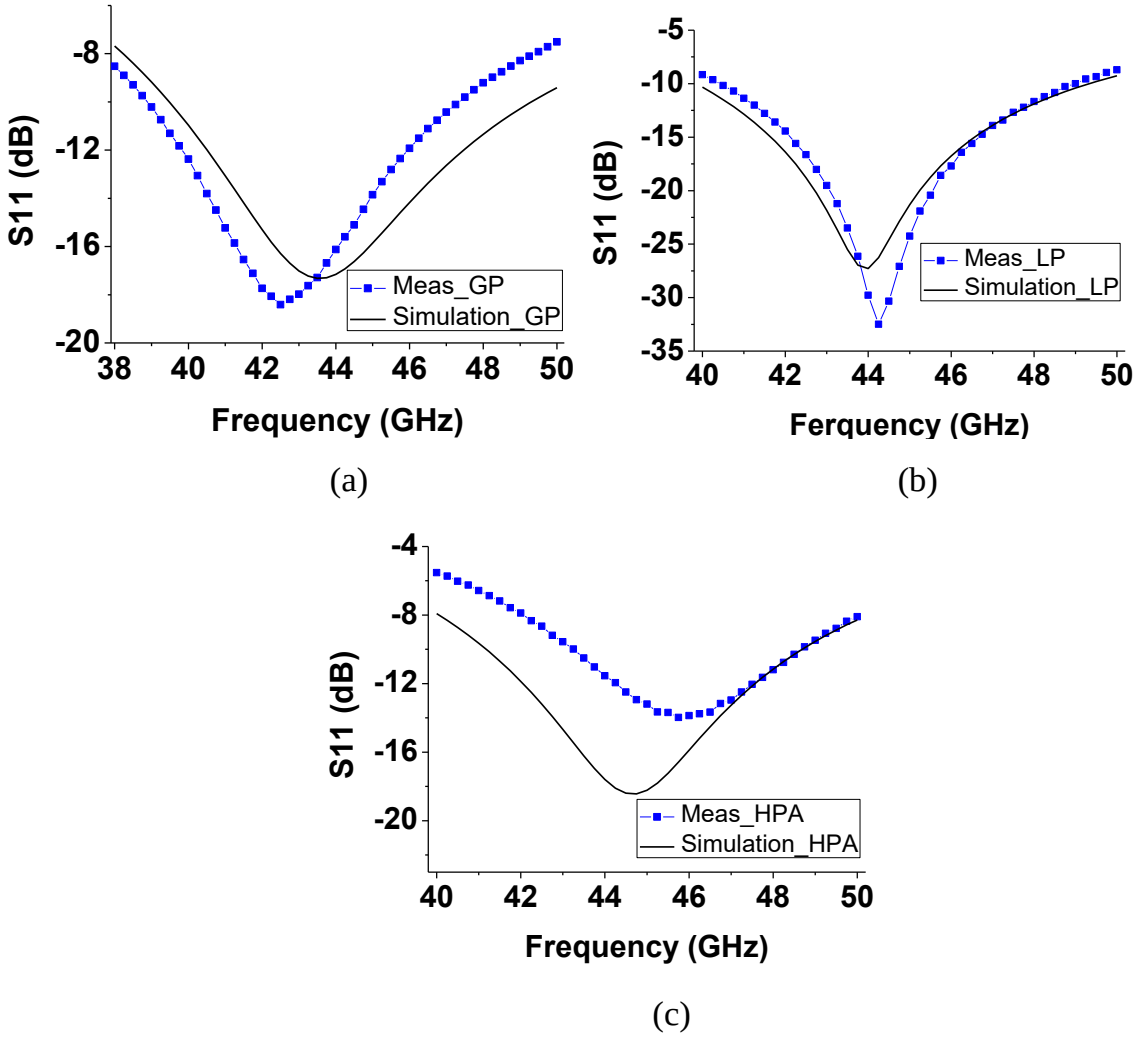


Figure 4.7 Measured and simulated S_{11} for: (a) GP, (b) LP, (c) HPA detectors at P_{in}=-12 dBm.

B. Measurement of voltage sensitivity γ

The measurements of voltage sensitivity are done using the same strategy presented in paragraph 3.4.5(c). The test bench used to extract the voltage sensitivity values of the ZBDs is shown in figure 4.8. No DC current source is required for the ZBDs, therefore, we only need the DC voltmeter at the detector output. The voltage V_{OFF} and V_{ON} are measured, and then applied in equation 3.8.

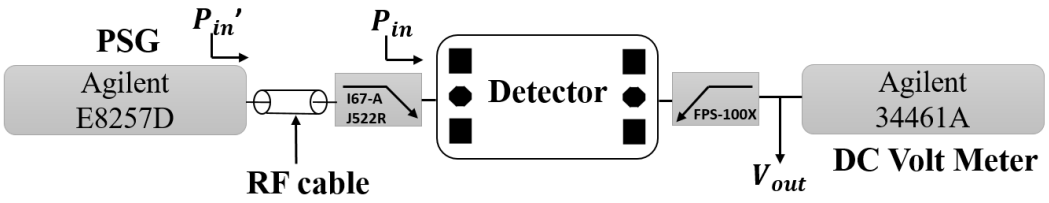


Figure 4.8 Test bench block diagram to extract the voltage sensitivity of zero bias detectors.

Figures 4.9 (a,b,c) show the measured and simulated voltage sensitivity curves versus the frequency of the GP, LP and HPA detectors. From the obtained results, it can be concluded that:

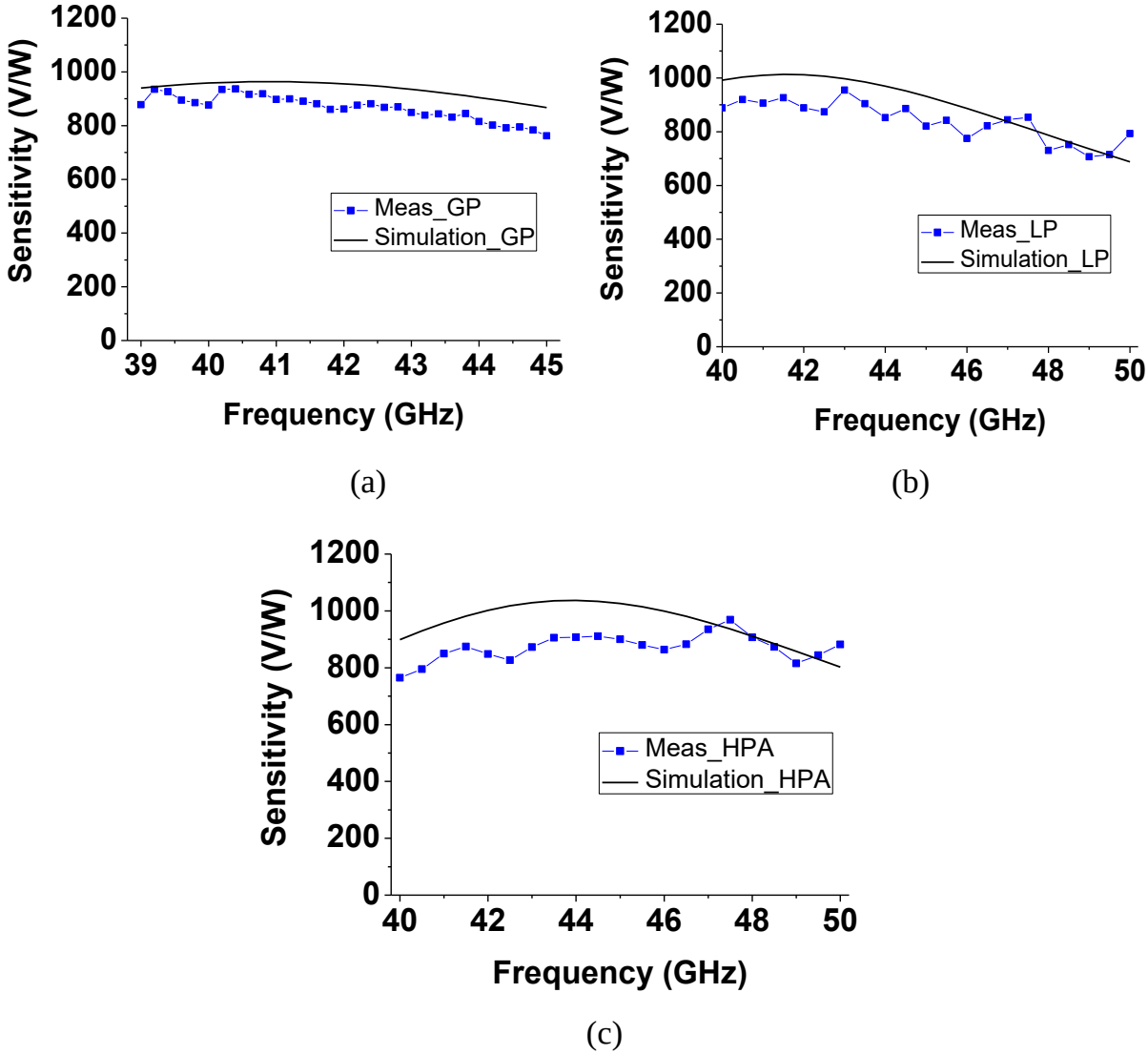
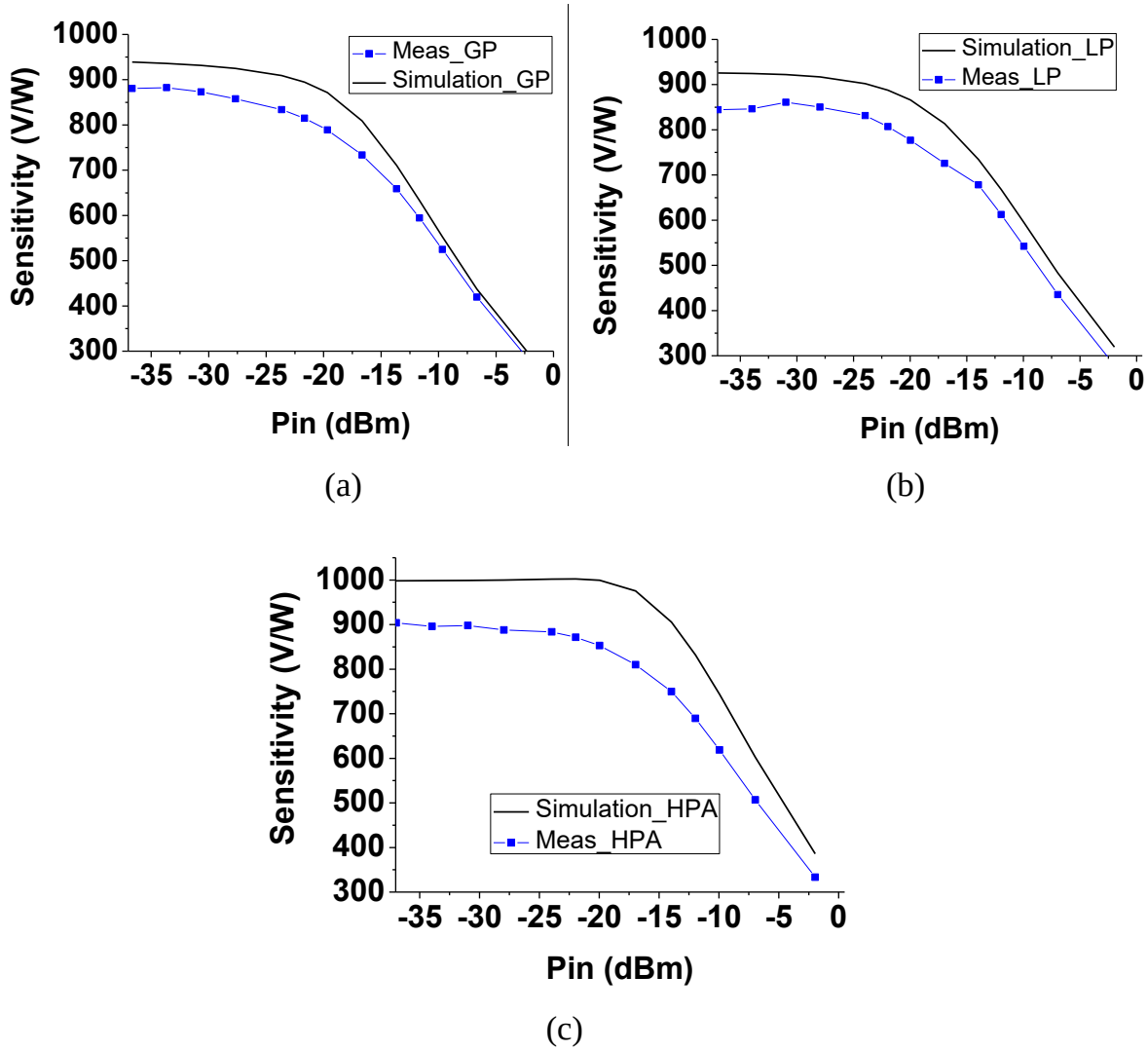


Figure 4.9 The measured and simulated voltage sensitivity curves vs frequency @ P_{in}= -25 dBm for: (a) GP, (b) LP, (c) HPA detectors.

- The sensitivity curves are relatively flat in the frequency band of interest for the HPA detectors ($\gamma = 850$ V/W $\pm$ 11%).
- A good agreement is obtained between the simulation and measurement results, where the deviation is smaller than 10% for all the frequency band.

Figures 4.10 (a,b,c) show the measured and simulated sensitivity curves versus input injected power at 44 GHz. The compression point P_{in_max} is defined as the input power level for which the sensitivity value is degraded by 10% comparing to its value in the linear zone.



Figures 4.10 The measured and simulated voltage sensitivity curves vs input power at 44 GHz for: (a) GP, (b) LP, (c) HPA detectors.

Based on the obtained results, it can be concluded that the P_{in_max} occur at (-20, -20, -17) dBm corresponding to the GP, LP and HPA detectors respectively, showing the agreement with the simulation.

C. The estimation of the video resistance R_V and NEP

For DC and low frequencies, the diode connected transistor can be represented by a resistor R_{DS} (the channel resistance). The value of this resistance depends on the channel doping (NMOS category), the transistor size and biasing conditions.

The video resistance values of the designed zero bias detectors are equal to the R_{DS} values of their NMOS transistors, where the attenuating resistance (50 Ω) is negligible comparing to R_{DS}. In order to extract the value of video resistance, the voltage V_{ON} is measured (at certain RF power) for loaded and unloaded detector. The equivalent circuit of the loaded detector at DC is shown in figure 4.11.

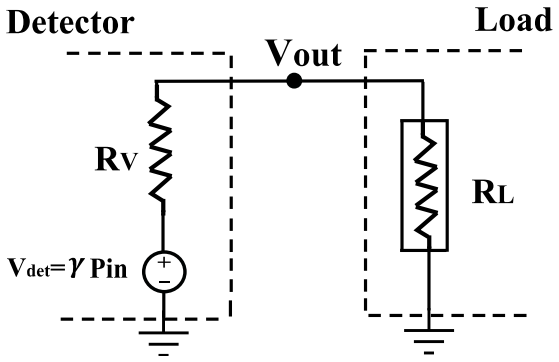


Figure 4.11 The DC equivalent circuit of detector loaded by resistance R_L.

The output voltage $V_{out\_unloaded}$ is equal to V_{det} for the unloaded detector. When the detector is loaded by a certain resistor R_L, the voltage V_{out_loaded} is given in the following:

$$V_{\text{out\_loaded}} = V_{\text{out\_unloaded}} \cdot \frac{R_L}{R_L + R_V} \tag{4.4}$$

The R_L value has to be high enough as compared to R_V, hence it does not affect the transistor impedance, i.e. the voltage $V_{out\_loaded} > 0.9.V_{out\_unloaded}$. Based on the equation 4.4, the value of the video resistance can be calculated as the following:

$$R_V = R_L\left(\frac{V_{\text{out\_unloaded}}}{V_{\text{out\_loaded}}} - 1\right) \tag{4.5}$$

Extracting the video resistance value helps to:

- Demonstrate the detector performance under load, and so, determine the minimum allowed impedance value of the load to avoid load effect (as explained in paragraph 2.3.5).
- Calculate the thermal noise generated in the device.

In order to determine the dynamic range of the detectors (*Dy*), extracting the value of the minimum detectable power (P_{in_min}) is required.

Since no DC current passes through the transistor, the thermal noise (generated by the resistance R_{DS}) is considered as the only source of noise in the circuit. The noise equivalent power (NEP) for zero bias diode is mentioned in equation 2.14 in chapter 2 as in the following:

$$NEP = \frac{\sqrt{4.K.T.R_V}}{\gamma} \qquad (\text{W}/\sqrt{Hz})$$

For continues wave (CW) RF power, the video bandwidth is considered to be 1Hz, thus the P_{in_min} is equal to NEP value (equation 2.12).

D. <u>The figure of merit and results summary</u>

In order to evaluate the detectors performances, a figure of merit FOM proposed in chapter 2 is calculated for each detector based on the equations 2.19 and 2.22 :

$$Dy = \frac{P_{in\_\max}}{P_{in\_\min}}$$

$$FOM = Dy \times \gamma \times 1e-7$$

The factor 1E-7 makes the FOM values in appropriate scale.

E. The extracted detectors parameters

Table 4.1 summarizes the extracted parameters of the detectors GP, LP and HPA at 44 GHz. It can be concluded that the HPA detector has the lowest value of NEP, and so P_{in_min}. In addition, it provides the largest dynamic range and the best performance comparing to other detectors.

Detector	R_V (kΩ)	P_{in_min} @ CW (dBm)	NEP (pW/$\sqrt{Hz}$)	P_{in_max} (dBm)	Dy (dB)	γ (V/W)	FOM (V/W)
GP	85	-74	42	-20	54	880	22.5
LP	4500	-65	322	-20	45	850	2.7
HPA	0.8	-84	3.8	-17	67	900	473

Table 4.1 The extracted parameters of the zero bias detectors based on single transistor at 44 GHz.

In the HPA detector, the total input power is absorbed in the transistor, therefore it exhibits higher performance comparing to GP and LP detectors (where part of input power is absorbed in the resistor R_a).

4.2.3 Zero bias detector using stack of 6 NMOS

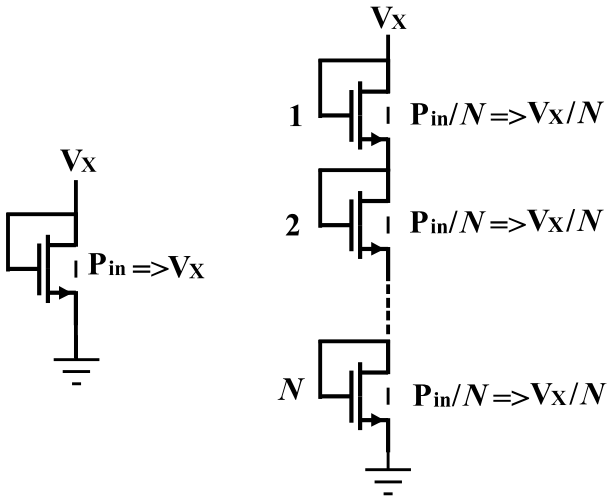
Table 4.1 in the previous paragraph shows that the maximum compression point is obtained at -17dBm. Three main strategies can be used in order to maintain the linearity at higher input power (P_{in}):

1) Adding an attenuator, however it decreases the sensitivity levels.

2) Using a stack of *N* identical transistors (or diodes), where the P_{in_max} is extended without reducing the sensitivity value. Therefore, this topology is considered more advantageous as compared to the attenuator. This will be explained in the next paragraphs.
3) Linearizing the detector response by using equation 4.10 (instead of equation 3.8) to extract the sensitivity curves (or calculate the input power). This method is explained in the paragraph 4.2.4.

4.2.3.1 Theoretical background

When RF power (P_{in}) is absorbed by a transistor NMOS, a DC voltage V_x is generated depending on the power level and responsivity of the transistor. The same voltage value V_x is obtained (and so the same sensitivity γ) when stack of the same transistor is used, where each transistor absorbs (P_{in}/N) of power. This concept is illustrated in figure 4.12.



(a) (b)

Figure 4.12 The DC voltage generated using (a) single transistor, (b) stack of *N* transistors.

If the compression point of single transistor occurs at the power (P_{in_max}), hence the compression point of stack of *N* transistors will be occurred at the power ($N \times P_{in\_max}$), since only the power (P_{in}/N) is absorbed in each individual transistor. Meanwhile, the sensitivity value is kept at the same value (same V_x).

If the video resistance of single transistor is (R_V), hence the video resistance of stack of N transistors is ($N \times R_V$), and so we can write the relation between the NEP values:

$$NEP_{Stack} = \frac{\sqrt{4.K.T.N.R_V}}{\gamma} = \sqrt{N}.NEP_{Single} \tag{4.6}$$

hence
$$P_{in\_\min\_Stack} = \sqrt{N}.P_{in\_\min\_Single} \tag{4.7}$$

Where the index 'Stack' and 'Single' are for stack of N transistors and single transistor respectively. The dynamic range is calculated as the following:

$$Dy_{Stack} = \frac{N.P_{in\_\max}}{\sqrt{N}P_{in\_\min}} = \sqrt{N}.Dy_{Single} \tag{4.8}$$

hence in dB
$$Dy_{Stack} = 5\log(N) + Dy_{Single} \tag{4.9}$$

It can be concluded that the stack of transistors topology offers two advantages:

- It helps to increase the dynamic range (equation 4.9).
- It helps to maintain the linearity at higher input power (compression point occurs at $N \times P_{max}$).

On the other hand, two disadvantages can be mentioned:

- The minimum detectable power (P_{in_min}) is higher as compared to single transistor (equation 4.7).
- The stack structure exhibits higher impedance requiring larger matching network.

In order to overcome the second disadvantage, a parallel stack structure can be used as shown in figure 4.13. For the RF signal, the transistors are considered to be in parallel exhibiting low impedance. On the other hand, they are considered to be in series for DC and low frequencies. Therefore, this structure takes the advantages of stack transistors while exhibiting low impedance (for RF signal).

To avoid a parallel stack with very low impedance, we propose in this thesis to use a hybrid structure (series-parallel) stack in order to obtain a moderate impedance (as explained in the next paragraph).

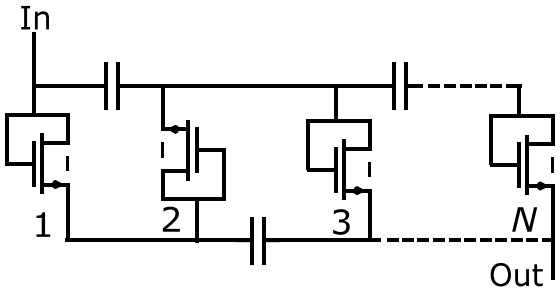


Figure 4.13 Parallel stack of *N* transistors.

4.2.3.2 Detector design

The transistor LP was chosen to build zero bias detector based on (series-parallel) stack topology (as a proof of concept), its schematic is shown in figure 4.14.

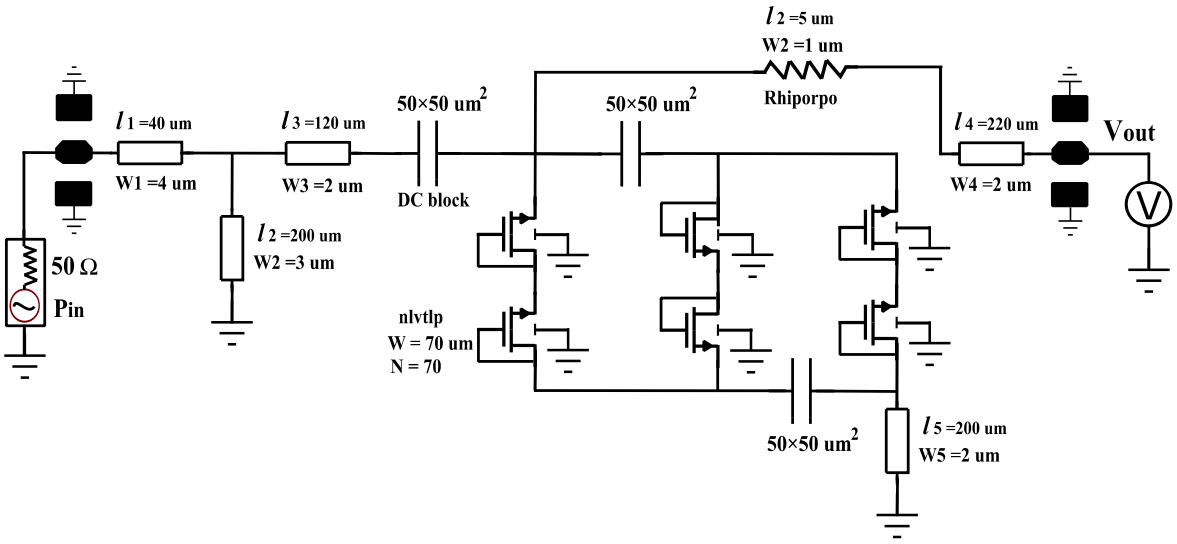


Figure 4.14 Zero bias detector schematic based on stack of 6 transistors.

The stub l_5 is used as an inductive element in order to help to match the detector. The resistor (Rhiporpo of 30 kΩ) is used as a high impedance to isolate the detector output at high frequencies, whereas the output DC voltage can be observed at the output pad

(since no current passes through the resistor). The stubs l1, l2, l3 and DC block capacitance are used as a matching network. The transistor LP is used to build the stack structure, hence the performance of this detector will be compared to the performance of the LP detector which uses single transistor.

4.2.3.3 Measurement results

The layout of the stack zero bias detector is shown in figure 4.15, where the detector area is 0.1 mm^2 without the pads.

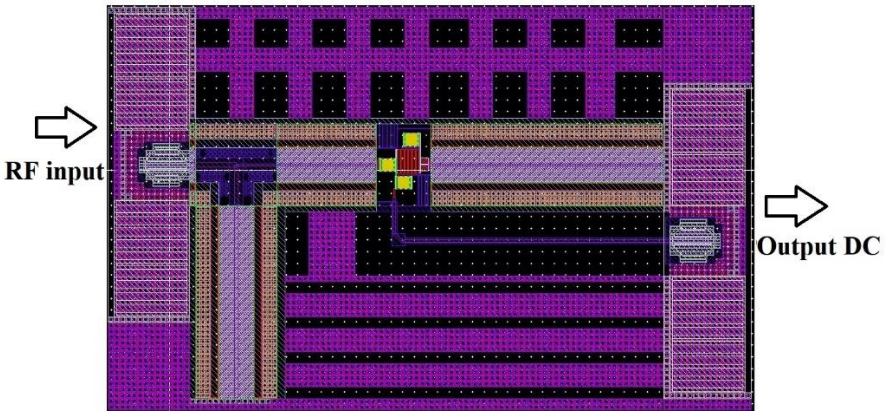


Figure 4.15 The layout of zero bias detector based on stack of 6 transistors.

A. <u>Measurement of the reflection coefficient</u>

Figure 4.16 shows the measured and simulated S_{11} curves of the Stack detector, the frequency band of matching is (42-55) GHz, where $|S_{11}| \leq$ -8 dB. A shift in frequency is obtained between the simulation and measurements as in the previews detectors (paragraph 4.2.2.2).

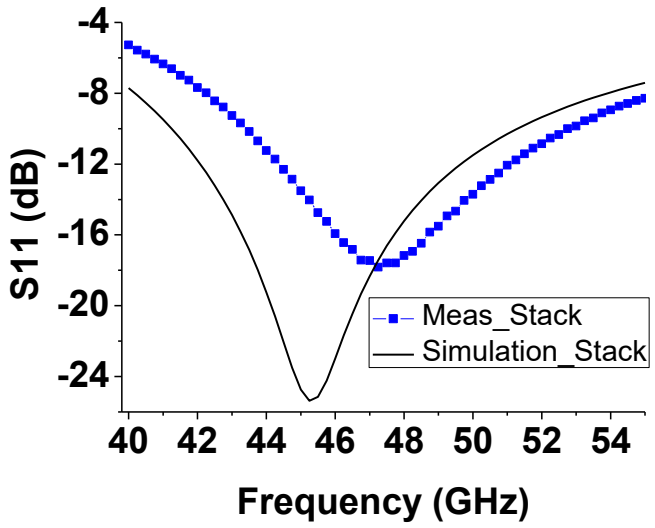
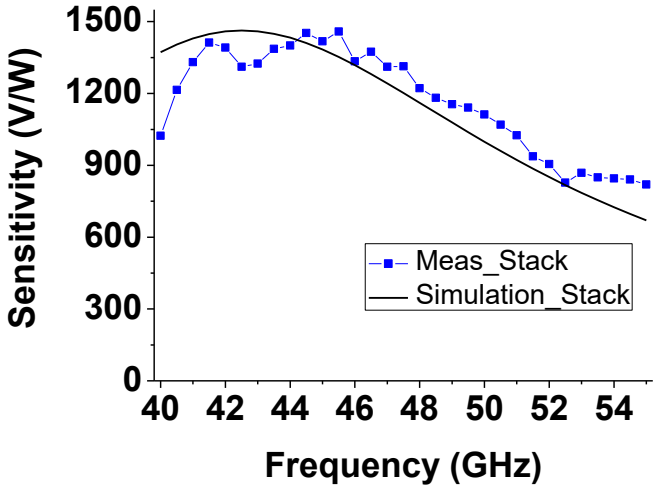


Figure 4.16 The measured and simulated S_{11} of the stack zero bias detector @ P_{in}= -12 dBm.

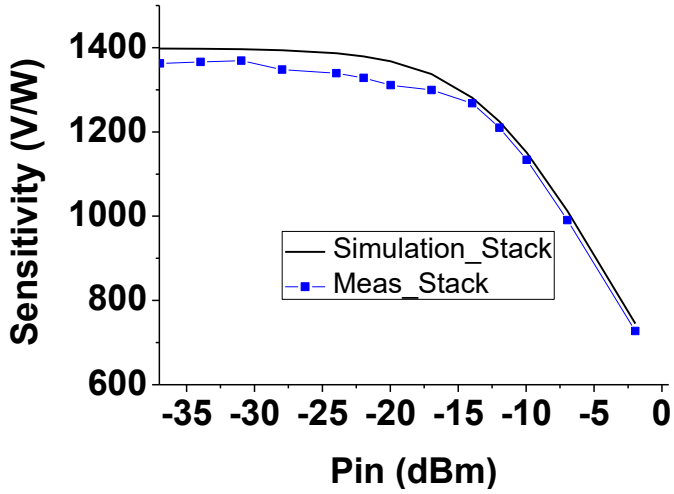
B. Measurement of voltage sensitivity γ

The extraction of the voltage sensitivity values is done using the same bench setup in 4.2.2.2 B. Figure 4.17 shows the measured and simulated sensitivty curves versus the frequency for the stack zero bias detector, where good agreement is obtained.



Figures 4.17 The measured and simulated voltage sensitivity curves vs frequency of the Stack detector @ P_{in}= -25 dBm.

Figure 4.18 shows the measured and simulated sensitivty curves versus the input power at frequency 44 GHz. From the obtained results, it can be concluded that:



Figures 4.18 The measured and simulated voltage sensitivity curves vs input power of Stack detector at 44 GHz detectors.

- A good agreement is obtained between the simulation and measurement results.
- The P_{in_max} occurs at -12 dBm exhibiting higher level comparing to the LP detector.

C. The extracted detectors parameters

The values of R_V, NEP, P_{in_min} and FOM are extracted using the equations 4.5, 2.14 and 2.22 as in the previews paragraphs. The following table summarizes the extracted parameters for the stack zero bias detector.

R_V (kΩ)	P_{in_min} @ CW (dBm)	NEP (pW/$\sqrt{Hz}$)	P_{in_max} (dBm)	Dy (dB)	γ (V/W)	FOM (V/W)
27000	-63	485	-12	51	1380	18

Table 4.2 The extracted parameters of the Stack zero bias detector @ 44 GHz.

Several conclusions can be mentioned based on the results in table 4.2:

- The Stack detector provides the highest P_{in_max} value (as compared to the other detectors in table 4.1), hence it can be used at higher levels of RF power.
- Using stack of N transistors (instead of single transistor) can enhance the detector performance, this can be noticed by comparing the FOM of LP with Stack detectors.
- The NEP value is relatively high (as compared to the other detectors in table 4.1), this is considered as the disadvantage of the stack topology.

- A better detector performance is expected to be obtained by stacking HPA instead of LP transistors (since the performance of the HPA transistor is better than LP).

4.2.4 Linearizing the detector response

When low RF power (P_{in}) is applied on a detector, the output voltage is proportional to P_{in}, and so, the detector exhibits linear response. However, for higher levels of RF power ($P_{in} > P_{in\_max}$), the polynomial terms with higher weights in the DC current relation become important ((*) Annex1), hence the detector response is no more linear. The equation 4.10 (deduced in Annex 2) helps linearizing this response at higher power levels.

$$\gamma = \frac{2.n.V_T}{P_{in}} \ln\left(0.5 + 0.5.\exp\left(\frac{V_{OFF} - V_{ON}}{n.V_T}\right)\right) \quad (4.10)$$

As an example, figure 4.19 shows the extracted sensitivity curves for the detector GP, where two different equations are used (3.8 and 4.10), hence the compression point (P_{in_max}) is increased by 12 dB using equation 4.10. Table 4.3 summarizes the extracted parameters for the GP detector using the equation 4.10.

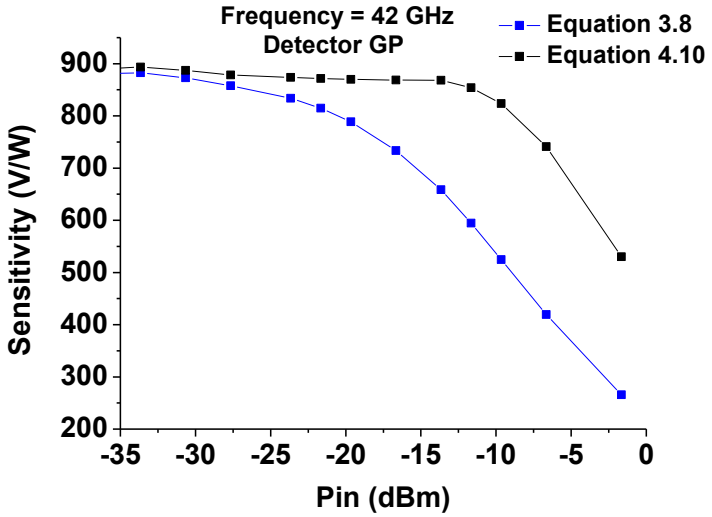


Figure 4.19 The extracted voltage sensitivity curves of GP detector using the equations 3.8 and 4.10.

Detector	R_V (kΩ)	P_{in_min} @ CW (dBm)	NEP (pW/$\sqrt{Hz}$)	P_{in_max} (dBm)	Dy (dB)	γ (V/W)	FOM (V/W)
GP	85	-74	42	**-8**	**66**	880	**331**

Table 4.3 The extracted parameters of the GP detector at 44 GHz, using the equation 4.10.

As a conclusion, using the equation 4.10 significantly increases the dynamic range, and so enhances the detector performance (FOM becomes 331 instead of 22.5).

On the other hand, applying this method also increases the processing delay, this is considered as a limitation in the real time applications. Application-specific integrated circuit (ASIC) can be used in order to process the output signal.

It is worth to mention that this method is just an example of mathematically linearizing the detector response, i.e. the equation 4.10 can be more complex, providing higher level of P_{in_max}.

4.2.5 Temperature compensated zero bias detector

In the paragraph 4.2.1, it has been concluded that the I-V behavior of diode connected transistor in zero bias condition is similar to a diode, thus its performance is temperature dependent.

In the literature, several techniques are proposed to design temperature compensated power detectors. The technique in [80] proposes to add a dummy detector which is not fed by the input power; the output of this dummy is used as a temperature dependent offset in order to compensate the effect of temperature variation. The design in [81] proposes a power detector using the subtraction between two temperature dependent DC currents in order to produce a DC current independent of temperature. However, those techniques require higher power consumption, larger areas and more complex circuitries.

In [82], it is proposed to add a temperature-sensitive voltage divider (including diode and resistors). However, adding those elements on the detector output can significantly increase the NEP value.

In the application note [83], it is proposed to use a Schottky diode where the DC biasing current is temperature dependent. This is established by adding thermistor with positive

temperature coefficient (PTC) in series with the DC biasing source. However, adding the thermistor increases the power consumption, in addition, this technique cannot be used with zero bias devices.

In the following, we propose the design of power detector which has a robust performance against the temperature variations (real-time temperature compensated detector).

4.2.5.1 Theoretical background

When the ambient temperature increases, smaller voltage sensitivity value is produced (as the case of the PN diode). This behavior is verified using Cadence virtuoso.

In order to compensate the decrease of sensitivity values with temperature, we propose to increase the power delivered to the NMOS with temperature. This can be established by adding a positive temperature coefficient resistor (PTC) in parallel with the NMOS as illustrated in figure 4.20.

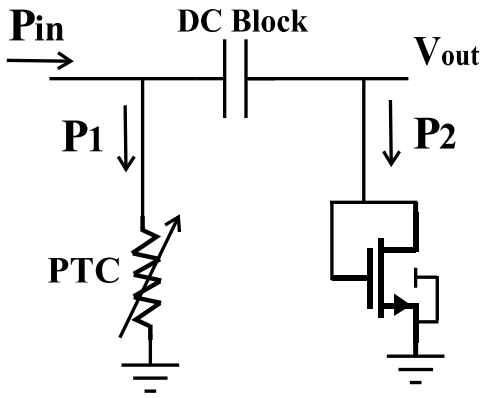


Figure 4.20 Temperature compensation technique by adding a PTC in parallel with the transistor.

The value of the PTC resistor increases with temperature, hence less power will be absorbed in this resistor (P_1); and higher power will be delivered to the transistor (P_2).

4.2.5.2 Detector design

Figure 4.21 shows the schematic of the proposed temperature compensated detector. The technology 55nm-BiCMOS does not provide thermal elements such as PTC and NTC. The transistor nhpalp (HPA) is used to act as a thermal element since its impedance varies significantly with temperature (according to the simulation).

The diode connected HPA transistor can be represented by a resistor R_{DS} in parallel with a capacitor C_{DS} (for RF signal). The R_{DS} value decreases with the temperature

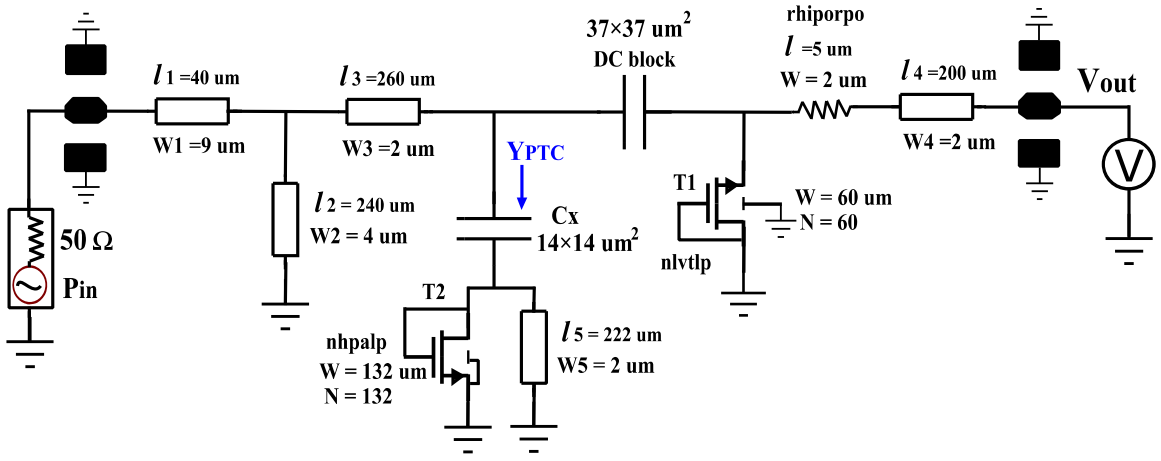


Figure 4.21 The schematic of temperature compensated detector.

following the rate 0.7 Ω/°C (according to the simulation). In our design, a PTC resistor in parallel with the transistor (T_1) is required, thus, the capacitor C_X is added in series with the transistor T_2 for two reasons :

- To produce the opposite behavior of R_{DS} over the temperature, i.e. producing a parallel resistance (R_{PTC}=1/real(Y_{PTC}) which increases with the temperature.
- The rate of increasing the resistance value with temperature ($\Delta R_{PTC}/\Delta T$) can be adjusted by varying the value of the capacitor C_X.

The stub l5 is connected in parallel with the transistor (HPA) in order to compensate (reduce) the effect of its C_{DS}. The stubs l1, l2, l3 and DC block capacitor are used as a matching network. The resistor (rhiporpo of 30 kΩ) at the output is used as a high impedance to isolate the detector output at high frequencies.

The proposed temperature compensation circuit (represented by C_X, l5 and T_2) has 4 advantages:

- Simple structure.
- Passive structure, i.e. no biasing source is required.
- It is isolated from the output DC circuit because of the DC block capacitor, hence it does not contribute to the DC noise voltage (V_{noise}), and so the NEP value is not affected.
- It offers an instantaneous compensation, i.e. real time response.

The elements of the temperature compensation circuit are sized using Cadence virtuoso in order to obtain the desired Y_{PTC} values in the temperature range (20 - 90)°C.

4.2.5.3 Measurement results

The layout of the temperature compensated detector is shown in figure 4.22, where the detector area is 0.16 mm^2 without the pads.

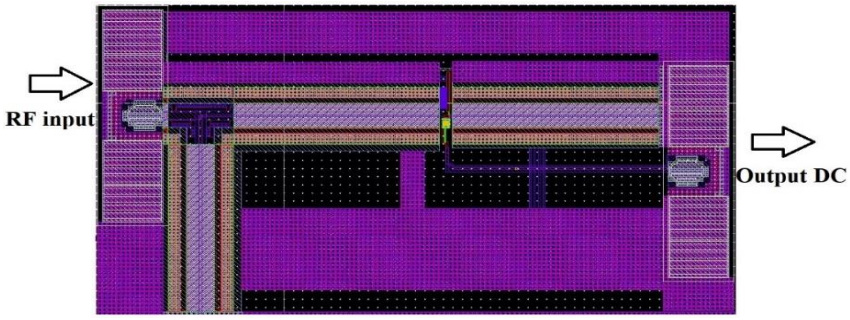


Figure 4.22 The layout of the temperature compensated detector.

A. Measurement of the reflection coefficient

Figures 4.23, 4.24 show the simulated and measured S_{11} curves for several temperatures. The deviation between the simulation and measurement results is due to the same reasons explained in 4.2.2.2 (A).

Based on the measurements, the detector is matched in the frequency band (42-52) GHz for the temperature range (20 - 90)°C, where $|S_{11}| \leq$ -8 dB.

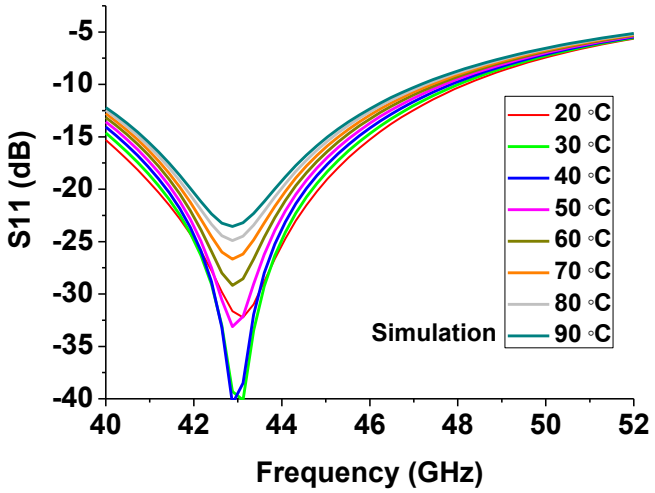


Figure 4.23 The simulated S_{11} of the temperature compensated detector for several temperatures.

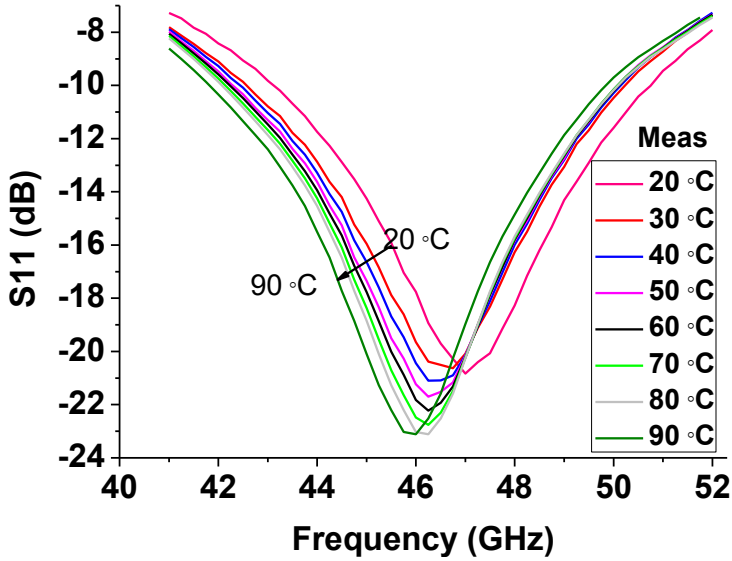


Figure 4.24 The measured S_{11} of the temperature compensated detector for several temperatures.

B. Measurement of the Y_{PTC}

The S_{11} parameters of the PTC circuit stand alone were extracted (one port configuration) in the frequency band (41 – 52) GHz, and for several temperatures. The extracted S parameters are transferred into Y parameters which represent Y_{PTC}.

The figures 4.25 (a, b) show the simulated and measured equivalent parallel resistance (R_{PTC}=1/real(Y_{PTC})) exhibited by the PTC circuit versus frequency, and for several temperatures.

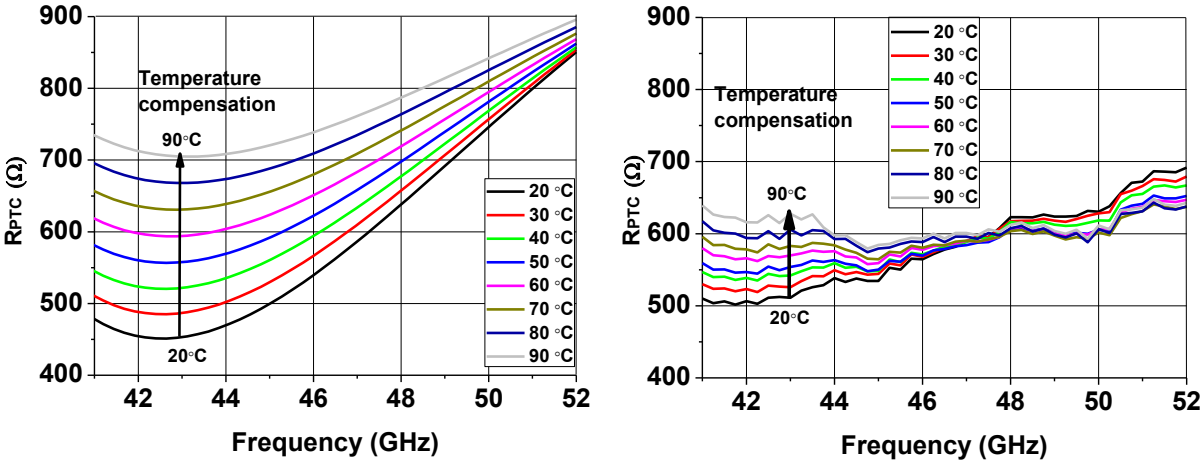


Figure 4.25 The equivalent parallel resistor of the PTC circuit for several temperatures: (a) simulation, (b) measurement.

It can be concluded that:

- The variation ratio ($\Delta R_{PTC}/\Delta T$) in the measurement (1.65 Ω/°C at 43 GHz) is smaller than the simulation (3.5 Ω/°C at 43 GHz) in the temperature range (20 -90) °C. This difference may be due to the inaccuracy of the thermal model of the HPA transistor.
- Based on the measurements, the temperature effect is compensated in the frequency band (41- 43) GHz, since the R_{PTC} value increases with temperature.
- The measured R_{PTC} value does not vary with temperature at 47 GHz, thus the temperature effect is not compensated at this frequency.

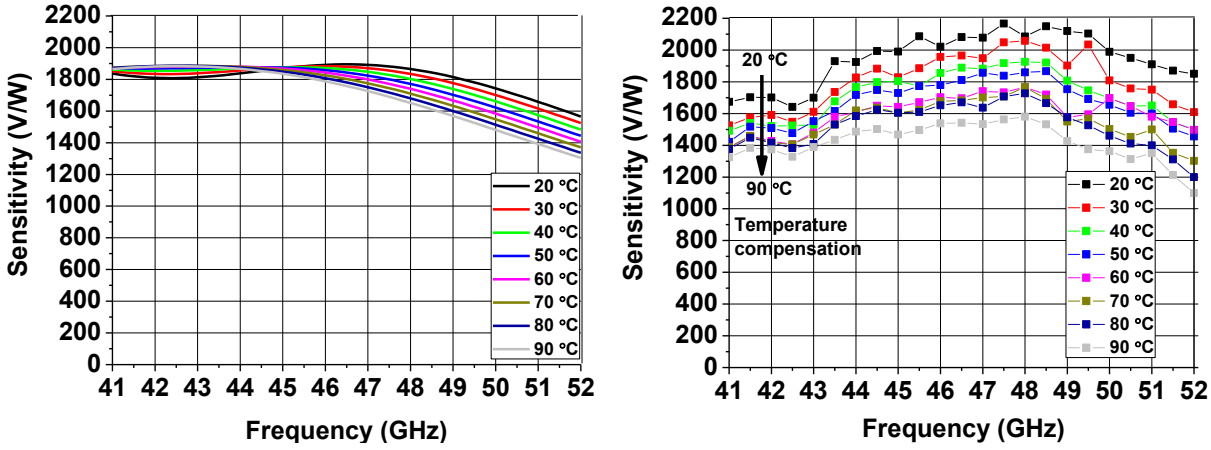
C. Measurement of voltage sensitivity γ

The extraction of the voltage sensitivity values is done using the same bench setup in 4.2.2.2 B, where the wafer holder is heated up to apply different temperatures. The figures 4.26 (a, b) show the simulated and measured sensitivty curves versus the frequency for several temperatures, in addition, the figure 4.27 shows the sensitivity curves versus temperature for two frequencies. From the obtained results, it can be concluded:

- The temperature effect is completely compensated in the simulation in the frequency band (41 - 45) GHz (the sensisitivity value γ is nearly constant over the

temperature). This frequency band was chosen following the targeted band of ADVENT project, and so, as a proof of concept.

- The measured sensitivity values decrease by 8.1 V/(W.°C) with temperature at 47 GHz (temperature effect is not compensated), whereas this ratio is 4.2 V/(W.°C) at 43 GHz, thus, the temperature effect is compensated by 50% at this frequency.
- Since the measured variation ratio ($\Delta R_{PTC}/\Delta T$) is smaller than the simulation, the measured sensitivity value is not completely compensated with temperature. The detector can be modified to exhibit a complete temperature compensation by tuning the capacitance C_x value, and so increasing the ratio ($\Delta\ R_{PTC}/\Delta T$).



(a) (b)

Figure 4.26 The voltage sensitivity curves vs frequency of the temperature compensated detector @ P_{in}= -25 dBm: (a) simulation, (b) measurements.

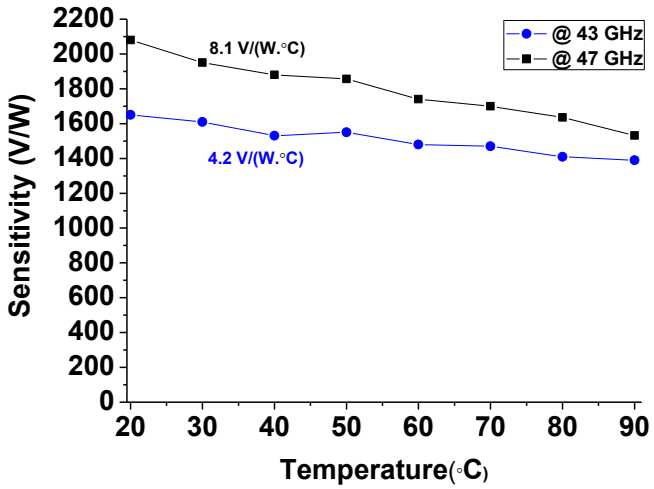


Figure 4.27 The measured sensitivity curves vs temperature of the temperature compensated detector at two frequencies, P_{in}= -25 dBm .

Figure 4.28 shows the measured sensitivty curves versus the input power at frequency 45 GHz, and two temperatures (20°C and 90°C), where the compresion point (P_{in_max}) occurs at -22 dBm and -20 dBm for the two temperatures respectivilly.

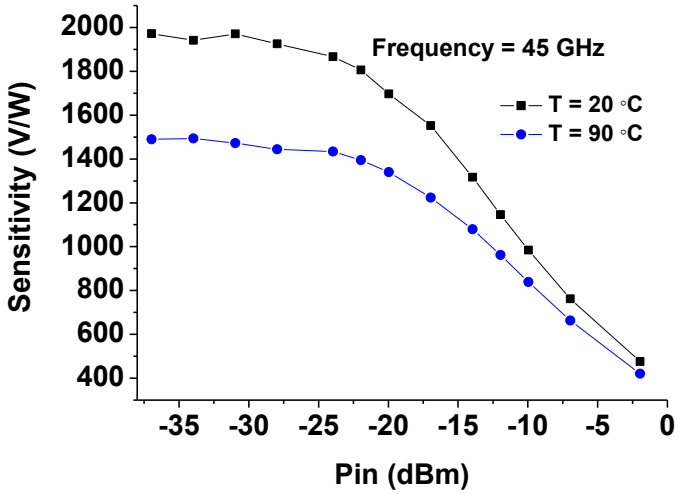


Figure 4.28 The measured voltage sensitivity curve vs input power of the temperature compensated detector at 45 GHz.

D. The extracted detector parameters

The values of R_V, NEP, P_{in_min} and FOM are extracted using the equations 4.5, 2.14, 2.22 as in the previews paragraphs. The following table summarizes the extracted parameters for the temperature compensated detector at 45 GHz for two temperatures.

T (°C)	R_V (kΩ)	P_{in_min} @ CW (dBm)	NEP (pW/$\sqrt{Hz}$)	P_{in_max} (dBm)	Dy (dB)	γ (V/W)	FOM (V/W)
20	5200	-68	147	-22	46	2000	8.4
90	527	-71.6	68	-20	51.6	1500	22

Table 4.4 The extracted parameters of the temperature compensated detector at 45 GHz for two temperature.

Comparing to other detectors in table 4.1, this detector has higher sensitivity value (2000 V/W at 20°C), thus, the compression point (P_{in_max}) occurs at lower power level (-22 dBm). It can be also noticed that the sensitivity is degraded with temperature,

however, the dynamic range *Dy* is improved; this is because the γ and *Dy* depend on the R_V value, and have opposite behavior (as explained in chapter 2).

4.2.6 State of the art

Table 4.5 presents the comparison with other recent zero biased detectors. The HPA detector performance is belong the state of the art exhibiting very low NEP value (3.8 pW/$\sqrt{Hz}$) and large dynamic range (67 dB). This performance is very interesting, where such large dynamic range is necessary to maintain the linear responses in the modern modulations, since their signals have high peak to average power ratios (PAPR).

Refrence	Technology	Frequency (GHz)	NEP (pW/$\sqrt{Hz}$)	P_{in_min} (dBm)	Dy (dB)	γ (V/W)
[84]	Glass substrate	40 – 75	-	-50	>50	15 (at 60 GHz)
[85]	Alumina 5 mil	57 – 65	-	-48	42	8250 (at 61 GHz)
[86]	GaAs/AlAS	15 - 35	20	-	-	1300 (at 24 GHz)
[87]	Commercial Schottky diode	2 – 18	5	-	-	2000 (at 18 GHz)
This work	55-nm BiCMOS		*@ 44 GHz*	*@ 44 GHz*	*@ 44 GHz*	*@ 44 GHz*
		38 – 48 (GP)	42	-74	54	880
		40 – 50 (LP)	322	-65	45	850
		42 – 50 (HPA)	**3.8**	**-84**	**67**	900
		42 – 55 (Stack)	485	-63	51	1380

Table 4.5 The state of the art of ZBDs for the frequencies < 110 GHz.

4.3 Frequency compensated power detector in G-band

As discussed in chapter 2 (paragraph 2.3.3), the sensitivity value depends on the frequency of the RF power. This makes the measurement more complicated (especially for broadband PD), since the sensitivity value has to be calibrated according to the frequency. In the literature, there is only one paper who discusses the frequency compensation in power detectors [88]. This paper proposes adding a feed-forward frequency detection circuit, which helps varying the load of the power detector

according to input frequency, hence compensating the variation of the sensitivity value over the frequency band (3 - 5) GHz. However, the proposed circuit design is complicated, where several analog and digital circuits are required (such as 2 bit ADC, frequency to voltage converter, inverter chain, etc…), and so, the compensation is not in real time (processing delay is required). In addition, it is only compatible with silicon technologies, since the digital circuits are required to be integrated with the PD.
In this thesis, we propose the design of real-time frequency compensated power detector for a wide frequency range (140 - 220) GHz, using an innovative simple circuit.

4.3.1 Theoretical background

When the frequency increases, the effect of the parasitic capacitances in the NMOS (such as channel capacitor C_{DS}) become more dominant, hence, smaller power is absorbed in the transistor, and smaller sensitivity value is produced.
In order to compensate the decrease of sensitivity values with frequency (frequency effect), we propose to increase the power delivered to the NMOS with frequency. This can be established by adding a self-varied attenuator with frequency as illustrated in figure 4.29.

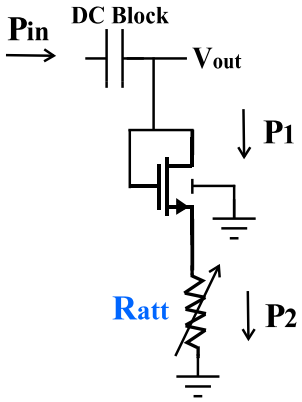


Figure 4.29 Frequency compensation technique by adding a self-varied resistance with frequency.

As the frequency increases, the attenuator exhibits smaller resistance value (R_{att}), and so, smaller power (P_2) is absorbed. Consequently, higher power (P_1) is absorbed in the NMOS, and the sensitivity value is compensated.

4.3.2 Detector design

Figure 4.30 shows the schematic of the proposed frequency compensated detector in G-band. The HPA transistor (T_1) is used as the active device to detect the RF power, since it exhibits the best performance comparing to other transistor type (table 4.1).

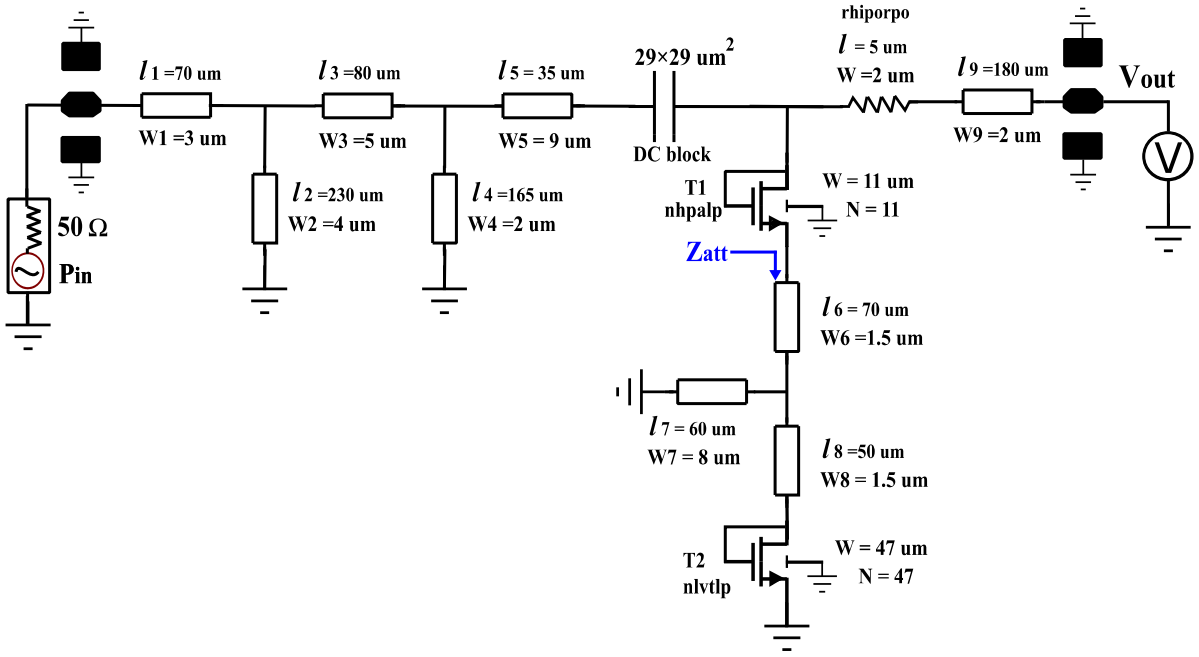


Figure 4.30 The schematic of the frequency compensated detector in G-band.

The stubs (l1, l2, l3, l4, l5) and the DC block capacitance represent the matching network, which guaranties that the detector absorbs the maximum of input RF power. The resistor (rhiporpo of 15 kΩ) at the output is used as a high impedance to isolate the detector output at high frequencies.

The stubs (l6, l7, l8) and the transistor (T_2) represent the attenuator circuit. The series impedance represented by the attenuator is ($Z_{att} = R_{att} + j\,X_{att}$). This circuit has several advantages:

- The value of the real part impedance R_{att} decreases with the frequency in order to compensate the frequency effect.
- It exhibits an inductive impedance (X_{att} > 0) in the frequency band of interest, this helps to match the detector by compensating the capacitive effect of the transistor (T_1).
- It exhibits a short circuit at DC and low frequencies (due to the stubs l6, l7), thus, it does not increase neither the video resistance (R_V) nor the noise voltage (V_{noise}).

The elements of the attenuator circuit are sized using Cadence virtuoso in order to obtain the desired Z_{att} values in the frequency band of interest.

4.3.3 Measurement results

The layout of the frequency compensated detector in the G-band is shown in figure 4.31, where the detector area is 0.08 mm^2 without the pads.

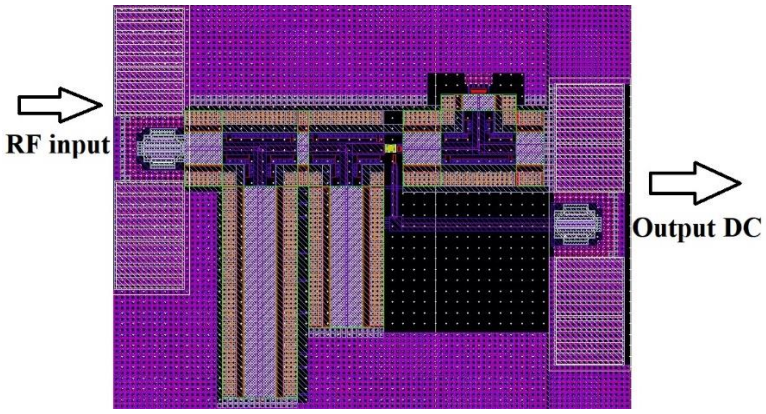


Figure 4.31 The layout of the frequency compensated detector in the G-band.

A. Measurement of the reflection coefficient

Figure 4.32 shows the simulated and measured S_{11} in the G-band. The simulation shows that the detector is matched in the whole G-band, where $|S_{11}| \leq$ -9.5 dB. However, the measured results show some differences as compared to the simulation. The transistors models were verified and validated up to 220 GHz, therefore, those

discrepancies are attributed to the T structures in the layout design. It is worth to mention that the resistor at the detector's output avoids having standing waves.

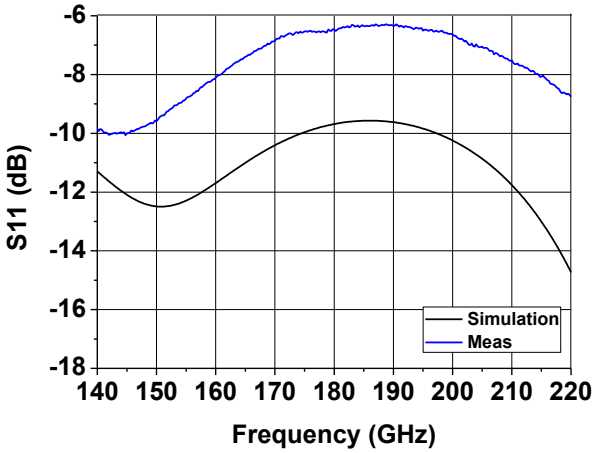


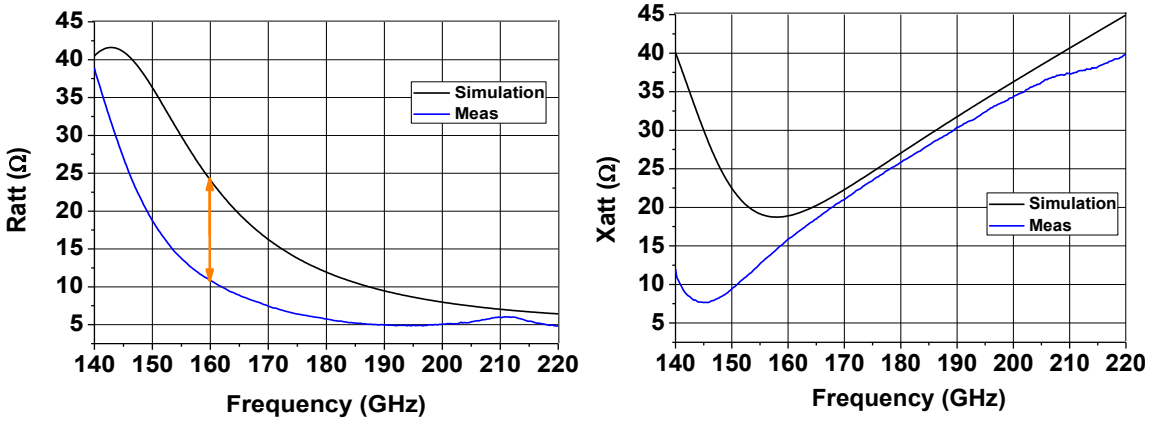
Figure 4.32 The measured and simulated S_{11} of the frequency compensated detector in G-band.

B. Measurement of the Z_{att}

The S_{11} parameters of the attenuator circuit stand alone were extracted (one port configuration) in the frequency band (140 – 220) GHz. The extracted S parameters are transferred into Z parameters which represent Z_{att}.

The figures 4.33 (a, b) show the simulated and measured R_{att} and X_{att} versus frequency, where two conclusions can be mentioned :

- The values of the measured R_{att} show lower levels as compared to the simulation.
- Based on the measurements, positive values of X_{att} are obtained, i.e. the attenuator circuit exhibits an inductive impedance (as expected).



(a) (b)

Figure 4.33 The simulated and measured: (a) R_{att}, (b) X_{att}.

C. Signal power source configuration in G-band

The maximum frequency can be provided using the PSG E8257D is 67 GHz, therefore, frequency converter is required in order to generate power signal in the G-band. The VNA "R&S ZVA Vector Network Analyzers" from *rohde & Schwarz* company [89] is used as the source of RF power at 24 GHz, then, the frequency is stepped up to (140 - 220) GHz using the "ZC220 Millimeter Wave Converter" from *rohde & Schwarz* company [90].

Figure 4.34 shows the test bench used in order to characterize the G-band power source. The maximum power of this source ($P_{max}{}'$) is measured using mmW power meter (PM5 calorimeter from VDI company [91]) for several frequencies (as shown in figure 4.35). The variable attenuator (in the frequency converter) is used to sweep the output power ($P_{in}{}'_{(dBm)} = P_{max}{}'_{(dBm)}$ - attenuating factor $_{(dB)}$).

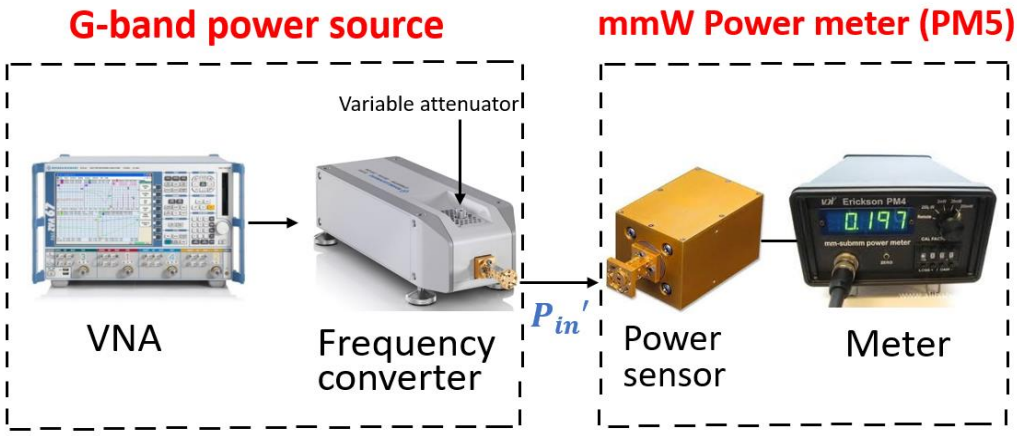


Figure 4.34 The test bench used to characterize the G-band power source.

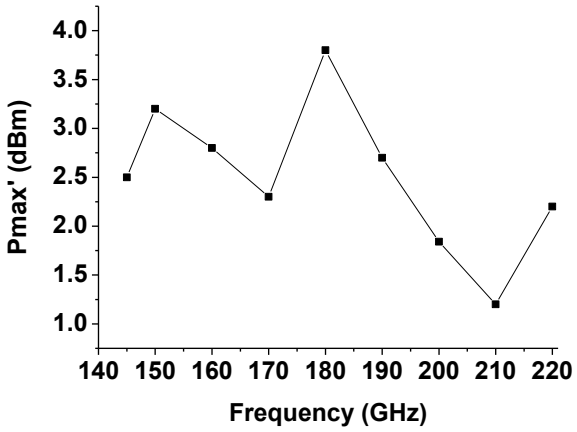


Figure 4.35 The measurements of the maximum output power of the G-band source.

Several output power levels ($P_{in}{}' < P_{max}{}'$) are also measured to verify the functionality of the attenuator.

D. Measurement of voltage sensitivity γ

The extraction of the voltage sensitivity values is done using the bench shown in figure 4.36. The G-band power source is used to inject the input power signal in the frequency band (140 - 220) GHz. The detector is probed using the coplanar probe I220 from infinity [92]. The output DC voltage of the detector is measured using the voltmeter Agilent 34461A via the DC output of the probe (using the integrated T bias). The power at the plane $P_{in}{}'$ is already measured (as explained in the previous section). In order to shift the reference power plane from $P_{in}{}'$ to P_{in} , the losses of the input probe are subtracted from the injected power $P_{in}{}'$.

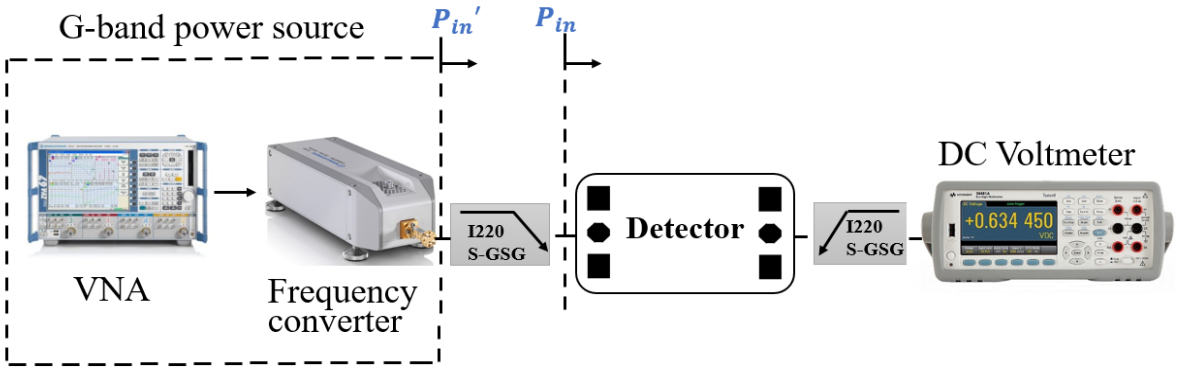


Figure 4.36 The test bench used to extract the voltage sensitivity values of the frequency compensated detector in G- band.

Figure 4.37 shows the measured and simulated sensitivity curves versus frequency, where several conclusions can be mentionend:

- The frequency effect in the simulation is completely compensated all over the G-band (the sensisitivity value γ is nearly constant over the frequency).
- Based on the measurments, the frequency effect is compensated all over the G-band (γ= 1800 V/W $\pm$10%), on the other hand, this value (γ) is nearly constant in the frequency band (160 - 200) GHz.
- In the frequencies 145 GHz and (210 - 220) GHz, the measured sensitivity values are in a good agreement with the simulation, this is because the measured and

simulated R_{att} values of the attenuator are very close (figure 4.33 (a)). In the frequency band (160 - 200) GHz, smaller R_{att} values are obtained in the measurements as compared to the simulation, consequently, higher γ values are produced (2000 V/W).

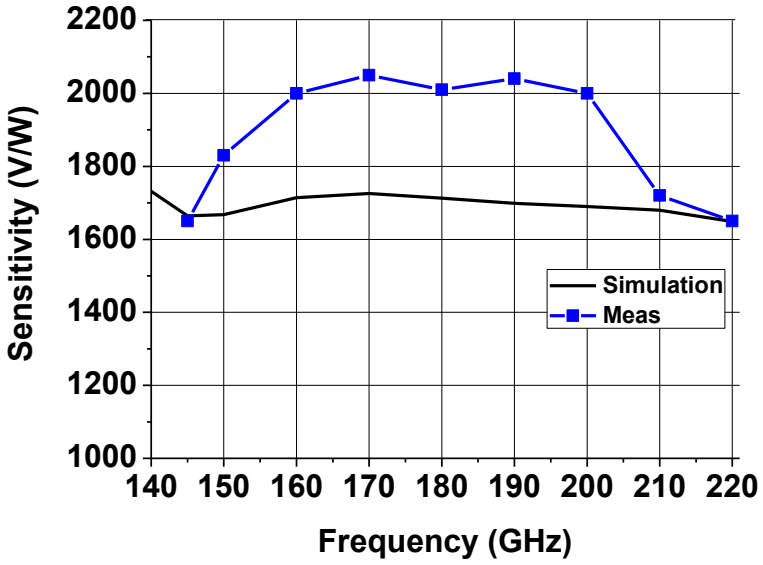


Figure 4.37 The measured and simulated voltage sensitivity curves vs frequency of the frequency compensated detector in G-band, at P_{in}= -25 dBm.

In order to determine the compression point (P_{in_max}), the sensitivity values are measured for different input power levels at 180 GHz and 220 GHz (as shown in figurer 4.38).

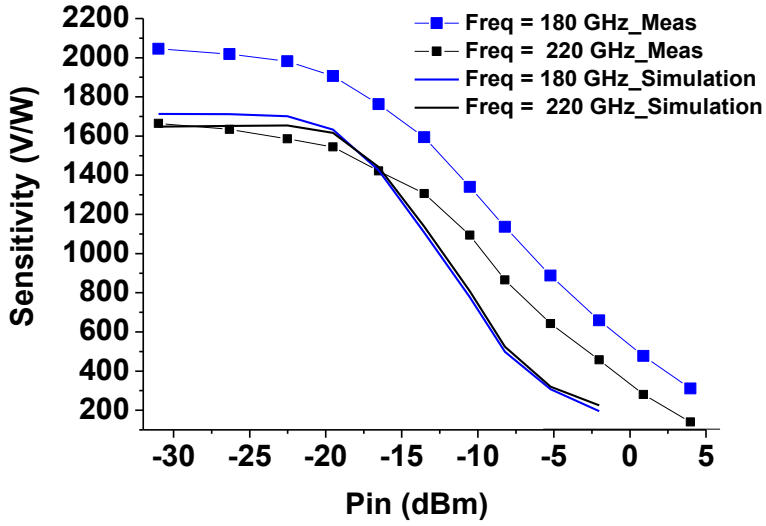


Figure 4.38 The simulated and measured voltage sensitivity curves vs input power of the frequency compensated detector in G-band at 180 GHz and 220 GHz.

E. The extracted detector parameters

The values of R_V, NEP, P_{in_min} and FOM are extracted using the equations 4.5, 2.14, 2.22 as in the previews paragraphs. The following table summarizes the extracted parameters for the frequency compensated detector in G-band at 180 GHz and 220 GHz.

Frequency (GHz)	R_V (kΩ)	P_{in_min} @ CW (dBm)	NEP (pW/$\sqrt{Hz}$)	P_{in_max} (dBm)	Dy (dB)	γ (V/W)	FOM (V/W)
180	5	-83.41	4.56	-18	65.4	2000	666
220	5	-82.57	5.53	- 17	65.5	1650	559

Table 4.6 The extracted parameters of the frequency compensated detector in G-band at 180 GHz and 220 GHz.

The detector has higher sensitivity value (2000 V/W)) at 180 GHz, thus, the compression point (P_{in_max}) occurs at lower power level (-18 dBm).

4.3.4 State of the art

The performance of the frequency compensated detector in G-band is compared to some commercial detectors and other recent works in table 4.7. The performance of this detector is belong the current state of the art exhibiting very low NEP value with relatively high sensitivity levels. In addition, it provides a broadband detection by covering all the frequencies in the G-band.

Ref.	Technology	Freq. (GHz)	NEP (pW/$\sqrt{Hz}$)	Sensitivity (kV/W)
[93]	Commercial ELVA	110 - 170	-	150 @ 170 GHz
[94]	130-nm CMOS (SBD)	265 -295	33 @ 280 GHz	0.25 @ 280 GHz
[95]	Commercial Quinstar	110 - 170	-	250 @ 170 GHz
[96]	Commercial CMOS	_	31 @ 297 GHz	0.55 @ 297 GHz
[97]	Commercial VDI (SBD)	140 - 220	1.5 @ 150 GHz	4 @ 150 GHz
This work	55-nm BiCMOS (MOSFET)	140 - 220	4.56 @ 180 GHz 5.53 @ 220 GHz	2 @ 180 GHz 1.65 @ 220 GHz

Table 4.7 The state of the art of power detectors for the frequency band (140 – 320) GHz.

4.4 THz power detector

In this work, a power detector integrated in the technology 55-nm BiCMOS is designed in the frequency band (450 - 600) GHz, for THz applications (such as THz imaging). The frequency effect is compensated (as in the G-band detector) all over the frequency of interest.

Figure 4.39 shows the schematic of the THz detector. The transistor T_2 is used to rectify the THz signal. The transistor T_1 is used to absorb part of the input power. The stubs l1, l2 and the DC block capacitor help to match the detector. At such high frequencies, this capacitor acts as an inductive element, where its fingers become as small transmission lines, this help to vary the real part impedance (real(Z_X) in figure 4.39) with the frequency.

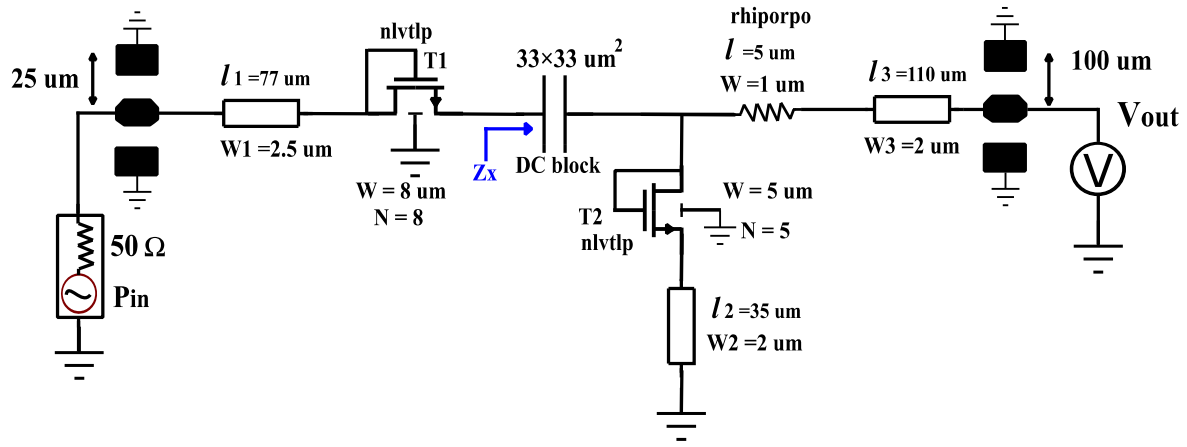


Figure 4.39 The schematic of the THz detector.

The value of the DC block capacitor is tuned so the real(Z_X) value increases with the frequency. Consequently, as the frequency increases, higher level of power is delivered to the transistor T_2 and smaller power is absorbed in the transistor (T_1). Therefore, the frequency effect is compensated. The resistor rhiporpo (of 30 kΩ) is used to isolate the detector output at high frequencies.

Figures 4.40, 4.41 show the simulated S_{11} parameters and the voltage sensitivity values in the frequency band (450 - 600) GHz.

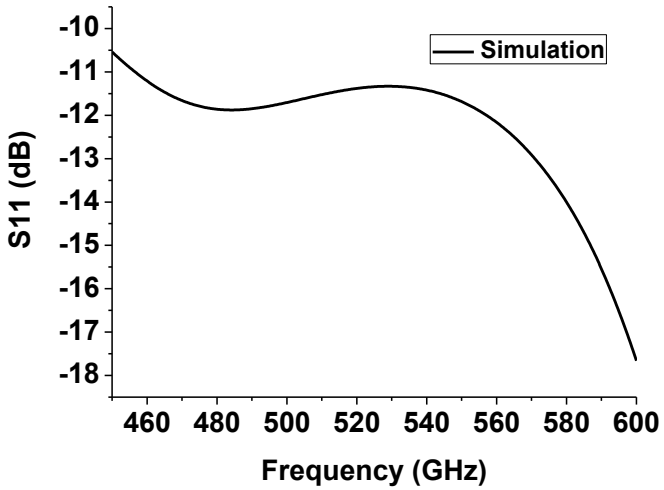


Figure 4.40 The simulated S_{11} parameters of the THz detector.

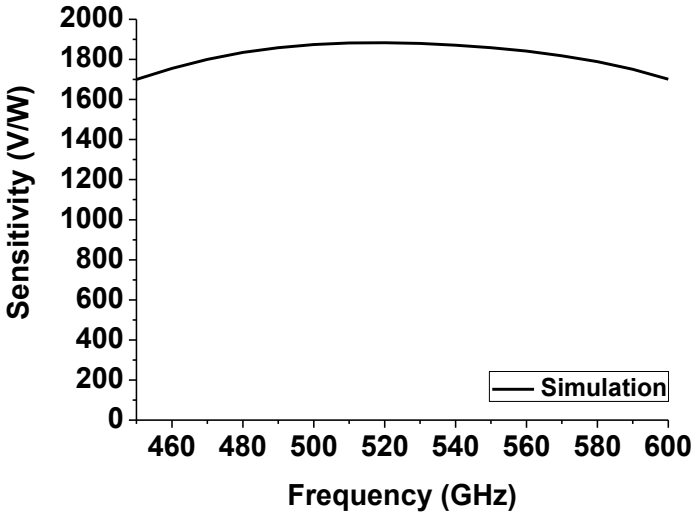


Figure 4.41 The simulated voltage sensitivity curve versus frequency of the THz detector.

The simulation shows that the detector is matched ($|S_{11}|$ < -10 dB), and the frequency effect is compensated for the all frequency band of interest, with relatively high sensitivity value ($\gamma = 1750$ V/W $\pm$ 2.5%). The characterization of this detector and the comparison with the state of the art of THz detectors are planned as future work.

4.5 Conclusion

In this chapter, the design and characterization of several zero bias detectors were presented in different frequency bands. For 5G applications, three detector topologies were presented in the frequency band (38 - 55) GHz:

- Detector based on single transistor, where three categories of NMOS transistor were used in order to compare their performances. The detector based of the HPA transistor exhibits the best performance comparing to the other categories.
- Detector based on stack of 6 transistors, which exhibits larger dynamic range (*Dy*), higher level of compression point (P_{in_max}), and better performance than the previews topology.
- Temperature compensated detector, which provides a robust performance against the temperature variations. The measurement results of this detector shows that the temperature effect is partially compensated.

A frequency compensated detector in G-band was designed, where the measured sensitivity value is (γ= 1800 V/W $\pm$10%) all over the frequency band of interest (140 - 220) GHz. Finally, a frequency compensated detector in the frequency band (450 - 600) GHz was also designed, where the simulated sensitivity value is (γ= 1750 V/W $\pm$2.5%) all over the frequency band of interest. The measurement of this detector is planned as future work.

General conclusions and future works

Power detector (PD) is considered as one of the most important circuit block in the microwave and millimeter wave systems, since it is the key block to establish the power measurement. So many applications can be mentioned where measuring the power is required. The most common applications of power measurement were discussed in chapter 1 (such as proof of design, regularity, improving the efficiency, THz applications..) showing the required detector parameters following each application. For example, in the envelope tracking technique (which is used to improve the efficiency of power amplifiers), a PD with minimum power consumption is required to take the full benefit of this technique. On the other hand, the applications at high frequencies (such as G-band and THz) require PDs with high sensitivity values, since the losses are relatively high.

Two types of power sensors were briefly presented (heat and diode based sensors) by discussing their principles, cons and pros of each type. The heat based sensors are able to measure the true RMS power with high accuracy by converting this power into heat. Consequently, the measurement is not affected by the waveform. For these reasons, heat based sensors are mainly used as reference power standards. However, their response is relatively slow, and so, they cannot be used to detect (extract) the fast variation of signal envelope. On the other hand, the diode based detector has fast response allowing to track the fast variation of signal envelope, and also, it can be easily integrated on chip with other circuits.

The basic circuit configuration of the diode based detector was presented by explaining the function of each element in this circuit. The detector parameters are also explained in detail showing the correlation between each other. Depending on the application, some detector parameters can be more important than others. For example, PD with large dynamic range is necessary to maintain the linear responses in the modern modulations, since their signals have high peak to average power ratios (PAPR). Due to the correlation between the detector parameters, some are usually sacrificed (or degraded) in order to improve (or make the trade-off with) others. For example,

using smaller size of zero bias diode can be used in order to produce higher sensitivity and smaller NEP values, however the dynamic range will be decreased.

In this work, several detector topologies have been designed and characterized in the frequency range (35 - 55) GHz, dedicated to 5G applications, integrated in the SiGe 55-nm BiCMOS technology from STMicroelectronics.

The first topology is tunable detector based on PN diode, where the biasing current can be controlled in order to adjust the detector parameters. This includes the video resistance (R_V), maximum input RF power (P_{in_max}), voltage sensitivity (γ), and power consumption (P_D). This characteristic makes the detector suitable for different 5G applications by providing adjustable parameters. The small signal model of the PN diode was extracted and validated up to 110 GHz in order to use it in the detector design. Two tunable detectors were designed based on two sizes of PN diode in order to compare their performances. The matching networks were configured to keep the detectors matched for large range of biasing current I_b (1 nA - 100 µA), providing (simulated) tunable sensitivity values (10 - 1500) V/W. A circuit block (named N-load) was added in series to the diode in order to absorb part of the input RF power (as an attenuator), and so maintain the linear response at higher power levels. The measured sensitivity values of the detectors are between (500 - 1400) V/W corresponding to the current range (100 nA – 10 µA), with very low power consumption (down to 60 nW).

The diode model was also extracted and validated for three temperatures (25°C, 60°C, 90°C), this will help to design a temperature compensated detector (based on this diode). The diode is biased by current source (instead of voltage source) since its small signal model becomes less sensitive to the temperature.

The second topology is zero bias detector (ZBD) based on single diode connected NMOS transistor. The ZBDs can be very advantageous in the 5G and IoT applications, where the power efficiency and the autonomy are required. Three detectors were designed based on three categories of NMOS (GP, LP, HPA), in order to compare their performances. The HPA transistor exhibited the best performance which is belong the current state of the art, with very low NEP value (3.8 pW/$\sqrt{Hz}$) and large dynamic range (67 dB).

The third topology is ZBD based on stack of 6 transistors. Each transistor absorbs part of the input power, thus the compression point (P_{in_max}) is extended without decreasing the sensitivity. Based on the measurements, relatively high sensitivity (1380 V/W) and P_{in_max} (-12 dBm) levels are obtained. On the other hand, high level of noise (NEP) is generated by the transistor stack (the extracted NEP value is 485 pW/$\sqrt{Hz}$), which is considered as the drawback of this topology.

The forth topology is temperature compensated ZBD. The temperature effect is compensated in real-time using an innovative passive circuit. This circuit is connected in parallel with the NMOS acting as a PTC resistor. As the temperature increases, higher power is delivered to the NMOS, and so, the sensitivity value is compensated. Based on the measurements, the sensitivity values are between (1400 - 1650) V/W in the temperature range (20 - 90)°C at 43 GHz.

A frequency compensated PD was designed and characterized for higher frequencies (G-band, 140 - 220 GHz) using the same technology. This PD can be integrated on chip with the digital circuits, increasing the efficiency of power measurements at such high frequencies. The frequency effect is compensated in real-time using an innovative passive circuit. This circuit is connected in series with the NMOS acting as a self-varied attenuator, where the attenuation factor decreases with frequency. Based on the measurements, the sensitivity value is compensated (γ= 1800 V/W $\pm$10%) showing small variation all over the G- band frequencies.

Finally, a frequency compensated PD was also designed in the frequency bands (450 - 600) GHz for THz applications (such as THz imaging). Based on the simulation, the sensitivity value is compensated (γ= 1750 V/W $\pm$ 2.5%) showing very small variation all over the frequency band of interest (450 - 600) GHz.

In the frame of finalizing this work, several future works were planned:

- Since the flicker noise is dominant in the tunable detector (at DC and baseband frequencies), the NEP value could not be estimated. Therefore, this value will be measured in order to determine the minimum detectable power (P_{in_min}) and the dynamic range (*Dy*).

- The detectors performances of this work were investigated for continues wave detection (CW). These detectors will be characterized using modulated signals (such as AM and pulse signals) in order to fulfill the need of real-world applications (such as 5G and pulse detection in radar applications). In order to do that, a capacitor will be added to the detector output forming a (RC) low pass filter with the video resistance.
- In the temperature compensated PD, the measured variation ratio ($\Delta R_{PTC}/\Delta T$) is smaller than the simulation, thus the temperate effect (in the measured sensitivity values) is partially compensated. The detector can be modified to exhibit a complete temperature compensation by tuning the value of the capacitor C_x.
- The heat based detector (designed by the LNE laboratory) will be used in order to calibrate the detectors of this work. This can be done by making direct comparisons between the results given from the heat and diode based detectors, for the same input RF power.
- The THz detector is under fabrication, the characterization and the comparison with other recent works will be done in the future work.
- Design a feature to integrate the G-band detector in a package. Hence, this detector can be used in power measurement benches at the G-band frequencies.
- Executing post-layout simulation (or electromagnetic simulation) in order to take into account the T effects in the future detector design.
- Since the HPA transistor exhibits small video resistance and high performance, it will be employed in a rectenna for wireless energy harvesting.

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List of Publications

Publications in international journals

I. Alaji *et al.*, "Design of tunable power detector towards 5G applications," *Microw. Opt. Technol. Lett.*, no. mop.32685, 2020.

H. Ghanem et al., "Modeling and analysis of a broadband Schottky diode noise source up to 325 GHz based on 55-nm SiGe BiCMOS technology," IEEE Trans. Microw. Theory Tech., vol. 68, no. 6, pp. 2268–2277, 2020.

I. Alaji et al., "Design and characterization of (140-220) GHz frequency compensated power detector," IEEE Trans. Microw. Theory Tech. (under review).

I. Alaji et al., " Design of zero bias power detectors towards 5G applications," Microelectronics journal. (under review).

International communications with panel review

J. C. Azevedo Goncalves *et al.*, "On wafer millimetre wave power detection using a PN junction diode in BiCMOS 55 nm for in-situ large signal characterization," in *2018 48th European Microwave Conference (EuMC)*, 2018, pp. 37–40.

J. C. Azevedo Goncalves et al., "Investigating the potential of SiGe Diode in BiCMOS 55nm for power detection and datacom applications at 300 GHz," in 2018 43rd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz), 2018

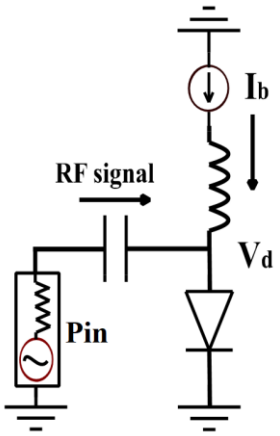
International communications without panel review

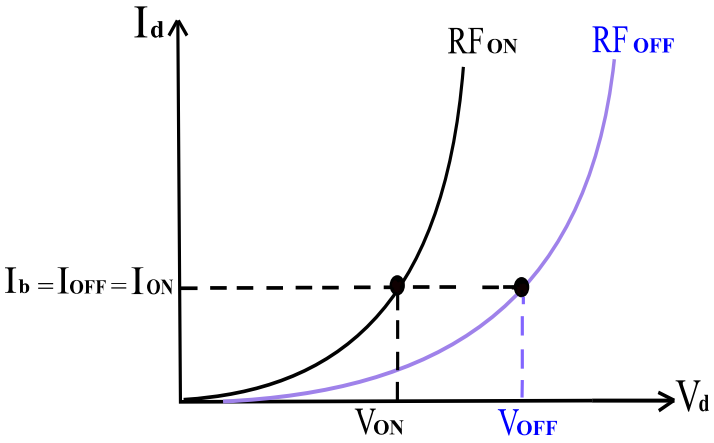
I.Alaji, D. Gloria, G. Ducournau and C. Gaquière «Power detection based on Silicon Schottky diode for 5G and THz applications» Workshop, European Microwave Week 2019, Paris, France.

National communications with panel review

I.Alaji, J. Goncalves, W. Aouimeur, H. Ghanem, D. Gloria, G. Ducournau, et C. Gaquière «Détection de puissance sur wafer à l'aide d'une diode PN pour les applications THz», JNM 2019, Caen, France.

Annex 1





The diode voltage is composed of DC and RF voltages:

$$V_d = V_{DC} + V_{RF} = V_{DC} + A.\cos(wt)$$

$$I = I_S.[\exp(V_d / n.V_T) - 1] \approx I = I_S.\exp(V_d / n.V_T) \quad \text{Where} \quad I >> I_S$$

$$\Rightarrow I = I_S.\exp(V_{DC} / n.V_T).\exp(A.\cos(wt) / n.V_T) \Rightarrow \quad I = I_{DC}\exp(A.\cos(wt) / n.V_T)$$

Using Taylor series $\exp(x) = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + ...$

$$I = I_{DC}(1 + \frac{A^2}{4n^2.V_T^2} + \frac{A^4}{66.6n^4.V_T^4} + \frac{A^6}{2325n^6.V_T^6} + ...) \quad .....(*)$$

$$+ I_{DC}(\frac{A}{n.V_T} + \frac{A^3}{8n^3.V_T^3} + \frac{A^5}{192n^5.V_T^5} + ...)\cos(wt)$$

$$+ I_{DC}(\frac{A^2}{4n^2.V_T^2} + \frac{A^4}{50n^4.V_T^4} + \frac{A^6}{1538n^6.V_T^6} + ...)\cos(2wt) + ...$$

When RF power P_{in} is OFF, and the biasing current is I_b

$$\Rightarrow I_{OFF} = I_b = I_S.\exp(V_{OFF} / n.V_T)$$

$$\Rightarrow V_{OFF} = n.V_T.[\ln(I_b) - \ln(I_S)]$$

When low level of RF power is applied (RF ON) while maintaining the DC biasing current I_b, this current can be expressed as the following:

$$\Rightarrow I_{ON} = I_b = I_{DC}(1+\frac{A^2}{4n^2.V_T^2}) \quad \Rightarrow I_{ON} = I_S.\exp(V_{ON}/n.V_T).(1+\frac{A^2}{4n^2.V_T^2})$$

$$\Rightarrow I_{ON} = I_S'.\exp(V_{ON}/n.V_T) \quad \text{where} \quad I_S' = I_S.(1+\frac{A^2}{4n^2.V_T^2})$$

$$\Rightarrow V_{ON} = n.V_T.[\ln(I_b)-\ln(I_S')] \quad \Rightarrow \quad V_{OFF}-V_{ON} = n.V_T.[\ln(I_S')-\ln(I_S)]$$

$$\Rightarrow V_{OFF}-V_{ON} = n.V_T.\ln(1+\frac{A^2}{4n^2.V_T^2}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \;(**)$$

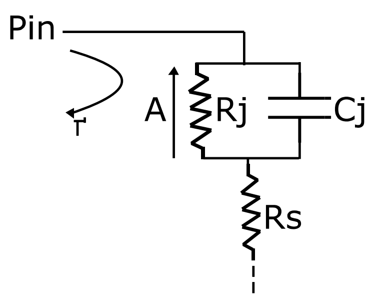
Using the logarithmic series $\ln(1+x) = x-\frac{x^2}{2}+\frac{x^3}{3}-\frac{x^4}{4}+\ldots$

$$\Rightarrow V_{OFF}-V_{ON} = n.V_T.(\frac{A^2}{4n^2.V_T^2}-\frac{A^4}{32n^4.V_T^4}+\frac{A^6}{192n^6.V_T^6}-\ldots.)$$

For low level of RF power $\Rightarrow$ $V_{OFF}-V_{ON} \approx n.V_T.(\frac{A^2}{4n^2.V_T^2})$

Intrinsic sensitivity $\Rightarrow$ $\gamma_{Intrinsic} = \frac{V_{OFF}-V_{ON}}{P_{in}} \approx \frac{n.V_T}{P_{in}}.(\frac{A^2}{4n^2.V_T^2}) = \frac{1}{P_{in}}.(\frac{A^2}{4n\ .V_T})$

$$\gamma_{Intrinsic} \approx \frac{1}{P_{in}}\left(\frac{2.R_j.P_j}{4n\ .V_T}\right) = \frac{1}{P_{in}}\left(\frac{2.R_j.X.P_{in}}{4n\ .V_T}\right)$$



Where $P_j = X.P_{in}$

P_j is the power absorbed in the diode junction, X is the ratio between the input power and the power absorbed in the junction. This ratio depends on the matching condition (Γ) and the power division between the diode and other elements in the circuit.

$$\Rightarrow \boxed{\gamma_{Intrinsic} \approx \frac{R_j.X}{2.n\ .V_T}}$$

This value represents the intrinsic sensitivity (the response of the junction only) for low levels of power P_{in}.

Annex 2

In the following, we present the development of the proposed formula which can mathematically linearize the detector response at higher level of RF power.

For high level of RF power, the equation (**) in Annex 1 can be written as the following (where all the polynomial terms are taken into account):

$$V_{OFF} - V_{ON} = n.V_T.\ln(1 + \frac{A^2}{4n^2.V_T^2} + \frac{A^4}{66.6n^4.V_T^4} + \frac{A^6}{2325n^6.V_T^6} + ...)$$

And can also be expressed as : $Delta = n.V_T.\ln(1 + i1 + i2 + i3...)$ ……..…….(***)

$$\Rightarrow \exp\left(\frac{V_{OFF} - V_{ON}}{n.V_T}\right) = 1 + \frac{A^2}{4n^2.V_T^2} + \frac{A^4}{66.6n^4.V_T^4} + \frac{A^6}{2325n^6.V_T^6} + ...$$

$$\Rightarrow 0.5.\exp\left(\frac{V_{OFF} - V_{ON}}{n.V_T}\right) = 0.5 + \frac{0.5A^2}{4n^2.V_T^2} + \frac{0.5A^4}{66.6n^4.V_T^4} + \frac{0.5A^6}{2325n^6.V_T^6} + ...$$

The RF amplitude A becomes smaller ($0.5A^2$ instead of A^2 in the first term)

$$\Rightarrow 0.5 + 0.5.\exp\left(\frac{V_{OFF} - V_{ON}}{n.V_T}\right) = 1 + \frac{0.5A^2}{4n^2.V_T^2} + \frac{0.5A^4}{66.6n^4.V_T^4} + \frac{0.5A^6}{2325n^6.V_T^6} + ...$$

$$\Rightarrow 0.5 + 0.5.\exp\left(\frac{V_{OFF} - V_{ON}}{n.V_T}\right) = 1 + i1' + i2' + i3' + ...$$

$$\Rightarrow Delta' = n.V_T.\ln(1 + i1' + i2' + i3'...)$$

$$\Rightarrow Delta' = 2.n.V_T.\ln\left(0.5 + 0.5.\exp\left(\frac{V_{OFF} - V_{ON}}{n.V_T}\right)\right)$$

(Where the factor 2 is added to compensate the diminution of the A value).

Design and characterization of power detectors in 55-nm BiCMOS technology for 5G and THz applications

Abstract Power detectors are the key blocks to establish the power measurement. Therefore, they are considered among the most important circuits in many microwave and millimeter wave applications (such as communication systems, medical equipments, radar systems, etc.). In this context, this thesis presents the design, characterization and theoretical analysis of different diode based power detectors, built in 55nm-BiCMOS technology from STMicroelectronics, in different frequency bands, towards different applications. For 5G applications in the frequency band (35-55) GHz, tunable detectors are designed to be used in different applications, since their parameters can be adjusted. In addition, several topologies of zero bias detectors are designed to help improving the efficiency in the 5G and IoT devices. This can be realized by employing those detectors in envelop tracking circuits which reduce the power consumption of power amplifiers. Two frequency compensated detectors in the frequency bands (140-220) GHz and (450-600) GHz are designed providing stable and high sensitivity value over the whole frequency band of interest. These detectors can be used for on-chip power detection which helps increasing the power measurement efficiency at such high frequencies. These detectors can be also used in THz applications such as THz imaging and radars. Some detectors in this work reach the state of the art performances in several frequency bands, thanks to their original designs executed in STMicroelectronics technology.

Keywords: *5G and IoT sensors, BiCMOS integrated circuits, frequency compensated power detector, millimeter waves, tunable power detector, zero bias power detector.*

Résumé Les détecteurs de puissance sont les blocs clés pour établir la mesure de puissance. Par conséquent, ils sont considérés parmi les circuits les plus importants dans de nombreuses applications micro-ondes et ondes millimétriques (telles que les systèmes de télécommunication, les équipements médicaux, les systèmes radar, etc.). Dans ce contexte, ce manuscrit présente la conception, la caractérisation et l'analyse théorique de différents détecteurs de puissance basés sur la technologie BiCMOS 55-nm de STMicroelectronics, dans différentes bandes de fréquences, et cela pour plusieurs applications. Pour les applications 5G dans la bande (35-55) GHz, des détecteurs ajustables sont conçus pour être utilisés dans différentes domaines, surtout que leurs paramètres peuvent être ajustés. En outre, plusieurs topologies de détecteurs non polarisés sont conçues pour aider à améliorer l'efficacité énergétique des équipements 5G comme IoT. Cela peut être réalisé en utilisant ces détecteurs dans des circuits d'«envelope tracking» qui réduisent la consommation d'énergie des amplificateurs de puissance. Deux détecteurs à fréquence compensée dans les bandes de fréquences (140-220) GHz et (450-600) GHz sont conçus pour fournir une valeur de sensibilité stable et élevée sur toute la bande passante d'intérêt. Ces détecteurs peuvent être utilisés pour la mesure de puissance sur puce pour augmenter l'efficacité de mesure à telles fréquences élevées. Ces détecteurs peuvent également être utilisés dans des applications THz telles que l'imagerie THz et les radars. Certains détecteurs de ce travail atteignent des performances à l'état de l'art dans plusieurs bandes de fréquences, cela grâce à leurs conceptions originales exécutées en technologie STMicroelectronics.

Mots clés: *Capteurs 5G et IoT, circuits intégrés BiCMOS, détecteur de puissance à fréquence compensée, ondes millimétriques, détecteur de puissance ajustable, détecteur de puissance non polarisé.*